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Eliana Isabel Arango Zuluaga

MODELLING AND CONTROL OF AN ASYMMETRIC INTERLEAVED DC TO DC SWITCHING CONVERTER

Doctoral Thesis

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Departament d'Enginyeria Electrónica Elèctrica i Automàtica

UNIVERSITAT ROVIRA I VIRGILI

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We, Javier Calvente Calvo and Roberto Giral Castillón, associate professors in the Department of Electronics, Electric and Automatic Engineering of the Rovira i Virgili University,

CERTIFY:

That the present work, entitled "Modelling and Control of an Asymmetric Interleaved DC to DC Switching Converter", submitted by Eliana Isabel Arango Zuluaga for the award of the degree of Doctor, has been carried out under our supervision at the Department of Electronics, Electric and Automatic Engineering of this university.

Tarragona, April 20th, 2009.

.... Javier Calvente Calvo, PhD.

.... Roberto Giral Castillón, PhD.

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Me dio el corazón que agita su marco:
¡Cuando miro el fruto del cerebro humano!
¡Gracias a la vida!...
¡Gracias a la vida!"

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ABSTRACT

The two main topics presented in this thesis are the generation and mathematical modelling of new converter structures.

The fundamental idea behind the methodology used to generate the new converter structures was to break the symmetry. This involved modifying the circuit structure on the basis of the simulation results. This methodology allowed the generation of the family of asymmetrical interleaved converters, which consists of the AIDB, the AIDBB and the AIDF-group.

A new conceptual modelling approach was developed on the basis of ideas taken from previous research which is reviewed in the state of the art. This approach was called Modified Averaging Using Graphical Methods. Because of its features, this new method can be used to model the state space average of the new converter family presented here.

The accuracy of the AIDB converter small signal model was verified by measuring the frequency response and by designing an LQR controller.

RESUMEN

La generación de nuevas estructuras convertidoras y su modelado matemático son las dos temáticas principales estudiadas en esta tesis.

El seguimiento de una metodología que modifica la estructura del circuito, realizando una ruptura de la simetría con base en los resultados de simulación, permitió generar la familia de convertidores en “interleaving” asimétrico compuesta por el AIDB, el AIDBB y el grupo-AIDF.

En el apartado de modelado se ha desarrollado una nueva aproximación conceptual inspirada en las ideas de trabajos previos que se estudian en el estado del arte. El nombre dado a esta nueva aproximación es: Promediado Modificado Usando Métodos Gráficos. Este nuevo enfoque ha sido utilizado para obtener el modelo promediado de la nueva familia de convertidores en el espacio de estados.

Las mediciones experimentales de la respuesta en frecuencia del convertidor AIDB y el diseño del controlador LQR permitieron verificar la aproximación del modelo en pequeña señal obtenido.

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INTRODUCTION

A continuing objective in the field of power electronics is to generate new and improved structures of switching converter circuits.

The work presented here, as its title suggests, begins with the development of a new converter structure with interesting features in order to increase its range of possible applications.

The starting point of this development is a structure designed in a previous thesis that will be studied at the beginning of Chapter Two. Then, a new converter is developed using a methodology that will also be described in detail in that chapter.

The converter is named the Asymmetrical Interleaved Dual Boost Converter (AIDB) for two reasons: the methodology used in its development and its operation features.

Other converter circuits with similar characteristics to the AIDB are developed by applying the same methodology to different basic converters. The advantages of the entire family of Asymmetrical Interleaved Converter Circuits are verified by simulation, as will be seen in Chapter Two.

The initial goal was to make a mathematical analysis of the new converter to further explore the characteristics of the plant and to obtain the model-based controller that would allow the output voltage to be regulated in the presence of disturbances. The first attempts to achieve this goal involved mathematical modelling using the traditional method of state space averaging; however, this did not provide suitable results.

After that, it was decided to focus this thesis on the issue of converters modelling and to begin a comprehensive study of the state of the art in this field. The initial aim was to find a method that would allow the converter modelling. However a second objective was achieved with this global review: enough information in this field that provides the basis for developing a new mathematical modelling approach.

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Therefore, the first chapter of this thesis will present a brief introduction into general aspects of converters followed by this exhaustive study of modelling methods in continuous conduction mode (CCM) and discontinuous conduction mode (DCM).

The first chapter will also include a review of methods for classifying and generating DC-to-DC converters in PWM because the original aim of this study was to generate a new converter structure. Some analytical approaches are described at the beginning because they are the basis of almost all the most popular DC-to-DC converters circuits used nowadays. After this, another approach to the generation of new converter structures is revised, this providing the starting point of the new converter developed in this study.

That chapter also presents a review of the conduction modes of converters because the new converter family generated shows an unusual combination of conduction modes, resulting in the interesting behaviour that gives the name to the family.

Specifically in the case of modelling methods in DCM, the review concludes with the study of the more recent work in this area. Its contributions were the inspiration for the changes introduced in the traditional averaging method that will be developed in the third chapter.

The second chapter of this thesis explores the method of generating the new converter structure and shows the results obtained by the simulations and by the measurements with the experimental prototype. The simulations were made for both the first new converter and the new family of converters that had been generated using the same methodology but starting from other basic circuits. These results are useful for determining the advantages of the new converter family.

This chapter also describes the first approximation of the steady state analysis and the comparison of the AIDB converter's open loop experimental results with those obtained in simulations.

The third chapter is the central chapter of this thesis and describes the procedure followed in obtaining the new modelling approach based on graphical methods. The chapter presents the mathematical calculations used to find the state space averaged model of the converter through the new modified approach. It will also describe the steady state analysis and the linearized small-signal model around an operating point.

Some comparisons are then made between the results obtained by each of the modelling methods in the time domain. The comparisons in the frequency domain include the experimental measurements made in open loop using the frequency response analyzer.

The new modelling approach is also used to find the small signal model of the new family of asymmetrical interleaved converters, the results being shown in the third chapter.

The fourth chapter makes use of the recently calculated small signal model of the AIDB converter for the controllability calculation and the Linear Quadratic Regulator (LQR) control design.

This chapter will also present the simulation results of the interconnection of the AIDB controlled converter with a Fuel Cell, an application that is possible because of certain features inherent in the AIDB converter. The simulation results will allow an initial verification to be made using the simulations of the converter operation with a model of a real source.

Finally, the conclusions of the thesis will be presented and will suggest possible areas for future research on the basis of the results obtained in this thesis.

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CHAPTER 1

STATE OF THE ART:

GENERATION AND MODELLING OF DC-TO-DC SWITCHING CONVERTERS

Power conversion emerged as an interdisciplinary field that requires a fundamental knowledge in several areas: power circuit configurations, mathematical modelling, control systems, electronic devices, and magnetic circuits. In its beginnings, there were two alternatives for the power delivery from a DC source to a load in a controllable manner: linear and switched mode power conversion. Usually, linear power conversion relies on the presence of a series linear element (resistor or transistor in linear mode) such that the total load current is passed through the series linear element. The main disadvantage of this conversion is the inefficiency, because even in its ideal form its efficiency ranges from 30 % to 60 %. On the contrary in the switched mode power conversion, where the controlling device is an ideal switch, the power flow to the load can be controlled in a very efficient way. Ideally its efficiency is almost 100 % even for a wide range of power being controlled [1].

Nowadays, the use of the switched mode power converters is widely generalized. It is the preferred way to provide power processing for different applications going from computing and communications to medical electronics, appliance control, transportation, renewable sources and high-power transmission. The associated power levels extend from milliwatts to megawatts in function of the application. Therefore, the design, analysis, modelling, and control of the switching power converters constantly present new and significant challenges to be achieved [2].

This chapter is mainly a bibliographic journey through two aspects of DC-to-DC switched mode power conversion: circuit structures generation and its mathematical modelling. The first section is an introduction to some elementary aspects of DC-to-DC switching converters, the second studies the new structures generation and classification, the third explains the operating modes and the final section is an overview in converters modelling and simulation.

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1.1 ELEMENTARY ASPECTS OF DC-TO-DC SWITCHING CONVERTERS

The power conversion and control function in switching converter circuits requires the use of semiconductor switches such as thyristors, MOSFETs and diodes, as its basic components. The need to generate a DC output voltage introduces passive storage elements such as inductors and capacitors whose role is to smooth out the inherent pulsating behaviour originated from the switching action. Sometimes, transformers are also used for isolation. Due to the many possibilities of combining these elements, a great variety of converter structures is possible, but taking into account that they have to form effectively a low pass filter in order to achieve the basic DC-to-DC conversion function [1].

In general one converter has power input and control input ports, and a power output port as can be seen in Figure 1.1. The raw input power is processed as specified by the control input, yielding the conditioned output power. Specifically in a DC-to-DC converter, the DC input voltage is converted into a DC output voltage having a larger or smaller magnitude, possibly with opposite polarity or with isolation of the input and output ground references. Furthermore, an accurate control is undeniably required, since a well-regulated output voltage in the presence of variations of the input voltage and load current is desired. Moreover, high efficiency is one of the main goals in the designer's work [3].

In the next subsection, the boost converter will be studied in detail, in order to present the nomenclature.

1.1.1 THE PWM CONTROLLED BOOST CONVERTER

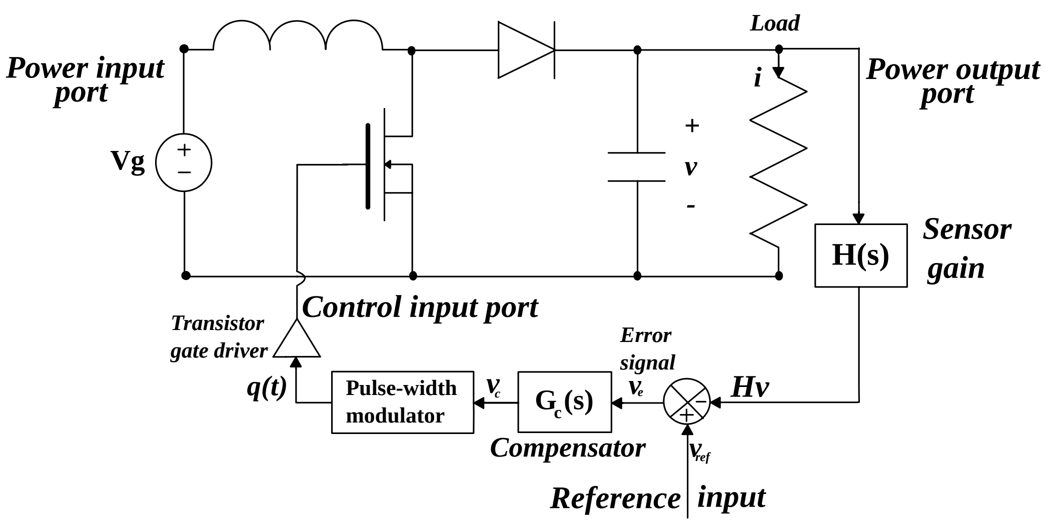

Figure 1.1: The boost converter with PWM control

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The Figure 1.1 shows a basic step-up (boost) converter structure capable of producing a DC output voltage greater in magnitude than the DC input voltage. This structure utilizes only switches, inductors and capacitors. The switches are realized using power semiconductors devices, such as transistors and diodes. The transistors are controlled to turn on and off as required to perform the function of the ideal switch that can be seen in Figure 1.2. For simplicity, in the analysis to be performed the switches are supposed to be non dissipative and the switching frequency f_s (inverse of the switching period T_s) to be a constant. That frequency generally lies in the range of *1 kHz* to *1 MHz*, depending on the switching speed of the semiconductor devices. The duty ratio D is the fraction of time the switch spends in position 1, and is a number between zero and one. The complement of the duty ratio D' is defined as $(1-D)$. In general, the duty ratio is a variable $d_k(t)$ that can change its value every *kth* cycle to fit itself to the requirements of the control signal.

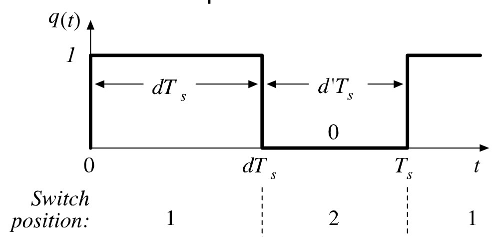

Figure 1.2: The function of the ideal switch

The boost converter in continuous conduction mode has two topologies of operation depending on the position of the switch, which can be observed in Figure 1.3. The inductor current waveform shows that the inductor L stores energy when the switch is in position “1” (from zero to DT_s seconds). This energy is transferred to the charge when the switch is in position “2” (from DT_s to T_s).

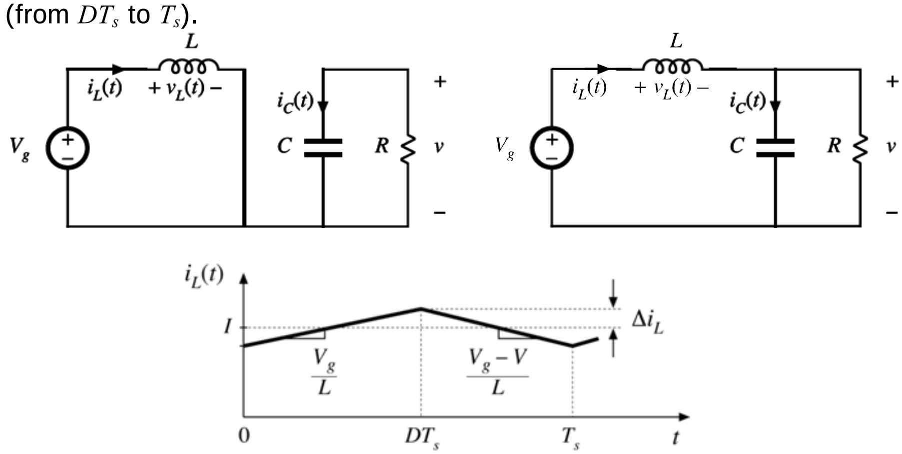

Figure 1.3: Topologies and inductor current waveform of the boost converter

Thus, the inductor voltage and current relationship are defined:

$$v_L(t) = L\frac{di_L(t)}{dt} \tag{1}$$

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When the switch is in position 1 the inductor voltage is V_g, and in position 2 the inductor voltage is $(V_g - V)$, where V is almost constant if the output ripple is small.

According to the principle of inductor volt-second balance [1], in periodic steady state, the net change in inductor current is zero, hence, the total area (or volt-seconds) under the inductor voltage waveform is zero whenever the converter operates in steady state. An equivalent form of this principle is that the average inductor voltage is zero in steady state.

Applying this principle over one switching period to the boost converter, it can be obtained

$$\int_{o}^{T_s} v_L(t)dt = (V_g)DT_s + (V_g - V)D'T_s \tag{2}$$

equating to zero, collecting terms and solving for V

$$V_g(D + D') - VD' = 0$$

$$V = \frac{V_g}{D'} \tag{3}$$

thus, the voltage conversion ratio is

$$M(D) = \frac{V}{V_g} = \frac{1}{D'} = \frac{1}{1-D} \tag{4}$$

The equation (4) shows that the output voltage magnitude can be controlled through the variation of the duty ratio. In the Figure 1.4 it can be seen the control characteristic of the boost converter calculated using equation (4) that allows the duty ratio D to be adjusted in order to regulate the converter output voltage using a compensator as in Figure 1.1.

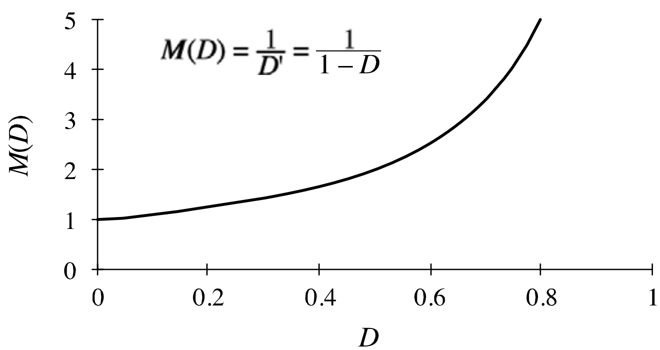

Figure 1.4: Boost converter control characteristic

The control of the duty ratio d, at constant switching frequency, is commonly called Pulse Width Modulation (PWM) control. As can be seen in the Figure 1.1, in order to obtain the control signal $v_c(t)$, the output voltage value is sensed (H_v) and compared with a reference input (v_{ref}). Then, the error signal $v_e(t)$ is applied to the input of a compensator and its output signal $v_c(t)$ is the modulation input of the PWM. Inside the PWM there is a comparator. The input to the "-" terminal of the comparator is a sawtooth waveform of period T_s that starts

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from 0 at the beginning of every cycle, and ramps up linearly to F by the end of the cycle. At some instant t_k in the kth cycle, this ramp crosses the level of the modulating signal $v_c(t)$ at the "+" terminal of the comparator. Hence, the output of the comparator is set to 1 every T_s seconds when the ramp restarts, and reset to 0 later in the cycle, at time t_k, when the ramp crosses $v_c(t)$. The duty ratio of the PWM output signal $q(t)$ thus ends up being $d_k=v_c(t)/F$ in the corresponding switching cycle. By varying the modulation signal $v_c(t)$ from cycle to cycle, the duty ratio can be varied. The PWM's output signal shown in Figure 1.2 is connected to the gate transistor driver that establishes the portion of time in which the circuit is ON, controlling in this way the output voltage magnitude, because it depends directly on the time that the converter is in ON state. Note that the samples $v_c(t_k)$ of $v_c(t)$ are what determine the duty ratio signal $q(t)$. In order to avoid the aliasing effect associated with sampling, the modulation signal is restricted to vary considerably more slowly than half the switching frequency. The modulating signal is usually generated by a feedback scheme as is shown by the input to the PWM in Figure 1.1.

The low pass capacitive filter would have to smooth the inherent pulsating behaviour of the output voltage originated from the switching action, and therefore generate an ideal DC output voltage. However the output voltage is not ideal, in addition to its DC component, it consists of a small ripple voltage component at the switching frequency f_s. From the frequency point of view, the PWM voltage waveform at the input of the low pass filter is divided into its DC component, harmonics at the switching frequency f_s, and its integer multiples harmonics by using Fourier series. The DC component passes unattenuated through the filter to generate the desired DC output. Given that the filter corner frequency is significantly lower than the switching frequency (typically at least a decade below f_s), the first and higher order harmonics are substantially attenuated by passing through the filter, resulting in an acceptably low switching ripple voltage at the output [1].

1.2 GENERATION AND CLASSIFICATION OF PWM DC-TO-DC CONVERTERS

One of the first studies on this subject was presented in [4] where the investigation of a variety of switching converters structures culminates in the establishment of the duality relationship, a general correlation law between the converter structures. The duality between converter structures can be observed in the dual nature of their components: inductors and capacitors, open and closed switches, input voltage and current sources, load resistance and load conductance. Starting from this law, new converter structures were generated by the application of the duality transformation to the existing converter configurations. In this way the duality between the buck and boost converters, and between the buck-boost and CUK converters is demonstrated as well. In addition to this duality other two topological properties were studied in that paper: inversion, in which the source and load interchange would result in an equally viable switching converter configuration, and symmetry, in which the source and load interchange results in the same configuration.

The study of more general approaches to the problem of the structure generation will be discussed in the next section

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1.2.1 THE CONVERTER CELL

In the literature there are a lot of DC-to-DC converter structures performing similar power processing functions, seemingly without a unifying connection between them. In [5] a fundamental block known as converter cell, whose diagram is in Figure 1.5, was used to generate basic converter structures. Therefore a relationship between basic converters was established. This converter cell can be used to analyze them too.

As Figure 1.5 describes, the converter cell is defined as the remaining network when the input source and output voltage sink are removed. Then, the result is a topological combination of reactive elements (*Ls* and *Cs*), and switches (actives and passives), where the duty cycle has the control of the output voltage.

The Figure 1.5 also shows that the converter cell is a three terminal device. Their terminals can be connected to the input source, output sink or common terminal in six different possible ways that correspond to the number of permutations of three. Therefore a family of six converters may be derived from each converter cell, except in the cases of symmetric cells, where the numbers of family members reduces down to three.

The converters that have this structure are DC-to-DC voltage converters without isolation. The Use of other strategies as isolation or interleaving allows the derivation of an infinite number of converters from these basic set.

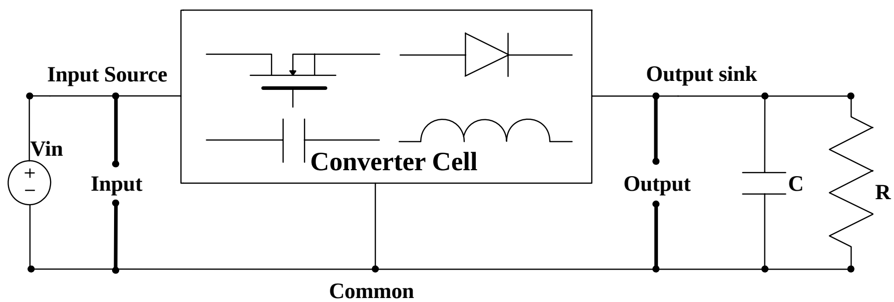

Figure 1.5: Converter Cell with ports indicated

A classification scheme of basic converters can be made in terms of converter-cell generated families. These converter cells were obtained without a formal synthesis procedure from known converters, and classified in four categories according to their order. The order indicates the number of storage elements and the number of switches used thus:

1) First-order, 2 switch: one type of converter cell as can be seen in Figure 1.6;
2) First-order, 4 switch: one possibility of converter cell.
3) Third-order, 2 switch: five types of converters cells, two of them in Figure 1.7;
4) Third-order, 4 switch: seven types of converter cells.

For example, the “Cell A” of the first category is the basic converter cell of the buck, boost and buck-boost converters that are the most well-known structures and can be seen in Figure 1.6.

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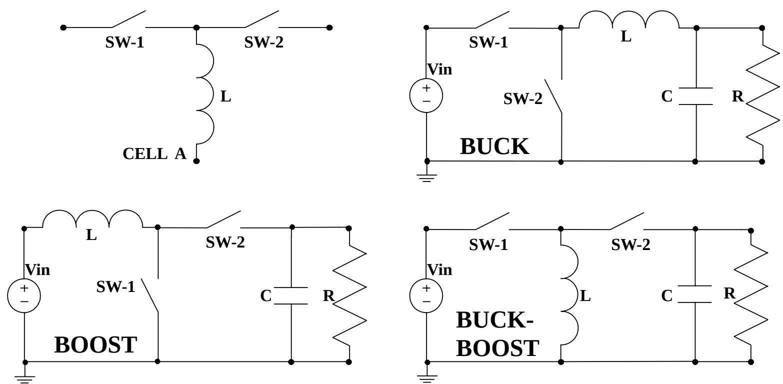

Figure 1.6: First order converters

Two examples of the third category are the “Cell C” and the “Cell G”, which are the basic converter cells of other known structures: the Cuk and SEPIC converters respectively. These structures can be seen in Figure 1.7.

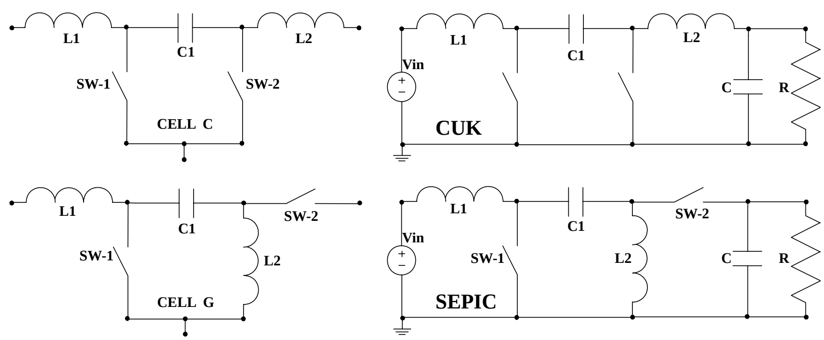

Figure 1.7: Third order converters

1.2.1.1 ANOTHER SCHEMES OF GENERATION AND CLASSIFICATION

Based on a formal definition of PWM converters, the study of the general topological constraints and properties of PWM converter networks made in [6] derivates completely formalized synthesis procedures that, in contrast to earlier approaches, guarantees the generation of complete sets of converters with prescribed attributes.

In the Chapter Two of [7] there is another detailed study of the generation and classification of DC-to-DC converters based on the converter cell. However in this case the generation of structures are also based on a set of synthesis rules that enables the refining of the process. The generated converters are classified first according to the number of nodes, and second, after the static analysis, according to the conversion ratio.

In [8] there is a classification scheme of a large class of PWM DC-to-DC, non isolated, and voltage to voltage converters of second and fourth order, that use only one transistor and one diode. The criteria used in the classification is based on the analysis of the linearized zero dynamics of the converter, which allows the observation of structure corrections in order to obtain a better dynamic behaviour.

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In the Chapter Six of [3] was developed another scheme of DC-to-DC converters classification that includes converters with isolation and explores the properties that allowed the generation of the new converter structures.

1.2.1.2 CONVERTER ANALYSIS WITH CONVERTER CELLS

The concept of converters cells is more versatile when it is used for the analysis of the converters that it generates. Each converter cell can be treated as a three-terminal device, deriving the average models for each converter cell and obviating the need to derive again these models for each of the converters of a particular family. The cell model can then be substituted point-by-point for the cell in any of the converters derived by the cell to give the converter model which can then be solved.

This approach to converter analysis is analogous to ordinary transistor circuit analysis. A converter cell and a transistor are both nonlinear three-terminal devices. Operation of these devices for small excursions about a DC operating point allows deriving small-signal models. Once these models have been derived, the nonlinear device (the converter cell or the transistor) may be replaced point by-point by its linearized model. This allows the use of ordinary linear circuit analysis techniques in order to analyze the circuit in which the nonlinear device (converter or a transistor circuit) was embedded.

1.2.2 THE INTERLEAVING AS A STRATEGY OF CONVERTER GENERATION

A different approximation to the generation of new converter structures that improves the characteristics of the resulting circuit have been studied in [9]. This approximation begins from both basic converter structures and control techniques already known, and continues by performing a new combination of all of them. The first step applied by this technique consists in a structural change through a parallel interconnection of a determined number of identical converter cells (N canonical cells). The second step consists in the application, to each canonical cell, of the strategically phase shifted control signals in one switching period. The name of this technique is interleaving. It was initially presented in [10] as a method of incrementing the switching frequency of all the converter without increasing the switching frequency of the N canonical cells that conform it, at the time that divides the input power between the N canonical cells. The resulting converter improves some of the characteristics of the basics structures that conforms it, especially when it works at high power.

Some of the advantages of the use of interleaving are the following:

- The ripple reduction in the output voltage and the input current due to the increment in the switching frequency. This increment also diminishes the electromagnetic interferences (EMI) associated, making easier the observance of the standards about line current harmonics and conducted EMI.
- The decrease of switching losses as a result of the use of switching frequencies in the optimal range.
- The decrease in the converter size because of the filters reduction.

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- The global decrease in the thermal dissipation due to the decrease of the losses.
- The converter fast dynamic response due to the smaller energy storage necessity.
- The improvement in the thermic management by the spreading of the hot spots.

1.2.2.1 COMPLEMENTARY INTERLEAVING

The technique of interleaving consists in the application of phase shifted control signals to each canonical cell in one switching period. If the phase shift of the signals is equal to the 50 % of the switching period, this is, the circuit switches are activated in a complementary way, the interleaving is called complementary. One of the characteristics of the 50 % phase shifted is that the circuit only works in configurations where the switches have different states and its analysis is easier.

In the Chapter Two of [9] the complementary interleaving is applied to the interconnection of two boost converters with output filter in continuous conduction mode. The name of the new structure is Interleaved Dual Boost "IDB" shown in Figure 1.8. The analysis of this converter not only confirms the reduction in the global variables ripple but also finds the extremely sensibility to the losses and the possibility of using the circuit as a doubler with a 50% duty cycle.

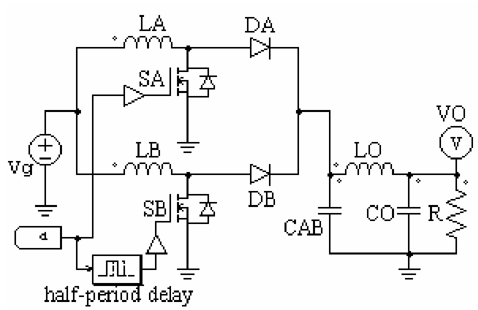

Figure 1.8: Interleaved Dual Boost (IDB) with Output Filter

Searching for alternatives to the IDB circuit, the Chapter Six of [9] began making modifications into the original structure using another technique: the design of classical multipliers. The addition to the unidirectional structure of the IDB of two diodes, keeping the two original capacitors of the canonical boost cells, generates a new boost converter structure. This interconnection between capacitors and diodes remembers the classical voltage multiplying nets constituted precisely by these two elements and can be interpreted as a net of switched capacitors, originating therefore the denomination chosen for the new converter circuit: Switched Capacitor Interleaved Dual Boost "SCIDB" depicted in Figure 1.9.

The open loop analysis of the SCIDB shows the decrease of the sensibility problems in comparison with the previous structure (IDB). Consequently, the converter can operate in a very extensive range of duty cycles. The structure also exhibits a symmetrical operation for a 50 % duty cycle and basic conversion rate of a quadruplier.

Following the methodology presented in this subsection, it has been generated the family of converters that will be explained in the Chapter Two of this thesis.

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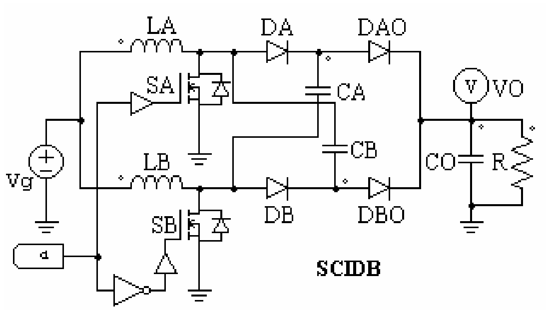

Figure 1.9: Switched Capacitor Interleaved Dual Boost (SCIDB)

1.3 SWITCHING CONVERTERS OPERATION MODES

Two main modes of switching converter operation may be distinguished: the continuous conduction mode CCM, where the inductor current or capacitor voltage never fails to zero, and the discontinuous conduction mode DCM, where the inductor current or capacitor voltage becomes zero for one interval of the switching period.

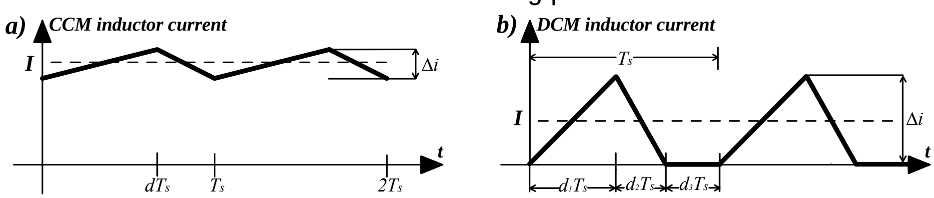

Figure 1.10: Inductor current waveform in a) CCM and b) DCM

1.3.1 CONTINUOUS CONDUCTION MODE CCM

The operation in CCM is guaranteed under the small-ripple assumption that all the AC ripples of steady-state inductor currents and capacitor voltages are relatively small comparing to their DC quantities [11]. As can be seen in the Figure 1.10a, in CCM the waveform has two intervals of operation, corresponding to the duty cycle: dT_s and the complementary $d'T_s$. Where $d'= (1-d)$.

1.3.2 DISCONTINUOUS CONDUCTION MODE DCM

The DCM occurs in converters containing current or voltage unidirectional switches, when the inductor current or capacitor voltage ripple is large enough to cause the switch current or voltage to reverse its polarity. A typical example can be a DC-to-DC converter operating at light load (small load current). Although sometimes, for low power applications, it is also quite common to operate the converter in DCM even at full load in order to avoid the

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reverse recovery problem of the diode [12]. In boost derived converters it can be found another use of this conduction mode with the aim to avoid the right half plane zero in the control-to-output transfer function [13].

The DCM has been classified in two modes. If only the small-ripple assumption in inductor currents is not satisfied, the converter will operate in discontinuous inductor current mode DICM, and if only the small-ripple assumption in capacitor voltages is not satisfied, the converter will operate in discontinuous capacitor voltage mode DCVM, reported for the first time in [4].

As it can be seen in Figure 1.10b, in DCM mode, the waveform has three intervals of operation. The energy stored in the inductor or capacitor during the first interval d_1T_s is completely released to the load during the second interval d_2T_s. Then, the inductor current or capacitor voltage becomes zero for the third interval d_3T_s.

Conditions for operation in the discontinuous conduction mode can be found by determining when the inductor current or capacitor voltage ripples and their DC components cause the switch on-state current or off-state voltage to reverse polarity. Some of these conditions are the increase of load R (therefore the averaged of DC current I or voltage V diminishes) or the decrease of the inductance L, capacitor C or switching frequency f_s. In any case, however, the operation in DCM mode results in an additional topology compared with the operation in CCM. Commonly the properties of converters change radically when DCM is entered: the conversion ratio M becomes load-dependent, output impedance is increased, dynamics are altered and control of output voltage may be lost when load is removed. Despite of these changes some circuits are purposely designed to operate in DCM over the entire line cycle in order to simplify the control [12].

1.3.3 Discontinuous quasi-resonant mode DQRM

A systematic study of possible operating modes of PWM converters realized in [14] revealed that, in addition to the three known modes CCM, DICM and DCVM, when the small-ripple assumption in both inductor currents and capacitor voltages are not satisfied, the converter will operate in another mode: the discontinuous quasi-resonant mode DQRM. The name of this mode is because the inductor and the capacitor form a resonant circuit in one of the operating states. DQRM can be considered as a combination of DICM and DCVM.

When a PWM converter operates in DQRM, the transistor turn-ON and the diode turn-OFF are at zero current, while the transistor turn-OFF and the diode turn-ON are at zero voltage, so that switching losses are reduced, as in various quasi-resonant converters. Unlike quasi-resonant converters, which require a variable frequency control, the PWM converter in DQRM can be controlled just as PWM converters in CCM: by varying the duty ratio of the active switch at constant switching frequency. In addition, the active switch does not need to be two-quadrant.

The operation in DCVM and DQRM is guaranteed under some specific conditions: the first is the order of the circuit topology that must be higher than two, and the second is that the transistor and diode must form a cut-set with a non-empty set of inductors for DICM operation or a loop with a set of capacitors (except output filter capacitor) and possibly voltage source for DCVM operation. Therefore, in a switching period there exists one time stage during which, both the transistor switch and the diode switch, can be in the same ON

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state for DCVM and DQRM operation, which means parallel or short connection of voltage source and/or capacitor for the basic two-order PWM switching converters, such as buck, boost, buck-boost circuits. So these basic converters can only operate in CCM and DICM [15].

1.3.4 OTHER DISCONTINUOUS MODES

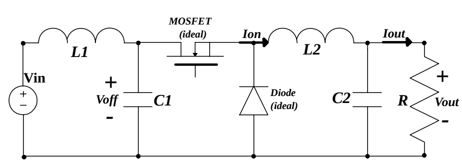
The existence of new discontinuous modes in PWM DC-to-DC converters has been pointed out in [13]. Such modes have been named Multi-Discontinuous Modes (MDMs) as they are characterized by the presence of multiple current and voltage discontinuities within the switching period. This means that the discontinuity of the state current meets the discontinuity of the state voltage within the same state of the switch, which is the main difference with the DQRM mode described previously.

Multi-Discontinuous Modes (MDMs) were detected in fourth order PWM DC-to-DC converters with light load conditions. The authors use a Cuk-PWM converter in order to exemplify and characterize this mode of conduction. The experimental measuring of the control-to-output frequency responses have shown an order reduction due to the discontinuous behaviour of the converter, this is, the frequency response looks like a first order circuit although it is of fourth order. Another important observation reported by the authors is that the resonant stage lies on the output side instead of the input side, as it usually happens in QR converters; consequently, large output inductor current ripple can be involved, so that the demand for low ESR output capacitors increases. The experimental tests have also shown that a high feedback gain can lead sometimes to (instant) chaos in presence of MDMs.

In Chapter Two it will be shown that in addition to these modes of conduction, when the interleaving technique is used for the generation of the circuit, another infrequent discontinuous mode could appear.

1.3.5 EXAMPLE

As an example, Figure 1.11a shows a buck converter with input filter and in Figure 1.11b the periodic sequence of states in all four possible modes of conduction can be observed. More exactly, the modes of conduction can be seen as follows. The loop of the CCM mode is described by the periodic sequence of states *(1, 0) -> (0, 1)*, because in this mode the diode switching is synchronous with the transistor switching -when the transistor is ON, the diode is OFF and vice versa-. The operating states are denoted according to the position of the transistor and the diode switch (ON=*1*, OFF=*0*). Thus, two linear, time-invariant networks (operating states) are repeatedly switched in CCM.



a) Buck converter with input filter.

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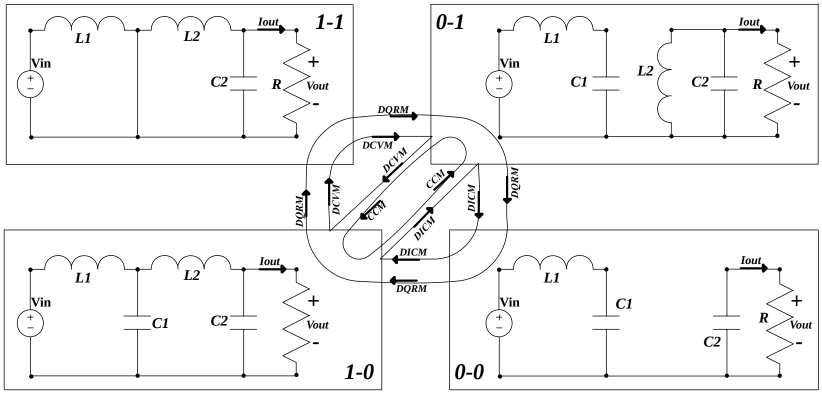

b) Loops in diagram of operating states represent possible operating modes

Figure 1.11: Periodic sequence of states in all the possible modes of conduction

As was previously seen, the discontinuous conduction mode takes place when low rippled assumption is removed, either in the inductor or in the capacitor. The loop of three states, *(1, 0) -> (0, 1) -> (0, 0)*, of the discontinuous inductor current mode DICM, occurs when the ac ripple of the output inductor current is sufficiently large, because the diode will cease to conduct before the end of the transistor OFF-time. If the small-ripple assumption is removed from the capacitor, the discontinuous capacitor voltage mode DCVM appears, this is, the ac ripple in the capacitor voltage can be sufficiently large so that the diode starts to conduct before the end of the transistor ON-time. Their corresponding states are *(1, 0) -> (1, 1) -> (0, 1)*. It was shown that DCVM and DICM are dual operating modes.

The remaining possibility is to remove the small-ripple assumption from both the inductor and the capacitor. This option, which naturally follows from the preceding discussion, yields a previously neglected operating mode of PWM converters. The mode will be called the discontinuous quasi-resonant mode DQRM because the inductor and the capacitor form a resonant circuit in one of the operating states. The sequence of operating states in DQRM are then *(1, 0) -> (1, 1) -> (0, 1) -> (0, 0)*, where it is apparent that DQRM can be considered as a combination of DICM and DCVM. The waveforms shown in Figure 1.12, corresponding to the circuit in Figure 1.11a, can be used as a reference for qualitative description of the operation in DQRM.

Assume that initially the converter is in the *(0-0)* state, then both the transistor and the diode are OFF. At the beginning of a switching cycle, the transistor is turned ON and the resonant *(1-0)* state is entered. Note that the transistor current is equal to zero before and immediately after the turn-ON transition or, saying this in another way, the transistor is turned ON at zero current. In the *(1-0)* state, the capacitor voltage and inductor current evolve in a quasi-sinusoidal manner until the capacitor voltage reaches zero and the diode starts to conduct at zero voltage. The converter remains in the *(1-1)* state until the transistor is turned OFF at zero voltage, and the *(0-1)* state is entered. In the *(0-1)* state, the diode current decays linearly, while the transistor voltage ramps up linearly. The remaining *(0-0)* state is entered when the diode current drops to zero. The converter stays in the *(0-0)* state until the transistor is turned-ON again and the switching cycle is completed.

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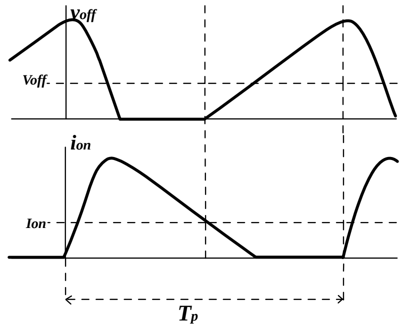

Figure 1.12: Waveforms of converter operating in DQRM mode

Then it can be concluded that when a PWM converter operates in DQRM, the transistor turn-ON and the diode turn-OFF are at zero current, while the transistor turn-OFF and the diode turn-ON are at zero voltage, so that switching losses are reduced, as in various quasi-resonant converters. Unlike quasi-resonant converters, which require a variable frequency control, the PWM converter in DQRM can be controlled just as PWM converters in CCM: by varying the duty ratio of the active switch at constant switching frequency.

1.4 AN OVERVIEW IN CONVERTERS MODELLING AND SIMULATION

Modelling and simulation are the essential ingredients of the analysis and design process in the power electronics area. They help a design engineer to gain an increased understanding of circuit operation. With this knowledge the designer can, for a given set of specifications, choose a structure, select appropriate circuit component types and values, estimate circuit performance, and complete the design by ensuring—using Monte Carlo simulation, worst case analysis, and other reliability and production yield analyses—that the circuit performance will meet specifications even with the anticipated variations in operating conditions and circuit component values. The combination of modelling, analysis, and simulation would provide better understanding of circuit operation and the basis for good design rather than working directly with a detailed schematic because simulation of a full production schematic still remains an elusive goal; some of its obstacles are for example the need for extensive model building, excessively long simulation times and the effects of layout, packaging, and parasitic losses. The combination of these insights with hardware prototyping and experiments constitutes a powerful and effective approach to design [2].

1.4.1 INITIAL ANALYSIS AND SIMULATION

The first step in the analysis of a converter circuit is to obtain the voltage and current waveforms that describe basic power-stage circuit operation. For this task it is necessary to

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eliminate some circuit elements that are secondary for the basic power processing function of the circuit, like the EMI filter, the bridge rectifier, the snubber net, etc.

Moreover, the switch must be replaced by a simple switch model which is controlled by a duty cycle pulse derived from a modulating signal. This signal is compared with the sawtooth waveform at the input of a comparator IC in order to establish the duty ratio of the converter. This is a simple implementation of the so-called PWM.

Therefore, the basic steady-state analysis and circuit waveforms can be obtained using the simplified circuit by simulations in a general circuit simulator or by computations using straightforward circuit analysis and computational tools [2].

1.4.2 MATHEMATICAL AND CIRCUIT MODELLING

In order to obtain the dynamic characteristics of the switching converter circuit in addition to the static ones, a modelling method is imperative. Its dynamic behaviour directly determines, or influences, four of the most important characteristics of a power converter: the stability of the feedback loop, the rejection of input voltage ripple and the closely-related transient response to input voltage perturbation, the output impedance and the closely-related transient response to load perturbation, and the compatibility with the input EMI filter [16].

It is important to note that each position of the switch results in one linear switched network. Consequently, for modelling purposes, the problem is well defined since it is completely described by the two (or more) linear networks. However, it is precisely this switching among several linear circuits that made the modelling problem nonlinear (piecewise linear) and difficult [1].

The complexity of modelling a switching converter circuit can also be observed when a small signal perturbation of a unique frequency is applying on a control signal because that signal generates an output which contains a multitude of frequencies: the fundamental signal and its harmonics. Even though the problem is not as severe as it looks because of the basic requirement of low output switching ripple compared with its DC value, this is the filter effect that highly accentuates the component of the output at the control fundamental frequency, and de-emphasizes its harmonics [1].

Due to the complexity characteristics of converter operation, the work of predicting its dynamic behaviour with the adequate precision is not easy but is very necessary. Because if one depends only on building the circuit and fixing it until the operation is satisfactory the engineering cost could escalate and it would be impossible to follow the chronograms. Therefore, the need of improving dynamic behaviour, that is no possible without an in-depth understanding of the operation of switching cells and easy-to-use and accurate models, explains the proliferation of papers related to switching cells analysis and modelling in the last years [16].

Since the objective is to solve for the transfer functions of a DC-to-DC converter, the requirement is for a small signal ac (dynamic) model linearized around a particular large-signal DC (steady-state) operating point, where the operating point is defined by certain values of steady state input voltage V_g and duty ratio D [1]. The small signal analysis can be used to predict accurately at all DC operating points: the stability margin of the converter

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against closed loop oscillation, and the frequency-domain and time-domain responses to perturbations in input voltage and/or output current [16].

Elementary circuit modelling of a power converter typically produces detailed continuous-time nonlinear time-varying models in state-space form. These models have rather low order, provided one makes approximations that are reasonable from the viewpoint of control-oriented modelling, like neglecting dynamics that occur at higher frequencies than the switching frequency (for instance, dynamics due to snubber elements, whose time scales are typically shorter than the switching period), and focusing instead on components that are essential to the power processing and control functions of the converter [2].

Such models capture essentially all the effects that are likely to be significant for analysis of the basic power conversion function, but they are generally still too detailed and awkward to work with. The first challenge, therefore, is to extract from the detailed model a simplified approximate model, preferably time-invariant, that is well matched to the particular analysis or control task for the converter being considered. There are systematic ways to obtain such simplifications, remarkably through averaging, which excludes the detailed switching intricacies, and sampled-data modelling, which suppresses the details internal to a switching cycle, focusing instead on cycle-to-cycle behaviour. Both methods can produce time-invariant but still nonlinear models. The following are the main methods to attain a mathematical or circuit model.

1.4.2.1 SWITCHED STATE-SPACE MODEL METHOD

The state space description is a canonical form of writing the differential equations that describe a system. For a linear network, the derivatives of the state variables are expressed as linear combinations of the system independent inputs and the state variables themselves. For a typical converter circuit, the physical state variables are the independent inductor currents and capacitor voltages because they are usually associated with the storage of energy.

The switched or instantaneous name is because to calculate the model, the switching function $q(t)$ is used (Figure 1.2). That function represents the position of the switch. When $q(t)=1$ the switch is closed and when $q(t)=0$ the switch is open. The switching function $q(t)$ may be thought of as (proportional to) the signal that has to be applied to the gate of the MOSFET in Figure 1.1 to turn it on and off as desired.

As an example, the calculation procedure will be applied to the boost converter of Figure 1.1. It begins by choosing the inductor current $i_L(t)$ and capacitor voltage $v_C(t)$ as the natural state variables and picking the resistor voltage $v(t)$ as the output, after this, it is necessary to apply the electrical laws and express the equations in function of the switched signal $q(t)$. The result is the following state-space model that describes the idealized converter.

$$\frac{di_L(t)}{dt} = \frac{1}{L}\left[\left(q(t)-1\right)v_C(t) + v_g(t)\right]$$

$$\frac{dv_C(t)}{dt} = \frac{1}{C}\left[\left(1-q(t)\right)i_L(t) - \frac{v_C(t)}{R}\right]$$

$$v(t) = v_C(t) \tag{5}$$

Denoting the state vector by

$$\mathbf{x}(t) = \begin{bmatrix} i_L(t) \\ v_C(t) \end{bmatrix} \tag{6}$$

And defining the following matrices

$$\mathbf{A_0} = \begin{bmatrix} 0 & -\frac{1}{L} \\ \frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \qquad \mathbf{A}_1 = \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{RC} \end{bmatrix} \qquad \mathbf{b} = \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} \tag{7}$$

The equation in (5) can be rewritten as

$$\frac{d\mathbf{x}(t)}{dt} = \left[(1 - q(t))\mathbf{A_0} + q(t)\mathbf{A_1} \right] \mathbf{x}(t) + \mathbf{b} v_g(t) \tag{8}$$

This model is named switched or instantaneous model to distinguish it from the averaged and sampled-data models. It is of interest for nonlinear control approximations.

Switched model in control

An example of the use of this model in control design can be seen in [17], where the authors used the previously explained procedure in order to get the equations of a CUK converter. They calculated a control law based in the sliding-mode control methodology. This control scheme extends the properties of hysteresis control to multi-variable environments and is able to constrain the system status to follow trajectories which lie on a suitable surface in the state space (sliding surface). For this purpose, each of the two state-space regions, separated by the sliding surface, are associated to one switch status. The corresponding system trajectories result from the switched state space model of the converter.

Exact calculation of RMS values in the switched model

In [18] another analytical method, whose starting point are the state space equations of the two-switched models, is presented. That method allows the exact calculation of the DC and RMS values of the state space variables in a switching converter, and bridges the existing gap between the state-space technique and the small signal approximation that considers negligible the steady state ripple values. The proposed method departs from the fact that the switching power converters are inherently nonlinear. Consequently, it is very difficult to calculate the RMS values of the state variable ripple using exact methods since the resulting differential equations cannot generally be solved. The small signal approximation that linearizes the state space equations around a quiescent operating point, could provide a sense of absence of the RMS values of the switching converter variables. As an example, the RMS value of a capacitor current is considered to be zero due to the fact that the DC ripple of the capacitor voltage is zero. So, despite the fact that there is zero ripple voltage across the capacitor, there is RMS current that flows through the capacitor.

Therefore, according to the procedure followed by the authors, the DC and RMS values of the state variables of a switching structure can be calculated by the replacement of the conventional state-space equations by a new set of equations. In order to obtain these

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equations a new extended state vector and an output vector were introduced. For a given frequency, they find two operating points and the time dependence of the newly created variables during a period can be plotted in order to obtain the steady state switching ripple using the new set of extended equations. Finally, using this method with the specifications and the components values of the power converter, a design engineer can calculate exactly their RMS values. These RMS values are important in order to calculate the current stresses of the different power converter devices as well as to design the filter in order to achieve the given specifications. Also they can be used in the optimization of the power converter components.

1.4.2.2 STATE SPACE AVERAGED MODELLING METHOD

Recalling the history of power electronics, it was easily found that averaging has been a dominant technique for analysis and control of switching power converters. The most important one is the state space averaging method proposed by Middlebrook and CUK in [19]. This was the first approach to result in a complete linear model of a switching cell and the major contribution to the dynamic analysis of switching structures. For this reason, it has been adopted by a lot of investigators nowadays, and can be said that is one of the most used standard techniques for the analysis and control of switching power converters. As it will be shown, the main advantages of this method are the establishment of a complete cell model (including both DC and AC quantities), and the mathematical rigor with which it can be carried out [16].

This method obtains a model that relates the modulating signal $v_c(t)$ or the duty ratio $d(t)$ to the output voltage characteristic $v(t)$, which is very useful in the design of analog feedback control schemes. Precisely, since the ripple in the instantaneous output voltage is made small by design, and the details of this small output ripple are not of interest in designing the feedback compensation, the continuous-time dynamic model obtained by this method has to relate specifically the modulating signal $v_c(t)$ or the duty ratio $d(t)$ to the local average of the output voltage $v(t)$ (where this average is computed over the switching period). A natural approach to obtain this model is to take the local average of the state-space model.

As it was explained in section 1.3.1, a typical switching converter circuit in CCM has two intervals of operation corresponding with the duty cycle dT_s and the complementary $d'T_s$. The topologies of the boost converter in CCM operation can be observed in Figure 1.3, in general, the corresponding set of state space equations to each topology can be written as:

Interval dT_s Interval $d'T_s$

$$\frac{d\mathbf{x}(t)}{dt} = \mathbf{A_1}\mathbf{x}(t) + \mathbf{b_1}v_g(t) \qquad \frac{d\mathbf{x}(t)}{dt} = \mathbf{A}_2\mathbf{x}(t) + \mathbf{b}_2v_g(t)$$

$$y_1(t) = \mathbf{c}_1\mathbf{x}(t) \qquad y_2(t) = \mathbf{c}_2\mathbf{x}(t) \tag{9}$$

Where $\mathbf{x}(t)$ is the vector of the state variables, that was defined in (6) for the boost of Figure 1.1, $y(t)$ represents the circuit output, and the matrices for the same example are:

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$$\mathbf{A}_1=\begin{bmatrix}0 & 0\\ 0 & -\dfrac{1}{RC}\end{bmatrix}\qquad \mathbf{b}_1=\begin{bmatrix}\dfrac{1}{L}\\ 0\end{bmatrix}\qquad \mathbf{c}_1=\begin{bmatrix}0 & 1\end{bmatrix}$$

$$\mathbf{A}_2=\begin{bmatrix}0 & -\dfrac{1}{L}\\ \dfrac{1}{C} & -\dfrac{1}{RC}\end{bmatrix}\qquad \mathbf{b}_2=\begin{bmatrix}\dfrac{1}{L}\\ 0\end{bmatrix}\qquad \mathbf{c}_2=\begin{bmatrix}0 & 1\end{bmatrix}\qquad (10)$$

Now, the objective is to replace the state space description of the two linear circuits emanating from the two successive phases of the switching cycle d by a single state space description which represents approximately the behaviour of the circuit across the whole period T_s. Then the next step is to take the average for both equations of (10) by summing up the equations for the interval dT_s multiplied by d and the equations for the interval $d'T_s$ multiplied by d'. The following linear continuous system results:

$$\frac{d\mathbf{x}(t)}{dt}=d\left(\mathbf{A}_1\mathbf{x}(t)+\mathbf{b}_1 v_g(t)\right)+d'\left(\mathbf{A}_2\mathbf{x}(t)+\mathbf{b}_2 v_g(t)\right)$$

$$y(t)=d\mathbf{c}_1^T\mathbf{x}(t)+d'\mathbf{c}_2^T\mathbf{x}(t)\qquad (11)$$

After rearranging (11) into the standard linear continuous system state space description:

$$\frac{d\mathbf{x}(t)}{dt}=\left(d\mathbf{A}_1+d'\mathbf{A}_2\right)\mathbf{x}(t)+\left(d\mathbf{b}_1+d'\mathbf{b}_2\right)v_g(t)$$

$$y(t)=d\mathbf{c}_1^T\mathbf{x}(t)+d'\mathbf{c}_2^T\mathbf{x}(t)\qquad (12)$$

This model is the basic averaged state-space description over a single period T, which is the starting model for all other derivations, both state space and circuit oriented.

The justification and the nature of the approximation made in the substitution of the two switched models of (9) by the averaged model of (12) is indicated in the appendixes of [19]. The basic approximation also coincides with the requirement for low output voltage ripple:

$$\frac{f_c}{f_s}<<1\qquad (13)$$

That is, the effective filter corner frequency (formed by the L's and C's) has to be much lower than the switching frequency.

If the duty ratio is constant from cycle to cycle, $d=D$ (steady state DC duty ratio). Then the model in (12) is a linear system that holds superposition and can be perturbed by introduction of line voltage variations, causing a corresponding perturbation in the state and the output vector. This can be expressed as the DC value (V_g, X, Y) in addition to the superimposed AC perturbation to the variable as follows:

$$v_g(t)=V_g+\hat{v}_g\qquad x(t)=X+\hat{x}\qquad y(t)=Y+\hat{y}\qquad (14)$$

Including these perturbations in (12):

$$\frac{d\hat{\mathbf{x}}(t)}{dt} = \mathbf{A}(X+\hat{x}) + \mathbf{b}(V_g + \hat{v}_g)$$

$$Y + \hat{y} = \mathbf{c}^T (X+\hat{x}) \tag{15}$$

where:

$$\mathbf{A} = D\mathbf{A_1} + D'\mathbf{A}_2 \qquad \mathbf{b} = D\mathbf{b_1} + D'\mathbf{b}_2 \qquad \mathbf{c}^T = D\mathbf{c}_1^T + D'\mathbf{c}_2^T \tag{16}$$

This model can be separated in the steady-state (DC) part and the dynamic (AC) part. Then the steady-state (DC) model:

$$0 = \mathbf{A}X + \mathbf{b}V_g$$

$$Y = \mathbf{c}^T X \qquad Y = -\mathbf{c}^T \mathbf{A}^{-1}\mathbf{b}V_g \tag{17}$$

And the dynamic (AC) model:

$$\frac{d\hat{\mathbf{x}}(t)}{dt} = \mathbf{A}\hat{x} + \mathbf{b}\hat{v}_g$$

$$\hat{y} = \mathbf{c}^T \hat{x} \tag{18}$$

It is interesting to note that in (17) the steady state (DC) vector X will only depend on the DC duty ratio D and resistances in the original model, but not on the storage element values (L's and C's). This is in complete agreement with the first-order approximation of the exact DC conditions shown in appendixes of [19].

From the dynamic (AC) model, the line voltage to state-vector transfer functions in the Laplace domain can be easily derived as:

$$\frac{\hat{\mathbf{x}}(s)}{\hat{v}_g} = (s\mathbf{I} - \mathbf{A})^{-1}\mathbf{b} \qquad \frac{\hat{y}(s)}{\hat{v}_g} = \mathbf{c}^{\mathbf{T}}(s\mathbf{I} - \mathbf{A})^{-1}\mathbf{b} \tag{19}$$

Hence at this point, both steady-state (DC) and line transfer functions are available. The inclusion of the duty ratio modulation effect into the basic averaged model (12) will be done by the appending of AC variations in the form of perturbations. The corresponding perturbation definitions of (14) are complemented by the following definition that represents the duty ratio changes from cycle to cycle:

$$d(t) = D + \hat{d} \tag{20}$$

Then the basic model (12) becomes in the equations (21) and (22). As it can be seen, this description is nonlinear owing to the presence of the product of the two time dependent quantities $\hat{x}$ and $\hat{d}$.

$$\frac{d\mathbf{x}(t)}{dt} = \underbrace{\mathbf{A}X + \mathbf{b}V_g}_{\text{DC term}} + \underbrace{\mathbf{A}\hat{x} + \mathbf{b}\hat{v}_g}_{\text{line variation}} + \underbrace{[(\mathbf{A_1} - \mathbf{A}_2)X + (\mathbf{b_1} - \mathbf{b}_2)V_g]\hat{d}}_{\text{Duty ratio variation}} + \underbrace{[(\mathbf{A_1} - \mathbf{A}_2)\hat{x} + (\mathbf{b_1} - \mathbf{b}_2)\hat{v}_g]\hat{d}}_{\text{nonlinear second order term}} \tag{21}$$

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$$Y+\hat{y}=\underbrace{\mathbf{c}^{T}X}_{\text{DC term}}+\underbrace{\mathbf{c}^{\mathbf{T}}\hat{x}}_{\text{AC term}}+\underbrace{\left(\mathbf{c}_1^{T}-\mathbf{c}_{\mathbf{2}}^{\mathbf{T}}\right)X\hat{d}}_{\text{AC term}}+\underbrace{\left(\mathbf{c}_1^{T}-\mathbf{c}_{\mathbf{2}}^{\mathbf{T}}\right)\hat{x}\hat{d}}_{\text{nonlinear term}} \tag{22}$$

Therefore, it becomes necessary to apply a linearization step to the model, so the next step is the small signal approximation, which considers that AC variations values (perturbations) are negligible compared to the steady state values:

$$\frac{\hat{v}_g}{V_g}<<1 \qquad \frac{\hat{x}}{X}<<1 \qquad \frac{\hat{d}}{D}<<1 \tag{23}$$

Applying (23) into (21) and (22) the nonlinear second order terms can be neglected. The result is a linear system that includes the duty ratio modulation. After rearranging AC and DC terms the final state space averaged model is:

Steady state (DC) model:

$$X=\mathbf{A}^{-1}\mathbf{b}V_g$$

$$Y=\mathbf{c}^{T}X \qquad Y=-\mathbf{c}^{T}\mathbf{A}^{-\mathbf{1}}\mathbf{b}V_g \tag{24}$$

Dynamic (AC small signal) model:

$$\frac{d\hat{\mathbf{x}}(t)}{dt}=\mathbf{A}\hat{x}+\mathbf{b}\hat{v}_g+\left[(\mathbf{A}_{\mathbf{1}}-\mathbf{A}_2)X+(\mathbf{b}_{\mathbf{1}}-\mathbf{b}_2)V_g\right]\hat{d}$$

$$\hat{y}=\mathbf{c}^{\mathbf{T}}\hat{x}+\left(\mathbf{c}_1^{T}-\mathbf{c}_2^{\mathbf{T}}\right)X\hat{d} \tag{25}$$

Equations (24) and (25) represent the small-signal low frequency model of any two-state switching DC-to-DC converter working in the continuous conduction mode.

It is important to note that by neglecting the nonlinear terms, the source of harmonics is removed. This small signal approximation is possible due to the fact that output ripple in the instantaneous variables are made small by design.

The use and interpretation of this model should be restricted to frequencies below half the switching frequency; converter dynamics up to around one-tenth the switching frequency are generally well captured by the averaged model. [19]

Some drawbacks of the SSA approach commented by [16] are the following. First, it does not result in a general linear model of a switching cell that could be independent of the cell configuration, operating mode, and controlled quantity. Second, it requires extensions and modifications if the controlled quantity is other than the duty ratio.

From the beginnings of the development of this modelling method, a lot of authors have used it, through the analysis of its disadvantages, as a starting point of new methodologies. This new ideas and contributions will be presented immediately afterwards.

Switching frequency dependent averaged models

Two approximation problems of the conventional state space averaged model have been reported in [20]. The first one is the steady-state DC offset error of the output voltage exhibited in transient responses for low switching frequencies, and the second one are the

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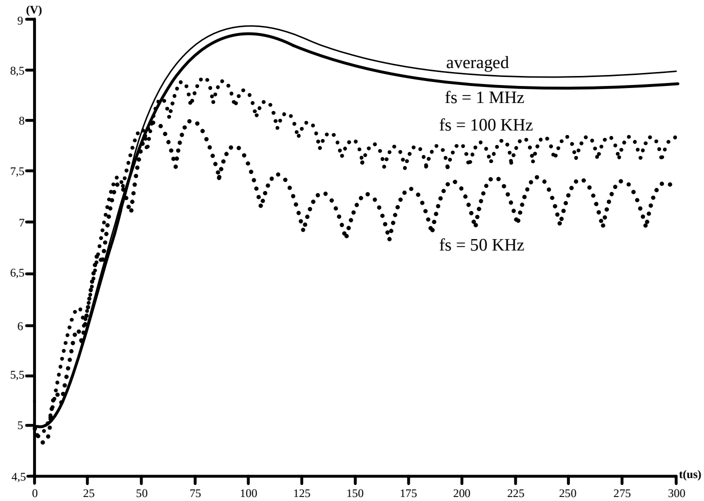
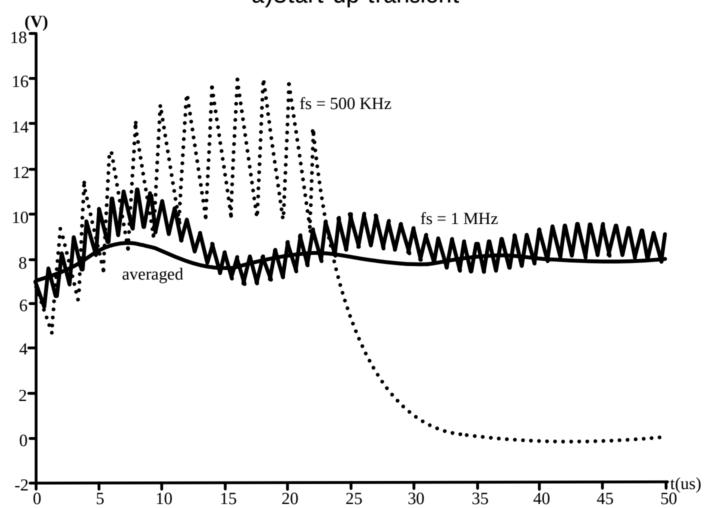
discrepancies of the results for the closed loop stability. The simulation results of the PWM controlled boost converter can be seen in Figure 1.13.



a)Start-up transient



b)Transient

Figure 1.13: Output voltage simulated for averaged and switching models

As it can be seen in Figure 1.13a the approximation improves as the switching frequency increases. Conversely, at slower switching frequencies, the averaged model fails to accurately capture the average value in steady-state. This is a practical concern in applications where semiconductor device capabilities constrain the controller to operate at slower switching frequencies. The DC offset discrepancy has been previously reported for open-loop converters [21]. This affects the linearization. However, it can often be compensated by including an integrator in the control loop for the variable of interest.

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Figure 1.13b shows that the closed-loop system is stable for frequencies greater than f_s=500 kHz, and unstable for lower frequencies. As expected the averaging approximation improves as switching frequency increases. On the contrary, the conventional averaged model [19], which is independent of switching frequency, predicts that the closed-loop system is stable. An explanation for this result is that the SSA model [19] is based on the assumption that the switching frequency is “fast enough.” While it is not known precisely how fast is “fast enough,” designers typically take a rule-of-thumb linearized loop-gain crossover frequency on the order of 1/4-1/10 of the switching frequency. The practical concern here is that the conventional averaged model gives no insight or guidance as to “how fast” the switching frequency needs to be in order to obtain an acceptable closed-loop performance. As a result, transient performance is sacrificed and the designers avoid slow switching frequencies in order to have confidence in the averaged model.

In order to correct the problems that have been reported, the authors in [20] derive a modified averaging technique for PWM DC-to-DC converters using formal mathematical methods with the employ of periodic ripple functions introducing a correction in the approximation. The new averaged model is switching frequency dependent. Although, it is important to remark that the model derived is valid only when the switching period is sufficiently small as in all general averaged models.

The classical averaging approach of Krylov, Bogoliubov and Mitropolsky - KBM

Power electronics is not the unique field where averaging methods have been applied. In fact, even 200 years ago, in Gauss’ time, averaging techniques had already found their applications in celestial mechanics. Therefore theoretic foundations for the averaging have already been studied by many authors, specifically the classical approach of Bogoliubov and Mitropolsky was used in some papers like [22, 23] where the authors work with the rigorous averaging theory as a way of answering some fundamental questions that still remain due to the heuristic nature of the state-space averaging modelling method.

A generalization of averaging known as the KBM (Krylov-Bogoliubov-Miltropolsky) method, which considers a change of variables, was the algorithm applied for the authors of [22] in order to clarify the relationships between the original circuit and the large-signal averaged models, and provide higher order approximations for ripple estimation.

The averaging theory can be applied to time-varying equations which admit the introduction of a small parameter ε. A helpful perspective to understand the role of ε is to consider the analogy between averaging and linearization. In the broader context, averaging and linearization can both be classified as perturbation methods which yield simpler approximate models. Linearization provides a linear approximation to a nonlinear system, while averaging provides a time invariant approximation to a time varying system. In both cases, the simpler approximate model is exact at some nominal point. For linearization, that point is in the state space, $x=x_n$. For averaging, the point is in the parameter space, $\varepsilon=0$ (i.e., infinite switching frequency, zero ripple solutions). In addition, the simpler model is a good approximation in some neighborhood of the nominal point. Linearization considers a neighborhood in the state space, and averaging considers a neighborhood in the parameter space.

Some interesting conclusions of the rigorous averaging theory application in [22] are the following. First, it is important to note that the models of power electronic converters based on averaging theory are, in general, the same as those obtained by heuristic state-space

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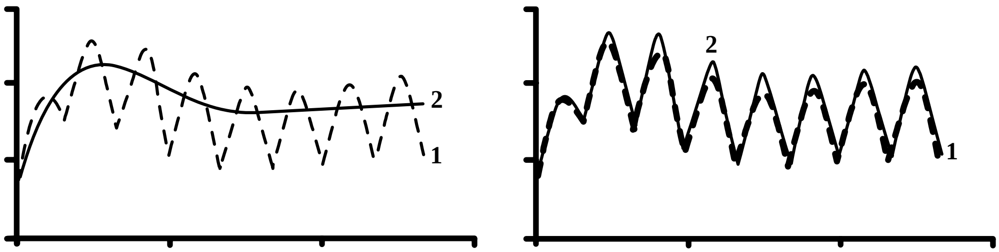
averaging, but the theory allows some key inferences. Second, the averaged model does not need to be restricted to small signals or linear approximations because the large signal nonlinear averaged model retains important properties of the original system under certain conditions. Third, some ripple correction functions can be found so that the behaviour of a given converter can be estimated to any desired degree of accuracy from the behaviour of the averaged model. Finally, a correction can be made to the initial condition to improve tracking of the system behaviour by mean of the averaged system when large transients appear.



a) 1. Exact, 2. Averaged b) 1. Exact, 2. Averaged with first order correction

Figure 1.14: Boost converter: ripple and initial condition correction

Figure 1.14 illustrates a first-order correction for ripple and initial condition for the start-up of a slow switching boost converter. Making a comparison, the state trajectories of the original system are labelled as curve 1 in each graph. Curve 2 in Figure 1.14a corresponds to the state trajectories of the averaged system with first-order initial condition correction, curve 2 can be seen to closely approximate moving averages along the original system trajectories (curve 1) beginning at $t=0$. Curve 2 in Figure 1.14b reflects the first-order ripple correction that closely tracks the original system trajectories (curve 1) and provide a first-order estimate for peak-to-peak ripple.

Averaging based on the slow and fast variables classification

Another approximation to the rigorous averaging methods can be found in [23]. The aim of that paper is to establish uniform averaged modelling methods for switching power converters using averaging methods for differential equation systems with discontinuous right-hand sides or discontinuous systems that are the class of equations found in the state space models of any types of switching power converters. The averaging methods are the means of transforming the discontinuous system models into continuous ones, so that control methods for continuous systems become applicable. This is because the discontinuities of the original discontinuous models are smoothed and in many cases the averaged models will be continuous.

The uniform averaging procedures proposed in [23] respond to the classification of the ordinary differential equations from the viewpoint of applying averaging methods into two groups: one-time scale (OTS) systems where all state variables evolve at the same order of rate with respect to time, and two-time scales (TTS) systems where some state variables are usually called slow variables because they evolve slowly respect to time, while another state variables evolve faster and are usually called fast variables. The names of the methods used with each class of systems are: averaging method for one-time scale discontinuous system (AM-OTS-DS), and averaging method for two-time scale discontinuous system (AM-TTS-DS).

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From the classification made, it is known that AM-OTS-DS can be applied to averaged modelling of open-loop or duty-rate controlled PWM converters, while AM-TTS-DS can be applied to PWM converters employing current programmed control and PWM converters under DCM where the inductor currents are fast variables while capacitor voltages are slow variables. Also it can be applied to resonant and quasi-resonant converters where the state variables of the resonant sections are fast variables while state variables of filter sections are slow variables. The detail description of these methods is out of the scope of this state-of-the-art but it is important to highlight one final conclusion: the currently used state space averaging modelling method and its several extensions can be derived from the AM-OTS-DS and AM-TTS-DS methods. Therefore these methods are a generalization of averaging modelling.

A symbolic analysis package to apply these methods, based on partitioning the converter circuit into a slow and fast subsystem, was developed in [24]. The slow subsystem contains the main energy-storage elements of the converter as well as its input and output sections. The fast subsystem is composed by the switching devices, the associated resonant tank and the snubber circuit. With the converter circuit partitioned in that way, an averaged model can be derived following three steps: relaxation where the fast subsystem is analyzed by assuming constant input from the slow subsystem, decoupling by replacing the fast subsystem with a static network, and averaging that expands the time-varying input to the slow subsystem using Fourier series. Since the switching frequency is usually very high and the slow subsystem is insensitive to fast-varying inputs, the time-varying terms can be neglected such that only the DC component remains. Finally, a nonlinear time-invariant-averaged model approximately describing the slow dynamics of the converter is obtained. The method may also be termed state-space averaging, as the averaging can be carried out in state space. The authors explained that the classical state-space averaging is, in fact, a special case of the more general method discussed in this paper.

However, the proposed averaging method of [24] is not applicable to all converters. Two basic limitations of the method are the need for analytical solution of the relaxed fast subsystem and the assumption that this solution is periodic, with a period equal to one switching cycle. To obtain an analytical solution, the fast subsystem may not include any nonlinear element except ideal switches and diodes. The fast subsystem should also be kept as simple as possible to facilitate computer analysis, which implies that most parasitic effects have to be neglected. On the other hand, the relaxed solution will be periodic only when the fast subsystem does not contain continuous energy-storage elements. Otherwise, the fast subsystem exhibits nontrivial low-frequency dynamics and needs to be replaced by a dynamic network rather than a resistive one. The necessity to assume a periodic solution of the relaxed fast subsystem can also be understood in the frequency domain. A non-periodic solution will have components at frequencies lower than the switching frequency, whose effects on the slow subsystem cannot be neglected.

Finally, it can be said that the popularity of the State Space Averaged model method is due largely to its clear justification, simple methodology, and demonstrated practical utility. The averaged model can be used to solve the steady-state or operating point relations and make more efficient simulations of converter dynamic behaviour than the simulations that can be obtained using the switched model; also, it forms a convenient starting point for

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various linear and nonlinear control design approaches. More traditionally, the small-signal control design to regulate operation in the neighborhood of a fixed operating point can be based on the corresponding Linear-Time-Invariant linearization of this averaged model. Moreover, it can be easily modified to approximately represent the dynamics of a high-frequency PWM converter operated under so-called current-mode control. Therefore this model is an essential design tool because it provides physical insight and leads to analytical results that can be used in the design process to select component and controller parameters values for a given set of specifications.

1.4.2.3 INJECTED-ABSORBED CURRENT METHOD

The essence of the injected-absorbed current analysis method is the establishment of a set of six characteristic coefficients of the converter circuit, so that its averaged currents - absorbed (input) and injected (output)- are expressed as linear functions of the input and output voltages and the controlled quantity. Applying partial derivatives to those functions, a simple proportional relation among the small increments of the involved quantities is obtained. These increments are considered to be equal to the ac components to which the Laplace transformation is applied. The results are the equations with the six characteristic coefficients. They are functions of the steady state input and output voltages, the load current, the circuit topology, the components values, the operation mode and the complex frequency s. The characteristic coefficients can be established with the desired accuracy e.g. with or without second-order parasitic elements, and taking into account or neglecting the voltage drops across the conducting switches and diodes.

These functions are then used as a starting point for the synthesis of the general, low frequency, small signal model. They can be linearized if and only if all six characteristic coefficients exist. For example, since the coefficients are partial derivatives they do not exist if the converter is exactly at the border of CCM and DCM operation mode.

After the linearization, the equations can be transformed into a form that permits the synthesis of an equivalent circuit model of the converter that comprises two dependent generators and two impedances, defined as simple functions of the characteristic coefficients. This equivalent circuit model possesses all essential small signal properties of the switching converter, including its output and input impedance, as well as the input to output voltage and the controlled quantity to output transfer functions. The obtained cell is valid for all switching power converters described by the characteristic coefficients. It can have constant frequency or free running configuration and its controlled quantity can be the duty ratio, the maximum inductor current, or the switching frequency. The structure of the synthesized equivalent circuit model is invariable. That reduces the difficulties of linearizing a switching power converter to the precisely defined procedure of deriving its characteristic coefficients. It is important to remark that the equivalent circuit can be embedded in any linear electronic structure to which the whole arsenal of linear analysis methods can be applied.

In summary, using this method, the transfer functions and the equivalent circuit of a switching power converter can be obtained. According to those results, it can be said that this method is more focused to control, because departing from them, the application of the control theory methods is direct. This method is a linear method whose validity is limited to

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low frequency, small signal phenomena, accurate at frequencies up to 1/20 to 1/3 of the switching frequency. It provides insight into the physical operation of the converter and the results lead to a compact and general circuit model that can be used in order to derive all essential dynamic parameters of the converter in closed form expressions [16]. Another technical advantage of this method is the possibility of representing the small-signal model either by an electrical equivalent circuit or by a functional block diagram that is more suitable than the equivalent circuit for computer simulation (for example, with MATLAB or SIMULINK), while designing the control circuit.

Generalization of the injected-absorbed current method

Until this point this method has been applied only to converters with a single state variable (not counting the output voltage). But in [25] it has been shown how the injected-absorbed-current dynamic analysis approach can be used with structures with any number of state variables. This paper generalizes the method for an arbitrary number of state variables obtaining general expressions for all six characteristic coefficients, and applies the proposed method to a series resonant converter operating above resonance and compared to the previously reported measurements.

Current injected equivalent circuit approach - CIECA

In [26] another modelling method, that starts with the current injected approach and results in either a set of equations which describe input and output properties or an equivalent linear circuit model valid at small signal and low frequency levels, is developed. Its name is current injected equivalent circuit approach –CIECA-.

The first step of this method is to identify the nonlinear part of the converter circuit, and linearize only that part of the converter as the remaining part is inherently linear. Hence this approach becomes simple as the linearization is achieved by averaging the current through the nonlinear part that is injected into the linear part of the converter.

After that, it can be obtained a set of equations based on the relationships between the current and voltage waveforms that can be deduced from the converter diagram. Those relationships are the average current of the nonlinear part, that is injected into the linear part in a switching period, the voltage across the inductor in each subinterval in a switching period, and the relationship between average injected current and output voltage in which appears the impedance of the linear part of the converter.

In the second step a steady-state solution is achieved by setting derivatives and perturbations to zero. Since the set of converter equations is linear, superposition holds and it can be perturbed by the introduction of a small AC variation over the steady-state operating point.

The nonlinear second order terms are neglected in order to obtain once again a linear set of equations. Next, only the AC part is retained, which describes the small signal, low frequency behaviour of the converter, and the input-to-output and control-to-output transfer functions are obtained by taking its Laplace transform.

Using the same set of equations calculated in step one, an equivalent circuit can be drawn which represents the input and output small signal, low frequency properties of the nonlinear converter.

The circuit model gives more physical insight into the qualitative nature of the results, especially the right half-plane zeros in boost and buck-boost converters.

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In summary, the application of the CIECA modelling method permits to describe, for nonlinear power converters, the input and output small signal low frequency properties and the transfer properties.

In [27] the application of the CIECA method is carried out in a CUK converter in order to demonstrate its possibilities of modelling. The unique difference with the application of the method to the basic converters is that, in this case, the converter is divided on two parts for making easier the analysis.

1.4.2.4 CIRCUIT AVERAGING AND THE AVERAGED SWITCH METHODS

Instead of averaging the converter state equations, this sort of methods averages directly the characteristics or waveforms associated with each of the components in the converter. Therefore, this technique gives a physical interpretation to the model because manipulations are performed on the circuit diagram instead of on its equations. It can be also applied directly to a number of different types of converters and switch elements because of its generality and the ease with which the resulting models are simulated in standard circuit simulators. It should be noted that the definition of the switch network and its dependent variables is not unique. Different definitions, depending of the approximation used to obtain them, lead to equivalent but not identical averaged circuit models; some choices may be better suited than others to any particular analysis task.

The minimum separable switching configuration - MISSCO

The first approximation to this method appeared in [28]. This paper describes an approach to model the low-frequency behaviour of the power switches in a DC-to-DC switching converter. This approach starts with a simplification of the converter circuit to a Minimum Separable Switching Configuration (MISSCO) containing all power switches but a minimum number of other components. Then by making use of an impulse-response method and averaging technique, a set of equations describing the low-frequency behaviour of the MISSCO are derived. The resultant equations can be used to generate a low-frequency equivalent circuit of the MISSCO, which can then be combined with the rest of the switching converter circuit to form a complete low frequency equivalent circuit of the converter that can be used for the determination of the transfer functions.

The PWM switch model

In [29] another circuit-oriented method of analysis of PWM converters is presented. That method develops and uses the model named PWM switch that is a three-terminal nonlinear device which represents the total nonlinearity in a PWM converter just as the transistor represents the total nonlinearity in an electronic amplifier. It is used in the same way as the model of the transistor is used in the analysis of electronic amplifier circuits. Hence, it is not necessary to linearize the entire equations of a PWM converter as well as it is not necessary to linearize the entire equations of an amplifier along with the Ebers-Moll equations of the transistor to determine its DC and small-signal characteristics, this is the characteristic that makes the difference with the state-space averaging modelling method.

In order to obtain the PWM switch model, the active and passive switches of the four familiar converters (buck, boost, buck-boost and CUK) are lumped together in a single functional block called the PWM switch. This functional block represents the total nonlinearity in these converters and is shown as a three-terminal nonlinear device in Figure 1.15a. The terminal designations -a, p, c- refer to active, passive, and common, respectively. The voltage and current port designations of this device are connected to the external circuit elements of every converter as to provide the proper port conditions. Hence, the four basic converters are obtained by a simple permutation of the PWM switch.

After the definition of this functional block, and following some simple calculations, it is possible to obtain a DC model of the PWM switch that can be seen in Figure 1.15b. Therefore, it can be used in order to analyze the DC characteristics of any converter. In Figure 1.15c it has been applied for the analysis of the boost converter. In the paper, it has been obtained other models of PWM Switch for small signal analysis, calculation of control-to-output transfer functions, and analysis including effects of storage-time modulation. The resulting circuits can be easily analyzed on standard electronic circuit analysis programs even in closed-loop operation without the need for special-purpose programs. Even though this method is useful like a tool of modelling, calculation, and simulation, its primary purpose is educational. This is, students at this level are familiar with the procedure of replacing the nonlinear part of a circuit by an equivalent circuit model, and therefore the PWM switch Equivalent Averaged Model can make easier for them to learn all about the DC and small-signal properties of PWM converters. [29, 30]

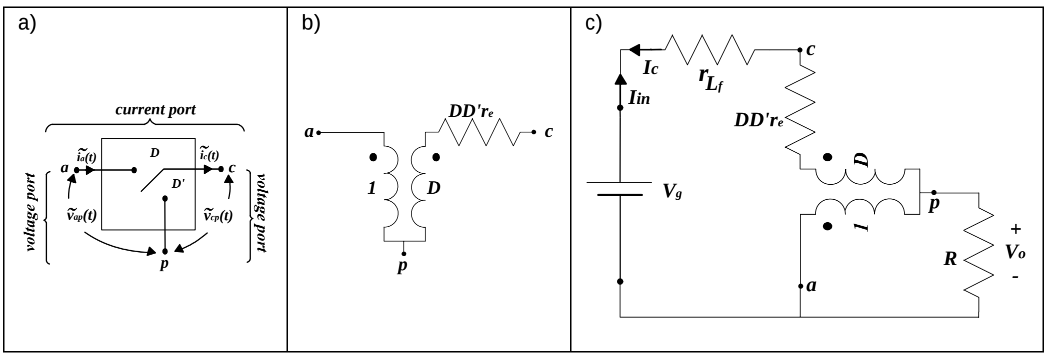

Figure 1.15: a) PWM Switch, b) PWM Switch Equivalent Average Model for fixed D
c) Schematic of a Boost converter for DC analysis.

The switched inductor model - SIM

A structure-independent model method, that was conceived in order to be used with general purpose simulators as SPICE, is presented in [31]. The SIM -Switched Inductor Model- Method is based in a close examination of the basic PWM converters that reveals some similarities in their structures: a switched inductor, which serves as a temporary energy storage element between the input and output terminals. Then this method consists in replacing that part by an equivalent circuit compatible with simulators such as SPICE. The basic switched inductor assembly (Figure 1.16a) consists of an inductor that is switched at one end between two terminals b and c at a frequency f, and a duty ratio D_{ON}, for port b, and D_{OFF} for port c.

The equivalent circuit of the switched inductor (Figure 1.16b) is easily developed by considering the average signals of the ports a, b, and c under the assumption that the switching period is much smaller than the basic time constants of the converter system.

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Eliana Isabel Arango Zuluaga
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Under these assumptions, the terminal voltage of ports b and c do not change markedly over a switching period. The current and voltage sources of the equivalent circuit are, for the general case, nonlinear dependent sources, i.e. their magnitude is a product of two parameters, both of which could be variables of the system. The behavioural description of these dependent current sources, i.e. their magnitude as a function of other parameters of the converter, will be a function of the operational mode of the converter [32]. The resulting equivalent circuit can then be used to run both time and frequency domain simulation using a general purpose circuit simulator such as SPICE, and get the responses for steady-state, transient and small signal analysis [33].

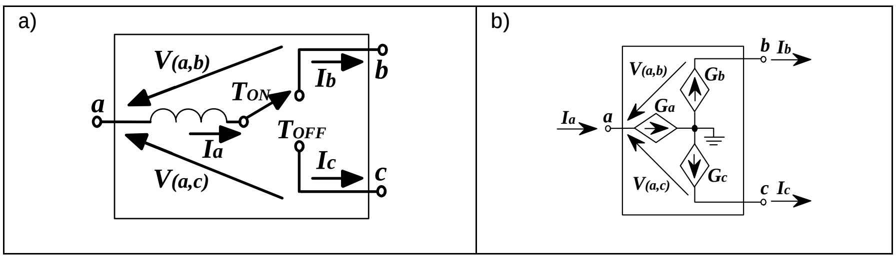

Figure 1.16: a) Switched Inductor Assembly, b) Generic Switched Inductor Model.

This approach differs from previous proposed methods in two main aspects, first, it is structure-independent, as it deals only with the switched inductor in any given converter; except that it has to be properly oriented to fit each given PWM configuration; and second it does not require any analytical manipulation or model transformation as a prerequisite for simulation by a general-purpose simulator. Once the switched inductor is replaced by the proposed equivalent circuit, the system is ready for simulation.

One limitation of this method common to all averaged analysis methods is that the transient response and the small-signal response obtainable through the simulation are averaged responses. Owing to its inherent nature, the proposed equivalent circuit of the switch is incapable of describing processes within the modulation cycle or with a bandwidth close to the switching frequency f.

In [32] three basic blocks for the application of this methodology are presented, a Generic Switched Inductor Model (GSIM), an Inductor Current Generator (ICG), and a Duty Cycle Generator (DCG). The major advantage of the proposed structure-independent models is the fact that they can be defined as a sub-circuit and directly applied to run DC, small signal (AC), and large signal (TRAN) analysis in open and closed loop configurations.

In [33, 34] this method is extended to the converters operating in the current feedback mode. The benefits of this method for teaching are shown in [35]. One application of the GSIM to the modelling of current shared DC-to-DC converters is developed in [36].

Finally, in [37] the GSIM methodology was modified in order to include, in a more accurate way, the conduction losses due to the inductor's resistance and the voltage drops across the switch and diode. In this way it is possible to estimate the real large signal response and the real small signal transfer functions that take into account the damping effect of the losses. The proposed model handles the problems of conduction losses and completely neglects switching losses.

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The major objection to the numerical approach presented in [30-37] is that it lacks of rigorous analytical description of the systems under study (such as state equations and transfer functions). However, this methodology can be used as a trial-and-error simulation procedure in order to simplify and accelerate the design phase of switching systems. Another failure of the method, exhibited in [30], is the lack of flexibility because the GSIM models only one inductor and it cannot be applied to converters with two inductors connected to the common terminal.

Alternative PWM switch models

An alternative to the PWM switch model of [29] was presented in [38]. This paper developed two alternative PWM switch models referred as the “a-PWM switch model” and “c-PWM switch model”. The PWM switch model described in [29] is referred in that paper as the “p-PWM switch model” since it uses terminal p as the common terminal. The p-PWM switch model is natural for the analysis of PWM converters in which the p-terminal is the circuit common like the ideal buck converter. The other two models are used for the analysis of the converters in which the a-terminal is the circuit common like the ideal boost converter and those converters in which the c-terminal is the circuit common such as the ideal CUK converter. Each one of these PWM switch models has three external terminals: p, a, and c. A three terminal PWM-transformer and a parasitic-dependent nonlinear resistor are connected among their external terminals. Any transformer terminal can be selected as the common terminal (and the other two, as input and output terminals), resulting in three PWM transformers: the p-transformer with transformation ratio $1:d$, the a-transformer with transformation ratio $d':1$, and the c-transformer with transformation ratio $d':d$. There are three PWM switch models corresponding to every PWM-transformer. For a given converter circuit, the a- (or p- or c-) PWM switch model would be the natural one to use if the a- (or p- or c-) terminal is the circuit common after all loss elements have been set to zero (or the circuit idealized), all inductors to short-circuits, and all capacitors to open-circuits. After the natural PWM switch model has been inserted in the converter circuit, all three forms of the PWM transformer can be used to manipulate the circuit graphically to a form that can be analyzed by inspection.

These models have been found to be useful not only as design-oriented analysis techniques, but also as teaching and education tools.

Synthesis of the averaged circuit models

In [39] averaged circuit models for switching converters using a direct circuit averaging method are developed. The method proceeds in a systematic form by determining appropriate averaged circuit elements that are consistent with the averaged circuit waveforms. The averaged circuit models that are obtained are syntheses of the state-space averaged models for the underlying switching circuits. An important feature of the method is that it is applicable to switching circuits whose non-switch elements may be nonlinear.

Another PWM switch approach

In [40] there is a method with a different equivalent circuit for the PWM-switch. This PWM-switch model has been developed averaging only the switches of the converter. Its equivalent circuit is formed by a controlled voltage source and a controlled current source that are obtained using the relations between the instantaneous terminal currents and

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voltages. When this model is applying to analyze a converter, a continuous averaged circuit model is obtained. That model will give the same results as the state-space averaging technique. One important quality of this PWM-switch modelling method is that, contrary to others methods revised, the model corresponds directly to the original converter circuit. Only the switches are replaced by their models. All branch currents and node voltages of the converter are directly available from the model as averaged quantities. This model can also be implemented in any circuit-oriented simulation tool. It is a nonlinear, large-signal, averaged model. No small signal assumptions have been made and only the nonlinearity due to the switching process in a converter is included.

Nonlinear large-signal equivalent circuit model

Based on switching function with two states (1 and 0) defined to express the four configurations of two switches, a general unified nonlinear large-signal equivalent circuit model and its mathematics description, which can be used to describe PWM switching converters operating in all the possible conduction modes, is presented in [15]. The equivalent circuit of the PWM switching model includes an inductor. The three terminals of the model have been numbered 1, 2, and 3. Terminal 1 is designated as the active terminal connected to voltage or current source. Terminal 2 is designated as the passive terminal connected to loads. Terminal 3 is connected to an inductor, and denoted as the common terminal. For CUK and Sepic converters, the inductor of the model represents the equivalent inductor. This model includes all the nonlinear characteristics of the original circuits.

1.4.2.5 GENERALIZED AVERAGING AND DYNAMIC PHASORS

Another approach to obtain an average model of a DC-to-DC converter is presented in [21]. This approach offers refinements to the theory of state-space averaging, permitting a framework for the analysis and design when small ripple conditions do not hold, as it takes place in resonant-type converters.

The generalized averaging method is based on the fact that a waveform can be approximated to arbitrary accuracy with a Fourier series expansion. The Fourier coefficients are functions of time since the interval under consideration slides as a function of time. The analysis computes the time-evolution of these Fourier series coefficients as the window of known length slides over the waveform. This representation results in unified time-invariant set of differential equations where the state variables are the coefficients of the corresponding Fourier series of the circuit state variables. Thus, the greater the order of harmonics described in the model, the closer the results will be to the exact topological state-space solution. In practice, some simplifying assumptions can be considered in order to reduce the number of Fourier terms and simplify the calculations.

The switching converters typically have state-space description with some periodic time-dependence. To apply this scheme to a converter, the first step is to compute the relevant Fourier coefficients of both sides of standard state-space description of the instantaneous (switched) variables and averages both sides invoking the properties of dynamic phasors as needed. The next step is to make approximations that allow the averaged model itself to be written in state-space form, using the Fourier coefficients (dynamic phasors) as state variables. The slow variation of the phasors is usually one of the critical assumptions in making reasonable approximations. One of its advantages is the possibility of obtaining

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models with various degrees of detail. With the use of this method is possible to find not only the steady state solution but also the small signal transfer functions.

In [41], the generalized state-space averaging model is applied to the basic DC-to-DC single-ended structures, such as the buck, boost, buck-boost, and CUK. The simulation's results are compared with the exact topological state-space model and the well-known state-space averaging method. It becomes evident that when the switching frequency is not much higher than the converter natural frequencies, the approximation order is an important factor in improving the model accuracy, though at the expense of increasing the calculations. It can also be observed that the results obtained with the generalized state-space averaged in first-order approximation are closer to the approximations of the corresponding ones of the topological model when the duty-ratio is around 0.5 (absence of even harmonics) and for specific state variables. It can also be seen that the structure complexity in terms of number of components does not determine the approximation order for a satisfactory model.

Multi-frequency averaged model MFA

Some details of the generalized averaging method are presented in [42]. Using a boost converter as an example, a new multi-frequency averaged (MFA) model with an additional structure that permits more detailed analytical results is derived. The inherent frequency dependence of these models is studied. Using the boost converter as an example, the details involved in constructing the models applying index-0 and index-1 averaging are showed, these models are able to estimate the average as well as the ripple in state variables, even when the switching frequency is low (and the ripple is large). These index-1 components represent the effect of the ripple on the average values of the state variables. Of course, if it is assumed that the converter has negligible ripple (as is the case in most well-designed converters), then the index-1 terms could be neglected, and there would be no appreciable difference between the index-0 state variables predicted by what is now the conventional state space averaged (SSA) model and the true state variables of the switching converter. The differences between the predictions of normal SSA models and those of the new MFA models become increasingly significant at low-switching frequencies and high-ripple levels.

In-place circuit averaging based on the generalized averaging

Finally, in [43] it is presented a unified approach to in-place circuit averaging that is based on the generalized averaging, this is, the averaged circuit elements are calculated following the outlines of [21] and the equivalent circuit obtained is replaced in the original circuit. This approach allows the refinement of an averaged circuit model to obtain an arbitrary degree of accuracy by including higher order averages in the procedure.

As a final comment it can be said that the generalized averaging method relies on Fourier series representation of the state variables and has been applied to buck, boost and CUK converters. It has to be said that this method involves high order matrix of differential equations in the computation of the Fourier series coefficients evolution, and no known results are available to estimate the number of coefficients needed in the Fourier series representation for any desired accuracy using this method. Typical studies on its application for closed loop stability analysis indicate that the number of complex Fourier series coefficients needed for each state variables can be up to $N=20$ and for a CUK converter with

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four state variables, this involves solving a state-matrix of size $4(2N+1)\times4(2N+1) = 164\times164$. What implies a very complicated computational job [44].

1.4.2.6 SAMPLED-DATA MODELLING METHOD

Sampled-data models are naturally matched to power electronic converters, firstly because of the cyclic way in which power converters are operated and controlled; secondly, because such models are well suited to the design of digital controllers that are increasing their use in power electronics. Like averaged models, sampled-data models allow focusing on cycle-to-cycle behaviour, ignoring details of the intra-cycle behaviour. This makes them effective in studying and controlling ripple instabilities (i.e., instabilities at half the switching frequency), and also in general simulation, analysis, and design.

A sampled-data model can be obtained from the switched model. The state evolution of the variables for each of the two possible values of the switched signal can be described very easily using the standard matrix exponential expressions for LTI systems, and the trajectories in each segment can then be pieced together by invoking the continuity of the state variables. For a well-designed high-frequency PWM DC-to-DC converter in continuous conduction, the state trajectories in each switch configuration are close to linear, because the switching frequency is much higher than the filter cut-off frequency. What this implies is that the matrix exponentials are well approximated by just the first two terms in their Taylor-series expansions. The model obtained by this method can be recognized as the usual forward-Euler approximation of the continuous time model [45].

Discrete-averaging models

The first approximations to sampled-data modelling presented in [46-48] combined the continuous form of state space averaging with the accuracy of discrete modelling. In [46] the sampled-data model has been realized for the high-frequency portion of the buck converter current-loop and the exact continuous-time model obtained has an infinite number of poles and zeros. Consequently, that representation was not so useful for design and analysis applications. The discrete-averaging model of [47] preserved the averaging state variables but the output was determined by a discrete-sampling approach in order to correct the inaccuracy that is introduced when the output voltage expression is averaged because the averaging effect of the output voltage waveform in essence combines the amplitude modulation with the PWM of the ESR capacitor voltage. Then, an expression that will allow determining the envelope of the discrete output voltage is obtained by sampling the output voltage at a constant frequency. This means that the second order term of the numerator in the control-to-output transfer function was eliminated and this results in a model that estimated the high-frequency characteristics more closely than the averaging model. In [48] the same approximation is used for converters in a feedback loop.

The approximate sampled-data models can be more accurate than continuous time averaged models, because they properly represent the cyclic operation of switching converters [49]. They can be used, for example, to predict sub-harmonic instabilities that the averaged models cannot present without far more elaborate treatment. Essentially the same approximate sampled-data models were presented in [46] and in [49]. Those models permit prediction of both sub-harmonic instability and slower dynamics. But the models in [46] are presented in the form of continuous time models that contain impulse samplers,

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even though these are no easier to analyze than the corresponding discrete time systems. The model in [49], works with the discrete-time models directly.

In [50] the author extends the results of discrete-time averaging method presented before to include the effect of feedback loop in the PWM system. This model provides the exact one cycle average values of the output signal with the presence of feedback even at low switching frequency and the basis for discrete-time simulation of the averaged value of any state in the PWM system, even during transient non-periodic operation condition. The result is the one-cycle average large signal model. The accuracy of this method does not depend on the switching frequency.

Continuous approximations of discrete behaviour

The sampled-data modelling has special application in current mode control converters because some small signal characteristics of this mode can only be explained with discrete-time modelling. In [51] the accuracy of sampled-data modelling is combined with the simplicity of the model of the three-terminal PWM switch [29] with the aim of making a complete model that accurately predicts characteristics from DC to half the switching frequency. In order to obtain the model is not necessary to attempt modelling the complete power stage with sampled-data analysis. Instead, only the current-sampling function needs to be modelled, and converted into continuous-time representation to combine with the rest of the power stage and feedback models. The continuous sampling gain is approximated up to half the switching frequency with a complex pair of RHP zeros. This second-order model of the sampled-data system can be chosen to match the exact equation at the lower and upper limits of the frequency range of interest. This model gives the possibility of transfer functions which have more zeros than poles when the current loop gain is derived. The reason for this apparent anomaly is the choice of a model which is good only to half the switching frequency. If the model is extended to higher frequencies, more poles will be needed for accurate modelling and the number of zeros will not be greater than the number of poles. The extra zeros in the current feedback loop will cause additional poles in the closed-loop transfer functions, leading to the significant differences of the model. Based on the same procedure that has been explained, a complete small-signal model for the average current-mode control is presented in [52].

In [53], the modelling approaches presented in [51, 54], are reviewed and compared. Those approaches produce continuous approximations to the discrete behaviour of the current mode controlled converters, and include modulator gain and sampling effects. The “Ridley approach” [51] and the “Tan approach” [54] were based on the same discrete transfer equation. Both of them produce identical transfer behaviour predictions, at least below the Nyquist frequency. However, these two approaches produce distinctly different loop gain predictions. The main difference between the approaches is the derivation of the low-frequency modulator gain, because the Tan approach, in contrast to the Ridley approach, assumes that the sampling should be unity, and the modulator gain is frequency dependent. The loop gain derived using the Ridley approach was found to be in good agreement with the experimental data at both low and high frequencies. The modulator gain predicted by the Tan approach did not agree with the low-frequency loop gain data. It was found that erroneous data could be obtained with the digital modulator if care was not taken to maintain high-ripple rejection in the logic power supply used by the measuring equipment.

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Low frequency sampled data model

In [55] a sampled-data model of switched mode converters applicable for the low frequency range is presented. The assumption made is that sampling rate is high enough as it is dictated by the sampling theorem. Therefore, both sampling and switching frequencies are higher than twice the natural frequency of the converter. The model obtained is linear for small signal operation but represent a bilinear system under large signal conditions.

Sampled data modelling based on slow-fast variables classification

A new focus for the discrete time modelling based on the partition of the state variables in two subsets, one corresponding to the fast variation components, and the other to the slow variation ones, leads to the dynamic description presented in [56]. After this classification a nonlinear discrete recurrence valid in each of the two conduction modes is derived. Subsequently, a special-purpose program based on the discrete recurrence is presented. The same variables partition is used in [57, 58] in order to present two continuous models that are initially described in terms of discrete variables. Afterwards, they are replaced by their equivalent continuous variables. The modelling procedure of [57] derives a small-signal high-frequency model that can be easily programmed for computer-aided analysis. The model of [58] can be used in large-signal analysis of switching regulators provided that any converter time constant be considerably larger than the switching period. It has been validated by comparison with the exact simulation of the regulator differential equations, and the results have shown that the simulation of the proposed model is between eight and ten times faster than the exact simulation. The last modelling procedure was used in [59] in order to get a converter model for applying a new control scheme.

State space model with a high sampled frequency

The issue of considering a high sampled frequency was studied in [60]. This paper proposed a state-space model that may be either a hybrid continuous-discrete-time one or a full discrete-time one. The model was developed according to classical formulations in system theory that includes action of switches in the model as discrete-time systems, but not as external restrictions. Therefore, the switch states are considered additional state variables of the circuit with a true state transition function in the same way than classical state variables (energy state variables), and the control inputs of switches are considered additional inputs of the circuit in the same way than classical inputs (independent sources). Although the circuit is not assumed to be operated cyclically and the number and identity of the energy state variables are allowed to change from one configuration to another, the same model is valid for all operating conditions of the circuit because possible discontinuities at the switching instants are considered. Moreover, this model is valid as a circuit simulator.

Fixed switching frequency sampled-data

The previous work on sampled-data modelling is extended for PWM converters with fixed switching frequency in [61]. General block diagram models for converters in CCM and DCM were proposed. The ramp function, which is crucial in the dynamics, was carefully modelled. The models can be applied to current mode control and voltage mode control, as well as other possible control schemes. Based on the block diagram models, detailed nonlinear and linearized sampled-data dynamics can be derived. Another important feature of this work is that the results are exact if the source and reference voltage signals are constant.

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Employing the last modelling approach, poles and zeros for sampled-data models of buck and boost converters were derived in closed forms in [62]. The closed forms are also numerically verified from the sampled-data dynamics. The closed forms are useful because the effect of different parameters on the pole and zero locations can be readily seen. Accurate knowledge of sampled-data poles and zeros are useful for discrete-time controller design. The sampled-data poles and zeros depend on the switching frequency, the duty ratio, and the modulation scheme. There are some interesting results about the existence, location and shifting of the zeros and poles for the buck, boost and buck-boost converters. Care has to be taken to interpret the sampled-data poles and zeros. No simple correspondence exists between a continuous-time system and its sampled-data version about the number and location of the zeros. The sampled-data model has similar frequency response than the averaged model, even though they have different number and location of poles and zeros. The sampled-data poles and zeros give a different perspective on the DC-to-DC converter dynamics.

Time Lifting Technique

Recent progress in sampled-data control system has resulted in the development of various mathematical tools to handle periodic systems. One of these tools is the lifting technique for continuous time signals, which transform a time periodic system to a LTI system, mapping between two Hilbert spaces. Seeing that DC-to-DC converters are also quasi-periodic systems, time-lifting technique can provide a better way of representing these systems. In [63] the application of the time-lifted concept for DC-to-DC converter was presented, and its corresponding model was derived. In [64] the notion of frequency response of time-lifted DC-to-DC converter system model is introduced, and its definition has been extended to entire frequency range. This is an important difference with the classical forms of frequency response that has been defined up to the half of the switching frequency in sampled data model and is not accurate even at frequencies lower than half of the switching frequency in averaged models. Additionally, the notion of the frequency response power function was extended to the field of PWM converter systems. It has been shown that the sampled data and continuous time approximation are the restricted cases of frequency response power function. Finally, in [65] some computational aspects of the application of this concept was discussed.

As a final comment, it can be said that the sample data approach has some characteristics and advantages that are important to have into account. A common assumption in the sampled-data approach is that source voltage and reference signal can be viewed as constant within each cycle, this assumption is reasonable because the switching frequency is generally very high. Once the circuit operation is assimilated, the derivation of the sampled-data dynamics in various modes and control schemes is straightforward. In this approach, discontinuous conduction mode and current mode control can be handled systematically, making the modelling for these cases simpler than with the use of averaging. Since fewer assumptions than in the averaging approach can be made, the sampled-data approach is more accurate. The only numerical extensive procedure in the sampled-data approach is to find the fixed-point, and the remaining analysis is eased by the analytical form of the dynamic models.

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1.4.3 A SPECIALIZATION IN CONVERTERS MODELLING: THE DCM MODE

In principle, the DCM mode of conduction for DC-to-DC switching converters offers many challenges related to its analysis and control. These challenges have only been considered as a problem to resolve not as a disadvantage. There are also some advantages of this mode of conduction that make this topic even more attractive.

The challenges in the analysis and control can be summarized in the following list: converters in DCM are characterized by the presence of internally controlled switching instants which greatly complicate the analysis and involve high current and voltage peaks and then intensive device stresses. Their conversion ratio M may become load-dependent, their output impedance can be increased, their dynamics are altered and their control of output voltage may be lost when load is removed. Moreover, as it was presented in 1.3, the operation in DCM mode results in an additional topology compared with the operation in CCM mode.

Some converter structures can operate inherently in DCM and can exhibit great challenges in their modelling, as it will be show in the next chapter.

The DCM mode of operation exhibits some interesting features and actually many designers prefer to operate the converter in this mode, even at full load, due to the advantages enlisted next. First, the DCM permits to avoid the reverse recovery problem of the diode. Second, it is considered as a possible solution to the right-half plane (RHP) zero problem encountered in buck-boost and boost derived structures. Third, the DCM allows the simplification of the control in some PFC circuits [12]. The fourth are the low losses associated to zero-current and zero-voltage commutations occurring at internally controlled switching instants and the last one is that DCM allows easier feedback stabilization with respect to CCM mode operating converters. The last advantage, is indeed the main reason by which DC-to-DC converters are often designed to operate in DCM mode [66].

Afterwards, proper analytical models for DCM operation of PWM converters are essential for the analysis and design of converters in a variety of applications, and almost all the methods studied for CCM have an extension for their use in DCM converters. The exception is the generalized multi-frequency averaging [21, 41-43] where the authors have assumed that the inductor currents in the converter are in continuous conduction mode and no attempt has been made to study the application of this method to discontinuous current mode or to converters operating in both continuous and discontinuous modes as in the presence of limit cycles [44].

1.4.3.1 REDUCED-ORDER AVERAGED MODELS

In reduced-order models [5, 11, 23, 24], the inductor current (or one of the inductor currents when there are multiple inductors) does not appear as a state variable. A reduced-order model can correctly predict the behaviour of a converter in the low-frequency range. However, large discrepancies appear at high frequencies (over about one-tenth of the switching frequency), particularly in the phase response. Also, the absence of the inductor current in the averaged model is undesirable for applications such as single phase PFC in which the inductor current is the ultimate control target.

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1.4.3.1.1 CONVENTIONAL STATE-SPACE AVERAGING

In the literature of modelling, the first DCM method cited by everyone is the approach presented in [11]. In that article, the authors described a procedure for DCM modelling that is viewed as a special case of the procedure for CCM modelling. The CCM procedure was explained by the same authors in a previous paper [19] that is described in detail in section 1.4.2.2. In DCM, the starting model for the switching converter is also in terms of the state space description of the switched network even though there are two main differences with CCM mode: The three structural configurations within each switching period, and the behaviour of the instantaneous inductor current whose starts at zero at the beginning of the switching period and falls to zero again even before the switching period has expired.

Therefore, the objective in modelling converters operating in DCM and exhibiting “three state” configuration behaviour is supplementing the generalized state-space averaging step for three state converters by additional constraints which reflect the special behaviour of one of the state variables: the inductor current. Hence the converter, operating in the discontinuous conduction mode (and having three structural changes), may be viewed as a special case of the ordinary "three-state" converters which are free from any restrictions on state variables. Thus, the primary goal is to determine these additional constraints and find how they propagate through the modelling.

First, it is applied the same step than in one ordinary three state switching converter. The original description through three state space equations is substituted by a single state space averaged model. However, as indicated before, the inductor current $i(t)$, does not behave as a true state space variable in the DCM mode since it does not have free boundary conditions (but fixed at zero) which is shown to lead to the following constraint:

$$\frac{di}{dt} \equiv 0 \tag{26}$$

This immediately reduces by one the order of the basic state-space averaged model, since one of the dynamic equations (the inductor current one) reduces to a static equation. In addition to this, an expression describing the average inductor current i can be found directly from the converter itself becoming in the second constraint. This expression is termed the perturbation equation I:

$$i = i\left(v_g, v, d, L, T_s\right) \tag{27}$$

This equation permits to find the average inductor current i in function of the listed variables: T_s, the switching period; L, the value of the inductor; d, the duty ratio; v_g, the input voltage; and v, the output voltage. Thus, the two additional constraints together with the generalized state-space averaging step completely determine the converter model in the discontinuous conduction mode.

It remains only to apply the standard perturbation techniques, and (on the basis of the small signal assumption) the linearization techniques to both state-space averaged equations and the perturbation equation, in order to arrive at the final state-space averaged model. This model gives separately both DC and AC small-signal descriptions through general matrices $\boldsymbol{A}_1$, $\boldsymbol{A}_2$, $\boldsymbol{A}_3$ and vectors $\boldsymbol{b}_1$, $\boldsymbol{b}_2$, $\boldsymbol{b}_3$, of the starting switched models and constraints corresponding to those of (26) and (27).

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Although the results obtained are in terms of linear equations, it can be obtained the circuit realizations. Then, for purposes of illustration, the method can be applied to an ideal boost in DCM.

For the ideal boost of Figure 1.1, the three switched networks in the discontinuous conduction mode of operation are shown in Figure 1.17.

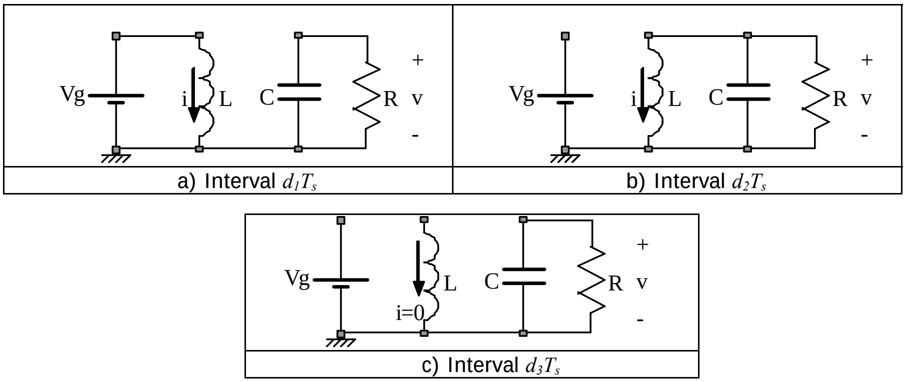

Figure 1.17: Three switched networks of a boost converter operating in DCM

For the choice of the state-space vector $x = (i\ \ v)^T$, the three state space equations of the three linear switched networks in Figure 1.17 become:

$$\dot{\mathbf{x}} = \mathbf{A}_1 x + \mathbf{b}_1 v_g \qquad \text{For interval } d_1T_s$$

$$\dot{\mathbf{x}} = \mathbf{A}_2 x + \mathbf{b}_2 v_g \qquad \text{For interval } d_2T_s$$

$$\dot{\mathbf{x}} = \mathbf{A}_3 x + \mathbf{b}_3 v_g \qquad \text{For interval } d_3T_s \qquad (28)$$

Where

$$\mathbf{A}_1 = \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{RC} \end{bmatrix} \qquad \mathbf{A}_2 = \begin{bmatrix} 0 & -\frac{1}{L} \\ -\frac{1}{C} & -\frac{1}{RC} \end{bmatrix} \qquad \mathbf{A}_3 = \begin{bmatrix} 0 & 0 \\ 0 & -\frac{1}{RC} \end{bmatrix}$$

$$\mathbf{b}_1 = \begin{bmatrix} \frac{1}{L} & 0 \end{bmatrix}^T \qquad \mathbf{b}_2 = \begin{bmatrix} \frac{1}{L} & 0 \end{bmatrix}^T \qquad \mathbf{b}_3 = \begin{bmatrix} 0 & 0 \end{bmatrix}^T \qquad (29)$$

In addition to this, perturbation equation I (27) is needed. However, it can easily be found from Figure 1.17a as:

$$i = \frac{i_{\max}}{2} = \frac{v_g}{2L} d_1 T_s = i\left(v_g, d_1, L, T_s\right) \qquad (30)$$

Equations (29) and (30) contain now all that is needed to determine both DC and AC small-signal models by application of a procedure similar to the described for CCM in

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equations (11) to (25), with the only difference of the constraint (30) and the replacement of the third switching cycle by:

$$\hat{d}_3 = -(\hat{d}_1 + \hat{d}_2) \tag{31}$$

Then the steady-state (DC) model can be obtained following the indications of (24):

$$\mathbf{A}X + \mathbf{b}V_g = 0$$

Where

$$\mathbf{A} = \begin{bmatrix} 0 & -\dfrac{D_2}{L} \\ \dfrac{D_2}{C} & -\dfrac{1}{RC} \end{bmatrix} \qquad \mathbf{b} = \begin{bmatrix} \dfrac{D_1 + D_2}{L} \\ 0 \end{bmatrix} \tag{32}$$

This DCM model is subject to the constraint in (30), whose form in steady-state is

$$I = \frac{V_g}{2L} D_1 T_s \tag{33}$$

The solutions of (32) are the following equations

$$\frac{V}{V_g} = 1 + \frac{D_1}{D_2} \tag{34}$$

$$I = \frac{V}{D_2 R} \tag{35}$$

Hence, the DC conditions depend only on duty ratios D_1, D_2, and resistance R. In (34) it can be observed that the boost converter has even in the DCM the step-up property. By the use of the additional constraint (33), together with (34) and (35), D_2 is determined as

$$D_2 = \frac{V}{R} \frac{2L}{D_1 T_s V_g} \tag{36}$$

The small-signal model can be obtained following the indications of (25) and (30):

$$\begin{bmatrix} \dfrac{d\hat{i}}{dt} \\ \dfrac{d\hat{v}}{dt} \end{bmatrix} = \begin{bmatrix} 0 & -\dfrac{D_2}{L} \\ \dfrac{D_2}{C} & \dfrac{1}{RC} \end{bmatrix} \begin{bmatrix} \hat{i} \\ \hat{v} \end{bmatrix} + \begin{bmatrix} \dfrac{D_1 + D_2}{L} \\ 0 \end{bmatrix} \hat{v}_g + \begin{bmatrix} \dfrac{v_g}{L} \\ 0 \end{bmatrix} \hat{d}_1 + \begin{bmatrix} \dfrac{v_g - v}{L} \\ \dfrac{I}{C} \end{bmatrix} \hat{d}_2 \tag{37}$$

with the additional constraints:

$$\frac{d\hat{i}}{dt} = 0 \tag{38}$$

$$\hat{i} = \frac{I}{V_g} \hat{v}_g + \frac{I}{D_1} \hat{d}_1 \tag{39}$$

The introduction of the constraints (38) and (39) in (37) reduces the first dynamic equation in a static one and the dynamic model becomes in the next expressions, which include also the equation of the additional constraint of (39).

$$-D_2+(D_1+D_2)\hat{v}_g+V_g\hat{d}_1+(V_g-V)\hat{d}_2=0 \tag{40}$$

$$C\frac{d\hat{v}}{dt}=D_2\hat{i}-\frac{\hat{v}}{R}+I\hat{d}_2 \tag{41}$$

In (40) it is possible to determine the modulation of the second interval d_2 in terms of the other DC and AC quantities. Finally substituting (39) and (40) in (41) it is possible to complete the dynamic description to obtain:

$$C\frac{d\hat{v}}{dt}=-\left(\frac{D_2I}{V-V_g}+\frac{1}{R}\right)\hat{v}+\left(\frac{D_2}{V_g}+\frac{D_2+D_1}{V-V_g}\right)I\hat{v}_g+\left(\frac{D_2}{D_1}+\frac{V_g}{V-V_g}\right)I\hat{d}_1 \tag{42}$$

As a conclusion of this method it is important to remark that this model considers that the inductor current does not behave as a true state space variable in DCM since it does not have free boundary conditions (but fixed at zero), which leads to the constraint that reduces the dynamic equation of the current to a static equation. Then the order of the final averaged model is reduced by one from those of the original state-space model because of the imposed constraint.

In [67] this state space averaged method in DCM was applied for modelling the small signal behaviour of the Cuk converter operating in DCM and controlled by a PWM. As the method describes, two constraints have to be applied to the two inductor currents. The voltage of the input capacitor has to be calculated operating on the equation of its current. The results of the modelling were the analytical formulation of both input-to-output and control-to-output transfer functions. Both transfer functions are of third order which implies a reduction of order with respect to the CCM mode as was expected when it is used this method of modelling.

An inconsistent use of variables of this DCM method was reported in [68]. Due to the fact that the average inductor current in the averaged definition (12) (as an element of X) is a true average over an entire switching cycle, but in the second constraint (39), the inductor current is defined as the average over the first two intervals of a switching cycle and differs from the true average by a factor that can be calculated for every case. These two different quantities are treated in this method [11] as if they were interchangeable.

1.4.3.1.2 SLOW-FAST VARIABLES APPROACH

This modelling method [23, 24], which has been already presented in CCM modelling methods, can also be used in DCM mode. The essence of this method is the partitioning of converter state variables into slow and fast ones, from which an averaged model is derived in three steps.

Due to the behaviour of the inductor current in DCM that reaches a peak when the switch turns off and resets to zero before the end of a switching cycle, it can be considered a fast variable. Then, it can be applied the same procedure described in the section of the modelling methods in CCM to derive a reduced-order averaged model. The model obtained

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is the same reduced order model of the averaging method. Nevertheless, this one avoids the inconsistency problem in the calculation of the inductor current average.

It is important to remark that this method is not applicable to all converters because of some limitations that were described in 1.4.2.2.

1.4.3.1.3 CIRCUIT AVERAGING

As an alternative to state-space averaging, circuit averaging has been applied to model DCM PWM converters too. The switch cells defined in [5] are three-terminal circuits containing the switch, the diode, as well as the inductor in the case of DCM operation. The equivalent average circuit for the DCM switch cell is a three-terminal static network described by algebraic terminal relations. Since the inductor has been included in the switch cell but the equivalent average circuit is a static network, it is apparent that the inductor will disappear in the final averaged circuit model of the converter. Therefore, the use of the equivalent average circuit presented in [5] for DCM PWM switch cell also yields a reduced-order averaged converter model. Furthermore, it can be readily checked that the resulting averaged model is the same as the reduced-order models getting with the last two methods. However, as it was shown in [68], large discrepancies exist between model prediction and responses at high frequencies, especially in phase response.

1.4.3.2 FULL-ORDER AVERAGED MODELS

Following some modified procedures to the modelling methods described for converters in CCM, it is possible to find out a full order model, this is, a model that includes also the variables in discontinuous mode. These methods improve the model approximation to the converter real behaviour at high frequencies as it will be shown.

1.4.3.2.1 EQUIVALENT DUTY RATIO METHOD

The method presented in [14] is based on the definition of an equivalent duty ratio, m, as a function of the actual duty ratio d. The converter is then treated as if it worked in the continuous conduction mode with the duty ratio of the switch at m rather than d. Consequently, the averaged model is obtained. The equivalent duty ratio m is defined as the ratio of the average diode voltage over the average of the total voltage across both the switch and the diode.

$$m \equiv \frac{\bar{v}_d}{\left(\bar{v}_S + \bar{v}_d\right)} \tag{43}$$

For each mode, the equivalent duty ratio is a function of the duty ratio, the active switch, the input voltage, and the output current. Nevertheless, it does not depend on any particular converter topology.

$$m = m\left(D, \frac{V_g}{I_{out}}\right) \tag{44}$$

In the discontinuous modes studied in this paper the equivalent duty ratio is a load-dependent function, which indicates that PWM converters in the DCM exhibit a non-zero output resistance at DC. Some geometrical considerations in the waveform of the inductor current were used in order to obtain the relationships between the variables that permit to reach the equation of the equivalent duty ratio for every conduction mode.

A small-signal AC model is derived using the general method described in [11] but without using the constraint equations. Therefore, the average of the inductor current is computed over the complete switching cycle. The averaged AC model incorporates the state-space averaged model of the power stage but replacing the steady-state duty ratio D by the steady-state equivalent duty ratio m. The effects of the discontinuous mode are taken into account via additional feedback loops with gains that depend on the steady-state operating point.

The structure of the model implies two general conclusions regardless of the operating mode and specific circuits. First, the order of the model in the discontinuous modes is the same as the order of the state-space averaged model in CCM. Second, the zeros of the control-to-output transfer function (including RHP zeros, as may be the case) in the discontinuous mode are the same as the zeros of the control-to-output transfer function in CCM. The zeros exhibit the same dependence on the circuit parameters and the DC conversion ratio, regardless of the mode of operation.

In the AC model, the load-dependence of the conversion ratio implies lossless damping in the dynamic response of the converter. The effect is similar to the effect of the current-mode programming on the power stage in CCM where a pair of complex poles is split into a low-frequency and a high-frequency pole. The poles are well-separated if both the converter operates away from the boundary with CCM and the output-filter time constant (RC) is much larger than the switching period. In practice, the latter condition is always satisfied because the output voltage must have a low AC ripple. In DICM, if the poles are well-separated, the high-frequency pole is higher than approximately one third of the switching frequency. This result is also quite general because it is derived without reference to any particular PWM structure. The effect of the high-frequency pole is noticeable in the measured responses presented in the paper. Those measurements confirm that the full-order averaged model provides improved predictions when compared to the earlier, reduced-order state-space-averaged model for DICM.

As a conclusion, it can be said that this modelling method is a variety of the well-known state-space averaged model for CCM.

1.4.3.2.2 AVERAGE-SWITCH MODELS

The DCM PWM Switch

The pulsewidth modulation (PWM) switch of [29] is extended and used in [69] to the analysis of PWM converters operating in discontinuous conduction mode (DCM). As in the case of continuous conduction mode (CCM), the model of the PWM switch in DCM represents the DC and small-signal characteristics of the nonlinear part of the converter, which consists of the active and passive switch pair as shown in Figure 1.15a. In contrast to the model in CCM, the model of the PWM switch in DCM contains small-signal resistances which damp the low-pass filter to the point where two real poles are formed. The physical significance of these small-signal resistances is easy to understand as they represent the load dependent nature of the conversion ratio of converters in DCM.

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Whereas, the use of the PWM switch model in CCM yields the same results as those given by the method of state-space averaging, in DCM the model of the PWM switch yields results that are different than those given by state-space averaging [11]. The fundamental difference between the two methods is that state-space averaging predicts that the discontinuous current state does not contribute to the order of the average model while the PWM switch model predicts that there is simply neither theoretical nor experimental justification to the disappearance of the discontinuous current state from the average model as previously believed.

Prior to the development of the methods of analysis known today, power supply designers observed the transient response of power supplies in continuous and discontinuous conduction mode. For the buck, boost, and buck-boost converters operating in CCM, the transient response was clearly seen to be second order. In DCM, however, the transient response of these converters seemed to be first order. The methods of analysis that were developed later, namely the method of state-space averaging, literally were constrained to yield results that would corroborate the observed first-order transient response. The phase response in a simple frequency-response measurement (up to one-half the switching frequency), however, clearly shows that the system is still a second-order system. The model of the PWM switch in DCM explains these results in a very simple and succinct way. When the model of the PWM switch in DCM is substituted in the converter while the inductor is left intact, the system has two real poles. The first pole is the same as that given by state-space averaging, whereas the second pole occurs in the range of frequencies greater than F_s/π. The contribution of the second pole on the phase response can be significant and easily verifiable in the frequency range below one-half the switching frequency. Furthermore, since the second pole corresponds to a time constant shorter than half the switching period, its contribution to the transient response will decay in one switching period or less. Therefore, the observed transient response will be dominated by the first pole [69].

The expressions for the average terminal currents and voltages of the PWM switch in DCM are calculated using geometrical considerations in the instantaneous waveforms of Figure 1.18a. Therefore, the relationships between the averaged terminal voltages and currents can be deduced, and it is possible to obtain the DC averaged model that can be seen in Figure 1.18b and the small signal model of Figure 1.18c.

Afterwards, the models of the PWM switch are replaced in the circuit in order to analyze the converters in DCM mode. Some interesting results obtained by the analysis are: First, the high frequency pole, which starts at F_s/π Hz when the converter is operating at the boundary between DCM and CCM, begins to move outwards as the converter enters deeper into DCM, this result is general and common to the buck, boost, buck-boost, and CUK converters. It clarifies the reason why the contribution of this pole to the magnitude response is hardly noticeable but the contribution to the phase response is quite noticeable. Second, the conversion ratio in DCM, that is larger than the conversion ratio in CCM for the same structure.

In addition to the widespread belief that the order of PWM converters in DCM was less than their order in CCM by one, there existed the myth that the right-half-plane zero in the control-to-output transfer function of the boost and buck-boost converters in CCM simply disappeared in DCM, but with the use of PWM switch model it is found that the right-half-

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plane zero has exactly the same dependence on the circuit parameters and the conversion ratio as it does in CCM. This was demonstrated in [69] for the CUK, boost and buck-boost converters. The relative position of the right-half-plane zero to the second pole was also determined, so it was verified that the right-half-plane zero occurs always after the second pole for the boost and buck-boost converters.

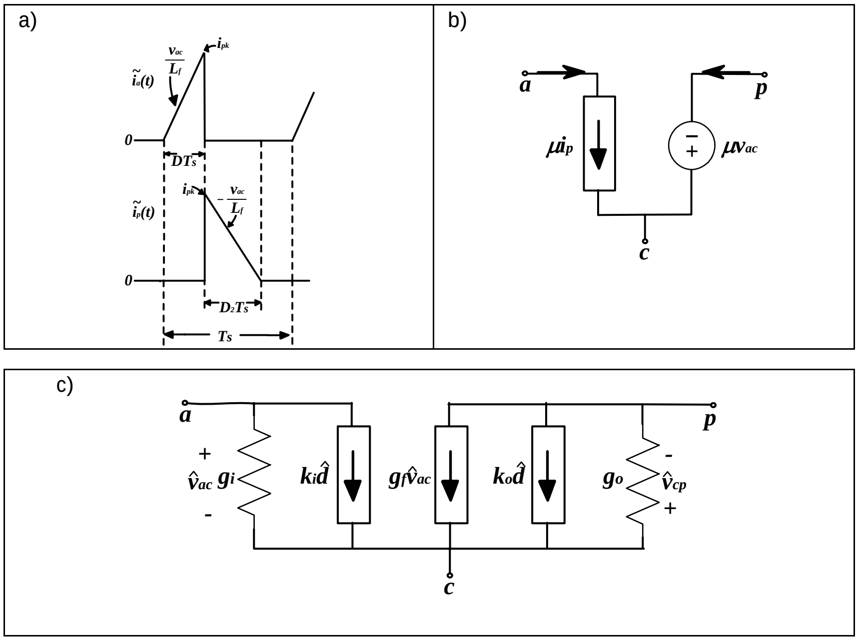

Figure 1.18: a) Terminal currents of PWM Switch, b) DC averaged model of PWM in DCM c) Small signal model of PWM switch in DCM

The PWM Switch model is critically examined in [30]. There is suggested that the omission of the inductor from the model has led to errors in the modelling of DCM because its operation is not a function of the voltage across the inductor. The author affirms that models that attempt to replace the switching part of PWM converters must include information on the voltage across the terminals of the inductor especially in DCM mode in which the switching periods may be a function of the inductor voltage. In the same paper [30], the author of [29, 69] explains that exclusion of the inductor, thence, the exclusion of the inductor voltage, was made taking into account the differences between average (continuous) and instantaneous (discrete) quantities, and the fact that in discontinuous conduction mode the average voltage per cycle across the inductor is always zero, even under a transient. Therefore, the inclusion of the inductor in the model is not necessary, and it might be harmful by diminishing the flexibility and versatility of the modelling technique.

Alternate PWM switch cell models

The recognition that any of the three PWM switch cell terminals can serve as the common terminal leads to two alternate PWM switch cell models that were defined in [70, 71], and can be seen in Figure 1.19.

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For a given converter, one of the three PWM switch models defined in the Figure 1.19 is more “natural” for graphic-oriented analysis design, e.g., it allows the idealized converter to be analyzed by inspection. The PWM switch model of DCM converters described in [69] can be referred as the “c-PWM switch model” since it uses terminal c as the common terminal. The c-PWM switch model is “natural” for the analysis of PWM converters in which the c-terminal is the circuit common. Thus, it enables the ideal buck-boost converter and CUK converter to be analyzed by inspection. The two alternate PWM switch models, the “p-PWM Switch Model” and “a-PWM Switch Model”, would facilitate the analysis of those converters in which the p-terminal is the circuit common (e.g, the ideal buck converter), and the a-terminal is the circuit common (i.e., the ideal boost converter).

The common terminal for a given converter circuit can be found after all loss elements have been set to zero (or the circuit idealized), all inductors to short-circuits, and all capacitors to open-circuits. This way, it is possible to decide what is the natural PWM switch model to use (c- or p- or a-).

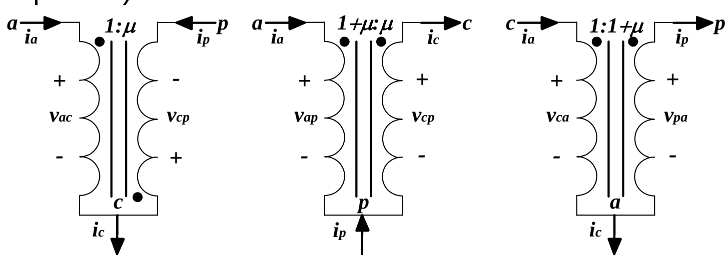

Figure 1.19: Three forms of the PWM Switch Model

The three forms of the PWM switch models are used in [71] only for steady state analyses of ideal converters and converters with parasitics.

The DCM averaged model derived in this approach is exactly the same as that obtained using the equivalent duty ratio method presented in the previous subsection [68].

The Unified Switched Inductor Model (USIM)

The SIM (switched inductor model) originally introduced in [31] for PWM converters operating in CCM, is also extended to describe the DCM conditions in [72], where the authors proposed a unified Switched Inductor Model (USIM) that uses the idea that the CCM is a limit, or special case, of the DCM. In order to define the USIM, the basic switched inductor assembly of Figure 1.16a is switched at a duty ratio D_{ON}, for port b, and D_{OFF} for port c, where:

For CCM $$D_{OFF} = 1 - D_{ON} \quad (45)$$

For DCM $$D_{OFF} < 1 - D_{ON} \quad (46)$$

The equivalent circuit of the USIM is developed by considering the various possibilities of the inductor current waveforms, DICM and CCM, and applying a geometric approach to their analysis. Thus, the relationships between the average inductor currents of the ports (a, b and c), and the peak inductor current can be obtained. Once the basic equivalent circuit of the switched inductor is constructed, large and small signal simulation becomes trivial. All

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that is required in order to simulate a given structure is the node connection and the values of the components. During simulation, the model automatically follows the CCM and DCM operation, with fewer convergence problems compared to previous simulation models.

For the DCM case the average inductor current is an algebraic (and not a dynamic) function of the controlling parameters in the three basic blocks defined in [32]: the Generic Switched Inductor Model (GSIM), the Inductor Current Generator (ICG), and the Duty Cycle Generator (DCG). In other words, the currents of the GSIM are related to the peak current by simple geometrical relationships obtained from the current waveforms.

The extension of the GSIM methodology in order to include the conduction losses due to the inductor's resistance and the voltage drops across the switch and diode presented in [37], is also applicable to both current conduction mode (CCM) and discontinuous conduction mode (DCM) operations. The switching from one to the other is automatic by selecting the correct D_{OFF} for each case. As in the last explanations, the expression for D_{OFF} is calculated using geometrical considerations.

DCM circuit model including parasitics

A small-signal circuit model composed of controlled current sources, an independent voltage source and resistances, where the principle of energy conservation approach was used to take into account parasitic resistances of the transistor and diode, like the diode threshold voltage, was presented in [73]. Because it is a DCM model, the approximation that the current through the inductor is nearly constant cannot be used. Therefore, the true RMS value of the currents through the converter components has to be considered to determine the averaged values of parasitic components. Furthermore, in order to calculate the average current through the inductor branch of the circuit, some graphical assumptions using geometrical approximations in the inductor current waveform were made. The proposed model is suitable for small-signal, frequency-domain representation of the converters. As an example it was used to derive the expressions of control-to-output transfer function, input-to-output voltage transfer function, input impedance and the output impedance for a boost converter [73, 74] and a buck-boost converter [75].

1.4.3.2.3 SAMPLED DATA MODELS

Zero-order-hold

In [76] a zero-order hold (ZOH) equivalent discrete time model of the boost converter for computing its small signal frequency response and closed loop behaviour for both large and small signals is derived and experimentally confirmed. In this model, non-ideal conductive loss effects can be taken into account in continuous and discontinuous inductor current modes. An implicit equation for the determination of the duration of the conduction current in the inductor has been explicitly characterized in terms of the parameters of the converter. The computation of the frequency response needs a discrete-time steady-state simulation at each frequency. Then it is necessary to make a comparison between the magnitudes and phases of the output voltage and input sinusoid that is computationally intensive. Therefore, an alternative faster method using Newton-Raphson technique to accelerate the computation of the frequency-response from the developed discrete-time model is introduced in this paper. The ability of the sampled-data model to capture large signal behaviour has been demonstrated by experiment and simulations of the closed loop system

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subject to set point perturbations. It is observed that the small signal behaviour holds only for 1 % perturbations of the set point waveform in these experiments and simulations. The smallness of the region of linear behaviour can be used to capture nonlinear behaviour of the converter over larger perturbations.

Comparative study

In [44] a comparative study between multi-frequency averaging and sampled-data models has been done throughout the examples of the multi-frequency literature, that were reworked using the sampled-data models. It has been found that the lower-order sampled data models can provide all the results derived before by the higher-order multi-frequency literature but with less computational effort. Specifically, using the sampled-data models, it is shown that the steady-state ripple for such converters in CCM and DCM can be easily computed with and without feedback, and can be used to assess closed-loop stability.

Approach to the state-space model reduction problem

The problem of state-space model reduction for DC-to-DC switching converters has been treated in [66]. A sampled data approach has been adopted to find a discrete-time full order state-space model of the circuit valid for all operation modes. In [13] it is shown that further complex DCM modes can be entered by DC-to-DC converters under extreme load conditions, i.e., in every converter operating in DCM there are combinations of switches ON-OFF states forcing some state variable either (a) to rest at zero (frozen state) or (b) to linearly depend (ghost state) on the remaining state variables, within entire intervals of the switching period. In both cases one state is lost in the state-space model and these intervals are called reduced state phases.

The full-order discrete-time large signal model of the circuit is firstly determined by adopting resistive non ideal models for switching devices and a moving polynomial approximation for the calculation of internally controlled switching instants. The model is based on a moving linear interpolation of the diode current and voltage for the calculation of the instants where reduced state phases start. A full-order small-signal model is then obtained allowing the analysis of joint controllability and observability properties of the circuit. The principal component analysis is then applied to perform a structural decomposition of the system into a dominant subsystem, which carries most of the energy of the control-to-output impulse response, and a weak subsystem, which contributes little to the response so that it may be neglected in the control-to-output analysis of the circuit. This way, the principal component analysis has been used to establish an energetic criterion for order reduction. It has been shown that in all discontinuous modes a proper order reduction can be usually performed, provided that the joint controllability-observability of a balanced realization of the original system is analyzed.

Large signal model

A large signal model of a converter operating in DCM can be calculated using the methodology presented in [58]. That methodology is based on the nonlinear discrete recurrence relating the state vector at the beginning to the state vector at the end of the cycle and, in order to detect this mode of operation, an auxiliary variable that is defined as a linear combination of the fast-variation components. Afterwards, as in the current injected method, a nonlinear continuous formulation is obtained in the next step by defining and

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generating a set of continuous variables equivalent to the discrete ones at the beginning of the cycle.

1.4.3.2.4 CURRENT INJECTED APPROACH

In the Chapter Two of [16] it is illustrated the DCM application of the dynamic method already described in 1.4.2.3 for CCM. The transfer functions of the three basic converters operating at constant frequency with duty ratio control in DCM mode, that the authors have called light mode, were derived in a step by step procedure and tabulated in order to facilitate their use. The mathematical procedure includes the calculation of the mean current injected from the inductor by geometrical considerations applied in the figure of the inductor current waveform in DCM mode.

It is important to remark a significant difference between expression for the injected current in CCM and the corresponding expression for DCM: the DCM Injected current has no term corresponding to the first term at the CCM injected current. This first term indicates the dependence of the injected current at the beginning of the switching interval; no such dependence exists in DCM because there, the inductor current begins at zero in every cycle. This additional dependence in CCM results because the inductor stores energy during the entire switching period; the energy the inductor receives from the source in one switching period is not transmitted entirely to the output network during the same period. The waveform of the inductor current in one period depends on the voltage that had been applied to the inductor during the previous period (i.e., in CCM, the inductor provides circuit “memory” from one cycle to the next; no such phenomenon exists in DCM). As a result, the transfer functions for CCM are completely different from those for DCM.

In [77] the CIECA introduced in 1.4.2.3 is extended to the converters operating in DCM and applied to obtain the models of the three basic converters.

1.4.3.2.5 LOSS-FREE RESISTOR MODEL

Reference [3] also presents an equivalent circuit model for the PWM DCM switch cell. Unlike the average circuit models, which use dependent voltage and current sources, the average circuit developed in [3] is represented by a dependent power source and a so-called loss-free resistor. It can be easily verified that both circuits are in fact equivalent and lead to the same full-order averaged converter model for a given converter structure.

This approach begins with the identification of the general two-switch (MOSFET and diode) network and its terminal currents and voltages. Then, all the waveforms that correspond to the inductor and to the switch network currents and voltages are drawn. Afterwards, the averaged terminal equations and the second duty cycle of the switch network in DCM are calculated using the waveforms and geometrical considerations. Next, using the relationships between terminal variables already calculated, the authors construct an equivalent circuit corresponding to the averaged switch network.

The averaged large-signal model of the general two-switch network in DCM is illustrated in Figure 1.20. The input port behaves effectively as resistance R_e. The instantaneous power apparently consumed by R_e is transferred to the output port, and the output port behaves as a dependent power source. This lossless two-port network is called the loss-free resistor model (LFR). The loss-free resistor represents the basic power conversion properties of DCM switch networks. In order to calculate the steady state and large signal behaviour of any

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converter circuit, the switch-network has to be replaced by the LFR model. For the small signal response, it can be used the small signal equivalent circuit of LFR also reported in [3].

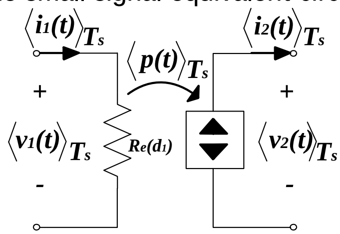

Figure 1.20: The lost free resistor –LFR– Model

1.4.3.2.6 REVISED AVERAGING APPROACH

Considering, as a starting point, the unsatisfactory situation in the modelling of discontinuous conduction mode DCM, the authors of [12] have studied the various issues involved in DCM modelling, starting with a re-examination of all existing models. The paper presents a physically-based modelling procedure for PWM converters which serves as a general framework for comparing different models, along with new full-order averaged models, in both analytical and circuit forms that overcome the problems of existing models.

In general, some of the problems of the existing models are the following. In reduced-order models (1.4.3.1), the inductor current (or one of the inductor currents when there are multiple inductors) does not appear as a state variable. A reduced-order model can correctly predict the behaviour of a converter in the low-frequency range. However, large discrepancies appear at high frequencies (above about one-tenth of the switching frequency), particularly in the phase response. Also, the absence of the inductor current in the averaged model is undesirable for applications such as single-phase PFC in which the inductor current is the ultimate control target. In full-order averaged models (1.4.3.2), the inductor current is retained and they have shown improved accuracy over reduced-order models. However, relatively large discrepancies still exist at high frequencies. Moreover, the model developments did not include analysis of accuracy, and it was not quite clear what attributes of these full-order models contribute to their improved accuracy.

In order to derive the basic equations of this method, the Figure 1.21 was used. This figure reflects the fact, already mentioned, that DCM operation of PWM converters differs from CCM (continuous conduction mode) operation by an additional time interval in each switching cycle during which an inductor current or capacitor voltage is clamped to zero (or a constant when there are multiple energy storage elements).

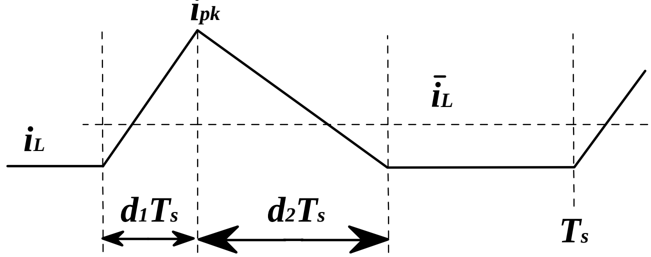

Figure 1.21: Inductor current waveform of PWM converter in DCM

Consider a DC-to-DC converter with two switches. For DCM operation involving inductors, the inductor current rises in the first interval d_1 when the switch is turned on, reaches a peak when the switch is to be turned off, and resets to zero (or a constant) at the end of the second interval d_2.

The converter can be described accurately with a piecewise-linear state-space model that was already presented in (28). Notice that the second duty ratio, d_2, in DCM is not independent, but rather has algebraic dependency on state and control variables. For the purposes of an averaged model, it is necessary to reflect this dependency in terms of the average values of voltage and current. That way, the second duty ratio can be eliminated and a model expressed solely in the averaged state variables can be obtained. The algebraic function defining this dependency is called the duty-ratio constraint in this paper.

The modelling method employed for DCM operation consists of three steps: Averaging, Correction, and Duty-ratio constraint. That will be explained in detail in the following paragraphs.

Averaging and Correction

As in the continuous conduction mode, state-space averaging can be applied to (28) to give the following averaged model, where $\bar{\mathbf{x}}$ denotes the average of $\mathbf{x}$ over an entire switching cycle.

$$\dot{\bar{\mathbf{x}}} = \left(d_1\mathbf{A_1} + d_2\mathbf{A}_2 + (1-d_1-d_2)\mathbf{A}_3\right)\bar{\mathbf{x}} + \left(d_1\mathbf{b_1} + d_2\mathbf{b}_2 + (1-d_1-d_2)\mathbf{b}_3\right)v_g(t) \quad (47)$$

The problem with the state-space averaging approach in DCM is that it averages just the matrix parameters, and not necessarily the state variables themselves. It is intended that (47) will apply when the true average of each state variable is used, but the average inductor current depends on the parameters and duty ratios. In CCM, the average of the duty ratio and inductor current products is the same as the product of the averages, and state-space averaging gives the same result as formal averaging of the circuit equations. In contrast, in DCM the average of product terms in the inductor current equation will not be the same as the product of the averages.

Based on the waveform shown in Figure 1.21, the average of the inductor current can be written as

$$\bar{i}_L = \frac{i_{pk}}{2}(d_1 + d_2) \quad (48)$$

Now consider a general case in which a capacitor is connected to the inductor when the switch is on ($t \in [0, d_1T_s]$). The current delivered to the capacitor is not necessarily the same as the average inductor current.

Since the inductor current is changing rapidly with time, it is convenient to formulate the capacitor equation in terms of conservation of charge before performing the averaging step.

In this case the total amount of charge that the capacitor receives from the inductor over a switching cycle is:

$$Q_C = \frac{i_{pk}d_1T_s}{2} \quad (49)$$

This is equivalent to an average charging current of:

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$$\frac{Q_C}{T_s} = \frac{i_{pk} d_1}{2} \tag{50}$$

If the capacitor is connected to a resistive load, the net charge delivered to the capacitor on the average is:

$$C\frac{dv_C}{dt} = \frac{i_{pk} d_1}{2} - \frac{v_C}{R} \tag{51}$$

This result is a fundamental implication of charge conservation in the capacitor. Notice, however, that it is not the same as the KCL expression for the capacitor generated by state-space averaging. The state-space averaged model (47) would imply that the equivalent average current charging the capacitor is $\bar{i}_L d_1$, that is, the average of the inductor current times the duty ratio of the subinterval in which the capacitor is charged by the inductor, which will be called the state-space-averaged (SSA) charging current. Using (48), the SSA equivalent charging current can be written as

$$\bar{i}_L d_1 = \frac{i_{pk} d_1}{2}(d_1 + d_2) \tag{52}$$

That is different from the actual charging current identified in (50). The implication is that an unmodified SSA approach, in which the averaging step is performed on a complete model rather than on the equations themselves, might not preserve charge conservation under DCM conditions. The correction to reflect (50) does not involve any inconsistency: in continuous mode, the conventional SSA model results regardless of how the averaging step is performed. In DCM, the rapid change in inductor current requires that averaging be performed more formally on the KVL and KCL expressions.

Table I

Charging of Capacitor by an Inductor Operating in DCM

Inductor Charging Capacitor	SSA Equivalent Charging Current	Actual Equivalent Charging Current
When Switch in ON	$\bar{i}_L d_1 = \frac{i_{pk} d_1}{2}(d_1 + d_2)$	$\frac{i_{pk} d_1}{2}$
When Switch in OFF	$\bar{i}_L d_2 = \frac{i_{pk} d_2}{2}(d_1 + d_2)$	$\frac{i_{pk} d_2}{2}$
Over the Entire Cycle	$\bar{i}_L (d_1 + d_2) = \frac{i_{pk}}{2}(d_1 + d_2)^2$	$\frac{i_{pk}}{2}(d_1 + d_2)$

Table I shows the difference between the actual average charging current and the SSA charging current for a capacitor that is connected to the inductor when the switch is on, off, or over the entire switching cycle. Responses defined by the original state-space averaged model (47) would be expected not to match the actual averaged response of the converter because of these differences. A modification of (47) is therefore necessary to correct for this mismatch. As can be seen from Table I, this can be achieved by dividing inductor current(s) on the right-hand side of (47) by the factor $d_1 + d_2$. In order to apply this operation to the state space averaging, first it has to be defined a matrix $\boldsymbol{M}$ as follows:

$$\mathbf{M} = diag\left[\frac{1}{d_1 + d_2},\ldots,\frac{1}{d_1 + d_2},1,\ldots,1\right] \tag{53}$$

The number of elements that are different from *1* is equal to the number of inductor currents in (47). With this, the modified averaged model that would correctly predict the behaviour in DCM becomes

$$\dot{\bar{\mathbf{x}}} = \left(d_1\mathbf{A_1} + d_2\mathbf{A}_2 + (1-d_1-d_2)\mathbf{A}_3\right)\mathbf{M}\bar{\mathbf{x}} + \left(d_1\mathbf{b_1} + d_2\mathbf{b}_2 + (1-d_1-d_2)\mathbf{b}_3\right)v_g(t) \tag{54}$$

As an example of application of this correction, it can be considered the ideal boost of Figure 1.1. The three switched networks for the boost in DCM were shown in Figure 1.17 and the state matrices and input vectors were established in (28) and (29).

Since there is only one inductor and the dimension of $\boldsymbol{x}$ is two, the modification matrix is simply

$$\mathbf{M} = diag\left[\frac{1}{d_1 + d_2},1\right] \tag{55}$$

Hence using (54), the modified averaged model of the boost converter in DCM is

$$\frac{d}{dt}\begin{bmatrix}\bar{i}_L \\ \bar{v}_C\end{bmatrix} = \begin{bmatrix} 0 & -\dfrac{d_2}{L} \\ \dfrac{d_2}{C(d_1+d_2)} & -\dfrac{1}{RC}\end{bmatrix}\begin{bmatrix}\bar{i}_L \\ \bar{v}_C\end{bmatrix} + \begin{bmatrix}\dfrac{d_1+d_2}{L} \\ 0\end{bmatrix} v_g \tag{56}$$

Duty-ratio constraint

The derivation of a full-order model starts from the modified averaged model (54). Unlike the conventional approach that relies on the volt-second balance relation for the definition of d_2, a different duty-ratio constraint will be derived here. Equation (48) can be used for this purpose.

If it is considered the boost converter again, v_g is the voltage across the inductor when the switch is on (during $[0, d_1T_s]$), and the inductor peak current can be written as

$$i_{pk} = \frac{v_g}{2} d_1 T_s \tag{57}$$

Substituting this into (48) and solving the resulting equation for d_2 yields

$$d_2 = \frac{2L\bar{i}_L}{d_1 T_s v_g} - d_1 \tag{58}$$

That is different from the result based on the volt-second balance relation because it enforces the correct average charging of the output capacitor i.e. this expression balances both flux and charge as the converter operates.

The duty-ratio constraint (58) can be substituted into the modified model (56), which was obtained using (54), in order to generate the revised full-order averaged model for boost converter in DCM that can be seen in the next equation:

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$$\begin{aligned} \frac{d\bar{i}_L}{dt} &= \frac{2\bar{i}_L}{d_1 T_s}\left(1-\frac{\bar{v}_C}{v_g}\right)+\frac{d_1\bar{v}_C}{L} \\ \frac{d\bar{v}_C}{dt} &= \frac{\bar{i}_L}{C}-\frac{d_1^2 T_s v_g}{2LC}-\frac{\bar{v}_C}{RC} \end{aligned} \tag{59}$$

DC Analysis

The DC operating point of the boost converter with a constant duty ratio $d_1=D_1$ can be determined by letting the right-hand sides of the differential equations of (59) equal to zero and solving the two resulting algebraic equations for i_L and v_C. Let the scalar value of M be the intended output–input voltage ratio. The results can be expressed as

$$\begin{aligned} M &= \frac{V_C}{V_g}=\frac{1}{2}+\frac{1}{2}\sqrt{1+\frac{2D_1^2 R}{Lf_s}} \\ \bar{I}_L &= \frac{D_1^2 V_g M}{2Lf_s(M-1)} \end{aligned} \tag{60}$$

It can be verified that this equations represent the same DC operating point as that predicted by the conventional reduced-order model [11] as well as by the previous full-order model [14, 69].

Small-Signal Linear Model

Using standard linearization techniques, a small-signal model can be derived from (59) as follows:

$$\frac{d}{dt}\begin{bmatrix}\hat{i}_L\\ \hat{v}_C\end{bmatrix}=\mathbf{A}\begin{bmatrix}\hat{i}_L\\ \hat{v}_C\end{bmatrix}+\mathbf{B}\begin{bmatrix}v_g\\ d_1\end{bmatrix} \tag{61}$$

Where

$$\mathbf{A}=\begin{bmatrix}\frac{2(1-M)}{D_1T_s} & -\frac{2M}{D_1RT_s}\\ \frac{1}{C} & -\frac{1}{RC}\end{bmatrix} \qquad \mathbf{B}=\begin{bmatrix}\frac{M^2}{L(M-1)} & \frac{2MV_g}{L}\\ -\frac{D_1^2T_s}{2LC} & -\frac{D_1T_sV_g}{LC}\end{bmatrix} \tag{62}$$

According to the needs, various transfer functions can be determined from this small signal model.

Model comparison and verification

The new full-order averaged models are compared with the reduced-order model [11] and the full-order averaged models presented in [14, 69]. The comparison is made at the small-signal level. Table II summarizes the poles and the zero in the control-to-output transfer function of the boost converter predicted by the three different models. The reduced-order model does not include the second pole or the right- half-plane (RHP) zero. There is also a significant difference between the second poles and the RHP zeros predicted by the new model and the previous full-order model.

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Table II

Comparison of pole and zero locations for the boost converter in DCM

Model	1st Pole s_{p1}	2nd Pole s_{p2}	RHP Zero s_z
Reduced Order	$\frac{2M-1}{M-1}\frac{1}{RC}$	none	none
Full Order	$\frac{2M-1}{M-1}\frac{1}{RC}$	$\frac{2(M-1)^2}{D_1^2 M^2 T_s}$	$\frac{2(M-1)}{D_1^2 M T_s}$
Revised Averaging	$\frac{2M-1}{M-1}\frac{1}{RC}$	$\frac{2(M-1)}{D_1 T_s}$	$\frac{2}{D_1 T_s}$

The converter was simulated with a detailed switching model using SABER. ESR of both the inductor and the capacitor are taken into account in the simulation in order to match the experimental set-up. The new averaged model gives the most accurate response compared to detailed simulation. The response is almost identical to that of the detailed switching model in the frequency range up to one third of the switching frequency. The improvement of the new model over previous models is significant, especially in the phase response. Simulated frequency responses above one third of the switching frequency were not studied. This is because the converter response is dependent on the phase of the disturbance, and this sensitivity cannot be captured with any average-based LTI model. The phase dependency becomes especially significant above about 1/3 of the switching frequency. The new model predicts almost exactly the same response as the experiments up to one third of the switching frequency, at which point the disturbance phase effect begins to be significant.

Understanding the dynamic behaviour of DCM operation

The numerical and experimental results clearly showed the improved accuracy of the new revised model over previous models. The results, however, do not explain why this model is more accurate. Some analytical results are provided in order to understand the dynamic behaviour of DCM operation in general.

It is important to point out that averaged modelling of PWM converters in DCM involves two steps at which approximations are introduced: the determination of the dependent duty ratio, and the averaging process. This is in contrast to the CCM case, in which only averaging is involved. It is possible to quantify the error introduced by averaging. In the DCM case, we would expect similar accuracy of the averaged model if we could find an “exact” expression for d_2. In other words, the unusually large discrepancies (compared to CCM case) exhibited by previous DCM models can largely be attributed to the use of inaccurate constraints that define d_2.

All models compared predict the same DC as well as low-frequency responses. The differences and discrepancies exist only at high frequencies. Since the inductor current in DCM resets to zero (or a constant) in every switching cycle, the energy flow in the inductor is independent from cycle to cycle, i.e., the inductor does not carry any information from cycle to cycle. From this standpoint, one could argue that the inductor current no longer acts as a state variable. However, within each switching cycle, the inductor current is still a dynamic variable and does contribute to the fast dynamics of the converter. Previous models

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failed to accurately capture these fast dynamics, hence are unable to predict converter responses at high frequencies.

The Fast Dynamics

To understand the origin of the fast dynamics associated to the inductor current, a small-signal disturbance in the d_1 duty cycle was introduced in the inductor current waveform. The effect of this perturbation is to delay the leading edge of d_2. Based on the waveform, the shift of the trailing edge of the second interval and the peak of the perturbation can be calculated. Afterwards, taking the Laplace transform of the inductor current shifted equation, the transfer function from a perturbation in the duty cycle to the corresponding perturbation in inductor current is

$$\frac{\hat{I}_L(s)}{\hat{D}_1(s)}=\frac{V_{on}+V_{off}}{L}\left(\frac{1-e^{-D_2T_ss}}{s}\right) \tag{63}$$

where, V_{on} and V_{off} are the voltages across the inductor when the switch or the diode conducts the current respectively. Their reference directions are taken such that both are positive. Applying the Pade approximation of the exponential function to (63), it can be expanded as

$$\frac{\hat{I}_L(s)}{\hat{D}_1(s)}=\frac{V_{on}+V_{off}}{L}\left(\frac{D_2T_s}{1+\frac{D_2T_ss}{2}}\right) \tag{64}$$

It can be concluded from (64) that the effect of the fast dynamics associated with the inductor current in DCM is to introduce a high-frequency pole at $s_p=2/D_2T_s$. It can be verified that this is the same high-frequency pole predicted by the new revised full-order model for the three basic converter structures.

In summary, PWM converters operating in DCM exhibit fast dynamics due to the transient behaviour of the inductor current within a switching cycle. The constraint defining d_2 is the key to the accurate prediction of these fast dynamics with averaged models. The constraint (58), proposed by the authors of the paper discussed, results in accurate averaged models because it correctly captures the fast dynamics associated with the inductor current. All averaged models have limited utility above about one third of the switching frequency, since the response above that value depends on the specific timing of the disturbance and is not captured with a conventional frequency-domain model.

In the paper, the revised averaging approach is used only for the calculation of the models for the three basic structures operating in DICM. The analysis of the high order structures working in another conduction mode, like DVCM, DQRM, MDM's or others (see 1.3), is a topic that the authors left for a future work.

The methodology followed by this revised averaging approach, was utilized in [78] to derive the peak-current-mode control (PCMC) models in DICM for a buck-type converter. The author verifies that the models developed using this revised averaging methodology are much more approximate and correct than the developed using [51].

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1.4.3.3 LATER DEVELOPMENTS

Unified Average Modelling of Direct-On-Time Control

In [79, 80] it was presented a consistent formalism to model a direct-on-time (DOT) controlled converter, which is applicable to fixed and variable-frequency operations in DCM and CCM at open loop conditions. The resulting fixed-frequency models are naturally the same as presented earlier for CCM [19] and DCM [12]. The main difference is the formalism to obtain the models that allows the inclusion of parasitic elements in the models, which has not been considered earlier in DCM, because it was stated that their effect is minimal, but their effects had not been studied before. This paper was shown that the effect of parasitic elements is minimal as is usually assumed, e.g., in [12], and difficult to assess using frequency response measurements. Therefore, it may be well justified to use a simpler formulation for assessing the dynamics of the converters in DCM.

One of the fundamental issues that were taken into account in the calculation of this modelling method is the time-varying local average value of the inductor current as a state variable that is continuous within a cycle regardless of conduction mode. Its charge contents within ON and OFF times are, however, dependent on the mode of operation. In addition, the derivatives of the state variables may be estimated accurately based on the basic electrical concepts of the associated circuit elements, i.e., the average slope of the inductor current and the average change of charge in a capacitor. The duty ratio constraint is developed in this method using the same equation as in [12]. Using the resulting nonlinear state-space equations and according with the assumptions already cited, it may be obtained the small-signal models by applying partial derivatives. These models are the representation known as G-parameter model, which may be represented also as a circuit theoretical two-port model consisting of Norton's equivalent circuit as an input port and Thevenin's equivalent circuit as an output port.

Additionally, the technique known as "unterminated modelling" is introduced, facilitating the assessing of the effect of different types of loads on converter dynamics, because the load of a converter is very seldom resistors as are usually assumed in typical power electronics textbooks, but composed of a combination of different loads and/or other converters. In this technique, the state-space representation, and consequently, the transfer functions are first derived without the effect of the load. The load effect may be later added using special reflection rules. This kind of formulation actually simplifies the state-space representation, removing terms related to the load resistor (i.e., $R\rightarrow\infty$) compared to the terminated representations. Moreover, the technique does not restrict the form of the load impedance. The program packages such as Matlab (Math Works Inc.) might be used for the analysis of this kind of combined transfer functions. The extra-element theorem [3], developed by Middlebrook, might be equally used to obtain the formalism facilitating the load-effect analysis. The state-space representation for the "unterminated" representation may be obtained from the standard representations by letting the load resistor $R\rightarrow\infty$ and taking the limiting representation as an "unterminated" representation. When the "unterminated" state space is linearized applying partial derivatives and solved in the frequency domain, we get the "unterminated" G-parameters of the corresponding dynamical system. The effect of load on the output dynamics may be assessed by computing the perturbed output voltage at the presence of the external load. The effect of the load on the input dynamics may be taken into account by first computing the perturbed output current at the presence of the external load and then replacing it at the input port with its new formula, giving the terminated transfer functions as a function of the “unterminated” transfer functions and the load.

Bond Graph

A unified graphical method of modelling PWM DC-to-DC converters using bond graphs is presented in [81]. The concept of switched power junctions is used as a model for switching phenomenon in the converters. There is one-to-one correspondence between the physical system and bond graph elements. This model visually indicates the cause and effect relationships between energy variables, which enhance the visual understanding of the system. The bond graph unifies the method of obtaining the large signal, steady-state and small-signal model for switched mode power converter through the logical process of graphical reduction. Furthermore, the bond graph can handle multi-domain systems without sacrificing the ease of deriving the state space representation of physical systems by inspection. Switching converters in CCM and DCM can be modelled by bond graph. However, the use of this method implies some familiarity with the converter operation. The bond graph method displays all the physically achievable switching states in a single graph. Furthermore, the bond graph of the converter explicitly displays the structure of the dynamic equations of the converter.

Complementarity Formalism

In [82] the authors model DC-to-DC power converters using the complementarity formalism. For each position of the switches, in this approach the dynamics are given by a linear complementarity system which incorporates, in a natural way, the description of generalized discontinuous conduction modes (GDCM), characterized by a reduction of the dimension of the effective dynamics. Linear complementarity systems are obtained as follows. Take a standard linear system, select a number of input/output pairs and impose for each of these pairs that at each time both of them must be nonnegative, and at least one of them should be zero (non-negativity + orthogonality). These are called the “complementarity conditions” (CC), and the pairs are called “complementary variables.” Complementarity conditions are well known in mathematical programming, although they are not usually in combination with differential equations. In the context of electrical circuits, imposing complementarity conditions simply means that some ports are terminated by ideal diodes, with the diode current and the negative of the diode voltage as complementary variables. Associated to each complementary pair there are two general situations allowed by the CC: one is when the variable is equal to zero and the other when the variable is greater than zero and vice versa. In electrical engineering terminology, diodes may be blocking or conducting. Afterwards, some aspects of the dynamics of the simplest power converters for a given switch configuration can be analyzed by taking into account only the changes associated to the diodes.

If a complementary variable is nonzero, the complementarity condition forces its conjugate to remain equal to zero for a while, and hence one or more state variables (or combination of them) may be kept to a constant value for a time. If the variable is a current, this situation is known as a “discontinuous conduction mode” (DCM) in the power converter literature. Since this can happen to a wider class of variables, other than currents, this

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situation can be called "generalized DCM" (GDCM). The GDCM lasts until a switch state change takes place, or until the companion complementary variable returns to zero due to the dynamics of the other state variables. DCM has been extensively studied in the literature in connection with control algorithms, i.e., switching policies, such as PWM, where averaged methods or small-signal frequency domain descriptions are generally used, or in connection to bifurcation theory and chaos. Instead, the aim of the paper is to obtain, for a given switch position, an exact state-space condition which indicates the appearance of a GDCM.

The basic power converters can be formulated as linear complementarity system, with the positivity condition relaxed. A simple analytical test to look for GDCM in power converters with a single diode was presented. This test can be verified at several orders; the higher the order, the smoother the change in one variable. The test can be applied to the CUK converter, and the conditions under which GDCM can appear.

1.4.4 SIMULATION OF SWITCHED AND AVERAGED DYNAMIC MODELS

In the design verification of power electronic systems by simulation, it is often necessary to use component and system models of various complexity levels. Detailed, complex models that attempt to accurately represent the physical behaviour of devices are necessary for tasks that involve finding switching times, details of switching transitions and switching loss mechanisms, or instantaneous voltage and current stresses. Component vendors often provide libraries of such device models for use with general-purpose circuit simulators such as SPICE or SABER. Because of the complexity of detailed device models and the fine time resolution, the simulation tasks can be very time consuming. In practice, time-domain simulations using detailed device models are usually performed only on selected parts of the system, and over short time intervals involving a few switching cycles.

Since an ON–OFF switching transition usually takes only a small fraction of a switching cycle, the basic operation of switching power converters can be explained using simplified, idealized device models. Such simplified models yield physical insight into the basic operation of switching power converters, and provide the starting point for the development of the analytical models described earlier. Simplified device models are also useful for time-domain simulations aimed at determining or verifying converter and controller operation, switching ripples, current and voltage stresses, responses to load or input transients, and small-signal frequency-response characteristics. With simple device models, and ignoring details of switching transitions, simulations over many switching cycles can be completed efficiently, using general-purpose circuit simulators or specialized simulators.

Simulations of averaged circuit models can be performed to test for losses (apart from those due to switching) and efficiency, steady-state voltages and currents, stability, dynamic and large-signal transient responses. Since switching transitions and ripples are removed by averaging, simulations over long time intervals and over many sets of parameter values can be completed efficiently. Therefore, averaged models are also well suited for simulations of large electronic systems that include multiple switching converters. Furthermore, although large-signal averaged models are nonlinear, they are time-invariant and can be linearized about any constant operating condition to produce LTI small-signal models, from which one can generate various frequency responses of interest [32, 33, 35, 72].

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1.4.4.1 TRANSIENT RESPONSE ANALYSIS

In the design of control loops in connection with converters, it is often necessary to perform transient simulations over many switching cycles. Transient simulations can be used to determine current harmonic distortion, component stresses during start-up or load transients, and so on. Such simulations can be performed on a switching circuit model using a switched-circuit simulator or a general-purpose simulator, or on the converter averaged model, or using a sampled-data model.

1.4.4.2 STEADY-STATE AND SMALL-SIGNAL ANALYSIS

There are many numerical and simulation approaches to determine the steady state of a switched model. Small-signal models, and particularly sampled-data small-signal models, can now be constructed to represent small deviations from this steady state [83, 84].

A designer is also often interested in determining the boundaries in the space of parameters (such as input voltage amplitude, frequency, load resistance or current, and so on) that mark transitions from one steady-state operating mode to another in a switching circuit. Of complementary interest is the determination of stability domains in the state space for particular operating modes, i.e., the sets of initial conditions that respectively converge to these operating modes.

Both steady-state computations and the construction of small-signal models are easily carried out with averaged circuits, because circuit averaging leads to a nonlinear, time-invariant circuit model. Linearized averaged models are also the starting point for the modelling and stability analysis of paralleled converters.

Frequency responses of interest can alternatively be obtained by appropriate time-domain simulations of switching circuit models or by AC simulations of nonlinear averaged circuit models.

1.4.4.3 USE OF SIMULATORS IN CIRCUIT GENERATION

Switched-circuit and averaged simulators have also proven to be very valuable in the synthesis of new power electronic circuits. Generally, there are large numbers of possible combinations of switches and passive elements that can be combined to create new circuit topologies. Simulation of these topologies remains a key tool in comparing topologies for an application, discovering problems in a new circuit or control approach, trying out variations to overcome each successively discovered hurdle, and then refining the circuit or controller to meet performance requirements. The ability in a simulator to build models of increasing complexity, starting from very idealized models, provides a strong tool for the power electronics design engineer exploring a new design concept, in essence by using the computer tool to help understand how a new circuit works (or does not work). The development of approaches to rapidly determining the cyclic steady-state sequence of a switching circuit has meant that long simulations to reach steady state are avoided, leading to significant increases in design engineer productivity [2].

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1.5 CHAPTER CONCLUSIONS

This chapter has been a bibliographic journey through the important aspects of the DC-to-DC switched mode power conversion: circuit structures generation and its mathematical modelling. The elementary aspects of DC-to-DC switching converter explained in the first sections have been the starting point that helps to the understanding of the following sections.

The generation of new structures and its classification have been thoroughly explored taking into account different schemes and the interleaving was presented as a strategy of converter generation. That is actually a different approximation of the generation of new converter structures that improves the characteristics of the resulting circuit. This approximation begins from both basic converter structures and control techniques already known, and continues performing a new combination of all of them through the application of some basic rules of interconnection.

A refining method of this interconnection was the complementary interleaving, that consists in the application of 50 % phase shifted control signals to each canonical cell in a switching period. Consequently, the circuit switches are activated in a complementary way. This complementary interleaving is, indeed, the origin of many structures with very interesting characteristics that will be explored further in next chapters.

Furthermore, a deep study of some different possibilities of operating modes in DC-to-DC switching converters was useful as an introduction for the modelling methods explained, and for the presentation of the conduction modes of operation of the new structures that will be shown in the next chapters.

The most important part of this state of the art has been the extensive review of all the modelling methods applied to DC-to-DC PWM converters operating in CCM and DCM modes. The objective of this study has been to place the main subject of this thesis (modelling methods) inside its bibliographic background.

This review began with the modelling methods applied to converters working in CCM. The first is the switched state-space model method. Second, the State Space Averaged (SSA) that is the most used modelling method. It can be said that the popularity of the SSA modelling method is due largely to its clear justification, simple methodology, and demonstrated practical utility. Afterwards, the injected-absorbed current modelling method was presented as one option to the SSA, and works directly with the transfer functions. Moreover, some circuital approaches, like the circuit averaging and the averaged switch methods were also presented in this state-of-the-art. Another technique that offers refinements to the theory of state-space averaging, permitting a framework for the analysis and design when small ripple conditions do not hold, was the generalized, averaging and dynamic phasors. And finally, the sampled-data models that are naturally matched to power electronic converters because of the cyclic way in which power converters are operated and controlled.

The modelling methods applied to the converters operating in DCM are most of the times a specialization of the CCM methods. This means that almost all the methods studied for

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CCM have an extension for their use in DCM converters, excepting the generalized multi-frequency averaging.

Some of these extensions obtain reduced-order models, where the inductor current does not appear as a state variable. This model can correctly predict the behaviour of a converter in the low-frequency range. However, large discrepancies appear at frequencies above about one-tenth of the switching frequency, particularly in the phase response. The SSA method that was so useful in CCM, obtains a reduced order model when the converter is working in DCM, due to an inconsistent use of variables that was explained.

Due to the special characteristics of the DCM, the modelling methods that permit to obtain a full-order averaged model have exhibited better approximations to the real responses of the converters than the reduced order model approaches.

The full order average approaches make some improvements using different simulation and analysis tools. This is the case of the equivalent duty ratio method, average-switch models, sampled data models, current injected approach and loss-free resistor model.

Finally in this modelling matter, it was presented the revised averaging approach where, through the study of various issues involved in DCM modelling, it develops a physically-based modelling procedure for PWM converters. The modelling method consisted basically of three steps: averaging, correction, and a new definition of one duty-ratio constraint. The results clearly showed the improved accuracy of the new revised model over previous models because it takes into account the fast dynamics associated to the transient behaviour of the inductor current within a switching cycle.

The final review of the latest developments in modelling shows that no major advances have been made lately.

Some brief comments about the simulation of switched and averaged dynamic models have been included because this is a very important step in the processes of analysis and design of new DC-to-DC power converters.

The detailed study of the great variety of DC-to-DC switching converter modelling methods has demonstrated that this area is still in continuous evolution and developments due to the new needs and the advancements in the available tools. For example the simulation tools, that have had a large developed from its beginnings. Those tools have provided some useful results in the initial simulation applied in many modelling methods.

This initial simulation of a new circuit structure permits the checking of its output waveforms in order to verify if the obtained results are useful, that is, are the desired results, and is largely employed in the explained modelling methods. Those methods have used the simulated waveforms of some circuital variables in order to obtain some relationships between variables that are useful in the model calculation specifically if the converter circuit is working in DCM mode.

Another important conclusion is the fact that there is not an approach for the analysis of the high order structures working in other DCM modes like DVCM, DQRM and MDMs, because all the approaches have been applied to the three basic structures operating in DICM.

In the next chapters the matter of study will be a new high order structure operating in one special case of DCM mode and the modelling method developed for its analysis and controllers design.

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CHAPTER 2

ASYMMETRICAL INTERLEAVED DC TO DC SWITCHING CONVERTERS CIRCUITS: GENERATION

As was outlined in Chapter One, up to now new converter structures have been obtained by changing the original structures after their general topological properties have been studied. These studies enable a completely formalized synthesis procedure to be devised that is based on a set of synthesis rules which refine the process. When new structures are generated, the addition of isolation to the basic converters is also considered.

This chapter will present a different approach to generating converters that consists of using known control techniques in combination with known circuital structures to generate new structures with novel features. This idea was also briefly described in Chapter One. The following paragraphs will set out the topics studied in each section of this chapter.

The first section will review the basic concepts and the benefits of the control technique to be used: the interleaving [1]. The second section will describe the specialization of this control technique, that is, the complementary interleaving, that was used in previous works [2] and that will be used in the development of structures of this chapter.

The third section takes as its starting point the final circuit of the last section and will show how the concept of structure modification can be used in order to obtain a new circuit with a good performance.

The new converter will be studied in the fourth section by using simulations and initial calculations of its steady state operating point.

In the fifth section, two additional converter families were obtained by applying the same structure modification methodology that was used for the first new converter. This section also includes simulations results and initial mathematical calculations.

The sixth section presents the experimental results of the first circuit converter in the time domain.

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2.1 THE BASIC INTERLEAVING CONCEPT

As explained in Chapter One, interleaved power conversion refers to the strategic interconnection of multiple switching cells that are operating synchronously but that are also shifted in phase. This arrangement reduces the net ripple amplitude through harmonic cancellation and raises the effective ripple frequency of the overall converter without increasing switching losses or device stresses. An interleaved system can therefore realize savings in ripple filtration and energy storage requirements, resulting in greatly improved power conversion densities without sacrificing conversion efficiency.

The benefits of interleaving can be understood intuitively by comparing the interleaved and non-interleaved performance of a converter system. For example, let us consider a particular case of two boost switching cells connected in parallel. For simultaneous synchronous operation (wherein the turn-on and turn-off commands of the two controlled switches are identical), the total inductor current, being the sum of two identical currents, has a peak-to-peak amplitude equal to twice that of a single inductor current (Figure 2.1a). For interleaved operation, the commutation instants of the second switch are delayed in relation to those of the first switch by half of a switching period. While the peak to peak amplitude of the individual inductor current remains unchanged, the net peak to peak amplitude of the composite input ripple waveform is smaller than it is for the non-interleaved case (Figure 2.1b).

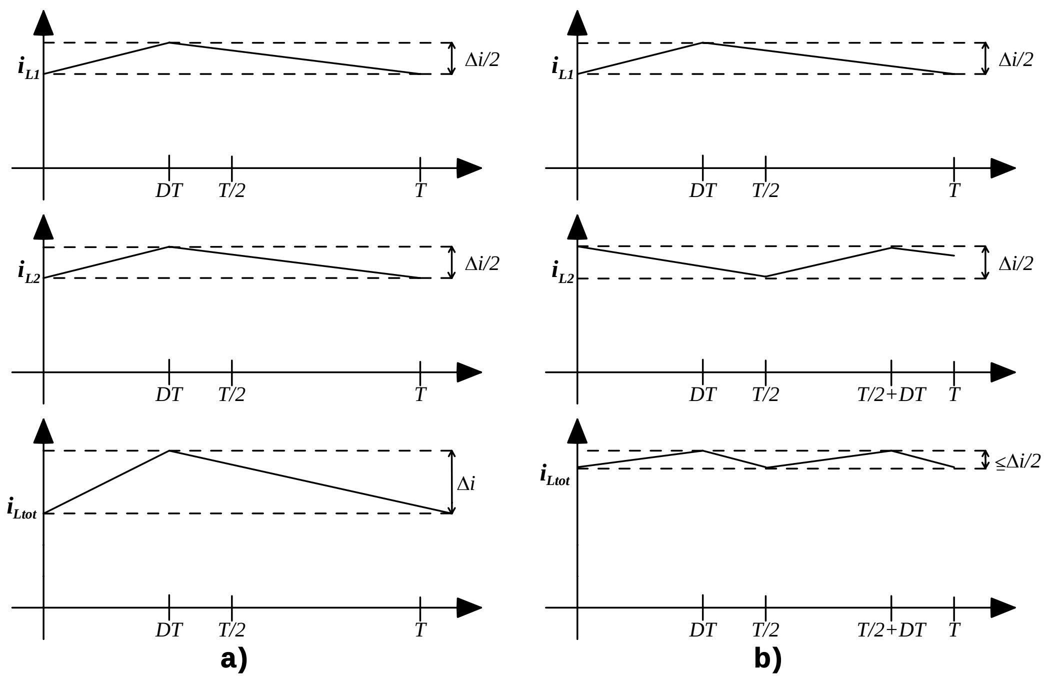

Figure 2.1: Input current ripple waveforms for the parallel of two boost converters: a) Non-interleaved case, b) Interleaved case

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The composite amplitude in the interleaved case is always less than or equal to the contribution from a single switching cell, yielding a reduction factor of two or more in worst case ripple amplitude compared with the non-interleaved case. In fact, under certain conditions (e.g. two cells each operating at a $50\,\%$ duty cycle) the composite ripple in the interleaved case is reduced to zero. It is important to note that this reduction was achieved without increasing either the switching losses or the energy storage of the system.

In addition to producing this ripple amplitude reduction, interleaving increases the ripple frequency of the waveform in the input of the filter components which are common to both switching cells branches. This ripple frequency increment (by a factor of two) results in further savings in filtration for a given ripple amplitude.

Because ripple amplitude is tied to other converter characteristics, interleaving can also be used to increase conversion efficiency and/or power conversion density. This is important in cases where the ripple may already be so small that further reductions are of limited benefit.

Let us consider again the previous dual-cell comparison example, in which the total inductor energy storage and the switching frequency were both held constant, resulting in a substantial reduction in ripple. We might instead choose to reduce the switching frequency of the interleaved system (Figure 2.1b) by a factor of two in order to reduce the switching losses. In addition, the inductance per cell might be reduced by a factor of two to reduce the converter size.

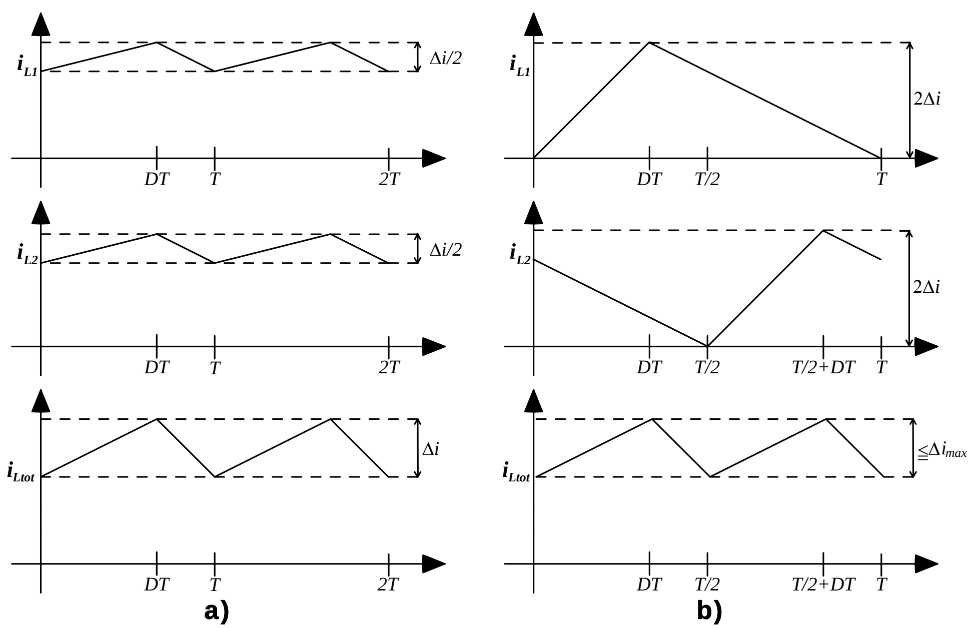

Figure 2.2: Input current ripple waveforms for the parallel of two boost converters: a) Non-interleaved case, b) Adjusted parameters interleaved case

The input current ripple of the “non-interleaved” converters and the “adjusted-parameters interleaved” converter are shown in Figure 2.2. It can be seen that under constant output voltage conditions, the worst case peak-to-peak amplitudes of the net input

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currents are equal. Nevertheless, without interleaving, the ripple of the “adjusted-parameters” converter could be four times larger than the ripple of the original “non-interleaved” converter. In this way, interleaving can be used to improve conversion efficiency and power density. In general, it serves as a technique for getting higher performance from a given set of technologies.

With reference to the reduction of stress in the components, in the interleaved case, each switching cell handles only a fraction of the total peak power, and the peak device stresses are reduced accordingly. This reduction combined with the reduction in ripple filtration requirements was one of the main motivating factors behind the first known use of true interleaving in switch mode power conversion.

One of the drawbacks of the interleaving technique that is sometimes mentioned is the duplicity of the elements; however, in some cases this duplicity is imposed even in the non-interleaved cases. Examples of this are the MOSFET or diodes in parallel due to the high levels of mean currents, the partition of the inductors, the multi-core inductors, etc.

Interleaving techniques can be applied to various converter topologies and the general usefulness of interleaving is one of its major attractions; virtually any present system design can benefit from the incorporation of interleaving techniques. Unfortunately, development and practical application of the interleaving concept have been limited by the complexity of multi-cell converter analysis. [1]

2.2 THE PREVIOUS WORKS

The next paragraphs briefly described the results, that were presented in [2], of the complementary interleaving technique’s application into the generation of new converter circuits.

2.2.1 COMPLEMENTARY INTERLEAVING

The interleaved interconnection of two switching cells requires the internal switching instants of the two cells to be sequentially phased over equal fractions of a switching period. Generally, these fractions are equal to half of the switching interval, that is, the OFF-ON step of one cell occurs when the other cell is in the middle of its ON time. With this arrangement of switching times, an interleaved circuit with two canonical cells in parallel can present four different configurations in CCM. From the point of view of the ripples, only two configurations are optimal: when one switch is ON at the same time that the other switch is OFF. In these optimal configurations, the inductor of one cell is charging while the other is discharging and the inductor current waveforms of the two converters have slopes with opposite signs; for this reason their sum, that is, the slope of the total interleaved input current, can be the minimum, as can its ripple. A similar analysis can be made for the output voltage ripple.

Consequently, if the aim is to obtain low input and output ripples for the interleaved interconnection of two converter cells, then the duty cycles of the two converters have to be different, in other words, the interleaved circuit has to be controlled in order to turn on the switches in a complementary way. Therefore, the circuit will only exhibit two of the four

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configurations and the other two configurations with the switches in the same state and with high ripples will not appear.[2]

Another advantage that complementary interleaving has over other kinds of interleaving is the simplicity of control, because one activation signal is the opposite of the other activation signal.

2.2.2 INITIAL CIRCUIT: IDB

The application of the complementary interleaving technique to the parallel of two boost converters was studied in Chapter Two of [2]. The circuit was named IDB (Interleaved Dual Boost) and can be seen in Figure 2.3. In an open loop, every boost converter works as a voltage source, and due to the difficulties of paralleling two voltage sources, the circuit is highly dependent on the parasitics. If the two voltage sources are equal, then this sensibility can disappear. This condition is satisfied for a steady state duty cycle of *50 %*, where the circuit is a doubler. Consequently, the usefulness of the circuit is restricted to a *50 %* duty cycle. Despite the problems described, the IDB has a low ripple in its global variables, input current and output voltage as do all interleaved circuits. To control this circuit, it is necessary to establish one condition that forces the IDB to operate in a *50 %* duty cycle. The deciding condition was the equality of the currents' mean values, which only happens in a *50 %* duty cycle. This characteristic makes it impossible to regulate the output voltage.

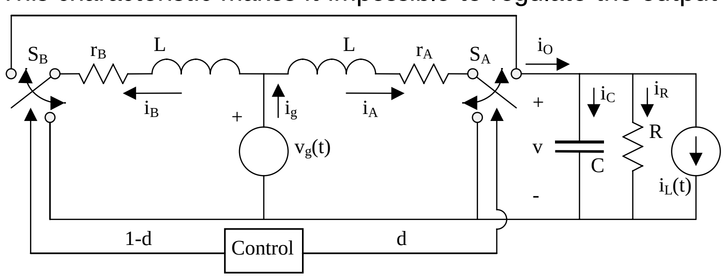

Figure 2.3: Interleaved dual boost (IDB) converter

2.2.3 MODIFICATIONS OF THE IDB CONVERTER

The constraints observed in this converter were the main reason why other forms of applying complementary interleaving were tested. Chapter Five of [2] deals with this matter and studies some modifications to the structure of the IDB in order to improve its characteristics.

The first option explored was to use coupled inductors in order to prevent difficulties in the fabrication of two equal inductors. This change increases the ripple and modifies the IDB circuit dynamics. The second option used unidirectional switches. The IDB circuit behaviour is the same in CCM, but in DCM there are some changes: the variables' ripple increases and the dynamic is modified. On the other hand, the mean value of the output voltage is increased.

Although it is possible to design the parameters of the circuit in order to control the overshoots on the dynamics of the start-up, there are other alternatives that may achieve similar effects, such as the inclusion of a nonlinear network in the circuit which partially helps to charge the output capacitor. Another possibility is the connection of the capacitor in floating form between the input and output. This last change, despite having serious difficulties, is the origin of the converter explained in the following section.

2.2.4 THE SWITCHED CAPACITOR INDUCTOR DUAL BOOST - SCIDB

The SCIDB [2] is the result of an alternative interconnection of the canonical cell capacitors that constitute the IDB circuit. As Figure 2.4 shows, the circuit can be interpreted as the combination of an IDB with one classical voltage multiplier net, that was built using diodes and capacitors. This multiplier net can be understood as a switched capacitor net and this in turn gave rise to the name of this converter: the Switched Capacitor Inductor Dual Boost (SCIDB).

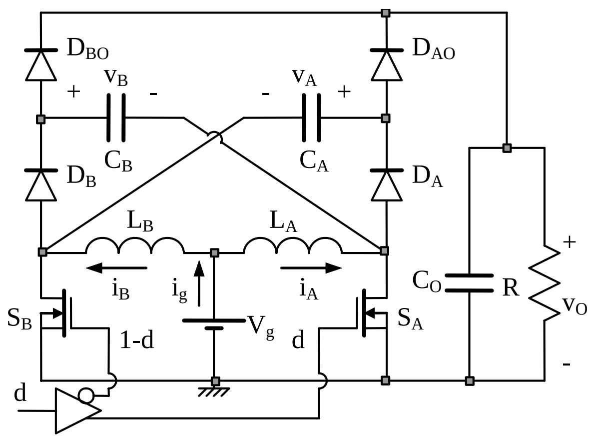

Figure 2.4: Schematic circuit diagram of the SCIDB converter

The interconnection of these two stages means that this SCIDB converter is a four order converter, where the switches are controlled in a complementary way. It exhibits a greater analytical complexity than the IDB, but its possibilities are also greater because this converter does not depend on parasitics in the same way that the IDB does.

The study of the conversion ratio in terms of the duty cycle shows some interesting results: the SCIDB converter always acts as a boost and the conversion ratio is symmetric in relation to a *50 %* duty cycle. The minimum value of the conversion ratio is four and occurs in a duty cycle of *50%*. When the duty cycle approaches to zero or one, the conversion ratio tends to infinity but, in practice, these values of duty cycle are hardly reachable for the circuit.

Thus, the SCIDB can operate as a boost converter in an large range of duty cycles, providing output voltages greater than four times the input voltage, and quadrupling voltage when $D=0{,}5$. However, the SCIDB converter has controllability problems with the

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aforementioned duty cycle resulting from the cancellation of the global variables in its small signal transfer functions.

The presence in the transfer functions of poles on the left-hand side, whose proximity to the imaginary axis depends on the system's losses, could complicate the SCIDB's control design because of the existence of zeros on the right-hand side in some of its transfer functions.

The complementary way of controlling the SCIDB switches allows the input current to be distributed to each loop of the circuit regardless of the control strategy, thus providing the means of controlling the output voltage. The control strategies calculated on the basis of the small signal transfer function expressions are discarded because of their complexity. The strategy considered in [2] was the sliding mode control.

The SCIDB experiments allowed the verification of the theoretical results and the simulations results of the dynamics and the average values of the variables. The main difference is the switching noise due to the nonlinearity of the switches. The switch peaks that appear in the output voltage make it difficult to measure the output voltage mean value and the efficiency, and necessitate the inclusion of an output filter in order to suppress them. The filter used is a capacitor in parallel with the load. From the beginning it was expected that this capacitor would be needed; however, because of the existence of a capacitor loop in the circuit structure, the filter was not included in the theoretical analysis. Figure 2.5 shows that, after increasing the value of the output capacitor, the ripple corresponding to the experiment with $3\ \mu F$ is sufficiently small. Thus, it can be concluded that further increases will not produce significant improvements. Consequently, this will be the final value for this capacitor. The other parameters have the following values: $L_A=L_B=1\ mH$, $C_A=C_B=1.6\ \mu F$, $V_g=12\ V$, $R_L=103.5\ \Omega$, and $D=50\ \%$.

After determining that one capacitor of $3\ uF$ satisfactorily reduces the ripple, some adjustments were made in order to obtain a better performing output voltage that was closer to the theoretical value.

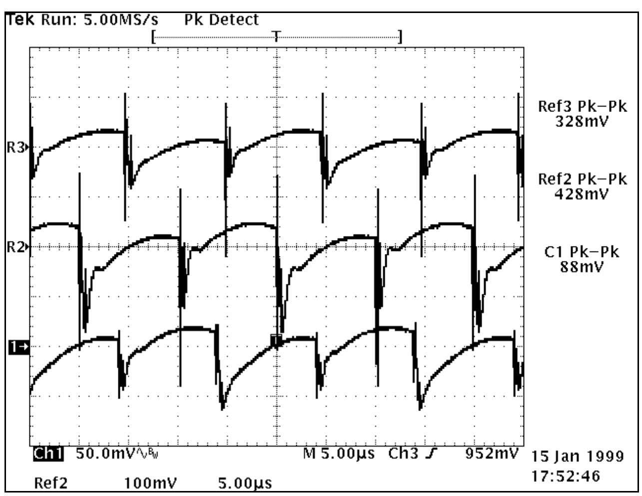

Figure 2.5: SCIDB converter output voltage ripple with different values of the output capacitor. Ref2: $C_O=1\ \mu F$. Ref3: $C_O=2\ \mu F$. C1: $C_O=3\ \mu F$ [2].

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Finally, some experiments showed that the dynamic response of the circuit is dampened less than the response without the output capacitor, but the steady state waveforms of the circuit are almost the same in both cases.

2.3 GENERATION OF THE ASYMMETRICAL INTERLEAVED DUAL BOOST AIDB

Given the interesting results obtained with the SCIDB, this section begins with an exploration of some topics featured in the future research section of [2]. The simulation results have been used in order to evaluate the performance of the new circuits. As mentioned in Chapter One, the simulations prior to the mathematical analysis have proven very valuable in the evaluation of new converter structures because they reveal any problems the circuit may have and allow variations to be tried out in order to resolve these problems, thus allowing us to understand how a new circuit works.

2.3.1 THE FIRST MODIFICATIONS INTRODUCED TO SCIDB

In order to improve the output voltage ripple, an output filter is included in the SCIDB circuit, and the basic cell can be seen as a boost with an output filter. This change increases the order of the system. The output voltage ripple of this circuit for $L_O=5\ \mu F$ can be seen in Figure 2.6. In the previous structure, the SCIDB, the two capacitors were interconnected in parallel for some values of the duty cycle thus causing current spikes in order to balance the SCIDB's voltages. Therefore, the output voltage ripple is improved by the presence of an inductor that smoothes the changes of the output current by decreasing its harmonic contents.

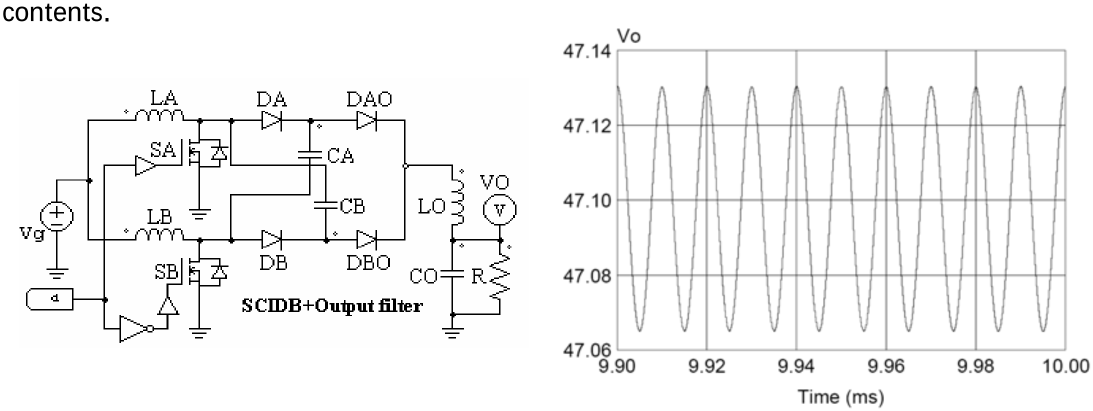

Figure 2.6: SCIDB converter with output filter and its output voltage simulated using PSIM

Another option is to increase the output filter order, changing the diodes D_{AO} and D_{BO} for two inductors. As with the SCIDB, the new structure with an output filter behaves symmetrically regarding the $50\,\%$ duty cycle. Also, the diodes D_A and D_B operate in discontinuous conduction mode (DCM) except in a narrow margin around $50\,\%$ duty cycle,

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which reduces the converter’s regulation capabilities by half. The name of this structure is the SCIDOFB (Switched Capacitor Interleaved Dual Output-Filtered Boost). The output voltage ripple of this circuit can be seen in Figure 2.7.

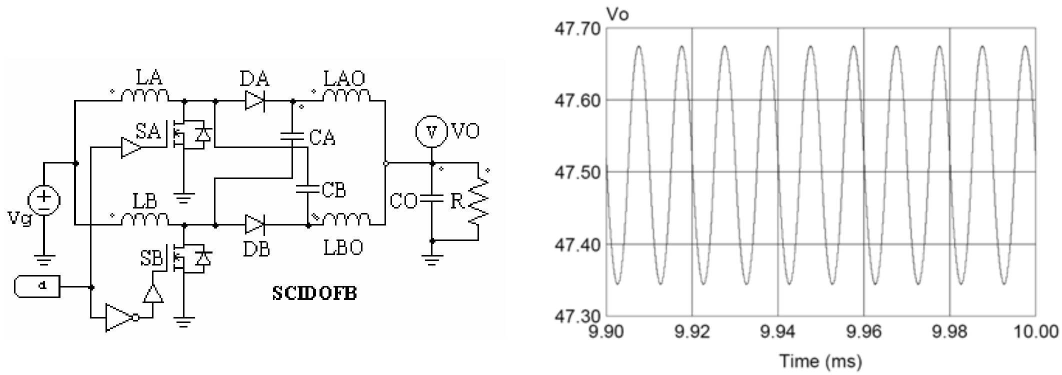

Figure 2.7: SCIDBOFB converter and its output voltage simulated using PSIM

Figure 2.8 shows how in the ASCIDOFB structure was broken the symmetry of the SCIDOFB structure in order to extend the converter's margin of output voltage (Asymmetric SCIDOFB). Figure 2.8 also shows the output voltage ripple of the circuit.

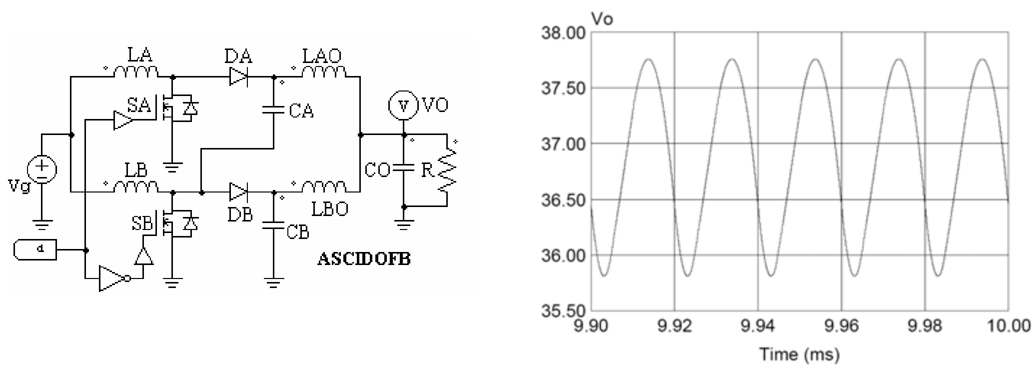

Figure 2.8: Asymmetric SCIDBOF converter and its output voltage simulated using PSIM

These simulations show some important differences compared with the results for the SCIDBOF before breaking the symmetry. The first difference is the mean value of the output voltage; which is smaller in the asymmetric SCIDBOF than in the symmetric SCIDBOF. The second difference is that the frequency of the output voltage signal is also smaller. Figure 2.9 shows the asymmetric currents of the asymmetric SCIDBOF. Because of the lack of symmetry, one of the output inductor currents, I_{LAO}, is larger that the other current, I_{LBO}. Thus, the frequency and the mean value of the output voltage are mainly due to the bigger current whereas the smaller current has little influence on the output voltage.

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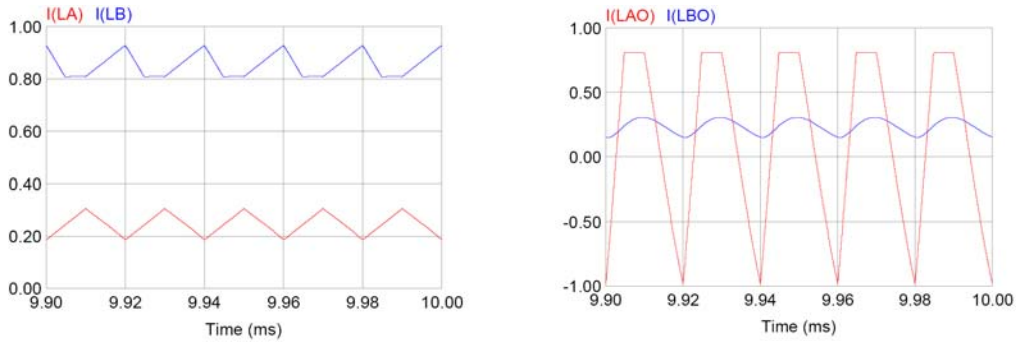

Figure 2.9: Inductor currents of the asymmetric SCIDBOF converter simulated by PSIM

2.3.2 THE AIDB

The methodology followed up to now has allowed the improvement of certain circuit characteristics such as ripples and duty cycle margins. In this section, we make further modifications to the structure of the circuit according to the results obtained in the simulations in order to extend the duty cycle margins of operation. From the simulation waveforms it can be observed that the average values of the currents flowing through the branch of the inductor L_{BO} and the capacitor C_B are very small in DCM (Figure 2.9). In other words, the effect of this filter is not so important and it can therefore be eliminated [3].

The new converter obtained is shown in Figure 2.10 and has been named the asymmetrical interleaved dual boost (AIDB). In the figure, the name of capacitor C_A has been changed to C_{AB}. The AIDB converter can be understood as a parallel interconnection between a boost with an output filter (branch A) and a boost simple cell (branch B) in which the first capacitor of the A-branch output filter is connected to the intermediate node of the boost of the B-branch, as are capacitors C_A and C_B in the SCIDB converter. This method follows the philosophy of switching capacitors. The MOSFETs of branches A and B are activated in a complementary way.

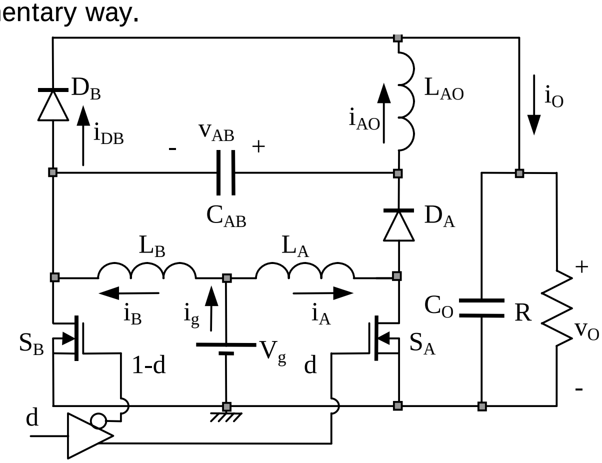

Figure 2.10: Schematic circuit diagram of the AIDB Converter

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The following section studies the simulation results obtained by PSIM for this new topology and will analyze its characteristics and advantages. The theoretical analysis and modelling of the AIDB converter will be studied in the next chapter

2.4 AIDB OPEN LOOP SIMULATION RESULTS

The simulations were done using the PSIM which allowed the converter to be modelled with ideal elements. Initially, the parameters of the converter were taken from previous research into the SCIDB [2]. After some preliminary simulations, the values of the capacitors and inductors are readjusted. On one hand, the inductor values guarantee that the current ripples are easily observed and sufficiently small in relation to their mean value (ripple $\leq 0{,}1\ A$). On the other hand, the capacitor values establish an output voltage ripple of less than $20\ mV$ and a voltage ripple in capacitor C_{AB} of $3\ \%$, meaning that the voltages are almost constant. All of these characteristics are calculated for a steady state duty cycle of $50\ \%$.

Therefore, the selected values for the parameters are: $V_g=10\ V$, $L_A=L_B=L_{AO}=1\ mH$, $C_{AB}=50\ \mu F$, $C_O=20\ \mu F$, $R_L=10\ \Omega$, $T=20\ \mu s$, and the duty cycle is from $10\ \%$ to $90\ \%$ with steps of $10\ \%$.

2.4.1 ANALYSIS OF THE RESULTS: WAVEFORMS AND TABLES

The waveforms of the steady state circuit variables were obtained for a duty cycle of $50\ \%$ in order to illustrate that the CCM and DCM modes of operation occur in the AIDB converter at the same time, but in different switches. Figure 2.11 shows the waveforms of the AIDB converter input currents.

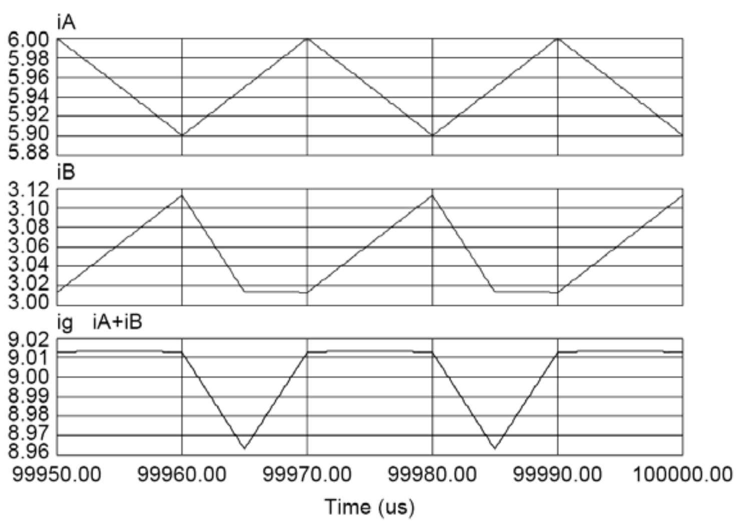

Figure 2.11: AIDB Converter input currents simulated using PSIM

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The waveform of the current i_A, in the inductor L_A, is at the top of the figure. It is triangular with a ripple of $100\ mA$ over a mean value of $5.95\ A$. Its shape shows two slopes of opposite signs resulting from the two operation intervals of the CCM mode in the associated switches S_A-D_A.

The waveform in the middle is the current i_B in the inductor L_B. It has three operation intervals that show the existence of the DCM mode in the other pair of circuit switches S_B-D_B. Its mean value is $3.05\ A$ and the ripple is $100\ mA$.

The last waveform is the input current i_g. This was directly measured and calculated by the sum of i_A and i_B. The mean value of i_g is $9\ A$ with a ripple of $50.37\ mA$; therefore, the ripple is $0.56\ \%$ of the mean value. At this point it is important to highlight that the input current ripple is very small in comparison with its mean value. This current has also three well differentiated operation intervals such as i_B. Two of these are rectilinear with slopes of opposite signs, while the third interval has a slope near to zero. In the interval that begins at the left from $99.95\ ms$, it can be observed that the waveforms of i_A and i_B have almost opposing slopes. For this reason, the waveform of i_g, which is the result of adding the two other currents, has a slope almost equal to zero in the same interval (despite some second order effects that can be observed). This is the conduction interval of the switches D_A and S_B.

In the next interval, the switches D_B and S_A are in conduction. The slopes of i_A and i_B have opposing signs, although the i_B slope is greater. Adding these slopes results in a negative slope interval until the zero slope of the i_B current. Finally, in the third interval, only S_A is in conduction and i_g has a positive slope due to the positive slope of i_A whereas the slope of i_B is zero.

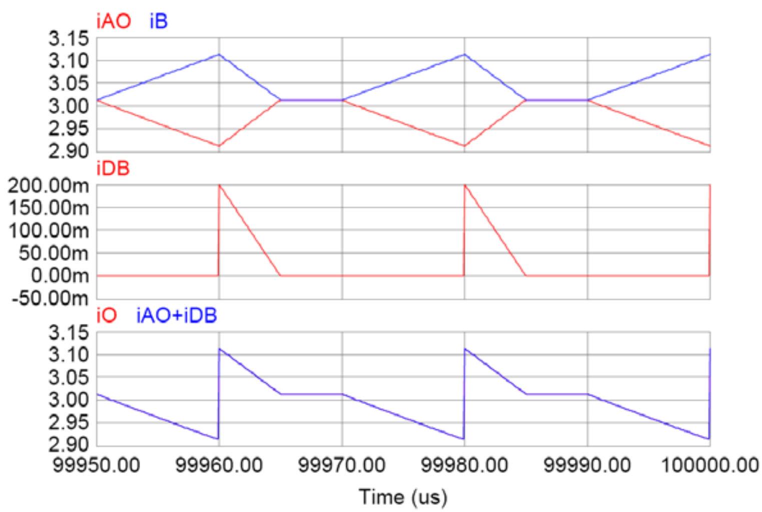

Figure 2.12: AIDB converter output currents simulated using PSIM

Figure 2.12 shows the AIDB output currents and one of the input currents in the top plot. Comparing the first and second plots, it can be seen that the i_{DB} current is equal to zero when the i_{AO} and i_B have the same value. From this point these two currents keep the same value until the next commutation of S_A and S_B, which turns off and on simultaneously. The

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i_{AO} and i_B have slopes of opposite signs until the diode D_B begins to conduct again. Afterwards, their slopes change simultaneously in order to reach the same zero value again. The mean value of i_{AO} is $2.96\ A$ with a ripple of $100\ mA$.

The triangular pulses, rather than the trapezoidal pulses, of the i_{DB} current waveform in the middle plot also confirm that the diode D_B is actually in DCM. Its mean value is $25.47\ mA$ and the ripple is $200\ mA$.

The existence of three intervals is due to the discontinuous conduction of the D_B diode as was also confirmed by the currents waveforms of the other plots. The presence of a third interval with an almost zero slope on the currents affected by the discontinuity is characteristic of the DCM mode [4, 5].

The waveform at the bottom plot was directly measured in the PSIM and was also obtained by the sum of i_{AO} and i_{DB}. This waveform is the current that flows to the output capacitor and the load and is responsible for the output voltage ripple. It also has three intervals, one of them with a zero slope and the other two with negative slopes that are separated by a positive discontinuity. This waveform shows that the current through the diode D_B affects the current that flows toward the circuit output (i_O) by influencing the output voltage and its ripple. As can be seen, the i_{AO} current shows a strong change in the shape of its ripple when it is added with i_{DB}. The area of the flat interval (DCM) of the output current that is under the constant value is bigger than the area that is over the constant value. For this reason, the mean value of the current is slightly smaller than the level of the flat interval. The mean value of this output current is $3\ A$ with a ripple of $199\ mA$, therefore the ripple is $6.6\ \%$ of the mean value. At this point it is important to emphasize that the output current ripple is also very small in comparison with its mean value.

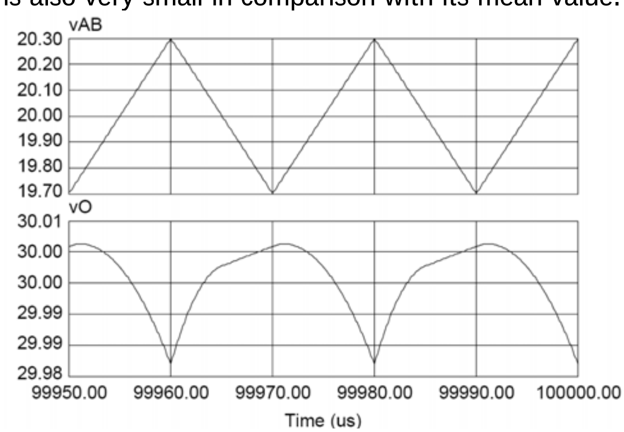

Figure 2.13: AIDB converter voltages simulated using PSIM

The waveform of the capacitor C_{AB} at the top of Figure 2.13 is triangular with only two intervals. The discontinuous conduction of D_B does not affect the V_{AB} voltage. This voltage is similar to the intermediate capacitor voltage in a boost converter with an output filter.

The ripple of the output voltage at the bottom of Figure 2.13 has two parabolic concave sections between the two consecutive minimums with a positive sloping rectilinear sub-interval in the middle. This is due to the form of the output current that has already been described, that is, the difference between its areas and to the flat sub-interval. The mean

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value of v_O is $30\ V$ with a ripple of $19.3\ mV$, therefore the ripple is very small in comparison with its mean value because is less than $0.1\ \%$. In this waveform it can be seen that the AIDB has a voltage step-up characteristic with an input-to-output voltage conversion ratio of three.

Table 2.1 shows the mean values and Table 2.2 shows the ripples in steady state for the following converter variables: the input current $I_g= I_A+I_B$; the inductor state variables are I_A I_B I_{AO}; the diode current is I_{DB}; the output current is $I_{AO}+I_{DB}$ and the capacitor state variables are V_{AB} and V_O. The data are obtained from the steady state waveforms in the [$99.5\ ms$ - $100\ ms$] interval when the converter starts up from zero initial conditions.

Table 2.1: Mean values of the AIDB variables in steady state

D	Ig	I_A	I_B	I_{AO}	I_{DB}	$I_{AO}+I_{DB}$	V_{AB}	V_O
0.1	99.94	1.0 mA	99.94	0.0 mA	9.99	9.99	89.92	99.92
0.2	25.00	5.3 mA	24.99	1.3 mA	5.00	5.00	39.98	49.98
0.3	11.11	15.7 mA	11.09	6.7 mA	3.32	3.33	23.32	33.32
0.4	7.11	4.37	2.74	2.62	42.5 mA	2.67	16.67	26.67
0.5	9.00	5.95	3.05	2.96	24.3 mA	3.00	20.00	30.00
0.6	12.25	8.72	3.53	3.49	12.3 mA	3.50	25.00	35.00
0.7	18.78	14.43	4.35	4.33	5.0 mA	4.33	33.33	43.33
0.8	36.00	29.99	6.01	6.00	1.3 mA	6.00	50.00	60.00
0.9	120.98	109.98	11.00	11.00	0.0 mA	11.00	99.98	109.98

(Excepting indications in the table, the currents are in A and the voltages in V)

Table 2.1 shows the mean values of the AIDB converter variables in steady state, and allows the detection of two zones of operation that are well differentiated within the converter, whose boundary is between $D=0.3$ and $D=0.4$. By refining the simulations, it was verified that the boundary is around $D=0.38$.

Table 2.2: Ripples of the AIDB variables in steady state

D	Δig	Δi_A	Δi_B	Δi_{AO}	Δi_{DB}	$\Delta(i_{AO}+i_{DB})$	Δv_{AB}	Δv_O
0.1	180.7	24.0	179.7	179.9	100.1 A	100.0 A	13.7	9.0 V
0.2	140.1	40.0	160.0	160.1	25.1 A	25.1 A	7.8	4.0 V
0.3	95.3	61.0	140.0	140.0	11.2 A	11.2 A	6.0	2.3 V
0.4	48.0	80.0	120.0	120.2	236.6	238.3	421.0	28.0
0.5	50.7	100.0	100.0	100.8	195.9	198.0	597.6	19.3
0.6	88.0	120.0	80.0	81.0	154.9	157.5	839.8	12.6
0.7	122.0	140.0	60.0	61.1	113.2	116.6	1214.1	7.5
0.8	152.0	160.0	40.0	41.9	69.8	74.9	1920.8	3.7
0.9	178.0	180.0	20.0	24.5	19.5	29.8	3960.4	1.0

(Excepting indications in the table, the currents are in mA and the voltages in mV)

For duty cycles below 38%, branch A is in DCM and the mean value of the inductor current I_A is very small. In that interval, branch B determines the output voltage because the mean value of the inductor L_{AO} current is also small. In that region of operation, the converter behaves basically as a simple boost converter and provides the following boost converter output voltage mean value:

$$V_O = \frac{V_g}{D_{SB}'} \quad (1)$$

Where the duty cycle of the S_B MOSFET is equal to D:

$$D_{SB}' = D \quad (2)$$

For $D<38\ \%$, the output voltage ripple is high (see Table 2.2), whereas the input current ripple is smaller in comparison (see Δv_o Δi_g Δi_B). The D_B diode is in conduction during the interval that is complementary to the conduction of the S_B MOSFET, and its current satisfies the equation

$$I_{DB} = D_{SB}' \cdot I_B = D \cdot I_B \quad (3)$$

This region of operation with duty cycles that are smaller than $38\ \%$ is of relatively little interest because there is no current distribution between the two branches of the circuit and the high output voltage ripple. The study of the AIDB converter will therefore focus on duty cycles greater than $38\ \%$.

Table 2.1 shows that for duty cycles greater than $38\ \%$, the mean values of the AIDB input inductor currents (I_A, I_B) are appreciable, which indicates that power is shared without any specific control strategy, a feature that is quite desirable. Moreover, the output voltage and input current ripples are comparatively small, particularly the output voltage ripple, which tends to zero when the duty cycle is increased.

In this region of operation, the only element in DCM mode is the D_B diode. The I_{DB} current has very small values compared with the I_B current and does not satisfy the expression (3). In this case, the expression is

$$I_{DB} << D_{SB}' \cdot I_B << D \cdot I_B \quad (4)$$

Other characteristics of the relationship between the variables of this mode of operation ($D<38\ \%$) will be studied in more detail in the following sections.

Figure 2.14 shows graphically the data of Table 2.1 (mean values) and Table 2.2 (ripples) for the two most important variables: the input current and the output voltage. It clearly shows the converter ripple behaviour and which duty cycles make the circuit behave better.

Finally, to conclude the simulation results, we saw that there are two different modes of operation for this system depending on the duty cycle. The duty cycle of $d=0.38$ represents a boundary between two main operation modes. For duty cycles greater than $38\ \%$, diode D_B operates in DCM, whereas for duty cycles lower than $38\ \%$, diode D_A operates in DCM. In this case, the circuit inherently operates in DCM; however, when the diode D_A is in DCM the converter has a large output ripple and does not distribute the input current, this being an undesirable feature in practice. Therefore, it is only cases where the duty cycle is greater than $38\ \%$ that are of any interest.

One advantage observed is that for duty cycles greater than $38\ \%$, the operation in DCM causes the input current to be unequally shared between the two branches of the circuit. This was observed in the waveforms of the input current and is verified by mathematically calculating the operating point in the next section (Equation (26)). This current distribution takes place without any specific control strategy, and minimizes the aggregated input current ripple. Therefore, the ripples of both output voltage and input current are relatively

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small, particularly the output voltage ripple which tends to zero as the duty cycle increases. Another advantage is that the input-to-output DC voltage transfer ratio is considerably improved, meaning that, for example, it is equal to three for $D=50\%$.

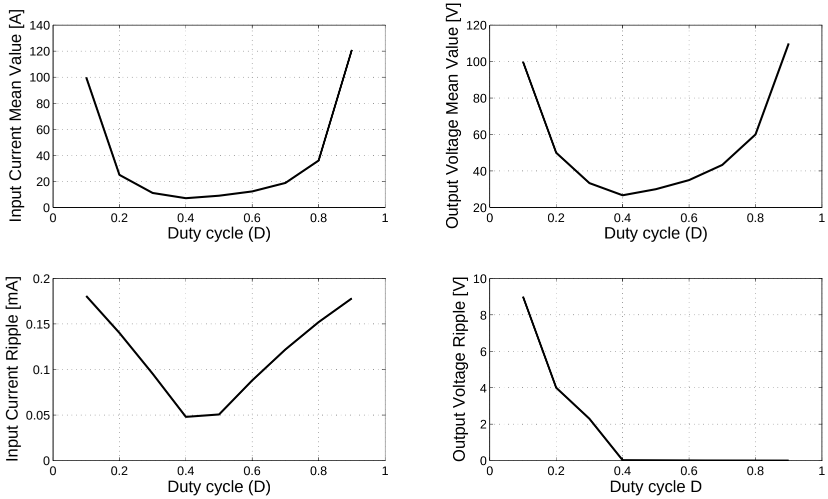

Figure 2.14: Mean values and ripples of the input current I_g and output voltage V_O in the AIDB Converter

2.4.2 AIDB TOPOLOGIES

The sequence of operation intervals can be defined using the Figure 2.15 that shows the DCM currents in the AIDB circuit for a duty cycle of 50%. It can be observed again that the output current i_O is equal to the sum of i_{DB} and i_{AO}. It also shows the moment at which the currents i_A and i_B are equal and the diode D_B does not conduct.

In Figure 2.15, the sequence of operation intervals are numbered 1, 2 and 3 and have the respective duration of d_1T, d_2T and d_3T. According to the figure, the definition of the operation intervals is:

$$d_1 + d_2 + d_3 = 1 \tag{5}$$

$$d_1 = d'; \quad d_2 + d_3 = d \tag{6}$$

The Figure 2.16 shows the topologies of the converter in every operation interval. The topologies were identified using both the waveforms of the simulation results and the usual procedure of assuming all the possible positions in the switches. The states of the switches in the four topologies are defined as:

- Topology 1 (S_B y D_A ON, S_A y D_B OFF). Interval 1: $d'=d_1$.
- Topology 2 (S_A y D_B ON, S_B y D_A OFF). Interval 2: d_2.
- Topology 3 (S_A ON, S_B, D_A y D_B OFF) where D_B is in DCM. Interval 3: d_3.
- Topology 4 (S_B ON, S_A, D_A y D_B OFF) where D_A is in DCM

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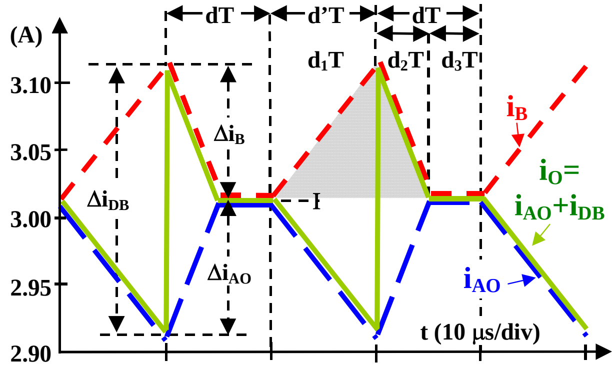

Figure 2.15: Definition of the relative duration of the three operation intervals (d_1, d_2 and d_3)

The two different modes of operation for this system, depending on the duty cycle, define the three topologies that are possible in every mode. For duty cycles greater than *38 %*, the circuit goes through the first three topologies in every corresponding interval (d_1T, d_2T and d_3T) and for duty cycles less than *38 %* the circuit goes through the first, second and fourth topologies.

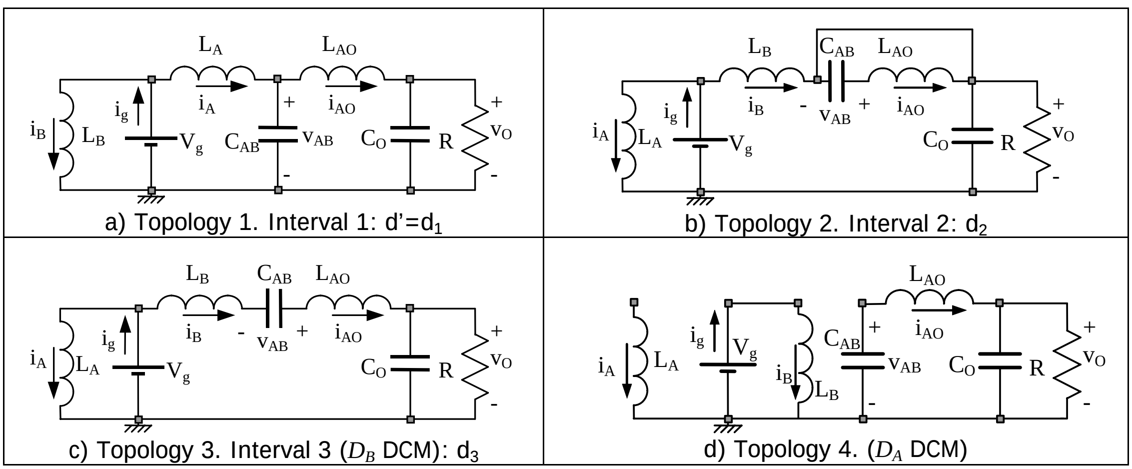

Figure 2.16: Topologies of the AIDB converter in each operation interval

2.4.3 FIRST APPROXIMATION OF THE AIDB OPERATING POINT

Using the topologies and the steady state waveforms obtained in the last two sections, it is possible to calculate the equations for a first approximation of the operating point of the AIDB under the hypothesis of low ripple in the state variables. In order to make these calculations, the mean values of the variables in steady state will be represented by capital letters. Therefore, the state variables will be defined as I_A, I_B, I_{AO}, V_{AB}, and V_O, the input voltage will be defined as V_g and the duty cycles will be defined as:

$$D_1 + D_2 + D_3 = 1 \tag{7}$$

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$$D_1 = D'; \quad D_2 + D_3 = D \tag{8}$$

2.4.3.1 MEAN VALUES OF THE CAPACITOR VOLTAGES IN STEADY STATE

In the AIDB circuit diagram (Figure 2.10), a permanent loop can be seen, which is constantly interconnected regardless of the states of the switches. This permanent loop is formed by the source voltage V_g, the inductors L_B and L_{AO}, and the capacitors C_{AB} and C_O.

Taking into account that the mean values of the inductor voltages are equal to zero in steady state (inductor flow balance), the following equation can be obtained by applying the KVL to the permanent loop of the AIDB.

$$V_g + V_{AB} = V_O \tag{9}$$

The steady state waveform of i_A in Figure 2.11 shows that the ripple amplitude can be easily calculated because of the linear form of the ripple.

The ripple amplitude calculated from the first topology (left side) and the ripple amplitude calculated from the second or third topology (right side) for the i_A current have to be equal. This gives

$$\frac{V_{AB} - V_g}{L_A} D'T = \frac{V_g}{L_A} DT \tag{10}$$

By using (10), it has been easy to derive the expression for the steady state mean value of the intermediate capacitor voltage V_{AB}, this being the same equation of the voltage of a boost with output filter in the intermediate capacitor.

$$V_{AB} = \frac{V_g}{D'} \tag{11}$$

The mean value of the AIDB output voltage can be calculated from (9) and (11)

$$V_O = V_{AB} + V_g = V_g \left(1 + \frac{1}{D'}\right) \tag{12}$$

2.4.3.2 EXPRESSIONS FOR THE DURATION OF THE OPERATION INTERVALS

Figure 2.11 shows the linear form of the i_B ripple in its steady state waveform. Therefore, when making the equation for the i_B current, the ripple amplitude calculated from the first topology (left side) must be equated with the ripple amplitude calculated from the second topology (right side), because in the third topology there is no ripple. This is gives the following equation:

$$\frac{V_g}{L_B} D'T = \frac{V_O - V_g}{L_B} (D - D_3) T \tag{13}$$

The simplification of (13) is

$$V_g (1 - D_3) = V_O (D - D_3) \tag{14}$$

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From (12) and (14), it can be obtained

$$D_3 = 1 - D' - D'^2 \tag{15}$$

The substitution of (8) in (15) gives

$$D_2 = D'^2 \tag{16}$$

(15) and (16) show another interesting characteristic of this converter, that is, it is possible to obtain the expressions for the duration of the operation intervals in steady state that are independent of the circuit parameters.

An analysis of D_3 explains the existence of the boundary in the duty cycle when D is approximately 0.38. The equation (15) is negative for values of D' higher than 0.618 or values of D less than 0.382. Refining the simulations in PSIM shows that for a very small interval around 0.382, the AIDB converter has the two branches in CCM and all the currents are different. If the duty cycle decreases further, the i_B current increases whereas the i_{AO} current approaches zero, making the diode D_A enter DCM.

This case is similar to the situation that was detected in the boost cell associations connected in parallel [2], in which the boost cell associations behave as voltage sources in open loop. The incompatibility that is created by connecting sources of different value in parallel voltage is resolved when one of the converters operates in CCM and the rest operate in DCM [2].

2.4.3.3 MEAN VALUES OF THE INDUCTOR CURRENTS IN STEADY STATE

The steady state waveform of v_{AB} in Figure 2.13 shows that the ripple has also a linear form. Therefore, by equating the ripple amplitude calculated from the first topology (left side) with the ripple amplitude calculated from the second or third topology (right side) for the v_{AB} voltage (capacitor charge balance), the following equation can be obtained

$$\frac{I_A - I_{AO}}{C_{AB}} D'T = \frac{I_{AO}}{C_{AB}} DT \tag{17}$$

By operating with (17), it has been easy to obtain the expression for the steady state mean value of the I_A inductor current

$$I_A = \frac{I_{AO}}{D'} \tag{18}$$

The steady state waveform of v_O (output voltage) is not linear, as can be seen in Figure 2.13; however, in order to calculate the mean values of the converter currents, a linear approximation has been made when calculating the ripple for this capacitor. Therefore, by equating the ripple amplitude of the output voltage (v_O) calculated from the first topology (left side) with the ripple amplitude calculated from the second or third topology (right side), the following equation can be obtained

$$\frac{\frac{V_O}{R} - I_{AO}}{C_O} D'T = \frac{I_B - \frac{V_O}{R}}{C_O} DT \tag{19}$$

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where

$$I_{AO} \cdot D' + I_B \cdot D = \frac{V_O}{R} \tag{20}$$

Since in the third topology the currents i_B and i_{AO} are equal, the equation in (19) can be written

$$\frac{\frac{V_O}{R} - I_{AO}}{C_O} D'T = \frac{I_B - \frac{V_O}{R}}{C_O} D_2 T + \frac{I_{AO} - \frac{V_O}{R}}{C_O} D_3 T \tag{21}$$

The substitution of (15) and (16) in the last equation gives

$$I_{AO}\left(1 - D'^2\right) + I_B \cdot D'^2 = \frac{V_O}{R} \tag{22}$$

From (20) and (22)

$$I_{AO} = I_B \tag{23}$$

The substitution of (23) in (20) with (12) yields

$$I_{AO} = I_B = \frac{V_g}{R}\left(1 + \frac{1}{D'}\right) \tag{24}$$

Finally, from (18)

$$I_A = \frac{V_g}{R}\left(1 + \frac{1}{D'}\right)\frac{1}{D'} \tag{25}$$

2.4.3.4 COMPARISONS WITH THE SIMULATION RESULTS

$$\begin{cases} I_A = \frac{1}{D'}\left(1 + \frac{1}{D'}\right)\frac{V_g}{R} \\ I_B = \left(1 + \frac{1}{D'}\right)\frac{V_g}{R} \\ I_{AO} = \left(1 + \frac{1}{D'}\right)\frac{V_g}{R} \\ V_{AB} = \frac{V_g}{D'} \\ V_O = \left(1 + \frac{1}{D'}\right)V_g \end{cases} \tag{26}$$

A comparative table has been made to verify if the expressions obtained in the last three subsections using conventional averaging assumptions are sufficiently accurate. The equations in (26) are a summary of the results for the steady state mean values of the circuit variables for duty cycles greater than *38 %*.

This summary of equations shows that for the point of operation there is a relationship between the currents:

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$$I_A = \frac{1}{D'} I_B = \frac{1}{D'} I_{AO} \qquad (27)$$

The values of the parameters used to calculate Table 2.3 are the same as those used in the simulations, that is: V_g=10 V, R_L=10 Ω, and the duty cycle goes from 40 % to 90 % in steps of 10 %. In the table, $I_g=I_A+I_B$.

Table 2.3: Mean values of the AIDB variables in steady state using expressions of (26)

D	Ig	I_A	I_B	I_{AO}	V_{AB}	V_O
0.4	7.11	4.44	2.67	2.67	16.67	26.67
0.5	9.00	6.00	3.00	3.00	20.00	30.00
0.6	12.25	8.75	3.50	3.50	25.00	35.00
0.7	18.78	14.44	4.33	4.33	33.33	43.33
0.8	36.00	30.00	6.00	6.00	50.00	60.00
0.9	121.00	110.00	11.00	11.00	100.00	110.00

(The currents are in A and the voltages in V)

The following table shows the errors in the steady state mean values when compared with Table 2.1.

Table 2.4: Errors of the AIDB variables in steady state (Comparing tables 2.1 and 2.3)

D	Ig	I_A	I_B	I_{AO}	V_{AB}	V_O
0.4	-0.02	-1.70	2.68	-1.78	-0.02	0.01
0.5	0.00	-0.84	1.64	-1.35	0.00	0.00
0.6	0.00	-0.34	0.85	-0.29	0.00	0.00
0.7	0.01	-0.10	0.38	-0.08	0.01	-0.01
0.8	0.00	-0.03	0.17	0.00	0.00	0.00
0.9	-0.02	-0.02	0.00	0.00	0.02	-0.02

(All the values are in %)

Table 2.4 shows that the expressions for the steady state mean values of the AIDB currents summarized in (26) are a good approximation but that they can be adjusted more closely to the simulation results because of the magnitude of the relative errors; this is especially the case for the smaller duty cycles. These issues will be studied in the third chapter. In contrast, the average values of the capacitor voltages are the same as those in the simulations, as is shown by their relative errors.

The appearance of the relative errors may initially be explained by the approximation that is made in the averaging when it is assumed that the average current value in one of the intervals coincides with the average current value throughout the period, without taking into account that two inductor currents have an interval with zero slope into one period. Another approximation was made to calculate the output voltage ripple, which was assumed to be linear.

2.4.4 Comparison between AIDB and interleaving boost including parasitics

In order to determine the behaviour of the converter when losses are considered, the simulations have been repeated with the same parameters for the system. These are: V_g=10 V, L_A=L_B=L_{AO}=1 mH, C_{AB}= 50 μF, C_O=20 μF, R_L=10 Ω, T=20 μs and a duty cycle from *10 %* to *90 %* with steps of *10 %*. However, these new simulations also include some conduction losses: r_L=r_C=1 mΩ for inductors and capacitors, r_{ON} =10 mΩ for the two MOSFET and V_{DON} = 0.8 V for the diodes. The simulation results can be seen in Table 2.5. The last column shows the efficiency for the AIDB including losses. It is around *96 %* and *97 %* for duty cycles between *0.4* and *0.8*, and drops to *89 %* for *D=0.9*. In the following tables the two zones of operation of the converter are well differentiated by a division.

Tabla 2.5: Mean values of the AIDB variables in steady state considering losses

D	Ig	I_A	I_B	I_{AO}	I_{DB}	$I_{AO}+I_{DB}$	V_{AB}	V_O	η (%)
0.1	90.06	1.1 *mA*	90.06	52.3 *μA*	9.01	9.01	80.14	90.05	90.09
0.2	24.04	5.4 *mA*	24.04	1.3 *mA*	4.81	4.81	38.11	48.08	96.20
0.3	10.74	15.8 *mA*	10.73	6.8 *mA*	3.22	3.22	22.24	32.33	96.93
0.4	6.88	4.23	2.65	2.54	42.3 *mA*	2.58	15.79	25.78	96.68
0.5	8.72	5.76	2.96	2.88	24.2	2.91	19.07	29.06	96.98
0.6	11.88	8.46	3.43	3.88	12.2 *mA*	3.40	23.96	33.95	97.16
0.7	18.20	13.98	4.22	4.19	4.9 *mA*	4.20	32.01	42.00	96.92
0.8	34.55	28.78	5.77	5.76	1.3 *mA*	5.76	47.59	57.58	95.99
0.9	108.10	98.27	9.83	9.83	0.0 *mA*	9.83	88.29	98.27	89.36

(Excepting indications in the table, the currents are in *A* and the voltages in *V*)

In order to provide a comparison, steady state simulations were also carried out using two interleaved boost converters with a single conventional output filter (see Figure 2.17).

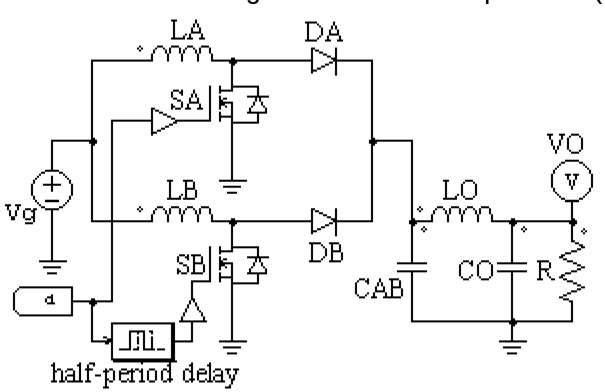

Figure 2.17: Two boost converters in interleaving with a single output filter

The duty cycles of the two interleaved boost converters are calculated so they obtain the same theoretical output voltage as the AIDB. This makes the two converters almost equivalent. The parameters of the two interleaved boost converters are: input inductor and

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output filter inductor of $1\ mH$, intermediate capacitor of $50\ \mu F$, output capacitor of $20\ \mu F$, and a $10\ \Omega$ resistor load. The same losses as the AIDB have been considered.

Table 2.6 shows the simulation results of the converter in the last figure. It is important to note that the two interleaved boost converters with a single output filter have more difficulties because a control must be applied to maintain the distribution of the input current. This is not necessary in the AIDB because the input current distribution occurs without any control strategy. The last column shows the efficiency including losses. It is around $97\ \%$ and $96\ \%$ for duty cycles between 0.6 and 0.9. These high duty cycles (greater than 0.5) make it more difficult to control the circuit.

Table 2.6: Mean values of the variables in steady state of the two boost converters in interleaving with a single output filter considering losses

D	Ig	I_A	I_B	I_{LO}	I_{DB}	$I_{DA}+I_{DB}$	V_{AB}	V_O	η (%)
0.9	94.43	47.21	47.21	9.44	4.72	9.43	94.43	94.42	94.29
0.8	24.32	12.16	12.16	4.86	2.43	4.86	48.64	48.64	97.20
0.7	10.79	5.40	5.40	3.24	1.62	3.24	32.39	32.38	97.23
0.625	6.88	3.44	3.44	2.56	1.29	2.58	25.80	25.80	96.75
0.667	8.91	4.46	4.46	2.94	1.47	2.94	29.40	29.40	97.01
0.714	11.97	5.99	5.98	3.41	1.70	3.41	34.11	34.11	97.17
0.769	18.40	9.20	9.20	4.23	2.12	4.23	42.32	42.32	97.29
0.833	35.62	17.81	17.81	5.88	2.94	5.87	58.78	58.78	96.87
0.909	115.31	57.66	57.65	10.38	5.19	10.37	103.79	103.78	93.33

(Excepting indications in the table, the currents are in A and the voltages in V)

A comparison of the last two tables shows that the efficiency is better in the interleaved converter when losses have been considered (although it is the same for small duty cycles).

Tables 2.7 and 2.8 show the ripples of the two converters including losses. Again, the duty cycles of the two interleaved boost converters are calculated so they obtain the same theoretical output voltage as the AIDB. In this way, the two converters are almost equivalent.

Table 2.7: Ripples of the AIDB variables in steady state considering losses

D	Δig	*% of Ig*	Δi_A	Δi_B	Δi_{AO}	Δi_{DB}	$\Delta(i_{AO}+i_{DB})$	Δv_{AB}	Δv_O	*% of V_O*
0.1	161.0	*0.18 %*	20.0	162.2	161.9	90.2 A	90.1 A	8.2	8.2 V	*9.11 %*
0.2	70.7	*0.29 %*	40.0	155.7	155.6	24.2 A	24.1 A	7.5	3.9 V	*8.11 %*
0.3	93.4	*0.87 %*	60.0	138.3	138.3	10.9 A	10.8 A	5.6	2.3 V	*7.11 %*
0.4	47.7	*0.69 %*	79.6	119.5	119.6	235.5	237.2	410.6	28.0	*0.11 %*
0.5	50.4	*0.58 %*	99.4	99.4	100.1	194.7	196.7	584.8	19.2	*0.07 %*
0.6	87.1	*0.73 %*	118.9	79.3	80.2	153.5	156.0	823.2	12.6	*0.04 %*
0.7	120.1	*0.66 %*	137.8	59.1	60.1	111.5	114.9	1190.8	7.4	*0.02 %*
0.8	147.0	*0.43 %*	154.8	38.8	40.6	67.6	72.6	1872.1	3.6	*0.01 %*
0.9	159.0	*0.15 %*	160.6	18.0	21.9	17.6	26.8	3366.3	1.3	*0 %*

(Excepting indications in the table, the currents are in mA and the voltages in mV)

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In the duty cycles of interest, the output voltage ripple is better for the interleaving case, although in the worst case the ripple of the AIDB output voltage does not exceed the *0.11 %* of the mean value, and improves as the duty cycle increases.

The ripple in the input current is similar in both cases: less than *160 mA* in the worst case and always below *0.9 %* in relative terms.

Table 2.8: Ripples of the two boost converters in interleaving with a single output filter variables in steady state considering losses

D	Δig	*% of Ig*	Δi_A	Δi_B	Δi_{LO}	Δi_{DB}	$\Delta(i_{DA}+i_{DB})$	Δv_{AB}	Δv_O	*% of V_O*
0.9	151.6	*0.16 %*	170.6	170.6	1.9	47.3 *A*	47.3 *A*	1558.1	0.2	*0 %*
0.8	118.4	*0.49 %*	157.9	157.9	0.7	12.2 *A*	12.2 *A*	595.9	0.1	*0 %*
0.7	79.6	*0.74 %*	152.5	152.4	0.3	5.5 *A*	5.5 *A*	264.5	0.0	*0 %*
0.625	49.8	*0.72 %*	124.5	124.5	0.2	3.5 *A*	3.5 *A*	132.5	0.0	*0 %*
0.667	67.7	*0.76 %*	133.4	133.4	0.3	4.5 *A*	4.5 *A*	204.5	0.0	*0 %*
0.714	85.5	*0.71 %*	142.1	142.1	0.3	6.1 *A*	6.1 *A*	299.5	0.1	*0 %*
0.769	106.9	*0.58 %*	152.5	152.4	0.6	9.3 *A*	9.3 *A*	466.3	0.0	*0 %*
0.833	131.4	*0.37 %*	163.7	163.7	1.0	17.9 *A*	17.9 *A*	805.6	0.1	*0 %*
0.909	153.0	*0.13 %*	170.5	170.5	2.1	57.7 *A*	57.7 *A*	1760.0	0.0	*0 %*

(Excepting indications in the table, the currents are in *mA* and the voltages in *mV*)

To conclude, a comparison of the results shows that the AIDB performs well even when losses are taken into account. Certain results are better with the two interleaved boost converters, but it is important to remark that it is easier to design the control for the AIDB because it does not need a control to share the input current (input power) between the two branches. In addition, for the same theoretical output voltage, the high duty cycles (greater than *0.5*) needed for the two interleaved boost increase the losses and stress in components and make it more difficult to control the circuit than the duty cycles of the AIDB.

2.5 THE FAMILY OF ASYMMETRICAL INTERLEAVING CONVERTERS

The concept of complementary interleaving and the methodology of modifying the converter structure in order to improve its characteristics can be applied to different elementary converters and can generate a family of converters. The converters of the asymmetrical interleaving family, whose first member is the AIDB, have the same main characteristics: the low ripple in global variables, the two zones of operation and others that will be featured in the following sections.

2.5.1 THE AIDBB

If the same circuit generation methodology described from section 2.2.2 to section 2.3.1 is applied to a different basic structure, that is, the buck-boost converter, it is possible to generate a new circuit with other interesting characteristics [6].

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2.5.1.1 STRUCTURE GENERATION

The first structure considered is the IDBB in Figure 2.18a. This structure was generated by applying the complementary interleaving technique to the parallel of two buck-boost converters. This structure has the same disadvantages as the IDB. The SCIDBB (Figure 2.18b) was obtained by following a similar procedure to the one described in 2.2.3 and 2.2.4.

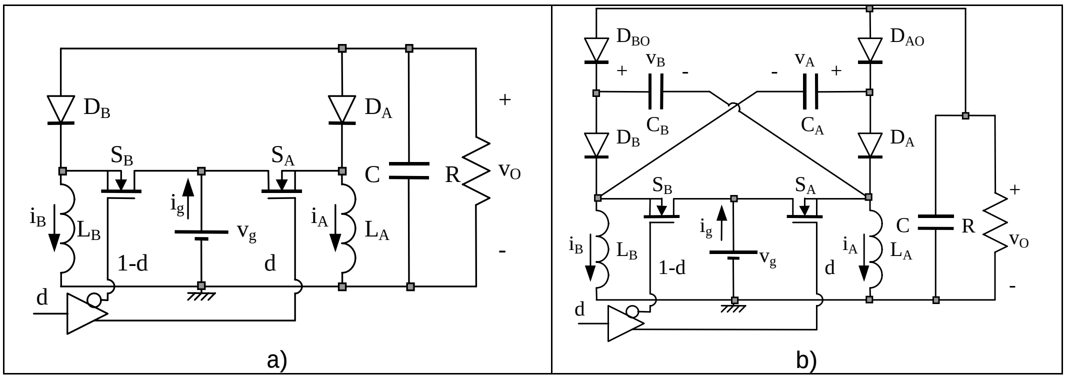

Figure 2.18: a) Interleaved dual buck-boost (IDBB) and b) Switched capacitor interleaved dual buck-boost (SCIDBB)

The IDBB and the SCIDBB operate symmetrically for a *50 %* duty cycle. The SCIDBB has an important drawback: a high output voltage ripple. This disadvantage can be solved following the two options already described in 2.3.1. The first option is to increase the output filter order by adding an inductor and the second option is to increase the order of the output filter by substituting the diodes D_{AO} and D_{BO} with two inductors.

The second option was chosen because it still allows the structure to be modified. The name of this circuit is SCIDOFBB (see Figure 2.19).

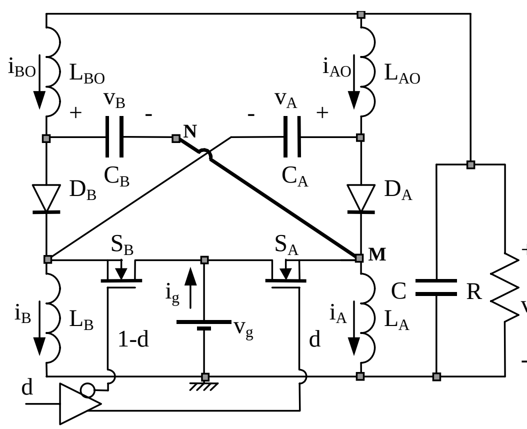

Figure 2.19: Switched capacitor interleaved dual output filter buck-boost (SCIDOFBB)

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Except for a narrow margin around a *50 %* duty cycle, diodes D_A and D_B of the SCIDOFBB operate in discontinuous conduction mode (DCM). As with IDBB and SCIDBB, the new structure SCIDOFBB behaves symmetrically regarding to a *50 %* duty cycle, which reduces by half the regulation capabilities of the converter.

In order to extend the duty cycle margins of operation, the same procedure described in 2.3.1 is applied to the SCIDOFBB. The circuit symmetry for $D=50$ % is broken by disconnecting the Node N from the Node M (Figure 2.19) and reconnecting N to the reference node.

For $D>50\%$, the mean values of the currents flowing through the inductor L_{BO} and the capacitor C_B associated to the diode D_B are very small in DCM. For this reason these currents are considered negligible compared with other currents in the circuit and, therefore, these elements can be eliminated.

The suppression of inductor L_{BO} and capacitor C_B creates a new converter, the asymmetrical interleaved dual buck-boost (AIDBB) (see Figure 2.20). In the figure, the name of capacitor C_A has been changed to C_{AB}.

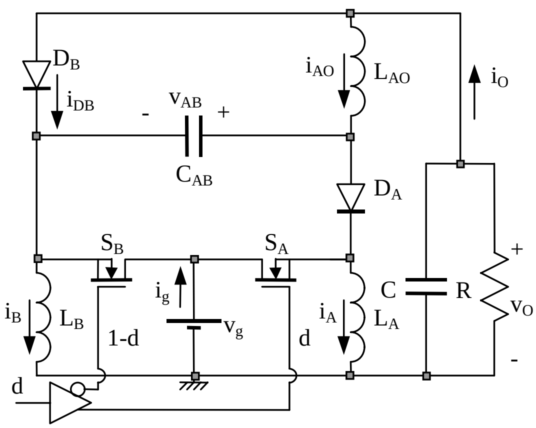

Figure 2.20: Asymmetrical interleaved dual buck-boost (AIDBB)

The AIDBB converter can be seen as a parallel interconnection of a buck-boost simple cell (branch B) and a buck-boost with output filter (branch A) in which the first capacitor of the A-branch output filter is connected to the intermediate node of the buck-boost of the B-branch, in the same way as capacitors C_A and C_B are connected in the SCIDBB converter.

2.5.1.2 SIMULATION RESULTS: WAVEFORMS

The simulation results were obtained using the PSIM program with the following parameters for the AIDBB converter circuit (Figure 2.20): $V_g=10\ V$, $L_A=L_B=L_{AO}=1\ mH$, $C_{AB}=50\ \mu F$, $C_O=20\ \mu F$, $R_L=10\ \Omega$, $T=20\ \mu s$. A duty cycle of *60 %* was used in order to obtain the waveforms of the circuit.

The Figure 2.21 shows a detail of the output voltage ripple (v_O) and the intermediate capacitor voltage ripple (v_{AB}). It can be observed that, as in the AIDB, the voltage in the

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capacitor C_{AB} has only two subintervals (with positive and negative slopes respectively) because the discontinuous conduction of the diode D_B has no influence on C_{AB} voltage.

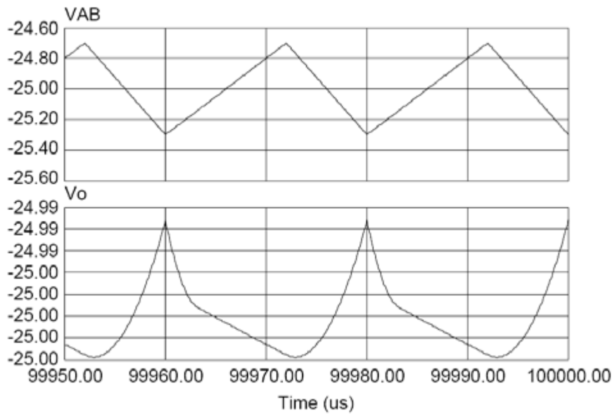

Figure 2.21: Waveforms of the AIDBB capacitor voltages simulated by PSIM

The waveform of v_O (Figure 2.21a) has a ripple of -*12.7 mV* over a mean value of -*25 V*, which is *0.051 %* above the mean value. As can be seen, this converter offers a negative input-to-output voltage conversion ratio, since the output voltage has the opposed polarity of the input voltage. The v_O ripple has the same shape as the ripple of the AIDB but in negative direction.

Figure 2.22 shows the waveforms of the circuit's output currents. As in the AIDB converter, the output voltage ripple is determined by the current $I_O=I_{AO}+I_{DB}$ that is flowing through the output capacitor, which can be seen in the third plot. The output current has a mean value of *2.50 A* and a ripple of *157.5 mA*, which corresponds to *6.3 %* of the mean value.

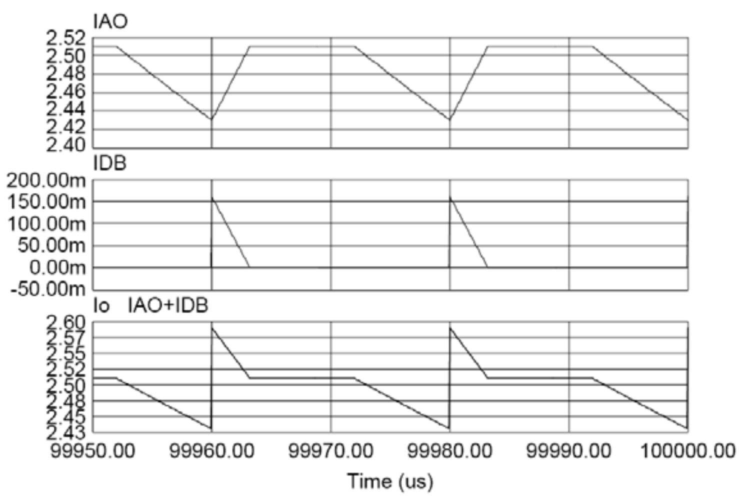

Figure 2.22: Output currents in the AIDBB: a) I_{AO}, b) I_{DB} and c) $I_O=I_{AO}+I_{DB}$

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The second plot shows that the diode D_B is operating in DCM. The positive direction has been chosen in order to display the waveforms of the circuit currents in all the plots.

Figure 2.23 shows the waveforms of the circuit's input currents. It can be seen that the input current waveforms behave in very similar way to those of the AIDB. The I_A current has only two intervals because the I_B current is affected by the DCM mode in I_{DB}. The input current has been calculated slightly differently from that of the AIDB; in this case Ig is the addition of the I_A and I_B currents minus the output current ($I_O=I_{AO}+I_{DB}$). It is important to remark that the input current ripple $\Delta ig=160\ mA$ is significantly smaller compared with its mean value $Ig=6.25\ A$ ($2.54\ \%$).

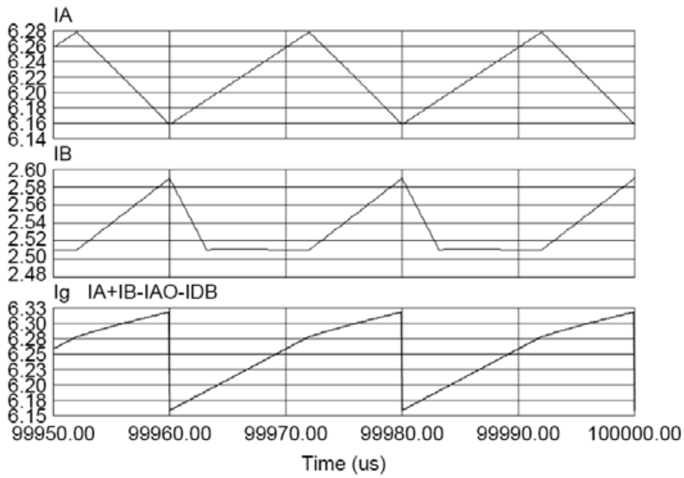

Figure 2.23: Input currents in the AIDBB: a) I_A, b) I_B, c) $Ig = I_A + I_B - I_O$

The superposition of the I_{AO}, I_B, I_{DB} and I_O currents in the same plot (Figure 2.24) demonstrates that the output current ripple has the same magnitude as the addition of the I_{AO} and I_B ripple. This addition is also equal to the magnitude of the I_{DB} ripple, if the DC level is not taken into account.

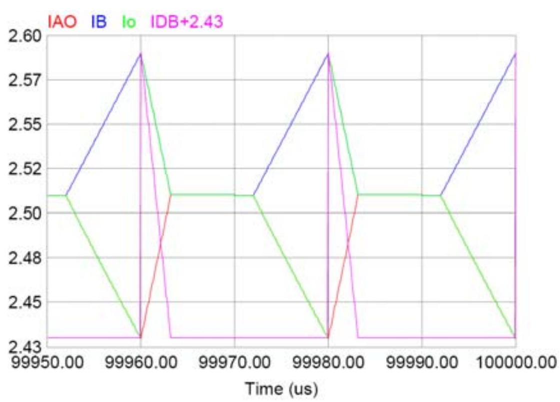

Figure 2.24: Superposition of the I_{AO}, I_B, I_{DB} and I_O currents in the same screen

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2.5.1.3 SIMULATION RESULTS: TABLES

Table 2.9 shows the mean values and Table 2.10 shows the ripples in steady state for the following AIDBB converter variables: the input current ($I_g = I_A + I_B$), the inductor state variables (I_A, I_B, I_{AO}), the diode current (I_{DB}), the output current ($I_{AO}+I_{DB}$) and the capacitor state variables (V_{AB}, V_O) The data are obtained from the steady state waveforms in the [*99,5 ms* - *100 ms*] interval when the converter starts up from zero initial conditions. The duty cycle is varied from 30 % to 90 % in steps of 10 %. Simulations with duty cycles smaller than 30 % showed high input current ripples and the results obtained were disregarded

Table 2.9: Mean values of the AIDBB variables in steady state

D	Ig	I_A	I_B	I_{AO}	I_{DB}	$I_{AO}+I_{DB}$	V_{AB}	V_O
0.3	2.63	37.8 *mA*	4.21	23.2 *mA*	1.60	1.62	-16.22	-16.21
0.4	2.78	2.71	1.74	1.62	42.5 *mA*	1.67	-16.67	-16.67
0.5	4.00	3.95	2.05	1.98	24.4 *mA*	2.00	-20.00	-20.00
0.6	6.25	6.22	2.53	2.49	12.3 *mA*	2.50	-25.00	-25.00
0.7	11.10	11.10	3.35	3.33	5.0 *mA*	3.33	-33.33	-33.33
0.8	24.99	24.99	5.01	5.00	1.3 *mA*	5.00	-50.00	-50.00
0.9	99.99	99.98	10.00	10.00	-	10.00	-99.98	-99.98

(Excepting indications in the table, the currents are in *A* and the voltages in *V*)

As with the AIDB, Table 2.9 shows that it is possible to differentiate two operating regions whose border is around $D=0.38$. It can be also seen that the AIDBB behaves in the same way as the AIDB converter; for $D<0.38$, branch A is in DCM and therefore the mean value of inductor current I_A is very small and the mean value of inductor current I_B establishes the mean value of the output voltage because I_{AO} is also small.

As occurs in the AIDB, the AIDBB's global variables have high ripples. For this reason the study will focus on duty cycle values higher than *38 %*.

Table 2.10: Ripples of the AIDBB variables in steady state

D	Δig	Δi_A	Δi_B	Δi_{AO}	Δi_{DB}	$\Delta(i_{AO}+i_{DB})$	Δv_{AB}	Δv_O
0.3	4.32 *A*	76.5	129.3	126.6	4.31 *A*	4.32 *A*	6.8	1.02 *V*
0.4	240.0	80.0	120.0	120.1	236.6	238.3	260.4	27.9
0.5	199.0	100.0	100.0	100.5	195.9	198.0	397.6	19.2
0.6	159.0	120.0	80.0	80.7	154.9	157.5	599.8	12.5
0.7	139.0	140.0	60.0	60.8	113.2	116.6	934.1	7.4
0.8	158.9	160.0	40.0	41.6	69.8	74.9	1600.8	3.7
0.9	178.3	179.6	20.0	24.0	19.5	29.8	3599.7	1.3

(Excepting indications in the table, the currents are in *mA* and the voltages in *mV*)

For $D>40\,\%$, Tables 2.9 and 2.10 show that the only element in DCM is the diode D_B, whose current I_{DB} has mean values which are much smaller than those of current I_B ($I_{DB} << D \bullet I_B$). In this operating mode, ripples of both output voltage and input current are relatively small, particularly the output voltage ripple, which tends to zero as the duty cycle increases.

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Table 2.9 shows the conversion ratio of the AIDBB for $D>40\,\%$ and relates the output voltage with the input voltage and the duty cycle. This relationship is:

$$V_O = V_g\left(-\frac{1}{D'}\right) \tag{28}$$

From these simulation results it can be concluded that the AIDBB behaviour in steady state is very similar to the steady state behaviour of the AIDB converter, because they have many characteristics in common which will be described in the following two paragraphs.

The AIDBB converter in steady-state has an operation frontier at a duty cycle of approximately *38 %*. Above this frontier, diode D_B operates in DCM, whereas for smaller duty cycles, it is diode D_A that operates in DCM. Since there is always one diode in DCM, the circuit operates inherently in DCM.

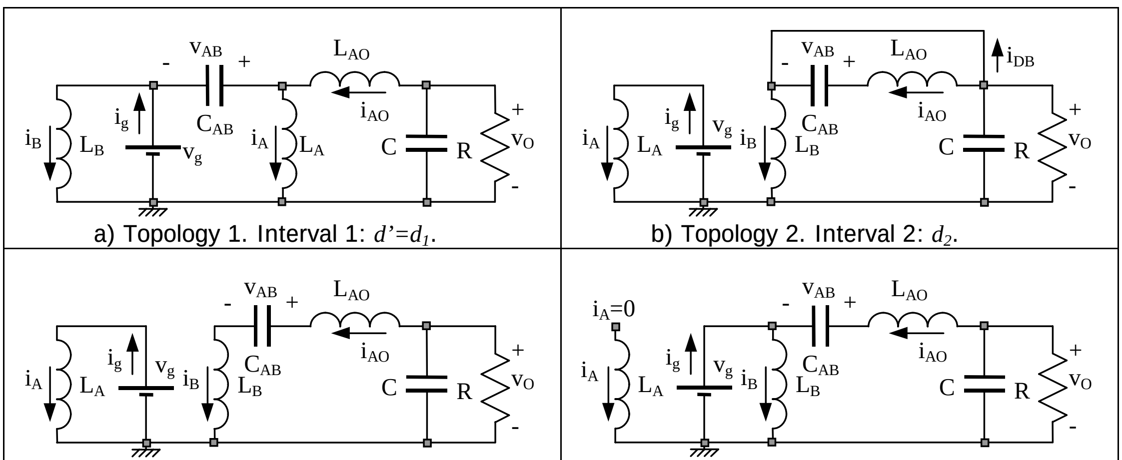
If the duty cycle is greater than 38 %, then operating in DCM causes an unbalanced sharing of the input current between the two branches of the circuit. This can be seen in the mean values of I_A and I_B shown in Table 2.9. Because of this current distribution (which occurs without using any control strategy), the aggregated input current ripple is minimized.

2.5.1.4 AIDBB TOPOLOGIES

The same procedure used for the AIDB can be applied to the AIDBB converter, whose different topologies are obtained first as a function of the conduction states of the MOSFETs and diodes and second from the simulation waveform.

Figure 2.25 shows the topologies of the converter in every operation interval. The states of the switches in the four topologies are as follows:

- Topology 1 (S_B y D_A ON, S_A y D_B OFF). Interval 1: $d'=d_1$.
- Topology 2 (S_A y D_B ON, S_B y D_A OFF). Interval 2: d_2.
- Topology 3 (S_A ON, S_B, D_A y D_B OFF) where DB is in DCM. Interval 3: d_3.
- Topology 4 (S_B ON, S_A, D_A y D_B OFF) where D_A is in DCM



a) Topology 1. Interval 1: $d'=d_1$.
b) Topology 2. Interval 2: d_2.
c) Topology 3 (D_B DCM) Interval 3: d_3.
d) Topology 4 (D_A DCM)

Figure 2.25: Topologies of the AIDBB converter in each operation interval

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The two different operating modes for this system, depending on the duty cycle, defined the three topologies that were possible in every mode. For duty cycles greater than *38 %*, the circuit goes through the first three topologies in every corresponding interval (d_1T, d_2T and d_3T) and for duty cycles less than *38 %* the circuit goes through the first, second and fourth topology. The same figure as that used for the AIDB (Figure 2.15) can be used to define the times of operation of every topology in the AIDBB.

2.5.1.5 FIRST APPROXIMATION TO THE AIDBB OPERATING POINT

The methodology that was described in 2.4.3 for the AIDB will be used to obtain the AIDBB's expressions for the variables in steady state.

2.5.1.5.1 MEAN VALUES OF THE CAPACITOR VOLTAGES IN STEADY STATE

In the AIDBB circuit diagram (Figure 2.20), there is also a permanent loop, which is formed by the inductors L_B and L_{AO}, and the capacitors C_{AB} and C_O. From this loop, the following equation can be obtained

$$V_{AB} = V_O \tag{29}$$

From the steady state waveform of i_A, the following equality can be obtained

$$\frac{V_{AB}+V_g}{L_A} D'T = -\frac{V_g}{L_A} DT \tag{30}$$

Equation (30) gives the expression for the steady state mean value of the intermediate capacitor voltage V_{AB}, which is the same as the mean value of the AIDB output voltage (29)

$$V_{AB} = V_O = -\frac{V_g}{D'} \tag{31}$$

2.5.1.5.2 EXPRESSIONS FOR THE DURATION OF THE OPERATION INTERVALS

From the steady state waveform of i_B the following equality can be obtained

$$\frac{V_g}{L_B} D'T = \frac{V_O}{L_B}(D-D_3)T \tag{32}$$

The simplification of (32) gives

$$V_g(D') = V_O(D-D_3) \tag{33}$$

After combining (31) and (33) and arranging the terms, it was found that the duration of the AIDBB's operation intervals was the same relationship as that of the AIDB, as can be seen in equations (15) and (16).

2.5.1.5.3 MEAN VALUES OF THE INDUCTOR CURRENTS IN STEADY STATE

The steady state waveform of v_{AB} gives

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$$\frac{I_{AO}-I_A}{C_{AB}}D'T=-\frac{I_{AO}}{C_{AB}}DT \tag{34}$$

Equation (34) can be used to calculate the expression for the steady state mean value of the I_A inductor current, which is

$$I_A=\frac{I_{AO}}{D'} \tag{35}$$

The steady state waveform of v_O can be used to calculate the following expression

$$-\frac{I_{AO}+\frac{V_O}{R}}{C_O}D'T=\frac{I_B+\frac{V_O}{R}}{C_O}DT \tag{36}$$

The simplification of (36) gives

$$I_{AO}\cdot D'+I_B\cdot D=-\frac{V_O}{R} \tag{37}$$

Given that the currents i_B and i_{AO} in the third interval are equal, the equation in (36) can be written

$$-\frac{I_{AO}+\frac{V_O}{R}}{C_O}D'T=\frac{I_B+\frac{V_O}{R}}{C_O}D_2T+\frac{I_{AO}+\frac{V_O}{R}}{C_O}D_3T \tag{38}$$

The substitution of (15) and (16) in Equation (38) yields

$$I_{AO}\left(1-D'^2\right)+I_B\cdot D'^2=-\frac{V_O}{R} \tag{39}$$

From (37) and (39)

$$I_{AO}=I_B \tag{40}$$

The substitution of (40) in (37) yields

$$I_{AO}=I_B=\left(\frac{1}{D'}\right)\frac{V_g}{R} \tag{41}$$

Finally, from (35)

$$I_A=\left(\frac{1}{D'^2}\right)\frac{V_g}{R} \tag{42}$$

The following (43) is a summary of the equations for the steady state mean values of the circuit variables for duty cycles greater than *38 %*. This summary shows that the AIDBB has the same relationship between the currents as that which was described in (27) for the AIDB.

This calculation is a first approximation to the operating point of the AIDBB converter. This approximation will be improved by the methodology that will be exposed in the third chapter.

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$$\begin{cases} I_A = \left(\dfrac{1}{D'^2}\right)\dfrac{V_g}{R} \\ I_B = \left(\dfrac{1}{D'}\right)\dfrac{V_g}{R} \\ I_{AO} = \left(\dfrac{1}{D'}\right)\dfrac{V_g}{R} \\ V_{AB} = -\dfrac{V_g}{D'} \\ V_O = -\dfrac{V_g}{D'} \end{cases} \tag{43}$$

2.5.1.6 Comparison with the IBB

A comparison has been made between ripple values of the AIDBB input currents and the IBB input currents to verify one of the main advantages of the interleaving operation that was explained in the section 2.1 and plotted in the Figure 2.1. The IBB circuit, as can be seen in Figure 2.26, has two conventionally Interleaved Buck-Boost converters with a common third-order output filter.

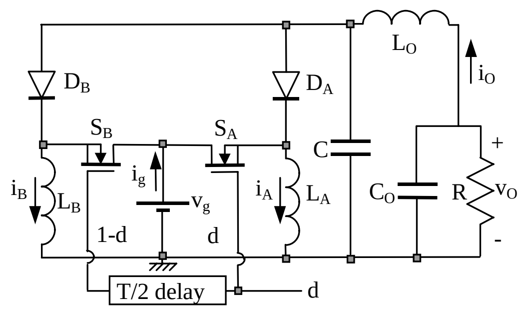

Figure 2.26: Two conventionally Interleaved Buck-Boost converters (IBB) with a common third-order output filter

In order to perform the IBB simulations in approximately the same conditions as the AIDBB simulations, the IBB's duty cycles must be calculated taking into account that the output voltage and input current of the two converters were approximately equal. The simulation results are shown in Table 2.11.

Table 2.11: Ripples of the IBB input currents in steady state

AIDBB D	*D IBB*	AIDBB Δig	Δig *IBB*	AIDBB Δi_A	Δi_A *IBB*	AIDBB Δi_B	Δi_B *IBB*
0.4	*0.625*	240.0	*2.32 A*	80.0	*125*	120.0	*125*
0.5	*0.667*	199.0	*3.06 A*	100.0	*133*	100.0	*133*
0.6	*0.714*	159.0	*4.51 A*	120.0	*143*	80.0	*143*
0.7	*0.769*	139.0	*7.39 A*	140.0	*154*	60.0	*154*
0.8	*0.833*	158.9	*15.46 A*	160.0	*167*	40.0	*167*
0.9	*0.90*	178.3	*56.31 A*	179.6	*182*	20.0	*182*

(Current ripples are in *mA* except indications in the table)

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The results of the IBB are written in italic letters so they can be clearly seen. A comparison of both circuits' simulated results reveals that the AIDBB exhibits lower ripple for each duty cycle in all the input currents than the IBB. The ripple is much lower, especially in the input current i_g, due to the ripple addition when the converters are interleaved.

2.5.2 THE AIDF-GROUP

Six possible structures of interest can be found if the same procedure that was followed in previous circuit generations is applied to two flyback converters. These six circuits constitute a new group of converters called Asymmetrical Interleaved Dual Flyback (AIDF) converters [7].

2.5.2.1 GENERATION OF THE CONVERTERS' GROUP

The AIDF converters are generated from AIDBB by substituting the inductor for transformers in order to obtain a new conversion ratio. The buck-boost structures change into flyback structures. For this reason, the AIDF converter group has the same operation characteristics as the AIDBB. For example, the ripples of the output voltage and input current are very small in comparison with their mean values and the input power is divided between the two branches of the structures without using any control strategy.

The structures of the new AIDF group can be seen in Figure 2.27, where the I_A and I_B currents represent the magnetization currents of the transformers. The negative output voltage AIDF converter in Figure 2.27(a) works in a similar way to the AIDBB, as is shown by the simulation waveforms in the following section. The new characteristic of this circuit is that different values for n_A and n_B can be used, thus increasing the conversion ratio range.

The others structures were generated by taking advantage of the flyback transformer. In Figure 2.27(b) the AIDF of positive output voltage uses the flyback in order to invert the output voltage. The structures in Figures 2.27(c) and 2.27(d) can have a floating load if the isolation of the transformers is broken. This condition also allows the creation of the structures in Figures 2.27(e) and 2.27(f), whose input voltage is connected to the secondary sides of the flyback transformers.

2.5.2.2 ANALYSIS OF SIMULATION RESULTS: WAVEFORMS AND TABLES

Again, PSIM was used for the simulations. The values of the parameters for all the converters in the AIDF family have been taken from the previous simulations of the AIDBB [6]. These values are: $V_g=10\ V$, $L_A=L_B=L_{AO}=1\ mH$, $C_{AB}=\ 50\ \mu F$, $C_O=20\ \mu F$, $R_L=10\ \Omega$, $T=20\ \mu s$ and a duty cycle of $60\ \%$. The transformer relationship was selected so it could be compared with the AIDBB. Its value is $n_A/n_B=1$. The waveforms of the output voltage and input current for all the converters in the AIDF family are shown in Figure 2.28.

Table 2.12 lists the numerical results of the simulation. The columns headed with the symbol *%* show the percentage of the mean value of each ripple. The results show that input current and output voltage ripples for all the structures in the AIDF converter family are very low in relation with their mean values.

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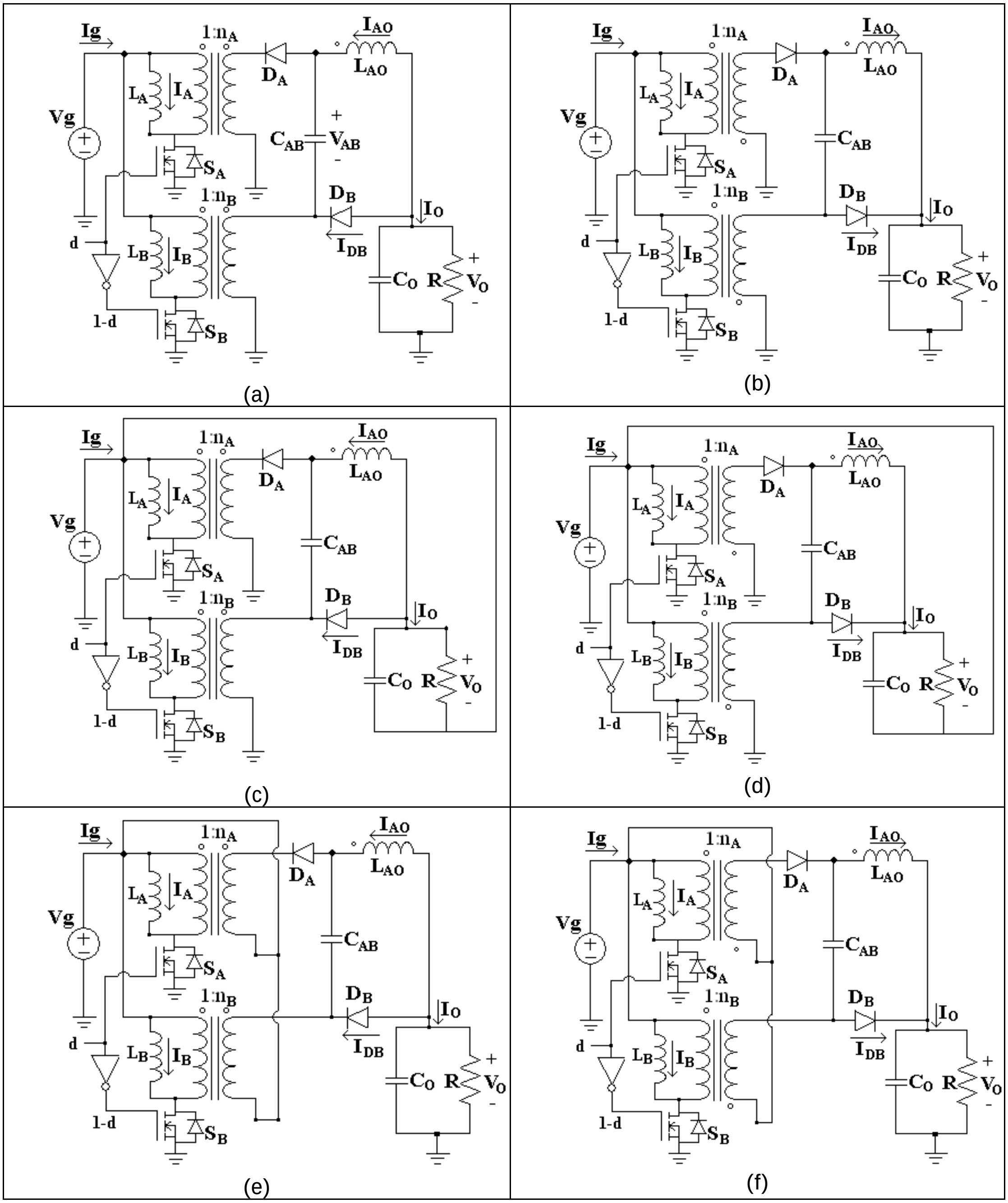

Figure 2.27: Asymmetrical Interleaved Dual Flyback (AIDF) converters

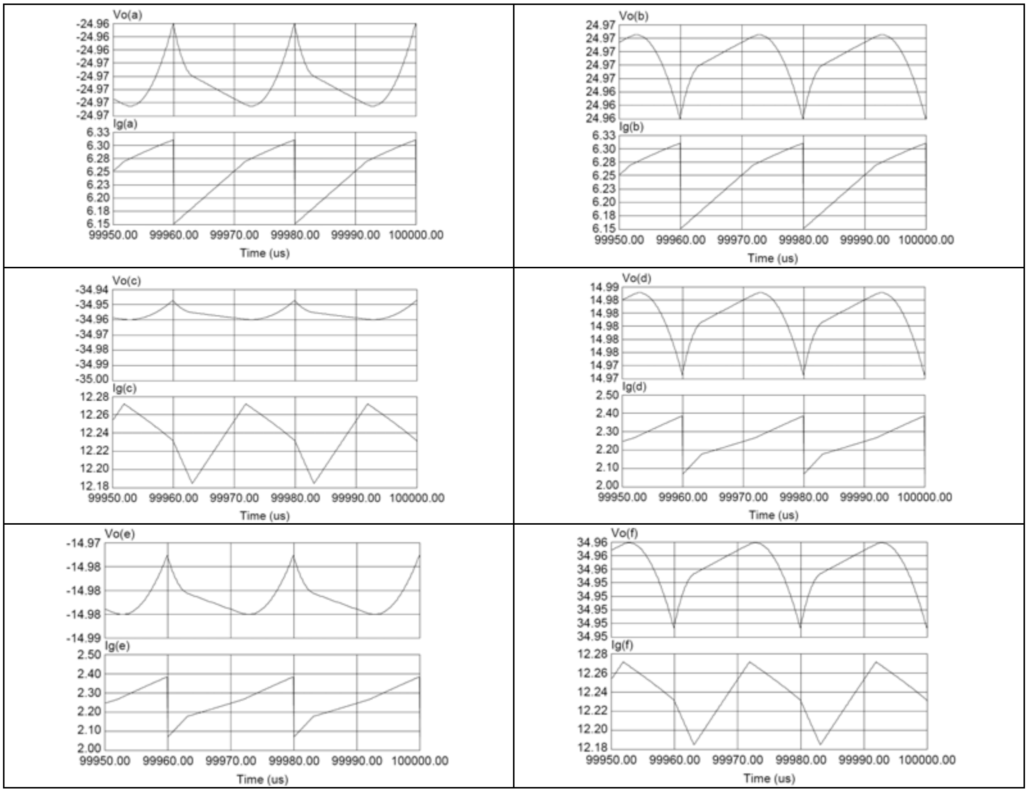

Figure 2.28: Simulation results of all the converters in the AIDF Family

Table 2.12: Numerical Values for the steady state input current and output voltage of the AIDF Converters Family

AIDF Structure	*Ig(A)*	*Δig(mA)*	*%*	$V_o(V)$	$\Delta v_O(mV)$	*%*
a	6.24	158.87	2.55	-24.97	12.5	0.05
b	6.24	158.87	2.55	24.97	12.5	0.05
c	1.23	87.50	0.72	-34.97	12.3	0.04
d	2.24	313.91	14	14.90	12.3	0.08
e	2.25	316.27	14.1	-14.98	12.4	0.08
f	12.23	87.50	0.72	34.96	12.6	0.04

In order to make some comparisons between the simulation results of AIDBB and the AIDF of negative output (Figure 2.27(a)), the steady state waveforms of the AIDF(a)'s state variables are shown in the Figure 2.29. As can be seen, the waveforms are very similar to the waveforms of the AIDBB. Thus, it may be said that the AIDF-group of converters has the same characteristics as all the asymmetrical interleaved converters studied in this chapter, that is, low ripple in output voltage and input current, a current distribution that occurs without any specific control strategy and two different modes of operation, depending on the duty cycle, with a frontier at $D=38\,\%$.

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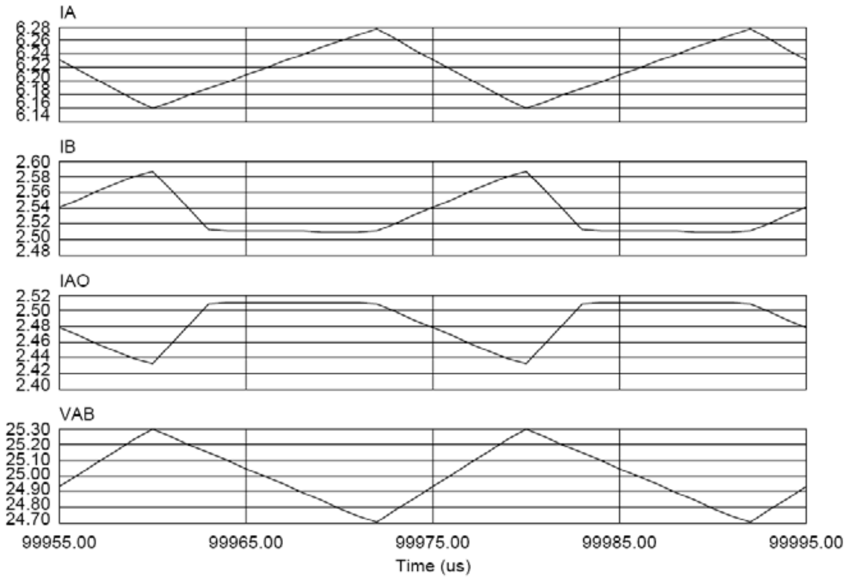

Figure 2.29: Steady state waveforms of the negative output voltage AIDF converter

The converters in this new group have many possible applications because they have a wide range of conversion ratios and isolation possibilities that can be reached with the use of transformers.

2.5.2.3 TOPOLOGIES OF THE AIDF-GROUP

The operation topologies of the AIDF-group differ from those of the AIDB and the AIDBB families because they include flyback transformers.

In any case, when determining the different topologies of all the structures in the AIDF-group , the conduction states of the MOSFETs and diodes were taken into account.

The operation intervals were defined in the same way as they were for the AIDB. The states of the switches in the four topologies are defined as:

- Topology 1 (S_B y D_A ON, S_A y D_B OFF). Interval 1: $d'=d_1$.
- Topology 2 (S_A y D_B ON, S_B y D_A OFF). Interval 2: d_2.
- Topology 3 (S_A ON, S_B, D_A y D_B OFF) where D_B is in DCM. Interval 3: d_3.

The two different modes of operation for this system defined the three topologies that are possible in every mode, depending on the duty cycle. For duty cycles greater than $38\,\%$, the circuit goes through the three topologies in every corresponding interval (d_1T, d_2T and d_3T) and for duty cycles less than $38\,\%$ the circuit goes through the first and second topologies as well as a fourth topology that is not included here.

2.5.2.3.1 TOPOLOGIES OF THE POSITIVE OUTPUT AIDF

A comparison of Figures 2.30 and 2.31 shows that the topologies are almost the same, the only difference is the direction of some currents and voltages.

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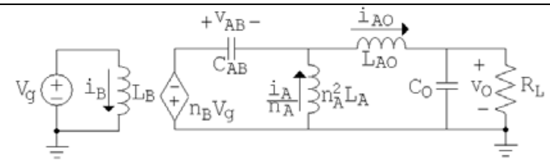
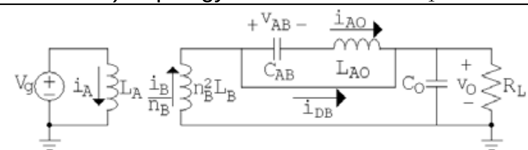
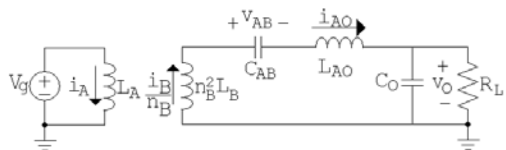


a) Topology 1. Interval 1: $d'=d_1$.



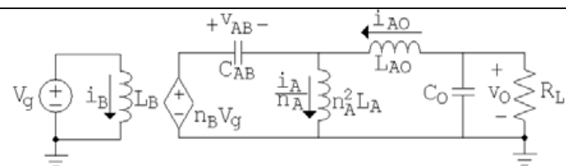
b) Topology 2. Interval 2: d_2.



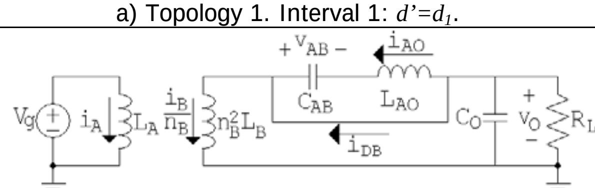
c) Topology 3. Interval 3: d_3.

Figure 2.30: Topologies of the AIDF of positive output converter in each operation interval

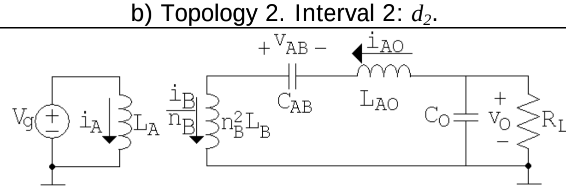
2.5.2.3.2 TOPOLOGIES OF THE NEGATIVE OUTPUT AIDF



a) Topology 1. Interval 1: $d'=d_1$.



b) Topology 2. Interval 2: d_2.



c) Topology 3. Interval 3: d_3.

Figure 2.31: Topologies of the AIDF of negative output converter in each operation interval

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2.5.2.3.3 TOPOLOGIES OF THE OTHERS CONVERTERS OF THE AIDF-GROUP

The topologies of the structures with a floating load in Figures 2.27(c) and 2.27(d) are very similar to the topologies that can be seen in Figures 2.30 and 2.31 respectively. The only difference is the interconnection between the load and the input voltage (see Figure 2.32).

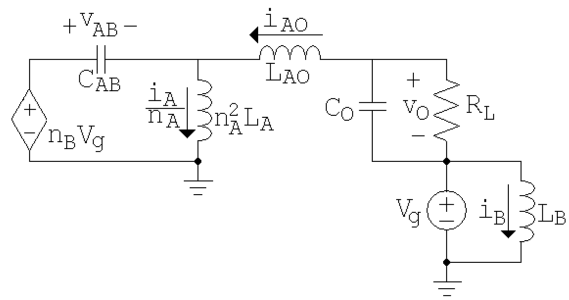

Figure 2.32: Topology 1 of the AIDF (c) of Figure 2.27

Almost the same thing occurs with the topologies of the structures in Figures 2.27(e) and 2.27(f). The difference is that the input voltage is connected to the secondary sides of the flyback transformers (see Figure 2.33).

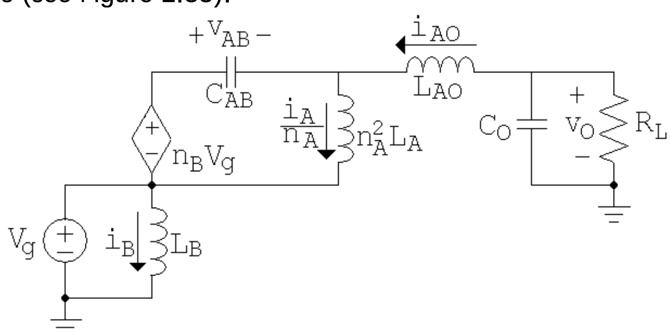

Figure 2.33: Topology 1 of the AIDF (e) of Figure 2.27

2.5.2.4 FIRST APPROXIMATION TO THE AIDF-GROUP OPERATING POINT

The expressions for the variables in steady state were obtained for the AIDF with negative output voltage (Figure 2.27(a)) so they could be compared with the expressions for the AIDBB. The methodology used was the same as that described in 2.4.3 for the AIDB.

2.5.2.4.1 MEAN VALUES OF THE CAPACITOR VOLTAGES IN STEADY STATE

The permanent loop of the AIDF in Figure 2.27(a) is also formed by the inductors L_B and L_{AO}, and the capacitors C_{AB} and C_O. Equation (44) is obtained from this loop:

$$V_{AB} = V_O \qquad (44)$$

From the steady state waveform of i_A, the following equality can be obtained

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$$\frac{V_{AB}+n_B V_g}{n_A L_A} D'T = -\frac{V_g}{L_A} DT \tag{45}$$

Operating on (45), the expression for the steady state mean value of the intermediate capacitor voltage V_{AB} and the mean value of the output voltage (44) is

$$V_{AB} = V_O = -\frac{V_g}{D'}\left(n_A D + n_B D'\right) \tag{46}$$

If $n_A = n_B = n$, the output voltage will be

$$V_O = -\frac{V_g n}{D'} \tag{47}$$

2.5.2.4.2 Mean values of the inductor currents in steady state

The steady state waveform of v_{AB} gives

$$\frac{I_{AO} - \dfrac{I_A}{n_A}}{C_{AB}} D'T = -\frac{I_{AO}}{C_{AB}} DT \tag{48}$$

Operating on (48), the expression for the steady state mean value of the I_A inductor current is

$$I_A = \frac{I_{AO} n_A}{D'} \tag{49}$$

Using the steady state waveform of v_O, the following expression can be calculated

$$-\frac{I_{AO} + \dfrac{V_O}{R}}{C_O} D'T = \frac{\dfrac{I_B}{n_B} + \dfrac{V_O}{R}}{C_O} DT \tag{50}$$

The simplification of (50) is

$$I_{AO} \cdot D' + \frac{I_B}{n_B} \cdot D = -\frac{V_O}{R} \tag{51}$$

If the currents i_B and i_{AO} are equal in the third interval, then the equation in (50) can be rewritten

$$-\frac{I_{AO} + \dfrac{V_O}{R}}{C_O} D_1 T = \frac{\dfrac{I_B}{n_B} + \dfrac{V_O}{R}}{C_O} D_2 T + \frac{I_{AO} + \dfrac{V_O}{R}}{C_O} D_3 T \tag{52}$$

The substitution of (15) and (16) in Equation (52) yields

$$I_{AO}\left(1 - D'^2\right) + \frac{I_B}{n_B} \cdot D'^2 = -\frac{V_O}{R} \tag{53}$$

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From (51) and (53)

$$I_{AO} = \frac{I_B}{n_B} \tag{54}$$

The substitution of (54) in (51)

$$I_B = \frac{V_g n_B}{RD'}(n_A D + n_B D') \tag{55}$$

From (54)

$$I_{AO} = \frac{V_g}{RD'}(n_A D + n_B D') \tag{56}$$

Finally, from (49:

$$I_A = \frac{V_g n_A}{RD'^2}(n_A D + n_B D') \tag{57}$$

Then, the following is the summary of the equations for the mean values of the steady state variables of the AIDF with negative output, for duty cycles greater than *38 %*:

$$\begin{cases} I_A = \dfrac{V_g n_A}{RD'^2}(n_A D + n_B D') \\ I_B = \dfrac{V_g n_B}{RD'}(n_A D + n_B D') \\ I_{AO} = \dfrac{V_g}{RD'}(n_A D + n_B D') \\ V_{AB} = -\dfrac{V_g}{D'}(n_A D + n_B D') \\ V_O = -\dfrac{V_g}{D'}(n_A D + n_B D') \end{cases} \tag{58}$$

This calculation is a first approximation of the operating point, which will be improved by the methodology described in the third chapter. Following the same procedure described here, it is possible to obtain the expressions of the steady state variables for all the structures in the AIDF-group. Table 2.13 shows the expressions for the output voltage and input current of all the AIDF converters when $n_A=n_B=n$.

Table 2.13: Expressions of the steady state input current and output voltage for each AIDF converter of Figure 2.27

(a) $V_O = -\dfrac{V_g n}{D'}$ $\quad Ig = \dfrac{V_g n}{RD'}\left(\dfrac{n}{D'} + n - 1\right)$	(b) $V_O = \dfrac{V_g n}{D'}$ $\quad Ig = \dfrac{V_g n}{RD'}\left(\dfrac{n}{D'} + n - 1\right)$
(c) $V_O = -V_g\left(\dfrac{n}{D'} + 1\right)$ $\quad I_g = -\dfrac{V_g}{R}\left(\dfrac{n}{D'} + 1\right)^2$	(d) $V_O = V_g\left(\dfrac{n}{D'} - 1\right)$ $\quad I_g = \dfrac{V_g}{R}\left(\dfrac{n}{D'} - 1\right)^2$
(e) $V_O = V_g\left(-\dfrac{n}{D'} + 1\right)$ $\quad I_g = \dfrac{V_g}{R}\left(-\dfrac{n}{D'} + 1\right)^2$	(f) $V_O = V_g\left(\dfrac{n}{D'} + 1\right)$ $\quad I_g = \dfrac{V_g}{R}\left(\dfrac{n}{D'} + 1\right)^2$

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2.6 OPEN LOOP EXPERIMENTAL RESULTS IN TIME DOMAIN

A prototype of the AIDB converter was built in order to verify the accuracy of the results predicted by simulation and preliminary analysis.

In this prototype, some of the initial circuit elements had to be readjusted in accordance with what was possible in the laboratory, and the simulations had to be repeated for the new values so that they included parasitics of the real elements.

The results of the comparisons between the simulations and the experimental data will be shown in the following sections.

2.6.1 AIDB CIRCUIT PROTOTYPE

Figure 2.34 shows the AIDB circuit for the experimental testing. It shows the references of the MOSFET, diodes and driver that were used in to construct the circuit, and also shows the values of the elements and voltage sources.

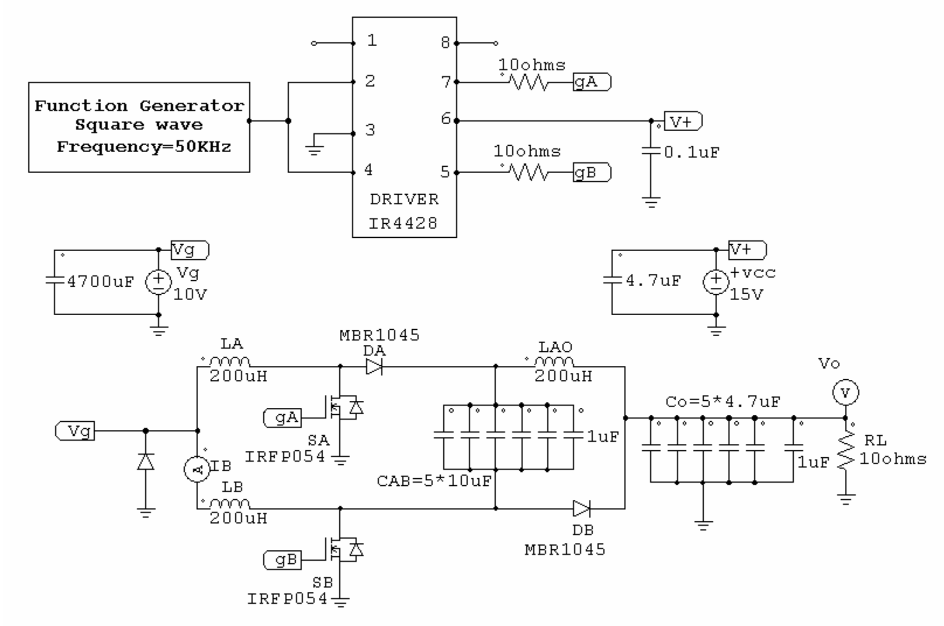

Figure 2.34: Schematic of the AIDB converter prototype

The values of the inductors L_A, L_B, and L_{AO} were changed from $1\ mH$ to $200\ \mu H$ because the first inductors were very large, although when making this change it was taken into account that the ripples of the input current continued to be low. The inductors were designed using the MAGNETICS Inductor Design Using Powder Cores Software. This software uses a design algorithm intended to specify the smallest design package size for the given input parameters (currents, inductance values, frequency, etc.). It also provides the values for the parasitics that will be used in the simulations of the circuit prototype.

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MMK technology capacitors were used because of their good characteristics. The maximum RMS current and peak current (ripple) that the capacitor could tolerate without breaking was also taken into account.

A parallel of five capacitors $10\ \mu F$ was used for the C_{AB} capacitor and a parallel of five $4.7\ \mu F$ capacitors was used for the C_O capacitor in order to diminish the parasitics associated with the capacitors.

The ceramic $1\ \mu F$ capacitor in parallel with the other capacitors reduces high frequency noise because its frequency response has a $1\ MHz$ attenuation peak. The capacitors in parallel with the sources remove line noise.

The value of the output capacitor is not very large. It thus allows the ripple and the testing behaviour of this circuit in open loop to be observed. This was necessary because this converter had never been assembled before.

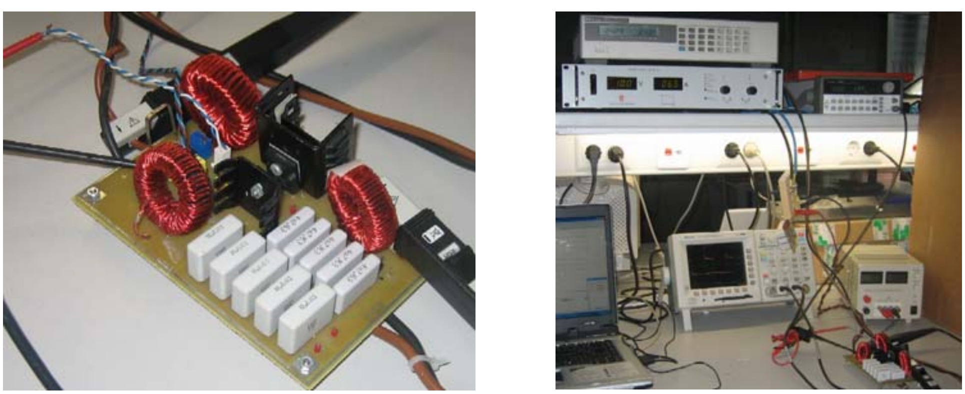
The MOSFET (IRFP054) and the diodes (MBR1045) were chosen on the basis of their maximum voltages, currents and power dissipation. The chosen MOSFET had to be very fast because is considered ideal at switching frequency, such as the only thing that should be modelled in the simulation is the R_{ON}.

The initial experimental measures show an oscillation due to a parasitic capacitance in the MOSFET SB. The value of this capacitance was taken from the MOSFET datasheets. This way, the oscillation could be also observed in PSIM simulations. This oscillation was eliminated by a RC-filter ($R=180\ \Omega$, $C=220\ nF$) in parallel with the MOSFET.

The IR4428 is a low side driver with a logic inverter that gives the complementary duty cycle for the MOSFET in the B-branch. A decouple capacitor of $100\ nF$ was used in the reference voltage of the chip.

In the open loop prototype, the duty cycles were controlled with a function generator and an active load was used.

Figure 2.35 shows two photographs with the AIDB converter prototype. The photograph on the left side clearly shows the experimental prototype of the AIDB circuit. The photograph on the right shows the interconnection between the prototype and the laboratory equipment, that is, the voltage sources, the function generator, the active load and the oscilloscope.



(a)AIDB Converter Prototype (b) Sources and measurement equipments

Figure 2.35: Photograph of the AIDB converter prototype and its interconnection with the sources and the measurement equipments

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2.6.2 PSIM SIMULATIONS OF THE AIDB CIRCUIT PROTOTYPE

Figure 2.36 shows the schematic used in simulations of the circuit prototype. The parasitics were taken into account in order to bring the simulations closer to the real measurements and to enable the comparisons.

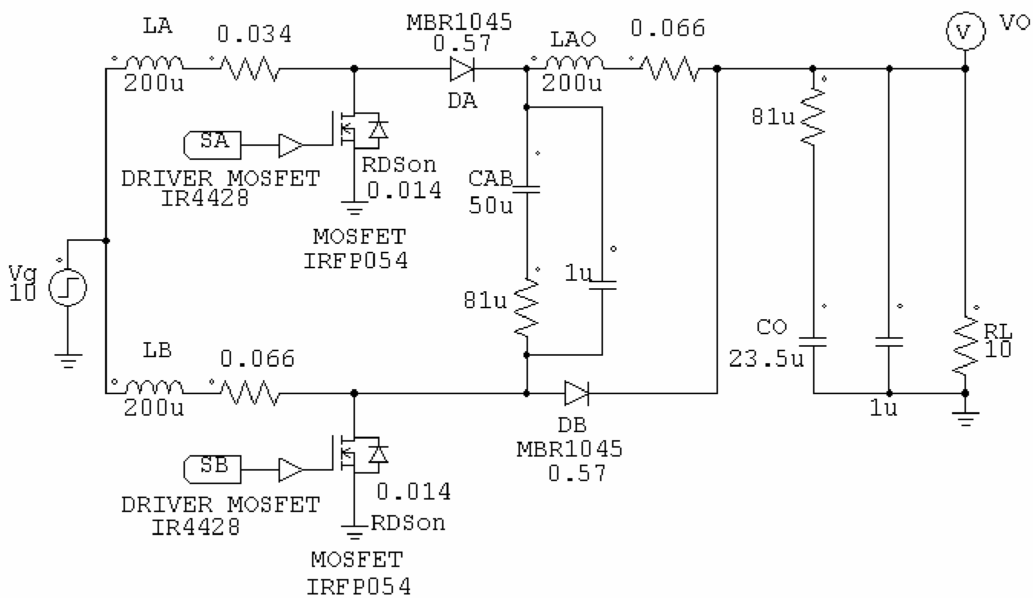

Figure 2.36: Simulation schematic of the AIDB converter circuit prototype

The inductors' parasitics were calculated using the MAGNETICS Inductor Design Using Powder Cores Software. The parasitics of the MOSFET and diodes were taken from the specifications sheets. The capacitors' parasitics were calculated using the quality factor equation (59) and the measurements made in the laboratory.

$$Q = \frac{2\pi f_c}{R} \qquad (59)$$

The simulation results, waveforms and tables that were obtained using the schematic of Figure 2.36 will be compared with the experimental results in the following section.

2.6.3 EXPERIMENTAL MEASUREMENTS, SIMULATIONS AND COMPARISONS

The following figures show the results of simulation versus experimental measurements so that the waveforms obtained can be visually compared. Measurements and simulations

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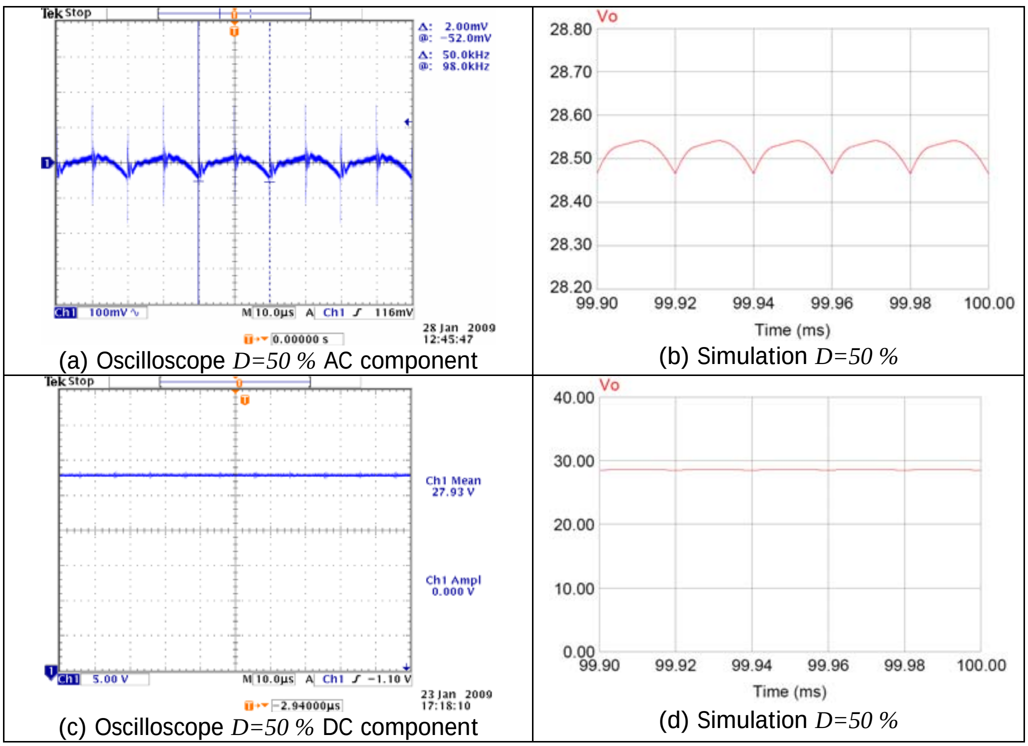
were performed for different values of the duty cycles, including the duty cycle of *38 %*, to check the two operation zones of the AIDB Converter.

In all the graphs that will be shown below, the experimental measurements are on the left side and the simulation results are on the right side. The simulations were made using PSIM.

2.6.3.1 Output Voltage Waveforms

Figures 2.37 and 2.38 show the waveforms of the output voltage obtained using two methods: experimental measurement and simulation with the PSIM.

Figure 2.37 shows the waveforms for a duty cycle of *50 %*, which is the reference duty cycle for the AIDB converter. Figure 2.38 explores the behaviour of the AIDB circuit with other duty cycles. Both figures show that the experimental results have reproduced the findings of the simulations.



(a) Oscilloscope *D=50 %* AC component
(b) Simulation *D=50 %*
(c) Oscilloscope *D=50 %* DC component
(d) Simulation *D=50 %*

Figure 2.37: Output voltage waveforms of the AIDB converter circuit prototype obtained by experimental testing and simulations for a duty cycle of *50 %*.

Figure 2.38 confirms the existence of the converter's two areas of operation, because the ripple is triangular for a duty cycle of *38 %*, whereas it is roughly parabolic for duty cycles greater than *38 %*. This second duty cycles operation area is of particular interest because of its reduction in ripples and its conversion ratios.

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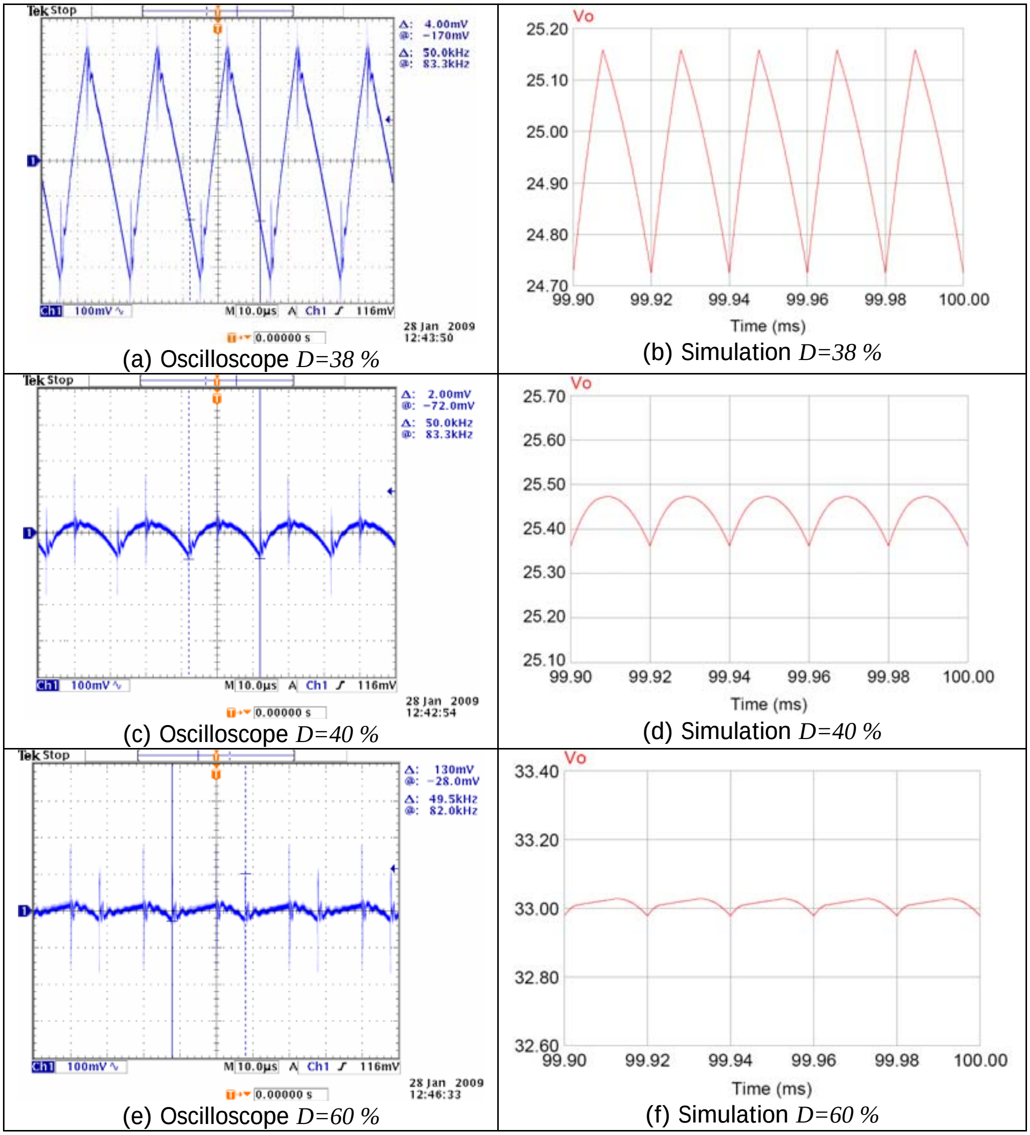
Table 2.14 shows the numerical results obtained from experimental testing and simulation. The experiment confirmed the good ripple results and mean output voltage values that were obtained from the simulations.

The reason for giving the numerical values in the tables is so that the simulations can compared with the experimental tests. The experimental measurements of the ripple only took into account the characteristic shape of the ripple, whereas the high frequency ripple spikes at the switching point were not considered.



(a) Oscilloscope $D=38\ \%$

(b) Simulation $D=38\ \%$

(c) Oscilloscope $D=40\ \%$

(d) Simulation $D=40\ \%$

(e) Oscilloscope $D=60\ \%$

(f) Simulation $D=60\ \%$

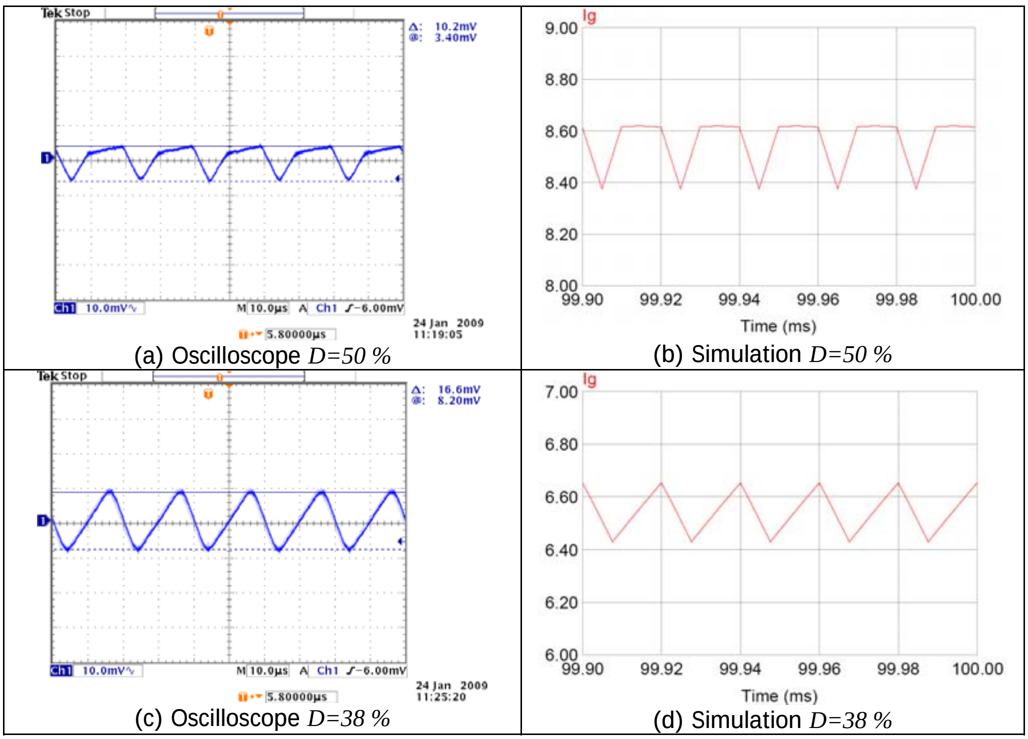
Figure 2.38: Output voltage waveforms of the AIDB converter circuit prototype obtained by experimental testing and simulations for duty cycles of *38 %* and *40 %*.

Table 2.14: Steady state mean values and ripples of the AIDB output voltage

	Experimental		Simulations	
D (%)	V_O (V)	Δv_O (V)	V_O (V)	Δv_O (V)
38	23.15	0.602	24.96	0.440
40	24.99	0.092	25.44	0.110
50	27.93	0.064	28.52	0.080
60	31.58	< 60 mV	33.01	0.050

2.6.3.2 INPUT CURRENT WAVEFORMS

Figure 2.39 shows that the input current has triangular ripples in the operation zone of duty cycles equal to or less than *38 %*, whereas it is trapezoidal in the operation zone of duty cycles greater than *38 %*.



(a) Oscilloscope D=50 %
(b) Simulation D=50 %
(c) Oscilloscope D=38 %
(d) Simulation D=38 %

Figure 2.39: Input current waveforms of the AIDB converter circuit prototype obtained by experimental testing and simulations for duty cycles of *38 %* and *50 %*.

2.6.3.3 DC VALUES OF INPUT AND OUTPUT CURRENTS

From Figure 2.40 was measured the average value of the input and output currents included in the Table 2.15. The table shows that the converter provides a very good input current ripple, because the ripple values measured were even lower than those obtained in the simulations, although the mean values were quite close to the simulation values.

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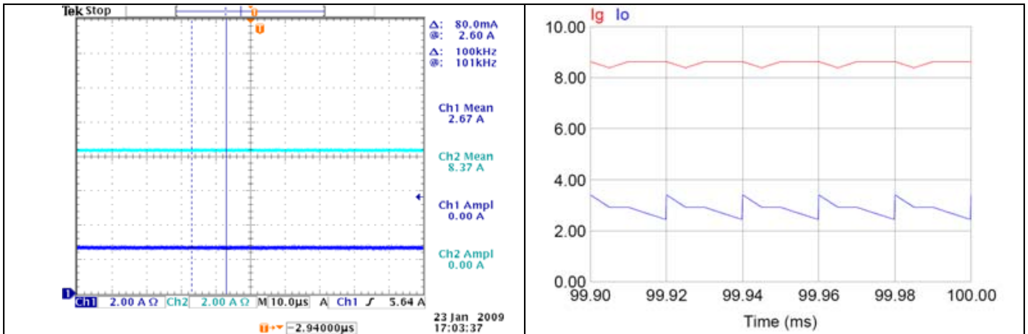

(a) Oscilloscope D=50 % DC component (b) Simulation D=50 %

Figure 2.40: Input and output currents of the AIDB converter circuit prototype obtained by experimental testing and simulations for a duty cycle of *50 %*.

Table 2.15: Steady state mean values and ripples of the AIDB input and output current

	Experimental		Simulations	
D (%)	I_g (A)	Δi_g (A)	I_g (A)	Δi_g (A)
38	6.24	0.166	6.54	0.220
50	8.37	0.102	8.50	0.230
D (%)	I_O (A)		I_O (A)	Δi_O (A)
50	2.67		2.85	0.97

2.6.3.4 Inductor Current Waveforms

The following figures show that the waveforms of the currents obtained by simulation match very well with those obtained experimentally. It is clear that the third operation interval is only found in the currents that are in DCM mode (I_{AO} and I_B). The currents for the duty cycle of reference can be seen in the Figure 2.41

The duty cycle limit of *38 %* is verified in the Figure 2.42, this is, the two modes of operation of the AIDB converter are also observed in the experimental data.

Figure 2.42 clearly shows that the DCM mode of operation starts in a duty cycle of *39 %* ((c) and (d)) and lasts longer in a duty cycle of *43 %* ((e) and (f)).

The numerical values show in Tables 2.16 and 2.17 verified that the experimental measurements follow the simulations results with reasonable accuracy, thus corroborating the information shown in the figures.

Table 2.16: Steady state mean values and ripples of the AIDB I_{AO} current

	Experimental		Simulations	
D (%)	I_{AO} (A)	Δi_{AO} (A)	I_{AO} (A)	Δi_{AO} (A)
38	1.271	0.580	1.64	0.600
39	2.315	0.548	2.30	0.590
43	2.435	0.540	2.45	0.560
50	2.650	0.480	2.73	0.490

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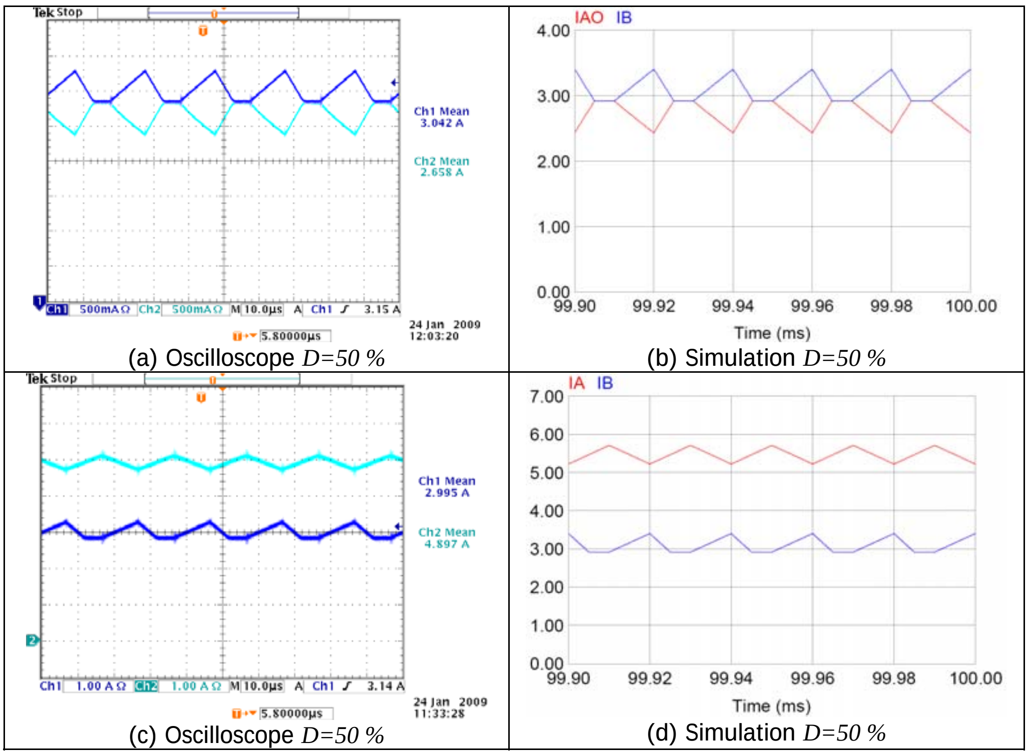
Table 2.17: Steady state mean values and ripples of the AIDB I_B current

	Experimental		Simulations	
D (%)	I_B (A)	Δi_B (A)	I_B (A)	Δi_B (A)
38	4.734	0.650	3.89	0.600
39	2.861	0.550	2.88	0.590
43	2.903	0.540	2.94	0.550
50	3.040	0.450	3.10	0.480



(a) Oscilloscope D=50 %
(b) Simulation D=50 %
(c) Oscilloscope D=50 %
(d) Simulation D=50 %

Figure 2.41: Inductor currents waveforms of the AIDB converter circuit prototype obtained by experimental testing and simulations for a duty cycle of *50 %*.

Figure 2.43 shows the unusual behaviour of currents I_A and I_B. Figures (a) and (b) show that current I_B is greater than current I_A for duty cycles of *38 %* or less because in these duty cycles I_A is in DCM mode. For duty cycles of *39 %*, I_A is greater than I_B but not by much, because the waveforms of the currents are in contact (c). In the simulations, this contact occurs for a duty cycle of *38.2 %*, as shown in (d). In (e) and (f), current I_B is already in DCM for a duty cycle of *43 %*.

The numerical measurements for I_A current can be seen in Table 2.18.

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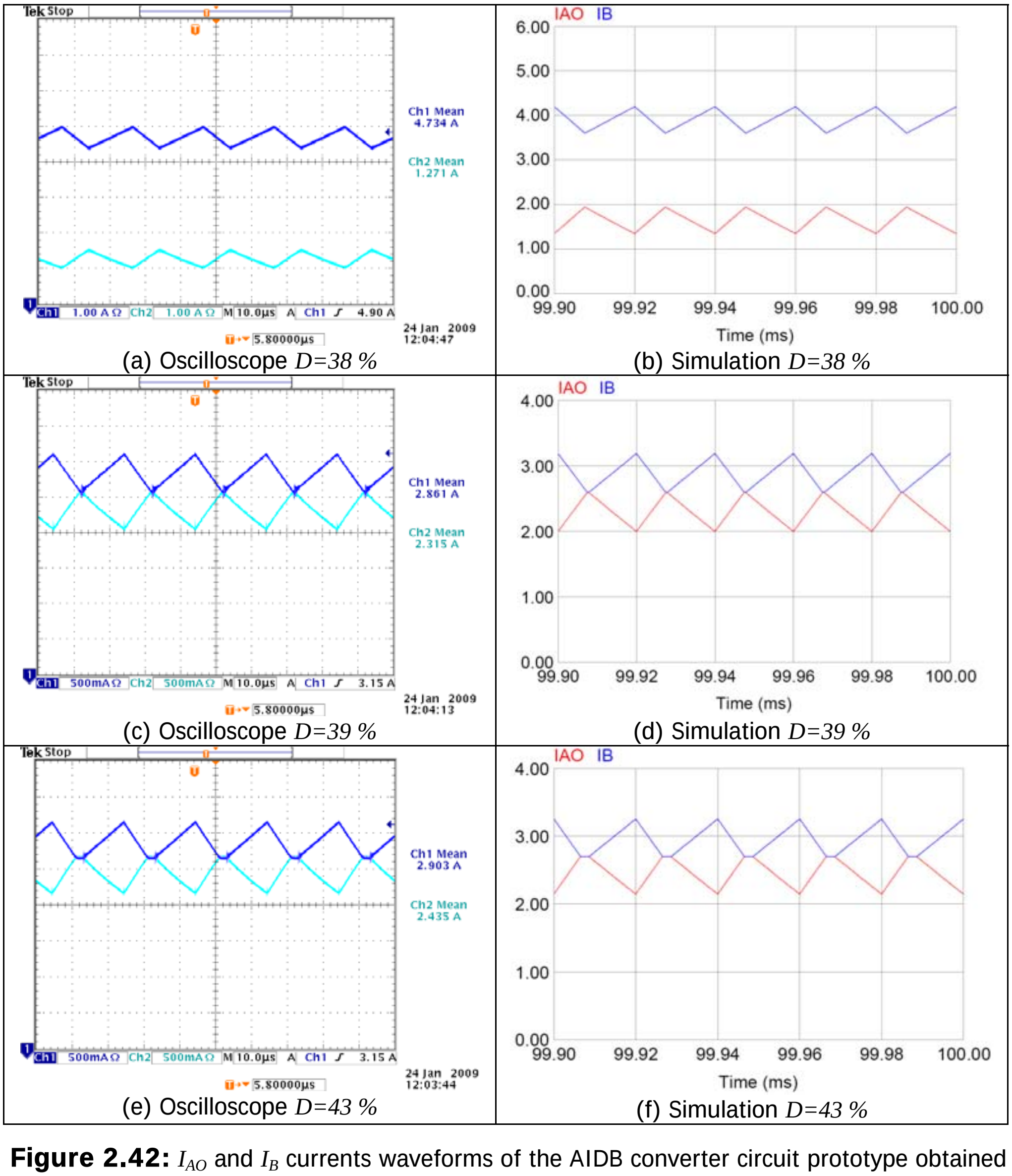
Table 2.18: Steady state mean values and ripples of the AIDB I_A current

	Experimental		Simulations	
D (%)	I_A (A)	Δi_A (A)	I_A (A)	Δi_A (A)
38	1.520	0.390	2.65	0.370
39	3.259	0.400	3.76	0.380
43	3.754	0.450	4.29	0.420
50	4.897	0.500	5.46	0.480



(a) Oscilloscope D=38 % (b) Simulation D=38 %
(c) Oscilloscope D=39 % (d) Simulation D=39 %
(e) Oscilloscope D=43 % (f) Simulation D=43 %

Figure 2.42: I_{AO} and I_B currents waveforms of the AIDB converter circuit prototype obtained by experimental testing and simulations for duty cycles of 38 %, 39 % and 43 %.

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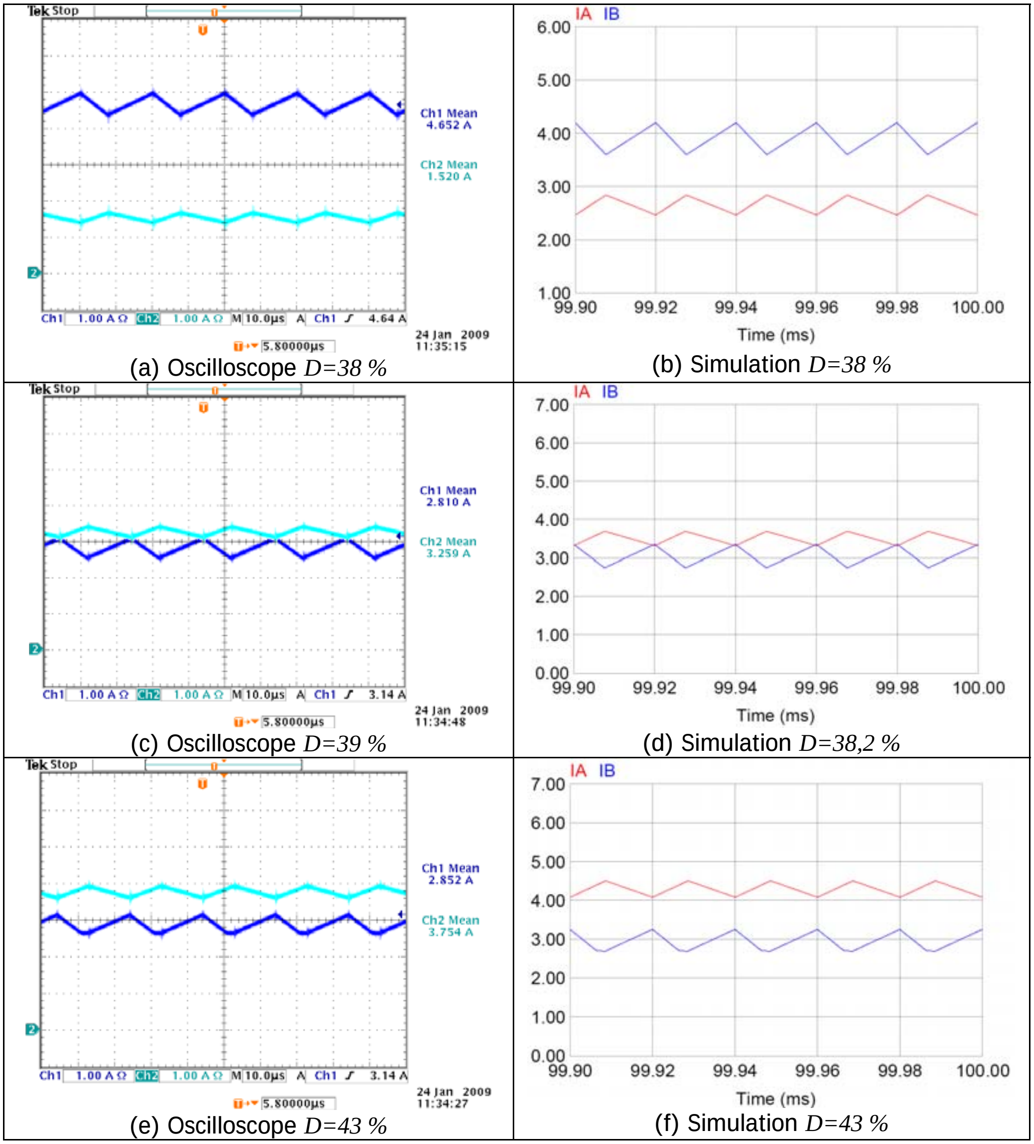

(a) Oscilloscope *D=38 %* (b) Simulation *D=38 %*
(c) Oscilloscope *D=39 %* (d) Simulation *D=38,2 %*
(e) Oscilloscope *D=43 %* (f) Simulation *D=43 %*

Figure 2.43: I_A and I_B currents waveforms of the AIDB converter circuit prototype obtained by experimental testing and simulations for duty cycles of *38 %*, *39 %* and *43 %*.

2.6.3.5 INTERMEDIATE CAPACITOR VOLTAGE WAVEFORMS

Table 2.19 shows the numerical values obtained for the intermediate voltage capacitor in a duty cycle of *50 %*.

The waveforms of this state variable can be seen in Figure 2.44. It can be concluded that the experimental results have reproduced the findings of the simulations.

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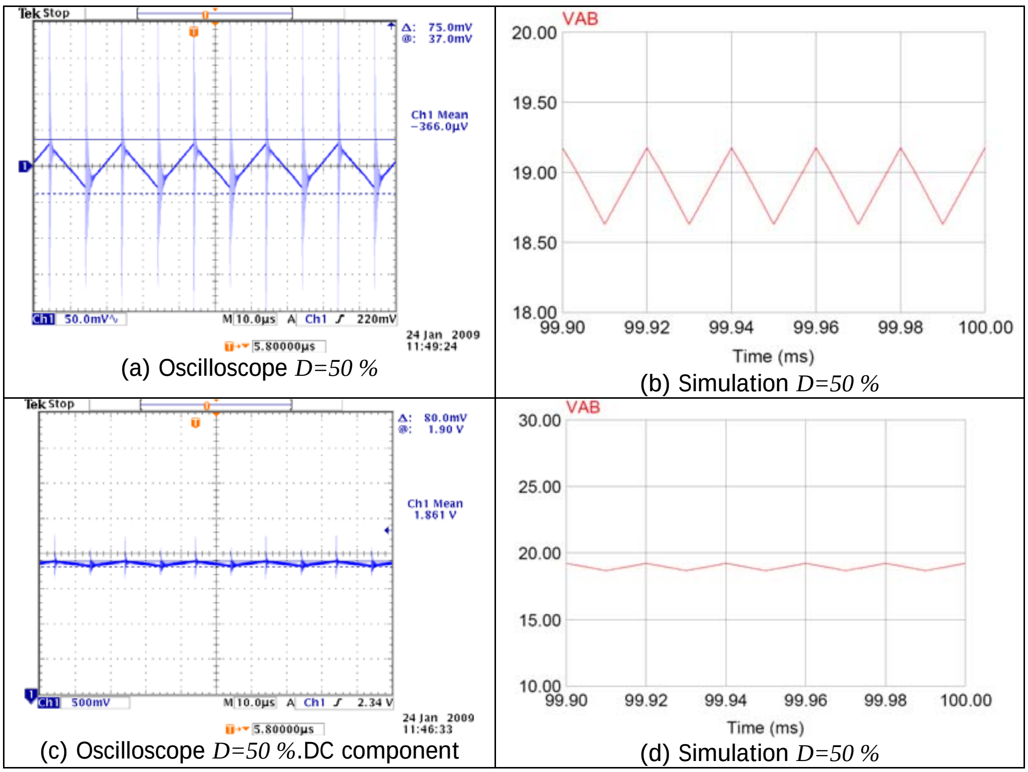
As with the output voltage, it is important to point out that only the characteristic shape of the ripple was taken into account when calculating the numerical values in the table, i.e. the ripple caused by commutation was not measured, because the aim was to compare the simulations and the experimental measurement of the ripple.

Table 2.19: Steady state mean values and ripples of the AIDB V_{AB} voltage

	Experimental		Simulations	
D (%)	V_{AB} (V)	Δv_{AB} (V)	V_{AB} (V)	Δv_{AB} (V)
50	18.61	0.750	18.9	0.540



(a) Oscilloscope D=50 %
(b) Simulation D=50 %
(c) Oscilloscope D=50 %.DC component
(d) Simulation D=50 %

Figure 2.44: VAB voltage waveforms of the AIDB converter circuit prototype obtained by experimental testing and simulations for a duty cycle of 50 %.

2.6.3.6 Comparative Graphics

The experimental and simulation data used for Figure 2.45 were measured for duty cycles from *39 %* to *66 %*.

It can be seen that the experimental data curves are very close to those of the simulation data, except in terms of efficiency. This can be explained by the difference between the losses during simulation and the actual losses.

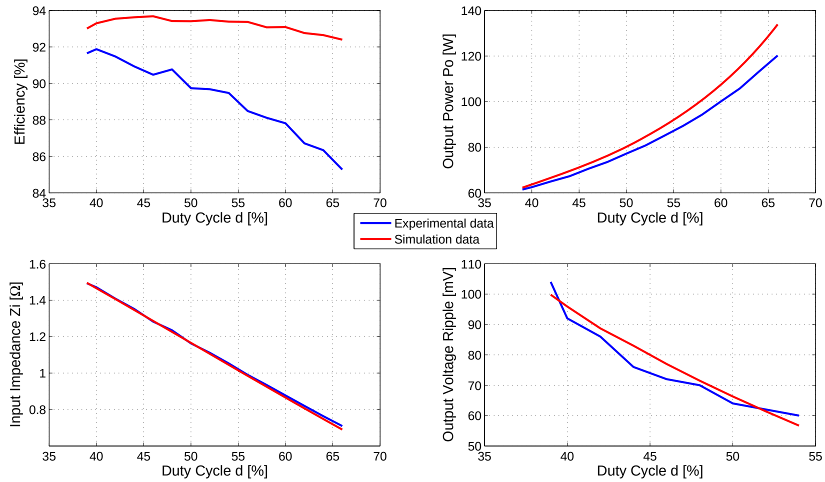


Figure 2.45: Comparative Graphics of Efficiency, Output Power, Input Impedance and Output Voltage Ripple, using the experimental and the simulation data of the AIDB Circuit Prototype.

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2.7 CHAPTER CONCLUSIONS

This chapter presents the family of asymmetrical interleaved converters. This family was developed from a concept established in previous theses [1, 2] and followed a methodology called circuit structure modification that is based on simulation results and on the fundamental idea of breaking the symmetry.

Breaking the symmetry allowed the generation of a new family of converters with very interesting characteristics. These were first seen in the simulations and later verified with the experimental prototype of the AIDB converter.

The first important characteristic of this converter family is that there are two different modes of operation depending on the duty cycle. For duty cycles greater than *38 %*, diode D_B operates in DCM, whereas for duty cycles lower than *38%*, diode D_A operates in DCM. This means that the circuit inherently operates in DCM. However, when diode D_A is in DCM the converter has large output ripple, which is not desired in practice. This operation in DCM causes the input current to be unevenly shared between the two branches of the circuit. and this occurs without any specific control strategy and reduces the aggregated input current ripple. Compared with other conventional interleaved converters, this characteristic of asymmetrical interleaved converters allows the regulation strategy to be simplified.

Other interesting characteristics of this family are that it has a low output voltage ripple which tends to zero as the duty cycle increases, and that the duration of the operation intervals in steady state does not include the parameters of the circuit. All of these features were verified by the experimental results obtained with the AIDB converter prototype.

The experimental measurements also confirmed that the converter has two areas of operation, that is, they revealed the differences between the shapes and values of the waveforms for a duty cycle of *38 %* and the waveforms for duty cycles greater than *38 %*. The numerical results obtained by experimental testing and simulation allowed the verification of the good ripple results and mean values of the converter variables.

It should be pointed out that asymmetrical interleaved converters have interesting characteristics regarding to their transfer ratio: the AIDB converter offers a considerably improved input-to-output voltage transfer ratio, the AIDBB converter can also have a negative output, and the AIDF family has a wide range of conversion ratios that can be reached with the use of transformers.

The initial theoretical calculations for the AIDB, the AIDBB and the AIDF family were made using the averaging assumptions. The numerical tables demonstrated that the expressions obtained for the AIDB contain relative errors compared with those obtained through PSIM simulation. These relative errors may occur when estimating the averages. It is assumed that the average value of the currents in one of the intervals coincides with the average value throughout the period, without taking into account that two currents have three different slopes. An improvement in these results will be presented in the following chapter which will discuss the analysis and modelling of the family of AIDB converters.

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CHAPTER 3

ASYMMETRICAL INTERLEAVED DC TO DC SWITCHING CONVERTERS CIRCUITS: MODELLING

In the previous chapter, the new AIDB converter was simulated determine its operating characteristics, which were then verified using an experimental prototype.

These features were very interesting because AIDB generally offered low ripple and a wide range of conversion. In addition, the control technique was relatively simple to design because the input current is inherently distributed between the two branches, without any specific control strategy. Consequently, this converter has a large range of possible applications. It was decided to continue with the mathematical analysis of the AIDB because of the advantages it displayed. This revealed the analytical expressions that govern it so that they could be used to design the controller (see following chapter).

Modelling the AIDB is complicated because of its inherent DCM mode of operation; AIDB always has a branch in DCM, meaning that the conventional averaging modelling methods do not work properly to find out which equations govern it. Therefore, a modelling method had to be found that allowed the circuit to be theoretically analyzed.

As a result of this, a new conceptual approach, inspired by ideas from some of the papers analyzed in the state of the art, was used to arrive at the averaged model and at the other analytical equations for the AIDB. This approach will be explained in detail in this chapter.

The mathematical program MAPLE has been used for all the mathematical calculations that are presented in this chapter.

3.1 AIDB ANALYSIS

The discontinuous conduction mode, in which the AIDB converter works, limits the modelling possibilities to methods that can be applied to the DCM mode.

According to the literature review in Chapter One, the DCM modelling method that offers the best approximation is “the revised averaging method” that was presented in [1]. This paper shows that, before the revised averaging, all the DCM modelling methods permit the generation of reduced order or complete order models. However, these DCM modelling methods do not provide as good an approximation as the simulation results of the revised averaging method because they provide an inexact approximation of the high-frequency poles. For this reason, it was immediately decided that the methodology developed in [1] should be used to provide a full order model.

3.1.1 AIDB MODELLING USING THE REVISED AVERAGING METHOD

As was explained in Chapter One, the revised averaging modelling method, explained in [1] and employed for DCM operation, consists of three steps: Averaging, Correction, and Duty-ratio constraint definition.

First, conventional state space averaging was applied, followed by correction. This correction consists of dividing all the inductor currents in the converter by the factor $(d1+d2)$, because these are the two duty ratios in which the inductors are conducting. In order to apply this operation to the state space averaging, a diagonal matrix $\boldsymbol{M}$ must first be defined. This matrix is then used to multiply the average matrix A in the state space averaging.

This correction must be made because in DCM, the inductor currents (or, depending on the specific mode, the variables in DCM, as explained in Chapter One) have three intervals instead of the two intervals when the converter operates in CCM. Therefore, the averaging procedure, as carried out in previous averaging methods, is not correct.

3.1.1.1 AVERAGING AND CORRECTION APPLIED TO THE AIDB CONVERTER

This correction cannot be directly applied to the AIDB because, as shown in the simulations in Chapter One, there are two inductor currents with three intervals (i_B and i_{AO}) and one inductor current with two intervals (i_A) in the duty cycles of interest ($D>38\%$). Therefore, in the AIDB it is only necessary to apply this correction to the equations for the two currents with three intervals because the averaging is already correct in the other current.

3.1.1.1.1 TOPOLOGIES AND EQUATIONS

The topologies (which have already been shown in Chapter Two) are included here again in order to bring greater clarity to the calculations. However, in this case, only the first three topologies exhibited by the AIDB for the duty cycles of interest have been taken into account ($D> 38\%$).

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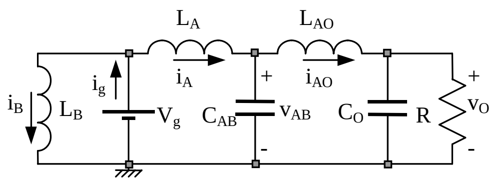
Figure 3.1 shows the topologies and each of their equations. The states of the switches in every topology and interval are defined:

- Topology 1 (S_B y D_A ON, S_A y D_B OFF). Interval 1: $d'=d_1$.
- Topology 2 (S_A y D_B ON, S_B y D_A OFF). Interval 2: d_2.
- Topology 3 (S_A ON, S_B, D_A y D_B OFF) where D_B is in DCM. Interval 3: d_3.

According to the definition of intervals in the second chapter:

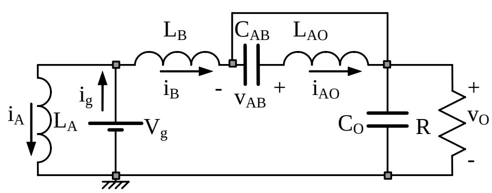
$$d_1 + d_2 + d_3 = 1 \tag{1}$$

$$d_1 = d'; \quad d_2 + d_3 = d \tag{2}$$



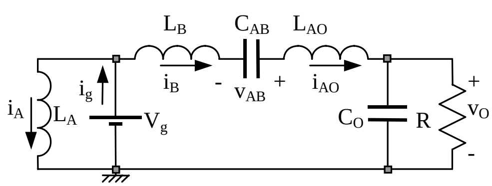
a) Topology 1. Interval 1: $d'=d_1$

$$\begin{aligned} L_A \frac{d\,i_A}{dt} &= v_g - v_{AB} \\ L_B \frac{d\,i_B}{dt} &= v_g \\ L_{AO} \frac{d\,i_{AO}}{dt} &= v_{AB} - v_O \\ C_{AB} \frac{d\,v_{AB}}{dt} &= i_A - i_{AO} \\ C_O \frac{d\,v_O}{dt} &= i_{AO} - \frac{v_O}{R} \end{aligned} \tag{3}$$



b) Topology 2. Interval 2: d_2

$$\begin{aligned} L_A \frac{d\,i_A}{dt} &= v_g \\ L_B \frac{d\,i_B}{dt} &= v_g - v_O \\ L_{AO} \frac{d\,i_{AO}}{dt} &= v_{AB} \\ C_{AB} \frac{d\,v_{AB}}{dt} &= -i_{AO} \\ C_O \frac{d\,v_O}{dt} &= i_B - \frac{v_O}{R} \end{aligned} \tag{4}$$



c) Topology 3. Interval 3 (DCM): d_3

$$\begin{aligned} L_A \frac{d\,i_A}{dt} &= v_g \\ (L_B + L_{AO}) \frac{d\,i_B}{dt} &= v_g + v_{AB} - v_O \\ i_{AO} &= i_B \quad * \\ C_{AB} \frac{d\,v_{AB}}{dt} &= -i_{AO} \\ C_O \frac{d\,v_O}{dt} &= i_{AO} - \frac{v_O}{R} \end{aligned} \tag{5}$$

Figure 3.1: Topologies and equations of the AIDB converter for $d > 38\,\%$.

The equation of the third interval marked with an asterisk (∗) reflects the reduction of order that occurs in the discontinuous mode and makes more difficult the averaging calculations in the state space, because the equality of the variables imposes a stronger restriction than the equality of the derivatives of the variables.

3.1.1.1.2 CONVENTIONAL AVERAGING

In the next step, the equations are obtained using conventional averaging, that is, by adding the products of the topology equations and their corresponding intervals. The state space averaged system (*D>38%*) is

$$\begin{aligned}
\frac{d\,\bar{i}_A}{dt} &= \frac{v_g - \bar{v}_{AB} d_1}{L_A} \\
\frac{d\,\bar{i}_B}{dt} &= \frac{v_g}{L_B}(d_1 + d_2) - \frac{\bar{v}_O}{L_B} d_2 + \frac{v_g - \bar{v}_O + \bar{v}_{AB}}{L_B + L_{AO}} d_3 \\
\frac{d\,\bar{i}_{AO}}{dt} &= \frac{\bar{v}_{AB}}{L_{AO}}(d_1 + d_2) - \frac{\bar{v}_O}{L_{AO}} d_1 + \frac{v_g - \bar{v}_O + \bar{v}_{AB}}{L_B + L_{AO}} d_3 \\
\frac{d\,\bar{v}_{AB}}{dt} &= \frac{\bar{i}_A d_1 - \bar{i}_{AO}}{C_{AB}} \\
\frac{d\,\bar{v}_O}{dt} &= \frac{\bar{i}_{AO}}{C_O} - \frac{\bar{v}_O}{RC_O}
\end{aligned} \tag{6}$$

3.1.1.1.3 CORRECTION

After averaging, the correction described in 3.1.1 can be applied. For the AIDB converter analysis, it is only necessary to apply this correction to the equations for the two currents with three intervals because the averaging is already correct in the other current. Consequently, it is not necessary to multiply the equations of all the currents by the matrix M [1]; instead, it is enough if the averaging equations of the two currents i_B and i_{AO} are divided by the factor $(d1+d2)$, as can be seen in the following

$$\begin{aligned}
\frac{d\,\bar{i}_A}{dt} &= \frac{v_g - \bar{v}_{AB} d_1}{L_A} \\
\frac{d\,\bar{i}_B}{dt} &= \frac{1}{d_1 + d_2}\left[\frac{v_g}{L_B}(d_1 + d_2) - \frac{\bar{v}_O}{L_B} d_2 + \frac{v_g - \bar{v}_O + \bar{v}_{AB}}{L_B + L_{AO}} d_3\right] \\
\frac{d\,\bar{i}_{AO}}{dt} &= \frac{1}{d_1 + d_2}\left[\frac{\bar{v}_{AB}}{L_{AO}}(d_1 + d_2) - \frac{\bar{v}_O}{L_{AO}} d_1 + \frac{v_g - \bar{v}_O + \bar{v}_{AB}}{L_B + L_{AO}} d_3\right] \\
\frac{d\,\bar{v}_{AB}}{dt} &= \frac{\bar{i}_A d_1 - \bar{i}_{AO}}{C_{AB}} \\
\frac{d\,\bar{v}_O}{dt} &= \frac{\bar{i}_{AO}}{C_O} - \frac{\bar{v}_O}{RC_O}
\end{aligned} \tag{7}$$

3.1.1.2 DUTY-RATIO CONSTRAINT APPLIED TO THE AIDB CONVERTER

The second step of [1] implies that once the averaged model has been calculated, the duty cycle d_2 has to be replaced by an expression depending on other variables of the circuit;

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this expression should be consistent with the correction made in the averaging of the currents. This expression was obtained in [1] by using the average obtained from the waveform of the converter current and calculating the peak inductor current directly from the topology equations. Equation (8) shows the expression obtained in the paper, where $\bar{i}_L$ is the average value of the current in DCM and v_{on} is the voltage across the inductor when the switch is *ON* (during $[0, d_1T]$).

$$d_2 = \frac{2L\bar{i}_L}{d_1 T v_{on}} - d_1 \tag{8}$$

To obtain the equation for the duty ratio constraint in the AIDB, it should be taken into account that there are two currents in DCM and that it must be possible to define d_2 for the two currents.

For i_B

$$d_2 = \frac{2L_B\bar{i}_B}{d_1 T v_g} - d_1 \tag{9}$$

For i_{AO}

$$d_2 = \frac{2L_{AO}\bar{i}_{AO}}{d_1 T\left(\bar{v}_O - \bar{v}_{AB}\right)} - d_1 \tag{10}$$

The substitution of the equations obtained for d_2 (9 and 10) in (7) does not provide a solution for the system state equations neither the point of operation ($D = 50\%$) nor the location of the poles and zeros of the system. Because, when (9) is replaced in (7), an operating point is obtained that does not match the simulation results of the previous chapter, in which i_B has a value close to zero and in which there are RHP poles that make this model unstable and behave totally differently from the plant. In addition, by replacing (10) in (7), the situation worsens because the variable i_B does not appear in the equations and it is impossible to obtain a solution for the system.

Therefore, it became necessary to explore another way to get d_2 that was consistent with the corrected average described in the "the revised averaging method" [1].

3.1.1.3 NEW METHOD FOR CALCULATING THE SECOND DUTY CYCLE

Consequently, it was decided to explore the graphics obtained from the simulation of the AIDB converter in order to determine the relationships between variables and thus provide a solution to the problem of finding an expression for d_2.

The graph of the waveforms for currents in DCM allows some interesting deductions and makes it very easy to obtain the expression for the second duty cycle d_2 directly from the waveforms. This figure has already been presented in Chapter Two and is repeated here because it is needed to work out the following method.

As in [1], the averages for the converter currents can be calculated using the areas of the triangles in the waveforms in Figure 3.2, as can be seen in the following equations [2-4].

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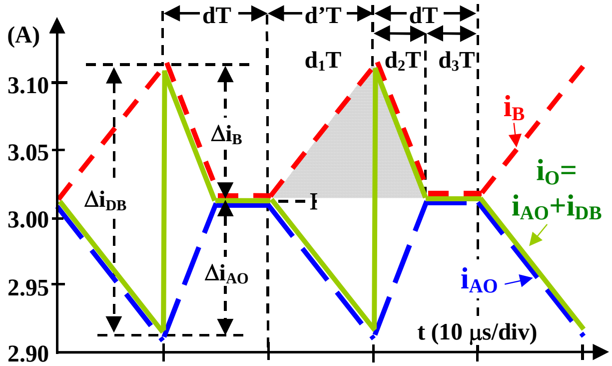

Figure 3.2: DCM currents in the AIDB converters and definition of the relative duration of the three operation intervals (d_1, d_2 and d_3)

The area of the upper triangle is

$$\frac{\Delta i_B}{2}(d_1 T + d_2 T) \tag{11}$$

therefore, the mean value of the i_B current

$$\bar{i}_B = I + \frac{\Delta i_B}{2}(d_1 + d_2) \tag{12}$$

In the same way, the area of the lower triangle is

$$\frac{\Delta i_{AO}}{2}(d_1 T + d_2 T) \tag{13}$$

consequently, the mean value of the i_{AO} current is

$$\bar{i}_{AO} = I - \frac{\Delta i_{AO}}{2}(d_1 + d_2) \tag{14}$$

Now, the equations for the Δi_B and Δi_{AO} can be obtained from the corresponding equations of the first topology (3) taking into account the peak current.

$$\Delta i_B = \frac{v_g}{L_B} d_1 T; \quad \Delta i_{AO} = \frac{\bar{v}_O - \bar{v}_{AB}}{L_{AO}} d_1 T \tag{15}$$

Then, the expression for d_2 is obtained by subtracting the equations (12) and (14), and replacing Δi_B and Δi_{AO} by the expressions of the equation (15). The result is

$$d_2 = \frac{2(\bar{i}_B - \bar{i}_{AO})}{\left(\frac{v_g}{L_B} + \frac{\bar{v}_O - \bar{v}_{AB}}{L_{AO}}\right) d_1 T} - d_1 \tag{16}$$

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3.1.1.4 SSA FOR THE AIDB USING THE REVISED AVERAGING

Replacing the equations (1) and (16) in (7), it is possible to obtain the state space averaged system, for $D>38\%$, in terms of the duty cycle d_1.

$$
\begin{aligned}
\frac{d\bar{i}_A}{dt} &= \frac{v_g - \bar{v}_{AB} d_1}{L_A} \\
\frac{d\bar{i}_B}{dt} &= \frac{2\bar{i}_B L_B L_{AO}^2 (a_1) + 2\bar{i}_{AO} L_B L_{AO}^2 (a_2) + \bar{v}_{AB} d_1 T L_B^2 (a_3) + \bar{v}_O d_1 T L_B L_{AO} (a_4) + d_1 T V_g (a_5)}{2 L_{AO} L_B^2 (L_{AO} + L_B)(-\bar{i}_B + \bar{i}_{AO})} \\
\frac{d\bar{i}_{AO}}{dt} &= \frac{2(\bar{i}_{AO} - \bar{i}_B) L_B L_{AO} (a_6) + d_1 T V_g L_{AO}^2 (a_7) + \bar{v}_O d_1^2 T L_B (a_8) + d_1 T L_{AO} L_B (a_9)}{2 L_{AO}^2 L_B (L_{AO} + L_B)(-\bar{i}_B + \bar{i}_{AO})} \\
\frac{d\bar{v}_{AB}}{dt} &= \frac{\bar{i}_A d_1 - \bar{i}_{AO}}{C_{AB}} \\
\frac{d\bar{v}_O}{dt} &= \frac{\bar{i}_{AO}}{C_O} - \frac{\bar{v}_O}{R C_O}
\end{aligned}
\qquad (17)
$$

where

$$a_1 = -V_g + \bar{v}_O + \bar{v}_{AB} \qquad a_2 = V_g - \bar{v}_O - \bar{v}_{AB} \qquad a_3 = V_g + \bar{v}_{AB} + \bar{v}_O d_1 - 2\bar{v}_O$$

$$a_4 = V_g - d_1 V_g + d_1 \bar{v}_{AB} - \bar{v}_O \qquad a_5 = (-V_g - \bar{v}_{AB}) L_B L_{AO} - \bar{v}_O L_B^2 - \bar{v}_O d_1 L_{AO}^2$$

$$a_6 = (-V_g + \bar{v}_O) L_{AO} + \bar{v}_{AB} L_B \qquad a_7 = -V_g + \bar{v}_O (d_1 + 1) - \bar{v}_{AB} \qquad a_8 = -\bar{v}_{AB} + \bar{v}_O$$

$$a_9 = d_1 \bar{v}_O (V_g - \bar{v}_{AB}) + V_g (\bar{v}_{AB} - \bar{v}_O) - 2\bar{v}_{AB}\bar{v}_O + \bar{v}_{AB}^2 + \bar{v}_O^2$$

This system was obtained not only by following the steps in the revised averaging method but also by using the new method to calculate the second duty cycle.

It can be observed that $d_1=d'$ has been chosen as the control input for obtaining the model of the converter because of the simplicity of its the equations, although this is not the convention.

3.1.1.4.1 OPERATING POINT

Let us assume that the state variables and the control variables can be expressed as the sum of their steady state and small signal components, as follows:

$$\dot{\bar{x}} = \dot{\hat{x}}; \quad \bar{x} = X + \hat{x}; \quad v_g = V_g + \hat{v}_g \qquad (18)$$

$$d_1 = d' = 1 - d = 1 - D - \hat{d} = D' - \hat{d} = D' + \hat{d}_1 \qquad (19)$$

The operating point can be obtained by solving the system equations, which can generally be expressed as:

$$0 = f(X, D') \qquad (20)$$

The expressions for the operating point obtained using the revised averaging method can be seen in (21).

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A comparison with the equations in (26) in Chapter Two shows that this method has corrected the expression for the mean value of the current I_B, despite it being said in Chapter Two that an approach needed to be found to improve the approximation of the expressions for the three currents and thus reduce the relative errors associated with them.

$$\begin{cases} I_A = \dfrac{1}{D'}\left(1+\dfrac{1}{D'}\right)\dfrac{V_g}{R} \\ I_B = \left(1+\dfrac{1}{D'}\right)\dfrac{V_g}{R} + \dfrac{V_g T}{2}\dfrac{(L_{AO}+L_B)}{L_{AO}\cdot L_B}D'^2(1+D') \\ I_{AO} = \left(1+\dfrac{1}{D'}\right)\dfrac{V_g}{R} \\ V_{AB} = \dfrac{V_g}{D'} \\ V_O = \left(1+\dfrac{1}{D'}\right)V_g \end{cases} \tag{21}$$

In order to verify the approximation of the new expression for the I_B current, a comparative table has been made using the numerical values of the simulations of the AIDB converter in section 2.4. These are: $V_g=10\ V$, $L_A=L_B=L_{AO}=1\ mH$, $C_{AB}=\ 50\ \mu F$, $C_O=20\ \mu F$, $R_L=10\ \Omega$, $T=20\ \mu s$ and a duty cycle from *40 %* to *90 %* with steps of *10 %*.

Table 3.1: Mean value and relative error of I_B using the expression of (21)

D	I_B *(21)*	I_B *PSIM*	*Relative error*
0.4	2.78	2.74	-1.53
0.5	3.08	3.05	-0.82
0.6	3.54	3.53	-0.42
0.7	4.36	4.35	-0.15
0.8	6.01	6.01	0.01
0.9	11.00	11.00	-0.02

(The current is in *A* and the relative error in %)

Table 3.1 indicates that there is an improvement in the approximation obtained by the revised averaging method (with a new calculation method for the second duty cycle) in the I_B current because the relative error has been halved, although this is still not equal to zero. There has been no change in the expressions and approximations of the other two currents. Therefore, the approximation of the modelling method still needs to be corrected.

In the last equation of (21), it can be verified analytically that the conversion ratio in the AIDB converter has been improved in such a way that it gives a higher conversion ratio than the basic boost converter.

All calculations from now on will be made with the values of the parameters used in the experimental circuit assembly in order to facilitate the graphical comparisons that will be made in the following paragraphs. These values are: $L_A=L_B=L_{AO}=200\ \mu H$, $C_{AB}=50\ \mu F$, $C_O=23.5\ \mu F$, $R_L=10\ \Omega$, $T=20\ \mu s$.

The numeric values of the circuit variables in the operating point for $D=50\ \%$ that were calculated using (21) are as follows:

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$$\begin{cases} I_A = 6 \text{ A} \\ I_B = 3.38 \text{ A} \\ I_{AO} = 3 \text{ A} \\ V_{AB} = 20 \text{ V} \\ V_O = \left(1 + \dfrac{1}{D'}\right) V_g = 30 \text{ V} \end{cases} \tag{22}$$

It is important to remark that for this input voltage and duty cycle, the AIDB converter output voltage is three times the input voltage.

3.1.1.4.2 LINEAR EQUATIONS AROUND THE OPERATING POINT

The state space averaged system of (17) can be expressed as a small signal linear system in the following equation:

$$\dot{\hat{x}} = A\hat{x} + B\hat{d}_1 \tag{23}$$

Where A is the Jacobian Matrix of (17) regarding to the state variables vector and B is the Jacobian Matrix of (17) regarding to the duty cycle. Both Jacobian Matrices are evaluated at the operating point, as is shown in (24) and (25).

$$A = \left.\frac{\partial f(\overline{x}, d_1)}{\partial \overline{x}}\right|_{\overline{x}=X, d_1=D'} \tag{24}$$

$$B = \left.\frac{\partial f(\overline{x}, d_1)}{\partial d_1}\right|_{\overline{x}=X, d_1=D'} \tag{25}$$

In this system, once matrices A and B are obtained, and before the numeric values are replaced, it becomes necessary to make a time normalization because otherwise there will be numerical errors. This normalization consists of a change in the time scale [5]:

$$t_N = \frac{t}{10^{-6}} \tag{26}$$

Then, the corresponding scaling up for the inductors and the capacitors is

$$C_N = C \times 10^6, L_N = L \times 10^6 \tag{27}$$

The numeric values of matrices A and B, which can be seen in the following equations, use the same parameters values as the experimental prototype in section 2.6, but also take into account the normalization. These values are as follows: L_A=L_B=L_{AO}=200 μH, C_{AB}=50 μF, C_O=23.5 μF, R_L=10 Ω, T=20 μs. Thus, the matrices obtained can be used directly for comparisons with the experimental data

$$A=\begin{bmatrix} 0 & 0 & 0 & -0.0025 & 0 \\ 0 & -0.2678 & 0.2678 & -0.004171 & 0.002515 \\ 0 & 0.2675 & -0.2675 & 0.01086 & -0.0092 \\ 0.01 & 0 & -0.02 & 0 & 0 \\ 0 & 0 & 0.04255 & 0 & -0.004255 \end{bmatrix} \tag{28}$$

$$B=\begin{bmatrix} -0.1 \\ 0.4011 \\ -0.401 \\ 0.115 \\ 0 \end{bmatrix} \tag{29}$$

3.1.1.4.3 SMALL SIGNAL TRANSFER FUNCTIONS

The expression in (30) shows the control-to-output transfer function particularized for the same converter parameters used in the last paragraph (without normalization). As expected, the transfer function is of the fifth order.

$$G(s)=\frac{\hat{v}_O(s)}{\hat{d}(s)}=\frac{-4.65\cdot10^{-10}(s+3.66\cdot10^{19})(s+2.41\cdot10^{4})(s^2-2.69\cdot10^{4}s+1.86\cdot10^{8})}{(s^2+1625s+1.66\cdot10^{7})(s^2+3380s+2.14\cdot10^{8})(s+5.34\cdot10^{6})} \tag{30}$$

All the system poles are in the left half-plane, one of them very far from the origin. There are some zeroes in the right half-plane.

3.1.1.5 COMPARISONS IN THE FREQUENCY DOMAIN

The frequency response of the small signal model for the AIDB, described in (23), (28) and (29), can be calculated using MATLAB. In order to verify the accuracy of the calculated model it is necessary to compare it with theoretical and experimental frequency responses. The frequency domain simulation results of PSIM allow the theoretical Bode diagram of the circuit to be obtained. The experimental Bode diagram of the converter circuit can be measured using a frequency response analyzer (FRA). The details of the circuit schemes used in simulations and in the experimental measures will be presented in section 3.4 of this chapter. This section will not enter into these details because to do so would be to depart from the central issue that concerns us here.

The Bode diagrams were obtained for the control-to-output transfer function. The following figure shows three Bode diagrams in the same screen: the theoretical diagram (PSIM), the diagram that was measured experimentally (FRA), and the diagram calculated using the revised averaging modelling method (MODEL). Representing the three diagrams in only one screen allows us to clearly identify the differences between them.

Figure 3.3 shows that the discrepancies between the peaks of the three Bode diagrams are too great. It is normal for the experimental Bode diagram to show some differences with the theoretical diagrams (PSIM and MODEL) because of all the factors involved in the experimental assembly. But the other two Bode diagrams should look more similar to each

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other. For this reason this approximation can not be considered accurate enough, which means that it must be improved by searching for new information regarding the operation of the circuit that has not yet been taken into account, for example in the waveforms.

3.1.2 THE NEW MODIFIED AVERAGING APPROACH APPLIED TO AIDB

In order to achieve a better approximation, it was necessary to study and propose a new improvement to the modelling method used to analyze the AIDB. The origins and application of the new ideas will be studied in the following sections.

3.1.2.1 ORIGINS OF THE NEW APPROACH

Figure 3.2 shows that the output current I_O is exactly determined by adding two currents: the current in the inductor L_{AO} and the current in the diode D_B.

Therefore, in order to make a good approximation of the AIDB output current, it is necessary to include the current in diode DB in the analytical model. In this way, it would be possible to fix the error that is generated when this current is not included.

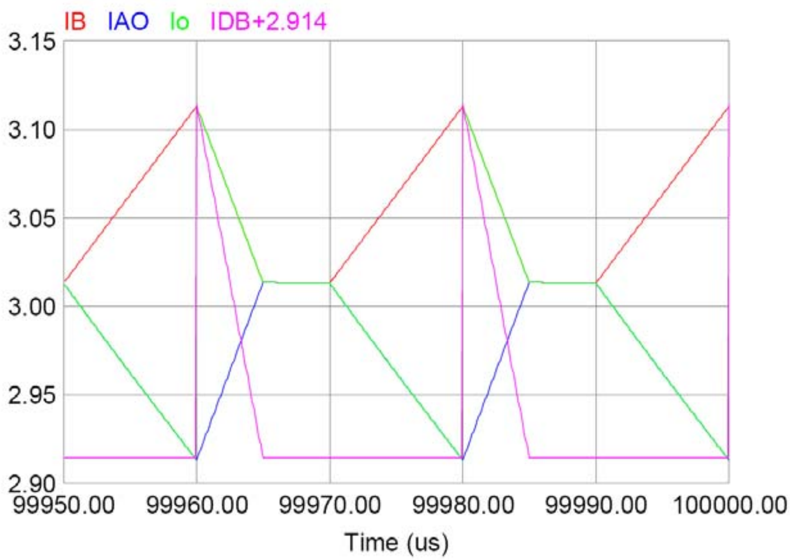

Figure 3.4: Calculation of the output current in the AIDB

3.1.2.2 MODIFICATIONS IN TOPOLOGY AND EQUATIONS

The circuital topologies (Figure 3.1) show that diode D_B conducts in topology 2. This topology and its equations can be modified in order to include the current I_{DB} in the following way [2-5]

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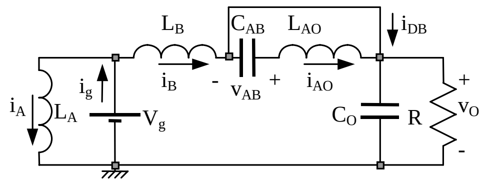

a) Topology 2. Interval 2: d_2

$$
\begin{aligned}
L_A\frac{d\,i_A}{dt} &= v_g\\
L_B\frac{d\,i_B}{dt} &= v_g - v_O\\
L_{AO}\frac{d\,i_{AO}}{dt} &= v_{AB}\\
C_{AB}\frac{d\,v_{AB}}{dt} &= -i_{AO}\\
C_O\frac{d\,v_O}{dt} &= i_{AO} + i_{DB} - \frac{v_O}{R}
\end{aligned}
\qquad (31)
$$

Figure 3.5: AIDB second topology 2 and equations including I_{DB}

3.1.2.3 NEW SSA FOR THE AIDB INCLUDING MODIFICATIONS

The new state space averaged system (*D>38%*) including this new variable is as follows:

$$
\begin{cases}
\dfrac{\mathrm{d}\bar{i}_A}{\mathrm{d}t} = \dfrac{v_g - \bar{v}_{AB}d_1}{L_A}\\
\dfrac{\mathrm{d}\bar{i}_B}{\mathrm{d}t} = \dfrac{v_g}{L_B}(d_1+d_2) - \dfrac{\bar{v}_O}{L_B}d_2 + \dfrac{v_g - \bar{v}_O + \bar{v}_{AB}}{L_B + L_{AO}}d_3\\
\dfrac{\mathrm{d}\bar{i}_{AO}}{\mathrm{d}t} = \dfrac{\bar{v}_{AB}}{L_{AO}}(d_1+d_2) - \dfrac{\bar{v}_O}{L_{AO}}d_1 + \dfrac{v_g - \bar{v}_O + \bar{v}_{AB}}{L_B + L_{AO}}d_3\\
\dfrac{\mathrm{d}\bar{v}_{AB}}{\mathrm{d}t} = \dfrac{\bar{i}_A d_1 - \bar{i}_{AO}}{C_{AB}}\\
\dfrac{\mathrm{d}\bar{v}_O}{\mathrm{d}t} = \dfrac{\bar{i}_{AO} + \bar{i}_{DB}}{C_O} - \dfrac{\bar{v}_O}{RC_O}
\end{cases}
\qquad (32)
$$

Where d_2 and d_3 were calculated in equations (16) and (1), respectively. The other new variable $\bar{i}_{DB}$ will be calculated in the next paragraph.

3.1.2.4 GRAPHICAL CALCULATION OF THE NEW VARIABLE

As in 3.1.1.3, using the triangle area formula described by the waveform of the $\bar{i}_{DB}$ current in Figure 3.4 , the average value of this current can be calculated as follows [2-5]

$$\bar{i}_{DB} = \frac{\Delta i_B + \Delta i_{AO}}{2}d_2 \qquad (33)$$

Now, substituting the expressions for Δi_B and Δi_{AO} that were obtained in (15)

$$\bar{i}_{DB} = \left(\frac{v_g}{L_B} + \frac{\bar{v}_O - \bar{v}_{AB}}{L_{AO}}\right)\frac{d_1 T}{2}d_2 \qquad (34)$$

Then, replacing the expression with d_2, which was obtained in (16)

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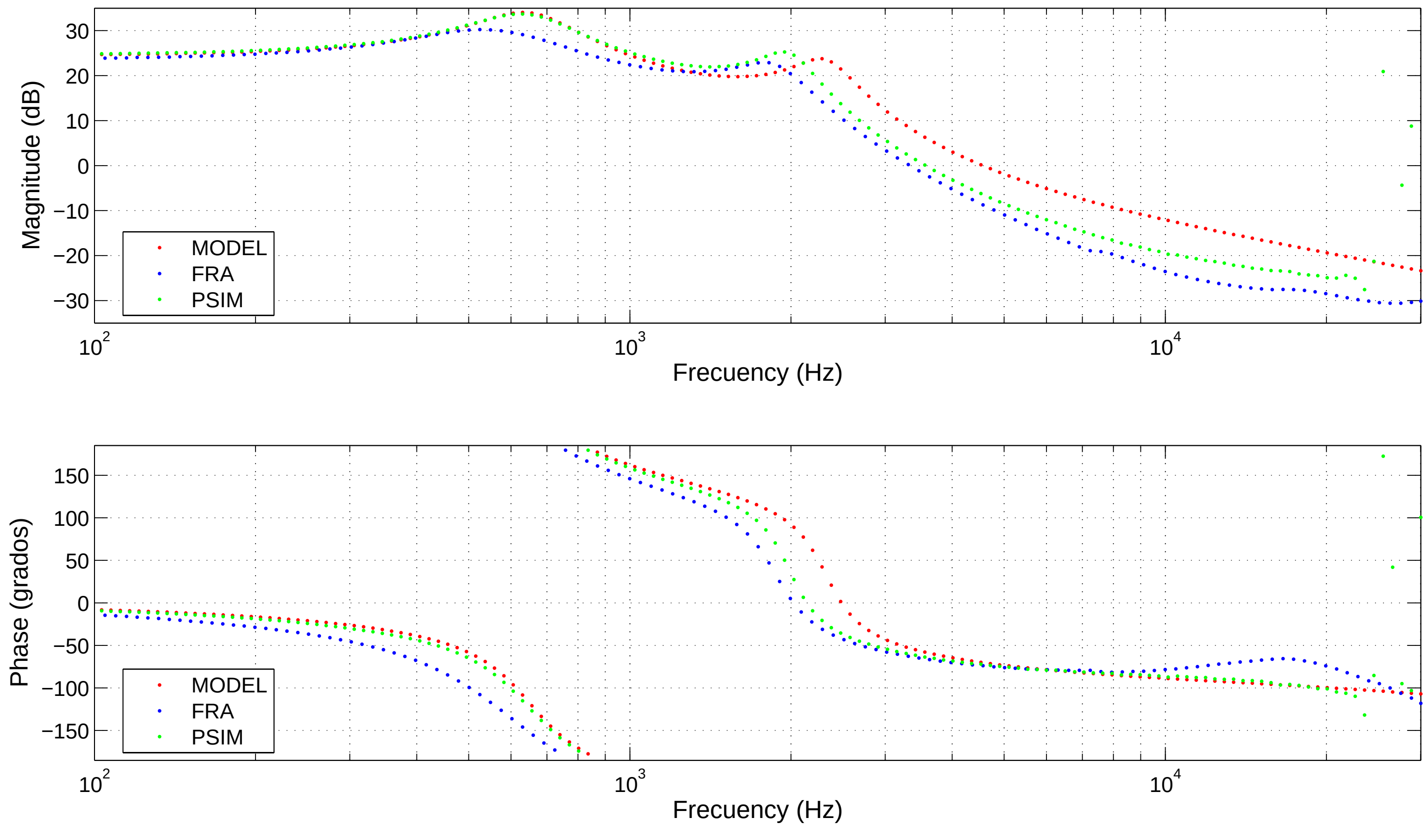

Figure 3.3: Three AIDB Bode Diagrams.
PSIM: theoretical, FRA: experimental and MODEL: calculated by the Revised Averaging Method.

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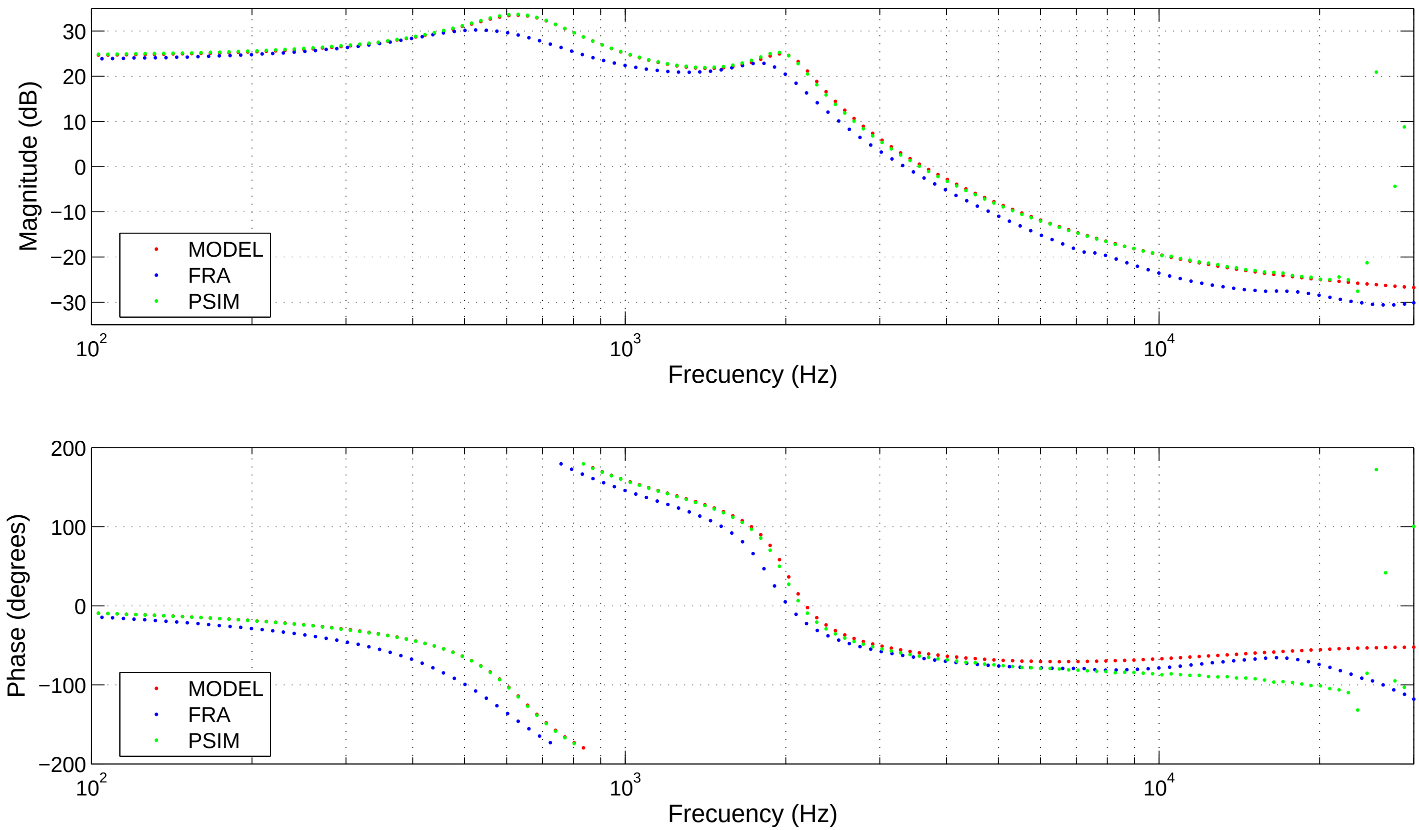

Figure 3.6: Three AIDB Bode Diagrams.
PSIM: theoretical, FRA: experimental and MODEL: calculated by the Modified Averaging Using Graphical Methods.

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$$\bar{i}_{DB} = \left(\frac{v_g}{L_B} + \frac{\bar{v}_O - \bar{v}_{AB}}{L_{AO}}\right)\frac{d_1 T}{2}\left(\frac{2(\bar{i}_B - \bar{i}_{AO})}{\left(\frac{v_g}{L_B} + \frac{\bar{v}_O - \bar{v}_{AB}}{L_{AO}}\right)d_1 T} - d_1\right) \tag{35}$$

3.1.2.5 SSA OF THE AIDB BY THE MODIFIED AVERAGING APPROACH

Replacing the equations (1), (16) and (35) in (32), the state space averaged system, for $D>38\%$, in terms of the duty cycle d_1 is obtained as

$$\begin{aligned}
\frac{d\,\bar{i}_A}{dt} &= \frac{v_g - \bar{v}_{AB} d_1}{L_A}\\
\frac{d\,\bar{i}_B}{dt} &= \frac{2\bar{i}_B L_B L_{AO}^2(a_1) + 2\bar{i}_{AO} L_B L_{AO}^2(a_2) + \bar{v}_{AB} d_1 T L_B^2(a_3) + \bar{v}_O d_1 T L_B L_{AO}(a_4) + d_1 T V_g(a_5)}{(-V_g L_{AO} - L_B \bar{v}_O + L_B v_{AB}) L_B (L_{AO} + L_B) d_1 T}\\
\frac{d\,\bar{i}_{AO}}{dt} &= \frac{2(\bar{i}_{AO} - \bar{i}_B) L_B L_{AO}(a_6) + d_1 T V_g L_{AO}^2(a_7) + \bar{v}_O d_1^2 T L_B(a_8) + d_1 T L_{AO} L_B(a_9)}{(-V_g L_{AO} - L_B \bar{v}_O + L_B v_{AB}) L_{AO} (L_{AO} + L_B) d_1 T}\\
\frac{d\,\bar{v}_{AB}}{dt} &= \frac{\bar{i}_A d_1 - \bar{i}_{AO}}{C_{AB}}\\
\frac{d\,\bar{v}_O}{dt} &= \frac{R_L\left[2\bar{i}_B L_B L_{AO} - d_1^2 T (V_g L_{AO} + \bar{v}_O L_B - \bar{v}_{AB} L_B)\right] - 2\bar{v}_O L_B L_{AO}}{C_O R_L L_B L_{AO}}
\end{aligned} \tag{36}$$

where

$$a_1 = -V_g + \bar{v}_O + \bar{v}_{AB} \qquad a_2 = V_g - \bar{v}_O - \bar{v}_{AB} \qquad a_3 = V_g + \bar{v}_{AB} + \bar{v}_O d_1 - 2\bar{v}_O$$

$$a_4 = V_g - d_1 V_g + d_1 \bar{v}_{AB} - d_1 \bar{v}_O \qquad a_5 = (-V_g - \bar{v}_{AB}) L_B L_{AO} - \bar{v}_O L_B^2 - \bar{v}_O d_1 L_{AO}^2$$

$$a_6 = (-V_g + \bar{v}_O) L_{AO} + \bar{v}_{AB} L_B \qquad a_7 = -V_g + \bar{v}_O (d_1 + 1) - \bar{v}_{AB} \qquad a_8 = -\bar{v}_{AB} + \bar{v}_O$$

$$a_9 = d_1 \bar{v}_O (V_g - \bar{v}_{AB}) + V_g (\bar{v}_{AB} - \bar{v}_O) - 2\bar{v}_{AB}\bar{v}_O + \bar{v}_{AB}^2 + \bar{v}_O^2$$

In (35) $d_1 = d'$.

3.1.2.5.1 OPERATING POINT

Following the same procedure described in 3.1.1.4.1, the operating point equations for $D>38\%$ can be obtained by solving the derivatives of the system equations equated to zero.

The following expressions (37) include modifications in the equation of the three currents (I_A, I_B and I_{AO}) that are the result of the correction introduced by the I_{DB} current. These improvements are the first difference between the operating point calculated by the new approach and the last two calculations of the operating point, that is, equation (26) in Chapter Two and equation (21) in this chapter.

As will be verified in the following calculations, these modifications have improved the approximation of the model. In the last equation it can be observed that the conversion ratio of the AIDB converter is the same as that obtained for the calculation of the operating point in (21) [2]. Further simplification of (37) can be obtained if $L_B=L_{AO}$.

$$\begin{cases} I_A = \dfrac{1}{D'}\left(1+\dfrac{1}{D'}\right)\dfrac{V_g}{R} - \dfrac{V_g}{2}\left(\dfrac{L_B+L_{AO}}{L_B L_{AO}}\right)D'^2\,T \\ I_B = \left(1+\dfrac{1}{D'}\right)\dfrac{V_g}{R} + \dfrac{V_g}{2}\left(\dfrac{L_B+L_{AO}}{L_B L_{AO}}\right)D'^2\,T \\ I_{AO} = \left(1+\dfrac{1}{D'}\right)\dfrac{V_g}{R} - \dfrac{V_g}{2}\left(\dfrac{L_B+L_{AO}}{L_B L_{AO}}\right)D'^3\,T \\ V_{AB} = \dfrac{V_g}{D'} \\ V_O = \left(1+\dfrac{1}{D'}\right)V_g \end{cases} \tag{37}$$

The same values for the parameters that were taken in 2.4 have been used to compare the results with the PSIM simulation results in Chapter Two. These are: $V_g=10\ V$, $L_A=L_B=L_{AO}=1\ mH$, $C_{AB}=\ 50\ \mu F$, $C_O=20\ \mu F$, $R_L=10\ \Omega$, $T=20\ \mu s$ and a duty cycle from $40\ \%$ to $90\ \%$ with steps of $10\ \%$.

Table 3.2: Mean values of the AIDB variables in steady state using expressions of (37)

D	Ig	I_A	I_B	I_{AO}	V_{AB}	V_O
0.4	7.11	4.37	2.74	2.62	16.67	26.67
0.5	9.00	5.95	3.05	2.98	20.00	30.00
0.6	12.24	8.71	3.53	3.49	25.00	35.00
0.7	18.78	14.43	4.35	4.33	33.33	43.33
0.8	36.01	30.00	6.01	6.00	50.00	60.00
0.9	121.00	110.00	11.00	11.00	100.00	110.00

(The currents are in A and the voltages in V)

The following table compares the relative errors of the steady state mean values with Table 2.1 in Chapter Two, whose values are used as the theoretical values.

Table 3.3: Relative errors of the AIDB variables in steady state (Comparing tables 2.1 and 3.2)

D	Ig	I_A	I_B	I_{AO}	V_{AB}	V_O
0.4	0.00	0.00	0.00	0.00	0.00	0.00
0.5	0.00	0.00	0.00	-0.07	0.00	0.00
0.6	0.08	0.11	0.00	0.00	0.00	0.00
0.7	0.00	0.00	0.00	0.00	0.00	0.00
0.8	-0.03	-0.03	0.00	0.00	0.00	0.00
0.9	-0.02	-0.02	0.00	0.00	-0.02	-0.02

(All the values are in %)

Table 3.3 shows that the average values obtained with (37) and the theoretical values obtained in the simulations are almost equal. The differences are in the order of milliamps and are rounded to two decimal places. The graphics of these initial results obtained with the modified averaging method show this method is more accurate than previous

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approximations. Another observation is that as the duty cycle increases, the average value of the current in diode D_B decreases, so the effect of the correction is smaller.

All the calculations made from now on in this paper will use the values of the parameters from the experimental circuit prototype in Chapter 2, so as to facilitate the graphical comparisons that will be made in the following paragraphs. Those values are: $L_A=L_B=L_{AO}=200\ \mu H$, $C_{AB}=50\ \mu F$, $C_O=23.5\ \mu F$, $R_L=10\ \Omega$, $T=20\ \mu s$.

The differences between the two methods shown can also be verified by comparing the numeric values of the $D=50\ \%$ operating point (shown in (22)) with the numeric values of the next equation

$$\begin{cases} I_A = 5.752\text{ A} \\ I_B = 3.25\text{ A} \\ I_{AO} = 2.876\text{A} \\ V_{AB} = 20\text{ V} \\ V_O = \left(1+\dfrac{1}{D'}\right)V_g = 30\text{ V} \end{cases} \tag{38}$$

Where the conversion ratio for the input voltage is again equal to three.

3.1.2.5.2 OPERATING POINT BY AN AVERAGING ON THE WAVEFORMS

The expressions in (37) were obtained by operating in the state equations. These expressions can be also calculated using the procedure in section 2.4.3 of Chapter Two (hypothesis of low ripple in the state varibles, inductor flow balance and capacitor charge balance), which directly averages the waveforms, but including the correction proposed by the new modified averaging approach. From the waveforms in Figure 3.4

$$\Delta I_{DB} = \Delta I_B + \Delta I_{AO} \tag{39}$$

Using the expressions of equation (15) in the operating point and taking into account equations (2) and (9) in Chapter Two

$$V_g + V_{AB} = V_O \tag*{(9$_{\text{chapter 2}}$)}$$

The following can be obtained

$$\Delta I_{DB} = V_g\left(\frac{1}{L_B}+\frac{1}{L_{AO}}\right)D'T \tag{40}$$

The same waveform in Figure 3.4 can be used to obtain the mean value of the current in the diode D_B. This is done by first calculating the area and then dividing it by the period.

$$I_{DB} = \frac{V_g}{2}\left(\frac{L_{AO}+L_B}{L_{AO}L_B}\right)D'^3\,T \tag{41}$$

Figure 3.2 shows that

$$I_O = I_{AO} + I_{DB} \tag{42}$$

The substitution of the expression for the output voltage in the last equation yields

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$$I_{AO}=\left(1+\frac{1}{D'}\right)\frac{V_g}{R}-\frac{V_g}{2}\left(\frac{L_{AO}+L_B}{L_{AO}L_B}\right)D'^3\,T \tag{43}$$

This equation coincides with the expression obtained in (37) for the current in inductor L_{AO}.

Now, using the equation for the relationship between the currents I_{AO} and I_A obtained through a correct average in Chapter Two, we get the following

$$I_A=\frac{I_{AO}}{D'} \tag{18$_{\text{chapter 2}}$}$$

Then:

$$I_A=\frac{1}{D'}\left(1+\frac{1}{D'}\right)\frac{V_g}{R}-\frac{V_g}{2}\left(\frac{L_{AO}+L_B}{L_{AO}L_B}\right)D'^2\,T \tag{44}$$

This coincides with the expression for the current in inductor L_A obtained in (37).

A power balance has been made in order to find the expressions for I_B. After this, the equation for the output voltage and the equation (44) has been substituted in the results. The Organization of the expression gives us the following

$$I_B=\left(1+\frac{1}{D'}\right)\frac{V_g}{R}+\frac{V_g}{2}\left(\frac{L_{AO}+L_B}{L_{AO}L_B}\right)D'^2\,T \tag{45}$$

This is the same expression for the current in inductor L_B which was obtained in (37).

This averaging on the waveforms procedure is shown to be valid because the expressions obtained with (43), (44) and (45) coincide with those that were calculated in (37).

3.1.2.5.3 LINEAR EQUATIONS AROUND THE OPERATING POINT

The state space averaged system of (36) can be expressed as a small signal linear system in the following equation

$$\dot{\hat{x}}=A\hat{x}+B\hat{d}_1 \tag{46}$$

Where A and B are calculated as in 3.1.1.4.2. The numeric values of these matrices used the same values for the circuit parameters that were used in the experimental circuit prototype, but also took into account the normalization [5].

$$A=\begin{bmatrix} 0 & 0 & 0 & -0.0025 & 0 \\ 0 & -0.2 & 0.2 & -0.003114 & 0.001875 \\ 0 & 0.2 & -0.2 & 0.00812 & -0.00688 \\ 0.01 & 0 & -0.02 & 0 & 0 \\ 0 & 0.4255 & 0 & 0.000532 & -0.004788 \end{bmatrix} \tag{47}$$

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$$B = \begin{bmatrix} -0.1 \\ 0.2998 \\ -0.3 \\ 0.115 \\ -0.04255 \end{bmatrix} \tag{48}$$

3.1.2.5.4 SMALL SIGNAL TRANSFER FUNCTIONS

The expression in (49) shows the control-to-output transfer function particularized for the same converter parameters used in the last paragraph (without normalization). As expected, the transfer function is of the fifth order.

$$G(s) = \frac{\hat{v}_O(s)}{\hat{d}(s)} = \frac{-42550(s+7.67\cdot 10^4)(s+5.67\cdot 10^4)(s^2-2.58\cdot 10^4)(s-8895)}{(s^2+1785s+1.65\cdot 10^7)(s^2+2812s+1.61\cdot 10^8)(s+4\cdot 10^5)} \tag{49}$$

All the system poles are in the left half-plane, one of them very far from the origin. There are some zeroes in the right half-plane which will make it difficult to design a control loop for the system.

3.1.2.6 COMPARISONS IN FREQUENCY DOMAIN

Again it is necessary to make comparisons in order to verify the accuracy of the model that was calculated by modified averaging using graphical methods. The frequency response of the small signal model for the AIDB, described in (46), (47) and (48), can be calculated using MATLAB. As in 3.1.1.5, the theoretical Bode of the control-to-output transfer function of the circuit was calculated using PSIM and the experimental Bode was calculated using the frequency response analyzer (FRA) equipment.

As already explained in this chapter, the details of the circuit schemes used in simulations and experimental measures will be presented later.

Figure 3.6 shows three Bode diagrams in the same screen: the theoretical diagram (PSIM), the diagram that was measured experimentally (FRA) and the diagram calculated by modified averaging using graphical methods (MODEL). Showing the three diagrams in only one screen allows us to clearly identify the differences between each diagram.

The frequency response of the new model is the red diagram. The figure shows that the approach has been improved because it virtually coincides with the theoretical Bode diagram calculated by PSIM. Consequently this approach has also improved in comparison with the experimentally measured bode diagram (FRA).

The Magnitude diagram shows that the approximation obtained with the new modelling method is better than the approximation of the PSIM at high frequencies (greater that $2{\cdot}10^4$). The phase diagram of the MODEL shows this improvement for a frequencies interval between $1{\cdot}10^4$ and $2{\cdot}10^4$.

This interesting result validates the method used for modelling the converter AIDB, demonstrating that the model generated by modified averaging using graphical methods provides a better approach to the frequency behaviour of the AIDB converter.

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3.2 MODIFIED AVERAGING USING GRAPHICAL METHODS

The method of modified averaging using graphical methods, which was explained in the previous sections and used to model the AIDB converter, has its origins in previous studies by various authors, as will be shown in the following section.

3.2.1 PREVIOUS WORK

In previous papers, in addition to [1], the use of graphical waveforms of the circuit has also been studied as a means of getting results that can be applied to the modelling method.

All the papers that will be revised here were analyzed and classified in Chapter One in accordance with the methodology proposed. But this section will specifically highlight the kind of graphical approximation proposed and the way it is used in the modelling method.

Reference [6] provides the first use of circuit waveforms. In this case, the inductor current waveform of a boost converter provides the average inductor current injected into the output circuit during a switching period. This was used in the paper in order to get the transfer functions and the equivalent circuit model.

In [7], there is a correction in the derivation of the averaged models for current mode control converters that was deduced by elementary geometrical calculations from the inductor current waveform of a DC to DC switching converter in constant frequency, current mode controlled and continuous conduction mode.

In [8], the expressions for the averaged terminal currents and voltages were obtained by applying geometrical calculations to the waveforms of the terminal currents of the PWM switch in DCM. These expressions were then used to determine the relationships between variables in the PWM switch model.

In [9], an equivalent duty ratio is calculated applying basic geometric concepts to the current waveform and using the averaged value of the current. A unified model for PWM converters in DCM is then developed using this equivalent duty ratio.

In [10-13], geometrical calculations were applied to the inductor current waveforms in order to calculate some variables for deducing the behavioural PWM average model of the switched inductor, known as USIM and GSIM. The GSIM permits the calculation of an equivalent circuit model that is used in SPICE simulations.

In [14], the expression of the average current through the inductor branch of the circuit was obtained from geometrical calculations on the waveforms of a PWM converter in DCM. These expressions were then used to obtain the equivalent circuit model and the small signal model including losses.

This brief review shows that the authors have used the waveforms of the circuits to calculate variables that could not be obtained from other methods and that were necessary for the modelling method applied.

The main difference between these approaches and the new method proposed in this chapter is that the graphics of the waveforms have not only been used to calculate variables, but also to show that in order to improve the accuracy of the model, it must include a variable that has not been considered so far by any other author: the current through the diode in DCM.

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3.2.2 DETAIL DESCRIPTION OF THIS NEW APPROACH

On the basis of the results of the modelling method applied to the AIDB converter, a detailed description of this new approach will be made in the following sections so it can be used to model the other asymmetric interleaved converters explored in the Chapter Two.

3.2.2.1 MODIFICATIONS INCLUDED

This method averages the state variables of the converter in a conventional way but includes two changes that improve the approximation of the model.

The first is topological generated on the basis of the comparisons between the circuit topologies for each conduction interval and the waveforms of the circuit variables in DCM. These comparisons show that a new current variable, the current of the diode in DCM, must be included in the topologies for every interval and in the state equations for each topology. This variable is not normally taken into account in these methods of modelling and its inclusion improves the accuracy of the model.

The second is graphical. The improvement comes from using the waveforms of the currents in DCM to correctly calculate the second duty cycle and the averaged value of the new variable introduced. The modification uses basic geometric calculations of the waveforms to obtain the average calculation. This is necessary because in the currents with three intervals (DCM) the average in the duty cycles is different from the average throughout the whole period.

3.2.2.2 STEPS

Summarizing, the steps of the modified averaging using graphical methods are follows:

1) Initial simulation with the aim of identifying the discontinuous variables and making graphic relationships between the state variables of the circuit
2) Deciding if it is necessary to include some new variables
3) Obtaining the circuit topologies
4) Obtaining the equations for each topology including new variables
5) Averaging the equations obtained, taking into account that the included variables are not state variables and their expressions must be obtained from waveforms
6) Deriving the expressions for the new variables and for the second duty cycle using the waveforms of the state variables in DCM
7) Replacing the expressions calculated in the state averaged system and obtaining the final system.
8) Calculating the operating point and the linearized state equations around an operating point
9) Calculating the small signal transfer functions.

3.2.2.3 WHY IS IT NECESSARY TO APPLY THIS NEW APPROACH?

The application of this method is necessary because of the simultaneous appearance of DCM currents (with three intervals) and CCM currents (with two intervals). In theory, if the

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CCM and DCM currents were not concurrent, the revised averaged method would provide an accurate approach.

3.2.2.4 CONVERTERS ANALYZED WITH THIS METHOD

This method has been applied to asymmetric interleaving converters that operate in DCM with two characteristics: currents in DCM and CCM simultaneously and DCM currents that equal their values in the third interval. In addition, these are high order converters.

Further research arising from this thesis could study the application of this method to other high order converters that exhibit linear relationship between their variables in DCM (Cuk and SEPIC) or meet the other requirements mentioned here.

The next section will show the application of this method to the other asymmetrical interleaving converters of the family presented in the second chapter.

3.3 APPLYING MODIFIED AVERAGING USING GRAPHICAL METHODS

The converters generated in section 2.5 will be analyzed in the following paragraphs.

3.3.1 ANALYSIS OF THE AIDBB

The analysis of the AIDBB using the modified averaging method is presented in this subsection. The characteristics of this asymmetrical interleaved converter are confirmed by the analysis results [3].

3.3.1.1 PREVIOUS SIMULATIONS

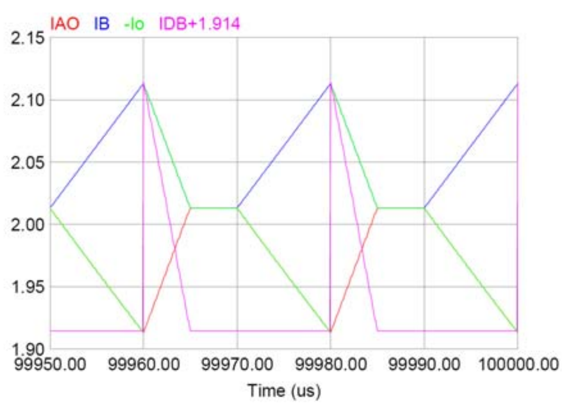

Figure 3.7: Waveforms of the DCM currents in the AIDBB ($D=50\%$)

The simulations results in Chapter Two showed that the currents in DCM are the same as the currents in the AIDB: i_{AO}, i_B, i_O and i_{DB}. In this case the output current is negative,

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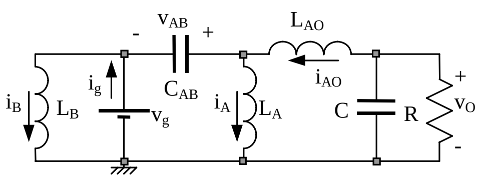
because the AIDBB offers a negative output, but relationships between currents similar to those shown in Figure 3.4 can be obtained with some operations on the waveforms.

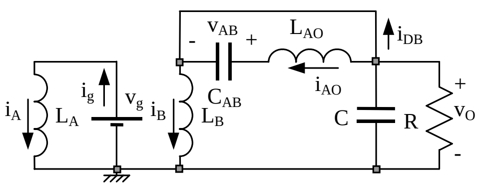
The second step of this modified methodology indicates that the variables that have to be included in the model are obtained from the initial simulations. In this case, this variable is the current in the diode D_B, similar to the situation with the AIDB.

3.3.1.2 TOPOLOGIES AND EQUATIONS



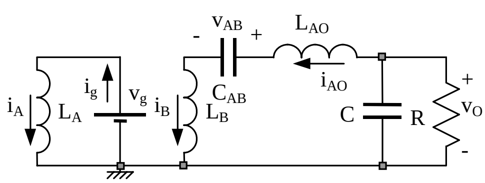
a) Topology 1. Interval 1: d'=d1
(S_B and D_A ON; S_A and D_B OFF)

$$L_A \frac{d\,i_A}{dt} = v_g + v_{AB}$$
$$L_B \frac{d\,i_B}{dt} = v_g$$
$$L_{AO} \frac{d\,i_{AO}}{dt} = -v_g - v_{AB} + v_O \qquad (50)$$
$$C_{AB} \frac{d\,v_{AB}}{dt} = -i_A + i_{AO}$$
$$C_O \frac{d\,v_O}{dt} = -i_{AO} - \frac{v_O}{R}$$



b) Topology 2. Interval 2: d2
(S_A and D_B ON; S_B and D_A OFF)

$$L_A \frac{d\,i_A}{dt} = v_g$$
$$L_B \frac{d\,i_B}{dt} = v_O$$
$$L_{AO} \frac{d\,i_{AO}}{dt} = -v_{AB} \qquad (51)$$
$$C_{AB} \frac{d\,v_{AB}}{dt} = i_{AO}$$
$$C_O \frac{d\,v_O}{dt} = -i_B - \frac{v_O}{R}$$



c) Topology 3. Interval 3 (DCM): d_3
(S_A ON; S_B, D_A, and D_B OFF)

$$L_A \frac{d\,i_A}{dt} = v_g$$
$$(L_B + L_{AO}) \frac{d\,i_B}{dt} = -v_{AB} + v_O$$
$$i_{AO} = i_B \quad * \qquad (52)$$
$$C_{AB} \frac{d\,v_{AB}}{dt} = i_{AO}$$
$$C_O \frac{d\,v_O}{dt} = -i_{AO} - \frac{v_O}{R}$$

Figure 3.8: Topologies and equations in the AIDBB converter for $d > 38\,\%$.

Figure 3.8 shows the different topologies that the AIDBB converter can adopt as a function of the conduction states of switches and diodes. The corresponding state equations are in front of the topology. The new variables added to the analysis appear in the circuits and the equations.

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The converter topologies follow one another cyclically in the order shown in Figure 3.8, where d_1, d_2 and d_3 (DCM) are the relative duration of the corresponding operation intervals. The relative duration of the intervals can be related to the duty cycle of the reference switch S_A, as indicated in equations (1) and (2).

It can be observed that the equation of the third interval marked with an asterisk ($*$) again reflects the reduction of order in the DCM of the asymmetrical interleaved converters and imposes a stronger restriction than the equality of the derivatives of the variables.

3.3.1.3 AVERAGING

The averaged state equations ($D>38\%$) of the system are shown in (53). In the equations there are some variables, specifically the current through the DCM diode D_B and d_2, that must be expressed in terms of the state variables.

$$\begin{aligned}
\frac{d\,\bar{i}_A}{dt} &= \frac{v_g + \bar{v}_{AB} d_1}{L_A} \\
\frac{d\,\bar{i}_B}{dt} &= \frac{v_g}{L_B} d_1 + \frac{\bar{v}_O}{L_B} d_2 + \frac{\bar{v}_O - \bar{v}_{AB}}{L_B + L_{AO}} d_3 \\
\frac{d\,\bar{i}_{AO}}{dt} &= \frac{\bar{v}_O - v_g}{L_{AO}} d_1 - \frac{\bar{v}_{AB}}{L_{AO}} (d_1 + d_2) + \frac{\bar{v}_O - \bar{v}_{AB}}{L_B + L_{AO}} d_3 \\
\frac{d\,\bar{v}_{AB}}{dt} &= \frac{-\bar{i}_A d_1 + \bar{i}_{AO}}{C_{AB}} \\
\frac{d\,\bar{v}_O}{dt} &= \frac{-\bar{i}_{AO} - \bar{i}_{DB}}{C_O} - \frac{\bar{v}_O}{RC_O}
\end{aligned} \tag{53}$$

3.3.1.4 ADDITIONAL VARIABLES CALCULATION

The sixth step of this modified methodology indicates that the relationships between the variables can be obtained by applying a geometrical procedure to the waveforms of Figure 3.7 similar to that which was followed in 3.1.1.3 and 3.1.2.4.

The average for the converter currents can be calculated using the areas of the waveform triangles in Figure 3.7, as can be seen in the following equations [3].

Therefore, the mean value of the i_B current is

$$\bar{i}_B = I + \frac{\Delta i_B}{2}(d_1 + d_2) \tag{54}$$

Consequently, the mean value of the i_{AO} current is

$$\bar{i}_{AO} = I - \frac{\Delta i_{AO}}{2}(d_1 + d_2) \tag{55}$$

Now, the equations for the Δi_B and Δi_{AO} can be obtained by integrating the corresponding equations of the first topology (53), and taking into account the peak current

$$\Delta i_B = \frac{v_g}{L_B} d_1 T; \quad \Delta i_{AO} = \frac{v_g + \bar{v}_{AB} - \bar{v}_O}{L_{AO}} d_1 T \tag{56}$$

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Then, the expression for d_2 is obtained by subtracting equations (54) and (55), and replacing Δi_B and Δi_{AO} with the expressions in equation (56). The result is

$$d_2 = \frac{2(\bar{i}_B - \bar{i}_{AO})}{\left(\frac{v_g}{L_B} + \frac{v_g + \bar{v}_{AB} - \bar{v}_O}{L_{AO}}\right) d_1 T} - d_1 \tag{57}$$

The average value of the $\bar{i}_{DB}$ current can be obtained using the formula of the area of the triangle described by this current waveform in Figure 3.7

$$\bar{i}_{DB} = \frac{\Delta i_B + \Delta i_{AO}}{2} d_2 \tag{58}$$

Now, substituting the expressions for Δi_B and Δi_{AO} which were obtained in (56)

$$\bar{i}_{DB} = \left(\frac{v_g}{L_B} + \frac{v_g + \bar{v}_{AB} - \bar{v}_O}{L_{AO}}\right) \frac{d_1 T}{2} d_2 \tag{59}$$

Then, replacing (57) in (59)

$$\bar{i}_{DB} = \left(\frac{v_g}{L_B} + \frac{v_g + \bar{v}_{AB} - \bar{v}_O}{L_{AO}}\right) \frac{d_1 T}{2} \left(\frac{2(\bar{i}_B - \bar{i}_{AO})}{\left(\frac{v_g}{L_B} + \frac{v_g + \bar{v}_{AB} - \bar{v}_O}{L_{AO}}\right) d_1 T} - d_1 \right) \tag{60}$$

3.3.1.5 SSA WITH THE MODIFICATIONS INCLUDED

Replacing the equations (1), (57) and (60) in (53), it is possible to obtain the state space averaged system in terms of the duty cycle d_1. This is a very large system of equations, as shown in 3.1.2.5 for the AIDB calculations, and it will not be included here for simplicity. The averaged system can also be expressed as

$$\dot{\bar{x}} = f(\bar{x}, d_1) \tag{61}$$

Where $\bar{x}$ $\dot{\bar{x}}$ are the vectors of the averaged state variables and their derivatives in the order that they appear in (53). In (61), $d_1 = d'$ has been chosen again as the control input for obtaining the model of the converter.

3.3.1.6 OPERATING POINT

Solving (61) when the derivatives of the state variables are equal to zero leads to the steady-state average equations that are shown in (62).

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$$\begin{cases} I_A = \left(\dfrac{1}{D'^2}\right)\dfrac{V_g}{R} - \dfrac{V_g}{2}\left(\dfrac{L_B + L_{AO}}{L_B L_{AO}}\right) D'^2\, T \\ I_B = \left(\dfrac{1}{D'}\right)\dfrac{V_g}{R} + \dfrac{V_g}{2}\left(\dfrac{L_B + L_{AO}}{L_B L_{AO}}\right) D'^2\, T \\ I_{AO} = \left(\dfrac{1}{D'}\right)\dfrac{V_g}{R} - \dfrac{V_g}{2}\left(\dfrac{L_B + L_{AO}}{L_B L_{AO}}\right) D'^3\, T \\ V_{AB} = -\dfrac{V_g}{D'} \\ V_O = -\dfrac{V_g}{D'} \end{cases} \tag{62}$$

The input-to-output DC transfer ratio is *–1/D’* instead of the conventional buck-boost transfer ratio (*–D/D’*). This transfer ratio is more similar to the ratio of an inverting conventional boost (*-1/D’*).

3.3.1.6.1 LINEAR EQUATIONS AROUND THE OPERATING POINT

The state space averaged system of (61) can be expressed as a small signal linear system in the following equation

$$\dot{\hat{x}} = A\hat{x} + B\hat{d}_1 \tag{63}$$

Where A and B are calculated as in 3.1.1.4.2. The numeric values of these matrices have been obtained with the same converter parameters of the Chapter Two simulations. These are: $V_g=10\ V$, $L_A=L_B=L_{AO}=1\ mH$, $C_{AB}= 50\ \mu F$, $C_O=20\ \mu F$, $R_L=10\ \Omega$, $T=20\ \mu s$ and $D=60\%$.

$$A = \begin{bmatrix} 0 & 0 & 0 & 400 & 0 \\ 0 & -312500 & 312500 & 460 & -310 \\ 0 & 312500 & -312500 & -1460 & 1310 \\ -8000 & 0 & 20000 & 0 & 0 \\ 0 & -50000 & 0 & 80 & -5080 \end{bmatrix} \tag{64}$$

$$B = \begin{bmatrix} -25000 \\ 69375 \\ -69375 \\ -124360 \\ 8000 \end{bmatrix} \tag{65}$$

3.3.1.7 SMALL SIGNAL TRANSFERS FUNCTIONS

The expression in (66) shows the control-to-output transfer function particularized for the same converter parameters used in the last paragraph.

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$$G(s)=\frac{\hat{v}_O(s)}{\hat{d}(s)}=\frac{8\cdot 10^3(s-3315)(s-1600)(s+185100)(s+397900)}{(s^2+1957s+2.7\cdot 10^6)(s^2+3088s+2.96\cdot 10^7)(s+6.25\cdot 10^5)} \quad (66)$$

As expected, the transfer function is of the fifth order. All the system poles are in the left half-plane, one of them very far from the origin. There are some zeroes in the right half-plane which will make it difficult to design a control loop for the system.

3.3.2 ANALYSIS OF THE AIDF-GROUP

An AIDF converter of positive output voltage has been chosen for the theoretical analysis (see following figure). However, the same analysis procedure can be applied to the other converters in the AIDF-group [4].

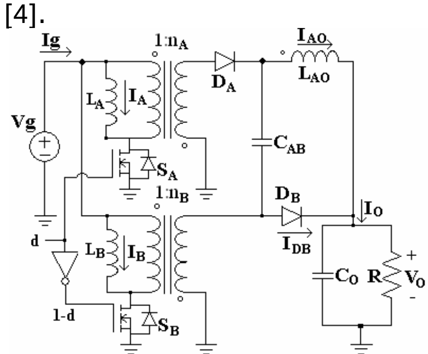

Figure 3.9: AIDF Converter of positive output voltage.

3.3.2.1 PREVIOUS SIMULATIONS

The figure that relates the currents in DCM i_{AO}, i_B, i_O and i_{DB} has been obtained again in previous simulations in the same way that was obtained for the other converters of the family (Figures 3.4 and 3.7). But, in this case the current in the diode D_B has a slope that is not completely vertical due to the effects of the transformers in simulations. However, it is possible to obtain the same relationship between the currents, making an approximation.

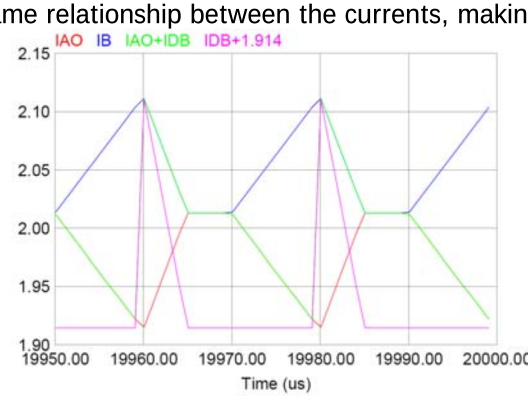

Figure 3.10: Waveforms of the DCM currents in the AIDF of positive output (D=50%)

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3.3.2.2 TOPOLOGIES AND EQUATIONS

The schematics of the topologies can be seen in Figure 2.30 of the second chapter. The following are the state equations for each of the switching intervals of interest, d_1, d_2, d_3. Both, schematics and equations, correspond to duty cycles greater than *38%*. The magnetization inductances of each transformer are L_A and L_B, whose conversion relationships are $1{:}n_A$ and $1{:}n_B$. A general mathematical analysis has been done and it has been decided that $n_A=n_B=n$.

The converter topologies follow one another cyclically in the order shown in (67), (68) and (69), where d_1, d_2 and d_3 (DCM) are the relative duration of the corresponding operation intervals. The relative duration of the intervals can be related to the duty cycle of the reference switch S_A as was indicated in equations (1) and (2).

The equation of the third interval marked with an asterisk ($*$) reflects the reduction of order that occurs in the DCM of the asymmetrical interleaved converters.

$n_A L_A \frac{d\,i_A}{dt} = n_B v_g - v_{AB}$ $L_B \frac{d\,i_B}{dt} = v_g$ $L_{AO} \frac{d\,i_{AO}}{dt} = -n_B vg + v_{AB} - v_O$ $C_{AB} \frac{d\,v_{AB}}{dt} = \frac{i_A}{n_A} - i_{AO}$ $C_O \frac{d\,v_O}{dt} = i_{AO} - \frac{v_O}{R}$ (67) Topology 1. Interval 1: d'=d1 S_B and D_A ON; S_A and D_B OFF	$L_A \frac{d\,i_A}{dt} = v_g$ $n_B L_B \frac{d\,i_B}{dt} = -v_O$ $L_{AO} \frac{d\,i_{AO}}{dt} = v_{AB}$ $C_{AB} \frac{d\,v_{AB}}{dt} = -i_{AO}$ $C_O \frac{d\,v_O}{dt} = i_{AO} + i_{DB} - \frac{v_O}{R}$ (68) Topology 2. Interval 2: d2 S_A and D_B ON; S_B and D_A OFF	$L_A \frac{d\,i_A}{dt} = v_g$ $(\frac{n_B^2 L_B + L_{AO}}{n_B}) \frac{d\,i_B}{dt} = v_{AB} - v_O$ $i_{AO} = \frac{i_B}{n_B} \quad *$ $C_{AB} \frac{d\,v_{AB}}{dt} = -i_{AO}$ $C_O \frac{d\,v_O}{dt} = i_{AO} - \frac{v_O}{R}$ (69) Topology 3. Interval 3 (DCM): d3 S_A ON; S_B, D_A, and D_B OFF

3.3.2.3 AVERAGING

The averaged state equations ($D>38\%$) of the system are shown in (70). The equations have two variables, specifically the current through the DCM diode D_B and the duration of the second interval d_2, which must be expressed in terms of the state variables.

$$
\begin{aligned}
\frac{d\,\bar{i}_A}{dt} &= \frac{v_g(n_B d_1 + n_A(1-d_1)) - \bar{v}_{AB} d_1}{n_A L_A} \\
\frac{d\,\bar{i}_B}{dt} &= \frac{v_g}{L_B} d_1 - \frac{\bar{v}_O}{n_B L_B} d_2 + \frac{\bar{v}_{AB} - \bar{v}_O}{n_B^2 L_B + L_{AO}} n_B d_3 \\
\frac{d\,\bar{i}_{AO}}{dt} &= \frac{-n_B \bar{v}_g - v_O}{L_{AO}} d_1 + \frac{\bar{v}_{AB}}{L_{AO}}(d_1 + d_2) + \frac{\bar{v}_{AB} - \bar{v}_O}{n_B^2 L_B + L_{AO}} d_3 \\
\frac{d\,\bar{v}_{AB}}{dt} &= \frac{\bar{i}_A d_1 - \bar{i}_{AO}}{C_{AB}} \\
\frac{d\,\bar{v}_O}{dt} &= \frac{\bar{i}_{AO} + \bar{i}_{DB}}{C_O} - \frac{\bar{v}_O}{R C_O}
\end{aligned}
\qquad (70)
$$

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3.3.2.4 ADDITIONAL VARIABLES CALCULATION

The average for the converter currents can be calculated using the areas of the waveform triangles in Figure 3.10, as can be seen in the following equations [4].

Therefore, the mean value of the i_B current is

$$\frac{\bar{i}_B}{n_B} = I + \frac{\Delta i_B}{2n_B}(d_1 + d_2) \tag{71}$$

Consequently, the mean value of the i_{AO} current is

$$\bar{i}_{AO} = I - \frac{\Delta i_{AO}}{2}(d_1 + d_2) \tag{72}$$

Now the equations for the Δi_B and Δi_{AO} can be obtained by integrating the corresponding equations of the first topology (67), and taking into account the peak current.

$$\Delta i_B = \frac{v_g}{L_B} d_1 T; \quad \Delta i_{AO} = \frac{n_B v_g - \bar{v}_{AB} + \bar{v}_O}{L_{AO}} d_1 T \tag{73}$$

Then, the expression for d_2 is obtained by subtracting the equations (71) and (72), and replacing Δi_B and Δi_{AO} by the expressions of the equation (73). The result is

$$d_2 = \frac{2\left(\frac{\bar{i}_B}{n_B} - \bar{i}_{AO}\right)}{\left(\frac{v_g}{n_B L_B} + \frac{n_B v_g - \bar{v}_{AB} + \bar{v}_O}{L_{AO}}\right) d_1 T} - d_1 \tag{74}$$

The average value of the $\bar{i}_{DB}$ current can be obtained using the area formula of the triangle described by the this current waveform in Figure 3.10

$$\bar{i}_{DB} = \frac{\frac{\Delta i_B}{n_B} + \Delta i_{AO}}{2} d_2 \tag{75}$$

Now, substituting the expressions for Δi_B and Δi_{AO} that were obtained in (73)

$$\bar{i}_{DB} = \left(\frac{v_g}{n_B L_B} + \frac{n_B v_g - \bar{v}_{AB} + \bar{v}_O}{L_{AO}}\right) \frac{d_1 T}{2} d_2 \tag{76}$$

Then, replacing (74) in (76)

$$\bar{i}_{DB} = \left(\frac{v_g}{n_B L_B} + \frac{n_B v_g - \bar{v}_{AB} + \bar{v}_O}{L_{AO}}\right) \frac{d_1 T}{2} \left(\frac{2\left(\frac{\bar{i}_B}{n_B} - \bar{i}_{AO}\right)}{\left(\frac{v_g}{n_B L_B} + \frac{n_B v_g - \bar{v}_{AB} + \bar{v}_O}{L_{AO}}\right) d_1 T} - d_1 \right) \tag{77}$$

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3.3.2.5 OPERATING POINT

The state space averaged system can be obtained by replacing the equations (1), (74) and (77) in (70). After that, the operation point of the system can be obtained using the symbolic mathematical analysis program, MAPLE

$$X = A^{-1} B V_g \tag{78}$$

Therefore, the steady-state average equations of the operating point are

$$\begin{cases} I_A = \left(\dfrac{n_A(D'n_B + (1-D')n_A)}{D'^2}\right)\dfrac{V_g}{R} - \dfrac{V_g}{2}\left(\dfrac{n_A(n_B^2 L_B + L_{AO})}{L_B L_{AO}(D'n_B + (1-D')n_A)}\right)D'^2 T \\ I_B = \left(\dfrac{n_B(D'n_B + (1-D')n_A)}{D'}\right)\dfrac{V_g}{R} + \dfrac{V_g}{2}\left(\dfrac{n_B^2 L_B + L_{AO}}{L_B L_{AO}}\right)D'^2 T \\ I_{AO} = \dfrac{I_A D'}{n_A} \\ V_{AB} = V_g\left(\dfrac{D'n_B + (1-D')n_A}{D'}\right) \\ V_O = V_g\left(\dfrac{D'n_B + (1-D')n_A}{D'}\right) \end{cases} \tag{79}$$

If the $n_A = n_B = n$ and $L = L_{AO} = n^2 L_B$ are imposed, then the operation point equations can be simplified, as can be observed in (80)

$$\begin{cases} I_A = \left(\dfrac{n}{D'}\right)^2 \dfrac{V_g}{R} - \dfrac{V_g}{L}(n\,D')^2 T \\ I_B = \left(\dfrac{n^2}{D'}\right)\dfrac{V_g}{R} + \dfrac{V_g}{L}(n\,D')^2 T \\ I_{AO} = \dfrac{I_A D'}{n} \\ V_{AB} = V_g\left(\dfrac{n}{D'}\right) \\ V_O = V_g\left(\dfrac{n}{D'}\right) \end{cases} \tag{80}$$

According to (80), the relationship between the output voltage and the input voltage of the AIDF converter is n/D', which is similar to the boost converter conversion ratio, although in this case the relationship may be further modified because of the conversion factor n provided by the transformers.

3.3.2.5.1 LINEAR EQUATIONS AROUND THE OPERATING POINT

The state space averaged system of (81) can be expressed as a small signal linear system in the following equation

$$\dot{\hat{x}} = A\hat{x} + B\hat{d}_1 \tag{81}$$

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Where A and B are calculated as in 3.1.1.4.2. The numeric values of these matrices have been obtained with the same converter parameters of the Chapter Two simulations. These are: V_g=10 V, L_A=L_B=L_{AO}=1 mH, C_{AB}= 50 μF, C_O=20 μF, R_L=10 Ω, T=20 μs and D=60%.

$$A=\begin{bmatrix} 0 & 0 & 0 & -400 & 0 \\ 0 & -312500 & 312500 & -460 & 310 \\ 0 & 312500 & -312500 & 1460 & -1310 \\ 8000 & 0 & -20000 & 0 & 0 \\ 0 & 50000 & 0 & 80 & -5080 \end{bmatrix} \quad (82)$$

$$B=\begin{bmatrix} -25000 \\ 69375 \\ -69375 \\ -124360 \\ -8000 \end{bmatrix} \quad (83)$$

3.3.2.6 SMALL SIGNAL TRANSFERS FUNCTIONS

Finally, the small-signal transfer functions can be obtained. The expression in (84) shows the control-to-output transfer function particularized for the same converter parameters used in the last paragraph.

$$G(s)=\frac{\hat{v}_O(s)}{\hat{d}(s)}=\frac{-8\cdot 10^3(s+196600)(s+1617)(s^2-5590s+1228\cdot 10^6)}{(s^2+1957s+2.7\cdot 10^6)(s^2+3088s+2.96\cdot 10^7)(s+6.25\cdot 10^5)} \quad (85)$$

As expected, the transfer function is of the fifth order. All the system poles are in the left half-plane, one of them very far from the origin. There are some zeroes in the right half-plane which will make it difficult to design a control loop for the system.

3.4 SIMULATION RESULTS OF THE AIDB IN TIME DOMAIN

In order to evaluate the performance of the model obtained for the AIDB converter some open loop simulations with PSIM, and MATLAB-SIMULINK were carried out using the following values for the circuit parameters: V_g=10 V, L_A=L_B=L_{AO}=1 mH, C_{AB}= 50 μF, C_O=20 μF, R_L=10 Ω, T=20 μs and D=50%.

In MATLAB, a response to a *1%* duty cycle step was obtained with two models: small and large signal. The matrices of the small signal model (46) calculated using the values of the parameters listed above, are:

$$A=\begin{bmatrix} 0 & 0 & 0 & -5\cdot 10^{-4} & 0 \\ 0 & -2\cdot 10^{-1} & 2\cdot 10^{-1} & -6\cdot 10^{-4} & 4\cdot 10^{-4} \\ 0 & 2\cdot 10^{-1} & -2\cdot 10^{-1} & 16\cdot 10^{-4} & -14\cdot 10^{-4} \\ 1\cdot 10^{-2} & 0 & -2\cdot 10^{-2} & 0 & 0 \\ 0 & 5\cdot 10^{-2} & 0 & 1\cdot 10^{-4} & -51\cdot 10^{-4} \end{bmatrix} \quad (86)$$

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$$B = \begin{bmatrix} -2\cdot10^{-2} \\ 59\cdot10^{-2} \\ -59\cdot10^{-2} \\ 119 \\ -1\cdot10^{-2} \end{bmatrix} \qquad (87)$$

Figure 3.11 shows that the open loop responses of all the variables in the converter have the characteristic behaviour of a dominant RHP-zero system. However the responses reached the steady state in a relatively short time interval.

Figure 3.12 shows the output voltage using matrices A and B. Figure 3.13 shows the large signal model of equation (36) that was implemented in MATLAB-SIMULINK. The output voltage of the large signal model, where the *1%* duty cycle step was applied after *1 ms*, can be observed in Figure 3.14.

Comparing Figures 3.12 and 3.14, it can be observed that the waveforms are very similar and that the output voltage has a final error because the system is in open loop simulation.

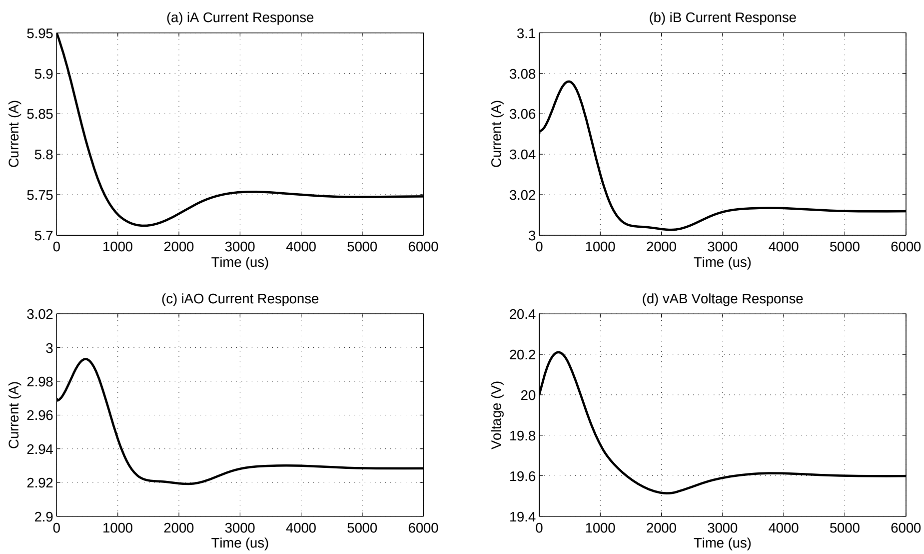

Figure 3.11: AIDB states variables response using the small signal model

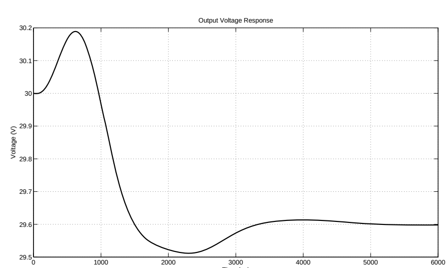

Figure 3.12: AIDB Output Voltage response using the small signal model

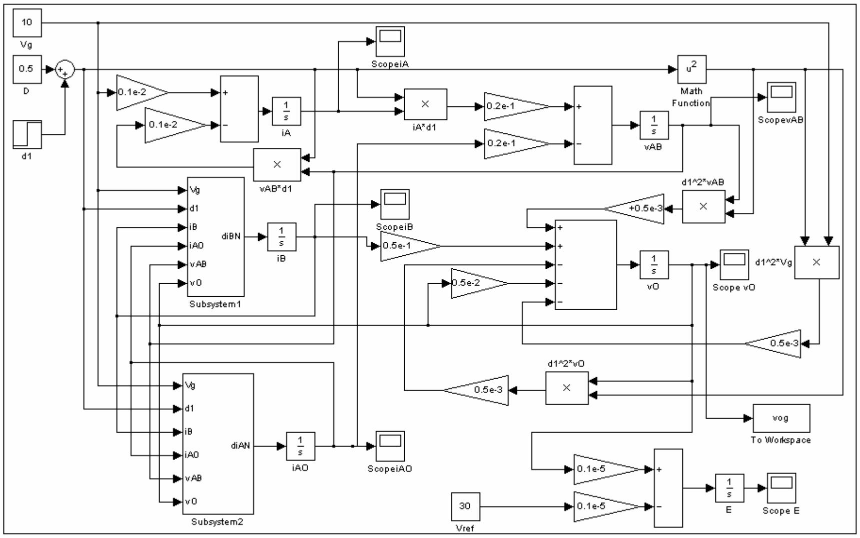

Figure 3.13: Large Signal AIDB Model in MATLAB-SIMULINK

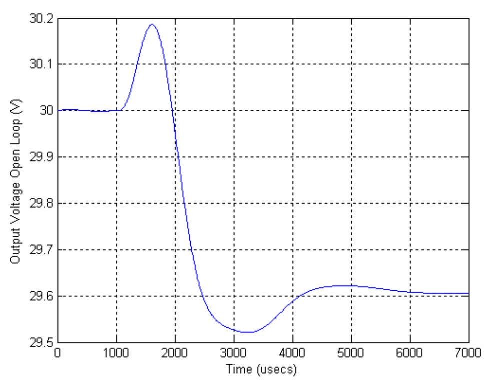

Figure 3.14: AIDB Output voltage response using the large signal model

A PSIM simulation was then carried out using the schematic diagram in Figure 3.15. In this case the *1%* duty cycle step was applied after *6 ms*. The response obtained (see Figure 3.16) matches well with the last two responses. This observation confirms that the converter model is sufficiently accurate because the responses in Figures 3.12, 3.14, and 3.16 are similar, although the models used to obtain these responses are different (these models being the small signal model (MATLAB), the large signal model (SIMULINK) and the PSIM model). This confirms the validity of the new small signal model for the AIDB Converter.

Also, it should be noted that the step signal is applied to d' and not to d, because the control input used to calculate the model was d_1 (d'). Then a *1 %* step in d_1 is equivalent to a *–1 %* step in d, the conventional reference duty cycle, which is why the final voltage is smaller than the initial voltage, although it looks as though the duty cycle was increased.

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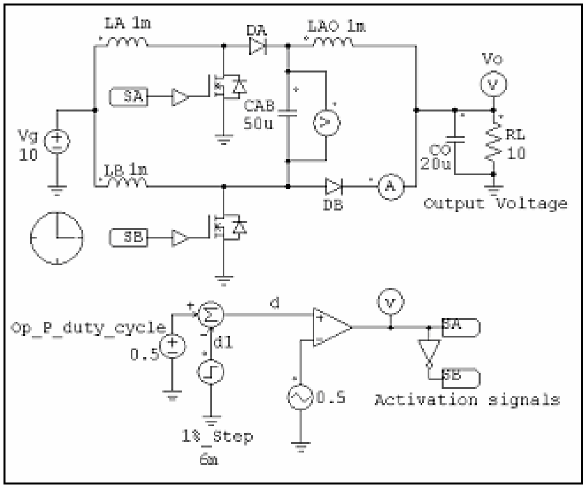

Figure 3.15: PSIM schematic diagram of the open loop AIDB converter

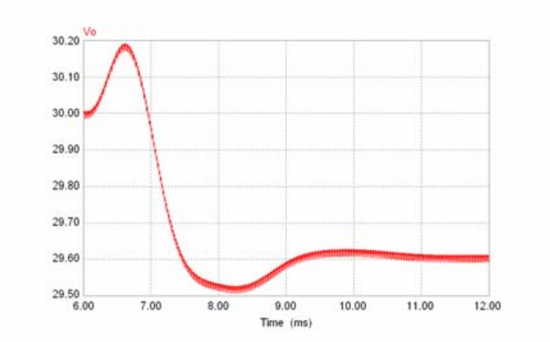

Figure 3.16: PSIM simulation Output voltage response to a *1%* step change in d_1.

3.5 AIDB SIMULATION RESULTS IN FREQUENCY DOMAIN

This section will present the schematics of the simulation results that have already been presented in the Bode diagrams of the first sections.

3.5.1 PSIM SIMULATIONS

Figure 3.17 shows the schematic used for the simulations in the PSIM frequency domain. The figure shows that the element values are the same as those used for the experimental prototype. The PSIM tool AC-Sweep was used to obtain the frequency domain response.

The simulation results using this schematic are shown in Figures 3.3 and 3.6. These results were drawn by loading the simulation results of PSIM in MATLAB.

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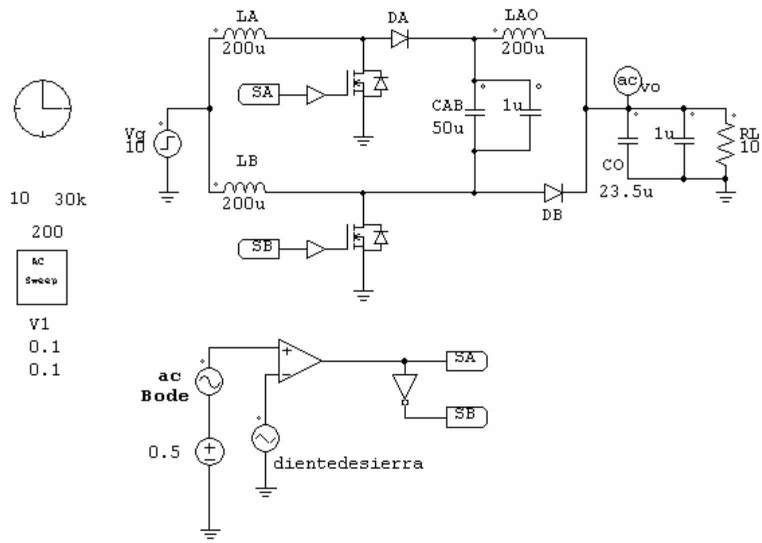

Figure 3.17: PSIM schematic of the AIDB for the frequency domain response

3.5.2 MATLAB SIMULATIONS

The small signal model of equations (46), (47) and (48) was used in MATLAB to obtain the frequency response shown in Figures 3.3 and 3.6.

Figure 3.18 shows another result that can be obtained using the same model: the root locus. The figure shows the location of the zeros RHP that cause the initial behaviour of the responses in time domain.

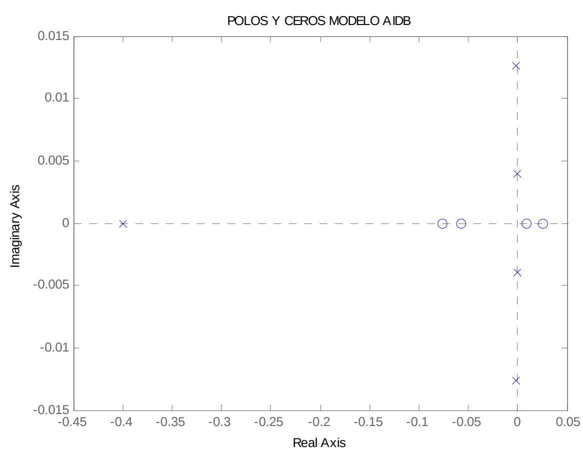

Figure 3.18: Root locus of the AIDB small signal model

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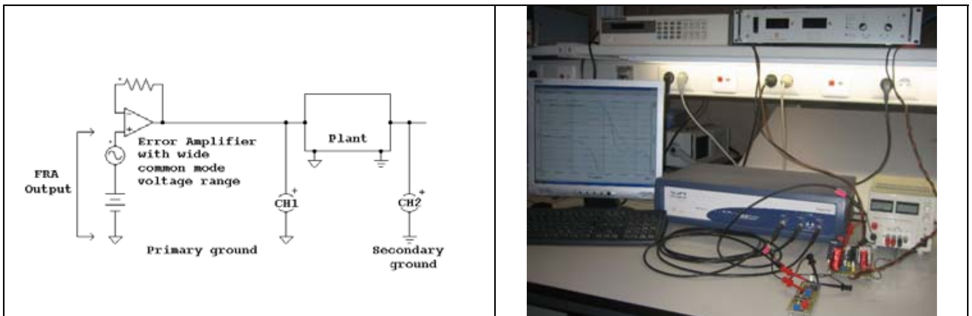
3.6 EXPERIMENTAL RESULTS IN FREQUENCY DOMAIN

The experimental data in frequency domain were obtained with the frequency response analyzer (FRA), following the instruction manual of the equipment and software. The schematic of the interconnection with the plant, in this case the AIDB converter, can be seen in the Figure 3.19a. The figure on the right (3.19b) shows a photograph of the interconnection that was taken in the laboratory.



(a) Schematic of the interconnection (b)Photograph of the interconnection

Figure 3.19: Interconnection between the FRA and the AIDB converter

Figure 3.20 shows the Bode diagram that was taken directly from the FRA using its own software. The comparative graphs between the experimental results obtained with the AIDB prototype and the simulation results obtained with the AIDB models and PSIM have been already shown in Figures 3.3 and 3.6. These figures were drawn by loading the experimental data, which was measured with the FRA in MATLAB.

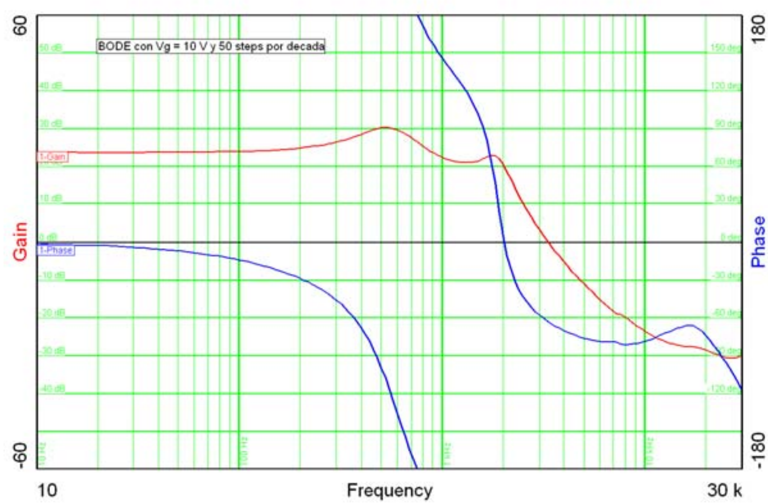


Figure 3.20: Bode diagram of the control-to-output transfer function of the AIDB converter taken directly using the FRA and its software.

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3.7 CHAPTER CONCLUSIONS

The methods proposed in the first chapter are not suitable for some converters in DCM because of their special characteristics, as is the case with the converters in the asymmetrical interleaved family. These characteristics include, for example, the fact that they always have one branch of the circuit in CCM and another branch in DCM, and that the mean value of the currents in the switching intervals are different from the mean values of these state variables throughout the whole operation period.

Therefore, a new conceptual approach was created taking its inspiration from revised averaging and other ideas in previous published papers. This approach was used to arrive at the averaged model.

The approach involves a formal averaging which takes into account the current in the diode that is not a state variable. The inclusion of this current was one of the corrections proposed by the new DCM converter modelling approach. The second correction is a methodology for calculating the second duty cycle.

The procedure for obtaining the new state space averaged system of the AIDB Converter has been explained in detail in this chapter, taking into account the corrections.

Modified averaging using graphical methods was applied to other asymmetrical interleaved converters: AIDBB and AIDF of positive output.

The accuracy of the model was validated by comparing the experimental measures in the frequency domain (obtained with a frequency response analyzer) with the simulations in PSIM and MATLAB. The results of these comparisons were very satisfactory and demonstrated the accuracy of the approximation obtained with the new modelling approach.

One important characteristic of Modified averaging using graphical methods is the possibility of obtaining the linear models of DCM converters that are very difficult to model by other methods.

Another end-result is the creation of a linear and relatively simple model for complex converters.

Finally it ca be said that until now, Modified averaging using graphical methods has only been applied to high order asymmetrically interleaved converters operating in DCM with two simultaneous characteristics: currents with three intervals and two intervals of operation and currents that equal their values in the third interval. Further research could involve applying this method to other high order converters.

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CHAPTER 4

ASYMMETRICAL INTERLEAVED DUAL BOOST: CONTROL DESIGN AND APPLICATIONS

In order to design a practical application of the AIDB converter, it is necessary to obtain a controller that guarantees the regulation of the output voltage in the presence of disturbances.

The improved small-signal linearized model, which was obtained in the previous chapter for the AIDB converter, will be used in this chapter in order to design a controller. As it was explained, this model provides a good approximation to the characteristics of the converter and allows the design of a controller with good performance.

The controller is calculated using the linear optimal quadratic regulator (LQR). An advantage of using this scheme is that the system designed will be asymptotically stable in small signal if it satisfies the controllability condition.

The closed loop performance of the AIDB converter will be verified by simulations using MATLAB, PSIM and SIMULINK.

The final section will discuss the possible applications of the AIDB LQR controlled converter. In general, the possible applications could be extensive and varied. This chapter will study the interconnection with a fuel cell.

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4.1 QUADRATIC OPTIMAL CONTROL

In order to introduce this approach (following [1]), the following system equations have been used:

$$\dot{x} = Ax + Bu \tag{1}$$

The quadratic optimal control scheme is used in designing stable control systems by choosing the control vector $u(t)$ such that a given performance index is minimized. Therefore, the designing problem is reduced to determine the matrix K of the optimal control vector

$$u(t) = -Kx(t) \tag{2}$$

so as to minimize the complex quadratic performance index

$$J = u\int_0^{\infty}\left(x^{*}Qx + u^{*}Ru\right) \tag{3}$$

where Q is a positive-definite (or positive-semidefinite) Hermitian or real symmetric matrix and R is a positive-definite Hermitian or real symmetric matrix. The matrices Q and R determine the relative importance of the error and the expenditure of the energy in the system.

The linear control law given by the equation (2) is the optimal control law. Therefore, if the unknown elements of the matrix K are determined so as to minimize the performance index, then (2) is optimal for any initial state $x(0)$. Figure 4.1shows the block diagram with the optimal configuration.

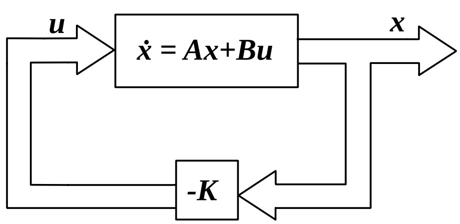

Figure 4.1: Optimal Control System

In order to solve the optimization problem a direct relationship between Liapunov functions and quadratic performance indexes are used. If the second method of Liapunov is utilized to form the basis for the design of an optimal controller, then it can be assured that the system will work; that is, the system output will be continually driven toward its desired value. Thus the designed system has a configuration with inherent stability characteristics but taking into account that the system has to be controllable in order to apply the quadratic optimal control.

The derivations followed to find the matrix K begin with the enouncement of the parameter-optimizing problem, then using the second method of Liapunov the performance index J can be evaluated and minimized, and the result is the reduced-matrix Riccati

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equation that has to be solving in order to find the optimal matrix K. The details of the derivation are outside the scope of this section, but they can be seen in [1].

4.1.1 SOLVING QUADRATIC OPTIMAL CONTROL PROBLEMS WITH MATLAB

The command in MATLAB that solves the continuous-time, linear, quadratic regulator problem and the associated Riccati equation is the following:

lqr(A,B,Q,R)

This command calculates the optimal feedback gain matrix K such that the feedback control law satisfies (2) and minimizes the performance index of (3), subject to the constraint equation (1).

4.2 QUADRATIC OPTIMAL CONTROL DESIGN FOR THE AIDB

The AIDB converter model described in the previous chapter will be used to calculate the linear optimal quadratic regulator (LQR) and thus obtain a controlled system such as that shown in Figure 4.1. This scheme is generally called state feedback, but in this particular case the state feedback gain matrix has been obtained using the minimization methods of the quadratic performance index described in the concepts of the quadratic optimal control [2].

4.2.1 GENERAL ASUMPTIONS

The controllability condition of the model matrices should be verified in order to apply the linear optimal quadratic regulator (LQR) technique. Previous calculations of the controllability condition using the matrices A and B of the state space model for the AIDB converter obtained in the third chapter were useful to verify the need of the matrix normalization. The normalization was made with a change in the time scale:

$$t_N = \frac{t}{10^{-6}} \tag{4}$$

Then the corresponding scale-ups for the inductors and the capacitors are

$$C_N = C \cdot 10^6 \tag{5}$$

$$L_N = L \cdot 10^6 \tag{6}$$

The other parameters are not altered by the time scale.

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4.2.2 CONTROLLABILITY VERIFICATION

Due to the initial difficulties that were presented in the controllability verification for the lack of matrix data normalization, once the system was normalized, the controllability condition was checked by three different methods to assure that the result is correct. MATLAB was used for the application of the three calculation methods.

The numerical values of the AIDB parameters were taken from the Section 2.4: $V_g=10\ V$, $L_A=L_B=L_{AO}=1\ mH$, $C_{AB}=50\ \mu F$, $C_O=20\ \mu F$, $R_L=10\ \Omega$, $T=20\ \mu s$ and $D=50\ \%$. After normalization, the values of the inductors and the capacitors are

$$L_A = L_B = L_{AO} = 1 \cdot 10^3 \tag{7}$$

$$C_{AB} = 50 \tag{8}$$

$$C_O = 20 \tag{9}$$

The numerical system matrixes of the AIDB converter after normalization are

$$A = \begin{bmatrix} 0 & 0 & 0 & -5\cdot 10^{-4} & 0 \\ 0 & -2\cdot 10^{-1} & 2\cdot 10^{-1} & -6\cdot 10^{-4} & 4\cdot 10^{-4} \\ 0 & 2\cdot 10^{-1} & -2\cdot 10^{-1} & 16\cdot 10^{-4} & -14\cdot 10^{-4} \\ 1\cdot 10^{-2} & 0 & -2\cdot 10^{-2} & 0 & 0 \\ 0 & 5\cdot 10^{-2} & 0 & 1\cdot 10^{-4} & -51\cdot 10^{-4} \end{bmatrix} \tag{10}$$

$$B = \begin{bmatrix} -2\cdot 10^{-2} \\ 59\cdot 10^{-2} \\ -59\cdot 10^{-2} \\ 119 \\ -1\cdot 10^{-2} \end{bmatrix} \tag{11}$$

The first method was explained in [3]. This method can be applied when the system has non repeated eigenvalues and uses a transformation to convert matrix A into diagonal (canonical) form, so that the modes of each eigenvalue are decoupled.

The matrix T that transforms the matrix A in a diagonal matrix A_D of its eigenvalues is called the modal matrix. The transformation is the indicated in the following

$$A_D = T^{-1}AT \tag{12}$$

If it is defined this change of variables

$$x = Tz \tag{13}$$

By the substitution of Equation (13) into Equation (1) can be obtained

$$\dot{z} = T^{-1}ATz + T^{-1}Bu \tag{14}$$

Each transformed state z_i represents a mode and can be directly affected by the input $u(t)$ only if B' has no zero row.

$$B' = T^{-1}B \tag{15}$$

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B' is called the mode-controllability matrix. A zero row of B' indicates that the corresponding mode is uncontrollable.

In order to obtain the modal matrix T, the procedure described in [3] will be used. The first step is to obtain the eigenvalues of the matrix A (10). In the following $j=\sqrt{-1}$

$$\begin{aligned} \lambda_1 &= -0.4001 \\ \lambda_2, \lambda_3 &= -0.0015 \pm 0.0053j \\ \lambda_4, \lambda_5 &= -0.0011 \pm 0.0018j \end{aligned} \tag{16}$$

For each λ_i, one adjoint matrix can be calculated (the adjoint matrix is the transpose of the cofactors matrix of the elements of $[\lambda_i I\text{-}A]$)

$$T_i = adj[\lambda_i I - A] \tag{17}$$

The columns of the T_i matrices are linearly related. Therefore, it is only necessary to take one column of every adjoint matrix. If the first column of each Ti corresponding to each eigenvalue is noted by: T_{11}, T_{21}, T_{31}, T_{41}, and T_{51}, then, the modal matrix will be

$$T = \begin{bmatrix} T_{11} & T_{21} & T_{31} & T_{41} & T_{51} \end{bmatrix} \tag{18}$$

Consequently, the modal matrix of the matrix A (10) will be

$$T = 1\times10^{-8}\begin{bmatrix} 0 & -0.5-0.2j & -0.5+0.2j & 0.5+1.7j & 0.5-1.7j \\ -175.4 & 0.7+1.0j & 0.7-1.0j & 0.8+0.3j & 0.8-0.3j \\ 175.4 & 0.7+1.1j & 0.7-1.1j & 0.8+0.4j & 0.8-0.4j \\ 8.8 & -3.2+4.3j & -3.2-4.3j & 7.1+2.1j & 7.1-2.1j \\ 22.2 & 10+0.1j & 10-0.1j & 10 & 10 \end{bmatrix} \tag{19}$$

The diagonal matrix A_D (12) is

$$A_D = 1\times10^{-3}\begin{bmatrix} -400.1 & 0 & 0 & 0 & 0 \\ 0 & -1.5+5.3j & 0 & 0 & 0 \\ 0 & 0 & -1.5-5.3j & 0 & 0 \\ 0 & 0 & 0 & -1.1+1.8j & 0 \\ 0 & 0 & 0 & 0 & -1.1+1.8j \end{bmatrix} \tag{20}$$

A_D satisfies the condition that the elements in the diagonal are the eigenvalues of the matrix A.

Then, the mode mode-controllability matrix B' (15) is

$$B = 1\times10^{5}\begin{bmatrix} -0.3417 \\ -6.7911-2.514j \\ -6.7911+2.514j \\ 6.6681+9.0883j \\ 6.6681-9.0883j \end{bmatrix} \tag{21}$$

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Since matrix B' does not have any zero rows, the system represented by matrixes A (10) and B (11) is completely state controllable.

The second method was based on the similarity transformation and can be applied using the following MATLAB commands

$$[A,B,C,T,k] = \mathrm{ctrbf}(A,B,C)$$

$$\mathrm{number\_controllable\_states}=\mathrm{sum}(k)$$

The command ctrbf(A,B,C) decomposes the state-space system represented by A, B, and C into the controllability staircase form. T is the similarity transformation matrix and k is a vector of length n, where n is the order of the system represented by A. Each entry of k represents the number of controllable states factored out during each step of the transformation matrix calculation. The number of nonzero elements in k indicates how many iterations were necessary to calculate T, and the addition of the elements in vector k is the number of the controllable states.

This second method provides five controllable states, therefore the system represented by matrixes A (10) and B (11) is completely state controllable.

The third method simply calculates the controllability matrix and obtains its rank using MATLAB:

$$Co=\mathrm{ctrb}(A,B)$$

$$\mathrm{rank}(Co)$$

If the rank of the controllability matrix is equal to the order of matrix A, then the system is completely state controllable. This is the case for matrixes A (10) and B (11).

The results obtained by the three methods confirm that the AIDB converter model represented by matrixes A (10) and B (11) is completely state controllable as is usually the case in a switching converter. Consequently, a linear quadratic optimal regulator can be calculated for the converter model.

4.2.3 LAST STATE EQUATION

A sixth state variable, the integral of the error, has been added to the system to guarantee zero error in steady state. Therefore, the last state equation will be:

$$\frac{\mathrm{d}\bar{e}}{\mathrm{d}t} = \bar{v}_{\mathrm{O}} - V_{ref} \tag{22}$$

Where *Vref* is the reference voltage, that is, the desired steady-state value for the output voltage, because of the parameters used, *Vref=30 V*.

4.2.4 CALCULATION OF THE LINEAR QUADRATIC REGULATOR

The feedback vector gains (2) *Ki* (*i=1…6*) for the optimal quadratic control are obtained using the MATLAB command

$$[K,S,e] = \mathrm{lqr}(A,B,Q,R)$$

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This command provides the solution to the Riccatti equation in continuous time (matrix S), determines the optimal feedback matrix gains (vector K) and the closed loop poles location (vector e).

The matrices Q and R of the performance quadratic index (3) are usually selected by the designer using his knowledge of the system, and are tested by trial and error by MATLAB simulation.

For this case, the matrices Q and R have been defined taking into account energy considerations and the relative weight of the output variable and the error. In this way, the following coefficients can be defined:

$$\begin{bmatrix} QI_A = (5.95)^2 \times 1 \\ QI_B = (3.05)^2 \times 1 \\ QI_{AO} = (2.97)^2 \times 1 \\ QV_{AB} = (20)^2 \times 50 \times 10^{-3} \\ QV_O = (30)^2 \times 20 \\ QE = 1 \times 10^{10} \end{bmatrix} \tag{23}$$

Because the Q matrix is related to energy expenditure, the initial value of the coefficients in (23) was taken from the stored energy equation of the capacitors and inductors:

$$E_C = \frac{1}{2}CV^2, E_L = \frac{1}{2}LI^2 \tag{24}$$

The voltages and currents that appear in the equations were the values of the operation point of the AIDB converter, which were calculated in the second chapter. The starting point for this calculation, this is (23), was chosen because this LQR is calculated for a specific operating point, since it was used the small-signal model of the AIDB converter.

Therefore, it was demonstrated by the fact that the definition of the matrix Q taking into account the energy at the point of operation provided better results than other initial values that were tried.

In order to give a greater weight to the variables of most interest, the output voltage and the derivative of the error, some changes in the coefficients were made by trial and error and the final matrix Q is:

$$Q = \frac{1}{\mathrm{QV_O}} \begin{bmatrix} QI_A & 0 & 0 & 0 & 0 & 0 \\ 0 & QI_B & 0 & 0 & 0 & 0 \\ 0 & 0 & \mathrm{QI_{AO}} & 0 & 0 & 0 \\ 0 & 0 & 0 & \mathrm{QV_{AB}} & 0 & 0 \\ 0 & 0 & 0 & 0 & \mathrm{QV_O} & 0 \\ 0 & 0 & 0 & 0 & 0 & \mathrm{QE} \end{bmatrix} \tag{25}$$

The matrix R must be small enough for a fast correction of the perturbations.

$$R = [1] \tag{26}$$

Using the lqr instruction the following vector was obtained:

$$K = \begin{bmatrix} -3.79 & 0.12 & 0.10 & -0.40 & 0.31 & -745 \end{bmatrix} \quad (27)$$

This vector will be used in the feedback simulations schemes.

4.3 CLOSED LOOP SIMULATION RESULTS

The closed loop performance of the AIDB converter will be verified using MATLAB-SIMULINK and PSIM simulations. The models for the AIDB in large signal and small signal obtained in the third chapter are simulated in MATLAB-SIMULINK with a LQR feedback loop.

The schematics in PSIM also include the feedback loop and PSIM uses its own modelling method for the simulations. In this way, it is possible to compare the results obtained with the three models of the AIDB converter circuit [2].

4.3.1 SIMULATIONS WITH THE SMALL SIGNAL MODEL

The simulations in MATLAB-SIMULINK use the small signal model of the AIDB converter that was calculated in the third chapter (3.1.2.5.3) but with the same parameter values that were used to verify controllability (4.2.2).

An advantage of using the quadratic optimal control scheme is that the system designed is stable, except for when it is not controllable. However, in this case the system satisfies the controllability condition. Consequently, one of the objectives of the simulations is to verify stability in all the state variables.

The only parameter that affects all the state variables at the same time is the duty cycle. Then the disturbance is caused by introducing a step of *10 %* in the duty cycle, which allows us to observe how all the state variables respond to a disturbance.

It should be noted that the step signal is applied to d' and not to d, because the control input used to calculate the model was d_1 (d'). Then, according with the equation (19) of the Chapter Three, a *10 %* step in d1 is equivalent to a *–10 %* step in the conventional reference duty cycle d. In order to observe the response of the controlled system around the operating point, the following initial conditions were used in the simulations: are the operating point ($D=50\ \%$; $I_A=5.95\ A$; $I_B=3.05\ A$; $I_{AO}=2.97\ A$; $V_{AB}=20\ V$ and $V_O=30\ V$).

Figure 4.2 shows the output voltage response $v_O(t)$ of the circuit to a *10 %* step in d'. The figure shows the performance of the linear quadratic regulator (LQR). The small signal component of the duty cycle is correctly adjusted by the controller to compensate for the initial error of the output voltage $v_O(t)$ and the final error is close to zero. The dominant zero RHP of this transfer function meant that the voltage response initially increases despite the fact that the disturbance was applied in the complementary duty cycle.

The response of other state variables can be seen in Figure 4.3, which verifies the stability and the null error in the steady state of all the variables of the controlled system.

The system responses are considered good enough given that this is the first attempt to design a control using the new model calculated for the converter. Further development of the control design could include transient response requirements in order to improve the responses

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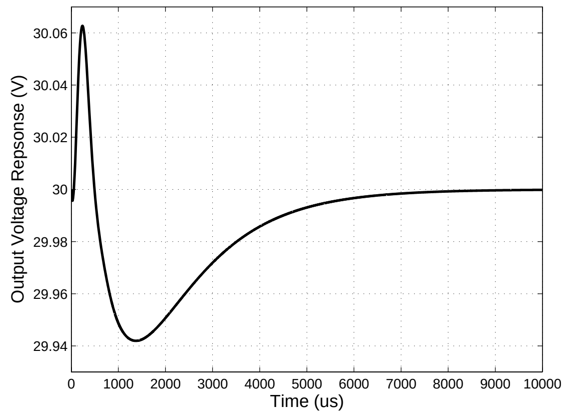

Figure 4.2: Output voltage response of the LQR controlled AIDB converter calculated with the small signal model

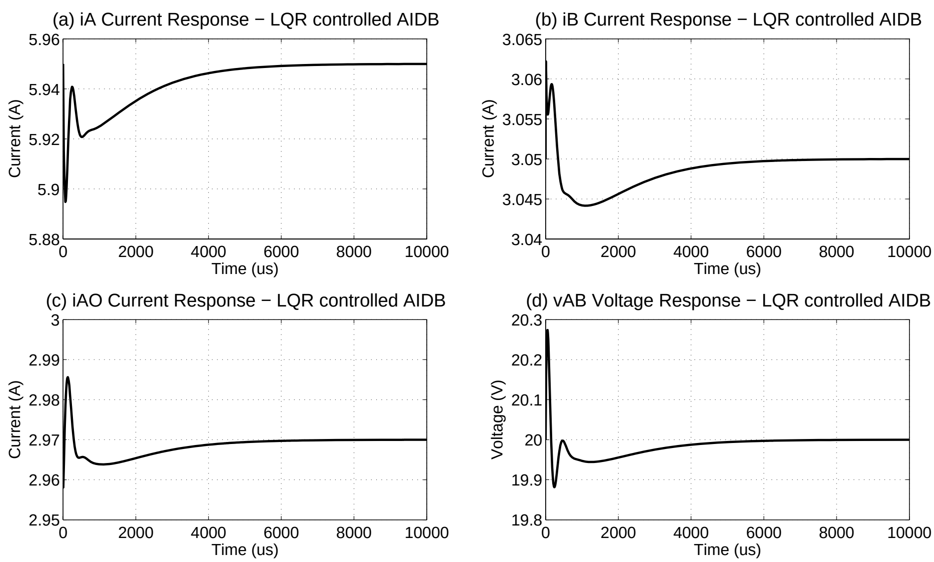

Figure 4.3: State variables response of the LQR controlled AIDB converter calculated with the small signal model

4.3.2 SIMULATIONS WITH THE LARGE SIGNAL MODEL

Given that the stability of all the state variables' response has already been verified in the previous section, the large signal model simulations aim to verify the operation of a controller that has been calculated with the small signal model.

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Figure 4.4 shows the large signal model of the AIDB converter that was implemented in SIMULINK. The figure also shows the feedback of the state variables by the control law in the form of an LQR that was calculated using the AIDB converter small signal model linearized around an operating point (in this case $D=50\%$).

Figure 4.5 shows the result obtained. The circuit is initially in the operating point ($D=50\ \%$ and $V_O=30\ V$). According to the explanation of last section, the same step disturbance in the duty cycle is applied ($d_1=10\ \%$ and $d=-10\ \%$) in order to obtain the voltage response. In this case the step is introduced $2\ ms$ after the initial time of the simulation.

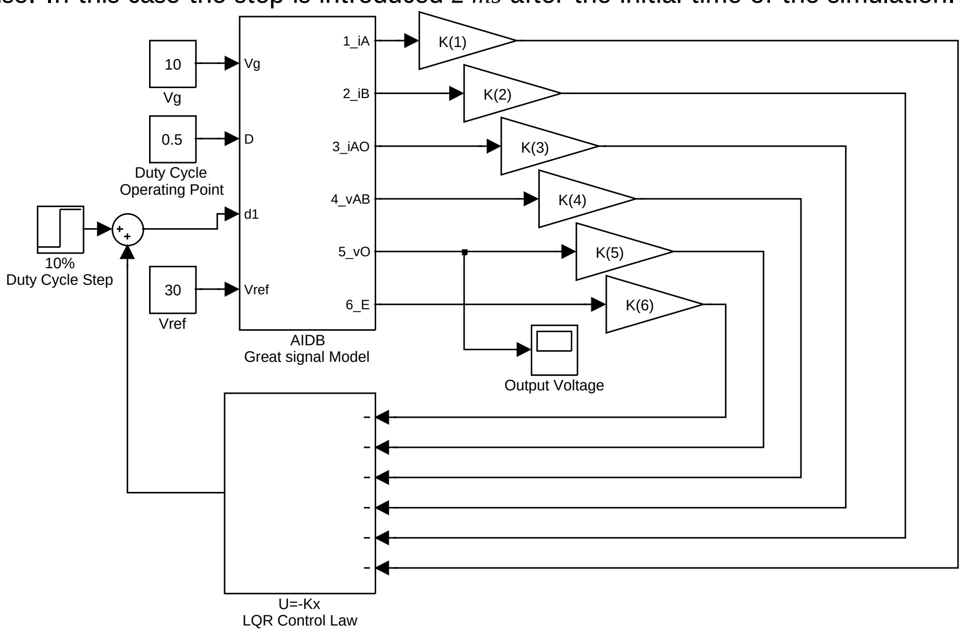

Figure 4.4: SIMULINK block diagram for the LQR feedback system with large signal model

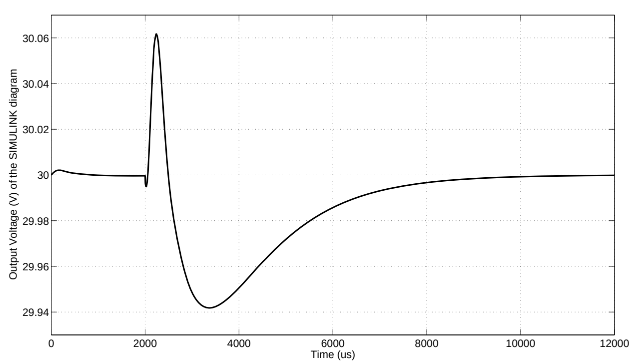

Figure 4.5: Output Voltage response of the SIMULINK block diagram for the LQR feedback system with large signal model

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The response of the model in SIMULINK is very similar to the previous response. It can also be seen that the control is working properly because the output voltage goes back to its operating point value after the transient.

Thus, the accuracy of the model used for calculating the LQR control law is demonstrated by the correct operation of the controlled system and the good response of the system to a large signal perturbation in the duty cycle.

4.3.3 PSIM

Figure 4.6 shows the schematic of the AIDB converter in closed loop with the LQR calculated in 4.2.4. All variables show the subtraction of the operation point because the controller was calculated with small-signal variations on the state variables of the AIDB converter.

Figure 4.7 shows the output voltage of this circuit, which has the same shape as those in the other simulations; however, in this case it shows the ripple of the output voltage due to the simulation algorithm of the PSIM.

It is important to take into account that this controller design was made to obtain a stable state variables response to a disturbance and to verify the good performance of the small signal model of the converter. Both objectives were achieved because the controller of the plant designed with the model demonstrated its effectiveness, although the plant has experienced some control difficulties such as the zero on the right semi-plane of a very low frequency which imposes a limit on the bandwidth.

It is important to note that there are only five variables in the feedback because the output response began to swing if the V_{AB} voltage was included. This behaviour may be due to an algorithm limitation in the simulator, in this case the PSIM. The fact that it is not necessary to include all the state variables in the closed loop simulations so that it operates correctly was the starting point for the simplification of the circuit.

In order to make a future experimental mounting of the LQR controlled AIDB converter, it was made more simulations (Figure 4.8) till finding that was only necessary the feedback of two variables: the current i_A and the integral of the error. This was because the response of the circuit, i.e. the output voltage, still behaved well with the feedback of these two variables (Figure 4.9). In this way, it would require to sense only two variables in the experimental mounting: the current i_A and the output voltage v_O, which is very convenient as it facilitates the measurement and achievement of the operation of the circuit.

4.4 Applications of the family of asimmetrical interleaved converters

Possible applications of this family should take advantage of its best qualities. For example, the low ripples in the input current and output voltage can reduce the conducted EMI and be useful in automotive electronics, amongst other areas.

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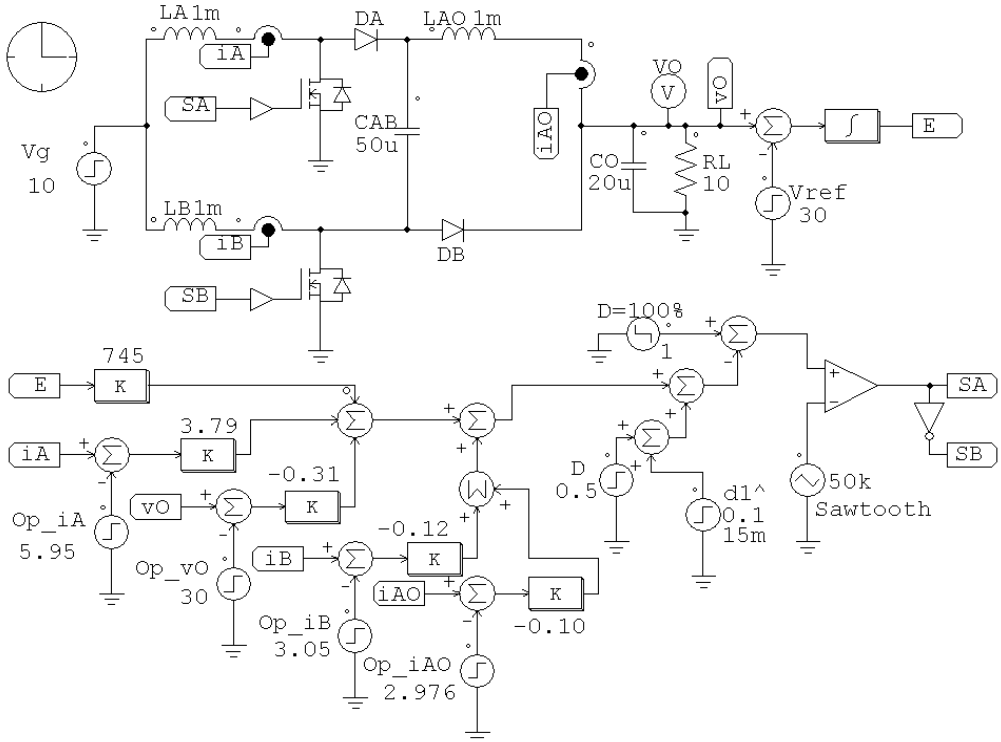

Figure 4.6: PSIM schematic of the AIDB converter in closed loop with a LQR

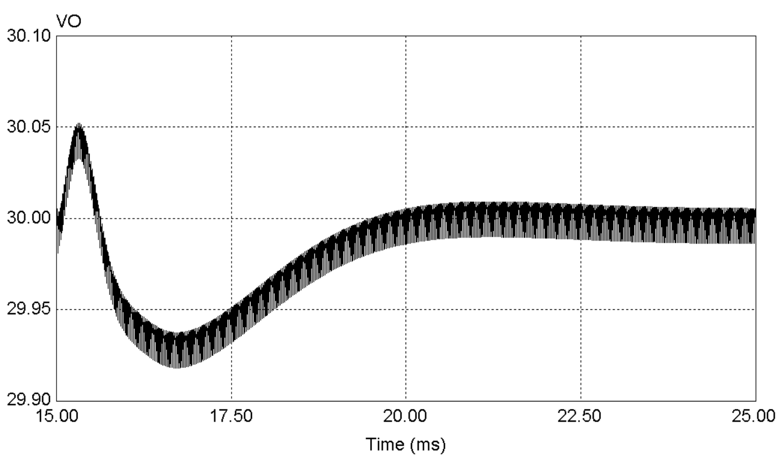

Figure 4.7: Output Voltage response of the PSIM schematic for the AIDB converter in closed loop

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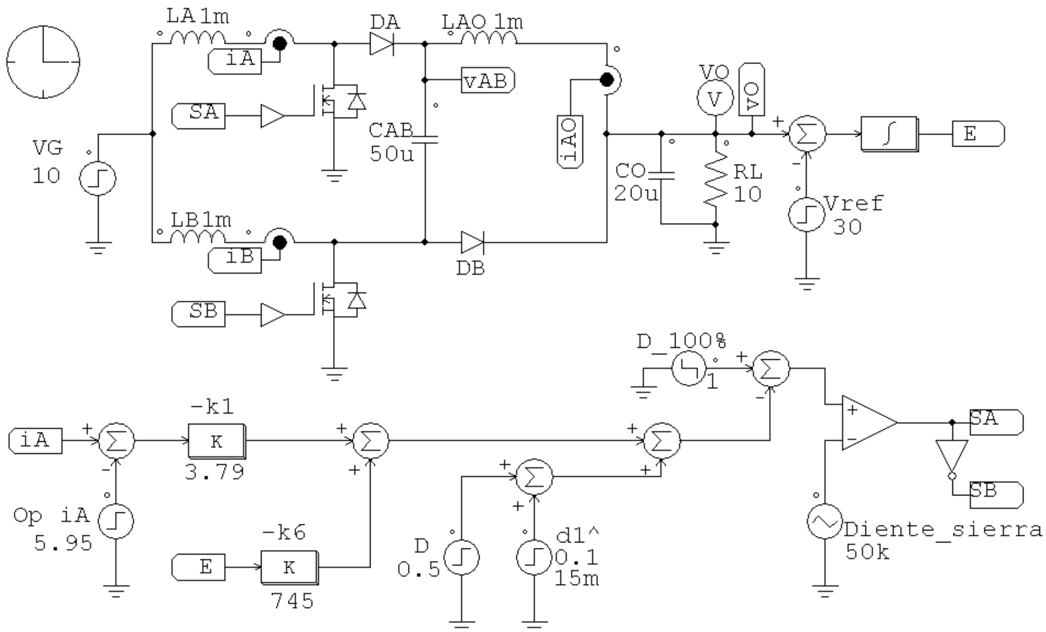

Figure 4.8: PSIM schematic of the AIDB converter in closed loop with only two variables in feedback

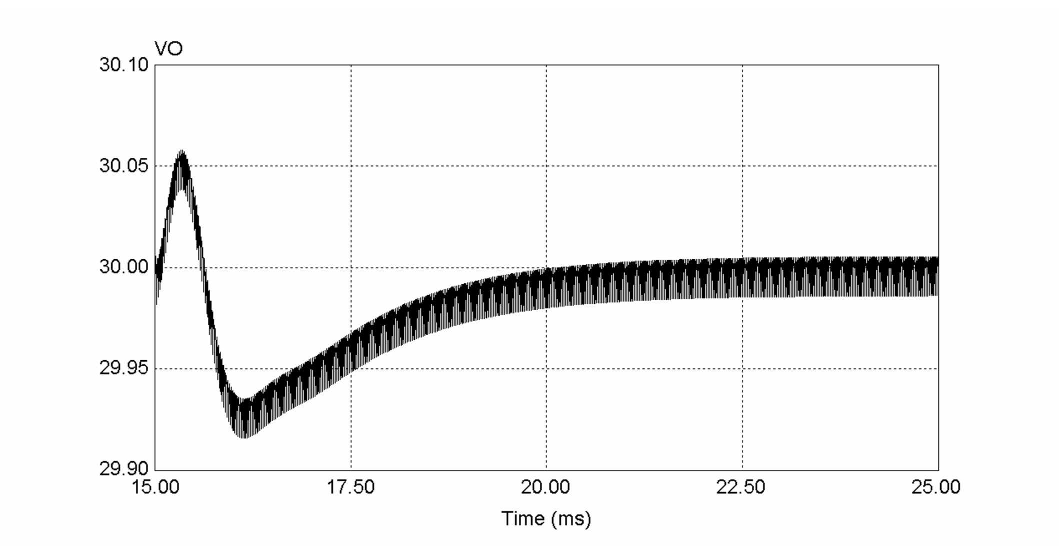

Figure 4.9: Output Voltage response of the PSIM schematic for the AIDB converter in closed loop with only two-variables feedback

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The AIDF-group has the additional advantage of wide range conversion with or without reverse polarity, and this could be useful in applications requiring high elevation or reduction of voltage with or without isolation.

In general, the possible applications could be extensive and varied. In this case the feature of low-ripple in the input current of the AIDB has been used to interconnect it with a fuel cell. The fuel cell imposes the condition of the high frequency low ripple in current because in other case it may offer a poor efficiency and even physical damages.

4.4.1 FUEL CELL SYSTEM MODEL

The fuel cell is a new efficient and clean electric power generator. Figure 4.10 shows a scheme of the basic operation principle of the Proton Exchange Membrane Fuel Cell (PEMFC), which uses hydrogen and oxygen to generate electricity.

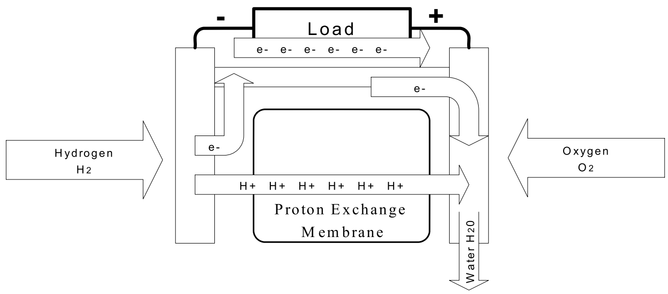

Figure 4.10: Basic operation principle of a PEM Fuel Cell.

A short explanation of the operation of the PEM fuel cell, its the model and the verification of the properly behaviour of the model are explained in [4] and the references cited in that work. Here they are not included because are out of the scope of this chapter.

4.4.2 INTERCONNECTION OF THE AIDB AND A FUEL CELL

The AIDB converter was initially designed without any specific application in mind. Thus, the criteria for choosing the converter parameters were that the simulation results should be easy to observe in order to determine how the converter operates. The values of the elements for the experimental prototype were chosen using the same criteria.

The stability of the state variables was the control objective in the design of the LQR. The integrator was added to ensure zero error in steady state in the output voltage. This means that the control was designed with no specific application in mind.

The initial design criteria have been useful for characterizing the AIDB converter because it is a new circuit that has not been tested before. However, if a specific application had been chosen from the beginning, the plant and the control would had been designed using very different criteria that could be strongly dependent on the selected application.

It was suggested the exploration of possible applications for the AIDB LQR controlled converter system without making changes in either the initial plant or control. The goals

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proposed were simply to verify some performance characteristics and to see if the use of the AIDB converter could be feasible.

The initially proposed application was the interconnection with a fuel cell by its need of low ripple in the converter input current, which is one of the advantages of the AIDB that can be observed in the Figure 2.11 of the second chapter.

With this in mind, the SIMULINK model of the fuel cell (which had already been tested by other authors cited in [4]) was interconnected with the SIMULINK model of the AIDB controlled converter.

The main objective of this interconnection was to verify the converter operation with an approximate model of a real source with very specific characteristics. The simulation results can be seen below.

The simulations indicate that the stack is forced to modify its operation point for the sole purpose of verifying the operation of the converter control.

Figure 4.11 shows the whole energy generation and conversion fuel cell system. The AIDB converter input current I_g is used to generate the states of the fuel cell model, (*I Stack*: stack current in Fuel Cell system). These states generate the output voltage of the stack (*V Stack*: Stack Voltage in Fuel Cell system), that is being used as the voltage source V_g for the LQR controlled DC-to-DC AIDB converter.

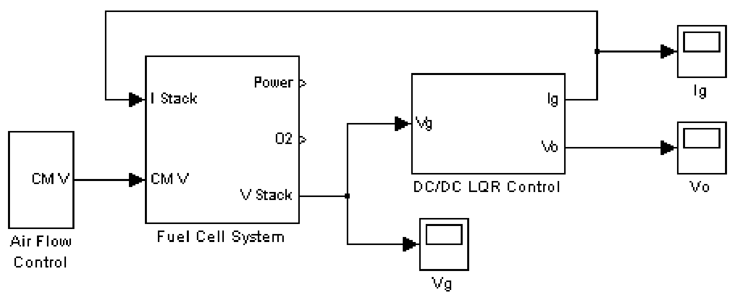

Figure 4.11: Block diagram of a fuel cell system coupled with a LQR controlled AIDB converter

4.4.3 SIMULATION RESULTS

The simulation starts at one converter operation point ($D=50$ %, $V_O=30V$) in order to verify only the system response in the presence of perturbations. It has been assumed that the disturbances in the feeding of the fuel cell reagents have been generated by some unspecified external cause. These disturbances are reflected in the variation of the fuel cell output voltage (Stack Voltage) which in turn generates a variation in the fuel cell input current (Stack Current) and therefore in the converter input current. The simulation results can be seen in Figure 4.12.

Figures 4.12(a) and (b) show the variations in the source current (Stack Current) and the source voltage (Stack Voltage) of the converter respectively. The wide variations in these waveforms mean that the controlled converter must be operated properly.

Figures 4.12 (c) and (d) exhibit the response of the converter. Figure 4.12(c) shows that the LQR controlled AIDB converter has responded well to quite complicated regulation test

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of because the output voltage remains in the small band of operation despite the wide variation in the input signals.

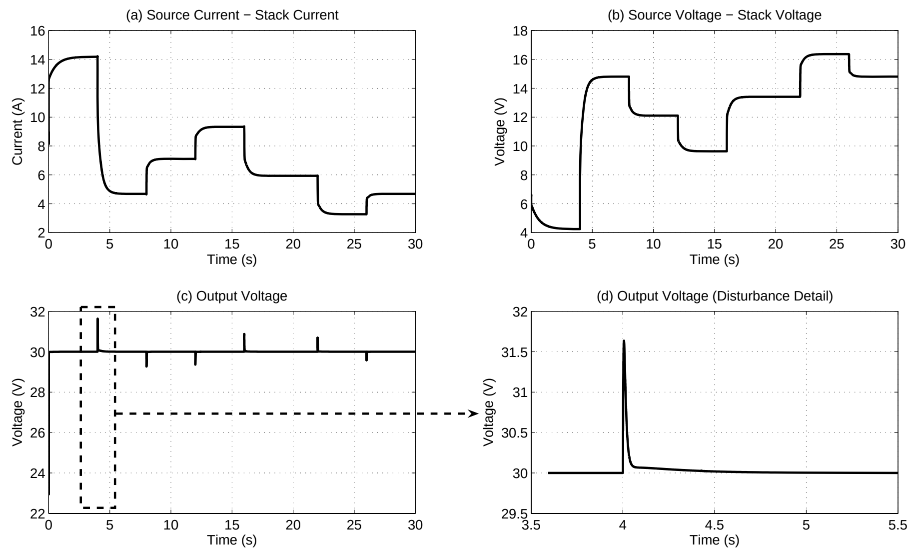

Figure 4.12: Simulation responses of the Fuel Cell energy generation coupled with a LQR controlled DC-to-DC AIDB converter.

Figure 4.12(d) provides the details of the LQR controlled AIDB converter's output voltage response to a disturbance in the whole system. The waveform has zero error in the steady state and the speed of the response is quite good. Nevertheless, it can be seen that the control was not designed to improve the transient response because the output voltage response of the converter is regulated, robust and stable, although it has some peaks that show the low optimization of the input-to-output transfer function's audio-susceptibility. This could be improved by designing the control and the converter specifically for this application.

Finally, it can be concluded that the response of the whole system has some interesting features such as regulation, speed of response, robustness, stability and zero steady state error, although the audio-susceptibility should be improved. That could be achieved by designing the converter and the control for one specific application. Further research, therefore, could be the design of a controlled converter system for specific application in fuel cells.

The design of such an application should take into account that the improved DCM model of the AIDB converter calculated in the last chapter offers a very good approximation of the converter's behaviour at high-frequencies. The variable that permits this feature of the model to be used is the input current because the output voltage has a dominant RHP zero in its transfer function that limits the band-with of a controller. One possible application of this feature would be the design of a battery charging system in which a current control would optimize the response of the AIDB converter input current.

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4.5 CHAPTER CONCLUSIONS

The first topic of this chapter looked at the design of an LQR controller for the AIDB converter using the improved small signal model described in the third chapter.

The MATLAB command "lqr", that gives the solution to the continuous-time Riccati equation and determines the optimal feedback gain matrix, was used in the design of the controller based on the minimization of quadratic performance indexes.

An advantage of using the quadratic optimal control scheme is that the system designed will be stable, unless it is not controllable. However, in the case of the AIDB converter, it was demonstrated that the system was controllable.

The controller was designed so that the variables gave a stable state response to a disturbance and so that the performance of the small signal model of the converter could be verified. That both these objectives were achieved is demonstrated by the effectiveness of the controller of the plant that was designed using this model, although the plant has had some control difficulties such as the bandwidth limit imposed by the very low frequency zero RHP.

Nevertheless, this was the first control design approach to use the new model calculated for the converter. Leading on from this research, the next controller design could include transient response requirements to improve the responses.

The second topic of the chapter reviewed possible applications for the asymmetrical interleaved converter family. This review took into account these converter's main advantages, such as low ripples in the input current and output voltage. In this case, the low-ripple in the AIDB input current has been used to connect the converter with a fuel cell.

The interconnection was made between the SIMULINK model of the fuel cell, which had already been tested by other authors cited in [4], and the SIMULINK model of the AIDB controlled converter. The simulation results permitted an initial verification of the converter operation with a real source model. The LQR controlled AIDB converter responded well enough because its output voltage remained within a small operating band despite the wide variation in the input signals.

To conclude, it can be said that the response of the whole interconnected system has some interesting features such as regulation, speed of response, robustness, stability and zero steady state error, although its audio-susceptibility should be improved. This could be achieved by specifically designing the converter and the control for the intended application. Further research could involve designing a controlled converter system for a specific application with fuel cells.

Other research arising from this chapter could use the improved approximation of the AIDB converter's behaviour at high-frequencies in the DCM model to design an application that optimizes the input current response.

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CONCLUSIONS

The two main topics that have been studied in this thesis were the generation of new family of switching converters and the modelling of a new mathematical approach by which these could be analyzed.

The first chapter of this thesis was an exhaustive review of the modelling methods applied to DC-to-DC PWM converters operating in CCM and DCM modes. This review provided the knowledge needed to develop the new modelling approach that is presented in this thesis.

Detailed study of the different methods for modelling DC-to-DC switching converters showed that the latest approaches use the simulated waveforms of certain circuital variables to obtain any relationship between them that are useful for calculating models, specifically if the converter circuit is working in DCM mode.

Another conclusion from this chapter is that modelling the high order structures in other DCM modes such as DVCM, DQRM and MDM is an open research field because all these approaches have been applied to the three basic structures operating in DICM.

In the second chapter, interleaving was presented as an alternative strategy for generating new converters by combining known basic converter structures and control techniques, but interconnecting them in complementary interleaving, thus improving the resulting circuit. This concept led to the development of the first important contribution of this thesis: the family of asymmetrical interleaved converters consisting of the AIDB, AIDBB and the AIDF-Group.

The methodology followed in order to generate the new converter structures can be called circuit structure modification and it is based on simulation results and on the fundamental idea of breaking the symmetry.

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The first important characteristic of the converter family is that it inherently operates in DCM. The second is that the unbalanced sharing of the input current between the two branches of the circuit takes place without any specific control strategy and reduces the aggregated input current ripple caused by operating in DCM. Other features of this new converter family are the considerably improved input-to-output voltage transfer ratio of the AIDB, the low output voltage ripple that tends to zero as the duty cycle increases, the length of the operation intervals in steady state that do not include the parameters of the circuit, the low input current ripple in the AIDBB, the wide range of conversion ratios and the possibility of reversing the polarity in the AIDF family because of the use of transformers.

The experimental results obtained with the AIDB converter prototype confirm that the converter has two operation regions. This is demonstrated by the differences between the shapes and values of the waveforms for a duty cycle of *38 %* and the waveforms for duty cycles greater than *38 %*. The numerical results obtained by experimental testing confirmed the good results in terms of ripples and mean values obtained in the simulations of the converter variables.

The third chapter presented a new conceptual modelling approach, inspired by the concept of revised averaging and the findings of other studies. This approach was used with the converters in the asymmetrical interleaved family in order to arrive at the averaged model. This family of converters has some special features that make the methods studied in the first chapter unsuitable. These features are the high order of the converters and the fact that the operation in DCM has two simultaneous characteristics : three and two intervals currents and currents that equal their values in the third interval.

The new approach was called modified averaging using graphical methods, and it proposes two main corrections: a formal averaging process that takes into account the current in the diode, which is not a state variable, and a different methodology for calculating the second duty cycle.

This new modelling approach was used to obtain the state space averaged system of the AIDB, AIDBB and positive output-AIDF converters.

The accuracy of the model was validated by comparing the frequency response calculated using the model with the PSIM and the experimental data of the Frequency Response Analyzer. The results of these comparisons demonstrated the accuracy of the approximation obtained with the new modelling approach.

The Modified averaging using graphical methods was used to find a linear model of converters in DCM that could not be modelled in any other way. The end-result is a linear and relatively simple model even for such complex converters. Therefore, the application of this method to other high order converters operating in DCM is another open research line leading on from this thesis.

In Chapter Four, an LQR controller for the AIDB converter was calculated using the improved small signal linearized model. The design of the controller had two objectives, both of which were achieved: to ensure a stable state variable response to a disturbance and to verify the good performance of the AIDB converter small signal model.

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Nevertheless, this was the first approximation of a control design using the new model. The AIDB model could be used in future research in this area in order to calculate another controller that takes into account transient response requirements to improve the responses.

In the second topic of the fourth chapter, the low-ripple feature in the input current of the AIDB has been used in the interconnection of the converter with a fuel cell.

The interconnection was made between the SIMULINK model of the fuel cell and the SIMULINK model of AIDB controlled converter. The simulation results have verified good characteristics in the response to disturbances of the LQR controlled AIDB converter. The most interesting are the regulation, the speed of response, the robustness, the stability and the zero steady state error. The response remains within a small band of operation despite the wide range of variation in the input signals; however the audio-susceptibility has to be improved.

This improvement could be achieved if the converter and the control are specifically designed for the intended application. For example the converter structure could be modified to solve the problem of zero RHP.

These results mean that another line of research continuing from this thesis could be the design of a controlled converter system for a specific application in fuel cells.

Other lines of research could also look into constructing experimental prototypes of the other converters, in particular the AIDB controlled converter and the AIDF because these could have a wide range of applications.

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ANNEX: LIST OF PUBLICATIONS

[1] **E. Arango**, C. Ramos, J. Calvente, R. Giral, A. Romero, and L. Martinez, "Fuel Cell Power Output Using a LQR Controlled AIDB Converter," in IEEE ICCEP Conference Proceedings, Capri, 2007.

[2] **E. Arango**, J. Calvente, R. Giral, A. El Aroudi, and L. Martinez-Salamero, "LQR control of an asymmetrical interleaved boost converter working in inherent DCM," in IEEE ISIE Conference Proceedings, Dubrovnik, 2005, vol. 2, pp. 721-726.

[3] **E. Arango**, R. Giral, J. Calvente, and L. Martínez, "Convertidores Tipo Flyback Dual En Interleaving Asimétrico (AIDF)," in SAAEI'04 - EPF'04 Conference Proceedings, Toulouse, France, 2004, vol. OS-4, p. N. 163.

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