Departament d'Enginyeria Electrònica

UNIVERSITAT POLITÈCNICA DE CATALUNYA

Universitat Politècnica de Catalunya

Departament d'Enginyeria Electrònica

Design of Frequency Divider with Voltage Controlled Oscillator for 60 GHz Low Power Phase-Locked Loops in 65 nm RF CMOS

Dissertation for the Ph. D. Degree submitted by:

Davide Brandano

Thesis Advisor: Jose Luis González Jiménez

Commissariat à l'Energie Atomique et les Energies Alternatives (CEA)
Laboratoire de l'Electronique et la Technologies de l'Information (LETI)
MINATEC Campus, Grenoble, France

I hereby certify that the work presented in this thesis is my own and that work performed by others is appropriately cited.

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SUMMARY

Increasing memory capacity in mobile devices, together with the transition to wireless connections for consumer electronics and PC products, is driving the need for wireless equipment with data rates of up to 10 Gbits/sec.

The worldwide 7 GHz unlicensed band around 60GHz provides the opportunity for multi-gigabit *persecond* wireless communication and it is a real opportunity for developing next generation of Wireless High-Definition (WirelessHD[TM1]) devices. The notation WirelessHD[TM] has recently replaced the first definition of Wireless High-Definition Multimedia Interfaces (WHDMIs) for the frequency range around 60 GHz, as shown in Figure 1. The HDMI by wire, where it already exists, can be replaced by wireless systems transmitting uncompressed video streaming from DVD players, or from PCs to TV or monitor. Other applications are regarding cellular phone, or *smart* phones: considering an hypothetical 60 GHz enabled smart phone (i. e. Android, Iphone, *etc*.), which uses the 60 GHz connection to download movies from a stand (i.e. airport, train station, etc.), transmits audio/video to a larger screen for better viewing, and connects to several external and wireless peripherals (i.e. hard disk, optical networks, *etc*.). In this scenario, with reasonable low power consumption using inexpensive silicon technology like CMOS, it is possible to say that such phone with that capability can truly replace the laptop computer.

On one hand, addressing 10 Gbits/sec data speed with current standard Wi-Fi at 5 GHz will require extremely complex base-band modulation systems. Moreover, tight regulation specifications exist for this band, making it unlikely to be able to operate with 10 Gbits/sec at 5 GHz: current WirelessHD[TM] products that utilize the 5 GHz unlicensed spectrum have the critical drawback of the limited bandwidth. As a consequence, these systems implement lossy or lossless compression, dramatically adding components, design cost and product size. On the other hand, the nascent UWB technology could be a better

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[1] The frequency band requirement for the WirelessHD[TM] has been obtained from public documents available in Internet (e.g. http://www.ieee802.org/15/pub/TG3c.html), since neither UPC nor CEA-Leti are members of the WirelessHD[TM] Consortium.

solution, but it has some drawbacks including interference problems, limited data rates and limited SNR due to limited transmit power.

From Shannon theory, it is know that a way to increase communication data rate is to utilize more bandwidth. Since the information signal is usually modulated around a carrier frequency for proper propagation, the higher the carrier is, the more bandwidth is available for propagation: selecting the 60 GHz band will offer the benefits of 7 GHz unlicensed bandwidth with few regulatory specifications.

The actual allocated bandwidth at 60 GHz varies from country to country as shown in Figure 1. However, there is an overlap bandwidth of 3 GHz within the 60 GHz band which is available worldwide. The 60 GHz frequency also allows for small form factor antennas (easy antenna integration in the transceiver) and it is well suited for short range communication, as at 60 GHz 98% of energy is absorbed by O_2 above 1km.

Frequency [GHz]

57	58	59	60	61	62	63	64	65	66
			AUSTRALIA						
CANADA & USA									
		JAPAN							
EU									
WirelessHD™									
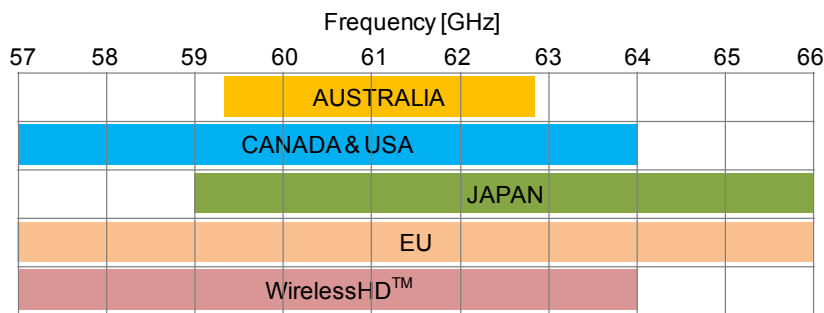
Figure 1: Spectrum Available around 60 GHz

Mass production requirements coupled with the cost constraints of mobile devices result in a need to identify an alternative to existing, expensive Gallium Arsenide (GaAs) and Indium Phosphide (InP) technologies, currently used widely in millimeter-Wave (mm-W) Microwave Monolithic Integrated Circuit (MMIC) fabrication. Radio Frequency (RF) Complementary Metal Oxide Semiconductor (CMOS) 65 nm and 45 nm technologies currently show very attractive performance for mm-W MMIC design, even if the technology environment is a critical issue in the design of frequency synthesizers operating at mm-W frequencies.

Recent developments in mm-W CMOS systems have begun to address the integration of building blocks to form transceivers. In addition to generic challenges such as high-frequency operation and low-noise design, the implementation of transceivers at these frequencies must deal with three critical issues related to the frequency synthesis:

1) generation of the Local Oscillator (LO) signal

2) division of the LO signal for the Phase-Locked Loop (PLL) closed loop

3) distribution of the LO signal

It is therefore important to develop "synthesizer-friendly" transceivers in order to alleviate these issues.

Therefore, transmitting and receiving using 60 GHz in CMOS remains an attractive and unsolved topic in the RF ICs design research field.

The aim of this thesis is to design a frequency divider for a PLL of a direct-conversion transceiver operating at mm-W frequencies in 65 nm RF CMOS technology; in order to achieve this goal, frequency synthesizers architectures and frequency divider topologies will be explored; several previous works in CMOS technologies operating at mm-W frequencies will be visited and analysed. Important issues such as Process, Voltage and Temperature (PVT) variations, Electro-Magnetic (EM) simulations and power consumption will be addressed in this context in order to select and design a frequency divider with high frequency dividing range.

Furthermore, the frequency generation issue will be experimentally faced up, since a wide tuning range, low phase noise 60 GHz Voltage Controlled Oscillator (VCO) will be also designed and integrated in the same die, in order to provide the frequency divider with mm-W input signal without using external RF source.

The implementation of calibration techniques will be also taken into account in the VCO and frequency divider co-design. In fact, in order to address the hard constraint of covering the required bandwidth, not still properly attained at the state-of-art due to the technology impairments at mm-W frequencies (PVT variations), the PLL wherein the two RF blocks will be embedded can implement self-compensation thanks to calibration mechanisms that will be exposed and which is the subject of a registered patent of the author.

1   INTRODUCTION

1.1   Why 60 GHz?

Wireless connectivity trends have tended to track but lag wired solutions in terms of data-rate. Current wireless standards address data rates on the order of tens of megabits per second, with 802.11b at up to 11 Mbps and 802.11a at up to 54 Mbps.

Standards that address mobile users at longer ranges provide much lower data rates as shown in Figure 2. Network interface cards operating at 1Gbps are now standard or available as an option in many new PC's and laptops. It is believed that as consumers grow accustomed to transferring files and other data at 1Gbps, they will also demand the option of doing it wirelessly. Other wired standards, such as Firewire/IEEE_1394 are also following this trend upward in data rates. IEEE_1394 has been deployed for some time at 400Mbps with the next generation in early deployment at 800Mbps, and there exist standards defined for the future at rates of up to 3.2Gbps. What is still missing is a wireless connection with USB transfer capability that can support high data rates, accorded to the demand of consumer electronics, like large data rate multimedia applications.
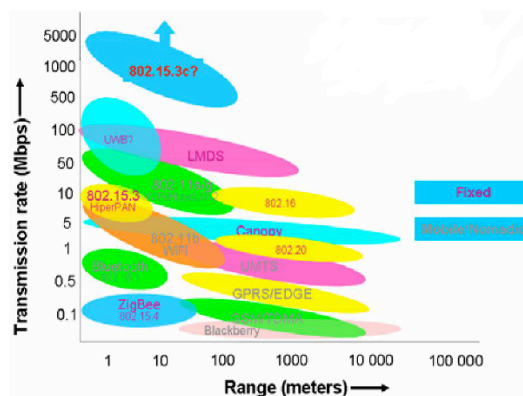
Figure 2: Mobile users Standards

The spectrum between 30 GHz and 300 GHz is referred to as the mm-W band because the wavelengths for these frequencies are about one to ten millimetres. The *Federal Communications Commission (*FCC) has allocated the 57-64 GHz mm-W band for general unlicensed use, which opens a door for very high data rate wireless applications over the 7 GHz unlicensed band. Since oxygen absorption peaks at 60 GHz, this frequency band is particularly interesting for high-dense, high-rate applications in Wireless Personal Area Networks (WPANs).

In an office but also in home environment, the 60 GHz connections can basically replace the wires bundle (USB, IEEE 1394), providing multi-gigabit wireless Ethernet and multimedia delivery. In such scenario, a PC can communicate to all external peripherals (i. e. DVD, printers, digital cameras, external hard disks, *etc.*). Both Wireless Gigabit Ethernet and Wireless ad-hoc networks using 60 GHz are attractive applications for conference room or library management. as well. Furthermore, commercial applications like that so called "Kiosk File Downloading", in which users can download movies, games, *etc*. from a stand placed at public locations such airport, train stations, markets, *etc*., could get a tremendous push to their diffusion in utilization. These applications examples are summarized in Figure 3.

Communications between PC or mobile phone to different peripherals

point-to-point HDTV transmission   **Kiosk file downloading**
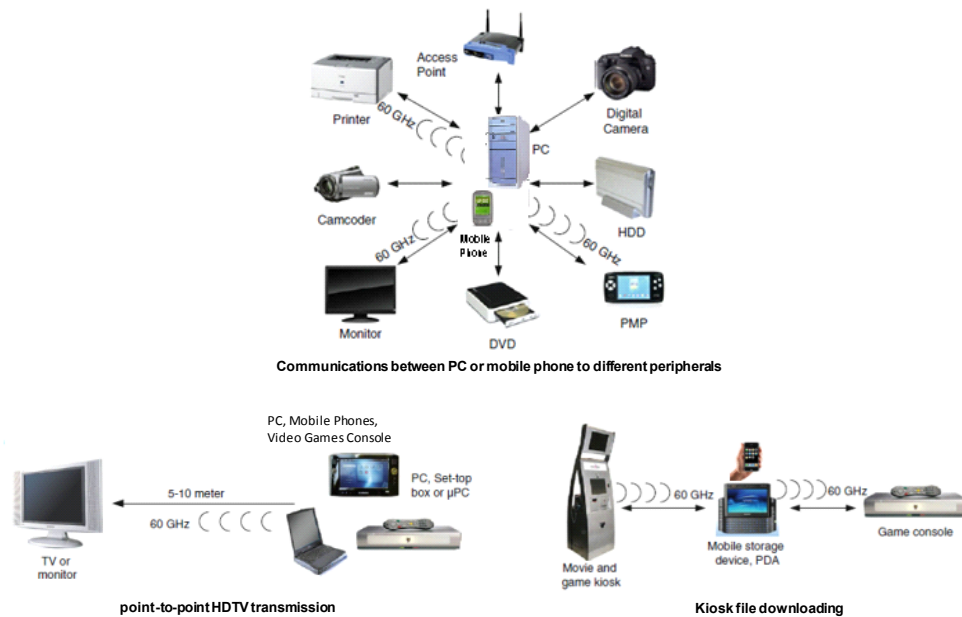
Figure 3: Potential 60 GHz applications

IEEE 802.15.3c has been recently formed to develop a mm-W based alternative physical layer (PHY) for the existing 802.15.3 WPAN standard. The

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mm-W based WPANs have many salient features. First, the mm-W communication is anticipated to achieve very high data rate (over 1 Gbits/sec), so it will enable many killer applications such as high speed Internet access, video on demand, HDTV, home theatre, etc. According to the standard, optional data rates in excess of 3 Gbps is anticipated. Second, mm-W systems can coexist with existing wireless communication systems, such as Wi-Fi (IEEE 802.11), Bluetooth, 2G/3G/4G cellular systems, and Ultra Wide Band (UWB) systems, because of the large frequency difference. Third, because of the larger path-loss, the interference among different mm-W WPANs is very limited, which allows mm-W WPANs to be widely and highly densely deployed. In addition, since the mm-W signal degrades significantly when passing through walls and over the distance, this will help ensure the security of the content. Although mm-W prototype chipsets according to IEEE 802.15.3c specification have been emerging, their performance in a networked environment is an open area beckoning for further investigation. To ensure the success of mm-W based WPANs, how to efficiently and effectively allocate resource for co-existing mm-W devices is a very critical issue.

1.1.1 List of Applications

The data rate in the unlicensed 7 GHz band around 60 GHz should be between 50 Mbits/sec and 60 Gbits/sec, in order to satisfy consumer's requirement and market applications that are going to be detailed.

Briefly, a list of opportunities that this new-service can provide is shown, from the point of view of the consumers:

❖ Automotive applications

➢ Radar items

– Long Range Radar (ACC) (76-77GHz bands)

– Short Range Radar (Stop & Go) (77-81GHz bands)

➢ Ground to vehicle and vehicle to vehicle links (HDR Communications)

❖ High data-rate communications

➢ Last Inch applications (57 to 66GHz bands)

– Wireless HDMI video streaming

– Communications between nomadic devices (such as pocket HD, …)

- Communications between/with mobile devices such as: digital (still) cameras, mobile phones, PDAs)

- HD video transmission on home TV's

- Short Range Ultra fast file transfer

➢ Last Mile applications (71-76GHz, 81-86GHz licensed E-bands)

- Telecom backhauls
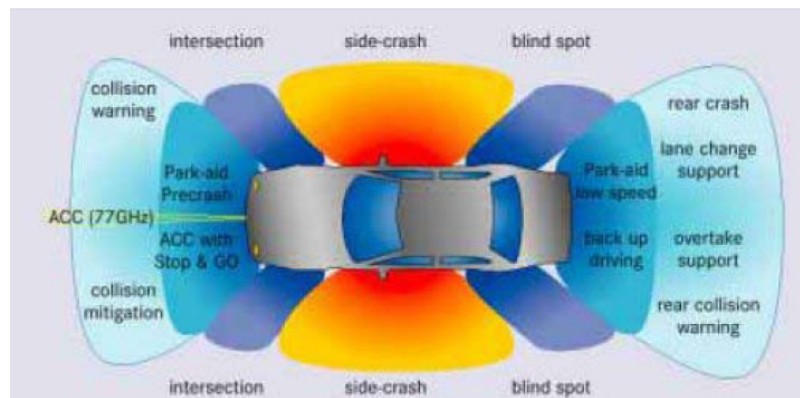
Figure 4: Long and Short Range Radar Applications
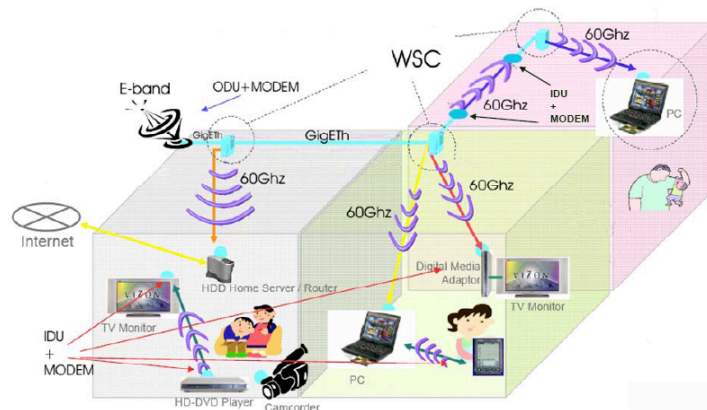
Figure 5: Indoor network scenario and interfacing to the outdoor network

❖ Low data-rate communications (94GHz, >100GHz bands)

➢ Sensor network applications

❖ Optical communications

❖ Chip to chip wireless communications

❖ Imaging

➢ Security non-intrusive investigations

➢ Medical/biological imaging
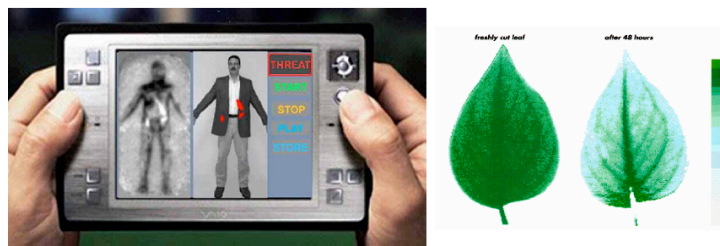
Figure 6: emerging mm-W imaging

1.2   60 GHz RF Front-End: a cost issue

As it is possible to see in Figure 1, there is a more than 3 GHz overlap of unlicensed band around 60 GHz that is worldwide available; the IEEE standard 802.15.3c, alternate PHY for 802.15.3, specifically targets this application space. One of the most significant challenges in utilizing the potential of this frequency band is the cost of the RF front end.

Millimeter wave (mm-W) frequencies have historically been costly to utilize, and have been traditionally used almost exclusively for government, military and non-consumer products [1]. Recent advances in semiconductor technology and low cost high frequency packaging provide an opportunity for this spectrum to become useable for broadband consumer applications within the next 2-3 years [2].

Hardware operating at mm-W frequencies has been expensive to implement. The RF front end of these systems is considered by many to be a significant area of risk because of the high cost of implementation [3]. The RF front end is made up of three key components that drive its implementation which include the semiconductor technology/chipset, packaging along with manufacturing tolerances and yields.

Historically, monolithic microwave integrated circuits (MMICs) have been built using III-V semiconductor technologies, such as GaAs and InP, which

have superior performance compared to CMOS due to their higher electron mobility, higher breakdown voltage, and the availability of passives with high Q. But CMOS implementation ensures higher levels of integration and reduced cost. Several recent developments have combined to enable CMOS circuit blocks to operate at "ever"-increasing frequencies. Millimeter-Wave CMOS circuits directly benefit from the higher speed of the scaled technology. Up to 2009/2010, only CMOS oscillators have been demonstrated beyond 30/40 GHz, while CMOS amplifiers, mixers and frequency dividers are quite lagged regarding frequency operation. A key reason for this large discrepancy is the lack of accurate CMOS active and passive device models at mm-wave frequencies.

Technology advances and trends can be leveraged to cost reductions in these areas. Recent and ongoing advances in packaging and semiconductor technology continue to trend towards higher frequencies, as it is possible to see in the following figures. In addition to allowing for a lower "bill of materials" cost, these advances can also be leveraged to improve final assembly and yield; mm-W CMOS radios present formidable challenges at all levels of abstraction, demanding that designers ascend and descend the device-circuit-architecture-system ladder with ease and confidence; last advances of RF CMOS technology show that there is an alternative to existing, expensive GaAs and InP technologies, currently used widely in mm-W MMIC fabrication; furthermore, the technology scaling for CMOS allows to work in mm-W region, as shown in Figure 7 [4], where it is possible to note the attractive CMOS opportunities versus other technologies:

Unity current gain frequency of different IC Technology, plotted as a function of year forecasted in the 2008 ITRS roadmap

Unity current gain frequency of CMOS plotted as a function of gate length

R&D progress for SiGe HBT and CMOS RF power amplifiers
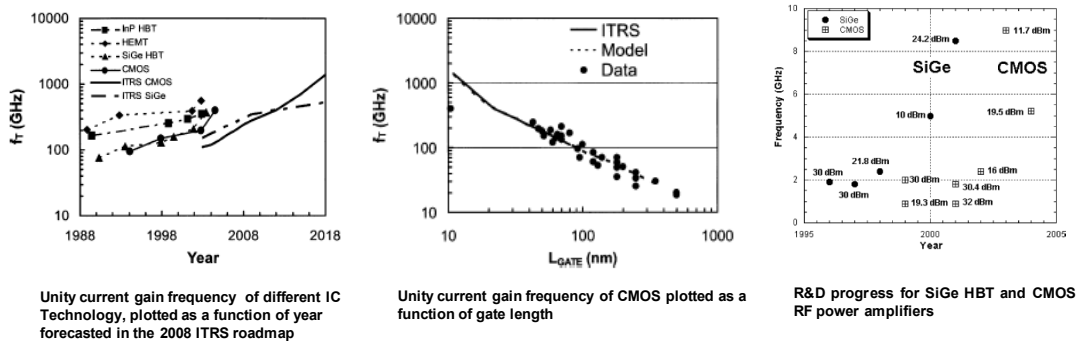
Figure 7: CMOS device and technology evolution for Si-based RF Integrated Circuits according to ITRS forecast

1.2.1   mm-W on CMOS Technology

Currently, it is possible to say that devices and integrated circuits are manufactured on four substrate materials: GaAs, InP, SiC, and Si. While the ,

III-V compounds dominated the millimetre wave spectrum a decade ago, Si-based device technologies have crept into this applications arena, driven primarily by advantages in cost and integration level. In the future, we may see other III-V compound semiconductors, and even C-based semiconductors, including diamond, being developed for this spectrum. RF and Analog Mixed-Signal (AMS) technologies serve the rapidly growing wireless communications market and represent essential and critical technologies for the success of many semiconductor manufacturers. Communications products are becoming key drivers of volume manufacturing; the consumer products demand for mm-W applications is estimated in millions of 60 GHz transceivers that will be produced and sold by 2015 [5]. The consumer portions of wireless communications markets are very sensitive to cost. With different technologies capable of meeting technical requirements, time to market and overall system cost will govern technology selection.

Together with the recently reported 60GHz receiver in 90nm CMOS [6], other receivers in 65nm CMOS demonstrates [7] that scaling of entire mm-wave receivers is possible in both frequency coverage and across technology nodes, as predicted by Gordon Moore in the last paragraph of [8]. Furthermore, with the reduction of the die area occupied by lumped passives at higher frequencies, and with the intrinsic speed improvement anticipated in future CMOS technology nodes, one can expect that entire CMOS transceivers can be scaled to 120 GHz in 45nm, and to 160 GHz in 32nm technologies, as it is possible to note by observing the technology requirements in the 2010 (updated at 2011) International Technology Roadmap for Semiconductors (ITRS) [9] for Analog Mixed-Signal, RF CMOS Technology, as reported in Table 1. Also, mm-W transceivers can be integrated with antennas and other systems to implement wireless I/Os for chip-to-chip communication at 40Gb/s.

Year of Production	2009	2010	2011	2012	2013	2014	2015	2016	2017	2018	2019
Device Technology—RF CMOS [common to High Performance CMOS with 2-year delay]											
V_{dd}: Power Supply Voltage (V)	1,1	1,1	1,1	1,1	1,0	1,0	1,0	1,0	1,0	0,9	0,9
EOT: Equivalent Oxide Thickness (Å)	12	12	10	9,5	8,8	7,5	7,5	7,5	7	6	6
L_g: Physical L_{gate} for High Performance logic (nm)	37	29	27	24	22	20	18	17	15	14	12,8
Peak F_t (GHz)	240	310	330	370	400	440	490	520	590	630	680
Peak F_{max} (GHz)	300	330	360	410	450	500	560	590	680	730	810
NF_{min} (dB) at 24GHz	1,8	1,6	1,6	1,5	1,4	1,4	1,3	1,3	1,2	1,2	1,1
NF_{min} (dB) at 60GHz	3,5	3,3	3,2	3,0	3,0	2,9	2,7	2,7	2,6	2,5	2,4
NF_{min} (dB) at 94GHz	4,7	4,4	4,3	4,1	4,0	3,9	3,8	3,7	3,5	3,5	3,4
peak DC g_m at $V_{DS}=V_{DD}$	1,46	1,75	1,84	2,00	2,12	2,25	2,41	2,49	2,68	2,79	2,93
MSG/MAG (dB) at 24 GHz	14,8	15,9	16,2	16,7	17,0	17,4	17,9	18,1	18,7	19,0	19,3
MSG/MAG (dB) at 60 GHz	10,8	11,9	12,2	12,7	13,0	13,4	13,9	14,1	14,7	15,0	15,3
MSG/MAG (dB) at 94 GHz	8,8	10,0	10,2	10,7	11,1	11,5	11,9	12,2	12,7	13,0	13,4

Table 1: 2010 (updated 2011) ITRS Roadmap for RF CMOS. Near terms requirements

Nevertheless, there are two years lag in meeting the requirements for mm-W applications; one has to note that the yellow squared means that

manufacturable solutions are known, even if their process is still under optimization. In addition and more critical, red squared means that the manufacturable solutions are NOT known. If f_t is the transistor cut-off frequency and f_0 is the operating frequency, usually the latter can be estimated as $f_t/2\sqrt{3}$ and so the WirelessHD^{TM} band is closed to the theoretical maximum operating frequency. Other technological critical points for CMOS technology are the performance degradation due to low gain, linearity constraints and poor noise.

1.3   Critical Issues in CMOS Frequency Synthesizers Design

VCOs and Frequency Dividers (FDs) play critical roles in every synchronous circuit, such as the PLL. Both of them constitute the frequency synthesizer core components and they would need co-design, having a big impact in the overall performance especially because they are the blocks in the PLL that work at the highest frequency. We have seen in the last two decades a great proliferation of VCO and FD topologies in RF ICs on silicon, but reaching high performance VCOs and FDs operating at mm-W is in today's technology a enormous challenge.

When addressing the PLL design at circuit level, the challenges are several: low frequency blocks are not easily scalable to 60 GHz, due to foundry models not well characterized at this frequency; the parasitic elements of active devices also contribute to reduce high frequency operation; the devices are very sensitive to PVT variations at these frequencies. As a consequence, several margins have to be taken into account in the design resulting in high power consumption and big chip area. On the other hand, the fact that the components became affordable in terms of silicon footprint leads to the availability of poor models, in terms of uncertainty, for passive devices like inductors and to the need of EM simulations as well as dummy designs for initial dry-runs to characterize the components, resulting in highest design time. The quality factor (Q) of the varactors, widely used to give tuning capability to VCO and FD, decreases critically at mm-W frequencies, if compared to lower operation frequencies [10], resulting in a Q of the LC tanks that is very dependent on the varactors, while at lower frequencies the Q of the tank is completely dominated by the inductor. Moreover, low-ohmic substrate and low metals conductivity at 60 GHz are an effective further drag in order to approach a reasonably low lossy design.

At layout level, as the 60 GHz wavelength is comparable to circuit dimension, the interconnections between components and blocks inside the chip, as well as supply voltages distribution, are a crucial part in the design. They must be EM simulated in order to take into account layout parasitic and, if it is the case, re-design the circuit in order to compensate or eliminate their

unwanted effects. As the number of metal layers in the selected 65nm RF CMOS design kit is seven (from M1 to M7), it is easy to understand that modelling and simulation steps are time consuming if all the metal layers and vias are included in the simulations. Also, due to the proximity of devices in the chip, EM simulations are needed also to evaluate unwanted coupling effects and losses: this issue must be taken into account in the layout design, with apposite strategies. Just for instance, a capacitance underestimation of 10 fF in a 60 GHz layout interconnections, i. e. with all metal layers and vias employed, can lead to a frequency shift of around 2 GHz!

Regarding measurements at 60 GHz, the critical points are related to the need of accurate calibrations, de-embedding techniques and, in some case, indirect measurements. Losses and mismatch of cables, connectors, adapters, etc., must be taken accurately into account. Additionally, stability and repeatability of the accurate measurements is a further critical points at this frequency.

So it is enough clear that there are several challenges in reaching the transceivers scaling previously mentioned, in terms of operating frequency and technological node, while the market opportunities are very attractive, taking into account consumers demands and trends, as well as CMOS costs.

In this work, all the challenges related to the previously mentioned issues (technological environment, circuits design and simulations, layout with EM simulations and measurements) for a 60 GHz FD and VCO co-design in 65 nm CMOS will be practically faced up and discussed.

1.4   Objectives and Methodology

The first main objective of this Thesis is to design a divide-by-two FD working in the 60 GHz band and showing a frequency dividing range of at least 7 GHz in order to cover the WirelessHD^{TM} band. Indeed, this dividing range should be higher than 7 GHz, to take into account the frequency shifts and offsets due to PVT variations, which constitutes the second main objective of the Thesis.

Furthermore, a low phase-noise, wide tuning range VCO for the WirelessHD^{TM} band is also co-designed and implemented in the same die with the FD, in order to provide it with input frequency. The critical challenges related to PVT variations at 60 GHz and frequency distribution of the LO signal are faced up in the VCO-FD co design, being the third objective of this Thesis, to demonstrate that the FD is able to work along with the integrated VCO. The VCO and the FD are designed in order that each one can be measured separately, in "stand alone" (VCO ON - FD OFF or VCO OFF - FD ON) or both

operating simultaneously (VCO ON - FD ON) as would be the case in a 60 GHz PLL for direct-conversion transceivers operating in such band.

It has been already observed how the implementation of communication applications in the 60 GHz band for large market and hand-held devices require the utilization of low-cost state-of-the art CMOS technologies. Some transceivers built using such process (CMOS 90nm, 65nm) have been already demonstrated, as in [11] and [12]. There exist, however, some important issues to be solved. Most of the them use heterodyne principle with double conversion stages or sliding-IF architecture since the realization of a frequency synthesizer block covering the whole band (7 GHz) plus additional margin for PVT compensation has not been completely solved. Another reason to operate at lower frequency is due to the need of very low phase noise, and it is another still open research issue for 60 GHz CMOS direct-conversion transceiver design, not considered as objective of this thesis. This topic could be considered as future work when the first problem is solved, i. e. the operation frequency issue at 60 GHz.

Some oscillators have been proposed, like [13], that could be used to fulfil those requirements, but the implementation of the FD block that necessarily follows in the PLL of the frequency synthesizer was still an open research topic at the beginning of this Thesis.

The work reported in this Thesis describes the study, analysis and implementation of a 60 GHz FD and VCO co-design in 65 nm CMOS technology, to push on the research in 60 GHz PLLs for direct conversion transceivers for mm-W application. This has been the main motivation of this Thesis work.

As a summary of the aforementioned situation, the main challenge boarded in this Thesis is that the FD must work at 60 GHz and it has to cover the overall VCO tuning range, that is 7 GHz plus an additional margin for taking into account the effects of PVT variations and devices models. The goal is to maximize the tuning range of the ensemble VCO + FD with the minimum power consumption. The centre frequency of the tuning curves should be that required for a direct-conversion or very low-IF transceiver architecture.

These main objectives have been divided into the following sub-objectives, that can be mapped to specific tasks:

1) *Selecting the FD topology most suitable to operate at 60 GHz.*

2) *Designing the "core" of the 60 GHz FD and VCO.*

3) *Designing VCO and FD output buffers, taking into account that both VCO and divider should be measured "stand alone" (where*

one of them is OFF when the other is ON) and also both ON, like in a PLL.

4) *Investigating the PVT variations impact in the FD and VCO, especially the relation between VCO tuning range and FD dividing range.*

5) *Inventing a suitable strategy in order to calibrate and compensate the divider for covering properly the whole VCO tuning range, taking into account the result achieved in 4).*

It is possible to say that the required design techniques and tools are determined for the type of circuits and operating conditions. Along the development of this Thesis, the principal activity has been researching circuit alternatives and design techniques based on simulations, using a pre-characterized set of models and elements corresponding to a particular technology (a design kit provided by the silicon vendor). However, this is not enough since some of the models available are not appropriate for the operating frequency range. Therefore, specific modelling activities have also required in the framework of this thesis. The impact of PVT variations in the design have been analysed by simulation, as well.

The circuits designed have been validated by measuring prototypes that have been fabricated by the foundry that provides the selected technology. Experimental results are used to validate the methodology, the basic operation of the circuits and the techniques found during the research process, as well as the simulation environment. A complete experimental validation of the PVT impact and the effectiveness of the technique is, however, not possible, since this would require the access to many different samples of the prototypes for many different fabrication process conditions. This type of access is usually only available to the foundry itself and not to external users or academic institutions.

The FD and VCO co-design has been carried out through simulations, then prototyping and finally measurements. The work presented in this Thesis report is related to circuit level design, so that no simulations at system level are considered.

In order to model passive devices and layout interconnections for RF distribution at mm-W band, electromagnetic modelling tools, such as Momentum from Agilent technologies, has been used. This is needed to exactly quantify unwanted parasitic layout effects, as well as, regarding the inductors, alternative models to those provided by the design kit. The circuit models for inductors available in the design kit have been qualified only up 40 GHz. Therefore electromagnetic simulations are essential in mm-W circuits design on silicon

and its accuracy level is a prerequisite for the design methodology validation by experimental results.

The frequency domain simulation environment at circuit level for the FD and VCO behaviour has been based in GoldenGate and ADS simulators, run in the Virtuoso design environment of Cadence, while SpectreRF has been used for simulations in the time domain. This is because SpectreRF is not so robust in frequency domain when applied to distributed models at mm-W frequencies, while it is very solid to perform transient analysis to evaluate intermediate states of the FD. Therefore, a combination of both frequency domain and time domain techniques has been required.

For simulations of oscillation circuits, autonomous analysis based in Harmonic Balanced (HB) or in Periodically Steady-State (PSS) analysis has been performed. When managing injected systems, since they are not autonomous but driven, a robust way to simulate them is transient analysis, because they are strongly non-lineal systems and the small-signals analysis does not make any sense.

The physical design and prototyping has consisted in FULL-CUSTOM layout, starting from library elements (PCELLs) of the basic component, and from regular complex interconnections and other elements that have been built for "ad-hoc" purposes. The information of the selected technology, as well as simulation models for various platforms and verification files for correct layout and manufacturing, is provided to external users by the foundry in the form of the Physical Design Kit (PDK). The fabrication of the prototype has been done through Circuit Multi-Project (CMP) with the selected CMOS technology, since this allows academic institutions to fabricate at lower prices using state-of-the-art processes.

The fabricated samples have been measured with the collaboration of the Cea-Leti Laboratory at MINATEC in Grenoble (France), which is one of the few available labs equipped for 60 GHz measurements on wafer.

The objectives of this thesis work are compatible with existing collaboration with STMicroelectronics, one of the most important foundries offering state-of-the-art CMOS technologies, as well within the framework of a European project in which the research group participates (ENIAC MODERN project). Additionally, the investigation of PVT effects in RF integrated circuits and the design of compensation techniques is one of the main objectives of a national project funded by the Spanish Science and Innovation Ministry (TEC2008-01856) in which the research group, in where this thesis work has been developed, is currently working. Both projects have provided financial support for the realization of this thesis.

1.5   Thesis Report Organization

In Chapter 2, starting from an overview of the architectures for CMOS transceivers, the state-of-art concerning the frequency synthesizer block of wireless transceivers is deeply analysed, with a special focus on the alternatives proposed for mm-W applications. A 40 GHz PLL for sliding-IF transceiver for 60 GHz application will be presented as a paradigmatic example of such type of circuits.

Chapter 3 reports a state-of-art review about FDs implemented in CMOS technologies used for mm-W applications. Several FD topologies are presented and a comparison among them in terms of performance and efficiency is given. Two FD topologies are deeply analysed and selected as the more suitable circuit alternatives for 60 GHz CMOS FDs. The PVT variations impact in fabricated CMOS FDs and VCOs is analysed as well in this chapter. Finally, some calibration techniques for PLLs operating at mm-W frequencies proposed in the literature are reviewed.

Chapter 4 is devoted to the design of the 60 GHz VCO at circuit level using a 65 nm CMOS process. All the different parts composing the VCO core are accurately sized in order to achieve a good compromise among tuning range, phase noise and power consumption. A design methodology for VCO operating at mm-W is also proposed, focused on maximizing the VCO tuning range to account for PVT variations compensation and a final optimization process is carried on to optimize the VCO phase noise.

In Chapter 5, the design of a 60 GHz FD in 65 nm CMOS technology is presented. The FD topology selected is the Injection Locked FD, shown to be the best candidate among the FD topologies analysed for operation at mm-W frequencies for direct-conversion transceivers. The phenomenon of frequency locking in LC oscillators is deeply analysed and simulated in both time and frequency domains. Several injection architectures are simulated and compared in order to select the most efficient injection scheme. Finally, a novel FD circuit operating at 60 GHz is designed at circuit level and a design methodology to achieve wide dividing range, low power consumption, and high speed operation is presented.

Chapter 6 describes the physical design (layout) phase to carry out the 60 GHz FD and VCO design using a 65 nm CMOS process. The ILFD and VCO output buffers design and implementation is described. In this chapter the EM simulations and modelling approach of the inductors, layout interconnections and transmission lines are presented. In this way the S-parameters models for such structures are extracted from the layout to be included in the post layout simulations and final optimization. Finally, the simulation results of the whole

system composed by the 60 GHz VCO and divide-by-two FD, providing the 30 GHz output, are presented.

Chapter 7 addresses the issue of PVT variations and its impact in the circuits operation. The results of the PVT variations simulation are presented, where usual process corners along with the variations of voltage supplies and temperature are considered. One of the objectives of this Thesis is investigating the PVT variations impact in the whole system composed of the VCO followed by the FD. Therefore, based on the PVT simulation results, a calibration methodology to compensate the PVT impact in the frequency synthesizer built upon those two blocks is presented, in order to ensure a robust ILFD tracking of the VCO in all processes and environmental conditions. Such calibration technique is the subject of a registered patent of the author.

The experimental results are reported in Chapter 8, where also some post measurement simulation results are presented, in order to investigate the causes of the differences between measurements and simulations.

In Chapter 9 the most relevant conclusions of the Thesis work are given and the main activities and contributions of this Thesis are summarized. A roadmap is also provided, considering the future works that can stem from the presented work.

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2 ARCHITECTURES FOR CMOS TRANSCEIVERS IN mm-W BAND

In this section, several architectures of transceivers operating in mm-W frequencies are going to be explored, with a special focus on the block regarding the frequency synthesis.

There are three big issues regarding the frequency synthesis: generation, division and distribution of the LO signal; these three issues form three challenges, especially when operating at mm-W frequencies in CMOS technology.

While starting from providing a list of the transceivers architectures, with just a brief explanation of each block, then the advantages and problems of the different conversion topologies will be show and analyze. Sub-section 3.1 includes the heterodyne transceiver architectures, where single and double conversions will be analysed. Sub-section 3.2 concerns the homodyne transceiver architectures and then a brief summary regarding considerations about down-conversion scheme for transceivers in mm-W band is provided.

In sub-section 3.4 the issues related to frequency synthesis block issues are addressed and several frequency synthesizers architectures are exposed.

Figure 8 shows, in a basic and brief way, a generic block diagram of a wireless receiver:
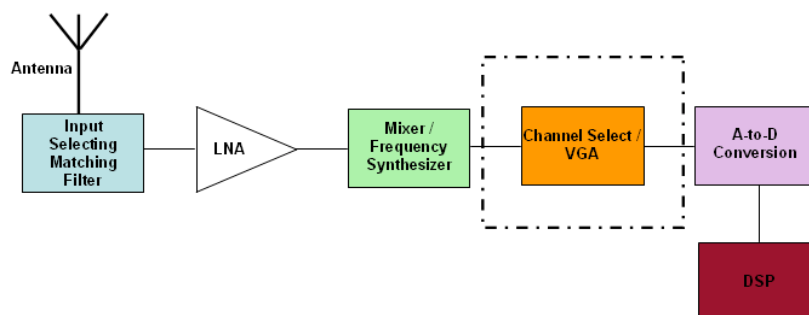
Figure 8: Generic receiver block diagram

The broadband antenna signal is fed into a highly selective band-pass filter (the pre-selector filter) which suppresses all interferers residing outside of the band and matches the antenna to the receiver, in order to limit insertion-loss that is disastrous in terms of noise performance. By removing this out-of-band blocking signals, the dynamic range requirements of the receiver can be relaxed considerably. A Low Noise Amplifier (LNA) boosts the weakest channels above the noise floor of the first mixing stage.

The first key block of a receiver is the LNA: the task of the LNA is to provide the following stages with power gain, without increasing the overall noise figure of the receiver, or "injecting" as lower noise as possible; the design of the LNA addresses the challenge of meeting together: input and output power matching, low noise figure, high power gain, good linearity performance in terms of high 3rd Order intermodulation resistance with low power consumption.

The RF mixer can be realized as either a passive structure followed by an amplifier or an active topology: at 60 GHz, usually, the passive mixer presents low impedance to the LNA, lowering the gain of the LNA/mixer cascade. A candidate for active mixers operating at mm-W frequencies is an active topology using auxiliary current path; furthermore, in order to avoid a large mismatch, thus creating large variations in the current flowing from the switching pair, an active topology with capacitive coupling can be used [1], as shown in Figure 9:
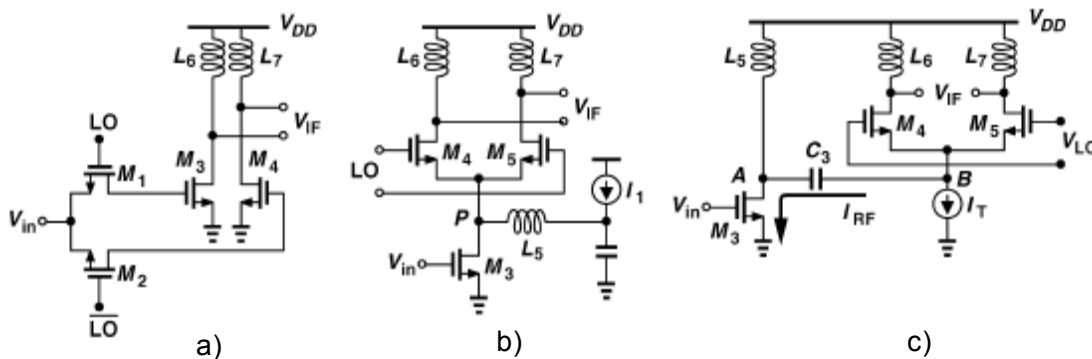
Figure 9: Mixer topologies: a) passive, b) active with auxiliary current path, c) active with capacitive coupling

About the frequency synthesizer block, that is the PLL circuit, the sub-sections 2.4 and 2.5 are dedicated to the issues regarding its design at mm-W frequencies; furthermore, the rest of the pages are dedicated to the two key blocks inside a PLL that are the FD and the VCO. By now, one has just to consider that for the frequency synthesiser, the large bandwidth feature requires

wider tuning range VCOs and high speed FDs to cover reliably the whole 7 GHz of bandwidth available around 60 GHz; additionally, achieving a wide locking range is also a critical issue in a FD if the low power consumption becomes a severe requirement.

2.1 Heterodyne Transceiver Architecture

Single Conversion Heterodyne

In Figure 10, a simple **heterodyne** down-conversion system block diagram is shown:

$$A_0 \cos\omega_0 t$$
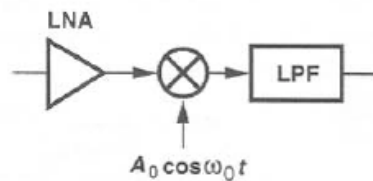
Figure 10: Generic heterodyne down-conversion block diagram

In the heterodyne architecture, the signal band is translated to "much lower" frequencies; this relaxes the Quality Factor (Q) required for the channel-select filter (see Figure 6). The frequency translation is carried by means of a mixer which could be viewed also as a simple analog multiplier.

If f_0 is the frequency synthesizer output signal (LO), f_1 is the RF signal coming from the LNA and f_2 is the so called Intermediate Frequency (IF),such that $f_0 = |f_1 - f_2|$; f_2 is the centre frequency of the down-converted band and it is a critical parameter.

The problems that affect heterodyne architecture are the "image-frequency", that must be rejected, and the channel selection; these issues establish a trade-off. Furthermore, the effect of the half IF in a heterodyne receiver must be considered as well [2].

The trade off between sensitivity and selectivity in the basic heterodyne architecture often proves quite difficult to optimize with a single conversion stage. To resolve this issue, the concept of heterodyne can be extended to multiple down/up-conversions.

In digital modulation receivers, the second down-conversion typically comprises both in-phase (I) and quadrature (Q) components of the signal while translating the spectrum to zero or very low frequency. This technique allows

skipping a second intermediate frequency stage, since the I/Q low frequency channels can be directly demodulated in the digital domain after A/D conversion.

2.1.1 Double Conversion Heterodyne

In Figure 11, the heterodyne receiver architecture with double frequency conversion is shown. Two LO signals at different frequencies are required, obtained, in this case, by frequency multiplication and division from a single VCO.
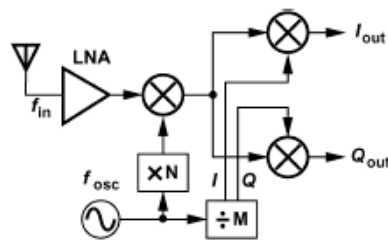
Figure 11: Double Conversion Heterodyne receiver

This architecture [1] must deal with the losses of the frequency multiplier and the problem of image rejection of the heterodyne receivers. Depending on the choice of f_0, N and M, for a mm-W signal f_{in} = 64 GHz, the image lies at 45.7 GHz, experiencing only some attenuation if the front end must accommodate frequencies as low as 57 GHz [3].

As another example, the receiver in [4] uses f_0 = 29 GHz and N = 2, thereby suffering from an in-band image. Consequently, the image thermal noise produced by the antenna, the LNA, and the mixer is down-converted to the IF, raising the receiver noise figure by about 3 dB. For the receiver in [5] the image is suppressed by the selectivity of the antenna and the RF front end. Nevertheless, f_0 is still relatively high.

The heterodyne architecture of Figure 11 greatly simplifies the three LO-related tasks: 1) generation occurs at 40 GHz with no need for quadrature phases; 2) frequency division also occurs at 40 GHz, permitting a broadband design; and 3) distribution of the differential 40 GHz LO is much simpler than that of quadrature 60 GHz components. Note that no LO buffer is necessary as interferers in the vicinity of 40 GHz are suppressed by the selectivity of the front-end (including the antenna). The divide-by-two circuit in this circuit is driven by a 40 GHz LO; it provides LO signals for the two IF mixers as well; as such, the divider must satisfy difficult requirements that are the object of this thesis and

that are going to be discussed in the following pages. Furthermore, the following issues must not be underestimated, regarding FD constraints: 1) drive a total capacitance corresponding to the two inputs IF mixers while presenting a small capacitance to the LO; 2) provide relatively large output swings to optimize the switching in the IF mixers; 3) employ no input or output buffers as such buffers would require additional inductors; and 4) use no more than one inductor to allow a reasonable floor plan. The last condition rules out the possibility of quadrature outputs.

A natural choice of the LO frequency in a heterodyne system is half of the input frequency as it places the image in the vicinity of zero while greatly simplifying the design and distribution of the LO and divider signals [5]. But, a simple heterodyne chain consisting of a single RF mixer and quadrature IF mixers suffers from an additional image introduced by the third harmonic of the LO in the RF mixing operation, which flips the signal spectrum horizontally and superimposes it on the original down-converted spectrum. The corruption of the down-conversion, due to the LO third harmonic amplitude, proves serious problem in modulation scheme having asymmetric spectra (FM, QPSK and QAM).

Figure 12 (left) shows a transceiver architecture [6] that relaxes the LO-related issues (the VCO output is centred at 30 GHz) while avoiding frequency multiplication. Placing the image around zero, this scheme incorporates the lowest possible LO frequency (relaxing the FD working frequency) and has provided a compact design in terms of floor plan.
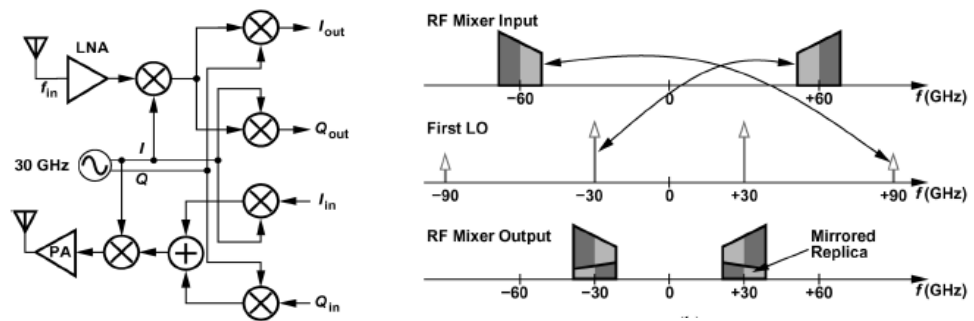
Figure 12: Half-RF heterodyne transceiver architecture: receiver's scheme (left); signals spectra (right)

This "half-RF" architecture however, exhibits a number of drawbacks: the first is related to the LO third harmonic and the mirrored replica generated, as it is illustrated in Figure 12 (right). The second drawback of such half-RF receiver stems from the inevitable result that the first IF is equal to f_{LO}. Thus, the LO-IF feed-through of the RF mixer cannot be filtered, potentially desensitizing

the IF mixers. This issue makes it difficult to utilize a single-balanced RF mixer, which is the preferred choice if the LNA is single-ended.

In order to avoid the signal replica, the work [7] describes a heterodyne receiver architecture that incorporates a 30GHz LO without quadrature phases and resolves the issue of the third harmonic of the LO as well. The architecture thus lends itself to better integration and signal distribution while consuming lower power. As shown in Figure 13 (left), the receiver performs quadrature separation in the RF path and down-converts the signal to 30GHz and then to baseband. Figure 13 (right) illustrates the operation showing the spectra at various points along the receiver chain. By virtue of quadrature separation, the positive frequency content of the signal is removed.
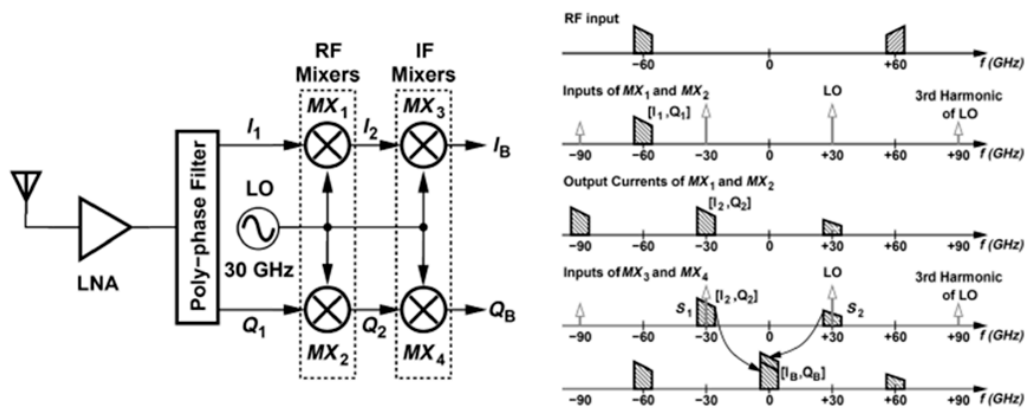
Figure 13: Heterodyne receiver with 30 GHz LO: receiver's scheme (left); signal spectra along the receiver chain (right)

The advantage of this architecture is to suppress spur component. The image rejection ratio (IRR) of the poly-phase filter contributes to the spur suppression as well. For example, with a 0.5dB gain mismatch and a 5° phase mismatch, the unwanted replica remains 35dB below the desired signal. A 2-stage poly-phase filter is required in order to obtain a reasonable image rejection compared to other architectures, [1], [3], [4]-[5] and [8], as well as to accommodate a wide bandwidth. The filter architecture also converts the single-ended output of the LNA to differential form.

2.2   Homodyne Transceiver Architecture

In the direct-conversion or zero-IF architecture, the RF spectrum is simply translated to the baseband in the first down-conversion; this conversion topology entails vastly different issues compared to heterodyne topologies.

Important constraints related to direct-conversion architecture, due to the translation at zero-frequency that does not apply in heterodyne receiver, are the channel selection (1), before the analog-to-digital conversion (Figure 8) and due to the noise-linearity-power trade-offs, the DC-Offset (2), because since the down-converted band extends to zero-frequency, extraneous offset voltages can corrupt the signal and saturate the following stages; 2nd and 3rd Order Distortion (3) that implies the need of high-linear LNA to attenuate RF mixer behaviour, Flicker Noise (4), that may be lowered by using active mixers, and LO Leakage (5).

In the simple zero-IF architecture, the LO frequency is equal to the input RF frequency. But a simple direct conversion receiver operates properly only with double-sideband AM signals, because it overlaps positive and negative parts of the input spectrum. For frequency and phase modulated signals, the down-conversion must provide quadrature output, like the architecture shown in Figure 14 [1], so as to avoid loss of information: this is because the two sides of FM or QPSK or the modulation used in mm-W receivers spectra carry different information and must be separated into quadrature phases in its translation directly to baseband.
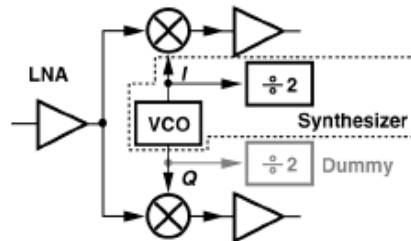
Figure 14: Direct conversion architecture

This issue is related to the I/Q mismatch and requires shifting either the RF signal or the LO output by 90°; but this entails severe noise-power-gain trade-offs; the errors in the nominally 90° phase shift and mismatches between the amplitude of the I and Q signals corrupt the down-converted signal constellation, thereby raising the bit error rate.

It is possible to say that the generation of I and Q phases of the LO at 60 GHz entails, basically, two issues: (a) quadrature operation typically degrades the phase noise considerably (because two core oscillators consume power, they must operate away from resonance frequency of the tanks, and they do not improve each other's phase noise) and (b) the comparatively low tank (Q) results in serious design trade-off (phase-noise and wide tuning range).

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In order to realize such architecture at least two inductors in the LNA, one in each mixer, two in the quadrature voltage-controlled oscillator (VCO), and at least one in the FD are required. The dummy divider serves to keep balanced the I and Q outputs.

LO frequency division also proves problematic in this architecture. Injection-Locked FD (ILFD) and Miller dividers typically suffer from a narrow lock range if designed for 60 GHz applications, as it will be exposed in the following chapter. The task, namely, LO frequency division, also proves problematic in this architecture.

In order to ameliorate the issue of the frequency division, a direct conversion topology with frequency doubler has been also proposed in [6], as shown in Figure 15:
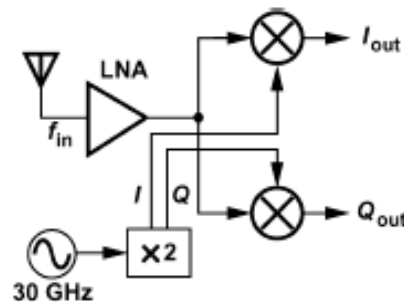
Figure 15: Zero-IF architecture with frequency doubler

While simplifying the task of division in the frequency synthesizer, this approach suffers from other drawbacks: 1) CMOS doublers tend to be quite lossy at these frequencies, raising the LO noise floor, necessitating post-amplification to achieve sufficient swings, and consuming additional inductors; 2) typical doubler topologies do not produce quadrature outputs, requiring additional (lossy) quadrature separation stages; and 3) the distribution of the 60 GHz quadrature phases around large layout structures such as inductors still proves difficult.

2.3 Summary of Transceivers Architectures

It is important to note that a direct conversion is certainly the most convenient and simple conversion topology but at mm-W frequency it implies, along other challenges, that the frequency synthesizers needs FDs that must operate at frequencies where the speed, sensitivity and selectivity, in terms of

wide locking-range, are severe requirements, and where the PVT variations have a tremendous impact.

Heterodyne receiver architecture will be chosen, instead of direct-conversion one, if no other solution could be more feasible and commercially interesting at 60 GHz; but the aim of this thesis is pushing on this issue and contributing to implement frequency synthesizer for direct-conversion transceiver operating in mm-W band.

The first challenge consists in designing a frequency synthesizer that works in mm-W band, as shown in Figure 16, taking into account power consumption and tuning-range of the VCO; these issues carry on the need of 60 GHz FD, considering the tremendous impact of PVT variations and speed requirements.
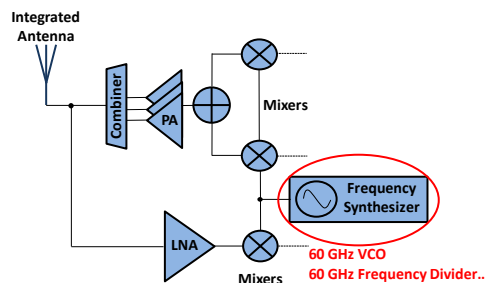
Figure 16: 60 GHz Direct-Conversion Transceiver for mm-W band

The second challenge for direct-conversion transceivers design at 60 GHz, that is the accurate I/Q LO signals generation as already mentioned, is out of the scope of this thesis.

2.4   Frequency Synthesizers Architecture

The oscillators used in RF transceivers are usually embedded in a frequency synthesizer circuit so as to achieve a precise definition of the output frequency. Synthesizer design still remains one of the challenging tasks in RF systems because it must meet very stringent requirements. Furthermore, at mm-W frequencies these requirements become more severe, due to the impact of PVT variations.

Frequency synthesizers are essential part of wireless transceivers and often consume a large percentage (20–30%) of the total power [9]. A typical PLL-based frequency synthesizer comprises both high and low frequency blocks. The high frequency blocks, mainly the VCO and first stage of the FDs, are the main power consuming blocks, especially in a CMOS implementation.

Up to now, other technologies have often been chosen over CMOS to design the high frequency block in the 60 GHz band, while the low frequency blocks are commonly implemented by using CMOS technologies.

The typical frequency synthesizers issues are frequency accuracy and stability, channel spacing, phase noise, sidebands (that is, spurs) and lock time. Figure 17 shows a basic frequency synthesizer architecture operating at mm-W frequency; it is very similar, as architecture, to lower frequency synthesizers, except for the FD.
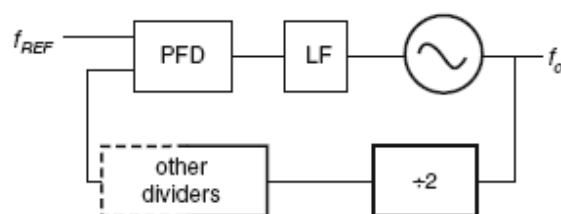
Figure 17: mm-W band PLL architecture

Regarding the FD, next chapter is completely dedicated to the state-of-art issues related to the design of that block.

The VCO is the frequency synthesizer block in charge of the frequency generation. The VCO output frequency is $f_{out} = f_0 + K_{VCO} \cdot V_C$, where f_0 is the self-oscillating frequency of the VCO, that is the free-running frequency, K_{VCO} is the VCO gain and V_C is the control voltage. The fundamental critical points in designing VCOs are to achieve a wide tuning range and a low as possible phase noise. At mm-W frequencies, reaching these requirements is a big challenge, since a suitable balance between them should be achieved, considering their high operating frequencies and the PVTs impact. It is possible to find in literature many papers regarding VCO design in CMOS technologies for 60 GHz applications, as demonstrated in [10] and [11]-[12]. Chapter 4 is completely dedicated to the design of a 60 GHz wide tuning range VCO in 65 nm CMOS.

2.4.1   Type-I PLL

If we consider the system of Figure 17 without the dividers, the PLL is a feedback system operating on the excess of phase of nominally periodic signals. The Phase Frequency Detector (PFD) or Phase Detector (PD) works as an "error detector" in the feedback loop in the phase domain (Figure 18). The

loop is considered locked if the phase differences are constant with time: in fact, it means that the input and output frequencies are equal.
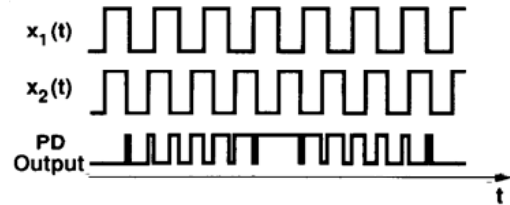
Figure 18: Input and Output PD waveforms

Ideally, the DC value of the output signal is linearly proportional to the difference between the phases of the two input frequencies; but PD characteristic of a real implementation may not be linear as the phase difference increases. Furthermore the amplitude and the duty-cycle of the inputs have an impact on the gain of the phase detector [2].

The Low-Pass Filter (LPF) suppresses high frequency components of the PD output, allowing the DC component of the PD output signal to control the VCO frequency.

Type-I PLLs have shortcomings that often prohibit utilization in high performance integrated circuits; they suffer critical drawbacks: limited acquisition range and locking range (1) and potential instability (2) due to realistic RC implementation of the loop filter. The PD and loop filter plays important role in the system dynamics; for this reasons Type-II PLLs are often required. The fundamental difference between two topologies is that the open loop transfer function of the Type-I has only one pole at the origin whereas that of Type-II has two poles at the origin, resulting in better stability. Regarding PLL theory and design several papers and books exist, where the reader can find further details [13]-[14].

2.4.2 Type-II PLL

By increasing the loop gain it is possible to make the PLL "more" stable. Considering the basic PLL architecture, in the LPF the average value of the PD output is obtained by depositing charge onto a capacitor during each phase comparison event, and so allowing the charge to decay afterwards. Charge-Pump PLLs can be used in PLLs incorporating a Phase-Frequency Detector (PFD), that is a Phase/Frequency detector and a Charge-Pump are used instead of the "standard" combination of PD and LPF. Combining the PFD and

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the Charge–Pump offers two important advantages: (1) the capture range is only limited by VCO output frequency range, and (2) the static phase error is zero if mismatches and offsets are negligible [2]. Type-II PLLs are usually of 3rd order, because an additional capacitor placed in parallel with series RC network contributes to a 3rd pole.

2.4.3 N-Integer PLL

Frequency synthesizer often requires that the output frequency of the PLL be a multiple of the input frequency; so a PLL can "amplify" a frequency in the same way a feedback circuit amplifies a voltage. In such a circuit, the channel spacing is equal to the input reference; the loop gain is divided by M and the input phase noise is multiplied by M, where M is the division ratio between the VCO output frequency and the reference frequency.
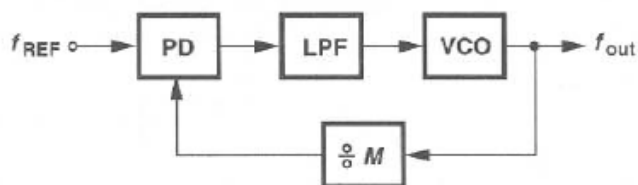
Figure 19: N-Integer PLL architecture

To implement the architecture of Figure 19 for multiple channel systems, a variable or programmable M is required, in order to get f_{out} = M·f_{REF}. That architecture has two fundamentals drawbacks: reference spurs generation (1), because the VCO output f_{out} is modulated by f_{REF}, since even when locked the PFD generates pulses at f_{REF}; limited loop bandwidth (2), since channel spacing is equal to input reference: Type-II PLL stability is limited. In order to reduce reference spurs, several solutions have been used [15]; the PLL can be made as 3rd Order (shunt capacitance) and a notch filter can be inserted before VCO input to suppress unwanted spurs or Fractional-N architecture can be used.

2.4.4 Fractional-N PLL

In Fractional-N architecture, the output frequency can vary as a fraction of the input reference and it allows the channel spacing to be much smaller than the input reference frequency.

The loop bandwidth can be larger than 1/10 of the channel spacing and the reference spurs are out of band. Figure 20 shows fractional-N PLL architecture:
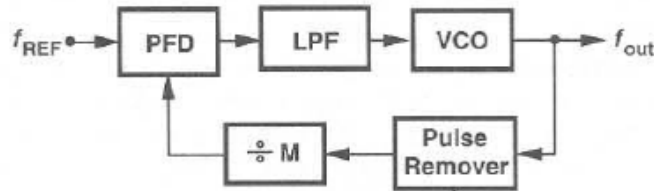
Figure 20: Fractional-N PLL with prescaler

The M block is a modulus selection (divider) with a prescaler and counters. The Pulse Remover (PR) output is a waveform equal to the input, except for a pulse that is removed every T_p period; considering the architecture of Figure 19, $f_{out} = M \cdot (f_{REF} + 1/T_p)$; T_p is the period with which the remove command is applied.

Fractional-N PLL architecture suffers from the critical drawback of the fractional spurs generated; that is, the real VCO frequency provided by the frequency synthesizer is $f_{out} = (N + \alpha) \cdot f_{REF}$; this is due to the ramp waveform with period $1/(\alpha \cdot f_{REF})$ that modulates VCO output frequency. In the frequency domain it means the presence of spurs at $f_{out} \pm \alpha \, f_{REF}$, $f_{out} \pm 2 \, \alpha \, f_{REF}$. Several techniques can be implemented in order to overcome to the fractional spurs issue, such a compensation and randomization techniques.

Modern implementations of N-Fractional PLL replace the PR, and eventually the other divider block, with a dual modulus prescaler, as the architecture presented in [15], reported in Figure 21, for application in mm-W band: the VCO frequency is around 40 GHz.
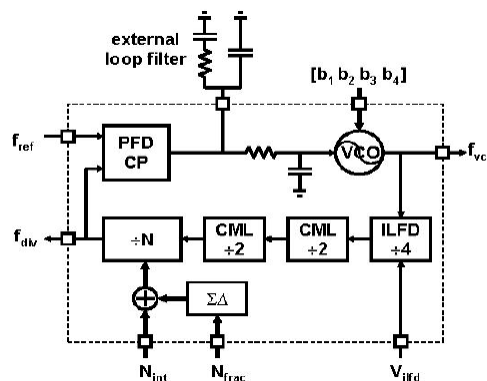
Figure 21: N-fractional PLL with dual modulus prescaler

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2.5   PLL at mm-W Frequencies

As previously mentioned, Figure 21 shows one of the proposed architecture of frequency synthesizer for 60 GHz applications; the tuning range of the VCO frequency in this case is 39.1 GHz to 41.6 GHz.

When operating at mm-W, the most critical block in a PLL is the first FD, which is usually a divide-by-two divider, even if in Figure 21 it is a divide-by-four FD. The big challenge in designing FDs for mm-W application is to ensure a wide dividing range that covers properly the VCO tuning range, with the lowest as possible power consumption.

The PLL in Figure 21 has been designed to operate at 50GHz for sliding-IF receiver architecture. In such architecture, the IF is generated by dividing the RF LO frequency by an integer: so, the IF changes as a function of the selected channel. The IF range is from 6 GHz to 7 GHz. The final I/Q-down-conversion LO is generated by division-by-8 (divide-by-4 and divide-by-2) of the 50 GHz PLL signal. This architecture has the advantages of heterodyne receivers and does not require an I/Q LO for the first down-conversion.

The VCO has 4 digitally controlled NMOS varactors equally sized to produce 5 frequency bands. The analog varactor is twice as large to ensure proper overlap between the different bands. Coplanar waveguide (CPW) stubs implement the inductors. The VCO runs from 1 V to reduce the stress on the active devices and improve reliability.

The first divider stage in the PLL feedback loop is a divide-by-4 ILFD, based on a two-stages ring oscillator; two PMOS devices have been used as resistors controlled by an external voltage in order to change the ILFD self-resonance frequency (these issues will be more clear starting from next chapter).

A digital calibration technique is also implemented to overcome the FD locking-range limitations due to higher-order harmonic locking. That is, the locking range of the FD is limited to approximately 1GHz, and it is not enough to cover the tuning range of the VCO, especially if PVT variations are taken into account. The PLL is fabricated in 90nm CMOS and locks from 39.1 to 41.6 GHz. It uses an 18 bits $\Delta\Sigma$ modulator to achieve 3 kHz resolution with 50MHz reference.

In Figure 22 are shown, respectively, the output spectrum of the described frequency synthesizer, left side, and its phase noise at the VCO output and at divider output, right side.
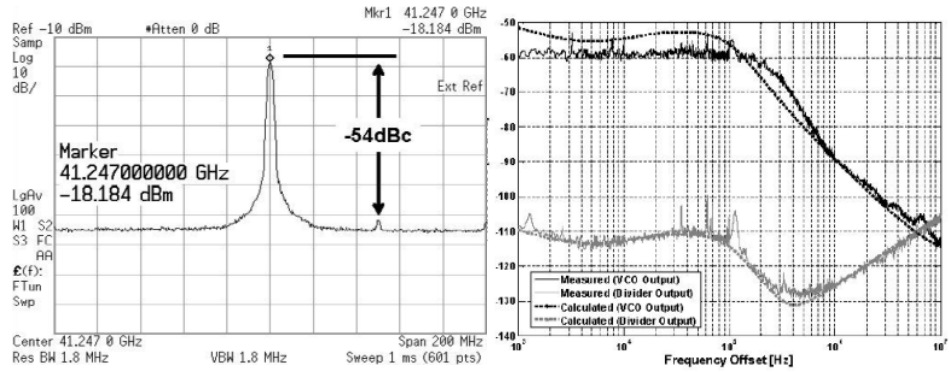
Figure 22: Output spectrum of Figure 19 PLL (left); Frequency Synthesizer Phase Noise at VCO and at FD chain output (right)

This circuit is one of the few examples, like [16], found in the literature addressing the issue of frequency synthesis in low down-conversion sliding-IF transceivers for mm-W applications with frequency calibration. In this thesis work we want to go further, investigating the possibility of increasing the VCO frequency and enlarging its tuning range, allowing the implementation in CMOS of zero-IF transceiver at 60 GHz.

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Chapter 3

3   STATE-OF-ART REVIEW OF mm-W FREQUENCY DIVIDERS

As already widely mentioned, the exploration of emerging mm-W applications has gained increasing momentum recently because of the wide available frequency spectrum. In addition to avoiding the interference of low gigahertz radio, the wide frequency spectrum at mm-W facilitates high data-rate communications.

To take advantage of the wide spectrum, the two primary challenges of developing CMOS Integrated Circuits (ICs) for mm-W applications are high operation frequency and wide frequency coverage.

Usually in high speed communication systems, the frequency synthesis is achieved by the on die high frequency VCO's output. Unfortunately the output frequency of this VCO varies with process, bias and temperature. These effects are much more important in CMOS technology (greater process variability, lower carrier mobility constants and smaller device breakdown voltages) when compared with more expensive process such SiGe, GaAs. In order to stabilize VCO output frequency, it is divided down, as part of a phase locked loop, and compared to a frequency stable low phase noise external crystal: this division is achieved by utilizing a FD.

In a frequency synthesizer for applications in the mm-W band, due to speed requirements a FD-by-2 is typically used as the first stage of the divider chain in the PLL feedback loop. To cover the required VCO frequency range and PVT variations, the divider locking-range needs to be maximized. Usually this operation results in higher power consumption and larger VCO load [1]. Moreover, the following divider stage, see Figure 17, has still to operate in a frequency range that is high, i.e. in the 20 to 30GHz range if the VCO frequency is around 60 GHz.

The FD is the first block in the feedback loop of a PLL, so it is the block that has to work with the maximum operating frequency; it is possible to say that the its fundamental task is to "relax" the operating frequency of the following blocks, by lowering it; therefore, the first stage of the FD chain, Figure 23 , is the critical design in a typical mm-W PLL system, besides the VCO itself, because of its high-speed operation.
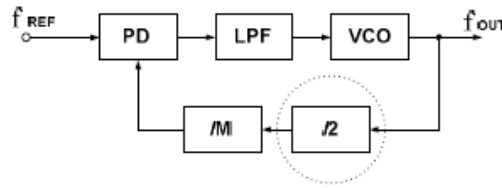
Figure 23: Typical high speed PLL blocks diagram

As a summary, for high frequency PLLs, the crucial blocks are the VCO and the FD: wideband and high operating frequency FDs are required for mm-W applications, in order to implement high speed transceivers to transmit and receive serial data at tens of gigabits per second.

At high operating frequency, the trade-off between operating frequency and dividing range of FDs becomes more important. For mm-W broadband communication systems, by now it is clear that there is the need of wide dividing range at high input frequencies. That is, high-speed and wideband FDs are critical building blocks for modern high-frequency wireless communication systems. The dividing range of a FD is defined, for a fixed input power level, usually 0 dBm, as $100 \times (BW/F_c)\%$, where BW is the bandwidth in which the divider works properly, i.e. $BW = f_{max}-f_{min}$, and F_c is the centre frequency, that is $F_c = (f_{max}-f_{min})/2$.

While the FD phase noise is not a so severe design issue compared to the VCO phase noise, since the noise of the output frequency depends mainly on the VCO phase-noise, however the prescaler (an alternate notation for the FD) sensitivity is an important and critical constraint.

Figure 24 shows the performance, in terms of sensitivity, of the frequency prescaler for 60 GHz applications proposed in [2]:
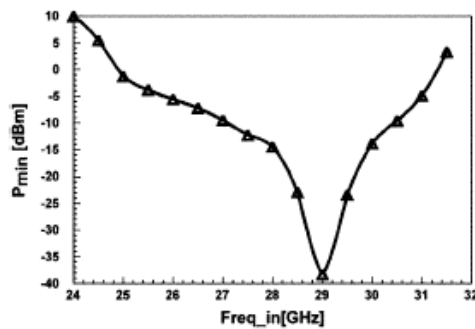
Figure 24: Frequency Divider input sensitivity

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The sensitivity of a prescaler is characterized, for each frequency, as the minimum input power, that is the VCO output amplitude, required to correctly divide the VCO frequency.

3.1 Frequency Dividers Topologies

The FDs or prescalers can be categorized into digital and analog circuit implementations. The digital implementation of FDs is based on flip-flop logic circuits [3]-[9]. The analog implementation of FDs includes ring-oscillator-based injection locking [10]-[11], frequency regeneration [12]-[18], and resonator-based injection locking [19]-[25].

The flip-flop-based FDs have the advantages of wide dividing range and various division ratios, but usually suffer from high power consumption and low operation frequency. On the contrary, the analog FDs are capable of high-frequency operation with low power consumption, but they usually suffer from small dividing ranges. Lately, ILFDs are very popular for mm-W applications because they feature the highest operation frequency and lowest power consumption among the dividers implemented with a specific semiconductor technology; the drawback is the limited dividing range, which is directly related with its locking range.

In order to clarify FDs topologies, a list of them will be provided, for high-frequency application:

- Current Mode Logic (CML) FD

- Miller Divider

- Dynamic Logic FD

- Injection Locked FD (ILFD)

In the following sub-sections a performance comparison among the topologies is illustrated. Next, a more detailed analysis of CML and ILFD implementations is presented.

3.2 Performance and Efficiency Comparison of Frequency Dividers for mm-W Applications

As we have seen in the previous chapter, PLL is a block that consumes a large part of the overall power consumption of the RF front end. It is obvious the need of FDs where the low power consumption and low cost are a must, if mm-W applications want to become a worldwide service.

Current Mode Logic (CML) FDs have been quite used for frequency division in frequency synthesizers, due to the wide dividing range provided. But for high operation frequencies, i.e. for taking advantage of the unlicensed 7 GHz WirelessHD^TM band around 60 GHz, they show a limit due to the speed requirements. Furthermore, CML FDs are a topology that could be defined as "power-hungry", since its sample and hold stages require high power consumption. In the next pages, some state-of-art CML FDs are presented.

Miller dividers suffer of high power consumption, as well; also, it is important to note that the Miller topology is difficult to be realized in CMOS technology, due to insufficient transconductance of MOS devices necessary for loop gain, at mm-W band. Some techniques to extend its operation frequency up to 40 GHz have been proposed, like LC band-pass load, but the small locking range of 6%, obtained is insufficient for 60 GHz applications where nominal 12% locking range is needed.

Other topology, **dynamic logic dividers**, presents low power consumption, but they have shown a fundamental limit for the maximum operating frequency, which is a problem when working at mm-W band.

Injection Locked Frequency Dividers (ILFDs) have captured the interest, for short-range high speed data communications around 60 GHz, mostly for its low power consumption, if compared to CML and Miller topologies, and for its high operation frequency.

Figure 25 shows a basic divide-by-two ILFD circuit. Its inherent self-oscillation frequency is designed to be only half of the input signal frequency, if the division factor is D=2. For a generic division factor D, the divide-by-D ILFD is designed in order that its self-oscillation frequency is 1/D of the input signal frequency.
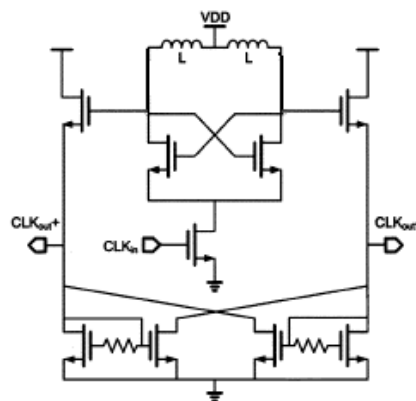
Figure 25: Conventional ILFD structure

The big drawback of the ILFD is its limited bandwidth. Therefore it is imperative, at mm-W, to maximize the locking range of such divider topology, ideally to expand the 7 GHz of the unlicensed band. But, in reality, the locking range has to be higher than 7 GHz, in order to cover properly the required VCO frequency range and to overcome PVT variations.

In order to overcome such critical drawback, a possible solution could be increasing the amplitude of the injected signal; but this means increasing the power consumption, as well as the VCO load. Furthermore, it could be possible to realize a ring-oscillator based ILFD [26], at the expenses of a higher power consumption. Also, a series inductive peacking technique has been proposed in [27], but at the expenses of increasing critically the chip area and therefore the cost. It is clear and worldwide accepted that it is tremendous challenging to design a wide locking-range and low-power ILFD for mm-W applications, and this is still considered a research objective.

3.3   PVT Impact in sub-100 nm RF CMOS Technology

As already mentioned, in PVT acronym P is referred to **P**rocess, that is the overall alteration from nominal doping concentrations in ICs manufacturing causing non-univocal simulation models for the devices reflecting in poor comparison between simulations and measurements. The letter V is referred to **V**oltage, in order to consider the realistic case in which the DC voltages provided by the voltage sources in the set-up measurements are not constant in time and not exactly equal to the nominal simulated values. T is related to **T**emperature and considers the fluctuations of the devices parameters caused by temperature variations.

There is a big impact of PVT variations when designing in CMOS technology, especially at mm-W frequencies and in sub-100nm processes, as reported in many works like [28]-[29]. In this section the concept of PVT variations is revisited briefly, in order to analyze and try to quantify their effects over analog-RF CMOS design for FDs.

About device models, they are provided by the foundry and a designer must trust in their behaviour in mm-W band; but the reason of difficult design due to the technological environment, is linked also to the accuracy of such device models.

Regarding process variations, we must consider active and passive devices. Because of unavoidable uncertainties during manufacturing process, integrated circuit suffer deviations from their nominal characteristic due to inter-die (1) and intra-die variations (2). Inter-die variations affect all the devices of the same die simultaneously, being fluctuations in parameters from lot-to-lot,

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wafer-to-wafer and die-to-die. A typical analysis to predict the worst case of performance is the corner analysis (SF, SS, FF, FS). In Very Large Scale Integration (VLSI) for digital electronics, considering a NMOS and PMOS transistors forming a complementary logic port, the first letter of "SF, SS, FF, FS" refers to the N-channel corner and the second letter is referred to the P-channel corner. In this convention, three corners exist: Typical, Fast and Slow. Fast and Slow corners exhibit carrier motilies higher and lower than normal (Typical), respectively. For example the corner FS denotes fast NMOS and slow PMOS. Therefore following this convention there are four possible corners (FF, FS, SF, SS) plus the typical one, denoted as TT. In the three corners TT, SS and FF both devices are affected evenly, and generally do not adversely affect the logical correctness of the circuit. However, the resulting devices can work at slower or faster clock frequencies, and they are often not usable for the application requested. The last two corners (FS, SF) are cause for concern. This is because one type of MOS will switch much faster than the other, and this form of imbalanced switching can cause one edge of the output to have much less slew than the other edge.

Intra-die variations consist of both random and deterministic variations and cause a non-uniform distribution of the devices electrical characteristics. Montecarlo analysis is required to predict the behaviour of the circuit taking into account those variations. Intra-die variations are very critical in analog design, since they affect the matching between two nominally identical devices, leading to errors in differential structures.

Due to the constant technological scaling, typical sources of variations in active devices are the random dopant fluctuations [30]-[32] and Line-Edge (LER) and Line-Width Roughness [33]-[34].

Other sources of process variations are:

- Variations in the Oxide Thickness [35]

- Fixed charge in the oxide [36]-[37]

- Defects and traps [38]

- Patterning Proximity effects [39]

- Strain [40]-[41]

- Implant and anneal [42]

Figure 26 shows process variations in a VCO [28] tuning range and divider free-running frequency over a wafer: these inter-die variation patterns are very systematic: the cross correlation between different wavers is more than

90% on average. From the measurement of 65 dies (sites) it has been demonstrated that the VCO tuning range variation is mainly caused by the variation in the MOS varactor.
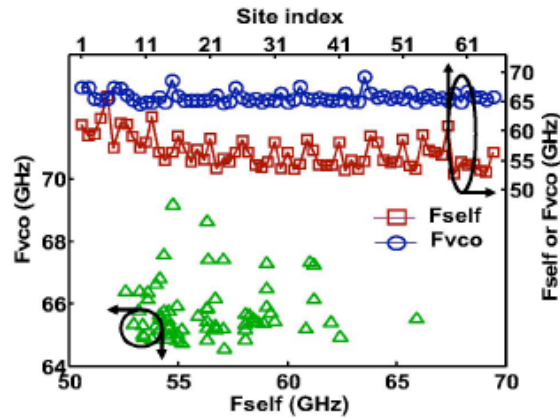
Figure 26: Inter-die variation of VCO frequency and FD self-oscillation frequency over a wafer with scattering diagram

As it is possible to note, VCO and FD operating ranges do not track each other in the presence of significant inter-die variation. The scattering diagram suggest an important concern in PLL front-end design at mm-W frequencies in a RF CMOS technology: the divider operating range must cover the VCO tuning ranges in the worst case corners combinations in order to guarantee high manufacturing yield.

About process variations in passive devices, analog-RF design also depends on them, in contrast with digital design. Process variability in inductors, capacitors and resistors is a well known issue. Passive devices design should not be based on nominal value of the components whenever possible. Instead, the ratio of two or even components is preferable and, sometimes, replacing passives with active counterparts may help to reduce process variability impact in analog ICs, even if the active solutions still remain less attractive because active devices suffer from more aggressive non-ideality and parasitics. For rationed passive devices, the intra-die process variation, that is mismatch, becomes the important problem.

Nevertheless, in RF design there is the need of exact component values, for example to set a VCO center frequency. Therefore, circuit design by using rationed passive devices is not always possible, and so component value variations due to process variations must be taken into account. RF circuits like power amplifiers, LNAs, LC based VCOs and ILFDs are very sensitive to process variations in passive devices, because in such circuits impedance-

noise-power matching and resonant frequency are key issues. Usually, when designing a tuned circuit, process variations of passive devices have a critical impact. Hence it is realistic to assume that PVT variations have a critical impact in a CMOS ILFD at 60 GHz, since, has already mentioned, the ILFD has a self-resonance frequency which is affected by PVT variations, reflecting in an impact in the correct PLL operation, for the reasons exposed. However, also CML topology has shown to be affected. For rail-to-rail square wave a 65 nm SOI CMOS technology CML prescaler can be analysed as a digital flip flop. But, for weak input signals around twice of the free-running frequency, it has been reported [29] that the operating mechanism of the CML becomes similar to an Injection Locking Oscillator (ILO), therefore suffering the same type of PVT induced variations.

Bias Voltage (V_{BIAS}) variations impact tremendously in the behavior of the FD, and they are translated directly to the self-oscillation frequency, potentially decreasing the operating frequency range by moving the dividing range out of the preceding VCO output frequency band. Figure 27 shows the simulated input sensitivity curves of a CML latch structure FD [29] at various V_{BIAS}. A higher bias voltage results in higher free-running frequency, even if the supply voltage is adjusted to achieve the nominal current consumption. These curves show that generally the divider operating range is highly sensitive to V_{BIAS}.
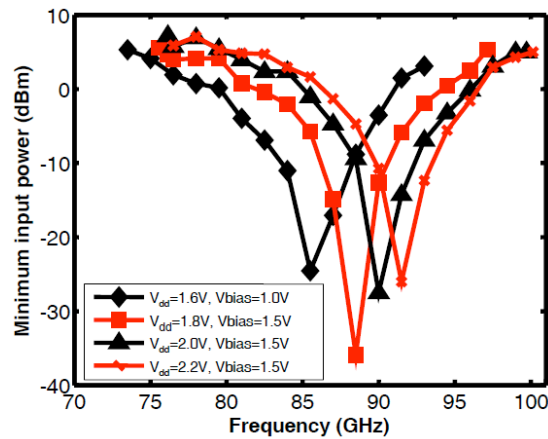
Figure 27: Sensitivity curves at different V_{BIAS}

It has been reported in [43] that the self-oscillation frequency of a prescaler depends on bias current, load resistance, and parasitic capacitance at the output nodes. Furthermore, the bias current is highly sensitive to the bias transistor threshold voltage variation. The threshold voltage variation affects the FD, similarly to the V_{BIAS} changes shown in Figure 27.

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Figure 28 depicts how the changes of V_{BIAS} have an impact in the operation of the PLL front-end in IBM 65 nm CMOS technology. As it is possible to see in the inset plot, the VCO is relatively robust against device skewing, if compared to the divider. Moreover, it is possible to note that the divider sensitivity curve is well below the VCO output power over the VCO tuning range for a particular value of V_{BIAS}. A slight variation makes the VCO output power move just partly below the sensitivity curve in the VCO tuning range, resulting in a failure zone as shown in the figure.
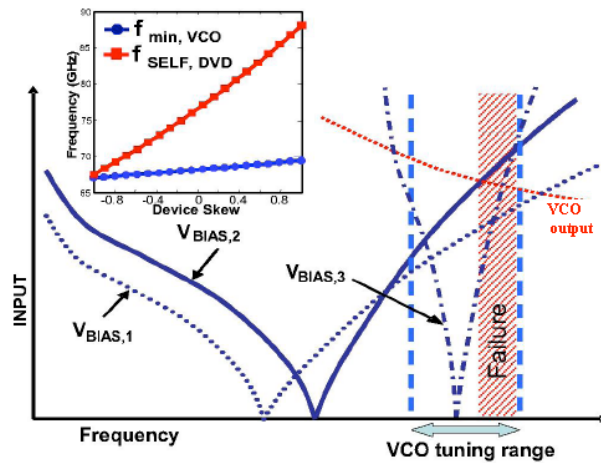
Figure 28: Effects of voltage variations in input sensitivity and locking-range

As a summary for this case of study, V_{BIAS} can be increased in order to centre the VCO tuning range, but it results in a very steepened sensitivity curve. Furthermore, a V_{BIAS} too high results in larger output swing and provides larger gate over-drive of input devices, so that increasing V_{BIAS} to stabilize divider performance against threshold voltage variation have critical drawbacks. Another challenge is to find an optimal V_{BIAS} to solve the trade-offs in a PLL design.

From the previous examples, it becomes clear the critical and tremendous impact of PVT variations in the design of CMOS VCOs and FDs at mm-W frequencies. This is one of the reasons, probably the most important one, why achieving around 60 GHz a wide FD dividing range is still a research objective.

In the remaining part of this chapter, some published works regarding FD design at mm-W frequencies in CMOS technology will be visited and analysed, with a special focus on CML and ILFD structures. FDs are used as the first stage division in the PLL, basically in order to reduce the VCO output

frequency in the PLL feedback loop and therefore only such two fast operating FD topologies are considered.

3.4   Current-Mode Logic (CML) Frequency Dividers

The fundamental element of a digital FD is a flip-flop, that is two level sensitive latches in master-slave configuration. A wide variety of D-flip-flop circuits have been reported in the literature. CML latch was first introduced in [44] and some modified latches can be found in [45]-[46]. The CML latches exhibit better performance in terms of speed than other latch structures.

3.4.1   Conventional CML Latch

In general, a CML circuit consists of three main components, as shown in Figure 29, which includes the pull-up load, the Pull-Down Network (PDN) and a constant current source. CML is a completely differential and static logic. Due to its differential nature, it is highly immune to common mode noise.
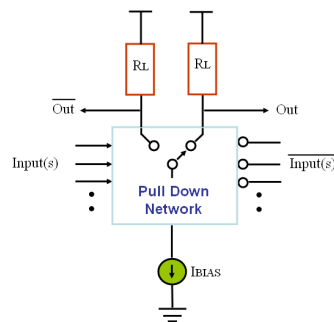
Figure 29: Generic CML structure

Depending on the input combination and on the logic implemented by the PDN, all the current flows through one of the two differential branches, providing complement output signals. Voltage at the output of the branch with no current reaches V_{DD}, whereas for the other branch some voltage drops across the load resistor and the output voltage becomes V_{DD} - $I_{BIAS} \cdot R_L$.

The reduced voltage swing makes it a faster gate compared to rail-to-rail logic families [46] due to quick voltage transition and. In general, it is possible to say that, from a power consumption point of view, it is the better solution among the other logic structures used for frequency division at high frequency, even if its power consumption increases with the frequency.

For designers, a thorough understanding of latch timing parameters, like setup time, hold time, Clk – Q delay, etc. is essential for reliable operation, especially as the operation frequency increases. Speed optimization in CML FDs is another and particular critical issue. For clarification the parameters are stated. **Setup time** is defined as the minimum time before the clock edge by which the data should be stable in order to be captured as the next state. It should be noted that satisfying this condition does not necessarily mean that the output will change accordingly. **Hold time** is defined as the minimum time after the clock edge until which the data must be hold in the same state.

For successful and reliable operation both conditions must be satisfied. These times define a sampling window, in which the data is captured as next state. Any data change in that window will result in failure of the latch operation. The minimum width of the data pulse is, therefore, the sum of setup and hold time.

Measurement of setup and hold time for comparison is not trivial, because the time the data changes before the clock edge, i.e. the D-Clk delay, as depicted in Figure 30, depends on hold time. If the change in data occurs sufficiently before the clock edge, the hold time is constant and it does not depend on D-Clk delay. This is known as the stable region. As D-Clk delay decreases, at a certain point the hold time starts to rise exponentially. This region is called the metastable region. As the D-Clk delay further decreases, setup time violation occurs. Any change in data after this point cannot be transferred to the output. This is known as the failure region.
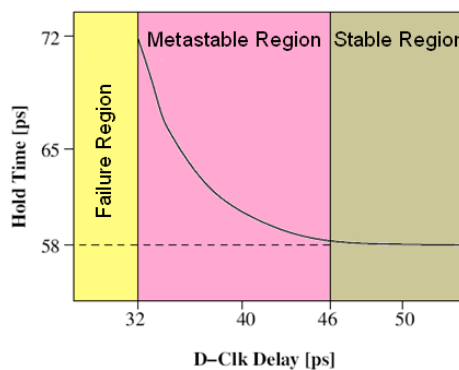
Figure 30: Hold Time for MOS CML latch

Another important parameter is Clk-Q delay, which is the time between the triggering edge of clock and the change in the output (Q), provided that the data changes before the minimum setup time. In the metastable region, as reported in [47], the D-Q delay reaches its minimum value which is smaller than

setup + the Clk-Q delay in the stable region. Obviously the cycle time will be reduced if the data changes near this point. Therefore the minimum D-Q delay is the only true measure of the performance of a master-slave latch or flip-flop.

A conventional current mode logic latch consists of a sample and a hold stage, as shown in Figure 31.
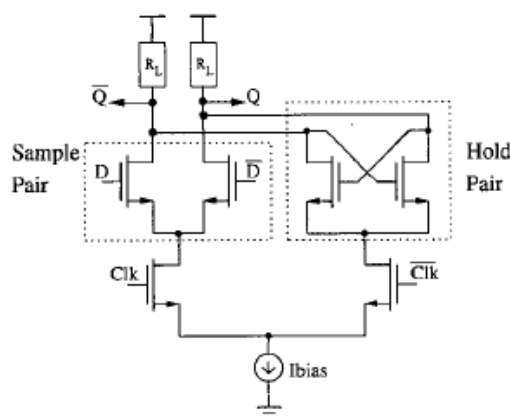
Figure 31: Conventional CML latch

The sample pair works as a CML buffer and when it is activated by the clock signal, it keeps track of the input data and translates it to the outputs. This is known as the sampling mode of the latch. Small propagation delay in the sampling mode and isolation from the data in hold mode through current switching are the most important issues in the CML latch performance. When the clock polarity changes the hold pair becomes active. The cross-coupled transistors in hold pair form a regenerative positive feedback structure and keep the output data in the same previous state. This is known as the hold mode because the output is isolated from any changes in the input data, as no current should be flowing through the sampling pair. In the stable region the propagation delay (D-Q) is a function of the total output capacitance and load resistance, $T_{DQ} = C_{TOT} \cdot R_L$. If the data changes near the clock edge the D-Q delay increases due to finite current transition time and causes metastability at the output.

3.4.2   Other Modified CML Latches

Some modified latch structures are found in the literature for improved performance. In [46], the regenerative latch is modified so that the sample circuit and the hold circuit use two distinct tail currents. Because of the parasitic capacitance of the transistors of the sample circuit, the tail current must be sufficiently high to achieve a wider range of linearity and a larger

transconductance. On the other hand the hold circuit does not need a large bias current. This technique shows significant improvement. However it increases the static power consumption and circuit complexity.

The maximum operation frequency of MOS CML is reduced by the variation of the threshold voltage (V_{th}). A feedback CML D-Latch has been proposed in [47] for improving performance against V_{th} variations. Feedback transistors are connected between the input and the output, as reported in Figure 32.
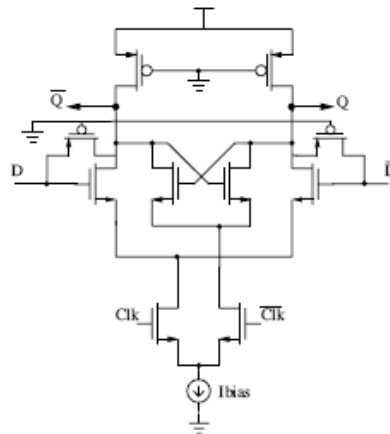
Figure 32: Feedback CML latch

The effect of these feedback resistances results in wider operation bandwidth, or at the same operating frequency, results in larger stability against threshold voltage fluctuation. Since feedback transistors are connected between data inputs and outputs of the latch, in hold mode any change in the input data will directly affect the output state. As MOS CML output swing is relatively small, these fluctuations in the output may result in a false state and metastability in the master slave configuration.

Another important aspect is the input to output coupling and clock feed-through due to the device overlap capacitances. This effect can be eliminated using the capacitive feedback. However any additional capacitance connected at the output should be avoided because it will result in higher D-Q delay. Cross-coupled capacitors connected at the Clk transistors will neutralize the effect of clock feed through. At high frequencies these capacitors can result in spikes at the output due to sharp clock edges. The addition of a series resistance can eliminate this problem. However, a purely resistive component will try to equalize the differential outputs resulting in failure of the latch operation. So a high resistance is required for clock feed through cancellation.

As it is not area efficient to use large capacitors in a integrated environment, a cross-coupled feedback transistor pair at the Clk terminals will suffice for the requirement of both the capacitor and resistor, as shown in Figure 33 and it was reported by [48] as clock-feedback CML latch structure. This circuit topology has significantly improved the performance in terms of speed as compared to normal feedback structure, and the latch operation is more reliable. It also results in reduced dynamic power dissipation due to more stable output.
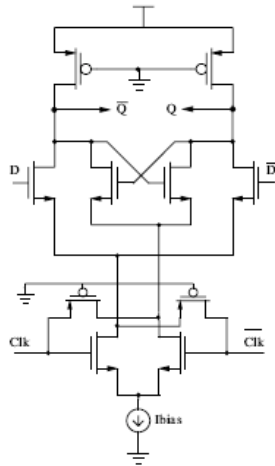
Figure 33: Clock-feedback CML latch

The aspect ratio of feedback transistors $(W/L)_{FB}$ should be kept small for higher resistance, whereas larger width is required for more capacitance. However larger $(W/L)_{FB}$ will create instability and spikes at the output, or complete failure at the extreme. So careful sizing must be performed according to other transistor sizes and currents in the latch.

3.4.3   CML Frequency Dividers for 60 GHz Applications

In the work of [49], a 43 GHz 2:1 FD in IBM 0.13μm CMOS was implemented. The manufactured NMOS transistors used have a f_t of 100 GHz. To reach that operating frequency, the frequency divider adopts Shunt Peacking (SP) spiral inductors and Split Resistors (SR) loads to boost the bandwidth and to reduce parasitics capacitances and Miller Effect, which is a compromise between high internal voltage swing (DC gain) and reasonable RC time constant.

The FD is shown in Figure 34 (left) and it consists of a master-slave flip-flop (MS-FF) with feedback from its output to its input and a 3-stage output buffer, not shown in the figure, which provides better signal waveform, appropriate amplitude, proper DC level and good output matching.
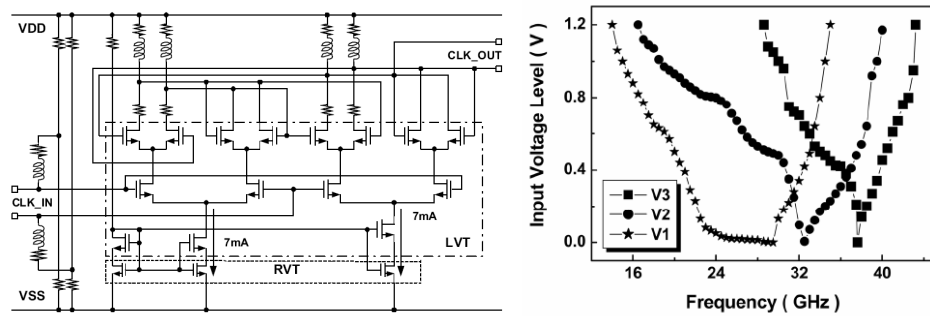
Figure 34: 43 GHz CML frequency divider (left). Input Sensitivity curves (right)

The FD Master-Slave flip-flop consists of two latches connected in series. All the transistors used are NMOS, since they have higher speed if compared to the PMOS. They are low V_T 120 nm NMOS devices, allowing low supply, like 1.2 V or less. The latches use series gating between clock and data inputs. In order to reduce parasitic capacitance at the output nodes and to make the clock pairs switch more easily, all the data path transistors are 2/15 the width of the clock transistor. In order to speed up the sampling-holding process, the hold stage transistors size is slightly smaller than the size of those in the sample stage.

To achieve very high operating frequency and low phase noise, SP coils are implemented using on-chip spiral inductors with high Q-value. Both latches and output buffer employ stacked current sources to achieve higher output impedances and more stable DC operating points. In addition, NMOS transistors with a channel length of 180 nm are used as current source to reduce short channel effects and geometric mismatches.

The overall power consumption of the frequency divider is 40 mW, from a 1.2 V power supply. In the reported work a comparison among the master-slave flip flop using a conventional CML frequency divider (V1), the same structure but with SP spiral inductors (V2) and the new topology using SP and SR (V3), corresponding to the schematic of Figure 34 (left) are compared by reporting the input sensitivity curves, self-oscillation frequencies and amplitudes of the three frequency divider versions operating under 1.2V supply, as shown in Figure 34 (right). As it is possible to note, V3 operates at the highest frequency of 43.2 GHz, which confirms that the employed on-chip spiral SP inductors and SR loads can greatly improve the operating speed of CML circuits up to 50%. The reported work also has demonstrated that the frequency divider operates at higher frequency and larger output swing under a higher supply at expenses of higher power dissipation. However, as clearly seen in the figure, the dividing range is reduced as the operating frequency increases.

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In the following reported work [50], a design procedure that can be used to achieve high-speed performance and low power consumption without self-oscillation condition was proposed. Using such procedure, a static CML divider-by-2 that realizes a division range from 12 to 40 GHz with 12 mW power consumption on standard 0.13-μm CMOS has been realized. Figure 35 (left) illustrates the schematic of the proposed static FD-by-2. The divider uses a conventional CML structure with master and slave latches.
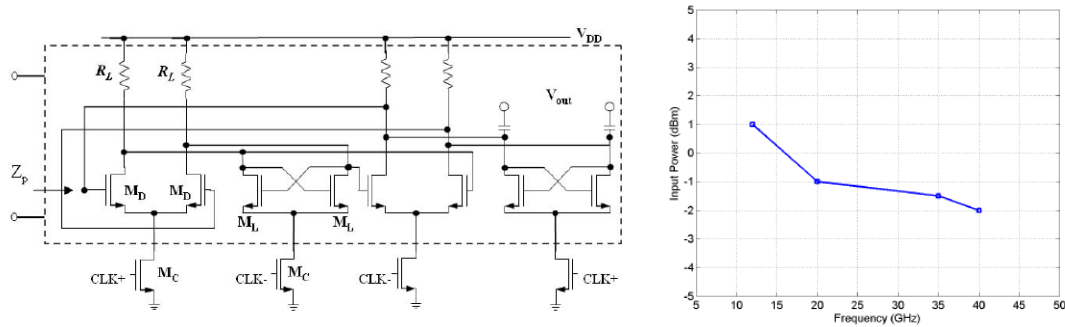
Figure 35: 40 GHz CML FD w/o self-oscillation condition (left). Measured input sensitive curve of the divider (right)

An important design step was to optimize the size and layout of the transistors since routing has an important impact in the speed performance and power dissipation. The transistor sizes of the latch transistor M_L and drive transistor M_D were optimized, while satisfying $g_{mL} \cdot R_L > 1$ to guarantee self-oscillation [51], where g_{mL} is the transconductance of latch transistor M_L. This self-oscillation condition is a conservative condition as it is sufficient but not necessary for the circuit of Figure 35 (left) to work as a divider. It has limited the operating frequency below the 30 GHz, in order to achieve the negative resistance to ensure self-oscillation. A Z-parameter aided technique for estimating the maximum division frequency has been proposed in the presented work. This approach involves optimizing the latch and drive transistors independently.

The size of the latch transistor M_L must guarantee that the clock transistor M_C remains in the saturations region. At this point the structure is simulated and it is established that the device operates as a divider. The next step was to optimize the drive transistor width. The drive transistors were optimized, by fixing the current through them starting from low power consumption constraint.

In [52] it was shown that the ratio of g_{mD}/C_{gd} impacts the maximum division frequency where g_{mD} and C_{gd} are the transconductance and gate-drain

overlap capacitance of the drive transistor M_D. Following the approach reported to optimize the latch transistors it is possible to vary the width of the drive transistors such that the peak of the maximum absolute value of the real part of the input impedance occurs at the maximum frequency.

In the measurements the divider, which shows no self-oscillation, achieves 2:1 frequency division from 12 to 43 GHz. Figure 35 (right) gives the measured input sensitivity curve. It is interesting to observe that this input sensitivity curve of the proposed divider does not exceed 43 GHz frequency, and it is different from the usual "V" curve as reported previously and in other works [53]-[54].

Usually, in order to ensure self-oscillation, a sufficient but not necessary condition, most of the previously referenced CML prescaler designs rely on reduced technology feature sizes and/or increased power dissipation in order to realize higher speed operation. This approach limits the application of CML dividers when compared with competing dividers such as injection-locked dividers that are going to be analysed in the following pages.

The highest operation frequency of a CML divider demonstrated and reported previously in 180 and 130 nm CMOS technology is around 40GHz. Other most recent works in 65nm have achieved higher operation frequency with CML based FDs, like [55], in order to allow their implementation in a 60 GHz direct-conversion transceiver. Nevertheless, the locking range achieved seems not enough to cover the WirelessHD[TM] bandwidth taking into account PVT variations and it is clear the need of calibration techniques that in the case of the proposed design should lead to implement very complex architectures.

3.5   Injection-Locked Frequency Dividers

In this sub-section, ILFD topology will be studied and analysed. As previously mentioned, ILFDs have captured the interest of the designers for application in mm-W band, mostly for its lower power consumption and for its higher operation frequency, if compared to static CML topology.

CML FDs have been already analysed in the previous sub-section, exposing their limits for mm-W applications. On the other hand, Miller-based FDs are difficult to be realized in CMOS due to insufficient transconductance of MOS devices necessary for loop gain. To overcome this problem, a bandpass-load was adopted to extend its operation frequency up to 40 GHz [56] but the small locking range of 5.75% obtained is insufficient for 60 GHz applications, where nominal 12% locking range is needed.

Although both Miller and CML dividers have been demonstrated in mm-W range, they require high power consumption. The divide-by-D ILFD is viewed as the suitable candidate for low power mm-W operation with respect to a fixed transistor f_t (cut-off frequency) because its inherent self-oscillation is designed to be only 1/D of input signal frequency. However, ILFD has the drawback of limited locking range and hence, some techniques have been proposed to improve it.

Ring-based ILFDs [57]-[58] show the wide locking range due to the inherent wideband self-oscillation property of the ring structure. Nevertheless they have the drawback of higher power consumption, as it will be shown in the next paragraph.

A conventional LC-based divide-by-two ILFD is shown in Figure 36. In the conventional topology, the input stage M_{in} is used to provide both an input signal path and a dc bias path. The input signal at f_{in} is applied at the gate of the bias transistor M_{in} (the RF input signal path is DC decoupled) and then injected into the ILO which is self-resonating at $\approx f_{self} = f_{in}/2$. Thus, M_{in} is typically large, resulting in a large input capacitance. Moreover, the input signal is significantly degraded by the parasitic capacitor C_{tail}. By using a peaking inductor between the drain terminal of and the ground, this problem can be reduced, by resonating out C_{tail}; however, this strategy requires a greater chip area. In the conventional ILFD topology the injection from the current source can be considered as indirect, since the input signal is not directly injected into the ILFD tank.
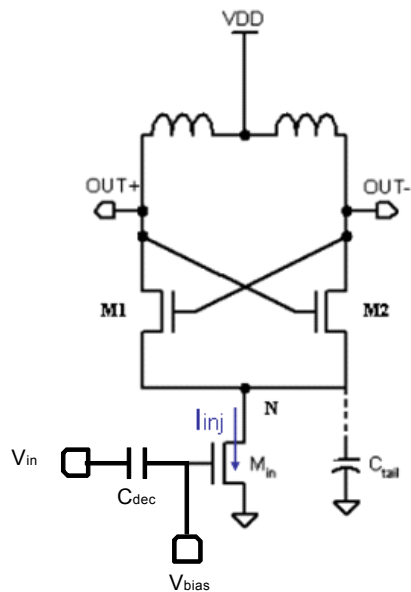
Figure 36: Conventional ILFD

If the circuit of Figure 36 divides correctly, transistors M_1 and M_2 switch at a rate of $f_{in}/2$ while M_{in} injects a current at f_{in}. Thus, in a way similar to a single-balanced mixer, M_1 and M_2 translate the input to $f_{in} \pm f_{in}/2$, injecting the result into the tank which is designed to resonate at $f_{in}/2$, if the FD division factor is 2. This translation is accompanied by a conversion factor of $2/\pi$ [56] if the cross-coupled pair switches abruptly and the capacitance at node N is neglected. As a result, the current injected into the tank at $f_{in}/2$ has a peak value of $(2/\pi) \cdot I_{inj}$, allowing to find an expression for the locking range of the ILO of Figure 36, that has been reported, by simulations and measurement results, to be accurate enough:

$$\Delta\omega\Big|_{\frac{f_{in}}{2}} = \frac{\omega_n}{2Q}\eta\frac{2}{\pi} \tag{1}$$

where η is the injection efficiency equal to I_{inj}/I_{osc}, I_{osc} is the oscillation current, approximately equal to the tail current, ω_n is the resonant angular frequency of the tank and equal to $2\pi \cdot (f_{in}/2)$ when the circuit works properly, and Q is the quality factor of the tank. In (1), the subscript $f_{in}/2$ emphasizes that the locking range is measured at the output. It follows that the lock range at the input is equal to:

$$\Delta\omega\Big|_{f_{in}} = \frac{\omega_n}{2Q}\eta\frac{4}{\pi} \tag{2}$$

In order to overcome to the problem related to large injection transistors in the conventional topology, the direct-injection ILFD structure is considered. The following Figure 37 depicts a direct-injection ILFD, in which the bias circuit is omitted:
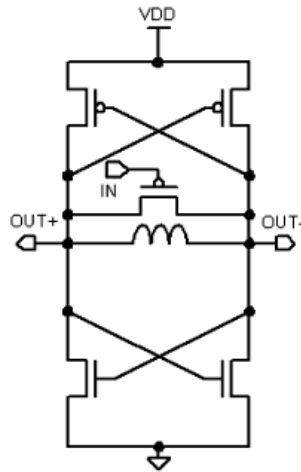
Figure 37: Direct ILFD arquitecture

With this injection architecture, the problem related to signal degradation, due to the parasitic tail capacitor in the conventional scheme, is avoided. However, capacitive loads at the ILFD output nodes are present, as it will be detailed in Chapter 5. In order to resonate out those capacitances, a series inductive peaking [27] technique has been used to enhance the loop gain, reflecting in wider ILFD locking range, but large chip-area is required due to the use of inductors.

The injection transistor is in the tank and consequently its parameters must be carefully taken into account when designing and sizing the ILFD tank. As already mentioned, according to (1) it is possible to increase the ILFD locking range by increasing the amplitude of the injecting signal: but with direct-injection arquitecture this could be done at expenses of higher power consumption, as well as providing a higher VCO load, decreasing its tuning range, since the injection transistor would be "over" sized. Furthermore, one has to take into account that, at mm-W, a VCO provides relative lower output power level if compared to others operating at lower frequencies, due to the physical and technological environment. This consideration leads to design strategies that are going to be presented in chapter 5.

Accordingly to both (1) and (2) the ILFD locking range is inversely proportional to the Q factor of the tank. However, it has been demonstrated that for a direct-injection ILFD [59], increasing the Q factor can reduce the power consumption without reducing the locking range. This result differs from the conventional one. In chapter 5, where the proposed ILFD design object of this Thesis is discussed, a locking range comparison between high-Q and low-Q tanks ILFD will be reported with simulation results.

3.5.1 CMOS ILFDs for 60 GHz Applications

As reported in [59], three guidelines can be followed in order to achieve a larger as possible locking range when designing a FD with injection locked topology: 1) maximize the quality factor of the passive load; 2) maintain low output amplitude; and 3) increase the dc overdrive voltage of the input device. This approach contrasts with equation (1), regarding tank design, but the sensitivity curve reported in such work demonstrates an ILFD locking range larger than the one from a low-Q ILFD, with the advantages of lower power consumption. By applying such three design guidelines, the resulting circuit structure is "more" simple in the sense that it has no varactor, i.e., no tuning capability, but it still provides a large frequency locking range. The proposed ILFD circuit is shown in Figure 38 (left), and it uses a direct-injection structure:
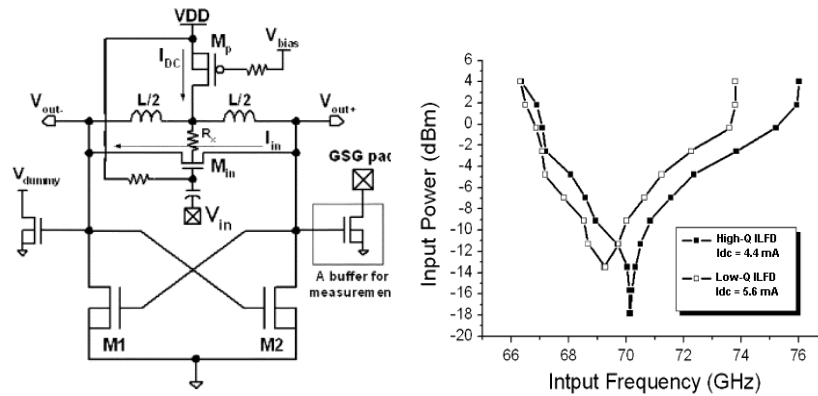
Figure 38: Direct structure for the high -Q ILFD reported (left). Input sensitivity curves (right)

Since the frequency locking range is inversely proportional to the total capacitance value at the output node, as reported in [60], the absence of a PMOS cross-coupled pair can significantly increase the frequency locking range. Adding a PMOS current source M_p, as shown in Figure 38 (left), provides two advantages over an ILFD presented in an earlier study [22], that furthermore help in increasing the locking range. Firstly, since a trade-off exists between the output voltage amplitude and the frequency locking range, the output voltage amplitude can be set to its minimum value by designing an appropriate dc current of M_p that maximizes the locking range. Secondly, the dc voltage at the output node can be set much lower than the VDD because the dc current is limited by M_p. Therefore, M_{in} can be biased in the high overdrive voltage region. Additionally, through the resistor R_x, the dc voltage at the substrate node of M_{in} can be equal to those at the drain and source nodes such that the threshold voltage of M_{in} can be kept low to increase overdrive voltage.

Nevertheless, such ILFD does not seem able to work at 60 GHz in presence of PVT variations, since the ILFD bandwidth is only slightly higher than WirelessHD[TM] band, and therefore it would not be able to cover it if taking into account process corners. Furthermore, the proposed strategy means low ILFD output power level, which is not completely suitable for its integration in a 60 GHz CMOS PLL and also it could lead to experiment oscillation start-up problems in some critical corner. The maximum measured locking range, corresponded to typical corner, is 13.6% (66.4–76 GHz) for a 0 dBm input power, with a I_{DC} of 4.4 mA from a 1 V supply.

In the following reported work [2], a frequency locking range of 25% (corresponding to 6.2 GHz bandwidth around 30 GHz) has been achieved, basically, by lowering the Q factor of the resonator tank. One can say that as the Q factor of the resonator tank decreases, the FD behaves as an ideal divider

once it is injection locked, also due to the larger bandwidth. However, it would be desirable not reducing the Q factor unlimitedly in order to achieve a larger locking range, since that results in a loop gain too small to start the oscillation. So, an optimum design point should be to choose a tank a with a Q as small as possible, while keeping the oscillation sustained for each PVT corner.

Figure 39 (left) shows the schematic of the above mentioned ILFD. In the colored area, the schematics of the output buffers are marked:
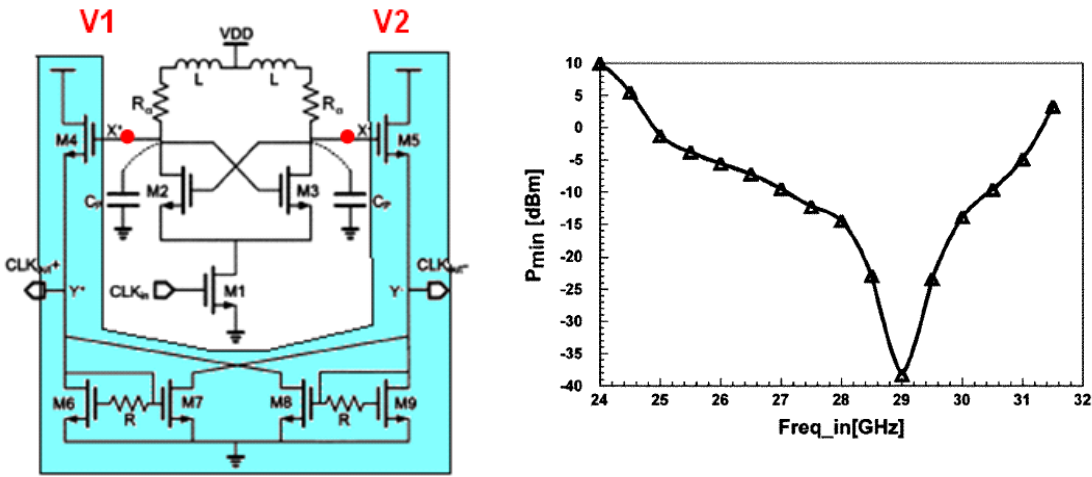
Figure 39: 30 GHz ILFD schematic (left). Input sensitivity curves (right)

The resistor R_α can be modelled as $R_\alpha = \alpha \cdot Z_0$, where Z_0 can be assumed to be 50 ohm. In a tank like that of the design of Figure 39 (left), where no capacitor and/or varactor are used, it is also possible to assume that α is almost equal to zero, because, basically, R_α is equal to the parasitic series resistance of L and dominates the overall Q factor of the tank:

$$Q_{tot} \approx Q_L \rightarrow Q_{C_P} \gg Q_L \tag{3}$$

C_P refers to the parasitic capacitance at nodes X and X´, i. e. the combined contributions from the transistor drain, input buffer gate and layout parasitic capacitances. If the condition $\alpha > 0$ is satisfied, i. e. if an integrated resistor is physically inserted in the schematic and layout, assuming to operate at the same frequency and in the presence of the same integrated coil:

$$\omega_0 = \sqrt{\frac{1}{LC_P} - \frac{R_\alpha^2}{L^2}} \tag{4}$$

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$$C_P = \frac{1}{\omega_0^2 L + \frac{\alpha^2 Z_0^2}{L}} \qquad (5)$$

The Q factor of the resonator tank in these conditions is:

$$Q_\alpha = \frac{\omega_0 L}{\alpha Z_0} \qquad (6)$$

According to (1) and (2), by lowering the Q factor of the resonator tank it is possible to increase the ILFD locking range. Nevertheless, in the reported work a comparison between low-Q and high-Q tank impact in the "almost" same ILFD is missing in order to better understand the effect of a low and high Q in the ILFD locking range, since as we have seen in the strategy of [59] a lower Q as a prerequisite for an higher locking range is not completely agreed among the designers.

The output buffer in [2] is a source follower with an active load. The most important problem of this buffer topology is that the leakage signal from input signal, corresponding to the 2nd harmonic of the self-oscillation frequency, will appear at the output. Nevertheless, in the reported work a mechanism that allows performing a 2nd harmonic cancellation by properly sizing the buffers transistors (basically sizing $M_4 = M_5 = g_{m1}$ and $M_6 = M_7 = M_8 = M_9 = g_{m2}$) is implemented.

Figure 39 (right) shows the input sensitivity curves. In this work, a wide locking range is achieved, but the operating frequency is just 30 GHz; therefore, the reported FD cannot be used in a PLL embedded in a direct conversion transceiver for 60 GHz applications. Several others techniques have been used to increase the locking range of ILFD: direct injection arquitecture with continuous tuning varactor has been implemented in [61] but this work fails to cover the full band at 60 GHz and it can only be used in sliding-IF 60 GHz transceivers. Moreover, the continuous tuning capability is not perfectly suitable for frequency calibration in high precision PLL for mm-W application. To optimize the locking range allowing higher operation frequency, transformer feedback [62] technique has been adopted, but at expenses of increasing critically the chip area, like in [27] where, as already commented, a series inductive peaking was used. A band switching [19] and power matching [63] techniques have been also used, but the achieved ILFD operation ranges and locking ranges avoid the integration of these ILFDs in direct conversion transceiver for WirelessHD[TM]. Also, forward body biasing technique, applied to the direct injection scheme in order to increase the locking range, have been proposed in [64]-[65], but even if the locking range is slightly increased, its little

improvement does not justify the big complications in the layout that such technique requires.

Designing a wide locking range CMOS ILFD at 60 GHz is not trivial, and this is the main reason for the proliferation and adoption of different schemes and injection topologies. Nevertheless, until now it continues to be an open issue. This is the main aim of this thesis: the co-design and co-fabrication of a wide locking range ILFD and VCO both operating at 60 GHz for a PLL of a direct conversion transceiver.

3.6   Calibration Techniques

As already exposed, in a PLL for mm-W applications the FD and VCO operational range may not align exactly, due to the inaccurate passive/active device modeling and large PVT variations at 60 GHz. So that a calibration technique is required to allow the ILFD to cover properly the VCO tuning range. In this section we are going to visit calibration techniques that have been implemented in ILFDs, inside the PLL, in order to overcome to the limited locking range. In the referenced work [66] a digitally calibrated PLL in 130 nm CMOS technology has been proposed. The block architecture shown in Figure 40 (left):
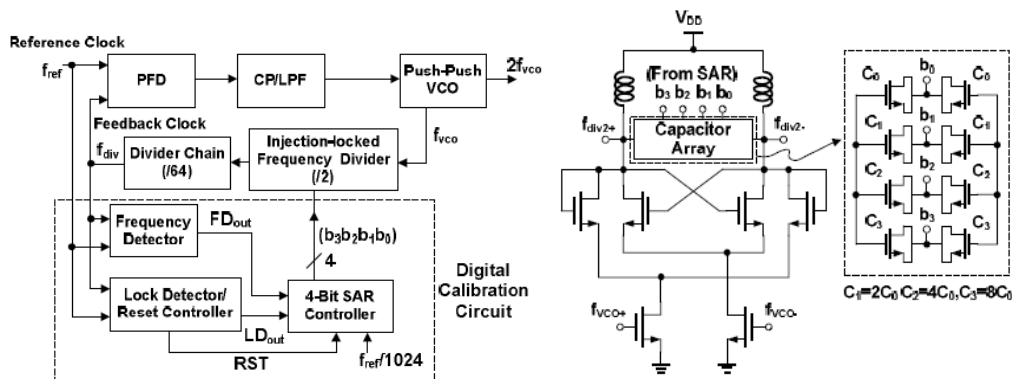
Figure 40: Digitally calibrated 60 GHz PLL (left). Divide-by-two ILFD schematic (right)

The VCO is composed by a conventional LC-based VCO with continuous tuning capability and a push-push frequency doubler. The push-push VCO tuning range is 64-to-66.4 GHz. The first divider stage is a fully differential divide-by-two ILFD in which the ILFD tank capacitance, formed by a capacitor array, is digitally controlled with a four bits bus. Its schematic is reported in Figure 40 (right).

By using the ILFD discrete tuning mechanism, the ILFD locking range can be shifted in frequency and such capability is used in order to implement the calibration. According to the input reference frequency, the digital calibration circuit calibrates the ILFD free running frequency by a binary search algorithm. In this way, the ILFD self-resonance frequency is aligned with the VCO output frequency in order to be locked by it. The digital calibration for the ILFD allows the PLL to work between 64.3 GHz and 66.2 GHz: that is, this is the frequency range in which the VCO tuning range is tracked by the ILFD. In this work, both VCO tuning range and ILFD locking range are poor if compared to the WirelessHD[TM] bandwidth, nevertheless, thanks to the calibration technique, the ILFD is locked by the VCO for ≈ 80% of the VCO tuning range.

A more detailed explanation of the calibration technique proposed in the 40 GHz PLL in 90 nm CMOS technology of [1] is now exposed. Such PLL has been designed to operate at 50 GHz for sliding-IF receivers. The digital calibration circuit is reported in Figure 41 (left). The cross coupled LC-VCO has both continuous and discrete tuning capability. The prescaler architecture consists of a divide-by-four ILFD, as the block that works at the higher frequencies in the PLL, and then, once that the frequency operation has been relaxed, a series of two divide-by-2 CMLs. The ILFD is based on a 2-stage ring oscillator, Figure 41 (right), and consumes 10 mW; two PMOS devices are implemented as resistors controlled by V_{ilfd} to adjust ILFD self-resonance frequency.
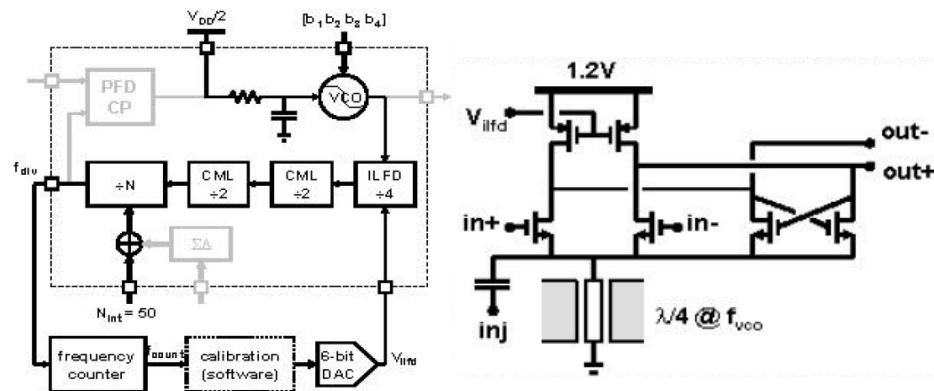
Figure 41: Calibration circuit of PLL [1] (left). Divide-by-4 ILFD schematic (right)

The VCO signal is injected into the divide-by-four ILFD, allowing the ILFD to be locked on the 4th harmonic of its output. In order to increase the ILFD locking range, the current source is replaced by λ/4 co-planar waveguide (CPW) at f_{VCO}. Nevertheless, the ILFD locking-range is limited to 1 GHz, not enough to covering the VCO range frequencies, especially if PVT variations are

considered. To ameliorate it, the calibration algorithm is run: the integer division ratio is set to 50 and the VCO control voltage is kept at $V_{DD}/2$. For each VCO frequency band, they are five bands, the control voltage V_{ilfd} of the ILFD is swept using a 6-bit DC DAC. When the ILFD is not locked, the control voltage V_{ilfd} directly changes the ILFD self-resonance frequency measured by the Frequency Counter (FC) after the divider chain, that is f_{count}. The frequency f_{div} is measured by the FC with 0.1 MHz resolution. On the other hand, when the ILFD is locked, its output becomes $f_{VCO}/4$ and f_{count}, that is the FC output, is no longer affected by V_{ilfd}. In order to centre the ILFD locking range around the VCO frequency, the steps are:

1) Searching algorithmically the V_{ilfd} range where df_{count}/dV_{ilfd} is below a given threshold.

2) Selecting the centre of this range as final V_{ilfd}.

If the VCO is turned off, the ILFD never locks and its self-resonance frequency always tracks the control voltage V_{ilfd}. Figure 42 shows the plots performed by the calibration algorithm for the lowest and highest VCO frequency band.
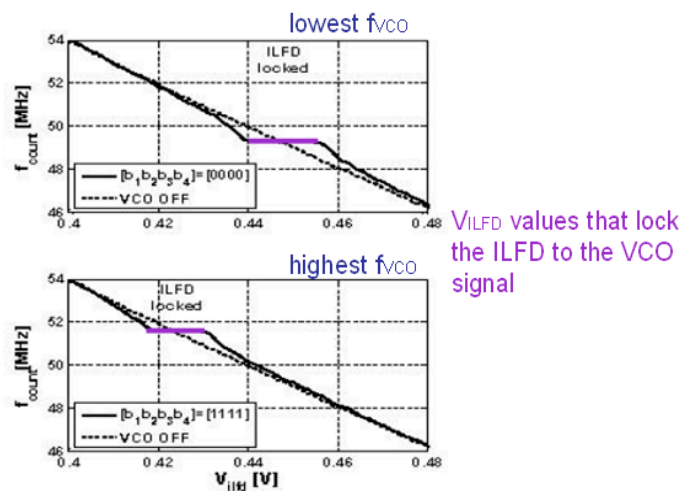
Figure 42: Calibration algorithm plot

Summarizing what has been reported in this section, it is possible to note that a FD working at 60 GHz for direct conversion transceiver frequency synthesizers, for applications in mm-W band, still has not been achieved. For the existing FDs either the operating frequency is down 60 GHz or the locking range is not wide enough. Furthermore, the impact of PVT variations in both VCO and FD simultaneously is still a critical point that has not be solved.

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4   60 GHZ LC-VCO DESIGN

In this section, the design of a wide tuning range, 60 GHz LC-VCO in 65 nm CMOS technology will be presented. Such VCO is suitable to be integrated in a 60 GHz frequency synthesizer for direct conversion WirelessHD[TM] transceiver.

The schematic of the proposed 60 GHz VCO is reported in Figure 43.
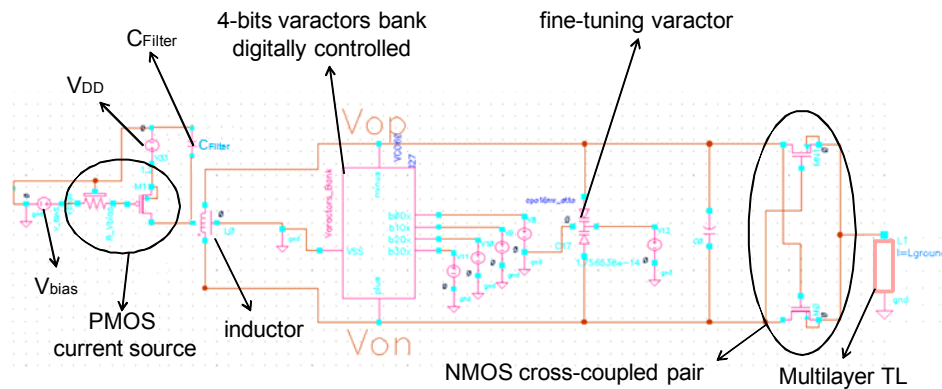
Figure 43: 60 GHz LC-VCO core schematic

Its active stage is composed by a cross-coupled NMOS transistors implemented in an isolated Pwell surrounded by deep Nwell implantation, to minimize substrate noise coupling. A single turn inductor is implemented to resonate out the VCO tank capacitance. It consists in sets of varactors binary scaled, which form the varactors bank, digitally controlled by 4-bits, plus a fine tuning varactor. The varactors forming the varactors bank are constituted of multiples of a unit varactor and grouped in four sets of 1, 2, 4 and 8 unit varactors. So that the VCO frequency can be continuous tuning over sixteen different frequency curves, by changing the overall capacitance of the varactors bank.

The current source is implemented with a PMOS transistor connected to V_{DD} through its source terminal. A capacitor C_{Filter} and a multilayer transmission line provide frequency filtering for noise optimization. In the proposed VCO, the DC value of the VCO outputs is set approximately to $V_{DD}/2$, in order to maximize

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the range of variation of the varactors capacitance, as it will be described. Furthermore, the PMOS current source ensures reliability by lowering the voltage peak in the NMOSs drain, if compared to the VCO topology in which the current source is implemented with an NMOS. Moreover, PMOS transistors add less flicker noise [1], so that the VCO phase noise can be improved.

The 60 GHz LC-VCO presents both discrete and continuous tuning capabilities. Its output frequency can be tuned by an analog input, i.e. by changing the capacitance of the fine tuning differential varactor; moreover, a control bus allows coarse tuning for PVT calibration, by changing the capacitance of the 4-bit digitally controlled varactors bank.

The VCO design is presented at circuit level. Some passive structures (inductor, layout interconnections and transmission lines) are used. The models for such structures are derived and obtained as results of EM simulations, as described in Chapter 6. The work reported in this chapter demonstrates that very large tuning ranges (> 20%) can be achieved at mm-W frequencies in 65nm CMOS processes using a LC tank VCO with differential accumulation type of varactors and a combination of continuous tuning and digital switching of varactors sets.

4.1   Motivation and Objective

As already mentioned, the first and greatest objective of this Thesis is the design of a CMOS FD for WirelessHD[TM] direct conversion transceiver, that is, 60 GHz operation frequency. However , at such frequencies, it is not very recommended to design separately all the blocks since some of the performance depends on the interconnection between two consecutive blocks inside a PLL, addressing the "distribution" critical issue in 60 GHz CMOS frequency synthesizers design, previously mentioned.

In the case of the FD, the preceding block is the VCO and some of the FD characteristics (e.g. the locking range) depends on the input signal amplitude, i.e. the VCO output. Furthermore, if PVT variations are taken into account, both blocks must be analysed jointly since the division range of the FD must be aligned with the oscillation range of the VCO under all possible PVT scenarios.

The VCO should not be considered only as the PLL block in charge of the frequency generation, but also as the input stage of the FD, specially for mm-W circuits.

The starting point of the 60 GHz LC-VCO designed in this Thesis is the circuit presented in [1], which was designed in the same research group and it

uses the same topology. Nevertheless, some significant changes have been introduced. The VCO in [1] was implemented in a 65 nm RF CMOS process, but with six metal layers. In order to get a VCO-FD co-design (and co-layout) the VCO needs to be designed with the same process utilized to fabricate the FD, that is the same 65 nm RF CMOS process of [1] but with seven metal layers. Furthermore, one of the main lessons learnt after the experimental characterization done in [1], the VCO gain should be decreased, in order to get reliable and stable phase noise measurements. To achieve it, the continuous tuning varactor size needs to be sensitively reduced and the digital control bus should be brought from 3-bit to 4-bit. As a consequence, the size of the unit varactor of the varactors bank should be reduced, in order to ensure 60 GHz as center frequency, while keeping an inductor value similar to that in [1]. The inductor has been also moved from a 6 metal layers to a 7 metal layers process. All these changes have required a new full design and layout of the VCO core. Further improvements and changes have been introduced in the output buffers stage in order to connect efficiently the VCO to the FD and to facilitate the FD and VCO experimental characterization, as will be presented later in the Thesis report.

4.2   Circuit Level Analysis of the Inductor

The VCO design process starts with the inductor selection.

Some functions and simulation test benches have been built in order to evaluate quality factors and inductance values, taking into account the unavailability of an Inductor Selection Tool in the design kit. They are used to select the best inductor option from the set available inside the design kit from the process manufacturer. For such inductors, lumped models are available that can be simulated in both time domain (e.g. SpectreRF from Cadence [2]) and frequency domain simulators (e.g. ADS [3] or GoldenGate [4] from Agilent).

The inductor of the VCO tank used in this Thesis is a single turn differential inductor made with the three upper copper metal layers (M7, M6 and M5) plus the aluminum metallization layer (ALUCAP). It has a patterned grounded shield.

Since the circuit level models of the inductors available in the design kit were qualified only up to 40GHz, the inductor has been also simulated using Agilent Momentum [5], in RF mode, in order to achieve a better accuracy of the VCO and FD simulations at 60GHz. The results of such simulations will be presented in Chapter 6.

Figure 44 (left) shows the schematic of the simulation test bench used for the inductor analysis:
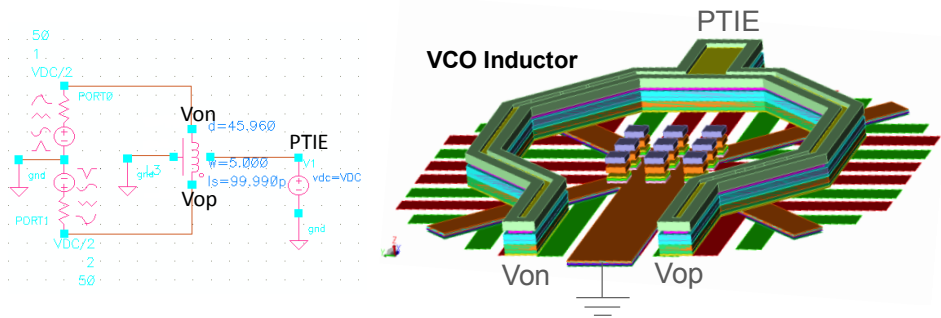
Figure 44: Schematic circuit for Inductor analysis (left). Inductor 3D layout view (right)

The port components are used also to provide the DC bias points at nodes V_{on}, V_{op} and PTIE. The default value of V_{DC} is set to 0.9V at this point of the design flow. This was considered a reasonable value. Later, when the fine tuning varactor will be sized, an analysis will be done in order to determine the optimum value of V_{DC} that maximizes the varactor capacitance change.

From the S-parameters analysis, the inductance and quality factor at 60 GHz of the selected inductor are ≈ 97.55 pH and 19, respectively, while the inductance value at DC is ≈ 95 pH, as shown in Figure 45. These values have been obtained for conductor width of 5 µm and inductor diameter of 45.96 µm. Larger inductor values (in terms of diameter and length) implies lower self-resonance frequency, so a good trade-off between self-resonance frequency and quality factor is obtained for the selected inductor.
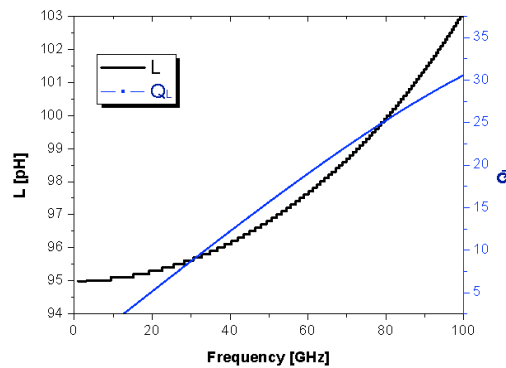
Figure 45: Inductor quality factor (Q) and inductance

The traces shown in Figure 45 have been obtained from the S-parameters analysis of the circuit of Figure 44 (left), performing a [S] to [Y] matrix transformation. Then, under the assumption that the differential inductor

is modelled as a floating impedance between the 2-ports of the π-network [6], its complex series impedance is calculated using the following expression is:

$$R+jX=\frac{Y_{11}+Y_{22}+2Y_{12}}{Y_{11}Y_{22}-Y_{12}^2} \quad (7)$$

Finally the inductance and quality factor of the selected inductor are found using:

$$L = \frac{Im\{R+jX\}}{2\pi f} \quad (8)$$

$$Q = \frac{Im\{R+jX\}}{Re\{R+jX\}} \quad (9)$$

4.3 Varactors Design

As previously said, one of the objectives of the 60 GHz VCO design was to reduce de VCO gain achieved in [1]. In order to do it, the fine tuning varactor should be physically reduced, in order to reduce the varactor capacitance change and consequently the VCO frequency change associated to a continuous control voltage sweep. Additionally, to compensate for the reduction of the overall tank capacitance, the capacitance associated to the varactors bank should be increased by the same amount to ensure basically the same VCO center frequency, under the assumption that the inductance has not change sensitively.

The varactors are implemented using a thick gate oxide available in the process, providing a capacitance ratio $C_{max}/C_{min} \approx 3$ for control voltage (V_C) sweep between 0 and 1.8V. The generic cell cpo18nw_atto, 1 column by 1 row (1x1), available in the process, is a N$^+$poly/Nwell varactor. Larger capacitance values can be obtained through an array of n×m unit cells using a waffle structure to distribute the common signals (i.e. substrate biasing and V_C). The N$^+$poly gates are connected to the nodes V_{on} and V_{op}, as shown in Figure 46.
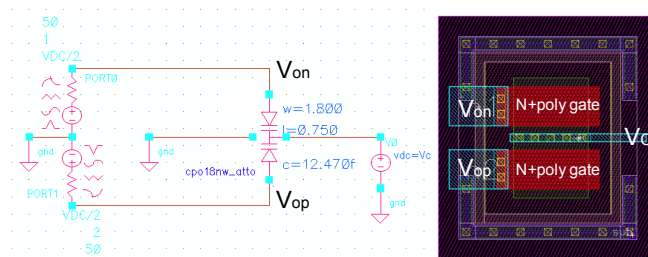
Figure 46: cp018nw_atto (1x1) varactor available in the kit

Just to summarize, in the VCO presented in [1] the following varactors were used:

➢ Fine Tuning Varactor (FTV):

  – 5x5 cpo18nw_atto, W=1.10 μm, L=0.28 μm

  – C_{max} = 32 fF (V_C = 0V); C_{min} = 10 fF (V_C = 1.8V), see Figure 48

➢ Varactors bank digitally controlled for coarse tuning:

  – binary scaled set of varactors (one, two and four units cell)

  – 3-bits [b0, b1, b2]; b0 is controlling the one unit cell, b1 the two units cell and b2 the four units cell

  – Unit Varactor Cell (UVC):

    o 1x1 cpo18nw_atto, W=2 μm, L=0.235 μm

    o C_{max} = 1.98 fF (b_n = 0); C_{min} = 0.54 fF (b_n = 1)

In Figure 47 it is shown a view of the varactors bank allocation for a better understanding.
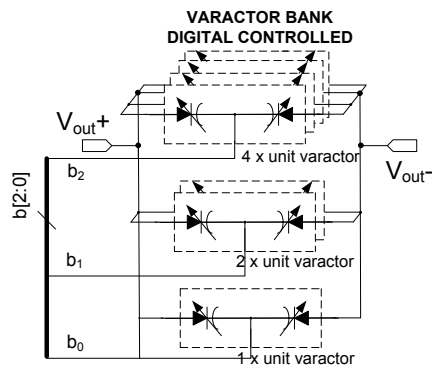
Figure 47: 3-bit varactors bank binary scaled

Therefore, the total capacitance associated to the 3-bit varactors bank in [1] approximately vary from 14 fF, corresponding to b[2:0] = 000, to 4 fF in the case of b[2:0] = 111. This digital controlled capacitance change provides the VCO with coarse tuning, extending its tuning range to cover the WirelessHD^TM taking into account an additional margin for PVT calibration. The changes with respect to [1] introduced in the VCO varactors designed in this Theses are detailed in the next sub-sections.

4.3.1 Fine Tuning Varactor (FTV)

The VCO output frequency is:

$$f_{out} = f_0 + K_{VCO}.V_C \qquad (10)$$

where f_0 is the VCO self-oscillation frequency, which changes being controlled by the digital code b[2:0]. K_{VCO} is the VCO gain, and from (10):

$$K_{VCO} = \frac{\partial}{\partial V_C}\left(f_{out}\right) = \frac{\partial}{\partial V_C}\left(\frac{1}{2\pi\sqrt{LC}}\right) \qquad (11)$$

L and C are, respectively, the tank inductance and the overall tank capacitance. In (11), once that the b[2:0] is set, C is completely dependent on V_C value, consequently K_{VCO} is determined by the FTV capacitance change with V_C.

In order to reduce K_{VCO}, the FTV should be reduced from the value used in [1]. The proposed re-size for the FTV is:

- 4x4 cpo18nw_atto, W=0.46 µm, L=0.28 µm

- C_{max} = 9 fF (V_C = 0V); C_{min} = 2.7 fF (V_C = 1.8V), Figure 48, Figure 50

In Figure 48 the comparison between the FTV capacitances is shown as the results of S-parameters simulation in SpectreRF of the circuit shown in Figure 46 at 60 GHz and by applying to the results some post-simulation functions (these functions are detailed in Appendix A).
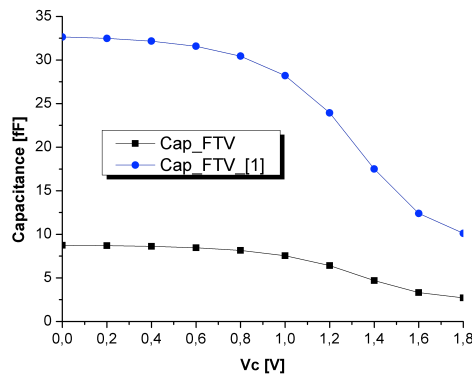
Figure 48: FTV capacitance comparison

The main change with respect to the varactor of [1] is that the N[+]poly/Nwell gate width of the cpo18nw_atto varactor unit cell has been

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reduced, while keeping the same length. The waffle structure was also reduced, decreasing the n×m array. In Figure 49 a comparison between the FTVs capacitance changes is shown, at 60 GHz:
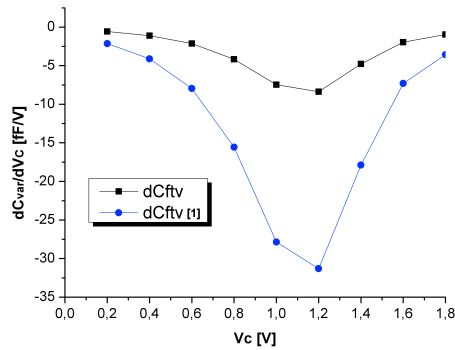
Figure 49: FTV capacitance variation

The FTV capacitance change with V_C has been reduced approximately from 30 fV/V down to 10 fF/V. Therefore, we expect to find the same reduction by factor ≈ 1/3 in K_{VCO}.

In Figure 50 it is shown the quality factor for the VCO FTV designed in this Thesis at 60 GHz, as a function of V_C.
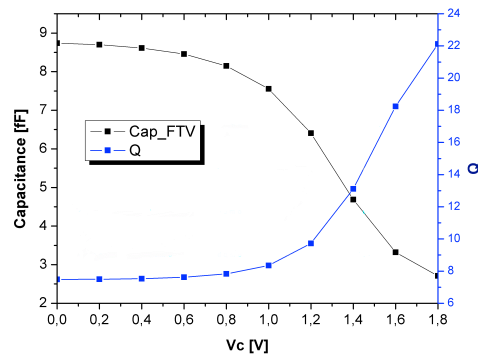
Figure 50: FTV capacitance and quality factor

As it is possible to see from Figure 49 and Figure 50, the maximum slope of the capacitance versus voltage characteristic is not found at V_C = 0.9V, i.e. the half point between 0 and 1.8V. This because, as previously mentioned, the starting value for V_{DC} was set to 0.9V. For this bias condition, the optimum biasing point for the varactor is found around V_C = 1.2V. Since the VCO tuning

characteristic should be centred at V_C = 0.9V, for maximizing the tuning range, the V_{DC} value should be changed to 0.75V, as Figure 51 depicts:
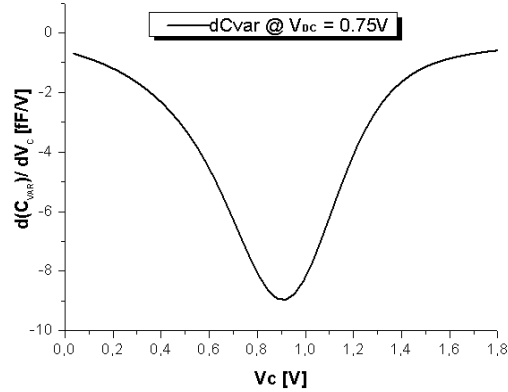
Figure 51: FTV capacitance variation @ V_{DC}=0.75V

As a summary of the previous analysis, it has been found that the optimum DC value in order to centre the VCO tuning characteristic at V_C = 0.9V is V_{DC} = 0.75V. This is the optimum VCO DC operation point regarding the FTV and it should be taken into account when designing and sizing the VCO bias circuit and the VCO cross-coupled transistors.

4.3.2   Varactors Bank for Coarse Tuning

The VCO tuning range can be extended by adding switched (ON/OFF) capacitors to the tank. Usually, the most standard solution is with a transistor-based design. The main drawback of this approach is that the NMOS transistors used in the switches contribute significantly to the phase noise of the oscillator. The topology proposed uses a differential varactor without switches to implement the switched capacitor. The VC signal of such varactor is directly connected to a digital signal that switches the varactor ON or OFF by applying 0 V or 1.8 V to the gate of a N+poly/Nwell differential varactor.

In order to compensate the reduction of the FTV capacitance, the varactors bank should provide the VCO tank with more ON/OFF capacitances if compared to [1]. The design strategy selected to design the 60 GHz VCO in this Thesis consists on adding one bit to the control bus, i.e. adding a set of eight cpo18nw_atto unit varactor to the varactor bank of Figure 47. The UVC will be also slightly re-sized, by reducing the N+poly gate width for a better layout integration of the digitally controlled 4-bit varactor bank. The proposed size for the UVC is:

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- 1x1 cpo18nw_atto, W=1.4 µm, L=0.4 µm

- C_{max} = 2.6 fF (b_0 = 0V); C_{min} = 0.6 fF (b_0 = 1.8V), see Figure 52
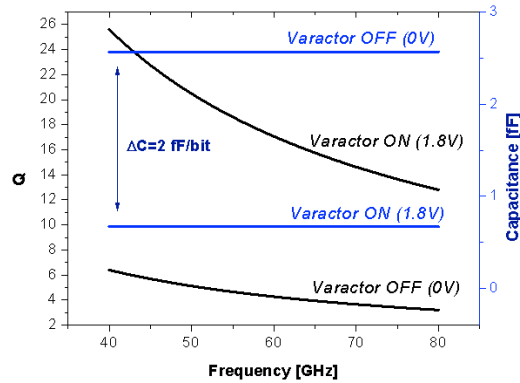
Figure 52: Simulated UVC capacitance and quality factor

In the following, it is assumed that a binary control bit '0' corresponds to 0 V while a '1' corresponds to 1.8 V. A '0' means that this varactor is OFF providing the larger capacitance value, whereas a '1' means that the varactor is ON, providing the lower capacitance. Note also that the varactors bank is binary weighted so that the Least Significant Bit (LSB) of the 4-bit code just turns ON or OFF a single (2^0) UVC, the next bit turns ON or OFF the set composed by two (2^1) UVCs; the next does the same for the set composed by four (2^2) UVCs and the Most Significant Bit (MSB) turns ON or OFF the set composed by eight (2^3) UVCs.

The unloaded capacitance provided by the accumulation of the FTV and the coarse tuning varactors bank corresponding to the coarse tuning code b[3:0]=0000 with V_C = 0V, i.e. C_{Tmax}, is approximately 48 fF. This value is contributed by 9 fF from the FTV and by 15x2.6 fF = 39 fF from the fifteen varactors of the bank in OFF state. Similarly, the unloaded capacitance corresponding to b[3:0]=1111 with V_C = 1.8V, i.e. C_{Tmin}, is approximately 11.7 fF, i. e. 2.7 fF of the FTV plus the contribution of the fifteen varactors of the bank in ON state, that is 15x0.6 fF = 9 fF. The values of C_{Tmax} and C_{Tmin} achieved with the 4-bits code are very close to the same values obtained in [1] with a 3-bits code and a different varactors arrangement. Nevertheless, we expect some improvement in the 17% of tuning range reported in [1], since C_{Tmax} > C_{Tmax}[1] and C_{Tmin} < C_{Tmin}[1]

4.4   Unloaded Tank Analysis

Next Figure 53 shows the schematic test bench used for the VCO unloaded tank analysis. It contains the inductor and the various varactors presented in the previous sub sections An ideal fixed capacitance C_F placed in parallel with the tank should be added to the schematic, to anticipate in this early design stage, the loading impact of the cross coupled transistors, output buffers and layout interconnections. As the design progresses, this ideal capacitor will see decrease its value since the capacitive effects of devices and EM models will replace it in the VCO design at schematic level, progressively.
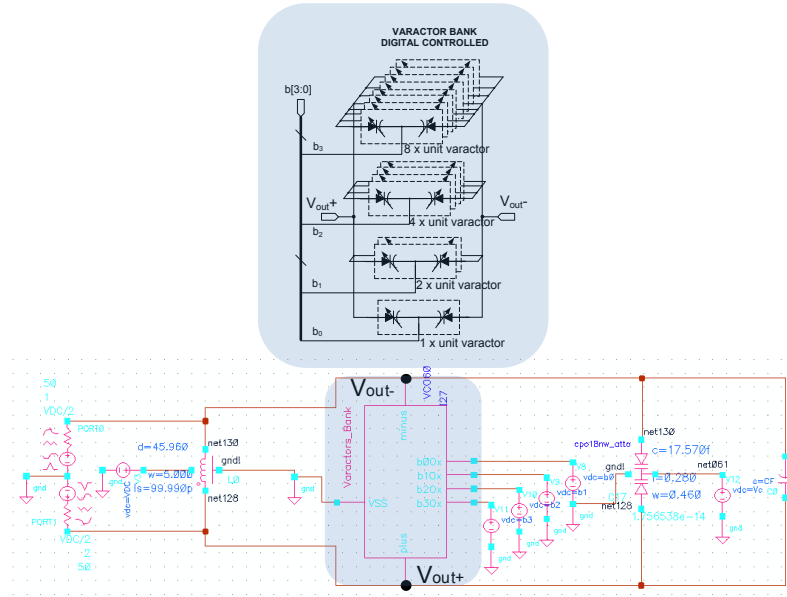
Figure 53: Schematic circuit for VCO tank S-parameters simulation

The maximum and minimum tank resonance frequencies, f_{max} and f_{min} respectively, of the circuit of Figure 53 can be expressed as:

$$f_{max} = \frac{1}{2\pi\sqrt{L(C_{T,min} + C_F)}} \tag{12}$$

$$f_{min} = \frac{1}{2\pi\sqrt{L(C_{T,max} + C_F)}} \tag{13}$$

where L is the tank inductance, which is plotted in Figure 45, while C_{Tmax} and C_{Tmin} as previously said are the previously defined maximum and minimum varactors capacitance, respectively. From the result of the last sub-section,

C_{Tmax}, corresponding to b[3:0]=0000 with V_C= 0V, is 48 fF and C_{Tmin}, corresponding to b[3:0]=1111 with V_C= 1.8V, is 11.7 fF.

The value of C_F is very critical: at mm-W frequencies its underestimation has a tremendous impact in the VCO, since the VCO operation frequencies will be shifted down in the spectrum. That is, the VCO f_{max} could become lower than the maximum frequency of interest, avoiding to properly covering the band. This problem is aggravated if PVT variations are taken into account. If the final f_{max}, after the design is completed, is lower than required, the only solution is a complete re-design of the VCO core, implying even a change of the inductor. On the other hand, a C_F overestimation has a lower but ever critical impact, since in order to increase f_{min}, for achieving the desired low end of the band, fixed Metal-Over-Metal (MOM) or Metal-Insulator-Metal (MIM) capacitances or metal stack capacitors should be added in the layout, increasing the VCO load and consequently lowering its tuning range.

Figure 54 shows the sixteen tank resonance frequency curves from the S-parameters simulation of the test bench of Figure 53, achieved for a of C_F = 40 fF. f_{max} is around 68.5 GHz and f_{min} = 54.2 GHz. This tuning range seems reasonable to cover the WirelessHD[TM] band even in presence of PVT variations, since it is verified that [7]:

$$\Delta C_T = \left(C_{T,max} - C_{T,min} \right) \geq \frac{4 \cdot \left(f_{max} - f_{min} \right)}{L\pi^2 \left(f_{max} + f_{min} \right)^3} \qquad (14)$$
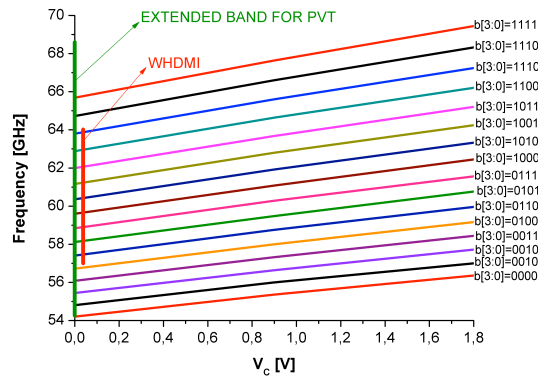
Figure 54: Tank resonance frequency curves

The tuning range shown in Figure 54 marked with a green bar superimposed onto the vertical axis, is a good approximation of the VCO tuning range, which will be obtained in the next pages performing a most accurate

large-signal Periodic Steady-State (PSS) simulation of the VCO. Note that the results of Figure 54 are obtained from a [S] parameter analysis, where non-linear effects are ignored. Such non-linear effects may affect significantly the tuning range specially for medium and large tank oscillation amplitudes, since the assumed DC bias voltage of the varactors (V_{DC} = 0.75V) is no longer a constant but a time varying signal centred around this V_{DC} value, so that the varactors capacitance varies with time along the oscillation cycle even if V_C and the coarse control binary code are kept constant.

In order to investigate the impact of the loading effects of the rest of VCO components and the parasitics in the tank, the impact of a C_F = 40 ± 10 fF in the tank resonance maximum and minimum frequencies is shown in Figure 55. As it is possible to note, red squared markers, corresponding to f_{min} for C_F = 30 fF and f_{max} for C_F = 50 fF, result in tank resonance frequencies not fulfilling the specifications at each of the extremes of the tuning range, respectively.
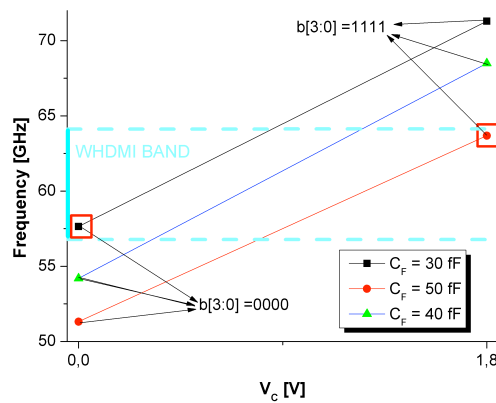
Figure 55: C_F impact on tuning range

The tank resonance frequencies have been calculated as the frequency values which maximize the real part of the inverse of the tank differential admittance Y_D of the tank,), i.e. the parallel equivalent resistance , R_{peq}, of the tank (see Appendix A). These curves are reported in Figure 56 for C_F = 40 fF, which is the selected value of C_F, that is our capacitance budget during the following design steps:
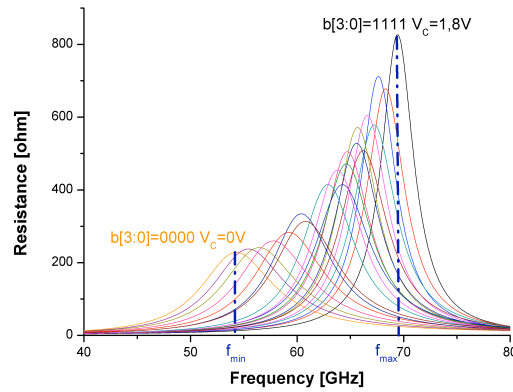
Figure 56: Real{1/Y$_D$} curves

The VCO cross-coupled transistor size is dictated by the transconductance g_m necessary to compensate the losses of the tank, hence ensuring start-up oscillation, according to:

$$g_m \geq \frac{2}{R_{p,eq}}$$

(15)

The values of R_{peq} used in (15) are the maximum values of the curves in Figure 56, that is the parallel resistance at tank resonance frequency. The worst case for start-up oscillation corresponds to the minimum control voltages of the varactors, i. e. b[3:0]=0000 with V_C= 0V, that set the minimum oscillation frequency f_{min}. For this point of the tuning curves the parallel losses of the tank are slightly over Rp,eq = 200 ohms.

Next step is to calculate the unloaded tank quality factor, Q_T, as the ratio between the resonance frequency f_0 of the curves of Figure 56 and its 3 dB bandwidth, that is:

$$Q_T = \frac{f_0}{BW_{3dB}}$$

(16)

The unloaded quality shown in Figure 57 factor varies from 9, corresponding to the lowest resonance frequency, up to 19, corresponding to the highest one. Now all the data required for the sizing of the rest of components of the VCO are available, that are, VCO DC operation point and minimum R_{peq}. This design step is described in the next sub-section.

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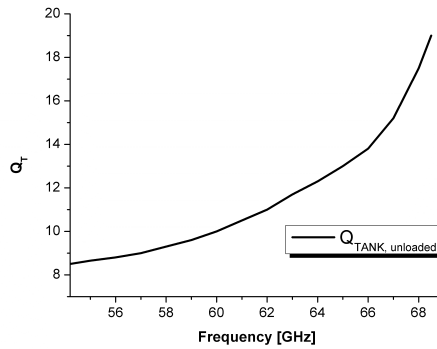
Figure 57: Unloaded tank quality factor

4.5   Transistor Sizing and VCO PSS Simulation

Minimum transistors size, as already mentioned, is dictated by (15). It is mandatory to size the transistor in order that its transconductance g_m compensates the tank losses, allowing start-up and oscillation.

4.5.1   DC Analysis and Loaded Tank Simulation

Figure 58 shows the test bench circuit used for the DC simulation of the MOSFET transistors, including a low-V_t RF NMOS transistor in diode connection:
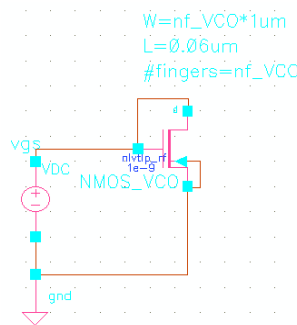
Figure 58: Schematic circuit for NMOS DC simulation

From (15), the minimum g_m required, corresponding to the lowest R_{peq} value, is found to be 10 mS. Since additional losses and start-up condition requires to leave some design margin, a g_m = 20 mS is selected as the design goal for the cross-coupled pair of the VCO.

In Figure 59, relevant NMOS parameters are reported for a V_{GS} voltage sweep from 0 up to 1.2V. These results refer to different transistor widths W, while transistor length is kept constant to its minimal value of 60 nm. W variation is achieved with a different number of transistor fingers. The finger width is 1 µm.
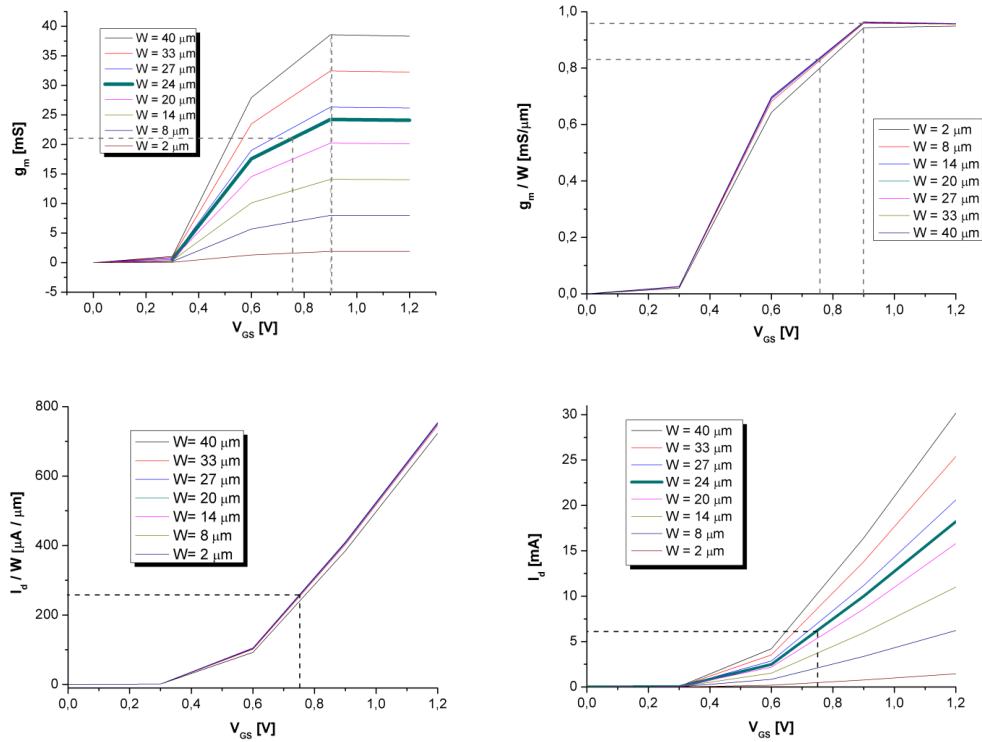
Figure 59: NMOS DC simulation. g_m (upper-left); g_m/W (upper-right); I_d (lower-right); I_d/W (lower-left)

The optimal value of V_{GS}, from the point of view of transistor transconductance, is found around 0.9V, since increasing the V_{GS} beyond 0.9V does not improve significantly the g_m, independently on W . Nevertheless, from the result of Figure 51, the optimum DC voltage for tuning range was found around 0.75V. This bias voltage restricts the current biasing of the NMOS, independently of its size, to ≈ 280 µA/µm.

The required g_m is achieved with a number of fingers of 24 for a V_{GS} = 0.76V. Therefore, the total transistor width will be set to 24 µm. The biasing current consumption is set univocally per each NMOS of the cross-coupled pair, to 6.2 mA, consequently it results in 12.4 mA for the VCO core.

Figure 60 shows the simulation test bench circuit used for S-parameters and DC simulations of the VCO loaded tank. It is based on the circuit of Figure

53, with the addition of the cross-coupled NMOSs. An ideal biasing current source, injecting 12.4 mA DC in the central tap of the differential inductor, is used and the ports for S-parameters simulation are connected to the tank using ideal 100 nF DC blocking capacitors. The voltage supply is 1.2V.
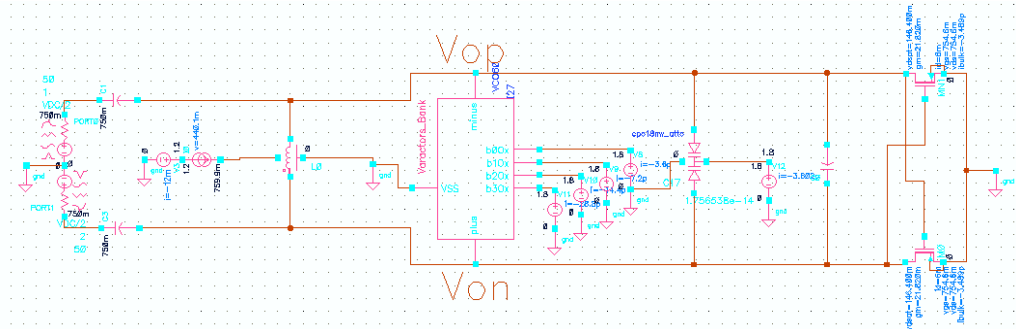
Figure 60: Loaded tank circuit for [S] and DC simulations

The DC voltage at nodes V_{op} and V_{on} found after the DC operating point simulation is 0.76V and g_m = 21.8 mS.

The parasitic capacitance of the NMOSs cross-coupled pair drains and gates lower the tank resonance frequency if the fixed capacitance C_F is kept to 40 fF. An optimization loop is run in order to find the right C_F value that allows obtaining the same tuning range shown in Figure 54. In Figure 61 the tank resonance frequencies and now loaded quality factors are reported as a function of V_C, corresponding to b[3:0]=0000, b[3:0]=1000 and b[3:0]=1111, for a reduced C_F = 14 fF. It means that the parasitic capacitance added by the cross-coupled NMOS pair to the VCO tank amounts to 26 fF at 60 GHz.
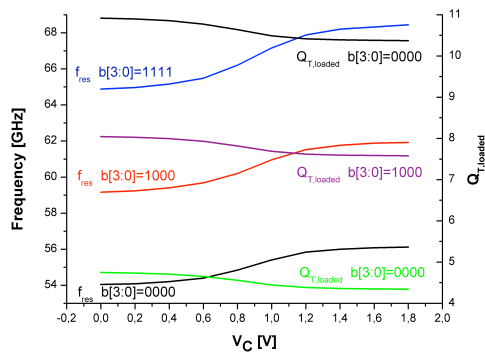
Figure 61: Resonance Frequency and quality factor of the loaded tank

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The total fixed capacitance remaining budget of 14 fF should account mostly for the output buffers input capacitance and the layout interconnections capacitance.

4.5.2   PSS Simulation with Ideal Current Source

Once that the tank has been analysed and sized, as well as the active stage (the cross-coupled transistors pair), the performance of the 60 GHz VCO is simulated using large signals PSS simulation. Phase Noise (PN) analysis at 1 MHz offset frequency from the carrier is also done in order to characterize the VCO PN. Figure 62 depicts the test bench circuit used for these simulations:
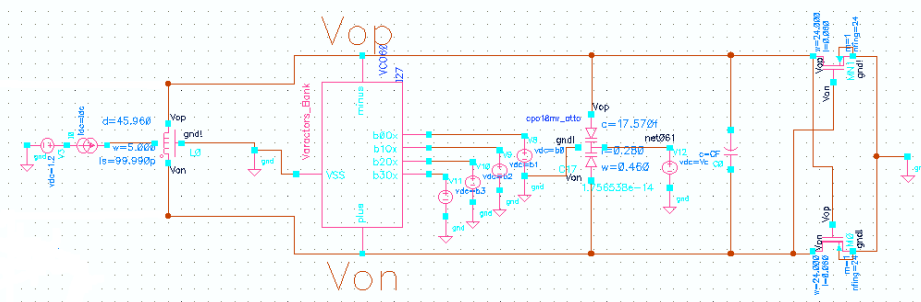
Figure 62: 60 GHz VCO schematic circuit for PSS and PN analysis: ideal current source

An ideal current bias source is still used to provide the VCO with DC operation point. The voltage supply is 1.2V. Next Figure 63 shows the overall VCO tuning range by plotting the output frequencies corresponding to the first harmonic of V_{op} (left side), as well as some V_{op} output frequency waveforms corresponding to digital control code b[3:0]=1111.
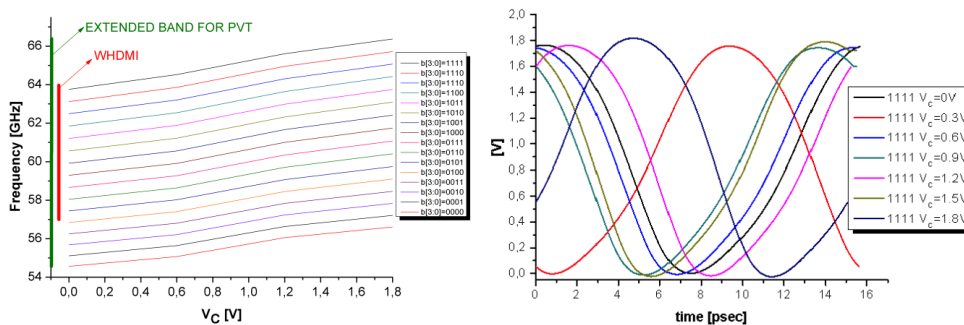
Figure 63: PSS simulation: VCO tuning range (left); VCO output curves for b[3:0]=1111 (right)

If Figure 63 (left) is compared to Figure 54, it is possible to note a reduction in the tuning range from 54.2 - 68.5 GHz to 54.3 - 66.5 GHz. Whereas the low frequency range is basically the same, the higher frequency range has been reduced by ≈ 2 GHz (corresponding to ≈ 3% of VCO tuning range reduction). This is consequence of the above mentioned limitation of the linear analysis that was used to obtain the results of Figure 54.

Nevertheless, the VCO tuning range shown in Figure 63 (left) is still appropriate to cover the WirelessHD[TM] band with a security margin for PVT variations compensation. The VCO tuning range is around 20%, which is almost the double of that required for the WirelessHD[TM] band coverage (11.5%). This extremely large tuning range achieved for an LC based VCO at 60 GHz is a consequence of the design approach in which the optimum VCO DC output voltage, i. e. the VCO DC operation point, from the varactors point of view, has been selected, maximizing the capacitance variation range.

In Figure 64 the VCO outputs voltage amplitude (single-ended) and the VCO PN values at 1 MHz frequency offset are shown.
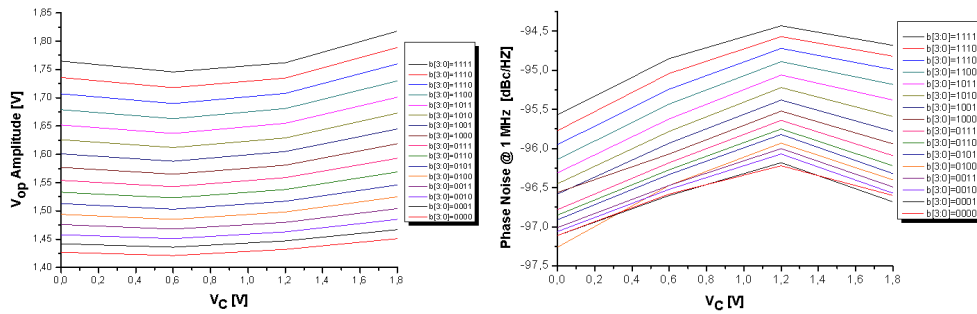
Figure 64: VCO output voltage (left); VCO PN @ 1 MHz frequency offset (right)

The VCO outputs voltage amplitude V_{op} in Figure 64 (left) are quite high. An extra-loop for optimization, reducing the peak levels, will be performed if such large VCO output causes the VCO output buffers to stay in deep compression.

4.5.3   Considerations About Tuning Range Maximization

There exists a trade-off between DC bias point/transistors size and PN/tuning range: for smaller transistors and lower biasing currents, the tuning range is increased (paying attention to ensure start-up oscillation with a security margin in g_m), since the overall VCO output load is reduced. But in this scenario the PN will becomes higher, due to the reduction of the VCO output voltage.

Figure 65 shows an example of an alternative VCO sizing where a smaller NMOS width and bias current are used, resulting in larger phase noise.
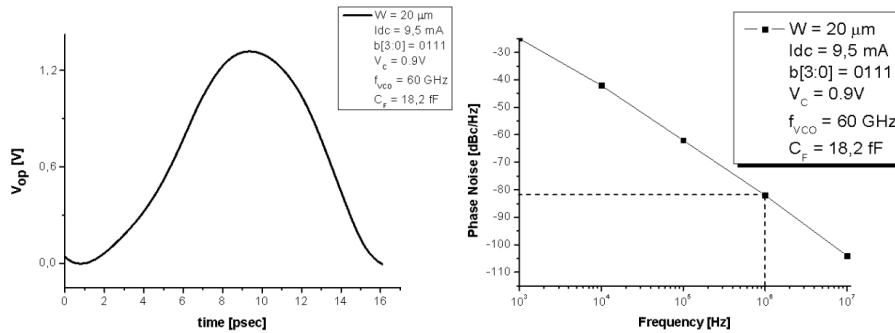
Figure 65: VCO output wave (left) and its phase noise (right) for reduced W

Otherwise, if both transistor size and biasing current are increased, the VCO tuning range is reduced (higher VCO load) but the PN is lower; another drawback of this approach is the reduced budget for the C_F, since the NMOS cross-coupled pair parasitics become more important for larger transistor widths.

On the other hand, if the varactors are made larger, in order to increase its capacitive variation range, the tuning range can be increased. However, this will reduce the tank quality factor as well as the C_F.

PN basically depends on the biasing current and, consequently, on the parallel resistance of the tank at its resonance frequency resonance for each tuning point. In fact, we have seen previously (Figure 56 and Figure 57) that this value increases as the quality factor increases. Hence, for lower quality factors, in order to compensate the reduction of parallel resistances at resonances, the DC biasing current could be increased. However, since the DC operation point should be kept constant (at the optimum value), a larger bias current requires enlarging the NMOS transistors, which has the already mentioned unwanted consequence of reducing the tuning range and the available budget for the capacitances provided by layout interconnections and output buffers. Last, but not least, another consequence will be the increase of power consumption.

If tuning range is considered a priority, it has been shown in the previous reasoning that for smaller size transistors, the tuning range is maximized, even more if the VCO DC operation point is at its optimum value for the varactors biasing. On the contrary, it has been shown the PN is penalized. An aggressive approach in order to improve the PN could be increasing the current consumption, consequently the VCO power consumption, without increasing the NMOS width. This is a not good strategy, since even if the PN

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can be improved, the tuning range will be dramatically reduced since the VCO DC operation point will be far from the optimum value set by the varactor capacitance change.

As a summary, there exist several challenges in achieving high-Q, Low-PN, high-tuning range and low power consumption VCO simultaneously: the VCO sizing shown in this Thesis results in a circuit that presents a good trade off among them.

4.6 VCO Core Simulations including a PMOS Current Source

The bias source of the designed VCO is implemented using a PMOS transistor of 200 μm of width, that is with 200 fingers, where each finger has 1 μm width. The PMOS channel length is 140 nm since this is not an high-frequency device. Short channel effects and matching are improved for longer transistor length. Figure 66 shows the test bench circuit used for the 60 GHz VCO simulations reported in this sub-section.
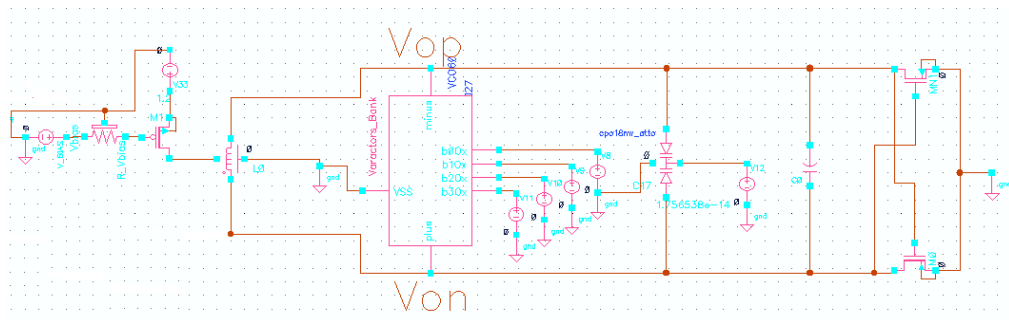
Figure 66: 60 GHz VCO with PMOS current source

A 18.5 KΩ resistance, implemented with three parallel high resistive Poly resistors, for Electro-Static Discharge (ESD) damage prevention, connects the DC voltage bias source to the PMOS gate. The bias voltage V_{bias} is adjusted to obtain the required bias current I_{dc} = 12.4 mA. The plot of Figure 67 shows the $I_{DC, VCO}$ versus V_{bias} curve:
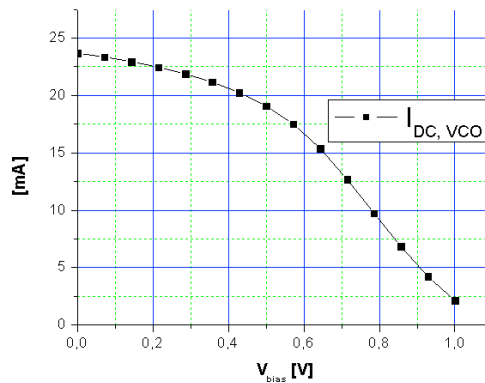
Figure 67: $I_{dc,VCO}$ vs V_{bias}

The required VCO DC current is found for a VCO bias voltage V_{bias} = 715 mV. For this bias, the PMOS transistor stays deeply in saturation state.

As a summary, the DC parameters of the VCO core are listed:

- VCO Power Consumption P_{dc} = 15.19 mW

- I_{dc} = 12.4 mA at V_{DD} =1.2V

- V_{bias} = 715 mV

- NMOS transconductance g_m = 22 mS

- VCO DC output voltage $V_{DC,out}$ = 0.761V

Now that the PMOS current source is sized, the further step is simulating the circuit of Figure 66 with large signal PSS analysis. The insertion of the PMOS transistor reduces slightly the maximum VCO operation frequency, if the last value of C_F, corresponding to the schematic of Figure 62, is kept to 14fF. This is compensated by reducing the value of C_F by 1.7 fF, in order to re-centre the VCO core tuning range. Therefore, the total fixed capacitance in the circuit of Figure 66 is C_F = 12.7 fF. Figure 68 and Figure 69 show the results corresponding to the PSS simulation of the tuning curves and PN analysis, as well as the output voltage waveforms for some tuning point .
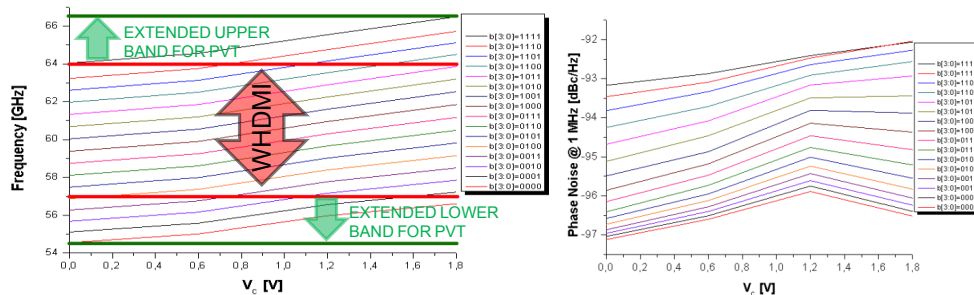
Figure 68: VCO core. Tuning range, V_{op} output frequency (left); PN @ 1 MHz frequency offset (right)
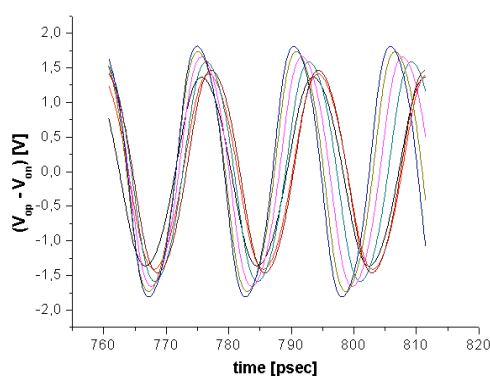
Figure 69: Differential output waveforms V_{op}-V_{on}

4.6.1 Phase Noise Optimization

A final optimization process is now performed in order to improve the VCO phase noise characteristic. A filter capacitance C_{Filter} is inserted between the drain and source terminals of the PMOS. This capacitor filters out some of the low-frequency noise components, specially flicker noise from the current bias transistor that may be up-converted impacting in the PN at the VCO outputs. This capacitance, that should have a large value, will be implemented in the layout with a set of source-drain shorted transistors in order to reduce the area occupation.

Additionally, an inductance L_{ground} is also inserted between the cross-coupled NMOS common sources and the ground plane. The bulk of the NMOS is also connected to this node, since the NMOSs will be realized in a isolated Pwell surrounded by deep Nwell implantation to minimize substrate noise coupling. At layout level, the inductor will be implemented with a multilayer Transmission Line (TL). The inductance is used to reduce the 2nd harmonic oscillation at the common source node, which is also a strong contribute of low

frequency flicker noise up-conversion to the oscillator fundamental harmonic. Both the capacitor and the inductor form a filter that, if correctly sized, can reduce the PN of the VCO [8].

The VCO core circuit test bench for noise optimization is reported in Figure 70:
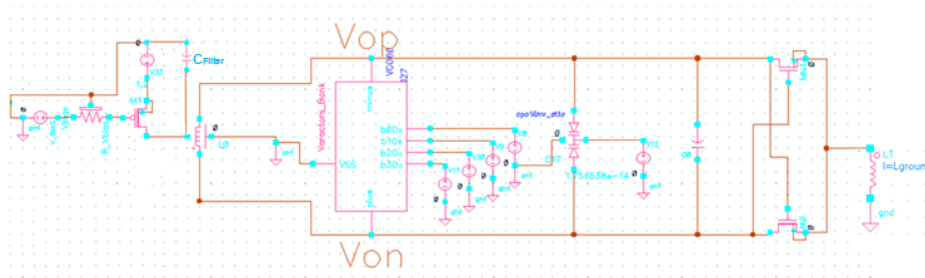
Figure 70: VCO core schematic

In this sub-section the optimum value for C_{Filter} and L_{ground} are found simulating the response of the VCO. At first, an optimal value for C_{Filter} is achieved with L_{ground} disconnected, by calculating the PN values at 1 MHz frequency offset corresponding to a C_{Filter} capacitance sweep. The results are shown in Figure 71:
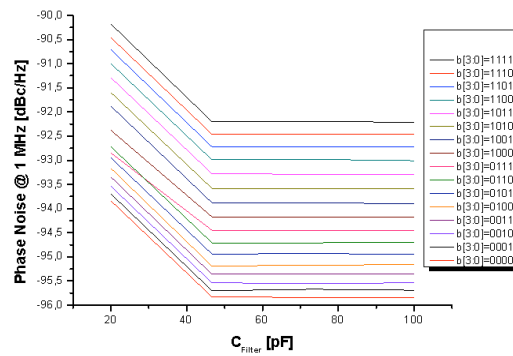
Figure 71: PN @ 1 MHz vs C_{Filter}; V_C = 0.9V

The curves reported in Figure 71 have been achieved calculating the PN, at 1 MHz frequency offset, associated to the VCO output voltage V_{op}, for different C_{Filter} values. The V_C is set to 0.9V, in order to evaluate C_{Filter} impact in noise performance at the centre of each VCO frequency curve. As it is possible to note, for C_{Filter} = 47.5 pF the PN improves for all the sixteen VCO centre frequencies around 4 dB compared to the initial values. Increasing C_{Filter} value above 47.5 fF does not change significantly the PN, so that the selected C_{Filter}

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value is set to 50 pF. Such capacitance will be implemented in the layout taking advantages of the surrounding areas around the differential inductor, as it will be exposed later.

The optimal value for L_{ground} is now selected making the same operation just exposed, but using L_{ground} as the sweep variable for a fixed value of C_{Filter} = 50 pF. The results are shown in Figure 72 (left).
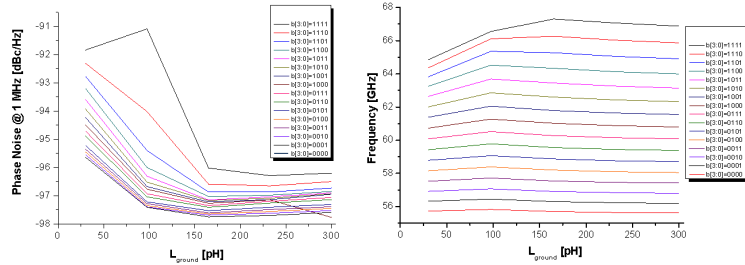
Figure 72: PN @ 1 MHz vs L_{ground}. V_C = 0.9V (left); VCO output frequency V_{op} vs L_{ground}. V_C = 0.9V (right)

The results of the previous analysis indicate that the for L_{ground} = 165 pH the PN, at 1 MHz frequency offset, is always below -96 dBc/Hz, while in the best case is very closed to -98 dBc/Hz. Hence, the selected optimal inductance for the TL which connects the NMOSs common source terminals to ground will be 165 pH. It will be taken into account when the VCO core will be placed in the layout and EM simulations will be run in order to accurately design the TL having the selected inductance.

The insertion of the $L_{ground}C_{Filter}$ filter makes the VCO output frequencies move slightly, as Figure 72 (right) depicts, causing that the lower VCO output frequency is now closer to the WirelessHD^{TM} minimum frequency. A final step is needed in order to fine tune the fixed capacitance value an re-centre again the VCO tuning curves. The final value for C_F before starting the layout is 14.4 fF. For this value, Figure 73 shows the VCO tuning range and PN.
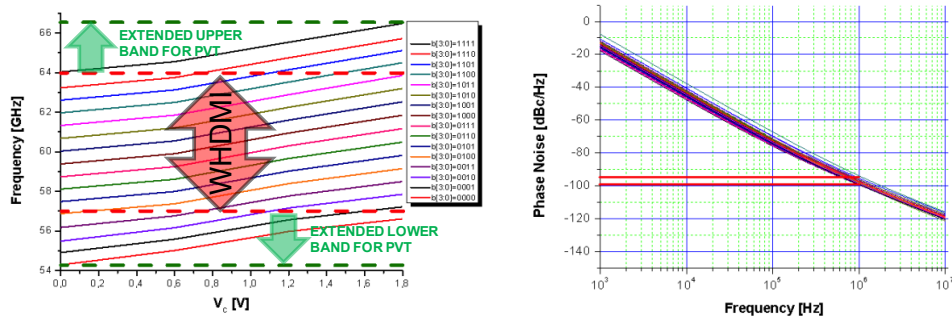
Figure 73: 60 GHz VCO core. Frequency curves (left); Phase Noise (right)

The VCO oscillation amplitude (differential output), varies between 1.7V and 1.8V. In Figure 74, some single-ended (V_{op} and V_{on}) and differential (V_{op} - V_{on}) output waveforms for several V_C values and b[3:0] =1111 are shown:
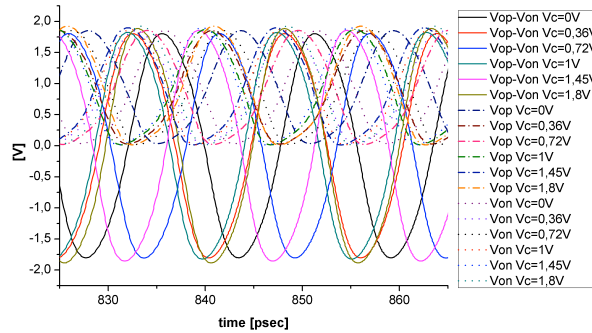
Figure 74: VCO Output waveforms for V_{op}, V_{on} and (V_{op} - V_{on}); b[3:0]=1111

The VCO core has a very wide tuning range of 20.4%, corresponding to a maximum frequency of 66.49 GHz, and a minimum frequency of 54.2 GHz, as reported in Figure 73 (left). The central frequency is 60.4 GHz. This wide tuning range allows to cover the overall WirelessHD[TM] with an additional margin for PVT compensation and to the author knowledge it is the VCO with widest tuning range for this kind of application in mm-W.

Finally, the VCO gain K_{VCO} curves are reported in Figure 75. As it is shown, the K_{VCO} maximum is achieved for each curve around V_C=0.9V, since the varactors are biased at their optimal DC value. Furthermore, the maximum value is K_{VCO} = 1.8 GHz/V and, as it was advanced in sub-section 4.3.1, its reduction if compared to [1] is by a factor ≈ 1/3.
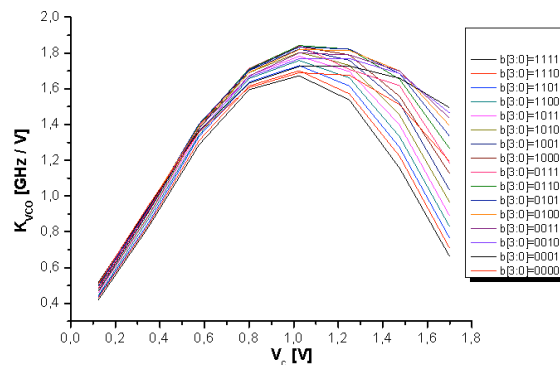
Figure 75: K_{VCO}

4.7   Conclusions

A 60 GHz cross-coupled LC-VCO core design in 65 nm CMOS technology has been presented at circuit level. The VCO presents both continuous tuning and coarse tuning for PVT variations compensation. The wide tuning range achieved is mostly due to the selection of the optimal DC voltage biasing the varactors. The current consumption is 12.4 mA from 1.2V voltage supply.

The results achieved in this chapter allows to consider the VCO core object of this Thesis as suitable to be integrated in a 60 GHz frequency synthesizer for direct conversion WirelessHD^{TM} transceiver.

In order to finish the VCO design at circuit level some parts are still missing like control lines for DC voltages distribution, DC-to-ground decoupling capacitors and output buffers. In order to design these parts, at least a preliminary view at floor plan level of the top circuit (i. e., the VCO and the FD) should be considered, so that the next step consists in designing the FD core at circuit level.

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5   60 GHZ LC-ILFD DESIGN

In this chapter, the design of a wide locking range, 60 GHz divide-by-two ILFD in 65nm CMOS technology is presented. Such ILFD is suitable to be integrated in a 60 GHz frequency synthesizer for direct conversion WirelessHD^{TM} transceiver.

Injection locking topology has been chosen as the optimum FD topology to be inserted in the control loop of mm-W PLL for direct-conversion transceiver, due to the extremely high speed requirements at these frequencies and the power consumption constraint. That is, since a down conversion from RF to baseband (and viceversa) must be achieved in a single step, the LO and consequently the FD operate at 60 GHz. From the state of art review presented in Chapter 3 it is clear that frequency divisions at such frequency suppose a evident limit for topologies other than the ILFD (flip-flop based, static, etc), taking into account that low power consumption is a must.

The divide-by-two ILFD, when no input signal is injected into it, is a not-locked ILO oscillating at its self-resonance frequency, which should be around $f_{in}/2$ to achieve frequency division by two with reasonably low input power level, where f_{in} is the input frequency to be divided, i. e. the frequency of the VCO output in the PLL. Therefore, the divide-by-two ILFD to be inserted in a 60 GHz PLL should self oscillates around 30 GHz. It is possible to consider the injection mechanism as the mixing of the injected signal at f_{in} with the ILO output signal at $f_{in}/2$. Such mixed signal, consisting of $f_{in}/2$ and $3f_{in}/2$ frequency components is filtered by the band pass filter constituted by the ILFD tank, in order to generate the ILFD output signal at $f_{in}/2$.

The ILFD presented in this work has discrete tuning capabilities, since its output frequency can be tuned by a three-bit digital control bus, i.e. by changing the capacitance of the binary weighted varactors bank, allowing coarse tuning for PVT calibration.

In this chapter the design of the ILFD is presented at schematic level, while regarding fixed and parameterized EM models for some of the passives (inductor, layout interconnection structures and transmission lines) they will be discussed in Chapter 6. This work reported in this chapter demonstrates that wide locking ranges (> 20%) can be achieved at mm-W frequencies in 65nm

CMOS processes using a LC tank ILO with differential accumulation type varactors and digital switching of varactor banks.

5.1   Motivation, Objective and Methodology

PVT variations has so much impact at mm-W in CMOS process that it is not clear if direct-conversion architectures are possible for WirelessHD[TM] applications, since the divider must operates at 60 GHz. The objective of this thesis is push on this direction, proposing an ILFD design at 60 GHz that is PVT variations robust.

A wide tuning range ILFD should be designed, in order to cover properly the WirelessHD[TM] band also in presence of PVT variations. Inside a PLL, they affect both VCO and ILFD, i. e. the PLL blocks working at 60 GHz operation frequency in zero-IF topology, so extra margin in band counting must be considered and the extended band should be taken into account from the beginning of the design.

Discrete tuning capability are implemented in the ILFD to compensate PVT variations, under the assumption that they impact in the same way on both VCO and ILFD, that is each PVT corner causes the same trend in VCO oscillation frequency and ILO self-resonance frequency. This assumption will be experimental verified (Chapter 7) and so it simplifies the calibration scheme to compensate PVT variations in the VCO-ILFD system.

At first, the simulation environment will be set in order to evaluate and analyze divider locking state, with the objective to build the ILFD input sensitivity curves, proposing a first ILFD design with continuous tuning. S-parameters simulations will be used to extract the proper numerical value for tank design and characterization, in the same way as the methodology exposed in the previous chapter.

The ILFD locking state is simulated by means of transient analysis: this is because SpectreRF is not so robust in frequency domain when applied to distributed models at mm-W frequencies, hence injection locking is difficult to simulate in the frequency domain. Steady-state simulations will be used to evaluate ILO self-resonance frequency. Furthermore, steady-state of the autonomous system will be simulated with GoldenGate [1] when no external source are employed at schematic level, for example to simulate locking conditions of the system VCO-ILFD (Chapter 7). Therefore, a combination of both frequency domain and time domain techniques will be employed.

In order to design a wide locking range, low power consumption ILFD, the impacts of various alternatives of low/high Q tank and injection scheme will

be experimental analysed. It since from (1) and (2), the ILFD locking range depends on the Q of the tank, but also on the injection efficiency. The unique way to maximize the injection ratio is investigating on the injection scheme that presents the lowest losses.

5.2   Continuous Tuning ILFD Design

In order to analyze the locking state, a first version of 60 GHz divide-by-two ILFD is designed. The schematic circuit is shown in Figure 76. It consists of a 30 GHz cross-coupled LC-ILO with a fine tuning varactor. This design will be also helpful to understand locking range possibility of future discrete tuning solutions, required for a practical implementation of the PVT calibrations.
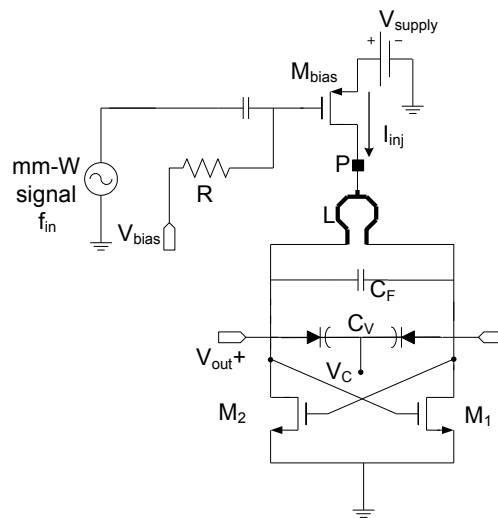
Figure 76: Continuous tuning 60 GHz divide-by-two ILFD schematic

The design starts from the inductor selection; then, a differential varactor is sized to cover the required bandwidth taking into account PVT variations. The locking state will be simulated in the time domain and the ILFD input sensitivity curves are consequently built, according to varactor control voltage V_C and input power and frequency provided by an external input source.

5.2.1   Circuit Level Analysis of the Inductor

The differential inductor used for this first ILFD design has the same characteristics of that one used for the VCO design. The test bench circuit utilized in this sub-section for inductor analysis is the same of Figure 44, except for the inductance value, while the simulation functions used to evaluate inductors parameters are the same used in section 4.2.

From the S-parameters analysis, the inductance and quality factor at 30.75 GHz, that corresponds to the centre frequency of the divided-by-two WirelessHD[TM] bandwidth, are 256 pH and 25, respectively, while the inductance value at DC is 243.5 pH, as shown in Figure 77. These values have been obtained for a single turn differential inductor of 10 μm width and diameter of 110 μm, implemented using a stack of M5, M6 and M7 metal layers and ALUCAP over a patterned ground shield.
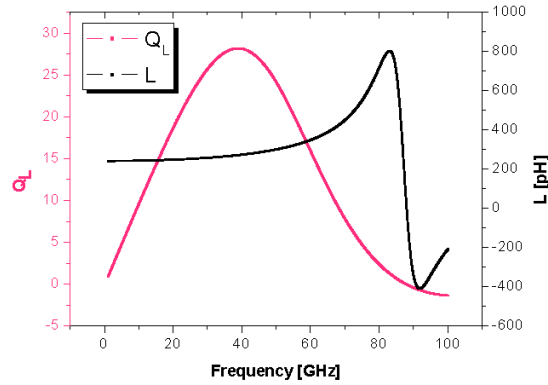
Figure 77: Inductor quality factor and inductance

It is possible to note that the inductor resonance frequency is around 90 GHz, far enough from the inductor operation frequency.

5.2.2   Fine-Tuning Varactor Sizing

In order to select and size the varactor of the ILO tank, a quickly calculus is required in order to determine the total amount of capacitance variation needed to design a tank resonating in the desired frequency range. The WirelessHD[TM] centre frequency is 60.5 GHz. It means that the divide-by-two ILFD centre self-resonance frequency f_C should be at 60.5/2 = 30.75 GHz. Besides the required centre tank resonance frequency, the extremes of the required injection range result in an output frequency range of f_{min} = 57/2 = 28.5 GHz and f_{max} = 64/2 = 32 GHz. An additional margin should be considered to take into account for PVT variations. Next table resume the band/capacitance counting:

	f_{min} [GHz] / C_{max} [fF]	f_C [GHz] /C_C [fF]	f_{max} [GHz] / C_{min} [fF]
WirelessHD[TM]	28.5 / 124	30.75 / 106	32 / 98.3
Extended-WirelessHD[TM] (PVT)	25.5 / 155.5	30.75 / 106	35 / 82.1

Table 2: Frequency-capacitance calculus for continuous tuning LC-ILO sizing

In order to achieve the capacitance values just reported, the following equation has been considered, that is the expression of tank resonance frequency:

$$f_{res} = \frac{1}{2\pi\sqrt{LC}} \qquad (17)$$

In (17), from the results of Figure 77, the inductance values L corresponding to f_{max} and f_{min} have been set to 265 pH and 250 pH respectively, while L is 256 pH at f_C. The fine tuning cpo18nw_atto varactor available in the design kit library should be sized in order that the total tank capacitance of the ILFD changes from 82.1 fF minimum to 155.5 fF maximum, according to the control voltage, allowing the ILO self resonance frequencies covering the WirelessHD^{TM} band with the additional margin for PVT compensation.

In the capacitance calculation in (17) should be included the load contributions of layout interconnections, output buffers and parasitic capacitance of the cross-coupled pair. Therefore, a fixed capacitance C_F representing all such contributions to the tank capacitance, must be taken into account when sizing the varactor, according to (12) and (13). Anyway, since the objective of this first ILFD version is setting the simulation environment to analyze the locking state, at this stage is not necessary a detailed account of C_F. The only important values considered now at schematic level are the maximum C_{max} and minimum C_{min} ILFD tank capacitances, that should be ≥ 155.5 fF and ≤ 82.1 fF, respectively, in order to cover the required extended WirelessHD^{TM} band.

The test bench circuit used for the varactor sizing in this section is the same reported in Figure 46, while the simulation and functions employed to get varactors parameters are the same reported in 4.3.1 and 4.3.2. In Figure 78 is shown the layout of the cpo18nw_atto varactor sized in this way:

- 5 x 5 cpo18nw_atto, W=1.8 µm, L=0.75 µm

The varactors terminals V_{op} and V_{on} are placed at the M5 layer (i.e. the blue tracks in Figure 78).
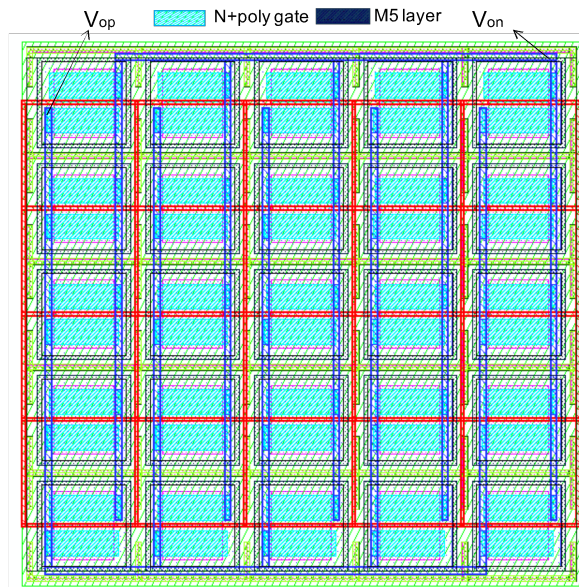
Figure 78: Layout of the 5x5 cpo18nw_atto varactor, W=1.8 µm, L=0.75 µm

Figure 79 shows the varactors characteristics at 30 GHz of the, for different varactor biasing voltage V_{DC}:
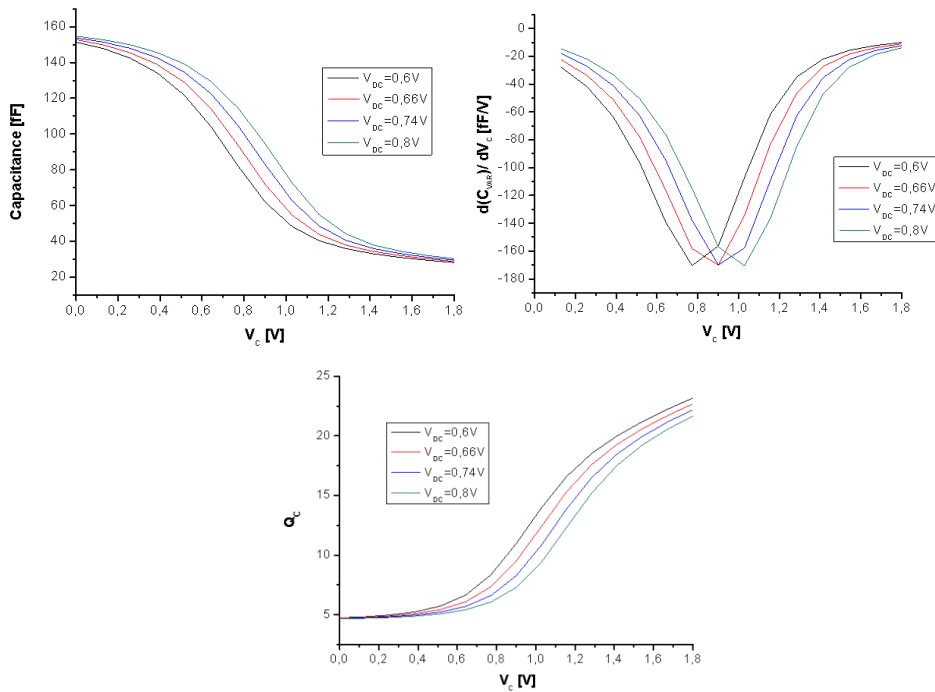
Figure 79: Varactor parameters at 30 GHz for different V_{DC}: varactor capacitance (upper-left); varactor capacitance variation dC/dVc (upper-right); varactor quality factor (lower)

The selected varactor seems to be adequate to cover the required extended capacitance range. Nevertheless, the C_{max} required value is achieved in the extreme of the varactor characteristic, but this is not considered a problem at this point of the design flow since the parasitic capacitance of the cross-coupled pair will add some extra capacitance that would help to cover properly the required range. The curves of Figure 79 have been achieved at 30 GHz simulation frequency for different V_{DC} voltages, that is the DC voltage at varactor terminals, in order to consider the optimum ILO DC output for the varactor. Since the ILO tuning characteristic should be maximized at $V_C = 0.9V$, the optimum DC value for the ILO is found once again around 0.75V (Figure 76 upper-right), and, taking into account that the same value is obtained for the VCO, it seems to be a characteristic of the cpo18nw_atto varactor, independently on its size.

5.2.3 Tank Analysis and ILO PSS Simulation

Figure 80 shows the test bench circuit for the ILO tank S-parameters simulation. The inductor is the one simulated in Figure 77, the varactor is the one just sized in the previous sub-section. C_F is set to 20fF.
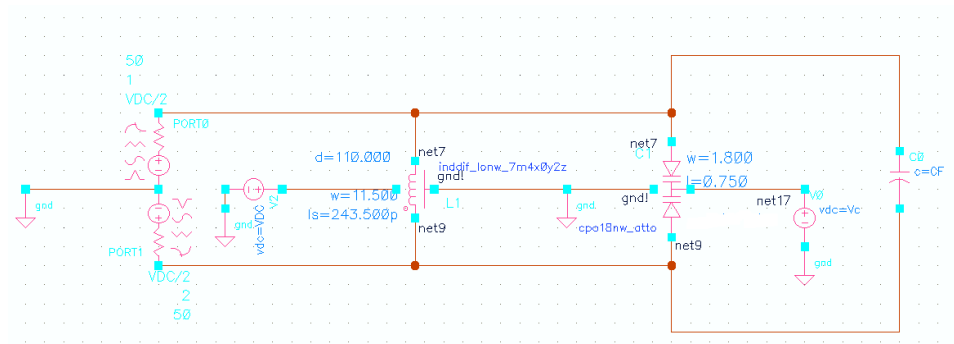
Figure 80: Schematic circuit for continuous tuning ILFD tank

In Figure 81 the tank parameters calculated with the S-parameters simulation of the circuit of Figure 80 are reported:
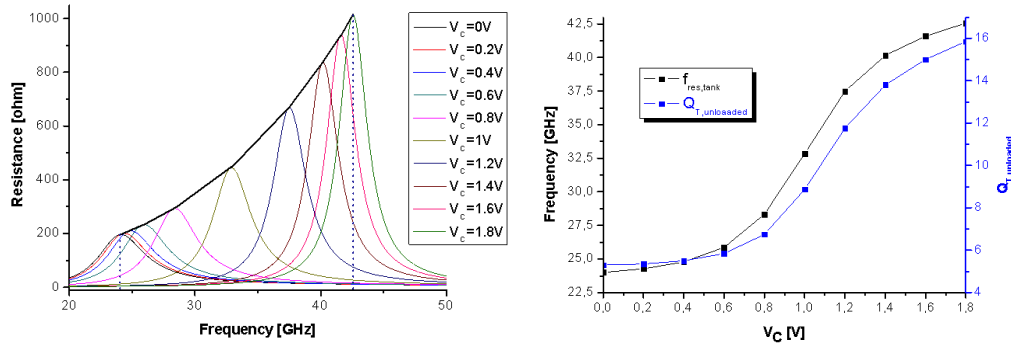
Figure 81: Tank parallel equivalent resistance R$_{p, eq}$ (left); quality factor and resonance frequency of the unloaded tank (right)

The sizing of the continuous tuning varactor, with a fixed capacitive contribution of 20 fF, ensures a ILO tank resonance frequency variation according to the values specified in 5.2.2. The tank resonance frequencies have been calculated as the frequency values which maximize the real part of the inverse of the differential admittance Y_D of the tank (mathematical post processing functions used for these calculations are shown in Appendix A), i.e. the parallel equivalent resistance, $R_{p,eq}$, of the tank. The lower value of $R_{p,eq}$ determines the NMOSs cross-coupled sizing, according to (15), in order to ensure the start-up oscillation at the lower frequency, corresponding to $V_C = 0$.

The curves of Figure 59 are used to size the NMOS transistors. Taking into account an additional margin, a g_m of 20 mS is required for start-up oscillation, corresponding to $g_m = 4 \cdot R_{peq,worst}$. It is achieved with a 25 μm NMOS of 25 fingers, each finger having a width of 1 μm, with minimum length of 60 nm. The cross-coupled pair size and the NMOS V_{GS} (≈ 0.75V) set the overall DC current consumption around 12 mA.

A PMOS transistor is then sized to implement the current source; it is sized with W = 200 μm (200 fingers, each finger 1 μm width) and minimum channel length of 140 nm. In the same way as Figure 67, the bias voltage V_{bias} is adjusted to provide the required DC current. The continuous tuning ILO schematic circuit is shown in Figure 82.

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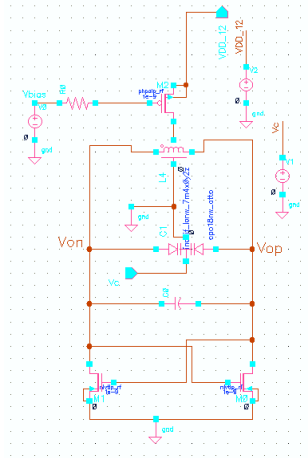
Figure 82: Continuous tuning ILO schematic

The final DC parameters of the circuit obtained after simulation are now reported:

- g_m=21.88 mS

- $V_{DC,out}$=730 mV

- I_{dc}=11.5 mA; V_{dd}=1.2 V

- V_{bias}=760 mV

Steady-state and transient simulations of the circuit of Figure 82 are performed in order to get the ILO self-resonance frequencies and ILO single-ended output waveforms V_{op}, when no signal is injected. The Discrete Fourier Transform (DFT) is then applied to the output waveforms and the results are reported in Figure 83. As it is possible to note, the specified lower and upper f_{min} and f_{max}, respectively, are met; the fixed capacitance C_F has been finely adjusted after a first simulation round for centring the ILO self-oscillation range, resulting in a final value of C_F = 18.2 fF.

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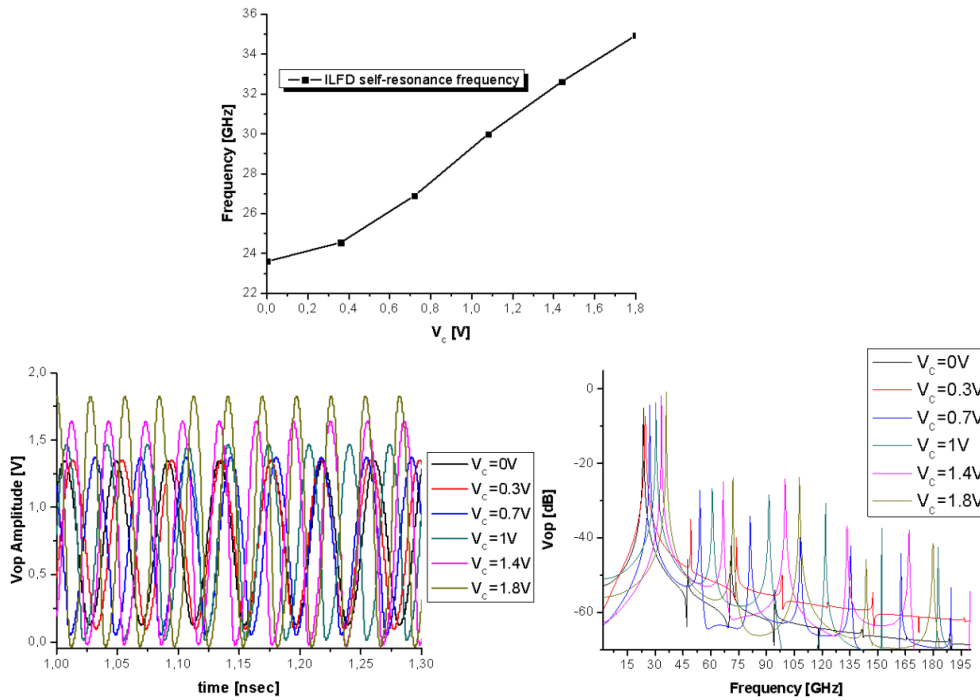
Figure 83: ILFD self-resonance frequency (upper); single-ended V$_{op}$ output waveforms (lower-left) and their DFTs (lower-right)

5.2.4 ILFD Locking Analysis

Once that the free-running ILO has been designed and sized, it is time to set-up the simulations in order to analyze its locking behaviour. In this first divide-by-two ILFD version, a conventional injection scheme is implemented: that is, the 60 GHz signal is injected into the tank through the PMOS transistor, which, hence, has not only biasing function.

Figure 84 shows the schematic circuit of the continuous tuning divide-by-two ILFD. Basically, the difference with the free-running ILO is that an injection path is added to the circuit of Figure 82, connecting an external 60 GHz source to the PMOS gate. A large decoupling capacitor C$_{dec}$ of 10 pF is used for this purpose. An ideal switch is also inserted between the RF source and C$_{dec}$. The switch is used to distinguish between the free-running and injection-running states. In the time domain simulations the switch is closed after a delay (5 nsec in this case). This technique allows for some time for the ILO to start-up and settle in its self-oscillating frequency before applying the input signal for injection locking.

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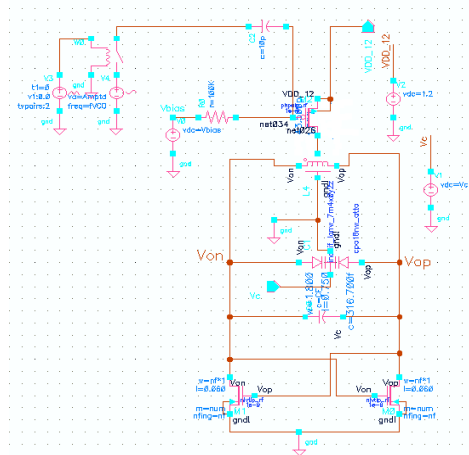
Figure 84: 60 GHz divide-by-two continuous tuning ILFD

The ILFD output frequency is plotted in Figure 85. This result is obtained using a post-processing function: using a given threshold level , the frequency function counts the crossing times of the ILFD output waveform V_{op} (or V_{on} or the differential signal V_{op} - V_{on}) for a transient (time domain) simulation, in order to determine the periodic signal frequency. Figure 85 depicts the transition from the free-running to the locking state: the input signal $V_{inj}(t) = V_{inj} \cdot \sin(\omega_{in}t + \varphi)$, where φ is the initial phase, $\omega_{in} = 2\pi f_{in}$ and f_{in} is the input frequency equal to 60 GHz, is injected into the ILFD tank, through the PMOS source, after 5 nsec the simulation is running. During this period the ILFD output frequency is set to its self-oscillation value, corresponding to the V_C value applied to the fine tuning varactor (in this case $V_C = 0.8V$). After 5 nsec the switch is closed and the signal at f_{in} is injected into the ILFD. If the injected signal has enough power to injection-lock the divider at $f_0 = f_{in}/2$, the ILFD output frequency moves from its self-resonance value to f_0, as illustrated in Figure 85:
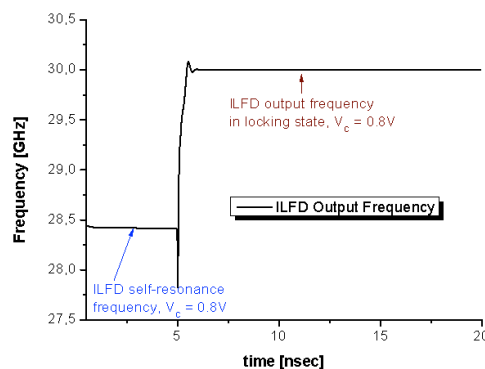
Figure 85: ILFD output frequency, locking state, V_C=0.8, f_{inj}=60 GHz, V_{inj}=300mV

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In Figure 86 $V_{inj}(t)$ and $V_{op}(t)$ are shown, corresponding to the locking state transition just illustrated. Since the amplitude V_{inj} is 300mV, the power associated to the injection signal $V_{inj}(t)$, in a 50 Ω environment, is around 0 dBm. As it is possible to note, before the switch is closed no signal is injected and the ILFD is self-oscillating.
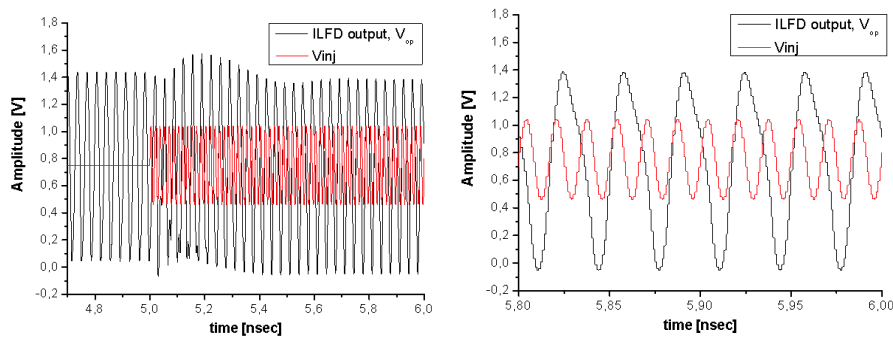
Figure 86: $V_{inj}(t)$ and $V_{op}(t)$, locking state, V_C=0.8V, f_{inj}=60 GHz, V_{inj}=300mV at two different time scales

In the following plot the AC components of the PMOS current is reported, together with its frequency.
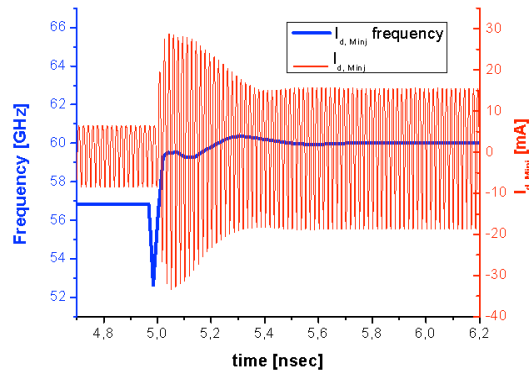
Figure 87: M_{inj} current, locking state, V_C=0.8, f_{inj}=60 GHz, V_{inj}=300mV

The PMOS current, before the switch is closed, is oscillating at its self-resonance frequency, in this case $2 \cdot f_{res}$. After injection, being V_{inj} sufficient to injection-lock the ILFD, the PMOS current frequency moves to $f_{in} = 2 \cdot f_0$. This is the injection current available and at this point a consideration should be done: from (1) and (2) it is clear that the locking range depends on the Q of the tank and on the injection current I_{inj}. Regarding the Q impact on locking range, the next section is completely dedicated to the impact of Q in the ILFD locking range. Regarding I_{inj}, the larger it is, the wider the locking range results,

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according to (1) and (2). It is important to distinguish between the injection current from the source and the injection current effectively available into the ILFD. In the implementation of the circuit in Figure 84 the input signal is injected to the PMOS gate, while the internal injection point is the PMOS drain. Although increasing the injection current from the source increments the available one as well, the locking range is defined by the effective injection power reaching the ILO core. Hence, the locking range can be enhanced by maximizing the available I_{inj}, that is the PMOS (M_{inj}) drain current, while keeping the same injection current from the source, that is by minimizing the losses mechanisms related to the injection scheme, which in this case consists in a power loss across the input source and the M_{inj} drain.

Now the no-locking behaviour is analysed. This means finding for which input power or amplitude, or for which input frequency the ILFD is not injection-locked by the input signal. Keeping the same input amplitude V_{inj} and the same $V_C = 0.8V$, the input frequency fin is first set to 55 and next to 63 GHz. In these conditions, the ILFD is not able to divide properly the input frequency. In Figure 88 the ILFD output frequencies are shown. Note that in both cases, the ILFD self-resonance frequency is the same, corresponding to an instant before the switch is closed, in this case at 2.5 nsec.
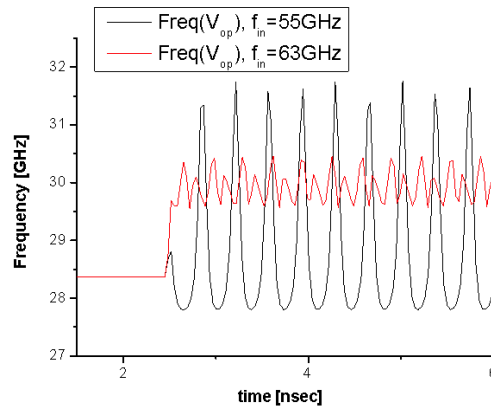
Figure 88: ILFD output frequency, no-locking, V_C=0.8, V_{inj}=300mV

The output waveforms $V_{op}(t)$ and the input signal $V_{inj}(t)$ corresponding to these situations are shown in Figure 89.
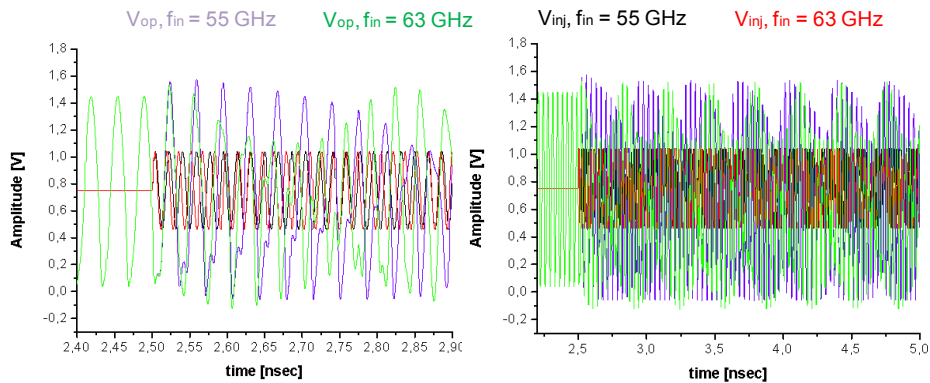
Figure 89: $V_{inj}(t)$ and $V_{op}(t)$, no-locking state, $V_C=0.8$, $V_{inj}=300mV$ at two different time scales

In these situations the ILFD cannot divide properly the input frequencies applied to the M_{inj} gate, basically for two reasons: the injection amplitude V_{inj} is too low, so higher V_{inj} are needed to injection-locking the ILFD, and/or the ILFD self-resonance frequency is too far from $f_{in}/2$. This situation is reflected in a ILFD output signal modulated. In Figure 90 (left) the DFTs of $V_{op}(t)$ of Figure 89 are reported and it is possible to note that there are several tones around $f_{in}/2$. For comparison, in Figure 90 (right) the DFT of the ILFD output frequency function in the case of f_{in} = 55 GHz is reported, that is the DFT applied to the signal of Figure 88 corresponding to f_{in} = 55 GHz. By comparing both spectra it is clear how the ILFD output, in no-locking condition, carries out the information of the beat frequency between $f_{in}/2$ and ILFD output frequency, whereas when locked the ILFD output spectrum only contains the harmonics of the oscillation. This behaviour could be used as an indicator of how much is the ILFD far from the locking state. This issue will be further clarified in the following pages:
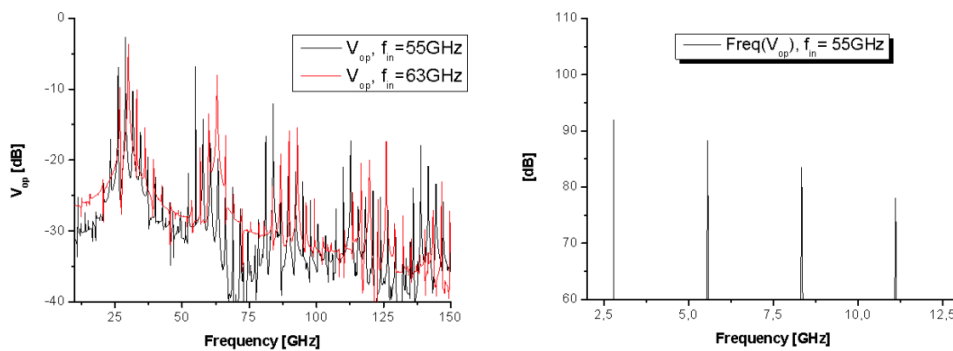
Figure 90: $V_{op}(t)$ DFTs (left); ILFD output frequency DFT (right). No-locking state $V_C=0.8$, $V_{inj}=300mV$

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Finally, the available injection currents and their frequencies, corresponding to the two no-locking states considered above, are reported in Figure 91 and Figure 92, respectively. It is important to note that the "pseudo" available injection current, since there is no locking, vanishes periodically, hence the injected power is not enough to lock the ILFD at $f_{in}/2$.
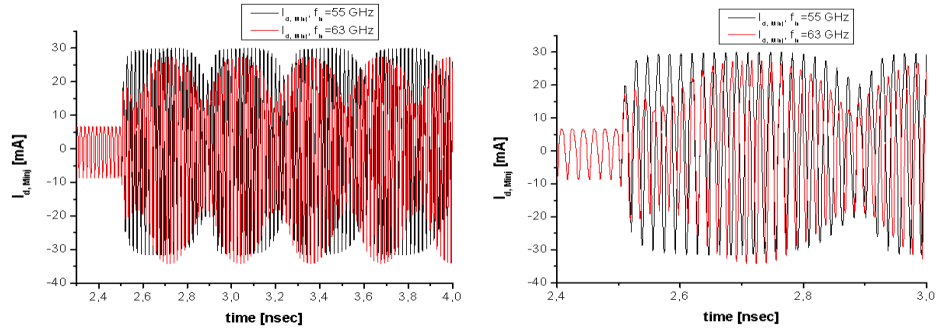
Figure 91: Available I_{inj} in no-locking state, V_C=0.8, V_{inj}=300mV at two different time scales
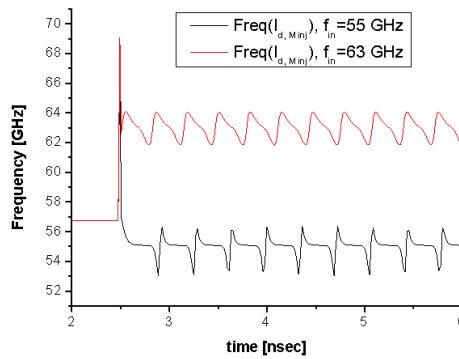
Figure 92: Frequency function of the curves of Figure 91

5.2.5 *ILFD Input Sensitivity Curves*

In order to obtain the ILFD input sensitivity curves, it is important to note that there is a curve for each value of V_C. The couple of points (Input Frequency; Input Power) that set the limit between the locked and un-locked states should be reported in a "Input Power" versus "Input Frequency" Cartesian plane for each V_C. To do it, the ILFD input frequencies and the ILFD input power, corresponding to the V_{inj} applied, are swept, together with V_C, in order to get the typical "V-shaped" curves. This shape is caused by the fact that the farther (above or below) is the input frequency from the 2nd harmonic of the ILFD self-

oscillation frequency for a particular V_C value, the higher is the input power required for locking.

As previously mentioned, the ILFD output frequency, even if in no-locking state, carries out in some way the information regarding how much far from reaching locking the ILFD is. This is better understood by comparing Figure 93 (black curve) with Figure 88 (black curve), where f_{in} is increased up to 56 GHz, while keeping the same V_{inj} and V_C; the locking is not yet reached, although the periodic change of the ILFD output frequency is slowed down. This reflects a lower beat frequency. It means that, since now f_{in} is moved up nearer to $2 \cdot f_{self,res\_Vc=0.8V}$, the ILFD is closer to be locked. In fact, if V_{inj} is increased up to 400 mV, Figure 93 (red curve), while keeping V_C and f_{in} constant, the ILFD output frequency is exactly $f_{in}/2$, meaning that the ILFD is now injection-locked.
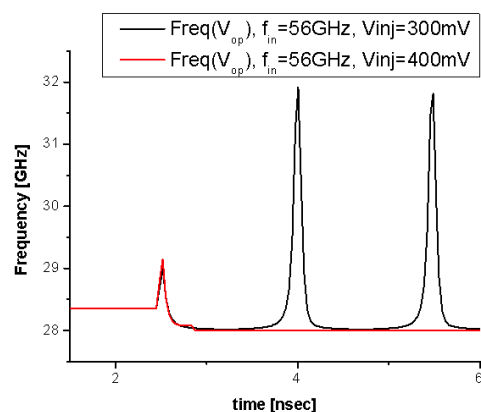
Figure 93: ILFD output frequency, V_C=0.8

The input sensitivity curve corresponding to a given V_C value can be obtained in the following way. For each V_{inj}, f_{in} is swept above and below the self-oscillation frequency of the ILFD, for that V_C, and the points corresponding to lower and upper f_{in} values that result in locking are noted. These two values are plotted in the Cartesian plane (Input Frequency; Input Power). Then, the operation is repeated, but at a lower V_{inj}, reducing the input frequency range. This process is iterated up to the number of required points is achieved. In Figure 94 the ILFD output frequency curves, corresponding to V_C = 1.8V, for different V_{inj} and f_{in} are shown. Using the above explained technique it is easy to distinguish the curves corresponding to locking or un-locking situations.
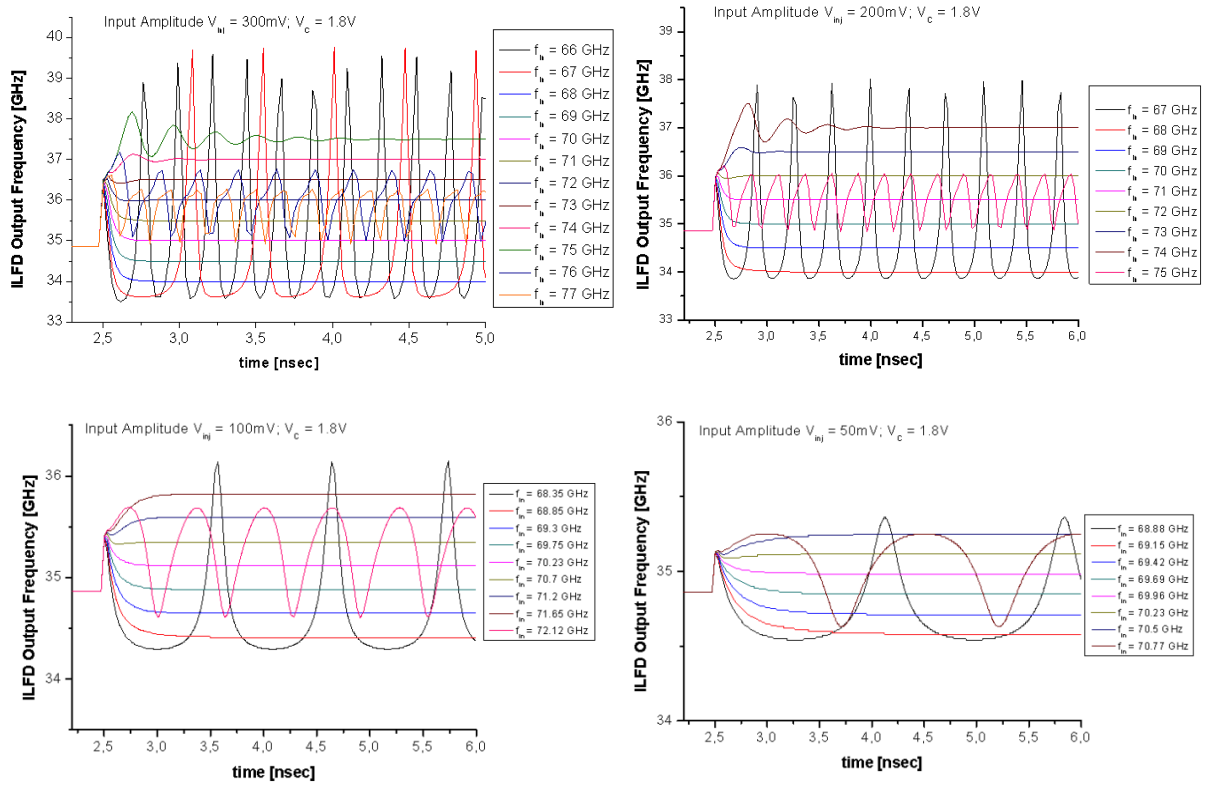
Figure 94: ILFD output frequencies, V_C = 1.8V

The operation illustrated in Figure 94 is then repeated for V_C = 0V, in order to plot the lower and upper ILFD sensitivity curves, shown in Figure 95. Usually the locking range is reported corresponding to 0 dBm input power, which corresponds to V_{inj} ≈ 300mV at 50Ω. Hence a conversion volt-to-dBm is performed to plot the input sensitivity curves using the usual units (Hz ; dBm).
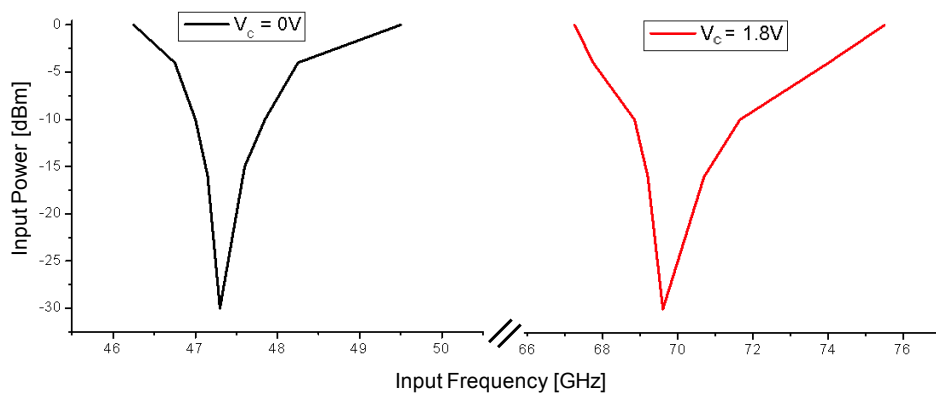
Figure 95: Lower and upper ILFD input sensitivity curves

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The locking range achieved at 0 dBm, using the continuous tuning mechanism employed in the first version of the ILFD designed in the framework of this Thesis, is ≈ 47.5%, i. e. from 46.5 GHz to 75.5 GHz, wide enough to cover the WirelessHD^{TM} band also taking into account PVT variations. Nevertheless, this ILFD is not suitable to be integrated in a 60 GHz PLL, since the PVT calibration will be difficult to be implemented due to the continuous tuning. That is, a discrete tuning is needed. But the objective of this first ILFD design, presented at DCIS 2010 [2], is mostly to set-up the simulation environment required for the next design optimization while investigating the opportunity of tuning mechanisms to cover the overall bandwidth with an extra frequency range for PVT compensation.

Two final remarks are done before closing this section. The first one is about the feasibility of a fixed-frequency ILFD, i.e. without tuning capabilities. In Figure 96, the input sensitivity curve for V_C = 0.85V is reported. The locking range at 0dBm is between 57 GHz and 64.2 GHz, that is only 11.88%. It covers the WirelessHD^{TM} band, but no extra margin for PVT is available without the tuning mechanism.
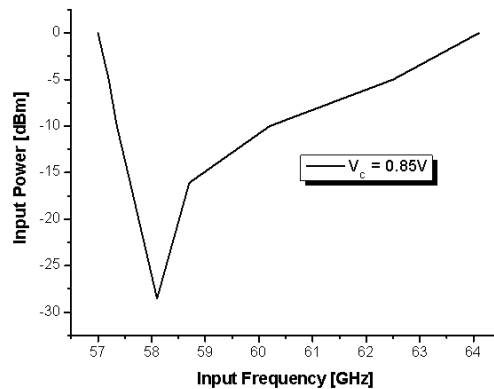
Figure 96: ILFD Input sensitivity curve, V_C = 0.85V

The second remark is about the different locking behaviour in the two extremes of the input frequency band. From Figure 95 and Figure 96 it is possible to note that the ILFD is hard to be locked for input frequencies below 2·$f_{self,res}$. That is the locking range is higher for input frequencies higher than 2·$f_{self,res}$ and the ILFD input sensitivity curve is not symmetrical. This is due to the band-pass filter shape produced by the ILFD tank, where the frequencies below $f_{self,res}$ are more attenuated if compared to those above $f_{self,res}$, as shown in Figure 97, where the S_{21} parameter corresponding to the simulation of the circuit in Figure 80 is plotted. The curve shown in the figure illustrates the asymmetrical bandpass characteristic of the ILFD tank.

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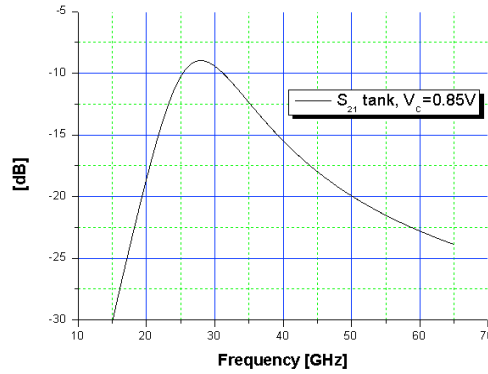
Figure 97: S$_{21}$ ILFD tank

5.2.6 Conclusions

The ILFD locking range achieved with continuous tuning seems to be able to cover the overall WirelessHD[TM] band taking into account an extra frequency dividing range for PVT calibration. Nevertheless, as already mentioned, the continuous tuning varactor should be replaced by a digitally controlled varactors bank, in order to integrate the ILFD inside a PLL where a calibration circuit has to be implemented. The optimization of some parameters is essential in order to maximize the locking range. As previously said, optimizing the injection efficiency, that is reducing the parasitic capacitance to ground in the injection path, at the PMOS drain in the schematic of Figure 84, will increase the locking range since more injection current is available into the ILO. As reported in Figure 98, where the current gain corresponding to locking state is plotted, it is possible to note that $I_{inj,av}/I_{inj,source}$ in this first ILFD version is around -5 dB for f_{in} = 70 GHz (V_C = 1.8V), which is the higher end of the input dividing band, while it has been found to be around -4 dB for f_{in} = 48 GHz (V_C = 0V), the lower end.
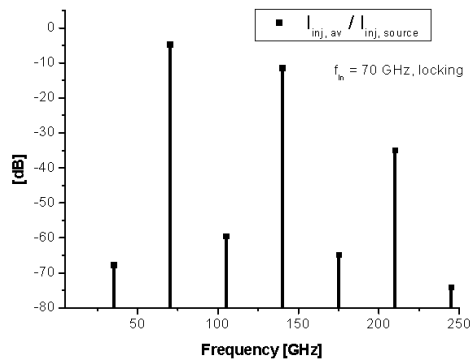
Figure 98: $I_{inj,av}/I_{inj,source}$, V_C=1.8

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The circuit of Figure 84 has considerably parasitic capacitance at M_{inj} drain, basically formed by the C_{gd} and C_{db} of the PMOS. Furthermore, taking into account that M_{inj} has also a biasing function, such transistor width needs to be large, hence increasing the parasitic capacitance at the drain node. To alleviate this issue, a shunt peacking inductor has been inserted in the circuit to resonate out that capacitance [3], but at expenses of increasing the chip area due to the inductor integration. Therefore, other injection scheme should be investigated to improve the injection efficiency in order to maximize the locking range without impacting the area significantly.

Other option available for increasing the locking range from (1) and (2) consists on decreasing the tank quality factor (Q). This should lead to increase the ILFD locking range, since smaller Q values correspond to wider band-pass bandwidths for the LC tank. Next section is devoted to the analysis of the impact of High Q and Low Q ILFD tank on the ILFD locking range. Nevertheless, low Q tanks lead to higher ILFD power consumption, since higher g_m is required to achieve oscillation start-up. As a conclusion, there is a trade-off between wide locking range and low power consumption, if the ILFD locking range is optimized only acting on the tank Q.

A final remark about locking range for tuneable ILFDs follows. By analyzing Figure 95 and Figure 96 it is possible to see that the achieved locking range is wider when the ILFD is tuned to operate at higher input frequencies: this is consistent with the ILO locking range expression given by [4]:

$$\Delta\omega = \frac{I_{inj}}{V_o} \frac{1}{C_T} \tag{18}$$

where V_o is the oscillation amplitude and C_T is the whole tank capacitance: the locking range is wider where the tank capacitance is lower, i. e. when the varactor used in this first ILFD version is set to its minimum capacitance value and the ILFD self-oscillation frequency is at its higher value. So in order to maximize the locking range, low tank capacitance should be implemented.

The next design step consists in conceiving a first version of a discrete tuned ILFD, since in order to implement frequency calibration for high precision mm-W PLL a digital control is needed. This will be combined with the study of the impact of the tank Q in the ILFD locking range.

5.3 Impact of Tank Q in Divide-by-Two ILFD Locking Range

In this section the design of two divide-by-two discrete tuned ILFDs is presented. In both designs, a 4-bit digitally controlled varactors bank, differently sized, is implemented. The ILFD tanks present high and low tank Qs and the

locking ranges achieved in both circuits are compared. For both ILFDs, the implemented injection scheme is the same, that is, both use a conventional injection from the current source, since the objective is to evaluate the impact on locking range of the tank design.

At first the tank design flow is shown, presenting the main tank parameters. Then two discrete tuned ILOs are designed and their power consumption and tuning range are evaluated. Finally, the input sensitivity curves of the two ILFDs are plotted and compared.

5.3.1 High Q / Low Q ILFD Tanks Design

At mm-W frequencies, the silicon implementation of the varactors has an high impact in the overall Tank Q (Q_T) of a LC oscillator. While at lower frequencies it is true that $Q_T \approx Q_L$, where Q_L is the inductor quality factor, at mm-W frequencies Q_T is:

$$\frac{1}{Q_T} = \frac{1}{Q_C} + \frac{1}{Q_L} \tag{19}$$

where Q_C is the varactor quality factor. If $Q_C \gg Q_L$, $Q_T \approx Q_L$. But at higher frequencies this assumption is not true for on-silicon varactors since their design has larger weight in (19) due to their higher losses. So, in order to get high and low Q_T, the design starts from the varactors banks and then the required inductances are selected.

Figures 99 shows the architecture employed in order to implement the 4-bit varactors bank. Such architecture is the same used for the VCO design in 4.3: a set of cpo18nw_atto varactors that are binary scaled. There is a total of 15 unit varactors, used to provide discrete tuning by means of a digitally controlled capacitance change. Each digital bit controls a multiple of a unit varactor, grouped in 1 (2^0), 2 (2^1), 4 (2^2) and 8 (2^3) cells, for bits b_0, b_1, b_2 and b_3, respectively.
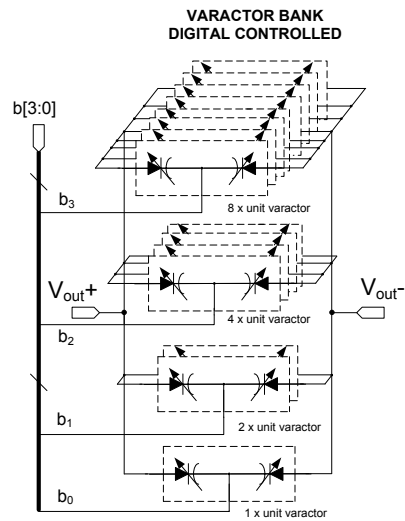
Figure 99: 4-bit varactors bank binary scaled

In Figure 100 the test bench circuit for the varactors banks simulation is shown. The unit cell cpo18nw_atto varactor is a 2x2 array with W=0.96 μm and L=0.5 μm for the low Q_T, while it is a 3x3 array with W=0.9 μm and L=0.15 μm for the high Q_T. The V_{DC} value for the low and high Q_T is 740 mV and 720 mV, respectively. Such values have been found by simulation, calculating the abscise at which the varactors bank dC/dV is maximized for the central digital code b[3:0] = 1000.
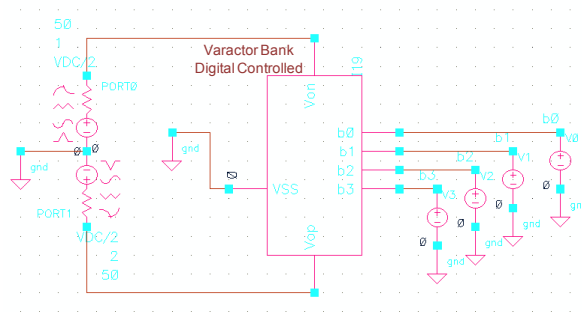
Figure 100: Schematic circuit for 4-bit varactors bank simulation

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Figure 101 compares the two varactors banks main characteristics (capacitance, parallel equivalent loss and quality factor). The high-Q varactors bank shows lower C_{max}, while C_{min} is almost the same in both cases. This is because the ON[2] capacitance (corresponding to V_C = 1.8) of the unit varactor cell is basically the same in both cases. In order to achieve low Q_T in a LC discrete tuned ILFD, large varactors are required. This means getting higher capacitances. Consequently, there is a trade-off between (1)-(2) and (18), since in order to maximize the locking range low Q_T is needed, but to achieve it a higher tank capacitance is required that degrades the locking range.
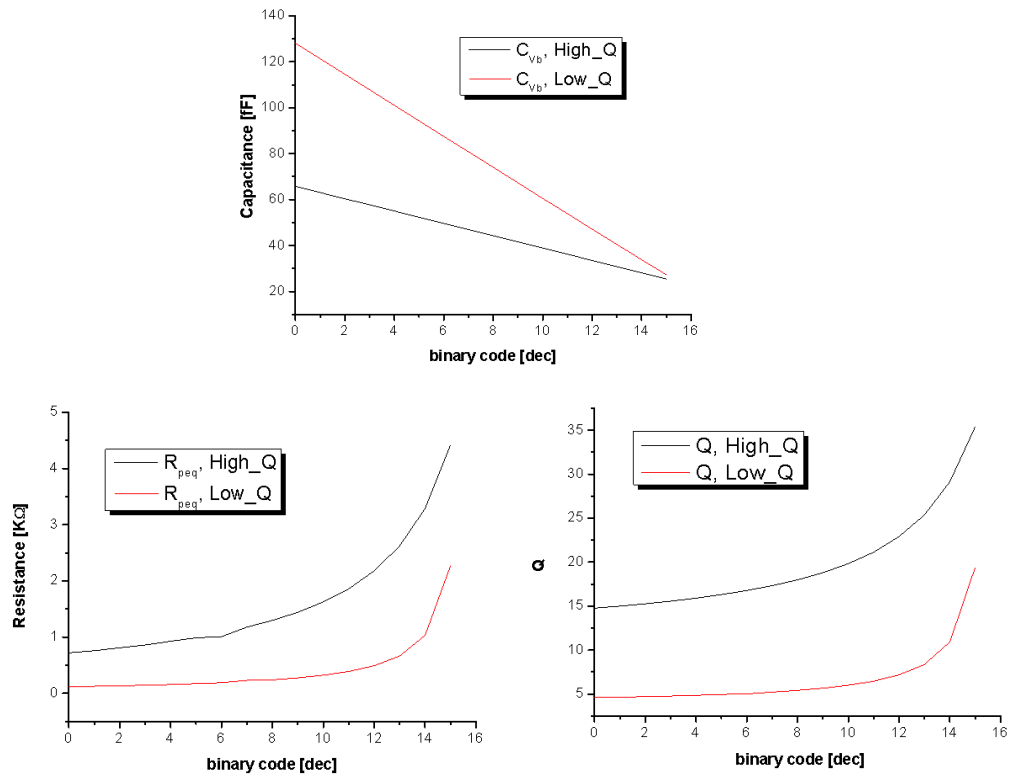
Figure 101: Capacitance (upper), parallel losses (lower-left) and quality factor (lower-right) of the High/Low Q varactors banks

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[2] Note that the code "1111" sets all the varactors ON, i.e. to their minimum capacitance. A "0" logic value corresponds to a voltage control of 0V and a "1" to 1.8V.

It is important to avoid confusing between the ILFD locking range and its digitally controlled tuning range. The first is the width of the sensitivity curve for a given digital code (see for example Figure 96). This is the locking range that is affected by high or low Q_T and tank capacitance value. The second one is set by the achievable C_{max}/C_{min} for the extreme digital codes. Such discrete tuning range is increased for low-Q varactors bank, since C_{max} is higher in this case. However, since the locking range is reduced for larger capacitance values (18) it may happen that two consecutive binary codes in the low ILFD input frequency range result is non-overlapping the corresponded sensitivity curves, which implies that a portion of the input band could not be divided since it falls between the dividing range of these two consecutive binary codes. This situation is further illustrated later. As a summary, a wider ILFD discrete tuning range does not necessarily result in a wider ILFD dividing range.

In order to cover the required bandwidth with an additional margin for PVT compensation, two different inductors have been selected to resonate out each one the previously designed discrete tuning varactors banks. The following table resumes the calculations using (12) and (13):

L [pH] @ 30 GHz	f_{min} [GHz] / C_{max} [fF]	f_{max} [GHz] / C_{min} [fF]	C_F [fF]
372 (High-Q)	27.4 / 68 + C_F	36.1 / 25 + C_F	24
243 (Low-Q)	25 / 129 + C_F	39.5 / 27.3 + C_F	40

Table 3: Inductors selection for High / Low tank Qs.

An higher C_F is obtained in the case of low Q_T, since wider transistors formed the cross-coupled pair are required, to compensate higher tank losses. Note that at this stage C_F includes the loading capacitance contributions of the cross-coupled pair, output buffers and parasitics of the layout for interconnections.

In the next Figure 102 the series inductance and quality factor of the selected inductors are reported. The test bench circuit used for simulating the inductors is the same of Figure 44.
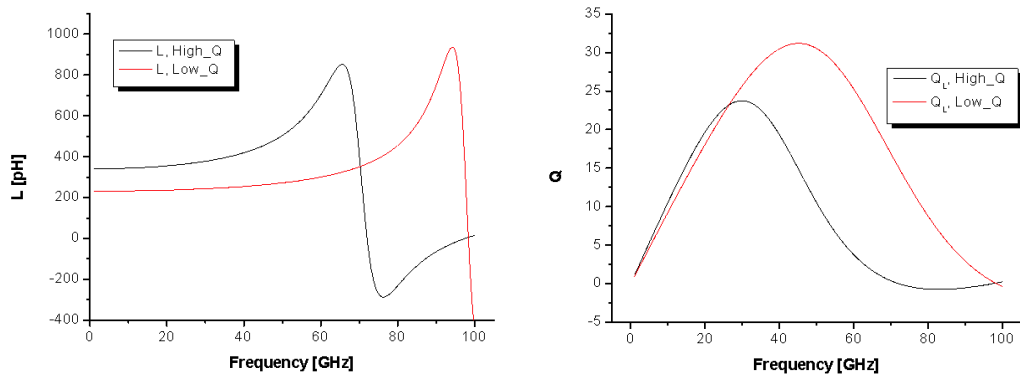
Figure 102: High Q / Low Q inductance (left) and Q (right)

The two selected inductors have the same conductor width (W = 9.5 µm), while obviously the diameter is different, since different inductance are required. For the low Q_T the inductor diameter is 110 µm, while in the case of high Q_T it is 145 µm. Furthermore, the inductors have been selected in order that Q_L is nearly the same at 30 GHz in both case, so that Q_C is dominating Q_T in both cases.

The test bench circuit for tank simulation is reported in Figure 103:
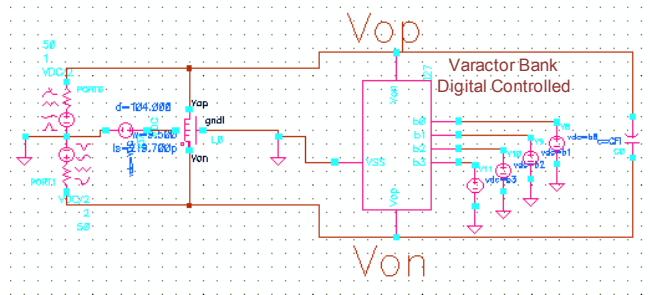
Figure 103: Schematic circuit for low /high Q tank simulation

Summarizing, C_F = 24fF and V_{DC} = 720mV for the high Q_T, with its varactors bank and inductor, while C_F = 40fF and V_{DC} = 740mV in the case of low Q_T, with the other varactors bank and inductor.

Figure 104 shows the resonance frequency, parallel equivalent losses and Q of the tank in both cases. The required g_m for the low and high Q_T is 6.2 mS and 2.5 mS, respectively, calculated using (15). Taking into account that an extra margin is required to ensure reliable and robust start-up oscillation at lower frequencies, basically a further factor 2 in (15) is used. As a consequence,

the goal is achieving a g_m of 12.4 mS and 5 mS, for the low and high Q_T, respectively.
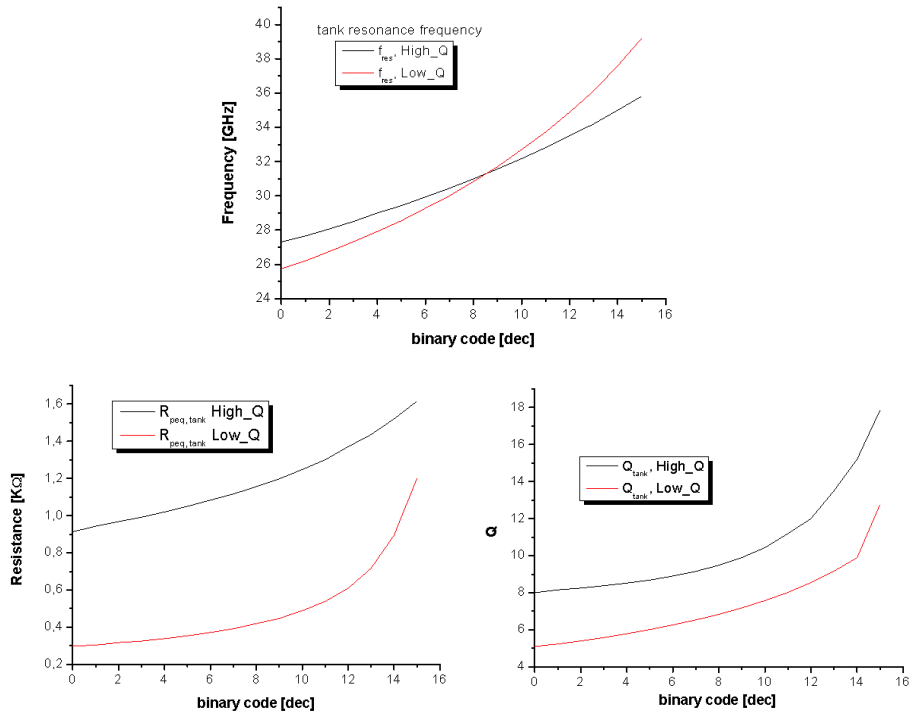
Figure 104: Low / high Q tank parameters

5.3.2 High Q / Low Q Discrete Tuned Free-Run ILO

Figure 105 shows the schematic circuit of the 4-bit discrete tuned ILO:
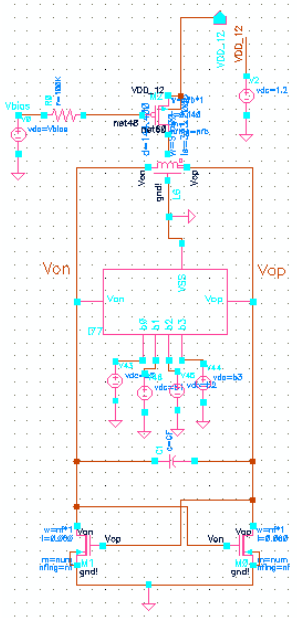
Figure 105: 4-bit discrete tuned ILO

In the next Table 4, sizing of transistors and DC parameters of both low and high Q ILOs are reported, considering a voltage supply of 1.2V:

	W_{CC} [μm]	W_{inj} [μm]	V_{bias} [mV]	I_{dc} [mA]	V_{DD} [V]	g_m [mS]	$V_{DC,out}$ [mV]	C_F [fF]
Low-Q ILO	14	150	750	7.8	1.2	5.1	735	22
High-Q ILO	6	60	730	3.33	1.2V	12.6	710	20

Table 4: High Q / Low Q ILFD transistor sizing and DC parameters

W_{CC} is the NMOS cross-coupled transistor width, sized according to the results of the simulation shown in Figure 59. W_{inj} is the PMOS transistor width which is used for biasing but also to inject the input mm-W signal. All the transistors are sized at the minimum channel length (it is 60 nm for the NMOS and 140 nm for the PMOS).

In the case of the high-Q ILFD, the PMOS transistor has been sized with a lower as possible width, in order to reduce the parasitic capacitance to ground at its drain terminal, which impacts the injection path gain. This is

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because, due to the high-Q, a narrow locking range is expected. Therefore, a compensation is applied by decreasing the parasitic capacitance to increase the injection current available.

The power consumption is higher in the case of low-Q, as expected: it is more than twice compared to that of the high-Q ILO. The fixed-capacitance C_F is lowered down to 22 fF in the case of low-Q ILO, since wider cross-coupled pair is required if compared to high-Q, where C_F is reduced only by 4 fF due to the insertion of 6 μm width NMOSs.

Figure 106 shows the ILFD self-resonance frequencies. Wider ILO tuning range is achieved in the case of low-Q as expected, due to the higher variation of tank capacitances for the same binary code range, compared to the high-Q ILO tuning range. In both case, the divided-by-two WirelessHD^{TM} band is covered, but the high-Q ILO has a smaller margin for PVT compensation.
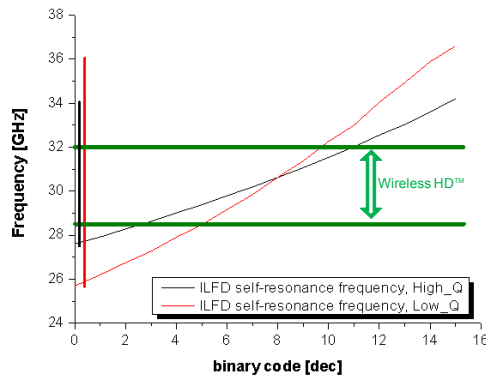
Figure 106: Low / high Q ILFD self-resonance frequencies

Next Figure 107 shows the differential output waveforms (V_{op} - V_{on}), corresponding to all the sixteen binary code of the b[3:0] control word when the ILFDs are self-oscillating.
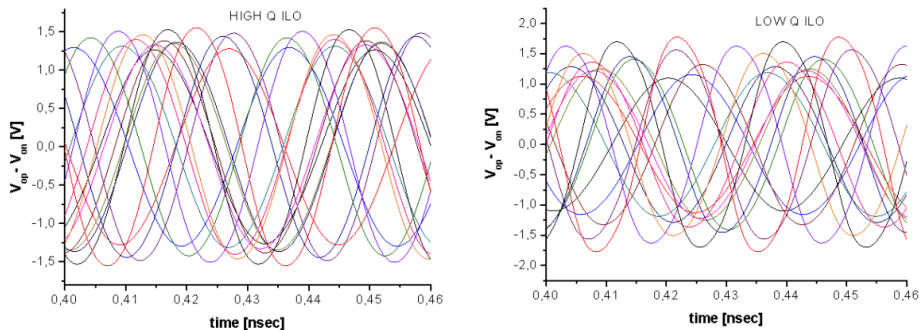
Figure 107: Low / high Q ILFD differential output in self-oscillation

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5.3.3 High Q / Low Q Discrete Tuned Divide-by-Two ILFD

Figure 108 reports the schematic circuit of the 4-bit discrete tuning divide-by-two ILFD in order to compare the locking range in both high and low Q designs. Comparing to the circuit of Figure 105 an injection path is added, connecting the external mm-W input source to the PMOS gate, through a large decoupling capacitor C_{dec} (C = 10 pF).
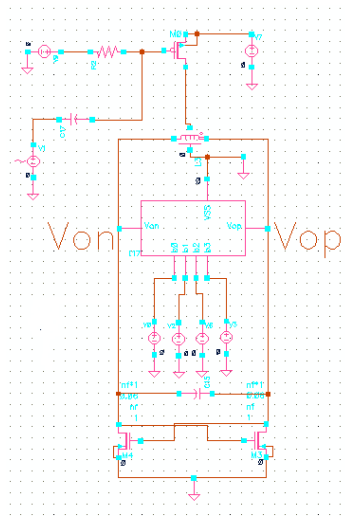
Figure 108: 4-bit discrete tuned ILFD

In the same way as that presented in 5.2.5, the low / high Q ILFD input sensitivity curves are obtained and plotted in Figure 109 and Figure 110, respectively. Since these ILFDs have discrete tuning capability, there are sixteen sensitivity curves, corresponding to the sixteen binary codes b[3:0].
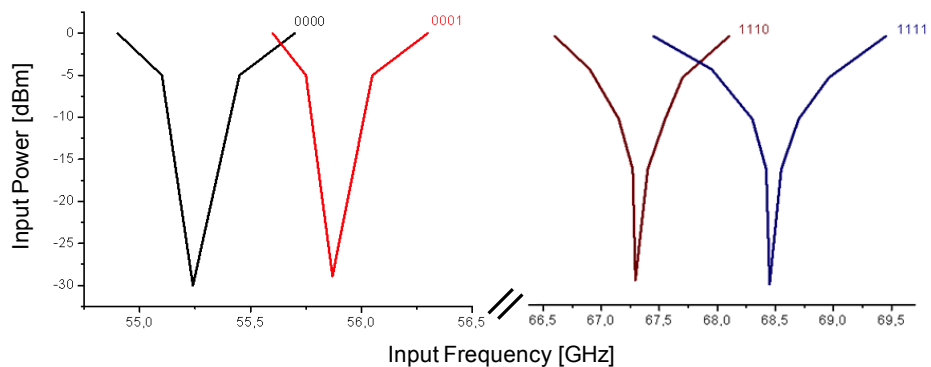
Figure 109: High Q 4-bit discrete tuned ILFD input sensitivity curves

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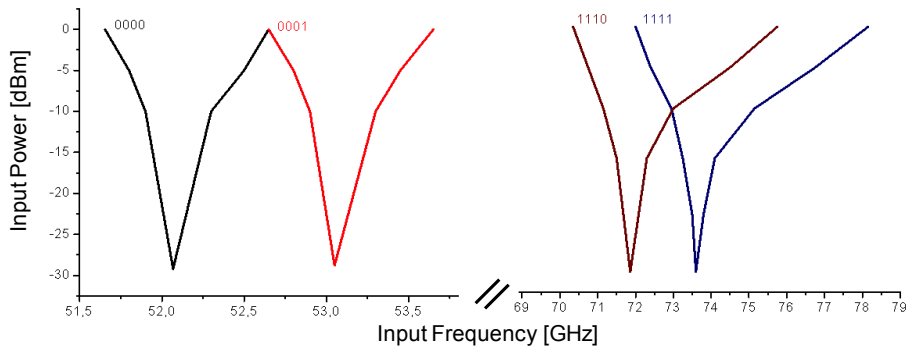
Figure 110: Low Q 4-bit discrete tuned ILFD input sensitivity curves

The locking range achieved for an input power of 0 dBm for the high and low Q discrete tuned ILFDs is 23.42% and 41.7% respectively, corresponding to an input frequency range of 54.85 GHz-to-69.4 GHz and 51.25 GHz-to-78.3 GHz, respectively. This is the total locking range provided when the ILFD is tuned adequately for each input frequency sub-range using the binary code b[3:0].

Both ILFDs are able to cover the full WirelessHD^{TM} band with some additional margin for PVT compensation, but as it is made evident by comparing the sensitivity curves of Figure 109 and Figure 110, the high-Q ILFD shows less overlapping between two consecutives input sensitivity curves if compared to the low-Q ILFD. This is mainly because the high-Q ILFD input sensitivity curves are not as wider as the ones of the low-Q. This means that the locking range at 0 dBm, corresponding to the single input sensitivity curves for the low-Q ILFD, is wider if compared to that related to the single input sensitivity curves for the high-Q ILFD, as shown in Figure 111. This is consistent to (1) and (2).
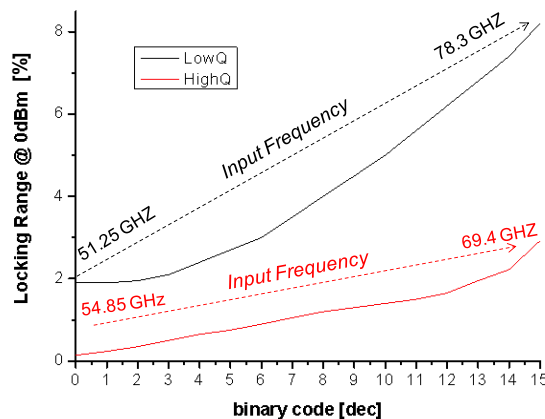
Figure 111: Locking range of the single sensitivity curve

In addition to the previous consideration, low-Q discrete tuned ILFD achieves wider total locking range. It could be explained with the consideration that the self-resonance frequencies corresponding to two consecutive binary codes are more spaced between them (see Figure 106) if compared to the high-Q ILFD, so that two adjacent input sensitivity curves in this case are farer from each other. Nevertheless, as already observed, considering single input sensitivity curves, their width is always higher for the low-Q ILFD, reflecting in narrower total locking range for the high-Q ILFD.

On the other hand, the impact of the tank capacitance seems to not affect the overall tuned locking, since even if the whole tank capacitance is lower in the case of high Q for each binary code, the locking range is narrower in this case and, therefore, the total tuned locking range is reduced since adjacent sensitivity curves need to have some overlap. Figure 111 is a good illustration of the locking range analytical expressions presented previously. First of all, the higher Q ILFD shows the smaller locking ranges for all the binary tuning codes, consistent to (1) and (2). Secondly, as the binary tuning code increases, lowering the total tank capacitance in both ILFDs, the locking range is increased, according to (18).

Finally, although the injection parasitic capacitance in the high-Q ILFD is lower (since W_{inj} = 60 μm), it is still high: $I_{inj,av}/I_{inj,source}$ is around -3.5 dB at f_{in} = 69 GHz (b[3:0]=1111, high-Q ILFD) while it is -4.4 dB at f_{in} = 73 GHz (b[3:0]=1111, low-Q ILFD).

5.3.4   *Conclusions*

In a discrete tuned ILFD it is very important to evaluate the crossings between adjacent input sensitivity curves. Figure 111 illustrates an interesting trade-off between tuning and locking range. The locking range can be enhanced by decreasing the tank Q but this brings as a consequence a larger capacitance range in the discrete tuned varactors bank, which results in a wider tuning range. This has to be carefully analysed since it could result in non-overlapping sensitivity curves. On the other hand, an high-Q varactor bank results in narrower sensitivity curves but also in a total smaller tuning range since the varactors bank capacitance range is smaller. In this case it may be easier to attain overlapping of the adjacent ILFD input sensitivity curves, but the total dividing range may result not wide enough.

Figure 112 shows the plot of the resulting discrete tuned ILFD input sensitivity curve, for both low and high Q ILFDs:
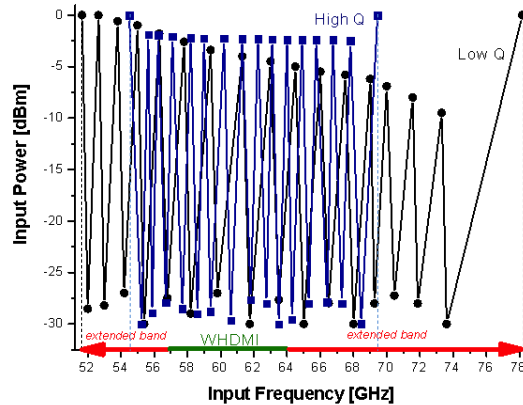
Figure 112: Resulting discrete tuned ILFD input sensitivity curves

Both ILFDs have at their disposal lower and upper additional bandwidths, as marked in Figure 112, in order to compensate frequency shifts due to PVT variations. The high-Q ILFD achieves a total locking range at 0 dBm of 23.42%, practically twice the nominal one required corresponding to WirelessHD[TM] band, while the locking range of the low-Q ILFD is the wider locking range ever reported, at least to the best of the author knowledge. The low-Q discrete tuned ILFD design reported in this section has been presented at ESSCIRC 2010 [5]. However, it is important to note that the low-Q ILFD requires 7.8 mA of current consumption, more than twice the one of the high-Q ILFD (3.33 mA).

In order to ensure a robust operation between VCO and ILFD in a 60 GHz PLL, an high sensitivity FD is required. That is, it is not realistic to expect 60 GHz signals, proceeding from the VCO output buffers, with amplitudes much larger than 200 mV, as reported in [6] and also shown in this Thesis (see Chapter 6 and Chapter 8). Note that 200 mV corresponds to an ILFD input power around - 4 dBm in 50 Ω environment. It is possible to see in Figure 112 that, in the case of the low-Q discrete tuned ILFD, the input frequencies that are locking the divider for an input power lower than -4 dBm are only from around 61 GHz up to ≈ 77 GHz, while in the high-Q ILFD the locking is ensured between 54.5 and 69 GHz for input power lower than -2.5 dBm.

A closer look at the sensitivity curves overlapping shown in Figure 113, allows to verify that for input powers of - 4 dBm some VCO frequencies like those around 54.5 GHz, 55.7 GHz, 56.25 GHz and 57.1 GHz cannot be tracked, i. e. divided, by the high-Q ILFD. The same consideration applies also to the low-Q ILFD, as reported in the same graph in Figure 113, although the frequencies not correctly covered vary.
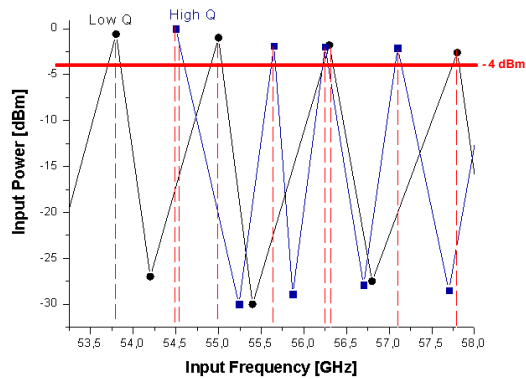
Figure 113: Sensitivity analysis

As a summary of the previous analysis, adopting a digital controlled varactors bank in order to improve the ILFD locking range is indeed a good strategy, although a different injection scheme than this considered until now in this work should be implemented in order to improve the injection efficiency. This should allow to get an overall wider ILFD locking range corresponding to lower input power, in the overall band of interest. Using, the current source as injection transistor results in a large parasitic capacitance to ground in the injection path, degrading the injection efficiency. In such scheme, the PMOS has both mixing and biasing functions requiring a large transistor width, which is incompatible with the lower parasitic capacitance required to improve the injection efficiency.

As a conclusion, even if it is true that a low-Q tank results in wider ILFD locking range, as it has been demonstrated, it requires higher power consumption due to higher tank losses. From (1) and (2) it is clear that the ILFD locking range can be improved by optimizing the tank design (Q) but also by optimizing the injection scheme ($I_{inj,av}$). Therefore, it would be possible taking advantage of the low power high-Q ILFD design by compensating the negative impact of a large Q in the locking range with an improvement in the injection efficiency, with the goal of implementing a low power consumption, wide locking range ILFD. This issue is addressed in the next section.

5.4 Dual-Mixing Discrete Tuned ILFD Design

In this section the final ILFD design that is selected to be manufactured is presented. The design is completed in the following chapter, where the layout issues are presented. A different injection scheme, compared to the one used in the previous ILFD designs, is investigated and implemented in order to improve the injection efficiency and maximize the locking range at lower input power. The dividing range is further enhanced taking advantages of the discrete tuning capability provided by a 3-bit digitally controlled, binary scaled varactors bank..

Dual mixing technique starts from the consideration that injecting the input signal directly into the ILFD tank, so named direct-injection scheme as illustrated in 3.5, Figure 37, allows to improve the locking range, because of the increased injection efficiency, since the injection transistor has no biasing function and it could be sized independently and made smaller, therefore minimizing the parasitic capacitance to ground that leaks some of the input power.

Nevertheless, in the conventional direct-injection, Figure 114 (left), the transistor M_{inj} acts as a mixer: in order to achieve higher locking range for wideband operation, its transconductance g_m should be large. However, a large g_m implies larger parasitic capacitance. Hence, the conventional direct injection scheme has the drawback of reducing the ILO operation frequency range due to the M_{inj} contribution to the overall ILO tank capacitance (C_{p+} and C_{p-}). In addition, even if the capacity to ground in the injection path is reduced, since now the injection transistor has no bias function, some amount of parasitic capacitance is always presents. A series peacking technique has been introduced in [7], to resonate out those capacitances, but this is always at the expenses of increasing significantly the chip area with additional on-chip inductors. C_{p+} and C_{p-} are capacitances to ground that are Miller equivalent to the differential capacitance between ILFD outputs V_{out+} and V_{out-}. Therefore, higher g_m for wider locking range, in direct injection ILFD topology, implies an M_{inj} sizing which gives an upper limit to the ILO operation frequency.

Figure 114 (right) shows the discrete tuned dual mixing ILFD schematic. In both ILFDs in Figure 114 the bias circuits of the injection stage are omitted:
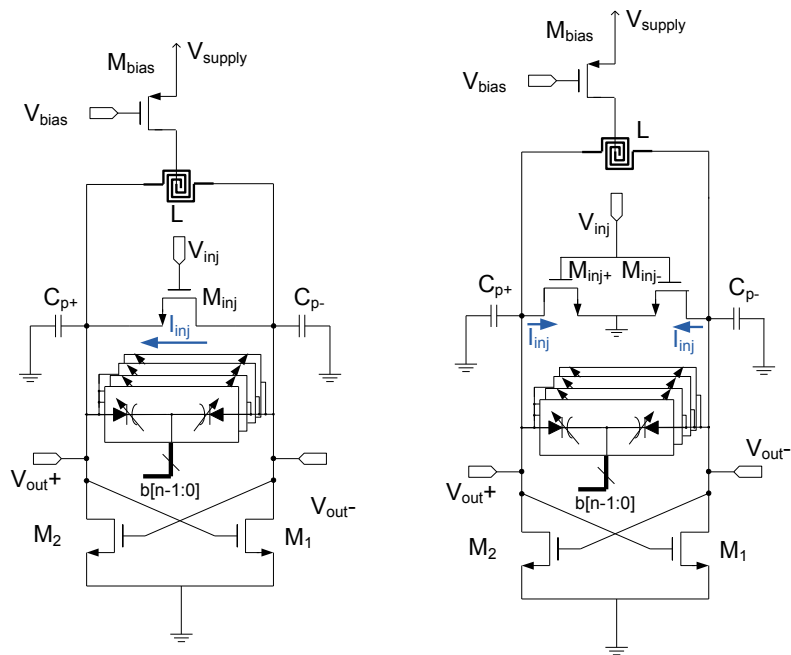
Figure 114: ILFDs discrete tuned: conventional direct injection (left), dual-mixing injection (right)

If the circuits of Figure 114 are sized so that $W_{inj+}/L = W_{inj-}/L = 2 \cdot (W_{inj}/L)$, the capacitive contributions of the injection transistors to both tanks, that are named direct-conventional and dual mixing ILFD, respectively, is the same, as demonstrated in [8]. However, the locking range, from (1) and (2), is doubled in the dual-mixing ILFD at the same parasitic capacitance level than the conventional direct-injection, since the injection current is doubled, as Figure 115 shows. In that figure a simplified block diagram of the dual mixing circuit of Figure 114 (right) is depicted together with the small-signal circuit of the transconductance NMOS mixer corresponding to a single path.
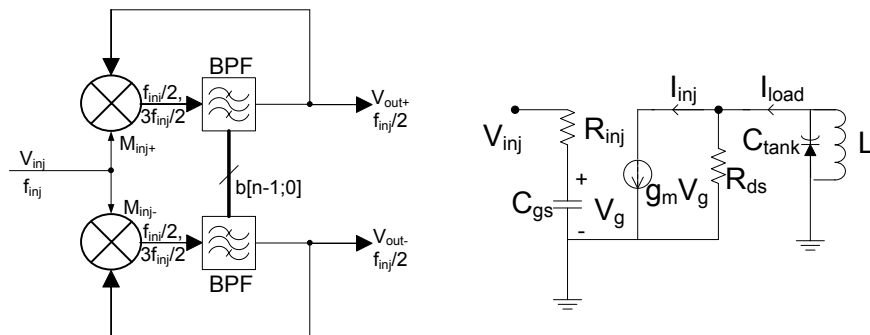
Figure 115: Dual-mixing ILFD block diagram (left); small signal circuit (right)

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In other words, the effective g_m of the resulting mixer formed by M_{inj+} and M_{inj-} has doubled compared to the g_m of M_{inj} in the conventional direct-injection ILFD, while the parasitic capacitive contribute is the same. Therefore, smaller injection transistors can be implemented with the dual-mixing injection scheme, ensuring lower extra tank capacitance, with the advantage of wide locking range, without adding series peacking inductors (that result in an increase of chip area).

As Figure 115 (left) illustrates, the injection signal $V_{inj}(t)=V_{inj}\cdot\sin(2\pi f_{in}\cdot t)$ is mixed in two paths with the divide-by-two ILFD output signals, V_{out+} and V_{out-}, that are exactly at $f_0=f_{in}/2$ in locking state. The mixer output signals, consisting of frequency components at $f_{in}/2$ and $3f_{in}/2$ after mixing operation, is then filtered by the discrete tuned band-pass filter, in order to get ILFD output signals at $f_{in}/2$. Transistors M_{inj+} and M_{inj-} are active drain-pumped mixers, due to the dc voltage $V_{ds}\neq0$ and it gives a further enhance of g_m of the injections transistors [9].

In locking state, where $\omega_0 = \omega_{in}/2$, Figure 115 (right) illustrates how the output load current $I_{load}(t,\omega_0)$ from M_{inj} drain to the LC ILFD tank, that is the injection current, assuming an ideal filtering of all frequency components except f_0, can be expressed as:

$$I_{load}\left(t,\omega_0\right) = g_{m(1),M_{inj}}\left(t\right)\times k\frac{R_{ds}\cdot V_{inj}}{R_{ds}+\left|Z_L\left(j\omega_0\right)\right|} \tag{20}$$

where $g_{m(1),M_{inj}}(t)$ is the fundamental component of $g_{m,M_{inj}}(t)$. It is calculated by the corresponding term of the Fourier series expansion as $(\sigma/2)\cdot g_{m(1),M_{inj},max}\cdot\cos(2\pi f_0\cdot t)$, where $g_{m(1),M_{inj},max}$ is the peack value of $g_{m(1),M_{inj}}(t)$ and σ is a coefficient depending on the DC voltage V_{ds}; k is the factor that relates $V_{inj}(t)$ to $V_g(t)$, such that $V_g(t) = k\cdot V_{inj}(t)$, while $\left|Z_L(j\omega_0)\right|$ is the tuned load impedance equal to $\left|\omega_0 L/(1-\omega_0^2\cdot LC_{tank})\right|$, where C_{tank} depends on b[n-1:0].

As a summary, the objective of the discrete-tuned divide-by-two ILFD design with dual-mixing technique is achieving a wide locking range, taking advantages of an optimized injection scheme, which is more efficient if compared to the conventional (through the bias current transistor) and conventional-direct injection mechanism. This optimized injection scheme is combined with a higher as possible Q tank, without extremely degrading the locking range, in order to ensure low power consumption. In this way, a higher ILFD sensitivity is expected inside the band of interest.

5.4.1 Circuit Level Analysis of the Inductor

The design of the final ILFD circuit starts from the selection of the inductor. As a consequence of the previous designs, the inductor will be sized in

order to achieve high inductance at 30 GHz. In this way the capacitive contribution of the varactors bank to the tank is reduced, which results in an increased locking range according to (18). Note that the dual mixing injection scheme adds an additional capacitance to the ILFD tank, proportional to injection transistors width that needs to be taken into account as well. Furthermore, for the dual-mixing ILFD design the control bits will be reduced to three, since from the previous results it can be concluded that eight wide input sensitivity curves are enough to achieve an overall wide tuned ILFD locking range to cover the WirelessHD[TM] band with an additional band extension for PVT compensation. In addition, lower varactors bank capacitance leads to smaller tank losses allowing to obtain an overall lower power consumption. The selected inductor characteristics are shown in Figure 116. The test bench used to obtain such results is the same of Figure 44, where an S-parameters simulation is performed to get the inductor characteristics.
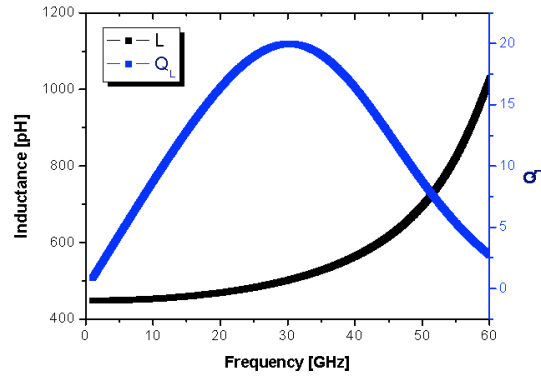
Figure 116: Inductance and inductor quality factor for dual-mixing ILFD

A ≈ 500 pH inductance at 30 GHz is achieved with a 5.5 μm metal width with 171.66 μm of inductor diameter. The inductor quality factor is around 19, which peaks in the middle of the divided-by-two WirelessHD[TM] band, as can be observed in the figure.

Table 5 reports the tank capacitance, calculated by using (12) and (13), required to resonate out the selected inductor. Those values are used to design and size the varactors bank, in order to achieve the specified minimum and maximum ILFD self-resonance frequencies f_{min} and f_{max}, respectively.

	f_{min} [GHz] / C_{max} [fF]	f_{max} [GHz] / C_{min} [fF]
Extended- WirelessHD[TM] (PVT)	28 / 67.9	33.5 / 44.3

Table 5: Tank capacitance calculus for dual-mixing ILFD tank

Since lower and upper frequency bands are available for division-by-two below and above each one of the discrete tuned ILFD self-resonance frequencies, it is not useful to set f_{min} and f_{max} too much far away from 57/2 GHz and 64/2 GHz, respectively. This design strategy leads to sizing a varactors bank where the discrete capacitance variation has a lower step if compared to the previous designs and it allows to reduce the power consumption since the resulting unit varactor cell is smaller, which results in decreasing the overall tank losses.

5.4.2   3-bit Varactors Bank Design

In the following Figure 117, the test bench circuit for the S-parameters simulation of the 3-bit digitally controlled, binary scaled varactors bank, is shown. A unit cell cpo18nw_atto N^{+}poly/Nwell varactor, constituted of a 4x4 array with small width and length (W = 0.5 µm and L = 0.175 µm) is sized in order to maximize the varactors bank quality factor (Q_C). In this way, high ILFD tank losses are avoided, reflecting in an overall ILFD low power consumption. In the circuit of Figure 117 V_{DC} is set to 750 mV, in order to centre the varactors bank capacitance change between b[2:0] = 011 and b[2:0] = 100.
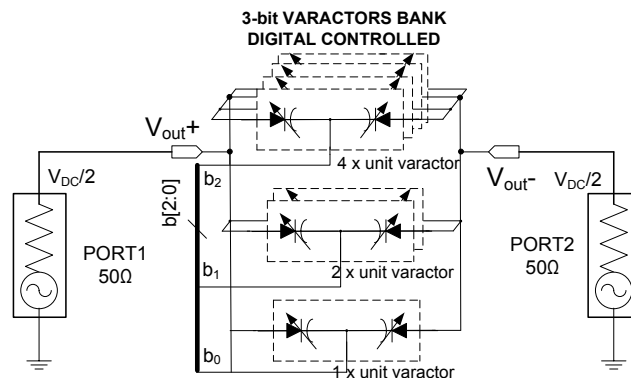
Figure 117: Schematic circuit for 3-bit varactors bank used for S-parameters simulation

Figure 118 illustrates the results of 3-bit digitally controlled varactors bank simulation. Due to higher parallel equivalent losses, Q_C is high if compared to the previous designs. From (19) and Figure 116, the overall contribute to Q_T is practically equally distributed between Q_C and Q_L at lower frequency end, corresponding to b[2:0] = 000, while at the higher frequency end, corresponding to b[2:0] = 111, the contribute of Q_C to Q_T is reduced to approximately a 16%. On the other hand, in order to achieve the required minimum and maximum varactors bank capacitance, an additional capacitive contribution needs to be considered. It is provided by the dual-mixing injection stage plus a fixed

capacitance C_F that takes account the contribution of the cross coupled transistors, input buffers and layout interconnections.
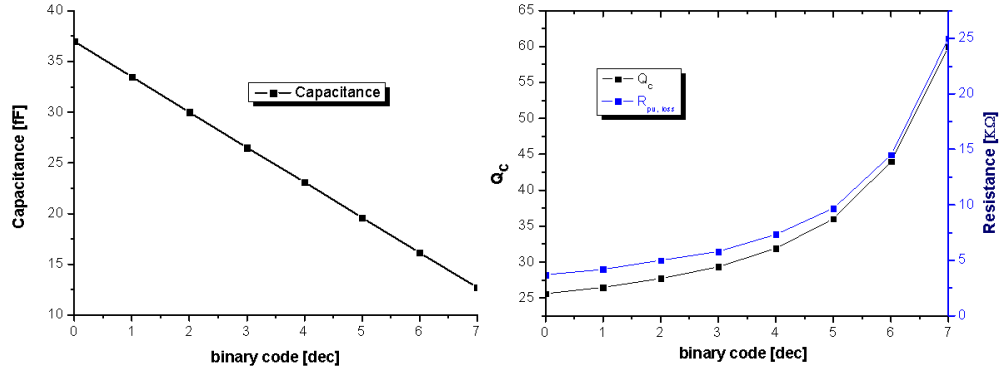
Figure 118: 3-bit varactors bank for dual mixing ILFD. Capacitance (left); quality factor and parallel equivalent losses (right)

5.4.3   3-bit Tank Bank Design

Before simulating the complete ILFD tank for the dual-mixing ILFD design, a DC simulation of the mixing transistor is reported , in order to evaluate the DC g_m and the impact of its sizing in the power consumption. For this analysis the DC drain voltage V_{ds} is set to the DC ILFD output voltage level expected, that is 750mV. This value, along with the V_{gs} and the NMOS transistor width, set the current consumption of the injection stage. The simulation results for a wide range of NMOSs widths and DC V_{gs} bias voltages are shown in Figure 119.
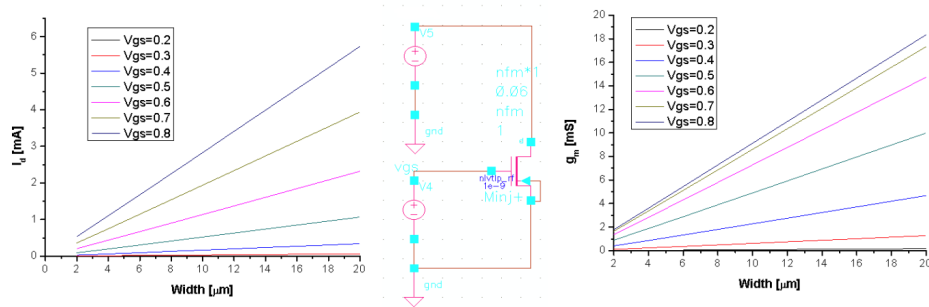
Figure 119: Injection transistor: DC current (left); g_m (right)

Next Figure 120 is the test bench circuit used for the dual mixing, 3-bit discrete tuned 60 GHz divide-by-two ILFD tank simulation, where the injection transistors M_{inj+} and M_{inj-} are included:

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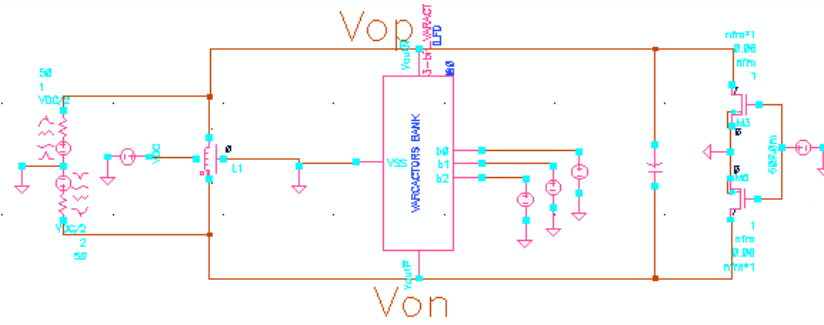
Figure 120: Dual-mixing ILFD tank schematic circuit

In order to keep the minimum ILFD self-resonance frequency to 27.5 GHz, the impact of M_{inj+} and M_{inj+} sizing must be carefully taken into account. From (13), the values of the differential fixed capacitance C_F corresponding to different injection transistors width W_{inj} is calculated, for a fixed DC bias voltage of the dual mixing NMOSs $V_{biasInj}$, that is V_{gs}, set to 600mV. The results of these calculations are plotted in Figure 121. As expected, C_F decreases as W_{inj} increases. This effect is more important as $V_{biasInj}$ becomes higher.
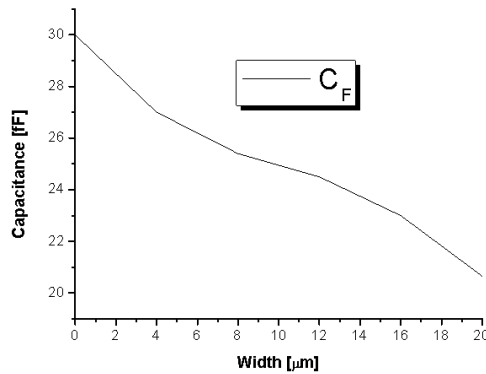
Figure 121: Tank fixed-capacitance as a function of W_{inj}

Figure 122 illustrates the ILFD tank resonance frequencies and tank parallel equivalent losses $R_{p,eq}$ corresponding to different injection transistors widths. The values of C_F are set accordingly to each W_{inj} used, in order to compensate the capacitive contribute of M_{inj+} and M_{inj-}, in order to keep the same tank resonance frequencies for each simulation cycle. Wider W_{inj} results in lower $R_{p,eq}$, resulting in higher tank losses. A W_{inj} = 16 µm, corresponding to 1 µm x 16 fingers NMOS, is selected with minimum channel length (i. e. 60 nm). This values ensures a fixed capacitance budget, in the tank circuit of Figure 120, around 23 fF. Considering a $V_{biasInj}$ = 600 mV, the current consumption per

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injection transistor is set to 1.85 mA, according to the simulation results reported in Figure 119.
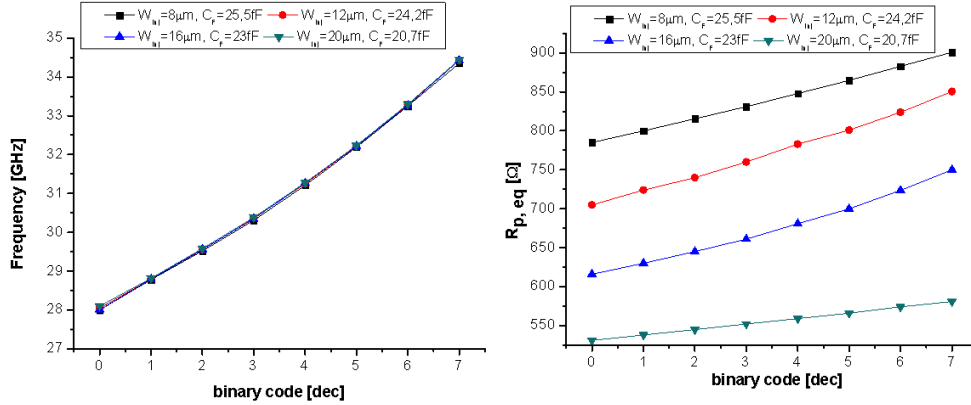
Figure 122: Tank resonance frequencies (left); parallel equivalent losses (right)

The lowest value of $R_{p,eq}$ for a $W_{inj} = W_{inj+} = W_{inj-} = 16$ µm, sets the required NMOSs cross coupled pair transconductance $g_{m,CC}$ to 3.25 mS, according to (15). Taking into account a security margin for robust and reliable start-up oscillation at low frequencies, the goal is a $g_{m,CC} \geq 6.5$ mS.

There is a trade-off between W_{inj} and $V_{biasInj}$ with ILO tuning range and ILFD locking range in dual mixing architecture: lower W_{inj} and $V_{biasInj}$ result in higher frequency operation range, since the ILO output capacitive load is lower. On the other hand, higher $V_{biasInj}$ and W_{inj} lead to higher ILFD locking range, according to (1) and (2), but $V_{biasInj}$ and mostly W_{inj} cannot be extremely increased, mainly due to injected signal degradation, since C_{p-} and C_{p+} are higher and also due to the already mentioned ILO tuning range reduction.

5.4.4   Dual-Mixing Discrete Tuned Free-Run ILO

For the rest of this work, the topology that is kept is the dual-mixing ILFD. In order to extend the dividing range of this circuit, a discrete tuning capability for the divider self-oscillation frequency is implemented. In Figure 123 a 3-bit dual-mixing discrete tuned ILO is shown. The NMOSs cross-coupled pair is sized in order to get the g_m required to achieve start-up oscillation at the selected ILFD $V_{DC,out}$ (750mV). The transistor width is set to $W_{CC} = 8$ µm, corresponding to 8 fingers NMOS where each finger has 1 µm width. As usual, the NMOSs have minimum channel length. The PMOS transistor is then sized (W = 300 µm, L = 140 nm) to provide the ILO with the required DC current. The two injecting transistors have $W_{inj} = 16$ µm, as derived from the analysis in the previous sub-section.
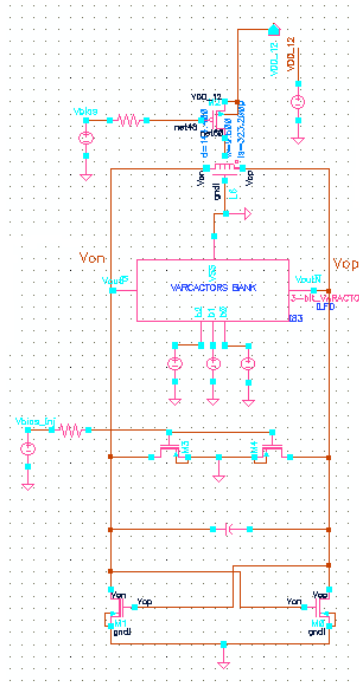
Figure 123: 3-bit discrete tuned dual-mixing ILO

The DC simulation results parameters for the circuit of Figure 123 are::

- V_{bias} = 850 mV

- $V_{DC,out}$ = 752 mV

- $g_{m,CC}$ = 7.35 mS

- I_{dc} =8.4 mA

- V_{supply} = 1.2V

The specified value of f_{min} in Table 5 is slightly modified down to 27.5 GHz and, consequently, C_F is fine tuned (C_F = 17.4 fF) in order to achieve the specification, taking into account the insertion of the NMOSs cross coupled pair. The resulting ILFD self-resonance frequencies are reported in the following Figure 124 (left). Note that at least four input sensitivity curves, that are the two lower and two upper, would be centred outside the band of interest, but they are available for PVT compensation, while the remaining four curves, which would be centred around the four remaining self-resonance frequencies, would be inside the band of interest. The ILFD phase noise is reported in Figure 124 (right). It is not a key parameter in ILFD design, mostly because the phase noise in a PLL is dictated by the VCO, as it will be illustrated in Chapter 6 and 7.

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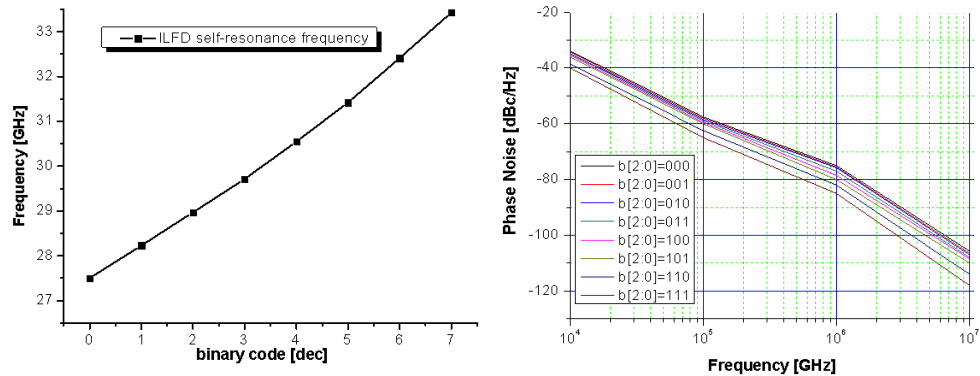
Figure 124: 3-bit dual mixing ILFD self-resonance frequencies (left); Phase Noise (right)

Figure 122 shows the ILFD output waveforms, corresponding to V_{op} and V_{on}, single-ended output, for all the eight binary codes when the ILFD is self-oscillating:
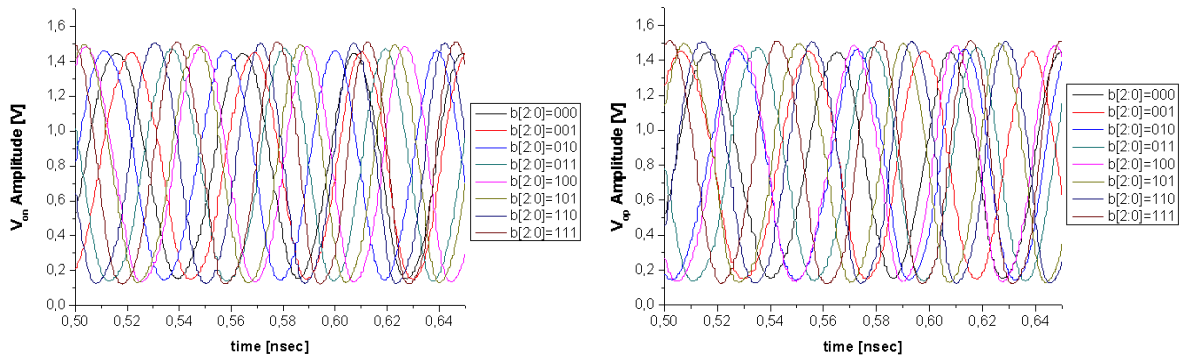
Figure 125: ILFD output waveforms in self-oscillation

5.4.5   Input Sensitivity Curves

Figure 126 reports the schematic circuit of the 3-bit discrete tuning dual-mixing divide-by-two ILFD. The only change introduced here from the circuit of Figure 123 is that an injection path is added by connecting the external mm-W input source to the common gate of the dual mixing transistors. A large decoupling capacitor C_{dec} (C = 10 pF) is used to block the DC component and prevent it reaches the input source. A high value poly-silicon resistor is inserted in the bias path of the injection transistors, between the bias source and the dual-mixing transistors gates, to choke the RF input and prevent it reaches the biasing circuit, forcing it to be injected into the ILFD tank.

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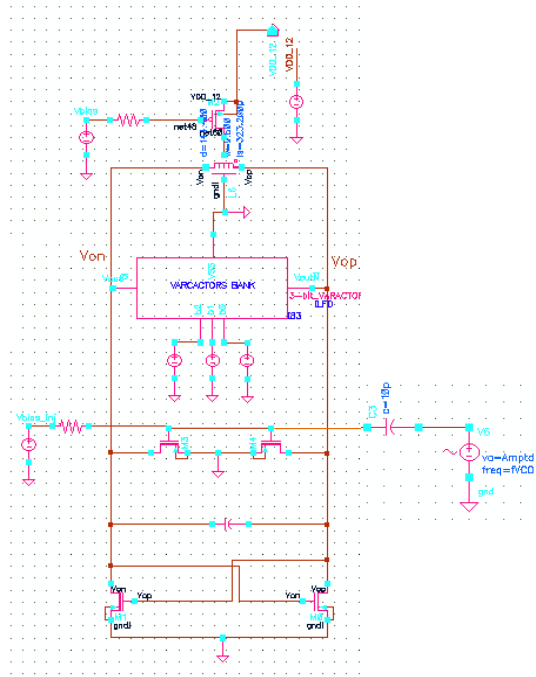
Figure 126: 3-bit discrete tuned dual-mixing divide-by-two ILFD

In the same way as that presented in 5.2.5, the ILFD input sensitivity curves are obtained and plotted in Figure 127. Since the ILFD has discrete tuning capability provided by a 3-bit digitally controlled varactors bank, there are eight sensitivity curves, corresponding to the eight binary codes b[2:0].
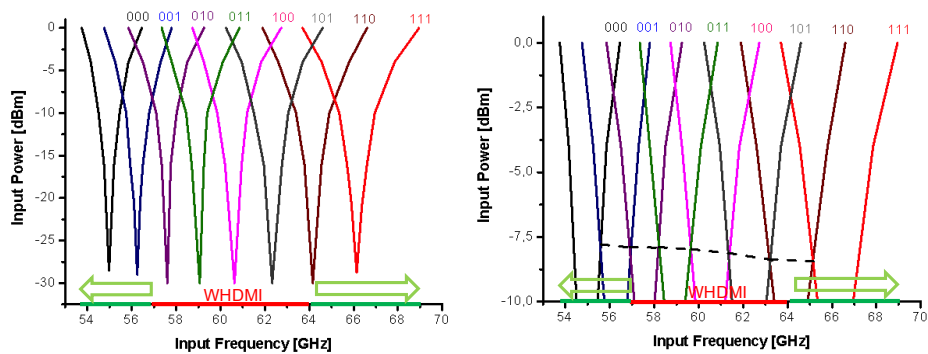
Figure 127: 3-bit discrete tuned dual-mixing divide-by-two ILFD input sensitivity curves (left). Detail for high input frequency (right)

The achieved ILFD total dividing range, with tuning mechanism, for 0 dBm input power is around 24.7%, from 53.75 GHz to 68.95 GHz. The locking range at 0 dBm of the single ILFD input sensitivity curves varies from 4.7%,

corresponding to b[2:0] = 000, up to ≈ 8%, for that corresponding to b[2:0] = 111. As it is possible to observe from the right plot of Figure 127, the dual-mixing discrete tuned divide-by-two ILFD input sensitivity curves intersections occur for an input power level ≤ -7.5 dBm. That is, the ILFD tuned dividing range at -7.5 dBm input power is around 21.7%, corresponding to input frequencies from 54.25 GHz up to 67.5 GHz. This results in a very high sensitive, wide dividing range ILFD for WirelessHD[TM] applications.

A further analysis of the curves in Figure 127 reveals that from approximately 56 GHz to 65 GHz the same frequency can be tracked, that is divided, by three different ILFD binary codes. This is illustrated in Figure 128, for an input signal at 62 GHz with an amplitude of 300 mV, that is ≈ 0 dBm. The ILFD output frequency locks always at 31 GHz, for three different ILFD binary codes. Before the input signal is injected into the ILFD, it is oscillating at its self-oscillating frequency, corresponding to the three binary codes b[2:0]. After 2 nsec the input signal is injected and the ILFD sets its output frequency exactly at 31 GHz.
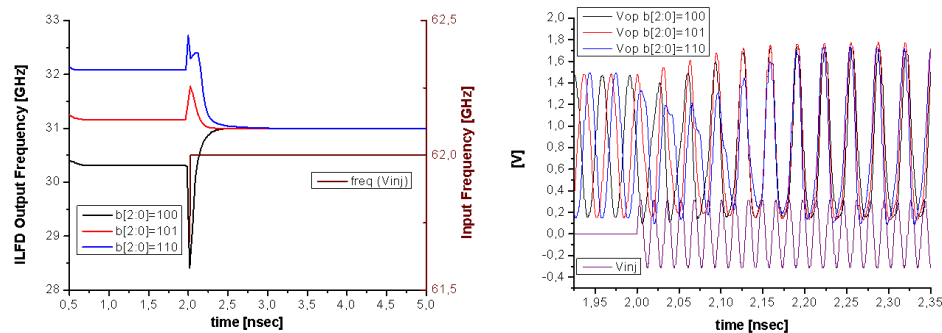
Figure 128: ILFD locking for three different binary codes

5.4.6   Conclusions

In the previous sub-section it has been shown that the direct-injection topology with dual-mixing scheme maximizes the ILFD locking range due to an improved injection scheme which allows optimizing, as it has been demonstrated by comparing the locking range of the single ILFD sensitivity curve with the other topologies presented in the previous sub-sections. In addition, a digitally controlled varactors bank provides discrete tuning for ILFD wide-band operation around the WirelessHD[TM] band, as illustrated in Figure 127 where the extended bands for PVT calibrations are also indicated.

In order to analyze quantitatively what is improving the ILFD locking range, the ILFD currents are considered when the ILFD is locked. In Figure 129

(left) the currents of dual-mixing transistors M_{inj+} and M_{inj-} are plotted. In the same graph, the injection currents, i. e. the current available inside the tank and the one that is delivered by the source, are also shown. In Figure 129 (right) the DFTs of the time domain waveforms are calculated and depicted. The ILFD is locked in this case for a 0 dBm input signal at 60.3 GHz, with control binary code b[2:0] = 101.
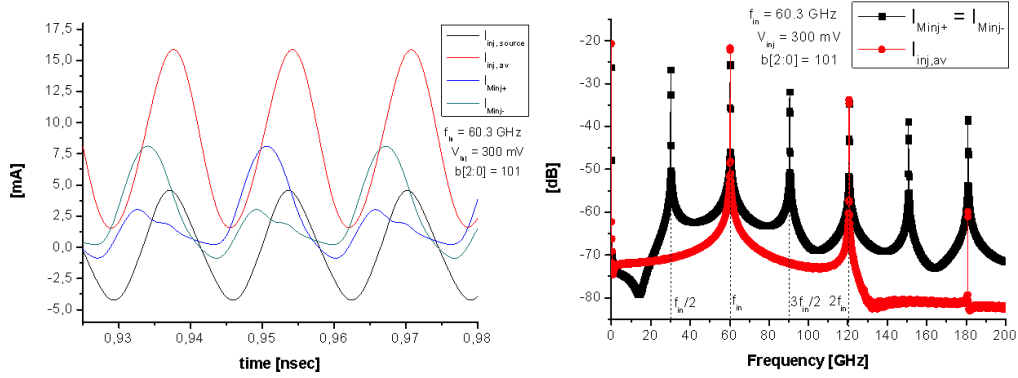
Figure 129: ILFD currents in locking state: f_{in}=60.3 GHz

From the circuit of Figure 114 (right), $I_{inj,av}$ is the available ILFD injection current flowing in the inductor central tap, such that $I_{inj,av} = 2 \cdot I_{Minj}$. I_{Minj} is the dual-mixing transistor drain current and from the schematic in Figure 115 (right) can be expressed as:

$$I_{M_{inj}} = I_{M_{inj+}} = I_{M_{inj-}} = g_{m(1),M_{inj}}(t) \cdot V_g(t) \tag{21}$$

The combination of the dual-mixing transistors drain currents performs a frequency cancellation of the components at $f_{in}/2$ and $3f_{in}/2$, as Figure 129 (right) illustrates. The resulting $I_{inj,av}$ is the effective current injected into the ILFD tank.

Figure 130 shows the current gain $I_{inj,av}/I_{inj,source}$ corresponding to the ILFD locking state just described: it is possible to note the improvement achieved with the presented injection scheme if compared to the current gains of the conventional injection topology already reported in the previous sub-sections.

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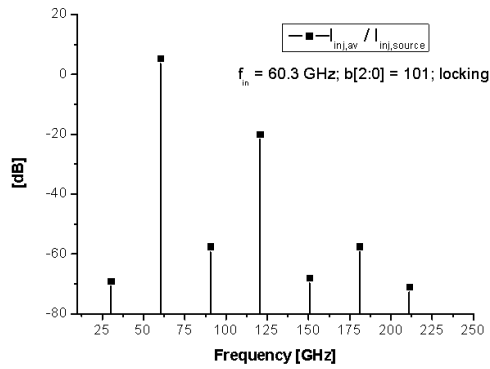
Figure 130: Dual-mixing ILFD: $I_{inj,av}/I_{inj,source}$

As already mentioned, M_{inj+} and M_{inj-} sizing cannot be ever increased in order to improve the ILFD locking range. In Figure 131 the ILFD sensitivity curves corresponding to b[2:0] = 100 are reported considering different dual-mixing transistors width.
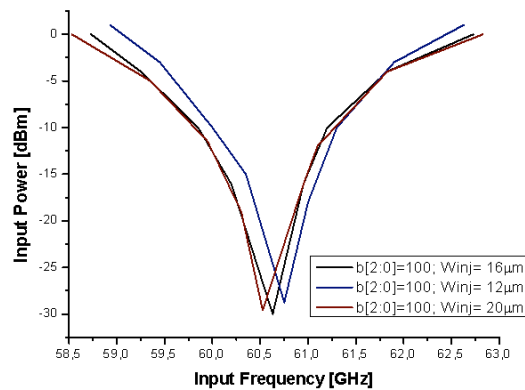
Figure 131: ILFD sensitivity curve (b[2:0]=100) for different injection transistor width

In the analysis shown in Figure 131 only W_{inj} is varying, while the NMOSs cross-coupled pair width is kept constant to 8 µm, although it should be increased in order to ensure robust ILFD start-up oscillation in the case of W_{inj} = 20 µm, as illustrated in the following summary Table 6. What is changing for each case is the C_F value, in order to achieve the same resonance frequency in all the cases.

W_{inj} [µm]	ILFD operation frequency [GHz]	LR at 0 dBm (tuned) %	Intersection (worst-case) [dBm]	ILFD DC V_{out} [V]	ILFD DC Current [mA]	M_{inj} current X2 [mA]	NMOS pair current [mA]	$g_{m,CC}$ [mS]	$g_{m,min,CC}$ [mS]	C_F [fF]
12	54.5-67.6	21.4	-5.2	0.79	8	2.96	5.01	7.5	5.7	21
16	53.75-68.95	24.77	-7.6	0.752	8.3	3.82	4.358	7.35	6.5	17.4
20	53.3-69.45	26.3	-7.9	0.715	8.55	4.71	3.736	7.1	8	14

Table 6: Dual-mixing ILFD parameters for different injection transistors sizing

The DC biasing voltage for the injection transistors is kept constant ($V_{biasInj}$ = 600 mV) for all the three M_{inj} sizings reported, as well as the ILFD bias voltage (V_{bias} = 850mV). As it is possible to observe in Table 6, while the ILFD locking range is wider for W_{inj} = 20 µm, it is lower for W_{inj} = 12 µm, consistent to the fact that lower injection current is available in the ILFD tank to be tracked. However, the DC current consumption is increased for W_{inj} = 20 µm, due to the higher DC drain current corresponding to larger W_{inj}, taking into account that the DC current biasing the cross-coupled NMOSs is slightly reduced, if compared to W_{inj} = 16 µm, due to approximately 35 mV reduction in the DC ILFD output voltage. Therefore, selecting W_{inj} = 12 µm leads to lower sensitive ILFD, if compared to W_{inj} = 16 µm and W_{inj} = 20 µm, with a lower DC current consumption (anyway just 0.3 mA less if compared to W_{inj} = 16 µm), even if a lower W_{inj} at the same bias voltages, causes higher ILFD DC output voltage, hence higher DC biasing current of the NMOS cross coupled pair. These results are reported above in the table.

On the other hand, with W_{inj} = 20 µm the ILFD achieves 26.3% locking range (it is higher if compared to W_{inj} = 16 µm), at expenses of a higher power consumption. Such result is consistent with the locking range equations (1) and (2), since the injection efficiency is improved by lowering I_{osc} and increasing I_{inj}. Nevertheless for robust circuit design, the NMOSs cross coupled pair width should be increased (at least up to 10 µm) to get a higher $g_{m,CC}$ that assures start-up oscillation at lower ILFD operation frequencies. In facts, in this case a $g_{m,CC}$ of 8 mS is required, $g_{m,min,CC}$ = 4/$R_{pe,worst}$, see Figure 122 (right). It has been verified by simulation that to increasing $g_{m,CC}$ leads to increase the total ILFD current consumption up to 9.5 mA with the disadvantage of a critical reduced budget of fixed capacitance ($C_F \approx$ 10 fF) in order to keep the same ILFD operation frequency band. Furthermore, since higher tank losses are expected due to larger transistors sizes, the injection efficiency is degraded. In addition, the ILFD V_{bias} should be adjusted, in order to keep the ILFD DC output voltage around 750 mV , which causes a total current consumption of 10.6 mA and a further reduced C_F budget. As a consequence of all these modifications,

that are resumed in Table 7, the locking range corresponding to W_{inj} = 20 µm is reduced, if compared to that achieved for the same injection transistor sizing and reported in Table 6. In summary, no actual benefit is expected from increasing the injection transistor width W_{inj} = 16 µm to W_{inj} = 20 µm, once all the implications of such change are considered in the rest of device sizing.

W_{inj} [µm]	W_{cc} [µm]	ILFD operation range [GHz]	LR at 0 dBm (tuned) %	Intersection (higher) [dBm]	ILFD DC V_{out} [V]	ILFD DC Current [mA]	M_{inj} current x2 [mA]	NMOS pair current x2 [mA]	V_{bias} [mV]	C_F [fF]
20	10	53.5-69	25.3	-7.7	0.75	**10.6**	4.88	5.6	800	9
16	8	53.75-68.95	24.77	-7.6	0.752	8.3	3.86	4.358	850	17.4

Table 7: Comparison between dual-mixing ILFD designs for different injection transistors sizing

Therefore, W_{inj} cannot be arbitrarily increased in order to enhance the injection transistor transconductance $g_{m,Minj}$ to maximize the injection current. A limit for its maximum value exists that is set by the ILFD operation frequency. In addition, the effective $g_{m,Minj}$ should be considered. Furthermore, increasing the injection transistors size in dual-mixing ILFD leads to carefully consider the required $g_{m,CC}$ for start-up oscillation and it results in a NMOSs cross-coupled pair re-sizing. This reflects the compromise between the injection efficiency and the ILFD overall power consumption. Furthermore, larger injection transistor widths reduce the budget of fixed capacitance, that is intended to anticipate layout interconnections, output buffers loading, etc. If this budget approaches zero, or reaches a negative value, it means that no layout solution would exist.

Finally, increasing $V_{biasInj}$ to improve the injection efficiency is not a good strategy since as reported in Figure 119. It leads to a significant $g_{m,Minj}$ increase, which translates into higher ILFD current consumption, causing critical added capacitive load and reducing the ILFD operation band. This consideration is under the assumption that V_{bias} should be re-adjusted to keep the ILFD DC output voltage to 750 mV (which is the optimum biasing point to maximize the varactors capacitance change). These considerations lead to select a compromise value W_{inj} = 16 um that completes the ILFD core design at circuit level.

The achieved ILFD dividing range, taking into account the discrete tuning mechanism, for 0 dBm input power results in a 24.7%, i. e. for input frequencies from 53.7 to 68.95 GHz, while for - 7.5 dBm input power it is still greater than 20%, allowing its implementation, together with the 60 GHz VCO, in high precision PLL direct conversion transceiver for 60 GHz applications.

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6 EM SIMULATIONS - OUTPUT BUFFERS DESIGN - LAYOUT

In this chapter the layout of the whole test chip, i. e. the 60 GHz VCO and ILFD designed at circuit level in the previous chapters, is carried out. Note that a 65 nm CMOS process offering 7 layers of Cu metallization is used. The two upper layers (M6 and M7) are thick metal layers and allow the implementation of good passive structures such as inductors and TLs, that are fundamental for mm-W ICs. EM simulations of the critical parts of the layout are performed. As already mentioned, EM simulations are a critical process inside the design flow in a mm-W IC design mainly for two reasons: first because the accuracy of the models provided by the foundry should be contrasted with the results of the simulations including the EM extracted models, taking into account that the models for simulations provided by the foundry are certified only up 40 GHz. Second, EM simulations are time hungry so that they have a critical impact in the IC design flow.

This chapter stars with the EM characterization of the two inductors used in the design process presented in the previous chapters: the VCO and ILFD inductors. Then, the layouts of the cores of both ILFD and VCO circuits are built. In this stage the S-parameters of the layout interconnections are extracted in order to account for their parasitics in the post-layout simulations of the design. Going on, a preliminary floor-plan of the chip to be manufactured is done in order to place the needed PADs and to consider the available area in the chip in order to design and implement at layout level the output buffers for connecting the outputs of both the VCO and ILFD to external 50Ω loads (i.e. the measuring equipment). In other words, in the current design phase schematic and layout should go hand by hand (it is no strategically feasible designing the output buffer without taking into account its placement in the layout, as it is shown in this chapter). Indeed, the placement of the TLs used in the output buffers is strictly linked to the layout disposition, conditioning their routing.

TLs with electrical length equal to λ/4 at the frequencies of interest (60 GHz for the VCO and 30 GHz for the ILFD) are going to occupy a significant surface in the layout. They are used to provide the output buffers with voltage supply and biasing voltage to the ILFD input stage (in this case the TL would be λ/4 at 60 GHz).

Due to manufacturing cost constraints, the area limit for the chip is 1 mm^2. It is clear that this limit set a critical point for the λ/4 TLs routing, mostly for the ILFD, since λ/4 at 30 GHz is ≈ 1.2 mm. Therefore EM simulations are essential in order to design the proper TL with the required electrical length.

The layout is then completed by adding control lines and decoupling capacitors with ad-hoc self-built structures that are exposed later.

Finally, some post-layout simulations are performed, taking into account the measurements that are performed and shown in Chapter 8 with the delivered test chip.

6.1 VCO and ILFD Cores Layout

6.1.1 Inductors

Figure 132 shows the 3D view of the VCO and ILFD inductors that have been selected and simulated at circuit level in sections 4.2 and 5.4.1, respectively. Edge ports for Momentum [1] EM simulations are placed in order to extract a 4-ports model for each inductor, based on S-parameters.
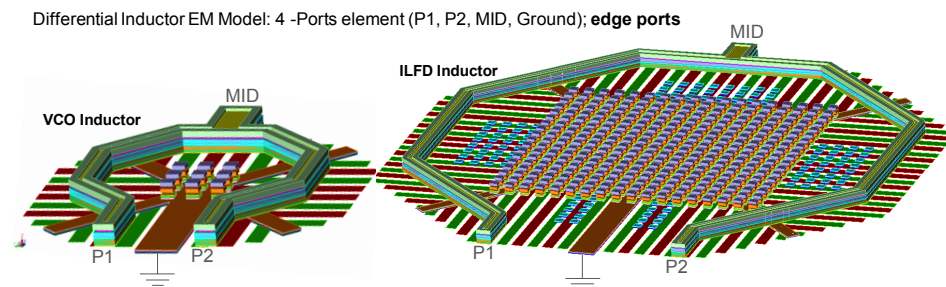
Figure 132: 3D view of VCO inductor (left) and ILFD inductor (right) for EM simulation

The 4-ports extracted model to include in the simulations at circuit level is shown in Figure 133.
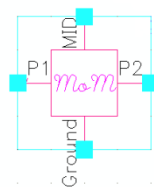
Figure 133: Momentum extracted model for inductor

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Figure 134 shows the test bench circuit used for inductors characterization with ADS [2].
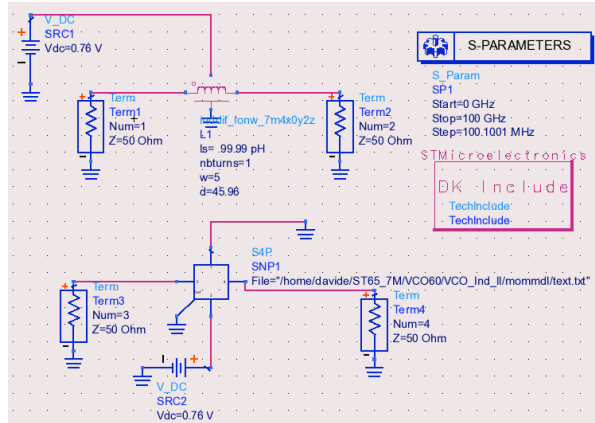
Figure 134: Test bench circuit for inductors with ADS

In the test bench the electrical parameters (inductance, quality factor, etc) of the inductor model provided in the Design Kit library (*L DK*) are extracted in the same conditions that the EM model of the same inductor obtained in the previous step (*L mom*). The results of this comparison is shown in Figure 135, which reports the results for the VCO inductor, while Figure 136 shows the results related to the ILFD inductor.
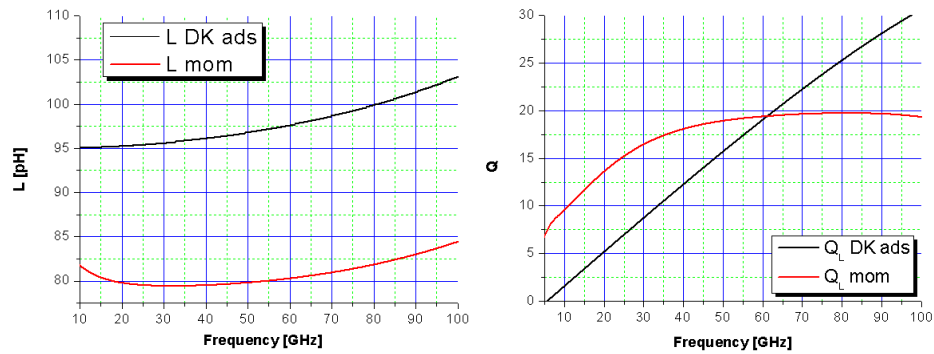
Figure 135: VCO differential inductor: inductance (left); quality factor (right)
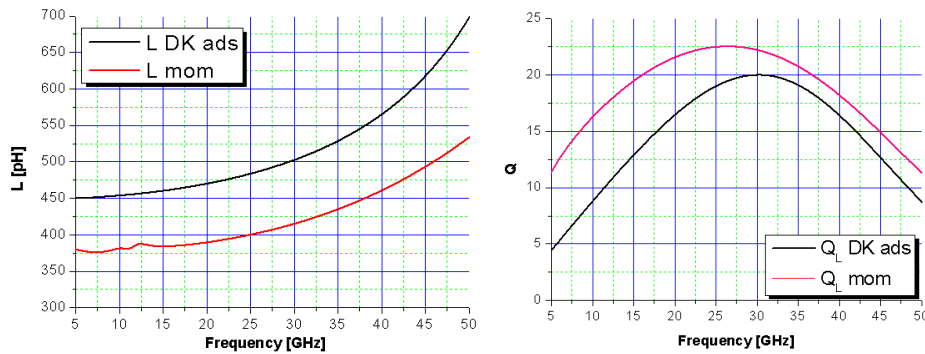
Figure 136: ILFD differential inductor: inductance (left); quality factor (right)

The first consideration follows: the results of the inductors simulation considering the DK models with ADS is basically the same as those obtained with SpectreRF (see for comparison Figure 45 and Figure 116).

The substrate needed to run the EM simulation has been provided directly by the foundry and the results corresponding to the corner TYP of the substrate are plotted in the Figure 135 and Figure 136. Very small variations are found if the other provided substrate corners (MIN and MAX) are used, i. e. less than 3%, in the case of inductance, and 10% for the inductor quality factor. Nevertheless, the results of EM simulation show that at 60 GHz a difference of ≈ 16.5 pH (corresponding to ≈ 17%) is found between the VCO inductance value calculated with the DK model and the value extracted from the EM simulation. In the case of the ILFD inductor, its inductance at 30 GHz shows a difference of ≈ 86 pH (corresponding also here to ≈ 17%) between the extracted model from the EM simulation and the DK model for the same component.

These differences are significant and should be taken into account. Since the accuracy of the inductors from the DK library is, according to the foundry, qualified up to 40 GHz for passive devices, at mm-W, the EM models should be indeed more accurate and those are the models used in the rest of the design process.

6.1.2   VCO Core

Once that the inductors have been characterized using an EM analysis, it is time to start the layout of the active area of the 60 GHz VCO. The active area includes the cross-coupled NMOSs, the varactors bank and the fine tuning varactor.

The VCO 4-bits digitally controlled binary scaled varactors bank for coarse tuning, which is composed by fifteen varactors equally sized (see section

4.3.2) is implemented at layout level using a "centroid" structure with dummies, where the unit varactor controlled by the LSB, i. e. b_0, is placed at the centre of the structure, as shown in Figure 137, and marked with a black square. This structure has been implemented in order to get, as maximum as possible, a complete symmetry. The two varactors controlled by b_1 are marked with red squares, while the four varactors controlled by b2 are marked with violet squares. The eight varactors controlled by the MSB b3 are marked with orange square. The rest of varactors are floating and they constitute dummies to achieve symmetry and the same spatial environment for all the useful varactors.
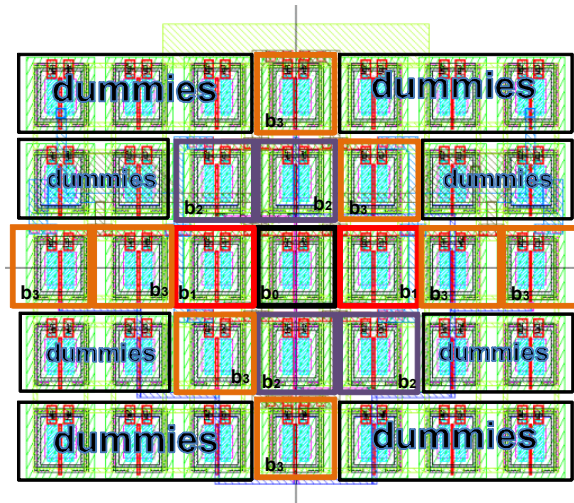
Figure 137: VCO 4-bit varactors bank

The NMOSs cross-coupled pair is implemented inside a deep-Nwell, as shown in Figure 138 (left) where only one transistor of the pair is depicted. This is done for reducing substrate coupling and to provide a ground signal through a proper transmission line in order to implement the previously described filter for phase noise optimization. Such implementation results in the formation of Nwell to substrate N diodes, which are shown in Figure 138 (right), corresponding to both NMOSs. The diodes should be added to the schematic for Layout Versus Schematic (LVS) comparison. The presence of the diodes should be taken into account in the circuit simulation as well.
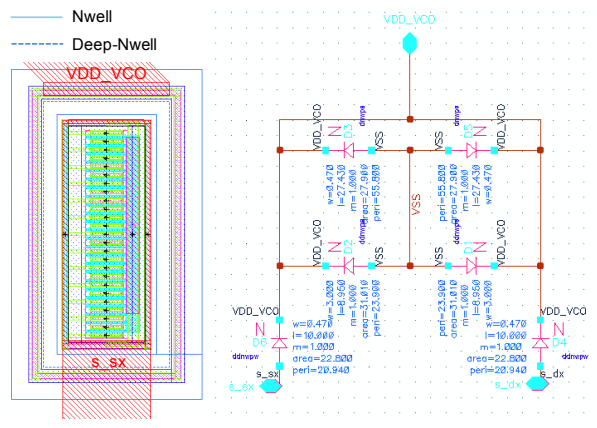
Figure 138: NMOS layout in deep-Nwell (left); schematic of resulting N diodes

In next Figure 139, the 3D view of the VCO active area layout interconnections for EM simulation is shown. It is analysed by a mix of edge and point type ports. The point ports are indicated as a black circle and in these points the fingers of the varactors (at M5 layer) are connected to the rest of the circuit according to the schematic of Figure 43. V_{op} and V_{on} are the edge ports connecting to the differential inductor.
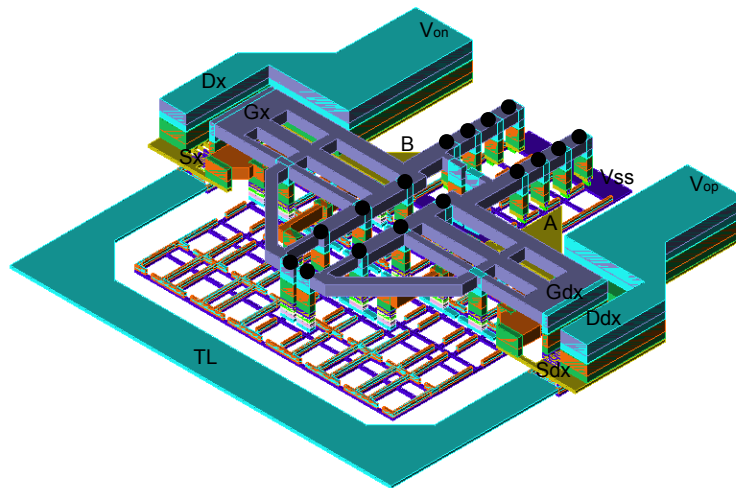
Figure 139: VCO active area layout interconnection

The ground plane of the VCO core is composed by M1 plus M2 layers. Two metal layers are used in order to reduce losses, increasing the conductivity of the resulting ground plane.

In order to reduce simulation time during the EM extraction, contacts and vias simplifications are performed, treating them as stacked conductors. That is, the arrays of contacts used to connect locally M1 with Poly and active layers are merged in a single contact, and the same process is done for vias VIA6 to VIA1. The size of this simplified vias is slightly enlarged compared to the original size of the array to stack M7 - M6 together, in the case of VIA6, for example, M2 - M1 together for VIA1, and going on for the rest of vias (VIA5, VIA4, VIA3 and VIA2). Figure 140 shows the Momentum dialog window that details the options used to perform vias and contacts simplification. The same simplification criteria has been adopted for the inductor models extraction exposed in the previous sub-section 6.1.1.
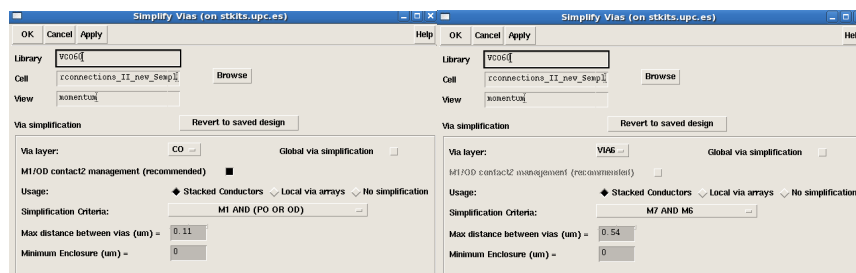
Figure 140: Momentum Vias and Contacts simplifications

Next Figure 141 shows the VCO schematic circuit and the VCO core layout. In the schematic the S-parameters models extracted from EM simulation for the inductor and interconnections structure previously described are included as symbols.
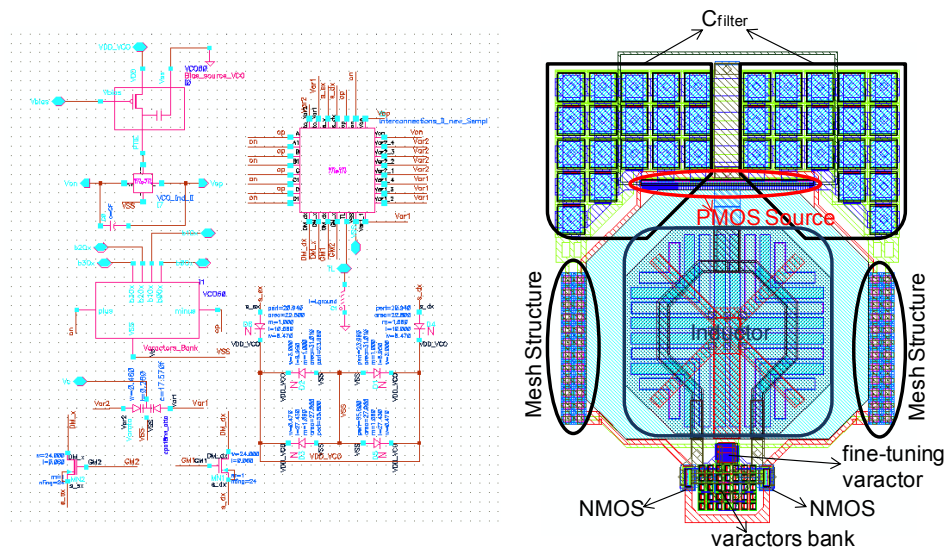
Figure 141: VCO core schematic including EM extracted models (left). VCO core layout (right)

The bias current source is composed by the PMOS and the 50 pF filter capacitor C_{filter}. Such capacitance is implemented with a matrix of 36 parallel NMOSs in which the bulk, drain and source terminals are connected together to the ground plane. The single NMOS transistor width and length are 10.5 μm and 10.5 μm, respectively.

In Figure 141 (right) it is possible to note two areas indicated as Mesh Structure, which is an array of a unit cell used to carry a DC voltage in different layout areas ensuring at the same time the continuity of the ground plane. This structure also provides some local decoupling capacitance between the carried signal and ground in the form of metal-to-metal capacitance. Figure 142 shows a 3D view of the unit cell named *Mesh Single* which has been used to form the arrays indicated in Figure 141, in order to provide the Nwell areas with 1.2V voltage supply.
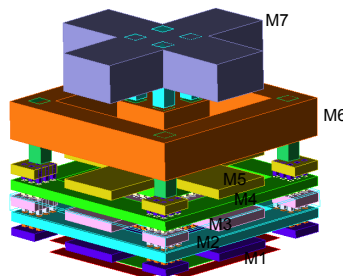
Figure 142: Mesh Single 3D view

The 5 μm x 5 μm unit cell *Mesh Single* of Figure 142 is a superposition of ring and cross structures that complies with density rules and allows to distribute two signals across the surface of the IC adding some de-coupling capacitance between them. The bottom metal M1 is used as ground plane and it is connected to M3, M5 and M7 in the middle of the cell, while M2, M4 and M6 are carrying the DC signal and they are connected throw vias in the corners of the cell. The unit cell *Mesh Single* has been simulated with Momentum and it has a total capacitance between the two signals of around 6 fF. This means that each 12 x 2 array indicated in the layout of Figure 141 (right) provide a decoupling capacitance of 144 fF.

The last design step for the physical implementation of the 60 GHz VCO consists in performing a simulation of the circuit of Figure 141 (left). The simulator used is GoldenGate (GG) with Harmonic Balance (HB) and noise analysis, since SpectreRF shows limits when evaluating autonomous steady-state in high frequency circuits with distributed models. The ideal filter inductor L_{ground} = 165 pH presented in 4.6.1 is still considered to connect the TL terminal in the schematic of Figure 141 (left) to ground.

As a summary, the DC parameters are reported:

- VCO Power Consumption P_{dc} = 15.12 mW

- I_{dc} = 12.6 mA at V_{DD} =1.2V

- V_{bias} = 715 mV

- NMOS transconductance g_m = 22.12 mS

- VCO DC output voltage $V_{DC,out}$ = 0.765V

The layout interconnections adds to the VCO core a differential capacitive load contribution which is estimated in ≈ 13 fF. This is very similar to that one of the final budget found in 4.6.1 for the parasitic capacitance in parallel to the tank. In fact, with a C_F = 0 in the circuit of Figure 141 (right), if the inductance is 97.5 pH, as provided by the DK inductor model, the achieved tuning range is basically the same shown in Figure 73. Nevertheless, since as the result of the EM extraction of the inductor a reduction of ≈ 16.5 pH in its inductance is obtained, in order to keep the same VCO tuning range of Figure 73 the total remaining budget for parasitic capacitance, considering now the loading effect of the interconnections structure abovementioned, is C_F = 14.8 fF. Therefore any other element connected to the output of the VCO core (e.g. the buffers) should not add a parasitic loading effect higher than that C_F. In Figure 143, the results of GG HB and noise simulations of the VCO schematic of Figure 141 (right) are shown.
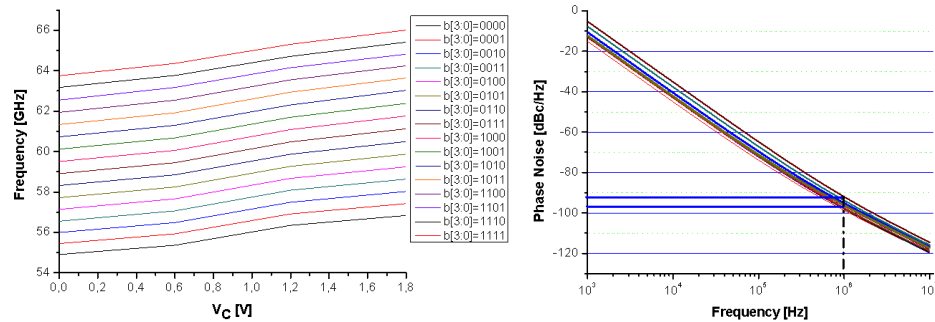
Figure 143: 60 GHz VCO core. Frequency curves (left); Phase Noise (right)

A VCO tuning range, considering both continuous and discrete tuning, of ≈ 20% is achieved, from 53.85 GHz (for b[3:0] = 0000 and Vc=0V) to 66.15 GHz (for b[3:0] = 1111 and Vc=1.8V).

The phase noise is slightly increased if compared to the results reported in Figure 73. The worst case, at an offset frequency of 1 MHz, is found around -

92.65 dBc/Hz and the best one is lower than -97 dBc/Hz. Also the tuning range is slightly reduced, however just a 0.25%. One has to take into account that non-idealities are considered at this phase of the design process, such diodes and models from EM extraction that may contribute some noise to the VCO circuit.

Figure 144 shows the waveforms corresponding to the single-ended VCO core outputs V_{op} and V_{on}, for the central binary code for coarse tuning b[3:0]=1000, and a V_C fine-tuning control voltage sweep.
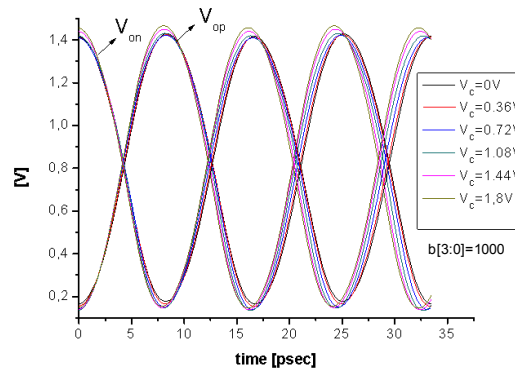
Figure 144: VCO core single-ended output waveforms

6.1.3   ILFD Core

The ILFD 3-bits digitally controlled binary scaled varactors bank of Figure 117 is implemented, in the same way as the VCO, with a centroid structure, in which the unit varactor cell, marked with a black square, controlled by the LSB b_0 is placed at the centre of it, as depicted in Figure 145:
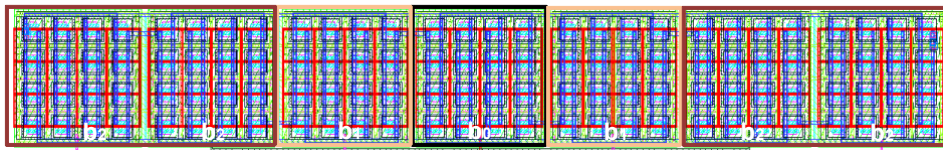
Figure 145: ILFD 3-bit varactors bank layout

The two varactors controlled by b_1, which are adjacent to b_0, are placed around the central varactor, while the MSB b_2 is controlling the four varactors placed at the extreme of the structure. Figure 146 shows the 3D view of the layout interconnections for the active area of the ILFD, including its injection stage. This is the structure used to perform the EM extraction.
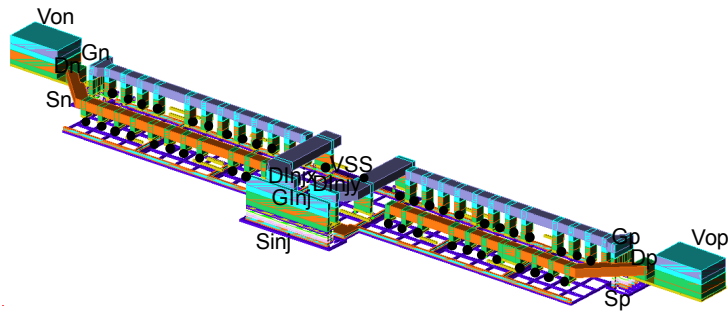
Figure 146: 3D view of the ILFD active area interconnections

The simplification of contacts and vias is performed with the same criteria exposed in the case of the VCO. The ILFD interconnections EM extracted model is a 67-ports element, which is a mix of edge and point ports. All the connections branching from the varactors bank are considered, assigning a port to each of them. They are marked with black circles in Figure 146.

As already exposed in 5.4.2, the ILFD varactors bank is constituted by an accumulation of seven unit varactor cells, each one is a 4x4 array, so high accuracy in the extraction is required also to take into account connections between adjacent unit varactors (in the case of the VCO varactors bank this issue is alleviated since the unit varactor cell is a 1x1 array).

Next Figure 147 shows the ILFD core schematic circuit included the extracted S-parameters models from Momentum. All the terminals of the DK instances are inputs of the EM model of the interconnections and then they are connected among them throw it.
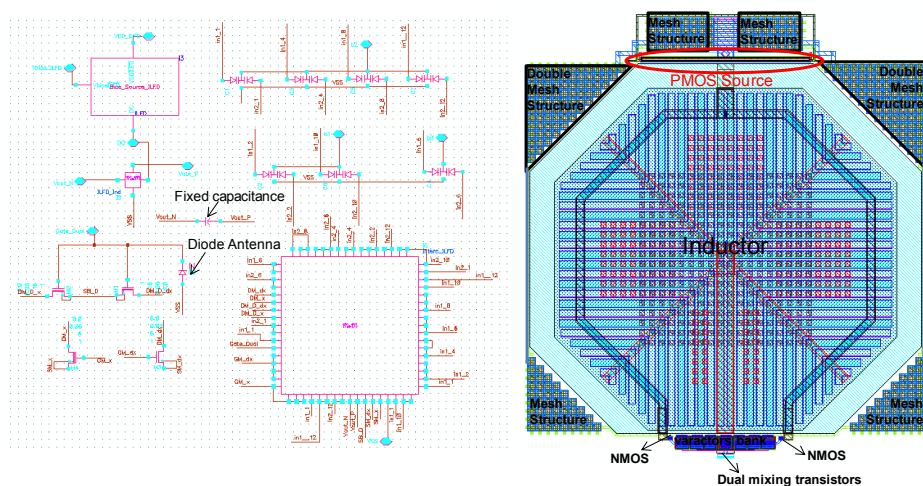
Figure 147: ILFD core schematic including EM extracted models (left). ILFD core layout (right)

Two parallel diodes to avoid antenna DRC violations, indicated as "Diode Antenna" in the schematic circuit of Figure 147, are implemented with an n+ implant in the p-substrate. This is because the bias voltage is provided to the dual mixing transistors M_{inj+} and M_{inj-} with a $\lambda/4$ at 60 GHz TL connected to their common gate, as it will be illustrated in the following pages of this chapter. Therefore such diodes are connected to M1 in the proximity of the gates of both M_{inj+} and M_{inj-}, as shown in Figure 148 where a detailed view of the active area of the ILFD core layout shown. These diodes are required to avoid a collection of charge that can potentially cause yield and reliability problems during the manufacturing of CMOS integrated circuits.
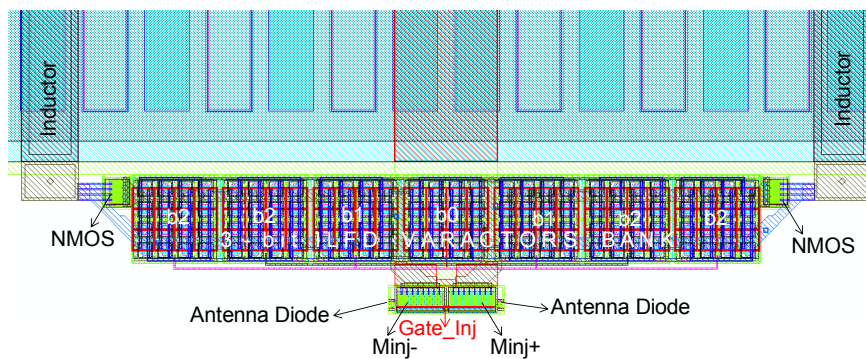
Figure 148: ILFD core: active area layout

The area in Figure 147 (right) indicated as *Double Mesh Structure* is a composition of arrays of a modified version of the unit cell depicted in Figure 142, for voltage supplies and biasing distribution. The 3D view of such modified version, named as *Mesh Double*, is shown in Figure 149, up-down flipped in order to show M1 at the top. It is used to isolate one of the two signals other than the ground plane. It allows the distribution of three signals (the ground plane and two DC voltage signals) across a reduced area of the layout, while fulfilling density rules. In *Mesh Double* cell, M1 is not connected to the rest of metal layers. In this way, three signals can be passed through the plane. The ground plane is always in M1. However, M2, M4 and M6 layers are connected together using vias in the four corners (there are dummy squares of the other metal layer for density reasons, as well in the corners). On the other hand, M3, M5 and M7 are connected together in the centre using vias (there are dummy squares of the other metal layer for density reasons in the centre).
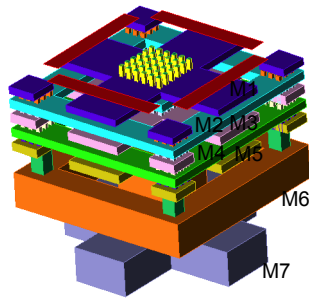
Figure 149: Mesh Double 3D view

The unit cell *Mesh Double* has been simulated with Momentum and the total capacitance to M1 is around 2.75 fF for the signal connected to M2, M4 and M6, and around 3.15 fF for the signal connected to M3, M5 and M7.

In Figure 147 (right) the two *Mesh Double* Structures are used to distribute the ILFD bias voltage V_{bias} and the ILFD voltage supply V_{DD}.

The *Mesh Structures* indicated in the upper area in the ILFD core layout of Figure 147 (right) are two 4x8 arrays of the unit cell depicted in Figure 142. They provide 384 fF of DC decoupling capacitance between ground and V_{DD}. The *Mesh Structures* surrounding the ILFD inductor in the lower area of the ILFD core are just dummy structures, providing ground plane extension and fulfilling density rules.

The circuit of Figure 147 (left) is simulated with GG by performing a HB analysis. In Figure 150 the free-running divide-by-two ILFD discrete tuning range and its single-ended output waveforms are shown. The C_F respecting the budget for parasitic capacitance should be changed (the last value set in 5.4.6 was 17.4 fF) in order to centre the ILFD self-resonance frequencies in the divide-by-two WirelessHD[TM] band, achieving a tuning range very similar to that reported in Figure 124 (left). The C_F value is reduced since in these simulations it is taken into account the effects on the ILFD output load provided by the layout interconnections, and the effective ILFD inductance (L_{ILFD}) resulting from EM simulations should be compensated. After a fine tuning step C_F is set to 12.1 fF.
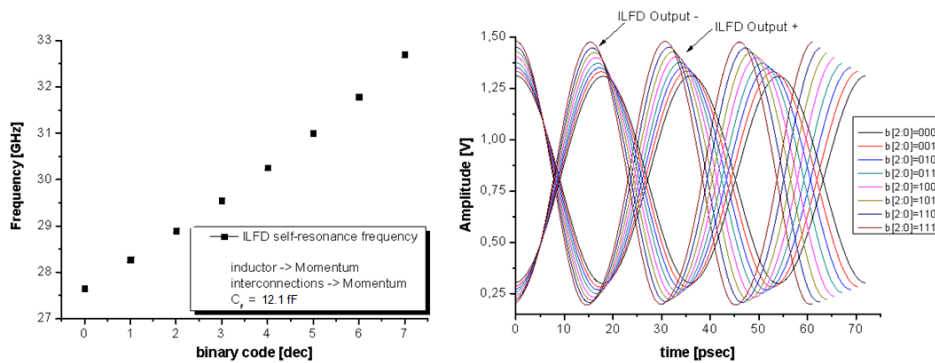
Figure 150: Divide-by-two ILFD tuning range (left). Single-ended output waveforms (right)

As a summary, C_F has been decreased slightly, if compared to 17.4fF, which was the value of C_F for the ILFD schematic of Figure 123 considering the DK inductor model and no interconnections model. Nevertheless, note that the contribution of the ILFD interconnections is not only (17.4 - 12.1) fF = 5.3 fF, since the L_{ILFD} considered now is smaller than the one used in section 5.4.6 , as a result of the EM simulation of the ILFD inductor.

The differential capacitance contribution of the ILFD interconnections in the whole ILFD tank capacitance is estimated in 12.2 fF. This value has been obtained by replacing the extracted EM model of L_{ILFD} in the schematic circuit of Figure 147 (left) by the DK model of this same inductor L_{ILFD}. In this case, C_F needs to have a value of 5.2 fF in order to get the same ILO tuning range than Figure 124 (left). That is, since such ILO tuning range corresponds to the schematic circuit of Figure 123 (where the layout interconnections are not considered and C_F = 17.4 fF), indirectly it results in a capacitance contribution of the ILFD layout interconnections equal to (17.4 - 5.2) fF = 12.2 fF.

The ILO tuning range is slightly decreased if compared to that reported in Figure 124 (left), however just ≈ 1.3%. Now it is almost 17% (from 27.65 GHz to 32.7 GHz) while before it was found around 18.3% (from 27.5 GHz to 33.05 GHz). This reduction is due to non-idealities effects that now have been considered.

The DC values of the circuit of Figure 147 (left) are listed below. They are very similar to those reported 5.4.4 using the SpectreRF simulator.

- V_{bias} = 850 mV

- $V_{DC,out}$ = 755 mV

- $g_{m,CC}$ = 7.38 mS

- I_{dc} = 8.7 mA

- V_{supply} = 1.2V

To simulate the injection locking, an ideal large capacitor (C_{dec} = 10 pF) is inserted in the schematic of Figure 147 (left) in order to DC decouple the Gate_Dual node and the mm-W input source. The DC voltage at such node should be 600 mV, and in the final circuit is provided through a λ/4 TL at 60 GHz, but in this simulation the TL is replaced with the high poly resistor as in the schematic circuit of Figure 126. The final value of such capacitor is not still defined, since it depends on power matching issues related to the VCO output buffer design and, therefore, its value in the final layout will be set during the VCO output buffer design stage.

The ILFD input sensitivity curves can be obtained in a faster way with HB analysis using GG simulator, avoiding longer time domain transient analysis, as is the case when using SpectreRF. A "Frequency Divider Probe" should be placed at the ILFD output, i. e. at ILFD positive output single-ended, and it should be referred to the first harmonic of the signal. Hence, the frequency of the injected signal should be referred at the second harmonic and if the simulation converges, depending on the ILFD input frequency and amplitude, the ILFD is locked, dividing by two the input frequency. If the simulation does not converge, it means that the input signal is not able to lock the ILO. Next Figure 151 shows the dialog windows of GG used to set-up the simulation. Note that in this way it is not possible to analyze the waveforms as done in Chapter 5, since transient analysis is not running and the data are available only in case of convergence, i. e. when the ILFD is injection locked.
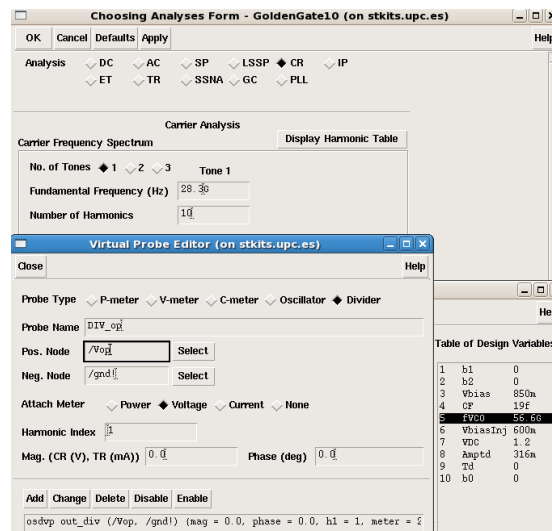
Figure 151: GoldenGate windows to set the simulation for locking analysis with HB

In Figure 152 some waveforms are reported, corresponding to the ILFD injection locked state, for different ILFD tuning codes, input frequencies and amplitudes.
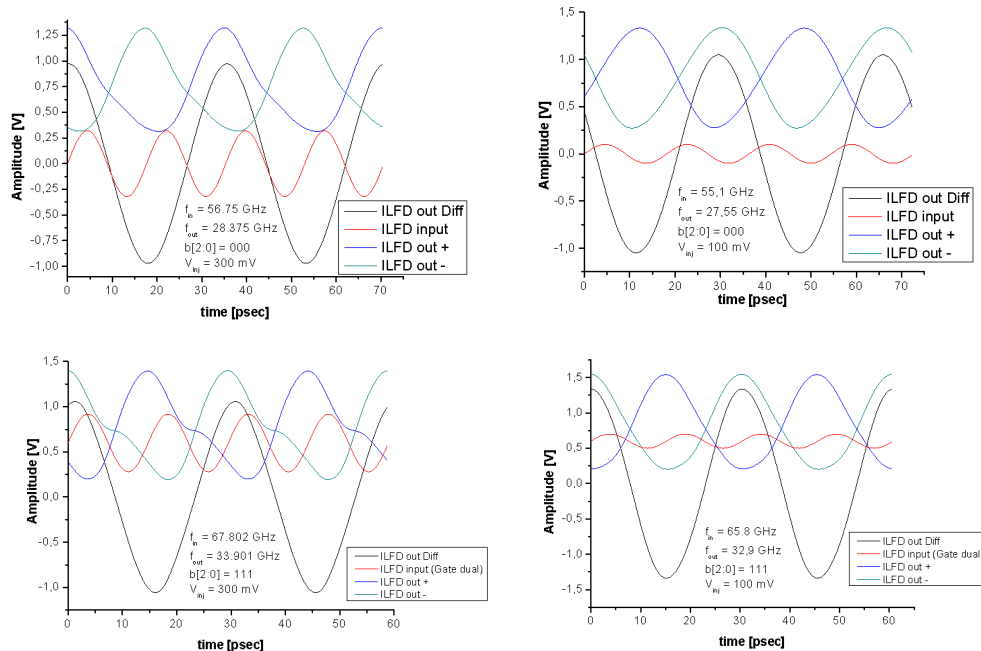
Figure 152: Some ILFD waveforms in locking states

Note that in the upper plots, the injecting input signal is considered at the mm-W input source, i. e. the input signal is DC decoupled, while in the lower plots it is considered at the common gate of the injection transistors, where the DC component of the input signal is present.

Repeating the above described procedure for different ILFD codes, input frequencies and amplitudes, the ILFD input sensitivity curves are obtained and plotted in Figure 153. For comparison, they are superposed to the sensitivity curves obtained in 5.4.5, marked with dashed lines, where only the models from the DK library at circuit level have been considered.
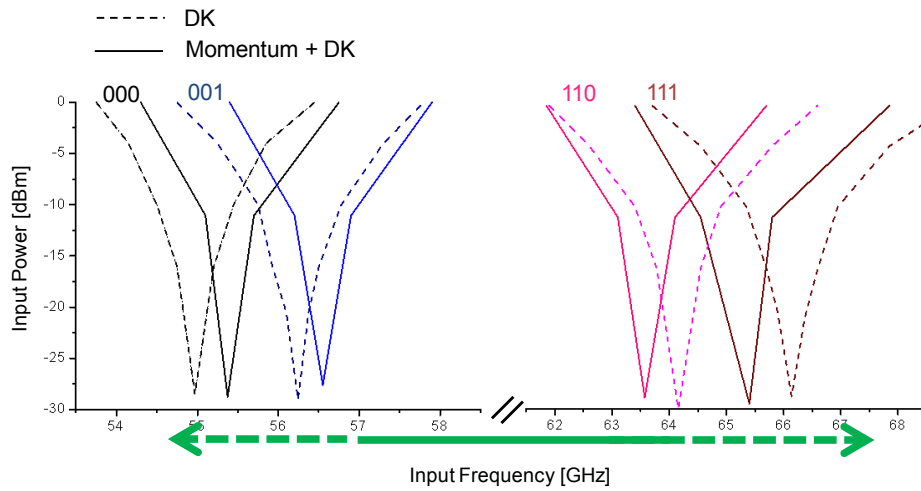
Figure 153: ILFD input sensitivity curves

As it is possible to note, the overall ILFD dividing range corresponding to 0 dBm input power, taking into account the discrete tuning mechanism, is slightly reduced if compared to that one achieved in 5.4.5, where a 24.7% of dividing range at 0 dBm input power was found.

The ILFD dividing range, considering the tuning mechanism for 0 dBm input power and the extracted models from the EM analysis, is ≈ 22%, from 54.3 GHz to 67.8 GHz. The green arrow in the horizontal axis indicates the tuning range. The continuous part of the line corresponds to the WirelessHD[TM] band. Additional lower and upper bands, marked with dashed green lines are available for PVT compensation. The total extended bandwidth for PVT is equal to 6.5 GHz, which is almost a 100% of the band of interest.

6.2 Output Buffers Design and Layout

Once that the ILFD and VCO cores have been laid out, the circuit level (schematics) and physical level (layout) design should done concurrently, in the rest of the design process. The design and sizing of the VCO and ILFD output buffers is constrained by their placement in the layout. The operation of such blocks, but also their size, is strictly determined by the TLs connected at their inputs and outputs and, specially, by the λ/4 TLs at the working frequencies of each block (60 GHz and 30 GHz for VCO and ILFD, respectively). Such λ/4 TLs are required in order to provide the output buffers with voltage supply.

The design of the VCO e ILFD output buffers, at 60 GHz and 30 GHz, respectively, in the same chip can be considered as a further objective of this Thesis. Complex microwave active and passive circuits have to be designed and implemented in the 65 nm CMOS in order to distribute the 30 GHz and 60 GHz signals to allow measurements in a 50 Ω environment. Furthermore, the mm-W signal at 60 GHz must be also carried out from the VCO output to the ILFD injection signal input, which results in a hard design and layout challenges.

The expected chip area should not be higher than 1 mm^2 to avoid incurring in expensive extra charges from the foundry for IC manufacturing. It is a big challenge, taking into account that a λ/4 at 30 GHz TL is ≈ 1.1 mm long (and two of them are needed). Therefore, some trade-offs would be considered: only one single-ended VCO output will be connected to the ILFD input stage, providing it with an internal input source avoiding the need of an external source, like in a PLL. This implies that the VCO output after the buffers is unbalanced. This is because there is no available space in the chip to implement a dummy, composed by the ILFD input stage, in order to provide balanced VCO outputs. As a consequence, only one VCO output buffer is the ILFD input source when the chip is measured in the condition VCO ON - ILFD ON. In addition, in order to minimize the number of the PADs, the VCO core voltage supply and its two output buffers voltage supplies will be connected to the same PAD.

Furthermore, the VCO and ILFD output buffers are designed in order to measure the VCO alone (VCO ON - ILFD OFF) and the ILFD alone (VCO OFF - ILFD ON). In this last measurement situation, there is the need of an external mm-W input source for injecting the 60 GHz signal into the ILFD. The VCO output buffer is therefore designed, sized and fine-tuned in order to provide a 50 Ω matched output for measurement, but also to provide the divide-by-two ILFD with an input signal. Next Figure 154 shows a block diagram of the chip. It has been included the part of the VCO buffer that would be needed in order to achieve balanced outputs for the VCO. It is marked by a dashed square and it consists in a copy of the injection TL (TL$_{in}$) reaching the ILFD and the ILFD input

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stage, i. e. the common gate injection transistors. Note that this block diagram is just to have a preliminary idea of the chip floor-plan, and consequently the number of the TLs is not the final one. However, the ILFD buffer is still considered as a top level block.
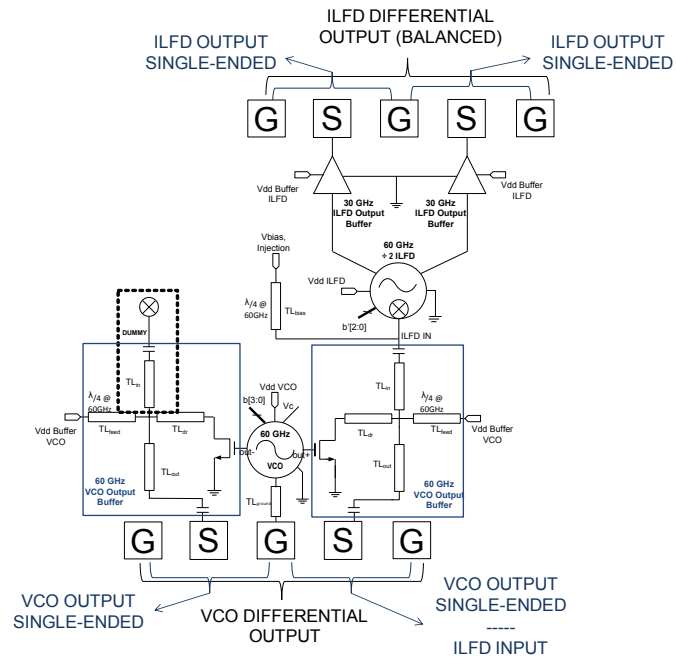
Figure 154: Preliminary block diagram of the chip

The output buffers, for both ILFD and VCO, are common source amplifiers with some TLs. A simplified output buffer schematic is depicted in Figure 155 just an illustrative example. More complicated structures, such as stubs, will be implemented when needed in order to achieve a good matching to 50 Ω.
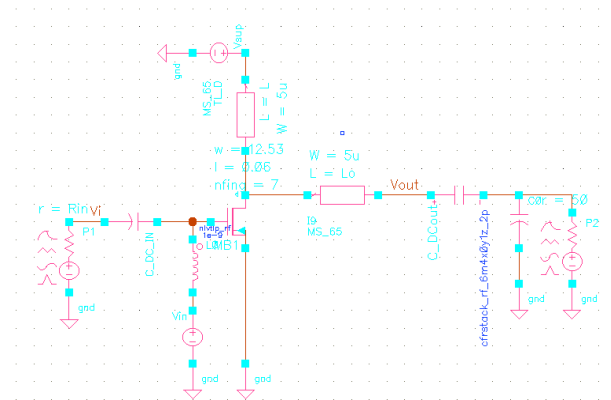
Figure 155: Common source amplifier as output buffer

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The transistor is biased with an external DC source through a large inductance in order to choke the RF signal. Nevertheless, in the final design the external DC source is eliminated, since the DC outputs of the ILFD and VCO cores are providing the DC bias voltage. In this way, no DC blocking capacitors are needed at the buffer input stage.

The ILFD outputs are balanced at the differential mm-W PADs required for measurements, since two symmetrical output buffers are implemented for the ILFD. In the case of the VCO, the differential outputs are unbalanced, for the above mentioned reasons.

The available silicon surface is organized to dedicate half of the 1mm x 1mm die to the ILFD e and the other half to the VCO, as depicted in the following Figure 156, where a preliminary floor-plan of the chip is shown. The mm-W GSGSG differential PADs are re-used from a previous design. The S-parameters of such PADs are available so that they can be included in the simulation for fine tuning of the buffers output impedance including such PADs. They are considered during the buffers design. The PADs 1-to-16 are DC PADs for biasing and voltage supplies.
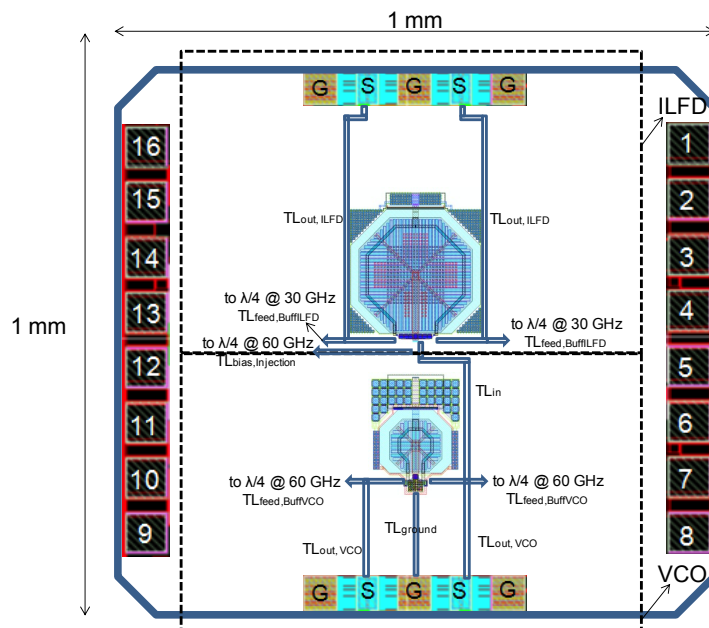
Figure 156: Preliminary chip floor-plan

As it is possible to note it is very difficult to achieve a complete symmetry for the VCO output stage in order to obtain balanced differential outputs. In addition, due to the limited area available, all the λ/4 TLs and some other TLs in the buffers are going to be implemented with serpentine structures.

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Therefore they are simulated with Momentum in order to achieve the required characteristics according to the geometry imposed by the available space.

Other critical layout issue is the mutual coupling between close TLs. For instance, in Figure 156 it is possible to observe that the $\lambda/4$ at 60 GHz TL biasing the ILFD injection stage ($TL_{bias,Inj}$) would be very close to the $\lambda/4$ at 30 GHz TL used to provide the ILFD output buffer with voltage supply ($TL_{feed,BuffILFD}$). Therefore, shielding walls, composed by stacked metal layers M1-to-M7, are implemented in order to avoid coupling between TLs.

As it is possible to note in the floor-plan of Figure 156, one of the VCO output PADs is directly connected to the ILFD input through the track composed by $TL_{out,VCO}$ and TL_{in}. This path is used in order to test the ILFD in the case VCO OFF - ILFD ON, which requires the injection of the 60 GHz input signal from an external source. On the other hand, the VCO is internally connected to the ILFD input stage through TL_{in}, which therefore is a component that has to be considered in the VCO output buffer design. Some TLs crossings and T-junctions are present in the design and they should be modelled to take into account their impact in the TL characteristics at the working frequencies during the design.

Sixteen PADs are available for DC biasing and voltage supplies. One of them is for ground connection. Another one is for the VCO core and its output buffers voltage supply. Eight PADs are dedicated to the fine and coarse tuning control signals of the VCO and ILFD. Three PADs are for the ILFD core and its output buffers voltage supplies. The remaining three PADs are for the bias voltage of the VCO, and the bias of the ILFD and its injection stage.

Once that the ILFD and VCO, including their output buffers, are placed in the layout, the remaining available areas would be filled with regular arrays of ad-hoc decoupling capacitors, as it will be exposed later.

Next sub-section is dedicated to the design and layout of the ILFD output buffer with a deep analysis of the related issue just mentioned. The VCO output buffer will be treated with less details, since the design methodology adopted is basically the same.

6.2.1 ILFD Output Buffers

Figure 157 shows the schematic circuit of the 30 GHz output buffer for the 60 GHz divide-by-two ILFD. It is a common source amplifier. The active stage is a NMOS transistor. The TL_{feed} is $\lambda/4$ at 30 GHz TL used to provide the active device with voltage supply, i.e. 1.2V. Some other TLs are implemented in order to reach the ILFD output PAD ensuring 50 ohm impedance matching. The

TLs are modelled using a parameterized microstrip multilayer model, as will be exposed soon.
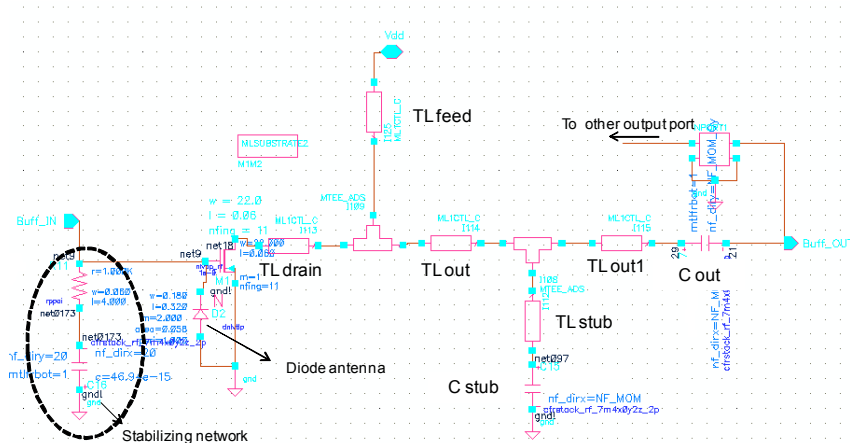
Figure 157: ILFD output buffer schematic

A stabilizing network is implemented in order to avoid any unwanted oscillation provided by the buffer. A N+/Pwell diode is inserted to avoid antenna effects in the gate of the transistor. The S-parameters model of the GSGSG mm-W differential PADs implemented in the layout is considered during all the buffer design process, to take into account the loading effects of the PADs. This model is provided by the foundry. Even if differential measurements are therefore potentially allowed, single-ended measurements will be performed with GSG probes, due to the unavailability of GSGSG probes and external balun. Some capacitances are implemented with stacked MOM capacitors.

The buffer design starts using GG S-parameters analysis to determine the output impedance of the ILFD. The Figure 158 shows the test bench circuit and the results of the S-parameters analysis for Z- and Y-parameters of one of the ports, taking into account that they are the same for the other port. As expected, at resonance frequencies, the LC ILFD shows no imaginary part in the output impedance.

There are some constraints in the design that should be considered a priori in the buffer design. The connections to the positive supply of the drain of the buffer transistor will always require a long interconnection that effectively acts as a TL. So at first the λ/4 at 30 GHz TL is considered and designed. In order to design such TL, some basic building blocks are considered. Following they are briefly presented.
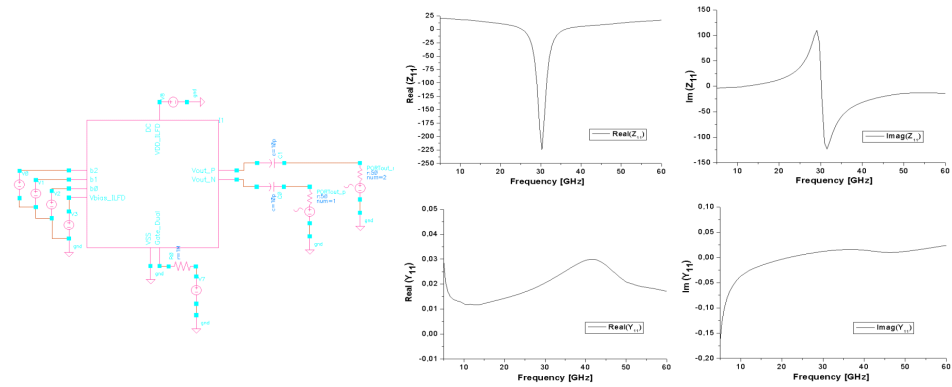
Figure 158: Test bench for ILFD output impedance (left). Z$_{11}$ and Y$_{11}$ plots (right)

The ground plane of the microstrip TL is made of an array of basic cells named *MASSA_M1M2*, shown in Figure 159 (left). Figure 159 (right) shows an example of a 4x4 array of these cells. It is composed by M1 plus M2 layers to increase the conductivity of the ground plane, and the layout is done in for fulfilling density rules. The basic cell dimension are 1.7 μm x 1.3 μm. M1 is a ring structure while M2 is a cross connected to M1 at the end of each arm, as shown in Figure 159 (left) and Figure 159 (centre). In the microstrip TL the RF signal is laid on M7 while the ground plane is hence constituted by M1+M2. For such structure, considering a TL width of 6 μm, the substrate parameters provided by the foundry are reported in Table 8.
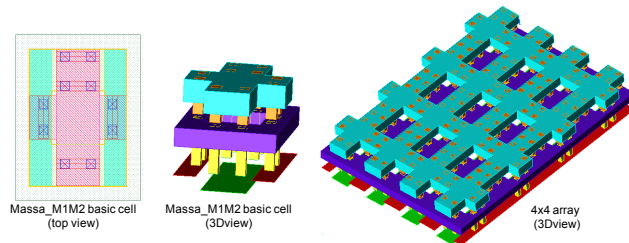
Figure 159: Detailed images of the ground plane implementation for the TLs

Relative dielectric constant	5.273416478
Substrate thickness [μm]	3.62
M7 conductivity [S/m]	50e6
M7 thickness [nm]	900
M1+M2 conductivity [S/m]	50e6
Dielectric loss tangent	0.004

Table 8: Substrate parameters for M1+M2 ground plane, RF signal of M7 and TL width of 6 μm

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Taking into account the parameters reported in Table 8, the guided wavelength λ at 30 GHz is $\lambda = \lambda_0/\sqrt{\varepsilon}$, where λ_0 is the wavelength in the free-space, such that $\lambda_0 = c/f$ and ε is the relative dielectric constant. Being c the speed of the light in the vacuum and $f = 30$ GHz, $\lambda/4$ at this frequency is ≈ 1.088 mm. Figure 160 shows a 3D view of the $\lambda/4$ at 30 GHz TL used to provide the ILFD output buffer with voltage supply. The ports used and their location for the S-parameters model extraction from EM Momentum simulations are also shown. Note that some corners are implemented in order to achieve the serpentine path required to fit in the available space.
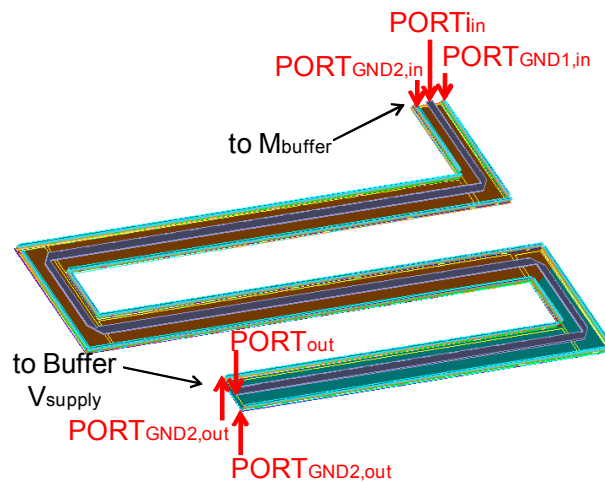
Figure 160: 3D view of the 30 GHz λ/4 TL feed for ILFD buffer

In Figure 161 some details of the TL of Figure 160 are shown. Wall structures composed of a stack of M1-to-M7 are implemented at the edges of the TL to shield the RF signal reducing losses and coupling effects. They are located at both sides, 10 μm away from the signal line. The geometry of the corners used in order to minimize the impact of a non-straight microstrip at high frequencies [3] is also depicted in Figure 161 (right).
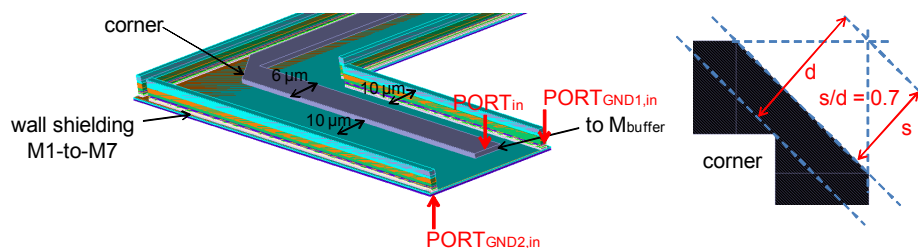
Figure 161: Detail of Figure 160 (left). Corners geometry (right)

Figure 162 shows the imaginary part of the impedance of the TL of Figure 160, simulated with Momentum, in the form of admittance extracted from the S-parameters analysis. Such TL is 1.155 mm long. Alternatively an analytical model of the TL can be used in the simulations. This analytical model is encapsulated in a library cell from the GG library. The model if fully parameterable. The user must provide the basic horizontal geometry of the line and the length, while the vertical dimensions are input in the form of a substrate definition file. The simulation results obtained with such a TL model (labelled "*Distributed*") are compared with the Momentum model results in the same Figure 162. The multilayer TL model does not takes into account corners or other shapes. For this reason, the length of the multilayer TL is set exactly to the theoretical value of 1.088 mm. Note that the length of the Momentum line has been optimized to behave as a λ/4 feed at 30 GHz including the effects of the corners, which requires to enlarge it by 67 μm compared to the theoretical value.
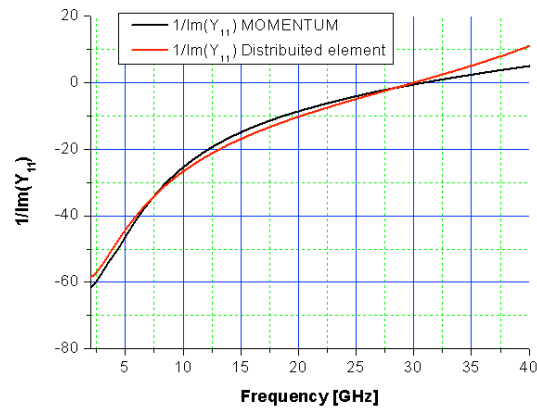
Figure 162: 30 GHz λ/4 TL parameter

From the preliminary floor-plan of Figure 156, a TL of ≈ 25 μm length (TL$_{drain}$) is required in order to reach the λ/4 TL$_{feed}$ from the drain of the ILFD buffer transistor. In addition, a TL of ≈ 400 μm length is required in order to reach the ILFD output PADs. This first configuration of the ILFD output buffer is shown in the schematic of Figure 163, where the input port is set to the real impedance value dictated by the S-parameters analysis of the ILFD core shown in Figure 158 and the bias voltage of the transistor is provided using an ideal bias-T.
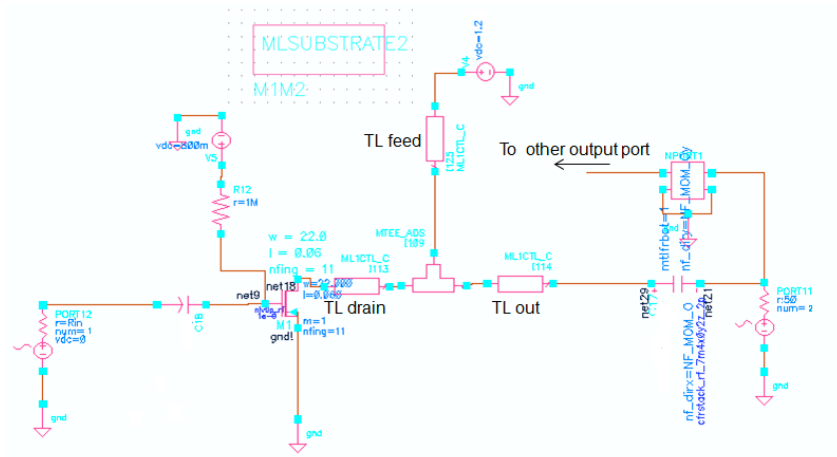
Figure 163: First version of ILFD buffer

When the buffer is connected to the ILFD output, the large input decoupling capacitor is eliminated, since the DC output voltage of the ILFD is used to bias the buffer active stage. The NMOS transistor width is set to 22 µm, with 22 fingers in order to reduce its capacitive load, at minimum channel length (60 nm). This transistor width will be reduced if the differential input capacitance provided by the buffers is above the final budget of fixed capacitance for the ILFD (12.1 fF) found in 6.1.3.

The output drain is DC decoupled with a RF MOM capacitor available in the foundry components library. Its capacitance varies with its sizing, which is left as an optimization parameter, and it is connected to a 50 Ω port. The output PADs impact is taken into account by inserting in the test bench a s2p file modelling them. The TL$_{feed}$ is that implemented above. It is simulated in the buffer schematic by means of the extracted Momentum model, while the rest of TLs are modelled using the multilayer microstrip components from GG library. They are defined by a substrate model that takes into account the implementation in M7 for the signal line, and M1+M2 for the ground plane, having 6 µm of width in all the cases.

The RF MOM capacitor is constituted by selectable stacked metal layers (from M2 to M5) with different number of fingers in X and Y directions, x and y respectively, that vary in number for different capacitance values.
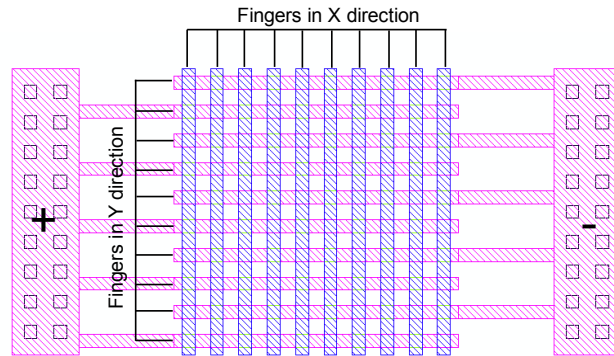
Figure 164: 10x10 fingers stacked RF MOM capacitor

The intersection due to TLs crossing (i. e., TL_{feed}, TL_{out} and TL_{drain}) is taken into account using in the schematic a "T" multilayer microstrip component from GG library. The range of variation of TL_{drain} length is very restricted by the floor-plan of Figure 156, so that it cannot be considered as a design variable in order to achieve a good 50 ohm matching at 30 GHz. In this first version it is set to its final value, that is 90 μm according to such floor-plan. Figure 165 shows some results of S-parameter analysis for different TL_{out} length and different C_{out}. The length of this line could be made longer than 400 μm if necessary by implementing a serpentine structure.
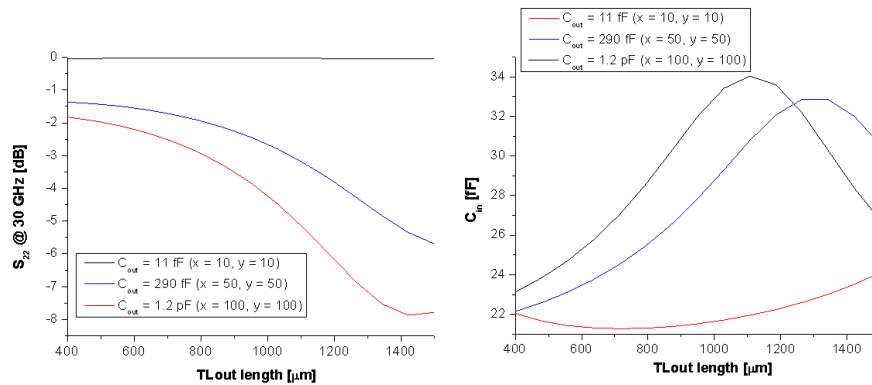
Figure 165: 50Ω output matching at 30 GHz (left). Buffer input capacitance at 30 GHz (right)

As it is possible to note from the results of Figure 165 (left), a good matching is not achievable with the architecture of the first version of the buffer. Stubs should be added in appropriate and convenient points of the buffer, but this complicates the layout, since other TLs and MOM capacitors must be implemented. The C_{in} plotted in Figure 165 (right) is the buffer input capacitance such that $C_F = C_{in}/2$. C_{in} is calculated from the S-parameters results as

$C_{in} = Im(Y_{11})/2\pi f$. The buffer DC current consumption for this first implementation is 8.9 mA at 1.2V.

After several optimization loops, taking always into account the available area in order to implement appropriate structures for the TLs, a second version of the ILFD output buffer schematic is designed, as shown in the Figure 166 :
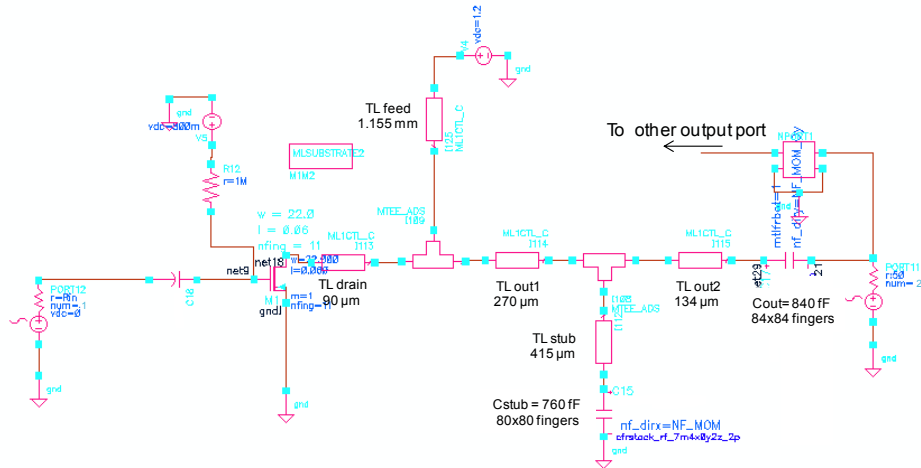
Figure 166: Second version of the ILFD buffer

The most important change is the addition of a stub. The required TL_{stub} length is determined with an optimization process using the multilayer microstrip component from GG library, and once the final length is found it is laid out in the space available. Figure 167 shows the 3D view of the 415 µm long TL_{stub}. It has been simulated with Momentum in order to extract its S-parameters to be included in a final post-layout simulation of the buffer.
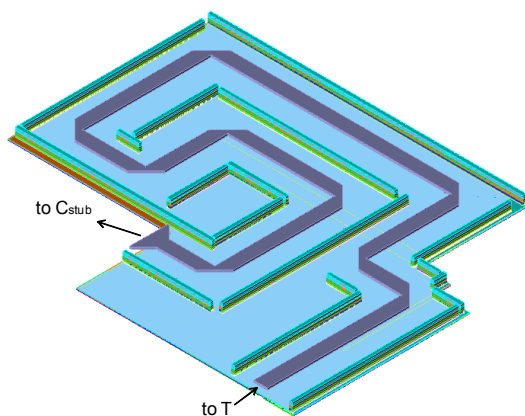
Figure 167: ILFD output buffer, TL stub, 3D view

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A serpentine structure is required to implement the TL$_{stub}$ in order to achieve the required TL length. In Figure 168 the layout view of the ILFD buffer of Figure 166 is shown.
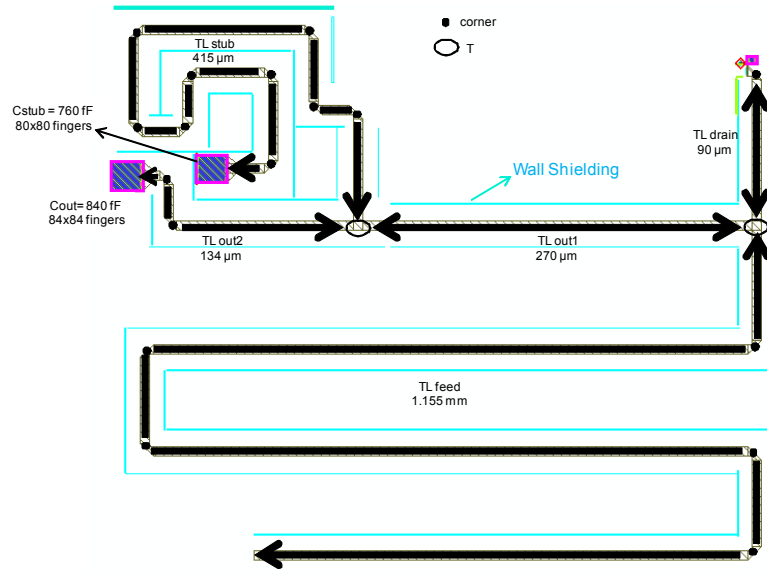
Figure 168: ILFD buffer layout

All the TLs implemented in the layout are simulated with Momentum in order to extract their S-parameters. They are included in the post-layout simulation of the buffer shown below. In the next Figure 169 some results of the buffer S-parameters simulation, using the distributed models (multilayer microstrip TLs) from GG library, are compared with those achieved using the extracted models from Momentum.
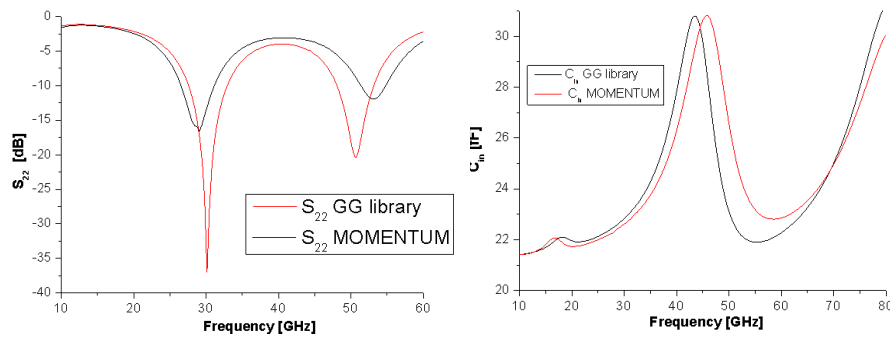
Figure 169: 50Ω output matching (left). Buffer input capacitance (right)

A good output matching is achieved around 30 GHz. The capacitance provided by the ILFD output buffer is around 23 fF at 30 GHz. The next step is to check the buffer stability. The result of the stability analysis up to 100 GHz is reported in Figure 170. Being the μ_1 and/or the μ_2 factors > 1, the 2-ports network constituted by the ILFD output buffer isn't unconditionally stable.
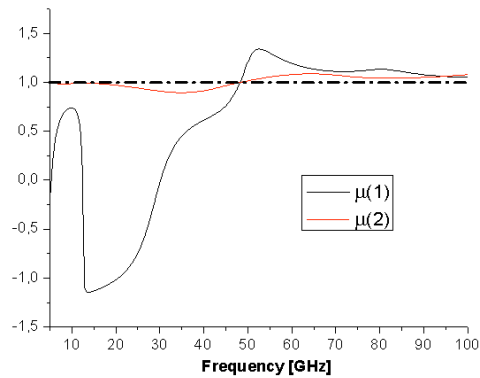
Figure 170: μ_1 and μ_2 factors

A 2-ports is unstable, and consequently potentially oscillating, if the admittance of either port has a negative conductance for a passive termination on the second port. Therefore, the Re(Y_{11}) and Re(Y_{22}) parameters of the circuit of Figure 166 are calculated and plotted in Figure 171, in order to localize the cause of the instability.
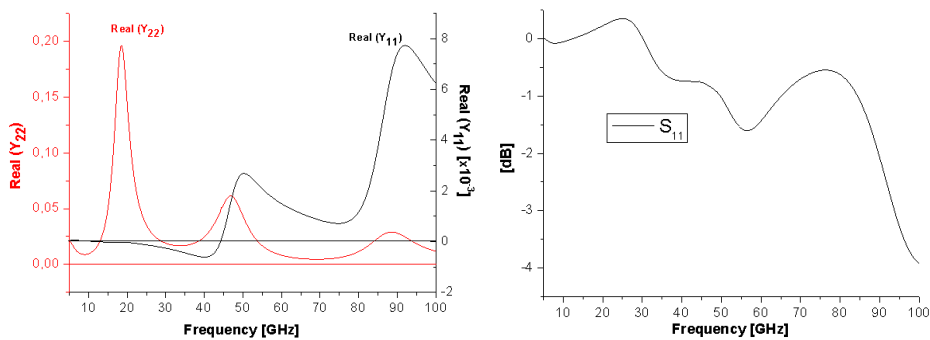
Figure 171: Re(Y_{11}) and Re(Y_{22}) (left). S_{11} parameter (right)

While Re(Y_{22}) is always positive, there is a frequency range in which Re(Y_{11}) is negative. It results in a S_{11} parameter > 0 dB around 20 GHz. In order to solve the instability issue, a pole is added at a higher frequency, implemented in the buffer input stage by the stabilizing network already illustrated in Figure 157. It is composed by the series combination of a 1 KΩ poly silicon resistor and

a 47 fF stacked MOM capacitor placed between the gate of the NMOS and ground. Such network has been inserted at the buffer input stage, since the cause of the instability is at the input (i. e., Re(Y_{11}) < 0). A more detailed description of the procedures that can be used in order to detect, analyze and solve the instability issue can be found in [4].

Figure 172 shows a detail of the layout of the ILFD buffer input stage. The stabilizing network is shown, as well as the N+/Pwell diodes added to avoid antenna effects during the IC manufacturing.
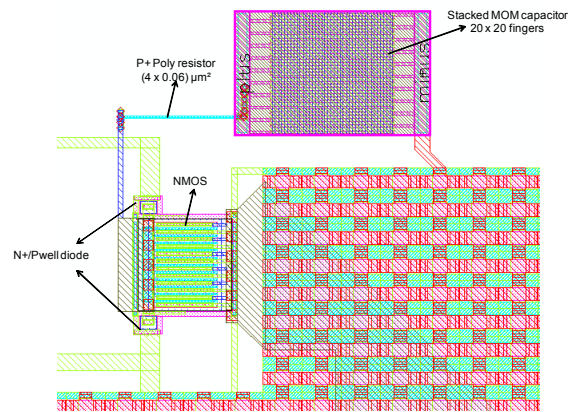
Figure 172: Layout of the ILFD buffer input stage

The buffer stability is now re-checked. Figure 173 shows how the instability problems have been solved.
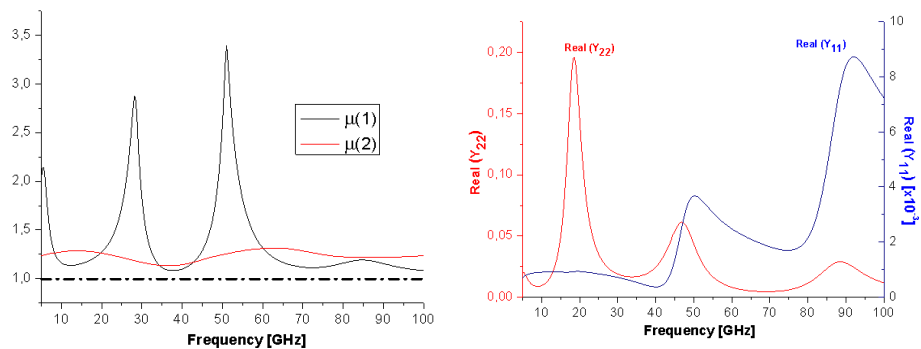
Figure 173: Results of the solved instability

The output matching of the final ILFD buffer, including the stabilizing network and the whole non-idealities, is hence shown in Figure 174, together with its input capacitance (only Momentum models for the TLs are used in this case).
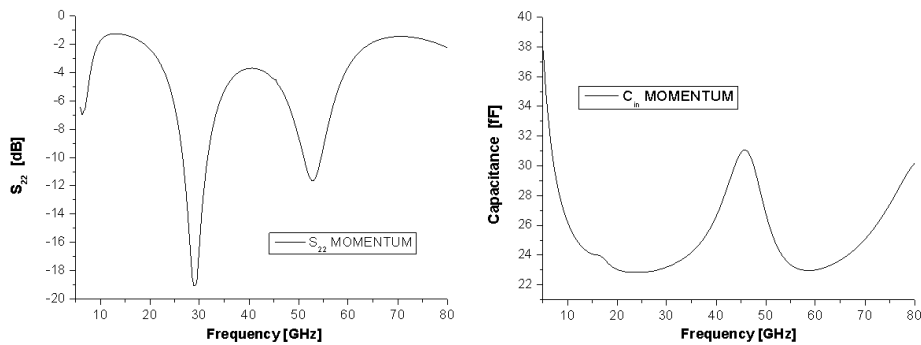
Figure 174: Final results. 50Ω output matching (left). Buffer input capacitance (right)

C_{in} is around 24 fF at 30 GHz. It results in a differential capacitive contribution to the ILFD load of ≈ 12 fF. Since the available budget was 12.1 fF, no buffer re-sizing is needed. Nevertheless, this will be confirmed later when the buffer is connected to the ILFD core. The buffer DC current consumption is 8.9 mA for a voltage supply of 1.2V.

Regarding the buffer voltage gain, both AC and HB simulations are needed to obtain it. This is because the AC analysis assumes small signals and linear behaviour, which is not true in a oscillator, since the input signal of the output buffers is quite large. Next Figure 175 shows the ILFD buffer voltage gain from AC simulation, considering the extracted models from Momentum for all the TLs of the buffer:
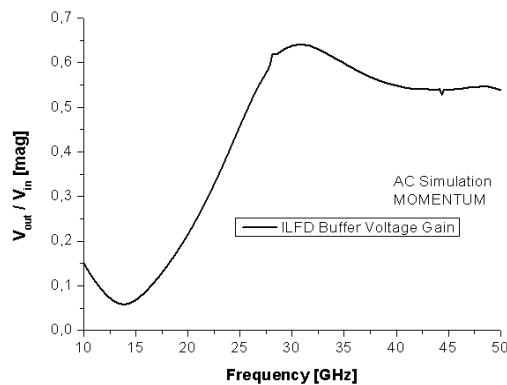
Figure 175: Buffer voltage gain. AC simulation

As mentioned, the buffer could be operating in gain compression when driven by the ILFD output signal, such as that shown in Figure 152. It is checked in the following analysis. The HB simulation results for non-linear buffer

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behaviour are shown in the Figure 176. The input frequency is 30 GHz, and the Momentum extracted models of the TLs are considered.
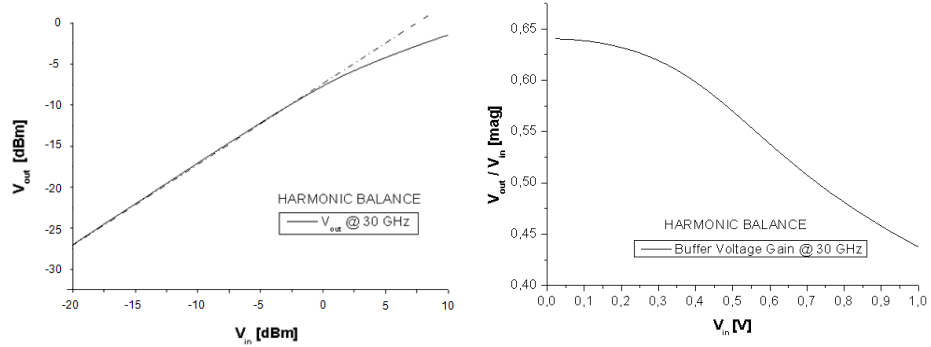
Figure 176: HB results at 30 GHz. V_{out} vs V_{in} (left). Voltage gain (right)

As it is possible to observe, the AC and HB results of the ILFD buffer analysis are consistent only for small input signals (up to 0.15V input amplitude). The realistic buffer operation range is for around 0.9V input signals, where the buffer voltage gain is reduced to 0.47, approximately. Nevertheless, the buffer is very linear and not very much affected by compression.

In Figure 177 the input and output buffer waveforms resulting from the HB analysis are reported, corresponding to an input amplitude of 1V, for different frequencies.
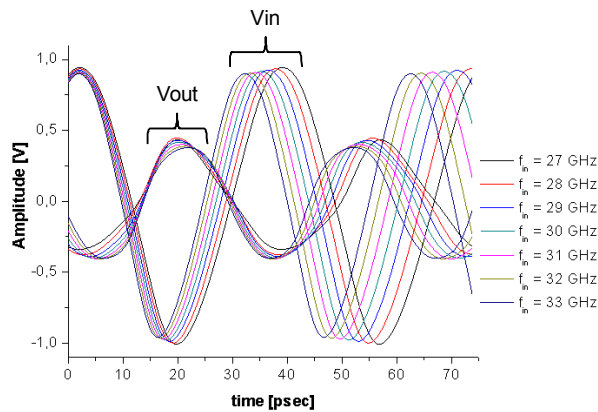
Figure 177: Input and output Buffer waveforms

The next step is the design and layout of the VCO output buffer, which provides the ILFD with 60 GHz input source inside the chip. In addition, such

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buffer is designed to perform the 60 GHz VCO measurement in 50 Ω environment.

6.2.2   VCO Output Buffers

The VCO output buffers design follows the same steps exposed for the ILFD buffer design. In this case, the operation frequency is 60 GHz, so that TLs feeds of λ/4 electrical length at 60 GHz (TL$_{feed}$) are needed in order to provide the buffer with voltage supply. The VCO output buffer implemented in this Thesis is a common source amplifier stage. Its schematic circuit is shown in Figure 178.
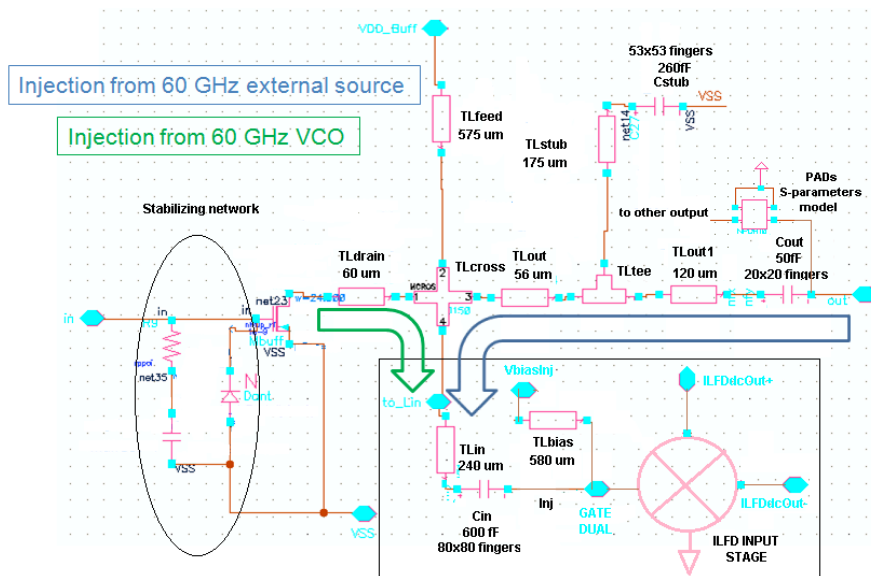
Figure 178: VCO output buffer schematic (ILFD input stage is included)

The selected width for the NMOS is 24 µm, with 24 fingers, at minimum channel length (60 nm). Since we have a lot of budget for the VCO load capacitance (C$_F$ = 14.8 fF, as reported in 6.1.2) a quite large width transistor has been selected, in order to increase the buffer gain allowing higher signal injecting from the VCO into the ILFD. If the post-layout input capacitance provided by the VCO buffer would result too high, the NMOS will be re-sized.

The VCO core DC output voltage (i. e., 750 mV) is used to provide the buffer with biasing voltage since no DC blocking capacitors are inserted between the two blocks. Some microstrip TLs and MOM capacitors are used in order to match the buffer to 50 Ω and allow the measurements of the VCO output signals. Simultaneously, the TL used to connect the 60 GHz output buffer to the ILFD (TL$_{in}$), allowing internal injection from the VCO to the ILFD, is

designed and it has to be considered in the VCO output buffer design. This because, as already mentioned, the overall VCO+ILFD test chip is designed in order to allow both the injection from an external input source (VCO OFF - ILFD ON) and from the VCO (VCO ON - ILFD ON). In addition, the VCO stand-alone can also be measured (VCO ON - ILFD OFF). Therefore, the sizing of TL_{in} impacts in the buffer design parameters.

During the VCO output buffer design the RF choke required to provide the ILFD injection stage with biasing voltage is also designed. It is implemented by means of a λ/4 at 60 GHz TL (TL_{bias}). In order to fit it in the available area, the TL_{feed} and TL_{bias} are implemented with serpentine structures.

The VCO output buffers are designed taking into account the ILFD input stage, i. e. the circuit composed by the common gate injection transistors M_{inj+} and M_{inj-} of the ILFD. As a consequence, only one VCO output PAD is considered during measurement (that one from which the ILFD input signal is injected, when a 60 GHz external input source is used). The injection signal paths corresponding to both cases VCO OFF - ILFD ON and VCO ON- ILFD ON, are indicated with a blue and green arrows, respectively, in Figure 178.

Two multilayer microstrip TL models available in the GG library, i. e., TL_{cross} and TL_{tee}, are used in order to model the crossing among 4 TLs (in the schematic of Figure 178 they are TL_{drain}, TL_{out}, TL_{in} and TL_{feed}) and the "T" junction for TL_{out1}, TL_{stub} and TL_{out}.

A stabilizing network is inserted at the VCO buffer input stage in order to achieve unconditionally stability. Such condition is obtained by connecting the NMOS gate to ground through the series of a high value (1 KΩ) poly silicon resistor and a MOM staked capacitor (50 fF). A N+/Pwell diode is also connected to the NMOS gate to avoid antenna effects during the IC manufacturing, potentially caused by the buffer implementation in the layout.

The same S-parameters model of the mm-W output PADs used for the ILFD buffer design are considered here to take into account output loading effects of the differential GSGSG PADs. However, single-ended measurements will be performed with GSG probes. Note that also the 60 GHz input signal will be injected into the ILFD from one of the VCO output PAD by using a GSG probe (ILFD ON - VCO OFF).

The VCO buffers current consumption is 7.78 mA from 1.2V voltage supply.

Figure 179 shows some results from the S-parameters analysis of the circuit in Figure 178, comparing the DK and GG library models with the DK and Momentum extracted ones. That is, all the TLs have been simulated with

Momentum and their extracted models have been included in the post-layout buffer simulation:
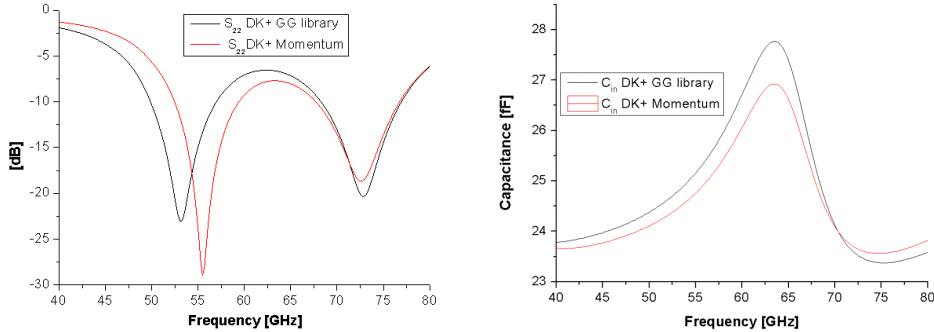
Figure 179: 50Ω output matching (left). Buffer input capacitance (right)

The buffer input capacitance is ≈ 25 fF at 60 GHz. It means a differential capacitive contribution to the VCO load of ≈ 12.5 fF. This value should be subtracted to the C_F budget set in 6.1.2. As it is possible to observe in Figure 179 (left), none of the S_{22} minima are centred in the band of interest. This is done intentionally in order to achieve the maximum of the buffer voltage gain (V_{out}/V_{in}) at 60 GHz, as shown in Figure 180, where some results of the AC analysis are reported. The injection voltage gain (V_{inj}/V_{in}) is also plotted in the same figure, in order to evaluate how much signal coming from the VCO is effectively injected into the ILFD. The signal V_{inj} is considered at the ILFD input stage, as reported in the schematic of Figure 178.
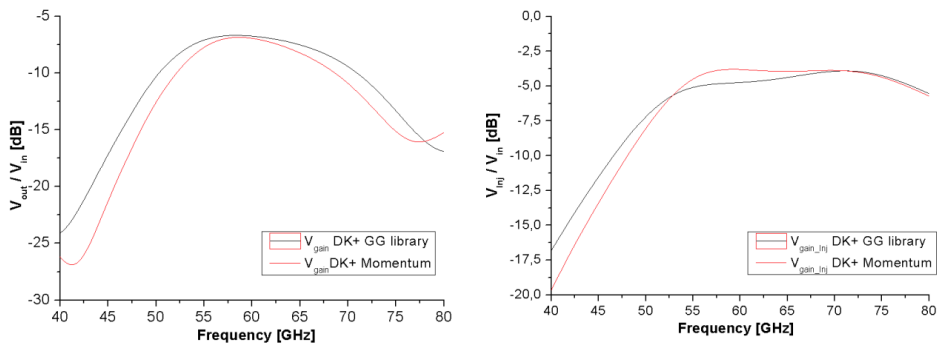
Figure 180: Buffer voltage gain V_{out}/V_{in} (left). Injection voltage gain V_{inj}/V_{in} (right)

Considering the result of the injection gain V_{inj}/V_{in} from the post-layout EM extraction, the VCO core signal at 60 GHz that is injected into the ILFD gets attenuated by around 3.75 dB. Note that the buffer is further attenuating the VCO injection signal up to ≈ 5 dB for the lower VCO frequency range. Taking

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into account the VCO core output impedance and amplitude, the VCO signal injected into the ILFD is expected to be always > -5 dBm, across the overall VCO tuning range. Therefore, all the VCO output frequencies are tracked by the ILFD, allowing division-by-two (see Figure 153). This is further verified in the section 6.4, where the VCO and the ILFD are simulated together.

The next Figure 181 shows the buffer waveforms as the result of a large signal HB simulation, for an input signal amplitude of 1.2V, which frequency varies from 57 to 64 GHz.
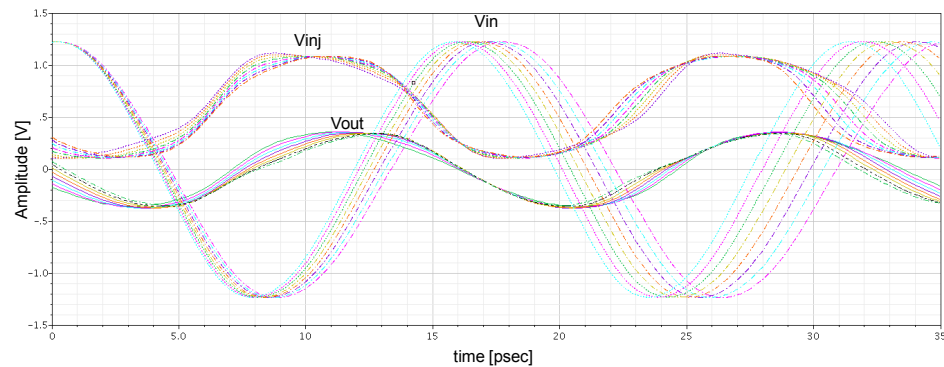
Figure 181: 60 GHz buffer waveforms

6.3   Top Schematic and Layout Completion

In this section, it is described how the top circuit layout is completed, comprising some design strategy issues and considerations. The next section 6.4 is dedicated to the post-layout simulation results of the top circuit.

The layout including PADs, VCO and ILFD cores, VCO and ILFD output buffers and control lines for DC voltages is shown in Figure 182 . Note that there is only one PAD (PAD 7) to provide the VCO core and both the VCO output buffers with DC supply voltage. That is, these nodes are internally connected each other's by using decoupling capacitors structures, as it is detailed in the following. The TL TL_{ground} of 190 um is designed and placed in the layout (it starts from the central G PAD of the GSGSG mm-W PADs of the VCO outputs) in order to provide the VCO active stage in deep Nwell with ground contact. This line is part of the phase noise filter, as described in 4.6.1.
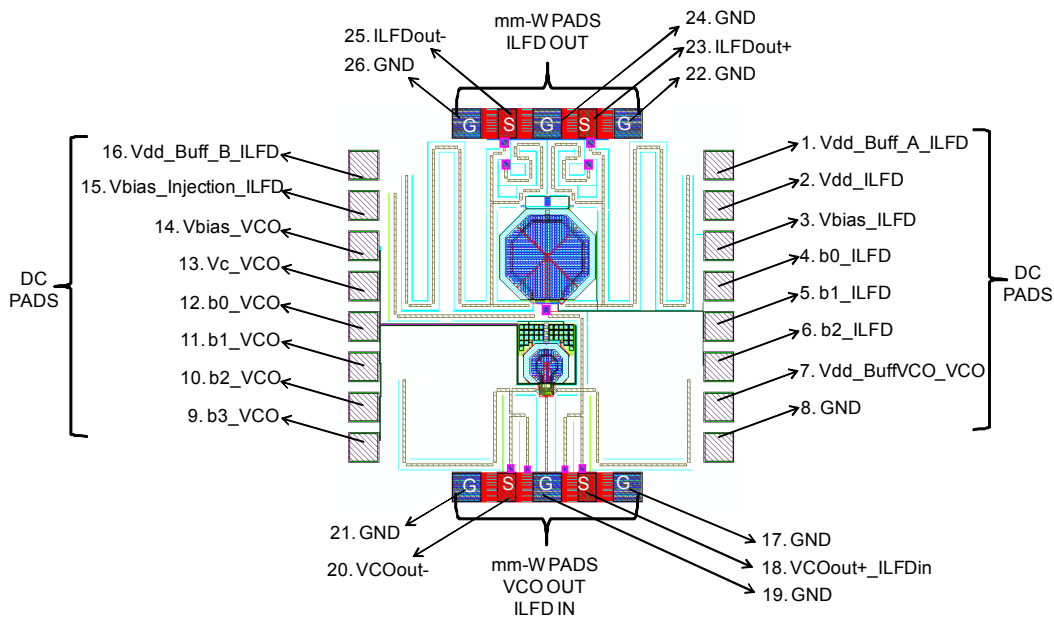
Figure 182: ILFD-VCO TOP partial layout

Note that, regarding the measurements, in the scenario VCO OFF - ILFD ON, when an external 60 GHz input source is providing the ILFD with the injecting signal, the PADs to be considered are 17-18-19. The GSG coplanar probe connected to the external source should be placed in these PADs, since as it is possible to see in the layout, no injection track exists from the other 19-20-21 PADs (the VCO differential output is unbalanced).

Finally, the empty space in the layout is filled with decoupling capacitor structures which are used also to distribute the DC voltage supplies and biasing, as well as ground plane extension, while avoiding density rules violations.

These decoupling structures are composed by arrays of basic decoupling cell shown in Figure 183 and Figure 184. It is composed by a MOM capacitor, a NMOS transistor (L = W = 10 μm) with its source, bulk and drain connected together to form one capacitor terminal, whereas the gate forms the other one. This MOM+MOS capacitor is surrounded by a ring of the basic decoupling cells already described in sections 6.1.2 and 6.1.3 The two Mesh cells used are shown in Figure 142 (*Mesh Single*) and Figure 149 (*Mesh Double*). If the signals to be distributed are two, where one of them is ground, the decoupling cell in Figure 183, which includes the *Mesh Single* cells, is used. Otherwise, if the signals to be distributed are three, where one of them is always ground, the decoupling cell in Figure 184, which includes the *Mesh Double* cells, is considered. The diode indicated in the schematics is implemented to avoid

antenna effects. VM is the ground terminal. The decoupling capacitances associated to both these cells are indicated in the captions of the Figure 183 and Figure 184. These values have been provided by a post layout simulation of the RCc and Cc extracted views, i. e. from the equivalent circuit including parasitics extracted from the layout.
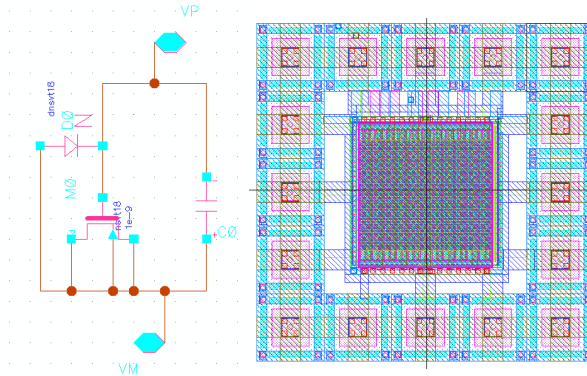
Figure 183: Mesh Single Decoupling Capacitor Extended cell (total C$_{dec}$=485 fF)
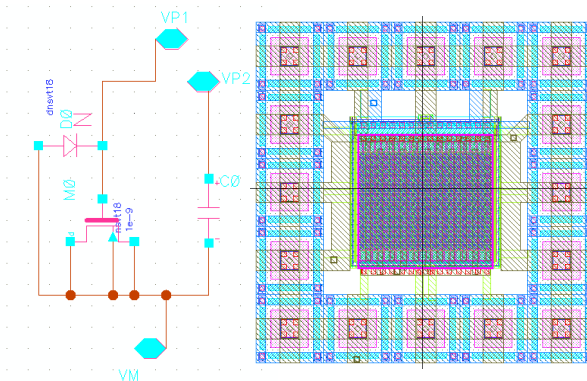
Figure 184: Mesh Double Decoupling Capacitor Extended cell (C$_{dec1}$=240 fF (from VP1 to VM), C$_{dec2}$=212fF (from VP2 to VM))

Figure 185 and Figure 186 show the VCO and ILFD TOP schematics, respectively, including all the decoupling capacitors, required for LVS comparison. The blocks named "*Control lines*" are high value resistances implemented with poly silicon resistors, used for connecting the circuit terminals of bias signals to the PADs, to prevent ESD damages.
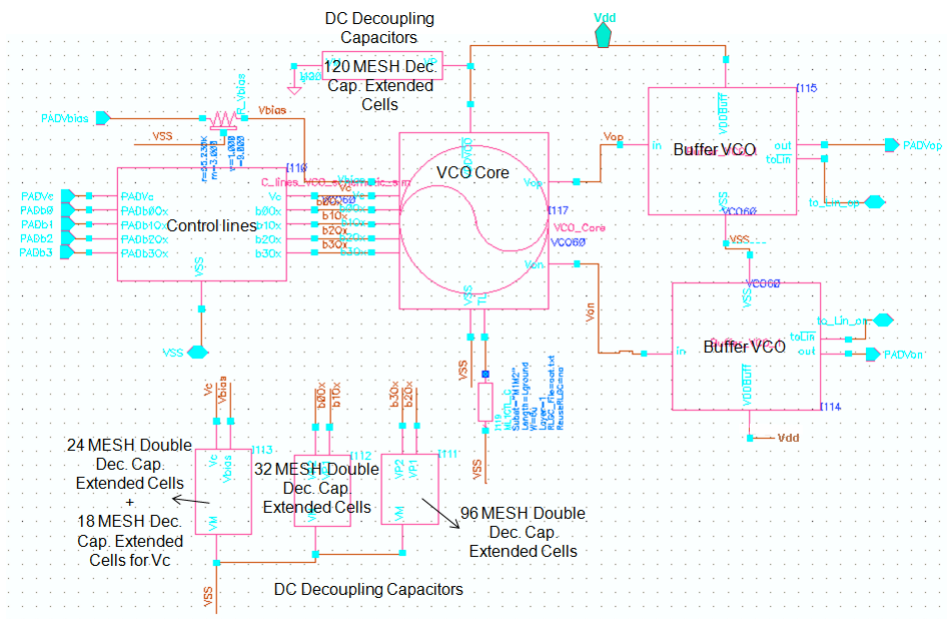
Figure 185: VCO TOP schematic

# and type of Dec. Cap. Extended	Signals
100 MESH Double	Vdd_ILFD and Vdd_Buff_ILFD_A
95 MESH Double	Vbias_Inj and Vdd_Buff_ILFD_B
50 MESH Double	Vbias_ILFD with b0_ILFD
81 MESH Double	b1_ILFD with b2_ILFD
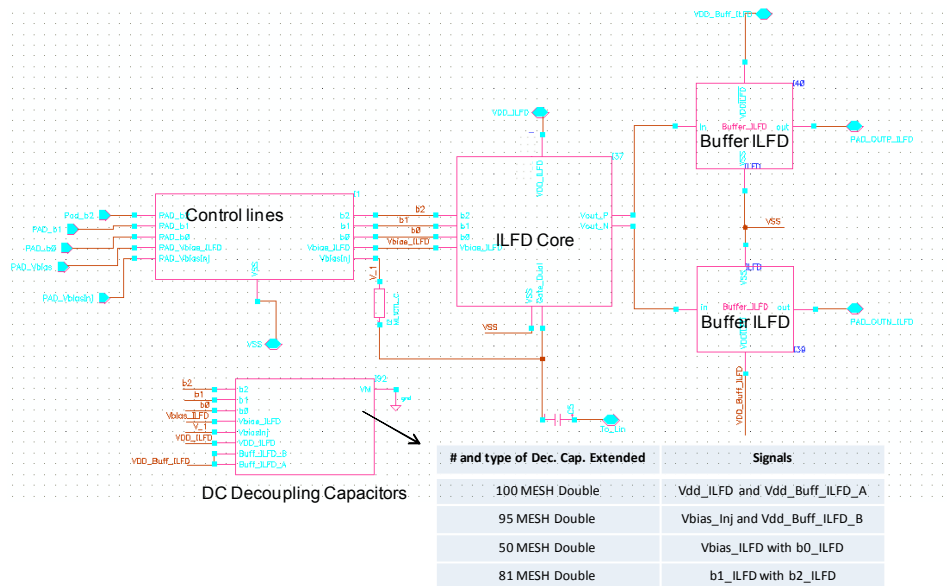
Figure 186: ILFD TOP schematic

In Figure 187 the TOP schematic of the whole test circuit composed by the TOP VCO and TOP ILFD schematics is shown.
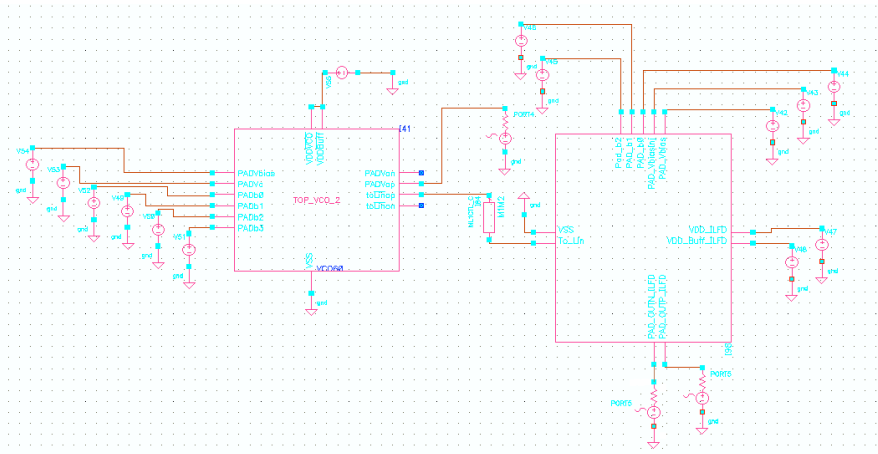
Figure 187: VCO-ILFD TOP schematic

The layout is then completed by adding the seal ring and making several iterations in order to achieve zero Design Rule Check (DRC) violations for density rules. The ST^{TM} logo and the chip reference are also added before sending the chip for manufacturing. It is important for a mm-W IC design to provide the foundry with a layout having NO DRC violations for density rules, in order to avoid the intervention of a third person to complete the dummies generation. This is because only the designer knows the details of the circuit and the misplacement of dummy cells may impact on the correct system operation, especially close or around the transmission lines. For this reason the density rules are fulfilled 'by construction' using regular structures and 'smart' dummy fills (not automatically generated) wherever required. Figure 188 shows the complete TOP layout of the chip.
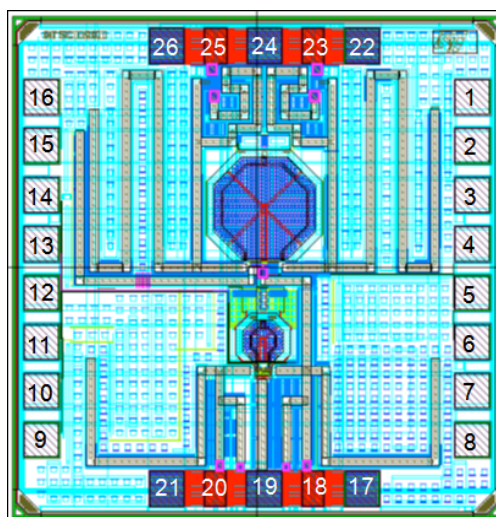
Figure 188: ILFD - VCO TOP layout

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6.4   Final Post-Layout Simulations

In this section, the simulations at top level of the three measurement cases are reported. All the models that have been extracted from the layout with the EM simulator are considered in such simulations.

Once the layout was terminated, a RCc view   extraction (i. e. a extended schematic view that includes the RC parasitics for the interconnections not modelled otherwise, which value is extracted from the layout geometry and the process parameters). This parasitic extraction was done for the overall chip (active and passive devices) before sending the chip for manufacturing, by using StarRCXT from Synopsis. The RCc extracted view is used for a final validation before manufacturing. Only a DC simulation is performed to check that no short circuit or anomalous consumption exist. This view not valid for RF simulation, since the momentum models of the TL lines and other layout structures are not included in this case.

6.4.1   VCO ON - ILFD OFF

In this simulation case, the ILFD is turned OFF; that is all the ILFD supplies and bias voltage are connected to ground. The test bench circuit for this case is shown in Figure 189.
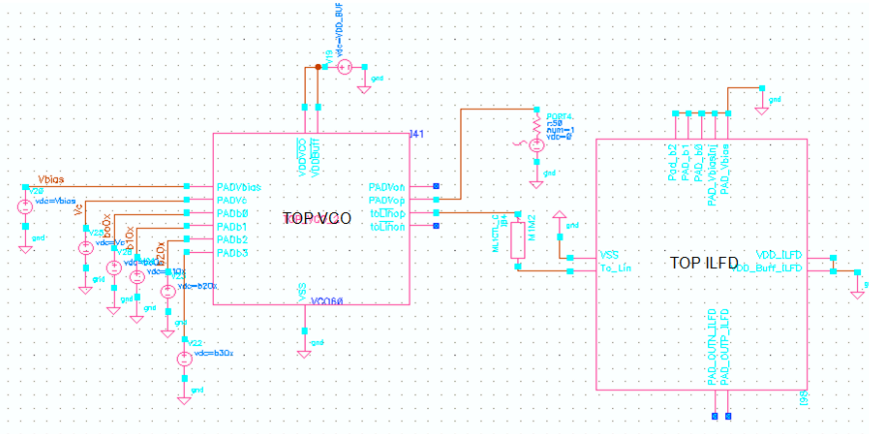
Figure 189: VCO ON - ILFD OFF. Test bench circuit

The same DC source (at PAD 7 in Figure 188) is providing the VCO core and its output buffers with voltage supply (i. e., 1.2V). The VCO bias voltage V_{bias} VCO is 715 mV (at PAD 14 in Figure 188). Figure 190 shows the VCO current consumption of the top layout RCc extraction view, considering a V_{bias} sweep from 0 to 1.2V, for a fixed voltage supply of 1.2V. Note that, as

already mentioned, this current corresponds to the VCO core and output buffers.
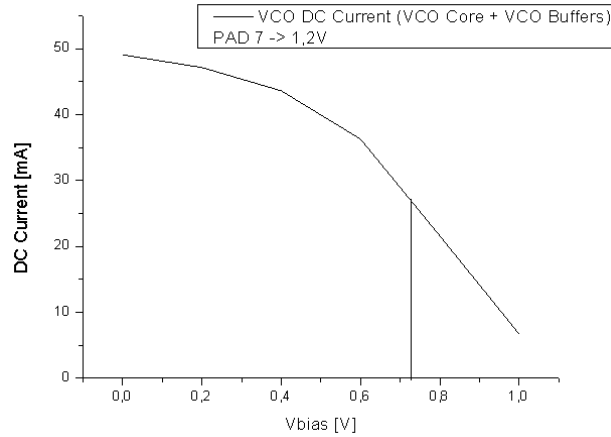
Figure 190: VCO DC current consumption (RCc extraction of the top layout)

The result of Figure 190 is very similar to the DC current consumption achieved from the circuit level simulation. The overall VCO DC current consumption for 1.2 V voltage supply is 28.36 mA, corresponding to 12.66 mA of VCO core plus the 7.85 mA of each buffer, according to the values found previously in 6.1.2. and 6.2.2.

HB simulation with noise analysis is now performed for the test bench of Figure 189, in which all the post-layout models from EM extractions are considered. The single-ended VCO output considered is at the VCO output buffer V_{op} (i. e., the PAD 18 in Figure 188). This PAD corresponds to the output buffer branch that is connected to the ILFD input stage.

In Figure 191 the VCO frequency curves and the phase noise are reported. In order to centre the tuning curves in the WirelessHD[TM] band, a residual contribution of C_F equal to 3 fF is still considered in the VCO load, connected at the buffers inputs. That is, the differential capacitance contribution provided by the output buffers is not enough in order to eliminate completely the available budget for parasitic capacitance C_F that was considered as design margin during the VCO transistor level design. In this conditions the VCO tuning range, taking into account the continuous and coarse tuning mechanisms, is from 54.42 GHz to 66.4 GHz, as shown in Figure 191 (left). Otherwise the overall tuning range, for a $C_F = 0$, is from 55.8 GHz to 66.9 GHz. A VCO tuning range > 19.8% is achieved and the overall bandwidth available for PVT variations compensation is higher than the 70% of the band of interest.
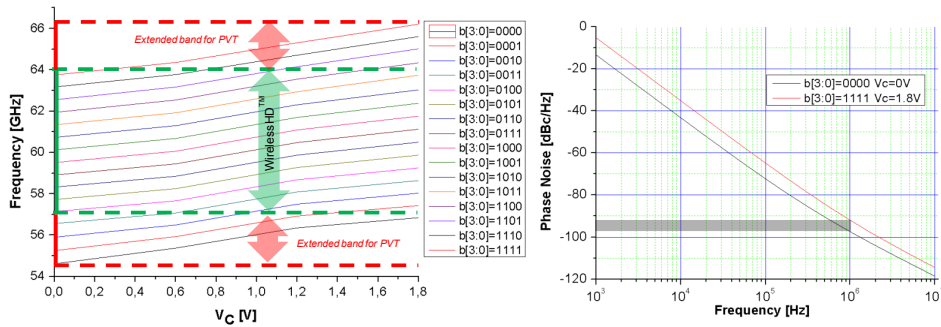
Figure 191: VCO tuning range (left). VCO Phase-noise at Δf=1 MHz (right)

The VCO phase-noise for a frequency offset Δf of 1 MHz from the carrier varies from ≈ -92 dBc/Hz to ≈ -98 dBc/Hz, depending on the output frequency.

Figure 192 shows the single-ended output waveforms of the VCO circuit (after the buffer) on a 50 Ω load, for different coarse tuning codes b[3:0] and control voltages V_C. The single-ended VCO output amplitude available for measurement varies from ≈ 150 mV (-6.5 dBm), corresponding to the lowest VCO frequency, for b[3:0] = 0000 with V_C = 0V, to ≈ 205 mV (-3.7 dBm), for the highest VCO frequency, obtained by coarse tuning code b[3:0] = 1111 with V_C = 1.8V.
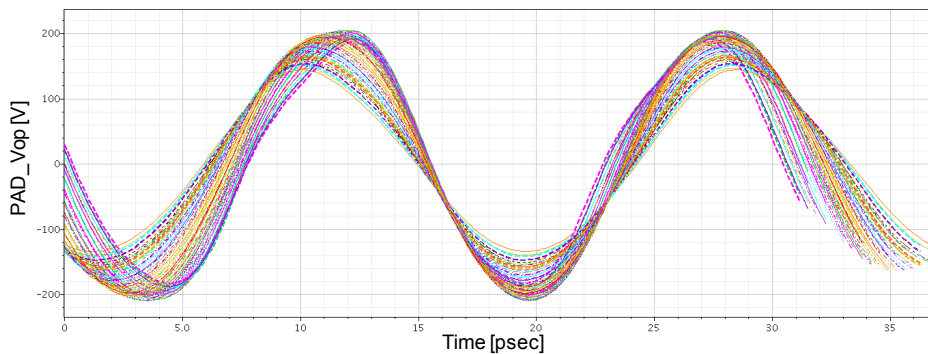
Figure 192: VCO single-ended output waveforms

As summary, the available power range, delivered to 50 Ω, is from ≈ -6.5 dBm to ≈ -3.7 dBm, as depicted in Figure 193. Table 9 summarizes the performance of the VCO.
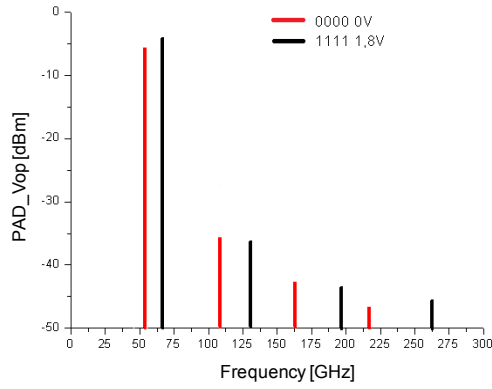
Figure 193: VCO single-ended output spectrum

V_{supply} (PAD 7) [V]	1.2
V_{bias} (PAD 14) [mV]	715
Current consumption [mA]	12.66 (VCO core)
	7.85 (Buffer)
	28.36 (VCO core + 2 Buffers)
Tuning range [GHz]	**54.42-to-66.4 (19.83%)**
Output Amplitude (single-ended, PAD 18) [dBm]	**-6.5 (min) -3.7 (max)**
Phase Noise (Δf = 1 MHz) [dBc/Hz]	**-98 (min) -92 (max)**

Table 9: VCO post-layout simulation data. C_F = 3 fF

6.4.2 VCO OFF - ILFD ON

In this simulation case, the VCO is turned OFF; that is all the VCO supplies and bias voltage are connected to ground. The test bench circuit for this case is shown in Figure 194.
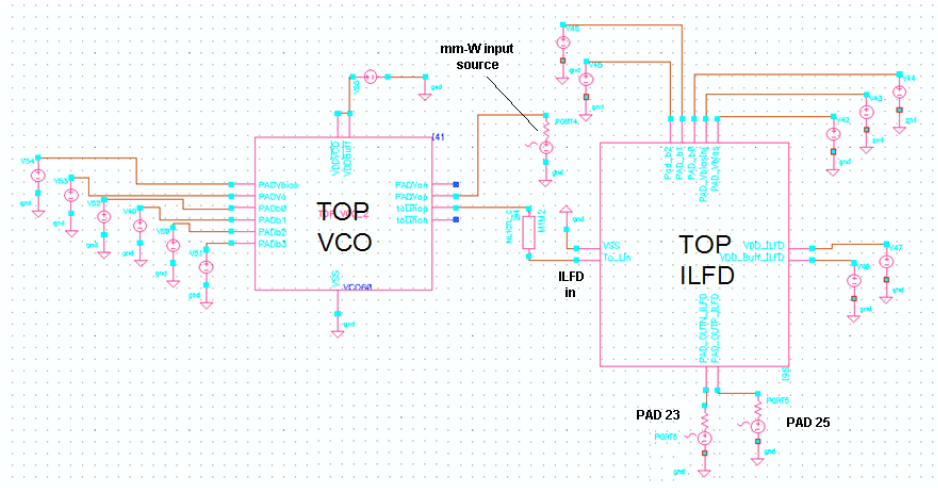
Figure 194: VCO OFF - ILFD ON. Test bench circuit

Figure 195 shows the ILFD core and buffer current consumptions (for both buffers the current consumption is the same) of the top layout RCc extraction view, considering a V_{bias_ILFD} sweep from 0 to 1V, for a fixed voltage supply of 1.2V and for different V_{bias_Inj} values.
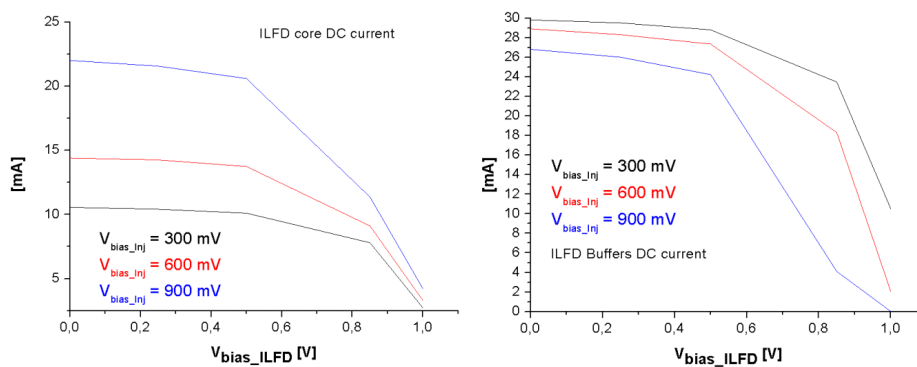
Figure 195: ILFD DC current consumptions (RCc extraction of the top layout)

The results of Figure 195 are very similar to the DC current consumption achieved from the circuit level simulation.

The differential ILFD output is balanced, hence both ILFD single-ended output PAD could be considered in measurements. For the test bench of Figure 194, in which all the post-layout model from EM extractions are considered, HB simulation with noise analysis are performed in order to achieve the ILFD free-running tuning range and input sensitivity curves.

a) Free-running operation

The ILFD tuning range, obtained by considering its self-resonance frequencies depending on the ILFD coarse tuning codes b[2:0], and its phase noise in free running state are shown in Figure 196. In this situation, no signal is injected into the ILFD.
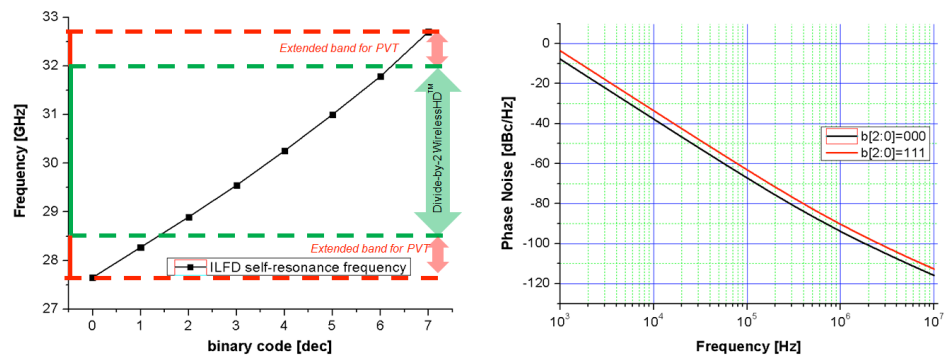
Figure 196: ILFD free-running state. Self-resonance frequencies (left). Phase Noise (right)

The ILO self-resonance frequencies vary from 27.6 GHz to 32.55 GHz. This results in a tuning range of ≈ 16.45%. The ILFD output buffers insertion spends completely the available budget for C_F found in 6.1.3, as expected after the result reported in Figure 174 (right). Figure 197 shows the ILFD output waveforms in its self-oscillating state, corresponding to the eight combinations of the coarse tuning code b[2:0].
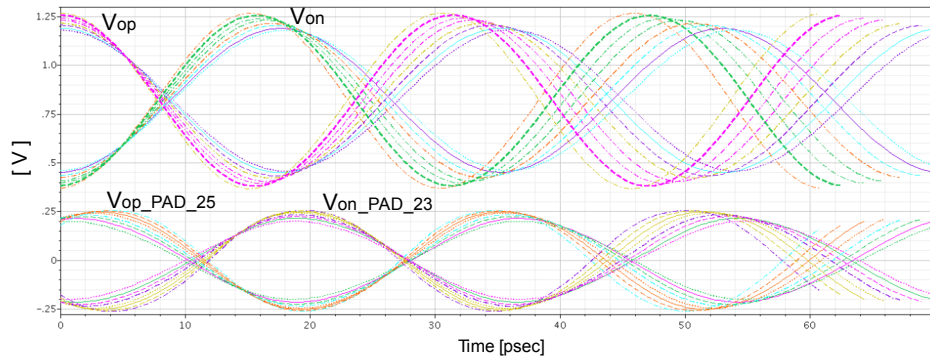
Figure 197: ILFD waveforms in free running

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V_{op} and V_{on} are the ILFD core single-ended outputs, which are the input signals of the ILFD buffers. The other two signals plotted are the output signals of the ILFD buffers, which are the ILFD single-ended output signals available for measurements at PAD 23 and 25. As it is possible to note, it results in a differential balanced ILFD output. The single-ended ILFD output amplitude available for measurements in 50 Ω environment varies from 201 mV, corresponding to the lowest ILFD self-resonance frequency, for b[2:0] = 000, to 256 mV, related to the highest self-resonance frequency, for b[2:0] = 111. It results in an available power range, delivered to 50 Ω, from ≈ -3.9 dBm to ≈ -2 dBm, as depicted in Figure 198.
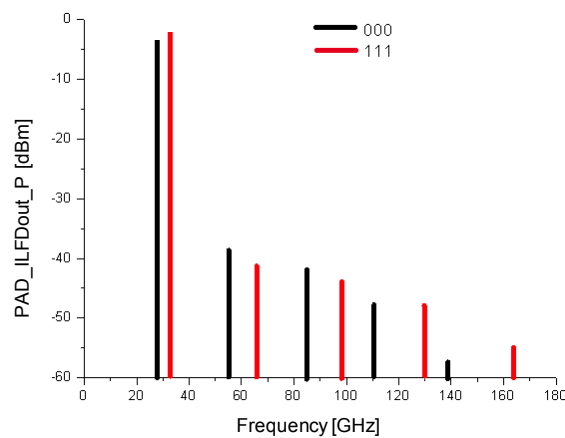
Figure 198: ILFD output spectrum in free running state

b) Injection-locking operation

The next step consists in evaluating the ILFD locking state when the 60 GHz input signal is injected from an external source. The mm-W input signal is injected from PAD 18, which is also the VCO single-ended output PAD when the VCO is ON. This is achieved by replacing the DC 50Ω-Port (in which the DC level is set to 0V) of the schematic of Figure 189, with a RF 50Ω-Port, as depicted in the test bench of Figure 194.

The ILFD input sensitivity curves are built by sweeping the amplitude and frequency of the input source and changing the ILFD coarse tuning codes, determining the minimum signal power required for each input frequency to lock the ILFD. Figure 199 shows some ILFD waveforms when the injection locking is reached. V_{inj} is the signal injected into the ILFD at $f_0 ≈ 60$ GHz, at its input terminal, that is at "*ILFD in*" in the schematic of Figure 194, which is an internal node of the circuit. V_{op} is the signal injected from the input source on PAD 18, at the same f_0 as well. V_{ILFD_op} is the ILFD output signal, exactly at $f_0/2$.
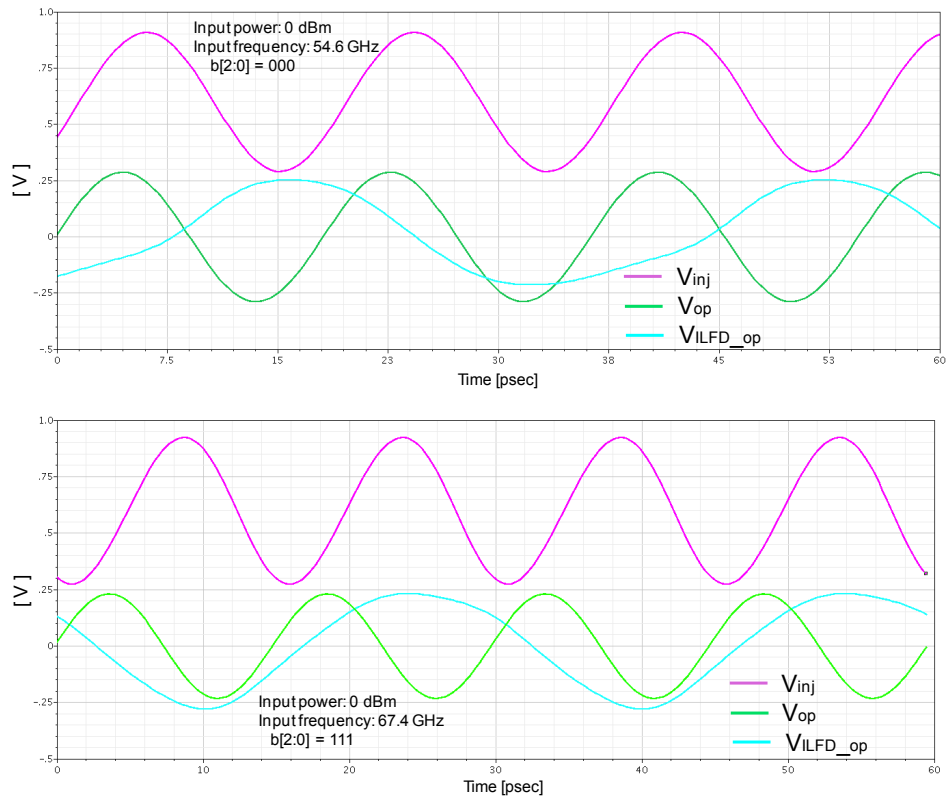
Figure 199: Divide-by-two ILFD waveforms in locking condition

Figure 200 shows the ILFD input sensitivity curves achieved. The input power injected into the ILFD is referred to the effective amplitude of V_{inj}. From simulation results it has been calculated that 1.6 dBm at 54.6 GHz and 2 dBm at 67.4 GHz are needed as the port available power in order to obtain an operating power at the ILFD input of 0 dBm. This is due to the mismatching existing between the port impedance (50 Ω) and the internal injection pin input impedance. The achieved ILFD dividing-by-two range corresponding to 0 dBm input power, is from 54.6 GHz to 67.4 GHz, taking into account the ILFD tuning mechanism, which results in an overall ILFD dividing range of ≈ 21%.
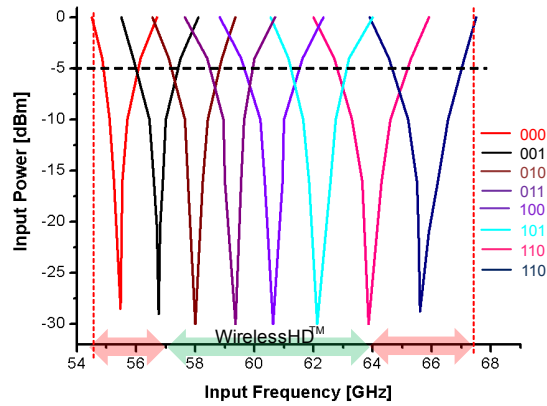
Figure 200: Divide-by-two ILFD input sensitivity curves

From the analysis of the overlapping between adjacent sensitivity curves in the plot of Figure 200, the ILFD is able to divide properly, by using the tuning mechanism, all the input signal with a power < - 5 dBm for a frequency range from ≈ 55.2 GHz to ≈ 66.5 GHz, which results in a dividing range of ≈ 18.5 %, related to such input power. The ILFD extended dividing range, available for PVT compensation, taking into account 0 dBm of input power, is estimated in ≈ 83% of the band of interest.

In the next Table 10 the performance of the divide-by-two ILFD is summarized.

V_{supply_core} (PAD 2) [V]	1.2
V_{supply_Buff} (PAD 1 and PAD 16) [V]	1.2
V_{bias} (PAD 3) [mV]	850
V_{bias_Inj} (PAD 15) [mV]	600
I_{DC_core} [mA]	9
$I_{DC\_Buffers}$ [mA]	9.15 x 2
Tuning range (free-running) [GHz]	27.6-to-32.55
Output Amplitude (single-ended, PAD 23 or 25) [dBm]	-3.9 (min) -2 (max)
Phase Noise (Δf = 1 MHz, free-running) [dBc/Hz]	-89.5 (min) -92.4 (max)
Dividing range [GHz]	54.6-to-67.4 (21%) 0 dBm Input Power

Table 10: Divide-by-two ILFD post-layout simulation data

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In the next sub-section the injection signal is provided directly by the 60 GHz VCO. The sensitivity of the ILFD is so tested with the power and frequency provided by the VCO, so that only the coarse tuning codes of both ILFD and VCO and the control voltage of the VCO can be varied in order to get injection locking.

6.4.3   VCO ON - ILFD ON

In this simulation case, both the VCO and the ILFD are turned ON; that is all the VCO and ILFD supplies and bias voltages are set their nominal values. The test bench circuit for this case is shown in Figure 201.
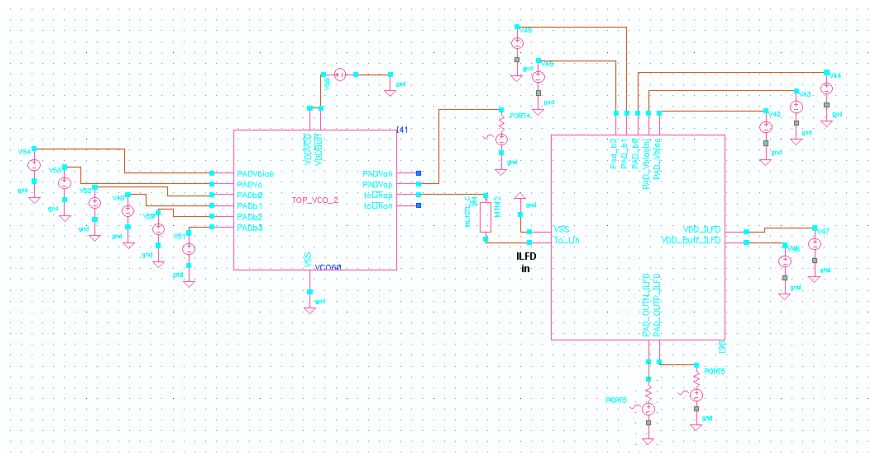
Figure 201: VCO ON - ILFD ON. Test bench circuit

The RF 50Ω-Port used in the schematic of Figure 194 at the single-ended VCO output considered for injection, i. e., at PAD 18, is now replaced in the schematic of Figure 201 with a 50 Ω load, i. e., a DC 50Ω-Port (its DC value is set to 0V). The DC values of the top circuit in this situation, i.e. the VCO and ILFD current consumptions including their output buffers, are the same that have been achieved in 6.4.1 and 6.4.2, for the stand-alone VCO and ILFD, respectively. Figure 202 shows the plots which report some VCO and ILFD waveforms, corresponding to the injection locking state reached. They are related to different coarse tuning codes, of both the ILFD and VCO, and the control voltage V_C of the VCO for fine tuning. When the VCO is operating at f_{VCO}, it forces the divide-by-two ILFD output frequency to move itself towards exactly $f_{VCO}/2$, if the VCO injected power is enough to lock the ILFD, achieving in this way the division-by-two operation. Simultaneously, it is important to set the ILFD self-oscillating as close as possible to $\approx f_{VCO}/2$, by using the appropriate binary code for coarse tuning. As farer is the ILFD self-resonance frequency from $f_{VCO}/2$, as wider is the ILFD sensitivity, if the division-by-two is achieved.
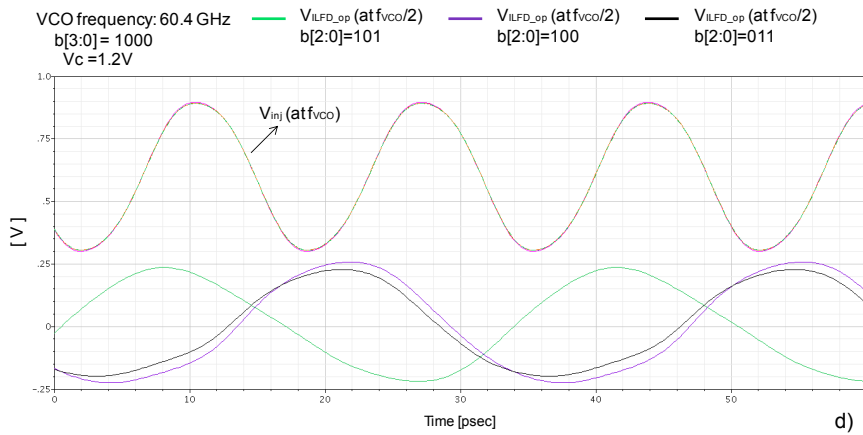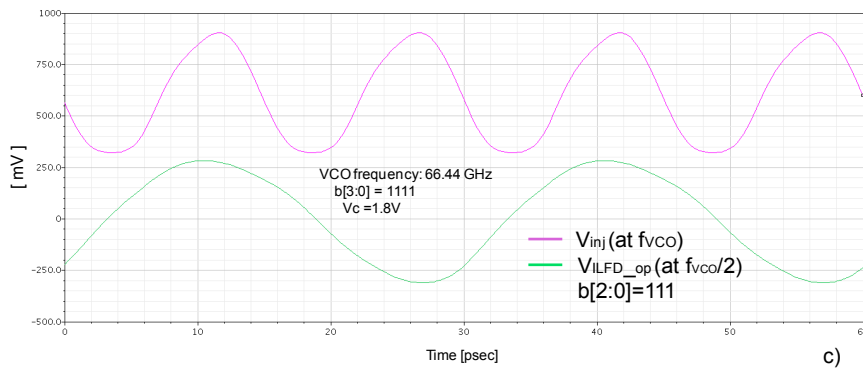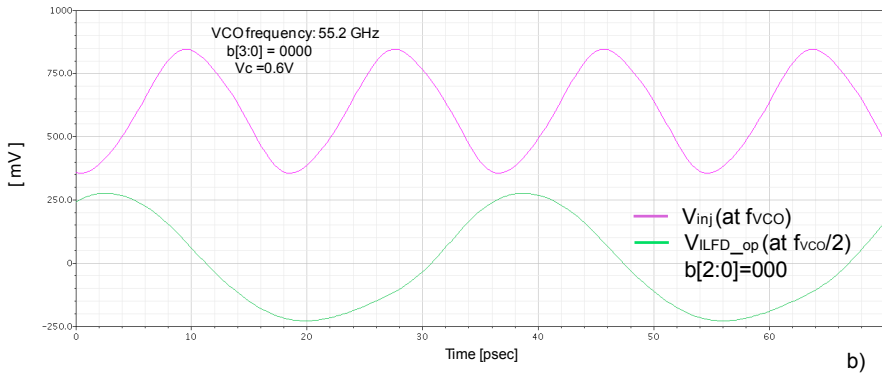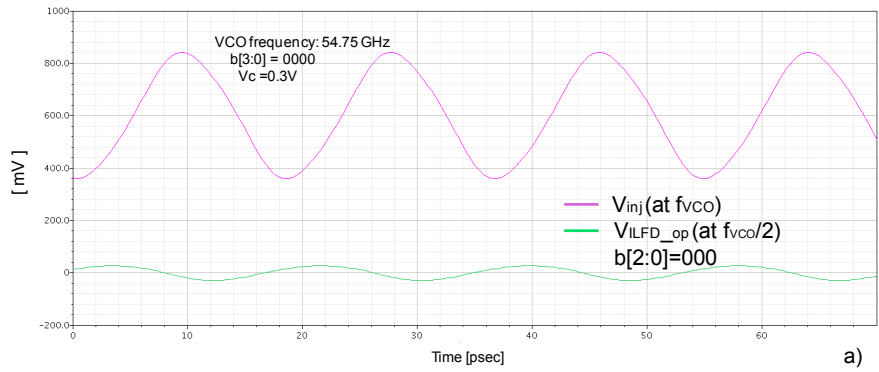
Figure 202: ILFD - VCO waveforms in locking condition

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A C_F = 3 fF is considered between the input of the VCO buffers. V_{inj} is the mm-W signal, generated by the VCO, hence at f_{VCO}. Such signal is injected into the ILFD, at its input terminal, proceeding from the VCO output buffer. As it is possible to observe from all the plots reported in Figure 202, the VCO injection signal amplitude increases with the VCO frequency.

V_{ILFD_op} is the ILFD single-ended output at its buffer output, i.e., at PAD 23 or 25 since the ILFD differential output is balanced. Such signal is at $f_{VCO}/2$, since the injection locking is reached.

Considering Figure 202(a), the amplitude of V_{ILFD_op}, is so small ($\approx$ 27 mV) in the case of the lowest VCO frequency division (f_{VCO} = 54.75 GHz) basically for two reasons: firstly because the ILFD buffer is strongly attenuating the signal below 28 GHz, as can be observed in Figure 175. Secondly because that higher losses should be compensated at this frequency in order to allow the ILFD to oscillate, i. e. a lower equivalent parallel losses of the ILFD tank R_{peq} is observed at this frequency, as illustrated in Figure 122 (right). That is, such frequency is lower than the ILFD self-resonance frequency f_{self} corresponding to the ILFD code b[2:0] = 000. In other words, the g_m of the ILFD cross-coupled pair is at the limit in order to satisfy the start-up oscillation condition, dictated by (15). This results in a low forced oscillation amplitude. As the VCO frequency is slightly increased, see Figure 202(b), $f_{VCO}/2$ is approaching f_{self} and consequently the ILFD output amplitude is higher, similar at the expected value. The ILFD output amplitude dependency on the injecting frequency f_{VCO} and f_{self} is also reflected in Figure 202(d). In this plot the same VCO frequency f_{VCO}=60.4 GHz, in the centre of the WirelessHD[TM] band, is divided-by-two using three different ILFD codes. Note that for these three cases V_{inj} is the same, since the VCO coarse tuning code and V_C are not changed. When the ILFD code is set to b[2:0] = 100, the ILFD output amplitude is higher. In this case f_{self} is $\approx$ 30.25 GHz. A similar ILFD output amplitude, but slightly lower, is achieved for the code b[2:0] = 101, when the ILFD self-resonance frequency is $\approx$ 31.2 GHz . The lowest ILFD output amplitude is found for a ILFD code b[2:0] = 011, i.e. when f_{self} is lower than $f_{VCO}/2$. As a summary, the ILFD output amplitude in locking condition depends on how far away is f_{self} from $f_{VCO}/2$. This effect is emphasized if $f_{VCO}/2 < f_{self}$. The remaining plot of Figure 202(c) depicts the VCO and divide-by-two ILFD waveforms corresponding to the locking condition achieved at the upper extreme of the VCO tuning range.

Figure 203 shows a picture in which the overall ILFD sensitivity curves are reported, taking into account the VCO frequency and output power injected into the divider in the VCO ON - ILFD ON case. The VCO amplitude is related to V_{inj} and it corresponds to the VCO frequency continuous ranges of the sixteen VCO binary codes b[3:0]. For simplicity of the illustration, the amplitude of the VCO is assumed to be the same for the each coarse tuning code.
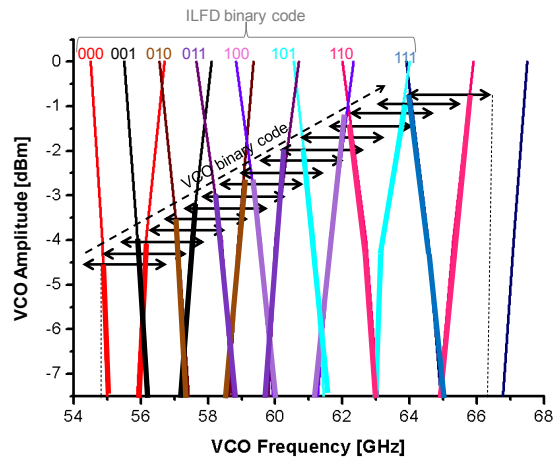
Figure 203: VCO-ILFD sensitivity

The ILFD, with the discrete tuning mechanism, is able to divide-by-two the VCO frequencies across almost all its discrete and continuous tuning range. The division is not achieved for the lower VCO frequency range, where the injected power is lower. The ILFD can track the VCO from 54.9 GHz to 66.44 GHz, by changing the coarse tuning codes. Figure 204 shows the VCO phase noise, when the ILFD is injection locked. In this case, the VCO phase noise obtained at the ILFD single-ended output (i.e. PAD 23 or 25), which is oscillating exactly at $f_{VCO}/2$, is ≈ 6 dB lower, if compared to that measured at the VCO output (PAD 18), according to:

$$PN\left(\Delta f\right)_{VCO} = PN\left(\Delta f\right)_{ILFD} + 20\log\left(2\right) \qquad 22)$$

being the division factor equal to 2.
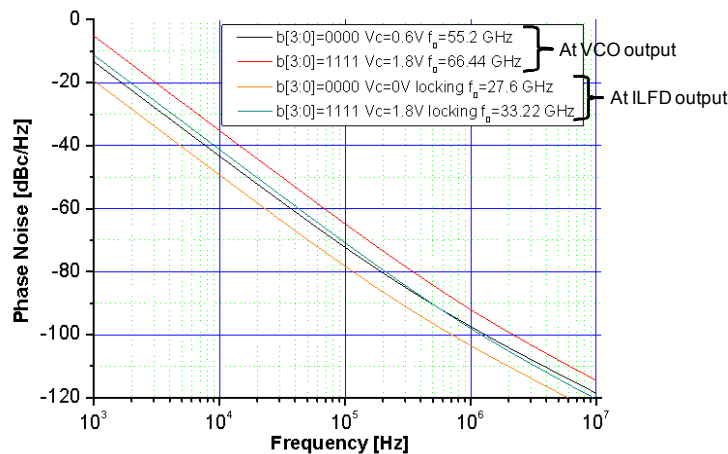
Figure 204: VCO phase noise in ILFD locking condition

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Next Table 11 summarizes the performance of the test circuit corresponding to VCO ON - ILFD ON. Regarding the DC values and bias settings, they are the same exposed in Table 9 and Table 10. For the ILFD dividing range, very low ILFD outputs amplitudes have not been considered.

VCO Tuning range [GHz]	54.42-to-66.4
VCO Injected amplitude [dBm]	-4.5 (min) ; -0.95 (max)
ILFD dividing range [GHz]	54.9-to-66.4 (18.9%)
ILFD Output Amplitude (single-ended) [dBm]	-3.2 (min) ; -2 (max)
Power Consumption (VCO+ILFD) [mW]	66.8

Table 11: VCO-ILFD post-layout simulation data

6.5   Conclusions

In this chapter the 60 GHz VCO and divide-by-two ILFD co-design has been completed and the test chip is finished to be ready for manufacturing. The resulting chip area is 1 mm^2, PADs included. Departing from this finished layout, the corners, i. e. PVT variations, analysis is performed and presented in the following chapter.

The results from post-layout simulations indicate that a low-noise, wide tuning range LC-VCO with a low-power, wide locking range divide-by-two LC-ILFD can be designed in a 65 nm CMOS process, for operation at 60 GHz inside a PLL for direct-conversion transceiver compatible with WirelessHD^{TM} applications.

The VCO tuning range obtained with both discrete and continuous tuning mechanism is found to be > 19.8%, centred around 60 GHz. Its power consumption is ≈ 34 mW, output buffers included, from 1.2 V supply voltage. The VCO phase noise at 1 MHz of frequency offset is < -92 dBc/Hz.

The overall dividing range of the 60 GHz divide-by-two ILFD is > 20 %, taking into account the discrete tuning of its self-resonance frequency, for an input power of 0 dBm. This is a very wide dividing range achieved around 60 GHz, if compared to the state-of-art reported in the bibliography of this Thesis. The overall ILFD power consumption is ≈ 32.8 mW, output buffers included, from 1.2 V supply voltage.

When the VCO is used as input source in the test circuit, the power consumption of the overall test circuit is 66.8 mW, output buffers included, from 1.2 V supply voltage. The dividing range of the ILFD, taking into account the

discrete tuning of both VCO and ILFD and the continuous tuning of the VCO, is ≈ 18.9%. The ILFD is not able to track the lower VCO frequency range for typical conditions. Such frequency range corresponds to a 4% of the VCO tuning range, but it is outside the band of interest.

The test prototype has been designed such that each of the two blocks, i. e. the VCO and the ILFD, can be measured in their stand-alone configuration or both operating together (the VCO providing the ILFD with input signal, like in a PLL). Hard design challenges have been faced up, specially at layout level, in order to properly distribute the 60 GHz signal and complete the compact layout that fits in the 1 mm^2 area constraint.

Critical and long design processes have been required for EM extractions, passive devices modelling and post-layout simulations. They are needed in order to reach a proper reliability for manufacturing. As abovementioned, the models of some devices used in the circuit design, which are provided by the foundry, are qualified up to 40 GHz. Therefore, also the accuracy and correctness of the EM modelling will be verified by the experimental results, which are exposed in Chapter 8.

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7   PVT VARIATIONS SIMULATION AND CALIBRATION TECHNIQUE

7.1   Introduction

In this chapter the simulation of the PVT variations in the overall design, i. e. the VCO plus ILFD configuration, is carried on.

Regarding process variations, the process corners for transistor models TT, FF, FS, SF and SS provided by the foundry are considered. These corners are defined by respect to the NMOS and PMOS transistors, as described in 3.3. Simultaneously, for each corner, a supply voltage variation of ± 5% from its nominal value of 1.2V is considered. Concerning temperature variations, in addition to the nominal 27º, 0ºC and 105ºC are also considered as operation temperatures for each corner and each supply voltage. Note that the typical corner for the simulation of the design, considered until now, consists in process corner TT with a supply voltage of 1.2V at a temperature of 27ºC. As a consequence, 27 cases (3x3x3) have been considered to achieve the MIN, TYP and MAX corners of the whole design. From these 27 cases, the more constraining corners sets are selected, as discussed in the next section. Regarding passive devices, i. e. inductors and varactors, they also present process corners (MIN, TYP and MAX) if the DK models are considered. The models of the inductors used in the PVT variations simulation are those extracted from EM simulation, and it has been already observed (see sub-section 6.1.1) that the variations in their characteristics due to the available substrate corners are very small. Regarding varactors, the corner considered in the simulations is TYP, since it has been checked that very small variations in the tank resonance frequency (< 0.6% and < 0.35% for the VCO and ILFD, respectively) correspond to MIN and MAX corners (this is because the varactors used in the design present very low capacitances).

PVT variations impact in the operation of the stand-alone VCO and ILFD circuits is important, but the most critical issue is if there is a correlation between the amount and sign of the variation of the VCO frequencies and ILFD self-oscillation frequencies for the different PVT cases, since both need to operate together, the VCO providing the ILFD with input signal. For a PLL

architecture that allows frequency calibration of the VCO and the ILFD circuits, a simplest approach would be possible if both vary with PVT in the same direction. Therefore, the overall system VCO+ILFD is considered in the PVT analysis. All the simulations are performed taking into account the extracted models from Momentum for inductors, layout interconnections and transmission lines.

7.2 Simulation Results for MIN, TYP and MAX Corners

All possible combination of process corners for active devices, as well as temperature and voltage corners are grouped in such a way that three global PVT corners are defined. They are shown in the next Table 12 and named FMIN, FTYP and FMAX PVT corners:

	PVT [FMAX]	PVT [FTYP]	PVT [FMIN]	PVT [FMIN*]
P	FF	TT	SS	SS
V$_{DD}$	1.26V	1.2V	1.26V	1.14V
T	0ºC	27ºC	105º	105º

Table 12: Design corners

The criteria to establish FMIN and FMAX corners has been, respectively, for which PVT combination the minimum f_{min} (i. e. the lower end of the VCO and ILFD tuning curves) and the highest f_{max} (i. e. the highest end of the tuning curves) are achieved. The passives process corner has been fixed to TYP in all the cases. Note that in this design most of the passives (i. e. inductors, TLs and layout interconnections) are modelled using EM extracted models. It has been shown in Chapter 4, sub-section 6.1.1, that the impact of changing the process corner for such passives structures is very small. Since using different EM models for each corner complicates significantly the simulation database, the same model for passives has been used in all the cases, obtained with the substrate definition corresponding to the typical process corner.

In the case of the corner indicated as FMIN*, the oscillation does not start-up for the lower end of the tuning curves of the circuits if the bias voltages are fixed at their typical values. It is necessary to increase the VCO code up to b[3:0] = 0011 with V$_C$=0.6V, and the ILFD code up to b[2:0] =010 for the ILFD. This is due to a low DC current, corresponding to this corner, driving the ILFD and the VCO cores, i. e. 3.2 mA and 6 mA, respectively. This situation prevents the oscillation start-up since not enough negative resistance is available from the cross-coupled NMOS pairs. Hence, the biasing voltage V$_{bias}$ at the PMOSs bias current sources of both the VCO and the ILFD should be decreased down

to 670 mV and 790 mV, respectively, or the supply voltage increased up to 1.26 V (which results in corner FMIN. In this alternative bias condition both circuits operate correctly for all possible coarse tuning codes. A PVT adaptive bias voltage generator such as a constant g_m [1] bias or a circuit as that one reported in [2] could be implemented to overcome the problem related to oscillation star-up in this corner.

In the rest of this chapter the circuits simulated for each corner does not consider a V_{bias} adjusting, except for the tuning ranges characteristics. The following sub-section presents the results of post-layout simulations taking into account the PVT variations, according to Table 12, in order to show if the designed circuits will be able to operate correctly in all situations. Note that the types of results that are reported correspond to both self-oscillating ILFD and VCO, or to the ILFD locked by the VCO.

7.2.1   ILFD-VCO Locking

In the next Figure 205, a plot depicting the frequency shifts of the higher and lower ends of the tuning characteristics, due to PVT variations for both the VCO and ILFD, is shown. Each point in the curve corresponds to the self-oscillation of the ILFD (Y axis) and output frequency of the VCO (X axis). There are two points for each corner corresponding to the f_{min} (i.e. the lower end of the VCO and ILFD tuning curves) and the f_{max} (i.e. the highest end of the tuning curves) for each circuit and PVT corner.
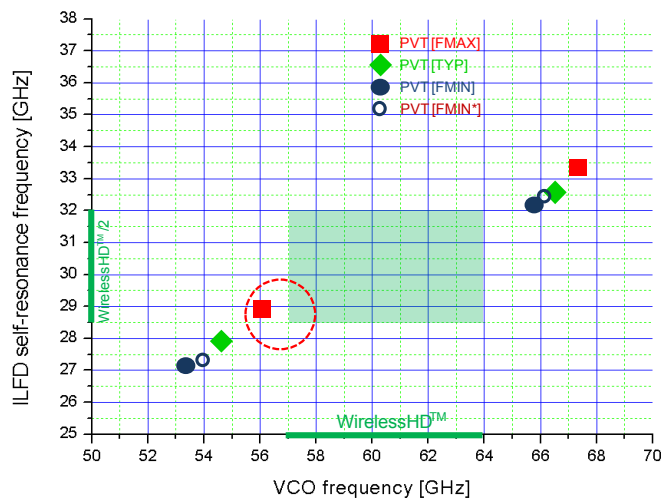
Figure 205: VCO frequencies vs ILFD self-resonance frequencies

The green filled square in the centre of the plot marks the area corresponding to the bands of interest, that are the WirelessHD[TM] band for the

VCO and the divided-by-two WirelessHD[TM] band for the ILFD self-resonance frequencies.

Note that in all process corners the ends of the tuning ranges cover the required bands except for the f_{min} of the ILFD for the FMAX corner (indicated with a dashed line red circle in the figure). However, it is important to take into account that the ILFD is able to lock the VCO output for input frequencies away from its self-resonance frequency. Actually, when the VCO + ILFD simulation is done for this PVT corner the ILFD is able to lock and provide the correct divided by two output for the lower end of the WirelessHD [TM] band, as shown below. The ILFD lowest self-resonance frequency, corresponding to ILFD coarse tuning code b[2:0] = 000 in the FMAX corner is higher than 57/2 = 28.5 GHz. In this case, the VCO is able to generate the lowest WirelessHD[TM] frequency, i. e. 57 GHz, but the lowest ILFD self-resonance frequency is above 57/2 = 28.5 GHz, around 28.9 GHz. It means that the first available ILFD sensitivity curve corresponding to the ILFD code b[2:0] = 000 is centred ≈ 800 MHz inside the WirelessHD[TM] band. For this case, the VCO-ILFD locking is analysed in Figure 206 where some ILFD and VCO waveforms for the VCO frequency around 57 GHz are shown.
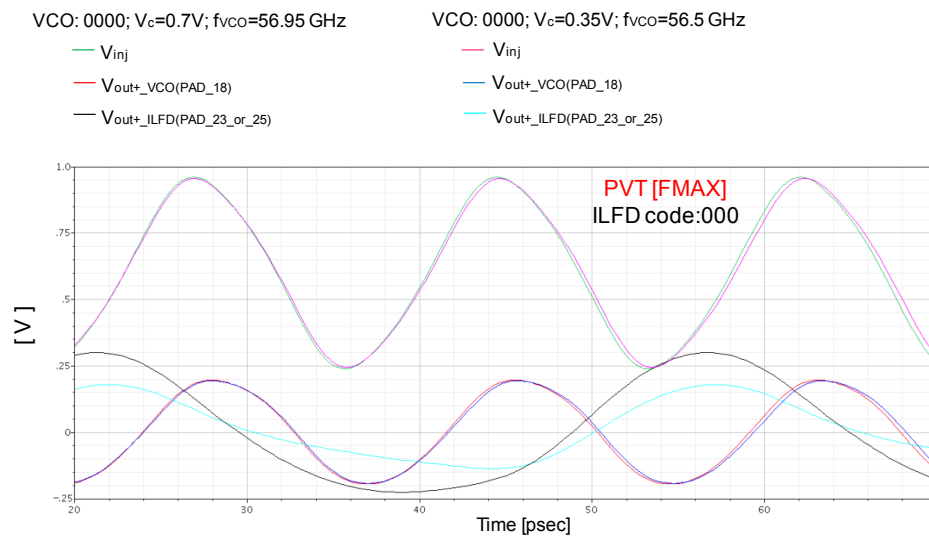
Figure 206: VCO-ILFD locking around 57 GHz, FMAX corner

The VCO and ILFD coarse tuning codes are kept to 0000 and 000, respectively. Two VCO fine-tuning control voltage values of V_C are considered, i. e. V_C = 0.35V and V_C = 0.7V, which leads to a VCO frequency, injected into the ILFD, equal to 56.5 GHz and 56.95 GHz, respectively. In both cases the divide-by-two ILFD is inject-locked by the VCO. Note that the amplitude V_{inj} (i. e. the VCO injection signal at the ILFD input stage) is higher in the FMAX corner if

compared to the FTYP corner (see for comparison the plots in Figure 202(a) and Figure 202(b)). This helps the locking occurrence for this case at lower VCO-ILFD operation frequency range.

On the other hand, even if the FMIN corner is ok from the frequency covering point of view (see Figure 205), the VCO signals amplitudes are lower compared to the FTYP corner. This may compromise the locking of the ILFD when both circuits are simulated together. For this corner weaker VCO signals are injected into the ILFD and it has a critical impact in the overlapping of adjacent ILFD sensitivity curves, reflecting in a lower overall ILFD sensitivity. Nevertheless, one has to note that with the previously explained approach based on an adaptive biasing scheme, that would set a constant DC current for the ILFD and VCO independently of the PVT corner, this problem would be alleviated.

The ILFD dividing range, for to the actual VCO output signal amplitude injected into the ILFD, has been evaluated for the FMIN corner case. Note that in such corner (see Table 12) the supply voltage V_{DD} is 1.26V. In this case the oscillation start-up is achieved for both the ILFD and VCO. FMIN is more critical than FMIN* from the band of interest covering point of view (see Figure 205) and, for this reason, it is analysed deeply in the following. The VCO coarse tuning code b[3:0] and V_C are kept constant to 0000 and 0.6V, respectively. Therefore, the VCO frequency injected into the ILFD is always at 54.55 GHz, while the ILFD code is b[2:0] = 000 and 001. The VCO and ILFD waveforms corresponding to this simulation case are shown in Figure 207.
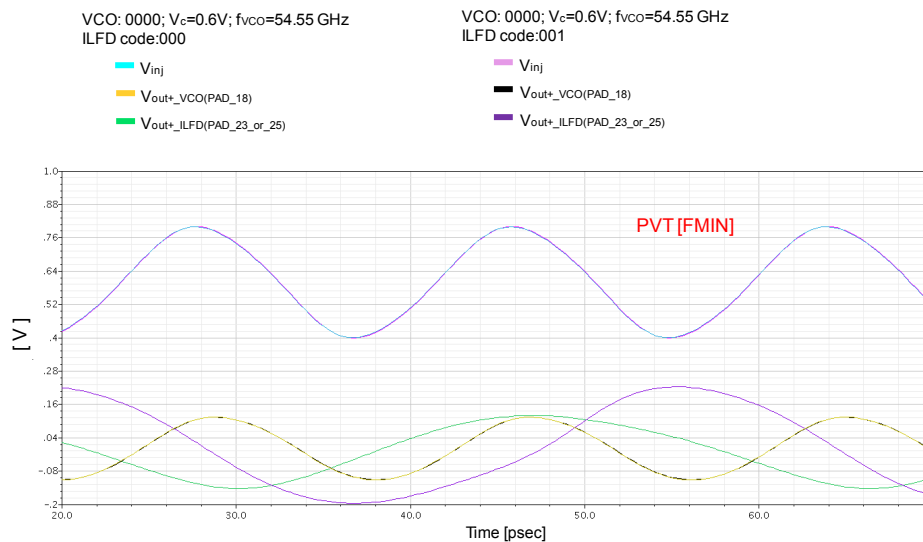
Figure 207: VCO-ILFD locking. FMIN corner

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As it is possible to note, the amplitude of V_{inj} is lower in the FMIN corner if compared to the TYP one (see for comparison the Figure 202(a) and Figure 202(b)). Nevertheless, for this voltage level the VCO signal is able to lock the ILFD in the two adjacent codes b[2:0] = 000 and 001. It means that the VCO output signal amplitude in corner FMIN is enough to avoid a failure operation.

The ILFD sensitivity curves corresponding to the FMIN corner are calculated and plotted in Figure 208. In the same plot, the VCO output signal amplitude injected into the ILFD is also superposed. The figure shows clearly that the available signal amplitude from the VCO for all oscillating frequencies is enough to lock the ILFD in the FMIN corner.
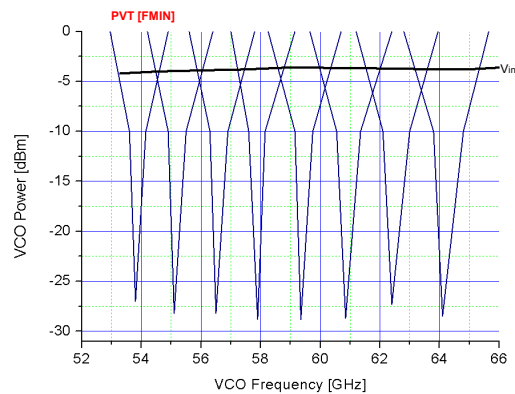
Figure 208: ILFD dividing range: FMIN corner

As a summary, it is important to note that in FMAX corner there is a potential critical operation in the whole system since, even the overall frequencies increase, the tuning ranges of both the VCO and the divide-by-two ILFD are reduced (i.e. the f_{min} is increases more than the f_{max} in both circuits). In this corner case the lowest ILFD self-resonance frequency is higher than 57/2 = 28.5 GHz, so that the lowest WirelessHD^{TM} frequency, i. e. 57 GHz, is $\approx$ 800 MHz away from the centre of the lowest ILFD input sensitivity curve, corresponded to the ILFD code b[2:0] = 000.

On the other hand, in corner FMIN, even if there is no problem from the frequency range covering point of view, the critical issue is determined by the reduced VCO output amplitude that is injected into the ILFD. In such perspective it is justified one of the design goals of this Thesis, i. e. the need of a high sensitivity divide-by-two ILFD (that is an ILFD in which adjacent sensitivity curves cross themselves at a lower as possible input power level). Nevertheless, in both FMIN and FMAX corners, the ILFD and the VCO designed in this Thesis are shown to be able to properly oscillate and divide by two the overall Wireless HD^{TM} band.

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7.2.2   Other Results from PVT Variations Simulation

Once that the VCO-ILFD locking has been analysed in the corners cases, the DC results are now reported in the following Table 13.

	PVT [FMAX]	PVT [FTYP]	PVT [FMIN]	PVT [FMIN*]
V_{DD} (V)	1.26	1.2	1.26	1.14
I_{dc} ILFD (mA)	13.8	8.7	5.9	5.55
I_{dc} VCO (mA)	18.2	12.6	9.8	8.9
$V_{DC\_out\_ILFD}$ (mV)	798	752	825	746
$V_{DC\_out\_VCO}$ (mV)	805	760	840	750
I_{dc} Buff_ILFD (mA)	12.25	8.9	6.1	5.9
I_{dc} Buff_VCO (mA)	11.3	7.78	5.5	5.35
V_{bias_VCO} (mV)	715	715	715	670
V_{bias_ILFD} (mV)	850	850	850	790

Table 13: DC results

Please, note that the results shown in the Table 13 for corner FMIN* correspond to the case in which the biasing voltages V_{bias} of both ILFD and VCO are changed to supply a higher DC current to both circuits, so that oscillation starts-up. Figure 209 reports the ILFD output buffer voltage gain and 50Ω output matching, as results from AC and S-parameter simulations, respectively.
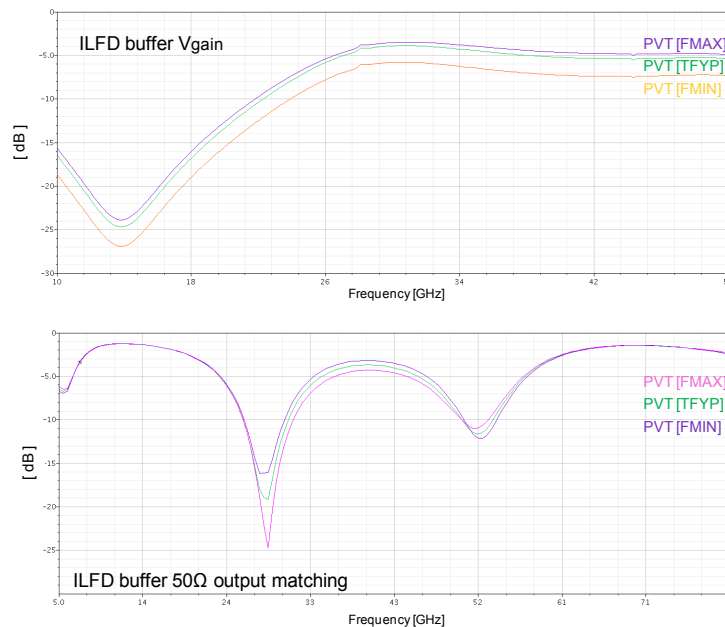
Figure 209: ILFD output buffer: voltage gain (upper), output matching (lower).

In the following Figure 210 the results of the VCO buffer simulation are reported. In the upper plot the 50Ω output matching is shown, while in the medium one the VCO buffer voltage gain V_{out}/V_{in} is considered. This gain is considered at the VCO output single-ended V_{out+} at PAD 18. The lower plot depicts the VCO buffer injection gain, that is the ratio V_{inj}/V_{in}, where V_{inj} is the internal node at the ILFD input stage (in Figure 178 it is the terminal GATE_DUAL after C_{in}).
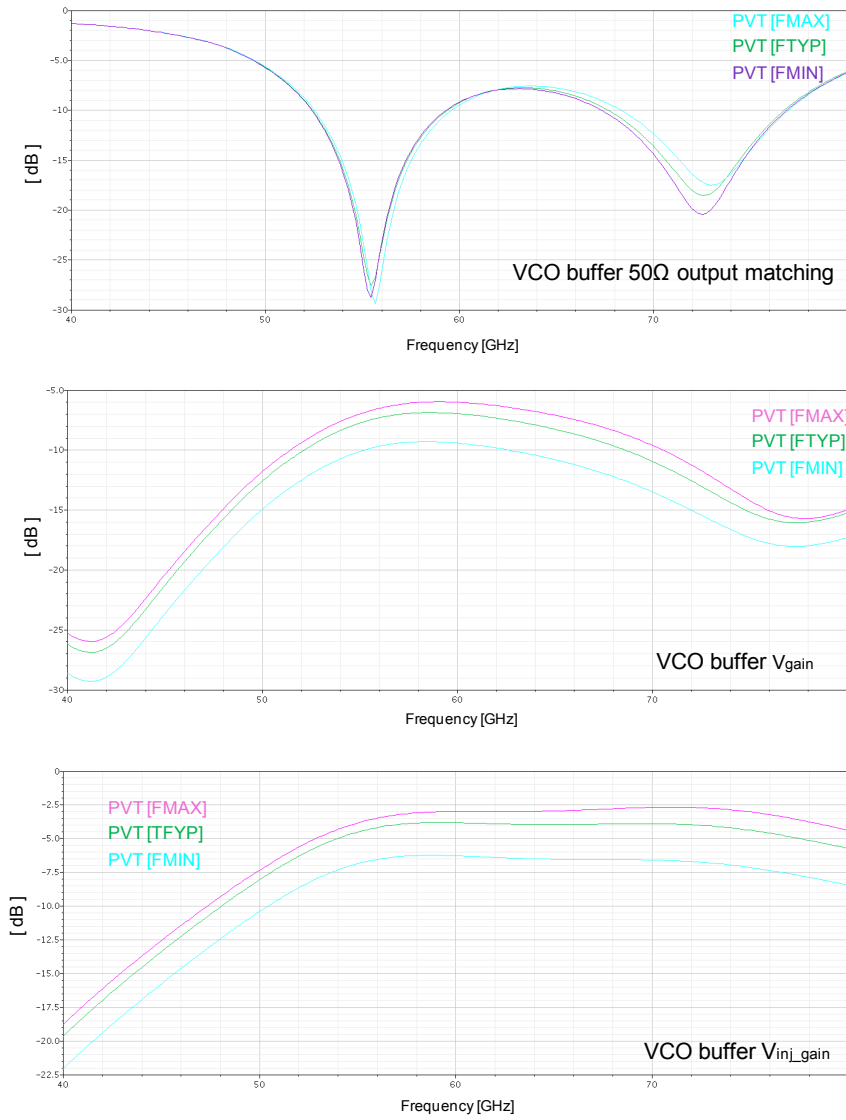
Figure 210: VCO output buffer: output matching (upper), V_{out}/V_{in} (medium), V_{inj}/V_{in} (lower).

Figure 211 shows the VCO phase-noise at 1 MHz of frequency offset from the carrier, considering the central coarse tuning code 1000 for a sweep of the VCO control voltage V_C.
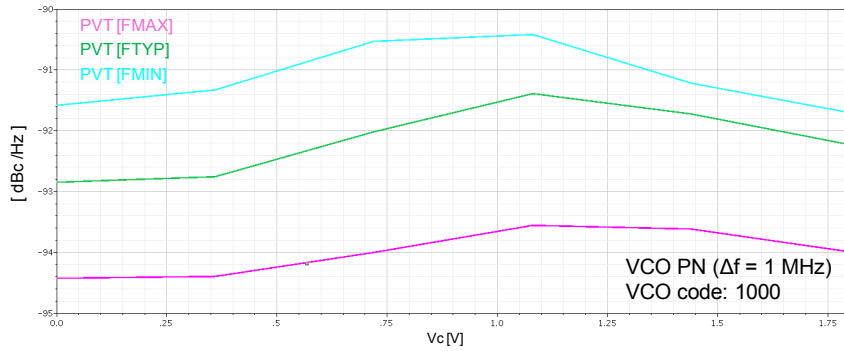
Figure 211: VCO phase-noise

Finally, the ILFD single-ended output amplitude, at PAD 23 or 25, corresponding to the self-running operation state of the ILO are reported in Figure 212.
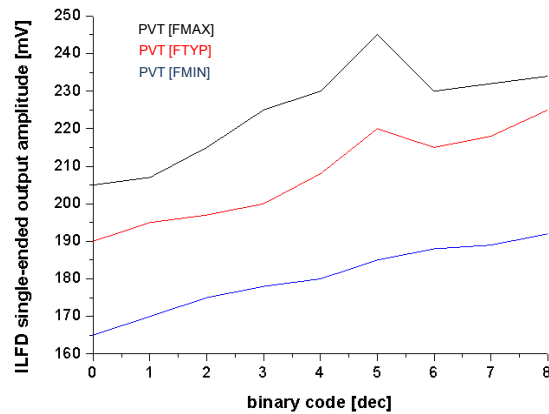
Figure 212: ILFD output amplitude, single-ended, in free-running state

7.3 Calibration Technique

In this sub-section a calibration technique for a PLL, in which the VCO and ILFD presented in this Thesis can be implemented, is exposed.

The most important conclusion that can be drawn from the results of the PVT variations simulation presented in the previous section is that the PVT variations affect the VCO and the ILFD in the same way. That is, when they

impact in the VCO by lowering its operation frequency range, they reduce in the same way the self-resonances of the ILFD for the various coarse tuning codes. On the other hand, when the PVT variations are causing an increase of the ILFD operation frequency range, this is reflected also in the VCO, which working range is increased in frequency.

This assumption, verified by the results of the PVT variations simulation in the whole VCO - ILFD co-design, is the starting point for the elaboration of the design technique for high frequency PLLs, which is subject of a registered patent of the author [3]. The patent is annexed in Appendix B. It is exposed in Spanish, since it has been presented last January 2011 the 25th, to the Spanish Office for Patents and Brands (OEPM) of the Spanish Ministry of Trade, Industry and Tourism.

Next Figure 213 shows the PLL architecture object of the invention.
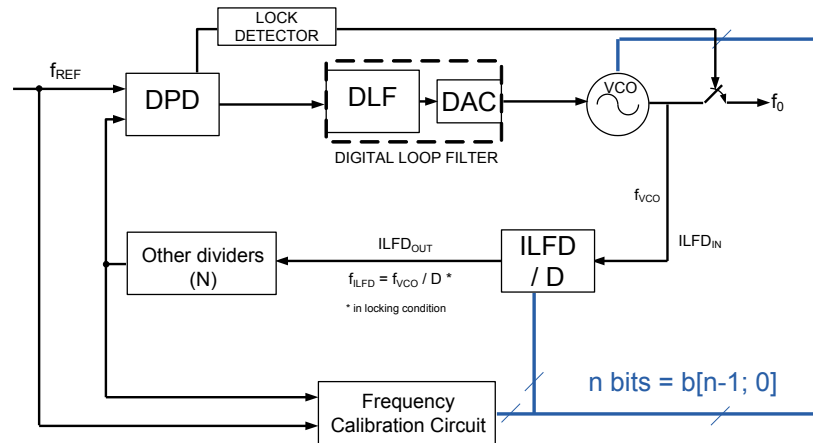
Figure 213: Frequency Synthesizer object of the invention

The PLL of Figure 213 has the architecture comprising an input reference frequency, a Digital Phase error Detector (DPD), a Digital Loop Filter (DLF) followed by a Digital-to-Analog Converter (DAC), an analogue and digitally controlled VCO and a divider chain that has in the first stage a divide-by-D ILFD. The PLL includes two additional blocks. The first one is a Lock Detector (LD) which outputs a bit in order to enable/disable the PLL output as a consequence of the frequency comparison of the DPD. The LD is depicted as a separated block in Figure 213, however it can be included in the DPD, like in the PLL architecture presented in [4]. The second added block is a Frequency Calibration Circuit (FCC). The output of the FCC is a bus of n bits which is controlling both the ILFD and VCO. The control bit string b[n-1:0] can be the same for the ILFD and the VCO, as in Figure 213 is depicted. Nevertheless, the FCC may output two control bit strings b[n-1:0] and k[m-1:0] (n≠m), if required.

The b[n-1:0] bits may control the VCO operating frequency curve and the k[m-1:0] may control the ILFD self-resonance frequency. The lower and higher ILFD self-resonance frequencies correspond, simultaneously, to the lower and higher VCO operating frequency curve.

However, the control word of n bits which tunes the VCO and the ILFD is assumed unique for simplicity in the description, taking advantage that both circuits vary in the same direction and proportional amount due to PVT variations as presented in the previous section.

With the proposed technique, it is possible to overcome to the impact of the PVT variations since, due to the connection scheme, the VCO generated frequency curve is always related to the proper ILFD self-resonance frequency, in order that the lower and higher VCO generated frequencies correspond, in every moment, to the lower and higher, respectively, ILFD self-resonance frequencies.

The need of a block to allow lock detection is due to the fact that when the VCO changes between two frequencies (due to the FCC and DLF outputs), such transition is done through the frequencies in between. This results in a PLL output spectrum which is polluted and, therefore, the PLL output has to be turned off while the PLL is switching between frequencies. For this reason the LD should disable the output until a stable phase-lock is detected. The LD can provide lock or out-of-lock information. It can be implemented with logic ports, [4], and with D Flip-Flop and frequency counters [5].

Depending on FCC output bus, the VCO selects a curve among the 2^n operation frequency curves. The FCC receives as inputs the local oscillator signal at f_{REF} and the divided signal proceeding from the VCO, and it outputs a control string of n-bits as the result of the comparison between the two input frequencies, to adjust and to set the proper VCO frequency curve. As described in this Thesis, it can be achieved by changing the VCO varactors bank capacitance by means of the n control bits. When the binary word [b_{n-1}, b_{n-2},...,b_0] is set, it causes a change in the capacitance of the VCO varactors bank, allowing the VCO to set the proper frequency curve, among the totality of its frequency curves.

The same n control bits can be used also to select the ILFD self-resonance frequency. As seen, it can be achieved by changing the ILFD varactors bank capacitance by means of the same n control bits. When the binary word [b_{n-1}, b_{n-2},...,b_0] is set, it causes a change in capacitance of the ILFD varactors bank, allowing the ILFD to set the proper self-resonance frequency, among the 2^n self-oscillation frequencies available.

As a consequence of the DLF and FCC outputs, the VCO frequency is set to $f_{VCO} = f_0$ and the ILFD self-resonance frequency is set to f_0/D, approximately. Therefore, once that a control bit string is set, the VCO operating frequency curve is set, as well as the ILFD self-resonance frequency. The discrete tuning happens simultaneously for both VCO and ILFD.

In this way the frequency calibration between ILFD and VCO is done and the oscillation signal at f_{VCO} is injected into the ILFD which is self-oscillating at f_0/D, approximately. If the VCO output power is enough to inject-locking the divide-by-D divider, the ILFD output frequency is exactly f_{VCO}/D.

In this condition, the ILFD is in its locking state and its output frequency is exactly equal to f_{VCO}/D. Here, the PLL feedback frequency is lowered, relaxing the frequency division of the next block. Furthermore, the overall ILFD locking range is extended since with this technique the ILFD output frequency is capable to cover the overall VCO tuning range, also in presence of PVT variations (see as example of the implementation Figure 214, where n=4 and D=2).
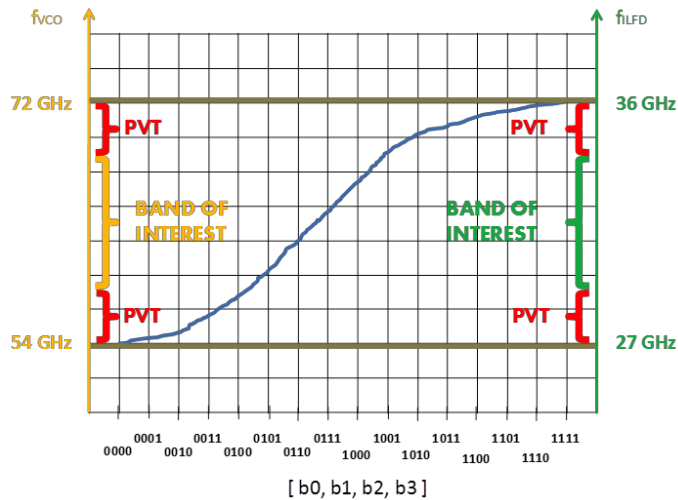
Figure 214: ILFD Output frequency and VCO frequency in locking condition as a function of the control bus, for a given VCO control voltage Vc.

If the PLL loop is not closed, the PLL output is disabled, and the FCC starts the calibration. Once the ILFD locking is achieved, if the DLF output is such that the generated VCO frequency is at the proper value to close the PLL loop, the LD outputs a signal to enable the PLL output.

It is important to remark that the ILFD and the VCO are designed in order that the lower and higher VCO varactors bank capacitance correspond to

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the lower and higher, respectively, ILFD varactors bank capacitance. The ILFD tank and the VCO tank are designed in order to resonate at approximately f_0/D, and at f_0, respectively, depending on the n control bits, for the ILFD, and depending on the same n control bits and on the DC output voltage V_C of the DLF, for the VCO.

7.4   Conclusions

In this chapter, the results of the PVT variations simulation have been presented, taking into account the whole system composed by the VCO and ILFD. The ILFD is able to track the VCO frequencies inside the Wireless HD^{TM} band, for all the PVT corners. However, in some of the extreme PVT corners, a constant bias prevents the circuit to start-up. Therefore, an adaptive bias strategy may be necessary to guarantee the operation in all possible, even unlikely, cases.

The main result achieved with the simulation analysis presented in this chapter testifies that the PVT variations impact with the same trend in the VCO and ILFD tuning ranges.

With the results achieved, a PVT robust PLL has been invented and the subject of the related patent of the author has been presented.

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C h a p t e r   8

8   MEASUREMENTS

8.1   Introduction

In this chapter, the experimental results achieved from the measurements of the manufactured chip are presented, as well as some post-measurements simulation results.

The measurements were performed in the DACLE/LAIR on wafer probing Laboratory of CEA-Leti, in MINATEC, Grenoble (France).

Figure 215 shows some taken photos of the chip. A part the overall die, which dimension is 1 mm x 1mm, pads included, some detailed are illustrated.
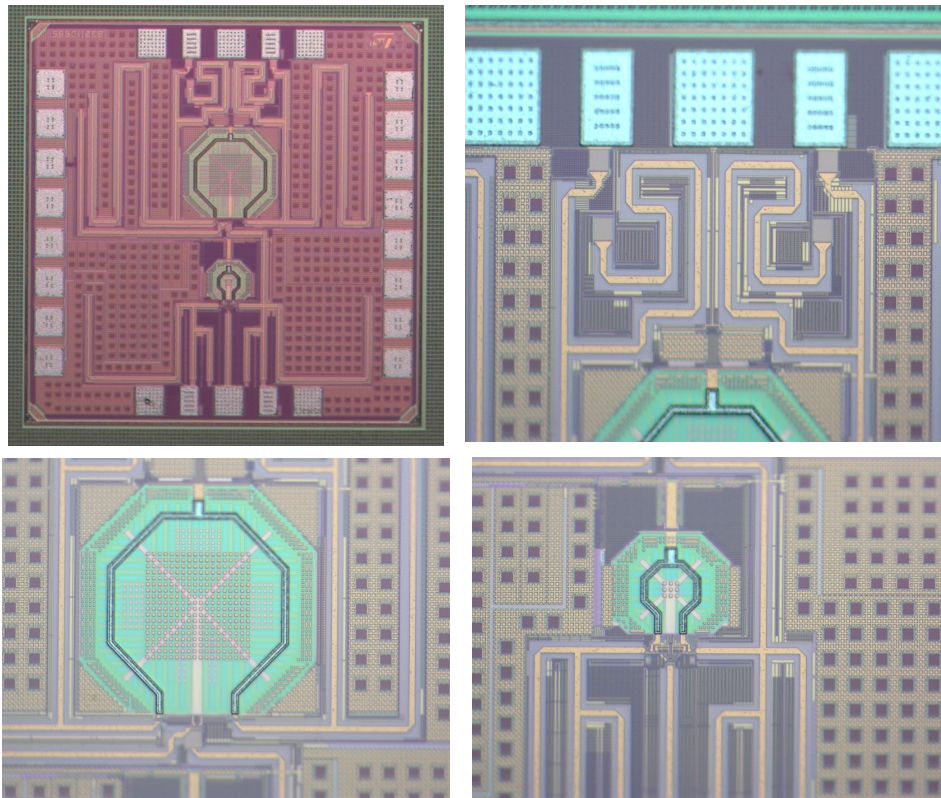
Figure 215: Die photo (upper-left). ILFD out detail (upper-right). ILFD core (lower-left). VCO core (lower-right)

The upper-left picture in Figure 215 shows the full circuit. The ILFD is in the top half and the VCO in the bottom half. DC, bias and control bits are provided through pads in the East and West sides through 100μm pitch pads. The outputs of the ILFD are at the North side and can be accessed using GSGSG 100μm pitch probes. The outputs of the VCO are at the South side and can be accessed using GSGSG 100μm pitch probes as well. Note that the right signal pad of the VCO circuit is used additionally for providing an input signal to the ILFD in the VCO OFF - ILFD ON test case. The upper-right picture shows a detail of the ILFD output buffer matching TLs. The lower-left picture is a detail of the ILFD core where the single turn, differential, patterned ground shielded inductor is clearly visible, whereas the lower-right shows the VCO core with its inductor and output buffer matching TLs.

All the measurements presented next are performed using a Signatone S-1160 Probe Station. The experimental results presented in the following sections correspond to the three test or simulation cases reported in Chapter 6. The VCO ON - ILFD OFF configuration is used to measure the VCO only. VCO OFF - ILFD ON is the measurement configuration used to characterize the ILFD, with the VCO turned OFF. Finally, VCO ON - ILFD ON is the case used to evaluate the operation of the ILFD when driven by the VCO, which corresponds to the real implementation of both circuits inside a PLL.

As a general conclusion from the measurements, which are detailed in the following sections, it has been observed a shift down in the operation frequency ranges of the VCO and ILFD, of around a 16%. As a first explanation of this effect, the hypothesis of an EM modelling error in the inductors has been drawn since this percentage is very close to the difference observed between the results of the EM simulation of the inductors and the value obtained from the DK models.

The post-layout simulations of the circuit is then repeated at top level, but including the inductors models from the DK library, instead of those resulting from the EM extraction. Additionally, a more detailed analysis of the EM simulation methodology for the 65 nm CMOS process, with 7 metal layers, is performed in order to clarify this issue. It is worth to note that the predictions of inductance value obtained with Momentum EM simulation provide an underestimation of the inductance for small differential inductors in the order of a 17% according to analytical formulas for spiral inductors, [1]-[2]. This situation has been reported to the Agilent engineers in charge of supporting the tool and they are investigating the issue. At the time of writing this report, Agilent has not yet provided an explanation.

However the operating range of the circuits is out of the specified range, the measurements have provided an experimental proof that the technique

proposed in this thesis is feasible. The deviation in operation frequency can be reproduced by simulation if the inductors values is changed. In this way, we can show a very good agreement between simulations and measurements. This allows to validate the post-layout simulation methodology and, therefore, provides the required experimental check for the results provided in Chapter 6 for the whole circuit and the VCO and ILFD stand-alone blocks.

8.2   VCO ON - ILFD OFF

Figure 216 shows the measurement set-up required to characterize the 60 GHz VCO. In this configuration the ILFD is turned OFF, i. e. all its DC PADs are connected to ground, while its outputs are not connected (the ILFD output buffers are loaded with an open circuit).
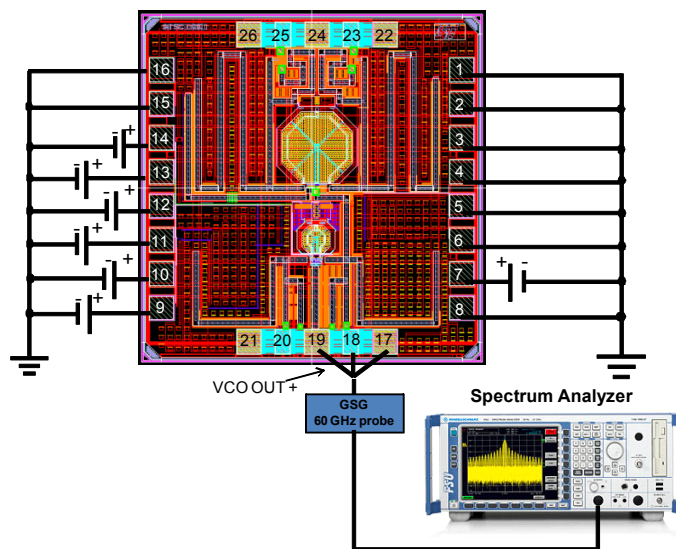
Figure 216: Measurement layout for VCO characterization

The VCO single-ended output is measured at PAD 18, for the reason detailed in Chapter 6, with a 60 GHz co-planar GSG microprobe. The Spectrum Analyzer (SA) used for the VCO measurement is a Rhode & Schwarz FSV 20 Hz-to-67 GHz SA. The losses provided by measurement system, i. e. the GSG probe plus the transitions and the coaxial cable that connects the probes to the 67 GHz SA are available in the form of an S-parameters file for de-embedding them from the measurements, in order to determine the single-ended output power level at the pads output reference plane. They are depicted in Figure 217.
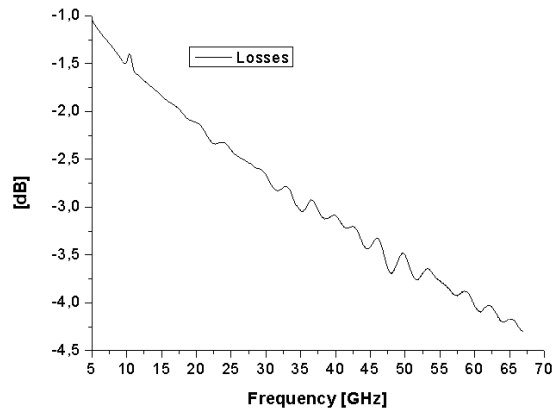
Figure 217: Losses of the measurement system (GSG probe + transitions + coaxial)

Figure 218 shows the DC current consumption of the VCO circuit, for a VCO bias voltage sweep from 0 to 1 V. This measurement is repeated for different supply voltage V_{dd}, in order to find the best value that compensates the DC voltage drop due to the probe and cable losses. Note that the VCO core and VCO buffers supply lines are connected together to PAD 7. For a V_{dd} = 1.25V, the total VCO DC current of 27 mA, is slightly lower than the value achieved in simulation, i. e. 28.36 mA, for a V_{bias} = 715 mV. For such biasing voltage, a total VCO DC current equal to 28.4 mA has been measured for V_{dd} = 1.27 V.
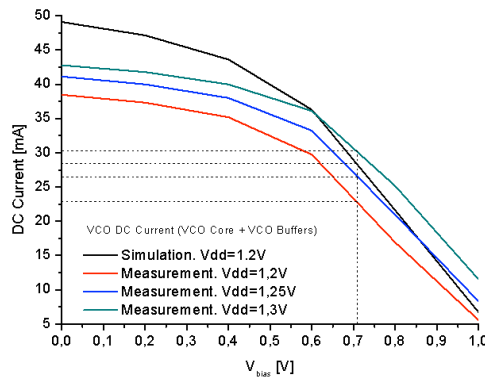
Figure 218: VCO DC measurements

Once that the DC characteristics of the VCO has been quantified, the next step is to measure the VCO frequency characteristics. V_{dd} and V_{bias} are set to 1.25 V and 715m V, respectively. The Resolution Bandwidth (RBW) of the 67 GHz SA is set to 5 MHz, with a Sweep Time (ST) of 30 ms and a Video Bandwidth (VBW) of 10 MHz. The frequency span is set to 5 GHz, while the

centre frequency is set every time at the measured VCO oscillation frequency. The V_{dd} and VCO control voltage V_C, for continuous tuning, is provided by a very low noise DC source from an Agilent 10 MHz-to-7 GHz Signal Source Analyzer (SSA) E5025A, in order to ensure more reliable and stable measurements. In fact, the varactors are very sensitive to the voltage fluctuations of the DC sources. The SSA is also used to measure the VCO phase noise, as it is described later.

Figure 219 (left) shows the measured VCO frequency tuning curves for all possible coarse tuning codes. The figure at the right shows and example of frequency domain signal obtained using the SA for the highest frequency generated by the VCO (note that the output power level corresponds to a single ended output and the losses of the probe + cable should be corrected).
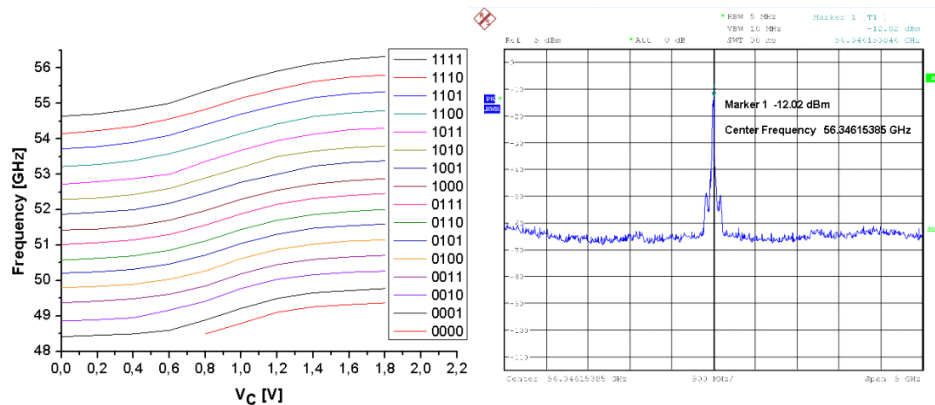
Figure 219: VCO measured frequency curves (left). VCO highest frequency spectrum (right)

The highest measured VCO frequency, corresponding to a binary code b[3:0] = 1111 with V_C = 1.8V, is ≈ 56.35 GHz, which is around 10 GHz below of the expected value from post-layout simulation (see sub-section 6.4.1, where a frequency of 66.9 GHz was found for C_F = 0). It results in a relative error of ≈ 15.7%.

The lowest VCO frequency measured is ≈ 48.5 GHz, which can be obtained with the coarse tuning binary codes b[3:0] = 0000 or 0001 with V_C = 0.8V and 0V, respectively. The oscillation is not observed for b[3:0] = 0000 with $0 \leq V_C < 0.8V$ basically for two reasons. Firstly, the VCO output buffer is strongly attenuating the signal at this frequency and, secondly, the NMOSs cross-coupled pair of the VCO may not be able to properly compensate the VCO tank losses, since they have not been sized to achieve oscillation at such frequencies.

The measured VCO tuning range is ≈ 15%, which results in a very wide VCO tuning range for mm-W applications.

Figure 220 shows the single-ended VCO output power measured at PAD 18. In the traces shown, the cable + probe losses of the measurement set-up have been compensated. The abovementioned issues related to the tank losses compensation and buffer attenuation result in a VCO output power which is lower as the frequency decreases.
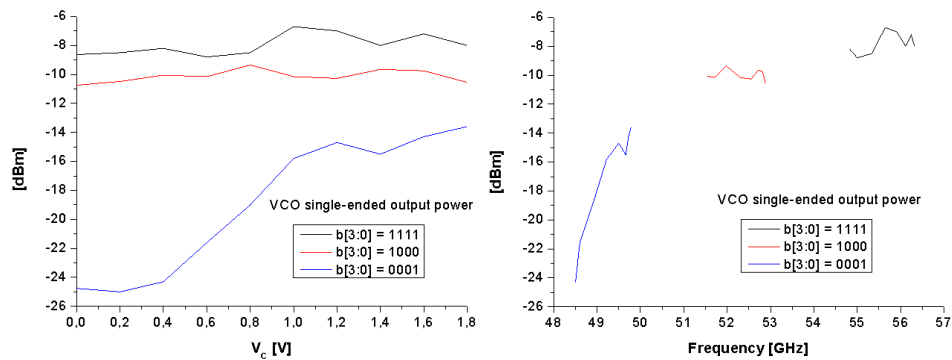
Figure 220: VCO output power (single-ended)

The VCO buffer output matching have been also measured by replacing the SA of Figure 216 with a Rhode & Schwarz ZVA 50Ω 67 GHz Vector Network Analyzer (VNA). Figure 221 shows a screen capture of the instrument for such measurement.
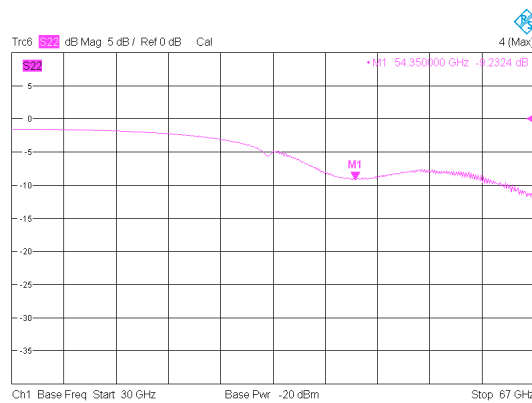
Figure 221: VCO 50Ω output matching

The result illustrated in Figure 221, if compared to the plot of Figure 179 (left), validates the design of the VCO output buffer presented in this Thesis. This measurement indicates that the EM modelling approach using Momentum

demonstrates to be reliable when applied to microstrip transmission lines at 60 GHz in a 7 metals, 65 nm CMOS process, which are the basis for the output buffer matching characteristic. On the other hand, the VCO frequency operation range down-shift observed in measurements in comparison with the simulations, leads to re-consider the accuracy of the VCO inductor model extracted with the EM simulation presented in 6.1.1. The inductance value corresponding to the EM extracted model of the inductor was ≈ 17% below that one provided by the DK model. It is quite the same percentage corresponded to the VCO frequency down-shift percentage. This issue is faced up in the following sub-section.

8.2.1 VCO Post-Measurement Simulation

Referring to the schematic of Figure 189, in the top VCO circuit the inductor model resulted from the EM extraction (see Figure 141 (left) where the VCO core is shown) is replaced with the DK library model. For such test bench, the following Figure 222 shows some VCO frequency curves from the new post-layout simulation, compared to the measured curves.
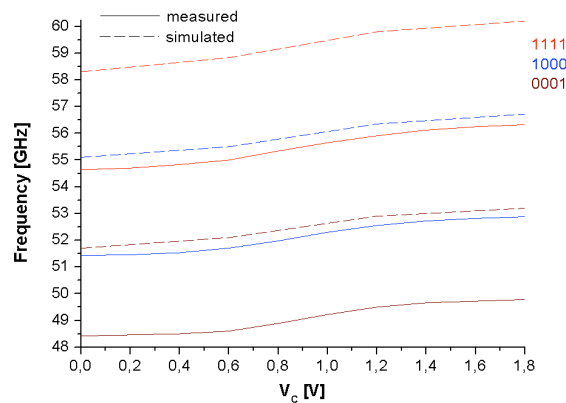
Figure 222: VCO frequency curves comparison, L DK, C_F=0

If the inductor model provided by the DK library is considered in the simulation, the VCO operation range is strongly reduced (see Figure 191 (left) for comparison), approaching the experimental results. Nevertheless, from Figure 222, a constant shift of 3.2 GHz for the VCO oscillation frequencies is still observed. This has been quantified as an underestimation of 13.92 fF in the fixed capacitance C_F of the VCO tank. It results in a 9.3% modelling error. If this capacitance is added to the VCO tank, the measured and simulated curves agree, as shown in Figure 223 (left). In the case of this new post-layout simulation, the VCO does not oscillate with the coarse tuning binary code b[3:0] = 0000 and the control voltage V_C < 0.75V. This result is quite well in agreement with measurements.
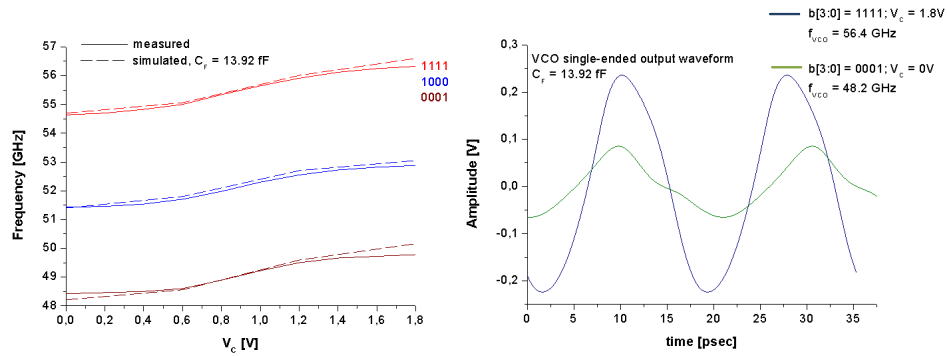
Figure 223: VCO with L DK, C_F=13.92 fF. Frequency curves (left). Single-ended output waveform (right)

In Figure 223 (right) the simulated VCO single-ended output waveforms, corresponding to the highest and lowest VCO frequencies achieved for the coarse tuning b[3:0] = 1111 and 0001, with V_C = 1.8 V and 0, respectively, are shown. Their amplitudes deliver to a 50 Ω load a power of ≈ -3 and -14 dBm, respectively. Therefore, the differences of ≈ -4.5 and -11.5 dB in the VCO single-ended output power, are observed between measurement and simulation.

The reliability and accuracy of the EM extraction with Momentum for the inductors of the 7 metals design process is investigated in the following sub-section. The VCO inductor is extracted using different simulation criteria and performing different layout simplifications, and a comparison of the results achieved is presented.

8.2.2   *EM Analysis of the VCO Inductor*

In this sub-section the inductor used in the 60 GHz LC-VCO is deeply analysed through several simulation loops with Momentum in order to investigate the reasons of the lower inductance value provided in 6.1.1, if compared with the DK model. The modelling approach used has caused an underestimation of the VCO inductance and, consequently, the rest of the circuit has been designed, at layout level, taking into account such value. With a lower value of the inductance, the final parasitic capacitance budget was respected and the output buffers transistors gate size and interconnections structure was sized to consume this entire budget. However, if the inductance value is actually higher than expected, the total parasitic capacitance of the VCO circuit would be too large. Therefore, this has resulted in a lower VCO operation frequency, as discovered in the measurements.

As previously mentioned, the inductor used in this Thesis (which has the same characteristics for both the ILFD and VCO tanks, a part its inductance

value) is composed by a single turn differential inductor made with the three upper copper metal layers (M7, M6 and M5) plus the aluminum metallization layer (ALUCAP). It has a patterned grounded shield made of M1, M2 and poly-silicon. In the following Table 14, different layout manipulations and simplifications criteria for the VCO inductor simulated with Momentum are exposed:

Notation	Comments
DK	Inductor model provided by the DK library
mom	Momentum model of the Inductor composed by **only M7**
mom2	Momentum model of the Inductor (with all its metal layers) in which the vias are treated as 3D elements. Vias simplification is performed
mom3	Momentum model of the Inductor (with all its metal layers) in which the vias are treated as 2D elements. Vias simplification is performed
mom4	Momentum model of the Inductor (with all its metal layers) in which the vias are treated as 2D elements. **No vias simplification is performed**
mom5	Momentum model of the Inductor (with all its metal layers but **the ALUCAP layer is removed**) in which the vias are treated as 2D elements. Vias simplification is performed
mom7	Momentum model of the inductor according to a loaded pre-defined state available in CEA-Leti (all the metal layers are considered, with vias simplification)

Table 14: VCO Inductor EM simulation cases

Figure 224 shows the VCO differential inductance (L) as the result of the EM simulation with Momentum, corresponding to the cases exposed in Table 14. Furthermore, Figure 225 reports the achieved quality factor (Q) for all the simulation cases. The test bench circuit in order to evaluate L and Q is that shown in Figure 44 (left) and the post-simulation function (7), (8) and (9) are used.
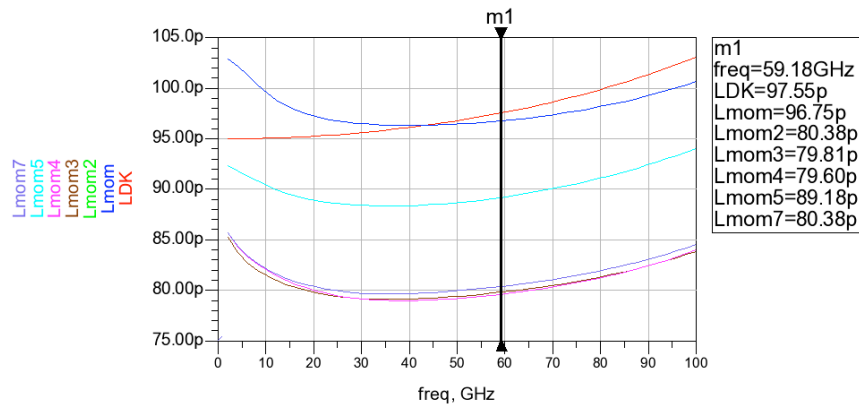
Figure 224: VCO inductance
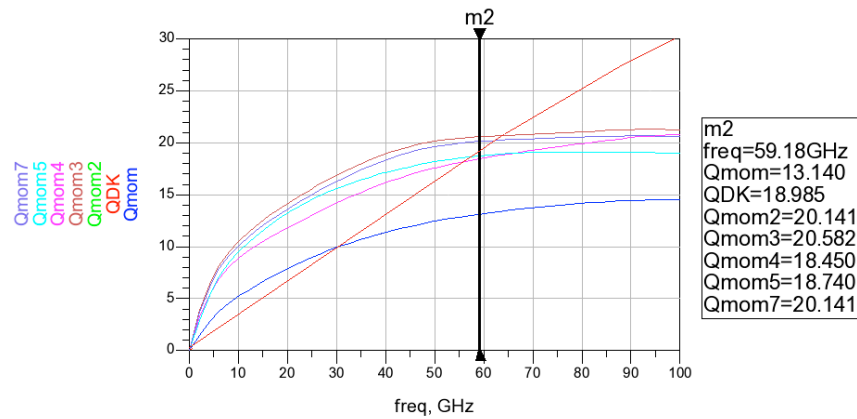
Figure 225: Quality factor of the VCO inductor

As reported in Figure 224, the L value at 60 GHz corresponding to "*mom*" and "*mom5*" are closer to the value provided by the DK model of the inductor. In "*mom5*" the inductor is composed by M5, M6 and M7 (with related vias and contacts disposed in arrays along the single turn), but the ALUCAP layer has been removed, so that it isn't considered in the EM extraction. The ALUCAP modelling is indeed critically impacting in the resulted L, since in the case of "*mom3*" (which is the same of "*mom5*" plus the ALUCAP) very similar results as those found in 6.1.1 are achieved. The value of L in the case of "*mom*", where the single turn is composed only by the top M7 layer, that is without any via and contact and without any other layer turn, is very close to the value provided by the DK library model and to the analytical value obtained by [1]-[2] from the geometrical description of the inductor. For this case, obviously the Q is strongly reduced, since higher losses are accounted in the model of such inductor, due to the lower total cross-section of the inductor. From the

results so far considered it is clear that the ALUCAP layer is affecting the accuracy of the modelling. On the other hand, the impact of the vias and contact simplifications criteria are also evaluated. In order to reduce the long simulation times (i. e., seven hours in the case of the large inductor of the ILFD, performing simplifications) the vias and contacts between two consecutive metal layers can be treated as a stacked conductor (see Figure 140). In addition, the vias can be handled as a 2D element (reducing the extraction time) or as 3D. It could impact in the modelling process since the effects of the incident electromagnetic wave in a 2D or 3D structure could be different. The results achieved in the "*mom2*", "*mom3*", "*mom4*" and "*mom7*" cases allows to give the following conclusions, related to the inductor extraction with Momentum: firstly, performing or not the vias and contacts simplifications does not affect the results. Secondly, handling the vias as a 2D or 3D model has a minimum impact in the results. Therefore, the way the layout is simplified has been not find as the cause of the modelling error in the inductors. Note that, even though the above analysis has been restricted to the VCO inductor, it is possible to assume that the same modelling problem is also affecting the EM extraction of the ILFD inductor model used for post-layout simulations. Indeed, the same difference, in percentage, between the inductance values provided by the DK and Momentum models has been found for the both VCO and ILFD inductors.

8.3   VCO OFF - ILFD ON

Figure 226 shows the measurement set-up required for the experimental characterization of the 60 GHz divide-by-two ILFD. The VCO is turned OFF, i. e. all its DC PADs are connected to ground.
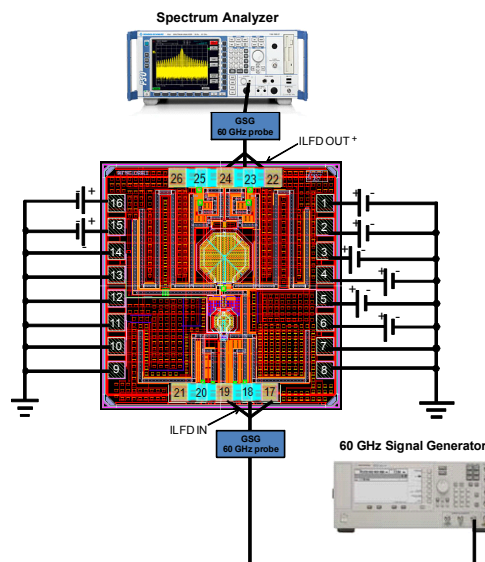
Figure 226: Measurement layout for VCO characterization

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The ILFD single-ended output is measured at PAD 23 with a 60 GHz co-planar GSG microprobe. However, the ILFD single-ended output could be measured also at PAD 25, achieving the same results since the ILFD differential output is balanced. A Rhode & Schwarz FSIQ 20 Hz-to-40 GHz SA is used. The losses provided by GSG probe plus the transitions and the coaxial cable used to connect the test circuit to the 40 GHz SA have been previously experimental characterized and they are available for de-embedding. This allows to determine the ILFD single-ended output power level at the output pads plane.

An Agilent E8257D 250 KHz-to-67 GHz Signal Generator (SG) is used to provide the ILFD with an input signal. Such SG is connected through a co-planar GSG microprobe to the PAD 18, that was used as the VCO output in the previous test case. Also in this case, the losses of the measurement system are known and they are used in order to calibrate the input power injected into the ILFD.

Figure 227 shows the current consumption of the ILFD core and its output buffers, for a ILFD bias voltage sweep (V_{bias_ILFD}). The measurement is repeated for different injection transistors biasing voltage (V_{bias_Inj}), i. e. different DC bias of the common gate NMOSs which compose the ILFD injection stage. Its nominal value is 600 mV. The measurements next are performed by setting the voltage supplies of the ILFD core and buffers to 1.25V, in order to compensate the DC voltage drop due to the DC probes and cables losses. As mentioned, the supply lines of both ILFD buffers are internally connected, so that the DC current consumption in Figure 227 (right) corresponds to the two output buffers. For a V_{dd} = 1.25V, considering the nominal value V_{bias_ILFD} = 850 mV, the measured DC current consumption of the ILFD core is very similar to that obtained in the post-layout simulation. In this condition, for a V_{bias_Inj} = 600 mV, a current of 8.75 mA is measured for the ILFD core, while its buffers consume 17.3 mA (i.e. 8.65 mA for each buffer).
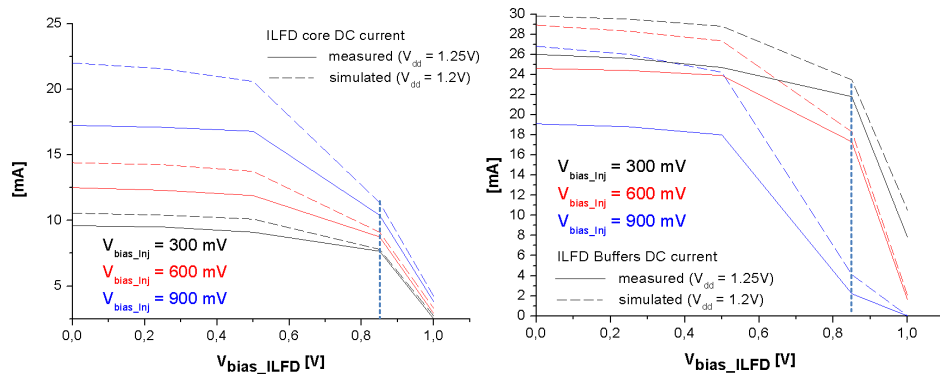
Figure 227: ILFD DC measurements. ILFD core current (left). ILFD buffers current (right)

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As a summary of the DC measurements, there is a good agreement between simulation and experimental results.

In order to evaluate the divide-by-two ILFD self-resonance frequencies, the RF signal of the SG is turned OFF. V_{dd} and V_{bias_ILFD} are set to 1.25V and 850 mV, respectively. The ILFD self-oscillates only for the binary code b[2:0] = 111. That is, only one of the expected eight self-resonance frequencies is measured. The measured self-oscillation frequency is reported in Figure 228. It is found at 26.96 GHz for V_{bias_Inj} = 300 mV. This can be explained by the fact that the ILFD maximum frequency is ≈ 5.5 GHz below the expected value from post-layout simulation using EM model of the inductor. The NMOSs cross coupled pair of the ILFD has not been sized to achieve oscillation for a frequency range below 27 GHz. If compared to the expected maximum self-resonance frequency, i. e. ≈ 32.5 GHz, a relative difference of ≈ 17% is found. The ILFD single-ended output power for this self-oscillation frequency is around -14.5 dBm (the measurements set-up losses have been extracted). In addition, for V_{bias_Inj} > 300 mV the ILFD self-oscillation vanishes. This is because, as seen in sub-section 5.4.3, as higher is V_{bias_Inj} (or the NMOSs injection transistors width W_{inj}) as larger the NMOSs cross coupled pair width of the ILFD should be, in order to ensure oscillation start-up.
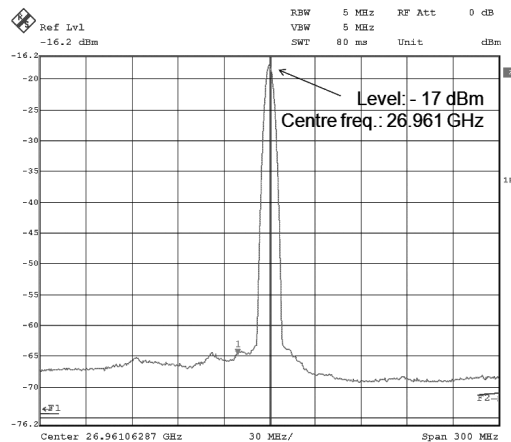
Figure 228: ILFD self-resonance frequency, b[2:0] = 111, V_{bias_Inj} = 300mV

As a summary of the dynamic measurements of the ILFD, the same problem found in the VCO is observed in the ILFD: a down-shift of the operating frequencies. Indeed, since in the case of the ILFD few bits are available for coarse tuning, only the higher oscillation frequency can be obtained. For the other values either the output buffer is not providing enough signal to be observed in the SA for the lower self-oscillation frequencies, either the negative resistance of the cross-coupled pair is not high enough to compensate the tank

losses for lower frequencies and start-up the oscillation, or even both things occur.

However, the sensitivity curves of the divide-by-two ILFD can be calculated, for 150 mV ≤ V_{bias_Inj} ≤ 300 mV. This will allow to demonstrate the operation of the dual-mixing ILFD, as presented in 5.4, i. e. the fact that the ILFD locking range can be enhanced by increasing the injection efficiency through increasing V_{bias_Inj}.

Next Figure 229 shows the sequence of the locking. in a), the SG sub-harmonic frequency at $f_{in}/2$ with a constant power level (i. e. -10 dBm referred to f_{in}) is approaching the ILFD self-resonance frequency (f_{self}). The locking is not achieved and the resulting signal seen in the SA at the ILFD single-ended output is a mixed signal where the two tones are observable. This situation is similar to that simulated and reported in Figure 90 (left). In b), $f_{in}/2$ is decreased, by decreasing the SG f_{in}, and the injection locking is almost achieved, while in c) it occurs and the ILFD output frequency presents one single tone exactly at $f_{in}/2$. If the frequency of the SG is further lowered, the ILFD tracks it, if the injection locking is still kept, as shown in d).

In order to build the ILFD sensitivity curves, the frequency and power of the SG are swept. Simultaneously, the ILFD single-ended output is observed at the screen of the 40 GHz SA, in order to detect when the injection locking occurs. This operation is repeated for different V_{bias_Inj}. The input power is calibrated, taken into account the losses of the cable plus transitions and GSG microprobe. Figure 230 shows the measured sensitivity of the divide-by-two ILFD around the double of its self-oscillation frequency. As expected, the ILFD locking range increases as V_{bias_Inj} is higher, since the injection efficiency is improved, according to equations (1) and (2) . In addition, the centre of the reported curves move at lower frequencies as V_{bias_Inj} decreases. This is because V_{bias_ILFD} is kept constant to 850 mV and consequently higher bias current is flowing in the NMOSs cross coupled pair for a lower V_{bias_ILFD}, resulting in a higher ILFD tank capacitance, which according to (18) leads to a reduced ILFD locking range. Simultaneously, the reduction of V_{bias_ILFD} results in a lower bias current for the dual mixing injection transistors, decreasing the injection efficiency, and, consequently the locking range of the ILFD.
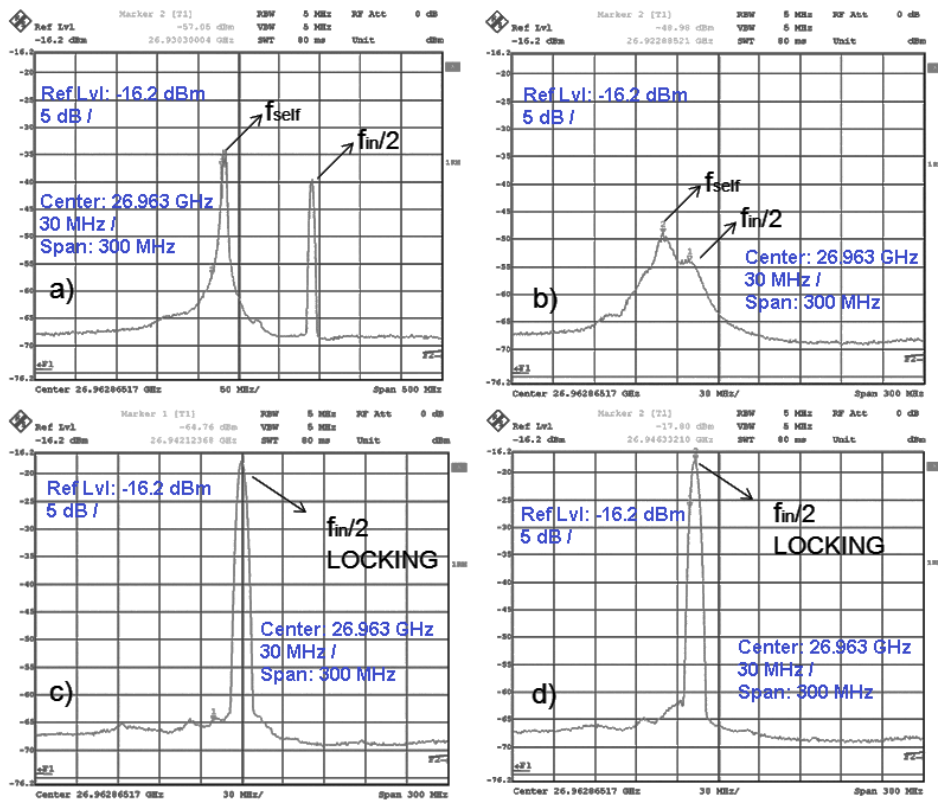
Figure 229: Injection locking mechanism
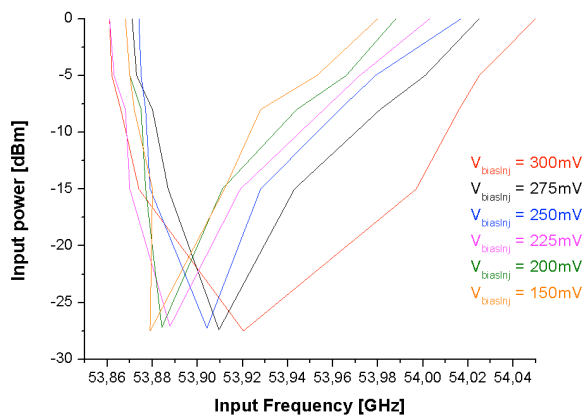
Figure 230: Divide-by-two ILFD sensitivity curves

A locking range of ≈ 200 MHZ is found for 0 dBm input power around 53.92 GHz for V_{bias_Inj} = 300 mV. This is a very poor locking range and the causes of such result are investigated in the following sub-section.

The ILFD buffer output matching has been also measured by replacing the SA of Figure 226 with the 67 GHz VNA. Figure 231 shows a screen capture of the instrument for such measurement.
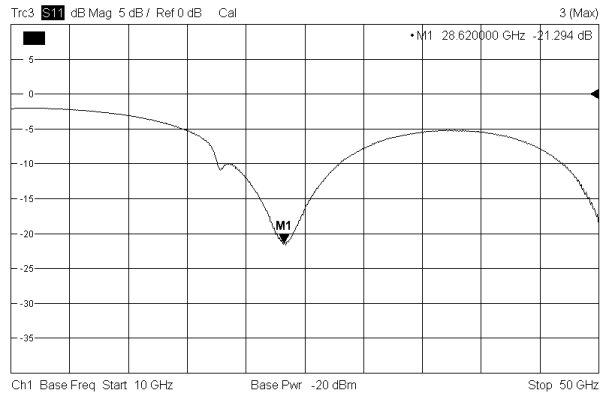
Figure 231: ILFD 50Ω output matching

Similarly to the VCO, the ILFD output buffer measurement is in agreement with the simulation result, i. e. see for comparison Figure 174 (left).

8.3.1 ILFD Post-Measurement Simulation

As already seen in 8.2.2, a modelling error in the EM extraction process with Momentum of the inductors models used in the post-layout simulation, for the selected 7 metal layers 65 nm CMOS process, has been detected. In 6.1.1 the ILFD inductance value corresponded to the EM extracted model of the inductor was found to be ≈ 17% below the value provided by the DK model.

In order to verify that the modelling error in the inductor is the cause of the ILFD frequency operation range down-shift, referring to the schematic of Figure 194, the inductor model resulted from the EM extraction (see Figure 147 (left) where the ILFD core schematic is shown) is replaced in the top ILFD circuit with the DK library model of the same inductor. In this case, for the binary code b[2:0] = 111 and V_{bias_Inj} = 600 mV, the ILFD self-oscillates at 30.1 GHz. Two issues have to be considered. Firstly, the simulation result is not in agreement with the measurement, since the ILFD self-oscillates for such V_{bias_Inj} value, while in the measured circuit the self-oscillation was not observed for V_{bias_Inj} values higher than 300mV. However, it has been confirmed that if an ideal differential resistance R_F = 800 Ω is inserted between the ILFD core single-ended outputs, i. e. between the nodes V_{out_P} and V_{out_N} in the schematic of Figure 147 (left), the ILFD self-oscillates at 30.1 GHz but only for the binary code b[2:0] = 111 and V_{bias_Inj} ≤ 300 mV. This is interpreted as an underestimation of the losses of the layout interconnections. It results in a lower

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R_{peq} of the ILFD tank which impacts critically in the ILFD operation range. Secondly, the self-oscillation frequency difference between the measured and simulated ILFD, for case when the DK model of the inductor is used, corresponding to b[2:0] = 111 and V_{bias_Inj} = 300 mV has been quantified as an underestimation of 12 fF in the fixed capacitance C_F of the ILFD tank. This represents a 10.4 % modelling error of the interconnection parasitic capacitance. If a fixed capacitor of 12 fF is added in parallel to the tank output, the measured results can be matched by post-layout simulations.. Figure 232 shows the ILFD single-ended output waveform corresponding to the above mentioned setting. Note that the peack amplitude is ≈ 85 mV, which results in a power level delivered to a 50 Ω load equal to -11.5 dBm (there are -3 dB of difference between such measured value and the simulated value).
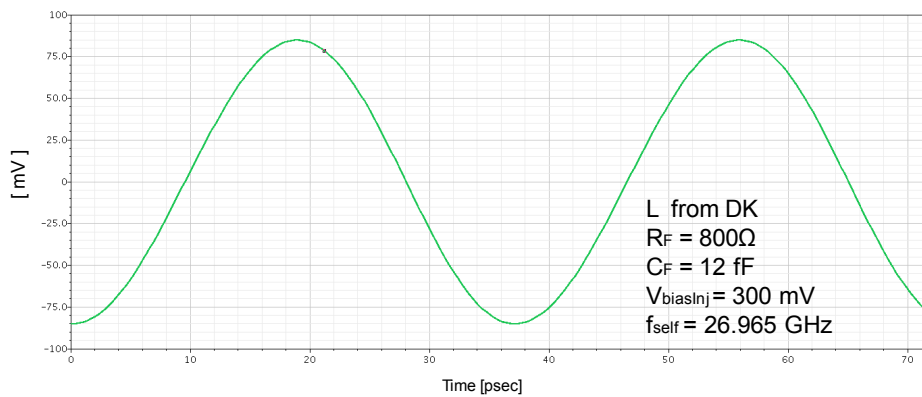
Figure 232: Post measurement simulation. ILFD self-resonance frequency

Finally, for the post-measurement simulation case so far considered, the ILFD input sensitivity curve is obtained. The goal is to determine if there is an agreement between the measured and post-measurement simulated ILFD locking range. In order to do it, in the ILFD tank the inductor model provided by the DK library is used and the compensation of the layout interconnections model provided by Momentum, i. e. including a R_F = 800 Ω and considering a C_F = 12 fF, is considered. The results are shown in Figure 233, where both the ILFD simulated and measured input sensitivity curves are plotted. The simulation results obtained with *a posteriori* analysis are quite in agreement with the measurements. The measured ILFD locking range, for 0 dBm input power, is 200 MHz, from 53.86-to-54.06 GHz, while the simulated one is found to be 250 MHz, corresponded to 53.85-to-54.1 GHz. The ILFD locking range is strongly reduced, mostly due to the errors in modelling the inductor and layout interconnections of the ILFD core with Momentum.
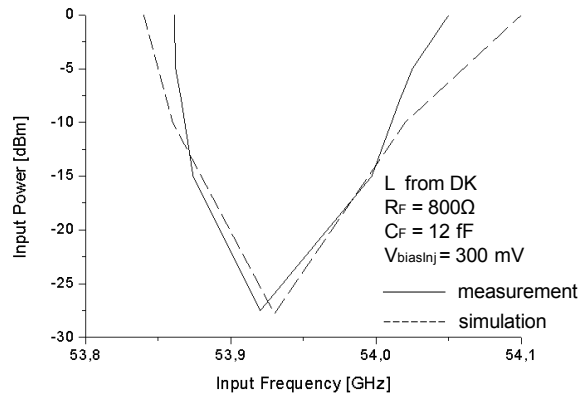
Figure 233: Post measurement simulation. ILFD sensitivity curve

8.4   VCO ON - ILFD ON

As a consequence of the decreased operation range of both the ILFD and VCO, for the reasons mentioned previously, the locking range of the ILFD when the VCO is injecting the mm-W signal is critically reduced. However, it is still possible to experimentally verify that both circuits operate correctly when connected together. Figure 234 shows the test-bench used in this last test case.
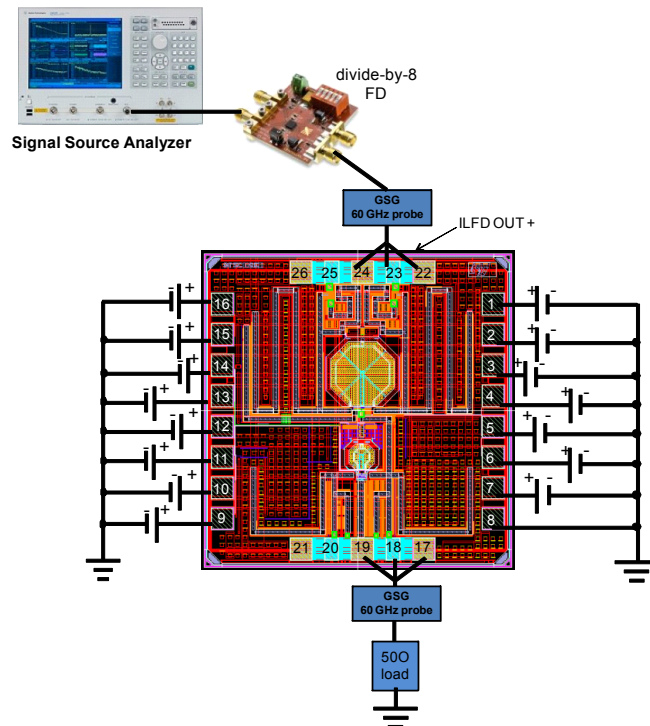
Figure 234: VCO ON - ILFD ON measurement layout

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The SSA is used for the measurements in this case. A divide-by-8 logic Frequency Divider (FD) available in the Laboratory is used in order to divide the 30 GH band signal output by the ILFD up to the measuring range of the SSA. In this way the single-ended divide-by-2 ILFD output is connected to the input of the divide-by-8 FD. Therefore, the SSA measures the divided-by-16 VCO frequency, if the injection locking is achieved, or the divided-by-8 ILFD self-oscillation frequency, if the VCO is OFF. The VCO control voltage V_C is connected to the very low-noise DC source of the same SSA, in order to ensure more reliable and stable measurements. In fact, the varactors are very sensitive to the voltage fluctuations of the DC source and to observe the injection locking between the VCO and the ILFD also some other control bits have needed to be connected to such low-noise source, instead of the normal DC sources previously used in the measurements. Figure 235 shows a picture of the test set-up, for a better understanding of the measurements done,.
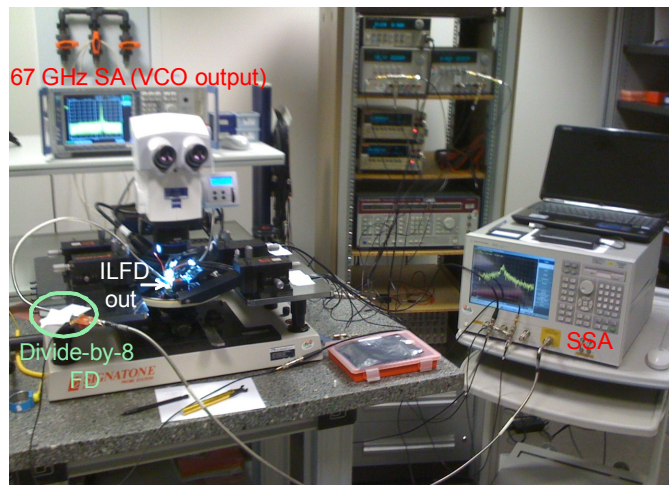
Figure 235: Photo of the measurement in CEA-Leti MINATEC Laboratory

The locking state between the VCO and the ILFD is achieved from ≈ 53.875-to-54.01 GHz. Figure 236 (upper) shows the divided-by-16 VCO frequency measured by the SSA, i. e. when the ILFD is injection locked by the VCO. The VCO frequency is around 53.96 GHz, corresponding to b[3:0] = 1101 and V_C = 0.55 V, and the control bits of the ILFD are set obviously to b[2:0] = 111.
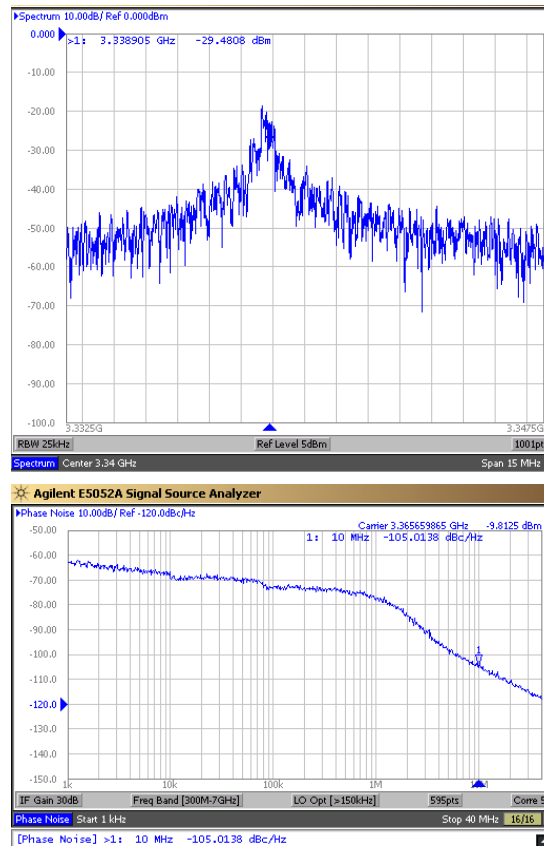
Figure 236: Divided-by-16 VCO frequency spectrum (upper). VCO phase noise (lower)

Figure 236 (lower) reports the phase noise (PN) of the divided VCO frequency. The marker is placed at 10 MHz frequency offset from the carrier and in order to correctly evaluate the VCO PN at 1 MHz frequency offset, the following expression must be used:

$$PN\left(\Delta f=1MHz\right) = PN\left(\Delta f=10MHz\right) + 20\log\left(16\right) + 20dB \qquad (23)$$

The measured VCO PN at 1 MHz frequency offset from the carrier is ≈ -62 dBc/Hz, which is far from that expected from simulation (see Figure 204). However, the considered carrier is not the same, since the measured PN is related to a lower carrier (around 10 GHz lower) if compared to that of the simulation results.

In order to measure the PN of the ILFD, in its self-oscillating state, the VCO is turned OFF, so that the ILFD free-running frequency is measured. Figure 237 shows the measured ILFD PN.

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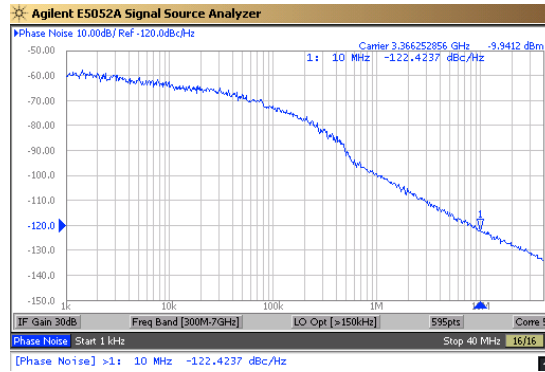
Figure 237: ILFD phase noise (free-running)

Also in this case the marker is placed at 10 MHz frequency offset from the carrier, According to (23), where a factor 8 is now considered instead of 16 since the measurement is related to the ILFD self-resonance frequency, the measured ILFD PN at 1 MHz frequency offset is -84.4 dBc/Hz. Such value is ≈ 5 dB higher than that obtained in simulation (see Figure 196 (right)).

8.5   Conclusions

The experimental results reported in this Thesis for a 60 GHz VCO and divide-by-two ILFD co-design in 65 nm CMOS technology demonstrate how tremendously difficult is achieving a complete agreement between simulations and measurements for mm-W ICs design. In addition, open issues not still solved exist in the current available CMOS technologies and devices modelling for such application, as it has been shown with the post measurement analysis of the inductor with the EM simulator for the selected 7 metal layers process.

Furthermore, one has to note that the differences between the simulation and experimental results, in both ILFD and VCO, are due to a summation of causes. On one hand the detected error in the modelling of the inductors. On the other hand, there is an error in the modelling which is not clear if it is caused by the simulation environment or by the methodology used to extract the layout parasitics. However, these are the most critical issues for mm-W ICs design in CMOS, already experienced in other works that are included in the bibliography of this Thesis.

Nevertheless, since the detected problem for the inductors modelling with Momentum for the selected 7 metal layers process has not been discovered until the measurement phase, a re-design has not been considered. Indeed, as seen in this chapter, due to the inaccurate EM modelling of the inductors, both the VCO and the ILFD cores would have needed a re-sizing, i.e.

replacing the same inductors with others with lower inductances or lowering the capacitances of the varactors, or re-considering the interconnection structures in both ILFD and VCO, in order to achieve the required operating frequencies.

However, in the case of the ILFD, regarding the modelling of the losses in the layout interconnections, it is very difficult to determine if the error is due only to the design methodology used, or if there is some inaccuracy in the EM extraction process (or both of them), taking into account what is exposed in 8.2.2. In addition, the poly-silicon resistor used to implement the stabilizing networks at the input stage of the ILFD and VCO output buffers, see Figure 157 and Figure 178, respectively, presents a parasitic capacitance to ground which is not considered in the model used in the design simulations. Such capacitance contributes to increase the ILFD and VCO capacitive loads, decreasing their frequency operation ranges. From geometrical considerations, by comparing to others poly-silicon resistor models available in the DK library which consider such parasitic contribution but allow the implementation of higher resistances then the required, i. e. 1 KΩ, the capacitance to ground of the selected poly resistor is estimated in 0.15 fF. However, this results in a differential capacitive contributions to both ILFD and VCO loads of 750 aF, that is only a 0.625% and 0.55%, respectively, of the modelling errors.

As *a posteriori* remark*,* the selection of a 4x4 varactor for the ILFD 3-bit binary scaled varactors bank (see Figure 145) could have complicated the modelling of the layout interconnections of the ILFD core. Such structure, even if it allows to design high quality factor varactors banks, has the drawback of a higher fingers number (if compared to other simplest structures like 1x1 or 2x2), which requires more complicated layout interconnections that could easily result in a modelling error or inaccuracy. Momentum has been demonstrated to be accurate when it has been used to model the transmission lines for the mm-W signal distribution and output matching in the chip, since the results of the output buffers measurements, at 30 and 60 GHz, are in agreement with the simulations, for both the ILFD and VCO, respectively.

In the next Table 15 and Table 16 a performance summary of the ILFD and VCO circuits, respectively, presented in this Thesis is given. Additionally, for each circuit, the results are compared to those already reported which constitute the State-Of-Art for mm-W CMOS ILFDs and VCOs. In the case of the ILFD performance, the results related to this work correspond to those achieved with post-layout simulations (see 6.4.2).

Ref.	Year	Div. Ratio	P_{DC}[1] [mW]	V_{DD} [V]	Dividing Range[2] [GHz]	Dividing Range[2] [%]	Output Power[3] [dBm]	CMOS Tech. [nm]
This work	2012	2	10.65	1.2	54.6 - 67.4	21	-4	65
[3]	2011	2	1.32	0.5	63.25 - 65.75	3.9	-16.4	90
[4]	2011	4	12.6	1.8	57.78 - 60.22	4.135	-7	180
[5]	2011	2	8.6	1.2	52.7 - 64.8	20.6	-16.5	90
[6]	2010	2	1.65	1.2	48.5 - 62.9	25.85	-5	65
[7]	2009	2	1.6	0.8	59.6 - 67	11.7	N.A.	130

[1]output buffers not included; [2]0 dBm input power; [3]single-ended.

Table 15: ILFD performance summary and comparison

Ref.	Year	CMOS Tech. [nm]	P_{DC}[1] [mW]	V_{DD} [V]	Centr. Freq. f_0 [GHz]	Tuning Range [%]	Phase Noise[3] [dBc/Hz]	Output Power[4] [dBm]
This work	2012	65	32.4	1.2	52.425	15	-62	-10.5
[8]	2011	65	16.5	1	59	5.4	-90.3	-0.9[5]
[9]	2011	90	3.16[2]	0.6	64	8.75	-88	N.A.
[10]	2011	180	7.7	1.2	59.5	8.3	-91.5	-27
[11]	2010	65	24.6	1.2	56	17	-99.4	-9.8
[12]	2009	130	0.8[2]	0.8	56.5	7	-73	N.A.

[1]output buffers included; [2]VCO core only; [3]1 MHz frequency offset; [4]single-ended; [5]differential.

Table 16: VCO performance summary and comparison

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9   CONCLUSIONS

In this Thesis, a state-of-art review of CMOS frequency dividers has been presented. The locking mechanism in 60 GHz oscillators has been deeply analysed and a methodology in order to simulate and evaluate qualitatively and quantitatively the locking and non-locking ILFD states has been proposed. The impact of a high/low tank quality factors in the locking range of a LC based divide-by-two ILFD has been investigated and evaluated for the selected 65 nm CMOS process.

Additionally, the operation principle and the optimization trade-offs involving power consumption, tuning and locking ranges of the selected ILFD topology (i.e. the dual-mixing) have been demonstrated. Even if the experimental results are not completely in agreement with the simulations, for the reasons previously illustrated, the proposed technique has been validated with post-measurement simulations. As demonstrated experimentally, the locking range of a low-power ($\approx$ 10 mW), discrete tuned divide-by-two ILFD can be enhanced by increasing the injection efficiency of its input stage, without the drawbacks of higher power consumption and chip area required by other approaches.

A 4-bits LC-VCO with very wide tuning range (around 15%) for mm-W applications has been co-designed and implemented using the selected 65 nm CMOS process. The VCO has both discrete and continuous tuning mechanism. The discrete tuning mechanism is provided by means of binary scaled differential varactors. The VCO power consumption is $\approx$ 33.75 mW, output buffers included. The operation range of the presented VCO is suitable to allow the implementation of zero or very low-IF transceivers for the WirelessHD$^{\text{TM}}$ band.

In this Thesis, the injection locking phenomena of the designed ensemble composed by the VCO and the divide-by-two ILFD has been experimentally demonstrated. The well known frequency synthesizers design issue related to the distribution of the frequency signals at mm-W in CMOS has been addressed in the presented work. The VCO and ILFD co-design and co-layout have implied the design, EM modelling and implementation of complex active and passive mm-W circuits in order to provide the ILFD with an input

signal and the required 50 Ω output matching of both the ILFD and VCO outputs for measurements.

Several passive devices have been extracted from the layout using EM simulations in order to include the extracted models in the post-layout simulations. The experimental results of the VCO and ILFD output buffers validate the methodology and techniques described in this Thesis for the design process of such structures for the frequency distribution across the test chip. Even though the experimental measurements have revealed an important discrepancy between the EM models for inductors and the reality, this is not an issue of the methodology used but of a bug or problem in the EM simulation tool used when applied to the inductors in the particular 7 metal layer CMOS process which has been selected in this work (it is providing good results for other structures as transmission lines and for inductors in other technology process). This issue is being investigated by the provider of the EM simulator at the time of writing this Thesis report.

The impact of the PVT variations in the overall circuit composed by the VCO and ILFD has been analysed. The activities related to the investigation of PVT variations effects in CMOS RF ICs presented in this Thesis have provided a contribution inside the framework of a European project in which the research group, in which this Thesis has been developed, participates (ENIAC MODERN project). A PLL architecture considering a frequency calibration strategy based on the results of the PVT variations simulations has been proposed. Such PLL is the subject of a registered patent of the author.

In order to perform the measurements of the test circuit a stay of one week in the DACLE/LAIR on-wafer probing Laboratory of CEA-Leti, in MINATEC, Grenoble (France), has been done last October 2011.

The enormous difficulty and open issues inherent to the current available CMOS technologies and devices modelling for mm-W ICs design have been encountered and faced up in this Thesis. In order to allow mass-production for electronics consumers demanding low cost mm-W transceivers, the CMOS technologies and passives modelling processes should achieve higher accuracy.

9.1   Summary of Contributions and Future Works

As a summary of the main activities related to this Thesis, the following contributions have crystallized:

- − The design of a 60 GHz, wide locking range 60 GHz divide-by-two ILFD with continuous tuning capability that has been presented at the DCIS 2010 Conference, [1].

- − The design of a 60 GHz, 4-bits, discrete tuned, low power, wide locking range 60 GHz divide-by-two ILFD that has been presented at the ESSCIRC 2010 Conference, in the fringe poster session[2].

- − A patent related to a PLL architecture based on the VCO and ILFD co-design presented in this Thesis, [3], which considers a frequency calibration to overcome the critical issue related to PVT variations. Such patent was registered last January 2011.

- − A contribution to the MOdeling and DEsign of Reliable, process variation-aware Nanoelectronic devices, circuits and systems (MODERN) project, of the European Nanoelectronics Initiative Advisory Council (ENIAC). A summary of the results achieved in this Thesis regarding PVT variations has been included in the final version of the deliverable document [4].

As future works, the 60 GHz VCO and divide-by-two ILFD overall circuit should be re-designed to be scaled in the 45 nm or 32 nm CMOS processes. In parallel, the issue related to phase noise and I/Q generation in direct-conversion transceiver for 60 GHz applications should be addressed. A 60 GHz PLL, considering a frequency calibration circuit for robust operation taking into account the PVT variations, could be implemented, once that the previously described issues are solved. Otherwise, if the operation frequency will reveal a limit to the implementation of a direct-conversion transceivers, other architectures will be considered in order to design and implement a PVT variations aware CMOS PLL, for WirelessHD^{TM} or other wide band requiring applications at mm-W.

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APPENDIX A

Procedures contained in the Procedures.il file. They are pre-defined functions that can be used in expressions inside Cadence SpectreRF calculator or simulation environment. They are used to extract single-ended S-parameters, impedances and admittances from differential S-parameters measurements.

Lines to be added at the end of the .cdsinit file to load some functions and bindkeys.

```
;--------------------------------LOAD PROCEDURES FOR ARTIST-------------------------

printf ( "Loading Procedure.il" )

load ( "/home/davide/ST65_7M/Procedures.il" )

procedure(GD(s11 s12 s21 s22)

let((out)

out=((2*s11-s21)*(1-s22-s12)+(1-s11-s21)*(1+s22-2*s12))/((2-s21)*(1-s22-s12)+(1-s11-s21)*(1+s22))

);let

);procedure

procedure(ZD(s11 s12 s21 s22)

let((out)

out=50*((1+GD(s11 s12 s21 s22))/(1-GD(s11 s12 s21 s22)))

);let

);procedure

procedure(YD(s11 s12 s21 s22)

let((out)

out=(1-GD(s11 s12 s21 s22))/(50*(1+GD(s11 s12 s21 s22)))

);let

);procedure

procedure(Qs(s11 s12 s21 s22)

let((out)

out=imag(ZD(s11 s12 s21 s22))/real(ZD(s11 s12 s21 s22))

);let
```

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);procedure

procedure(Rs(s11 s12 s21 s22)

let((out)

out=real(ZD(s11 s12 s21 s22))

);let

);procedure

procedure(Cs(s11 s12 s21 s22)

let((out)

out=-1/(imag(ZD(s11 s12 s21 s22))*2*pi*xval(YD(s11 s12 s21 s22)))

);let

);procedure

procedure(Cpe(s11 s12 s21 s22)

let((out)

out=imag(YD(s11 s12 s21 s22))/(2*pi*xval(YD(s11 s12 s21 s22)))

);let

);procedure

procedure(Ls(s11 s12 s21 s22)

let((out)

out=imag(ZD(s11 s12 s21 s22))/(2*pi*xval(YD(s11 s12 s21 s22)))

);let

);procedure

procedure(Rpe(s11 s12 s21 s22)

let((out)

out=real(ZD(s11 s12 s21 s22))*(1+Qs(s11 s12 s21 s22)*Qs(s11 s12 s21

s22))

);let

);procedure

procedure(Xpe(s11 s12 s21 s22)

let((out)

out=imag(ZD(s11 s12 s21 s22))*((Qs(s11 s12 s21 s22)*Qs(s11 s12 s21

s22)+1)/(Qs(s11 s12 s21 s22)*Qs(s11 s12 s21 s22)))

);let

);procedure

procedure(wo(s11 s12 s21 s22)

let((out)

out=xmax(mag(ZD(s11 s12 s21 s22)) 1)

);let

);procedure

procedure(Qo(s11 s12 s21 s22)

let((out)

  res=xmax(mag(ZD(s11 s12 s21 s22)) 1)

  imp=mag(ZD(s11 s12 s21 s22))

  impo=value(imp res)

  bw=bandwidth(imp 3 "band")

  out=res/bw

);let

);procedure

APPENDIX B

Sintetizador de frecuencia y divisor de frecuencia por D basado en la topología de enganche por inyección
P201130084
Inventores: Davide Brandano y Jose Luis Gonzalez Jimenez

<u>Sector de la técnica</u>

La presente invención concierne, en un primer aspecto, a un sintetizador de frecuencia que incluye un VCO y un ILFD, y más particularmente a un sintetizador de frecuencia que proporciona una calibración de frecuencia, de ambos, el VCO y el ILFD, que garantiza que la frecuencia de salida del VCO, que es la frecuencia de entrada del ILFD, pueda ser siempre dividida adecuadamente por el ILFD.

Un segundo aspecto de la invención concierne a un divisor de frecuencia por D basado en la topología de enganche por inyección, o ILFD, adaptado para su inclusión en el sintetizador de frecuencia propuesto por el primer aspecto.

<u>Estado de la técnica anterior</u>

En general, la arquitectura basada en divisores ILFD resulta atractiva e interesante por varios motivos, principalmente por su bajo consumo de potencia y por su capacidad de alta velocidad. Por otra parte, el principal inconveniente viene dado por el limitado ancho de banda, que se refleja en un margen de enganche reducido si se compara con otras topologías de divisores de frecuencia, haciendo difícil su integración en un PLL para la conversión directa de un transductor operando a altas frecuencias, i.e. ondas milimétricas.

Por este motivo es indispensable maximizar el margen de enganche del ILFD si se quiere considerar la ventaja que supone una arquitectura con bajo consumo de potencia. Para aplicaciones de alta frecuencia, como WHDMI, no funcionan otras topologías de divisores, ya que los requerimientos de altas velocidades suponen un impedimento en estos casos.

Para incrementar las posibilidades de mercado de las aplicaciones de alta frecuencia, como WHDMI, son necesarios productos con un bajo coste de producción y un bajo consumo de potencia en el ámbito de la electrónica de consumo, lo que pone de relieve la necesidad de alternativas a las caras tecnologías existentes, como las que emplean Arsenio de Galio (GaAs) o Fosfito de Indium (InP), que actualmente son ampliamente usadas en la fabricación de circuitos integrados monolíticos de microondas (MMIC).

La tecnología CMOS resulta aún hoy muy atractiva desde una perspectiva de costes, pero las variaciones PVT para estos procesos, especialmente a altas frecuencias, como en la banda de ondas milimétricas, son altas y eso crea la necesidad de sistemas que garanticen una frecuencia de calibración para cubrir correctamente la banda de interés.

Por la patente US7804367 se conoce un sintetizador de frecuencia para su uso en un circuito integrado, que utiliza un VCO con un valor bajo de ganancia Kvco, y que tiene un tiempo corto de calibración automática de frecuencia, y es capaz de hacer frente, de manera automática, a cambios

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en el entorno, así como un método de frecuencia de calibración. El sintetizador de frecuencia incluye un divisor de referencia, un detector de fase, un divisor principal, un circuito de bomba de carga, un filtro en bucle, un primer interruptor, un segundo interruptor, un VCO, y un bloque de calibración automática de frecuencia. El método de calibración de frecuencia incluye una etapa de inicialización y unas etapas de ejecución de una serie de algoritmos.

El sintetizador propuesto por US7804367 realiza, de forma rápida y sencilla, una calibración de frecuencia en modo grueso usando la señal de referencia y una salida de un pre-escalador, lo que reduce el consumo de energía del sintetizador de frecuencia y las dimensiones del área donde se implementa el mismo. El sintetizador obtiene efectivamente un enganche de frecuencia en un corto período de tiempo, y utiliza el VCO con menos ruido. El sintetizador afronta de forma automática un cambio en las condiciones del entorno, evitando así el mal funcionamiento de un PLL causado por un cambio en la temperatura.

US7154348 describe un sintetizador de frecuencia que incluye un circuito de calibración de frecuencia adaptativo y un PLL, y que es capaz de trabajar en un modo de enganche de frecuencia y en un modo de enganche de fase. En el modo de enganche de frecuencia, el circuito de calibración de frecuencia adaptativo compara la frecuencia de una señal de entrada con la frecuencia de una señal de salida de un oscilador controlado por tensión del PLL y genera unos bits de control como resultado de la comparación. El oscilador controlado por tensión tiene una pluralidad de curvas características de funcionamiento y selecciona una de ellas en respuesta a los bits de control. En el modo de enganche de fase, el PLL controla una fase de salida del oscilador de voltaje controlado mediante una tensión de sintonización de la curva característica de operación seleccionada.

El sintetizador ajusta con precisión la fase del oscilador en un modo de enganche de fase cuando se determinan, en modo de frecuencia, los bits de control, reduciendo así y controlando con precisión el tiempo de configuración. El sintetizador puede lograr una pequeña ganancia para el oscilador y por lo tanto puede generar frecuencias precisas en una variedad de sistemas de transmisión y recepción RF, tales como GSM, GPRS, CDMA, CDMA de banda ancha y Bluetooth.

La patente EP1271788 propone un sintetizador de frecuencia para su uso en comunicaciones de radio para generar una señal de frecuencia estable, que incluye un circuito VCO con dos o más estados operacionales en cada uno de los cuales el circuito VCO es operable para proporcionar la activación de un PLL seleccionado, mediante unos medios de conmutación incluidos en el circuito VCO, de entre dos o más PLLs diferentes conectables al circuito VCO.

Explicación de la invención

La presente invención concierne a un sintetizador de frecuencia, que comprende:

- un oscilador controlado por tensión, o VCO, que proporciona, por una salida, al menos una señal de salida con una frecuencia determinada f_{VCO}; y

- un divisor de frecuencia por D basado en la topología de enganche por inyección, o ILFD, con una entrada conectada a dicha salida de dicho VCO, y que proporciona por una salida, en condiciones de enganche, una señal con una frecuencia de enganche f_{VCO}/D, siendo D un entero.

A diferencia de los sintetizadores de frecuencia convencionales, en el propuesto por la invención, de manera característica, el VCO está previsto para trabajar según una pluralidad de curvas de frecuencia distintas, el ILFD está previsto para trabajar según una pluralidad de frecuencias de auto-resonancia distintas, y el sintetizador de frecuencia comprende un circuito de calibración de frecuencia previsto para generar y enviar a unas respectivas entradas de control de dichos VCO e

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ILFD al menos una señal de sintonización, para sintonizar, de manera simultánea, al VCO a una curva de frecuencia determinada, y al ILFD a una frecuencia de auto-resonancia determinada.

Para un ejemplo de realización, el circuito de calibración de frecuencia está previsto para enviarle a ambas entradas de control, la del VCO y la del ILFD, la misma señal de sintonización, la cual es, para una realización no limitativa, una señal digital en la forma de una palabra de n bits.

El sintetizador de frecuencia comprende un bus de n bits por el que enviar dicha palabra de n bits a las respectivas entradas de control del VCO y del ILFD, según un ejemplo de realización.

Para otro ejemplo de realización, el circuito de calibración de frecuencia está previsto para generar como mínimo dos señales de sintonización distintas y enviarle una a la entrada de control del VCO y la otra a la entrada de control del ILFD, señales de sintonización las cuales son, para una realización no limitativa, dos respectivas señales digitales, en la forma de una palabra de n bits y una palabra de m bits.

El sintetizador de frecuencia comprende, según un ejemplo de realización, un bus de n bits por el que enviar dicha palabra de n bits a la entrada de control del VCO y un bus de m bits por el que enviar dicha palabra de m bits a la entrada de control del ILFD.

El circuito de calibración de frecuencia es apto para variar el valor de dicha o dichas señales de sintonización, dentro de un rango de valores correspondiente a un rango de frecuencias de trabajo del VCO y del ILFD, con el fin de hacerlos trabajar en unas u otras frecuencias de operación.

Según un ejemplo de realización, el circuito de calibración está dispuesto para recibir, respectivamente, a través de una primera y una segunda entradas, una señal con una frecuencia de referencia f_{REF}, y la señal de salida de dicho ILFD a dicha frecuencia de enganche f_{VCO}/D o tras dividirse por al menos otro divisor de frecuencia adicional, estando el circuito de calibración previsto para comparar las señales recibidas por sus dos entradas y para generar dicha o dichas señales de sintonización como resultado de dicha comparación.

Para otros ejemplos de realización menos preferidos, el circuito de calibración genera las señales de sintonización por otros medios distintos a la mencionada comparación de señales.

Según un ejemplo de realización preferido, el sintetizador de frecuencia está formado por un lazo de seguimiento de fase, o PLL (Phase-Locked Loop), siendo el VCO de banda ancha y el ILFD de ancho margen de enganche.

Otros ejemplos de realización se hallan descritos en las reivindicaciones adjuntas y en un apartado posterior de la presente memoria descriptiva.

Mediante el sintetizador de frecuencia propuesto por el primer aspecto de la invención se consigue incrementar el margen de enganche de un ILFD integrado en un PLL, reduciendo el impacto de las variaciones de Proceso, Voltaje y Temperatura (PVT) en un circuito integrado, ya que la curva de frecuencia generada por el VCO está siempre relacionada con la propia frecuencia de auto-resonancia del ILFD, debido a que la frecuencia más baja y la más alta generadas por el VCO corresponden, a cada momento, a la más baja y la más alta, respectivamente, de las frecuencias de auto-resonancia del ILFD.

No es necesario añadir más circuitos para ajustar las frecuencias de calibración, lo que supone una evidente ventaja en términos de área de chip y de consumo de potencia, ya que la topología del ILFD permite la arquitectura de más bajo consumo en cuanto a divisores de frecuencia se refiere.

El funcionamiento del sintetizador de frecuencia propuesto, y en particular la operativa del circuito de calibración de frecuencia para generar y aplicar la señal o señales de sintonización comentadas, constituyen una metodología que, sin bien no se ha reivindicado, es objeto de protección de manera independiente a los dos aspectos de la presente invención reivindicados.

Un segundo aspecto de la invención concierne a un divisor de frecuencia por D basado en la topología de enganche por inyección, o ILFD, previsto para su inclusión en el sintetizador de frecuencia según el primer aspecto de la invención.

Breve descripción de los dibujos

Las anteriores y otras ventajas y características se comprenderán más plenamente a partir de la siguiente descripción detallada de unos ejemplos de realización con referencia a los dibujos adjuntos, que deben tomarse a título ilustrativo y no limitativo, en los que:

La Figura 1 muestra la arquitectura típica de un PLL, donde (1) es el Detector de Fase-Frecuencia, (2) es el filtro pasa bajo (LPF) que genera una señal en continua (Vc) que controla el VCO (3) permitiendo generar la frecuencia f_0 requerida en función de la señal de error que proporciona el Detector de Fase-Frecuencia (1), (4) es el divisor por D, o divisor de frecuencia, donde D es el factor de división, que puede ser 2, 3 ó 4 (básicamente un entero), (5) es una cadena divisora, que disminuye la frecuencia de la señal de salida del divisor de frecuencia (4) permitiendo al Detector de Fase-Frecuencia (1) hacer una comparación con la frecuencia (f_{REF}) del Oscilador Local (LO).

La Figura 2 muestra la arquitectura del sintetizador de frecuencia propuesto por la invención, para un ejemplo de realización donde éste está formado por un PLL. Los bloques (1), (2), (3) y (4) son los mismos que en la Figura 1, excepto por la arquitectura del VCO (3), que es un VCO como el mostrado en la Figura 4, con un banco de varactores (Figura 11), controlado por n bits. El divisor por D de frecuencia (4) es un divisor por D ILFD, como el mostrado en la Figura 3, basado en una topología LC, con un banco de varactores (8) controlado por los mismos n bits que controlan el VCO (3). (6) es un Circuito de Calibración de Frecuencia encargado de proporcionar una palabra de n bits como resultado de la comparación de frecuencias de la señal del LO a f_{REF} y de la señal divida proveniente del VCO en lazo de realimentación.

La Figura 3 muestra el circuito esquemático del ILFD (4) del sintetizador ilustrado por la Figura 2.

La figura 4 muestra el circuito esquemático de un VCO (3), del sintetizador de frecuencia de la Figura 2.

En las Figuras 5 y 6 se muestra un ejemplo del esquema del tanque LC del ILFD (4) y del tanque LC del VCO (3), respectivamente. Los inductores L_I (7) y L_V (9), así como los bancos de varactores C_{VI} (8) y C_{VO} (11) y el varactor Cv (10), están diseñados para que el VCO y el ILFD resuenen en una banda a f_0 y $\approx f_0/D$ respectivamente, como frecuencias centrales, en función de los n bits de control y de la tensión en continua Vc.

La Figura 7 muestra una arquitectura para implementar un banco de varactores para sintonización discreta, en este caso controlado por 4 bits, para proporcionar un cambio de capacidad escalado en binario.

La Figura 8 muestra una gráfica con las curvas de frecuencias operativas del VCO, en consecuencia con la estructura de PLL mostrada en la Figura 2, donde n=3, en función del voltaje en continua Vc.

La Figura 9 muestra un ejemplo de la frecuencia del VCO (3) y de la salida de frecuencia del ILFD (4), en condiciones de enganche en un PLL como el mostrado en la Figura 2, en función de los n bits de control, para un tensión de operación dada del VCO (Vc) que es la salida en continua del filtro paso bajo (2). En el ejemplo de la figura, n=4 y D=2 y el rango de frecuencia de operación es aquél para un PLL operando a frecuencias de ondas milimétricas.

La Figura 10 muestra la salida en frecuencia del ILFD, como el mostrado en la Figura 3, antes y después que ocurra el enganche, para D=2 y n=4, donde Pin = 0 dBm a 65 GHz.

La Figura 11 muestra las curvas de sensibilidad del ILFD, como el mostrado en la Figura 3, que puede implementarse en el PLL de la Figura 2, para D=2 y n=4.

La Figura 12 muestra la curva resultante de los diferentes cruces entre las curvas de sensibilidad adyacentes mostradas en la gráfica de la Figura 11. En la Figura 12 las condiciones son las mismas que en la Figura 11.

Descripción detallada de unos ejemplos de realización

La presente invención hace referencia a un sintetizador de frecuencia, o PLL, que para un ejemplo de realización se encuentra ilustrado en la Figura 2, y que está formado por un VCO 3 y un divisor de frecuencia por D 4 basado en la topología de enganche por inyección.

Tanto el VCO 3 como el ILFD 4 están basados en tanques LC y controlados por una tira de bits, que por simplicidad en la siguiente descripción se asumirá como única y de longitud n, siendo n un entero. El factor de división D es tal que D=1, 2, 3, 4… es decir un entero.

De la Figura 2 se deduce que los n bits de control son empleados para darle 2^n curvas de frecuencias de operación al VCO 3, como puede verse, por ejemplo, en la Figura 8 para el caso de n=3. Dependiendo de la salida del bus del Circuito de Calibración de Frecuencia 6, el VCO 3 selecciona una curva sobre las 2^n curvas de frecuencia de operación. El Circuito de Calibración de Frecuencia 6 recibe como entradas la señal del Oscilador Local a frecuencia f_{REF} y la señal dividida procedente del VCO 3, y proporciona una salida de n bits de control como resultado de la comparación entre las dos frecuencias de entrada, para ajustar y asignar al VCO 3 la curva de frecuencia adecuada. Ello puede lograrse cambiando la capacidad del banco de varactores 11 del VCO 3 por medio de n bits de control. Una vez establecida, la palabra binaria $[b_{n-1}, b_{n-2},…, b_0]$ provoca un cambio en la capacidad en el banco de varactores 11 del VCO 3, permitiendo al VCO 3 establecer la curva de frecuencia apropiada sobre la totalidad de curvas de frecuencias operativas (ver Figura 8).

Los mismos n bits de control pueden utilizarse también para seleccionar la frecuencia de auto-resonancia del ILFD 4. Para un ejemplo de realización, ello se consigue cambiando la capacidad del banco de varactores 8 por medio de los mismos n bits de control. Una vez establecida, la palabra binaria $[b_{n-1}, b_{n-2},…, b_0]$ provoca un cambio en la capacidad en el banco de varactores 8 del ILFD 4, permitiendo a éste establecer la frecuencia de auto-resonancia apropiada sobre las 2^n posibles frecuencias de oscilación disponibles.

Como consecuencia de la salida del Filtro Paso Bajo 2 y de las salidas del Circuito de Calibración de Frecuencia 6, la frecuencia de resonancia del VCO 3 se establece en f_0 y la frecuencia de resonancia del ILFD se establece en f_0/D, aproximadamente. Una vez que la tira de bits de control se ha conformado, se establece la curva de frecuencia operativa del VCO 3 así como la frecuencia de resonancia del ILFD 4. La sintonización discreta sucede simultáneamente para el VCO 3 y el ILFD 4.

De esta manera se establece la frecuencia de calibración entre el ILFD 4 y el VCO 3 y se inyecta la frecuencia de oscilación f_{VCO} en el ILFD 4, que oscila por sí mismo a una frecuencia de auto-resonancia de f_{VCO}/D, aproximadamente. Si la potencia de salida del VCO 3 es suficientemente elevada para el enganche por inyección del divisor por D 4, la frecuencia de salida del ILFD 4 es exactamente f_{VCO}/D.

En esta situación el ILFD 4 está en estado de enganche y su frecuencia de salida es exactamente igual a f_{VCO}/D. La frecuencia de realimentación del PLL disminuye, relajando la división de frecuencia del siguiente bloque 5. Además el margen de enganche del ILFD 4 se extiende (Figura 11 y Figura 12) ya que con esta técnica la frecuencia de salida del ILFD 4 es capaz de cubrir la totalidad del rango de sintonía del VCO 3 también en presencia de variaciones PVT (Figura 9, donde n=4 y D=2).

El ILFD 4 y el VCO 3 están diseñados para que la capacidad del banco de varactores 11 del VCO 3 más baja y más alta correspondan, respectivamente, a la capacidad del banco de varactores 8 del ILFD 4 más baja y más alta. En la Figura 7 puede verse un ejemplo de banco de varactores compuesto de cuatro grupos de varactores, 12, 13, 14 y 15, para el ILFD 4 y el VCO 3, controlados por la palabra b[3:0], correspondiente a n=4.

El tanque del ILFD 4 (Figura 7) y el tanque del VCO 3 (Figura 8) están diseñados para resonar a aproximadamente f_O/D, y f_O, respectivamente, dependiendo de los n bits de control, para el ILFD, y dependiendo de los mismos n bits de control y de la tensión de salida en continua Vc del LPF 2 para el VCO 3.

Un ejemplo de realización, que no debe ser interpretado como una restricción del alcance de la invención, sino como un ejemplo de cómo puede implementarse el sintetizador de frecuencia de la invención, se presenta para un PLL, como el mostrado en la Figura 2, operando a frecuencias de ondas milimétricas: n=4 y D=2. Se establece una tira de 4 bits de control, es decir 0000, según la salida del Circuito de Calibración de Frecuencia 6. En consecuencia, la frecuencia de resonancia del ILFD 4 se establece en el mínimo valor, así como la frecuencia del VCO 3, para una tensión dada Vc, en función de la salida del LPF 2. Cuando para un nivel de potencia dado de salida del VCO 3, la frecuencia de salida del ILFD 4 es exactamente $f_{VCO}/2$, se sitúa un punto en un plano cartesiano [frecuencia del VCO, potencia de salida del VCO] para construir, repitiendo la misma operación para las 16 posibles combinaciones de bits (0001, 0010,…, 1111), curvas como las mostradas en la Figura 11.

Todas las dieciséis curvas de sensibilidad del ILFD del ejemplo de realización previo pueden también así obtenerse, mostrándose en la Figura 11 solamente las más significativas. Analizando el cruce entre curvas adyacentes, como las partes marcadas de las curvas de la Figura 11 indican, es posible obtener la totalidad ajustable (o sintonizable) del margen de enganche alcanzado para una potencia de entrada dada para el ILFD 4, que es la salida de potencia del VCO 3, como muestra la gráfica de la Figura 12. Como consecuencia, con el objetivo técnico de esta invención, se amplía el margen de enganche del ILFD 4.

A continuación se hace una descripción más detallada de la invención, para unos ejemplos de realización.

Tal y como se ha dicho anteriormente, el sintetizador de frecuencia propuesto por la invención se ha ilustrado en la Figura 2, para un ejemplo de realización para el que éste está formado por un PLL, con los elementos arriba mencionados, es decir un VCO 3 y un ILFD 4, ambos controlados por el mismo bus de n bits, un detector de Fase-Frecuencia 1, un filtro paso bajo 2, un Circuito de Calibración de Frecuencia 6 y una cadena de divisores 5.

Todos los bloques del circuito del PLL en la Figura 2, exceptuando eventualmente el LPF 2, se encuentran integrados, para un ejemplo de realización. Además, todos los bloques de la Figura 2 se implementan, para una realización, en tecnología CMOS, incluyendo el VCO 3 y el ILFD 4, garantizando el rango de frecuencias operativo del PLL hasta la banda de ondas milimétricas.

El Detector de Fase-Frecuencia 1 compara la fase de la señal de referencia del oscilador local f_{REF} con la fase de la señal de realimentación procedente de la Cadena de Divisores 5 y genera una señal de error en función del resultado de la comparación. Funciona como un detector de error en lazo de realimentación.

El LPF 2 es el bloque encargado de suprimir las componentes a altas frecuencias del Detector de Fase-Frecuencia 1, dando como salida una tensión en continua Vc que controla, en parte, la frecuencia del VCO.

El VCO 3 genera una señal de salida a $f_{VCO} = f_0$ haciendo uso de los bits b[n-1:0], provenientes del Circuito de Calibración de Frecuencia 6, y de la tensión en continua Vc, que sale del LPF 2. El bus de bits de control b[n-1:0] está compuesto de n bits (siendo n un entero). El VCO 3 tiene diversas curvas de frecuencias operativas, concretamente 2^n.

El ILFD 4, en condiciones de no enganche, genera una señal de salida a aproximadamente f_0/D haciendo uso de los bits de control b[n-1:0] provenientes del Circuito de Calibración de Frecuencia 6. La tira de bits de control b[n-1:0] está formada por n bits (siendo n un entero). El ILFD 4 tiene diversas curvas de frecuencias de auto-resonancia, concretamente 2^n.

Para una tira concreta de bits b[n-1:0], la frecuencia de auto-resonancia más baja y más alta del ILFD 4 corresponden, simultáneamente, a la curva de frecuencia operativa más baja y más alta del VCO 3.

El Circuito de Calibración de Frecuencia 6 proporciona a la salida una tira de n bits de control b[n-1:0] en función del resultado de la comparación entre la señal de realimentación proveniente de la Cadena de Divisores 5 y la señal de referencia a f_{REF}.

El bus de n bits se conecta al VCO 3 y al ILFD 4 y se usa para controlar la curva de frecuencia del VCO 3 y la frecuencia de auto-resonancia del ILFD 4.

El VCO 3 selecciona una curva de entre las 2^n posibles en función de los bits de control b[n-1:0], como los mostrados por la Figura 6 donde n=3.

El ILFD 4 selecciona una frecuencia de auto-resonancia sobre las 2^n posibles en función de los bits de control b[n-1:0].

Para un ejemplo de realización, la tira de bits de control b[n-1:0] es la misma para el ILFD 4 y el VCO 3, como se ilustra en la Figura 2. No obstante, para otro ejemplo de realización el Circuito de Calibración de Frecuencia 6 genera y proporciona en su salida dos tiras de bits de control b[n-1:0] y k[m-1:0] (n ≠ m) en función de la comparación de frecuencias. En tal caso, los bits b[n-1:0] controlan la curva de frecuencia operativa del VCO 3 y los bits k[m-1:0] la frecuencia de auto-resonancia del ILFD 4, y la frecuencia de resonancia del ILFD 4 más baja y más alta corresponden, simultáneamente, a la curva de frecuencia operativa más baja y más alta del VCO 3.

La Figura 3 muestra un circuito esquemático del ILFD 4 de la Figura 2, para un ejemplo de realización. En la Figura 3 un inductor L_I 7 (que puede implementarse como un inductor diferencial) se conecta entre el drenador del PMOS M_{bias_i} y los nodos V_{out_i+} y V_{out_i-}. Un banco de varactores 8 controlado por n bits se conecta entre los nodos V_{out_i+} y V_{out_i-}.

La puerta del transistor M1I se conecta a V_{out_i+}, que es el drenador del transistor M2I, mientras que la puerta del transistor M2I se conecta a V_{out_i-}, que es el drenador del transistor M1I. Ambas fuentes de los transistores M2I y M1I están conectadas a tierra, por ejemplo a través de una línea de transmisión, que se ha omitido en el esquema. La relación W/L de M1I y de M2I es la misma.

El transistor de polarización M_{bias-i}, es decir la etapa de entrada del ILFD 4 en la Figura 3, se usa para proporcionar un camino para la señal de entrada y un camino para la polarización CC. Si no hay señal de entrada o su amplitud (resultante de la corriente de inyección I_{inj}) es demasiado baja,

el ILFD 4 oscila a su propia frecuencia de resonancia, dependiendo de los bits de control b[n-1:0]. En estado de enganche, los transistores M1I y M2I conmutan a un régimen de f_{in}/D mientas M_{bias_i} inyecta una corriente de suficiente amplitud para el enganche por inyección del ILFD 4.

Para el caso de utilizar un ILFD divisor por 2 (D=2), de una forma similar a un mezclador de equilibrado sencillo, M1I y M2I trasladan la entrada a $f_{in} \pm f_{in}/2$, inyectando el resultado al tanque del ILFD. Esta traslación viene acompañada de un factor de conversión $2/\pi$ si el par conectado en cruz (M1I y M2I) conmutan abruptamente y la capacidad del nodo P se desprecia. Como resultado, la corriente inyectada al tanque del ILFD a $f_{in}/2$ tiene un valor de pico de $2/\pi \cdot I_{inj}$, permitiendo encontrar la siguiente expresión para el margen de enganche del ILFD de la Figura 3:

$$\Delta\omega_{f_{in}/2} = \frac{\omega_n}{2Q}\eta\frac{2}{\pi} \qquad\qquad 1)$$

donde η es la relación de inyección igual a I_{inj} / I_{osc}, donde I_{osc} es la corriente de oscilación, aproximadamente igual a la corriente de cola del circuito de la Figura 3, ω_n es la frecuencia angular de resonancia del tanque del ILFD y es igual a $2\pi \cdot (f_{in}/2)$ cuando el circuito funciona correctamente. Q es el factor de calidad del tanque del ILFD.

Una capacidad C_{dec} se usa para desacoplar la señal en continua de la fuente de entrada f_{in}, mientras que el resistor R se usa para atenuar la señal RF, garantizando la tensión de polarización.

La Figura 4 muestra un circuito esquemático del VCO 3 de la Figura 2. En la Figura 4, un inductor L_V 9 (que puede ser implementado como un inductor diferencial) se conecta entre el drenador del PMOS M_{bias_v} y los nodos V_{out+} y V_{out-}. Un banco de varactores 11 controlado por n bits se conecta entre los nodos V_{out-} y V_{out+} así como también un único varactor 10. Una capacidad C_f se encarga del filtraje del ruido.

La puerta del transistor M1V se conecta a V_{out+}, que es el drenador del transistor M2V, mientras que la puerta del transistor M2V se conecta a V_{out-}, que es el drenador del transistor M1V. Ambas fuentes de los transistores M2V y M1V están conectadas a tierra, por ejemplo a través de una línea de transmisión que se ha omitido en el esquema. La relación W/L de M1V y de M2V es la misma. La Figura 5 muestra un circuito esquemático del tanque del ILFD 4 de la Figura 3. El banco de varactores 8 se diseña para que resuene la inductancia LI 9 del tanque del ILFD 4 a la frecuencia de resonancia.

El cambio en la capacidad del banco de varactores 8 está garantizado por medio del bus de n bits. El banco de varactores 8 permite seleccionar la frecuencia de auto-resonancia del ILFD 4 requerida, en función de la tira de n bits que proporciona el Circuito de Calibración de Frecuencia 6. El tanque del ILFD se diseña para resonar a f_0/D aproximadamente, dependiendo de los n bits. Esto hace que el ILFD pueda proporcionar 2^n frecuencias de auto-resonancia.

La capacidad más baja y la más alta del banco de varactores 8 del ILFD 4 corresponden, con la misma tira de bits, a la curva de capacidad más baja y más alta, respectivamente, del banco de varactores 11 del VCO 3. En consecuencia, la frecuencia de auto-resonancia más baja y la más alta del ILFD 4 corresponden, con la misma tira de bits, a la curva de frecuencia operativa más baja y más alta, respectivamente, del VCO 3.

La Figura 6 muestra un circuito esquemático del tanque del VCO 3 de la Figura 4. El banco de varactores 11 se diseña para que, junto con el único varactor 10, hacer resonar a la inductancia L_V 9 del tanque del VCO 3 a la frecuencia de resonancia. El cambio en la capacidad del banco de

varactores 11 está garantizado por medio del bus de n bits, mientras que el cambio en la capacidad del varactor único 10 se asegura por medio de la salida en continua Vc del LPF 2.

El banco de varactores 11 permite seleccionar la curva de frecuencia del VCO 3 requerida, como las mostradas en la Figura 8 donde n=3, en función de la tira de n bits que proporciona el Circuito de Calibración de Frecuencia 6. El varactor único 10 permite obtener una sintonización continua y seleccionar la frecuencia del VCO 3 requerida en función de la salida en continua Vc del LPF 2.

El tanque del VCO está diseñado para resonar a f_0, dependiendo de los n bits y de la tensión continua de control Vc. El VCO proporciona 2^n curvas de frecuencias operativas.

La Figura 7 muestra un circuito esquemático de un banco de varactores controlado por n bits. En el caso de la Figura 7, n=4. Se compone de n grupos de varactores en paralelo 12, 13, 14 y 15, donde n=4 en el ejemplo de la Figura 7.

Un grupo de varactores puede constituirse mediante varactores diferenciales MOS N+poly/Nwell en paralelo. La tensión de control de cada grupo de varactores está directamente conectada a una señal digital que conmuta el grupo de varactores a ON o a OFF, mediante la aplicación de una tensión continua (0 ó 1,8V en el presente ejemplo) a la puerta de los varactores diferenciales N+poly/Nwell.

La sintonización discreta, por medio de los n bits, se implementa, para un ejemplo de realización, en el VCO 3 y en el ILFD 4 usando un grupo de varactores escalado en binario. El banco de varactores produce, según una realización, un cambio en la capacidad escalada en binario si se implementa como una combinación del mismo varactor unitario 15 y los grupos de 4, 2, 1 unidades (en el caso de 3 bits de control) o grupos de 8 (12), 4 (13), 2 (14) y 1(15) unidades (en el caso de 4 bits de control, como en el caso de la Figura 7). En general, para el caso de n bits, un cambio de la capacidad escalada en binario se proporciona mediante la combinación de un conjunto de varactores agrupados a su vez en conjuntos de 2^{n-1}, 2^{n-2}, …, $2^{n-(n-1)}$, 1 elementos.

El bit menos significativo (LSB: Least Significant Bit) b_0 se conecta al varactor unitario 15, que es el varactor que proporciona un mínimo cambio en la capacidad. El segundo bit b_1 se conecta al conjunto de 2 varactores. Así en adelante, el bit más significativo (MSB: Most Significant Bit) b_{n-1} se conecta al conjunto de 2^{n-1} varactores, el cual proporciona el máximo cambio en la capacidad.

El banco de varactores 8 del ILFD 4 y el banco 11 del VCO 3 están diseñados para que la capacidad más baja y más alta del banco de varactores 8 del ILFD 4 corresponda a la capacidad más baja y más alta, respectivamente, del banco de varactores 11 del VCO 3, con la misma tira de n bits, pero también en el caso de tener dos tiras de bits diferentes b[n-1:0] y k[m-1:0] (n ≠ m) que estén controlando un VCO 3 y un ILFD divisor por D 4, respectivamente.

El banco de varactores controlados digitalmente de la Figura 7 proporciona una amplia sintonización para la compensación de PVT y la calibración de frecuencia.

La Figura 8 es una gráfica que ilustra las curvas de frecuencia del VCO 3 en función de la tensión de salida en continua Vc del LPF 2, en el caso de n=3. La frecuencia mínima f_0 del VCO 3 plasmada en la Figura 8 puede expresarse como:

$$f_{0_{min}} = \frac{1}{2\pi\sqrt{L_V(C_{VV,max} + C_{v_{max}} + C_p)}}$$

$$C_{VV,max} = \max\{C_{VV}\} = \max\{f(b[n-1:0])\} \qquad 2)$$

$$C_{v_{max}} = \max\{C_v\} = \max\{f(V_c)\}$$

En el grupo de ecuaciones 2), $C_{VV,max}$ representa el valor máximo de la capacidad del banco de varactores 11, que es función de la tira de n bits de control. C_{vmax} es el valor máximo de la capacidad del varactor único 10 del VCO 3, que es función de la tensión de salida en continua Vc del LPF 2. L_V 9 es la inductancia del tanque del VCO, mientras que C_p es la contribución de una capacidad parásita debida a las capacidades de los transistores y a los efectos capacitivos de las interconexiones en el circuito de la Figura 4.

La suma de la capacidad del banco de varactores Cvv y las capacidades Cv y Cp del varactor único del VCO 3 es la capacidad total del tanque del VCO 3, que es función de Vc y b[n-1:0].

La frecuencia máxima f_{0max} del VCO 3 es aquella tal que la variación total ΔC en la capacidad del tanque del VCO es:

$$\Delta C \geq 4 \frac{f_{0_{max}} - f_{0_{min}}}{L_V \pi^2 (f_{0_{max}} + f_{0_{min}})^3} \qquad 3)$$

para permitir al VCO 3 cubrir la banda de interés con un margen adicional para compensar las variaciones PVT. ΔC es función de Vc y b[n-1:0].

La Figura 9 es una gráfica que muestra, en dos ejes, la frecuencia del VCO 3 y la frecuencia de salida del ILFD 4 en condiciones de enganche, para una tensión de salida en continua Vc del LPF 2, como función de los bits de control b[n-1:0], donde n=4 y el factor de división D es dos (D=2). El rango de frecuencias de operación es aquél que permite al PLL trabajar a frecuencias de ondas milimétricas.

En el PLL de la Figura 2, dependiendo de los bits de control b[n-1:0] para una tensión de salida en continua Vc del LPF 2, la frecuencia de salida del VCO 3 a f_0 se inyecta en el ILFD 4. Un instante antes de que ocurra dicha inyección, el ILFD 4 está auto-oscilando a una frecuencia de $f_0/2$ aproximadamente. Una vez que la señal del VCO 3 a f_0 se inyecta en el ILFD 4, la frecuencia de salida de éste se establece exactamente en $f_0/2$ (la Figura 10 puede servir también para entender el mecanismo de enganche).

Se reporta la banda de interés, referida a un ILFD divisor por 2 y a un VCO, así como el margen adicional para compensaciones de variaciones PVT.

La Figura 10 muestra la frecuencia de salida de un ILFD divisor por 2 antes y después de que ocurra la inyección. Para obtener la respuesta del ILFD representada en la Figura 10 se ha añadido en el circuito de la Figura 3 un interruptor temporizado (omitido en el esquema) entre la capacidad de desacoplo C_{dec} y la fuente de entrada en f_{in}. Antes de que se cierre el interruptor, el ILFD auto-oscila a una frecuencia de $f_{in}/2$ aproximadamente, para una tira de bits de control dada, en este caso 1000, correspondiente a n=4. Después de 5 ns el interruptor se cierra y la señal en f_{in} se inyecta en el ILFD divisor por 2 y la frecuencia de salida del ILFD se establece exactamente en $f_{in}/2$.

La Figura 11 muestra un conjunto de curvas de sensibilidad de entrada del ILFD 4, para el caso de n=4, que se producen con los bits de control b[n-1:0] y D=2. En el eje x se representa la frecuencia del VCO 3 que se inyecta en el ILFD, así como la banda de interés. En el eje y se representa el nivel de potencia de salida del VCO 3 correspondiente a la frecuencia del VCO 3 para la cual ocurre la condición de enganche del ILFD.

El número total de curvas de sensibilidad de entrada del ILFD es 2^n. La salida del Circuito de Calibración de Frecuencia 6 selecciona una curva de sensibilidad de entrada, así como una curva de frecuencia de operación del VCO.

En la Figura 11 se muestran las curvas de sensibilidad de entrada más significativas, para el caso de un ILFD divisor por 2 (D=2) controlado por n=4 bits. Analizando los cruces entre curvas de sensibilidad de entrada adyacentes (por ejemplo 0001 con 0000 y 0010), como indican las marcas en la gráfica, es posible obtener la totalidad ajustable (o sintonizable) del margen de enganche del ILFD para el nivel más alto de potencia en el que ocurre un cruce, lo que fija el peor caso de margen de enganche del ILFD.

En la Figura 12 se muestra la curva resultante de los cruces de niveles de potencia de las curvas de la Figura 11. En el eje x se representa la frecuencia del VCO 3, inyectada en el ILFD, así como la banda de interés. En el eje y se representa el nivel de potencia de salida del VCO 3 correspondiente a la frecuencia del VCO 3 para la cual ocurre la condición de enganche del ILFD. Se muestra también el margen adicional de banda logrado para la compensación de variaciones PVT, así como la totalidad del margen de enganche del ILFD logrado para un potencia de entrada de 0 dBm.

La totalidad del margen de enganche del ILFD, para un nivel de potencia de entrada dado, ha sido extendido haciendo uso de un banco de varactores, como se muestra en la Figura 7.

Un experto en la materia podría introducir cambios y modificaciones en los ejemplos de realización descritos sin salirse del alcance de la invención según está definido en las reivindicaciones adjuntas.

Reivindicaciones

1.- Sintetizador de frecuencia, del tipo que comprende:
- un oscilador controlado por tensión, o VCO (3), que proporciona, por una salida, al menos una señal de salida con una frecuencia determinada (f_{VCO}); y
- un divisor de frecuencia por D basado en la topología de enganche por inyección, o ILFD (4), con una entrada conectada a dicha salida de dicho VCO (3), y que proporciona por una salida, en condiciones de enganche, una señal con una frecuencia de enganche f_{VCO}/D, siendo D un entero;
estando dicho sintetizador de frecuencia **caracterizado** porque dicho VCO (3) está previsto para trabajar según una pluralidad de curvas de frecuencia distintas, dicho ILFD (4) está previsto para trabajar según una pluralidad de frecuencias de auto-resonancia distintas, y porque el sintetizador de frecuencia comprende un circuito de calibración de frecuencia (6) previsto para generar y enviar a unas respectivas entradas de control de dichos VCO (3) e ILFD (4) al menos una señal de sintonización, para sintonizar, de manera simultánea, al VCO (3) a una curva de frecuencia determinada, y al ILFD (4) a una frecuencia de auto-resonancia determinada.

2.- Sintetizador de frecuencia según la reivindicación 1, caracterizado porque dicho circuito de calibración de frecuencia (6) está previsto para enviarle a ambas entradas de control, la del VCO (3) y la del ILFD (4), la misma señal de sintonización.

3.- Sintetizador de frecuencia según la reivindicación 2, caracterizado porque dicha señal de sintonización generada por dicho circuito de calibración de frecuencia (6) es una señal digital, en la forma de una palabra de n bits.

4.- Sintetizador de frecuencia según la reivindicación 3, caracterizado porque comprende un bus de n bits por el que enviar dicha palabra de n bits a las respectivas entradas de control del VCO (3) y del ILFD (4).

5.- Sintetizador de frecuencia según la reivindicación 1, caracterizado porque dicho circuito de calibración de frecuencia (6) está previsto para generar al menos dos señales de sintonización distintas y enviarle una a la entrada de control del VCO (3) y la otra a la entrada de control del ILFD (4).

6.- Sintetizador de frecuencia según la reivindicación 5, caracterizado porque dichas dos señales de sintonización generadas por dicho circuito de calibración de frecuencia (6) son dos respectivas señales digitales, en la forma de una palabra de n bits y una palabra de m bits.

7.- Sintetizador de frecuencia según la reivindicación 6, caracterizado porque comprende un bus de n bits por el que enviar dicha palabra de n bits a la entrada de control del VCO (3) y un bus de m bits por el que enviar dicha palabra de m bits a la entrada de control del ILFD (4).

8.- Sintetizador de frecuencia según una cualquiera de las reivindicaciones anteriores, caracterizado porque el circuito de calibración de frecuencia (6) es apto para variar el valor de dicha o dichas señales de sintonización, dentro de un rango de valores correspondiente a un rango de frecuencias de trabajo del VCO (3) y del ILFD (4).

9.- Sintetizador de frecuencia según una cualquiera de las reivindicaciones anteriores, caracterizado porque dicho circuito de calibración de frecuencia (6) está dispuesto para recibir, respectivamente, a través de una primera y una segunda entradas, una señal con una frecuencia de referencia f_{REF}, y la señal de salida de dicho ILFD (4) a dicha frecuencia de enganche f_{VCO}/D o tras dividirse por al menos otro divisor de frecuencia adicional, estando el circuito de calibración de frecuencia (6) previsto para comparar las señales recibidas por sus dos entradas y para generar dicha o dichas señales de sintonización como resultado de dicha comparación.

10.- Sintetizador de frecuencia según una cualquiera de las reivindicaciones anteriores, caracterizado porque que está formado por un lazo de seguimiento de fase, o PLL.

11.- Sintetizador de frecuencia según la reivindicación 10 cuando depende de la 9, caracterizado porque comprende una cadena divisora de frecuencias (5), que incluye a dicho divisor de frecuencia adicional, con una entrada conectada a dicha salida del ILFD (4) y una salida por la que proporciona una señal de salida con una frecuencia más baja que dicha frecuencia de enganche f_{VCO}/D a al menos dicha segunda entrada del circuito de calibración de frecuencia (6).

12.- Sintetizador de frecuencia según la reivindicación 11, caracterizado porque comprende un detector de fase-frecuencia (1) dispuesto para recibir, respectivamente, a través de una primera y una segunda entradas, dicha señal con una frecuencia de referencia f_{REF}, y dicha señal de salida de dicha cadena divisora de frecuencias (5), estando dicho detector de fase-frecuencia (1) previsto para comparar las señales recibidas por sus dos entradas y para generar, por una salida, una señal de error, en función del resultado de dicha comparación.

13.- Sintetizador de frecuencia según la reivindicación 12, caracterizado porque comprende un filtro paso bajo (2) con una entrada conectada a dicha salida del detector de fase-frecuencia (1) y una salida conectada a la entrada del VCO (3), para eliminar las componentes a altas frecuencias de la salida del detector de fase-frecuencia (1), proporcionando por su salida una señal continua para colaborar en el control de la frecuencia del VCO (3).

14.- Sintetizador de frecuencia según una cualquiera de las reivindicaciones anteriores, caracterizado porque el VCO (3) y el ILFD (4) están basados en tanques LC, o inductor-condensador, donde al menos parte de los condensadores de dichos tanques LC son de capacidad variable, o varactores, estando al menos parte de sus entradas de ajuste conectadas a dichas entradas de control del VCO (3) y del ILFD (4).

15.- Sintetizador de frecuencia según la reivindicación 14 cuando depende de la 13, caracterizado porque uno de dichos varactores del VCO (3) tiene su entrada de ajuste conectada a dicha salida del filtro paso bajo (2) y está previsto para ajustar su capacidad en función del valor de dicha señal continua proporcionada por el filtro paso bajo (1).

16.- Sintetizador de frecuencia según la reivindicación 14 cuando depende de la 4 o de la 7, caracterizado porque los varactores del VCO (3) y los del ILFD (4) están agrupados, respectivamente, formando conjuntos de varactores escalados binariamente, y dispuestos de manera que cada conjunto es controlado por al menos un bit de la palabra de n ó m bits recibida, para variar la capacidad total de manera escalada binariamente.

17.- Sintetizador de frecuencia según una cualquiera de las reivindicaciones anteriores, caracterizado porque está previsto para trabajar en al menos una de las siguientes frecuencias de aplicación: mm-W, WHDMI, según IEEE 802.15.3c, y banda V.

18.- Sintetizador de frecuencia según una cualquiera de las reivindicaciones anteriores, caracterizado porque el circuito de calibración (6) está previsto para sintonizar al VCO (3) y al ILFD (4) de manera que las curvas de frecuencia mínima y máxima a las que se sintoniza el VCO (3) corresponda, simultáneamente, a las frecuencias de auto-resonancia mínima y máxima de sintonización del ILFD (4).

19.- Sintetizador de frecuencia según la reivindicación 14, caracterizado porque el circuito de calibración (6) está previsto para generar y enviar dicha o dichas señales de sintonización al VCO (3) y al ILFD (4) d manera que las curvas de capacitancia mínima y máxima del tanque LC del VCO (3) correspondan, simultáneamente, a las curvas de capacitancia mínima y máxima del tanque LC del ILFD (4).

20.- Divisor de frecuencia por D basado en la topología de enganche por inyección, o ILFD, **caracterizado** porque está previsto para su inclusión en el sintetizador de frecuencia según una cualquiera de las reivindicaciones 1 a 19.
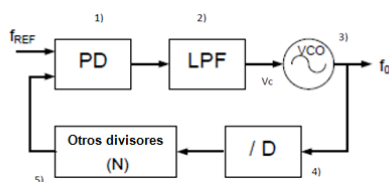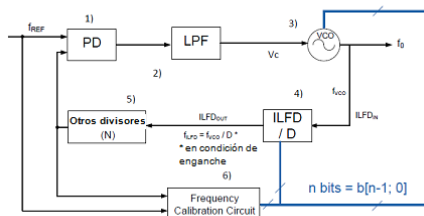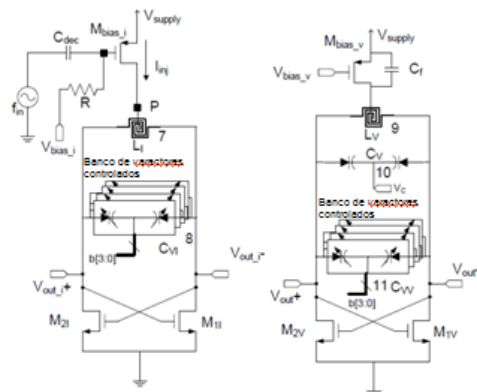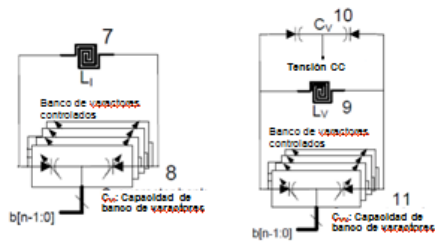

Figura 1

Figura 2

Figura 3

Figura 4

Figura 5
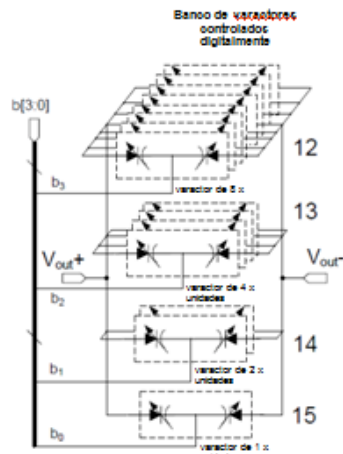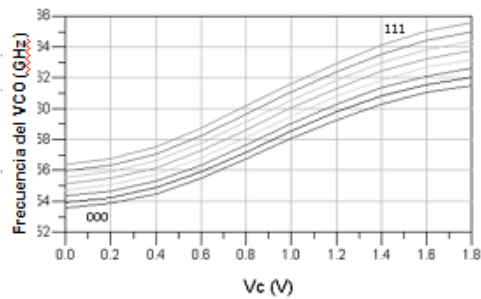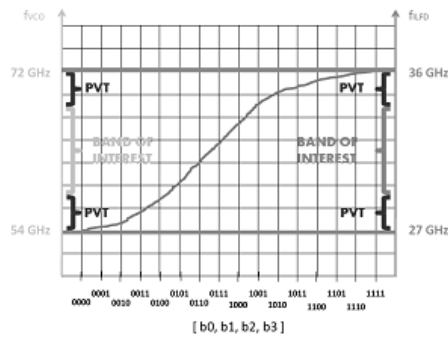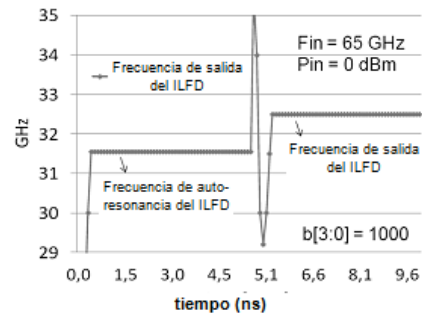

Figura 6

Figura 7

Figura 8
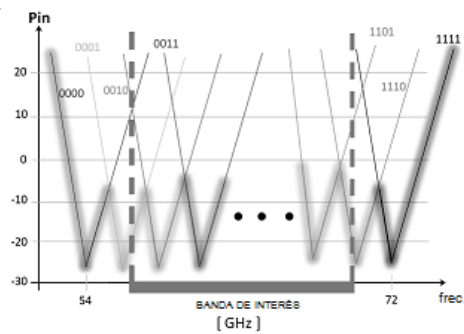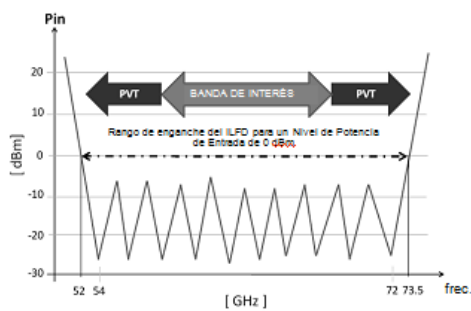
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Figura 9

Figura 10

Figura 11

Figura 12

Resumen

Sintetizador de frecuencia y divisor de frecuencia por D basado en la topología de enganche por inyección

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El sintetizador comprende:

  - un VCO (3), que proporciona una señal de salida con una frecuencia determinada (f_{VCO});

  - un ILFD (4), con una entrada conectada a la salida del VCO (3), y que proporciona, en condiciones de enganche, una señal con una frecuencia de enganche f_{VCO}/D, siendo D un entero; y

  - un circuito de calibración de frecuencia (6) que genera y envía a unas entradas de control del VCO (3) y del ILFD (4) una o más señales de sintonización, para sintonizar, de manera simultánea, al VCO (3) a una curva de frecuencia determinada, y al ILFD (4) a una frecuencia de auto-resonancia determinada.

El divisor de frecuencia por D basado en la topología de enganche por inyección, o ILFD, está adaptado para su inclusión en el sintetizador de frecuencia.