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Contributions to the design, development and evaluation of network processors for automotive zonal gateway controllers

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Contributions to the Design, Development and Evaluation of Network Processors for Automotive Zonal Gateway Controllers

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Abstract

(English version) This PhD dissertation analyzes the evolution of vehicular networks and focuses on the main network processing platform integrated in them: the Gateway (GW). First, a thorough analysis of state of the art technologies involved in vehicular networks is performed, leading to the definition of the requirements of future network processing platforms. Then, the available options in the state of the art for network processing, both in industry and academia, are analyzed. This analysis shows a gap in this area: there is currently no architecture fulfilling all the requirements of future automotive GW controllers. Moreover, Hardware (HW) accelerators and custom processor design are identified as a key differentiation factor which boosts the performance of the devices.

Linking the result of this analysis with the current trend towards application specific processors, this thesis proposes the novel Elastic Gateway (eGW) System on Chip (SoC) architecture as a high performance network processor for future zonal GW controllers. The proposed architecture aims at fulfilling the identified gap, advancing towards future GW SoC solutions. Elastic Gateway SoC concept aims at synthesizing a scalable and future-proof architecture embracing all new and already established functions and features demanded in a zonal gateway controller for the new era of mobility.

The challenge now is not only to design the right processor that can meet the requirements available today, but also to make this design suitable for the future. For this reason, the modularity, flexibility, scalability and configurability of these future processors take, more than ever, a starring role in the early design stages. This thesis is also providing a complete lifecycle methodology for the design and validation of different network processing products based on the proposed eGW SoC architecture.

Throughout this work the architecture is evaluated from a functional perspective, proving how the different technologies required in future vehicular networks are integrated in eGW and how the previously defined requirements are met. Then, a proof of concept is implemented showing the viability of the proposed concept and methodology, providing details of the experimental results. The architecture is also evaluated from a scalability point of view, looking at HW cost and power consumption, proving that eGW is able to provide a high level of performance at a reasonable cost.

Together, the eGW SoC concept and methodology become an alternative that can contribute to overcome the existing challenges, advancing over state of the art solutions.

(Versió en Català) Aquesta tesi doctoral analitza l'evolució de les xarxes vehiculars i se centra en la principal plataforma de processament de xarxa integrada: el *Gateway* (GW). Primer es realitza una anàlisi exhaustiva de les tecnologies capdavanteres involucrades en les xarxes vehiculars, que porta a la definició dels requisits de les futures plataformes de processament de xarxes. Després, s'analitzen les opcions disponibles a l'estat de l'art per al processament de xarxes, tant a la indústria com al món acadèmic. Aquesta anàlisi mostra una bretxa en aquesta àrea: actualment no hi ha cap arquitectura que compleixi amb tots els requisits dels futurs controladors GW per a automòbils. A més, els acceleradors de *hardware* (HW) i el disseny de processadors dedicats s'identifiquen com un factor de diferenciació clau que augmenta el rendiment dels dispositius.

Vinculant el resultat d'aquesta anàlisi amb la tendència actual cap als processadors d'aplicació específica, aquesta tesi proposa una nova arquitectura anomenada *Elastic Gateway (eGW) System on Chip (SoC)* com a processador de xarxes d'alt rendiment per als futurs controladors GW. L'arquitectura proposada té com a objectiu cobrir la bretxa identificada i avançar cap a futures solucions GW SoC. El concepte *Elastic Gateway SoC* té com a objectiu sintetitzar una arquitectura escalable i preparada per al futur que inclogui totes les funcions i característiques noves i ja establertes que s'exigeixen en un controlador *gateway* per a la nova era de la mobilitat.

El desafiament ara no és només dissenyar el processador correcte que pugui complir amb els requisits disponibles actualment, sinó també fer que aquest disseny sigui adequat per al futur. Per això, la modularitat, la flexibilitat, l'escalabilitat i la configurabilitat d'aquests futurs processadors cobren, més que mai, un paper protagonista en les primeres etapes de disseny. Aquesta tesi també proporciona una metodologia de cicle de vida completa per al disseny i la validació de diferents productes de processament de xarxa basats en larquitectura proposada de eGW SoC.

Al llarg d'aquest treball s'avalua l'arquitectura des d'una perspectiva funcional, demostrant com s'integren a eGW les diferents tecnologies requerides en xarxes vehiculars futures i com es compleixen els requisits definits anteriorment. Per tant, s'implementa una prova de concepte que mostra la viabilitat del concepte i la metodologia proposada, proporcionant detalls dels resultats experimentals. L'arquitectura també s'avalua des del punt de vista de l'escalabilitat, considerant el cost de recursos HW i el consum d'energia, demostrant que eGW pot proporcionar un nivell alt de rendiment a un cost raonable.

Tot plegat, el concepte i la metodologia d'eGW SoC proposen una alternativa que pot contribuir a superar els desafiaments existents, avançant sobre l'estat de l'art.

(Versión en Español) Esta tesis doctoral analiza la evolución de las redes vehiculares y se centra en la principal plataforma de procesamiento de red integrada en ellas: el *Gateway* (GW). Primero se realiza un análisis exhaustivo de las tecnologías punteras involucradas en las redes vehiculares, que lleva a la definición de los requisitos de las futuras plataformas de procesamiento de redes. A continuación, se analizan las opciones disponibles en el estado del arte para el procesamiento de redes, tanto en la industria como en el mundo académico. Este análisis muestra una brecha en esta área: actualmente no existe ninguna arquitectura que cumpla con todos los requisitos de los futuros controladores GW para automóviles. Además, los aceleradores de *hardware* (HW) y el diseño de procesadores dedicados se identifican como un factor de diferenciación clave que aumenta el rendimiento de los dispositivos.

Vinculando el resultado de este análisis con la tendencia actual hacia los procesadores de aplicación específica, esta tesis propone la nueva arquitectura *Elastic Gateway (eGW) System on Chip (SoC)* como un procesador de redes de alto rendimiento para los futuros controladores GW. La arquitectura propuesta tiene como objetivo cubrir la brecha identificada, avanzando hacia futuras soluciones GW SoC. El concepto *Elastic Gateway SoC* tiene como objetivo sintetizar una arquitectura escalable y preparada para el futuro que abarque todas las funciones y características nuevas y ya establecidas que se exigen en un controlador *gateway* para la nueva era de la movilidad.

El desafío ahora no es solo diseñar el procesador correcto que pueda cumplir con los requisitos disponibles en la actualidad, sino también hacer que este diseño sea adecuado para el futuro. Por ello, la modularidad, flexibilidad, escalabilidad y configurabilidad de estos futuros procesadores cobran, más que nunca, un papel protagonista en las primeras etapas de diseño. Esta tesis también proporciona una metodología de ciclo de vida completa para el diseño y la validación de diferentes productos de procesamiento de red basados en la arquitectura propuesta de eGW SoC.

A lo largo de este trabajo se evalúa la arquitectura desde una perspectiva funcional, demostrando cómo se integran en eGW las diferentes tecnologías requeridas en futuras redes vehiculares y cómo se cumplen los requisitos definidos anteriormente. Después, se implementa una prueba de concepto que muestra la viabilidad del concepto y la metodología propuesta, proporcionando detalles de los resultados experimentales. La arquitectura también se evalúa desde el punto de vista de la escalabilidad, considerando el coste de recursos HW y el consumo de energía, demostrando que eGW puede proporcionar un alto nivel de rendimiento a un coste razonable.

En conjunto, el concepto y la metodología de eGW SoC proponen una alternativa que puede contribuir a superar los desafíos existentes, avanzando sobre el estado del arte.

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Abbreviations

The next list describes several abbreviations that will be later used within the body of the document

ABS Anti-lock Braking System

ACAP Adaptive Compute Acceleration Platform

ACES Autonomy, Connectivity, Electrification and Sharing

ACF AVTP Control Format

ACL Access Control List

ADAS Advanced Driving Assistance Systems

ADC Analog to Digital Converter

AES Advanced Encryption Standard

AI Artificial Intelligence

API Application Programming Interface

AQM Active Queue Management

ARM Advanced RISC Machine

ASIC Application Specific Integrated Circuit

ASIL Automotive Safety Integrity Level

ATS Asynchronous Traffic Shaping

AUTOSAR AUTomotive Open System ARchitecture

AV Audio Video

AVB Audio Video Bridging

AVTP Audio Video Transport Protocol

BIST Built In Self Test

BRAM Block Random Access Memory

BW Bandwidth

C&C Command & Control

CAD Computer Assisted Design

CAM Content Addressable Memory

CAN Controller Area Network

CBS Credit Based Shaper

COPA COnfigurable network Protocol Accelerator

COTS Commercial Off-The-Shelf

CPU Central Processing Unit

CQF Cyclic Queueing and Forwarding

CRC Cyclic Redundancy Check

CRE CAN Routing Engine

CS Checksum

CSRM Cyber Security Real-time Module

DAC Digital to Analog Converter

DAE Distributed Arbitration Engine

DDS Data Distribution Service

DPDK Data Plane Development Kit

DPI Deep Packet Inspection

DPU Data Processing Unit

DRE Data Routing Engine

dRMT disaggregated Reconfigurable Match-Action Tables

DRP Dynamically Reconfigurable Processor

DSP Digital Signal Processor

DuT Device under Test

E/E Electric/Electronic

ECU Electronic Control Unit

EDA Electronic Design Automation

eGW Elastic Gateway

EQE Elastic Queueing Engine

EVITA E-safety Vehicle Intrusion proTected Applications

FIFO First-In First-Out

FMC FPGA Mezzanine Card

FPC Flow Processing Core

FPGA Field Programmable Gate Array

FRER Frames Replication and Elimination for Reliability

FRR Fast Re-Route

FRTI Fault Reaction Time Interval

FSD Full Self Driving

FSM Finite State Machine

FTTI Fault Tolerant Time Interval

FuSa Functional Safety

GCL Gate Control List

gPTP Generic Precision Time Protocol

GPU Graphic Processing Unit

GUI Graphical User Interface

GW Gateway

HDL Hardware Description Language

HPC High Performance Computer

HSM Hardware Security Module

HW Hardware

IC Integrated Circuit

IDS Intrusion Detection System

IEEE Institute of Electrical and Electronics Engineers

IO Input Output

IP Intellectual Property

IPS Intrusion Prevention System

IPV Internal Priority Value

ISA Instruction Set Architecture

ISO International Organization for Standardization

IT Information Technology

IVN In-Vehicle Network

JPEG Joint Photographic Experts Group

JSON JavaScript Object Notation

KPI Key Performance Indicator

LACP Link Aggregation Control Protocol

LAN Local Area Network

LIDAR Laser Imaging Detection and Ranging

LIN Local Interconnect Network

LLCE Low Latency Communication Engine

LUT Look Up Table

M&A Match & Action

MAC Media Access Control

MACSec Media Access Control Security

MCAL Microcontroller Abstraction Layer

MCU Microcontroller Unit

MMAP Memory Map

MOST Media Oriented System Transport

MPSoC Multi Processor System on Chip

MPU Memory Protection Unit

NC Node Controller

NFP Network Flow Processor

NFV Network Function Virtualization

NIC Network Interface Card

NIDS Network Intrusion Detection System

NoC Network on Chip

OEM Original Equipment Manufacturer

OPCODE Operation Code

OS Operating System

OSI Open Systems Interconnection

P4 Programming Protocol-independent Packet Processors

PC Personal Computer

PCAP Packet CAPture

PCIe Peripheral Component Interconnect express

PDF Portable Document Format

PDU Protocol Data Unit

PFE Packet Forwarding Engine

PHY PHYsical layer

PISA Protocol Independent Switch Architecture

PL Programmable Logic

PLL Phase Locked Loop

PNG Portable Network Graphics

PoC Proof of Concept

PP Packet Processor

PPC Packet Processor Core

PS Processing System

PSA Portable Switch Architecture

PSFP Per Stream Filtering and Policing

PTP Precision Time Protocol

QoS Quality of Service

RAM Random Access Memory

RISC Reduced Instruction Set Computer

RMT Reconfigurable Match-Action Tables

RT Routing Table

RTL Register Transfer Level

RTPS Real Time Publish Subscribe

SAE Society of Automotive Engineers

SBC System Basis Chip

SDN Software Defined Networking

SDNC Software Defined Node Controller

SDV Software Defined Vehicle

SoA Service oriented Architecture

SoC System on Chip

SOTA Software Over The Air

SOTIF Safety Of The Intended Functionality

SP Strict Priority

SPC Smart Power Controller

SR Stream Reservation

STE System Time Engine

SW Software

TAS Time Aware Shaper

TC Traffic Class

TCAM Ternary Content Addressable Memory

TCL Tool Command Language

TCP/IP Transmission Control Protocol / Internet Protocol

TCU Telecommunications Control Unit

TM Traffic Manager

TSE Traffic Shaping Engine

TSN Time Sensitive Networking

UML Unified Modelling Language

V2C Vehicle to Cloud

V2V Vehicle to Vehicle

V2X Vehicle to Everything

VCD Value Change Dump

VeGA Vehicular Gateway Architecture

VHDL Very High-speed integrated circuit HDL

VLAN Virtual Local Area Network

VUCA Volatility Uncertainty Complexity and Ambiguity

WCRT Worst Case Response Time

WRED Weighted Random Early Drop

Chapter 1

Introduction

The world as we know it is changing at a fast pace. Devices that are used on a daily basis are shifting from isolated and mono-function to connected, shared, electric, multi-function and even autonomous. This shift applies to everything: from house appliances to your own (or shared!) vehicle. Users demand vehicles to be smarter, user-friendly, energy efficient and environmentally friendly. For this purpose, Original Equipment Manufacturers (OEMs) are changing their concepts faster than ever towards meeting their customers requirements. This change is powered by the evolution on Information Technology (IT) and communications technology that has been going on during the past decades. However, it is now when all these technologies are mature enough and cost-effective to be adopted in automotive.

Computing and processing platforms design and development has traditionally been reserved for a few companies in the world. The associated high development cost and required infrastructure were not easy to access for the vast majority of technology companies. Moreover, general purpose computing and processing platforms used to be sufficient for industry applications, making other technology companies uninterested in developing custom devices. However, in recent years, the need for more specialized and customized computing platforms has emerged and, supported by development platforms like reconfigurable System on Chip (SoC) available for the general public, it has disrupted the computing and processing platforms world. Now, application specific processors are becoming a key differentiation factor across different industries. Starting from traditional digital signal processing (DSP) modules for audio processing, continuing with graphic processing units (GPUs) for image processing applications and moving now towards specific cryptography modules for new security frameworks, the design of custom processors is enabling key innovations across many different verticals [1]. The area of communications and networking is not an exception, and there are more and more application specific solutions there as well [2, 3].

At the same time, the automotive industry has also experienced a great revolution going from a fully mechanical product to a completely different one where mechanics are no longer the core technology and electronics and IT are taking the starring role. In order to succeed in this mission, the whole vehicular architecture needs to be redefined, starting at the lowest level: the intra-vehicular network and its components. With the amount of sensors and actuators that need to be integrated in vehicles

in order to be able to provide the required functionalities (mainly autonomy and connectivity), the exchange of data between the different devices becomes of utmost importance. To process the internal communications, the traditional approach was to use general processing platforms such as microcontroller units (MCUs) running software (SW) implementations. However, the new functionalities bring certain constraints that can not always be met with this traditional approach. For instance, now more bandwidth (BW) and throughput is required to transfer data from/to different sensors and actuators (e.g. cameras), while, more than ever, these data need to be transmitted in a safe and reliable way.

This PhD dissertation focuses on the suitability of application specific processors, or application specific integrated circuits (ASIC) for the automotive networking domain. It aims to devise a new architecture for computing platforms in the area of in-vehicle networking, making use of hardware-software (HW-SW) codesign strategies, in order to design the optimal coprocessor to solve the challenges of future In-Vehicle Networks (IVNs).

For this purpose, first an exhaustive analysis of the background of vehicular networks and the state of the art of the technologies involved in this research is conducted in Chapter 2. Then, the requirements of future network processing platforms are derived in Chapter 3, and an analysis of how well existing architectures can fulfill these requirements is presented. Based on this analysis, the specific objectives of this research project are described in Chapter 4 and a new network processing architecture is proposed to fill the existing gap: elastic Gateway (eGW) System on Chip (SoC). This is a HW-centric network processing architecture specifically designed to meet the identified requirements, which is introduced in Chapter 5. Afterward, an analysis of how the required technologies are integrated in the proposed architecture is presented in Chapter 6. Then, Chapter 7 evaluates the proposed architecture by checking its capability of fulfilling the requirements identified in Chapter 3. Afterward, Chapter 8 presents the proposed design methodology for new network processors based on the presented architecture. Chapter 9 exposes the proof of concept of the architecture and experimental results obtained, followed by a scalability analysis of the architecture in Chapter 10. Finally, this research is concluded in Chapter 11. The publications and intellectual property derived from this work are summarized in Appendix A.

Chapter 2

Background / State of the Art

2.1 Automotive Electronics Industry

The automotive industry has traditionally been one of the most conservative industries regarding the incorporation of new technologies. This used to be linked to the strict regulatory requirements, especially related to safety, that are inherent to this industry and to the fact that the added value of incorporating these new technologies versus the associated risk and investment was not enough to make it through. However, in the last decade this has completely changed. The emergence of a new player (Tesla) coming with a revolutionary concept (electric and autonomous car sooner than expected) has put the automotive industry upside down and has made traditional and prestigious OEMs to change their mindsets and adapt to the new concepts. The journey of the automotive industry in recent years goes from a completely mechanical product, to the one we are describing today, where mechanics are not the core at all. IT technologies, which were once only used in data centers or enterprises, are now being fully integrated into vehicles in order to provide new functionalities, changing radically the user experience. The first steps were to introduce some electronics for automatic control of mirrors, climate regulation, or the inclusion of the infotainment system, moving from a fully mechanical product, to a mechatronics based design. However, today we are assisting to the full electrification of vehicles where the most important technology is no longer mechanics, but the electronics and inclusion of IT technologies.

This revolution is based on the so-called automotive megatrends that are changing the concept of mobility in our societies. The full industry (product, customers, suppliers and business model) are facing challenging changes associated to disruptive new concepts and behaviors that are emerging in the society. Therefore, this revolution is here to stay and adapting to change will be the only way to be part of the future.

In this section, an overview of the main contributors to this VUCA (Volatility Uncertainty Complexity and Ambiguity) context is given. The focus is not only on social megatrends that connect with the automotive industry, but also on the observation of the current key technologies and factors that are enablers and/or motivators of the future adaptation.

..... *Confidential Information* .....

2.2 Semiconductor Industry

The semiconductor industry is also seeing significant changes on their well established design model. While at manufacturing level the race towards smaller technologies which lead to higher integration, lower production costs and higher performance continues to be the norm, the revolution is happening in the design of the ICs itself. Traditionally, big Integrated Circuit (IC) designers like Intel or Nvidia would design the best general purpose compute platforms in the market and companies in different industries would make their designs based on these platforms. Competition and differentiation between companies within a sector like the automotive would be based on the design of functionalities and capabilities reached with one platform that could be the same platform used in a competitors product.

However, now there is an ongoing trend to change this model of operation: big technology companies are starting to develop their own ICs customized to their specific needs in order to generate a competitive advantage over competitors. Tesla [4], Google [5], Amazon [6], Facebook [7] and Apple [8] have already made this decision and are ready to launch their products with their own customized ICs. There is of course a great entry barrier in this approach, but all the big companies that can afford it are shifting towards this paradigm because of the customization opportunity that can increase the performance of their products significantly, and also to prevent competitors from using the same technology that they use. This decision not only provides freedom for developing the hardware accelerators and coprocessors that each of them needs, but also eliminates the dependence on IC designers both in economical aspects and capabilities.

..... Confidential Information .....

2.3 New Technologies integrated in Future IVNs

..... Confidential Information .....

2.4 Network Processing Platforms in the State of the Art

In this section, an analysis of the main architectures available in the state of the art for network processing devices is performed. The main characteristics of each of them are highlighted, focusing on their specific goals, advantages and disadvantages. Additionally, the biggest bottlenecks in each of them that prevent them from being a viable solution for automotive gateway devices are identified.

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2.5 Design and Validation tools for SoC

This section provides an overview of the tools available for the design and validation of new SoC designs in the context of automotive network processors. It starts with generic tools for SoC design including some options for automatic code generation. Then, different steps of the validation phase are

covered, from simulation to real platform testing. Finally, tools specific for the generation of traffic for network processing and tools specific for the automotive use case are discussed. Overall, there are several options in the state of the art targeting the development lifecycle of systems design, with some automation options for SW based products. However, none of the available solutions provides a complete and automatic framework for the design, development, verification and validation of HW-based networking devices.

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2.6 Chapter summary

This chapter provides an in-depth overview of the trends and technologies that affect, in one way or another, the design of future zonal gateway controllers. It starts with an overview of changes affecting the automotive industry: from social changes that demand the integration of new technologies in vehicles to the consequences of this integration in vehicular networks, and the new paradigm of software defined vehicles. Then, trends in the semiconductor industry are also analyzed, providing insights on the benefits of application specific ICs for the automotive industry.

Afterward, the different technologies that can be of use in future vehicular networks are analyzed in detail. This analysis covers a wide range of technologies: software defined networking, time sensitive networking, functional safety, network security, tunneling of frames, data distribution service and the processing of high level applications. For each of them an overview of the technology is given, together with the most recent research or industry advances in the state of the art.

Thereafter, the state of the art architectures for network processing platforms are analyzed in detail. For each of them, the main advantages and disadvantages from architecture point of view are highlighted, identifying their biggest bottlenecks.

Finally, an overview of design and validation tools for SoC devices is given. Tools related to the full lifecycle of a design are covered, going from high level design to code generation and also design validation and verification. Tools specific for automotive are also reviewed.

To finalize this chapter, a taxonomy of the works reviewed is given in the next section.

Overall, this chapter provides the required background to understand the ecosystem of future vehicular network processors, laying the foundations for the research conducted throughout this thesis. The next chapter uses the information gathered in this background analysis to derive the requirements of future vehicular network processors.

2.7 Taxonomy of research works reviewed

This section provides a taxonomy of the research works reviewed, with the goal of facilitating the reader navigating the bibliography. In some cases, one work might be classified under two different categories, when it relates to different topics as organized in this research work.

- **Automotive Electronics Industry**
  - **IVN architecture and evolution**
    - Five trends transforming the Automotive Industry [9]
    - Race 2050 - A vision for the European Automotive Industry [10]
    - System architecture and software design for Electric Vehicles [11]
    - In-Vehicle Networks outlook [12]
    - Future Vehicle Networks and ECU [13]
    - Intra-Vehicle Networks: a Review [14]
    - Next Generation Intra-Vehicle Backbone Network Architectures [15]
    - An Architecture for In-Vehicle Networks [16]
    - E/E Architecture Synthesis: Challenges and Technologies [17]
    - The case for Ethernet in automotive communications [18]
    - In-vehicle network average response time analysis for CAN-FD and automotive Ethernet [19]
  - **Traffic Patterns**
    - Insights on the Performance and Configuration of AVB and TSN in Automotive Ethernet Networks [20]
    - Traffic Categories and Overall Performance Goals [21]
  - **Management of different Network Protocols**
    - Design and development of an extensible multi-protocol automotive gateway [22]
    - Heterogeneous Communication Virtualization [23]
    - In-Vehicle Software Defined Networking: An Enabler for Data Interoperability [24]
    - Configurable Network Protocol Accelerator [25]
  - **Software Defined Vehicle**
    - Service-oriented dynamic connection management for software-defined internet of vehicles [26]
    - A distributed in-vehicle service architecture using dynamically created web Services [27]
    - SODA: Service-Oriented Architecture for Runtime Adaptive Driver Assistance Systems [28]
    - RACE: A centralized platform computer based architecture for automotive applications [29]
    - Achieving determinism in adaptive AUTOSAR [30]
    - Software-Defined Networking in Automotive [31]

Figure 2.1: Taxonomy of Related Work on Automotive Electronics Industry

- **Technologies required in future IVNs**
  - **Time Sensitive Networking**
    - **Introduction and Overview**
      - Introduction to Time-Sensitive Networking [32]
      - Time-Sensitive Networking: An Introduction [33]
      - Timely Survey of Time-Sensitive Networking: Past and Future Directions [34]
      - Ultra-Low Latency (ULL) Networks: The IEEE TSN and IETF DetNet Standards and Related 5G ULL Research [35]
    - **Time Synchronization**
      - Distributing Deterministic, Accurate Time for Tightly Coordinated Network and Software Applications: IEEE 802.1AS, the TSN profile of PTP [36]
      - Time synchronization method of IEEE 802.1AS through automatic optimal sync message period adjustment for in-car network [37]
      - IEEE 802.1AS time synchronization in a switched Ethernet based in-car network [38]
    - **Egress Traffic Management**
      - Latency and Backlog Bounds in Time-Sensitive Networking with Credit Based Shapers and Asynchronous Traffic Shaping [39]
      - Analysis and modeling of asynchronous traffic shaping in time sensitive networks [40]
      - Formal worst-case timing analysis of ethernet tsn's time-aware and peristaltic shapers [41]
      - On the Performance of Stream-based, Class-based Time-aware Shaping and Frame Preemption in TSN [42]
      - Gate-Shrunk Time Aware Shaper: Low-Latency Converged Network for 5G Fronthaul and M2M Services [43]
      - An Approach to Improve Bandwidth Utilization in TSN Networks [44]
      - Time-Triggered Switch-Memory-Switch Architecture for Time-Sensitive Networking Switches [45]
      - SP-PIFO: Approximating Push-In First-Out Behaviors using Strict-Priority Queues [46]
      - Chamaleon: Predictable Latency and high Utilization with Queue-Aware and Adaptive Source Routing [47]
      - Performance assessment of the IEEE802.1Qch in an automotive scenario [48]
      - Assessments of Real-Time Communications over TSN Automotive Networks [49]
      - No-wait packet scheduling for IEEE time-sensitive networks (TSN) [50]
      - Development of an Ethernet-based heuristic time-sensitive networking scheduling algorithm for real-time in-vehicle data transmission [51]
      - Deadline-aware online scheduling of TSN flows for automotive applications [52]
      - Implementation Aspects of Multi-Level Frame Preemption in TSN [53]
      - A novel frame preemption model in TSN networks [54]
      - Quantitative performance comparison of various traffic shapers in time-sensitive networking [55]
      - Comparison of IEEE802.1Q and IEEE802.1AVB in multi switch environment in embedded system [56]
      - Insights on the Performance and Configuration of AVB and TSN in Automotive Ethernet Networks [20]
      - An Architecture for In-Vehicle Networks [16]

Figure 2.2: Taxonomy of Related Work on TSN - I

Technologies required in future IVNs
- **Time Sensitive Networking**
  - **Network Reliability**
    - Application Layer Benefits of Redundant Disjoint Paths in a Real-Time Ethernet [57]
    - Evaluation of QoS Under the Network with SPQ, FRER and FP [58]
    - Redundancy Management for Safety-Critical Applications with Time Sensitive Networking [59]
    - Redundancy path implementation for schedule traffic [60]
    - Fault-Tolerant Dynamic Scheduling and Routing for TSN based In-vehicle Networks [61]
    - Cooperation or competition? Coexistence of safety and security in next-generation Ethernet-based automotive networks [62]
    - Design and Experimental Evaluation of the Proactive Transmission of Replicated Frames Mechanism over Time-Sensitive Networking [63]
    - Challenges and Limitations of IEEE 802.1CB-2017 [64]
    - Enhancing Fault Detection in Time Sensitive Networks using Machine Learning [65]
  - **Configuration**
    - Harmonization of TSN parameter modelling with automotive design flows [66]
    - TSN-Builder: Enabling Rapid Customization of Resource-Efficient Switches for Time-Sensitive Networking [67]
    - Self-configuration of IEEE 802.1 TSN networks [68]
    - UML visualization of YANG models [69]
    - SDN-based configuration solution for IEEE 802.1 Time Sensitive Networking (TSN) [70]
    - Software-Defined Networks Supporting Time-Sensitive In-Vehicular Communication [71]
    - Software-Defined Time Sensitive Networks Configuration and Management [72]
    - Time-sensitive software-defined networking: A unified control- plane for tsn and sdn [73]
  - **Experimentation with TSN**
    - Nesting:Simulating ieee time-sensitive networking (tsn) in omnet++ [74]
    - A time-sensitive networking (tsn) simulation model based on omnet++ [75]
    - Evaluation of time-triggered traffic in time-sensitive networks using the opnet simulation framework [76]
    - Performance Analysis of the IEEE 802.1 Ethernet Audio/Video Bridging Standard [77]
    - n Extension of the OMNeT++ INET Framework for Simulating Real-time Ethernet with High Accuracy [78]
    - Simulating TSN traffic scheduling and shaping for future automotive Ethernet [79]
    - Holistic Modeling of Time Sensitive Networking in Component-Based Vehicular Embedded Systems [80]
    - EnGINE: Developing a Flexible Research Infrastructure for Reliable and Scalable Intra-Vehicular TSN Networks [81]
    - Time-sensitive networking (tsn): An experimental setup [82]

Figure 2.3: Taxonomy of Related Work on TSN - II

Technologies required in future IVNs

- **Security**
  - **Overview**
    - Survey and taxonomy of information-centric vehicular networking security attacks [83]
    - Securing the connected car: A security-enhancement methodology [84]
    - Security of vehicular ad-hoc networks: A comprehensive survey [85]
    - Strategies for integrating control flows in software-defined in-vehicle networks and their impact on network security [86]
    - Secure time-sensitive software-defined networking in vehicles [87]
    - Security of sdn-based vehicular ad hoc networks: State-of-the-art and challenges [88]
    - Layers of Automotive Security [89]
    - Considerations for cyber security implementation in autonomous vehicle systems [90]
  - **V2X**
    - Securing vehicle-to-everything (v2x) communication platforms [91]
    - Reliable and secure v2x communications with wi-fi neighbor aware networking [92]
    - Recognition of outlying driving behaviors: A data-driven perspective with applications to v2x collective perception [93]
  - **Intrusion Detection System**
    - Heavy Hitter Detection on Multi-Pipeline Switches [94]
    - Automotive electrical and electronic architecture security via distributed in-vehicle traffic monitoring [95]
    - Netfpga-based firewall solution for 5g multi-tenant architecture [96]
    - A survey of intrusion detection for in-vehicle networks [97]
    - Intrusion detection game for ubiquitous security in vehicular networks: A signaling game based approach [98]
  - **Data Encryption**
    - A Modular , Reconfigurable and Updateable Embedded Cyber Security Hardware Solution for Automotive [99]
    - Secure vehicular data communication in named data networking [100]
    - Evaluation of a zone encryption scheme for vehicular networks [101]
    - A secure cooperative transmission model in VANET using attribute based encryption [102]
    - Secure data encryption in vanet [103]
    - Conventional and hybrid encryption schemes for security against attacks in vehicular ad-hoc network [104]
    - Security architecture for automotive communication networks with CAN FD [105]
    - Secure key management in vehicular ad-hoc network: A review [106]
    - An efficient authentication scheme for secured service provisioning in edge-enabled vehicular cloud networks towards sustainable smart cities [107]
    - Energy-efficient end-to-end security for software-defined vehic- ular networks [108]
    - FPGA synthesis of an AES encoder circuit for vehicular communication networks [109]
  - **Limitations**
    - Cooperation or competition? Coexistence of safety and security in next-generation Ethernet-based automotive networks [62]
    - 5G QoS: Impact of security functions on latency [110]
    - Cross-layer tradeoff of QoQ and security in vehicular ad hoc networks: A game theoretical approach [111]

Figure 2.4: Taxonomy of Related Work on Security

- **Technologies required in future IVNs**
  - **Software Defined Networking**
    - **Introduction and Overview**
      - OpenFlow: Enabling innovation in campus networks [112]
      - Software-defined networking: A comprehensive survey [113]
      - Software defined networks: A survey [114]
    - **SDN in Automotive**
      - Software-Defined Networking in Automotive [115]
      - Poster: An In-Vehicle Software Defined Network Architecture for Connected and Automated Vehicles [116]
      - In-Vehicle Software Defined Networking: An Enabler for Data Interoperability [24]
      - Retrofitting SDN to classical in-vehicle networks: SDN4CAN [117]
      - An SDN Architecture for Automotive Ethernets [118]
      - Requirements analysis and performance evaluation of SDN controllers for automotive use cases [119]
    - **SDN for embedded systems**
      - Full-stack SDN: The next big challenge? [120]
      - On offloading programmable SDN controller tasks to the embedded microcontroller of stateful SDN dataplanes [121]
      - Shifting the Network-on-Chip Paradigm towards a Software Defined Network Architecture [122]

Figure 2.5: Taxonomy of Related Work on SDN

- **Technologies required in future IVNs**
  - **Functional Safety**
    - **Safety mechanisms embedded in IVNs**
      - Freedom from Memory Interference [123]
      - Safety island in safety critical hardware [124]
      - Asil-decomposition based routing and scheduling in safety-critical time-sensitive networking [125]
      - Network information flow [126]
      - Coupling source routing with time-sensitive networking [127]
      - Failure handling for time-sensitive networks using sdn and source routing [128]
      - On the evaluation of the active queue management mechanisms [129]
      - Achieving flexible, low-latency and 100gbps line-rate load balancing over ethernet on fpga [130]
      - Smartnic-based load management and network health monitoring for time sensitive applications [131]
      - Precise real-time monitoring of time-critical flows [132]
      - Shortcutting Fast Failover Routes in the Data Plane [133]
      - Fast failover in ethernet-based automotive networks [134]
      - A survey of fast-recovery mechanisms in packet-switched networks [135]
    - **State of the Art Functional Safety Deployment**
      - FPGA-based automotive ECU design addresses AUTOSAR and ISO 26262 standards [136]
      - Security aware network controllers for next generation automotive embedded systems [137]
      - A Modular , Reconfigurable and Updateable Embedded Cyber Security Hardware Solution for Automotive [99]

Figure 2.6: Taxonomy of Related Work on Functional Safety

Technologies required in future IVNs
- **Tunneling of Frames**
  - Gateway Framework for In-Vehicle Networks Based on CAN, FlexRay, and Ethernet [138]
  - Mapping can-to-ethernet communication channels within virtualized embedded environments [139]
  - A novel Flexray/Ethernet gateway for in-vehicle networks [140]
  - Efficient data communication automotive gateway system for CAN-Ethernet networks [141]

Figure 2.7: Taxonomy of Related Work on Frames Tunneling

Technologies required in future IVNs
- **Data Distribution Service**
  - **Analysis of DDS middleware**
    - Data Distribution Service (DDS): A performance comparison of OpenSplice and RTI implementations [142]
    - Oops! It's Too LateẎour Autonomous Driving System Needs a Faster Middleware [143]
  - **DDS in Automotive**
    - A middleware journey from microcontrollers to microprocessors [144]
    - Middleware Protocols in the Automobile: Service-Oriented, Data-Centric or RESTful? [145]
    - Data distribution service on top of Ethernet networks [146]
    - Modeling, implementation, and analysis of xrce-dds applications in distributed multiprocessor real-time embedded systems [147]
    - DDS middleware on FlexRay network: Simulink blockset implementation of wheel's subblocks and its adaptation to DDS concept [148]
    - Iceoryx — True zero-copy inter-process-communication [149]
    - Performance evaluation of IoT protocols under a constrained wireless access network [150]
  - **DDS with TSN**
    - Multi-Level Time-Sensitive Networking (TSN) Using the Data Distribution Services (DDS) for Synchronized Three-Phase Measurement Data Transfer [151]
    - Using DDS over TSN to support NATO Generic Vehicle Architecture (NGVA) for Land Systems [152]
    - Enabling QoS for collaborative robotics applications with wireless TSN [153]
    - Driving Interoperability and Performance in Automotive Systems with DDS and TSN [154]

Figure 2.8: Taxonomy of Related Work on DDS

- **Network Processing Platforms**
  - **MCU based architectures**
    - **Autosar SW Architecture**
      - In-car Gateway Architecture for Intra and Inter-vehicular Networks [155]
      - ElectroKnox Makes Software-Defined Vehicles a Reality with the Xilinx Zynq® Platform [156]
      - Ethernovia - Virtualizing Vehicle Communication [157]
    - **Open vSwitch**
      - Open vSwitch [158]
      - Why Open vSwitch [159]
    - **DPDK**
      - Myth-busting DPDK in 2020 [160]
    - **Many/Multi-core Architecture**
      - Multi-Core Gateway Architecture and Scheduling Algorithm for High-Performance Gateway Implementation [161]
      - Kickstarting high-performance energy-efficient manycore architectures with Epiphany [162]
      - WCRT Analysis and Evaluation for Sporadic Message-Processing Tasks in Multicore Automotive Gateways [163]
  - **HW offloading**
    - **Finding acceleration opportunities**
      - Accelerometer: Understanding Acceleration Opportunities for Data Center Overheads at Hyperscale [164]
      - NOVIA: A Framework for Discovering Non-Conventional Inline Accelerators [165]
    - **HW Acceleration in IT Networks**
      - Performance Analysis of Application-Specific Instruction-Set Routers in Networks-on-Chip [166]
      - Azure Accelerated Networking: SmartNICs in the Public Cloud [167]
      - A Reconfigurable Fabric for Accelerating Large-Scale Datacenter Services [168]
      - Xilinx SDNet: A New Way to Specify Network Hardware [169]
      - Configurable Network Protocol Accelerator [25]
    - **HW Acceleration in Automotive**
      - FPGA-based automotive ECU design addresses AUTOSAR and ISO 26262 standards [136]
      - Security aware network controllers for next generation automotive embedded systems [137]
      - A Modular , Reconfigurable and Updateable Embedded Cyber Security Hardware Solution for Automotive [99]
      - VEGa: A high performance vehicular Ethernet gateway on hybrid FPGA [170]
      - A hardware/software co-design approach for Ethernet controllers to support time-triggered traffic in the upcoming IEEE TSN standards [3]
      - Development of a flexible gateway platform for automotive networks [171]
      - Smart Network Interfaces for Advanced Automotive Applications [172]
      - Reconfigurable Computing in Next-Generation Automotive Networks [173]

Figure 2.9: Taxonomy of Related Work on Network Processing Platforms - I

- **Network Processing Platforms**
  - **Programmable Dataplanes**
    - **PISA and P4 - Introduction and Overview**
      - P4: Programming Protocol-Independent Packet Processors [174]
      - A Survey on Data Plane Programming with P4: Fundamentals, Advances, and Applied Research [175]
      - An Exhaustive Survey on P4 Programmable Data Plane Switches: Taxonomy, Applications, Challenges, and Future Trends [176]
      - The programmable data plane: Abstractions, architectures, algorithms, and applications [177]
      - Modeling and Performance Analysis of P4 Programmable Devices [178]
      - One for All, All for One: A Heterogeneous Data Plane for Flexible P4 Processing [179]
      - Toward an Abstract Model of Programmable Data Plane Devices [180]
      - Application Layer Packet Processing Using PISA Switches [181]
      - Reimagining automotive service-oriented communication: A case study on programmable data planes [182]
      - P416 Portable Switch Architecture (PSA) Version 1.1 [183]
    - **Design frameworks for P4 switches**
      - P4 to FPGA-A Fast Approach for Generating Efficient Network Processors [184]
    - **Different PISA related Architectures**
      - Forwarding Metamorphosis: Fast Programmable Match-Action Processing in Hardware for SDN [185]
      - DRMT: Disaggregated Programmable Switching [186]
      - FlowBlaze: Stateful Packet Processing in Hardware [187]
      - Challenging the Stateless Quo of Programmable Switches [188]
      - High Performance Packet Processor Architecture for Network Virtualization: Programmable Packet Processor Architecture as a Data Flow Machine [189]
      - P4GPU: Acceleration of programmable data plane using a CPU-GPU heterogeneous architecture [190]
      - A Folded Pipeline Network Processor Architecture for 100 Gbit/s Networks [191]
    - **Limitations**
      - Hardware-Based Evaluation of Scalable and Resilient Multicast With BIER in P4 [192]
      - Heavy Hitter Detection on Multi-Pipeline Switches [94]
      - Tofino + P4: A Strong Compound for AQM on High-Speed Networks? [193]
      - Event-Driven Packet Processing [194]
      - Automatic performance-optimal offloading of network functions on programmable switches [195]
      - Accelerator-aware in-network load balancing for improved application performance [196]
      - The Actual Cost of Programmable SmartNICs: Diving into the Existing Limits [197]
  - **Full HW-based Network Processing Architecture**
    - VEGa: A high performance vehicular Ethernet gateway on hybrid FPGA [170]

Figure 2.10: Taxonomy of Related Work on Network Processing Platforms - II

- **Design and Validation tools for SoC**
  - **CAD tools**
    - Design assembly framework for FPGA back-end acceleration [198]
    - Yosys+nextpnr: An open source framework from verilog to bitstream for commercial FPGAs [199]
    - Real Silicon Using Open-Source EDA [200]
  - **Automatic Code Generation**
    - TSN-Builder: Enabling rapid customization of resource-efficient switches for time-sensitive networking [67]
    - P4 to FPGA-A Fast Approach for Generating Efficient Network Processors [184]
    - Generating VHDL Source Code from UML Models of Embedded System [201]
    - Automation of Domain-specific FPGA-IP Generation and Test [202]
    - DNNBuilder: an Automated Tool for Building High-Performance DNN Hardware Accelerators for FPGAs [203]
  - **Simulation Frameworks**
    - The gem5 simulator [204]
    - Gem5 + RTL: A framework to enable RTL models inside a full-system simulator [205]
    - GTK Wave [206]
  - **Automatic Testing**
    - Time-sensitive networking (tsn): An experimental setup [82]
    - Towards an ecosystem for reproducible research in computer networking [207]
    - Implementation of an integrated FPGA based automatic test equipment and test generation for digital circuit [208]
    - SAT-ATPG for application-oriented fpga testing [209]
    - Poster: Performance evaluation of an open-source audio-video bridging/time-sensitive networking testbed for automotive ethernet [210]
    - Ducked tails: Trimming the tail latency of(f) packet processing systems [211]
    - The pos framework: A methodology and toolchain for reproducible network experiments [212]
  - **Product lifecycle development frameworks**
    - Xandar: X-by-construction design framework for engineering autonomous & distributed real-time embedded software systems [213]
    - Xandar: Exploiting the x-by-construction paradigm in model-based development of safety-critical systems [214]
  - **Traffic Generation and Monitoring**
    - Precise real-time monitoring of time-critical flows [132]
    - Moongen: A scriptable high-speed packet generator [215]
    - Efficient dynamic flow tracking for packet analyzers [216]
    - High-performance packet processing and measurements [217]
    - FloWatcher-DPDK: Lightweight line-rate flow-level monitoring in software [218]
    - Fluent10g: A programmable FPGA-based network tester for multi-10-gigabit etherne [219]
  - **Automotive Specific Tools**
    - EnGINE: Developing a Flexible Research Infrastructure for Reliable and Scalable Intra-Vehicular TSN Networks [81]
    - Challenges with automotive test case specifications [220]
    - Testing methods used in the automotive industry: Results from a survey [221]
    - Design of vehicle gateway automatic test system based on canoe [222]
    - The case for Ethernet in automotive communications [18]
    - Methodology and Infrastructure for TSN-Based Reproducible Network Experiments [223]

Figure 2.11: Taxonomy of Related Work on Design and Validation tools for SoC

Chapter 3

Requirements of future Network Processing Platforms

The overall mission of this research is to accelerate the design and evaluation of new high performance network processing SoC devices for automotive, in order to enable the integration of technology changes that are happening at a fast pace. For this, the first step is to thoroughly study and define the requirements that are now applicable to network processing platforms derived from the integration of new technologies and functionalities within IVNs. Then, the currently available network processing platforms need to be evaluated in terms of their fulfillment of the identified requirements. These requirements are classified into functional requirements and structural requirements.

- **Functional requirements** relate to a functionality that must be provided by the GW platform as part of the network infrastructure in a vehicle.
- **Structural requirements** relate to design practices and the viability of the architecture design towards a real Network/System on Chip (NoC/SoC) that may evolve into a commercial product.

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Chapter 4

Research Goals

After the previous analysis, an interesting research opportunity is identified, that emerges from the revolution that is currently undergoing both in automotive and semiconductor industry. This thesis aims at contributing to the evolution of the current landscape, where there is a gap pointing to a lack of high performance solutions for automotive network processing. Additionally, HW-centric architectures are identified as an enabler for these future solutions. With this in mind, the following goals (G) are defined:

- **G1. Design and evaluation of new network processing architecture**: By reflecting on the existing limitations in the solutions available in the state of the art, the main goal is to define a new architecture for automotive network processors that is capable of fulfilling all the identified requirements with the right level of performance. The architecture must be future-proof, i.e. it must provide a modular approach for the integration of current and future required functionalities (both in SW and HW). This architecture shall be evaluated from a theoretical point of view, as well as through a real proof of concept. Another goal of the architecture is to reduce the complexity of designing and programming network processing devices, through the support of HW accelerators.
- **G2. Definition of a design and evaluation methodology with a focus on scalability and automation**: An important aspect towards the acceleration of the design lifecycle is to provide the right methodology and design flow to support the GW designer. The complete flow from requirements definition to implementation and to system validation shall be covered by the defined methodology. This methodology must be scalable and allow for automating the complete design and validation process, by providing a SW-like interface for the design of HW-centric network processors.

The accomplishment of these goals is described throughout the following Chapters. Starting with the first goal (G1), Chapter 5 describes the design of a proposal for a new network processing architecture targeting vehicular networks. Then, Chapter 6 evaluates the integration of the different technologies required in vehicular networks within the proposed architecture. The functional validation

of the architecture is concluded in Chapter 7, showing how it is capable of fulfilling the requirements identified in Chapter 3.

Continuing with the second goal (G2), Chapter 8 describes the proposed automation methodology for the design and validation of network processors conforming to the architecture proposed in G1.

Afterward, both goals are completed with a proof of concept of the proposed system architecture and method. This proof of concept together with the experimental results is described in Chapter 9. Finally, the scalability of the architecture and methodology is evaluated in Chapter 10.

Chapter 5

Elastic Gateway (eGW) SoC Architecture

This section presents a new network processing architecture specifically designed to meet the requirements of future IVNs: elastic Gateway (eGW). The architecture provides a fully HW-centric datapath based on a set of IP cores that compose a library for gateway SoC design. Next, the architecture is introduced, highlighting its main innovative features and showing how it fulfills the requirements listed in Chapter 3. First, the high level architecture design is detailed and second, each of the blocks that compose the architecture are described in detail.

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Chapter 6

Technologies Integration in eGW and Benchmark with State of the Art

This chapter covers the integration of the most relevant technologies related to networking and network processors within the eGW SoC architecture. Some of them are related to the state of the art of network processor architectures while others are functionalities that need to be integrated in a GW design. For each of them, it provides an overview of the state of the art, and how eGW is able to integrate the main concepts of each technology advancing over the state of the art. Fig. **??** provides an example of a design based on eGW where the different use cases discussed in this section are implemented. The different sections explain all the functionalities deployed in this figure, which can easily coexist in an eGW-based design. A summary of this technologies is given in Table 6.1.

Each section also provides a comparison between available alternatives in the state of the art, looking at the key aspects of each technology in the form of a spider graph. Elastic GW is included in this comparison, helping to understand the design choices of the architecture, how each of them supports the fulfillment of the previously derived requirements and how eGW correlates with the state-of-the-art of each of these technologies.

At the end of this chapter a different perspective is provided, comparing the different architectures available in state of the art and eGW in terms of structural requirements and architecture design. The aim of this is to provide a good understanding of the trade offs that exist when designing the vehicular networking platforms of the future, supporting system designers in making design choices. ..... *Confidential Information* .....

Table 6.1: Technologies integrated in eGW

Technologies integrated in eGW
Software Defined Networking (SDN)
Programmable Dataplanes
Time Sensitive Networking (TSN)
Safety and Security
Frames tunneling (IEEE1722)
Data Distribution Services (DDS)
Application layer processing

Chapter 7

Functional Validation

As seen before, one of the challenges that arises when designing new network processors for automotive is the management of heterogeneous technologies at different system levels. The complexity is not in giving the best performance on one particular aspect, but in supporting a wide range of applications which require the integration of different technologies while keeping performance under control for each of them. Fig. **??** exposes a summary of the coverage of the different required functionalities for IVN provided by the different network processing architectures introduced above, including eGW. This shows that the strength of eGW is its capability of integrating such a wide range of functionalities and technologies while being competitive in each area, i.e., even though sometimes custom solutions perform better in a specific area, eGW is capable of providing a solution that is good enough in each of them, becoming the only one that can cover them all. This characteristic also makes eGW a future-proof solution, capable of integrating new requirements and functionalities in a flexible and scalable way, helping thus to solve the challenge of technologies integration in future network processors.

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Chapter 8

Design Methodology

This section describes the methodology proposed for the design of vehicular network processors based on the eGW SoC architecture, which addresses all the limitations identified in the methods available in the state of the art. The aim of the proposed methodology is to provide an easy to use SW-based approach for the design of HW-centric network processors for automotive. It follows the V-model, which is the most used design methodology in the automotive industry. Additionally, it integrates the concept of agile design loops within the V-model, allowing for iterating the design in a natural way.

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Chapter 9

Proof of Concept and Experimental Results

9.1 Definition of Scenarios and Experiments

This section describes the experiments that were run on a HW platform with the aim of evaluating eGW SoC. The configuration is based on the zonal architecture. In this architecture there are 4 zonal gateways distributed in the vehicle which are handling the connections to the sensors and actuators that are physically located close to the zonal GW. The zonal GWs are interconnected between them with an Ethernet backbone, while the connection to the different sensors/actuators can use also Ethernet or different network protocols. In the center, there is a High Performance Computer in charge of running applications and distributing functions across the network. This HPC also has a direct connection to each zonal GW via a dedicated Ethernet link. Several scenarios are defined, focusing on the traffic flowing through each zonal gateway. Each scenario represents a particular situation of the IVN with a predefined set of sensors and actuators present in the network. For each scenario there is a specific set of functionalities running on the network that influence the traffic that is exchanged between zonal gateways and the HPC. In the different scenarios, a set of experiments are run, permitting to show how eGW performs under different configurations. The experiments also allow for showcasing configuration and design customization aspects of the architecture. To finalize this section, the configuration used in the HW for the different experiments is described.

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9.2 Experimental Framework and Infrastructure

This section describes the framework used for the experimentation, which follows the structure of the validation framework previously described. First, the setup at network level together with the components used to emulate the vehicular network are presented. Afterward, the specific design used to deploy an eGW-based zonal GW that permits to perform the experiments introduced above is described in detail.

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9.3 Experimental Results

This section presents the results obtained for each experiment. Through the different iterations, the impact of the different configuration parameters on the system behavior is shown, as well as the capabilities of the design. This is of course a selection of the most relevant and representative results obtained through several trial and error iterations. The results chosen are the ones considered most useful for the reader in order to understand the behavior of the system, showing the high level of flexibility and elasticity of the eGW SoC approach in spite of being a HW solution, as well as to understand the design choices aiming at fulfilling the previously defined traffic requirements.

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9.4 Chapter summary

This chapter described the proof of concept developed to validate eGW architecture and the proposed methodology. First, the scenarios where experiments were run are presented, and all the experiments performed are described. The main idea is to perform experiments in two scenarios to see the behavior of eGW under different circumstances. Additionally, the transition between these two scenarios is also evaluated, proving how eGW is able to detect events and react to it. The experiments focus on the integration of different technologies within eGW, covering TSN, functional safety, security, frames tunneling and application processing.

Second, the experimental framework and the infrastructure used for the experiments is presented. The deployment of eGW is performed using the design framework, showing the viability and usability of the design methodology.

Finally, the experimental results are described in detail, showing that eGW is able to perform the required tasks while keeping performance under control. With this, Goal 1 in Chapter 4 is successfully fulfilled.

In the next chapter, the scalability of the architecture is analysed, completing the evaluation of eGW architecture and this proof of concept.

Chapter 10

Scalability Analysis

This section looks at the HW resources and power consumption required by eGW under different configurations in order to evaluate the scalability of the solution. Different design geometries are implemented in an FPGA in order to measure how they increase when scaling the design. The platform used for this evaluation is the same one used for the experiments described in the previous chapter, ProFPGA Zynq Ultrascale+ ZU19EG [224]. In particular, this section looks at the impact of adding more Input Output (IO) ports and/or more processing units. With this, the impact of different architectural choices is analyzed.

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Chapter 11

Conclusions and Future Work

This PhD dissertation provides an in depth analysis of state of the art and future challenges of automotive network processing devices. It starts by analyzing the trends within the automotive industry, the changes in the vehicular E/E architecture (from function-based to domain-based to zonal-based) and how they affect the IVN. In parallel, the evolution of the semiconductor industry is also analyzed, focusing on the current trend towards application specific computing platforms. In the sweet spot between these two industrial changes, an opportunity is identified: the use of application specific platforms for automotive network processing and, in particular, for the design of the future zonal gateway controllers. Then, the technologies that need to be integrated in future vehicular networks are analyzed, even if they have not been used in automotive industry yet. Afterward, the main state of the art architectures for network processing is reviewed, looking at their internal architecture details. To complete the state of the art, a high level overview of the available tools for the design and validation of SoC devices is also provided. The different tools used during the design and validation process of a new IC product are discussed. Specific tools for automotive or tools that facilitate the automation of the design and validation process are of particular interest within this research work.

Considering all the information gathered from the state of the art analysis, it is possible to derive the set of requirements that need to be fulfilled by future IVN processing platforms. Afterward, a review of how each of the existing network processing architectures complies (or not) with the previously inferred requirements is performed, highlighting the main bottlenecks of each of them. This analysis shows that none of the available architectures in the state of the art is capable of providing this particular set of requirements. It also shows the importance of balancing functional and structural requirements, and suggests that the solution relies on the introduction of specific HW accelerators that support the specific functions required in IVNs.

Within this landscape, this thesis focuses on the definition of a new HW-centric network processor for the automotive industry that can fulfill the requirements of future IVNs. Additionally, it aims at providing a complete methodology for the design and validation of network processors based on the proposed architecture, with the goal of improving and accelerating the design lifecycle. Next, the main contributions of this research work are summarized.

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Appendix A

Dissemination of results

In this Appendix, a compilation of results dissemination and intellectual property generated is presented. This collection of works summarizes the content of this dissertation and helps to spread the insights gained with the research community. Some works are thought of as educational resources that can speed up the learning curve of researchers starting with this topic, while others are focused on presenting the new ideas and insights gained throughout the PhD journey. At the end of the Appendix, a summary of research and dissemination activities carried out within the industrial team where the PhD candidate took part during the thesis is provided.

A.1 Publications

- **State of the art analysis**
  - *A. G. Mariño, F. Fons and J. M. M. Arostegui, "The Future Roadmap of In-Vehicle Network Processing: A HW-Centric (R-)evolution," in IEEE Access, vol. 10, pp. 69223-69249, 2022, doi: 10.1109/ACCESS.2022.3186708.*

    This article covers the state of the art of future network processing platforms exposed in Chapter 2.4 and the analysis of requirements of future network processors performed in Chapter 3.

- **Architecture and IP cores design and PoC**
  - *A. G. Mariño, F. Fons and J. M. M. Arostegui, Elastic Gateway SoC Design: a HW-centric Architecture for inline In-Vehicle Network Processing, 2023, submitted to Vehicular Communications Journal*

    This article describes the architecture of eGW presented in Chapter 5 and the integration of technologies described in Chapter 6.
  - *Angela Gonzalez Mariño, Francesc Fons, Juan Manuel Moreno Arostegui, Elastic gateway SoC proof of concept: Experiments design and performance evaluation, Vehicular Communications, 2023, 100636, ISSN 2214-2096, https://doi.org/10.1016/j.vehcom.2023.100636.*

This article focuses on the Proof of Concept of eGW architecture described in Chapter 9.

– *A. G. Mariño, F. Fons and J. M. M. Arostegui, Vehicular Network Processor Design for Scalability & Automation: Elastic Gateway SoC Concept & Builder, 2023, submitted to Journal of Systems Architecture*

  This article describes the complete design methodology presented in Chapter 8 including the library of IP cores and SW interface of eGW, and the scalability analysis of the architecture described in Chapter 10.

– *A. G. Mariño, F. Fons, A. Gharba, L. Ming and J. M. Moreno Arostegui, "Elastic Queueing Engine for Time Sensitive Networking," 2021 IEEE 93rd Vehicular Technology Conference (VTC2021-Spring), Helsinki, Finland, 2021, pp. 1-7, doi: 10.1109/VTC2021-Spring51267.2021.9448758.*

  This article describes the internal architecture of the queuing block described in Chapter **??** together with some queuing optimization strategies.

– *Angela Gonzalez Mariño, Francesc Fons, Li Ming, and Juan Manuel Moreno Arostegui. 2021. PDU Normalizer Engine for Heterogeneous In-Vehicle Networks in Automotive Gateways. In Applied Reconfigurable Computing. Architectures, Tools, and Applications: 17th International Symposium, ARC 2021, Virtual Event, June 29–30, 2021, Proceedings. Springer-Verlag, Berlin, Heidelberg, 140–155.* `https://doi.org/10.1007/978-3-030-79025-7_10`

  This article describes the internal architecture of the normalizer block described in Chapter **??** and the SDN normalization strategy.

– *A. G. Marino, F. Fons, Z. Haigang and J. M. M. Arostegui, "Traffic Shaping Engine for Time Sensitive Networking Integration within In-Vehicle Networks," 2021 IEEE Vehicular Networking Conference (VNC), Ulm, Germany, 2021, pp. 182-189, doi: 10.1109/VNC52810.2021.9644668.*

  This article describes the internal architecture of the Traffic Shaping Engine described in Chapter **??**, with some examples of how different TSN technologies can be integrated in eGW.

– *A. G. Mariño, F. Fons, Z. Haigang and J. M. M. Arostegui, "Loopback Strategy for TSN-compliant Traffic Queueing and Shaping in Automotive Gateways," 2021 IEEE Conference on Network Function Virtualization and Software Defined Networks (NFV-SDN), Heraklion, Greece, 2021, pp. 47-53, doi: 10.1109/NFV-SDN53031.2021.9665092.*

  This article describes the loopback path strategy for TSN technologies described in Chapter **??** together with some use cases that help to illustrate the concept.

– *Angela Gonzalez Mariño, Francesc Fons, Zhang Haigang, and Juan Manuel Moreno Arostegui. 2021. Loopback strategy for in-vehicle network processing in automotive gateway network on chip. In Proceedings of the 14th International Workshop on Network on Chip Architectures (NoCArc '21). Association for Computing Machinery, New York, NY, USA, 22–28.* `https://doi.org/10.1145/3477231.3490429`

This article describes the loopback path strategy for frames processing described in Chapter **??** together with some example use cases.

- **Integration of technologies in eGW architecture**

  – *Angela Gonzalez Mariño, Abdoul Aziz Kane, Francesc Fons, and Juan Manuel Moreno Arostegui. 2022. Enhancements for Hardware-based IEEE802.1CB embedded in Automotive Gateway System-on-Chip. In Proceedings of the Symposium on Architectures for Networking and Communications Systems (ANCS '21). Association for Computing Machinery, New York, NY, USA, 31–37.* `https://doi.org/10.1145/3493425.3502754`

  This article proposes some enhancements to the FRER functionality described in IEEE802.1CB and describes the deployment of this strategy in eGW, as explained in **??**.

  – *A. A. Kane, A. G. Mariño, F. Fons, S. Nueesch, P. Serwa and M. Schoetz, "Elastic Gateway Functional Safety Architecture and Deployment: A Case Study," in IEEE Access, vol. 10, pp. 91771-91801, 2022, doi: 10.1109/ACCESS.2022.3199356.*

  This article describes a new methodology for the deployment of safety concepts in modern vehicular networks, and uses eGW to illustrate this concept. Part of the article relates to the content of Chapter **??** where the deployment of safety mechanisms in eGW is exposed.

  – *C. Scordino, A. G. Mariño and F. Fons, "Hardware Acceleration of Data Distribution Service (DDS) for Automotive Communication and Computing," in IEEE Access, vol. 10, pp. 109626-109651, 2022, doi: 10.1109/ACCESS.2022.3213664.*

  This article describes the idea of deploying part of the DDS middleware in HW accelerators. It uses eGW architecture as an example of the deployment. This corresponds to Chapter **??**. It also explores the integration of DDS and TSN supported by eGW described in Chapter **??**.

- **Design automation and validation framework**

  – *A. G. Marino, N. N. Halinge, F. Fons and J. M. M. Arostegui, "Build Automation Framework for Architecture Design of Automotive Elastic Gateway", Embedded World Conference 2022*

  This article describes the automation design methodology described in Chapter 8.

  – *A. G. Marino, N. N. Halinge, F. Fons and J. M. M. Arostegui, "Build Automation Framework for Design Validation of Automotive Gateway Controllers," 2022 IFIP Networking Conference (IFIP Networking), Catania, Italy, 2022, pp. 1-6, doi: 10.23919/IFIPNetworking55013.2022.9829801.*

  This article focuses on the validation and verification part of the design methodology described in Chapter **??**.

A list with all the articles is available in ORCID: `https://orcid.org/0000-0003-2123-7915`

A.2 Patents

- *Flexible & Scalable Coarse-Grained Communication Gateway Architecture. System and Method for building a Network Gateway based on Modular & Configurable Hardware Functional Blocks. Authors: Francesc Fons, Angela Gonzalez, Li Ming. 2020*

  This patent describes the proposed architecture described in Chapter 5 as well as the building automation process described in Chapter 8 which are the core concepts that have been developed and validated within this PhD thesis.

- *Queues release and optimization in IEEE 802.1Qbv using Run-Time Adaptive and Dynamic IPV. Authors: Ahmed Gharba, Francesc Fons, Angela Gonzalez, Li Ming. 2020*

  This patent describes a novel and smart queue management system for TSN networks where 802.1Qbv is combined with dynamic IPV. Although this specific processing is not the core of this PhD thesis, the implementation and proof of concept of this patent proposal has been done with the architecture proposed in this project and is included as a feature in the queuing block described in Chapter **??**.

- *Queues release and optimization in IEEE 802.1Qbv using Run-Time Adaptive and Dynamic GCL. Authors: Ahmed Gharba, Francesc Fons, Angela Gonzalez, Li Ming. 2020*

  This patent describes a novel and smart queue management system for TSN networks where 802.1Qbv is combined with dynamic gate control list. Although this specific processing is not the core of this PhD thesis, the implementation and proof of concept of this patent proposal has been done with the architecture proposed in this project and is included as a feature in the queuing block described in Chapter **??**.

- *Smart Queueing Engine for TSN-Compliant Networking Devices. Angela Gonzalez, Francesc Fons. 2021*

  This patent describes the internal architecture of the queueing block presented in Chapter **??**, together with the smart control algorithms for the management of the read and write interface. The concept has been prototyped and validated within the context of this PhD thesis.

- *PDU Normalizer for Heterogeneous Networks in Automotive Gateways. Francesc Fons, Angela Gonzalez. 2021*

  This patent describes the architecture of the normalization block together with the SDN approach for the normalization of frames described in Chapter **??**. The concept has been prototyped and validated within the context of this PhD thesis.

A.3 Other related works

A.3.1 Supervision of Master Thesis

- ”Design and Implementation of Build Automation Tool for HDL Architecture of Gateway Controllers” Nikhil Naganath-Halinge. Darmstadt University of Applied Sciences, Department of Electrical Engineering and Information Technology, Germany, Master of Science in Electrical Engineering and Information Technology, Industrial Supervisors: Ms.-Ing. Angela Gonzalez-Marino, Dr.-Ing. F.Fons, Academic Supervisors: Prof. Dr.-Ing. Christian Jakob, Prof. Dr.-Ing. Markus Haid, Completion Date: February 07, 2022

A.3.2 Participation in research lab cooperation between Technical University of Munich (TUM) and Huawei Munich Research Center

- M.Bosk, F.Rezabek, K.Holzinger, A.Gonzalez-Mariño, A.A. Kane, F.Fons, J.Ott, G.Carle, Methodology and Infrastructure for TSN based Reproducible Network Experiments, IEEE Access, vol. 10, pp. 109203 – 109239, October 2022. https://ieeexplore.ieee.org/document/9910175

- F.Rezabek, M.Bosk, T.Paul, K. Holzinger,S.Gallenmüller, A.Gonzalez, A.Kane, F.Fons, Z.Haigang, G.Carle, J.Ott, EnGINE: Flexible Research Infrastructure for Reliable and Scalable Time Sensitive Networks, Journal of Network and Systems Management, vol. 30, no. 74, Springer, September 2022. https://link.springer.com/article/10.1007/s10922-022-09686-0

- K.Holzinger, F.Biersack, H.Stubbe, A.Gonzalez-Mariño, A.Kane, F.Fons, Z.Haigang, T.Wild, A.Herkersdorf, G.Carle, SmartNIC-based Load Management and Network Health Monitoring for Time Sensitive Applications, IEEE/IFIP Network Operations and Management Symposium (NOMS 2022), Workshop on Intelligent Transportation and Autonomous Vehicles Technologies (ITAVT 2022).

- K.Holzinger, H.Stubbe, F.Biersack, A.Gonzalez-Mariño, A.Kane, F.Fons, Z.Haigang, T.Wild, A.Herkersdorf, G.Carle, Poster: Precise Real-Time Monitoring of Time-Critical Flows, ACM International Conference on emerging Networking EXperiments and Technologies (CoNEXT 2021).

- M.Bosk, F.Rezabek, K.Holzinger, A.Gonzalez-Mariño, A.A.Kane, F.Fons, Z.Haigang, G.Carle, J.Ott, Demo: Environment for Generic In-vehicular Network Experiments – EnGINE, IEEE Vehicular Networking Conference 2021 (VNC 2021).

- F.Rezabek, M.Bosk, T.Paul, K.Holzinger, S.Gallenmüller, A.Gonzalez-Mariño, A.A.Kane, F.Fons, Z.Haigang, G.Carle, J.Ott, EnGINE: Developing a Flexible Research Infrastructure for Reliable and Scalable Intra-Vehicular TSN Networks, International Conference on Network and Service Management (CNSM 2021), Workshop on High-Precision, Predictable, and Low-Latency Networking (HiPNet 2021).

A.4 Talks and conference presentations

- F.Fons, A.A.Kane, A.Gonzalez-Mariño, Reliable in-vehicle networks through inline processing of safety mechanisms embedded in networking SoCs, exida Automotive Symposium 2022, Spitzingsee, Germany, October 2022.

  LinkedIn post: https://www.linkedin.com/posts/francesc-fons_exidaautomotivesymposium2022excerptffons-activity-6990228534845702144-tgzd/

- F.Fons, A.Gonzalez-Mariño, A.A.Kane, The paradigm shift in automotive zonal gatewaying, TUM Academic Salon 2022, Garching, Germany, September 2022.

  Video: https://www.net.in.tum.de/talks/workshops/academic_salon_22.html

- F.Fons, A.Gonzalez-Mariño, A.A.Kane, Elastic Network SoC Architecture driven by Parameterizable Hardware Accelerators, HiPEAC CSW Spring 2022, Tampere, Finland, April 2022.

  Video: https://www.youtube.com/watch?v=16tNs0Fwgzo

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