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Dc-dc converters for HVDC heterogeneous interconnections

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Doctoral Thesis

Dc-dc Converters for HVDC Heterogeneous Interconnections

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Echando a perder se aprende.

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Abstract

High voltage direct current (HVDC) technologies have been used for bulk power transmission over long distances since the 1950s. These technologies have proven to be the most cost-efficient, compared to the high voltage alternate current (HVAC), for applications considering long distances such as offshore power transmission, connecting remote loads or generation, and the interconnection of non-synchronized grids.

In recent years, the study of HVDC grids has been of interest in some research projects but, its development is still uncertain. The dc grid can be planned beforehand or it can use the installed lines. But, from the installed HVDC projects, it can be identified different operating voltages, used technologies, and line topologies. There are two HVDC technologies: the line commutated converter (LCC), and the voltage source converter (VSC). Four different line topologies are identified: asymmetric monopole, symmetric monopole, bipole, and rigid bipole. Developing a dc grid interconnecting isolated lines with different characteristics cannot be possible without an intermediary device: the dc-dc converter.

This thesis studies the dc-dc converters interconnecting HVDC lines with different characteristics. These converters can be seen as the equivalent of ac transformers in dc applications because they are capable to adapt the voltage difference between two dc systems. These converters are also capable to adapt the line topology and different technologies. The power electronics required for these dc-dc converters provide increased control flexibility used to supply additional ancillary services that the classical transformers cannot furnish.

Three dc-dc converter topologies are modeled and simulated for the interconnection between a bipole and a symmetric monopole. The front-to-front modular multi-level converter (F2F-MMC) is chosen as the reference because it represents state-of-the-art technology. The second converter is the dc-dc MMC (dc-MMC) because of the topological similarity to the MMC. Then, a third converter is proposed and studied as a result of this thesis, the asymmetric dc-dc converter (ADCC). A set of simulations are performed for multiple operating points and faults scenarios. Then, the converters are compared quantitatively and qualitatively. The results and analysis are used to conclude and bring some perspectives for future works.

Resumen

Las transmisión en corriente continua a alta tensión (HVDC-por sus siglas en inglés) se han utilizado para la transmisión de grandes cantidades de energía a largas distancias desde la década de 1950. Estas tecnologías han demostrado ser las más rentables en comparación con la corriente alterna de alta tensión (HVAC) para algunas aplicaciones como la transmisión de energía en alta mar, la conexión de cargas o generación remotas y la interconexión de redes no sincronizadas.

En los últimos años, el estudio de las redes HVDC ha sido de interés en algunos proyectos de investigación, pero su desarrollo aún es incierto. La red de dc se puede planificar de antemano o puede utilizar las líneas instaladas. Pero, a partir de los proyectos HVDC instalados, se pueden identificar diferentes voltajes de operación, tecnologías utilizadas y topologías de línea. Hay dos tecnologías HVDC: el convertidor de línea conmutada (LCC) y el convertidor de fuente de voltaje (VSC). Se identifican cuatro topologías de línea diferentes: monopolo asimétrico, monopolo simétrico, bipolo y bipolo rígido. El desarrollo de una red de dc que interconecte líneas aisladas de diferentes características no es posible sin un dispositivo intermediario: el convertidor dc-dc.

Esta tesis estudia los convertidores dc-dc interconectando líneas HVDC de diferentes características. Estos convertidores pueden verse como el equivalente de los transformadores de ac en aplicaciones de dc porque son capaces de adaptar la diferencia de tensión entre dos sistemas de dc. Pero, estos convertidores también son capaces de adaptar la topología de línea y diferentes tecnologías. La electrónica de potencia necesaria para estos convertidores dc-dc proporciona una mayor flexibilidad de control que se utiliza para proporcionar servicios auxiliares adicionales que los transformadores clásicos no pueden proporcionar.

Se modelan y simulan tres topologías de convertidores dc-dc para la interconexión entre un bipolo y un monopolo simétrico. El convertidor multinivel modular de frente a frente (F2F-MMC) se elige como referencia porque representa tecnología de punta. El segundo convertidor es el MMC dc-dc (dc-MMC) debido a la similitud topológica con el MMC. Luego, se propone y estudia un tercer convertidor como resultado de esta tesis, el convertidor asimétrico dc-dc (ADCC). Se realiza un conjunto de simulaciones para múltiples puntos de operación y escenarios de fallas.

Luego, los convertidores se comparan cuantitativa y cualitativamente. Los resultados y el análisis se utilizan para concluir y aportar algunas perspectivas para trabajos futuros.

Contents

Nomenclature

AAC	Alternate Arm Converter
AAM	Average Arm Model
AC	Alternating Current
ACCB	AC Circuit Breaker
AFCB	Active Forced Commutated Bridge
AM	Asymmetric Monopole
AT	Auto-transformer
B	Bipole
BCA	Balancing Capacitor Algorithm
CIGRÉ	Conseil International des Grands Réseaux Électriques
CSC	Current Source Converter
DAB	Dual Active Bridge
DBSRC	Dual Bridge Series Resonant Converter
DC	Direct Current
DCCB	DC Circuit Breaker
F2F	Front-to-Front
FBC	Fault Blocking Capability
FBSM	Full Bridge Sub-module
FRT	Fault Ride-Through
HBSM	Half-Bridge Sub-module
HV	High Voltage
HVDC	High Voltage Direct Current
HVAC	High Voltage Alternating Current
IGBT	Insulated-Gate Bipolar Transistor
LCC	Line-Commutated Converter
LV	Low Voltage
MMC	Modular Multilevel Converter
OHL	Over Head Line
PFD	Power Flow Direction
PI	Proportional-Integral controller
PIR	Proportional-Integral-Resonant controller
PLL	Phase Locked Loop

PWM	Pulse Width Modulation
RB	Rigid Bipole
RMS	Root Mean Square
SBC	Series Bridge Converter
SCR	Short Circuit Ratio
SM	Sub-module
SyM	Symmetric Monopole
TSO	Transmission System Operator
ULM	Universal Line Model
UPC	Universitat Politècnica de Catalunya
VSC	Voltage Source Converter

Chapter 1

Introduction

This chapter is based in the following publication:

C1 D. Gómez A., J. D. Páez, M. Cheah-Mane, J. Maneiro, P. Dworakowski, O. Gomis-Bellmunt, F. Morel, "Requirements for interconnection of HVDC links with DC-DC converters", *IECON 2019 - 45th Annual Conference of the IEEE Industrial Electronics Society*, Lisbon, Portugal, 2019, pp. 4854-4860, doi: 10.1109/IECON.2019.8927640.

1.1 General context

Renewable sources of energy have taken an important place in the energy markets in the last few years as they are one of the strategies to reduce carbon emissions while supplying the increasing energy demand.

The European Commission has estimated an offshore wind capacity increase, from 12 GW to 300 GW, by 2050 [1]. This increased capacity will be distributed across all of the EU sea basins, one of the main locations is the North Sea.

There is an increasing number of wind power plants and cross-country interconnections in the North Sea. Figure 1.1 shows the numerous, present and future, high voltage direct current (HVDC) projects in the region. These projects require the use of submarine cables over long distances carrying high power. Most of the projects in this region use HVDC transmission lines as they reduce the total cost compared to the high voltage alternating current (HVAC) lines. HVDC lines are exempt of reactive power consumption avoiding also the losses associated to the frequency, e.g. skin effect and Foucault/Eddy currents. However, HVDC transmission lines require a higher investment cost linked to the ac-dc

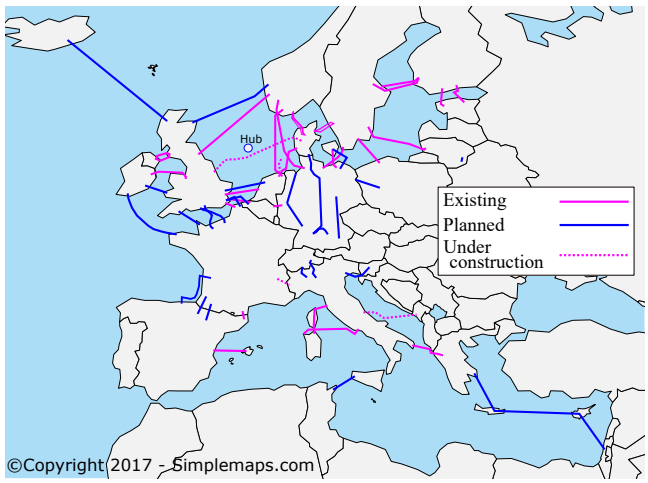


Figure 1.1: Present and future HVDC projects in Europe.

converter station. A general comparison between the ac and dc transmission lines total cost is presented in Fig. 1.2. The break-even distance depends on the project characteristics, e.g. total distance, rated power, and transmission line technology. In general, the break-even distance for projects with cable can be between 40 km and 120 km [2,3]. For projects with over-head lines (OHL), the distance could be above 800 km [4, 5].

The development of dc grids has been identified as an interesting approach to extend the benefits of HVDC lines to the interconnected system [6–8]. The North Sea has been subject to some related works [9–12] exploring the development of a new dc grid with homogeneous technical characteristics, e.g. same voltage level and line topology. However, as a promising solution to investigate, the already installed lines could be used to develop the dc grid. This last approach needs the development of dc-dc converters capable to interconnect lines with different technical specifications.

The dc-dc converters have been identified as one of the important building blocks for the development of future dc grids [6–8]. They can interconnect lines with different dc voltages but also with different technologies or line topologies.

This thesis studies dc-dc converters allowing the interconnection between lines that were not initially designed for multi-terminal operation. As example, Fig. 1.3 presents possible locations for a dc-dc converter interconnecting two links. The locations were chosen based on the intersection between projects.

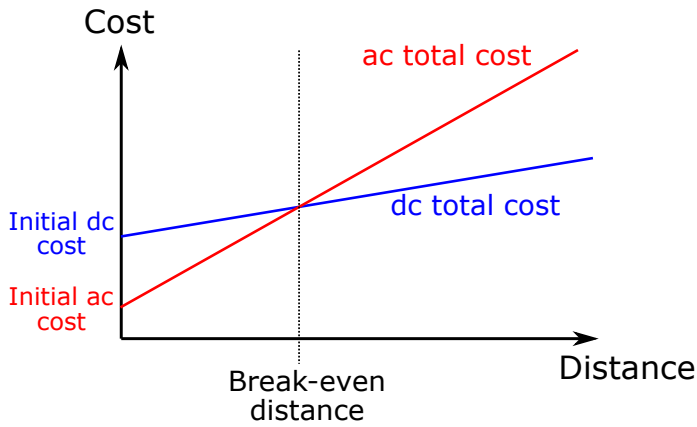


Figure 1.2: General comparison between the total cost of a project in HVAC (red) and HVDC (blue).

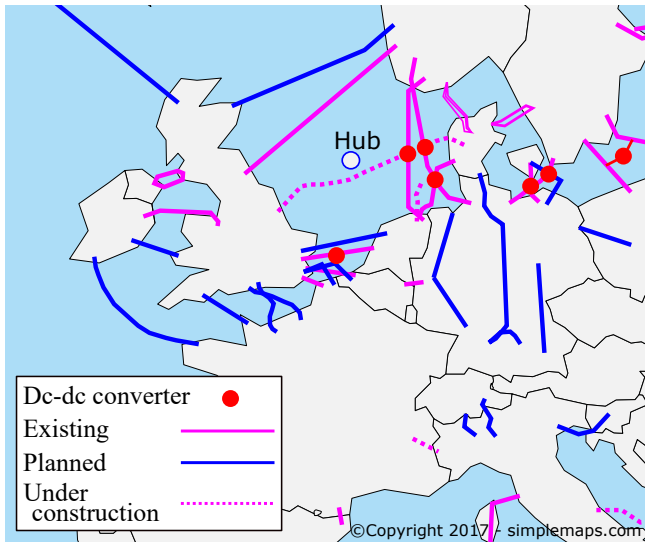


Figure 1.3: Examples of possible locations for a dc-dc converter using the present and future HVDC links (based on the situation in 2021).

To understand the general context of this thesis, different concepts must be introduced. Section 1.2 presents the different HVDC technologies used in the already installed projects. The different line topologies are explained in Section 1.3. A possible classification for the interconnections is proposed in Section 1.4. Then, the focus of this thesis is explained in Section 1.7.

1.2 HVDC technologies

Currently, there are two technologies used in HVDC projects: current source converters (CSC), also called line commutated converters (LCC); and voltage source converters (VSC). Both technologies are presented in the following subsections.

1.2.1 Line commutated converters

LCCs are the first technology used for HVDC applications. The first projects were developed during the 50s, where LCCs were initially based on mercury valves. However, with the development of the semiconductor devices, and to reduce the risk related with the mercury toxicity, the valves were replaced by thyristor valves, a presented in Fig. 1.4.

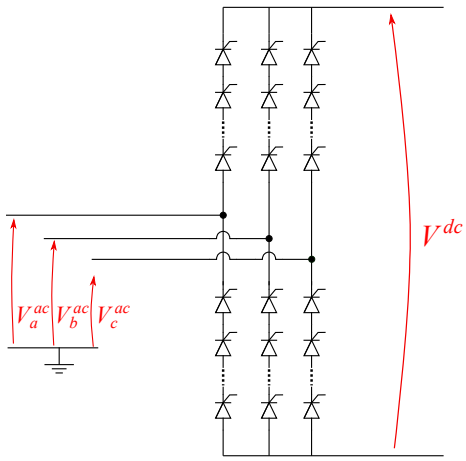


Figure 1.4: Basic schematic of a line commutated converter.

The thyristors are semiconductor switches that have a controlled turn-on. In order to turn off the device, an external source of energy should force the current through the thyristor to zero. Hence, the topology is named LCC as the converter depends on the ac grid (line) to turn off the thyristors. When the thyristors are in on-state, the current is allowed to flow in a single direction. LCC projects need to change the voltage polarity to change the power flow direction, which increases the complexity to implement them in multi-terminal schemes [5, 13, 14]. The thyristor valves are a mature technology that has excellent current and voltage ratings compared to the other HVDC valves. These switches have good resilience to overcurrents.

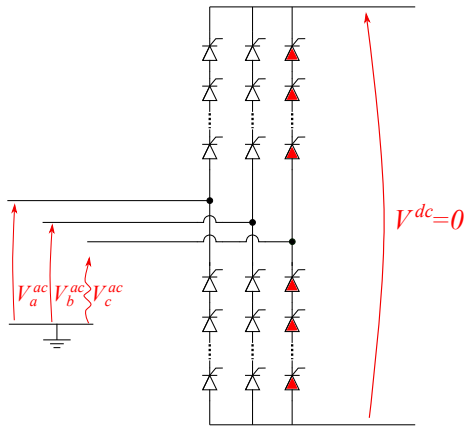


Figure 1.5: Commutation failure due to a transient event on the ac phase C.

One of the LCC drawbacks is that their commutation depends on the ac voltage. If a transient on the inverter ac side occurs, the LCC station might be unable to commutate, i.e. the converter has a commutation failure, equivalent to a dc short circuit (see Fig. 1.5). The detailed commutation failure process, with the different possible triggers, can be found in [15]. After a commutation failure, the LCC line control can reduce the dc voltage (reducing reactive consumption) until the ac system is recovered, which could take a few grid cycles. On the other hand, in the case of a dc fault, the LCC line can change the voltage polarity to extinguish the dc fault current without the need of a dc circuit breaker (DCCB) or triggering the ac protections. Since the LCC needs the ac grid to commutate the current in the valves, the HVDC projects based on this technology need to be connected to strong ac grids.

Another disadvantage of LCC projects is their footprint. LCC needs additional ac filters to compensate the reactive power and filter the harmonic produced by the valves switching events. This technology continues to be relevant for future projects considering OHL over long distances [16].

1.2.2 Voltage source converters

The voltage source converters have been used for HVDC applications since the late 90s. These converters are based on IGBTs with anti-parallel diodes, which allow the current flow in both directions but, the voltage polarity is fixed. The switches are controlled for the turn-on and turn-off events allowing higher converter controllability.

VSCs are capable to have independent active and reactive power control and they do not depend on the ac grid voltage to turn off the switches. Thus, these converters can be connected to weak ac grids providing them support in case of a fault, e.g. reactive current control during ac faults. Additionally, these converters can provide black-start capability as they can set the ac voltage reference to the ac grid.

Two level converters

The first VSC topology used in HVDC applications was the two level converter. The two level converter employs a series connection of IGBTs that require snubber circuits to balance the voltage at the time of switching. Additionally, this converter use a pulse width modulation (PWM) operating at some kilohertz which leads to a 1.4 % losses increase, compared to the 0.8 % for the LCCs [13]. An example of this converter is presented in Fig. 1.6.

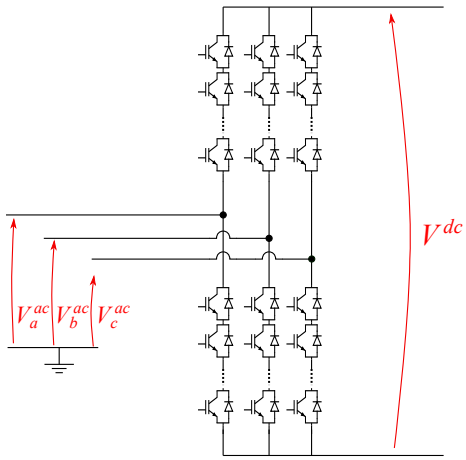


Figure 1.6: Two levels converter.

Modular multi-level converters

The modular multi-level converter (MMC) first proposed in [17, 18], has promote the use of VSCs in HVDC applications. This converter is composed of a series connection of sub-modules (SMs) as presented in Fig. 1.7. The MMC avoids the series connection of multiple IGBTs, which makes this converter easier to scale to high voltage applications compared to the two-level converter. The modular design of the MMC allows to change the voltage rating by changing the number of SMs per

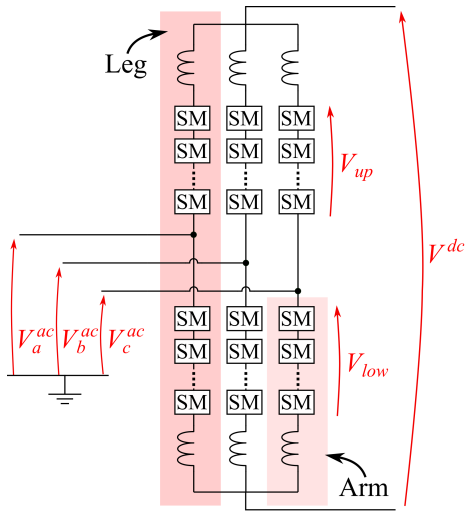


Figure 1.7: Modular multi-level converter. The squares between the ac-dc converters and the ac transformers represents the ac circuit breaker (ACCB) used to stop the fault current contribution from the ac grid.

arm. The MMC reduces the total losses by a lower switching frequency and the lack of snubber circuits. Due to the increased number of levels, the MMC does not need dc or ac filters, reducing the footprint of the converter station. Today, MMCs are the main VSC used in HVDC applications. They will be studied in detail in Chapters 2 and 5.

1.3 Line topologies

HVDC technologies are flexible and can be designed for different dc operating voltages and different line topologies. The operating voltages are mainly linked to the cable technology while the line topology could depend on the budget available and the required redundancy.

From the projects around the world, four different line topologies have been identified and presented in Fig. 1.8.

The first topology is the asymmetric monopole (AM), presented in Fig. 1.8a. It has a single high voltage (HV) conductor (cable or overhead line) and the return can be done through the ground or a metallic return with low voltage isolation, but full current capability. If a metallic return is used, a grounding point at one of the converter stations gives the reference. In case of a fault, the dc voltage collapses and high currents

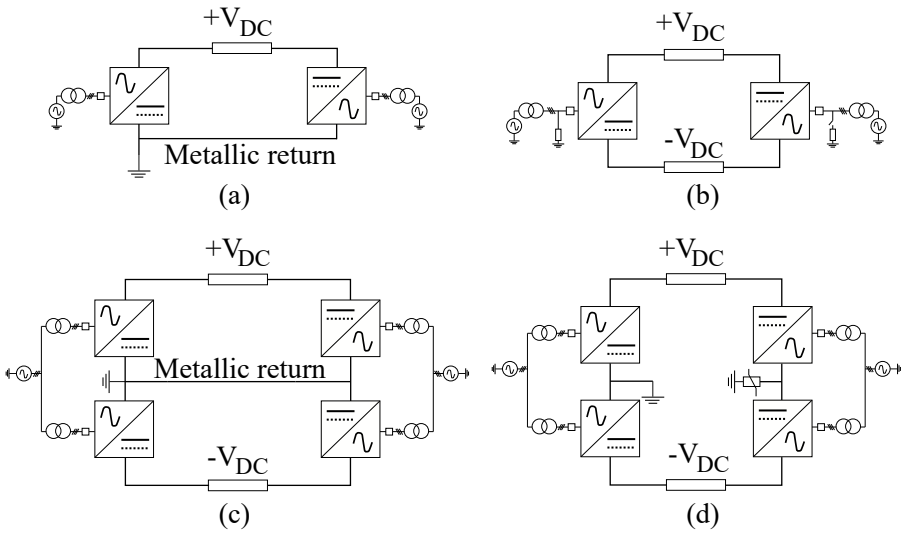


Figure 1.8: Line topologies identified in current HVDC links. (a) asymmetric monopole, (b) symmetric monopole, (c) bipole and (d) rigid bipole.

are present in the circuit. The pole-to-ground and pole-to-pole fault have similar behavior as one of the poles is earthed. The link is out of service until the fault is cleared.

The second topology is the symmetric monopole (SyM), showed in Fig. 1.8b. It uses two HV conductors whose voltages are symmetrically distributed to ground in normal operation. The converter does not have a dc connection to ground and the reference is given by the grounding strategy, generally, on the ac side. The ground reference is usually made with high impedance, represented as a rectangle in Fig. 1.8b. The SyM line might have a grounding impedance installed at both converter stations, depending on the project and manufacturers specifications, they can be both connected. In case of a fault in a conductor or converter, the power transmission is stopped until the fault is cleared. A pole-to-ground fault creates a pole displacement and the healthy pole may have an overvoltage, up to 2 p.u. without overcurrents. The pole-to-pole faults produce high currents similar to those described in the AM fault behavior.

The third topology is the bipole (B), showed in Fig. 1.8c. It is composed by two AMs. In normal operation, the current through ground or metallic return is negligible. In case of a fault (in a conductor or a converter) the bipole can continue to operate uninterrupted, at half of the nominal power, using the healthy pole and ground or metallic return.

The fourth and last topology is the rigid bipole (RB) [19, 20], showed in Fig. 1.8d. It is different to the bipole in that, it does not have a ground/metallic return and is different to the symmetrical monopole in that the RB has a dc reference point and an ac-dc converter per pole. The unearthed station is protected with a surge arrester presented in Fig. 1.8d. The RB can continue to operate after a converter fault, bypassing the faulted converter. This operation requires the activation of switchgears to isolate the faulted converter, i.e. the power transmission is interrupted. In case of a line contingency, the complete P2P link will be out of service until the faulted cable is repaired, or until the fault has been cleared in case of an overhead line.

1.3.1 Immediate and interrupted redundancy

As mentioned above, the bipoles have partial redundancy in case of pole faults as they can continue to operate with half of their initial rated power. A bipole link is redundant to converter and conductor faults, while the RB only for converter outages. The two line topologies (B and RB) have different process from the fault event to the post-fault scenario. The bipole with metallic or ground return provides immediate redundancy, meaning that it can continue to exchange half of the power rapidly, while the RB must interrupt the power flow, reconfigure the circuit to isolate the faulted converter and restart the power exchange. The terms immediate redundancy and interrupted redundancy are used in this thesis to refer to the different process to achieve the post-fault redundancy.

1.4 Possible HVDC interconnections

HVDC multi-terminal schemes or HVDC grids can be developed designing everything before its construction or using the already installed projects. Most of the already installed HVDC projects have not been designed to operate as a multi-terminal scheme. These projects have different line topologies, different technologies, and different voltage and power ratings. Thus, dc-dc converters can be used to control and adapt the differences between the projects.

Depending on the characteristics of the projects to be interconnected, the interconnection between two HVDC projects or grids can be classified into homogeneous and heterogeneous interconnections. The concepts are detailed below.

1.4.1 Homogeneous Interconnections

The HVDC homogeneous interconnections are interconnections between dc systems with similar characteristics. These interconnections require a dc-dc converter to adapt the dc voltage difference, similar to the use of ac transformers in the classical ac transmission system. The voltage ratio is the relation between the dc voltages of the interconnected lines, as follows.

$$V_{ratio} = \frac{V_1^{dc}}{V_2^{dc}} \tag{1.1}$$

where V_1^{dc} and V_2^{dc} are the dc voltage of the first and second line respectively.

The dc-dc converters considered for homogeneous interconnections have low to medium voltage ratio [7] and interface projects with the same line topology. The interconnection between project with different technologies (LCC-VSC) are also considered homogeneous interconnections if the power flow on the LCC side is not reversed, i.e. if the voltage polarity on the LCC link remains unchanged.

Most of the literature presenting dc-dc converters for HVDC applications evaluate the converter behavior for homogeneous interconnections as they propose the interconnection between projects with the same line topology.

1.4.2 Heterogeneous Interconnections

The heterogeneous interconnections are the interconnections between dc systems with different line topologies, different technologies, or with a high voltage ratio [7].

The differences in voltage and line topology make it impossible to interconnect the two systems without a dc-dc converter. The dc-dc converter is needed to withstand the voltage difference. As explained earlier, the line topologies have different transient responses during faults thus, the dc-dc can be used to decouple the dc systems during these events. As previously stated, the interconnection between different technologies can be challenging if the LCC project considers the power reversal.

1.5 Dc-dc converter degraded operation

The power outages in HVDC systems could be costly and could have a considerable impact on the connected ac grids. Thus, reducing the outage time is of high interest. Some HVDC projects use line topologies with redundancy, see Section 1.3.1, which can reduce the impact of a contingency on the stability of the ac grids. Therefore, it seems natural to request a dc-dc converter, interconnecting a B or RB, to provide the same redundancy of the interconnected lines, e.g. for a bipole, after a fault on one pole the healthy pole continues to operate uninterruptedly.

For the dc-dc converter to provide redundancy it is possible to require a reconfiguration or operate in a degraded mode. The dc-dc converter is considered to be in degraded operation if the line topology at its terminals has changed. This can occurs after the complete loss of a pole of an initial B or RB line. In this situation, the initial bipole line continues to operate as an AM which changes the operating conditions of the dc-dc converter (see Fig. 1.9b). When a fault occurs in a system able to isolate the faults, the line topology at the terminals of the dc-dc converter does not change thus, it is not considered a degraded operation (see Fig. 1.9a).

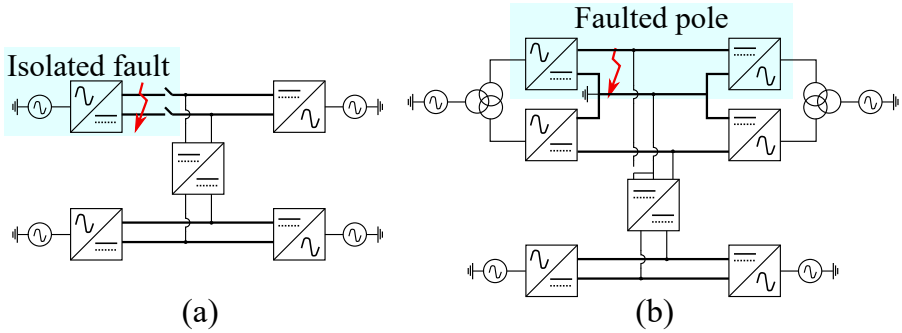


Figure 1.9: Impact of a fault on the dc-dc converter. (a) in this example the system able to reconfigure does not change the line topology, i.e. the dc-dc converter is connected to a SyM before and after the fault. (b) A fault on a bipole could take out of service the complete pole, the dc-dc converter is now connected to an AM.

1.6 Fault blocking capability

The fault blocking capability (FBC) is the dc-dc converter ability to avoid the fault propagation to healthy zones. For instance, the fault event in one link should not generate transients on the second link that can trigger

its protection schemes, i.e. the fault cannot be propagated to healthy zones. Depending on the event, some voltage or current transients can appear on the healthy zones but these must be kept operational. The study carried in this thesis assume that the dc-dc converter must have FBC.

1.7 Problem statement and thesis scope

With the increased interest to integrate renewable sources in the electrical transmission system, HVDC technologies have been taking place as complementary solution especially for offshore applications. HVDC grids could interconnect different sources of energy and countries over long distances strengthening the overall transmission system. In the case of Europe, the North Sea is a particular region where this development could take place.

From the already installed projects, it can be estimated that the dc grid could have a step-wise development interconnecting links with dc-dc converters creating multi-terminal radial schemes or dc meshed systems. Due to the flexibility of HVDC converters and systems, the technical characteristics of the HVDC projects vary from one to another depending on the requirements of each project. The dc-dc converter needs to adapt not only the dc voltage but, also (probably) the line topology or the technology.

This thesis focuses on the dc-dc converters suitable for these HVDC heterogeneous interconnections. The interconnection is based on the hypothesis that the HVDC links are already installed and no major modifications can be implemented, e.g. voltage ratings, protection scheme, cables or converters. The dc-dc converter should be a device that does not affect the normal operation of any of the initial HVDC links and should provide FBC. The system level studies are out of the scope of this work, e.g. multi-terminal control, system protections, ac grids stability. The main objectives of this thesis can be summarized as follows.

1. **Identify the requirements for the dc-dc converters interconnecting heterogeneous HVDC links.**

2. **Improve the converter topologies found in the literature or propose new ones.**

3. **Validate the technical solutions with simulation models.**

The specific objectives needed to achieve the main thesis goals are:

- **Study the state-of-the-art of dc-dc converters for HVDC applications.** Evaluate the different dc-dc converters proposed in the literature and estimate their technical feasibility for the heterogeneous interconnections.

- **Study the present and future HVDC links in Europe.** From the already installed and future HVDC projects, identify the most probable interconnection.

- **Identify the converter requirements for the most probable interconnection.** From the identified interconnection, determine the dc-dc converter requirements which respect the initial assumptions.

- **Identify the main dc-dc converters suitable for the chosen interconnection.** From the literature review, propose a set of dc-dc converters suitable for the identified interconnection.

- **Analyze the considered dc-dc converters.** Create the mathematical models and propose a simplified control strategy for each of the considered dc-dc converters. The validation can be done with simulation models or practical implementation (if possible).

- **Compare the considered dc-dc converters.** Propose quantitative and qualitative indicators to compare the feasibility and performance of the chosen dc-dc converters.

1.8 Thesis outline

The thesis is divided in the following chapters:

- **Chapter 2** presents the dc-dc converters for HVDC applications found in the literature. The different solutions are analyzed for their application on heterogeneous interconnections. Three converters are chosen as candidates for the identified interconnection (the front-to-front modular multi-level converter, the flexible dc-MMC, and the asymmetric dc-dc converter).

- **Chapter 3** introduces a proposed methodology to analyze the modular converters. The methodology is used to define the mathematical model, size the passive components and design the control strategy.

- **Chapter 4** defines the case study where the dc-dc converters are tested. The case study considers the interconnection identified from the present and future HVDC links. The links are modeled including ac circuit breakers, ac-dc converters, cables, grounding strategy and some protection devices. This chapter also presents the proposed simulation scenarios to test the dc-dc converters under nominal, normal, and fault conditions.

- **Chapter 5, 6 and 7** analyze the front-to-front with modular multi-level converters, the flexible dc-MMC, and asymmetric dc-dc converter respectively. The analysis is based on the methodology introduced in Chapter 3 which includes the mathematical model, sizing and control strategy design. The simulation results of the converters operating in the case study are also presented.

- **Chapter 8** compares the three dc-dc based on a set of key performance indicators (quantitative comparison) and the ancillary services that the converters can provide to the dc system (qualitative comparison).

- **Chapter 9** summarizes the conclusion of the thesis and introduces the future research based on the topics addressed in this work.

Chapter 2

Overview of HVDC dc-dc converters

2.1 Introduction

This chapter presents an overview of the dc-dc converters found in the literature dedicated to the HVDC applications. The converters are classified based on the categories proposed in previous publications [21–23]. Isolated and non-isolated converters are presented in this chapter evaluating their adaptability to heterogeneous applications.

Some of the dc-dc converters proposed in the literature use ac-dc converters in a front-to-front (F2F) configuration (see Section 2.3.1). Therefore, a general review of the principal ac-dc converters is presented first.

2.2 Ac-dc converters

A general state of the art of the ac-dc converters is presented here as they can be used as part of the isolated dc-dc converters (see Section 2.3).

2.2.1 Modular multi-level converter (MMC)

After its first publication in [17,18], the MMC is the main converter studied in the literature for HVDC applications. The ac-dc MMC is currently used in multiple HVDC projects around the world and continues to be considered for future applications. Figure 2.1 shows an MMC, which is composed of 3 legs (or phases), but the converter can work with n legs ($n \geq 2$). If a single-phase converter is considered, additional filters are needed to avoid ac components circulating in the dc side. Each leg of the MMC has two arms, which are a series connection of sub-modules (SM) and an arm inductor. At the connection point between the two arms, an output terminal connects the converter to an ac system (V^{ac}) through an equivalent inductance (it could be an ac transformer).

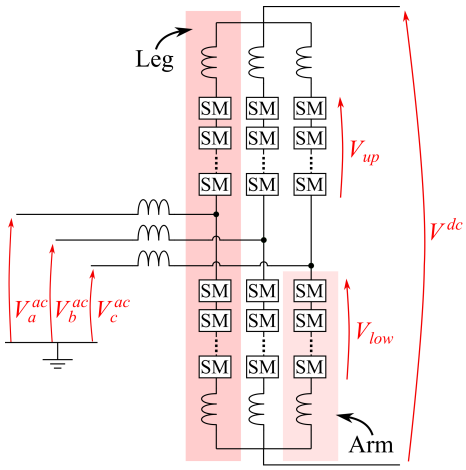


Figure 2.1: Ac-dc modular multi-level converter.

The main SMs used in the MMC are presented in Fig. 2.2: the half-bridge SMs (HBSM) in Fig. 2.2a and the full-bridge SMs (FBSM) in Fig. 2.2b. Different structures of SMs can be found in [24–27], but they usually increase the number of semiconductor devices and, in consequence, the conduction losses. The HBSM is capable to insert and bypass the SM capacitor (C_{SM}). The FBSM have an additional state where the capacitor is inserted in negative polarity, i.e. the converters using FBSMs can have negative modulation.

When the HBSM is not controlled, i.e. it is in blocked state, the IGBTs are open and the current through the SMs depends on the voltage across the diodes. The voltage across the upper diode depend on the arm voltage and the voltage of the internal capacitor (C_{SM}). The voltage of the lower diode is equivalent to the voltage at the terminals of the SM. If the upper diode is forward biased, the current can flow through the capacitor charging it. On the other hand, if the voltage at the terminals of the SM is negative, the current is bypassed through the lower diode.

When the FBSM is in blocked state the four diodes can allow the current flow through the SM depending on the arm voltage and the voltage of the internal capacitor. Different from the HBSM, the current through the blocked FBSM always goes through the internal capacitor, charging it. The current stops when arm voltage disappear or when the equivalent voltage of all FBSMs in the arm equalizes the external voltage. If enough FBSMs are installed in a converter they can be used to control or stop the fault currents, i.e. a converter with enough FBSMs has fault blocking capability.

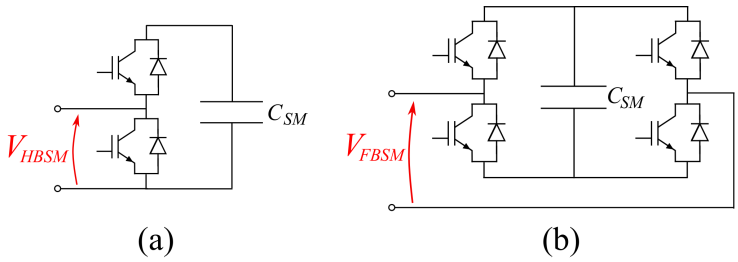


Figure 2.2: Most common sub-modules used in MMCs: the half-bridge SM (HBSM) presented in (a) and the full-bridge SM (FBSM) presented in (b).

The converter can insert or bypass SMs in the arms to control the voltages V_{up} and V_{low}, shown in Fig. 2.1. In steady state, neglecting the losses and the voltage drop across the arm inductances, the sum of the arm voltages is V^{dc}, and the difference is the ac voltage V^{ac}.

Depending on the rated voltage of the SM, the MMC arm can be composed of dozens or even hundreds of them. The total number of SMs per arm should be able to generate the dc voltage V^{dc} (if the third harmonic injection is not considered [28]). The large number of SMs employed by the MMC allows it to define ac voltages with low harmonic content. The MMC is controlled to have low switching losses. The main losses come from the conduction losses, which increase with the number of IGBTs in series.

2.2.2 Hybrid ac-dc converters

Hybrid ac-dc converters combine a series connection of switches and SMs [29, 30]. The series connection of multiple switches is challenging in HV applications as it requires special strategies to balance the voltage across the connected switches [31]. The main hybrid converters are introduced in the following subsections.

Alternate arm converter (AAC):

The AAC is proposed to decrease the MMC losses while adding the fault blocking capability [32–35]. It is composed of two arms per leg, and each arm is composed of a series connection of SMs, an inductor, and a director switch as shown in Fig. 2.3. The director switch can be a series connection of IGBTs [32–34] or anti-parallel thyristors [35]. The AAC creates the ac voltage (V^{ac}) alternating the connection of the arms. The

upper arm is used for the positive part of the ac signal, while the lower arm only is connected to the negative part. This operation avoids the simultaneous conduction of the complete leg, reducing the conduction losses. For the AAC, the voltage rating of each arm is around half of the dc voltage (V^{dc}), but the use of FBSM is mandatory because the peak of the ac voltage is higher than half of the dc voltage [32], i.e. a negative modulation is required. Soft switching can be achieved by reducing the voltage across the director switches. The combination of a lower number of SMs per arm and soft-switching operation leads to lower power losses compared to the MMC.

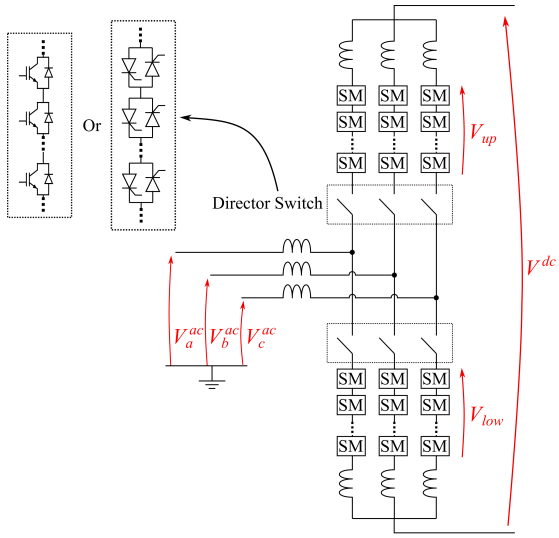


Figure 2.3: Alternate arm converter.

The power loss reduction comes with some additional difficulties such as the abrupt current commutation between arms every time the ac voltage changes its sign; difficulties to keep the internal energy balance, i.e. voltage on the SMs, and high dc current ripple. To solve these problems, an overlap time is used to commutate the current between arms in a smoother way. Depending on the duration of the overlap time, each arm will withstand an increased dc voltage, which increases the required number of SMs per arm [33]. This strategy works better for power factors near to 1 and a maximum modulation index of 1.27 (sweet spot) [30]. The AAC can have fault blocking capability if a sufficient number of FBSMs are installed on each arm. Despite the strategies to balance the

energy in the converter, the dc current ripple is still present, hence, dc filters or the installation of a flying capacitor proposed in [34], might be necessary.

The AAC might reduce the losses compared to the MMC, but it requires a sensible operation leading to difficult energy balance and harmonics. The AAC uses a series connection of IGBTs for the director switch, which is difficult to achieve in HV applications.

Series bridge converter (SBC)

The SBC, shown in Fig. 2.4a, was first proposed in [36]. It is composed of identical building blocks, each one connected to an ac phase. Each block comprises a rectifier, IGBT based, and a series connection of SMs then, the blocks are connected in series to achieve the dc voltage (V^{dc}). This initial converter has the problem of coupling the magnitudes of the ac and dc voltages, so it is not possible to control the reactive power exchange [37].

A variation of the initial SBC was proposed in [37] allowing the reactive power control, i.e. decoupling the ac and dc voltages. The new converter is presented in Fig. 2.4b. Compared to the initial converter, the new SBC has a series connection of FBSM between the rectifier and the main HBSMs stack. Due to its configuration, the SBC has a reduced number of components, about 30 - 35% of those required by an equivalent MMC [37].

References [37,38] present a balancing mechanism using a second harmonic circulating current. This harmonic allows the converter to exchange power between the FBSMs and the HBSMs without disturbing the ac or dc sides, i.e. no need of filtering.

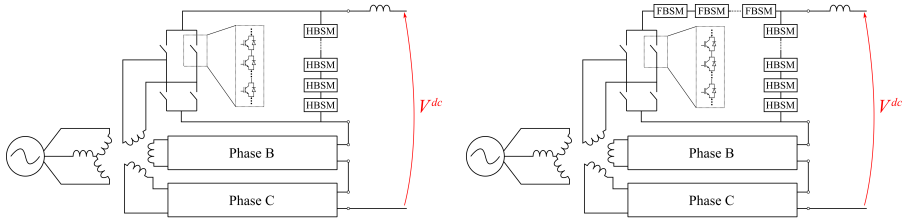


Figure 2.4: Series bridge converter proposed in [37].

The SBC is a suitable alternative to the MMC ac-dc, but further research should be done to understand the complex energy interactions.

Active forced commutated bridge

The active-forced commutated bridge (AFCB), initially proposed in [39–41], uses a series connection of anti-parallel thyristors per arm. Associated to each arm, there is a FBSM stack used to force the thyristors commutation (see Fig. 2.5). By using thyristors, the converter reduces the conduction losses compared to the MMC. The FBSM stacks are mostly used to control the converter. The principal power circuit is through the thyristors [40]. Therefore, the FBSMs do not increase the power losses in the converter. In addition to the low conduction losses, the AFCB can reduce the switching losses by commutating the thyristors at a near-zero voltage (zero voltage switching). Furthermore, the FBSMs can be used to stop the fault currents. The number of FBSMs should be enough to commutate the current in the thyristors, i.e. the stack must be able to generate more than $V^{dc}/2$.

The main drawbacks of the AFCB are the harmonics presented on the ac side. These harmonics can increase the complexity of the ac transformer. The use of dc capacitors or dc filters is also inconvenient for applications where the footprint is important. For ac applications, the AFCB should have additional ac filters.

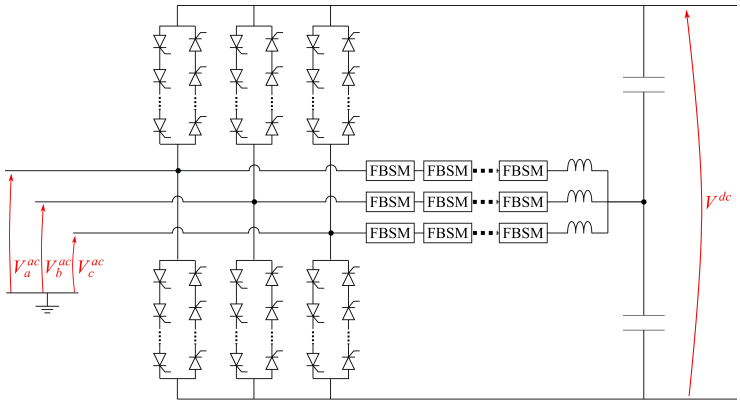


Figure 2.5: Active forced commutated bridge.

2.2.3 Unidirectional ac-dc converters

Under the category of unidirectional ac-dc converters, we can find the diode and thyristor rectifiers [42]. These converters can be used in specific applications where the power flow is needed in only one direction. For instance, a line interconnecting a generator and a load as shown in Fig. 2.6.

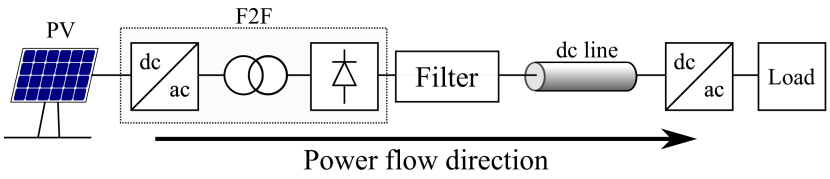


Figure 2.6: Unidirectional F2F converter interconnecting a photovoltaic (PV) generation plant with a load.

2.3 Isolated dc-dc Converters

The isolated dc-dc converters decouple the interconnected systems by means of a galvanic separation, provided by an ac transformer or coupled inductors [21]. The galvanic isolation can simplify the interconnection between systems with different characteristics, hence isolated converters are suggested for the heterogeneous interconnections in [6, 7].

2.3.1 Dual Active Bridge

The dual active bridge (DAB) employs two ac-dc converters linked by an ac transformer [23]. The DAB converter suitable for HVDC applications can be based on cascaded multi-converters or the front-to-front (F2F) converters presented in the following subsections. These converters could use any ac-dc converter presented in the previous section.

Cascaded Multi-converter

As its name suggests, the cascaded multi-converter uses multiple converters to achieve the interconnection between two dc systems [43–46]. Usually, the multi-converter uses a parallel connection at the low voltage (LV) and a series connection at the high voltage (HV) side but any combination of series/parallel connection can be implemented depending on the power and voltage level of the interconnection [43]. Figure 2.7 shows the simplest ac-dc converter that can be used in this configuration: the VSC two-level.

This structure is highly modular and scalable, which grants it adaptability to different applications. The main inconvenience is the insulation coordination of each of the modules. Indeed, each of the elementary DAB has different insulation constraints depending on its position in the structure. The insulation requirements could increase the complexity of the transformer design. For instance, the winding on the HV side of DAB 1 in Fig. 2.7 has additional insulation requirements compared to

the DAB n, changing its geometry, i.e. each DAB is designed individually or most of them will have an oversized insulation. This limits the use of this topology to applications of medium voltage ratio [21, 23]. An additional challenge for this structure is the volume used by the passive components, in particular the transformers. Increasing the operating frequency can reduce the size of the components [21, 23], but the voltage insulation requirements can limit the volume reduction.

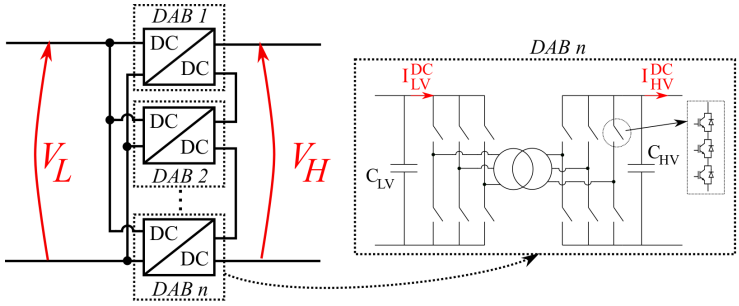


Figure 2.7: Modular multi-converter with parallel connection at the LV and series connection at the HV side.

Front-to-Front

The front-to-front is the principal topology suggested for HVDC applications [42, 47–50]. The F2F uses two HV ac-dc converters and an ac transformer, as shown in Fig. 2.8. The ac-dc converters can be identical on both sides or may differ, depending on the application. The choice of the ac-dc converter might impact the transformer requirements, but they are not limiting factor. The principal ac-dc converters suitable for the F2F converter were presented in Section 2.2.

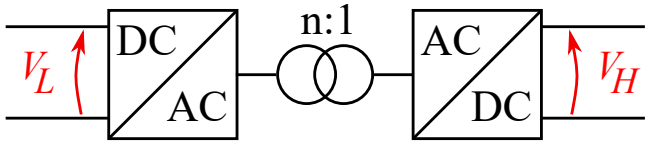


Figure 2.8: Basic F2F interconnecting two dc systems. the transformation ratio of the transformer is proportional to the voltage ratio of the dc sides: V_L/V_H.

The F2F is a flexible configuration that can be adapted to any interconnection thanks to the ac transformer. The transformer allows changing the voltage ratio decoupling the dc sides. Most of the F2F proposed in

the literature have an internal ac system decoupled from the transmission ac grid therefore, the parameters of the ac system are a degree of freedom in the converter design, i.e., voltage magnitudes, frequency.

The different applications are detailed below.

- **Different voltage level:** thanks to the ac transformer, the voltage ratio can be adapted to any application by changing the turns in the windings. As explained early, the main challenge for the transformer is the voltage insulation. References [42, 51] present an example for a F2F with high voltage transformation: the low power high ratio (LPHR) converter.

- **Different technology:** the interconnection between VSC and LCC systems can be achieved if a suitable ac-dc converter is used on the LCC side [52–56]. If the LCC system changes the power flow direction, an ac-dc converter with bipolar dc voltage capability should be used, e.g. MMC with FBSM [52] or current source SMs as presented in [53]. Otherwise, if the power flow direction is constant, any ac-dc can be used on the LCC side. The F2F must be able to withstand commutation failures (see Section 1.2.1) on the LCC side, either by control strategy or FBC in the ac-dc converter. The F2F-AFCB is presented in [39] for this heterogeneous interconnection. The F2F-AFCB is interesting because the ac harmonics are not restricted by the ac grid code. However, the impact on the ac transformer has not been studied.

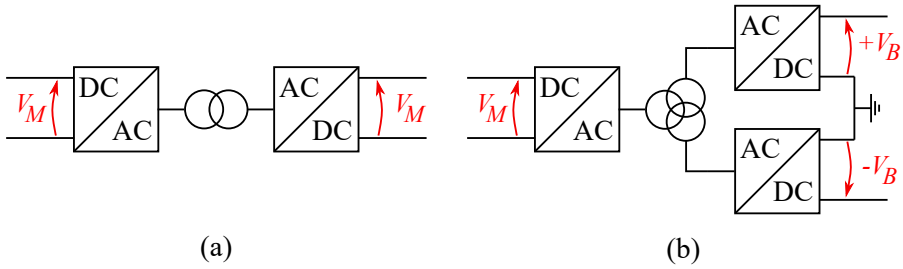


Figure 2.9: Front-to-front configurations for heterogeneous interconnections. (a) interconnection between monopoles (AM-SyM). (b) interconnection between a monopole, either AM or SyM, and a bipole (B or RB).

- **Different line topology:** the transformer in the F2F not only allows to change the voltage ratio but also adapts the different line topologies by decoupling the grounding schemes at both sides of the

transformer. Changing the configuration of the windings [57–61], allows the F2F to interconnect any of the four line topologies presented in Section 1.3. Figure 2.9 shows the transformer configuration for the interconnections between two monopoles (Fig. 2.9a), and between a monopole and a bipole (Fig. 2.9b).

2.4 Non-isolated dc-dc Converters

The non-isolated dc-dc converters do not provide galvanic isolation. A reduced total volume and power losses, compared to the F2F, is the main expected advantage of the non-isolated converters [6, 62]. This feature is particularly important in offshore applications where the cost of the platform footprint is critical.

The non-isolated dc-dc converters suitable for heterogeneous interconnections, are presented below.

2.4.1 Dc Auto-transformer

This converter has been proposed to reduce the number of switches and the total volume of the converter, compared to the F2F-MMC [63–65]. It is composed of two ac-dc converters connected in series on the dc side and front-to-front on the ac side (see Fig. 2.10).

The main advantage of the auto-transformer (AT), compared to the F2F, is that only a portion of the total exchanged power has to be inverted and rectified [64]. The power through the ac link depends on the total transferred power and the voltage ratio, defined in (1.1), of the interconnected lines. The ac power is defined by:

$$P^{ac} = P\frac{V_{ratio} - 1}{V_{ratio}} \tag{2.1}$$

where P is the power exchanged between the dc lines.

The reduced ac power decreases the size of the ac transformer, which in turn decrease the total volume of the dc-dc converter [64]. The ac transformer turns ratio can be adapted to improve the device utilization.

The AT has better performances for small voltage ratios due to the internal ac circulating power, i.e. the AT have highers losses when the dc voltage ratio increases. For high voltage ratios, the rated power of the ac transformer and switches becomes similar to the F2F-MMC, reducing

the interest of the AT [63, 64]. Despite the volume reduction, the ac transformer has important design requirements, such as an dc offsets that can increase the insulation requirements [66].

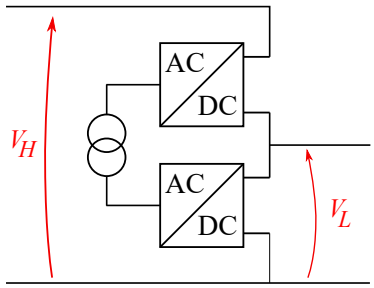


Figure 2.10: Dc auto-transformer for homogeneous interconnection.

The AT can be used for the interconnection between different technologies as the study case presented in [65]. Different converter configurations can be used to interconnect different line topologies as presented in [58].

2.4.2 Transformerless converters

The non-isolated dc-dc converters can reduce the number of switches, the conduction, and switching losses compared to the F2F-MMC. But the main advantage of the non-isolated converters is the volume reduction due to the absence of a bulky ac transformer. The F2F and AT can reduce the transformer volume by increasing the operating frequency, but the insulation requirements remain a complicated issue to solve. The transformerless dc-dc converters are proposed to improve the F2F performances without the presence of an ac transformer. The most interesting converter topologies, for heterogeneous interconnections, are presented below.

Transformerless auto-transformer

Figure 2.11 shows the transformerless AT presented in [67]. Similar to the AT, the transformerless AT works better for low voltage ratio applications, but the transformerless AT has a reduced device utilization.

The transformerless AT replaces the ac transformer with a filter, which must use a capacitor to withstand the dc voltage difference between the interconnected systems. Reference [67] explores the steady-state operation, but further fault studies must be carried to evaluate the effect of

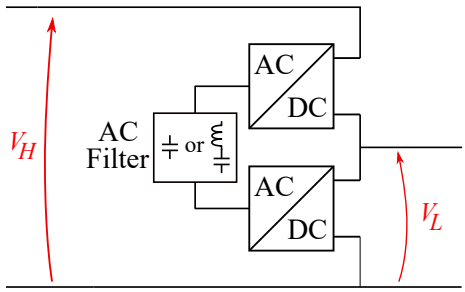


Figure 2.11: Transformerless auto-transformer.

the filter resonances. Analogous adaptations, to interconnect different line topologies [58] or different technologies [65], can be applied to the transformerless AT.

Non-isolated F2F

Similar to the transformerless AT, the non-isolated F2F replaces the ac transformer with a filter. The filter is usually an inductance-capacitor (LC) tank but different configurations can be used. A series connection of inductances is presented in [68] and a series connection of inductances with a shunt capacitance (LCL) is presented in [69]. The non-isolated

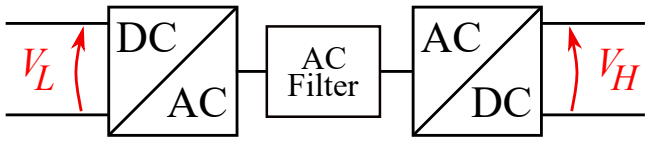


Figure 2.12: Non-isolated F2F converter.

F2F does not have the inconvenience of the insulation transformer design, therefore the harmonic content in the ac stage is not critical. Similar to the isolated F2F, the non-isolated can use different converter topologies at both ends. The non-isolated F2F, cannot be used for high voltage ratio interconnections. The resonant filters can lead to important stress in the switching devices. This topology continues to use two ac-dc converters rated to the full transmitted power, which is bulky and costly.

Dc modular multi-level converter

The dc modular multi-level converter (dc-MMC) or M2dc [70, 71] is presented as a promising solution as it reduces the total converter size, compared to the F2F, by avoiding the ac transformer and reducing the total number of components. The dc-MMC has less components than the

F2F-MMC because it has a single dc-dc conversion stage. This reduction depends on the voltage ratio, decreasing the number of components down to 50% for a 2:1 ratio [72,73]. The dc-MMC can block the fault currents if enough FBSMs are installed in the upper arm, which can countervail the lack of galvanic isolation. The dc-MMC could have a fast industrial development because of its similarity with the ac-dc MMC [18]. The main topological difference is the connection of the ac ports (see Fig. 2.13).

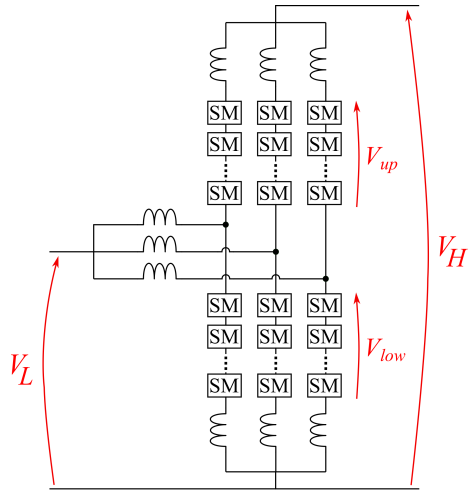


Figure 2.13: Monopolar dc modular multi-level converter.

The dc-MMC presented in Fig. 2.13 is a bidirectional dc-dc converter able to interconnect two AM systems [6, 74–76]. It can be evidenced that there is a common terminal between the two dc sides (usually the ground). In consequence, this converter is called the *monopolar* dc-MMC in the rest of this thesis.

The monopolar dc-MMC is an interesting topology that has been the subject of several studies. A comparison with the F2F-MMC has been presented in [62, 77], concluding that the dc-MMC is an attractive solution for low voltage ratio applications. An optimal design workflow to size the arm inductance and the SMs capacitance is presented in [78,79]. The control strategy and optimal operation points are studied in [74,76,80,81]. The control presented in [80], reduces the disturbances on the healthy side by controlling the internal energy during a fault. The optimization of the internal ac voltages and the number of SMs is presented in [75]. An optimal design workflow to size the arm inductance and the SMs capacitance is presented in [78,79]. A dc-MMC with active ac filtering and fault blocking capability is presented in [82]. Recently, a

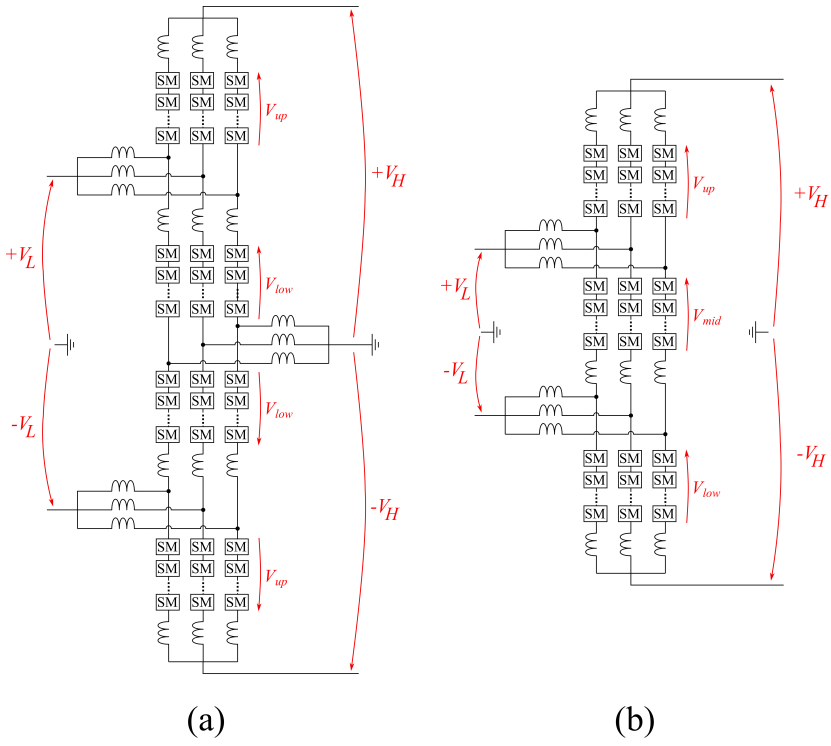


Figure 2.14: Dc-MMC for bipolar interconnections (a). Flexible dc-MMC for heterogeneous interconnections (b).

monopolar structure has been presented in [73], which reduces the arm currents stresses using a center-tapped transformer, replacing the output inductances. A variation of the monopolar dc-MMC is presented in [83] for multi-port applications. The monopolar dc-MMC has drawn the attention of the CIGRÉ working group B4.76, which has evaluated the converter response in steady-state operation and faults [6,84], finding good performances.

The monopolar dc-MMC has been widely studied, but it has a limited range of applications. The converter can be only used for the interconnection between two asymmetric monopoles. The arrangement of two monopolar dc-MMCs (one per pole) was proposed for the bipolar interconnections [72,85,86] and presented in Fig. 2.14a. The bipolar dc-MMC can be used to interconnect two bipoles or two symmetric monopoles. The new converter uses a set of inductors providing a low impedance dc path to ground. These inductances also allows the ac circulatin power inside the converter [85]. The control modeling and control strategy pro-

posed in [86] can be used for the interconnection between a symmetric monopole and a bipole, but in case of a fault on the bipole side, the control is not suitable to operate in the degraded mode (see Section 1.5).

The flexible dc-MMC (see Fig. 2.14b), which is based on the bipolar dc-MMC, is a result of this thesis proposed in [87] for different heterogeneous interconnections. The converter avoids the use of inductors to ground, which links the interactions between the three arms. The publication explores the interconnection RB-SyM, presenting simulation results in steady-state operation. The degraded mode is also considered, equivalent to an interconnection AM-SyM, with satisfactory simulation results. The flexible dc-MMC is suitable for the interconnection B-SyM if immediate redundancy is not required, i.e. after a fault on the B side the power transmission stops while the flexible dc-MMC is reconfigured to isolate the fault. Additional details on the flexible dc-MMC can be found in Chapter 6.

Double Wye converter

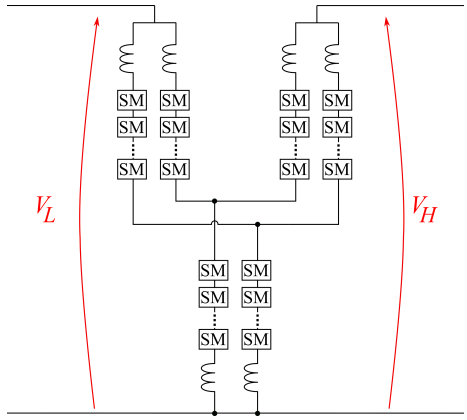


Figure 2.15: Double wye converter proposed in [88].

The double Wye converter is similar to the monopolar dc-MMC but instead of a passive filter, the low voltage side is connected through an additional arm [88], i.e. a stack in series with an inductor. The double Wye converter does not require FBSMs to stop the fault currents if enough HBSMs are installed to withstand the dc voltages during a fault. The converter structure is presented in Fig. 2.15.

Due to its similarity to the monopolar dc-MMC, the double Wye converter could be adapted to the interconnection between different line topologies as the bipolar or flexible dc-MMC. It would be necessary to

duplicate the monopolar circuit (one per pole), similar to the converter presented in Fig. 2.17c. The final circuit and variations can be the object of future researches. The converter remains optimal for low voltage ratios.

Dc-dc MMC

Another non-isolated converter, the dc-dc MMC, is proposed in [89, 90]. It has an structure in "H" as presented in Fig. 2.16. The converter is composed of four hybrid stacks, i.e, a series connection of FB and HB SMs, and two FB stacks. The hybrid stacks are sized to provide FBC. The high voltage dc system is connected at the terminals of the hybrid legs and the low voltage is connected at the output of the FB stacks.

The converter is proposed for the interconnection between two bipoles with different technologies (VSC-LCC). The converter presented in [90] proposes an additional auxiliary leg to allow the degraded mode operation, i.e. after a fault in a pole of a line, the converter can continue to operate at half of the rated power.

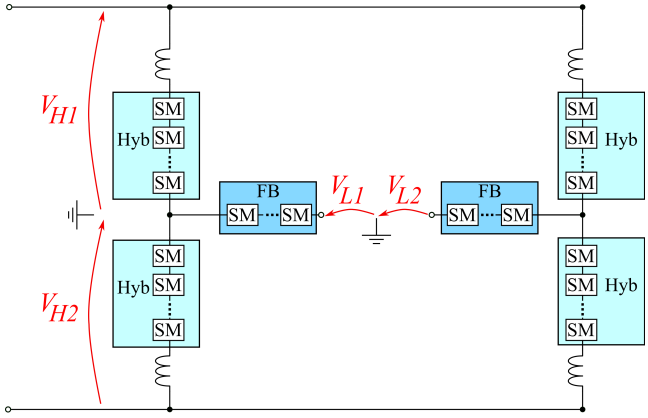


Figure 2.16: Dc-dc MMC proposed in [89, 90]. The converter uses FB stacks and stacks with HB and FB SMs (Hyb).

MMC dc-dc buck-boost

Based on the dc-dc converters for LV applications, reference [92] presents a methodology to adjust the circuits for HVDC applications. A base circuit, from which different dc-dc converters can be obtained, is presented in [91]. The converter includes three main sections (k, r, and h) interconnected by an optional ac transformer, as shown in Fig. 2.17a. By remov-

ing the legs (k, r, or h), or the transformer the structure can represent most of the non-isolated dc-dc converters presented in this chapter. Figure 2.17b displays the converter presented in [92], which can be adapted to the SyM interconnections [22] (shown in Fig. 2.17c). The buck-boost converters are compared in [22] to obtain the optimal voltage ratio for each of the converters.

Following the structure presented in Fig. 2.17c, the buck-boost converters can be adapted for the interconnections between different line topologies.

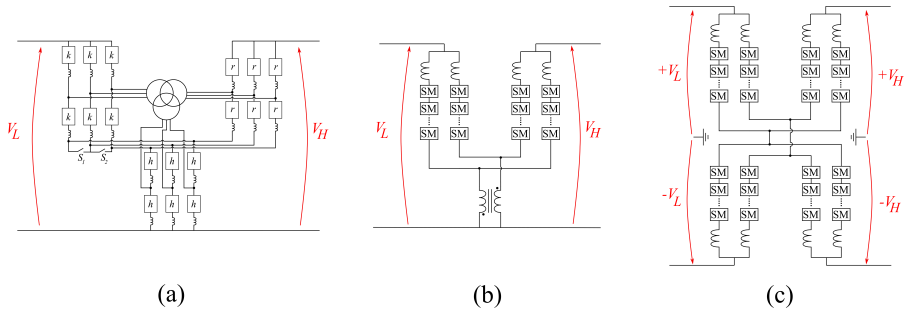


Figure 2.17: Buck-boost topologies. (a) General circuit for non-isolated topologies proposed in [91]. (b) Buck-boost topology proposed in [92]. (c) Simplified dc-dc converter interconnection of SyMs [22].

Hybrid cascaded dc-dc converter

The hybrid cascaded dc-dc converter (HCDC) [93] is a converter family that mixes the series connection of switches and SMs to simplify the structure of the converter (see Fig. 2.18). The HCDC has been proposed for the interconnection of different line topologies and different technologies in [94]. The main challenge of this converter is the series connection of switches.

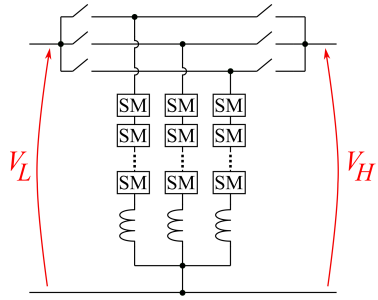


Figure 2.18: Hybrid cascaded dc-dc converter presented in [93].

Double Π

The dc-dc converter double Π has been initially presented in [95, 96] for monopolar interconnections. The bipolar converter is proposed in [97] (see Fig. 2.19), which can be adapted to the interconnections between different line topologies as presented in [94]. The main drawback of this converter is the existing voltage ripple on the dc sides, which can lead to the installation of additional filters.

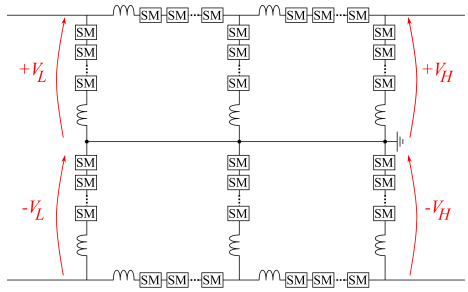


Figure 2.19: Double Π dc-dc converter presented in [95]

2.5 Multi-port converters

A new family of converter topologies has emerged in recent years denominated the multi-port converters. These converters are designed to interconnect multiple lines or systems. The multi-port converters can be designed as dc-dc, dc-ac, or ac-ac converters. The multi-port dc-dc converters can be also divided into isolated [98–102] and non-isolated converters [83, 103, 104]. The isolated multi-port converters could have complicated converter and transformer arrangements. Compared to the F2F these converters continue to use intermediary ac transformers that can be of high volume and cost. The non-isolated multi-port converters can reduce their volume, compared to the F2F but, they have complex control strategies. Furthermore, the dc-dc interconnections are mostly based between lines of the same topology, e.g. interconnecting multiple AM lines with different voltage ratings [83, 100, 103]. Due to their complexity, these converters are not considered in this thesis.

2.6 Topologies comparison

The dc-dc converters for HVDC applications proposed in the literature were presented in this chapter. The F2F is the most direct solution to implement a dc-dc converter for heterogeneous interconnections. The ac

transformer employed in the F2F allows the interconnection between two systems with different voltages, line topologies and/or technologies. The F2F-MMC proposes the use of the well-known MMC, which increases the adaptability of the dc-dc converter for different applications. However, the F2F has an increased volume as it has to convert the complete transferred dc power into ac and back to dc using the transformer and two full rated ac-dc converters.

The non-isolated converters are recommended for low to medium voltage ratio applications (see (1.1)), i.e. below a voltage ratio of 5. Without the ac transformer, the voltages are withstood with the semiconductor devices. The dc-dc converters need to have a series connection of switches or SMs to achieve the rated voltages. The series connection of SMs can be easily compared to the series connection of switches, which reduce the design and operation requirements. In the present thesis, the converters using a series connection of SMs have increased interest. The non-isolated converters can be adapted to the interconnection with different line topologies and different technologies, which remain interesting for the study of this thesis.

A general comparison between the main dc-dc converters found in the literature, is presented in Table 2.1 with their general advantages and drawbacks.

From the isolated dc-dc converters, the F2F-MMC is used in this thesis as the reference converter (see Fig. 2.1). The F2F-MMC uses elements with high technological maturity (MMC and ac transformer as shown in Fig. 2.8 and 2.9). This converter could be implemented with the current know-how from the ac applications. The other dc-dc converters can be compared to the F2F to determine their interest.

From the different non-isolated converters explored in the literature, the dc-MMC (see Fig. 2.13 and 2.14) stands out due to the expected reduction in volume and number of components compared to the F2F. The dc-MMC has a single dc-dc stage of conversion without using an ac transformer. Additionally, due its similarity to the ac-dc MMC (see Fig. 2.1), the dc-MMC can develop its industrialization faster than other converters. Some of the non-isolated converters have a series connection of switches or transformers with dc offsets (Fig. 2.10, 2.18), increasing the converter volume and design requirements.

<table>
<tr><th rowspan="2">Converter</th><th colspan="3">Different</th><th rowspan="2">Additional Comments</th></tr>
<tr><th>Voltage</th><th>Line Topology</th><th>Technology</th></tr>
<tr><td>Cascaded Multi-converter (Fig. 2.7)</td><td colspan="3" rowspan="6">The transformer can adapt the voltage ratio and grounding scheme differences. FBSMs are needed for a controlled voltage reversal. These converters have an important volume as they use two full rated ac-dc converters and an ac transformer. The general structures are presented in Fig. 2.8 and 2.9.</td><td>High transformer insulation requirements</td></tr>
<tr><td>F2F-MMC (Fig. 2.1)</td><td>–</td></tr>
<tr><td>F2F-AAC (Fig. 2.3)</td><td>Series connection of switches. Possible ac and dc filters needed.</td></tr>
<tr><td>F2F-SBC (Fig. 2.4)</td><td>Series connection of switches</td></tr>
<tr><td>F2F-AFCB (Fig. 2.5)</td><td>Ac harmonics</td></tr>
<tr><td>F2F-unidirectional (Fig. 2.6)</td><td>Power reversal not possible.</td></tr>
<tr><td>Non-isolated F2F (Fig. 2.12)</td><td rowspan="9">Recommended for low to medium voltage ratios [7], i.e. voltage ratios below 5</td><td>Voltage insulation requirements</td><td rowspan="7">FBSMs needed for the voltage polarity change</td><td>Resonances can increase the stress in the switches</td></tr>
<tr><td>Auto-transformer (Fig. 2.10)</td><td rowspan="2">Reconfiguration presented in [58]</td><td>Ac transformer with dc offset</td></tr>
<tr><td>Transformer-less auto-transformer (Fig. 2.11)</td><td>Resonances</td></tr>
<tr><td>dc-MMC (Fig. 2.13 and 2.14)</td><td>Reconfiguration presented in [87]</td><td>–</td></tr>
<tr><td>Hybrid cascaded (Fig. 2.18)</td><td>Reconfiguration presented in [94]</td><td>Series connection of switches</td></tr>
<tr><td>Buck-boost (Fig. 2.17)</td><td rowspan="3">Circuit reconfiguration needed</td></tr>
<tr><td>Double Π (Fig. 2.19)</td><td rowspan="2">Voltage polarity change hard to achieve</td><td>–</td></tr>
<tr><td>Double Wye (Fig. 2.15)</td><td>–</td></tr>
</table>

Table 2.1: Summary of dc-dc converters for HVDC heterogeneous interconnections.

2.7 Conclusions

The dc-dc converters for HVDC applications are a subject of high research interest. The converters proposed in the literature can be classified as isolated or non-isolated converters. The most common structure proposed for the isolated converters is the front-to-front (F2F) configuration. It is composed of two full-rated ac-dc converters and a full-rated ac transformer. The F2F-MMC is the most obvious solution for the heterogeneous interconnection as it uses the state-of-the-art components and operation principles. For this reason, the F2F-MMC is chosen as the reference converter. The F2F-MMC is studied in detail in Chapter 5.

On the other hand, the non-isolated converters are proposed to decrease the total volume compared to the F2F by reducing the number of components and, for some structures, avoiding the use of ac transformers. These improvements are obtained by sacrificing the galvanic isolation. Therefore, the non-isolated topologies are recommended for low to medium voltage ratio applications. From the non-isolated converters, the dc-MMC was chosen as a candidate to be compared with F2F-MMC. Topologies like the auto-transformer (AT) and transformerless AT are also of high interest but, these topologies employs two ac-dc converters and ac transformer with especial design requirements, probably increasing the volume compared to the dc-MMC. The dc-MMC has a single dc-dc conversion stage without series connection of switches or ac transformers which can reduce the volume of the converter compared to the F2F. In addition, the dc-MMC is topologically similar to the MMC which could promote its industrialization. The dc-MMC for heterogeneous interconnection (the flexible dc-MMC) is studied in detail in Chapter 6.

Based on the analysis of the flexible dc-MMC, a new topology is proposed and added to the set of converters to be compared. The new topology is called the asymmetric dc-dc converter (ADCC) and it is studied in detail in Chapter 7.

The methodology used to analyze the modular converters is presented in the next chapter. The methodology is applied to the three aforementioned converters.

Chapter 3

General Modelling, Sizing and Control Design Approach

3.1 Introduction

This chapter explains the general approach used in this thesis to obtain the mathematical model, have a preliminary sizing of the passive components and design a simplified control strategy of the dc-dc converters analyzed in Chapters 5, 6, and 7. This methodology can be used for modular HVDC converters, where a modular converter is understood as a converter using stacks composed of a series connection of SMs.

The proposed process allows to understand the converter and its basic requirements not only for the steady-state operation but, also for the fault and post-fault scenarios. The passive components, i.e. the number of sub-modules (SMs) per arm, the capacitors in the SMs and the circuit inductors are sized based on the converter analysis.

Based on the mathematical model, a generalized control design is proposed. The control design can be applied to modular converters. The control strategy aims to use simple controllers such as proportional-integral (PI) controllers which are easy to tune and implement in simulation models.

The general flow chart explaining the methodology to obtain a converter model is presented in Fig. 3.1. The modeling hypotheses are presented in Section 3.2, the mathematical model is presented in Section 3.3, the diagonalization in Section 3.6.1, the steady-state analysis is presented in Section 3.5, the sizing is presented in Section 3.5, and the control strategy is presented in Section 3.6. The simulation validations are presented in Chapters 5, 6, and 7 for the three different dc-dc converters considered in this thesis.

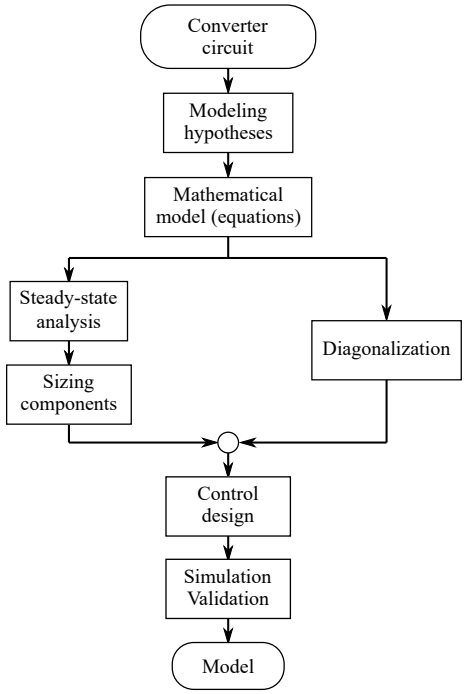


Figure 3.1: General flow chart indicating the principal process used in this thesis.

3.2 Modeling hypotheses

Modular converters for HVDC applications have a large number of components (in the order of a thousand of elements per arm), including switches, inductors, and capacitors. The interactions between all the elements are complex and vary in time depending on the operation point. Detailed mathematical modeling includes the individual states of all the components, such as the voltages on the SM capacitors, the state of the switches (on/off), and the currents in the inductors.

3.2.1 Equivalent arm voltage

To simplify the mathematical modeling, a widely accepted simplification is to reduce the stack model into an equivalent voltage source, as presented in Fig. 3.2, which represents the voltage inserted by the SMs in the stack. The simplification allows to have a model with only the state variables linked to the circuit inductors, i.e. the arm currents, neglecting the voltage in the capacitors.

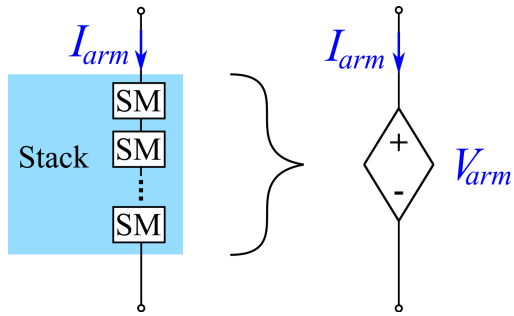


Figure 3.2: Equivalent arm voltage used for the mathematical modeling.

This model neglects the discontinuities dues to the switching events and the differences between the voltages in the SMs. The model is ideal to evaluate the aggregated behavior of the SM stack. Additionally, the equivalent arm voltage facilitates the derivation of analytical models, as it represents the converter model with a reduced number of state variables.

3.2.2 Average arm model

As presented in Fig. 3.1, part of the modeling strategy is to validate the results and hypotheses with simulation models. However, detailed converter models could require extended calculation efforts. The simulation models for the HVDC converters can vary in complexity and simulation efforts. Depending on the objective of the study, a more or less detailed model should be used. The CIGRÉ working group B4.57 has published a guide to implement simulation models for HVDC converters [105]. The generalities of the 7 types of models, proposed by this working group, are presented in table 3.1.

For this thesis, the behavior of the individual components (switches) is not needed thus, a model type 5 is enough to represent the converter [105, 106]. The converter can be modeled with the average-arm model (AAM), which is a type 5 model that can effectively reduce the simulation time, conserving the dynamics needed to test the converter outer control, i.e. power, voltage, energy, and current controllers. The inner control, i.e. voltage balancing between the SMs in a stack, is not considered at this stage. But, the AAM assumes an ideal low level control ensuring the insertion or bypass of the individual SMsin the arm.

The AAM have been used for the MMC modeling in [107, 108] and validated with experimental results in [109].

Different types of AAM can be found in the literature [110–114], a simplified AAM is presented in Fig. 3.3a, which can be used for an arm composed of any type of SM, but it does not emulate the blocked state.

The blocked state represents the case where none of the IGBTs of the SMs in the arm is activated. Then, the equivalent capacitor is inserted in the circuit through the freewheeling diodes, depending on the current direction. The blocked state is useful to simulate faults, converter start-up sequences and, in general, to verify the charging and discharging of the SMs in the blocked state.

Table 3.1: Types of simulation models, extracted from [105].

Model	Description
Type 1	Full Physics Based Models - switches and diodes are represented by differential equations.
Type 2	Full Detailed Models - models based on simplified nonlinear IGBT models.
Type 3	Models based on simplified switchable resistances - IGBT and diodes are represented by two-value resistors.
Type 4	Detailed Equivalent Circuit Models - this type of models is based on Type 3 but uses a computationaly more efficient solution method.
Type 5	Average Value Models based on switching functions - the ac and dc side characteristics are modeled as controlled current and voltage sources with harmonic content.
Type 6	Simplified Average Value Models - The ac and dc side characteristics are modeled as controlled current and voltage sources (phasor domain).
Type 7	RMS Load-Flow Models – steady-state.

Figure 3.3b shows an AAM for the arms composed of HBSMs, including the blocked state modelling as proposed in [110, 115, 116]. Fig. 3.3c shows an AAM for arms composed of FBSMs including the blocked state [111]. The term m_{ctrl} is the modulation index calculated by indirect modulation [106, 117], as follows:

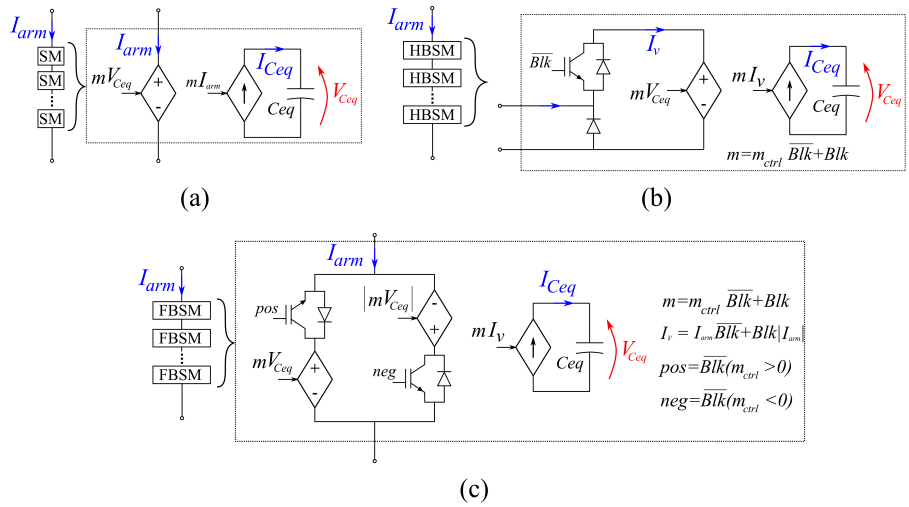


Figure 3.3: Average arm models. Simplified general model (a). For half bridge SMs (HBSMs) with blocked state [110] (b). For full bridge SMs (FBSMs) with blocked state [111] (c).

$$m_{ctrl}(t) = \frac{V_{arm}^{ref}(t)}{V_{C_{eq}}(t)} \tag{3.1}$$

where V_{arm}^{ref} is the equivalent voltage to be generated by the stack of SMs, which is calculated by the converter controller, C_{eq} is the equivalent arm capacitance $\frac{C_{SM}}{N_{SM}}$, where C_{SM} is the capacitance of an individual SM and N_{SM} is the number of SMs in the arm, and Blk is the blocking signal, 0 for unblocked state, and 1 for blocked state. The upper bar in $\overline{Blk}$ represent the logical operator NOT. The models and their associated logic are designed to have $m = 1$ in the blocked state, i.e. the total voltage $V_{C_{eq}}$ is inserted depending on the arm current. The detailed operation of the AAMs can be found in [106, 110, 111].

This thesis uses the AAMs presented in Fig. 3.3b and Fig. 3.3c to simulate the F2F-MMC, the flexible dc-MMC, and ADCC in Chapters 5, 6, and 7 respectively. In the case of a mixed arm, consisting of HBSMs and FBSMs, a series connection of the two models is used. The modulation index is assumed to be equal for both type of SMs in the arm, when positive modulation is required ($m_{ctrl} > 0$). When the modulation calculated by the converter control is negative ($m_{ctrl} < 0$), only the FBSMs are inserted. The model controls the total energy of the two models (HB

plus FB) assuming that a low level control manage the voltage variations between the SMs (HB and FB), and that the number of FBSMs is enough to create the negative part of the voltage reference.

3.3 Mathematical Modeling

Using the equivalent arm voltage, the range of the system is reduced by neglecting the individual voltages of the C_{SM} or the accumulated voltage $V_{C_{eq}}$. The model depends only on the arm currents and voltages. A more complete mathematical model can include the capacitor dynamics as the AAM but, for the aim of this study the equivalent arm voltage is sufficient. Additional hypotheses considered for the mathematical model are listed below.

1. The electrical variables (voltages and currents) are balanced between the converter legs.
2. The analysis is realized for one leg, but it can be expanded to n legs.
3. The dc systems are free of ac components.
4. Only the dc and the fundamental ac component (first harmonic) waveforms are considered.
5. The dc voltages are separated into their equivalent pole-to-ground voltages as shown in Fig 3.4. The dc system voltages are considered to be constant and balanced during steady-state operation, e.g. $V_1^{dc} = V_2^{dc}$ for a symmetrical monopole.

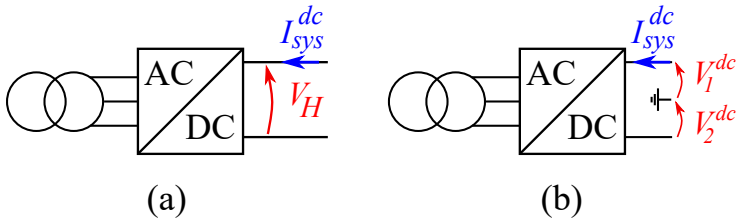


Figure 3.4: (a) pole-to-pole dc voltage. (b) pole-to-ground dc voltages, where $V_H = V_1^{dc} + V_2^{dc}$.

The mathematical model is the system of equations that describes the converter arm current dynamics. The general structure can be organized into a matrix from as follows:

$$\boldsymbol{L}\frac{d}{dt}\boldsymbol{I_{arm}} = \boldsymbol{R}\,\boldsymbol{I_{arm}} + \boldsymbol{V_c}\,\boldsymbol{V_{arm}} + \boldsymbol{K_V}\,\boldsymbol{V_k} \tag{3.2}$$

where $\boldsymbol{L}$ is the matrix containing the converter inductances, $\boldsymbol{I_{arm}}$ is the vector containing the independent currents per leg, $\boldsymbol{R}$ is a matrix containing the converter resistances. $\boldsymbol{V_c}$ and $\boldsymbol{K_V}$ are constant matrices relating the $\boldsymbol{V_{arm}}$ vector and $\boldsymbol{V_k}$, which is the vector containing the dc system voltages, e.g. V_1^{dc} and V_2^{dc}.

The dimension of the matrices and vectors depends on the number of independent currents per leg. For a system with n variables, the vectors of (3.2) can be generalized as:

$$\boldsymbol{I_{arm}} = \begin{bmatrix} I_{arm_1} & I_{arm_2} & \cdots & I_{arm_n} \end{bmatrix}^T \tag{3.3}$$

$$\boldsymbol{V_{arm}} = \begin{bmatrix} V_{arm_1} & V_{arm_2} & \cdots & V_{arm_n} \end{bmatrix}^T \tag{3.4}$$

$$\boldsymbol{V_k} = \begin{bmatrix} V_1^{dc} & V_1^{ac} & V_2^{dc} & V_2^{ac} & \cdots & V_{N_{ac}}^{dc} & V_{N_{dc}}^{ac} \end{bmatrix}^T \tag{3.5}$$

where N_{dc} is the number of system dc voltages and N_{ac} is the number of system ac voltages. These vectors depends on each converter topology. The matrices in (3.2), are considered as $n \times n$ square matrices, except for $\boldsymbol{K_V}$ which is a $n \times (N_{dc} + N_{ac})$ matrix.

To clarify some of the definitions used in the methodology, the modeling of the ac-dc MMC is presented as example.

Figure 3.5a presents the MMC circuit model composed of three legs and each leg composed of two arms, which in turn are composed of an inductor and a SM stack. The single leg model is presented in Fig. 3.5b, where the system dc current, I_{sys}^{dc}, is divided equally between the converter legs. The single leg model also shows the ac current, I_{int}^{ac}, that circulates inside the converter but not into the dc system.

Based on the single leg model and (3.2), the mathematical model describing the MMC is:

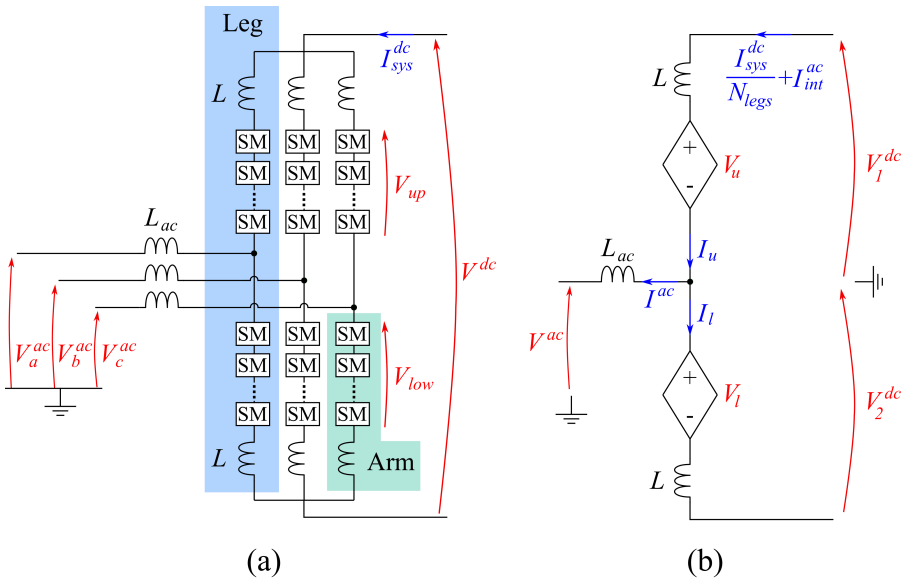


Figure 3.5: Modular multi-level converter. (a) three-phase circuit. (b) single-phase circuit used for the mathematical modeling.

$$\begin{bmatrix} L+L_{ac} & -L_{ac} \\ -L_{ac} & L+L_{ac} \end{bmatrix} \begin{bmatrix} \dot{I}_u \\ \dot{I}_l \end{bmatrix} = \begin{bmatrix} -(R+R_{ac}) & R_{ac} \\ R_{ac} & -(R+R_{ac}) \end{bmatrix} \begin{bmatrix} I_u \\ I_l \end{bmatrix} - \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} V_u \\ V_l \end{bmatrix} + \begin{bmatrix} 1 & 0 & -1 \\ 0 & 1 & 1 \end{bmatrix} \begin{bmatrix} V_1^{dc} \\ V_2^{dc} \\ V^{ac} \end{bmatrix} \quad (3.6)$$

For this specific example, there are two state variables I_u, and I_l; $\boldsymbol{I_{arm}}$, and $\boldsymbol{V_{arm}}$ are 2×1 matrices. The considered MMC has two system dc voltages V_1^{dc}, and V_2^{dc}, and one ac voltage contained in V_k. Thus, $N_{dc} = 2$, and $N_{ac} = 1$. The matrix K_V is a 2×3 matrix.

3.4 Steady-State Analysis

The previous section has shown the mathematical modeling, the steady-state analysis is presented in this section to understand the converter operation. The principal objective in this section is to check if the converter can operate maintaining balanced its energy.

3.4.1 Energy balance

Modular converters stored energy in the capacitors of the SMs. The converter control must keep this energy within operational limits, which requires having the capacitor voltages controlled. If the voltage on the capacitors increases above the physical limits of the semi-conductors, the switches in the SMs can be damaged. On the other hand, reducing the voltage in the capacitors may lead to uncontrollable currents in the converter, because the arm will be incapable of generating the needed voltage equivalent to have $|m_{ctrl}| > 1$.

To keep the stability in a lossless converter, the average value of the energy must be controlled to be constant in steady-state conditions. This can be represented by the following equation:

$$\left\langle \frac{d}{dt} E_{converter} \right\rangle = 0 \tag{3.7}$$

where $E_{converter}$ is the total energy of the converter.

The variation of the energy over the time is a power thus, (3.7) can be expressed in terms of the input and output power:

$$\left\langle \frac{d}{dt} E_{converter} \right\rangle = P_{in} + P_{out} = 0 \tag{3.8}$$

where P_{in} and P_{out} are the total input and output powers.

This is equivalent to say that, in steady-state conditions, the input power should be equal in magnitude and opposite in sign to the output power (neglecting the converter losses).

The energy balance can be applied to individual legs or arms. The analysis can be directly in terms of the stored energy or through the power analysis. The following subsections analyze the energy equilibrium by estimating the power balance starting with the dc steady-state.

3.4.2 Dc steady-state analysis

The dc steady-state analysis is used to verify the converter dc operating conditions. The steady-state depends on the transmitted power and the system dc voltages. It is worth reminding that the dc steady-state does not consider the ac voltages or dynamic variations and, for this analysis, the dc voltage drop in the arm inductances is neglected, i.e. an inductor resistance equal to zero.

The arm dc currents can be defined in terms of the system dc currents I_{sys}^{dc} (see Fig. 3.4). The system currents depend on the system dc voltages, V_1^{dc} and V_2^{dc} in Fig. 3.4, and the power transferred through the modular converter, as follows:

$$I_{sys_i}^{dc} = \frac{P_T^{dc}}{V_{eq}^{dc}} \tag{3.9}$$

where P_T^{dc} is the transmitted power and V_{eq}^{dc} is the equivalent system dc voltage (V_H in Fig. 3.4a). $I_{sys_i}^{dc}$ is the i^{th} current for $i \in [1, N_I]$ (N_I the number of system dc currents).

The number of system dc currents and voltages depends on the converter topology. An ac-dc converter might have only one system dc current, while a dc-dc converter has at least two (input and output dc current). V_{eq}^{dc} are voltages set by the system, normally the pole-to-pole voltages. The V_{eq}^{dc} voltages are included in the voltage vector $\boldsymbol{V_K}$ (3.5), as one or a combination of multiple elements.

Then, the arm dc currents can be approximated with the following expression:

$$\boldsymbol{I}_{arm}^{dc} = \boldsymbol{K}_{I_{sys}} \boldsymbol{I}_{sys}^{dc} \tag{3.10}$$

where $\boldsymbol{K}_{I_{sys}}$ is a matrix $n \times N_I$, with n the number of state variables, i.e. independent arm currents, and N_I is the number of system dc currents. The matrix $\boldsymbol{K}_{I_{sys}}$ is defined by inspection depending on the modular converter topology.

From the mathematical model (3.2), the converter dc steady-state can be found by replacing the arm current variation $\frac{d}{dt}\boldsymbol{I_{arm}} = 0$ (left hand of (3.2)), as follows:

$$0 = \boldsymbol{R}\,\boldsymbol{I}_{arm}^{dc} + \boldsymbol{V_c}\,\boldsymbol{V}_{arm}^{dc} + \boldsymbol{K_V}\,\boldsymbol{V_k}^{dc} \tag{3.11}$$

where $\boldsymbol{V_k^{dc}}$ contains only the system dc voltages, replacing the system ac voltages by zeros.

Using (3.10) and (3.11), the arm dc voltages (V_{arm}^{dc}) can be found, but an accepted simplification is to neglect the voltage drop on the circuit resistances (normally small with respect to the rest of the voltages). In this case, the arm dc voltages depend only on the system dc voltages contained in $\boldsymbol{V_k^{dc}}$, as follows:

$$0 = \boldsymbol{V_c}\,\boldsymbol{V}_{arm}^{dc} + \boldsymbol{K_V}\,\boldsymbol{V_k}^{dc}$$

$$\boldsymbol{V}_{arm}^{dc} = -\boldsymbol{V_c}^{-1}\boldsymbol{K_V}\,\boldsymbol{V_k^{dc}}. \tag{3.12}$$

Applying the dc steady-state analysis for the MMC presented in Fig. 3.5, can lead to the arm dc voltages and currents. The considered MMC has only one system dc current, it can be defined depending on the transmitted power and the pole-to-pole voltage as follows:

$$I_{MMC}^{dc} = \frac{P_T^{dc}}{V_1^{dc} + V_2^{dc}} \tag{3.13}$$

Following (3.10), the matrix $K_{I_{sys}}$ is a 2×1 matrix. The dc arm currents are:

$$I_{arm_{MMC}}^{dc} = \begin{bmatrix} 1/N_{legs} \\ 1/N_{legs} \end{bmatrix} \frac{P_T^{dc}}{V_1^{dc} + V_2^{dc}} \tag{3.14}$$

where N_{legs} is the number of legs of the converter.

Using (3.6) in (3.12), and changing the ac voltage by zero (because only the dc values are needed), the dc steady-state voltage in the arms correspond to:

$$V_{arm_{MMC}}^{dc} = \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix}^{-1} \begin{bmatrix} 1 & 0 & -1 \\ 0 & 1 & 1 \end{bmatrix} \begin{bmatrix} V_1^{dc} \\ V_2^{dc} \\ 0 \end{bmatrix} = \begin{bmatrix} V_1^{dc} \\ V_2^{dc} \end{bmatrix} \tag{3.15}$$

which meas that each arm operates at a dc voltage equivalent to the pole-to-ground voltage of the dc system.

3.4.3 Dc power balance

Based on the arm dc current (3.10) and arm dc voltage (3.12), the arm dc power can be calculated. The general expression is expressed as:

$$P_{arm}^{dc} = I_{arm}^{dc} V_{arm}^{dc}. \tag{3.16}$$

Assuming that neither I_{arm}^{dc} nor V_{arm}^{dc} are zero, the dc power in the arm has a no-null value. Using the AAM presented in Fig. 3.3a with positive I_{arm} and m, it can be evidenced that a positive current $I_{C_{eq}}$ charges the capacitor C_{eq}, i.e. increasing $V_{C_{eq}}$. A similar analysis can be done for negative powers e.g. with negative I_{arm} and positive m, which discharges C_{eq}. The continuous arm charge or discharge may result in either an insufficient stored voltage to generate V_{arm} or the overvoltage of C_{eq}.

As the capacitor C_{eq} is the main storage element, a variation in its voltage is equivalent to a variation of its energy. The energy in the equivalent arm can be expressed as follows:

$$E_{arm} = \frac{1}{2} C_{eq} V_{C_{eq}}^2 \tag{3.17}$$

and its dynamic variation:

$$\frac{d}{dt} E_{arm}(t) = C_{eq} V_{C_{eq}}(t) \frac{d}{dt} V_{C_{eq}}(t) \tag{3.18}$$

From the AAM (see Fig. 3.3), the arm current and voltage can be expressed depending on the modulation index m as:

$$V_{arm}(t) = m(t)\ V_{C_{eq}}(t) \tag{3.19}$$

$$I_{C_{eq}}(t) = m(t)\, I_{arm}(t) \tag{3.20}$$

$$I_{C_{eq}}(t) = C_{eq} \frac{d}{dt} V_{C_{eq}}(t) \tag{3.21}$$

Combining (3.19), (3.20) and (3.21), (3.18) can be simplified as follows:

$$\begin{aligned} \frac{d}{dt} E_{arm}(t) &= I_{C_{eq}}(t)\, V_{C_{eq}}(t) \\ &= m(t)\ I_{arm}(t)\ \frac{V_{arm}(t)}{m(t)} \\ &= I_{arm}(t)\ V_{arm}(t) \end{aligned}$$

$$\frac{d}{dt} E_{arm}(t) = P_{arm}(t) \tag{3.22}$$

As presented in (3.8), the energy in the converter (or the arm in this case), (3.22), should have an average value of zero. From expression (3.16) it has been found that the arms exchange dc power, which has an non-null average value. To balance the energy in the arms, an additional ac power should be generated. The ac power should have the same magnitude of P_{arm}^{ac} but, opposite sign to respect (3.8). To generate the ac power, additional ac voltage need to be superposed to the dc voltages calculated previously. In general, the ac power circulates inside the converter to avoid ac components on the dc systems. However, the modular converters can have ac outputs to exchange ac power. The power balance

in the arm is defined as:

$$\frac{1}{T}\int_{t_0}^{t_0+T}\left(P_{arm}^{dc}(t)+P_{arm}^{ac}(t)\right)dt=\langle P_{arm}\rangle=0 \tag{3.23}$$

where t_0 is the initial time of integration and T is the fundamental period of operation of the converter.

In consequence, the sum of the power in all the arms in a leg should be:

$$\sum_{i=1}^{g}\langle P_{arm_i}\rangle=0 \tag{3.24}$$

where g is the number of arms per leg.

Dc power balance in dc-dc converters

In dc-dc modular converters, the ac power is used to keep the converter energy controlled, but this power circulates inside the converter [80]. The circulating ac power acts as an energy carrier, which takes the excess of energy from the arms charged by the dc power and sends it to those discharged by the dc power. Additional to (3.24), the following expression can be used to evaluate the converter energy balance capability:

$$\sum_{i=1}^{g}P_{arm_i}^{dc}=0 \tag{3.25}$$

Expression (3.25) means that the dc power generated by some arms should be absorbed by other arms. If (3.25) is not respected, i.e. there is a surplus or a lack of energy to balance the converter, an external energy source is needed to exchange the ac power, e.g. a connection to an ac grid.

3.4.4 Ac steady-state analysis

To have ac power in the arms, the voltages and currents should have an alternative component, as follows:

$$I_{arm}(t)=I_{arm}^{dc}+I_{arm}^{ac}\cos\left(\omega\,t+\theta_{Iarm}\right) \tag{3.26}$$

$$V_{arm}(t)=V_{arm}^{dc}+V_{arm}^{ac}\cos\left(\omega\,t+\theta_{Varm}\right) \tag{3.27}$$

where I_{arm}^{ac} and V_{arm}^{ac} are the arm current and voltage magnitudes, and ω is the operating frequency of the converter in rad/s. As stated in the modeling hypothesis (see Section 3.3), only the first harmonic is considered.

Using (3.23), (3.24), (3.26) and (3.27) the general power equilibrium is expressed as:

$$\begin{aligned} P_{arm}(t) = \; & I_{arm}^{dc} V_{arm}^{dc} \\ & + I_{arm}^{ac} V_{arm}^{ac} \cos(\omega t + \theta_{I_{arm}}) \cos(\omega t + \theta_{V_{arm}}) \\ & + I_{arm}^{dc} V_{arm}^{ac} \cos(\omega t + \theta_{V_{arm}}) \\ & + I_{arm}^{ac} V_{arm}^{dc} \cos(\omega t + \theta_{I_{arm}}) \end{aligned} \tag{3.28}$$

where the average value is:

$$\begin{aligned} P_{arm}^{dc} &= -P_{arm}^{ac} \\ V_{arm}^{dc} I_{arm}^{dc} &= -V_{arm_{RMS}}^{ac} I_{arm_{RMS}}^{ac} \cos(\theta_{Varm} - \theta_{Iarm}) \end{aligned} \tag{3.29}$$

To respect the power balance defined in (3.25), the average value of the energy should be controlled. As the energy dynamic variation of the energy is linked to the power, controlling the average power in the arms, (3.29), can guarantee the energy balance.

The steady-state arm ac currents and voltages can be found solving the circuit equations (3.2), in phasor domain, respecting the power restriction (3.29). The ac analysis can be developed analytically for the converters with simple structures, e.g. having only two arms per leg. For a more complex converter, e.g. with three or more arms per leg, an optimization problem is suggested in this thesis.

The optimization problem has the same initial restrictions as the analytical analysis, but additional restrictions can be taken into account, such as the maximum number of SMs in the arms, the presence of FB-SMs, and reactive power inside the converter. Based on these restrictions, the objective function can be set to reduce the conduction losses in the arms. The solution found, sets an ac operation point that should be reached by the control strategy.

The restrictions can vary depending on the converter. Thus, this detailed analysis is developed in the chapters dedicated to the dc-dc converters (chapters 5, 6, and 7).

3.5 Preliminary converter sizing

3.5.1 Number of sub-modules per arm

In modular converters, the number of SMs per arm is defined by three main constraints: the switches rated voltage, which determines the operating voltage of the SMs, the maximum arm voltage given by the steady-state analysis and the fault blocking capability (FBC). Some ac transients can also impact the number of SMs but, as the ac systems are internal to the dc-dc converters, i.e. decoupled of the ac transmission system, the ac impact on the converter sizing is neglected.

The switches used in the SMs determine V_{SM}, the operating voltage of C_{SM}. V_{SM} is used to calculate the number of SMs per arm depending on the maximum arm voltage to be generated. As explained in the previous section, modular converters operate with a superposition of dc and ac voltages. The maximum peak voltage (dc value plus ac peak value) in an arm (V_{arm}^{max}), determines the minimum required number of SMs, N_{SM}^{min}, as follows:

$$N_{SM}^{min} = \frac{V_{arm}^{max}}{V_{SM}}. \tag{3.30}$$

The third restriction is related to the cases where the converter is subject to faults. In these cases, the converter must withstand the imposed voltages and ensure the security of the healthy protection zones, if fault blocking capability is assumed, see Section 1.6. Depending on the converter and the interconnected systems, the fault scenarios can increase the number of SMs needed in one or multiple arms in a leg. In the situations where the arm must withstand negative voltages, the use of FBSMs could be necessary, e.g. when a fault on the high voltage side of the dc-MMC (see Fig. 2.13) occurs, the upper arm withstands a negative voltage. The FBC can be achieved with a dc circuit breaker (DCCB) or by adding FBSMs. In this thesis only the FBC with FBSMs is studied.

Additionally to the presented restrictions, supplementary SMs are installed in modular converters to ensure the converter availability between maintenance periods [118, 119]. The percentage of redundant SMs can vary depending on the used semiconductors, the required availability, and the time between maintenance interventions. Reference [118] has found a redundancy required between 4% and 20% changing the maintenance interval from 1 to 8 years, for an offshore application. In this thesis, the redundant number of SMs is not taken into account as the simulations do not emulate the SMs failure or the semiconductor switches lifetime estimation [120].

3.5.2 Circuit inductors

The circuit inductors are needed to reduce the magnitude of the circulating currents, limit the high-frequency components in the current, enable the smooth current control, and to reduce the slope of the dc fault currents [112, 119]. The arm inductor may have a value between 0.05 p.u. (for filtering purposes) and 0.2 p.u. (for fault current limitation) [112, 119] depending on the main converter constraints. The arm inductors should be sized as small as possible to reduce the reactive power consumed by these elements but, big enough to respect the aforementioned conditions.

In this thesis, the circulating current and resonance issues are put aside to focus on the approximated inductor sizing based on the dc fault currents. Two simplified approaches are considered, described below.

Use the recommended inductance value suggested by the literature

In this case an inductor between 0.15 p.u. and 0.2 p.u. is considered. The arm inductance can be found as:

$$L = Z_{base}\, k_L \tag{3.31}$$

$$L = \frac{V^{ac2}}{S_{base}\, 2\,\pi f} k_L \tag{3.32}$$

where V^{ac} is the RMS system ac voltage, e.g. the voltage at the ac terminals of the MMC, S_{base} is the apparent base power, f is the operating frequency of the ac system, and k_L is the percentage of the base impedance mentioned above, i.e. between 15% and 20%.

This estimated value is proposed for MMCs operating at 50 Hz. Changing the operational frequency can lead to a reduced inductance value. But, it could be insufficient to limit the dc fault current slope if the dc voltage remain unchanged. The approach below takes into account the dc fault current slope to size the arm inductors.

Evaluate the estimated fault slope analytically

Similar to the approach used in [121]. With this approach the circuit equations are used to find the inductors that respect a given di/dt.

From (3.2), the n equations can be used to find the inductances values. Replacing the objective di/dt, $\boldsymbol{I_{arm}}$ and $\boldsymbol{V_{arm}}$ by their steady-state values (the dc operating point found in Section 3.4.2 can be a first ap-

proach), as follows:

$$\boldsymbol{L}\left(\frac{d}{dt}\boldsymbol{I}\right)_{crit} = \boldsymbol{R}\,\boldsymbol{I}_{\boldsymbol{arm}}^{\boldsymbol{dc}} + \boldsymbol{V_c}\,\boldsymbol{V}_{\boldsymbol{arm}}^{\boldsymbol{dc}} + \boldsymbol{K_V}\,\boldsymbol{V_k} \tag{3.33}$$

where $(d/dt\boldsymbol{I})_{crit}$ is the critical fault current slope.

The critical rate of change of the fault current ($(d/dt\boldsymbol{I})_{crit}$) can be fixed based on the maximal di/dt of IGBTs and diodes, the processing time delay, and the maximal current that the IGBTs can open. An estimate range of 3-12 A/µs has been found in [122]. A value of 6.4 A/µs is used in this thesis, which is found using the parameters of INELFE HVDC project, i.e. $V^{dc} = 640$kV and $L_{arm} = 50$mH values [123]. Using these values in the critical slope approximation for a MMC [112], yields to:

$$\frac{d}{dt}I_{crit} \approx \frac{V^{dc}}{2 \cdot L_{arm}} \approx \frac{640\,\mathrm{kV}}{2 \cdot 50\,\mathrm{mH}} \approx 6.4\,\mathrm{A/\mu s} \tag{3.34}$$

In general, the critical fault current slope is found for the dc pole-to-pole fault analysis. For the example of the MMC, it is equivalent to analyze the circuit when V_1^{dc} and V_2^{dc}, in Fig. 3.5, are zero.

3.5.3 Capacitor in the sub-modules

The capacitor in the SMs can be sized using the procedure presented in [106, 124, 125]. The calculation depends on the variation of the energy (ΔW) in a cycle, the accepted SM voltage ripple in p.u. (ϵ), the number of SMs per arm (N_{SM}) and the average voltage per SMs ($\overline{V_{SM}}$). A general flow chart is presented in Fig. 3.6 and the C_{eq} is calculated in (3.35).

$$C_{eq} = \frac{\Delta W}{2\,\epsilon\,\left(N_{SM}\overline{V_{SM}}\right)^2} \tag{3.35}$$

The variation of the energy is calculated from the following expression:

$$\Delta W = \int_{t_0}^{t1} \frac{dW_{C_{eq}}(t)}{dt}\,dt \tag{3.36}$$

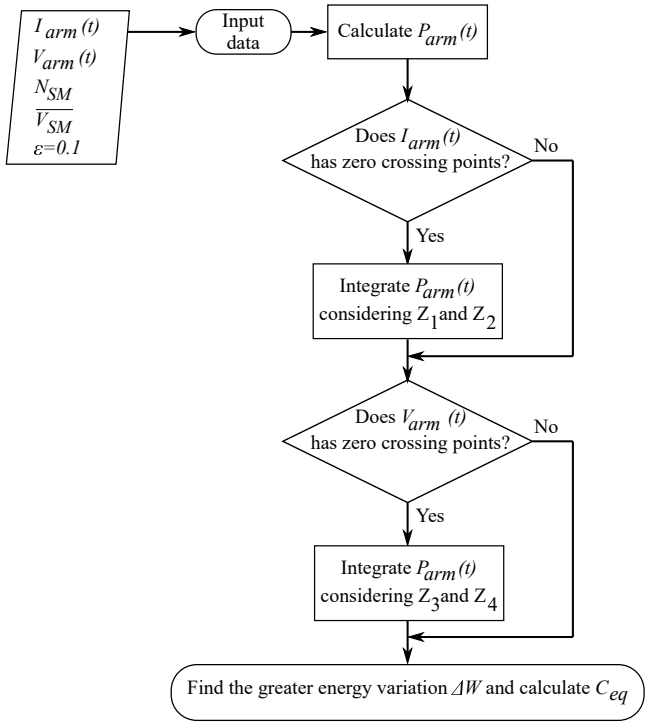


Figure 3.6: Flow chart to calculate C_{eq}. If neither the current nor the voltage have zero crossing points, the equivalent capacitance cannot be calculated with this methodology.

where the limits of the integral (t_0 and t_1) are two adjacent zeros of $dW_{C_{eq}}(t)/dt$. Using (3.23), (3.26), and (3.27), the general integral can be expressed as:

$$\begin{aligned}
\Delta W &= \int P_{arm}(t)\, dt \\
&= \int \left(V_{arm}^{dc} + V_{arm}^{ac}\cos(\omega t + \theta_V)\right)\left(I_{arm}^{dc} + I_{arm}^{ac}\cos(\omega t + \theta_I)\right) dt \\
&= V_{arm}^{dc} I_{arm}^{dc}\, t + \frac{V_{arm}^{ac} I_{arm}^{ac}\cos(\theta_V - \theta_I)}{2}\, t \\
&\quad + \frac{V_{arm}^{dc} I_{arm}^{ac}\sin(\omega t + \theta_I)}{\omega} + \frac{V_{arm}^{ac} I_{arm}^{dc}\sin(\omega t + \theta_V)}{\omega} \\
&\quad + \frac{V_{arm}^{ac} I_{arm}^{ac}\sin(2\omega t + \theta_V + \theta_I)}{4\omega}
\end{aligned} \tag{3.37}$$

The arm power could have the following zero crossing points:

$$Z_1 = \frac{\pi - \arccos\left(\frac{I_{arm}^{dc}}{|I_{arm}^{ac}|}\right) - \theta_{I_{arm}}}{\omega} \tag{3.38}$$

$$Z_2 = \frac{\pi + \arccos\left(\frac{I_{arm}^{dc}}{|I_{arm}^{ac}|}\right) - \theta_{I_{arm}}}{\omega} \tag{3.39}$$

$$Z_3 = \frac{\pi - \arccos\left(\frac{V_{arm}^{dc}}{|V_{arm}^{ac}|}\right) - \theta_{V_{arm}}}{\omega} \tag{3.40}$$

$$Z_4 = \frac{\pi + \arccos\left(\frac{V_{arm}^{dc}}{|V_{arm}^{ac}|}\right) - \theta_{V_{arm}}}{\omega} \tag{3.41}$$

The first two zeros (3.38) and (3.39) correspond to the zeros of the current, while (3.40) and (3.41) are the zeros linked to the voltage. If the arm has only positive modulation, i.e. no negative voltages are generated, only the first two zeros exist.

The literature [106, 124, 125] presents only the first two zeros as the modular converters are designed to use only positive voltage modulation. With the increasing consideration of FBSMs, the possibility for negative modulation needs to take into account the zero crossing point of the arm voltage.

In consequence, to obtain the maximum variation of the energy in a period, the expression (3.36) must be evaluated between all existing zeros and find the maximum variation. A graphical interpretation of the equation is presented in Fig. 3.7 for an example with negative modulation. The maximum energy variation is found with the integrated area A_3.

From (3.37) it can be evidenced that increasing the operating frequency, ω, the energy variation, ΔW is reduced, and the minimal equivalent capacitance found with (3.35), is smaller. Thus, increasing the operating frequency can reduce the capacitance value.

The previous analysis can be used to size the capacitor for the operation at nominal power. For operating points below the rated power, the energy variations are lower. Hence, the capacitor size is not affected by the normal operating conditions.

In contrast, the fault events can charge or discharge the capacitor in the SMs beyond the limits found in the steady-state analysis. During the first instants of the fault event, the current in the arms can increase rapidly, discharging the capacitors in the inserted SMs. Once the con-

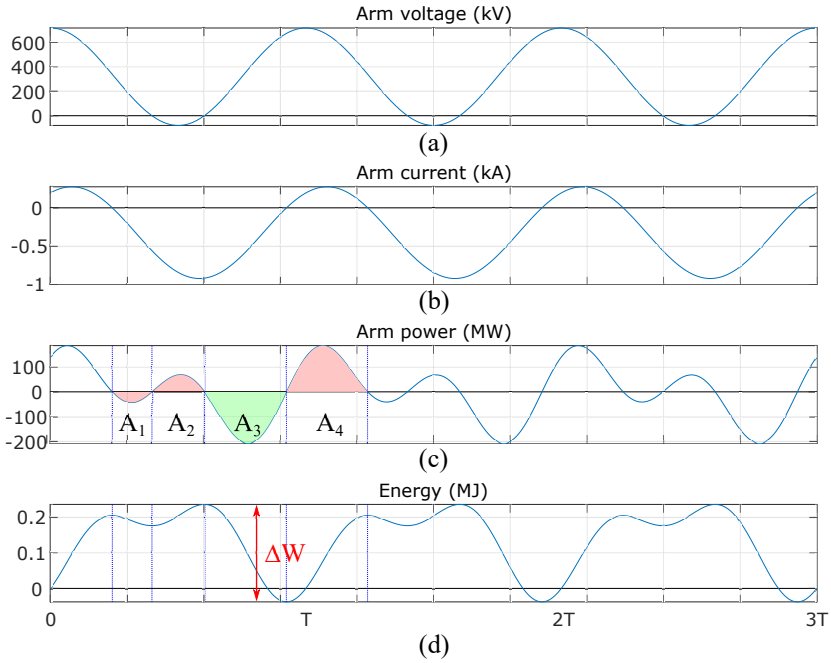


Figure 3.7: Graphical interpretation of expression (3.36). (a) presents the arm voltage with negative modulation. (b) shows the arm current. (c) shows the arm power identifying the zero crossings. (d) presents the energy variation.

verter is blocked, positive currents can charge the capacitors in both HB and FB SMs, while the negative currents only charge the capacitors in the FBSMs. The capacitor discharge could keep the arms from modulate the required voltages. On the other hand, charging the capacitor in the SMs could lead to the overvoltage on the switches which could lead to degradation in the lifetime of the components or even internal faults. The capacitor size can be affected by the fault events. A bigger capacitor could be needed to avoid the large energy variations generated by the faults. These variations depend on the system configuration and control. A system simulation is required to verify the converter behavior. The energy variations are simulated and analysed in Chapters 5, 6, and 7.

3.6 Control Design

Modular converters control is generally divided into two main stages: the lower level control and the upper level control. The former ensures the inserted voltage follows the required arm voltage required by the

high level control by inserting and bypassing the SMs. Several strategies have been used for the low-level control such as pulse-width modulation (PWM), carrier-based modulation, multilevel carrier-based modulation, or balancing capacitor algorithm (BCA) [119, 126].

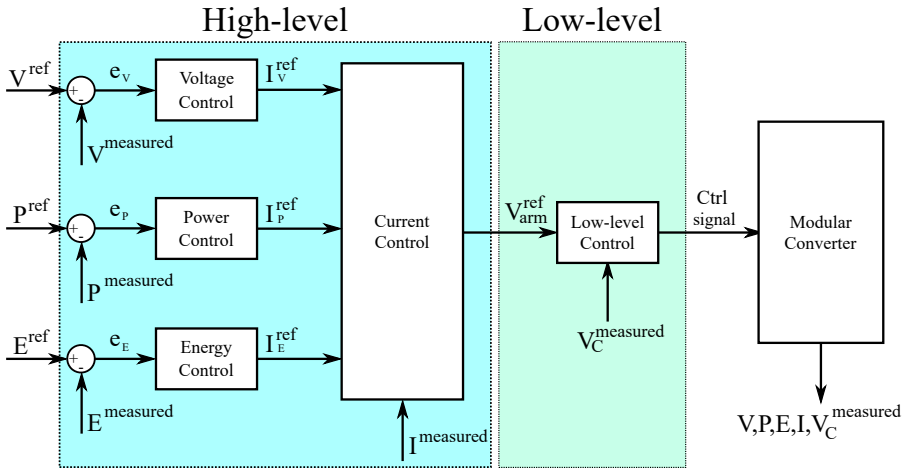


Figure 3.8: Simplified control structure for the modular converters.

The high-level control, used in this thesis, can be subdivided into current and energy control. The energy control keeps the average energy value controlled and sets the reference to the current control. The current control governs the arm currents by setting the arm voltage reference used as an input in the low-level control. Additional controllers can be included at this level such as a power and voltage controller. The general control structure is presented in Fig. 3.8.

This thesis is focused on high-level control. The objective is to design a simple controller to test the converter in a simulation model. Following the hypotheses established for the mathematical model in Section 3.3, the controllers are implemented per leg. The energy and current control design is based on the diagonalization of the system model (3.2), explained below.

3.6.1 System diagonalization

The mathematical model obtained in (3.2) usually defines a non-diagonal system, i.e. the state variables are coupled. The objective of the diagonalization is to decouple the arm currents in a way that each equivalent

current dynamics depends only on itself and on an equivalent voltage. The system diagonalization is achieved by a current, voltage, and energy transformations.

The system diagonalization has been used for the modeling and control of different modular converters such as the MMC [127], or the dc-MMC [80]. The diagonalization of these topologies can be done by the sum and difference transformations (Σ, Δ or sum, $diff$), because the converter has only two state variables per leg: the arm currents. For more complex structures, where the number of state variables increases, the transformations needed to diagonalize the model are not evident. This thesis presents a general methodology to diagonalize a mathematical model describing a modular converter with n state variables. The model follows the equivalent arm voltage simplification from Section 3.2.1, i.e. the voltage in the capacitors are neglected.

The diagonalization allows the use of decoupled, simple controllers such as proportional-integral (PI) controllers. These controllers govern the equivalent variables resulting from the transformations mentioned above (currents, voltages, and energy).

To diagonalize the system, the circuit equations must be first rearranged into the state space canonical form. Then, the procedure presented in [128] can be applied.

The general canonical representation of a state-space system is expressed as:

$$\dot{\boldsymbol{x}} = \boldsymbol{A}\,\boldsymbol{x} + \boldsymbol{B}\,\boldsymbol{u} + \boldsymbol{K_V^{ss}}\,\boldsymbol{V_k} \tag{3.42}$$

where $\boldsymbol{x}$ is the state variable (arm currents), $\boldsymbol{u}$ is the control variable (arm voltages), $\boldsymbol{A}$ is the state matrix, $\boldsymbol{B}$ is the input matrix, $\boldsymbol{K_V^{ss}}$ is a constant matrix that relates the external voltages $\boldsymbol{V_k}$ with the converter. The matrix $\boldsymbol{K_V^{ss}}$ has the same dimensions of $\boldsymbol{K_V}$, i.e. $n \times (N_{dc} + N_{ac})$ (see Section 3.3).

The methodology used in this thesis, assumes that $\boldsymbol{A}$ and $\boldsymbol{B}$ are square matrices $n \times n$ (with n the number of state variables). If this condition is not respected, the model must be adjusted.

Once the system is in the canonical form, the diagonalization of $\boldsymbol{A}$ can be done using a transformation matrix $\boldsymbol{P}$. This diagonalization is a well-know procedure, which is detailed in appendix A. The new diagonal

state matrix, containing the system eigenvalues is expressed as follows:

$$\boldsymbol{A_D} = \boldsymbol{P}^{-1}\boldsymbol{A}\,\boldsymbol{P} = \begin{bmatrix} \lambda_1 & 0 & \cdots & 0 \\ 0 & \lambda_2 & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & \lambda_n \end{bmatrix} \tag{3.43}$$

where λ_n is the n^{th} eigenvalue of the system.

Using the system structure as (3.2), the eigenvalues have a general form as follows:

$$\lambda_i = -\frac{R_{eq_i}}{L_{eq_i}} \tag{3.44}$$

where R_{eq_i} and L_{eq_i} are the equivalent resistance and inductance for each row of $\boldsymbol{A_D}$ ($i \in [1, n]$). Using the transformation matrix $\boldsymbol{P}$ the following relations can be found:

$$\boldsymbol{x} = \boldsymbol{P}\boldsymbol{x'} \tag{3.45}$$

$$\boldsymbol{x'} = \boldsymbol{P^{-1}}\boldsymbol{x} \tag{3.46}$$

The system (3.42) after the diagonalization of the state matrix is expressed as:

$$\boldsymbol{x'} = \boldsymbol{A_D}\,\boldsymbol{x'} + \boldsymbol{B'}\,\boldsymbol{u} + \boldsymbol{K_V^{ss'}}\,\boldsymbol{V_k} \tag{3.47}$$

Contrary to $\boldsymbol{A_D}$, $\boldsymbol{B'}$ could not have a diagonal form. A diagonal $\boldsymbol{B'}$ is needed to have a complete decoupled system. A non-diagonal $\boldsymbol{B'}$ couples the state variables with multiple control variables, decoupling the control variables simplifies the design of a control strategy.

To diagonalize $\boldsymbol{B'}$, a control transformation matrix $\boldsymbol{T}$ is required, such that $\boldsymbol{B'}\,\boldsymbol{T}$ is a diagonal matrix. Unfortunately, there is no general procedure to diagonalize this matrix. If a similar procedure used for the state matrix $\boldsymbol{A}$ is applied, the expression (3.47) will lose its form, and $\boldsymbol{A'}$ will be no longer diagonal. To diagonalize $\boldsymbol{B'}$ this thesis proposes three methods described below.

1. **By inspection:** this method defines the elements of $\boldsymbol{T}$ to have the non-diagonal elements of $\boldsymbol{B'}\,\boldsymbol{T}$ equal to zero. The elements on the diagonal can be any number Λ_n. The general equation is expressed

as:

$$\boldsymbol{B'}\begin{bmatrix} t_{11} & t_{12} & \cdots & t_{1n} \\ t_{21} & t_{22} & \cdots & t_{2n} \\ \vdots & \vdots & \ddots & \vdots \\ t_{n1} & t_{n2} & \cdots & t_{nn} \end{bmatrix} = \begin{bmatrix} \Lambda_1 & 0 & \cdots & 0 \\ 0 & \Lambda_2 & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & \Lambda_n \end{bmatrix} \tag{3.48}$$

This approach requires a system of n equations that can be cumbersome to implement and solve, therefore it is only recommended for $n = 2$.

2. **Using $\boldsymbol{P}$:** some systems can diagonalize $\boldsymbol{B'}$ using $\boldsymbol{T} = \boldsymbol{P}$ or $\boldsymbol{T} = \boldsymbol{P^{-1}}$, although is not always possible. Using this proposed $\boldsymbol{T}$ could lead to non-diagonal control matrices.

3. **Solving $\boldsymbol{B'T} = \boldsymbol{B_D}$ by fixing $\boldsymbol{B_D}$:** this is the most direct method, and recommended in this work. Setting the control matrix $\boldsymbol{B_D}$ to a desired diagonal matrix can be used to solve the matrix equation as follows:

$$\begin{aligned} \boldsymbol{B'T} &= \boldsymbol{B_D} \\ \boldsymbol{T} &= \boldsymbol{B'}^{-1}\boldsymbol{B_D} \end{aligned} \tag{3.49}$$

This method is possible if the initial input matrix ($\boldsymbol{B}$) is invertible.

Setting different objective input matrices ($\boldsymbol{B_D}$) can lead to different diagonalizations. A trivial diagonalization can set $\boldsymbol{B_D}$ equal to the identity matrix $\boldsymbol{I_n}$. In this case the control variable transformation matrix $\boldsymbol{T}$ is equal to $\boldsymbol{B'^{-1}}$:

$$\boldsymbol{T} = \boldsymbol{B}^{-1}\boldsymbol{I_n} = \boldsymbol{B}^{-1} \tag{3.50}$$

This is a direct diagonalization that may change the physical interpretation of the new control variables. For instance, a model (3.2), where the state variables $\boldsymbol{x}$ are the arm currents, the control variables $\boldsymbol{u}$ are the arm voltages, and $\boldsymbol{V_k}$ are the system voltages,

the elements of $\boldsymbol{B'}$ have the following general form:

$$\boldsymbol{B'} = \boldsymbol{P}^{-1}\boldsymbol{L}^{-1}\boldsymbol{V_c} = \begin{bmatrix} \frac{k_{11}}{L_{eq1}} & \frac{k_{12}}{L_{eq1}} & \cdots & \frac{k_{1n}}{L_{eq1}} \\ \frac{k_{21}}{L_{eq2}} & \frac{k_{22}}{L_{eq2}} & \cdots & \frac{k_{2n}}{L_{eq2}} \\ \vdots & \vdots & \ddots & \vdots \\ \frac{k_{n1}}{L_{eqn}} & \frac{k_{n2}}{L_{eqn}} & \cdots & \frac{k_{nn}}{L_{eqn}} \end{bmatrix} \tag{3.51}$$

where k_{ij} are constants multiplying the equivalent inductances L_{eqj} (with $i, j \in [1, n]$). Then, the transformation matrix $\boldsymbol{T}$ can be expressed as:

$$\boldsymbol{T} = \boldsymbol{B'}^{-1} = \begin{bmatrix} k'_{11}L_{eq1} & k'_{12}L_{eq2} & \cdots & k'_{1n}L_{eqn} \\ k'_{21}L_{eq1} & k'_{22}L_{eq2} & \cdots & k'_{2n}L_{eqn} \\ \vdots & \vdots & \ddots & \vdots \\ k'_{n1}L_{eq1} & k'_{n2}L_{eq2} & \cdots & k'_{nn}L_{eqn} \end{bmatrix} \tag{3.52}$$

The relation between the new control variables ($\boldsymbol{u'}$) and the initial variables $\boldsymbol{u}$ is expressed as:

$$\boldsymbol{u} = \boldsymbol{T}\,\boldsymbol{u'} \tag{3.53}$$

From (3.52) and (3.53), it is evident that the new control variables $\boldsymbol{u'}$ are a linear combination of $\boldsymbol{u}$, but they are not longer voltages, they are variations of currents in the time, dI/dt. If the state variable transformation $\boldsymbol{P}$, and the control variable transformation $\boldsymbol{T}$ are applied to the initial system found in (3.2), the following system is found:

$$\frac{d}{dt}\boldsymbol{I'} = \boldsymbol{A_D}\,\boldsymbol{I'} + \boldsymbol{B_D}\,\boldsymbol{V'}$$

$$\frac{d}{dt}\boldsymbol{I'} = \boldsymbol{P^{-1}}\boldsymbol{L^{-1}}\boldsymbol{R}\,\boldsymbol{P}\,\boldsymbol{I'} + \boldsymbol{I_n}\,\boldsymbol{V'} \tag{3.54}$$

where $\boldsymbol{I_n}$ is the identity matrix of size n, with n the number of state variables of the mathematical model.

As the identity matrix is unitless, the new control variable $\boldsymbol{V'}$ must have the same dimensions of the left hand of the expression, i.e. a variation of current in time. The new control variables $\boldsymbol{u'}$ ($\boldsymbol{V'}$ in previous example), might complicate the control strategy

design as the mathematical model has coupled terms depending on the equivalent inductances of the circuit, which can lead to bulky calculations.

To avoid changing the physical interpretations of the new variables, the objective $\boldsymbol{B_D}$ should consider the equivalent inductances in its elements. With this approach, it can be assured that the elements of $\boldsymbol{T}$, t_{ij}, are indepedent from the circuit parameters, and that $\boldsymbol{u'}$ is a set of equivalent voltages. From (3.51) the suggested structure of $\boldsymbol{T}$ is:

$$\boldsymbol{B'\,T} = \boldsymbol{B_D} = \begin{bmatrix} \frac{t_{k1}}{L_{eq1}} & 0 & \cdots & 0 \\ 0 & \frac{t_{k2}}{L_{eq2}} & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & \frac{t_{kn}}{L_{eqn}} \end{bmatrix} \tag{3.55}$$

$$\boldsymbol{T} = \boldsymbol{B'}^{-1} \begin{bmatrix} \frac{t_{k1}}{L_{eq1}} & 0 & \cdots & 0 \\ 0 & \frac{t_{k2}}{L_{eq2}} & \cdots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \cdots & \frac{t_{kn}}{L_{eqn}} \end{bmatrix} \tag{3.56}$$

where L_{eq_j} is the equivalent inductance found in (3.44), and t_{kj} is a set of constants that can be changed to adapt the physical interpretation of the new variables, in this thesis $t_{kj} = 1$, with $j \in [1, n]$.

Finding the correct $\boldsymbol{T}$ allows to decouple the control variables with the following transformations:

$$\boldsymbol{u} = \boldsymbol{T}\,\boldsymbol{u'} \tag{3.57}$$

$$\boldsymbol{u'} = \boldsymbol{T}^{-1}\boldsymbol{u} \tag{3.58}$$

The complete diagonal system can be expressed as:

$$\dot{\boldsymbol{x}}' = \boldsymbol{A_D}\,\boldsymbol{x'} + \boldsymbol{B_D}\,\boldsymbol{u'} + \boldsymbol{K_V^{ss'}}\,\boldsymbol{V_k} \tag{3.59}$$

where $\boldsymbol{B_D} = \boldsymbol{B'}\,\boldsymbol{T}$, and $\boldsymbol{K_V^{ss'}} = \boldsymbol{P}^{-1}\,\boldsymbol{K_V^{ss}}$.

The system (3.59) is a set of decoupled equations that describe the initial converter. From the initial mathematical model (3.2), (3.59) can be expressed in terms of the circuit parameters as follows:

$$\begin{aligned}\frac{d}{dt}\boldsymbol{I'_{arm}} =& \boldsymbol{P^{-1}\,L^{-1}\,R\,P\,I'_{arm}} \\ &+ \boldsymbol{P^{-1}\,L^{-1}\,V_c\,T\,V'_{arm}} \\ &+ \boldsymbol{P^{-1}\,L^{-1}\,K_V\,V_k}\end{aligned} \tag{3.60}$$

The decoupled equations in (3.60) can be represented by equivalent circuits as the one presented in Fig. 3.9. Each circuit has an equivalent impedance composed of an inductor, L_{eq_i}, and a resistance, R_{eq_i}. The circuit depends on the equivalent voltage $[\boldsymbol{B_D\,u'}]_{\boldsymbol{i}}$ ($\boldsymbol{u'} = \boldsymbol{V'_{arm}}$) and the system voltages $[\boldsymbol{K_V^{ss'}\,V_k}]_i$, which can be dc or ac voltages. The equivalent current x'_i ($x'_i = I'_{arm_i}$) is also represented in the circuit, for $i \in [1, n]$.

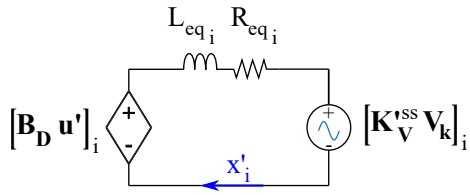


Figure 3.9: Equivalent circuit for the i^{th} line of (3.59).

The diagonalization methodology leads to a decoupled system, facilitating the control design of the converter, but the new system may be difficult to interpret. The equivalent circuit in Fig. 3.9 should have a physical interpretation to set the objective of the controller governing this equivalent current. For instance, an equivalent circuit representing the path through the ground could be controlled to maintain the current to zero, avoiding interactions between interconnected systems.

If the physical interpretation of the equivalent circuit is hard to find, the system can be adjusted, by changing the factors k_j in (3.56) or multiplying one or multiple columns of $\boldsymbol{P}$ by a constant k_{ej}.

Following the example of the MMC (see Section 3.3), to diagonalize the MMC mathematical model found in (3.6), the transformations matrices $\boldsymbol{P}$ and $\boldsymbol{T}$ must be found. The currents transformation, $\boldsymbol{P}$, can be found

following the method presented in Appendix A. The $\boldsymbol{P}$ matrix found is:

$$\boldsymbol{P} = \begin{bmatrix} 1 & 1 \\ -1 & 1 \end{bmatrix} \quad \boldsymbol{P}^{-1} = \begin{bmatrix} \frac{1}{2} & -\frac{1}{2} \\ \frac{1}{2} & \frac{1}{2} \end{bmatrix} \tag{3.61}$$

The MMC eigenvalues are:

$$\lambda_1 = -\frac{2\,R_{ac} + R}{2\,L_{ac} + L} \tag{3.62}$$

$$\lambda_2 = -\frac{R}{L} \tag{3.63}$$

Following the recommended method, the $\boldsymbol{T}$ matrix, based in (3.56) is:

$$\boldsymbol{T} = \begin{bmatrix} -\frac{1}{2(2L_{ac}+L)} & \frac{1}{2(2L_{ac}+L)} \\ -\frac{1}{2L} & -\frac{1}{2L} \end{bmatrix}^{-1} \begin{bmatrix} \frac{1}{2\,L_{ac}+L} & 0 \\ 0 & \frac{1}{L} \end{bmatrix} = \begin{bmatrix} -1 & -1 \\ 1 & -1 \end{bmatrix} \tag{3.64}$$

Using the found $\boldsymbol{P}$ and $\boldsymbol{T}$, the complete diagonal system for the MMC is:

$$\begin{aligned} \begin{bmatrix} \dot{I}_1 \\ \dot{I}_2 \end{bmatrix} &= \begin{bmatrix} -\frac{2\,R_{ac}+R}{2\,L_{ac}+L} & 0 \\ 0 & -\frac{R}{L} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \\ &+ \begin{bmatrix} \frac{1}{2\,L_{ac}+L} & 0 \\ 0 & \frac{1}{L} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \\ &+ \begin{bmatrix} \frac{1}{2(2L_{ac}+L)} & -\frac{1}{2(2L_{ac}+L)} & -\frac{1}{2L_{ac}+L} \\ \frac{1}{2L} & \frac{1}{2L} & 0 \end{bmatrix} \begin{bmatrix} V_1^{dc} \\ V_2^{dc} \\ V^{ac} \end{bmatrix} \end{aligned} \tag{3.65}$$

where I_1 and I_2 are a linear combination of the arm currents I_u and I_l, similar to V_1 and V_2 which are a linear combination of the arm voltages V_u and V_l.

3.6.2 Energy control

The main goal of the energy control is to keep the converter energy controlled. Based on (3.23) it can be evidenced that the energy can be controlled by adjusting the ac or dc power in the arms. From the power

balance per arm presented in (3.28) and (3.29), the energy variation can be related to the arm power as follows:

$$\frac{d}{dt}\boldsymbol{E_{arms}}(t) = \begin{bmatrix} V_{arm_1} I_{arm_1} \\ V_{arm_2} I_{arm_2} \\ \vdots \\ V_{arm_g} I_{arm_g} \end{bmatrix} \tag{3.66}$$

where g is the number of arms per leg of the converter.

The energy in the arm can be controlled either with the ac or dc components of the arm voltage, V_{arm}, or the arm current, I_{arm}. As the mathematical model is set to keep the arm currents as the state variables, the control strategy is centered in the arm currents. As presented previosly, the energy control sets the reference to the current control (see Fig. 3.8).

From (3.2) the coupling between the arm variables can be evidenced. Hence, changing the current in one arm changes also the current in the others affecting the energy in both arms. Similarly, the arm powers expressed in the new variables $\boldsymbol{x'}$ and $\boldsymbol{u'}$ have coupled terms which complicates the energy control.

To simplify the energy control, a third change of variables is used ($\boldsymbol{W_T}$). The energy transformation relates the new energy variables ($\boldsymbol{E'}$) with the initial arm energy ($\boldsymbol{E_{arms}}$), as follows:

$$\frac{d}{dt}\boldsymbol{E'}(t) = \boldsymbol{W_T}\frac{d}{dt}\boldsymbol{E_{arms}}(t) \tag{3.67}$$

where $\boldsymbol{W_T}$ is the energy transformation matrix. $\boldsymbol{W_T}$ has the same size of the initial system (3.2), i.e. a square matrix $n \times n$. The energy transformation matrix can be equal to either $\boldsymbol{P}$, $\boldsymbol{T}$ or a new matrix setting new energy variables as a linear combination of the arm powers.

To design the control strategy, $\boldsymbol{E'}$ is expressed in terms of the new variables $\boldsymbol{x'}$ and $\boldsymbol{u'}$, similar to the following expression:

$$\frac{d}{dt}\boldsymbol{E'}(t) = \begin{bmatrix} V_1 I_1 + V_1 I_2 + \cdots + V_n I_n \\ \vdots \\ V_n I_n + V_n I_2 + \cdots + V_n I_n \end{bmatrix}_{n\times 1} \tag{3.68}$$

where $V_i \in \boldsymbol{u'}$ and $I_i \in \boldsymbol{x'}$ for $i \in [1, n]$.

The expression (3.68) is just an example illustrating the possible structure of $\frac{d}{dt}\boldsymbol{E'}$ as the energy transformation ($\boldsymbol{W_T}$) depends on each converter topology (see chapters 5, 6, and 7).

Additional to the energy transformation, the energy controller has the following assumptions:

1. As mentioned previously, the energy control sets the reference to the current control, the time response of the current control loops should be fast enough to be neglected on the energy control design, i.e. $\tau_I << \tau_E$.

2. The energy controllers are designed to follow average variations, controlling the average value of the converter energy.

3. The energy controller uses the measurements of the voltages in the arm equivalent capacitances. This voltage has oscillations at the first and second harmonic, that need to be filtered to obtain the average value of energy. The filter measuring the energy (feedback) has a fast response compared to the energy control, i.e. $\tau_{filter} << \tau_E$.

The general control loop and the simplifications due to the previous assumptions are presented in Fig. 3.10, where the internal loops and filters are simplified to unitary gains. In Fig. 3.10, $K_E(s)$ represents the energy controller, and $K_I(s)$ the current controller. The estimated current plant is represented by $G_I(s)$, while the relation between the arm power and the arm energy is represented by an integrator. P_C is the power calculated by the energy controller. P_D and V_D are the equivalent power and voltage disturbances.

To control the energy in the converter, a proportional-integral (PI) controller is considered. The PI controller has the following structure:

$$PI(s) = K_E(s) = K_p + \frac{K_i}{s} \tag{3.69}$$

The close loop transfer function, obtained from Fig. 3.10, has the structure of a second order system as follows:

$$G_E(s) = \frac{K_p\, s + K_i}{s^2 + K_p\, s + K_i} \tag{3.70}$$

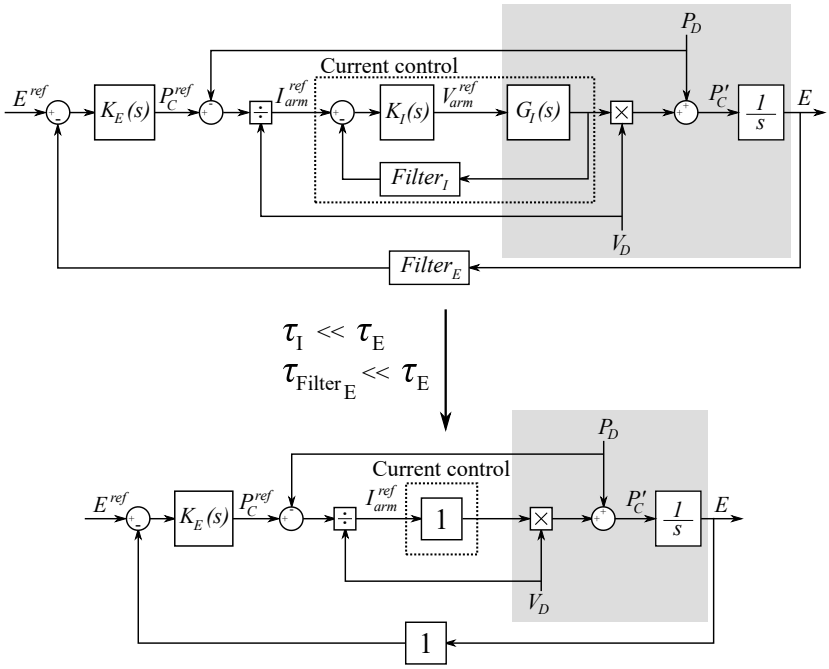


Figure 3.10: General scheme of energy and current control (top). Simplified energy control (bottom). The colored blocks are the estimated converter plant.

where the characteristic equation is adjusted to follow the desire response:

$$K_i = \omega^2 = \left(\frac{1}{\tau_E}\right)^2 \tag{3.71}$$

$$K_p = 2\zeta\sqrt{K_i} \tag{3.72}$$

where $\zeta = 0.707$, and τ_E is the time response desired for the energy controller. It can be set depending on the time response of the filter as follows:

$$\tau_E = K_F \ \tau_{filter_E} \tag{3.73}$$

where K_F is a constant that allows the control loop simplification illustrated in Fig. 3.10. Usually, K_F has a value grater than 5.

To obtain the average value of the energy, the measurement is filtered using two notch filters for the first and second harmonic, present in the voltages of the arm equivalent capacitors. The general transfer function is:

$$N(s) = \frac{s^2 + \omega_n^2}{s^2 + 2\omega_n s/Q + \omega_n^2} \cdot \frac{s^2 + 4\omega_n^2}{s^2 + 4\omega_n s/Q + 4\omega_n^2} \tag{3.74}$$

where ω_n is the operation frequency of the converter and Q is the quality factor, set to 3 [80,127]. The time constant of the notch filter, equivalent to τ_{filter_E} in (3.73), is:

$$\tau_{Notch} = \frac{Q}{\omega_n} \tag{3.75}$$

Assuming an operating frequency of 150 Hz, and $K_F = 9$, the constants used in the energy control are:

$$K_{i_{Energy}} = \frac{\omega_n}{K_F\, Q} \approx 1.2k \tag{3.76}$$

$$K_{p_{Energy}} = 2\zeta\sqrt{K_i} \approx 49 \tag{3.77}$$

The relation between the energy and the current control can be established from the equivalent energies found in (3.67). Using the example (3.68), each row represent an equivalent energy controller. One current is selected to control the energy, and the rest of the terms become feed forwards used in the control implementation. The general interaction is expressed as follows:

$$I^{ref} = \frac{P_C^{ref} + P_{FF}^{dc} + P_{FF}^{ac}}{V_D} \tag{3.78}$$

where P_C^{ref} is the output of the energy controller. P_{FF}^{dc} and P_{FF}^{ac} are the dc and ac components of the power disturbance P_D in Fig 3.10. V_D is the equivalent voltage. I^{ref} is expressed in terms of the transformed variables $\boldsymbol{x'}$, thus (3.78) depend on the converter modelling and the transformations $\boldsymbol{P}$, $\boldsymbol{T}$, and $\boldsymbol{W_T}$. The detailed expression is developed in the chapters dedicated to the dc-dc converters.

The ac and dc feed forwards can be implemented from the measurements of the corresponding powers, current and voltages. For some cases, a simplified approach is to use the steady-state values of the disturbances, leaving the controller $K_E(s)$ adjust its response to the dynamic variations in the system.

The current reference I^{ref} can be dc or the magnitude of an ac current, and it is used in the current control, which is detailed in the next section.

3.6.3 Current control

The current controller can be calculated directly from the diagonal system (3.59). The controllers are designed to govern the transformed currents $\boldsymbol{x'}$. There is one controller per equivalent state variable, in other words, for a mathematical model with n state variables, there are n independent equations, and in consequence, n current controllers.

From the diagonal system (3.59), where $\boldsymbol{x}$ are the arm currents and $\boldsymbol{u}$ are the arm voltages, as presented in (3.2), the equivalent i^{th} circuit can be represented by the following general expression:

$$(s\,L_{eq_i} + R_{eq_i})\,I'_{arm_i} = \left(\boldsymbol{B_D}\,\boldsymbol{V'_{arm}}\right)_i + \left(\boldsymbol{K_V^{ss'}}\,\boldsymbol{V_k}\right)_i \tag{3.79}$$

where s represent the Laplace variable. Rearranging into the equivalent transfer function:

$$G_I(s) = \frac{I'_{arm_i}}{V_{eq_i}} = \frac{1}{s\,L_{eq_i} + R_{eq_i}} \tag{3.80}$$

where V_{eq_i} is the equivalent voltage:

$$V_{eq_i} = \left(\boldsymbol{B_D}\,\boldsymbol{V'_{arm}}\right)_i + \left(\boldsymbol{K_V^{ss'}}\,\boldsymbol{V_k}\right)_i \tag{3.81}$$

From (3.80), it can be evidenced that the diagonalized system simplifies the equivalent current transfer function into a first order system depending on an equivalent inductor and resistance. The simplified current control loop is presented in Fig. 3.11.

As previously stated, the arm currents have dc and ac components (3.26). To control both components, a PI-resonant (PIR) controller is used, $K_I(s)$ in Fig 3.11. The PIR structure and tuning strategy is based on the one presented in [129].

The PIR transfer function is presented in (3.82), where K_{PIR}, (3.83), is a constant depending on the crossover frequency ω_c, (3.84), the resonance frequency ω_r and the equivalent circuit parameters $L_{eq\,j}$ and $R_{eq\,j}$. The desired phase margin at the resonance frequency is φ_{PM}, T_d is the time delay, and α_{PIR} is estimated in (3.85).

$$G_{PIR}(s) = K_{PIR}\frac{(s+\alpha_{PIR})^3}{s\,(s^2+w_r^2)} \tag{3.82}$$

$$K_{PIR} = \frac{\left(\omega_c^2 - \omega_r^2\right)\sqrt{\omega_c^2 L_{eq\,j}^2 + R_{eq\,j}^2}}{\omega_c} \tag{3.83}$$

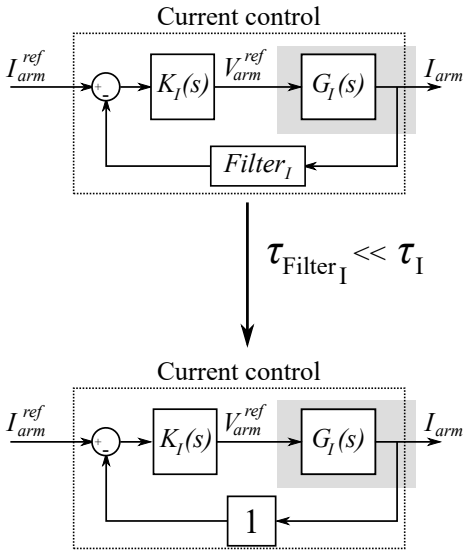


Figure 3.11: General current control (top) and its simplification (bottom). The colored blocks represent the estimated converter plant.

$$\omega_c = \frac{\pi/2 - \varphi_{PM}}{T_d} \tag{3.84}$$

$$\alpha_{PIR} = \frac{\omega_c}{10} \tag{3.85}$$

3.6.4 Power and voltage control

The power control ensures that the power exchanged is following the reference. The power control can be designed to limit the rate of change of the power exchanged by adjusting its response time (τ_P).

The voltage control is normally used for the dc side of the converter. For the dc-dc converters, the control can be done in one of the interconnected systems at a time. The voltage control must have an estimation of the capacitance in the dc line [119].

The dc-dc converters studied in this thesis are set to control the power between the lines. The voltage control is done by the dedicated ac-dc converters on the lines. Other type of control modes can be studied in future works.

The power control depends on the converter topology, therefore it is detailed on the chapters dedicated to each dc-dc converter (Chapters 5, 6, and 7).

3.6.5 Low-level control

The low-level control depends on the type of model being simulated. The *Ctrl signal* presented in Fig. 3.8 is different if the converter model is detailed or semi-detailed (type 1-4, see table 3.1 [105]), or if it is an average model (type 5-6). For the main simulations developed in this thesis, the *Ctrl signal* sent to the converter model corresponds to a modulation index (3.1) as an AAM is used.

For detailed converter models, the *Ctrl signal* is a binary signal (for HBSMs) with length equal to the number of SMs, which indicates the insertion or bypass of each SM[1]. This signal comes from a balancing capacitor algorithm (BCA) or a pulse width modulation (PWM) [49, 112, 130–132].

For the AAM used in this thesis, an additional signal is added to indicate the blocked state of the converter (see Fig. 3.3).

3.7 Chapter conclusions

This chapter has presented the general hypotheses and assumptions for the modeling, analysis, and control design of modular multi-level converters. The reduced order average arm model (AAM) and the equivalent arm voltage are introduced as the base of the converter model simplification, from which the mathematical model is developed. A dc steady-state analysis is presented to understand the converter balancing requirements. A preliminary converter sizing is presented to calculate the number of SMs per arm, the needed capacitance, and the circuit inductances. Then, from the mathematical model, a system diagonalization is proposed to simplify the converter control design. The generalities for the control tuning are presented along with the general structure. The methodology presented in this chapter is applied in detail for the dc-dc converters studied in Chapters 5, 6, and 7. The next chapter presents the case study defined to design and validate the dc-dc converters under study.

[1] For the converters with FBSMs the control signal has three states for the positive insertion, bypass, and negative insertion. In the AAM this is equivalent to have a modulation index between -1 and 1.

Chapter 4

Case Study definition

4.1 Introduction

This chapter presents the parameters and hypotheses for a considered interconnection. First, the considered interconnection is introduced and then, the simulation model and the different simulation scenarios are detailed.

4.2 Considered interconnection

In Chapter 1 the heterogeneous interconnection were defined as the connections between lines with different line topologies, different technologies, or high voltage ratio (see Section 1.4.2). A review of the present and future HVDC projects is compiled in Appendix G. From this list, the three characteristics to define an heterogeneous interconnection can be analyzed.

From the current and future projects, there is a tendency to use B and SyM line topologies. The projects with high rated power, i.e. above 600 MW, have similar dc voltages, which could lead to a medium voltage ratio interconnection. Even if most of the new projects are based on VSCs, LCCs cannot be put aside but, this interconnection is more probable in China because of it large HVDC corridors. Focusing in the case of Europe, the most probable interconnection is between a B and a SyM, and is studied in the rest of this thesis.

4.3 System under study

The interconnection between a B and a SyM is modeled in Simulink/Matlab environment. The model employs six ac-dc converters (four for the B and two for the SyM line) and one dc-dc converter. Each ac-dc converter has an adjacent ac circuit breaker (ACCB) (squares in Fig 4.1), which is

triggered in the case of fault detection. The ACCBs have a time delay of 100 ms to simulate the opening time of a real ACCB. The lines are controlled in a classical master-slave strategy, where one station controls the dc voltage while the remaining station controls the power. The dc-dc converter is in power control mode, similar to a slave ac-dc converter. The dc-dc converter is connected in the middle of the two lines. The principal line parameters were based in the NordLink-COBRA cable interconnection as they represent the most similar example to the considered case study. The parameters are presented in Table 4.1.

Table 4.1: Principal parameters of the interconnected lines

Parameter	Bipole	Symmetric monopole
Power	1400 MW	700 MW
Dc voltage	±525 kV	±320 kV
Length	623 km	325 km

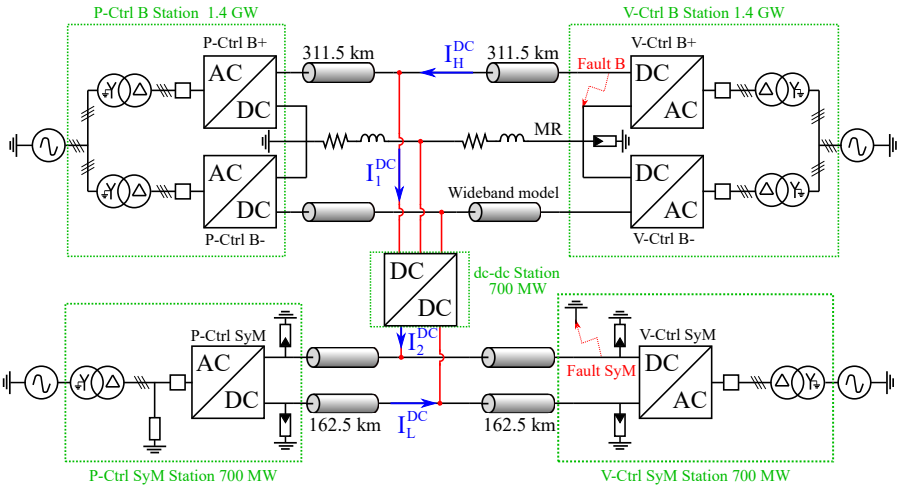


Figure 4.1: General scheme for the case study interconnection.

Fig. 4.1 shows the general sketch of the proposed interconnection. The system is analyzed in normal operation and under faults. Two fault locations studied are shown on the diagram as Fault B and Fault SyM. The fault on the B line is equivalent to a pole-to-pole fault in the positive

ac-dc converter of the voltage-controlled station. The fault considered in the SyM is a pole-to-ground fault on the positive pole of the voltage-controlled station.

The main characteristics of the model are presented in the following sections.

4.3.1 Ac-dc converters

An MMC is considered for each of the six ac-dc converters in the case study. The converter is implemented with the average arm model (AAM, see Section 3.2.2) to reduce the simulation time while keeping the dominant transient behavior [105, 106].

The MMC modeling and control has been object of multiple publications [18, 114, 127, 133–136]. The control of the ac-dc MMCs used in this case study follows the design presented in [137], which implements the virtual capacitor concept for the voltage control of the HVDC links.

The virtual capacitor uses the internal energy of the converter, i.e. the energy stored in the capacitors of the SMs, to support the dc voltage stability. Different from the classical control where the converter energy is controlled to follow a constant reference, the virtual capacitor allows energy variations during voltage transients on the dc side. The maximum energy variation depends on a virtual capacitor constant, which links the internal equivalent converter capacitor with the voltage control ($C_{vc} = C_{eq\,conv}\,k_{vc}$). For this study case, the virtual capacitor constant (k_{vc}) is set to 1. The simplified MMC control strategy is presented in Fig. 4.2, where the energy is controlled per leg ($W_{vertical}$), the difference between legs ($W_{horizontal}$), and the total energy in the converter (W_{total}).

4.3.2 Cables

The HV cables are modelled with the universal line model (ULM) developed in the Best Paths project [138]. The ULM allows to have a frequency dependant model. The model developed in the Best Paths project is designed for a single conductor cable, i.e. a central conductor and an insulator as shown in Fig. 4.3. There are two types of cables used in this study a ±525 kV and a ±320 kV [139]. The principal characteristics are presented in Table 4.2. Based on the cable geometries, the equivalent capacitances are: $C_{525} = 178.9\,\mathrm{nF/km}$ and $C_{320} = 175.9\,\mathrm{nF/km}$.

The bipole uses an RL equivalent to model the metallic return (MR) as shown in Fig. 4.1. The MR is modeled with a resistance of 8.8 mΩ/km and an inductance of 96.3 µH/km. Each cable model (HV cables and MR), is separated into two halves to allow the connection of the dc-dc.

4.3.3 Surge arresters

Five surge arresters (SA) are included in the model to protect against overvoltages after the considered faults. There is a surge arrester at the end of the MR (at the terminal of the V-Ctrl station) in the bipole. This surge arrester keeps the MR voltage within the operational limits during the fault events to avoid disturbances on the healthy pole. The

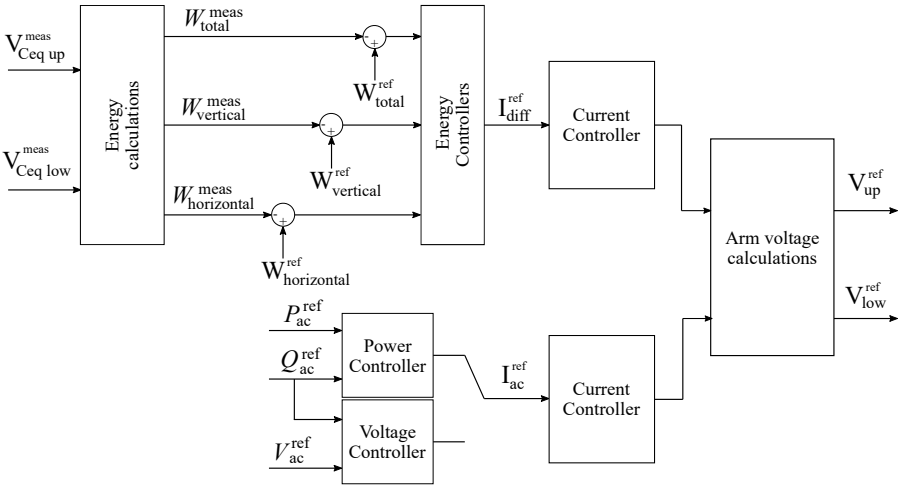


Figure 4.2: General control strategy for the ac-dc MMCs.

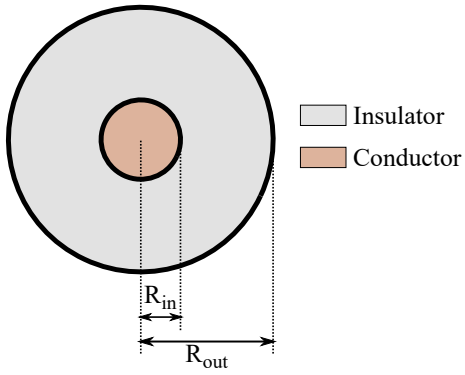


Figure 4.3: General geometry used for the ULM from [138].

other four voltage protections are implemented at the terminals of each stations of the SyM. The poles in the bipole line are not protected with SAs as the voltage in these poles have smaller variations than the pole displacement in the SyM for the considered faults. The SA protecting the MR has a protection voltage of 25 kV, while the SAs on the SyM are rated to 512 kV.

4.3.4 Ac grids

The ac grids are considered to be strong and balanced. The ac system is modeled with a Thévenin equivalent having a short-circuit power of 45 GW and a X/R ratio of 10. The four ac systems are considered equal with a phase-to-phase RMS voltage $U_{ac} = 400$ kV. Three-phase transformers, with a leakage inductance of 0.15 p.u., are used to interface the MMCs with the ac grids. The RMS ac phase-to-phase voltage (U_{ac}^{MMC}) at the terminals of the MMCs respects the following expression:

$$U_{ac}^{MMC} = k_{ac} \frac{V_{pole-to-pole}^{dc}}{2} \sqrt{\frac{3}{2}} \tag{4.1}$$

where k_{ac} is a constant smaller than 1, normally 0.85, that sets U_{ac}^{MMC} smaller than the maximal available voltage generated by the MMC. k_{ac} can be chosen depending on the system requirements and restrictions, e.g. the strength of the ac grid.

Using (4.1), with $k_{ac} = 0.85$, the ac voltages for the MMCs on the bipole and SyM are 333 kV and 273 kV respectively.

Table 4.2: Cable parameters

Section	Cable 320kV [139]	Cable 525kV
Length	325 km 2 sections of 162.5 km	623 km 2 sections of 311.5 km
Core (R_{in})	$R_{in} = 25.1$ mm $\rho = 1.7e^{-8}\ \Omega\,\mathrm{m}$	$R_{in} = 25.95$ mm $\rho = 1.7e^{-8}\ \Omega\,\mathrm{m}$
Insulator (R_{out})	$R_{out} = 74$ mm $\epsilon_r = 2.5$ $\mu_r = 1$	$R_{out} = 73.5$ mm $\epsilon_r = 2.5$ $\mu_r = 1$

The SyM has a unique ac grounding point at the power-controlled station (P-Ctrl) through a star point reactor [105,123,140]. The structure and values are presented in Fig. 4.4. The Bipole is solid grounded at the power-controlled station, as presented in Fig. 4.1.

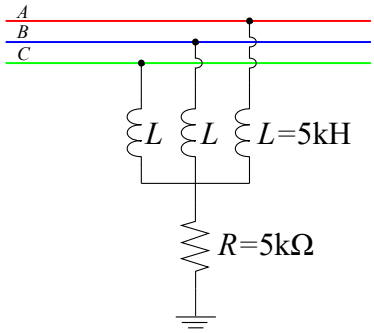


Figure 4.4: Star point reactor used for the grounding of the SyM [105, 123, 140].

4.3.5 Dc-dc converters

This thesis studies three dc-dc converters: the front-to-front modular multi-level converter (F2F-MMC), the flexible dc-MMC, and the asymmetric dc-dc converter (ADCC).

As mentioned in Chapter 2, the F2F-MMC is the preferred dc-dc converter, in the literature, for heterogeneous interconnections. This is considered as the reference solution. Indeed, with the industrial maturity of the ac-dc MMC, the implementation of a F2F-MMC (operating at 50 Hz) does not represent a significant technical challenge. The F2F-MMC modeling and simulation results are presented in Chapter 5. The flexible dc-MMC is a non-isolated converter adapted for the heterogeneous interconnections, presented in Chapter 6. The third dc-dc converter, the asymmetric dc-dc converter (ADCC), is a new topology proposed and studied in Chapter 7. The three converters consider three legs configurations but, any other number could be chosen.

4.3.6 Fault detection

The ac-dc and dc-dc converters are implemented with a fault detection algorithm that triggers the blocking signals of the converters, and the ACCB (in the case of ac-dc converters). A fault can be detected by the measurement of the voltages or currents. The two approaches are explained below.

Inspired in the dc voltage profiles for multi-terminal systems presented in [6, 141], the dc voltage operating and blocking zones for the ac-dc and dc-dc converter are proposed. The zones are presented in Fig. 4.5. The figure shows the voltage in p.u. on the vertical axis and the time length of a voltage transient on the horizontal axis. The transients are separated in fast (t_f), medium (t_m), and slow (t_s) events. The operational dc voltage limits are presented in Table 4.3.

The fault detection in the ac-dc converters is focused on the dc faults. As mentioned above, the ac systems are considered strong, balanced, and no ac faults are considered. The behavior of the ac-dc converters during ac faults is out of the scope of this thesis.

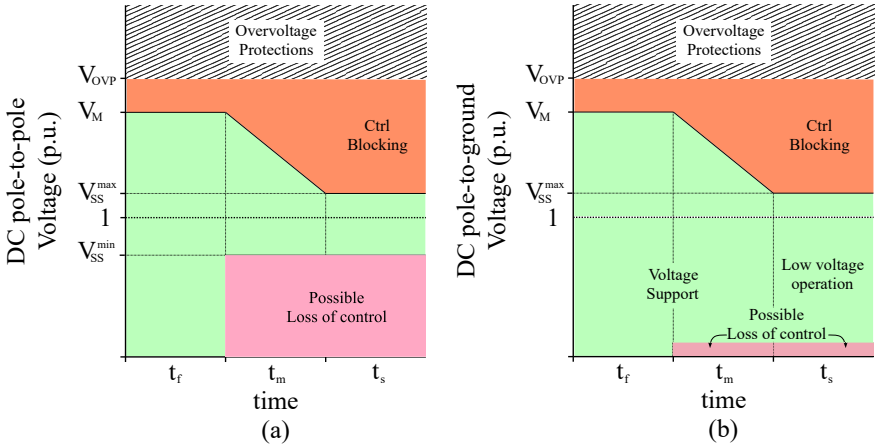


Figure 4.5: Proposed operating zones for the ac-dc converters (a) and the dc-dc converters (b).

Table 4.3: Parameters for the operating zones of the converters.

Parameter		Value	
		ac-dc	dc-dc
Fast transients time	t_f	$\sim$ 1 ms	$\sim$ 1 ms
Medium transients time	t_m	$\sim$ 4 ms	$\sim$ 4 ms
Slow transients time	t_s	$\sim$ 200 ms	$\sim$ 200 ms
Maximum peak transient	V_M	1.2 p.u.	1.2 p.u.
Minimum steady-state voltage	V_{SS}^{min}	0.85 p.u.	0 p.u.*
Maximum steady-state voltage	V_{SS}^{max}	1.05 p.u.	1.05 p.u.

* Ideal limit, in reality the converter needs a minimal dc voltage to control the dc current and its internal energy.

The measurement of a dc overvoltage leads to the trigger of the blocking signal. The main difference between the ac-dc converters (Fig. 4.5a) and the dc-dc converters (Fig. 4.5b) is the operational limits for the under voltage scenarios. The ac-dc converters have a restricted operation when the dc voltage decreases because they cannot modulate the ac voltage (fixed by the ac systems) and HBSMs have been considered. The dc-dc converter can reduce the power exchanged between the interconnected systems while the dc voltage is reduced working at maximal current. The main problem for the under voltages is the loss of current control. If the converter cannot control the current the overcurrent control triggers the blocking signal.

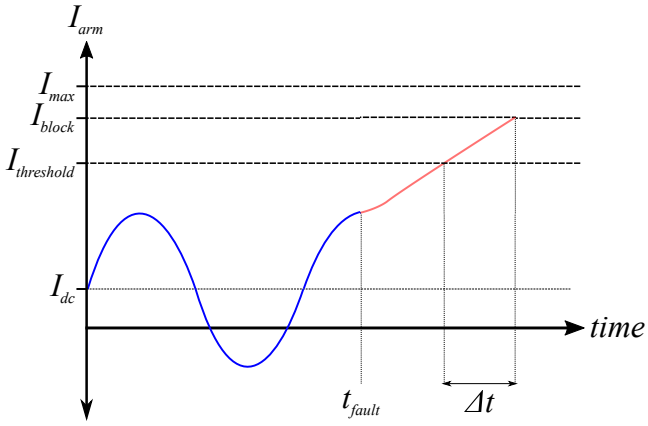


Figure 4.6: Fault arm current indicating the detection threshold ($I_{threshold}$), the processing time delay (Δt_{max}) and the maximum current that the switches can open (I_{max}).

The limit in the arm currents is set based on the current capacity of the considered semiconductors. In general, the IGBTs used for HVDC applications can open twice their nominal current. In consequence, the complete process, from the fault detection, sending the blocking signal to the SMs, to the opening of the IGBTs, must be done before reaching the physical limit of the switches ($I_{max} \approx 2$ p.u.). The considered IGBTs are rated to 3.3 kV and 1.8 kA, therefore the maximum current is 3.6 kA. The processing time can vary from one provider to another and the current threshold should be adjusted depending on the critical slope of the fault current. A maximum process time of $\Delta t_{max} = 300$ µs [123] is employed in this thesis. Fig. 4.6 illustrates the relation between the fault current detection threshold ($I_{threshold}$), the maximum processing time (Δt_{max}) and the slope of the current to block before the maximum current (I_{max}).

Supplementary criteria follows the slope of the arm current and triggers the blocking signal if the following condition is true:

$$\frac{d}{dt}I_{arm} > \frac{d}{dt}I_{crit} \tag{4.2}$$

where the critical fault current slope, dI_{crit}/dt, used in this thesis is 6.4 A/µs (see Section 3.5.2).

4.4 Simulation scenarios

To test the behavior of the dc-dc converters studied for the interconnection B-SyM, multiple simulations are proposed. There are a total of 22 simulations for each of the three studied converters. The simulations can be separated into the normal, and fault operation.

4.4.1 Normal operation

For the normal operation, the simulations are focused on the variations of the power flow direction (PFD) in the lines and through the dc-dc converter. Six simulation scenarios are proposed for these operation cases, they are presented in Table 4.4, the positive convention for the power flow directions are presented in Fig. 4.7.

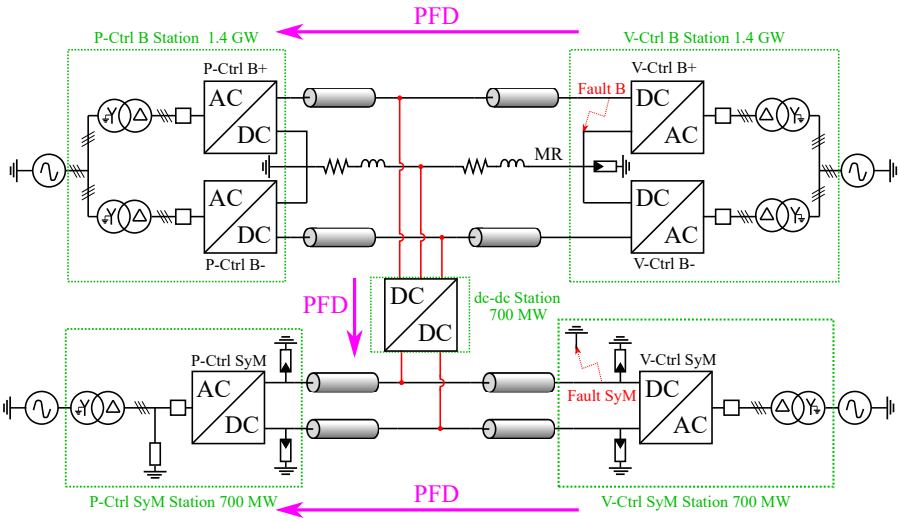


Figure 4.7: General scheme for the proposed case study with the positive power flow directions (PFD) considered.

Table 4.4: Simulation scenarios for the normal operation. PFD stands for power flow direction. The positive convention presented in Fig. 4.7 is used as reference.

Case	Description	
	Variable PFD	Fixed PFD
1	B ± 900 MW and SyM ± 200 MW	Positive in the dc-dc
2		Negative in the dc-dc
3	dc-dc ± 500 MW	Positive B and SyM
4	dc-dc ± 500 MW	Positive B, negative SyM
5	dc-dc ± 500 MW	Negative B, positive SyM
6	dc-dc ± 500 MW	Negative B and SyM

The six simulations help to verify the converter behavior during changes in the power reference. The power references (for the lines and dc-dc converter) have a constant rate of change of 2.5 p.u./s.

During the normal operation simulations, the power reference in the bipole is 900 MW and in the SyM is 200 MW. This reference is followed by the P-Ctrl stations on each line. Then, the dc-dc converter is set to exchange 500 MW between the lines. As example, in Case 4 the PFD in the B and SyM lines is fixed during the complete simulation with a power reference of +900 MW and -200 MW respectively. On the other hand, the dc-dc converter starts exchanging +500 MW (power exchanged from the B to the SyM) and, after reaching steady-state conditions, the power reference is changed to -500 MW (power exchanged from the SyM to the B).

The six simulations are repeated for the three dc-dc converters. Only the dc-dc converter model is changed.

4.4.2 Faults simulations

As mentioned at the beginning of this chapter, two dc faults are considered in this thesis: a pole-to-ground fault on the bipole and the same fault on the SyM line, both in the positive pole. The fault locations are presented in Fig. 4.7. Sixteen faults scenarios are tested, eight with a fault in the B and eight with a fault in the SyM. The eight variations correspond to different PFD in the lines and the dc-dc converter. The 8 possible PFD in the system at the moment of the simulated fault are presented in Table 4.5.

Table 4.5: Possible PFD in the interconnected system. Each case is simulated twice. Fist, a simulation with a fault on the B and then, with a fault on the SyM side. The positive power flow is presented in Fig. 4.7.

Case	B $\left(P_{ref}^{dc} = 900\text{MW}\right)$	dc-dc $\left(P_{ref}^{dc} = 500\text{MW}\right)$	SyM $\left(P_{ref}^{dc} = 200\text{MW}\right)$
1	Positive	Positive	Positive
2	Positive	Positive	Negative
3	Positive	Negative	Positive
4	Positive	Negative	Negative
5	Negative	Positive	Positive
6	Negative	Positive	Negative
7	Negative	Negative	Positive
8	Negative	Negative	Negative

The fault simulations start with the power references proposed for the normal operation simulations. After reaching steady-state operation, the fault is simulated. For the cases where the fault is on the B side, only 350 MW (half of the nominal power of the dc-dc converter) are exchanged between the interconnected lines (healthy pole of the bipole and SyM) after the fault clearing, without changing the power references in the B or SyM sides. For a fault in the SyM, the B line does not change the power reference and the SyM line is blocked.

As an example, in Case 6 the B has a power reference of -900 MW, the dc-dc converter exchanges 500 MW from the B to the SyM, and the power reference in the SyM line is -200 MW. Similar to the normal operation scenarios, the fault cases are repeated for the three considered dc-dc converters. Taking into account the normal and fault simulations for the three converters, a total of 66 simulations are proposed.

The general objective of these simulations is to validate the FBC of the dc-dc converters, i.e. validating that after a fault, the healthy protection zones should remain operational. The three dc protections zones of the interconnected system are presented in Fig. 4.8.

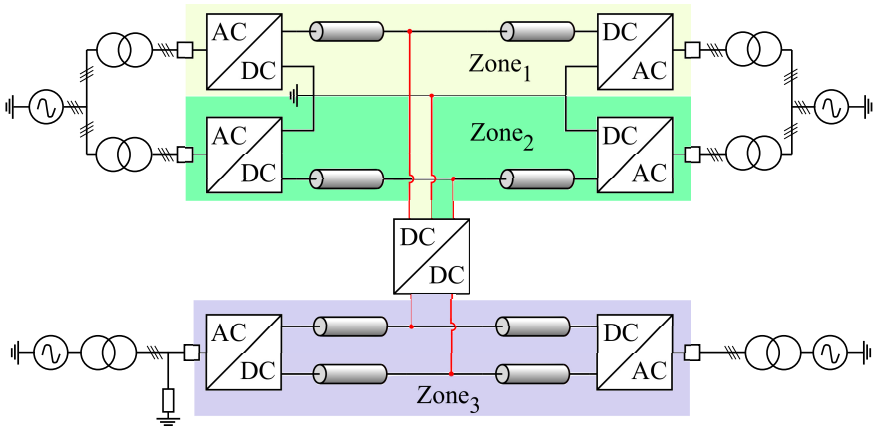


Figure 4.8: Protection zones of the proposed interconnected system. One protection zone per pole on the bipole line and a single protection zone for the SyM.

4.5 Chapter conclusions

This chapter has presented the case study proposed for this thesis: the interconnection between a bipole and a symmetric monopole. The details on cables, ac-dc and dc-dc converters were introduced. A proposition for the operating zones of the converters was presented to detect the faults on the dc side. Multiple simulations are proposed to test the dc-dc converter behavior during the power flow exchange and two fault scenarios. The proposed case study is used to evaluate the behavior of the F2F-MMC presented in Chapter 5, the flexible dc-MMC presented in Chapter 6, and the asymmetric dc-dc converter (ADCC) presented in Chapter 7.

Chapter 5

Front-to-Front Modular Multi-level Converter

5.1 Introduction

As presented in Chapter 2, the front-to-front is the most common solution presented in the literature, for the HVDC interconnections and specially for heterogeneous HVDC interconnections [39, 42, 47–61].

The industrial maturity of the ac-dc MMC, operating at 50 Hz can be used for the F2F-MMC development. This thesis considers a F2F-MMC operating at 150 Hz, which can reduce the size of some passive components such as the capacitors in the SMs and the ac transformer[6]. Reducing the size of these passive components could reduce the initial cost of the dc-dc converter. The increased frequency can also be challenging for the design of the ac transformer because of the isolation constraints. The volume can be reduced but, the voltage to isolate remains the same. It is expected that future developments can allow a dc-dc converter operating at this proposed frequency [6].

This chapter presents the modeling, sizing, control design, and simulation results following the structure and scenarios presented in Chapters 3, and 4.

5.2 Mathematical Modeling

The F2F needed for the case study defined in Chapter 4, should provide immediate redundancy on the bipole side (see Section 1.3.1). A F2F with three MMCs is considered as presented in Fig. 5.1. The dc-dc converter uses an MMC per pole, on the bipole side, and an MMC on the SyM side. The considered F2F uses 2 ac transformers with delta star windings. Both sides are unearthed to avoid ground loops with the grounding strategies of the lines. The impact of other winding configurations has not been studied.

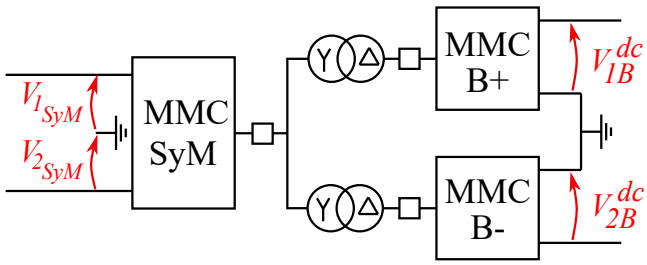


Figure 5.1: F2F-MMC considered for the case study. The squares represent the ac circuit breakers (ACCB) used in case of dc faults.

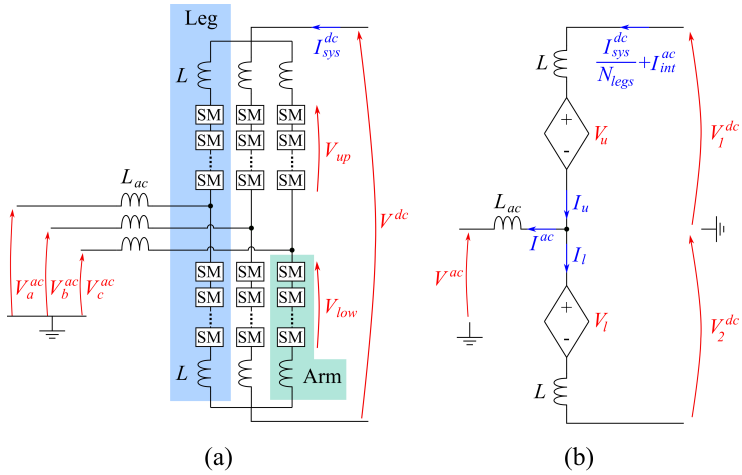


Figure 5.2: Modular multi-level converter. (a) three-phase circuit. (b) single-phase circuit used for the mathematical modeling.

As the MMCs employed on the F2F are separated by transformers, the dc-dc converter can be based on the MMC modeling. This section completes the mathematical modeling of an MMC, that has been partially developed in Chapter 3.

Adopting the modeling hypotheses presented in Section 3.3, the three-phase MMC circuit presented in Fig. 5.2a is reduced to the single-phase circuit as shown in Fig. 5.2b. The system current I_{sys}^{dc} is assumed to be equally divided between the number of legs, N_{legs}. The ac current I_{int}^{ac} is the internal ac current circulating inside the converter, between legs, i.e. it does not circulate in the dc system. Additionally, the dc voltage V^{dc} is separated into the pole-to-ground voltages V_1^{dc} and V_2^{dc}, and the series connection of SMs are replaced by a controlled voltage

source (see equivalent arm voltage in Section 3.2.1). The inductance L_{ac} is the equivalent inductance on the ac connection point, i.e. the leakage inductance of the transformer.

From Fig. 5.2b, two independent currents are identified: I_u and I_l. The two circuit equations are (5.1) and (5.2).

$$V^{ac} + L_{ac}\frac{d}{dt}(I_u - I_l) + R_{ac}(I_u - I_l) + V_u + L\frac{d}{dt}I_u + R\,I_u - V_1^{dc} = 0 \quad (5.1)$$

$$-V^{ac} - L_{ac}\frac{d}{dt}(I_u - I_l) - R_{ac}(I_u - I_l) + V_l + L\frac{d}{dt}I_l + R\,I_l - V_2^{dc} = 0 \quad (5.2)$$

where R_{ac} and R represent the ac inductance and the arm equivalent resistances respectively (not shown on Fig. 5.2).

The equations can be organized in the matrix form as follows:

$$\begin{bmatrix} L + L_{ac} & -L_{ac} \\ -L_{ac} & L + L_{ac} \end{bmatrix} \begin{bmatrix} \dot{I}_u \\ \dot{I}_l \end{bmatrix} = \begin{bmatrix} -(R + R_{ac}) & R_{ac} \\ R_{ac} & -(R + R_{ac}) \end{bmatrix} \begin{bmatrix} I_u \\ I_l \end{bmatrix} - \begin{bmatrix} 1 & 0 \\ 0 & 1 \end{bmatrix} \begin{bmatrix} V_u \\ V_l \end{bmatrix} + \begin{bmatrix} 1 & 0 & -1 \\ 0 & 1 & 1 \end{bmatrix} \begin{bmatrix} V_1^{dc} \\ V_2^{dc} \\ V^{ac} \end{bmatrix} \quad (5.3)$$

where the state variables are the arm currents I_u and I_l, the control variables are the arm voltages V_u and V_l and the system voltages are V_1^{dc}, V_2^{dc}, and V^{ac}.

5.3 Steady-state analysis

Using the mathematical model defined in (5.3) and the converter circuit presented in Fig. 5.2b the MMC steady-state operation can be analysed.

5.3.1 Dc steady-state analysis

As presented in Section 3.4.2, the arm dc currents can be expressed depending on the system dc currents. In the MMC case, there is only one system dc current as follows:

$$I_{sys}^{dc} = \frac{P_T^{dc}}{V_1^{dc} + V_2^{dc}} \quad (5.4)$$

where P_T^{dc} is the transmitted dc power. I_{sys}^{dc} is presented in Fig. 5.2 with a positive convention when the power exchange is from dc to ac side. Respecting the convention presented in Fig. 5.2b, the arm dc currents are related to I_{sys}^{dc} as follows:

$$I_u^{dc} = I_l^{dc} = \frac{I_{sys}^{dc}}{N_{legs}} = \frac{1}{V_1^{dc} + V_2^{dc}} \frac{P_T^{dc}}{N_{legs}}. \tag{5.5}$$

The arm dc voltages can be found with the following expression (see Section 3.4.2):

$$\boldsymbol{V}_{arm}^{dc} = -\boldsymbol{V_c}^{-1} \boldsymbol{K_V}\, \boldsymbol{V_k^{dc}} \tag{5.6}$$

From (5.3), $\boldsymbol{V_c}$ is the identity matrix of order two, $\boldsymbol{-I_2}$, and $\boldsymbol{K_V}$ is a 2×3 matrix, and $\boldsymbol{V_k^{dc}}$ is the vector containing only the system dc voltages. Then, the general expression (5.6) yields to:

$$\boldsymbol{V_{arm}^{dc}} = -\begin{bmatrix} -1 & 0 \\ 0 & -1 \end{bmatrix}^{-1} \begin{bmatrix} 1 & 0 & -1 \\ 0 & 1 & 1 \end{bmatrix} \begin{bmatrix} V_1^{dc} \\ V_2^{dc} \\ V^{ac^{dc}} \end{bmatrix} = \begin{bmatrix} V_1^{dc} - V^{ac^{dc}} \\ V_2^{dc} + V^{ac^{dc}} \end{bmatrix} \tag{5.7}$$

For the case where the MMC is connected in a SyM configuration, i.e. $V_1^{dc} = V_2^{dc}$, the ac voltage V^{ac} has no dc component, so $V^{ac^{dc}} = 0$. On the other hand, an MMC connected as an AM, i.e. with a pole connected to ground, e.g. $V_2^{dc} = 0$, and assuming $V^{ac^{dc}} = 0$ in expression (5.7) would suggest to have one arm operating with zero dc voltage, implying the use of FBSMs to modulate the negative part of the arm ac voltage (see Section 3.4.4 for the need of an ac component). For the MMC connected as an AM, the ac side has a dc component $V^{ac^{dc}} = V^{dc}/2$.

The dc voltage per arm in both cases is the same, $V^{dc}/2$, but the AM connection e.g. the positive pole of a B, add a dc voltage on the ac side of the converter.

5.3.2 Ac steady-state analysis

The MMC equivalent ac circuit is presented in Fig. 5.3. The voltage V^{ac} is the ac system phase-to-ground voltage, while V_u^{ac} and V_l^{ac} are the ac voltages in the MMC arms. It can be noticed that the arms and the system ac voltage are in parallel (including the inductors). The common node (ground reference), is the connection node for the converter n legs. For the MMC on the B side, this node represents the connection to

the ground or metallic return. The model is equivalent for both type of MMCs (connected to the B and to the SyM), the difference is the dc offset of V^{ac} for the MMC on the B side. From the ac circuit, the general expression, relating the grid ac voltage and the arms ac voltages, is obtained as:

$$V^{ac} + V_{L_{ac}} = V_l^{ac} + L\frac{d}{dt}I_l^{ac} = -V_u^{ac} - L\frac{d}{dt}I_u^{ac} \tag{5.8}$$

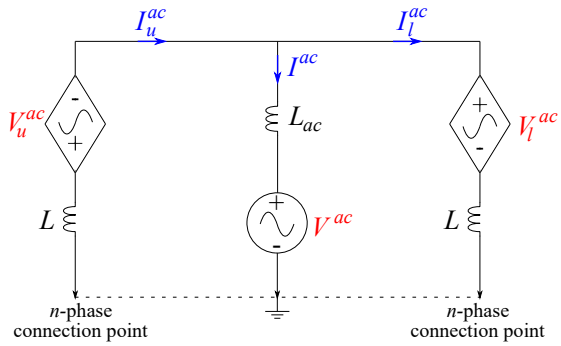


Figure 5.3: Equivalent ac circuit for the MMC.

From (5.7), the arm dc voltage is equal to $V_{u,l}^{dc} = V^{dc}/2$. Assuming that the arms are composed of only HBSMs, i.e. only positive modulation is considered, the maximum arm ac peak voltage generated by each arm is equal to $V^{dc}/2$ as shown in Fig. 5.4.

However, since the MMC does not use the complete range of V_{ac}, the ac voltage is usually scaled with k_{ac}, see (4.1), to have room for transients. Following this analysis, the complete arm voltages are expressed below:

$$V_u = V_1^{dc} + \frac{V^{dc}}{2}k_{ac}\cos(\omega t) \tag{5.9}$$

$$V_l = V_2^{dc} + \frac{V^{dc}}{2}k_{ac}\cos(\omega t + \pi) \tag{5.10}$$

In consequence, the ac voltage magnitude, V^{ac}, is set by $\frac{V^{dc}}{2}k_{ac}$, and the grid ac voltage magnitude is adapted to the MMC ac voltage using a transformer.

From Fig. 5.3 the ac current can be linked to the arm currents as follows:

$$I^{ac} = I_u^{ac} - I_l^{ac} \tag{5.11}$$

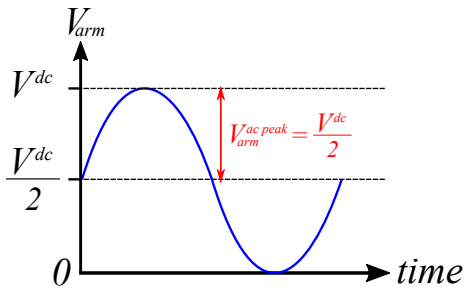


Figure 5.4: Maximum $V_{arm}^{ac\,peak}$ allowed for an MMC arm composed of HBSMs.

The arm currents magnitudes and phases can be defined depending on the power balance presented below.

5.3.3 Power balance

Using the arm dc currents (5.5) and arm dc voltages (5.7), the upper and lower arm dc powers can be found as follows:

$$P_u^{dc} = \frac{V_1^{dc} - V^{ac^{dc}}}{V_1^{dc} + V_2^{dc}} \frac{P_T^{dc}}{N_{legs}} \tag{5.12}$$

$$P_l^{dc} = \frac{V_2^{dc} + V^{ac^{dc}}}{V_1^{dc} + V_2^{dc}} \frac{P_T^{dc}}{N_{legs}} \tag{5.13}$$

Replacing $V^{ac^{dc}}$ by zero for the MMC connected to the SyM and $V^{dc}/2$ for the MMC connected on the B side the power, both converters, in steady-state and balanced conditions, have the same dc power per arm:

$$P_u^{dc} = P_l^{dc} = \frac{1}{2} \frac{P_T^{dc}}{N_{legs}}. \tag{5.14}$$

Considering a power transfer from the dc to the ac side, the dc power charges the arms in steady state. As mentioned in Chapter 3, to balance the energy in the converter, the excess of power absorbed by the arm should be transformed in ac power. Expression (5.14) is used to analyze the ac steady-state operation.

As indicated in (3.29), the power per arm, i.e. upper and lower arm, should respect the condition $P_{arm}^{dc} + P_{arm}^{ac} = 0$, which results in:

$$P_{arm}^{dc} = -P_{arm}^{ac}$$

$$\frac{1}{2}\frac{P_T^{dc}}{N_{legs}} = -\frac{V^{dc}}{2\sqrt{2}}k_{ac}\frac{|I_{arm}^{ac}|}{\sqrt{2}}\cos\left(\theta_{V_{arm}} - \theta_{I_{arm}}\right) \tag{5.15}$$

Considering a positive power, P_T^{dc}, the arm dc power, left hand of expression (5.15), is positive. To respect the equality, the current phase must comply with the following condition:

$$\cos\left(\theta_{V_{arm}} - \theta_{I_{arm}}\right) < 0 \tag{5.16}$$

For the upper arm, the ac voltage defined in (5.9) considers $\theta_{V_u} = 0°$. The angle giving the maximum ac power is $\theta_{I_u} = 180°$ or π rad. Replacing this angle in (5.15) yields to:

$$\frac{1}{2}\frac{P_T^{dc}}{N_{legs}} = |I_u^{ac}|\frac{V^{dc}}{2}k_{ac} \tag{5.17}$$

isolating the arm ac current magnitude:

$$|I_u^{ac}| = \frac{P_T^{dc}}{N_{legs}}\frac{2}{k_{ac}V^{dc}} \tag{5.18}$$

The same approach can be applied for the lower arm current. In this case, the arm voltage phase is $\theta_{V_l} = \pi$ rad, to respect power equality the current phase is $\theta_{I_l} = 0$ rad. Thus, the arm ac currents magnitudes are equal, i.e. $|I_u^{ac}| = |I_l^{ac}|$. The generalized arm current magnitude, for the MMC, is:

$$|I_{arm}^{ac}| = \frac{P_T^{dc}}{V^{dc}k_{ac}}\frac{2}{N_{legs}} \tag{5.19}$$

Then, the upper and lower arm currents can be expressed as:

$$I_u = \frac{1}{V_1^{dc} + V_2^{dc}}\frac{P_T^{dc}}{N_{legs}} + \frac{P_T^{dc}}{V^{dc}k_{ac}}\frac{2}{N_{legs}}\cos\left(\omega t + \pi\right) \tag{5.20}$$

$$I_l = \frac{1}{V_1^{dc} + V_2^{dc}}\frac{P_T^{dc}}{N_{legs}} + \frac{P_T^{dc}}{V^{dc}k_{ac}}\frac{2}{N_{legs}}\cos\left(\omega t\right) \tag{5.21}$$

Following expression (5.11), the ac current can be found with the difference between (5.20)-(5.21) as follows:

$$I^{ac} = \frac{P_T^{dc}}{V^{dc}k_{ac}}\frac{2}{N_{legs}}\left(\cos\left(\omega t + \pi\right) - \cos\left(\omega t\right)\right) \tag{5.22}$$

in phasor domain it is equivalent to:

$$\underline{I^{ac}} = -\frac{2P_T^{dc}}{V^{dc}\, k_{ac}\, N_{legs}} \tag{5.23}$$

The system ac current is linked to the magnitude and phase of the arm ac currents, i.e. changing the phase in the arm currents changes the active and reactive power exchanged with the ac system.

The present section has identified the dc and ac steady-state MMC operating conditions. For a positive power exchange, the dc power charges the arms while the ac discharges them. The excess of power in the arms is exchanged directly with the ac system using the ac currents. The interactions between dc and ac power are presented in Fig. 5.5.

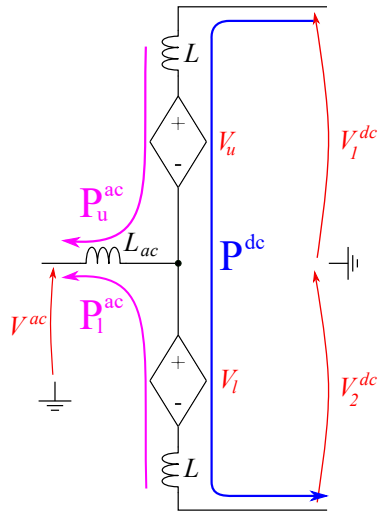


Figure 5.5: Energy balance in the MMC.

5.4 Preliminary converter sizing

5.4.1 Number of sub-modules per arm

Based on the case study and methodology described in Chapter 3, the number of SMs per arm depends on the semiconductor switches, which defines the operating voltage of each SM, the maximum voltage generated by the arm found in (5.9) and (5.10), and the fault blocking capability (FBC).

As stated in Section 5.3.2, the maximum voltage generated per arm is V^{dc}. During the normal operation of the MMC, the arms do not reach this maximum voltage. The ac modulation is limited with the k_{ac} factor. However, during this sizing stage, $k_{ac} = 1$ is considered. For the F2F-MMC operation, a factor k_{ac} of 0.7 and 0.8 for the B and SyM are used respectively. A large voltage margin is used on the MMCs connected to the B to provide the reactive power in the ac link. The k_{ac} factors used in the F2F are smaller than the one used in the ac-dc converters (see Chapter 4), to have a larger operation range for the dynamic variations in active and reactive power in the ac link between the MMCs.

The F2F-MMC used in this thesis needs two types of MMC, the first working at 525 kV (two MMC of this type are required for the bipole), and the second working at 640 kV (for the SyM side). Considering an average operating voltage for each SM of 1.6 kV (assuming IGBTs of 3.3 kV), and using (3.30), the minimum number of SMs needed per arm, for the first type of MMC is:

$$N_{SM_B}^{min} = \frac{V_{arm}}{V_{SM}} = \frac{525\,\text{kV}}{1.6\,\text{kV}} \approx 329 \tag{5.24}$$

The minimum number of SMs for the MMC on the SyM is:

$$N_{SM_{SyM}}^{min} = \frac{640\,\text{kV}}{1.6\,\text{kV}} \approx 400 \tag{5.25}$$

As explained in Section 3.5.1, the number of SMs can change depending on the FBC requirements. In this case, the FBC relays on the control strategy and the ACCBs. Therefore, the minimal number of SMs found in (5.24) and (5.25) remain unchanged.

Dc faults in a front-to-front with three MMCs

Reminding the structure presented in Fig. 5.1, the F2F-MMC proposed in this thesis has three MMCs that are interconnected on their ac sides. The equivalent ac circuit is presented in Fig. 5.6 where the MMC connected to the SyM sets the ac voltage reference, see Section 5.5.5.

In case of a dc fault on one pole of the bipole (B+), the healthy zones should continue to operate without disturbances, i.e. the MMCs connected to the healthy zones are not blocked (B- and SyM). The MMC connected to the faulted pole is blocked and it behaves as a diode rectifier as presented in Fig. 5.6. Due to the ac interconnection, the fault is fed

from the ac side and power exchange between SyM and B- is compromised. To avoid these fault currents, the F2F-MMC should use either ACCBs, DCCBs, or FBSMs.

In this thesis, ACCBs are used to block the dc faults (as shown in Fig. 5.1). Therefore, the presence of FBSMs is not needed. Taking into account the ac conditions inside the F2F, such as the operating frequency (150 Hz), and the fast dc fault detection (hundreds of µs), a shorter breaking time, compared to the ACCBs in the ac-dc converter, is considered feasible with the current breaker technologies. The ACCBs in the F2F model have a time delay of 30 ms to simulate the breaking time. The break time is defined in the IEC 62271-100 as the time from the instant when the breaker has received the opening signal to the instant of final arc extinction in all poles [142].

5.4.2 Circuit inductors

The arm inductance value can be calculated from the two suggested approaches presented in Section 3.5.2: using a value of 15% recommended in the literature [112,119], and evaluating the critical fault current slope in the mathematical model. The suggested approaches are presented more in detail as follows:

1. **Recommended 15%:** the arm inductance value is calculated from the base impedance as follows:

$$L_{15\%} = 0.15\,\frac{Z_{base}}{2\pi f} \tag{5.26}$$

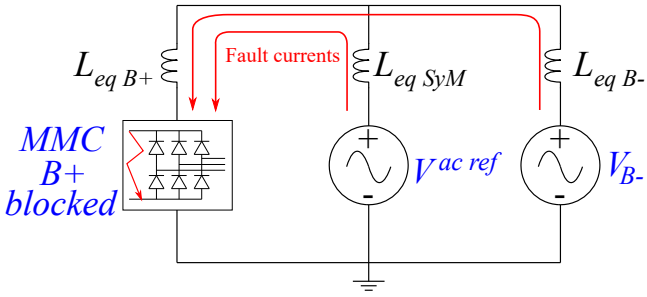


Figure 5.6: Equivalent ac system between the three MMCs for the considered F2F presented in Fig. 5.1. In case of a fault in the positive pole of the bipole, the MMC is blocked acting as a diode rectifier.

where Z_{base} is calculated with the values on the ac side of each of MMCs:

$$Z_{base_B} = \frac{(U^{ac})^2}{S^{ac}} = \frac{(225\,\mathrm{kV})^2}{700\,\mathrm{MW}} \approx 72\,\Omega \tag{5.27}$$

$$Z_{base_{SyM}} = \frac{(333\,\mathrm{kV})^2}{700\,\mathrm{MW}} \approx 140\,\Omega \tag{5.28}$$

The arm inductance values calculated with (5.26) are:

$$L_{15\%_B} = 0.15\,\frac{72\,\Omega}{2\pi 150\,\mathrm{rad}} \approx 11.5\,\mathrm{mH} \tag{5.29}$$

$$L_{15\%_{SyM}} = 0.15\,\frac{140\,\Omega}{2\pi 150\,\mathrm{rad}} \approx 22.3\,\mathrm{mH} \tag{5.30}$$

2. **Evaluation of critical fault current slope:** this approach needs to evaluate the possible dc faults in the converter. For the MMC, three faults can be considered: two pole-to-ground and one pole-to-pole fault. The pole-to-ground faults can be evaluated with the circuit equations (5.1), and (5.2) changing the pole-to-ground voltages, V_1^{dc} and V_2^{dc}, to zero. The pole-to-pole faults are analyzed with the equivalent circuit loop. The fault with the greater current slope is in the case of a fault pole-to-pole. The equation that describes the pole-to-pole fault in the MMC is:

$$V_u + L\left(\frac{d}{dt}I_u\right)_{crit} + R\,I_u + V_l + L\left(\frac{d}{dt}I_l\right)_{crit} + R\,I_l = 0 \tag{5.31}$$

Neglecting the voltage drop in the resistances and replacing the arm voltages with the voltages at the fault instant, the expression relating the critical fault current slope and the arm inductance is:

$$2\,L\left(\frac{d}{dt}I\right)_{crit} \approx -V_u - V_l \approx -V^{dc} \tag{5.32}$$

where $(d/dtI)_{crit}$ is the equivalent short circuit current variation in the loop, assuming $\frac{d}{dt}I_u = \frac{d}{dt}I_l$. This is the equation presented in the literature for the MMC inductances [112]. Using a critical fault current slope of $6.4\,\mathrm{A/\mu s}$, found in (3.34), the arm inductance values for the MMCs on the bipole and SyM sides are:

$$L_{fault_B} = \frac{-V^{dc}}{2\,(di/dt)_{crit}} = \frac{525\,\mathrm{kV}}{2\,(6.4\,\mathrm{A/\mu s})} = 41\,\mathrm{mH} \tag{5.33}$$

$$L_{fault_{SyM}} = \frac{-V^{dc}}{2\,(di/dt)_{crit}} = \frac{640\,\text{kV}}{2\,(6.4\,\text{A/µs})} = 50\,\text{mH} \tag{5.34}$$

Using the proposed approaches, two values for the arm inductance were found: $L_{15\%}$ and L_{fault}. The value using the 15% of Z_{base} is considerably smaller than the fault-current-related value. It is worth mentioning that this recommended inductance, $L_{15\%}$, value comes from MMCs operating at 50 Hz [112, 119], while a 150 Hz MMC is considered in this thesis.

Assuming that the restrictions related to the fault current detection remain unchanged from the 50 Hz applications, e.g. current measurements delays, processing time, and semiconductor switches restrictions, the arm inductance value calculated with the equivalent fault circuit is preferred. Hence, the arm inductances considered for the bipole and SyM are L_{fault_B} and $L_{fault_{SyM}}$ respectively.

5.4.3 Capacitor in the sub-modules

As presented in Section 3.5.3, the equivalent capacitor C_{eq} can be found with the maximum dynamic variation of energy in the arm (ΔW), the voltage ripple (ϵ), the number of SMs (N_{SM}), and the average voltage per SM (V_{SM}).

The maximum energy dynamic variation ΔW can be found from the steady-state analysis, replacing the arm voltages (5.9), (5.10), and the arm currents (5.20), (5.21) in the expression of the energy variation (3.37). The voltage ripple considered in this thesis is 10%. The number of SM has been found in (5.24) and (5.25) for the arms for the MMC connected to the bipole and the SyM respectively. As previously stated, the voltage per SM is considered to be 1.6 kV.

Using the aforementioned values in the equivalent capacitance expression (3.35), the values found for both MMCs are:

$$C_{eq_B} \approx 5.28\,\text{µF} \tag{5.35}$$

$$C_{eq_{SyM}} \approx 5.83\,\text{µF} \tag{5.36}$$

Using (5.24) and (5.25) the capacitance per SM for both MMCs are:

$$C_{SM_B} = C_{eq_B} \cdot N_{SM_B} \approx 1.7\,\text{mF} \tag{5.37}$$

$$C_{SM_{SyM}} = C_{eq_{SyM}} \cdot N_{SM_{SyM}} \approx 2.3\,\text{mF} \tag{5.38}$$

The values found in (5.37) and (5.38) are the minimal capacitances needed to operate under steady-state conditions. The values are smaller than the capacitances used in similar HVDC projects where the values are around 10 mF [123], because of the increased considered frequency (see Section 3.5.3).

Ideally, these reduced values of capacitance could reduce the volume of each SM and, in turn, reduce the total size of the dc-dc converter. But, it could be possible that only discrete steps of different sizes of capacitors are available. Furthermore, an industrial logic could lead to the use of a single size of capacitor over the complete converter, e.g. using 2.3 mF for the MMCs on the B and SyM side.

5.5 Control design

As introduced in Section 3.6, the control design is based on a diagonalized system. This section presents the diagonalization used for the MMCs in the F2F-MMC, needed to tune the energy and current controllers.

5.5.1 System diagonalization

The objective of this section is to diagonalize the model obtained in (5.3). First, a diagonal state matrix ($\boldsymbol{A}$) can be obtained using the procedure presented in Appendix A. The new model including the diagonal state matrix ($\boldsymbol{A_D}$) is expressed as:

$$\begin{aligned}\begin{bmatrix}\dot{I}_1\\ \dot{I}_2\end{bmatrix} = &\overbrace{\begin{bmatrix}-\frac{2R_{ac}+R}{2L_{ac}+L} & 0\\ 0 & -\frac{R}{L}\end{bmatrix}}^{\boldsymbol{A_D}}\begin{bmatrix}I_1\\ I_2\end{bmatrix}\\ &+\underbrace{\begin{bmatrix}-\frac{1}{2(2L_{ac}+L)} & \frac{1}{2(2L_{ac}+L)}\\ -\frac{1}{2L} & -\frac{1}{2L}\end{bmatrix}}_{\boldsymbol{B'}}\begin{bmatrix}V_u\\ V_l\end{bmatrix}\\ &+\begin{bmatrix}\frac{1}{2(2L_{ac}+L)} & -\frac{1}{2(2L_{ac}+L)} & -\frac{1}{2L_{ac}+L}\\ \frac{1}{2L} & \frac{1}{2L} & 0\end{bmatrix}\begin{bmatrix}V_1^{dc}\\ V_2^{dc}\\ V^{ac}\end{bmatrix}\end{aligned} \tag{5.39}$$

where I_1 ans I_2 are the new equivalent state variables ($\boldsymbol{x'}$). They are a linear combination of the upper and lower arm currents, which have been obtained with the transformation matrix $\boldsymbol{P}$:

$$\boldsymbol{P} = \begin{bmatrix} 1 & 1 \\ -1 & 1 \end{bmatrix} \quad \boldsymbol{P}^{-1} = \begin{bmatrix} \frac{1}{2} & -\frac{1}{2} \\ \frac{1}{2} & \frac{1}{2} \end{bmatrix} \tag{5.40}$$

To diagonalize the control matrix ($\boldsymbol{B'}$), the third method presented in Section 3.6.1 is used. The transformation matrix $\boldsymbol{T}$ is found with the following expression:

$$\boldsymbol{T} = \boldsymbol{B'}^{-1}\boldsymbol{B_D}$$

where $\boldsymbol{B_D}$ follows the structure suggested in (3.55).

$$\boldsymbol{T} = \begin{bmatrix} -(2L_{ac}+L) & -L \\ 2L_{ac}+L & -L \end{bmatrix} \begin{bmatrix} \frac{1}{2L_{ac}+L} & 0 \\ 0 & \frac{1}{L} \end{bmatrix}$$

$$\boldsymbol{T} = \begin{bmatrix} -1 & -1 \\ 1 & -1 \end{bmatrix} \tag{5.41}$$

with

$$\boldsymbol{T}^{-1} = \begin{bmatrix} -\frac{1}{2} & \frac{1}{2} \\ -\frac{1}{2} & -\frac{1}{2} \end{bmatrix} \tag{5.42}$$

Using $\boldsymbol{T}$ in (5.39), yields to:

$$\begin{aligned} \begin{bmatrix} \dot{I}_1 \\ \dot{I}_2 \end{bmatrix} = & \begin{bmatrix} -\frac{2R_{ac}+R}{2L_{ac}+L} & 0 \\ 0 & -\frac{R}{L} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \end{bmatrix} \\ & + \begin{bmatrix} \frac{1}{2L_{ac}+L} & 0 \\ 0 & \frac{1}{L} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} \\ & + \begin{bmatrix} \frac{1}{2(2L_{ac}+L)} & -\frac{1}{2(2L_{ac}+L)} & -\frac{1}{2L_{ac}+L} \\ \frac{1}{2L} & \frac{1}{2L} & 0 \end{bmatrix} \begin{bmatrix} V_1^{dc} \\ V_2^{dc} \\ V^{ac} \end{bmatrix} \end{aligned} \tag{5.43}$$

where V_1 and V_2 are the new control variables ($\boldsymbol{u'}$). They are a linear combination of the upper and lower arm voltages.

The new variables $1, 2$ can be expressed depending on the initial variables u, l with the following expressions:

$$\boldsymbol{I_{12}} = \boldsymbol{P}^{-1}\, \boldsymbol{I_{ul}}$$

$$\begin{bmatrix} I_1 \\ I_2 \end{bmatrix} = \begin{bmatrix} \frac{I_u - I_l}{2} \\ \frac{I_u + I_l}{2} \end{bmatrix} \tag{5.44}$$

$$\boldsymbol{I_{ul}} = \boldsymbol{P}\, \boldsymbol{I_{12}}$$

$$\begin{bmatrix} I_u \\ I_l \end{bmatrix} = \begin{bmatrix} I_1 + I_2 \\ -I_1 + I_2 \end{bmatrix} \tag{5.45}$$

$$\boldsymbol{V_{12}} = \boldsymbol{T}^{-1}\, \boldsymbol{V_{ul}}$$

$$\begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} \frac{-V_u + V_l}{2} \\ -\frac{V_u + V_l}{2} \end{bmatrix} \tag{5.46}$$

$$\boldsymbol{V_{ul}} = \boldsymbol{T}\, \boldsymbol{V_{12}}$$

$$\begin{bmatrix} V_u \\ V_l \end{bmatrix} = \begin{bmatrix} -V_1 - V_2 \\ V_1 - V_2 \end{bmatrix} \tag{5.47}$$

The physical interpretation of the new set of variables ($\boldsymbol{V_{12}}$ and $\boldsymbol{I_{12}}$) should be understood. From the expressions in (5.43), it can be noticed that the first resulting equation is only related to V^{ac} (assuming that $V_1^{dc} = V_2^{dc}$), and the second resulting equation is only related to the dc voltages.

The equations in (5.43) represent decoupled equivalent circuits that can be linked to closed paths in the initial converter topology. The physical interpretation of I_{12} can be established by following their path in the equivalent circuit, through the MMC as presented in Fig. 5.7.

The equivalent I_1 is related to the ac current exchanged with the external ac system, while I_2 is linked to the dc current as presented in Fig. 5.7. Both equivalent currents I_{12} may have ac and dc components but, the ac should not circulate on the dc systems. Similar to the equivalent circuit presented in Fig. 5.3, the equivalent ac currents, I_{12}^{ac}, have a close loop using the n-phase connection points, i.e. the upper and lower node (see Fig 5.2). In this case, I_1^{ac} has a complete close loop from the ac

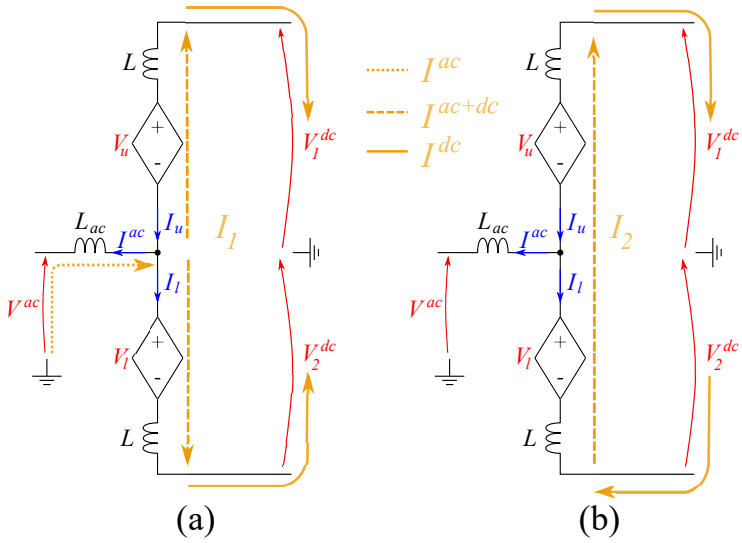


Figure 5.7: Physical interpretation for the equivalent currents (a) I_1 and (b) I_2.

system to the n-phase connection points. Current I_2^{ac} has no interaction with the external ac system, remaining inside the converter, between the nodes connecting the n-phases.

Similar to the ac components, the dc components must have an equivalent closed loop to circulate. In this case, the current I_1^{dc} has no close loop different from the one going through the ac system and the ground. To avoid the dc currents in the ac system, the current I_1^{dc} should be controlled to zero. The dc component of I_2 has a close loop on the converter dc side. Due to the superposition of ac and dc components, the arms in the MMC have ac currents with a dc offset, as presented in Fig. 5.7.

5.5.2 Energy control

The energy control keeps the converter energy controlled during the dynamic variations in the system such as dc voltage, change of power reference or fault events. The generalities of the energy control are explained in Section 3.6.2.

The diagonalized system expressed in (5.43) has decoupled the equivalent currents and voltages but, the arm energies remain coupled.

The energy per arm can be expressed as the energy in the equivalent capacitor:

$$E_u = \frac{1}{2} C_{eq_u} V_{C_{eq_u}}^2 \tag{5.48}$$

$$E_l = \frac{1}{2} C_{eql} V_{C_{eql}}^2 \tag{5.49}$$

As presented in Section 3.6.2 the energy dynamic variation can be linked to the power as follows:

$$\frac{d}{dt} E_u = V_u I_u = P_u \tag{5.50}$$

$$\frac{d}{dt} E_l = V_l I_l = P_l \tag{5.51}$$

From the initial mathematical model, presented in (5.3), it can be noticed that the arm powers are coupled as the upper arm current is linked to the lower arm current. The coupling using the new variables I_{12} and V_{12} can be evidenced in the following expressions:

$$P_u = -V_1 I_1 - V_1 I_2 - V_2 I_1 - V_2 I_2 \tag{5.52}$$

$$P_l = -V_1 I_1 + V_1 I_2 + V_2 I_1 - V_2 I_2 \tag{5.53}$$

where P_u and P_l are found using (5.45) and (5.47).

It can be noticed that the power in one arm depends on a combination of the equivalent decoupled voltages, V_{12}, and currents, I_{12}. From the physical interpretation of the equivalent currents presented in Fig. 5.7, there is no current that can control the energy in the arm independently from the other. To simplify the energy control, an energy transformation ($\boldsymbol{W_T}$), is used. The energy transformation is a linear combination of the arms energy. The $\boldsymbol{W_T}$ chosen for the MMC control is given by:

$$\boldsymbol{W_T} = \begin{bmatrix} 1 & 1 \\ 1 & -1 \end{bmatrix} \tag{5.54}$$

Using $\boldsymbol{W_T}$, the new set of energies is obtained:

$$\frac{d}{dt} \begin{bmatrix} E_\Sigma \\ E_\Delta \end{bmatrix} = \boldsymbol{W_T} \begin{bmatrix} P_u \\ P_l \end{bmatrix} = \begin{bmatrix} P_u + P_l \\ P_u - P_l \end{bmatrix} \tag{5.55}$$

Replacing (5.52) and (5.53) in (5.55), yields to:

$$\frac{d}{dt} E_\Sigma = -2 \left(V_1 I_1 + V_2 I_2 \right) \tag{5.56}$$

$$\frac{d}{dt}E_{\Delta} = -2\left(V_1 I_2 + V_2 I_1\right) \tag{5.57}$$

where V_{12} and I_{12} have ac and dc components. As mentioned before, the physical interpretation of the equivalent currents determines their use and their reference in the control strategy. With the energy transformation, it is possible to use the equivalent currents I_{12} to control the equivalent energies. The energy control is detailed below.

Following the generalities presented in Section 3.6.2, the different energy controllers, $K_E(s)$, use a PI controller and a notch filter to avoid the first and second harmonic in the measurement (see Fig. 3.10).

Total energy

As stated in Section 3.6.2, the energy controllers are designed to follow and control the average values of the energy over time. Considering only the dc and fundamental frequency components, the average value of the total energy, obtained in (5.56), is:

$$\begin{aligned}\left\langle \frac{d}{dt}E_{\Sigma} \right\rangle = -2V_1^{dc}I_1^{dc} - 2V_2^{dc}I_2^{dc} - 2\frac{V_1^{ac}\,I_1^{ac}}{2}\cos\left(\theta_{V_1} - \theta_{I_1}\right) \\ - 2\frac{V_2^{ac}\,I_2^{ac}}{2}\cos\left(\theta_{V_2} - \theta_{I_2}\right)\end{aligned} \tag{5.58}$$

Neglecting the voltage drop on the resistances, the mathematical model (5.43) represents a set of equations where the voltage V_i is in quadrature with the current I_i (for $i \in [1, 2]$). Then, the average value of $V_i^{ac}I_i^{ac}$ is zero and (5.58) can be simplified as:

$$\left\langle \frac{d}{dt}E_{\Sigma} \right\rangle = -2\left(V_1^{dc}I_1^{dc} + V_2^{dc}I_2^{dc}\right) \tag{5.59}$$

Following this analysis, the total energy per leg should be controlled either with I_1^{dc} or I_2^{dc}, but I_1^{dc} should be controlled to zero to avoid dc currents on the ac side. In consequence, E_{Σ} is controlled with I_2^{dc}. Additionally, the dc steady-state voltages in the upper and lower arm are equal, see (5.7), thus $V_1^{dc} = V_u^{dc} - V_l^{dc} = 0$. In consequence, the relation between the total energy and I_2^{dc} is:

$$\left\langle \frac{d}{dt}E_{\Sigma} \right\rangle = -2V_2^{dc}I_2^{dc} \tag{5.60}$$

Using (5.48) and (5.49), the energy reference for this control loop corresponds to:

$$E_{\Sigma}^{ref} = \frac{1}{2}\left(C_{eq_u} V_{C_{eq_u}}^{nom\ 2} + C_{eq_l} V_{C_{eq_l}}^{nom\ 2}\right) \tag{5.61}$$

where $V_{C_{eq_u}}^{nom}$ and $V_{C_{eq_l}}^{nom}$ are the nominal voltages of the arm equivalent capacitance for the upper and lower arm respectively.

The current reference can be obtained from the energy controller following (3.78), in this case the reference for I_2^{dc} has the following structure:

$$I_2^{dc\,ref} = -\frac{P_{E_{\Sigma}}^{ref}}{2\,V_2^{dc}} \tag{5.62}$$

where $P_{E_{\Sigma}}^{ref}$ is the output from the energy controller, and V_2^{dc} in steady-state is:

$$V_2^{dc} = -\frac{V_u^{dc} + V_l^{dc}}{2} = -\frac{V^{dc}}{2} \tag{5.63}$$

The structure for the total energy controller is presented in Fig. 5.8.

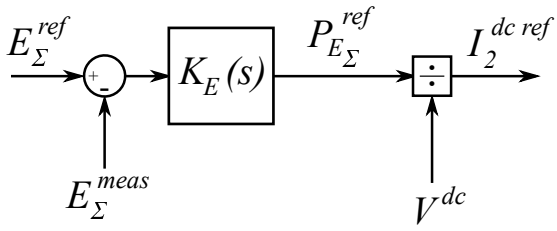


Figure 5.8: Total energy controller and the relation with the current reference $I_2^{dc\,ref}$.

Energy difference

Contrary to the total energy, the average value of E_{Δ} is given by the ac power, as V_1^{dc} and I_1^{dc} are controlled to zero. $\langle d/dt\, E_{\Delta} \rangle$ given by:

$$\begin{aligned}\left\langle \frac{d}{dt} E_{\Delta} \right\rangle =& -2V_1^{dc} I_2^{dc} - 2V_2^{dc} I_1^{dc} - 2\frac{V_1^{ac}\, I_2^{ac}}{2}\cos\left(\theta_{V_1} - \theta_{I_2}\right) \\ & - 2\frac{V_2^{ac}\, I_1^{ac}}{2}\cos\left(\theta_{V_2} - \theta_{I_1}\right) \\ \left\langle \frac{d}{dt} E_{\Delta} \right\rangle =& -0 - 0 - V_1^{ac}\, I_2^{ac}\cos\left(\theta_{V_1} - \theta_{I_2}\right) \\ & - V_2^{ac}\, I_1^{ac}\cos\left(\theta_{V_2} - \theta_{I_1}\right)\end{aligned} \tag{5.64}$$

As I_1^{ac} has a direct relation with the current I^{ac}, it is used to control the power exchanged with the ac system. To control E_Δ, the current I_2^{ac} is used. As it was mentioned above, the ac component of I_2 is kept circulating inside the converter assuming that the internal ac system is balanced between the converter legs.

Considering that the equivalent capacitance in the upper arm is equal to the lower arm, the reference for E_Δ should be zero. The current reference and its relation with the energy controller can be expressed as:

$$I_2^{ac\,ref} = -\frac{P_{E_\Delta}^{ref} + V_2^{ac}\, I_1^{ac} \cos\left(\theta_{V_2} - \theta_{I_1}\right)}{V_1^{ac} \cos\left(\theta_{V_1} - \theta_{I_2}\right)} \tag{5.65}$$

where $P_{E_\Delta}^{ref}$ is the output of the energy controller.

The structure linking the E_Δ controller with the current reference $I_2^{ac\,ref}$ is presented in Fig. 5.9. As mentioned in Chapter 3 the controllers are implemented for the n legs of the converter. The output of the n controllers is feed to the matrix $\boldsymbol{M_k}$, which assures the balance between the legs [136]. As explained in Section 3.6.2, the energy controllers have a PI structure, following the average value only. The energy controller sets the magnitude of the ac current but its oscillation and phase is set from the steady-state analysis with $\cos\left(\omega t + \theta_{I_2}\right)$, where the angle is set from the ac steady-state found in Section 5.3.2. It is worth noting that the power feed forward, $\langle V_2^{ac} I_1^{ac} \rangle$, helps the controller to avoid violent transients or saturation but, without the feed forwards the PI controllers can reduce the error in steady-state. The rest of the values can be obtained from the steady-state analysis (see Section 5.3).

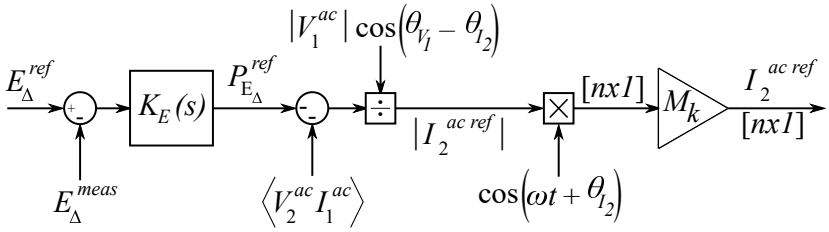


Figure 5.9: MMC energy difference controller and its relation with the current reference $I_2^{ac\,ref}$.

5.5.3 Current control

From the mathematical model (5.43) two current control loops can be designed, one per equivalent current. The general transfer function depends on the equivalent inductance (L_{eq}), resistance (R_{eq}), and voltage (V_{eq}). The PIR controller, $K_I(s)$, used for the current control (3.82), can be tuned with the parameters presented in Table 5.1. Where ϕ_{PM} is the desireed phase margin at the resonance frequency and T_d is the discretization time of the controller. The control loops are presented in Fig. 5.10.

Table 5.1: Parameters to tune the current controllers

	L_{eq}	R_{eq}	V_{eq}	ϕ_{PM}	T_d
I_1	$2\,L_{ac}+L$	$2\,R_{ac}+R$	$V_1+\frac{V_1^{dc}-V_2^{dc}}{2}-V^{ac}$	60°	40 µs
I_2	L	R	$V_2+\frac{V_1^{dc}+V_2^{dc}}{2}$		

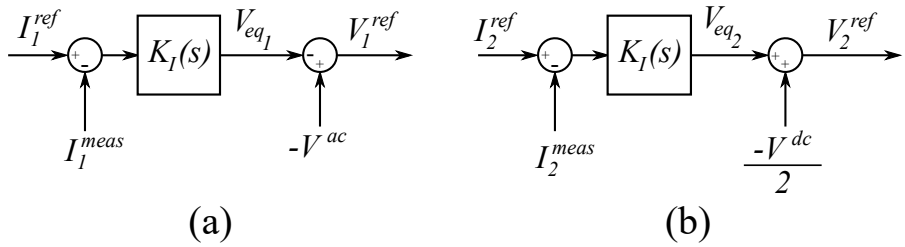


Figure 5.10: Current controllers for (a) I_1, and (b) I_2. The feed forwards show the equivalent voltage in steady-state, the complete term can be found from V_{eq} in Table 5.1.

5.5.4 Power control

As previously stated, the power is controlled with the ac current. For the MMC studied here, I_1^{ac} is used. The ac current is generated from the references in the dq0 frame, using an invariant-power park transformation aligned with the q-axis, the current references can be obtained as follows:

$$I_d^{ac\,ref} = \frac{P^{ref}}{V_d} \tag{5.66}$$

$$I_q^{ac\,ref} = -\frac{Q^{ref}}{V_d} \tag{5.67}$$

where the relation between the ac current and I_1^{ac} is:

$$I_1^{ac} = \frac{I^{ac}}{2} \tag{5.68}$$

Thus, $I_d^{ac\,ref}$ and $I_q^{ac\,ref}$ are used to generate $I_1^{ac\,ref}$ though an inverse park transformation.

The control implemented in the simulation model uses a first order low pass filter, with $\tau = 10$ ms, for the power references.

5.5.5 Control of the front-to-front with three MMCs

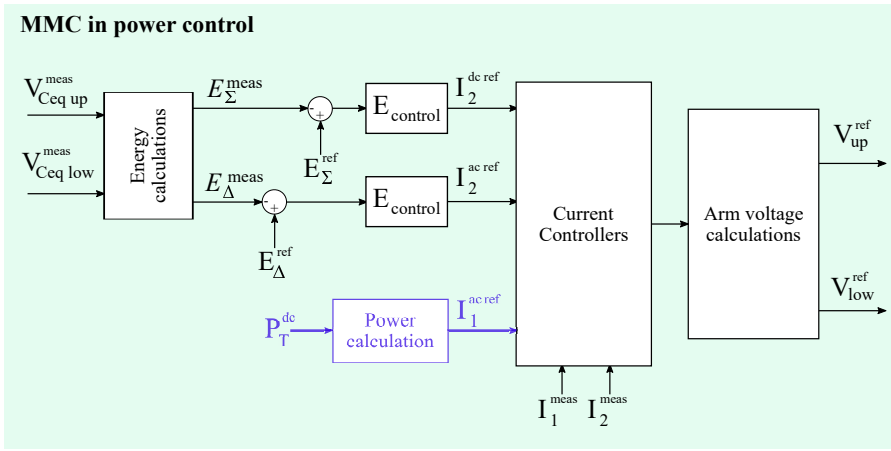
The particular structure of the F2F-MMC considered in this thesis has been presented in Fig. 5.1. The two converters connected to the bipole line are in power control (see Fig. 5.11a). The metallic return in the B line decouples the dc current of positive and negative pole thus, both MMCs can be define their power exchange independently.

As the power through the two MMCs connected to the bipole is controlled, the MMC on the monopole side sets the ac voltage reference, see Fig. 5.11b. The MMC connected to the SyM acts as a slack bus providing adequate, P and Q, power exchange to keep the ac system stable.

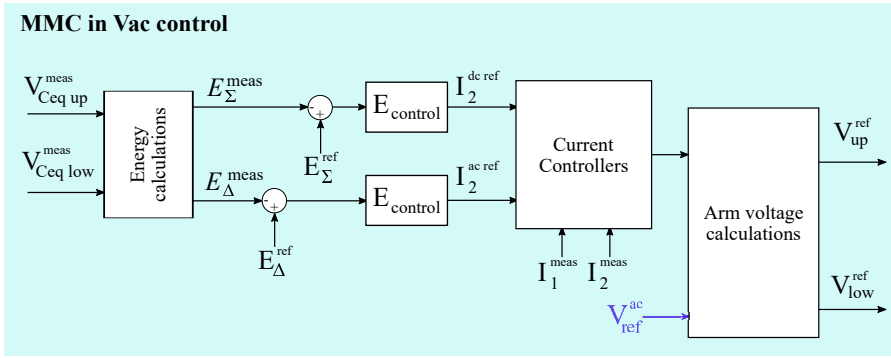
Setting the ac voltage with the MMC connected to the SyM allows maintaining an ac reference even if the MMCs connected to the bipole are blocked. This is convenient in case of a fault in a pole of the bipole, to have an immediate redundancy. In case of a fault in the SyM, as no system reconfiguration is considered in this thesis, the complete F2F-MMC is blocked and the power exchange is stopped.

5.6 Case study simulations and results

The performed simulations follow the case study and scenarios proposed in Chapter 4. The F2F-MMC is used to interconnect a bipole with a SyM. The system considered is presented in Fig. 5.12 indicating the five converter stations and the positive conventions for the power flow direction (PFD). The main characteristics of the dc-dc converter are presented in Table 5.2.



(a)



(b)

Figure 5.11: Control strategy implemented for (a) the MMCs connected to the bipole line and (b) the MMC connected to the SyM.

Three sets of simulations are performed to verify the control and converter behavior in nominal, normal, and faults operation. The simulations in nominal operation are performed to verify the converter design, the results are presented in Appendix B.1. The main results in normal and fault scenarios are presented in the following sections.

5.6.1 Normal operation

The normal operation is different from the nominal operation in that the power exchanged through the F2F-MMC is not the rated power. The normal operation simulations consider a power flow through the dc-dc converter of 500 MW, which is equivalent to 71% of the converter rated power. The power-controlled station on the bipole line has a power refer-

ence at 900 MW, while on the SyM line the power reference is 200 MW. These references leave a margin to deal with the 500 MW through the F2F-MMC without exceeding the line rated power.

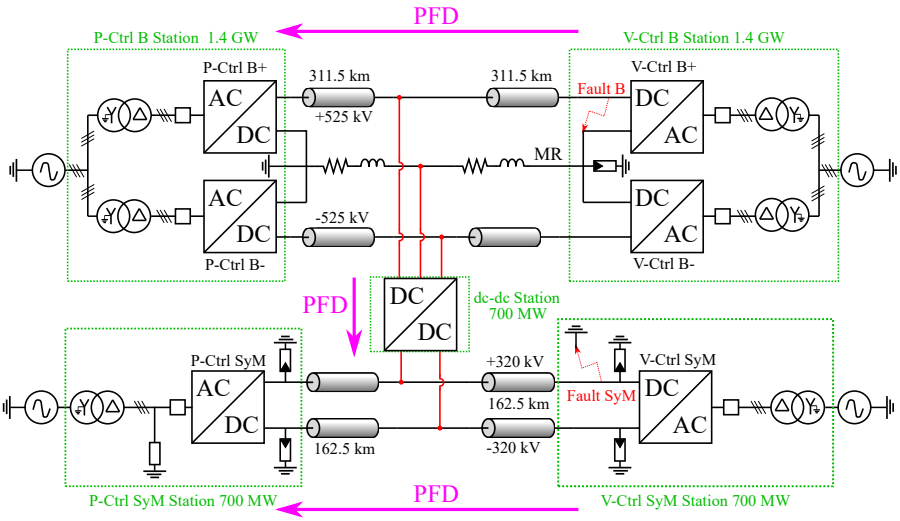


Figure 5.12: Case study system proposed for this thesis and the positive convention for the power flow directions (PFD), see Chapter 4.

Table 5.2: Main parameters of the MMCs constituting the F2F converter.

Parameters	Value	
	MMC Bipole (one per pole)	MMC SyM
Power	350 MW	700 MW
$V_1^{dc} = V_2^{dc}$	262.5 kV	320 kV
U^{ac}	225 kV	313.5 kV
L_{ac}	15.5 mH	14.9 mH
Operating frequency	150 Hz	
N_{legs}	3	

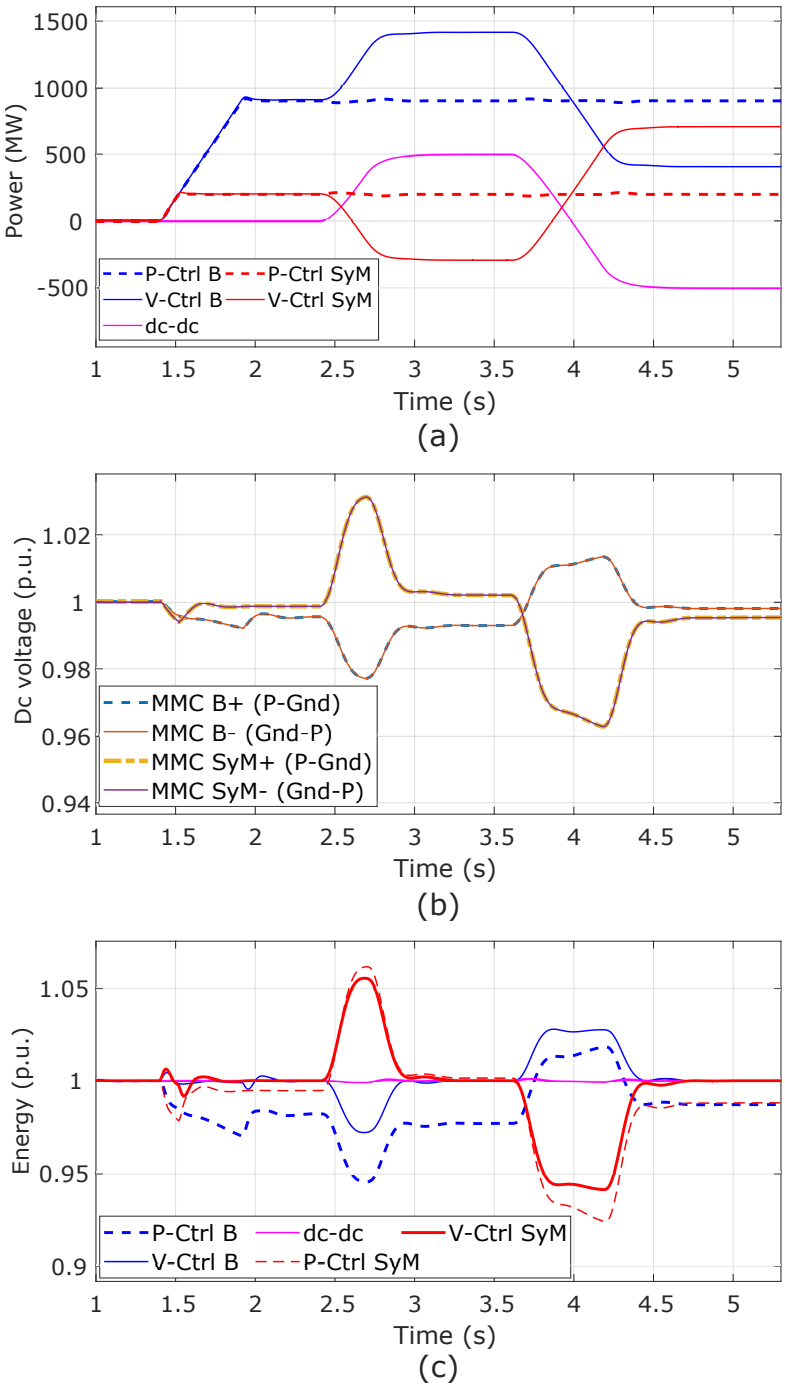


Figure 5.13: Results for the normal operation of Case 3. (a) the power per converter station, (b) the dc voltage at the terminals of the MMCs of the F2F, and (c) the energy per converter station.

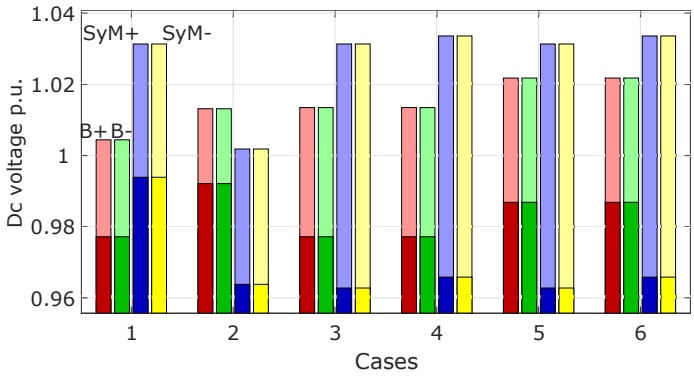


Figure 5.14: Maximum (light bars) and minimum (dark bars) pole-to-ground dc voltage registered in the F2F for the six cases of normal operation (see Table 4.4). Red, green, blue, and yellow are the voltages of the positive pole of the bipole, negative pole of the B, the SyM positive pole, and SyM negative pole respectively.

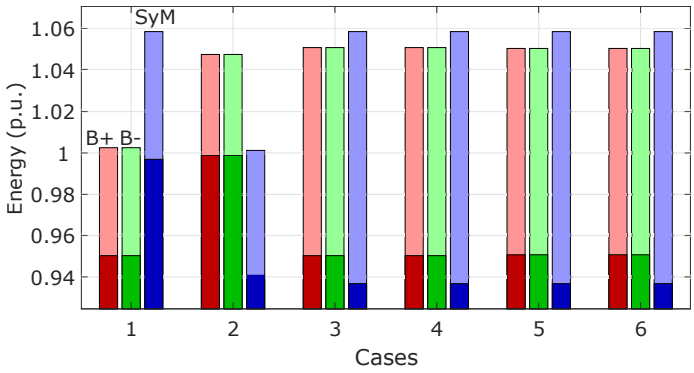


Figure 5.15: Maximum (light bars) and minimum (dark bars) energy per MMC in the F2F for the six cases of normal operation (see Table 4.4). Red, green and blue are the MMCs connected to the positive pole of the bipole, negative pole of the B, and the SyM respectively.

The normal operation is tested simulating six scenarios where the power flow directions in the system are changed (see Table 4.4). From the simulated scenarios, Case 3 presents the greatest dc voltage dynamic variations (worst case). The system results, for Case 3 (see Table 4.4), are presented in Fig. 5.13. The power through the five converter stations is presented in Fig. 5.13a. The bipole line starts with a positive power

flow of 900 MW at 1.4 s, while the SyM line only has 200 MW. At 2.4 s the F2F-MMC exchanges 500 MW in both directions according to the Case 3.

The dc voltages measured at the terminals of the F2F-MMC are presented in Fig. 5.13b. Small dc voltage dynamic variations are present during the change of power reference. The steady-state dc voltages are not 1 p.u. as small voltages differences are needed to create a power flow in the dc system. The dc voltage on the SyM side has a bigger dynamic variation (4%) compared to the voltage variations on the B (2%), due to the cable equivalent capacitance. The total equivalent cable capacitance for the cable on the SyM, 42.5 µF, is roughly half of the capacitance on the B side, 84.8 µF, which is mainly linked to the length of the cables.

The energy per converter station is presented in Fig. 5.13c, normalized to their nominal values. The energy on the voltage-controlled stations and the dc-dc converter follow their respective nominal values while the power-controlled stations have steady-state conditions different from the nominal, due to the virtual capacitor control [137]. The detailed F2F-MMC results are presented in Appendix B.2.

The voltage dynamic variations measured at the terminals of the MMCs of the F2F, for the six cases of normal operation, are presented in Fig. 5.14. The measurements are within a margin of ±5%, which do not represent a problem to the system or the converter.

The dynamic energy variations per MMC in the F2F are presented in Fig. 5.15. Similar to the voltage variations, the energy fluctuations are within operational range and do not represent a problem to the MMCs.

5.6.2 Fault scenarios

Following the power flow direction variations presented in Table 4.5, eight cases where simulated for a fault on the bipole and additional eight cases for a fault on the SyM. The results are presented in the following subsections.

Fault on the bipole line

For the cases where the fault is on the bipole side, the dc-dc converter should avoid disturbances on the healthy zones, i.e. the healthy pole of the bipole and SyM line. To do so, the F2F-MMC should block only the MMC connected to the faulted pole while the other two MMCs continue to operate. From the eight simulated cases, Case 1 is the scenario

presenting the greatest dynamic variations of the dc voltage in the SyM side during the fault event. The results for this case are represented the worst conditions.

The results for the Case 1 (see Table 4.5), are presented in Fig. 5.16. The power per converter station is presented in Fig. 5.16a. The simulation begins ramping up the power flow in the lines to 900 MW for the bipole and 200 MW for the SyM. Then, the F2F-MMC starts to exchange 500 MW from the bipole to the SyM line. At 3.7 s, a fault on the positive pole of the bipole is simulated. During the fault, the bipole line has a power disturbance due to the loss of 450 MW from the faulted pole. The power oscillations are present until the ACCBs, adjacent to the ac-dc converters, are opened avoiding the rectification of the ac currents into the fault (100 ms after the fault detection).

During the fault, the power in the F2F-MMC also has power oscillations due to the internal ac system feeding the fault (see Fig. 5.6). Similar to the bipole line, the oscillations in the F2F-MMC are eliminated once the internal ACCBs are opened and the fault is isolated. As mentioned previously, the time to open the internal ACCBs is 30 ms, and the faster the time to open, the better results can be obtained. For opening times longer than 30 ms, the fault transient on the SyM can trip the line protection, blocking the complete F2F-MMC (similar to a fault on the SyM). After the fault, the healthy MMCs in the F2F recover steady-state conditions exchanging 250 MW from the healthy pole of the B ($3.8\,s < t < 4.2\,s$). The reference of the F2F-MMC is changed to 700 MW at 4.2 s, i.e. the rated power but, as the system has lost a pole, only 350 MW are exchanged.

The SyM line reacts to the fault in the bipole as if it is a power disturbance, the voltage-controlled station adapts its power exchange to keep the dc voltage in the line. During the transient both converter stations in the SyM line are affected with the fault on the bipole, but the disturbance is not high enough to trigger the blocking signals, according to the operating limits defined in Section 4.3.6.

The F2F-MMC considered in this thesis, i.e. one MMC per pole on the bipole side, allows to have and immediate redundancy, because a fault in a pole does not trigger the blocking signal on the healthy pole. It can be noticed that the power exchanged through the F2F-MMC does not stop during the fault. After the fault, the F2F-MMC operates in degraded mode, as it is equivalent to the interconnection between an AM and a SyM.

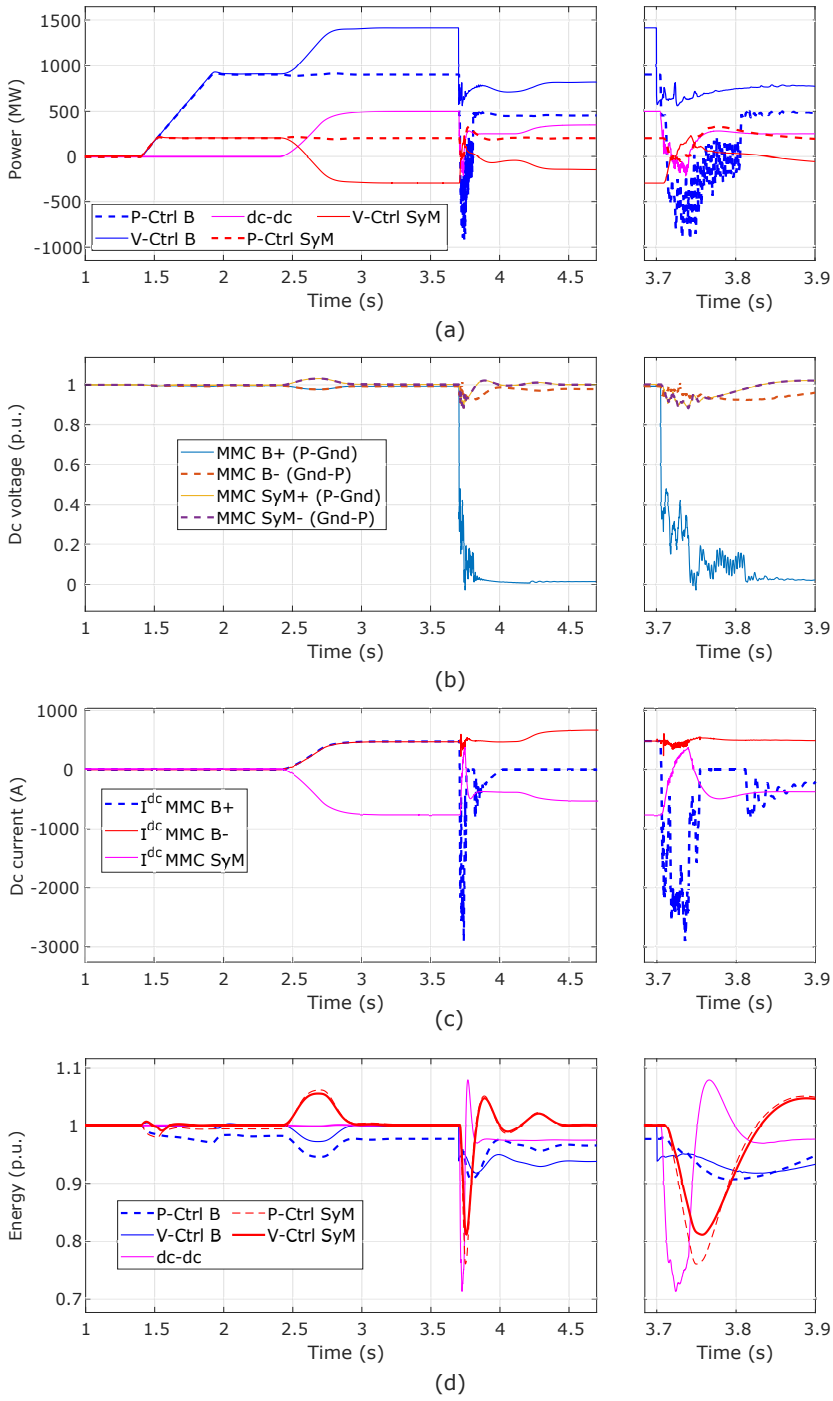


Figure 5.16: Results for the Case 1 when the fault is on the bipole line (see Table 4.5). (a) the power per converter station (b) the dc voltage at the terminals of the MMCs of the F2F, and (c) the dc current at the terminals of the F2F-MMC. (d) the energy per converter station.

The voltages measured at the terminals of the MMCs in the F2F are presented in Fig. 5.16b. At the instant of the fault, the voltage in the positive pole of the B drops to zero having oscillations. These oscillations are mainly driven by the rectified ac currents through the ac-dc converters. The oscillations are cleared once the ACCBs, adjacent to the ac-dc converters, are opened. The healthy zones have some dc voltage disturbances but, they are capable to recover steady-state conditions without triggering their fault detection thresholds. After the fault, the dc voltages on the healthy zones have additional disturbances due to the change of the power reference in the F2F-MMC.

The dc currents are presented in Fig. 5.16c. It can be noticed that the current in the faulted pole increases up to 3 kA before the MMC is blocked. The healthy pole has small disturbances while the ACCB is opened but, it follows the power reference. The current on the SyM converter changes of polarity around 3.75 s to feed the fault through the freewheeling diodes. After opening the ACCB, the current on the SyM recovers normal conditions extracting from the healthy pole of the bipole.

The energy per converter station is presented in Fig. 5.16d. The energy in the converters is also disturbed by the changes in the power references. At the time of the fault, the energy in the five converter stations are disturbed. After the fault, the energies in the B and the dc-dc converter cannot recover steady-state conditions because they have lost half (a third for the case of the F2F) of the converters considered per station, see Fig. 5.12. During the fault, the converters connected to the faulted pole have partially discharged, as these converters have been blocked, it is not possible to use the control to charge them again.

The detailed F2F-MMC results are presented in Fig. 5.17. The ac currents in MMC connected to the positive pole of the B are presented in Fig. 5.17a. It can be noticed that the magnitude of the currents increases after the fault at 3.7 s as the ac currents are rectified to feed the fault. The ac currents presented in Fig. 5.17a are stopped with the opening of the internal ACCB, 30 ms after the fault detection. The ac currents in the MMC connected to the negative pole of the B and the MMC connected to the SyM, Fig. 5.17b-c, have disturbances while the ACCB isolate the faulted pole. If the internal ACCB is not fast enough to avoid the rise of the arm currents on the healthy zones, the complete F2F-MMC could be blocked. The FBC of this structure is dependent on the coordination with the internal protection devices. After the fault transient, the ac currents are controlled to regain steady-state conditions.

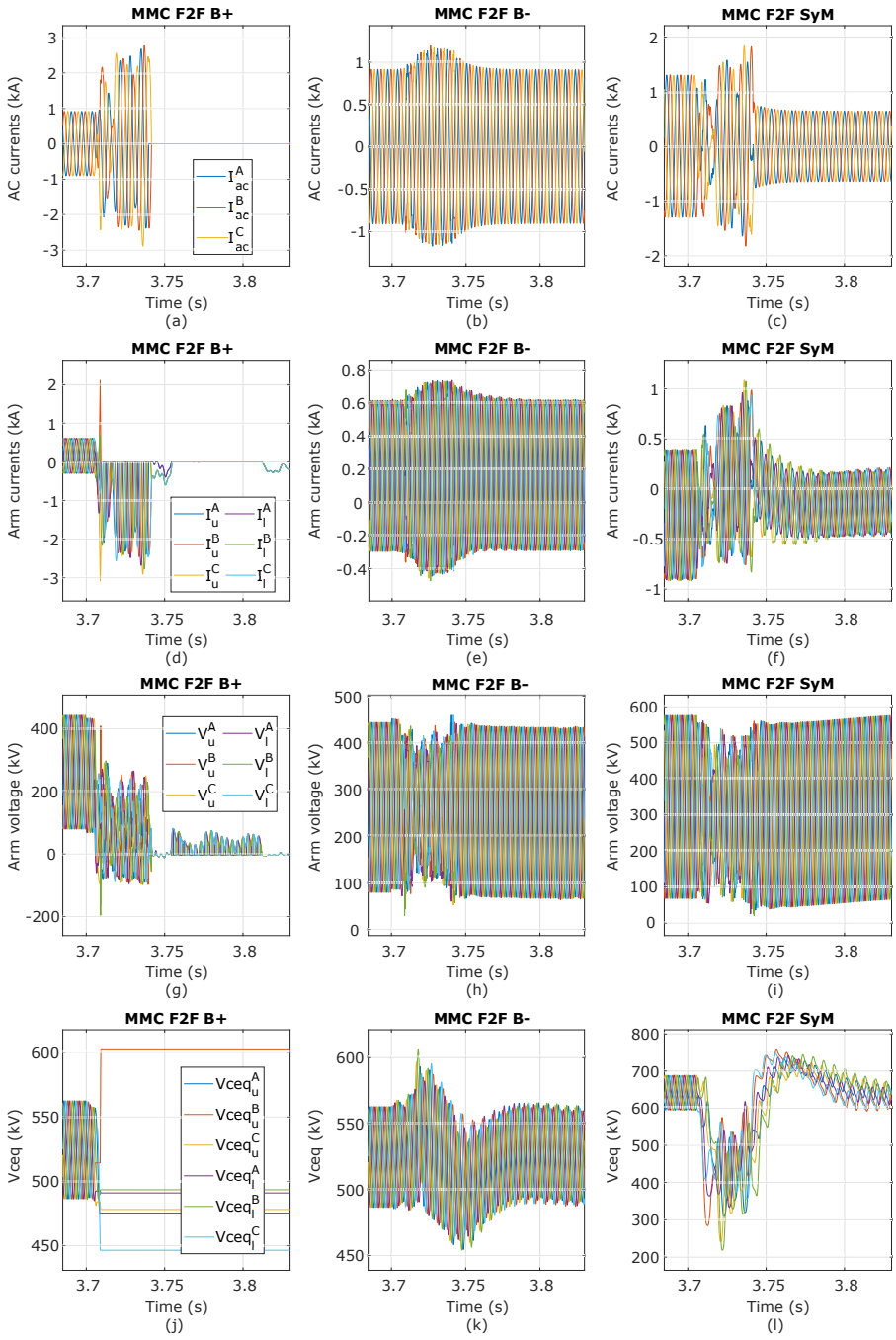


Figure 5.17: Ac currents (first row), arm currents (second row), arm voltages (third row), and the voltage of the equivalent arm capacitor for the three MMCs in the F2F for the Case 1 when the fault is on the bipole line (see Table 4.5).

The arm currents are presented in the second row of Fig. 5.17. It can be evidenced that the currents in the MMC connected to the faulted pole, Fig. 5.17d, are rectified ac currents from the time when the converter is blocked (a few ms after the fault) to the instant when the ACCB is opened. Disturbances of about 200 A can be observed at the instants when the ACCBs are opened, i.e. at ∼3.75 s for the ACCB in the F2F and ∼3.82 s for the ACCBs on the bipole line (Fig. 5.17d). The disturbances are induced by voltage variations through the cable. The arm currents in the healthy MMCs, presented in Fig. 5.17e, f, show the fault disturbance and how the currents are controlled to regain steady-state conditions.

The voltages measured at the arm terminals are presented in the third row of Fig. 5.17. The arm voltages in the MMC connected to the positive pole of the bipole have disturbances during the fault event until the ACCBs are opened. Negative voltages can be detected, these voltages are set by the ac system and not by the arm modulation as they are blocked and only HBSMs are considered. The MMCs connected to the negative pole of the bipole and the SyM are capable to regain steady-state ∼500 ms after the fault event (not shown in Fig. 5.17).

The voltage in the equivalent arm capacitor is presented in the fourth row of Fig. 5.17. When the MMC connected to the faulted pole is blocked, the steady-state oscillations in the voltages of the equivalent arm capacitor stop, and can be discharged or charged depending on the current direction in the arm. In Fig. 5.17d, it can be evidenced that the arms currents are negative, discharging most of the capacitors. The current in the upper arm of phase B has a positive peak that charges the equivalent capacitor in that arm, presented in Fig. 5.17j. The overvoltage on this capacitor represents 14% of the rated voltage, which could be acceptable for the semiconductor switches rating, i.e. twice the average operating voltage.

For the different fault scenarios proposed in Table 4.5, the F2F-MMC is able to maintain the healthy zones operational, i.e. the fault does not propagate through the dc-dc converter. The maximum and minimum dc voltages measured at the terminals of the F2F-MMC are presented in Fig. 5.18. The maximum and minimum energy measured per MMC in the F2F are presented in Fig. 5.19.

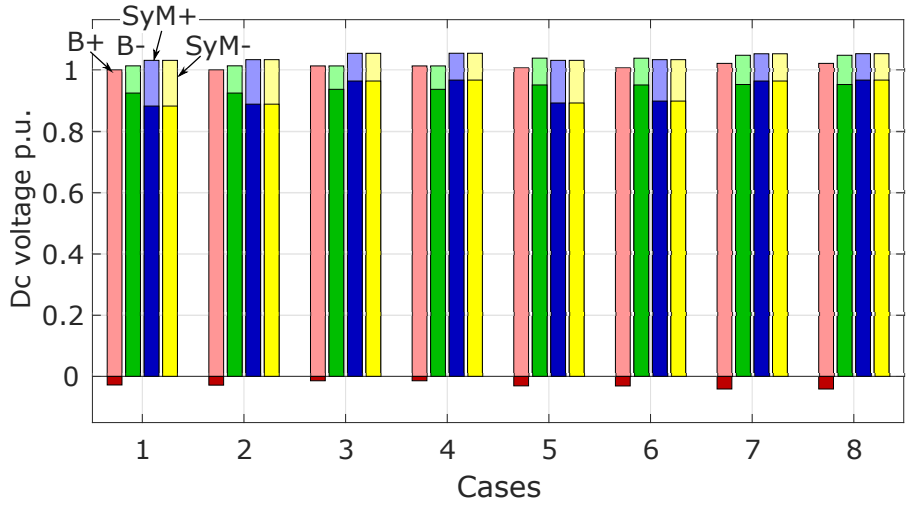


Figure 5.18: Maximum (light bars) and minimum (dark bars) pole-to-ground dc voltage registered in the F2F for the eight cases when the fault is located on the B line (see Table 4.5). Red, green, blue, and yellow are the voltages of the positive pole of the bipole, negative pole of the B, the SyM positive pole, and SyM negative pole respectively.

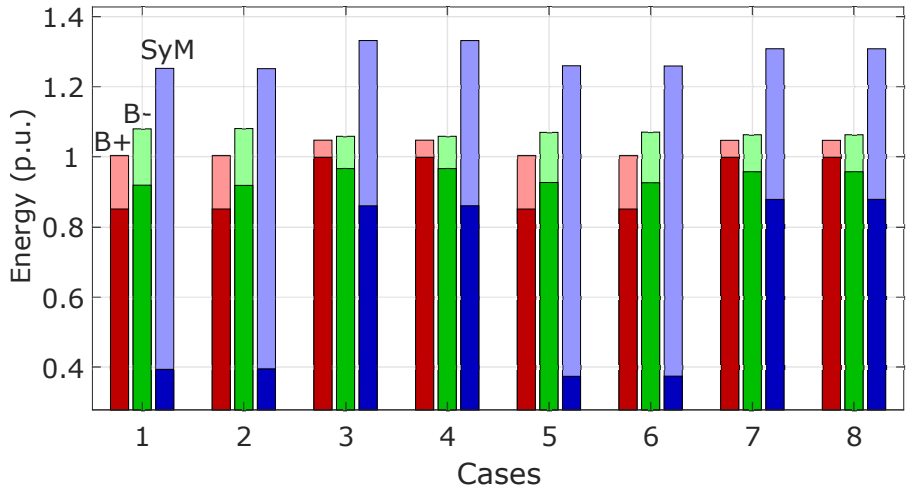


Figure 5.19: Maximum (light bars) and minimum (dark bars) energy per MMC in the F2F for the eight cases when the fault is located on the B line (see Table 4.5). Red, green and blue are the MMCs connected to the positive pole of the B, negative pole of the B, and the SyM respectively.

Fault on the symmetric monopole line

The eight power flow conditions proposed in Table 4.5 have been simulated for a fault on the SyM line. The results for Case 4 are presented in this section, as it is the case with worst performances (having the greatest dynamic variations).

For a fault on the SyM, the F2F-MMC is completely blocked as the degraded operation is not possible. A system reconfiguration is can be done if the faulted part of the system is isolated but, this is not considered a degraded mode as it does not change the line topology at the terminals of the dc-dc converter (see Section 1.5). The main objective of the F2F-MMC is to preserve the healthy zones without triggering their blocking signals. For a fault on the SyM side, the healthy zones are the positive and negative pole of the bipole (see Fig. 4.8).

The system results for Case 4 are presented in Fig. 5.20. The power per converter station is presented in Fig. 5.20a. For Case 4 the power in the bipole is positive while the power in the SyM and through the dc-dc is negative (see positive conventions in Fig. 5.12). At the instant of the fault, the SyM line and the F2F-MMC are blocked. The bipole line sees the fault as a power disturbance that is damped by the voltage-controlled station. After the fault, the bipole line regains steady-state conditions as if the dc-dc converter was not connected, i.e. the power on the voltage-controlled is equal to the power in the power-controlled station.

The dc voltage measured at the terminals of the MMCs in the F2F is presented in Fig. 5.20b. The voltages have small perturbations, less than 10%, at every change of power reference. At the time of the fault, 3.7 s, the voltages pole-to-ground in the SyM are disturbed triggering the blocking signals in the line and the F2F-MMC. The faulted pole, the yellow continuous line in Fig. 5.20b, drops to zero after a fast transient. The negative pole of the SyM is also disturbed reaching over 2 p.u. at the first ms. These transients could be dangerous for the equipment installed in the F2F-MMC. As mentioned in Chapter 4, the case study uses overvoltage protections at the terminals of the ac-dc converters in the SyM but, the dc-dc converter does not have. To avoid large overvoltages at the terminals of the F2F-MMC additional surge arresters must be installed. These elements belong to the protection strategy, which is out of the scope of this thesis. The dc-dc converter was simulated without surge arresters to study the worst scenarios. On the other hand, the voltages on the bipole have a disturbance of less than 7%, allowing the line to recover steady-state conditions under one second.

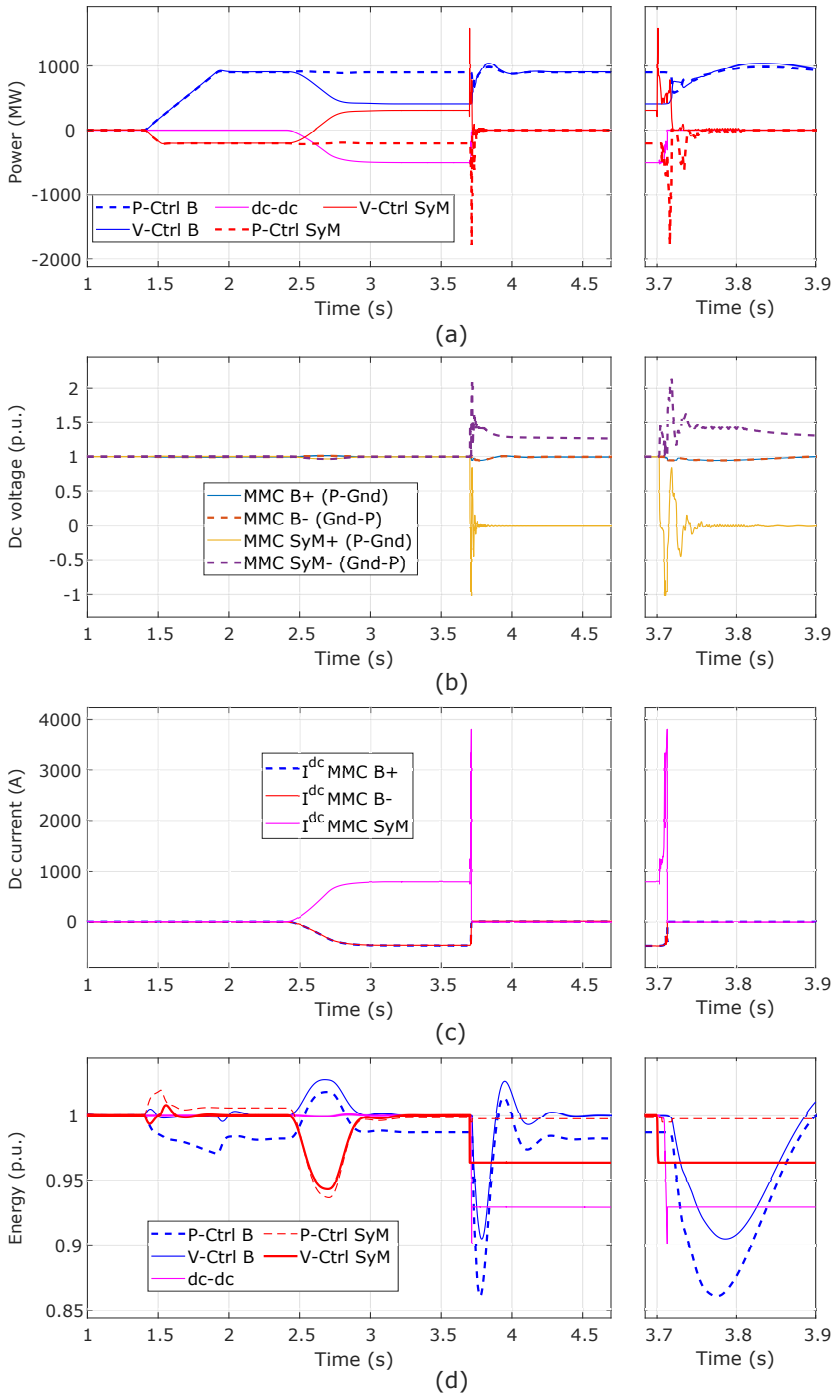


Figure 5.20: Results for the Case 4 when the fault is on the SyM line (see Table 4.5). (a) the power per converter station, (b) the dc voltage at the terminals of the MMCs of the F2F, (c) dc current at the terminals of the F2F-MMC, and (d) the energy per converter station.

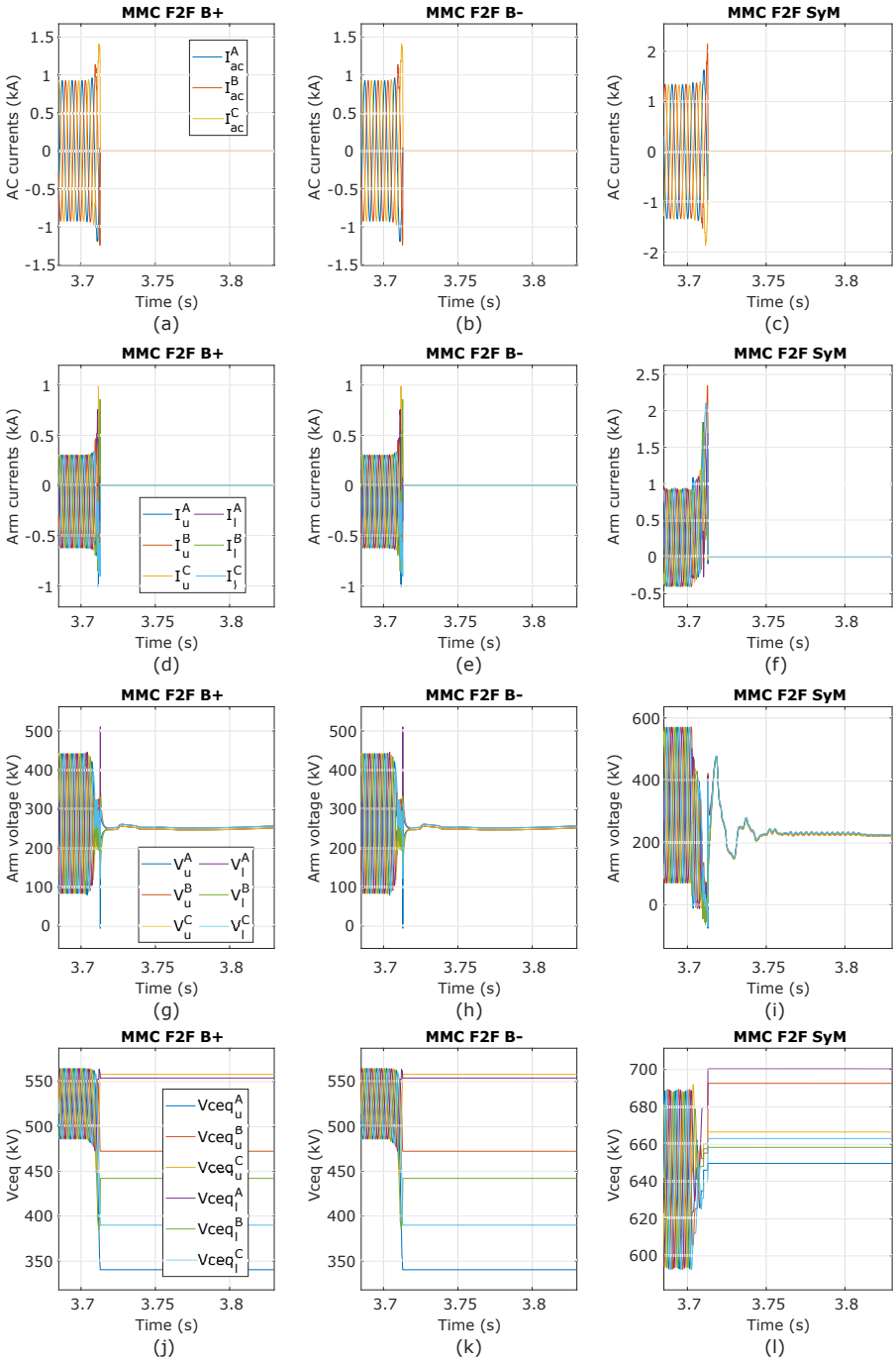


Figure 5.21: Ac currents (first row), arm currents (second row), arm voltages (third row), and the voltage of the equivalent arm capacitor for the three MMCs in the F2F for the Case 4 when the fault is on the SyM line (see Table 4.5).

The dc currents at the terminals of the F2F-MMC are presented in Fig. 5.20c. At the time of the fault, the current on the SyM increases near to 4 kA. The dc currents on the MMCs connected to the bipole are reduced to zero as the complete dc-dc converter is blocked. The current disturbance in this fault is shorter as it depends on the blocking time of the three MMCs and not the ACCB opening time. The ACCBs are opened as secondary protection devices.

The energy per converter station is presented in Fig. 5.20d. As previous results, the energy in the converter stations is disturbed with changes in the dc voltage. At the time of the fault, the converter stations have a drop in their total energy except for the power-controlled station of the SyM. The bipole stations have an energy drop due to the loss of power from the dc-dc converter. The F2F-MMC has an energy drop because it continues to feed the bipole line discharging its capacitors. The voltage-controlled station on the SyM line has an energy drop because they partially discharge their capacitors into the fault. On the contrary, the power-controlled station on the SyM line is blocked before the discharge of the capacitors. After the fault event, the blocked stations are unable to recover steady-state conditions, and only the stations in the bipole can control the energy back to steady-state conditions.

The converter results are presented in Fig. 5.21. As the converter is blocked completely, the transients are short and with low magnitudes. The ac current is presented in Fig. 5.21a, b, and c. It can be noticed that the ac currents in the three MMCs stop in a few ms, in this case, the ACCBs are not needed because blocking the three converters is enough to stop the ac currents. Similar to the ac currents, the arm currents are stopped in a few ms.

The voltages measured at the terminals of each arm are presented in the third row of Fig. 5.21. Similar to previous results, the arm voltages present negative values after blocking the converter. These transients are set by the ac system and not by the arms modulation. Indeed, at the instant of the fault the MMC connected to the SyM is subject to a fast transient which is partially transferred to the other MMCs in the F2F through the transformers. After the fault event, the voltages at the terminals of the arms stabilize on $V^{dc}/2$. On the bipole side, it is equivalent to 262.5 kV while, on the SyM, it depends on the final pole-to-pole dc voltage. For the fault considered in this thesis, the positive pole drops to zero while the negative pole has an overvoltage limited by the surge arresters. As presented in Chapter 4 the surge arresters are designed to limit the overvoltage to 1.6 p.u. at the terminals of the ac-dc converters in the SyM (see Fig. 5.12). For Case 4, the voltage of the

negative pole after the fault is around 1.4 p.u., in Fig. 5.20. Thus, the voltage per arm of the MMC connected to the SyM stabilize at ∼224 kV in Fig. 5.21i.

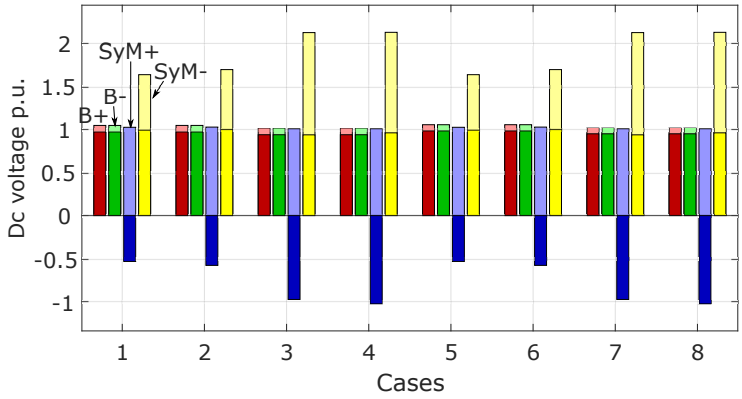


Figure 5.22: Maximum (light bars) and minimum (dark bars) pole-to-ground dc voltage registered in the F2F for the eight cases when a fault is considered in the SyM (see Table 4.5). Red, green, blue, and yellow are the voltages of the positive pole of the bipole, negative pole of the B, the SyM positive pole, and SyM negative pole respectively.

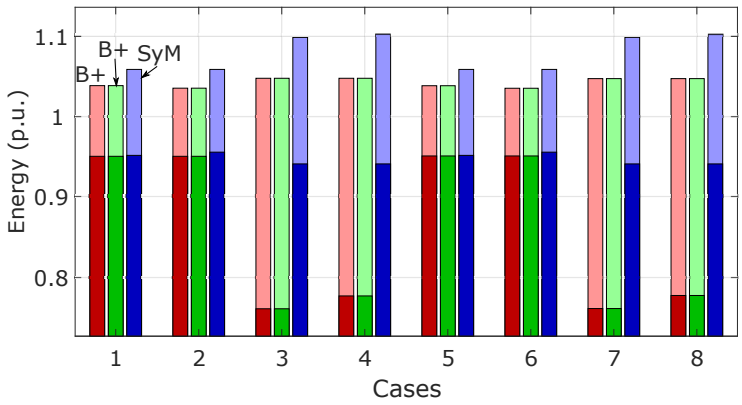


Figure 5.23: Maximum (light bars) and minimum (dark bars) energy per MMC in the F2F for the eight cases when a fault is considered in the SyM (see Table 4.5). Red, green and blue are the MMCs connected to the positive pole of the bipole, negative pole of the B, and the SyM respectively.

As mentioned previously, the F2F-MMC has a drop of its total energy due to the power flow direction. This can be evidenced in Fig. 5.23, where the cases with negative power flow direction through the dc-dc converter have the greater energy drop, i.e. cases 3, 4, 7, and 8. The F2F continues to feed the bipole line, partially discharging the capacitors in the MMCs connected to the bipole Fig. 5.21j, and k. The capacitor on the MMC connected to the SyM are presented in Fig. 5.21l. These capacitors are charged by the power flow from the power-controlled station on the monopole line. The overvoltage in is less than 1.1 p.u. which should not represent a problem to the semiconductor switches in the arm.

The F2F-MMC is able to isolate the fault in the SyM line without triggering the blocking signals in the bipole line. The F2F-MMC is tested in the eight different power flow directions proposed in Table 4.5 obtaining similar results to those presented above. The maximum voltage dynamic variations are presented in Fig. 5.22 and the maximum energy dynamic variations are presented in Fig. 5.23.

5.7 Conclusions

This chapter presents the dc-dc front-to-front modular multi-level converter (F2F-MMC). A mathematical model, following the hypotheses presented in Chapter 3, is developed and used to understand the behavior of the converter in steady-state. Based on the steady-state operation, a pre-sizing of the converter is done to set the arm inductance and capacitance values. The proposed converter operates at 150 Hz, which reduces the size of the capacitors compared to the 50 Hz applications. On the other hand, the size of the arm inductors cannot be decreased as they are sized for the fault conditions, i.e. maximum di/dt and dc voltage, which do not change from the 50 Hz applications.

A control strategy is designed, using the diagonalization proposed in Chapter 3. The converter model and its control are implemented in Simulink/Matlab to test the case study proposed in Chapter 4, i.e. the interconnection between a bipole and a SyM. Three sets of simulations are performed: the nominal and normal operation where the power flow through the F2F-MMC is changed, and the fault scenarios. The fault cases are performed for a fault on the bipole, equivalent to a pole-to-pole on the positive MMC of the bipole, and a fault pole-to-ground on the SyM line.

The simulation results for the two faults considered show that the F2F-MMC is capable to isolate the fault and stop the fault currents without exceeding the switches voltage or current ratings. As explained in Chapter 4, the semiconductor switches considered can open a fault current with a magnitude of twice their nominal current, i.e. 3.6 kA. The blocking signal is activated to open the fault currents below this limit. However, in case of increased fault current, a bypass thyristor can be used to protect the lower diodes on the HBSMs. For this case, the results presented do not change, what changes is the path taken by the fault current, i.e. through the protective thyristors instead of the diodes. More detailed studies analyzing the thermal impact on the semiconductor switches must be done to determine the need of these bypass thyristors.

The overvoltages measured in the equivalent arm capacitor do not represent a problem for the converter as they do not exceed the switches rated voltage (3.3 kV). In case of increased voltages, the capacitances in the SMs can be adjusted, increasing their value to reduce the voltage variation. Or, additional elements inside the SMs can be installed to avoid damaging the IGBTs or the capacitors, such as the bleed and rapid discharge resistors mentioned in [143].

The fault simulation results have demonstrated the F2F-MMC fire-wall capability and immediate redundancy for a fault on the bipole side. With a correct coordination with the internal ACCBs, the F2F-MMC is capable to isolate a fault on either the bipole or SyM, without triggering the blocking signals on the healthy zones. Another fault clearing strategy, is to block the complete F2F-MMC and restart the converters connected to the healthy zones. However, the immediate redundancy is no longer achieved. The F2F-MMC degraded mode, introduced in Section 1.5, equivalent to the interconnection AM-SyM, is also verified, exchanging 350 MW (0.5 p.u.) after the fault clearance.

For the cases when the fault is on the B line, the worst dc voltages and total F2F-MMC energy variations can be linked to the positive power flow direction through the dc-dc converter, i.e. cases 1, 2, 5, and 6 in Fig. 5.18 and Fig. 5.18. Indeed, losing the power contribution from the faulted pole on the B, has a direct impact on the SyM line. For the cases where the fault is located on the SyM line, the greatest variations are found for the negative power flow direction through the dc-dc converter, i.e; cases 3, 4, 7, and 8 in Fig. 5.22 and Fig. 5.23. In these cases, the power towards the B line increases the discharge of the F2F-MMC and the oscillations on the dc voltages on the SyM line.

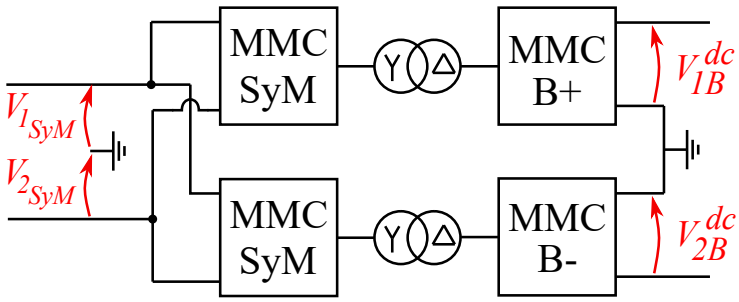


Figure 5.24: Interconnection between a bipole and a SyM using two F2F-MMCs, one per pole of the bipole, allowing immediate redundancy in case of a faulted pole on the bipole side.

The chapter was focused on the dc faults and their impact on the dc-dc converter and the B and SyM lines. However, the analysis of internal faults is missing. The faults in the ac system could lead to additional requirements on the converter sizing. This analysis is left for future studies.

As explained in Section 5.4.1, the F2F structure considered in this thesis, presented in Fig. 5.1, needs additional elements to stop the fault currents. The use of ACCB is explored in this chapter but, it does not allow a clean decoupling between the fault and the healthy zones. Due to the long opening time of the ACCBs the SyM is disturbed with a change of power direction. However, the blocking signals are not triggered. The use of FBSMs is partially explored and presented in Appendix B.3. The simulation results of the F2F-MMC with FBSMs suggest a better performance as it reduces the disturbances in the healthy zones. The use of FBSMs could lead to an increased initial and operational cost of the F2F-MMC. Another possible structure could be the use of one, decoupled, F2F-MMC per pole as shown in Fig. 5.24. The new structure could decouple the poles avoiding the use of either ACCBs or FBSMs because the power flow is stopped when both converters are blocked (similar to a fault on the SyM studied in this chapter). Additionally, the control proposed in [106] could be implemented, further reducing the impact on the healthy zones.

Chapter 6

Flexible dc Modular Multi-level Converter

This chapter is based in the following publications:

J1 D. G. Acero, M. Cheah-Mane, J. D. Páez, F. Morel, O. Gomis-Bellmunt and P. Dworakowski, "Dc-MMC for the Interconnection of HVDC Grids With Different Line Topologies," in *IEEE Transactions on Power Delivery*, vol. 37, no. 3, pp. 1692-1703, June 2022, doi: 10.1109/TPWRD.2021.3095966.

J2 D. Gómez A. et al., "Case study of dc-MMC interconnecting two HVDC lines with different grid topologies", *CIGRE Science & Engineering*. No. 24, pp. 100-114, Feb. 2022.

6.1 Introduction

The dc-MMC is one of the most studied dc-dc converters in the literature due to its advantages with respect to the F2F-MMC. The dc-MMCs proposed and studied in the literature are presented in Fig. 6.1. The monopolar dc-MMC (Fig. 6.1a) can interconnect two HVDC grids with similar grid topologies sharing a dc terminal, i.e. the interconnections AM-AM or B-B sharing the reference point. The bipolar dc-MMC, presented in Fig. 6.1b, can be used to interconnect two bipoles or a bipole with a SyM [85,86,144] but, only the normal operation has been studied in the literature. In case of a fault in one pole of the bipole, the control proposed in the literature is unable to continue in a degraded mode, i.e. interconnecting an AM with a SyM, because it is designed for the nor-

mal operation. Moreover, the bipolar dc-MMC must be reconfigured to isolate the faulted pole on the bipole line, which has not been explored in the literature.

Based on the bipolar dc-MMC, the flexible dc-MMC is proposed to have the capacity to interconnect different line topologies (see Fig. 6.2a). The main advantage of the flexible dc-MMC is that it provides a degraded mode for the interconnections B-SyM, i.e. it can be used for different heterogeneous interconnections. Contrary to the bipolar dc-MMC, the new converter does not have a connection to ground, which allows to unify the middle arms, removing the arm inductor.

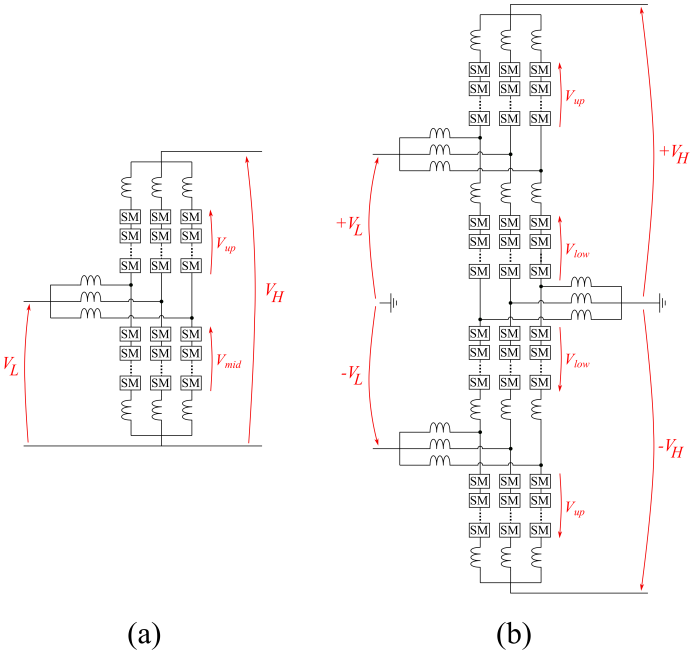


Figure 6.1: Dc-MMCs explored in the literature: (a) the monopolar dc-MMC and (b) the bipolar dc-MMC.

In this chapter, the flexible dc-MMC is studied. The converter control design follows the structure presented in Chapter 3 and the simulations follow the cases proposed in Chapter 4.

6.2 Mathematical modeling

Following the hypotheses formulated in Section 3.3, the converter legs are considered to be balanced, i.e. there are no ac components on the dc sides, and therefore only one leg is analyzed. The dc currents per leg

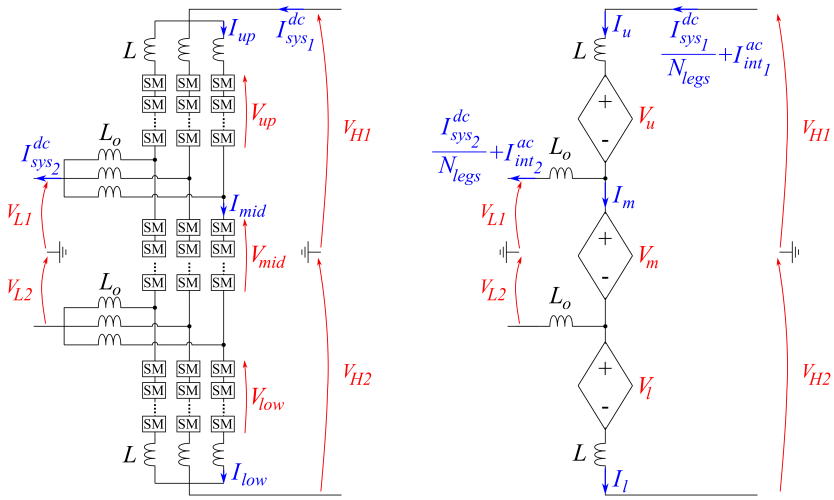


Figure 6.2: Flexible dc-MMC. (a) three phase circuit. (b) Single phase circuit used for the mathematical model.

depend on the number of legs, N_{legs}, considered for the converter. As the internal ac system is decoupled from the ac transmission grid, the number of legs is not fixed to three, it can be changed depending on the transmitted power. In this thesis, a three-phase converter is considered but, the analysis can be applied for n legs (with $n > 1$).

The flexible dc-MMC single phase circuit used for the mathematical model is presented in Fig. 6.2b. The single leg circuit uses the equivalent arm voltage simplification presented in Section 3.2.1. In Fig. 6.2a two dc currents can be identified $I^{dc}_{sys_1}$ and $I^{dc}_{sys_2}$, which are presented in Fig. 6.2b as a N^{th}_{legs} part of the initial currents. The currents $I^{ac}_{int_1}$ and $I^{ac}_{int_2}$ represent the internal ac currents circulating between the converter legs. These ac currents do not circulate through the dc systems.

From Fig. 6.2b, three independent currents per leg can be identified: I_u, I_m, and I_l. The three equations describing the converter circuit are:

$$V_{L1} + L_o \frac{d}{dt}(I_u - I_m) + R_o(I_u - I_m) + V_u + L\frac{d}{dt}I_u + R\,I_u - V_{H1} = 0 \quad (6.1)$$

$$V_{L2} - L_o \frac{d}{dt}(I_m - I_l) - R_o(I_m - I_l) + V_l + L\frac{d}{dt}I_l + R\,I_l - V_{H2} = 0 \quad (6.2)$$

$$\begin{aligned} -V_{L1} - V_{L2} - L_o\frac{d}{dt}\left(I_u - I_m\right) - R_o\left(I_u - I_m\right) + V_m \\ +L_o\frac{d}{dt}\left(I_m - I_l\right) + R_o\left(I_m - I_l\right) = 0 \end{aligned} \tag{6.3}$$

where R and R_o are the arm and the output inductor resistances (not represented in Fig. 6.2). The circuit equations can be organized in matrix form as follows:

$$\begin{aligned} &\begin{bmatrix} L+L_o & -L_o & 0 \\ 0 & -L_o & L+L_o \\ -L_o & 2L_o & -L_o \end{bmatrix} \begin{bmatrix} \dot{I}_u \\ \dot{I}_m \\ \dot{I}_l \end{bmatrix} = \\ &\qquad \begin{bmatrix} -(R+R_o) & R_o & 0 \\ 0 & R_o & -(R+R_o) \\ R_o & -2R_o & R_o \end{bmatrix} \begin{bmatrix} I_u \\ I_m \\ I_l \end{bmatrix} \\ &+ \underbrace{\begin{bmatrix} -1 & 0 & 0 \\ 0 & 0 & -1 \\ 0 & -1 & 0 \end{bmatrix}}_{\boldsymbol{V_c}} \begin{bmatrix} V_u \\ V_m \\ V_l \end{bmatrix} + \underbrace{\begin{bmatrix} 1 & 0 & -1 & 0 \\ 0 & 1 & 0 & -1 \\ 0 & 0 & 1 & 1 \end{bmatrix}}_{\boldsymbol{K_V}} \underbrace{\begin{bmatrix} V_{H1} \\ V_{H2} \\ V_{L1} \\ V_{L2} \end{bmatrix}}_{\boldsymbol{V_k}} \end{aligned} \tag{6.4}$$

where the state variables are the arm currents I_u, I_m, and I_l, the control variables are the arm voltages V_u, V_m, and V_l. In this particular case the system voltages have only dc components V_{H1}, V_{H2}, V_{L1}, and V_{L2}.

6.3 Steady-State analysis

6.3.1 Dc steady-state analysis

Following the general analysis presented in Section 3.4.2, the arm dc currents can be expressed in terms of the system dc currents. The flexible dc-MMC has two system dc currents: $I^{dc}_{sys_1}$ and $I^{dc}_{sys_2}$, which can be expressed as:

$$I^{dc}_{sys_1} = \frac{P^{dc}_T}{V_{H1} + V_{H2}} \tag{6.5}$$

$$I^{dc}_{sys_2} = \frac{P^{dc}_T}{V_{L1} + V_{L2}} \tag{6.6}$$

where P_T^{dc} is the dc power transmitted through the dc-dc converter.

The system dc currents are presented in Fig. 6.2 with a positive convention when the power flow is from the high voltage side (right) to the low voltage system (left). Following the positive conventions, the arm dc currents, per leg, are obtained as follows:

$$I_u^{dc} = \frac{I_{sys_1}^{dc}}{N_{legs}} = \frac{1}{V_{H1} + V_{H2}} \frac{P_T^{dc}}{N_{legs}} \tag{6.7}$$

$$I_m^{dc} = \frac{I_{sys_1}^{dc} - I_{sys_1}^{dc}}{N_{legs}} = \left(\frac{1}{V_{H1} + V_{H2}} - \frac{1}{V_{L1} + V_{L2}} \right) \frac{P_T^{dc}}{N_{legs}} \tag{6.8}$$

$$I_l^{dc} = \frac{I_{sys_1}^{dc}}{N_{legs}} = -\frac{1}{V_{H1} + V_{H2}} \frac{P_T^{dc}}{N_{legs}} \tag{6.9}$$

where N_{legs} is the number of legs of the converter. For the converter studied in this thesis $N_{legs} = 3$, as the circuit presented in Fig. 6.2a.

The arm dc voltages can be found with the following expression (see Section 3.4.2):

$$\boldsymbol{V_{arm}^{dc}} = -\boldsymbol{V_c^{-1}} \boldsymbol{K_V} \boldsymbol{V_k^{dc}} \tag{6.10}$$

where $\boldsymbol{V_c}$ is the control matrix linked to the arm voltages, $\boldsymbol{K_V}$ is the matrix linked to the system voltages, which are contained in $\boldsymbol{V_k}$.

Using the corresponding matrices from (6.4) in (6.10), yields to:

$$\boldsymbol{V_{arm}^{dc}} = -\begin{bmatrix} -1 & 0 & 0 \\ 0 & 0 & -1 \\ 0 & -1 & 0 \end{bmatrix}^{-1} \begin{bmatrix} 1 & 0 & -1 & 0 \\ 0 & 1 & 0 & -1 \\ 0 & 0 & 1 & 1 \end{bmatrix} \begin{bmatrix} V_{H1} \\ V_{H2} \\ V_{L1} \\ V_{L2} \end{bmatrix}$$

$$\boldsymbol{V_{arm}^{dc}} = \begin{bmatrix} V_u^{dc} \\ V_m^{dc} \\ V_l^{dc} \end{bmatrix} = \begin{bmatrix} V_{H1} - V_{L1} \\ V_{L1} + V_{L2} \\ V_{H2} - V_{L2} \end{bmatrix} \tag{6.11}$$

6.3.2 Dc power balance

Using the arm dc currents (6.7)-(6.9) and arm dc voltages (6.11), the arm dc power can be expressed as:

$$P_u^{dc} = \frac{V_{H1} - V_{L1}}{V_{H1} + V_{H2}} \frac{P_T^{dc}}{N_{legs}} \tag{6.12}$$

$$P_m^{dc} = \left(\frac{V_{L1} + V_{L2}}{V_{H1} + V_{H2}} - 1 \right) \frac{P_T^{dc}}{N_{legs}} \tag{6.13}$$

$$P_l^{dc} = \frac{V_{H2} - V_{L2}}{V_{H1} + V_{H2}} \frac{P_T^{dc}}{N_{legs}} \tag{6.14}$$

As it was mentioned in Section 3.4.3, the energy balance of a dc-dc converter depends on the sum of the arms dc power (containing SMs) in a leg. This addition must be equal to zero, meaning that the excess of energy of one arm can supply the lack of it in another. This energy balance is achieved with the internal circulation of ac power. For the case of the flexible dc-MMC, the sum of the three arms is given by:

$$P_u^{dc} + P_m^{dc} + P_l^{dc} = 0$$

From the hypothesis $P_{in} = P_{out}$, and assuming steady-state conditions where $V_{H1} = V_{H2} = V_H$ and $V_{L1} = V_{L2} = V_L$, the previous expression yields to:

$$\left(\frac{V_H - V_L}{2V_H} + \frac{V_L}{V_H} - 1 + \frac{V_H - V_L}{2V_H} \right) \frac{P_T^{dc}}{N_{legs}} = 0 \tag{6.15}$$

which indicates that, with the proper energy control, the flexible dc-MMC is able to keep the energy balance without external source of energy.

The arm dc power equations (6.12)-(6.14) are used to analyse the ac steady-state in next section.

6.3.3 Ac steady-state analysis

As explained in Chapter 3, modular HVDC converters need an ac power exchange to balance the energy in the arms. The flexible dc-MMC requires an ac power circulating inside the converter to exchange power between arms without disturbing the interconnected dc systems. The

average power balance per arm is:

$$\left\langle P_{arm}^{dc} + P_{arm}^{ac} \right\rangle = 0 \tag{6.16}$$

The equations for the power balance per arm (u, m, and l) defined in (6.12)-(6.14), can be detailed as follows:

$$\frac{V_{H1} - V_{L1}}{V_{H1} + V_{H2}} \frac{P_T^{dc}}{N_{legs}} = -V_u^{ac} I_u^{ac} \cos\left(\theta_{V_u} - \theta_{I_u}\right) \tag{6.17}$$

$$\left(\frac{V_{L1} + V_{L2}}{V_{H1} + V_{H2}} - 1\right) \frac{P_T^{dc}}{N_{legs}} = -V_m^{ac} I_m^{ac} \cos\left(\theta_{V_m} - \theta_{I_m}\right) \tag{6.18}$$

$$\frac{V_{H2} - V_{L2}}{V_{H1} + V_{H2}} \frac{P_T^{dc}}{N_{legs}} = -V_l^{ac} I_l^{ac} \cos\left(\theta_{V_l} - \theta_{I_l}\right) \tag{6.19}$$

Assuming the steady-state values for the pole-to-ground voltages considered in the case study, i.e. $V_{H1} = V_{H2} = 525$ kV and $V_{L1} = V_{L2} = 320$ kV, and a power transfer from the high voltage (right) to the low voltage side (left, see Fig. 6.2b), the internal ac power needed to balance the converter is presented in Fig. 6.3.

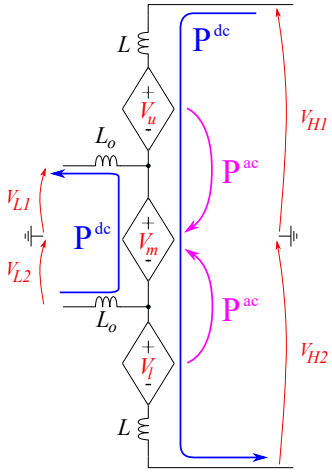


Figure 6.3: Power exchanges between the arms in the flexible dc-MMC to keep the energy balanced.

To find the ac solution that respects the energy equilibrium (as presented in Fig. 6.3), the ac voltages in magnitude and phase must be defined. Considering only the ac circuit, i.e. neglecting the dc voltages and currents, the equivalent ac circuit can be found. The single phase ac

circuit of the flexible dc-MMC is presented in Fig. 6.4. It can be noticed that the ac sources are not in series nor in parallel creating an inter-dependence between the arms. Therefore, the variation in one arm ac voltage has an indirect impact on the current of the other two. Different from the circuit found for the MMC in Fig. 5.3, the ac solution for the flexible dc-MMC has not an easy analytical formulation.

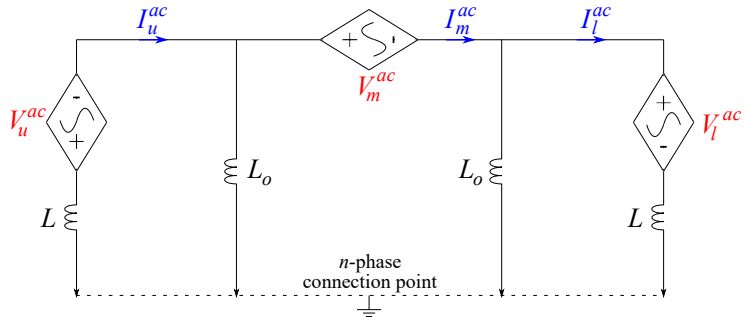


Figure 6.4: Equivalent ac circuit, per leg, of the flexible dc-MMC. The dashed line indicates the theoretical reference, which is in fact a n-phase connection point.

To complete the ac steady-state solution, it is necessary to know 12 variables: three arm voltage magnitudes, three arm voltage phases, three arm current magnitudes, and three arm current phases. From the 12 variables, only the half are independent variables as the arm currents (in magnitude and phase) depend on the circuit equations (6.1)-(6.3). Thus, only 6 variables are needed.

If the angle of the middle arm is fixed as the reference, i.e. $\theta_{V_m} = 0°$, only five independent variables are left to define. The ac steady-state solution is restricted by the power balance equations (6.17)-(6.19), leading to a problem with five independent variables and three equations. Due to the imbalance between the number of variables and equations, an optimization problem is proposed to solve the ac steady state of the flexible dc-MMC (see Section 6.3.4).

First ac voltage estimation from steady state dc voltages, FBC, and degraded operation requirements

The maximal ac voltage magnitude can be estimated from the dc steady-state analysis, the fault blocking capability (FBC) requirements, and the degraded operation. The different dependencies are explored in this section.

The dc voltage per arm can be calculated using (6.11). Considering the values from the proposed case study, the arm dc voltages are:

$$\boldsymbol{V_{arm}^{dc}} = \begin{bmatrix} V_u^{dc} \\ V_m^{dc} \\ V_l^{dc} \end{bmatrix} = \begin{bmatrix} V_{H1} - V_{L1} \\ V_{L1} + V_{L2} \\ V_{H2} - V_{L2} \end{bmatrix} = \begin{bmatrix} 205\,\text{kV} \\ 640\,\text{kV} \\ 205\,\text{kV} \end{bmatrix} \tag{6.20}$$

These are the minimum voltages needed to withstand the system dc voltages without transferring power. In superposition to this dc voltage, the ac voltage is added to keep the converter energy balanced. To modulate the ac voltage, a first assumption is to install twice the steady-state dc voltage, allowing to have an ac voltage with a magnitude equal to the dc voltage (see maximum $V_{arm}^{ac\,peak}$ in Fig. 5.4).

Installing twice the dc voltage allows the converter to operate in normal conditions. Additional SMs (HB or FB), could be needed to provide FBC. A direct way to analyze the voltage needed to stop the pole-to-ground faults in the interconnected systems is using the general expression for the arm voltage (6.10), changing the pole-to-ground voltages, in $\boldsymbol{V_K^{dc}}$, to zero. Table 6.1 summarize the four possible faults for the flexible dc-MMC. The cells highlighted in red are the cases that do not match the initial estimation found in (6.20). It is worth to mention that the voltages found in Table 6.1 are the minimum voltage requirements, i.e. the flexible dc-MMC must have enough SMs to withstand these voltages. The FBC requirements for the pole-to-ground faults cover the requirements for the pole-to-pole faults thus, no additional SMs should be considered. For the pole-to-ground faults on the monopole, a pole displacement can appear on the healthy pole but, it does not imply additional voltage requirements.

It can be evidenced that the upper and lower arm need a combination of HBSM and FBSMs to withstand the negative voltages produced in case of a fault on the HV side. However, when the flexible dc-MMC operates in degraded mode, i.e. after a fault on the bipole side, additional SMs are needed to modulate the ac voltage. Thus, the possible degraded modes should be determined.

The degraded cases are determined from the possible faults in the poles of a bipole. The flexible dc-MMC could have, up to four degraded cases for the situation where it is used to interconnect two bipoles. For this thesis, only two degraded cases are considered to match with the proposed case study.

Table 6.1: Voltage requirements per arm depending on the fault location

Arm voltage	$V_{H1}=0$	$V_{H2}=0$	$V_{L1}=0$	$V_{L2}=0$
V_u	$-V_{L1}$	$V_{H1}-V_{L1}$	V_{H1}	$V_{H1}-V_{L1}$
V_m	$V_{L1}+V_{L2}$		V_{L2}	V_{L1}
V_l	$V_{H2}-V_{L2}$	$-V_{L2}$	$V_{H2}-V_{L2}$	V_{H2}

The case study considers a bipole on the high voltage side of the flexible dc-MMC. The two degraded cases are related to the faults presented in the first two columns in Table 6.1. Assuming that the arm ac voltage has the same magnitude as the arm dc voltage, the ranges of voltages per arm are estimated as follows:

$$V_u \in \begin{bmatrix} -2\,V_{L1} & V_{H1} \end{bmatrix} \tag{6.21}$$

$$V_m \in \begin{bmatrix} 0 & 2\,(V_{L1}+V_{L2}) \end{bmatrix} \tag{6.22}$$

$$V_l \in \begin{bmatrix} -2\,V_{L2} & V_{H2} \end{bmatrix} \tag{6.23}$$

where the maximum voltages in the upper and lower arms are determined by the faults on the bipole side (see Table 6.1) and the minimum voltages are estimated from the degraded operation (twice the operating dc voltage). The middle arm does not need FBSM and its maximum voltage is estimated as twice the normal operating dc voltage.

Replacing the values considered for the case study in (6.21)-(6.23), the estimated voltage range per arm is:

$$V_u \in \begin{bmatrix} -640 & 525 \end{bmatrix} \text{ kV} \tag{6.24}$$

$$V_m \in \begin{bmatrix} 0 & 1280 \end{bmatrix} \text{ kV} \tag{6.25}$$

$$V_l \in \begin{bmatrix} -640 & 525 \end{bmatrix} \text{ kV}. \tag{6.26}$$

The ac solution needs to define the angle between the ac voltages and ac currents to keep the energy in the converter balanced. To complete the ac analysis an optimization problem is proposed, where the ranges are a first overestimation of the ac voltage magnitudes per arm used as limits for the optimization problem.

6.3.4 Optimization problem

To facilitate the implementation of the optimization problem, the variables are expressed in phasor form. The phasor, polar and rectangular representations are:

$$\underline{X_i} = X_i \angle\theta = X_i^d + jX_i^q \tag{6.27}$$

where X is either an ac current or voltage for $i \in u, m, l$. Using this notation, and reminding that only the first harmonic is considered, the RMS arm currents can be expressed as follows.

$$I_i^{RMS} = \sqrt{\frac{I_i^{ac\,2}}{2} + I_i^{dc^2}} \tag{6.28}$$

The optimization problem considers the 11 variables of the ac system, i.e. five independent voltages and six dependent currents, organized in the vector $\boldsymbol{X}$, as follows:

$$X^T = \left[V_u^d,\, V_u^q,\, V_m,\, V_l^d,\, V_l^q,\, I_u^d,\, I_u^q,\, I_m^d,\, I_m^q,\, I_l^d,\, I_l^q\right] \tag{6.29}$$

The objective function aims to reduce the conduction losses in the converter by minimizing the currents in the arms. It is expressed as follows:

$$\min f(x) = N_{sm_u} \cdot I_{u_{RMS}}^2 + N_{sm_m} \cdot I_{m_{RMS}}^2 + N_{sm_l} \cdot I_{l_{RMS}}^2 \tag{6.30}$$

where N_{sm_i} is a weight factor depending on the number and type of SM per arm (for $i \in u, m, l$). It can be expressed as:

$$N_{sm_i} = N_{sm_{HB_i}} + 2N_{sm_{FB_i}} \tag{6.31}$$

where $N_{sm_{HB_i}}$ is the number of HBSMs and $N_{sm_{FB_i}}$ is the number of FBSMs per arm.

As the optimization problem involves the dependent variables, the circuit equations have been included as equality constraints. The circuit equations are expressed in their real and imaginary parts following the rectangular form presented in (6.27). Similarly, the power balance equations are included using their rectangular representation.

Additional inequality constraints are included to bound the variables. The arm currents are limited to the maximum RMS current allowed by the considered switches (I_{rated}), and the arm voltages are limited to a

maximum number of SM allowed per arm ($V_{arm_i}^{max}$), as presented in (6.32).

$$\begin{aligned} I_{i_{RMS}} &\leq I_{rated} \\ V_i^{dc} + V_i^{ac} &\leq V_{arm_i}^{max} \end{aligned} \tag{6.32}$$

where I_{rated} is fixed from the considered IGBT, and $V_{arm_i}^{max}$ is set by the user depending on the operational and system requirements (for $i \in u, m, l$). For this study, the ac voltage limits, $V_{arm_i}^{max}$, are determine by the ranges found in (6.24)-(6.26).

Optimization input/output data

The optimization problem is solved numerically in particular with the *fmincon* function from Matlab. The optimization is used to obtain the ac and dc steady-state solution, i.e. $\underline{V^{ac}}$, $\underline{I^{ac}}$, V^{dc}, and I^{dc} per arm. The general process is presented in Fig. 6.5. The input parameters are detailed below, with the estimated values considered for the case study.

- k_{ac}: the ratio between the amplitude of the ac voltage and the total installed voltage per arm. As the flexible dc-MMC is not dependent on an external ac grid, the internal ac voltages can be freely defined. In this case $k_{ac} = 0.92$ is used.
- I_{rated}: the nominal current of the used IGBT (1.8 kA considered for the case study).
- V_{H1}, V_{H2}, V_{L1}, and V_{L2}: the pole-to-ground voltages. The case study considers $V_{H1} = V_{H2} = 525$ kV and $V_{L1} = V_{L2} = 320$ kV.
- P^{dc}: the dc-dc converter rated power (700 MW).
- N_{legs}: the number of legs (3 considered for the case study).
- L and L_o: the circuit inductuctances calculated as introduced in Section 3.5.2 (See Section 6.4.1). These values are needed to solve the ac circuit equations.
- f: the ac operating frequency (150 Hz considered for the case study).
- V_{SM}: the voltage per SM (1.6 kV).
- V_{arm}^{max}: the maximal ac voltage magnitude per arm. Estimated in (6.24)-(6.26).

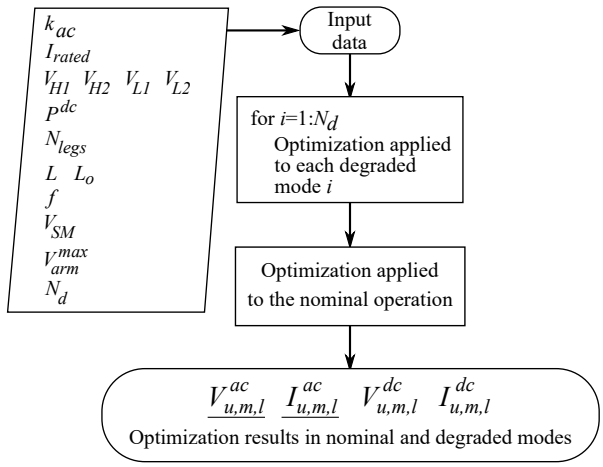


Figure 6.5: General flowchart representing the process used to calculate the steady-state solution of the flexible dc-MMC.

- N_d: the number of degraded modes and its location (HV or LV). For this study two degraded modes on the HV side are considered.

To have the results from the optimization problem, the inductance sizing should be calculated first. Then, the capacitance in the SMs can be calculated.

6.4 Preliminary converter sizing

As mentioned above, the circuit inductors are needed for the ac steady-state solution. The rest of the elements, i.e. the number of SMs, the type of SMs (HB or FB), and the capacitance value per SM, are calculated from the optimization results.

6.4.1 Circuit inductors

The circuit inductors are sized based on the critical fault current slope, which is one of the suggested approaches presented in Section 3.5.2. This approach is the only applicable to the flexible dc-MMC, as the converter does not have an ac reference system to calculate the base impedance.

There are six fault cases that can be evaluated, four pole-to-ground and two pole-to-pole scenarios. From the six scenarios, the two pole-to-pole faults are the most important in terms of fault current slopes. The current slopes and the relation with the inductance values can be

described by the circuit equations, found from the high and low voltage loops, presented below.

$$-V_{H1} - V_{H2} + L\frac{d\,I_u}{dt} + V_u^{ss} + V_m^{ss} + V_l^{ss} + L\frac{d\,I_l}{dt} = 0$$

$$-0 - 0 + L\frac{d\,I_u}{dt} + V_u^{ss} + V_m^{ss} + V_l^{ss} + L\frac{d\,I_l}{dt} = 0 \tag{6.33}$$

$$-V_{L1} - V_{L2} - L_o\frac{d}{dt}\left(I_u - I_m\right) + V_m^{ss} - L_o\frac{d}{dt}\left(I_l - I_m\right) = 0$$

$$-0 - 0 - L_o\frac{d}{dt}\left(I_u - I_m\right) + V_m^{ss} - L_o\frac{d}{dt}\left(I_l - I_m\right) = 0 \tag{6.34}$$

where V_u^{ss}, V_m^{ss}, and V_l^{ss} are the steady-state arm voltages. A first approximation is to use the dc steady-state conditions for the arm voltages, presented in (6.20), as follows:

$$\left(V_u + V_m + V_l\right)^{dc\,ss} \approx -L\left(\frac{d\,I_u}{dt} + \frac{d\,I_l}{dt}\right) \tag{6.35}$$

$$V_m^{dc\,ss} = L_o\left(\frac{d}{dt}\left(I_u - I_m\right) + \frac{d}{dt}\left(I_l - I_m\right)\right) \tag{6.36}$$

Assuming that the fault current slope in the upper and lower arm are equal at the time of the pole-to-pole fault, the expressions above can be simplified to obtain the minimal inductance values. Replacing the fault slope by the critical slope yields to:

$$L^{min} = \frac{\left(V_u + V_m + V_l\right)^{dc\,ss}}{2\left(di/dt\right)_{crit}} \tag{6.37}$$

$$L_o^{min} = \frac{V_m^{dc\,ss}}{2\left(di/dt\right)_{crit}} \tag{6.38}$$

where the factor 2 on the denominators corresponds to the two arm inductors, L, on the HV loop and the two output inductors, L_o, on the LV loop.The critical fault current slope, $(di/dt)_{crit}$, is 6.4 A/µs estimated in (3.34).

Using the arm dc voltage estimations for the case study, presented in (6.20), in (6.37) and (6.38), the minimal arm and output inductance values are found as follows:

$$L^{min} = \frac{1050\,\mathrm{kV}}{2\left(6.4\,\mathrm{A/\mu s}\right)} \approx 82\,\mathrm{mH} \tag{6.39}$$

$$L_o^{min} = \frac{640\,\text{kV}}{2\,(6.4\,\text{A/µs})} \approx 50\,\text{mH}. \tag{6.40}$$

The inductance values found above correspond to the minimum values needed to ensure the fault current slope. However, to reduce the conduction losses due to internal circulating power, the output inductors should be as large as possible [80], although if they are too large, the voltage requirements on the arms will increase. The sizing of the output inductors is a trade-off between the current and voltage constraints, which is out of the scope of this thesis. The inductance values used in this work are $L = 82$ mH and $L_o = 200$ mH.

Optimization results

The optimization problem, is performed for three cases: nominal operation, and the two degraded cases, obtaining the steady-state solution. The solutions are used to size the arm, defining the equivalent capacitance, the number of HB and FBSMs. Additionally, the optimization results are used in the control strategy to set the references of the currents (see Table 6.4). The final number of SMs per arm (considering FBC and degraded mode operation), and the ac steady-state results for the nominal operation are presented in Table 6.2. The steady-state results of the degraded modes are presented in appendix C.2.

Table 6.2: Number of SMs and ac steady-state solution for the nominal operation of the flexible dc-MMC.

Arm	Number of HBSMs	Number of FBSMs	$\underline{V^{ac}}$ (kV)	$\underline{I^{ac}}$ (kA)
Upper	0	372	$225\angle -171.2°$	$0.5\angle -27.6°$
Middle	661	0	$409\angle 0°$	$0.96\angle 62.35°$
Lower	0	372	$225\angle -171.2°$	$0.5\angle -27.6°$

6.4.2 Capacitor in the sub-modules

The equivalent arm capacitance can be calculated using the steady-state results (see Section 3.5.3). In this case, the equivalent capacitance is calculated for the worse case scenario, i.e. with the biggest energy variation per arm. The greatest energy variation in the upper arm is when the converter is working in the degraded mode after a fault on the positive pole of the bipole. Inversely, the lower arm has its biggest energy

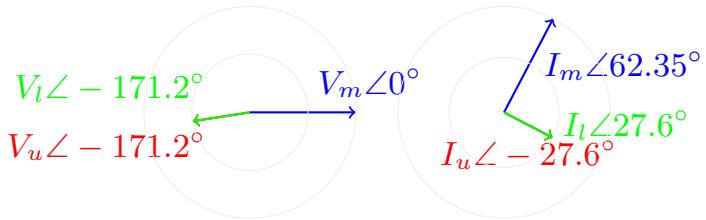


Figure 6.6: Graphical representation of the arm voltages and currents found with the optimization problem for the nominal operation.

variation in the degraded mode after a fault on the negative pole of the bipole. The middle arm has its worst energy variation for the normal operation.

The equivalent arm capacitance can be calculated using the expression (3.35), which depends on the number of SMs per arm, the voltage per SM, and the arm energy variation in steady-sate. Using the optimization results for the case study, presented in tables 6.2, C.1, and C.2, the calculated equivalent arm capacitance values are:

$$C_{eq_u} = 5.6\,\mu\text{F} \tag{6.41}$$

$$C_{eq_m} = 6.6\,\mu\text{F} \tag{6.42}$$

$$C_{eq_l} = 5.6\,\mu\text{F} \tag{6.43}$$

and the capacitance per SM are:

$$C_{SM_u} = C_{eq_u}\, N_{SM_u} = 5.6\,\text{mF} \cdot 372 = 2.1\,\text{mF} \tag{6.44}$$

$$C_{SM_m} = C_{eq_m}\, N_{SM_m} = 6.6\,\text{mF} \cdot 661 = 4.4\,\text{mF} \tag{6.45}$$

$$C_{SM_l} = C_{eq_l}\, N_{SM_l} = 5.6\,\text{mF} \cdot 372 = 2.1\,\text{mF} \tag{6.46}$$

6.5 Control design

Similar to the F2F-MMC, the flexible dc-MMC control is based on the decoupling of the state and control variables in (6.4). This section follows the procedure presented in Section 3.6.

6.5.1 System diagonalization

Using the diagonalization of the state matrix presented in appendix A for the initial model (6.4) yields to:

$$\begin{bmatrix}\dot{I}_1\\ \dot{I}_2\\ \dot{I}_3\end{bmatrix} = \begin{bmatrix}-\frac{R_o+R}{L_o+L} & 0 & 0\\ 0 & -\frac{R}{L} & 0\\ 0 & 0 & -\frac{R_o}{L_o}\end{bmatrix}\begin{bmatrix}I_1\\ I_2\\ I_3\end{bmatrix} + \begin{bmatrix}-\frac{1}{2(L_o+L)} & 0 & \frac{1}{2(L_o+L)}\\ -\frac{1}{2L} & -\frac{1}{2L} & -\frac{1}{2L}\\ 0 & -\frac{1}{2L_o} & 0\end{bmatrix}\begin{bmatrix}V_u\\ V_m\\ V_l\end{bmatrix} + \begin{bmatrix}\frac{1}{2(L_o+L)} & -\frac{1}{2(L_o+L)} & -\frac{1}{2(L_o+L)} & \frac{1}{2(L_o+L)}\\ \frac{1}{2L} & \frac{1}{2L} & 0 & 0\\ 0 & 0 & \frac{1}{2L_o} & \frac{1}{2L_o}\end{bmatrix}\begin{bmatrix}V_{H1}\\ V_{H2}\\ V_{L1}\\ V_{L2}\end{bmatrix} \tag{6.47}$$

where the current transformation matrix is:

$$\boldsymbol{P} = \begin{bmatrix}1 & 1 & 0\\ 0 & 1 & 1\\ -1 & 1 & 0\end{bmatrix} \qquad \boldsymbol{P}^{-1} = \begin{bmatrix}\frac{1}{2} & 0 & -\frac{1}{2}\\ \frac{1}{2} & 0 & \frac{1}{2}\\ -\frac{1}{2} & 1 & -\frac{1}{2}\end{bmatrix} \tag{6.48}$$

Based in the suggested voltage transformation presented in (3.56) the following expression can be found:

$$\boldsymbol{T} = \begin{bmatrix}-\frac{1}{2(L_o+L)} & 0 & \frac{1}{2(L_o+L)}\\ -\frac{1}{2L} & -\frac{1}{2L} & -\frac{1}{2L}\\ 0 & -\frac{1}{2L_o} & 0\end{bmatrix}^{-1}\begin{bmatrix}\frac{1}{L_o+L} & 0 & 0\\ 0 & \frac{1}{L} & 0\\ 0 & 0 & \frac{1}{L_o}\end{bmatrix}$$

$$\boldsymbol{T} = \begin{bmatrix}-1 & -1 & 1\\ 0 & 0 & -2\\ 1 & -1 & 1\end{bmatrix} \qquad \boldsymbol{T}^{-1=} = \begin{bmatrix}-\frac{1}{2} & 0 & \frac{1}{2}\\ -\frac{1}{2} & -\frac{1}{2} & -\frac{1}{2}\\ 0 & -\frac{1}{2} & 0\end{bmatrix} \tag{6.49}$$

The complete diagonal model using $\boldsymbol{T}$ transformation corresponds to:

$$\begin{aligned}\begin{bmatrix}\dot{I}_1\\ \dot{I}_2\\ \dot{I}_3\end{bmatrix} &= \begin{bmatrix}-\frac{R_o+R}{L_o+L} & 0 & 0\\ 0 & -\frac{R}{L} & 0\\ 0 & 0 & -\frac{R_o}{L_o}\end{bmatrix}\begin{bmatrix}I_1\\ I_2\\ I_3\end{bmatrix}\\ &+ \begin{bmatrix}\frac{1}{L_o+L} & 0 & 0\\ 0 & \frac{1}{L} & 0\\ 0 & 0 & \frac{1}{L_o}\end{bmatrix}\begin{bmatrix}V_1\\ V_2\\ V_3\end{bmatrix}\\ &+ \begin{bmatrix}\frac{1}{2(L_o+L)} & -\frac{1}{2(L_o+L)} & -\frac{1}{2(L_o+L)} & \frac{1}{2(L_o+L)}\\ \frac{1}{2L} & \frac{1}{2L} & 0 & 0\\ 0 & 0 & \frac{1}{2L_o} & \frac{1}{2L_o}\end{bmatrix}\begin{bmatrix}V_{H1}\\ V_{H2}\\ V_{L1}\\ V_{L2}\end{bmatrix}.\end{aligned} \tag{6.50}$$

The transformations between the 123 and the *uml* variables are presented below:

$$\boldsymbol{I_{123}} = \boldsymbol{P}^{-1}\,\boldsymbol{I_{uml}}$$

$$\begin{bmatrix}I_1\\ I_2\\ I_3\end{bmatrix} = \begin{bmatrix}\frac{I_u-I_l}{2}\\ \frac{I_u+I_l}{2}\\ \frac{-I_u+2I_m-I_l}{2}\end{bmatrix} \tag{6.51}$$

$$\boldsymbol{I_{uml}} = \boldsymbol{P}\,\boldsymbol{I_{123}}$$

$$\begin{bmatrix}I_u\\ I_m\\ I_l\end{bmatrix} = \begin{bmatrix}I_1+I_2\\ I_2+I_3\\ -I_1+I_2\end{bmatrix} \tag{6.52}$$

$$\boldsymbol{V_{123}} = \boldsymbol{T}^{-1}\,\boldsymbol{V_{uml}}$$

$$\begin{bmatrix}V_1\\ V_2\\ V_3\end{bmatrix} = \begin{bmatrix}\frac{-V_u+V_l}{2}\\ -\frac{V_u+V_m+V_l}{2}\\ -\frac{V_m}{2}\end{bmatrix} \tag{6.53}$$

$$\boldsymbol{V_{uml}} = \boldsymbol{T}\,\boldsymbol{V_{123}}$$

$$\begin{bmatrix} V_u \\ V_m \\ V_l \end{bmatrix} = \begin{bmatrix} -V_1 - V_2 + V_3 \\ -2V_3 \\ V_1 - V_2 + V_3 \end{bmatrix} \tag{6.54}$$

Fig. 6.7 presents the interpretation of the new currents I_{123}, which is needed to design the control strategy. As mentioned in Section 3.6, the new currents have ac and dc components, but only the dc components are allowed on the dc sides. This can be achieved by controlling the legs to be balanced, i.e. without ac homopolar components.

The equivalent path of I_1 is presented in Fig. 6.7a. It is the current through the ground between the two interconnected systems. The ground current is controlled to zero in steady-state operation. However, I_1^{dc} can be useful to balance the poles on the SyM side, e.g. after a transient a current though the ground can be used to regain the steady-state condition $V_{L1} = V_{L2}$. The current I_2, presented in Fig. 6.7b, is the current that links the three arms with the HV side. I_3 is the current on the LV loop as presented in Fig. 6.7c. All three currents may have ac components (dashed lines) that are controlled to circulate inside the converter without disturbing the dc sides. Fig. 6.7 presents the single-phase circuit, but since the converter has at least two legs, the ac currents circulate between the n-phases of the complete converter (see modeling hypotheses in Section 3.3). From the variable transformations and Fig. 6.7, it can be noticed that $V_2^{dc} = V^{dc}$ and that $V_3^{dc} I_3^{dc} = P_T^{dc}/N_{legs}$.

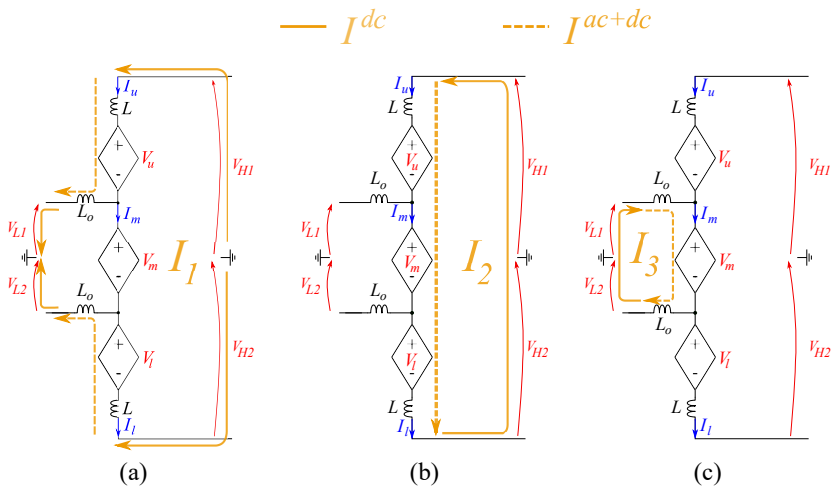


Figure 6.7: Physical interpretation of the equivalent currents for the flexible dc-MMC. (a) I_1, (b) I_2, and (c) I_3.

6.5.2 Energy control

Energy in the dc-dc converter should be controlled during the complete operation including the dynamic variations produced by changes in the system, e.g. power, voltage, or current disturbances. The energy control follows the methodology presented in Section 3.6.2, where the average value of a set of equivalent energies is regulated with a PI controller.

The energy control controls equivalent energies, which are a linear combination of the arm energies. The energy transformation, $\boldsymbol{W_T}$, used to find the equivalent energies for the flexible dc-MMC is:

$$\boldsymbol{W_T} = \begin{bmatrix} 1 & 1 & 1 \\ 1 & -1 & 1 \\ 1 & 0 & -1 \end{bmatrix} \tag{6.55}$$

The new set of energies is:

$$\begin{bmatrix} E_\Sigma \\ E_{\Delta T} \\ E_{u-l} \end{bmatrix} = \boldsymbol{W_T} \begin{bmatrix} E_u \\ E_m \\ E_l \end{bmatrix} = \begin{bmatrix} E_u + E_m + E_l \\ E_u - E_m + E_l \\ E_u - E_l \end{bmatrix} \tag{6.56}$$

and their dynamic variations are:

$$\frac{d}{dt}\begin{bmatrix} E_\Sigma \\ E_{\Delta T} \\ E_{u-l} \end{bmatrix} = \boldsymbol{W_T} \begin{bmatrix} P_u \\ P_m \\ P_l \end{bmatrix} = \begin{bmatrix} P_u + P_m + P_l \\ P_u - P_m + P_l \\ P_u - P_l \end{bmatrix} \tag{6.57}$$

where E_Σ is the sum of all arm energies in a leg, $E_{\Delta T}$ is the energy difference between the three arms, and E_{u-l} is the energy difference between the upper and lower arms.

Using expressions (6.52) and (6.54), the power per arm can be expressed in terms of the new variables 123 as follows:

$$P_u = -V_1 I_1 - V_1 I_2 - V_2 I_1 - V_2 I_2 + V_3 I_1 + V_3 I_2 \tag{6.58}$$

$$P_m = -2\left(V_3 I_2 + V_3 I_3\right) \tag{6.59}$$

$$P_u = -V_1 I_1 + V_1 I_2 + V_2 I_1 - V_2 I_2 - V_3 I_1 + V_3 I_2 \tag{6.60}$$

Replacing (6.58), (6.59), and (6.60) in (6.57), yields to:

$$\frac{d}{dt}E_{\Sigma} = -2\left(V_1 I_1 + V_2 I_2 + V_3 I_3\right) \tag{6.61}$$

$$\frac{d}{dt}E_{\Delta T} = 2\left(-V_1 I_1 - V_2 I_2 + 2V_3 I_2 + V_3 I_3\right) \tag{6.62}$$

$$\frac{d}{dt}E_{u-l} = 2\left(-V_1 I_2 - V_2 I_1 + V_3 I_1\right) \tag{6.63}$$

The controllers are presented in the following subsections. Each energy controller, $K_E(s)$, uses a notch filter to avoid the first and second harmonic components in the measurement (see Fig. 3.10), and a PI controller as explained in Section 3.6.2.

Total energy controller

The energy controllers designed in Section 3.6.2 follow only the average value of the energy. Recalling that the new variables 123 have ac and dc components, the average value of the total power, found in (6.61), in the time can be expressed as:

$$\begin{aligned}\left\langle \frac{d}{dt}E_{\Sigma} \right\rangle = &-2\left(V_1^{dc} I_1^{dc} + V_2^{dc} I_2^{dc} + V_3^{dc} I_3^{dc}\right) \\ &- 2\frac{V_1^{ac} I_1^{ac}}{2}\cos\left(\theta_{V_1} - \theta_{I_1}\right) \\ &- 2\frac{V_2^{ac} I_2^{ac}}{2}\cos\left(\theta_{V_2} - \theta_{I_2}\right) \\ &- 2\frac{V_3^{ac} I_3^{ac}}{2}\cos\left(\theta_{V_3} - \theta_{I_3}\right)\end{aligned} \tag{6.64}$$

Similar to the new variables 1,2 found from the u, l variables in Chapter 5, the ac voltage, V_i^{ac}, and ac current, I_i^{ac}, are in quadrature (for $i \in 1, 2, 3$). Thus, the average value $\langle V_i^{ac} I_i^{ac} \rangle = 0$. Additionally, the dc current I_1^{dc} should be zero in steady-state conditions to avoid dc currents through the ground (see Fig. 6.7a). Therefore, the total energy can be simplified as follows:

$$\left\langle \frac{d}{dt}E_{\Sigma} \right\rangle = -2\left(V_2^{dc} I_2^{dc} + V_3^{dc} I_3^{dc}\right) \tag{6.65}$$

The current I_2^{dc} is used for the total energy control as it links the three arms in the leg (see Fig. 6.7b). Using the dc steady-state values found in Section 6.3.1 and the transformations (6.51) and (6.53), the reference

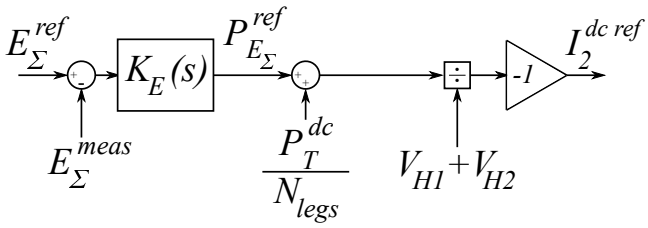


Figure 6.8: Total energy controller for the flexible dc-MMC and the relation with the current reference.

for the current I_2^{dc} corresponds to:

$$I_2^{dc\ ref} = \frac{P_{E_\Sigma}^{ref} + \frac{P_T^{dc}}{N_{legs}}}{V_{H1} + V_{H2}} \tag{6.66}$$

where $P_{E_\Sigma}^{ref}$ is the output of the total energy controller, P_T^{dc} is the power transmitted between HV and LV side, and N_{legs} is the number of legs of the converter. The structure of the total energy controller is presented in Fig. 6.8, where the reference for the energy is given by:

$$E_\Sigma^{ref} = \frac{1}{2}\left(C_{eq_u}V_{C_{eq_u}}^2 + C_{eq_m}V_{C_{eq_m}}^2 + C_{eq_l}V_{C_{eq_l}}^2\right) \tag{6.67}$$

Energy total difference controller

The second energy controller, $E_{\Delta T}$ defined in (6.62), here called total energy difference because it involves the three arms. It compares the energy in the middle arm with the external arms, to keep their difference constant.

Recalling that the dc component of I_1 is zero, the average value of $\frac{d}{dt}E_{\Delta T}$ is:

$$\begin{aligned}\left\langle \frac{d}{dt}E_{\Delta T} \right\rangle =& 2\left(-V_2^{dc}I_2^{dc} + 2V_3^{dc}I_2^{dc} + V_3^{dc}I_3^{dc}\right) \\ &+ 4\frac{V_3^{ac}\,I_2^{ac}}{2}\cos\left(\theta_{V_3} - \theta_{I_2}\right)\end{aligned} \tag{6.68}$$

In this case, the total difference energy is controlled with I_2^{ac} as this current links the three arms in a leg of the flexible dc-MMC (see Fig. 6.7b). The reference for the current I_2^{ac} and its relation with the energy total

difference can be expressed as:

$$I_2^{ac\,ref} = \frac{\frac{P_{E_{\Delta T}}^{ref}}{2} + V_2^{dc} I_2^{dc} - 2V_3^{dc} I_2^{dc} - V_3^{dc} I_3^{dc}}{2V_3^{ac} \cos\left(\theta_{V_3} - \theta_{I_2}\right)}. \tag{6.69}$$

Using the steady-state conditions the expression above leads to:

$$I_2^{ac\,ref} = \frac{\frac{P_{E_{\Delta T}}^{ref}}{2} + \left(\frac{V_{L1}+V_{L2}}{V_{H1}+V_{H2}} - 1\right) \frac{P_T^{dc}}{N_{legs}}}{2V_3^{ac} \cos\left(\theta_{V_3} - \theta_{I_2}\right)}. \tag{6.70}$$

The relation between the total difference energy controller and the current reference is presented in Fig. 6.9. The controller is implemented for the n legs of the converter. The output of the n controllers are fed into the matrix $\boldsymbol{M_k}$, which is used to assure the balance between phases [136]. As explained in Section 3.6.2, the energy controllers, $K_E(s)$, are PI controllers that govern the average energy. The controller sets the amplitude of the current I_2^{ac}, while the sinus with the angle is set from the optimizations results obtained in Section 6.3.4. The voltage disturbance $V_{D_{\Delta T}}$ (see Section 3.6.2), corresponds to the denominator of (6.70) and it is calculated at the nominal operation, i.e. the control implemented has a fixed $V_{D_{\Delta T}}$, and the dynamic variations caused by the operating conditions are corrected by the PI controller.

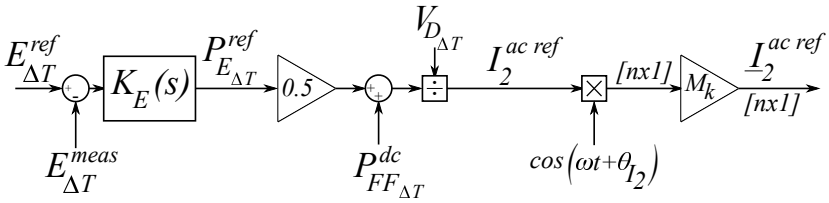


Figure 6.9: Total difference energy controller for the flexible dc-MMC and the relation with the current reference.

The term $P_{FF_{\Delta T}}^{dc}$ is the dc power feed forward obtained from (6.70), and it corresponds to:

$$P_{FF_{\Delta T}}^{dc} = \left(\frac{V_{L1} + V_L}{V_{H1} + V_{H2}} - 1\right) \frac{P_T^{dc}}{N_{legs}}. \tag{6.71}$$

The energy reference $E_{\Delta T}^{ref}$ is:

$$E_{\Delta T}^{ref} = \frac{1}{2}\left(C_{eq_u} V_{C_{equ}}^2 - C_{eq_m} V_{C_{eqm}}^2 + C_{eq_l} V_{C_{eql}}^2\right) \tag{6.72}$$

where $V_{C_{eq_i}}$ is the reference voltage of the arm equivalent capacitance, with $i \in u, m, l$.

Energy difference between the upper and lower arm

Expression (6.63) represents the energy difference between the upper and lower arm. Reminding that the dc components of V_1 and I_1 are controlled to zero, the average value of $\frac{d}{dt}E_{u-l}$ is:

$$\begin{aligned}\left\langle \frac{d}{dt}E_{u-l} \right\rangle = &- 2\frac{V_1^{ac}\, I_2^{ac}}{2}\cos\left(\theta_{V_1} - \theta_{I_2}\right) \\ &- 2\frac{V_2^{ac}\, I_1^{ac}}{2}\cos\left(\theta_{V_2} - \theta_{I_1}\right) \\ &+ 2\frac{V_3^{ac}\, I_1^{ac}}{2}\cos\left(\theta_{V_3} - \theta_{I_1}\right).\end{aligned} \tag{6.73}$$

In this case there is no possibility to control the energy with dc currents, only the ac currents participate in a non-null average power value. I_1^{ac} is used for this controller as it links the upper and lower arm without an effective interaction with the middle arm (see Fig. 6.7a). The magnitude of I_1^{ac} current reference, depending on the energy controller output can be expressed as:

$$I_1^{ac\,ref} = \frac{P_{E_{u-l}}^{ref} + V_1^{ac}\, I_2^{ac}\cos\left(\theta_{V_1} - \theta_{I_2}\right)}{V_3^{ac}\cos\left(\theta_{V_3} - \theta_{I_1}\right) - V_2^{ac}\cos\left(\theta_{V_2} - \theta_{I_1}\right)}. \tag{6.74}$$

The control scheme for the E_{u-l} is presented in Fig. 6.10, where P_{FF}^{ac} and $V_{D_{u-l}}$ are the feed forward power and voltage disturbance from (6.74). Similar to the $E_{\Delta T}$, the E_{u-l} controller is implemented in the n phases of the converter and balanced with the matrix $\boldsymbol{M_k}$. The sinus and its angle are set from the optimization results found in Section 6.3.4.

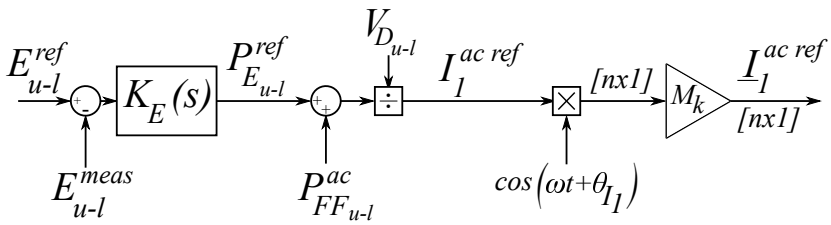


Figure 6.10: Difference (up-low) energy controller for the flexible dc-MMC, and the relation with the current reference.

The energy reference E_{u-l}^{ref} is:

$$E_{u-l}^{ref} = \frac{1}{2}\left(C_{eq_u}V_{C_{eq_u}}^2 - C_{eq_l}V_{C_{eq_l}}^2\right). \tag{6.75}$$

6.5.3 Current control

From the decoupled system found in (6.50), three current controllers are implemented. The current controllers are proportional-integral-resonant (PIR) following the structure presented in (3.82) [129]. The parameters presented in Table 6.3 are used to tune the PIRs. The implementation is presented in Fig. 6.11.

Table 6.3: Parameters to tune the current controllers of the flexible dc-MMC

	L_{eq}	R_{eq}	V_{eq}	ϕ_{PM}	T_d
I_1	$L + L_o$	$R + R_o$	$V_1 + \frac{V_{H1}-V_{H2}-V_{L1}+V_{L2}}{2}$	60°	40 µs
I_2	L	R	$V_2 + \frac{V_{H1}+V_{H2}}{2}$		
I_3	L_o	R_o	$V_3 + \frac{V_{L1}+V_{L2}}{2}$		

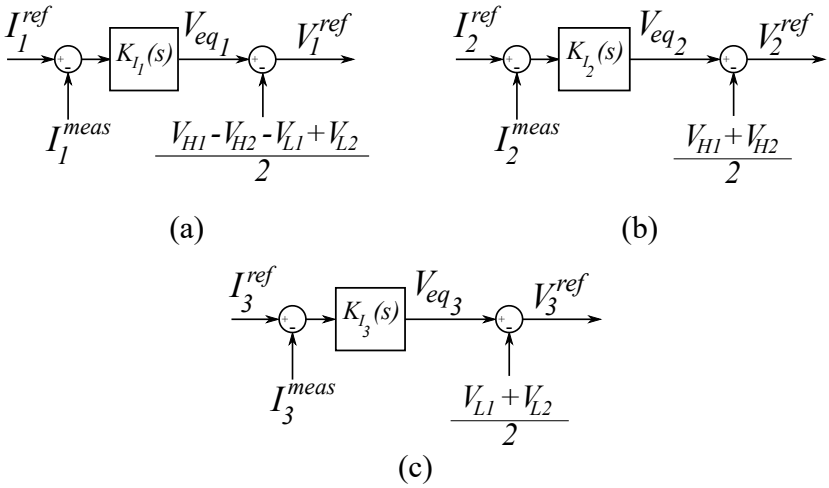


Figure 6.11: Current controllers for the equivalent currents of the flexible dc-MMC. (a) I_1, (b) I_2, and (c) I_3.

6.5.4 Power reference

The power reference is calculated using the dc component of I_3, as this current is equivalent to the dc current on the LV side ($I_3^{dc} = -I_L$). Thus, the dc power can be used to set the reference of I_3^{dc}, as follows:

$$I_3^{dc\,ref} = -\frac{1}{V_{L1} + V_{L2}} \frac{P_T^{dc}}{N_{legs}}. \tag{6.76}$$

The reference is set to the current controller in open loop, i.e. there is no power controller implemented.

6.5.5 Pole balancing control

The flexible dc-MMC is able to control the unbalance between the poles on the SyM line. Using the interpretation of the new currents I_{123} (see Fig. 6.7), the current I_1^{dc} can be used for this purpose. Assuming that the MMCs connected to the line fix the pole-to-pole voltage, I_1^{dc} can increase the pole-to-ground voltage V_{L1} while reducing V_{L2}. This action can balance the poles with respect to the ground. The control assumes the plant as the equivalent capacitor of the cable on the SyM line, the estimated closed loop is shown in Fig. 6.12.

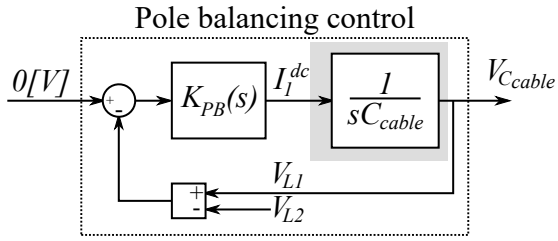


Figure 6.12: Closed loop estimation for the pole balancing control tuning.

The plant for the design of the pole balancing controller is an integrator depending on the capacitance of the cable. The controller K_{PB} is a PI controller. The closed loop describes a characteristic equation of second order, which is compared to an objective second order system to define the constants of the PI controller. The objective second order response considers a damping factor $\zeta = 0.7$ and a time constant five times greater than the energy control time constant (see Section 3.6.2), as follows:

$$\tau_{pole\,bal} = 5\tau_E \tag{6.77}$$

$$\omega_{pole\,bal} = \frac{1}{5\tau_E} \tag{6.78}$$

The PI gains can be found with the following expressions:

$$K_i = \frac{C_{cable}}{(5\tau_E)^2} \tag{6.79}$$

$$K_p = \frac{1.4 \cdot C_{cable}}{5\tau_E} \tag{6.80}$$

The time constant for the energy control is $\tau_E \sim 29$ ms, and the estimated capacitance of the cable on the SyM is $C_{cable} \sim 21.3\,\mu$F (see Section 4.3.2) thus, the K_i and K_p gains are:

$$K_i \approx 1 \times 10^{-3}\ \ \mathrm{F\,s^{-2}} \tag{6.81}$$

$$K_p \approx 0.2 \times 10^{-3}\ \ \mathrm{F\,s^{-1}} \tag{6.82}$$

6.5.6 Control summary

The summary of the different components of the equivalent currents and their use on the control strategy is presented in Table 6.4. The current I_3^{ac} is set from the results obtained in Section 6.3.4, i.e. it does not change depending on the operating point.

Table 6.4: Different components of the equivalent currents I_{123}, and their use in the control strategy of the flexible dc-MMC.

Current	Control use
I_1^{dc}	Pole balancing on the LV side
I_1^{ac}	E_{u-l} control
I_2^{dc}	E_Σ control
I_2^{ac}	$E_{\Delta T}$ control
I_3^{dc}	P_T^{dc} reference on the LV side
I_3^{ac}	Reference set from the steady-state solution

The current references for the degraded modes are calculated replacing $V_{H1} = 0$ or $V_{H2} = 0$ in the steady-state analysis and control references. The current reference $I_3^{ac\,ref}$ change to follow the optimization results (see Appendix C.1).

The general control strategy implemented for the flexible dc-MMC is presented in Fig. 6.13. Compared to the control implemented on the F2F-MMC (see Fig. 5.11) the flexible dc-MMC implements the pole balancing controller and requires a pre-calculated reference for I_3.

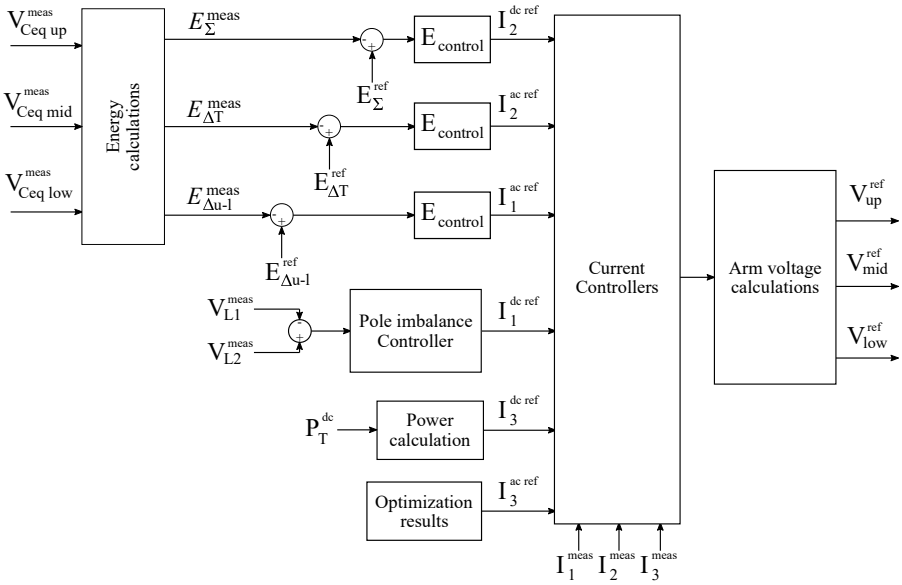


Figure 6.13: General control strategy implemented for the flexible dc-MMC.

6.5.7 Dc faults in a flexible dc-MMC

In Section 6.3.4, a preliminary analysis for the faults on the flexible dc-MMC has been done to find the voltage requirements, i.e. to evaluate the number of HB and FB SMs needed to withstand different faults. But the general behavior of the dc-dc converter has not been addressed.

From Table 6.1 the voltage requirements per arm, per fault case, can be identified. These values have been found analytically using the mathematical model. These voltage requirements can also be identified from the circuit diagram. Figure 6.14 presents the case where a fault pole-to-ground on the HV side. When the fault occurs, the upper arm need to withstand $-V_{L1}$ to stop the fault current contribution from the LV side. During the time to block the current, the healthy pole of the bipole is disturbed due to the loop shown in Fig. 6.14a. Ideally, the control strategy could be adjusted to control the flexible dc-MMC during the fault but, to continue in degraded operation the fault must be isolated.

Figure 6.14b presents the operation in degraded mode after the fault isolation. To achieve this configuration the converter should be blocked to isolate the faulted pole, and re-started to operate in degraded mode.

The flexible dc-MMC does not provide immediate redundancy, the converter does not have the capacity to isolate the fault, change the control strategy references without affecting the power through the healthy pole of the bipole.

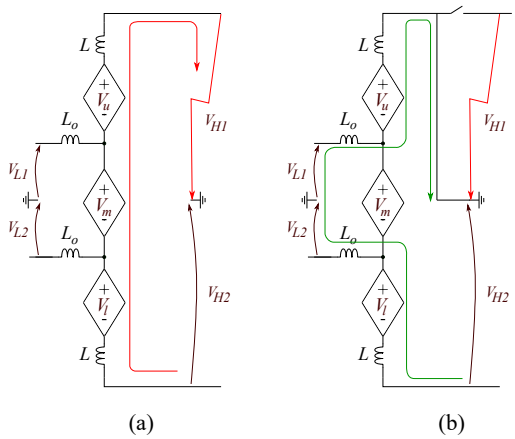


Figure 6.14: (a) fault on the HV side of the flexible dc-MMC. (b) degraded mode operation after the fault isolation.

6.6 Case study simulations and results

The case study chosen for this thesis is the interconnection between a bipole and a SyM. The general scheme is presented in Fig. 6.15. Additional details can be found in Chapter 4.

Since the flexible dc-MMC does not provide immediate redundancy, additional disconnectors should be included to isolate the faults on the HV side. Figure 6.16 presents the simulated model. Two sets of switches are added to the converter to isolate the faulted pole on the bipole side. SW_1 is composed of a switch in series, normally closed, and a shunt switch, normally open. A similar switch is used to isolate the faults on the negative pole of the bipole, SW_2. In case of a fault the current is stopped and the respective set of switches are activated, either SW_1 or SW_2.

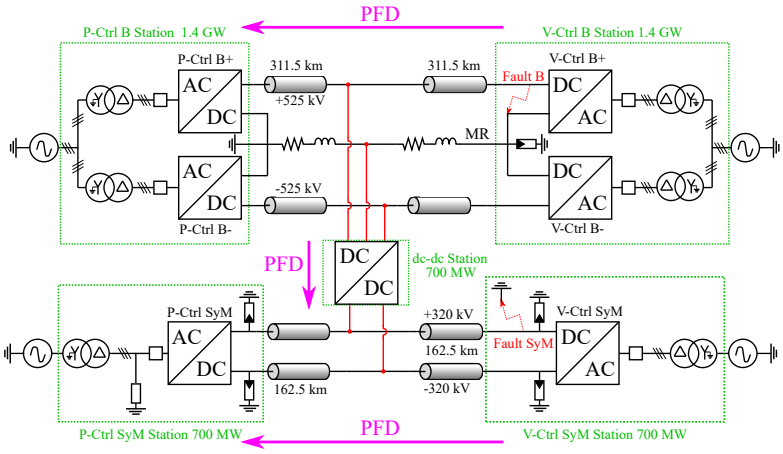


Figure 6.15: Case study system proposed for this thesis and the positive convention for the power flow directions (PFD), see Chapter 4.

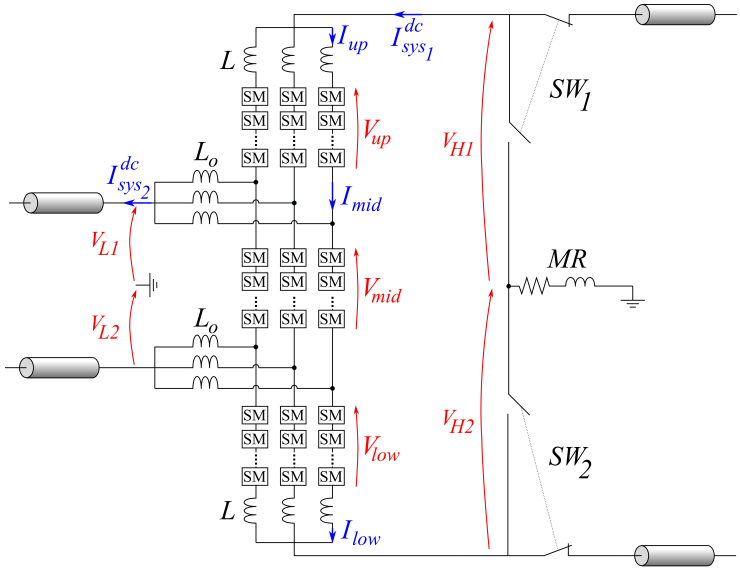


Figure 6.16: Simulated flexible dc-MMC. The metallic return (MR) is not connected during normal operation.

The converter analysis has been done neglecting the losses in the circuit. For the simulation model the arm resistances are included based on the number of SMs per arm. The arm resistance is calculated as:

$$R_{arm} = R_{IGBT} \cdot (2 \cdot N_{FBSMs} + N_{HBSMs}) \tag{6.83}$$

where R_{IGBT} is the IGBT on-state equivalent resistance, N_{FBSMs} and N_{HBSMs} is the number of FB and HBSMs in the arm respectively.

Assuming an on-state resistance of the IGBT of 1 mΩ, and using the number of SMs found in Table 6.2, the equivalent resistance per arm are: $R_u = 0.744\Omega$, $R_m = 0.661\Omega$, and $R_l = 0.744\Omega$. This estimation neglects the circuit inductor equivalent resistance which can be comparable to these values but do not interfere with the converter operation.

6.6.1 Normal operation

The nominal converter operation is simulated to verify the converter sizing and control design. The results from the nominal operation can be found in Appendix C.3.1.

The normal operation simulations test the dc-dc converter power exchange capability with a power reference of 500 MW and multiple power flow directions (see Chapter 4). The normal operation is tested in six different scenarios proposed in Table 4.4. The results of Case 4 are presented as they represent the worst results from the six simulated cases.

The system results, for Case 4 in Table 4.4, are presented in Fig. 6.17. In this scenario, the power in the bipole line is fixed to 900 MW and the power in the SyM line is fixed to 200 MW. The power through the flexible dc-MMC is 500 MW initially from the bipole to the SyM and then the power flow is inverted from the SyM to the B line. The power per converter station is presented in Fig. 6.17a. The power-controlled stations keep their power constant (dashed lines), while the voltage-controlled stations adjust their power to maintain the dc voltage stable.

The dc voltages measured at the terminals of the flexible dc-MMC are presented in Fig. 6.17b. It can be noticed that the changes in the power flow disturbs the dc voltages. However, the maximum dynamic variations are within the normal operation limits, i.e. $\pm 5\%$. The dc voltages in steady-state can be different from the nominal value due to the virtual capacitor controller implemented in the ac-dc converters. The dynamic variations of the dc voltage in the SyM line are bigger than those of the bipole line because the former has a smaller equivalent line capacitance.

The energy variations per converter station are presented in Fig. 6.17c. The power-controlled stations have an energy level, in steady-state conditions, different from their nominal value as the virtual capacitor controls the energy depending on the voltage drop in the line. This voltage drop is required to have a power flow in the dc system. The greater the power transmitted, the higher the voltage drop in the line.

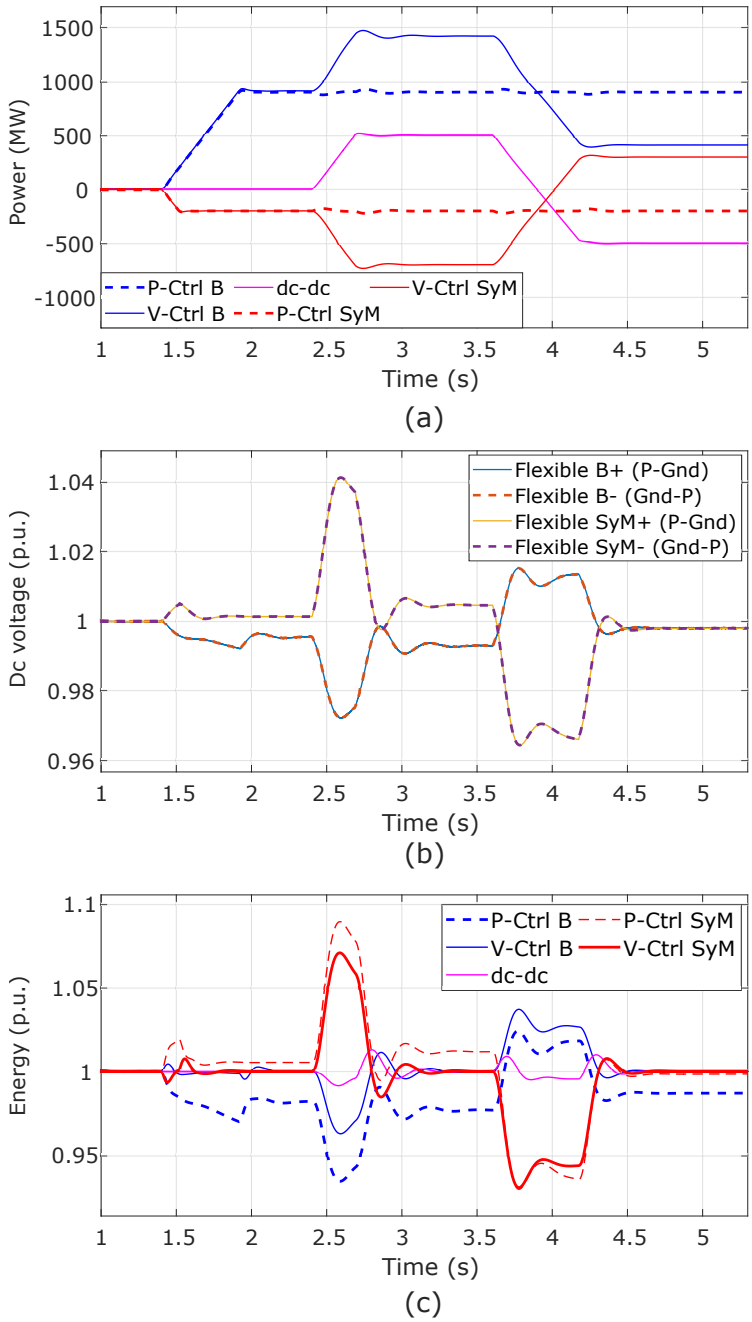


Figure 6.17: Results for the normal operation of the flexible dc-MMC (Case 4). (a) The power per converter station, (b) the dc voltages at the terminals of the dc-dc converter, and (c) the energy per converter station.

The arm voltages are presented in Fig. 6.18. It can be noticed that the upper and lower arm voltages are in phase and have the same dc offset, similar to the nominal operation results (see Fig. 6.6 and Appendix C.3.1). The dc offsets have small changes according to the power exchanges.

The arm currents are presented in Fig. 6.19. Similar to the arm voltages, the arm current dc offsets follow the changes in the power reference. Around 3.9 s, a change on the power direction can be evidenced. With the change of power flow direction the phases of the arm currents are changed. the current in the middle arm does not change as the upper and lower arm currents as I_m is linked to I_3 which has a power-invariant reference from the optimization results (see Table 6.4).

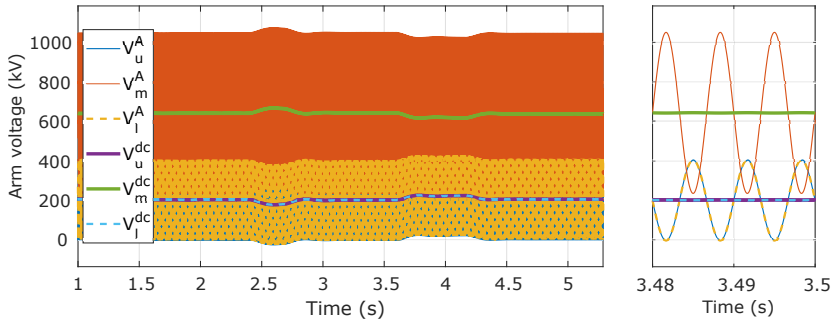


Figure 6.18: Arm voltages per arm of the flexible dc-MMC in normal operation, Case 4. Only the phase A is presented.

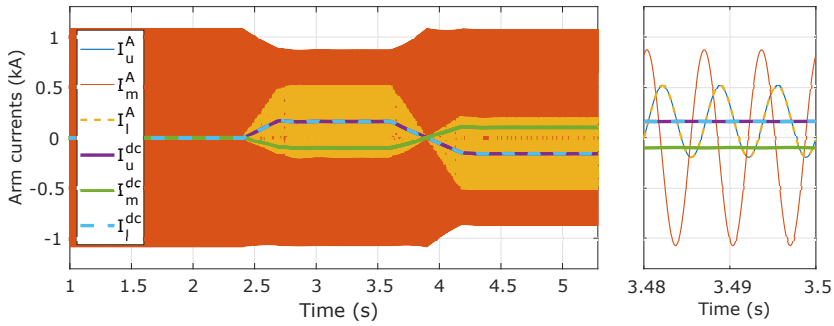


Figure 6.19: Arm currents per arm of the flexible dc-MMC in normal operation, Case 4. Only the phase A is presented.

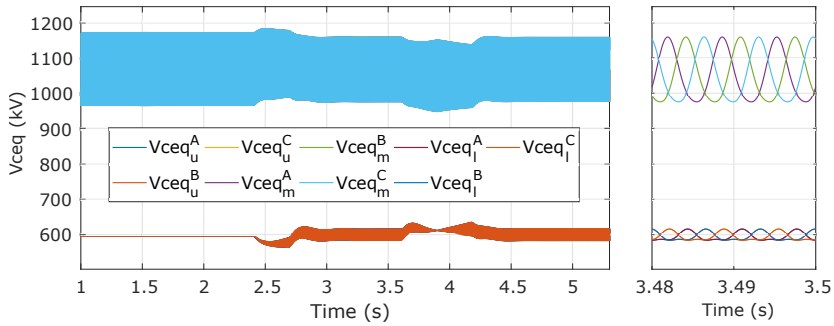


Figure 6.20: Voltage of the equivalent arm capacitance in normal operation of the flexible dc-MMC, Case 4.

The voltage on the equivalent arm capacitances are presented in Fig. 6.20. It can be noticed that the energy is controller during the power reference changes.

The maximum and minimum dc voltage measured at the terminals of the flexible dc-MMC, for the six proposed cases, are presented in Fig. 6.21. Similarly, the maximum energy dynamic variations are presented in Fig. 6.22.

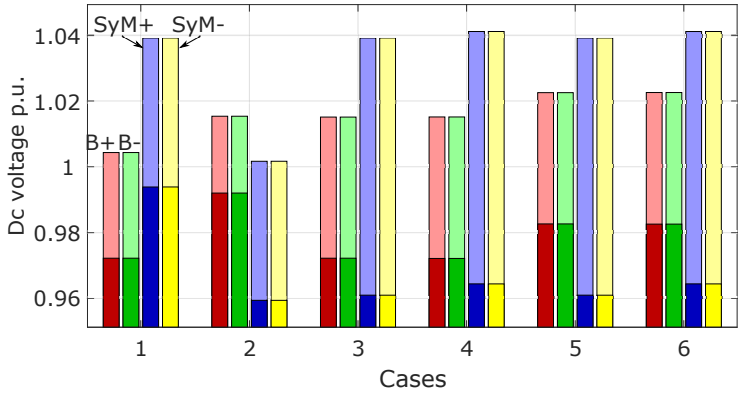


Figure 6.21: Maximum (light bars) and minimum (dark bars) pole-to ground dc voltage registered in the flexible dc-MMC for the six cases of normal operation (see Table 4.4). Red, green, blue, and yellow are the voltages of the positive pole of the bipole, negative pole of the B, the SyM positive pole, and SyM negative pole respectively.

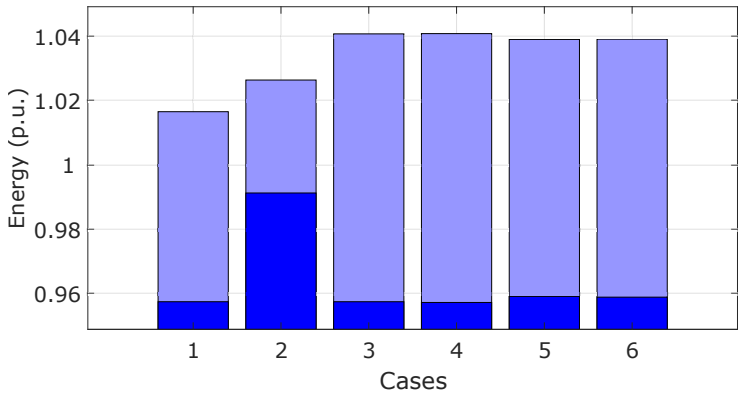


Figure 6.22: Maximum (light bars) and minimum (dark bars) total energy of the flexible dc-MMC for the six cases of normal operation (see Table 4.4).

6.6.2 Fault scenarios

Following the different power flow scenarios proposed in Table 4.5, eight simulations with a fault on the bipole line, and eight simulations considering a fault on the SyM are performed. The results are presented in the following sections.

Fault on the bipole line

When a fault on the bipole line occurs, the dc-dc converter should avoid the fault propagation to the healthy zones, i.e. the healthy pole of the bipole and the SyM. Providing immediate redundancy is the ideal behavior of a dc-dc converter but, as it was mentioned before, the flexible dc-MMC is not able to continue uninterrupted power exchange with the healthy pole of the bipole (see Fig. 6.14). At the instant of a fault, the flexible dc-MMC must be blocked, reconfigured and re-started to provide degraded operation.

The system results, for the Case 8 in Table 4.4, are presented in Fig. 6.23. The power per converter station is presented in Fig. 6.23a. The power references, followed by the power-controlled stations before the fault, are -900 MW in the bipole, -200 MW in the SyM, and -500 MW through the flexible dc-MMC. Short after the fault event (hundred of µs after the fault detection), the flexible dc-MMC is blocked and the power through the converter drops to zero (magenta line). The power in the bipole (power and voltage-controlled stations) drops to half of the reference power as it has lost a pole, i.e. from 900 MW to 450 MW. The power

in the voltage-controlled station on the SyM drops to -200 MW (equal to the power reference in that line). After blocking the flexible dc-MMC, the bypass switch SW_1 (see Fig. 6.16), is activated to isolate the faulted pole. The flexible dc-MMC has been set to re-start after 140 ms after the fault exchanging 350 MW (half of the rated power) using the healthy pole of the bipole. In other words, after the circuit reconfiguration, the flexible dc-MMC is able to operate in a degraded mode interconnecting an AM with a SyM. The dc system regains steady-state conditions after 0.9 s after the fault event.

The dc voltages at the terminals of the flexible dc-MMC are presented in Fig. 6.23b. It can be noticed that at the time of the fault, the dc voltages on the SyM line have considerable overvoltages but, they do not trigger the fault blocking signal (see Section 4.3.6). Before the fault the voltage-controlled station on the SyM line was feeding the dc-dc converter. When the flexible dc-MMC is blocked, the voltage-controlled station takes some time to adjust the input dc power. The excess of energy in the dc system is seen as a temporal overvoltage. After the fault event and the re-start of the flexible dc-MMC, the lines recover steady-state conditions.

The dc currents measured at the terminals of the flexible dc-MMC are presented in Fig. 6.23c. At the time of the fault, there is a current transient of 2 kA on the bipole side. The dc current peak at the SyM side is only 500 A. The flexible dc-MMC is blocked and the fault current through the converter is stopped under 10 ms. Around 4.2 s the flexible dc-MMC is restarted in degraded mode exchanging power with the healthy pole.

The energy per converter station is presented in Fig. 6.23d. It can be noticed that the energies of all converters are controlled and can recover steady-state conditions. At the time of the fault, the energy in the SyM MMCs increase considerably. This is because part of the excess of energy injected from the voltage-controlled station is absorbed by the converters with virtual capacitor control. After the fault is isolated, the dc-dc converter controls its energy to reach steady-state conditions.

The detailed converter results, at the time of the fault event, are presented in Fig. 6.24. The voltages at the terminals of the stack of SMs are presented in Fig. 6.24a, b, and c for the upper, middle, and lower arm respectively. The arm voltages have a fast transient at the instant of the fault (3.7 s) and the converter is blocked after some ms after the fault detection. During the blocked state, the arm voltages follow the dc voltage set by the external dc systems. In this case, only the upper arm

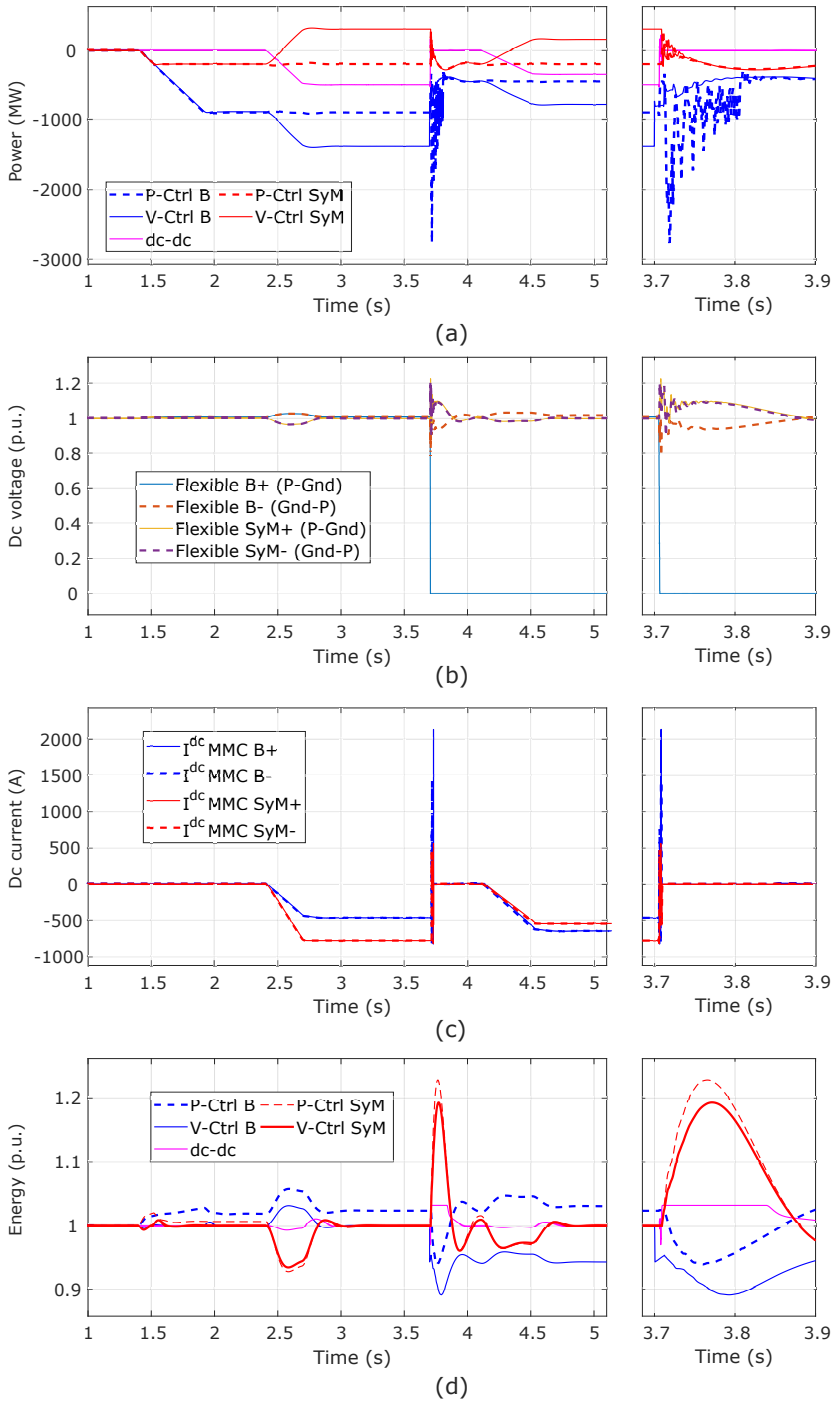


Figure 6.23: Simulation results for the flexible dc-MMC. The power flow of Case 8 (see Table 4.5) is simulated with a fault on the B line. (a) The power per converter station, (b) the dc voltages at the terminals of the dc-dc converter, (c) the dc currents at the terminals of the flexible dc-MMC, and (d) the energy per converter station.

changes its dc voltage from 205 kV to -320 kV as the positive pole of the bipole goes to zero. The middle and lower arms remain at 640 kV and 205 kV respectively.

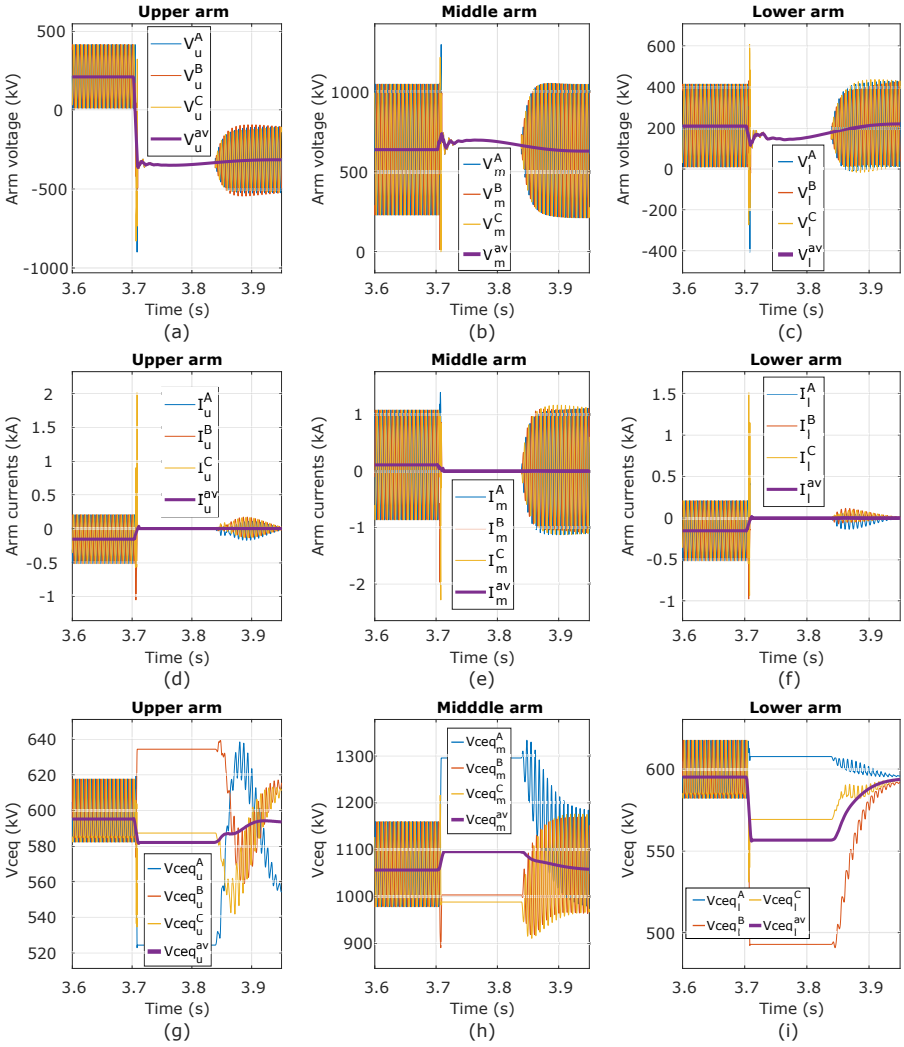


Figure 6.24: Arm voltage (first row), arm currents (second row), and voltage of C_{eq} (third row), for the upper, middle, and lower arm of the flexible dc-MMC, when the fault is located on the bipole side (Case 8).

The arm currents are presented in Fig. 6.24d, e, and f for the upper, middle, and lower arm respectively. Similar to the arm voltages, the arm currents are subject to a fast transient at the instant of the fault. After

the converter is blocked, the arm currents are stopped within a few ms. When the converter is restarted, the arm currents in the upper and lower arm have a small disturbance (less than 200 A) to re-balance the energy in the converter. The middle arm has the nominal current because this current is proportional to I_3^{ac}, which is set from the ac solution found for the degraded mode (see Appendix C.2 and Table 6.4).

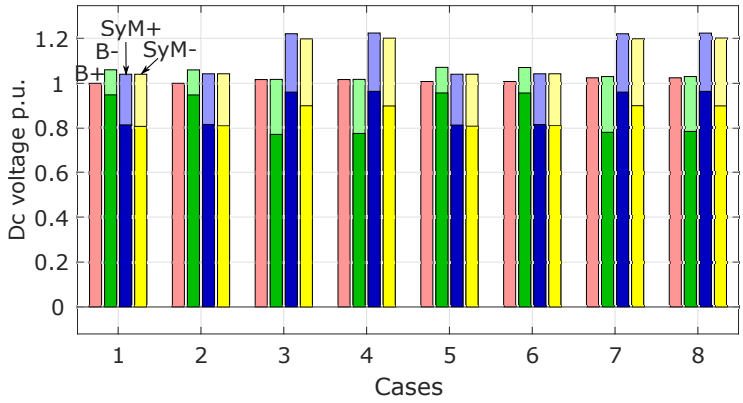


Figure 6.25: Maximum (light bars) and minimum (dark bars) pole-to-ground dc voltages registered in the flexible dc-MMC for the eight fault cases (see Table 4.5), when the fault is located on the bipole line. Red, green, blue, and yellow are the voltages of the positive pole of the bipole, negative pole of the B, the SyM positive pole, and SyM negative pole respectively.

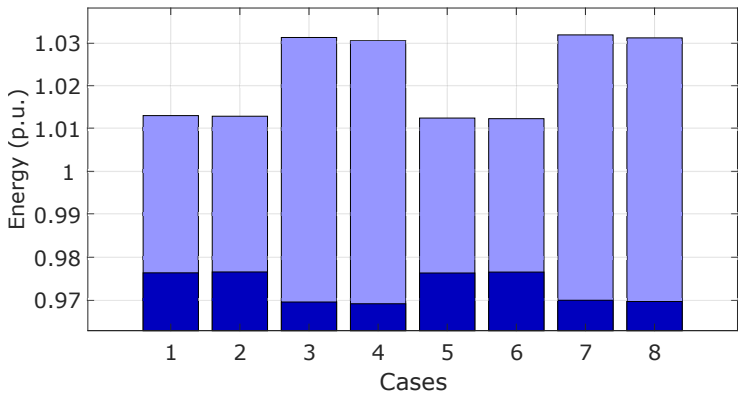


Figure 6.26: Maximum (light bars) and minimum (dark bars) total energy of the flexible dc-MMC for the eight cases in Table 4.5, when the fault is on the bipole line.

The voltage of the arm equivalent capacitance is presented in Fig. 6.24g, h, and i, for the upper, middle, and lower arm respectively. At the time of the fault, and during a short time (less than 10ms), the flexible dc-MMC control acts to keep the exchanged power (-500 MW) by discharging some arms, e.g. the lower arms. When the converter is blocked, the currents in the circuit take some ms to drop to zero. During this time, the capacitors in the HBSMs can be charged if a positive current goes through the arm, and the capacitors on the FBSMs are charged for any current polarity in the arm. The charging event can be observed in some of the phases in the upper and middle arm. When the flexible dc-MMC is unblocked (3.84 s), the energy control recovers the energy steady-state conditions after another 160 ms i.e., around t=4s, (magenta line presented in Fig. 6.23c).

The different cases proposed in Table 4.5 were simulated obtaining similar results. In general, the flexible dc-MMC is capable to act as a firewall in case of a fault on the bipole line. The healthy zones, i.e. negative pole of the bipole and the SyM line, have considerable disturbances during the fault event but, the lines can recover steady-state conditions. The flexible dc-MMC can block the fault currents in a short period of time (a few ms). After the circuit reconfiguration using SW_1, see Fig. 6.16, the flexible dc-MMC can reestablish the power flow between the healthy zones in degraded mode operation.

The maximum and minimum dc voltage dynamic variations are presented in Fig. 6.25. The energy dynamic variations are presented in Fig. 6.26. The results previously presented, Case 8, correspond to one of the cases with greater voltage and energy dynamic variations.

Fault on the symmetric monopole line

For the fault scenarios when the fault is located on the SyM line, the flexible dc-MMC is blocked without a re-starting sequence. The degraded mode operation is not available on the monopole side thus, the dc-dc converter remains blocked until the fault is cleared. This strategy allows to keep the healthy zones operational, i.e. the positive and negative poles of the bipole (see Fig. 4.8).

The eight different power flow directions proposed in Table 4.5 are simulated to test the dc-dc converter behavior. The system results for Case 5 are presented in Fig. 6.27. The power per converter station is presented in Fig. 6.27a. As expected, after blocking the flexible dc-MMC, the powers on the SyM line and the dc-dc converter are zero, while the power on the bipole regains the conditions as if the dc-dc was

not connected, i.e. the voltage-controlled station has the same power as the power-controlled station. The bipole line can recover steady-state conditions, thanks to the fast blocking of the flexible dc-MMC, under 300 ms.

The voltages measured at the terminals of the flexible dc-MMC are presented in Fig. 6.27b. The positive pole of the SyM line (faulted pole), drops to zero while the negative pole is subject to an overvoltage limited by the surge arresters (see Section 4.3.3). The voltages measured on the bipole side have small disturbances (less than 9%), which are damped by the line control. From the bipole line perspective, the fault on the SyM line is equivalent to a power disturbance of 500 MW.

The dc currents measured at the terminals of the flexible dc-MMC are presented in Fig. 6.27c. Similar to the fault on the bipole line, at the moment of the fault the dc current increases up to 1.5 kA on the bipole line and around 1.1 kA for the dc current on the SyM. The dc-dc converter is blocked under 1 ms and the fault currents are stopped under 15 ms allowing the bipole line to continue normal operation. Different from the fault on the bipole, the fault on the monopole does not have degraded operation, i.e. the flexible dc-MMC remains blocked until the end of the simulation.

The energy per converter station is presented in Fig. 6.27d. After the fault detection, the dc-dc converter is blocked and the arm currents are stopped thanks to the installed FBSMs. The FBSMs charge through the freewheeling diodes, increasing the total energy of the flexible dc-MMC. The energy in the voltage-controlled station of the SyM line has a small drop due to the discharge of the internal capacitors into the fault. The energy of the power-controlled station of the SyM line does not have energy variations due to its distance to the fault location. The energy in the bipole line increases as the power exported to the SyM line has stopped abruptly, i.e. there is an excess of dc energy that is absorbed by the MMCs with virtual capacitor control to keep the dc voltage stable. After the fault event, only the bipole line can recover steady-state conditions as the rest of the system is blocked.

The detailed converter results are presented in Fig. 6.28. The voltages at the terminals of the SM stack are presented in Fig. 6.28a, b, and c, for the upper, middle, and lower arm. After a short time after the fault (some hundreds of µs after the fault detection), the flexible dc-MMC is blocked and the ac voltage is stopped. The arms are subject to fast voltage transients that stabilizes depending on the external dc voltages. The upper arm voltage stabilizes to 525 kV equivalent to the positive pole of the bipole (V_{H1}). The middle arm voltage stabilizes to 400 kV

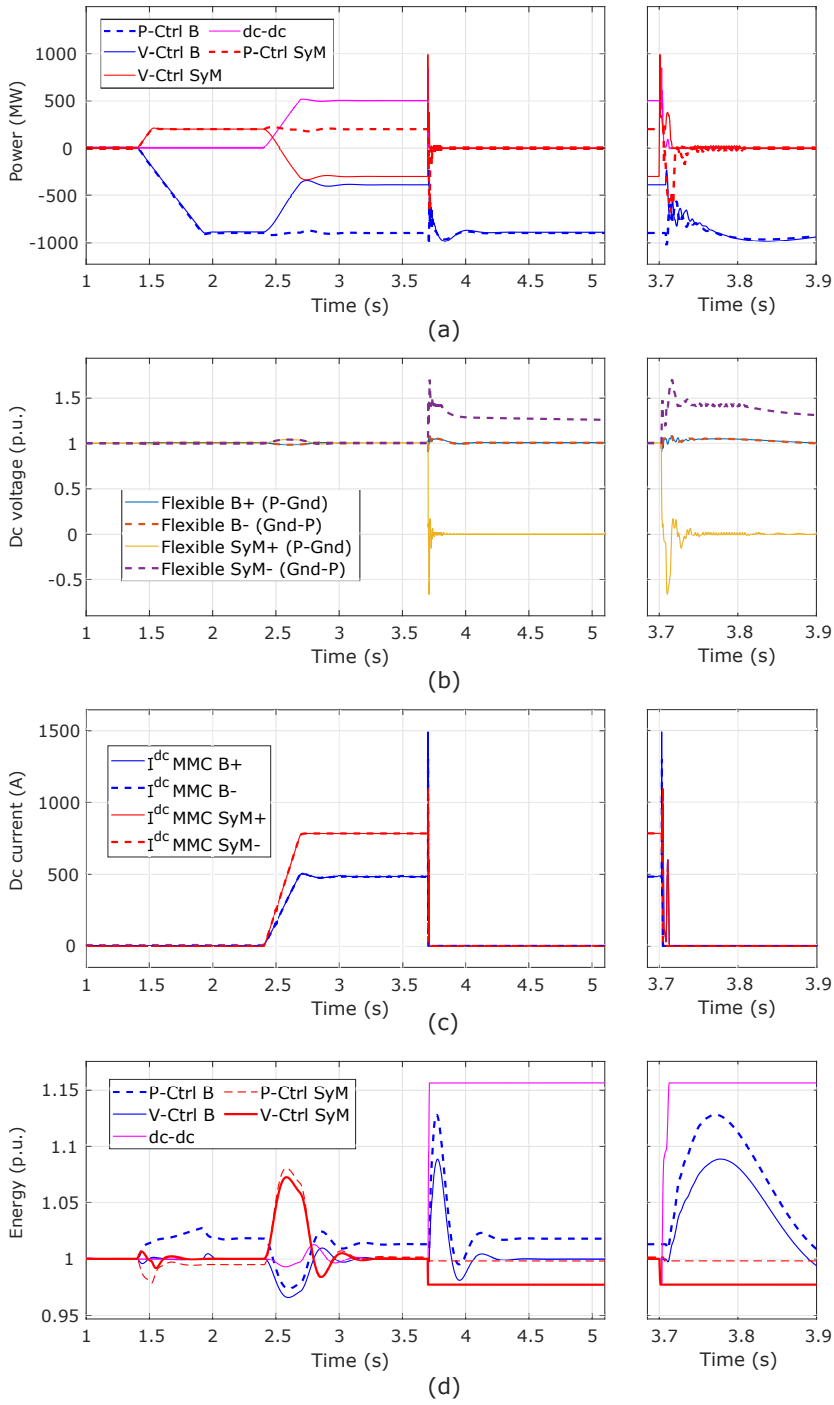


Figure 6.27: Simulation results for the flexible dc-MMC. The power flow of Case 5 (see Table 4.5) is simulated with a fault on the SyM line. (a) The power per converter station, (b) the dc voltages at the terminals of the dc-dc converter, (c) the dc currents measured at the terminals of the flexible dc-MMC, and (d)the energy per converter station.

that is the final pole-to-pole voltage on the SyM line, $V_{L1} + V_{L2}$, (see Fig. 6.27), equal to the negative pole, as $V_{L1} = 0$. The lower arm has a final voltage of 125 kV which is the difference between the negative pole of the bipole and the negative pole of the SyM ($V_{H1} - V_{L1}$). It can be noticed that the voltage transient of the faulted pole (yellow line in Fig. 6.27b) affects the transient seen by the arms in Fig. 6.28a, c.

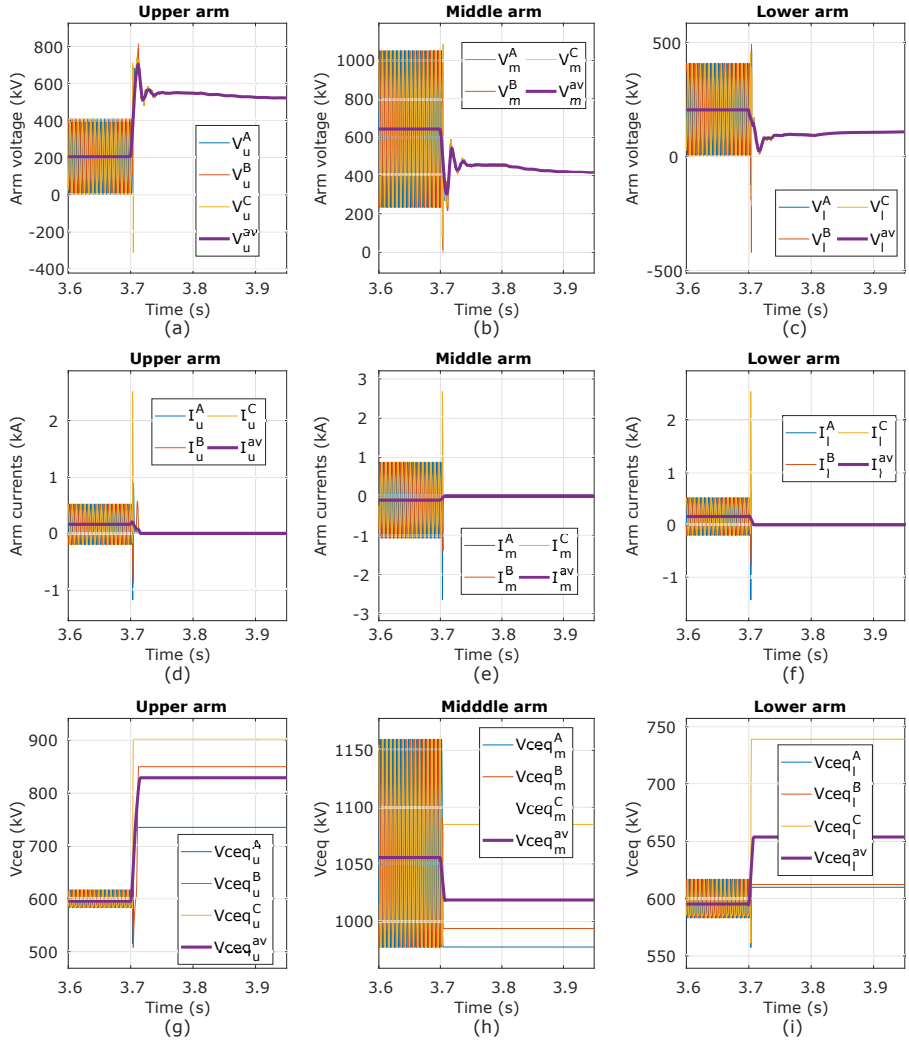


Figure 6.28: Arm voltage (first row), arm currents (second row), and voltage of C_{eq} (third row), for the upper, middle, and lower arm of the flexible dc-MMC, when the fault is located on the SyM side (Case 5 in Table 4.5).

The arm currents are presented in Fig. 6.28d, e, and f, for the upper, middle, and lower arms. At the time of the fault, the arms have an increased current transient that is stopped once the converter is blocked. The fault currents are blocked in a few ms (less than 8 ms) after the fault event. When the converter is blocked the currents in all arms drop to zero.

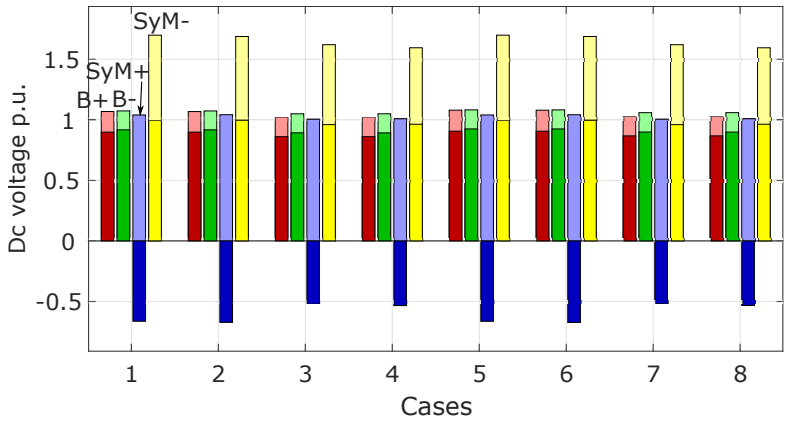


Figure 6.29: Maximum (light bars) and minimum (dark bars) pole-to-ground dc voltages registered in the flexible dc-MMC for the eight fault cases (see Table 4.5), when the fault is located on the SyM line. Red, green, blue, and yellow are the voltages of the positive pole of the bipole, negative pole of the B, the SyM positive pole, and SyM negative pole respectively.

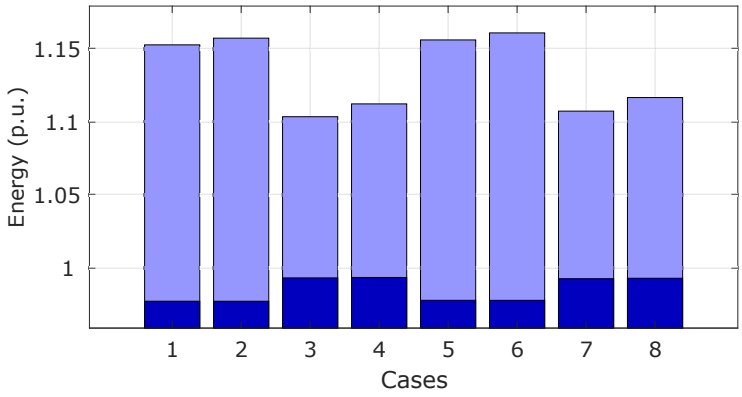


Figure 6.30: Maximum (light bars) and minimum (dark bars) total energy of the flexible dc-MMC for the eight cases in Table 4.5, when the fault is on the SyM line.

The voltages of the equivalent arm capacitor are presented in Fig. 6.28g, h, ans i, for the upper, middle, and lower arm. It can be noticed that the arms with FBSMs (upper and lower arms), have an overvoltage due to the charging of the FBSMs. For the upper arm, the overvoltage can reach 1.5 times the operational voltage. The overvoltage can be reduced if the SM capacitance value is increased. If the overvoltage reaches values that can damage the switches or capacitors in the SMs, bleed or rapid discharge resistors [143], can be considered. These overvoltages depend on the energy stored in the system inductors, e.g. arm, line inductances, during the fault event. Reducing the size of the output inductors, L_o, could be another strategy to reduce the FBSMs energy requirements.

The flexible dc-MMC has the capacity to stop the propagation of the fault currents, without triggering the blocking signal in the bipole line. The fault is seen by the bipole as a power disturbance that can be damped with the voltage-controlled station. The presented scenario, Case 5, is one of the cases with greater dynamic variations. The maximum and minimum voltage dynamic variations for the eight cases proposed in Table 4.5 are presented in Fig. 6.29. The dynamic variations registered for the energy of the flexible dc-MMC are presented in Fig. 6.30.

6.7 Conclusions

This chapter has presented the flexible dc-MMC, a non-isolated dc-dc converter capable of interconnecting different line topologies. The mathematical model is obtained following the hypotheses introduced in Chapter 3, from which the dc steady-state operation has been analyzed. The flexible dc-MMC has a cross interaction between the arms, which complicates the ac steady-state analysis. The dc and a preliminary ac steady-state analysis has been performed. However, the complete ac analysis have been obtained with an optimization problem.

The optimization problem is proposed to minimize the currents in the arms respecting the energy balance requirements. The optimization takes into account the number and type of used SMs, i.e. FBSMs or HBSMs. The optimization is performed for the nominal and degraded operation. For the case study proposed in this thesis, two degraded modes are evaluated: a fault on the positive pole of the B and a fault on the negative pole of the B.

The flexible dc-MMC pre-sizing is also presented. The arm inductors are estimated from the fault conditions as introduced in Chapter 3. The number of SMs and capacitance sizing follows the general methodology using the steady-state results from the aforementioned optimization problem.

A control strategy, following the methodology presented in Chapter 3, has been designed and implemented in Matlab Simulink. The control strategy uses the results from the optimization problem to set the angles of the ac currents. A simulation in nominal operation, i.e. exchanging the rated power in both directions, confirmed the appropriate behavior of the control strategy, which follows the steady-state solution found previously. Six normal conditions were tested and compared, presenting the results of the worse case. In general, the normal operation respects the steady-state operation limits of both lines confirming the adequate operation of the dc-dc converter.

Sixteen fault simulations (eight with a fault on the bipole and eight with a fault located on the SyM line), were conducted to confirm the firewall capability of the flexible dc-MMC and its degraded operation. The results suggest that the flexible dc-MMC can stop the fault propagation preserving the healthy zones operational. The FBSMs are considered to provide FBC. These SMs can prevent the propagation of the fault through the dc systems but, they need to absorb the energy stored during the fault, mainly in the system inductors. The energy absorbed by the FBSMs could lead to overvoltages. The capacitance values can be adapted depending on the system energy requirements, e.g. increasing the capacitance value to avoid overvoltages.

During the fault scenarios the arm currents do not exceed the maximum peak current allowed by the IGBTs (3.6 kA). However, further studies should be performed to determine the worst case scenario that defined the fault detection thresholds, e.g. di/dt or $I_{arm_{max}}$. Similar to the F2F-MMC, a thermal analysis must be performed to determine the need of bypass thyristors for the HBSMs. For the FBSMs, such bypass thyristor can be not implemented as these SMs are able to stop the fault currents. If the fault currents exceed the thermal limits of the diodes on the FBSMs, they can be replaced by thyristors, or an arrangement of diodes in parallel. Other solutions can be found in future, detailed studies.

The flexible dc-MMC can operate in degraded mode after a circuit reconfiguration. A set of disconnectors are needed to isolate the faulted pole. Then, the converter is restarted for the degraded operation. The

flexible dc-MMC does not allow immediate redundancy but, if fast disconnectors are implemented, the converter can reestablish degraded operation within some hundreds of ms.

Chapter 7

Asymmetric dc-dc converter

7.1 Introduction

The Asymmetric dc-dc converter (ADCC) is a non-isolated converter proposed in this thesis for HVDC heterogeneous interconnections. The ADCC is proposed within the goal to interconnect lines with different line topologies. The ADCC can be used to interconnect an AM and a SyM as presented in Fig. 7.1. However the interconnection between a B and a SyM is also possible using two ADCCs, see Fig. 7.2. The simulations and analysis are based on the B-SyM structure.

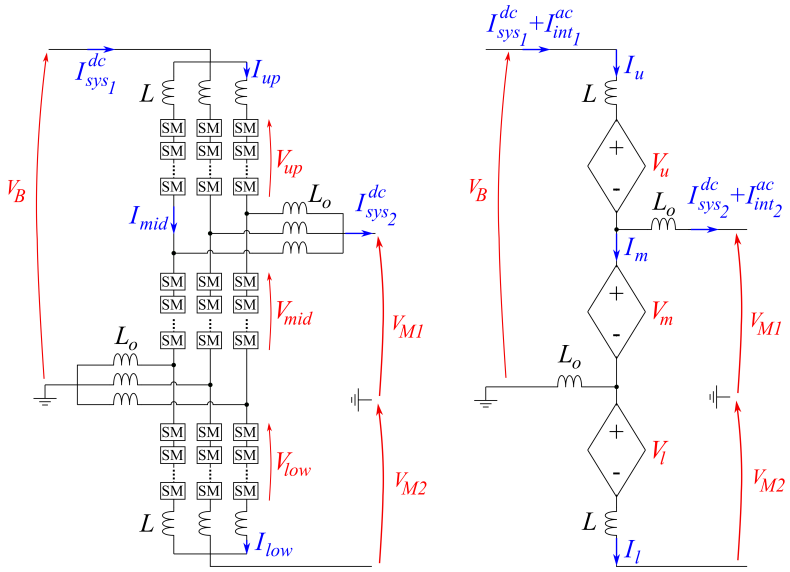


Figure 7.1: Asymmetric dc converter. (a) Three phase circuit. (b) Single phase circuit used for the mathematical model.

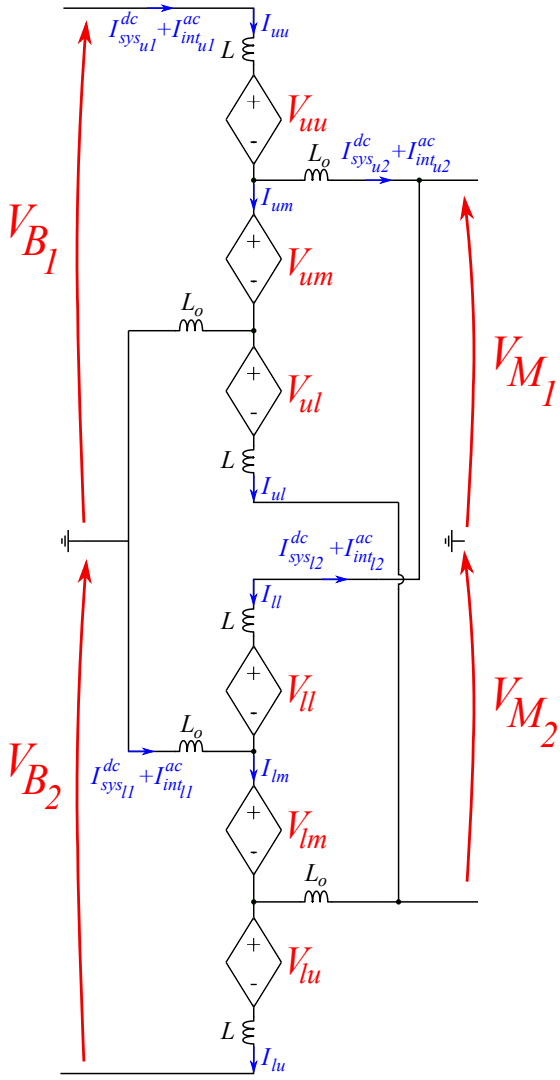


Figure 7.2: Asymmetric dc converter interconnecting a bipole (left side) and a SyM (right side). This is the configuration used to simulate and analyze the case study proposed in this thesis.

The ADCC is can reduce the weight compared to the F2F-MMC as it does not require ac transformer. Similar to the flexible dc-MMC, the ADCC can provide FBC using FBSMs. This could be advantageous compared to the F2F-MMC with ADCC as the FBSMs can block the fault current faster. Compared to the flexible dc-MMC, the ADCC can provide immediate redundancy for the interconnections B-SyM, as the poles on the bipole are decoupled with the separated ADCCs. In case of

a fault in one pole of the B, only the ADCC connected to the faulted pole is blocked, while the healthy pole continues to exchange power through the second ADCC. This configuration avoids the use of disconnectors considered for the flexible dc-MMC degraded operation.

The ADCC is composed of three arms: upper, middle, and lower. The upper and lower arms have an arm inductance while the middle arm does not. The ADCC has two sets of output inductors (L_o) needed to exchange power between legs and to avoid ac currents on the dc sides. Similar to the dc-MMC or the flexible dc-MMC, the ADCC has lower losses when the output inductors are greater that the arm inductors [80, 87].

Fig. 7.2 shows the single phase connection B-SyM. The ADCCs are connected in series on the bipole side, while on the SyM they are connected in parallel. The ADCC connected to V_{B_1} is equal to the one presented in Fig. 7.1b, whilst the ADCC connected to V_{B_2} needs to inverse the polarity of the SMs in the arms to withstand the reversed voltage. Assuming that the poles on the SyM are balanced, the converter connected to the negative pole follows the same sizing, control strategy, and references calculated for the positive ADCC. Therefore, only the positive ADCC is studied in the first sections. For the simulations models the complete solution, presented in Fig. 7.2 is used. Each converter is rated to half of the total transmitted power between the interconnected lines, i.e. for the case study proposed in this thesis, see Chapter 4, each ADCC is rated to 350 MW.

7.2 Mathematical modeling

To model the ADCC, the single phase circuit presented in Fig. 7.1b is used. As mentioned before, the analysis for the positive ADCC can be extended to the negative ADCC for the complete solution presented in Fig. 7.2. The model employs the equivalent arm voltage simplification (see section 3.2.1). The ADCC have three independent currents: I_u, I_m, and I_l. Three equations can be used to describe the converter as follows:

$$-V_B+V_u+L\frac{d}{dt}I_u+R\,I_u+L_o\frac{d}{dt}\left(I_u-I_m\right)+R_o\left(I_u-I_m\right)+V_{M1}=0 \quad (7.1)$$

$$-L_o\frac{d}{dt}\left(I_m-I_l\right)-R_o\left(I_m-I_l\right)+V_l+L\frac{d}{dt}I_l+R\,I_l-V_{M2}=0 \quad (7.2)$$

$$V_m + V_l + L\frac{d}{dt}I_l + R\,I_l - V_{M1} - V_{M2} - L_o\frac{d}{dt}\left(I_u - I_m\right) - R_o\left(I_u - I_m\right) = 0 \tag{7.3}$$

From the circuit equations, the matrix form is obtained:

$$\begin{bmatrix} L+L_o & -L_o & 0 \\ 0 & -L_o & L+L_o \\ -L_o & L_o & L \end{bmatrix} \begin{bmatrix} \dot{I}_u \\ \dot{I}_m \\ \dot{I}_l \end{bmatrix} = \begin{bmatrix} -(R+R_o) & R_o & 0 \\ 0 & R_o & -(R+R_o) \\ R_o & -R_o & -R \end{bmatrix} \begin{bmatrix} I_u \\ I_m \\ I_l \end{bmatrix} + \underbrace{\begin{bmatrix} -1 & 0 & 0 \\ 0 & 0 & -1 \\ 0 & -1 & -1 \end{bmatrix}}_{\boldsymbol{V_c}} \begin{bmatrix} V_u \\ V_m \\ V_l \end{bmatrix} + \underbrace{\begin{bmatrix} 1 & -1 & 0 \\ 0 & 0 & -1 \\ 0 & 1 & 1 \end{bmatrix}}_{\boldsymbol{K_V}} \underbrace{\begin{bmatrix} V_B \\ V_{M1} \\ V_{M2} \end{bmatrix}}_{\boldsymbol{V_K}} \tag{7.4}$$

where the state variables are the arm currents I_u, I_m, and I_l. The control variables are the arm voltages V_u, V_m, and V_l. Similar to the flexible dc-MMC presented in chapter 6, the system voltages are the dc voltages of the interconnected lines V_B, V_{M1}, and V_{M2}.

7.3 Steady-state analysis

The converter steady-state conditions can be analyzed using the mathematical model obtained in the previous section. This analysis is important to understand the basic requirements and operation of the converter.

7.3.1 Dc steady-state analysis

The dc operating conditions can be obtained following the methodology introduced in section 3.4.2. The arm dc currents can be expressed in terms of the system dc currents. The ADCC has two system dc currents: I_{sys_1} and I_{sys_2}, presented in Fig. 7.1. These currents correspond to the input and output dc currents as follows:

$$I_{sys_1} = \frac{P_T^{dc}}{V_B} \tag{7.5}$$

$$I_{sys_2} = \frac{P_T^{dc}}{V_{M1} + V_{M2}} \tag{7.6}$$

where P_T^{dc} is the dc transmitted power.

The arm dc currents can be expressed as:

$$I_u = \frac{I_{sys_1}}{N_{legs}} = \frac{1}{V_B}\frac{P_T^{dc}}{N_{legs}} \tag{7.7}$$

$$I_m = \frac{I_{sys_1} - I_{sys_2}}{N_{legs}} = \left(\frac{1}{V_B} - \frac{1}{V_{M1}+V_{M2}}\right)\frac{P_T^{dc}}{N_{legs}} \tag{7.8}$$

$$I_l = -\frac{I_{sys_2}}{N_{legs}} = -\frac{1}{V_{M1}+V_{M2}}\frac{P_T^{dc}}{N_{legs}} \tag{7.9}$$

where N_{legs} is the number of legs of the converter, in this case $N_{legs} = 3$.

The arm dc voltages can be found with the following expression (obtained in section 3.4.2):

$$\boldsymbol{V_{arm}^{dc}} = -\boldsymbol{V_c^{-1}}\,\boldsymbol{K_V}\,\boldsymbol{V_K^{dc}} \tag{7.10}$$

where $\boldsymbol{V_c}$ is the matrix linked to the arm voltages, $\boldsymbol{K_V}$ and $\boldsymbol{V_K^{dc}}$ are the matrix and vector related to the system dc voltages. As the ADCC does not have an external ac system, $\boldsymbol{V_K} = \boldsymbol{V_K^{dc}}$. Using the matrices from the mathematical model obtained in (7.4), the dc arm voltages correspond to:

$$\boldsymbol{V_{arm}^{dc}} = -\begin{bmatrix} -1 & 0 & 0 \\ 0 & 0 & -1 \\ 0 & -1 & -1 \end{bmatrix}^{-1} \begin{bmatrix} 1 & -1 & 0 \\ 0 & 0 & -1 \\ 0 & 1 & 1 \end{bmatrix} \begin{bmatrix} V_B \\ V_{M1} \\ V_{M2} \end{bmatrix}$$

$$\boldsymbol{V_{arm}^{dc}} = \begin{bmatrix} V_u^{dc} \\ V_m^{dc} \\ V_l^{dc} \end{bmatrix} = \begin{bmatrix} V_B - V_{M1} \\ V_{M1} \\ V_{M2} \end{bmatrix}. \tag{7.11}$$

Similar results can be found for the ADCC connected to the negative pole of the bipole:

$$\boldsymbol{V_{arm}^{dc}} = \begin{bmatrix} V_u^{dc} \\ V_m^{dc} \\ V_l^{dc} \end{bmatrix} = \begin{bmatrix} V_B - V_{M2} \\ V_{M2} \\ V_{M1} \end{bmatrix}. \tag{7.12}$$

7.3.2 Dc power balance

From the arm dc currents defined in (7.7)-(7.9), and the dc voltages defined in (7.11), the dc power per arm is obtained:

$$P_u^{dc} = \frac{V_B - V_{M1}}{V_B} \frac{P_T^{dc}}{N_{legs}} \tag{7.13}$$

$$P_m^{dc} = \left(\frac{V_{M1}}{V_B} - \frac{V_{M1}}{V_{M1} + V_{M2}} \right) \frac{P_T^{dc}}{N_{legs}} \tag{7.14}$$

$$P_l^{dc} = -\frac{V_{M2}}{V_{M1} + V_{M2}} \frac{P_T^{dc}}{N_{legs}}. \tag{7.15}$$

As discussed in Chapter 3, the power balance of the modular dc-dc converters can be achieved by an internal ac circulating power. The sum of the arm powers in a leg should be zero. For the ADCC, the power balance is:

$$P_u + P_m + Pl = \frac{V_B - V_{M1}}{V_B} + \frac{V_{M1}}{V_B} - \frac{V_{M1}}{V_{M1} + V_{M2}} - \frac{V_{M2}}{V_{M1} + V_{M2}} \tag{7.16}$$

Assuming the steady-state conditions: $V_{M1} = V_{M2}$, the power balance can be expressed as:

$$P_u + P_m + Pl = \frac{V_B}{V_B} - \frac{V_M}{2V_M} - \frac{V_M}{2V_M} = 0 \tag{7.17}$$

which confirms that the ADCC can balance its energy, without an external source, exchanging ac power between the arms in a leg.

7.3.3 Ac steady-state analysis

The total converter energy balance can be achieved by balancing the energy in the arms. Keeping constant the average value of the converter energy, is equivalent to balance the total power exchanged per arm, given by:

$$\left\langle P_{arm}^{dc} + P_{arm}^{ac} \right\rangle = 0 \tag{7.18}$$

Using the dc power per arm found in (7.13)-(7.15), the power balance per arm can be expressed as:

$$\frac{V_B - V_{M1}}{V_B} \frac{P_T^{dc}}{N_{legs}} = -V_u^{ac} I_u^{ac} \cos\left(\theta_{V_u} - \theta_{I_u}\right) \tag{7.19}$$

$$\left(\frac{V_{M1}}{V_B} - \frac{V_{M1}}{V_{M1}+V_{M2}}\right)\frac{P_T^{dc}}{N_{legs}} = -V_m^{ac}\, I_m^{ac} \cos\left(\theta_{V_m} - \theta_{I_m}\right) \tag{7.20}$$

$$-\frac{V_{M2}}{V_{M1}+V_{M2}}\frac{P_T^{dc}}{N_{legs}} = -V_l^{ac}\, I_l^{ac} \cos\left(\theta_{V_l} - \theta_{I_l}\right) \tag{7.21}$$

Replacing the system dc voltages by the values of the case study (see Chapter 4), i.e. $V_{M1} = V_{M2} = 320$ kV, and $V_B = 525$ kV, and assuming that the power is transferred from the V_B to the V_M side, the interactions between the arms and the dc-ac power are presented in Fig. 7.3.

The ac equivalent circuit, presented in Fig. 7.4, is almost identical to the ac circuit per phase of the flexible dc-MMC (see Fig. 6.4). The main difference is the grounding location. The flexible dc-MMC has a virtual reference at the n-phase connection point, while the ADCC has one node directly connected to the reference conductor on the bipole (or AM) side. The ac equivalent circuit of the ADCC presents the same connection between the arms, i.e. they are not in parallel nor in series.

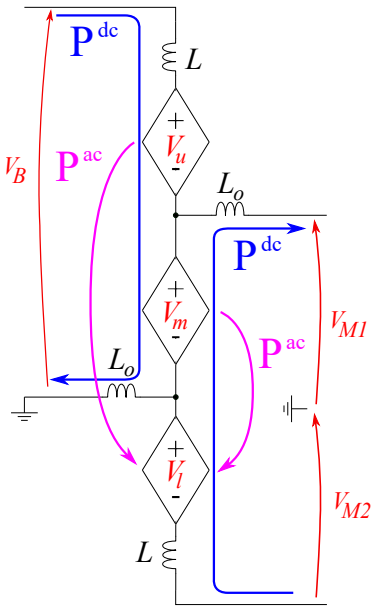


Figure 7.3: Internal power exchanges between the arms of the ADCC to keep the energy balanced.

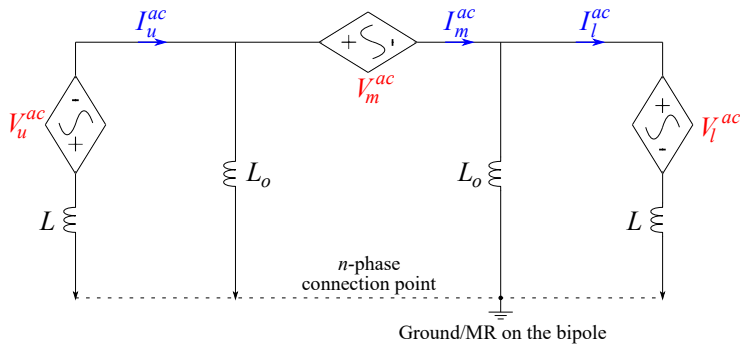


Figure 7.4: Equivalent ac circuit, per leg, of the ADCC. The dashed line indicates the theoretical reference, which is in fact a n-phase connection point.

Analogous to the procedure in Chapter 6, to find the ac steady-state solution, an optimization problem is proposed. A preliminary ac analysis can be done to find the limits of the arm ac voltages.

First ac voltage estimation from steady state dc voltages, FBC, and degraded operation requirements

The maximum amplitude of the arm ac voltages can be calculated from the dc steady-state, the FBC, and degraded operation requirements.

Using (7.11), and the dc voltages from the case study, the arm dc voltages are:

$$\boldsymbol{V}_{\boldsymbol{arm}}^{\boldsymbol{dc}} = \begin{bmatrix} V_u^{dc} \\ V_m^{dc} \\ V_l^{dc} \end{bmatrix} = \begin{bmatrix} V_B - V_{M1} \\ V_{M1} \\ V_{M2} \end{bmatrix} = \begin{bmatrix} 205\,\text{kV} \\ 320\,\text{kV} \\ 320\,\text{kV} \end{bmatrix}. \tag{7.22}$$

The dc voltages on the ADCC connected to the negative pole of the bipole are:

$$\boldsymbol{V}_{\boldsymbol{arm}}^{\boldsymbol{dc}} = \begin{bmatrix} V_u^{dc} \\ V_m^{dc} \\ V_l^{dc} \end{bmatrix} = \begin{bmatrix} V_B - V_{M2} \\ V_{M2} \\ V_{M1} \end{bmatrix} = \begin{bmatrix} 205\,\text{kV} \\ 320\,\text{kV} \\ 320\,\text{kV} \end{bmatrix}. \tag{7.23}$$

The first approach is to consider an ac modulation with the same amplitude than the dc voltage.

Concerning the requirements to have FBC, the different pole-to-ground faults should be considered. This can be done using (7.11) and changing the corresponding voltage pole-to-ground to zero. Table 7.1 summarizes the three scenarios for a pole-to-ground fault. The FBC requirements for the pole-to-ground faults cover the requirements for the pole-to-pole faults thus, no additional SMs should be considered. The cases that do not match with the initial estimation (7.22) are highlighted in red. From the results presented in Table 7.1, only the upper arm has additional conditions. The upper arm has an extended installed voltage including FBSMs to stop the fault on the bipole side. The middle and lower arms do not require additional SMs for the fault scenarios. The presented results are for the ADCC connected to the positive pole of the bipole but, similar results are found for the ADCC connected to the negative pole as $V_{M1} = V_{M2}$ is assumed.

Table 7.1: Voltage requirements per arm depending on the fault location for the ADCC.

Arm voltage	$V_B = 0$	$V_{M1} = 0$	$V_{M2} = 0$	$V_{M1} = V_{M2} = 0$
V_u	$-V_{M1}$	V_B	$V_B - V_{M1}$	V_B
V_m	V_{M1}	0	V_{M1}	0
V_l	V_{M2}	V_{M2}	0	0

As the ADCC proposed here is mainly for the interconnections between AM and a SyM, in case of a fault in any side, the converter is blocked, i.e. the individual ADCC does not have degraded mode. The voltage requirements found in Table 7.1 are the minimal required voltage per arm. Assuming additional SMs in the middle and lower arms to modulate the ac voltage (twice the dc steady-state voltage), the general voltage limits per arm are:

$$V_u \in \begin{bmatrix} -V_{M1} & V_B \end{bmatrix} \tag{7.24}$$

$$V_m \in \begin{bmatrix} 0 & 2\,V_{M1} \end{bmatrix} \tag{7.25}$$

$$V_l \in \begin{bmatrix} 0 & 2\,V_{M2} \end{bmatrix} \tag{7.26}$$

Replacing the system dc voltages considered for the case study the voltage limits per arm are:

$$V_u \in \begin{bmatrix} -320 & 525 \end{bmatrix} \text{ kV} \tag{7.27}$$

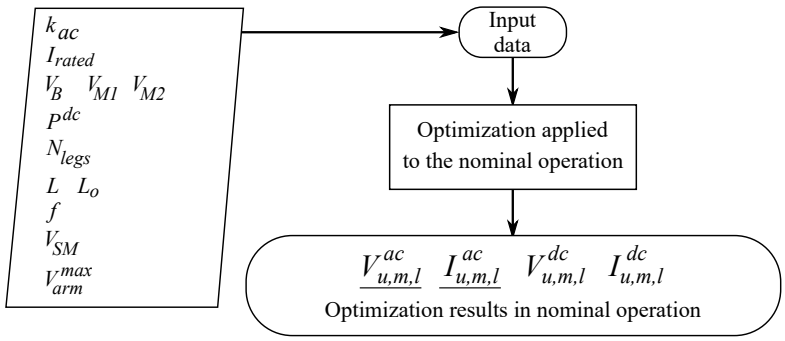


Figure 7.5: General flowchart representing the process used to calculate the steady-state solution of the ADCC.

$$V_m \wedge V_l \in \begin{bmatrix} 0 & 640 \end{bmatrix} \text{ kV} \tag{7.28}$$

These voltages are used as the limits for the optimization algorithm. The initial condition can be also determined within these limits.

7.3.4 Optimization problem

The optimization problem follows the same structure proposed for the flexible dc-MMC, see Section 6.3.4. However, the circuit equations and input data are adapted to the the ADCC. As previously stated, the ADCC does not have degraded mode thus, the optimization problem is solved only for the nominal steady-state operation. The general flowchart is presented in Fig. 7.5.

As the optimization requires the circuit inductances, they are sized in the next section.

7.4 Preliminary converter sizing

7.4.1 Circuit inductors

To size the circuit inductors of the ADCC, the critical fault current slope approach is used. This is one of the two approaches presented in Section 3.5.2. The second approach, i.e. using 15% of the base impedance cannot be applied to the ADCC as it does not have ac system to calculate the ac base impedance.

There are 4 possible dc faults in the ADCC, two pole-to-ground faults on the V_M side and two pole-to-pole faults (one on the V_M and one on the V_B side). The scenarios with the greater fault current slope are the

pole-to-pole faults. The equations describing the fault loops are:

$$-V_B + L\,\frac{d\,I_u}{dt} + V_u^{ss} + V_m^{ss} + L_o\,\frac{d}{dt}\,(I_m - I_l) = 0$$

$$-0 + L\,\frac{d\,I_u}{dt} + V_u^{ss} + V_m^{ss} + L_o\,\frac{d}{dt}\,(I_m - I_l) = 0 \tag{7.29}$$

$$-V_{M1} - V_{M2} - L_o\,\frac{d}{dt}\,(I_u - I_m) + V_m^{ss} + V_l^{ss} + L\,\frac{d\,I_l}{dt} = 0$$

$$-0 - 0 - L_o\,\frac{d}{dt}\,(I_u - I_m) + V_m^{ss} + V_l^{ss} + L\,\frac{d\,I_l}{dt} = 0 \tag{7.30}$$

where V_u^{ss}, V_u^{ss}, and V_u^{ss} are the steady-state arm voltages estimations.

Using (7.29), (7.30), and approximating the arm voltages in steady-state as the arm dc voltages found in (7.11), the simplified expressions to size the circuit inductors are:

$$(L + L_o)_{V_B\ side} = \frac{V_B}{(di/dt)_{crit}} \tag{7.31}$$

$$(L + L_o)_{V_M\ side} = \frac{V_{M1} + V_{M2}}{(di/dt)_{crit}} \tag{7.32}$$

Replacing the values considered for the case study yields to:

$$(L + L_o)_{V_B\ side} = \frac{525\,\mathrm{kV}}{6.4\,\mathrm{A/\mu s}} = 82\,\mathrm{mH} \tag{7.33}$$

$$(L + L_o)_{V_M\ side} = \frac{640\,\mathrm{kV}}{6.4\,\mathrm{A/\mu s}} = 100\,\mathrm{mH} \tag{7.34}$$

Similar to the dc-MMC [80] and the flexible dc-MMC (see Chapter 6), the ADCC reduces its conduction losses if the output inductors are greater than the arm inductors. In this case, an inductance of 200 mH for both sets of output inductors is considered. The chosen output inductor, L_o, respects both conditions (7.33) and (7.34), thus a small value of L can be used. In this thesis, a value of 15 mH is considered for the arm inductors in the ADCC.

Optimization results

The optimization problem is performed using the maximum ac voltage estimated in (7.27)-(7.28) and the circuit inductors calculated in previous section. The number of SMs, the arm voltage and currents are presented in Table 7.2 and Fig. 7.6. The arm voltages and currents are also used

in the control strategy to set the references (see Table 7.4). It is worth reminding that the analysis made for the positive ADCC can be extended for the negative ADCC.

Table 7.2: Number of SMs and ac steady-state solution for the nominal operation of the ADCC.

Arm	Number of HBSMs	Number of FBSMs	$\underline{V^{ac}}$ (kV)	$\underline{I^{ac}}$ (kA)
Upper	129	200	$186\angle -136.8°$	$0.56\angle 13.6°$
Middle	400	0	$294\angle 0°$	$0.87\angle 95.8°$
Lower	339	0	$203.34\angle 140.3°$	$0.72\angle 177.7°$

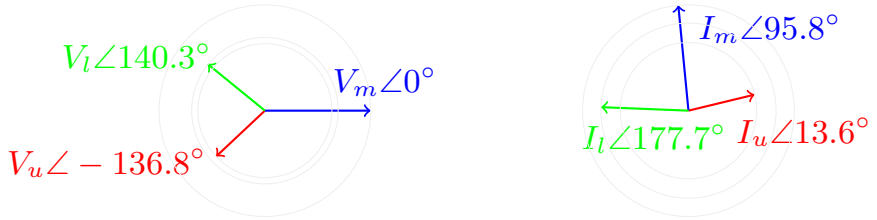


Figure 7.6: Graphical representation of the arm voltages and currents found with the optimization problem for the nominal operation of the ADCC.

7.4.2 Capacitor in the sub-modules

The equivalent capacitance can be calculated with (3.35), which requires the energy variation (3.37), calculated from the steady-state solution. The equivalent capacitances per arm are:

$$C_{eq_u} = 3.4\,\mu\text{F} \tag{7.35}$$

$$C_{eq_m} = 7.15\,\mu\text{F} \tag{7.36}$$

$$C_{eq_l} = 7.55\,\mu\text{F} \tag{7.37}$$

and the capacitance per SM are:

$$C_{SM_u} = C_{eq_u} N_{SM_u} = 3.4\,\mu\text{F} \cdot 329 = 1.1\,\text{mF} \tag{7.38}$$

$$C_{SM_m} = C_{eq_m} N_{SM_m} = 7.15\,\mu\text{F} \cdot 400 = 2.9\,\text{mF} \tag{7.39}$$

$$C_{SM_l} = C_{eq_l} N_{SM_l} = 7.55\,\mu\text{F} \cdot 339 = 2.6\,\text{mF} \tag{7.40}$$

7.5 Control design

Following the process introduced in section 3.6, the control strategy for the ADCC is detailed here.

7.5.1 System diagonalization

The methodology presented in Chapter 3 proposes the diagonalization of the mathematical model to simplify the control strategy used. Diagonalizing the state matrix of (7.4), i.e. $\boldsymbol{L}^{-1}R$, with the procedure explained in appendix A, the following model is found:

$$\begin{aligned}
\begin{bmatrix} \dot{I}_1 \\ \dot{I}_2 \\ \dot{I}_3 \end{bmatrix} &= \begin{bmatrix} -\frac{R_o+R}{L_o+L} & 0 & 0 \\ 0 & -\frac{R}{L} & 0 \\ 0 & 0 & -\frac{R_o}{L_o} \end{bmatrix} \begin{bmatrix} I_1 \\ I_2 \\ I_3 \end{bmatrix} \\
&+ \begin{bmatrix} -\frac{1}{2(L_o+L)} & 0 & \frac{1}{2(L_o+L)} \\ -\frac{1}{2L} & -\frac{1}{2L} & -\frac{1}{2L} \\ 0 & -\frac{1}{2L_o} & 0 \end{bmatrix} \begin{bmatrix} V_u \\ V_m \\ V_l \end{bmatrix} \\
&+ \begin{bmatrix} \frac{1}{2(L_o+L)} & -\frac{1}{2(L_o+L)} & -\frac{1}{2(L_o+L)} \\ \frac{1}{2L} & 0 & \frac{1}{2L} \\ 0 & \frac{1}{2L_o} & 0 \end{bmatrix} \begin{bmatrix} V_B \\ V_{M1} \\ V_{M2} \end{bmatrix}
\end{aligned} \tag{7.41}$$

where the arm current transformation matrix is:

$$\boldsymbol{P} = \begin{bmatrix} 1 & 1 & 0 \\ 0 & 1 & 1 \\ -1 & 1 & 0 \end{bmatrix} \qquad \boldsymbol{P}^{-1} = \begin{bmatrix} \frac{1}{2} & 0 & -\frac{1}{2} \\ \frac{1}{2} & 0 & \frac{1}{2} \\ -\frac{1}{2} & 1 & -\frac{1}{2} \end{bmatrix} \tag{7.42}$$

A transformation matrix, $\boldsymbol{T}$, can be found using (3.56), as follows:

$$\boldsymbol{T} = \begin{bmatrix} -\frac{1}{2(L_o+L)} & 0 & \frac{1}{2(L_o+L)} \\ -\frac{1}{2L} & -\frac{1}{2L} & -\frac{1}{2L} \\ 0 & -\frac{1}{2L_o} & 0 \end{bmatrix}^{-1} \begin{bmatrix} \frac{1}{L_o+L} & 0 & 0 \\ 0 & \frac{1}{L} & 0 \\ 0 & 0 & \frac{1}{L_o} \end{bmatrix}$$

$$\boldsymbol{T} = \begin{bmatrix} -1 & -1 & 1 \\ 0 & 0 & -2 \\ 1 & -1 & 1 \end{bmatrix} \qquad \boldsymbol{T}^{-1=} = \begin{bmatrix} -\frac{1}{2} & 0 & \frac{1}{2} \\ -\frac{1}{2} & -\frac{1}{2} & -\frac{1}{2} \\ 0 & -\frac{1}{2} & 0 \end{bmatrix} \tag{7.43}$$

The complete diagonal model corresponds to:

$$\begin{bmatrix}\dot{I}_1\\ \dot{I}_2\\ \dot{I}_3\end{bmatrix} = \begin{bmatrix}-\frac{R_o+R}{L_o+L} & 0 & 0\\ 0 & -\frac{R}{L} & 0\\ 0 & 0 & -\frac{R_o}{L_o}\end{bmatrix}\begin{bmatrix}I_1\\ I_2\\ I_3\end{bmatrix} + \begin{bmatrix}\frac{1}{L_o+L} & 0 & 0\\ 0 & \frac{1}{L} & 0\\ 0 & 0 & \frac{1}{L_o}\end{bmatrix}\begin{bmatrix}V_1\\ V_2\\ V_3\end{bmatrix} + \begin{bmatrix}\frac{1}{2(L_o+L)} & -\frac{1}{2(L_o+L)} & -\frac{1}{2(L_o+L)}\\ \frac{1}{2L} & 0 & \frac{1}{2L}\\ 0 & \frac{1}{2L_o} & 0\end{bmatrix}\begin{bmatrix}V_B\\ V_{M1}\\ V_{M2}\end{bmatrix} \tag{7.44}$$

The transformations between the 123 and the uml variables are presented below:

$$\boldsymbol{I_{123}} = \boldsymbol{P}^{-1}\,\boldsymbol{I_{uml}}$$

$$\begin{bmatrix}I_1\\ I_2\\ I_3\end{bmatrix} = \begin{bmatrix}\frac{I_u-I_l}{2}\\ \frac{I_u+I_l}{2}\\ \frac{-I_u+2I_m-I_l}{2}\end{bmatrix} \tag{7.45}$$

$$\boldsymbol{I_{uml}} = \boldsymbol{P}\,\boldsymbol{I_{123}}$$

$$\begin{bmatrix}I_u\\ I_m\\ I_l\end{bmatrix} = \begin{bmatrix}I_1+I_2\\ I_2+I_3\\ -I_1+I_2\end{bmatrix} \tag{7.46}$$

$$\boldsymbol{V_{123}} = \boldsymbol{T}^{-1}\,\boldsymbol{V_{uml}}$$

$$\begin{bmatrix}V_1\\ V_2\\ V_3\end{bmatrix} = \begin{bmatrix}\frac{-V_u+V_l}{2}\\ -\frac{V_u+V_m+V_l}{2}\\ -\frac{V_m}{2}\end{bmatrix} \tag{7.47}$$

$$\boldsymbol{V_{uml}} = \boldsymbol{T}\,\boldsymbol{V_{123}}$$

$$\begin{bmatrix}V_u\\ V_m\\ V_l\end{bmatrix} = \begin{bmatrix}-V_1-V_2+V_3\\ -2V_3\\ V_1-V_2+V_3\end{bmatrix} \tag{7.48}$$

These results are similar to those found for the flexible dc-MMC in Chapter 6. It can be noticed that the current and voltage transformations are equal, as well as the state, $\boldsymbol{A_D}$, and control, $\boldsymbol{B_D}$ matrices. But, the system voltages are not the same.

The new equivalent currents could have dc and ac components, but the ac components are controlled to circulate inside the converter without disturbing the dc sides.

The physical interpretations of the equivalent currents are presented in Fig. 7.7. The current I_1 is the current linking the upper and lower arm with the dc systems. It is the outer loop of the circuit (see Fig. 7.7a). The current I_2, presented in Fig. 7.7b, links the three arms of a converter leg with V_B and V_{M2}. Fig. 7.7c presents the equivalent I_3 current which only affects the middle arm. Only the dc components (continuous lines) are allowed to circulate into the dc systems. The ac components (dashed lines) are contained inside the converter circulating between the n phases of the circuit (with $n > 1$).

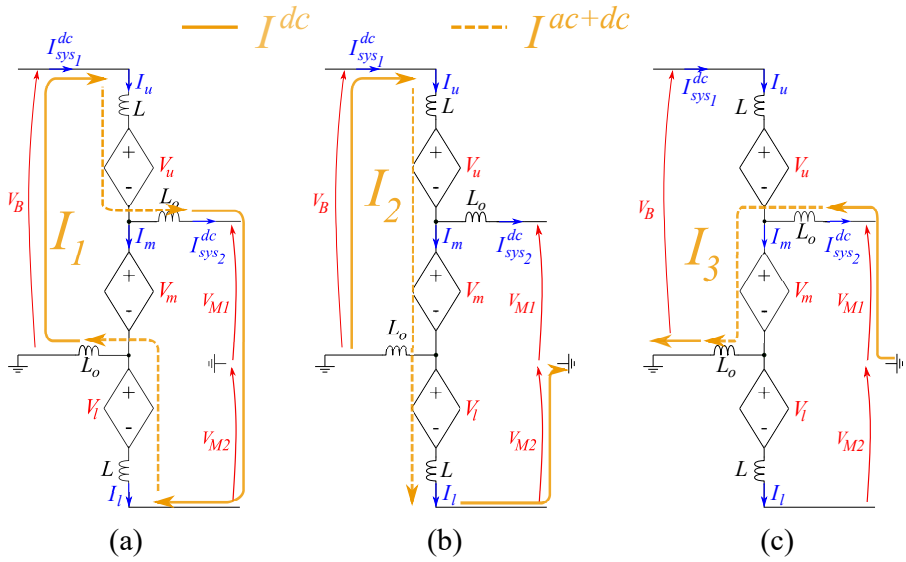


Figure 7.7: Physical interpretation of the equivalent currents. (a) I_1, (b) I_2, and (c) I_3.

7.5.2 Energy control

The energy in the converter should be controlled during the different transients in the system, e.g. voltage, power, current transients. The energy in the ADCC is controlled following the proposed strategy presented in Section 3.6.2. The energy is not controlled per arm but, with

a linear combination of the arm energies. The ADCC uses the following energy transformation, $\boldsymbol{W_T}$:

$$\boldsymbol{W_T} = \begin{bmatrix} 1 & 1 & 1 \\ 1 & -1 & 1 \\ 1 & 0 & -1 \end{bmatrix} \tag{7.49}$$

The new set of energies is:

$$\frac{d}{dt}\begin{bmatrix} E_\Sigma \\ E_{\Delta T} \\ E_{u-l} \end{bmatrix} = \boldsymbol{W_T}\begin{bmatrix} P_u \\ P_m \\ P_l \end{bmatrix} = \begin{bmatrix} P_u + P_m + P_l \\ P_u - P_m + P_l \\ P_u - P_l \end{bmatrix} \tag{7.50}$$

where E_Σ is the sum of all arm energies in a leg, $E_{\Delta T}$ is the energy difference between the three arms, and E_{u-l} is the energy difference between the upper and lower arms.

The power per arm can be expressed in terms of the new variables 123 by using (7.46) and (7.48) as follows:

$$P_u = -V_1 I_1 - V_1 I_2 - V_2 I_1 - V_2 I_2 + V_3 I_1 + V_3 I_2 \tag{7.51}$$

$$P_m = -2\left(V_3 I_2 + V_3 I_3\right) \tag{7.52}$$

$$P_u = -V_1 I_1 + V_1 I_2 + V_2 I_1 - V_2 I_2 - V_3 I_1 + V_3 I_2 \tag{7.53}$$

Replacing (7.51), (7.52), and (7.53) in (7.50), yields to:

$$\frac{d}{dt}E_\Sigma = -2\left(V_1 I_1 + V_2 I_2 + V_3 I_3\right) \tag{7.54}$$

$$\frac{d}{dt}E_{\Delta T} = 2\left(-V_1 I_1 - V_2 I_2 + 2V_3 I_2 + V_3 I_3\right) \tag{7.55}$$

$$\frac{d}{dt}E_{u-l} = 2\left(-V_1 I_2 - V_2 I_1 + V_3 I_1\right) \tag{7.56}$$

Total energy

The first equivalent energy is the sum of the three energies per arm, here called the total energy. The energy is controlled using the average power over time. The average total power, per leg, can be expressed as:

$$\begin{aligned}\left\langle \frac{d}{dt}E_{\Sigma} \right\rangle = &- 2\left(V_1^{dc}I_1^{dc} + V_2^{dc}I_2^{dc} + V_3^{dc}I_3^{dc}\right) \\ &- 2\frac{V_1^{ac}\,I_1^{ac}}{2}\cos\left(\theta_{V_1} - \theta_{I_1}\right) \\ &- 2\frac{V_2^{ac}\,I_2^{ac}}{2}\cos\left(\theta_{V_2} - \theta_{I_2}\right) \\ &- 2\frac{V_3^{ac}\,I_3^{ac}}{2}\cos\left(\theta_{V_3} - \theta_{I_3}\right).\end{aligned} \tag{7.57}$$

From the diagonal mathematical model defined in (7.44), and negecting the voltage drop in the resistances, it can be noticed that the currents I_i are in quadrature with the voltages V_i (for $i \in 1, 2, 3$), as an inductive circuit. Thus, the average value $\langle V_i^{ac} I_i^{ac} \rangle = 0$. The total energy can be simplified as follows:

$$\left\langle \frac{d}{dt}E_{\Sigma} \right\rangle = -2\left(V_1^{dc}I_1^{dc} + V_2^{dc}I_2^{dc} + V_3^{dc}I_3^{dc}\right) \tag{7.58}$$

From Fig. 7.7, the current I_2^{dc} is selected to control the total energy as it goes through the three arms in the converter leg. Using the dc steady-state currents (7.7)-(7.9), the dc steady-state voltages (7.11), the transformations (7.45) and (7.47), the reference for the current I_2^{dc} corresponds to:

$$I_2^{dc\,ref} = \frac{P_{E_\Sigma}^{ref} + \overbrace{\dfrac{V_{M2}^2 + V_{M1}V_{M2} + V_B V_{M1} - V_B^2}{V_B\left(V_{M1} + V_{M2}\right)}\dfrac{P_T^{dc}}{2\,N_{legs}}}^{P_{FF}^{dc}}}{V_B + V_{M2}} \tag{7.59}$$

where $P_{E_\Sigma}^{ref}$ is the output of the total energy controller, P_T^{dc} is the transmitted power, and N_{legs} is the number of converter legs.

The structure of the total energy controller is presented in Fig. 7.8, where P_{FF}^{dc} is the dc power feed forward in (7.59), and the reference for the energy is given by:

$$E_{\Sigma}^{ref} = \frac{1}{2}\left(C_{eq_u}V_{C_{equ}}^2 + C_{eq_m}V_{C_{eqm}}^2 + C_{eq_l}V_{C_{eql}}^2\right) \tag{7.60}$$

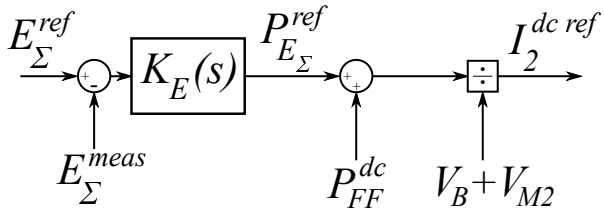


Figure 7.8: Total energy controller for the ADCC and the relation with the current reference.

Energy total difference

The second energy controller ($E_{\Delta T}$), here called total energy difference because it involves the three arms, compares the energy in the middle arm with the external arms, keeping their difference constant.

The average value of $\frac{d}{dt}E_{\Delta T}$ is:

$$\begin{aligned}\left\langle \frac{d}{dt}E_{\Delta T} \right\rangle =& 2\left(-V_1^{dc}I_1^{dc} - V_2^{dc}I_2^{dc} + 2V_3^{dc}I_2^{dc} + V_3^{dc}I_3^{dc}\right) \\ &+ 4\frac{V_3^{ac}\,I_2^{ac}}{2}\cos\left(\theta_{V_3} - \theta_{I_2}\right)\end{aligned} \tag{7.61}$$

In this case, as the equivalent power $E_{\Delta T}$ involves the three arms, the ac component of I_2 is selected to control it. Using the steady-state conditions, the relation between the energy total difference controller and the current reference I_2^{ac} is:

$$I_2^{ac\ ref} = \frac{P_{E_{\Delta T}}^{ref} + \overbrace{\frac{V_{M1}V_{M2} + V_M^2 - V_B V_{M1}}{V_B\left(V_{M1}+V_{M2}\right)}\frac{2P_T^{dc}}{N_{legs}}}^{P_{FF_{\Delta T}}^{dc}}}{\underbrace{2V_3^{ac}\cos\left(\theta_{V_3} - \theta_{I_2}\right)}_{V_{D_{\Delta T}}}} \tag{7.62}$$

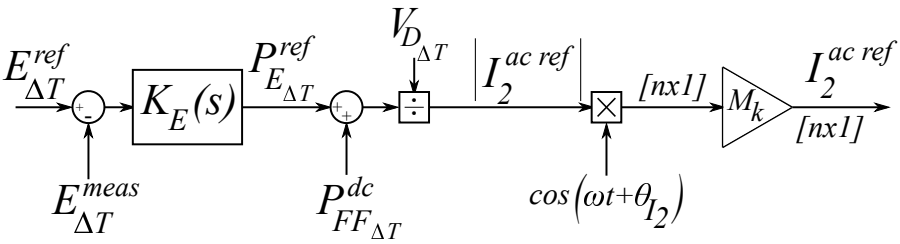


Figure 7.9: Total difference energy controller for the ADCC and the relation with the current reference.

The relation between the total difference energy controller and the current reference is presented in Fig. 7.9. The controllers are implemented for the n phases of the converter. The disturbance voltage $V_{D_{\Delta T}}$ (see section 3.6.2), corresponds to the denominator of (7.62) and it is calculated at the nominal operation, i.e. the control implemented has a fixed $V_{D_{\Delta T}}$, the dynamic variations caused by the operating conditions are corrected by the PI controller. The dc power feed-forward ($P_{FF_{\Delta T}}$) is calculated depending on the transmitted power P_T^{dc}. The $I_2^{ac\,ref}$ frequency (ω) and phase (θ_{I_2}) are set from the optimization results (see Section 7.4.1). The output of the n controllers are fed into the matrix $\boldsymbol{M_k}$, which is used to assure the balance between phases [136]. The energy reference $E_{\Delta T}^{ref}$ is:

$$E_{\Delta T}^{ref} = \frac{1}{2}\left(C_{eq_u} V_{C_{equ}}^2 - C_{eq_m} V_{C_{eqm}}^2 + C_{eq_l} V_{C_{eql}}^2\right) \tag{7.63}$$

Energy difference between the upper and lower arm

The third equivalent energy is the difference between the upper and lower arm. The average value of $\frac{d}{dt}E_{u-l}$ is:

$$\begin{aligned}\left\langle \frac{d}{dt}E_{u-l} \right\rangle =& 2\left(-V_1 I_2 - V_2 I_1 + V_3 I_1\ \right) - 2\frac{V_1^{ac} I_2^{ac}}{2}\cos\left(\theta_{V_1} - \theta_{I_2}\right) \\ & - 2\frac{V_2^{ac} I_1^{ac}}{2}\cos\left(\theta_{V_2} - \theta_{I_1}\right) + 2\frac{V_3^{ac} I_1^{ac}}{2}\cos\left(\theta_{V_3} - \theta_{I_1}\right)\end{aligned} \tag{7.64}$$

As this equivalent energy only involves the upper and lower arm, the ac component of I_1 (Fig. 7.7a) is used for this control. The magnitude of I_1^{ac} current reference, depending on the energy controller output can be expressed as:

$$I_1^{ac\,ref} = \frac{P_{E_{u-l}}^{ref} + P_{FF}^{dc} + P_{FF}^{ac}}{V_3^{ac}\cos\left(\theta_{V_3} - \theta_{I_1}\right) - V_2^{ac}\cos\left(\theta_{V_2} - \theta_{I_1}\right)} \tag{7.65}$$

were the power feed forwards are:

$$P_{FF}^{dc} = \frac{V_{M2}^2 + V_{M1}V_{M2} - V_B V_{M1} + V_B^2}{V_B\left(V_{M1} + V_{M2}\right)}\frac{P_T^{dc}}{N_{legs}} \tag{7.66}$$

$$P_{FF}^{ac} = V_1^{ac} I_2^{ac}\cos\left(\theta_{V_1} - \theta_{I_2}\right). \tag{7.67}$$

The relation between the current reference and the energy E_{u-l} controller is presented in Fig. 7.10. The energy reference E_{u-l}^{ref} is:

$$E_{u-l}^{ref} = \frac{1}{2}\left(C_{eq_u} V_{C_{equ}}^2 - C_{eq_l} V_{C_{eql}}^2\right). \tag{7.68}$$

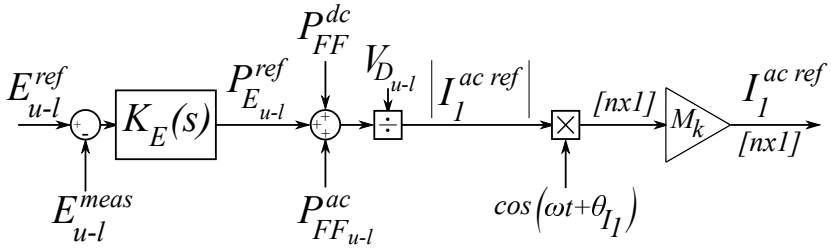


Figure 7.10: Difference (up-low) energy controller for the ADCC, and its relation with the current reference.

Similar to the energy total difference controller, the frequency and phase of $I_1^{ac\ ref}$ is set from the optimization results.

7.5.3 Current control

The current controllers are tuned with the diagonal system (7.44). Three current controllers are designed, one per equivalent current. The controllers considered are proportional-integral-resonant (PIR) controllers following the structure presented in Section 3.6.3. The current controllers and their relation with the equivalent voltages are presented in Fig. 7.11. The controllers are tuned with the parameters presented in Table 7.3.

Table 7.3: Parameters to tune the current controllers of the ADCC.

	L_{eq}	R_{eq}	V_{eq}	ϕ_{PM}	T_d
I_1	$L + L_o$	$R + R_o$	$V_1 + \frac{V_B - V_{M1} - V_{M2}}{2}$	60°	40 µs
I_2	L	R	$V_2 + \frac{V_B + V_{M2}}{2}$		
I_3	L_o	R_o	$V_3 + \frac{V_{M1}}{2}$		

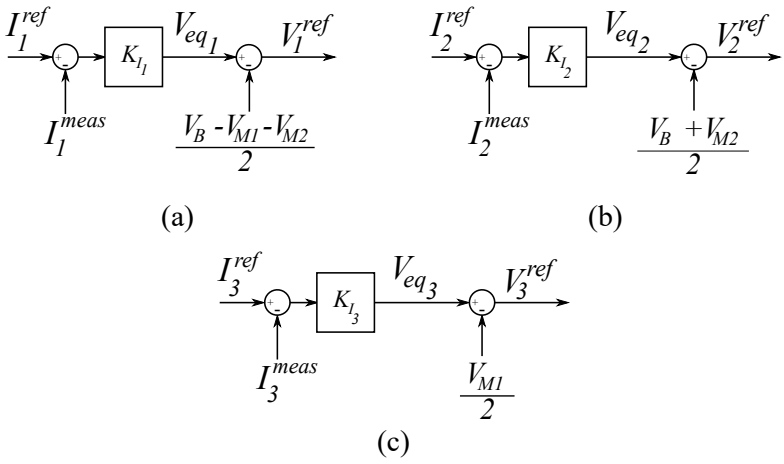


Figure 7.11: Current controllers for the equivalent currents of the ADCC. (a) I_1, (b) I_2, and (c) I_3.

The current I_2^{dc} could incur in an asymmetric disturbance on the negative pole of the monopole (V_{M2}). To avoid the unbalance, I_3^{dc} can be prepositioned to the dc value of I_2^{ref} reducing the control effort to keep the voltages balanced.

7.5.4 Power reference

Based on the physical interpretation of the equivalent currents (see Fig. 7.7), there is not a current that can be linked to the input, $I_{sys_1}^{dc}$, or output current, $I_{sys_2}^{dc}$. The power reference for the ADCC is set by the dc component of I_1:

$$I_1^{dc\,ref} = \left(\frac{1}{V_B} + \frac{1}{V_{M1} + V_{M2}}\right) \frac{P_T^{dc}}{2N_{legs}} \tag{7.69}$$

During the implementation of this power reference the dc voltages V_B, V_{M1}, and V_{M2} use a low-pass filter with $\tau = 10$ ms to avoid oscillations.

7.5.5 Pole balancing control

Similar to the flexible dc-MMC, the ADCC can be used to control the voltage unbalances on the SyM line. The ADCC uses the dc component of I_3^{dc} to control the current through the ground modifying the positive pole of the SyM (see Fig. 7.7). The controller is presented in Fig. 7.12.

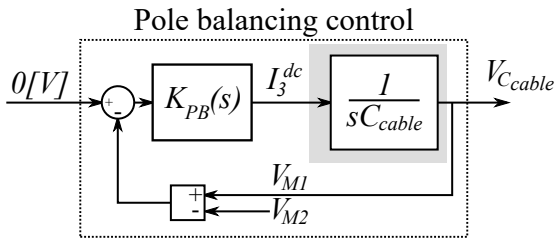


Figure 7.12: Close loop estimation for the pole balancing control tuning.

As the controller depends on the energy time constant and the equivalent capacitance on the cables, the same tuning strategy, presented in Section 6.5.5, can be applied to the ADCC. The controller gains are:

$$K_i \approx 1 \times 10^{-3} \ \mathrm{F\,s^{-2}} \tag{7.70}$$

$$K_p \approx 0.2 \times 10^{-3} \ \mathrm{F\,s^{-1}} \tag{7.71}$$

Control summary

The general control strategy implemented for the ADCC is presented in Fig. 7.13. The control strategy follows the same structure presented in Fig. 6.13 for the flexible dc-MMC with small changes on the current references I_3^{dc} and I_1^{dc} (highlighted in blue).

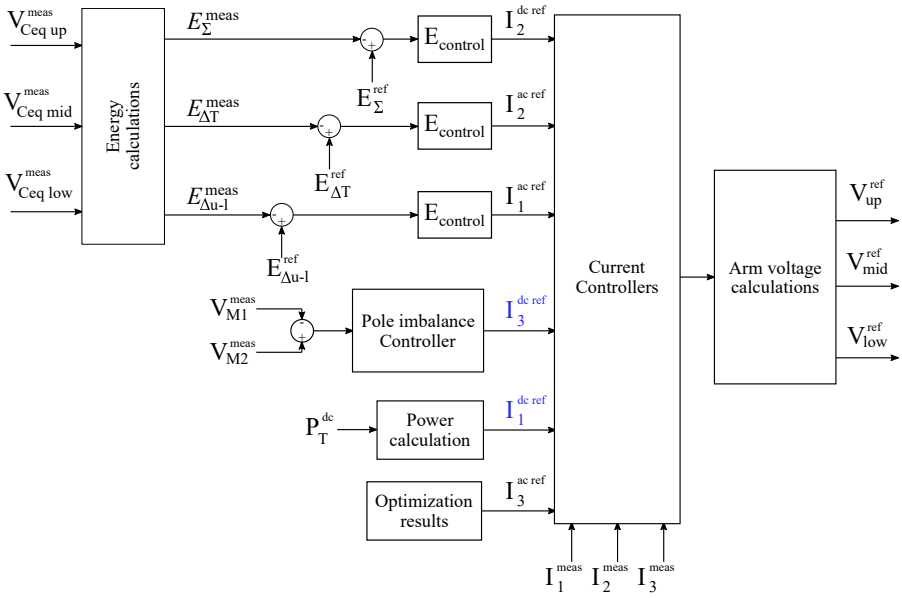


Figure 7.13: General control strategy implemented for the ADCC.

The summary of the different components of the equivalent currents and their use on the control strategy is presented in Table 7.4. The current I_3^{ac} is calculated in steady-state and is used as the reference for the rest of the variables.

Table 7.4: Different components of the equivalent currents I_{123}, and their use in the control strategy of the ADCC.

Current	Control use
I_1^{dc}	Transmitted power P_T^{dc}
I_1^{ac}	E_{u-l} control
I_2^{dc}	E_{Σ} control
I_2^{ac}	$E_{\Delta T}$ control
I_3^{dc}	Pole balancing on the SyM side
I_3^{ac}	Reference set from the steady-state solution

7.6 Case study simulations and results

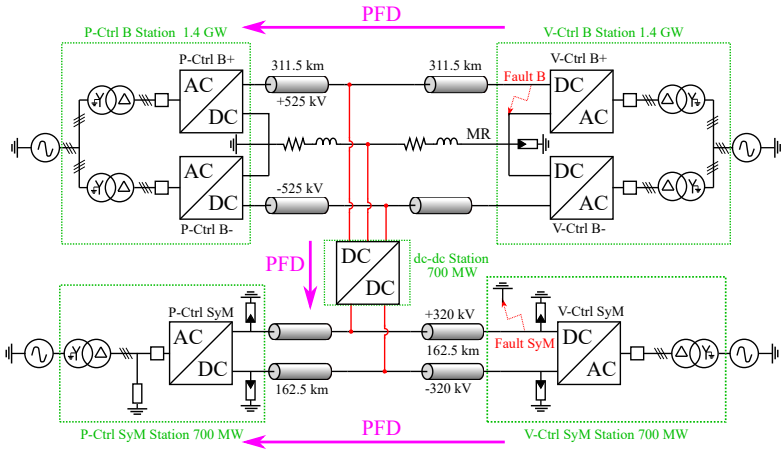


Figure 7.14: Case study system proposed for this thesis and the positive convention for the power flow directions (PFD), see Chapter 4.

Following the considered case study described in Chapter 4, a simulation model is implemented in Simulink Matlab. The general system structure is presented in Fig. 7.14 with the five converter stations and the consid-

ered positive conventions for the power flow directions. The considered dc-dc converter is composed of two ADCCs, one per pole, as presented in Fig. 7.2.

To test the control strategy proposed in this chapter, three groups of simulations are performed. A first simulation to test the nominal operation, a group of six simulations to test the normal operation changing the power flow direction (see Table 4.4), and 16 simulations testing the behavior during and after faults (see Table 4.5).

7.6.1 Normal operation

The normal operation is tested with a set of simulations exchanging 500 MW between the interconnected lines. Six simulations are performed changing the power flow directions as indicated in Table 4.4. From the simulated scenarios, Case 3 presents the worse results. They are presented in this section.

The system results are presented in Fig. 7.15. The power per converter station is presented in Fig. 7.15a. The simulation starts with the power flow on the lines, where the B has a power reference of 900 MW and the SyM 200 MW. Once the lines have reached steady-state conditions, the ADCC is set to exchange 500 MW between the lines. The voltage-controlled stations change their power depending on the power through the dc-dc converter. By contrast, the power-controlled stations (dashed lines) keep their power constant.

The dc voltages at the terminals of the ADCCs are presented in Fig. 7.15b. During the changes in the power references, the dc voltage is subject to dynamic variations that do not exceed the normal operation conditions, i.e. $\pm 5\%$ of their nominal value.

The energy per converter station is presented in Fig. 7.15c. It can be seen that the energies in the MMCs stations change with the power reference variations. These changes are linked to the dynamic variations in the dc voltages. As the ac-dc converters implement a virtual capacitor controller (see Chapter 4), the energy in the ac-dc stations depends on the dc voltage at their terminals. This can be evidenced with the power-controlled stations that have a lower steady-state energy value compared with the voltage-controlled stations.

The arm voltages are presented in Fig. 7.16. It can be noticed that the dc offsets change during the power transients. The arm voltages are controlled during the complete simulation.

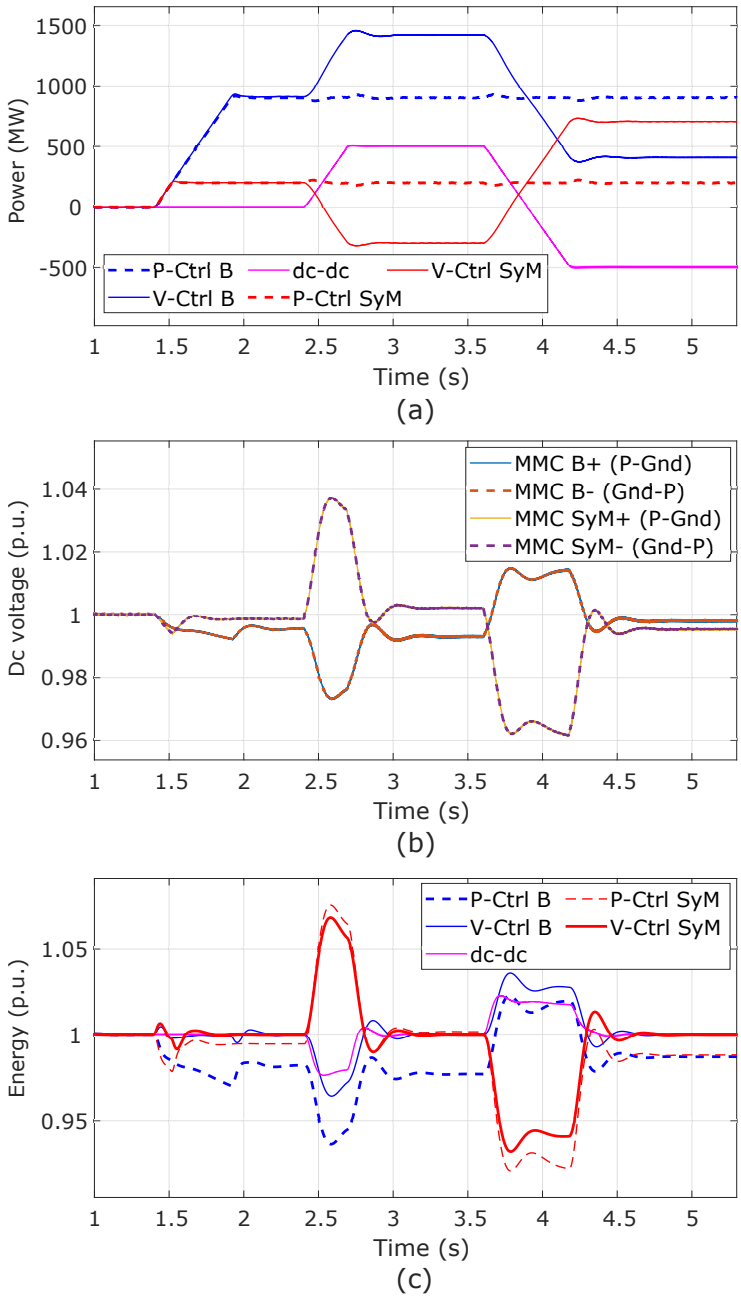


Figure 7.15: Results for the normal operation of the ADCC (Case 3 of Table 4.4). (a) The power per converter station. (b) The dc voltages at the terminals of the dc-dc converter in p.u. (c) The energy per converter station in p.u.

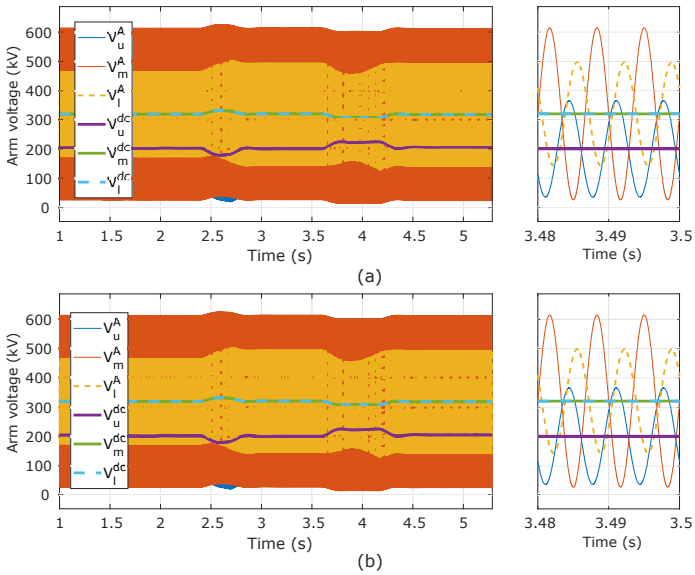


Figure 7.16: Arm voltages. (a) ADCC connected to the positive pole of the bipole, and (b) ADCC connected to the negative pole of the bipole (b).

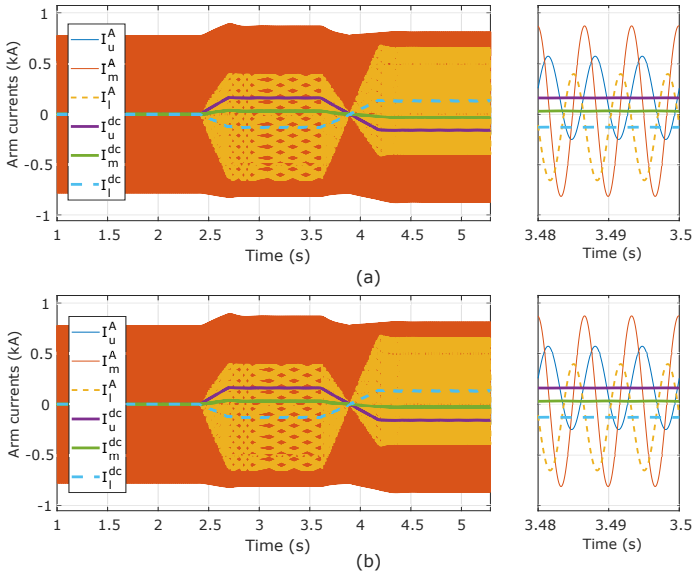


Figure 7.17: Arm currents in normal operation. (a) ADCC connected to the positive pole of the bipole, and (b) ADCC connected to the negative pole of the bipole (b).

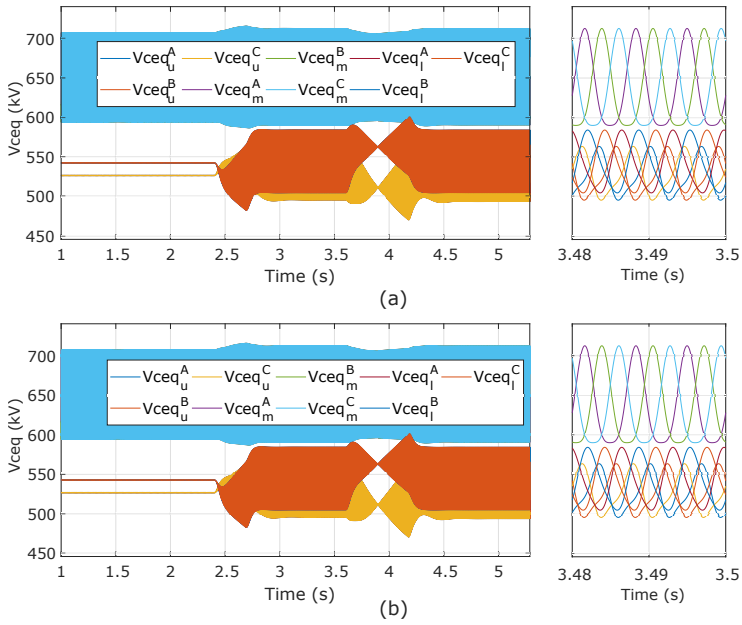


Figure 7.18: Voltage of the equivalent capacitance per arm in normal operation. (a) ADCC connected to the positive pole of the bipole, and (b) ADCC connected to the negative pole of the bipole.

The arm currents are presented in Fig. 7.17. The arm current on the upper and lower arm change their amplitude and phase depending on the transmitted power. Around 3.9 s, the currents change of phase to follow the change of power flow direction set by the power reference. The middle arm does not have the change in phase as its ac component is linked to I_3^{ac}, which is fixed from the steady-state solution. However, the calculation of I_3^{ac} can be made depending on the transmitted power, which can improve the converter performance. The arm currents determine the voltage ripple in the arm equivalent capacitors (see Fig. 7.18). Thus, the arm equivalent capacitors in the upper and lower arm change their ripple depending on the transmitted power.

The maximum and minimum dc voltage dynamic variations measured at the terminals of the ADCCs, for the six cases of normal operation, are presented in Fig. 7.19. During the six cases of normal operation, the dc voltages in the lines do not exceed the normal operation limits, i.e. $\pm 5\%$ of their nominal values.

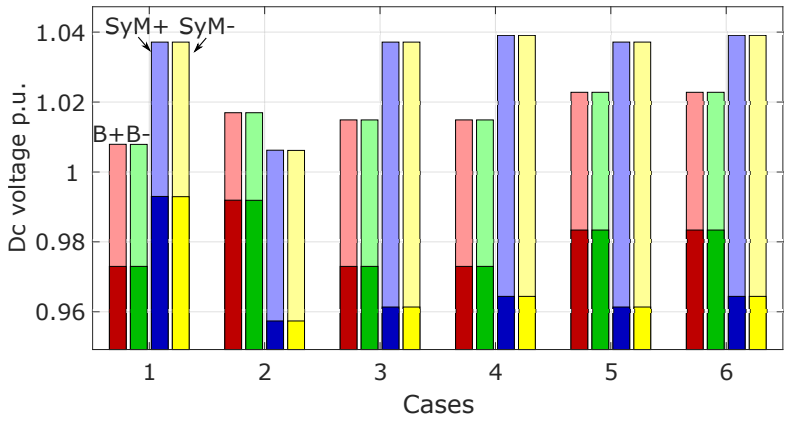


Figure 7.19: Maximum (light bars) and minimum (dark bars) pole-to-ground dc voltage registered in the ADCC for the six cases of normal operation (see Table 4.4). The red, green, blue, and yellow bars are the voltages of the positive pole of the bipole, negative pole of the B, the SyM positive pole, and SyM negative pole respectively.

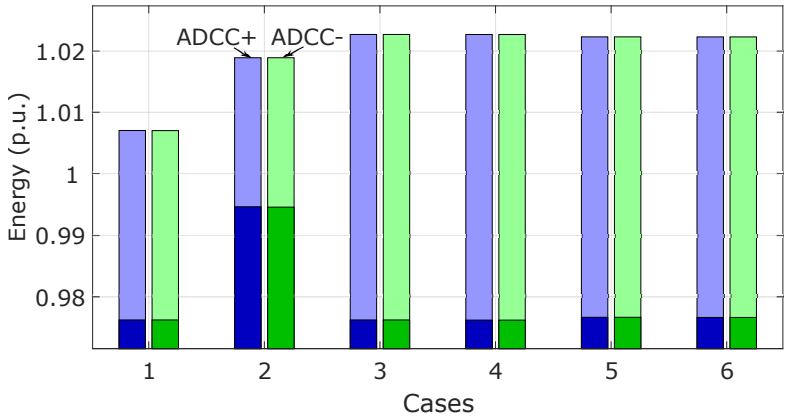


Figure 7.20: Maximum (light bars) and minimum (dark bars) energy per ADCCs interconnecting the B with the SyM line for the six cases presented in Table 4.4. The blue bars represent the energy in the ADCC connected to the negative pole of the B while the green bars are the energy in the ADCC connected to the negative pole of the B.

The energy dynamic variations are presented in Fig. 7.20 for the six cases proposed in Table 4.4. The energy vary between ±3% which do not represent any inconvenience for the elements in the dc-dc converter.

7.6.2 Fault scenarios

During the initial simulations of the faults located on the bipole, the ADCC was unable to provide FBC because the fault event was propagated to the healthy zones provoking the block of the ADCC connected to the negative pole of the bipole and the SyM line. The fault on the bipole creates a current through the converter that charges one of the poles on the SyM line. When the fault is on the positive pole of the B, the fault current charges V_{M2}, see Fig. 7.21a. When the fault is on the negative pole of the B, the fault current charges V_{M1} as presented in Fig. 7.21b. The fault current charges the pole on the SyM faster than the control time constants, blocking the line and the adjacent ADCC.

To prevent the propagation of the fault, the fault simulations performed with the ADCC have a different fault detection criteria from the conditions used for the F2F in Chapter 5, or the flexible dc-MMC in Chapter 6, see Section 4.3.6. The ADCC implements a low voltage detection, which triggers the converter blocking signal if the dc voltage pole-to-ground drops below 0.6 p.u. The new blocking criteria for the ADCC is presented in Fig. 7.22.

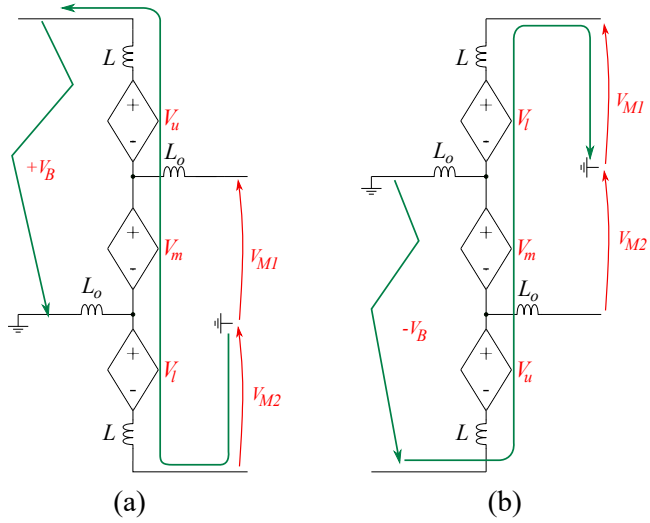


Figure 7.21: Fault currents charging (a) the negative pole of the SyM (V_{M2}) after a fault on the positive pole of the B, and (b) the positive pole of the SyM (V_{M1}) after a fault on the negative pole of the B. The paths are forced by the condition where $L_o > L$.

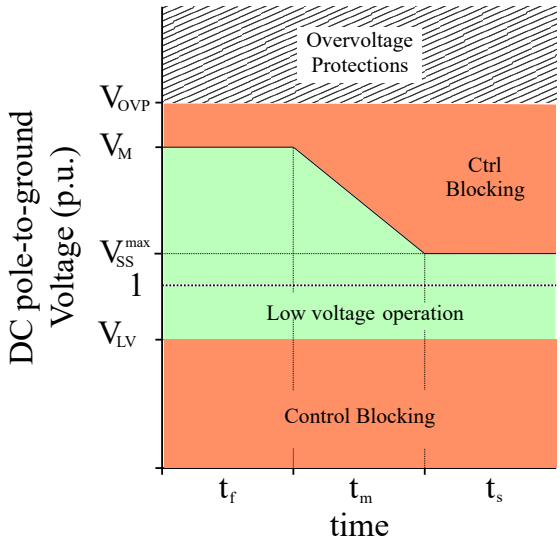


Figure 7.22: Operating zones of the ADCC (see Section 4.3.6). The converter is blocked if a pole-to-ground voltage drops below $V_{LV} = 0.6$ p.u.

The new fault detection criteria reduces the operating zone (green area in Fig. 7.22) but, it does not affect the results for the case study. The low voltage threshold in the ADCC is 15% below the ac-dc converters threshold, see Section 4.3.6, i.e. the ac-dc converters will block before the ADCC. As the B line is inoperative, keeping the ADCC operational does not provide additional benefits.

Based on the power flow directions presented in Table 4.5, eight simulations are performed for a fault on the bipole line, and eight simulations considering a fault on the SyM line (see fault locations in Fig. 7.14). The results are presented in the following sections.

Fault on the bipole line

When the fault is on the positive pole of the bipole line, the dc-dc converter should keep the healthy zones operational, i.e. the blocking signals should not be triggered in the negative pole of the bipole, the SyM, or the second ADCC. As the dc-dc converter uses one ADCC per pole, immediate redundancy can be achieved, i.e. at the time of the fault, the power from the healthy pole of the bipole is not stopped.

The system is simulated in normal conditions following the eight scenarios proposed in Table 4.5. The Case 8 is one of the scenarios with greater dynamic variations. The system results for the Case 8 are pre-

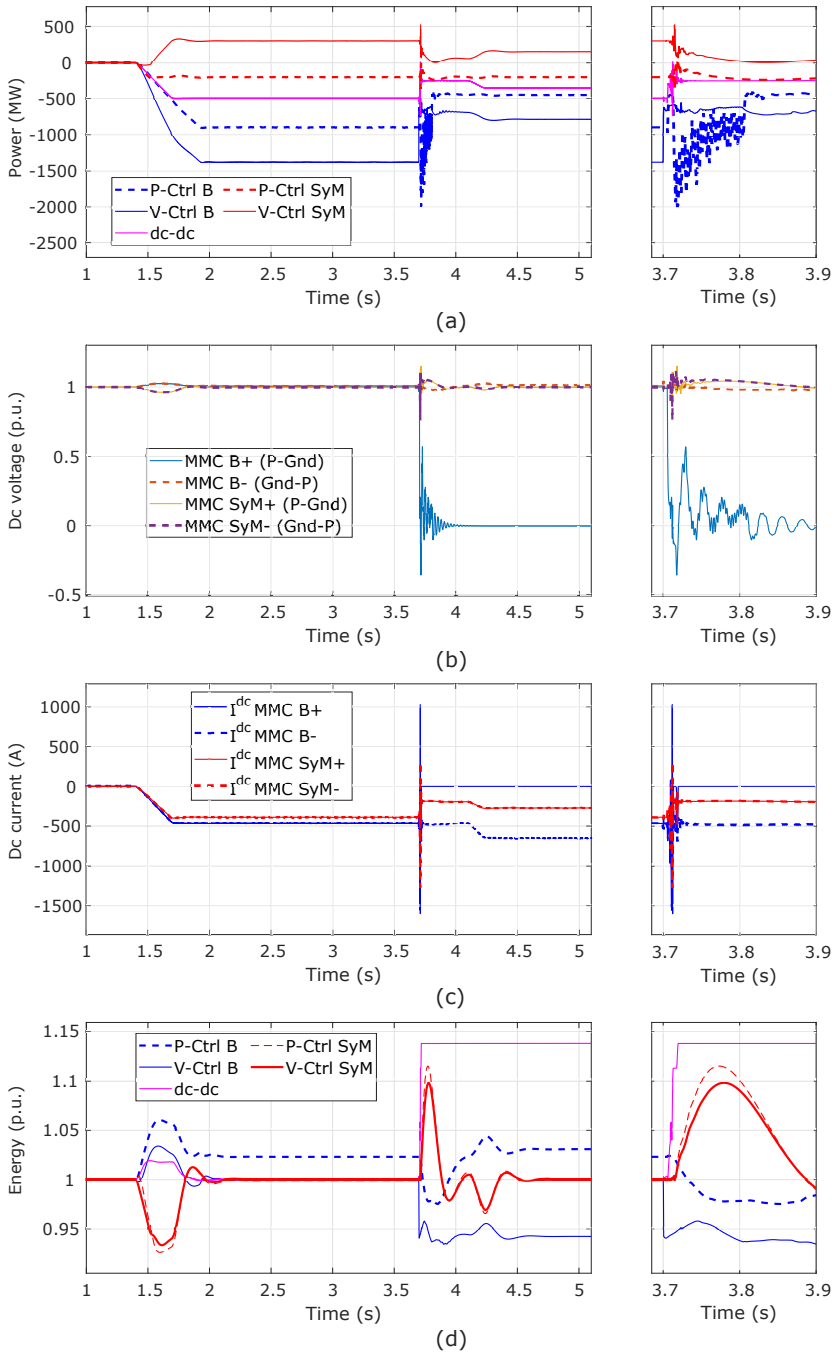


Figure 7.23: Results for a fault on the bipole side (Case 8). (a) The power per converter station. (b) The dc voltages at the terminals of the ADCCs in p.u. (c) Dc currents measured at the terminals of the ADCCs. (d) The energy per converter station.

sented in Fig. 7.23. The power per converter station is presented in Fig. 7.23a. As presented in Table 4.5, the power flow references at the time of the fault are -900 MW for the B line, -200 MW for the SyM line, and -500 MW for the ADCCs (-250 MW per converter). These references are followed by the power-controlled stations (dashed lines). The voltage-controlled stations (continuous lines) change their power to keep the voltage stable. At the instant of the fault, there is a power disturbance in both lines but, it does not trigger the fault detection on the healthy zones. The power through the dc-dc converter drops to half of the power transmitted before the fault, i.e. 250 MW. The power reference in the ADCC is increased to 350 MW, 400 ms after the fault event to exchange the rated power of the ADCC.

The dc voltages measured at the terminals of the ADCCs are presented in Fig. 7.23b. The dc voltages are disturbed with every power change. The dc voltage on the SyM is disturbed during the fault event. However, the voltage is controlled to regain steady-state conditions without triggering the blocking signals in the healthy zones. The negative pole of the B is also disturbed but it remains stable during the fault clearance.

The dc currents measured at the terminals of the ADCCs are presented in Fig. 7.23c. At the time of the fault, the overcurrents can reach 1.5 kA then, they are stopped rapidly thanks to the blocking of the ADCC connected to the faulted pole. The fault current is stopped after 20 ms. After the fault isolation, the currents on the healthy pole of the bipole (dashed blue line) and the currents on the SyM line (red lines) continue uninterruptedly. Around 4.2 s the power through the dc-dc converter is adjusted to exchange the nominal power of the healthy pole on the B line.

The energy per converter station is presented in Fig. 7.23d. It can be noticed that the power-controlled station in the bipole line has a different total energy value, this is because of the virtual capacitor controller implemented in the ac-dc converters (see Section 4.3.1). At the instant of the fault, the dc-dc converter station has an increased energy due to the fault currents charging the FBSMs. The SyM line has an increased energy value during the fault because half of the power exported to the bipole line has stopped, i.e. the line has an excess of energy. The energy is stored in the ac-dc converters while the dc voltage regain steady-state conditions. During the fault, the energy in the ac-dc converters on the bipole line discharges into the fault. After the fault, the MMC connected to the faulted pole is blocked and cannot recover nominal steady-state conditions. The energy in the bipole converter remains lower than its nominal value due to the discharged MMCs connected to the faulted

pole. Similar to the energy measured in the bipole line, the energy in the dc-dc converter station remains above its nominal value due to the charged FBSMs in the ADCC connected to the faulted pole.

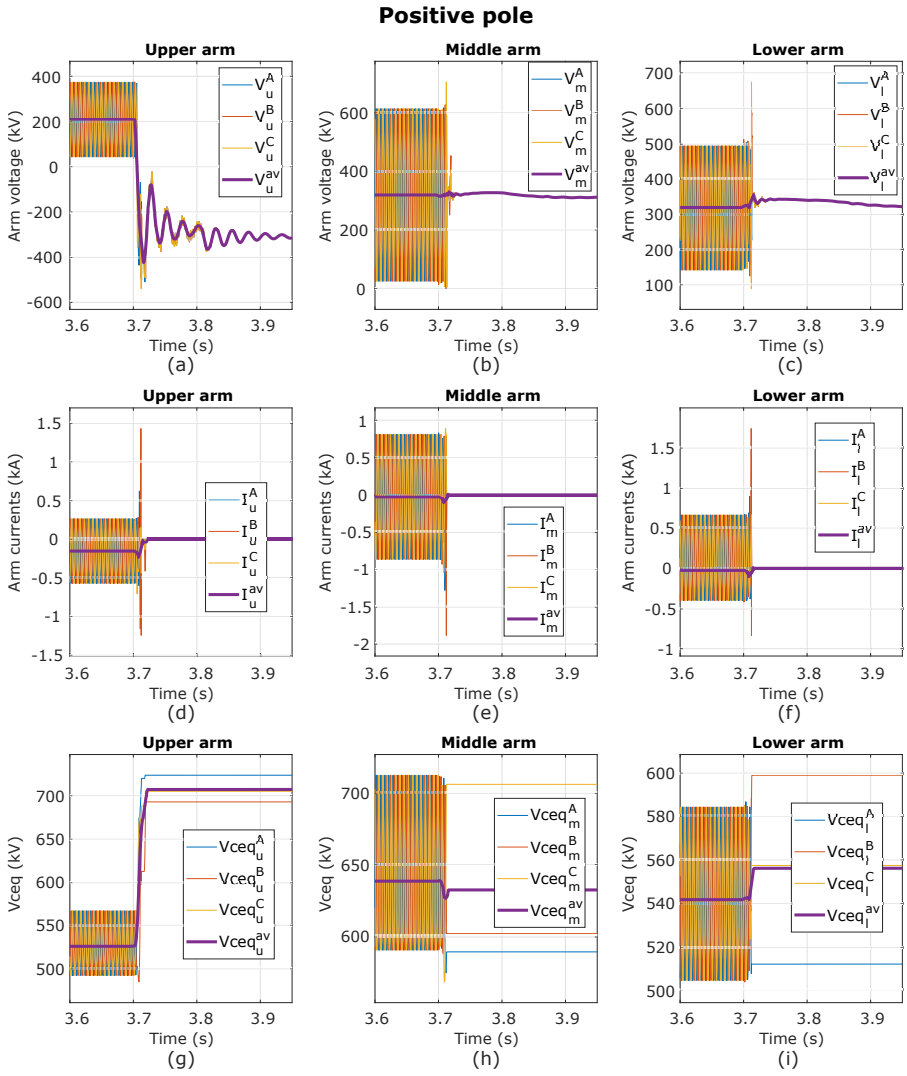


Figure 7.24: Results for the ADCC connected to the positive pole when a fault on the bipole side is simulated (Case 8). The first row presents the arm voltages, the arm currents are presented in the second row, and the voltage in the equivalent arm capacitances in the third row, for the upper, middle, and lower arms.

The detailed results of the ADCC, connected to the positive pole of the bipole (ADCC+), are presented in Fig. 7.24. The voltage at the terminals of the stack of SMs are presented in Fig. 7.24a, b, and c, for the upper, middle, and lower arm. At 3.7 s, the fault event is detected and the converter is blocked in a few ms. When the ADCC+ is blocked, the ac modulation stops and the arm withstands the system dc voltages. The arm dc voltage can be estimated with (7.22). The upper arm is subject to a big disturbance as it is connected to the faulted pole. The voltage after the fault, in the upper arm, stabilizes to $-V_{M1} \approx -320$ kV. The middle arm stabilizes to V_{M1} and the lower arm to V_{M2}, both approximately 320 kV.

The arm currents of the ADCC connected to the positive pole of the bipole are presented in Fig. 7.24d, e, and f, for the upper, middle, and lower arm. It can be evidenced that the arm currents in the ADCC do not exceed the limit estimated for the considered IGBTs (3.6 kA). The arm currents are stopped after a few milliseconds after the fault event.

The voltages of the arm equivalent capacitances are presented in Fig. 7.24g, h, and i, for the upper, middle, and lower arm. It can be noticed that the energy in the upper arm, containing FBSMs, rises after blocking the converter as the FBSMs charge with the fault currents (independently of its sign). Once the fault currents are stopped, the FBSMs stop charging. The lower arm is also charged but, to a lower voltage. The overvoltage in the upper arm can rise up to 1.4 the nominal voltage. To reduce the overvoltage the capacitance value can be increased or rapid discharge resistors [143] can be considered.

The detailed results, for the ADCC connected to the negative pole (ADCC-), are presented in Fig. 7.25. The voltages at the terminals of the stack of SMs are presented in Fig. 7.25a, b, and c for the upper, middle, and lower arm. at the time of the fault (3.7 s), the voltages in the three arms have a small disturbance which is damped to regain steady-state conditions.

The arm currents are presented in Fig. 7.25d, e, and f, for the upper, middle, and lower arm. Similar to the arm voltages, the arm currents have a small disturbance but, the currents remain controlled within the operational limits. It is worth to mention that the middle arm current have a small perturbation, compared to those in the upper and lower arm, because the current in this arm is fixed by I_3^{ac}, which is set from the optimization results (see Table 7.4).

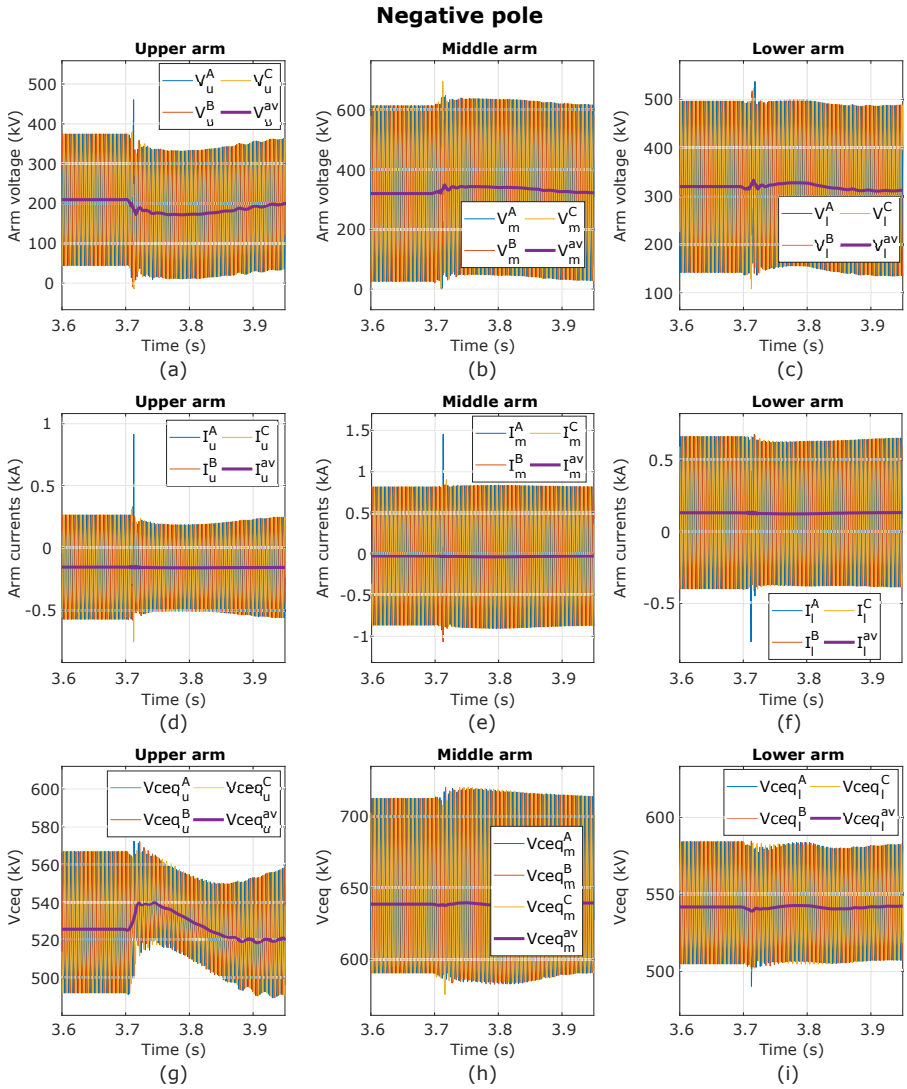


Figure 7.25: Results for the ADCC connected to the negative pole when a fault on the bipole side is simulated (Case 8). The first row presents the arm voltages, the arm currents are presented in the second row and the voltage in the equivalent arm capacitances in the third row, for the upper middle and lower arm.

The voltage of the equivalent arm capacitances are presented in Fig. 7.25g, h, and i, for the upper, middle, and lower arm. Similar to the arm voltages and currents, the voltages of the equivalent arm capacitor have a disturbance at the time of the fault but, the energy control is able to recover steady-state conditions.

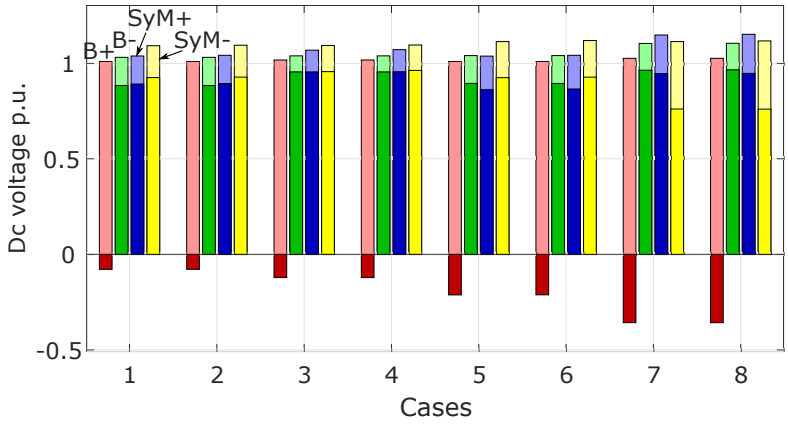


Figure 7.26: Maximum (light bars) and minimum (dark bars) pole-to ground dc voltage registered in the ADCCs for the eight cases where the fault is on the bipole line (see Table 4.5). Red, green, blue, and yellow are the voltages of the positive pole of the bipole, negative pole of the B, the SyM positive pole, and SyM negative pole respectively.

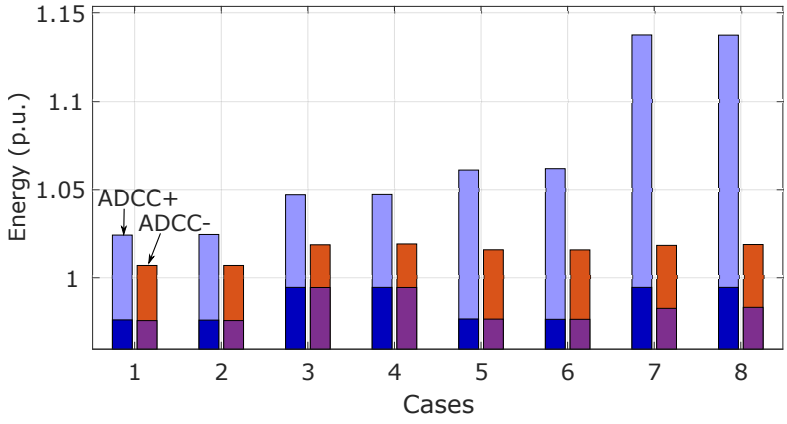


Figure 7.27: Maximum (light bars) and minimum (dark bars) total energy of the ADCCs for the eight cases of when the fault is on the bipole line (see Table 4.5).

In general, the dc-dc converter composed of two ADCCs provides immediate redundancy and the operation in degraded mode does not require additional components, or control strategy changes. The ADCC connected to the faulty pole is blocked while the ADCC- continues to operate to exchange power between the healthy zones.

The maximum and minimum voltage dynamic variation measured at the terminals of the ADCCs, for the eight cases proposed in Table 4.5, are presented in Fig. 7.26. The maximum and minimum energy dynamic variation, for the different cases, are presented in Fig. 7.27. In both figures, the worse cases are 7 and 8. The eight cases validate the FBC of the ADCC arrangement.

Fault on the symmetric monopole line

For the cases where the fault is located on the SyM line, the system does not have a degraded mode. The ADCCs can block themselves to preserve the bipole line operation. From the eight fault cases proposed in Table 4.5, the Case 4 presents the largest dynamic variations. The system results, for the Case 4, are presented in Fig. 7.28.

The power per converter station is presented in Fig. 7.28a. The power reference for the bipole line is 900 MW, for the SyM is 200MW and for the ADCCs is -500 MW (see Table 4.5). The power references are followed by the power-controlled stations, while the voltage-controlled stations adapt their power to keep the dc voltage constant. At the instant of the fault (3.7 s), the ADCCs are blocked and the power exchange is stopped within a few milliseconds. The bipole line recovers steady-state conditions as if the dc-dc converter is not connected, i.e. the power in the voltage-controlled station match the power reference in the line.

The dc voltages measured at the terminals of the ADCCs are presented in Fig. 7.28b. At the time of the fault, the positive pole voltage of the SyM drops to zero, while the negative pole has an overvoltage. The overvoltage in the SyM is limited by the surge arresters (see Section 4.3.3). On the bipole line, the voltages have a small disturbance (less than 10%) but, the steady-state conditions are recovered under 300 ms. After the fault event, as the ADCCs are blocked, the bipole continues to operate decoupled from the SyM.

The dc currents measured at the terminals of the ADCCs are presented in Fig. 7.28c. At the moment of the fault the current has a transient with a peak of 1.6 kA. When the ADCCs are blocked the current on the B side is stopped shortly after. However, the SyM side has a residual current that takes around 400 ms to be extinguished. The residual current

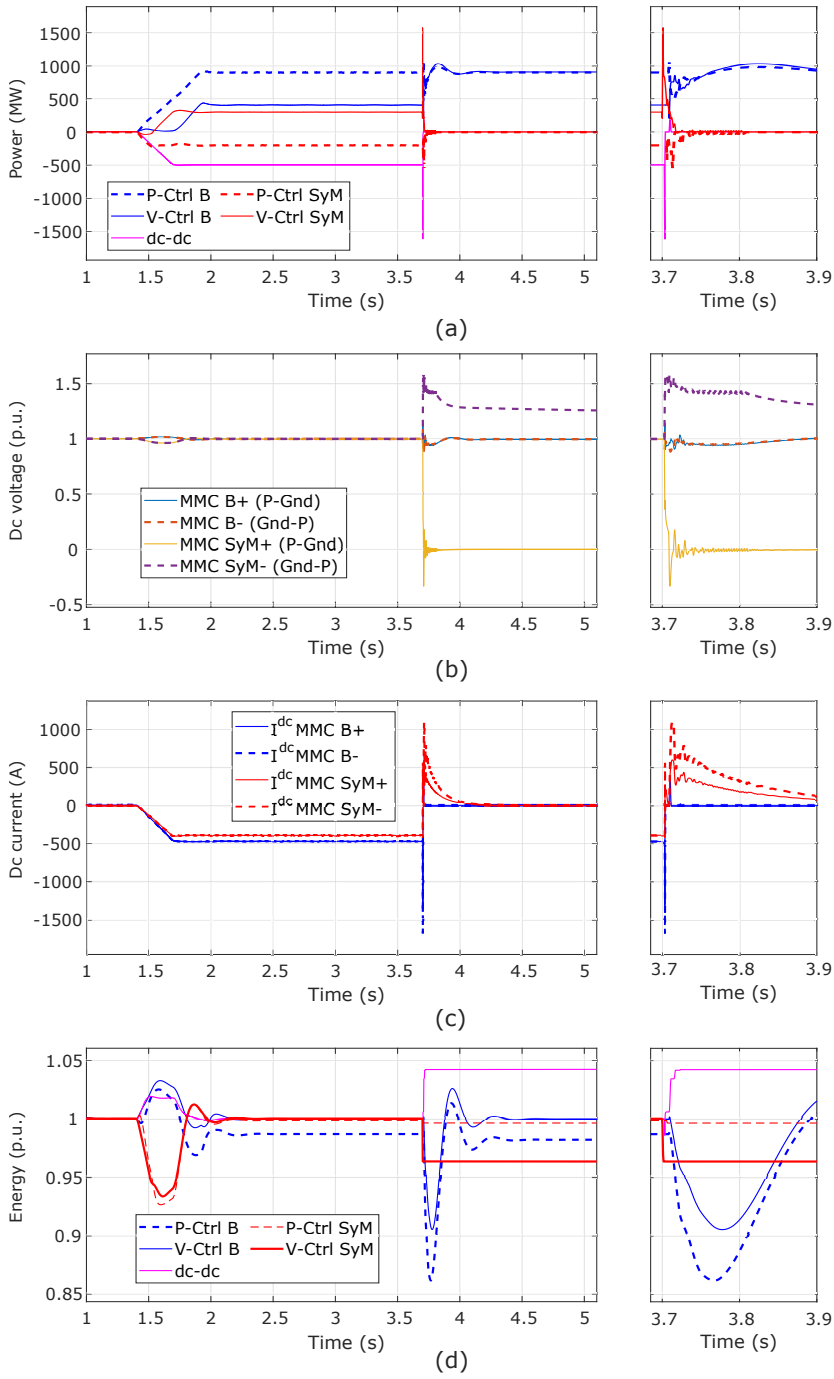


Figure 7.28: Results for a fault on the SyM side (Case 4). (a) The power per converter station. (b) The dc voltages at the terminals of the ADCCs in p.u. (c) Dc currents measured at the terminals of the ADCCs. (d) The energy per converter station.

is created by the circuit inductances discharging. After the fault isolation and current extinction, the ADCCs remain blocked and the B line operational.

The voltages of the equivalent arm capacitors are presented in Fig. 7.28d. At the instant of the fault, the energy in the ADCCs increases as the FBSMs in the upper arms charge with the fault current. On the SyM line, the voltage-controlled is partially discharged into the fault, while the power-controlled converter has a negligible energy variation. As the dc-dc converter and the SyM line are blocked, the energy in those converter stations are unable to regain nominal operation values. On the bipole line, the stations have a considerable energy dynamic variation produced by the fault on the SyM. But, steady-state conditions are recovered under 800 ms.

The detailed results for the ADCC connected to the positive pole are presented in Fig. 7.29. The voltage at the terminals of the stack of SMs is presented in Fig. 7.29a, b, and c, for the upper, middle, and lower arm. When the converter is blocked after the fault detection, the voltage in the arms are fixed by the external dc systems. The dc voltage in the arms can be estimated with (7.22). As the pole-to-ground voltage V_{M1} drops to zero, the upper arm stabilizes around 525 kV, the middle also drops to zero and the lower arm voltage follows the pole-to-ground voltage V_{M2}, which stabilizes around 400 kV (equivalent to the 1.25 p.u. voltage presented in Fig. 7.28b).

The arm currents are presented in Fig. 7.29d, e, and f, for the upper, middle, and lower arm. The currents in the upper and lower arm are stopped under a few milliseconds after the blocking signal. The upper current is blocked with the FBSMs and the lower arm currents are stopped with the HBSMs. The middle arm current is negative, corresponding to the discharging of Lo connected to the SyM. The negative current in the middle arm cannot be stopped with HBSMs. The time to stop the middle arm current depends on the energy stored in the L_o inductor and the equivalent resistance in the discharging path.

The voltages of the equivalent arm capacitors are presented in Fig. 7.29g, h, and i, for the upper, middle, and lower arm. As mentioned above, the upper arm has an increased average voltage as the FBSMs charge with the fault current. Similarly, the lower arm charges with the positive fault current through it. The middle arm changes in $V_{C_{eq}}$ are negligible as the negative current passes through the freewheeling diodes instead of the capacitor.

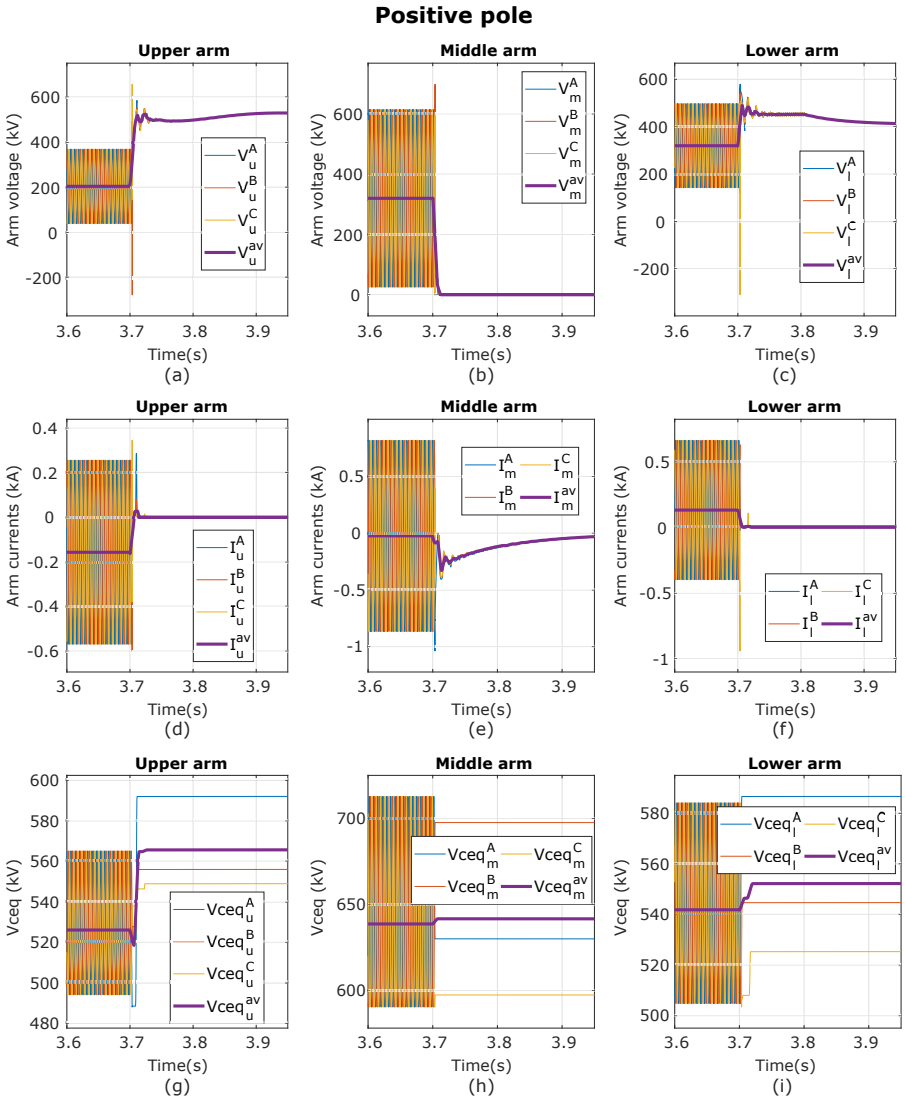


Figure 7.29: Results for the ADCC connected to the positive pole when a fault on the SyM side is simulated (Case 4). The first row presents the arm voltages, the arm currents are presented in the second row and the voltage in the equivalent arm capacitances in the third row, for the upper middle and lower arm.

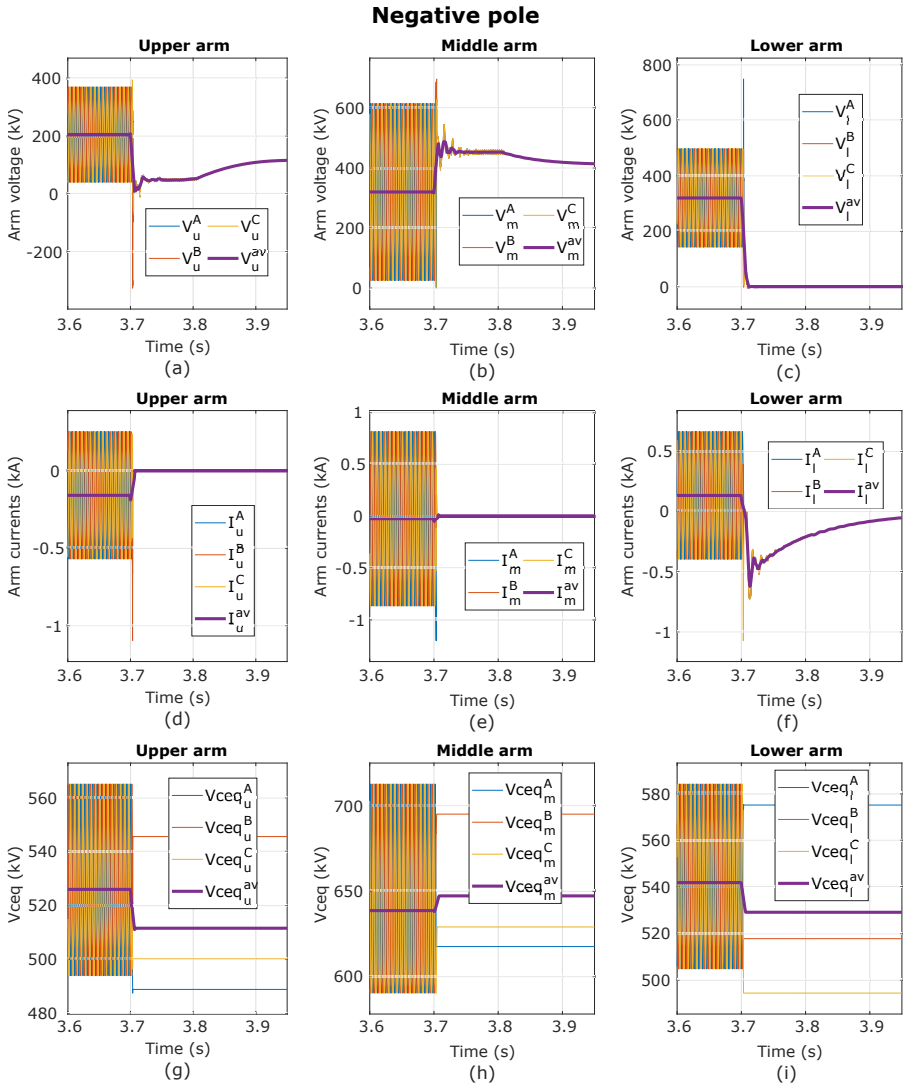


Figure 7.30: Results for the ADCC connected to the negative pole when a fault on the SyM side is simulated (Case 4). The first row presents the arm voltages, the arm currents are presented in the second row and the voltage in the equivalent arm capacitances in the third row, for the upper middle and lower arm.

The detailed results, for the ADCC connected to the negative pole of the bipole, are presented in Fig. 7.30. The voltage at the terminals of the arms are fixed by the external dc systems. The arm dc voltage

can be estimated with (7.23), it can be seen that the upper arm voltage stabilizes at $V_B - V_{M2} \approx 125$ kV, the middle arm stabilizes around 400 kV and the lower arm drops to zero following V_{M1}.

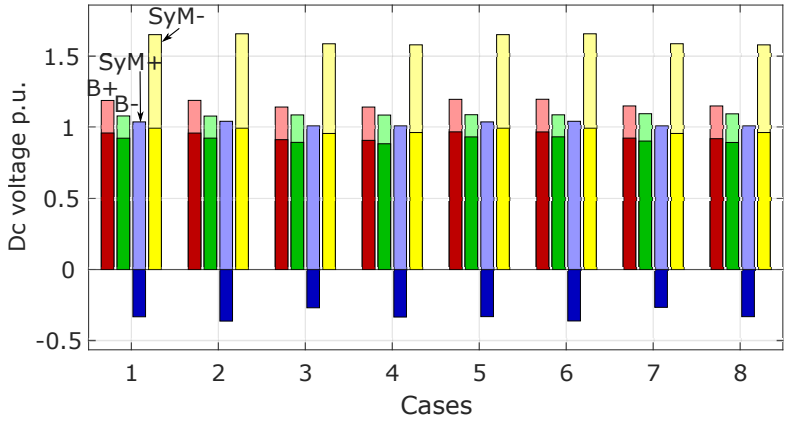


Figure 7.31: Maximum (light bars) and minimum (dark bars) pole-to ground dc voltage registered in the ADCCs for the eight cases where the fault is on the SyM line (see Table 4.5). Red, green, blue, and yellow are the voltages of the positive pole of the bipole, negative pole of the B, the SyM positive pole, and SyM negative pole respectively.

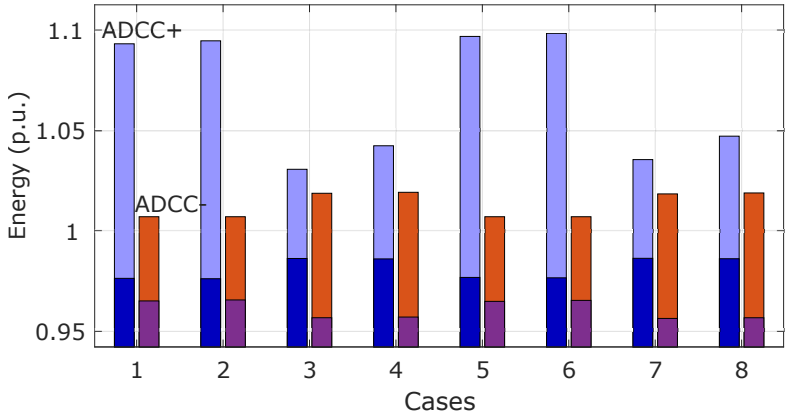


Figure 7.32: Maximum (light bars) and minimum (dark bars) total energy of the ADCCs for the eight cases of when the fault is on the SyM line (see Table 4.5).

The arm currents are presented in Fig. 7.30d, e, and f, for the upper, middle, and lower arm. In this case the upper and middle arm can stop the fault currents with their SMs opposing the external dc voltage. On the contrary, the lower arm does not have external dc voltage, and it is subject to a negative current of the L_o discharging. As the lower arm does not have FBSMs, the time to stop the current depends on the energy stored in L_o and the equivalent resistance of the discharging path.

The voltages of the equivalent arm capacitors are presented in Fig. 7.30g, h, and i, for the upper, middle, and lower arm. In the ADCC- there are not significant transients after blocking the converter, therefore, the voltages in the equivalent arm capacitors do not have considerable changes.

The ADCCs are capable to isolate the fault on the SyM without triggering the blocking signals in the bipole line. The results presented above, for Case 4, represent one of the worse cases explored in this thesis (see Table 4.5). The maximum and minimum dynamic variations of the voltage measured at the terminals of the ADCCs are presented in Fig. 7.31. The energy dynamic variations are presented in Fig. 7.32.

7.7 Chapter conclusions

This chapter has presented a new topology called the asymmetric dc converter (ADCC). The ADCC is proposed for the interconnections between an asymmetric monopole (AM) and a symmetric monopole (SyM). However, the interconnection B-SyM is possible if two ADCCs are used (positive and negative). The two ADCCs are connected in series on the bipole side and in parallel on the SyM side. The new configuration creates a physical redundancy from the bipole point of view as it has one converter per pole.

A single positive ADCC was modeled and analyzed following the methodology presented in Chapter 3 but, the results can be extended to the negative ADCC for the B-SyM configuration. The dc steady-state analysis was performed using the conditions of the interconnected systems, i.e. pole-to-ground voltages and transferred power. To keep the energy balance, circulating ac currents are needed inside the ADCC. As the ADCC does not have an ac system that fixes the characteristics of the ac values, i.e. frequency, voltage, and currents amplitudes and phases. The ac steady-state is calculated from the energy balance requirements. The ac solution is described by a underdetermined system for which an optimization algorithm has been used to define the ac operation that reduces the power losses in the arms.

Based on the steady-state solution, a preliminary converter sizing is proposed. The inductors are sized based on the pole-to-pole faults allowing to have a small arm inductance but, increasing the size of the output inductance. The capacitors in the SMs are sized based on the nominal operation.

The control design follows the methodology presented in Chapter 3. The control strategy is based on the diagonalization of the mathematical model of the converter, allowing to design simple controllers such as proportional-integral (PI) or PI-resonant (PIR) controllers. The diagonalization is achieved with current, voltage, and energy transformations. The new transformations create equivalent circuits that are controlled independently.

The converter model and the control strategy are implemented and simulated in a Matlab-Simulink environment for the interconnection B-SyM proposed in this thesis. Three sets of simulations are performed: nominal operation, normal operation and operation during and after a fault. The nominal operation simulation tests the converter behavior while exchanging the rated power, i.e. $700\,MW$. The normal operation tests the converter when it exchanges power between the bipole and the SyM under 6 different power flow conditions. The last set of simulations checks the ADCC behavior under fault conditions. A total of 16 cases were tested: eight different power flows when the fault is located on the bipole and the same power flow scenarios when the fault is on the SyM side. The simulation results confirm the good performance of the converter and control strategy under the different proposed cases.

The configuration of two ADCCs considered for the interconnection B-SyM could have coupling paths, between the poles of the B, when there is a fault on the B side. The coupling could affect the healthy zones, specially the SyM line, during the fault clearing time. To avoid major disturbances, the dc fault threshold was modified. The new threshold reduces the operating range of the ADCC compared to the other dc-dc converters studied in this thesis. However, it does not reduces the interest of the topology as the ADCC provides FBC.

The interconnection between a bipole and a SyM using ADCCs allows having immediate redundancy when a fault on a pole of the bipole occurs, e.g. the ADCC connected to the healthy pole of the bipole continues to operate during and after the fault event. After the fault event, the ADCC is able to exchange its rated power between the remaining healthy zones (350 MW).

Similar to the F2F-MMC and flexible dc-MMC, future studies should be performed to analyze the thermal behavior of the semiconductor devices face to the dc faults and, if necessary, find strategies to protect the devices such as the bypass thyristors for the HBSMs.

Chapter 8

Dc-dc Converters Comparison

8.1 Introduction

This thesis has modeled and simulated three different dc-dc converters under the same system conditions, obtaining similar results in steady-state conditions. The three converters are the F2F-MMC, the flexible dc-MMC, and the ADCC for the B-SyM. During the fault simulations, the results can change depending on the type of redundancy (immediate or not), and the degraded operations.

This chapter proposes a methodology to compare the dc-dc converters quantitative and qualitatively. The quantitative comparison is made based on key performance indicators (KPI), initially proposed in [106, 145]. The qualitatively comparison is based on the possible system requirements or ancillary services that the dc-dc converters can provide. The following sections explain in detail the two approaches.

8.2 Comparison factors

As mentioned above, the quantitative comparison is based on a set of KPIs. The KPIs are linked to the footprint of the converter station, which in turn is linked to the investment and operational cost of a project. The direct costs of a project is not straightforward to calculate. Thus, these KPIs give a global idea of a relative cost between the converters.

8.2.1 Energy factor

The cost of the capacitors is one of the main contributors to the total cost and volume of an MMC [119]. The energy factor is related to the size of the capacitors in the converter, i.e. the capacitors in the SMs. Reducing the installed capacitance can reduce the total cost and volume of the modular dc-dc converters. The energy factor is the ratio between the installed energy and the transmitted power:

$$k_E = \frac{W_{installed}}{P_T} = \frac{\sum \frac{1}{2} C_{SM} \overline{V_{SM}}^2}{P_T} \tag{8.1}$$

where C_{SM} is the capacitance per SM, $\overline{V_{SM}}$ is the average voltage in the SM, and P_T is the transmitted active power.

The average SM voltage, $\overline{V_{SM}}$, is a design parameter to calculate the capacitance per SM, C_{SM}. The design method is presented in Section 3.5.3.

As energy factor is related to the volume of the capacitors in the SMs. It represent lower volumes and cost as its value tends to zero.

8.2.2 Power losses factors

The power factors are linked to the power losses in the converter. These losses are linked to the operating cost of the project thus, the power losses factors represent better performances as their values tend towards zero. The power losses factors are the ratio between the sum of the losses in the converter and the transmitted power. Two losses factors are considered in this thesis, the conduction losses and the switching losses factors.

Conduction losses factor

The conduction losses factor is defined as follows:

$$k_C = \frac{\sum P_{SW_{conduction}}}{P_T} \tag{8.2}$$

where the conduction losses are calculated for all the semiconductor devices of the converter operating at nominal power.

The conduction losses are calculated depending on the arm current magnitude and direction and the bypass/insertion of SMs. The calculation discriminates the diode from the IGBT losses. For the HBSMs the calculation also differentiates between the upper and lower switches. For the converters considering FBSMs, the losses can be separated between the different diodes and IGBTs when the SMs are inserted. When the FBSMs are bypassed, two paths are possible, either using the upper or lower switches. To differentiate the two bypass options, the factor β is used [106]. The general expression to calculate the losses in a switch is:

$$P_{SW_{conduction}} = V_{on_{SW}} \cdot I_{SW} \tag{8.3}$$

where $V_{on_{SW}}$ is the voltage drop of the switch when closed, and I_{SW} the current through it.

To calculate the converter losses, the arms in a leg are simulated with a semi-analytical detailed model (see Appendix E.2) recording the arm current and SMs control signals. Then, the following expression is used to calculate the losses:

$$P_{SW_{conduction}} = \frac{\int_{t_0}^{t_1} \mathrm{V_{on}}\left(I(t)\right) \cdot I(t) \cdot u(t) \cdot dt}{t_1 - t_0} \tag{8.4}$$

where $\mathrm{V_{on}}$ is an approximation of the V-I curve found in the switch data sheet (see Appendix E.1). Two regressions are needed, one for the IGBT and another for the anti-parallel diode. $I(t)$ is the current through the conducting switch (IGBT or diode), and $u(t)$ is the SM control signal, i.e. 1 or 0 for HBSMs and 1, 0, and -1 for FBSMs. t_0 is the time when the simulation has reached steady-state conditions and t_1 is the total simulation time.

The steady-state time t_0 depends on the arm controller (PI implemented in this thesis), and the total simulation time is estimated as:

$$t_{sim} = t_0 + t_1 = t_0 + N_{SM} \cdot T_n. \tag{8.5}$$

where T_n is the period of the fundamental arm ac currents, i.e. 6.7 ms for the converters operating at 150 Hz.

Expression (8.4) is used for each switch contained in a leg of the converter, then it is multiplied by N_{legs} to obtain the total conduction losses.

Switching losses factor

The switching losses factor is calculated by computing the switching losses of all switches in the converter, defined as follows:

$$k_{Sw} = \frac{\sum P_{SW_{switching}}}{P_T} \tag{8.6}$$

Similar to the conduction losses, the switching losses are calculated for the nominal steady-state solution. Some analytical switching losses calculations have been proposed in the literature [13,112,146,147]. However, analytical calculation of the switching losses is not recommended for converters different from the MMC [106]. The switching losses are highly dependent on the balancing capacitor algorithm (BCA) and the arm average modulation index. Some of the converters considered in this

thesis (flexible dc-MMC and ADCCs), have different behavior from the MMC, which do not respect the hypotheses made for the formulation of the analytical evaluation of the switching losses.

To calculate the switching losses, the semi-analytical detailed model (see Appendix E.2) is simulated for the arms in a converter leg. Then, the switching losses are estimated using the energy curves found in the datasheets of the considered switches (IGBTs and diodes separately). The regressions, depending on the current, are presented in Appendix E.1.

To calculate the switching losses the following expression is used:

$$P_{SW_{switching}} = \frac{\sum_{t=t_0}^{t_1} E_{on,\,off}\left(I\left(t\right)\right) \cdot u'(t)}{t_1 - t_0} \tag{8.7}$$

where $E_{on,\,off}$ is the regression for the turn-on energy (IGBT) or the turn-off energies (diode or IGBT) depending on the current through the switch $I(t)$). The term $u'(t)$ represents the time instants where a switching event has took place.

8.2.3 Number of sub-modules

The number of SMs is used as a comparison criteria as it can be linked to the initial investment cost of the converter and the power losses, especially for the conduction losses. For example, the FBSMs installed in a converter to provide FBC are only used in case of fault. However, during the normal operation they have conduction losses even if they are bypassed. In the losses calculation the number of SMs can change the modulation index $m(t)$ or the control signal $u(t)$.

The number of SMs per converter is calculated depending for the nominal steady-state operation, the fault blocking requirements, and the degraded operation. They are calculated in Chapters 5, 6, and 7 for the F2F-MMC, the flexible dc-MMC, and the ADCCs respectively.

Number of switches

Based on the number and type of SMs (FB or HB), the number of switches can be calculated as follows:

$$N_{SW} = 2 \cdot N_{HB} + 4 \cdot N_{FB} \tag{8.8}$$

where N_{HB} is the number of HBSMs and N_{FB} is the number of FBSMs in the converter.

8.2.4 Utilization factor

This factor is defined as the ratio between the transmitted power, P_T, and the total installed power [106]:

$$k_U = \frac{P_T}{P_{required}} \tag{8.9}$$

where $P_{required}$ is the minimal installed power required by the converter to operate at nominal conditions.

The required power is calculated from the steady-state operation at rated operation point, as follows:

$$P_{required} = \sum V_{SW_{pk}} \cdot I_{SW_{RMS}} \tag{8.10}$$

where $V_{SW_{pk}}$ is the peak voltage on the switch, estimated as $V_{SW_{pk}} = \overline{V_{SM}} * (1 + \epsilon)$, where ϵ is the ripple of the capacitor in the SM. The term $I_{SW_{RMS}}$ is the RMS current through the switch, which depends on the arm current and the control signal $u(t)$.

In practical applications, the required power is smaller than the installed power as the installed semiconductors have higher ratings than the minimal ratings required. The rated power of the final semiconductors could increase due to security and reliability requirements or due to the available devices found commercially. The power $P_{required}$ is used here, as it is an ideal estimation of the minimal power required independent from the semiconductor devices technology and the converter topology.

The utilization factor can have values between 0 and 1, it represents better device utilization when approaches to one. To homogenize the utilization factor with the rest of the KPIs, the following factor is proposed:

$$k_o = \frac{1}{k_U} \tag{8.11}$$

where k_o is the oversize factor.

The new factor k_o represents how much required power is needed to exchange the rated power. This factor can have values from 1 to infinite, where 1 is the ideal converter. As the performances of k_o are degraded as it is bigger, the oversize factor represents better results when it tends to 1.

8.2.5 Magnetic factors

The previous factors have been proposed in [106], additional details and conclusions can be found in the original publication. To compare the dc-dc converters, two additional factors are considered in this thesis: the magnetic factors. These factors are used to compare the use of magnetic components in the dc-dc converter topology, i.e. the inductors and transformers. The factors assume the following hypotheses:

- As the voltage increases, the insulators should be adapted, increasing the total volume of the inductor. As the current increases the cross section of the conductors should increase, increasing the total volume, weight, and cost of the inductor. In general, the magnetic elements increase their cost proportionally to their apparent power.
- The volume of the metallic core elements, is inversely proportional to the operating frequency.
- The losses in the magnetic elements can be neglected compared to the losses of the semiconductor switches.

The magnetic factors are defined as follows:

$$k_{air-core} = \frac{\sum_{i=1}^{N_{a-c}} S_{air_i}^{required}}{P_T} \tag{8.12}$$

$$k_{solid-core} = \frac{\sum_{i=1}^{N_{s-c}} S_{core_i}^{required}}{P_T \cdot f} \tag{8.13}$$

where $k_{air-core}$ is the magnetic factor of the inductive elements with air core; N_{a-c} is the number of inductances with air core in the converter; $k_{solid-core}$ is the magnetic factor of the inductive elements with solid core, e.g. ac transformers; N_{s-c} is the number of magnetic elements with solid core in the converter; $S_i^{required}$ is the apparent power of the i^{th} magnetic element (either air or solid core) calculated for the nominal operating power; and f is the operating frequency.

The apparent power of the air core elements can be estimated as:

$$S_{air}^{required} = X_{L_{air}} \cdot I_{RMS}^2 = 2\pi\, f\, L_{air} \cdot I_{RMS}^2 \tag{8.14}$$

where L_{air} is the inductance, and I_{RMS} is the RMS current through the air core inductor.

The magnetic factors can be related to the cost of the elements (inductors and transformers) thus, the magnetic factors represent lower initial costs as they approach zero.

8.3 Ancillary services

The dc-dc converters, in HVDC applications, can provide some ancillary services [148] such as: increased power flow flexibility, pole balancing, dc voltage support, fault blocking capability, redundancy, degraded operation, and black start capability. The different system services are detailed below.

8.3.1 Power flow flexibility

Using dc-dc converters to interconnect two (or more) dc lines can increase the power flow flexibility and system controllability. The dc-dc converters can be used to interconnect new loads or generation centers to an existing HVDC line. The dc-dc converter allows the control of the power flow between the interconnected systems.

8.3.2 Pole Control

The dc-dc converters can help to balance the poles in a bipole or a SyM. Depending on the nature of the unbalance, a power or voltage control could be needed. The generalities are presented below.

Bipole

During the normal operation of a bipole, the poles are balanced and the current through the ground/metallic return is zero. In case of any unbalance, a current on the ground/metallic return could appear to keep the voltage balanced. As the bipole has a control decoupled per pole, the voltage unbalances can be controlled automatically. But, for future dc grids or dc multi-terminal schemes the bipole lines could be subject to power unbalances, which can be re-balanced using the dc-dc converters in the system.

The dc-dc converters capable to re-balance the power in a bipole line are those converters that can decouple the power per pole. For the three converters considered in this thesis, only the F2F and the ADCCs are able to set different power references per pole.

The bipole lines without ground/metallic return, i.e. the rigid bipole could behave differently. The absence of a path to re-balance the voltage could lead to variations in the pole-to-ground voltages. The control proposed for the RB lines [20] can balance the pole-to-ground voltages on the grounded converter station but, the power-controlled station voltage could vary during transients. In this particular case, a dc-dc converter with decoupled voltage control per pole can re-balance the pole voltages.

Symmetric monopole

Similar to the B lines, the SyM the poles are balanced and there is no current through the ground. The symmetric monopole controls the pole-to-pole voltage, and in case of an asymetrical disturbance, e.g. a pole-to-ground fault, the pole voltages are disturbed. It is known that the pole-to-ground fault in a SyM line created an overvoltage on the healthy pole, which is limited thanks to the overvoltage protections in the line. To recover steady-state conditions, the ac-dc converters could use an homopolar current that goes through the ac grounding (see Section 4.3.4).

In the future dc grids or dc multi-terminal scheme, the voltage re-balancing control could be an important ancillary service for the SyM lines. To achieve this control, the dc-dc converter should be able to control the currents through the ground. The current magnitude can be comparable to the currents through the ground/metallic return in the bipole lines and should be only needed for small disturbances or to recover a faulted SyM line.

8.3.3 Dc voltage support

The dc-dc converter can help in the dc voltage support in different ways listed below.

- Allowing a generalized droop control in the multi-terminal scheme. The converters change their power exchanged depending in the voltage variation.
- Controlling the fault currents. The dc-dc converters can be set to control and reduce the fault currents reducing the impact on the dc voltage variation.
- Supporting the dc voltage with its internal energy. The dc-dc converters can use their internal energy to feed the healthy zones during a fault transient.

- Fast blocking. Depending in the dc-dc converter and the interconnected systems, a fast fault detection could reduce the impact of the fault on the healthy zones.

In general, the voltage control depends on the dc inertia which can be adjusted with the dc grid or multi-terminal control. This system approach is out of the scope of this thesis.

8.3.4 Fault blocking capability

As explained in Section 1.6, the fault blocking capability (FBC) is the ability of a dc-dc converter to isolate the faulted zones without triggering the blocking signals or exceeding the operating limits (voltages and currents) of the healthy zones.

The FBC can be achieved with different approaches, the most common ones are using FBSMs or DCCBs. The FBC could be inherent to the dc-dc converter topology, as the F2F-MMC interconnecting two asymmetric monopoles or the F2F using ac-dc converters with inherent FBC, e.g. the AAC or the AFCB (see Chapter 2). In consequence, the dc-dc converter can be an element that participates in the protection strategy of a system.

8.3.5 Redundancy

The redundancy is the capacity of a dc-dc converter to exchange power after a fault in the system, normally after a fault in a pole of the bipole. There are two possible scenarios explored in this thesis, the immediate redundancy or the interrupted redundancy (see Section 1.3.1). The redundancy can reduce the impact of a fault on the interconnected systems.

8.3.6 Degraded operation

The degraded operation defined in this thesis (see Section 1.5), is the scenario where the line topology at the terminals of the dc-dc converter changes after a fault. This can only happen for faults in a pole of a bipole (either B or RB). The dc-dc converter with degraded operation can be used to exchange power between a faulted line and a healthy system while the repairs are made, reducing the cost of the contingency.

8.3.7 Black-start capability

After a fault that has triggered the blocking signals in one of the interconnected dc systems, the dc-dc converter can be used to restart the system after the fault clearance. The dc-dc converter can provide a ramping

dc voltage helping to charge the SMs in the faulted side. The dc-dc converter could use part of its internal energy or use the power from a healthy side.

8.4 Converter Comparisons

8.4.1 Quantitative comparisons

This section presents a quantitative comparison of the considered converters studied in this thesis. The eight comparison factors (KPIs) presented in Section 8.2 are used to compare the considered converters. The KPIs are calculated for three scenarios: the converters sized for the case study, the converters without FBSMs, and the F2F operating at 50 Hz. The cases are detailed below.

- **Converters considered for the case study (Case 1):** The first comparison is between the converters considered for the case study. The details of each converter can be found in Chapters 5, 6, and 7.

  To recall, the F2F-MMC operates at 150 Hz and provides FBC with ACCBs. The flexible dc-MMC uses FBSMs to stop the fault currents and to operate in degraded mode. Lastly, the ADCCs also provide FBC with FBSMs but, they are not needed for the degraded operation.

- **Converters without FBSMs (Case 2):** One of the principal reason to consider FBSMs in the converter design is to provide FBC but, this ancillary service can be provided by external DCCBs. The FBC is not a service that can be achieved for free, it requires additional investment. This comparison scenario is proposed to make evident the impact of the additional FBSMs.

  For this comparison scenario only the non-isolated converters are affected as the F2F-MMC does not use this type of SMs. The difference between the flexible dc-MMC and the ADCCs is that the former used the FBSMs not only for the FBC but also to operate in degraded mode (see Chapter 6). Thus, the flexible dc-MMC without FBSMs looses the capacity to operate in degraded mode. On the other hand, the ADCCs only uses the FBSMs to stop the fault currents, it does not loose the capacity to operate in degraded mode as it has physical redundancy with an ADCC per pole.

- **Transformer operating at 50 Hz (Case 3):** The medium frequency transformer operating at high voltage and high power has not been developed yet. The design of this transformer could be challenging [6]. This third comparison scenario is proposed to show the impact of the operating frequency on the converter design. As the F2F-MMC is the only converter with an ac transformer, this is the only topology changed in this scenario.

Table 8.1 presents a summary of the comparison cases and their differences. The comparison results are presented below.

Table 8.1: Differences between the comparison scenarios proposed

<table>
<tr><th></th><th>Case 1</th><th>Case 2</th><th>Case 3</th></tr>
<tr><td>F2F-MMC</td><td rowspan="3">Reference</td><td>No change</td><td>50 Hz transformer</td></tr>
<tr><td>Flexible dc-MMC</td><td rowspan="2">No FBSMs</td><td rowspan="2">No change</td></tr>
<tr><td>ADCCs (one per pole)</td></tr>
</table>

Comparison results

The results of the comparison are presented in Fig. 8.1. It is worth reminding that all the comparison factors represent better performances when the value approaches zero, i.e. the center of the diagram. The eight factors are normalized with respect to to the greater value between the three converters and the three cases.

The results for the Case 1 are presented in Fig. 8.1a. It can be noticed that the F2F-MMC is the topology with lower energy factor, followed by the flexible dc-MMC and lastly by the ADCCs. As the energy factor is linked to the cost of the capacitors, a greater energy factor could lead to increased converter cost (compared to the F2F-MMC).

The power losses (k_c and k_{Sw}) are higher for the F2F-MMC. The non-isolated converters have better performances. The flexible dc-MMC has the lowest switching and conduction losses due to a lower number of SMs and relative low arm currents. The ADCCs have similar number of SMs and conduction losses as the F2F-MMC but, lower switching losses. The power losses factors are linked to a portion of the operational cost of the converter, the results suggest that the non-isolated converters could have lower operational cost compared to the F2F-MMC.

One of the impacts of using FBSMs is the total number of switches required (N_{SW}). It can be noticed that the number of SMs (N_{sm}) in the F2F is similar to that of the ADCCs but, as the ADCCs use FBSMs, the number of switches in this last topology is higher. Similar analysis can be done between the number of SMs and switches of the F2F and the flexible dc-MMC, where the former has more installed SMs but similar number of switches as the flexible dc-MMC.

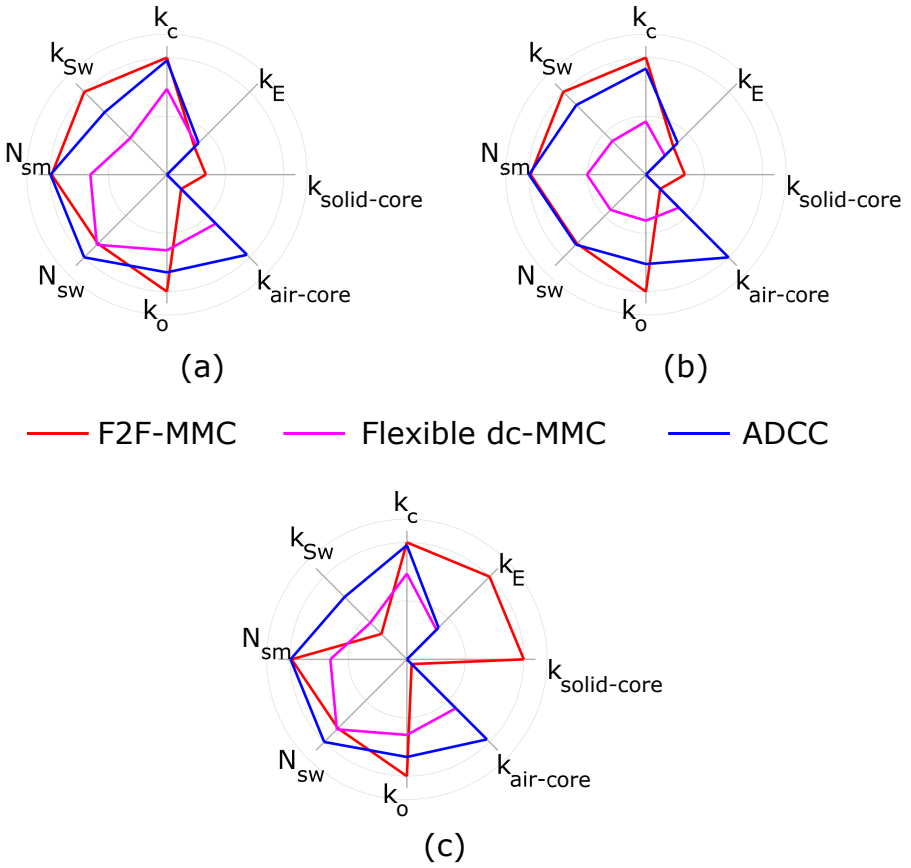


Figure 8.1: Comparison results for the three proposed cases: (a) original converters considered for the case study, (b) converters without FBSMs, and (c) F2F-MMC operating at 50 Hz.

When comparing the oversize factor (k_o), the F2F-MMC has the higher value as it requires an installed power at least twice as the transmitted power (because of the two ac-dc transformation stages). The converter with lower power requirements is the flexible dc-MMC and the ADCCs is in between the other two.

From the three topologies compared, the F2F-MMC is the one with lower air-core inductance requirements, represented by $k_{air-core}$. The converter with higher inductive requirements is the ADCCs because of the internal circulating power required to keep the energy balanced. Even if the flexible dc-MMC has bigger inductances, $L = 82$ mH and $L_o = 200$ mH, compared to the $L = 15$ mH and $L_o = 200$ mH of the ADCCs, the flexible dc-MMC has lower value of $k_{ari-core}$ because of the relative lower internal currents.

The last factor to compare is the $k_{solidcore}$. As the F2F-MMC is the only converter using a transformer, it is the only that has a non-null factor.

The results for the comparison Case 2 are presented in Fig. 8.1b. Recalling Table 8.1, the F2F results do not change as the F2F-MMC does not use FBSMs. The results for the flexible dc-MMC and ADCCs have changes compared to the results presented in Fig. 8.1a. The flexible dc-MMC without FBSMs improves in every factor but, it losses the capacity to block fault currents and to operate in degraded mode. If the flexible dc-MMC is designed to operate in degraded mode, it would naturally have the FBC as the number of FBSMs required to operate in degraded mode is higher than the FBSMs needed to block the fault currents (see Chapter 6). On the other hand, the ADCCs does not improve as much as the flexible dc-MMC. Compared to the Case 1, the ADCCs without FBSMs have lower number of switches, which is comparable to the F2F-MMC.

The results for Case 3 are presented in Fig. 8.1c. In this case, the non-isolated converter frequencies remain the same and the F2F-MMC changes its operating frequency to 50 Hz (see Table 8.1). In this case, the F2F-MMC increases k_E and $k_{solid-core}$. On the other hand, the switching losses are reduced and the rest of the factors do not change. In general, the F2F-MMC operating at 50 Hz have a greater volume with respect to the converter operating at 150 Hz, which is expected.

In general, it can be concluded that the flexible dc-MMC (magenta line) has better performances compared to the other two topologies. The ADCCs are penalized for their internal circulating power (see Appendix F) but, its design could be optimized to improve its performances. The flexible dc-MMC has lower internal ac currents

Additional comparison cases

Four additional comparison scenarios are proposed to check the variations in the KPIs of the three converters. The converters designed for the case study are set as the reference to the new scenarios. The first scenario changes the voltage ratio (VR) $VR = 1.1$ and $VR = 1.8$. The second scenario considers converters without FBSMs (case presented in Fig. 8.1b). The third scenario changes the operating frequency to 100 Hz and 50 Hz. The last scenario changes the number of legs to $N_{legs} = 2$ whenever is possible. The results, per converter, are presented below.

- **F2F-MMC results:** The results for the four scenarios are presented in Fig. 8.2. It can be noticed that the F2F-MMC could have better performances when the voltage ratio is low ($VR = 1.1$), except for the conduction losses, the reactive power and $k_{air-core}$ factor. As presented in previous section, the F2F-MMC considered in this thesis does not uses FBSMs, thus it does not change in Fig. 8.2b.

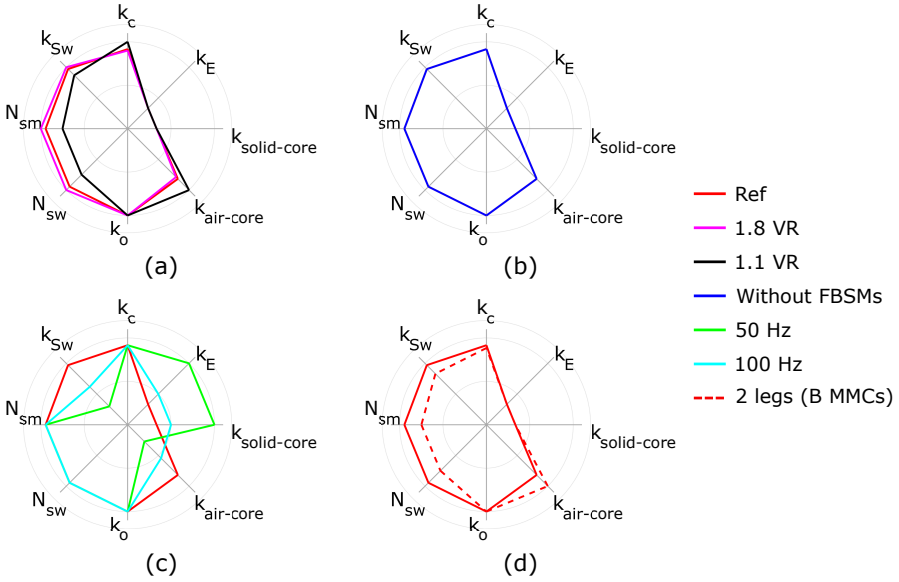


Figure 8.2: Comparison results for the F2F changing: (a) the voltage ratio, (b) without FBSMs, (c) the operating frequency, and (d) the number of legs on the B side.

Figure. 8.2c presents the case when the operating frequency is changed. It can be noticed that $k_{air-core}$ and k_{Sw} increase with the frequency. It is worth to mention that the inductance value

does not change with the frequency but it's impedance does. On the other hand, $k_{solid-core}$ and k_E decrease when the operating frequency is increased.

The last scenario reduces the number of legs when possible. For the IGBTs considered in this thesis (3.3 kV and 1.8 kA), only the MMCs on the B side can be reduced to 2 legs. The MMC on the SyM continues to use three legs. In this case, the transformer should use an special Scott connection between HV and LV [149]. The F2F-MMC with two legs on the B converters improve most of the KPIs evaluated, except for $k_{air-core}$ factor, due to the increased arm currents.

- **Flexible dc-MMC:** The results for the flexible dc-MMC are presented in Fig. 8.3. In general, the converter has better KPIs when decreasing the VR, except for the number of SMs and switches. These elements have little changes as the mainly depend on the degraded operation and FBC requirements. As presented before, the converter has better KPIs when it does not use FBSMs.

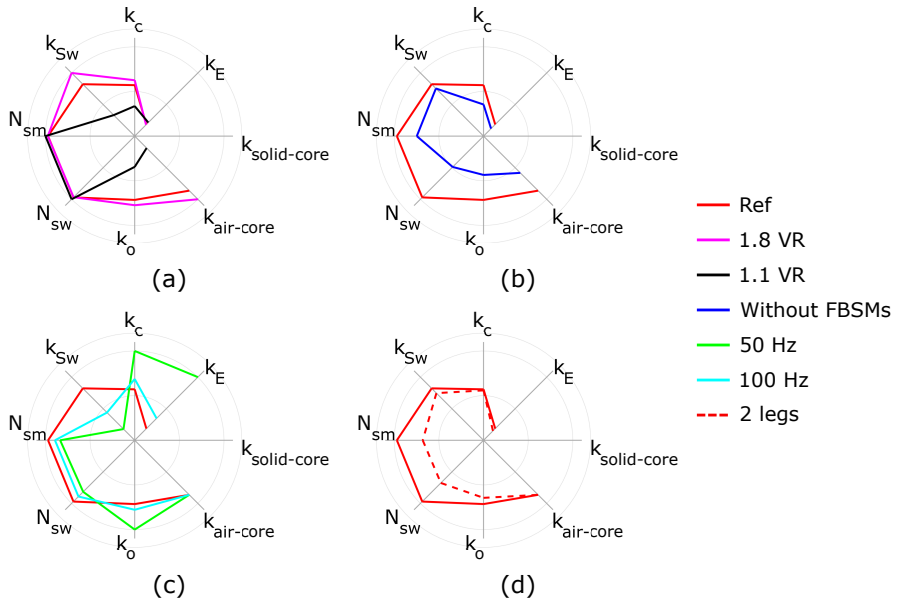


Figure 8.3: Comparison results for the Flexible dc-MMC changing: (a) the voltage ratio, (b) without FBSMs, (c) the operating frequency, and (d) the number of legs.

When the operating frequency is changed, see Fig. 8.3c, the converter can reduce the number of SMs required because the impedance of the inductors is reduced, reducing the ac voltage generated in the arms. However, this also increases the conduction losses as the arm currents increase with the reduced voltage and impedances. This can be observed in the increased results of k_C and k_o factors when the operating frequency is also increased (see Fig. 8.3c).

- **ADCC:** The results for the ADCCs are presented in Fig. 8.4. The ADCCs present better KPIs when the VR is reduced to 1.1. On the other hand, the ADCCs without FBSMs do not improve the results, see Fig. 8.4b.

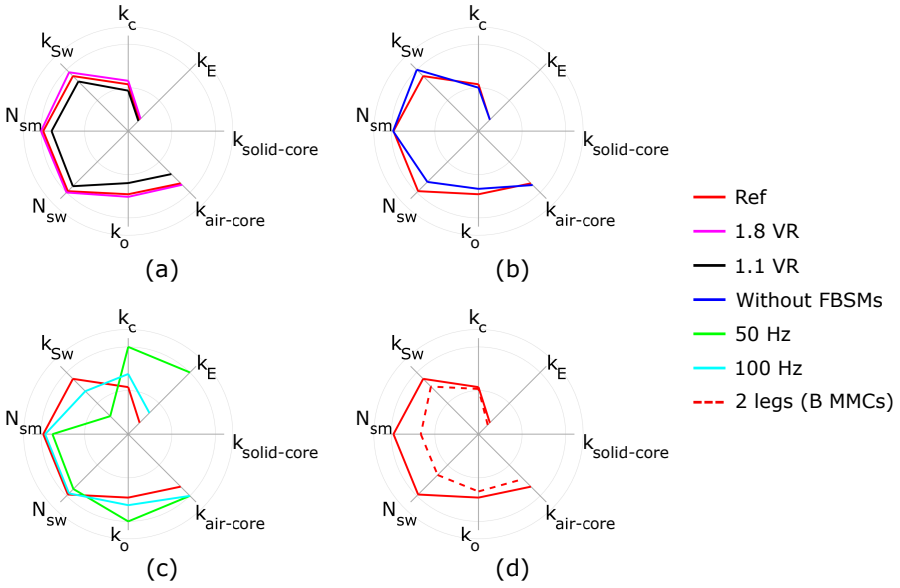


Figure 8.4: Comparison results for the ADCCs changing: (a) the voltage ratio, (b) without FBSMs, (c) the operating frequency, and (d) the number of legs on the B side.

Similar to the flexible dc-MMC, the ADCCs with reduced operating frequency improve k_{Sw}, N_{sm}, N_{sw}, but increase k_E, k_c, and k_o, see Fig. 8.4c. Lastly, the ADCCs improve all their KPIs when a converter with only two legs is considered, see Fig. 8.4d.

8.4.2 Qualitative comparisons

This section presents the comparison based on the ancillary services that the converters can provide.

From the simulation results presented in Chapters 5, 6, and 7, it can be concluded that the three converters can provide the same power flexibility for the considered case study. The three converters were capable to operate under the different power flow conditions proposed in Section 4.4.1.

The capacity to balance the poles can vary depending on the converter. The F2F-MMC considered for this thesis can balance the poles only on the bipole side as this converter does not have a path to ground on the SyM side. A F2F considering an ac grounding, e.g. a star point reactor, could have a balancing control using currents through the grounding point. However, the system impact of a new grounding is not clear. The flexible dc-MMC proposed in this thesis is able to re-balance the poles on the SyM only. The solution with the ADCCs uses two converters that can be used to balance the poles on the SyM (as proposed in this thesis) or the poles on the bipole (changing the power reference per converter). The ADCCs are the only converter that might provide pole control on both sides at the same time thanks to the decoupled control per converter.

The dc voltage support is a complex subject not studied this thesis. The dc-dc converters can support the dc voltage changing the control mode to voltage control, or droop control. These options depend on the grid control strategy, the disturbance events and system characteristics in general.

The fault blocking capability (FBC) can be achieved with additional FBSMs (or ACCB for the F2F-MMC). In all three converters, the FBC can be also provided by DCCBs.

The redundancy after a fault on one pole of B can be provided with the three topologies presented in this thesis. The F2F and ADCCs can provide immediate redundancy, while the flexible dc-MMC needs to stop the power transmission to isolate the fault. After the fault clearance, the three converter can operate in degraded mode, equivalent to an AM-SyM interconnection. The structures of the F2F and ADCCs do not require additional elements to operate in degraded mode. In contrast, the flexible dc-MMC requires additional FBSMs to operate in degraded conditions.

Table 8.2: Ancillary services provided by the dc-dc converters considered for the case study

	F2F-MMC			Flexible dc-MMC			ADCCs		
	Case 1	Case 2	Case 3	Case 1	Case 2	Case 3	Case 1	Case 2	Case 3
Power flexibility	All converters can provide the same power flexibility								
Pole control	Bipole			SyM			Both		
dc voltage support	Possible								
FBC	ACCB, DCCB, or FBSMs	ACCB or DCCB	ACCB, DCCB, or FBSMs	FBSMs, or DCCB	DCCB	FBSMs, or DCCB	FBSMs, or DCCB	DCCB	FBSMs, or DCCB
Redundancy	Immediate			Interrupted	No	Interrupted	Immediate		
Degraded operation	Yes			After circuit reconfiguration	No	After circuit reconfiguration	Yes		
Black start capability	Possible								

Linked to the voltage control, the three dc-dc converters are able to provide black-start capability. The dc-dc converter can be used to start the faulty side using the healthy zones or its internal energy. The different ancillary services that the dc-dc converters can provide are presented in Table 8.2.

8.5 Conclusions

The three converters studied in this thesis, i.e. the F2F-MMC, the flexible dc-MMC, and the ADCCs were compared in this chapter. The reference for the comparison are the converters designed for the case study presented in Chapter 4. Then, two additional scenarios were proposed: without FBSMs and with the F2F operating at 50 Hz, as the medium frequency transformer for high voltage and high power has not been developed yet.

The results suggest that the flexible dc-MMC is a topology that could have reduced operating cost, compared to the other two converters, thanks to its low power losses. The flexible dc-MMC could also provide a volume reduction compared to the F2F-MMC, as the dc-MMC does not use an intermediary ac transformer. Further reductions in the KPIs values of the flexible dc-MMC can be achieved if the fault blocking capability and the degraded operation is not required. For this case, the converter initial cost (linked to k_E, N_{sw}, k_o, and $k_{air-core}$), could be halved, with respect to the F2F-MMC.

On the contrary, the ADCCs do not have significantly better KPI results compared to the F2F-MMC. However, the ADCCs can reduce the project cost compared to the F2F-MMC, because the ADCCs do not need an ac transformer. The operating cost can be also reduced as the ADCCs have lower switching losses. The ADCCs can be used to balance the poles on the B and SyM line, which cannot be done with the flexible dc-MMC or the F2F without an ac grounding point. Different to the flexible dc-MMC, the ADCCs do not need additional elements (FBSMs) to operate in degraded and provides immediate redundancy. Further studies on the ADCC should be done, as the topology could improve its performances with optimized inductances (L and L_o).

Some design parameters were changed to evaluate their impact on the KPI per converter. The converters designed for the case study were set as the reference. The KPIs were evaluated changing the voltage ratio, the use of FBSMs, the operating frequency and the number of legs (when possible). The F2F-MMC has better performances when the voltage

ratio and number of phases is reduced. The KPIs for the flexible dc-MMC are improved when FBSMs are not required and with a reduced number of legs. Finally the ADCCs (one per pole) have better KPIs when the number of legs is reduced. These results could help future studies to identify the possible applications of each converter.

Chapter 9

Conclusions and future work

The dc-dc converters for high voltage direct current (HVDC) applications are one of the key elements for the step-wise development of dc multi-terminal schemes (radial) and dc grids (meshed). The dc-dc converters could help to develop the dc grid as it can interface two, or more, dc systems. The dc-dc converters are usually compared to the ac transformer as they can adapt the voltage difference between two systems but, the dc-dc converter can adapt the differences in line topologies or HVDC technologies (VSC and LCC). This allows interconnecting dc projects already existing, with different characteristics, reducing the initial cost of a multi-terminal project. Compared to the ac transformers, the dc-dc converters provide additional features such as increased controllability, voltage control, fault blocking capability, redundancy, degraded operation, and black-start capability.

This thesis has explored the possible heterogeneous HVDC interconnections, i.e. the interconnections between dc systems with different technologies, with medium to high voltage ratio, or with different line topologies. The general conclusions, contributions, and perspectives of the thesis are presented below.

9.1 General conclusions

Analyzing the existing and future HVDC projects (see Appendix G), it can be noticed that the voltage source converters (VSCs) are the preferred HVDC technology. VSCs present extended control flexibility compared to the line commutated converters (LCC), which makes them interesting to support the ac grid. From the project list, it was also observed the similarity between the voltages. The projects considering cable installations are restricted to the rated voltage of the cable technologies. From the list, it can be also noticed that the most common line topologies are the B and the SyM.

Assuming that the future dc networks can be developed interconnecting dc lines through dc-dc converters. The most probable interconnection could be between a bipole (B) and a symmetric monopole (SyM). The main requirements for the dc-dc converter are:

- Fault blocking capability: stopping fault current contribution from the dc lines.
- Immediate redundancy: after a fault on one pole of the B, the dc-dc converter should continue to exchange power with the healthy pole uninterruptedly.
- Degraded operation: the operation after a fault on one pole of the bipole, equivalent to a AM-SyM interconnection.
- Power exchange capability: exchanging power between the lines.

After a review of the literature on HVDC dc-dc converters, two initial topologies were chosen: the front-to-front modular multi-level converter (F2F-MMC) as it is based on the commercially available technologies, and the dc-dc MMC (dc-MMC) due to its resemblance to the ac-dc MMC and its smaller footprint (no need of an ac transformer and reduced number of components), compared to the F2F-MMC. The dc-MMC was modified to interconnect different line topologies, which resulted in a new converter topology called flexible dc-MMC. The flexible dc-MMC can be used for the B-SyM interconnection. However, this converter does not allows the immediate redundancy after a fault in a pole of the B. The flexible dc-MMC must stop the power transfer and reconfigure into degraded operation. The reconfiguration is required to disconnect the faulted pole. To provide FBC, the flexible dc-MMC uses FBSMs. These FBSMs are needed to block the fault currents through the converter. Additional FBSMs are needed to operate in degraded mode. To solve the problems found with the flexible dc-MMC, the asymmetric dc-dc converter (ADCC) was proposed and studied. The ADCC main application is the AM-SyM interconnection but, using two ADCCs (one per pole on the B) the B-SyM interconnection is possible. The ADCC provides immediate redundancy and degraded operation by simply blocking the converter connected to the faulted pole. The FBC can be achieved with additional FBSMs. Contrary to the flexible dc-MMC, the ADCC does not require additional elements or reconfigurations to operate in degraded mode.

The three converters were modeled following a strategy proposed in this work. The mathematical model was used to have a preliminary converter design and to implement a simplified control strategy. The

considered converters operate at 150 Hz to reduce the volume of the capacitors in the sub-modules (SMs). However, the inductor values cannot be reduced with the increased operating frequency. The main criteria to size the converter inductors is the fault current slope limitation. The worst scenario for the fault current is the pole-to-pole fault and the current slope depends on the pole-to-pole dc voltage, which is independent of the operating frequency.

To test the converter topologies, three sets of simulations were performed: nominal operation, normal operation, and two fault scenarios. The nominal operation was simulated to verify the control design and converter operation. The capacitor voltage ripple and precalculated operating points were respected by the three considered converters. The control strategy was validated as it is capable to follow the changes in the power reference. For the normal operation simulations, different power flow directions, though the dc-dc converter and the lines, were tested. From the results, it can be concluded that the three dc-dc converters have the same power control capability as the power exchanged did not violate the normal operation margins. The fault scenarios were performed to check the FBC and degraded mode operation.

The fault analysis and simulation results suggest that the considered structure for the F2F-MMC, i.e. three MMCs with two ac transformers, could not be the best arrangement to avoid disturbances on the healthy zones during a fault on the bipole line. The considered F2F-MMC relies on ACCBs, DCCBs, or FBSMs to stop the fault currents rapidly. The fault clearance time is a critical condition to isolate the healthy zones from the fault disturbance, because the fault impact is larger when the fault clearance time is increased. It has been shown that the only presence of an ac transformer does not ensure the decoupling of the different protections zones. The F2F-MMC requires a coordination between the protection devices (ACCBs, DCCBs, or FBSMs). The FBC could rely only on the control strategy, without DCCBs, ACCBs, or FBSMs, if a structure of two F2F-MMCs, one per pole, is considered. In case of a fault in a pole of the B, only the F2F connected to the faulted pole is blocked. The second dc-dc converter continues to operate uninterruptedly, i.e. this structure provides FBC and immediate redundancy. However, future studies must be done to confirm these hypotheses.

From the fault simulation of the flexible dc-MMC under fault conditions, it can be evidenced that the converter cannot provide immediate redundancy. The converter stops the complete power transfer, which dis-

turbs the healthy zones, and restart operation in degraded mode. After the fault clearance, the degraded operation provides power flexibility for the AM-SyM interconnection.

The ADCC has good performances during the fault simulations. The two converters provide the pole decoupling, i.e. after a fault in one pole of the bipole, the healthy one continues to operate uninterrupted (immediate redundancy). The solution with the considered ADCC has similar results than the F2F-MMC. However, the ADCC can reduce the dc-dc converter footprint as it does not use ac transformer.

After the individual analysis of the converters, a set of key performance indicators (KPIs) was presented to compare the three converters. Three comparison scenarios were considered: the converters used in the case study, the converters without full-bridge sub-modules (FBSMs), and a scenario comparing the F2F-MMC operating at 50 Hz. The flexible dc-MMC presents better indicators than the other two topologies for the aforementioned comparison scenarios. The F2F-MMC and ADCC have similar results except for the indicator related to the magnetic elements with metallic core ($k_{solid-core}$), where the ADCC had better results as it does not use ac transformers.

A qualitative comparison was also realized to evaluate the three dc-dc converters and the possible ancillary services that they can provide. For this comparison, the F2F-MMC and ADCC have better results as they can provide immediate redundancy and degraded mode operation even if the FBC is relying on external dc circuit breakers (DCCBs).

9.2 Main contributions of the thesis

- A general methodology to develop a simplified control strategy for modular converters. The methodology is based on the diagonalization of the mathematical model to decouple the state variables.

- Extended capacitor sizing comprising the negative modulation for the arm including FBSMs.

- Study of a F2F-MMC composed of three MMCs and two ac transformers. The study includes the normal operation and fault behaviour.

- Study of the flexible dc-MMC for the B-SyM and RB-SyM interconnections in normal operation and faults.

- Proposal of a new dc-dc converter, the ADCC, for the AM-SyM interconnections. By using two elementary converters the B-SyM interconnection can be performed.
- Study of the ADCC in normal operation and faults.
- Quantitative and qualitative comparison of the considered dc-dc converters (the F2F-MMC, the flexible dc-MMC, and the ADCC).

9.3 Future work

The future work from this thesis is detailed as follows:

- Chapter 3:
  - Validate the modeling strategy with different modular multilevel converters.
- Chapter 5:
  - Study in detail the internal ac system. The losses optimization and the reactive power contribution of each MMC.
  - Study different F2F structures changing the transformer coupling and grounding.
  - Study in detail the decoupled F2F, i.e. having a F2F per pole of the bipole.
  - Investigate the converter control during faults to reduce the impact on the healthy zones.
  - Assess the benefits and drawbacks of the different strategies to provide FBC, i.e. ACCBs, DCCBs, and FBSMs.
- Chapter 6:
  - Investigate the optimized design of the circuit inductor values L_o and L, as they have an impact on the power losses.
  - Further investigate the control strategy and optimize operation depending on the transmitted power.
  - Investigate the voltage isolation requirements as the converter have a large number of SMs connected in series.
- Chapter 7:

  - Optimize the the circuit inductor values L_o and L. The inductance value of the circuit inductors has an important impact on the converter losses.
  - Further investigate the control strategy and optimize operation depending on the transmitted power.
  - Explore the current control during the faults.

- Chapter 8:
  - Investigate the impact of the low-level converter control, i.e. balancing capacitor algorithm (BCA) on the converter losses.
  - Investigate the internal converter faults and its impact on the sizing.
  - Investigate the controllers that could provide additional ancillary services such as the dc voltage control, droop control.
  - Investigate the control strategies that can provide current control during dc faults.
  - Analyze the relation between the key performance indicators and the costs.
  - Investigate the requirements for the dc-dc converter when interrupted redundancy is allowed in a B line.
  - Further study the different strategies to provide FBC in the dc-dc converters (ACCB, DCCB, FBSMs), their benefits and drawbacks.
  - Study the thermal behavior of the semiconductors during the faults identifying additional requirements such as protective thyristors or parallel connection of diodes.

9.4 List of publications

This section presents the publications related to the specific topics of this thesis the author has contributed to.

Journal papers

Published - Included in the thesis

J1 D. Gómez A., M. Cheah-Mane, J. D. Páez, F. Morel, O. Gomis-Bellmunt and P. Dworakowski, "Dc-MMC for the Interconnection of HVDC Grids With Different Line Topologies," in IEEE Transactions on Power Delivery, vol. 37, no. 3, pp. 1692-1703, June 2022, doi: 10.1109/TPWRD.2021.3095966.

J2 D. Gómez A., K. Shinoda, J. D. Páez, F. Morel, M. Cheah-Mane, O. Gomis-Bellmunt, P. Dworakowski, "Case study of dc-MMC interconnecting two HVDC lines with different grid topologies", in CIGRÉ Science & Engineering - CIGRE Symposium 2021, no. 24 pp. 100-114, Feb. 2022.

Conferences

Published papers - Included in the thesis

C1 D. Gómez A., J. D. Páez, M. Cheah-Mane, J. Maneiro, P. Dworakowski, O. Gomis-Bellmunt, F. Morel, "Requirements for interconnection of HVDC links with DC-DC converters", IECON 2019 - 45th Annual Conference of the IEEE Industrial Electronics Society, Lisbon, Portugal, 2019, pp. 4854-4860, doi: 10.1109/IECON.2019.8927640.

Patent application

P1 Convertisseur de tension DC/DC non-isolé - "DC/DC non-isolated voltage converter", by D. Gómez A., F. Morel, J. D. Páez A., M. Cheah-Mane, O. Gomis-Bellmunt. (2021 April 27). Under evaluation.

Appendix A

State matrix diagonalization

The diagonalization of the state matrix ($\boldsymbol{A}$) is used in linear algebra and control theory to decouple the state variables. The diagonalization of $\boldsymbol{A}$ can give additional information about a system such as its eigenvalues.

The diagonalization requires to organize the system into the canonical form as follows:

$$\dot{\boldsymbol{X}} = \boldsymbol{A}\,\boldsymbol{X} + \boldsymbol{B}\,\boldsymbol{u} + \boldsymbol{K}\,\boldsymbol{V_k}. \tag{A.1}$$

This is the structure used in section 3.6.1. However, for a generalized approach, the matrix $\boldsymbol{K}\,\boldsymbol{V_k}$ can be neglected.

The transformation matrix $\boldsymbol{P}$ is a non-singular square $n \times n$ matrix, which is formed by adjoining columns of eigenvectors of $\boldsymbol{A}$ [128], as follows:

$$\boldsymbol{P} = \begin{bmatrix} \boldsymbol{e_1} & \boldsymbol{e_2} & \cdots & \boldsymbol{e_n} \end{bmatrix}_{n \times n} \tag{A.2}$$

where $\boldsymbol{e_j}$ (with $j \in [1, n]$) are the eigenvectors of $\boldsymbol{A}$, which constitute the n columns of $\boldsymbol{P}$.

The matrix $\boldsymbol{P}$ can be used to change the state variables to a new set of variables $\boldsymbol{X'}$. The relation between $\boldsymbol{X}$ and the new variables $\boldsymbol{X'}$ is:

$$\boldsymbol{X} = \boldsymbol{P}\,\boldsymbol{X'} \tag{A.3}$$

Replacing (A.3) in (A.1), the following expression is obtained:

$$\boldsymbol{P}\,\dot{\boldsymbol{X}}' = \boldsymbol{A}\,\boldsymbol{P}\,\boldsymbol{X'} + \boldsymbol{B}\,\boldsymbol{u} + \boldsymbol{K}\,\boldsymbol{V_k}. \tag{A.4}$$

Since $\boldsymbol{P}$ is non-singular matrix, (A.4) can be rearranged to have the canonical form (A.1), as follows:

$$\dot{\boldsymbol{X}}' = \boldsymbol{P}^{-1}\boldsymbol{A}\,\boldsymbol{P}\,\boldsymbol{X'} + \boldsymbol{P}^{-1}\boldsymbol{B}\,\boldsymbol{u} + \boldsymbol{P}^{-1}\boldsymbol{K}\,\boldsymbol{V_k} \tag{A.5}$$

where $\boldsymbol{P}^{-1}\boldsymbol{A}\,\boldsymbol{P}$ is a diagonal matrix $\boldsymbol{A_D}$ and the rest of the system is usually not diagonal. The new system can be expressed as:

$$\boldsymbol{X'} = \boldsymbol{A_D}\,\boldsymbol{X'} + \boldsymbol{B'}\,\boldsymbol{u} + \boldsymbol{K'}\,\boldsymbol{V_k} \tag{A.6}$$

where $\boldsymbol{B'}$ and $\boldsymbol{K'}$ are the not diagonal input and constant matrices.

Appendix B

Front-to-Front simulation results

The Front-to-Front MMC (F2F-MMC) presented in Chapter 5 is simulated to test its behavior for the interconnection proposed in Chapter 4, i.e., interconnecting a bipole and a SyM. The converter model and its control are implemented in Matlab-Simulink environment for the different cases proposed in Chapter 4. The detailed results of the converter, presented below, shows that the F2F-MMC is controlled during the proposed simulations.

B.1 Nominal Operation

To test the control strategy, a first simulation is performed testing the nominal operation of the F2F-MMC, i.e. F2F exchanging 700 MW in both directions. From the steady-state analysis presented in Section 5.3, the arm voltages and currents are calculated analytically and presented in Table B.1.

The power exchanged by the three MMCs in the F2F are presented in Fig. B.1, for the nominal operation. The MMCs on the bipole side, exchange half of the total power through the MMC connected to the SyM. The converter starts sending power to the SyM at 2.4 s and around 3.6 s the power starts to change direction to send 700 MW to the bipole line (negative power through the F2F-MMC).

The power per converter station is presented in Fig. B.2. At 1.4 s the bipole line starts sending 700 MW from the voltage-controlled station to the power-controlled terminal (positive convention). The SyM line is operating but it does not exchange power (red lines in Fig. B.2). At 2.4 s the F2F-MMC starts exchanging power from the bipole to the SyM (positive convention). The power in the power-controlled stations remains unchanged (dashed lines), while the voltage-controlled stations change their operating points to balance the system depending on the power exchanged through the F2F-MMC. When the F2F-MMC exchanges power from the bipole line to the SyM, the terminal in voltage control of the

Table B.1: Steady-state currents and voltages per arm for the considered F2F-MMC.

	MMC B		MMC SyM	
	Arm_u	Arm_l	Arm_u	Arm_l
I_{arm}^{dc}	222 A		365 A	
I_{arm}^{ac}	635 A		911.5 A	
$\theta_{I_{arm}^{ac}}$	π	0	π	0
V_{arm}^{dc}	262.5 kV		320 kV	
V_{arm}^{ac}	183.8 kV		256 kV	
$\theta_{I_{arm}^{ac}}$	0	π	0	π

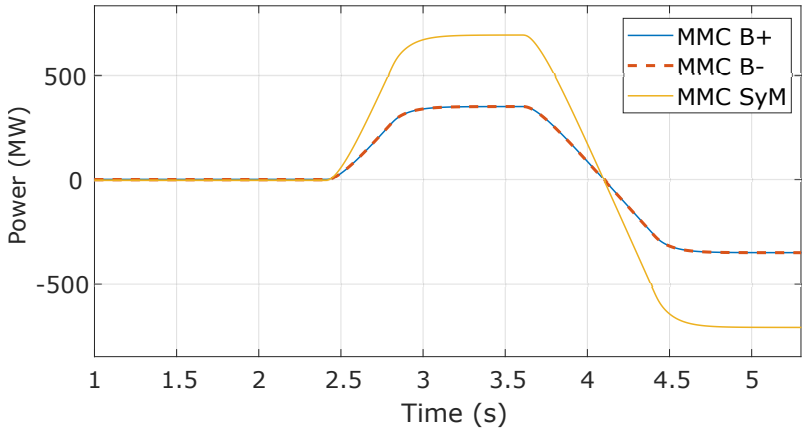


Figure B.1: Power per MMC in the F2F.

bipole supplies the additional power. On the SyM line, the voltage-controlled station absorbs the exchanged power. At 3.6 s the power through the F2F-MMC is reversed changing the power flow direction. On the bipole line, the power from the power-controlled station feeds the dc-dc converter thus, the voltage-controlled station does not exchange power. On the SyM the voltage-controlled station adjusts its operation to provide the power requested by the F2F-MMC.

The pole-to-ground dc voltages measured at the terminals of the F2F are presented in Fig B.3. The dc voltages are controlled by the ac-dc stations on each line. The voltage-controlled stations set the nominal voltage at their terminals, the rest of the system has a slightly different

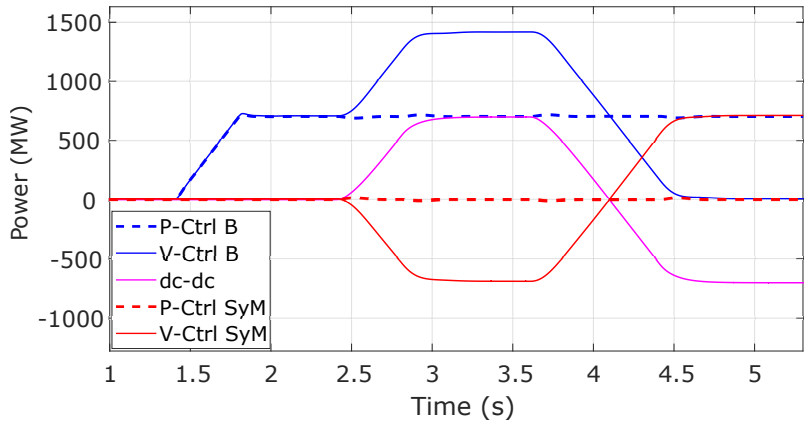


Figure B.2: Power per converter station of the interconnected system.

value above or below, depending on the magnitude and direction of the power flow in the system. Depending on the dc current, the line has a different voltage drop, which changes the energy reference in the ac-dc converters due to the virtual capacitor controller [137], i.e. the dc voltage do not follow a constant reference it changes depending on the voltage in the dc line.

The voltage in the lines has small dynamic variations (less than 4%) depending on the variations of power exchanges in the system (see Fig. B.2). When the bipole line starts exchanging power at 1.4 s, the voltage in the bipole line decreases reaching a steady-state around 2.2 s. At 2.4 s, when the F2F-MMC starts exchanging power, both lines have voltage disturbances reaching steady-state conditions around 3.4 s. When the F2F-MMC changes the power flow direction the voltages are disturbed again reaching steady-state around 5 s. It can be noticed that the dc voltage steady state at the terminals of the F2F-MMC is not always 1 p.u., the dc-dc converter sees the voltage difference needed to allow the power flow in the system. A particular operating point is achieved at the end of the simulation ($t > 5$ s), where the voltage measured on the bipole side is exactly 1 p.u., this is caused by the power balance between the power-controlled station and the dc-dc converter. As the voltage-controlled station do not exchange power, the voltage at its terminals is equal to the voltage at the terminals of the F2F-MMC. The voltage dynamic variations and steady-state values do not exceed $\pm 5\%$, which is an acceptable steady-state variation.

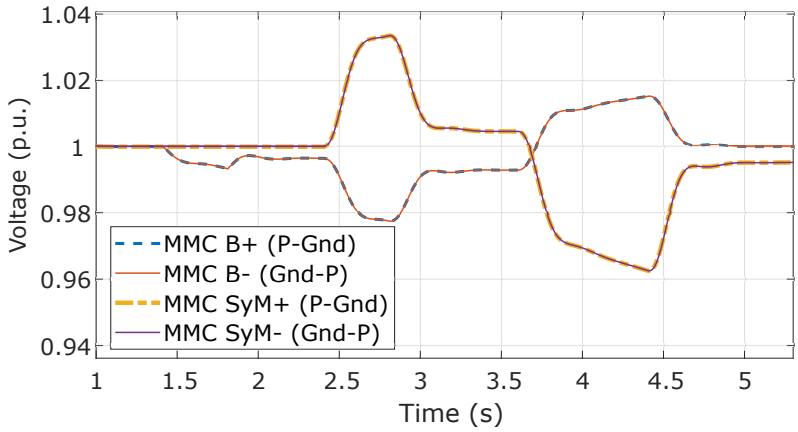


Figure B.3: Dc voltage per MMC in the F2F. The negative poles are inverted to be compared with the positive pole-to-ground voltages.

The detailed converter results are presented below. The arm voltages for the upper and lower arm, of phase A, are presented in Fig. B.4. As analyzed in Section 5.3 the arm dc voltage is approximately half of the pole-to-pole dc voltage (yellow line), 262.5 kV in Fig. B.4a-b, and 320 kV in Fig. B.4c. Depending on the power through the F2F-MMC, the arm dc voltage has small variations following the dc voltage variations (see Fig B.3). The ac voltages also follow the ac steady-state analysis presented in Table B.1 in magnitude and phases.

Similar to the arm voltages, the arm currents are presented in Fig. B.5. The arm dc current is proportional to the active power exchanged between the interconnected lines. The arm ac current follows the analytical results presented in Table B.1. Following the positive convention for the currents measured in the MMCs, i.e. from dc to ac side, the dc currents on the bipole side have the opposite sign that the dc current on the SyM side. The currents are controlled during the complete simulation.

The voltage of the equivalent capacitance $V_{C_{eq}}$, of the average arm model, is presented in Fig. B.6. The results confirm that $V_{C_{eq}}$ has a $\pm 10\%$ ripple at nominal power. The ripple depends on the transmitted power, it can be seen that when the power is zero, i.e. $t < 2.4$ s or $t \approx 4.1$ s, the voltage ripple is minimum. The average voltage of the equivalent arm capacitor is used in the energy control. It can be evidenced that this average value is controlled during the complete simulation.

B.2 Case 3 Normal operation

The detailed F2F-MMC results for the normal operation for Case 3 of Table 4.4 are presented in Fig. B.7, B.8, and B.9. The results are similar to those presented in Chapter 5 for the nominal operation, the difference is the magnitude of the oscillations and dc values, which are adjusted to the transferred dc power.

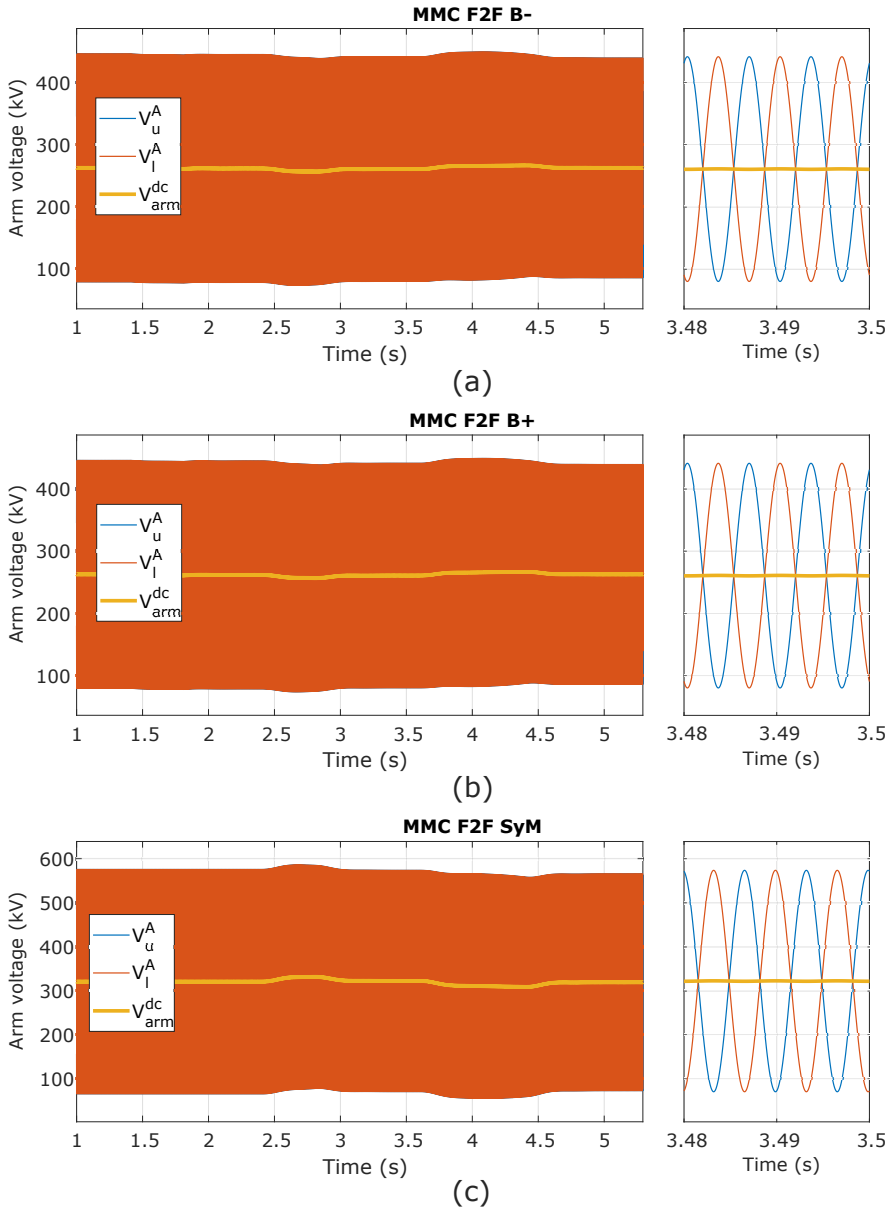


Figure B.4: Arm voltages for the upper and lower arm on phase A. (a) MMC connected to the negative pole of the B, (b) MMC connected to the positive pole of the B and (c) MMC connected to the SyM.

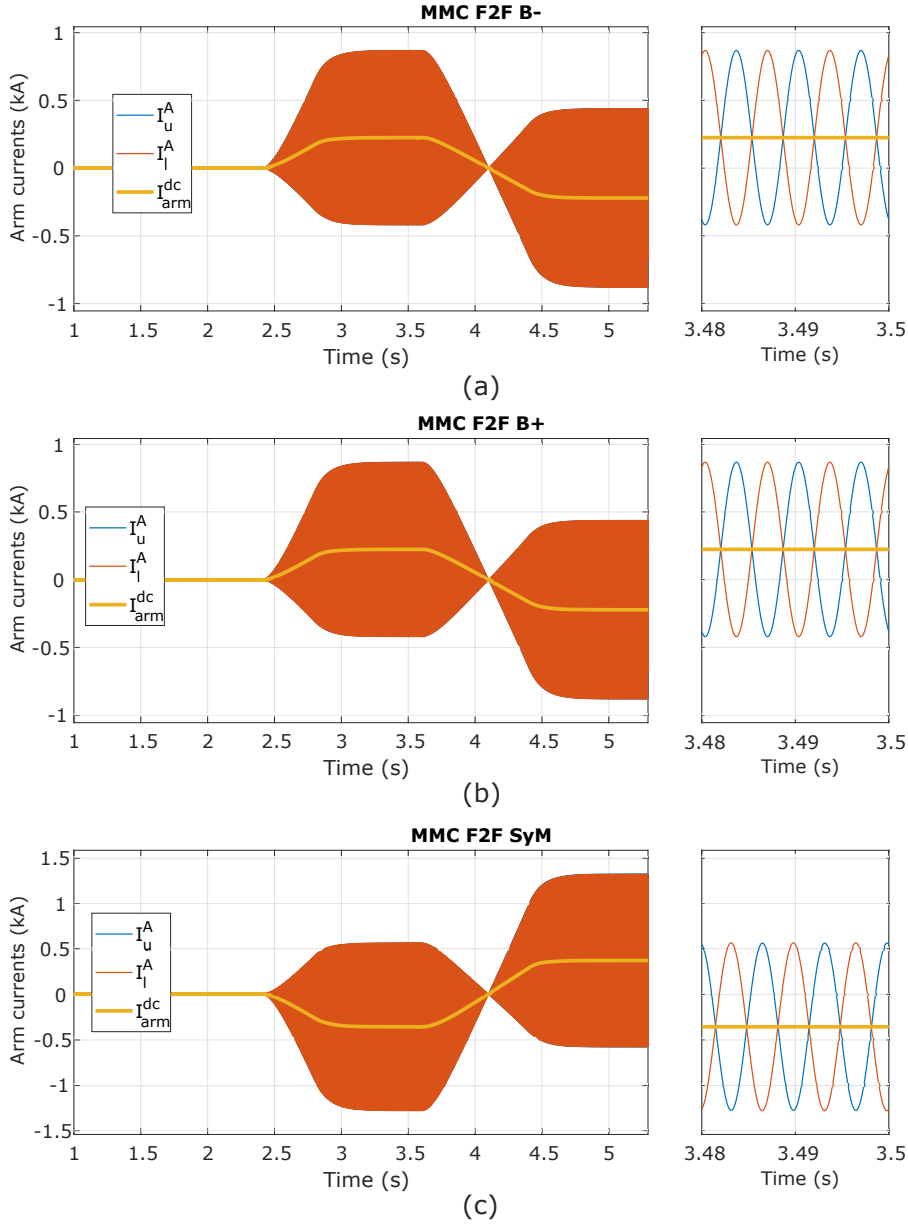


Figure B.5: Arm currents for the upper and lower arm on phase A. (a) MMC connected to the negative pole of the B, (b) MMC connected to the positive pole of the B, and (c) MMC connected to the SyM.

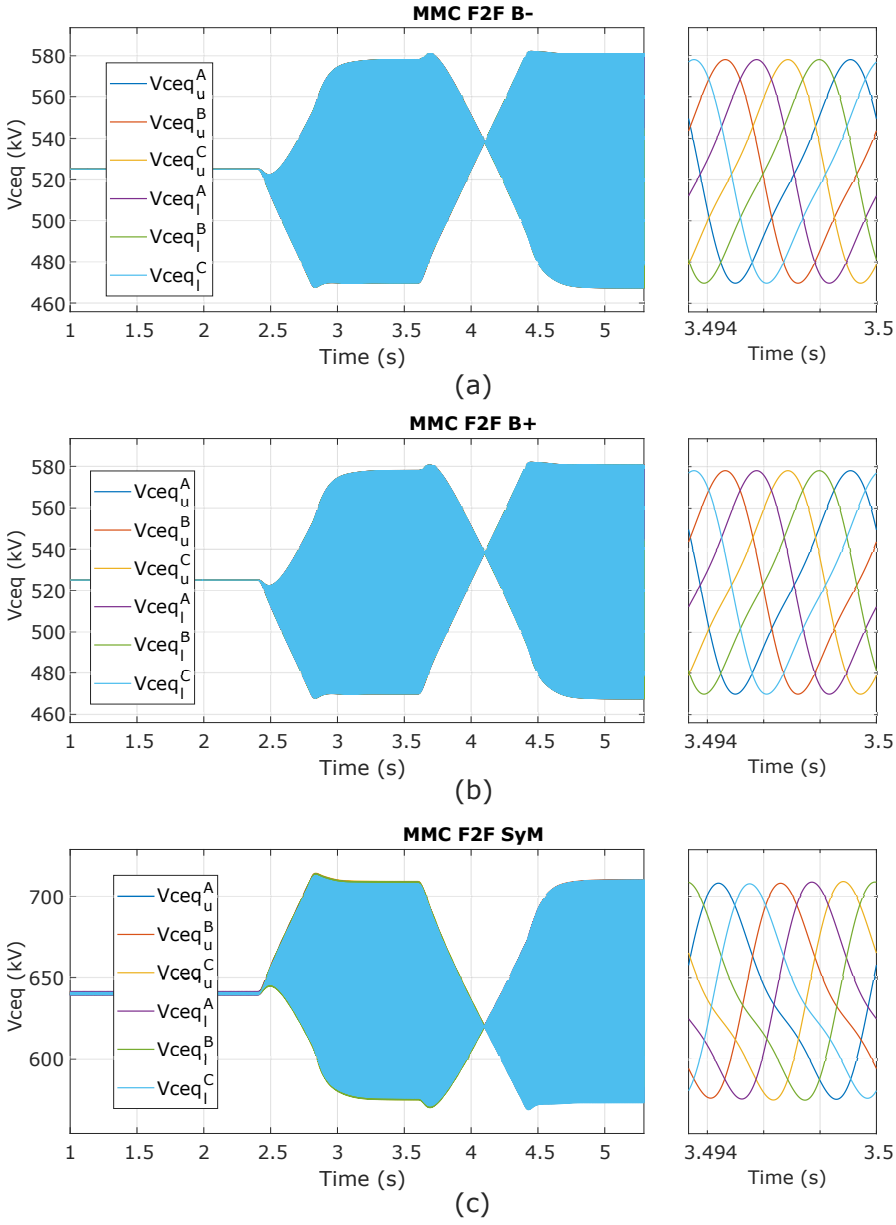


Figure B.6: Voltage of the equivalent arm capacitor (V_{Ceq}) on the three phases. (a) MMC connected to the negative pole of the B, (b) MMC connected to the positive pole of the B (b), and (c) MMC connected to the SyM.

B.3 F2F with Full Bridge Sub-Modules

Case 1 of Table 4.5 when the fault is on the bipole line was simulated to test the behavior of the F2F-MMC with FBSMs instead of ACCBs.

According to [150, 151] the minimum number of FBSMs to stop the faults for a positive modulation is 50% of the total installed SMs. Using the total number of SMs calculated in (5.24), the number of FBSMs needed to stop the fault currents is 165. Case 1 was simulated removing the ACCBs and replacing half of the HBSMs by FBSMs. The system results are presented in Fig. B.10.

The power per converter station is presented in Fig. B.10a. Compared to the results found using ACCBs, presented in Fig. 5.16, the results using FBSMs have smaller power disturbances in the voltage-controlled station on the bipole, the dc-dc converter and the stations on the SyM line. An important difference is that the power on the F2F-MMC does not change of sign, i.e., the FBSMs avoid feeding the fault on the bipole side.

The dc voltages measured at the terminals of the F2F-MMC (Fig. B.10b), do not have a significant change compared to the results with ACCBs. The energy per converter station, presented in Fig. B.10c, show a similar behavior to the energy variations presented in Fig. 5.16c.

The detailed converter results are presented in Fig. B.11. Compared to the results presented in Fig. 5.17, the results with FBSMs reduce considerably the current transient. The ac currents are presented in the first row of Fig. B.11. The converter connected to the positive pole of the bipole (the faulted pole), blocks the ac currents reducing the fault current. The current disturbances stop after opening the ACCBs on the ac-dc converters of the faulted pole of the bipole, i.e., 100 ms after the fault detection. The ac currents of the healthy MMCs in the F2F have a reduced disturbance compared to the results presented in Fig. 5.17.

The arm currents for the MMCs in the F2F using FBSMs are presented in Fig. B.11d, e, and f. As the MMC using FBSMs has blocked the ac currents, the currents in the arms have less rectified currents compared to the results presented for the F2F-MMC with ACCBs. The arm currents on the healthy MMCs have lower disturbances.

The voltages at the terminals of the arms are presented in the third row of Fig. B.11. As the F2F-MMC does not have ACCBs isolating the faulted pole, when the MMC is blocked, the arms are subject to an oscillating voltage that is blocked by the FBSMs. For the MMCs in F2F connected to the healthy zones, the arm voltages have small disturbances reducing the impact on the healthy zones.

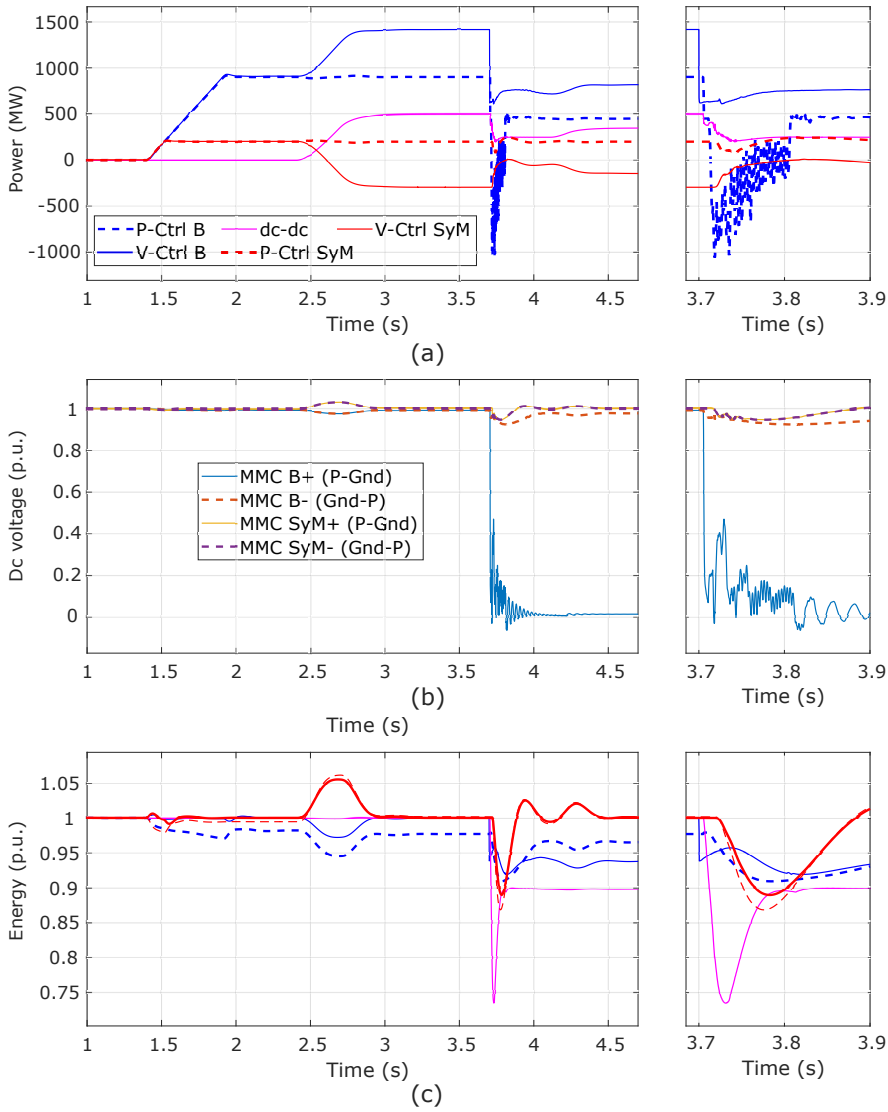


Figure B.10: Results for the Case 1 when the fault is on the bipole line (see Table 4.5) with FBSMs instead of ACCBs. The power per converter station (a). The dc voltage at the terminals of the MMCs of the F2F (b). The energy per converter station (c).

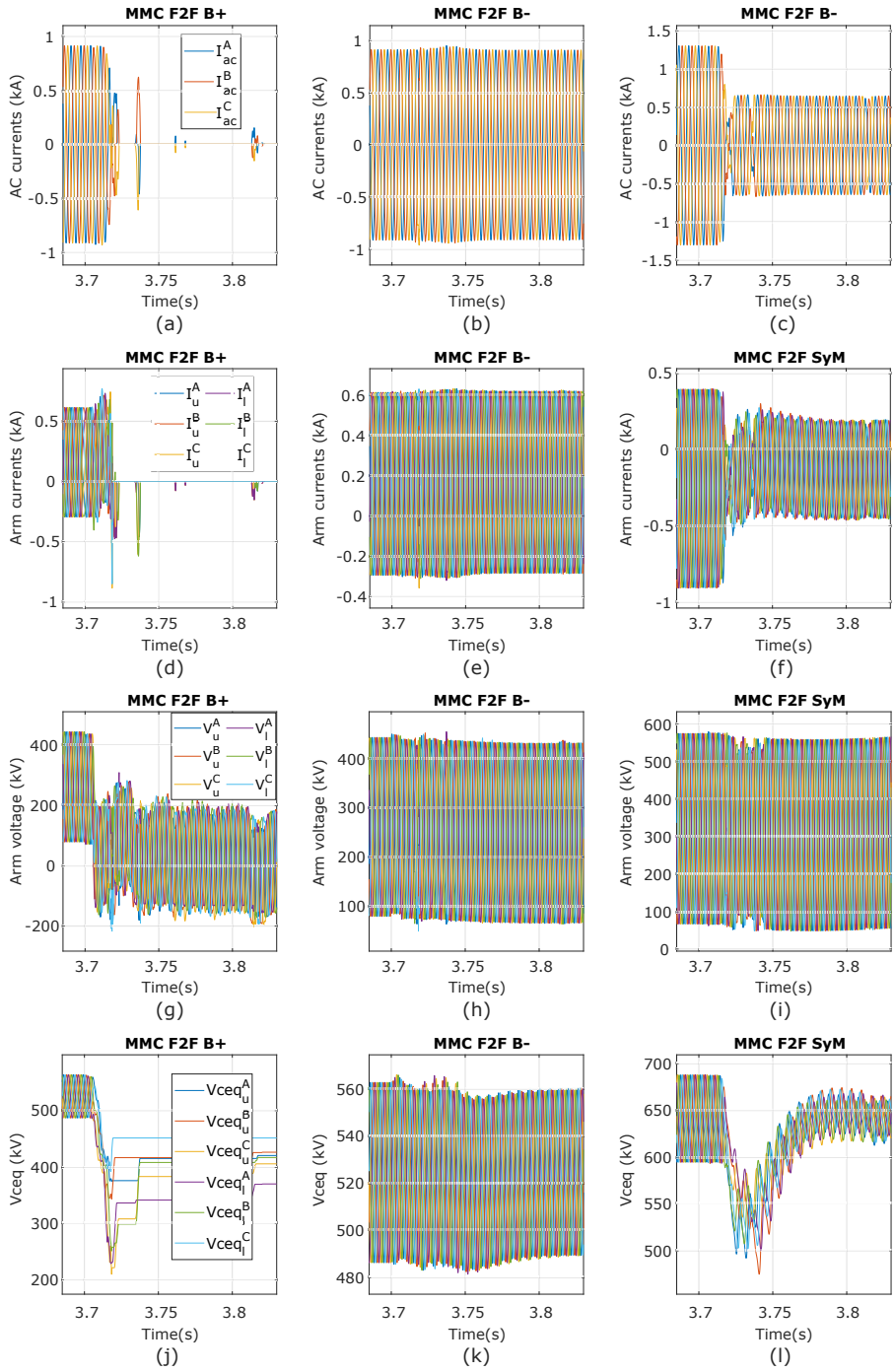


Figure B.11: Ac currents (first row), arm currents (second row), arm voltages (third row), and the voltage of the equivalent arm capacitor for the three MMCs in the F2F for the Case 1 when the fault is on the bipole line (see Table 4.5) ans FBSMs are used instead of ACCBs.

The voltages in the arm equivalent capacitance are presented in the fourth row of Fig. B.11. Similar to the previous results, the disturbances in these voltages are reduced compared to the results presented in Fig. 5.17.

In general, the results of the F2F-MMC using FBSMs to stop the faults show that the fast blocking of the converter can reduce the magnitudes of the disturbances in the healthy zones. The results suggest that the controller could have less efforts in recovering the steady-state conditions in the healthy zones.

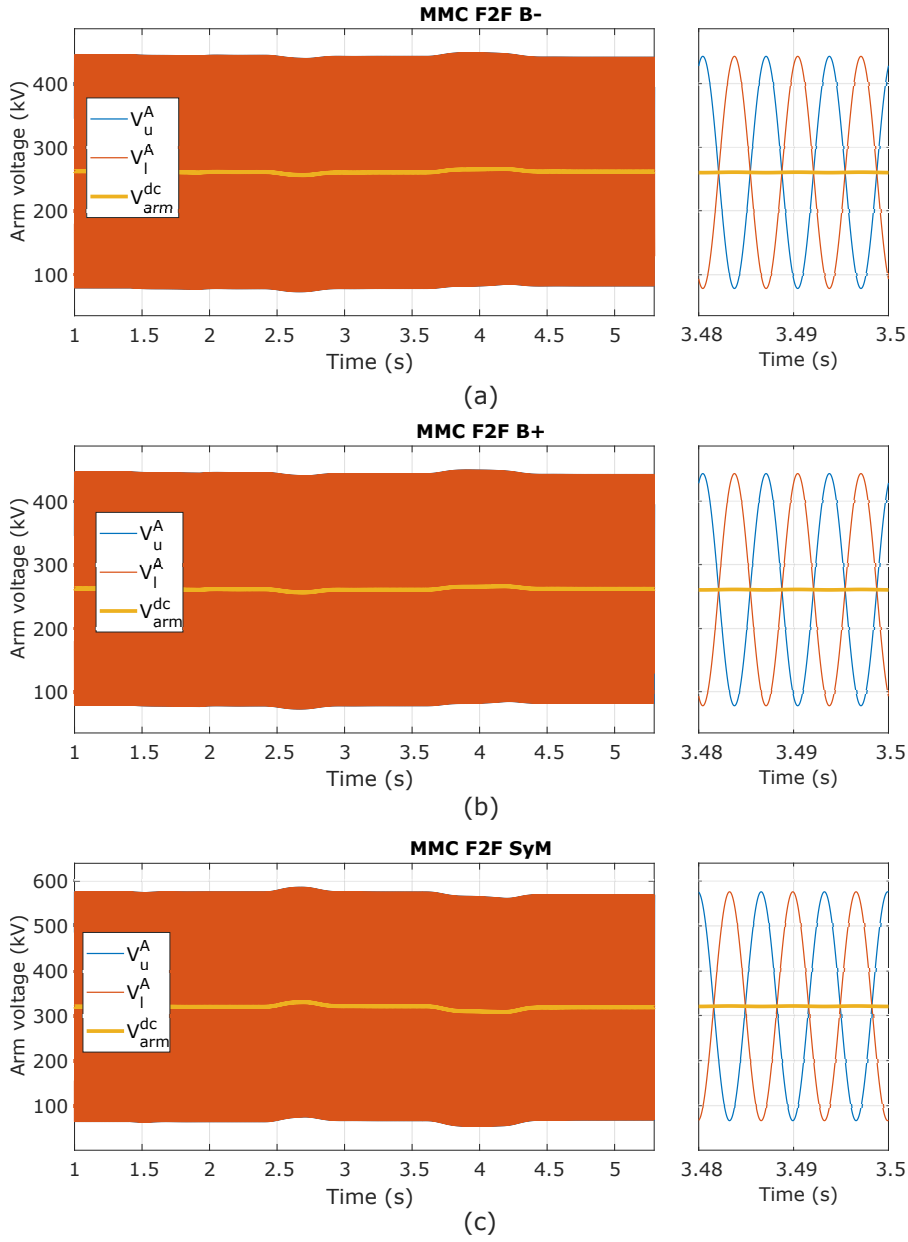


Figure B.7: Arm voltages for the upper and lower arm for Case 3 of Table 4.4. Only the phase A is presented for the MMC connected to the negative pole of the bipole (a), the MMC connected to the positive pole of the bipole (b), and the MMC connected to the SyM (c).

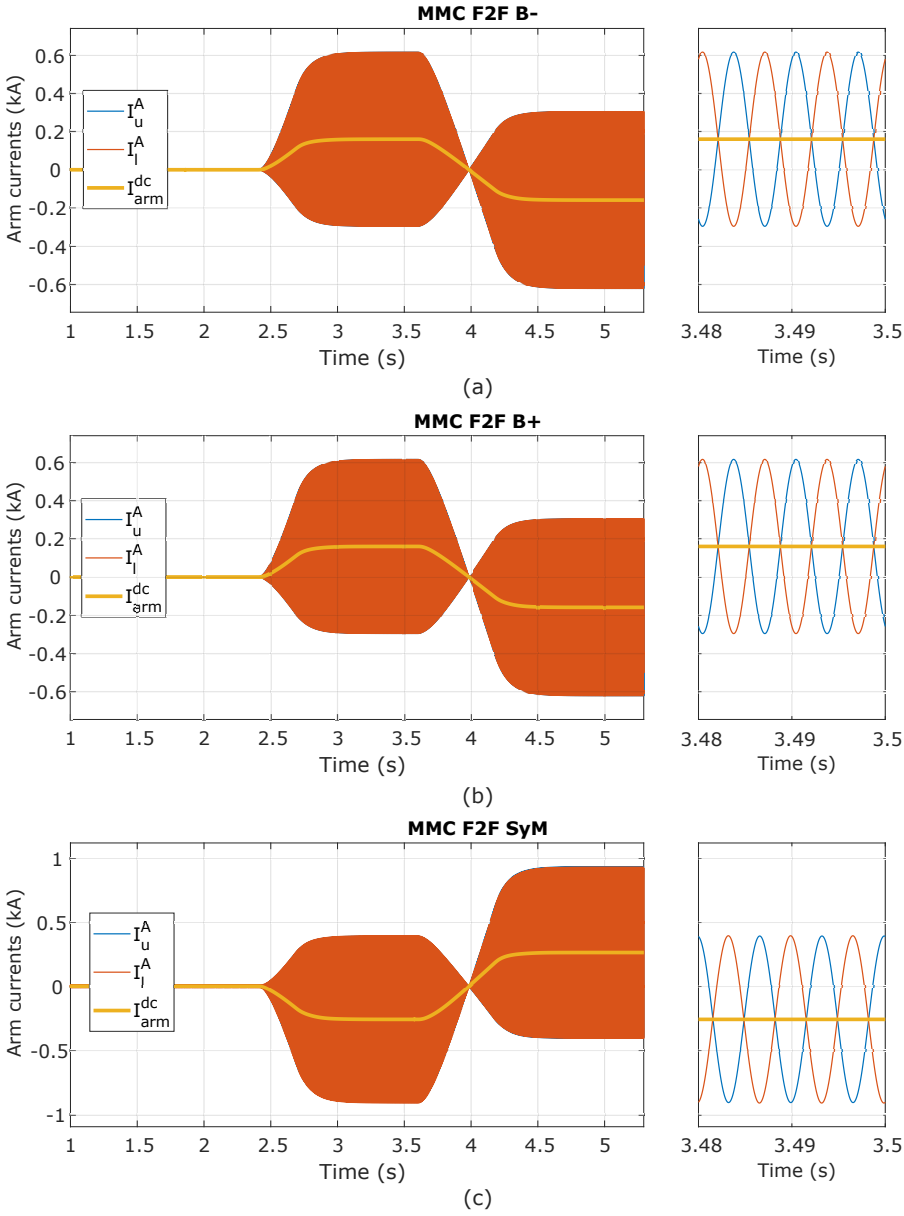


Figure B.8: Arm currents for the upper and lower arm for Case 3 of Table 4.4. Only the phase A is presented for the MMC connected to the negative pole of the bipole (a), the MMC connected to the positive pole of the bipole (b), and the MMC connected to the SyM (c).

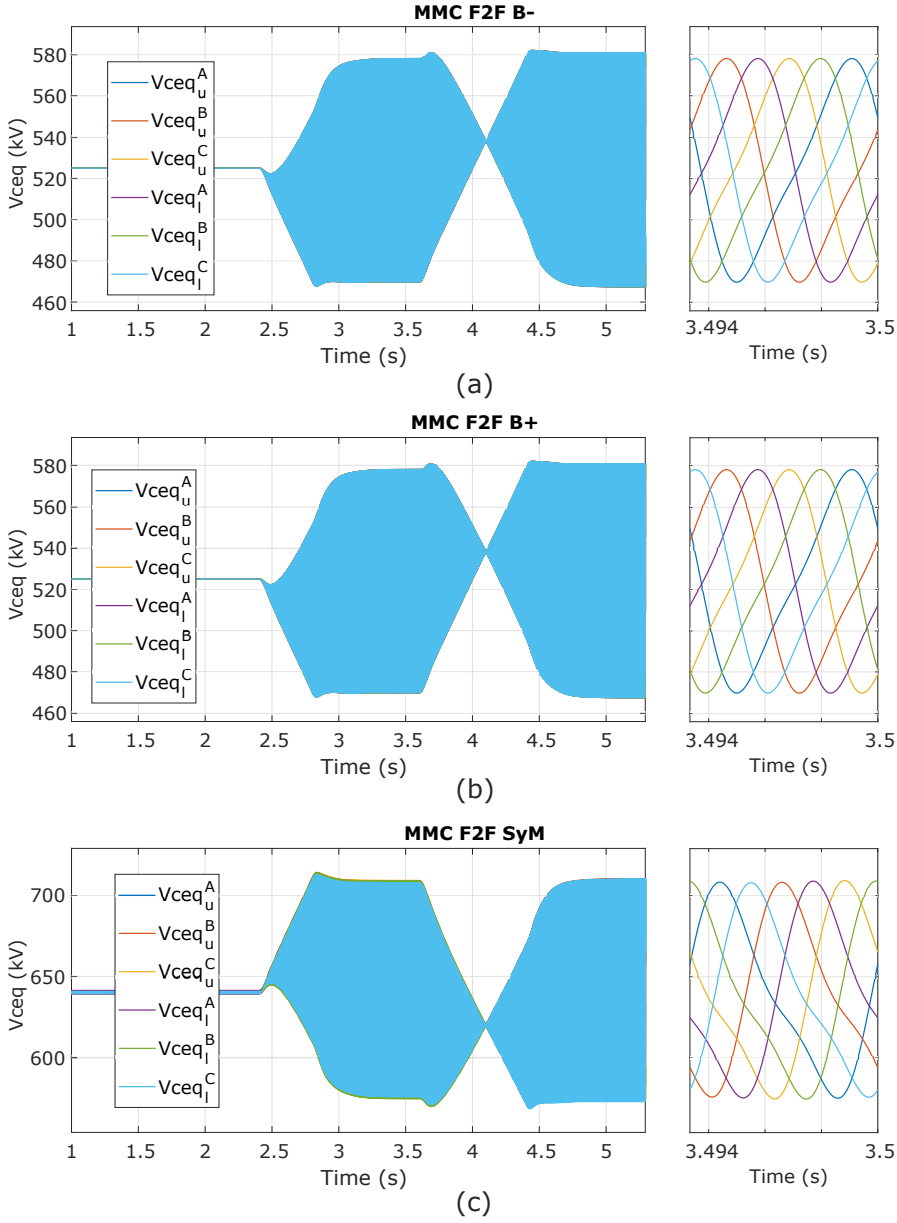


Figure B.9: Voltage of the equivalent arm capacitor ($V_{C_{eq}}$) for the upper and lower arm for the Case 3 of Table 4.4. The three phases are shown for the MMC connected to the negative pole of the bipole (a), the MMC connected to the positive pole of the bipole (b), and the MMC connected to the SyM (c).

Appendix C

Flexible dc-MMC additional results

C.1 Optimization results

From the optimization results presented in Chapter 6, the steady-state results for the degraded modes are presented in this appendix.

C.2 Flexible dc modular multi-level converter results

Table C.1: Steady-state solution for the degraded operation of the flexible dc-MMC after a fault on the positive pole of the bipole.

Arm	V^{dc} (kV)	I^{dc} (kA)	V^{ac} (kV)	I^{ac} (kA)
Upper	-320	0.222	$276\angle 145°$	$0.68\angle -173°$
Middle	640	0.04	$417\angle 0°$	$1.09\angle 96.4°$
Lower	205	0.222	$238\angle -144°$	$0.44\angle 6.4°$

Table C.2: Steady-state solution for the degraded operation of the flexible dc-MMC after a fault on the positive pole of the bipole.

Arm	V^{dc} (kV)	I^{dc} (kA)	V^{ac} (kV)	I^{ac} (kA)
Upper	205	0.222	$238\angle -144°$	$0.44\angle -6.4°$
Middle	640	0.04	$417\angle 0°$	$1.09\angle 96.4°$
Lower	-320	0.222	$276\angle 145°$	$0.68\angle -173°$

C.3 Simulation results

C.3.1 Nominal operation

The control strategy designed in Section 6.5 is tested with a simulation of the flexible dc-MMC operating at nominal power, i.e. exchanging 700 MW in both directions.

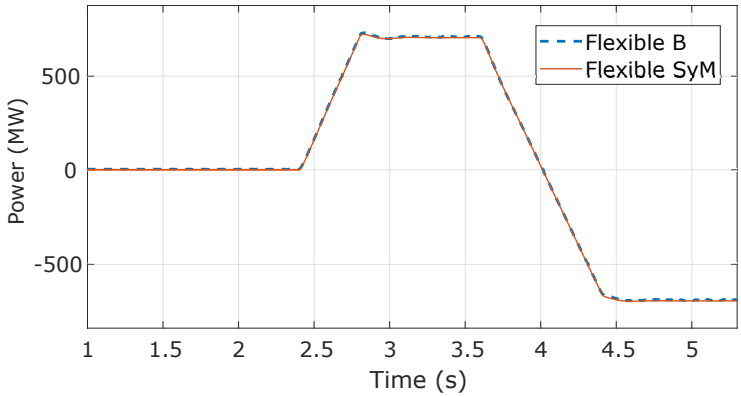


Figure C.1: Input power from the bipole and output power to the SyM, through the flexible dc-MMC in nominal operation.

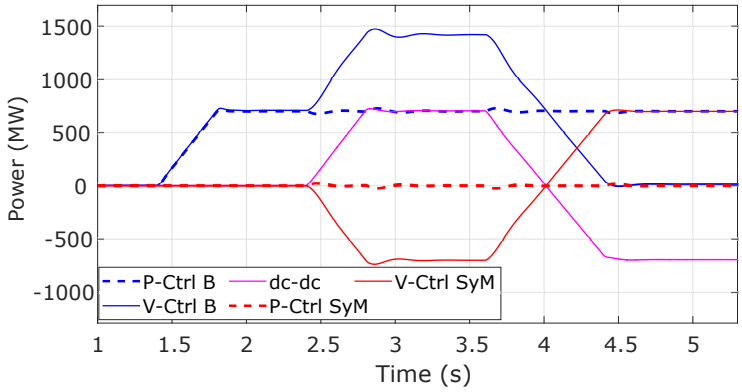


Figure C.2: Power per converter station when the flexible dc-MMC exchanges nominal power between the lines.

The power exchanged through the flexible dc-MMC is presented in Fig. C.1. The input power (dashed line) and the output power (continuous line) are almost identical. The flexible dc-MMC starts exchanging

power from the bipole to the SyM (positive convention) at 2.4 s, and around 3.6 s, the power through the dc-dc converter is inverted to feed the bipole line.

The power per converter station is presented in Fig. C.2. The bipole starts sending 700 MW, at 1.4 s, from the voltage-controlled station to the power-controlled station. At 2.4 s, the flexible dc-MMC starts exchanging power as presented in Fig. C.1. The voltage-controlled stations adapt their exchanged power to follow the voltage reference. When the power in the flexible dc-MMC is positive, the voltage-controlled station on the bipole supplies the power demanded by the dc-dc converter and the power-controlled station on that line. On the SyM, the voltage-controlled station, exports the power from the dc-dc converter to the ac system. When the power through the dc-dc converter is reversed, the behavior of the voltage-controlled stations on the lines changes accordingly. On the bipole line, the power from the dc-dc converter supplies the power-controlled station, therefore, the power exchanged through the voltage-controlled station is minimal (the necessary to keep the dc voltage reference). On the SyM, the voltage-controlled station changes the power direction, now feeding the dc-dc converter.

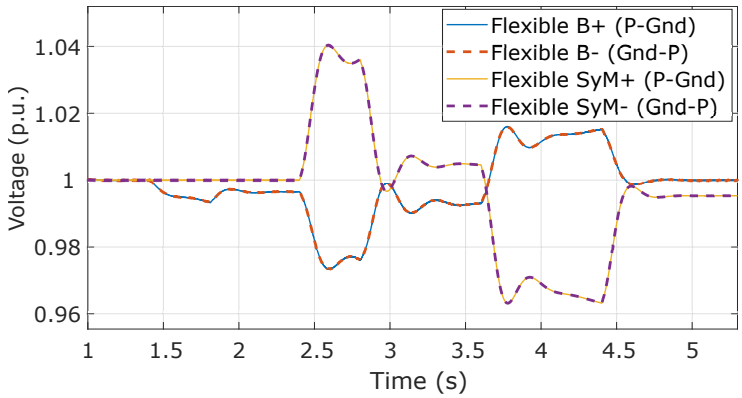


Figure C.3: Dc voltage at the terminals of the flexible dc-MMC in nominal operation. The pole-to-ground voltages are presented for the positive poles, while the ground-to pole voltages are presented for the negative poles.

The dc voltages measured at the terminals of the dc-dc converter are presented in Fig. C.3. Durling the changes in the power reference, the dc voltage dynamic variations respect the nominal operation of both lines, i.e. the dc voltage does not exceed the $\pm 5\%$ of its nominal value.

The difference between the dc measured voltage, and its nominal value, depends on the voltage drop in the cable from the voltage-controlled station to the measuring point.

The arm voltages are presented in Fig. C.4. The simulation results confirm the steady-state analysis of Sections 6.3.1 and 6.3.3. The arm dc voltages follow the approximated values found in (6.20) and the ac components follow the magnitudes and phase shifts presented in Table 6.2. The upper and lower arms present a small negative ac voltage, which is possible thanks to the FBSMs installed in those arms. During the simulation, the dc voltage in the arms have small variations to adjust the dc currents through the flexible dc-MMC.

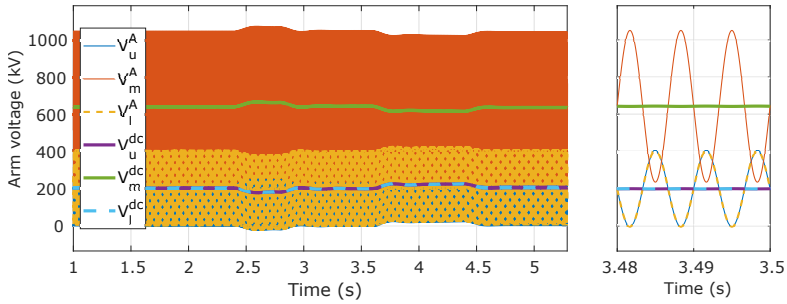


Figure C.4: Arm voltages per arm of the flexible dc-MMC in nominal operation. Only the phase A is presented.

The arm currents, presented in Fig. C.5, are controlled during the complete nominal operation. The dc currents change polarity depending on the power flow direction. The phase shift is also changed depending on the power flow direction to keep the balance of the energy in the converter. Similar to the ac voltages, the ac currents follow the magnitudes and phases presented in Table 6.2.

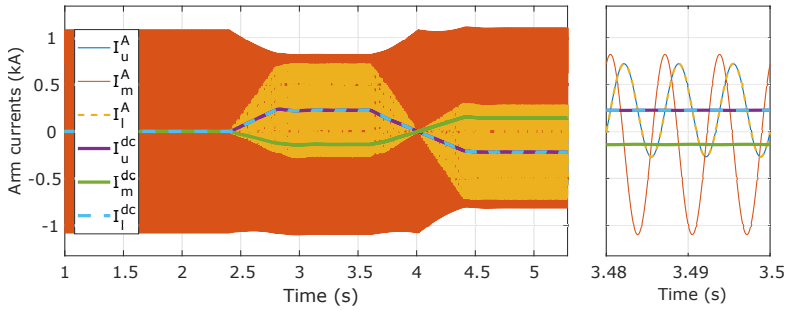


Figure C.5: Arm currents per arm of the flexible dc-MMC in nominal operation. Only the phase A is presented.

The voltage of the equivalent arm capacitance is presented in Fig. C.6. The voltage ripple respects the design of ±10% of the operating voltage. The voltage of the arm equivalent capacitor is related to the energy stored in the capacitors of the SMs. It can be evidenced that the energy is controlled during the different power exchanges as the voltages come back to their nominal value. At around 4 s, the upper and lower arms follow a change of phase, while the middle arm does not. This is because the main component of I_m^{ac}, which is I_3^{ac}, is fixed (see Table 6.4), while I_u^{ac} and I_l^{ac} are controlled and change with the operating point.

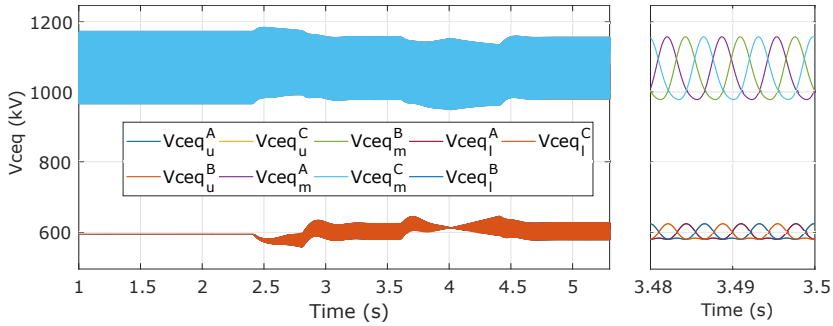


Figure C.6: Voltage of the equivalent arm capacitance in nominal operation of the flexible dc-MMC.

Appendix D

Asymmetric DC Converter simulation results

The asymmetric dc converter (ADCC), presented in Chapter 7, is simulated to test its behavior during the different cases presented in Table 4.4 and Table 4.5. The simulation model is implemented in Matlab-Simulink environment.

D.0.1 Nominal operation

A first simulation is made to verify the sizing of the ADCC. The converter is simulated operating at its nominal power, i.e. exchanging 700 MW. The power exchanged trough the ADCCs is presented in Fig. D.1. It can be noticed that each ADCC exchanges 350 MW between the interconnected dc systems. On the SyM side, an equivalent of 700 MW is exchanged.

The power per converter station is presented in Fig. D.2. The power-controlled stations (dashed lines) keep their power constant during the different power changes in the system. In contrast, the voltage-controlled stations change their power depending on the power through the dc-dc converter. The stations in voltage control mode adapt their power to keep the voltage stable in the lines. The power-controlled station in the SyM line has a power reference null to allow the voltage-controlled station to exchange its nominal power with the ADCCs.

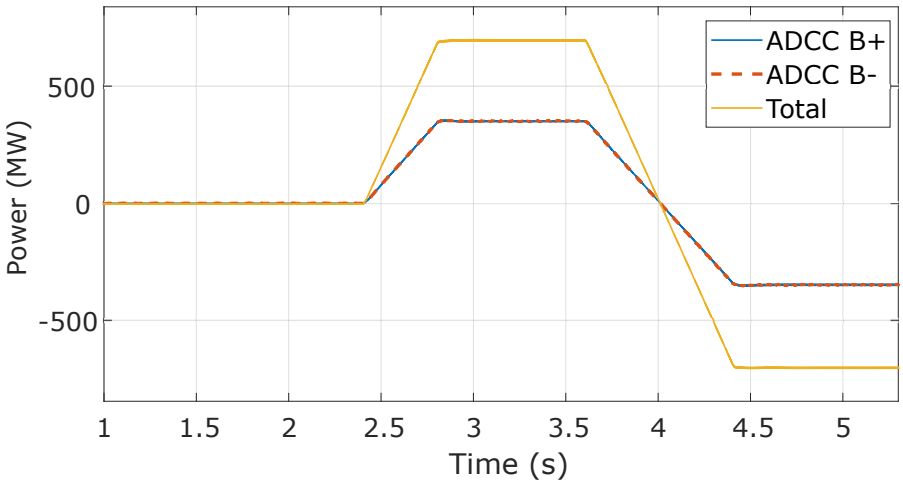


Figure D.1: Power transfer from the bipole to the SyM, through the ADCCs.

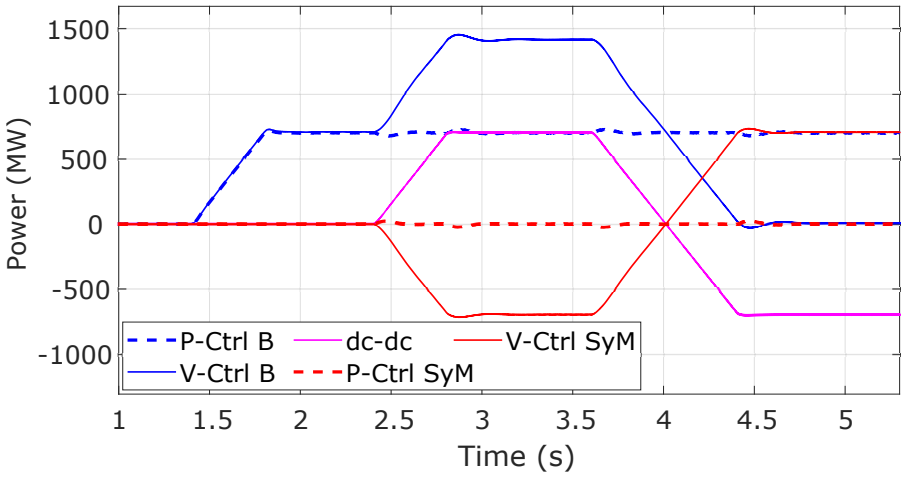


Figure D.2: Power per converter station when the ADCC exchanges nominal power (700 MW) between the bipole and SyM lines.

The dc voltages measured at the terminals of the ADCCs are presented in Fig. D.3. The dc voltages in the lines are disturbed during every power variation. It can be noticed that the steady-state dc voltage might be different form its nominal value because of the virtual capacitor controller implemented in the ac-dc converters [137] and the voltage drop in the line. During the different voltage dynamic variations, the nominal operation limits are not exceeded, i.e. $\pm 5\%$ of its nominal value.

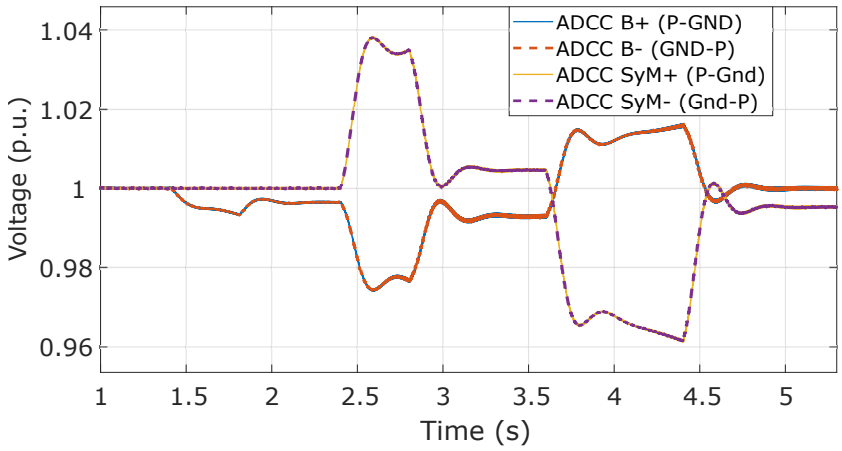


Figure D.3: Average dc voltages at the terminal of the ADCCs. Pole-to-ground on the bipole side and pole-to-pole on the SyM.

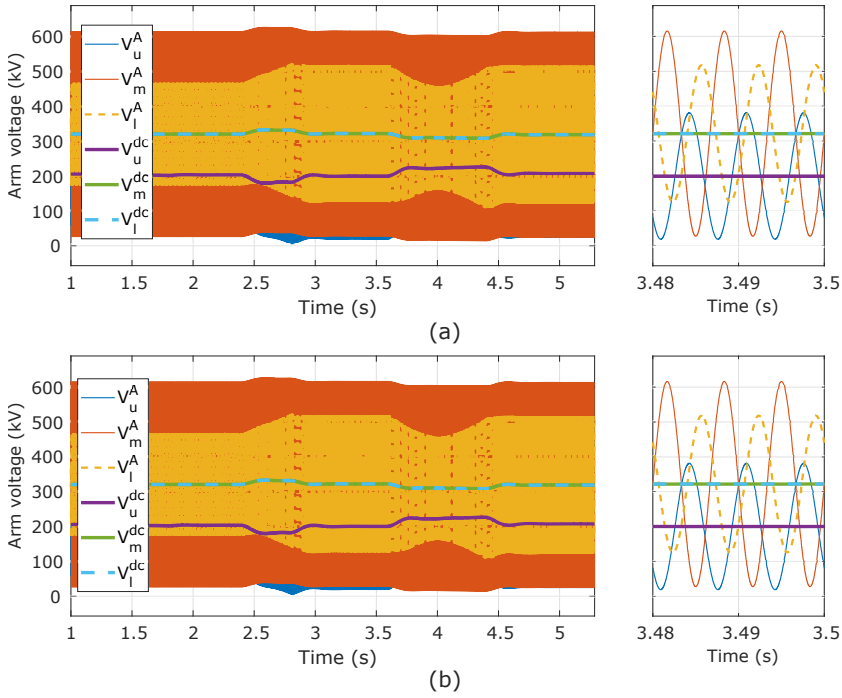


Figure D.4: Arm voltages in the ADCC. (a) connected to the positive pole of the bipole, and (b) connected to the negative pole of the bipole.

The arm voltages are presented in Fig. D.4. The results follow the polarity presented in Fig. 7.2. The results show that the ac voltage magnitudes and phases reach the operating conditions found in Table 7.2, and the dc voltages correspond to the values found in (7.22). The dc arm voltages have small dynamic variations depending on the different power references changes but, they remain controlled during the complete simulation.

The arm currents are presented in Fig. D.5. The dc and ac current components respect the estimations presented in (7.7)-(7.9), and Table 7.2. The magnitude of the upper and lower arms are controlled and depend on the exchanged power. On the other hand, the middle arm current have smaller dynamic variations compared to the currents in the other arms as the middle arm currents are mainly set by the I_3^{ac} which is fixed by the control strategy independent from the transmitted power (see Table 7.4).

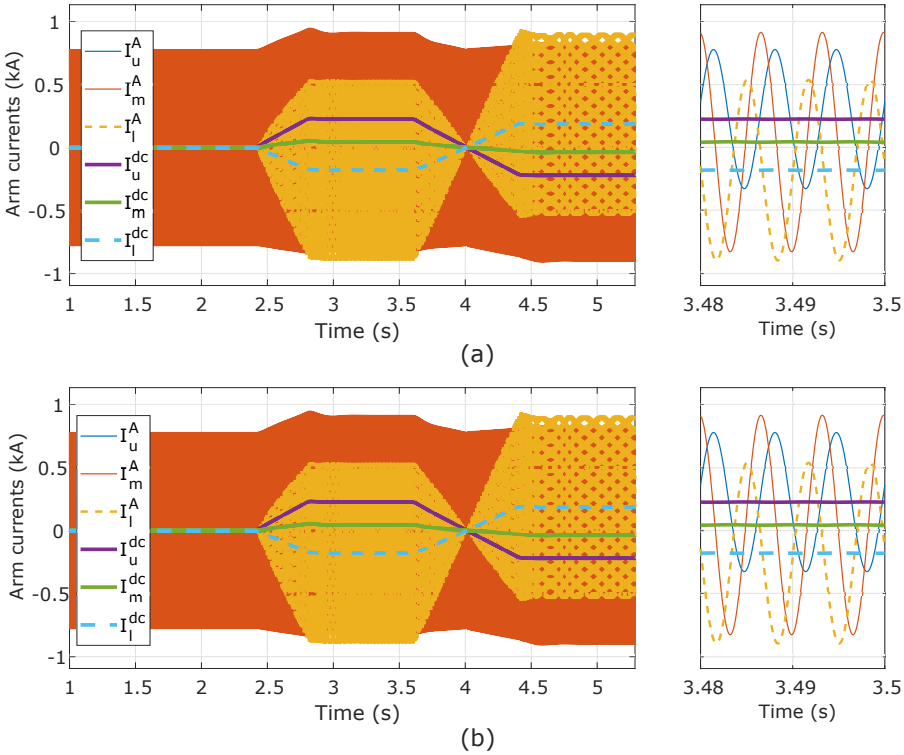


Figure D.5: Arm currents in the ADCC. (a) connected to the positive pole of the bipole, and (b) connected to the negative pole of the bipole.

The voltage of the equivalent arm capacitance is presented in Fig. D.6. The ripple respects the ±10% of the nominal arm voltage, defined for the capacitor sizing in Section 7.4.2. The nominal voltage per arm is $V_{nom_u} = 526.4\,kV$, $V_{nom_l} = 640\,kV$, and $V_{nom_u} = 542.4\,kV$. The voltage in the capacitors have dynamic variations depending on the power reference but, they are controlled during the complete converter operation. The upper and lower arms presents a variation in amplitude and phase depending on the power transfer, while the middle arm does not, as the middle arm current is mainly defined by I_3^{ac}.

The simulation in nominal operation has verified that the converter steady-state conditions calculated in Section 7.4.1 are reached by the control strategy proposed. The design criteria, i.e. voltage ripple in the equivalent arm capacitances and controller dynamic responses have been also verified.

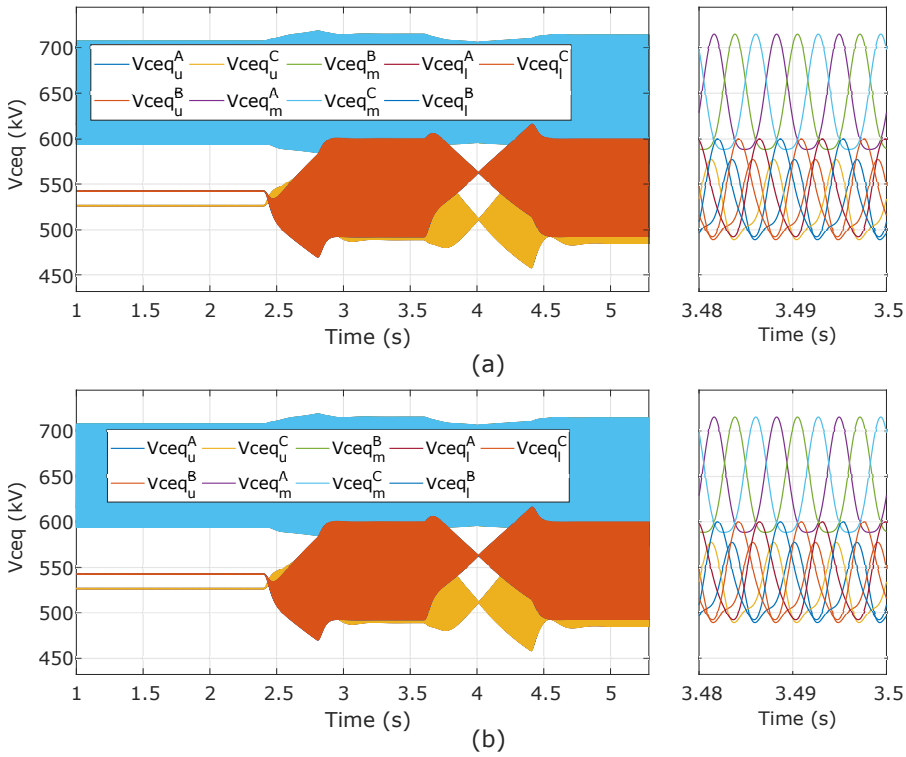


Figure D.6: Voltage of the equivalent capacitance per arm. (a) ADCC connected to the positive pole of the bipole, and (b) ADCC connected to the negative pole of the bipole.

Appendix E

Power Losses Calculations

This appendix presents the models used for the calculation of the conduction and switching losses.

E.1 Regressions from IGBT datasheet

To calculate the losses in the semiconductors, different regressions were obtained based on the datasheet of the considered IGBT [152]. All the regressions are made to be dependent of the current through the device. The regressions linked to the calculation of the conduction losses are the collector-emitter saturation voltage for the IGBT and the emitter-collector voltage for the diode. The mathematical regressions and comparison with the datasheet are presented below.

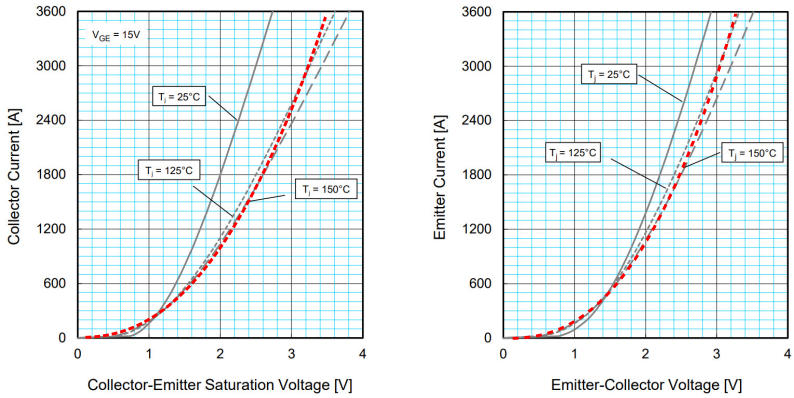


Figure E.1: Datasheet curves for the considered IGBT [152]. (a) Collector-Emitter saturation voltage for the IGBT and the estimated regression (red dashed line). (b) Emitter-collector voltage of the free-wheel diode and the estimated regression (red dashed line).

$$V_{CE}^{T} = 0.0976 \cdot {I_{IGBT}}^{0.4363} \tag{E.1}$$

$$V_{EC}^{D} = 0.1181 \cdot {I_{Diode}}^{0.4049} \tag{E.2}$$

To calculate the switching losses the regressions of the switching energies are obtained from the datasheet. The regressions and the comparison with the datasheet are presented below.

$$E_{on} = 4.7 \times 10^{-7} \cdot {I_{IGBT}}^{2} + 819 \times 10^{-6} \cdot I_{IGBT} + 0.4153 \tag{E.3}$$

$$E_{off} = 1.54 \times 10^{-3} \cdot I_{IGBT} + 0.395 \tag{E.4}$$

$$E_{rec} = -1.92 \times 10^{-7} \cdot {I_{Diode}}^{2} + 143.4 \times 10^{-6} \cdot I_{Diode} + 0.6369 \tag{E.5}$$

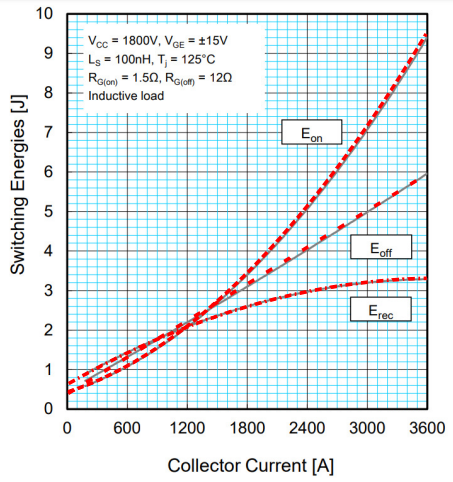


Figure E.2: Switching energies for the IGBT (E_{on} and E_{off}) and diode (E_{rec}) [152], with their respective regressions (red lines).

E.2 Arm simulation

To calculate the switching losses a semi-analytical detailed model is used to simulate one arm. If a modular converter is composed of g arms per leg, a total of g simulations are performed. As the converter operation is assumed to be balanced between the arms, to calculate the total losses it is only necessary to multiply the leg losses per the number of legs N_{legs}. The schematic of the simulation model is presented in Fig. E.3.

The simulation model is implemented in Matlab-Simulink. It uses a controlled current source that follows the analytical set point found in the steady-state analysis of the converter. The arm model is a controlled voltage source linked to the capacitor average arm model (see Section 3.2.2) expressed as a set of equations. The model represent the total number of SMs by a vector of length $N_{SM} \times 1$. The control has a simplified high level control (energy control) and the low level control implements a balancing capacitor algorithm (BCA) to determine the capacitors that should be inserted or bypassed. The BCA used is based on the algorithm presented in [153]. The algorithm was adapted to work with negative modulations emulating the presence of FBSMs in the arm.

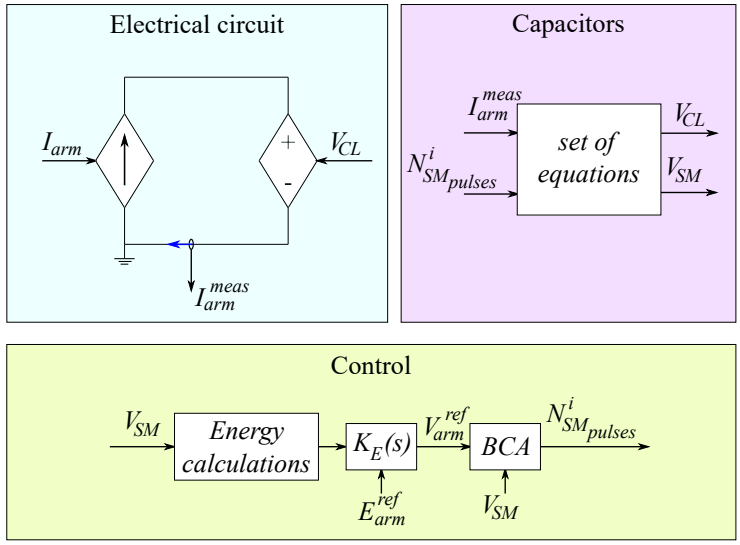


Figure E.3: General schematic of the semi-analytical detailed model.

From the simulated arm, three variables are saved and used in the losses calculations. They are the time vector, the arm current measurement, I_{arm}^{meas}, and the control vector $N_{SM_{pulses}}^{i}$. With the exported results, the conduction and switching losses can be calculated using the current magnitude during the conduction of each switch or at the moment of the commutation event. The calculations are developed for the total number of SMs, N_{SMs}, per arm.

Appendix F

Circulating power comparison

As mentioned in Chapters 3, 6, and 7, the non-isolated converters required an internal ac power to keep the energy balanced. This circulating power depends on the voltage ratio and the transmitted power. A comparison between the power required by the flexible dc-MMC and the ADCC is presented in this appendix.

Using the expressions for the dc power per arm of the flexible dc-MMC (6.12)-(6.14), and the ADCC (7.13)-(7.15), the internal circulating power, P_{cir}, can be found as follows:

$$P_{cir} = \max\left(|P_u|, |P_m|, |P_l|\right) \tag{F.1}$$

where P_u, P_m, and P_l are the dc powers of the upper, middle, and lower arms respectively.

The expression above can be used for the flexible and ADCC. Fig. F.1 presents the internal power of the two converters, normalized to the transmitted power, depending on the voltage ratio. It can be noticed that the flexible dc-MMC requires less circulating power than the ADCC. The ADCC requires to have an equivalent of the half of the transmitted power circulating to balance its energy.

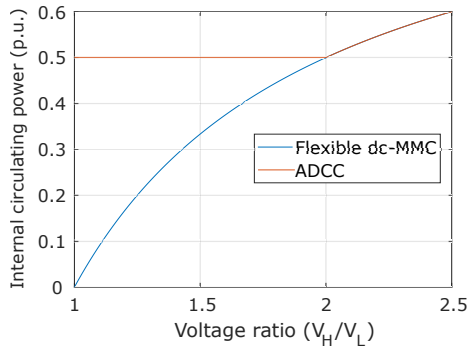


Figure F.1: Comparison internal power

For the ADCC, the detailed design to reduce the power losses is more critical as it has higher circulation power. The optimal design should optimize the size of the inductors and the number of SMs per arm to reduce the currents inside the converter.

Appendix G

HVDC project list

The VSC projects are based on the VSC-HVDC newsletter from Prof. Mike Barnes and Mr. Jack Andrews [154]. The LCC list is mainly based on [155]. Additional sources are available on the table.

Current VSC projects. Main source: Mike Barnes newsletter.										
	Name	**Year Commissioned**	**Power (MW)**	**Voltage DC (kV)**	**Voltage AC (kV)**	**Transmission Length (km)**	**Converter Manufacturer**	**Reference**	**Technology**	**Topology**
1	Hällsjön - Sweden	1997	3	±10	10	10	ABB	https://www.hitachiabb powergrids.com/cn/zh_cn/references/hvdc/zhangbei11111	VSC	SyM
2	Gotland, Sweden	1999	50	±80	80	70	ABB	https://www.hitachiabb-powergrids.com/uk ie/en/references/hvdc/the-gotland-hvdc-link	VSC	SyM
3	Direct Link /TerraNora, Australia	2000	3x60	±80	132/110	59	ABB	https://search.abb.com/library/Download.aspx?DocumentID=POW0027&LanguageCode=en&DocumentPartId=&Action=Launch	VSC	SyM
4	Tjaereborg, Den.	2000	7.2	±9	10.5	4.3	ABB	https://www.hitachiabb powergrids.com/africa/en/references/hvdc/tjaereborg	VSC	SyM
5	Eagle Pass, USA	2000	36	±15.9	132	Back-to-Back	ABB	https://www.hitachiabb powergrids.com/balkans/en/references/hvdc/eagle-pass	VSC	SyM
6	Cross Sound, USA	2002	330	±150	345/138	40	ABB	https://www.hitachiabb powergrids.com/africa/en/references/hvdc/cross-sound-cable	VSC	SyM
7	Murraylink, Australia	2002	220	±150	132/220	180	ABB	https://www.hitachiabb-powergrids.com/references/hvdc/murraylink	VSC	SyM
8	Troll A, Norway	2005	2x44	±60	56/132	70	ABB	https://www.hitachiabb-powergrids.com/references/hvdc/troll-a	VSC	SyM
9	Estlink, Finland	2006	350	±150	400/330	31 (underground) 74 (submarine)	ABB	https://www.hitachiabb powergrids.com/africa/en/references/hvdc/estlink	VSC	SyM
10	Caprivi Link, Namibia	2010	300	-350	330/400	950	ABB	https://www.hitachiabb-powergrids.com/uk ie/en/references/hvdc/caprivi-link	VSC	AM

11	Trans Bay Cable, USA	2010	400	±200	230/138	85	Siemens	http://www.transbaycable.com/	VSC	SyM
12	Valhall, Norway	2011	78	150	300/11	292	ABB	https://www.hitachiabb-powergrids.com/references/hvdc/valhall	VSC	AM
13	Nanhui	2011	18	±30	35/35	8.4 (underground)	C-EPRI	http://www.cepri.com.cn/products/details_39_121.html	VSC	SyM
14	EWIC:East-West Interconnector, Ireland-UK	2013	500	±200	400	75 (underground) 186 (submarine)	ABB	https://www.hitachiabb-powergrids.com/references/hvdc/east-west https://library.e.abb.com/public/4d580b5e493d268dc1257c00003e44dc/Overview%20of%20the%20500MW%20EirGrid%20East-West.pdf interconnector	VSC	SyM
15	Nan'ao Island, China	2013	200, 150, 50	±160	110	Multi-terminal	RXHK, XiDian, NR Electric	https://www.rxhk.co.uk/corporate/news/multi-terminal-vsc-hvdc/	VSC	SyM
16	Zhoushan, China	2014	400, 300, 3x100	±200	110/220	Multi-terminal, 129 subsea	XuJi Electric/NR Electric	http://www.cepri.com.cn/aid/details_71_262.html	VSC	Bipole
17	Mackinac, USA	2014	200	±71	138	Back-to-Back	ABB	https://www.hitachiabb powergrids.com/balkans/en/references/hvdc/mackinac	VSC	SyM
18	Skagerrak 4, Norway Denmark	2014	700	500	400	104 (underground) 140 (submarine) (in bipole with LCC)	ABB	https://www.hitachiabb-powergrids.com/references/hvdc/skagerrak	VSC	Bipole

19	BorWin1, Germany	2015	400	±150	380/170	75 (underground) 125 (submarine)	ABB	https://www.hitachiabb-powergrids.com/references/hvdc/borwin1	VSC	SyM
20	BorWin2, Germany	2015	800	±300	155/400	75 (underground) 125 (submarine)	Siemens	http://www.siemens.com/press/pool/de/feature/2013/energy/2013-08-x-win/factsheet-borwin2-en.pdf	VSC	SyM
21	HelWin1, Germany	2015	576	±250	155/400	45 (underground) 85 (submarine)	Siemens	http://www.siemens.com/press/pool/de/feature/2013/energy/2013-08-x-win/factsheet-helwin1-en.pdf	VSC	SyM
22	INELFE, France-Spain	2015	2x1000	±320	400	65	Siemens	https://www.inelfe.eu/en/projects/baixas-santa-llogaia	VSC	SyM
23	SylWin1, Germany	2015	864	±320	155/400	45 (underground) 160 (submarine)	Siemens	http://www.siemens.com/press/pool/de/feature/2013/energy/2013-08-x-win/factsheet-sylwin1-e.pdf	VSC	SyM
24	HelWin2, Germany	2015	690	±320	155/400	46 (underground) 85 (submarine)	Siemens	http://www.siemens.com/press/pool/de/feature/2013/energy/2013-08-x-win/factsheet-helwin2-en.pdf	VSC	SyM
25	Dolwin1, Germany	2015	800	±320	380/155	90 (underground) 75 (submarine)	ABB	https://www.hitachiabb-powergrids.com/references/hvdc/dolwin1	VSC	SyM
26	Xiamen, China, Fujian Province	2015	1000	±320	220	10.7 (Bipolar)	C-EPRI	http://www.cepri.com.cn/products/details_39_679.html https://ieeexplore-ieee-org.recursos.biblioteca.upc.edu/stamp/stamp.jsp?tp=&arnumber=7787134	VSC	Bipole

27	Troll A 3&4, Norway	2015	2x50	±60	66/132	70	ABB	https://www.hitachiabb-powergrids.com/references/hvdc/troll-a https://search.abb.com/library/Download.aspx?DocumentID=POW0027&LanguageCode=en&DocumentPartId=&Action=Launch	VSC	SyM
28	Ål-link – Finland	2015	100	±80	110	158 (submarine)	ABB	https://search.abb.com/library/Download.aspx?DocumentID=POW0027&LanguageCode=en&DocumentPartId=&Action=Launch	VSC	SyM
29	Luxi, Yunnan Province China	2016	1000	±350	/	Back-to-Back	China Southern Grid, RXHK (Yunnan) XD Group/IEECAS (Guangxi)	http://english.iee.cas.cn/rh/rp/201609/t20160905_167435.html	VSC	B2B
30	NordBalt, Sweden	2016/17	700	±300	400/330	450	ABB	https://www.hitachiabb powergrids.com/africa/en/references/hvdc/nordbalt	VSC	SyM
31	DolWin2, Germany	2017	916	±320	155/380	45 (underground) 90 (submarine)	ABB	https://www.hitachiabb-powergrids.com/references/hvdc/dolwin2	VSC	SyM
32	Maritime Link, Canada	2018	500	±200	230/345	187 OHL, 170 submarine, bipole	ABB	https://www.hitachiabb-powergrids.com/references/hvdc/maritime link	VSC	Bipole
33	Caithness Moray, UK	2018	800 (1200)	±320	275/400	113 (submarine) + overhead lines	ABB	https://www.hitachiabb-powergrids.com/references/hvdc/caithness moray-hvdc-link	VSC	SyM

34	DolWin3, Germany	2018	900	±320	/	78 (underground) 83 (submarine)	GE	http://www.tennet.eu/our-grid/offshore-projects-germany/dolwin3/	VSC	SyM
35	Johan Sverdrup Phase 1, Norway	2018	100	+/-80	300/33	200	ABB	https://www.hitachiabb-powergrids.com/references/hvdc/johan sverdrup shorturl.at/iltFJ	VSC	SyM
36	Yu'E, China	2018/9	1250x4	±420		Back-to-Back, 2 parallel pairs	RXHK, XuJi Electric and C-EPRI	https://www.rxhk.co.uk/corporate/news/yue-hvdc-commissioning complete/	VSC	B2B
37	NEMO GB-Belgium	2019	1000	±400	400/380	140	Siemens	https://www.nemolink.co.uk/ https://www.ptd.siemens.de/HVDC_Nemo.pdf	VSC	SyM
38	Hokkaido Honshu, Japan	2019	300	250	275	98 (overhead line) 24 (cable)	Toshiba	https://www.cigre2019.jp/_img/program/The%20New%20Hokkaido Honshu%20HVDC%20Link.pdf	VSC	Bipole
39	BorWin3, Gemany	2019	900	±320	150/400	30 (underground) 130 (submarine)	Siemens	https://assets.new.siemens.com/siemens/assets/api/uuid:dcc4289e-9325-4daf-9b29-f60e8ff3c194/Factsheet-BorWin3-en.pdf	VSC	SyM
40	Cobra Cable, Neth.-Denmark	2019	700	±320	400	325	Siemens	http://www.cobracable.eu/	VSC	SyM
41	ALEGrO, Belg.-Germany	2020	1000	±320	380	90	Siemens	https://www.elia.be/en/infrastructure-and-projects/infrastructure https://www.amprion.net/Dokumente/Projekte/ALEGrO/Downloads/Projektmedien/ALEGrO_amp_14_002_alegro_en_141024.pdf projects/alegro	VSC	Bipole

42	Kriegers-Flak Combined Solution, Germany/Den.	2020	410	±140	150/400	Back-to-Back	Hitachi ABB	https://en.energinet.dk/Infrastructure Projects/Projektliste/KriegersFlakCGS https://www.hitachiabb powergrids.com/africa/en/references/hvdc/kriegers-flak-combined grid-solutions--kf-cgs--hvdc	VSC	SyM
43	Zhangbei Phase 1	2020	3000x2 , 1500x2	±500	/	666 Multi-terminal	NR Electric, XuJi Electric, C-EPRI and ABB SiFang	https://www.hitachiabb-powergrids.com/references/hvdc/zhangbei https://www.nrec.com/en/index.php/about/newsInfo/65.html	VSC	Bipole
44	KunLiuLong / Wudongde CSG China	2021	8000, 5000, 3000	800	525	Hybrid Multi terminal	RXHK, Xuji, TBEA, NARI, Xidian	https://www.rxhk.co.uk/corporate/news/wudongde-uhvdc-scheme commercial-operation/	LCC/VSC	Bipole
45	NordLink, Germany Norway	2020	1400	±525	400/380	54 (underground) 516 (submarine) 53 overhead line bipole	Hitachi ABB	https://www.hitachiabb-powergrids.com/references/hvdc/nordlink	VSC	RB
46	IFA2, UK France	2021	1000	±320	400	240	Hitachi ABB	http://www.ifa2interconnector.com/ https://www.hitachiabb-powergrids.com/references/hvdc/ifa2	VSC	SyM

47	Pugalur Thirssur, India (PK2000)	2021	2x1000	±320	/	170 km overhead, 32 km cable	Siemens	https://new.siemens.com/global/en/products/energy/high https://transformers-magazine.com/tm-news/first-pole-of-pugalur-trichur-hvdc-link-commissioned/ voltage/high-voltage-direct-current-transmission-solutions/hvdc plus.html (HVDC references)	VSC	Bipole
48	SW Link, Sweden (SydVästlänken)	2021	2x600 (2x720)	±300	410	190 underground cable, 60 OHL	GE	https://www.gegridsolutions.com/products/applications/HVDC/South-West-Link-HVDC-case-study-EN-2015-10-Grid-PEA-0574.pdf https://www.svk.se/sydvastlanken	VSC	SyM
49	North Sea Link, Norway-UK	2021	1400	±525	420/400	730 (submarine)	Hitachi ABB	http://www.northsealink.com/ https://www.hitachiabb powergrids.com/cn/en/references/hvdc/nsn-link	VSC	Bipole

Future VSC projects. Main source: Mike Barnes newsletter										
	Name	**Year to be Commissioned**	**Power (MW)**	**Voltage DC (kV)**	**Voltage AC (kV)**	**Transmission Length (km)**	**Converter Manufacturer**	**Reference**	**Technology**	**Topology**
1	Savoie-Piedmont, Italy-France	2021	2x600	±320	/	190	GE	https://www.gegridsolutions.com/products/applications/hvdc/france-italy-hvdc-link-casestudy-en-2018-02-grid-pea-1641.pdf	VSC	SyM
2	Zhangbei Phase 2	2021	/	/	/	/	/	http://www.cepri.com.cn/release/details_66_745.html https://www.nrec.com/en/web/upload/2019/05/14/15578229444108hgcuh.pdf	VSC	Bipole

3	Wando DongJeju Jeju Island, Korea	2021	200		154kV	100	Hitachi ABB	https://www.hitachiabbpowergrids.com/balkans/en/references/hvdc/wando-dongjeju-3-hvdc-converter-station-project	VSC	SyM
4	Rudong offshore windfarm	2021/2 (estimated)	1100	400	500	100	RXHK, XJ Group	https://www.rxhk.co.uk/corporate/news/rudong-offshore-windpower-hvdc/	VSC	--
5	ElecLink, UK France	2022	1000	±320	400	51	Siemens	http://www.eleclink.co.uk/ https://www.sciencedirect.com/science/article/abs/pii/S0378779620302947	VSC	SyM
6	Johan Sverdrup Phase 2	2022	200	80	300/100	/	Siemens	https://ec.europa.eu/energy/sites/default/files/documents/10._sharifabadi_kamran_-_multivendor_hvdc_links_supplying_oil_and_gas_installations.pdf	VSC	SyM
7	Greenconnector, Switzerland-Italy	2022	1000	±400	/	150	/	http://www.greenconnector.it/	VSC	RB
8	Aquind, UK France	2022	2x1000	±320	400	242	/	http://aquind.co.uk/	VSC	SyM
9	Guangdong	tbc	2x1500	300	/	B2B	RXHK and partners	https://www.rxhk.co.uk/corporate/news/guangdong-b2b-contract award/	VSC	B2B
10	EuroAsia Interconnector	2023	2000	500		1208 Multi-terminal	Siemens	http://www.euroasia-interconnector.com/	VSC	--
11	Attica-Crete	2023	1000	±500	/	330	Siemens	https://www.nsenergybusiness.com/projects/attica-crete-hvdc-interconnector/	VSC	Bipole
12	Viking Link UK-Denmark	2023	1400	±525	400	767	Siemens	http://viking-link.com/	VSC	Bipole

13	FAB Link, UK France	2023	1400	2x ±320	/	2x 180	/	http://www.fablink.net/	VSC	SyM
14	Western-Isles Scotland	2023	450	±320	150	80 subsea 76 underground	/	https://www.ssen-transmission.co.uk/projects/western-isles/ https://www.ssen-transmission.co.uk/media/1247/1454_westernislesneedscasestakeholdersummary.pdf	VSC	--
15	DolWin 6	2023	900	/	/	/	Siemens	https://www.tennet.eu/our-grid/offshore-projects germany/dolwin6/	VSC	--
16	Neuconnect, UK-Germany	2023	1400	500	400	720	/	https://www.neuconnect.eu/	VSC	--
17	Creyke Beck A, UK	2023	1200	±320	66 off- 420 onshore	~130	Hitachi ABB	https://www.hitachiabb-powergrids.com/references/hvdc/dogger bank	VSC	SyM
18	Greenlink, UK Ireland	2023	500	/	/	160 offshore	Siemens-Sumitomo	http://www.greenlinkinterconnector.eu/ https://www.greenlink.ie/post/siemens-energy-and-sumitomo-electric-awarded-epc-contract-for-ireland-uk-interconnector	VSC	--
19	Creyke Beck B, UK	2024	1200	±320	66 off- 420 onshore	~130	Hitachi ABB	https://www.hitachiabb-powergrids.com/references/hvdc/dogger bank	VSC	SyM
20	Ultranet, Germany	2021	2000	±380	400	340 (hybrid OHL parallel with AC)	Siemens	https://new.siemens.com/global/en/products/energy/high voltage/high-voltage-direct-current-transmission-solutions/hvdc plus.html (HVDC references)	VSC	Bipole
21	Baihetan-Jiangsu UHVDC	tbc	/	±800	/	/	RXHK and partners	https://www.rxhk.co.uk/corporate/news/baihetan-jiangsu-uhvdc-transmission-project-contract-award/	LCC/VSC	--

22	Northconnect, UK-Norway	2024	1400	±500	400	655	/	http://www.northconnect.no/	VSC	--
23	DolWin 5	2024	900	/	/	100 km (subsea), 30 km (land cable)	Hitachi ABB	https://www.tennet.eu/our-grid/offshore-projects germany/dolwin5/ https://www.hitachiabb-powergrids.com/references/hvdc/dolwin-5	VSC	SyM
24	SOO Green Rail	2024	2100	525	345	500	Siemens	http://www.soogreenrr.com/	VSC	--
25	Shetland	2024	600	320	132	267	Hitachi ABB	https://www.ssen-transmission.co.uk/projects/shetland/ https://www.hitachiabb-powergrids.com/references/hvdc/shetland	VSC	SyM
26	Creyke Beck C, UK	2024/5	1200	±320	66 off-420 onshore	196 off-, 7 on shore	Hitachi ABB	https://www.hitachiabb-powergrids.com/references/hvdc/dogger bank	VSC	SyM
27	Sofia (Teeside B), UK	2024/5	1400	±320	400	220- offshore, 7 onshore	GE	https://www.ge.com/news/press-releases/ge-consortium-awarded-contract-to-build-state-of-the-art-hvdc-system-for-rwe-sofia-offshore-wind-farm	VSC	SyM
28	Biscay Gulf Link	2025	2200	/	/	370	/	https://www.inelfe.eu/en/projects/bay-biscay	VSC	--
29	Mares, UK-Ireland	2025	750	/	400 (UK)-220 (Ireland)	245	/	http://www.organicpowerinternational.com/mares/ https://maresconnect.ie/wp-content/uploads/2021/06/brochure-Final-2021.pdf	VSC	--
30	A-Nord Germany	2025	up to 2000	525	/	300	/	https://www.amprion.net/Grid-expansion/Our-Projects/A-North/ https://a-nord.amprion.net/Projekt/Erdkabel-und-Bauweise/	VSC	2 bipoles

31	Gridlink, UK France	2025	1400			160	/	https://gridlinkinterconnector.com/ https://bidstats.uk/tenders/2019/W33/708837622	VSC	SyM
32	SuedOstLink	2026	2000	/	/	580	/	http://www.50hertz.com/en/Grid-Extension/Onshore projects/SuedOstLink	VSC	--
33	Abu Dhabi	2025	3200	/	/	/	/	https://www.power-technology.com/comment/offers-abu-dhabi power-project/	VSC	--
34	BorWin 5	2025	900	320	/	120 subsea, 110 underground	Siemens	https://www.tennet.eu/our-grid/offshore-projects germany/borwin5/ https://press.siemens.com/global/en/pressrelease/siemens-energy delivers-technology-seventh-offshore-wind-farm-connection-north sea	VSC	SyM
35	Sunrise windfarm	2025	924	320	/	160	Siemens Energy	https://www.4coffshore.com/news/newsItem.aspx?nid=24409	VSC	--
36	Celtic Link	2026	700	320 to 500	220 and 400	575 (500 subsea)	/	http://www.eirgridgroup.com/the-grid/projects/celtic interconnector/the-project/	VSC	--
37	Norfolk Vanguard, wind farm, UK	Mid-2020s	1800	/	400	/	/	https://group.vattenfall.com/uk/newsroom/news-press releases/pressreleases/stories/hvdc-for-norfolk-offshore-wind farms	VSC	--
38	Norfolk Boreas, wind farm, UK	Mid-2020s	1800	/	400	/	/	https://group.vattenfall.com/uk/newsroom/news-press releases/pressreleases/stories/hvdc-for-norfolk-offshore-wind farms	VSC	--

39	AAPowerLink	2026-8		/	/	800km OHL 4200km subsea cable	/	https://suncable.sg/australia-asia-power-link/	VSC	--
40	Suedlink – DC3	2027	2000	525	400	700	Siemens Energy	https://www.transnetbw.de/de/suedlink https://www.tennet.eu/de/unser-netz/onshore-projekte deutschland/suedlink/	VSC	--
41	Suedlink – DC4	2027	2000	525	400	600	/	https://www.transnetbw.de/de/suedlink https://www.tennet.eu/de/unser-netz/onshore-projekte deutschland/suedlink/	VSC	--
42	Higashi-Shimizu	2027	600	/	275	Back-to-back	Hitachi ABB	https://www.hitachiabb-powergrids.com/references/hvdc/higashi shimizu	VSC	SyM
43	Xlinks1	2027	1800	/	/	3800	/	https://xlinks.co/		
44	AAPL	2027	3000	/	/	3750	/	https://suncable.sg/australia-asean-power-link/		
45	Marinus Link	2027/8	750	/	/	/	/	https://www.marinuslink.com.au/	VSC	
46	Nautilus	2028	1400	/	/	/	/	https://www.nationalgrid.com/group/about-us/what-we do/interconnectors-connecting-cleaner-future/nautilus interconnector	VSC	
47	DolWin 4	2028	900	/	/	/	/	https://www.offshorewind.biz/2020/03/18/amprion-cleared-to start-dolwin4-and-borwin4-public-planning-preps/	VSC	
48	BorWin 4	2029	900	/	/	/	/	https://www.offshorewind.biz/2020/03/18/amprion-cleared-to start-dolwin4-and-borwin4-public-planning-preps/	VSC	
49	Xlinks2	2029	1800	/	/	3800	/	https://xlinks.co/		

50	Marinus Link stage 2	2029/30	750	/	/	/	/	https://www.marinuslink.com.au/		
51	Egypt-Saudi Arabia	/	3000	/	/	/	Hitachi Energy	https://www.hitachienergy.com/news/press releases/2021/10/hitachi-abb-power-grids-consortium-awarded major-contract-for-the-first-ever-large-scale-hvdc-interconnection in-the-middle-east-and-north-africa		
52	Eurolink	2030	1400	/	/	/	/	https://www.nationalgrid.com/our-businesses/national-grid ventures/interconnectors-connecting-cleaner-future	VSC	
53	Eastern Link, UK	2030	2000 x2	/	/	440	/	https://www.ssen-transmission.co.uk/projects/eastern-hvdc-link/	VSC	
54	Icelink	2030 - Under considerati on	1000	/	/	1000	/	https://www.nationalgrid.com/group/about-us/what-we do/interconnectors-connecting-cleaner-future https://www.landsvirkjun.com/researchdevelopment/submarinecabletoeurope	VSC	
55	East Anglia 3	2030	1400	/	/	/	/	https://www.offshore-mag.com/renewable energy/article/14204028/aker-solutions-siemens-energy-to-deliver uk-north-sea-east-anglia-three-offshore-wind-hvdc-stations		
56	IJMUiden Alpha, Netherlands	2030 – R&D Phase	2000	525	/	/	/	https://www.tennet.eu/news/detail /tennet-develops-first-2gw offshore-grid-connection-with-suppliers/	VSC	

57	IJMUiden Beta, Netherlands	2030 – R&D Phase	2000	525	/	/	/	https://www.tennet.eu/news/detail/tennet-develops-first-2gw offshore-grid-connection-with-suppliers/	VSC	
58	HIP Atlantic Project	In planning	4x1000	/	/	/	/	https://www.4coffshore.com/news/102c000-mw-wind-project planned-for-north-atlantic-nid23555.html		
59	SylWin 2	Submitting for approval	900	/	/	/	/	http://www.4coffshore.com/windfarms/hvdc-converter-sylwin2-converter-cid13.html	VSC	
60	SENER-BC, Mexico	Pre-tender	1500	+/-500		700 (bipolar)	/	http://www.nortonrosefulbright.com/knowledge/publications/163291/mexicos-first-public-bid-for-electric-transmission-lines	VSC	
61	AWC, USA	In considerati on	1000	±320	/	Multi-terminal	GE	http://atlanticwindconnection.com/new-jersey-energy-link/	VSC	
62	Tres-Amiga's, USA	In considerati on	3x750	300	345	Back-to-back	GE	http://www.tresamigasllc.com/	VSC	B2B

Current LCC projects. Main source: https://web.archive.org/web/20140201181654/http://www.ece.uidaho.edu/hvdcfacts/Projects/HVDCProjectsListingMarch2012-existing.pdf										
	Name	**Year Commissioned**	**Power (MW)**	**Voltage DC (kV)**	**Voltage AC (kV)**	**Transmission Length (km)**	**Converter Manufacturer**	**Reference**	**Technology**	**Topology**
1	GOTLAND II - III, Sweden	1983	130	±150		100	ASEA		THY	Bipole
2	VOLGOGRAD-DONBASS, Russia	1962/65	720	±400		473	MINISTRY FOR ELECTROTECHNICAL INDUSTRY OF USSR		MERC/THY	Bipole
3	NEW ZEALAND HYBRID INTER ISLAND LINK	1992-2013	1240	±350		612	ABB		THY	Bipole
4	KONTI-SKAN (Denmark-Sweden)	1965-2006	250	Pole 1: 250 Pole 2: 300	pole 1: 30/150 pole 2: 400	180	ASEA	https://www.hitachienergy.com/references/hvdc/konti-skan	THY	Bipole (2 AM)
5	SACOI (Italy)	1965	200	200		385 multi-terminal	ENGLISH ELECTRIC	http://www.bestpaths-project.eu/contents/publications/03_06_cirio.pdf	THY	AM

6	PACIFIC INTERTIE - USA	1970-2020	3100	±560	230-500	1362	ABB	https://www.hitachienergy.com/references/hvdc/pacific-intertie https://www.semanticscholar.org/paper/Advances-in-HVDC-Technology-as-applied-to-the-HVDC-Litzenberger/94311a173cea23c38e0f5e8289f0667f8c5edff4	THY	Bipole
7	EEL RIVER - Canada	1972-2014	320	±80		B-B	GENERAL ELECTRIC - ABB	https://www.hitachienergy.com/references/hvdc/eel-river	THY	B2B
8	NELSON RIVER - Canada	1973-2004	1854 2000	±463 ±500		890	ENGLISH ELECTRIC/GEC ALSTHOM	https://www.ieee-pes.org/presentations/gm2014/Nelson_River_HVDC_Panel_Session.pdf	THY	2 Bipole
9	SKAGERRAK I-III (Norway - Denmark)	1976-2007	250 25 500	250 250 350	300 300 350	240	ASEA - ABB	https://www.hitachienergy.com/references/hvdc/skagerrak	THY	2 Bipole
10	SHIN-SHINANO 1 Japan	1999	53	125	375 66 66	B-B	HITACHI/TOSHIBA/NISSHIN	http://psg.mitsubishielectric.co.uk/products/hvdc-facts/hvdc-solutions/shin-shinano-vsc/	GTO	B2B

11	SQUARE BUTTE - USA	1977	500	±250		749	GENERAL ELECTRIC	https://www.hitachienergy.com/references/hvdc/square-butte	THY	Bipole
12	DAVID A. HAMIL - USA	1977	100	±50		B-B	GENERAL ELECTRIC		THY	B2B
13	CAHORA-BASSA (South Africa-Mozambique)	1975/1998	1920	±533	220-275	1456	AEG/BBC/SIEMENS /ABB	https://www.hitachienergy.com/references/hvdc/cahora-bassa	THY	Bipole
14	CU - USA	1979-2019	1000	±400	235-350	701	ASEA -ABB	https://www.hitachienergy.com/references/hvdc/cu-hvdc-project https://ieeexplore-ieee-org.recursos.biblioteca.upc.edu/stamp/stamp.jsp?tp=&arnumber=9299901	THY	Bipole
15	HOKKAIDO-HONSHU -Japan	1979	300	250		167	ASEA	https://www.toshiba-energy.com/en/info/info2019_0328_02.htm	THY	bipole
16	ACARAY (Paraguay-Brazil)	1981	55	±25		B-B	SIEMENS		THY	B2B
17	VYBORG (Russia - Findland)	1981	355	1X170(±85)		B-B	MINISTRY FOR ELECTROTECHNICAL INDUSTRY OF USSR		THY	B2B
18	ZHOU SHAN PROJECT - China	1982	50	100		42			THY	--

19	INGA-SHABA (Democratic republic of congo)	1982-2017	560	±500	220	1700	ASEA/GE/itachi	https://www.hitachienergy.com/references/hvdc/inga-kolwezi	THY	Bipole
20	EDDY COUNTY - USA	1983	200	82		B-B	GENERAL ELECTRIC		THY	B2B
21	POSTE CHATEAUGUAY (Canada - USA)	1984	2x500	145		B-B	BBC/SIEMENS		THY	B2B
22	CHATEAUGUAY UPGRADE - Canada	2009	2x500	145		B-B	ABB		THY	B2B
23	OKLAUNION - USA	1984	200	82		B-B	GENERAL ELECTRIC		THY	B2B
24	ITAIPU 1 - Brazil	1984-1990	1575	±600	500	785	ASEA - ITACHI	https://www.hitachienergy.com/references/hvdc/itaipu	THY	2 Bipole
25	BLACKWATER - Usa	1985	200	57		B-B	BBC		THY	B2B
26	HIGHGATE - USA	1985	200	±56		B-B	ASEA		THY	B2B
27	MADAWASKA - Canada	1985	350	130.5		B-B	GENERAL ELECTRIC		THY	B2B
28	MILES CITY HVDC SYSTEM (MCCS) - USA	1985	200	82		B-B	GENERAL ELECTRIC		THY	B2B
29	BROKEN HILL - Australia	1986	40	2x17 (±8.33)		B-B	ASEA		THY	B2B
30	INTERMOUNTAIN POWER PROJECT (I.P.P.) - USA	1986	1920	±500		785	ASEA	https://ieeexplore.ieee.org/document/193910	THY	Bipole

31	CROSS CHANNEL BP 1+2 (France -UK)	1985/86	2000	±270		70	CGEE ALSTHOM/GEC	https://www.enerzine.com/linterconnexion-franco-britannique-modernisee/4834-2008-07 https://www.gegridsolutions.com/products/applications/hvdc/hvdc-ifa2000renovation-casestudy-en-2018-04-grid-pea-0572.pdf	THY	2 Bipoles
32	QUEBEC-NEW ENGLAND (THREE TERMINAL) (Canada - USA)	1990-92	2250	±450		1500	ABB		THY	Bipole
33	VIRGINIA SMITH - USA	1987	200	50		B-B	SIEMENS		THY	B2B
34	GESHA (GEZHOUBA-SHANGHAI) - China	1989	600	500		1000	BBC/SIEMENS	https://www.hitachienergy.com/references/hvdc/gezhouba-shanghai	THY	Bipole
35	VINDHYACHAL - India	1989	500	2x69.7		B-B	ASEA		THY	B2B
36	McNEILL - Canada	1989	150	42		B-B	GEC ALSTHOM		THY	B2B
37	FENNO-SKAN (Findland-Sweden)	1989/98	500 800	400 500	400	303	ABB/ALCATEL	https://library.e.abb.com/public/38329002ed89478a9e37321e98938760/POW0106.pdf	THY	2 AM

38	BARSOOR LOWER SILERU - India	1989/91	100	±200		196	BHEL	https://web.archive.org/web/20051115122740/http://www.transmission.bpa.gov/cigresc14/Compendium/SILERU.htm	THY	Bipole
39	RIHAND-DELHI - India	1991	1500	±500		814	ABB/BHEL	https://www.hitachienergy.com/references/hvdc/rihand-delhi	THY	Bipole
40	SAKUMA - Japan	1993	300	±125		B-B	HITACHI/TOSHIBA/MITSUBISHI/NISSHIN		THY	B2B
41	URUGUAIANA (Brazl - Argentina)	1994	50	15		B-B	TOSHIBA		THY	B2B
42	BALTIC CABLE (Sweden - Germany)	1994	600	450		261	ABB		THY	AM
43	WELSH - USA	1995	600	170		B-B	SIEMENS		THY	B2B
44	KONTEK (Denmark-Germany)	1995	600	400		171	ABB/NKT CABLES		THY	AM
45	HAENAM-CHEJU - Korea	1997	300	±180		101	GEC ALSTHOM		THY	Bipole
46	CHANDRAPUR-RAMAGUNDUM - India	1997/98	1000	2x205		B-B	GEC ALSTHOM		THY	B2B
47	LEYTE-LUZON -Philippines	1998	440	350	230	455	ABB/MARUBENI	https://www.hitachienergy.com/case-studies/leyte-luzon	THY	AM
48	WELCH-MONTICELLO -USA	1998	600	162		B-B	SIEMENS		THY	B2B
49	MINAMI-FUKUMITZU -Japan	1999	300	125		B-B	HITACHI/TOSHIBA		THY	B2B

50	VIZAG 1 -India	1999	500	205		B-B	GEC ALSTHOM		THY	B2B
51	VIZAG 2 - India	2005	500	±88		B-B	ABB		THY	B2B
52	VISBY-NAS - Sweden	1999	50	80		70	ABB		THY	AM
53	SWEPOL LINK (Sweden - Poland)	2000	600	±450		254	ABB		THY	AM
54	KII CHANNEL - Japan	2000	1400	±250		102	HITACHI/TOSHIBA/MITSUBISHI		THY	Bipole
55	GARABI 1 - (Argentina-Brazil)	2000	1100	±70		B-B	ABB		THY	B2B
56	RIVERA (Uruguay - Brazil)	2000	70	20		B-B	GEC ALSTHOM		THY	B2B
57	GRITA (Greece-Italy)	2001	500	400		316	PIRELLI/ABB		THY	AM
58	TIAN-GUANG (China)	2001	1800	±500		960	SIEMENS	10.1049/cp:19960342	THY	Bipole
59	HIGASHI-SHIMIZU - Japan	2001	300	125		B-B	HITACHI/TOSHIBA		THY	B2B
60	MOYLE INTERCONNECTOR - Northern Ireland Scotland	2001	2x250	2x250		64	SIEMENS		THY	2 AM
61	THAILAND-MALAYSIA	2001	300	±300		110	SIEMENS	http://www.bigconnectivity.org/beta/sites/default/files/2017-03/01-Session%201.5-Thailand%20Case.pdf	THY	AM possible extenson to a Bipole

62	SASARAM - India	2002	500	205		B-B	GEC ALSTHOM		THY	B2B
63	RAPID CITY TIE - USA	2003	2 x 100	±13		B-B	ABB		THY	B2B
64	EAST-SOUTH INTERCONNECTOR II - India	2003	2000	±500		1450	SIEMENS	10.1049/cp:20010522	THY	Bipole
65	THREE GORGES-CHANGZHOU - China	2003	3000	±500		860	ABB/SIEMENS	https://library.e.abb.com/public/1a115447a1040f63c125721e0042bdf3/Three%20Gorges%20-%20Shanghai%20HVDC%20-%20%20Reinforcing%20Interconnection.pdf	THY	Bipole
66	GUI-GUANG I - China	2004	3000	±500		980	SIEMENS	https://www.researchgate.net/publication/3976648_Basic_design_aspects_of_Gui-Guang_HVDC_power_transmission_system	THY	Bipole
68	LAMAR - Usa	2005	210	±64		B-B	SIEMENS		THY	B2B
69	LINGBAO - China	2005	360	168		B-B	NR, ABB, C-EPRI		THY	B2B
70	BASSLINK - Australia	2006	500	400		350	SIEMENS	http://www.basslink.com.au/basslink-interconnector/operations/	THY	AM

72	NEPTUNE - USA	2007	660	500		105	SIEMENS	https://docplayer.net/17524322-The-neptune-regional-transmission-system-500-kv-hvdc-project.html	THY	AM
73	SHARYLAND (USA - Mexico)	2007	150	±21		B-B	ABB		THY	B2B
75	LEVIS DE-ICER - Canada	2008	250	±17.4		27 to 242	AREVA	https://www.researchgate.net/publication/280156147_De-Icer_Installation_at_Levis_substation_on_Hydro_Quebec's_High_Voltage_System	THY	De-icer SyM
76	NORNED (Norway-Netherlands)	2008	700	±450		580	ABB	http://www.jicable.org/TOUT_JICABLE_FIRST_PAGE/2007/2007-B7-2_page1.pdf	THY	Bipole
77	BALLIA - BHIWADI - India	2010	2500	500		800	SIEMENS	https://www.researchtrend.net/ijeece/pdf/17%20AHUTI.pdf	THY	Bipole
78	OUTAOUAIS - Canada	2009	2x625	315		B-B	ABB		THY	B2B
79	AL FADHILI - Saudi Arabia	2009	3 x 600	3 x 222		B-B	AREVA		THY	B2B
80	SAPEI (Italy - Mainland Sardinia)	2011	1000	±500		435	ABB		THY	Bipole
81	BRITNED (UK-Netherlands)	2011	1000	±400		260	SIEMENS		THY	SyM
82	YUNNAN-GUANGDONG - China	2010	5000	±800		1418	SIEMENS		THY	Bipole

83	STOREBAELT - Denmark	2010	600	400		56	SIEMENS	https://search.abb.com/library/Download.aspx?DocumentID=2GM5069%20GB&LanguageCode=en&DocumentPartId=&Action=Launch	THY	AM
84	XIANJIABA-SHANGHAI -China	2010	6400	±800	525	1980	ABB	https://www.hitachienergy.com/cn/zh_cn/case-studies/xiangjiaba--shanghai	THY	Bipole
85	HULUNBEIR-LIAONING HVDC LINK - China	2010	3 000	±500	525	920	ABB	https://www.hitachienergy.com/me/en/case-studies/hulunbeir--liaoning	THY	Bipole
86	LINGBAO II EXTENSION PROJECT -China	2010	750	168		B-B	ABB/ALSTOM		THY	B2B
87	JINDO-JEJU -Korea	2011	400	±250		105	ALSTOM	https://www.gegridsolutions.com/products/applications/hvdc/hvdc-jeju-casestudy-en-2018-04-grid-pea-0576.pdf	THY	Bipole
88	COMETA -Spain	2012	400	250	230	247	PRYSMIAN/NEXANS/SIEMENS		THY	Bipole
89	RIO MADEIRA - Brazil	2014	2 x 3150	±600		2375	ABB (BIPOLE 1) &ALSTOM (BIPOLE 2)	https://www.hitachienergy.com/references/hvdc/rio-madeira	THY	Bipole

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