

HYSTERESIS CONTROL IN HYBRID PEROVSKITE-BASED DEVICES FOR PHOTOVOLTAIC AND NEUROMORPHIC COMPUTING APPLICATIONS



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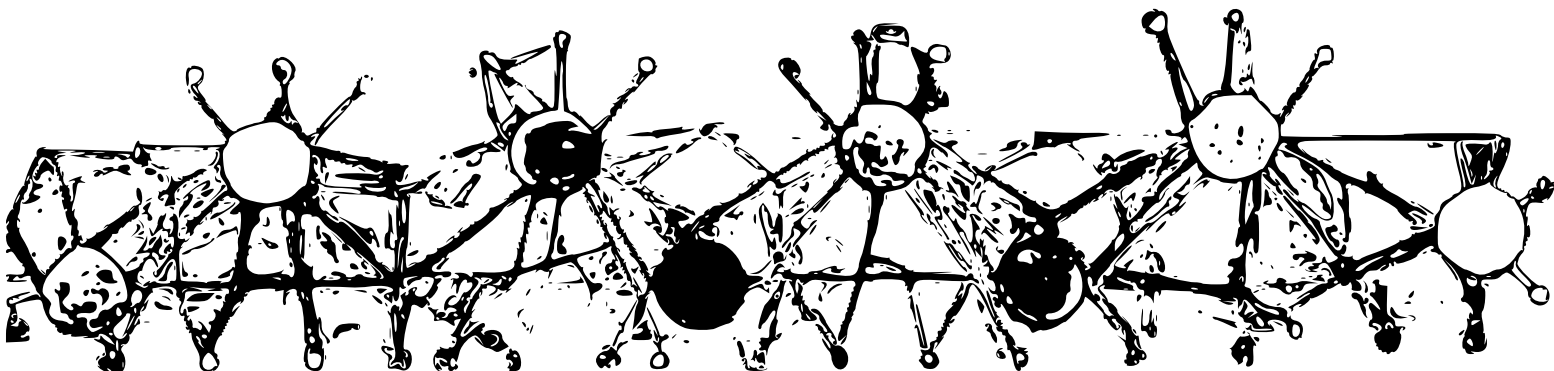


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Hysteresis Control in Hybrid Perovskite-based Devices for Photovoltaic and Neuromorphic Computing Applications

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ABSTRACT

Perovskite technology has emerged to be one of the most promising material platforms for versatile optoelectronic applications. Perovskite solar cells have been rapidly advancing in record efficiencies at an unprecedented rate already approaching the theoretical maximum efficiency in just over a decade of development. Despite this rapid advancement in efficiencies, commercialization of perovskite solar cells is hindered by the persistence of hysteresis critically related to device operational instability. Most notably, this intrinsic hysteretic effect of perovskite materials can be exploited for memory devices or memristors emulating the synaptic functions of the brain circumventing the physical limits of conventional computing architecture. Hence, the further advancement of perovskite materials as promising candidates in both photovoltaic and computing technologies relies fundamentally on the hysteresis control in the current-voltage ($I - V$) response. For perovskite solar cells, minimizing the $I - V$ hysteresis is crucial for the long-term stability requirements to meet the standards for commercialization. On the other hand, controlling the hysteretic memristive response is essential for memristor device designs with tailored memory properties for reconfigurable and more complex neuromorphic computing frameworks.

In this thesis, we control the hysteresis effect in perovskite-based devices via systematic sets of experimental designs with varying device configurations. We demonstrate control of the hysteresis by incorporating a thin Ag layer that has previously led to minimized hysteresis in perovskite solar cells, but also has exhibited considerable resistive switching in perovskite-based memristors. Moreover, by the proper selection of the perovskite formulation in solar cells, the type of hysteresis is determined – normal or inverted hysteresis. Notably, we demonstrate a perovskite solar cell exhibiting a transformation from a normal capacitive to an inverted inductive hysteresis. Finally, we modulate the resistance state transition in perovskite-based memristors by the inclusion of interfacial buffer layers exhibiting both volatile drift and nonvolatile diffusive resistive switching mechanisms depending on the applied external field.

Complementarily, we have developed an impedance spectroscopy (IS) measurement protocol to systematically investigate the dynamic state evolution of the perovskite solar cells and memristors unravelling the underlying mechanisms governing the hysteretic and memory effects. Most notably, this systematic anal-

ysis of the impedance spectral evolution has allowed us to develop a method to correlated the time domain $I - V$ response with the frequency domain IS revealing a vital insight in both solar cell and memristor configurations – normal hysteresis is capacitive, while inverted hysteresis is inductive. Furthermore, we demonstrate and model a distinct phenomenon of a voltage-dependent transformation from capacitive to inductive IS response revealing that the low frequency capacitor and inductor are not completely independent process, rather, they correspond to a similar process influenced by ionic transport at the interfaces.

The individual insights and achievements of the works included in this thesis have ultimately culminated in a more complete picture of the complex ionic transport dynamics involving the migrating ions, vacancies, activated metals, and interfacial reactivity in perovskite-based devices. This understanding of the dynamic ionic transport, in conjunction with the electronic transport, provides the necessary insight to control the hysteresis response of perovskite-based devices specifically suited for the targeted optoelectronic application. Moreover, the newly established IS measurement protocol can be implemented in any system allowing the extraction of essential parameters which can be further enriched by formulating dynamical models unravelling the underlying mechanisms. This hysteresis control would not only further advance the corresponding technologies by circumventing the theoretical and physical limits, but would also broaden and complement the already-well established theories and concepts in the field of perovskite technology.

RESUMEN

La tecnología de perovskita ha emergido como una de las plataformas de material más prometedoras para aplicaciones optoelectrónicas versátiles. Las células solares de perovskita han avanzado rápidamente en eficiencias récord a una tasa sin precedentes, acercándose ya a la máxima eficiencia teórica en poco más de una década de desarrollo. A pesar de este rápido avance en las eficiencias, la comercialización de las células solares de perovskita se ve obstaculizada por la persistencia de la histéresis críticamente relacionada con la inestabilidad operativa del dispositivo. Especialmente, este efecto intrínseco de histéresis de los materiales de perovskita puede ser explotado para dispositivos de memoria o memristores que emulan las funciones sinápticas del cerebro, evitando los límites físicos de la arquitectura de computación convencional. Por lo tanto, el avance de los materiales de perovskita como candidatos prometedores tanto en tecnologías fotovoltaicas como de computación depende fundamentalmente del control de la histéresis en la respuesta corriente-voltaje ($I - V$). Para las células solares de perovskita, minimizar la histéresis $I - V$ es crucial para los requisitos de estabilidad a largo plazo para cumplir con los estándares de comercialización. Por otro lado, el control de la respuesta memristiva es esencial para los diseños de dispositivos memristores con propiedades de memoria adaptadas para estructuras de computación neuromórfica reconfigurable y más compleja.

En esta tesis, controlamos el efecto de histéresis en dispositivos basados en perovskita a través de diseños experimentales sistemáticos con diferentes configuraciones de dispositivos. Demostramos el control de la histéresis mediante la incorporación de una capa delgada de Ag que ha llevado a minimizar la histéresis en las células solares de perovskita, pero también ha mostrado un cambio considerable de resistencia en memristores basados en perovskita. Además, mediante la selección adecuada de la formulación de perovskita en células solares, se determina el tipo de histéresis – normal o invertida. En particular, mostramos una célula solar de perovskita que presenta una transformación de una histéresis capacitiva normal a una histéresis inductiva invertida. Por último, modulamos la transición del estado de resistencia en memristores basados en perovskita mediante la inclusión de capas “buffer” interfaciales que exhiben mecanismos volátiles de deriva y no volátiles de difusión de cambio de resistencia dependiendo del campo externo aplicado.

Además, hemos desarrollado un protocolo experimental para medir espectroscopía de impedancia (IS) e investigar sistemáticamente la evolución del estado dinámico de las células solares y los memristores de perovskita desentrañando los mecanismos subyacentes que gobiernan los efectos de histéresis y de memoria. Lo más notable es que este análisis sistemático de la evolución espectral de la impedancia nos ha permitido desarrollar un método para correlacionar la respuesta de dominio de tiempo $I - V$ con el dominio de frecuencia IS, revelando una idea vital en las configuraciones de células solares y memristores – la histéresis normal es capacitiva, mientras que la histéresis invertida es inductiva. Además, demostramos y modelamos un fenómeno distintivo de transformación dependiente del voltaje de la respuesta IS capacitiva a inductiva, lo que revela que el capacitor y el inductor de baja frecuencia no son procesos completamente independientes, sino que corresponden a un proceso similar influenciado por el transporte iónico en las interfaces.

Las ideas e innovaciones individuales incluidas en esta tesis han culminado en una imagen más completa de la dinámica compleja del transporte iónico que involucra migración de iones, vacantes, metales activados y reactividad interfacial en dispositivos basados en perovskita. Esta comprensión del transporte iónico dinámico, en conjunción con el transporte electrónico, proporciona la información necesaria para controlar la respuesta de histéresis de los dispositivos basados en perovskita específicamente adaptados para la aplicación optoelectrónica deseada. Además, el protocolo de medidas para espectroscopía de impedancia recién establecido se puede implementar en cualquier sistema que permita la extracción de parámetros esenciales que se pueden enriquecer aún más mediante la formulación de modelos dinámicos que revelen los mecanismos subyacentes. Este control de histéresis no solo avanzaría aún más en las tecnologías correspondientes al evadir los límites teóricos y físicos, sino que también ampliaría y complementarían las teorías y conceptos ya bien establecidos en el campo de la tecnología de perovskita.

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Chapter 1

Introduction

In the advent of exponential technological growth and advancement, optoelectronic devices are currently approaching their theoretical and physical limits. Two of the most pressing technologies currently becoming more and more crucial today are the (i) *solar cell*, and the (ii) *information and computing* technologies. For solar cells, the continued effort in the rapid improvement of power conversion efficiencies with more cost-effective alternative technologies is now approaching the theoretical maximum efficiency also known as the *detailed balance limit* [1–4]. On the other hand, the continued downscaling of computing devices for high-speed, powerful and highly capable data processing doubling every two years, also known as *Moore’s law*, is now approaching its fundamental physical limits, i.e. heat wall and memory wall [5, 6]. In both technologies, one material system can address both limits as the new versatile emerging technology – the *perovskite*.

Perovskite solar cells as a new class of emerging photovoltaic technology has been gaining an unprecedented rise into one of the most promising materials for solar cell applications. Perovskite solar cells have been rapidly advancing in record efficiencies already exhibiting 25.7% efficiency in just over a decade of development as compared to crystalline silicon solar cells which took over half a century to reach 26.1% efficiency [7]. Most notably, the integration of perovskites with silicon photovoltaics as tandem solar cells has shown great potential in breaking the detailed balance limit of a single junction solar cell already reaching 32.5% efficiency [7, 8]. This remarkable advancement in perovskite solar cell record efficiencies is mainly due to its exceptional optoelectronic proper-

ties. These favorable optoelectronic characteristics, in addition to the facile and cost-effective fabrication technique via solution processing at low temperatures (~ 100 °C), make the perovskite an exceptional technology in photovoltaic applications [9–11]. The emergence of perovskite solar cells in photovoltaic applications is further discussed in detail in *Section 1.2*. However, despite the promising advancement in record efficiencies, perovskite solar cells exhibit hysteresis in the characteristic current-voltage ($I - V$) curve that has been critically related to device operational stability [12–17]. A more detailed discussion on the origin of this hysteretic effect in the $I - V$ curve is presented in *Section 1.3*. Hence, understanding the underlying mechanisms in this phenomenon is of paramount importance in the further development of perovskite solar cell technology towards long-term stability and commercialization.

On the other hand, the intrinsic hysteretic $I - V$ response of perovskite devices is required for *in-situ* data processing at the same place where the data is stored (in-memory computing), circumventing the fundamental physical limits in the traditional von Neumann computing architecture [5, 6, 18]. In the conventional von Neumann computing architectures, the data storage and the processing unit are physically separated leading to high energy consumption in demanding computing tasks [5, 6, 18, 19]. In contrast, devices exhibiting inherent memory effects (hysteretic $I - V$), called *memristors*, are considered to be new and emerging memory concepts for in-memory and neuromorphic computing [20]. This computational scheme aims to mimic the processes of the highly interconnected network of neurons and synapses in the human brain to achieve outstanding energy efficiency for data intensive computation such as big data analysis, machine learning, and artificial intelligence [21–23]. The theoretical and experimental foundations of the memristors, together with the introduction of memristive systems and resistive switching parameters for suitable in-memory computing applications, are presented in *Section 1.4*. The perovskite, as a material platform, possesses a vast range of options and combinations for memristive devices with switching physics suitable for a wide variety of neuromorphic computing architectures [24]. It has a compositional space of $>10^6$ formulations that can be further explored via a facile solution-based processing [25–28]. Reported perovskite-based memristors demonstrating state-of-the-art

switching performance are briefly summarized in *Section 1.5*. However, the current approach of optimizing memristors specific to a single switching requirement impede the possibility of integrating multiple computational schemes for a more complex implementation of neural network architectures all in a single processing unit. Hence, understanding and controlling the resistive switching mechanism in perovskite-based memristors would allow for tailored device design for specific and more complex computational platforms.

1.1 Thesis Structure

This Ph.D. thesis is formatted as a compilation of published journal articles with the following structure:

Chapter 1 introduces and reviews the fundamental theories and related literature on the state-of-the-art solar cell and memristor technologies. This includes the emergence of perovskite solar cells, hysteresis in perovskite solar cells, hysteresis and memristive systems, perovskite-based memristors, and the application horizon of perovskite-based devices in photovoltaic and in-memory computing applications.

Chapter 2 presents the critical overview of this work of controlling the hysteresis effect in perovskite-based devices. In order to achieve this general objective, this work is broken down into 4 sub-objectives culminating to a more complete insight on the complex interplay among the migrating ions, vacancies, activated metals and interfacial reactivity. This thesis critical overview summarizes the experimental designs, achievements and relevance of individual works addressing each sub-objective. Moreover, the essential insights carried over to the subsequent work are highlighted. Finally, the overall impact and contribution of the totality of the work in the scientific field are emphasized.

Chapter 3 discusses the experimental details implemented for this work. This includes the device fabrication of perovskite-based devices as solar cells and memristors, the electrical characterization, and the newly established CA-IS measurement protocol. Schematic diagrams are included to illustrate the methods employed for both the device fabrication and characterizations.

Chapters 4 to 7 present the complete published journal articles addressing

each of the 4 individual sub-objectives as stated previously.

Finally, **Chapter 8** summarizes the main results in accordance with the objectives highlighting the overall relevance and contribution of the work in the scientific field.

1.2 Emergence of Perovskite Solar Cells

1.2.1 Solar Cell Fundamentals

The most important photovoltaic device is the solar cell, a semiconductor absorber layer placed in between appropriate electron and hole selective contacts, which can convert solar radiation directly into electrical energy with high overall efficiency [29–31]. The ideal solar cell is assumed to have a diode $I - V$ characteristics with the simplified equivalent circuit shown in Fig. 1.1 . The current-voltage ($I - V$) characteristic response of such device is given by

$$I = I_s(e^{qV/kT} - 1) - I_L \quad (1.1)$$

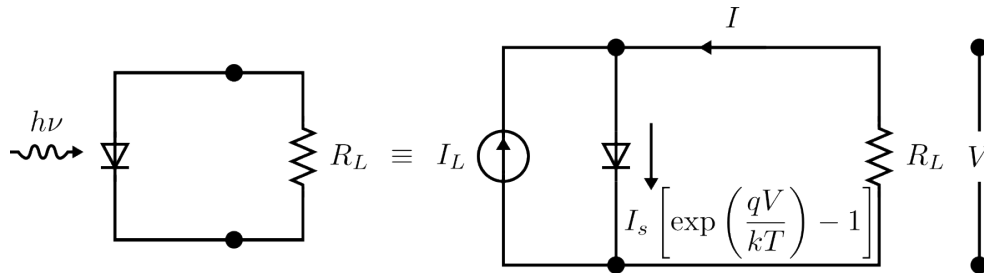


Figure 1.1: Ideal solar cell equivalent circuit.

where I_s is the saturation current, q is the electron charge, k is the Boltzmann constant, T is the temperature, and I_L is the strength of constant current source due to the incident light (photocurrent). It is noted that the curve passes through the fourth quadrant (Fig. 1.2a), hence, that power can be extracted from the device. The $I - V$ curve is more generally represented as the inversion of the current about the voltage axis as shown in Fig. 1.2b. Several key photovoltaic parameters of the $I - V$ curve are defined to describe the solar cell characteristics. The short-circuit current (I_{sc}) is the maximum current of the device at zero applied bias (0 V). Another key parameter is the open-circuit

voltage (V_{oc}) defined as the voltage at which the net current flow is zero. From Eq. 1.1, the V_{oc} is obtained by

$$V_{oc} = \frac{1}{\beta} \ln \left(\frac{I_L}{I_s} + 1 \right) \quad (1.2)$$

where $\beta = q/KT$. The maximum power output is defined as $P_{mpp} = I_{mpp} \times V_{mpp}$, where I_{mpp} and V_{mpp} are the corresponding current and voltage for the P_{mpp} , respectively. The output power is then given by

$$P = IV = I_s V (e^{\beta V} - 1) - I_L V \quad (1.3)$$

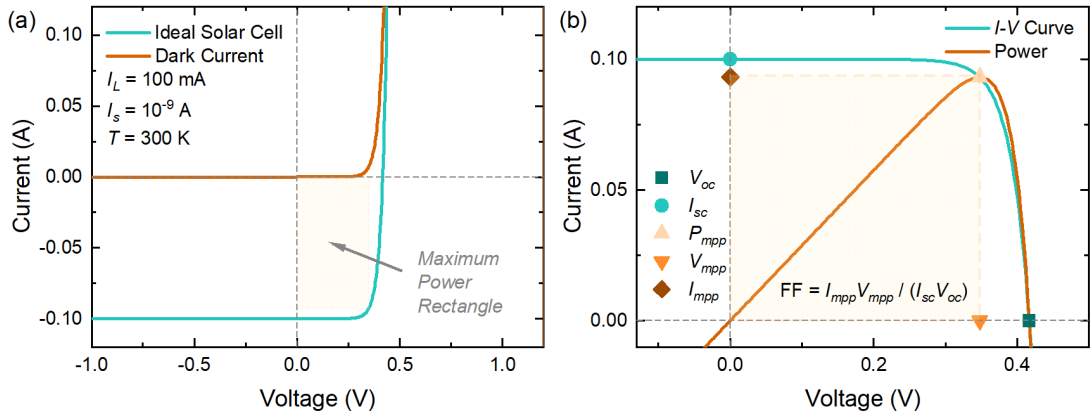


Figure 1.2: (a) The $I - V$ characteristics of an ideal solar cell under illumination with a photocurrent of $I_L = 100$ mA, saturation current of $I_s = 10^{-9}$ A and temperature of $T = 300$ K. (b) The typical representation of the $I - V$ curve as the inversion of (a) about the voltage axis.

The condition for the maximum power is obtained when $\partial P / \partial V = 0$ or

$$(1 + \beta V_{mpp}) e^{\beta V_{mpp}} = \left(1 + \frac{I_L}{I_s} \right) \quad (1.4)$$

$$I_{mpp} = |I_s (e^{\beta V_{mpp} - 1}) - I_L| = I_s \beta V_{mpp} e^{\beta V_{mpp}} \quad (1.5)$$

The power conversion efficiency (PCE) is then given by

$$\begin{aligned} \text{PCE} &= \frac{\text{maximum power output}}{\text{power input}} = \frac{I_{mpp} V_{mpp}}{P_{in}} \\ &= \frac{I_L \beta V_{mpp}^2}{(1 + \beta V_{mpp})} \left(1 + \frac{I_s}{I_L} \right) \frac{1}{P_{in}} \end{aligned} \quad (1.6)$$

By defining the fill factor parameter (FF) defined as the ratio between the maximum power and the product $I_{sc} \times V_{oc}$ given by,

$$\text{FF} = \frac{P_{mpp}}{I_{sc} V_{oc}} = \frac{I_{mpp} V_{mpp}}{I_{sc} V_{oc}} \quad (1.7)$$

the PCE can then be simplified in terms of the current density $J = I/A$ of a solar cell with the exposed active area A and an input power density of P_{in} as

$$\text{PCE} = \frac{J_{sc} V_{oc}}{P_{in}} \text{FF} \quad (1.8)$$

1.2.2 State-of-the-art Solar Cells

Significant effort has been allotted in the development of photovoltaic technologies to maximize the power conversion efficiencies of solar cells. The advancement in record efficiencies of research cells from various photovoltaic technologies is summarized in Fig. 1.3 [7]. Among the different technologies, a new class of emerging photovoltaics has been gaining an unprecedented rise into one of the most promising materials for solar cell applications – the perovskite solar cells. This is due to the rapid advancement in record efficiencies (25.7% for perovskite cells) already approaching the record PCEs of crystalline silicon (26.1% for single crystal without concentrator) in just over a decade of development. Most notably, the integration of perovskites with silicon photovoltaics as tandem solar cells has shown great potential in breaking the detailed balance limit of a single junction solar cell already reaching 32.5% efficiency [7, 8].

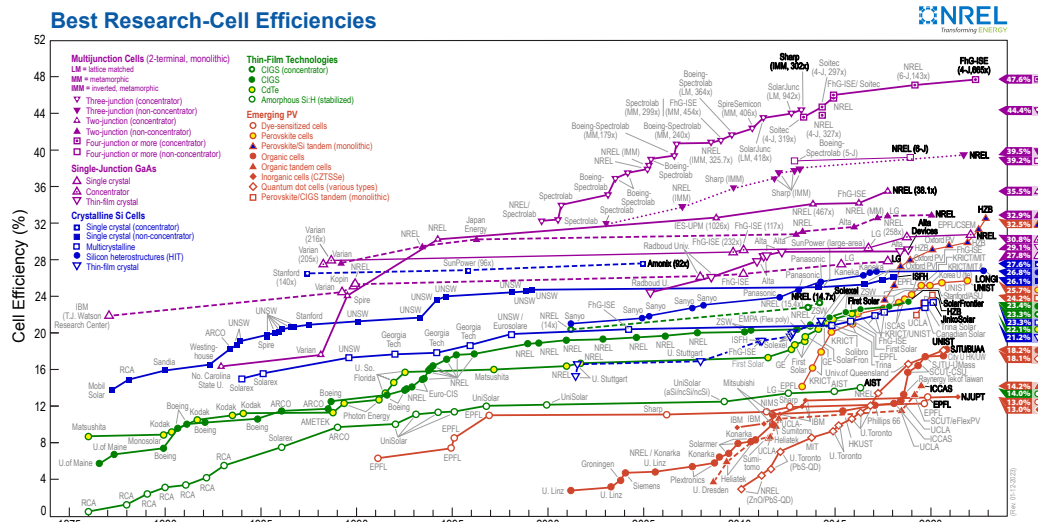


Figure 1.3: The highest confirmed power conversion efficiencies of research cells for a range of photovoltaic technologies. Certified data obtained courtesy of the National Renewable Energy Laboratory (NREL), Golden, Co. (<https://www.nrel.gov/pv/cell-efficiency.html>)

1.2.3 Perovskite Solar Cells

The term “perovskite” is the nomenclature used to describe any material that has the same crystal structure as calcium titanate (CaTiO_3) [32]. In general, the perovskite has a crystal structure of ABX_3 , where A is a monovalent cation [i.e. methylammonium ($\text{MA} = \text{CH}_3\text{NH}_3$)], B is a divalent cation (i.e. Pb^{2+}), and X is a halide anion (i.e. I^-) as illustrated in Fig. 1.4.

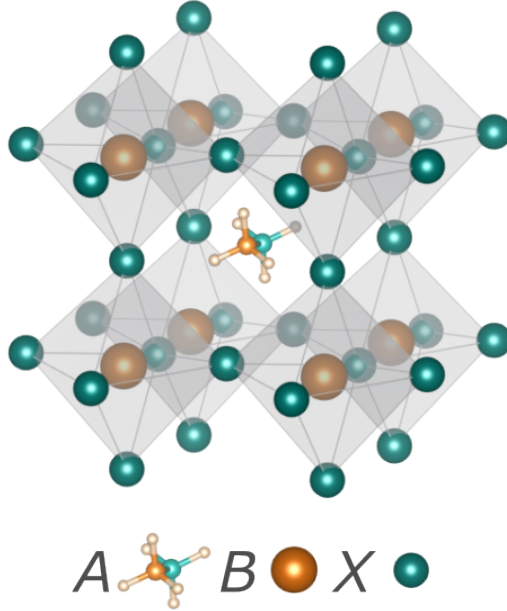


Figure 1.4: The crystal structure of a cubic ABX_3 perovskite. For methylammonium lead iodide (MAPbI_3) perovskite, A is methylammonium (CH_3NH_3 or MA^+), B is lead (Pb^{2+}) and X is iodide (I^-).

A typical perovskite solar cell is composed of a n - i - p junction where the intrinsic (i) absorber perovskite is stacked in between an n -type electron selective contact and a p -type hole selective contact as depicted in Fig. 1.5. As light, with an energy of $h\nu$, is made incident towards the solar cell, electron (e) - hole (h) pairs or excitons are generated from the photons with energies larger than the energy gap (E_g) of the perovskite semiconductor layer [31, 33]. The negatively charged electrons are photoexcited from the valence band (E_{VB}) to the conduction band (E_{CB}), leaving behind positively charged quasi-particles (holes) in the E_{VB} . Due to the energy band and Fermi level (E_{F}) alignment establishing a built-in voltage and an electric field across the device, the photogenerated carriers diffuse towards their corresponding selective transport materials. The

constant flow of the photogenerated carriers towards their respective electrodes generates current (photocurrent) which can then be extracted from the device.

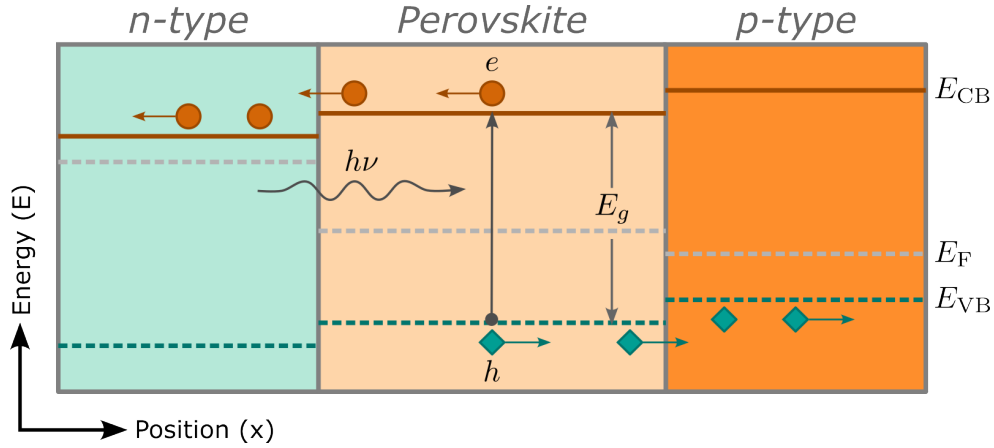


Figure 1.5: A simplified representation of the energy band diagram and the schematic flow of the photogenerated carriers in a typical perovskite solar cell.

The remarkable advancement in perovskite solar cell record efficiencies is mainly due to the exceptional optoelectronic properties. Perovskites have highly tunable, appropriate E_g (1.55 - 2.3 eV for Pb-based perovskites via compositional engineering [9, 10]), strong light absorption, and low exciton binding energy allowing for the effective generation of high-density carriers upon illumination [10]. Moreover, perovskites have high tolerance in defect or trap densities leading to low carrier recombination rates resulting to very long carrier lifetimes and large diffusion lengths of the photogenerated carriers [10]. Additionally, perovskites exhibit suppression of defect formation at the bulk/transport layer interfaces resulting to high V_{oc} . These intrinsic properties of the perovskite, in conjunction with the appropriate selection of substrates and electrode contacts, result to the efficient collection of the photogenerated carriers and high J_{sc} . With the optimization of the perovskite grain sizes, FF is also increased leading to high PCEs of PSCs. These favorable optoelectronic characteristics, in addition to the facile deposition technique via spin-coating and low annealing temperatures (~ 100 °C) [11], make the perovskite exceptional technology in photovoltaic applications.

1.3 Hysteresis in Perovskite Solar Cells

Despite the well-established protocols in measuring the efficiencies in conventional photovoltaics, PSCs exhibit a pronounced feature in the $J - V$ curves resulting to ambiguous determination of the PCEs. The standardized protocol on extracting the device efficiencies involves the $J - V$ curves measured by sweeping the voltage and measuring the current output of the cell while being illuminated by a standardized light source (air mass AM 1.5 spectrum) at 100 mW cm^{-2} irradiance. However, for perovskite solar cells, the determination of the efficiencies with conventional methods is subjected to significant ambiguity due to the phenomenon of dynamic hysteresis in the $J - V$ curve measurement [34]. Hysteresis occurs when the $J - V$ curve varies depending on the scan direction or the scan rate used [35–37] as shown in Fig. 1.6. These scan direction- and scan rate-dependent variations in the $J - V$ curve measurements in PSCs result to differences in the extracted photovoltaic parameters leading to inconsistent calculated PCEs of the same device. This inconsistency in determination of efficiency in PSCs makes the assessment of the device performance questionable.

1.3.1 Types of Hysteresis and Ionic Transport

The hysteresis in PSCs occurs in scan direction- and scan rate-dependent $J - V$ curves. They are generally classified into two main types – (i) *normal* and (ii) *inverted* hysteresis as illustrated in Fig. 1.6. The PSCs with higher current levels in the reverse scan compared to the forward scan direction exhibit normal hysteresis (Fig. 1.6a). This discrepancy in the scan direction-dependent $J - V$ curves results to the reverse scan having higher calculated PCEs than the reverse scan. Moreover, the current levels decrease as the scan rate increases for PSCs exhibiting normal hysteresis (Fig. 1.6c). In contrast, PSCs with different formulations can have higher current levels in the forward scan than the reverse scan direction depicting inverse hysteresis (Fig. 1.6b) [38, 39]. Correspondingly, the scan rate-dependent $J - V$ curves exhibit increasing current levels with increasing scan rate (Fig. 1.6d). The scan direction- and scan rate-dependent hysteresis varies in magnitude as compared with the steady-state $J - V$ curve which can be obtained at infinitely slow scan rate attaining the equilibrium response.

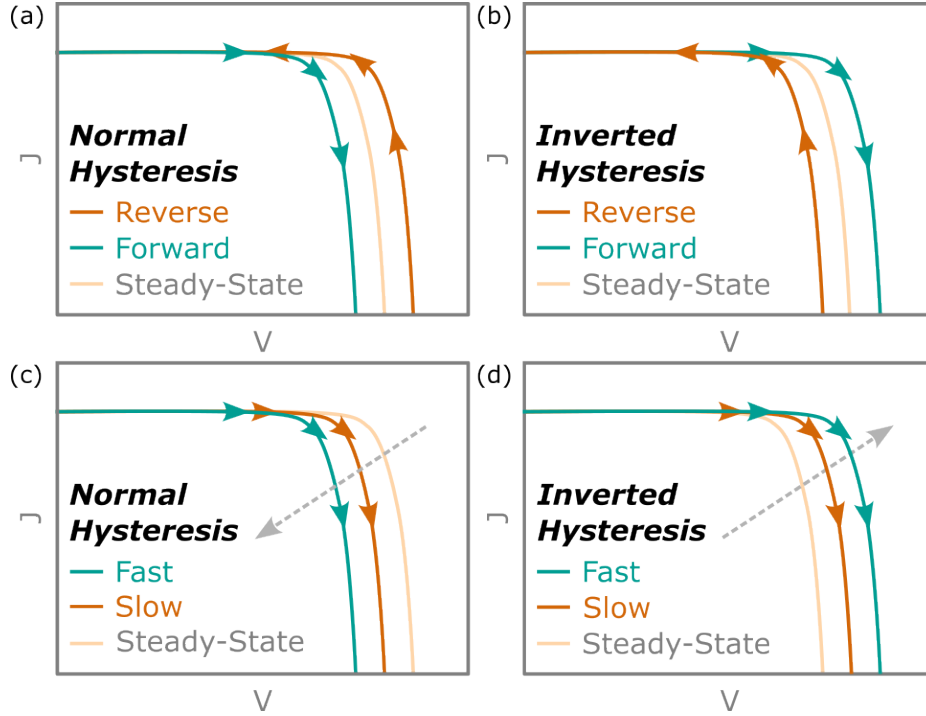


Figure 1.6: The normal-type hysteresis in the (a) scan direction-dependent and (c) scan rate-dependent $J - V$ curves. The inverted-type hysteresis in the (b) scan direction-dependent and (d) scan rate-dependent $J - V$ curves.

Ionic transport has been attributed to be one of the dominant factors contributing to these hysteretic effects in PSCs. For MAPbI_3 , under external electric field, three vacancy transport mechanisms have been identified (Fig. 1.7) – (i) I^- migration along an octahedron edge, (ii) Pb^{2+} migration along the diagonal $\langle 110 \rangle$ direction of the cubic unit cell, and (iii) MA^+ migration into a neighboring vacant A-site [40]. Notably, I^- ion vacancy (V_I^+) migration shows the lowest activation energy as compared to MA^+ ion vacancy (V'_{MA}) and Pb^{2+} ion vacancy (V''_{Pb}) indicating that the perovskites are mixed ionic-electronic conductors with I^- ions as the majority ionic carriers [40]. The migration of the vacancies under the influence of an external electric field could change the photogenerated charge collection efficiency with time resulting to the hysteresis in $J - V$ measurements [12–15]. Moreover, metal ions and dopants have also been reported to migrate into the perovskite layer further inducing hysteresis detrimental for device performance stability [14, 41–43]. Despite the remarkable progress in PSC record efficiencies, hysteresis still persists in state-of-the-art high efficiency devices with PCEs exceeding 22% [16].

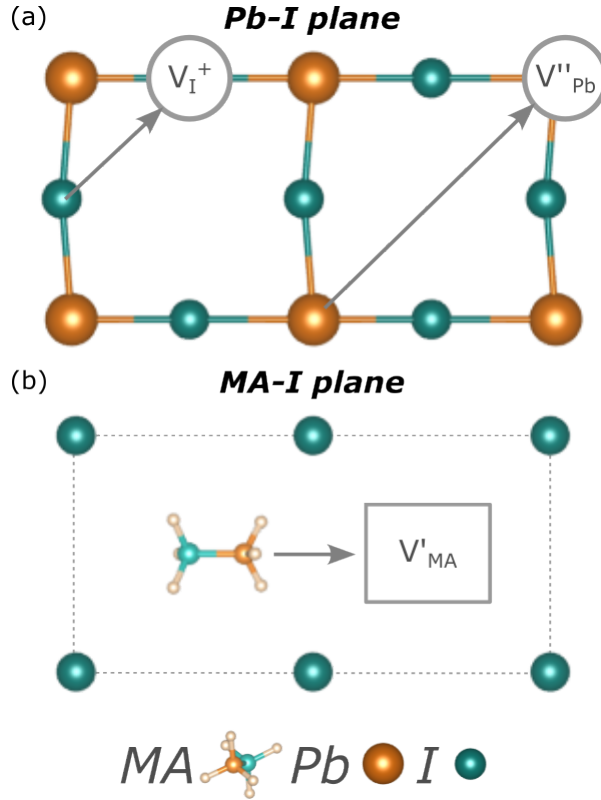


Figure 1.7: The schematic diagram of three ionic transport mechanisms involving the conventional vacancy hopping between neighboring sites: (a) I^- migration along the octahedron edge and Pb^{2+} migration along the diagonal direction $\langle 110 \rangle$; (b) MA^+ migration into a neighboring vacant A-site cage. Adapted from Eames, C. et al. Ionic transport in hybrid lead iodide perovskite solar cells. *Nat. Commun.* **6**, 7497, 2-9 (2015) used under CC BY 4.0.

1.3.2 Hysteresis and Impedance Spectroscopy

As perovskites exhibit ionic-electronic conductivity, understanding the underlying mechanisms in PSC device operation is not straightforward. A complete picture of the complex interplay between the electronic and ionic transport under operation resulting to the dynamic hysteresis effect is needed to fully characterize the PSCs. For this reason, impedance spectroscopy (IS) is used as a non-destructive electrical characterization tool for qualitative and quantitative analysis of complex material variables such as mass transport, chemical reactivity rates, dielectric properties, and compositional influences on the conductance of solids [44, 45].

Impedance spectroscopy involves the application of a small perturbation of

an oscillating voltage $\tilde{V}(\omega) = V_m \sin(\omega t)$ at a frequency $f = \omega/2\pi$ to a cell, and the resulting steady state current $\tilde{I}(\omega) = I_m \sin(\omega t - \theta(\omega))$ is measured. Here, V_m is the amplitude of perturbation, I_m is the amplitude of the steady-state current, and θ is the phase of $\tilde{I}(\omega)$ relative to $\tilde{V}(\omega)$. The impedance is then calculated given by

$$Z(\omega) = \frac{\tilde{V}(\omega)}{\tilde{I}(\omega)} \quad (1.9)$$

The impedance can then be expressed in complex form as

$$Z(\omega) = Z'(\omega) + iZ''(\omega) \quad (1.10)$$


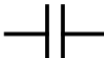

The impedance spectrum is then determined by measuring the impedance at a wide range of frequencies ranging from MHz to mHz. Analysis of the full frequency range impedance spectrum is supported by the establishment and interpretation of an equivalent circuit with idealized circuit elements. The ideal circuit elements and their corresponding impedances are tabulated in Table 1.1. The total impedance of n number circuit elements in a series combination is given by

$$Z_{\text{tot}} = Z_1 + Z_2 + \dots + Z_n \quad (1.11)$$

while the parallel combination is given by

$$\frac{1}{Z_{\text{tot}}} = \frac{1}{Z_1} + \frac{1}{Z_2} + \dots + \frac{1}{Z_n} \quad (1.12)$$

Table 1.1: Ideal circuit elements with their corresponding symbols and impedances $Z(\omega)$.

	Resistor	Capacitor	Inductor
Symbol			
$Z(\omega)$	$Z_R(\omega) = R$	$Z_C(\omega) = \frac{1}{i\omega C}$	$Z_L(\omega) = i\omega L$

A simple equivalent circuit is a resistance R in parallel to a capacitor C as illustrated in the inset of Fig. 1.8a. The corresponding impedance spectra of

the simple RC circuit with $R = 50 \Omega$, $C = 10 \mu\text{F}$ and a frequency range of 1 MHz to 1 mHz is illustrated in Fig. 1.8. The corresponding characteristic time constant of the RC circuit is given by $\tau = RC$. In the complex impedance $-Z''$ vs. Z' plot, the IS spectrum appears to have a perfectly semi-circular arc (Fig. 1.8a). In this representation, the real part of the impedance (Z') is associated to the resistive contribution, while the imaginary part (Z'') is associated to the capacitive contribution.

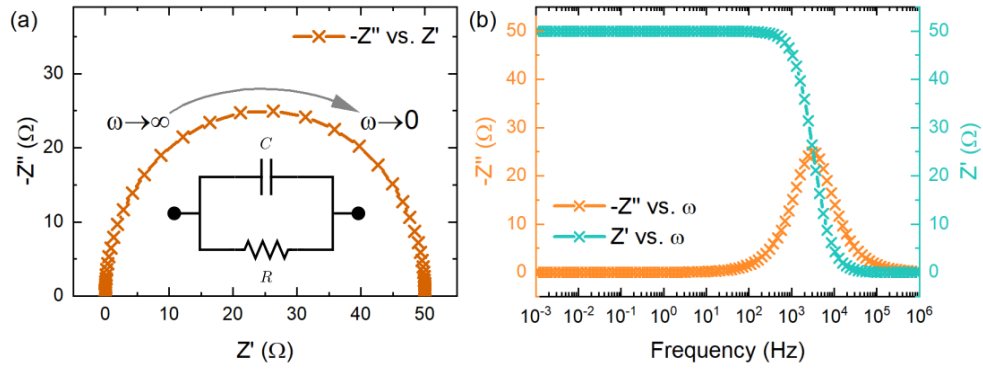


Figure 1.8: (a) Complex impedance plot with the arrow indicating the scan from high frequencies to low frequencies. (b) Frequency plot of the real and imaginary components of the impedance for a parallel RC circuit with $R = 50 \Omega$ and $C = 10 \mu\text{F}$.

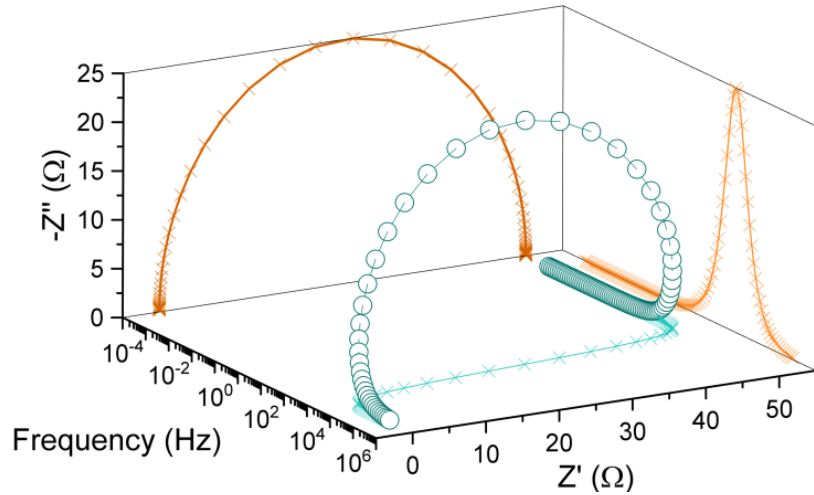


Figure 1.9: Three-dimensional complex impedance and frequency plot of the parallel RC circuit in Fig. 1.8 with the corresponding projections.

The real and imaginary parts of the impedance are also plotted against the frequency to fully represent the frequency-dependence of the impedance spectrum

as illustrated in Fig. 1.8b. The relationship among the complex impedance and frequency plots can be fully illustrated as a three-dimensional impedance plot as shown in Fig. 1.9. In practice, from the measured IS response of the devices, appropriate equivalent circuit models are implemented to extract circuit parameter values which are then correlated to physical interpretation of electronic and electrochemical processes [44, 45].

In PSCs, the IS measurements are conducted at an applied direct current (DC) voltage (V_{DC}) and the impedance is calculated from the corresponding current response. In order to understand the underlying mechanisms in PSCs under device operation, IS is measured at quasi-steady state conditions, i.e. at open circuit or short circuit conditions as schematically illustrated in Fig. 1.10 [45, 46]. The impedance is calculated from the total applied voltage of $V(\omega) = V_{DC} + \tilde{V}(\omega)$, and the total current response of $I(\omega) = I_{DC} + \tilde{I}(\omega)$. The perturbation amplitude V_m is chosen to be very low that the current-voltage relations are virtually linear at low applied voltages [47].

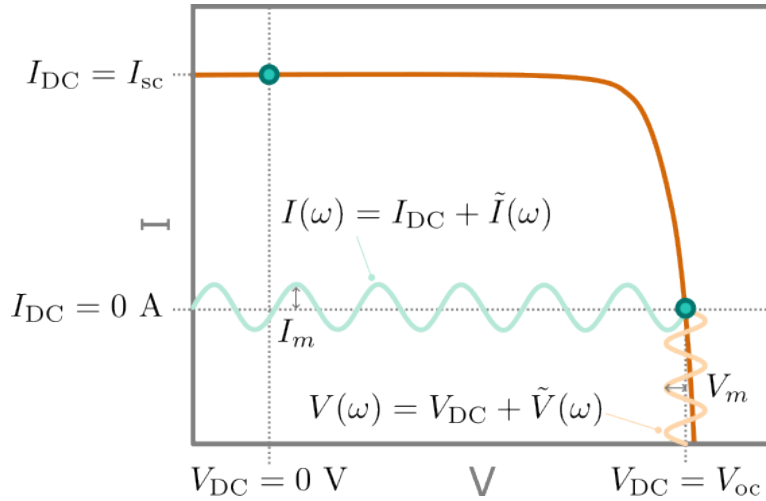


Figure 1.10: The schematic diagram of the IS measurements in PSCs under quasi-steady state conditions, i.e. open circuit or short circuit conditions (indicated by the green dots).

The IS spectra of PSCs vary considerably depending on the device architecture, composition, measurement conditions, and measurement protocols. The complex impedance plots of PSCs under steady state conditions (illuminated or dark) typically exhibit two distinct arcs – the high frequency (HF) and low frequency (LF) arcs as shown in Fig. 1.11a. These impedance features vary in

radius, relative magnitudes, may be convoluted, and may be partially resolved depending on the frequency range of the measurement. In general, the HF arc is attributed to the bulk electronic transport while the LF arc is attributed to electrochemical dynamics at the perovskite/contact interfaces [46, 48–50]. Notably, both arcs are in the first quadrant of the complex impedance plane (negative Z'' values) corresponding to positive capacitances as calculated from the real part of the complex capacitance given by

$$C(\omega) = \frac{1}{i\omega Z(\omega)} \quad (1.13)$$

This is explicitly observed in the capacitance-frequency ($C - f$) plot as shown in Fig. 1.11b. Further information can be extracted from the frequency-dependence of the capacitances, in conjunction with the equivalent circuit fitting and analysis calculated from the IS spectrum.

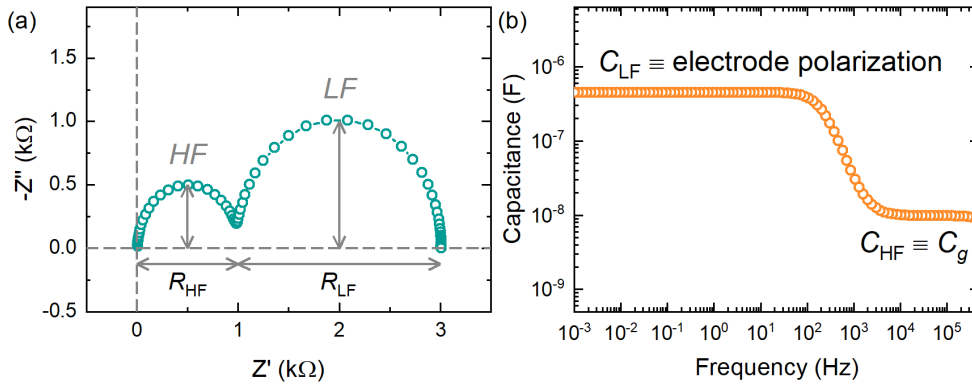


Figure 1.11: (a) Typical complex impedance spectrum of PSCs under steady state conditions exhibiting two distinct arcs – the high frequency (HF) and low frequency (LF) arc. (b) The corresponding capacitance vs. frequency ($C - f$) plot of the IS spectrum calculated from the real part of $C(\omega) = 1/i\omega Z(\omega)$.

The equivalent circuit model that has been amply used to analyze and interpret the IS response of PSCs exhibiting two distinct well-defined capacitive arcs is illustrated in Fig 1.12 [45, 51]. This equivalent circuit comprises of two resistors (R_{HF} and R_{LF}) and two capacitors (C_{HF} and C_{LF}) labeled accordingly. The HF and LF capacitances are untangled and are typically associated to the high frequency limit or geometric capacitance (C_g) and electrode polarization due to surface charge accumulation of ions at the interfaces, respectively [52]. Correspondingly, a shorter time constant τ_{HF} and a longer time constant τ_{LF} is

observed for the HF and LF RC pairs, respectively, provided that $C_{LF} \gg C_{HF}$ [51]. The time constants provide valuable information on the time scales of the processes occurring within the PSCs under device operation. The LF capacitance, with a corresponding longer τ_{LF} , is consistently observed for reported PSCs exhibiting normal hysteresis [52, 53].

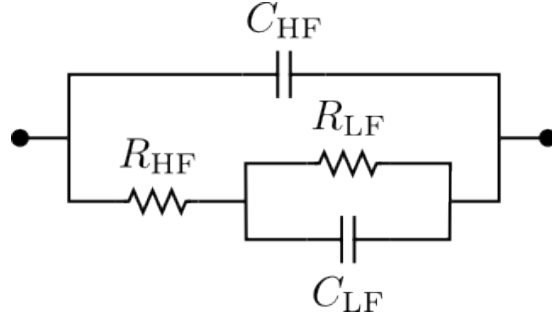


Figure 1.12: Equivalent circuit model typically used to analyze and interpret IS response of PSCs with two distinct well-defined arcs.

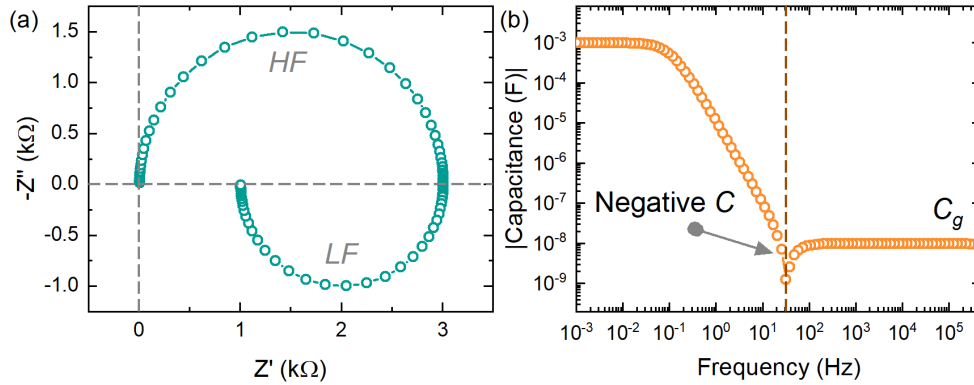


Figure 1.13: (a) The complex impedance plot of an IS spectrum exhibiting a LF negative capacitance arc. (b) The corresponding $C - f$ plot of the IS spectra with the absolute value capacitances indicating the point of inflection where the capacitance becomes negative.

As IS measurements have been implemented in various device configurations, perovskite formulations and different measurement conditions, distinct LF features are observed. One of the unusual LF feature observed in PSCs is the appearance of a negative capacitance (or inductive) arc [54–58]. In this case, the HF arc starts in the first quadrant of the complex impedance plot but the LF response crosses the fourth quadrant manifesting as a negative capacitance arc as illustrated in Fig. 1.13a with the corresponding absolute value $C - f$ plot

in Fig 1.13b. These negative capacitance arcs or inductive features have been attributed to a slow kinetic process upon ion displacement in the presence of electric field [54–56]. Interestingly, these inductive features also appear in the IS response of PSCs exhibiting inverted hysteresis [57, 58].

The persistence of hysteresis in PSCs has been critically related to device operational stability under dark and illuminated conditions [15, 17]. Hence, understanding the underlying mechanisms in this phenomenon is of paramount importance in the further development of PSC technology towards commercialization. Numerous approaches in device engineering have been developed to achieve hysteresis-free PSCs and suppress ion migration to improve the intrinsic stability of devices [59–61]. Remarkably, another completely different technology requires a strong hysteretic effect that would take advantage and embrace the intrinsic ionic-electronic conductivity of perovskites to emulate brain-like functions for in-memory and neuromorphic computing – the *memristors*.

1.4 Hysteresis and Memristive Systems

The concept of memory can be defined as the ability to store the state of a system at a given time, and access such information at a later time [62]. This history-dependent change of state property is exhibited by emerging memory devices when subjected to time-dependent perturbations, more specifically the resistance in memristive systems [63–65]. A memristive device is a two-terminal structure which undergoes a voltage- or current-controlled conductance variation depending on the history of the applied stimuli [62]. The distinctive signature of memristive devices is a hysteresis loop in the $I - V$ curve as illustrated in Fig. 1.14. This memory response may be “*self-crossing*” (Fig. 1.14a) related to a nonvolatile memory or “*not self-crossing*” (Fig. 1.14b) related to a volatile memory which will be discussed in a later section.

This nonlinear dynamic memristive response can be described by the time-dependent equations given by [62, 66]

$$I(t) = G(x, V, t)V(t) \tag{1.14}$$

$$\frac{dx}{dt} = f(x, V, t) \tag{1.15}$$

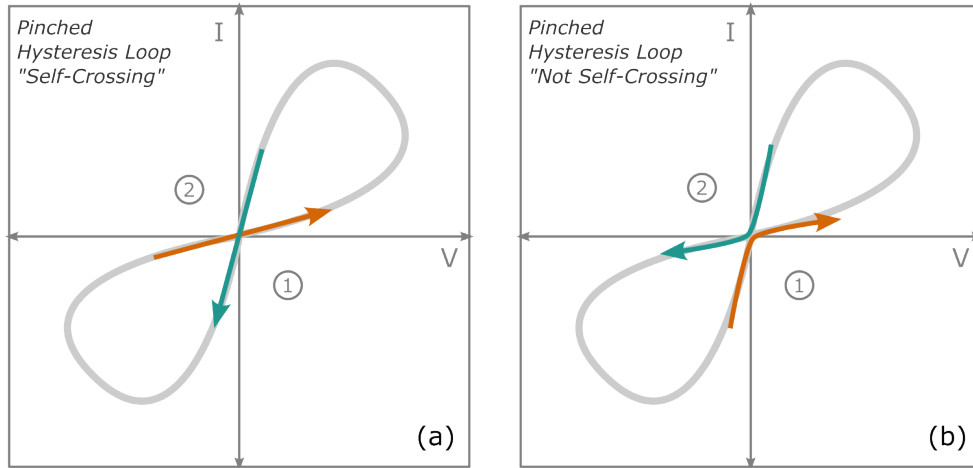


Figure 1.14: The pinched hysteresis loop of memristive devices when subjected to periodic stimulus. This memory response can be (a) “self-crossing” or (b) “not self-crossing”.

where $I(t)$ and $V(t)$ are the current and the voltage across the device, x is the set of n possible internal state variables related to the particular device, f is a continuous n -dimensional vector function, and G is the memory conductance or *memductance*. These systems are called the *voltage-controlled memristive systems* [62–65]. In this case, the response of the current $I(t)$ does not only depend on the voltage across the device, but also on one or more pertinent internal state variables that determine the state of the system at any given time. Moreover, the change of state of the system is not instantaneous to the applied stimulus, but rather, it generally depends on the past dynamics. Irrespective of the underlying physical mechanisms of the memristive systems, at a certain low frequency periodic stimulus, the change in conductivity of the system can be observed making the device behave like a nonlinear resistor [62].

1.4.1 Memristive Devices and Resistive Switching

As the focus on memory technology advances, memristive response (hysteretic $I - V$) has been demonstrated in various device configurations. This memristive response, denoted as *resistive switching*, is defined as the reversible phenomena of two-terminal elements which changes the resistance upon electrical stimuli [20, 64]. The underlying physical mechanisms of the resistive switching and the nature of the internal state variable vary from each system and de-

vice configuration. These systems of emerging memory technology show unique types of memristive response relying on the physics of the active materials. Four emerging two-electrode technologies have attracted considerable attention due to their unique resistive switching properties – (i) resistive random access memory (ReRAM), (ii) phase change memory (PCM), (iii) ferroelectric random access memory (FeRAM), and (iv) spin-transfer torque magnetic random access memory (STT-MRAM). Fig. 1.15 summarizes the main emerging memory technologies of two-terminal memory devices and their corresponding switching responses.

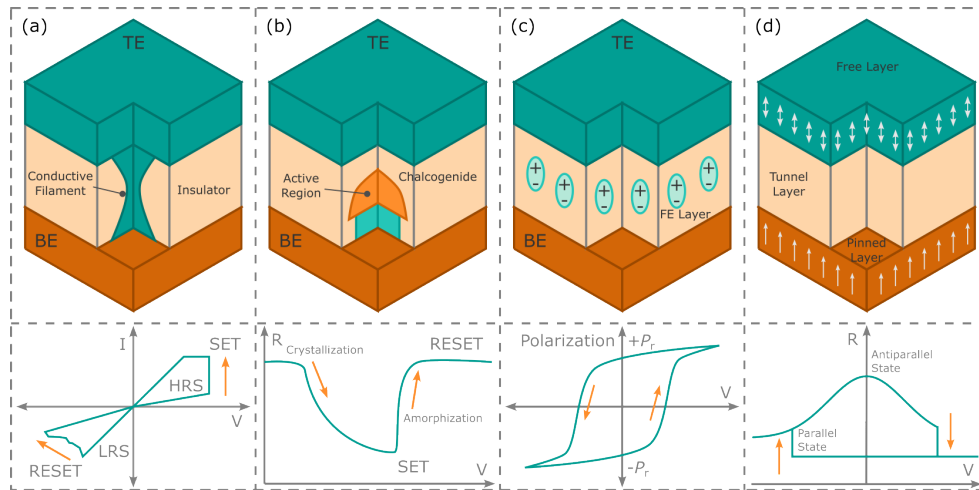


Figure 1.15: Schematic diagrams of the two-terminal emerging memory technologies – (a) resistive random access memory (ReRAM), (b) phase change memory (PCM), (c) ferroelectric random access memory (FeRAM), and (d) spin-transfer torque magnetic random access memory (STT-MRAM).

Resistive Random Access Memory (ReRAM)

The schematic diagram of the resistive random access memory (ReRAM), or more commonly known as memristor, is illustrated in Fig. 1.15a. The ReRAM consists of a metal-insulator-metal (MIM) configuration with the insulating layer acting as the switching material [20, 64]. The bottom electrode (BE) is typically composed of relatively inert metal, such as Pt or TiN, while the top electrode (TE) is composed of a wide range of a more reactive metal, such as Ti and Ta [67–71]. The switching layer can be composed of a wide variety of materials ranging from metal oxides [67–71], nitrides [72–74], chalcogenides [75], 2D materials [76], and organic materials [77, 78]. The resistive switching mechanism

for ReRAMs is the formation of conductive filaments (CF) across the switching material under applied external voltage switching the device from a high resistance state (HRS) or OFF state to a low resistance state (LRS) or ON state. This transition is reversed by applying a characteristic external voltage (either same or opposite polarity). In addition, nonfilamentary resistive switching has also been reported for devices exhibiting gradual resistive switching [79, 80].

Phase Change Memory (PCM)

The schematic diagram of the phase change memory (PCM) device is illustrated in Fig. 1.15b. The resistive switching mechanism of PCM relies on the ability of the phase change material to reversibly switch between the amorphous and crystalline phases effectively modifying the overall resistivity [81, 82]. The phase change material is typically composed of chalcogenides such as $\text{Ge}_2\text{Sb}_2\text{Te}_5$ or $\text{Ag}_5\text{In}_5\text{Sb}_{60}\text{Te}_{30}$ [81, 82]. The resistive switching is facilitated by the phase transition under the applied external voltage via Joule heating. Due to the temperature-dependent switching phenomenon, device operation is highly inefficient compared to other emerging memory technologies [81].

Ferroelectric Random Access Memory (FeRAM)

The schematic diagram of the ferroelectric random access memory (FeRAM) is illustrated in Fig. 1.15c. The resistive switching mechanism of FeRAM relies on the ability of the ferroelectric (FE) layer to maintain an electric polarization upon application of an external voltage [83]. The FE layer of FeRAMs is typically composed of BaTiO_3 [84], $\text{PbZr}_x\text{Ti}_{1-x}\text{O}_3$ [85] and HfO_2 [86]. Instead of changing the device overall resistance, the individual ferroelectric dipoles are reoriented changing the charge induced on the metallic electrodes. The application of a positive voltage leads to dipole reorientation with positive remnant polarization (P_r), while a negative voltage results in a negative remnant polarization ($-P_r$). However, FeRAM is measured by probing the displacement current during the ferroelectric switching that requires destructive characterization technique [5].

Spin-Transfer Torque Magnetic RAM (STT-MRAM)

The schematic diagram of the spin-transfer torque magnetic random access memory (STT-MRAM) is illustrated in Fig. 1.15d. STT-MRAM consists a magnetic tunnel junction (MTJ) composed of a thin insulator sandwiched in between two ferromagnetic (FM) materials. One of the FM layer has its ferromagnetic polarization pinned by the presence of adjacent magnetic layers, hence, acting as a reference for polarization. The other FM layer is free which can change its polarization under applied external voltage. The resistive switching mechanism relies on the magnetization of the free layer by applying current across the MTJ via spin torque resulting to either a parallel state (relatively low resistance) or an antiparallel state (relatively high resistance) [87, 88]. However, the resistance window is generally quite narrow making multistate operation difficult to achieve [20].

1.4.2 Comparison of Emerging Memory Technologies

The implementation of these emerging devices for memory applications are determined by the performance characteristics for storage and logic capabilities. Depending on these characteristics, each device shows different suitability of these devices for neuromorphic computing schemes, such as deep neural network (DNN) and spiking neural network (SNN). These performance characteristics can be classified as the following [20, 89, 90]:

- **Multilevel operation.** The number of measurable and relatively stable charge or current states. A bit represents two logic states – “0” or “1”.
- **Write voltage.** The applied voltage required to set the device state or the “write” process. The writing operation may be called the *store* operation.
- **Write time.** The time required to effectively promote the write process or the to store the information.
- **Read time.** The time required to effectively measure or sense the state of the device, “read” process, at a specific read voltage. The reading operation may be called the *recall* operation.

- **Write energy.** The energy required to store one bit.
- **Linearity.** The linearity of the conductance or weight changes based on the electrical stimulus.
- **Integration density.** The potential number of memory devices that can be integrated within a single chip.
- **Retention.** The elapsed time between data storage and the first erroneous readout of the data.
- **Endurance.** The minimum number of write-read cycles that the device can withstand.

Table 1.2: Comparison of different emerging memory technologies suited for in-memory computing. Adapted from Ielmini, D. and Ambrogio, S. Emerging neuromorphic devices. *Nanotechnology* **31**, 9 (2020) used under CC BY 3.0.

Technology	ReRAM	PCM	FeRAM	STT-MRAM
Multilevel operation	multibit	multibit	1 bit	1 bit
Write voltage (V)	<3	<3	<3	<1.5
Write time (ns)	<10	~50	~30	<10
Read time (ns)	<10	<10	<10	<10
Write energy (J/bit)	0.1 - 1 pJ	~10 pJ	~100 fJ	~100 fJ
Linearity	Low	Low	None	None
Integration density	High	High	Low	High
Retention	Medium	Long	Long	Medium
Endurance	10^5 - 10^8	10^6 - 10^9	10^{10}	10^{15}
Suitability for DNN training	Low	Low	No	No
Suitability for DNN inference	Moderate	Yes	No	No
Suitability for SNN algorithms	Yes	Yes	Yes	Moderate

A comparison of the performance characteristics of these emerging devices is summarized in Table 1.2 [20, 90]. Both FeRAM and STT-MRAM have exceptional endurance cycles with low write energies. However, both are limited to only 1 bit operation making them suitable for digital computing schemes with SNN integration. On the other hand, ReRAMs and PCMs possess multilevel operations with considerable endurance cycles and write energies. Moreover, these devices exhibit nonlinear switching and multilevel conductance tuning making them suitable for DNN and SNN implementations. However, due to the temperature-dependent switching in PCMs, device operation is more inefficient

as compared to other emerging technologies making ReRAMs promising candidates for further development.

1.4.3 Resistive Switching Types of ReRAMs

As the ReRAM technology promises exceptional memory properties suited for in-memory computing with significantly low energy consumption, considerable effort has been focused on the development of these memristor devices and their switching response. The type of resistive switching of memristor devices can be classified depending on the hysteretic $I - V$ response. The characteristic $I - V$ response is essential for obtaining the pertinent device performance parameters for different operation application modes. More specifically, for ReRAMs, the switching process entails the transition from a high resistance state (HRS) or ON state to a low resistance state (LRS) or ON state at a specific threshold voltage (V_{th}). This transition from the OFF to ON states is called the SET process. In contrast, the transition from the ON to OFF states at another specific threshold voltage is called the RESET process. The two most common resistive switching types reported in literature are bipolar resistive switching and threshold resistive switching [64, 91]. The schematic characteristic $I - V$ curves of the most common resistive switching types are illustrated in Fig.1.16.

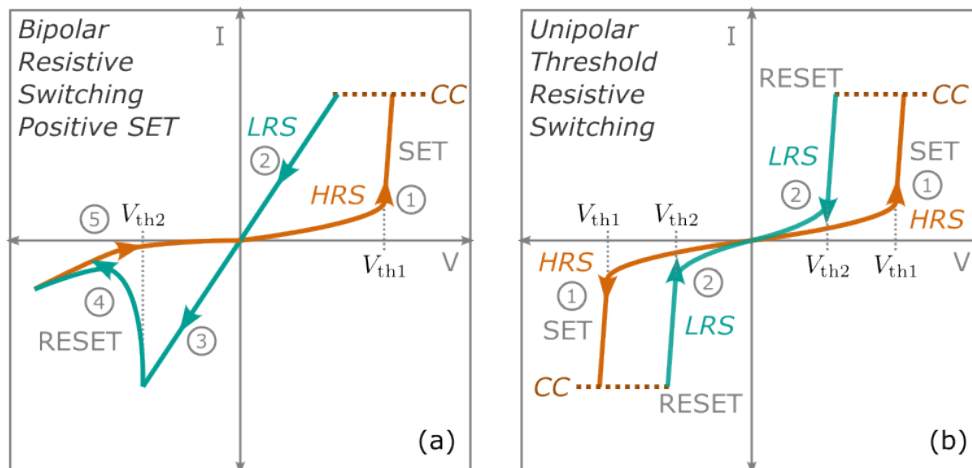


Figure 1.16: Types of resistive switching based on the $I - V$ response – (a) bipolar RS with positive SET process and (b) threshold RS with the arrows indicating the scan direction and sequence.

Bipolar Resistive Switching

The bipolar resistive switching (BRS) type involves the SET process from the HRS to the LRS occurring at a certain threshold voltage V_{th1} with the RESET process occurring at a threshold voltage V_{th2} in the opposite polarity. The BRS type memristor devices can exhibit either a positive SET with a negative RESET (Fig. 1.16a) or a negative SET with a positive RESET. A compliance current (CC) is typically implemented in the SET process in order to prevent irreversible switching breaking down the device under operation. The CC, in conjunction with the voltage measurement range, is selected to allow reversible and reproducible RS for optimized device operation. The BRS type devices are considered to have *nonvolatile memory* where the ON state current is maintained upon the removal of the applied external voltage.

Threshold Resistive Switching

On the other hand, the threshold resistive switching type involves the SET and RESET processes occurring at the same polarity. The SET process from HRS to LRS takes place at a certain V_{th1} , however, the RESET process occurs at the reverse scan direction at a lower V_{th2} in the same polarity as the SET process. A CC is also implemented to avoid device breakdown. Similarly, the threshold switching devices can exhibit SET and RESET processes in either the positive or negative polarities (Fig. 1.16b). The threshold switching type devices are considered to have *volatile memory* where the ON state relaxes back to the OFF state upon the removal or sufficient decrease of the applied external voltage.

1.4.4 Memristor Performance Parameters

Based on the characteristic $I - V$ response, the major performance parameters are determined. The $I - V$ curves are typically plotted in the semilog $\log |I|$ vs. V scale for the parameters to appear more pronounced. The representative $\log |I| - V$ curve of a BRS type ReRAM device is schematically presented in Fig. 1.17a. The performance parameters of ReRAM devices are the following:

- **Current states.** The current levels of the HRS (I_{HRS} or I_{OFF}) and LRS (I_{LRS} or I_{ON}) directly identified from the $I - V$ curve.

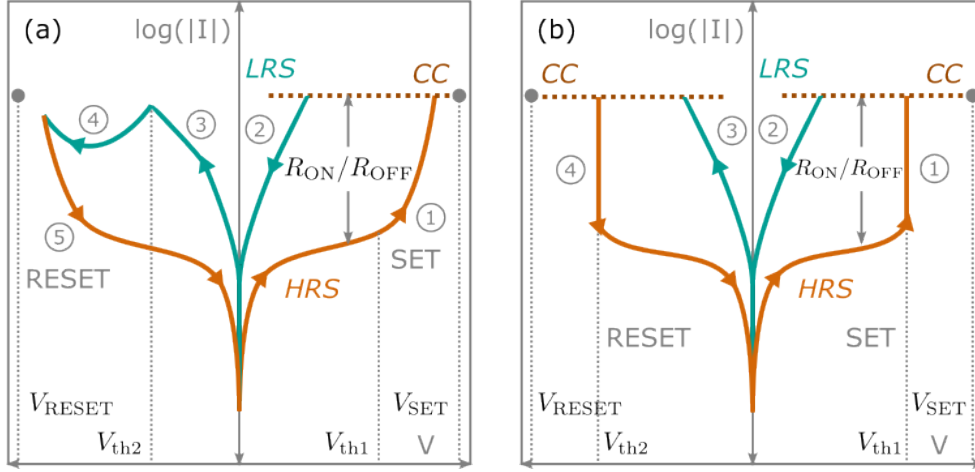


Figure 1.17: The performance parameters determined from the characteristic $I - V$ curve of BRS type memristors in the $\log |I|$ vs. V scale exhibiting (a) gradual and (b) abrupt SET processes. The arrows indicate the scan direction and sequence.

- **Resistance states.** The corresponding resistance values of the HRS (R_{HRS} or R_{OFF}) and LRS (R_{LRS} or R_{ON}). These resistances can be directly measured or calculated from the differential resistance given by $R = dV/dI$.
- **ON/OFF ratio.** The resistance ($R_{\text{ON}}/R_{\text{OFF}}$) or current ($I_{\text{ON}}/I_{\text{OFF}}$) ratio between the ON state and the OFF state.
- **SET voltage V_{SET} .** The external voltage required to promote the SET process with $V_{\text{SET}} > V_{\text{th1}}$
- **RESET voltage V_{RESET} .** The external voltage required to promote the RESET process with $V_{\text{RESET}} < V_{\text{th2}}$ for BRS and threshold RS.
- **Endurance.** The number of switching cycles the device can endure until the ON/OFF becomes undistinguishable or fatigues to an unacceptable value.
- **Switching speed.** The shortest duration of an applied external voltage pulse at V_{SET} to promote the SET process from HRS to LRS.
- **Retention time.** The time for which the ON or OFF state is maintained without an applied external voltage subsequently after the SET or RESET process, respectively.

- **Gradual or abrupt switching.** The manner in which the SET or RESET process occur. A *gradual* switching occurs when the SET or RESET process occurs continuously while an *abrupt* switching occurs when the SET or RESET process occurs instantly (Fig. 1.17b).
- **Operation energy per bit.** The energy required to promote the SET process of the ReRAM calculated from $E = qV = qIR$.
- **Scalability.** The geometrical size to which a ReRAM device can be miniaturized before it reaches intrinsic physical limits.
- **Two-state storage / binary switching.** ReRAM exhibiting two distinct states – the HRS (OFF state assigned to logic “0” state) and the LRS (ON state assigned to logic “1” state).
- **Multilevel or multistate storage / analog switching.** The ability of the ReRAM to attain different resistance or current states depending on the applied V_{SET} , V_{RESET} or current compliance (CC).
- **Threshold switching.** ReRAM exhibiting threshold resistive switching where the ON state relaxes to the OFF state upon the removal or sufficient decrease of the applied external voltage.

1.4.5 Memory Applications

The memristive response of ReRAMs allows *in-situ* computation where the data is located at the same time [5, 6, 18]. As the computation and memory is co-located in the same device, the miniaturization of the effective device sizes results to high density network structures. This computational scheme aims to mimic the processes of the highly interconnected neurons and synapses in the human brain to achieve outstanding energy efficiency. The ReRAMs can serve as artificially intelligent hardware for data-intensive computation schemes such as big data analysis, machine learning, and neuromorphic computing (can be generalized as *in-memory computing*).

The hardware implementation in various in-memory computing frameworks depends primarily on the specific switching type and performance parameters

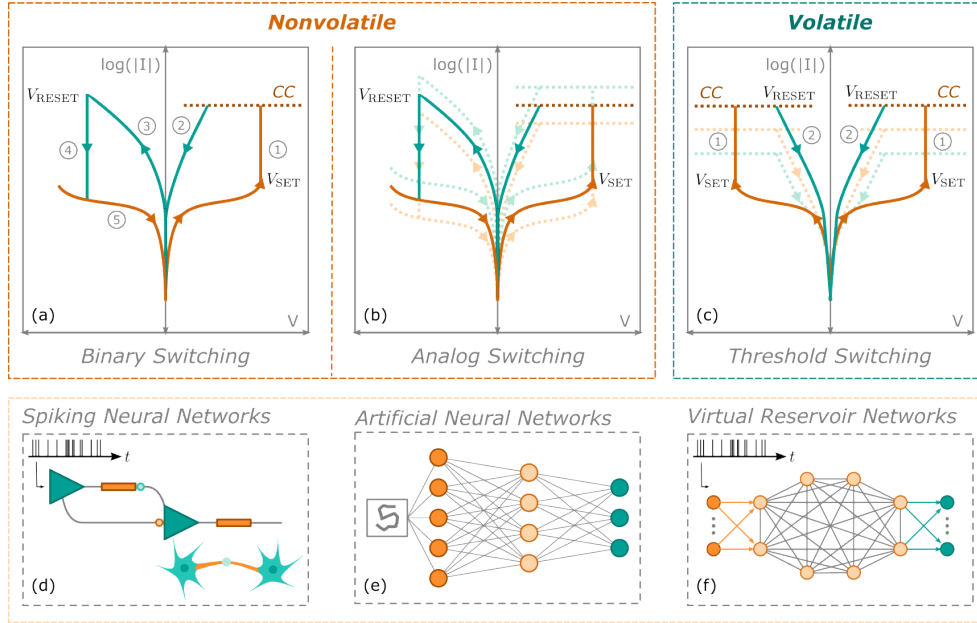


Figure 1.18: The hardware implementation of memristors with nonvolatile binary (a) and analog (b) switching, and (c) volatile unipolar switching with analog capabilities. The hardware implementation for in-memory computing of these ReRAMs depends on their switching type and performance parameters. The in-memory computing schemes can range from (d) spiking neural networks (SNN) that requires both nonvolatile and volatile memory, (e) artificial neural networks benefit from multistate nonvolatile memory, and (f) virtual reservoir networks that features volatile random weights and connections to transform sequential input data into high-dimensional dynamical state.

of ReRAMs. In order to meet these hardware specifications, the memristors are specifically designed to reflect the performance requirements of targeted in-memory computing configurations [21–23]. In general, these in-memory computing frameworks, such as artificial neural networks, spiking neural networks and virtual reservoir networks, rely on the volatility or nonvolatility of the memory devices for digital or analog computing systems as schematically summarized in Fig. 1.18.

Memristor devices exhibiting two-state (binary) and multistate (analog) bipolar switching are considered to have nonvolatile memory as shown in Fig. 1.18a and Fig. 1.18b, respectively. On the other hand, memristor devices exhibiting threshold resistive switching can also exhibit analog switching and are considered to have volatile memory (Fig. 1.18c). Both memory modes operating at multiple timescales (from tens of milliseconds to hours) are required in state-of-the-art

spiking neural network (SNN) models [92–94]. In SNNs, the two terminals of the ReRAM device act as the neurons while the conductance of the switching layer acts as the synaptic weights. The memristor network is implemented as a neuromorphic system where the information is exchanged among the neurons in the form of temporal spikes (Fig. 1.18d). The relative timing between the pre- and post-spikes changes the synaptic weight/conductance, called the synaptic plasticity. Several plasticity rules have been demonstrated that requires both the nonvolatile (long-term plasticity) and volatile (short-term plasticity) memory properties of the memristors [92–95].

Another in-memory computing scheme that requires nonvolatile multilevel switching and linear conductance response is the artificial neural networks (ANN) [96, 97]. In this scheme, the nonvolatile memory devices are employed as the synaptic weight element for on-chip acceleration during the training stage in an deep neural network (DNN) [98, 99]. Fig. 1.18e schematically illustrates a fully connected neural network for image classification with three synaptic layers. Every layer consists of memristors in a cross-bar array configuration executing matrix-vector-multiplication (MVM) where synaptic weights are mapped in the conductance matrix. Each programmable matrix element’s top and bottom electrodes are connected to common columns and rows, respectively. The vector multiplication is executed physically in the analog domain by the application of a voltage V_j at the j th column resulting in a current I_i at the i th row connected to ground given by,

$$I_i = \sum_j^N G_{ij} \cdot V_j \quad (1.16)$$

where G_{ij} is the conductance of the memristor at the position i,j and N is the total number of columns. Activations are used as input vectors being mapped in several MVM synaptic layers executing the inference operation [5, 20].

Moreover, volatile memory devices provide an ideal system that can reproduce short-term-memory (STM) in neuromorphic systems exhibiting short term potentiation (conductance increase) and depression (conductance decrease) [95]. Moreover, due to their retention times, the dynamical response of volatile memories is used as a physical reservoir process in a reservoir computing (RC) network for image recognition. In general, an RC network takes a sequential input

data and transforms it into a high-dimensional dynamical state via a reservoir layer. This reservoir layer consists of a network of volatile memories with random weights and connections, hence, minimizing the need for training to the readout layer [20, 100]. The single reservoir layer subverts the complexity of multilayer gradient-descent training techniques. Compared to DNNs, RC networks make use of fewer devices taking advantage of the rich analog, dynamic response of the volatile memory devices resulting to more power efficient operation [101, 102].

1.5 Perovskite-based Memristors

Owing to their ionic-electronic conductivity exhibiting intrinsic hysteretic $I - V$ response, perovskites have been gaining considerable attention as the switching material in ReRAM devices for neuromorphic computing applications [103–109]. From the solar cell point-of-view, the memristive response exhibits an inverted hysteresis under dark conditions which has been reported in literature for PSCs [57, 58]. With the vast effort and understanding of PSCs for photovoltaic applications, implementation of perovskites as the switching material in memristor technology makes it considerably beneficial for tailored device designs for targeted in-memory computing applications.

The perovskite, as a material platform, possesses a vast range of options and combinations for memristive devices with switching physics suitable for a wide variety of neuromorphic computing architectures [24]. It has a compositional space of $>10^6$ formulations that can be further explored via a facile solution-based processing [25–28]. Moreover, the integration of low-dimensional structures [110–112], mixed formulations [113, 114], nanocrystals [22, 115] and quantum dots [116, 117] further expands the already vast degrees of freedom or internal state variables in perovskite-based memristors. In addition, the electrochemical reactivity of the mobile ion species with the top and bottom electrodes proves to be crucial in the switching type and performance of perovskite-based memristors [118–120]. The top electrode (TE) can be selected to be electrochemically non-reactive (Pt, Au) or reactive (Ag, Al, Cu, Ti), while the bottom electrode (BE) can be selected to be symmetric or asymmetric with the TE. Furthermore, intermediate buffer layers at the interface between the perovskite switching layer and

the electrodes can be incorporated as protective layers (i.e. PMMA), capping layers [117, 121], [122–124] or carrier transport layers (i.e. PCBM, PEDOT:PSS, Spiro-OMeTAD) [113, 125, 126]. A summary of the device configuration variations resulting to varying memristive responses is schematically illustrated in Fig. 1.19.

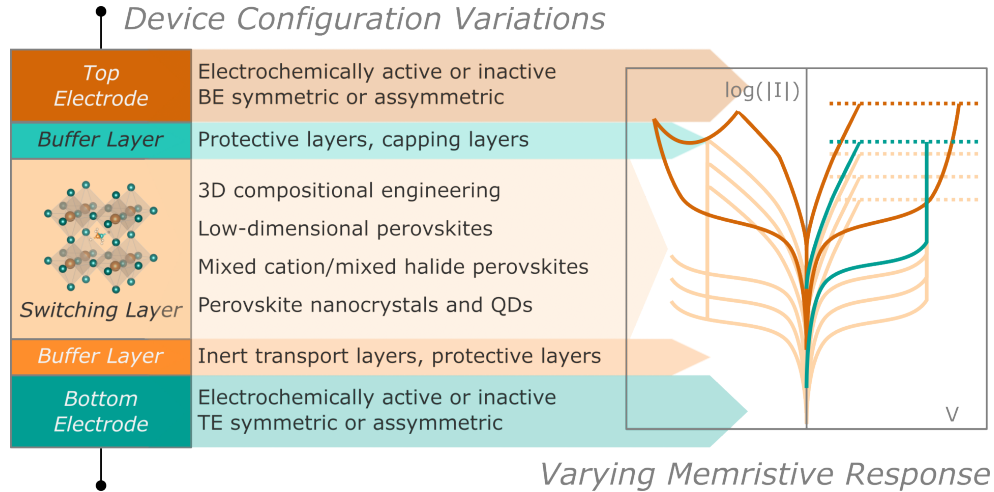


Figure 1.19: Perovskite-based memristors device configuration variations in the switching layer material, top and bottom electrode selection, and incorporation of intermediate buffer layers resulting in varying memristive responses.

1.5.1 State-of-the-Art Perovskite-based Memristors

With the increasing development of perovskite-based memristors, a wide variety of device configurations has been demonstrated to exhibit exceptional properties for in-memory applications. State-of-the-art perovskite memristors with non-volatile bipolar switching exhibit ON/OFF ratios of $\sim 10^2 - 10^9$, retention times of $\geq 10^3$ s, and endurance of $> 10^3$ cycles. In addition, volatile threshold switching memristors have been demonstrated to have multi-state memory suitable for analog applications exhibiting various synaptic functions for neuromorphic computing. The representative reported perovskite-based memristors with state-of-the-art performance parameters is summarized in Table 1.3.

Table 1.3: Summary of representative high performing perovskite-based memristors with distinct device configurations in terms of ON/OFF ratios, endurance cycles and retention times.

Configuration	ON/OFF Ratio	Endurance Cycles	Retention s
<i>Volatile Threshold Switching</i>			
Ag/MAPbI ₃ /Ag [127]	Analog	-	Synaptic
ITO/MAPbI ₃ /Au [128]	Analog	-	Synaptic
ITO/PEDOT:PSS/MAPbI ₃ /Au [27]	Analog	5×10 ²	Synaptic
FTO/CsPbBr ₃ /P3HT/Au [129]	Analog	1.2×10 ³	Synaptic
PET/ITO/MAPbI ₃ /PEAI/Au [112]	Analog	1.8×10 ³	Synaptic
<i>Nonvolatile Bipolar Switching</i>			
ITO/dimer-Cs ₃ Sb ₂ I ₉ /Au [121]	10 ²	5×10 ²	>10 ³
ITO/PEDOT:PSS/PrPr _y [PbI ₃]/PMMA/Ag [21]	10 ⁵	4.5×10 ²	>10 ⁵
ITO/Cs ₃ Cu ₂ I ₅ /PMMA/Ag [124]	10 ²	1×10 ²	>10 ⁴
Pt/(BzA) ₂ CuBr ₂ /PMMA/Ag [123]	10 ⁸	2×10 ³	>10 ³
ITO/PEDOT:PSS/MAPbI ₃ /PCBM/Ag [125]	10 ³	1×10 ³	>10 ⁴
ITO/PEDOT:PSS/MAPbI ₃ /Cu [130]	10 ⁴	3×10 ³	>10 ⁴
FTO/c-TiO ₂ /MAPbI _{3-x} Cl _x /Al [131]	10 ⁹	1.6×10 ²	>10 ³
PET/ITO/MAPbI ₃ /Au [132]	5×10 ¹	4×10 ²	>10 ⁴
FTO/(PMA) ₂ CuBr ₄ /PMMA/Ag [133]	9×10 ¹	1×10 ²	>10 ⁴
ITO/PMMA/PMMA:CsPbBr ₃ NC/PMMA/Au [115]	10 ⁶	4×10 ¹	>10 ³
FTO/TiO ₂ /MAPbI ₃ Au [134]	10 ³	3.5×10 ²	>10 ⁴
ITO/MAPbI ₃ /Au [135]	2×10 ¹	6×10 ²	>10 ⁴
PET/ITO/PEDOT:PSS/CsPbBr ₃ /Al [136]	10 ²	5×10 ¹	-
ITO/MAPbI ₃ /Ag [137]	10 ⁴	6×10 ¹	>10 ³
ITO/Cs ₃ Bi ₂ Br ₉ /Ag [138]	10 ¹	3.2×10 ³	>10 ³
Ag/MAPbI ₃ /Pt [139]	10 ⁶	1.3×10 ³	>10 ⁴
ITO/CsPbI ₃ /Ag [140]	10 ⁶	1×10 ²	-
ITO/2D DJ (3AMP)PbI ₄ /Al [111]	10 ³	1×10 ³	>10 ³
Ag/PMMA/CsSnI ₃ /Pt [122]	7×10 ³	6×10 ²	>10 ³
Si/SiO ₂ /Ti/Pt/(PEA) ₂ Cs ₃ Pb ₄ I ₁₃ /Ag [141]	10 ⁹	2.3×10 ²	>10 ³
ITO/PEDOT:PSS/(PEA) ₂ (MA) ₄ Pb ₅ I ₁₆ /PCBM/Ag [119]	10 ⁴	5×10 ²	>10 ⁵
FTO/MAPbI ₃ /Ag [142]	10 ⁶	1×10 ³	>10 ⁵
ITO/PMMA/en-doped MAPbI ₃ /PMMA/Ag [24]	>10 ³	1.2×10 ⁴	>10 ⁵

1.5.2 Perovskite-based Memristor Switching Mechanisms

As memristive response is demonstrated in a wide array of diverse designs and configurations, the underlying switching mechanism is still yet to be completely elucidated. In general, the switching mechanisms in perovskite memristors can be classified into (i) *nonfilamentary* switching, and (ii) *filamentary* switching. The application of an external voltage V_{SET} promotes switching physics specific to the device configuration from the HRS to the LRS. Depending on the resistive switching type, the application of a certain V_{RESET} (opposite polarity for bipolar switching type and a lower voltage in the same polarity for threshold switching) reversibly switches the device from the LRS back to the HRS. The

schematic diagrams of the general switching mechanisms in an ABX_3 perovskite-based memristors with a top metal electrode M is illustrated in Fig. 1.20.

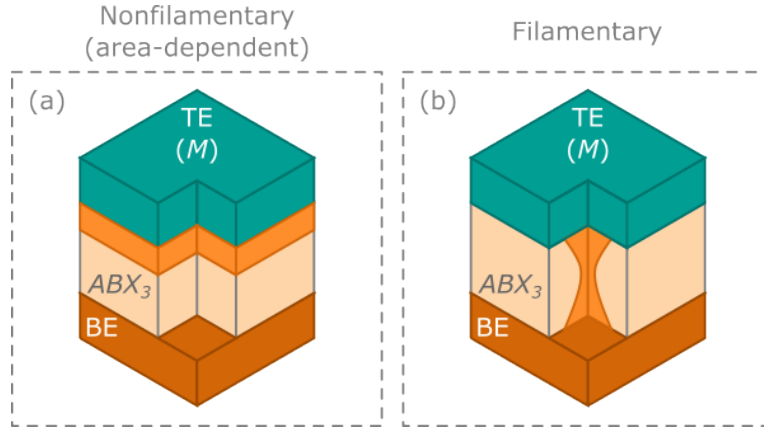


Figure 1.20: General resistive switching mechanisms in an ABX_3 perovskite-based memristors with a metal top contact electrode M exhibiting (a) nonfilamentary or area-dependent switching, and (b) filamentary switching. The nonfilamentary switching event occurs over the entire lateral plane of the switching material typically close to the contact, while the filamentary switching event occurs by the formation and dissolution of conductive filaments through the switching material.

Nonfilamentary Switching

Nonfilamentary switching entails the change in the overall device conductivity under an applied external field due to either ionic migration and redistribution [118, 132, 143], or interfacial reactivity of the migrating ion species with the top metal electrode (typically Ag) [119, 126, 127, 144, 145]. In the initial equilibrium state (FRESH state) of the device, the mobile X^- ions and the V_X^+ defects are uniformly distributed within the perovskite bulk layer (Fig. 1.20a). The application of V_{SET} promotes the motion of the ions and defects to the top and bottom electrodes, respectively, under the applied external field (drift). The accumulation of the mobile ions and defects at the perovskite/electrode interfaces considerably modifies the overall conductance of the memristor device (Fig. 1.20b) [128]. Moreover, in device configurations with Ag as the TE, the accumulation of the X^- ions at the TE interface forms metal-halide bonds (AgX) that modifies the injection properties of the TE consequently reducing the charge transfer resistance (Fig. 1.20c) [117, 119, 144, 146]. The implementation of the

CC prevents the permanent formation of the MX bonds/thin layers allowing the reversible process at V_{RESET} back to the HRS/OFF state (Fig. 1.20f).

Filamentary Switching

Filamentary switching entails the formation and rupture of conductive filaments (CF) within the perovskite layer under the influence of the applied external field. The CF can consist of either the halide vacancies V_{X}^+ (valence change mechanism) or the activated metal ions (M^+) (electrochemical metallization) [64]. From the FRESH state of the device, the ions and vacancies migrate towards their corresponding electrodes accumulating at the perovskite/electrode interface. Continuous application of the external field causes the further diffusion of the V_{X}^+ -rich towards the BE eventually forming a vacancy conductive filament bridging both electrodes (Fig. 1.20d) [117, 118, 127, 137]. In contrast, device configurations with Ag as the TE, again forms the AgX bonds/thin film activating the Ag^+ ions. The activated Ag^+ ions become mobile and diffuse through the perovskite layer towards the BE. The continuous application of the electric field eventually forms the metallic filament bridging both electrodes (Fig. 1.20e) [76, 114, 122, 147–151]. Similarly, the implementation of the CC prevents the permanent formation of the CFs allowing the reversible process at V_{RESET} back to the HRS/OFF state. However, as the memristive response is demonstrated in a wide variety of device designs and configurations, the a complete picture of the switching mechanism is yet to be fully elucidated.

1.6 Application Horizon

With the flexibility of perovskite structure as the switching material platform, it possesses a broad range of switching physics suitable for a wide variety of neuromorphic computing platforms. In-memory computing architectures can exploit not only the distinct ionic-electronic conductivity of perovskites as synaptic hardware, but also their optical properties that can generate photocurrent. Due to this optical property, perovskite-based memristive devices have also been demonstrated as photosynaptic devices for artificial visual-perception system, neuromuscular systems, pupil reflex, and light-sensitive optogenetic applications

[112, 113, 127, 152–154]. In general, the application of memristors for in-memory and neuromorphic computational schemes is highly dependent on their specific memristive responses. However, the current approach of optimizing memristors specific to a single switching requirement impede the possibility of integrating multiple computational schemes for a more complex implementation of neural network architectures all in a single processing unit. Hence, understanding and controlling the resistive switching mechanism in perovskite-based memristors would allow for tailored device design for specific and more complex computational platforms.

A complete picture of the underlying mechanisms in the kinetics of ionic motion within the full device configuration is paramount to tailor design memristors with versatile performance parameters and switching properties. As the ON/OFF ratio is calculated from the difference in the HRS and the LRS upon switching, the control of the ON/OFF ratio is not straightforward. In the HRS prior to the switching, the current levels are dictated by the overall resistance/conductivity of the device configuration. This can range from the perovskite formulation, incorporation of buffer layers, integration of two-dimensional structures, dopants, mixed formulations, and nanocrystals, to individual layer thicknesses and their corresponding resistances. Moreover, as the memristive response is measured by the total current, the effective device dimensions also play an important role in directly comparing the current levels of different systems. On the other hand, the current levels of the LRS are dictated by the switching types (volatile or nonvolatile) and mechanisms. The switching process can be either gradual or abrupt with the mechanisms define the resulting LRS and how strongly or weakly the device is activated as compared to the HRS. Hence, a more in depth understanding of the complex interplay among these factors under different stimuli is of utmost importance to have a more comprehensive understanding of the carrier and ion dynamics resulting to the switching properties in reconfigurable memristive systems.

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Chapter 2

Critical Overview

The advancement of perovskite materials as promising candidates in both the solar cell and computing technologies relies fundamentally on the hysteresis control in the $I - V$ response in order to break through the theoretical and physical limits of their corresponding fields. In the case of perovskite solar cells (PSCs), minimizing the $I - V$ hysteresis is crucial for the device's long-term stability and degradation requirements to meet the standards, such as the International Electrotechnical Commission (IEC) standards, for commercialization and integration in tandem solar cells approaching the theoretical efficiency limits [1, 2]. On the other hand, controlling the resistive switching (hysteresis effect) allows device designs of perovskite-based memristors with tailored memory properties exhibiting both volatile and nonvolatile modes for reconfigurable and more complex neuromorphic computing frameworks [3, 4]. In this regard, a complete picture of the underlying physical mechanisms of the interplay between the carrier and ionic dynamics is essential in the further development of perovskite-based devices in photovoltaic and neuromorphic computing applications.

2.1 Objectives

The aim of this work is to control and identify the origin of the hysteresis effect in perovskite-based devices (i) in order to improve the long-term operational stability of PSCs, and (ii) to design memristors exhibiting both volatile and nonvolatile memory for reconfigurable switching modes suitable for versatile neuromorphic computing applications. In order to achieve this general objective, this work is broken down into 4 sub-objectives culminating to a more complete insight on

the complex interplay among the migrating ions, vacancies, activated metals and interfacial reactivity. These sub-objectives are divided as follows:

- I. Demonstrate the resistive switching in perovskite-based memristors with the insight of interfacial reactivity between migrating ions and the thin Ag layer. Investigate the dynamic state transition during the SET process via a new established systematic chronoamperometry (CA) and IS measurements at varying applied potential in order to distinguishably analyze the IS response at distinct resistance states.
- II. Develop a method to correlate the frequency domain response (IS) to the time domain response ($I - V$) with the insight of the association between the appearance of a negative capacitance arc of devices exhibiting inverted hysteresis in perovskite-based memristors. Validate experimentally the correlation of the IS response with the corresponding observed hysteresis implementing the established CA-IS measurement protocol – normal hysteresis is capacitive and inverted hysteresis is inductive. Demonstrate a new phenomenon of a voltage-dependent transformation from capacitive to inductive hysteresis in perovskite solar cells similarly observed in memristors.
- III. Formulate a general dynamical model for perovskite solar cells exhibiting the transformation from capacitive to inductive hysteresis, both in the scan rate-dependent $I - V$ and IS response, with the insight of neuronal models describing memristive response. Investigate the origin of low frequency (LF) features by obtaining the time constants of the LF capacitors and inductors to uncover the underlying mechanism.
- IV. Demonstrate hysteresis control in perovskite-based memristors exhibiting a two-step resistive switching SET process by the incorporation of thin intermediate buffer layers with the insight of the transition mechanisms. Investigation of the complex interplay among mobile ions, vacancies and activated metal ions by developing a dynamical model in order to untangle the switching regimes associated to the gradual current increase followed by the abrupt resistive switching.

2.2 Significance

Understanding the underlying mechanisms governing the hysteretic $I - V$ effect in perovskite-based devices is of paramount importance in order to circumvent the theoretical and physical limits in both photovoltaic and neuromorphic computing technologies. A complete picture of the complex interplay among the dynamic carrier and ionic transport under operation would allow perovskite-based devices with tailored optoelectronic properties suitable for targeted applications. This entails the hysteresis control in the $I - V$ response of specific device configurations favoring the long-term operational stability of perovskite solar cells, and promoting reconfigurable switching modes for memristors for neuromorphic computing applications. This control over the hysteresis would not only further advance the corresponding technologies in the device-level, but also unravel fundamental microscopic mechanisms broadening and complementing the already well-established theories and concepts.

2.3 Thesis Critical Overview

Hysteresis in the scan direction- and scan rate-dependent $I - V$ curves of PSCs has been critically related to the device operational stability [5–11]. Not only does the PSCs suffer the well-understood degradation due to oxygen/water exposure, photodegradation, and phase-segregation in mixed cation/anion formations, they also exhibit degradation due to ionic transport [12–14]. Ionic transport has been attributed to be one of the dominant factors contributing to these hysteretic effects in PSCs [15]. The migration of the ions and vacancies under the influence of an external electric field could change the photogenerated charge collection efficiency with time resulting to the hysteresis in $I - V$ measurements [5–8]. However, migrating ions within the perovskite layer under the external electric field may also reach the external contacts leading to an irreversible reaction detrimental to the device performance and stability. Several studies have used a more reactive Ag layer (~ 100 nm) revealing the formation of an insulating AgI layer, measured via XPS measurement of the metal surface, blocking the charge extraction and reducing device performance [16, 17]. As the XPS measurement is only measured on the surface of the considerably thick Ag contact, the kinetics

at the metal interface is not directly probed. Moreover, the effect of the AgI formation within a thick Ag contact is not controlled, hence, the degradation mechanism due to the interfacial reactivity is not fully understood.

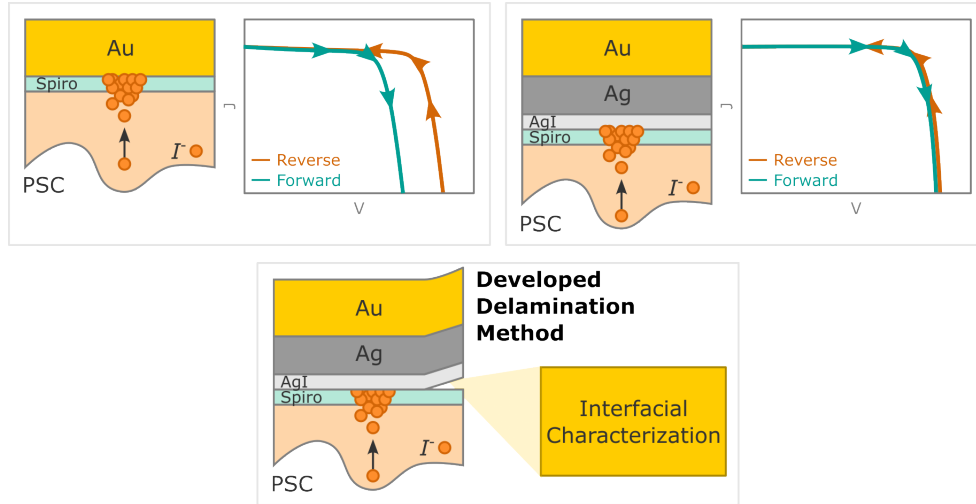


Figure 2.1: Schematic illustration of the interfacial passivation of perovskite solar cells by reactive ion scavengers [18].

We have previously demonstrated the reduction of the hysteresis in methylammonium lead iodide (MAPbI_3) perovskite solar cells (PSCs) by incorporating a thin Ag layer (<5 nm) in between the Spiro-OMeTAD electron transport layer (ETL) and the Au metal contact (work not included in this thesis) [18]. The experimental scheme is schematically illustrated in Fig. 2.1. The incorporation of a thin Ag layer passivates the external interfaces by the interfacial reaction between the migrating iodide I^- ions with the more reactive metal resulting to the formation of a thin AgI layer. This controlled chemical reaction, in conjunction with the appropriate transport layers, results to the immobilization of mobile ions significantly reducing the hysteresis, and in turn, improving the device long term stability. In addition, we have developed a new contact delamination method allowing the direct XPS measurement of the Ag interface to analyze the interfacial reactivity of the final hysteresis-free state. Most notably, the Ag thickness needs to be thick enough to capture all mobile ions but not too thick to prevent further induced degradation of the perovskite. Correspondingly, the impedance response is stable for the device with the Ag layer confirming that the promoted chemical reaction passivates the external interfaces. With the newly developed

delamination method, direct characterization of the interfacial reaction reveals the underlying kinetics that can be transferrable in various device systems and configurations.

From this insight of the interfacial reactivity modulating the hysteresis in PSCs as a starting point, the 4 individual sub-objectives are achieved by distinct sets of experimental designs to systematically control the hysteresis effect in perovskite-based devices. Each set of experimental design has resulted to pieces of insights that are carried over to the subsequent studies snowballing into the overall accomplishment of the collective goal. This thesis critical overview summarizes the experimental designs, achievements and relevance of individual works addressing each sub-objective. Moreover, the essential insights carried over to the subsequent work are highlighted. Finally, the overall impact and contribution of the totality of the work in the scientific field are emphasized.

2.3.1 Resistive Switching via Interfacial Reactivity

As the interfacial reactivity between migrating ions and a reactive metal contact has been uncovered, the understanding of this underlying mechanism has been directly applied to memristive systems utilizing Ag as the top electrode. Resistive random access memory devices (ReRAMs) or memristors have been gaining considerable attention due to their promising in-memory and neuromorphic capabilities [19, 20]. The resistive switching has been demonstrated in oxide films [21–24], two-terminal organic semiconductors [25], Si-based devices [26–29], and various halide perovskite materials [11, 30–32]. Numerous interpretations have been proposed to explain the resistive switching but are very specific to the device configuration [11, 30–35]. Moreover, several studies have qualitatively interpreted the distinction between the ON and OFF states of memristors via the impedance spectroscopy (IS) but not the full evolution of the state transitions [22, 36, 37]. Despite the resistive switching being demonstrated in a wide range of memristor configurations, the switching mechanism is still yet to be completely elucidated making interpretations based on traditional models rather challenging.

In this work, we address the sub-objective I of demonstrating the resistive switching in a 2D Ruddlesden-Popper (RP) perovskite-based memristor with the insight of the interfacial reactivity resulting to the formation of AgI layer to con-

control and modulate the interfacial reactivity of the mobile I^- ions with the Ag layer. Two device configurations are directly compared – 2D RP perovskite memristor with and without a thin undoped Spiro-OMeTAD interfacial layer between the 2D perovskite and Ag contact. As compared to the PSC, the resistive switching due to the thin Ag layer in the memristor configuration is more pronounced as the device does not contain the appropriate electron and hole selective layers. The characteristic $I - V$ curve, measured via cyclic voltammetry (CV), of the memristor without the Spiro-OMeTAD layer exhibits a gradual transition from the high resistance state (HRS) or OFF state to the low resistance state (LRS) or ON state. The state transition is attributed to the formation and dissolution of AgI layer the perovskite/Ag interface indicating a nonfilamentary switching mechanism. In contrast, the characteristic $I - V$ response of the memristor with the Spiro-OMeTAD buffer layer exhibits an abrupt transition from the OFF state to the ON state suggesting the formation of conductive filaments within the buffer layer. The experimental scheme is schematically illustrated in Fig. 2.2.

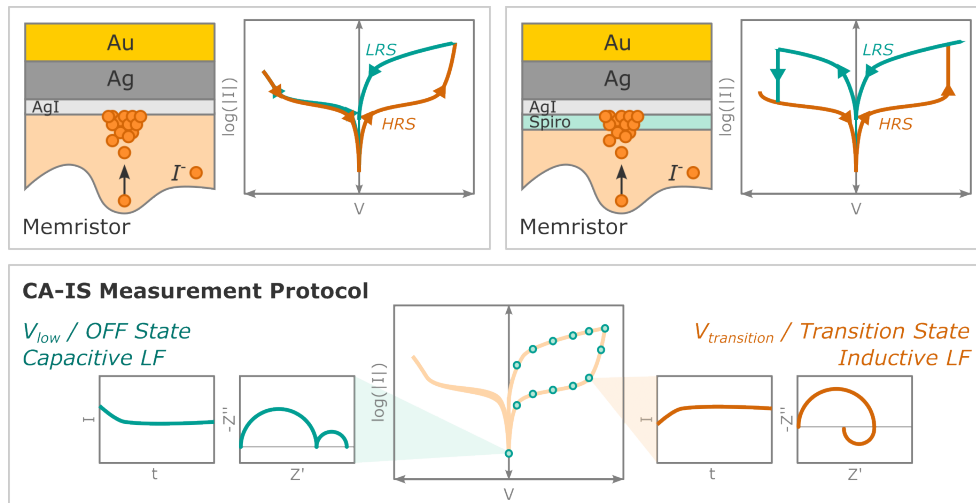


Figure 2.2: Schematic illustration of the spectral properties of the dynamic state transitions in metal halide perovskite-based memristor exhibiting negative capacitance [38].

As the memristive response of memristors exhibits two distinct states at the same applied voltages, a systematic electrical characterization protocol is required in order to distinguishably probe the physical origin of the state transitions. In this regard, we develop a sequence of chronoamperometry (CA) mea-

surement for 5 s, subsequently followed by the impedance spectroscopy (IS) with a frequency range of 1 MHz to 0.1 Hz and an amplitude of 10 mV to investigate the dynamic state transition. This CA-IS measurement protocol is conducted sequentially at varying voltages from 0 V to 2 V back to 0 V at 0.1 V intervals in order to simulate a the full CV scan. This newly developed measurement protocol allows for the stable tracking of the device resistance state in correlation with the corresponding IS response. In addition, all measurements are carried out inside the nitrogen filled glovebox under dark and controlled conditions to further isolate the system from external factors resulting to stable and reliable IS measurements.

The impedance spectral evolution of the memristor without the buffer layer exhibits a significant transformation of the low frequency arc to a negative capacitance arc. This negative capacitance or inductive feature has been disputed in the field due to the absence of an electromagnetic origin. Notably, the differential DC resistance from the reconstructed $I - V$ curve [$R_{\text{DC-jV}} = (dI/dV)^{-1}$] is highly correlated with the extrapolated DC resistance from the IS spectra [$R_{\text{DC-IS}} \sim Z'(f \rightarrow 0)$] indicating the validity of these inductive features that further reduces the device resistance during the dynamic state transition. The measurement in the glove box under controlled conditions has provided stable and reliable response corroborating the validity of the IS features. In contrast, no negative capacitance arc is observed during the abrupt state transition of the device with the Spiro-OMeTAD interfacial layer. This indicates that the negative capacitance arc is intimately correlated to the ion migration and redistribution promoting the formation and dissolution of AgI layer at the perovskite/Ag interface. Moreover, the thin undoped Spiro-OMeTAD layer acts as a physical barrier inhibiting the the interaction between migrating ions and the Ag contact wherein the conductive filaments are localized upon state transition to the ON state. This suggests that the incorporation of an undoped buffer layer provides another degree of freedom in the switching properties of perovskite-based memristors. The full article is presented in **Chapter 4**.

2.3.2 Correlation of Hysteresis with Equivalent Circuit

Impedance spectroscopy (IS) measurements have been widely implemented in PSCs to provide valuable information on the underlying mechanisms under device operation. Yet, the stability and reliability of the IS spectra have been a critical issue for the analysis as the device response changes depending on the measurement conditions [39, 40]. Moreover, the appearance of the contentious low frequency negative capacitance and inductive features in PSCs exhibiting inverted hysteresis associated to detrimental effects in the device performance has made it difficult to distinguish between intrinsic variations and slow degradation in PSCs [40–42]. In this regard, IS measurements are conducted at quasi-steady state conditions, i.e. illuminated short-circuit or open-voltage conditions, for more stable and reliable response [40, 43]. However, these two quasi-steady state conditions are measured at completely different voltages where the electronic and ionic transport dynamics vary significantly [44–46]. In addition, the negative capacitance or inductive features have also been observed at applied voltages between these two quasi-steady state conditions [41, 42, 47, 48]. Hence, correlation of the observed hysteresis in the $I - V$ curves with the corresponding IS features at different device states allowing the extraction of valuable insight in the mechanisms under device operation.

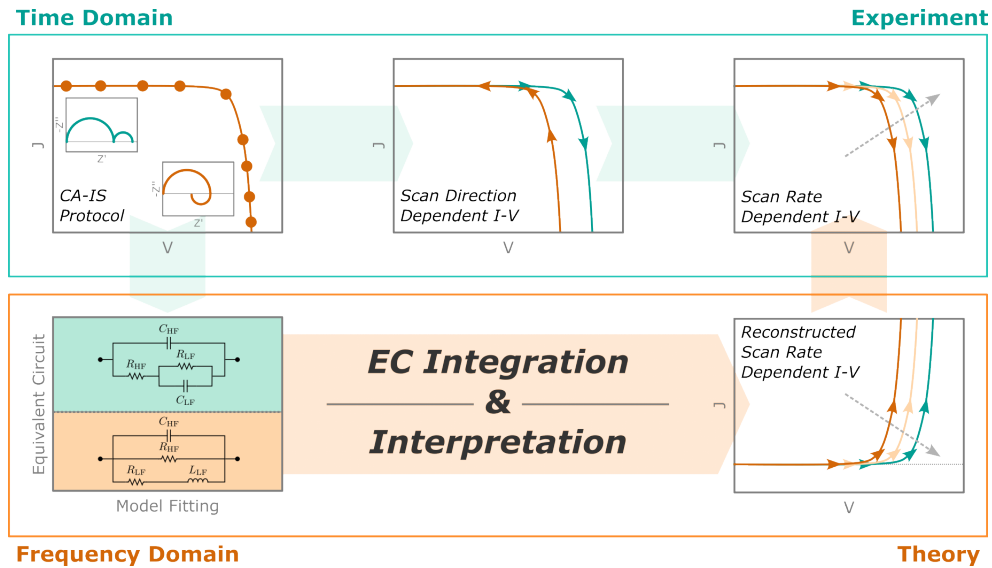


Figure 2.3: Schematic illustration of the theory of hysteresis in halide perovskites by integration of the equivalent circuit [49].

In this work, we address the sub-objective II of developing a method to correlate the frequency domain response from the IS to the time domain response from the $I - V$ with the insight of the appearance of negative capacitance (positive inductance) in memristors. The validation of the inductive IS features in memristive response, which can be considered as a strong inverted hysteresis, further supports the strong correlation between the IS response and the hysteresis features. Depending on the IS features of a PSC exhibiting a certain hysteresis type, the pertinent equivalent circuit model that describes the IS spectrum is determined. Here, we develop a method that converts the equivalent circuit model into a set of differential equations, in which the internal state variables emerge naturally and does not require to be predefined in terms of a physical model. These equations are then integrated with the appropriate voltage-dependence of the internal state variables given a linear voltage sweep. From this method, two elementary but relevant equivalent circuit models for PSCs and memristors are solved reconstructing the emergence of hysteresis in the scan-rate dependent $I - V$ curves. The reconstructed $I - V$ curves are consistent with the experimentally observed scan-rate dependent $I - V$ responses for both the normal and inverted hysteresis. We demonstrate quantitatively a general insight – capacitive effect corresponds to normal hysteresis, while inductive effect corresponds to inverted hysteresis. The integration scheme from the frequency domain IS equivalent circuit model to the time domain $I - V$ response is illustrated in Fig. 2.3.

Furthermore, the established CA-IS measurement protocol is utilized for PSCs to systematically validate the correlation between IS response from a catalogue of devices exhibiting normal and inverted hysteresis. Consistently, devices exhibiting normal hysteresis feature the scan-rate dependent $I - V$ response associated to the capacitive equivalent circuit model. Similarly, the devices exhibiting inverted hysteresis feature the scan-rate dependent $I - V$ response associated to the inductive equivalent circuit model. From the IS spectral evolution of these devices, voltage-dependent electrical circuit parameters are extracted providing valuable information on the response times attributed to the slow capacitive relaxation and the kinetic constant leading to the inductive effect. Moreover, a new phenomenon of transformation from capacitive to inductive hysteresis in

the scan rate-dependent $I - V$ response, consistent by the voltage-dependent IS evolution, further substantiates the predictive capability of the equivalent circuit model integration theory. The full article is presented in **Chapter 5**.

2.3.3 General Model of the Hysteresis Transition

From the previous work, we have recently demonstrated a transition from a LF capacitive to an inductive response consistent with the scan rate-dependent $I - V$ curve and the integration theory of the elementary equivalent circuit models. As the equivalent circuit is selected depending on a single IS response [40, 43, 50], the capacitive and inductive responses featured by the same device implies the need for a general dynamical model encompassing these transitions throughout the full range of voltages. Equivalent circuits have been modified in order to describe the negative capacitance or inductive feature but they require negative values in the fitting parameters [47, 51, 52]. Moreover, the equivalent circuit models are designed only to fit the experimental voltage-dependent IS spectra without the interpretation of the corresponding $I - V$ response at the same measurement voltages.

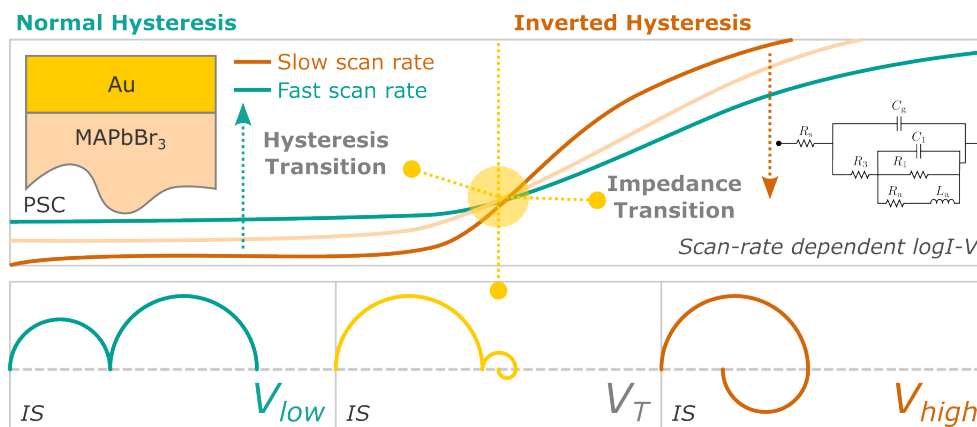


Figure 2.4: Schematic illustration of the transition from capacitive hysteresis: a neuron-style model to correlate $I - V$ curves to impedances of metal halide perovskites [53].

In this work, we address the sub-objective II of formulating a general dynamical model for PSCs exhibiting the transformation from capacitive to inductive hysteresis, observed from the previous work, with the insight of neuronal models describing the memristive response. As the inductive features in IS response are

observed in a multitude of chemical, biological and material systems, and further validated in our previous work on the physical model of memristors [54], the *chemical inductor* has recently been established and modeled [55]. This chemical inductor generally denotes a class of dynamical models which manifests an inductive response in the impedance and transient response without the occurrence of an electromagnetic induction effect. With the general insight from the integration theory, in conjunction with the chemical inductor model, we show that there is a specific voltage (crossing point) where the hysteresis transitions from normal to inverted. At the same time, the IS response transitions from capacitive to inductive as observed experimentally. The general dynamical model scheme is illustrated in Fig 2.4.

The general dynamical model is then implemented to a methylammonium lead bromide (MAPbBr₃) PSC device exhibiting the hysteresis and LF IS response transition. The pertinent impedance parameters are extracted by fitting the corresponding equivalent circuit of the general dynamical model to the experimental results. From the extracted parameters, the relevant time constants can be determined and analyzed. The high correlation between the kinetic time constants associated to the LF capacitor and inductor indicates that both responses are not completely independent processes. Both LF capacitive and inductive responses correspond to a similar ionic-controlled recombination influenced by ionic transport at the interface. This methodology provides great control and understanding over the dynamic properties of PSCs throughout a broad voltage range, including transitions states in both the $I-V$ hysteresis and the IS response. The full article is presented in **Chapter 6**.

2.3.4 Two-Step SET Process in Perovskite Memristors

As the emergence of perovskites as the switching material for memristor applications, the focus of the development has been shifted towards the best performing devices with the best switching properties, such as highest ON/OFF ratios, lowest operating voltages, fastest switching speeds, and longest operation endurance [56–62]. Rationally, a parallel effort has been dedicated on the demonstration of these recently developed materials in in-memory and neuromorphic computing platforms to further highlight the relevance of perovskite-based memristors

[63–75]. However, due to the distinct reported memristor configurations incorporating various intermediate layers, attention to the underlying kinetics on the resistive switching has been overlooked [38, 76, 77]. More importantly, as the development of in-memory and neuromorphic computing framework has been getting more and more complex, versatile memristors exhibiting reconfigurable volatile and nonvolatile memory are essential in order address the required hardware specifications.

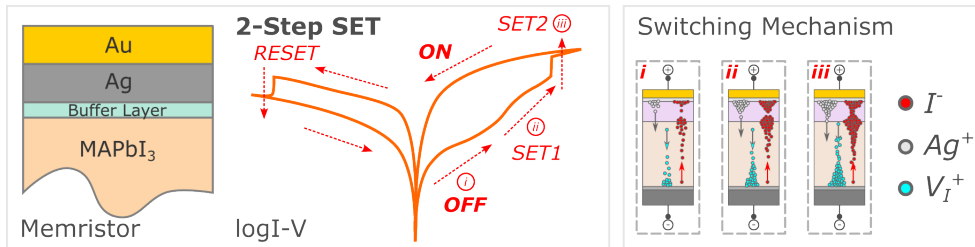


Figure 2.5: Schematic illustration of the mechanistic and kinetic analysis of perovskite memristors with buffer layers: the case of a two-step set process [78].

In this work, we address the sub-objective IV of demonstrating hysteresis control in perovskite-based memristors with the insight of the dynamic ionic transport and interaction mechanisms in the device state transitions. A two-step SET resistive switching SET process is demonstrated in MAPbI₃-based memristors with the incorporation of the thin Ag layer and thin undoped buffer layers. The resistive switching involves an initial gradual increase in current associated with a drift-related halide and vacancy migration within the perovskite bulk layer, followed by an abrupt resistive switching associated with diffusion of mobile Ag⁺ conductive filamentary formation. This two-step SET process is observed for memristors irrespective of the type of buffer layer. Direct comparison of the characteristic $I - V$ response devices with buffer layers to devices without the buffer and/or Ag layer indicates that the buffer layer not only acts as a physical barrier regulating the reactivity of migrating ions with Ag, but also as a pool of diffused ions within the buffer layer maintaining the resistive state once the applied field is removed. Moreover, the incorporation of the buffer and Ag layer transforms the volatile response with a unipolar threshold switching mechanism to a nonvolatile response with a bipolar resistive switching mechanism. The two-step SET process exhibits both volatile drift and nonvolatile diffusive

mechanisms depending on the applied external field. The experimental scheme is schematically illustrated in Fig. 2.5.

Moreover, we develop a dynamical model that explains the characteristic $I - V$ curve that untangles the switching regimes allowing the investigation of the complex interplay among mobile ions, vacancies and activated metal ions. This model, together with the piecewise linear fitting of the HRS, LRS and transition states, reveals that the current control is due to the accumulation of ions and interfacial reactions. From the model, relevant parameters are extracted and analyzed suggesting that the two-step SET process is governed by the same mechanism irrespective of the buffer layer. This insight into the mechanisms governing the switching response would be essential for controlling the memristive properties of memristor configurations tailored for targeted neural network applications with varying levels of complexity. The devices with the two-step SET process exhibit both drift and diffusive switching responses which can be utilized for adaptable and reconfigurable implementation of versatile in-memory computing frameworks. The full article is presented in **Chapter 7**

2.3.5 A More Complete Picture

The individual achievements of each of the five sub-objectives has ultimately culminated in a more complete picture of the complex ionic transport dynamics involving the migrating ions, vacancies, activated metals and interfacial reactivity for hysteresis control in perovskite-based devices. The overall picture is schematically illustrated in Fig. 2.6. In general, this dynamic ionic transport identified in the totality of this work can be classified in four different stages – (i) drift-related ionic migration under the influence of the applied external field, (ii) ionic accumulation at the interface of the top electrode, (iii) interfacial reactivity between the migrating halide ions and a more reactive Ag metal contact, and (iv) the ionic diffusion of the activated metal ions due to the interfacial reactivity through the buffer layer upon exposure to sufficiently applied external field.

The mechanisms of each of these distinct stages can manifest differently in the time domain (scan direction- and scan rate-dependent $I - V$ curves) and frequency domain (voltage-dependent IS spectra) response. The considerable drift-related ionic migration and redistribution can result to a gradual change in

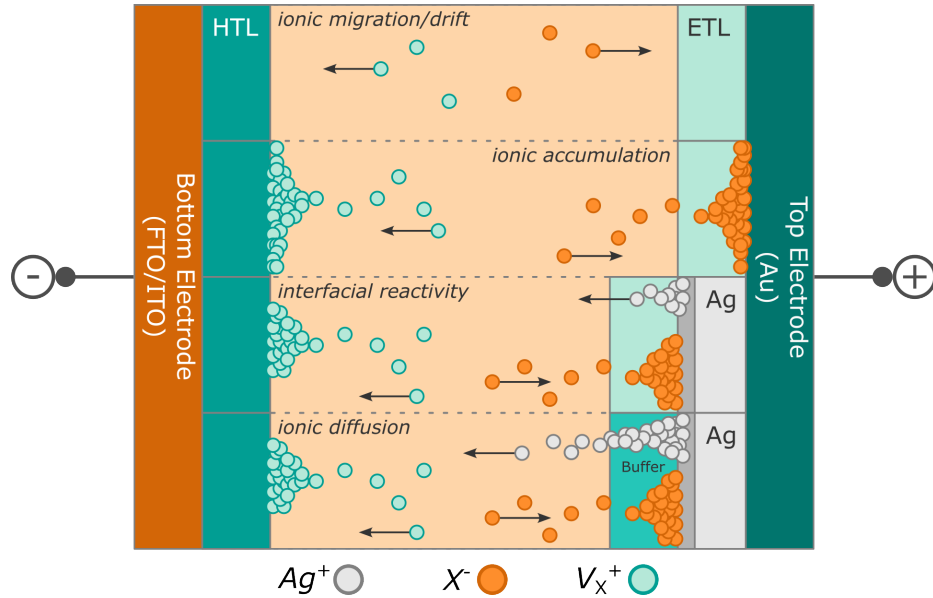


Figure 2.6: Schematic diagram of the ionic transport dynamics involving the complex interplay among the migrating ions, vacancies, activated metals and interfacial reactivity.

the perovskite bulk layer properties. This can be observed as a gradual current increase or decrease associated to the scan-rate dependent tendencies of the $I-V$ curves, with a corresponding reduction in the high frequency (HF) resistance in the voltage-dependent IS response. Continued ionic migration can, then, result to ion accumulation at the contact interface modifying the slower interfacial kinetics. This can manifest as a more pronounced hysteresis effect, either normal or inverted, with a corresponding increase in the LF capacitance associated to the ionic double layer formation. With the use of a more reactive contact such as Ag, interfacial reactivity can result to the formation and/or dissolution of a thin AgI layer modulating the ionic activity at the contact interface. This can be exhibited as a reduction in hysteresis or a steeper current increase depending on the overall thickness of the AgI layer, with a corresponding stabilized LF arc in the IS or the appearance of a LF negative capacitance/inductive feature in the IS spectra, respectively. Finally, the activation of metallic ions upon interfacial reactivity can diffuse through an undoped buffer layer towards the bottom contact which can result in conductive filamentary formation (either vacancy or metallic filaments, or a combination of both). This is exemplified as an abrupt increase in current in the $I-V$ response, with no observable inductive

feature due to the fast avalanche effect of the filament formation.

With a better understanding of the underlying mechanisms in the dynamic ionic and electronic transport in perovskite-based devices, hysteresis response can be controlled by precise device configuration designs specifically suited for the targeted optoelectronic application. This hysteresis control would not only further advance the corresponding technologies circumventing the theoretical and physical limits, but also broaden and complement the already well-established theories and concepts in the field of perovskite technology.

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Chapter 3

Methods

This chapter discusses the experimental details implemented in this work. This includes the detailed fabrication method for both the perovskite solar cells and memristors. The optoelectronic characterization setups are also specified, as well as the newly developed characterization protocol implemented throughout this work.

3.1 Device Fabrication

3.1.1 Perovskite Solar Cell

The PSCs are fabricated with a mesoporous *n-i-p* regular solar cell structure. The *n*-type electron transport layer (ETL) consists of a compact (*c*-TiO₂) and a mesoporous (*m*-TiO₂) titanium dioxide (TiO₂) layers. On the other hand, the *p*-type hole transport layer (HTL) is composed of a Li-doped Spiro-OMeTAD layer. The intrinsic active layer is made of varying perovskite formulations. The step-by-step fabrication method is schematically illustrated in Fig. 3.1.

Substrate Selection

Highly transparent fluorine-doped tin oxide (FTO) on TEC15 glass substrates are used as the transparent bottom electrode. The FTO-coated glass substrates are carefully selected to have highly uniform, unscratched and homogeneous surface required for the deposition of high quality thin films.

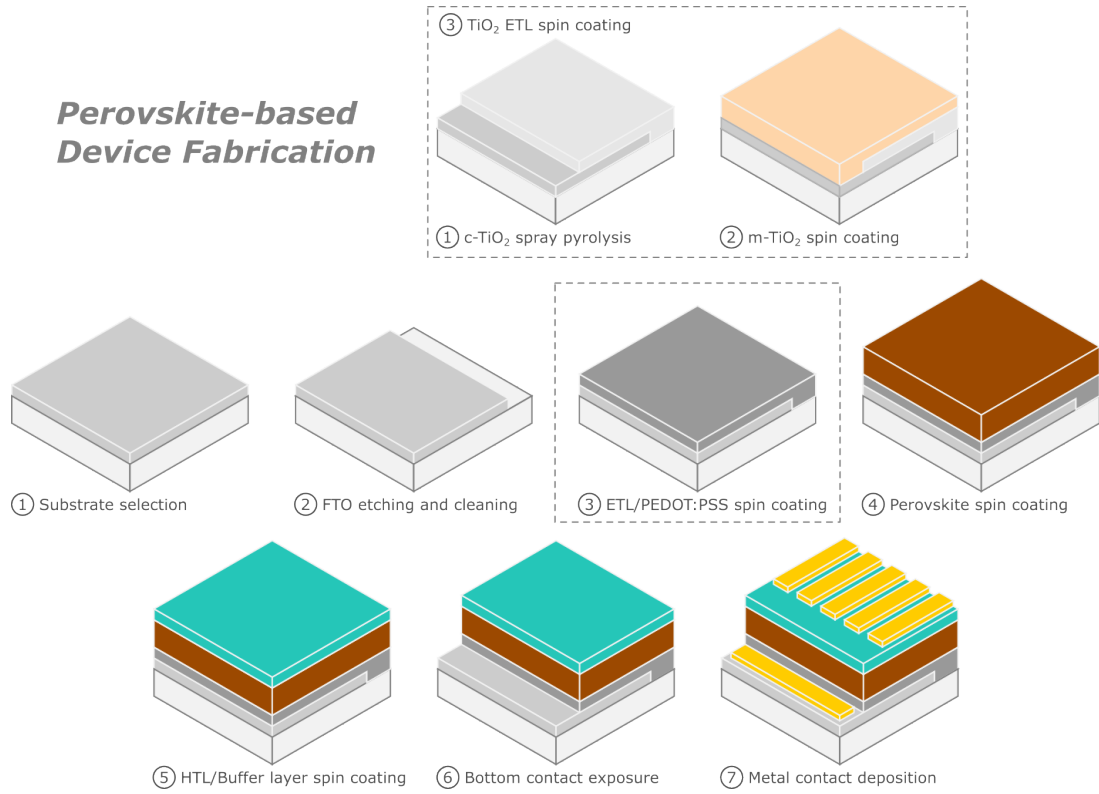


Figure 3.1: Schematic diagram of the step-by-step perovskite-based device fabrication.

FTO Etching and Cleaning

The FTO-coated glass substrates are partially etched using zinc (Zn) powder and a 2 M hydrochloric (HCl) solution. The etched samples are individually brushed to mechanically remove any residues of the etching process, then, rinsed with water. The brushed samples are then subjected to a sequence of 15-minute sonication in deionized water with Hellmanex detergent solution, acetone, and isopropyl alcohol. Finally, the cleaned samples are blow-dried using a nitrogen gun.

Compact TiO₂ Spray Pyrolysis

Prior to the deposition of the c-TiO₂ layer, the cleaned samples are subjected to an ultraviolet-ozone (UV-O₃) treatment for 15 minutes to further remove organic contamination on the surface and improve the surface wetting. The c-TiO₂ solution is prepared using 600 μ L titanium(IV) diisopropoxide bis(acetylacetonate) (TAA) (75% in 2-propanol, Sigma Aldrich), 400 μ L of acetylacetonone ($\geq 99\%$,

Sigma Aldrich), and 9 mL absolute ethanol (Sigma Aldrich). The UV-O₃ treated substrates are then placed on a temperature-controlled hotplate with strips of FTO-coated glass placed on top to mask the bottom electrode region. The substrate temperature is then increased from room temperature to ~ 440 °C with a ramp time of 25 minutes and a dwell time of 35 minutes. Once the temperature reaches 440 °C, the c-TiO₂ solution deposited onto the masked samples via spray pyrolysis with O₂ as carrier gas for a total of 10 seconds (~ 1 s spraying each sample). The spray pyrolysis step is repeated 4-5 times with a 1-minute interval between each spray sequence. After the 35-minute dwell time, the samples are cooled down to 150 °C before retrieving and safe-keeping inside a drybox.

Mesoporous TiO₂ Spin Coating

Similar to the c-TiO₂ deposition, the samples with the c-TiO₂ layer is again subjected to a 15-minute UV-O₃ treatment prior to the m-TiO₂ deposition to further improve surface wetting during spin coating. The m-TiO₂ solution is prepared using 450 mg of transparent TiO₂ paste (30 NR-D, Greatcell Solar) in 3 mL absolute ethanol (Sigma Aldrich) and is placed in a mechanical roller overnight to improve the dissolution. A 100 μ L m-TiO₂ solution is statically spin coated onto the samples for 10 s at 2000 RPM with 2000 RPM/s acceleration. Upon m-TiO₂ spin coating, the samples are heated at 100 °C prior to the annealing sequence of (i) 370 °C at a ramp time of 40 mins and dwell time of 10 mins, (ii) 470 °C at a ramp time of 25 mins and a dwell time of 10 mins, and (iii) 500 °C at a ramp time of 10 mins and a dwell time of 30 mins. After the annealing sequence, the samples are cooled down to 150 °C before retrieving and transporting immediately into the nitrogen-controlled glove box.

Perovskite Spin Coating

Inside the glove box, the samples are subjected to a dehydration treatment at 100 °C for 10 minutes to further remove water and humidity within the m-TiO₂ during transport. For MAPbI₃-based PSCs, a 1.4 M MAPbI₃ precursor solution is prepared using 681.5 mg lead iodide (PbI₂) (>98%, TCI) in 95 μ L : 1 mL dimethylsulfoxide (DMSO) ($\geq 99.9\%$, Sigma Aldrich) : N,N-dimethylformamide (DMF) (99.8%, Sigma Aldrich) solution. Once the PbI₂ is completely dissolved,

the PbI_2 precursor solution is added to 235 mg methylammonium iodide (MAI) (>99.9%, Greatcell Solar) to complete the 1.4 M MAPbI_3 precursor solution. The samples are then cooled down to room temperature prior to the MAPbI_3 deposition via the anti-solvent spin coating method. Once cooled, a 50 μL MAPbI_3 perovskite solution is statically spin coated onto the m- TiO_2 layer for 50 s at 4000 RPM with 1000 RPM/s acceleration. After 8 s from the start of spin coating sequence, a 500 μL chlorobenzene (CB) anti-solvent is dynamically injected onto the MAPbI_3 solution to promote the crystallization of high quality and homogeneous perovskite films. Once the spin coating sequence ends, the samples are annealed at 100 $^\circ\text{C}$ for 10 mins, then are cooled down to room temperature.

For MAPbBr_3 -based PSCs, a 1.4 M MAPbBr_3 precursor solution is prepared using 513.8 mg lead bromide (PbBr_2) in a 1 mL 4:1 DMF:DMSO solution. Once the PbBr_2 is completely dissolved, the PbBr_2 precursor solution is added to 156.7 mg methylammonium bromide (MABr) (>99.9%, Greatcell Solar) to complete the 1.4 M MAPbBr_3 perovskite solution. a 50 μL MAPbBr_3 perovskite solution is statically spin coated onto the m- TiO_2 layer using a two-step spin coating sequence – (i) 10 s at 1000 RPM with 1000 RPM/s acceleration, then subsequently followed by (ii) 40 s at 4000 RPM with 4000 RPM/s acceleration. After 28 s from the start of the spin coating sequence, a 400 μL toluene anti-solvent is dynamically injected on the MAPbBr_3 solution to promote the crystallization of high quality and homogeneous perovskite films. Once the spin coating sequence ends, the samples are annealed at 100 $^\circ\text{C}$ for 30 mins, then are cooled down to room temperature.

Spiro-OMeTAD Spin Coating

The Li-doped Spiro-OMeTAD (2,2',7,7'-Tetrakis[N,N-di(4-methoxyphenyl)amino]-9,9'-spirobifluorene) HTL is prepared using 72.3 mg Spiro-OMeTAD (99.9% HPLC, Feiming Chemical LTD) in 1 mL CB, 28.8 μL 4-tert-Butylpyridine (TBP) and 17.5 μL Li dopants from a stock solution of 520 mg lithium bis (trifluoromethanesulfonyl)imide (LiTFSI) (99.99%, Sigma Aldrich) in 1 mL acetonitrile. A 50 μL Li-doped Spiro-OMeTAD solution is dynamically spin coated on top of the perovskite layer for 30 s at 4000 RPM with 800 RPM/s acceleration.

Bottom Contact Exposure

Prior to the metal contact deposition, the FTO bottom contact is exposed by mechanically scratching the deposited layers using another FTO-coated glass substrate. The FTO-side of the spare FTO substrate is used to effectively remove the softer layers on top exposing an adequate region for the bottom contact.

Metal Contact Deposition

Finally, an 85 nm top Au metal contact is deposited via resistive thermal evaporation using a commercial Oerlikon Leybold Univex 250 evaporation chamber. In order to achieve homogeneous Au layer, a three-step sequence of evaporation rates are used – (i) 0.05 Å/s from 0 - 1 nm, (ii) 0.5 Å/s from 1 - 10 nm, and (iii) 1.0 Å/s from 10 - 85 nm.

3.1.2 Perovskite-based Memristor

The perovskite-based memristor are fabricated with some similar methods as the PSCs. However, the main difference in the memristor configuration as compared to the PSC is the use of intermediate buffer layers instead of ETL and HTL layers. Moreover, the top metal contact consists of a thin layer of a more reactive Ag metal followed by the Au top electrode.

PEDOT:PSS Spin Coating

The deposition of the poly(3,4-ethylenedioxythiophene) polystyrene sulfonate (PEDOT:PSS) intermediate layer is carried out in ambient conditions. Prior to the deposition of the PEDOT:PSS layer, the cleaned samples are subjected to an ultraviolet-ozone (UV-O₃) treatment for 15 minutes to further remove organic contamination on the surface and improve the surface wetting. The PEDOT:PSS solution (Clevios P VP.Al 4083, Heraeus) is let to set at room temperature before usage. Using a syringe, the PEDOT:PSS solution filtered using a PTFE 0.45 μm filter and is dropped onto the substrate to fully cover the surface. The PEDOT:PSS filtered solution is statically spin coated into the etched FTO substrate for 30 s at 3000 RPM with a 1000 RPM/s acceleration. Once the spin coating sequence ends, the samples are annealed at 100 °C for 5 minutes, then

are immediately transported inside the nitrogen-controlled glove box.

Perovskite Spin Coating

Inside the glove box, the samples are subjected to a dehydration at 100°C for 10 minutes to further remove water and humidity within the PEDOT:PSS layer. For the MAPbI₃-based memristors, the exact formulation and spin coating sequence for MAPbI₃ PSCs are implemented.

For the 2D Ruddlesden-Popper (RP) perovskite-based memristors, a stoichiometric 0.15 M (PEA)₂(MA) _{$\bar{n}-1$} Pb _{\bar{n}} I_{3 $\bar{n}+1$} (PEA = phenylethylammonium and MA = methylammonium) (PEAMAPI) perovskite solution, where \bar{n} is the dominant n component, is prepared using 345.8 mg PbI₂ in 1 mL DMF solution. Once the PbI₂ is completely dissolved, the PbI₂ precursor solution is added to a 95.4 mg MAI. Finally, the the solution is added to a 74.7 mg phenylethylammonium iodide (PEAI) (98%, Greatcell Solar). The samples are then cooled down to room temperature prior to the PEAMAPI deposition via the anti-solvent spin coating method. Once cooled, a 50 μ L PEAMAPI perovskite solution is statically spin coated onto the m-TiO₂ layer for 50 s at 4000 RPM with 1000 RPM/s acceleration. After 8 s from the start of spin coating sequence, a 500 μ L chlorobenzene (CB) anti-solvent is dynamically injected onto the PEAMAPI solution to promote the crystallization of high quality and homogeneous perovskite films. Once the spin coating sequence ends, the samples are the annealed at 100 °C for 10 mins, then are cooled down to room temperature.

Buffer Layer Spin Coating

The thin undoped buffer layers can consist of 10 mg/mL Spiro-OMeTAD, 10 mg/mL (6,6)-Phenyl C61 butyric acid methyl ester (PCBM) (nano-C) or 5 mg/mL Poly(methyl methacrylate) (PMMA) (Sigma Aldrich). The buffer solutions are prepared in 1 mL CB without any additional dopants/additives. A 50 μ L undoped buffer solution is dynamically spin coated on top of the perovskite layer for 30 s at 6000 RPM with 800 RPM/s acceleration.

Metal Contact Deposition

Finally, a 15 nm Ag/85 nm Au top contact is deposited via resistive thermal evaporation using a commercial Oerlikon Leybold Univex 250 evaporation chamber. The 15 nm Ag layer is deposited at 0.3 \AA/s , then is subsequently followed by the deposition of the 85 nm Au metal, same evaporation rate sequence as the PSCs, without breaking the evaporation chamber vacuum.

3.2 Optoelectronic Characterization

3.2.1 Solar Cell Illuminated $J - V$ Curve

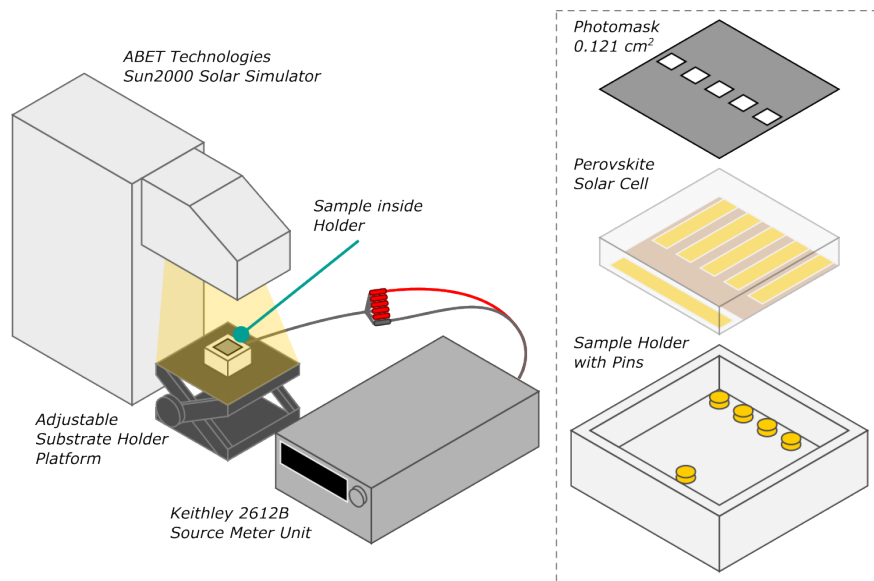


Figure 3.2: Schematic diagram of the $J - V$ curve measurements of PSCs under illuminated conditions.

The power conversion efficiency (PCE) of the PSCs are determined by measuring the illuminated $J - V$ curves using a standardized light source with air mass AM 1.5 spectrum at 100 mW cm^{-2} irradiance from an ABET Technologies Sun2000 Solar Simulator as schematically illustrated in Fig. 3.2. Before the actual illuminated $J - V$ measurements of the PSCs, the substrate holder platform height is adjusted to calibrate the light intensity to the standardized 100 mW cm^{-2} using a Si photodiode. Once calibrated, the samples are placed inside a custom sample holder with pogo pins aligned to the five individual pixels and the bottom contact. The active area of illumination for every pixel is controlled

via a photomask with 0.121 cm^2 window for each pixel. The $J - V$ curves are then measured via a voltage sweep in the forward and/or reverse scan directions using a software-controlled Kiethley 2612B source meter unit.

3.2.2 Memristor Characteristic $I - V$ Response

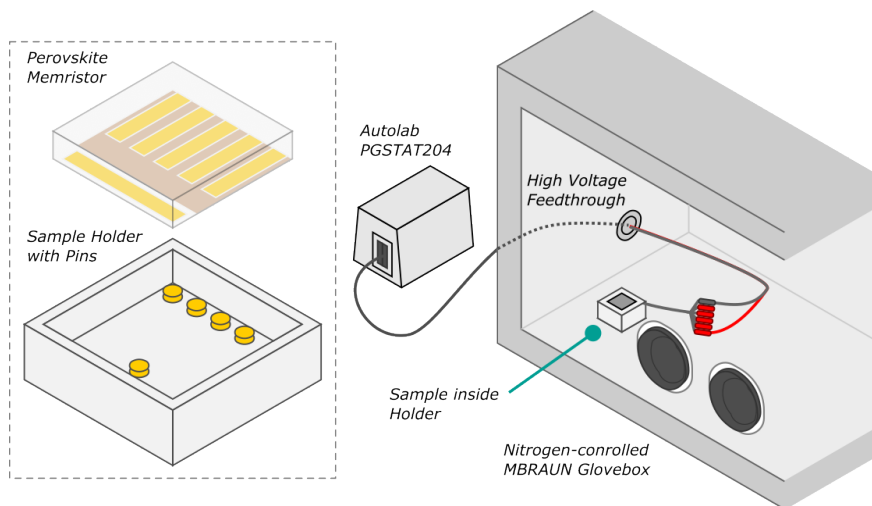


Figure 3.3: Schematic diagram of the characteristic $I - V$ response measurement of memristors inside the nitrogen-controlled glove box.

The characteristic $I - V$ response of the memristors are measured under dark and controlled conditions inside the nitrogen-controlled MBRAUN M200 glove box using an Autolab PGSTAT204 potentiostat as schematically illustrated in Fig. 3.3. The samples are transferred inside the glove box and are placed inside the custom sample holder. The sample holder is connected to the potentiostat through a high-voltage feedthrough installed in the glove box. The characteristic $I - V$ response of the perovskite-based memristors are then measured via a cyclic voltammetry (CV) method with varying voltage ranges for various cycles. Based on the memristive response parameters, the retention times, endurance, and switching speed measurements are also carried over in this experimental setup. Moreover, the newly developed CA-IS measurement protocols are also conducted.

3.2.3 Established CA-IS Measurement Protocol

The developed CA-IS measurement protocol consists of a CA measurement for 5 s, subsequently followed by the IS with a frequency range of 1 MHz to 0.1 Hz

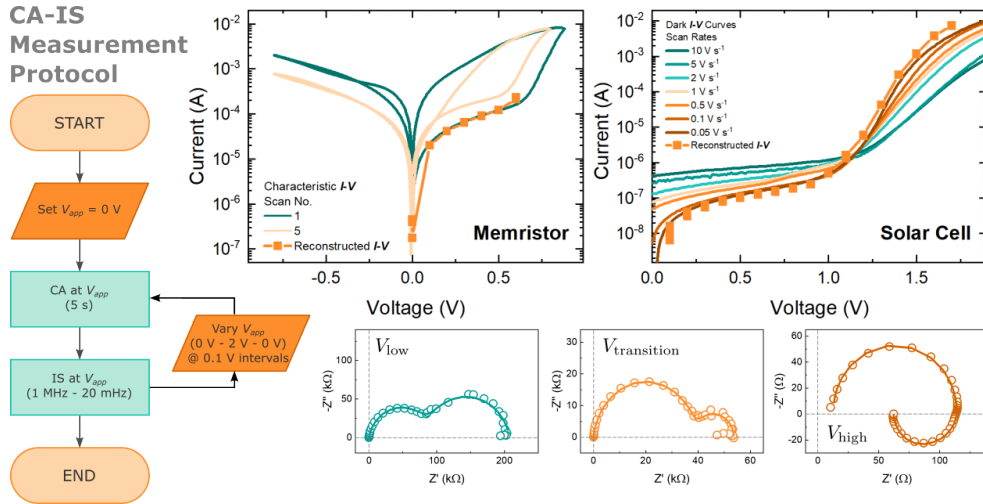


Figure 3.4: Schematic diagram of the established CA-IS measurement protocol.

and an amplitude of 10 mV to investigate the dynamic state transitions. This CA-IS measurement protocol is conducted sequentially at varying voltages from 0 V to 2 V back to 0 V at 0.1 V intervals in order to simulate a the full CV scan as illustrated in Fig. 3.4. The sequence of CA measurements measured at various applied voltages are plotted as a reconstructed $I - V$ curve with each voltage having a corresponding IS spectrum. The reconstructed $I - V$ curves, in conjunction with the pertinent time domain electrical measurements, i.e. CV measurements for memristors, and scan-rate dependent $I - V$ curves for PSCs, allows the identification of the device state associated to the corresponding IS spectrum. This provides valuable information on the analysis by correlating the time-domain to the frequency domain response of the devices.

Chapter 4

Spectral Properties of the Dynamic State Transition in Metal Halide Perovskite-based Memristor Exhibiting Negative Capacitance

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Extent of Contribution : 80%

The following tasks/activities are the author's contribution to this work:

- Synthesis and fabrication of 2D PEAMAPI-based memristor devices
- Optimization of fabricated memristor devices
- Optoelectronic characterization of fabricated devices
- Analysis of characterization measurement data and results
- Manuscript and response to reviewers' comments document preparation

Abstract

The evolution of device properties in memristor switching between high- and low-resistance states is critical for applications and is still highly subjected to

significant ambiguity. Here, we present the dynamic state transition in a 2D Ruddlesden-Popper perovskite-based memristor device, measured via impedance spectroscopy. The spectral evolution of the transition exhibits a significant transformation of the low frequency arc to a negative capacitance arc, further decreasing the device resistance. The capacitance-frequency evolution of the device indicates that the appearance of the negative capacitance is intimately related to a slow kinetic phenomenon due to ionic migration and redistribution occurring at the perovskite/metal contact interface. In contrast, no negative capacitance arc is observed during the state transition of a memristor device where the contact is passivated by an undoped Spiro-OMeTAD interfacial layer. The switching mechanisms are entirely different, one due to interface transformation and the other due to filamentary formation.

4.1 Introduction

Resistive random access memory (ReRAM) devices have been gaining considerable interest due to their nonvolatile switching properties allowing in-memory computing analogous to the synaptic response in the human brain [1, 2]. The promising in-memory and neuromorphic computing capabilities of ReRAM devices aim to subvert the traditional Von Neumann architecture and overcome its limitations, i.e., heat wall and memory wall, signifying an eventual end to Moore’s law [1, 2]. The resistive switching has been observed in oxide films in metal / oxide / metal structures [3–6], two-terminal organic semiconductors [7], silicon-based devices with complementary metal / oxide / semiconductor compatible architecture [8, 9], and various halide perovskite materials [10–13]. As the memristive response is demonstrated irrespective of the device design and configuration, the switching mechanism is still yet to be completely elucidated, making interpretations based on traditional models rather challenging.

Numerous interpretations have been proposed to explain the resistive switching mechanism specific to the device configuration. Most notably, the device switching mechanism in perovskite-based devices ranges from the formation and rupture of highly conducting filaments at applied voltage [10], nonfilamentary ionic and vacancy redistribution [11, 14–16], to silver-iodide (AgI)-induced re-

sistive switching [13]. However, there has been no concrete consensus on the memristive switching mechanism. Several studies have conducted nondestructive impedance spectroscopy (IS) to qualitatively interpret the distinction between the memristor ON and OFF states [4, 17, 18]. Despite the advances in memristive device designs, information on the device evolution during the dynamic state transition is still insufficient.

In this Letter, we demonstrate the evolution of the memristive switching in a two-dimensional (2D) Ruddlesden-Popper (RP) perovskite ReRAM device with particular focus on the transition state via IS. We have been able to obtain stable and reproducible IS results in these devices over a significant range of applied bias that enables a systematic investigation of the transition state from high to low resistance, providing insight into the electrical and physical origin of the transformation. The IS measurements reveal an evolution of the low frequency arc to a negative capacitance arc, suggesting an intimate correlation with the interfacial reactivity between perovskite and the metal contact layer. In contrast, an ReRAM device exhibiting stronger hysteresis with an interfacial layer between the perovskite and the metal contact did not feature a low-frequency negative capacitance arc.

4.2 Experimental Details

The fabricated resistive random access memory (ReRAM) device was based on the 2D RP $(\text{PEA})_2(\text{MA})_{\bar{n}-1}\text{Pb}_{\bar{n}}\text{I}_{3\bar{n}+1}$ perovskite (PEA = phenylethylammonium and MA = methylammonium), where $\bar{n} = 5$ is the dominant n component. The 2D RP perovskite formulation properties, such as considerable ON/OFF ratio, good data retention capability, high environmental stability, good electrical conductivity, and reduced ion migration, were highly suitable for memory applications [11]. The ReRAM device had a configuration of fluorinedoped tin oxide (FTO)/poly(3,4-ethylenedioxythiophene) polystyrene sulfonate (PEDOT:PSS)/2D RP perovskite/Ag (15 nm)/Au (85 nm); herein, the sample is called the Ag ReRAM device. For comparison, an ReRAM device with a thin, undoped Spiro-OMeTAD interfacial layer in between the 2D perovskite and Ag was also fabricated (Spiro/Ag ReRAM). The Ag and Spiro/Ag ReRAM devices

had effective active areas of 0.257 and 0.098 cm², respectively. The relatively large device sizes were implemented for ease of fabrication and measurement. The dynamic transition state was investigated via a sequence of chronoamperometry (CA) for 5 s subsequently followed by impedance spectroscopy (IS) with a frequency range of 0.1 MHz - 0.1 Hz and an amplitude of 10 mV. The CA-IS sequence was conducted at varying voltages from 0 V to 2 V back to 0 V at 0.1 V increments. All measurements were carried out inside the glovebox filled with nitrogen under dark and controlled conditions using an Autolab PGSTAT-30 potentiostat.

4.3 Results and Discussion

The complex plane impedance plots of the IS spectral evolution for the Ag ReRAM device with the corresponding reconstructed current density-voltage ($j - V$) curves from the CA measurements are shown in Figs. 4.1a and 4.1c, respectively. The high-resistance state (HRS) or OFF state and low-resistance state (LRS) or ON state are highlighted accordingly, with the arrows indicating the scan direction. At 0 V, the IS spectrum is in the initial OFF state exhibiting two distinct, well-defined impedance contours corresponding to the high and low-frequency arcs. The high frequency arc is generally attributed to the bulk response, while the low frequency arc is related to the perovskite/contact interface [19, 20]. At low applied voltages, up to 0.3 V, the low-frequency resistance slightly increases with an observable noise usually connected to the interaction of ions with the contact [21]. Conversely, the high-frequency resistance remains unchanged, indicating no significant difference in the bulk perovskite properties as the applied bias is modified. Approaching the threshold voltage, from 0.4 V to 0.5 V, both the high- and low-frequency arcs begin to decrease correlated with modifications in both the bulk and the interfacial properties, respectively. Beyond the threshold voltage, in the transition state of 0.6 V, the high-frequency arc begins to decrease more dramatically, suggesting a further transformation in the bulk. Most notably, the low-frequency arc begins to manifest as a negative capacitance arc. The negative capacitance arc persists up to 0.8 V, just before the device completely transitions to the ON state (0.9 V), exhibiting highly

unstable IS spectra throughout the measurement frequency range.

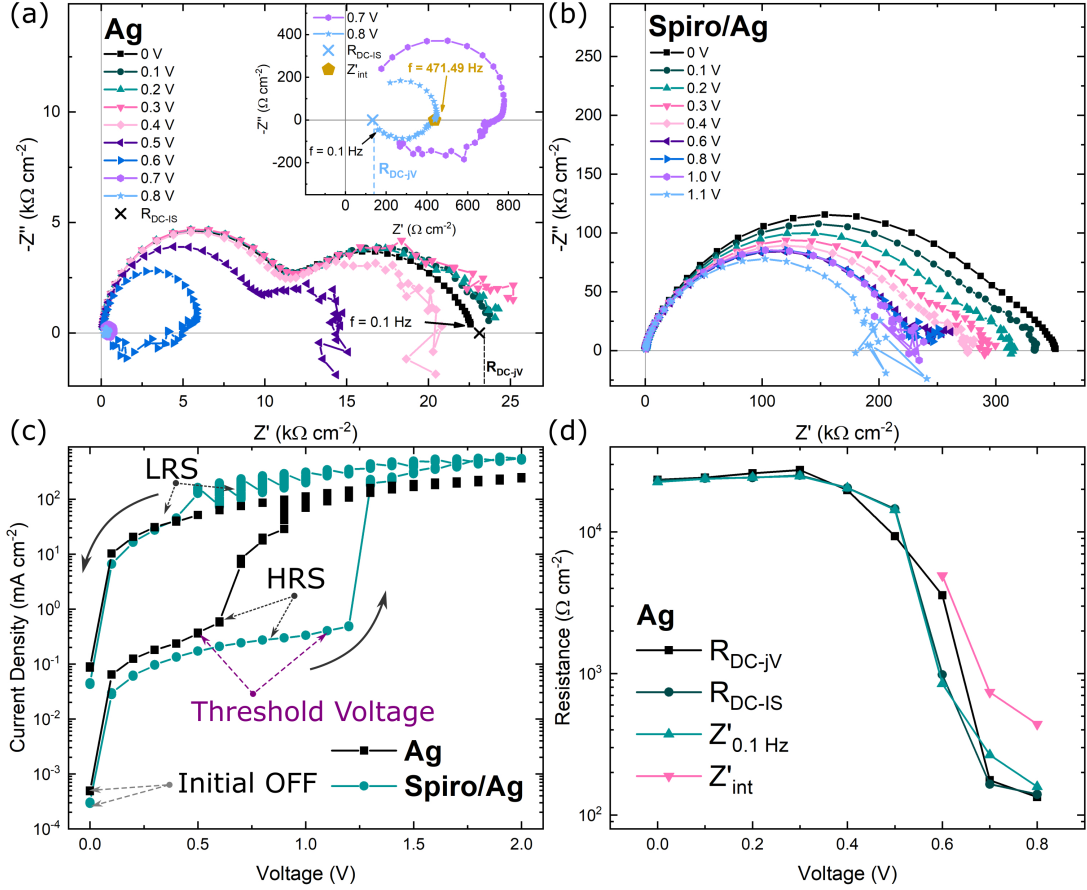


Figure 4.1: (a) The IS spectral evolution of the Ag ReRAM device at representative voltages, with R_{DC-jV} , R_{DC-IS} , and Z'_{int} highlighted for the representative OFF (0 V) and transition (0.8 V) states, (b) the IS spectra evolution of the Spiro/Ag ReRAM device, (c) the corresponding reconstructed $j - V$ curves, and (d) the R_{DC-jV} , R_{DC-IS} , $Z'_{0.1 Hz}$, and Z'_{int} voltage-dependence of the Ag ReRAM device.

The switching event of the Ag ReRAM device takes place within 3 s as revealed in CA measurements at the applied switching voltage of $V_{app} = 0.9$ V shown in Fig. 4.2a. The current response of the Ag ReRAM device exhibits a continuous gradual increase in current density and then eventually stabilizes before 3 s. We note that prior to each IS scan, a 5 s CA measurement is carried out. Hence, the observed reduction in resistances indicates a stabilized dynamic response in the bulk and perovskite/Ag interfacial properties [11, 22]. The gradual transition of the Ag ReRAM device implies a nonfilamentary switching mechanism due to ion migration and distribution at the perovskite/Ag interface

[11, 14–16]. The resistive switching mechanism has been attributed to the reversible reaction of formation and dissolution of the AgI monolayer at the 2D RP perovskite/Ag interface, sufficiently modifying the injection properties that control the electronic charge transfer rate [11].

In order to obtain clearer insight into the origin of the negative capacitance arcs, the IS spectra evolution of the Spiro/Ag ReRAM device is investigated. The complex impedance plots of the IS spectra evolution for the Spiro/Ag ReRAM device at representative applied voltages are shown in Fig. 4.1b. In contrast to the Ag ReRAM device, the initial OFF state of the Spiro/Ag ReRAM device exhibits two convoluted impedance contours with a significantly higher overall resistance. The higher overall resistance is expected for having the undoped Spiro-OMeTAD interfacial layer, due to its high transport resistance, inhibiting the direct contact of the 2D perovskite layer with the Ag metal contact [23]. As the applied voltage is increased up to 0.4 V, the overall resistance gradually decreases, suggesting a consistent modification in the Spiro-OMeTAD layer due to migrating ions' arrival at the interface. At higher applied voltages from 0.6 V to 1.0 V, the IS spectra exhibit no significant change in overall resistance but have observable low frequency noise, suggesting an interaction of ions with the Ag contact similar to the Ag ReRAM device response at low applied voltages. This suggests that the undoped Spiro-OMeTAD layer acts as a physical barrier inhibiting the interaction between migrating ions and the Ag contact at lower applied voltages. Approaching the threshold voltage at 1.1 V, the overall resistance appears to decrease once more with a more observable low-frequency noise, indicating a further change in the device properties and an increased interaction of ions with the Ag contact.

The higher threshold voltage is due to the high transport resistance of the Spiro-OMeTAD layer necessitating a higher applied bias to compensate the voltage drop experienced by the device. The Spiro/Ag ReRAM device then abruptly switches to the ON state at 1.2 V, without the low-frequency negative capacitance arc, as opposed to the Ag ReRAM device with a more gradual transition state from 0.6 V to 0.8 V. Correspondingly, an abrupt switching at 0.3 s of the Spiro/Ag ReRAM device is observed at $V_{app} = 1.2$ V and then continues to increase in current density until it eventually stabilizes before 1.5 s as shown in

Fig. 4.2a. The abrupt transition of the Spiro/Ag ReRAM device suggests the formation of conductive filaments within the Spiro-OMeTAD layer [10, 12, 13, 16]. Moreover, both devices exhibit high ON state retention times of $> 10^4$ s at a read voltage of 0.3 V as shown in Fig. 4.2b. Notably, the Ag and the Spiro/Ag ReRAM ON state currents gradually decrease and stabilize at $\sim 51\%$ and $\sim 74\%$ of the initial value, respectively. The larger sustained ON state current of the Spiro/Ag ReRAM device further implies a filamentary switching mechanism [24]. The higher overall resistance due to the undoped Spiro-OMeTAD layer together with the filamentary resistive switching results in a higher ON/OFF ratio of ~ 3 orders of magnitude for the Spiro/Ag ReRAM device as compared to ~ 2 orders of magnitude for the Ag ReRAM device. The absence of the low-frequency negative capacitance arcs in the Spiro/Ag ReRAM resistive switching indicates that the negative capacitance is intimately correlated with the ion migration and redistribution, promoting the reactivity at the perovskite/Ag interface.

In order to validate the low-frequency negative capacitance arcs of the Ag ReRAM device, the differential direct current (DC) resistance obtained from the reconstructed $j - V$ curves ($R_{\text{DC-}jV}$) is compared with DC resistance of the IS spectra ($R_{\text{DC-IS}}$). $R_{\text{DC-}jV}$, defined as the resistance at stationary conditions ($f = 0$ Hz), obeys the relationship given by $R_{\text{DC-}jV} = \partial V / \partial I$. From the complex impedance plot, $R_{\text{DC-IS}}$ is obtained from the real impedance intercept of the IS extrapolated at $f = 0$ Hz. $R_{\text{DC-}jV}$ and $R_{\text{DC-IS}}$ plotted against the IS spectra at representative OFF state (0 V) and transition state (0.8 V) voltages are illustrated in Fig. 4.1a and the inset of Fig. 4.1a, respectively. At the OFF state voltage, $R_{\text{DC-}jV}$ is in good agreement with $R_{\text{DC-IS}}$, confirming a high correlation between the reconstructed $j - V$ curve and the measured IS spectra. Consequently, the real impedance at the lowest measurement frequency ($Z'_{0.1 \text{ Hz}}$) corresponds well to both RDC values. On the other hand, the real impedance intercept (Z'_{int}) occurs at an intermediate frequency for the IS spectrum at 0.8 V, exhibiting the negative capacitance arc, highlighted in the inset of Fig. 4.1a. The correlation among $R_{\text{DC-}jV}$, $R_{\text{DC-IS}}$, $Z'_{0.1 \text{ Hz}}$, and Z'_{int} is plotted in Fig. 4.1d. The correlation among the resistances shows that the negative capacitance arc provides a major contribution to the DC resistance of the device, which highlights the significance of the negative capacitance phenomenon for practical device operation. In addition, it

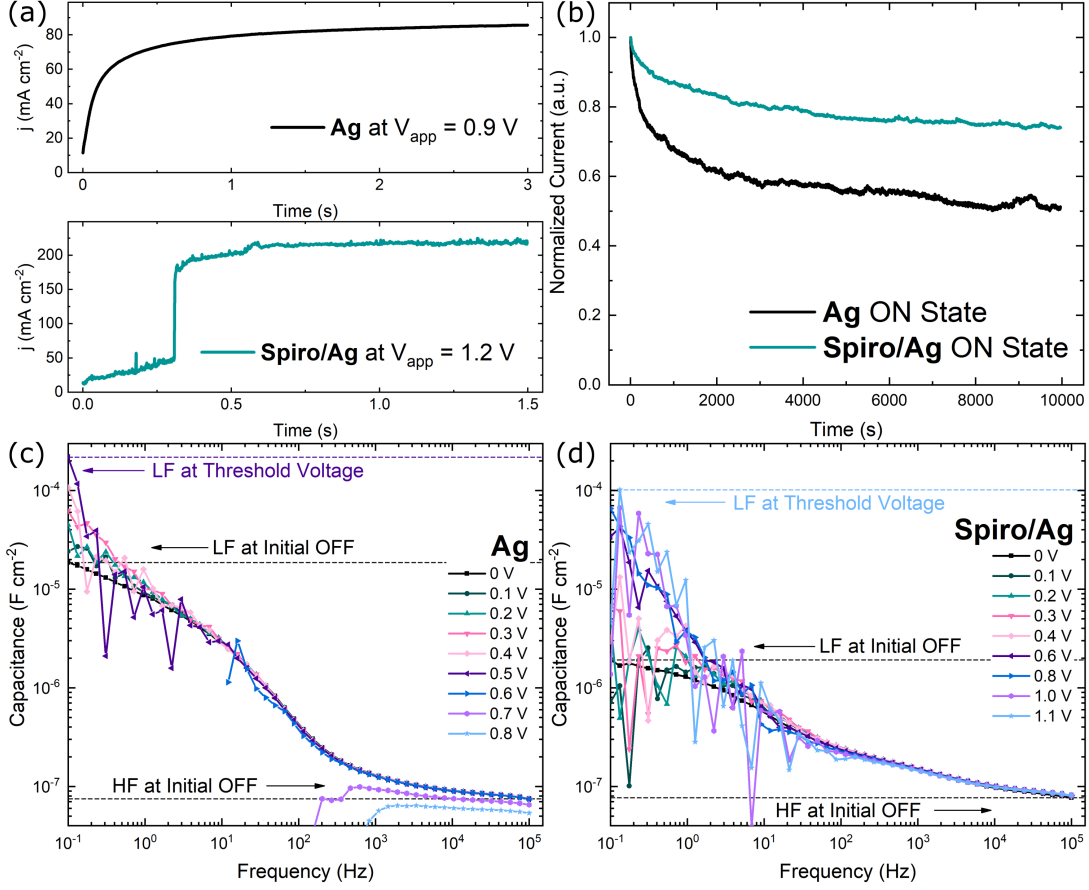


Figure 4.2: (a) The chronoamperometry measurements monitoring the switching speed for the Ag and Spiro/Ag ReRAM devices at switching voltages (V_{app}) of 0.9 V and 1.2 V, respectively, (b) the ON state retention measurement of the Ag and Spiro/Ag ReRAM devices measured at $V_{read} = 0.3$ V, and the $C - f$ plots of the (c) Ag and (d) Spiro/Ag ReRAM devices at varying applied voltages, highlighting the high- and low-frequency capacitances in the initial off state and at the threshold voltage.

has been frequently reported that slight variations in steady-state conditions of the system under measurement can significantly affect the device response during data collection, especially at low frequencies requiring longer measurement times [11, 25]. However, in our case, the measurement is reproducible, indicating no drift of the physical system and, thus, obtaining a reliable spectral response. It is noted that the current measurement for the reconstructed $j - V$ curve is conducted before the IS, suggesting that the high correlation among R_{DC-jV} , R_{DC-IS} , and $Z'_{0.1 \text{ Hz}}$ is indicative of a stable IS response by the ReRAM device for voltages prior to the ON state. The further reduction in resistance manifested by the low-frequency negative arcs indicates a slow kinetic interaction at the perovskite/Ag

interface occurring during the dynamic state transition.

Investigating the evolution of the capacitance-frequency ($C - f$) plots provides further information on the charge distribution during state transitions of the ReRAM devices. The $C - f$ plots of the Ag and Spiro/Ag ReRAM devices are shown in Figs. 4.2c and 4.2d, respectively. The high-frequency capacitive plateau is generally attributed to the bulk capacitance of the perovskite layer, while the low frequency plateau is attributed to electrode polarization due to charge accumulation [19, 22, 26]. Both devices exhibit nearly identical high-frequency capacitance in the initial OFF state, confirming that the 2D RP perovskite layers are of the same bulk capacitive properties. However, the OFF state low-frequency capacitance of the Spiro/Ag ReRAM device features a lower capacitance than the Ag ReRAM device. The lower low-frequency capacitance of the OFF state is attributed to the Spiro-OMeTAD layer acting as a physical barrier between the perovskite layer the Ag metal contact. The decrease in capacitance is consistent with the typical parallel plate capacitor governed by $C = \epsilon\epsilon_0/d$, where C is the capacitance per unit area, ϵ_0 is the vacuum permittivity, and d is the separation between the plates. As the voltage is increased for the Ag ReRAM device, the low-frequency capacitance gradually increases up to $\sim 10^4 \text{ F} \cdot \text{cm}^2$ at the threshold voltage, subsequently followed by a dramatic drop at the transition state voltages. Markedly, the low-frequency capacitances of the Spiro/Ag ReRAM device at the threshold voltage approach the low-frequency capacitance of the Ag ReRAM device at the threshold voltage. The high correspondence of low-frequency capacitances at the threshold voltage suggests a similar device response consistent with the IS spectra evolution. The delayed capacitive response of the Spiro/ReRAM device upholds the initial impediment to the interfacial reactivity of migrating ions with the Ag metal contact by the thin, undoped Spiro-OMeTAD layer, necessitating a higher applied voltage to promote the chemical reactivity.

4.4 Conclusion

In summary, we have demonstrated the dynamic state transitions in 2D RP perovskite-based memristor devices via IS. The interfacial reactivity between

the perovskite and the Ag metal contact resulted in a gradual state transition, indicative of a nonfilamentary switching mechanism, wherein the distinct, well-defined low-frequency arc transformed into a persistent negative capacitance arc during the device transition state. In contrast, a thin, undoped Spiro-OMeTAD interfacial layer, acting as a physical barrier with a higher overall resistance, impeded the reactivity between the migrating ions and the metal contact. Consequently, the ReRAM device with the Spiro-OMeTAD interfacial layer exhibited a higher ON/OFF ratio with an abrupt transition from the OFF state to the ON state, suggesting the filament formation within the Spiro-OMeTAD layer, but did not feature the negative capacitance arc. The switching and retention measurements further substantiate the distinction between the resistive switching mechanisms. The high correlation between the differential DC resistance from the reconstructed $j - V$ curve with the extrapolated DC resistance from the IS spectra suggested a further reduction in device resistance, corroborating the validity of the negative capacitance arcs. The $C - f$ evolution further confirmed the impediment to ionic migration and reactivity by the Spiro-OMeTAD interfacial layer. The dynamic IS spectra and $C - f$ evolution for both devices indicated an intimate correlation between the low frequency negative capacitance and the interfacial interaction attributed to a slow ionic migration and redistribution, leading to the formation and dissolution of AgI. Despite the relatively large device sizes, memristive responses were observed for both devices. Down-scaling the device dimensions for practical applications is expected to exhibit significantly stronger memristive behavior on the nanometer scale [27]. The insight into the dynamic state transition investigated by IS would allow for ReRAM device designs with tailored switching properties in terms of the ON/ OFF ratio, threshold voltage, and transition state control.

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Chapter 5

Theory of Hysteresis in Halide Perovskites by Integration of the Equivalent Circuit

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Extent of Contribution : 60%

The following tasks/activities are the author's contribution to this work:

- Synthesis and fabrication of MAPbI₃ and MAPbBr₃ perovskite solar cells
- Optoelectronic characterization and analysis of fabricated devices
- Manuscript and response to reviewers' comments document preparation

Abstract

Perovskite solar cells show a number of internal electronic-ionic effects that produce hysteresis in the current-voltage curves and a dependence of the temporal response on the conditions of the previous stimulus applied to the sample. There are many models and explanations in the literature, but predictive methods that may lead to an assessment of the solar cell behavior based on independent measurements are needed. Here, we develop a method to predict time domain response starting from the frequency domain response measured by impedance spectroscopy over a collection of steady states. The rationale of the method is to convert the impedance response into a set of differential equations, in which the

internal state variables emerge naturally and need not be predefined in terms of a physical (drift/diffusion/interfaces) model. Then, one solves (integrates) the evolution for a required external perturbation such as voltage sweep at a constant rate (cyclic voltammetry). Using this method, we solve two elementary but relevant equivalent circuit models for perovskite solar cells and memristors, and we show the emergence of hysteresis in terms of the relevant time and energy constants that can be fully obtained from impedance spectroscopy. We demonstrate quantitatively a central insight in agreement with many observations: regular hysteresis is capacitive, and inverted hysteresis is inductive. Analysis of several types of perovskite solar cells shows excellent correlation of the type of equivalent circuit and the observed hysteresis. A new phenomenon of transformation from capacitive to inductive hysteresis in the course of the current-voltage

5.1 Introduction

The phenomenon of dynamic hysteresis of current-voltage curves has been present since early studies of halide perovskite solar cells (PSCs) [1–8]. Hysteresis is often obtained when measuring the current of the solar cell under a voltage sweep at a constant velocity, which is a standard procedure to determine the solar cell efficiency. When the forward and reverse scans do not match, the current density-voltage curves ($J-V$) become separated and cast doubt on the true performance features of the devices at steady state, requiring more advanced protocols such as maximum power point tracking [9–12]. More generally, hysteresis phenomena encompass a wide variety of behaviors that depend on the applied perturbations such as scanning rate, external voltage range, and prescanning conditions. The response of PSCs is quite varied depending on the composition of the perovskite and the nature of the contacts [13, 14] and the hysteresis affects the measurement methods such as space-charge-limited currents [15]. Notably, perovskite-based devices show a significant ionic conductivity in addition to the electronic semiconductor properties [16]. The ionic influence modifies the interfaces and produces significant changes in device operation [17]. The hysteresis effect has been associated with the slow time dynamics due to ionic motion inside the perovskite layer [16, 18]. There have been presented a huge number of models and explanations

involving the modification of internal built-in fields, the effect of traps, and the ionic effect at the perovskite/contact interface [19–27].

It is widely acknowledged that the hysteresis effect consists of a response of the sample that depends on the previous history and treatments. There is a strong memory effect involving one or several internal properties. It is quite difficult to make a typical mixed electronic-ionic drift-diffusion model that captures the variation of essential internal parameters under a set of experimental perturbations [28, 29]. Therefore, the majority of analyses of hysteresis in PSCs are descriptions of the measurement using different types of mechanisms, often highly complex ones. These explanations typically do not have predictive power as to which circumstances, determined by independent measurements, will lead to hysteresis. It has been possible to minimize hysteresis effects in perovskite solar cells largely by empirical methods [30–32]. However, the presence of strong hysteresis in recent high-performance configurations, such as tandem solar cells, still persists [33–35]. Therefore, new methods that provide insight into hysteresis in PSCs via alternative measurement may have significant practical value.

Here, we aim to develop a method for the analysis of hysteresis that does not need to establish a specific physical model of the solar cell. Following the techniques of electrical engineering, we can predict the time evolution of the system by having information on the small perturbation response in the frequency domain, even in the case in which internal state variables present their own relaxation effects that result in memory properties.

In order to find the frequency domain response, we use the equivalent circuit (EC) model that results from the measurement of impedance spectroscopy (IS). Thereafter, we transform the EC into a set of dynamical equations in the time domain. Finally, the system of differential equations is solved as a function of time (or voltage) by integration for the required conditions and perturbations and is compared to the experimental curves. In this way, we obtain definite information on the causes of the hysteresis in the device, and we can then modify material components and measure them separately by IS.

A memristive device is a two-terminal structure that undergoes a voltage-controlled conductance change [36]. The hysteresis effects in halide perovskites facilitate the construction of effective memristors involving different mechanisms.

These have been applied to resistive random access memories [37], artificial neural networks (ANN) [38, 39], and photonic memories and synapses [40, 41]. The method developed in this paper will provide insight into the essential memory effects of perovskite memristor devices.

In the early years of PSC research, reproducibility was a very serious issue. In the measurement of $J-V$ curves, voltage or light pretreatments would modify the outcome significantly. Even a single measurement would change the subsequent response [42], and it was difficult to distinguish between the varied sample-drift effects associated with the uncontrolled casuistic hysteresis-type effects or the slow degradation modifying the cell irreversibly. In particular, the measurement of impedance spectroscopy could affect the state of the sample afterward. In such conditions, it would be rather difficult to attempt to effectively relate IS results and time domain response. At the present time, we are confident that robust PSCs can be prepared in which the response of the cell is the same after measurements, such as IS and cyclic voltammetry (CV), are performed. It has become possible to test complex temporal responses connected to frequency domain measurements. It is time to develop a robust theory that captures the essential physical elements of hysteresis.

Let us define the phenomenon that we want to study. Fig. 5.1 shows the $J-V$ curves of three perovskite solar cells that differ only slightly by the thickness of the compact TiO_2 layer at the contact in highly stable triple layer carbon PSC [8]. The $J-V$ curve is the essential characteristic to evaluate the performance of the solar cell. It requires a sweep of voltage from reverse to forward voltage (forward scan) or from forward to reverse voltage (reverse scan direction). Fig. 5.1a shows that the forward scan exhibits a lower current and voltage than the reverse scan. This is a normal hysteresis. In Fig. 5.1c, the opposite situation occurs, and it is called inverted hysteresis. In Fig. 5.1b, the forward and reverse scans give the same result. In this case, it is said that hysteresis has been suppressed. In Fig. 5.1d, an energy diagram explains the observed hysteresis effects in terms of physical mechanisms such as migration of ions to the surface, modification of band bending, and influence on recombination. In the present paper, we will propose a different type of understanding of hysteresis based on the interpretation of the impedance spectroscopy spectra and the associated EC.

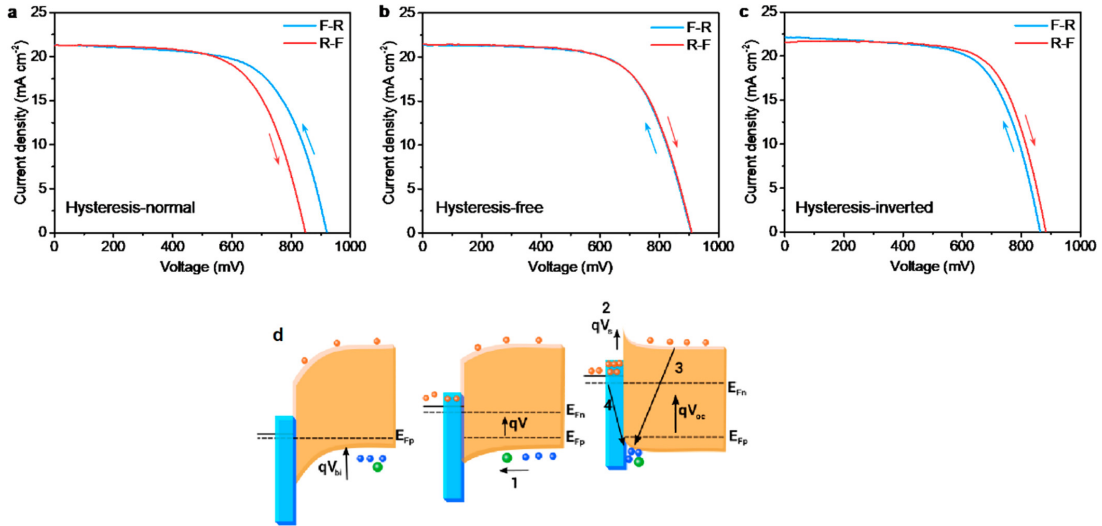


Figure 5.1: $J - V$ curves of triple-layer architecture of $c\text{-TiO}_2 / mp\text{-TiO}_2 / \text{ZrO}_2 / \text{carbon hole-conductor-free}$ printable mesoscopic PSCs with different hysteresis behaviors. (a) Hysteresis-normal device; (b) hysteresis-free device; (c) hysteresis-inverted device (F-R: from forward bias to reverse bias; R-F: from reverse bias to forward bias; scan rate 250 mV s^{-1}). (d) Diagram explaining the origin of hysteresis in this system: Process (1) indicates the kinetics of drift of cations and holes toward the interface. The accumulation of cations and holes at the interface creates an upward band bending which can be described by a surface voltage V_s represented in (2). These accumulated charges can act as a preferential zone for both recombination with electrons in the bulk (3) and in the $c\text{-TiO}_2/\text{FTO}$ region. Recombination pathway (4) is crucially dependent on the thickness of the $c\text{-TiO}_2$ layer, and is the dominant mechanism controlling recombination rates in a transient scan. Adapted with permission from ref [8]. Copyright 2017 Royal Society of Chemistry.

In the next section, still introductory, we describe major trends of the hysteresis in PSCs, as well as the general properties of the observed response in the frequency domain. Two basic but important EC models are introduced that will serve us, thereafter, to establish the correspondent behavior under cyclic voltammetry, revealing the connection between hysteresis and the EC. In the final section, we revise a set of experimental results on impedance spectroscopy and hysteresis in different PSCs that show a sound correlation, as predicted by the theory, and reveal new properties of time constants and ECs providing deep insight into the time domain behavior of perovskite solar cells.

5.2 Background of Impedance Spectroscopy and Hysteresis

5.2.1 Impedance Spectroscopy

The technique of impedance spectroscopy is amply used for the characterization of emergent solar cells [43, 44] and PSCs [11, 17, 45]. The electrical variables are the current I and voltage V measured at the contacts. The linear small perturbation variables associated with ac modulation amplitude bear a tilde, $\tilde{I}(\omega)$ and $\tilde{V}(\omega)$, whereas those associated with a steady state where the measurement was made bear an overbar, \bar{V} . The impedance is defined with respect to measurement of small perturbation signals at angular frequency ω , over a steady state at the operational point $\bar{I}(\bar{V})$

$$Z(\omega) = \frac{\tilde{V}(\omega)}{\tilde{I}(\omega)} \quad (5.1)$$

Fig. 5.2a shows the process of measurement of the impedance in terms of the small perturbations, and Fig. 5.2b incorporates an internal variable w that will be discussed in the later sections.

The impedance can be presented in terms of the real and imaginary parts

$$Z(\omega) = Z'(\omega) + iZ''(\omega) \quad (5.2)$$

The complex capacitance $C(\omega)$ is defined from the impedance as

$$C(\omega) = \frac{1}{i\omega Z(\omega)} \quad (5.3)$$

It can be separated into real and imaginary parts as

$$C(\omega) = C'(\omega) - iC''(\omega) \quad (5.4)$$

In Fig. 5.3, we show characteristic measurements of the IS response of PSCs when the conditions of illumination or photovoltage are modified, producing large changes in the parameters. In Fig. 5.4, we show the EC model that has been amply used to fit the optimized PSC devices [46, 47]. The circuit element C_g is the geometrical capacitance corresponding to dielectric polarization in the bulk, and C_1 is the large low-frequency (LF) capacitance associated with the

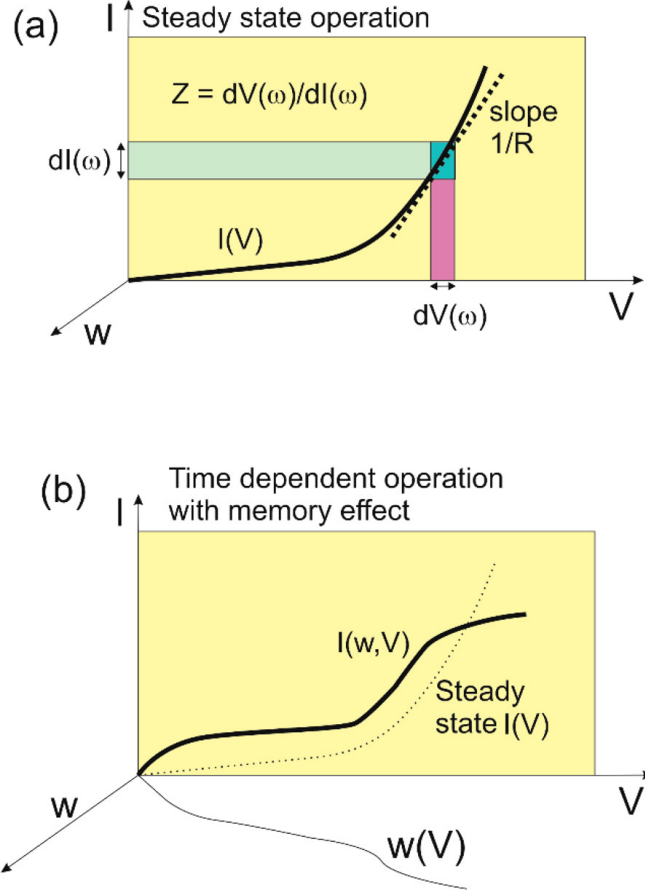


Figure 5.2: (a) Scheme of a current-voltage ($I - V$) curve indicating the measurement of small perturbation voltage and current that provide the impedance Z . At low frequency, the slope of the $I - V$ curve is the reciprocal resistance. (b) In the presence of the memory internal variable w , the actual $I - V$ curve depends on the evolution of w . The curve departs from the steady-state curve and shows hysteresis.

generation of the ionic double layer in the vicinity of the contacts [11, 48]. The capacitance-frequency plot (Fig. 5.4b) shows a plateau at high frequencies (HF) corresponding to C_g and increase toward the LF value, where the slow kinetics of C_1 becomes activated. The real part of the capacitance calculated from eq 5.3 at LF is

$$C'(\omega = 0) = C_g + \left(\frac{R_1}{R_1 + R_3} \right)^2 C_1 \quad (5.5)$$

The two arcs in Fig. 5.3a and 4a are associated with two resistances. We denote the LF arc resistance as R_1 (the parallel connection of R_1 to C_1 generates the LF arc) and the HF resistance as R_3 . The meaning of the resistances depends on the illumination conditions, but the LF arc usually relates to the

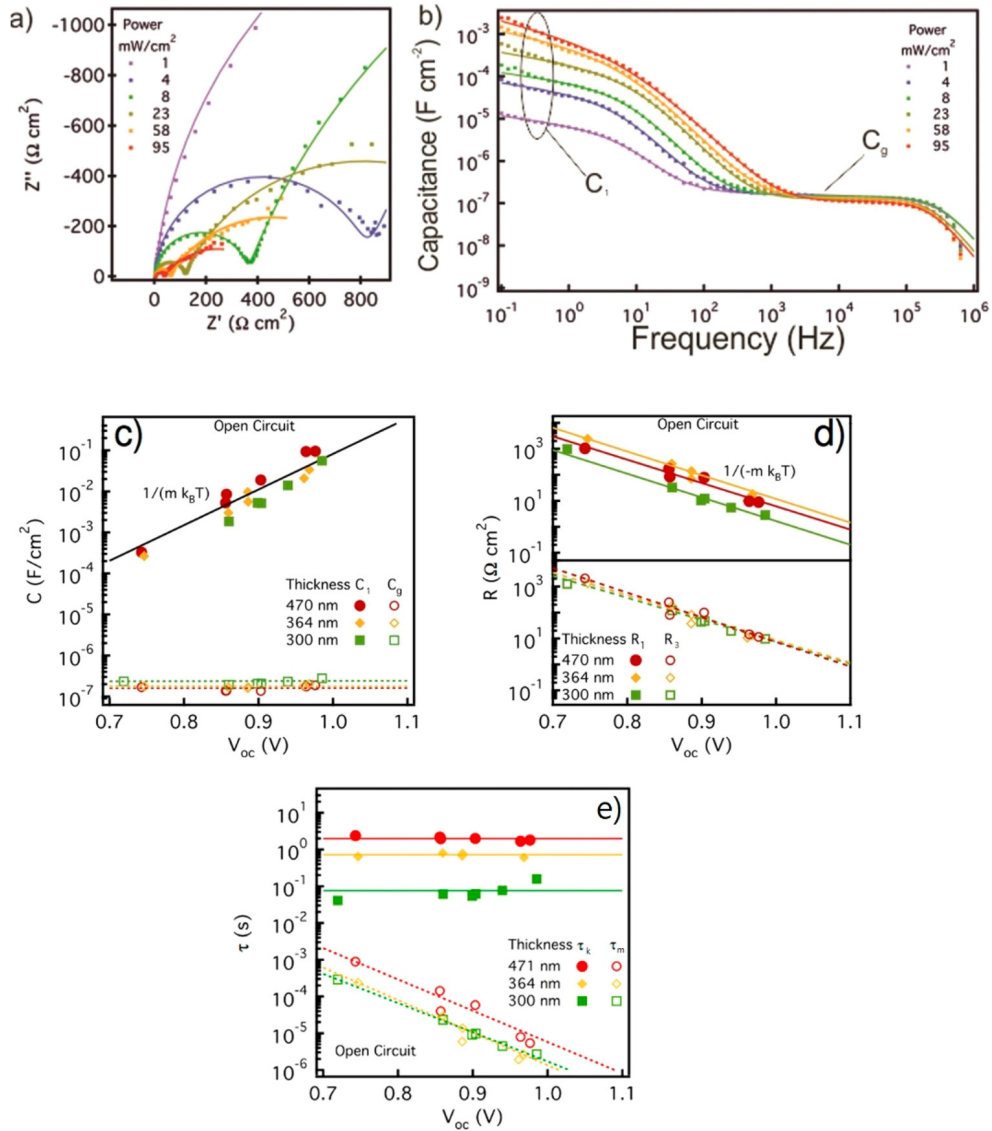


Figure 5.3: Impedance spectroscopy results of a planar structure FTO / TiO₂ / MAPbI₃ / Spiro-OMeTAD / Au solar cell. (a) Example of complex plane impedance plot measured under short-circuit conditions at different irradiation intensities. (b) Example of capacitance spectra corresponding to the conditions in panel (a). Solid lines correspond to fits using the EC. (c) Capacitances and (d) resistances under open-circuit conditions. Solid lines (low-frequency arc) and dashed lines (high-frequency arc) correspond to linear fits with m approaching 2. In panel (c), $m = 1.90 \pm 0.17$, and in panel (d), $m = 1.94 \pm 0.08$. (e) Response time calculated from the RC product for the low-frequency arc (solid line) and high-frequency arc (dashed line). Reproduced from [46]. Copyright 2016 American Chemical Society.

perovskite/contact interface (ion migration, accumulation, and recombination) [49].

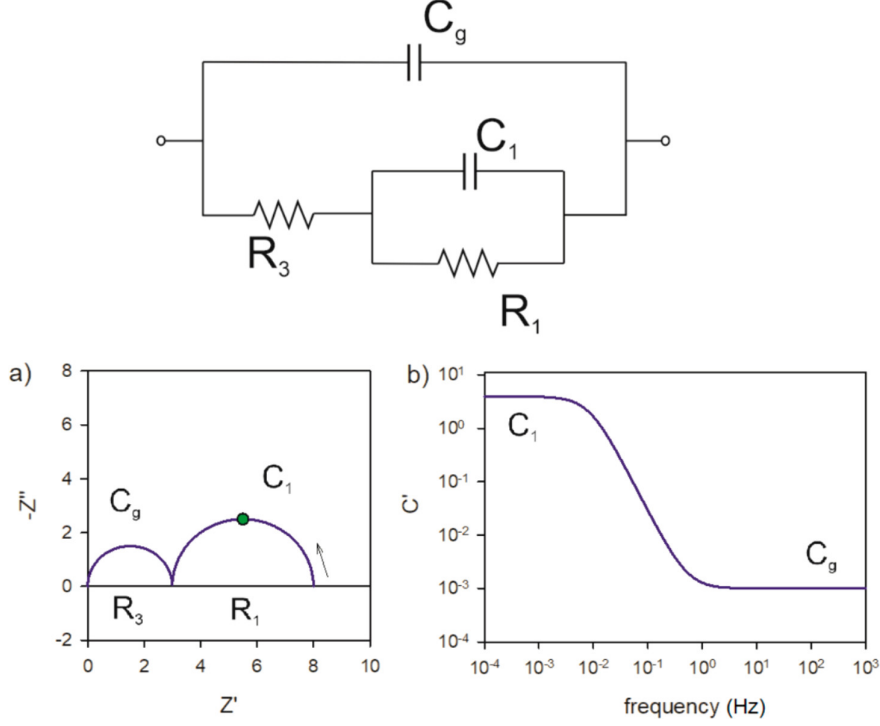


Figure 5.4: Equivalent circuit and (a) complex plane impedance spectrum (impedances in Ω). The arrow indicates the direction of increasing frequency. The point indicates the angular frequency $1/\tau_1 = 1/R_1C_1$. (b) Real part of the capacitance versus frequency. Parameters $R_1 = 5 \Omega$, $R_3 = 3 \Omega$, $C_1 = 10 \text{ F}$, $C_g = 10^{-3} \text{ F}$.

We note that from the fitted parameters under open-circuit conditions in Fig. 5.3b,c, the geometric capacitance is basically constant, but the other three parameters in the EC show an exponential dependence with the voltage (Fig. 5.3d) [50]; therefore, they may be expressed as

$$R_1(V) = R_{10}e^{-qV/m_1k_B T} \quad (5.6)$$

$$C_1(V) = C_{10}e^{-qV/m_C k_B T} \quad (5.7)$$

$$R_3(V) = R_{30}e^{-qV/m_3 k_B T} \quad (5.8)$$

where V is the solar cell voltage, q is the elementary charge, $k_B T$ is the thermal energy, and m_i is an ideality factor for each parameter. In the case of band-to-band recombination, it is $m = 1.54$. The values indicated in Fig. 5.3c,d are $m \sim 2$ in all cases. It is remarkable that the two elements of the low-frequency arc are strongly correlated, $m_C \sim m_1$, so that the response time for the slow relaxation phenomenon is a constant independent of the voltage

[11, 46, 51]

$$\tau_1 = R_1 C_1 \quad (5.9)$$

This is observed in Fig. 5.3e. It should be mentioned that these good correlations are obtained measuring each voltage point at open circuit, in the absence of background current. In contrast to this, the high-frequency relaxation time

$$\tau_m = R_3 C_g \quad (5.10)$$

is not constant and follows the trend of $R_3(V)$.

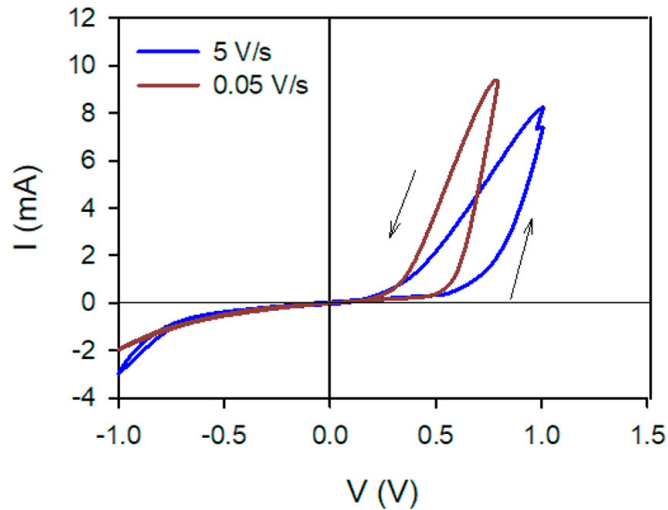


Figure 5.5: Current-voltage scans of a FTO / PEDOT:PSS / 2D Ruddlesden-Popper perovskite / Ag (15 nm) / Au (85 nm) memristor device in the dark at different scan rates.

By definition, memristor devices undergo strong memory effects and become interesting platforms for the analysis of hysteresis. Perovskite interfacial conductivity can be controlled by the ionic displacement and reaction, giving rise to memristive devices [52, 53]. A similar two-arc response as in PSCs has been observed in perovskite-based memristor devices at low applied voltages [53]. Fig. 5.5 shows the current-voltage loops in the dark of a memristor based on 2D halide perovskite with a Ag contact layer. The device shows a strong memory effect that causes the forward and reverse scan to be well-separated, even at slow scan rates. This is associated with the construction of a conductive ionic layer at the Ag contact [52, 53]. Note that Fig. 5.5 can be viewed as a huge inverted hysteresis of the type of Fig. 5.1c, with the corresponding semilog $I - V$ curve

shown in Fig. 5.6a. In the impedance spectroscopy response at low voltages in Fig. 5.6b, the same types of two-arc spectra are observed as in Fig. 5.3 [53]. However, when the memristor approaches the voltage of the transition to a low resistance state (LRS), that is, at about 0.5 V, a new feature appears in which the LF arc reduces size and enters the fourth quadrant of the complex plane, as shown in the enlarged view in the inset of Fig. 5.6b. This behavior consisting of a “hook” at low frequency has been observed in many of the halide perovskite solar cells [54–57]. The EC model shown in Fig. 5.7 contains a single RC process coupled to an RL line that describes the hook shape. In terms of the Laplace variable $s = i\omega$, the impedance of Fig. 5.7 takes the form

$$Z(\omega) = [R_b^{-1} + C_m s + (R_a + L_a s)^{-1}]^{-1} \quad (5.11)$$

Depending on the values of the circuit parameters, the impedance can show an inductive loop or not, as noted in the different types of spectra in Fig. 5.7a,c,d. The parallel RL line has been proposed in the literature in relation to the negative capacitance observed in solar cells (Fig. 5.7b) [58, 59]. The inductive loop describes a general memory effect, and it has been observed in metal oxides [60], in LiNbO₂ memristors [61], and in proton exchange membrane (PEM) fuel cells [62]. In PSC, it can be justified from a recent kinetic model [63, 64], in which an internal surface voltage that is slowed down by ionic motion relaxes to the quasi-equilibrium state imposed by the external voltage V applied to the solar cell.

In terms of the EC, the operation of the memory mechanism consists of modifying the overall resistance of the system as a function of the frequency. At high frequency, the impedance of the inductor is very large and R_a does not contribute to the response. When the frequency is reduced, the impedance of the inductor vanishes progressively, and the loop in the fourth quadrant reduces the overall resistance of the system.

A related issue that has been intensely discussed in the area of PSC is the meaning of the often observed negative capacitance [18, 55, 56, 58, 59, 65–67] that causes great uncertainty of interpretation. We remark that the EC of Fig. 5.7 consists of a positive inductor not a negative capacitor. However, as shown in Figs. 5.3 and 5.4, it is useful to plot the capacitance versus the frequency. In

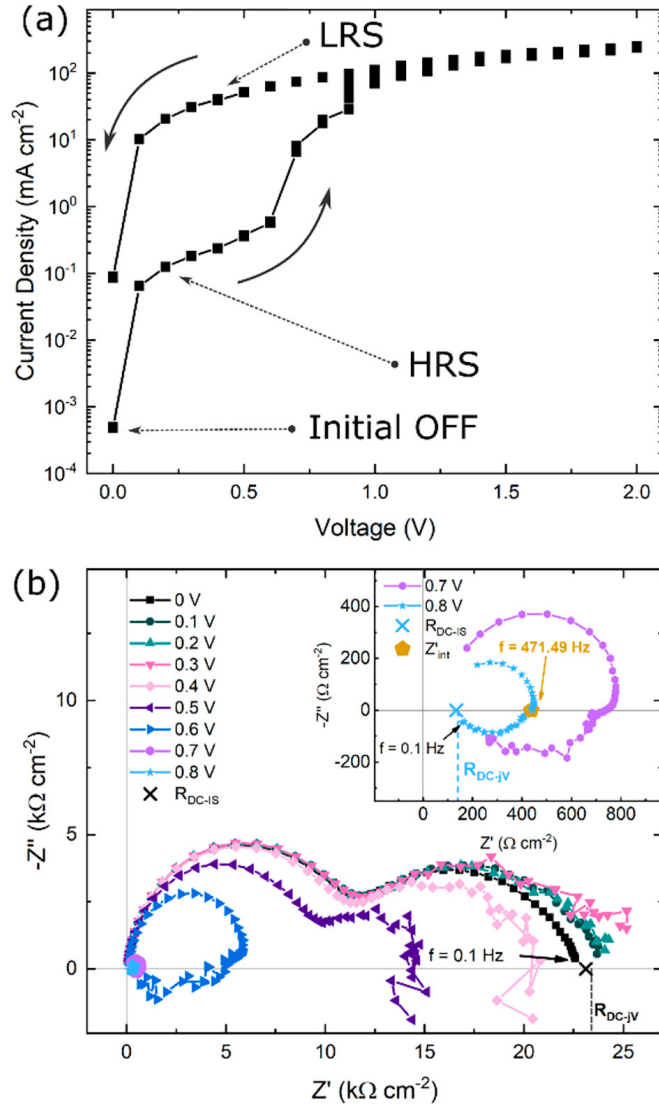


Figure 5.6: (a) Semilog current-voltage curve of a FTO / PEDOT:PSS / 2D Ruddlesden-Popper perovskite / Ag (15 nm) / Au (85 nm) memristor device showing the transition from high resistance state to low resistance state. (b) Impedance spectroscopy spectra evolution of the memristor at representative voltages. Reprinted with permission from ref [53]. Copyright 2021 American Institute of Physics.

the calculation of the real part of the capacitance by eq 5.3, the positive inductor RL line produces a negative capacitance effect (Fig. 5.7b). This is a customary denomination, but there are no negative elements in this model.

An EC such as those in Figs. 5.4 and 5.7 is not unique. It allows a number of possibilities of alternative expressions [68]. The adoption of a particular EC model is based on the physical interpretation of the elements based on experi-

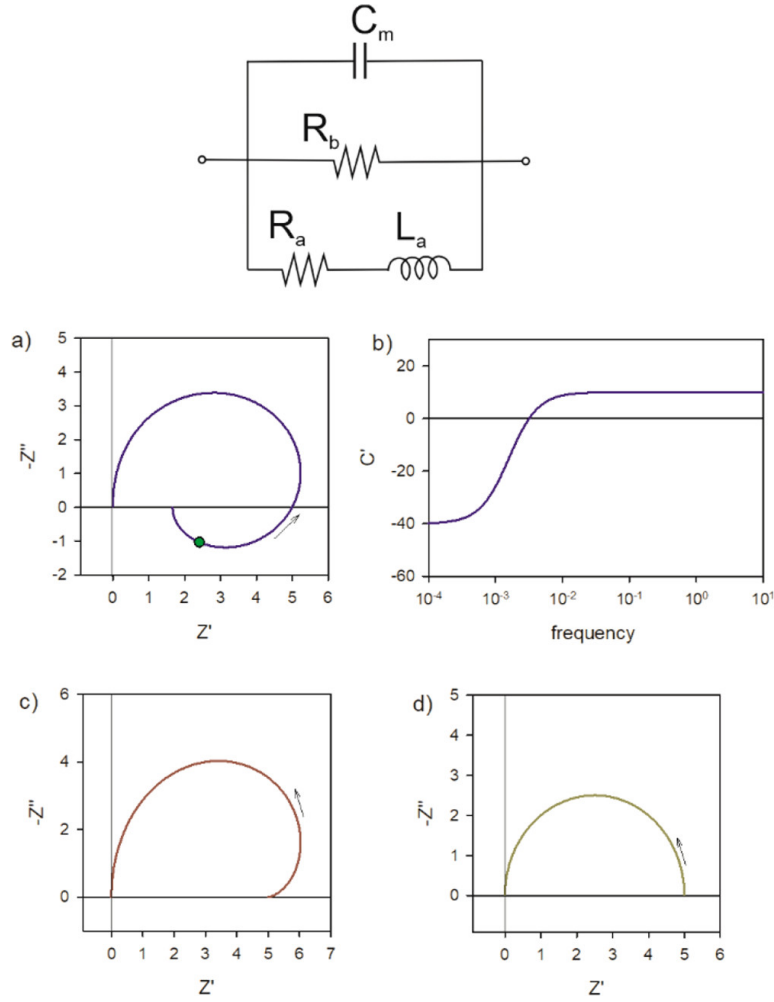


Figure 5.7: Equivalent circuit including an inductive branch and the associated complex plane impedance spectra. (a) $R_a = 2$, $R_b = 10$, $C_m = 10$, $L_a = 200$, (c) $R_a = 10$, $R_b = 10$, $C_m = 10$, $L_a = 1000$, (d) $R_a = 2$, $R_b = 10$, $C_m = 100$, $L_a = 100$. The arrow indicates the direction of increasing frequency. (b) Real part of the capacitance of the system parameters in (a). The highlighted point in (a) is at the angular frequency $1/\tau_k = R_a/L_a$.

ments in different configurations of the solar cell.

5.2.2 Relation between IS Values and $J - V$ Curve

We show the connection of the $J - V$ curve to the impedance Z with a simple example. Fig. 5.2a shows the small amplitude perturbation quantities in a point of the steady-state curve. Here, we restrict the analysis to the stationary condition, $\omega = 0$, and the impedance reduces to the DC resistance:

$$Z = R_{DC}(V) \quad (5.12)$$

These small amplitudes of the electrical perturbations can be treated as differentials, $\tilde{I}(\omega) \rightarrow dI$, $\tilde{V}(\omega) \rightarrow dV$. Hence eq 5.1 becomes

$$dI = \frac{1}{R_{DC}(V)} dV \quad (5.13)$$

As shown in Fig. 5.2a, $R_{DC}(V)$ is the reciprocal slope at each point of the curve. Let us suppose we measure the impedance at different voltages, and we arrive at the form

$$R_{DC}(V) = R_{DC0} e^{-qV/mk_B T} \quad (5.14)$$

Inserting eq 5.14 into 13 and performing the integration, we obtain the diode equation of the solar cell

$$I(V) = \frac{mk_B T}{qR_{DC0}} (e^{qV/mk_B T} - 1) \quad (5.15)$$

This trivial example shows that current voltage curve is linked to impedance spectroscopy by an integration. Our objective is to develop a general integration method valid for any EC and for all the frequencies related to a certain stimulus in the time domain represented by a specific applied voltage schedule $V(t)$.

5.2.3 Properties of Hysteresis in Perovskite Devices

Fig. 5.8 shows the measurements of the $J - V$ curve at a constant voltage sweep rate by following a ramp of voltage at successive voltage steps. When the steps take a long duration of 1 s, the forward and backward results are the same (Fig. 5.8a). However, for faster steps of duration 0.1 s, the relaxation to an equilibrium value has not been yet completed when the new step comes in. Hence, the scan in the forward direction shows currents lower than those of the stationary curve, and the scan in the reverse direction shows larger currents (Fig. 5.8b). Fig. 5.8c shows that the amount of hysteresis increases with the scan rate. The opening of the curve can be quantified by a hysteresis index defined by the change of a given property of the $J - V$ curve with respect to the velocity parameter [69]. This is useful to track the evolution of the hysteresis with some internal or external parameter, as the thickness of a layer in the solar cell (Fig. 5.1) or the humidity (Fig. 5.11).

In Fig. 5.8b, we can see that the overall hysteresis response can be obtained as a sum of the results of small perturbation steps. This is the essence of the

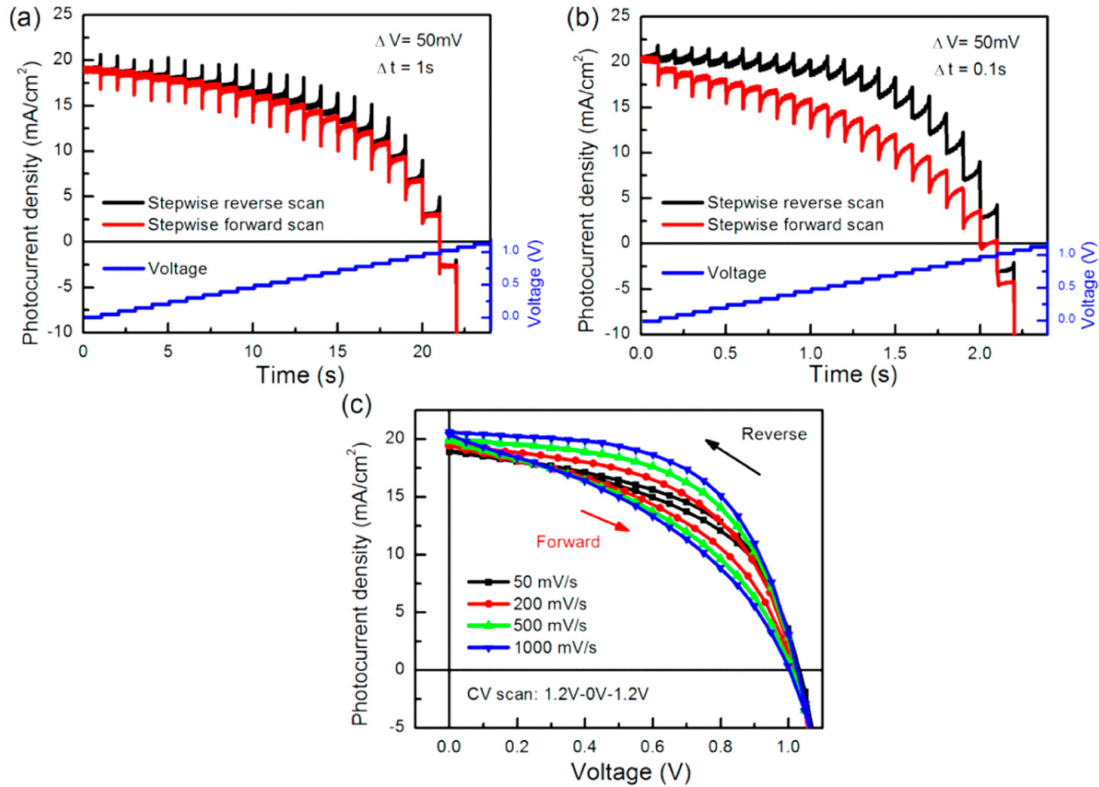


Figure 5.8: Time-dependent photocurrent response of planar perovskite solar cell on compact TiO_2 (cp- TiO_2) with 500 nm $\text{CH}_3\text{NH}_3\text{PbI}_3$ film as the light-absorber layer and 150 nm spiro-OMeTAD as the HTM layer under reverse and forward stepwise scans with (a) 1 s step time and (b) 0.1 s step time. (c) $J - V$ response for PSCs with different CV scan rates. Reproduced from ref [7]. Copyright 2015 American Chemical Society.

integration method in a kinetic situation that will be developed below: we will establish the same procedure mathematically.

It has been widely recognized that there is a strong connection between IS properties and the hysteresis features of PSCs. More concretely, the capacitive effect is well-recognized to be associated with hysteresis [7, 18, 70, 71]. The capacitive current increases with scan rate in forward direction [72] and changes sign when the direction of the scan is inverted, as shown in Fig. 5.9a. Since Fig. 5.9a shows the change of the dark current, it is related to a decrease of photocurrent in forward scan, as shown in Fig. 5.1a. This is termed capacitive current in a general sense. In contrast, no capacitive current is observed for an inverted contact structure device in Fig. 5.9b.

As an example of the correlation of capacitance and hysteresis, Fig. 5.10

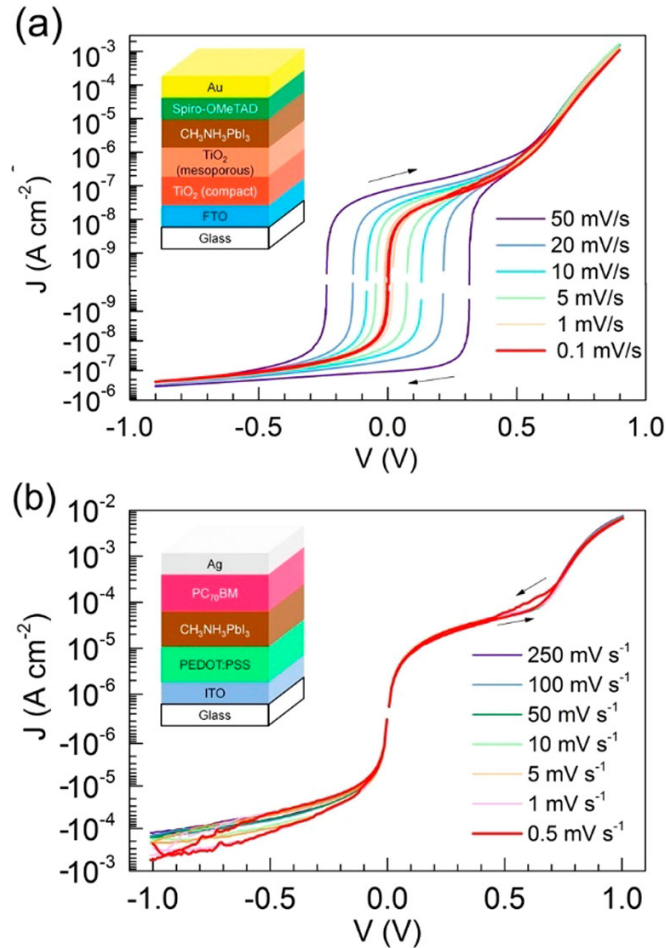


Figure 5.9: Dark $J - V$ curves at room temperature in logarithm scaled current representation: (a) Regular mesoporous PSC and (b) inverted PSCs at different scan rates with corresponding structures illustrated in the insets. Reproduced from [6]. Copyright 2016 American Chemical Society.

shows [5] the effect of capacitive hysteresis in two PSCs: one cell with TiO₂ contact (Fig. 5.10a) and a low-capacitance PSC with organic electron selective contact [13, 14]. The cell with TiO₂ contact displays a large capacitance at low frequency in both dark and illuminated conditions (Fig. 5.10d,e). Hysteresis in this cell is much larger than that in the cell with the organic contact (Fig. 5.10b). In addition, the time-dependent short-circuit current, J_{SC} , of the normal structure exhibiting the severe normal hysteresis shows an exponential decay attributed to the accumulated capacitive current (Fig. 5.10c) [5].

We have commented that in Figure 1c different behavior is observed. The forward scan increases the photovoltage, and this is called inverted hysteresis [8, 73, 74]. Note in Fig. 5.9b that, in a voltage sweep, the current changes in

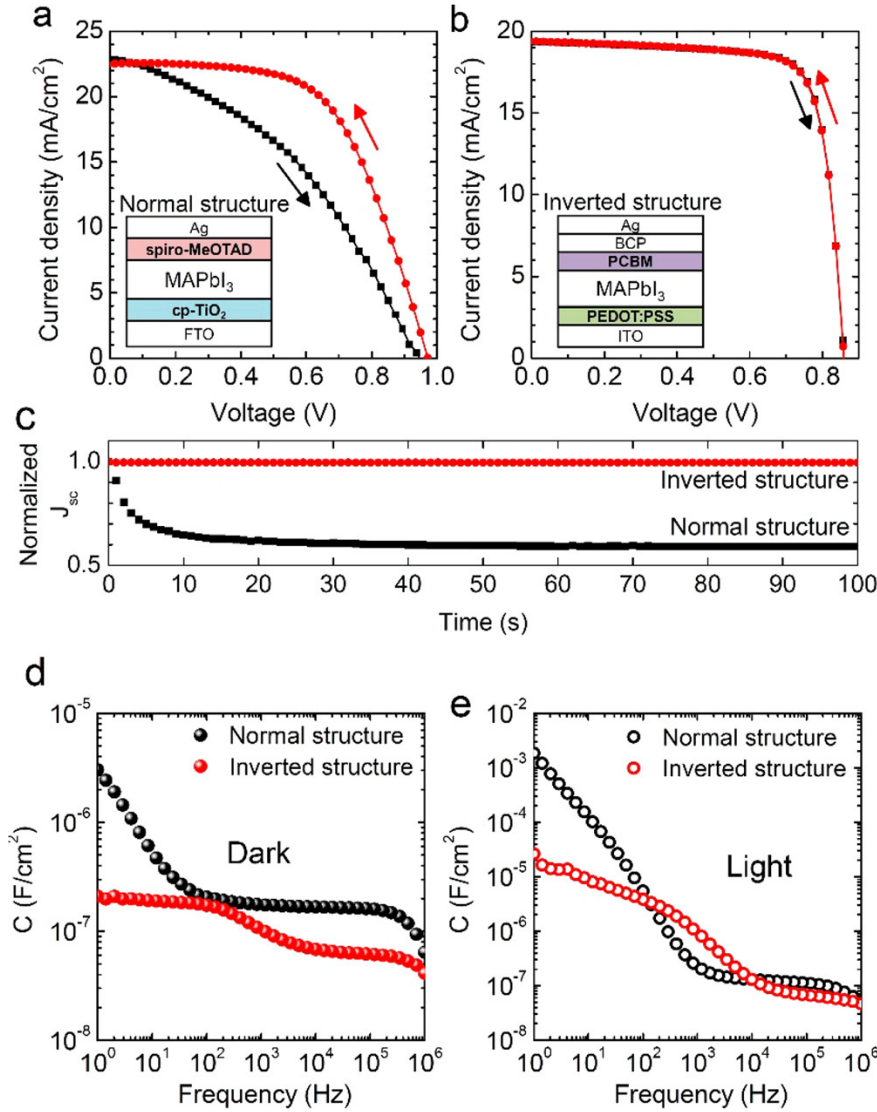


Figure 5.10: (a) $J - V$ hysteresis of the cp-TiO₂ / MAPbI₃ / Spiro-MeOTAD (normal) structure and (b) PEDOT:PSS/MAPbI₃/ PCBM (inverted) structure. During the $J - V$ scan, the current was acquired for 100 ms after applying a given voltage. (c) Normalized time-dependent short-circuit current density (J_{SC}) of the normal and the inverted structures. Open-circuit condition under one sun illumination was maintained before measuring J_{SC} . Capacitance-frequency ($C - f$) curves (d) under dark and (e) one sun illumination at short-circuit condition (bias voltage = 0 V). Reproduced from ref [5]. Copyright 2015 American Chemical Society.

the opposite way to the capacitive variation. By the relation of noncapacitive currents (Fig. 5.5 and Fig. 5.9b) and the inductor element, we may speak of inductive hysteresis (inverted) versus capacitive hysteresis (regular). Indeed, the connection between the inductive branch of the impedance results and the

inverted type of hysteresis in PSCs has been exposed by Fabregat- Santiago and co-workers, as shown in Fig. 5.11 [75]. They have associated the presence of the inductive loop (Fig. 5.11c,d) to a negative hysteresis index (Fig. 5.11b) that indicates an inverted hysteresis (Fig. 5.11a). However, a physical explanation for this connection between time and frequency domain results has not been elaborated. In the context of our methods developed below, we will show a clear scheme for this correlation.

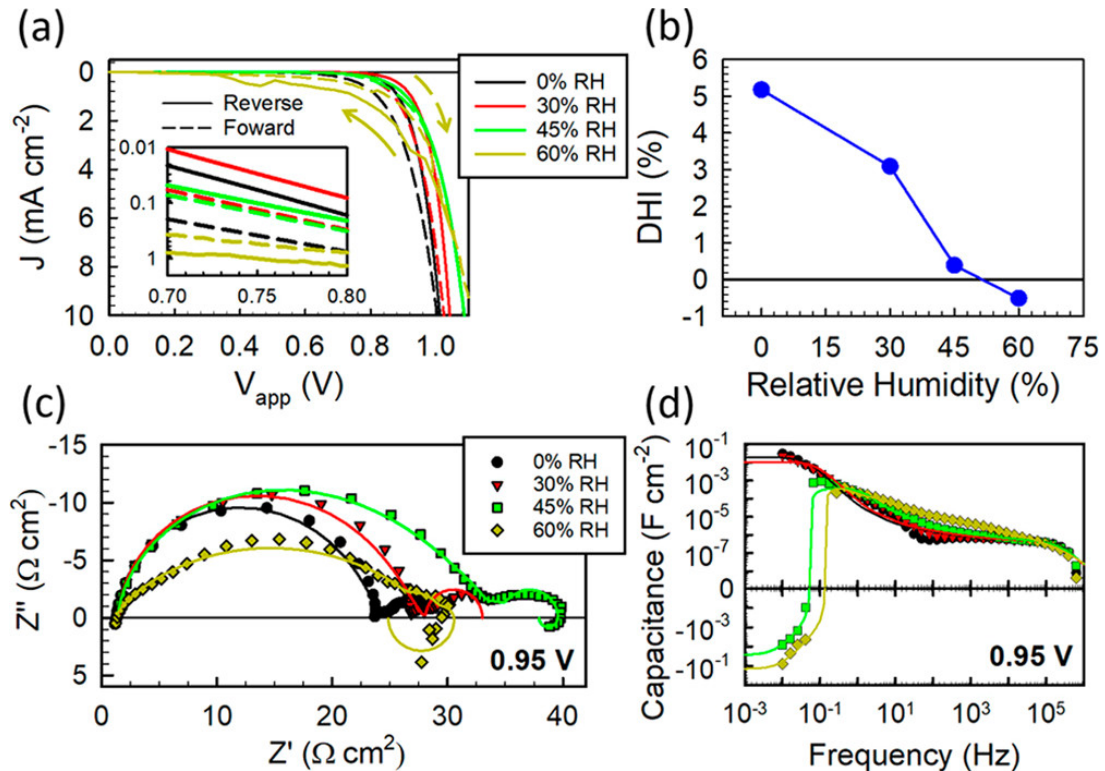


Figure 5.11: Measurements of regular MAPbI₃ solar cells (FTO / TiO₂ / mp-TiO₂ / MAPbI₃ / Spiro-OMeTAD / Au) at different relative humidity values (0, 30, 45, and 60%) under dark conditions. (a) CV curves and (b) their respective hysteresis index. (c) Impedance plots with (d) corresponding capacitance spectra at 0.95 applied voltage. Solid lines correspond to fits using the EC including a RL branch. Reproduced from ref [75]. Copyright 2020 American Chemical Society.

5.3 $J-V$ Hysteresis from the Equivalent Circuit

We start the description of the methodology to describe hysteresis features based on information in the frequency domain. The general operation to switch between time and frequency domain is the Laplace transformation and its inverse,

according to the desired direction. However, in the case of the experimental methods used to measure solar cells and related devices, the connection between time and frequency domain is not obvious. In the measurement of the impedance spectra of Fig. 5.3a, the system has been stabilized at a steady state, and the linear response $Z(\omega)$ is obtained by very small voltage amplitudes dV (Fig. 5.2a). In contrast, for the measurement of CV, the voltage makes a large excursion of about 1 V, as shown in Fig. 5.8, at a scan rate v_0 according to the expression

$$V(t) = V_0 + v_0 t \quad (5.16)$$

Typical sweep voltage rates start at 10 mV/s up to 100 V/s or more. In the fast voltage sweep, the physical processes in the sample are not sitting close to a quasi-equilibrium state, and the full nonlinearity and memory effects come into play, determining the response to the perturbation. We can invent a model based on detailed internal mechanisms that produces the required observed responses: electrical fields, ions situated in the wrong side of the polarization that screen the field, interfacial traps, surface barriers that change by photogenerated charges that pile up at the barrier, enhanced recombination in the absorber, and so on. However, each model can be arbitrary to a large extent requiring plenty of explanations. Our goal is to provide a methodology to pass directly from the impedance response obtained at the different voltages of the range of measurement to the large perturbation response like that in eq 5.16.

It seems hopeless at first sight since the information that we have is represented by an impedance function like eq 5.11 and the voltage dependence of the circuit elements obtained from fitting the spectra at different steady states. However, very often, the linearized response contains significant information about the response to a large-scale perturbation. These methodologies are widely used in electrical engineering, in stability and bifurcation and for the analysis of oscillating systems based on impedance spectroscopy [76, 77]. These methods define a dynamical system by a set of differential equations that refer to external variables applied to the system, that is, current I , voltage V , illumination, and a set of internal state variables w_i that correspond to the relevant evolving quantities that determine the internal evolution with time. By stating an initial condition to all the variables, the differential equations allow one to predict the evolution

of the system.

It is well-recognized that impedance spectroscopy has a great advantage in allowing separation of internal processes that determine the overall spectral response, for example, manifested as two neatly distinguished arcs in Fig. 5.3a. The central tool to obtain an interpretation of the impedance response is to establish an EC model. Then we can represent the system's response by the voltage dependence of the resistances, capacitors, and inductors in the EC.

Consider a PSC that shows an amount of hysteresis when $J - V$ is measured by a cycling method, as indicated in the top box of Fig. 5.12. We also have obtained the impedance spectra at different points of the quasi-stationary curve as indicated in the left diagram. We assume that we have determined an EC that describes the spectra over the whole voltage range of interest. We have also characterized the voltage dependence of parameters. Examples of such type of data information are in Fig. 5.3c,d and later on Fig. 5.20. Now we apply a method that converts the EC into a set of dynamical equations for the relevant variables in the system:

- V : the voltage at the contacts; this is the external input variable that we can program according to the chosen technique of measurement
- I : the current at the contacts; this is the external output variable
- $w_1, w_2, w_3 \dots$: internal state variables

The effect of the internal variables on a general curve with memory effect $I(V, w)$ is shown in Fig. 5.2b. The system's evolution depends not only on the present state of the external input V but also on the evolution of the internal variables w_i . Therefore, from the EC model, we can derive a set of differential equations where the voltage-dependent circuit elements derived experimentally provide the coefficients in the equations. Then we can solve mathematically, either analytically or by a numerical integration, and we arrive at the output response $I(V)$ for the particular imposed trajectory of $V(t)$. This is the lower box in Fig. 5.12. Finally, the theoretical scan rate-dependent $J - V$ curves are then reconstructed and are correlated to the experimentally determined data. Using this approach, we obtain an independent description of the observed hysteresis.

Furthermore, we can obtain an interpretation of the hysteresis by the effect of different elements in the EC, and we can investigate such elements independently to modify or improve the system's response in the time domain.

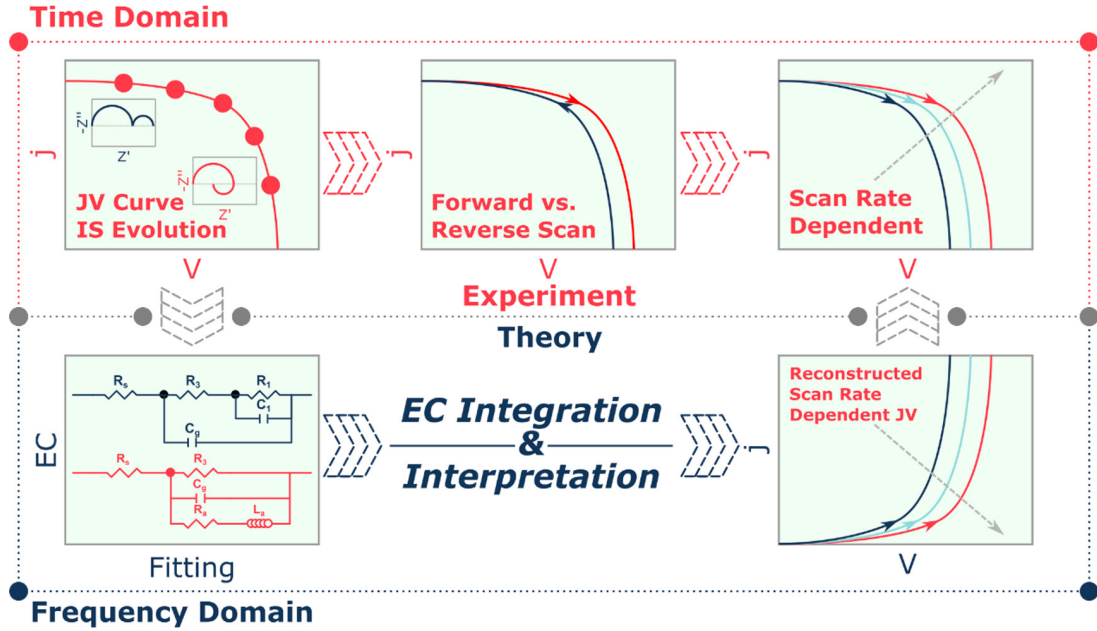


Figure 5.12: Integration scheme of the equivalent circuit from frequency domain to time domain.

5.4 Capacitive Circuit Model

5.4.1 Converting the Equivalent Circuit to Time Domain Equation

We describe the method to systematically convert the equations for the currents and voltages in the EC into a set of first order differential equations. We explain the method applied to the standard circuit of the PSC in Fig. 5.4, as shown in Fig. 5.13. The node voltage method to solve a circuit will provide the required structure of equations in the frequency domain. It has the following steps

- i. Assign a reference node
- ii. Assign node voltage names to the remaining nodes
- iii. Write Kirchoff's current law for each node

- iv. Manipulate the equations to the required form that will provide kinetic equations in the time domain

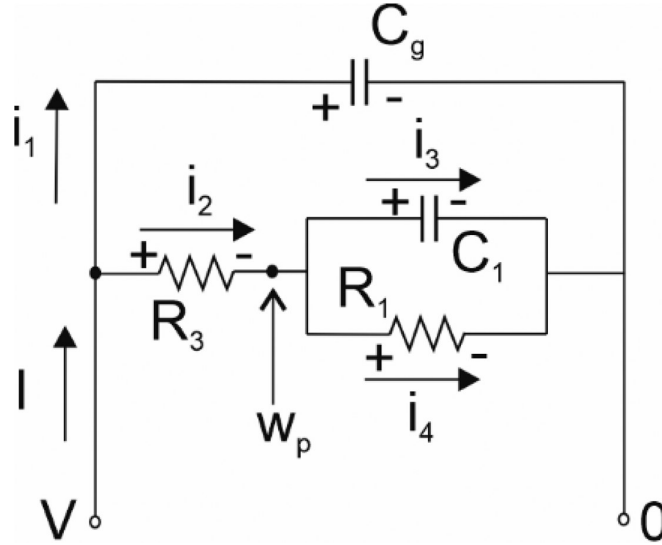


Figure 5.13: Application of the node voltages method to solve the capacitive circuit of Fig. 5.5.

Note that currents and voltages in Fig. 5.13 bear a tilde (not shown in the figure) since they correspond to the small amplitude of IS measurements. The zero node is at the right-hand side in Fig. 5.13. The external voltage \tilde{V} determines one node, and the external current is \tilde{I} . The other node is assigned a voltage \tilde{w}_p . This is the single internal state variable. We write the Kirchhoff equations for the two nodes. The result is

$$\tilde{I} = sC_g\tilde{V} + \frac{1}{R_3}(\tilde{V} - \tilde{w}_p) \quad (5.17)$$

$$\frac{1}{R_3}(\tilde{V} - \tilde{w}_p) = sC_1\tilde{w}_p + \frac{\tilde{w}_p}{R_1} \quad (5.18)$$

When taking the transformation to the time domain, the product by s gives the time derivative. We need to convert eqs 5.17 and 5.18 to a form in which each voltage is multiplied by s . By solving the equations, we find

$$sR_3C_g\tilde{V} = R_3\tilde{I} - (\tilde{V} - \tilde{w}_p) \quad (5.19)$$

$$sR_1C_1\tilde{w}_p = \frac{R_1}{R_3}\tilde{V} - \left(1 + \frac{R_1}{R_3}\right)\tilde{w}_p \quad (5.20)$$

Using the relaxation times introduced in eqs 5.9 and 5.10, we obtain the required differential equations in the time domain

$$\tau_m \frac{d\tilde{V}}{dt} = R_3 \tilde{I} - (\tilde{V} - \tilde{w}_p) \quad (5.21)$$

$$\tau_1 \frac{d\tilde{w}_p}{dt} = \frac{R_1}{R_3} \tilde{V} - \left(1 + \frac{R_1}{R_3}\right) \tilde{w}_p \quad (5.22)$$

5.4.2 Steady-State Solution

Let us first analyze the steady state in which $dt \rightarrow \infty$. Then we have

$$\tilde{I} = \frac{1}{R_3} (\tilde{V} - \tilde{w}_p) \quad (5.23)$$

$$\tilde{w}_p = \frac{R_1}{R_1 + R_3} \tilde{V} \quad (5.24)$$

Therefore

$$\tilde{I} = \frac{1}{R_{DC}} \tilde{V} \quad (5.25)$$

At zero frequency, the impedance is the total resistance, as previously explained in eq 5.13. The DC resistance in eq 5.25 is

$$R_{DC} = R_1 + R_3 \quad (5.26)$$

5.4.3 General Method of Solution

The EC model of Fig. 5.13 needs to be supplemented with the voltage dependence of the different elements. We use the exponential dependences in eqs 5.6 - 5.8. To simplify the problem, we assume that the different elements have the same ideality factor $m_i = m$. The correlation of the voltage dependence of resistances and capacitances is a realistic assumption observed experimentally [38, 39], but this is not generally satisfied; see Fig. 5.20 [50, 51]. The assumption $m_i = m$ allows us to solve completely the problem by analytical methods, without loss of generality. We thus have

$$R_1(V) = R_{10} e^{-V/V_m} \quad (5.27)$$

$$C_1(V) = C_{10} e^{V/V_m} \quad (5.28)$$

$$R_3(V) = R_{30} e^{-V/V_m} \quad (5.29)$$

where the ideality factor m in terms of voltage is defined as

$$V_m = \frac{mk_B T}{q} \quad (5.30)$$

If the assumption in eqs 27-29 is not satisfied, then the whole process must be performed by numerical integration. For convenience, we define

$$r_0 = \frac{R_{10}}{R_{30}} \quad (5.31)$$

$$r_1 = 1 + r_0 \quad (5.32)$$

In order to continue the analysis toward a solution, we make a further simplification valid for slow measurements. As τ_m is quite short, as shown in Fig. 5.3e, it is unlikely that we can observe the relaxation process associated with $R_3 C_g$. Therefore, we remove the term with the time derivative in eq 5.21. This is equivalent to ignoring the geometrical capacitance C_g . On the other hand, the relaxation of w_p is slow and will influence the measured $I - V$ curve, hence we leave the term with the derivative in eq 5.22. We obtain the equations

$$\tilde{I} = \frac{1}{R_3(\bar{V})} (\tilde{V} - \tilde{w}_p) \quad (5.33)$$

$$\tau_1 \frac{d\tilde{w}_p}{dt} = \frac{R_1(\bar{V})}{R_3(\bar{V})} \tilde{V} - \left(1 + \frac{R_1(\bar{V})}{R_3(\bar{V})}\right) \tilde{w}_p \quad (5.34)$$

These two equations have the functional form of a memristive system [36]: eq 5.33 is the conductance equation depending on the internal memory variable \tilde{w}_p , and eq 5.34 describes the temporal evolution of the memory variable. Equations 21 and 22, or the more concrete form 33 and 34, must be solved combined for a given external perturbation $V(t)$ to provide the external current I . The external perturbation depends on the technique that is used: it could be a step voltage, a large sinusoidal, or any required form. For the $J - V$ hysteresis problem, we focus our interest in the voltage variation at a constant voltage sweep rate v_0 that is termed CV in electrochemistry, as described by eq 5.16. In the following sections, we will solve the current for CV technique. We will start with a description of the voltage ramp in the forward direction ($v_0 > 0$).

For any possible specification of $V(t)$, we need to remark that the eqs 5.33 and 5.34 are not symmetric. The time dependence of \tilde{w}_p can be obtained only from eq 5.34. Since $V(t)$ is known, only when $\tilde{w}_p(t)$ has been solved, then the

solution of eq 5.33 can be attempted. Therefore, the process of integration begins with the equation for the memory variable(s).

5.4.4 Integration of the Memory Equation

We search the solution $I = I(V, v_0)$ starting with the eq 5.34 for the variable with memory w_p . For simplicity, we choose to work with the voltage V as the independent variable, instead of time, since the state of the system is fixed by the instantaneous voltage by eq 5.16. We express the scan rate as

$$V_s = \tau_1 v_0 \quad (5.35)$$

and we can write

$$V_s \frac{d\tilde{w}_p}{dV} = r_0 \tilde{V} - r_1 \tilde{w}_p \quad (5.36)$$

An integration of the differential eq 5.36 starting at V_0 gives the evolution of $w_p(V)$ during a forward voltage scan

$$w_p(V) = \left(-\frac{r_0}{r_1} V_0 + w_{p0} + \frac{r_0}{r_1^2} V_s \right) e^{-r_1/V_s(V-V_0)} + \frac{r_0}{r_1} V - \frac{r_0 V_s}{r_1^2} \quad (5.37)$$

5.4.5 Integration of the Conductance Equation: Steady-State Solution

The next and final step is the integration of eq 5.32 for a large amplitude voltage scan. First, let us assume that the variable w_p reaches the equilibrium value in eq 5.24. Then the variation of I expressed in eq 5.33 is

$$dI = \frac{1}{R_1(V) + R_3(V)} dV \quad (5.38)$$

This equation is the statement that the resistance is the derivative of the $I - V$ curve, as discussed in section 5.2.2. The integration from V_0 to V given the initial current I_0 results to

$$I_s(V) = I_0 + \frac{V_m}{R_{10} + R_{30}} (e^{V/V_m} - e^{V_0/V_m}) \quad (5.39)$$

This is the stationary $I - V$ curve, like eq 5.15, that is obtained at infinitely slow sweep velocity, or in any case in which the memory effects of w_p can be neglected. $I_s(V)$ is shown in the blue curve of Fig. 5.14. Equation 5.39 is also the $I - V$ curve under illumination (with an added negative photocurrent).

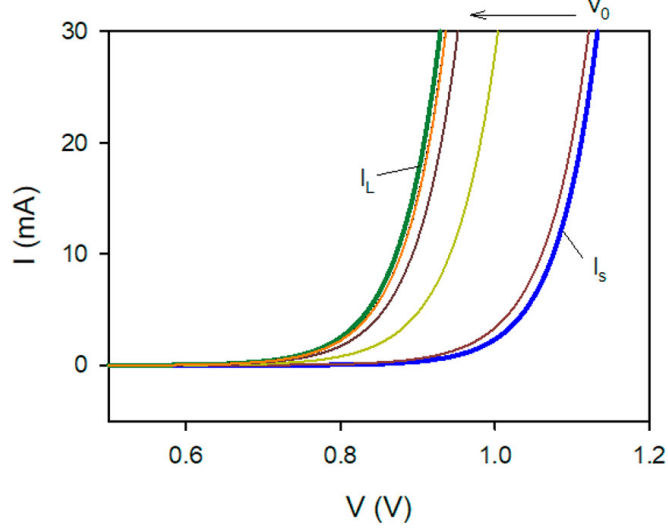


Figure 5.14: Stationary curve (eq 5.39) and $I - V$ curves (eq 5.45) at different forward scan rates starting at $I(0) = 0$ for the capacitive circuit with parameters $R_{10} = 49 \times 10^5 \Omega$, $R_{10} = 1 \times 10^5 \Omega$, $r_1 = 50$, $\tau_1 = 1$ s, $C_{10} = 10^{-5}$ F, $k_B T = 0.026$ V, $m = 2$, $V_m = 0.052$ V, $V_s = \tau_1 v_0$ for $v_0 = 10^1, 10^{1.5}, 10^2, 10^{2.5}$ V/s.

5.4.6 Integration of the Conductance Equation: General Solution for the Current in a Forward Scan

We now proceed to the integration of eq 5.33 in the form of

$$dI = \frac{1}{R_3(V)} (dV - dw_p) \quad (5.40)$$

For the general case of an arbitrary sweep rate parameter V_s , we obtain the differential dw_p in eq 5.40 from the second equation in our system, eq 5.36, resulting in

$$dw_p = \frac{r_0}{V_s} V dV - \frac{r_1}{V_s} w_p(V) dV \quad (5.41)$$

Inserting 41 into 40, we arrive at the equation

$$dI = \frac{1}{R_3(V)} dV - \frac{r_0}{R_3(V)V_s} V dV + \frac{r_1}{R_3(V)V_s} w_p(V) dV \quad (5.42)$$

Note that $w_p(V)$ is the state variable previously integrated in eq 5.37. Substituting it into eq 5.42 and with some algebraic manipulations, we obtain

$$dI = \frac{1}{R_1(V) + R_3(V)} dV + \frac{1}{R_3(V)} \left(\frac{r_0}{r_1} - \frac{r_0}{V_s} V_0 + \frac{r_1 w_{p0}}{V_s} \right) e^{V/V_m - r_1/V_s(V-V_0)} dV \quad (5.43)$$

The first term on the right-hand side is the stationary curve in eq 5.38, with the integrated form given by eq 5.39 as $I_s(V)$. The second term in eq 5.43 is the

current associated with the memory effect, $\Delta I(V_s, V)$. We, then, obtain

$$\Delta I(V_s, V) = \frac{1}{R_{30}} \frac{V_s}{V_s/V_m - r_1} \left(\frac{r_0}{r_1} - \frac{r_0}{V_s} V_0 + \frac{r_1 w_{p0}}{V_s} \right) (e^{V/V_m - r_1/V_s(V-V_0)} - e^{V_0/V_m}) \quad (5.44)$$

The total current obtained by integration of eq 5.33 is the final solution to the integration method

$$I(V) = I_s(V) + \Delta I(V_s, V) \quad (5.45)$$

The current at very large scan rate is

$$I_L = I_0 + \frac{1}{R_{30}} (e^{V/V_m} - e^{V/V_0}) \quad (5.46)$$

The large scan rate current I_L is shown by the green trace in Fig. 5.14. The calculated currents for different scan rates obtained by eq 5.45 are also presented in Fig. 5.14. The excess current ΔI is positive in all cases; hence, the voltage at a reference current decreases as the scan rate increases. The current changes between the limits I_S and I_L .

5.4.7 Interpretation of Forward Current in the Capacitive Circuit Model

The simple capacitive circuit explains the regular hysteresis in Figure 1a. Based on the solution of the problem, we can appreciate the general mechanism of hysteresis. At steady state, the effective resistance is $R_1 + R_3$, as indicated in eq 5.38, that describes the instantaneous ohmic behavior. However, if the system responds slowly to the external perturbation, \tilde{u}_p remains small and $\tilde{I} \sim \tilde{V}/R_3$ in eq 5.33. This is because the capacitor is shorted at high frequency. Then the resistance is smaller, and the total resistive pathway contains only a fraction of R_1 in addition to R_3 . The current is higher than at very slow scan rate. This higher current is capacitive, as demonstrated in measurements [70, 71].

Fig. 5.15 shows the evolution of voltage with sweep rate in two cases of the capacitive circuit with the same DC resistance defined by $R_{DC0} = R_{10} + R_{30}$. The voltage in equilibrium (slow scan rate) is the same in the two cases as they have the same total resistance. However, the voltage at $I = 20$ mA for higher scan rates is lower for the system with larger R_1 . Therefore, the quotient of resistances R_1/R_3 is the main factor controlling the amount of regular hysteresis.

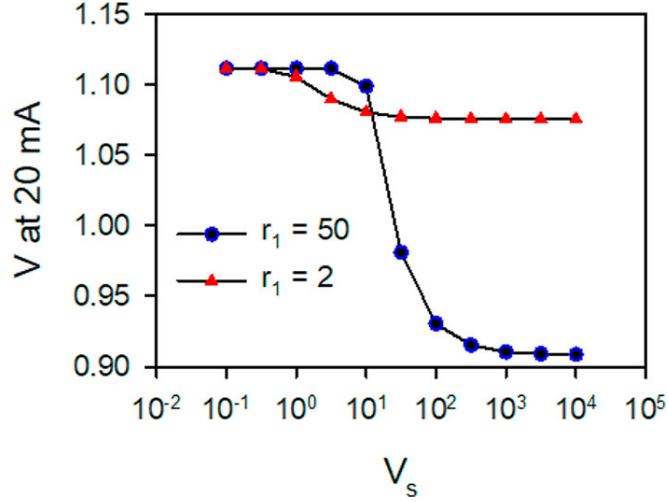


Figure 5.15: Forward scan rate dependence ($V_s = \tau_1 v_0$; $\tau_1 = 1$ s) of the voltage at $I = 20$ mA for two cases of the capacitive circuit with the same DC resistance $R_{DC0} = R_{10} + R_{30} = 10^6 \Omega$.

The onset of hysteresis as the scan rate increases occurs when the exponent in ΔI becomes positive, which is given by the condition

$$V_s > r_1 V_m \quad (5.47)$$

It can also be written in the form

$$v_0 > \left(\frac{1}{R_1} + \frac{1}{R_3} \right) \frac{1}{C_1} V_m \quad (5.48)$$

A large capacitance determines that the onset of hysteresis occurs at a low scan rate.

5.5 Inductive Circuit Model

We apply the method of integration to the inductive circuit of Fig. 5.7, according to the scheme illustrated in Fig. 5.16.

We obtain the equations

$$\tilde{I} = sC_g \tilde{V} + \frac{1}{R_3(\tilde{V})} \tilde{V} + \frac{1}{R_a(\tilde{V})} (\tilde{V} - \tilde{w}_2) \quad (5.49)$$

$$\frac{1}{R_a(\tilde{V})} (\tilde{V} - \tilde{w}_2) = \frac{1}{sL_a(\tilde{V})} \tilde{w}_2 \quad (5.50)$$

This result is not what we expected because the s in the second equation is in the denominator and will not produce a derivative term. However, since

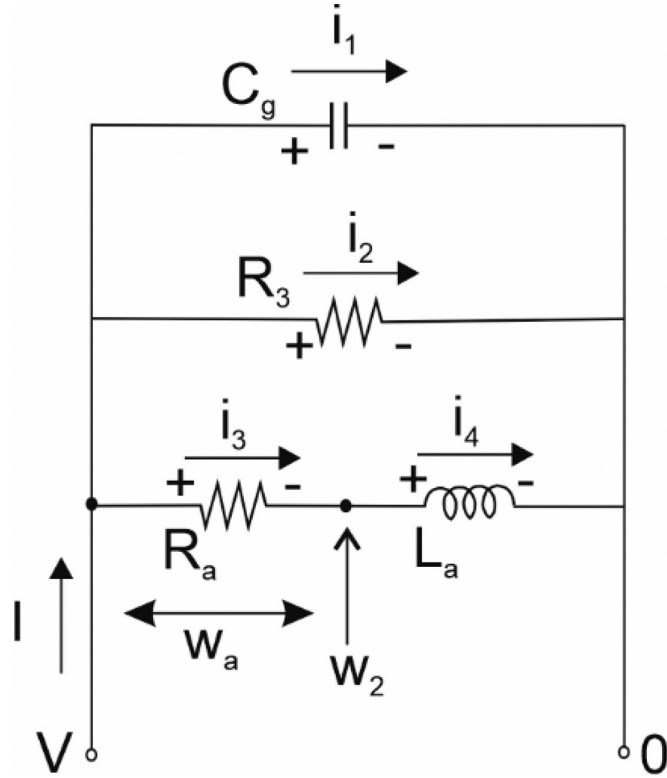


Figure 5.16: Application of node voltage method to solve the inductive circuit of Fig. 5.7.

the equations are linear, we are free to produce linear combinations of the state variables. In this case, we choose the transformation

$$\tilde{w}_a = \tilde{V} - \tilde{w}_2 \quad (5.51)$$

Neglecting again the relaxation process associated with $R_3 C_g$, we obtain

$$\tilde{I} = \frac{1}{R_3(\tilde{V})} \tilde{V} + \frac{1}{R_a(\tilde{V})} \tilde{w}_a \quad (5.52)$$

$$s \frac{L_a(\tilde{V})}{R_a(\tilde{V})} \tilde{w}_a = \tilde{V} - \tilde{w}_a \quad (5.53)$$

This last equation has the required form indicating that the physically meaningful state variable is the voltage \tilde{w}_a in the resistor R_a instead of the voltage in the inductor \tilde{w}_2 . We can express eq 5.53 in the time domain as

$$\tau_k \frac{d\tilde{w}_a}{dt} = \tilde{V} - \tilde{w}_a \quad (5.54)$$

where the kinetic constant is

$$\tau_k = \frac{L_a(\tilde{V})}{R_a(\tilde{V})} \quad (5.55)$$

This is the characteristic time of the inductive loop as shown in Fig. 5.7. In order to enable a relatively compact solution, we again assume that the voltage dependence of the EC elements is correlated with the same ideality factor V_m

$$R_3(V) = R_{30}e^{-V/V_m} \quad (5.56)$$

$$R_a(V) = R_{a0}e^{-V/V_m} \quad (5.57)$$

$$L_a(V) = L_{a0}e^{-V/V_m} \quad (5.58)$$

It follows that τ_k in eq 5.55 is a constant. In a steady-state situation, we obtain from eq 5.54

$$\tilde{w}_a = \tilde{V} \quad (5.59)$$

Therefore,

$$\tilde{I} = \left(\frac{1}{R_3(\tilde{V})} + \frac{1}{R_a(\tilde{V})} \right) \tilde{V} \quad (5.60)$$

Correspondingly,

$$dI = \frac{1}{R_{DC0}} e^{V/V_m} dV \quad (5.61)$$

where

$$\frac{1}{R_{DC0}} = \frac{1}{R_{30}} + \frac{1}{R_{a0}} \quad (5.62)$$

The stationary current is then

$$I_s = I_0 + \frac{V_m}{R_{DC0}} (e^{V/V_m} - e^{V_0/V_m}) \quad (5.63)$$

We focus our attention on the technique of CV. Defining

$$V_s = \tau_k v_0 \quad (5.64)$$

Equation 5.54 turns into

$$V_s \frac{d\tilde{w}_a}{dV} = \tilde{V} - \tilde{w}_p \quad (5.65)$$

By integration of this last equation, we find the evolution of the memory variable

$$w_a(V) = V - V_s + (w_{a0} - V_0 + V_s)e^{(V_0-V)/V_s} \quad (5.66)$$

Now we aim to integrate eq 5.52

$$dI = \frac{1}{R_3(V)} dV + \frac{1}{R_a(V)} dw_a \quad (5.67)$$

We use eq 5.54 as follows

$$dw_a = \frac{1}{V} (V - w_a) dV \quad (5.68)$$

Substituting into eq 5.67

$$dI = \frac{1}{R_3(V)} dV + \frac{1}{R_a(V)} dV - \frac{1}{V_s R_a(V)} [V - V_s + (w_{a0} - V_0 + V_s) e^{(V_0 - V)/V_s}] dV \quad (5.69)$$

The total current is

$$I(V) = I_s(V) + \Delta I(V_s, V) \quad (5.70)$$

where

$$\Delta I = -\frac{V_s + w_{a0} - V_0}{R_{a0}} \frac{1}{V_s/V_m - 1} (e^{V_0/V_s + (1/V_m - 1/V_s)V} - e^{V_0/V_m}) \quad (5.71)$$

The current at very large scan rate is

$$I_L = \frac{V_m}{R_{30}} (e^{V/V_m} - 1) \quad (5.72)$$

The $I-V$ curves at varying forward scan rates with I_S and I_L for the inductive circuit are shown in Fig. 5.17. The onset of hysteresis as the scan rate increases occurs when the exponent in ΔI becomes positive, which is given by the condition

$$V_s > V_m \quad (5.73)$$

It can also be written in the form

$$v_0 = \frac{V_m}{\tau_k} \quad (5.74)$$

When hysteresis is significant at high scan rate, the current ΔI in this model is negative. Therefore, the inductor branch explains the inverted hysteresis, which gives a sound ground to the observations in ref [75]. Consistently, the current moves between two limiting curves, from I_S toward I_L , at large sweep rates. At high frequencies, the inductor branch is an open circuit, and the current at high scan rate is determined by R_3 . At low scan rates, the inductor branch becomes active and the current is reduced by the parallel pathway R_a . The extent of hysteresis depends again on the relative size of resistances R_a/R_3 , as shown in Fig. 5.18, for two cells with the same DC characteristics. Moreover, the integration of the IS EC model to predict the evolution of the $I-V$ curves can also be implemented for reverse scan direction and under polarization effects (see the Supporting Information).

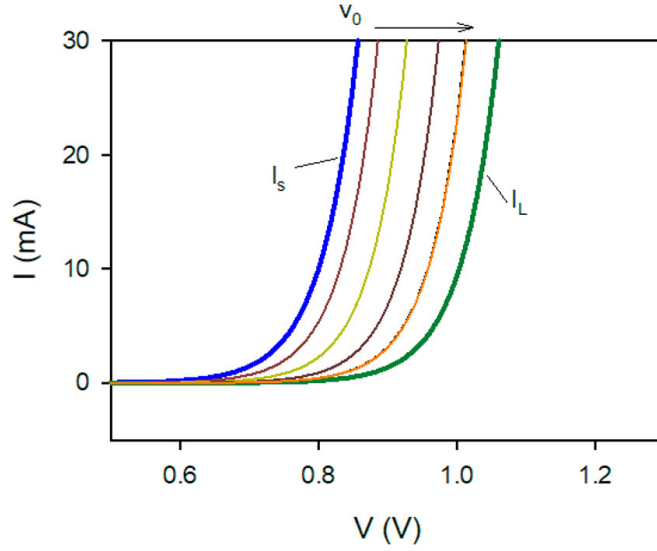


Figure 5.17: Stationary curve (eq 5.63) and $I - V$ curves (eq 5.70) at different forward scan rates starting at $I(0) = 0$ and $w_a = 0$ for the inductive circuit with the parameters $R_{DC0} = 2.5 \times 10^4 \Omega$, $R_{10} = 50/49 R_{DC0}$, $R_{30} = 50 R_{DC0}$, $\tau_k = 11$ s, $k_B T = 0.026$ V, $m = 2$, $V_m = 0.052$ V, $V_s = \tau_k v_0$ for $v_0 = 10^1, 10^{1.5}, 10^2, 10^{2.5}$ V/s.

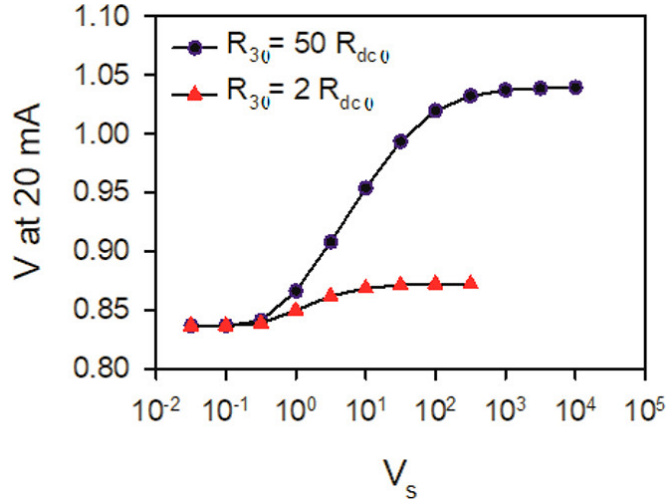


Figure 5.18: Forward scan rate dependence ($V_s = \tau_k v_0$; $\tau_k = 1$ s) of the voltage at $I = 20$ mA for two cases of the inductive circuit with the same DC resistance $R_{DC0} = 2.5 \times 10^4 \Omega$

5.6 Discussion

We have shown the transformation of the IS data to predict the evolution of $I - V$ curves at different voltage sweep rates, revealing the origin of the hysteresis in certain capacitive and inductive elements in the EC. We have illustrated the

method of integration using two elementary circuits that describe both types of hysteresis, regular and inverted, according to the time delay introduced by capacitive or inductive elements, respectively.

The method of integration is completely general. On the other hand, the specific models that we have solved are rather simple, e.g., by the assumption that all the elements have the same voltage dependence represented by the respective diode ideality factor m . Due to these simplifying assumptions, the models have been solved analytically and they provide certain conclusions regarding the kinetic constraints of hysteresis.

5.6.1 Conditions for Onset of Hysteresis

If an ac EC is made up of resistances only, the response to a voltage perturbation is immediate and there is no possible hysteresis. Delays are introduced by kinetic processes represented by capacitors and inductors. One can also associate certain time constants to the capacitive or inductive combination with resistors. Then, one finds that assessing the hysteresis entails a comparison of a voltage sweep rate, v_0 [V/s], and some characteristic time, τ [s]. However, these magnitudes have different units. How can they be compared? Our analysis shows that the diode quality factor represented in voltage units by V_m is the essential quantity that enables the transformation from a voltage sweep rate to a pure time constant. Our study with a constant V_m has provided clear criteria, involving a factor that compares the resistances in the system, for the presence of hysteresis: eq 5.48 for the capacitive circuit mode and eq 5.74 for the inductive circuit model.

5.6.2 Representative Experimental Behaviors

We are next set to illustrate some representative behaviors that have been observed in our research laboratories using different perovskite formulations. Fig. 5.19 shows a catalogue of responses for different types of perovskite solar cells. We represent the observed hysteresis traces and the associated impedance responses at different voltages, separated by capacitive and inductive effect according to the above classification.

The general partition of types of hysteresis is well-supported by the IS data.

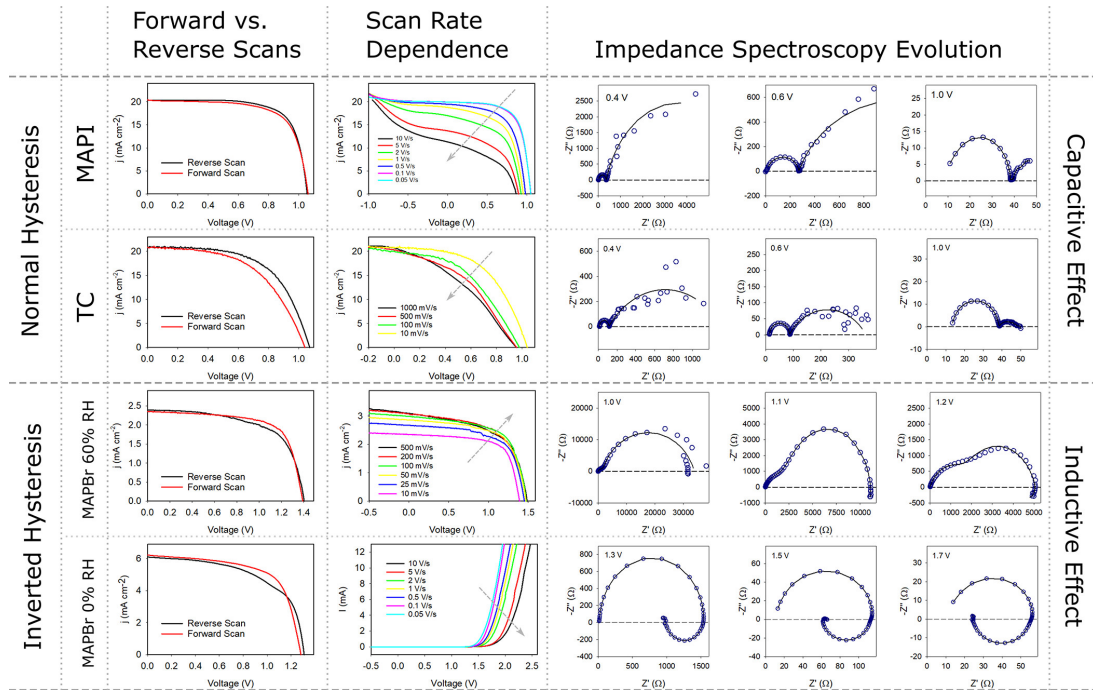


Figure 5.19: Catalogue of measured electrical response observed in our laboratories as a function of the perovskite formulation and measurement conditions. Normal hysteresis with capacitive response: MAPI and triple cation (TC) formulations. Inverted hysteresis with inductive response: MAPBr measured at RH = 60% [75] or in inert atmosphere (RH = 0%).

First of all, we have consistently observed normal hysteresis for devices measured under illumination conditions for compositions containing methylammonium lead iodide (MAPI) in the standard n-i-p structure or triple cation (TC, $\text{FA}_{0.85}\text{MA}_{0.15}\text{Pb}(\text{I}_{0.85}\text{Br}_{0.15})_3$). The normal hysteresis is clearly observed in the $J - V$ response as a function of the scan rate in which the V_{OC} of the devices decreases with an increase in the scan rate during the forward scan. In agreement with the integration theory, the impedance spectra of these devices clearly show a capacitive response at low frequencies at different applied dc voltages.

Alternatively, a perovskite composition based on the methylammonium lead bromide (MAPBr) has been reported to show inverted hysteresis when the device is exposed to high relative humidity (RH = 60%) [75, 78]. The $J - V$ response as a function of the scan rate clearly shows that the V_{OC} increases with the increase in the scan rate during forward scan. Impedance spectra measured in the dark in the range of 1.1 - 1.5 V show the appearance of the inductive effect which is responsible for the inverted hysteresis. We note that this inductive effect is not

fully developed even at frequencies as low as 0.065 Hz for the reasons discussed below.

To further study this system, here we prepared fresh MAPBr cells following the method of ref [78]. In this work, the MAPBr formulation has not been exposed to humid air, and devices are measured in inert atmosphere (RH = 0%). Interestingly, the $J-V$ curves measured in the dark also show inverted hysteresis as a function of the scan rates. In agreement with this result, the impedance spectra show an inductive arc which is fully developed touching the real Z axis at low frequency. As it can be observed, hysteresis and impedance response are consistent with the methodology presented in this article.

5.6.3 Voltage Dependence of Resistances

The experimental data from samples described in Fig. 5.19 are fitted to the ECs in Figures 4 and 7, depending on the capacitive or inductive characteristic of the spectrum. All impedance parameters are reported in the Supporting Information. The fitted parameters as a function of voltage are shown in Fig. 5.20. We note that, in contrast to the naïve models described in sections 4 and 5, the variable resistances are not exponential for most samples and they have different curvatures. In addition, we also observe some crossing of resistances R_3 with R_1 and R_a for MAPI and MAPBr, respectively.

The lack of voltage-dependent linear response of resistances in the semilog plot is related to the question of the diode quality factor in PSCs that has been amply discussed in the literature. In principle, with ideal contacts and well-defined recombination mechanism, one can obtain a single constant m value [42]. In fact, when the measurements are carried out at variable illumination and V_{OC} conditions, resistances in PSC show a well-behaved exponential variation, as shown in Fig. 5.3. The constant ideality factor in terms of voltage, V_m , over extended voltage ranges, often reported in the literature, has been typically obtained by measurement of different points at open-circuit potential [42, 46, 51, 79, 80]. However, the recombination mechanisms are often not ideal [81], and the continuous application of an external voltage may induce chemical and structural changes in the perovskite composition. It is well-known that tracking the dark $J-V$ curve produces a strongly voltage-dependent ideality

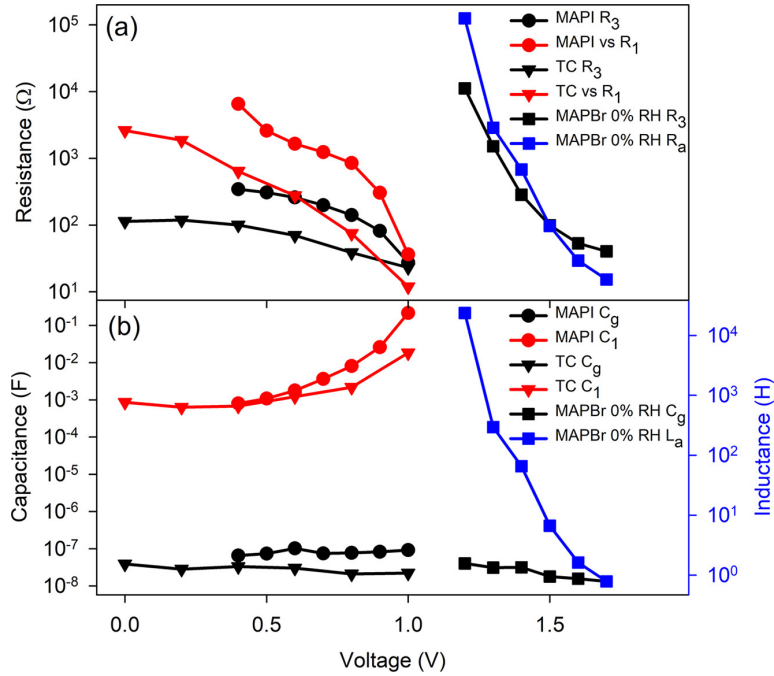


Figure 5.20: Summary of fitted (a) resistances, (b) capacitances and inductor of the ECs of Figures 4 and 7, extracted from the IS data of samples shown in Fig. 5.19, represented as a function of the applied DC voltages.

factor [80, 82, 83]. Therefore, the simple models that have been adopted to illustrate integration theory cannot directly be translated to the interpretation of measurements. Nevertheless, we can infer some conclusions from the previous results. It was shown that the $J - V$ curve changes between two limits, from very slow to very fast scan rate (Figs. 5.14 and 5.17). Each limit curve corresponds to a specific combination of resistances: a capacitor shorts the parallel resistance at high frequency, while the inductor activates its series resistance at low frequency. Correspondingly, in general, the diode exponent m is a variable element depending on scan rate: it will be determined by a certain combination of resistances at low frequency and a different combination at high frequency. If the resistances have different exponential dependences with respect to voltage, then the actual ideality factor of the $J - V$ curve will be variable with voltage, as observed experimentally [83]. A preliminary model with the different exponents for slow and fast modes of the resistance was shown in ref [64].

5.6.4 Kinetic Time Constants

Using the results of the fitting, it is possible to calculate the response time for the slow capacitive relaxation phenomenon (τ_1) and the kinetic constant that leads to the inductive effect (τ_k). As can be observed in Fig. 5.21, the response is highly dependent on the perovskite composition, with longer times (associated with lower frequency response) for MAPI ($\tau_1 \sim 5 - 10$ s) compared to those with the TC formulation ($\tau_1 \sim 0.1 - 1$ s). Similarly, the effect of ambient water on the kinetics of the inductive response is remarkable. In the case of MAPbBr₃ measured at RH = 60%, the inductive arc is only incipient with the lowest frequency data point measured that corresponds to a frequency $\omega = 0.41$ rad/s, with a corresponding τ_k longer than 2.4 s. This is consistent with the first reported determinations of τ_k between 20 and 30 s [63]. As the arc does not close due to the experimental limitations (long measurement time), it will not be possible to obtain reliable extracted values for Ra and La, due to the fact that τ_k is at the edge of the measuring window of frequencies, as shown in Fig. 5.21. Alternatively, for MAPbBr measured in a glovebox (RH = 0%), the time response of the inductive phenomenon is fast, with values in the range of $\tau_k \sim 0.01 - 0.1$ s. This fast response makes it possible to observe a fully developed inductive arc that closes within the measurement time: the typical range of measurement can capture it, and the good stability of the cell avoids interference of noise [84].

5.6.5 Transformation of the Equivalent Circuit along the Variation of Voltage

Finally, we comment on a peculiar behavior of PSCs that consists on the change of the equivalent circuit, from capacitive to inductive, as the dc voltage is varied. This transformation leads to a change of the hysteresis response in a single $J - V$ curve, as predicted by the integration theory. This transformation has been observed in the impedance response of memristors, as shown in Fig. 5.6 [53]. Here, we report the impact on the shape of the $J - V$ curve. Indeed, PSCs containing MAPBr measured in the dark and in the absence of ambient humidity (RH = 0%) show this mixed behavior, as shown in Fig. 5.22. The same $J - V$

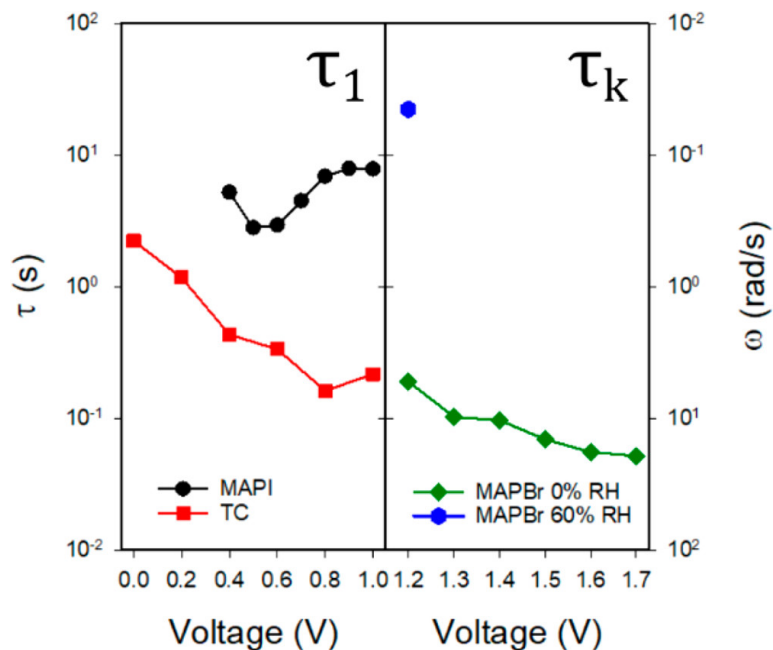


Figure 5.21: Response time for the slow capacitive relaxation phenomenon (τ_1) and the kinetic constant that leads to the inductive effect (τ_k) calculated from the fitted IS parameters obtained from the samples in Fig. 5.19.

curve described in Fig. 5.19 is replotted using a semilog scale, and we observe that the scans at different scan rates have a crossing point at approximately 1.2 V. At high voltages, the inverted hysteresis is observed as previously mentioned. In contrast, the baseline current at 0 V changes more than 1 order of magnitude with a capacitive response in this voltage range, in which the current increases with scan rate as expected in the elementary models of capacitive current [72]. Regarding the impedance spectroscopy data, in the capacitive regime at lower applied voltages, the spectra show the typical two arcs, and we can use the EC in Fig. 5.4 to fit the data. On the other hand, the EC of Fig. 5.7 fits the data at voltages above 1.2 V. In this voltage range, very well developed inductive arcs are observed. Indeed, the low-frequency arc and the inductive loop seem to be highly connected: as one decreases its magnitude as the other increases the weight in the response, as previously noted in Fig. 5.6.

5.6.6 General Remarks and Limitations of the Method

In general, the IS analysis of PSCs shows processes much more complex than those used in our reference simple models [85, 86]. The experimental quantity

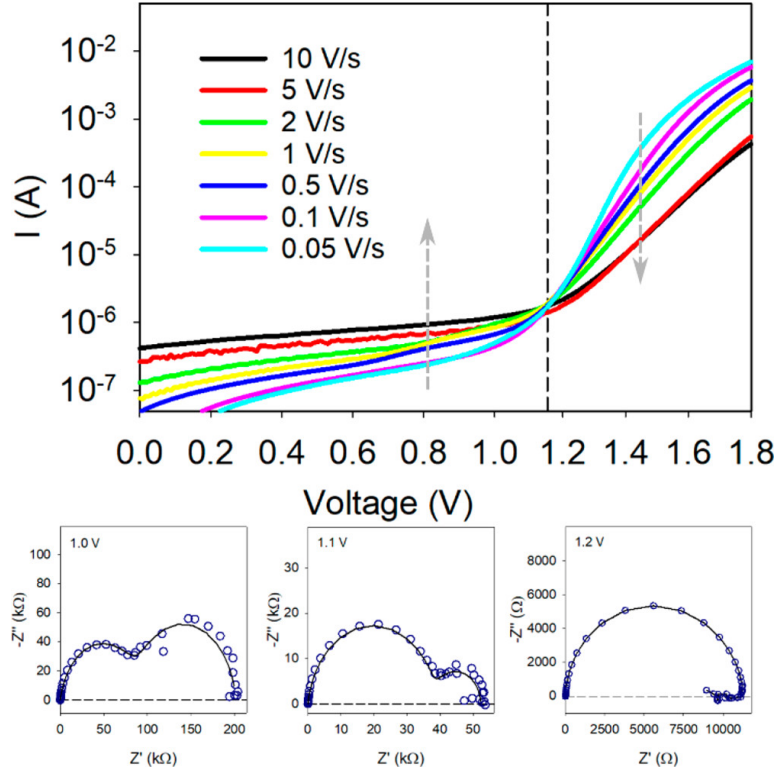


Figure 5.22: Forward scan $J - V$ curves measured in the dark and at different rates for a MAPBr solar cell (RH = 0%) and impedance response at voltages below the crossing point.

is the whole $Z(\omega)$ function while the decomposition into EC elements is a judgment of the experimenter. The resolution of the time domain processes in our integration method depends on the separation of the processes in the frequency domain. Integration over a wide voltage range using the relevant EC elements is necessary. Therefore, the description of experimental data will require the following:

- i. A sound EC that describes well the IS data over the voltage range of interest
- ii. A numerical integration method to turn the differential equations into a time domain response

We have emphasized the importance of the impedance spectroscopy analysis. We must not forget, however, that impedance $Z(\omega)$ is a two-port measurement and contains limited information about internal processes. One cannot expect a full picture of the internal variations. The complementary information should be

attempted by combining other techniques [87]. It is well-established that dark- and light-induced processes provoke very different variations and conditions. The modifications of currents may be investigated by complementary light-modulated techniques [88].

It is also important to note that if the current under an applied voltage scheme realizes a large excursion away from the steady-state line, the time- or voltage-dependent current data may not be well-obtained by integration of the linear impedance data as there are visited regions that lie far away from the steady-state $J - V$ curve. This is the case for a large reverse polarization [89] that introduces distinct phenomena such as holes tunneling into the perovskite due to sharp band bending near the contact [90].

5.7 Conclusion

Over the years, many regular properties of perovskite solar cells have emerged, and several phenomena have been consolidated and understood. However, an important uncertainty is how to deal with hysteresis that is deleterious for solar cells and, in practice, is often eliminated by trial and error. On the other hand, memristors show a magnified hysteresis effect that can be applied to resistive switching memories. Memristors have brought a new angle of analysis of hysteresis. They show a strong inverted hysteresis effect and indicate the pathway to relate hysteresis and impedance spectroscopy. We have built a method that, starting from IS data, is able to assess the amount of hysteresis that one may expect. The method works by turning the impedance spectroscopy model into a set of differential equations and integrating them for the required external voltage stimulus of the specific measurement technique. The system itself suggests the internal state variables, according to the complexity of the equivalent circuit: the number of internal variables corresponds to the number of internal nodes of the circuit. We solved two simple but relevant models. They show the physical reason for the dominant types of hysteresis reported in the literature: regular hysteresis is capacitive, whereas inverted hysteresis is inductive. Analysis of a variety of solar cells shows that the predicted properties are satisfied by the data. Moreover, we reported a system that undergoes transformation from capacitive

to inductive hysteresis in a single $J - V$, governed by an equivalent circuit that undergoes transformation at a certain voltage. An analysis of more complex experimental data requires sophisticated methods involving the determination of the equivalent circuit by experimental analysis and the numerical integration of the differential equations.

5.8 Supporting Information

Different polarization schedules

To analyze the hysteresis in CV in the reverse direction for the capacitive circuit we first choose a point at voltage V_1 in the stationary curve that starts at $I(0) = 0$. It has the values

$$I_1 = V_m / (R_{10} + R_{30})(e^{V_1/V_m} - 1) \quad (5.75)$$

$$w_{p1} = \frac{r_0}{r_1} V_1 \quad (5.76)$$

We use this point as the initial condition. We wish to apply a negative sweep velocity (from forward voltage to reverse voltage) that we write as $B_s = -V_s$. We obtain

$$w_p(V, V_1, B_s) = -\frac{r_0}{r_1^2} B_s e^{r_1/B_s(V-V_1)} + \frac{r_0}{r_1} V + \frac{r_0 B_s}{r_1^2} \quad (5.77)$$

with the current given by

$$I(V, V_1, B_s) = \frac{V_m}{R_{10} + R_{30}} (e^{V/V_m} - 1) + \frac{1}{R_{30}} \frac{r_0}{r_1} \frac{B_s}{B_s/V_m + 1} (e^{V/V_m + r_1/B_s(V-V_1)} - e^{V_1/V_m}) \quad (5.78)$$

The reverse scans at progressively large negative velocities (forward voltage to reverse voltage) are shown in Fig. 5.23. The current at the origin is given by the expression

$$I(0, V_1, B_s) = -\frac{1}{R_{30}} \frac{r_0}{r_1} \frac{B_s}{B_s/V_m + 1} (e^{V_1/V_m} - e^{-r_1 V_1/B_s}) \quad (5.79)$$

In the inductive circuit in the reverse direction for the capacitive circuit the point at voltage V_1 in the stationary curve that starts at $I(0) = 0$ gives

$$I_1 = \frac{V_m}{R_{DC0}} (e^{V_1/V_m} - 1) \quad (5.80)$$

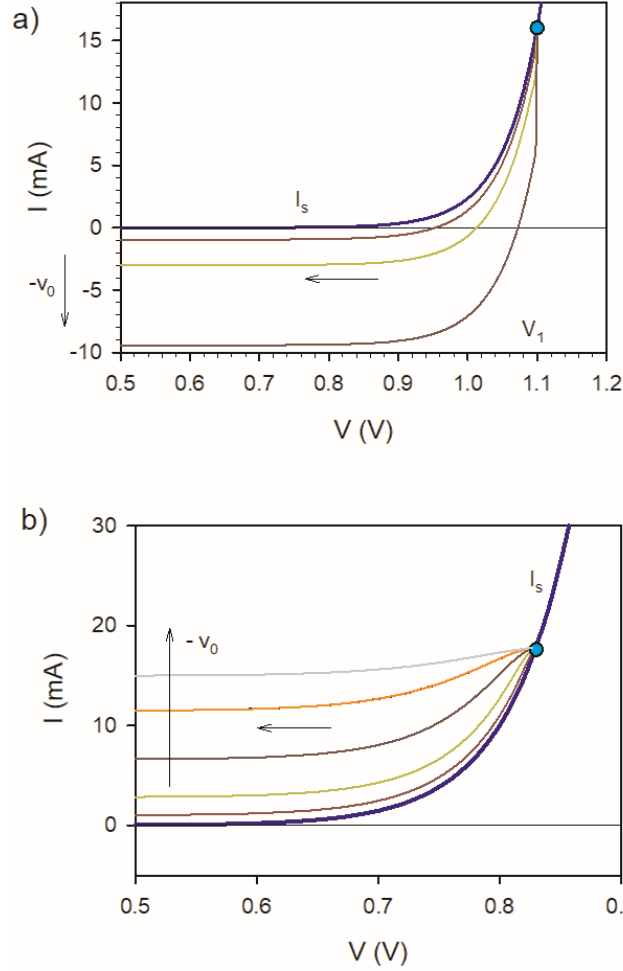


Figure 5.23: (a) Current-voltage curves at different reverse scan rates, Eq. (5), for the capacitive circuit with parameters $R_{10} = 1 \times 10^5 \Omega$, $R_{30} = 49 \times 10^5 \Omega$, $r_1 = 50$, $\tau_1 = 1$ s, $C_1 = 10^{-5}$ F, $k_B T = 0.026$ V, $m = 2$, $V_m = 0.052$ V, and the stationary curve. The reverse scan starts at the equilibrium curve at voltage $V_1 = 1.1$ V, indicated by a point. The sweep velocities $V_s = \tau_1 v_0$, are $-v_0 = 10^{-2.5}, 10^{-2}, 10^{-1.5}$ V/s. (b) Current-voltage curves at different reverse scan rates for the inductive circuit with parameters $R_{DC0} = 2.5 \times 10^4 \Omega$, $R_{10} = 50/49 R_{DC0}$, $R_{30} = 50 R_{DC0}$, $\tau_k = 1$ s, $k_B T = 0.026$ V, $m = 2$, $V_m = 0.052$ V, and the stationary curve. The reverse scan starts at the equilibrium curve at voltage $V_1 = 0.83$ V, indicated by a point. The sweep velocities $V_s = \tau_1 v_0$, are $v_0 = 10^{-2.5}, 10^{-2}, 10^{-1.5}, 10^{-1}, 10^{-0.5}$ V/s.

In the memory value we allow for a voltage ΔV_1 in excess of the equilibrium value

$$w_{a1} = V_1 + \Delta V_1 \quad (5.81)$$

We now take V_1 as the initial condition. We apply a negative sweep velocity $B_s = -V_s$. We obtain

$$w_p(V, V_1, B_s) = V + \Delta V_1 - B_s [e^{V-V_1/B_s} - 1] \quad (5.82)$$

with the current given By

$$I(V, V_1, B_s) = \frac{V_m}{R_{DC0}} (e^{V/V_m} - 1) + \frac{1}{R_{a0}} \frac{B_s - \Delta V_1}{B_s/V_m + 1} (e^{V/V_m} - e^{V/V_m + (V+V_1)/B_s}) \quad (5.83)$$

The reverse scans are shown in Fig. 5.23b. The current at the origin has the value

$$I(0, V_1, B_s) = \frac{1}{R_{a0}} \frac{B_s}{B_s/V_m + 1} (e^{V_1/V_m} - e^{-V_1/B_s}) \quad (5.84)$$

Besides the change of the $J - V$ curves by the sweep rate, another important hysteretic effect is the modification of $J - V$ curves by voltage or light pretreatment that induce polarization. Effects of poling are well known and can increase the performance of the solar cell, or reduce it by the artefact of the depolarization currents [91–94]. To describe these situations we start the forward evolution with initial value w_{a0} in the model for the inductive circuit, eq. 66. It produces an increase of the negative current discharge as shown in Fig. 5.24a. In the current-voltage curve under illumination this effect produces the overshoot of the $J - V$ curve under illumination. The effect of prepolarization of the memory variable by an amount ΔV_1 in excess of the equilibrium value, in reverse scan from a voltage V_1 , is shown in Fig. 5.24b. These effects have been discussed previously [17, 23, 64].

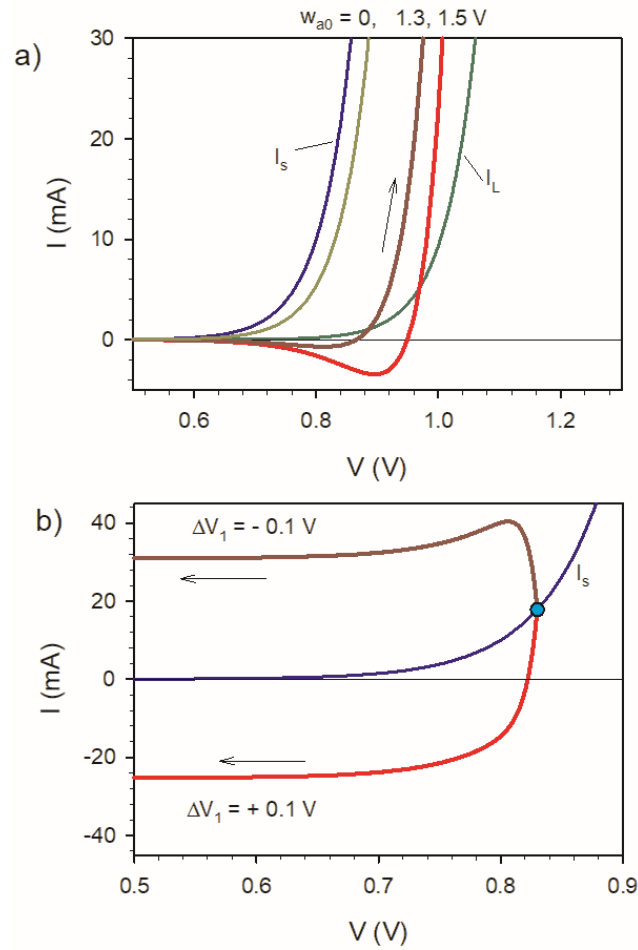


Figure 5.24: Prepolarization of the inductive circuit. (a) Current-voltage curves at forward scan at different w_{a0} values for the parameters $R_{DC0} = 2.5 \times 10^4 \Omega$, $R_{10} = 50/49R_{DC0}$, $R_{30} = 50R_{DC0}$, $\tau_k = 1$ s, $k_B T = 0.026$ V, $m = 2$, $V_m = 0.052$ V, $V_s = 1$ V/s. (b) Reverse scan at velocity $B_s = 0.01$ V/s starting at $V_1 = 0.83$ V (point) at positive and negative polarization.

IS Fit Parameters

The fitted IS parameters for all samples are summarized in Tables 5.1 and 5.2.

Capacitive Circuit

Table 5.1: IS fit parameters using the capacitive equivalent circuit model for the MAPI and Triple Cation samples, with effective areas of 0.12 cm² and 0.295 cm², respectively measured under illuminated conditions.

Sample	Voltage (V)	R_3 ($\Omega\cdot\text{cm}^2$)	C_g ($\text{F}\cdot\text{cm}^{-2}$)	R_1 ($\Omega\cdot\text{cm}^2$)	C_1 ($\text{F}\cdot\text{cm}^{-2}$)
MAPI (Illuminated)	0.4	41.292	5.47×10^{-7}	784.8	0.006625
	0.5	36.984	6.17×10^{-7}	311.52	0.009
	0.6	31.116	8.53×10^{-7}	198	0.01475
	0.7	23.784	6.22×10^{-7}	148.8	0.03008
	0.8	16.968	6.45×10^{-7}	102.012	0.067417
	0.9	9.8028	6.89×10^{-7}	36.576	0.21583
	1	3.3036	7.66×10^{-7}	4.3668	1.79325
TC (Illuminated)	0	33.4825	1.32×10^{-7}	769.95	0.000854
	0.2	35.046	9.64×10^{-8}	549.29	0.00063
	0.4	29.5295	1.13×10^{-7}	188.859	0.000674
	0.6	20.62345	1.02×10^{-7}	81.302	0.001215
	0.8	11.3988	7.14×10^{-8}	22.0306	0.002164
	1	6.8086	7.57×10^{-8}	3.5046	0.018233

Inductive Circuit

Table 5.2: IS fit parameters using the inductive equivalent circuit model for the MAPBr 0% RH sample, with an effective area of 0.237 cm², measured under dark conditions.

Sample	Voltage (V)	R_3 ($\Omega\cdot\text{cm}^2$)	C_g ($\text{F}\cdot\text{cm}^{-2}$)	R_1 ($\Omega\cdot\text{cm}^2$)	C_1 ($\text{F}\cdot\text{cm}^{-2}$)
MAPBr 0% RH (Dark)	1.2	2655.348	1.71×10^{-7}	29710.32	5629.461
	1.3	359.292	1.31×10^{-7}	681.849	69.915
	1.4	67.4502	1.34×10^{-7}	160.8756	15.54246
	1.5	23.50329	7.62×10^{-8}	22.95345	1.58458
	1.6	12.61077	6.64×10^{-8}	6.95595	0.38465
	1.7	9.59139	5.60×10^{-8}	3.62136	0.18677

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Chapter 6

Transition from Capacitive to Inductive Hysteresis: A Neuron-Style Model to Correlate $I - V$ Curves to Impedances of Metal Halide Perovskites

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Extent of Contribution : 60%

The following tasks/activities are the author's contribution to this work:

- Synthesis and fabrication of MAPbBr₃ solar cells
- Optoelectronic characterization of fabricated devices
- Analysis of characterization measurement data and results
- Model implementation and fitting of the impedance results
- Manuscript and response to reviewers' comments document preparation

Abstract

Metal halide perovskite (MHP) devices often show different types of hysteresis in separate voltage domains. At low voltage the impedance response is capacitive, and the cell gives regular hysteresis. At high voltage the hysteresis is inverted

corresponding to an inductive response that causes a negative capacitance feature. We calculate the hysteresis current due to a chemical inductor model, and we show that the current is inversely proportional to the voltage scan rate. We formulate a general dynamical model for the solar cell response in the style of neuronal models for the action potential, based on a few differential equations. The model allows to track the transition from capacitive to inductive properties, both by impedance spectroscopy, and current voltage measurements at different voltage sweep rates. We obtain a correlation of the time constants for the capacitor and the inductor. We interpret the origin of the low frequency features in terms of the ion-controlled surface recombination. This explains the strong correlation of the low frequency capacitance and inductor, as both originate from the same mechanism. The methodology derived in this paper provides great control over the dynamic properties of metal halide perovskite solar cells, even in cases in which there are qualitative changes of the solar cell current-voltage response over a broad voltage range.

6.1 Introduction

Metal halide perovskites (MHP) have established a new photovoltaic (PV) technology for large solar energy conversion efficiencies with low cost, solution processed materials [1–4]. The MHP can be described as ABX_3 where A = monovalent cations (i.e. methyl ammonium, MA; formamidinium, FA), B = divalent cations (i.e. Pb^{2+}) and X = halide anions (i.e. I^-). It is possible to use combinations of cations (MA, FA, Cs, and Rb) and anions (I, Br) to modify the band gap, efficiency and stability for different types of applications [5–8]. For example, $MAPbBr_3$ forms a semiconductor with a wide bandgap (2.3 eV) useful for tandem solar cell in combination with Si [9, 10]. In addition, the external interfaces play a very important role, and improvement of the charge extraction layers have enhanced the charge external collection and stability of the devices [11, 12].

MHP semiconductors show mixed ionic-electronic conduction in which a significant ionic conductivity exists in addition to the electronic photoconductivity [13–16]. These effects cause intrinsic memory effects (hysteresis) in current-

voltage ($I - V$) [17–26] that lead to substantial differences in the forward and reverse scan currents and permanent resistive changes. By different empirical methods, it has been possible to minimize hysteresis effects in perovskite solar cells [27–29]. However, hysteresis persists in recent high performance configurations, such as tandem solar cells [10, 30–32]. In addition, hysteresis and memory effects allow the storage of information by modification of device conductivity. This can be exploited in memristors [33–35] and artificial synapse devices [36, 37] in which MHPs are used for non-optoelectronic applications related to memory storage and neuromorphic computation [38–40].

Impedance Spectroscopy (IS) consists of the electrical measurement of the device at a steady state potential V by a small perturbation of current-to-voltage at varying angular frequency ω . It is a central technique for the characterization of PV cells and electrochemical devices [41, 42]. The knowledge about the system properties is represented by an equivalent circuit (EC), in which elements change according to the external conditions. Extensive studies of IS of MHP [43–49] have provided a basic picture of shape of spectra and EC models. These results show that the IS description of a MHP measured over a broad voltage range undergoes transformations in which some elements appear and dominate the impedance spectra while others lose relevance. There is a variety of reasons for this, such as that elements show an exponential dependence on bias voltage causing large changes of their values. Another one is that elements may be truly activated at some voltage, as observed in the onset of a large current in memristors [35, 50].

It has been remarked that hysteresis and impedance are closely related properties, since frequency and time domain response are intimately connected [25, 51]. However a quantitative analysis of this assertion in complex cases has not been presented before. This paper uses different tools that have been derived in recent years to provide a more complete methodology that addresses intricate changes of hysteresis and impedance response often found in perovskite solar cells. We aim to make a modelistic description of $I - V$ curves that change at different scan rates, compatible with the impedance spectroscopy properties.

There are different studies to this problem based on drift-diffusion simulations and related approaches [52–60]. Here we introduce a different complementary approach, in which the model is formed by a small number of equations, that

can describe consistently the different techniques: the $I - V$ curves at different scan rates, and other large perturbation methods such as the response to large voltage or illumination steps [61], in the one hand, and in the other hand the small perturbation measurements like IS, IMPS, IMVS [51]. Such a model provides an outstanding tool to correlate the different measurements, and to make predictions of solar cell characteristics based on a few fast measurement characterization.

In particular the model should have the following goal:

1. Explain the tendencies of hysteresis in current-voltage and the impedance spectroscopy with a single unified model that contains only a few number of parameters that account for the dominant properties of the device.
2. Identify and explain correlations of the impedance parameters.
3. Explain why the inductive behaviour (negative capacitance) appears at high voltage in halide perovskite solar cells.
4. Explain why it is observed in some cells and not in others.

We use as inspiration the models of neuron theory that describe extraordinarily complex phenomena including spiking, bifurcation and potentiation with just a few nonlinear differential equations (from two to four) [62–64]. Recently these models for the time domain responses have been put into correspondence with the impedance spectroscopy properties [65, 66]. The same methodology has been applied to halide perovskite memristors [50, 67].

Here we address the much broader problem of hysteresis and impedance properties of halide perovskite solar cells. We show general properties of the transformation of EC elements along the voltage changes in MHP solar cells. In order to summarize the available knowledge and tools we present in the next section a summary of the properties of hysteresis. Then we show the experimental results. Methylammonium lead bromide (MAPbBr_3) solar cells are selected as they present a manifest transformation from capacitive response at low voltage to a large inductor feature at high voltage [68].⁶⁹ The study in the dark conditions produces highly controlled conditions as compared to under illumination, which facilitates model validation. Furthermore, it avoids the photoinduced effects as the increased ionic conductivity and photo-degradation. Then, we build the

model to explain quantitatively the changing properties of hysteresis in relation with the variation of EC properties. We track the evolution of parameters and we find unexpected links between them. We provide a physical interpretation and finish with some conclusions.

6.2 Capacitive and Inductive Hysteresis in Halide Perovskites

6.2.1 Hysteresis and Stability

Hysteresis is obtained when measuring the current of the solar cell under a voltage sweep at a constant velocity. The $I - V$ curves become separated in the forward and reverse as shown in Fig. 6.1a,b. Hysteresis of current-voltage is a transient effect [17–24]. By waiting a sufficiently long time the current can be stabilized, and methods are proposed to establish the power conversion efficiency independent of hysteresis effects [69–72]. But in a reasonable dynamic measurement a divergence is often found between forward and reverse curves. It happens when the internal dynamic timescales of the device intersect the time duration of the measurement. Note that the forward photocurrent is smaller in the Fig. 6.1a than the reverse current (normal hysteresis) and conversely in the Fig. 6.1b (inverted hysteresis).

It is well known that one has to be cautious in MHP characterization. There are many types of transient phenomena in halide perovskites. These effects may be caused by the sample being away from equilibrium at the beginning of the measurement, or when a fresh sample is aiming at operation stability [73]. One example is the famous “pretreatment effect” in which one can produce favorable or deleterious effect according to initial biasing [74]. Pockett et al. showed that rapidly changing initial features of a carbon-based perovskite solar cell are captured consistently by TPV and IMVS techniques [75]. An example of a solar cell that is changing the characteristics by voltage cycling in the dark is shown in Fig. 6.1b, and under illumination in Fig. 6.1a and 6.1c. These properties haven been attributed to the slow ion transit effects that create uncompensated electrical fields or modify the interfaces by surface polarization effects [60, 76].

Fig. 6.1a shows a robust and reproducible solar cell where current-voltage

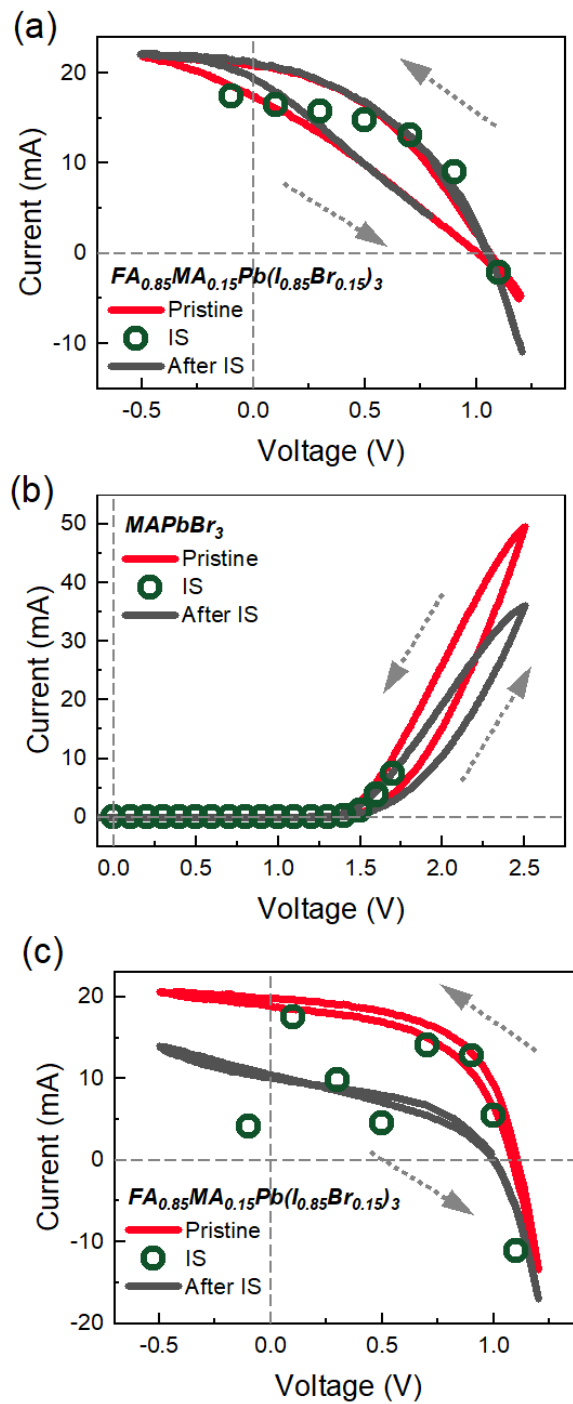


Figure 6.1: Representative $I - V$ response of halide perovskite solar cells measured at 50 mV/s, showing the pristine as-prepared device and after IS measurements. (a) Mixed halide perovskite solar cells under illumination. (b) $MAPbBr_3$ in the dark. (c) Mixed halide perovskite solar cells under illumination. The current extracted during the IS measurement is shown in circles to determine the correspondence of the electrical measurements $J - V$ and IS.

under voltage sweep and the current measured during IS measurement agree. In this paper we are interested in an initial situation that has been stabilized, so that the results of small or large perturbation measurements can be associated entirely to the applied signal and not to hidden memory effects or sample-drift effects. Based on this assumption, we can attribute an EC response to different equilibrated stages of the dynamics, and the full evolution in a voltage excursion can be reasonably treated by parameters that depend on the voltage.

6.2.2 Capacitive Hysteresis

The first well-identified hysteresis effect in halide perovskite was the description of capacitive current by Garcia-Belmonte and coworkers, see Fig. 6.2 that shows the results associated to the low frequency capacitance of halide perovskites [77]. Capacitive current effects are very common in electrochemical devices [78, 79]. Capacitive hysteresis for diodes in the dark occur with a forward current that is larger than the reverse current as shown in Fig. 6.2a,b. The capacitive current is proportional to the scan rate, Fig. 6.2c, and it changes sign when inverting the scan direction, producing the characteristic square shape of Fig. 6.2d. Capacitive hysteresis was often observed in other types of devices such as dye-sensitized solar cells [80].

Fig. 6.3 shows the correlation of the low frequency capacitance with the amount of hysteresis in MHP solar cells with different types of contacts [21]. The huge hysteresis response in Fig. 6.3a, is due to the large capacitive effect of TiO_2 contact, shown in Fig. 6.3d and e. In contrast, for the inverted structure the $I - V$ hysteresis and the equilibration time is decreased, Fig. 6.3b,c. In the $I - V$ illuminated characteristic of the solar cell in Fig. 6.3a, the increasing recombination current at large voltage turns more negative, hence in this representation capacitive hysteresis the forward current becomes smaller than the reverse current.

For the modeling of capacitive hysteresis we use the following equation,

$$I_{\text{tot}} = C_m \frac{dV}{dt} + I_b(V) \quad (6.1)$$

Here, I_{tot} is the total current, V is the voltage across the device, C_m is the capacitance and I_b is a conduction current that may have different types of values.

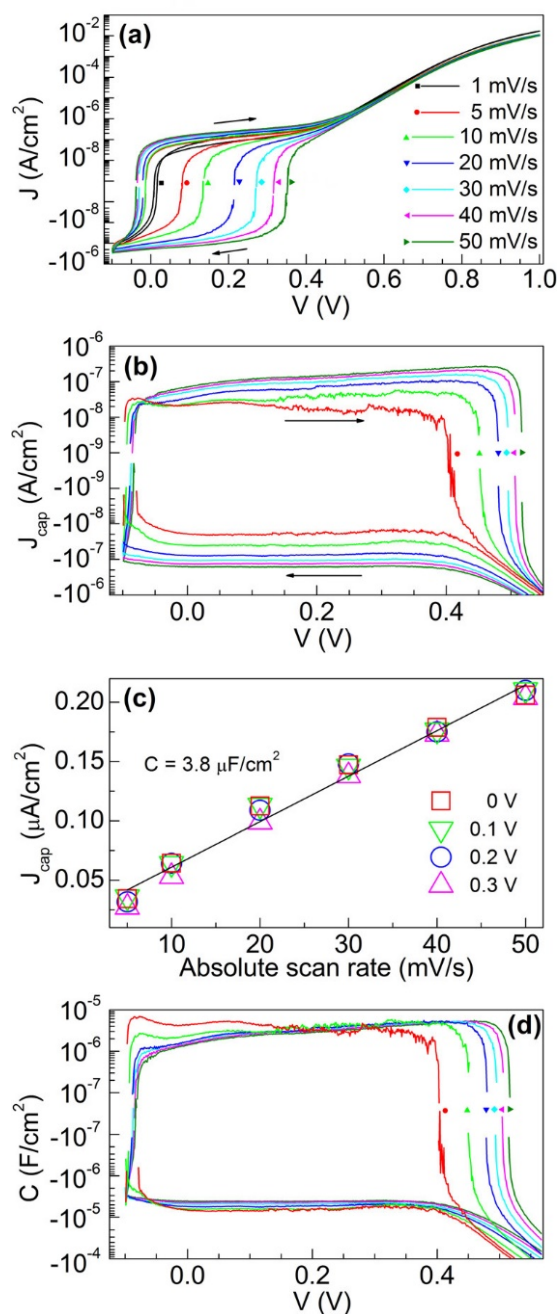


Figure 6.2: Measurements of $\text{CH}_3\text{NH}_3\text{PbI}_3$ solar cell in the dark. (a) $J-V$ curves at different scan rates as indicated with logarithmic scaled currents. (b) Capacitive current density J_{cap} extracted from $J-V$ curves. (c) Current proportional to the scan rate at different applied voltages. (d) Capacitance calculated from $J_{\text{cap}} \text{ s}^{-1}$ at different scan rates as in (a). Reproduced from Ref. [77]. Reproduced from Almora, O.; Zarazua, I.; Mas-Marza, E.; Mora-Sero, I.; Bisquert, J.; Garcia-Belmonte, G. Capacitive dark currents, hysteresis, and electrode polarization in lead halide perovskite solar cells, *J. Phys. Chem. Lett.* 2015, 6, 1645-1652. Copyright 2015 American Chemical Society.

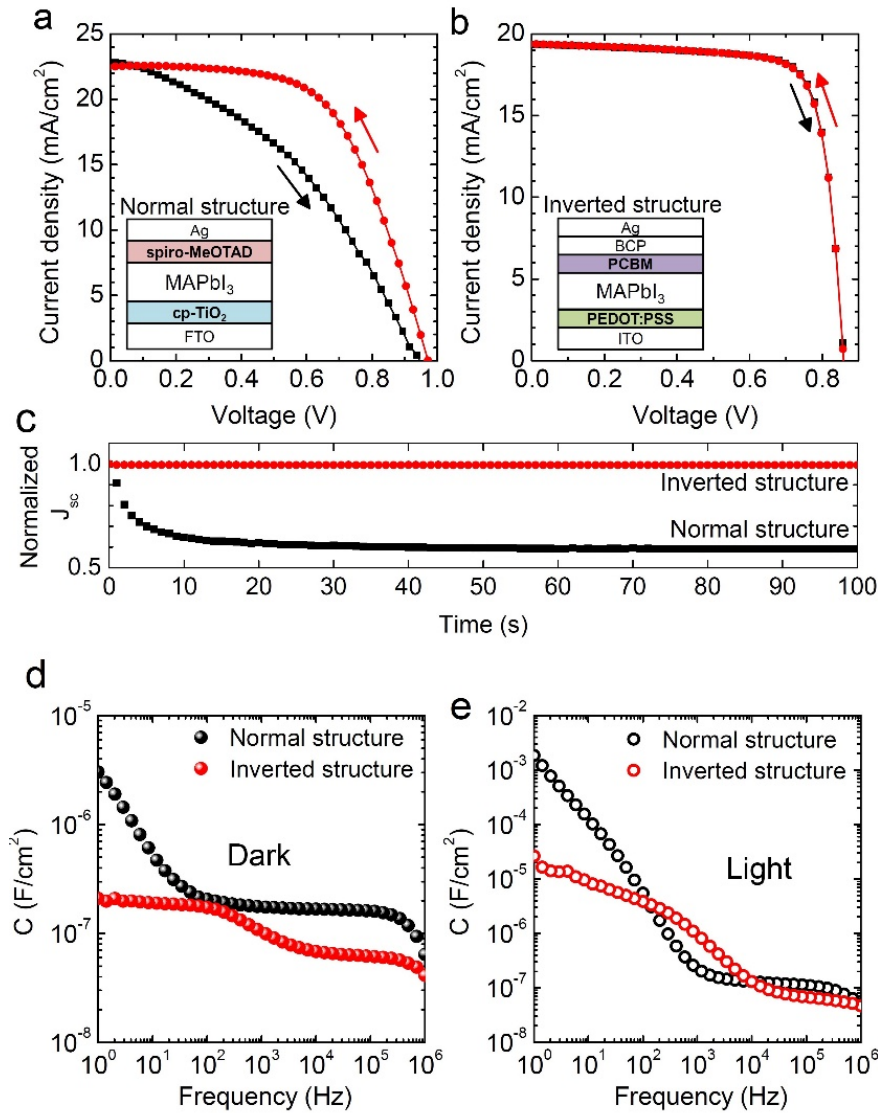


Figure 6.3: a) J – V hysteresis of the cp-TiO₂/MAPbI₃/spiro-MeOTAD (normal) structure and b), the PEDOT:PSS/MAPbI₃/PCBM (inverted) structure. During J – V scan, the current was acquired for 100 ms after applying a given voltage. c) Normalized time-dependent short-circuit current density (J_{sc}) of the normal and the inverted structures. Open-circuit condition under one sun illumination was maintained before measuring J_{sc} . Capacitance-frequency (C – f) curves (d) under dark and (e) one sun illumination at short-circuit condition (bias voltage = 0 V). Reproduced from Kim, H.-S.; Jang, I.-H.; Ahn, N.; Choi, M.; Guerrero, A.; Bisquert, J.; Park, N.-G. Control of I – V Hysteresis in CH₃NH₃PbI₃ Perovskite Solar Cell, *J. Phys. Chem. Lett.* 2015, 6, 4633-4639. Copyright 2015 American Chemical Society

For an ohmic current with a constant resistance R_b we have

$$I_b V = \frac{V}{R_b} \quad (6.2)$$

For a recombination current in a solar cell diode at forward bias

$$I_b V = I_{b0} e^{qV/(m_b k_B T)} \quad (6.3)$$

Here I_{b0} is a constant prefactor, q is the elementary charge, k_B is the Boltzmann's constant, T the absolute temperature, and m_b is an ideality factor [81–83]. For practical reasons we define the ideality factor with dimension of voltage

$$V_b = \frac{m_b k_B T}{q} \quad (6.4)$$

Then Eq. (6.3) can be expressed as

$$I_b(V) = I_{b0} e^{V/V_b} \quad (6.5)$$

For a voltage sweep measurement at velocity v_r we have

$$V = V_0 + v_r \quad (6.6)$$

Then Eq. (6.1) becomes

$$I_{\text{tot}}(V) = C_m v_r + I_{b0} e^{V/V_b} \quad (6.7)$$

The capacitive current is proportional to the scan rate, as commented earlier. In a forward scan the capacitive current is added to the diode exponential curve; while subtracted in the reverse scan (negative v_r). This is the feature of capacitive hysteresis. The representation of Eq. (6.7) is shown in Fig. 6.4a,b. The properties of the current describe very well those reported in Fig. 6.2.

6.2.3 Capacitive Impedance

In the impedance spectroscopy measurement we use a sinusoidal small perturbation $\hat{V}(t)$ over a steady state \bar{V} , $V = \bar{V} + \hat{V}(t)$. For the small perturbation components Eq. (6.1) becomes

$$\hat{I}_{\text{tot}} = C_m \frac{d\hat{V}}{dt} + \frac{1}{R_{\text{rec}}} \hat{V} \quad (6.8)$$

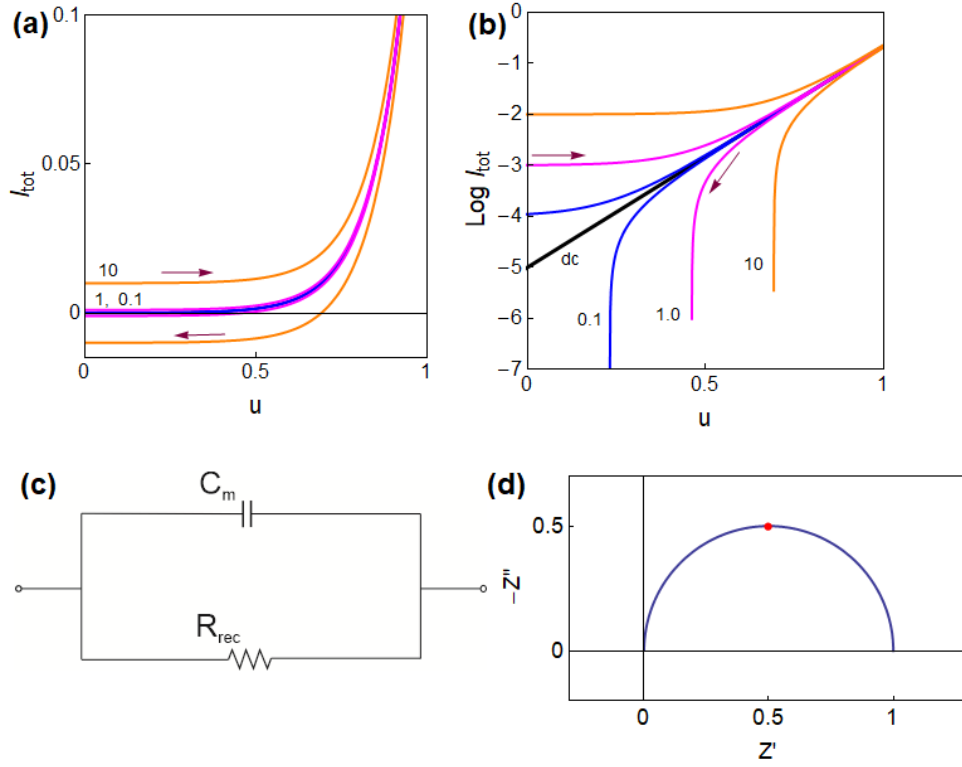


Figure 6.4: Simulation of hysteresis for a diode characteristic in the dark with a constant capacitor in (a) linear and (b) logarithmic current I_{tot} (in A cm^{-2}) as a function of voltage u (in V). In (b) only positive values of current are shown. Parameters $C_m = 0.001 \text{ F cm}^{-2}$, $i_{b0} = 10^{-5} \text{ A cm}^{-2}$, $V_b = 0.10 \text{ V}$. The scan rate v_r for each curve is indicated in V s^{-1} . The dc line of equilibrium is marked by a black line. (c) Equivalent circuit for small ac impedance. (d) Complex plane impedance spectrum for the parameters $C_m = 0.001 \text{ F cm}^{-2}$, $R_{\text{rec}} = \Omega \text{ cm}^2$. The red point is at the characteristic frequency $\omega_m = 1/\tau_m = 1/(R_{\text{rec}}C_m)$.

where the recombination resistance is, by Eq. (6.3),

$$R_{\text{rec}} = \left(\frac{\partial I_b}{\partial V} \right)^{-1} = \frac{V_b}{I_{b0}} e^{-V/V_b} \quad (6.9)$$

Taking the Laplace transformation of Eq. (6.8) we obtain

$$\hat{I}_{\text{tot}} = \left(C_m i\omega + \frac{1}{R_{\text{rec}}} \right) \hat{V} \quad (6.10)$$

Therefore the impedance is

$$Z = \frac{\hat{V}}{I_{\text{tot}}} = \left(C_m i\omega + \frac{1}{R_{\text{rec}}} \right)^{-1} \quad (6.11)$$

This last result is a parallel RC connection EC, Fig. 6.4c, that forms a semiarch in the complex impedance plot, Fig. 6.4d. The associated time constant

is $\tau_m = R_{\text{rec}}C_m$. The elementary EC of a solar cell [42, 84] has the same structure as Eq. (6.11) but C_m is interpreted as a chemical capacitance that depends exponentially on the potential [85].

The characteristic impedance patterns of halide perovskites have been recently summarized [42]. The simplest behaviour found experimentally is given by two arcs as shown in Fig. 6.5b and the related capacitance step in the frequency plot of Fig. 6.5c. It is described by an EC formed by two resistances and two capacitors, Fig. 6.5a. We denote the low frequency arc resistance as R_1 and the high frequency resistance as R_3 [43]. The meaning of the resistances depends on the illumination conditions, but the low frequency arc usually relates to the perovskite/contacts interface (ion migration, accumulation and recombination) [44]. hence, the capacitance C_1 is a surface capacitance related to ionic-electronic phenomena, and C_g is a dielectric geometrical capacitance. The parallel connection of R_1 to C_1 generates the low frequency arc. Typical experimental parameters as a function voltage are shown in Fig. 6.6. It should be noted that Fig. 6.5a cannot be obtained with a simple extension of Eq. (6.1). At least two voltages in series need to be used [25]. Such generalization will be described below.

Fig. 6.6 shows characteristic results of the fitted parameters of the model of Fig. 6.5a under open-circuit conditions. The geometric capacitance C_g is basically constant, but the other three parameters in the EC show an exponential dependence with the voltage [82, 86], and they may be expressed as

$$R_1(V) = R_{10}e^{-qV/(m_1k_Bt)} \quad (6.12)$$

$$R_3(V) = R_{30}e^{-qV/(m_3k_Bt)} \quad (6.13)$$

$$C_1(V) = C_{10}e^{qV/(m_Ck_Bt)} \quad (6.14)$$

Here m_i ($i = 1,3$) is an ideality factor for each resistance parameter and m_C for the low frequency capacitance. In the case of band-to-band recombination it is $m_i = 1$ [87]. In Fig. 6.6 it is obtained $m_i \sim 2$ in all the cases, indicating a recombination resistance. On the other hand C_1 cannot be suitably interpreted as a chemical capacitance [88].

A strong correlation occurs in the low frequency elements, $m_C \sim m_1$, so that the response time for the slow relaxation phenomenon is a constant independent

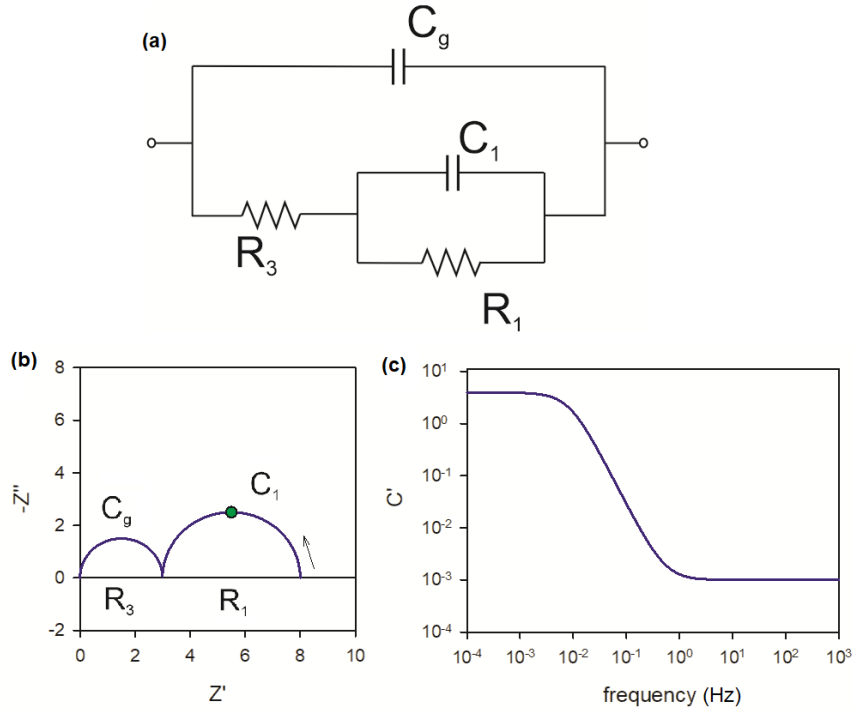


Figure 6.5: (a) Equivalent circuit and (b) complex plane impedance spectrum (impedances in Ω). The arrow indicates the direction of increasing frequency. The point indicates the angular frequency $1/\tau_1 = 1/(R_1C_1)$ (c) Real part of the capacitance vs. frequency. Parameters $R_1 = 5 \Omega$, $R_3 = 3 \Omega$, $C_1 = 10 \text{ F}$, $C_g = 10^{-3} \text{ F}$.

of the voltage [44, 86, 89],

$$\tau_1 = R_1C_1 \quad (6.15)$$

Eqs. (6.13)-(6.15) provide a suitable reference for the construction of a more general model later in this work.

6.2.4 Inductive Hysteresis

Fig. 6.7b shows the typical capacitive current in a dark perovskite diode, already discussed before. A different type of behaviour that produces non-capacitive currents as shown in Fig. 6.7c was identified by Garcia-Belmonte and coworkers [22]. In the region of separation of the current-voltage curves the forward current is smaller than the reverse current. In consequence the current in a voltage sweep changes in the opposite way to the capacitive variation. Fig. 6.7a provides a

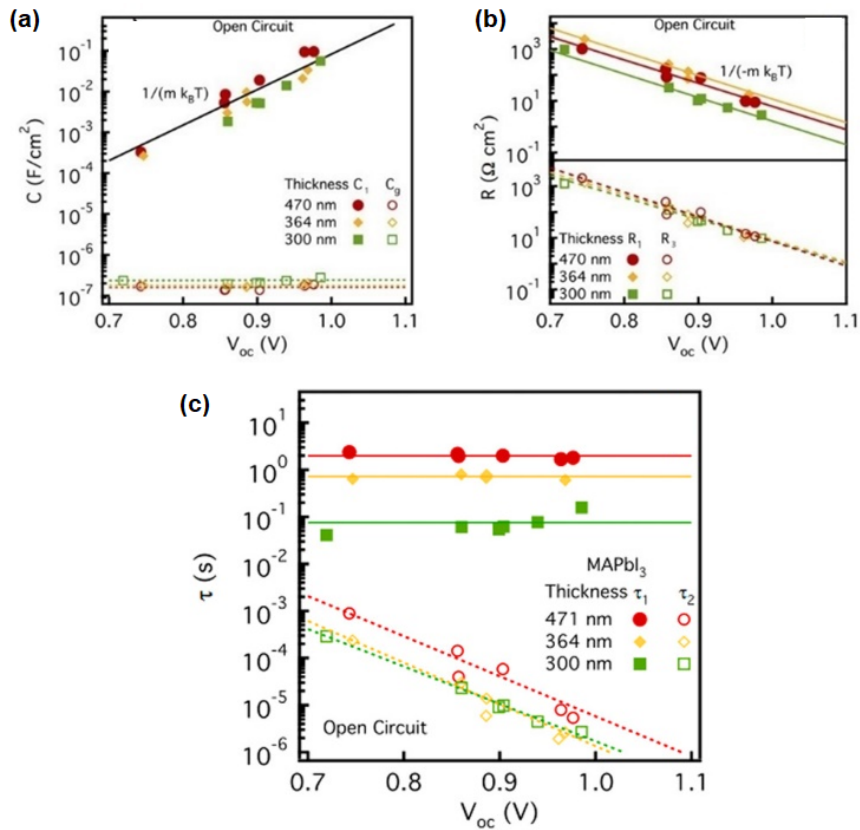


Figure 6.6: Impedance spectroscopy results of a planar structure FTO / TiO₂ / MAPbI₃ / Spiro-OMeTAD / Au solar cell under open-circuit conditions. Solid lines correspond to fits using the simplified EC of Fig. 6.5a. (a) Capacitances C_1 (solid circles) and C_g (empty circles) and (b) resistances R_1 (solid circles) and R_3 (empty circles). Solid lines (low-frequency arc) and dashed lines (high-frequency arc) correspond to linear fits. In panel a, $m = 1.90 \pm 0.17$, and in panel b, $m = 1.94 \pm 0.08$. (c) Characteristic response time calculated from the RC product, for different cell thickness. Solid circles $R_1 C_1$, empty circles $R_3 C_g$. Reproduced from Zarazua, I.; Han, G.; Boix, P. P.; Mhaisalkar, S.; Fabregat-Santiago, F.; Mora-Seró, I.; Bisquert, J.; Garcia-Belmonte, G. Surface Recombination and Collection Efficiency in Perovskite Solar Cells from Impedance Analysis, *J. Phys. Chem. Lett.* 2016, 7, 5105-5113. Copyright 2016 American Chemical Society.

summary of the different types of currents [90]. This behaviour was observed in illuminated solar cells [26], as shown in Fig. 6.8, and termed Inverted hysteresis [24, 26, 53, 54]. This feature is found in many perovskite devices, including solar cells and memristors [35].

For the description of inverted hysteresis we formulate a model that has been denoted a “chemical inductor” [91]. Chemical inductor is a general denomination for a class of dynamical models that occur in different types of systems (corrosion, batteries, neurons, electrocatalysis, memristors). These dynamical models produce a formal inductive response in impedance and transients *without* the occurrence of an electromagnetic (induction) effect. The chemical inductor is *not* related to the previously mentioned chemical capacitance, that describes a charge accumulation by the increase of the chemical potential [14].

Here we apply the chemical inductor to the solar cell [91]. We modify Eq. (6.1) as follows

$$I_{\text{tot}} = C_m \frac{dV}{dT} + i_d \quad (6.16)$$

Here, i_d is a new variable, a current across the solar cell device that does not respond instantaneously to the applied voltage V . It is regulated by the equation

$$\tau_d \frac{di_d}{dt} = I_a(V) - i_d \quad (6.17)$$

τ_d is a time constant parameter for the delay of the current. $I_a(V)$ in Eq. (6.17) is the dc current that gives the steady-state dependence. Indeed, in equilibrium condition we have from the Eqs. (6.16) and (6.17)

$$I_{\text{tot}} = i_d = I_a(V) \quad (6.18)$$

Throughout this paper the uppercase currents as $I_a(V)$ are closed expressions of current-voltage, while the lowercase i_d is a variable current determined by the set of differential equations.

To complete the solar cell model we use for $I_a(V)$ the diode recombination current of Eq. (6.5). The current for a constant sweep rate is given by the equations

$$I_{\text{tot}} = C_m v_r + i_d \quad (6.19)$$

$$V_R \frac{di_d}{dV} + i_d - i_{b0} e^{V/V_b} = 0 \quad (6.20)$$

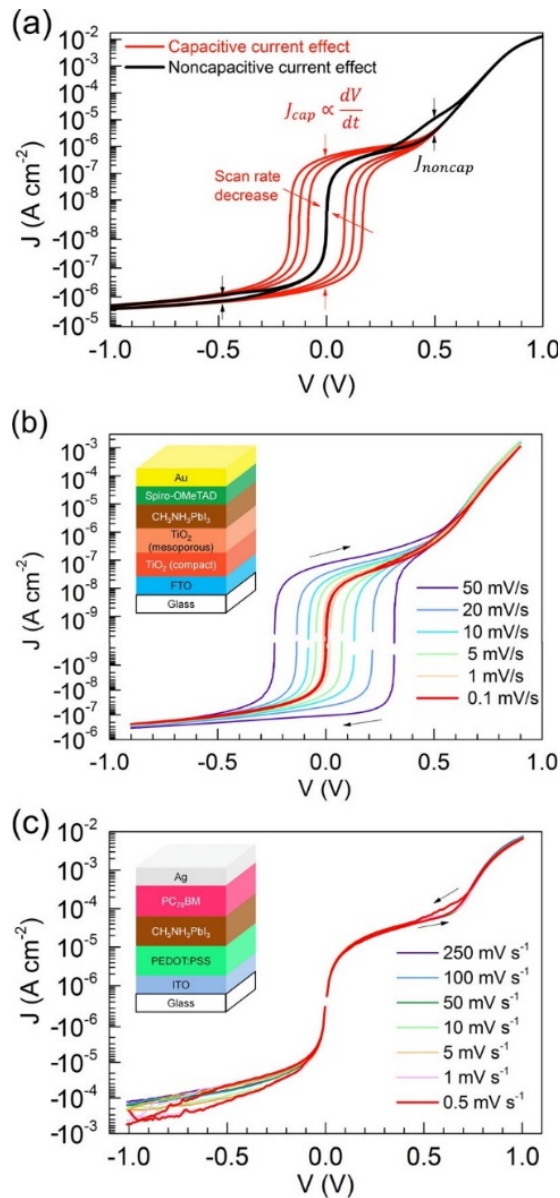


Figure 6.7: Dark $J - V$ curves at room temperature in logarithm scaled current representation: (a) simulation illustrating different hysteretic effects as a function of the scan rate during the bias sweep in both senses; experimental data from (b) Regular meso (FTO / cTiO₂ / mTiO₂ / MAPbI₃ / spiro-OMeTAD / Au) and (c) Inverted (ITO / PEDOT:PSS / MAPbI₃ / PC70BM / Ag) perovskite solar cells at different scan rates with corresponding structures sketched in the insets. Reproduced from Almora, O.; Aranda, C.; Zarazua, I.; Guerrero, A.; Garcia-Belmonte, G. Noncapacitive Hysteresis in Perovskite Solar Cells at Room Temperature, ACS Energy Lett. 2016, 1, 209-215. Copyright 2016 American Chemical Society.

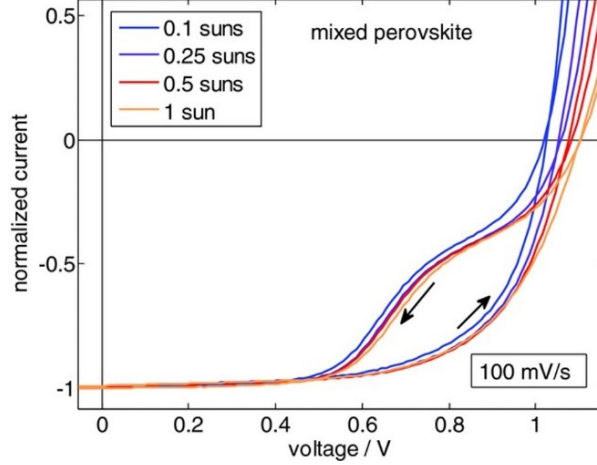


Figure 6.8: Normalized (at -0.2 V) current-voltage curves of a mixed perovskite device measured at different illumination intensities indicating that the S-shape hysteresis is independent of photogenerated charges. Reproduced by permission from Tress, W.; Correa Baena, J. P.; Saliba, M.; Abate, A.; Graetzel, M. Inverted Current-Voltage Hysteresis in Mixed Perovskite Solar Cells: Polarization, Energy Barriers, and Defect Recombination, *Adv. Energy Mater.* 2016, 6, 1600396. Copyright 2016 Wiley.

where we have defined the sweep velocity parameter as

$$V_R = \tau_d v_r \quad (6.21)$$

The differential equation (Eqs. 6.20) is expressed as a function of voltage and can be integrated. For the initial condition $i_d(V = V_0) = i_{d0}$ we obtain

$$i_d(V) = \frac{V_b}{V_b + V_R} I_{b0} e^{V/V_b} + \left(i_{d0} - \frac{V_b}{V_b + V_R} e^{V_0/V_b} \right) e^{(V_0 - V)/V_R} \quad (6.22)$$

Consider the evolution of the first term in the right side (the second term is a transient related to the initial conditions). If the scan rate is slow $V_R < V_b$ the equilibrium curve is not affected and there is not hysteresis. If the scan rate is fast $V_R > V_b$ we obtain

$$i_d(V) = \frac{V_b}{V_R} I_{b0} e^{V/V_b} \quad (6.23)$$

We conclude that the current in inductive hysteresis is inversely proportional to the scan rate.

The total current due to the model of Eqs. (6.16)-(6.17) is obtained inserting Eq. (6.22) into Eq. (6.20). We observe in Eq. (6.23) that the transient inductive current is smaller than the equilibrium current on the forward scan, as shown in

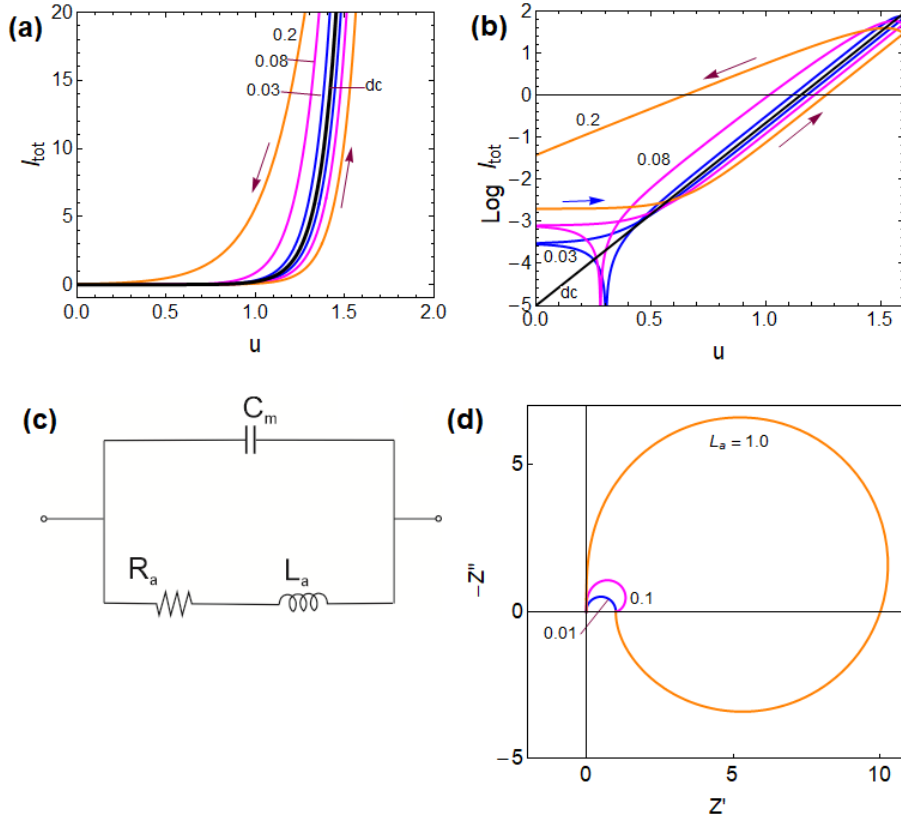


Figure 6.9: Simulation of hysteresis for a diode characteristic in the dark with a constant capacitor and a chemical inductor in (a) linear and (b) logarithmic current I_{tot} (in A cm^{-2}) as a function of voltage u (in V). In (b) the absolute values of current are shown. Parameters $C_m = 0.01 \text{ F cm}^{-2}$, $i_{b0} = 10^{-5} \text{ A cm}^{-2}$, $V_b = 0.10 \text{ V}$, $\tau_d = 1 \text{ s}$. The scan rate v_r is indicated in V s^{-1} . The dc line of equilibrium is indicated by a black line. The blue arrow in (b) indicates a capacitive hysteresis region. (c) Equivalent circuit and (d) Impedance spectra for $C_m = 0.1 \text{ F cm}^{-2}$, $R_a = 1 \Omega$, L_a as indicated (H).

Fig. 6.9a,b. We conclude that the Eqs. (6.16)-(6.17) for the chemical inductor applied to the solar cell describe well the inverted hysteresis features.

In Fig. 6.9b we observe that the capacitive current of Eq. (6.20) dominates at low voltage. There is a crossing from capacitive to inductive current. We will describe this phenomenon more completely later based on the experimental results.

6.2.5 Impedance Properties and Inductive Hysteresis

We analyze the small ac impedance of the chemical inductor model of Eqs. (6.16) and (6.17). We obtain the equations

$$\hat{I}_{\text{tot}} = C_m i\omega \hat{V} + \hat{i}_d \quad (6.24)$$

$$\tau_d i\omega \hat{i}_d = \frac{1}{R_a} \hat{V} + \hat{i}_d \quad (6.25)$$

where the resistance is

$$R_a = \left(\frac{\partial I_a}{\partial V} \right)^{-1} \quad (6.26)$$

We also introduce the chemical inductance

$$L_a = R_a \tau_d \quad (6.27)$$

and we obtain the impedance function

$$Z = \left(C_m i\omega + \frac{1}{R_a + L_a i\omega} \right)^{-1} \quad (6.28)$$

This analysis shows that the introduction of the delayed current i_d in Eq. (6.17) generates an inductor in series with the resistance in Eq. (6.28), cf. Eq. (6.11), so that the EC takes the form shown in Fig. 6.9c. The impedance of the inductor element is $Z(\omega) = L_a i\omega$. If the inductance is small it corresponds to a short circuit and barely changes the RC arc, as shown in the blue spectrum in Fig. 6.9d. But when the inductor is large it creates a big negative loop passing through the fourth quadrant, in the orange line of Fig. 6.9d, until it closes at the real axis of the complex impedance plane to the value of the dc resistance.

Based on the previous results we can establish a direct connection between the existence of an inductive branch in the EC of the impedance results, and the presence of inverted hysteresis in $I - V$ curves. This has been exposed by Fabregat-Santiago and coworkers [92] and it has been explained in general terms by the chemical inductor model [25, 91]. The inductor branch in the EC has a large impact in the solar cell performance as it reduces the recombination resistance and diminishes the power conversion efficiency [92, 93].

By the relation that we have established of noncapacitive currents (Figs. 6.7, 6.8, 6.9) with the inductor element, we may classify hysteresis in two distinct types: *capacitive hysteresis* (regular) and *inductive hysteresis* (inverted).

6.2.6 Interpretation of Inductive Current and the Negative Capacitance

The chemical inductor is normally found in conjunction with additional conduction pathways, leading to an extended model. If the ohmic conduction Eq. (6.2) is included in the model of Eqs. (6.16) and (6.17), then Eq. (6.25) will take the form

$$\hat{I}_{\text{tot}} = C_m i \omega \hat{V} + \frac{\hat{V}}{R_b} + \hat{i}_d \quad (6.29)$$

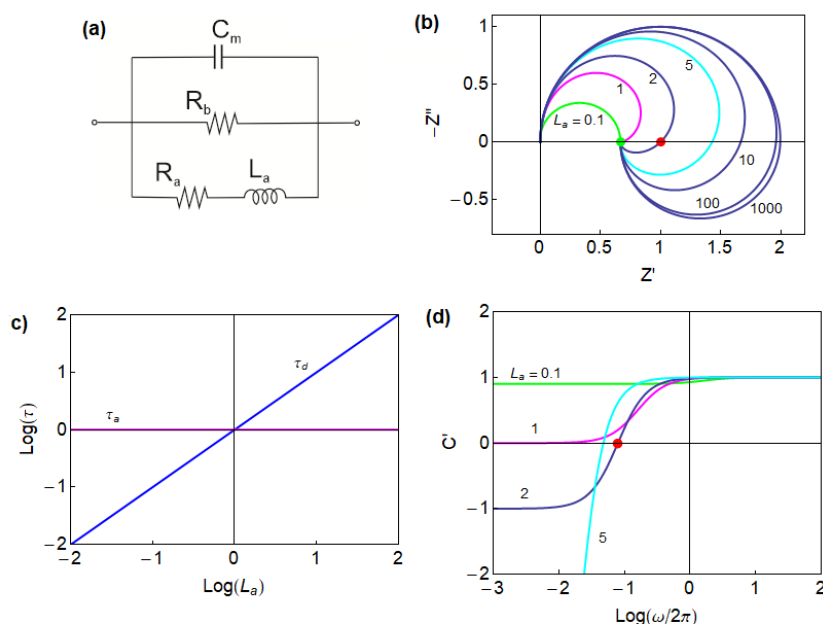


Figure 6.10: (a) Equivalent circuit of the chemical inductor with capacitance and additional conductance. (b) Impedance spectra generated for $C_m = 1 \text{ F}$, $R_a = 1 \text{ } \Omega$, $R_b = 2 \text{ } \Omega$ and L_a as indicated (H). The green dot is the dc resistance at $\omega = 0$, and the red dot is the resistance at the intercept when the spectrum crosses the real axis Z' . (c) The time constants $\tau_a = R_a C_m$ and $\tau_d = L_a / R_a$ for a varying inductance. The negative loop in the complex plane occurs when $\tau_d > \tau_a$ is satisfied. (d) Representation of the real part of the capacitance as a function of frequency. The red point indicates the crossing of the horizontal axis.

When combined with Eq. (6.17), this more general model leads to the EC of Fig. 6.10a, which displays a variety of spectra shown in Fig. 6.10b. Again, the negative loop is observed for the larger values of the inductor parameter. Fig. 6.10c indicates that the crossing to the fourth quadrant occurs when the

condition

$$\tau_d = \frac{L_a}{R_a} > \tau_a = R_a C_a \quad (6.30)$$

is satisfied [91]. In Eq. (6.29) the decrease of the current of the chemical inductor at increasing scan rate is limited by the parallel branch R_b [25].

The complex capacitance $C(\omega)$ is defined from the impedance as

$$C(\omega) = \frac{1}{i\omega Z(\omega)} \quad (6.31)$$

The real part of the capacitance is denoted $C'(\omega) = \text{Re}[C(\omega)]$. In the capacitive model of Fig. 6.5 the total capacitance is strictly positive, Fig. 6.5c. Fig. 6.10d shows an interesting phenomenon. When the loop in the fourth quadrant occurs in the complex plane impedance spectrum, the complex capacitance becomes negative. We arrive at the conclusion that the chemical inductor generates the feature of a negative capacitance at low frequency that has been extensively reported in halide perovskite solar cells [45, 47, 84, 94–98]. The negative capacitance can be described by a positive chemical inductor that arises from the model of Eqs. (6.16) and (6.17). A truly negative capacitance parameter is not necessary.

The chemical inductor is generally obtained from the delay equation (6.17), as shown above [99]. But what is the interpretation of this delay effect in halide perovskites? Since the observation of the negative capacitance is widespread, many different explanations are provided. Some examples are the physical surface polarization model [76, 100], the changing environment of ions when their occupation at the double layer is modified by the photovoltage or polarization [89, 101, 102], and the modulation of electronic conduction or recombination currents [52, 94–97, 103–105]. Most of these models have in common that a slow step of ionic displacement determines a faster step of electronic current recombination or transfer at the contact. These different models presented for negative capacitances and inductive hysteresis are compatible with the general operation principle of the chemical inductor. In fact the model of a chemical inductor originates from a voltage-gated ion channel in the neuron membrane originally described by Hodgkin and Huxley [62, 63]. It describes well a voltage gated electronic current at the bulk of surface of the solar cell [52, 94–96]. However, the

molecular mechanism of this behavior has not been determined yet in perovskite solar cells.

6.3 Methods

6.3.1 MAPbBr₃ Solar Cell Fabrication

The fluorine-doped tin oxide (FTO) substrates were partially etched with zinc powder and 2 M HCl solution. The etched samples were brushed to mechanically remove the remaining residues of the etching procedure, then, were sonicated for 15 minutes each in deionized water with Hellmanex detergent solution, acetone, and isopropyl alcohol, respectively. The cleaned substrates are then dried using a nitrogen gun.

In preparation for the electron selective titanium dioxide (TiO₂) compact layer deposition, the cleaned substrates were subjected to ultraviolet (UV) ozone treatment for 15 minutes to further remove organic contaminants on the substrate surface. The TiO₂ compact layer was then deposited via spray pyrolysis of 1:9 titanium (IV) diisopropoxide bis (acetylacetonate) (75% solution in 2-propanol, Sigma Aldrich) (60 % in acetylacetonate):ultrapure ethanol at 450 °C with oxygen as carrier gas. The TiO₂ compact layer is then kept at 450 °C for 35 minutes before letting the samples cool down to room temperature. Another UV ozone treatment for 15 minutes was conducted to samples with the TiO₂ compact layer to ensure ultraclean surface prior to the deposition of TiO₂ mesoporous layer. A 100 μL diluted TiO₂ paste (Dyesol) (150 mg: 1 mL ultrapure ethanol) was then spin-coated onto the TiO₂ compact layer at a speed of 2000 RPM, acceleration of 2000 RPM/s with a duration of 10 s. The deposited TiO₂ mesoporous layer was annealed under ambient conditions at the following temperature, ramp time and dwell time: 370 °C with 40 minutes ramp for 20 minutes, 470 °C with 25 minutes ramp for 10 minutes, and 500 °C with 10 minutes ramp for 30 minutes.

Once the annealing treatment of the TiO₂ mesoporous layer was completed, the samples were cooled down to 150 °C and were immediately transferred inside a glove box in preparation for the MAPbBr₃ deposition. A 1.4 M MAPbBr₃ precursor solution is prepared using PbBr₂ (>98 %, TCI) and MABr (>99.99 %, Greatcell Solar) in 1:4 dimethylsulfoxide (DMSO) (≥99.9 %, Sigma Aldrich):N,N-

dimethylformamide (DMF) (99.8 %, Sigma Aldrich) solution. A 50 μL MAPbBr₃ perovskite solution was statically spin-coated onto the TiO₂ mesoporous layer via a two-step anti-solvent method: 1000 RPM for 10 s then 4000 RPM for 40 s. A 100 μL toluene (99.8 %, Sigma Aldrich) anti-solvent was injected 22 seconds before spin coating ends. The samples were then annealed at 100 °C for 30 minutes.

The hole selective lithium-doped 2,2',7,7'-Tetrakis [N,N - di(4-methoxyphenyl) amino] - 9,9'-spirobifluorene (Spiro-OMeTAD) was deposited on top of the annealed perovskite layer. A 72.3 mg Spiro-OMeTAD in 1 mL chlorobenzene (99.8 %, Sigma Aldrich), 28.8 μL 4-tert-butylpyridine (98 %, Sigma Aldrich) and 17.5 μL of a stock solution of 520 mg lithium bis-(trifluoromethyl sulfonyl) imide (99.95 %, Sigma Aldrich) in 1 mL acetonitrile (99.8 %, Sigma Aldrich) was prepared. A 50 μL lithium-doped Spiro-OMeTAD solution was dynamically spin-coated at 4000 RPM, 800 RPM/s for 30 s. Finally, an 85 nm gold contact was thermally evaporated using a commercial Oerlikon Leybold Univex 250.

6.3.2 MAPbBr₃ Solar Cell Characteristic $J - V$ Curves and Statistics

The characteristic $J - V$ curves of the MAPbBr₃ solar cells were measured with a mask aperture area of 0.120 cm² using a computer controlled Keithley 2400 under a simulated AM1.5 solar spectrum from an ABET Technologies Sun 2000 solar simulator. The MAPbBr₃ solar cells had total active areas of ~ 0.257 cm².

6.3.3 Impedance Spectroscopy Measurements

All electrical measurements were conducted inside a nitrogen-controlled glove box under dark conditions using Autolab PGSTAT204. The voltage-dependent IS response was measured via a sequence of chronoamperometry (CA) for 5 s, subsequently followed by IS with a frequency range of 1 MHz to 0.02 Hz and a perturbation amplitude of 0.01 V. The CA-IS sequence was carried out at varying applied voltages (V_{app}) from 0 to 2 V at 0.1 V increments.

6.4 Results and Discussion

Fig. 6.11 shows the electrical characterization of the fabricated MAPbBr₃ solar cells. I-V characteristics and device statistics are presented in Fig. 6.11a,b. The power conversion efficiencies approaching 6 % in the forward and reverse scan direction, are within the normal values reported for this formulation [68]. Devices with optimized contacts can show still higher efficiency [106, 107].

The current-voltage curves in the dark at different scan rates in Fig. 6.11c show intense inverted hysteresis and correspondingly exhibit decreasing current levels with increasing scan rates, as indicated in Fig. 6.11d [25, 52]. The log scale representation of Fig. 6.11d reveals a region of capacitive hysteresis at low voltage as announced in Fig. 6.9 before. A crossing point is observed in which a transition from regular to inverted hysteresis occurs. This transition has been applied recently to explain the negative spikes observed in transient time measurements [99]. Fig. 6.11g shows that the forward current is inversely proportional to the scan rate for the slow voltage sweeps, as predicted in Eq. (6.23) for the chemical inductor. For faster scan rates the current tends to reach a minimum due to parallel pathways, as discussed before in Eq. (6.29). A similar behavior is observed in the current-voltage curves under illumination at different scan rates. However, the crossing point under light is not fixed. It shifts from values close to 0 V at low scan rates (Fig. 6.11e) to higher values with an increase in the sweep rate. At fast scan rates (Fig. 6.11f) the crossing point is not observed and the hysteresis is only inductive. Since this additional effect complicates the analysis in the following only data in the dark will be discussed.

These properties can be put in correspondence with the stabilized impedance spectra shown in Fig. 6.12. The fully capacitive spectra, consisting on several arcs in the low voltage region (Fig. 6.12a,b), correspond to the regular hysteresis domain. In the high voltage region, a large inductive feature appears (Fig. 6.12c,d) that causes a negative transient current resulting to an inverted hysteresis. These separate features have been explained in the Section 6.2. As described earlier, ionic charges can modulate the carrier extraction rate or recombination current. As the ionic motion is much slower than electronic response, a delay of the electrical current is observed that causes capacitive and inductive

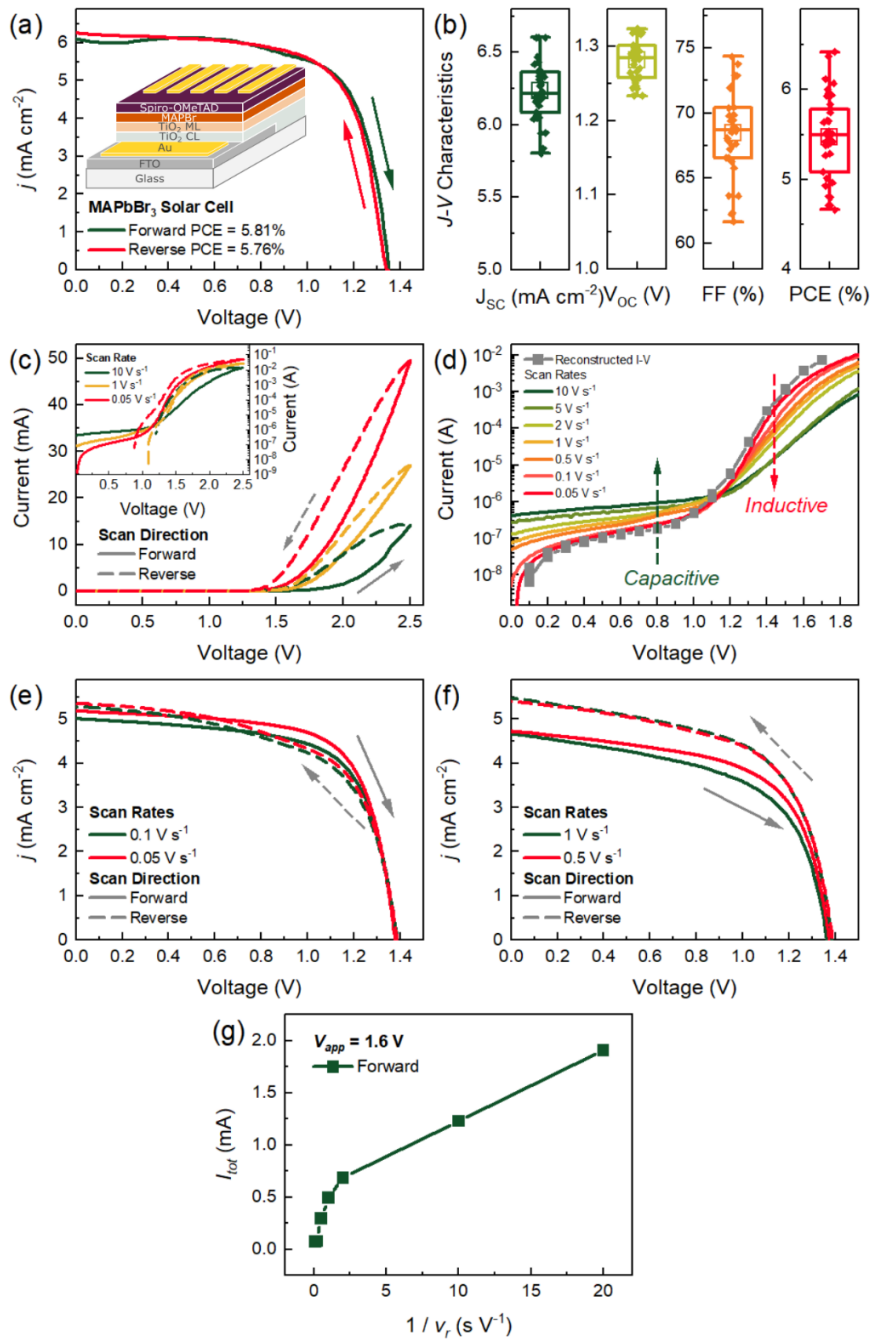


Figure 6.11: (a) Characteristic $I-V$ curve of the MAPbBr₃ solar cell under 1 sun illumination exhibiting inverted hysteresis with the inset showing the schematic diagram of the device configuration. (b) $I-V$ characteristic parameter statistics of 34 devices measured in the reverse scan direction. (c) Forward and reverse $I-V$ scans with varying scan rates exhibiting inverted hysteresis measured inside a nitrogen-controlled glove box under dark conditions. (d) Evolution of hysteresis in the forward direction in log vertical scale in dark. (e)-(f) Hysteresis under illumination conditions. (g) Current in forward for inverted hysteresis in the dark at 1.6 V, vs. reciprocal scan rate.

components.

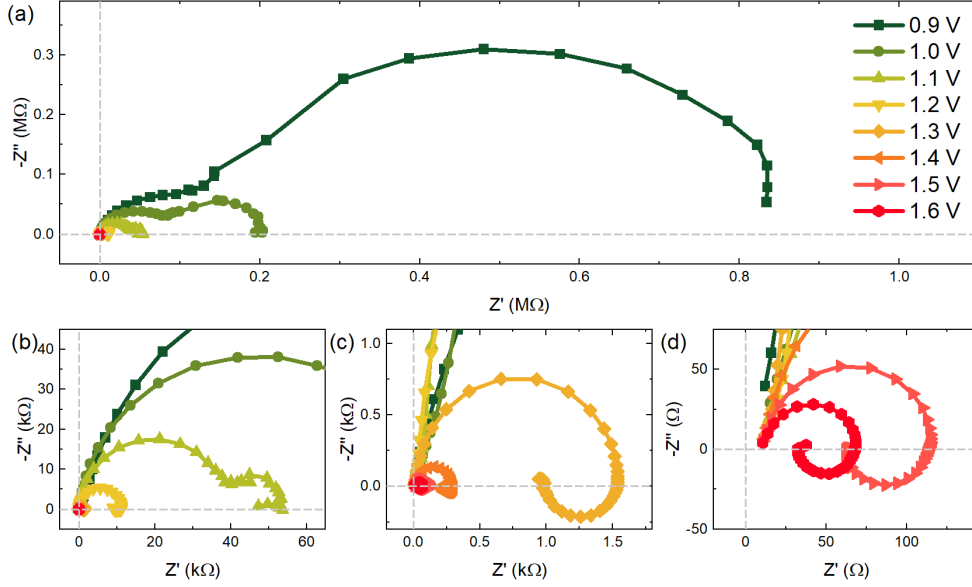


Figure 6.12: (a) Representative IS spectral evolution of the the MAPbBr₃ solar cell at $V_{\text{app}} = 0.9$ to 1.6 V under dark conditions. (b)-(d) shows different magnifications around the origin.

6.4.1 The Dynamical Model

We present here an advanced dynamical model that enables to correlate both the results of impedance and current-voltage curves, and obtain a physical interpretation of the evolution of parameters with the voltage. The model is formulated as a set of dynamical equations valid for any type of perturbation. These equations contain the minimal components to describe all the features shown in Fig. 6.11 and 6.12, based on the experience in different capacitive and inductive components and series and parallel elements that has been summarized in Section 6.2. This model goes further than combining the component parts as it needs to account for the data across the whole voltage range and especially it must explain the emergence of the inductor and the disappearance of the low frequency impedance arc in Fig. 6.12. The model is the first of its kind that introduces a voltage divisor in order to deal with two impedance arcs [50].

The physical basis for the model is shown in Fig. 6.13. The total current flowing through the device is divided into the following components:

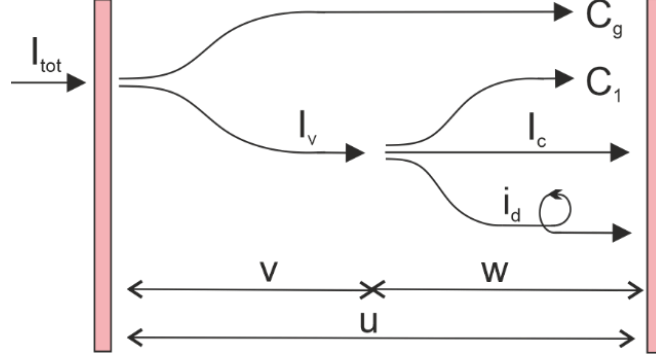


Figure 6.13: Scheme of the dynamical model showing total current I_{tot} and voltage u , internal voltages $u = v + w$, conduction (I_v , I_c , i_d) and capacitive (C_g , C_1) currents between the current collector plates. The lines arriving to the right contact indicate the dc current.

1. A part of I_{tot} is a displacement current that charges the geometrical capacitance of the perovskite material (C_g).

The remaining current I_v will be divided in three branches:

2. Charging the surface capacitance C_1 .
3. Extracting rapid current I_c at the contact.
4. Extracting current slowly via an ion modulated current i_d .

Therefore, the model equations are

$$I_{\text{tot}} = C_g \frac{du}{dt} + I_v(v) \quad (6.32)$$

$$I_v(v) = \frac{dQ_s(w)}{dt} + I_c(w) + i_d \quad (6.33)$$

$$\tau_d \frac{di_d}{dt} = I_d(w) - i_d \quad (6.34)$$

The external variables are the total current I_{tot} and voltage u . The voltage is divided in two internal parts v, w , that correspond to bulk and surface potential differences, respectively, and satisfy

$$u = v + w \quad (6.35)$$

The internal currents $I_v(v)$, $I_c(w)$ are instantaneous functions of the respective voltage, while i_d is a variable current that is delayed by a characteristic time τ_d due to ionic effects, as described in Section 6.2.4 [91]. Hence Eq. (6.34) is

the standard form of the chemical inductor introduced in (6.17). The model also includes a surface charge function $Q_s(w)$, and the stationary value of the delayed current, $I_d(w)$ [50].

We have noted in Eq. (6.13)-(6.14) that the resistances and capacitance in perovskite solar cells have exponential dependencies on voltage, and some of them are correlated. Based on these observations, we assume the exponential dependence in the currents

$$I_v(v) = I_{v0}e^{v/V_b} \quad (6.36)$$

$$I_c(w) = I_{c0}e^{w/V_b} \quad (6.37)$$

$$I_d(v) = Ie^{w/V_b} \quad (6.38)$$

Here I_{v0} , I_{c0} , I_{d0} are prefactors and V_b , V_d are ideality factors [81] with dimension of voltage.

According to Fig. 6.13 the partial currents satisfy the following equation in dc conditions

$$I_v(u - w) = I_c(w) + I_d(w) \quad (6.39)$$

By Eq. (6.39) the relation of external voltage u to internal potential is

$$u = V_b \ln \left(\frac{I_{c0}}{I_{v0}} e^{2w/V_b} + \frac{I_{d0}}{I_{v0}} e^{w/V_c} \right) \quad (6.40)$$

where

$$V_c^{-1} = V_d^{-1} + V_b^{-1} \quad (6.41)$$

The total current is shown in Fig. 6.14a and the distribution of the internal voltages in Fig. 6.14b. Since $V_d < V_c$, the delayed current I_d , that starts at a low value in Fig. 6.14a, overcomes the direct recombination current I_c at the internal voltage value given by the parameter

$$w_T = \left(\frac{1}{v_d} - \frac{1}{V_b} \right)^{-1} \ln \left(\frac{I_{c0}}{I_{d0}} \right) \quad (6.42)$$

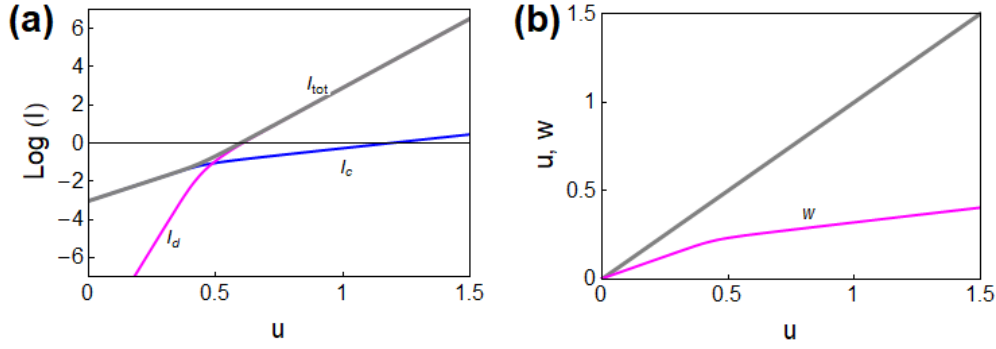


Figure 6.14: Model simulation. (a) Stationary current-voltage curve and the component currents, (b) distribution of internal voltage. Parameters: $I_{v0} = 10^{-3}$; $I_{c0} = 0.9 \times 10^{-3}$; $I_{d0} = 10^{-11}$; $V_b = 0.05$; $V_d = 0.01$. Currents in A and voltages in V.

6.4.2 AC Impedance Model

For the interpretation of impedance spectroscopy of our experimental results, we develop Eqs. (6.33)-(6.34) into the small perturbation equations, that become

$$\hat{I}_{\text{tot}} = C_g \frac{d\hat{u}}{dt} + \frac{1}{R_a} \hat{v} \quad (6.43)$$

$$\frac{1}{R_a} = C_1 \frac{d\hat{w}}{dt} + \frac{1}{R_1} \hat{w} + \hat{i}_d \quad (6.44)$$

$$L_a \frac{d\hat{i}_d}{dt} = \hat{w} - R_a \hat{i}_d \quad (6.45)$$

Here the new circuit elements have the form

$$C_1 = \frac{dQ_s}{dw} \quad (6.46)$$

$$R_1 = \left(\frac{I_c}{dw} \right)^{-1} \quad (6.47)$$

$$R_3 = \left(\frac{I_v}{dv} \right)^{-1} \quad (6.48)$$

$$R_a = \left(\frac{I_d}{dw} \right)^{-1} \quad (6.49)$$

$$L_a = \tau_d \left(\frac{dI_d}{dw} \right)^{-1} \quad (6.50)$$

C_1 is a capacitance related to the surface charging [67, 85],86,114 R_1 , R_3 , R_a are variable resistances connected to the currents of Eqs. (6.37)-(6.38), and L_a

is an inductor associated to the delayed current of Eq. (6.34). Now the different resistances can be calculated as a function of voltage.

$$R_1 = \frac{V_b}{I_{c0}} e^{-w/V_b} \quad (6.51)$$

$$R_a = \frac{V_d}{I_{d0}} e^{-w/V_d} \quad (6.52)$$

$$R_3 = \frac{V_b}{I_{v0}} e^{-v/V_b} \quad (6.53)$$

Noting the correlations of C_1 and R_1 commented in Fig. 6.6 we write

$$C_1 = C_{10} e^{w/V_b} \quad (6.54)$$

We have the characteristic times

$$\tau_1 = R_1 C_1 \quad (6.55)$$

$$\tau_a = R_a C_1 \quad (6.56)$$

$$\tau_d = \frac{L_a}{R_a} \quad (6.57)$$

By taking the Laplace transform of Eqs. (6.44)-(6.45) in terms of the variable $s = i\omega$, the calculation of the impedance $Z = \hat{u}/\hat{I}_{\text{tot}}$ gives the result

$$Z(s) = \left[C_g s + \frac{1}{R_s + \frac{1}{C_1 s + \frac{1}{R_1} + \frac{1}{R_a + L_a s}}} \right]^{-1} \quad (6.58)$$

The impedance in Eq. (6.58) becomes that of the EC of Fig. 6.15, with the addition of a constant series resistance R_s . The branch formed by R_a and L_a is the arrangement of the chemical inductor that describes delayed surface-controlled recombination as in Section 6.2.5.

6.4.3 Obtaining the Impedance Parameters

The analysis of the spectra of Fig. 6.12 cannot be done by direct fitting of the full equivalent circuit of Fig. 6.15, since the elements of the circuit are not present in the entire voltage range. Different simplifications of Fig. 6.15 are used as EC in separate voltage ranges as shown in Fig. 6.16, that displays the EC adopted in the various domains for the spectral analysis of IS data in Fig. 6.12.

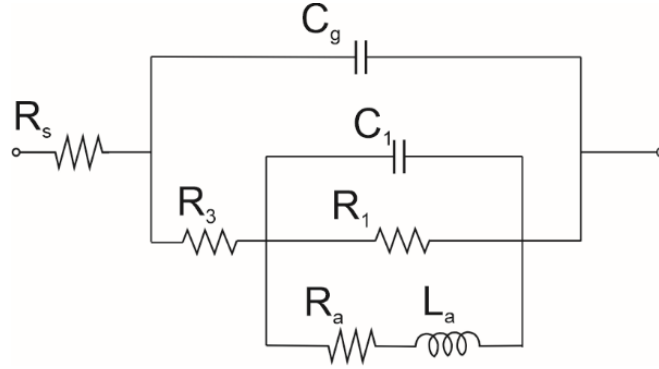


Figure 6.15: The schematic diagram of the general equivalent circuit model.

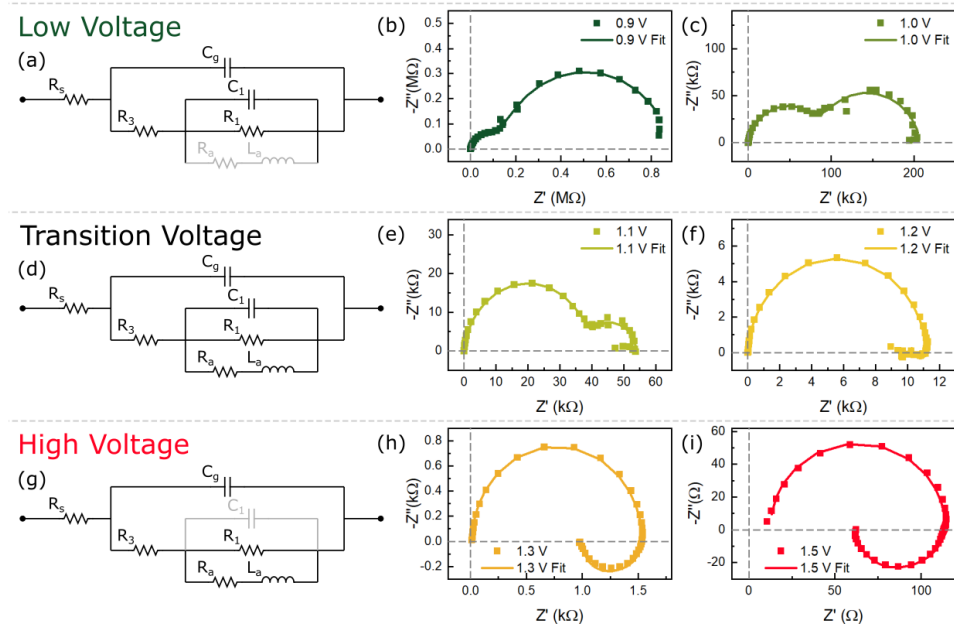


Figure 6.16: Individual representative IS spectral evolution of the MAPbBr₃ solar cell at varying applied voltages (V_{app}) under dark conditions exhibiting (b-c) the fully capacitive regime at low voltages ($V_{app} < 1.1$ V), (e-f) the region of transformation (1.1 V $\leq V_{app} \leq 1.2$ V), and (h-i) the inductive regime at high voltages ($V_{app} > 1.2$ V) with the corresponding equivalent circuits (a, d, and g), respectively.

At low voltages in Fig. 6.16a the inductor impedance is large, and we obtain the double RC feature of Fig. 6.16a that was shown previously in Fig. 6.5, see the spectra Fig. 6.16b,c. The intermediate region of voltages in Fig. 6.16d is a transition region where all the elements in the EC are present. The spectra in Fig. 6.16e,f show the replacement of the low frequency arc by an incipient inductive feature. At high voltages in Fig. 6.16g the capacitive arc associated to C_1 is not observed, and it is replaced by the chemical inductor feature of Fig. 6.10. Now the inductive arc is well developed in the experimental spectra in Fig. 6.16h,i. An additional parallel shunt resistance of constant value R_{sh} is used in the fitting as described in the Supporting Information. The fits capture well the features of the impedance spectra as shown in Fig. 6.16 with the resulting EC parameters summarized in Fig. 6.17: resistances (Fig. 6.17a), effective capacitances (Fig. 6.17b), effective inductance (Fig. 6.17c) and the corresponding time constants (Fig. 6.17d).

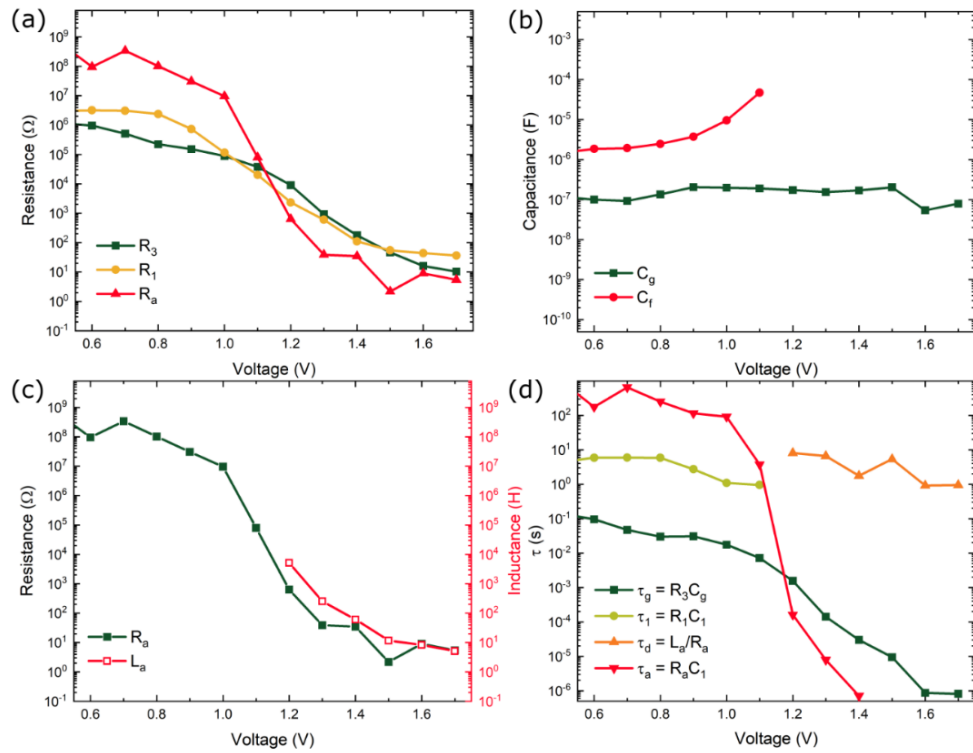


Figure 6.17: The voltage-dependent evolution of the (a) resistances, (b) capacitances, (c) inductance at high voltage, and (d) the corresponding time constants resulting from the fitting using Eq. (6.13) with a consistent shunt resistance of $\sim 1.24 \times 10^9 \Omega$ throughout the voltage range.

In Fig. 6.17, we find well established features of the impedance parameters of the low voltage region, by comparison to Fig. 6.6. The R_1 and R_3 decrease exponentially with voltage, with similar slopes, as in Fig. 6.6b. The R_a also decreases with voltage but with a different slope, and it is correlated to L_a , which makes τ_d a constant as assumed in the model. The C_1 increases exponentially as in Fig. 6.6a, inversely correlated to R_1 , hence the characteristic time τ_1 in Fig. 6.17d is a constant as in Fig. 6.6c.

6.4.4 Transition from Capacitor to Inductor

We now discuss the properties of the chemical inductor observed in Fig. 6.17. The change from capacitor to inductor is controlled by the relation of the time constants as explained in Fig. 6.10. When $\tau_d > \tau_a$, there is a transition of the spectra in the low frequency range, with the appearance of the inductor in the fourth quadrant (producing a negative capacitance feature).

Let us write the time constant τ_1 using Eqs. (46,47,55)

$$\tau_1 = \frac{dQ_s}{dw} \frac{1}{\frac{dI_c}{dw}} = \frac{dQ_s}{dI_c} \quad (6.59)$$

We obtain that the ionic charging of the interface occurs with the time constant τ_1 as follows

$$Q_s \approx \tau_1 I_c \quad (6.60)$$

We note the property of nearly continuity of characteristic times obtained in Fig. 6.17d

$$\tau_1 \approx \tau_d \quad (6.61)$$

We have remarked before that the capacitor C_1 vanishes when the inductive process appears. The match of time constants in Eq. (6.61) explains the relation between them. According to the proposed interpretations [44, 52, 58, 86], the current I_c in Fig. 6.13 is a surface recombination process observed at low voltages, influenced by ionic changing from the bulk via the ionic-electronic capacitance C_1 . The delayed current i_d in Fig. 6.13 dominant at high voltage is a recombination current influenced by ionic transport to the interface. Hence L_a and C_1 are not completely independent processes: they both relate to the ionic influence on recombination. Both correspond to a similar ionic-controlled recombination, one

is capacitive, the other inductive. Therefore, they are represented by different branches in Fig. 6.13 and Fig. 6.15. The connection between capacitive and inductive time constants is also found in a surface polarization model in which the slow variable that produces the chemical inductor is a surface voltage [100].

By the Eqs. (6.60) and (6.61), we write the prefactor of the capacitor in Eq. (6.54) as

$$C_{10} = \frac{I_{c0}\tau_d}{V_b} \quad (6.62)$$

and we get the charging function as

$$Q_s = I_{c0}\tau_d e^{w/V_b} \quad (6.63)$$

The EC elements are then plotted in Fig. 6.18a and reproduce the tendencies of the experimental features observed in Fig. 6.17. The model accounts successfully for the voltage variation of the impedance parameters.

In addition, the model shows that the correlation [82, 86, 89] often observed on R_1 and R_3 is based on Eq. (6.39) and occurs when there are no alternative pathways to the current, e.g., while $I_d(w)$ is small and the shunt resistance is large.

The characteristic times are shown in Fig. 6.18b. As already discussed, there is a continuity of $\tau_1 = \tau_d$ in the transition from capacitive to inductive impedance spectra. It can be stated that

$$\tau_a = R_a C_1 = \tau_d \frac{I_{c0} V_d}{I_{d0} V_b} e^{\left(\frac{1}{V_b} - \frac{1}{V_d}\right)w} \quad (6.64)$$

As already mentioned, the transition where the impedance enters the fourth quadrant, occurs when the time $\tau_a < \tau_d$ [66]. However, if $\tau_a > \tau_d$ at all voltages, there will not be a domain of negative capacitance effect. The condition (Eq. 64) therefore explains in which cases there will be an observation of inductive or negative capacitance features.

6.4.5 Change of Type of Hysteresis

Finally, we aim to explain the transition from regular to inverted hysteresis observed in the current-voltage curves of Fig. 6.11d, corresponding to the change

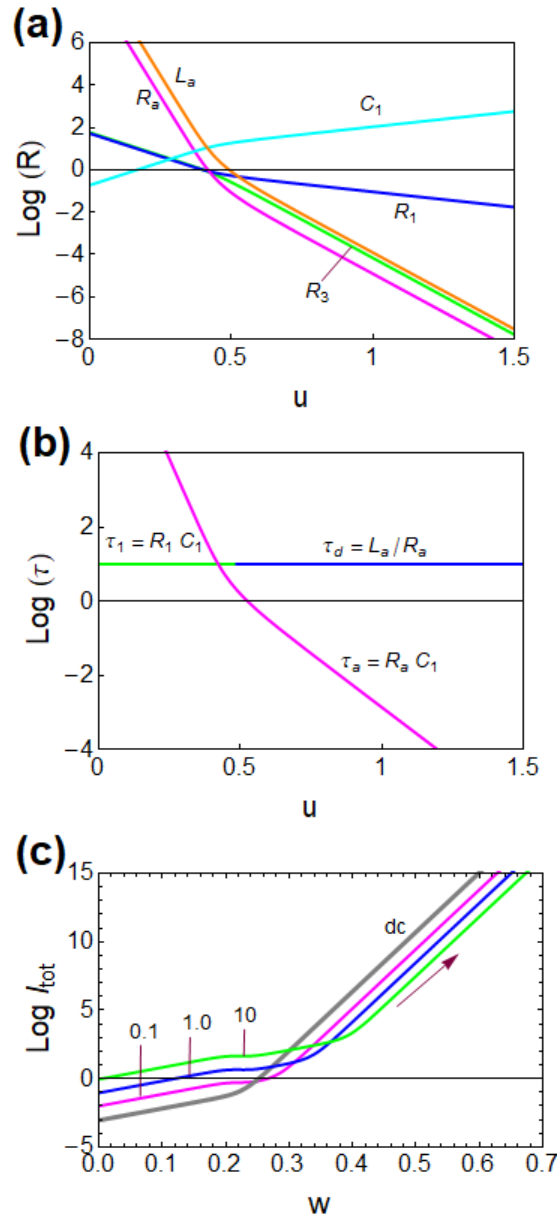


Figure 6.18: Simulation of the model. (a) Impedance parameters, C in F, R in Ω , L in H, current in A, voltages in V. (b) Characteristic times (s), and (c) current-voltage curves at different scan rates $v_r = 0.1, 1.0, 10$ (V s^{-1}) as indicated. The grey line is the dc stationary current. Parameters: $I_{v0} = 10^{-3}$; $I_{c0} = 0.9 \times 10^{-3}$; $I_{d0} = 10^{-11}$; $V_b = 0.05$; $V_d = 0.01$; $\tau_d = 10$ s. Currents in A and voltages in V.

of the impedance from capacitive to inductive response. We formulate the dynamical equations for the stimulus of a voltage sweep as in Eq. (6.6)

$$u = v_r t \quad (6.65)$$

Hence, we obtain

$$I_{\text{tot}} = C_g v_r + C_1(w) v_r \frac{dw}{du} + I_c(w) + I_v(w) \quad (6.66)$$

$$\tau_d v_r \frac{dw}{du} \frac{dI_d}{dw} = I_d(w) - I_d \quad (6.67)$$

where

$$\frac{dw}{du} = \frac{I_{c0} e^{2w/V_b + I_{d0} e^{w/V_c}}}{2I_{c0} e^{2w/V_b} + \frac{V_b}{V_c} I_{d0} e^{w/V_c}} \quad (6.68)$$

The differential equation Eq. (6.67) can be solved for the given v_r and inserted into Eq. (6.67) to provide the total current. The resulting current-voltage curves at forward scan are shown in Fig. 6.18c and reproduce the crossing due to change of hysteresis type observed in Fig. 6.11d.

6.5 Conclusion

We formulated a dynamical model for the external current, the voltage, and a few internal variables of a solar cell, to describe impedance spectroscopy and hysteresis in current-voltage curves of halide perovskite solar cells that show a transition from a capacitive domain at low voltage to an inductive domain at high applied voltage. The model reproduces the main experimental characteristics of impedance, steady state current-voltage, and the curves under different sweep rates.

It is well known that the capacitive excess current is proportional to the scan rate; we showed that the inductive current is inversely proportional to the scan rate.

The application of the model provides a great degree of control over the kinetic properties of halide perovskite solar cells, including the amount and type of hysteresis that may be expected from the measurement of impedance spectroscopy at different voltages. By determining a few parameters in an impedance spectroscopy measurement it is now possible to predict the amount and type of

hysteresis that the perovskite solar cell device will have. Furthermore one can correlate the hysteresis response with the device materials properties via the impedance parameters that are obtained in the equivalent circuit. The general model can track a transformation of the low frequency capacitor into a chemical inductor, both related to ionic-controlled surface recombination process. The different kinetic properties are regulated by the variation of certain time constants that determine the dominant impedance response. This explains why the inductive feature may not produce a negative capacitance, so that hysteresis will remain regular in the whole voltage range.

6.6 Supporting Information

Impedance Spectra Fitting using General Model

All impedance spectra are fitted by non-linear least squares fitting using the general equivalent circuit model with the impedance function

$$Z(s) = R_s + \left[C_g s + \frac{1}{R_3 + Z_1} \right]^{-1} \quad (6.69)$$

where

$$Z_1 = \left[C_1 s + \frac{1}{R_1} + \frac{1}{Z_a} \right]^{-1} \quad (6.70)$$

$$Z_a = R_a + L_a s \quad (6.71)$$

$$s = i\omega \quad (6.72)$$

The equivalent circuit model incorporating a parallel shunt resistance R_{sh} is illustrated in Fig. 6.19 with the impedance function given by

$$Z(s) = R_s + \left[C_g s + \frac{1}{R_3 + Z_1} + \frac{1}{R_{sh}} \right]^{-1} \quad (6.73)$$

In order to consider the distortions in the semi-circles of the complex impedance spectral arcs, the exponents (n 's) are incorporated to the different $s = i\omega$ terms.

The fitted impedance function is now given by,

$$Z(s) = R_s + \left[C_g s^{nC_g} + \frac{1}{R_3 + Z_1} + \frac{1}{R_{sh}} \right]^{-1} \quad (6.74)$$

$$Z_1 = \left[C_1 s^{nC_1} + \frac{1}{R_1} + \frac{1}{Z_a} \right]^{-1} \quad (6.75)$$

$$Z_a = R_a + L_a s^{nL_a} \quad (6.76)$$

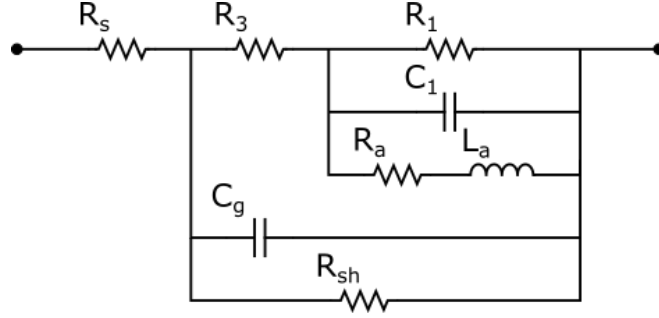


Figure 6.19: The schematic diagram of the general equivalent circuit model incorporating a parallel shunt resistance (R_{sh})

where n_{C_g} , n_{C_1} and n_{L_a} are the corresponding exponents to the capacitors C_g and C_1 , and the inductor L_a . The effective capacitance and inductance are then calculated with their corresponding resistor pairs by

$$C_{\text{eff}} = [R^{(1-n)}C]^{1/n} \quad (6.77)$$

and

$$L_{\text{eff}} = [R^{(1-n)}]^{1/n} L^n \quad (6.78)$$

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Chapter 7

Mechanistic and Kinetic Analysis of Perovskite Memristors with Buffer Layers: The Case of a Two-Step Set Process

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Extent of Contribution : 80%

The following tasks/activities are the author's contribution to this work:

- Design and fabrication of memristors with thin undoped buffer layers
- Electrical characterization of fabricated devices
- Analysis of characterization measurement data and results
- Model implementation and fitting of the impedance results
- Manuscript and response to reviewers' comments document preparation

Abstract

With the increasing demand for artificially intelligent hardware systems for brain-inspired in-memory and neuromorphic computing, understanding the underlying mechanisms in the resistive switching of memristor devices is of paramount importance. Here, we demonstrate a two-step resistive switching set process involving a complex interplay among mobile halide ions/vacancies (I^-/V_I^+) and silver

ions (Ag^+) in perovskite-based memristors with thin undoped buffer layers. The resistive switching involves an initial gradual increase in current associated with a drift-related halide migration within the perovskite bulk layer followed by an abrupt resistive switching associated with diffusion of mobile Ag^+ conductive filamentary formation. Furthermore, we develop a dynamical model that explains the characteristic $I - V$ curve that helps to untangle and quantify the switching regimes consistent with the experimental memristive response. This further insight into the two-step set process provides another degree of freedom in device design for versatile applications with varying levels of complexity.

7.1 Introduction

Artificially intelligent devices have been recently gaining considerable attention due to the increasing hardware demands of neural network configurations with varying levels of computational complexity [1–3]. Resistive random-access memory (ReRAM) based on memristor devices is widely considered as the most promising candidate for next-generation computational frameworks owing to their in-memory and neuromorphic computing capabilities [3–5]. This includes their simple device structure, high device density, low power consumption, fast switching speed, and monolithic integration compatibility with existing complementary metal/oxide/semiconductor (CMOS) systems [4, 6, 7]. Resistive switching has been demonstrated in a diverse range of devices from metal/oxide/metal structures [8–10], organic semiconductors [11–13], CMOS-compatible silicon-based devices [14–16], and numerous halide perovskite formulations [17–19].

Different neuromorphic computing schemes require specific switching properties from artificial neuromorphic hardware implementation. These characteristics range from non-volatile binary switching for digital in-memory computing and spiking neural networks [1, 3], to volatile analog switching for artificial neural network configurations and brain-inspired computing [4, 20–22]. The device application is intimately associated to the switching mechanism. In this respect, proposed resistive switching mechanisms range from drift-related non-filamentary oxygen vacancy migration and redistribution in metal and titanium oxide-based devices [23, 24], diffusive formation and rupture of metallic conductive filaments

in silicon oxide-based devices [15, 16], to halide filamentary formation followed by electrochemical interactions with contacts that promotes switching in perovskite-based devices [25, 26]. Despite the rapid development in material systems and configurations exhibiting distinct memristive switching properties, understanding of the precise mechanisms is essential in tailoring device design for a wider range of applications in more advanced computational frameworks.

Metal halide perovskite materials are versatile candidates for memory applications as they benefit from mixed ionic-electronic conduction due to ionic halide defect displacement resulting in intrinsic memory effects [27–29]. Metal halide perovskites are composed by the chemical structure ABX_3 , where A is a monovalent cation (i.e. $MA = CH_3NH_3^+$), B is a divalent cation (i.e. Pb^{2+}), and X is a halide anion (i.e. I^-). With the flexibility of the perovskite structure as the material platform, it possesses a broad range of switching physics suitable for a wide variety of neuromorphic computing architectures [30]. Perovskite-based memristive devices have been demonstrated to function as artificial synapses exhibiting essential synaptic behaviors for neuromuscular systems, pupil reflex, and for light-sensitive optogenetic applications [31–34]. Additionally, integration of two-dimensional structures [35, 36], mixed formulations [37, 38], and nanocrystals [21, 39] further increases the already vast degrees of freedom or state variables in perovskite-based memristors allowing tunability and versatility specific to the desired implementation. However, with the inclusion of various intermediate buffer [40, 41], a complete picture of the resistive switching mechanism is imperative to tailor design reliable memristive devices for more versatile applications.

Here, we present a two-step resistive switching (RS) SET process in methylammonium lead iodide ($MAPbI_3$) memristors with various thin undoped buffer layers. The $MAPbI_3$ perovskite formulation is selected in order to have a simple and well-established understanding of the electronic and ionic dynamics with low activation energy. The two different buffer layers used are (6,6)-phenyl C61 butyric acid methyl ester (PCBM), typically used as an electron selective layer [42], and the insulator poly(methyl methacrylate) (PMMA), typically used as a protective layer for the perovskite [43–45]. Based on the switching characteristics of the memristor devices, in conjunction with a direct comparison to a device configuration without a buffer layer, two distinct switching regimes are

untangled : (1) An initial gradual increase in current associated to drift-related I^- ion and V_I^+ defect migration and redistribution within the perovskite bulk layer followed by (2) an abrupt resistive switching associated to diffusion-related Ag^+ filamentary formation irrespective of the buffer layer. The two-step SET process exhibits both drift and diffusive mechanisms, depending on the applied field, allowing memristor device designs specifically tailored for targeted neural network configurations.

7.2 Results and Discussion

The cross-sectional SEM micrographs of the fabricated memristor devices with either PCBM or PMMA layers are shown in panels a and b of Fig. 7.1, respectively, with the device configuration indicating the layers. Both devices have $MAPbI_3$ perovskite layers with comparable thickness (~ 400 nm) and similar crystal morphology. The buffer layers are substantially thin with thicknesses ranging from ~ 5 -10 nm in order to have minimal voltage drop within these layers. The characteristic $I - V$ curves of a representative memristor device with the PCBM buffer layer is shown in Fig. 7.1c and RS activation and deactivation involves migration of I^-/V_I^+ and Ag^+ . The memristive response requires initial conditioning of the fresh device (electroforming process) at relatively high voltages which produces a significant change in the device conductance [46–50]. From the fresh state of the device, a positive voltage sweep is applied to promote the electroforming process (Fig. 7.1d). As the applied voltage approaches ~ 0.9 V, the current gradually increases and the continued voltage sweep abruptly increases the device current at ~ 1.45 V. A cutoff current of 50 mA is imposed to the measurement to avoid the irreversible processes that can lead to complete device breakdown. This cutoff current is reached at ~ 1.6 V where the scan direction is immediately reversed back to 0 V. Another scan towards positive bias reveals a new stabilized HRS. A positive voltage sweep gradually increases in current at a first threshold voltage of $V_{Th1} \sim 0.25$ V [SET1 process, (Table 7.1)], then abruptly switches ON to the LRS at a second threshold voltage of $V_{Th2} \sim 0.56$ V (SET2 process) with an ON/OFF ratio of ~ 21.3 . This two-step SET process indicates two distinct switching regimes at the different voltage ranges

as illustrated in Fig. 7.1d which will be discussed later in detail. The memristor device, then, stays at the LRS on the reverse scan direction and finally switches OFF to the HRS (RESET process) at $V_{\text{RESET}} \sim -0.59$ V. Once electroforming has taken place, the $I - V$ curve is stabilized and the curves of multiple cycles overlay as shown in Fig. 7.4. Both devices exhibit ON state retention times approaching 105 s at a read voltage of $V_{\text{read}} = 0.2$ V with endurance of > 50 cycles (Fig. 7.5), we note some performance degradation is observed during the initial 50 cycles. It is worth noting that the memristor device configuration is designed to emphasize the kinetics and dynamics of the resistive switching mechanism. Incorporation of large-size cation dopant, such as ethylenediammonium (en), has proved to substantially improve the device stability to record endurences of 1.2×10^4 cycles [30].

In order to investigate the effect of the buffer layer on the switching properties, the performance of memristors containing either PCBM or PMMA as buffer layers are compared with devices that contain no buffer layer. PCBM and PMMA are materials very different from the point of view of their electronic properties that will help to rule out any effects of energy level alignments that affect the charge extraction. Indeed, whilst PCBM is a semiconductor that is often used as an electron selective layer, the PMMA is an insulating material. The representative stabilized response of their memristors are shown in panels a and b of Fig. 7.2, respectively. Both memristors feature a resistive switching with the two-step SET process as described above with similar threshold values and current levels (Table 7.1). Therefore, effects related to energy level alignment at the perovskite interfaces do not appear to be related to the switching mechanisms and the resistive switching mechanism is of a different nature as explained below. The resistive switching with the SET and RESET processes occurring at opposite polarities of the applied voltage indicate a non-volatile bipolar resistive switching characteristic of the memristor device [40, 45, 51]. Alternatively, Fig. 7.2c shows the characteristic $I - V$ response of a memristor without any buffer layer and a non-reactive contact (MAPbI₃/Au). Interestingly, this device only exhibits the gradual SET1 process but without the abrupt SET2 process in the positive polarity. In addition, a gradual RESET process to the HRS in the reverse scan direction is observed. The SET and RESET processes occur in the same polarity

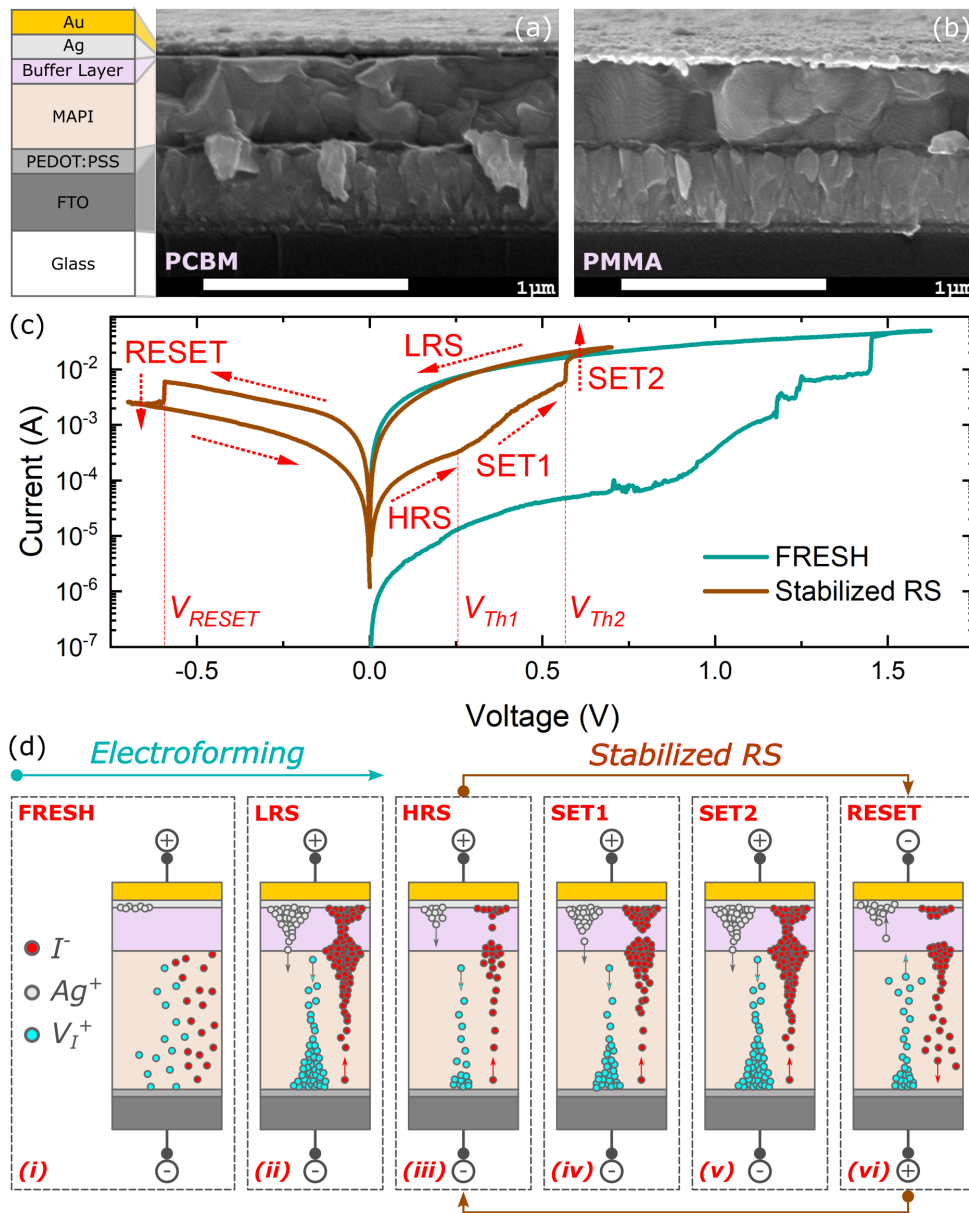


Figure 7.1: The cross-sectional SEM micrographs of memristors with thin undoped (a) PCBM and (b) PMMA buffer layers with schematic diagram of the device configuration. The (c) representative characteristic $I - V$ curves of the initial conditioning step of the FRESH device, and the stabilized two-step SET process and RESET process with the arrows indicating the scan direction. The (d) schematic diagram of the electroforming and two-step SET process mechanism under applied voltage of the memristive devices with buffer layers. The colors of the device configuration indicate the layers in the schematic diagram.

indicating that the device works as a volatile unipolar resistive switch [21, 51]. Therefore, a volatile memory device is transformed into a non-volatile device by addition of a buffer layer indicating that the buffer layer not only acts as a physical barrier to ions but also as a “pool” of ions that get trapped when the external electrical field is removed.

Table 7.1: Summary of the threshold voltages V_{Th1} , V_{Th2} and V_{RESET} corresponding to the SET1, SET2 and RESET processes respectively, with the ON/OFF ratios for all memristor devices.

Device	$V_{\text{Th1}}(\text{V})$	$V_{\text{Th2}}(\text{V})$	$V_{\text{RESET}}(\text{V})$	ON/OFF Ratio
PCBM	0.25	0.56	-0.59	21.3
PMMA	0.26	0.6	-0.59	39.3
MAPbI ₃ /Au	0.57	-	0.29	21

Regarding the activation mechanisms different authors have established that for devices that do not contain buffer layer and in the presence of non-reactive contact (i.e. Au), the gradual increase in current is attributed to the mobile I^+ ions migrating towards the Ag contact, consequently doping the intermediate buffer layer (Fig. 7.1d) [26, 27, 52, 53]. Correspondingly, the iodine vacancies (V_{I}^+) migrate towards the inert PEDOT:PSS leaving behind a doped perovskite material [25, 54]. In addition, the chemical interactions of migrating ions with the external contact can also lead to a reduction of the extraction barriers. Note that if the external contact is a reactive metal (i.e. Ag), a fast electrochemical reaction masks the memristive response as shown in the Fig. 7.6 for the MAPbI₃/Ag/Au interfaces. Alternatively, when buffer layers are used, we propose that the electroforming process at high applied voltages pushes the I^+ ions to cross the non-conductive buffer layer accumulating at the Ag contact leading to the formation of AgI (Fig. 7.1d) [25, 26]. The electrochemical reaction generates mobile Ag^+ ions which migrate toward the bottom contact under the influence of the applied field. Note that neutral Ag does not have a driving force to follow the electrical field. The migration and accumulation of mobile Ag^+ , I^- , and V_{I}^+ eventually switches the device abruptly to the low resistance state (LRS) or ON state. Once the applied voltage reaches back to 0 V, the mobile Ag^+ , I^+ and V_{I}^+ relax and a new stabilized high resistance state (HRS) or OFF

state is established. In addition, the thin Ag/Au contact is used to control and modulate the interactivity of the mobile I^- ions with Ag to prevent the formation of an excessively thick AgI structure with low ionic conductivity [55]. In general, the presence of the buffer layer in conjunction with the reactive Ag contact is responsible for the abrupt SET2 process by controlling the formation of a pool of slow moving ions within the buffer layer, the perovskite and by regulating the reactivity of migrating ions with Ag.

We next set to further analyze the characteristic $I - V$ response to understand if the kinetics of the SET processes can be correlated between different samples providing further insight on the mechanisms governing the switching processes. The SET process from the HRS to the LRS for all memristor devices are represented in the log-log scale as shown in Fig. 7.2b. At applied voltages $< V_{Th1}$, the memristor devices are in the HRS with the current exhibiting linear dependence to the applied voltage. Correspondingly, the calculated HRS slopes via piecewise linear fitting result to $m_{HRS} \sim 1$ for all memristor devices indicating an Ohmic conduction mechanism [45, 49, 56]. Beyond $< V_{Th1}$, the current gradually increases (SET1) with slopes of $m_{SET1} \sim 4.20$ and ~ 4.83 for the memristors with the PCBM, PMMA buffer layers, respectively. The m_{SET1} values > 1 are attributed to drift-related switching mechanism due to halide ion migration and redistribution within the perovskite material [57, 58]. Once the applied voltage reaches V_{Th2} , the memristor devices with buffer layers abruptly switch (SET2) to the LRS indicative of diffusion-related conductive filament formation across the buffer layer [22, 59–61]. In the reverse scan direction, the samples with the buffer layers maintain an Ohmic conduction response during the reverse scan with $m_{LRS} \sim 1$. On the other hand, the MAPbI₃/Au device exhibits an Ohmic HRS with a slope of $m_i \sim 0.98$ for applied voltages $< V_{Th1}$. As the applied voltage is further increased, the SET1 process exhibits a higher $m_{ii} \sim 12.78$. This higher m_{ii} of the MAPbI₃/Au could be attributed to the reduced series resistance of the devices, as compared to those with buffer layers. Thus, at a given applied external voltage, the electrical field present at the perovskite layer is higher than that of the devices with the buffer layers promoting a fast migration of ions and higher current injection. Once switched ON, the device then stays in the LRS with $m_{iii} \sim 2.66$ in the reverse scan direction followed by a gradual decrease in

current with $m_i v \sim 7.08$ and eventually switching the device OFF back to the Ohmic HRS with $m_v \sim 1.13$.

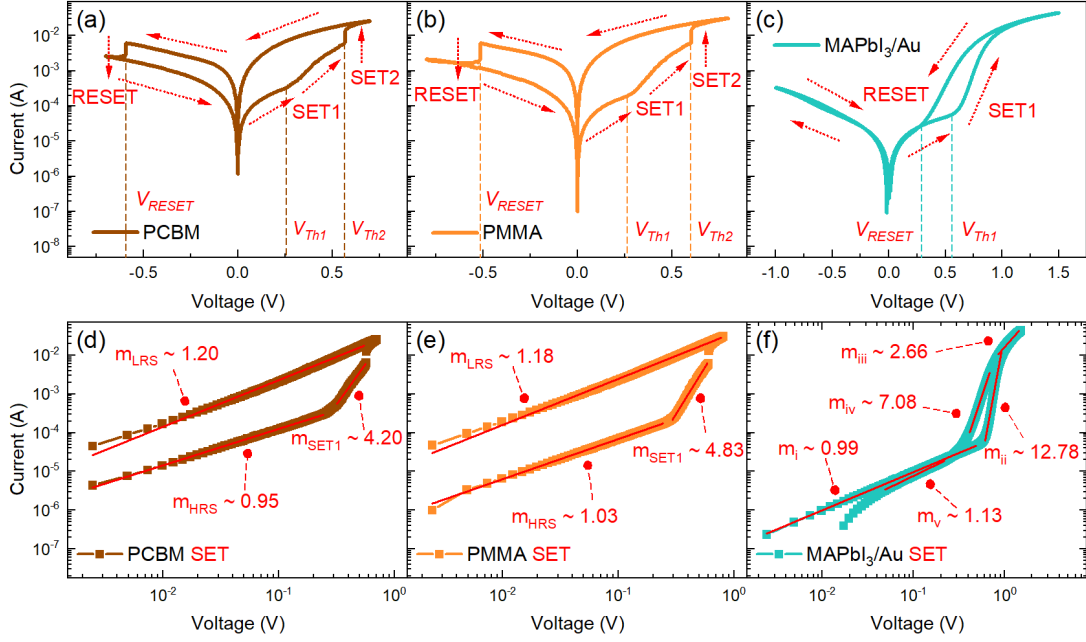


Figure 7.2: The characteristic $I - V$ curves in the semi-log scale of the memristor devices with thin undoped (a) PCBM and (b) PMMA buffer layers exhibiting non-volatile bipolar resistive switching, and the (c) MAPbI₃/Au device exhibiting volatile unipolar resistive switching. The arrows indicate the scan direction and the corresponding SET and RESET processes with their respective threshold voltages. The corresponding SET processes in the log-log scale of the (d) PCBM, (e) PMMA and (f) MAPbI₃/Au devices with the calculated slopes via piecewise linear fitting.

As the characteristic $I - V$ response of the memristor devices is carried out under dark and controlled conditions inside a glove box, the measurement protocol is identical to that of the space-charge limited conduction (SCLC) characterization [22, 45, 49, 62]. In SCLC analysis, the conduction mechanism at different voltage ranges is interpreted from the obtained slopes via a piecewise linear fitting. However, the SCLC characterization only considers the carrier transport and injection properties of the device. In lieu of the SCLC analysis, we present a dynamical model to elucidate the experimental observations and provide a clearer understanding of the complex features of the characteristic $I - V$ resistive switching response of the memristor devices with buffer layers. Our model takes into account interfacial reactions and charge accumulation and is not solely

based on carrier transport mechanisms. This general model lends an alternative analysis pathway to various approaches such as SCLC [22, 62], drift-diffusion simulations [16, 63], and SPICE modeling [64–67].

The dynamical model consists of a system of equations describing the characteristic $I - V$ response given by [68, 69],

$$I_{\text{tot}} = \frac{u}{R_b} + i_{c_1}f + i_{c_2}g + C_m \frac{du}{dt} \quad (7.1)$$

$$\tau_{k_1} \frac{df}{dt} = (1 - f) - e^{(u-V_{T_1})f/V_{m_1}} \quad (7.2)$$

$$\tau_{k_2} \frac{dg}{dt} = (1 - g) - e^{(u-V_{T_2})g/V_{m_2}} \quad (7.3)$$

The model considers four contributions for the extracted current (I_{tot}) under the applied electrical field. u/R_b is the Ohmic conduction response term with a constant resistance R_b . $i_{c_1}f$ is the gradual injection current term with a saturation value of i_{c_1} controlled by an occupation function f ($0 \leq f \leq 1$) associated to SET1 process, $i_{c_2}g$ is the subsequent current transition term with a saturation value of i_{c_2} controlled by a different occupation function g ($0 \leq g \leq 1$) associated to SET2 process, and the capacitive charging of the interfaces term with a capacitance C_m [68–70]. The four independent variables contribute to the total current I_{tot} , the applied voltage (u) and the occupation functions f and g . Both Eq. 7.2 and Eq. 7.3 represents the diffusion or migration time of ions introducing a delayed response that lags behind the applied voltage with characteristic times τ_{k_1} and τ_{k_2} , respectively. The delay equations are controlled by the onset potentials V_{T_1} and V_{T_2} , and ideality factors $m_1 = qV_{m_1}/(k_bT)$ and $m_2 = qV_{m_2}/(k_bT)$ for Eq. 7.2 and Eq. 7.3, respectively, where q is the electron charge, k_b is the Boltzmann constant and T is room temperature. Suppressing the time derivative, the steady state solutions become

$$f_{ss} = \frac{1}{1 + e^{-(u-V_{T_1})/V_{m_1}}} \quad (7.4)$$

$$g_{ss} = \frac{1}{1 + e^{-(u-V_{T_2})/V_{m_2}}} \quad (7.5)$$

Hence, the steady state current is, then, expressed as

$$I_{\text{tot}} = \frac{u}{R_b} + i_{c_1}f_{ss}(u) + i_{c_2}g_{ss}(u) \quad (7.6)$$

Implementing the dynamical model (Eq. 7.6) to the experimental results provides valuable information on the resistive switching of the memristor devices with buffer layers. The fitted SET process characteristic $I - V$ response of the memristor devices in the linear, semi-log, and log-log scales are presented in Fig. 7.3. The detailed fitting method is described in the Supporting Information to determine the relevant parameters as summarized in Table 7.2. The fitted curves capture the pertinent features of Ohmic LRS and the two-step SET process of the memristor devices from the linear to the log-log scales. From the extracted parameters of the fitting, the memristor devices have different R_b parameters. The R_b values can be attributed to the differences in buffer layer intrinsic resistivity and slight variations in layer thicknesses. In addition, the SET1 onset potential V_1 and the saturation current i_{c_1} of both the PCBM and PMMA devices have similar values. Moreover, both devices have comparable m_1 ideality factor values of ~ 2.6 and ~ 3.3 for the memristor with PCBM and PMMA buffer layer, respectively. These ideality factor values can be attributed to the slow and gradual migration and reaction of ions [18, 70] or the decrease in surface barrier at the perovskite/contact interface [70–72]. Similarly, the SET2 onset potential V_2 and the saturation current i_{c_2} of both the PCBM and PMMA devices also have similar values. Notably, the ideality factors m_2 of the memristor devices are significantly lower than their corresponding m_1 with values of ~ 0.01 and ~ 0.03 for the devices with the PCBM and PMMA buffer layers, respectively. The lower m_2 values capture the abrupt resistive switching and the continued current increase after the SET process suggesting that the conductive filamentary formation is an avalanche effect. The high correlation of the fitted SET1 parameters indicates that the mechanism during the gradual current increase is general in both devices regardless of the type of buffer layer. On the other hand, the differences in and m_2 parameters suggest that the avalanche SET2 process is affected by the slight variations in intrinsic properties and layer thicknesses of the buffer layers.

Based on these results, a two-step resistive switching SET process is proposed involving the complex interplay among mobile Ag^+ , I^- and V_I^+ as schematically presented in Fig. 7.1d. At the initial device state (FRESH state), (i) the mobile I^- ions and V_I^+ defects are uniformly distributed throughout the perovskite bulk

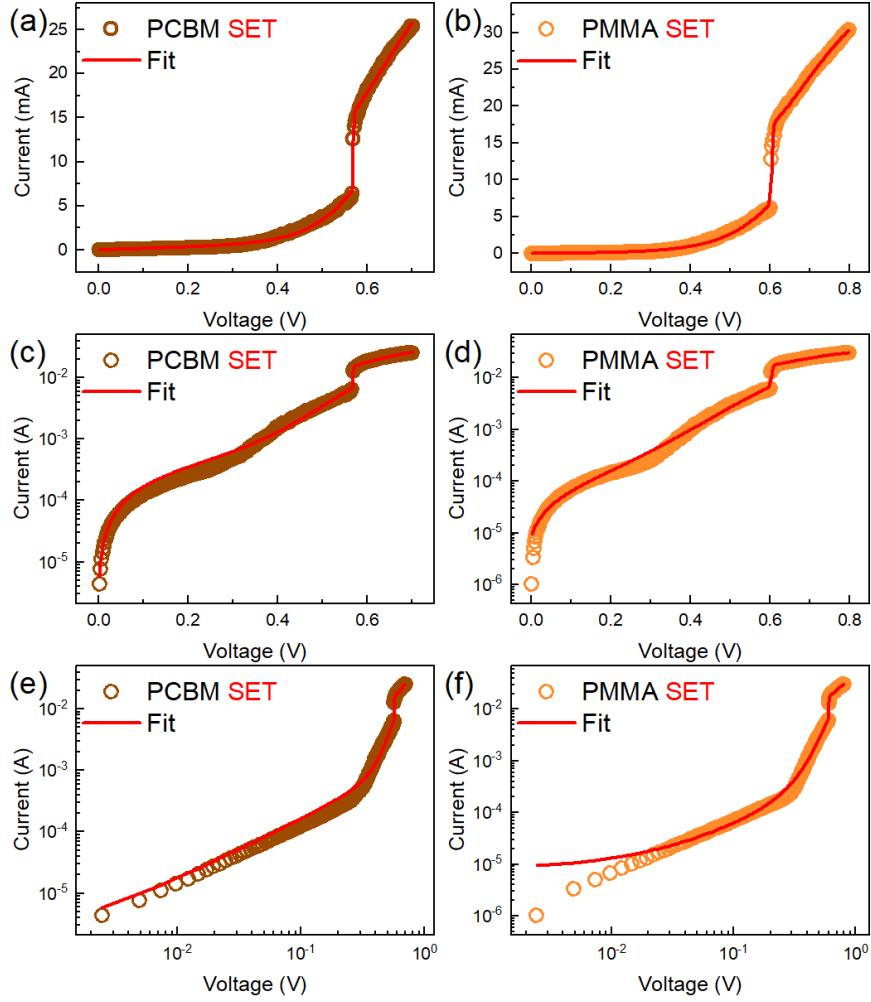


Figure 7.3: The characteristic $I - V$ SET process with the corresponding fitted curves using the dynamical model for both memristor devices in the (a-b) linear, (c-d) semi-log, and (e-f) log-log scales.

Table 7.2: Summary of the fitted parameters with the corresponding ideality factor m given by $V_m = mk_bT/q$ using the dynamical model for all memristor devices.

Device	R_b (Ω)	V_{T_1} (V)	V_{m_1} (V)	m_1	i_{c_1} (A)
PCBM	6.39×10^2	6.36×10^{-1}	6.81×10^{-2}	2.619	2.22×10^{-2}
PMMA	2.77×10^3	6.92×10^{-1}	8.65×10^{-2}	3.327	2.53×10^{-2}

Device	V_{T_2} (V)	V_{m_2} (V)	m_2	i_{c_2} (A)
PCBM	5.69×10^{-1}	5.77×10^{-4}	0.01	8.69×10^{-3}
PMMA	6.04×10^{-1}	1.89×10^{-3}	0.032	1.05×10^{-2}

layer. During the electroforming process, migrating I^- ions and V_I^+ defects accumulate at the top and bottom contacts, respectively, (ii) switching the device to the LRS. The implemented cutoff current avoids the device breakdown and the irreversible conductive filamentary formation which can permanently switch the device in the LRS state. The immediate reverse scan direction back to 0 V relaxes the ion and defect migration resulting to the rupture of conductive filaments and (iii) maintaining a stabilized HRS lower than that of the equilibrium FRESH state. From the new lower stabilized HRS with an Ohmic resistance R_b , a positive scan allows mobile I^- ions to migrate towards the Ag contact consequently doping the intermediate buffer layer [26, 52]. Correspondingly, the V_I^+ defects migrate towards the inert PEDOT:PSS and FTO bottom contacts [25, 54]. As the device is already at a less resistive HRS, a lower applied voltage (V_{Th1}) is required for the migrating I^- ions and V_I^+ defects to accumulate at the contacts, (iv) gradually switching the resistance state of the device (SET1). Subsequently, the accumulated I^- ions promote the oxidation reaction of the Ag contact resulting to the formation of AgI layer at the contact interface allowing activated Ag ions to migrate towards the bottom contact through the buffer layer [25, 41, 52]. The combination of the activated migrating ions and defects at a specific applied voltage (V_{Th2}) favor the conductive filamentary formation through the buffer layers (v) abruptly switching the device to the LRS (SET2). The memristor devices, then, stays in the LRS in the reverse scan direction necessitating a negative V_{RESET} (vi) to stably rupture the conductive filaments and to return back to the stabilized HRS. It is noted that the RESET process does not exhibit the two-step process. As observed in the two-step SET process, the diffusion of the migrating I^- and V_I^+ (SET1) occurs prior to the formation of the Ag^+ conductive filaments (SET2). Hence, during the reverse scan towards the negative voltages, the migrating I^- ions and V_I^+ defects already approach their relaxed state prior to the complete rupture of the conductive Ag^+ filaments. Therefore, the single step RESET process can be attributed to the difference in the time scales between the faster diffusion of ions and defects and the slower diffusion of the Ag ions.

7.3 Conclusion

In summary, we have demonstrated that a two-step resistive switching SET can be induced by the introduction of a buffer layer between the perovskite and the top contact. This additional layer turns a device that shows volatile memory response into a non-volatile memory. The buffer layer in conjunction with the reactive Ag contact is responsible for the abrupt SET2 process by controlling the formation of a “pool” of slow moving ions within the buffer layer, the perovskite and by regulating the reactivity of migrating ions with Ag. Furthermore, we present a dynamical model which distinctly describes the two different switching mechanism regimes indicated by the extracted ideality factors. The experiments reveal that the current control is due to accumulated charges and interfacial reactions. Moreover, the high correlation of the model parameters suggests that the two-step SET process is governed by the same mechanism irrespective of the buffer layer. This insight on the mechanisms governing the switching response would be relevant for memristor configurations specifically tailored for targeted neural network configurations with varying levels of complexity. These devices exhibit both drift and diffusive switching responses can be utilized for adaptable implementation of versatile device designs in more diverse computational frameworks.

7.4 Methods

The fabricated memristor device configuration consists of a fluorine-doped tin oxide (FTO) / poly (3,4-ethylenedioxythiophene) polystyrene sulfonate (PEDOT:PSS) / MAPbI₃ / buffer layer / Ag / Au. The two different buffer layers used are (6,6)-phenyl C61 butyric acid methyl ester (PCBM) and poly(methyl methacrylate) (PMMA). The thin buffer layers are prepared by spin coating without any additional dopants and with similar thicknesses. The fabrication method is further discussed in detail in the Supporting Information.

The film morphology of the memristor devices is inspected via cross-sectional scanning electron microscopy (SEM) (JEOL JSM-7001F). The electrical characterizations of the memristor devices are measured inside a nitrogen-controlled glove box under dark conditions using an Autolab PGSTAT204 potentiostat to

minimize moisture-related degradation effects and to improve reproducibility.

The electroforming step is initiated via a voltage sweep from $0\text{ V} \rightarrow 2.5\text{ V} \rightarrow 0\text{ V}$ with a cutoff current of 50 mA , which immediately reverses the scan direction once reached to avoid complete device breakdown. Instead of a current compliance, which limits the maximum operating current but continues the voltage scan direction, the cutoff current is implemented in order to observe the full switching response without loss of information. The characteristic $I - V$ response of the devices are then measured via a voltage sweep from $0\text{ V} \rightarrow +V_u \rightarrow -V_l \rightarrow 0\text{ V}$, where the upper (V_u) and lower (V_l) voltage vertices are selected for stable, reproducible resistive switching from a HRS or OFF state to a LRS or ON state.

7.5 Supporting Information

Memristor Device Fabrication

Substrate Preparation

The fluorine-doped tin oxide (FTO) substrates were partially etched with zinc powder and 2 M HCl solution. The etched samples were individually brushed to mechanically remove the remaining residues of the etching procedure, then, were sonicated for 15 minutes each in deionized water with Hellmanex detergent solution, acetone, and isopropyl alcohol, respectively. The cleaned substrates were then dried using a nitrogen gun.

PEDOT:PSS Deposition

Prior to the deposition of the PEDOT:PSS layer, the etched and cleaned FTO substrates were subjected to a 15 min-ultraviolet ozone treatment to further remove organic contamination on the surface and improve surface wetting. The PEDOT:PSS (Heraeus Clevis P VP Al 4083) solution was filtered using a $0.45\text{ }\mu\text{m}$ PTFE syringe filter before injection onto the substrate surface. The PEDOT:PSS was, then, spin-coated on the FTO substrates at 3000 RPM with an acceleration of 1000 RPM/s for 30 s . The spin-coated samples were heated at $100\text{ }^\circ\text{C}$ for 5 mins then were immediately transferred into the nitrogen-controlled glovebox.

MAPbI₃ Deposition

The FTO substrates with the PEDOT:PSS layer were subjected to dehydration inside the glove box at 100 °C for 10 minutes to further remove humidity during transport. . A 1.4 M MAPbI₃ precursor solution is prepared using PbI₂ (>98 %, TCI) and MAI (>99.99 %, Greatcell Solar) in 95 μ L:1 mL dimethylsulfoxide (DMSO) (\geq 99.9 %, Sigma Aldrich):N,N-dimethylformamide (DMF) (99.8 %, Sigma Aldrich) solution. A 50 μ L MAPBr perovskite solution was statically spin-coated onto the PEDOT:PSS layer via an anti-solvent method of 4000 RPM with 1000 RPM/s acceleration for 50 s. A 500 μ L chlorobenzene (99.8 %, Sigma Aldrich) anti-solvent was injected 8 seconds after the spin coating has started. The samples were then annealed at 100 °C for 10 minutes.

Thin Undoped Buffer Layer Deposition

The buffer layers consist of a 10 mg/mL (6,6)-Phenyl C61 butyric acid methyl ester (PCBM); an electron selective layer, and a 5 mg/mL Poly(methyl methacrylate) (PMMA); an insulating polymer. The buffer layer solutions are prepared in 1 mL chlorobenzene without any additional dopants. A 50 μ L undoped buffer solution was dynamically spin-coated at 6000 RPM with 800 RPM/s acceleration for 30 s.

Metal Contact Deposition

Finally, a 15 nm Ag contact, followed by an 85 nm Au contact was thermally evaporated using a commercial Oerlikon Leybold Univex 250.

Stabilized Characteristic $I - V$ Switching Response

The stabilized characteristic $I - V$ response of the PCBM and PMMA devices are shown in Fig. 7.4.

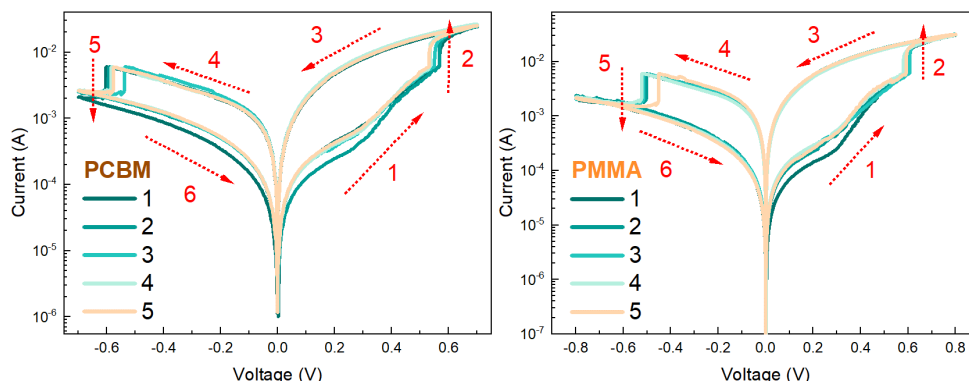


Figure 7.4: The representative stabilized characteristic $I - V$ switching response of the memristor devices with thin undoped (a) PCBM and (b) PMMA. The upper (V_u) and lower (V_l) voltage vertices are specifically selected for the devices to exhibit stable and reproducible resistive switching.

ON State Retention and Endurance Measurements

The ON state retention time and endurance measurements of the PCBM and PMMA devices are shown in Fig. 7.5.

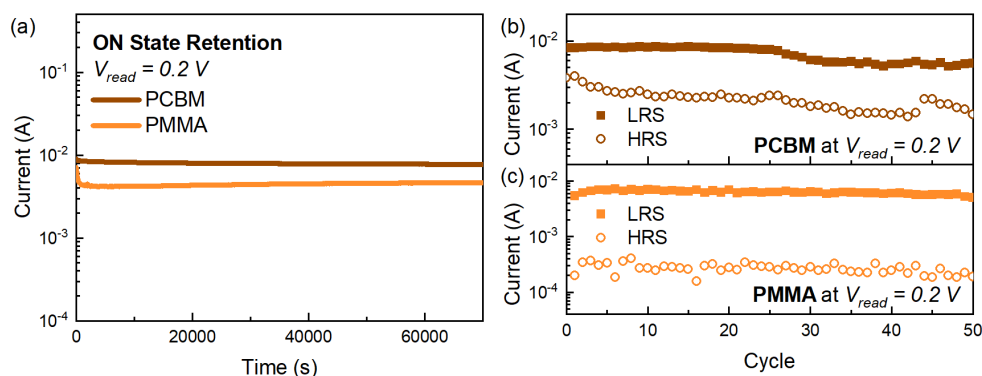


Figure 7.5: (a) The ON state retention times of both the PCBM and PMMA memristors by a SET voltage pulse of $V_{SET} = 1.5$ V for 5 s to switch the device to the ON state then subsequently measured at a read voltage of $V_{read} = 0.2$ V. Endurance measurements of the HRS (OFF state) and LRS (ON state) during cyclic voltammetry consecutive cycling for both the (b) PCBM and (c) PMMA devices measured at the same read voltage of $V_{read} = 0.2$ V.

Redox Reaction of MAPbI₃/Ag/Au Device

The characteristic $I - V$ response of a memristors without any thin undoped buffer layer is investigated as shown in Fig. 7.6. In the semi-log scale (Fig. 7.6a), the characteristic $I - V$ response of the device without the buffer layer (MAPbI₃/Ag/Au) does not exhibit a memristor resistive switching. Instead, a reduction-oxidation (redox) of Ag and I resulting to the formation and rupture of AgI at the perovskite/Ag interface is observed in the positive and negative polarities, respectively [15, 21, 48]. In the log-log scale, the MAPbI₃/Ag/Au memristor device (Fig. 7.6b) also initially exhibits an Ohmic conduction with $m_i \sim 0.93$ for applied voltages below the onset of current increase of ~ 0.21 V. Moreover, the slopes of the subsequent voltage ranges (m_{ii} to m_v) calculated via a piecewise linear fitting vary from ~ 0.73 up to ~ 7.27 . The low correlation of the slopes beyond the onset of current increase of the memristor without a buffer layer compared to the devices with varying buffer layers suggests that the abrupt resistive switching is intimately correlated to the filamentary formation occurring within the buffer layers [41]. Furthermore, the applied voltage range ($V_{\text{app}} < 0.8$ V) for memristor devices with the various thin undoped buffer layers has been reported to be insufficient to promote metal ion migration towards the perovskite bulk layer further confirming the filamentary conduction within the buffer layers [26, 52].

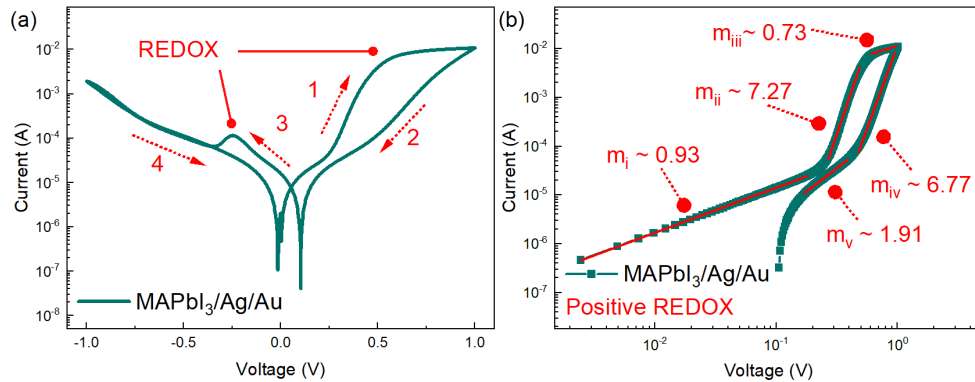


Figure 7.6: (a) The characteristic $I - V$ curve of the memristor device with no buffer layer in semi-log scale exhibiting a reduction-oxidation (redox) process instead of a memristive switching response with the arrows indicating the scan direction. (b) The corresponding positive scan redox in the log-log scale with the calculated slopes via piecewise linear fitting.

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Chapter 8

Conclusions and Future Outlook

8.1 Summary and Conclusions

In summary, we have demonstrated the current-voltage ($I - V$) hysteresis control in perovskite-based solar cells and memristors via sets of experimental designs with varying device configurations. Complementarily, the distinct state transitions are systematically investigated using a newly established impedance spectroscopy (IS) measurement protocol, together with the formulation of dynamical models correlating the $I - V$ measurements with the IS response, unravelling the underlying mechanisms governing the hysteresis under device operation. The understanding and control of the hysteresis effect in perovskite-based devices are achieved by the culmination of the following individual achievements:

- I. We have demonstrated the resistive switching in a 2D Ruddlesden-Popper perovskite-based memristors by utilizing the interfacial reactivity resulting to the formation and dissolution of AgI layer in order to control and modulate the gradual resistance state transition. We have developed a chronoamperometry (CA)-IS measurement protocol to track the device evolution during the state transition correlating the IS response from the corresponding $I - V$ curve. A transformation of the low frequency capacitive arc to a negative capacitance/inductive arc has been observed and validated. This inductive feature is intimately correlated to the ion migration redistribution promoting the formation and dissolution of AgI layer at the perovskite/Ag interface. Moreover, the incorporation of a thin undoped Spiro-OMeTAD buffer layer before the Ag contact exhibits an abrupt state transition in-

dicating the formation of conductive filaments localized within the buffer layer.

- II. We have developed a method to correlate the time domain $I - V$ response to the frequency domain IS response after having validated the appearance of the negative capacitance/inductive feature in the voltage-dependent CA-IS measurement protocol of perovskite solar cells. This method involves the conversion of the equivalent circuit model into a set of differential equations with internal state variables, which is then integrated with the appropriate voltage-dependence given a linear voltage sweep. From this integration theory, we have demonstrated quantitatively a vital insight consistent with experimental results – normal hysteresis corresponds to a capacitive effect, while inverted hysteresis corresponds to an inductive effect. Moreover, we have demonstrated a new phenomenon of a voltage-dependent transformation from low frequency capacitive to inductive features consistent with the hysteresis in perovskite solar cells similarly observed in memristors.
- III. We have formulated a general dynamical model for perovskite solar cells exhibiting the transformation from capacitive to inductive hysteresis, both in the scan rate-dependent $I - V$ curves and the voltage-dependent IS response, using neuronal models describing memristive systems and the recently established chemical inductor. With the general insight from the integration theory, in conjunction with the chemical inductor model, we have shown that there is a specific voltage (crossing point) where the hysteresis transition from normal to inverted. Consistently, the IS low frequency response transitions from capacitive to inductive as observed experimentally. Using the general dynamical model, the pertinent extracted parameters indicate that the low frequency capacitor and inductor are not completely independent processes, rather, they correspond to a similar ionic transport mechanism at the interface.
- IV. Finally, we have demonstrated hysteresis control in perovskite-based memristors exhibiting a two-step resistive switching SET process by using thin intermediate buffer layers with the insight of the dynamic ionic transport and interfacial reactivity mechanisms during the device state transitions.

The incorporation of the buffer and Ag layers transforms the volatile threshold switching to nonvolatile bipolar switching mechanism. Moreover, we have developed a dynamical model of the two-step SET process that untangles the switching regimes – low voltage volatile drift-related switching, then a higher voltage non-volatile diffusion-related switching.

These individual achievements have ultimately culminated in a more complete picture of the complex ionic transport dynamics governing the hysteresis effect in perovskite-based devices. This involves the complex interplay among the migrating ions, vacancies, activated metals, and interfacial reactivity depending on the device configuration. With a better understanding of the underlying mechanisms in the dynamic ionic and electronic transport in perovskite-based devices, hysteresis response is controlled by precise device configuration designs specifically tailored for the targeted optoelectronic application – highly stable perovskite based solar cells, and memristor implementation as artificially-intelligent hardware in reconfigurable and more complex neuromorphic computing frameworks.

8.2 Future Outlook

As the complex interplay of the dynamic ionic transport in perovskite-based devices addressed throughout this thesis is getting more understood, the device designs can be tailored for specific optoelectronic applications. It should be noted that the device configurations in this work are designed specifically to understand the underlying mechanisms governing the device operation. In order to fully impact the advancement of perovskite-based devices in photovoltaic and neuromorphic computing applications, experimental designs specific to more complex and promising systems are necessary to systematically gauge the viability of the perovskite-based devices for commercialization. This entails dedicated future work that is broadly classified as (i) material, (ii) device configuration, and (iii) implementation opportunities.

Material Opportunities

With the perovskite material possessing a vast compositional space, opportunities for the systematic investigation of the different formulations can be further

explored. This includes the mixed cation and halide formulations, various 2D Ruddlesden-Popper and Dion-Jacobson perovskites with varying levels of dimensionality, integration of 2D/3D perovskite architectures, graded heterojunctions, lead-free formulations, and incorporation of nanostructures such as nanocrystals and quantum dots. For PSCs, the hysteresis effect of these more complex perovskite formulations exhibiting record efficiencies and stabilities can be further investigated and improved. For memristors on the other hand, the switching physics and mechanisms with more complex ionic transport can be further studied for higher precision control of the memristive response.

Device Configuration Opportunities

In addition to the compositional space of the active material, the device performance for both photovoltaic and memory applications is controlled via architecture and interface engineering. The architecture engineering entails the selection of the top and bottom electrodes ranging from different metals with varying levels of reactivity to the use of carbon-based contacts. On the other hand, the interfacial engineering entails the selection of proper transport layers with suitable energy levels for highly efficient charge extraction in PSCs, and the incorporation of buffer layers at the contact interfaces to modulate interfacial reactivity in memristors. Moreover, three-terminal memristor device configurations have also been demonstrated as promising candidates in in-memory computing applications. The control of the memristive response in these newly emerging memory technologies requires a more in-depth investigation with the insight of the complex ionic transport dynamics in two-terminal devices.

Device Implementation Opportunities

Since the focus of this thesis is mainly on the individual lab-scale device-level investigation of the electronic and ionic transport dynamics, systematic studies of the device implementation in their pertinent applications offer a wider scope of research in the hysteresis control. For PSCs, the incorporation of perovskites in high efficiency tandem solar cells with the more established crystalline silicon platform brings about a more complex system in terms of electronic and ionic transport dynamics. This monolithic integration of tandem solar cells would be

more readily be implemented for large-scale devices towards commercialization. On the other hand, the downscaling of the memristor devices for practical implementation and demonstration for in-memory computing networks as cross-bar arrays offers a branch of research linking the device-level physics with the computational algorithm schemes. Moreover, neuromorphic implementation of these versatile memory devices in synaptic neural network configurations that require both volatile and nonvolatile switching modes would further highlight the impact of these unique devices in modern computing architectures. This connection between the two branches of research bridges the gap for a more concerted effort in designing computational frameworks taking full advantage of the versatile device memristive response.