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NANOSCALE CHARACTERIZATION AND SIMULATION OF ADVANCED CMOS AND EMERGING DEVICES VARIABILITY

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A thesis submitted in fulfillment of the requirements for the degree of Doctor of Philosophy in Electrical and Telecommunication Engineering

in the

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The undersigned, Dr. Marc Porti Pujal, Associate Professor of the Electronic Engineering Department (Engineering School) of the *Universitat Autònoma de Barcelona*

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that the thesis entitled "*Nanoscale characterization and simulation of advanced CMOS and emerging devices variability*" has been written by the PhD candidate **Ana Ruiz Flores** under his supervision, in fulfillment of the requirements for the PhD degree in Electrical and Telecommunication Engineering.

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Bellaterra (Barcelona), September 2022

In the middle of difficulty lies opportunity.

Albert Einstein

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- ⋆ A. Ruiz, N. Seoane, S. Claramunt, A. Garcia-Loureiro, M. Porti, C. Couso, J. Martin-Martinez, M. Nafría, "Workfunction fluctuations in polycrystalline TiN observed with KPFM and their impact on MOSFETs variability", *Appl. Phys. Lett.* 114, 093502 (2019).

- ⋆ A. Ruiz, N. Seoane, S. Claramunt, A. García-Loureiro, M. Porti, M. Nafría, "Combined nanoscale KPFM characterization and device simulation for the evaluation of the MOSFET variability related to metal gate workfunction fluctuations", *Microelectronic Engineering*, 216, 111048 (2019).

- ⋆ A. Ruiz, S. Claramunt, A. Crespo-Yepes, M. Porti, M. Nafría, H. Xu, C. Liu, Q. Wu, "Exploiting the KPFM capabilities to analyze at the nanoscale the impact of electrical stresses on OTFTs properties", *Solid-State Electronics*, Volume 186, 108061 (2021).

- ⋆ A. Ruiz, C. Couso, N. Seoane, M. Porti, A.J. García-Loureiro, M. Nafría, "Methodology for the simulation of the variability of MOSFETs with polycrystalline high-k dielectrics using CAFM input data", *IEEE Access*, Volume 9, pp. 90568 – 90576 (2021).

Contributions to conferences

- ⋆ S. Claramunt, Q. Wu, A. Ruiz, M. Porti, C. Couso, M. Nafría, X. Aymerich, "Nanoscale electrical characterization of a varistor-like device fabricated with oxidized CVD graphene," in 2017 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS), 2017, pp. 216–219.

- ⋆ S. Claramunt, Q. Wu, A. Ruiz, M. Porti, M. Nafría, X. Aymerich, "Role of

graphene as interfacial layer in RRAM devices," in th 12th Spanish Conference on Electron Devices, November 14-16, 2018.

- A. Ruiz, N. Seoane, S. Claramunt, A. García-Loureiro, M. Porti, M. Nafría, "Combined nanoscale KPFM characterization and device simulation for the evaluation of the MOSFET variability related to metal gate workfunction fluctuations," in the 21th Conference on Insulating Films On Semiconductors, July 1-3, 2019.

- S. Claramunt, A. Ruiz, Q. Wu, M. Porti, M. Nafría, X. Aymerich, "MIS structures with interfacial graphene for ReRAM applications: a nanoscale and device level characterization," in the International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS), 2020.

- A. Ruiz, N. Seoane, S. Claramunt, A. García-Loureiro, M. Porti, M. Nafría, "Analysis of metal gate workfunction fluctuations on MOSFETs variability uring KPFM characterization and device simulation tools," in the 13th Spanish Conference on Electron Devices, June 9-11, 2021.

- A. Ruiz, S. Claramunt, A. Crespo-Yepes, M. Porti, M. Nafría, H. Xu, C. Liu, Q. Wu, "Exploiting the KPFM capabilities to analyze at the nanoscale the impact of electrical stresses on OTFTs properties," in the 22th Conference on Insulating Films On Semiconductors, June 28- July 2, 2021.

Preface

During the last decades, electronic devices have become essential for our society and can be found around us in all aspects of our daily life. A paradigmatic exponent of this is the Internet of Things (IoT), which ranges from smart appliances in our houses to healthcare applications and devices. Indeed, this has been possible thanks to the technological advance in fabrication techniques; which has allowed, following the trend of Moore's Law, for higher integration levels. This last has led to the development of several devices and/or technologies (e.g.: smartphones, virtual reality, supercomputers...), which has changed our way of life all around the world and has led humanity to levels of comfort that were unimaginable a few decades ago. Nonetheless, the requirement of even higher integration levels to keep up with the Moore's is pushing the current technology to its fundamental limit, i.e. the atomic size. It is in that context, that to save Moore's law, besides the continuous scaling of MOSFETs dimensions, new structures and materials (as emerging devices) are being explored, as those based on graphene and/or organic materials. However, the variability found in these devices and reliability issues have become increasingly important with each technological node and, specially, with emerging devices. Finally, it is important to remark that variability sources and aging mechanisms are usually related to nanoscale properties of the materials, thus requiring nanoscale tools for their analysis as Atomic Force Microscopy (AFM) related techniques.

This thesis is focused on this topic. We have developed/improved different setups and/or methodologies to correlated nanoscale (observed with AFM related techniques) variability sources or aging mechanisms with their impact on device level characteristics of the corresponding devices. In particular, they have been applied to MOSFETs and emerging devices as graphene-FETs and Organic TFT.

The Thesis is structured as follows; Chapter 1 presents the fundamental concepts to understand the results presented in the thesis, In Chapter 2, we present in detail the advanced characterization techniques used throughout this thesis, such as Kelvin Prove Force microscopy (KPFM) and Conductive Atomic Force Microscopy (CAFM), used to obtain nanoscale information. Chapter 3 is devoted to the evalua-

tion of the effect of the polycrystallinity of gate metals and high-k dielectrics on the MOSFETs variability, by combining experimental data obtained at the nanoscale with CAFM and KPFM and simulations. In Chapter 4, we present a new smart and flexible experimental set-up that combines device level and nanoscale measurements on fully processed devices, by using a Semiconductor Parameter Analyzer and CAFM, which applies to evaluate at the nanoscale and at device level the effects of an electrical stress in graphene based transistors. Finally, in Chapter 5 we present a KPFM and device level study of the impact of electrical stress on the properties of the OTFTs.

1 Introduction

THE microelectronic field was born in the middle of the 20th century. Although Julius Edgar Lilienfeld theoretically devised the field effect transistor or FET in 1925 [1], the first (bipolar) transistor was not manufactured until 1947 by Walter Houser Brattain, John Bardeen and William Shockley, for which they received the Nobel Prize in Physics in 1956. The metal-oxide-semiconductor field effect transistor (MOSFET) was invented in 1960 as a breakthrough and upgrade of the FET transistor, by Dawon Kahng and Martin M. (John) Atalla [2], opening the door for its use in integrated circuits. Since the appearance of the first integrated circuits, it has been possible to increase the integration density of the devices thanks to the scalability of this type of transistor, which has undergone a progressive reduction of its dimensions. This scaling was also predicted by Gordon E. Moore with the well known Moore's law [3]. Thus, nowadays, MOSFET is the most widely used semiconductor device and is present in every digital circuit. However, the continuous reduction of MOSFETs dimensions has led to the appearance of important challenges that have been and are still the focus of an important research in the field of micro and nanoelectronics.

This chapter will give a general overview of the fundamental concepts that are necessary for understanding the rest of the manuscript. Firstly, the basics of MOSFET devices and how these devices have evolved by introducing different materials (metal gate, high-k dielectric, III-V semiconductor) is introduced. Then, due to the fact that the MOSFET is reaching the scaling limit, alternative architectures such as

graphene-based transistors (GFETs) and OTFTs are proposed. In all cases, reliability and variability issues are critical, so they will be introduced in this chapter.

Finally, since most of the experiments presented in this thesis have been performed with AFM related techniques, they will be presented. In particular, how they have contributed to the development of nanoelectronics has been introduced.

1.1 MOSFET device

The fundamental part of the MOSFET is the capacitive MOS structure. It consists of two electrodes with a layer of insulating material between them. Initially SiO_2 was used, but nowadays, high-k dielectrics [4], which allow to reduce the leakage current due to tunnelling are considered. One of the electrodes is called gate and can be made of metal or highly doped polysilicon, while the other electrode is the substrate terminal, called Bulk, and is made of a semiconductor material, usually silicon (Si). The silicon substrate can be dopped with P or N impurities, leading to p-type or n-type MOS structures. Figure 1.1 shows the structure of a MOS capacitor.

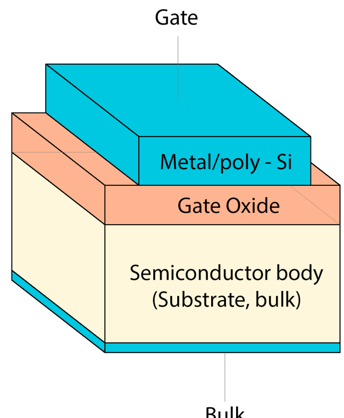


Figure 1.1: Schematic of a MOS structure.

Based on the MOS structure and adding two highly doped regions with opposite impurities to the substrate, the MOSFET device is obtained. The terminals con-

nected to these regions are called drain and source, having a total of 4 terminals together with the gate and substrate. Figure 1.2 shows the structure of the MOSFET with its four terminals called gate (G), drain (D), source (S) and substrate (B), in which the current that flows between drain and source is controlled by the voltage applied to the gate.

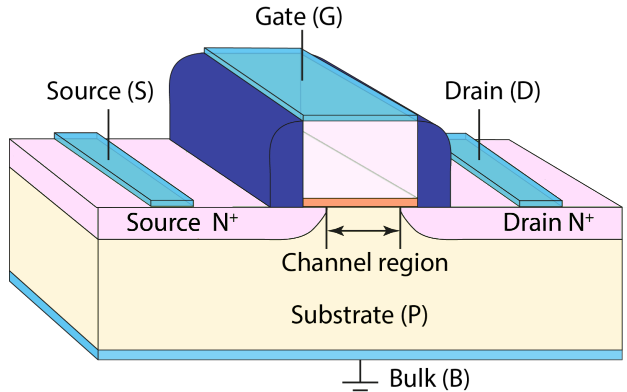


Figure 1.2: Scheme of a n-type MOSFET device.

1.1.1 Electrical characteristics of a MOSFET

The MOS capacitance has three different modes of operation depending on the voltage applied between the gate and the substrate. Figure 1.3 shows the ideal energy band diagram of a MOS capacity with an n-type substrate. One of the modes of operation is called accumulation, which occurs when a positive voltage is applied to the metal gate leaving the substrate terminal to ground ($V_{GB} > 0$), so that a large number of electrons are attracted to the semiconductor-oxide interface (that's why it is called accumulation). Figure 1.3(a) shows how the Fermi level drops, causing the conduction band to bend and the accumulation of the majority carriers in the conduction band of the semiconductor.

Another mode of operation is called depletion, which occurs when a negative voltage is applied to the gate contact ($V_{GB} < 0$), so that the electrons that are close to the semiconductor-oxide interface are repelled, depleting the semiconductor below

the oxide. Therefore, as shown in Fig. 1.3(b), the charge remaining in the depletion region is positive.

The last mode of operation is known as inversion. In this case, a higher negative voltage is applied to the gate, which causes the concentration of electrons near the surface to decrease even more, so the concentration of holes increases in the inversion region as shown in Fig. 1.3(c). In this situation, it is said that a channel between the drain and the source has been formed. Since the channel is formed with positive charges (holes), the transistors are called PMOSFETs. In a MOS capacitor with p-type substrate, the operation modes are the same but with opposite polarities. In this case, the transistor is a NMOSFET.

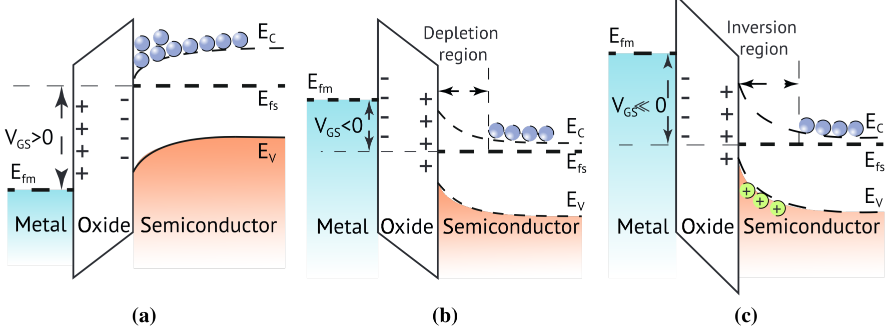


Figure 1.3: Energy-band diagrams of an ideal MOS capacitor: (a) accumulation, (b) depletion and (c) inversion.

It is worth commenting that we are considering the ideal MOS structure, in which the semiconductor and metal workfunctions are equal, and the MOS capacitance is

$$C_{ox} = \frac{Ak\epsilon_0}{t_{ox}} \tag{1.1}$$

where A is the area of the capacitor, k represents the relative permittivity of the dielectric, ϵ_0 the permittivity of vacuum and t_{ox} is the oxide thickness.

If a real MOS capacity is considered, there may be unwanted charges in the oxide/semiconductor interface and the work functions of the metal and the semiconductor are most likely not the same. Therefore, an adequate voltage must be applied to the gate to get the ideal situation.

Then, if we consider a p-type MOS structure (which leads to an NMOS transistor), when the gate voltage V_{GS} is zero or negative, the current between drain and source, I_{DS} is zero. The only way for current to flow through the transistor is by applying a positive gate voltage (reaching the inversion mode). In this way, the gate attracts free electrons into the p region of the substrate. When the gate voltage is positive enough, the hole concentration is very small, with free electrons in the semiconductor (region under the gate). It is the same effect as creating a layer of n-type material between the drain and source terminals, called the n-type inversion layer or channel (Fig. 1.2). The minimum voltage V_{GS} necessary to create the n-type inversion layer is called the threshold voltage, V_{TH}, and its typical values can vary depending on the technology. Once the channel is created, the application of a voltage between the drain and the substrate will lead to the flow of current in the NMOSFET. Therefore, three regions of operation of the MOSFET can be distinguished, which are as follows:

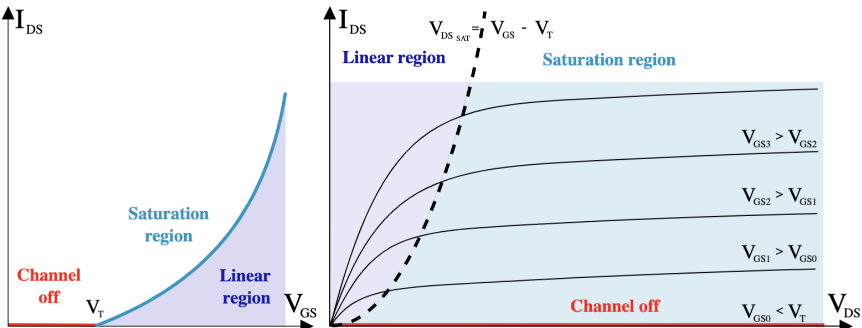


Figure 1.4: MOSFET output characteristics. Different operation modes can be observed depending on the applied bias [5].

- **Cutt-off or weak-inversion mode** is when $V_{GS} < V_{TH}$. In this region the channel has not been created and, therefore, there is no conduction between source and drain, so the MOSFET behaves like an open switch.

- **Linear region or ohmic mode**, when a sufficiently gate bias is applied ($V_{GS} > V_{TH}$), to form a inversion layer between the source and drain terminals and the drain voltage is $V_{DS} < (V_{GS} - V_{TH})$. In this case, the current has a behavior that is similar to a resistor controlled by the voltage applied to the gate.

- **Saturation or active mode**, if $V_{GS} > V_{TH}$ and $V_{DS} > (V_{GS} - V_{TH})$. The channel is created but "pinched off" at the drain end. It occurs when the saturation voltage is exceeded and the channel deforms. The current is no longer dependent on the potential difference between drain and substrate. At this point, this drain voltage and drain current (which saturates) is designated as V_{SAT} and I_{SAT} respectively.

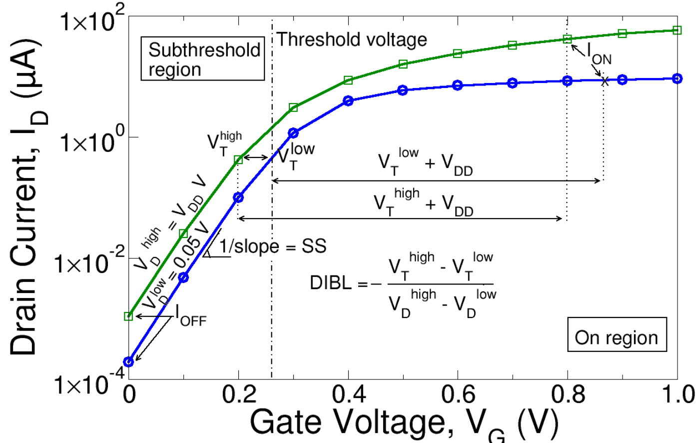


Figure 1.5: Example of typical I_D-V_G curves for a MOSFET. The different electrical parameters that can be obtained from those curves are indicated within the graph (V_{TH}, I_{off}, I_{on} and SS).

Figure 1.4 shows an example of typical I_{DS}-V_{DS} and I_{DS}-V_{GS} curves for a MOSFET, from which a set of parameters defining the MOSFET behavior can be extracted (e.g.: V_{TH}, I_{off}, I_{on}, SS, V_{DSAT},...). In this thesis we will focus on V_{TH}, I_{off}, I_{on} and SS, as they are the most important parameters for all the conducted experiments [6]. Regarding the V_{TH}, we use the constant current method (i.e. V_{TH} is the

voltage at a given current, determined by the user based on the particular device) to extrat it [7]. However, we note that there are several other methods to extract it from these curves, for instance: the extrapolation method in the linear region or the transconductance extrapolation method in the linear region. The importance of such parameter relies on the fact that the V_{TH} can be used as indicative of the device's degradation and device-to-device variability [8]. To obtain SS parameter, the value of the slope in the subthreshold region of the I_{DS}-V_{GS} curve is extracted. From the same plot, I_{on} and I_{off} can also be obtained, the former from the currrent at V_G=V_{TH}+V_{DD} (being V_{DD} the applied voltage) and the latter from V_G=0, as shown in Fig. 1.5.

1.1.2 MOSFET Scaling

The rise of microelectronics and the constant demand from society of smaller devices with greater processing capacity has caused the size of devices to reduce at an uncontrollable speed. The industry has followed the trend predicted by Moore's law, which has reflected the evolution of electronics, as shown in Fig. 1.6.

With the scaling, the MOSFET transistor has improved its performance until the end of the 20th century. However, since then, the reduction of the size of the transistors had associated problems, such as short channel effects, speed saturation or channel length modulation. Moreover, reliability issues gain importance as size reduces. As the gate oxide thickness decreases, tunnelling current through the device increases and failure mechanisms appear, as the dielectric breakdown, the Channel Hot Carriers (CHC) [11] or Bias Temperature Instabilities (BTI) [12] (see section 1.4.2). Therefore, it is essential to analize them in detail and propose alternatives to overcome all these issues.

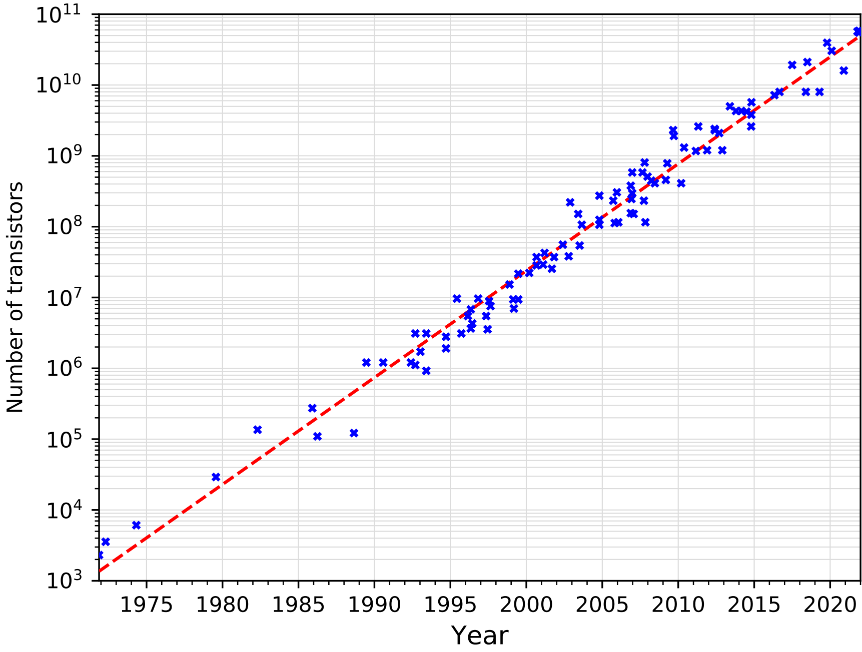


Figure 1.6: Number of thousands of transistors for several processors vs their release date. Data has been collected by Rupp [9] from the original work of Danowitz *et al.* [10] up to 2010, and from AMD, Intel and IBM data-sheets henceforth to 2022. The dashed red line provides Moore's law [3] trend.

1.2 Advanced materials for MOSFETs

One of the alternatives to solve the problem of scaling is to use new materials. Specifically, high-k dielectrics, metal gates and III-V substrates [13]. In this thesis, some of these new materials have been used, which are explained in more detail in the following sections.

1.2.1 High-k dielectrics

A solution to reduce the leakage current derived from the scaling of the thickness of the gate dielectric is the introduction of materials with high dielectric permittiv-

ity [4]. High-k materials allow to obtain the same capacity per unit area as with a SiO_2-based dielectric, but with a larger thicknesses. Therefore, the potential barrier between gate and substrate is wider and the leakage tunnelling current through the oxide is reduced [14]. Figure 1.7 shows how the leakage tunnelling current is reduced using high-k dielectrics taking into account that both MIS structures have the same capacitance.

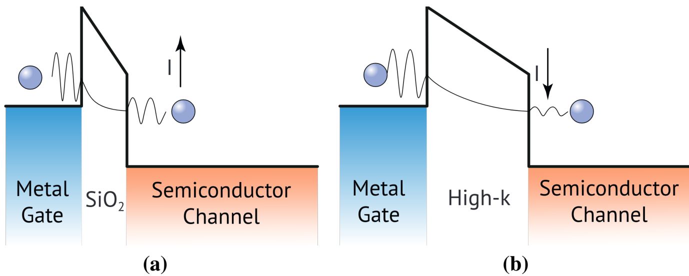


Figure 1.7: Schematics representation of the leakage current reduction in a MOS structure when a SiO_2 dielectric (a) is replaced by a high-k dielectric (b) with same capacitance, using a larger thickness.

The replacement of the SiO_2 layer by a high-k dielectric implies the introduction of a new parameter to describe the behavior of the transistor: the Equivalent Oxide Thickness (EOT), which is defined as the equivalent thickness of a SiO_2 layer needed to obtain the same capacitance as the one obtained by the high-k dielectrics (Equation 1.2),

$$EOT_{high-k} = t_{high-k} \frac{\kappa_{SiO_2}}{\kappa_{high-k}} \tag{1.2}$$

where K and t are the dielectric constant and physical thickness respectively, of the materials indicated in the subscript (high-k and SiO_2). The two main advantages of high-k dielectrics is that they offer a significant reduction in gate leakage current and they are capable of providing significantly lower EOT values, thereby allowing the use of lower gate voltages [15].

It should be noted that the replacement of SiO_2 by high-k dielectrics has not been an easy task since the only drawback of SiO_2 was the lower dielectric constant. In the 00's, the physical and electrical properties of various metal oxides where studied as candidates to replace SiO_2, such as ZrO_2, Al_2O_3, Y_2O_3 and La_2O_3 [16–21].

Despite having a high dielectric constant, high-k materials must be compatible with CMOS processing and achieve thermal stability. Moreover, defect density must be low to provide high carrier mobility in the channel, and they need to have a large gap power band. The semiconductor industry found oxides based on Hf as a good candidate, such as hafnium oxide, with ($\kappa \sim 20 - 25$) for the first generation of CMOS products with 45nm technology and metal gate electrodes [22, 23]. Despite their success in advanced technology nodes [24], its polycrystalline morphology is a drawback, which has been studied in different works [4, 25–27]. In some of them, the electrical properties and reliability of grains and grain boundaries of polycrystalline high-k dielectrics have been analyzed at the nanoscale using AFM related techniques [28].

1.2.2 Metal gates

The first MOSFET ever fabricated was made of silicon as channel material and aluminum for the gate in Bell Labs [29]; those materials were the general rule in the semiconductor industry all until the 70's, in which the problems added in the fabrication process by aluminum forced the industry to search for alternatives. The chosen substitute, owing to its low price and its compatibility with the other fabrication processes, was the highly doped polycrystaline silicon. However, with the continuous scaling of dimensions down to the nanoscale and the substitution of SiO_2 as insulator by high-k materials, polysilicon was replaced by metals, as several flaws of the former, i.e. poly depletion effect (not showed by metals) or its chemical incompatibility with the high-k materials, made it unsuited for the newer technological nodes. However, metals suffer from pollycrystallization. The metal polycrystallization results in grains with different sizes and orientations, which have associated different work functions (WFs). The random distribution of grains (and the corresponding WF) results in V_{TH} variability (TVV) [30–32]. Some works have already analyzed the impact of the WF fluctuations on the variability of MOSFETs [30, 31]. However, the statistical models that were used make assumptions that might not be representative of real devices. This thesis will contribute to evaluate the impact of both, metal gates and high-k dielectric (Chapter 3) polycrystallization on MOSFET variability.

1.3 Beyond the MOSFET device

The continuous scaling of devices over the last 50 years has been one of the keys for the development of the electronics industry [33, 34], so the minimum line width is reduced leading to new electronic nodes [35]. Besides the introduction of new materials in the MOSFET device (see section 1.2), another important line of research to continue with the scaling is to develop alternative structures to conventional MOSFETs. Figure 1.8 shows some examples of promising devices such as those made with graphene or other 2D materials from which field effect transistor can be build, Organic Thin Field effect Transistors (OTFTs) and Nanowire Transistors (NW), among others. In this thesis an analysis at the nanoscale of OTFTs and Graphene Field Effect Transistors (GFETs) are presented. For this reason, these devices are explained in the next sections.

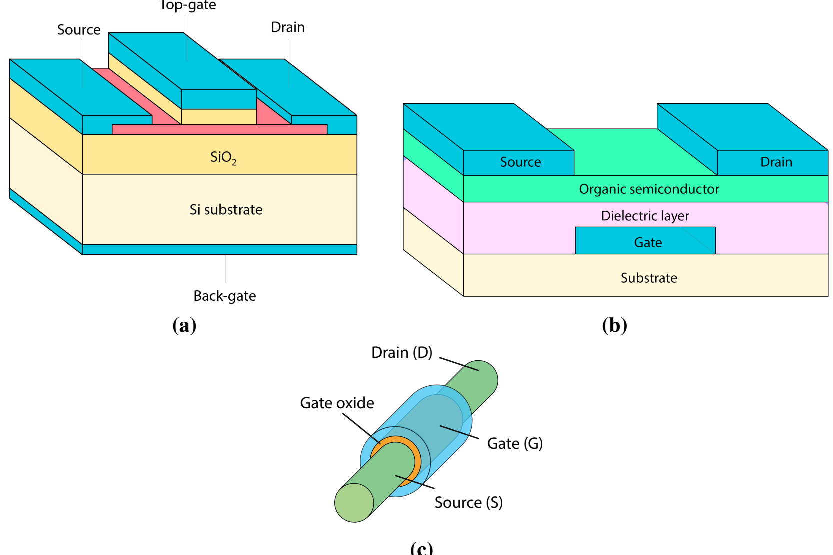


Figure 1.8: Several alternative devices to conventional MOSFET: (a) Graphene Field Effect Transistor (GFET) (red part corresponds to graphene area), (b) Organic Thin Field Effect Transistor (OTFT) and (c) Nanowire (NW) transistor.

1.3.1 GFET devices

Two dimensional materials (2DMs), with their atomic thickness and structural and electrical properties (e.g. low roughness, high mobility...), together with their compatibility with the CMOS fabrication techniques, provide an interesting alternative to the classical silicon devices, allowing for the survival of Moore's law down to nanoscale sizes. The most prototypical of those 2DMs is graphene, which was originally isolated from graphite by physical exfoliation by Geim and Novoselov [36], giving rise to the 2DMs field. In addition, in 2010 they obtained the Nobel Prize in Physics for the work carried out giving a great boost to research on graphene.

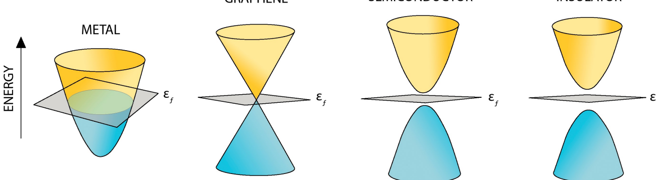


Figure 1.9: Graphene in contrast to other substances. (a) Metal. Electronic bands overlapped. (b) Graphene. Cone shaped electronic bands without band gap. (c) Semiconductor. Electronic bands separated by a very small energy gap. (d) Insulator. Electronic bands separated by a very large energy gap.

Graphene [36] is a two-dimensional material composed of a single layer of carbon atoms, forming a hexagonal lattice one atom thick. Carbon has several allotropic forms, being the base of all its configurations (fullerene, nanotube and graphene) [37]. In graphene, bounding is due to the hybrid sp2 orbitals, involving the s orbitals and the in-plane p orbitals, thus leaving free pz. Indeed, those pz orbitals are quite important from a chemical point of view as they are the ones allowing for -ization of graphene (e.g. oxidation). This is what determines the electronic properties of graphene. Graphene has properties between metals and semiconductors. The conduction band and the valence band are cone-shaped (instead of paraboloids), known as Dirac cones, and at the junction of these cones the Fermi level is found (Fig. 1.9). The upper band corresponds to the conduction band and the lower band corresponds to the Valence band. When the Fermi level is in the conduction band, the material behaves like a metal since electrons travel free through the band. In semiconductors and insulators, the Fermi level is in the gap, called for-

bidden band. In the case of graphene, the Fermi level is at the junction of the bands and, therefore, there is no gap and electrons can travel easily from one band to the other (as shown in Fig. 1.9), facilitating electrical conduction. Since graphene does not have a band gap, which is needed to switch on and off a device like a MOSFET, graphene based devices cannot be used for digital applications, but analogic ones. Moreover, taking into account the characteristics of this material (which is also flexible and transparent, for example), it has great potential for applications in flexible electronics, batteries, sensors or high frequency processors [38–40] among others.

Among the diferent devices that can be manufactured with graphene we will focus of GFETs, since will be studied in Chapter 4. A GFET is basically a FET device. There are two configurations, those with the gate at the top (top gate GFETs) and those without that terminal at the back, which are called back gate GFETs, as shown in Fig. 1.10.

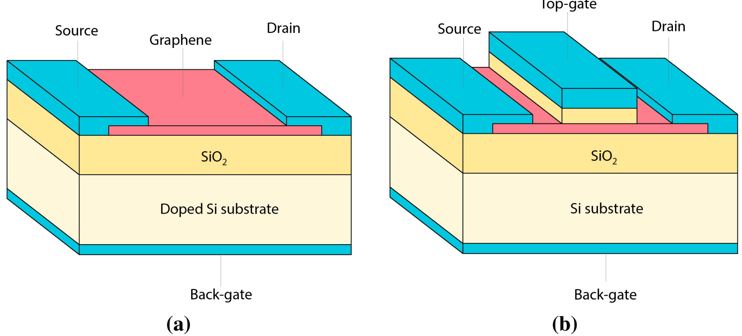
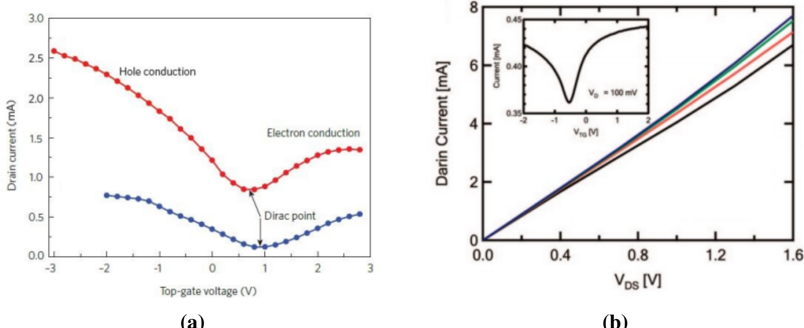


Figure 1.10: Schematic of the GFET configurations, (a) back-gate and (b) top-gate.

As can be seen in Fig. 1.10(a), in the back gate GFETs the channel is exposed to the environment, being easier to manufacture. In this case, however, the properties of graphene can only be maintained if it is possible to avoid contamination that may be introduced by contact with the environment. The gate contact area is much larger since it is contacted by the substrate, but it is more difficult to control the flow of current through the structure. On the other hand, in the top-gate GFETs the modulation of the electrical behavior of graphene is much better and the graphene is not exposed to enviroment. However, the manufacture of the gate terminal can damage the channel and modify the properties of the graphene.

The typical curves of a GFET are shown in Fig. 1.11(a). Figure 1.11(a) shows two typical I_{DS}-V_{GS} characteristics, that is, the drain current as a function of the voltage at the gate measured on a GFET (from -3V to 3V) when applying a small voltage on the drain terminal (with the source terminal at 0V).



(a) (b)

Figure 1.11: I_D-V_G (a) [41] and I_D-V_{DS} (b) [42] characteristic of GFET devices.

Note that the current is observed in both polarities, showing its ambipolar behaviour. The Dirac point (V_{DIRAC}, the point of minimum drain current, clearly located at 0V) is observed in both I_{DS}-V_{GS} curves, for a gate voltage Vg $\sim$ 1V. This point corresponds to the junction of the cones of the conduction band and the valence band, as previously commented. When V_{DIRAC} is different to zero, it means that there are non-ideal effects in the material as dopants. From V_{DIRAC}, the density and type of carriers, whether electrons or holes, in the channel, can be determined. In this case, gate voltages larger than V_{DIRAC} promote an accumulation of majority electrons while for V_G<V_{DIRAC}, it promotes the accumulation of holes.

Figure 1.11(b) shows typical I_{DS}-V_{DS} characteristics obtained on a GFET when applying a voltage sweep at the drain from 0 to 1.6V at different V_{GS}. The dependence shown by the I-V characteristic is almost linear for the measured voltage ranges. This behavior, without a saturation region, is due to the fact that graphene does not have a forbidden band or gap.

Althoug graphene based devices have been extensively studied during last years, these technologies are still in their infancy, and understanding issues such as their device-to-device (or time-zero) variability and reliability is essential to introduce

suitable countermeasures into the fabrication processes, device architecture and/or circuit design. Taking as example graphene-based devices, nanoscale defects, as Grain Boundaries (GB), wrinkles and corrugations, can appear in the graphene layer, which have been proved to hinder its electrical properties [43, 44], negatively affecting the corresponding device performance.

Though reliability of emerging devices is crucial for their commercialization, its study is also limited. As for Si-based devices, aging mechanisms [45], as Bias Temperature Instabilities (BTI) and Hot Carrier Injection (HCI) degradation have been observed in GFETs [46]. These mechanisms will introduce a time-dependent variability during the device operation in the circuit, so that drifts of key device parameters (as threshold voltage and carrier mobility) occur, which negatively impact the circuit performance. For example, Illarionov et. al. [46, 47] studied different degradation phenomena of the GFETs like BTI or CHC. They found that the electrical properties of the GFET changes after an electrical stress in a similar fashion to CMOS technology [48, 49] but those analysis are only carried out at device level.

1.3.2 OTFT devices

Thin-film transistor (TFT) is a type of transistor that is manufactured by depositing thin layers of an active semiconductor, a dielectric layer, and metal contacts on a substrate [50, 51]. In the case of OTFTs, the active semiconductor is an organic material, which during the last years, have been extensively investigated given the need for a constant reduction in the cost and physical size of consumer electronics [52]. In addition, organic materials hold great promise in terms of properties, sustainability and are more economical, unlike silicon-based technology, that involves high-temperature and high-vacuum deposition processes [53]. The mechanical flexibility of this type of materials makes them also compatible with plastic substrates for folding products [54,55]. However, the properties of organic polymers are very sensitive to environmental conditions as, for example, temperature and/or moisture (among others) affecting the reliability of these devices [56]. That is why the performance and the variability of these devices must be analyzed in detail, in addition to the aging mechanisms, to be able to compare them with conventional CMOS technologies.

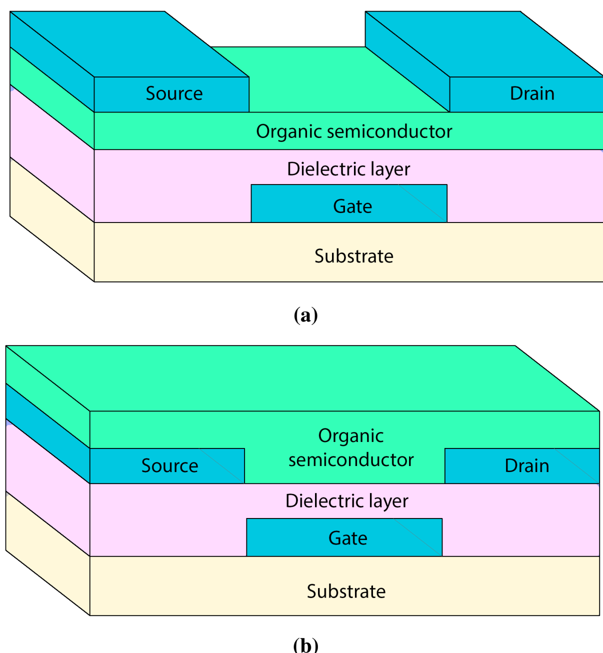


Figure 1.12: Top and bottom contact OTFT architectures.

Based on organic materials, there are different types of organic devices, for instance: OLED (organic light-emitting diodes) [56,57], which emit light when a voltage is applied to the device; solar cells which, when illuminated, produce an electrical voltage and finally, OTFTs [55, 56, 58], which are commonly used as switches. OTFTs can have different applications such as electronic paper, sensors and radio frequency identification (RFID) cards [55, 56, 59].

OTFTs are structurally similar to MOSFETs as can be seen in Fig. 1.12. In this case, the source and drain electrodes are metallic instead of doped semiconductors, which implies a variation in the manufacturing processes regarding the MOSFET. The conduction between the drain and source is through the organic semiconductor material, whose conductivity is controlled by a voltage applied at the gate. Therefore, the OTFT has the gate, drain, source terminals, and a dielectric and an organic semiconductor layer grown on a substrate. There are two types of configurations.

On the one hand, the top contact arquitecture, that has the source and drain electrode on the semiconductor layer, and on the other hand, the bottom contact arquitecture where the semiconductor layer covers the source and drain electrodes, remaining buried.

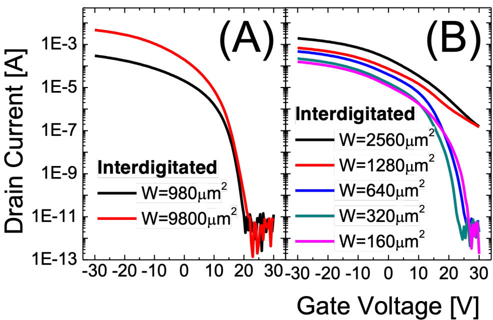


Figure 1.13: I_D-V_G charcteristics of two OTFT devices with different lenght [60].

Figure 1.13 shows typical I-V characteristics of an OTFT. This example in particular is a p-type transistor operating in depletion mode, as the subthreshold region is located at voltages above 0V [61]. From Fig. 1.13 we can see that these devices have an excellent distinction between the on and the off state and that the latter is very low (in the order of pA) which means an extremely low consumption in such state. On the other hand, in the on-state, currents as high as 1mA can be achieved by applying around ±30V [62]. Although such voltages are much larger than in CMOS technology, namely ∼0.8V [63], they are common and nothing surprising in organic devices, as their mobilities are much lower, i.e. between 1 to 1.75 cm^2/Vs at ±30V.

Despite the potential of these devices and all the studies carried out to improve their parameters, such as contact resistance or mobility of charge carriers [64, 65], there are few studies on the reliability of OTFTs [66]. Thus, the origin of possible reliability problems must be evaluated, which is one of the contributions of this thesis.

1.4 Variability

As already introduced in previous sections, the increasing variability of the main electrical parameters of devices, such as V_{TH}, etc.., is one of the most preeminent issues in the ultrascaled CMOS and emerging technologies, as it directly increases in line with the higher integration levels found in the cutting edge electronic devices [67, 68]. Consequently, it is essential to investigate the sources of variability that affect devices and circuits. These can be classified in two groups, depending on the origin of the varibility source: the time-zero variability (TZV) [69] (i.e. unwanted deviations of the parameters of the devices with respect to the ideal behaviour due to random variations during the fabrication process) and the time-dependent variability (TDV) which, in general terms, refers to time evolution of the variability when a circuit works on its operation conditions [70]; due to aging effects.

1.4.1 Time-zero variability

Time-zero variability is due to variations of the device parameters even before the circuits start to work and can be grouped into stochastic and systematic. Regarding stochastic variability, it is defined as a process of local variability that causes parametric fluctuations between identically manufactured devices. On the other hand, the systematic variability can theoretically be predicted since it is defined as a process of global variability causing a shift in the mean of the designated parameters, including the dimension of the devices, such as the width, length or thickness of the gate oxide.

During the last years, the stochastic variability has been studied deeply. Its impact on the variability of the devices clearly affect electrical parameters such as V_{TH}, I_{on}, I_{off} [71]. Variability inside the channel can be caused by random fluctuations in the dopants concentration along the device, and the material roughness causing deviations from the design pattern [72–75]. Although those are the most important sources of variability in large channel devices, it is also important to take into account the effect of granularity in polysilicon on metal gate [76], or variations in the oxide thickness due to high-k polycrystallization, among others. Focusing on the

granularity of the gate, it causes a non-uniform dopping or electronic density, in the case of metals, that generates local variation on the threshold voltage [75]. Consequently, it becomes of interest to study the granularity impact of the gates especially on modern high-k devices [77]. High-k polycrystallization must be also studied. Indeed, the methodology developed by Couso et al. [78] is of great interest for us, since, from experimental CAFM measurements, i.e. topographic and current maps, gate oxide thickness and charge density maps can be obtained at the nanoscale, reflecting these nanoscale fluctuations. This information can be used to evaluate its impact on the device variability. More details are given in Chapter 3. Finally it's important to emphasize that TZV is also important in emerging devices as those based on GFETs [79, 80] and/or OTFTs [81–84] since technology is not nature enough to manufacture devices with low variability.

1.4.2 Time-dependent variability

Time-dependent variability is considered to be the variability that occurs when a circuit begins to operate. It corresponds to the time evolution of the variability of the devices and/or circuits. Therefore, that variability will be determined by aspects such as the environment and the aging mechanisms, which affect the operating conditions of the circuit. This type of variability (reliability) has been studied for decades [85], and is still a matter of concern for researchers given the aggressive scaling of device dimensions and all the problems that have already been discussed previously derived from scaling. Depending on the nature of the phenomena associated to the reliability problems, different mechanisms are described in the literature such as BTI (Bias Temperature Instability), random telegraph noise, Channel Hot Carrier (CHC) and dielectric breakdown [86–89]. This section will be dedicated to review some of the most common failure mechanisms that will be considered in this thesis.

Bias Temperature Instabilities

The Bias Temperature Instability (BTI) is a severe degradation mechanism in ultra-scaled MOSFETs devices. This mechanism, which has become increasingly important as the devices reach the nanometric scale, leads to the degradation of the

electrical parameters of the MOSFETs when they have been operating under certain conditions of voltage and temperature (stress conditions). This stress mainly produces an increase in the threshold voltage (in absolute value) of the devices and also a degradation of the mobility. There are two types of BTI mechanisms, the negative BTI that occurs in PMOS devices when a negative voltage is applied to the gate terminal and the positive BTI, which occurs in NMOS devices when a positive voltage is applied to the gate terminal of the device. In both cases, the other contacts are grounded (Fig. 1.14).

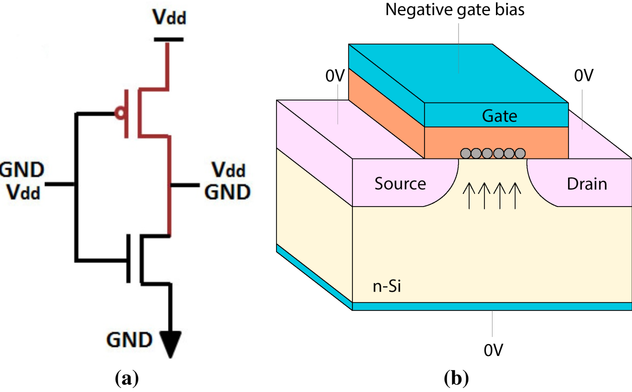


Figure 1.14: (a) Bias conditions during circuit operation of a CMOS inverter. When the input is connected to ground, the output is high and the pMOS FET (top) is under NBTI stress conditions. When the input is high, the output is zero and, in this case, the NMOSFET is under PBTI. (b) Schematic of a cross-section of a NBTI stressed p-channel MOSFET.

In both cases, this mechanism creates interface states that function as defects or traps which, together with permanent [90, 91] defects, give rise to the capture of charge at the interface of the gate oxide [92, 93]. This charge trapping causes a variation in the threshold voltage. In the case of NBTI, this trapping occurs to a greater extent at the interface of silicon with the dielectric [94, 95], although as scaling increases, the traps or pre-existing defects in the oxide must be taken into account [96]. In the case of PBTI, where the contribution to degradation is much lower than in the case of NBTI, charge trapping is a consequence of electron capture in pre-existing oxide traps, although the generation process also exists leading to new traps [97]. BTI has also been observed in emerging devices such as GFETs

[98, 99] and OTFTs [100–102]. We note that although the electronic devices show some degree of recovery after the application of an stress, such a recovery is never complete and thus there is always a permanent damage for each stress cycle.

Channel Hot Carrier

Degradation by injection of hot carriers (Channel Hot Carriers or CHC) is another important aging mechanism to consider due to the scaling of the transistors and the increase of the electric field in the channel. This mechanism occurs as a consequence of the current flowing through the transistor channel, when a voltage is applied to the gate terminal V_G (greater than the threshold voltage, V_{TH}) while applying a drain voltage above its saturation voltage (source terminal grounded).

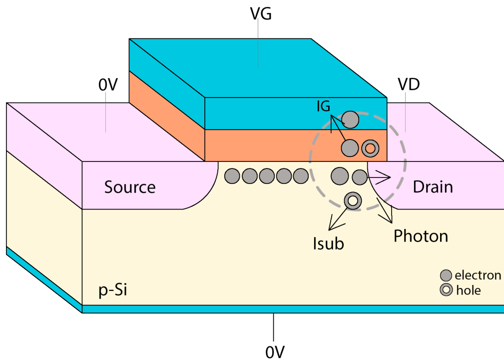


Figure 1.15: Typical channel hot-carrier stress condition and the resulting high-field region of the drain in an nMOS transistor.

Therefore, the drain-source voltage (V_{DS}) leads to high electric fields, which raises the energy level of the carriers, accelerating them and creating electron-hole pairs near the drain terminal. These carriers can be injected at the interface of the channel with the dielectric, degrading it and causing an increase in the threshold voltage as shown in Fig. 1.15 [103, 104]. CHC degradation affects both P-type and N-type transistors, although the impact is more pronounced in NMOS devices [105], neglecting in many cases the contribution in PMOS devices. The damage generated by CHC causes changes in the parameters of the device. Unlike BTI, the CHC does not seem to show relaxation effects and the damage induced in the device is permanent. Furthermore, degradation by BTI occurs homogeneously throughout the

oxide while CHC occurs near the drain region [106–108]. Although aging mechanisms have been extensively analyzed in CMOS technologies, these kinds of studies for OTFTs are scarce and focused on the device level but not on the nanoscale one. The same happens in the case of graphene-based FETs (GFETs). The study of their reliability is still to be fully addressed. For example, Illarionov et al. [46] have studied the different degradation mechanisms of the GFETs, namely BTI and CHC, finding a similar degradation in the electrical properties of the GFETs than that found in the more classical MOSFETs. However, they only addressed their effect at device level without giving any insight on the physical damage (i.e. nanoscale level). Consequently, in this thesis we focus not only on the variability and degradation mechanisms of OTFTs and GFETs at the device level, but also at the nanoscale, providing in this way a deeper discussion not achieved in previous works.

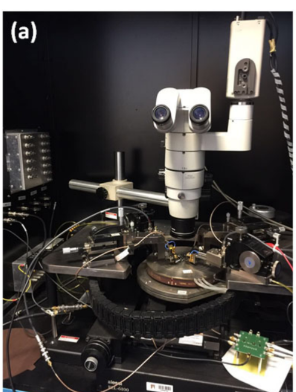
1.5 Characterization Techniques

Once the theoretical background has been introduced in the previous sections, in this section, the characterization techniques used to obtain information of the electrical properties at device level and at the nanoscale are presented.

1.5.1 Standard characterization techniques

The measurement of the electrical properties and the study of the failure mechanisms of electronic devices is carried out by subjecting the device to an electrical stress, and measuring the current or voltage through the device before and after the stress with a semiconductor parameter analyzer (SPA), as shown in the picture of Fig. 1.16(b). Given the dimensions of the devices, it is necessary to use a probe station Fig. 1.16(a), which consists of conductive tips that allow the devices to be electrically connected with the SPA. These tips are attached to micromanipulators that allow them to move in both directions in order to directly connect the devices (Fig. 1.16). In the central part of Fig. 1.16(a), one can see the optical system that allows the user to view both the tips and the sample, which is on a metal support

called chuck, where the wafer is placed and immobilized by vacuum. As the chuck is metallic, it can be used as a contact terminal. For example, to perform measurements in back gated GFETs, the chuck is polarized to apply a voltage to the gate of the device. The probe station is connected to the SPA through source measurement units (SMUs).



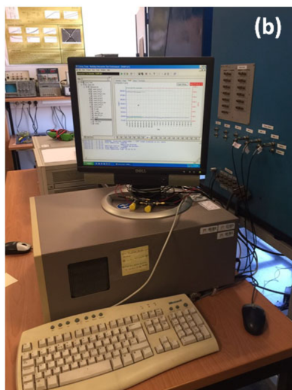


Figure 1.16: Images of the probe station (a) and Semiconductor Parameter Analyzer (SPA) (b).

Ramp voltage tests are commonly used to measure the electrical characteristics of the devices, for example of MOSFETs I_D-V_G, I_D-V_D, I_G-V_G curves, as well as to stress and study the failure mechanisms discussed in section 1.4.2 (BTI, CHC ..).

Customaryly, the degradation and failure mechanisms afecting the gate oxide of MOSFETs are characterized through the measurement of the variations of the electrical properties of the devices at the-device-level (on fully processed devices) before and after an electrical stress. Such variations, however, have their origin at the nanoscale, indeed they are related with the defect generation and the charge trapping at the gate oxide. Thus, to obtain an improved insight on those time-dependent variations, it becomes essential to study those dielectric layers at the nanoscale level. Furthermore, nanoscale effects are also essential to understand the variability in fresh devices, as such variability is dependent on local effect such as fluctuations of the dopands density, defects in the crystalline structures, and so on. Therefore, a complete study of the variability cannot be limited to only the device level (i.e.

with a SPA) as it gives only averages, but to the nanometer range. For the nanoscale analysis of electronic devices and/or materials, scanning probe microscopy (SPM) related techniques have become very powerful. These techniques allow to obtain nanometer resolution maps of the topography and electrical properties of different materials. Since they have been extensively used in this thesis, they are introduced in more detail in next section and Chapter 2.

1.5.2 Nanoscale characterization techniques

SPMs can be divided into two big families: Scanning tunneling microscopy (STM) and Atomic force microscopy (AFM). The first STM was developed in 1981 at IBM Zurich Research Laboratory by G. Bining and H. Rohrer. It allowed to generate atomic surface images [109]. The inventors were awarded with the Nobel Prize in Physics in 1986. This type of microscope provides sub-nanometer resolution images of materials in all three dimensions but is limited to conductive samples and requires a high vacuum environment. The STM is based on the concept of quantum tunneling. A conductive tip is located very close to the surface of the material (Fig. 1.17), and by applying an electrical voltage to the tip (or sample), we can image the topography of the surface at an extremely small scale, from the measurement of the tunneling current that flows between the tip and the sample (which depends on the distance between the tip and the surface of the sample).

All the limitations discussed before, led to the invention of the first atomic force microscope (AFM) in 1986 [110], where the high vacuum environment is not necessary and it is possible to extend the range of materials to be analyzed: non conductive samples can also be measured. An AFM consists of a cantilever with a tip at its end, which moves over the surface of the structure allowing to measure the interaction force between the tip and the sample, from which topography can be obtained. Therefore, with an AFM it is possible to reproduce the morphology of the surface under study without specific environment.

AFM has led to the appearance of other techniques which allow to measure, simultaneously to the topography, other electrical properties. Depending on the electrical magnitude to be measured, there are different AFM related techniques,

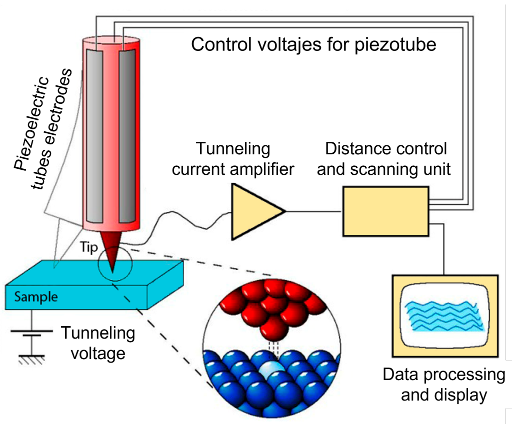


Figure 1.17: Scheme of an scanning tunneling microscope.

such as the Scanning Spreading Resistance Microscopy (SSRM) [111, 112], Scanning Capacitance Microscopy (SCM) [113, 114], Kelvin Probe Force Microscopy (KPFM) [115] and Conductive Atomic Force Microscope (CAFM). The CAFM was developed in the mid-1990s [116] to measure currents through gate dielectrics at nanometer scale. With a CAFM, the topography and current can be measured simultaneously by applying a voltage on the conductive tip. Kelvin Probe Force Microscope (KPFM) was introduced in 1991 to obtain nanoscale information of the electrical properties of materials for electronic devices. In this case, KPFM measures simultaneously the topography and the contact potential difference between the tip and the sample; that is, the difference of work functions between the tip and the sample. This technique can provide qualitative information of the surface chemistry or charge concentration in the sample.

The CAFM and KPFM have been broadly used to characterize the electrical properties at the nanoscale of several kinds of materials, ranging from 2D materials, as graphene [117–119], to organic materials [120], but also more classical materials such as the high-k gate dielectrics [121–127]. These techniques have help to study the effects of device shrinking into their electrical properties [128, 129], as they allow for a direct observation at the nanoscale of the physical mechanisms originating such effects, i.e. doping and/or material thickness variability. For in-

stance, Bersuker et al. [130] demonstrated (using AFM-based techniques) that in polycrystalline HfO_2 thin-films the leakage current flows preferentially through the grain boundaries, in which the material is thinner [128]. Furthermore, it is worth mentioning that AFM-based techniques have also been used to study the degradation mechanisms For example, the dielectric breakdown has been extensively analyzed on SiO_2 and high-k dielectrics. BTI and CHC have been also studied in MOSFETs [106] and, preliminary in alternative architectures. For instance, in Ref. [131], Bürgi et al. have studied the bias temperature inestability (BTI) degradation in OTFTs using a KPFM. They determined the change in the charge density at the polymer/dielectric interface after an applied electrical stress. Interestingly, herein it is also the case of graphene-based FETs (GFETs), the electrical properties of which have been extensively studied [132–135]. Although some works have also addressed their reliability [46,47], they only have studied their effect at device level without giving any insight on the local physical damage (i.e. the nanoscale level), thus providing an incomplete picture of the GFETs degradion.

In this thesis, we will take advantage of the nanoscale resolution of CAFM and KPFM to go one step further. Both techniques will be used to evaluate the impact of metal and high-k polycrystallization on MOSFETs electrical characteristics. It will also contribute to analyze the impact of aging mechanisms as NBTI and CHC in the nanoscale properties of in OTFTs and GFETs.

2 AFM and experimental considerations

As previously introduced in Chapter 1, the Atomic Force Microscope (AFM) is used to obtain topographic information with nanometer resolution. From an AFM and with the introduction of only some elements, electrical properties can also be measured, at the nanoscale, with other techniques such as CAFM (Conductive Atomic Force Microscopy), KPFM (Kelvin Probe Force Microscopy), SCM (Scanning Capacitance Microscopy) and SSRM (Scanning Spreading Resistance Microscopy), among others.

Since this thesis uses Atomic Force Microscopy based techniques extensively, this chapter is exclusively dedicated to them. First, the principle of operation and the different operation modes of an AFM are discussed. Afterwards, the different techniques with which is possible to measure, simultaneously with topography, other electrical properties, are introduced. In particular, the CAFM, which measures the conductivity, and the KPFM, which measures the contact potential between the tip and the sample, are described. Finally, details about the tips necessary for CAFM and KPFM experiments are also explained.

2.1 Principle of operation of the Atomic Force Microscope

The AFM is based on the measurement of the interaction forces between the sample and a tip when the distance between them is in the nanometric range. The tip is located at the end of a cantilever, which scans the surface of the sample of interest. The atoms at the end of the tip are the ones that interact with the sample, and the force that appears on the tip causes a deflection in the cantilever proportional to the applied force according to Hooke's law. This deflection is detected by a beam of laser that, once reflected at one of the edges of the cantilever, falls on a four-quadrant photodiode system capable of converting the detected intensity into a voltage that is collected by the AFM control electronics as shown in Fig. 2.1. The AFM control electronics is also in charge of keeping the distance between the tip and the sample constant while the measurement is being performed by means of the electronic feedback system. From this information, it is possible to reproduce the morphology of the surface under study when the cantilever is scanned over the surface thanks to a piezoelectric system. A computer is responsible for recording and storing the data obtained by the control electronics and, by means of adequate software, the image corresponding to the topography of the surface can be displayed and analyzed. In addition, we must not forget the need of a mechanical anti-vibration system that allows the experimental set-up to be isolated from external vibrations, achieving excellent lateral and vertical resolutions.

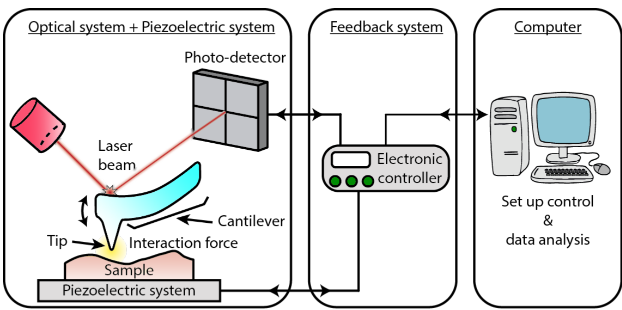


Figure 2.1: Schematic of a conventional Atomic Force Microscope.

Depending on the distance between the tip and the surface of the sample, different short-range or long-range forces [136] appear. The interaction forces between the tip and the sample can be described by a Lennard-Jones type intermolecular potential W(r), which represents a generic model of tip-sample interaction. This potential, which is shown in Fig. 2.2, is constituted by attractive and repulsive interactions as a function of the separation distance between the tip and the sample. On one hand, the long-range forces are mainly attractive forces as van der Waals, magnetic and electrostatic forces. The short range forces are basically repulsive forces as the Coulomb electron-electron interaction forces, which appear when the tip is in contact with the sample. In addition, there are capillary forces that appear in ambient conditions, due to a thin film of water between the tip and the sample [137, 138] because of ambient humidity. When the tip and sample are so close, a meniscus is formed between the tip and sample, leading to an attractive force.

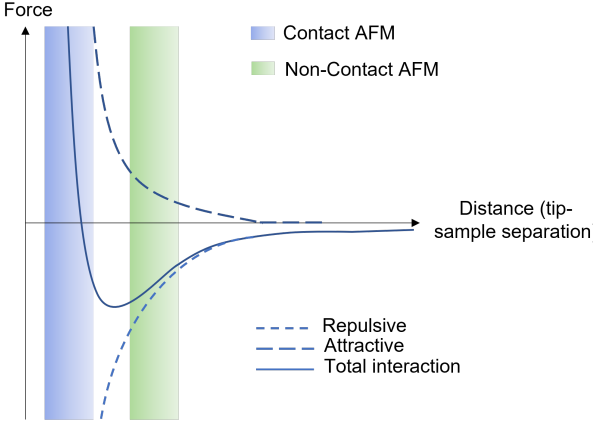


Figure 2.2: Interatomic force versus distance between AFM tip and sample surface.

2.2 Operation modes

Depending on the distance between the tip and the sample, two modes of operation can be described; the contact mode, which works in a repulsive regime, and the non-contact mode, which works in the attractive regime.

2.2.1 Contact mode

In this mode of operation, the tip is close enough to the sample so that the surface atoms of the sample interact in a repulsive regime [139]. The repulsive forces tend to separate the tip causing a deflection of the cantilever which is used to determine the topography of the sample. As its name suggests, the tip is in contact with the surface of the sample and, consequently, suffers wear out during scanning [140]. In the case of the measurements in air, the capillarity forces generated by a layer of water present on the surfaces due to the humidity of the environment must also be considered.

2.2.2 Non contact mode

In this case, the tip-sample interaction is in the attractive regime [141]. The tip is very close to the sample but not in contact as in the previous case. In this regime, the forces between the tip and the sample are smaller, so the resolution is lower than in the contact mode [142]. To increase the resolution, the tip is forced to oscillate around its ressonance frequency. Then, when the tip is close enough to the sample, Van der Waals forces vary the frequency of vibration of the cantilever, which serves as a feedback signal for adjusting the distance between the tip and the sample and get the surface topography. The main advantage of this mode is that the rapid deterioration of the tip or the sample is avoided.

2.2.3 Tapping mode

This mode [143] is an intermediate case between contact and non-contact mode. In this case, the topography is mapped by lightly touching the surface of the sample intermittently with an oscillating tip. The amplitude of oscillation of the cantilever changes according to the magnitude of the interaction force between the tip and the sample. For example, when the tip scans a protuberance on the surface, the distance between the tip and the sample decreases and the amplitude of oscillation decreases. The tapping mode allows to resist the lateral forces of the contact mode

and to use much higher scanning speeds. In addition, since it does not remain in continuous contact with the surface but intermittently, the tip does not wear as much as the contact mode. On the other hand, it offers a good resolution compared to non contact mode.

2.3 Conductive Atomic Force Microscopy (CAFM)

A CAFM is an AFM-based technique that enables topography and electrical current measurements simultaneously. Two different kind of test can be performed. On the one hand, topographical and current maps, which allow to analyze the homogeneity and conductivity changes of a specific area. Maps are obtained by applying a constant voltage to the sample while the tip scans the area. On the other hand, IV curves at a given position of the sample can be obtined. The IV curves allow to analyze different conduction mechanisms for different voltage ranges, applying a voltage ramp on the tip while it remains in a fixed position. To measure current and topography simultaneously a conductive tip and a low-noise preamplifier that picks up the current flowing through the tip when a bias is applied to the tip-sample system is required. The current that flows between the tip and the sample reveals information about the conductivity of the sample and allows a wide variety of applications for characterizing the electrical properties of new materials [144, 145]. Note that to perform measurements with CAFM, very resistant tips are needed since measurements are in contact mode. Figure 2.3 shows a schematics of a CAFM where the conductive tip, the preamplifier, and a voltage source necessary to apply a potential difference between the tip and the sample are shown.

Although standard CAFM is a technique widely used to evaluate the electrical properties of different kind of materials, the range of currents that can be measured was typically between 1pA to 1nA, depending on the characteristics of the preamplifier. So, if a higher range of intensity needs to be measured (as, for example, for the measurement of pre and post-BD current through gate oxides), some modifications, such as, the ECAFM (Enhanced CAFM) [146] are required. Specially designed modules such as log CAFM [147] or the resiscope module [148] have also been developed. In these cases, the range of currents that can be measured reaches mA. In this thesis the resiscope is used, so it is introduced in the next section.

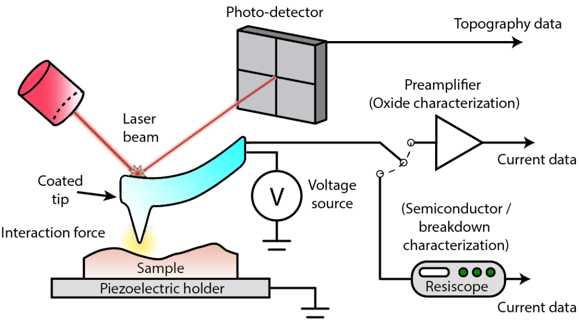


Figure 2.3: Atomic Force Microscope with the additional elements to configure a Conductive Atomic Force Microscope: conductive tip, preamplifier and voltage source to bias the sample.

2.3.1 Resiscope

The resiscope module, manufactured by Concept Scientific Instruments (CSI) [149] allows to measure the current from pA to mA in a single test, so it is one of the solutions to overcome the limitation of current range and can provide quantitative measurements of resistance and current of different materials. Figure 2.4 shows

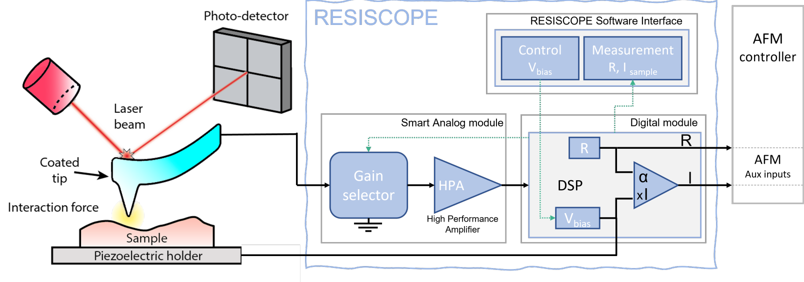


Figure 2.4: Schematic of working principle of a Resiscope connected with an AFM.

the schematic of a resiscope connected to the AFM where, by applying a voltage between the tip and the sample (while scanning in contact mode), the resiscope measures the resistance of the sample or the current through the high performance amplifier, simultaneously with the topography. This module has been used during the thesis to perform nanoscale measurements on back-gate graphene field effect transistors (see Chapter 4).

2.4 Kelvin Probe Force Microscopy (KPFM)

The KPFM technique is a tool that allows to obtain nanoscale images of the topography and contact potential difference (V_{CPD}) that exists between the surface of the analyzed sample and the material of the tip. This contact potential difference (V_{CPD}) is, actually, the difference between the work function of each material. It is widely used to characterize the electrical properties of metal and semiconductor surfaces. It was actually develop in the 90's for the measurement of the doping concentration in semiconductors for microelectronic applications [150]. In [150], for example, it was used to measure the V_{CPD} of different crystal facets of thin film, as CGSe on different substrates, showing that it allows to investigate the different crystal orientations of a polycrystalline material. KPFM can also provide information about gate dielectric properties. Since the V_{CPD} depends also on the amount of charge that is present in a dielectric (when measuring an oxide-semiconductor substrate, for example), KPFM can be used to analyze the amount of charge trapped in gate dielectrics of MOS structures [151]. In this thesis, KFPM has been used to study the impact of polycrystallization of metals on the contact potential variations of this materials and its impact on the variability of MOSFETs figures of merit (see Chapter 3). In addition, two different KPFM configurations (explained in Chapter 5) were combined to evaluate the effects of electrical stresses on the properties of organic thin-film transistors OTFTs. In the next section, the principle of operation of a KPFM is depicted in detail.

2.4.1 Principle of operation

The KPFM measures the V_{CPD} between a conductive AFM tip and a sample (Fig. 2.5). In Fig. 2.5(a) one can observe the energy levels of the tip and sample when they are separated by a given distance. Since, the tip and the sample are dissimilar materials, the fermi level is misaligned because the work functions are different. The contact potential difference between the tip and the sample is defined as:

$$V_{CPD} = \frac{\phi_{tip} - \phi_{sample}}{-e} \tag{2.1}$$

where ϕ_{tip} and ϕ_{sample} are the work functions of the sample and tip respectively, and e is the electron charge. When they are in electrical contact (for example, when the tip contacts the sample), as shown in Fig. 2.5(b), a current flows between the tip and the sample and, the Fermi levels are aligned. When this occurs, the vacuum levels (E_Ψ) are misaligned, and the difference between the vacuum levels is equivalent to the contact potential difference V_{CPD}. This contact potential can then be related to the difference in work functions of the tip and the sample. In the contact area, an electric force appears due to the V_{CPD} which can be cancelled by adding an external voltage of the same magnitude but different polarity between the tip and the sample, as seen in Fig. 2.5(c), so that the vacuum levels are again aligned.

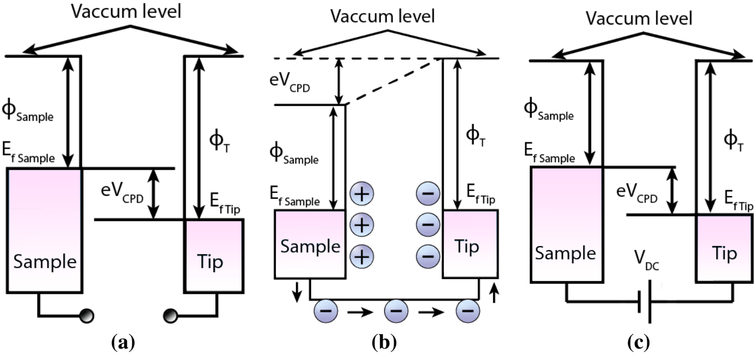


Figure 2.5: Energy band diagram of a sample and AFM tip for three cases: tip and sample are not in contact (a), tip and sample are in electrical contact (b), and a V_{DC} is applied between tip and sample to measure the V_{CPD} (c).

KPFM, as observed in Fig. 2.5(c), applies this voltage, that is, the voltage that is necessary to recover the situation shown in Fig. 2.5(a), which corresponds to V_{CPD}. To cancel the force between the tip and the sample, a potential containing a DC and an AC component with angular frequency ω is applied to the tip. Therefore, considering that the tip and the surface are separated by a distance z, the interaction force can be described mathematically by considering the sample-tip interaction as a capacitor. The electrostatic force can be described with the following Equation [150]:

$$F_{elec} = -\frac{1}{2}\frac{\partial C(z)}{\partial z}\left[(V_{DC} - V_{CPD}) + V_{AC}sin(\omega t)\right]^2 \tag{2.2}$$

where $\frac{\partial C(z)}{\partial z}$ is the gradient of the capacitance between the tip and the surface of the sample. This Equation 2.3 can be divided into three terms:

$$F_{elec} = F_{DC} + F_{\omega} + F_{2\omega} \tag{2.3}$$

- The first term gives rise to a static tip deflection:

$$F_{DC} = -\frac{\partial C(z)}{\partial z}\left[\frac{1}{2}\left(V_{DC} - V_{CPD}\right)^2\right] \tag{2.4}$$

- The second term is used to measure the V_{CPD}:

$$F_{\omega} = -\frac{\partial C(z)}{\partial z}\left(V_{DC} - V_{CPD}\right)V_{AC}sin(\omega t) \tag{2.5}$$

- The third term is used when taking measurements in a single pass mode, which will be explained later:

$$F_{2\omega} = \frac{1}{4}\frac{\partial C(z)}{\partial z}V_{AC}^2\left[cos(2\omega t) - 1\right] \tag{2.6}$$

From the Equations 2.4 and 2.5, we can obtain the voltage (V_{CPD}) by making the electrostatic forces between the tip and the sample zero when V_{DC}=V_{CPD} and therefore $F_{\omega} = 0$. So, by measuring V_{DC} as the tip scans the sample, a map of V_{CPD} on the scanned are can be otained simultaneously to the topography. This procedure corresponds to a measurement mode called double pass, which consists in taking both maps (topography and V_{CPD}) in two steps. The first step is to measure topography of the surface using the first resonance frequency in non-contact mode. Once the topography is obtained and stored, the tip is separated from the surface at a distance z and the stored topography is reproduced thereby maintaining a constant distance between the tip and the sample. During this second scan, the KPFM feedback applies V_{DC}=V_{CPD}, the cantilever stops vibrating (Equation 2.4) since the force $F_{\omega} = 0$, and the V_{CPD} map is stored. There is another measurement mode called single pass, where the topography and the V_{CPD} are measured during the same scan, using the second resonance frequency to obtain the V_{CPD}. In this mode, Equation 2.5 is used.

There are also two methods to measure V_{CPD} with KPFM, which are the amplitude modulation method (AM-KPFM) and the frequency modulation method (FM-KPFM). The amplitude modulation method allows measuring the potential very close to the surface and improves the lateral resolution. The frequency modulation method measures the electrostatic force gradient and has very high resolution and sensitivity. However, although FM-KPFM generally offers higher resolution than AM-KPFM [152–154], bimodal single-pass AM-KPFM measurements, thanks to the shorter tip-to-sample distance, can offer resolution comparable to FM-KPFM mode and minimizes cross-talk between topography and the contact potential data [153, 155]. In this thesis, the AM-KPFM single pass mode has been used.

2.5 AFM Probes

One of the most important issues that must be considered when performing measurements with AFM are the tips, since the resolution of the images depends on the geometric shape and mechanical characteristics. As previously mentioned, the tip is at the end of the cantilever as shown in Fig. 2.6. AFM tips are ideally modeled as

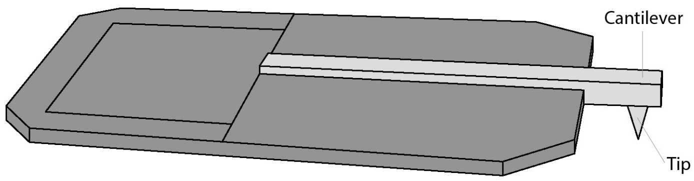


Figure 2.6: Typical schematics chip where the cantilever is mounted.

a cone with a hemisphere at its vertex as shown in Fig. 2.7 [156]. The radius of curvature R is defined as the radius of the hemisphere located at the vertex [Fig. 2.7(a)] and determines the limit for detecting structures with lateral dimensions of the order of the diameter of the tip [Fig. 2.7(b)], thus defining its resolution. In addition, the half-cone angle θ indicates the ability to image steep sidewalls [Fig. 2.7(c)]. Therefore, to obtain high resolution images with AFM, small radius of curvature and small semi-cone angles are required [157].

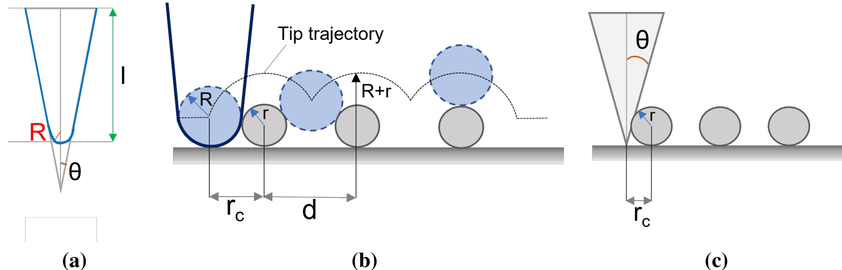


Figure 2.7: (a) Geometrical cross-section of a tip, with a finite length l, half-cone angle θ, and spherical apex radius R. (b) Influence of the curvature radius to detect structures. A smaller tip radius leads to a better AFM resolution. (c) Influence of the half-cone angle to image steep side-walls. Smaller θ leads to a better definition of the top side walls.

The geometry of the cantilevers with their length, width and thickness determines the mechanical properties of the cantilever. These properties are related to the elastic constant and the ressonance frequency. The tips can be pyramidal or conical in shape and can be made and/or coated with different materials (Fig. 2.8), such as doped diamond, PtIr among others.

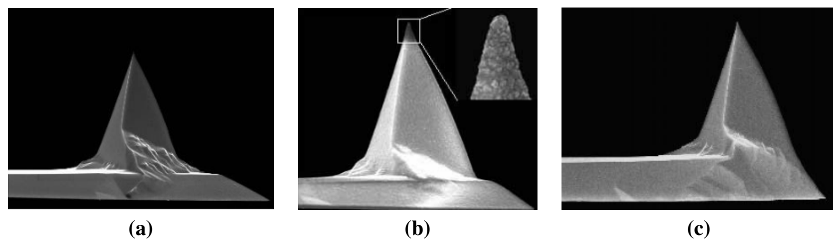


Figure 2.8: SEM images of (a) Silicon tip [158], (b) doped diamond coated Silicon tip [159] and (c) PtIr coated Silicon tip [159].

The materials used to manufacture the tips determine their properties. Depending on the AFM mode that needs to be used, some materials or others will be required. To carry out, for example, measurements with CAFM, conductive and very resistant tips are needed since the CAFM works in contact mode. Therefore, silicon tips are not suitable for this type of measurements as they wear out very quickly and have very low conductivity. So, metal-coated silicon tips or metal bulk tips are better. In metal coated tips, when coating wears out, they lose their conductivity. Therefore, metal bulk tips are the most suitable for this kind of measurements.

In addition, this type of tips implies a greater mechanical resistance leading to a longer tip lifetime. On the other hand, for measurements with KPFM, uncoated and highly doped Silicon tips can been used. With this type of tips, a higher resolution is achieved compared to coated tips. Moreover, since KPFM operates in non-contact mode, the tip wears out is minimum.

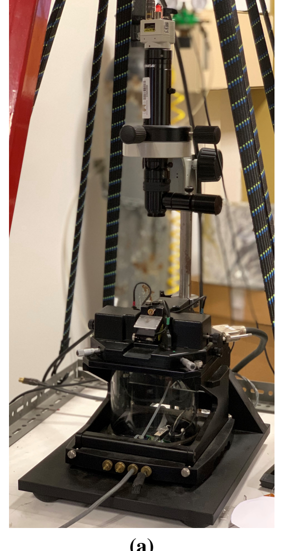
2.6 Setups used in this thesis

In this thesis, several experimental setups have been used to perform CAFM and KPFM experiments and different AFM tips have been used. In the following, their main characteristics are described.

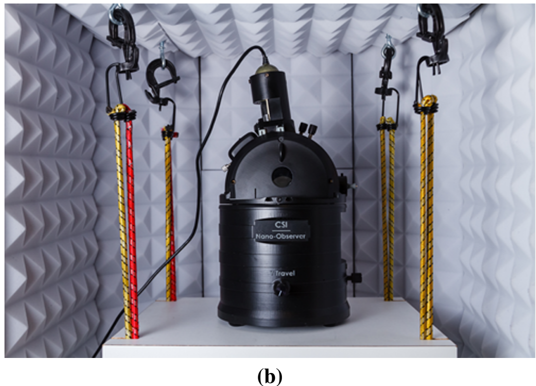
- Setup A: **Agilent 5100**
  AFM located at the laboratories of the REFEC group (Electronic Engineering Department of the Universitat Autònoma de Barcelona). This setup allows to work in contact or tapping mode and topography and CAFM measurements can be obtained in air and controlled atmospheres.

- Setup B: **Nano-Observer AFM**
  AFM located at the laboratories of the REFEC group (Electronic Engineering Department of the Universitat Autònoma de Barcelona). It allows performing topographic (in contact and tapping mode), CAFM and KPFM measurements in ambient and under controlled conditions.

A **Resiscope** module can be incorporated in both setups to measure currents from pA to mA.



(a)



(b)

Figure 2.9: Images of the Agilent 5100 (a) and the Nano-Observer (b) used in this thesis.

KPFM tips

- **NT-MDT Spectrum Instruments FMG01/Pt:** The size of the chip is 3.4 x 1.6 x 0.3 mm. These tips have a pyramidal geometry. The reflective side of the cantilever is platinum (Pt). The tip has a height (h) between $14 - 16$ μm, the curvature of the radius is 35 nm, and the side coating of the tip is platinum between $20 - 30$ nm. The cantilever specifications are shown in the Table 2.1:

Table 2.1: Cantilever specifications [160].

Cantilever lenght, $L \pm 5\mu m$	Cantilever width, $W \pm 5\mu m$	Cantilever thickness, μm	Resonant frequency, kHz	Force constant, N/m
225	35	3.0	47 - 76	1,2 - 6,4

* **AppNano SPM Probe Par# ANSCM-PT-10:** The size of the chip is 3.4 mm x 1.6 mm x 315 μm. The reflective side is platinum (Pt). The tip has a height (h) between $14 - 16$ μm, the curvature of the radius is 30 nm, and the side coating of the tip is platinum between $20 - 30$ nm.

  The cantilever specifications are shown in the Table 2.2:

Table 2.2: Cantilever specifications [161].

Cantilever lenght, $L \pm 5\mu m$	Cantilever width, $W \pm 5\mu m$	Cantilever thickness, μm	Resonant frequency, kHz	Force constant, N/m
225	30	3.0	43 - 81	1 - 5

* **AppNano SPM Probe Model: FORT Part# FORT-50:** The size of the chip is 3.4 mm x 1.6 mm x 315 μm. The reflective side is silicon (Si). The tip has a height (h) between $14 - 16$ μm, the curvature of the radius is 10 nm.

  The cantilever specifications are shown in the Table 2.3:

Table 2.3: Cantilever specifications [162].

Cantilever lenght, $L \pm 5\mu m$	Cantilever width, $W \pm 5\mu m$	Cantilever thickness, μm	Resonant frequency, kHz	Force constant, N/m
225	27	2.7	43 - 81	0.6 - 3.7

CAFM

- **BRUKER RMN-25PT400B:** The size of the chip is 3.4 mm x 1.6 mm x 315 μm. The reflective side of the cantilever is pure platinum and placed on a standard AFM probe sized ceramic substrate. These probes have a tip radius $< 20nm$.

  The cantilever specifications are shown in the Table 2.4:

Table 2.4: Cantilever specifications [163].

Cantilever lenght, $L \pm 5\mu m$	Cantilever width, $W \pm 5\mu m$	Cantilever thickness, μm	Resonant frequency, kHz	Force constant, N/m
400	100	3.0	5 - 11	6 - 14

Tapping mode

- **BRUKER NCHV-A:** The reflective side is aluminium and placed on a standard AFM probe sized ceramic substrate. These probes have a tip radius $8nm$.

  The cantilever specifications are shown in the Table 2.5:

Table 2.5: Cantilever specifications [164].

Cantilever lenght, L	Cantilever width, W	Cantilever thickness, μm	Resonant frequency, kHz	Force constant, N/m
125 μm	40 μm	4 μm	320	40

3 Impact of polycrystalline metal gates and high-k dielectrics nanoscale fluctuations obtained with AFM related techniques on MOSFETs variability

The results of this chapter are reproduced and/or adapted from:

- ⋆ *A. Ruiz, N. Seoane, S. Claramunt, A. Garcia-Loureiro, M. Porti, C. Couso, J. Martin-Martinez, M. Nafria, "Workfunction fluctuations in polycrystalline TiN observed with KPFM and their impact on MOSFETs variability", Appl. Phys. Lett. 114, 093502 (2019).*
- ⋆ *A. Ruiz, N. Seoane, S. Claramunt, A. García-Loureiro, M. Porti, M. Nafria, "Combined nanoscale KPFM characterization and device simulation for the evaluation of the MOSFET variability related to metal gate workfunction fluctuations", Microelectronic Engineering, 216, 111048 (2019).*
- ⋆ *A. Ruiz, C. Couso, N. Seoane, M. Porti, A.J. García-Loureiro, M. Nafria, "Methodology for the simulation of the variability of MOSFETs with polycrystalline high-k dielectrics using CAFM input data", IEEE Access, Volume 9, pp. 90568 – 90576 (2021).*

In the last years, many studies have been devoted to investigate how variability sources as Random Dopant Distributions [165–167], Line Edge Roughness [74, 168], high-k dielectric polycrystallization [78, 126, 128, 169, 170] and metal polycrystallization [30–32] affect ultra-scaled MOSFET technologies. This variability sources can change the properties of scaled devices and increase the device-to-device variability. Charges captured in traps [89, 171, 172] located at the semiconductor/insulator interface can also lead to fluctuations in the threshold voltage (V_{TH}) and the on-current [173, 174] of the device, introducing, therefore, device-to-device variations. Such V_{TH} fluctuations also depend on the position of the traps along the channel [174].

Regarding metal gates, the metal polycrystallization results in grains with different sizes and orientations, which have associated different work functions (WFs). The random distribution of grains (and the corresponding WF) results in V_{TH} variability [30–32]. Some works have already analyzed the impact of the WF fluctuations in metals on the variability of MOSFETs [30, 31]. However, the statistical models that were used make assumptions that might not be representative of real devices. In this chapter (section 3.1), a more realistic approach which relies on 2D experimental WF maps obtained by Kelvin Probe Force Microscopy (KPFM) is proposed to study the impact of metal polycrystallization on the electrical parameters of MOSFETs. From KPFM measurements, the metal gate WF fluctuations are determined on the nanoscale. This information is then introduced into a device simulator to analyze the impact of metal granularity on the variability of the device electrical properties. These results are compared to those obtained using the approximated WF distributions normally used in customary approaches for this kind of variability source. An analysis of the influence of the location of the WF fluctuations along the channel is also studied.

Finally, since high-k polycrystallization also affects the MOSFET variability, in this chapter (section 3.2), a simulation methodology, whose inputs are Conductive Atomic Force Microscope (CAFM) experimental data, is proposed to evaluate the impact of nanoscale variability sources related to the polycrystallization of high-k dielectrics (i.e., oxide thickness, t_{ox}, and charge density, ρ_{ox}, which happen at the nanometer range) on the MOSFET variability. To simulate this variability, a Thickness And Charge MAp Generator (TACMAG) has been developed and used in combination with an device simulator. From CAFM experimental data (topography and current maps) obtained on a small area of a given polycrystalline dielectric, the TACMAG generates a high amount of t_{ox} and ρ_{ox} configurations of the gate dielectric, with identical statistical characteristics to those experimentally measured. These dielectrics are then introduced into the device simulator, with which the impact of the t_{ox} and ρ_{ox} fluctuations on the variability of MOSFETs (i.e., V_{TH}) is analyzed.

3.1 Impact of metal gate workfunction fluctuations on MOSFETs variability

As discussed in Chapter 1, the continuous scaling of the MOSFET has led to the use of different materials for the gate stack, such as high-k dielectrics and metal gates [175,176]. However, depending on the growth temperature, the metals become polycrystalline, giving rise to grains with different orientations and sizes. Since the WF of the grains varies as a function of their orientation [177], the distribution of grains affect the average WF of the gate and the V_{TH} [30–32,178,179] of the device.

Some works have already studied the impact of the WF variation due to grain orientation on the MOSFET variability. For example, in Ref. [32] the effects of crystal structure and grain size in metal gates on V_{TH} variability were investigated experimentally showing that the V_{TH} variability of a MOSFET is affected by the grain size. However, since this study was performed at the device level, the individual impact of the WF variability on the device properties cannot be separated from other sources as random dopant fluctuation (RDF) or line edge roughness (LER). Other works have evaluated the variability of the V_{TH} through simulation and statistical models that make assumptions that could be unrealistic [30, 31] as they use discrete and homogeneous values of WF in a grain and do not consider the effect of grain boundaries.

In this section, some experimental measurements are presented, which combined with simulations, allow to obtain a deeper picture of the physical phenomena that occur in the devices. In particular, 2D experimental maps are obtained at the nanoscale using KPFM. All the information collected experimentally is entered into a device simulator to analyze the impact of the metal granularity on the variability of the MOSFET V_{TH}. This analysis, since its based on experimental data, provides a more realistic approach of the phenomenon under study. This is demostrated by comparing our results with those obtained using the approximated WF distributions that are used in the usual approaches.

3.1.1 Samples and measurement equipment

In this section, a TiN layer (100nm thick) grown over a HfO_2/Si substrate was used to obtain the experimental data (Fig. 3.1). The metal layer was fabricated by continuous e-gun evaporation of metallic TiN. The TiN formation was ensured by passing the Ti atoms through a reactive nitrogen-enriched atmosphere (nitrogen partial pressure of 8x10^4mbars). The structure of the TiN layer was determined by X-Ray Diffraction (XRD) using a PANalytical X'PERT PRO with the CuK^{α} line in BraggBrentano geometry.

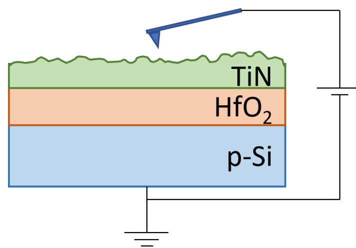


Figure 3.1: Schematic of the device structure.

The nanoscale morphological and electrical properties of the TiN layer were measured with a Nano-Observer AFM from Concept Scientific Instruments (see section 2.6). This technique allows bimodal single pass AM-KPFM measurements, so that it is possible to obtain during the same scan topographical and sample-tip contact potential difference (CPD) 2D maps with nanometer resolution [25, 180]. Compared to a lift mode based AM-KPFM (normally with a worse resolution [152–154]), our bimodal single pass AM-KPFM can provide a similar resolution to that obtained with a FM-KPFM [152–154, 181] and minimizes cross-talk between topography and the CPD data [153–155, 181].

In our case, the first resonant frequency has been used to track the topography (61.3kHz), while to measure the contact potential, the second resonant mode has been considered (380kHz). Note that it is high enough to avoid any dependency of the KPFM signal with frequency [182]. An internal algorithm selects the working frequency that maximizes the signals used to nullify the electrically driving oscillation, improving the sensitivity of the measurements. Since the ratio f_2/f_1 is typically

6.2, self-excitation of the second eigenmode through the 6th-harmonic of the first eigenmode is not present in the measurements, minimizing cross-talk between topography and the CPD image [155]. To measure the CPD image, we have biased the tip at V_{AC} = 1V, while keeping the TiN layer connected to ground. KPFM images were obtained with highly doped Si tips to get a better resolution.

Since the CPD image corresponds to the WF difference between the tip and the sample, assuming a constant value of the tip WF during the test, the measured CPD fluctuations can be related to the WF variations of the TiN layer. Therefore, CPD maps obtained with KPFM allow us to get information of the local value of the WF of the metal layer.

3.1.2 Experimental results

A. Impact of WF fluctuations on V_{TH} variability

The experimental data obtained at the nanoscale with KPFM are shown in Fig. 3.2(a) and 3.2(b). Figure 3.2(a) shows the topographical image of the TiN layer. Note that it shows a granular structure, which can be attributed to the polycrystallization of the metal layer: grains (Gs) are related to individual (or a cluster of) randomly oriented nanocrystals separated by grain boundaries (GBs, depressions in the topographical image) [128]. A statistical analysis of the Gs diameter is shown in Fig. 3.3(a). Figure 3.3(a) shows a histogram of the grain diameter with an average diameter ($G_{diameter}$) of ∼25.4nm. These results are compatible with values already reported, which point out a large range of diameters, depending on the growth conditions of the layer [30, 31].

The impact of the polycrystalline structure on the nanoscale WF of the layer was analyzed from the CPD image. Figure 3.2(b) shows the measured WF in the same surface region as in Fig. 3.2(a), suggesting that the WF is not uniform. A granular pattern, as also observed in Ref. [183], overlaps with that of the topographical image. Since the tip WF is not known and absolute values of WF are also very sensitive to ambient conditions [182], it has been assumed that the average value of the CPD image is 4.22 eV, which corresponds to the average WF of a TiN metal gate obtained from experimental devices [184], and only relative variations will be

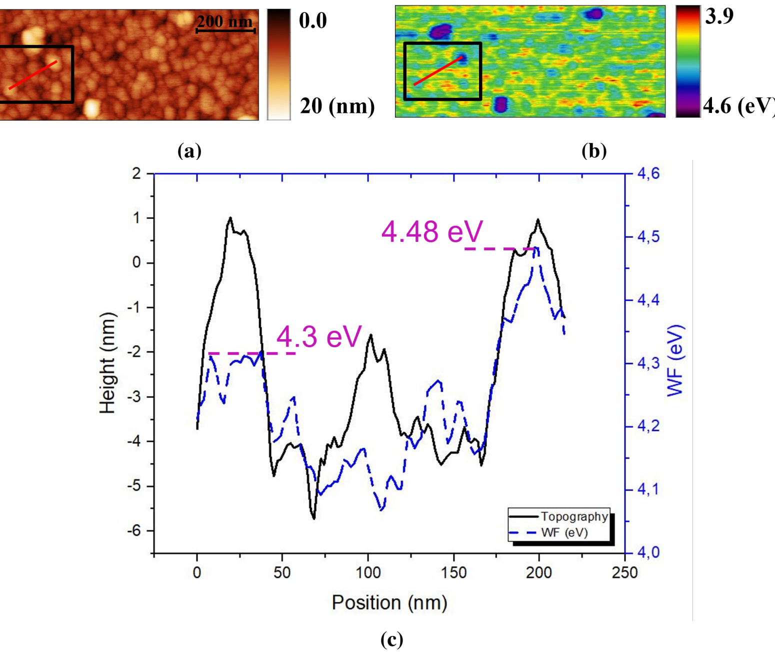


Figure 3.2: Topography (a) and WF (b) maps obtained by KPFM on a TiN layer (850nm x 290nm). (c) Topographical (continuous line) and the WF (dashed line) profile across the line plotted in (a) and (b).

considered. It is important to emphazise that this assumption does not affect the conclusions since we are only interested on the effect of the WF variations on the MOSFET variability, not on its absolute value.

By comparing images 3.2(a) and 3.2(b), one can see that there seems to be a correlation between the granular structure and the WF value. This is shown in Fig. 3.2(c), which corresponds to a topographical (continuous line) and a WF (dashed line) profile across the line plotted in Figs. 3.2(a) and 3.2(b) (inside the black square). Note that, in general, the positions with lower WF are located along the topographical depressions, though Gs with very low WF can also be found. This qualitative observation is verified statistically in Fig. 3.3(b), where the dependence of the WF with the Z-axis relative position (Z_{rel}, defined as the Z-position with respect to the Z-axis mean value of the image, which has been arbitrarily considered to be the zero-reference level) of all the pixels in Fig. 3.2 is plotted. The color scale

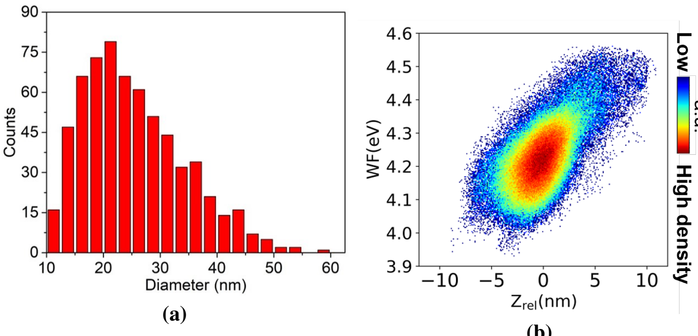


Figure 3.3: (a) Histogram showing the distribution of the nanocrystal diameter. The average diameter is 25.4nm. (b) Relationship between the WF and the topography (Z-axis relative position, Z_{rel}) map pixel by pixel. The color map shows the density of points for each region. Z_{rel} is defined as the Z-position with respect to the Z-axis mean value of the image, which has been arbitrarily considered to be the zero- reference level. The general trend is that depressed areas (regions with low Z_{rel}) show a lower WF.

of Fig. 3.3(b) shows the density of sites for a given WF and Z_{rel}. Figure 3.3(b) shows that, instead of discrete WF values, there is a continuous WF distribution that spans from ∼4.0 eV to ∼4.5 eV. The depressed areas (low Z_{rel}) tend to show a lower WF than hillocks. Since depressed regions correspond to GBs [see Figs. 3.2(a) and 3.2(c)] [128, 183], the results indicate that GBs tend to have a lower WF value than grains.

Note also that, besides the WF difference between GBs and Gs, the WF of Gs shows a continuous distribution. This distribution can be associated with, on the one hand, a non-homogeneous WF in the G or intra-G variability [see, for example, the G located at ∼200 nm in Fig. 3.2(c)] and, on the other, to differences in the WFs between Gs (inter-G variability). To analyze this inter-G variability, we have used the maximum value of WF as a parameter (if the average WF had been considered instead the same conclusions would have been drawn). Grains with different maximum WF values are measured, as in Ref. [183]. As an example, in Fig. 3.2(c) two Gs with a similar height and different maximum WF values (4.30 and 4.48 eV), whose difference is 200 meV are shown. These data are compatible with the presence of two grain orientations, [111] and [200], with 0.2 eV (Ref. [30]) WF difference. The presence of crystals with 2 different orientations is further supported by XRD analysis. The XRD spectrum of the TiN layer (see Fig. 3.4) shows two

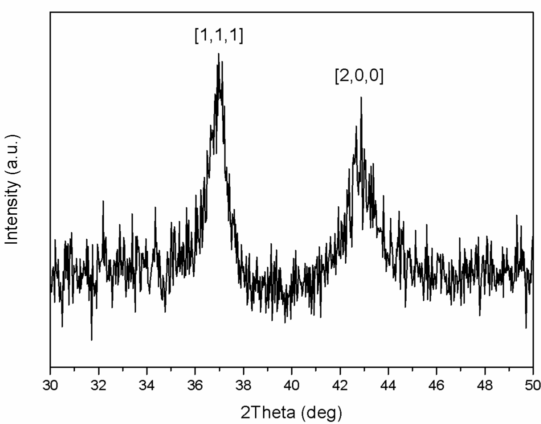


Figure 3.4: XRD spectrum of the TiN layer, showing the [111] and [200] orientations of TiN.

peaks, which correspond to the orientations mentioned above, the [111] orientation being dominant over the other. However, the KPFM map suggests a continuous distribution of values that spans from ∼4.29 eV for low WF values to ∼4.5 eV for high WF values [183], within the WF range of the two crystal orientations. A continuous distribution of WFs is also observed in the GBs. In this case, however, WFs range from 4.0 to 4.1eV, so the WF difference between grains and GBs ranges between ∼200 meV and ∼500 meV.

The results obtained until now from KPFM maps provide new data on the properties of the polycrystalline metal layer compared to those used in previous works to simulate WF variability. Besides the presence of different grain orientations, we have measured that they do not show discrete WF values but a continuous range of them (due to inter- and/or intra-G variability). Moreover, the presence of GBs with lower WF values is also observed (which were not considered in previous works). Such variations could also impact on the electrical characteristics and the variability of semiconductor devices and therefore should be taken into account. In order to demonstrate this, the nanoscale data experimentally obtained by KPFM have been introduced in a device simulator in order to study the variability of MOSFETs because of the WF fluctuations of the TiN layer.

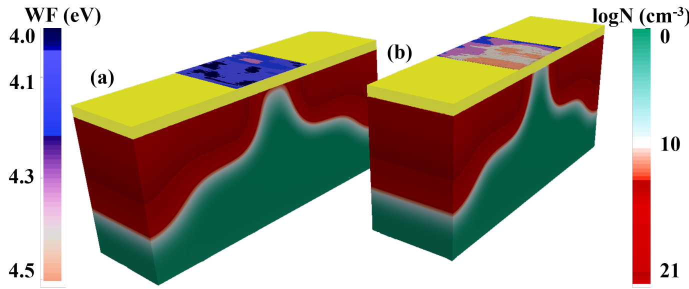


Figure 3.5: TiN metal gate experimental profiles that produce the highest (a) and the lowest (b) off-currents when considered as the metal gate of a 50nm gate length Si MOSFET. The electron concentration inside the device, at V_G = 0.0V and V_D = 50mV, is also shown.

To study the effect of the nanoscale WF fluctuations on the device electrical characteristics, a 3D in-house built finite-element drift-diffusion device simulator [185] was used. For simplicity, a W x L = 50x50nm^2 gate area n-type Si MOSFET with a HfO_2/SiO_2 gate stack was considered. The gate WF value (4.22 eV) and source/drain doping were obtained from the appropriate scaling and calibration of a 67nm effective gate length MOSFET experimental device [184]. From maps as those shown in Fig. 3.2, 100 different 50nm x 50nm metal gate maps were obtained and introduced in the device simulator, so that a set of 100 different WF maps (and therefore, device configurations) were studied. In Fig. 3.5, 2 extreme examples of device configurations are shown. Figure 3.5(a) corresponds to a device with very low TiN WF values (mainly occupied by GBs), while Fig. 3.5(b) corresponds to a device mainly occupied by Gs with WF values ranging from ∼4.29 to ∼4.5 eV. The corresponding statistical analysis of 100 MOSFET electrical characteristics is presented in Fig. 3.6 for the off-current (I_{off}), the subthreshold slope (SS), the threshold voltage (V_{TH}), and the on-current (I_{on}). The mean value and the standard deviation (σ) of the distributions are also indicated in this figure. All simulations were obtained at a low drain bias of 50 mV. Note that the V_{TH}, I_{off}, and SS histograms are not symmetric with behaviors far from the commonly assumed Gaussian distributions, with skewness values $\sim \pm 1$, because of the unbalanced grain WF probabilities. A correlation between G/GB distributions and electrical characteristics of the

device can be found, showing, for example, that higher values of the WF [as in Fig. 3.5(b)] lead to MOSFETs with higher V_{TH} and lower I_{off}. Then, from the I_{off} and V_{TH} histograms in Fig. 3.6, it can be concluded that the probability of occurrence of Gs with extremely high WF values (4.5 eV) is extremely low.

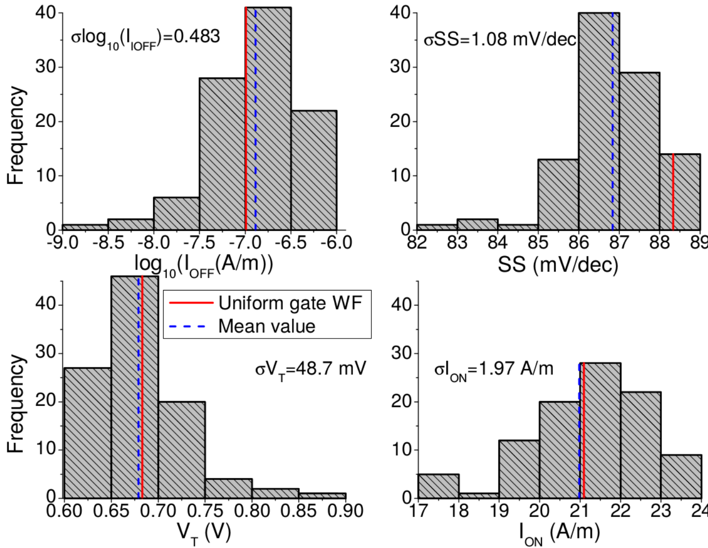


Figure 3.6: Distributions of I_{off}, SS, V_{TH}, and I_{on} due to the experimentally observed WFV for a 50nm gate length Si MOSFET at a drain bias of 50mV. The mean value and the standard deviation (r) of the statistical ensembles are indicated, together with the values obtained for a device with a uniform gate WF (set to 4.22eV).

We have compared our results with others obtained in previous works, as for example, in [186]. To perform a fair comparison between our WF variability results and those previously published in [186], corresponding to a 35nm gate length (GL) MOSFET, the ratio $G_{diameter}$/GL has been used [187]. When comparing results with a similar $G_{diameter}$/GL value of 0.5, our predicted σV_{TH} ($\sim$49mV) is around 10% lower than that reported by Wang. These large variability values explain why WF variability is currently considered as one of the major sources of variability that impact the device's performance. However, most of the previously TiN WF variability studies [186–189] consider that TiN has only two possible WF values spanning 0.2eV with probabilities of occurrence of 60% and 40% [190]. Our results show

that this hypothesis is quite simplistic since in real metals GBs may be present. We have observed a maximum excursion in V_{TH} values of 0.28 V (see Fig. 3.6), the mean V_{TH} of the distribution being 0.68 V, a value lower than the one obtained for a device with a gate composed only of Gs with extreme low WF values of 4.29 eV (0.75 V). This result suggests a huge influence of the GBs (with WF values ~4.0 eV) in the statistical distribution. Note that the gate of the device that exhibits the highest off-current [see Fig.3.5(a)] is mainly occupied by GBs and Gs with WF values ranging from ~4.0 to ~4.3 eV. Therefore, the influence of the GBs should not be ruled out when metal gate WF variability wants to be modeled.

B. Comparison between aproximated models and experimental data

Although the results shown in the previous section suggest that the models used until now may be unrealistic, our data have been compared with results of other works obtained on different devices and/or materials. To further verify the impact of the presence of GBs and the WF continuous distribution in metal gates, we have gone one step beyond and we have compared our experimental results with those that we would obtain using the approximated WF distributions normally used in customary approaches.

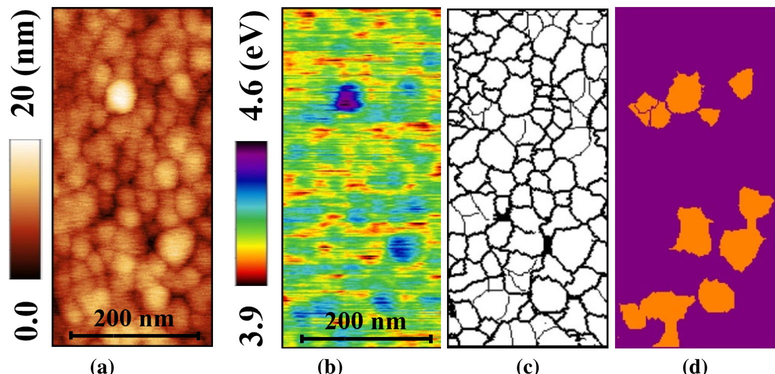


Figure 3.7: Topography (a) and WF (b) maps obtained with KPFM on a TiN layer. Binary mask (c) of the grains identified in the topographical map and an example of generated WF map (d) from the binary mask. Orange color corresponds to 4.5eV and purple color to 4.3eV.

The starting point of this analysis is, again, the experimental data we have obtained with KPFM. Figure 3.7(a) shows a 520 nm × 240 nm topographical image of the same TiN layer. Note again its granular structure, with Grains (Gs) surrounded by grain boundaries (GBs). Figure 3.7(b) shows the measured WF map of the same surface region. These images will be considered the starting point to evaluate the impact of polycrystalline metal gates on V_{TH}, taking into account, on one hand, raw experimental data as that obtained in Fig. 3.7, and, on the other hand, different approximations that will obtained from the same images.

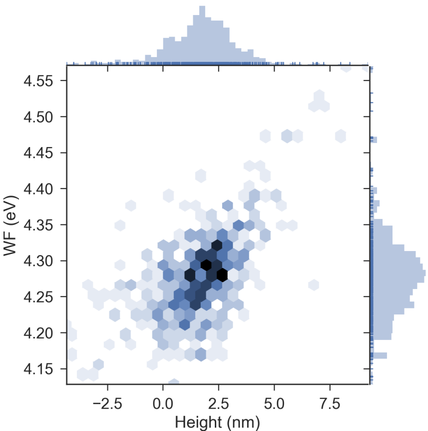


Figure 3.8: 2D-histogram showing the maximum WF vs maximum height of the grains, obtained from Fig. 3.7(c). In the X axis, the height of each grain is determined with respect to the mean value of the topographical image (Fig. 3.7(a)).

To obtain the different approximations, the open-source software Gwyddion [191] was used. Gwyddion was first used to identify the Gs and obtain the TiN granular pattern (Fig. 3.7(c)), where the GBs have not been considered. When only nanocrystals are taken into account, Gs with different maximum WF values are measured, as shown in Fig. 3.8, which corresponds to a 2D-histogram that relates the maximum WF and the maximum height (with respect to the mean height value of the topographical image shown in Fig. 3.7(a) Z_{rel}) of each grain in Fig. 3.7(c). Note that although a continuous distribution of maximum WFs is obtained, WFs are mostly concentrated at ∼4.3 eV and, with less frequency, around ∼4.5eV, suggesting two

predominant WFs and indicating a much higher number of nanocrystals with low WF than with high WF. This result, supported by XRD analysis (Fig. 3.4) [192], is compatible with the presence of two grain orientations in the TiN layer ([111] and [200]) as it was previously explained, whose WFs are separated by 200 mV [30].

In order to evaluate the device variability associated to the WF fluctuations of the TiN layer, different WF distributions representing the metal gate of a MOSFET were considered. WF images as those shown in Fig. 3.7 have been divided to generate 100 non-overlapping 50nm $\times$ 50nm gate WF profiles. Next, these profiles were introduced in a 3D in-house-built drift-diffusion device simulator [22] as metal gate, to evaluate the device electrical characteristics of MOSFETs with a gate area of $50\times50\text{nm}^2$. In order to compare the results obtained with our methodology, based on nanoscale experimental data, with those shown in the literature, we proposed the study of two cases: (i) the real WF distribution (as in Fig. 3.7(b), with GBs and a continuous distribution of Gs WF), and (ii) an approximated WF distribution, with two discrete values of the WF, as in Fig. 3.7(d). Note that the last is the customary approach for this kind of V_{TH} variability source [30]. To generate the approximated WF maps (Fig. 3.7(d)), the grain pattern in Fig. 3.7(c) is the starting point. We generated an approximated WF maps where GBs have been neglected and, for the Gs in Fig. 3.7(c), two discrete and constant values, corresponding to the [111] and [200] orientations, were only taken into account. We have assigned 4.3 eV to the nanocrystals with WF lower than 4.4 eV and 4.5 eV to those with higher values, leading to WF maps as those shown in Fig. 3.7(d). The MOSFET behavior for devices with metal gate WF distributions obtained from the WF maps as in Fig. 3.7(b) and (d) have been compared.

The results are shown in Fig. 3.9 and a summary in Table 3.1. Figure 3.9 corresponds to the off-current (I_{off}), threshold voltage (V_{TH}) and on-current (I_{on}) distributions obtained for these two cases. It is important to emphasize that, the approximate case (i. e., ruling out the GBs and the WF continuous distribution), in the right column, leads to a $\sim$10% and $\sim$18% reduction in σV_{TH} and $\sigma\log(I_{off})$, respectively, and to a considerable shift ($\sim$0.12 V in the case of the V_{TH}) in the mean value of the distributions. Note that we have compared the same granular pattern in both cases. Since the only difference is that, in one case, we have used the approximated

model and, in the other, experimental direct data obtained with KPFM was considered, the difference obtained in V_{TH} can be related to the fact that, the approximated model, is less realistic. Therefore, our results demostrate that our procedure is a more realistic approach for the analysis of the device-to-device variability (due to the presence of different grain orientations) since nanoscale differences of the metal WF are extracted from experimental data.

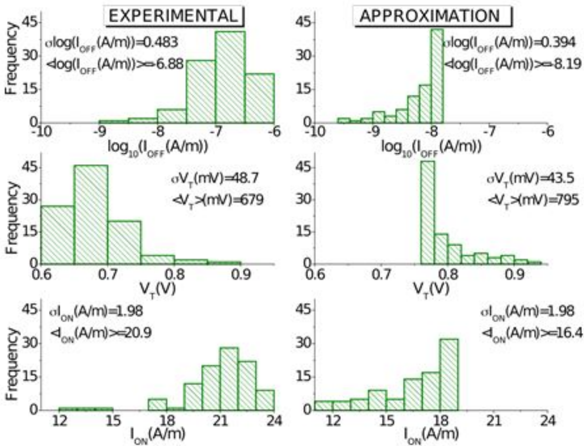


Figure 3.9: Distributions of I_{off} (top), V_{TH} (middle) and I_{on} (bottom) related to WF fluctuations in 50nm $\times$ 50nm Si MOSFETs (at a drain bias of 50mV) when using actual WF data (left column) an approximated WF (right column) from maps as those shown in Fig. 3.7(c) and (d) respectively. The mean value ($<\ >$) and standard deviation (σ) of the statistical ensembles are shown.

Table 3.1: The mean value and standar deviation (SD) of I_{off}, I_{on} and V_{TH} related to WF fluctuations using the experimental and approximated data.

	Experimental		Approximation	
	Mean <>	SD σ	Mean <>	SD σ
I_{off} (A/m)	6.88	0.483	8.19	0.394
I_{on} (A/m)	20.9	1.98	16.4	1.98
V_{TH} (mV)	679	48.7	795	43.5

C. Impact of WF fluctuations position along the channel on V_{TH}

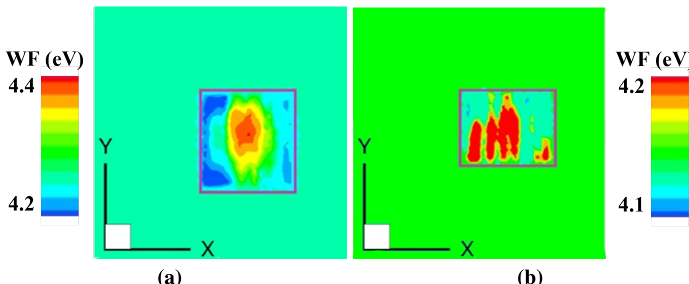


Figure 3.10: Two examples of isolated nanocrystals (enclosed in pink rectangles), with average WF values $< WF >$ of 4.3 eV, grain (a), and 4.18, grain (b). The larger green squares show the real dimensions of the 50×50nm device gate.

In [171] it was demostrated that the presence of charge in the gate dielectric of a MOSFET can affect V_{TH}. Not only that, but V_{TH} is also sensitive to its position along the channel [171]. If this is true, the position of WF fluctuations in metal gates could also affect the V_{TH} of a MOSFET. This is what we are going to investigate in this section. As an example, Fig. 3.10 shows the gate of two devices in which only one nanocrystal has been included. The average WF of the grains is 4.3eV for grain (a) and 4.18eV for grain (b). Since, in this section, we want to evaluate only the impact on V_{TH} of the position of the grains in the channel, the WF of the portion of the gate not covered by the nanocrystal has been set to same average value, that is, 4.3eV for Fig. 3.10(a) and 4.18eV for Fig. 3.10(b). The G has been swept along the device gate, from the source end (X=0nm) to the drain end (X=50nm), and for each position of the grain, the device was simulated and the corresponding V_{TH} extracted. Fig. 3.11 shows the V_{TH} variation with respect to the homogeneous case when the grain position is swept for the two cases shown in Fig. 3.10, at both low (red) and high (black) drain biases. Note that, although the distribution of WF is the same in all cases, the position of the G has a different effect on the V_{TH} values (depending on its position along L), leading to both positive and negative threshold voltage shifts with respect to the grain average WF value. Note also that, the device is clearly more sensitive to WF variations at the source electrode than at the drain electrode (as seen in Fig. 3.11 for both grains). At the drain end, the presence of

the grain does not have any influence on V_{TH}. The drain bias also has an influence on the V_{TH} variability, as seen on Fig. 3.11. We have also analyzed the effect of moving the grain along the width of the channel, but no significant changes of V_{TH} have been measured.

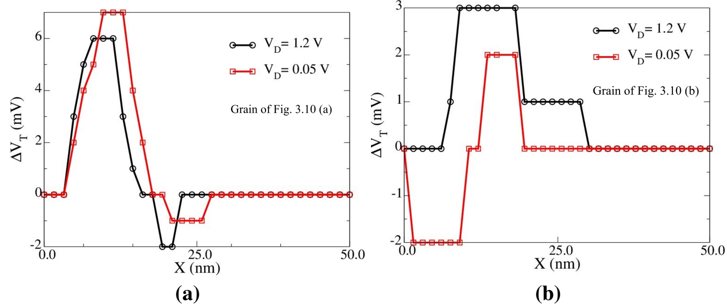


Figure 3.11: V_{TH} spatial sensitivity to a TiN grain WF fluctuations when its position is swept along the channel of the Si MOSFET at both low and high drain biases like those shown in Fig. 3.10(a) and (b) have seen considered for the simulation. ΔV_{TH} is calculated as the difference between the V_{TH} of a device with a gate WF equal to the $<WF>$ of the G and the V_{TH} of the device that includes the nanocrystal.

Therefore, the results demonstrate that, not only the WF values of the grains in the metal gate can impact on the MOSFET variability, but also V_{TH} depends on how those fluctuations are distributed along the channel direction. The dependence of V_{TH} on the G position can be explained taking into account the impact of the WF fluctuations on the electrostatics of the device. Depending on the G location, the potential distribution in the channel is affected differently, leading to variations of V_{TH}.

So, to conclude this section, we have demostrated that, when analyzing the impact of the WF fluctuations of polycrystalline metal gates on the MOSFET variability, the presence of GBs and the WF continuous distribution of the Gs need to be considered to obtain more realistic data. Moreover, the device characteristics and variability are also affected by the spatial distribution of such fluctuations: in small devices, where few nanocrystals may be present in the gate area, their location along the channel also may affect the electrical properties of the device.

3.2 Metodology for the simulation of the variability of MOSFETs with polycrystalline high-k dielectrics using CAFM input data

Many studies carried out with CAFM have shown that this technique is a very powerful tool to evaluate the morphological and electrical properties [124, 193–196] of polycrystalline high-k dielectrics [25,78,123,197]. As an example, it was found that in some polycrystalline layers of hafnium dioxide (HfO_2), the gate leakage current flows mainly through grain boundaries (GB) [130], where the oxide thickness (t_{ox}) was thinner [128]. In addition, the presence of defects have been observed in GB, which have been associated with an excess of oxygen vacancies [128, 130].

Due to the lack of experimental data, variability studies have been performed by implementing physical models that pretend to reproduce the real behavior of the sources of fluctuations [186, 198, 199]. However, more recently a new methodology has been proposed [78] which is based on the simulation of the I-V curves of MOSFETs whose gate oxide properties were directly determined from experimental data. In this way, it was possible to better link variability sources at the nanoscale with the variability of MOSFET parameters. In [78], a CAFM was used to measure topographical and current maps of polycrystalline high-k dielectrics. From these maps, the nanoscale t_{ox} and charge density, ρ_{ox} maps were obtained. Then, using this information as input, a simulator was used to evaluate their impact on the MOSFET V_{TH}. However, in that work, a statistical analysis was not possible. Only small regions of a particular sample were measured, so that the number of devices available for the analysis of the variability of the MOSFETs figures of merit was rather limited. Moreover, the complete evaluation of the impact of the different parameters that describe the polycrystallization of high-k dielectrics (as the grain size, Grain Boundaries depth and/or width, etc) was not allowed. On one hand, because samples obtained with other growth parameters (which result in different polycrystallinity properties) are not always possible. On the other, because it would be necessary a lot of experimental measurements, which is very time consuming and expensive.

To solve these limitations, in this section we propose a complete simulation flow to statistically evaluate the impact of polycrystalline high-k dielectrics on the MOSFET variability, starting from experimental nanoscale data obtained with a CAFM. In particular, topographical and charge density maps of polycrustakkube HfO_2 with identical structural parameters as those expermientally measured and simulated.Thus they are introduced in a device simulator evaluate its impact on the device properties. With our methodology, less experimental measurements and samples with different characteristics are needed, reducing the cost and time of such analysis. At this point, only the high-k polycristallinity is considered as variability source, but it could be afterwards combined with others to investigate their global effect on the device [200].

3.2.1 Experimental

Setup and device structure

In this section, a 5.3nm thick HfO_2 film deposited by atomic layer deposition (ALD) on a 0.7nm thick SiO_2 layer was used. The average thickness of both layers was measured by X-ray reflectivity. The gate stack was grown on a P-epitaxial Si substrate. In order to study the impact of the polycrystalline dielectric structure on the variability of the MOSFET device, an annealing process was carried out at 1000°C, which led to the polycrystallization of the high-k layer. The presence of the

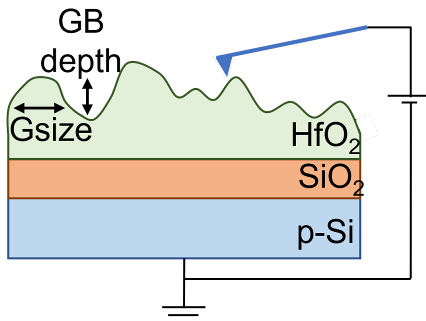


Figure 3.12: Schematic of the set up and device structure.

SiO_2 layer was taken into account during the TCAD simulations, as reported in the work [78]. However, the SiO_2 charges and tox fluctuations in SiO_2 were considered negligible compared to those associated with the high-k polycrystalline dielectric. This is justified by the fact that SiO_2 is not polycrystalline and because the number of charges is expected to be higher in HfO_2 than in SiO_2. Therefore, the measured t_{ox} and ρ_{ox} fluctuations are assumed to be related to the high-k polycrystalization.

The experimental setup used for the CAFM measurements is show in Fig. 3.12. Note that no top electrode is used. Therefore, the CAFM tip plays the role of the upper electrode, defining a MOS structure with an area that is the contact area between the tip and the sample. This area has been estimated to be $\sim$100nm^2 [201]. With this experimental setup, morphological and current maps can be measured at nanometer resolution. The current maps correspond to the tunneling currents flowing between the gate and the substrate, through the dielectric stack.

CAFM experimental data

The topographic and current map obtained on the HfO_2 sample described in the previous section is shown in Fig. 3.13(a) and 3.13(b). The current map was measured at 6.5V, in contact mode and using a diamond-coated silicon tip. From both maps, the charge density map has been determined using the methodology shown in [78] (Fig. 3.13(c)). If we pay attention to the morphology of the sample, it can be seen that the topography shows a polycrystalline surface where grain boundaries and grains can be distinguished. Note that direct information about the oxide thickness, t_{ox}, cannot be obtained from AFM images, because AFM only provides information about the top dielectric interface. However, the thickness of the HfO_2 layer at each surface site has been estimated assuming that the average thickness of the oxide layer measured by X-ray reflectivity (5.3nm) corresponds to the average height of the topographic map. Any height deviation with respect to the morphological average at any site of Fig. 3.13(a) has been attributed to a deviation from the average t_{ox} of the same value. Then, any morphological map can be interpreted also as a t_{ox} map. Figure 3.13(b) shows the current map corresponding to the topography (Fig. 3.13(a)), where the highest currents are measured in the GBs (depressions in Fig. 3.13(b)). Also, higher charge densisites, ρ_{ox}, are measured at the GBs, associated

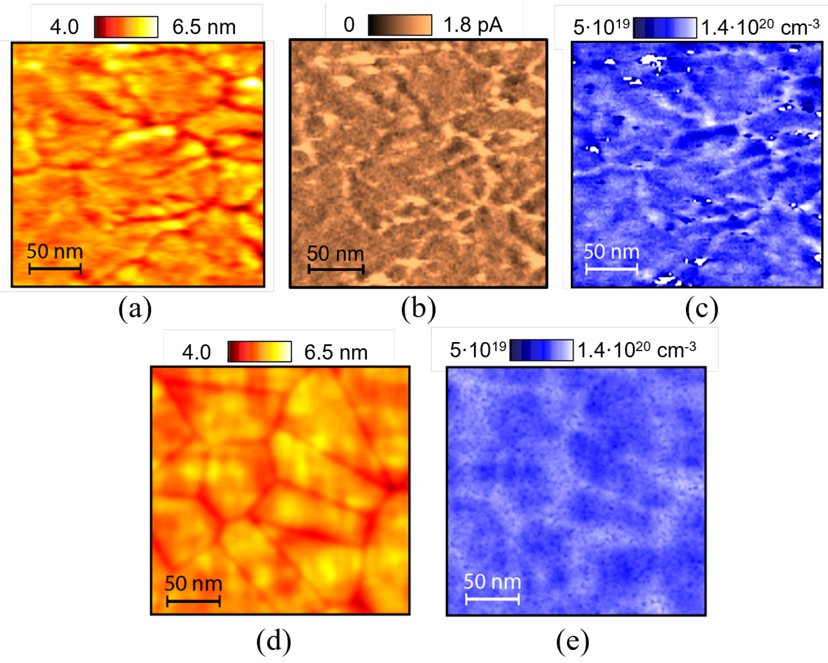


Figure 3.13: Morphological (a) and current (b) maps obtained at V_G=6.5V on a HfO_2/SiO_2/p-Si structure. (c) corresponds to the charge density map estimated from (a) and (b). Generated morphological (d) and and charge density (e) maps obtained with TACMAG.

to oxygen vacancies present at those sites. Note that a clear correlation between the three images is observed. The highest currents and charge densities are measured in GB (deeper areas on the morphological map).

3.2.2 Simulation tools

The proposed simulation methodology is based on two independent simulators that are executed sequentially. Fig 3.14 shows the complete flow of data, covering from the experimental information obtained with CAFM to the analysis of the variability of MOSFETs. Once the experimental (topography and current) information is obtained with CAFM, the TACMAG (Thickness And Charge MAp Generator) software is used, with which multiple maps (t_{ox}, ρ_{ox}) of gate oxides (output) are gen-

erated from the experimental morphological and current maps . Then a homemade semiconductor device simulator is used, which takes the output maps (t_{ox}, ρ_{ox}) of TACMAG as input data and simulates the electrical characteristics of the MOSFET. As a result, the impact of nanoscale fluctuations of t_{ox} and ρ_{ox} in the dielectric on device I-V characteristics and device-to-device variability in MOSFETs can be evaluated. In the next sections, both simulators are explained in detail.

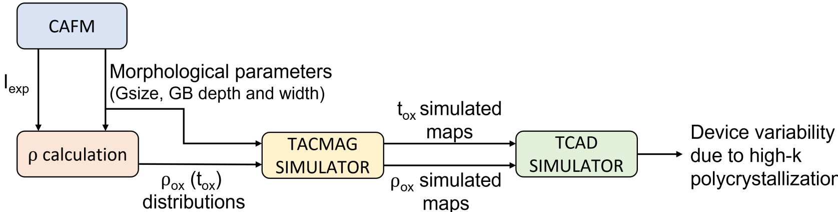


Figure 3.14: Flow diagram showing the different steps of the simulation methodology.

A. Thickness And Charge MAp Generator (TACMAG)

The starting point of this work was the generator developed in [202]. In that generator developed in [202], from the AFM measurement of morphological maps of a polycrystalline sample, 3 Dimension (3D) topographical maps could be reproduced with the same statistical morphological characteristics as the experimental sample under study [202]. Moreover, in [78], from pairs of experimental morphological and current maps obtained with CAFM (on the same area), the local charge density was also calculated at each position of the gate oxide. The present work, however, goes one step further, and improves and develops new capabilities of that simulator, called from now on TACMAG, which are necessary to evaluate the impact of the nanoscale properties on the variability of MOSFETs.

First, the methodology used to statistically reproduce the morphology of the sample has been improved, by using the Poisson-Voronoi diagrams, which are normally used to generate polycrystalline grain structures [203–205]. With this new technique, the inputs needed to create the grain structure of the samples are reduced, simplifying the generation of the map, so that only the grain size, width and depth of the grain boundaries are necessary. Figure 3.13(d) shows an example of a generated morphological map whose parameters correspond to those of the experimental topographic image.

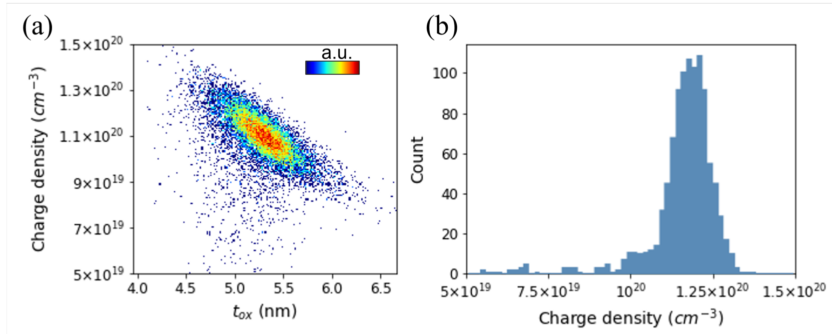


Figure 3.15: (a) ρ_{ox} values calculated from Fig. 3.13(a) and 3.13(b), and shown in Fig. 3.13(c) as a function of t_{ox} (Fig. 3.13(a)) for all the pixels of Fig. 3.13(a) and 3.13(c). The histogram on (b) shows the $\rho_{ox}(t_{ox})$ distribution for t_{ox}=5nm (interval between 4.95 and 5.05nm).

In addition, the new version of the generator (TACMAG) has also been extended to generate 2D charge density maps (i.e., the inputs of the Device simulator). To do that, first of all, from morphological and current maps experimentally obtained with CAFM (Fig. 3.13(a) and 3.13(b)), we use the methodology shown in [78] to calculate the corresponding ρ_{ox} map (Fig. 3.13(c)). Fig. 3.15(a) shows the calculated ρ_{ox} values (Fig. 3.13(c)) as a function of t_{ox} (Fig. 3.13(a)) for all the pixels of Fig. 3.13(a) and 3.13(c). Note that there seems to be a correlation between t_{ox} and its corresponding charge density (statistically, higher densities were found at GBs, which have smaller thicknesses). However, this relation is not univocal: for a given t_{ox}, a distribution of ρ_{ox} has been found. Fig. 3.15(b) also shows an example of a statistical distribution of charge for t_{ox} = 5nm (interval between 4.95 and 5.05nm). The ρ_{ox} (t_{ox}) statistical distributions have been determined and have been used as an input of the TACMAG to generate (t_{ox}, ρ_{ox}) maps of the dielectric. That is, for a given pixel of a generated morphological map (characterized by a given t_{ox}),the ρ_{ox} value has been determined by applying Montecarlo methods, considering the ρ_{ox} distribution found for that value of t_{ox}. As an example, Fig. 3.13(e) shows the generated ρ_{ox} map obtained for the morphological map in Fig. 3.13(d).

In summary, from the input morphological parameters (grain size, GB width and depth, and their statistics, obtained from morphological maps) and the current maps obtained with CAFM, TACMAG calculates the charge density distributions (ρ_{ox}, which depends on t_{ox}), and provides maps (t_{ox}, ρ_{ox}) in the output.

B. 3D Device Simulator

The 3D in-house built parallel drift- diffusion (DD) Device Simulator used to evaluate the impact of nanoscale t_{ox} and ρ_{ox} fluctuations in polycrystalline dielectrics on the device variability of MOSFETs is called VENDES [206] and allows obtaining the I_G-V_D characteristics of MOSFETs. For this, the finite element method (FEM) is used to discretize the simulation domain, allowing the simulation of complex device shapes with great flexibility. A more detailed description of the simulation methodology can be found in [206]. This 3D DD-DG simulator has been already used for modeling different sources of variability, such as random dopants [207], line edge roughness [208, 209] or metal gate granularity [184, 185, 207, 208].

In this thesis, this simulator has been used to study the impact of high-k dielectric polycrystallization on the V_{TH} variability of MOSFETs. With this purpose, a Width (W) x Length (L) = 50 $\times$ 50nm^2 gate area n-type Si MOSFET with a HfO_2/SiO_2 gate stack was considered as a test device. The device dimensions and doping values were obtained from the constant field scaling [210] of a n-type 67nm effective gate length MOSFET that was calibrated against experimental data [184]. To simulate the Drain current vs. Gate Voltage (I_D-V_G) curves of different devices, nanoscale (t_{ox}, ρ_{ox}) dielectric maps with a 50 $\times$ 50nm^2 size (the area of the gate region), have been obtained from Fig. 3.13, and have been considered as inputs of the Device Simulator. The introduced maps can be either directly measured (i.e, 50 $\times$ 50 nm^2 portions of Fig. 3.13(a) and 3.13(c)) or generated (in Fig. 3.13(d-e)).

Figure 3.16 shows some examples of simulated I_D-V_G curves. Figure. 3.16(a) shows a 3D picture of the electrostatic potential (cross section) and charge density (top of the image) for the two device configurations that lead to the largest (left figure) and lowest (right figure) drain currents (at V_G = 0.6V and V_D = 0.05V) when considering both ρ_{ox} and t_{ox} fluctuations in the device gate. Fig 3.16(b) shows, as example, a profile of the thickness of the high-k dielectric (continuous line).

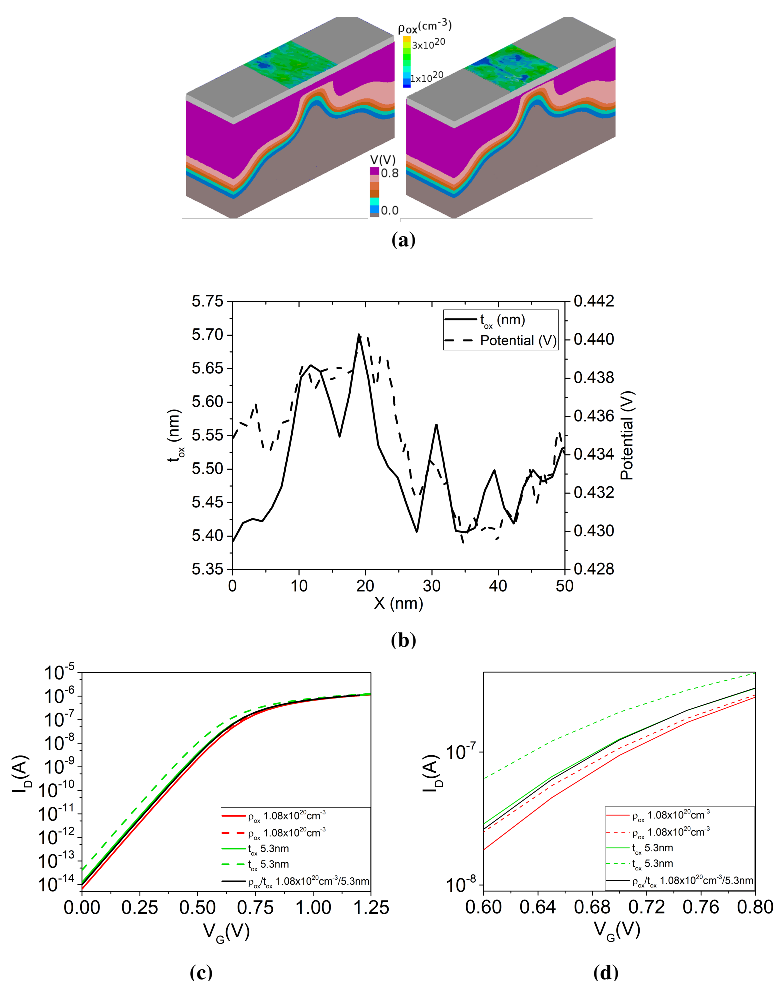


Figure 3.16: (a) Electrostatic potential inside the 50 × 50 nm^2 MOSFET device for the two particular configurations that produce the largest (left) and lowest (right) drain currents (at V_G = 0.6 V and V_D = 0.05 V) when considering both ρ_{ox} and t_{ox} fluctuations in the device gate. (b) Example of electrostatic potential in the channel (dashed line) and t_{ox} profile (continuous line), (c) I_D-V_G characteristics simulated at V_D = 50 mV for the two configurations shown in (a) when different variability sources are analyzed. Red curves correspond to the simulated I_D-V_G curves of devices with dielectrics with constant ρ_{ox} = 1.08 × 10^{20}cm^{-3} and with the t_{ox} fluctuations taken from (a). Green curves correspond to the simulated I_D-V_G curves of devices with dielectrics with constant t_{ox} = 5.3 nm and with the ρ_{ox} fluctuations taken from (a). Black curve corresponds to a device with constant ρ_{ox} and t_{ox} (same values as for the two other considered cases). (d) corresponds to a zoom of the I-V curves (c), showing V_G in the 0.6V to 0.8V range.

It has been extracted in the center of the channel perpendicular to the transport direction. The corresponding electrostatic potential inside the channel is also shown (dashed line). Note that the potential is not constant, but depends on the thickness fluctuations. In the regions with smaller thickness (related to GBs), the potential is lower. Since the presence of GBs is related to polycrystalline materials, the results demostrate that polycrystalization clearly affects the potential distribution along the channel. Fig. 3.16(c) shows the I_D-V_G curves at V_D = 50mV for the MOSFET configurations of Fig. 3.16(a) with different gate oxides characteristics. Figure 3.16(d) shows a zoom of the same plot, to better see that the I_D-V_G curves are different. First, the impact of t_{ox} and ρ_{ox} fluctuations have been separately evaluated, as unique nanoscale variability source. Red I_D-V_G curves in Fig. 3.16(c) correspond to two particular devices, characterized by gate dielectrics with constant ρ_{ox} = 1.08 $\times$ 10^{20}cm^{-3} (average charge density estimated from Fig. 3.13(c)). The t_{ox} fluctuations were introduced by considering the 50 $\times$ 50nm^2 regions of Fig. 3.16(a). Green I_D-V_G curves in Fig. 3.16(c) correspond to two particular examples of devices with constant t_{ox} = 5.3nm (average thickness) and two 50 $\times$ 50nm^2 ρ_{ox} maps corresponding to the configurations of Fig. 3.16(a). Finally, both sources are considered simultaneously. In this case, fluctuations in both, ρ_{ox} and t_{ox} parameters have been taken into account. The morphology of the dielectric corresponds to that of Fig. 3.16(a), with charge distributions following the same spatial pattern. For clarity, the resulting curves are not shown in Fig. 3.16. As reference, the I_D-V_G curve of the device with constant ρ_{ox} = 1.08 $\times$ 10^{20}cm^{-3} and t_{ox} = 5.3nm (black curve) has also been plotted in Fig. 3.16(c).

Note that the two I_D-V_G characteristics of each set of simulated devices show different conduction levels (see Fig. 3.16(c) and (d)). The different t_{ox} and ρ_{ox} distributions has lead to MOSFETs with different V_{TH} values. To extract V_{TH}, a constant current criterion was used. V_{TH} was chosen as the gate bias for which a drain current of 1.4A/m was obtained. With this criterion, V_{TH} is 0.664V/ 0.675V when ρ_{ox} is constant (red curves), 0.606V / 0.654V when t_{ox} is constant (green curves) and 0.628V / 0.678V when t_{ox} and ρ_{ox} fluctuations are considered, respectively. The V_{TH} of the device with constant t_{ox} and ρ_{ox} is 0.656V (black curve). From

these results, we can conclude that, first, ρ_{ox} and t_{ox} fluctuations lead to different MOSFET electrical properties, and, second, their impact changes when considered individually or combined.

Note that, the proposed simulation methodology is able to detect how nanoscale variability sources affect MOSFETs figure of merits, and also allow to study their individually or combined. It is also important to emphasize that the results shown in Fig 3.16(c) are only two particular cases. They do not correspond to a statistical analysis, which will be shown in next sections. However, before using our simulation tools to evaluate in more detail the impact of the high-k polycrystallization on MOSFETs V_{TH} variability, the TACMAG results representativeness must be first verified.

C. TACMAG verification

In this section, we are going to verify if TACMAG is capable of generating a statistically representative (t_{ox}, ρ_{ox}) set of maps for the sample of interest. To this end, the V_{TH} variability of MOSFETs, the dielectric characteristic of which have been obtained through the simulator (generated t_{ox}, ρ_{ox}) maps, has been compared to experimental obtained V_{TH}. To detail, from maps similar to those shown in Fig. 3.13; particularly we have used 100 different 50x50 nm^2 maps of each kind (see Figs. 3.13(a-c)/(d-e) for examples of the experimental/TCAMAG-generated maps used for the computation of V_{TH}) to set the gate oxide properties of the MOSFETs in a Device Simulator in order to obtain the information regarding VTH variability [211].

To verify if the TACMAG provides representative data of the analyzed sample for each of the considered variability sources (t_{ox} and ρ_{ox}), 3 different cases have been studied. First, t_{ox} was considered the single source of variability (being ρ_{ox} constant and equal to the average charge density found from Fig. 3.13(c), i.e. $1.08 \times 10^{20} cm^{-3}$), second, ρ_{ox} was considered the only source responsible for the variability (being t_{ox} constant and equal to 5.3nm, i.e. the measured average thickness of the sample) and, third, were both tox and rhoox are originating the varibility. For all the devices, the I_D-V_G characteristics were simulated and V_{TH} was estimated. The results of the statistical analysis of the V_{TH}, namely the mean and standard deviation

σV_{TH} are presented in Table 3.2. From these analysis, we can observe for all the cases an excellent agreement between experimental and simulated results. For a 100 devices sample size, the difference between σV_{TH} (indicative of the V_{TH} variability) of both kinds of devices is <2mV. As reference to the reader, this represents an error of 7.7% in the σ when both sources are considered. For the same case, the average V_{TH} difference is 17 mV, which corresponds to an error of 2.6%. Consequently, TACMAG maps both (t_{ox} and ρ_{ox}) accurately reproduce experimental results with a considerable precision. Therefore, the proposed simulation methodology and, in particular TACMAG, can be used for an accurate analysis of the variability of the MOSFETs figures of merit.

Table 3.2: Average and standard deviation of V_{TH} obtained from 100 devices with the device simulator, when the gate oxide characteristics have been set from experimental data (first row) and maps generated with TACMAG (second row). The different columns show the impact of the different nanoscale variability sources (t_{ox} and/or ρ_{ox}).

	V_{TH} (V)		
	Only t_{ox}	Only ρ_{ox}	t_{ox} and ρ_{ox}
Experimental	0.681±0.004	0.640±0.028	0.650±0.012
Generated	0.680±0.005	0.654±0.030	0.667±0.013

3.2.3 Impact of the HfO_2 polycrystallization on the V_{TH} variability

After the verifaction of our methodology, in particular of TACMAG, we have used the same to evaluate in more detail the impact of the polycrystallization of the HfO_2 layer on the V_{TH} variability of MOSFETs. Specifically, two cases of study have been considered.

A. Correlation between t_{ox} and ρ_{ox} on the impact on V_{TH} variability

In this section we have studied the impact of t_{ox} and ρ_{ox} fluctuations on V_{TH} and their relation (if any). In Fig. 3.15, a correlation between t_{ox} and ρ_{ox} was observed at the nanoscale from the analysis, the topographical and contact potential

images obtained with KPFM. Therefore, one could wonder if, when analyzing their impact on V_{TH}, the impact of both variability sources have some degree of correlation. Taking advantage of the versatility and capabilities of our simulation tools, the individual and combined impact of both variability sources has been carefully analyzed. Particularly, for this analysis, we have considered the data obtained with TACMAG (in Table 3.2, second row). Here note that, regarding the average value of V_{TH}, t_{ox} fluctuations have a higher impact (V_{TH} increases from 0.657V for the reference case to 0.680V) than ρ_{ox} variations (in this case it remains almost equal, changing only from 0.657V to 0.654V). Nonetheless, regarding the standard deviation, when both variability sources are analyzed independently, σV_{TH} due to ρ_{ox} is 6 times larger than that attributable exclusively to t_{ox} (30mV and 5mV, for the ρ_{ox} and t_{ox} case, respectively). Therefore, in the samples under the scope of this work, we can conclude that charge density fluctuations lead to larger V_{TH} variability than those related to the gate oxide morphology. Nevertheless, it is also worth comenting that when both variability sources are combined, the V_{TH} deviation falls within the values obtained from independent sources approach. Indeed, the global V_{TH} deviation does not correspond to the expected addition of independent variability sources, but it is reduced when compared with the impact of ρ_{ox}. These results indicates that ρ_{ox} and t_{ox} effect on V_{TH} are correlated (as suggested in Fig. 3.15) and their fluctuations are somehow compensated.

Consequently, the correlation between both sources has been carefully analyzed to gain an insight of the obtained results. To that end, Fig. 3.17 shows the probability plot (color scale), obtained from the data shown in Table 3.2 (second row, generated maps, first and second columns) of finding devices with V_{TH}'s related to t_{ox} variation only (X-axis) and V_{TH}'s related to ρ_{ox} variation only (Y-axis). Note that, for a given value of V_{TH} in the X axis (i.e., only t_{ox} fluctuations), a distribution of different V_{TH} values in the Y axis (i.e., only ρ_{ox} variations) is observed. This last, which can be seen as an inclination in the probability distribution, indicates that both variability sources are not independent when analyzing their impact on the V_{TH} of devices. Therefore, to quantify this correlation, the data shown in Fig. 3.17 has been fitted to a bivariate Equation (Equation 3.1), being σ_x and σ_y the standard deviation found for the case when only t_{ox} or ρ_{ox} fluctuations were taken into

account (that is, 5 and 30mV, respectively), μ_x and μ_y the average V_{TH} (0.680 and 0.654V, respectively) and ρ the correlation coefficient. Leaving ρ as free parameter, we have obtained an R-parameter of 0.85, demonstrating that our data can be really fitted to a bivariate Equation. As for ρ, it was fitted to 0.79, which suggest the existence of a correlation between both sources of variability.

$$f(x,y) = \frac{1}{2\pi\sigma_x\sigma_y\sqrt{1-\rho^2}} exp\left(-\frac{1}{2(1-\rho^{2)}}\left[\frac{(x-\mu_x)^2}{\rho_x^2} + \frac{(y-\mu_y)^2}{\rho_y^2} - \frac{2\rho(x-\mu_x)(y-\mu_y)}{\rho_x\rho_y}\right]\right) \tag{3.1}$$

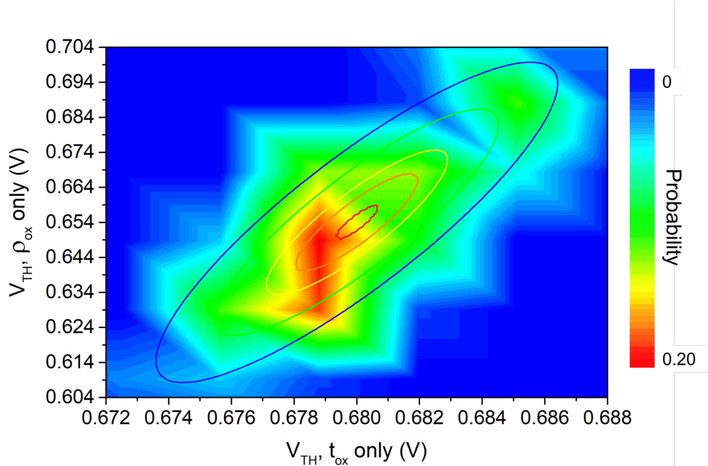


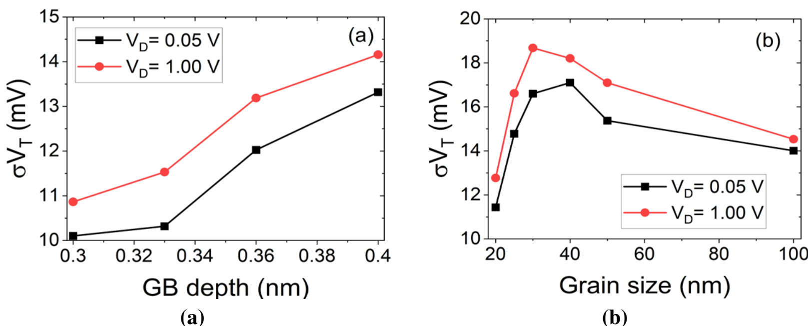
Figure 3.17: Probability (color scale) of finding devices as a function of the V_{TH} linked to t_{ox} fluctuations only (X-axis) and V_{TH} linked to ρ_{ox} variations only (Y-axis).

The analysis shown above clearly demonstrate that, at least in the HfO_2 layer studied in this thesis, the correlation between the polycrystalline morphology and the charge density (higher at GBs, already observed in [78]) implies that when considered together as variability sources, the V_{TH} variability does not correspond to the addition of the associated variabilities but, in our case, is smaller than the one observed when only ρ_{ox} is considered. Consequently, although other variabil-

ity sources might be studied independently as extensively discused in Refs. [200] and [212], the variability sources affecting the polycrystalline gate oxides cannot be studied independently as an specific analysis of the correlation is required for each specific case.

B. Impact of grain size and GB depth on the V_{TH} variability

With the development of TACMAG, one of the main characteristics of our simulation metodology is that, we can generate (ρ_{ox}, t_{ox}) maps without the need of fabricating new samples. Therefore, such variability sources and, in particular, the different parameters on which they depend (as, for example, Grain size, GB depth or width and/or charge density distribution), can be changed and analyzed independently at low cost. In this section, as a further example of the proposed methodology capabilities, we have evaluated the impact of some morphological parameters associated to the high-k polycrystallization on the MOSFET V_{TH} variability.



(a) (b)

Figure 3.18: Two cases of how morphological parameters involved in polycrystalline high-k dielectrics affect the V_{TH} variability of MOSFETs at 0.05 and 1.0 V drain biases. (a) and (b) show, respectively, the V_{TH} deviation for different values of the GB depth (a) and grain size (b).

Specifically, we have analyzed the impact of the GB depth and G size. Figure 3.18 shows the σV_{TH} obtained for a set of one hundred 50x50nm^2 MOSFET devices for different GB depths 3.18(a) and grain sizes 3.18(b) at both low (0.05V) and high (1.0V) drain biases. From Fig. 3.18(a) that σV_{TH} increases as the GB depth rises; something expected as an increase of the GB depth leads to a higher inhomogeneity in t_{ox} and ρ_{ox}, which clearly affects the V_{TH} variability. However, when the Grain size (Gsize) is considered as parameter, the V_{TH} trend changes. Note in Fig. 3.18(b)

that σV_{TH} reaches the largest value when Gsize is smaller than the channel length of the MOSFET and depends on V_D. Indeed, from that maximum value, when Gsize is reduced/increased, σV_{TH} decreases. This can be further understood as effect of averaging (low GS) and homogeneity (large GS). In the former, the large amount of grains and grain boundaries causes an avaraged impact over the V_{TH}, and thus lower variability, in other words the larger population the lower variability. For the latter, i.e when Gsize is larger than the MOSFETs dimensions, many MOSFETs could contain only one single crystal, increasing the homogeneity of the gate oxide characteristics and, therefore, reducing the V_{TH} variability. For grain sizes comparable to the channel length, the variability could be related to the inhomogeneity of the grain properties, since the thickness and charge in the grain are not homogeneous. Moreover, the V_{TH} may be affected by the particular position of the grain in the channel. A combination of all these factors will determine the particular position of the variability maximum for a give device polarization.

From a nanoscale point of view, the dependence of the MOSFET V_{TH} variability on the GB depth and Gsize could be explained by taking into account the nanoscale properties of the gate oxide (t_{ox} and ρ_{ox}) and how they affect the electrostatic potential in the channel. For instance, Fig. 3.19 shows different t_{ox} configurations and the corresponding t_{ox} and electrostatic potential profile measured along the highlighted lines.

Since the average value of the electrostatic potential depends on the position along the channel and, in our case, only relative variations with respect to the maximum are meaningful; for all the cases depicted here, the maximum value has been associated to 1000mV and just relative variations with respect to this maximum have been considered. In the first case, Fig. 3.19(a) a very deep GB (~0.5nm deep, dark area in the image) is analyzed. The other case, Fig. 3.19(b) corresponds to a big homogeneous grain (t_{ox} variations are in the range of < 0.1nm). If we compare the t_{ox} variations in the two images with the electrostatic potential fluctuations along the profile, values of ~15 and 6mV are measured in Fig. 3.19(a) and (b) respectively. Moreover, in Fig. 3.19(a), where a deep GB is detected, a clear correlation between the electrostatic potential and t_{ox} is registered. Therefore, these results indicate that the morphological parameters associated to the high-k polycrystallization

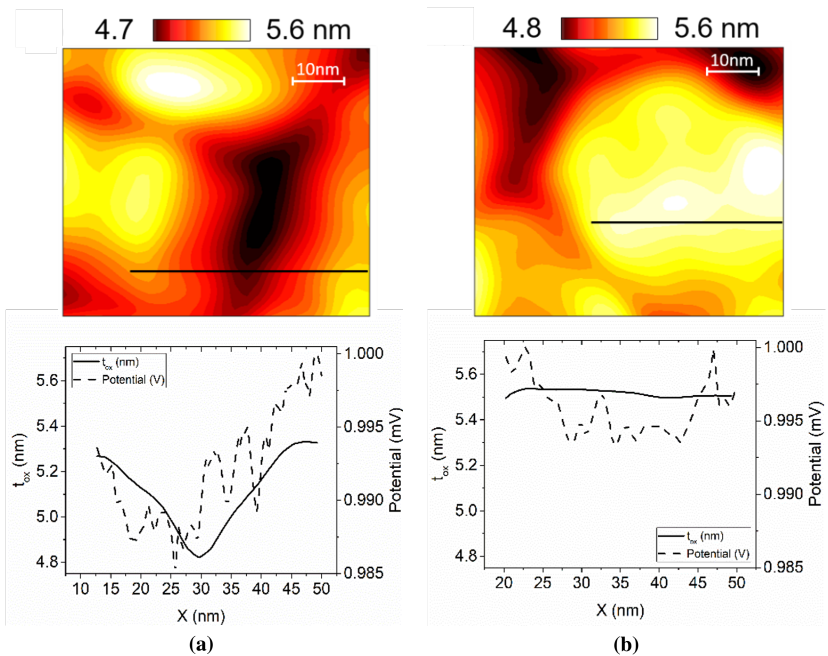


Figure 3.19: t_{ox} maps of different gate oxide configuration including (a) a deep GB and (b) a big grain. In both cases, the electrostatic potential (dashed line) and t_{ox} profile (continuous line) along the black lines indicated in the maps are shown below.

(as the GB depth and Gsize) affect the electrostatic potential in the channel, so that the higher the t_{ox} fluctuations, the higher the potential variations. Moreover, since the electrostatic potential along the channel determines the global electrical properties of the MOSFET, these results would explain why, the higher the fluctuation in t_{ox} and ρ_{ox}, the higher the V_{TH} variability.

So, to conclude this section, a simulation metodology was proposed to analyze the impact of nanoscale variability sources associated to polycrystalline high-k dielectrics (t_{ox} and ρ_{ox}) on MOSFETs V_{TH} variability. We have developed the TAC-MAG tool which, from topographical and current maps obtained with CAFM allows to generate t_{ox} and ρ_{ox} maps with identical statistical characteristic to the analyzed sample. These maps are then introduced in a device simulator to investigate the V_{TH} variability due to the t_{ox} and ρ_{ox} fluctuations. In particular, we have seen that t_{ox} and ρ_{ox} are not independent variability sources. They are correlated and, when combined, somehow compensated.

A smart measurement system for the combined nanoscale and device level characterization of Graphene FETs

ALTHOUGH silicon has been the unquestionable material of semiconductor industry for most applications, for some of them where higher flexibility [213, 214], transparency [215, 216] or mobility [217] are required, alternative emerging materials (e.g. 2D materials [133, 218], thin-films [219–221], inkjet-printed devices [222, 223] among others) are being deeply studied. However, these technologies are still in their infancy, and understanding issues such as their device-to-device (or time-zero) variability and reliability is essential to introduce suitable countermeasures into the fabrication processes, device architecture and/or circuit design.

Among all those alternatives to silicon, 2D materials are well positioned not only because they allow the survival of Moore's law down to the atomic level, i.e. to atomic thin layers, and are CMOS compatible, but for the wide range of physical properties available over the approximate 2000 known 2D materials [224]. The great range of properties make these materials quite interesting targets for the development of a variety of electron devices, like field-effect transistors [218], photodetectors [225], or resistive memories [226, 227] with properties that surpass the ones based on silicon [228–230].

However, their reduced thickness arises some particular issues in comparison to other materials; particularly, it makes them extremely sensitive to their surroundings, like the substrate, the environment (when they are exposed to air), and/or their own structure. For instance, in the case of graphene-based devices, nanoscale de-

fects, such as Grain Boundaries (GB), wrinkles, and corrugations, can appear in the graphene layer, which have been proved to hinder its electrical properties [43], negatively affecting the corresponding device performance.

This time-zero variability caused by the localized defects over the 2D structure can be studied with standard wafer level electrical tests, using, for example, a Semiconductor Parameter Analyzer (SPA) [49, 231]. However, in order to obtain a complete picture of the overall electrical characteristics of the 2D material/device it is essential to acquire also its nanoscale electrical and morphological characteristics. To do so, Atomic Force Microscopy (AFM) related techniques can be used [120, 192, 232] as described in section 1.5.

Finally, through reliability of emerging devices is crucial for their commercialization, its study is also limited. If we focus in the graphene-based field-effect transistors (GFET), although these devices have been studied [133–135, 233] at device level, the analysis of their reliability has not been fully addressed yet, specially at the nanoscale. However, due to the morphology of graphene, without any characterization at the nanoscale, the reasons behind the observed changes cannot be determined: one only can analyze the consequences of the electrical stress on the device performance, but they cannot be related to the actual changes (morphological and/or electrical) that happen in the material.

From the above, it can be concluded that understanding the sources of time-zero variability (related to the fabrication process) and of the time-dependent variability (associated to the effects of the aging mechanisms during the device operation) and their impact on the device behavior is essential for technology development. Since these variability sources are mostly related to nanoscale properties of the materials (grain boundaries, defects generation...), a combination of nanoscale and device level measurements is required to get complementary information and build a complete picture of the overall phenomena [234, 235]. An example of such kind of characterization was presented in [234], where different regions along the channel of a MOSFET were analyzed using CAFM and SPA measurements after an electrical stress. However, in that case, the tests were destructive (because the gate had to be removed), so that only one stress-measurement cycle could be carried out. More-

over, the sample preparation was time-consuming and annoying (the sample had to be physically moved from the wafer-probe station to the CAFM holder, the stressed transistor localized on the piece of wafer and the tip located on the area of interest). Finally, only currents through the gate oxide (i.e. gate-substrate currents) could be measured.

In this chapter we present a smart flexible experimental set-up which combines nanoscale AFM-related tests with standard electrical measurements at device level on fully-processed devices with an exposed active layer, so that no destructive sample preparation is required. Consequently, by integrating all the needed equipment into a unified measurement system, the proposed system simplifies the testing procedure, allows multiple stress-measurement stress cycles and also enlarges the capabilities of the system. With this smart system, we have preliminary evaluated the aging in back gated GFETs and correlated shifts in device parameters with the nanoscale changes of the material.

4.1 Architecture of the measurement system

In this section, we discuss our set-up, and how a typical aging cycle of measurement-stress-measurement (MSM) is conducted. Our set-up is composed of a CAFM and a SPA, which are used for the nanoscale and device level tests, respectively. The CAFM and the SPA are integrated into the same measurement system, in which the sample is located on the CAFM holder. This latter also has the additional advantage that a wafer probe station is not required, so the cost of the system is reduced. Figure 4.1 presents the equipment diagram of the complete developed set-up; where a PC is in charge of the configuration of the hardware, the execution of the user-defined test sequence, and the data acquisition. The use of the SPA or the CAFM (or both simultaneously) for biasing/measuring can be selected, depending on the configuration of the switch unit (Fig. 4.1, green box). A key point in the system is the connection of the instrumentation to the device terminals. For this purpose, a custom-made inkjet-printed circuit board (I-PCB) has been designed to be attached to the microscope holder, whose layout defines the device-instrumentation connectivity. All the needed connections are routed through an RJ45 connector (green line in Fig. 4.1), to ease the operability of the proposed system.

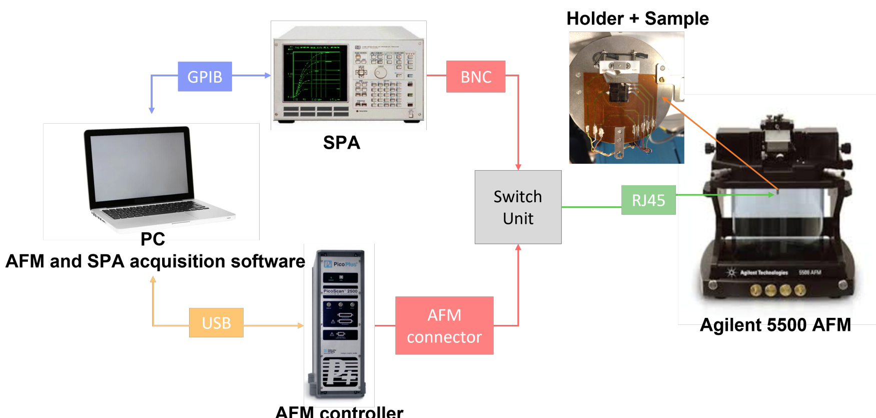


Figure 4.1: General equipment diagram of the developed set-up.

Then, to conduct a MSM reliability test combined with nanoscale measurements, with this set-up, one need to perform the following steps:

- First, the switch is configured to use the SPA, so the CAFM tip is not in contact with the layer of the device. SPA can be used to obtain I-V curves, in order to get the device conductivity before any stress. Then, the CAFM is connected (by correctly configuring the switch unit) and the channel is contacted by the CAFM tip, to obtain topographical and (lateral) current maps on different regions of the channel and to measure the nanoscale characteristics of the fresh device.

- To stress and measure again at device level, the CAFM tip is lifted and the switch unit configured to connect the SPA to the sample holder. The device was stressed and measured again with the SPA in order to evaluate the stress effect on the device. Finally, CAFM is connected again to measure the post aging characteristics at the nanoscale.

Note that the last step can be repeated as many times as defined by the user, in order to study the evolution of the degradation of the device as a function of time.

From all the aforementioned, it can be concluded that the keystone in the system is the way to rapidly and efficiently change the connection of the device terminal from the CAFM electronics to the SPA and vice versa. This means first, that the CAFM must be prepared for such a change, and second, that the device needs to be connected to the holder. Regarding the former point, the typical holders provided by equipment manufacturers only permit the most common connections, and moreover, the required connections are fully dependent on the specific contact pads of the device under test (DUT). Consequently, the most usual CAFM holders are impractical for such a purpose. Although one can manufacture ad-hoc holders for each specific measurement, the cost of that would be prohibitive, provide little flexibility, and consume too much time; hence discarding this alternative. To overcome those limitations, a low-cost extremely-flexible solution, consisting of the fabrication of a device-instruments connection interface, taking advantage of the versatility of ink-jet printing techniques [236, 237] is proposed here. To detail, we propose the fabrication of a custom-made inkjet-printed circuit board (I-PCB), with a suitable layout that, when stuck on the CAFM holder, defines the connectivity of the holder to the CAFM and the SPA. Here, it is worth noticing that once the I-PCB is printed, DUTs with the same contact pad distribution can be analyzed with the same system. Moreover, because of the ease with which the connection layout can be modified, the solution provides large flexibility.

The latter refers to the connection between the device and the I-PCB paths. Here, a critical point is a way the paths of the I-PCB are connected to the electrodes of the DUTs. Here is important to stress the impracticability of the traditional approach, which is wire-bonding; the reason behind this is the CAFM measurements, which have to be performed so that the wires would obstruct the tip movement while scanning the surface. To overcome this problem, again, ink-jet printing offers the best solution, since its resolution is enough to print paths inside the test chip to make the DUT connections, but without compromising the other devices (see in next section) when a particular case is studied. Additionally, this technique provides a further advantage, as the connections between the DUT and the I-PCB are printed, they are planar (i.e. just several nm high) which allows the free movement of the AFM tip over the whole surface of the sample.

4.2 Design of the I-PCB

In the previous section, the general concept behind the system has been introduced, where the I-PCB design is a key element. Depending on the architecture of the devices under test, their location in the chip, and measurements of interest, a specific I-PCB layout need to printed. In this section, as a particular example, an I-PCB to measure back-gated graphene-based transistors (GFET, with its channel exposed to air) combining a CAFM and a SPA is presented. The back-gated GFETs were fabricated on a SiO_2/Si substrate with an oxide thickness of 80 nm [238]. Note that the oxide thickness of the device is very large and no tunneling current through the oxide could be measured by CAFM. Therefore, the I-PCB has been designed in order to measure lateral currents only at the nanoscale. The designed I-PCB allows the connections of the GFETs to either a CAFM (in order to measure topography and current through the channel) or the SPA, in order to stress or measure the electrical characteristics of the GFET.

In our case, the I-PCB has been designed to characterize three of the GFETs in the chip. The I-PCB will connect the GFETs with the SPA and CAFM. The interconnection lines have been printed on an auto adhesive polyimide strip (Kapton, 50 μm thick, orange color material in Fig. 4.2(a) using the conductive ink Silverjet DGP HR [ANP, South Korea, grey material in Fig. 4.2(a) and grated grey boxes in Fig. 4.2(b)]. Then, the I-PCB is adhered on the existing AFM holder (Fig. 4.2). The printing process was done using a Dimatix printer with a 10 pl cartridge. In the I-PCB presented in this work [Fig. 4.2(a)], there is a total of 7 connection paths. Three of them (on the right side of Fig. 4.2(a) correspond to the source electrodes of three different GFETs. The following path to the left is the one that contacts the bottom part of the chip and will act as the gate electrode, which is common to the 3 GFETs. On the left side of Fig. 4.2(a) (black square), there are three more paths. The central one corresponds to the drain electrode of the three GFETs, which is common to the three selected devices. This path can be connected via an external switch (in the switch unit, Fig. 4.2(b) with one of the two adjacent paths. The one on the left corresponds to the electrical connection with the CAFM electronics (at the upper side of Fig. 4.2(a) and the one on the right to the connection to the SPA.

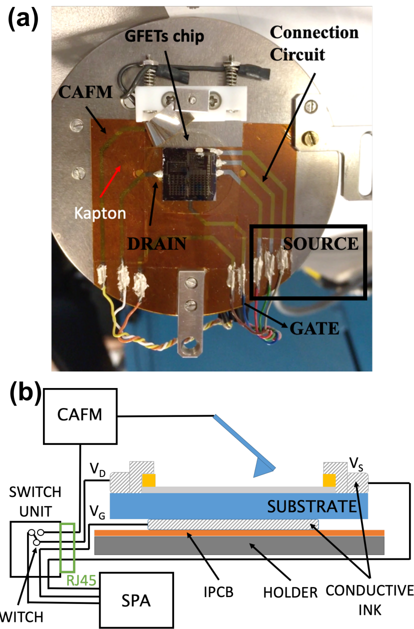


Figure 4.2: (a) Photography of the ink-jet printed connection circuit mounted over the AFM holder. It can be seen the auto adhesive I-PCB (orange-colored tape), the graphene transistor chip at the center and the connections corresponding to the source electrodes (black box) and to the measurement systems. (b) Cross-section of the I-PCB developed in this work for the analysis with a SPA and a CAFM of back-gate GFETs. The interface circuit allows to perform in-situ electrical measurements at device (with the SPA) and at the nanoscale (with CAFM). The switch unit allows the change of measurement modes changing the connections at the source electrode.

In this particular case, with the switch unit [Fig. 4.2(b)] it is possible not only to connect the drain electrode of the GFETs to the CAFM or to the SPA, but also to select which one of the three contacted GFETs is measured. All the printed paths terminations are welded to electrical wires using an isotopically conductive adhesive (ICA) silver epoxy (CircuitWorks Conductive Epoxy CW2400, Chemtronix) and these wires were connected to a RJ45 connector that is previously glued to the back of the AFM holder (not shown). In this way, all the signals can be routed outside the AFM by means of a standard ethernet cable to the switch unit.

Once the I-PCB has been designed and printed and the chip glued over the gate path, contacts between the printed lines therein and the GFETs electrodes in the chip must be done. As previously introduced, ink-jet printing techniques were also used with this purpose, instead of wire bonding due to the advantages explained before.

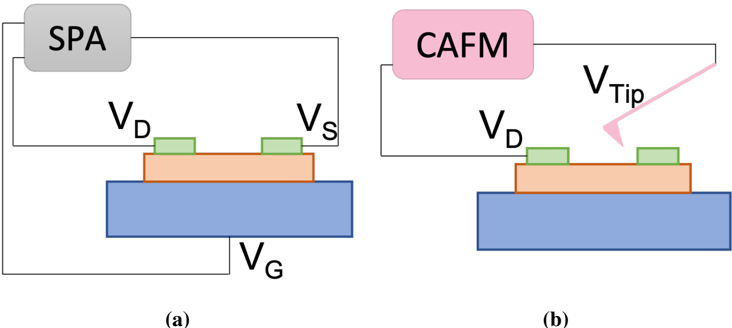
4.3 Electrical stress and measurement procedure

With the measurement system described in the previous section, we have followed the next procedure for the aging characterization of the GFETs, when subjected to different MSM cycles:

- **Step 1- Characterization of the fresh device (i.e. without previous stress).**

  First, the switch is configured to use the SPA. In this case the experimental configuration corresponds to Fig. 4.3(a). The inset in Fig. 4.5 presents the I_D-V_G curve obtained by applying V_D=-0.5V, V_S=0V and a V_G sweep between 20V and 50V. As one can see, the Dirac point is located around 37V. This indicates that the graphene layer is heavily p-doped due to its interaction with the atmosphere [239] and the conduction through the graphene channel will be associated to hole carriers. I_D-V_D curves at V_G=V_S=0V, when V_D is swept between V_D=-0.5 V and V_D=0.5 V have been also measured with the SPA, to get the device conductivity (i.e. the conductivity of the complete gate area, as a function of V_D) before any stress. Afterwards, the graphene channel is contacted by the CAFM to evaluate the electrical properties of the graphene layer between the GFET drain electrode and the tip [240]. The experimental configuration corresponds to Fig. 4.3(b). The current will be injected from the drain electrode with a V_D=+0.05V in order not to damage the graphene layer and will be collected by the AFM tip, meanwhile the source and gate terminals are disconnected. We have measured topographical and (lateral) current maps on different regions of the channel. In particular, lateral conductivity maps of regions close to the drain and source electrodes of the GFET have been obtained, to get nanoscale information of the graphene channel next to both

electrodes. For the CAFM experiments, in addition to the topography image, the friction image was also registered, as the contrast in the former is very low due to the low thickness of the graphene layer.



(a) (b)

Figure 4.3: Sketch of the connections for the measurements at (a) the device and (b) the nanoscale levels.

- **Step 2 – Electrical stress:**

  The device was stressed with the SPA. A constant voltage of 5V was applied at the source (V_S) and gate (V_G) terminals and 0V to the drain (V_D) terminal, a biasing configuration that corresponds to a Channel Hot Carrier (CHC) stress [46, 234].

- **Step 3 – Characterization after the electrical stress:**

  After the electrical stress (Step 2), we have followed the same procedure used in Step 1 to obtain the I_D-V_D characteristics at V_G=0V of the GFET and the graphene nanoscale features with CAFM of the same area characterized in the Step 1.

Steps 2 and 3 can be repeated as many times as defined by the user. In our case, the CHC stress was applied in 3 successive stress cycles of 2h, 4h and 8h (i.e. 14h of accumulated stress time).

4.4 Results and discussion

This section collects all the results obtained from performing all the previously mentioned steps.

A. Graphene properties before the CHC stress

To begin with, the I_D-V_D curves of the device and the conductivity of the graphene layer have been measured, with the SPA and the CAFM, respectively, before applying any electrical stress.

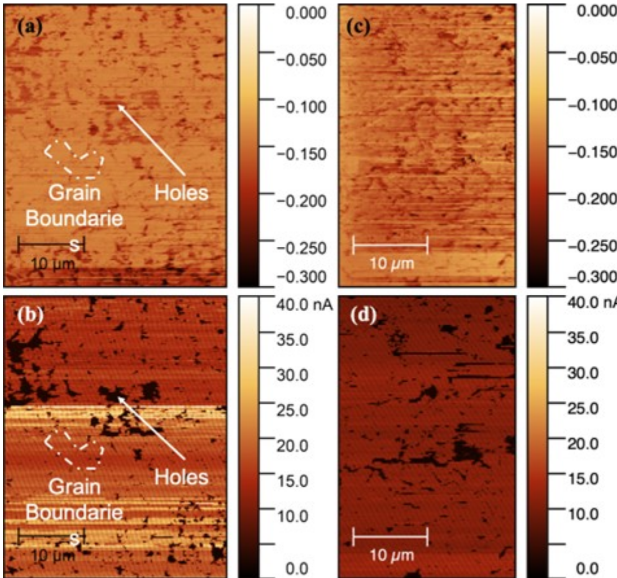


Figure 4.4: Friction (a, c) and the corresponding current images (b, d) of a region of the channel of a fresh GFET. The left images correspond to an area near the source electrode (size of the image 33.8 μm x 40 μm) meanwhile the right ones correspond to regions close to the drain electrode (size of the image 23.7 μm x 38 μm).

Regarding the CAFM measurements, the friction and current images measured before the stress are shown in Fig. 4.4. Figure 4.4(a/b) and (c/d) show the friction/current maps in a region close to the source (a/b) and close to the drain (c/d) of the GFET, respectively. In the friction map, Grain Boundaries and holes are measured, which could have been created during the CVD growth [241] and/or graphene transfer [242]. The same kind of features are registered in the current maps [Fig.

4.4(b) and (d)]. We consider holes as the areas of darker color in the friction maps, which can be also identified in the current image with current levels corresponding to the noise level of the AFM. These areas could be related to regions without graphene, so that the CAFM tip is directly contacting the SiO_2 substrate. Grain boundaries have also been measured, mainly in the friction image, as lines that lead to closed regions (the graphene single crystals [230]). These regions have lower currents than the grains themselves (although above the noise level), suggesting a different arrangement of atoms.

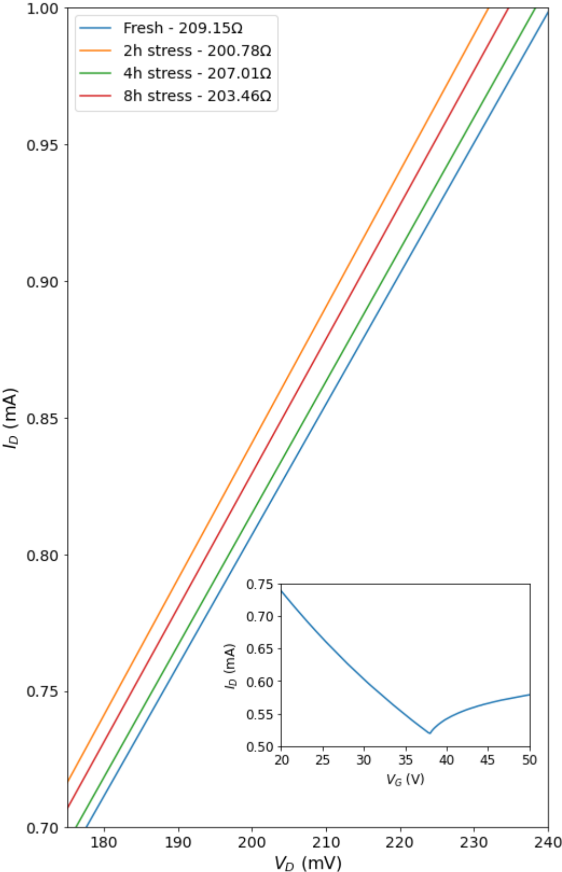


Figure 4.5: IV curves obtained from the GFET before and after different cycles of CHC stress.

The average current flowing through the tip in the regions close to the drain and source has also been estimated. It is around 17.26 nA in Fig. 4.4(b) (close to the drain) and 10.75 nA in Fig. 4.4(d) (close to the source). It is important to emphasize that the current registered close to the source is lower than that registered close to the drain. This is already expected due to the different resistance between the drain electrode and the position of the CAFM tip. When the tip is close to the source, the carriers have to travel along the whole graphene channel, so they will 'find' a higher resistance. Therefore, a smaller current will flow compared to the case when the tip is close to the drain electrode.

The electrical properties at device level were also measured with the SPA. Figure 4.5 (blue) shows an I_D-V_D curve when at V_G=0V. The resistance has been estimated to be $\sim$209Ω. This curve will be used as a reference, to which those obtained after the stress cycles will be compared in next sections.

B. Graphene properties after the CHC stress

After each of the 3 consecutive stress cycles have been applied, CAFM maps and device level I_D-V_D curves were also registered. Figure 4.5 shows the different I_D-V_D curves obtained on the GFET after each stress cycle and the corresponding estimated resistance. Note that, the resistance is quite stable after each CHC stress cycle and the changes between stresses are quite small. Note also that, the highest resistance is reached before any CHC stress (fresh state). This phenomenon could be related to the sintering of the Ag ink during the electrical stress and will be discussed in more detail when the nanoscale electrical measurements are analyzed.

A nanoscale analysis was also performed after the stress, Fig. 4.6 shows the effects of the stress sequence measured with CAFM (friction and current images). Figure 4.6a/b correspond to the images before the stress; Fig. 4.6c/d after the first stress cycle (2h of stress time), Fig. 4.6e/f after the second stress cycle (4h of stress time or 6h of accumulated stress time,) and Fig. 4.6g/h after the third stress cycle (8h of stress time or 14h of accumulated stress time) on the same region next to the drain (the x-y position of the Pt tip has not been changed during the electrical stress, so it is easy to return to the same region).

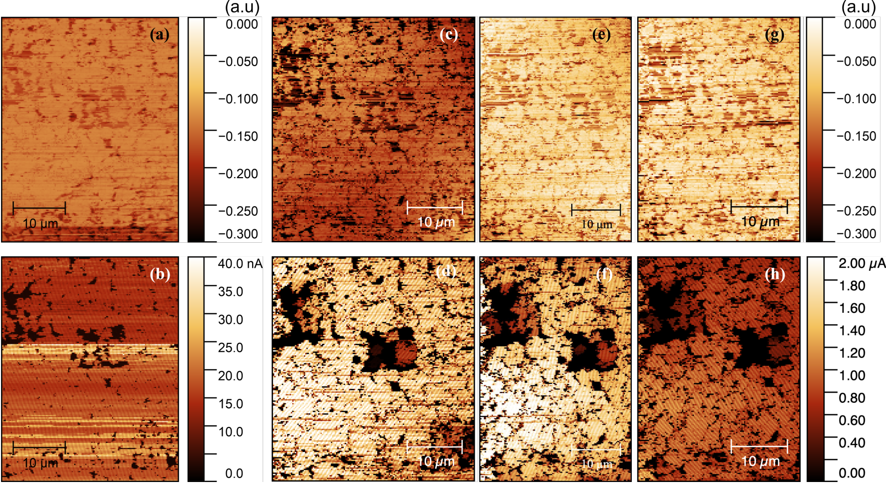


Figure 4.6: Friction (a, c, e and g) and their corresponding current images (b, d, f and h) of a zone near the drain of a GFET after different stress times. (a) and (b) corresponds to the fresh GFET, while (c), (d) is the same zone after a 2h electrical stress, (e) and (f) after 6h of electrical stress and (g) and (h) after 16h of electrical stress.

In the friction images [Fig. 4.6(c), (e) and (g)] we can see that the surface inhomogeneities have increased after the electrical stress compared to the fresh case [Fig. 4.6(a)], which have been related to defects created on the graphene layer during the stress. The current image [Fig. 4.6(e), (f) and (h)] further supports this idea. Note, first of all, that the average current before the stress is much lower than after any stress cycle. This is an effect of the sintering of the conductive epoxy used for the fabrication of the I-PCB through joule heating, that decreases its resistance during the electrical stress [243]. This phenomenon was also observed at device level (Fig. 4.5). This effect would explain the low initial current in the fresh device and would hidden the real impact of the first stress phase on the absolute values of the measured current. Therefore, a comparison of the current absolute values before and after the first stress is not meaningful at this moment. A next step to improve the proposed methodology would include how to sinter the conductive epoxy even before the first measurements. That would also allow to compare the fresh state with those after any stress cycle. However, relative variations within the same im-

age are fully relevant and indicative of what is actually happening in the graphene layer. In the current images recorded after the stress [Fig. 4.6(d), (f) and (h)], those regions with lower conduction (basically grain boundaries) and those without current (holes) have increased in size, suggesting that the electrical stress might have resulted in a burning of the sp2 hybridized carbon through the sp3 hybridized defects (grain boundaries and holes perimeters) due to the joule heating effect and its interaction with the oxygen present in the environment [244].

The results show until now, demonstrate that there is a clear damage of the graphene layer due to the electrical stress. Although at device level, the stress does not seem to affect too much the measured average current (see Fig. 4.6), at the nanoscale the results clearly show that the CHC stress has damaged the graphene layer. The reason why such nanoscale damage (measured with CAFM) is not clearly seen at device level can be related to the dimensions of the analyzed devices. Since the width of the GFETs is quite large, although the graphene channel might have been locally damaged at different regions, current can easily flow through other paths between drain and source, having little impact at device level. Therefore, it would be expected that in GFETs with a smaller area, a larger correlation between the observed nanoscale and device level properties would be obtained. In any case, the preliminary results presented here show a particular case where the CAFM reveals information that will remain hidden at device level. This result highlights the importance of the methodology presented in this thesis and the necessity to combine both techniques to have a global view of what is happening in the device. Otherwise, the use of only one technique can lead to misleading conclusions.

The nanocale resolution of the AFM also allows to investigate the uniformity along the channel of the damage induced during the stress. As in Ref. [234] where the impact of a NBTI and CHC stress on the gate oxide of a pMOSFET at different positions along the channel was investigated with a CAFM, here, we will preliminary analyze the impact of the CHC stress on the graphene layer of the GFET in regions close to the source and to the drain electrodes. Note that, since the comparison of the images before and after the first stress cycle is not meaningful (because of the sintering of the ink in the device contacts), we have only compared the evolution of the images with the stress time, from the images in Fig. 4.6(d), (f), (h) and the

analogous images taken in a region close to the source (not shown). In particular, from those current images, the average current and the percentage of area covered by graphene has been estimated. The average current was calculated ruling out the zero-current regions. The percentage of graphene coverage has been calculated also excluding also regions without current.

Figure 4.7 shows the average current (a), and graphene coverage (in %) (b), measured close to the drain (black) and to the source (red) after each stress cycle. Regarding the average current [Fig. 4.7(b)], note that the current measured next to the source is lower than that registered next to the drain. This phenomenon is due to, as expected, the different resistance value between the drain electrode and the CAFM tip position, as already discussed in Fig. 4.4.

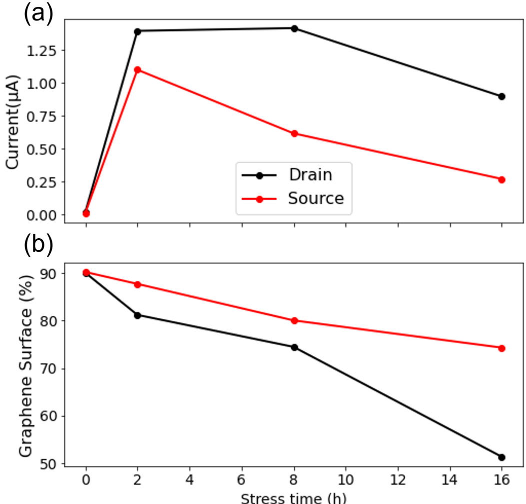


Figure 4.7: (a) Evolution of the average current (without taking into account the holes) after each CVS. (b) Evolution of the % of graphene surface after each stress cycle. The two graphs have the same x-axis.

Note also that after the initial increase in current due to the first stress cycle (due to the sintering of the conductive epoxy), a progressive reduction of the average current is measured as the stress proceeds, at both sides of the device. This reduction is a consequence of the stress and can be related to the progressive degradation of

the graphene channel after each stress cycle, as observed in Fig. 4.6. Actually, the percentage of graphene coverage continuously decreases with the stress time [Fig. 4.7(b)]. Note also that the drop is faster next to the drain terminal, reaching a 50% coverage after 14h of stress, whereas next to the source terminal it only decreases until 75%.

The origin of this discrepancy can be further understood by the CHC characteristics. Here is worth recalling that during the application of the CHC stress, 5V was applied at the gate and source terminals, whilst the drain terminal was forced to ground (i.e. 0V). This configuration leads not only to the presence of a lateral electric field, which can be assumed to be constant along the channel, and hence causes homogeneous damage to the graphene layer, but to the existence of a vertical field between the drain and the gate, which can affect the gate oxide at the drain electrode, as NBTI. Furthermore, the next-to-drain section of the SiO_2 layer can be further affected by the injection of hot carriers, as long as we are treating with positive carriers. Owing to the fact that such phenomena, in our specific case, only occur at the drain terminal, it also explains the difference observed in Fig. 4.7(b). Therefore, BTI and Hot Carrier injection are, at least partially, responsible for the higher graphene damage induced close to the drain. On the contrary, the damage induced next to the source is found to be principally caused by the lateral current flowing through the graphene channel. On top of all these, we found that the stress induced in the oxide due to the vertical field seems to somehow affect the whole graphene layer. Nonetheless, further analysis should be performed to verify these assumptions, these preliminary results demonstrate the potential of the methodology developed in this work.

5 Impact of electrical stresses on OTFTs properties: An analysis at the nanoscale with KPFM

Most of the results of this chapter are reproduced and/or adapted from:

⋆ *A. Ruiz, S. Claramunt, A. Crespo-Yepes, M. Porti, M. Nafria, H. Xu, C. Liu, Q. Wu, "Exploiting the KPFM capabilities to analyze at the nanoscale the impact of electrical stresses on OTFTs properties", Solid-State Electronics, Volume 186, 2021, 108061.*

NUMEROUS studies in the literature have focused on the analysis of devices based on organic materials (OTFTs) [60, 245–247]. However, in terms of their reliability, few studies have been carried out, being one of the key points for this technology to make its way into the market. On the other hand, as already pointed in Chapter 1 and as it has been shown in Chapter 4, a correlation between nanoscale properties of the materials that form a device and their electrical properties is mandatory to have an overall view of the phenomenology under study. For this reason, in this chapter, the impact of an electrical stress on OTFTs electrical properties has been evaluated at device level and at the nanoscale with KPFM. In particular, we have extended the use of this technique to preliminary analyze the impact of a CHC stress on both the polymer layer and the gate stack of the OTFT at the nanoscale. To do this, two KPFM measurement configurations have been used, obtaining complementary information, and allowing to correlate device level and nanoscale features.

5.1 Experimental details

We have characterized OTFTs grown on a heavily doped silicon wafer with a 300 nm-thick thermally grown SiO_2 dielectric layer on top [Fig. 5.1(a)]. In this kind of

structure, the Si bottom electrode plays the role of the gate electrode of the OTFT. The substrate was cleaned sequentially with acetone, isopropyl alcohol, and deionized water in an ultrasonic bath, followed by blowing dry with nitrogen gas. On top of the gate dielectric, Au source and drain electrodes 30 nm thick, Fig. 5.1(a) and (b) were defined by photolithography to get a channel length (L) of 20 µm and channel width (W) of 15 mm. The organic channel was grown through a procedure based on solution-processed organic semiconductors. Specifically, a semiconductor solution of DPP-DTT in 1,2-dichlorobenzene (10 mg mL-1) was then spin-coated and annealed at 80ºC for 10 min within a nitrogen environment, leading ti in an 80 nm thick P-type organic semiconductor. For reference, we provide a cross-section of the resulting device in Fig. 5.1(a). It is worth mentioning that the surface of the device is completely covered by the DPP-DTT polymer, but the height profile mirrors the profile of the defined Au electrodes that are buried under the polymer layer. In Fig. 5.1(c), we provide a topographical image and profile along the line of an OTFT channel between two of these Au electrodes.

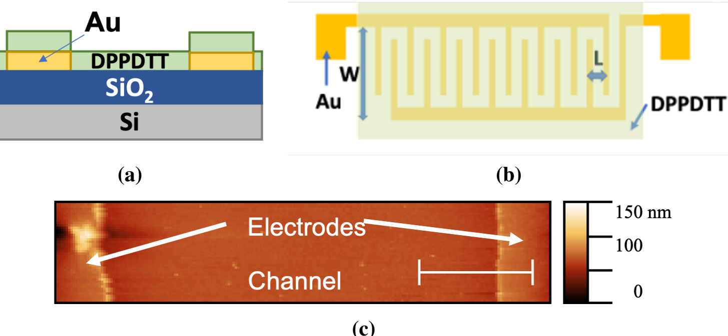


Figure 5.1: Cross-section (a), top view of the OTFT under study (b) and the topographical image of the resulting DDP-DTT layer on two Au electrodes (the scale bar is 5 µm) (c).

To evaluate the impact of an electrical stress, I-V characteristics at the device level (i.e. I_G-V_G and, I_D-V_G), and the nanoscale properties of the channel and gate stack were measured with a Semiconductor Parameter Analyzer (SPA) and with a KPFM, respectively, before and after the stress. The stress was applied using the Keithley 4200 SPA, which was also utilized to obtain the device level I-V characteristics. The stress was a -30V constant voltage applied at the gate and drain terminals

for 6000 s. As for the nanoscale properties of the OTFT, they were investigated with a Nano-Observer KPFM from Concept Scientific Instrumen, with this setup, one can measure at the same time both the topography and the Contact Potential Difference (CPD) between the tip and the sample.

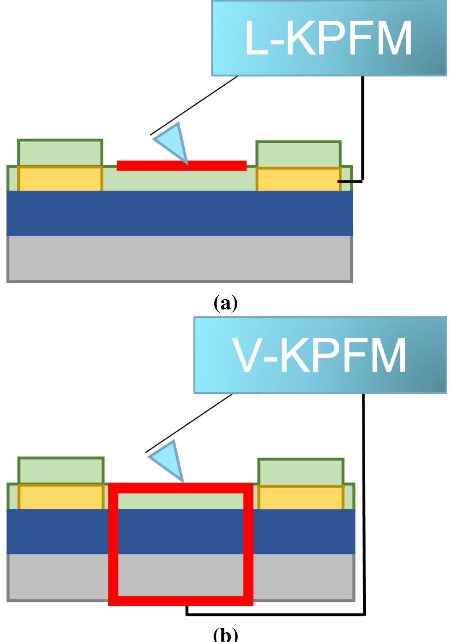


Figure 5.2: L-KPFM configuration (a) and V-KPFM configuration (b).

In our particular case, the KPFM images have been obtained in normal conditions, using Si tips from AppNano. Since the CPD data corresponds to the difference between the Work Functions (WF) of the tip and the sample, if one assumes a constant value of the tip WF during the whole experiment, the measured CPD variations can then be related to the WF fluctuations intrinsic to the sample. Consequently, the CPD maps provide information on the nanoscale value of the WF of the analyzed sample. Nonetheless, since the tip WF is unknown, and the absolute values of WF are also extremely sensitive to environmental conditions; it is not rare for it to change between different consecutive measurements so that only WF relative variations in a given image shall be considered. Our KPFM allows bimodal

single pass Amplitude Modulation KPFM (AM-KPFM) measurements [192]. Figure 5.2(a) and (b) show the two KPFM measurement configurations used in this study. In the former [Fig. 5.2(a)], the KPFM measurements are performed between the Organic channel and the electrodes (called from now on Lateral KPFM configuration, L-KPFM), as the ground of the microscope is connected to one of the metal electrodes. In the latter [Fig. 5.2(a)], the ground is instead connected to the gate. Therefore, the measurements are performed between the organic channel and the substrate (called from now on Vertical KPFM, V-KPFM). Therefore, each configuration will provide details of the properties of different layers/stacks of the analyzed structure.

5.2 Results

5.2.1 Before the electrical stress

This section shows the results obtained for each of the configurations presented in the previous section. In order to have a reference, the electrical properties of a pristine OTFT are first investigated, both at the device level and at the nanoscale for the L-KPFM and V-KPFM configurations, as shown in Fig. 5.3.

Fig. 5.3 shows, for the L-KPFM configuration, the topography (a) and CPD (b) images of a region overlapping the channel and one of the electrodes. Figure 5.3(c) corresponds to the profiles along the lines drawn in the maps. Figure 5.3(d) and (e) shows to the topography and CPD images and the corresponding profiles [Fig. 5.3(f)], for the V-KPFM case. Note that, in both configurations, in the topography map, a step is measured between the electrode (highest region) and channel (lowest region), also detected in the profile. This step is measured in the V-KPFM image as an artifact due to the crosstalk effect, in which a sudden change in the topography may induce an instantaneous change in the CPD map [248]. This phenomenology can be observed at the center of the V-KPFM map [Fig. 5.3(f)]. However, leaving aside this artifact, the images and the profiles indicate no relevant differences between the CPDs of both regions (channel and electrode), as expected.

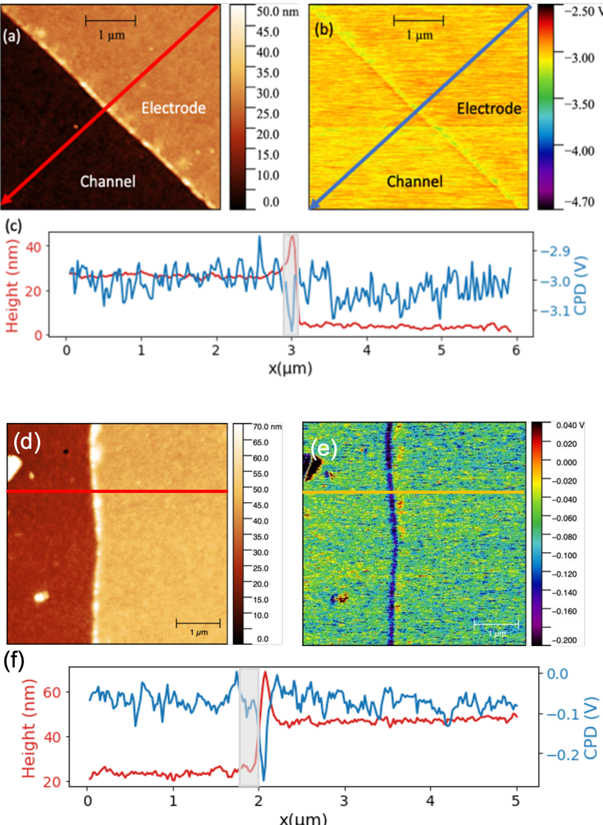
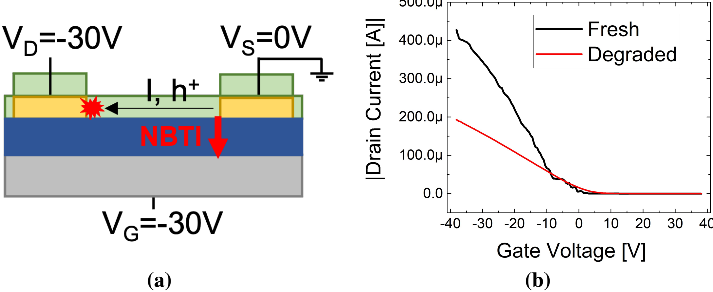


Figure 5.3: [(a) and (b)] Topographical and [(b) and (e)] corresponding KPFM images of a region that overlaps the channel and electrode areas, for the L-KPFM [(a) and (b)] and V-KPFM [(d) and (e)] configuration. A profile along the lines on the images in the topography/CPD maps is shown in ((c) and ((f). The CPD is approx. constant over the two regions except at the step between the channel and electrode (grey area in the profiles), related to measurement artifacts. The scale bar is 2 µm.

Remember that the tip is always contacting the as-deposited organic material and the devices have not been subjected to any kind of electrical stress. The device's electrical characteristics measured at devic level are shown in Fig. 5.4(b). The black I-V plot corresponds to the pre-stress I_D-V_G characteristic, and thus will be taken as a reference to compare the post-stress curves (red line).

5.2.2 After the electrical stress

After the analysis of the fresh device, a CHC stress has been applied to the OTFT with the SPA. Figure 5.4(a) shows a schematic of the device biasing. While the source was grounded, a voltage of -30 V was applied to the drain and back gate of the OTFT. It is worth noting that with this configuration, positive carriers flow from source to drain, getting the maximum energy near the drain, hence damaging that region. Additionally, since V_D=V_G at the drain area, vertical electric fields are negligible near the drain, so the NBTI damage (if any), should only appear near the source electrode.



(a) (b)

Figure 5.4: Cross-section (a) and top view of the OTFT under study (b).

After the CHC electrical stress, the I_D-V_G curves have been measured, i.e. the red curve in Fig. 5.4(b). We observe, a significant current reduction in the I_D-V_G curve after the stress. Such a reduction is due to a strong mobility reduction combined with negligible threshold voltage (V_{TH}) variation. Since BTI aging is mostly related to V_{TH} variations and CHC degradation to mobility reductions, the results shown in Fig. 5.4(b) suggest that CHC injection drives the device degradation, whilst the BTI seems to have a negligible role in the aging of the device [249].

To further study the effects of the stress on the properties of the different regions/materials of the device, L-KPFM, and V-KPFM measurements were performed along the channel, specifically close to source and drain electrodes. Figure 5.5 displays the L-KPFM (a-d) and V-KPFM (e-h) maps of the channel/drain (C/D) and channel/source (C/S) overlapping areas. The top/down maps show topography/CPD images. In the source/channel region [Fig. 5.5 (c/d/g/h)], very small

differences are measured in the CPD map between the electrode and the channel region, independently of the mode measurement, as was also observed in the fresh device [Fig. 5.3]. Only some observable differences in the CPD values are measured in Fig. 5.5(h); however those can be related to measurement artifacts associated to the topographical changes observed in Fig. 5.5.

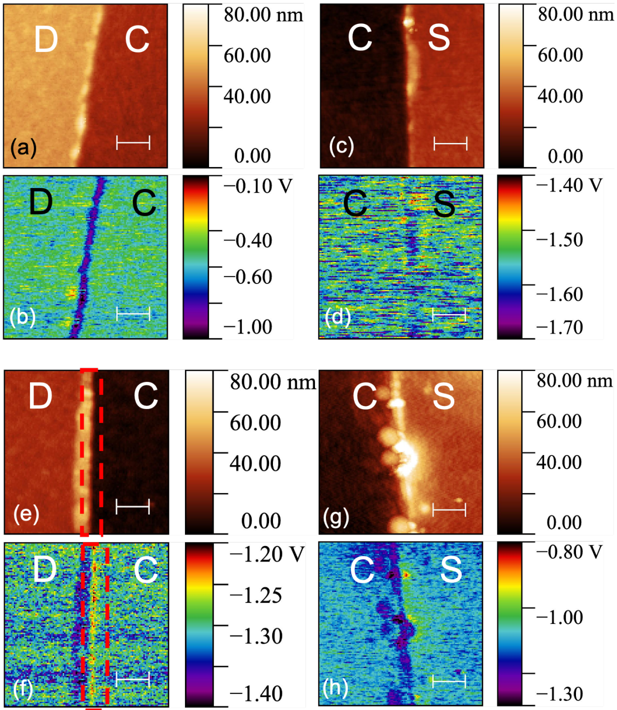


Figure 5.5: L-KPFM (a/b/c/d) and V-KPFM (e/f/g/h) images of the channel/drain (C/D) and channel/source (C/S) overlapping regions. The scale bar is 0.5 µm. In general, the changes in CPD values match the changes in topography, except in the drain region when measured using the V-KPFM configuration (e/f). In this case, an additional CPD signal appears along the drain electrode, that is enclosed by the red box.

Although these differences could be related to some kind of contamination of the organic layer, their origin is not clear and additional studies should be conducted . Nevertheless, our results suggest that the stress has not induced visible NBTI changes either in the channel or in the gate stack close to the source. Since

NBTI effects [see Fig. 5.4(a)] (if any) in this CHC stress are expected to be located in that region (further extending into the channel region), these results suggest that the NBTI has a negligible impact in this device, in line with what was observed in the device level analysis (Fig. 5.4). Indeed, the CPD L-KPFM, image in the drain/channel region [see Fig. 5.5(d)] did not show remarkable changes in the CPD between the drain electrode and channel regions, being those similar to that measured in pristine OTFTs [Fig. 5.3(b)]. This fact indicates that there is negligible damage on the surface of the OTFTs channel. However, the V-KPFM images (Fig. 5.5(e/f) suggest the presence of an additional difference in the KPFM signal, not previously measured, close to the step.

This difference, can be seen as a line that follows the drain/channel interface [in a red box in Fig. 5.5(f)], namely ∼90 nm wide into the channel region and with an increase of the CPD of ∼60 mV. This CPD signal variation cannot be related to any topographical feature near the step between the drain/channel interface. Nonetheless, L-KPFM results in the channel region show no damage at the surface, this could be indicative of local damage at the dielectric and/or at the gate oxide/channel interface. These results, athough preliminary, are compatible with the CHC degradation observed at the device level [Fig. 5.4(b)], whose damage is expected to be concentrated close to the drain electrode.

6 Summary and conclusions

Nowadays, within the 4th industrial revolution, the need of high performance computers, tablets, smartphones and flexible and low cost electronics for IoT, among other applications, has led the semiconductor industry to become a cornerstone of our society. Integrated circuits performance has improved thanks to the scaling of devices, the introduction of new materials in the MOSFET and/or the modification of its structure. On the other hand, flexible and low cost electronics is taking advantage of emerging devices as those based on graphene or organic materials (OTFTs). However, the variability found in such devices can cause significant fluctuations of their properties, whose origin can be found in the nanometer scale. Reliability issues are also become increasingly important with each technological node and, specially, with emerging devices. Therefore, the variability and reliability of electronic devices has risen in interest in the last decades. This thesis is focused on this topic. We have developed/improved different setups and/or methodologies to correlate nanoscale (observed with AFM related techniques) variability sources or aging mechanisms with their impact on device level characteristics of the corresponding devices. In particular, they have been applied to MOSFETs and emerging devices as graphene-FETs and Organic TFTs.

In Chapter 1, a brief introduction of the fundamental concepts necessary for the thesis are presented. Since most of the experimental data in this thesis has been obtained at the nanoscale with AFM related techniques, a detailed explanation of them (CAFM and KPFM) is presented in Chapter 2. The rest of the Chapters have been devoted to the results obtained in this thesis. In Chapter 3, we have evaluated

the impact of the polycrystallization of metal gates and high-k dielectrics on the variability of MOSFETs, by combining experimental data and a device simulator.

Regarding polycrystalline metal gates, the main results are:

⋆ The contact potential maps obtained with KPFM on pollycrystalline TiN layers show workfunction (WF) variations between the grains and grain boundaries of the metal gate. Regarding the grains, though two crystal orientations have been observed with KPFM, as expected, a continuous distribution of workfunctions has been also measured.

⋆ Areas of the WF maps measured with KPFM have been introduced into a device simulator as gate electrode to evaluate the impact of the WF fluctuations on the I_D-V_G curves of MOSFETs. The impact on the device parameters has been shown to be larger than when compared to approximated cases used in the literature.

⋆ Therefore, the results show that the presence of grain boundaries and a continuous work-function distribution of the grains need to be considered to obtain more accurate data: the procedure used in this thesis is a more realistic approach because the workfuncion fluctuations have been obtained from direct experimental data.

⋆ We have also shown that the device characteristics and variability of its parameters are affected by the spatial distribution of the workfunction fluctuations. Depending on the fluctuation location, the potential distribution in the channel is affected differently, leading to different values of the MOSFET V_{TH}.

Regarding polycrystalline gate dielectrics and their effect on MOSFETs variability:

⋆ We have proposed a new methodology of simulation to evaluate the impact of the nanoscale variability sources (obtained with CAFM) related to the high-k pollycrystalization on the MOSFETs variability.

- To do that, A Thickness And Charge Map Generator (TACMAG) was develop and used in combination with a device simulator. TACMAG uses experimental data as topography and current maps, obtained with CAFM, in polycrystalline gate dielectrics, as inputs. The outputs of TACMAG, that is, thickness and charge density maps, were used as inputs of a device simulator to evaluate their impact on the device parameters, as the V_{TH} variability.

- The TACMAG generator has been tested and used to evaluate the impact of thickness and charge density fluctuations of HfO_2 layers on the V_{TH} variability of MOSFETs. We have seen that the charge density fluctuations have a higher impact than the thickness fluctuations on V_{TH}. Moreover, the effect of both variability sources are correlated and can be modeled with a bivariate equation: when both variability source are combined, they are somehow compensated.

- Therefore, for an accurate study of the impact of polycrystalline dielectrics on the variability of V_{TH}, the gate oxide thickness and charge density fluctuations cannot be analyzed independently.

- The proposed methodology can be applied to any polycrystalline structure. Moreover, it allows to easily change morphological parameters of the dielectric and evaluate their impact on the device variability without the need of fabricating new samples.

In Chapter 4, we have presented a new smart and flexible experimental set-up that combines device level and nanoscale measurements on fully processed devices, by using a Semiconductor Parameter Analyzer (SPA) and CAFM, respectively.

- This equipment is integrated into a unique system through a custom-made inkjet-printed circuit board (I-PCB), that, when attached to the sample holder, allows the alternate or simultaneous connection of the device terminals to the required measurement instrumentation.

- This smart system has been used to evaluate at the nanoscale and at device level the impact of a CHC stress on graphene based devices. We have ob-

served that whereas the device level conductivity slightly decreases after the stress, an important change in graphene morphology and conductivity is measured. Moreover, the impact of the stress is more important close to the drain, where carrier injection happens during the stress.

- ⋆ The obtained results demonstrate the usefulness of our approach when compared to other alternatives, as not only provides a global view of what is happening on the device but also unmasks nanoscale effects inaccessible through the device level measurements.

Finally, in Chapter 5, we have evaluated the impact of a CHC electrical stress on the electric properties of OTFTs by combining two KPFM measurement configurations (L-KPFM and V-KPFM) and device level tests. The results show:

- ⋆ L-KPFM and V-KPFM configurations can provide complementary information to device level tests on the nanoscale damage of the different materials/regions of the device.
- ⋆ In the source/channel region, NBTI has not induced visible changes neither in the channel or in the gate stack close to the source.
- ⋆ In the drain/channel region, the L-KPFM image did not show remarkable changes in the CPD. However, the V-KPFM images suggest the presence of an additional difference in the KPFM signal which could be indicative of local damage at the dielectric and/or at the gate/channel interface
- ⋆ These results, though preliminary, are compatible with the CHC degradation observed at device level, whose damage is expected to be concentrated close to the drain.

To conclude, this thesis has shown that AFM related techniques, in combination with device level tests, are very useful to study and correlate the nanoscale phenomena responsible of the variability and reliability of the devices with their effect on the device electrical parameters.

Appendix I: Compendium of publications included in this Thesis

ARTICLE APL (MARCH-2019)

Workfunction fluctuations in polycrystalline TiN observed with KPFM and their impact on MOSFETs variability

Ana Ruiz, Natalia Seoane, Sergi Claramunt, Antonio García-Loureiro, Marc Porti, Carlos Couso, Javier Martin-Martinez, Montserrat Nafría

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Applied Physics Letters

Workfunction fluctuations in polycrystalline TiN observed with KPFM and their impact on MOSFETs variability

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Workfunction fluctuations in polycrystalline TiN observed with KPFM and their impact on MOSFETs variability

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ABSTRACT

A more realistic approach to evaluate the impact of polycrystalline metal gates on the MOSFET variability is presented. 2D experimental workfunction maps of a polycrystalline TiN layer were obtained by Kelvin Probe Force Microscopy with a nanometer resolution. These data were the input of a device simulator, which allowed us to evaluate the effect of the workfunction fluctuations on MOSFET performance variability. We have demonstrated that in the modelling of TiN workfunction variability not only the different workfunctions of the grains but also the grain boundaries should be included.

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The continuous scaling of MOSFET dimensions has led to the introduction of high-k/metal gate stacks in recent technological nodes. However, high-k dielectric polycrystallization has already been shown to be a variability source in ultrascaled MOSFETs affecting their electrical properties.[1–5] Metal gates were also introduced with high-k dielectrics because they have several advantages compared to polysilicon.[6,7] However, depending on the growth temperature, metals become polycrystalline, leading to grains with different sizes and orientations. Since the grain workfunction (WF) depends on their orientation,[8] the random distribution of grains (with their corresponding WF) also results in variations in the metal WF and the threshold voltage variability (TVV).[9–11] Therefore, it is critical to understand the origin of this variability in order to select the best fabrication process and materials that can reduce it.

Some works have already evaluated the impact of the grain orientation induced workfunction variation (WFV) on the variability of MOSFETs. In Ref. 11, for example, it was experimentally demonstrated that the TVV of a MOSFET is affected by the grain size. However, since this study was performed at the device level, the individual impact of the WFV on the device properties cannot be separated from other sources as random dopant fluctuation (RDF) or line edge roughness (LER). Other works have evaluated the TVV by means of simulation and statistical models that make assumptions that could be unrealistic.[9,10]

In this work, a more realistic approach which relies on 2D experimental WF maps obtained by Kelvin Probe Force Microscopy (KPFM) is proposed to study the impact of metal polycrystallization on the electrical parameters of MOSFETs. From KPFM measurements, the metal gate WF fluctuations are determined on the nanoscale. This information is then introduced into a device simulator to analyze the impact of metal granularity on the variability of the device electrical properties.

Experimental data were obtained from a sample containing a 100 nm thick TiN layer grown by continuous e-gun evaporation of metallic Ti over a HfO_2/Si substrate. The formation of TiN was ensured by passing the Ti atoms through a reactive nitrogen-enriched atmosphere, at a nitrogen partial pressure of 8×10^{-4} mbar. The structure of the TiN layer was determined by X-Ray Diffraction (XRD) using a PANalytical X'PERT PRO with the CuK_α line in Bragg-Brentano geometry. The morphological and electrical properties of the polycrystalline metal layer have been measured with a Nano-Observer AFM (from Concept Scientific Instruments), which allows bimodal single pass AM-KPFM measurements to simultaneously obtain topographical and sample-tip contact potential difference (CPD) 2D maps with a nanometer resolution.[12,13] Note that although FM-KPFM usually offers a better resolution than AM-KPFM,[14–16] bimodal single pass AM-KPFM measurements, thanks to the smaller tip sample distance, can offer comparable resolution to lift mode FM-KPFM.[14,17,18]

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The first flexural eigenmode resonance frequency of the cantilever ($f1 = 61.3$ kHz) was used to track the topography. The feedback to measure the CPD of the sample works at a frequency around the second eigenmode resonance frequency of the cantilever[15,19] ($f2 = 380$ kHz, high enough to avoid any KPFM signal dependence on the frequency[20]). An internal algorithm selects the working frequency that maximizes the signals used to nullify the electrically driving oscillation, improving the sensitivity of the measurements. Since the ratio f2/f1 is typically 6.2, self-excitation of the second eigenmode through the 6th-harmonic of the first eigenmode is not present in the measurements, minimizing cross-talk between topography and the CPD image.[21]

To obtain the CPD image, the tip is biased at $VAC = 1$ V, while the TiN layer is directly connected to the ground. Since the CPD data correspond to the difference between the WF of the tip and the metal layer, assuming a constant value of the tip WF during the experiment, the measured CPD variations are related to the WF fluctuations of the metal layer. Therefore, the CPD image provides information on the local value of the WF of the metal. In our case, KPFM images were obtained in air using a highly doped[20] Si tip (radius < 10 nm) from AppNano.

Figure 1(a) presents an 850 nm × 290 nm topographical image of the TiN layer obtained by KPFM at a scanning rate of 0.2 Hz. Note that it shows a granular structure, which has been attributed to the polycrystallization of the metal layer: grains (Gs) are related to individual (or a cluster of) randomly oriented nanocrystals separated by grain boundaries (GBs, depressions in the topographical image).[2] A statistical analysis of the Gs diameter has been done using the image analysis software Gwyddion.[22] Figure 2(a) shows a histogram of the grain diameter suggesting an average diameter (Gdiameter) of ~25.4 nm. These results are compatible with values already reported, which point out a large range of diameters, depending on the growth conditions of the layer.[9,10]

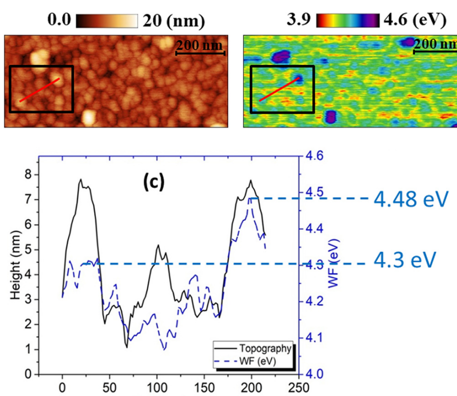

FIG. 1. Topography (a) and WF (b) maps obtained by KPFM on a TiN layer (850 nm × 290 nm). (c) Topographical (continuous line) and the WF (dashed line) profile across the line plotted in (a) and (b).

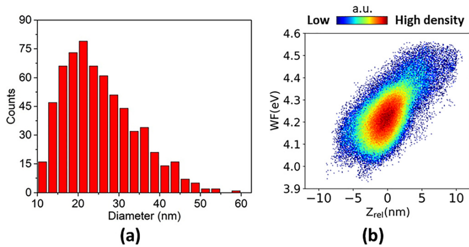

FIG. 2. (a) Histogram showing the distribution of the nanocrystal diameter. The average diameter is 25.4 nm. (b) Relationship between the WF and the topography (Z-axis relative position, Z_{rel}) map pixel by pixel. The color map shows the density of points for each region. Z_{rel} is defined as the Z-position with respect to the Z-axis mean value of the image, which has been arbitrarily considered to be the zero-reference level. The general trend is that depressed areas (regions with low Z_{rel}) show a lower WF.

The effect of metal polycrystallization on the nanoscale WF of the layer was investigated based on the CPD image. Figure 1(b) shows the measured WF in the same surface region as in Fig. 1(a), suggesting that the WF is not uniform. A granular pattern, as also observed in Ref. 23, overlaps with that of the topographical image. Since the tip WF is not known and absolute values of WF are also very sensitive to ambient conditions,[20] it has been assumed that the average value of the CPD image is 4.22 eV, which corresponds to the average WF of a TiN metal gate obtained from experimental devices,[24] and only relative variations will be considered. This assumption does not affect the conclusions of the work because we are interested on the impact of the WF fluctuations on the MOSFET variability.

Figure 1(c) shows a topographical (continuous line) and a WF (dashed line) profile across the line plotted in Figs. 1(a) and 1(b) (inside the black square). Note that, in general, the positions with lower WF are located along the topographical depressions, though Gs with very low WF can also be found. This qualitative observation is verified statistically in Fig. 2(b), where the dependence of the WF with the Z-axis relative position (Z_{rel}, defined as the Z-position with respect to the Z-axis mean value of the image, which has been arbitrarily considered to be the zero-reference level) of all the pixels in Fig. 1 is shown. The color scale of Fig. 2(b) indicates the density of sites with a given WF and Z_{rel}. This figure suggests that, instead of discrete WF values, there is a continuous WF distribution that spans from ~4.0 eV to ~4.5 eV. The depressed areas (low Z_{rel}) tend to show a lower WF than hillocks. Since depressed areas are associated with GBs [as shown in Figs. 1(a) and 1(c)],[2,23] the results indicate that Gs tend to have a higher WF value.

In addition to the WF difference between GBs and Gs, the WF of Gs also shows a continuous distribution. This distribution can be associated with, on the one hand, a non-homogeneous WF in the G or intra-G variability [see, for example, the G located at ~200 nm in Fig. 1(c)] and, on the other, to differences in the WFs between Gs (inter-G variability). To evaluate this inter-G variability, we have considered

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the maximum value of WF as a metric parameter (the same conclusions would have been drawn if the average WF would have been considered instead). Grains with different maximum WF values are measured, as in Ref. 23. As an example, Fig. 1(c) shows two Gs with a similar height and different maximum WF values (4.30 and 4.48 eV), whose difference is ~200 meV. This result is compatible with the presence of two grain orientations, [111] and [200], with 0.2 eV (Ref. 9) WF difference. The presence of crystals with 2 orientations is further supported by XRD analysis. The XRD spectrum of the TiN layer (Fig. 3) reveals the presence of two peaks, corresponding to aforementioned orientations, the [111] orientation being dominant over the other. However, the KPFM map suggests a continuous distribution of values that spans from ~4.29 eV for low WF values to ~4.5 eV for high WF values,[23] within the WF range of the two crystal orientations. A continuous distribution of WFs is also observed for GBs. In this case, however, WFs range from 4.0 to 4.1 eV, so the WF difference between grains and GBs ranges between ~200 meV and ~500 meV.

The data obtained from KPFM images (WF on the nanoscale) add new information on the properties of the polycrystalline metal layer compared to the data used in previous works to simulate WFV. Besides the presence of different grain orientations, we have observed that they do not show discrete WF values but a continuous range of them (due to inter- and/or intra-G variability). Moreover, the presence of GBs with lower WF values is also observed (which were not considered in previous works). Such variations could also affect the electrical characteristics and the variability of semiconductor devices and therefore should be taken into account. In order to demonstrate this, the nanoscale information experimentally obtained by KPFM is introduced in a device simulator to study the variability of MOSFETs (due to the WF fluctuations in the metal gate).

To evaluate the impact of the nanoscale WF fluctuations on the device electrical characteristics, a 3D in-house built finite-element drift-diffusion device simulator[25] was used. For simplicity, a W × L = 50 × 50 nm^2 gate area n-type Si MOSFET with a HfO_2/SiO_2 gate stack was considered. The gate WF value (4.22 eV) and source/drain doping were obtained from the appropriate scaling and calibration of

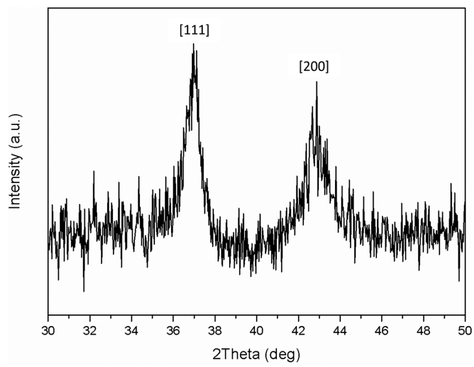

FIG. 3. XRD spectrum of the TiN layer, showing the [111] and [200] orientations of TiN.

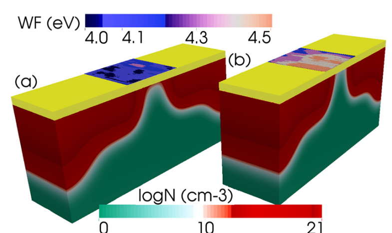

FIG. 4. TiN metal gate experimental profiles that produce the highest (a) and the lowest (b) off-currents when considered as the metal gate of a 50 nm gate length Si MOSFET. The electron concentration inside the device, at $V_G = 0.0$ V and $V_D = 50$ mV, is also shown.

a 67 nm effective gate length MOSFET experimental device.[24] From maps as those shown in Fig. 1, 100 different 50 nm × 50 nm metal gate maps (without overlapping) were obtained and introduced in the device simulator, so that an ensemble of 100 different WF maps (and therefore, device configurations) were analyzed. Figure 4 shows 2 extreme examples of device configurations. Figure 4(a) corresponds to a device with very low TiN WF values (mainly occupied by GBs), while Fig. 4(b) corresponds to a device mainly occupied by Gs with WF values ranging from ~4.29 to ~4.5 eV. The corresponding statistical analysis of 100 MOSFET electrical characteristics is presented in Fig. 5 for the off-current (I_{OFF}), the subthreshold slope (SS), the threshold voltage (V_T), and the on-current (I_{ON}) at a low drain bias of 50 mV. The mean value and the standard deviation (σ) of the distributions are also indicated in this figure. The V_T, I_{OFF}, and SS histograms are clearly asymmetric with behaviors far from the commonly assumed Gaussian distributions, with skewness values ~±1, because

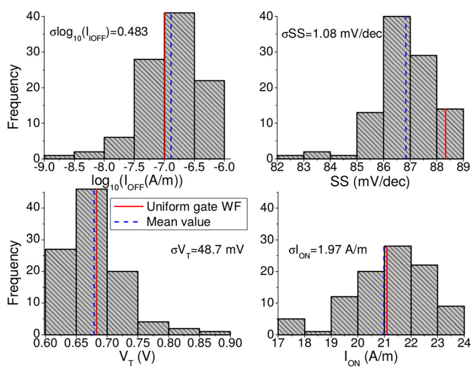

FIG. 5. Distributions of I_{OFF}, SS, V_T, and I_{ON} due to the experimentally observed WFV for a 50 nm gate length Si MOSFET at a drain bias of 50 mV. The mean value and the standard deviation (σ) of the statistical ensembles are indicated, together with the values obtained for a device with a uniform gate WF (set to 4.22 eV).

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of the unbalanced grain WF probabilities. A correlation between G/GB distributions and electrical characteristics of the device can be found, showing, for example, that higher values of the WF [as in Fig. 4(b)] lead to MOSFETs with higher V_T and lower I_{OFF}. Then, from the I_{OFF} and V_T histograms in Fig. 5, it can be concluded that the probability of occurrence of Gs with extremely high WF values (4.5 eV) is extremely low.

To perform a fair comparison between our WF variability results and those previously published by Wang *et al.*,[26] corresponding to a 35 nm gate length (GL) MOSFET, the ratio $G_{diameter}$/GL needs to be used.[27] When comparing results with a similar $G_{diameter}$/GL value of 0.5, our predicted σ V_T ($\sim$49 mV) is around 10% lower than that reported by Wang. These large variability values explain why WFV is currently considered as one of the major sources of variability impacting device's performance. However, most of the previously TiN WFV published studies[26–29] assume that TiN has only two possible WF values spanning 0.2 eV with probabilities of occurrence of 60% and 40%.[30] Our results demonstrate that such an assumption is quite simplistic since in real materials GBs may be present. We have observed a maximum excursion in V_T values of 0.28 V (see Fig. 5), the mean V_T of the distribution being 0.68 V, a value lower than the one obtained for a device with a gate composed only of Gs with extreme low WF values of 4.29 eV (0.75 V). This indicates a huge influence of the GBs (with WF values $\sim$4.0 eV) in the statistical distribution. Note that the gate of the device that exhibits the highest off-current [see Fig. 4(a)] is mainly occupied by GBs and Gs with WF values ranging from $\sim$4.0 to $\sim$4.3 eV. Therefore, the influence of the GBs should not be disregarded when modelling metal gate WFV.

In summary, the impact of metal gate polycrystallization on the variability of MOSFET devices has been studied using a combination of 2D experimental WF maps obtained using KPFM and a device simulator. The KPFM shows WF variations between Gs and GBs (the WF being lower in the GBs). Though two crystal orientations are observed (supported by XRD data), a continuous distribution of WFs is measured. Regions of the WF images have been mapped onto the gate of a MOSFET, to evaluate the device I_D-V_G curves. This procedure is a more realistic approach for the analysis of the device-to-device variability (due to the presence of different grain orientations) since nanoscale differences of the metal WF are considered from direct experimental data. Though TiN layers have been considered as a case study, the proposed methodology can be extended to any metal layer (polycrystalline or not) and growth conditions, since the electrical properties depend only on the WF.

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Combined nanoscale KPFM characterization and device simulation for the evaluation of the MOSFET variability related to metal gate workfunction fluctuations

Ana Ruiz, Natalia Seoane, Sergi Claramunt, Antonio García-Loureiro, Marc Porti, Montserrat Nafría

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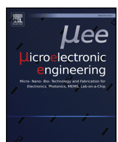

Research paper

Combined nanoscale KPFM characterization and device simulation for the evaluation of the MOSFET variability related to metal gate workfunction fluctuations

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ABSTRACT

In this work, a more realistic approximation based on 2D nanoscale experimental data obtained on a metal layer is presented to investigate the impact of the metal gate polycrystallinity on the MOSFET variability. The nanoscale data (obtained with a Kelvin Probe Force Microscope, KPFM) were introduced in a device simulator to analyze the effect of a TiN metal gate work functions (WF) fluctuations on the MOSFET electrical characteristics. The results demonstrate that the device characteristics are affected not only by the WF fluctuations, but also their spatial distribution, which is specially relevant in very small devices. The effect on these characteristics of the spatial distribution on the gate area of such fluctuations is also evaluated.

1. Introduction

Extensive studies have been devoted to investigate variability sources affecting ultra-scaled MOSFET technologies, as Random Dopant Distributions, Line Edge Roughness, high-k dielectric polycrystallization [1–5], interface traps [6–8] and metal polycrystallization [9–11]. Charges captured in traps located at the semiconductor/insulator interface can lead to fluctuations in the threshold voltage (V_T) and the on-current [12,13] introducing, therefore, device-to-device variability. Such V_T fluctuations also depend on the position of the traps along the channel [13]. Regarding metal gates, the metal polycrystallization results in grains with different sizes and orientations, which have associated different WFs. The random distribution of grains (and the corresponding WF) results in V_T variability (TVV) [9–11]. Some works have already analyzed the impact of the WF fluctuations on the variability of MOSFETs [9,10]. However, the statistical models that were used make assumptions that might not be representative of real devices.

In this work, the impact of metal polycrystallization on the electrical parameters of MOSFETs is studied, based on KPFM experimental WF maps. These results are compared to those obtained using the approximated WF distributions normally used in customary approaches for this kind of variability source. An analysis of the influence of the location of the WF fluctuations along the channel is also studied.

2. Experimental set-up

A 100 nm thick TiN layer grown over a HfO_2/Si substrate was used to obtain the experimental data. The layer was fabricated by continuous e-gun evaporation of metallic TiN. The TiN formation was ensured by passing the Ti atoms through a reactive nitrogen-enriched atmosphere (nitrogen partial pressure of 8×10^{-4} mbars). X-Ray Diffraction (XRD) was used to determine the structure of the TiN layer. The XRD spectrum shows a polycrystalline structure with two peaks [14], that correspond to the [111] and [200] orientations [9]. being the [111] orientation dominant over the [200] one.

The nanoscale morphological and electrical properties of the TiN layer were measured with a Nano-Observer AFM from Concept Scientific Instruments. This technique allows bimodal single pass AM-KPFM measurements, so that it is possible to obtain during the same scan topographical and sample-tip contact potential difference (CPD) 2D maps with nanometer resolution [15,16]. Compared to a lift mode based AM-KPFM (normally with a worse resolution [17–19], our bimodal single pass AM-KPFM can provide a similar resolution to that obtained with a FM-KPFM [17,20] and minimizes cross-talk between topography and the CPD data [18,21]. Since the CPD image corresponds to the WF difference between the tip and the sample, assuming a constant value of the tip WF during the test, the measured CPD fluctuations can be related to the WF variations of the TiN layer. Therefore, CPD maps give information of the local value of the WF of the sample. KPFM images were obtained with highly doped Si tips to get a better

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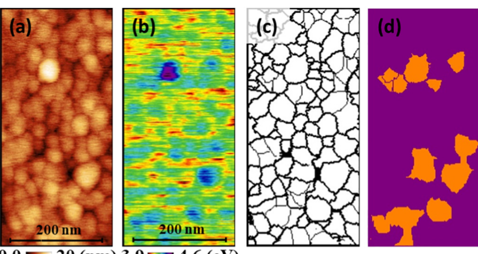

Fig. 1. Topography (a) and WF (b) maps obtained with KPFM on a TiN layer. Binary mask (c) of the grains identified in the topographical map and an example generated WF map (d) from the binary mask. Orange color corresponds to 4.5 eV and purple color to 4.3 eV. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

resolution.

3. Experimental results

Fig. 1a corresponds to a 520 nm × 240 nm topographical image of the TiN layer. It shows a granular structure, where the Grains (Gs) are surrounded by grain boundaries (GBs), which correspond to the depressions in the image. Fig. 1b shows the measured WF map of the same surface region. Note that GBs tend to show lower WFs (WF < 4.1 eV) than nanocrystals.

We used the open-source software Gwyddion to identify the Gs and obtain the TiN granular pattern (Fig. 1c), where the GBs have been neglected. When only nanocrystals are considered, Gs with different maximum WF values are measured, as shown in Fig. 2, which corresponds to a 2D-histogram that relates the maximum WF and the maximum height (with respect to the mean height value of the topographical image shown in Fig. 1a) of each grain in Fig. 1c. Note that although a continuous distribution of maximum WFs is obtained, WFs are mostly concentrated at ~4.3 eV and, with less frequency, around ~4.5 eV, suggesting two predominant WFs and indicating a much higher number of nanocrystals with low WF than with high WF. This result, confirmed by XRD [14], is compatible with the presence of two grain orientations in the TiN layer ([111] and [200]) whose WFs are separated by 200 mV [9].

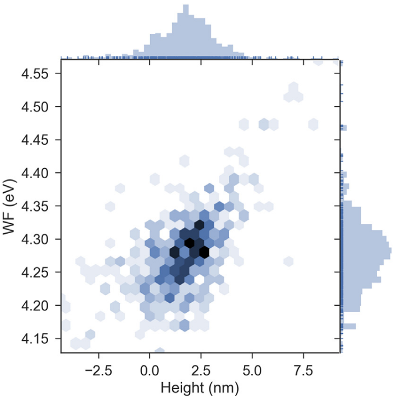

Fig. 2. 2D-histogram showing the maximum WF vs maximum height of the grains, obtained from Fig. 1c. In the X axis, the height of each grain is determined with respect to the mean value of the topographical image (Fig. 1a).

The data obtained from KPFM images add new information on the properties of the polycrystalline metal layer, not taken into account in previous works. Besides the dispersion in the WF of the nanocrystals (not only two discrete values are measured), GBs with lower WF than Gs are also observed, which could also affect the variability of devices. Therefore, all these features should be taken into account when studying the MOSFET variability and when considering the WF fluctuations as variability source.

4. Simulations

In order to evaluate the device variability associated to the WF fluctuations of the TiN layer, different WF distributions representing the metal gate of a MOSFET were considered. WF maps as those shown in Fig. 1 have been divided to generate 100 non-overlapping 50 nm × 50 nm gate WF profiles. Next, these profiles were introduced in a 3D in-house-built drift-diffusion device simulator [22] as metal gate, to evaluate the device electrical characteristics of MOSFETs with a gate area of 50 × 50 nm^2. In order to compare the results obtained with our methodology, based on nanoscale experimental data, with those shown in the literature, we proposed the study of two cases: (i) the actual WF distribution (as in Fig. 1b, with GBs and a continuous distribution of Gs WF), and (ii) an approximated WF distribution, with two discrete values of the WF, as in Fig. 1d. Note that the last is the customary approach for this kind of TVV source [9]. To generate the approximated WF maps (Fig. 1d), the grain pattern in Fig. 1c is the starting point. We generated an approximated WF maps where GBs have been neglected and, for the Gs in Fig. 1c, two discrete and constant values, corresponding to the [111] and [200] orientations (confirmed from XRD analysis), were only considered. We have assigned 4.3 eV to the nanocrystals with WF lower than 4.4 eV and 4.5 eV to those with higher values, leading to WF maps as that shown in Fig. 1d. The MOSFET behavior for devices with metal gate WF distributions obtained from the WF maps as in Fig. 1b and d have been compared.

Fig. 3 shows the off-current (I_{OFF}), threshold voltage (V_T) and on-current (I_{ON}) distributions obtained for these two cases. Note that, the approximate case (i. e., disregarding the GBs and the WF continuous distribution), in the right column, leads to a ~10% and ~18% reduction in σV_T and $\sigma\log(I_{OFF})$, respectively, and to a considerable shift (~0.12 V in the case of the V_T) in the mean value of the distributions.

To better understand these results, the effect of the spatial location of the Gs in the MOSFET metal gate has also been evaluated. As an example, Fig. 4 shows the gate of two devices in which only one nanocrystal has been included. The average WF of the grains is 4.3 eV for grain (a) and 4.18 eV for grain (b). Since, in this section, we want to evaluate only the impact on V_T of the position of the grains in the channel, the WF of the portion of the gate not covered by the nanocrystal has been set to same average value, that is, 4.3 eV for Fig. 4a and 4.18 eV for Fig. 4b. The G has been swept along the device gate, from the source end (X = 0 nm) to the drain end (X = 50 nm), and for each position of the grain, the device was simulated and the corresponding V_T extracted. Fig. 5 shows the V_T variation with respect to the homogeneous case when the grain position is swept, at both low and high drain biases. Note that, although the distribution of WF is the same in all cases, the specific location of the G may have a different impact on the V_T values (depending on its position along L), leading to both positive and negative threshold voltage shifts with respect to the grain average WF value. In addition, the device is clearly more sensitive to WF variations at the source end than at the drain end (as seen in Fig. 5 for both grains). At the drain end, the presence of the grain does not have any influence on V_T. The drain bias also has an influence on the TVV, as seen on Fig. 5. However, when the grains were swept along the y-direction (i.e. along the width of the gate area), no significant changes are observed in V_T.

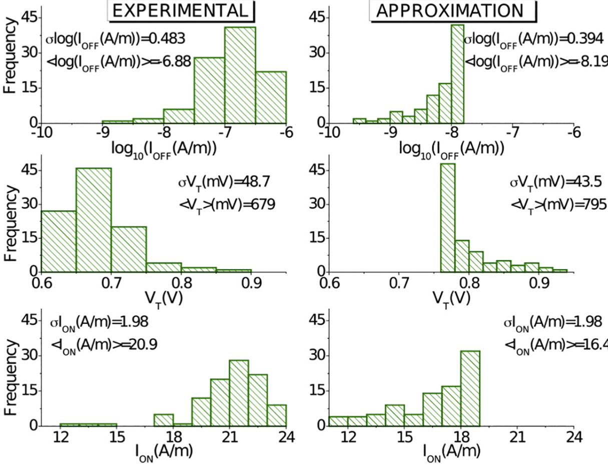

Fig. 3. Distributions of I_{OFF} (top), V_T (middle) and I_{ON} (bottom) related to W_F fluctuations in 50 nm × 50 nm Si MOSFETs (at a drain bias of 50 mV) when using actual WF data (left column) an approximated WF (right column) from maps as those shown in Fig. 1b and d respectively. The mean value (< >) and standard deviation (σ) of the statistical ensembles are shown.

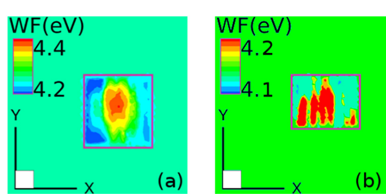

Fig. 4. Two examples of isolated nanocrystals (enclosed in pink rectangles), with average WF values < WF > of 4.3 eV, grain (a), and 4.18, grain (b). The larger green squares show the real dimensions of the 50 × 50 nm device gate. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

Therefore, the results demonstrate that, not only the WF values of the grains in the metal gate can impact on the MOSFET variability, but also V_T depends on how those fluctuations are distributed along the channel direction. This dependence of V_T on the G position can be explained taking into account the impact of the WF fluctuations on the electrostatics of the device. Depending on the G location, the potential distribution in the channel is affected differently, leading to variations of V_T. A similar effect was observed for other sources of variability, as is the case of interface traps in ultra-scaled MOSFETs [6].

5. Conclusion

When analyzing the impact of the WF fluctuations of polycrystalline metal gates on the MOSFET variability, the presence of GBs and the WF continuous distribution of the Gs need to be considered to obtain more realistic data. Moreover, the device characteristics and variability are also affected by the spatial distribution of such fluctuations: in small devices, where few nanocrystals may be present in the gate area, their location should also be considered in order to correctly estimate the variability at device level.

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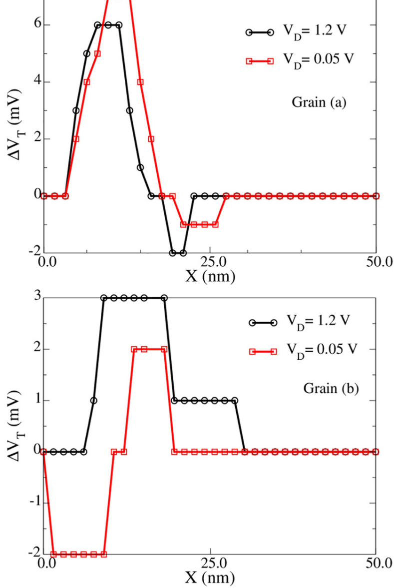

Fig. 5. V_T spatial sensitivity to a TiN grain WF fluctuations when its position is swept along the channel of the Si MOSFET at both low and high drain biases like those shown in Fig. 4a and b have seen considered for the simulation. ΔV_T is calculated as the difference between the V_T of a device with a gate WF equal to the < WF > of the G and the V_T of the device that includes the nanocrystal.

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Methodology for the Simulation of the Variability of MOSFETs With Polycrystalline High-k Dielectrics Using CAFM Input Data

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ABSTRACT In this work, a simulation methodology, whose inputs are Conductive Atomic Force Microscope (CAFM) experimental data, is proposed to evaluate the impact of nanoscale variability sources related to the polycrystallization of high-k dielectrics (i.e., oxide thickness, t_{ox}, and charge density, ρ_{ox}, fluctuations in the nanometer range) on the Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) variability. To simulate this variability, a Thickness And Charge MAp Generator (TACMAG) has been developed and used in combination with an in-house-built 3D device simulator (VENDES). From CAFM experimental data (topography and current) obtained on a small area of a given polycrystalline dielectric, the TACMAG generates a high amount of t_{ox} and ρ_{ox} configurations of the gate dielectric, with identical statistical characteristics to those experimentally measured. These dielectrics are then introduced into the device simulator, with which the impact of the t_{ox} and ρ_{ox} fluctuations in the dielectric on the variability of MOSFETs (i.e., threshold voltage) is analyzed. Finally, the impact of different nanoscale parameters, such as the Grain size and Grain Boundaries depth (of polycrystalline dielectrics) on such variability has been evaluated.

INDEX TERMS CAFM, high-k, MOSFET variability, polycrystalline dielectric, defect density, 3D device simulations.

I. INTRODUCTION

The continuous scaling of Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET) devices has driven the exploration of new materials [1]. For instance, to limit the gate leakage current, ultra-thin Silicon Dioxide (SiO_2) gate oxide has been replaced by high-k dielectrics [2]. However, some high-k materials show a polycrystalline structure [3], [4], which could affect the electrical properties of scaled devices [5] by increasing the leakage current and the device-to-device variability. Since high-k polycrystallization takes place at the nanometer scale [4], Conductive Atomic Force Microscopy (C-AFM) has been demonstrated to be a very powerful technique to evaluate at the suitable scale the morphological and electrical properties [6]–[10] of polycrystalline high-k dielectrics [11]–[15]. As an example, it has been found that in some polycrystalline Hafnium Dioxide (HfO_2) layers, the gate leakage current mainly flows through grain boundaries (GBs) [16], where a reduced oxide thickness (t_{ox}) was measured [3]. Moreover, the presence of defects has been observed at the GBs, which were associated to an excess of oxygen vacancies [3], [16].

Traditionally, due to the lack of experimental data, variability studies are done via the implementation of physical models that mimic the real behavior of the sources of fluctuations [5], [17], [18]. However, more recently a new methodology was proposed in [11]. It consisted in the simulation (using Technology Computer-Aided Design,

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TCAD [19]) of the I-V curves of MOSFETs whose gate oxide properties were directly determined from experimental data. In this way, it was possible to better link variability sources at the nanoscale with the variability of figures of merit of MOSFETs. In particular, a CAFM was used to measure topographical and current maps of polycrystalline high-k dielectrics (from which nanoscale t_{ox} and charge density, ρ_{ox} maps were obtained [11]) and a simulator was used to evaluate their impact on the MOSFET threshold voltage (V_{th}). However, in that work, a statistical analysis was not possible. Only small regions of a particular sample were measured, so that the number of MOSFETs instances available for the analysis of the variability of V_{th} and ON and OFF currents (I_{on} and I_{off}) was rather limited. In addition, the complete evaluation of the impact of the different parameters that describe the polycrystallization of high-k dielectrics (as the grain size, Grain Boundaries depth and/or width, etc) was not allowed. On one hand, because samples obtained with other growth parameters (which result in different polycrystallinity properties) are not always available. On the other, because it would be necessary a lot of experimental measurements, which is very expensive and time consuming.

The focus of this work is to propose a complete simulation flow to statistically evaluate the impact of polycrystalline high-k dielectrics on the MOSFET variability, starting from experimental nanoscale data obtained with a C-AFM. With the proposed methodology, less experimental measurements and samples with different characteristics are needed, reducing the cost and time of such analysis. At this point, only the high-k polycristallinity is considered as variability source, but it could be afterwards combined with others to investigate their global effect on the device [20].

II. EXPERIMENTAL

A. SET UP AND DEVICE STRUCTURE

Nanoscale data, that is, t_{ox} and ρ_{ox} and their fluctuations in the nanometer range, were obtained with CAFM on a sample containing a 5.3 nm thick HfO_2 film deposited by Atomic Layer Deposition (ALD) on a 0.7 nm thick SiO_2 layer. The average thickness of both layers was measured by X-Ray Reflectivity. The gate stack was grown on a Si epitaxial P-substrate. With the aim of studying the impact of the polycrystalline dielectric structure on the MOSFET device variability, an annealing process was carried out at 1000 °C, which lead to the polycrystallization of the high-k layer. The presence of the SiO_2 layer was taken into account during the TCAD simulations, as reported in [11]. However, SiO_2 charges and t_{ox} fluctuations in SiO_2 were considered to be negligible when compared to those linked to the polycrystalline high-k dielectric. This is justified by the fact that SiO_2 is not polycrystalline and because the amount of charges is expected to be larger in HfO_2 than in SiO_2. So, the measured t_{ox} and ρ_{ox} fluctuations are assumed to be related to the polycrystalline high-k.

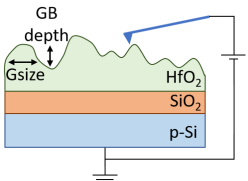

FIGURE 1. Schematic of the set up and device structure.

Figure 1 shows a schematic of the CAFM experimental set up. Note that no top electrode is used. Actually, the tip of the CAFM plays the role of the top electrode, defining a Metal-Oxide-Semiconductor structure whose size is determined by the tip-sample contact area, which is ~100nm^2 [21]. With this experimental configuration, morphological and current maps of different kinds of materials (as high-k dielectrics [12], [13], [22], [23]) can be measured with a nanometer resolution. Current maps correspond to the x-y spatial distribution of the tunneling currents flowing between the gate and the substrate, through the dielectric layer.

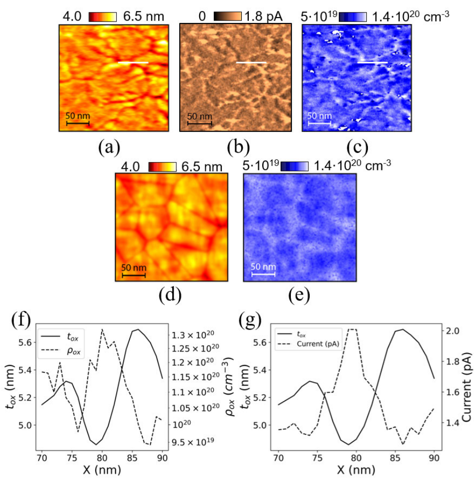

FIGURE 2. Morphological (a) and current (b) maps obtained at V_G = 6.5V on a HfO_2/SiO_2/p-Si structure (230 nm x 230 nm). (c) corresponds to the charge density map estimated from (a) and (b). The white line highlights a GB (depression in the morphological image), which shows higher current and charge density than that observed in the Grains (see profiles along the white line in (f) and (g)). Generated morphological (d) and charge density (e) maps obtained with TACMAG.

B. CAFM EXPERIMENTAL DATA

Figures 2a and 2b show, respectively, an experimental morphological and current map obtained with a CAFM in vacuum and using a diamond-coated tip. The current map was obtained at 6.5V, because it was the minimum voltage at which current above the noise level of the setup was

measured. From both maps, the corresponding charge density map (Fig. 2c) has been estimated using the methodology shown in [11]. It can be observed that there is a clear correlation between the three images. Higher currents and charge densities are measured at GBs (deeper areas in the morphological map). These larger values are assumed to be related to oxygen vacancies by incomplete atomic bonds between hafnium and oxygen [24], [25]. As examples, profiles of the morphological, current and ρ_{ox} maps through a particular GB (highlighted in the images) are shown in Fig. 2f-g. Note that direct information about the oxide thickness t_{ox} cannot be obtained from the morphological image. This is because t_{ox} depends not only on the characteristics of the scanned top (dielectric/gate) interface (Fig. 2a), but also on that of the dielectric/substrate interface, and this information is not available in this kind of experiment. However, Fig. 2a suggests that t_{ox} is smaller at the grain boundaries [26], [27]. Actually, t_{ox} at each pixel of the surface of Fig. 2a was estimated [11] by assuming that the average thickness of the oxide layer, 5.3nm, corresponds to the average height of the morphological map. Any height deviation with respect to the morphological average at any site of Fig. 2a has been attributed to a deviation from the average t_{ox} of the same value. Then, any morphological map can be interpreted also as a t_{ox} map, as it will be done from now on.

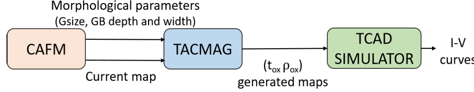

FIGURE 3. Flow diagram showing the different steps of the simulation methodology.

III. SIMULATION TOOLS

The proposed simulation methodology is based on two independent simulators, which are executed sequentially. Fig 3 shows the complete flow of data, covering from the experimental information obtained with CAFM to the analysis of the variability of MOSFETs. First, the TACMAG software (Thickness And Charge MAp Generator) is used, with which multiple (t_{ox}, ρ_{ox}) maps of gate oxides are generated (output) from the experimental morphological and current maps measured with CAFM (input). Secondly, a homemade Semiconductor Device Simulator is used, which takes the output (t_{ox}, ρ_{ox}) maps of TACMAG as input data and simulates the MOSFET electrical characteristics. As a result, the impact of the nanoscale fluctuations of t_{ox} and ρ_{ox} in the dielectric on the device I-V characteristics and the device-to device variability in MOSFETs can be evaluated. Both simulators are described in detail in the following sections.

A. THICKNESS AND CHARGE MAP GENERATOR (TACMAG)

The core of the Thickness And Charge MAp Generator (TACMAG) was partially developed in [28]. In the generator developed in [28], from the AFM measurement of morphological maps of a polycrystalline sample, 3 Dimension (3D) topographical maps could be reproduced with the same statistical morphological characteristics as the experimental sample under study [28]. Moreover, in [11], from pairs of experimental morphological and current maps obtained with CAFM (on the same area), the local charge density was also calculated at each position of the gate oxide. The present work, however, goes one step further, and improves and develops new capabilities of that simulator, called from now on TACMAG, which are necessary to evaluate the impact of the nanoscale properties on the device variability.

On one hand, in order to optimize the generation of morphological maps, in the new version of the generator, that is, in TACMAG, the methodology used to statistically reproduce the sample morphology has been improved by using the Poisson-Voronoi diagrams, which are commonly used to generate polycrystalline grain structures [29]–[31]. Implementing this new technique, the inputs needed to create the grain structure of new samples are reduced, simplifying the map generation. Now, only the grain size (Gsize), GB width and depth (and their corresponding statistics) are necessary, which are easily obtained from experimental data (Fig. 2a). Fig. 2d shows an example of a generated morphological map whose statistical parameters are the same as those that describe Fig. 2a.

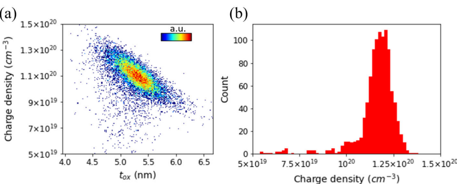

FIGURE 4. (a) ρ_{ox} values calculated from Fig. 2a and 2b, and shown in Fig. 2c, as a function of t_{ox} (Fig. 2a) for all the pixels of Fig. 2a and 2c. The histogram on (b) shows the $\rho_{ox}(t_{ox})$ distribution for a t_{ox} = 5nm (interval between 4.95 and 5.05 nm).

On the other hand, the new version of the generator (TACMAG) has also been extended to generate 2D charge density maps (i.e., the inputs of the Device simulator). To do that, first of all, from morphological and current maps experimentally obtained with CAFM (Fig. 2a and b), we use the methodology shown in [11] to calculate the corresponding ρ_{ox} map (Fig. 2c). Fig. 4a shows the calculated ρ_{ox} values (Fig. 2c) as a function of t_{ox} (Fig. 2a) for all the pixels of Fig. 2a and 2c. Note that there seems to be a correlation between t_{ox} and its corresponding charge density (statistically, higher densities were found at GBs, which have smaller thicknesses). However, this relation is not univocal: for a given t_{ox}, a distribution of ρ_{ox} has been found. Fig. 4b also shows an example of a statistical distribution of charge for t_{ox} = 5 nm (interval between 4.95 and 5.05 nm). The $\rho_{ox}(t_{ox})$ statistical distributions have been determined and have been used as an input of the TACMAG to generate (t_{ox}, ρ_{ox}) maps of the dielectric. That is, for a given pixel of a generated morphological map (characterized by a given t_{ox}),

the ρ_{ox} value has been determined by applying Montecarlo methods, considering the ρ_{ox} distribution found for that value of t_{ox}. As an example, Fig. 2e shows the generated ρ_{ox} map obtained for the morphological map in Fig. 2d.

So, to sum up this section, from the input morphological parameters (Grain size, GB width and depth and their corresponding statistics obtained from morphological maps) and current maps obtained with CAFM, TACMAG calculates the charge density distributions (ρ_{ox}, which depends on t_{ox}), and provides (t_{ox}, ρ_{ox}) maps at the output (Fig. 3).

B. 3D DEVICE SIMULATOR

To evaluate the impact of the nanoscale t_{ox} and ρ_{ox} fluctuations in polycrystalline dielectrics on the device variability of MOSFETs, a 3D in-house built parallel drift-diffusion (DD) Device Simulator (named VENDES) [19] was used, which allows to obtain the I_G-V_D characteristics of MOSFETs. The finite-element method (FEM) has been applied to discretize the simulation domain, which allows the simulation of complex device shapes with great flexibility. In addition, the use of FEM-based meshes allows to easily incorporate and model non-uniform effects (such as variability sources) affecting the device, that might require the deformation of the structure. On every node of the three-dimensional tetrahedral mesh, the classical electrostatic potential is obtained via the solution of the Poisson equation. In order to incorporate quantum mechanical corrections, this classical potential is corrected through the density-gradient (DG) approach. To model the transport inside the semiconductor, the quantum-corrected electrostatic potential is coupled with the current continuity equation for electrons, to obtain the electron current density that flows inside the device. To account for the carrier transport in the MOSFET device, VENDES incorporates the Caughey-Thomas doping dependent electron mobility model [32], to describe low electric field transport, coupled with perpendicular and lateral electric field models [33], that represent high field carrier transport. A more detailed description of the simulation methodology can be found in [19]. This 3D DD-DG simulator has been widely employed in the modelling of different sources of variability affecting semiconductor devices, such as random dopants [34], line-edge roughness [35], [36], or grains in the metal gate [34], [35], [37], [38].

In this work, this simulator has been used to evaluate the impact of high-k dielectric polycrystallization on the V_{th} variability of MOSFETs. With this purpose, a Width (W) x Length (L) = 50 × 50 nm^2 gate area n-type Si MOSFET with a HfO_2/SiO_2 gate stack was considered as a test device. The device dimensions and doping values were obtained from the constant field scaling [39] of a n-type 67 nm effective gate length MOSFET that was calibrated against experimental data [37]. To simulate the Drain current vs. Gate Voltage (I_D-V_G) curves of different devices, nanoscale (t_{ox}, ρ_{ox}) dielectric maps with a 50 × 50 nm^2 size (the area of the gate region), extracted from Fig. 2, were considered as inputs of the Device Simulator. The introduced maps can be either directly measured (i.e, 50 × 50 nm^2 portions of Fig. 2a and 2c) or generated (in Fig. 2d-e).

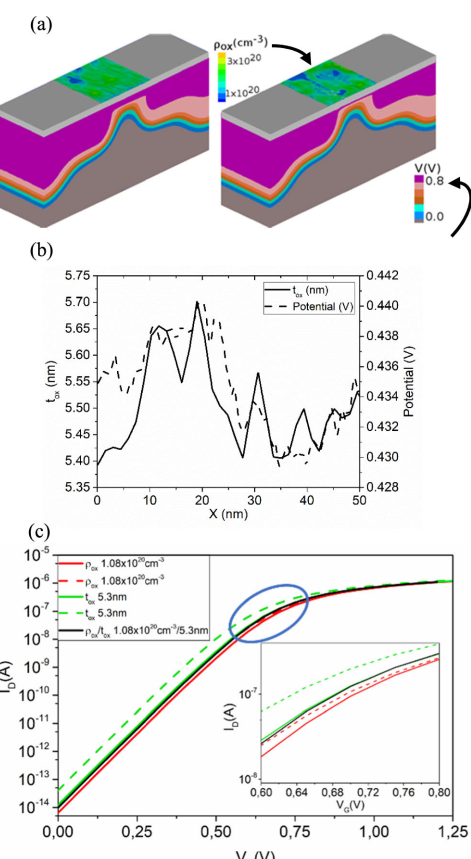

FIGURE 5. **(a) Electrostatic potential inside the 50 × 50 nm^2 MOSFET device for the two particular configurations that produce the largest (left) and lowest (right) drain currents (at V_G = 0.6 V and V_D = 0.05 V) when considering both ρ_{ox} and t_{ox} fluctuations in the device gate. (b) Example of electrostatic potential in the channel (dashed line) and t_{ox} profile (continuous line), (c) I_D-V_G characteristics simulated at V_D = 50 mV for the two configurations shown in (a) when different variability sources are analyzed. Red curves correspond to the simulated I_D-V_G curves of devices with dielectrics with constant ρ_{ox} = 1.08 × 10^{20} cm^{-3} and with the t_{ox} fluctuations taken from (a). Green curves correspond to the simulated I_D-V_G curves of devices with dielectrics with constant t_{ox} = 5.3 nm and with the ρ_{ox} fluctuations taken from (a). Black curve corresponds to a device with constant ρ_{ox} and t_{ox} (same values as for the two other considered cases). The inset corresponds to a zoom of the I-V curves inside the circle, showing V_G in the 0.6V to 0.8V range.**

As simulation example, Fig. 5a shows a 3D view of the electrostatic potential (cross section) and charge density (top view) for the two device configurations that produce the largest (left figure) and lowest (right figure) drain currents

(at $V_G = 0.6$ V and $V_D = 0.05$ V) when considering both ρ_{ox} and t_{ox} fluctuations in the device gate. The t_{ox} maps of both configurations are not shown, for simplicity. Fig 5b shows, as example, a 1D thickness profile of the high-k dielectric (continuous line). It has been extracted in the center of the channel perpendicular to the transport direction. The corresponding electrostatic potential inside the channel is also plotted (dashed line). Note that the potential is not constant, but depends on the thickness fluctuations. In this case, in those regions with smaller thickness (associated to GBs), a lower potential is found. Since the presence of GBs is related to the polycrystallization of the materials, the results demonstrate that polycrystalization clearly affects the potential distribution in the channel. Fig. 5c shows the I_D-V_G curves at $V_D = 50$ mV for the MOSFET configurations of Fig. 5a with different gate oxides characteristics. The inset corresponds to a zoom of the same plot, to better display the differences among the different I_D-V_G. curves. First, the impact of t_{ox} and ρ_{ox} fluctuations have been separately evaluated, as unique nanoscale variability source. Red I_D-V_G curves in Fig. 5c correspond to two particular devices, characterized by gate dielectrics with constant $\rho_{ox} = 1.08 \times 10^{20}$ cm^{-3} (average charge density estimated from Fig. 2c). The t_{ox} fluctuations were introduced by considering the 50 × 50 nm^2 regions of Fig. 5a. Green I_D-V_G curves in Fig. 5c correspond to two particular examples of devices with constant $t_{ox} = 5.3$ nm (average thickness) and two 50 × 50 nm^2 ρ_{ox} maps corresponding to the configurations of Fig. 5a. Finally, both sources are considered simultaneously, i.e., fluctuations in both, ρ_{ox} and t_{ox} parameters. The morphology of the dielectric corresponds to that of Fig. 5a, with charge distributions following the same spatial pattern (for clarity, the resulting curves are not shown in Fig. 5). As reference, the I_D-V_G curve of the device with constant $\rho_{ox} = 1.08 \times 10^{20}$ cm^{-3} and $t_{ox} = 5.3$ nm has also been plotted in Fig. 5c (black curve).

The two I_D-V_G curves of each set of simulated devices show different conduction levels (see Fig. 5c and the inset), which correspond to different V_{th} values. To extract V_{th}, a constant current criterion was used. V_{th} was chosen as the gate bias for which a drain current of 1.4 A/m was obtained. With this criterion, V_{th} is 0.664 V/ 0.675 V when ρ_{ox} is constant (red curves), 0.606 V / 0.654 V when t_{ox} is constant (green curves) and 0.628 V / 0.678 V when t_{ox} and ρ_{ox} fluctuations are considered, respectively. The V_{th} of the device with constant t_{ox} and ρ_{ox} is 0.656 V (black curve). These results indicate, first, that ρ_{ox} and t_{ox} fluctuations lead to different MOSFET electrical properties, and, second, that their impact changes when considered individually or combined. Therefore, the proposed simulation methodology can detect and evaluate the differences in their impact. It is important to emphasize that Fig 5c shows two particular cases, therefore they do not correspond to a statistical analysis, which will be shown in next sections. But before using our simulation tools to evaluate in more detail the impact of the high-k polycrystallization on MOSFETs V_{th} variability, the TACMAG results representativeness will be first verified.

C. TACMAG VERIFICATION

To verify that TACMAG is able to generate statistically representative (t_{ox}, ρ_{ox}) maps of the sample under study, the V_{th} variability of MOSFETs whose dielectric is described by generated (t_{ox}, ρ_{ox}) maps has been compared to that obtained when experimental data are used. In particular, from images as those shown in Fig. 2, 100 different 50 × 50 nm^2 (t_{ox}, ρ_{ox}) experimental (obtained from images like those shown in Fig. 2a-c) and 100 generated maps (obtained with TACMAG, as in Fig. 2d-e) were introduced into the Device Simulator to set the gate oxide properties of the MOSFETs, so that an ensemble of 100 different devices were analyzed for each case [26].

In order to verify the goodness of the TACMAG results for each of the considered variability sources (t_{ox} and ρ_{ox}), 3 different cases have been evaluated. First, t_{ox} is the only source of variability (being ρ_{ox} constant and equal to the average charge density found from Fig. 2c, that is 1.08×10^{20} cm^{-3}), second, ρ_{ox} is the only source of variability (being t_{ox} constant and equal to 5.3 nm, i.e. the measured average thickness of the sample) and, third, both variability sources are combined. For all the devices, the I_D-V_G characteristics were simulated and V_{th} was estimated. A statistical analysis of V_{th} (mean and standard deviation, σV_{th}) for the three cases has been done and the results are shown in Table 1. Note that, for the three cases, the statistics of the devices with experimentally obtained and simulated dielectric are very similar. In particular, for a 100 devices sample size, the difference between σV_{th} (indicative of the V_{th} variability) of both kinds of devices is <2 mV (representing, for example, an error of ∼7.7% for the case when both variability sources are considered). For the average V_{th}, for the same case, a difference of 17 mV is found, which corresponds to an error of 2.6%. These results indicate that the maps obtained by TACMAG (both, t_{ox} and ρ_{ox}) are representative of the sample under analysis. Therefore, the results demonstrate that the proposed simulation methodology and, in particular TACMAG, can be used for an accurate analysis of MOSFET variability.

TABLE 1. Average and standard deviation of V_{th} obtained from 100 devices with the device simulator, when the gate oxide characteristics have been set from experimental data (first row) and maps generated with TACMAG (second row). The different columns show the impact of the different nanoscale variability sources (t_{ox} and/or ρ_{ox}).

	V_{th} (V)		
	Only t_{ox}	Only ρ_{ox}	t_{ox} and ρ_{ox}
Experimental	0.681±0.004	0.640±0.028	0.650±0.012
Generated	0.680±0.005	0.654±0.030	0.667±0.013

IV. CASE OF STUDY: IMPACT OF THE HfO_2 POLYCRYSTALLIZATION ON THE VTH VARIABILITY

In this section, the methodology described in Section III has been used to evaluate in more detail the impact of the polycrystallization of the HfO_2 layer on the V_{th} variability of MOSFETs, as an example. Two cases of study will be considered. In both cases, since the aim is simply to show the capabilities of the proposed methodology, only 100 devices have been simulated, to reduce the simulation time. With this sample size, the relative standard error is around 5% (see section III.C). To reduce this error and obtain more accurate values of V_{th} and σV_{th} for a given gate dielectric, the proposed methodology could be extended to a larger number of devices by simply generating enough t_{ox} and ρ_{ox} maps with TACMAG.

A. CORRELATION BETWEEN t_{ox} AND ρ_{ox} ON THE IMPACT ON V_{th} VARIABILITY

We have started by analyzing the impact of t_{ox} and ρ_{ox} fluctuations on V_{th}. Remember that in Fig. 4, a correlation between t_{ox} and ρ_{ox} (at the nanoscale) was observed. Therefore, one could wonder if, when analyzing their impact on V_{th} (at device level), the impact of both variability sources is (or not) somehow correlated too. Taking advantage of the versatility and capabilities of our simulation tools, the impact of both variability sources has been studied individually and when they are combined. In particular, we have considered for this analysis the data in Table 1, second row, where V_{th} and σV_{th} were determined from the t_{ox} and ρ_{ox} maps generated with TACMAG. Note that, regarding the average value of V_{th}, t_{ox} fluctuations have a higher impact (V_{th} increases from 0.657 V for the reference case to 0.680 V) than ρ_{ox} variations (in this case it remains almost equal, changing only from 0.657 V to 0.654 V). Regarding the standard deviation, when both variability sources are analyzed independently, σV_{th} due to ρ_{ox} (30 mV) is 6 times larger than that due to t_{ox} only (5 mV). So, for the case of the sample analyzed in this work, charge density fluctuations introduce larger V_{th} variability than those related to the gate oxide morphology. However, note also that when both variability sources are combined, the V_{th} deviation is in between those obtained when the two variability sources are considered separately. In particular, the global V_{th} deviation does not correspond to the expected addition of independent variability sources, but it is reduced when compared with the impact of ρ_{ox}. These data suggest that, on one hand, ρ_{ox} and t_{ox} impacts on V_{th} are not independent (as suggested in Fig 4) and, on the other, t_{ox} and ρ_{ox} fluctuations are somehow compensated.

We have investigated the correlation between ρ_{ox} and t_{ox} and its impact on V_{th} in more detail. Figure 6 shows the probability plot (color scale), obtained from the data shown in Table 1 (second row, generated maps, first and second columns) of finding devices with V_{th}'s related to t_{ox} variation only (X-axis) and V_{th}'s related to ρ_{ox} variation only (Y-axis). Note that, for a given value of V_{th} in the X axis (i.e., only

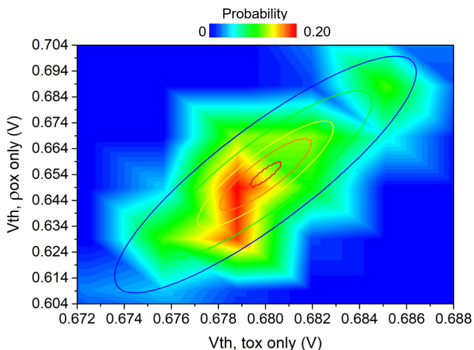

FIGURE 6. Probability (color scale) of finding devices as a function of the V_{th} linked to t_{ox} fluctuations only (X-axis) and V_{th} linked to ρ_{ox} variations only (Y-axis).

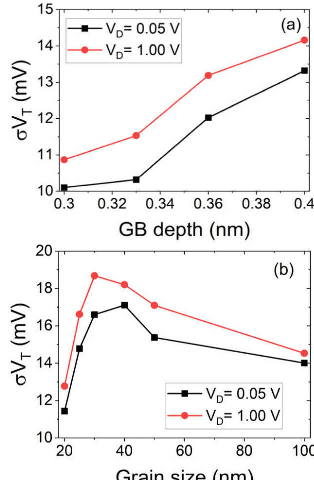

FIGURE 7. Particular examples of how morphological parameters involved in polycrystalline high-k dielectrics affect the V_{th} variability of MOSFETs at 0.05 and 1.0 V drain biases. (a) and (b) show, respectively, the V_{th} deviation for different values of the GB depth (a) and grain size (b).

t_{ox} fluctuations), a distribution of different V_{th} values in the Y axis (i.e., only ρ_{ox} variations) is observed. The inclination of the obtained probability plot suggests that both variability sources are not independent when analyzing their impact on the V_{th} of devices. To quantify this correlation, the data shown in Fig. 6 has been fitted to a bivariate equation (equation 1), being σ_x and σ_y the standard deviation found for the case when only t_{ox} or ρ_{ox} fluctuations were taken into account (that is, 0.005 and 0.030 V, respectively), μ_x and μ_y the average V_{th} (0.680 and 0.654 V, respectively) and ρ the correlation coefficient. Leaving ρ as free parameter, R-square = 0.85, demonstrating that our data can be really fitted to a bivariate

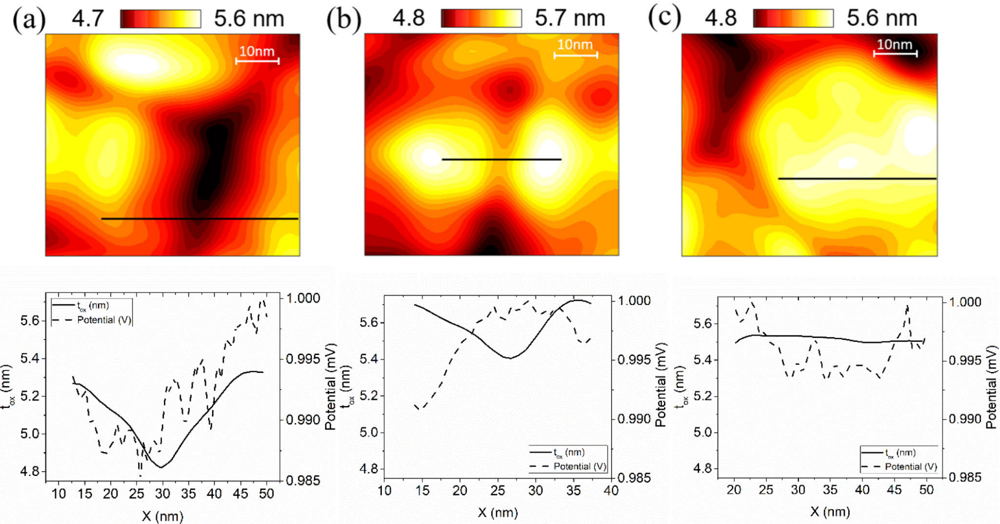

FIGURE 8. t_{ox} maps of different gate oxide configurations including (a) a deep GB, (b) a shallow GB between two Grains and (c) a big grain. In all cases, the electrostatic potential (dashed line) and t_{ox} profile (continuous line) along the black lines indicated in the maps are shown below.

equation. The best fitting was for $\rho = 0{,}79$, which indicates that both sources of variability are correlated.

$$f(x,y) = \frac{1}{2\pi\sigma_X\sigma_Y\sqrt{1-\rho^2}} \times \exp\left(-\frac{1}{2\left(1-\rho^2\right)}\left[\frac{(x-\mu_X)^2}{\sigma_X^2}+\frac{(y-\mu_Y)^2}{\sigma_Y^2} - \frac{2\rho\,(x-\mu_X)\,(y-\mu_Y)}{\sigma_X\sigma_Y}\right]\right) \quad (1)$$

These results clearly demonstrate that in the HfO_2 layer studied in this work, the correlation between the polycrystalline morphology and the charge density (higher at GBs, already observed in Fig. 2 and [11]) implies that when considered together as variability sources (as it happens in real devices), the V_{th} variability does not correspond to the addition of the associated variabilities but, in our case, is smaller than the one observed when only ρ_{ox} is considered. Therefore, the main conclusion of this section is that, although other variability sources affecting MOSFETs may be studied independently [20], [40], variability sources affecting the polycrystalline gate oxides are correlated and cannot be studied as independent statistical variables if an accurate analysis has to be performed.

B. IMPACT OF GRAIN SIZE AND GB DEPTH ON THE V_{th} VARIABILITY

One of the main characteristics of TACMAG is that, thanks to the possibility of generating (ρ_{ox}, t_{ox}) maps without the need of fabricating new samples, such variability sources and, in particular, the different parameters on which they depend (as, for example, Grain size, GB depth or width and/or charge density distribution), can be changed and analyzed independently. In this section, as another example of the proposed methodology capabilities, we have evaluated the impact of some morphological parameters associated to the high-k polycrystallization of the analyzed sample (as the GB depth and grain size) on the V_{th} variability (that is, on σV_{th}) of MOSFETs.

Fig. 7 shows the σV_{th} obtained for a set of one hundred 50×50 nm^2 MOSFET devices for different GB depths (a) and grain sizes (b) at both low (0.05 V) and high (1.0 V) drain biases. In all cases, smaller average value of V_{th} were obtained for higher V_D (not shown). However, since we are interested in the analysis of the variability, we have focused our analysis on σV_{th}. Note in Fig. 7a that σV_{th} increases as the GB depth rises, as expected: an increase of the GB depth leads to a higher inhomogeneity in t_{ox} and ρ_{ox}, which clearly affects the V_{th} variability. However, when the Grain size (Gsize) is considered as parameter, the V_{th} trend is different. Note in Fig. 7b that σV_{th} reaches the largest value when Gsize is smaller than the channel length of the MOSFET and depends on V_D. In any case, from that maximum value, when Gsize is reduced/increased, σV_{th} decreases. When the Gsize is much smaller than the MOSFET dimensions, every device contains a large amount of grains and, therefore, their impact on the V_{th} variability is averaged, leading to small values of σV_{th}. On the other hand, when Gsize is larger than the MOSFETs dimensions, many MOSFETs could contain

only one single crystal, increasing the homogeneity of the gate oxide characteristics and, therefore, reducing the V_{th} variability, as it is also observed in Fig. 7. For grain sizes comparable to the channel length the variability could be related to the inhomogeneity of the grain properties, since the thickness and charge in the grain are not homogeneous. Moreover, the V_{th} may be affected by the particular position of the grain in the channel. A combination of all these factors will determine the particular position of the variability maximum for a particular bias.

From a nanoscale point of view, the dependence of the MOSFET V_{th} variability on the GB depth and Gsize could be explained taking into account the nanoscale properties of the gate oxide (t_{ox} and ρ_{ox}) and how they affect the electrostatic potential in the channel (Fig. 5b). As an example, Fig. 8a-c shows different t_{ox} configurations and the corresponding t_{ox} and electrostatic potential profile measured along the highlighted lines.

Since the average value of the electrostatic potential depends on the position along the channel and, in our case, only relative variations are meaningful, in the three cases, the maximum value has been associated to 1000 mV and just relative variations with respect to this maximum have been considered. Note in Fig. 8a that a very deep GB (∼0.5 nm deep, dark area in the image) is analyzed. Fig. 8b shows two small grains with a shallow GB between them (∼0.3 nm deep). Finally, Fig. 8c corresponds to a big grain, which is quite homogeneous (t_{ox} variations are in the range of <0.1 nm). If we compare the t_{ox} variations in the three images with the electrostatic potential fluctuations along the profile, values of ∼15, 9 and 6 mV are measured in Fig. 8a, b and c respectively. Moreover, in Fig. 8a, where a deep GB is detected, a clear correlation between the electrostatic potential and t_{ox} is registered. Therefore, these results indicate that the morphological parameters associated to the high-k polycrystallization (as the GB depth and Gsize) affect the electrostatic potential in the channel: the higher the t_{ox} fluctuations, the higher the potential variations. Since the electrostatic potential along the channel determines the global electrical properties of the MOSFET, these results would explain why, the higher the fluctuation in t_{ox} and ρ_{ox}, the higher the variability observed in V_{th}.

V. CONCLUSION

To conclude, a simulation methodology has been proposed to evaluate the impact of nanoscale variability sources related to the polycrystallization of gate dielectrics on the variability of MOSFET devices. With this purpose, a Thickness And Charge MAp Generator (TACMAG) has been developed and used in combination with a semiconductor device simulator. CAFM experimental data, i.e., dielectric morphology and current, are the inputs to the TACMAG and the outputs are thickness and charge density maps of the dielectric. The TACMAG tool has been tested by comparing the V_{th} variability of MOSFETs whose gate oxide characteristics were determined either from the use of the TACMAG generator or measured with CAFM. The results show that the proposed methodology can be reliably used to evaluate the impact of the nanoscale t_{ox} and ρ_{ox} fluctuations of polycrystalline dielectrics on the device threshold voltage variability.

As a particular example, the developed simulation tools have been used to evaluate the impact of the t_{ox} and ρ_{ox} fluctuations of a HfO_2 polycrystalline layer on the V_{th} variability of MOSFETs. The results show that, at least for the case of the sample analyzed in this work, ρ_{ox} fluctuations have a higher impact on σV_{th} than the t_{ox} variations. Moreover, the impact of t_{ox} and ρ_{ox} fluctuations on V_{th} are correlated and can be described by a bivariate equation. When combined, both variability sources are somehow compensated, being the global σV_{th} smaller than that caused individually by ρ_{ox} fluctuations. Therefore, our results show that, for an accurate analysis of the impact of the high-k polycrystallization on the V_{th} variability and for a more realistic approach to real devices, the gate oxide morphology and ρ_{ox} cannot be considered independent variability sources.

Although the proposed methodology has been applied to a particular high-k dielectric, it can be extended to any other kind of polycrystalline structure. Moreover, since the input parameters are related with the morphological and electrical characteristics of the dielectric (Gsize, GB depth, charge density…), they can be easily changed, allowing also to evaluate their impact without the need of fabricating and measuring new samples and, therefore, reducing the cost and time of such analysis.

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ARTICLE SSE (DECEMBER-2021)

Exploiting the KPFM capabilities to analyze at the nanoscale the impact of electrical stresses on OTFTs properties

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Exploiting the KPFM capabilities to analyze at the nanoscale the impact of electrical stresses on OTFTs properties

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ABSTRACT

Two different Kelvin Probe Force Microscopy (KPFM) measurement configurations have been combined to evaluate at the nanoscale the effects of an electrical stress on Organic Thin Film Transistors (OTFTs) properties. As an example, Channel Hot Carrier (CHC) degradation has been induced to provoke some damage in the studied devices. The results show that the use of the two KPFM configurations, together with their nanoscale resolution, provides additional information about the damage in the different regions/materials of the devices, allowing to correlate device level characteristics with the nanoscale material properties.

1. Introduction

OTFTs are an interesting and promising alternative to Si-based technologies [1] in different applications such as wearable electronics, flexible devices and circuits or low-cost sensors. This diversity of applications is possible thanks to the good features they present, such as low fabrication complexity, mechanical flexibility, low-cost and/or higher compatibility with a wide range of substrates. Due to these good characteristics, many studies in the literature are focused on the analysis of the materials properties [2 –4] or device performance [5] and have proposed electrical models for describing their behavior [6], where the electrical properties of the organic material play a very important role. In spite of that, relatively few studies have been performed on the reliability of OTFTs [2], which is one of the key points in order to make this technology viable for the market. The electrical properties of the commonly used organic polymers are very sensitive to the environment conditions (temperature and humidity), what clearly affects the reliability of these devices. Moreover, the usual large operating conditions of the OTFTs can be also critical, due to the high voltages required (in the 10–30 V range). In this sense, the effect of the electrical stresses on the organic polymer and the device performance must be analyzed in detail. Moreover, the aging mechanisms activated in the OTFTs during the stresses should be studied and compared with those in conventional CMOS technologies to understand the role of the organic polymer in the device reliability. This task could be further complicated because of the large number of semiconductor polymers available in the market, so different strategies are necessary to assess the origin of the possible reliability issues.

In this regard, measurement techniques with nanoscale resolution, as Conductive Atomic Force Microscope (CAFM) and Kelvin Probe Force Microscope (KPFM) have been shown to be very powerful to get topographical and electrical information at the nanoscale of materials and devices. They can provide additional information about the causes of their degradation, beyond the electrical I-V curves obtained at device level. When the AFM tip is in contact with a given material, it plays the role of the top electrode, with a contact area that corresponds to the contact region between the tip and the sample. Since this area can be very small (~100 nm^2, on dielectrics [7]), the technique allows the nanoscale electrical characterization with a resolution of ~10 nm. CAFM and KPFM have been thoroughly used for the nanoscale electrical characterization of different materials, as graphene [8 –10], gate dielectrics [11 –17] or organic materials [18]. For example, in [19], KPFM has been used to study the effect of a Bias Temperature Instabilities (BTI) stress on OTFTs, obtaining information about the charge density at the polymer/dielectric interface after the electrical stress. In this work, we extend the use of this technique to preliminary analyze the impact of an electrical stress (in our case, a Channel Hot Carrier stress applied at device level) in both, the polymer layer (channel) and the gate stack of the OTFT (polymer and dielectric), at the nanoscale. With this purpose, two different KPFM measurement configurations have been used to obtain complementary information, which would allow to correlate device level characteristics with device level and nanoscale characteristics.

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2. Experimental details

The OTFTs were fabricated on a heavily doped silicon wafer (which plays the role of the gate electrode) with a 300 nm-thick thermally grown SiO_2 dielectric layer on top (Fig. 1a). The substrate was cleaned sequentially with acetone, isopropyl alcohol and deionized water in an ultrasonic bath, followed by blowing dry with nitrogen gas. On top of the gate dielectric, Au source-drain electrodes (thickness of 30 nm, Fig. 1a and 1b) were defined by photolithography to get a channel length (L) of 20 μm and channel width (W) of 15 mm. The organic channel was obtained by means a procedure based on solution processed organic semiconductors. A semiconductor solution of DPP-DTT in 1,2-dichlorobenzene (10 mg mL − 1) was then spin coated and annealed at 80 °C for 10 min under nitrogen environment, resulting in an 80 nm thick P-type organic semiconductor. A cross-section of the resulting device can be seen in Fig. 1a. It is worth noting that the surface of the device is totally covered by the DPP-DTT polymer, but the height profile mirrors the profile of the defined Au electrodes that are buried under the polymer layer. Fig. 1c correspond to a topographical image and profile along the line of an OTF channel between two Au electrodes.

Before and after the electrical stress, I-V curves at device level (i.e. I_G-V_G and, I_D-V_G) and the nanoscale properties of the channel and gate stack were measured with a Semiconductor Parameter Analyzer (SPA) and with a KPFM, respectively. The I-V curves were measured with the Keithley 4200 SPA, which was also used to apply the electrical stress. The stress was a −30 V constant voltage applied at the Gate and Drain Terminals during 6000 s. The nanoscale properties of the OTFT were investigated with a Nano-Observer KPFM from Concept Scientific Instruments, with which it is possible to measure, simultaneously to the topography, the Contact Potential Difference (CPD) between the tip and the sample. In our case, KPFM images have been obtained in air, using Si tips from AppNano. Since the CPD data correspond to the difference between the Work Functions (WF) of the tip and the sample, assuming a constant value of the tip WF during the experiment, the measured CPD variations are related to the WF fluctuations of the sample. Therefore, the CPD image provides information on the local value of the WF of the structure under analysis. However, since the tip WF is not known and absolute values of WF are also very sensitive to ambient conditions and can change between different measurements, only WF relative variations in a given image will be considered. The setup allows bimodal single pass Amplitude Modulation KPFM (AM-KPFM) measurements [20]. Fig. 2a and b show the two KPFM measurement configurations used in this work. In the first one (Fig. 2a), the KPFM measurements are performed between the Organic channel and the electrodes (called from now on Lateral KPFM configuration, L-KPFM), as the ground of the microscope is connected to one of the metal electrodes. In the second one (Fig. 2b), ground is connected to the gate electrode so, the measurements are performed between the organic channel and the substrate (called from now on Vertical KPFM, V-KPFM). Therefore, each configuration will provide details of the properties of different layers/stacks of the device.

3. Results

First, we have investigated the electrical properties of the OTFTs before the application of the electrical stress. A pristine OTFT, which will be considered as reference, has been analyzed at device level and at the nanoscale with the L-KPFM and V-KPFM configurations. Fig. 3 shows, for the L-KPFM configuration, the topography (a) and CPD (b) images of a region overlapping the channel and one of the electrodes, and Fig. 3c profiles along the lines drawn in the images. Fig. 3d-f correspond to the topography and CPD maps and the corresponding profiles (Fig. 3f), for the V-KPFM case.

In both cases, in the topography image (and its corresponding profile), a step is detected between the electrode (highest region) and channel (lowest region). This step is detected in the V-KPFM image as an artifact due to the crosstalk effect, in which a sudden change in the topography may induce an instantaneous change in the CPD [21]. This phenomenon can be seen at the center of the V-KPFM image (Fig. 3.f). However, leaving aside this artifact, the images and the profiles indicate no relevant differences between the CPDs of both regions (channel and electrode), as expected, since the tip is always contacting the as-deposited organic material and the devices have not been subjected to any electrical stress. The device electrical characteristics measured with the SPA is shown in Fig. 4b. There, the black curve corresponds to the I_D-V_G curve measured before the stress, which will be the reference to which the curves measured after the stress (red dots) will be compared.

After the pre-stress characterization, a CHC stress has been applied to the OTFT with the SPA. Fig. 4a shows a schematic of the device biasing. While the source was grounded, a voltage of −30 V was applied to the Drain and Back Gate of the device. Note that, with this configuration, positive carriers flow from Source to Drain, getting the maximum energy near the Drain and, therefore, damaging that region. On the other hand, since $V_D = V_G$ at the Drain area, vertical electric fields are negligible near the Drain and, therefore, NBTI damage (if any), should appear near the Source region only.

After the stress, the I_D-V_G characteristics has been measured (red curve in Fig. 4b). A large current reduction in the I_D-V_G characteristics is observed after the CHC stress, caused by a strong mobility reduction with negligible threshold voltage (V_{TH}) variation. Since BTI degradation is mostly related to V_{TH} variations and CHC degradation to mobility reductions, these results suggest that CHC degradation drives the device degradation while BTI seems to be negligible [22].

To investigate the effects of the stress on the properties of the different regions/materials of the device, L-KPFM and V-KPFM measurements were performed along the channel (close to Source and Drain electrodes). Fig. 5 shows L-KPFM (a-d) and V-KPFM (e-h) images of the channel/drain (C/D) and channel/source (C/S) overlapping regions. The top/down images correspond to topography/CPD maps. In the Source/Channel region (Fig. 5c/d/g/h), negligible differences are observed in the CPD image between the electrode and channel region, independently of the measurement mode, as was also observed in the fresh device (Fig. 3). Only some observable differences in the CPD values are measured in Fig. 5h, which can be related to measurement artifacts associated to the topographical changes observed in Fig. 5g. Although they could be related to some kind of contamination of the sample, their

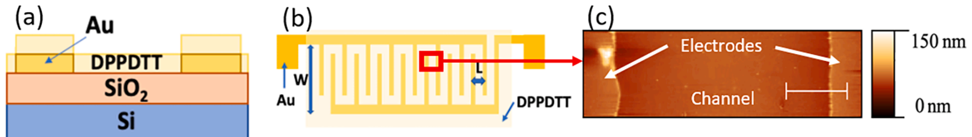

Fig. 1. (a) Cross-section and (b) top view of the OTFT under study. (c) shows the topographical image of the resulting DDP-DTT layer on two Au electrodes in the area inside the red box of (b). The scale bar is 5 μm. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

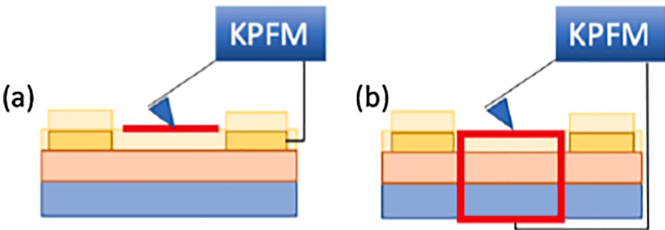

Fig. 2. KPFM configurations corresponding to the (a) lateral KPFM (L-KPFM) and (b) vertical KPFM (V-KPFM). The red lines indicate the area (for L-KPFM) or volume (for V-KPFM) analyzed. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

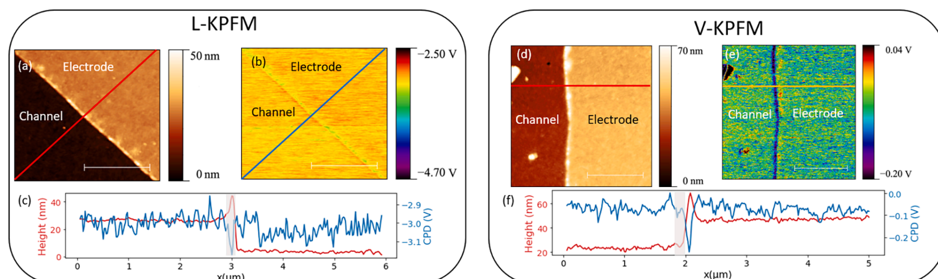

Fig. 3. (a and d) Topographical and (b and e) corresponding KPFM images of a region that overlaps the channel and electrode areas, for the L-KPFM (a and b) and V-KPFM (d and e) configuration. A profile along the lines on the images in the topography/CPD maps is shown in (c) and (f). The CPD is approx. constant over the two regions except at the step between the channel and electrode (grey area in the profiles), related to measurement artifacts. The scale bar is 2 μm.

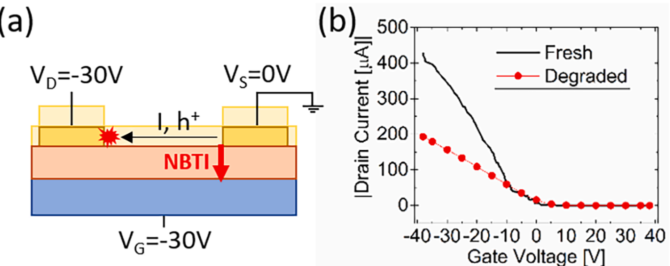

Fig. 4. (a) Scheme of the connections and biasing for the CHC stress (VD = -30 V, VG = -30 V and VS = 0 V for 6000 s). (b) I-V curves of the OTFT before (black) and after (red) the CHC stress. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

origin is not clear and further studies are required to investigate their origin. In any case, the results suggest that the stress has not induced visible NBTI changes neither in the channel nor in the gate stack close to the Source. Since NBTI effects (see Fig. 4a) (if any) in this CHC stress are expected to be located at that region, extending into the channel region, the results suggest that NBTI has little impact in this kind of devices, as also pointed out by the device level characterization (Fig. 4). In the Drain/Channel region, the CPD L-KPFM image (Fig. 5d) did not show remarkable changes in the CPD between the drain electrode and channel regions, being similar to that measured in pristine OTFTs (Fig. 3b). This suggests that there is a negligible damage on the surface of the OTFTs channel. However, the V-KPFM images (Fig. 5e/f) suggest the presence of an additional difference in the KPFM signal, not previously observed, close to the step. This difference, which is the main modification of the CPD observed, can be seen as a line that follows the Drain/Channel interface (enclosed in a red box in Fig. 5f), ~90 nm wide into the channel region and with an increase of the CPD of ~ 60 mV. This CPD signal is not related to any topographical feature near the step between the Drain/Channel interface. As it is observed in the channel region and with L-KPFM no damage is observed at the surface, this could be indicative of local damage at the dielectric and/or at the gate oxide/channel interface. These results, though preliminary, are compatible with the CHC degradation observed at device level (Fig. 4b), whose damage is expected to be concentrated close to the Drain.

4. Conclusions

In this work, two KPFM measurement configurations have been

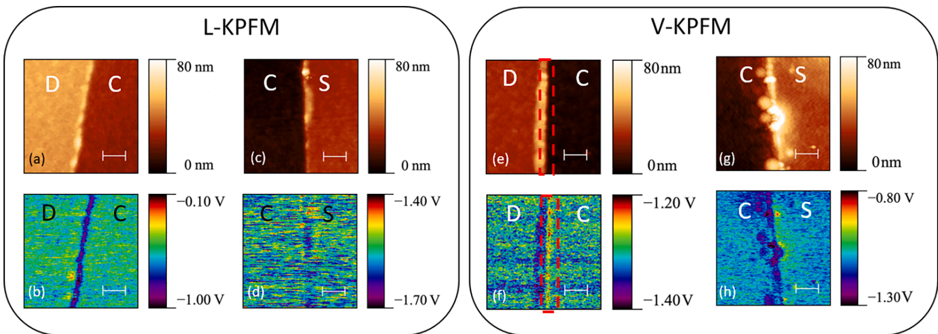

Fig. 5. L-KPFM (a/b/c/d) and V-KPFM (e/f/g/h) images of the channel/drain (C/D) and channel/source (C/S) overlapping regions. The scale bar is 0.5 μm. In general, the changes in CPD values match the changes in topography, except in the drain region when measured using the V-KPFM configuration (e/f). In this case, an additional CPD signal appears along the drain electrode, that is enclosed by the red box. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

combined with device level tests to evaluate the impact of an electrical stress (in this case, a CHC stress) on OTFTs electrical properties. The results show that the use of the L-KPFM and V-KPFM configuration can provide complementary information to device level tests on the nanoscale damage of the different materials/regions of the device. Because of the particular structure of these devices, destructive sample preparation is not required, so that measurement-stress-measurement sequences can alternate device level and nanoscale tests, allowing a time-dependent analysis of the device properties at both scales.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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