Universitat Autònoma de Barcelona

Design of a front-end ASIC for a fully integrated ultrasound PMUT array in CMOS

Iván Zamora

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Design of a front-end ASIC for a fully integrated ultrasound PMUT array in CMOS

A dissertation submitted in fulfillment of the requirements for the degree of Doctor in Electronic and Telecommunication Engineering

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2022

La Dra. Arantxa Uranga del Monte, Professor del Departament d'Enginyeria Electrònica de la Universitat Autònoma de Barcelona,

CERTIFICA:

que la memòria: "Design of a front-end ASIC for a fully integrated ultrasound PMUT array in CMOS" que presenta Iván Zamora Díaz-Comas per optar al grau de Doctor en Enginyeria Electrònica i de Telecomunicació, ha estat realizada sota la seva direcció.

Dra. Arantxa Uranga del Monte

Bellaterra, Septiembre del 2022

To my loving family...

Acknowledgements

Antes de comenzar me gustaría dedicarle unas palabras y agradecer a todas aquellas personas que de una forma u otra han contribuido a que este sueño se haga realidad.

En primer lugar, a mi tutora, la doctora Arantxa Uranga, por permitirme realizar mi tesis doctoral en el Departamento de Ingeniería Electrónica de la Universidad Autónoma de Barcelona. Muchas gracias por brindarme sus conocimientos, su apoyo y su ayuda en todo momento y guiarme en este fascinante mundo de la microelectrónica. También me gustaría agradecer a Núria por la oportunidad que me dio de formar parte del grupo de investigación ECAS, donde he aprendido y crecido muchísimo como profesional. A Francesc Torres y a todos los compañeros del departamento con los que he compartido. A todos muchas gracias por haberme hecho sentir como si estuviese en casa.

Quisiera especialmente agradecer a mis padres que ser su orgullo es la razón de mi esfuerzo y superación diaria. A mi esposa y compañera inseparable durante esta aventura, me faltarían palabras para agradecerle toda su dedicación, comprensión y amor brindado. A mi querido hermano, gracias por restarme preocupaciones y contribuir a que la separación familiar no haya afectado mi rendimiento. En sentido general, a toda mi familia y amigos por estar siempre pendiente y por sus consejos tan acertados.

Iván Zamora
Barcelona, Septiembre 2022

Summary

Nowadays, the advances in miniaturized MEMS ultrasonic transducers require major efforts in the design of the interface electronic circuits in order to take advantage of their lower power consumption, small size, and low fabrication cost. In this context, this Ph.D. thesis has focused on developing of an Analog Front-end Application-Specific Integrated Circuit (ASIC) for a fully integrated ultrasound phased array based on piezoelectric micromachined ultrasonic transducers (pMUT). The main goal is to achieve a compact system-on-chip ultrasound sensor with low power consumption and improved performance in terms of signal-to-noise ratio capable of being used in ultrasound imaging and ranging applications.

In particular, this thesis was aimed at the design and implementation of the electronics in charge of the generation of the PMUT driving signals, as well as the amplification of the PMUT signals generated, when the pMUT is working as a sensor. In this context, to optimize area, power consumption, and transmission efficiency, it has been proposed an HV Pulser based on level shifters and inverters, which is able to rise monophasic pulses from 3.3 V to 32 V. On the other hand, the reception analysis was performed to achieve a trade-off between noise performance, gain, and area needs. The proposed RX amplifiers include two LNA topologies (a voltage amplifier and a trans-impedance amplifier based on capacitive feedback), and a variable gain amplifier to implement the time-gain compensation function.

The pMUTs-on-CMOS ultrasound systems were validated, first, through a single pixel element capable to achieve higher signal-to-noise ratio levels in

comparison with the non-integrated system using the same fabrication process. Based on the excellent results achieved, a phased array (pMUTs-on-CMOS) was discussed and validated as a compact ultrasound system for imaging applications.

Finally, the last chapter was dedicated to presenting a new strategy to estimate very short relative distances with high accuracy based on the use of multi-frequency pulsed waves which opens the way to a future application of this system in CMOS electronic circuitry.

Resumen

Hoy en día, los avances en transductores ultrasónicos miniaturizados MEMS requieren de grandes esfuerzos en el diseño de los circuitos electrónicos de la interfaz para aprovechar su bajo consumo de energía, pequeño tamaño y bajo costo de fabricación. En este contexto, esta tesis doctoral se ha centrado en el desarrollo de un circuito integrado de aplicación específica (ASIC) de interfaz analógica para una matriz de transductores piezoeléctricos micromecanizados (pMUT). El objetivo principal es lograr un sistema completamente integrado y compacto, con bajo consumo de energía y con un rendimiento mejorado en términos de relación señal-ruido, capaz de ser utilizado en aplicaciones de imágenes de ultrasonido y aplicaciones de medida de distancias.

En particular, esta tesis tuvo como objetivo el diseño e implementación de la electrónica encargada de generar las señales eléctricas de excitación del transductor, así como la circuitería necesaria para la amplificación de la señal proveniente del transductor, tras ser excitado con una onda de ultrasonido. En este contexto, para optimizar el área, el consumo de energía y la eficiencia de transmisión, se ha propuesto un transmisor de alto voltaje basado en desplazadores de nivel e inversores, que es capaz de elevar pulsos monofásicos de 3.3 V a 32 V. Por otro lado, se realizó un análisis de recepción para lograr un compromiso entre el rendimiento del ruido, la ganancia y las necesidades del área. Los amplificadores RX propuestos incluyen dos topologías LNA (un amplificador de voltaje y un amplificador de transimpedancia basados en una retroalimentación capacitiva) y un amplificador de ganancia variable para implementar la función de compensación de ganancia de tiempo.

Los sistemas de ultrasonidos PMUTs−on−CMOS fueron validados, primero, a través de un elemento de un solo píxel capaz de lograr niveles más elevados de relación señal-ruido en comparación con el sistema no integrado que utiliza el mismo proceso de fabricación. Basados en los excelentes resultados obtenidos, se discutió y validó una matriz de pMUTs (integrados en CMOS) como un sistema de ultrasonido compacto para aplicaciones de imágenes.

Finalmente, el último capítulo se dedicó a presentar una nueva estrategia para estimar, mediante el uso de transductores de ultrasonido, distancias relativas muy cortas con alta precisión basada en el uso de ondas pulsadas multifrecuencia, lo cual abre el camino a una futura aplicación de este sistema en circuitos electrónicos CMOS.

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CHAPTER 1

INTRODUCTION

1.1 Background and Motivation

Ultrasound is defined as acoustic waves in solid, liquid, and gases, with frequencies higher than the upper audible limit of human hearing, around 20 kHz [1]. Precursors of ultrasound date back to ends of 19th century and at the beginning of 20th. The discovery of piezoelectricity by the Curie brothers in 1880, the invention of the triode amplifier tube by Lee de Forest in 1907, and the invention of the quartz ultrasonic transducer by P. Langevin, used for submarine detection during the World War I, were some of the milestones that made ultrasound a subject of interest in the scientific community [2], [3]. From that moment on, an intense period of experimentation and hopefulness began, turning ultrasound into a powerful tool with well-established fundamentals of the physical acoustics.

Ultrasound is considered as non-invasive, safe and does not have any cumulative biological side effects [3], hence it has become in a "gold standard" for diagnostic imaging and medical treatment. Besides these benefits, ultrasound has other advantages that make it in an attractive sensing method for ranging application. First, its propagation speed is lower than electromagnetic radiation, by a factor about 10^6 [4], which avoids the use of high-speed electronic. Second, the sound spectrum is unregulated outside the human audio band [5],

which permits a high degree of freedom to use.

From the beginning of the 21st century to date, new technological scenarios have been developed addressed to obtain a smarter world. Examples of these are: smart mobility, smartphones, Internet of Things (IoT), wearable health-care devices, remote health-care monitoring, etc. Within each of these scenarios is mandatory to develop new miniaturized sensory systems with high performance, which translates in high sensitivities, low cost and low power consumption. In this sense, the majority of research efforts are focused on: optimization the transducer element, reduction noise and power consumption of the electronics used for control and processing, trying to ease the integration of transducer into electronics by offering ultra-compact form factor, and to develop advanced signal processing algorithms. With the development of the MicroElectroMechanical Systems (MEMS) technology, the miniaturization and integration have been much simpler. MEMS devices are micro-scale structures such as cantilevers, membranes, and free-standing bridges, fabricated using micro-machined techniques in combination with microelectronic fabrication methodology and technology [6]. MEMS technology has allowed researchers to design robust transducers with small form factor and manufacturing scalability, making them a good fit for cost-effective smart devices.

Ultrasound sensing technology has been greatly benefited by the MEMS approach. Researchers have been able to micro-machine small membranes (in a range of 10 μm to 200 μm in size) onto a conductive silicon substrate, which are capable to emit and sense ultrasound signal in an efficient way [7]. These devices are recognized in the literature as MEMS ultrasound transducers (MUT), and in dependence of its transduction mechanism are classified in capacitive MUT (cMUT) and piezoelectric MUT (pMUT). MUT devices, in comparison with the conventional bulk piezoelectric transducers, which are the most used technology due to their mature, are easier to fabricate [8]. On the one hand, they have better impedance matching with a given propagation medium, hence, MUT devices do not require an additional matching layer. On the other hand, when high-frequency arrays need to be fabricated, the distance between bulk piezoelectric elements must be very tight in order to reduce unwanted emissions, which complexifies the mechanical dicing and therefore the fabrication process [9].

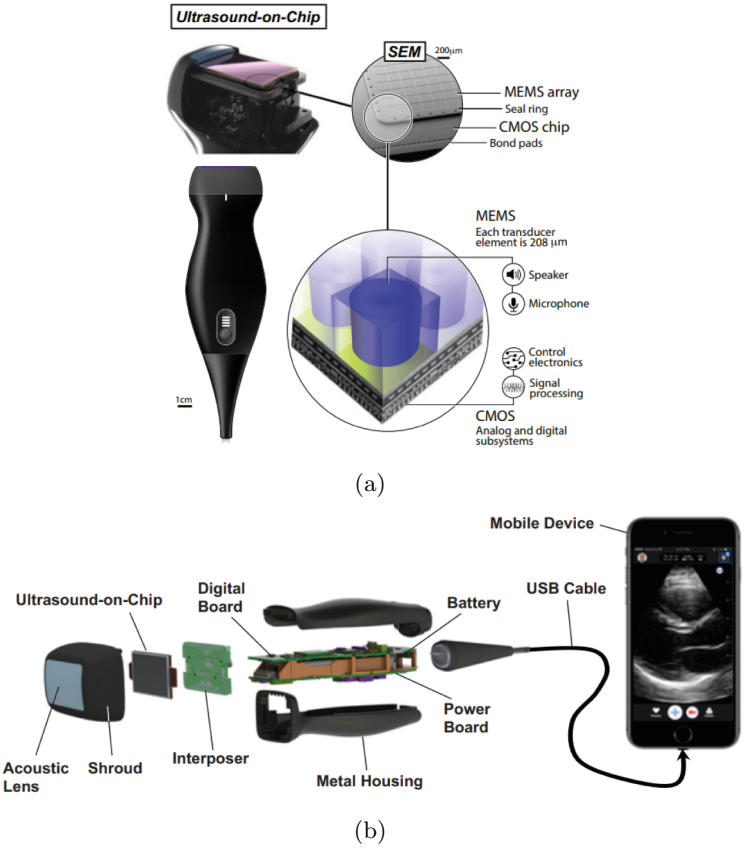


Figure 1.1: (a) Ultrasound-on-chip (UoC) probe, highlighting the cMUT and CMOS integrated chip (b), UoC probe breakdown [10].

Currently, a plurality of applications, within the scenarios mentioned above, based on MUT technologies can be found. Rothberg and et. al [10], have implemented a complete Ultrasound-on-chip (UoC) device based on cMUT transducers for medical imaging. This device, shown in Fig. 1.1a, is based on 140x64 cMUT array integrated into complementary metal–oxide–semiconductor (CMOS) circuitry for control and processing, to enable an inexpensive whole-body imaging probe. The CMOS circuitry contains thousands of transmitters, amplifiers, and analog-to-digital converters, and it is able to implement more than 1 trillion of operations per second with only 3 W of power consumption. Fig 1.1b shows a breakdown of the UoC probe, which is connected to a mobile device through USB cable to display the ultrasound image. The cMUTs and CMOS integrated chips are protected by the acoustic lens, and is wire-bonded to a printed-circuit-board (PCB)

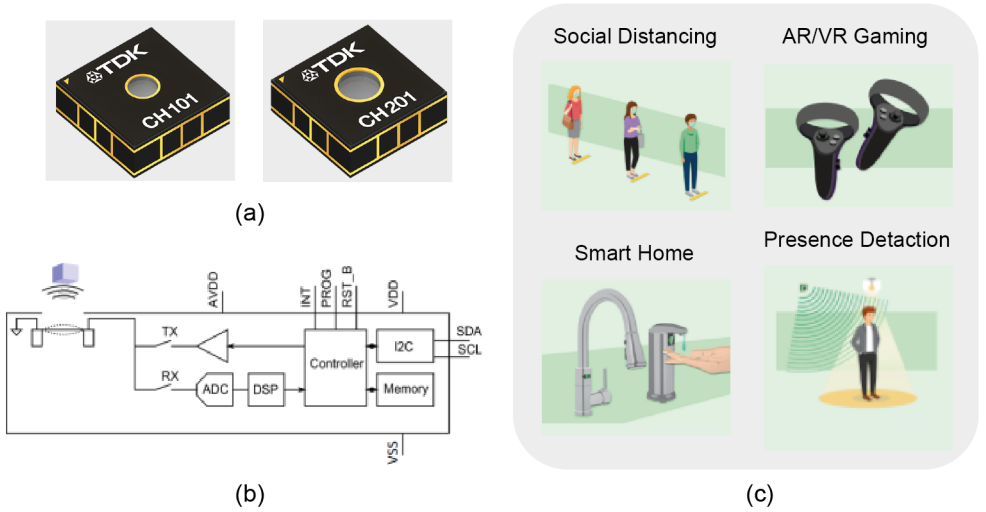


Figure 1.2: (a) Commercial ultrasonic ToF range sensors, (b) general block diagram, and (c) CH101 and CH201 applications [11], [12].

interposer, which is plugged into a board that contains a field programmable gate array (FPGA) and a universal serial bus (USB) interface to the mobile device [10]. This handheld scanner is part of a new generation of the ultrasound scanners, where the expertise is not mandatory, but it can be used by clinicians in general or even by general public.

TDK-Chirp Microsystems company has developed two ultrasonic Time-of-Flight (ToF) range sensors, see Fig 1.2a. Both of them, are based on pMUT transducers integrated with ultra-low power System-on-Chip (SoC), achieving a final footprint of 3.5x3.5 mm. CH101 ultrasonic ToF range sensor can measure an accurate range from 4 cm to 1.2 m, while CH201 can operate from 20 cm to 5 m. As shown in Fig 1.2b, the SoC includes the transmission and reception circuitry, an advanced ultrasonic Digital Signal Processing (DSP) algorithms, and a microcontroller, that provides the digital interface for communication with off-chip devices [11], [12]. During the coronavirus (Covid-19) pandemic, TDK-Chirp Microsystems developed a complete sensor API [1] based on ultrasonic technology to measure when users come into contact and notify those who may have been exposed to SARS-COV-2 when an infection does occur [13]. The proposed tracking solution uses CH101 ultrasonic transceiver (actuator and sensor device) to measure the distance between wearable tags of

[1] Application programming interface

each user, at ranges up to 8 feet with an accuracy of 1 cm [13]. In addition to social distancing application, both CH101 and CH201 ultrasonic sensors can be used for smart home and Augmented reality/virtual reality (AR/VR) systems, enabling presence detection in any lighting condition [11], [12].

After Apple announced the debut of its new iPhone 5S with fingerprint sensor in 2013, the biometric authentication systems began to increase their popularity in front of other authentication systems such as passwords. From there, mobile manufactures began to look for highly durable and button-free solutions with fingerprint sensors. Ultrasound technology takes advantages over other mechanisms for fingerprint recognition. Capacitive sensors have been a standard for identity authentication because they are fabricated using a conventional CMOS integrated circuit manufacturing process [14]. However, capacitive fingerprint sensors are extremely sensitive when the user's skin contains common contaminants such as oils, lotion, or perspiration [15]. On the other hand, optical fingerprint sensors are difficult to miniaturize and consume a lot of power, doing them inadequate for portable devices [16]. In contrast, ultrasound technology works well on contaminated fingers because finger's valleys and ridges are highly distinguished due to the acoustic impedance of the ridge's human tissue is much higher than the acoustic impedance of the air-filled valley (about 3500 x factor) [17]. In addition, ultrasonic fingerprint sensors are capable not only to capture images from the epidermis, but also they have the ability to provide images of the sub-surface dermis layer, which makes this technology very secure and robust for authentication solutions [16].

In this sense, InvenSense in collaboration with GLOBALFOUNDRIES have developed an ultrasonic fingerprint imaging technology for ultrasound fingerprint sensor solution [18]. This technology, that was patented in 2015 [19], is based on direct integration of aluminum nitride (AlN) piezoelectric MUT (pMUT) transducers with the CMOS integrated circuit (IC), see cross-section in Fig 1.3a. Also, a mass manufacture of AlN pMUT arrays where each transducer element is individually controllable through direct wafer-level interconnect to the CMOS ASIC was enabled. As results, two modules have been developed, enabling a breakthrough biometric authentication solution for mobile and IoT products [20]. TCFS-2000 and TCFS-3000 modules in Fig. 1.3b can sense under thick plastic or aluminum, converting in potential candidates for access controls in residential, hospitality, enterprise, and vehicle entry, as

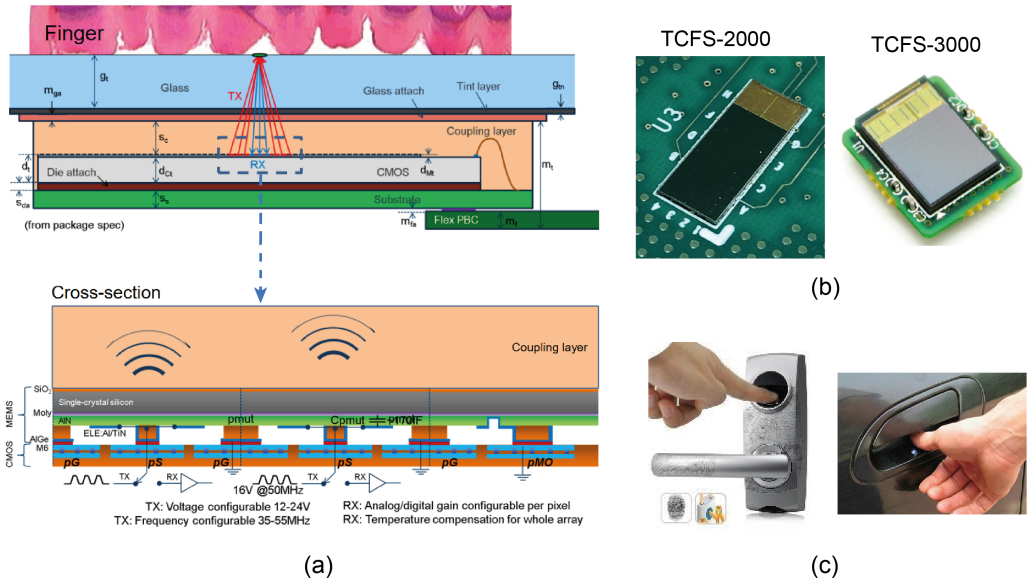


Figure 1.3: InvenSense UltraPrint™ Ultrasound Fingerprint Touch Sensor Solution. (a) Schematic cross-section, (b) TCFS-2000 and TCFS-3000 modules mounted into mockup housings, and (c) Application examples.

shown in Fig. 1.3c [20].

Beyond the great advances that have been obtained in the development of new ultrasound transducers (MUTs), the integrated circuits (ICs) and their integration with MUTs, play an important role to obtain a miniaturized and cost-effective ultrasound system. An electronic architecture for control and processing the ultrasound signal, based in IC technology, offers scalability and low power consumption, two ideal targets to implement an efficient ultrasound system with small form-factor. Considering this, IC manufacturers are trying to ease the integration of MUT transducers with IC electronics into the system by offering ultra-compact form-factors and supporting a range of operating voltages. In this sense, Silterra company, which is an IC manufacturer, has developed and patented a technology, by adding aluminum nitride-based piezoelectric capacity to its CMOS platform, enabling for the first time a monolithic pMUT-on-CMOS platform [21]. The Electronic Circuit and Systems (ECAS) group of the "Universitat Autónoma de Barcelona", research group to which this thesis project belongs, is in deep collaboration with Silterra for the design of ultrasound systems in order to verify its technology. At the beginning of this research, only pMUT devices fabricated with Silterra's platform had been

characterized from electrical to acoustic performance [22]. However, no information on application and results of acoustic performance of the ultrasound system based on monolithic integration of pMUTs and CMOS circuits had been reported. Considering this, the main objective of this thesis work is to design an analog front-end ASIC for pMUT transducers, using the MEMS-on-CMOS platform from Silterra, to obtain a fully integrated pMUT-on-CMOS system for imaging and ranging applications. Through the optimization in both pMUTs and CMOS circuits, a promise solution has been obtained. This has been demonstrated by the fabrication of several chips, which will be explained in the following chapters.

1.1.1 Market perspectives for MUTs

Thanks to new emerging applications, the ultrasound sensing market has shown an impressive growth. In this context, Yole Développement has estimated the billing forecast related to ultrasound sensing modules from 2019 to 2025 [23]. Fig 1.4 shows as a $4.6B market in 2019, it poised to reach around $6.2B in 2025, which means growth factor of 1.35, taking into account the terrible impact of the COVID-19 pandemic. This growth has been possible in large part to the development of MUTs, which have done possible to translate the ultrasound technology to new emerging applications where miniaturization and components cost are keys. Fig 1.5 shows the use of main ultrasound technologies in a wide range of applications in 2019 and 2025. From a tech-

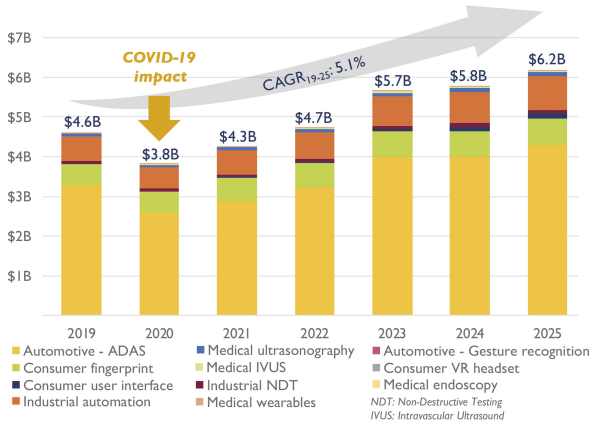


Figure 1.4: Market perspectives forecast in Ultrasound sensing modules.

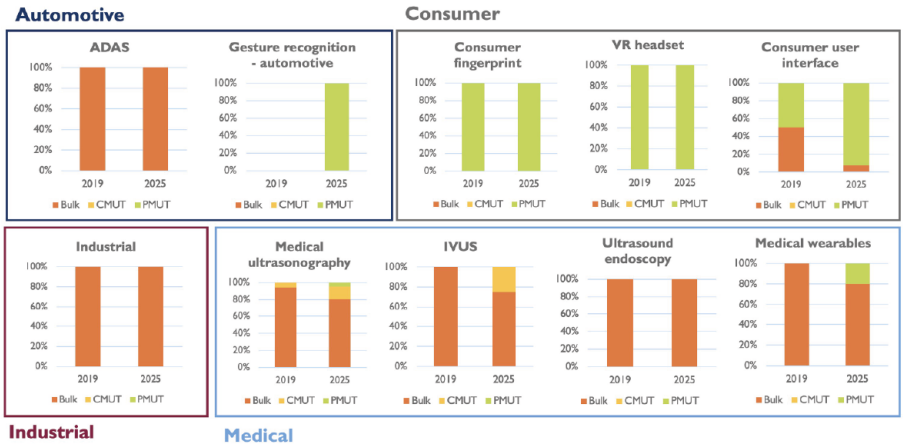


Figure 1.5: Ultrasound modules market forecast by segment and by technology.

nology perspective, we see that the conventional ultrasound transducers (bulk piezoelectric transducers) are still the most used in the ultrasound modules market. Besides, we can see how the popularity of pMUT devices is expected to increased considerable, coming to replace its counterpart cMUTs, and get become the main technology for consumer applications.

1.2 Basics of an ultrasound system

Most ultrasound measurements are based on the pulse-echo method, where a short ultrasound pulse is generated and propagated towards a specific direction of a given medium, and is partly reflected wherever there is an abrupt change in

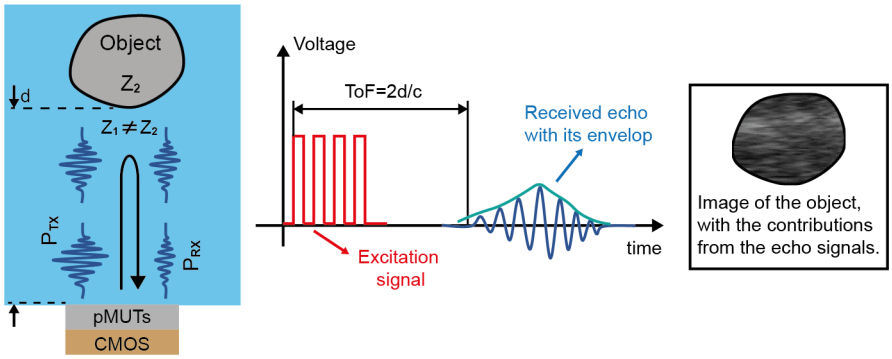


Figure 1.6: Transmission and reflection of an ultrasound pulse, time diagram of the excitation and received signals, and example of an ultrasound image of a detected object.

the acoustic properties of the medium, resulting in returning ultrasound signals towards transducer, which are defined as echoes, see Fig 1.6 left. The degree to which a pulse is reflected at an interface is determined by the change in acoustic impedance (Z_1 and Z_2 in Fig 1.6). Pulse-echo method can be used in both, to measure distance and to construct an image of a given object. When ultrasound wave travels with a known velocity c and the time from the emission to detection of the reflected pulse is estimated (Time of Flight), the distance d between the transducer and the object can be measured using the expression in Fig 1.6 center. Also, as shown in Fig 1.6 right, an ultrasound image of the detected object can be formed by mapping the echo strength versus ToF (proportional to the distance) and the beam direction. This image modality is referred to as Brightness-mode imaging (B-mode) [24].

A block diagram of a simplified ultrasound pulse-echo measurement system is shown in Fig 1.7. It consists of one or more transducers arranged in array configuration, the transmitter (TX) circuitry, the receiver (RX) circuitry, a control and signal processing module, and a display. The TX circuitry can generate a high voltage signal to excite the transducer. The driving voltage must be to a level where the transducer can generate an adequate amount of acoustic energy in a desired direction. In most cases, rectangular pulses are preferred in front of sine signals as driving voltage, in order to simplify the TX circuit design. TX circuits that can generate high voltage (HV) rectangular

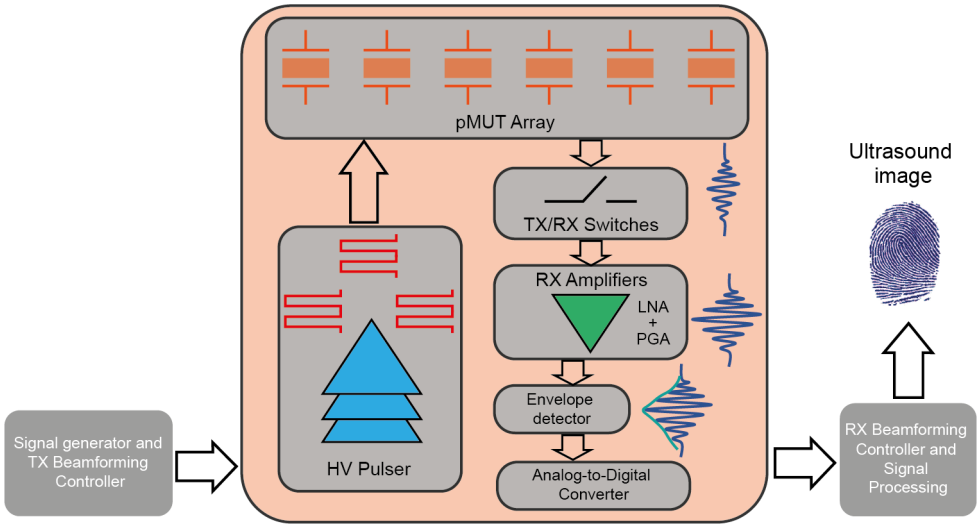


Figure 1.7: Block diagram of an ultrasound imaging system.

pulses, are defined as HV Pulsers.

Transducer elements translate an electrical signal into mechanical vibration and vice versa. Currently, the most used ultrasound transducers are the conventional bulk piezoelectric devices, and the MEMS ultrasound transducers (cMUT and pMUT). In order to achieve a high pressure level and high spatial resolution, a transducer array configuration is adopted. When array configurations are used, there are several transmission/reception channels, which allows to focus and steer the ultrasound beam (to be discussed later). To implement this, is necessary to provide a delay control circuit, TX/RX beamforming controller in Fig 1.7, which can be integrated in the same chip, or to be an external module, as in the present thesis.

On the reception side, a dedicated Front-end circuit is directly connected to the transducer. It contains an isolation switches (TX/RX switches in Fig 1.7) to prevent any transmission feed-through, and high gain and low-noise amplifier (LNA). Following the LNA there is a Variable/Programmable Gain Amplifier (V/PGA), which main purpose is to correct attenuation that suffers the signal when it travels through the medium. The gain of the PGA can be controlled by time [25], which would be a Time Gain Compensation (TGC) amplifier, or adapted depending on the input signal strength in real time [26]. Analogous to transmission, if transducer arrays are used, some time varying delay elements, and summing circuits will be part of reception chain. They can be performed in both, analog domain [27]–[29] or the digital one [30], [31]. After amplification the signals are envelope detected and digitized, and are fed into the signal processing module, which processes and displays the required results.

1.2.1 Ultrasound transducers

Bulk piezoelectric transducers are the conventional type of ultrasound transducers, that by the maturity reached throughout history, they have been converted in the most used transducer for ultrasound imaging [32]–[34]. These devices are composed of a piezoelectric layer sandwiched between top and bottom electrodes, see Fig 1.8a. The piezoelectric layer can be formed by piezoceramic materials such as lead-zirconate-titanate (PZT), or combining piezoelectric materials with polymer to fabricate piezocomposite ultrasonic transducers [8]. Its

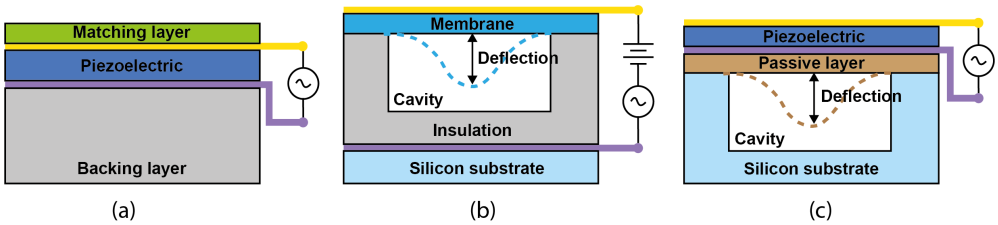


Figure 1.8: Schematic diagram of ultrasound transducers. (a) bulk piezoelectric, (b) capacitive MUT (cMUT), and (c) piezoelectric MUT (pMUT).

transduction mechanism is through piezoelectric effect, this is, when a controlled alternate current (AC) voltage is applied by means electrodes causes that the piezoelectric film get deformed (strain), which generates structural vibration at frequency of the applied voltage and as consequence the transmission of acoustic waves (converse piezoelectric effect). Conversely, when an acoustic wave hits the device surface causes a mechanical stress on the piezoelectric material, yielding an electrical charge or a voltage change across the electrodes proportional to the stress (direct piezoelectric effect) [35]. Usually, bulk piezoelectric transducers include a backing layer and a matching layer, as shown in Fig 1.8a. The propose of the backing layer is to shorten the emitted pulses through the damping of the ultrasound transducer and reduce ultrasound generation artifacts from the back side [8]. The matching layer is used to compensate the acoustic mismatch between transducer and the propagation medium [36]. However, although bulk piezoelectric transducers are a well-established technology, when array configuration is desired, they are converted in a complex, expensive, and high-time demanding fabrication process. This is mainly due to when high-frequency arrays are required, the gap between elements must be very small in order to optimize performances, which causes that the dice-and-fill method used for fabrication of bulk piezoelectric matrix will be complex and tedious [8].

To overcome this drawback, ultrasound transducers fabricated using silicon micromachining techniques have been extensively explored [37], [38]. These devices, knew in the literature as Micro-machined Ultrasound Transducers (MUTs), have created new opportunities to ultrasound technology where the miniaturization and high integration are essentials. MUTs are based on a thin flexible membrane fabricated that have at least on of their dimension in the range from hundreds of nanometers to hundreds of micrometers and are fab-

ricated using the same manufacturing technology of integrated circuits (ICs). As mentioned above, according to the transduction mechanisms, MUTs are classified as capacitive (cMUTs) or piezoelectric (pMUTs).

As seen in Fig. 1.8b, in the case of cMUTs, the membrane is suspended on top of a vacuum gap and is generally made of an insulating material (Si_3N_4) coated with a thin metal layer as top electrode [39]. The silicon substrate forms the bottom electrode, and an insulation layer is stacked on the substrate underneath in order to prevent contact between the electrodes [9]. cMUTs can be used in both: as actuator (transmission mode), and as sensor (reception mode). On the transmission mode, oscillation of the membrane is electrostatically induced applying both a direct current (DC) voltage and an alternating current (AC) voltage across the two electrodes. Due to the electrostatic force is always attractive, the DC voltage (usually much larger than AC voltage amplitude) is required to prevent the membrane from vibrating at twice the excitation frequency [39]. On the receive mode, the oscillation of the membrane is caused by the incident acoustic wave. The height of the gap is modulated, which produces changes in the capacitance of the device. When a DC voltage is applied between the electrodes, the capacitance variations result in a current flow to the readout circuit [9]. Generally, the cMUTs require of a narrow height gap to achieve large receiving sensitivity. This requirement causes two drawbacks: the first one is that during its fabrication, a control process of the nm-scale gap height is required, which increases the complexity of manufacturing, and the second one causes that the membrane displacement during transmission is limited [40].

Unlike cMUTs, pMUTs have no vacuum gap between the top and bottom electrodes for oscillation. As shown in Fig. 1.8c, a thin piezoelectric film is sandwiched between the top and bottom electrodes, and is deposited on top of the passive layer (usually SiO_2) to form the membrane, which is suspended over a cavity. On the same form of cMUTs, pMUTs have two operation mode: as actuator (described by converse piezoelectric effect) and sensor (described by direct piezoelectric effect).

The pMUT design has several attractive characteristics that makes it desired for some applications. Unlike cMUTs, pMUTs not require any DC bias to operate [41], the deflection of the membrane is not limited by the separation of

electrodes [38], and they have lower capacitive impedance than cMUTs, which facilities impedance macthing to electronic circuits [42]. Taking into account this, pMUTs are strong candidates for low-power ultrasound application. In contrast to these advantages, pMUTs have drawbacks that limits their applicability. Compared to cMUTs, pMUTs present lower electromechanical coupling coefficient (k^2), defined as the input mechanical energy to the storage electrical energy and vice versa, which is translated to lower sensing and actuation sensitivities. To date, the reported k^2 values for pMUTs are around 1%-6% [8], [43]–[45], whereas the coupling coefficients based on cMUTs are around of 70% [8]. On the other hand, pMUTs have a smaller bandwidth and larger quality factor (Q) than cMUTs [46], which represents a lower axial resolution, hence cMUTs are preferred in medical and high-resolution imaging applications [47].

1.2.2 Equivalent Circuit Model for pMUTs

When the pMUT transducer operates in linear regimen, the vibration of the membrane can be modeled as a second order mechanical system, which can be represented by an equivalent lumped mass, a spring and a damper. These mechanical properties can be mapped to equivalent electrical variables to model the dynamic behavior of the pMUT in terms of circuit parameters,

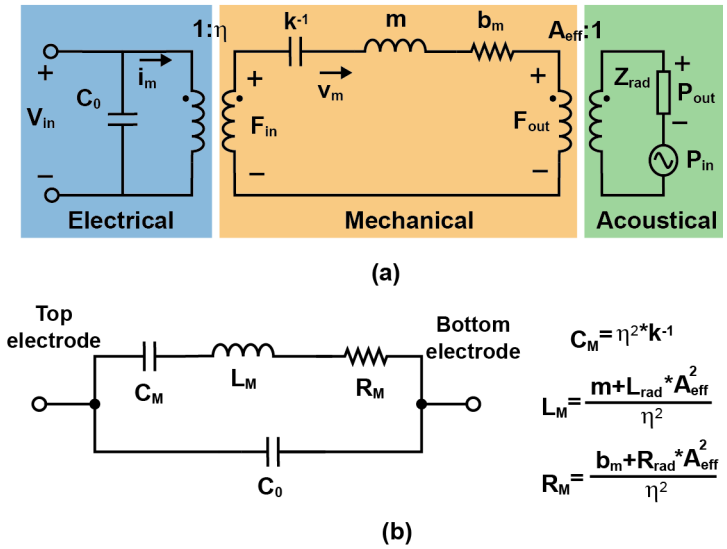


Figure 1.9: Equivalent circuit model for pMUTs. (a) Electrical-mechanical-acoustical model, (b) Equivalent electrical model (Butterworth-Van Dyke model).

for which there are well-established design techniques and powerful analysis tools. Figure 1.9a shows an accurate equivalent model of the pMUT, which includes the three operation domains coupled through ideal transformers [48]. For analogies, can be shown that the force (F) is represented by voltage, and the membrane velocity (v_m) is represented by currents.

The left portion of the circuit in Fig 1.9a represents the electrical domain, which is composed by static electrical capacitance C_0 (i.e. parallel plate capacitance formed by the piezoelectric material sandwiched between two metal electrodes). The first transformer, with the ratio η, models the piezoelectric effect that converts the applied voltage V_{in} to mechanical force F and vice versa. The central portion of the circuit in Fig 1.9a models the mechanical properties of the pMUT membrane, where the capacitance k^{-1} models the membrane stiffness (k), the inductance m models the mass of the membrane, and the resistance b_m models the substrate damping [49]. The mechanical domain is coupled to acoustic domain via the effective area of the pMUT. The right portion of the circuit in Fig 1.9a models the propagation media, which is represented by the radiation impedance Z_{rad} and an AC voltage source, which models the acoustic pressure that impinges over pMUT surface. The radiation impedance Z_{rad} is a complex function that depends of the medium density (ρ) and the sound velocity (c_0) [50]. The real part of the Z_{rad} models real acoustic power delivered to the media, and adds damping to the overall system, whereas the imaginary part of Z_{rad} models the mass of the media.

The electrical-mechanical-acoustical model represented in Fig 1.9a allows a direct evaluation of the frequency response of the pMUT, determine output acoustic powers, time-domain responses, and transmit and receive sensitivities. By applying the appropriates laws of the circuit theory, the circuit represented in Fig 1.9a can be simplified to the represented in Fig 1.9b. This simplified electrical model is recognized in the literature as Butterworth-Van-Dyke model, and its effectiveness has been demonstrated for a variety of transducers, such as: pMUT [26], cMUT [51], and bulk piezoelectric [52]. It can be easily obtained from the transducer impedance measurements with a Vector Network Analyzer (VNA), and can be used for modeling the load that the pMUT represents at the output of a transmit circuit, and in modeling of the pMUT as a small-signal source with an output impedance at the input of an LNA.

1.2.3 Transducer spatial resolution

The final quality of an ultrasound image is influenced by many parameters from the transducer to the display screen. One of the most influential parameters is the spatial resolution. It is defined as the ability of the ultrasound system to distinguish between two objects located at different position in space [53]. It can be separated in two: axial resolution and lateral resolution.

Axial resolution is the smallest separation that can be differentiated between two targets located along the axis of the ultrasound beam [54]. Mathematically, is defined as half the ultrasound pulse length [54]. To illustrate this, Fig 1.10 shows the transmitted pulses and the received echos from two objects, placed along the axis direction for three different separations. To clarify it, the pulse envelopes are used. In Fig 1.10a the objects are separated by a distance greater than the pulse length (L), with which two separated echos are received, and as a consequence, the objects can be displayed as two different images. When the objects are separated by L/2, as in Fig 1.10b, the round trip from object 1 to 2 is equal to L, which causes that the beginning of the second echo reaches the ending of the first one, making still possible their identifications. If the objects are brought closer to a distance less than L/2, an overlapping of the echoes will occur, making it impossible its differentiation, see Fig 1.10c.

From Fig 1.10, we can state that the axial resolution has a strong dependence with the pulse length, which in turn is directly proportional to the transmission frequency, number of excitation cycles, and the quality factor of the transducer. From this, we can say that high-frequency and low quality factor transducers are desired to obtain high axial resolutions [54].

Lateral resolution can be defined as the minimum distance that can be distinguished between two objects situated side by side perpendicular to the direction of the ultrasound beam [53]. It depends of the width of the ultrasound beam. A narrow ultrasound beam width provides a high lateral resolution [54]. To illustrate this, Fig 1.11a shows a shape of a typical ultrasound beam emitted by a transducer, and three objects placed perpendicular to the beam direction. Since the objects A and B are separated by a distance shorter than the beam width, they will appear as a single object in the display. In contrast, the object C if can be distinguished from A and B being separated at a distance larger

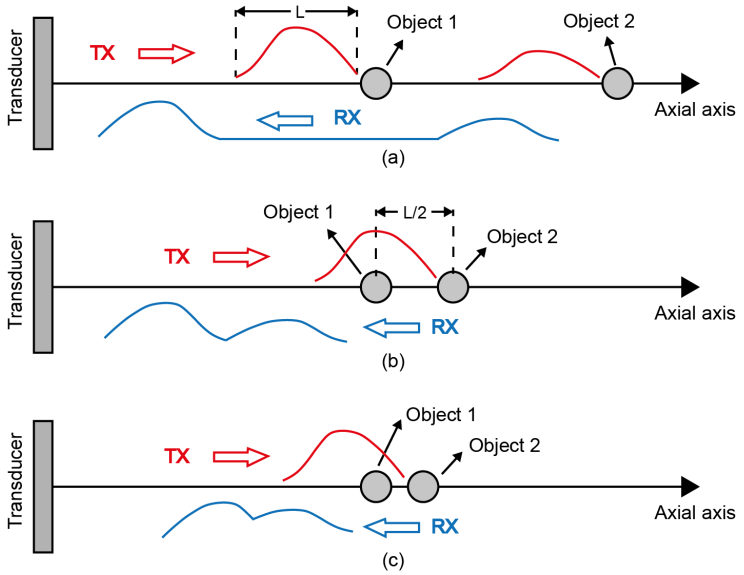


Figure 1.10: Diagram of pulse transmission and received echo from two locations in axial direction, separated by a distance: (a) larger than the pulse length (L), (b) equal to L/2, and (c) shorter than L/2.

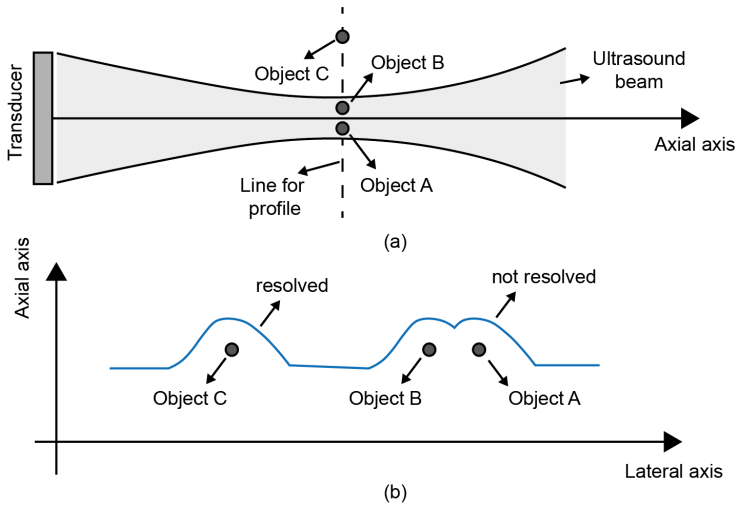


Figure 1.11: Illustration of lateral resolution: (a) Ultrasound beam with objects to detect, and (b) the brightness profile from laterally spaced objects.

than the beam width. As a result, Fig 1.11b represents an example of brightness profiles along a horizontal line in the image that passes through these three objects, showing how the object C is represented as a separated point meanwhile the objects A and B can not be seen as separate.

As be shown in Fig 1.11, the beam width changes with the distance between transducer and the reflector objects. Near to the transducer, the beam width is approximately equal to the transducer's aperture. As we move away from the transducer surface in axial direction, the beam converges to its narrowest width, which is obtained at near-field distance, resulting in the best lateral resolution. At this distance, the full width of the beam at half maximum (BW_{FWHM}) can be estimated by Eq. 1.1a [55], where A is the transducer's aperture, λ is the wavelength, defined as c/f, being c the sound velocity and f the transmit frequency, and F is the focal depth (near-field distance when no focusing is applied). At distances greater than the near-field length, the ultrasound beam gradually diverges, degrading the lateral resolution [54]. The near-field distance can be approximately obtained through Eq. 1.1b [56].

$$BW_{FWHM} \approx \frac{\lambda \cdot F}{A} \tag{1.1a}$$

$$NF = \frac{A^2}{4\lambda} \tag{1.1b}$$

Considering this, the lateral resolution is improved, when high frequency transducers with large aperture are designed.

1.2.4 Transducer arrays and beamforming

From the analysis done above, high-frequency and large transducers are required to maximize both axial and lateral resolutions. From a MUTs design perspective, large membranes with high resonance frequency are very difficult to obtain, due to they have an inversely proportional dependence [14] [57]. Considering this, small MUT elements are arranged in one or two dimensions to form an array transducer. Implementations of array configurations not only enable high-frequency and large transducers, but also they provide a greater flexibility than solid apertures, since each element in the array can be electronically controlled, allowing to focus and steer the ultrasound beam at different directions without requiring a mechanical movement. The most used array configurations for MUT are linear array (1-Dimension), and 2-Dimensions arrays. Linear array consists of a number of MUT elements aligned in a single row, see Fig 1.12a. Usually, each element of the array has the same dimension

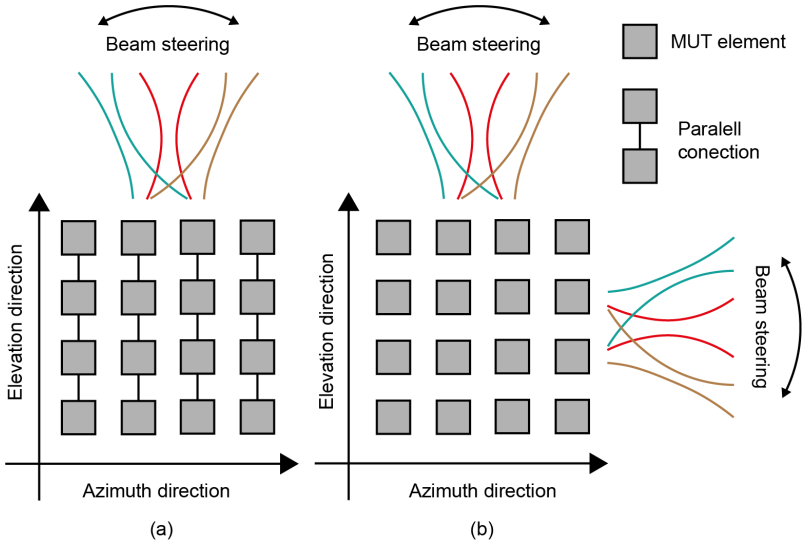


Figure 1.12: MUT array configurations. (a) Linear array, and (b) 2D array.

in both azimuth and elevation directions, and is formed by the parallel connection of multiple MUT single elements [38]. Since there are multiple elements in only one dimension of the linear array, the ultrasound beam can be only steer in azimuth direction. In spite of this restriction, MUT linear arrays find applications as: a wearable ultrasonic neurostimulator [58], acoustic angiography [59], and other [60]–[63].

Unlike linear array, two-dimension MUT arrays contain multiple elements in both azimuth and elevation directions, see Fig 1.12b. Therefore, 2D arrays are formed by a large number of MUT elements in both dimension, which can be individually controlled by electronic circuits to steer and focus the ultrasound beam of a dynamic manner in two orthogonal directions [64]. Because of this characteristic, 2-D MUT arrays bring benefits in electronic control flexibility, better reliability and quality of measurements. In contrast of these advantages, since there are a large number of elements, their electrical interconnections are more complex than 1-D MUT arrays [38]. Ultrasound-on-chip for medical imaging [10], three-dimension fingerprint sensor [16], ultrasonic rangefinder on a chip [5], and other [15], [26], [65], [66] are some recently applications that use 2-D MUT arrays.

When array configurations are used, the beamforming function can be implemented. In ultrasound imaging, beamforming is referred to an implemented

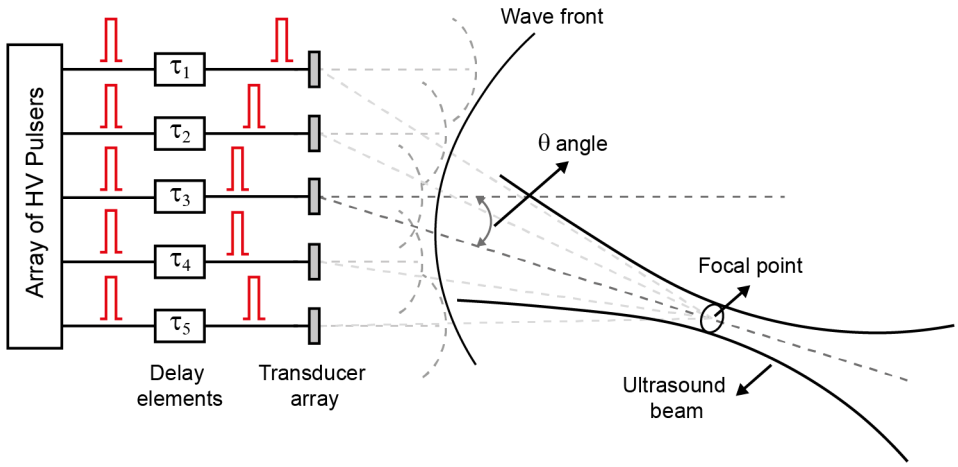


Figure 1.13: Transmit beam combined focusing and steering.

technique to shape the spatial distribution of the pressure field amplitude (the ultrasound beam) in a given volume [67]. In essence, when the beamforming technique is used, the transmit and received ultrasound signals are constructively combined in/from the desired location, whereas in/from other locations are filtered out. Beamforming can be divided into the simultaneous operations of focusing and steering [68]. Beam focusing refers to creating a narrow point in the ultrasound beam, which is defined as focal point. This point is a spatial location where the constructive interference occurs and the beam achieves the minimum width. The focal point can only be adjusted in the near-field region, defined by Eq. 1.1b. Beam steering refers to changing the principal direction of an ultrasound beam [69].

The beamforming function is realized by a beamformer circuit, which determines the shape, size and direction of the ultrasound beam. Figure 1.13 illustrates the general principle of the transmit beamforming. A transmit voltage excitation pattern is applied to the individual transducers elements in the array at the desired operation frequency, normally at or near the resonance frequency of the transducer. Delays are applied to the excitation pattern based on the steering angle θ and the distance from center of the array to focal point (focal distance). Each transducer element acts as a point source emitting a spherical wave, which propagates into the medium along the horizontal axis, and sums coherently at focal point. In this way, the ultrasound beam can be steered to scan various angles and be focused at different depth.

Beamforming is also done during reception in a similar fashion as on transmission. Figure 1.15 shows the beamforming technique implemented in the receive mode. When acoustic wavefront is reflected from an object, arrives at the transducer elements at different times, determined by the difference way between each element transducer and the object. The electrical signals by impinging acoustic wavefronts are time delayed through the delay elemnts in order to achieve that all echo signals will be aligned in phase at the summing point. Then a summer circuit sums the time-delayed waveforms to form a large electrical signal.

Beamforming technique offers a lot of advantages in ultrasound imaging application. Focusing operation creates a beamwidth narrower than what would be obtained for a non-focusing array, which means an improvement of the lateral resolution. Also, the peak pressure amplitude at the focal point is increased, and as consequence the signal-to-noise ratio is improved. The steering operation provides the ability to perform an electronic scan of the volume of interest, greatly reducing the time consumed for image reconstruction.

The beamforming controller circuit can be implemented in both analog and digital domains. In case of TX beamformer, the delays are typically implemented using digital control logic. For example, [70], [71] use a counter, shift registers and latch registers to implement the delay control unit. Also, [58], [72] propose a delay-locked-loop (DLL) based topology to define delays. For

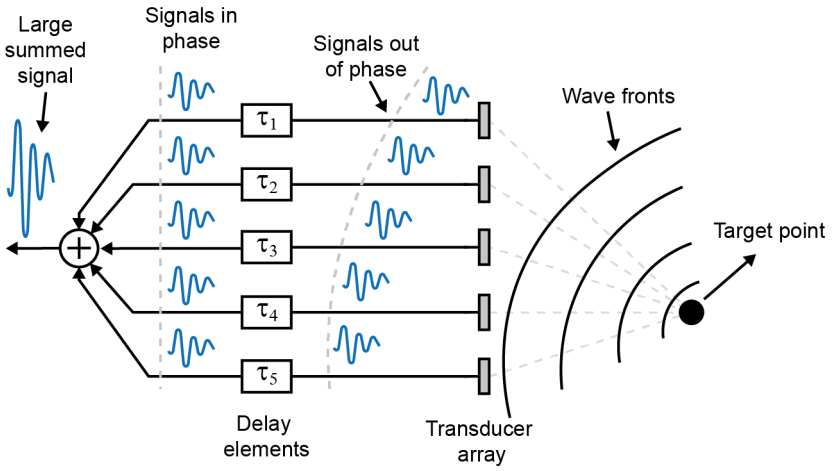


Figure 1.14: Illustration of the beamforming function in the received mode.

RX beamformer circuits the delay elements can be implemented using analog circuits as: switched-capacitor memory cells [27], all-pass filters [28], or LC based [29]. For digital RX beamforming implementations, the time delays are accomplished by using First-in First-out (FIFO) register [30] or by inclusion of field-programmable gate array (FPGA) chip in the system [31].

In addition to focusing and steering operations, apodization is sometimes used for transmit and receive beam formation. It is based on applying individual amplitude weights to each element of the array. In transmission mode, this involves exciting the transducer elements with non-uniform amplitudes to control the intensity profile across the ultrasound beam. In the receive mode it can be achieved by giving different amplifications to the received echo signals from each elements [64]. Apodization is used in order to reduce the presence of imaging artifacts caused by side lobes of the ultrasound beam. Side lobes are other acoustic beams on either side of the main beam, whose amplitudes are lower than the main lobe [69].

1.2.5 Signal-to-Noise Ratio

The Signal-to-Noise ratio (SNR) is another key parameter in the ultrasound systems since it has a great influence in the measurement accuracy and the image quality. The SNR depends on the differentiation of the meaningful echoes from the noise, which can be generated by the interference of undesired echoes from the surrounding objects and the electronic noise presented in the system components. There are some factors that can maximize the SNR at the output of the RX beamformer circuit. One of them is to increase the amplitude of the excitation signals. Aforementioned, the amplitude of the acoustic pressure emitted by a transducer is directly proportional to the amplitude of excitation signals, and therefore stronger echoes will be received if the emitted pressure in the media is increased. Another factor that will improve the SNR is to minimize the input referred noise of the LNA. To achieve these two factors, it is inevitable that the power consumption will be increased, which suggests that a trade-off should be achieved to obtain a desired SNR for low-power applications.

On the other hand, the implementation of the beamforming technique can also improve the SNR. TX focusing adds gain in the generation of the ultra-

sound beam. A general expression to compute the focusing gain is defined by [73] and rewritten as following:

$$G_{focal} = \frac{A^2}{F\lambda} \tag{1.2}$$

where A is the active aperture of the array, F is the distance from the center of the array to focal point (focal distance) and λ is the wavelength. Eq 1.2 suggests that the focusing gain is maximized when the focal point is closer to the transducers array. RX beamforming effect also improves the SNR. At the output of RX beamformer circuit, the correlated signals are added up constructively, and uncorrelated noise does not, giving a SNR improvement factor of $\sqrt{N}$, being N the number of RX channels [74].

1.3 Integration of MUTs to CMOS technology

On the way to the miniaturization of ultrasound systems, notable efforts, which is also present in this thesis, have been focused to combine MUTs and integrated circuits to form a single chip. Close integration of MUT transducers and supporting ICs enables shorter signal path lengths with superior electrical characteristics in terms of lower capacitive, inductive and resistive parasitic effects. This result causes the signal quality doesn't be degraded and therefore the achievable performance of the transducer is not limited.

To integrate MUTs with CMOS circuits several strategies have been adopted. These ones have been classified in three categories: Hybrid, Monolithic and Heterogeneous integration [75].

1.3.1 Hybrid Integration

In hybrid integration, the MUT and CMOS circuits are fabricated and tested on different wafers. The integration of both processes is performed at the chip level, where the MUT and IC chips are placed side-by-side or on top of each other, and are interconnected by wire [76], [77] or flip-chip [25], [74], [78] bonding. In wire-bonding, the interconnection are formed by a thin metal wire, which is mechanically and electrically connected using a wire-bonding tool to create chip-to-chip or chip-to-package interconnect [79]. In flip-chip

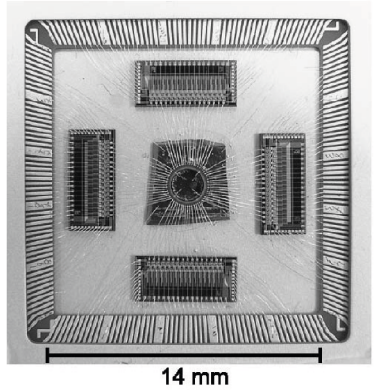


Figure 1.15: cMUT ring array wire bonded to CMOS electronics [76].

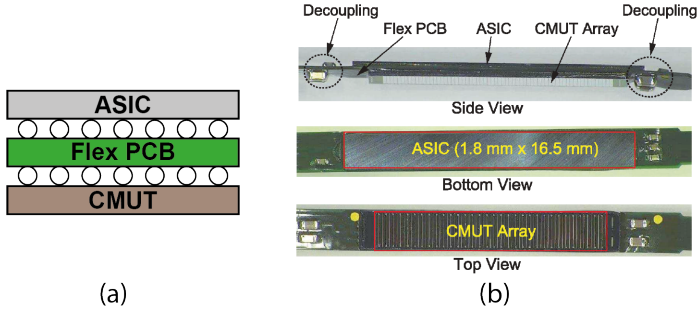


Figure 1.16: cMUT array flip-chip bonded to CMOS circuit. (a) Cross-section diagram, and (b) Photography of the prototype [25].

bonding, solder bumps are placed onto the chip pads, and then the chip is flipped upside down and aligned with another chip, with which is interconnect after a soldering process [80]. Hybrid integration approach using wire-bonding technology is most simple that flip-chip method due to an alignment process is not required, but at expense of occupying more area [75]. Figure 1.15 shows a 3-D ultrasound imaging system based on cMUT ring array, which was side-by-side wire bonded to a CMOS circuit, for intravascular applications [76]. In contrast, Fig 1.16 represents a prototype of a cMUT array flip-chip bonded to a CMOS circuit through an interposer Printed Circuit Board (PCB) for intracardiac echocardiography probes [25]. From figures 1.15 and 1.16, can be seen as the flip-chip technology optimizes the total area by its vertical placement.

Hybrid integration solution offers a modular approach, which allows an easy switching over to new generation of MUTs and more advance CMOS technol-

ogy because both processes are completely decoupled. Also, it enables rapid development cycles, reducing cost, time, risk, and time-to-market [81]. In contrast to theses advantages, MUT-CMOS systems based on hybrid integration have larger footprints and thickness, which limits their applicability when high density integration is needed. Besides, the wire/flip-chip bonding introduces parasitic elements that can be very harmful in very high frequency applications.

1.3.2 Monolithic Integration

In monolithic integration approach, the MUT device and the CMOS cirtcuit are building and combined on a same substrate. Until the beginning of the investigation that concerns this thesis, among MUT devices, only cMUTs have been possible to integrate monolithically with CMOS circuits. The most prevalent monolithic integration approaches to date include: cMUT-in-CMOS [82]–[87] and cMUT-on-CMOS [88]–[92].

cMUT-in-CMOS

The cMUT-in-CMOS process creates cMUT structures using the dielectrics and interconnection layers of the CMOS fabrication process, without adding any micromachining steps [82]. Generally, the first or any intermediate metal layer is used as sacrificial layer for the gap, and the adjacent metal or polysilicon layers are pattern to make top and bottom electrodes [83]. A post-CMOS wet etching step is necessary to release the cMUT membrane, and the sealing step for vacuum deposition in the cavity [82]. Since the sacrificial layer is a metal layer of CMOS process, the height cavity is limited by its thickness, which could affect the cMUT performance. Several efforts have been focused on improving this drawback; e.g, [85] proposes to use an interlayer metal, thinner than standard metal layers of the CMOS process, as sacrificial layer. With this architecture the height of the gap can be reduced and the cMUT sensitivity can be improved. Also, [87] proposes a titanium nitride composite (TiN-C) cMUT, where the sacrificial layer is composed by TiN-AlCu-TiN Metal-2 layer. After Al-etching and packing process, the height of the gap is around 200 nm, which is lower than the achieved one with standard CMOS process ($> 1\mu m$) [86].

In cMUT-in-CMOS both the cMUT device and ICs are built concurrently on

the same substrate, which means that the cMUT is fabricated side-by-side with electronic circuits. As consequence, the parasitic effects, fabrication time and production cost are greatly reduced in compare to hybrid integration approach. Fig 1.17 shows an schematic cross-section (Fig 1.17a), and Scanning Electron Micrograph (Fig 1.17b) of an ultrasound imager system based on 32x32 cMUT array manufactured using cMUT-in-CMOS approach.

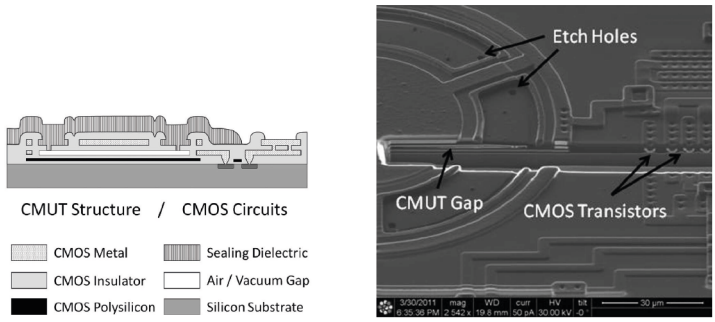


Figure 1.17: cMUT-in-CMOS process (a) Cross-section diagram, and (b) SEM image [83]

In contrast to the advantages mentioned above, the fabrication of the cMUT is limited by CMOS process options, in terms of materials and thickness. Moreover, the total area is not optimized due to side-by-side placement [89].

cMUT-on-CMOS

In the cMUT-on-CMOS approach, cMUT structures are completely built on top of a pre-processed CMOS wafer [89]. Most ultrasound systems based on cMUT-on-CMOS monolithic integration, the transducer is fabricated via layer deposition and surface micromachining, where the cMUT structures are built up layer-by-layer on the surface of complete CMOS wafer [88]–[92]. cMUT devices and electronic circuits are connected through interconnection vias, which greatly shortens the electrical connection paths, and as consequence the parasitic effects are drastically reduced in compare with integration strategies mentioned above. In contrast to cMUT-in-CMOS approach, in cMUT-on-CMOS, the available total area is used very efficiently, due to the cMUT transducer is located over CMOS circuits, hence this approach will be desired for large array

designs. Also, the cMUT structure is not constrained by CMOS fabrication process, therefore the transducer can be optimized in terms of materials and gap height, in order to obtain high performance cMUTs. The main disadvantage of this approach is that the deposition temperature for cMUT materials is limited to allowed temperature budget for the CMOS wafer [89].

Figure 1.18 shows a cross-sectional schematic and an optical image of a cMUT arrays for intravascular imaging, which was monolithically integrated on CMOS wafer using cMUT-on-CMOS approach.

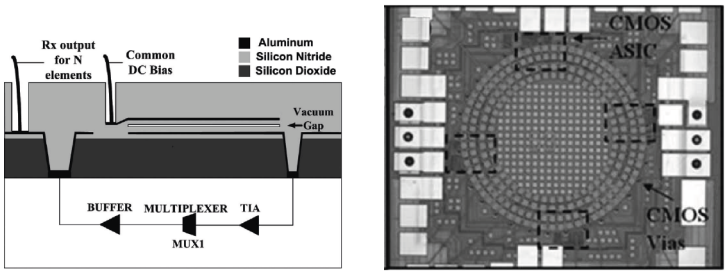


Figure 1.18: cMUT-On-CMOS process (a) Cross-sectional schematic, and (b) Optical image of the entire chip [83].

1.3.3 Heterogeneous Integration

Heterogeneous integration is an evolution of the hybrid approach, that allows two or more substrates, processed with different technologies (including MUTs and CMOS), to be combined at wafer level to form a System-on-Chip

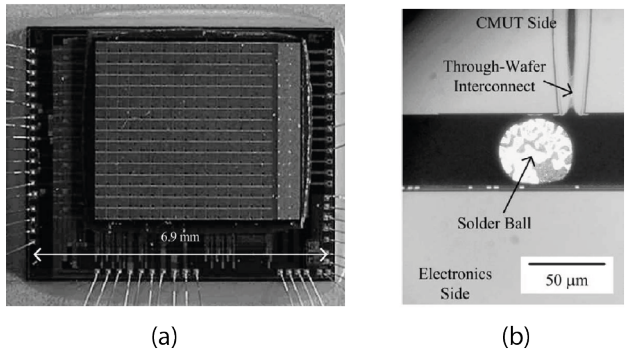


Figure 1.19: (a) Optical image of a cMUT array flip-chip bonded to a CMOS circuit, and (b) SEM image of a cross-section [93].

solution [80], [94]. A remarkable difference to hybrid process is that the integration step occurs at wafer level, whereas the hybrid approach is performed at the packaging level. The interconnection technology is close to the monolithic case, providing a vertical connection of the stacked system, which reduces the parasitic effects and optimizes the chip area [75]. Recently, the most establishes technologies to interconnect the two parts based on heterogeneous integration are: direct flip-chip bonding, where a pre-fabricated MUT wafer with through-vias is interconnected to a CMOS wafer with solder bumps on it [65], [66], [93], [95], and wafer bonding method, where a bonding material layer (e.g., germanium Ge) on the MUT wafer is eutecticaly bonded to the standard CMOS aluminum metalization [10], [14], [16], [17], [96]. Both methods allow to optimize the MUT performance and can achieve a high density integration, but require an aligned substrate-substrate process, which adds complexity to interconnection steps [97]. Moreover, in the direct flip-chip bonding method, the size of the solder bumps limits the MUT size and the gap between them when array configuration is used [14].

Figures 1.19 and 1.20 illustrate two MUT-to-CMOS heterogeneous integrated applications. Figure 1.19a shows an optical image of a 2D cMUT array integrated with a front-end electronic using direct flip-chip bonding technology for volumetric ultrasound imaging. Fig 1.19b illustrates a cross-section of the device after flip-chip bonding, where can be seem the through-wafer vias and the solder bumps.

Figure 1.20 shows an integrated pMUT-on-CMOS system using wafe bonding technologies for fingerprint applications. Fig 1.20a illustrates an schematic cross-section of the system, whereas Fig 1.20b shows a cross-sectional SEM image highlighting the Al-Ge eutectic pair bonding.

1.4 Research Framework

The research presented in this thesis has been carried out in the Electronics Circuits and System (ECAS) group in the Universitat Autónoma de Barcelona. The main research topics of the group involve:

- Design of Micro and nano-electromechanical devices (MEMS/NEMS).
- Integration of MEMS/NEMS resonators with standard CMOS process.

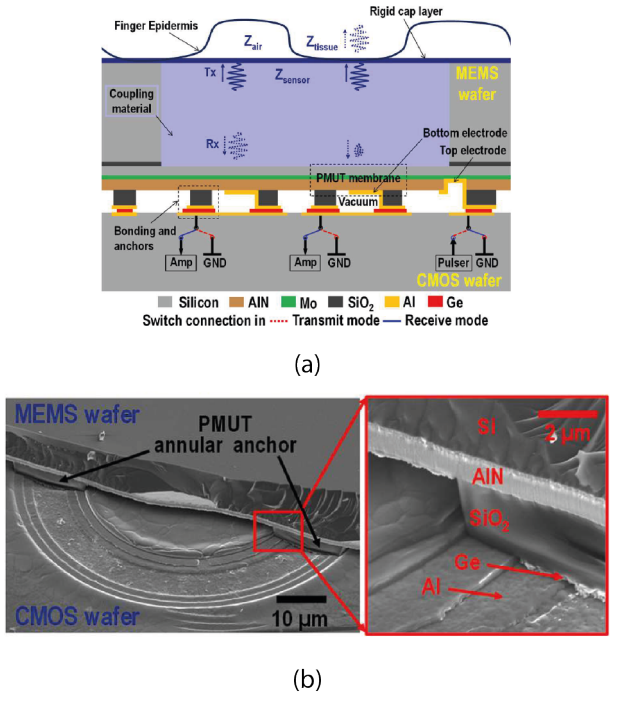


Figure 1.20: Fingerprint sensor based on pMUTs wafer bonded to CMOS circuits. (a) Cross-sectional system diagram, and (b) Cross-sectional SEM image [17].

- Design of front-end analog CMOS interfaces for fully integrated MEMS/NEMS systems.
- Novel Piezoelectrical Micromachined Ultrasound Transducers (pMUTs) for imaging and sensing in liquid and future gesture recognition applications.

The presented thesis has been performed under two different national projects:

- Emerging CMOS-M/NEMS resonant systems for smart sensing and novel ultrasound transducers. REF TEC2015-66337-R.
- Smart Multifrequency high-resolution PiezoMEMS-on-CMOS ultrasonic transducers for biometrics and imaging applications (Sonics-on-CMOS). REF PID2019-108270RB-I00.

In addition, this thesis project has been developed under the collaboration contract between ECAS group with the semiconductor manufacturing enterprise Silterra Malaysia Sdn. Bhd. As result of this collaboration, I have been

involved in the design pMUT-on-CMOS systems for ranging and imaging application using the Silterra MEMS-on-CMOS platform.

1.5 Thesis: Objectives and Outline

The focus of the present research is on designing the electronic interface for PMUT transducers, which will be, for the first time, monolithically integrated using the MUTs-on-CMOS approach. The specific objectives have been:

- Design of specific circuit aimed at driving and sensing the pmut transducer.
- Evaluation of the improvements achieved, in terms of signal to noise ratio, compared with the hybrid prototype.
- Application of the full system as an ultrasound imaging system. Beamforming techniques will be applied.
- Application of the full system as a distance measurement system.

The realization of PMUT-on-CMOS micro-system is discussed by means of examples of ultrasound applications. Consequently, the organization of this thesis is arranged as follow:

In **Chapter 2** the design of a High-Voltage driver is explained. In order to optimize the power efficiency, several architectures were reviewed and discussed. Simulation analysis and electrical characterization were done in order to evaluate the effectiveness of the chosen topology.

Chapter 3 describes the design of the Front-end Amplifier, which includes a Low-noise and high-gain amplifier(LNA) and a Variable Gain Amplifier (VGA). First, two different receive LNA approaches (VA and TIA) are reviewed and compared to evaluate which topology is more suitable for the pMUT-on-CMOS monolithic integration. A VGA circuit is designed to complete the amplification chain of an ultrasound system measurement.

Chapter 4 presents a prototype of a single pMUT-on-CMOS transceiver for imaging applications. The monolithically integrated system is compared to a wire-bonding system, composed of the same parts, in order to evaluate the effectiveness of the monolithic integration process.

In **Chapter 5** a prototype of 1D pMUT array monolithically integrated

over CMOS electronics is explained. First, several strategies to implement the beamforming technique are reviewed. Second, the overall 7x1 1-D ultrasound system is designed, which includes several transmission and reception channels, and then an extensively acoustic characterization is done, including B-mode imaging experiments.

Chapter 6 describes a new methodology to measure um-relative distances using pMUT transducers. Several methods used by ultrasound distance measurement systems are reviewed and compared. A complete description of the proposed methodology is presented, and an experimental demonstration is done using a single pMUT device.

Chapter 7 concludes this dissertation with discussion and a summary, which includes suggestions, approaches and applications for future work in the field of pMUTs.

CHAPTER 2

HIGH-VOLTAGE TRANSMITTERS FOR ULTRASOUND TRANSDUCERS

The transmitter (TX) circuit is in charge of driving an ultrasound transducer at its operating frequency, in order to emit enough acoustic pressure into the medium. Since the ultrasound wave propagation suffers from a strong attenuation, the TX circuit must drive the transducer with large voltage signals, with amplitudes ranging from tens of Volt to more than 100 V [98]. Depending on the excitation waveform, the TX circuit can be classified into: linear amplifiers and pulsers [36]. A TX linear amplifier is designed to obtain an output signal that is linearly proportional to the input signal, with a higher amplitude level [99]–[101]. It gives the possibility to excite the transducers with several driving waveforms. Unlike TX linear amplifiers, TX pulsers use a square input signal (normally low voltage) and generates high-voltage pulses, which can alternate between two voltage levels (unipolar or bipolar pulser) [5], [16], [90], [102]–[104] or to stagger different voltage levels (multi-levels pulser) [51], [70], [74], [105]. Although both transmitter types have been widely used in the state-of-the-art, TX pulser are preferred in microelectronic, since their designs are less complex and more power-efficiency [36]. Advances in CMOS technology have enable the High-Voltage (HV) process option, which has been a key factor to integrate the TX circuit into Ultrasound System-on-chip. In this chapter several architectures used for HV TX pulser are discussed, and a

solution adopted to drive pMUT transducers is described. Also, a summary comparison with state-of-the-arte is done.

2.1 Driving signal characteristics

The generated signal by the transmitter circuit has a strong dependence with the transducer element. The shape of the acoustic pulse emitted into surrounding media is limited by the transducer characteristics. Figure 2.1 shows the lumped Butterworth Van-Dyke electrical model to mimic the impedance of the transducer. The motion-branch impedance represented by the series combination of R_m, C_m, and L_m, models the mechanical resonance of the transducer, and the shunt parasitic capacitance C_0 is dominated by the overlap of the top and bottom electrodes. The effectiveness of this model have been demonstrated for pMUT [26], cMUT [51], and piezoelectric bulk [52] transducers. For pMUTs used in this thesis, R_m value is around of units of MΩs, C_m is lower than 1 fF, L_m is around of units of Henry, and C_0 is lower than 300 fF, which is translated to resonance frequencies in a range from 2 MHz to 20 MHz [22], [106]–[108].

When the transducer is operated in linear regime at its resonance frequency, it needs around Q cycles to ring-up to full amplitude [48]. This means that in order to improve the axial resolution low quality factor transducers are desired. Considering this, the transmit circuit must excite to the transducer during Q cycles, in order to optimize SNR and axial resolution.

The selection of driving amplitudes are dependent of the transmit sensitivity of the transducer, and the required SNR at a given distance. Figure 2.2a shows

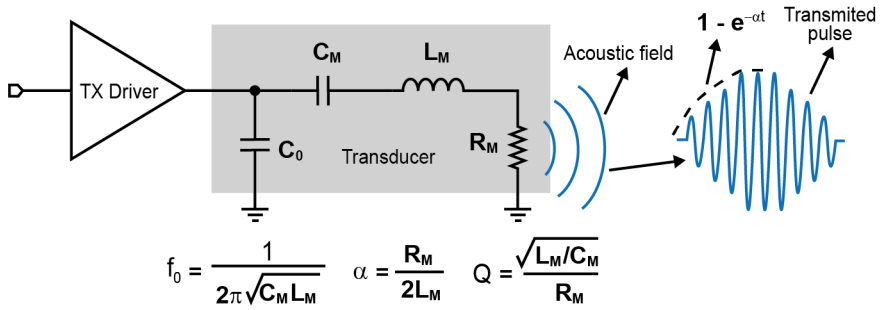
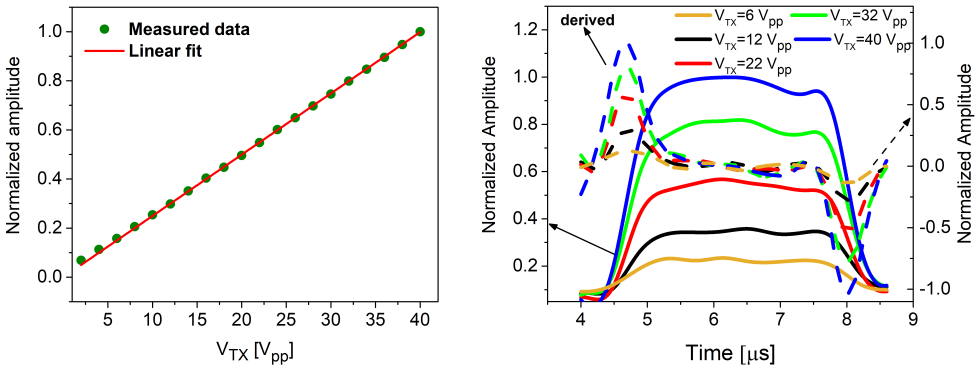


Figure 2.1: Butterworth Van-Dyke model for MUT transducers.



(a) (b)

Figure 2.2: (a) Normalized emitted pressure by pMUT as a function of the excitation signal, (b) Measured output envelope when the pMUT was driven with different voltage amplitudes.

the normalized amplitude at the output of a commercial hydrophone (ONDA-HNC-1500), which was used to measure the acoustic power emitted by one of our pMUTs at 3 mm, using fluorinert FC-70 as propagation media. The pMUT transducers was driven with eight cycles sine signal at 2.4 MHz with amplitudes from 1 Vpp to 40 Vpp. As result, the pMUT showed a linear behavior defined by its transmit sensitivity. On the other hand, the envelope of five of the received signals by the hydrophone were detected. As is illustrated in Fig 2.2b, when the amplitude of the excitation signal is increased, the envelopes reach the maximum value faster than for small excitation voltages. This means that if large driving voltages are used, the excitation time can be reduced, and the axial resolution can be improved. Taking into account that the CMOS process from Silterra has 1.5 V, 3.3 V, 5 V, 6 V, and 32 V transistors options, we have selected a process with 32 V transistors in order to improve SNR and axial resolution.

Usually, our pMUT devices have a bandpass filter behavior with a narrow bandwidth, around 1 MHz [22], [108], [109]. Considering this, the linearity of the transmitter circuit is not an important consideration, hence two-level pulses can be used to drive pMUT transducers. Moreover, at fundamental frequency, when square signals are used to excite the pMUT, the emitted pressure is around 1.27 times higher than when sine driving signals are used [110].

2.2 Trade-offs in HV Pulser design

The need to use HV technology process in TX circuit design implies that careful analysis must be done, especially if the intended application is a portable device, which need longer battery life and high density integration. Essential for this analysis is to consider three key requirements: power consumption, operation speed and area.

The overall power consumption is the sum of static and dynamic power dissipation. Since the pulse-echo method is employed by majority of Ultrasound systems, which means that the TX circuit will be in idle state for a long time of operation(around 1% or 2% of duty cycle), the static power consumption must be zero.

The dynamic power is only dissipated each time the TX input signal changes states. It is calculated by adding the short-circuit power consumption (instantaneous short-circuit connection between power-supply and ground), and capacitive-load power consumption (when charging and discharging the load capacitance). The first one has a strong dependency on the duration of the transition times, and the aspect ratio of the transistors involved in creating the parasitic path. The second one, is directly proportional to the operation frequency and the load capacitance.

Considering the RLC circuit represented in Fig 2.1 as transmitter load, if the transducer is driven at its resonance frequency, this electrical model is simplified to the parallel connection of R_m and C_m. Taking into account this, the electrical power dissipated by the R_m resistor (V_{rmsTX}^2/R_m) is converted to acoustic power through the transmit sensitivity of the transducer, where V_{rmsTX} is the root-mean-square of the excitation signal, whereas the power dissipated by the C_0, defined as $C_0 f V_{TX}^2$, contributes to capacitive-load power consumption, where V_{TX} is the peak value of the excitation signal, is wasted [51]. Considering this, a trade-off between acoustic pressure level transmitted into the medium and dynamic power consumption must be achieved.

Related to overall power consumption, there is another useful parameter that is very used to evaluate the TX circuit performance: the TX efficiency. It is defined as the ratio between the electrical power dissipation converted to acoustic power (V_{rmsTX}^2/R_m), and the total power dissipated, which includes

static and dynamic power consumption [51]. Power-efficiency TX circuit are desired, especially if low power applications are required.

The operation speed of the TX circuit is determined by the charge and discharge times of the load capacitance. Usually, in HV TX Pulsers the load capacitance is charged to V_{TX} through a pull-up pMOS transistor, whereas is discharged through a pull-down nMOS transistor. Considering this, the operation speed can be described in terms of propagation and transition times of the driving signal. The first one can be defined as the delay time between 50% points of the maximum value of the input and output, whereas the second are the difference time when the output changes from 10% to 90% of the maximum value of the output signal. Both, propagation and transition times are directly proportional to $\sim 1/W_{n,p}$, where W is the width of the transistor and the subscript n, p are referred to nMOS pull-down transistor and pMOS pull-up transistor, respectively. Considering this, if wide transistors are used, high operation speed is guarantee. However, wide transistors consume a lot of area, and increase the parasitic capacitance of the internal nodes of the TX circuitry, which could affect the operation speed. Taking into account this, from a design perspective, a trade off between occupied area and high speed operation is needed.

2.3 High-Voltage Pulser Architectures

Several HV pulser architectures have been used to drive MUT transducers. The simplest HV pulser is adopted by [90], where a single HV nMOS transistor

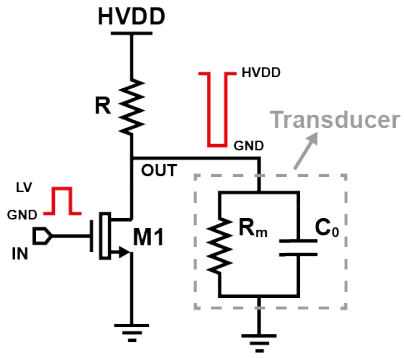


Figure 2.3: TX circuit implementation using a single HV nMOS transistor with a pull-up resistor [90].

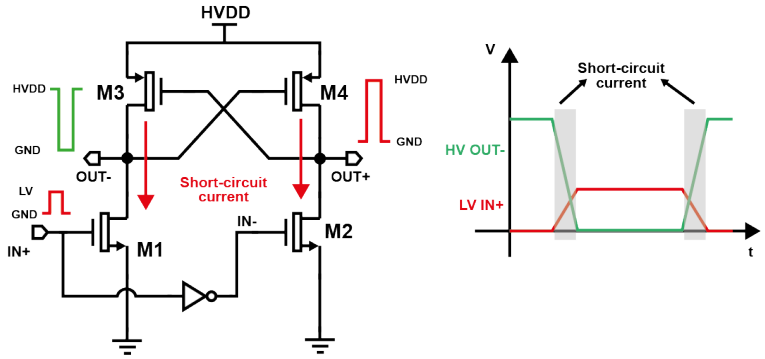


Figure 2.4: Conventional HV level-shifter with time diagram to illustrate when the short-circuit current flows [5].

and a pull-up poly resistor is used to convert 3.3 V unipolar input pulse into unipolar HV output pulse. A schematic circuit of this architecture is shown in Fig 2.3. This topology takes an advantage of being very simple and occupying a small area, hence it will be a practical solution where the space is limited, as occurs in intra-vascular ultrasound catheter-based clinical applications. However, this circuit suffers of several drawbacks. The first one is when the output signal is in low state, a direct current path is created from HV power supply to ground, which causes a large static power consumption. Moreover, the pull-up resistor limits the low-to-high transition of the driving voltage, which affects the operation speed.

Alternatively, a cross-coupled level shifter circuit in Fig 2.4 was proposed by [5], and was used to reduce the power consumption, avoiding the static

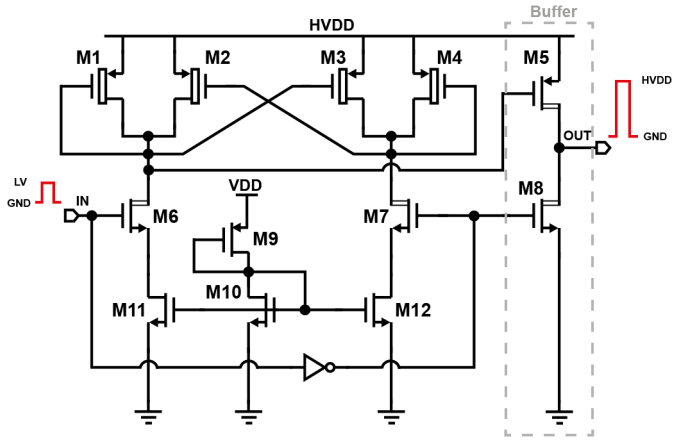


Figure 2.5: HV level-shifter with current limit [111].

current path. It consists on a nMOS differential pair that pulls the output nodes to ground, and the pull-up pMOS transistors as load. This structure although eliminates the static power consumption, during transitions of the input and output signals, suffers from a relative high short-circuit current, when both nMOS and pMOS transistors on the same branch are conducting. This current flow adds a wasted short-circuit power dissipation to the overall power consumption, which limits the TX circuit efficiency.

In order to reduce the short-circuit current, several level shifter topologies have been adopted. Figure 2.5 shows a cross-coupled level shifter with current limitation. This circuit, proposed by [111], uses a similar level shifter structure of Fig 2.5, but introduces a current mirror formed by low-voltage transistors M10-M12 to limits the short-circuit current, and an output stage to drive large capacitive loads. Since the output HV pMOS transistor M5 has a gate-oxide breakdown voltage much lower than the HV power supply, diode-connected pMOS transistors M1 and M4 are used to reduce the gate-source voltage of M5, when the common-source M6 transistor is in on. This structure, although it can be used to reduce the dynamic power dissipation, the operation speed decreases due to the reduced current, and the total area is increased.

The level shifter structure showed in Fig 2.6 achieves fast switching and reduces the short-circuit current. In this case, two pairs of cascode transistors are placed in series with nMOS input pair [16], [93], [112]. The purpose of the pMOS cascode transistors is to reduce the overdrive voltage of the pull-up

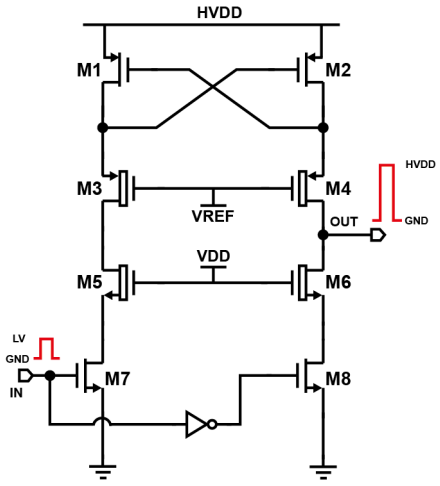


Figure 2.6: HV level-shifter with voltage limit [93].

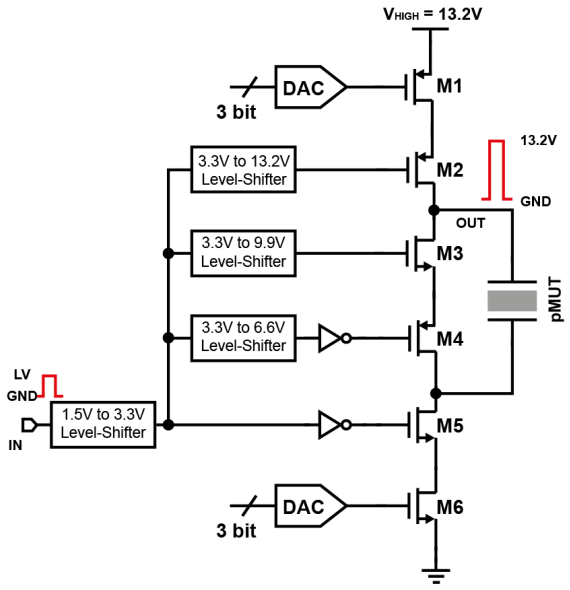


Figure 2.7: Charge-Recycling HV Pulser [26].

pMOS transistors, whereas the nMOS cascode pair reduces the drain-source voltage of the nMOS pull-down transistors. This causes a reduction of the short-circuit current and brings the possibility to use smaller pull-up and pull-down transistors, with which the parasitic capacitance are reduced and as consequence high operation speed is ensured. The main drawback of this structure is that requires different power supply levels, which is not desired.

In addition to the HV Pulser based on level shifter structures, there are other topologies to drive MUT transducers, which are mainly addressed to reduce the dynamic power consumption associated with the charge and discharge of the load capacitance ($fC_LV_{TX}^2$). For example, in Fig 2.7 is shown a TX circuit to drive a bimorph pMUT using the charge-recycling mechanism [26]. Its working principle is as following: during low-to-high transition of the input signal, takes place the charging phase, where the outer electrode is connected to V_{HIGH} through M1 and M2 transistors, and the inner electrode is grounded through M5 and M6 transistors. When the high-to-low transition occurs, M1-M2 and M5-M6 are turn off and M3-M4 are turn on, which causes that the outer and inner electrodes will be shorted. This gives rise to a charge redistribution process, and as a consequence the electrical capacitance associated with the outer and inner electrodes are charged to the same intermediate voltage (V_x). In the next charging phase, the outer electrode is charged from V_x to V_{HIGH}

and the inner electrode is discharged from V_x to ground. If the capacitance associated to outer and inner electrodes are the same, around $fC_LV_{TX}^2/2$ is saved. In order to use a standard CMOS fabrication process (less complex than HV CMOS process), six low-voltage transistors (M1-M6) were stacked and driven with appropriate gate voltages to generate the required excitation voltage. The two digital-analog converters and M1 and M6 transistors are used to compensate the dispersion of pMUT performance due to manufacturing process variation.

The TX circuit shown in Fig 2.7 although it can reduce the $fC_LV_{TX}^2$ dynamic power consumption, it suffers the same drawback of the architecture shown in Fig 2.6. Moreover, this TX circuit is only area-power efficient when driving high performance pMUTs, that can be excited with medium voltage to transmit enough acoustic pressure. If high voltage is required to drive the transducer, lot of transistors must be stacked, which increases the complexity and area of the TX circuit.

Other architectures intended to reduce the dynamic power dissipated by charging and discharging the load capacitance, are the multi-level pulsers. An N-level pulser employs $N-1$ HV switches, each connected to a regulated voltage source, to charge and discharge the load capacitance in a stepwise fashion. Thus, the dynamic power dissipation due to $fC_LV_{TX}^2$ is reduced by a factor of $1/(N-1)$ [51]. An implementation example of a multi-level pulser is shown in Fig 2.8, where 3-level pulses are obtained by adding return-to-zero switching to bipolar HV pulser [70]. Figure 2.8a shows the general diagram of the complete pulser, where conventional level-shifters are used in conjunction with a novel output stage to provide the return-to-zero pulsers. Figure 2.8b illustrates the circuit used to generate of the high-side pulser with the return-to-zero switch. HV transistors MP and M1 are turned on to pull the transducer to high output voltage (HV_{VDD}), while HV M1 and M3 are used to provide the return-to-zero switching. The HV M2 transistor and the parasitic capacitance relative to M1 and M2 are used as floating-gate driver. During TX phase the source of the M2 is grounded, with which the gate of M1 is floating. When MP is turned on and M3 is turned off, part of the HV pulse is coupled into the M1 gate through the capacitor divider formed by C_{GS1}, C_{DS2} and C_{SUB} parasitic capacitance, which causes that M1 turns on, and as consequence the transducer is pulled to HV_{VDD}. When MP is turned off, M1 remains on, and

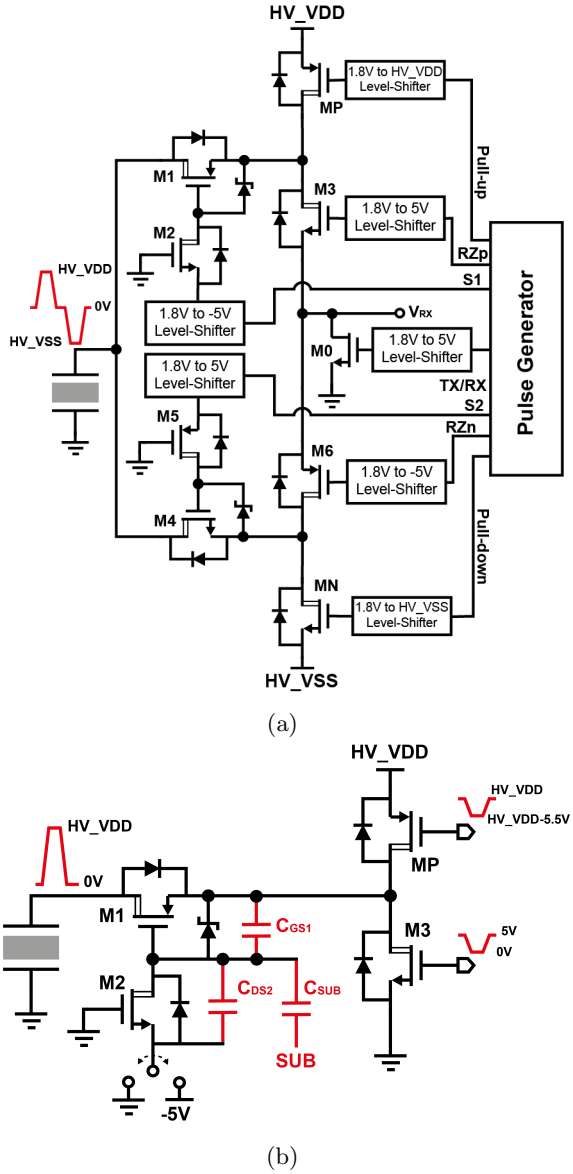


Figure 2.8: (a) Circuit diagram for complete HV bipolar pulser with return-to-zero switching and (b), Circuit diagram for a high-side with return-to-zero pulser [70].

when M3 is turned on, a direct discharging path from the transducer to ground is created, allowing the return-to-zero operation. An identical, complementary design to that of Fig 2.8b is used for the transition from ground to HV_{VSS} and HV_{VSS} to ground, to generate the 60 V_{pp} bipolar pulse with return-to-zero.

Multi-level pulser approach although reduces the dynamic power consump-

tion, and therefore improving the TX efficiency, has several drawbacks. First, they also need several power supply levels to generate the required waveform, which is not desired. Second, their architectures are more complicated and area spenders in compare to unipolar pulser.

Considering the advantages and disadvantages of the main HV pulser architectures used in the state-of-the-art, in this thesis an unipolar level-shifter topology is chosen due to simplicity, and a suppression mechanism of the short-circuit current is added to reduce the dynamic power consumption. The details of the circuit will be described in the next section.

2.4 Implemented Detailed Circuit Diagram

Figure 2.9a shows the main core of the HV Pulser used in this research to drive pMUT transducers. It was first proposed by [113], and it is composed by a conventional level shifter shown in Fig 2.4, with two HV pMOS switches connected in series between HV pull-up pMOS and HV pull-down nMOS transistors that forms the cross-coupled load. The main function of these HV switches is to suppress the short-circuit current flow when both the nMOS input transistors (M1 and M2) and pMOS latches transistors (M3 and M4) are conducting, which will cause a reduction of the dynamic power consumption and an improvement of the TX efficiency. A proper operation of the circuit

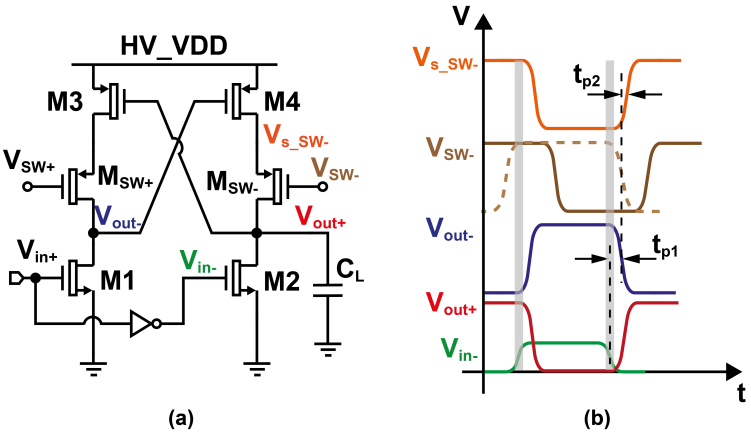


Figure 2.9: (a)High-Voltage Level Shifter with crowbar current mechanism suppression, and (b) Time diagram with involved signals in the performance of the right side of the circuit shown in (a).

shown in Fig 2.9a would take place if both HV switches keep open during each transition of the input signal V_{in}. This performance can be achieved in two different approaches but, in both cases it is necessary to guarantee that transitions from low-to-high and high-to-low of the V_{in} and V_{SW} signals do not occur at the same time. The first one consists of modifying the duty cycle of the control signals V_{SW+} and V_{SW-}, as shown in brown dashed line in Fig 2.9b. To achieve this is necessary to implement a HV non-overlapping circuit, which could increase area and power consumption. The second one, represented in brown solid line in Fig 2.9b, and is adopted in this thesis, is based on driving the HV switches (M_{SW+} and M_{SW-}) with a delayed replica of the output signals (V_{out+} and V_{out-}). In this case, as shown in Fig 2.9b, in the low-to-high transition of V_{in-}, V_{SW-} is in high level, and therefore the M_{SW-} transistor is off, avoiding that a current flows from HV_VDD to ground. For high-to-low transition of V_{in-}, the short-circuit current flow is avoided due to the propagation delay time between V_{in-} and V_{s_SW-} signals ($t_{p1} + t_{p2}$ in Fig 2.9b), which is the sum of the propagation delay time between V_{in+} and V_{out-} (t_{p1}), and V_{s_SW-} regarding V_{out-} (t_{p1}), neglecting the retard added by the low voltage inverter. If $t_{p1} + t_{p2}$ is higher than the fall time of V_{in-}, the short-circuit current could be avoided. This will occur because in the high-to-low transition of V_{in-} (fall time), the source voltage of M_{SW-} (V_{s_SW-}) will be low (due to the propagation delay time $t_{p1} + t_{p2}$), with which the HV M_{SW-} switch will be open regardless of the state of its control signal (V_{SW-}). As shown in Fig 2.9, the propagation delay time, $t_{p1} + t_{p2}$, is mostly dominated by the propagation delay time between V_{in-} and V_{out-} (t_{p1}), due to the threshold voltage of M1 is close to V_{in+}, and as consequence the equivalent resistance when it is conducting is relatively large. An analogous analysis can be done for the left branch of the circuit represented in Fig 2.9a.

Taking into account that the driving signal for HV switches, V_{SW+} and V_{SW-}, are a delayed replica of the V_{out-} and V_{out+}, respectively, they can be generated from the output signals of a similar level-shifter proposed in Fig. 2.9a, where whose inputs will be a delayed replica of the V_{in+} and V_{in-}. In this way, a delay element and two HV level-shifter with short-circuit current suppression mechanism, are connected of the proper form to implement an unipolar HV Pulser. The complete circuit is shown in Fig. 2.10, where a HV output buffer is added for testing purpose, in order to drive a large load

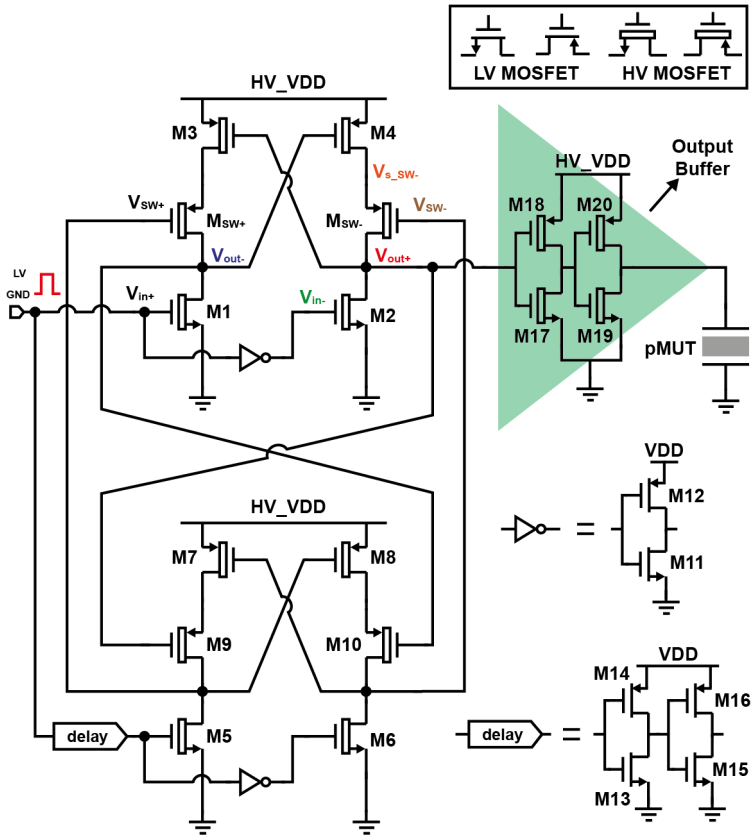


Figure 2.10: Complete architecture of the proposed HV Pulser.

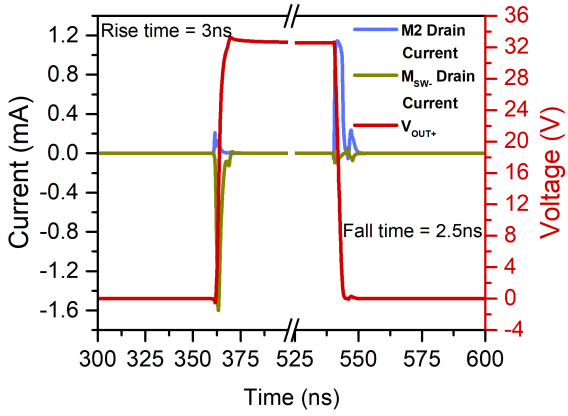


Figure 2.11: Voltage and source and sink currents in the Vout+ node.

capacitance.

A proper sizing of the transistors was done, to guarantee that $t_{p1} + t_{p2}$

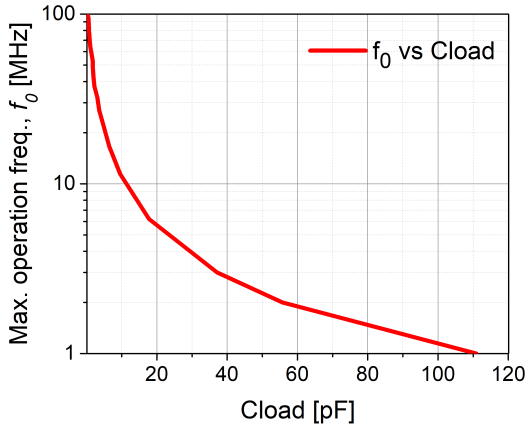


Figure 2.12: Maximum transmitter operating frequency as a function of load capacitance (simulation results).

Table 2.1: Dimensions of the MOSFET devices used in the HV Pulser

MOSFETs	**Aspect Ratio (W/L) (μm/μm)**
M1, M2	20/5.75
M3, M4, M_{SW+}, M_{SW-}	10/4
M5, M6	10/5.75
M7, M8, M9, M10	4.7/4
M11	10/1
M12	25/1
M13	1/4
M14	2.5/4
M15	1/3
M16	2.5/3
M17	10/4.8
M18	25/4
M19	20/4.8
M20	50/4

will be 4 times higher than the fall time of V_{in-}, and the delay element will introduce a retard of 8 ns to V_{in+}. Fig. 2.11 illustrates the simulated source and sink currents and the rise and fall times in the V_{out+} node. It can be seen how the presence of the M_{SW+} and M_{SW-} devices allows for the removal of the crowbar current. The dimensions of the selected MOSFETs for this circuit are shown in Table 2.1. Since the input capacitance of the output buffer charges the first level-shifter, the transistors of this one were dimensioned larger than those of the second level-shifter, resulting an improvement of the operation speed.

Figure 2.12 shows the simulation results of the maximum operation fre-

quency of the proposed HV Pulser, taking into account the designed output buffer, as a function of the load capacitance. Taking into account that the capacitance associated to an individual pMUT is in the range of 200 fF [109], Fig 2.12 indicates the maximum number of pMUTs simultaneously actuated by the proposed HV Pulser at a given frequency (e.g., in the case of 3 MHz, the maximum capacitance corresponded to 37 pF, which is equivalent to 185 individual pMUTs, a reasonable number for array configurations).

2.5 Experimental Results

The HV Pulser has been realized in 0.13 μm HV CMOS process from Silterra, which incorporates up to six levels of interconnection and provides 1.5 V, 3.3 V, 5.0 V, 6.0 V and 32 V N-P MOS transistors. Fig. 2.13 shows the final layout and the fabricated chip, which occupies a total area of 0.013 mm^2.

The HV transmitter circuit was characterized in terms of operation speed, power consumption and efficiency. For testing purpose, the chip was wire bonded to a Printed Circuit Board (PCB), and a function generator (Keysight 81150A, Santa Rosa, CA, USA) and an oscilloscope (Keysight DSOX3054A, Santa Rosa, CA, USA) were used to generate the input signal and measure the output signal, respectively. The circuit operated from two power supplies (3.3 V and 32 V), and with a 3.3-V-squared input signal with around 5 ns of rise and fall times. The dotted lines of the Fig. 2.14 represent the measured input and output waveforms of the HV Pulser, which achieves a rise/fall time of 47.5 ns and a propagation delay time around 31 ns. The solid lines in Fig. 2.14 show the simulation results when 17 pF (equivalent to 14 pF of the input port of the oscilloscope and 3 pF of parasitic capacitance, estimated from PCB and connectors) in parallel with 1 MΩ resistor was used as load impedance. As can

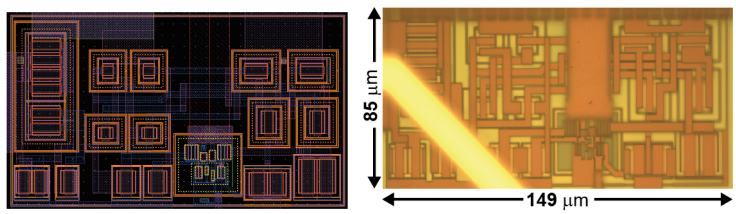


Figure 2.13: (a) Layout of the HV Pulser, and (b) optical image.

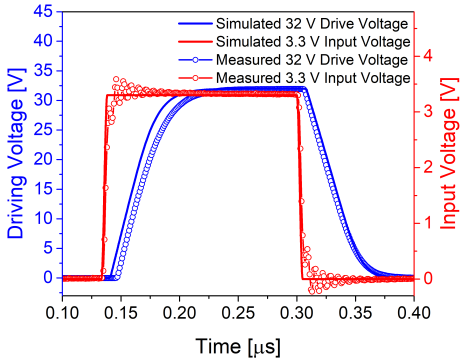


Figure 2.14: Simulated and measured waveform of the HV Pulser input and output.

be shown, the measurement is in good agreement with the simulation ones, differing in only 6.36 ns in both rise/fall times and 50%-50% latency, which may be caused by the estimation of the parasitic capacitance.

Taking into account the good agreement between simulated and measured results, the TX circuit efficiency, without considering the transducer, was estimated from simulation results. Fig. 2.15 shows the simulated output signal of the Fig. 2.14 in the rise time interval, the currents from 32 V and 3.3 V power supplies, and the current in 17 pF load capacitance. Neglecting the static power consumption and the dynamic power consumption from 3.3V power supply, the TX circuit efficiency was obtained dividing the root-mean squared (rms) output current (provided to the load capacitance) between rms current generated by the 32 V power supply, obtaining an efficiency of 98%.

Table 2 summarizes and compares our HV pulser to prior reported works. To

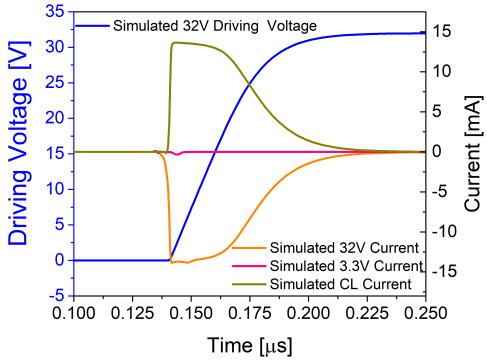


Figure 2.15: Simulated output waveform, sourced current from 32 V and 3.3 V power supplies, and sink current in load capacitance.

Table 2.2: HV Pulser performance summary and comparison

	This Work	**[26] (2021)**	**[70] (2020)**	**[102] (2017)**	**[16] (2016)**	**[74] (2016)**
Process technology	0.13μm HV CMOS	0.18μm CMOS	TSMC 0.18μm HV BCD	0.18μm HV BCD8-SOI	0.18μm HV CMOS	TSMC 0.18μm HV CMOS
Pulsed output voltage [V]	32	13.2	60Vpp	100	24	30
Load capacitance [pF]	17	N/A	18	9.2	2	2
TX freq [MHz]	3	5	9	10	14	5
Area [mm^2]	0.013	0.02	0.167	0.09[1]	0.017[1]	0.016
Rise time [ns]	47.5	N/A	N/A	14	10.56[2]	6.6
$fC_LV_{TX}^2$ saving [%]	0	42.6	∼50	0	0	46
FOM_{TX} [mA/mm^2]	881	-	-	732	267	568

[1] These areas were estimated using a chip micrograph.
[2] Obtained as trise = 2.2RC$_L$, where R = Vmax/Imax.

quantify the performance of these circuits, we have defined a Figure-of-Merit as following:

$$FOM_{TX}[mA/mm^2] = \frac{V_{TX}[V]C_L[pF]}{t_{rise}[ns]A_{TX}[mm^2]} \tag{2.1}$$

where V_{TX} is the maximum driving voltage, C_L is the load capacitance, t_{rise} is the rise time, and A_{TX} is the total area of the HV Pulser. Considering this, the proposed transmitter circuitry achieves the best FOM_{TX} (881 mA/mm^2), which is greatly attributed to the small area it presents (the smallest in Table 2.2). Despite this fact, the proposed HV pulser does not save any dynamic power consumption relative to $fC_LV_{TX}^2$, which will affect the overall transmission efficiency (emitted acoustic power/total power consumption). To improve this, the approaches proposed by [26], [70], [74] must be considered or to design a transducer with a high transmission sensibility.

2.6 Conclusion

A High-Voltage Pulser with a good balance between power and area-efficiency has been proposed. It is based in a conventional level-shifter structure with additional short-circuit current suppression mechanism in order to reduce the dynamic power consumption. An electrical characterization was realized, obtaining a competitive results with prior works, highlighting the small occupied area, which makes it an attractive driver for pMUT devices. If the overall transmission efficiency would like to be improved, HV Pulser with

charge-recycling or multi-level pulser approaches can be adopted.

CHAPTER 3

RX FRONT-END AMPLIFIERS FOR ULTRASOUND TRANSDUCERS

In the reception mode, the transducer is interfaced to the receiver (RX) circuitry in order to amplify the weak signals sensed by the transducer. The complete analog front-end ultrasound receiver consists of: low-noise amplifier (LNA), time-gain compensation amplifier (TGC), and transmit-and-reception switches (TRX SWs). This chapter describes the design of the LNA and TGC amplifiers. At first instant, the key requirements and several topologies for LNA are presented. This is followed by the implementation, characterization and comparison with the state-of-the-art of two of the most used LNA topologies for conditioning pMUT devices. After, the concept of TGC function is introduced, and an implementation of a Variable Gain Amplifier (VGA) to perform it, is presented. Finally, this chapter concludes with a discussion. The TRX SWs are presented in Chapters 4 and 5.

3.1 Characteristics of the pMUT as a sensor

As was explained in Chapter 1, the transducer impedance model is very useful during front-end amplifier design since it represents the impedance of

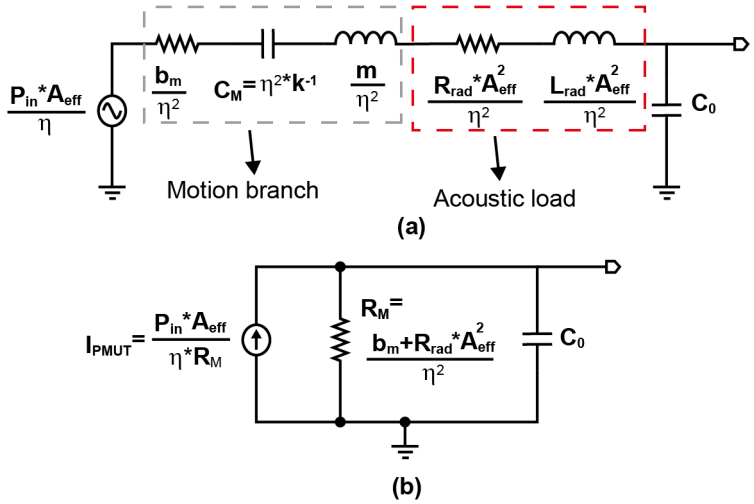


Figure 3.1: (a) Simplified electrical model of the pMUT in receiving mode, and (b) Expanded model with a current source of the pMUT in receiving mode at its resonance frequency.

the signal source at the LNA input. Therefore, the design requirements of the LNA are constrained by the impedance of the transducer in terms of frequency response, input noise, amplification type, etc. In the receive mode the pMUT acts as a sensor, and senses the dynamic mechanical excitation caused by the applied force over pMUT surface when an acoustic pressure is received. This transduction mechanism can be introduced to the electrical circuit shown in Fig 1.9b in form of a voltage source, that is coupled in series with the motion branch, see Fig 3.1a. This voltage source is frequency depended, and its value is determined by the effective area of the pMUT (A_{eff}), the electromechanical coupling coefficient (η) and the amplitude of the received pressure (P_{in}). On the other hand, when the pMUT is used in immersion, the radiation impedance of the media loads the pMUT (see Fig 3.1a), which modifies its frequency response. The imaginary part of the radiation impedance of the media (L_{rad}) causes a reduction of the resonance frequency of the pMUT, whereas the real part R_{rad} decreases the quality factor (Q) of the pMUT [114].

Our research group has designed a variety of pMUTs in terms of size, layer thicknesses, geometric forms, and piezoelectric materials, which causes that a range of electrical impedance of the transducer will be used for designing the front-end electronic instead of an unique RLC model. Considering fluorinert (ρ=1940 kg/m^3, c=685 m/s), distilled water (ρ=1000 kg/m^3, c=1500 m/s),

and polydimethylsiloxane (PDMS, ρ=982 kg/m^3, c=1000 m/s) as target propagation mediums, the R_M values are in a range of 10MΩ - 60MΩ, L_M from 3 H to 15 H, C_M from 0.7 fF to 3 fF, and C_0 from 200 fF to 500 fF. For these values, the pMUT resonance frequencies are in a range from 1 MHz to 12 MHz with the transducer's bandwidths from 1MHz to 3 MHz.

Usually, the pMUT is operated at its resonance frequency of the first resonance mode, or close to this one, with which the circuit of the Fig 3.1a can be simplified by ignoring the impedance of L_M and C_M. Moreover, since the R_M values are much higher than the impedance range of C_0, is more convenient to consider the pMUT as a current sensor instead of the voltage sensor. Considering this, based on Norton's theorem, the electrical circuit of the Fig 3.1a can be represented by the circuit shown in Fig 3.1b, where I_{PMUT} is the pMUT's short-circuit current. In this chapter we will use the electrical circuit represented in Fig 3.1b to model the pMUT as sensor, in order to design the signal conditioning circuit.

3.2 Requirements for LNA Amplifiers

The analysis of the pMUT characteristics as a sensor provides useful information for the receive (RX) interface electronic design. The RX amplifier requires an input that will be matched to the pMUT device, in terms of impedance, noise level, area, bandwidth, linearity, etc.

Design requirements

- Input noise

  The resistor R_M in the circuit shown in Fig 3.1b is the main noise source of the pMUT. It has a current thermal noise density defined as $4kT/R_M$, where k is the Boltzmann's constant, and T is the temperature in Kelvin. Based on the estimated values range of R_M, and considering the room temperature (T=300K), the estimated thermal noise density of the pMUT is in a range from 0.28x10$^{-27}A^2/Hz$ to 1.66x10$^{-27}A^2/Hz$. To have an order-of-magnitude estimation of the noise generated by the transducer element itself, we have integrated the thermal noise density over the pMUT's bandwidth (∼1MHz). The resulting noise currents are

in a range from 17 pArms to 41 pArms. Considering that, the noise levels of the transducer is very low, the RX front-end amplifier must adopt a Low-Noise Amplifier (LNA) topology. A proper readout circuit should be designed in such a way that the input-referred noise of the LNA must be equivalent to or lower than the noise of the pMUT.

- Area

  The area of the LNA should fit within the area of the pMUT device, in order to design a pixel pitch-matched style. In a pixel pitch-matched integration approach the occupied area by the circuitry is completely covered by the transducer area, with which the interconnections between pMUT and electronic are shortened, resulting in a reduction of the parasitic elements and the fabrication cost. The pixel pitch-matched style becomes more important when array configuration is employed, where the number of interconnection are increased, and the area must be minimized. The majority of our pMUTs have square form with sides of 40μm and 80μm, which demands that the area of the LNA must be smaller than 0.0016 mm^2.

- Bandwidth

  For our pMUT transducers, the frequency band of interest is from 1 MHz to 12 MHz. Considering this, the combination of LNA and VGA amplifiers should be designed in such a way that the Gain-Bandwidth product (GBW) will be much higher than 12 MHz.

- Interface single-ended.

  From the electrical circuit model for pMUT as a sensor represented in Fig 3.1b, it can be seen that the pMUT sensor has a single-ended nature. Taking into account this, an implementation of a single-ended amplifier could be an alternative to a differential amplifier, which will result in a reduction of power consumption and area.

- Gain and linearity.

  The expected input signal range is strongly dependent of the amount emitted acoustic pressure, the measurement target distance, and the number of the receive pMUTs connected at the LNA input. Considering the characteristics of our pMUTs, we will expect an input signal

range from hundreds of pArms to tens of nArms.

3.3 LNA Architectures

In most ultrasound systems the low-noise amplifier (LNA) is the functional block that directly interfaces with the transducer. The LNA must present high gain in order to amplify the weak signal sensed by the transducer above the noise of the successive analog processing circuits. The choices of the LNA architecture demands a trade-off between noise level, power consumption and area, and a depth knowledge of transducer characteristics. Depending on the impedance characteristics of the transducer, the LNA can be realized as: a Voltage Amplifier (VA) [26], [32], [52], [115], [116], a Transimpedance Amplifier (TIA) [16], [25], [51], [74], [88], [90], [93], [102], [117], a Transconductance Amplifier (TCA) [5], and a Current Amplifier (CA) [28], [118]. The VA and TCA are used to interface with low impedance transducers, and therefore, sense the transducer's voltage creating a high input impedance. In contrast, TIA and CA are adopted for high impedance transducers, with which they sense the transducer's current by establishing a low input impedance.

Regardless of which topology is selected, the LNA can be implemented as a single-ended or differential amplifier, or using open-loop or closed-loop structures. For example, *K. Chen et al.*, have implemented a LNA using VA topology to interface with bulk PZT transducers, which present a couple of kΩs

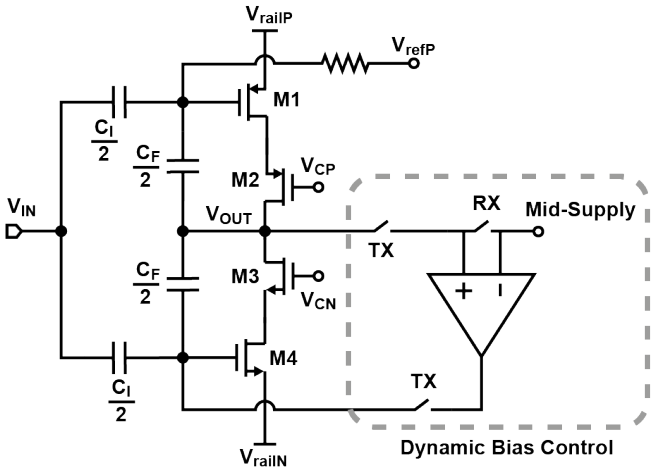


Figure 3.2: Simplified schematic of the LNA proposed in [115].

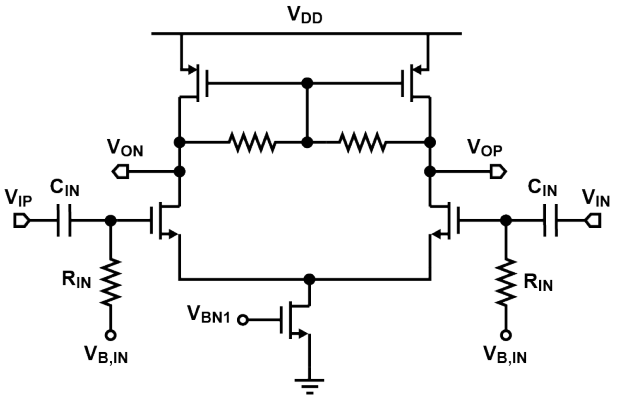


Figure 3.3: Schematic circuit of the LNA proposed in [116].

of electrical impedance around its resonance frequency [115]. The simplified schematic circuit of the proposed LNA in [115] is shown in Fig 3.2. The circuit uses a closed-loop single-ended approach, where a current-reuse cascoded CMOS inverter is used to optimize the power efficiency of the LNA. Due to the voltage gates of the M1 and M4 transistors experience a virtual ground, the mid-band voltage gain of this circuit is approximately C_I/C_F. Also, in order to maximize the output swing, the circuit shown in Fig 3.2 is properly biased using a dynamic DC bias control circuit to bias the output at mid-supply.

Another example of LNA implementation using VA topology, to interface with ultrasound transducers is shown in Fig 3.3. This circuit was proposed by [26], [116], and consists of a fully differential open-loop amplifier. The circuit was designed to interface with pMUTs transducers, which present an electrical impedance of $3.87k\Omega||15.4pF$ around their resonance frequencies [26]. The open-loop voltage gain is $gmN \cdot (roN||roP)$, where gmN is the nMOS differential pair transconductance, roN and roP are the output resistance of the nMOS differential pair and the pMOS current-source loads, respectively. The circuit was designed to obtain around 20 dB of DC gain [26].

As mentioned above, a transconductance amplifier (TCA) can also be used to interface with low impedance transducers. Figure 3.4 illustrates the implementation of a LNA based on TCA topology to amplify the siganl generated by pMUT transducers [5]. The proposed circuit is based on open-loop differential amplifier, where the nMOS and pMOS differential pair is biased in weak inversion to reduce the power consumption [5]. pMOS M5 and M6 transistors are used to implement the common-mode feedback. The switches S_{pwr} and

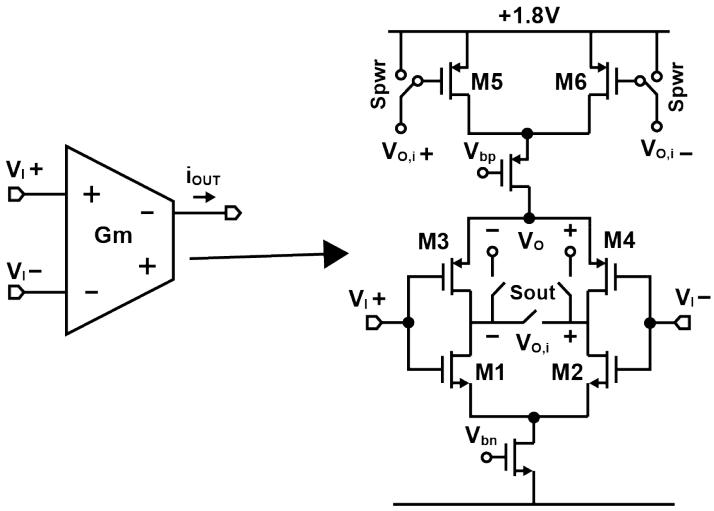


Figure 3.4: LNA implementation using TCA topology. Circuit proposed in [5].

S_{out} are used to disconnect and power down the TCA cell from the rest of the front-end circuitry when it is not used.

Usually, when the electrical impedance of the transducers is higher than 10 kΩ, is more efficient to amplify current instead of voltage signals [36]. Aforementioned, when in receive mode the transducer is considered a current signal source, the most power-efficient LNA topologies to interface with it are transimpedance (TIA) and current (CA) amplifiers. The most used TIA configurations are: based on resistive feedback [51], [74], [88], [93], [117], and based on capacitive feedback [16], [25], [90], [102].

Figure 3.5 shows a general scheme of a TIA amplifier based on resistive feed-

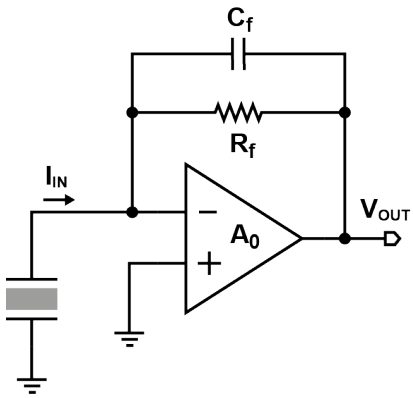


Figure 3.5: General architecture of a TIA based on resistive feedback.

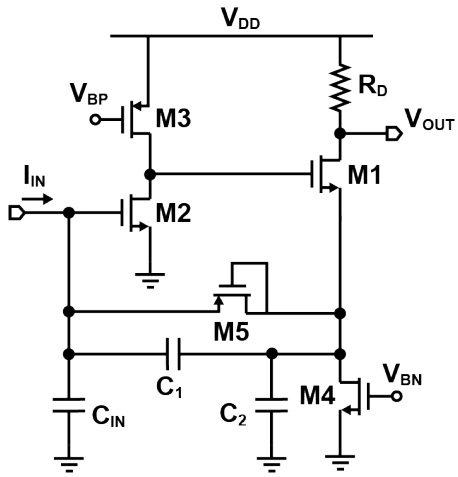


Figure 3.6: Implementation of a capacitive-feedback TIA proposed by [90].

back. Usually, this LNA topology adopt a closed-loop configuration with a negative feedback network formed by R_f and C_f. The resistor R_f defines the transimpedance gain, while the capacitor C_f is used to set the -3dB bandwidth and improves the stability. Although the amplifier A_0 in Fig 3.5 corresponds to a differential amplifier, it can also be implemented as a single-ended configuration [88], [93]. *K. Chen et al.* have implemented a TIA based on resistive feedback to interface with cMUTs transducers, which consists of a two stage operational amplifier (Op-Amp) followed by an output buffer [51]. The Op-Amp was implemented with a nMOS differential pair and a current mirror as load, followed by the Miller compensation stage. A similar circuit was proposed in [74], but they use a pMOS differential pair instead of the nMOS.

The main drawback to implement an LNA using resistive-feedback TIA approach, is that the feedback resistor adds thermal noise to the system. In order to optimize the noise performance in TIA amplifiers, the capacitive feedback approach is implemented. Figure 3.6 illustrates a typical implementation of a TIA based on capacitive feedback. The circuit was proposed by [90], and was designed to interface with cMUT transducers. The circuit consists of a closed-loop single-ended amplifier with shunt-series negative feedback topology. The single-ended amplifier is implemented in two stage, where the first one is a common-source amplifier with a current source as load, while the second stage is a source follower amplifier. To complete the transimpedance operation, the output current is passed through the resistor R_D. If the DC voltage gain (A_0)

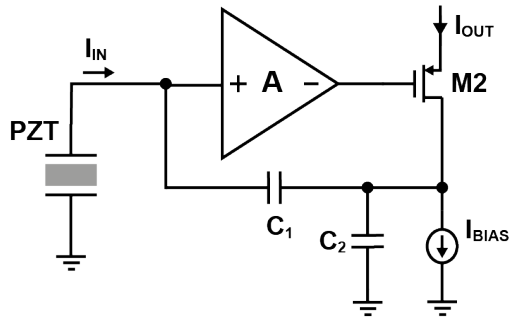


Figure 3.7: Simplified schematic circuit of the LNA proposed by [118]. The circuit is based on CA topology.

of the single-ended amplifier is much higher than 1, and $A_0 \cdot C_1 >> C_{in} + C_1$, the DC TIA gain of the circuit shown in Fig 3.6 is $\approx (1 + C_2/C_1) \cdot R_D$.

Current amplifiers (CA) are another LNA topology used to interface with high impedance transducers. In [118] have implemented a CA circuit to amplify the signal generated by PZT ultrasound transducer. A simplified schematic circuit of the CA proposed by [118] is shown in Fig 3.7. The core amplifier A is implemented in two common source stages with current sources as loads. If the input node does not change, it is considered an AC ground, and therefore the current gain $I_{OUT}/I_{IN} \approx 1 + C_2/C_1$.

3.4 Circuit Implementation

In this section, two LNA topologies are presented. The first one is a Voltage Amplifier (VA) where the input voltage signal is generated from the integration of the pMUT's short-circuit current (I_{PMUT}) on the input node. The second one is a Transimpedance Amplifier (TIA) based on capacitive feedback. Both of them were implemented in 0.13 μm HV CMOS technology from Silterra, with 1.5 V power supplied voltage. Moreover, both implementations were designed to achieve the target specifications mentioned in Section 1.2.

3.4.1 LNA Voltage Amplifier

In order to minimize the power consumption and area, the CMOS inverter is chosen to implement the main core of the VA circuit. Fig 3.8 shows the electrical scheme of the designed VA. It is an open-loop structure, based on

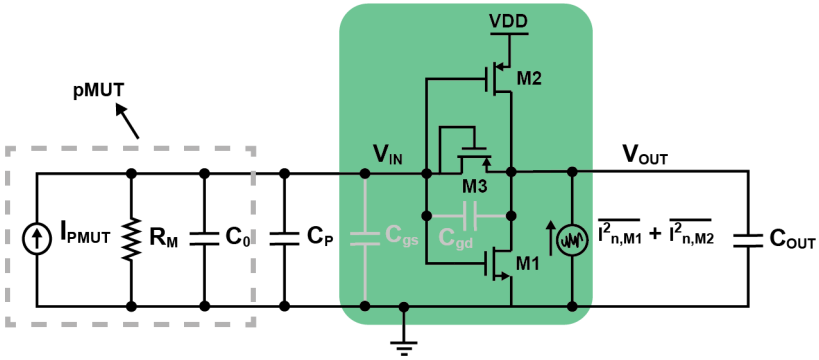


Figure 3.8: Schematic of the proposed Voltage Amplifier (VA) for pMUT transducers.

a single-ended input self-biased push-pull configuration. In order to bias the nMOS and pMOS transistors in their optimal operation region, the input and output of amplifier are connected through a large feedback resistor. In order to reduce noise, this feedback resistor is implemented by a pMOS transistor operating in the sub-threshold region, which works as a very high impedance resistance settling the DC bias input and output voltage to the mid-supply [119]. The main advantage of this implementation is that it does not need of a bias circuit, which can occupy a large silicon area. In contrast to this advantage, the circuit suffers from a poor power supply rejection ratio (PSRR), although some techniques to improve the PSRR in inverter-based amplifiers have been demonstrated [115], [120].

The transfer functions between the output voltage, V_{out} and the input voltage V_{in}, and between the V_{out} and the short-circuit pMUT's current, in Laplace domain, can be obtained by equations 3.1 and 3.2, respectively:

$$\frac{V_{out}(s)}{V_{in}(s)} = \frac{-(gm_{M1}+gm_{M2})(1-\dfrac{sC_{gd}}{gm_{M1}+gm_{M2}})}{(gds_{M1}+gds_{M2})(1+\dfrac{s(C_{gd}+C_{out})}{gds_{M1}+gds_{M2}})} \tag{3.1}$$

$$\frac{V_{out}(s)}{I_{PMUT}(s)} = \frac{-A_0\cdot(1-\dfrac{sC_{gd}}{gm_{M1}+gm_{M2}})}{s(C_{eq}+A_0C_{gd})\cdot[1+\dfrac{s(C_{eq}C_{out}+C_{eq}C_{gd}+C_{out}C_{gd})}{(gds_{M1}+gds_{M2})(C_{eq}+A_0C_{gd})}]} \tag{3.2}$$

where $A_0 = (gm_{M1}+gm_{M2})/(gds_{M1}+gds_{M2})$ is the DC voltage gain, gm

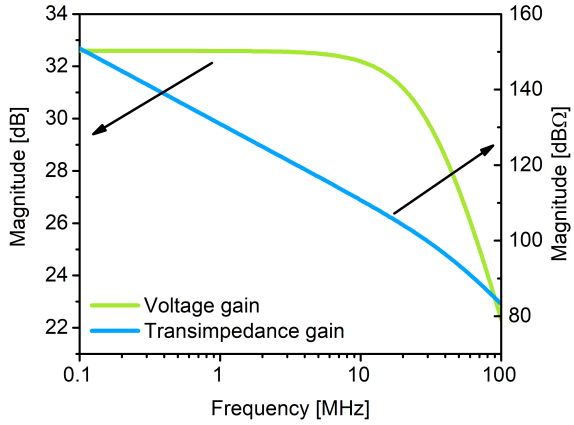


Figure 3.9: Frequency response of the simulated voltage and transimpedance gain functions of the implemented VA.

and *gds* are the transconductance and the output conductance of the M1 and M2 transistors, $C_{eq} = C_0 + C_p + C_{gs}$ is the equivalent capacitance given by the parallel connection of electrical capacitance of the pMUT (C_0), the parasitic capacitance (C_p), and the gate-source capacitance (C_{gs}) of the M1 and M2 transistors, C_{gd} is the gate-drain capacitance of the M1 and M2 transistors, C_{out} is the equivalent capacitance from the output node to ground, which can be computed by adding the bulk-drain capacitance (C_{bd}) of M1 and M2 transistors and the input capacitance of the succeeding circuit.

If the pMUT's noise is ignored by simplicity, the input-referred current noise of the designed VA amplifier can be obtained as following:

$$\overline{i_{n,in}^2} \approx (\overline{i_{n,M1}^2} + \overline{i_{n,M2}^2}) \cdot \left| \frac{s(C_0 + C_p + C_{gs})}{gm_{M1} + gm_{M2}} \right|^2 \tag{3.3}$$

where $\overline{i_{n,M1}^2}$ and $\overline{i_{n,M2}^2}$ are the mean-square current-noise sources for M1 and M2 transistors respectively.

Considering the equations 3.1, 3.2, and 3.3, the transistors were dimensioned in a proper form in order to achieve a trade-off between power consumption, noise performance, area, and gain. Table 3.1 summarizes the electrical characteristics of the proposed VA circuit. Figure 3.9 shows the simulated transfer functions of the implemented circuit considering $C_0 = 300fF$, $C_p = 1pF$, and $C_{out} = 500fF$. The simulated DC voltage gain is $A_0 = 32.5$ dB and the -3 dB bandwidth is around 32 MHz. The simulated transimpedance gain is 121 dBΩ

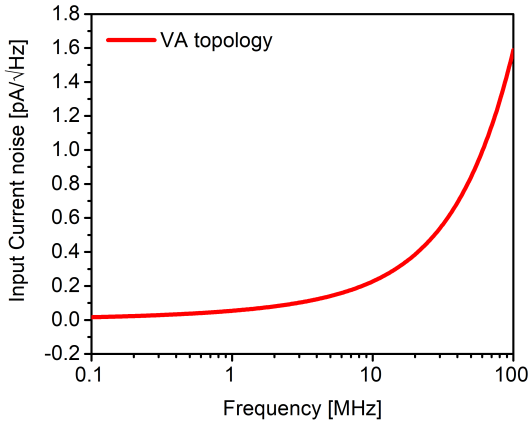


Figure 3.10: Simulated input-referred current noise of the implemented VA.

Table 3.1: Summary of the VA electrical parameters

Parameter	Value
W1/L1 (μm/μm)	10/0.22
W2/L2 (μm/μm)	25/0.22
W3/L3 (μm/μm)	0.2/0.2
Supply Voltage (V)	1.5
I_{BIAS} (μA)	200
C_{gd} (fF)	19
C_{gs} (fF)	63
DC Voltage Gain (dB)	32.5
TIA Gain (dBΩ)	121 @ 3MHz
Bandwidth (MHz)	32
Input referred noise ($pA/\sqrt{Hz}$)	0.1 @ 3 MHz
Area ($10^{-4}mm^2$)	6

at 3 MHz.

Figure 3.10 illustrates the simulated input-referred current noise of the designed VA. For the values of C_0, C_p, and C_{out} mentioned above, the simulated input-referred current noise density is 0.1 pA/$\sqrt{Hz}$ at 3 MHz.

3.4.2 LNA Transimpedance Amplifier

The second approach of LNA circuit designed in this thesis was a transimpedance amplifier (TIA) based on capacitive feedback. A general scheme of a TIA based on capacitive feedback, when is connected to the simplified electrical model of the pMUT, illustrated in Fig 3.1b, is shown in Fig 3.11. Considering that, the motion resistance of the pMUT (R_M) is much higher

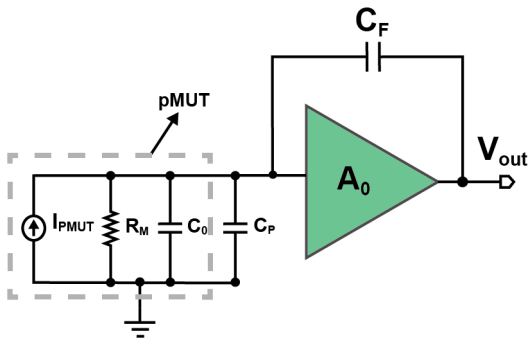


Figure 3.11: General electric scheme of a TIA based on capacitive feedback coupled to a pMUT device.

than the impedance of $C_0 + C_p + C_{in}$ at resonance frequency of the pMUT, the transimpedance gain can be defined as following:

$$\frac{V_{out}(s)}{I_{PMUT}(s)} \approx \frac{-A_0}{s(C_0 + C_P + A_0 C_F)} \tag{3.4}$$

where A_0 is the open loop gain of the core amplifier, and C_F is the feedback capacitance. From this equation can be seen that if $A_0 C_F \gg C_0 + C_p$, the transimpedance gain will be $\approx -1/sC_F$, being independent of the electrical capacitance of the pMUT (C_0) and the parasitic capacitance (C_p). To achieve this, it is required to design a capacitive feedback TIA circuit with high open-loop gain ($A0$), and high feedback capacitor (C_F). However, a high open-loop voltage gain increases the power consumption, while a high feedback capacitor causes a decrease of the transimpedance gain, and occupies a large silicon area. Taking into account this, a trade-off between power consumption, gain, and area is needed.

A good candidate to implement the open-loop voltage amplifier is the same single-ended input self-biased push-pull configuration designed for VA topology. It achieves a high open-loop gain with reduced dimensions and low power consumption. Figure 3.12 shows an schematic of the designed capacitive feedback TIA circuit. The transimpedance gain function of the pMUT/TIA combination can be computed as following:

$$\frac{V_{out}(s)}{I_{PMUT}(s)} = \frac{-A_0 \cdot (1 - \dfrac{sC_F}{gm_{M1} + gm_{M2}})}{s(C_{eq} + A_0 C_F) \cdot \left[1 + \dfrac{s(C_{eq}C_{out} + C_{eq}C_F + C_{out}C_F)}{(gds_{M1} + gds_{M2})(C_{eq} + A_0 C_F)}\right]} \tag{3.5}$$

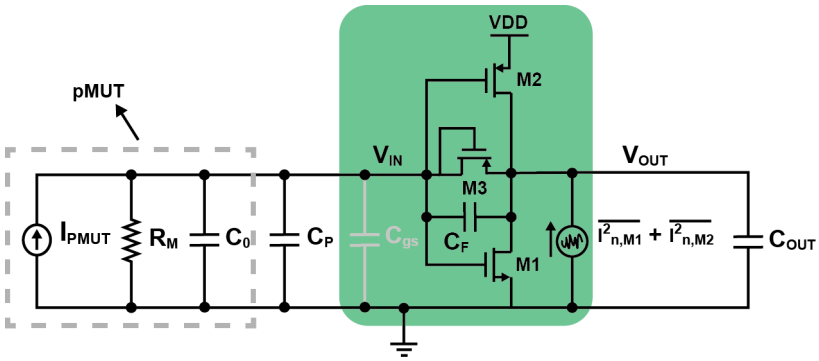


Figure 3.12: Schematic of the proposed Transimpedance amplifier (TIA) for pMUT transducers.

where C_F is the feedback capacitance and the rest of parameters keep the same definition used in Eq 3.2. Considering that $A_0 C_F \gg C_{eq}$, Eq 3.5 is reduced to:

$$\frac{V_{out}(s)}{I_{PMUT}(s)} \approx \frac{-1 \cdot (1 - \dfrac{sC_F}{gm_{M1} + gm_{M2}})}{sC_F \left[1 + \dfrac{s(C_{eq}C_{out} + C_{eq}C_F + C_{out}C_F)}{(gm_{M1} + gm_{M2})C_F)}\right]} \tag{3.6}$$

Assuming that the right half-plane zero is much larger than the operation range frequencies of our pMUTs, the input-referred current noise of the designed TIA amplifier can be obtained, ignoring the pMUT's noise for simplicity, as following:

$$\overline{i^2_{n,in}} \approx (\overline{i^2_{n,M1}} + \overline{i^2_{n,M2}}) \cdot \left| \frac{s(C_{eq} + C_F)}{gm_{M1} + gm_{M2}} \right|^2 \tag{3.7}$$

From equations 3.6 and 3.7 we can see that small feedback capacitance (C_F) is a benefit to both TIA gain and input-referred current noise. However, small C_F causes an increase of the input impedance ($\sim 1/s(1 + A_0 C_F)$), and as consequence a reduction in effectiveness of the TIA amplifier. Considering this, the chosen C_F value was done guaranteeing at least 85% of charge transfer from the short-circuit pMUT's current source to the feedback capacitance's current. Figure 3.13a illustrates the charge transfer percent ($I_{C_F}/I_{PMUT} \cdot 100$) for different values of C_F, and considering $C_0 = 300fF$ and $C_p = 1pF$. It can be seen, for C_F higher than 400 fF, at least 85% of charge transfer is guaranteed. Therefore, in order to maximize the transimpedance gain and reduce

Table 3.2: Summary of the TIA electrical parameters

Parameter	Value
W1/L1 (μm/μm)	10/0.22
W2/L2 (μm/μm)	25/0.22
W3/L3 (μm/μm)	7.5/0.22
Supply Voltage (V)	1.5
I_{BIAS} (μA)	200
C_F (fF)	411
C_{gd} (fF)	19
C_{gs} (fF)	63
TIA Gain (dBΩ)	100.8 @ 3 MHz
Input referred noise (pA/$\sqrt{HZ}$)	0.14 @ 3 MHz
Area ($10^{-4}mm^2$)	9

the input noise and area, 400 fF was selected as feedback capacitance. The C_F capacitor was implemented using interdigitated fingers, achieving a final value of 411 fF. Figure 3.13b shows the charge transfer as a function of the parasitic capacitance, taking into account the chosen C_F.

On the other hand, since the feedback capacitance is much higher than the gate-to-drain capacitance of the M1 and M2 transistors, the bias resistor implemented by M3 was reduced to avoid any leakage current that could charge C_F, without affecting the operation point of the M1 and M2. Table 3.2 summarizes the electrical characteristics of the TIA amplifier based on capacitive feedback.

Figure 3.14 shows the transimpedance gain (V_{out} versus short-circuit

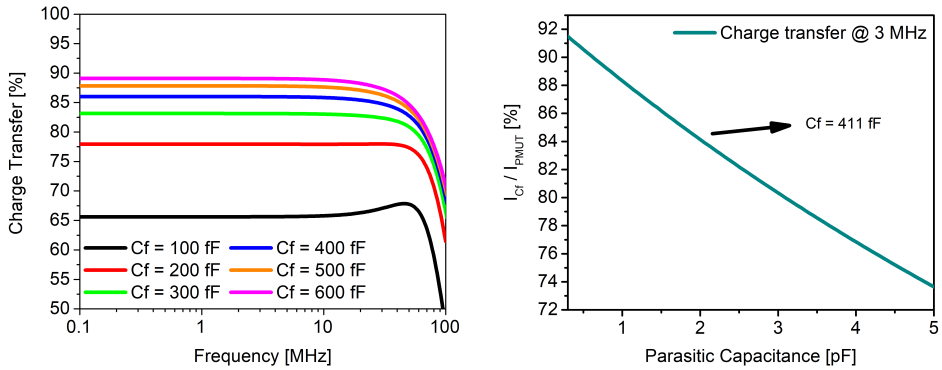


Figure 3.13: Simulated charge transfer for: (a) different feedback capacitance C_F, (b) different parasitic capacitance C_P at 3 MHz and $C_F = 411fF$.

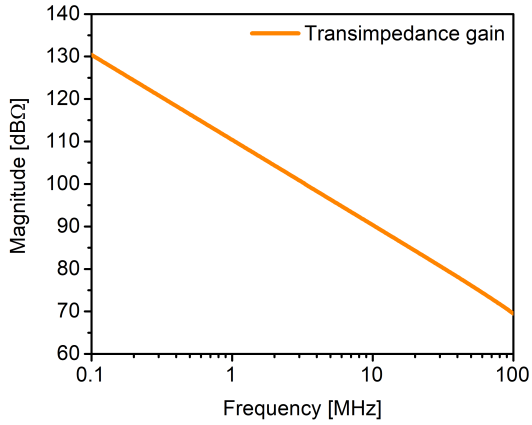


Figure 3.14: Simulated frequency response of the transimpedance amplifier (TIA) based on capacitive feedback.

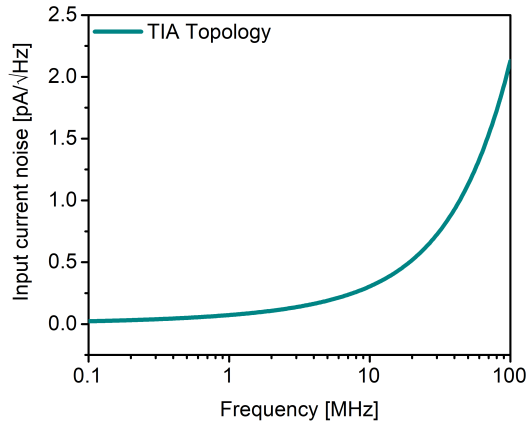


Figure 3.15: Simulated input-referred current noise of the implemented TIA.

pMUT's current source) of the designed TIA. As can be seen it has a capacitive impedance behavior, with a capacitance value of 483 fF. The designed feedback capacitance ($C_F = 411fF$) is around a 0.85 factor lower than this value, which translates to 85% of the short-circuit pMUT's current will be convert to voltage through C_F, being in agreement with the results plotted in Fig 3.13. At 3 MHz, the simulated transimpedance gain was 100.8 dBΩ.

Figure 3.15 illustrates the input-referred current noise density referenced to the short-circuit pMUT's current. For the assumed values of C_0, C_p, and C_{out}, the simulated input-referred current noise density is 0.14 pA/$\sqrt{Hz}$ at 3 MHz.

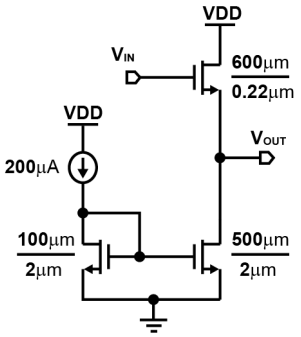
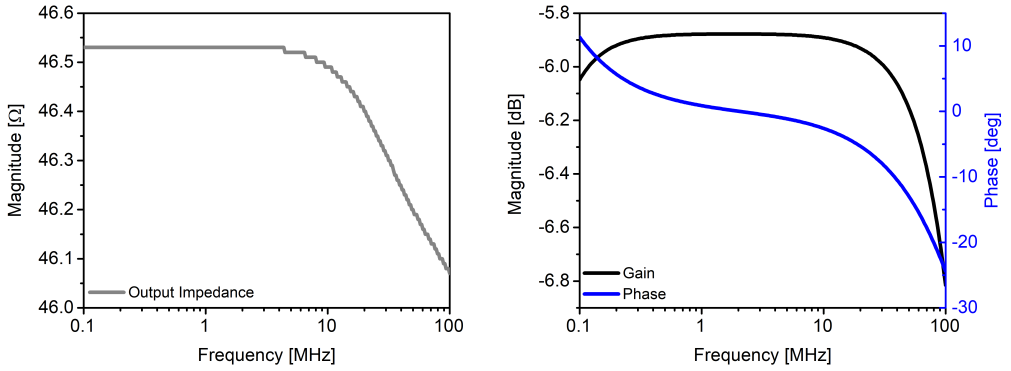


Figure 3.16: 50Ω Output Buffer designed for testing purposes.

3.5 50 Ω Output Buffer

In order to test the two designed LNA circuits, an output buffer stage has been designed. The main proposes of this circuit is to drive 50 Ω input impedance of the Radio-frequency (RF) measurement instruments (network analyzer, spectrum analyzer, oscilloscope). Figure 3.16 shows the schematic of the proposed output buffer circuit. It is based in a source follower amplifier with a current mirror as load. In order to guarantee maximum power transfer, the output buffer was designed to obtain around 50 Ω of output resistance.

Figure 3.17a represents the magnitude of the output impedance of the designed output buffer. It can be seen that at low frequency it has a resistive behavior with a value of 46.5 Ω, which is very close to 50 Ω. Figure 3.17b shows the frequency response of the designed output buffer when drives 50 Ω



(a) (b)

Figure 3.17: (a) Magnitude of the output impedance of the designed output buffer, (b) magnitude and phase of its transfer function.

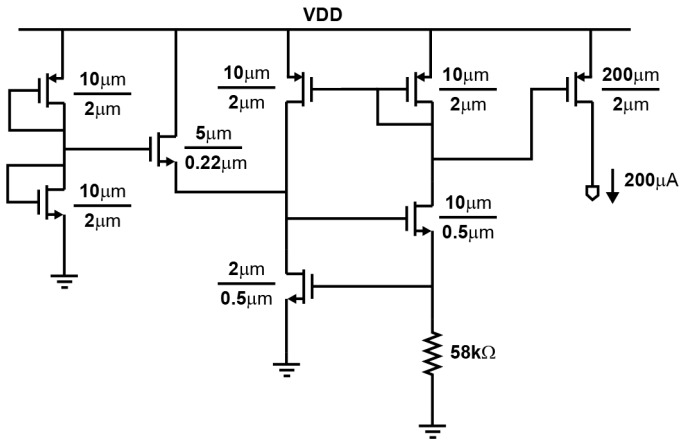


Figure 3.18: Schematic circuit of the 200μA I_{BIAS} current.

in parallel to 30 pF. As it was expected, at the frequencies of interest, the attenuation is around 6 dB, and the introduced phase shift is negligible.

The schematic of the designed 200 μA bias current is shown in Fig 3.18. It is based on a self-biased current reference with the start-up circuit. The resistor of 58 kΩ was implemented in Low-Voltage P-Well in order to optimize area.

3.6 Experimental results

Both TIAs were fabricated using a High Voltage (HV) 0.13 μm CMOS technology from Silterra. The presence of HV is because the transmitter circuit was fabricated in conjunction with the low-voltage (LV) RX amplifiers. Figure 3.19a and b present a micro-photograph and the layout view of the VA and TIA respectively. As can be seen the majority area is occupied by the output buffer (163μm x 50μm), while the VA and TIA occupy only an area of 23μm x 25μm and 28μm x 53μm respectively. The RX amplifiers were characterized in terms of transfer function, noise performance and 1-dB compression point. In order to carry out the measurements, both chips were wire bonded to a printed circuit board (PCB), where the estimated parasitic capacitance due to connectors and routing was 2.3 pF (extracted from COMSOL Multiphysic Software).

Figure 3.20 shows the measured as well as the post-layout simulation results voltage-voltage transfer function of the VA with a comparison to post-layout simulation results. The measured -3 dB bandwidth is around 22 MHz, and

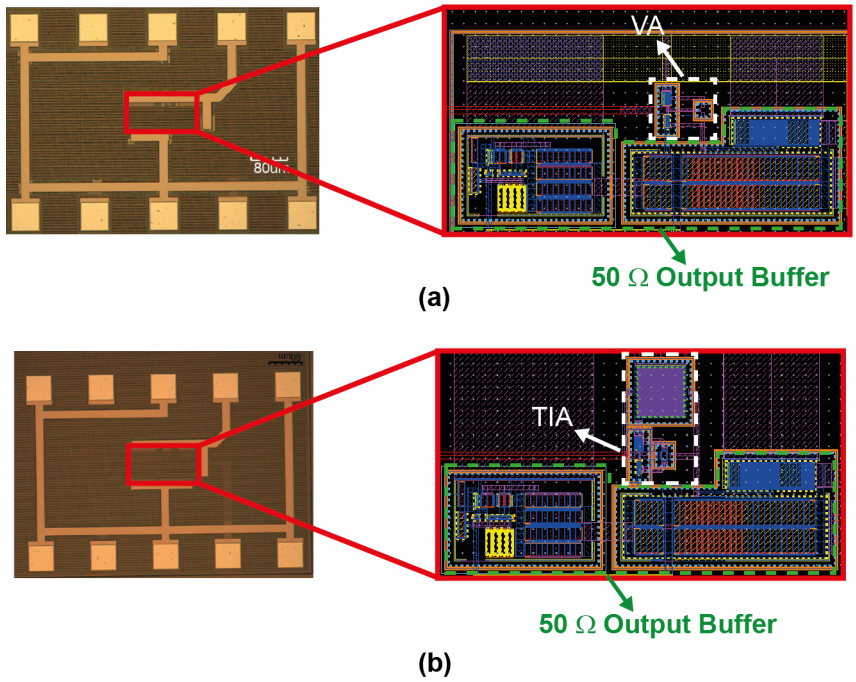


Figure 3.19: Photograph and layout of the chip. (a) Voltage amplifier (VA) with output buffer, and (b) Transimpedance amplifier with output buffer.

the measured DC gain is around 25 dB, which is 7.5 dB lower than the the designed gain (A_0) mainly due to attenuation of the output buffer (∼6 dB) when is loaded with 50 Ω resistor.

To measure the transfer function of the TIA based on capacitive feedback, it was operated in charge amplifier mode instead of current mode. In charge

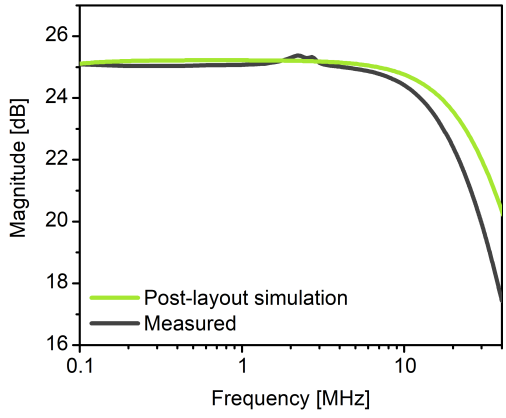
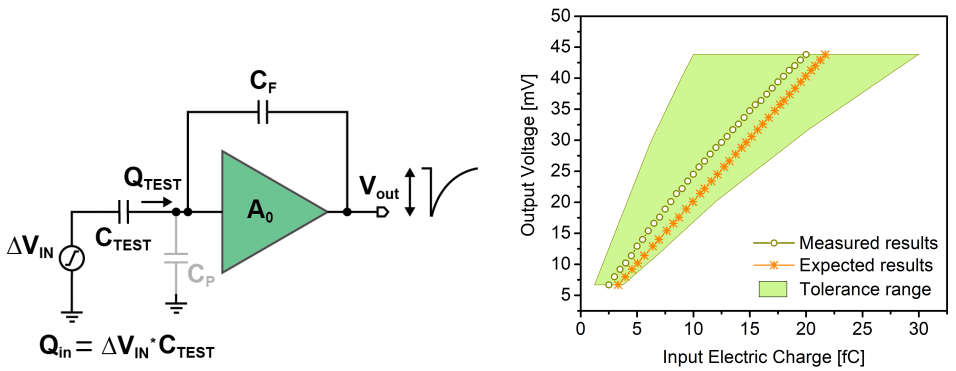


Figure 3.20: Measured Voltage-Voltage transfer function of the VA.

amplifier mode, the transfer function of the TIA can be measured by injecting electric charge at the TIA input and measuring the amplitude of the output voltage, which are related by the following equation, assuming that the total electric charge (Q_{TEST}) is fed into the TIA input:

$$V_{out} = \frac{Q_{TEST}}{C_F} \tag{3.8}$$

As explained above, if the total parasitic capacitance is comparable with the input capacitance of the TIA, only a fraction of the total electric charge will be convert to voltage through the feedback capacitance C_F. To generate the electric charge (Q_{TEST}) we apply small voltage steps to a test injection capacitor (C_{TEST}). Figure 3.21a illustrates the schematic diagram of the experimental setup used to test the TIA in charge amplifier mode. A 100 fF capacitor connected in series to the input was used as a test injection capacitor (C_{TEST}). Small voltage steps (ΔV_{IN}) were applied to C_{TEST}, which generated electric charges at the TIA input with values of $C_{TEST} * \Delta V_{IN}$. In this experiment we changed the amplitude of the voltage steps from 25 mV to 200 mV, which generated an electric charge from 2.5 fC to 20 fC. Figure 3.21b shows the measured output voltage after correcting the attenuation added by the output buffer (i.e the measured output voltage was multiplied by 2, assuming that the attenuation of the output buffer is around 6 dB when 50 Ω resistor is connected as load). Taking into account that the injection capacitor has a tolerance of ±50



(a) (b)

Figure 3.21: (a) Schematic diagram of the experimental set-up to measure the transfer function of the TIA in charge amplifier mode, and (b) measured transfer function of the TIA in charge mode amplifier.

fF, the injected charge at TIA input has a tolerance range of $\pm\Delta V_{IN} \cdot 50fF$. This tolerance range is illustrated in Fig 3.21b by the color filled polygon.

In order to validate the good performance of the TIA amplifier, we have graphed the expected results in conjunction of the measured ones and its tolerance range. The expected results were extracted assuming that the measured output voltages were obtained considering that a 83% of charge transfer occurs (from Fig 3.13b, being $C_P = 2.3pF$ and $C_F = 411fF$). As shown in Fig 3.21b, the expected results are inside of the tolerance range, and very close to the measured results, which demonstrates the good performance of the TIA amplifier based on capacitive feedback.

The noise performance of both, the VA and TIA amplifiers, was measured by opening the input and measuring the output noise. Figure 3.22a shows the measured output-referred voltage noise density for both RX amplifiers, with a comparison to post-layout simulation results, considering 2.3 pF of parasitic capacitance. The presence of the spikes is due to the power supply noise, which validates that the main disadvantage of these amplifiers is its poor PSRR. The input current noise was computed by dividing the measured output noise by their corresponding transfer functions. The resulting input-referred current noise densities are shown in Fig 3.22b, which are in good agreement with the post-layout simulation results. Also, these results are in agreement with Eqs 3.3 and 3.7, where is demonstrated that the VA is more noise-efficient than the TIA amplifier. The measured output-referred voltage noise density was 60.68 nV/$\sqrt{Hz}$ and 19.01 nV/$\sqrt{Hz}$ at 3 MHz for the VA and TIA amplifiers, respectively. At the same frequency, the measured input-referred current noise densities are 0.18 pA/$\sqrt{Hz}$ and 0.34 pA/$\sqrt{Hz}$ for the VA and TIA, respectively. From these results, the integrated input noise currents across the pMUT bandwidth (∼1 MHz in liquid) are 180 pArms and 340 pArms for VA and TIA respectively.

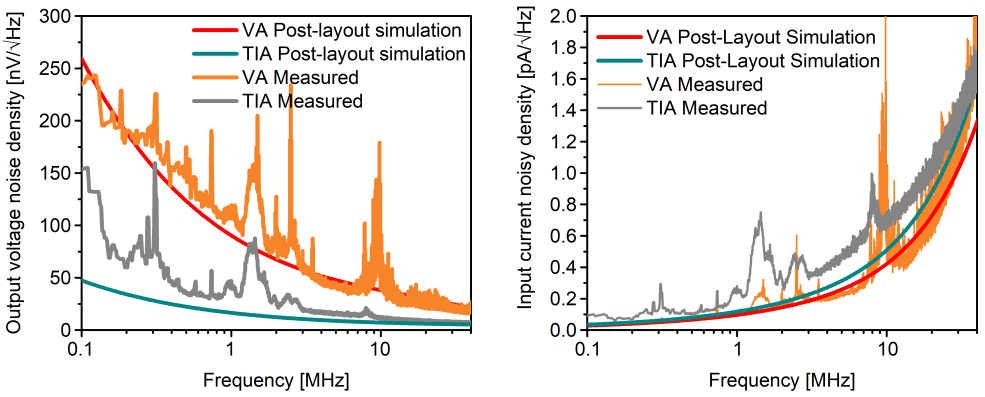
Figure 3.23 shows the post-layout simulations and the measurements of the VA and TIA output voltages for different input current levels at 3 MHz. The measured transimpedance gain was 106 dBΩ and 93 dBΩ, respectively. The maximum input currents are measured as 130.5 nArms and 652 nArms at the 1 dB compression point for VA and TIA respectively. These values are mainly limited by the source follower output buffer when is loaded with 50 Ω resistor.

To quantify the performance of the designed RX amplifiers, we have defined two Figure-of-Merit (FoM). The first one, defined as FOM_{RX1}, is used to quantify the voltage amplifier topologies, while the second one (FOM_{RX2}) is used for transimpedance amplifier approaches. They are defined as following:

$$FOM_{RX1}[\frac{MHz}{V^2 \cdot A \cdot \mu m^2}] = \frac{Gain_{VA}(V/V) \cdot \sqrt{BW_{transducer}(MHz)}}{v_{n,in}(nV/\sqrt{Hz}) \cdot P_{VA}(mW) \cdot \text{Area } (mm^2)} \quad (3.9)$$

$$FOM_{RX2}[\frac{Hz}{mA^3 \cdot \mu m^2}] = \frac{Gain_{TIA}(V/A) \cdot \sqrt{BW_{transducer}(MHz)}}{i_{n,in}(pA/\sqrt{Hz}) \cdot P_{TIA}(mW) \cdot \text{Area } (mm^2)} \quad (3.10)$$

where $Gain_{VA}$ and $Gain_{TIA}$ are the voltage and transimpedance gains at low frequencies, $BW_{transducer}$ is the transducer bandwidth, $v_{n,in}$ and $i_{n,in}$ are the input-referred voltage and current noise densities respectively, P_{VA} and P_{TIA} are the power consumption for VA and TIA circuits respectively. Table 3.3 summarizes the comparisons between the performance of the designed LNAs and that of the other amplifiers reported as being state-of-the-art, demonstrating competitive results. Taking the best computed $FOM_{RX1,2}$, the designed VA and TIA topologies achieve ∼4.38x and ∼5.5x higher improvement, respectively, guaranteeing the best electrical performance with a minimum area. These competitive FOM values are possible since the proposed LNAs have a smaller area (almost by 10 times), which makes these designs good candidates to implement a pitch-matched system, where the LNA can be implemented



(a) (b)

Figure 3.22: Measured and post-layout simulated spectral noise density for both VA and TIA. (a)Output-referred voltage noise density, and (b) Input-referred current noise density.

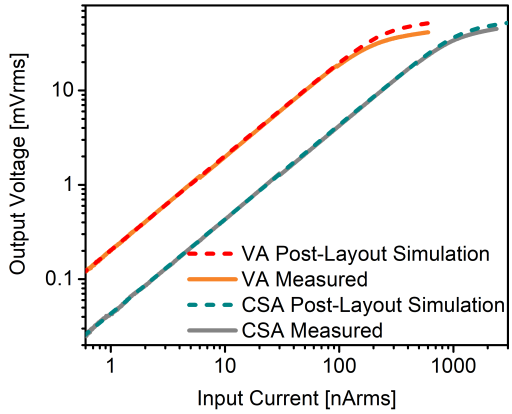


Figure 3.23: Post-layout simulation and measured 1-dB compression point for both VA and TIA at 3 MHz.

just below its ultrasound transducer.

3.7 Conclusions

Two compact LNA topologies for pMUT transducers have been presented. The first one is a single-ended open-loop voltage amplifier, while the second one is a transimpedance amplifier based on capacitive feedback. A single-ended input self-biased push-pull configuration is employed to implement the open-loop amplifier for both topologies. Both proposed of LNA architectures were electrically characterized, where the VA amplifier provided a remarkable improvement in terms of transimpedance gain and input-referred noise with the same power consumption, demonstrating that is more noise-efficient than the proposed TIA. Nevertheless, the great dependency of the VA gain on the parasitic capacitance means that the TIA is the more useful option when the amplifier is not fully integrated with the pMUTs, since all of the parasitic capacitance are difficult to efficiently control, providing different gains for the same devices. The VA is more adequate when the amplifier can be directly connected to the sensor, as happens when there is a monolithic integration of the CMOS and pMUTs.

Table 3.3: Measured LNA performance summary and comparisons.

	This Work		**[116] (2019)**	**[52] (2018)**	**[74] (2016)**	**[5] (2015)**	**[115] (2015)**
Topology	VA	TIA	VA	VA	TIA	TCA	VA
Process technology	0.13μm HV CMOS	0.13μm HV CMOS	0.18μm CMOS	0.18μm HV-BCD	TSMC 0.18μm HV CMOS	0.18μm HV CMOS	0.18μm HV CMOS
Transducer	pMUT	pMUT	pMUT	PZT	cMUT	pMUT	PZT
Power Supply [V]	1.5	1.5	1.5	1.8	1.8	1.8	1.8
Power consumption [mW]	0.3	0.3	0.08	0.79	1.4	N/A	0.135
Area [$10^{-4}mm^2$]	6	9	N/A	30[1]	280	310	60
Voltage-voltage gain [dB]	25	N/A	29/30/ 42/53[2]	18	N/A	N/A	-12/6/ 24
Transimpedance gain [dBΩ]	106 at 3 MHz	93 at 3 MHz	N/A	N/A	116/113.5/ 110/104	N/A	N/A
Bandwidth [MHz]	22	N/A	10	20	10.2/10.8/ 10.6/10.5	N/A	N/A
Input current noise [pA/$\sqrt{Hz}$]	0.18 at 3 MHz	0.34 at 3 MHz	N/A	N/A	0.41 at 5 MHz	N/A	N/A
Input voltage noise [nV/$\sqrt{Hz}$]	3.41 at 3 MHz	N/A	N/A	7.9 at 5 MHz	N/A	11 at 0.22 MHz	5.9 at 4 MHz
Input dynamic range [dB]	57	66	90	75	N/A	N/A	81
FOM_{RX_1} [$MHz/V^2A\mu m^2$]	29057	N/A	N/A	949	N/A	N/A	6633[3]
FOM_{RX_2} [$Hz/mA^3\mu m^2$]	N/A	0.5*10^9	N/A	N/A	0.09*10^9 [3]	N/A	N/A

[1] This area was estimated from a chip micrograph.
[2] Including a TGC amplifier as a second stage.
[3] Computed considering its higher gain.

3.8 Time Gain Compensation (TGC) Amplifier

The electrical signal produced by an ultrasound transducer in the receive mode has a certain intrinsic dynamic range. As was explained in Chapter 1, when the transmitted ultrasound signal is propagated in a media, and detects an abrupt change of acoustic impedance, the ultrasound signal is partially reflected and returns to the transducer in form of echos. Echo signals from deeper scatters take a longer time to arrive the transducer, and have lower amplitudes than the received from closer scatters, due to the propagation attenuation that experience the ultrasound signals [25]. As consequence, the dynamic range of

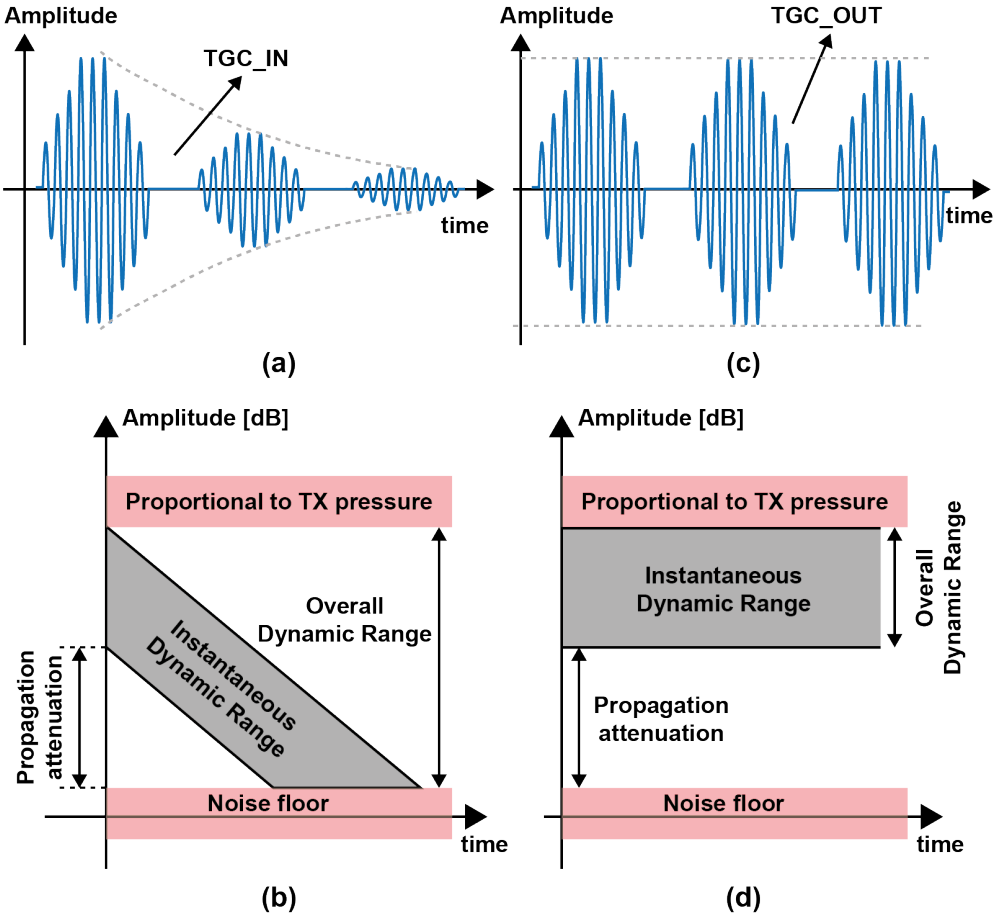


Figure 3.24: (a) and (b) Received signals and Dynamic range at TGC input, respectively, (c) and (d) Received signals and Dynamic range at ideal TGC output, respectively.

the transducer is time-dependent, where the upper bound is mainly related to the transmit acoustic pressure, while the lower bound is set by the transducer's noise.

Figure 3.24a shows the temporal diagram of the received echos from different depths and its corresponding dynamic range in Fig 3.24b. As can be shown, the amplitudes of the received echos have an exponential decay, which is translated to a linear decrease-in-dB with time, see Fig 3.24b. Also, it can be seen that the overall dynamic range of the electrical received signals on a transducer consists of two parts: the instantaneous dynamic range, which can be understood as the received-signal dynamic range at each imaging depth, and the dynamic range due to propagation attenuation [25]. Usually, the overall dynamic of

the echoes received by the transducer is very large, for example, in medical ultrasound imaging application, the overall dynamic range is in the order of 100 dB, causing strong echoes to appear as a bright spot while weak echoes manifest as an indistinguishable feature on the screen [121]. With a fixed-gain LNA, the overall dynamic range of the received echoes is unaltered, as long as the electronic noise of the LNA circuit is lower than the transducer's noise, with which is needed of a circuit that performs the time-gain compensation function. Such circuits are called in the literature as Time-Gain Compensation (TGC) Amplifier. Ideally, the TGC amplifier should provide a variable gain that increases linearly-in-dB with time in order to compensate the propagation attenuation, so that after compensation a uniform echo amplitudes across depth is provided and only the instantaneous dynamic range is remained, see Fig 3.24c and d. Since the main purpose of the TGC circuit is to compensate signal attenuation along the depth, the maximum gain of the TGC amplifier is limited by the total signal attenuation.

Depending on how the gain of the TGC amplifier is controlled, these circuits can be classified in two categories: Programmable Gain Amplifier (PGA) with discrete gain steps, and Variable Gain Amplifier (VGA) with continuous gain control [36].

A PGA circuit uses a series of switchable passive components networks, such as resistors [33], [122], or switches-capacitor techniques [123], [124] to approximate the exponentially varying gain with discrete gain steps, see Fig 3.25a. Moreover, the PGA gain steps can be divided across multiple amplifier stages, with coarse gain steps implemented in the LNA and the subsequent PGA realizes fine gain steps [124]. The main advantage to implement the TGC function with a PGA circuit is that their gain steps can be accurately set. In contrast, its main drawback is related to the appearance of switching artifacts in the ultrasound image associated with switching transients between gain steps [25].

A VGA circuit controlled by analog signal can be preferred for applications that require smooth gain transitions. Typically, the TGC function can be implemented with a VGA circuit by controlling the gain with analog voltage that changes linearly with time. An approach to implement a VGA is shown in Fig 3.25b. This circuit was proposed by [125], and uses a control voltage

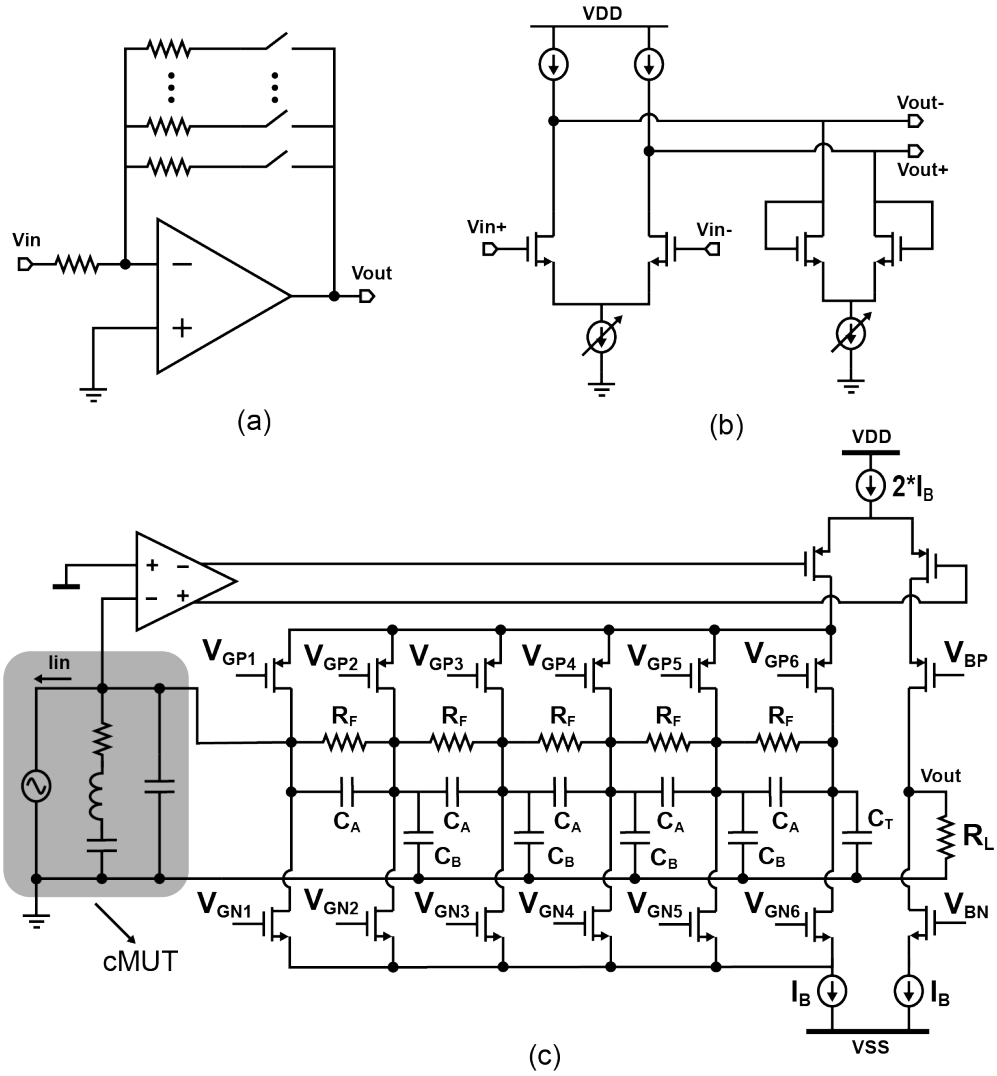


Figure 3.25: TGC amplifiers reported in the state-of-the-art: (a) PGA circuit ,(b) VGA circuit, and (c) VGA circuit with continuous interpolation between discrete gain steps.

to change both, the operating point of the input differential pair, and the impedance of the load, in order to obtain an approximated exponential transfer function. This approach although can achieve smoother gain transition than PGA circuits, tends to be sensitive to process, voltage, and temperature (PVT) variations [36].

Another approach to implement a VGA circuit is the continuous interpolation between discrete gain steps. An example of this approach is shown in Fig

3.25c, and was proposed by [25]. The input current signal is amplified by a current amplifier with discrete gain steps defined by the capacitive ladder feedback network. A sets of pMOS transistor are used to steer the feedback current between different taps of the capacitive ladder feedback network. A complementary nMOS current steering network is used to bias the circuit, which are controlled in a similar fashion that pMOS transistors in order to gradually change from one discrete gain step to the next. As a result, an approximately linear interpolation between exponential gain steps was obtained, resulting in an approximate linear-in-dB VGA circuit [25].

3.8.1 Requirements for the TGC amplifier

Aforementioned, the main function of a TGC amplifier is to reduce the large dynamic range of the transducer, compensating the propagation attenuation of the signals. Considering this, the variable gain range of the TGC amplifier will be limited by the total signal attenuation.

In this thesis we have considered that the target distance is in far-field region of the transducers designed by our research group, with a value around several millimeters.

The far-field pressure emitted by an array of M and N elements arranged in elevation and azimuth directions respectively, can be described as following [69]:

$$p(r,\theta,\phi) = \left[\frac{jNM\rho ckuAf(\theta,\phi)e^{-jkR}}{2\pi r}\right] \cdot D_A(\theta,\phi) \tag{3.11}$$

where $R = r - (N-1)Dsin(\theta)cos(\phi)/2 - (M-1)Lsin(\theta)sin(\phi)/2$, r is the distance from the array center to a field point, θ and ϕ represent the azimuth and elevation directions respectively in polar coordinate, D and L are the spacing between adjacent elements in azimuth and elevation direction respectively, ρ is the media density, c is the sound velocity, u is the individual transducer velocity, A is the individual transducer area, k is the wave number, $f(\theta,\phi)$ is the individual element directivity, and $D_A(\theta,\phi)$ is the array directivity. Eq 3.11 can be used to represent the far-field pressure, generated by a single pMUT if $M = N = 1$ and the second term is normalized to one.

If we considered that the acoustic pressure is propagated in a dissipated

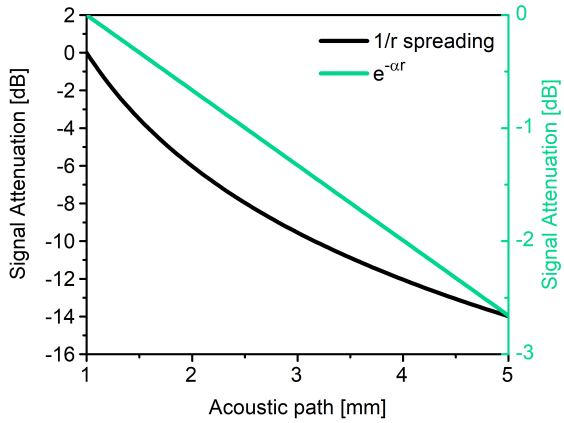


Figure 3.26: Ultrasound signal attenuation in fluorinert FC-70 vs acoustic path.

medium, it losses intensity due to some mechanisms such as viscosity, heat conduction, and relaxation [50]. This type of attenuation can be modeled as a multiplicative exponential term to Eq 3.11, which includes the frequency dependent attenuation coefficient (α). Considering this, the Eq 3.11 can be reformulated as following:

$$p(r,\theta,\phi) = \left[jNMP_0R_0 \cdot \frac{1}{r} \cdot e^{-\alpha r} \right] \cdot e^{-jkR} \cdot f(\theta,\phi) \cdot D_A(\theta,\phi) \tag{3.12}$$

where $P_0 = \rho cu$ is the pressure at the surface of the pMUT [45], and $R_0 = A/\lambda$ is the Rayleigh distance, being λ the wavelength of the acoustic signal in the propagation media [50].

From Eq 3.12 we can see that there are two terms that cause a decrease of the pressure amplitudes when the distance propagation (r) is increased. The first one is the $1/r$ term, which is due to the spread of the ultrasound wave in far-field region, while the second one ($e^{-\alpha r}$) is due to the dissipative properties of a real media. Figure 3.26 illustrates the attenuation associated with both terms for a propagation distance (r) from 1 to 5 mm. For this representation, the coefficient (α) was computed through Stoke's formula for liquids [126], which is rewritten as following:

$$\alpha = \frac{2}{3} \cdot \frac{\eta}{\rho} \cdot \frac{\omega^2}{c^3} \tag{3.13}$$

where η is the viscosity coefficient, ρ the density, c is the sound velocity,

Table 3.4: Target Specifications of the TGC Amplifier

Parameter	Value
Process technology	0.13μm CMOS
Power Supply [V]	1.5
Gain range	$\sim$14dB
Input voltage noise	$< 60.68nV/\sqrt{Hz}$ at 3 MHz
Bandwidth	$> 12MHz$

and $\omega = 2\pi f$ is the angular frequency, being f the operation frequency. Based on the viscosity coefficients for the target acoustic mediums in this thesis, fluorinert FC-70 ($\eta = 24cP$, $\rho = 1940Kg/m^3$, $c = 685m/s$ [127]) exhibits the highest value, and as consequently is considered the most critical dissipative medium. On the other hand, since Eq 3.13 is proportional to the square of the frequency, to compute α we have considered the highest frequency obtained by our pMUTs in FC-70 (around 9 MHz) [128]. As can be shown in Fig 3.26 the signal attenuation due to the spreading term $(1/r)$ is dominant, giving a maximum value of $\sim$14 dB. Considering this, we need to design a TGC amplifier whose transfer function will be linearly proportional to the penetration depth instead of exponential dependence. Moreover, the logarithm-in-dB gain range must be around 14 dB to compress the echo signals dynamic range.

On the other one, in order to avoid a degradation of the SNR of the complete conditioning circuitry (LNA and TGC amplifiers), the input voltage referred noise of the designed TGC amplifier needs to be lower than the output noise of the LNA circuit. Taking into account this, the input voltage referred noise density of the TGC circuit at the lowest gain must be lower than the measured output noise density of the proposed LNAs (60.68 $nV/\sqrt{Hz}$ at 3 MHz). Table 3.4 summarizes the target specifications to implement the TGC amplifier.

3.8.2 TGC Circuit Implementation

To implement the TGC amplifier we have chosen a VGA approach for better accuracy and to avoid any switching feed-through that may cause artifacts, which will degrade the SNR. We propose a VGA circuit where the gain can be well controlled by using a negative feedback topology to achieve high bandwidth and improve the linearity. The schematic circuit of the proposed TGC amplifier is shown in Fig 3.27. It consists of a single-ended cascode amplifier with a current mirror as load, and a degeneration resistor (Rs) is connected in series

with the source terminal of the input transistor (M1) to implement the negative feedback. M5 transistor is used to map the proposed circuit to voltage-voltage feedback topology, and then we can employ the two-port models to analyze the closed-loop circuit shown in Fig 3.27 [129]. In a similar way as in the LNA amplifier, we adopt a self-biased structure, which is implemented by a large MOS resistor connected between input and output.

To analyze the proposed circuit, it is first necessary to obtain the open-loop parameters. Figure 3.28a illustrates the small signal model of the feedforward amplifier taking into account the loading effect of the feedback network. Neglecting the bulk effect of the M1 and M2 transistors for purposes of simplicity, the open-loop gain at low frequency of the feedforward amplifier can be computed as following:

$$A_{OL} \approx \frac{-gm1}{gds3[1 + gm1 \cdot R_s]} \tag{3.14}$$

where $gm1$ is the transconductance of the M1 transistor, and $gds3$ is the output conductance of the M3 transistor. In Eq 3.14 we have assumed that the parallel combination of R_s and $1/gds5$, being $gds5$ the output conductance of the M5 transistor, is $\sim R_s$. The open-loop output resistance can be obtained by the parallel combination of $1/gds3$ and the output resistance of the cascode transistor M2 in series with the output resistance of the input transistor with the degeneration resistor (Rs). Thus, the open-loop output resistance of the

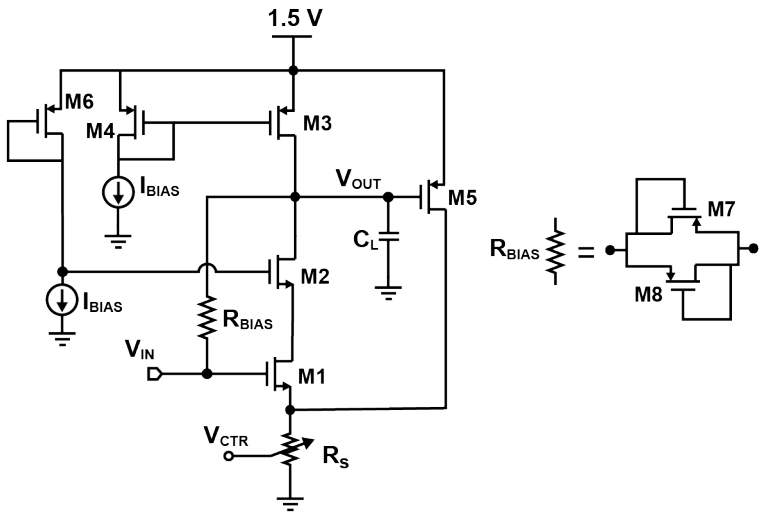


Figure 3.27: Schematic circuit of the proposed VGA.

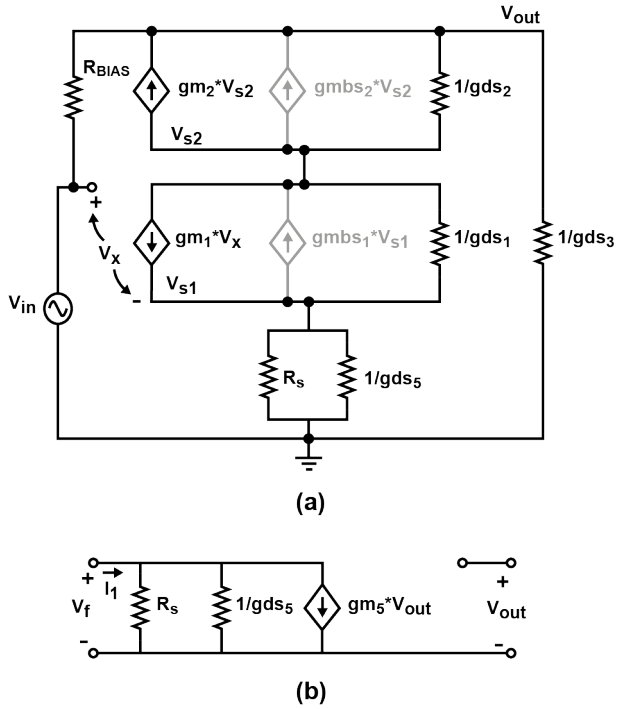


Figure 3.28: Small signal model at low frequencies of: (a) the feedfoward amplifier, (b) feedback network.

feedforward amplifier is described by the next equation:

$$R_{out-OL} \approx \frac{gm2 \cdot gm1 \cdot R_s}{gds1 \cdot gds2 + gm2 \cdot gm1 \cdot R_s \cdot gds3} \tag{3.15}$$

where $gm2$ is the transconductance of M2 transistor, $gds1$ and $gds2$ are the output conductances of M1 and M2 transistors, respectively.

The open-loop input resistance can be also obtained from the small-signal circuit represented in Fig 3.28a. It can be computed as:

$$R_{in-OL} \approx \frac{gds3 \cdot R_{BIAS} \cdot (1 + gm1 \cdot R_s)}{gm1} \tag{3.16}$$

where R_{BIAS} is the large DC bias resistor.

Figure 3.28b represents the small-signal circuit model at low frequencies of the feedback network, composed by the M5 pMOS transistor and the degeneration resistor (Rs). From this figure, the feedback factor β can be obtained as

following:

$$\begin{aligned}\beta &= \frac{V_f}{V_{out}}\Big|_{I_1=0} \\ &\approx -gm5 \cdot R_s\end{aligned} \tag{3.17}$$

where $gm5$ is the transconductance of M5 transistor.

From the theory of the negative feedback amplifier, is known that the closed-loop gain at low frequencies can be calculated as following:

$$A_{CL} = \frac{A_{OL}}{1 + \beta \cdot A_{OL}} \tag{3.18}$$

Considering this equation, and taking into account the Eqs. 3.14 and 3.17, the closed-loop gain at low frequencies of the circuit shown in Fig 3.27 can be obtained by the next equation:

$$A_{CL} = \frac{\dfrac{-gm1}{gds3[1 + gm1 \cdot R_s]}}{1 + gm5 \cdot R_s \cdot \dfrac{gm1}{gds3[1 + gm1 \cdot R_s]}} \tag{3.19}$$

From Eq. 3.19 can be shown that if the product of the open-loop gain (A_{OL}) and the feedback factor (β) is much higher than 1, the closed-loop gain of the designed amplifier is reduced to Eq 3.20, remaining only an a function of the feedback loop parameters. To achieve this, a proper dimensioning and biasing of the transistors were done. Table 5 summarizes the aspect ratio used to design the circuit illustrated in Fig 3.26, and the bias current source is around 20 μA.

$$A_{CL} \approx \frac{-1}{gm5 \cdot R_s} \tag{3.20}$$

From this result, we can see that if both, the transconductance of M5 transistor ($gm5$) and the degeneration resistor (R_s) are changed, a variable gain amplifier can be implemented with the circuit shown in Fig 3.27. Also, in this figure is illustrated that $gm5$ has a strong dependence of the DC output voltage of the feedforward amplifier, with which in order to change it, will be necessary

Table 3.5: Dimensions of the MOSFET devices used in the TGC amplifier

MOSFETs	**Aspect Ratio (W/L) (μm/μm)**
M1	6.4/0.15
M2	7.2/0.5
M3	15/1.5
M4	3/1.5
M5	4/1.3
M6	32/2
M7, M8	0.22/10

to change the operation point of the amplifier. This solution could be hard to implement, and therefore we opt to change R_s instead of $gm5$.

In order to implement a TGC amplifier using VGA approach, R_s resistor must be controllable by an analog voltage signal, which has a linear dependence with the acoustic path. Considering this, the degeneration resistor can be implemented by a nMOS transistor operated in deep triode region. Thus, the closed-loop gain of the proposed VGA at low frequencies can be rewritten as following:

$$A_{CL} \approx -\frac{K'_s W_s (V_{ctr} - V_{th-s})}{gm5 \cdot L_s} \tag{3.21}$$

where V_{ctr} is the acoustic path dependent analog voltage signal, K'_s is the technological constant of nMOS transistor, W_s, L_s, V_{th-s} are the width, length and the threshold voltage of the nMOS transistor used to implement R_s, respectively. To maximize the variable gain range, the degeneration resistor was implemented by the parallel connection of seven low threshold voltage nMOS transistor available in the CMOS process technology of Silterra. Figure 3.29 shows the implementation of the R_s resistor.

Figure 3.30a shows the behavior of the gain at low frequencies of the proposed VGA. It can be seen, it has a logarithm response in dB, being in a good agreement with Eq. 3.21, and a variable range from 17 to 29 dB. In Fig 3.30b, is represented the variation of both, the degeneration resistor (R_s) and the transconductance of M5 transistor ($gm5$), as a function of the control voltage. As illustrated, $gm5$ practically remains constant from 0.5 to 1.5 V of control voltage, while R_s changes around 12 dB, being this value close to the variable gain range of the Fig 3.30a. Considering this, we can say that the variation of the closed-loop gain of the proposed VGA is defined by R_s values.

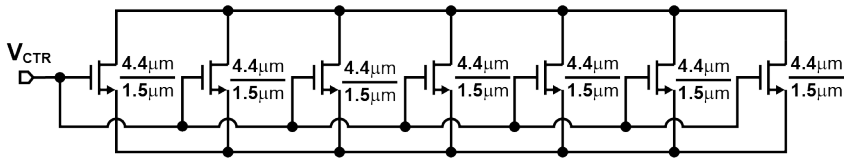
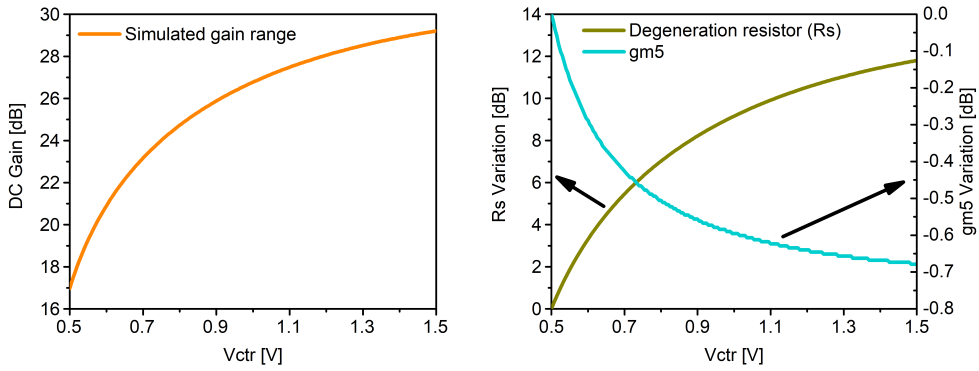


Figure 3.29: Implementation of the degeneration resistor. All devices are low-voltage and low-threshold voltage transistors.



(a) (b)

Figure 3.30: (a) Simulated DC gain as a function of the control voltage (V_{ctr}), and (b), Variation of the degeneration resistor (R_s) and the transconductance of M5 ($gm5$) in function of V_{ctr}

As mentioned above, TGC amplifier is usually the stage that precedes the LNA in the ultrasound conditioning circuitry. In this thesis, the LNA and TGC amplifiers are AC coupled by a capacitor to independently set the input DC bias condition of the TGC. In order to save area and not affect the overall frequency response, this capacitor has been implemented with three-metal finger-capacitor, whose total capacitance is around 1 pF.

To avoid saturation or distortion at the VGA output, for strong echoes coming from close distance to the transducer, the VGA circuit is bypassed. Figure 3.31 shows the schematic circuit of the combined LNA and TGC amplifiers, highlighting in red the transistors involved in the bypass operation. To enable the bypass option of the VGA, properly connection of the LNA and VGA is required. As shown in Fig 3.31b, a direct DC path is created from V_{DD} to LNA output through $M3$ and $M9$ transistors, when the baypass option is enabled. This results in a change of the operation point of the LNA, affecting its gain. To correct this, the DC current flow through the baypass path must be insignificant in front of the bias current of the LNA. To implement this,

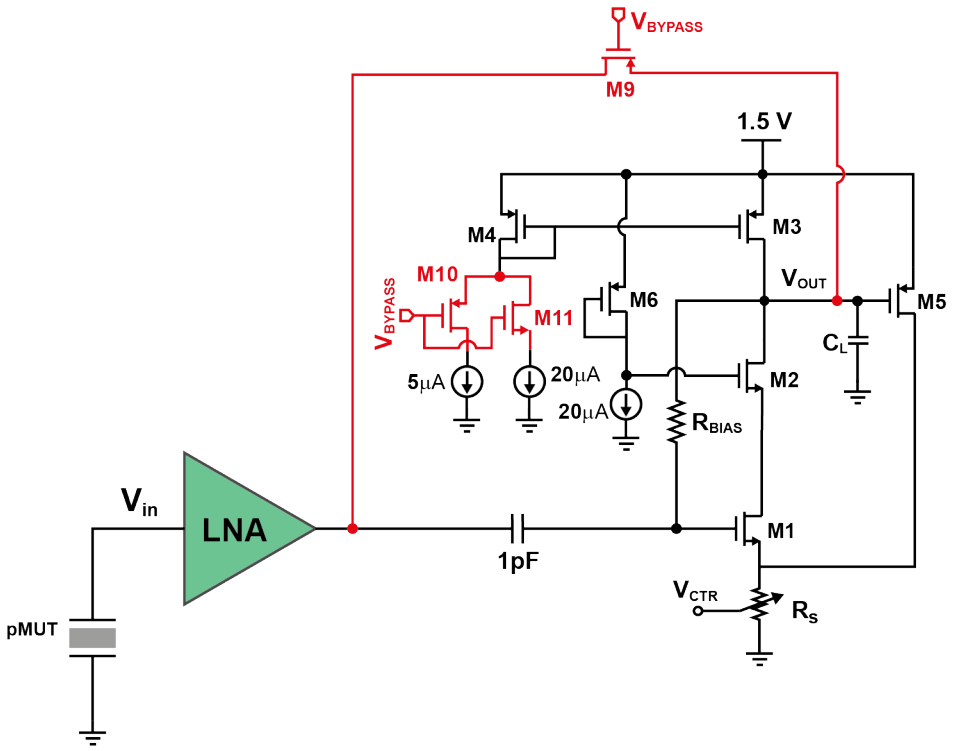
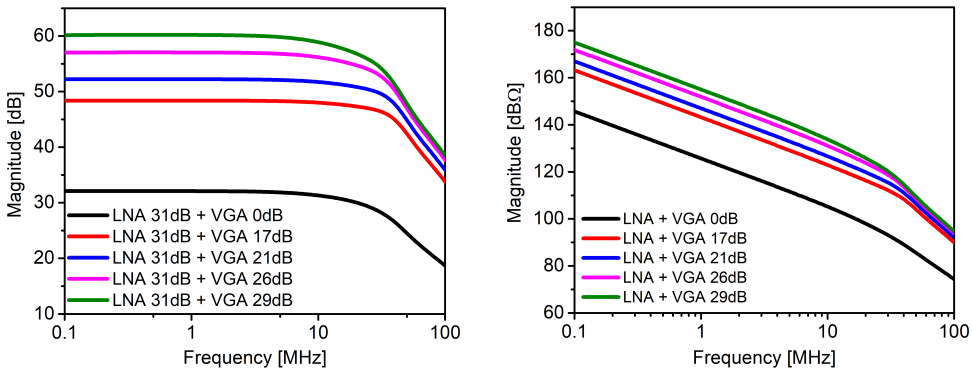


Figure 3.31: LNA and VGA connection scheme, highlighting in red the bypass option of the VGA circuit.

two chosen bias current sources fed the VGA circuit. The first one, is a small current source, around 5 μA, that is chosen when the bypass option is enabled. Thus, around 25 μA flows through the bypass path, being neglected in front of 200 μA of the LNA bias current. The second one is the bias current of the VGA amplifier, whose value is close to 20 μA, and is selected when the VGA is used. The selection of the bias current sources is implemented by two switches, $M10$ and $M11$, which are driven by the same drive signal of the bypass switch.

Figures 3.32a and 3.32b illustrate the simulated frequency responses of the combined LNA and VGA amplifiers, in terms of voltage-voltage and transimpedance transfer functions, respectively. Is shown that when the VGA is bypassed, VGA 0dB case, the frequency response is similar to the obtained LNA in Fig 3.9. On the other hand, when the VGA is enabled, the variable gain range of the VGA is added to the LNA gain, obtaining a maximum DC voltage gain of ~60 dB. In a similar form, a maximum of 145.34 dBΩ is obtained at 3 MHz for 2.3 pF of parasitic capacitance (C_p) and 300 fF of electrical



(a) (b)

Figure 3.32: Simulated transfer functions of the combined LNA and VGA amplifiers for four VGA gain setting ($V_{ctr} = 0.5, 0.6, 0.9 and 1.5V$), and when the bypass option is enabled. (a) Simulated voltage-voltage transfer functions, and (b), Simulated transimpedance transfer functions.

transducer's capacitance (C_0).

Frequency Response Analysis

The corner frequencies of the combined LNA-VGA, and the stability of the proposed VGA circuit are analyzed in this section. Since the LNA and VGA amplifiers are AC coupled, the overall frequency response of the combined circuits has a band-pass behavior. The lower corner frequency is defined by the high-pass filter formed by the LNA output resistance, VGA input resistance, and the AC coupling capacitor. Considering this, the magnitude of this pole can be computed as following:

$$f_{l_{-3dB}} \approx \frac{1}{2\pi \cdot C_d \cdot (R_{out-LNA} + R_{in-CL})} \tag{3.22}$$

where C_d is the AC coupling capacitor, $R_{out-LNA}$ is the output resistance of the LNA, and R_{in-CL} is the closed-loop input resistance of the VGA amplifier. R_{in-CL} can be obtained from the open-loop input resistance R_{in-OL}, the open-loop gain (A_{OL}), and the feedback factor β, given by equations 3.16, 3.14, and 3.17, respectively.

$$R_{in-CL} \approx R_{in-OL} \cdot (1 + A_{OL} \cdot \beta) \tag{3.23}$$

The upper corner frequency can be obtained using a dominant pole estimation

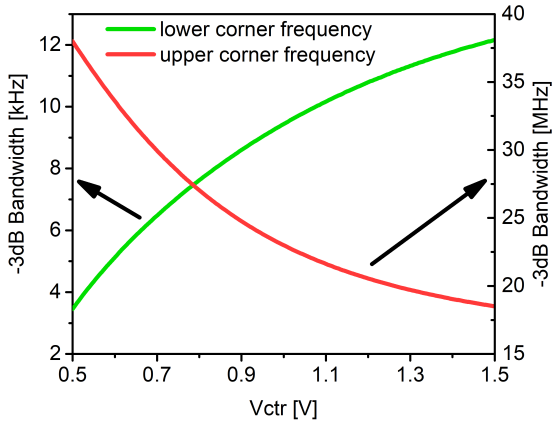


Figure 3.33: Variation of the lower and upper corner frequencies of the combined LNA and VGA amplifiers, as functions of the control voltage.

technique at the output node in the VGA circuit, which is defined from the closed-loop output resistance and the total capacitance from the output node to ground (C_{out}). This capacitance is mainly dominated by the input capacitance of the succeeding stage. In this analysis, we have considered the output buffer as succeeding stage to VGA, being approximately 32 fF. The closed-loop output resistance is computed as following:

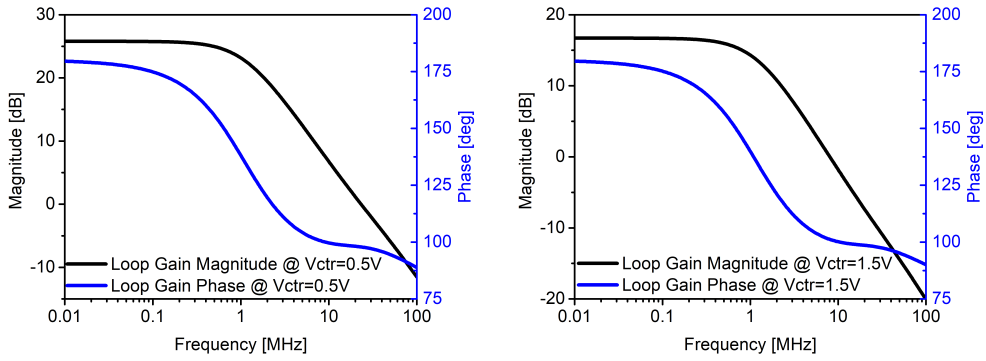
$$R_{out-CL} \approx \frac{R_{out-OL}}{1 + A_{OL} \cdot \beta} \tag{3.24}$$

where R_{out-OL} is the open-loop resistance, which is given by Eq. 3.15. Thus, the upper corner frequency can be estimated by the following equation:

$$f_{u_{-3dB}} \approx \frac{1}{2\pi \cdot R_{out-CL} \cdot C_{out}} \tag{3.25}$$

Figure 3.33 shows the behavior of the lower and upper corner frequencies for control voltages from 0.5 to 1.5 V. As can be shown, the most critical case is for 1.5 V of control voltage, obtaining a -3 dB bandwidth from ∼12 kHz to 19 MHz. These values are well far from the band of interest of our transducers.

To analyze the stability of the proposed VGA, we have simulated the magnitude and phase of the loop-gain ($A_{OL} \cdot \beta$). Figures 3.34a and 3.34b illustrate these results for variable gain range limits. From these figures, we can see that the proposed closed-loop VGA amplifier achieves almost constant margin phase



(a) (b)

Figure 3.34: Simulated magnitude and phase of the Loop-Gain ($A_{OL} \cdot \beta$). (a) For a control voltage (V_{ctr}) of 0.5 V (with which the lowest DC closed-loop gain is achieved), and (b) when $V_{ctr} = 1.5V$, with which the highest DC closed-loop gain is achieved.

Table 3.6: Performance summary of the combined LNA and VGA amplifiers.

Parameter	**LNA + Bypassed VGA**	**LNA + VGA @$V_{ctr} = 0.5V$**	**LNA + VGA @$V_{ctr} = 1.5V$**
DC Voltage Gain [dB]	32	48	60
TIA Gain [dBΩ]	116 @3MHz	134 @3MHz	145 @3MHz
-3dB upper frequency[MHz]	26	38	19
Input P1dB @3MHz	950 nApp	214 nApp	43 nApp
Output P1dB @3MHz	560 mVpp	809 mVpp	630 mVpp
Input current noise [pA/$\sqrt{Hz}$]	0.2 @3MHz	0.2 @3MHz	0.2 @3MHz
Output voltage noise [μV/$\sqrt{Hz}$]	0.15 @3MHz	0.9 @3MHz	3.4 @3MHz
DC Power Consumption [mW]	0.3	0.65	0.67
Phase Margin [deg]	–	98	101

range, from 97.85°to 101.3°, for the variable gain range. The lowest value of this range (97.85°) is well above 60°phase margin, which is the minimum condition to guarantee stability.

Electrical performance summary

Table 3.6 summarizes the electrical performance of the combined LNA and VGA circuits. All simulation results were obtained considering the electrical capacitance of the transducer ($C_0 = 300fF$), the parasitic capacitance esti-

mated in previous section ($C_p = 2.3pF$), and an output capacitance of 32 fF (equivalent to the input capacitance of the succeeding stage). The lowest simulated input 1 dB compression point was 43 nA peak-to-peak when the maximum achievable gain was set. This value is much higher than the expected echo strengths (in a range of hundreds of pA peak-to-peak). In this case, the LNA plus VGA, with its maximum gain, will be used. On the other hand, the highest simulated input 1 dB compression point was 950 nA peak-to-peak, which is much higher than the highest expected strengths of the received echoes (in a range of tens of nA peak-to-peak). Thus, the expected strengths of the received echoes will fall within the linear range of the combined LNA and VGA amplifiers, with which harmonic distortion is no longer a major problem.

The simulated input current noise density referred to the transducer, was 0.2 pA/$\sqrt{Hz}$ at 3 MHz, which is close to the experimental value obtained in above section. Also, can be shown that this value is mainly contributed by the LNA amplifier. As is expected, the power consumption is increased when the VGA circuit is enabled, although the obtained values remain competitive with the LNA state-of-the-art (see Table 3.3).

3.8.3 Bias current reference

To reduce power consumption, a 5 μA current reference has been designed, which will be mirrored to obtain 20 μA of bias current. If the 5 μA current reference is implemented with the circuit shown in Fig 3.18, a resistor of ∼100

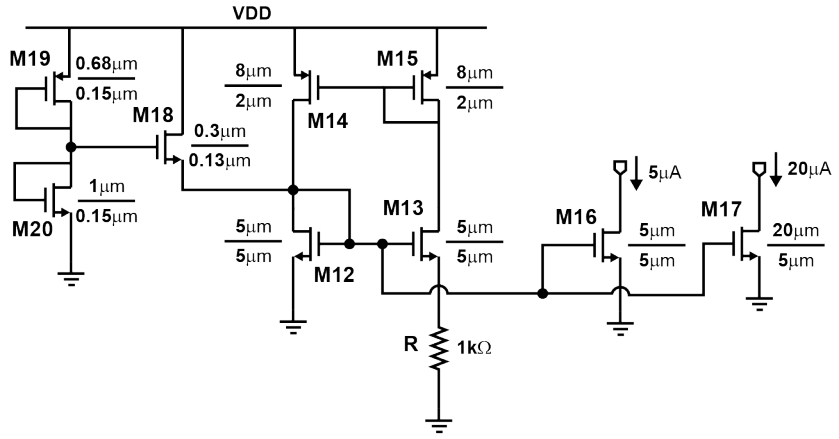


Figure 3.35: Implementation of the bias current references.

kΩ is needed. To implement this, a large silicon area is consumed, which is not beneficial. This drawback has been solved by implementing a self-biased micro-current reference, as shown in Fig 3.35. In this case, unlike the reference current represented in Fig 3.18, where the voltage across the resistor R is equal to the gate-source voltage of the M12 transistor, the voltage drop across the resistor R is the subtraction of the gate-source voltages of M12 and M13 transistors. Thus, 5 μA of current reference has been possible to generate with only 1 kΩ resistor, saving a large silicon area. The 20 μA bias current is obtained through the current mirror structure formed by M12 and M17 transistors. The designed current reference also has two equilibrium points, and therefore a start-up circuit, similar to used in Fig 3.18, is necessary.

3.8.4 Output Buffer for testing purposes.

To test combined LNA-VGA amplifiers, it is necessary to design an output buffer. The previously designed output buffer has two main drawbacks that makes it unsuitable for testing both the LNA and VGA together. The first one is the large input capacitance it presents, around 600 fF, which causes a reduction of the upper corner frequency, and as a consequence the overall bandwidth is affected. On the other hand, the output swing of the source follower structure is very limited, which will cause a large signal distortion when both amplifiers are used. To address these drawbacks, a new output buffer has been designed.

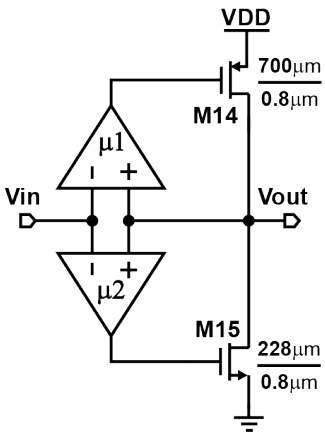


Figure 3.36: Proposed closed-loop output buffer.

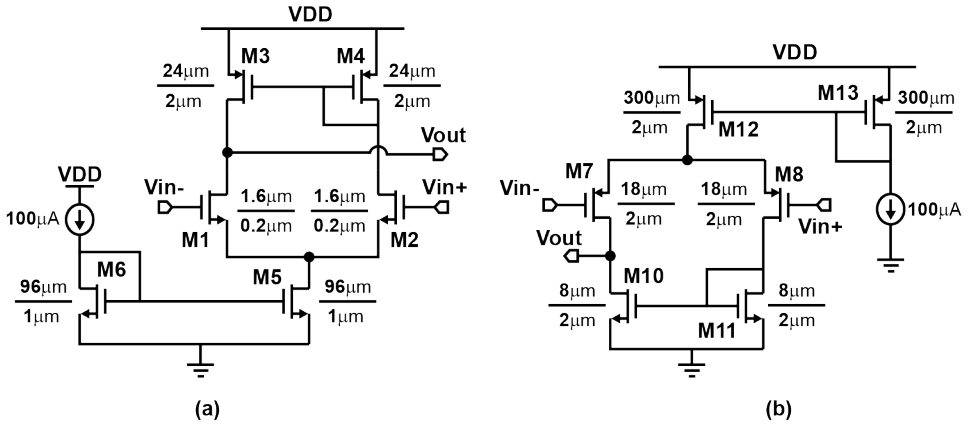


Figure 3.37: Implementation of the error amplifiers. (a) $\mu 1$ amplifier, and (b) $\mu 2$ amplifier.

Figure 3.36 shows the schematic circuit of the new designed output buffer. It uses a push-pull common source structure as output stage (M14 and M15 transistors) in order to maximize the output swing. To reduce the output resistance the negative feedback concept is implemented through the differential amplifiers $\mu 1$ and $\mu 2$. This circuit operates as following: if Vin increases, the output of both differential amplifiers decreases, causing that the gate-to-source voltage of M14 increases while that of M15 decreases. This causes that the M15 turns off and M14 sources the current to the load, resulting in an increase of the output voltage $Vout$. As $Vout$ is directly connected to the non-inverter input of the differential amplifiers, the error voltage between differential amplifier inputs decreases, which counteracts the increase of the Vin, demonstrating the negative feedback operation. A similar process occurs when the Vin decreases, where M14 turn off and M15 sinks the load current, causing that $Vout$ to decrease.

From a similar analysis done for the designed closed-loop VGA amplifier, if the loop gain is large ($A_{OL} \cdot \beta >> 1$), the closed-loop gain of the circuit shown in Fig 3.36 is $\approx 1/\beta$. From this figure, we can see that the feedback network does not contain any devices, and therefore $\beta = 1$, with which the proposed output buffer is like a voltage follower circuit. Taking into account this, the differential input voltages are very low, and therefore both differential amplifiers behave as error amplifiers with open-loop gains $\mu 1$ and $\mu 2$. The implementation of both amplifiers is represented in Fig 3.37a and b, respectively.

Table 3.7: Performance summary and comparison of the designed output buffers.

Parameter	Source follower output buffer	Closed-loop output buffer
Input capacitance	600 fF	32 fF
Input P1dB @3MHz	212 mVpp	843 mVpp
Output P1dB @3MHz	96 mVpp	715 mVpp
THD	14.22% @ 96 mVpp	9.3% @ 715 mVpp
Bandwidth @$C_L = 30pF$	200 MHz	55 MHz
Output resistance	46.5 Ω	1.2Ω
DC Power Consumption	1.8 mW	5.25 mW
Phase Margin	–	∼66deg @$C_L = 30pF$

The output resistance of the proposed closed-loop output buffer can be computed as following [130]:

$$R_{out} \approx \frac{1}{\mu \cdot (gm_{14} + gm_{15})} \tag{3.26}$$

where gm_{14} and gm_{15} are the transconductances of M14 and M15 transistors, and $\mu = \mu 1 = \mu 2$. The proposed closed-loop output buffer achieves an output resistance of ∼1.2Ω. Figure 3.38 illustrates the magnitude and phase of the circuit shown in Fig 3.36 when 50Ω in parallel with 30 pF was connected as load. As can be shown the attenuation can be negligible due to the very low output resistance obtained, and the phase shift in the band of interest is close to zero degree.

Table 3.7 summarizes the electrical performance of the closed-loop output

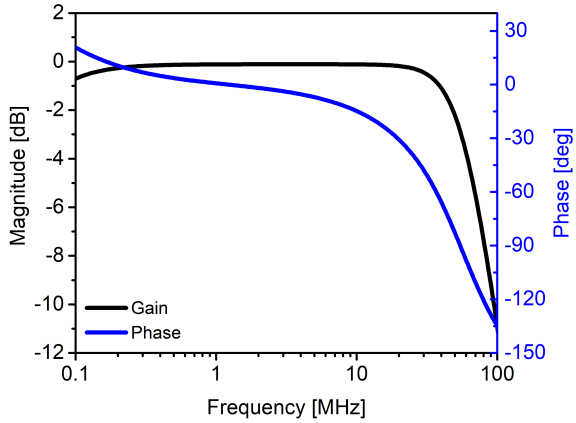


Figure 3.38: Magnitude and phase of the closed-loop transfer function of the circuit shown in Fig 3.36.

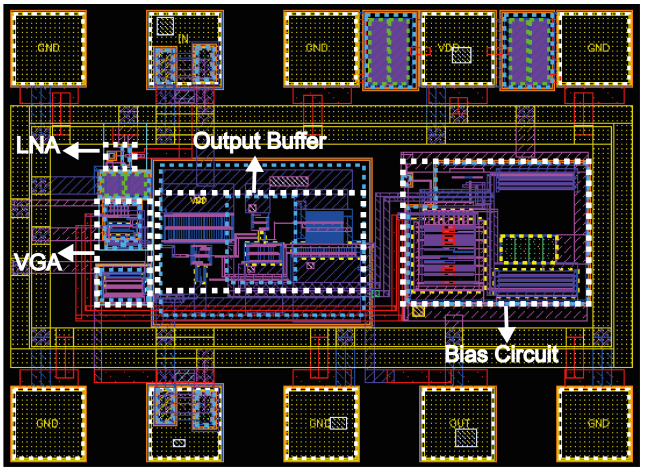


Figure 3.39: Final layout of the chip. It includes the LNA, VGA, bias circuit, and the output buffer.

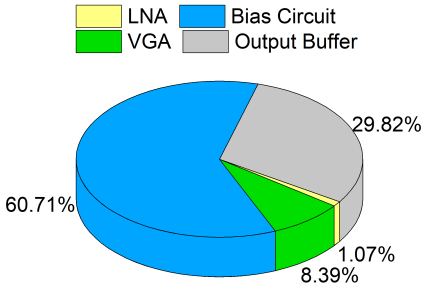


Figure 3.40: Area breakdown of the chip.

buffer and states a comparison with the source follower output buffer previously designed. The designed closed-loop circuit achieves an improvement of input and output voltage swing, distortion, and input capacitance. In contrast, to achieve this the DC power consumption was increased.

Figure 3.39 shows the layout of the chip, which includes: a LNA, a VGA, a bias circuit, a closed-loop output buffer, and bonding pads. The total consumed area, without including the bonding pads, is approximately of $0.056mm^2$. Figure 3.40 illustrates the area breakdown of the chip. We can see that the bias circuit and the output buffer occupy almost the entire total area, whereas the LNA and VGA consume an area of 0.0006 mm^2 and 0.0047 mm^2, respectively.

3.9 Conclusions

This section has presented the circuit implementation of the TGC amplifier to compensate the $1/r$ spreading attenuation. We adopt a variable gain amplifier approach to implement the TGC circuit in order to achieve smooth gain transitions. The proposed VGA circuit can provide gains from 17 to 29 dB. In order to avoid saturation at the VGA output when strong echoes are received, a bypass option was implemented. The combined LNA and VGA amplifiers achieve a maximum output dynamic range of 50 dB within the transducer's bandwidth ($\sim$1MHz), and consume only 0.67 mW.

On the other hand, to reduce the distortion when both amplifiers will be tested, we have implemented a closed-loop output buffer. This circuit improves the previously designed output buffer in terms of input capacitance and linearity.

CHAPTER 4

Monolithic Single pMUT-on-CMOS Ultrasound System

In this chapter, a single two-port AlN pMUT fully integrated with its analog front-end CMOS circuitry is presented. It'll start with describing the two-port pMUT design and fabrication process. This is followed by a theoretical analysis regarding the benefits of reducing the parasitic capacitance, enabling us to demonstrate an increase in signal-to-noise ratio (SNR). Finally, the acoustic experimental results will be presented and compared with the state-of-the-art. This chapter is based on the analysis and results discussed in: *I. Zamora, E. Ledesma, A. Uranga, and N. Barniol, "Monolithic Single PMUT-on-CMOS Ultrasound System with +17 dB SNR for Imaging Applications," IEEE Access, vol. 8, pp. 142785–142794, doi: 10.1109/ACCESS.2020.3013763., 2020.* All the acoustic characterization was carried out in collaboration with Eyglis Ledesma.

4.1 Design and Fabrication

The ultrasound transceiver is composed of a square pMUT with two-top electrodes (inner and outer electrodes) that allows it to act as a two-port pMUT

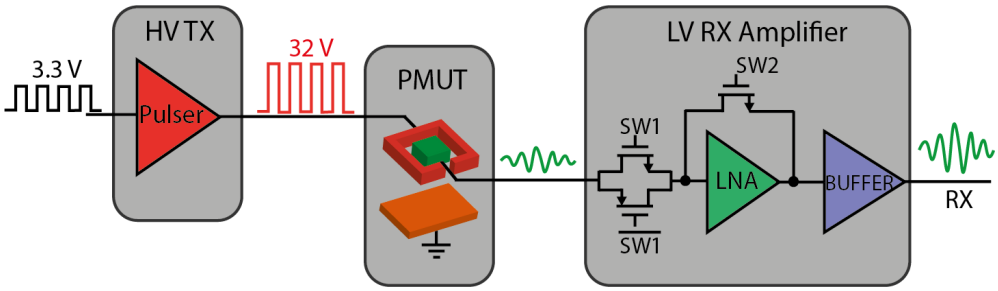
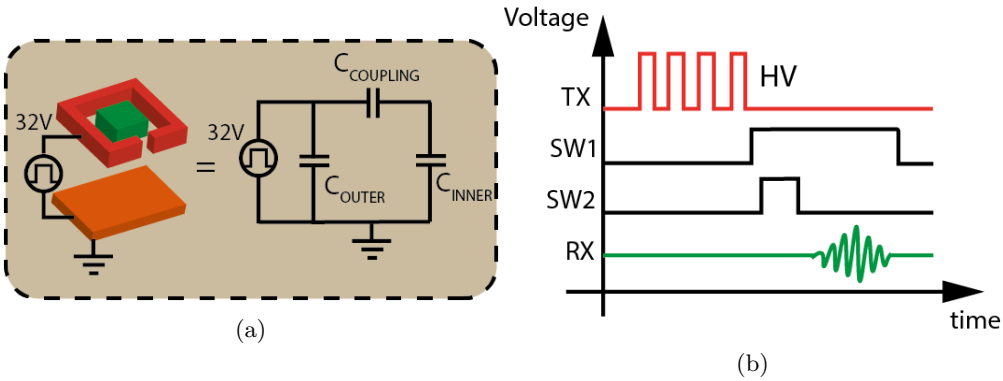


Figure 4.1: Block diagram of the proposed transmission and reception system. HV TX: High Voltage Transmitter; pMUT with two top electrodes and one bottom electrode; LV RX: Low Voltage Receiver.

device. The outer electrode is used to generate the ultrasound wave and the incoming acoustic pressure is sensed by the inner electrode. A general diagram of the ultrasound system is shown in Fig. 4.1. During the transmission, a High Voltage (HV) Pulser, such as the one described in Chapter 2, raised monophasic pulses from 3.3 V to 32 V at the pMUT resonance frequency in order to generate acoustic pressure. In the receiving mode, to convert the electric charge generated by the pMUT when an acoustic wave reached its surface, the LNA amplifier discussed in Chapter 3 was used. A Voltage Amplifier (VA) topology is considered instead of a Charge Sensitive Amplifier (CSA) in order to reach higher DC gain taking into account that the pMUT will be fully integrated with the analog front-end circuitry, and then the parasitic capacitance at the interface pMUT - LNA will be greatly reduced [110]. Also, as can be seen, two switches are used to prevent damage to the LNA, due to crosstalk between the top inner and outer electrodes. From Fig. 4.2a, $C_{COUPLING}$ appears as a consequence of the gap between both electrodes (2 μm) which causes that $\sim$1.6 V signal (0.82 V AC signal over 0.75 V LNA operation point) to be coupled to the inner electrode during transmission when the pMUT is directly loaded with the LNA (inner electrode capacitance, C_{INNER}, in parallel with VA equivalent input capacitance, C_{inLNA}). In this context, Switch 1 (SW1, between the inner electrode and the LNA input) prevents the gate-to-bulk voltage from exceeding its corresponding breakdown voltage, whereas Switch 2 (SW2, between input and output of the LNA) allows the LNA to quickly return to its adequate operation point (Vdd/2) after opening Switch 1, for the creation of the low impedance path among the LNA input and output. A time diagram considering one cycle of transmission and reception is shown in Fig. 4.2b.



(a) (b)

Figure 4.2: (a)Electrical equivalent circuit, with C_{OUTER} and C_{INNER}, capacitances between outer and inner pMUT electrodes and bottom pMUT electrode (grounded), respectively ($C_{COUPLING}$ is the coupled capacitance between both). (b) Time diagram for one cycle of transmission and reception.

The presented pMUT-on-CMOS ultrasound system has been fabricated with 130 nm CMOS technology using the SilTerra MEMS-on-CMOS fabrication process [108], [131], [132]. The pMUT consists of a square multilayered structure with an 80 μm side where 1.3 μm AlN is sandwiched between three Al electrodes (two tops with a thickness of 0.35 μm and one bottom with 0.4 μm thickness) and is covered by 1.5 μm of Si_3N_4 that seals the cavity and acts as an elastic layer [108]. The interconnection with the last metal of the CMOS Back-end-of-line (BEOL) is performed through metal vias avoiding any bonding technique and decreasing the parasitic capacitance. The final layout and a schematic cross-section of the pMUT built on the CMOS circuitry are shown in Fig. 4.3.

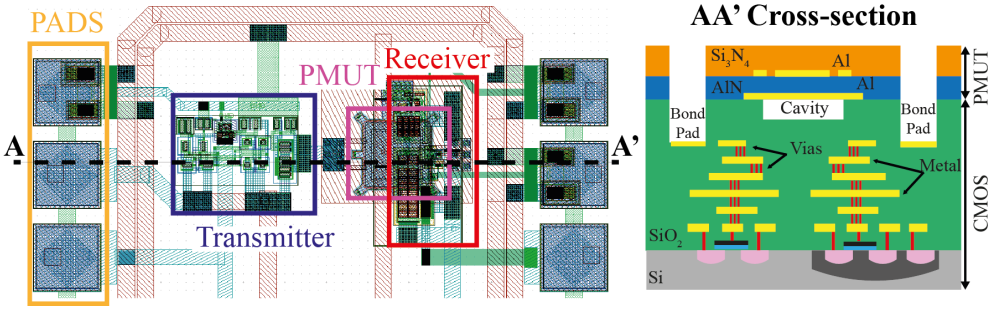


Figure 4.3: Full layout of the proposed Ultrasound System, with the pMUT (mallow box) monolithically integrated over the CMOS front-end circuitry TX (blue box) and RX (red box). Right: AA' Cross-section of the pMUT-on-CMOS Silterra technology (layers not to scale).

4.1.1 Signal-to-Noise Ratio Analysis

The signal-to-noise ratio (SNR) is one of the most important parameters that define the quality of an ultrasound image. For instance, in fingerprint sensors at least 12 dB are required to obtain accurate image results [133]. As it has been explained, the monolithic integrated system (IS) reduces the parasitic capacitance associated with any bonding techniques between pMUT and CMOS (for example, eutectic bonding), and even more with respect to a non-integrated system (NIS). In this context, the influence of the parasitic capacitances is analyzed in two of the most key parameters of an ultrasound channel reception: the signal and noise level. Based on the improvement factor in the signal (F_s, Eq. 4.1) and noise (F_n, Eq. 4.3) of an IS with respect to a NIS, the improvement in the SNR can be found through the product of $F_s \cdot F_n$. To obtain these parameters the electrical scheme shown in Fig. 4.4 was used, where the isolation switches are not considered; however, the individual behavior of the pMUT and LNA is expected to be the same in both scheme (with and without isolation switches).

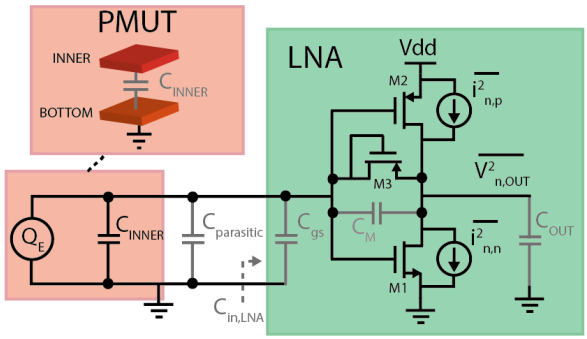


Figure 4.4: Reception scheme without isolation switches considering all electrical capacitances and noise current sources [109].

All electrical parameters of the pMUT and LNA amplifier are summarized in Table 4.1.

Equation 4.1 describes the signal improvement factor (F_s) where V_{IS} and V_{NIS} are the voltage amplitudes at the LNA output for the IS and NIS respectively. C_{INNER}, C_{inLNA} and $C_{parasitic}$ are defined in Table 4.1, where the last one is considered 0 pF for IS. Figure 4.5 blue shows a good agreement between

Table 4.1: Summary of LNA and pMUT electrical parameters.

	Parameter	Value	Comments
pMUT	C_{INNER} (fF)	262	[109]
	C_{OUTER} (fF)	216	
	$C_{COUPLING}$ (fF)	23	
LNA	C_M (fF)	19.8	Exctracted from Cadence
	C_{gs} (fF)	63	Exctracted from Cadence
	C_{OUT} (pF)	1	Exctracted from Cadence
	C_{inLNA} (fF)	609	$C_{gs}+C_M\cdot(1+A_{ol})$ Considering the Miller effect
pMUT+LNA	$C_{parasitic}$ (pF)	0-7	Due to PCB, connectors and bondings pads
	C_{inIS} (fF)	325	$C_{gs}+C_{INNER}$
	C_{inNIS} (pF)	0.33-7.33	$C_{gs}+C_{INNER}+C_{parasitic}$

simulated and computed values reported in [109].

$$F_s = \frac{V_{IS}}{V_{NIS}} = 1 + \frac{C_{parasitic}}{C_{INNER} + C_{inLNA}} \tag{4.1}$$

The equivalent output-mean-square voltage noise ($\overline{V^2{}_{n,OUT}}$) was obtained in order to analyze the noise improvement factor (F_n). Equation 4.2 describes it considering that all transistors works in saturation region.

$$\begin{aligned} \overline{V^2_{n,OUT}} = |Z_{out}(j\omega)|^2 \cdot \left(\overline{i^2_{n,n}} + \overline{i^2_{n,p}}\right) &= \frac{(C_M + C_{in})^2 \cdot \left(\overline{i^2_{n,n}} + \overline{i^2_{n,p}}\right)}{(A \cdot B)^2} \\ A &= \Big[C_M(g_{m,n} + g_{m,p}) + C_{in}(g_{ds,n} + g_{ds,p})\Big] \\ B &= \left[1 + \frac{j\omega(C_{in}C_M + C_{out}C_M + C_{out}C_{in})}{C_M(g_{m,n} + g_{m,p}) + C_{in}(g_{ds,n} + g_{ds,p})}\right] \end{aligned} \tag{4.2}$$

where $Z_{out}(j\omega)$ is the output impedance, ω is the angular frequency, $\overline{i^2_{n,n}}$ and $\overline{i^2_{n,p}}$ are the mean-square current-noise sources for nMOS and pMOS transistors respectively, C_M is the Miller capacitance between the input and output of the LNA, C_{in} is the equivalent input capacitance without considering the Miller effect (gate- to-source capacitance, C_{gs}, in parallel with C_{INNER} in parallel with $C_{parasitic}$), C_{out} is the output capacitance of the LNA (dominated by the input capacitance of the output buffer), g_m is the transconductance, g_{ds} is the output

conductance, where the subscript n and p are used to refer nMOS and pMOS transistor, respectively.

Based on this, the output noise improvement factor (F_n) can be written as Eq. 4.3 being $C_{in,IS}$ the integrated system equivalent input capacitance (C_{in} with $C_{parasitic} = 0$ pF), $C_{in,NIS}$ the non-integrated system equivalent input capacitance (C_{in}), and A_{ol} is the open loop gain of the LNA (28.5 dB without buffer). The computed values shown on the red line in Fig. 4.5 achieve a good correspondence with the simulation results using Cadence.

$$F_n = \sqrt{\frac{\overline{V^2_{n,OUT,NIS}}}{\overline{V^2_{n,OUT,IS}}}} = \frac{\frac{C_M}{C_{in,IS}} \cdot A_{ol} + 1}{\frac{C_M}{C_{in,NIS}} \cdot A_{ol} + 1} \tag{4.3}$$

From Figure 4.5, the monolithic approach corresponds to 0 pF of parasitic capacitance, which means that $F_s = F_n = 1$. However, if the parasitic capacitances increase the amplitude signal is degraded (F_s increases) and the system is noisier (F_n increases). In terms of signal-to-noise ratio when the $C_{parasitic}$ is 1 pF, the monolithic solution achieves an SNR 12 dB higher, even reaching 27 dB if the $C_{parasitic}$ is 7 pF demonstrating clearly the benefits of the reduction of the parasitic capacitances.

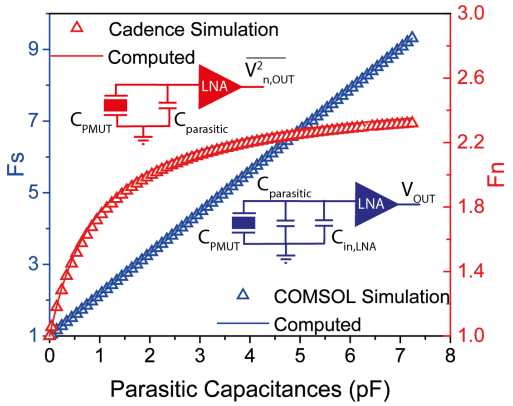


Figure 4.5: Computed and simulated results of: Signal Improvement Factor, F_s, (left axis, blue) and Noise Improvement Factor, F_n, (right axis, red) [109].

Finally, to complete the noise analysis, the isolation switches were considered using the equivalent electrical scheme shown in Fig. 4.6 where $\overline{V^2_{n,Rsw1}}$ corresponds to the thermal noise generated by Switch 1 (SW1) when is conducting,

and $\overline{V_{n,LNA}^2}$ and $\overline{i_{n,LNA}^2}$ are the voltage noise and input-referred current source of the LNA, respectively. The input-referred noise ($\overline{V_{n,IN}^2}$) can be obtained through Eq. 4.4 considering that $\overline{V_{n,LNA}^2}$ and $\overline{i_{n,LNA}^2}$ are correlated with each other, but uncorrelated with $\overline{V_{n,Rsw1}^2}$.

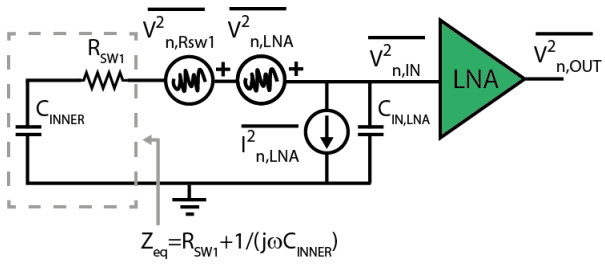


Figure 4.6: Simplified reception scheme considering the isolation switches and the input-referred noise sources [109].

$$\overline{V_{n,IN}^2} = \overline{\left(V_{n,LNA}\left|\frac{Z_{in,LNA}}{Z_{in,LNA}+Z_{eq}}\right| + i_{in,LNA}\left|\frac{Z_{in,LNA}Z_{eq}}{Z_{in,LNA}+Z_{eq}}\right|\right)^2} + \overline{V_{n,Rsw1}^2}\left|\frac{Z_{in,LNA}}{Z_{in,LNA}+Z_{eq}}\right|^2 \tag{4.4}$$

From this equation, $Z_{in,LNA}$ represents the equivalent input impedance of the LNA ($1/j\omega C_{in,LNA}$), and Z_{eq} is the equivalent impedance (indicated with gray dash line in Fig. 4.6) taking into account the serial connection of the ON resistor of the switch 1 (R_{SW1}) and the inner capacitance of the pMUT (C_{INNER}). The value of R_{SW1} is close to 11 kΩ, and at the pMUT resonance frequency $|1/j\omega C_{in,LNA}| \gg R_{SW1}$, which allows converting Eq.4.4 to Eq.4.5. As it can be seen, the equivalent input-referred voltage noise when the pMUT is loaded with the LNA without isolation switches is given by the first term, which means that the contribution of the switches in the noise performance can by represented by the second term of the expression.

$$\overline{V_{n,IN}^2} = \overline{\left(V_{n,LNA}\frac{C_{INNER}}{C_{INNER}+C_{in,LNA}} + i_{in,LNA}\frac{1}{\omega\cdot(C_{INNER}+C_{in,LNA})}\right)^2} + \overline{V_{n,Rsw1}^2}\left(\frac{C_{INNER}}{C_{INNER}+C_{in,LNA}}\right)^2 \tag{4.5}$$

4.2 Experimental results

Figure 4.7 shows the optical image of the proposed pMUT-on-CMOS system which has been fabricated with the 130 nm HV CMOS process using the MEMS-on-CMOS platform from Silterra. Note in the zoomed image the metal dummies of the CMOS BEOL metal layers (corresponding to M6 layer).

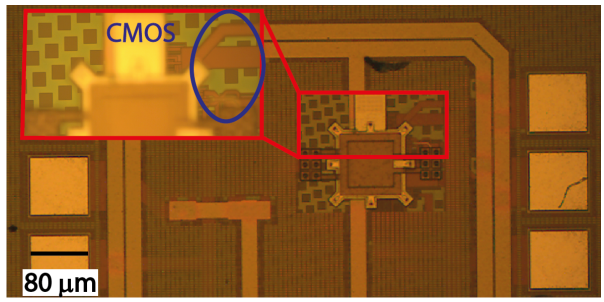


Figure 4.7: Optical image of the pMUT monolithically integrated on CMOS circuitry. The zoomed figure is focused on the M6 CMOS metal layer to clear visualize the different depth between pMUT and CMOS front end circuitry.

4.2.1 Integrated system vs Non-integrated system

The validation of the proposed system has been carried out using Fluorinert as an acoustic propagation medium, FC-70 (3M Company, c=685 m/s, ρ=1940 kg/m^3)[127], and the results have been compared with the non-integrated system in order to demonstrate the benefits of monolithic integration. Figure 4.8 depicts the schematic set-ups used to characterize the non-integrated (Fig. 4.8 *a*), and the integrated (Fig. 4.8 *b*) systems, respectively. In the first one, the pMUT and LNA amplifier are bonded on separated PCBs, and only the pMUT is immersed in the fluid, while in the second one, the pMUT and CMOS are in a single chip which is bonded to a PCB and immersed in FC-70. The acoustic pressure was generated by a commercial transducer from OPTEL which has been previously calibrated.

The "End-of-cable sensitivity" (SR_{EOC}) of the pMUT device is affected by all parasitic capacitances that interfere in the acoustic measurement and it can be defined through Eq. 4.6 [134]. From this equation, SR represents the receiving sensitivity being equal to V_{OUT}/P_{in} (where V_{OUT} is the acquired

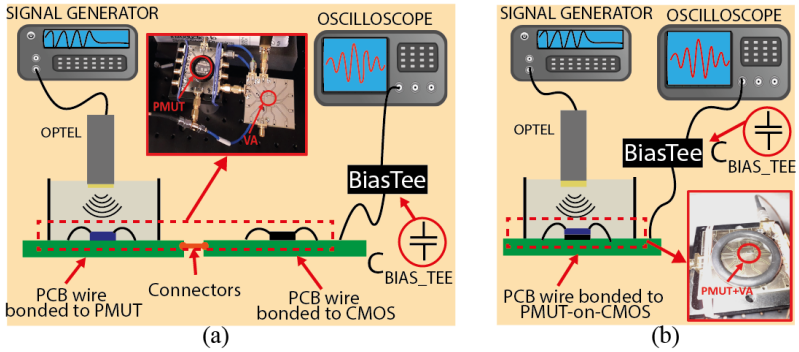


Figure 4.8: Set-up for the pMUT acoustic characterization as sensor in liquid environment: (a) non-integrated system and, (b) integrated system [109].

peak-to-peak voltage at the LNA+Buffer output and P_{IN} is the acoustic peak-to-peak pressure on the pMUT surface),G is the LNA+Buffer gain (21.5 dB), C_{INNER} is 262 fF, C_{inLNA} is 609 fF, and $C_{\mathrm{parasitic}}$ gives 6.5 pF and 0 pF for the NIS and IS, respectively.

$$SR = SR_{EOC} \cdot G \cdot \frac{C_{INNER}}{C_{INNER} + C_{inLNA} + C_{parasitic}} \tag{4.6}$$

Considering the non-integrated system, the OPTEL was driven at 2.4 MHZ with four cycles of 5 V_{pp}, which represents a pressure of 3 kPa_{pp} on the pMUT surface. Under these conditions, the peak-to-peak voltage acquired is about 8 mV_{pp}, giving an SR of 2.67 V MPa^{-1}. Based on Eq. 4.6, the SR_{EOC} gives $\sim$ 6.4 V MPa^{-1}. Comparing the SR and SR_{EOC} there is a 42% degradation in the intrinsic pMUT sensitivity as a consequence of the loaded capacitances. On the contrary, using the fully-monolithic integration, these ones are avoided, which should improve the behavior of the ultrasound system. In this context, Fig. 4.9 shows the received signal when the input acoustic pressure ranges from 0.03 kPa_{pp} to 13 kPa_{pp} (the OPTEL was driven at 2.4 MHz, and amplitude voltages from 50 mV_{pp} to 20 V_{pp})). As it can be seen, the minimal detectable pressure is around 60 Pa_{pp} being mainly limited by the integrated noise in the readout oscilloscope bandwidth (20 MHz). The receiving sensitivity was computed considering a linear fit from 300 Pa^{pp} to 3 kPa^{pp} giving 22.6 V MPa^{-1}. Compared with the non-integrated system, an improvement of the factor 8.5$\times$ is achieved, which corresponds to Eq. 4.6 MHz assuming as the only difference the presence of the $C_{\mathrm{parasitic}}$. In addition, the highlighted P1-

dB compression point with a value of 5.25 kPa_{pp} represents the maximum acoustic pressure detected by the system without clamping. Note this value is limited by the source follower output buffer since this topology behaves as a voltage level-shifter and in order to achieve an output resistance of 50 Ω, the DC output voltage is substantially lower than VDD. Based on these results, the input dynamic range, represented as the ratio between the maximum and the minimum acoustic pressure, gives around 55 dB.

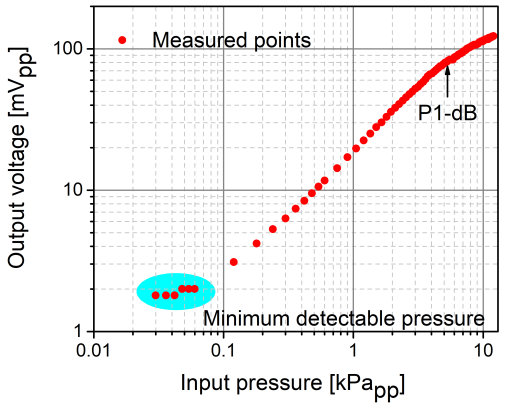


Figure 4.9: Dynamic range of the pMUT-on-CMOS system as a sensor [107].

The SNR analysis was first performed by implementing a 6^{th}-order Butterworth passband filter in MATLAB over a frequency range of 1.9 MHz to 2.9 MHz (considering the pMUT central frequency and bandwidth of 2.4 MHz and 1 MHz, respectively [109]). Figure 4.9 inset depicts the filtered time-response for the non-integrated (blue line) and integrated (red line) systems. Taking an interval time away from the echo, the output-referred integrated noise gives 46 μV_{rms} for IS and 111 μV_{rms} for NIS that corresponds to an input-referred integrated noise of 3.87 μV_{rms} and 9.34 μV_{rms} respectively. With these values and considering the pMUT sensitivity when is loaded by the LNA (1.9 $VMPa^{-1}$), the input-referred pressure noise spectral density averaged inside the passband are 2.04 $mPa/\sqrt{Hz}$ and 41.57 $mPa/\sqrt{Hz}$ respectively, which demonstrates that the IS can detect signals 20.34× factor lower than NIS. Likewise, the rms output signal, using only the echo part of the time-response, can be obtained approximately as $V_{max}/\sqrt{2}$. Taking into account this, the SNR was computed for the IS, see the red dots in Fig. 4.10, when the applied pressure ranges between 300 Pa_{pp} and 3 kPa_{pp}, ensuring values from 30 dB to 50 dB. Fur-

thermore, compared to the NIS when the applied pressure is 3 kPa_{pp} (Fig. 4.10 blue square), the integrated system achieves an improvement of 27 dB, demonstrating a good agreement with the expected value based on Fig. 4.5 ($F_{SNR} = 20 \cdot log(F_s \cdot F_n) \approx 26\ dB$ using F_s=8.5 and F_n=2.3). This difference can be minimized if the parasitic capacitances in the non-integrated system are decreased, for instance, by bonding the LNA in the same PCB as the pMUT. All experimental results clearly show that the monolithic integration of the pMUT on CMOS enhances the signal (due to the reduction of parasitic capacitance) and reduces the noise, improving the overall SNR.

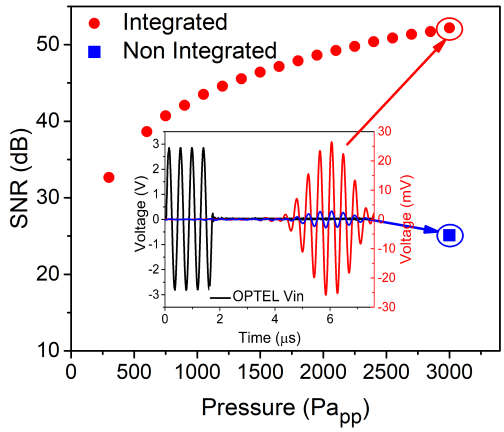


Figure 4.10: Measured signal-to-noise ratio as a function of applied pressure. Inset: Time domain response for integrated (red) and non-integrated (blue) [109].

4.2.2 pMUT-on-CMOS pulse-echo verification

The capability of the pMUT-on-CMOS as a single ultrasound system was demonstrated using the set-up shows in Fig. 4.11. The transmitter input signal consists in four monophasic pulses at 2.4 MHz with 3.3 V amplitude and the interface between air and FC-70 is used as reflecting surface.

For the first experiment no decoupling capacitor was used between output buffer and oscilloscope in order to avoid slow charging and discharging of this capacitance when the switches change state. This fact results in a variation of the output buffer biasing point that changes its output resistance to 21 Ω. Considering these new conditions the overall gain of the receiver amplifier (LNA+ Buffer) is 25.5 dB. Taking into account this gain and based on the fact

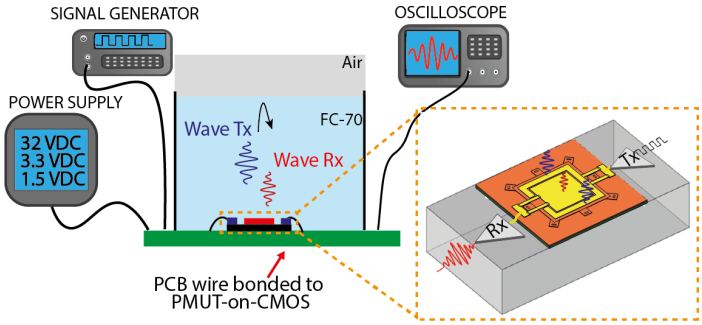


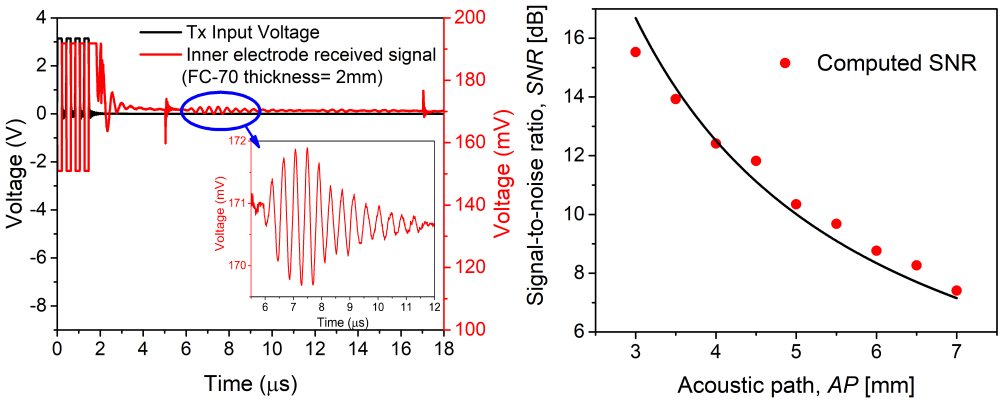
Figure 4.11: Set-up for single TX/RX pMUT-on-CMOS in liquid environment.

that the system is the same as the previous one (i.e. the switches do not affect the parasitic capacitances) the receiving sensitivity was obtained, giving 35.7 V MPa^{-1}.

Figure 4.12a depicts the received signal by the inner electrode when the acoustic path is 2 mm. Note how the crosstalk effect decreases by a factor of 410× reaching up to 2 mV_{pp} (41 mV_{pp}/25.5 dB) with respect to the estimate in the theoretical analysis (820 mV_{pp}). As mentioned above, the signal-to-noise ratio was obtained filtering the time-response with the same band-pass filter. In this case, the output-referred integrated noise gives 116 μV_{rms}, and considering the system gain gives an input-referred integrated noise of 6.2 μV_{rms}. Based on the input-referred integrated noise without isolation switches, here, the system is 1.6 times noisier. In order to quantify theoretically the influence of the isolation switches in the equivalent input-referred voltage noise, the second term of the Eq.4.5 was computed giving $\sim$ 4.1 μV_{rms}. The thermal noise ($\overline{V^2_{n,Rsw1}}$) can be defined as $4kTR\Delta f$ and gives 13.5 μV^2 where k is the Boltzman's constant, T is the temperature (300 K), R is the ON resistance of the switch (R=11 kΩ), and Δf is the pMUT bandwidth (1 MHz). Considering the difference between the experimental equivalent input-referred power noise with (Eq. 4.5: $\overline{V^2_{n,IN}} = 6.2^2 \mu V^2$) and without (first term of Eq. 4.5: $3.87^2 \mu V^2$) isolation switches, the input-referred voltage noise as a consequence of the isolation switches gives around 4.8 μV_{rms}, demonstrating a good agreement with the theoretical one (4.1 μV_{rms}).

The signal-to-noise ratio was computed considering the measured rms output voltage ($2.4\, mV_{pp}/(2\sqrt{2}) = 0.85\, mV_{rms}$) and the output-referred integrated

voltage noise (116 μV_{rms}), giving 17.3 dB which ensures the minimal value to obtain an accurate fingerprint images. Likewise, it is important to analyze the behavior of the system taking into account the noise of the acoustic medium. This one can be represented as $\sqrt{4kTR_{medium}\Delta f \cdot S^{-1}}$ where R is the acoustic medium resistance (1.35 MRayls in FC-70), S is the pMUT effective area ($80\mu m^2/3$), and the rest of the parameters have been mentioned above. Considering the result, 3.25 Pa_{rms}, and the pressure on the pMUT surface, 23.7 Pa_{rms} ($0.85/35.7 = 23.7Pa_{rms}$), the pMUT-on-CMOS system achieves a pressure of 7.3 times than the acoustic noise, allowing a successful measurement. Finally, based on the output-referred integrated voltage noise and the receiving sensitivity (35.7 V MPa^{-1}), the equivalent pressure noise spectral density gives 3.26 $mPa/\sqrt{Hz}$ at 2.4 MHz.



(a) (b)

Figure 4.12: Pulse-echo experiments: (a)Time domain pulse-echo response using the single TX/RX pMUT system (without decoupling capacitor) (b) Signal-to-noise ratio dependence with the acoustic path when the reflected surface is the FC-70-air interface (with decoupling capacitor).

In the second experiment, the decoupling capacitor was used between the output buffer and the oscilloscope, and the acoustic path (in FC-70) was modified giving round trips from 3 mm to 7 mm. Using the rms voltage measured at each point and the aforementioned output-referred integrated noise (116 μV_{rms}), the signal-to-noise ratio (SNR) was computed. Figure 4.12b shows the dependence of the SNR and the acoustic path. From these results, SNRs higher than 12 dB are guaranteed for acoustic paths less than 4 mm, demonstrating a good performance for a single pixel imaging with only one transducer.

4.2.3 System level comparison with the state-of-the-arte

The end of this chapter is dedicated to compared the discussed pMUT-on-CMOS system with and without isolation switches with the state-of-the-art, see Table 4.2. The principal Figure-of-Merit defined to compare with prior works was the noise-efficient factor written as $NEF' = P_{n,in}\sqrt{Power}$ [74]. From the results, the pMUT-on-CMOS without isolation switches achieves a NEF' close to the lowest [135], and lower to the rest of the works (either based on CMUTs [74], [88], pMUTs [136] or based in PZT [117]) demonstrating the benefits of the monolithic integration. Based on other parameters included in Table 4.2, the ultrasound system reported in [135] detects 4.7 times smaller signals (considering the same bandwidth, 1 MHz), however, the power consumption increases 16.3 times.

Focusing on the bonded system based on pMUTs [137], our monolithic approach achieves a lower NEF' as a consequence of the competitive values regarding RX sensitivity, circuitry noise, and power. In addition, taking into account that this system [137] was used to obtain a fingerprint image, and based on the results achieved by our pMUT-on-CMOS, we can conclude that our proposal will be able to implement a fingerprint sensor with less fabrication complexity and cost (avoiding, for instance, the need of an eutectic bonding between piezoelectrical layer and CMOS integrated circuit, which increases complexity and decreases the achievable fill factor).

From the results exhibit in Table 4.2 the pMUT-on-CMOS system fabricated with the Silterra platform only adds some post-processing steps (including deposition of the AlN layer) similarly as is done for CMUT approaches [88]. The monolithic approach, as it has been explained in Chapter 1, has a less complex and cheaper fabrication process without special equipment to align the CMOS and MEMS chips like in the flip-chip approach shown in [74], [135]. Furthermore, it does not require to use an inter-layer conductive glue between PZT and the CMOS integrated circuit (as it is done in the direct interconnection process reported in [32], [117]).

Table 4.2: System level comparison with the state-of-the-art.

	This work		[135] (2020)	[117] (2018)	[74] (2016)	[14] (2016)	[88] (2011)
	w/o switches	With switches					
Process	0.13 μm HV CMOS		0.18 μm BCDMOS	0.18 μm HV CMOS	0.18 μm HV CMOS	0.18 μm HV CMOS	0.35 μm CMOS
Transducer	pMUT,AlN		CMUT	PZT	CMUT	pMUT,AlN	CMUT
Integration method	Monolithic		Flip - chip	Direct Interconnection[2]	Flip - chip	Eutectic bonding	Monolithic
Acoustic medium	FC-70		Tissue Phantom	Water	Vegetable oil	PDMS	Water
Transducer bandwidth (MHz)	1		N/A	6	N/A	4.67[4]	10
Max. TX Amplitude (V)	N/A	32	N/A	30	30	24	N/A
Overall RX Voltage-Voltage Gain (dB)	21.5	25.5	N/A	N/A	N/A	34	N/A
Overall RX Transimpedance Gain (dBΩ)	119[9]	123[9]	106	108//119	104//116	N/A	130
Overall RX area(10^{-4} mm^2)	6		1200	N/A	600	N/A	98
RX Sensitivity IN (pMUT+LNA)(V MPa^{-1})	1.9		N/A	4	N/A	0.344	N/A
RX Sensitivity OUT (pMUT+LNA)(V MPa^{-1})	22.6	35.7	N/A	N/A	123	17.2[5]	130
Input Referred Voltage noise (LNA)(nV/$\sqrt{Hz}$)	3.87@2.4 MHz	6.2@2.4 MHz	N/A	N/A	N/A	21@14 MHz	N/A
Input Referred current noise (LNA)(fA/$\sqrt{Hz}$)	50.8@2.4 MHz[10]	81.4@2.4 MHz[10]	2000@5 MHz	2000@13 MHz	410@ 5MHz	N/A	90@15 MHz
Input Referred Pressure noise ($P_{n,in}$)(mPa/$\sqrt{Hz}$)	2.04@2.4 MHz	3.26@2.4 MHz	0.43@5 MHz[1]	1.9@13 MHz[1]	2.3@5 MHz	61.88@14 MHz	3@15 MHz
Power Consumption(mW)	0.3		4.9	0.42	1.4	1.86[7]	6.6
NEF'(mPa/$\sqrt{Hz}\cdot\sqrt{mW}$)	1.12	1.79	0.96	1.23[3]	2.72	84.39[8]	7.71[8]

[1] Computed using the power consumption and NEF'.

[2] The bond pads on the ASIC provides electrical connections to the transducer elements [32].

[3] According with the reported value in [135].

[4] Computed using BW = f_0/Q where Q is the Quality Factor in PDMS (Q $\sim$ 3) and f_0 is the resonance frequency (14 MHz).

[5] Considering the reception sensitivity at the LNA input (0.344 V/MPa) and the overall gain of the receiver chain (34 dB).

[6] Computed using the input voltage reference noise (46 μV_{rms}), the estimated bandwidth (4.67 MHz) and the reception sensitivity at the LNA input (0.344 V/MPa).

[7] Including the overall receiver chain (computed using the consumed energy per column (2.4 μJ) and the full readout sequence per column (2.64 ms).

[8] Computed using $NEF' = P_{n,in} \cdot \sqrt{Power}$ where $P_{n,in}$ is the input referred noise (mPa/$\sqrt{Hz}$) and the LNA power consumption.

[9] Computed using G_{TIA}[dBΩ] = G[dB]-20*log10(2*π*f_0*(C_{INNER}+$C_{in,LNA}$)), where G[dB] is the Overall RX Voltage-Voltage Gain and f_0 is the resonant frequency (2.4 MHz).

[10] Computed using $i_{n,IN} = V_{n,IN} \cdot 2 \cdot \pi \cdot f_0 \cdot (C_{INNER} + C_{in,LNA})$, where $V_{n,IN}$ is the input referred voltage noise [V/$\sqrt{Hz}$].

CHAPTER 5

Phased Array Based on AlScN pMUTs Monolithically Integrated on CMOS

In the previous chapters, the designs of the key functional blocks of the analog front-end circuitry for pMUT transducers, i.e. a High Voltage (HV) Pulser, a Low Voltage (LV) Low-Noise Amplifier (LNA), and a LV Time-Gain Compensation (TGC) Amplifier, have been realized. In this chapter we present an ultrasound system, which was designed using the aforementioned building blocks. The proposed system is based on the monolithic integration of the 7x7 AlScN pMUT array over the analog front-end CMOS circuitry. The beamforming technique has been implemented on both the transmitting and receiving sides, resulting in a fully integrated phased array ultrasound transceiver. A complete characterization of the proposed system is presented. Measurement results demonstrate the effective functionality of the proposed system for making B-mode ultrasound images. This chapter is based on the published paper cited as *I. Zamora, E. Ledesma, A. Uranga, and N. Barniol, "Phased Array Based on AlScN Piezoelectric Micromachined Ultrasound Transducers Monolithically Integrated on CMOS," IEEE Electron Device Lett., vol. 43, no. 7, pp. 1113–1116, doi:10.1109/LED.2022.3175323, 2022.*

5.1 System Architecture Overview.

Figure 5.1a shows an overview of the proposed system. It consists of an analog front-end ASIC with an array of 49 pMUT devices based on Aluminum-Scandium-Nitride (AlScN), monolithically integrated on top of the ASIC. A

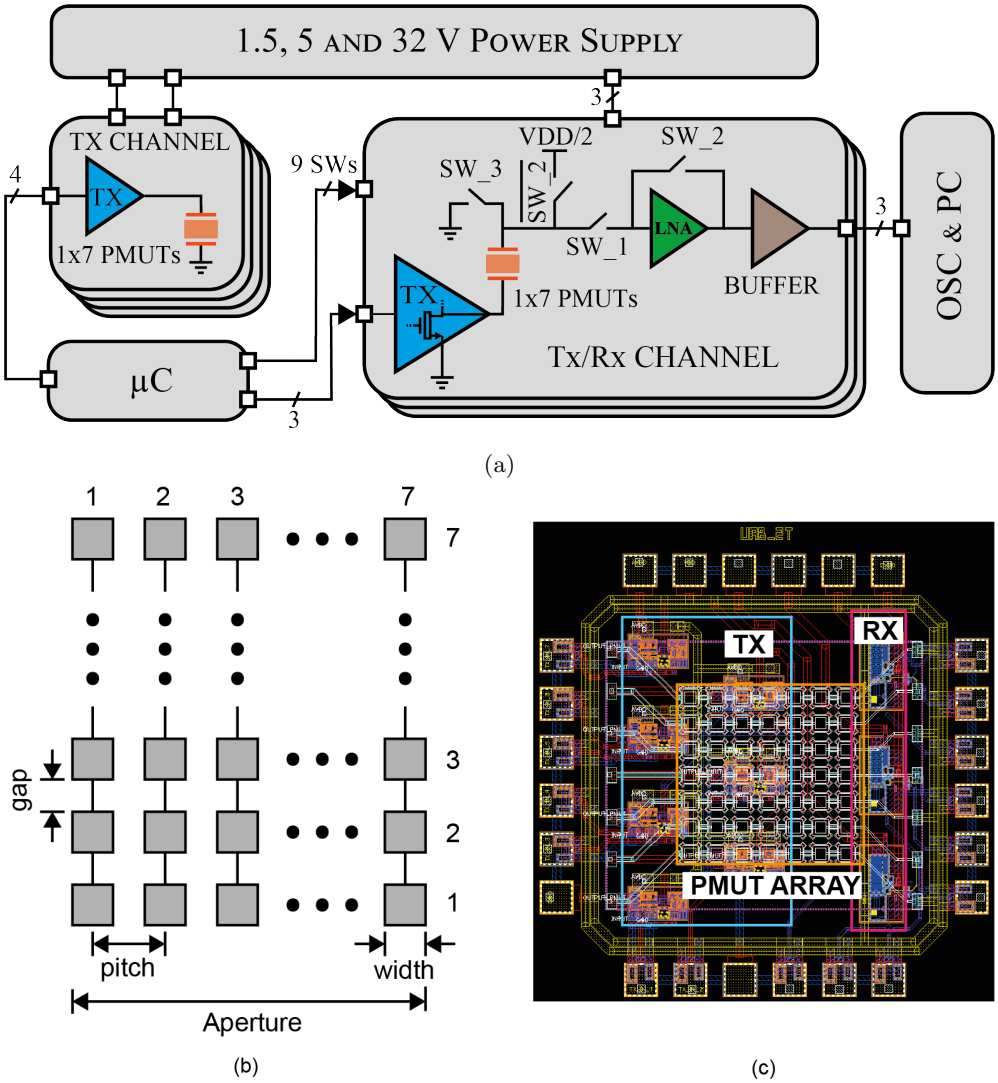


Figure 5.1: (a) Diagram of the system used to drive the 7×7 pMUT array in a 7 channel configuration (7×1 PMUTs connected in parallel) with 4 TX channels and 3 TX/RX channels, and (b) Diagram of the pMUT array configuration, and (c) Layout of the PMUT-on-CMOS array.

diagram of the pMUT array configuration used in this work is presented in Fig. 5.1b. The array element is a square shaped pMUT with 40 μm side (element width). It has two Al electrodes (top and bottom) that are used to sense and excite the device. The transducers exhibit a resonant frequency around 7 MHz immersed in liquid (fluorinert FC-70 [127]). In this system, every seven pMUT elements in the same column are connected together in parallel, in order to reduce the overall IN/OUT (I/O) count, saving silicon area and power consumption. Thus, the 7x7 pMUTs array is turned into 1-Dimension phase array with a broad beam profile in elevation direction. The proposed pMUT array measures 430 μm x 430 μm, with an element pitch of 65 μm, and a gap of 25 μm.

The transceiver chip includes seven channels (four TX-only channels and three TX/RX channels). In each channel, a 32 V_{pp} High Voltage (HV) Pulser, proposed in [110] and explained in Chapter 2, drives seven pMUT transducers to emit acoustic energy to the surrounding medium. In each TX/RX channel, in addition to the TX circuit, the LNA amplifier proposed in [110] and presented in Chapter 3, is used to amplify the weak signal generated by seven pMUTs in respond to an impinging ultrasound wave. The LNA circuit used in this system is the open-loop single-ended voltage amplifier described in Chapter 3. An arrangement of four low-voltage switches on the received side are used to protect the LNA during a transmission event. These switches are part of one of the main functional blocks of an ultrasound system, which will be explained below. The final layout of the proposed system is shown in Fig. 5.1c, , where the main blocks are highlighted: Transmitter, Receiver, and pMUTs. As can be seen, the CMOS circuitry is below the pMUTs.

As a proof of concept, the proposed system has intended to reconstruct a B-mode ultrasound image of a given phantom, in order to demonstrate its imaging capability. To implement this, the system shown in Fig 5.1a, realizes the beamforming technique in both transmission and reception operations. Transmit beamformation is realized by controlling and applying different delays to the seven channels. To generate the waveform of the excitation signals with their corresponding delays and the gate signals of the switches, we use the microcontroller STM32H743ZI (μC block in Fig 5.2a) [138]. The received signals at the output of the three TX/RX channels are collected by an oscilloscope (OSC), and in a similar fashion to the TX beamforming, a RX beamforming is

implemented in a Personal Computer (PC). All DC voltage levels are supplied by external sources.

5.1.1 Protection schemes for the receive circuitry.

Most ultrasound systems are able to realize both the transmitting and the receiving operations, with which they can be considered as transceiver devices. Typical implementations of this can be using a part of the ultrasound array to transmit and another section to receive [33], [90], [117], [124] or using the same array elements to transmit and receive the ultrasound signals [26], [51], [52], [62], [70], [71], [74], [104], [118]. The implementation of the transmitting and receiving operation by separated sectors of the array requires that fewer transmitter circuits and fewer amplifiers are needed, resulting in a reduction of the power consumption and area of the ASIC [33]. However, since only one sector of the array is dedicated to either transmission or reception, the active area is reduced, an as consequence the lateral resolution and the SNR are affected. In contrast, when the full array is used to transmit and receive the ultrasound signals, the active aperture is increased and therefore, the lateral resolution and the SNR are maximized. Nevertheless, when the same element of the array realizes the transmitting and receiving operations, is necessary to design a protection/switching circuit to isolate the low voltage RX circuitry from the high voltage driving signal. This causes an increase in system complexity and affects noise performance in the receive chain [90].

As was explained in Chapter 1, either conventional piezoelectric transducers as MUT devices contain two terminals. With the exception of the ultrasound systems that separate the transmit elements of the receiving ones, the most of the ultrasound arrays are fabricated in such a way that one of the terminals of each element is connected to a common connection (usually to ground), while the another terminal is inevitably shared by both the transmit and the receive circuitry.

Figure 5.2a illustrates one of the most used schemes to isolate the RX circuitry during the TX operation [26], [52], [62], [70], [71], [118]. It uses two HV switches, which must be operate in opposition. In some designs, the HV SW1 can be embedded in the output stage of the TX circuit [62], [70], [71]. This protection scheme although is very used in ultrasound systems, requires of HV

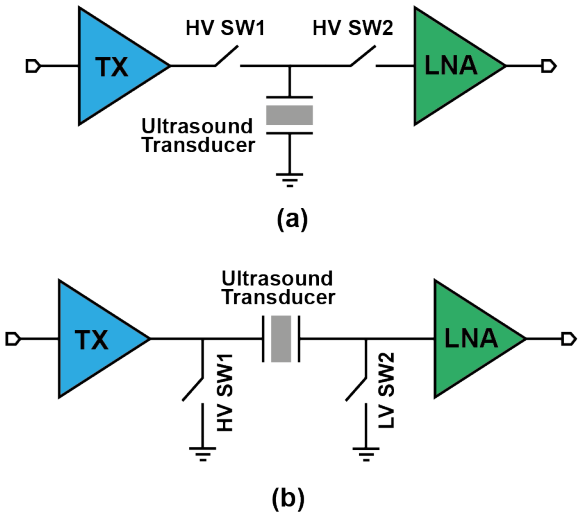


Figure 5.2: Block diagram of LV RX circuitry protection schemes. (a) When all elements of an ultrasound transducers array have a common node (ground), and (b) When there is no a fixed ground node on one side of the transducers.

transistors to implement the HV Switches, which occupy a large silicon area, need HV gate signals, and introduce large parasitic capacitance.

In this thesis we adopt the protection scheme shown in Fig 5.2b. This scheme has been previously implemented by [16], [139]. As can be seen, in this case, the array elements do not share any common node, and therefore they can be used as isolation element between the transmit circuit and the receive circuit. During transmission the HV SW1 is opened and LV SW2 is closed, allowing the ultrasound transducer to be driven with amplitude pulses from HV power supply to ground. Due to, the TX and RX circuits are isolated by the transducer element itself, LV SW2 can be implemented in standard CMOS process. LV SW2 can be implemented with a wide nMOS transistor and close to the minimum length, in order to create low enough impedance to ground during a transmit event.

During receive mode, LV SW2 is turned off while HV SW1 is turned on, creating a low impedance to ground on the transmit side, which allows that the received echo signal to appear at the input of the LNA circuit. In this case, due to HV SW1 is on the TX side, it must be implemented in HV CMOS process.

For the proposed system, the HV SW1 in Fig 5.2b is implemented by the

HV nMOS pull-down transistor of the HV Pulser's output stage. The LV SW2 of the Fig 5.2b is implemented by a LV nMOS transistor SW_3, which shunts the current to ground during TX operation. This transistor was dimensioned with aspect ratio of $60\mu m/0.3\mu m$, obtaining an ON-resistance in the range of unit of Ωs. The other three LV switches are used to fasten the LNA biasing recovery, avoiding undesirable peaks. The time diagram for one transmission and reception cycle is illustrated in Fig 5.3.

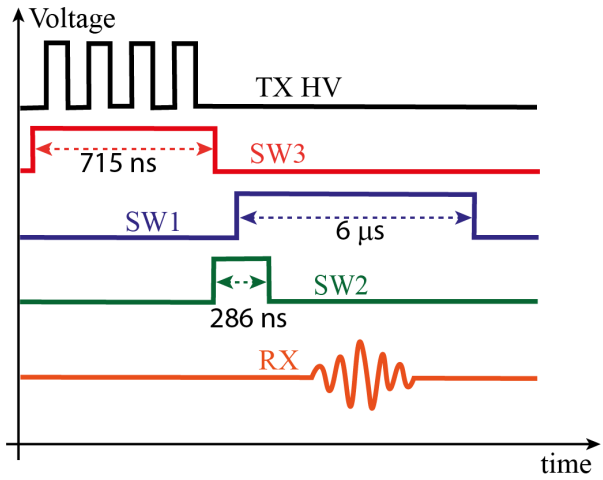


Figure 5.3: Time diagram for one cycle of transmission and reception.

5.1.2 B-mode ultrasound image.

One of the most popular application of the ultrasound technology is the imaging reconstruction. Once information about a spatial region that has been examined by ultrasound system is acquired and processed, there are some modalities to display it. The most commonly used ultrasound imaging modes today are: Amplitude-mode (A-mode), Brightness-mode (B-mode), Motion-mode (M-mode) and Doppler-mode [53]. As a proof of concept, in this thesis we focus on reconstructing a B-mode ultrasound image, in order to demonstrate the capability of the proposed system for imaging applications.

A B-mode image is a cross-sectional image, in which can be represented tissues, organ boundaries, material interfaces, etc, see Fig 5.4a. It is constructed from the returning echoes, which are displayed as of varying intensities. The

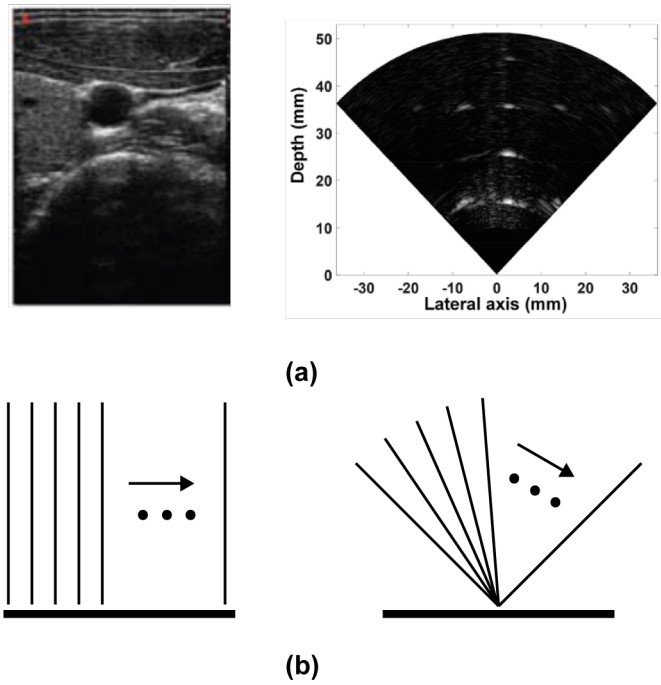


Figure 5.4: Representation of the ultrasound information using B-mode image format. (a) B-mode images of: left carotid artery [47], and right 10 nylon wires [71]. (b) Scan line arrangements of the scan process for: left B-mode linear format, and right B-mode sector format.

intensity of a dot (the brightness) is related to the strength or amplitude of the echoes, such that strong echoes appear as bright points, while echoes received from deep penetrating depth appear as dark. The position of a dot is a measurement of the distance between the reflector target and the transducer, in the beam direction. For a given beam direction, a line of dots is displayed, which is referred to a scan line. When the ultrasound beam is swept across the interest region (scan process), multiple scan lines are created. Usually, the scan process is a sequential process, where the N scan line is launched in the next incremental direction after the previous pulse-echo sequence (N-1 scan line) had completed its necessary round-trip time.

Figure 5.4b shows two different scan line arrangement for B-mode format, illustrating the scan process. In Fig 5.4b left the beam is progressively displaced along the array generating a new image line at each position, while in Fig 5.4b right the next line is incremented by steering the beam with small angle steps [73]. After the scan process has been completed, the generated scan lines

are combined to provide a 2-D image, where one dimension is relative to the penetration depth, while the another dimension represents lateral variations in the direction of the beam sweep.

In this chapter, a B-mode image will be made following the scheme presented in Fig 5.4b right. Before constructing it, is very important to know what is the maximum steerable angle of the proposed system. In this context, when several single transducers are spaced and arrangement to form an array, the generation of grating lobes can occur. The grating lobes are replicas of the main lobe but wider, and they appear in the wave field at certain angles on each side of the main lobe [140]. Their appearance causes a beam widening effect, which degrades the lateral resolution, and contributes to the generation of spurious echoes [141]. The condition to avoid their generation has a strong dependence with the geometric of the array's element, the propagation medium, and the steering angle. The maximum steerable angle to completely eliminate the grating lobes can be determine by the following equation [141]:

$$(\theta_s)_{max} = \sin^{-1}\left(\frac{\lambda(N-1)}{d \cdot N} - 1\right) \tag{5.1}$$

where N is the number of elements in the array, d is the inter-element spacing or pitch (between center-to-center of two adjacent active elements), $\lambda = c/f$ is the wavelength, being f the operation frequency, and c the wave-speed.

Considering this, the maximum steerable angle of the proposed system, which operates at 7 MHz in fluorinert FC-70 ($c = 685m/s$), and seven ac-

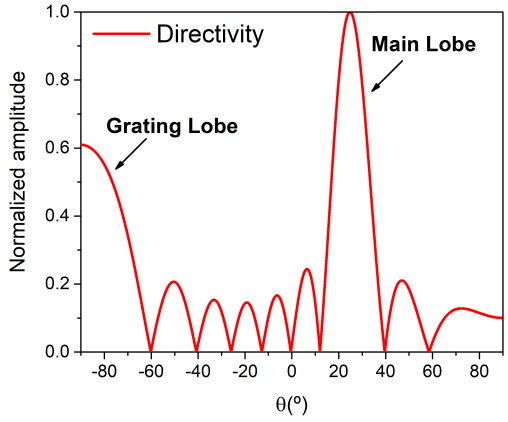


Figure 5.5: Directivity computed when the steering angle is 25 °.

tive elements are used to transmit, separated by 65 μm, is $\pm 17°$. However, in order to increase the field of view, we have steered the beam at a maximum of 25°. Figure 5.5 shows the directivity of the proposed array when the beam has been steered 25°. From the result, the first-order grating lobe appears at 90°, which is outside the area of interest to be imaged.

5.2 Simulation Results

The simulation results discussed throughout this section were carried out with the ultrasound simulation software, Field II [142]. This program is based on numerical analysis, and runs under MATLAB, hence it is widely used in the literature.

5.2.1 Time delay estimation.

In order to provide the beamforming technique to steer and/or focus the ultrasound beam, several time delay are required to compensate the different acoustic paths between each TX/RX channels and the target point to be imaged. When is desired to steer the ultrasound beam but not focusing is required, the time delay for the adjacent TX/RX channel can be derived from Fig 5.6. Due to the front wave of the generated acoustic wave is plane when no focusing is applied, the time delay between adjacent elements is constant, and can be obtained by following equation [143]:

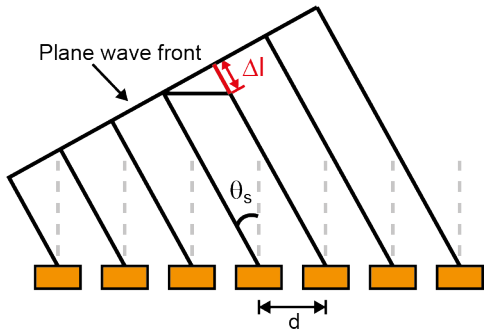


Figure 5.6: Steering delay for a Plane Wave.

$$\Delta t = \frac{\Delta l}{c} = \frac{d \cdot \sin \theta_s}{c} \tag{5.2}$$

where Δl is the difference acoustic path between two adjacent channels, d is the element pitch, θ_s is the required steering angle, and c is the speed of the sound.

When focusing technique is applied, the delay time required for each TX/RX channel can be obtained from Fig 5.7. In this case a spherical timing relationship is applied to a linear array to steer and focus the ultrasound beam at a given focal point. A general solution to determine the required element focusing delays for an array, composed by even or odd elements was proposed by [143], and is rewritten as Eq. 5.3:

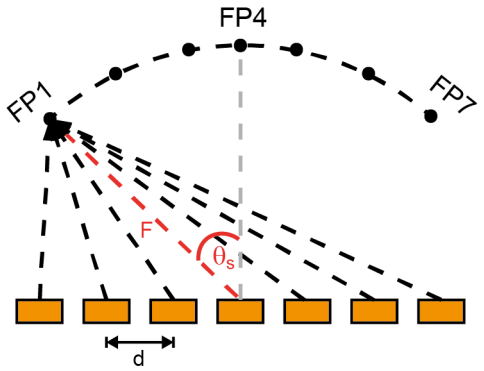


Figure 5.7: Focusing and steering delay.

$$t_n = \frac{F}{c}\left\{\left[1+\left(\frac{\bar{N}d}{F}\right)^2+\frac{2\bar{N}d}{F}\sin\theta_s\right]^{1/2} - \left[1+\left(\frac{(n-\bar{N})d}{F}\right)^2-\frac{2(n-\bar{N})d}{F}\sin\theta_s\right]^{1/2}\right\} \tag{5.3}$$

where t_n is the required time delay for element $n = 0, ..., N-1$, F is the focal point, c is the speed of the sound, d is the pitch element, $\bar{N} = (N-1)/2$, being N the number of elements in the array, and θ_s is the steering angle.

5.2.2 TX Beamforming scheme.

In Chapter 1 of this thesis has been explained that the shape of the ultrasound beam has a great significance in ultrasound imaging application. As was

explained, the size of the transducer, the beam frequency, and the beamforming technique implementation have a great influence in the ultrasound beam. Considering this, in this section different transmission schemes that can be implemented with the proposed system have been studied, in order to choose the most optimal for reconstructing a B-mode image in far-field region. In this analysis, we have considered the most commonly parameters used to measure the quality of an image: resolution and contrast [144]. The image resolution has a strong dependence with the spatial resolution of the transducers, while image contrast is related with the dynamic range, which in turn, as explained in Chapter 3, has a strong dependence with the SNR at different depth.

Figure 5.8 shows the four transmission schemes that have been analyzed. In Fig 5.8a only one TX channel is used to emit the acoustic pressure. The sense to transmit with a small aperture is to emit a wide acoustic beam in order to illuminate a large volume in the space. The second studied approach is represented in Fig 5.8b, where a sub-aperture is used to transmit the acoustic field. Similarly to the first one, we have chosen only three channels to emit a wide acoustic beam, but increasing the emitted field intensity. Figures 5.8c and d use the total array aperture to transmit the acoustic pressure, and in both, the beamforming technique is implemented. For the scheme represented in Fig 5.8c no TX focusing is implemented, and as consequence a plane wave is emitted. For this case the beam is steered from -25°to 25°. In the scheme represented in Fig 5.8d the ultrasound beam is both focused and steered. Since the near-field distance for this case (obtained from Field II simulation) is around 615 μm, the focal point was defined at 500 μm, and the same beam steering scheme applied in Fig 5.8c was used.

Figure 5.9 illustrates the simulated lateral resolution for each of the analyzed schemes, as a measured of the beam-width at -6 dB (BW_{-6dB}), in a direction perpendicular to the transducer's aperture. As was expected, to transmit with only one channel causes the emission of the widest beam, and as consequence the worst performance in terms of lateral resolution. The best performance in far-field region is achieved when the full aperture is used to transmit, and no focusing is applied, black curve in Fig 5.9. The results shown by green curve illustrate that when the focusing is applied, the lateral resolution is improved during the focal depth, distance from the aperture's center to the point where constructive interference occurs, being in this case 500 μm. However, this

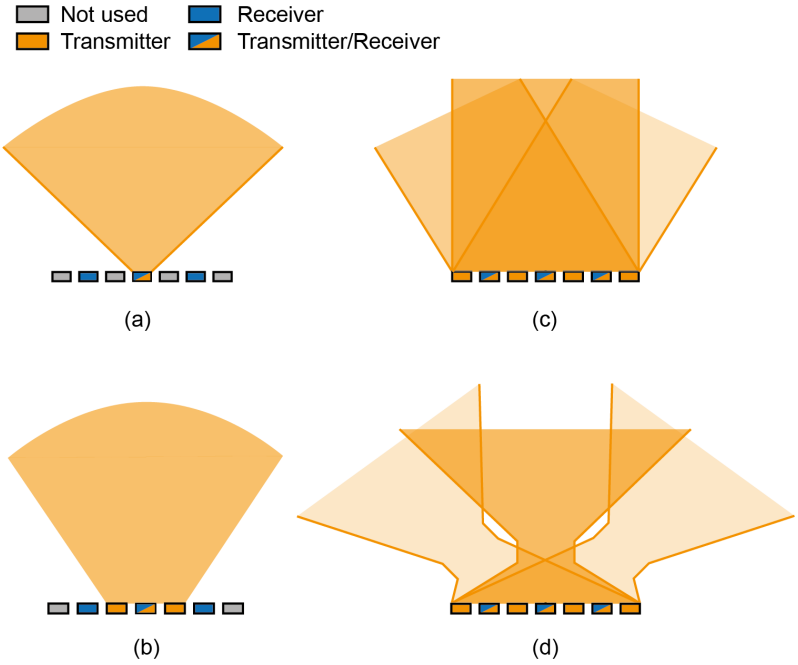


Figure 5.8: Transmission schemes analyzed in this thesis. (a) single TX element, (b) three TX elements, (c) full TX aperture (7 TX channels) to emit and steered a plane wave, and (d) full TX aperture to focus and steer the ultrasound beam.

causes the ultrasound beam to start diverging before the beam when no focus is applied, with the same divergence angle. In this case, in the far field region, the beam is wider and the lateral resolution deteriorates.

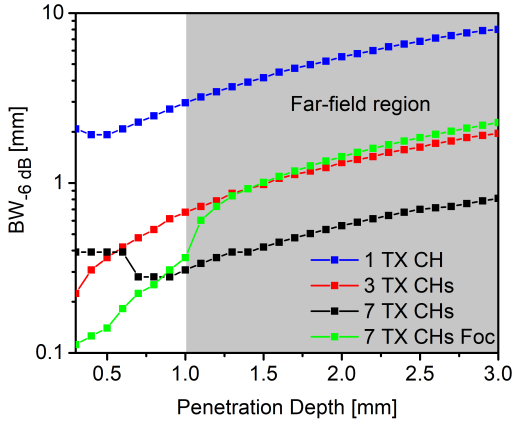


Figure 5.9: Simulated full width of the beam at half maximum ($BW_{-6\ dB}$) for the four analyzed TX schemes.

A similar result to the illustrated in Fig 5.9, has been obtained for the strength of the emitted acoustic field. Figure 5.10 shows the normalized ultrasound pressure along the axial distance for the four analyzed TX schemes. As was expected too, while fewer channels are dedicated to transmit, lower pressure level will be emitted to the media. On the other hand, when the focusing is applied, the pressure level is maximized at focal point, but the attenuation due to the spread of the ultrasound wave in far-field region begins before that when no focusing is used. Based on this, the Signal-to-Noise ratio for penetration depth in far-field region is improved when the full aperture is used to emit and no focusing technique is applied.

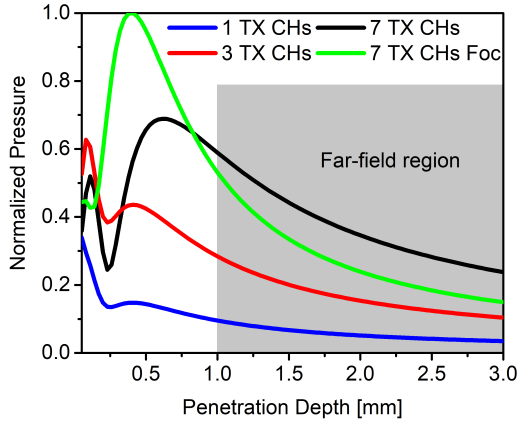


Figure 5.10: Simulated normalized pressure along axial distance.

5.2.3 B-mode ultrasound images simulation results.

On the reception side, the same RX scheme has been implemented for the four TX approaches mentioned above. It consists on simultaneously receiving with the three available RX channels, and then to apply the respective delays to implement both the focusing and steering with a focal point. Figure 5.11 shows a representation of the RX beamforming scheme where the d is the pitch between receiver elements (130 μm) and F is the focal point (2.1 mm).

To validate the aforementioned results, four B-mode ultrasound images have been reconstructed, corresponding to the four analyzed transmission schemes. In Field II software, two square scatters of 300 μm of side, have been defined at positions over the transducer's array. One scatter was defined with coordinates

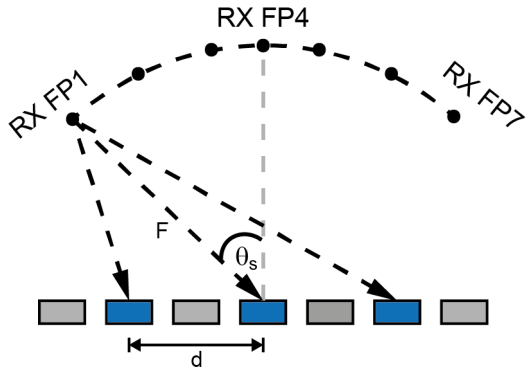


Figure 5.11: Received focusing and steering delay for the proposed ultrasound system.

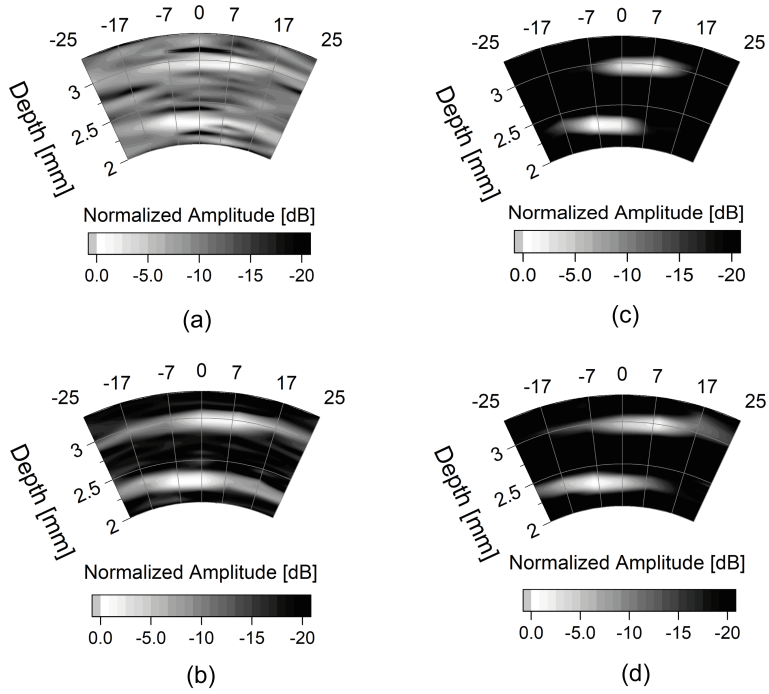


Figure 5.12: Simulated B-mode ultrasound image for the four analyzed TX schemes. (a) Only one TX channel, (b) three TX channels, (c) full array's aperture is used to transmit a plane wave and the beam is steered from -25°to 25°, and (d) full array's aperture is used to transmit, and the beam is focused to 500 μm and steered from -25°to 25°.

(x, y, z) of (-0.25, 0, 2.1)mm, while the second one was defined at (0.25, 0, 2.8)mm. The origin of the coordinate system was placed at center of the array. Figure 5.12 shows the simulated B-mode images for the four analyzed TX schemes, which are represented with the same dynamic range for a fairer

comparison. As was expected, the image obtained when only one channel is used as transmitter shows the poorest performance. This results were improved when the transmission channels were increased to three, but still the image quality is bellow that obtained when the full aperture was used to transmit. The highest quality image in terms of contrast and resolution was obtained when the plane wave is transmitted and steered from -25°to 25°, which is in good agreement with the simulated result illustrated in Figs 5.9 and 5.10.

5.3 Experimental results.

The ultrasound system has been fabricated using the 130 nm HV CMOS process from Silterra discussed in the previous chapter. Figure 5.13a depicts the optical image of the proposed 7×7 AlScN (Aluminum Nitride doped with a 9.5% Scandium) PMUTs-on-CMOS array. The piezoelectric layer consists of a 0.6 μm thick covered by 1 μm Si_3N_4 passive layer following analogous processing already presented in [45], [145]. The top and bottom electrodes are short-circuited at each column forming 7×1 channels. Each column is driving by an individual TX circuit described in Chapter 2, and the RX is carried only out by the even ones (Rows # 2, # 4, and # 6) using the LNA discussed in Chapter 3. As it can been seen the ASIC is under the PMUTs.

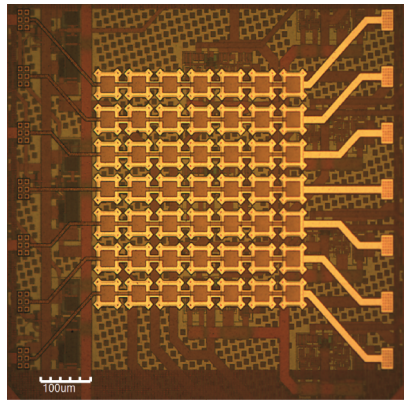


Figure 5.13: Optical image of the 7x7 PMUTs-on-CMOS array.

The ultrasound system was first characterized as an acoustic transmitter and sensor, and then as an acoustic imaging system in a pulse-echo scenario. Once the array was wire-bonded to a PCB, it was immersed in Fluorinert (FC-70,

c=689 m/s, ρ=1940 kg/m^3) for the acoustic characterization.

Figure 5.14 shows the computed inter-element delay for the proposed steering angles, considering that the used system has an element pitch of 65 μm, and the sound is propagated in fluorinert FC-70 at 685 m/s. From the results, a minimum delay time of 11.56 ns and a maximum of 240.6 ns are required to steer the ultrasound beam at previously defined angles.

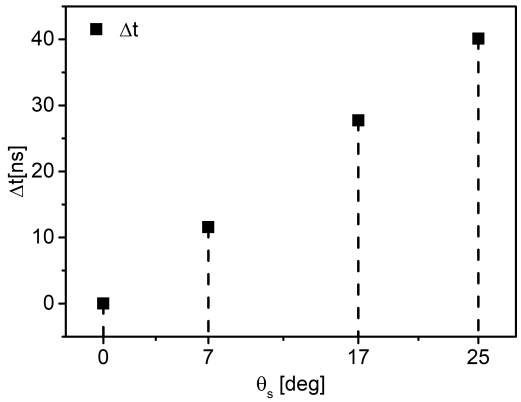


Figure 5.14: Computed inter-elements delay for used steering angles.

As was explained, in the proposed system, the focusing is only applied on the receive side. Taking into account this, the pitch element is 130 μm and the number of receive channel is three. Considering this, in Fig 5.15 is represented the time delay estimated by equation 5.3 at θ_s=0°, 7°, 17°, and 25°. From these results, the minimum and maximum required steering and focusing time delay are 5.87 ns and 160.2 ns, respectively.

5.3.1 Transmitter PMUT-on-CMOS array performance

The performance of the array as a transmitter was evaluated using a commercial hydrophone from ONDA (HNC−0200) obtaining 7 MHz as the center frequency. Based on the the hydrophone frequency response, the average resonance frequency slightly shifts from 7 MHz to 7.58 MHz (σ = 0.05 MHz) and a -6 dB bandwidth of 4.55 MHz (σ = 0.25 MHz) is found, demonstrating a small dispersion in the frequency behavior between channels. The central frequency and the - 6 dB bandwidth are shown in Fig. 5.16.

The acoustic pressure was measured by placing the hydrophone at 2 mm and

driving each column/channel with three monophasic pulses of 32 V amplitude. An XYZ manual micro-positioning system was used to displace and optimize the position of the hydrophone over each of the 7 channels under test. Taking the peak-to-peak amplitude of the temporal response, Fig. 5.17a shows the emitted pressure by each column (red points) and the mean value (dotted blue line). From the results, the mean peak-to-peak acoustic pressure value is 2.55 kPa with a σ of 0.3 kPa, giving a homogeneous behavior of the system in terms of transmitting acoustic pressure. In addition, from the same temporal responses, the delay between each channel and the center one (Column # 4) was extracted, see Fig. 5.17b. The mean delay whose value is 11.8 μm (equivalent to 0.12 λ) is small enough to avoid corrections in the time delay for each channel during the transmission beamforming.

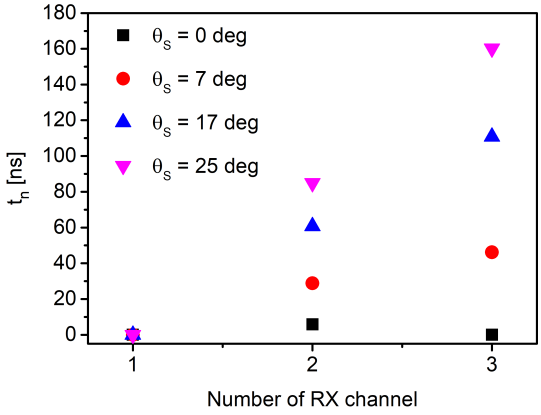


Figure 5.15: Computed steering and focusing time delay.

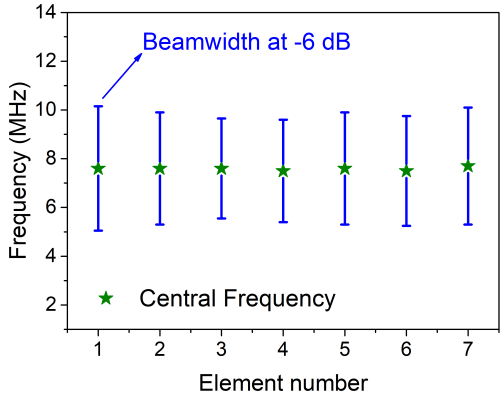


Figure 5.16: Frequency characterization of each individual channel in FC-70.

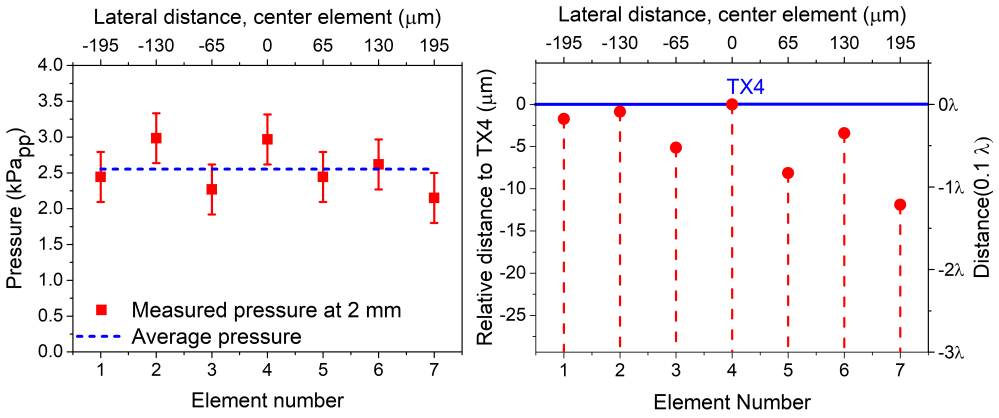


Figure 5.17: Dispersion in the acoustic characterization as an actuator (a) Peak-to-peak acoustic pressure; and (b) Relative arrival delay [146].

Such as aforementioned, the presented PMUT-on-CMOS array is able to steer the ultrasound beam. The transmission delays were computed in order to modify the direction of the main lobe of the ultrasound pattern from θ = -25°to 25°when all channels were actives. After that, the experimental verification was performed by placing the hydrophone at 2.1 mm, and the peak-to-peak pressure was acquired by moving it along ±1.4 mm in the lateral direction. Figure 5.18 depicts the normalized amplitudes for three different lines (Line #4=0°, Line #5=7°, and Line #6=17°) that fit very well with those simulated ones through Field II software [142], [147] and the analytical expressions [69]. The lateral resolution was estimated based on the experimental beamwidth at - 6 dB, giving 545 μm, 571 μm, and 707 μm when θ is 0°, 7°, and 17°, respectively. Note if the steering angle increases, the beamwidth is larger as expected [141]

5.3.2 Reception PMUT-on-CMOS array performance

The acoustic characterization as a sensor was performed using the capability to transmit and receive with the same channel. In this context, channels/columns # 2, #4, and #6 were driven individually, and the FC-70/air interface was used as a reflecting surface. Figure 5.19 inset shows the schematic set-up used in the pulse-echo characterization. When the TX/RX columns are powered, as was explained in the electrical schema, the excitation signal (three

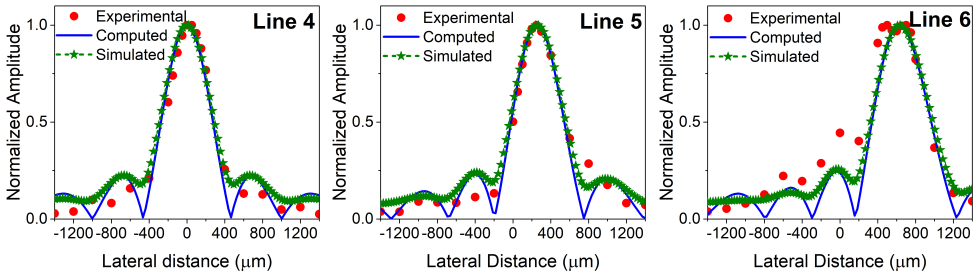


Figure 5.18: Measured, simulated, and computed acoustic beam profiles for different steering angles where (a) 0°(Line 4), (b) 7°(Line 5), and (c) 17°(Line 6).

squared pulses at 7 MHz with 32 V amplitude) was applied to the bottom electrode, and actuating the proper switches, the amplitude of the incoming ultrasound signals were measured.

Figure 5.19a shows the peak-to-peak amplitude using channel 4 to transmit and receive. Based on the ToF, the thickness of the liquid was adjusted with steps of 200 μm, giving an acoustic path range from 2.4 mm to 4.4 mm. To compute the SNR as a function of the acoustic path, the experimental points were fitted by assuming 1/AP dependence, and the output rms noise voltage was extracted from the simulation for the 7×1 PMUTs channel with a bandwidth of 1 MHz. The SNR gives 59 (dB·mm)·AP^{-1} (mm) considering a dependency

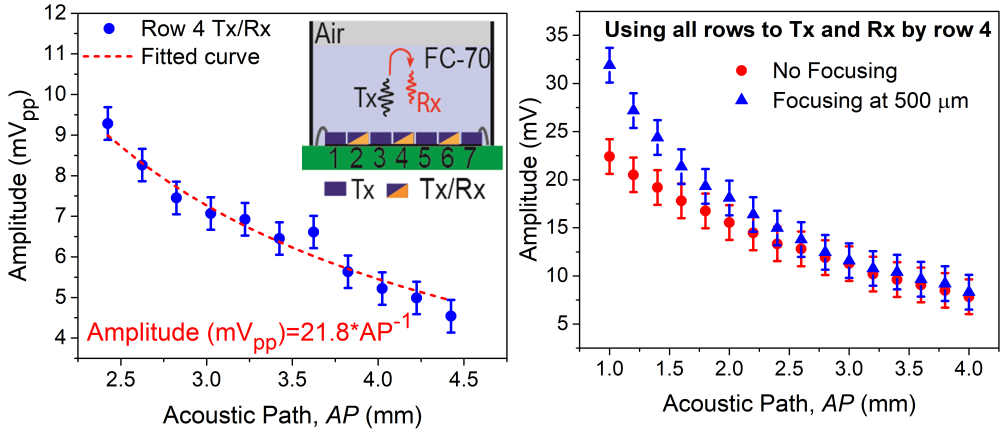


Figure 5.19: Pulse−echo signal at different acoustic path: (a) when channel #4 is used as TX/RX, and (b) when all 7 channels are used to TX and channel #4 to RX (with and without beamforming techniques) [146].

of 21.8 (mV_{pp}·mm), and an rms simulated output noise of 130 μV_{rms}, which corresponds to an SNR of 23.4 dB when the acoustic path in 4 mm. This value is twice as much as the presented in [148], where the same front-end CMOS analog circuit with a single 80 μm square AlN PMUTs working at a lower frequency (2.4 MHz) is used.

In the same context, Fig. 5.19b red dots, shows how the amplitude of the received signal by channel # 4 increases if the number of transmitting channels is greater (7 instead of 1), which would result in an improvement in the SNR. Furthermore, keeping in mind that this array allows beam focusing, the driving signals were configured to focus at 500 μm. Figure 5.19b (blue triangles) depicts the maximum amplitude received by channel # 4 focusing at this point, achieving an enhancement of a factor of 1.4×, which corresponds to the results of the Field II simulation (the natural focus for the 7×7 array is located around 600 μm).

5.3.3 B-mode ultrasound image

The ultrasound imaging capability was performed by using the set-up shown in Fig. 5.20. Based on the schematic representation (Fig. 5.20a), the phantom consists of two gold-plated copper pins with a diameter of 300 μm separated by 200 μm and 720 μm in the lateral and axial directions, respectively. Finally, once the system was immersed in Fluorinert, the pin closest to the array surface (pin 1) was placed at 2.1 mm; therefore, the second one was at 2.82 mm. Figure 5.20 shows a photography during the experiment.

The electronic scanning was carried out through seven steering lines in order

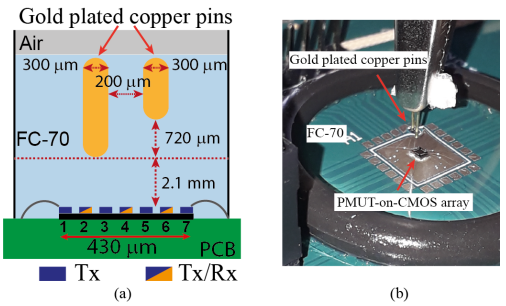
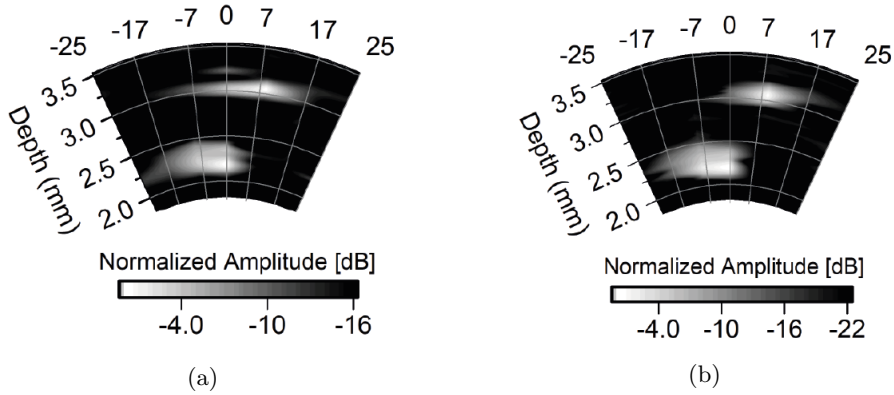


Figure 5.20: Ultrasound imaging set-up: (a) Schematic representation, and (b) Photography.



(a) (b)

Figure 5.21: B−mode image generated: (a) using only channel # 4 as receiver, and (b) using all reception channels as receivers [146].

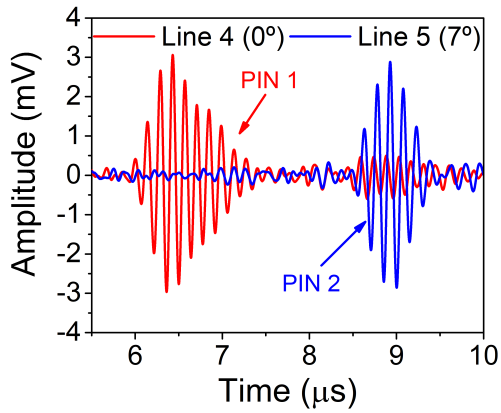


Figure 5.22: Time domain signal obtained at 0°and 7°with the all RX channels (# 2, # 4, and # 6) [146].

to sweep the previously discussed angles (-25°, -17°,-7°, 0°, 7°, 17°,25°). Based on this, the driving signal applied in each channel consists of three square pulses with 32 V amplitude at 7 MHz and the corresponding delays were obtained from an external micro-controller.

The B-mode ultrasound image was obtained at first by receiving through the central column only (channel # 4). The final result is shown in Fig. 5.21a with a dynamic range of 16 dB. Such as mentioned above, to improve the lateral resolution, all reception channels were used. In this sense, the echoes read by channel # 2, # 4, and # 6 have been added using a delay and sum beamforming algorithm implemented externally. Figure 5.21b depicts the final B-mode image when all RX channel were used, giving a dynamic range of 22 dB, which is 6

dB higher than when channel # 4 was used. Finally, the temporal response corresponding to Line 4 (0°steering angle) and Line 5 (7°steering angle) is shown in Fig. 5.22 where, as it can be seen, the echoes coming from both pins appear in Line 4, however, in Line 5 is clearly visible only the second pin. From the results and taking advantage of the capabilities of the PMUT-on-CMOS platform, the ultrasound image can be improved by increasing the number of pitch-matched channels.

5.4 Conclusions.

This chapter focuses on an ultrasound system based on a PMUT-on-CMOS phased array which could be used in imaging applications. The arrayed system has been proven for electronic steering and focusing, with proper beamforming from the seven PMUT channels. A complete simulation analysis has been provided for the optimal array configuration to achieve an ultrasound image. Furthermore, the system has been designed in order to achieve a pitch−matched system between each channel and the front−end circuit that is easily scalable to larger arrays, making our system to be a promising solution for area-demanding applications, such as IVUS systems. Such as in the previous chapter, the monolithic integration ensures high values of signal−to−noise ratio (SNR). The B-mode imaging capability was demonstrated, as a proof of concept, using a simple set−up based on a two pins phantom.

CHAPTER 6

High Accuracy Ultrasound Micro-Distance Measurements with PMUTs under Liquid Operation

This chapter focuses on a novel strategy to estimate very short relative distances with high accuracy using multi-frequency pulsed waves (MFPW). As the first step, this method's details and procedure will be discussed, highlighting the benefits over multi-frequency continuous waves (MFCW). In the second part, as a proof of concept, we implemented a system (based on a PMUT device and a commercial hydrophone) that demonstrates the functionality of the proposed measurement strategy working in liquid for short distances. The comparison with state-of-the-art concludes the chapter and opens the way to a future application of this system in CMOS electronic circuitry. This chapter is based on the analysis and results discussed in: *I. Zamora, E. Ledesma, A. Uranga, and N. Barniol, "High accuracy ultrasound micro-distance measurements with pmuts under liquid operation," Sensors, vol. 21, no. 13, 2021.* All the acoustic characterization was carried out in collaboration with Eyglis Ledesma.

6.1 Background and motivation

Time of flight (ToF) estimation has been a widely used procedure to measure distances, using various forms of energy, such as ultrasound, radio frequency and light. Several techniques have been utilized for ultrasonic distance measurement systems to estimate the ToF. The simplest one is the delay estimation based on a short signal [5], [149], where an ultrasound pulse is transmitted to the surrounding medium, and the elapsed time between the outgoing signal and the detection of the reflected echo (ToF) is measured ($d = ToF \cdot c/2$, see Fig. 1.6 in Chapter 1).

Most of the systems based on the pulse-echo method employ the ToF estimation, based on cross-correlation techniques [48], [150]–[152]. This one uses the cross-correlation function between the transmitted and received signal to obtain the ToF, demonstrating robustness against disturbances, although it requires a high-level of signal processing.

Frequency modulated continuous wave (FMCW) is an alternative method to short signal delay estimation. The approaches discussed by *Kunita et al.* [153] and *Sahu et al.* [4] are based on this method, where the transmitter (TX) emits a frequency modulated continuous wave (CW), which is reflected at the target and is acquired by the receiver (RX), then considering the difference in frequency between TX and RX, the ToF can be estimated. Continuous waves is affected by multipath reflection, which can be avoided using a combination of the frequency modulation waves with burst, known as Chirp modulation. *Pedersen et al.* [154] and *Berkol et al.* [155], [156] used this approach where the transmission time is defined by a pulse with a T_{sweep} duration and the frequency changes with time. When comparing these two methods (FMCW and Chirp modulation), they both achieve the same range accuracy and the chosen transducer is limited by its bandwidth; however, the Chirp signal can discriminate echoes from multiple targets.

Unmodulated CW signals is other approach used to estimate the ToF. In this case, the ToF is estimated based on the phase shift. To compute the distance between TX and RX, the phase shift between the continuous electrical excitation signal and the continuous received signal is measured. In this method, phase data can be sampled for a significant number of wave periods, canceling

the random noise and therefore, guaranteeing a system relatively insensitive to disturbances [157]. However, the distance measurement range is limited to a wavelength due to the phase shift interval (0-360 degrees). To solve it, approaches are implemented based on two-frequency continuous waves (TFCW) [158] or multi-frequency continuous waves (MFCW) [157], [159]. Taking into account this, the phase shift of two or more frequencies are compared, which allows to have range measurements distances higher than one wavelength.

Short distance (mm) measurements, such as micro-positioning applications, cannot be implemented using CW approaches (modulated or unmodulated) because they suffer from multipath reflections that cause large errors [160]. In this context, this chapter presents a new strategy that allows us to determine the relative position between a target and a reference point for short-range measurements (mm) with high accuracy avoiding multipath reflections. The discussed results were presented in [161].

6.2 Theoretical analysis

This section describes the conventional Multi-frequency continuous waves (MFCW) and the proposed Multi-frequency pulsed waves (MFPW) algorithms to measure distances. Furthermore, they will be evaluated and compared in order to expose the benefits of MFPW.

6.2.1 Multi-frequency continuous waves (MFCW) algorithm

Nowadays, the MFCW algorithm has been widely used in radio frequency distance measurement and in accurate air-coupled ultrasonic rangefinder [157]. It is based on the two-frequency continuous waves method (TFCW) [158] including a third frequency to obtain a large distance range while keeping the same accuracy. Taking into account this, the ultrasound transducer is driven sequentially with a continuous wave at these three frequencies (f_1, f_2, and f_3), causing three reflected signals when the target is reached. Once the incoming signals are received, the phase shifts (φ_1, φ_2, and φ_3) between the TX and RX electrical signals are measured, where each one corresponds to each continuous wave (f_1, f_2, and f_3). Equation 6.1 describes the distance d between the TX and RX based on the MFCW where where $Int[]$ is the integer operation, $\Delta\varphi_{1,2}$

and $\Delta\varphi_{1,3}$ are the phase differences (in degrees) between φ_1,φ_2 and φ_1, φ_3, respectively, $\Delta f_{1,2}$ and $\Delta f_{1,3}$ are the frequency differences between f_1, f_2 and f_1, f_3, respectively. The maximum allowed measured distance using the MFCW method is determined by $c/\Delta f_{1,2}$.

$$d = Int\Big[\frac{\Delta\varphi_{1,2}}{360}\cdot\frac{\Delta f_{1,3}}{\Delta f_{1,2}}\Big]\cdot\frac{c}{\Delta f_{1,3}} + Int\Big[\frac{\Delta\varphi_{1,3}}{360}\cdot\frac{f_1}{\Delta f_{1,3}}\Big]\cdot\frac{c}{f_1} + \frac{\varphi_1}{360}\cdot\frac{c}{f_1} \quad (6.1)$$

From this expression, the distance d, can be estimated in three steps: (a) the term $(c/\Delta f_{1,3})/360°$ represents the largest resolution scale, dividing the maximum range into $\Delta f_{1,3}/\Delta f_{1,2}$ divisions; (b) the finer resolution is given by subdividing each division of (a) into $f_1/\Delta f_{1,3}$; and (c) the phase shift φ_1 is used yield the highest-level resolution, written as $(c/f_1)/360°$. Based on this, the frequencies should be carefully selected in order to achieve a compromise among maximum measurable range, resolution, and signal-to-noise ratio (SNR). In this sense, the first consideration to take into account is that f_1, f_2, and f_3 must be within the -3 dB transducer bandwidth to maximize the SNR. In addition, the first and second-order resolutions are better if f_1 is high enough and f_3 far away as possible from f_1. Likewise, f_2 and f_1 must be closer together to get high measurable distances.

As mentioned above, if the TX and the target are close together, a standing wave will appear when using continuous waves. These multipath reflections, as they are known, cause an error in the phase shift measurements, leading to a non-linear distortion of the phase–distance relationship and therefore directly affecting the measurement results [160]. In addition, going back to Eq. 6.1, the integer operation ($Int[\ ]$) can cause errors of values $\pm c/\Delta f_{1,3}$ and $\pm c/f_1$, (first and second term of Eq. 6.1, respectively) in the distance estimation if $\Delta\varphi_{1,2}$ gets closer to multiples of $360° \times \Delta f_{1,2}/\Delta f_{1,3}$ and $\Delta\varphi_{1,3}$ gets closer to multiples of $360° \times \Delta f_{1,3}/f_1$, respectively.

6.2.2 Multi-frequency Pulsed Wave (MFPW) algorithm

To decrease the non-linear distortion of the phase–distance relationship as a consequence of the multipath reflections, *Kuratli et al.* proposed some solutions in [160]. However, these ones cause an increase in the measurement time and computational complexity. In this section, we propose a new ultra-

sound distance measurement method, defined as Multi-frequency Pulsed Wave (MFPW), which uses a combination of the short signals transmitting and a modified MFCW algorithm (see Eq 6.1).

MFPW is based on the determination of the ToF using three burst-tone signals transmitted sequentially, see Fig. 6.1. In this approach, each signal uses a fixed number of sinusoidal cycles with a fixed frequency (f_1, f_2, and f_3, respectively). The number of cycles in each burst is chosen limiting the transmission time (TX time) to be less than the arrival time of the echo signal (the echo is generated by the reflection of the ultrasound signal when it reaches the target) in the pulse-echo method. Therefore, the TX time is determined by the position of the reflecting target and the time for the transducer to reach its steady state. The initial position of the target was determined by estimating the ToF using a simple and fast pulse-echo evaluation.

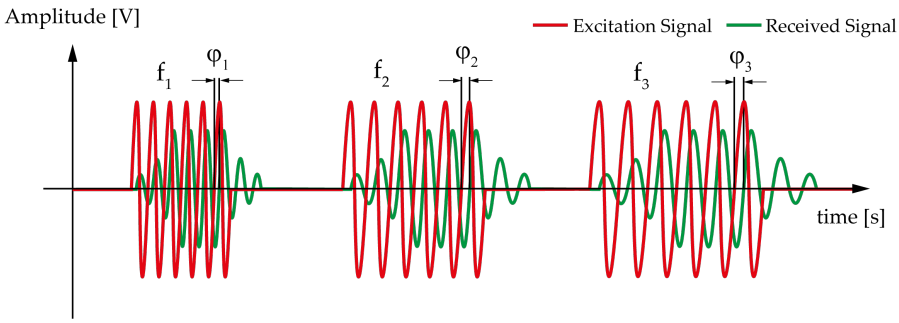


Figure 6.1: Schematic representation of the excitation signals and received signals using MFPW [161].

To enhance accuracy at points that generate $\Delta\varphi_{1,3}$ phase differences multiples of $360° \times \Delta f_{1,3}/f_1$, which corresponds to distances multiples of λ_1 (c/f_1), we propose to apply on Eq. 6.1 the round operation ($Round[\ ]$) on points located in the neighborhood of integer multiples of λ_1, and to apply the integer $Int[\ ]$ operation on the rest of the points. To identify the neighborhood of integer multiples of λ_1, the measured phase (φ_1) is compared with $\pm 90°$. If distances larger than $c/\Delta f_{1,3}$ need to be measured, the same algorithm should be applied to the first term of Eq. 6.1, using $\Delta\varphi_{1,3}$ instead of φ_1 as a test variable. Figure 6.2 shows the flow diagram of the new proposed MFPW method.

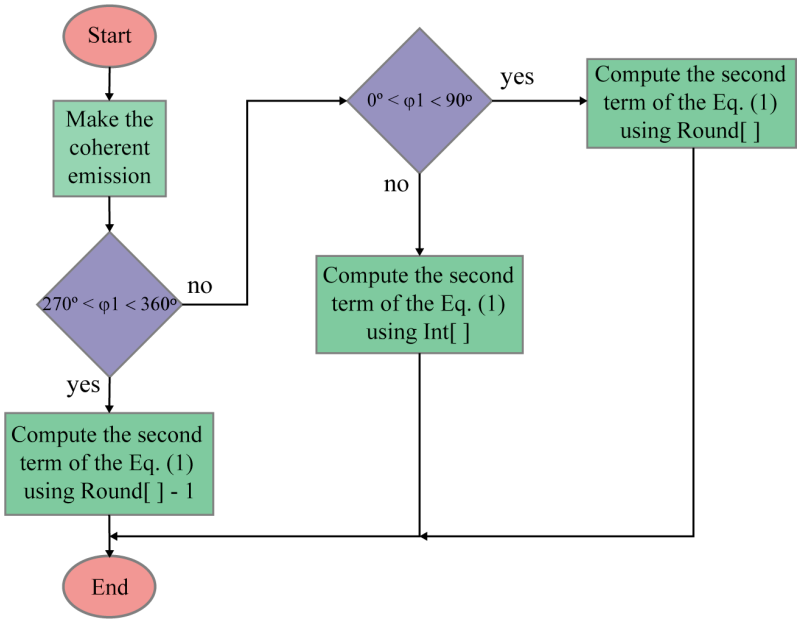


Figure 6.2: Algorithm flowchart used to compute the second term of Equation (1) [161].

6.2.3 Approaches evaluation results

To validate theoretically the MFPW and compare it with the MFCW, the experimental system was considered, which will be explained in more detail in the next section. The chosen frequencies and sound velocity correspond to the experimental values (f_1 = 2.3962 MHz, f_2 = 2.3270 MHz and f_3 = 2.1195 MHz and c = 685 m/s). Figure 6.3a shows a simulation of the phase ($\Delta\varphi_{1,3}$) for a distance range of $c/\Delta f_{1,3}$ (2500 μm), and its allowed margin of error (values inside the red rectangle) that do not modify the distance computation. The range error is given by the integer operation in the second term of Eq. 6.1. As it can be seen, the integer operation changes at $N \times \lambda_1$, being "N" an integer and λ_1 the wavelength relative to f_1 ($\lambda_1 = c/f_1 = 285.9\mu m$). Note that, although the MFCW algorithm allows a maximum range error of $360° \times (\Delta f_1, 3/f_1)$ (41.5° for the chosen frequencies), it is asymmetrically distributed around the measured $\Delta\varphi_{1,3}$. Moreover, at the neighborhood of integer multiples of λ_1, the allowed error is reduced drastically in one of its borders, superior or inferior value. In particular, it causes that both, the maximum allowed error for smaller distances than $N \times \lambda_1$ and the minimum allowed error for bigger distances

than $N \times \lambda_1$ to be very small, see Fig. 6.3a Inset. As a result, if the measured $\Delta\varphi_{1,3}$ is outside that range, the computed distance will have an error of $\pm\lambda_1$, which is not acceptable for the micro-ranging applications. This error could be minimized choosing f_1 as the highest frequency within the bandwidth of the transducer, but at the expense of sacrificing the signal-to-noise ratio.

On the other side, Fig. 6.3b in blue shows the allowed error in the simulation of $\Delta\varphi_{1,3}$ using the round operation in Eq. 6.1 instead of the $Int[\,]$. Note that, in the vicinity of integer multiples of λ_1, the allowed error using the round operation is greater than the allowed one from the integer operation. Figure 6.3b inset shows how the combination of them increases the allowed error in the points close to λ_1, giving a margin of error of $\pm(360° \times \Delta f_1, 3/f_1)/2$ ($\pm$ 20.75° for the chosen frequencies). These results demonstrate the benefits to use the MFPW approach to measure short distances.

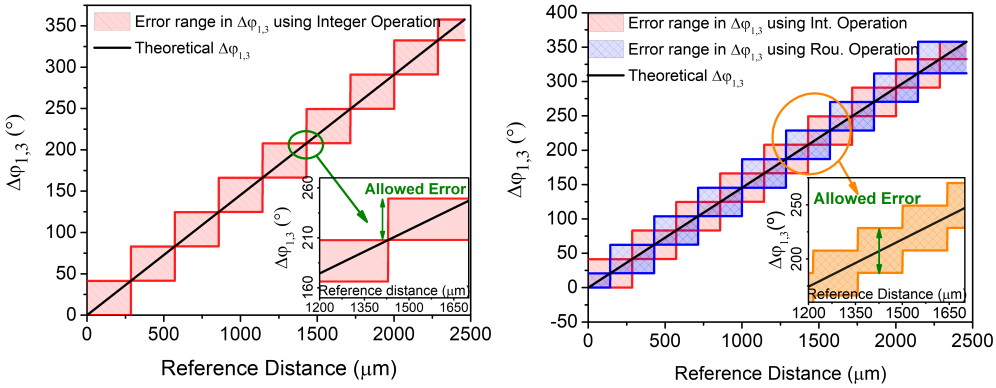


Figure 6.3: Theoretical phase $\Delta\varphi_{1,3}$, and its allowed error using: (a) The MFCW algorithm and (b) the MFPW algorithm. The $5\lambda_1$ neighborhood distance is zoomed in both cases.

6.3 Experimental results and discussion

Figure 6.4 depicts the experimental set-up used to validate the discussed measurement approach. The TX transducer consist on an AlScN (Aluminium Nitride doped with 9.5 % Scandium) square PMUT with 80 μm side presented in [145] with a center frequency of 2.3270 MHz, and a -3 dB bandwidth of 740 kHz in Fluorinert (FC-70, c=685 m/s). The PMUT was fabricated using the

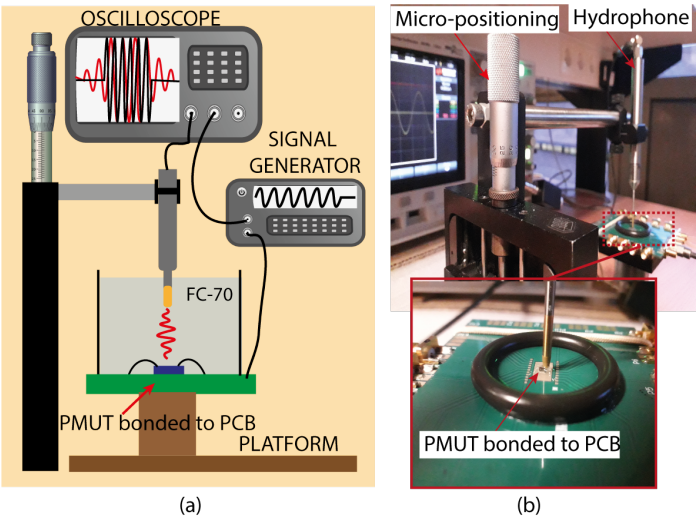


Figure 6.4: Experimental set-up: (a) Schematic representation, and (b) Photograph.

MEMS-on-CMOS process developed by Silterra [108], [148]. On the other side, a commercial hydrophone from ONDA (ONDA−HNC−1500, Sunnyvale, CA, USA) was used both as a receiver and as a target (to measure the distance between the hydrophone and a fixed reference point). Burst electrical signals were generated and applied to the inner electrode using a signal generator (Keysight 81150A, Santa Rosa, CA, USA). Finally, the phase shift angle between the TX signal and the amplified received signal was measured using the zero-crossing approach directly on the oscilloscope (Keysight DSOX3054A, Santa Rosa, CA, USA). To validate the relative measured distances, the hydrophone was placed in a manual micro-positioning system which was lifted every 20 μm with 10 μm resolution. Keep in mind that the chosen frequencies that were introduced in the previous section are $f_1 = 2.3962$ MHz, $f_2 = 2.3270$ MHz, and $f_3 = 2.1195$ MHz, resulting in a 6.88 $\mu m/^\circ$ coarse-resolution and 0.79 $\mu m/^\circ$ fine-resolution.

Taking into account the experimental configuration, the distance between the PMUT and the hydrophone (d) is given by the unidirectional ToF, which corresponds to the time at which the ultrasound signal appears ($t_{ultrasound} = d/c$). For the proposed method, the minimum unidirectional ToF is achieved when the excitation signal (using the minimum frequency, f_3=2.1195 MHz) and the start of the steady state of the received signal overlap in time, keeping in mind that this time has to be small enough to avoid the arrival of the first echo ($t_{1^{nd}echo} = 3 \times t_{ultrasound}$). Since our PMUT reaches its steady state

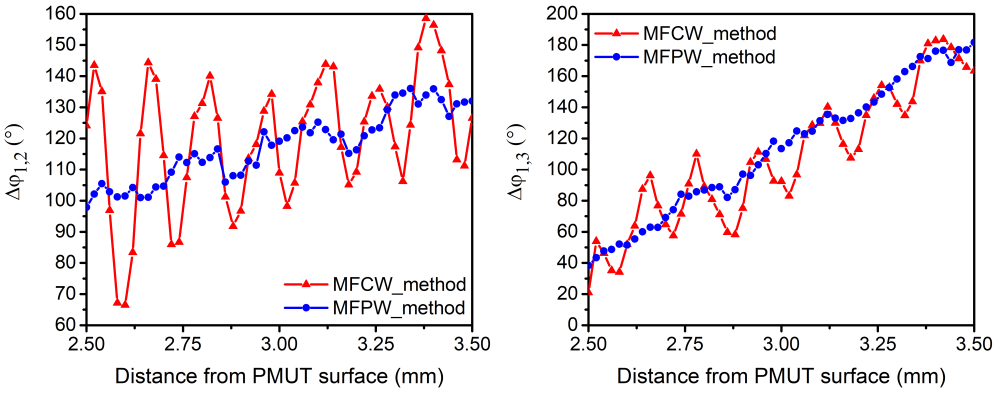
at least after 4 cycles (4T, being T is the period of the excitation signal), these two conditions force that the minimum time needed for the ultrasound signal to arrive ($t_{ultrasound}$) should be larger than two cycles (2T). Based on this result, the minimum transmission time gives six signal cycles and the minimum measurable distance is around 750 μm.

The experimental characterization was carried out in two stages: (1) based on the acquired data, the MFCW and MFPW approaches were evaluated and compared; (2) the improvement of the MFPW method in terms of absolute error and standard deviation was studied.

6.3.1 Multi-Frequency Continuous Waves (MFCW) vs. Multi-Frequency Pulsed Waves (MFPW)

The base point was estimated driving the PMUT with four-sine cycles at 2.3270 MHz with an amplitude of 22 V_{pp}. Considering the unidirectional ToF and the sound velocity in Fluorinert, the hydrophone was placed at 2.5 mm over the PMUT surface. In a second step, the PMUT was sequentially excited with 16 period-long sine waves with an amplitude of 22 V_{pp} at f_1 (2.3962 MHz), f_2 (2.3270 MHz), and f_3 (2.1195 MHz), respectively. Such as aforementioned, the hydrophone moved 1 mm in the axial position with a step of 20 μm, giving a measurement range from 2.5 to 3.5 mm. At each position (including the base point) three-phase shift angles φ_1, φ_2, and φ_3 (one for each frequency) were measured, which were used as input data for the algorithms (MFCW and MFPW). For each distance point, five measurements of the three phase-angles were taken. To continue to ensure overlapping of the excitation and received signals, avoiding the multi-path reflection signals, the number of cycles was increased by one each time the hydrophone raised one λ_1.

Figure 6.5 depicts the measured phase differences (Fig. 6.5a: $\Delta\varphi_{1,2}$, and Fig. 6.5b: $\Delta\varphi_{1,3}$) using both approaches, MFCW (red curves) and MFPW (blue curves). As it is expected, MFCW method show a non-linear behavior, giving a periodic error for $\Delta\varphi_{1,2}$ of 140 μm and for $\Delta\varphi_{1,3}$ of 160 μm. Based on [160], the multi-path reflections are responsible for this periodic component and it has a periodicity of λ_{avg} where for $\Delta\varphi_{1,2}$ $\lambda_{avg} = c/((f_1+f_2)/2)$ and for $\Delta\varphi_{1,3}$ $\lambda_{avg} = c/((f_1+f_3)/2)$, demonstrating a good agreement with the experimental results. On the other hand, taking into account the results obtained with the MFPW,



(a) (b)

Figure 6.5: Measured difference phase using Multi Frequency Continuous Wave (MFCW-red) and Multi Frequency Pulsed Wave (MFPW-blue). (a)$\Delta\varphi_{1,2}$; (b) $\Delta\varphi_{1,3}$ [161].

the non-linearity effect is considerably reduced, although a residual distortion is maintained as a consequence of the electronic noise of the hydrophone's pre-amplifier, which will be explained later. Also, compared to the MFCW method, the periodic error is suppressed.

The signals received by the hydrophone at 3 mm above the PMUT surface are shown in Fig. 6.6. Note how the non-linear distortion due to multi-path reflections is avoided because the phase shift measurement is performed before the first echo.

6.3.2 Relative Distance Measurements

Since the experimental set-up does not guarantee an ultrasound wave coherent beam, relative distances are computed instead of absolute distances. For this purpose, the initial phase angles; φ_1_2.5 mm, φ_2_2.5 mm, and φ_3_2.5 mm, (corresponding to the base point) were subtracted from each phase angle. As the hydrophone was displaced from 2.5 mm to 3.5 mm, the relative displacement is 1 mm making 50 steps of 20 μm each. From the measured phase angles, relative distances were computed using the original and modified (according to MFPW) Eq. 6.1. Figure 6.7 depicts the real relative distances (obtained according to the micro-positioning) versus the computed ones. The use of Eq. 6.1 (red points in Fig. 6.7) shows how large errors in the computed distance are obtained (around $\pm\lambda_1$) when distances are very close to an integer of λ_1.

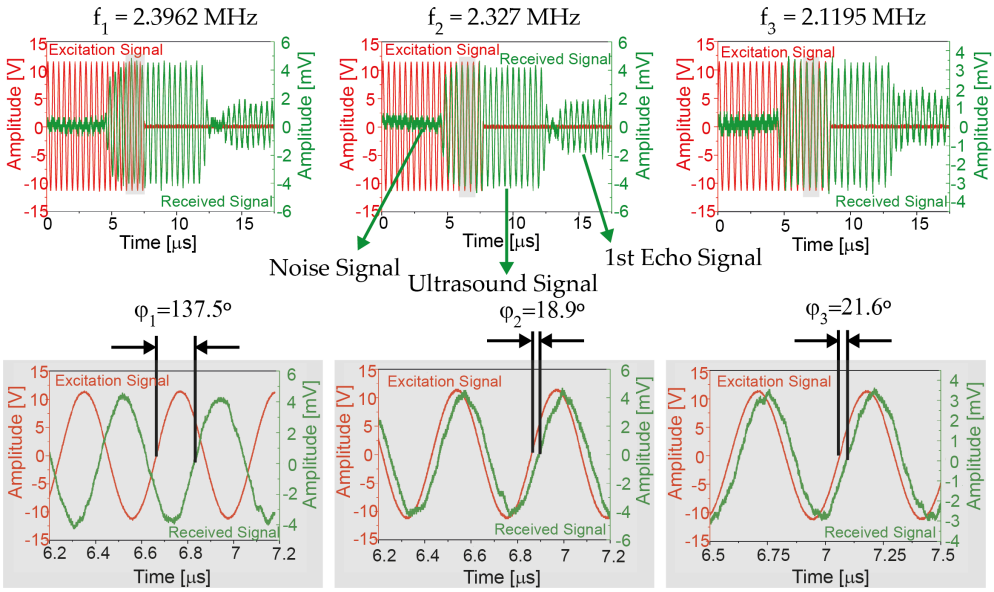


Figure 6.6: Measurement results 3 mm from PMUT surface. The red curves are the electrical excitation signals, and the green curves are the electrical received signals by the hydrophone [161].

These jumps around integer multiples of λ_1 can be suppressed if the proposed algorithm is used (see the flowchart shown in Fig. 6.2). Blue dots in Fig. 6.7 show the accuracy when measuring distance using the MFPW approach.

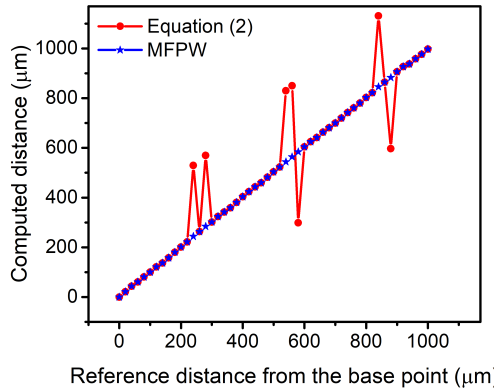


Figure 6.7: Experimental computed relative distances vs. real relative distances from the reference point (2.5 mm) using Equation (2) in red and with the proposed MFPW algorithm in blue.[161].

Figure 6.8 presents the obtained absolute distance errors computed as the difference between the average of the five measurements done at each point and

the real distance. In this case, when the $Int[\,]$ operation was used, a maximum error of ∼291 μm was obtained. However, when the MFPW algorithm was applied, this maximum error was greatly reduced to ∼6.2 μm.

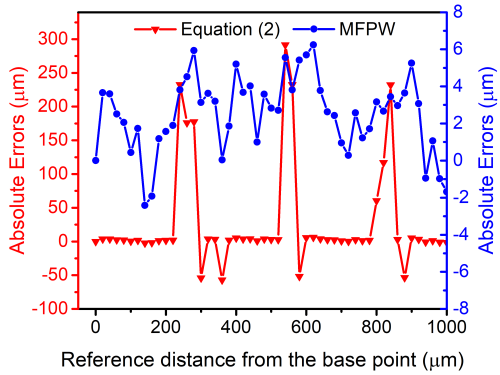


Figure 6.8: Obtained absolute errors using Equation (2) in red and the proposed MFPW algorithm in blue [161].

6.3.3 Uncertainty Analysis

In the experimental set-up used, the random errors were caused by three uncertainly sources: (a) ultrasound velocity, (b) oscillator stability, and (c) phase shift measurements at the zero crossing. Based on (a), the acoustic propagation medium (FC-70) consists of a thermal and chemical stable fluid [127], which allows the uncertainty caused by the sound velocity to be neglected. Considering (b), the used signal source in our experiment is a high stable oscillator (Keysight 81150A Signal Generator), and for this the distance error caused by oscillator error will not be a concern. Therefore, (c) is dominant error source that allows to estimate the random errors. The standard deviation of the phase angle (σ_φ in radians) at zero crossing for a sinusoidal pulse can be written as [162]:

$$\sigma_\varphi = \frac{1}{\sqrt{E/N_0}} \tag{6.2}$$

where E is the pulse energy and N_0 is the power noise spectral density. Equation 6.2 can be rewritten as Equation 6.3 when the root mean squared (rms) values of both signal ($V_{a,rms}$) and noise (σ_n) are considered, SNR is the signal-

to-noise ratio.

$$\sigma_\varphi = \frac{1}{V_{a,rms}/\sigma_n} = \frac{1}{SNR} \tag{6.3}$$

Taking into account that the derivative of both, the integer and round functions are zero when their arguments belong to Real Domain, the standard deviation of the distance (σ_d) according to Eq. 6.1 can be computed as:

$$\sigma_d = \sqrt{\left(\frac{\partial d}{\partial \sigma_{\varphi_1}}\sigma_{\varphi_1}\right)^2} = \frac{c}{2\pi f_1} \cdot \frac{1}{SNR} \tag{6.4}$$

From the reported results in [145], the used PMUT exhibits an exponential pressure distribution in far-field given by $2.66(kPa_{\text{pp}}\ mm) \cdot z^{-1}(mm)$, where z is the axial distance. Taking into account this, the rms voltage at output of Hydrophone's preamplifier ($V_{a,rms}$) is given by Eq. 6.5 where M is the reception sensitivity at the output of hydrophone's preamplifier (11.22 μV/Pa) [134].

$$V_{a,rms}(z) = M \cdot \frac{2.66}{z} \cdot \frac{1}{2\sqrt{2}} \tag{6.5}$$

Keeping in mind that the distances range from 2.5 mm to 3.5 mm, therefore giving measured amplitudes from 4.2 mV_{rms} to 3 mV_{rms}. The standard deviation of the distance can be obtained by combining Eq. 6.4 and Eq. 6.5, which shows a linear dependency with the distance as follows:

$$\sigma_d(z) = \frac{c \cdot \sigma_n}{10.53 \cdot 10^{-6} \cdot 2\pi f_1} \cdot z \tag{6.6}$$

Based on the experimental frequencies (f_1, f_2, and f_3), Eq. 6.6 can only be applied from the minimal measurable distance (750 μm) to the maximum range ($c/\Delta f_1 = 9.8mm$). Figure 6.9 shows the theoretical (black dotted line) and measured (green stars) standard deviation for each distance point. The first one was computed taking into account the output-referred noise of the preamplifier (AH-2010 from Onda) of 160 μV_{rms} in its -3dB bandwidth (from 50 kHz to 25 MHz) [134].

The confidence interval was obtained by assuming that the experimental data have a Student's t distribution because of only five measurements were done at each point (the number of measured points is small). Based on the maximum

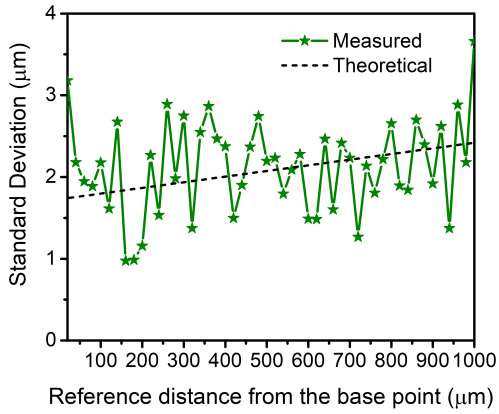


Figure 6.9: Experimental and theoretical σ_d vs. relative distances from the reference point (2.5 mm) [161].

value of the standard deviation depicted in Fig, 6.8, the 70% confidence limit is $\sim$1.95 μm.

A comparison of the MFPW approach discussed until now with other reported methods implemented to measure distances using ultrasound is shown in Table 6.1. The accuracy in measuring the distances, which depend on the central frequency and SNR (see Eq. 6.4), was used to compare them. Based on the final accuracy, the proposed MFPW gives a range error of $\pm$6.2 μm which is the smallest one. Compared to [150], [151] which operates in a liquid environment in the MHz frequency range, MFPW is more accurate at the expense of a reduced measurement range. Consequently, the proposed MFPW provides an attractive alternative in a liquid environment at high frequencies for target micro-positioning with fine steps.

6.4 Conclusions

The new strategy presented in this chapter allows the measurements of relative distances with high accuracy using an ultrasound system based on a PMUT device. With MFPW method, the multi-path reflections are avoided, and therefore, the linear dependence between phase angles and the target's range is improved. In addition, the accuracy in relation to the traditional MFCW algorithm is improved by decreasing considerably the error around integer multiples of the wavelength. The experimental verification was carried out by an 80 μm square AlScN PMUT device in a liquid environment (Fluo-

rinert) which achieves a measured range error of ± 6.2 μm in 3.5 mm, offering better performance than the described algorithm by Equation (2), under the same conditions.

Integration of the presented AlScN PMUT over CMOS circuitry would derive SNR levels comparable with those reported here. Considering this, a very compact and low power ultrasound distance measurement system based on a single PMUT using the MFPW strategy will achieve very high accuracy for short distances in liquid environments.

Table 6.1: Performance comparison of ultrasound measurement distance [161].

	2012 [158]	2015 [5]	2021 [156]	2015 [150]	2019 [151]	This work
Method	TFCW	Pulse-echo	Chirp Modulation	Cross-correlation/PSM	Cross-correlation	MFPW
Transducer	N/A	AlN PMUT	PZT	Commercial (Vico WK-21B)	Commercial (Goworld 1P28)	AlScN PMUT
Propagation medium	Air	Air	Air	Liquid (distilled water)	Liquid (water)	Liquid (FC−70)
Frequency (kHz)	40/40.82	220	94−107	1000	1000	2392.6/2327/2119.5
SNR (dB)	N/A	33[2] at 500 mm	25.26[3] at 550 mm	N/A	N/A	25.5 at 3.5 mm
Standard deviation (μm)	155.7[1] at 200 mm	N/A	N/A	40 at 200 mm	N/A	1.95[5] at 3.5 mm
Range error (μm)	±136 at 200 mm	410_{rms} at 500 mm	18700[4] at 550 mm	N/A	±202 at 25 mm	±6.2 at 3.5 mm

[1] Corresponds to the greater value of all reported.
[2] Extracted from a SNR versus range graph.
[3] Computed using the received power characterization in air of their transducer (−60 dBm) and the input-referred noise of the amplifier (12.2 μV_{rms}).
[4] Corresponds to the standard deviation of the absolute error
[5] Represents the 70% confidence limit considering that the measurements have a Student's t distribution.

Conclusions

In this final Chapter, general conclusions of the thesis work are given. Furthermore, a vision for future research direction are mentioned.

6.5 General Conclusions

The main contribution of this Ph.D. thesis has been the design and implementation of the Analog Front-end ASIC of the first ultrasound system based on monolithic integration of pMUT-on-CMOS. Several systems were implemented and fabricated using the novel CMOS-MEMS monolithic integration platform from Silterra foundry.

For a fair comparison with the state-of-the-art, several Figures-of-Merit were defined, both to evaluate the transmitter (TX) and the receiver (RX) circuits, taking into account the main electrical design parameters. In particular, the transmitter circuit was able to drive pMUTs with 32 V square signals from 3.3 V square input signals. It shown high speed operation capability, achieving 47.5 ns of rise/fall times, and added only 31 ns of propagation delay time when was loaded with around 17 pF. On the other hand, the two implemented LNA topologies (a Voltage Amplifier (VA) and a Transimpedance Amplifier (TIA) based on capacitive feedback) achieved very low input noise levels with high gains and low power consumption. In general, the VA achieved a better performance than TIA when low parasitic capacitance are present (monolithic solution), obtaining an input referred noise of 3.41 nV/$\sqrt{Hz}$ at 3 MHz with 25 dB of DC voltage gain and 0.3 mW of power consumption.

The proposed ASIC solution showed competitive results in comparison with previous works with the minimum area ($0.013mm^2$ of TX circuit and $6 \cdot 10^{-4}mm^2$ of RX circuit). This was an important result for the integration with our pMUT, which occupy an area in the range of $0.0016mm^2$ (square pMUT with 40 μm of side) to $0.0064mm^2$ (square pMUT with 80 μm of side).

A Variable Gain Amplifier (VGA) circuit was designed in order to compensate the signal attenuation due to the spreading propagation in far-field region. This chip is actually under fabrication, and is expected to be completed by the end of the year. In particular, from simulation results, the designed VGA can be programmed from 17 dB to 29 dB, within a -3 dB bandwidth as low as ∼19 MHz (12 kHz to 19 MHz).

The monolithic integration was demonstrated through two PMUTs-on-CMOS ultrasound systems: (a) a single two-port pMUT device, and (b) a 7×7 phased array. Based on the results from the first approach, the monolithic integration demonstrated an improvement of both the signal level and the noise in comparison to the non-integrated system (pMUT wire bonded to CMOS) with the minimization of the parasitic capacitance in the interface pMUT-CMOS. The output-referred integrated noise for the integrated system was reduced a 41 % (46 μV_{rms} versus 111 μV_{rms}), whereas the signal level was improved ∼9x factor, which translates to around 27 dB of SNR gain in comparison to non-integrated system. With the implemented single pMUT-on-CMOS system, a +17 dB of SNR was measured in a pulse-echo experiment when the chip was immersed in 2 mm of fluorinert (FC-70) thickness. This value is higher than the minimum SNR (12 dB) required to differentiate among ridges and valleys in fingerprint imaging application.

The second implemented pMUT-on-CMOS ultrasound system consisted of a 7×7 pMUT array monolithically integrated over seven TX circuit and three LNAs, based on voltage amplifier (VA) topology. To isolate the high voltage (HV) from the TX circuitry of the low voltage of the RX circuitry, the pMUT transducer itself was used as isolation device. This adopted protection scheme avoids the use of HV switches, which resulted in a reduction of the parasitic elements, and saved silicon area. The seven PMUTs on the same column were connected in parallel to reduce the I/O count and consequently reduce the area and power consumption. This resulted in a pitch-matched front-end ASIC with

integrated 1-D pMUT array. This capability allows for easy scalability to larger arrays, making our system a promising solution for applications that require a demanding area, such as IVUS systems. The proposed system was able to perform an electronic scan from -25°to +25°through the implementation of the beamforming technique in both transmission and reception side. As a result, a B-mode image was obtained with a dynamic range of 22 dB.

Finally, in this thesis was presented a new strategy (Multi-Frequency Pulsed Wave) applied to an ultrasound system based on PMUTs that allows the measurements of relative distances with high accuracy. The new approach avoids the multipath reflections and improves the accuracy in relation to the traditional Multi-Frequency Continuous Wave (MFCW). The experimental verification in liquid environment (FC-70), ensured a measured range error of ± 6.2 μm in 3.5 mm, offering better performance than the MFCW algorithm under the same conditions. A very compact, low-power ultrasonic distance measurement system based on a PMUT-on-CMOS system could be implemented using the MFPW strategy, which will achieve very high accuracy for short distances in liquid environments. The results open the way to a future application of this system in CMOS electronic circuitry through a phase detector.

The results obtained in this thesis demonstrate the feasibility of the fully integrated ultrasound system implementation based on pMUT-on-CMOS. On the one hand, the validation of the designed Analog Front-end ASIC to interface with pMUT transducers, and on the other hand the validation of the pMUT-on-CMOS monolithic integration, are an attractive solution to obtain a compact high performance Ultrasound-on-Chip with low-power consumption at a lower cost than those currently in existence, capable of being used not only for imaging or distance measurement applications.

6.6 Future Work

All the results shown in this thesis work have focused on the validation of the new MEMS-on-CMOS fabrication process developed by Silterra, through the implementation of mockups to demonstrate concepts widely used in ultrasound systems such as: estimation of Time-of-Flight, application of the beamforming technique, and image reconstruction. In order to enter the ultrasound sensor industry, it is necessary to implement systems based on large aperture arrays.

Current ultrasound systems are based on hundreds of transmission/reception channels, which allows focusing at much greater distances, improves lateral resolution, and provides greater flexibility in transmission/reception schemes by defining sub-apertures. In this sense, as future work, it is proposed to extend the systems implemented in this thesis work to arrays of pMUTs with a greater number of TX/RX channels, not only in 1-Dimension configuration, but also in large 2D array configuration for realization of 3D images. This would mean a great challenge, since the complexity of the interconnection is greatly increased.

On the other hand, it is necessary to continue with the design and implementation of the remaining functional blocks of the ultrasound system, such as: analog to digital converters, element delays for the implementation of beamforming, charge pump to generate the power supply voltages, etc. With this, we hope to obtain a quasi Ultrasound-on-chip, based on monolithically integrated pMUT-on-CMOS, where very few functionalities will be performed by external electronic control units.

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Author Contributions

Contributions in international journals

- E. Ledesma, **I. Zamora**, J. Yanez, A. Uranga, and N. Barniol, "Single-cell system using monolithic PMUTs-on-CMOS to monitor fluid hydrodynamic properties," Microsystems Nanoeng., vol. 8, no. 1, p. 76, 2022.
- **I. Zamora**, E. Ledesma, A. Uranga and N. Barniol, "Phased array based on AlScN Piezoelectric Micromachined Ultrasound Transducers monolithically integrated on CMOS," in IEEE Electron Device Letters, doi: 10.1109/LED.2022.3175323. *He shares first authorship with E.Ledesma.*
- Ledesma, E.; **Zamora, I.**; Uranga, A.; Torres, F.; Barniol, N. Enhancing AlN PMUTs' Acoustic Responsivity within a MEMS-on-CMOS Process. Sensors 2021, 21, 8447. https://doi.org/10.3390/s21248447
- Ledesma, E.; **Zamora, I.**; Uranga, A.; Barniol, N. Multielement Ring Array Based on Minute Size PMUTs for High Acoustic Pressure and Tunable Focus Depth. Sensors 2021, 21, 4786. https://doi.org/10.3390/s21144786
- **Zamora, I.**; Ledesma, E.; Uranga, A.; Barniol, N. High Accuracy Ultrasound Micro-Distance Measurements with PMUTs under Liquid Operation. Sensors 2021, 21, 4524. https://doi.org/10.3390/s21134524
- **I. Zamora**, E. Ledesma, A. Uranga and N. Barniol, "Monolithic Single PMUT-on-CMOS Ultrasound System With +17 dB SNR for Imaging Applications," in IEEE Access, vol. 8, pp. 142785-142794, 2020, doi: 10.1109/ACCESS.2020.3013763.*He shares first authorship with*

E.Ledesma.

- E. Ledesma **I. Zamora**, A. Uranga and N. Barniol, "Tent-Plate AlN PMUT With a Piston-Like Shape Under Liquid Operation," in IEEE Sensors Journal, vol. 20, no. 19, pp. 11128-11137, 1 Oct.1, 2020, doi: 10.1109/JSEN.2020.2995643
- **Zamora, I.**;Ledesma, E.; Uranga, A.; Barniol, N. Miniaturized 0.13-μm CMOS Front-End Analog for AlN PMUT Arrays. Sensors 2020, 20, 1205. https://doi.org/10.3390/s20041205

Contribution to scientific conference

- E. Ledesma; **I. Zamora**; A. Uranga; N. Barniol;"A 0.5 mm^2 pitch-matched AlN PMUT-on-CMOS ultrasound imaging system," accepted for lecture presentation in IUS 2022 (October 10-13, 2022. Venice, Italy).
- E. Ledesma, **I. Zamora**, A. Uranga and N. Barniol, "Monolithic PMUT-on-CMOS Ultrasound System for Single Pixel Acoustic Imaging," 2021 IEEE 34th International Conference on Micro Electro Mechanical Systems (MEMS), 2021, pp. 394-397, doi: 10.1109/MEMS51782.2021.9375231. (Sharing first authorship)
- E. Ledesma, **I. Zamora**, A. Uranga and N. Barniol, "9.5 % Scandium Doped ALN PMUT Compatible with Pre-Processed CMOS Substrates," 2021 IEEE 34th International Conference on Micro Electro Mechanical Systems (MEMS), 2021, pp. 887-890, doi: 10.1109/MEMS51782.2021.9375359
- E. Ledesma; **I. Zamora**; V. Tzanov; F. Torres; A. Uranga; N. Barniol; E. Marigó; Mohan Soundara-Pandian, "Liquid operable AlN PMUT with high output pressure capabilities," 2019 IEEE International Ultrasonics Symposium (IUS), 2019, pp. 251-254, doi: 10.1109/ULTSYM.2019.8926234
- E. Ledesma; **I. Zamora**; F. Torres; A. Uranga; V. Tzanov; N. Barniol; E. Marigó; Mohan Soundara-Pandian, "AlN Piezoelectric Micromachined Ultrasonic Transducer Array Monolithically Fabricated on Top of Pre-Processed CMOS Substrates," 2019 20th International Conference on Solid-State Sensors, Actuators and Microsystems & Eurosensors XXXIII (TRANSDUCERS & EUROSENSORS XXXIII), 2019, pp. 655-658, doi:

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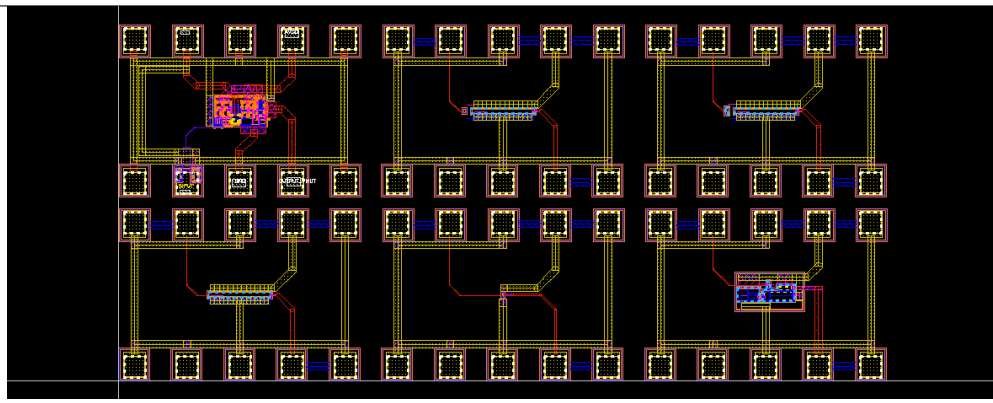
- E. Ledesma; V. Tzanov; **I. Zamora**; F. Torres; A. Uranga; N. Barniol; E. Marigó; Mohan Soundara-Pandian, "ALN Pmut with Crossed-Cavity for Better Acoustic Pressure Outputs in Liquid at High Frequency," 2019 20th International Conference on Solid-State Sensors, Actuators and Microsystems & Eurosensors XXXIII (TRANSDUCERS & EUROSENSORS XXXIII), 2019, pp. 825-828, doi: 10.1109/TRANSDUCERS.2019.8808260
- **I. Zamora**, E. Ledesma, A. Uranga and N. Barniol, "DESIGN OF A FULLY INTEGRATED CMOS-PMUT SYSTEM," 2018 Conference on Design of Circuits and Integrated Systems (DCIS), 2018, pp. 1-5, doi: 10.1109/DCIS.2018.8681498
- **I. Zamora**,E. Ledesma, A. Uranga and N. Barniol, "Fully Integrated CMOS-PMUT Transceiver," 2018 25th IEEE International Conference on Electronics, Circuits and Systems (ICECS), 2018, pp. 149-152, doi: 10.1109/ICECS.2018.8618044
- Ledesma, E.; **Zamora, I.**; Torres, F.; Uranga, A.; Tzanov, V.; Barniol, N.; Marigó, E.; Soundara-Pandian, M. Squared PMUT with Enhanced Pressure Sensitivities. Proceedings 2018, 2, 925, doi: 10.3390/proceedings2130925

RUNs Description

This annex describes all the different runs that contain all the CMOS circuitry developed during this thesis using the Silterra platform. The PMUTs were designed by Eyglis Ledesma.

B.1 Run April 2018

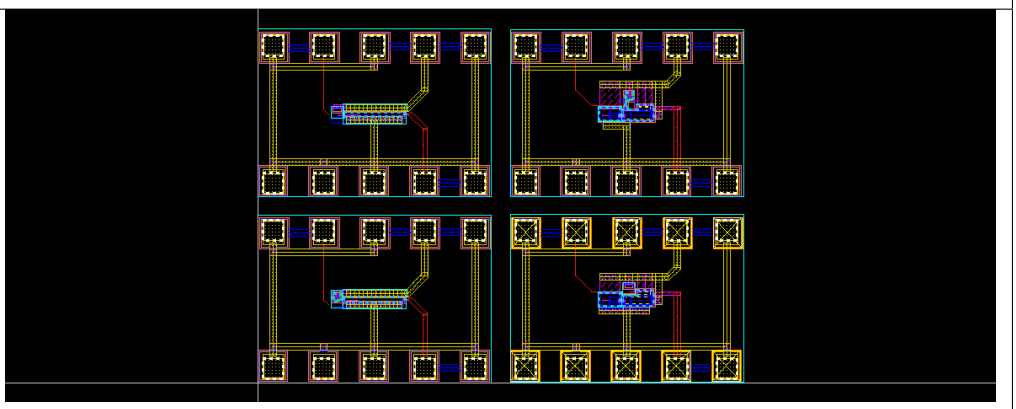
Technology: 130 nm CMOS	**Area:** 1006 x 2183 μm^2	**# Chips:** 6
Description: • HV Pulser Transmitter • LNA Voltage amplifier		



B.2 Run August 2018

Technology: 130 nm CMOS	**Area:** 1050×1444 μm^2	**# Chips:** 4

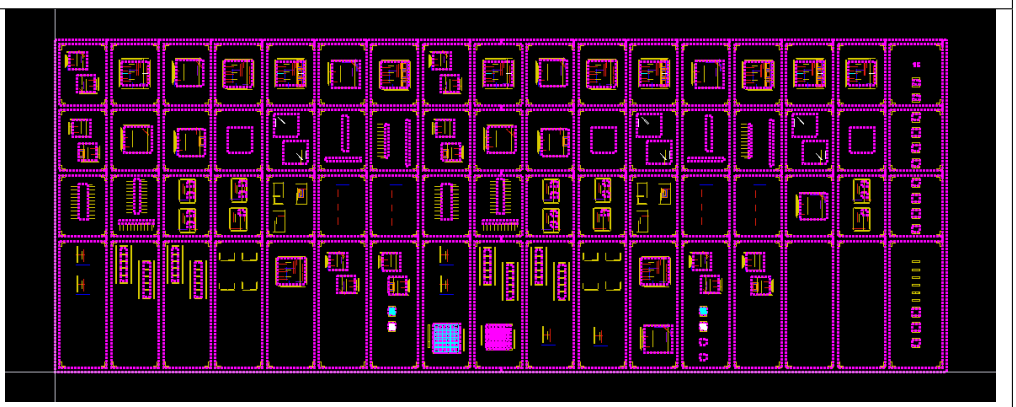
Description:
- LNA Transimpedance amplifier



B.3 Run March 2019

Technology: 130 nm CMOS	**Area:** 9500×25500 μm^2	**# Chips:** 46

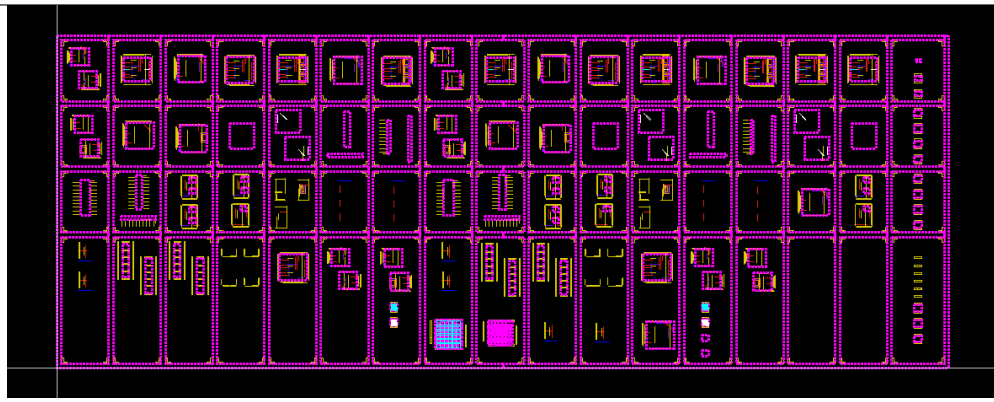
Description: PMUT-on-CMOS systems from single PMUT to phased array configuration using *AlN*. pMUTs were designed by Eyglis Ledesma.



B.4 Run November 2020

Technology: 130 nm CMOS	**Area:** 9500×25500 μm^2	**# Chips:** 46

Description: PMUT-on-CMOS systems from single PMUT to phased array configuration using *AlScN*. The layout is the same as the Run March 2019.



B.5 Run December 2021

Technology: 130 nm CMOS	**Area:** 1528×2800 μm^2	**# Chips:** 10

Description:

- Voltage amplifier with a Variable gain amplifier (VGA) and a close loop output buffer.