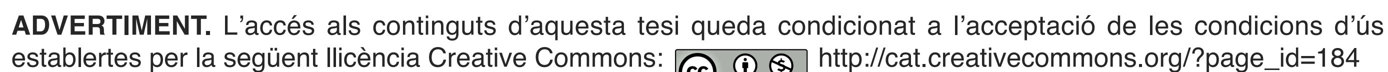
ADVERTIMENT. L'accés als continguts d'aquesta tesi queda condicionat a l'acceptació de les condicions d'ús establertes per la següent llicència Creative Commons:  http://cat.creativecommons.org/?page_id=184

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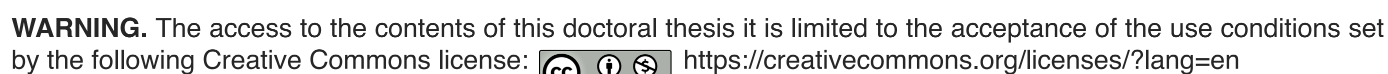
WARNING. The access to the contents of this doctoral thesis it is limited to the acceptance of the use conditions set by the following Creative Commons license:  https://creativecommons.org/licenses/?lang=en

華中師範大學
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Design and Characterization of a MAPS for the CEPC Vertex Detector

Tianya Wu

Doctoral Dissertation

Supervisors: Prof. Sebastian Grinstein,
Dr. Raimon Casanova,
Prof. Guangming Huang
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Dissertation

Design and Characterization of a MAPS for the CEPC Vertex Detector

By

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Abstract

Chinese scientists proposed building a next-generation Circular Electron Positron Collider (CEPC) and later upgraded it into a Super Proton Proton Collider (SPPC) to study the Higgs boson and look for new physics at the energy frontier. One of the challenges faced by the CEPC is to construct a vertex detector (the innermost sub-detector system) capable of providing excellent position resolution, fast readout, and low material budget. To accurately measure the properties of the Higgs boson, the spatial resolution of the vertex detector must be less than 5 μm. At present, the pixel sensors developed by the largest ATLAS and CMS experiments on the Large Hadron Collider (LHC) in Switzerland have spatial resolutions of 10 μm or more. Although the ALPIDE pixel sensor in the ALICE upgrade of the heavy-ion experiment and the MIMOSA pixel sensor in the STAR experiment can reach a position resolution of 5 μm, the readout speed of these chips is not enough (10 kHz to 100 kHz). The bunch crossing of 40 MHz and a dead time of less than 500 ns, needed for the CEPC, cannot be achieved. Thus, it is necessary to design an advanced dedicated pixel sensor according to the physical requirements of CEPC.

A MAPS prototype, TaichuPix, with non-zero compression data-driven and a column-drain readout architecture, has been implemented to provide a fast readout and high spatial resolution for the CEPC vertex detector. This series of chips includes a sensing cell, in-matrix front-end electronics, peripheral readout logic, and high-speed serial data interface modules. It is targeted to develop and verify a prototype for the baseline vertex detector of CEPC. The main content and innovation aspects of the dissertation are presented below:

This dissertation implements a fast readout, non-zero compression data-driven prototype chip TaichuPix for the CEPC vertex detector. The chip improves the readout speed in the array from both analog and digital parts. In the analog part, by enhancing the gain of the analog front-end pre-amplifier, the peaking time is optimized from the conventional few microseconds to less than 400 ns, ensuring the high-speed readout of subsequent digital readout circuitry. The matrix readout speed improves rapidly in the digital readout part by a token ring priority encoder and non-zero compression

data-driven approach. The readout time of this prototype is around 50 times shorter than the JadePix2 solution under a full-scale matrix with the same hit rate.

The FEI3 readout chip architecture of the ATLAS pixel detector is improved to adapt it to a 25×25 μm^2 pixel size. It combines high spatial resolution and fast readout. The FEI3 chip array uses data-driven readout and token priority to transfer data to the end of the column. However, the pixel size is 400×50 μm^2, and the complete readout logic cannot be implemented in a 25×25 μm^2 area. Therefore, a column-drain-based readout architecture is proposed. The timestamp is not stored inside the pixels but at the end of the column, and the ROM that stores the hit information is changed to a direct address encoding MOS transistor matrix, and a double-column scheme is used to share the readout bus. Thus, the area of the readout logic circuit is reduced to 13.7×25 μm^2.

A two-level FIFO architecture is proposed to solve the high data rate readout of a 1024×512 matrix. The peripheral readout logic needs to consider the pixel hit rate and an acceptable dead time. The most stringent condition given by the CEPC CDR is to meet the readout frequency of 120 pixels per microsecond per chip in W boson events. Therefore, this dissertation studies a dedicated high data rate digital peripheral readout. Each double-column is read out in parallel. Every hit pixel is encoded with a 32-bit word, and the hit information is buffered in a column FIFO with a depth of 12 at a clock frequency of 40 MHz. Then it is sent to the chip-level FIFO with a 160 MHz output clock to achieve the data readout frequency of 120 pixel/μs.

The TaichuPix1 test platform was designed based on the ZC706 SoC FPGA. The radioactive source ^{90}Sr was used to verify the full functionality of the chip. The charge deposited from the β particle ionization is amplified by the analog front-end circuit and converted into a voltage signal. Then the position information can be digitalized successfully under the 40 MHz operating clock. At the same time, an external trigger experiment setup with a scintillator was used to verify the function of the trigger mode, and the average cluster size was 2.6. Compared with the ALPIDE of a 29.24×26.88 μm^2 pixel size, the smaller pixel size of TaichuPix1 is expected to achieve a spatial resolution of less than 5 μm.

Keywords: Circular Electron-Positron Collider; Monolithic Active Pixel Sensor; Vertex detector; High spatial resolution; Fast data-driven readout; Token ring encoder

摘　要

为了进一步研究希格斯玻色子，在高能量前沿寻找新的物理突破口，我国科学家在 2012 年 9 月提出了建造下一代环形正负电子对撞机（CEPC）并在后期将其改造成高能质子对撞机（SPPC）的计划。CEPC 面临的其中一项研究难点是构建顶点探测器（最内层的径迹探测器），用于实现出色的位置分辨，快速的读出和低物质量。为了精确测量希格斯玻色子的性质，它的空间分辨率必须小于 5 μm。然而由瑞士大型强子对撞机（LHC）上最大的 ATLAS 与 CMS 实验发展出来的像素传感器的位置分辨率都在 10 μm 或者以上。重离子实验 ALICE 升级中的 ALPIDE 像素传感器与 STAR 实验的 MIMOSA 像素传感器的位置分辨率虽然可以达到 5 μm，但其读出速度不够（10 kHz~100 kHz），无法满足 40 MHz 的对撞环境与 500 ns 以下死时间的要求。因此本课题需要根据 CEPC 的物理要求设计一款全新的专用像素传感器。

本文采用单片有源像素传感器（MAPS）技术，应用非零压缩事例驱动与按列收集的读出架构实现了能应用于 CEPC 顶点探测器的、高位置分辨率及快速读出的 TaichuPix 系列像素传感器原型芯片，该系列芯片包含像素传感单元，阵列内前端电路，阵列外读出电路以及高速串行数据接口等模块，用于研发和验证 CEPC 顶点探测器原型样机，为实际建造 CEPC 顶点探测器奠定了基础。其主要内容与创新点为：

第一，本文针对 CEPC 顶点探测器，设计实现了快速读出的、非零压缩事例驱动像素传感原型芯片 TaichuPix。该芯片分别从模拟和数字两个方面来提升阵列内读出速度，在模拟部分，通过优化模拟前端放大电路增益，将电荷收集器输出信号的最慢上升时间由传统的几微秒缩短至 400 ns 以内，保障了后续数字信号的高速读出。在数字读出部分，应用令牌环优先编码及非零压缩事例驱动的方式大大提高了阵列内的读出速度。该芯片在全规模和常规击中率下，读出时间较前期 JadePix2 芯片读出方案缩短了 50 倍。

第二，改进了 ATLAS 像素探测器的 FEI3 的读出芯片架构，使之适应于 25×25 μm^2 的像素读出，实现像素传感器高空间分辨率与快读出的融合。FEI3 芯片阵列内利用事例驱动读出与令牌环优先传递编码至列端，其单像素面积 400×50 μm^2，完整的读出逻辑在 25×25 μm^2 的像素内无法实现。因此本文提出了按列收集的方案，且将时间戳电路从单个像素内转移到了列端，而存储击中信息的 ROM 则用直接地址编码 MOS 管阵列代替，同时采用双列共享读出总线，使得阵列内读出逻辑电路面积降至 13.7×25 μm^2。

第三，提出了两级 FIFO 架构的阵列外读出方案，解决了大规模 1024×512 阵列芯片高数据率读出问题。阵列外读出电路需要考虑像素的击中率和可接受的死区时间。CEPC 概念设计给出的最严苛条件是 W 玻色子单芯片每微秒 120 个像素被击中。本文采用双列并行读出方式，每个击中像素按 32 位数据编码，击中信息以 40 MHz 的时钟频率先缓存在深度为 12 字节的列级

FIFO 中，再发送给 160 MHz 输出时钟的芯片级 FIFO，实现每微秒 120 像素的数据读出需求。

基于 ZC706 SoC FPGA 设计了 TaichuPix 测试平台，利用放射源 ^{90}Sr 验证了芯片 TaichuPix1 像素传感单元探测到 β 粒子电离沉积的电荷后，经过模拟前端电路放大转化成电压信号，进而转换成击中位置信息的数字逻辑，在 40 MHz 的时钟下，能正确读出。此外，采用闪烁体与放射源搭建的外部触发实验平台，对芯片的触发模式进行测试，分析得到平均簇团大小为 2.6。类比于 29.24×26.88 μm^2 像素面积的 ALPIDE 芯片，更小像素面积的 TaichuPix 芯片将有望实现小于 5 μm 的位置分辨率。

关键词：环形正负电子对撞机；单片有源像素传感器；顶点探测器；高位置分辨；事例驱动快速读出；令牌环优先编码

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Introduction

The Standard Model (SM) of particle physics [1-4] is a theory that encompasses the electromagnetic, weak, strong interactions and includes all the elementary particles known. It is one of the pillars of the current understanding of the Universe. In order to study the SM predictions, particles are accelerated to high energies in dedicated accelerator complexes. The collisions of these particles are studied in extensive experiments that rely on the performance of various detector systems. In particular, detectors need to identify and determine the path and origin of the particles produced in the collisions.

The Higgs boson [5-8] discovery in 2012 by the ATLAS (A Toroidal LHC ApparatuS) and CMS (Compact Muon Solenoid) Collaborations [9,10] at the Large Hadron Collider (LHC) [11-16] at CERN has created a new era for particle physics. Due to its low mass, the Higgs boson can be produced in the relatively clean environment of a circular electron-positron collider with a reasonable luminosity at an affordable cost. To better understand the Higgs boson and look for new physics at the energy frontier, Chinese scientists proposed building a next-generation circular collider. It was first presented to the international conference at the ICFA Workshop "Accelerators for a Higgs Factory: Linear vs. Circular" (HF2012) in November 2012 at Fermilab [17]. Scientists proposed to build a Circular Electron Positron Collider (CEPC) first and later transform it into a Super Proton Proton Collider (SPPC). The collider with a circumference of 100 km is designed to operate at center-of-mass energies of 240 GeV for a Higgs factory, around 91.2 GeV for a Z factory, and around 160 GeV for the WW threshold scan. It will produce large samples of Higgs, W, and Z boson to allow precision measurements of their properties as well as searches for beyond SM physics. A Preliminary Conceptual Design Report (Pre-CDR) [18, 19] was published in March 2015. In June 2018, the CEPC benchmark design plan passed the international evaluation. The evaluation report shows that the design work has proved that the project is feasible and can be approved to the Technical Design Report (TDR) stage. The second volume of the CDR came out in October 2018 [20].

CEPC is a complex scientific project that requires the cooperation of scientists from all over the world, and a number of research and development practices in the

early stage are essential. In November of 2016, the CEPC steering committee clarified the CEPC-SPPC relationship based on the CEPC research results and the future development potential to the SPPC. The physical target and collision environment are clarified in the CDR. And the requirements for the particle detectors are given therein. The physical event rate on CEPC is much lower than that of the LHC. Even the frequency foreseen to study the Z boson, which has the highest event rate, is less than 100 kHz, and there is no pile-up effect, which allows the detector to record all events. The CEPC detector may cover the full spatial angle to record comprehensive physical information as much as possible.

The CEPC detector should be based on the stringent performance requirements needed to deliver a precision physics program. Thus, it is supposed to test the SM and search for new physics over a wide range of center-of-mass energies and beam luminosities. These specifications include large and precisely defined solid angle coverage, excellent particle identification, particle energy measurements, efficient vertex reconstruction, excellent jet reconstruction, and flavor tagging. Considering the detector technologies that CEPC may adopt, the working group has launched many research lines on key technologies. Silicon pixel detectors stand out among many solutions due to their high resolution, fast time response, and high data rate and become the most promising candidate for CEPC. To reconstruct the τ leptons and identify b-, and c-jets, from other types of particles at the CEPC, the measurement accuracy of the impact parameter of the vertex detector should be better than 5 μm. At the same time, precise measurement of charged particles requires the detector material budget as low as possible to reduce the impact of multiple scattering. To satisfy the requirements of the material budget and the low occupancy of the detector, the readout circuitry, cooling system, and mechanical support all need to be light and thin. So far, China has not fully mastered the relevant technology. To fulfill this demand, the Ministry of Science and Technology (MOST) of China supported several institutes and universities in 2016 and 2018, respectively, to carry out a research and development plan. This research is expected to tackle key problems in terms of spatial resolution, material budget, and power consumption by 2023 and produce a prototype of a silicon pixel detector that meets the requirements of CEPC experiments.

One of the challenges faced by the CEPC is the vertex detector (innermost tracking detector). As mentioned before, the CEPC vertex detector must have an excellent spatial resolution to study the Higgs boson to the Bottom quark [102] or Charmed quark [103], which requires accurate track and vertex reconstruction

decay path. In addition, it must withstand ionizing radiation to ensure stable operation in the high luminosity collision environment of the CEPC. The performance of the vertex detector directly determines the physical output of the CEPC experiment. Monolithic Active Pixel Sensors (MAPS) are being investigated for the CEPC due to their high granularity, high speed, low material budget, low power consumption, and radiation tolerance.

This dissertation starts from the CEPC vertex detector requirements discussion, analyzes the current research status domestically and abroad, combines the previous research experience, and proposes a dedicated fully functional MAPS prototype, the TaichuPix, that meets the needs of vertex detectors. The full dissertation can be summarized as follows:

Chapter 1 provides a general introduction to the CEPC project and discusses the key elements to implement a particle detector to exploit the accelerator system. The vertex detector is the most demanding sub-detector system, which should provide excellent spatial resolution while being able to cope with a high particle rate in a radiation environment. The MAPS is the most promising technology for the innermost pixel detector due to its high spatial resolution, fast readout speed, low material budget, and low power consumption.

Chapter 2 discusses some MAPS prototypes used in high-energy physics experiments in domestic and foreign frameworks. The concept of PN junctions, the interaction of the charged particles and photons with the matter, signal formations, and radiation damage are presented. The hybrid silicon pixel detectors and MAPS approaches are also discussed. On the MAPS side the multiple wells' technology for small collection electrodes of the CMOS (Complementary Metal Oxide Semiconductor) pixel sensor is presented. At the same time, the Alice PIxel DEtector (ALPIDE) [21] chip from the A Large Ion Collider Experiment (ALICE) [13] and depleted MAPS designed for the ATLAS experiment are reviewed. Besides, some previous prototypes for the CEPC vertex detector are presented. A table list is summarized at the end of this chapter to compare different pixel sensors and provide a baseline for realizing a fully functional prototype for the CEPC vertex detector.

Chapter 3 presents a fully functional MAPS prototype, TaichuPix1, a small-scale chip that otherwise includes many aspects that are needed for the vertex detector ultimate chip. This chapter introduced an in-pixel analog front-end circuit that has been optimized to have a fast peaking time and short time walk but at the expense of increasing the power consumption. Two parallel in-matrix readout

architectures based on ALPIDE and FEI3 [22] were designed in this prototype. Improvements were made to meet the requirements in terms of the smaller pixel area and higher speed. In order to reduce the area, the timestamp is not stored inside the pixel but at the end of the column. This approach, together with a fast-speed interface and configuration of the digital periphery is critical to achieve the data rate readout requirement of 120 MHz/chip.

Chapter 4 details the optimization of the analog front-end. To meet the fast readout requirement, it is necessary to achieve a fast-rising edge signal with a short time-walk in the analog part of the chip. This chapter presents common front-end electronics architecture solutions used in high-energy physics front-end electronics design. The development of monolithic devices and the limitations of existing devices for the CEPC vertex detector are also presented. The time walk performance is very important since it will determine the speed of the readout system. In the design simulation, the time walk is less than 25 ns, corresponding to the injected charges from 400 e^- to 3000 e^-, assuming a 2.5 fF diode capacitance and 182 e^- thresholds. This is achieved at the expense of increased power consumption, which is around 130 mW/cm^2. The sensor can work at 0 V applied to the PWELL, which results in a threshold value of 268 mV (roughly 300 e^-), with a typical dispersion FPN of 24.4 mV, and a noise distribution with a typical TN of 9.7 mV, for the pixels based on FEI3-like scheme. With this threshold setting, the time walk is measured roughly by an oscilloscope of 57 ns that the injected voltage from 350 mV (~390 e^-) to 1100 mV(~1220 e^-).

Chapter 5 discusses commonly used readout methods, rolling shutter [23], and data-driven [24] architecture. From the CDR of the CEPC, the ultimate chip should meet the requirement of small pixel size and fast readout. This guides the design of in-matrix readout logic. Two practical readout approaches, FEI3 and ALPIDE AERD [25] are good references to start the in-matrix logic design. But the initial circuit implementations do not fully satisfy the requirements of the CEPC vertex detector. Some further optimizations are needed to be done to fulfill the desired target. The space for the in-matrix logic is very limited within a 25 ×25 μm^2 pixel size. Apart from the sensor implementation and the analog front-end area, around 55% is reserved for digital logic. In the FEI3-like approach, the address ROM has been replaced by a pull-up and pull-down network matrix due to area limitations. The timestamp is not stored in-pixel but at the end of the column. In the ALPIDE-like scheme, the pixel cell structure is the same. Still, a dynamic edge-triggered flip-flop has replaced the hit storage registers to prevent reading out one hit

repeatedly before the analog front-end resets. A boosting speed AERD (Address Encoder Reset Decoder) was implemented. For the simulation and one-column test, both approaches meet the requirement of operating at 40 MHz.

Chapter 6 presents the high data-rate peripheral readout logic design of the 512×1024 pixel matrix [26]. According to the CEPC vertex detector requirement, the bunch spacing of the CEPC colliding beams are 680 ns, 210 ns, and 25 ns, respectively, for the Higgs, W, and Z operations. Among these requirements, the most stringent one is to satisfy W boson hit density and bunch spacing. Assume the cluster of 3 and a 512×1024 pixel matrix, the triggerless data rate is around 120 MHz/chip, and the interface speed for a 32-bit word needs to be 3.84 Gbps. A dedicated high data rate peripheral readout logic has been designed that includes a DCOL (Double COLumn) reader, FIFO1, trigger and matches logic, address priority readout, hierarchical data multiplex, and dual-port SRAM. At the same time, a fast readout group of 32 DCOLs is designed. A trigger mode is also considered to reduce the interface speed. From the simulation, the speed of peripheral readout logic is sufficient to achieve a data rate of 120 MHz without any data loss. The power evaluation of the peripheral readout logic shows a density of 25~30 mW/cm^2 for trigger mode and 35~45 mW/cm^2 for triggerless mode.

Chapter 7 presents the test platform designed for TaichuPix1, which is based on the Xilinx FPGA ZC706 Kit [27]. It consists of an integrated processing system (PS) and programmable logic (PL) on a single die. User-defined firmware blocks to the PL were implemented that allow communication with the PS via the AXI bus. A Software Development Kit (SDK) that includes the embedded PetaLinux [28] operation system is used to develop the software. Before measuring the performance of the TaichuPix1 chip, the chip initialization process was verified. The chip has a one-bit shifting register chain to configure every pixel of the whole matrix. A debug core was designed into the TaichuPix1, the data from FIFO2 can be read out directly, which is an efficient way to check the output status of the pixel cells.

Chapter 8 is mainly about the laboratory measurement results using a radioactive source (^{90}Sr) [29]. The results prove that the analog front-end, in-matrix digitization, peripheral readout logic, and serializer can correctly transmit the collected charges to the data interface. The trigger mode of the peripheral readout logic has also been proved, agreeing with the designed trigger setup. This chapter also described some issues that exist in TaichuPix1 and proposed some solutions to overcome these problems. A new prototype, TaichuPix2, is introduced. Section

8.4 focuses on the enhancements implemented on TaichuPix2. Power consumption improvement is the main target of the new prototype chip. For the power dissipation of in-matrix readout logic, a reduction of 60 % is achieved in the TaichuPix2 with respect to the TaichuPix1. At the same time, a laser was used to induce a signal and verify that the TaichuPix2 device could successfully detect traversing charged particles.

Chapter 9 is a summary of the dissertation. It presents the main achievements of the TaichuPix1. At the same time, the drawbacks of the chip are pointed out, and some possible solutions have been discussed.

Authorship contribution statement

As one of the principal designers of the TaichuPix chip, my main contribution is to design the in-matrix digital logic. It is a critical part of the ASIC, which builds a bridge between the analog front-end and the peripheral circuitry. My contributions in the TaichuPix1 and TaichuPix2 can be summarized as follows:

1) Partly worked on the analog front-end schematic simulation. Played a leading role in the pre-amplifier measurement, collected the waveform, and analyzed threshold and noise.
2) Developed the in-matrix digital logic. Conceived the design and simulations of both schemes, FEI3 and ALPIDE. I also worked on the layout and post-layout simulation and all measurements and analyses related to this part.
3) Partly worked on the peripheral readout logic simulations. Conceived the design and analyzed the timing to the end of the column.
4) Fully worked on the TaichuPix1 chip characterization. Designed the test platform, both on firmware and software that used as the data acquisition system, and I carried out all the studies of the chip performance. Construct a setup for the radioactive source measurement. Also worked on data analysis and wrote the documentation.
5) Fully worked on TaichuPix2 optimization, a lower power solution was implemented to the in-matrix readout logic.

Chapter 1

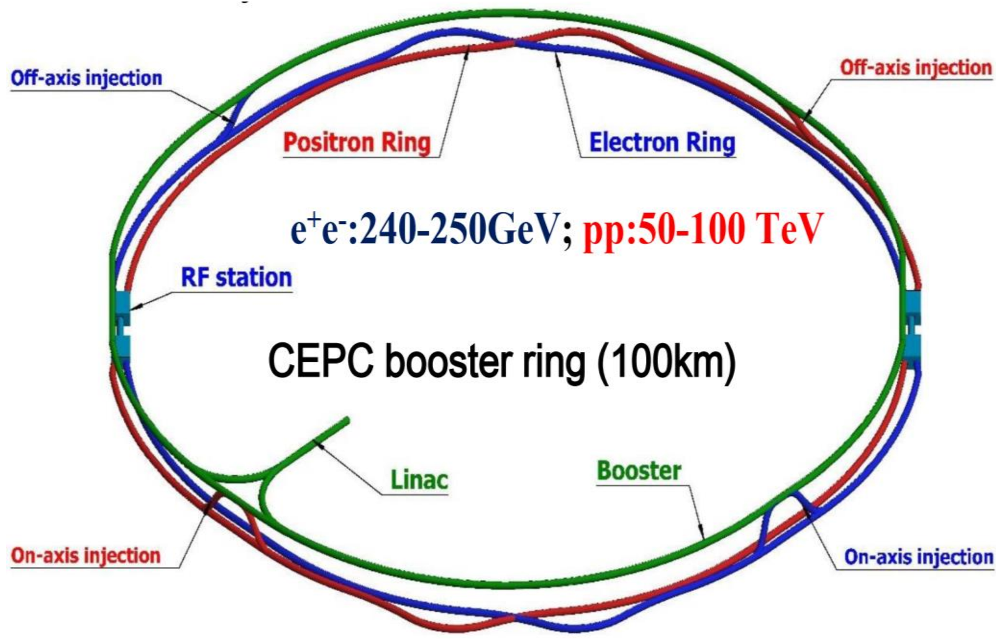
The vertex detector for the CEPC

This chapter briefly introduces the CEPC project and discusses the key elements to implement a particle detector to exploit the accelerator system. The vertex detector is the most demanding sub-detector system, which should provide excellent spatial resolution while being able to cope with a high particle rate in a radiation environment. In particular, the pixel detector, since it is the most innermost detector layer, is the most important for tracking and track impact parameter determination. MAPS is the most promising technology for the pixel detector due to its high spatial resolution, fast readout speed, low material budget, and low power consumption.

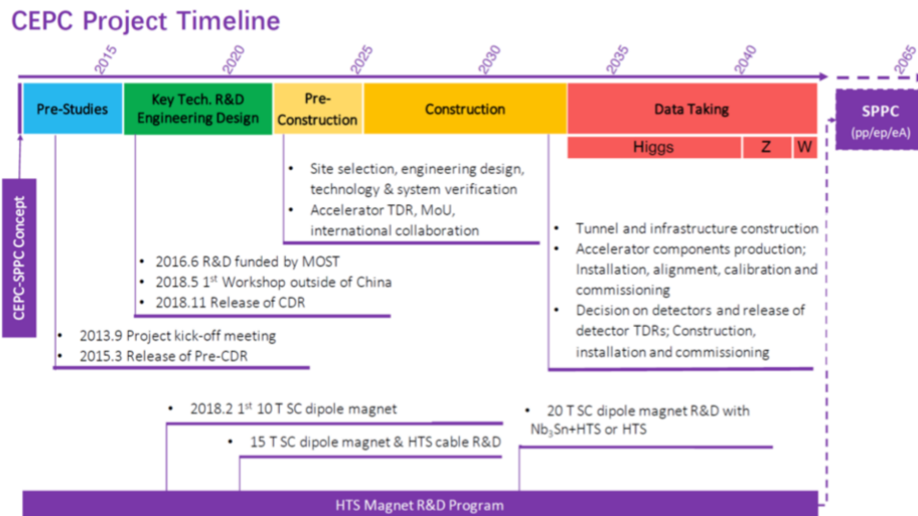
Section 1.1 provides a perspective overview of the CEPC. Section 1.2 discusses two proposed concepts of the detector, the baseline detector concept and the Innovative Detector for Electron-positron Accelerator (IDEA). Both detector concepts include a vertex detector, and it is one of the critical detectors whose requirements are presented in section 1.3. The baseline design of the vertex detector is described in section 1.4. At the end of this chapter, different pixel sensors are discussed, while a review of the sensor technologies is illustrated in section 1.5.

1.1 Perspective overview of the CEPC

The CEPC is a large international scientific complex initiated and hosted by China. According to the accelerator CDR [19], it will be located in a 100 km circumference underground tunnel. As shown in figure 1.1(a), the accelerator complex includes the linear accelerator (Linac), the damping ring (DR), the Booster, the Collider, and several transport lines. The tunnel space is big enough to allow for an upgrade to the optional SPPC. The CEPC center-of-mass energy is 240 GeV that corresponds to the Higgs boson operation mode of the accelerator (ie, operated as a Higgs factory). The design also allows running at 91 GeV for a Z factory and 160 GeV for a W factory. The center of the CEPC is a double-ring collider. It has two Interaction Points (IP) where large detectors are located. The



(a)



(b)

Figure 1.1 Overall construction (a) and time schedule (b) for the CEPC. Adapted from [20].

Booster is in the same tunnel above the collider. A transmission line made of permanent magnets connects the Linac to the Booster. In addition, the collider can also be used as a powerful Synchrotron Radiation (SR) light source. It will extend the available SR spectrum to an unprecedented range of energies and brightness. According to the timeline of CDR (see figure1.1(b)), construction is expected to start in ~2025 and be completed in ~2033. Once the CEPC is operating well, the plan is to start the upgrade work towards the SPPC. The SPPC construction is expected to start in ~2050. The possible preliminary sites being considered for the location of the CEPC are Qinhuangdao in Hebei, Huangling County in Shaanxi,

Shenzhen-Shantou Special Cooperation Zone, Huzhou in Zhejiang, Xiong'an in Hebei, and Changchun in Jilin, all of which received strong support from local governments.

1.2 Proposed detector concept for the CEPC

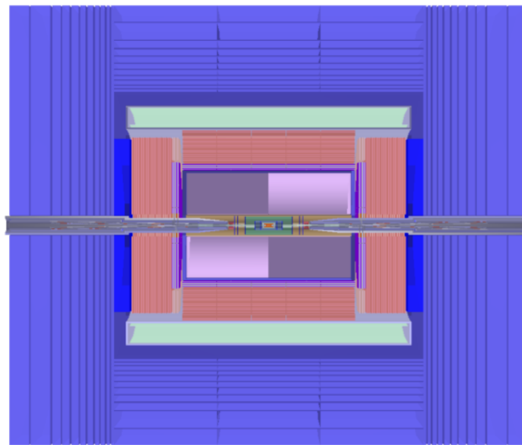
Two primary detector concepts were studied, a baseline detector concept with two approaches to the tracking systems and an alternative detector concept with a different strategy to meet the jet energy and position resolution requirements. The baseline detector concept incorporates the particle flow principle. It includes a precision vertex detector, a Time Projection Chamber (TPC), a silicon tracker, a 3 Tesla solenoid, and a high granularity calorimeter, followed by a muon detector. A variant of the baseline detector concept incorporates a full silicon tracker (instead of the TPC). An alternative detector concept is based on the dual readout calorimetry with a precision vertex detector, a drift chamber tracker, a 2 Tesla solenoid, and a muon detector. The different technologies for each detector subsystem are being pursued actively with R&D programs and provide many opportunities to leverage leading advances in detector development in the coming years.

1.2.1 Baseline detector concept

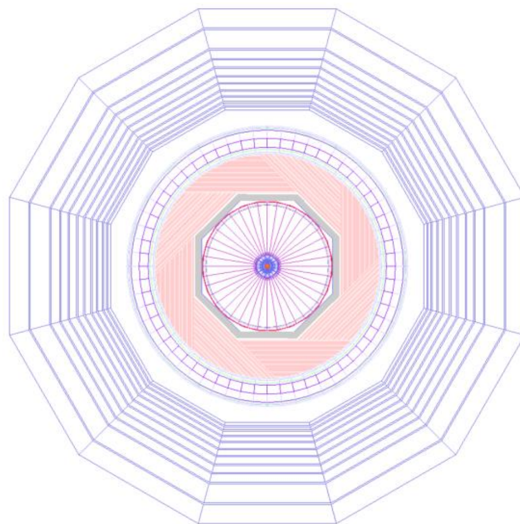
The baseline detector concept is guided by the particle flow principle of measuring the final state particles in the most suitable detector subsystem. The particle flow algorithm (PFA) reconstructs the list of low-level particles (called PFA particles) and associates the detector hits with these particles. All physics objects input to physics analyses is then identified or reconstructed from this unique list of PFA particles for each physics event.

As shown in figure 1.2, the baseline concept, from innermost to outermost sub-detector system, is composed of a silicon pixel vertex detector, a silicon inner tracker, a TPC surrounded by an external silicon tracker, a silicon-tungsten sampling Electromagnetic Calorimeter (ECAL), steel-Glass Resistive Plate Chambers (GRPC), a sampling Hadronic Calorimeter (HCAL), a 3 Tesla superconducting solenoid, and a flux return yoke embedded with a muon detector. In addition, five pairs of silicon tracking disks are placed in the forward regions at either side of the interaction point (IP).

The vertex detector consists of six concentric cylindrical pixel layers at a radius between 1.6 cm and 6.0 cm, providing impact parameter measurements with a resolution of 5 µm. The next detector system is the silicon inner tracker outside the vertex consisting of two microstrip layers at radii of 15.3 cm and 30 cm before the TPC. The external silicon tracker consists of one microstrip layer at a radius of 181 cm after the TPC. The forward silicon tracker comprises five pairs of silicon disks located at either side of the IP in between *z* positions of 20–100 cm. The baseline concept employs high granular sampling ECAL and HCAL, providing 3-dimensional spatial and energy information.



(a)



(b)

Figure 1.2 *r*–*z* view(a) *r*–*φ* view (b) of the baseline detector concept. Adapted from [30].

1.2.2 Full Silicon Tracker (FST) concept

Silicon detectors are at present the most precise tracking devices for charged particles in high-energy physics experiments. They have an excellent spatial resolution and granularity to separate tracks in the environment of dense jets and deal with high hit occupancy from beam-related backgrounds at high luminosities. An attractive option is a variant of the CEPC baseline detector concept with a full-silicon tracker (FST) without the TPC. The FST is able to provide excellent tracking efficiency, momenta resolution, and vertexing capability for charged particles from the IP and secondary vertices. The FST replaces the TPC and the baseline silicon tracking system with a full-silicon tracker while keeping other detector subsystems unchanged. A toy Monte Carlo simulation optimized the number of layers, single-sided versus double-sided layers, and the layout geometry. An alternative approach based on the ILC-SiD (International Linear Collider-Silicon Detector) design [31] is also being considered. The FST detector geometry, as shown in figure 1.3, has been implemented in the simulation and track reconstruction software. Initial studies show promising tracking performance. However, many improvements in the simulation and reconstruction are needed to demonstrate the full potential of the FST.

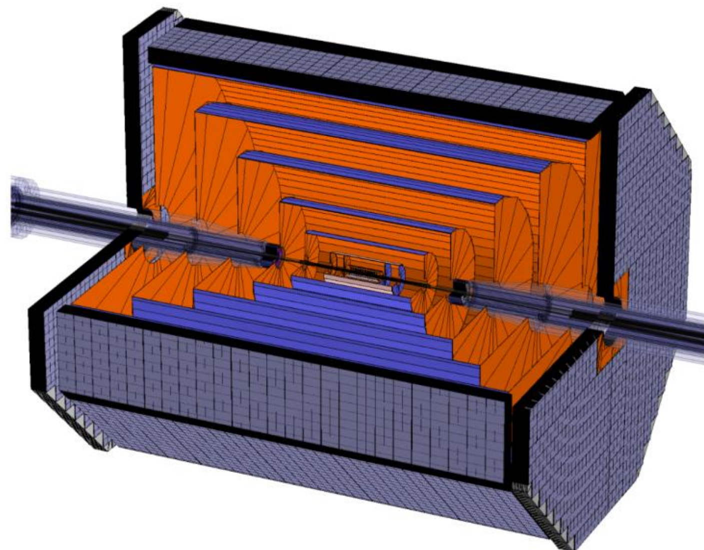


Figure 1.3 The cutaway view of the full silicon tracker proposed as an option for the CEPC baseline detector concept. Adapted from [30].

1.2.3 Innovative Detector for Electron-positron Accelerator (IDEA) concept

An optional detector concept, the Innovative Detector for Electron-positron Accelerator (IDEA), has been designed for a circular electron-positron collider. It is also being adopted as a reference detector for the FCC-ee (Future Circular Collider, e^+e^-) studies. The concept design attempts to lower the overall cost of the detector and proposes different technologies than the baseline concept for some of the main detector subsystems. It provides an opportunity to take advantage of challenges and advances in detector development before the CEPC detector construction begins.

The structure of the IDEA detector is outlined in figure 1.4, which also shows its overall dimensions. A key element of IDEA is a thin, 30 cm, and low mass, 0.8 X_0 solenoid with a magnetic field of 2 Tesla. The low mass and thickness of the solenoid allow it to be located between the tracking volume and the calorimeter without a significant performance loss. According to studies done for the FCC-ee, the low-magnetic field is optimal as it minimizes the impact on emittance growth and allows for manageable fields in the compensating solenoids. On the other hand, it puts stringent constraints on the tracker design required to achieve the necessary momentum resolution. IDEA has consequently adopted a large low-mass cylindrical drift chamber (DCH)as its main tracker.

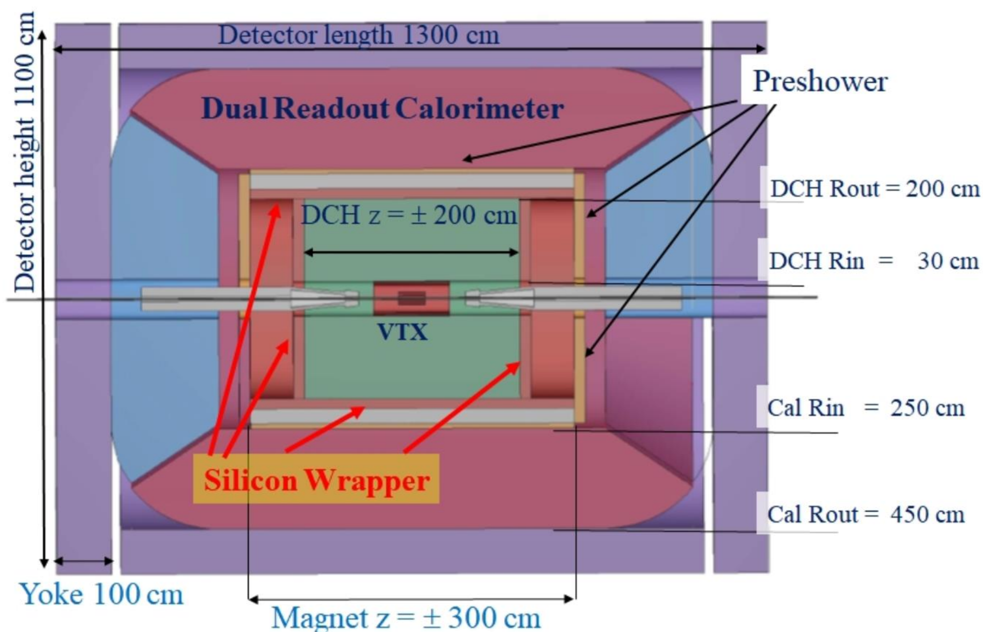


Figure 1.4 Schematic layout of the IDEA detector. Adapted from [30].

1.3 Performance requirement of the vertex detector

Identifying heavy (*b*- and *c*-) quarks and τ leptons is crucial to the CEPC physics program. CEPC detectors need to accurately determine the track parameters of the charged particles near the interaction point so as to be able to reconstruct the displacement attenuation vertex of the short-lived particles. This drives the demand for vertex detectors with a low material budget and high spatial resolution. The baseline design of the CEPC vertex detector is a cylindrical barrel with six silicon pixel sensor layers. It is optimized for the CEPC energy system and uses modern sensors.

Figure 1.5 shows the preliminary layout of the tracking system of the CEPC baseline detector concept. The Time Projection Chamber (TPC) surrounds the Silicon Tracker. Colored lines represent the positions of the silicon detector layers: The Vertex Detector (VTX) layers are shown in red lines; the Silicon Inner Tracker (SIT) and Silicon External Tracker (SET) components of the silicon tracker are drawn in orange lines; the Forward Tracking Detector (FTD) and Endcap Tracking Detector (ETD) components of the silicon tracker are with gray-blue lines. The beam pipe is shown in cyan lines, and the dashed red line shows the beamline position with the beam crossing angle of 0.0165 rad. The ETD is not currently

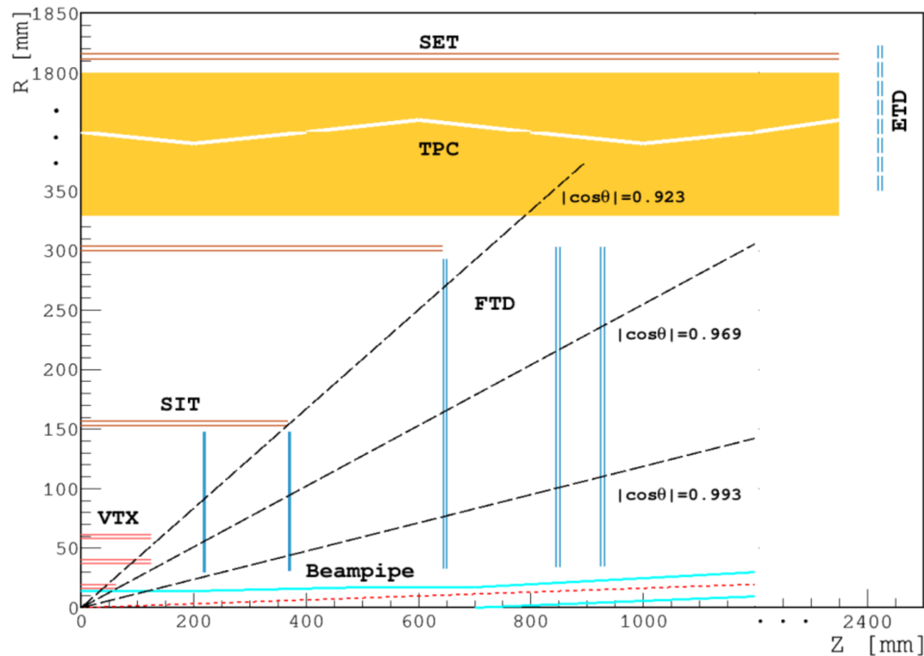


Figure 1.5 Preliminary layout of the tracking system of the CEPC baseline detector concept. Adapted from [30].

included in the full simulation. The radial dimension scale is compressed at about 350 mm just for clarity.

To support the precision physics program, the CEPC vertex detector is designed to realize excellent impact parameter resolution, which in the $r\varphi$ plane can be parametrized by:

$$\sigma_{r\varphi} = a \oplus \frac{b}{p(GeV)\sin^{3/2}\theta} \quad (1.1)$$

Where $\sigma_{r\varphi}$ represents the impact parameter resolution, p is the track momentum, and the θ is the polar track angle. The first term describes the intrinsic resolution of the vertex detector without multiple scattering. It is independent of orbital parameters, and the second term reflects the effect of multiple scattering. With parameters a = 5 μm and b = 10 μm • GeV are regarded as the design value of the CEPC vertex detector. Three concentric cylinders can achieve the main physical performance goals with double-layer pixelated vertex detectors, which have the following characteristics:

1) Single-point resolution of the innermost layer better than 3 μm;
2) Material budget below 0.15% X_0 per layer;
3) the first layer located close to the beam pipe at a radius of 16 mm;
4) Detector occupancy not exceeding 1%.

The sensor power consumption and readout electronics should be kept below 50 mW/cm^2 if the detector is only cooled with air. The readout time of the pixel sensor needs to be shorter than 10 μs to minimize pile-up from consecutive bunch crossings. The radiation tolerance is also essential for the innermost detector layer. The current maximum radiation requirement of nonionizing energy loss (NIEL) is about 6.2×10^{12} 1 MeV neq/cm^2 per year and the total ionizing dose (TID) is estimated of 3.4 Mrad/year, see table 1.2.

1.4 Baseline design of the vertex detector

The baseline layout of the CEPC vertex detector consists of six concentric cylindrical layers. The high spatial resolution silicon pixel sensors are located between 16 and 60 mm in radii from the beamline (see figure 1.6), providing six precise space points for charged particles traversing the detector. The main

Table 1.1 The baseline design parameters of CEPC vertex detector (including position and single-point resolution)

	R(mm)	|z|(mm)	σ(μm)
Layer1	16	62.5	2.8
Layer2	18	62.5	6
Layer3	37	125	4
Layer4	39	125	4
Layer5	58	125	4
Layer6	60	125	4

mechanical structure is called a ladder. Each ladder supports sensors on both sides; thus, there are three sets of ladders for the vertex detector. The material budget of each detector layer amounts to around 0.15% X_0, including their related supporting material. Extensive simulation studies show that this configuration with the single-point resolutions listed in table 1.1 achieves the required impact parameter resolution [30].

When operating the machine at the center-of-mass energy of $\sqrt{s}$ = 240 GeV, the main detector backgrounds come from pair-production of heavy particles (like WW). The contribution from the off-energy beam particles is nearly an order of magnitude lower. Figure 1.7 shows the hit density at different vertex detector layers originating from pair production. At lower operation energies, $\sqrt{s}$ = 160 GeV for W and $\sqrt{s}$ = 91 GeV for Z, the background particles are usually produced with lower energies but higher rates given the higher machine luminosities. In addition, the pair-production dominates the main source of the radiation backgrounds.

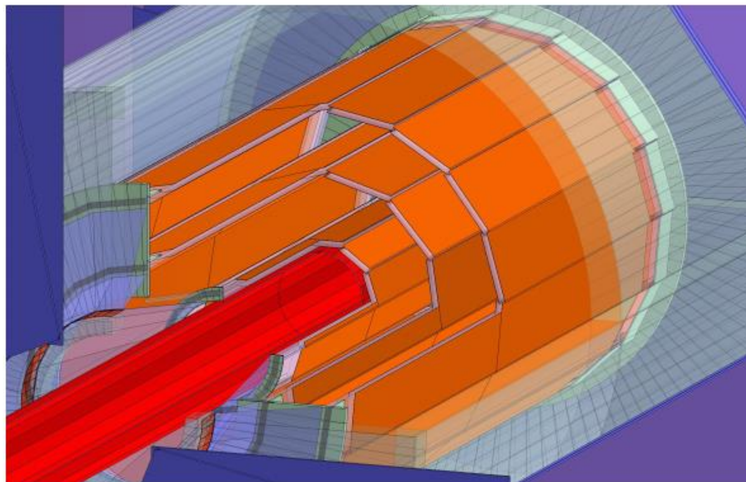


Figure 1.6 Schematic view of pixel detector. Adapted from [30].

The resulting radiation backgrounds at the first vertex detector layer at different operation energies are summarized in table 1.2. The most stringent requirement is the 25 ns bunching spacing of the Z boson and the high data rate of the W, which should satisfy both 210 ns bunching spacing and hit density of 2.3 hits/cm^2·BX (where BX is bunch-crossing).

1.5 Sensor technology options for the vertex detector

Silicon pixel detectors are essential for the precise determination of tracks and

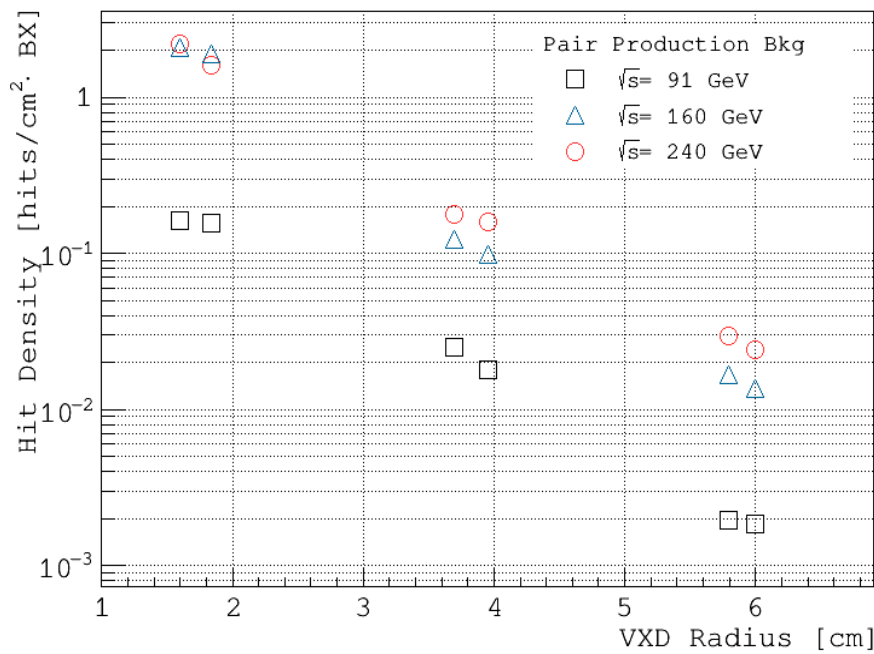


Figure 1.7 Hit density at different layers of the vertex detector due to pair production for the machine operation with $\sqrt{s}$ =240,160 and 91 GeV, respectively. Adapted from [18].

Table 1.2 Summary of hit density, total ionizing dose (TID), non-ionizing energy loss (NIEL) and bunching spacing with combined contributions from pair production and off-energy beam particles, at the first vertex detector layer (r = 1.6 cm) at different machine operation energies $\sqrt{s}$ = 240, 160 and 91 GeV, respectively.

	H (240)	W (160)	Z (91)
Hit density [hits/cm^2·BX]	2.4	2.3	0.25
TID [Mrad/year]	0.93	2.9	3.4
NIEL [10^{12} 1 MeV n_{eq}/cm^2.year]	2.1	5.5	6.2
Bunching spacing (μs)	0.68	0.21	0.025

vertices, enabling the selection of interesting events by identifying b-jets (b-tagging). As accelerator complexes are improved (like the LHC in the near future), to probe the energy frontier further, new pixel sensor technologies must be developed to maintain the detector performance. Hybrid detectors are composed of a silicon sensor connected to a readout ASIC with a similar array of readout channels via bump-bonding solder balls. The fact that the readout and the sensor part of the detector are separate entities has the advantage that the technology for each part can be optimized independently. However, hybrid detectors suffer from some limitations. The bump-bonding coupling of the sensor and the ASIC adds a high cost to the detector assembly while it also increases the capacitance of the system

An alternative to the standard hybrid devices is monolithic detectors. In this approach, the sensor and the readout chip are integrated into the same silicon substrate, thus removing the need to perform the bump-bonding procedure and reducing the capacitance of the devices substantially. Monolithic devices have already been used in high energy physics (HEP) [32], but with higher costs associated with the specialized fabrication process. For example, the TowerJazz CMOS Imaging Sensor process can be customized by the user [65]. In the early MAPS prototypes, the charge was mainly collected by diffusion. This increases the probability that the substrate defects are trapped in the generated charge leading to less radiation tolerance. If the charge is collected by drift, the probability of being trapped drops substantially, making the sensor more robust to radiation [107,114].

The development of a new kind of monolithic device for usage in high-energy physics collider experiments is being pursued. The novelty relies upon using the standard high voltage (HV) [108-110] and high resistivity (HR) [115] CMOS technology to fabricate the monolithic pixel detectors. In this standard process, the electronics are placed inside deep nwells. At the same time, a large depletion region is grown on the same substrate (enabled by the HV and/or HR process) to collect the charge generated by the incoming radiation. Depleted CMOS detectors have been proposed for imaging applications in the recent past [33]. During the last few years, an intense research and development (R&D) program has also been launched to investigate the usage of this technology for HEP instrumentation.

Many research and design efforts have already been taking place in the HEP community to develop pixel sensors for vertex tracking [34], driven by track density, single-point resolution, and radiation level. As mentioned in section 1.3, the detector challenges for the CEPC are high impact parameter resolution, low

material budget, low occupancy. It should also tolerate sufficient radiation, which is mild compared to the LHC but necessary to consider. In order to fulfill these requirements, sensor technologies must be selected to achieve fine pitch, low power, and fast readout. These demands bring many challenges to the CEPC vertex detector. CEPC has a bunch spacing of 0.68 μs for the Higgs factory operation and 25 ns for the *Z* factory operation. Experiments such as the STAR [35], BELLE II [36], and ALICE upgrade [37] readout continuously as the CEPC. However, there are less stringent requirements for them in terms of spatial resolution and material budget. The monolithic pixel sensor is a promising technology to satisfy the low-material and high-resolution requirements for the CEPC vertex detector. This technology has been developing rapidly. The first-generation MAPS-based vertex detector for the STAR HFT upgrade [38] successfully finished its 3-year physics run. The new generation HR CMOS Pixel Sensor for ALICE ITS upgrade is in mass production. With the previous double-well process, only NMOS transistors can be selected in the pixel design. This constraint has been solved in the new 0.18 μm quadruple-well process [39]. Both NMOS and PMOS transistors can be used in pixel design. Together with smaller feature size, it is a very appealing technology. The ALPIDE design [40], with its pixel size of 29×27 μm^2, being developed for the ALICE-ITS upgrade, has a performance very close to the requirements of the CEPC and could thus serve as a starting point for the CEPC vertex detector. Further research and development are needed to reduce the pixel pitch to around 16 μm (suppose the sensor performance is as good as ALPIDE) to achieve the required 2.8 μm single-point resolution.

An alternative monolithic process is the Silicon On Insulator (SOI) pixel sensor [111]. Fundamental issues, including the transistor shielding [41] and the TID tolerance [42], have been addressed, and wafer thinning [43] has been proved. At the same time, the development of ILC and CLIC [44,45] explored time stamping and analog readout schemes. SOI has a unique characteristic, that is, as a fully depleted substrate of active silicon. Its 0.2 μm CMOS process provides the same transistor density as 0.18 μm CMOS in HR CMOS. Therefore, it is envisaged that the CEPC vertex detector readout design can be applied to these two processes and exploit the advantages of each approach.

The depletion P-channel Field Effect Transistor (DEPFET) [46] is considered semi-monolithic because the first-stage amplification can be integrated into the pixel. The subsequent processing circuit is still connected to a separate ASIC. BELLE II plans to install a DEPFET-based vertex detector recently. It is helpful to

place the readout ASIC (the main heat source) outside the sensitive part of the detector itself while keeping the sensor inside to achieve extremely low power and low material budget. The challenge is to periodically sample the modulation current on a large pixel array in an interval of 20 μs/frame or less. Hybrid pixels have been used in the Hadron Collider for the past few decades, and now the CLIC R&D department is promoting a thinned sensor, which is bumped to a 50 μm thinned ASIC at a 25 μm pitch [47]. Hybrid methods continue to evolve and benefit from the development of industrial technology. However, it seems unlikely that pixel pitches as small as the one needed by the CEPC is achievable with hybrid devices. In addition to the Very-Deep Sub-Micron (VDSM) [104] ASIC technology that achieves complex functions and excellent performance, the industrial development of vertical and horizontal interconnection technologies may also help satisfy a low material budget.

Summary

The CEPC will consist of a 100 km circumference accelerator system located in an underground tunnel to carry out precision measurements in the energy range 240 GeV to 91 GeV (Higgs and Z "factory" modes). The CEPC will include space reserved for a future Super Proton Proton Collider. Two primary detector concepts were studied, a baseline detector concept with two approaches to the tracking systems and an alternative detector concept with a different strategy for meeting the jet resolution requirements. The vertex detector is one of the critical elements among those detectors. It is placed at the innermost layer and has the most stringent requirements. Most critically, it should provide an excellent spatial resolution. Several silicon technologies were introduced in this chapter. According to the requirement of the vertex detector, the MAPS is the most promising one due to its high spatial resolution, fast readout speed, low material budget, and low power consumption.

Chapter 2

State of the art Monolithic Active Pixel Sensors (MAPS)

This chapter reviews the state of the art of MAPS used in high-energy physics

experiments. A brief overview of solid-state physics for particle detectors is given in section 2.1. It covers the concept of PN junctions, the interaction of the charged particles and photons with matter, signal formations, radiation damage, hybrid pixel detectors, and monolithic pixel devices. Section 2.2 describes the ALPIDE chip used in the ALICE experiment. Depleted MAPS designed for the ATLAS experiment are covered in section 2.3. Some previous prototypes for the CEPC vertex detector have been presented in section 2.4. And section 2.5 is a summary of these prototypes. A table list is summarized at the end of this chapter to compare different pixel sensors and provide a solution for realizing a fully functional prototype for the vertex detector.

2.1 Silicon sensors

A silicon sensor is a PN-junction depleted by applying a reverse voltage. Only a very small thermally generated current flows in a reverse-biased diode. As an external bias voltage is applied, a large electric field is built up in the depleted zone. Photons and ionizing particles crossing the sensor create electron-hole pairs. The electrons and holes would diffuse towards the depleted region. The charge carriers within the depleted region drift to the collecting electrodes in the electric field, inducing a signal. Thus, the generated signal is much faster compared to the conventional APS [48] (where charge collection is diffusion). From the known position of the electrode where the signal is induced, the position of the ionizing particle can be deduced. Position information can be obtained by segmenting the electrodes creating many independent diodes. In the following sections, these aspects will be discussed in more detail.

2.1.1 The PN Junction

Silicon crystal can be doped with donors' atoms (elements of group V) or acceptors atoms (elements of group III), making the silicon n-type or p-type, respectively. Dopants will introduce available energy levels in the band diagram, which translate in a displacement of the Fermi level [105] from the intrinsic level towards the conductive band in the case of n-type or to the valence band the case of p-type material. The basic element of a silicon particle sensor is the PN junction, which consists of n-type silicon in contact with p-type silicon. A schematic view of a PN junction at equilibrium is shown in figure 2.1. Putting in contact n-type and p-type

materials, the different concentrations of majority carriers will lead to a diffusion current, removing all free carriers from the junction region. Ionized dopants fill the junction area. This area is referred to as the space-charge region or depleted region. The fixed charge of the ionized dopants will generate a built-in potential V_B, as shown in figure 2.1. This figure shows the abrupt model of the PN junction, and it includes schematics of space charge density, electric field, and electrical potential. The potential generates a drift current, which balances the diffusion current. A reverse bias voltage V_R can be applied to the junction in the same direction of V_B, making the space charge region W larger than the one at equilibrium. Defining N_D and N_A as the donors and acceptor concentrations, x_n and x_p as the space region extensions as shown in figure 2.1, the total space width W can be calculated with the next equation [49]:

$$W = x_n + x_p = \sqrt{\frac{2\epsilon_S(V_B+V_R)}{e}\left[\frac{N_A+N_D}{N_A N_D}\right]} \tag{2.1}$$

where ϵ_S is the permittivity of the semiconductor, and e is the electron charge.

The proportionality factor between the current density and the electric field is the conductivity σ or, equivalently, the specific resistance ρ of the material. The conductivity is proportional to the concentration of donors and acceptors, and it can be found as:

$$\sigma = \frac{1}{\rho} \tag{2.2}$$

where resistivity ρ is dependent on the mobility of each charge carrier, which is also dependent on the electric field applied across the silicon. μ_e and μ_h are the mobilities, n and p are the densities respectively of electrons and holes. This equation can be

$$\rho = \frac{1}{e(\mu_e n+\mu_h p)} \approx \frac{1}{e(\mu_d N_d)} \tag{2.3}$$

In the case of a much greater number of charge carriers of a particular type, this equation can be simplified as shown in equation 2.3, where μ_h and N_d are the mobility and density of the majority dopant. Comparing with 2.1, one can find that

$$W \propto \sqrt{\rho(V_B + V_R)} \tag{2.4}$$

Therefore, high resistivity silicon requires a lower voltage to reach the same depletion depth W. This is relevant as the depleted volume of a PN junction constitutes the sensitive region of a particle detector. If the n and p regions have different doping concentrations, the depletion will extend more in the higher resistivity zone, the less doped one. The charge carriers generated inside the depletion region W will drift towards the edges of the region because of the electric field. The thermally generated carriers will form the leakage current, which will increase with the volume of the depleted region.

2.1.2 Interaction of Charged Particles with Matter

When charged particles pass through matter, they interact with the material atoms, thus continuously losing part of their energy. For relativistic charged particles in a momentum range of $\beta\gamma \in [0.1,1000]$, the mean energy loss per distance is described by the Bethe-Bloch equation [50]:

$$-\langle\frac{dE}{dx}\rangle = \frac{Kz^2Z}{A}\frac{1}{\beta^2}\left(\frac{1}{2}ln\frac{2m_ec^2\beta^2\gamma^2W_{max}}{I^2} - \beta^2 - \frac{\delta(\beta\gamma)}{2}\right) \tag{2.5}$$

with $K = 4\pi N_A {r_e}^2 m_e c^2$, where N_A is the Avogrado number, r_e is the classical electron radius and m_ec^2 is the electron rest mass. z is the charge of the particle in multiples of the electron charge, Z is the atomic number of the medium, A is the atomic mass of the medium, W_{max} is the maximum energy transfer in a single

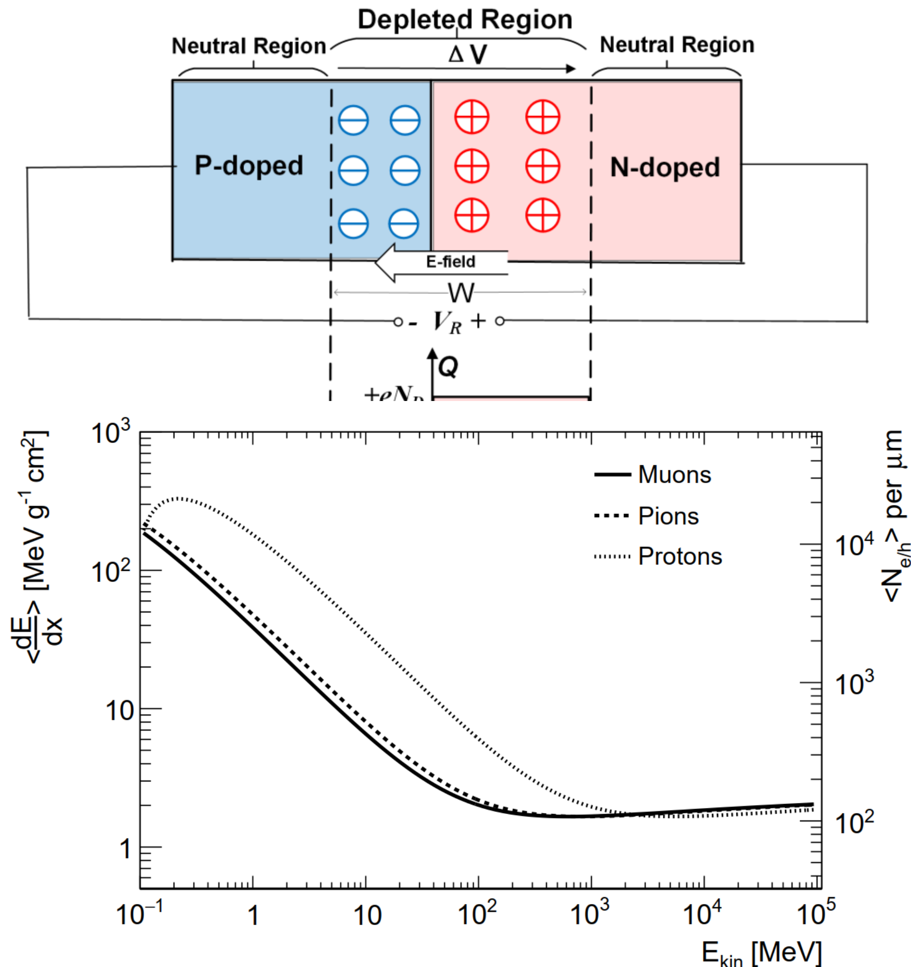


Figure 2.2 Average stopping power for muons, pions and protons in silicon as a function of the kinetic energy. The average number of created electron/hole pairs per micrometer is also shown. Adapted from [52].

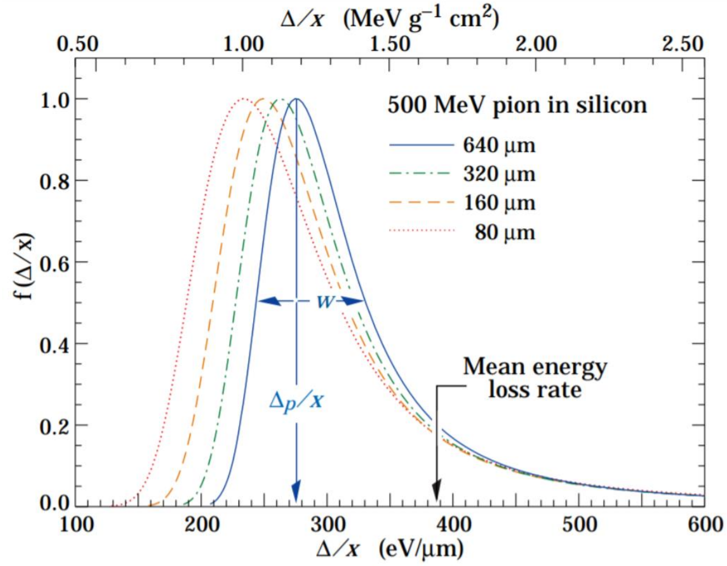


Figure 2.3 Landau distribution of the deposited energy by 500 MeV pions in silicon for different silicon thicknesses. The distributions are normalized to the most probable value of each distribution. Adapted from [53].

collision, I is the mean excitation energy of the medium, $\beta = v/c$, $\gamma = \frac{1}{\sqrt{1-\beta^2}}$ is the Lorentz factor, and $\delta(\beta\gamma)$ is a correction factor for high energy ionization [51]. The Bethe-Bloch formula is shown in figure 2.2 for muons, pions, and protons in silicon. The formula has a minimum at $\beta\gamma \sim 3$ (around 500 MeV for pions) that hardly increases for several orders of magnitudes of momentum. At this point, particles are called Minimum Ionizing Particles (MIPs). A MIP has an average stopping power of dE/dx = 1.66 MeV cm^2/g in silicon, which corresponds to the creation of about 107 e/h pairs per µm. Note that in silicon, 3.6 eV is required to create an electron/hole pair, this is higher than the band-gap of 1.12 eV due to the indirect band-gap that requires the creation of phonons for momentum conservation.

The energy loss probability distribution follows roughly a Landau distribution. This asymmetric distribution has a long tail, thus shifting the mean energy loss to higher values. Therefore, it is more common to quote the most probable value Δp (MPV) of the Landau Distribution:

$$\Delta \mathrm{p} = \xi \left[\log \frac{2m_e c^2 \beta^2 \gamma^2}{I} + log \frac{\xi}{I} + 0.200 - \beta^2 - \delta(\beta\gamma)\right] \tag{2.6}$$

with $\xi = (K/2)\ [Z/A]\ (x/\beta^2)$ MeV for a detector with a thickness x expressed in g/cm^2. The MPV of this distribution thus depends on the active thickness. The distribution for a MIP for several detector thicknesses is shown in figure 2.3.

2.1.3 Interaction of Photons with Matter

Photons interact differently than charged particles when passing through matter.

They do not lose energy continuously along their path but instead release most of their energy locally after being absorbed by the material. The absorption probability increases exponentially with the penetration depth, and the cross-section (and absorption mechanism) also depends on the photon energy.

The main three processes in which photons usually produced in the context of HEP experiments interact with matter are the following:

Photoelectric Effect: The photon is completely absorbed by an atom and frees an electron, with an energy equal to the photon energy minus the ionization energy. The cross-section of this process strongly depends on the proton number Z of the atom ($\sigma_{pe} \propto Z^n$ Where n ranges from 4 to 5 [54]), thus materials with high Z have a much higher probability for photon absorption. This effect is the dominating contribution to the cross-section in silicon at energies below 100 keV. For higher energies, the cross-section falls off several orders of magnitude.

Compton Scattering: At higher energies between ~ 100 keV and ~ 10 MeV. Compton scattering of the photons with the electrons in the material becomes a more important cross-section component. This process results in a lower energy photon and a recoil electron.

Pair Production: For photon energies above twice the electron rest mass (1.022 MeV), *e/h* pairs can be created. If the *e/h* pairs are created with high enough energy, they can, in turn, create further photons through bremsstrahlung.

2.1.4 Signal Formation

The *e/h* pairs generated by a traversing particle will induce a signal into the electrode. This is usually referred to as charge collection, this name is somehow misleading as it associates the signal formation only to the charge reaching the electrode. The actual current formation starts before this occurs [55]. The generated free charge, in a depleted PN junction, will move by drift under the effect of the electric field E, with an average velocity that can be expressed as:

$$v_{e/h} = \mu_{e/h} E \tag{2.7}$$

The mobilities of electrons and holes $\mu_{e/h}$ in silicon at T=300K usually are μ_e= 1400 cm^2/V/s and μ_h= 450 cm^2/V/s, respectively.

From the Shockley-Ramo theorem [55] [56] the induced current will be

$$i = e\vec{v} \cdot \overrightarrow{E_w} \tag{2.8}$$

The weighting field $\overrightarrow{E_w}$ is obtained by applying a unit potential to one electrode, zero potential to all the other electrodes, and solving the Laplace

equation $\nabla^2 \Phi_w = 0$, where Φ_w is the weighting potential. In this case, the unit potential is applied to the collection electrode. The collected charge is the integral of the current i over the collection time:

$$Q = \int_{t1}^{t2} i(t)dt = \mathrm{e}\Phi_w \tag{2.9}$$

This assumes that in the time frame, all the charge carriers reach the electrodes. Thus, the collected charge is equal to the number of generated electron/hole pairs. One should notice that if the electrode is smaller or comparable to the detector thickness, the weighting potential will get considerably smaller along the sensor depth. Therefore, in the case of small electrodes with respect to the detector thickness, the charge has to travel almost to the collection electrode to induce a current. Usually, only one electrode is read out in silicon sensors; therefore, only one charge carrier will contribute to signal formation. Sensors are usually operated under full depletion to avoid charge recombination, which would reduce the induced signal.

2.1.5 Radiation Damage

In the HEP experiments, the detector around the interaction point is exposed to the large flux of high-energy particles produced by the energy released by proton-proton collision. These particles will damage the detector and reduce its performance. Thus, it is important to design a radiation-resistant detector to ensure reliable performance before the end of detector life. Radiation damage can be divided into two main types: ionization damage and displacement damage. Ionization damage, also known as surface damage, is caused by the ionization energy loss of photons and charged particles. It affects the silicon oxide on the detector surface and the interface between silicon oxide and silicon. The displacement damage is mainly caused by hadrons, which displace silicon atoms from the lattice. This is the main source of radiation damage in the silicon bulk and impacts charge collection and leakage current. One consequence of displacement damage is the effective removal of the initial receptor.

- **Surface damage**

  Surface radiation damage or ionization damage occurs after the electron-hole pair is generated by the incident radiation of the ionizing medium. Its range is measured by the total ionization dose (TID) absorbed by the material. TID is measured in Gray (Gy = *J/kg*) or equivalent in rad (1 rad = 0.01 Gy). In the silicon lattice, the newly generated carriers recombine almost instantaneously,

so there is no long-term effect. On the other hand, there will be persistent defects at the interface of silicon oxide SiO_2 and SiO_2-Si. The decisive factor is that the mobility of holes in SiO_2 is very low, while the electron mobility prevents holes from leaving the oxide and recombining [57]. This leads to the accumulation of trap holes in the SiO_2-Si interface, resulting in a positive space charge in the oxide. The improvements in integrated circuit technology, whose basic unit is the transistor, resulting in thinner gate insulation. This has a positive effect on TID radiation tolerance. When the thickness of typical gate oxide decreases in the range of several nanometers, the captured holes are likely to escape the trap and recover part of the radiation damage through the tunnel effect. For more details of surface damage, examples can be found in [58,59].

- **NIEL Scaling Hypothesis**

Through the Non-Ionizing Energy Loss (NIEL) hypothesis, a common basis for comparing the degree of displacement damage from different sources is established. It shows that the degree of displacement damage is linearly proportional to the energy transmitted in displacement collision but independent of the spatial distribution of subsequent defects. NIEL assumes at a given fluence Φ (number of particles per unit area), the damage of any particle can be scaled to the damage of the reference particle according to certain energy. The usual reference particle is a 1 MeV neutron. The following formula is used to calculate the equivalent fluence Φ_{eq}:

$$\Phi_{eq} = k\Phi = k\int_{E_{min}}^{E_{max}} \Phi(E)dE \tag{2.10}$$

Where k is the hardness coefficient, which scales each particle displacement damage and energy to 1 MeV neutron equivalent. The hardness coefficient can be determined by using the weighted fluence of energy-related displacement damage cross-section $D(E)$ and normalized to the integral fluence and damage cross-section of reference particles.

$$k = \frac{\int_{E_{min}}^{E_{max}} D(E)\Phi(E)dE}{D(E_n{=}(1\ MeV))\int_{E_{min}}^{E_{max}} \Phi(E)dE} \tag{2.11}$$

For 1 MeV neutrons, D (En= $(1\ MeV)$) =95 MeV mb. The NIEL hypothesis relates the fluences from different particles equivalent to the 1 MeV neutron fluence. It can help study the devices in different radiation environments.

- **Impact on Sensor Performance**

Ionization damage to silicon sensors is not the main issue since free charge carriers recombine and the initial state can be recovered. On the other hand, displacement damage caused by non-ionizing energy depositions affects the charge collecting properties of the silicon bulk. It occurs when an incident particle knocks an atom out from its site in the crystal lattice and creates a Frenkel pair [60]. Around 60% of interstitials and vacancies recombine on the spot, while the rest interact with each other or with impurity atoms to produce point defects [61]. This leads to an energy state of deep levels in the band-gap. If the imparted energy on the displaced atom is high enough, the primary knock-on atom (PKA) can displace further atoms with cluster defects.

Both point defects and cluster defects can change the electrical properties of silicon and cause radiation damage in bulk. There are three main effects on the sensor performance.

1) A change in the bulk doping concentration that affects the sensor depletion region. Typically, the radiation induces an acceptor-like state, increasing the acceptors and leading to a higher depletion voltage. Increasing the voltage may result in a breakdown, which may limit the possibility of achieving a full sensor depletion.
2) Increase leakage current. The leakage current increases linearly with fluence and has several adverse consequences to the detector. It results in a higher shot noise and leads to a reduced SNR (Signal Noise Ratio). Besides, it also brings a higher ohmic loss to the sensor and produces uncontrolled sensor heating. To avoid thermal runaway, cooling systems are usually needed when operating silicon detectors.
3) Decrease charge collection efficiency due to defects (charge trapping). The deep level introduced by radiation acts as a trap for drift charge carriers. If the time for the trapped charge to be released from the defect is greater than the shaping time of the electronic device, the charge is effectively lost and is not detected, resulting in a reduction in the SNR. Radiation also inhibits the charge collection by diffusion, partly due to capture and the increased charge recombination on the defects introduced by radiation.

Some defects can recover with time since the energy level of the induced defects is higher than a pure lattice structure. This is usually called the annealing process, which is strongly temperature-dependent. Sometimes defects produce stable complexes in oxygen or phosphorus atoms combination

that cannot anneal over time [62].

2.1.6 Hybrid Silicon Pixel Detectors

Hybrid detectors used in the LHC experiments are usually composed of a silicon sensor, a two-dimensional array of (typically) 100×100 μm^2 PN-diodes, connected to a readout ASIC with a similar array of readout channels. The channels on the sensor and ASIC are connected through small (25 µm diameter) solder balls through a complicated alignment, heating, and compression process called bump-bonding. The fact that the readout and the sensor part of the detector are separate entities has the advantage that the technology for each part can be optimized independently. However, hybrid detectors suffer from some limitations. The bump-bonding coupling of the sensor and the ASIC adds a high cost to the detector assembly (about a factor of 2). At the same time, it increases the system capacitance as well, which is usually of the order of hundreds of fF. It also limits the minimum pixel size that can be achieved to the minimum solder ball diameter. This last point effectively rules out hybrid devices for the CEPC.

2.1.7 Monolithic Active Pixel Sensors

Monolithic Active Pixel Sensors are made in standard CMOS technology, often with some process adjustments. The cornerstone of this approach is that these devices include both sensor and front-end in the same substrate. The availability of high resistivity substrates compatible with CMOS technology has enabled the development of Depleted-MAPS (DMAPS), which are of high interest in HEP (High Energy Physics) experiments, where the amount of charge collected (or generated signal) degrades with radiation fluence. Monolithic detectors offer advantages in detector assembly and production cost, as no flip-chip process is needed.

Two different DMAPS design approaches are described in the following sections. These are often called *large collection electrodes* and *small collection electrodes* [63,106]. For sensors in HEP, the *e/h* can be generated relatively far from the collection electrode and travel in the depleted volume inducing a signal, even in a small collection design.

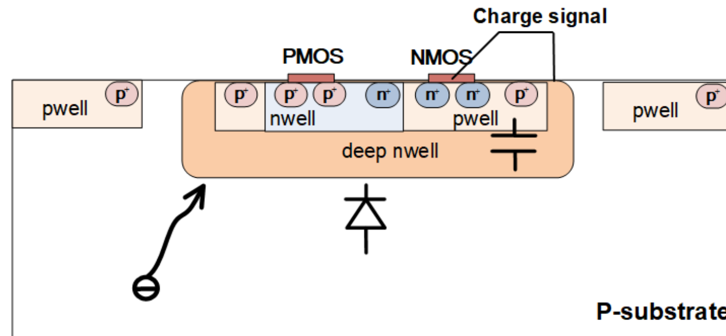


Figure 2.4 Large collection electrode design

2.1.8 Large Collection Electrode

In monolithic devices, the NMOS transistors are isolated from the sensor with a deep pwell layer. In the cross-section in figure 2.4, the deep nwell constitutes the collection electrode, which extends underneath the pixel area, and the substrate here is p-type. Using such a large implant, which is the basis of the large collection electrode approach, improves the radiation hardness because a large depletion region can be easily achieved, and the electrons have to travel a short path to generate a current. The pixel capacitance is comparable to a hybrid detector (> 100 fF) due to the large junction between the p-substrate and the deep nwell. Therefore, they do not present advantages for hybrid pixel detectors regarding signal-to-noise ratio, power consumption, and crosstalk. It is critical to highlight that the total capacitance of the pixel has two main contributions: the capacitance of the deep nwell/p-substrate and the capacitance of the pwell/deep nwell. The former is not present in the small collection electrode sensors as we shall see below.

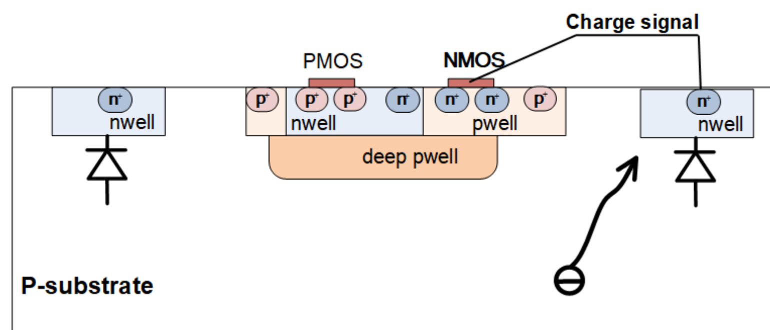


Figure 2.5 Small collection electrode design

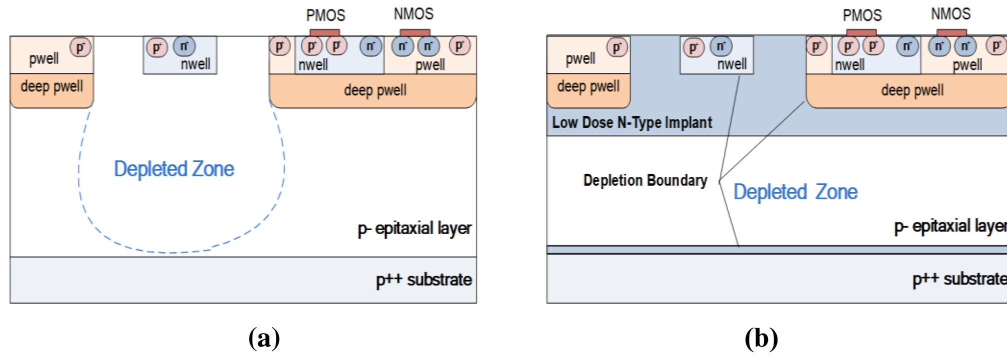


Figure 2.6 Cross section of the standard process (a) and modified process (b)

2.1.9 Small Collection Electrode

In this approach, the free carriers diffuse to the depletion region which is small compared to the full pixel size. The in-pixel circuits are isolated using a deep pwell, which prevents electrons from being collected by the PMOS nwell, as shown in the cross-section in figure 2.5. The collection electrode with an area of a few μm^2 induces a signal at the input of the front-end, with a much smaller input capacitance ($\sim$ 5 fF), improving power consumption, timing performance and noise with respect to hybrid pixel detectors and monolithic large collection electrode designs. However, the spatial separation of charge collection from digital electronics and the large distance between collection electrodes (in the order of the pixel pitch) reduces the risk of crosstalk. Furthermore, as the junction is relatively small, it is not easy to fully deplete the sensor and the e/h pairs diffuse across a longer path (about half of the pixel pitch), affecting operation after irradiation. As discussed in the following section, in principle, this limitation can be overcome with a process modification, including an additional n-layer.

2.1.10 A Multiple Wells Technology

A CMOS multiple wells technology for small collection electrode pixel sensors was developed for the ALPIDE chip [64], implemented for the ALICE ITS upgrade. As mentioned above, the advantage of a small collection electrode design is the low pixel capacitance (< 5 fF), which reduces the power consumption requirement of the front-end. The cross-section of a pixel is shown in figure 2.6(a). The process is the same as the one presented in figure 2.5. A high resistivity (> 1 kΩ) p-epitaxial layer is grown on a p-type substrate. Typical values for the thickness of this layer

are in the range between 18 and 30 μm. A small nwell constitutes the collection electrode. Hybrid pixel front-end chips use the die substrate as a ground reference. In this monolithic technology, it is crucial to reversely bias the p-epitaxial, and therefore the substrate, with respect to the collection electrode, to collect charges and deplete the sensing volume. The electric field in the depleted volume allows collecting by drift the electrons generated by the energy deposition of an ionizing particle, which are transported towards the nwell collection electrode generating a signal. Inside the undepleted volume, instead, the diffusion transport is dominant, which, as already discussed, is slower and more sensitive to degrade with irradiation. The nwells of the PMOS will collect electrons if not shielded. They are typically biased at 1.8 V, limiting the electrode charge and causing a noise injection into the electronics. Therefore, a high-dose deep pwell implant is added to separate the CMOS electronics from the epitaxial layer.

A process modification has been developed to increase the depletion region in these small electrode devices. A low dose n-layer is introduced underneath the collection electrode, covering the entire pixel area, as shown in the cross-section of the technology in figure 2.6 (b). The n-implant is sufficiently low dose to fully deplete up to the nwell implant of the collection electrode, with a reverse bias of a few Volts. This yields a sensor capacitance of only a few fF. Before full depletion is achieved in the n- layer, the front-end input capacitance is much higher than at full depletion. Since the pwell in the pixel matrix and the substrate are now separated by a depletion layer and hence isolated, they can be biased independently, provided a sufficiently large potential barrier prevents the holes in the pwell from entering the epitaxial layer and hence avoids punch-through [65].

As it has been seen, monolithic pixel sensors offer high position resolution and low material budget. In the following sections, some recent monolithic prototypes will be introduced. The ALPIDE chip is the first to use a quadruple well process to develop a pixel detector in high energy physics. Both NMOS and PMOS transistors could be used in the pixel design, while in the previous double-well process, only NMOS can be used. For the ATLAS inner tracker upgrade, depleted MAPS prototypes were designed to cope with a very high events pile-up [66], though they were finally not adopted as the baseline technology for the High Luminosity LHC upgrade. The sensors and the readout architecture have to be fast enough to match the hit rate requirement within 25 ns of the bunch crossing. The feasibility of the modified quadruple well process was taken into consideration. The following sections will introduce two prototypes, the TJ-Monopix [100,112] and the TJ-

MALTA [101,113].

2.2 MAPS for the ALICE experiment

As mentioned above, the ALPIDE chip was fabricated with a 180 nm CMOS imaging sensor (CIS) process from TowerJazz [70]. The signal sensing element is a nwell diode (about 2 μm in diameter). This area is much smaller than the area of the pixel cell. The electrons reaching the depleted volume of the diode induce a current signal at the input of the pixel front end. The size of the ALPIDE chip is 15 mm × 30 mm, including a matrix of 512×1024 pixel cell, and the size of each pixel unit is 29.24 μm×26.88 μm. The analog bias, control, readout, and interface functions are implemented in the 1.2×30 mm^2 peripheral area.

As it is shown in figure 2.7, each pixel unit includes a sensing diode, a front-end pre-amplifier with a shaping stage, a discriminator, and a digital part. There is a pulse injection capacitor in each pixel, which is used to inject test charges into the input of the front end. The digital part includes three hit storage registers (multi-event buffer) and a pixel mask register. The front end and the discriminator are always active. The pre-amplifier has a non-linear response, and their transistors have a bias in weak inversion. Their total power consumption is 40 nW/pixel. The small-signal gain of the front end is 4 mV/e^-, the equivalent noise charge is 3.9 e^-, and the minimum threshold is lower than 100 e^-.

The capacitance of the sense diode has a typical value of 2.5 fF. The input capacitance of the front end is less than 2 fF. The peaking time of the front end is about 2 μs, while the typical duration of the identified pulse is 10 μs. The front end and discriminator act as an analog delay line. This delay is longer than the waiting time of the first level trigger in ALICE. The chip can be operated in trigger mode, meaning the data is stored until a trigger signal arrives, and then the corresponding data is read out. The general threshold level is applied to all pixels. The global strobe signal controls the latch of the identified hit point in the storage register. The event frame will be saved in one of the three frame memory slices when the strobe is triggered. Reading out the frame data from the matrix is zero suppressed and is performed by a priority encoder circuit. There are 512 pixels of this circuit, one for every two-pixel column. The priority encoder sends the address of the first pixel to the periphery when it has the hit in a double column. Then, the storage element of the pixel is reset. This cycle is repeated until the addresses of all pixels that initially present a valid hit value at the input of the priority encoder have been

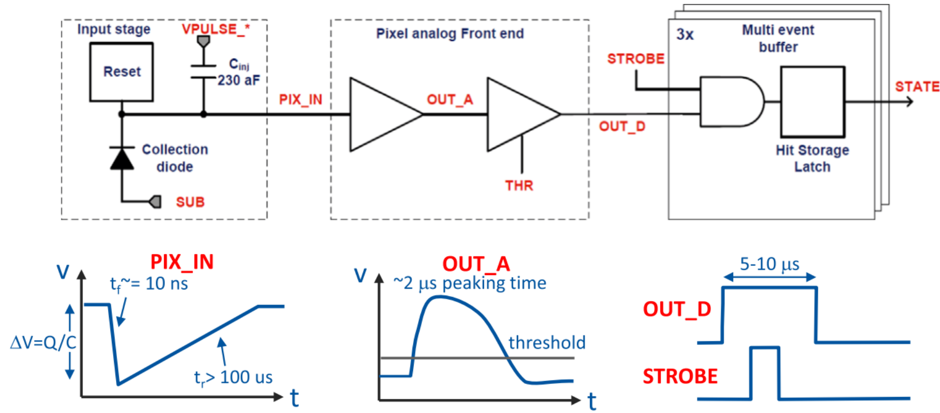


Figure 2.7 Block diagram of the ALPIDE pixel cell. Taken from [40].

transmitted to the peripheral device. Each priority encoder is set as a unit, a completely combined circuit consisting of peripheral sequential logic during the readout matrix frame [25]. It is implemented in a very narrow area between pixels and extends vertically over the entire height of the column. There is no free-running clock allocated in the matrix, and if there is no hit to read, there is no signaling activity. The average energy required to encode the address of the hit pixel is about 100 pJ. The power consumption is proportional to the reading rate and the hit occupancy rate. For the nominal design value, the reading of the matrix consumes approximately 3 mW. The priority encoder also realizes the readout of the pixel and the buffering and distribution of the configuration signal through the offset of the pixel front end. The analog power consumption of the ALPIDE chip is usually 25 mW.

2.3 DMAPS prototypes “TJ MALTA” and “TJ Monopix”

The prototypes designed for the ATLAS inner tracker upgrade include a complete analog front end and all in-pixel digital readout logic with a pixel pitch of approximately 36 µm to 40 µm. Especially interesting for the CEPC is the ATLAS prototype fabricated using the improved TowerJazz 180 nm process, two different readout architectures have been designed and implemented for small electrode size CMOS sensors in this process: the asynchronous readout scheme ("TJ MALTA") and the synchronous readout scheme ("TJ MonoPix"). The asynchronous design avoids the clock propagation in the active pixel matrix area, thereby reducing the risk of crosstalk and providing the best low-power operation. Each hit address, time,

and charge information are encoded in an asynchronous signal propagated to the peripheral device via the column bus. The address is decoded, and the arrival time and deposited charge are measured. Then, the decoded information is buffered and transmitted from the sensor. However, the asynchronous approach is challenging in complexity, and it is not well established as the synchronous solution. The synchronous design is based on the column emission architecture. Hits are buffered in pixel units, and the "token" clock signal passes through each pixel from top to bottom in a column. If the pixel is hit, the pixel address is declared to the column bus when timing the pixel. At the end of the column, a timestamp is added and the threshold time is encoded using a 40 MHz beam cross clock. In both architectures, the end-of-column logic buffers all hits on the sensor and transmits the hits off-chip. MALTA is a complete ATLAS size sensor with a pixel pitch of 36.4×36.4 μm^2 and asynchronous reading of a 512×512 pixel matrix. TJ MonoPix is a half-size ATLAS sensor with a pitch of 36.4×40 μm^2 and a 224 ×448 pixel matrix simultaneous reading. MALTA and MonoPix share the same analog front-end design aimed at reducing noise and power consumption. The analog front end includes a charge-sensitive amplifier, followed by a discriminator and hit buffer. The design goal is that the analog current per pixel is in the range of 250 nA to 500 nA, making the analog power consumption less than 70 mW/cm^2. In contrast, the estimated digital power consumption of the outer matrix readout is lower than MonoPix's 100 mW/cm^2, and the MALTA is less than 10 mW/cm^2. The analog front end and in-pixel logic are fully custom-designed to achieve the best performance and optimal pixel area utilization. The distance between the collecting electrodes is 3 µm to 4 µm.

2.4 Previous prototypes designed for the CEPC vertex detector

The R&D program to study the viability of MAPS for the CEPC vertex detector started in 2016 within the MOST1 project (supported by the Ministry Of Science and Technology of China). Several prototypes were produced to study the performance of different architectures. JadePix-1 [67,117,118] and JadePix-2 [68] were designed with different pixel sizes to investigate the large area and high-resolution devices. And another prototype, the MIC4 [69], was designed to study a data-driven readout architecture [119]. The results of the MOST1 are promising but distant from a complete prototype that is needed for the CEPC vertex detector, so the MOST2 project was launched in 2018 to develop a fully functional pixel sensor and implement the baseline structure of the inner tracking detector. The first result of this effort was the TaichuPix1. The cross-section of this prototype is shown in figure 2.8. The sensor and readout electronics are integrated on the same

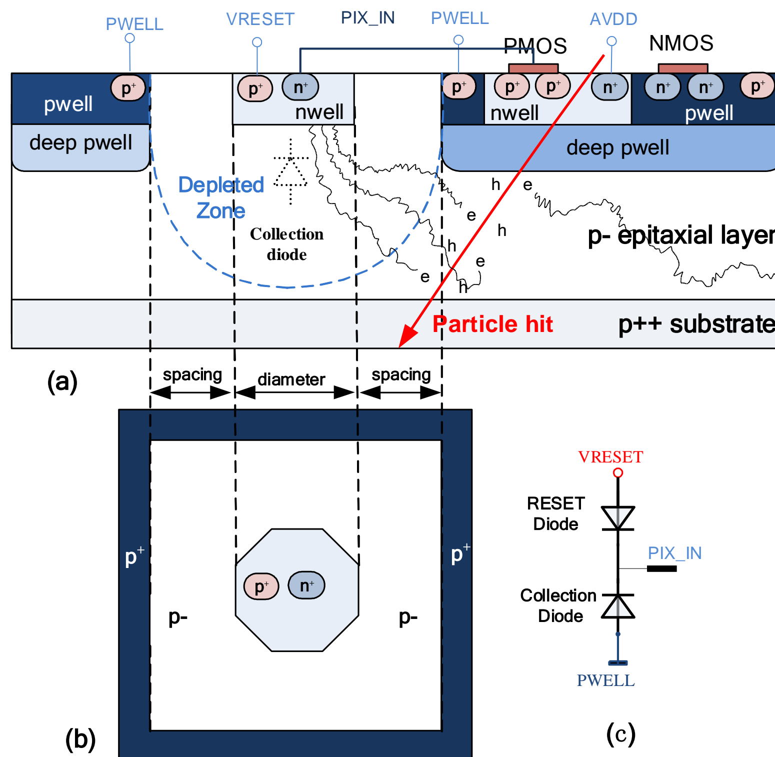


Figure 2.8 Cross section(a), top view(b) and RESET schematic(c) of TaichuPix1

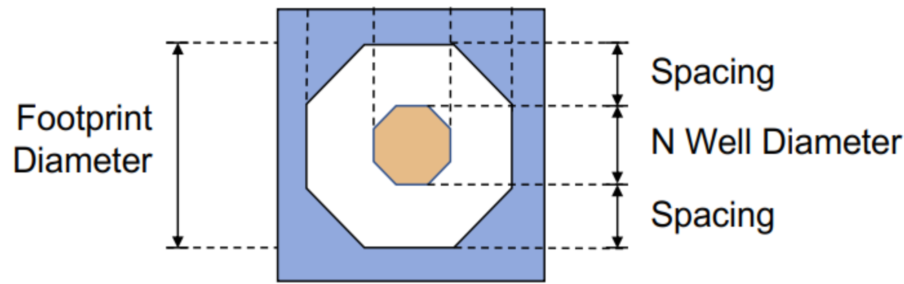


Figure 2.9 Cross sectional view of JadePix-1 and schematic of its in-pixel readout circuitry. Taken from [67].

silicon bulk, similar to figure 2.6(a). The readout electronics are integrated inside a deep pwell surrounding the collecting electrode with an octagonal shape (figure 2.8 (b)). The diameter of the nwell electrode is 2 μm and the nwell to pwell spacing is between 2 and 3 μm, while the total dimension of the pixel in one direction is 25 μm. The sensor reset is provided by a diode which makes the sensor compact. The schematic of this method is illustrated in figure 2.8 (c). All of the prototypes mentioned above are introduced in detail in the following context.

JadePix-1is the first prototype developed for the CEPC vertex detector to study the performance of different sensor geometries. JadePix-1 has implemented several different pixel sectors on the same chip. The electrode area and footprint are two critical elements in sensor diode geometry that impact the sensor charge collection performance. As it is shown in figure 2.9, the diode surface is made into an octagonal shape, with the area varied from 4 um^2 to 15 um^2. Experimental results show a larger diode surface would improve the charge collection efficiency but increase sensor noise. The footprint is defined as the total area formed by the surrounding pwell. The measurements done on these prototypes show larger footprint has a small impact on the sensor gain. However, it can improve charge collection efficiency. The signal readout electronics are inside the shielding deep pwell. The JadePix-1 is a 7.9 × 3.9 mm^2 chip with two-pixel matrices fabricated in a process shown in figure 2.6(a). Matrix-1 contains large pixels of 33×33 μm^2, while Matrix-2 contains small pixels of 16×16 μm^2. Conventional 2/3 T source-follower [71] readout structures are implemented to read out the analog signals. After the characterization at DESY [72] using an electron beam, the obtained spatial resolutions are 5 μm and 3.5 μm for the 33×33 μm^2 and 16×16 μm^2 pixels, respectively.

JadePix-2 is the second prototype designed for the vertex detector, and it is

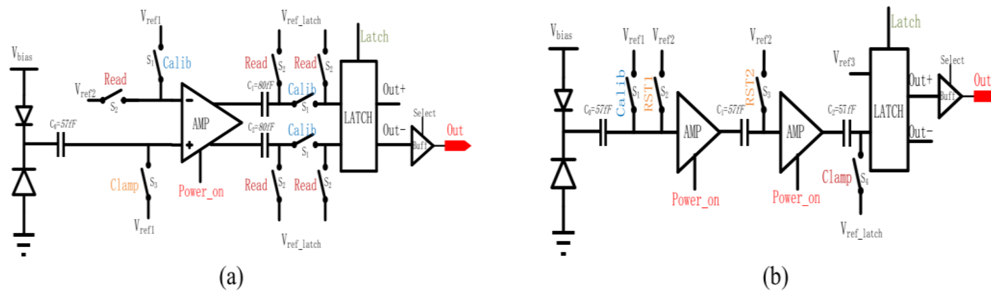


Figure 2.10 Two pixel structures with a differential amplifier and Latch (a), and two stage Common-Source amplifier and Latch (b). Taken from [68].

focused on the in-pixel readout logic implementation. The full dimension of JadePix-2 is 3×3.3 mm^2, containing 112×96 square pixels with 22 μm pitch size. Two in-pixel digitalization circuits are proposed, as shown in figure 2.10, both designs employ a high-voltage biased charge collection diode (Vbias up to 10 V), and a comparator with output offset storage (OOS) technique [73] to mitigate the output offset of the amplifiers from pixel to pixel. Collected charges are converted proportionally into a voltage signal, which is AC-coupled to the discriminators. The voltage signal is amplified and compared with a threshold voltage of discriminators. The hit result of '1' or '0' is then stored in the latch and transferred row-by-row to the column through a digital buffer. The main difference between the two designs lies in signal amplification, with one utilizing a differential amplifier and the other using a two-stage single-ended amplifier architecture. The pixel array is read out in the rolling shutter mode [74]. The averaged processing time is 100 ns/row and 80 ns/row, respectively. Experimental results show that the total ENC of the two structures is around 29.5 e$^-$ and 31 e$^-$, respectively.

Apart from the JadePix-1 and the JadePix-2, another prototype, the MIC4 (MAPS In CCNU) has been implemented in a pixel matrix of 128×64 with a pixel pitch of 25 μm in parallel. Figure 2.11 shows the architecture of MIC4, which could be divided into two parts, pixel array and periphery circuitry. Each pixel cell includes an analog front-end and digital readout logic, and one super pixel contains 64 pixels. And the periphery contains a band-gap, DACs, digital readout circuitry, 8B10B encoder, serializer, and an LVDS interface [120].

The experimental results show that the analog front-end features a peaking time of 1 μs, a shaping time of less than 3 μs, a charge threshold of 100 e$^-$, the average temporal noise of 6 e$^-$, and a fixed pattern noise of 36 e$^-$. The single event

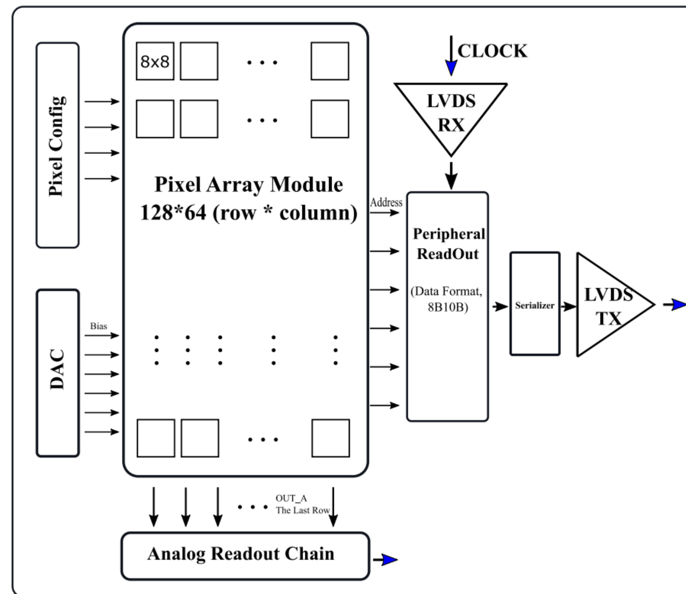


Figure 2.11 Block diagram of MIC4. Taken from [69].

latch-up probability is 1.02 × 10^{-6} cm^2 at 20.05 MeV cm^2/mg linear energy transfer. The addresses of the hit pixels can be read out in the digital part at a clock running at 30 MHz with the data-driven readout circuit architecture, which is different from the rolling shutter readout method of the JadePix-2.

A new prototype, the JadePix-3, was recently implemented with 180 nm CMOS process, which features a high spatial resolution, low power consumption, and modest readout speed [98,99]. The chip has a total area of 10.4 × 6.1 mm^2, with a pixel matrix of 512 rows ×192 columns, and a minimum pixel size of 16×23.11 μm^2. The chip uses the rolling shutter readout approach, reading out one row at a time, and reset the previous row register when processing the matrix scanning. If the read time and reset time used for each row are evaluated at 200 ns, a total of 102 µs is required to complete the reading of 512 rows. The measured integral time for the matrix is 98.3 µs, while the power dissipation of JadePix-3 is less than 100 mW/cm^2.

2.5 Limitations of the existing MAPS for the CEPC vertex detector

Previous prototypes implemented within the MOST1 project concentrated on a few key performance aspects of the chip. However, these prototypes cannot fulfill the main requirements of the CEPC vertex detector completely, though they are useful as intermediate steps towards a more complete device. To move forward

with the program, benefiting from the MOST1 project, the MOST2 project was launched in 2018. The target of MOST2 is to develop a fully functional device that could implement a baseline vertex detector. As mentioned in chapter 1, the requirements for the CEPC vertex detector should be a small pixel pitch, a low power consumption, a fast readout speed, and a light structure. The pixel chip requirements for this work are summarized in table 2.1. It aims to implement a fully functional chip with a spatial resolution of around 3~5 μm, a pixel size of 25×25 μm^2, and satisfy the 25 ns bunching crossing with an operating frequency of 40 MHz, to the digital readout periphery. The data rate has to be 3.84 Gbps and 120 Mbps for the triggerless and trigger mode respectively. The radiation hardness for the Total Ionizing Dose (TID) shall be over 1 Mrad. To realize a detection efficiency higher than 99%, the dead time shall be less than 500 ns for each double column.

Power density is also a critical parameter, but for the first prototype, the functionality of the pixel is the priority. Power consumption of 50 mW/cm^2 or below is difficult to achieve at this stage, but this issue will be considered in the future.

Three major constraints are presented in table 2.1, the single point resolution, the readout speed, and the TID radiation hardness. Table 2.2 concludes some parameters of existing pixel sensors mentioned in this chapter. It is apparent that the ALPIDE chip has a small pixel pitch, but the interaction rate does not satisfy the requirement of the target of the CEPC vertex detector. Both TJ-Monopix and TJ-MALTA meet the interaction rate of 40 MHz, but the pixel pitch is not small enough. Therefore, none of the existing pixel prototypes could satisfy the

Table 2.1 Main design specifications of pixel sensor for this work

Parameter	Value
Single point resolution	3~5 μm
TID radiation hardness	>1 Mrad
Pixel size	25×25 μm^2
Operating frequency	40 MHz
Data rate	3.84 Gbps (Triggerless mode)
	160 Mbps (Trigger mode)
Dead time	<500 ns

Table 2.2 Parameters of the existing monolithic active pixel sensors

Parameter / Pixel Sensors	Pixel size (μm^2)	Spatial resolution (μm)	Readout architecture
ALPIDE	29.24×26.88	5	Hit driven
TJ-Monopix	36×40	-	Synchronous
TJ-MALTA	36.4×36.4	4	Asynchronous
JadePix-1	33×33/16×16	5/3.5	Rolling shutter
JadePix-2	22×22	-	Rolling shutter
JadePix-3	16×26/16×23	3-5	Rolling shutter
MIC4	25×25	-	Hit driven

requirements completely. It is inevitable to develop a new dedicated prototype that can meet all the requirements of the CEPC listed in table 2.1.

Benefiting from the previous prototypes designed in the MOST1 project and from the existing pixel chips of ALICE and the ATLAS experiment, a fully functional MAPS prototype, together with the column drain [112] readout architecture, based on the ALPIDE and FEI3 approaches, has been implemented to achieving a fast readout with a small pixel size of 25×25 μm^2. The name of this prototype is TaichuPix1, which is derived from the ancient Chinese text, and it refers to the beginning of the universe as the CEPC will explore the origin of the matter. Comparing to the existing pixel sensors, TaichuPix1 has the following enhancements:

The analog front-end has been optimized for a faster-rising edge and short time walk. The peaking time of TichuPix1 is below 400 ns, while this value to ALPIDE and MIC4 is 2 μs and 1μs, respectively.

The in-pixel readout logic for TaichuPix1 operates at 40 MHz, which meets the requirement of a 25 ns bunch spacing. It is the same as the TJ-Monopix and TJ-MALTA, but the pixel pitch is optimized to 25 μm.

Compared to the JadePix-1 and JadePix-2, TaichuPix1 is a fully functional prototype. Both pixel pitch and readout speed are taken into consideration. The high data rate digital periphery circuitry was designed. It supports two different readout modes, trigger and triggerless. And the interface data rate for these two modes is 5 MHz/32 bits and 120 MHz/32 bits, respectively.

Summary

This chapter presents the fundamentals of silicon sensors, including the working principles of the PN junction, the interaction of charged particles and photons with matter, and the signal formation inside the sensor. In addition, the hybrid silicon pixel detectors and MAPS are also introduced—the multiple wells' technology for small collection electrodes of the CMOS pixel sensor. In TowerJazz's 180 nm technology, the CMOS sensor implements a small collecting diode outside the deep pwell, containing all the electronic devices. Smaller collecting electrodes have the advantage that the analog circuit in the pixel matrix can be very simple, so only a small part of the pixel area is required. Therefore, a larger part of the surface can be used for digital circuits. Meanwhile, the lower capacitance of the smaller collecting electrode leads to lower dissipated power.

Several existing pixel sensors are shown in the later sections. Section 2.1 presents the ALPIDE chip from the ALICE experiment, which is a potential option for the CEPC vertex detector due to the low power consumption and small pixel size. Two monolithic prototypes recently designed for the ATLAS experiment are described in section 2.2 since pixel readout speed meets the requirements. Some prototypes developed during the R&D period of the CEPC vertex detector are shown in section 2.3. Though the results are promising, it concluded that these early prototypes do not meet the main requirements of the CEPC that are detailed in section 2.4. In summary, a new device, the TaichuPix1, is proposed as the fully functional prototype for the CEPC that aims to meet the main requirements of small pixel size, high readout speed, and high rate capabilities.

Chapter 3

TaichuPix1 Chip overview

The ultimate TaichuPix chip will consist of a 512×1024 pixel array with a 25 μm pixel pitch. In the development process of such a complex and critical ASIC, smaller chips are usually designed and fabricated to verify the feasibility of the new front-end electronics and readout architecture. TaichuPix1 chip is one of the small-scale prototypes with fully functional architecture. It aims to demonstrate the feasibility of the individual blocks and the performance of full architecture based on the column drain readout.

In this chapter, the general description of the chip (section 3.1) will be presented. Then every main block will be introduced one by one, including the in-pixel analog front-end, the in-matrix digital logic and the periphery circuitry. The physical implementation of the TaichuPix1 is described in section 3.5.

3.1 General description of the TaichuPix1

As mentioned before, for the full-scale prototype with the 1024×512 matrix [26], the expected hit density when operating at the Higgs boson and WW thresholds in the CEPC is around 2.5 hits/cm^2 per bunching crossing. At the same time, the readout system should be able to meet the 25 ns bunching spacing for the Z boson operating mode.

A block diagram of the small-scale prototype TaichuPix1[75] is shown in figure 3.1. The overall architecture can be divided into two parts, the pixel array, and the periphery circuitry. The TaichPix1 includes a matrix of 192×64 pixels. The in-matrix digital logic is implemented following two approaches, half of them follow the FEI3-like logic while the other half implements the ALPIDE-like scheme. Both pixel flavors employ the same readout scheme based on double column drain architecture. The pixel readout is arbitrated by priority logic, with the topmost pixel having the highest readout priority. Each double column is terminated with an EoC (End of Column). The EoC handles the column readout and includes a counter running at 40 MHz to generate the timestamp with a step

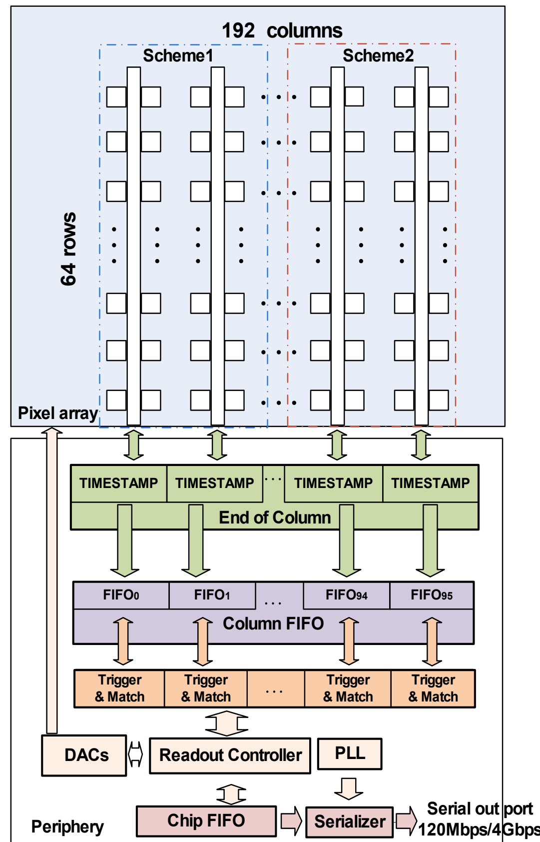


Figure 3.1 Block diagram of TaichuPix1 chip

of 25 ns. When a hit is detected in one of the pixels of the column, a flag is raised by the pixel, and the EoC immediately stores the current timestamp in a temporal buffer. The EoC identifies the pixel that was hit and transmits the stored timestamp and the address of the pixel to a first-level FIFO with a depth of 16. Data are stored there until the arrival of a trigger. Then a trigger match unit looks for data related to the received trigger in the first level FIFO. Matched data are transferred to a second level FIFO to be stored until they are passed to a serializer. Data transmission rates range from 160 Mbps to 4 Gbps. Triggerless mode is also supported to preserve all the readout data before buffering to be readout. In addition, the analog biasing is supported by the 8-bit current DAC (Digital to Analog Converter) and 10-bit voltage DAC, and the reference bias for DAC could be optional set up by external supply.

3.2 In-pixel electronics

As shown in figure 3.2, the pixel matrix is subdivided into two matrices of 96×64 pixels, each with a different in-matrix readout digital logic. Both schemes employ the same double-column drain architecture [77] in the peripheral part of the chip, as drawn in the bottom part of figure 3.1. The same EoC circuitry within peripheral readout logic was implemented.

Each pixel consists of a sensing diode and an analog front-end surrounded by the in-matrix digital logic. The analog front-end includes a preamplifier followed by a shaper and a hit discriminator based on the ALPIDE architecture. In this work, the in-pixel architecture was optimized for a faster-rising edge. Two digital fast in-matrix readout strategies have been implemented: an FEI3-like scheme (Scheme1 in figure 3.2) and an ALPIDE-like scheme (Scheme2 in figure 3.2) which benefited from the AERD (Address Encoder and Reset Decoder) structure.

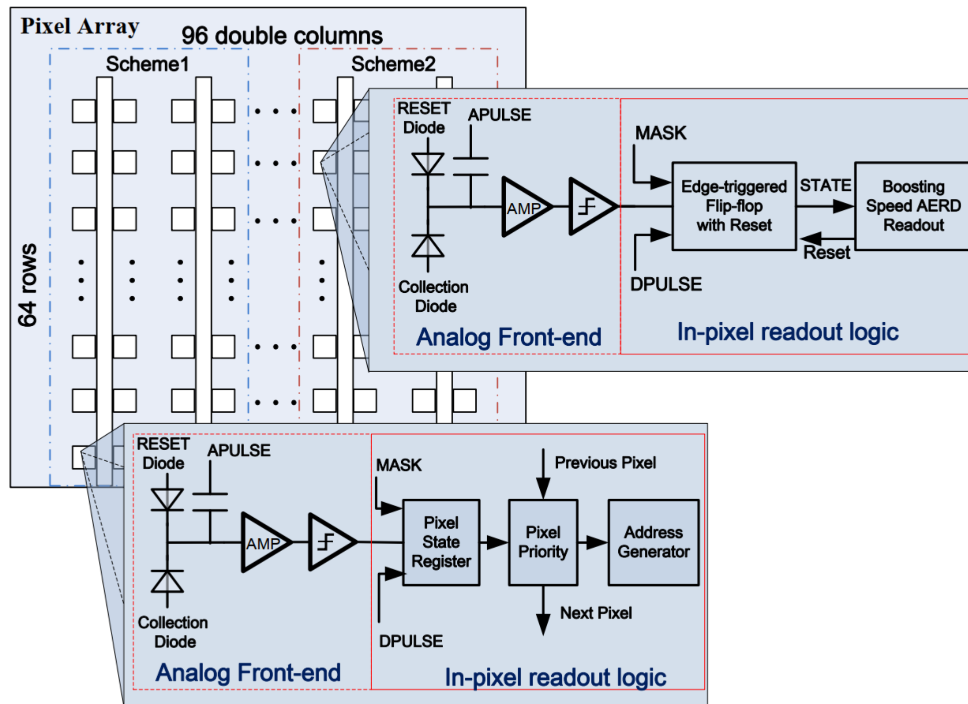


Figure 3.2 Two parallel in-matrix readout schemes, FE-I3 like scheme (scheme1) and ALPIDE like scheme (scheme2).

3.2.1 In-pixel analog front-end

The pixel cell, depicted in figure 3.3, contains a sensing diode, an analog front-end circuit, and in-matrix readout logic. The analog circuitry includes an amplifier and a discriminator. The capacitance of the input node integrates the signal charge, and the resulting voltage signal will be amplified and shaped by the front-end circuit. When the charge collected by the diode exceeds a certain programmable

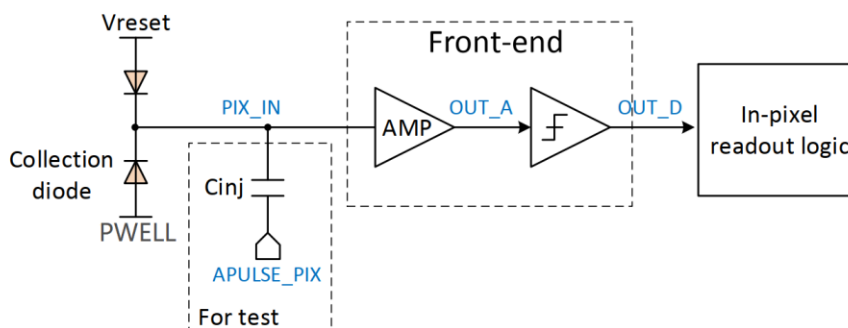


Figure 3.3 Block diagram of a pixel

threshold level, the output of the discriminator goes from low to high, indicating the detection of a hit. The analog front-end is based on the one on the ALPIDE chip [76].

Though the analog front-end of the TaichuPix1 is based on the ALPIDE chip, it features a short time walk, which is a critical modification, since the TaichuPix1 should be able to deal with the particle rate expected at CEPC and meet the bunch crossing period of 25 ns. Thereby the analog front-end electronics have been optimized for fast rising time and short duration time (<400 ns). However, meeting these timing requirements leads to an increase in power dissipation. The estimated power density of the analog front-end electronics is around 130 mW/cm^2, while this calculated value in MOST1 is only 18 mW/cm^2. In this prototype, a standard manufacturing process is used to prove the feasibility of the new architecture. A modification process to increase the depletion region and thus the better performance of the chip will be considered in the future prototype.

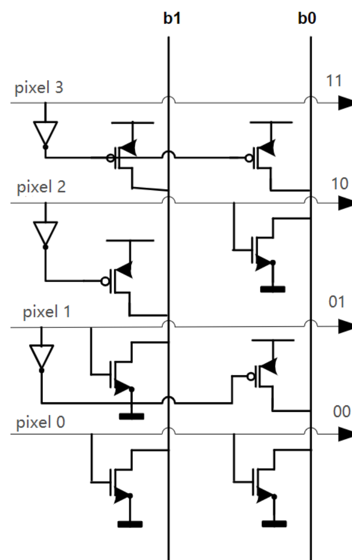


Figure 3.4 Address encoding arbiter architecture

3.2.2 In-matrix readout logic

As mentioned above, two new digital fast in-matrix readout logics have been designed: an FEI3-like scheme and ALPIDE-like scheme. In the first scheme, the in-matrix digital electronics follow the FEI3 design. However, the address ROM has been replaced by a pull-up and pull-down network matrix due to area limitations, as shown in figure 3.4. One pixel can be encoded at a time, and all the transistor states have to be consistent within a column. For instance, when *pixel3*

(see figure 3.4) gets a hit and goes to logic "1", the rest of the pixels must be at logic "0". Then the output of the *b1* column is pull up to logic "1", and all the transistors within column *b1* are set the bus to logic "1". In addition, the timestamp is not stored in-pixel but at the end of the column. Therefore, if two hits arrive in a short time in the same pixel, they will be merged as one. If the hits are in different pixels, they will be read out with the same timestamp. In the ALPIDE-like scheme, the in-pixel analog front-end is the same. In the TaichuPix1, a dynamic edge-triggered flip-flop has replaced the hit storage registers to prevent reading out one hit repeatedly before the analog front-end resets.

Moreover, the priority block AERD has been modified to boost its speed to 40 MHz with respect to [25] reference. There are two different methods to implement the AERD readout in [25]. One is the standard architecture to read out with the rising edge of the clock, and the other is the boosting speed one, where extra address enable signals are added to read out with both rising and falling edge. The latter one has been designed in the TaichuPix1, but the experimental results are not as good as expected. More details about the readout architecture can be found in chapter 5.

3.3 High data rate peripheral readout logic

The block diagram of the periphery readout electronics is shown in figure 3.5. All the double columns of the pixel array are read out in parallel. A timestamp is recorded at the end of the double-column (DCOL). In the trigger mode, when the chip receives a trigger, the data with a matched timestamp are buffered for output. In the triggerless mode, all the data are buffered and processed. This work proposes a new architecture for a fast readout of the 512 DCOLs, as shown in figure 3.5. The whole matrix has been divided into 4 blocks considering the system clock of 40 MHz and the average data frequency of 120 MHz. Each block contains a readout of 128 DCOLs. The column FIFO (FIFO1) depth should be enough to read out the data in trigger mode without any data loss. In this design, FIFO1 stores the data in 10 µs considering the maximal trigger latency of 6 µs. The FIFO2 is integrated into each block to match the system clock speed and the data output clock.

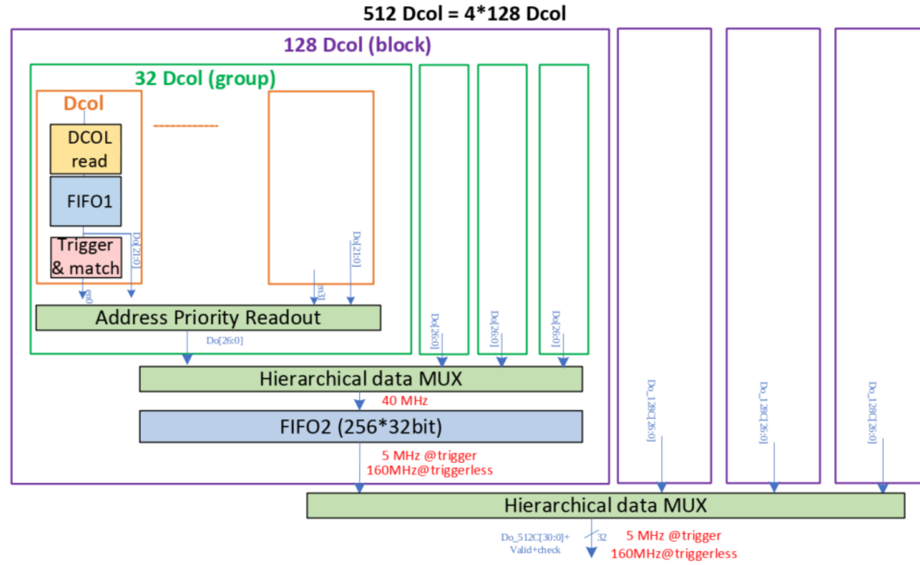


Figure 3.5 Block diagram of the readout architecture. Taken from [26].

The triggerless mode presents a challenge to the readout architecture design of the TaichuPix1. The amount of data that need to be read out in trigger mode are much less than those in the triggerless mode. In order to read out the data quickly and avoid unnecessary readout, a data-driven scheme is preferred at the bottom level of each group of 32 DCOLs. Only the nonempty FIFOs (FIFO1) are read out according to the address priority. For one of the groups with 32 DCOLs, the hit rate achieves 7.5 pixel/μs. A hierarchical data multiplexer with a special token control avoids blocked data by providing equal output opportunity among the read requests from the four groups of 32 DCOLs.

In order to verify the feasibility of the peripheral readout logic, the TaichuPix1 was implemented with three fast readout groups, and each group contains 32 DCOLs (every DCOL has 128 pixels). The TaichuPix1 includes a full architecture of the peripheral readout logic (see figure 3.5), DCOL reader, FIFO1, trigger and match logic, address priority readout, hierarchical data multiplex, dual-port SRAM, 32-bit shift register, and serial data transmission interface.

3.4 Physical implementation of the TaichuPix1

The TaichuPix1 was designed with a 0.18μm CMOS process, and it occupies a total area of 5×5 mm^2. A picture of the layout has shown in figure 3.6. The pixel array is placed at the top part of the chip, and the periphery is placed below the matrix. A summary of the main features has been given in table 3.1. More details

will be discussed in the next chapters.

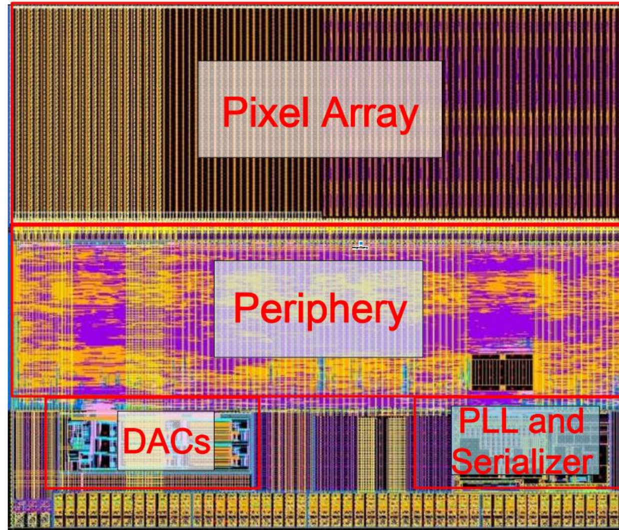


Figure 3.6 Layout of the TaichuPix1

Table 3.1 Main parameters of TaichuPix1

Parameters		TaichuPix1
CMOS technology		TowerJazz 180 nm
Chip size		5×5 mm^2
Pixel size		25×25 μm^2
Matrix array		192×64
Power density	Periphery Circuitry	Trigger mode: 25~30 mW/cm^2
		Triggerless mode: 80~140 mW/cm^2
	Analog front-end:	130 mW/cm^2
	In-pixel digital logic	scheme1[a]: 123 mW/cm^2
		scheme2[a]: 49 mW/cm^2

[a.] The chip is operating during the readout phase

Summary

A fully functional monolithic pixel sensor prototype has been presented in this chapter. The TaichuPix1 is a small-scale prototype close to the final chip for the vertex detector. This chapter introduced an in-pixel analog front-end circuit that has been optimized to have a fast peaking time and short time walk but at the expense of increasing the power consumption. In this prototype, two parallel in-matrix readout architectures based on ALPIDE and FEI3 were designed. Improvements were made to meet the requirements in terms of the critical requirements of area and speed. The timestamp is not designed into the pixel but at the end of the column to reduce the area. Periphery circuitry targets a fast-speed interface of the chip and the configuration. The digital readout periphery implemented is such that of the full data flow satisfies the data rate of 120 MHz/chip.

Chapter 4

Optimization of analog front-end

This chapter is focused on the optimization of the analog front-end to meet the 25 ns readout requirement. As was discussed before, the analog front-end of the TaichuPix1 is based on the ALPIDE chip, the main topic of this chapter is how to improve it to achieve a fast-rising edge and a short time walk. Section 4.1 discusses the design of the analog front-end within monolithic devices for high-energy physics. Section 4.2 presents the motivation on why designing a fast analog front-end is necessary. Section 4.3 describes the limitations of the existing front-end for the CEPC vertex detector. Section 4.4 presents a common front-end architecture introducing the function of the charge-sensitive amplifier and the timing effect from the shaper. The noise and time walk concepts are discussed in section 4.5. The simulation and characterization results of the TaichuPix1 analog front-end are shown in the last sections.

4.1 Analog front-end design within MAPS

There are several sensor options (see chapter 1) for the CEPC vertex detector. The MAPS is the most promising one due to its low material budget, low power consumption, fast readout speed, and low cost compared with the hybrid structure.

In the early 1990s, people first tried to process CMOS readout electronics on a completely depleted sensor substrate [32]. These sensors are made of high-resistivity p-type material with an n+ junction on the back. The signal charge is collected through the ohmic contact on the top. The PMOS transistor can amplify the signal, which is protected by the nwell. However, NMOS transistors cannot be used in the device's active area and can only be used for further signal processing and transmission in peripheral circuits. A prototype of this technology was successfully implemented with the beam test [80]. A different approach is to use technology based on optical CMOS sensors, such as digital cameras. As discussed in chapter 2, there are already MAPS for ionized particle detection implemented using this technology [81]. These devices are made in a p-type epitaxial layer on a low-resistivity p-type substrate using standard CMOS technology. The charge generated by the ionized particles in the nondepleted epitaxial layer is diffused and

collected in the n-doped gate. A circuit with three transistors is used for amplification and row/column selection for each pixel. These transistors are n-channel FETs embedded in a pwell. The doping of the pwell and the body is much higher than that of the epitaxial layer, which creates a barrier to prevent signal electrons from being lost in the body or the pwell.

Therefore, almost all electrons reach the nwell through diffusion to achieve charge collection. Collecting charges by diffusion causes a longer collection time (~100 ns), and the generated charge is spread over several pixels. The thin epitaxial layer (~ 10 μm) produces only a small signal. On the other hand, the inherent capacitance of these devices is very low, so they have an excellent signal-to-noise ratio (30:1) [82]. In sub-micron technology, the pixel size can be made as small as 10×10 μm^2 so that the position resolution can be very good. And this circuit only works during pixel readout, so the power consumption is also very small. Since only a thin epitaxial layer (<20 μm) is used for signal generation, the detector can be made very thin, and an ultra-thin device with minimal scattering can be constructed. But very thin devices, in which the effect of multiple scattering is reduced, can also suffer from low detection efficiency, a very critical parameter in HEP.

The disadvantage of early MAPS devices is that only NMOS transistors can be used in the active area, limiting the circuit complexity. Generally, only the simple three transistor circuits required for amplification and addressing are used in the active area. More complex signal processing requires the use of both NMOS and PMOS transistors to move to the non-sensitive periphery of the chip. For example, the ALPIDE chip (already discussed in chapter 2) is produced in a 180 nm CMOS technology of TowerJazz. It features a quadruple well structure that allows PMOS and NMOS devices within the pixel matrix. It could be improved by using a deep pwell, where the nwells of PMOS transistors could be shielded against the bulk and would not act as parasitic collection anodes.

4.2 Motivation of a fast analog front-end

As described in chapter 2, silicon sensors usually use PN junction diodes depleted by applying a reverse voltage. A large electric field is established in the depletion region in the reverse bias diode with a small thermal current. Photons and ionized particles produce electron-hole pairs in the depleted region of the diode. These charge carriers drift to the electrode, where they generate the signal. The position

information can be obtained by segmenting the electrode in many independent diodes. The position of ionized particles can be inferred from the known position of the electrode of the induced signal. Ideally, the signal is only proportional to the amount of charge collected on the readout electrode. In fact, according to Ramo's theorem [55], the current can be measured before the first charge carrier reaches the electrode. In most detectors, the integration time of readout electronics is much longer than the typical charge collection time. However, collection time becomes important when targeting fast electronic devices, especially in partially depleted sensors, or if trapping [78] occurs. The CEPC vertex detector aims to achieve excellent impact parameter resolution and meet the 25 ns bunching crossing. Thus, a fast-analog front end is critical to fulfill these requirements.

4.3 Limitations of the existing front-end for the CEPC

MAPS has matured enough to be used in high-energy physics experiments as high precision tracking and vertexing devices. In terms of the readout speed and precision spatial resolution, none of the existing pixel sensors can fully satisfy the requirement for the CEPC vertex detector. Besides of the MAPS prototype ALPIDE chip, this section introduces the MAPS used for the STAR experiment at RHIC (Brookhaven National Laboratory-BNL).

The PiXeL detector (PXL) for the STAR experiment at RHIC completed its three-year physics program in July 2016. Added to the STAR apparatus in 2014 as part of the Heavy Flavor Tracker (HFT) upgrade [83], the PXL detector is the first application of state-of-the-art thin MAPS technology in a collider environment. As a result of the low material budget and the excellent position resolution, the PXL detector provided the track pointing resolution needed by STAR to perform a direct topological reconstruction of short-lived charm hadron decays in the heavy-ion collision environment and access the heavy flavor domain [84]. In the PXL detector, the sensors used are designed with a 20.7 μm pixel pitch in a 928×960 pixel arrays and have been fabricated in the 0.35 μm CMOS process. These sensors include on-chip correlated double sampling, column-level discriminators, and a zero-suppression system that passes hit pixel addresses. And these addresses are read out through two Low-Voltage Differential Signal (LVDS) outputs per sensor with a clock speed of 160 MHz, and the integration time is 185.6 μs. In terms of the pixel size, it meets the requirement of the CEPC vertex detector, but the readout speed is not adequate. In contrast, the readout speed for the CEPC should be better

than 10 μs to minimize event accumulation from consecutive bunch crossings.

In short, both MAPS implemented in STAR or ALICE experiments (ALPIDE chip that discussed in chapter 2) do not fully satisfy the CEPC vertex detector requirement because the analog front-end is not fast enough.

4.4 Common front-end electronics architecture

A charge-sensitive amplifier (CSA), followed by a shaper, is the most commonly used structure in the analog part of the ASICs used in HEP since the charge is a basic signal generated from the silicon sensor. This is shown on figure 4.1, where I_s is the signal current, *Cd* is the sensor capacitance, C_f is the feedback capacitance, and "RESET" stands for a reset circuit to restore the baseline. The shaper is simply a CR-RC structure, where CR means the differentiation circuit and the RC represents the integration circuit.

A charge Q_{in} is released into the sensor capacitance C_d, which causes a voltage step at the amplifier input node. This voltage step is amplified until it is compensated by the feedback capacitor C_f. With an amplifier gain of

$$dV_{out}/dV_{in} = -a \tag{4.1}$$

the output voltage corresponding to an input charge Q_{in} is

$$A_q = dV_{out}/dQ_{in} = -\frac{1}{C_f+\frac{C_f+C_d}{a}} \approx \frac{1}{C_f}(where\ a \gg 1) \tag{4.2}$$

The charge Q_d which is remaining on the sensor can be given by

$$\frac{Q_d}{Q_{in}} = \frac{C_d}{C_d+C_f(1+A)} \tag{4.3}$$

The sensor capacitance should be small compared to $C_f(1+A)$ to obtain the

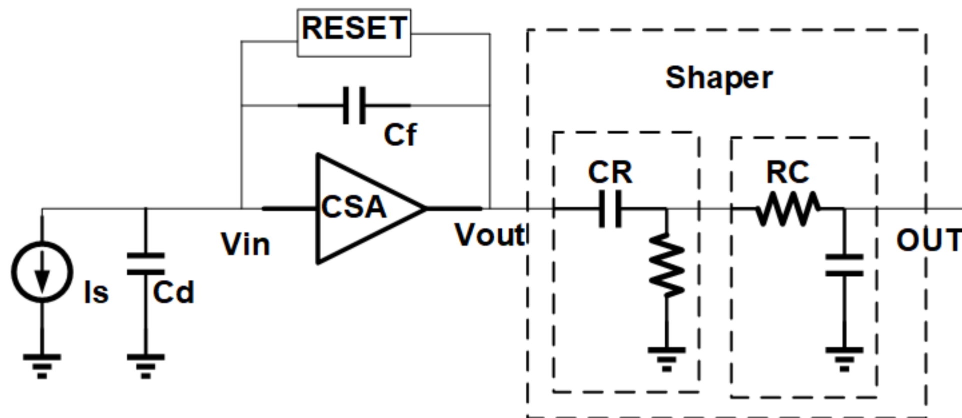


Figure 4.1 Common front-end electronics architecture

highest efficiency. Such an amplifier alone would have a step response. In order to

deliver pulses with a pulse height proportional to Q_{in}, the CSA is usually followed by a shaper, which converts the step function into a shaped pulse with a characteristic time τ. The waveform shape and time of the shaper have some impact on the noise performance of a detector system. But it affects the signal amplitude as well. According to the Fourier transform, the time domain of the shaper output V_o should be the convolution:

$$V_0(t)=V_i(t) * g_{int}(t) * g_{diff}(t) \tag{4.4}$$

Where $g_{int}(t)$ and $g_{diff}(t)$ are the functions of the integrator and the differentiator. When the input signal is a unit step, then the pulse shape is given by

$$V_0(t)=\frac{\tau_{\text{diff}}}{\tau_{\text{diff}}-\tau_{int}}\left[e^{-t/\tau_{\text{diff}}}-e^{-t/\tau_{int}}\right] \tag{4.5}$$

Where the τ_{diff} is the time constants of the differentiator and τ_{int} is of the integrator.

Figure 4.2 shows the shaper response with different CR and RC time combinations (when the CR time τ_{diff} fix to 100 ns, and adjust the RC time τ_{int} from 10 ns to 100 ns). It can be concluded that the peaking time of pulse will be extended with a longer τ_{int} and the difference in amplitude can be observed. In order to restore the baseline of the CSA, a reset circuit must be used, which discharges the CSA after some time which should be longer than the shaping time. This can be realized using a resistor, a constant current source, or a switch.

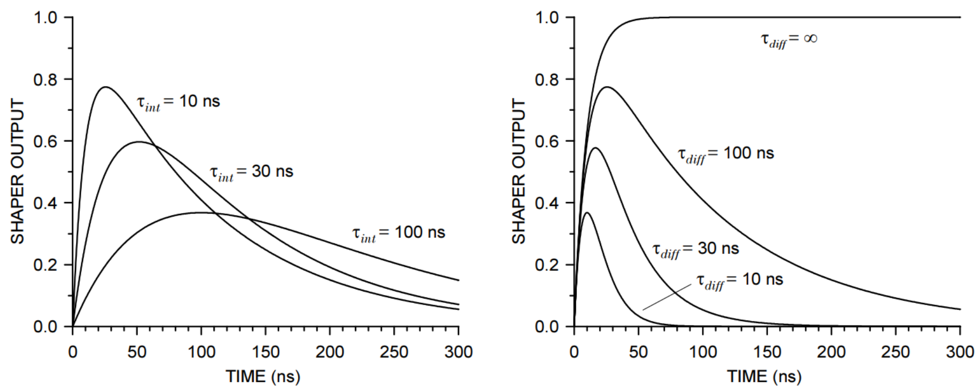


Figure 4.2 Pulse amplitude vs. integrator time constants (RC time τ_{int}) for a fixed differentiator time constants of 100 ns (left) and vs. differentiator time constants (CR time τ_{diff}) for a fixed integrator time of 10 ns (right). Taken from [79].

4.5 Noise and time walk

4.5.1 Noise analysis

The input noise current spectral density i_n and input noise voltage e_n are two basic noise mechanisms that determine the equivalent noise charge (ENC). For both time-invariant and time-variant shapers, the ENC is given by [79]

$$Q_n^2 = i_\mathrm{n}^2 F_i Ts + e_\mathrm{n}^2 F_v \frac{C^2}{Ts} + F_{vf} A_f C^2 \quad (4.6)$$

where C is the sum of all capacitances shunting the input. F_i, F_v, and F_{vf} are determined by the frequency or time response of the shaper and T_S is a characteristic time, the shape factors Fi, Fv are calculated by

$$Fi = \frac{1}{2Ts}\int_{-\infty}^{\infty}[W(t)]^2 dt\,,\ Fv = \frac{Ts}{2}\int_{-\infty}^{\infty}\left[\frac{dW(t)}{dt}\right]^2 dt. \quad (4.7)$$

Where $W(t)$ is simply the system's impulse response with the peak output signal normalized to unity for time-invariant pulse shaping. For a time-variant shaper, the same equations apply, but the shape factors are determined differently. Figure 4.3 illustrates the dependence of ENC on basic noise parameters. At short shaping times (large bandwidth), the ENC is dominated by voltage noise, whereas at long shaping times (large integration time), the current noise contributions dominate. The total noise assumes a minimum where the current and voltage

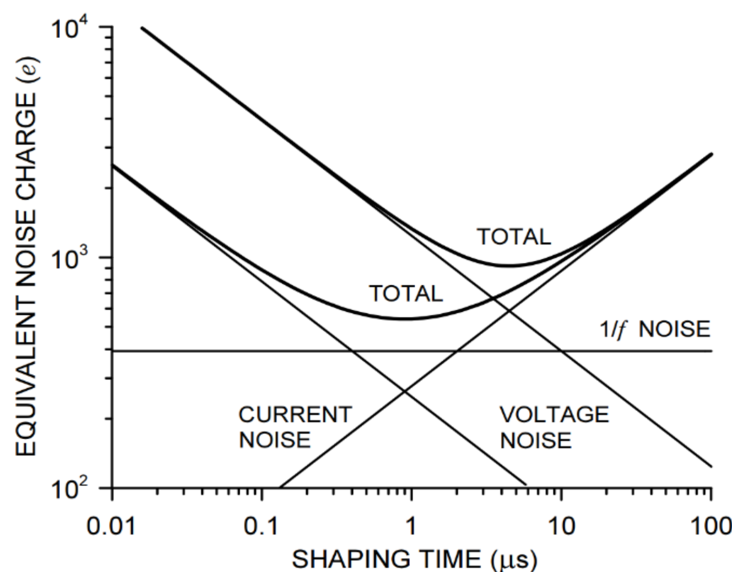


Figure 4.3 ENC *vs*. shaping time. Taken from [79].

contributions are equal. The "1/*f*" noise contribution (see figure 4.3) is independent of shaping time and flattens the minimum noise. The "1/*f*" noise is increasing the voltage or current noise contribution.

Many systems only need to detect the passage of particles. This is done by checking if the integrated charge exceeds a given threshold level with a discriminator. Noise affects the resolution of amplitude measurements and also determines the minimum detectable signal threshold. Figure 4.4 shows a system that only records the detection of a signal if the integrated charge exceeds a fixed threshold. Since this amplitude evaluation yields only a yes/no result, it is frequently called a binary readout. The threshold has to be set low enough to capture most of the signal but must be high enough to reduce the noise rate to an acceptable level. The noise rate is invariably much higher than the signal rate. Figure 4.5(a) illustrates the noise pulses would exceed an amplitude threshold with a rate dependent on the threshold setting. Typically, the threshold is set at the beginning of signal pulses, but as shown in figure 4.5 (b), a noticeable rate of noise pulses usually exceeds the threshold.

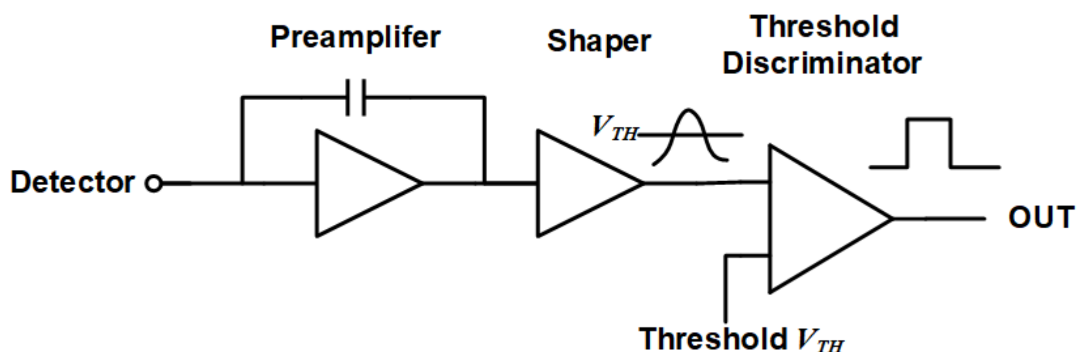


Figure 4.4 A threshold discriminator diagram

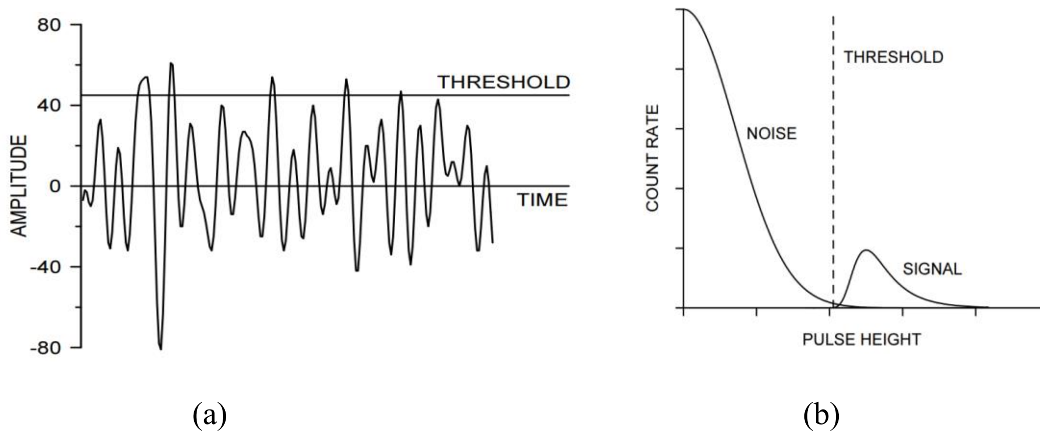


Figure 4.5 Threshold setting to the noise pulse (a) and the count rate vs. pulse height (b). Taken from [79].

4.5.2 Time walk

Timing measurements seek to optimize the determination of the time at which a particle enters the detector. This time largely corresponds to the time in which the integrated charge exceeds the threshold level. Although, as in amplitude measurements, the signal-to-noise ratio is important, the determining parameter is not signal-to-noise but the slope-to-noise ratio. This is illustrated in figure 4.6, which shows the leading edge of a pulse fed into a threshold discriminator

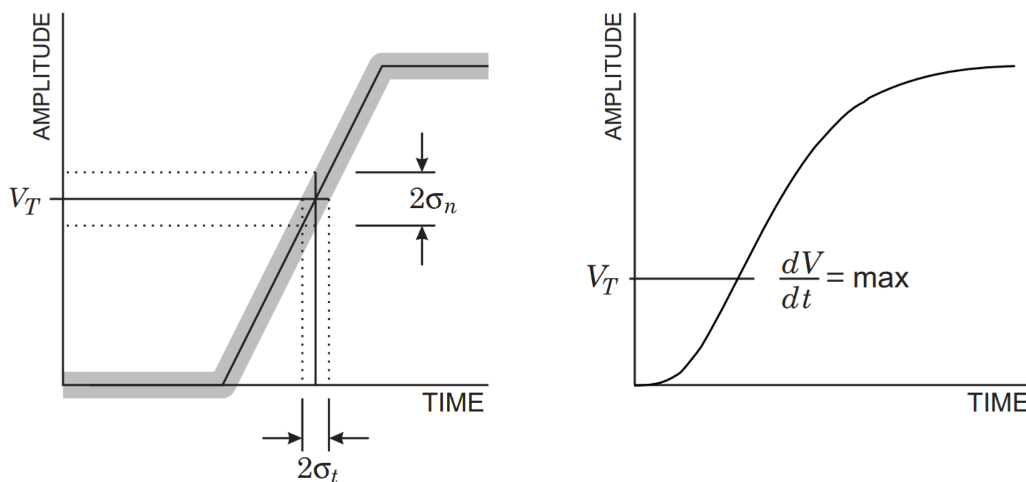


Figure 4.6 Fluctuations in signal amplitude crossing a threshold vs. timing fluctuations (left), the slope changes with amplitude in realistic pulses (right). Taken from [79].

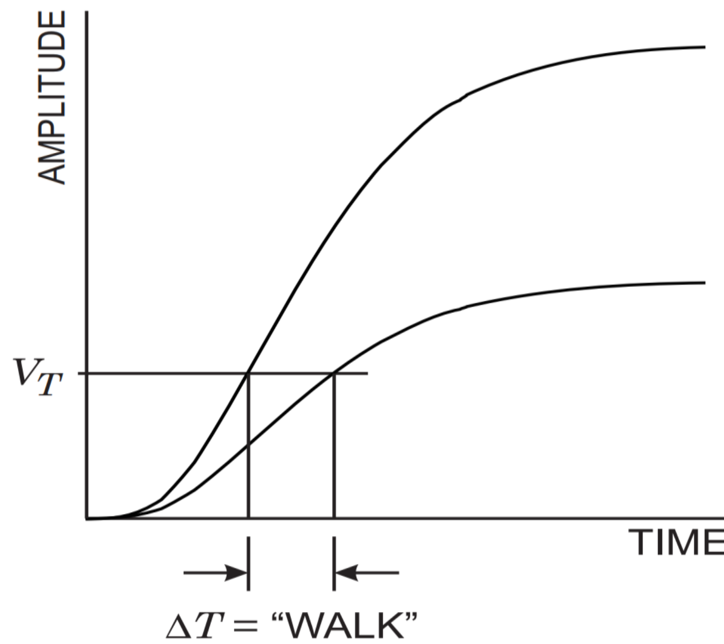


Figure 4.7 Time walk definition. Taken from [79].

(comparator), a "leading edge trigger." The instantaneous signal level is modulated by the noise, where the shaded band indicates the variations. Because of these fluctuations, the time of threshold crossing fluctuates. By simple geometrical projection, the timing variance, or "jitter," is

$$\sigma_t = \frac{\sigma_n}{\left.\frac{dV}{dt}\right|_{V_T}} \approx \frac{t_r}{S/N} \tag{4.8}$$

where σ_n is the RMS noise, and the derivative of the signal *dV/dt* is evaluated at the threshold level V_T, and t_r is the rise time of the pulse. In general, the leading edge is not linear, so the optimum trigger level is the maximum slope point, as shown on the right side of figure 4.6.

In addition to the time "jitter," the time at which the signal crosses a fixed threshold depends on pulse amplitude. The moment that the signal crosses the threshold level depends on its amplitude, so variations in signal amplitude will broaden the timing distribution. This phenomenon is called "time walk" and is illustrated in figure 4.7. As a result, the timing measurement accuracy is limited by the combination of jitter (due to the noise) and time walk (due to the amplitude variations). When the rise time is known, "time walk" can be compensated in software for each particle or event, by measuring the pulse height and then correcting the time measurement. But this technique will fail if both amplitude and rise time are not well correlated. In semiconductor sensors, the rise time combines both electron and hole components, so the slope has two components. Time walk

can be reduced in the front-end circuit by setting the threshold to the lowest practical level or using compensating circuitry to equilibrate the amplitude. All particles traverse the sensor in charged particle tracking detectors, so the relative contribution of electrons and holes is always the same, so rise-time compensation is unnecessary. Minimum ionizing particles deposit the same average energy in the sensor, but the amplitude distribution is rather broad, so time walk is an issue. In order to operate with a 40 MHz bunching crossing as needed in the CEPC vertex detector, the time walk should be taken into consideration to achieve a fast timing system that can meet the ultimate requirement that can satisfy the 25 ns bunching crossing.

4.6 Design of the analog front end in TaichuPix1

The analog front-end of TaichuPix is based on the one used in ALPIDE [76] but the requirements in terms of the interaction rate are different, from 0.1 MHz to 40 MHz. Thus, it was necessary to redimension the size of the transistors. Figure 4.8 shows a schematic of the analog front-end electronics at the transistor level. It is a compact structure of only 11 transistors that includes a preamplifier and discriminator. It was conceived for minimizing the total area, so the discriminator is very simple with the possibility of setting the threshold level externally through the ITHR but with no room to design individual in-pixel DAC to compensate the offset of the discriminator due to process variations from pixel to pixel. M1 operates as a source follower to avoid loading the input. M2 is a cascode transistor to increase the gain on the output node and eliminate the Miller effect for the input node. The analog output node is stabilized at low frequency by active feedback on the transistor M3. The bias VCASN and ITHR are used to define the baseline value

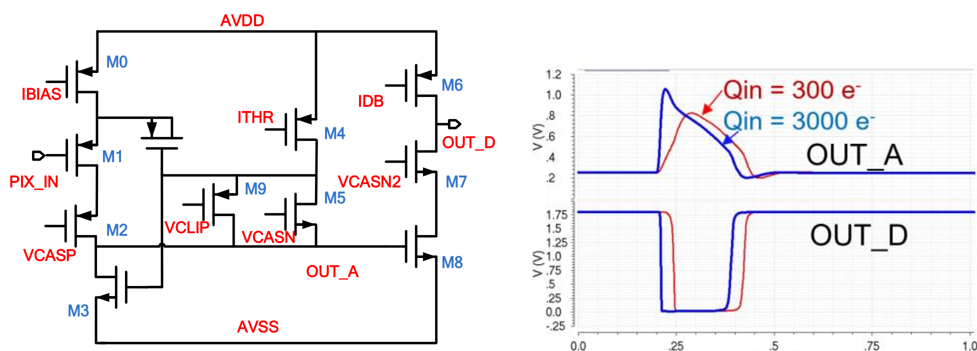


Figure 4.8 Schematic of the front-end (left side) and the post layout simulation output of OUT_A and OUT_D (right side).

of OUT_A. They also determine the return to baseline after a particle hit. OUT_A controls the second stage input transistor M8, and the baseline is determined when $I_{M8} < IDB$. The baseline of OUT_A to where $I_{M8} = IDB$ defines the charge threshold. If OUT_A voltage level is higher than the threshold where $I_{M8} > IDB$, the discrimination output on OUT_D is generated. VCLIP is a clipping mechanism implemented to limit the pulse duration for large input signals.

As described in chapter 2, based on the same analog front-end structure illustrated in figure 4.8, the peaking time of the ALPIDE front-end is around 2 μs, the equivalent noise charge is 3.9 e^-, and the minimum threshold is lower than 100 e^-. The time walk is at a level of several hundred nanoseconds. In order to reduce the rising time of the analog front-end, further optimization has been carried out in the TaichuPix1. As mentioned before, time walk is mainly caused by amplitude variations. Increasing the magnification of the preamplifier can shorten the arrival time at the threshold, and the peaking time will be reduced as well. The analog front-end principle based on ALPIDE indicates that more charges lead to a higher amplitude, as the simulation waveforms are shown at the top of figure 4.9. The height of the signal determines the rising time, and the higher amplitude brings a faster-rising edge. An OUT_A simulated comparison between ALPIDE and

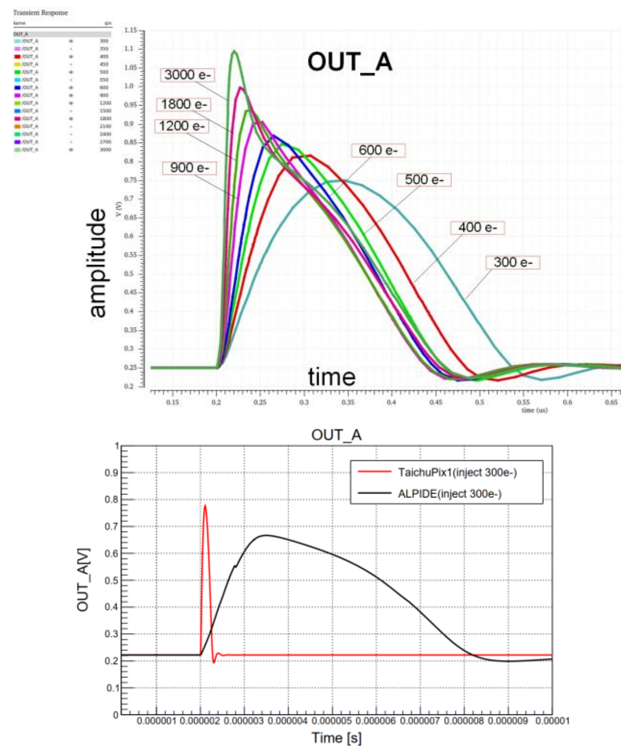


Figure 4.9 OUT_A amplitude simulation with different injected charge(top), simulation difference between ALPIDE and TaichuPix1 with injecting charge of 300 e^- (bottom).

TaichuPix1 is drawn at the bottom of figure 4.9. It is apparent that the peaking time of TaichuPix1 is much faster than the ALPIDE parameters published on [76].

Apart from the gain of the preamplifier, the threshold will also affect the performance of the time walk since a smaller signal leads to a slow rising edge that will broaden the time walk. Noise is another limitation, and it affects the resolution of amplitude measurements and determines the minimum detectable signal threshold as discussed above. To design low noise and a faster-rising edge with a short time walk, a trade-off was taken into consideration.

In order to determine the threshold of a single-pixel with a certain setting, a constant charge is injected N_{inj} times to the diode capacitance C_d (typical 2.5 fF) and then read it out from the OUT_D, to record the number of states flips from "1" to "0". This is repeated with different injected charges. The resulting function would be a step function at the threshold voltage V_{th} in the absence of noise. However, the noise is inevitable (in the simulation the internal noise σ_{noise} was assumed), so the expected number of responses (N_{resp}) follows a convolution of a step function and a Gaussian distribution, which is called an S-curve:

$$N_{resp} = \frac{N_{inj}}{2}\,\mathrm{Erfc}\left(\frac{\mathrm{Vth-V}}{\sqrt{2}\,\sigma_{noise}}\right) \tag{4.9}$$

where Erfc(x) is the complementary error function:

$$\mathrm{Erfc}(x) = \frac{2}{\pi}\int_{\pi}^{\infty} e^{-t^2}\,dt \tag{4.10}$$

Fitting this function to the responses of a single pixel allows the determination of the threshold V_{th}. In this simulation, different constant charges have been injected into the chip 50 times. Then the threshold is the value where the probability of a detected hit is 50%. As illustrated in figure 4.10. The threshold to the analog front-end is about 181.1 e^- with the ENC of 7.1e^- with the typical corner. The threshold dispersion is around 4.4 e^- given by the Monte Carlo simulation. Considering different potential collection diode capacitances, more conditions are evaluated. When C_d is set to 1.5 fF, the threshold is about 140.6 e^- with a dispersion of 3.3 e^-, while the 3.5 fF C_d would obtain a 224.1 e^- threshold corresponding to a 5.5 e^- dispersion. This result indicates that the threshold of the analog front-end will also depend on the value of the C_d capacitance.

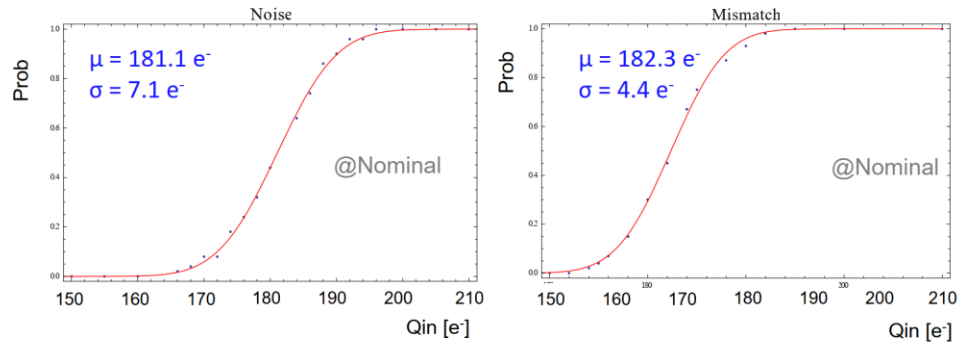


Figure 4.10 S-curve simulation and mismatch of analog front-end.

The analog front-end circuit in each pixel shares bias voltage and current with common DACs due to the consideration of area and power. The signal charge is integrated into the capacitance of the input node, and the resulting voltage signal will be amplified and shaped by the front-end circuit. When the charge collected by the diode exceeds a certain threshold, the front-end stage (OUT_D) outputs a logical '0'. Then the digitalized hit signal "OUT_D" is processed by the in-matrix readout logic. The right of figure 4.8 shows the simulated waveforms of the amplifier output (OUT_A) and discriminator output (OUT_D) corresponding to injected charges of 300 e^- and 3000 e^-, respectively. A Monte Carlo mismatch simulation analysis is shown in figure 4.11, the time walk is at the range of 32.4 ns ±1.1 ns.

The TaichuPix1 should be able to deal with the particle rate expected at CEPC and meet the bunch crossing operation of 25 ns. To this end, the analog front-end

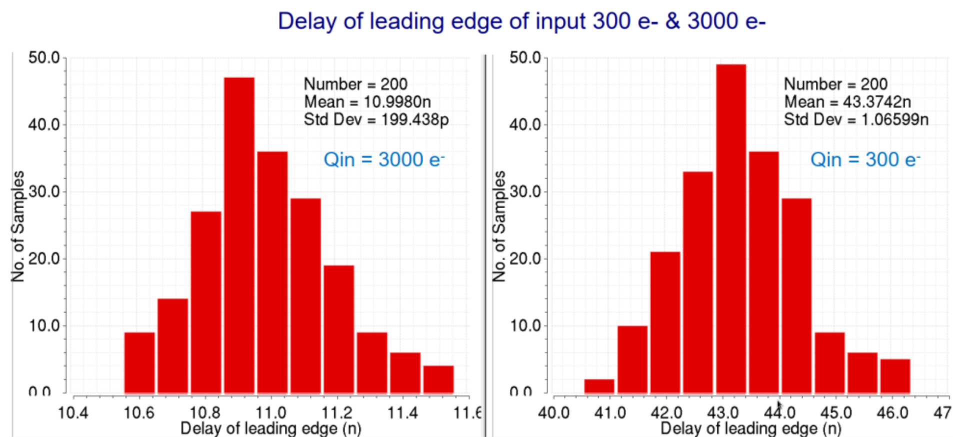


Figure 4.11 The Monte Carlo analysis of the leading-edge delay at 300 e^- and 3000e^-. The estimated input capacitance is 2.5 fF and the threshold is about180 e^-.

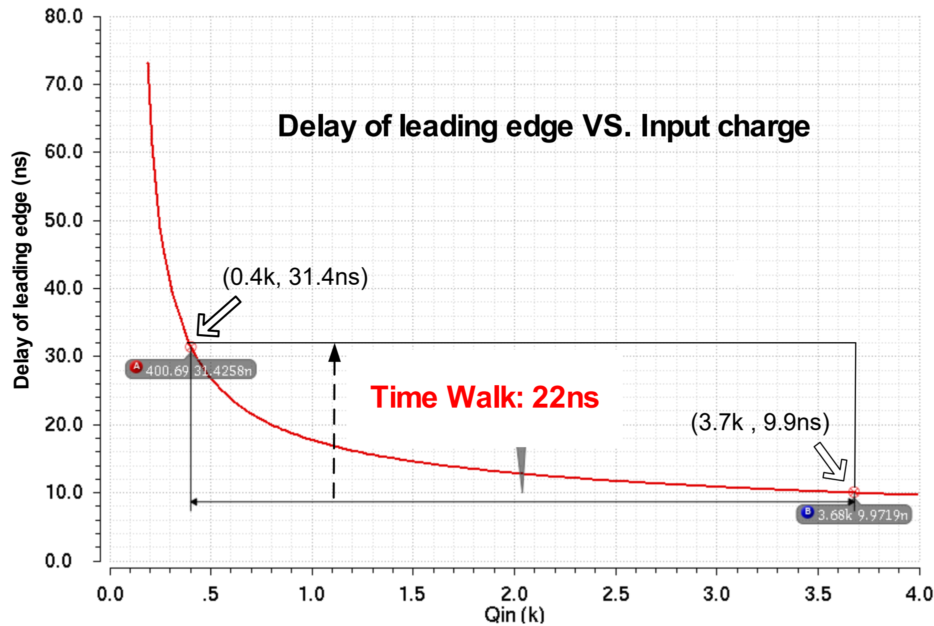


Figure 4.12 Simulated rising time of the in-pixel analog front-end as a function of the input charge. The estimated input capacitance is 2.5 fF and the threshold is 180 e^-.

electronics have been optimized for a fast-rising time and a short time walk. Figure 4.12 shows the simulated delay of the leading edge of the discriminator for an input charge varying from 400 e^- to 4000 e^-. The response for the stimulus of 3700 e^- is around 9.9 ns, and 31.4 ns for 400 e^-, so that the simulated time-walk of the analog front-end is about 21.5 ns at the injected charge range of 400 e^- to 4000 e^-.

However, meeting these requirements leads to an increase in power dissipation. The power density of the analog front-end evaluation of the TaichuPix1 is illustrated in figure 4.13. As already mentioned, the analog front-end power density of MIC4 [85] is less than 18 mW/cm^2, corresponding to a peaking time of 1 μs. The TaichuPix1 is designed with the same principle of the analog front-end but has been optimized to a faster-rising edge with a short time walk. It is then expected that the power density would increase rapidly. Figure 4.13 shows that a shorter time walk will bring a higher power dissipation. The simulation shows that indeed the power density is around 138 mW/cm^2, with the IBIAS setting to 440 nA. In principle, the power consumption and time walk can be adjusted by tuning the value of IBIAS from the on-chip DACs.

4.7 Characterization of the analog front-end of the TaichuPix1

The analog front end is calibrated by injecting various amounts of charges with an

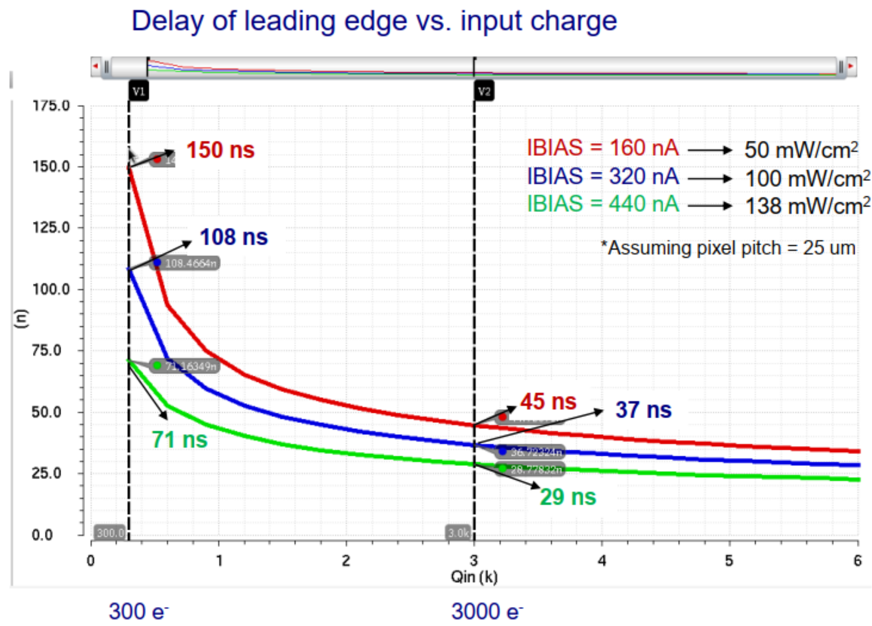


Figure 4.13 Power consumption of the analog front-end with different time walk.

impulse response switch circuit. As discussed, the analog front-end has capacitance and a test pin APULSE designed for analog circuit calibration. Figure 4.14 shows the schematic of the impulse response switch circuit and the simulated waveforms from the analog front-end. V_HIGH and V_LOW are constant voltage signals supplied by an external DAC, and APULSE_EN/ENB is enabled by an enable signal PULSE_EN (shown in figure 7.2). The value of APULSE_PIX (see figure 3.3) depends on the difference between V_HIGH and V_LOW. At the same time, the amplitude of the OUT_A is also related to the voltage difference of APULSE_PIX.

The testing platform, used for the measurements, will be discussed in detail in chapter 7. The pixels in the last row (ROW<64> at the bottom of the column) are dummy pixels, including only pixel analog circuits without pixel digital logic. This is used to separate the periphery circuitry and decrease the edge effect on the chip. So as to monitor the analog signal of the front-end, the node OUT_A of several pixels in the ROW<63> is connected to the on-chip analog readout buffer of the chip. These pixel analog outputs are selected one by one, controlled by the registers in the periphery readout.

Table 4.1 Bias settings by the DACs.

Bias	IBIAS	ITHR	IDB	VCLIP	VCASP	VCASN	VCASN2	VRESET
Design value	440 nA	4.5 nA	1 µA	0.2 V	0.6 V	0.55 V	0.5 V	1.4 V
Settings-1	440 nA	4.5 nA	1 µA	0.043 V	0.6 V	0.55 V	0.5 V	1.71 V
Settings-2	472 nA	1.77 nA	0.7 µA	0.048 V	0.65 V	0.44 V	0.68 V	1.6 V
Settings-3	472 nA	4.01 nA	0.7 µA	0.048 V	0.65 V	0.44 V	0.68 V	1.6 V

As already mentioned, the parameters of the analog front-end are tuned by the on-pixel DACs, which are used to adjust the bias voltage and current. However, the band-gap designed for the DACs cannot achieve the setting value, which leads to the ITHR not being set to a correct value, and then the range of IBIAS cannot reach the expected value. The strength of the bias output from the DACs is not adequate to drive the analog front-end. Thus, the band-gap is bypassed, and an external power supply sets the reference bias to the DACs. Table 4.1 list the values of the settings. When the bias settings are the same as the design value (Settings-1), the VRESET (see figure 2.8), which is used to reset the collection diode, should be set up to 1.71 V, this would increase the baseline voltage of the OUT_A and lower the amplitude of the response signal. In order to operate the analog front-end at an appropriate point, all the parameters are set to the Settings-2 values, shown in table 4.1. The following experimental results are based on this setting.

The PWELL is connected to the 0 V for this electronic test, and the external bias circuit is used to provide the reference bias for the DACs. Figure 4.15 demonstrates the experimental results of OUT_A waveforms from the oscilloscope with different injected charges. The oscilloscope is set with display persistence. The ΔV can be obtained by:

$$\Delta V = V_HIGH - V_LOW \tag{4.11}$$

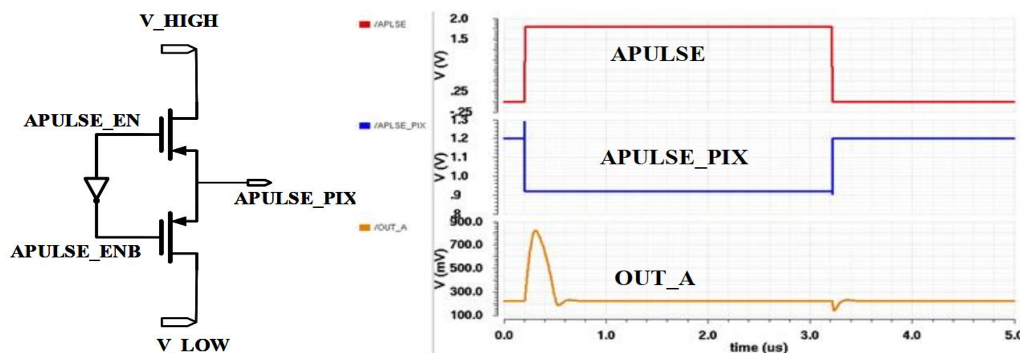


Figure 4.14 APULSE switch circuit (left) and simulation waveforms (right).

For a better view of waveforms, figure 4.16 illustrates the smooth curves of experimental results of OUT_A using ROOT [79]. With the parameters of Settings-2(see figure 4.16(a)), when ΔV is set to 800 mV, the amplitude of OUT_A read from the oscilloscope is about 410 mV and the peaking time is around 160 ns. When it is set to 100 mV, the amplitude is around 97 mV and the peaking time is around 150 ns. And the DC baseline with this setting is around 900 mV and the peaking time is less than 400 ns. The only difference of Settings-3 is the value of ITHR, which is apparent from the waveforms. The OUT_A response signal shows a higher threshold which is illustrated in figure 4.16 (b). In order to obtain the same amplitude, Settings-3 has to inject more voltages into the chip. The pixel front-end transient waveforms indicate that the analog front end can respond to different amounts of charges, and more charges lead to a faster-rising edge. When the injected charges are saturated, the change of signal is very small.

4.8 Noise performance of TaichuPix1

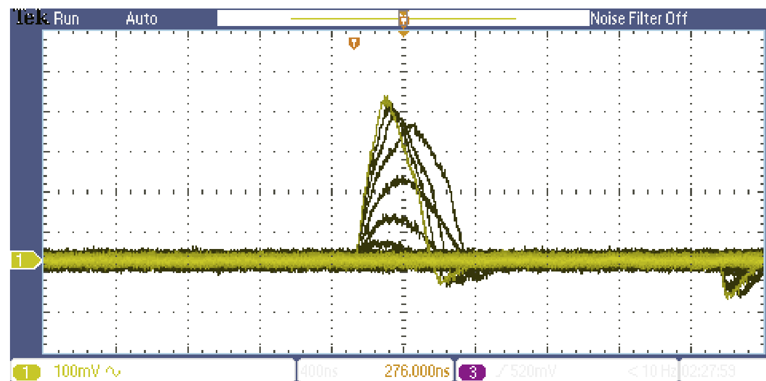
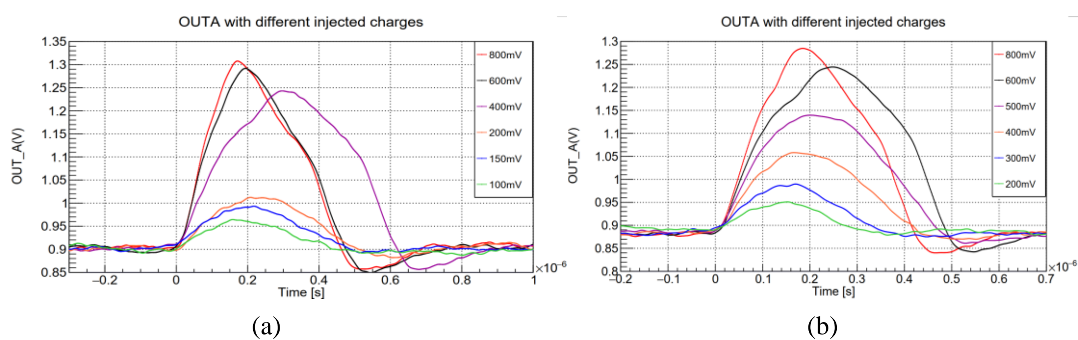


Figure 4.15 Initial waveforms of OUT_A measured by the oscilloscope in persistence display mode with different injected voltage.



(a) (b)

Figure 4.16 Plots of OUT_A smoothed by the ROOT from oscilloscope data under different injected charges with Settings-2(a) and Settings-3 (b) in table 4.1.

As mentioned before, the ENC is used to characterize the noise performance of the

chip. It usually includes the Temporal Noise (TN) and the Fixed Pattern Noise (FPN). The TN is used for electrical noise, and the FPN shows the threshold dispersion of the matrix.

As shown in chapter 3, an APULSE test pin and an injection capacitor are implemented in each pixel, which could be used to measure the analog front-end performance with different charges. To determine the threshold of a single-pixel with the Settings-2 in table 4.1, one ΔV is injected 100 times to the calibration capacitance and then read out from the FIFO_chip (FIFO2). This is repeated with different injected ΔV. The resulting function would be a step function at the threshold voltage V_{th} in the absence of noise. However, since the discriminator has internal noise, the expected number of responses follows equation 4.9. The threshold is defined at the value where a pixel responds 50 times to the injected voltage. The noise (σ_{noise}) TN can be extracted from the fit, this is shown in figure 4.17. The figure shows that for pixel (DBCOL 31, ROW 12), the threshold is around 225.2 mV, and the TN is about 10.31 mV. One has to mention that the threshold is determined in terms of the injection voltage ΔV, which has to be calibrated with a reference charge. The charge to voltage factor (C_{factor}) from the simulation is around 0.88 mV/e$^-$.Then the number of charges (Q_{in}) could be converted by:

$$Q_{in} = \frac{\text{V_HIGH} - \text{V_LOW}}{C_{factor}} = \frac{\Delta V}{0.88mV/e^-} \tag{4.12}$$

Where the threshold and TN in figure 4.17 are 255.91 e$^-$ and 11.72 e$^-$, respectively.

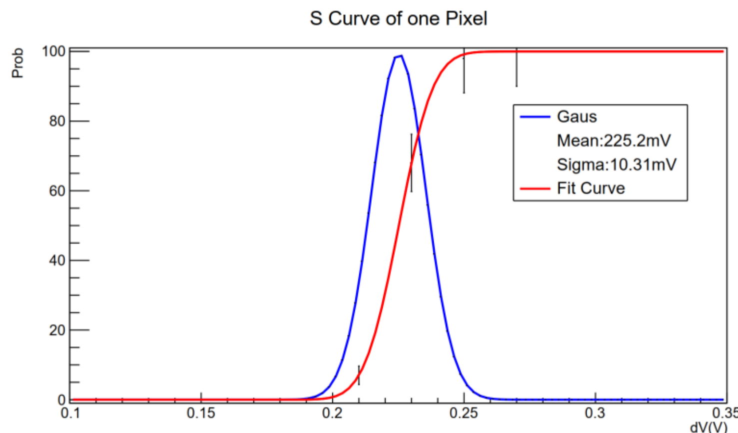


Figure 4.17 S-curve of one single pixel(Double column 31,row 12).

Besides, the threshold dispersion and noise distribution can be determined by the S-curve scan of the matrix. With the same threshold settings as used above, figure 4.18 shows the FPN of the FEI3-like matrix. There are two different sensor geometries designed for the FEI3-like pixels, the left half of the matrix is sector 1 (columns 0 to 47), and the right half is sector 2 (columns 48 to 95). As shown in figure 2.8, the spacing of sector 1 is 3 μm while for sector 2 is 2 μm. The threshold dispersion is shown on the left side of figure 4.18, and the right side is the noise distribution. The charge was injected by the step voltage through the C_{inj} in each pixel in the noise measurement. Therefore, the noise value obtained in such a way is indeed is the sum of both the fluctuations on the injected signal and the fluctuations on the threshold. The pixels of sector 2 behave better in terms of threshold and noise. The average threshold for sector 1 is around 304.6 mV while the value for sector 2 is about 268.4 mV, and the FPN for them is 30.57 mV and 24.4 mV, respectively, while the average TN is 13.5 mV and 9.8 mV, respectively. Since the global threshold of the pixel array is adjusted by the same DACs, there

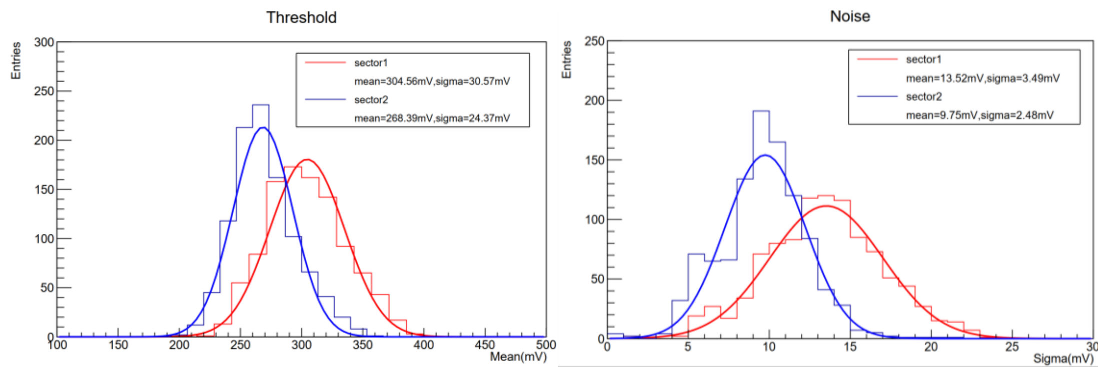
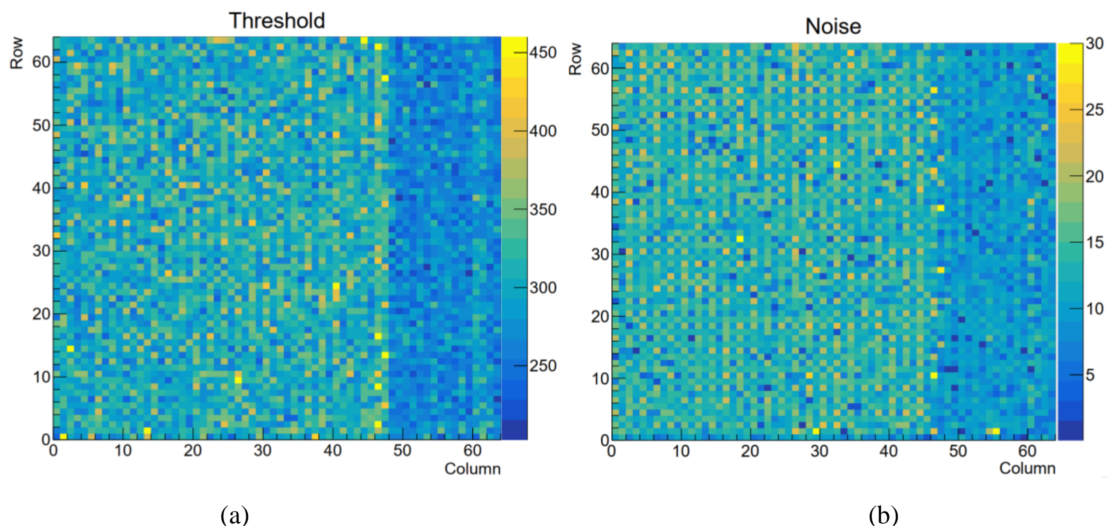


Figure 4.18 Threshold distribution and noise distribution of 16 columns.



(a) (b)

Figure 4.19 Threshold(a) and noise (b) value of each pixel of 64 columns.

is no way to optimize the dispersion by tuning each pixel. Figure 4.19 plots the threshold and noise of each pixel. Both maps show a uniform distribution. The boundary is between the 2 μm and 3 μm spacing, which may relate to the different input capacitances.

Compared to the simulation, the threshold of the measurement is much higher. In the measurement, the PWELL connects to 0 V, however, it should connect to -6V. In principle, applying a -6 V bias on the chip substrate decreases the sensor capacitance, leading to a lower threshold. However, it was observed that applying a reverse bias will sometimes damage the chip through a process that is not fully understood. Therefore, zero bias voltage is used to measure the threshold and noise. From the results of [87], the input capacitance C_d will be around 5 fF, at PWELL on 0 V bias and 2.5 fF at -6 V. As already discussed, the threshold will be higher when C_d increases.

The time walk measurement method of the analog preamplifier is shown in figure 4.20. As mentioned, different injected voltages to C_{inj} (see figure 3.2) will lead to a different leading edge of OUT_A. The rising edge of APULSE is set as a timing reference, then the delay of the leading edge of OUT_A is recorded, and a curve versus input voltage can be obtained. The time walk at the 268.4 mV threshold (roughly 300 e^-) of the preamplifier measured by an oscilloscope is around 57 ns, corresponding to the input voltage from 350 mV (~390 e^-) to 1100 mV(~1220 e^-), while the simulated value is 33 ns. The evaluated diode capacitance C_d is 5 fF, the evaluated threshold is about 300 e^-, corresponding to the experimental results of 268.4 mV. Figure 4.22 shows the delay of the leading-edge of 78 ns to 156 ns as a function of the OUT_A amplitude. The measurement curve (black line in figure 4.22) is parallel with the simulation (red line in figure 4.22), proving the test agrees with the design.

Although the analog front-end is optimized for a fast-rising edge and a short time walk, the standard CMOS Imaging Sensor (CIS) process adopted may not satisfy the speed requirement imposed by the CEPC completely. As the pixel structure in figure 2.8 shows, the charge collection time would be larger if the charge is generated in the nondepleted part of the pixel. A modification process [65] with a full depletion epitaxial layer has been adopted in the latest prototype.

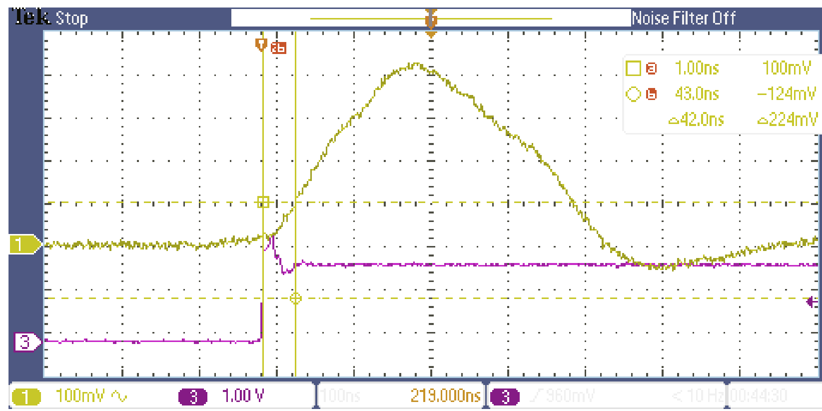


Figure 4.20 Leading-edge delay measurement with the oscilloscope, where the ΔV is 600 mV, the delay between the APULSE rising edge to the OUT_A of 100 mV is 42 ns.

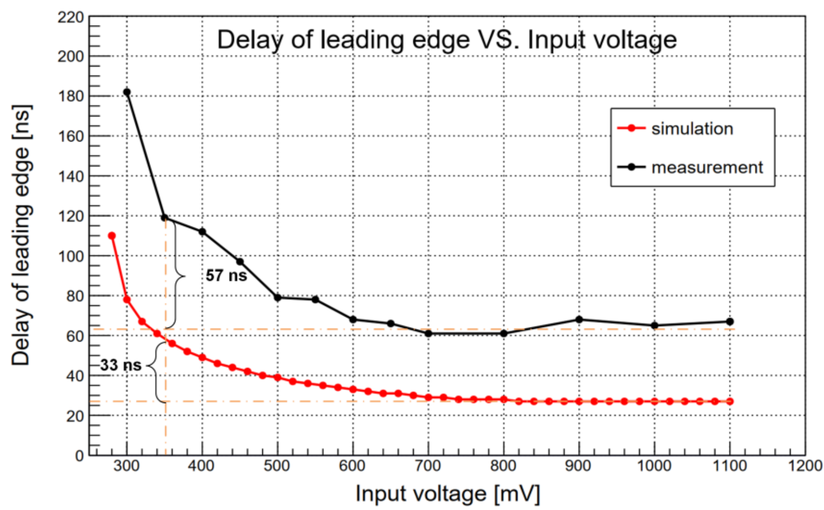


Figure 4.21 Delay of leading edge vs input voltage,simulation compared with measurement.

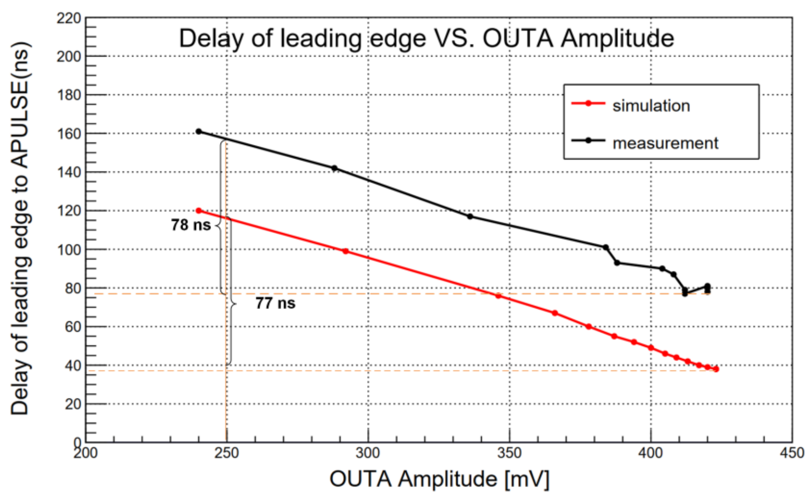


Figure 4.22 Delay of leading edge vs OUT_A amplitude.

Summary

This chapter details the optimization of the analog front-end. The common front-end electronics architectures were introduced to give an overview of the high-energy physics front-end electronics design. The development of monolithic devices and the limitations for the CEPC vertex detector were also presented. Modifications to the ALPIDE approach are needed to achieve the target of a fast-rising edge and a short time walk that are critical for the CEPC vertex detector. From the design simulation, the time walk is less than 25 ns, corresponding to the injected charges from 400 e^- to 3000 e^-, 2.5 fF diode capacitance and 182 e^- thresholds. This was achieved at the expense of increased power consumption, which is around 130 mW/cm^2. However, the characterization is not as good as expected since the reverse bias mechanism does not operate correctly. The sensor can work at 0 V PWELL, which results in an achievable threshold value of 268 mV (roughly 300 e^-), and a typical dispersion FPN of 24.4 mV, with a noise distribution with a typical TN of 9.7 mV for the pixels based on FEI3-like scheme. With this threshold setting, the time walk is measured roughly by an oscilloscope of 57 ns, at the injected voltage range from 350 mV (~390 e^-) to 1100 mV(~1220 e^-). More studies on how to reduce the diode capacitance and enable the biasing of the PWELL will be addressed in the future.

Chapter 5

Fast in-matrix digitalization

After the introduction of the analog front-end in chapter 4, this chapter will discuss the design of fast in-matrix digital design. This chapter will focus on the optimization of the in-matrix logic. Section 5.1 presents the motivation on why a fast in-matrix readout logic is needed. Two readout methods, rolling shutter, and data-driven architecture are introduced in section 5.2. It also provides a practical example of these approaches. Some limitations of the existing design for the CEPC vertex detector are discussed in section 5.3. The design of the chip and some characterization results are shown in sections 5.4 to 5.7.

5.1 Motivation of fast in-matrix readout logic

As already discussed, the output of the discriminator in the analog front-end stays high as long as the signal is over the threshold for a binary system. For a big matrix, when several pixels respond to the charges, it is necessary to process the data in a non-compressed way and store the pixel addresses. In a hybrid system, the sensor and readout chip are two different devices connected through a solder ball in a process called bump-bonding. This assembly process is complicated and expensive, the bump bond ball also increases the detector capacitance. On the other hand, monolithic devices do not require bump-bonding, they can provide devices with a smaller pixel area and significantly decrease the noise. But while the small pixel size improves the position resolution, it is more difficult to integrate the readout circuitry into the pixel cell. The CDR of the CEPC specifies that the readout speed for the vertex detector should be better than 10 μs, in order to minimize pile up from consecutive bunch crossings. Thus, the speed of in-matrix readout logic is critical to achieve this goal. On the other hand, as already noted, the pixel pitch for the CEPC vertex detector has to be 25 μm.

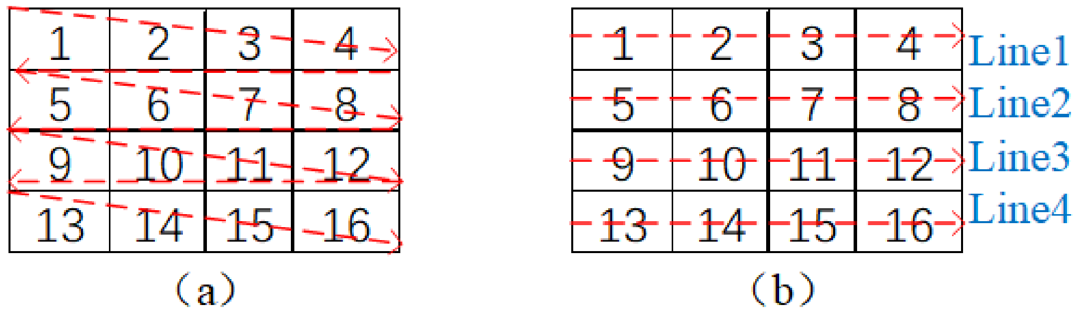


Figure 5.1 Readout pixel by pixel (a) and line by line(b).

5.2 Centralized readout and data-driven architecture

Two commonly used readout architectures are centralized readout and data-driven. In the case of centralized readout, all the pixels in the matrix are read out from the periphery of the pixel matrix and then eventually processed by a data sparsification algorithm [88] before being transmitted to the DAQ (data acquisition system). While in the data-driven readout case, only the pixels containing the hit are readout, which requires that the logic for starting the readout is allocated in each pixel.

5.2.1 Rolling shutter readout

The easiest way to perform the readout of a pixel matrix is to read it row by row, for example, from left to right, as illustrated in figure 5.1(a). The first prototype of the MIMOSA (Minimum Ionizing Particle MOS Active Pixel Sensor) chips based on MAPS was realized in this way [89]. In order to improve the readout speed and time resolution, all of the pixels in a row can be read out in parallel (see figure 5.1(b)). Each pixel is externally addressed and read through two shift registers, one is for the row, and the other is for column addresses. Later prototypes like MIMOSA22/MIMOSA26 were implemented with this approach [116].

Each row or line is processed at a fixed time interval in the rolling shutter operation. The rows are read from top to bottom and then the process is repeated. The sequencer activates different lines one by one. The time of reading all rows in the matrix gives the time resolution of the sensor. Figure 5.2 shows a block diagram of a basic rolling shutter matrix in which a column shift register and a row shift register are used to select a single pixel for readout. The logic to control the readout

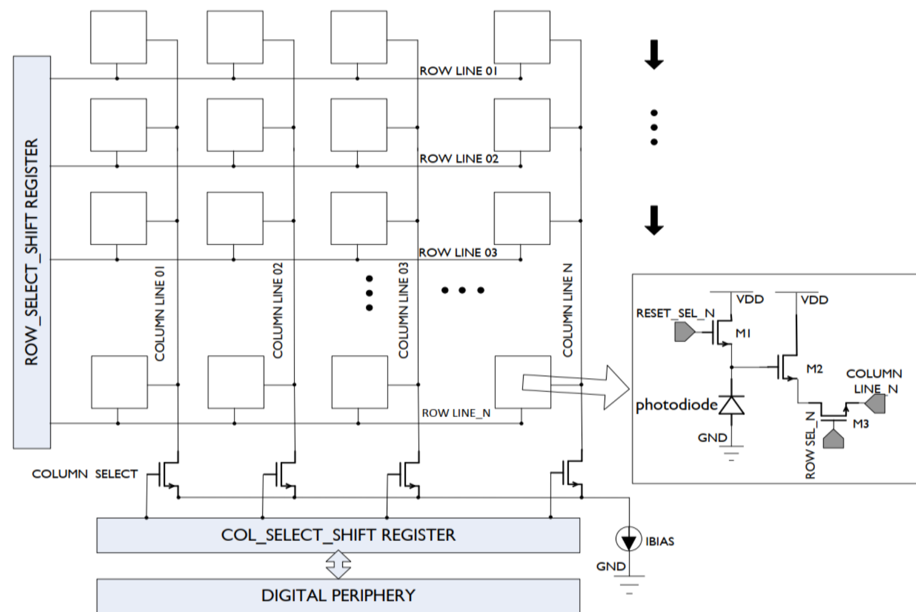


Figure 5.2 Three transistors pixel readout of the rolling shutter architecture. Taken from [71].

is located in the peripheral area of the active pixel matrix. Since the rolling shutter approach can be implemented without using a lot of space in the pixel cell, this approach can provide very high spatial resolution.

5.2.2 Data-driven readout

- **FEI3 readout architecture**

An alternative to centralized processing is data-driven distributed processing, in which each pixel unit independently detects that it has a hit and starts readout. Through this method, readout and sparsity are combined to improve the time resolution.

In the data-driven approach, usually, a counter is provided to each pixel unit, which runs freely until a hit is detected. Each hit cluster can be assigned to a specific beam crossing if the counter is synchronized with the experimental beam crossing clock. An effective and logical way to realize data-driven readout is to implement a sparse scan token ring between pixels in each column. The first pixel that gets the token can send data and pass the token to another pixel in the next clock cycle. As shown in figure 5.3, the FEI3 readout chip for the ATLAS pixel detector is a design example that relies on this structure. The pixels in each column share a token ring and a data bus, and the pixel holding the token places its hit information on the data bus. The information on the data bus is stored in the hit buffer in the chip periphery, and when a trigger signal arrives, it initializes the

buffer readout. Then the hits with the timestamp corresponding to the trigger event are readout, and the rest are rejected. The main problem of the token-passing scheme is that the readout speed is limited by the time the token needs to travel along the whole column. One way to improve timing is to implement some fast forward-looking and ripple logic. An example of this implementation is the priority look ahead logic implemented in the ATLAS pixel front-end electronic devices (like the FEI3 and FEI4 ASICs).

The fast priority scan paths are achieved by minimizing delays in critical data paths. In the case of the FEI3, each column with 160 pixels is arranged in 10 groups, each pixel group consisting of 16 pixels of three different types. The first two types of pixels are NAND and NOR units for fluctuating priority during sparse scanning. Pixels alternate between NAND and NOR versions to minimize priority sparse scanning delay and improve readout speed. At the end of each group, the third type of pixel unit is connected to the look-ahead path to achieve fast priority fluctuation [22].

Another example is the BUSY logic of the FEI3 readout chip. As just explained, each column is divided into ten 16-unit blocks to accelerate readout, calculated at the block level. The block-level BUSY OUT is the OR function of block-level BUSY IN and unit-level BUSY OUT [90]. Compared with the sequence line

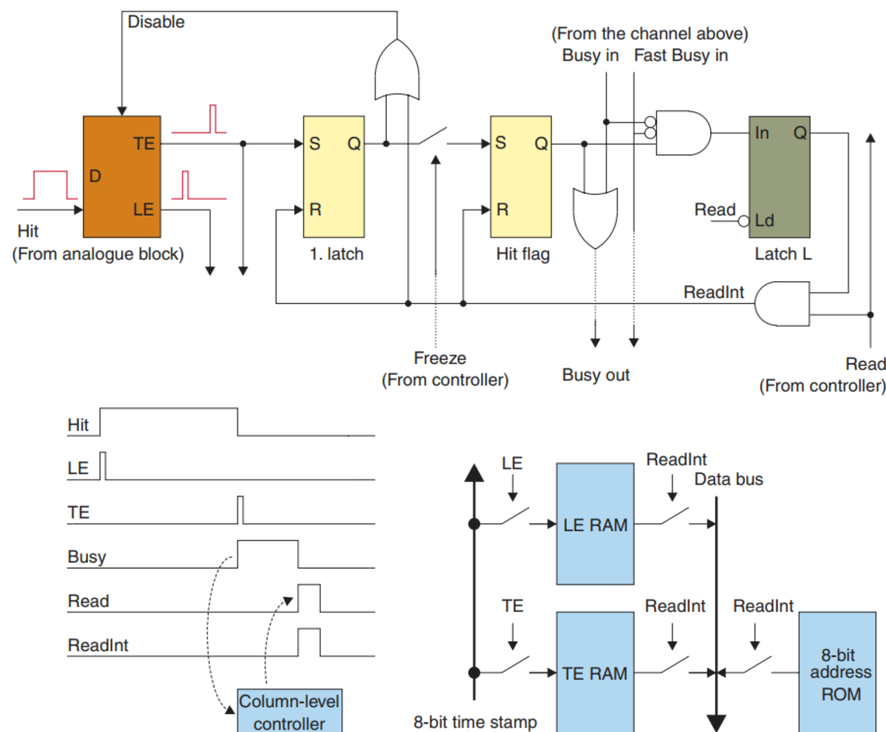


Figure 5.3 FE-I3 readout architecture. Taken from [22].

processing that has a fixed frame readout time, if the percentage of pixels occupied during the frame is relatively low, the data-driven method is particularly effective in terms of readout time. By immediately transmitting the hit information from the matrix, the overlap between hits is avoided. In order not to lose a second hit while waiting for the read priority, each hit pixel may also contain a buffer for a second hit, or at least one overflow bit to indicate that such a hit has occurred. Compared with the continuous readout, the trigger readout also effectively reduces the bandwidth required by the sensor readout circuit. The premise is that the buffer in the chip periphery is large enough to store the hit information of trigger events approaching each other in time. Otherwise, the buffer will overflow in some cases and introduce dead time.

- **Address-Encoder and Reset-Decoder (AERD) readout architecture**

Based on the arbitration tree scheme, the AERD readout circuit is implemented through a hierarchical address encoder and reset decoder [25]. The basic logic of the tree consists of three units, shown in figure 5.4 (a). FASTOR gate chains are used to generate VALID signals and propagate them to the periphery of the chip. The address encoder receives the priority logic output to generate the address value of each basic block. The reset decoder (NOR gate) is fed by the output of the priority encoder and a synchronization signal SYNC from a higher level to generate

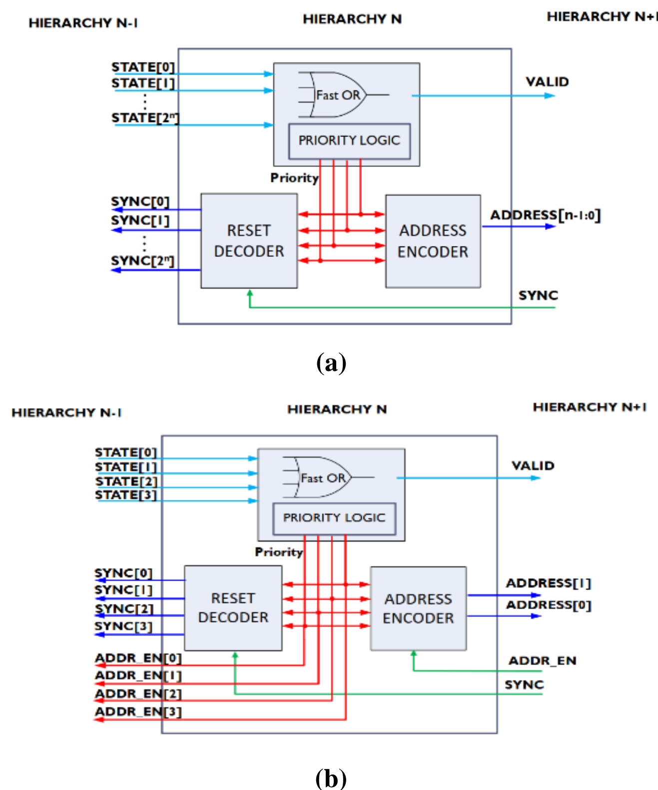


Figure 5.4 Standard AERD cell (a) and the boosting speed AERD cell (b). Taken from [25].

a SYNC for a lower level. The SYNC signal is then used to select the pixel with the highest priority to read and reset.

By using a full clock cycle instead of half a clock cycle to generate and propagate the address value to the end of the column, the readout speed can be improved to operate at 40 MHz. The main difference of the new logic block is that the output of the priority logic is used to enable the lower-level address encoder (figure 5.4 (b)). The address encoder at the top level is always active because there is only one block at the top level, and there is no conflict on the ADDRESS bus. More than one ADDR_EN output can be active because all blocks run parallel to the tree's second level. In order to ensure that only the pixels with the highest priority are enabled to encode the address and avoid conflicts on the address bus, additional OR gates are required to manage the priority path on the ADDR_EN signal.

The AERD data-driven readout structure shows significant advantages in readout time and power consumption, at the expense of complexity. The test results of the fabricated prototypes show that the AERD circuit running at 10 MHz [25] meets or exceeds the specifications of the ALPIDE. By separating the decoding and reset phases without any additional silicon region, the readout speed can be increased from 10 MHz to 40 MHz.

5.3 Discussion of the readout architecture for the CEPC

As discussed above, the rolling shutter readout with sequential row processing was the first architecture implemented in standard MAPS. The 0.35 µm CMOS technology devices used in the PXL detector of the STAR experiment achieve an integration time of 185.6 µs with a 20.7 µm pixel pitch. The integration time of the rolling shutter structure is defined by the readout time, while the matrix is always sensitive. The integration time of the rolling shutter depends on the number of rows for a given readout clock frequency. The frame readout time can be reduced by embedding row-wise parallel readout by increasing column-level discriminators. Since the particle rate of the RHIC experiment is around 3.8 kHz/mm^2[97], this approach meets the needs of the experiment.

Data-driven FEI3 readout chips for the ATLAS with time stamping are the architectures of choice for hybrid pixel detectors. However, for a 0.18 µm CMOS technology with 25 µm pixel pitch, MAPS do not have sufficient area per pixel cell for the standard FEI3 readout architecture. Another data-driven architecture AERD was also mentioned above. It was initially designed with TowerJazz 0.18 µm CIS technology, which is the same as TaichuPix. For the ALICE ITS, the standard architecture of AERD with 10 MHz readout speed is fast enough to meet the Pb-Pb 100 kHz interaction rate [40]. Since the boost speed AERD can be operating at 40 MHz, it is an interesting option for the CEPC vertex detector.

5.4 In-matrix readout architecture implemented in TaichuPix1

It has already been mentioned that TaichuPix1 includes two different pixel flavors: some based on the FEI3-like readout scheme and others on the ALPIDE scheme. These are shown in figure 5.5, half of the array implements FEI3 pixels (scheme1), and the other half ALPIDE pixels (scheme2). Both have a configuration register to enable an external APULSE signal for calibrating the analog front-end and DPULSE for testing the in-matrix readout logic. It also allows enabling/disabling the digital logic to mask the pixel.

The proven rate capability of the column drain implementations at the LHC, where the particle rate is similar to what is expected at the CEPC, makes this an attractive approach. However, to meet the small pixel size, the scheme needs some

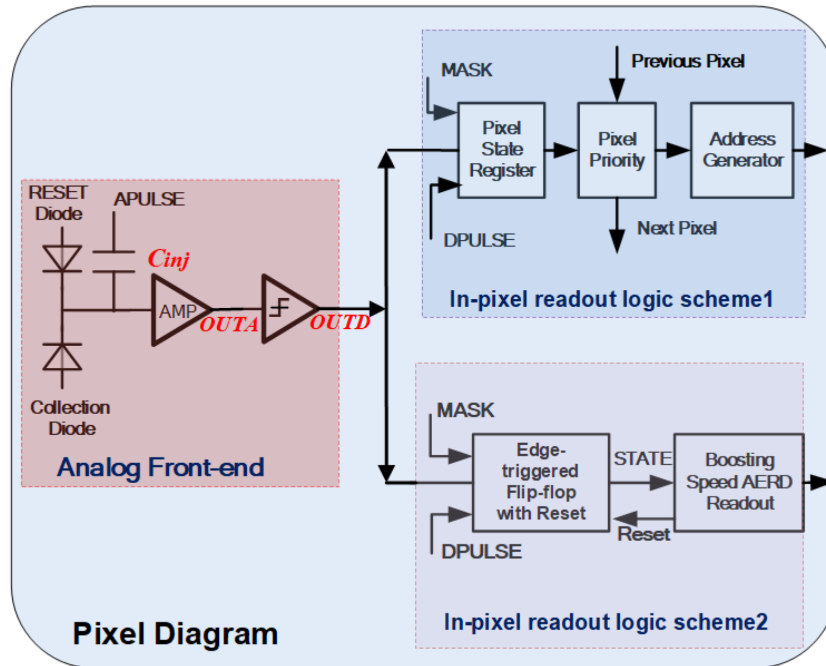


Figure 5.5 Two parallel in-matrix readout schemes, ALPIDE like scheme (scheme1) and FE-I3 like scheme (scheme2).

modifications. This is shown in figure 3.1. The timestamp is not stored at the pixel level but the EoC. In addition, the pixel address generator in figure 5.5 consists of pull-up and pull-down network matrices instead of a ROM memory as in the FEI3. The NMOS and PMOS transistors were dimensioned by finding a trade-off between the area and the drive strength. When a hit is detected, a hit flag is asserted. This is propagated through a priority OR chain in the double column. When the flag is received by the EoC cell, the current timestamp is stored. The priority OR chain is subdivided into 4 sub-priority OR chains to reduce the propagation time. In the worst case, the post-layout simulated propagation time is 9 ns. Since the period of a bunch crossing is 25 ns, it means that only those hits detected in the initial 16 ns after the beginning of a bunch crossing will be tagged with the correct timestamp. Such a situation is not a problem in the FEI3 chip. For FEI3, the timestamp is stored in the pixel immediately after a hit is detected.

The scheme based on the ALPIDE chip works in the same way as the FEI3 scheme: it detects hits and asserts hit flags. The main difference is the logic used to generate pixel addresses and how flags are propagated through columns. Those tasks are performed by a circuit named AERD. An AERD block manages the hit flag of four pixels generating a single hit flag and a 2 bit address. The pixels of the double-column are grouped in groups of 4 pixels, each one with an AERD circuit.

The bottom hierarchy of AERD module shown in figure 5.4(b) can handle 4 pixels at the input node of STATE. The output node VALID will connect the SYNC of the upper hierarchy of the AERD. And four cells are packed as a group to connect to one upper cell. Four upper groups can also connect as a new group, and in this way, pixels are merged by a factor of 4.

The priority AERD circuits are structured in an arbiter tree scheme. In this prototype, the arbiter tree in a double-column has 4 levels of AERD circuits and it generates a 7-bit address as a function of the 128 hit flags. It also multiplexes the 128 hit flags into a one-hit flag. The post-layout simulated propagation time of this multiplexer is 6 ns in the worst case. This propagation time has been achieved by modifying the AERD circuit according to [25]. The boosting speed mode of the AERD block uses the full clock cycle rather than half the clock cycle to generate and propagate the address value to the EoC. This improves the readout speed to run at 25 ns. Finally, the new in-matrix readout logic does not include the global control signal "STROBE" which is used for trigger latency, and the hit storage registers have been implemented with a small size flip-flop.

5.5 Token priority encoder implementation

To reduce the area of the in-matrix readout logic, some improvements have to be made to reduce space usage. The main token readout, shown in figure 5.6, was kept. It consists of an SR latch, a D flip-flop, and several basic gate logics. The READ signal is from the end of the column, which is used to read out the firing pixel and reset it. The previous hit would occupy the token bus until it has been read out, and then the next pixel can be read. The token also determines the priority of the pixels in a column, where the topmost pixel has the top priority to be read out when all the pixels fire simultaneously.

Compared with the initial FEI3 readout architecture in figure 5.3, a logic optimization has also been done in addition to removing the timestamp and memory inside the pixel. A standard AND gate will cost around 6 transistors, while the NAND gate has only 4 transistors required. At the same time, a dynamic flip-flop can save half of the transistors. Therefore, every logic cell has been replaced with the minimum transistors' solution. In this way, the overall readout logic has been reduced up to 44% of the space with respect to the initial one. Thus, more space can be reserved for the address encoder and bus routing. Finally, the area of in-matrix readout is optimized to $13.7\times25\ \mu m^2$.

Figure 5.6 Token readout implemented inside a pixel.

5.6 Timing sequences of in-matrix digital logics

Compared with the rolling shutter prototypes in MOST1, one of the improvements for TaichuPix1 is based on the column drain readout architecture. In the column drain approach, complex data buffering and trigger verification tasks are in the peripheral circuitry. Figure 5.7 illustrates the readout strategy for one double column. Take the first double column as an example. When the pixel receives a hit from the collection diode, it will generate a negative pulse that will be processed by the in-matrix readout logic. Then the hit information will be arbitrated by a token propagate to the EoC. The topmost pixel has the highest priority (red pixel in figure 5.7). When several hits arrive at the same time, the pixel with the higher priority is the faster to be readout. A FASTOR signal will be generated at the EoC as long as a pixel is fired, and then the digital circuitry will respond to a READ signal to read it out and reset the firing pixels. The address information of the firing pixels together with the timestamp will be stored into a column FIFO and

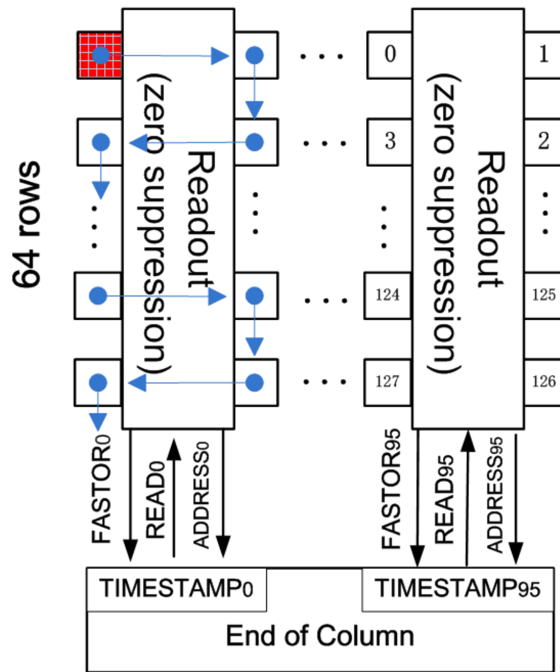


Figure 5.7 Readout diagram of TaichuPix1

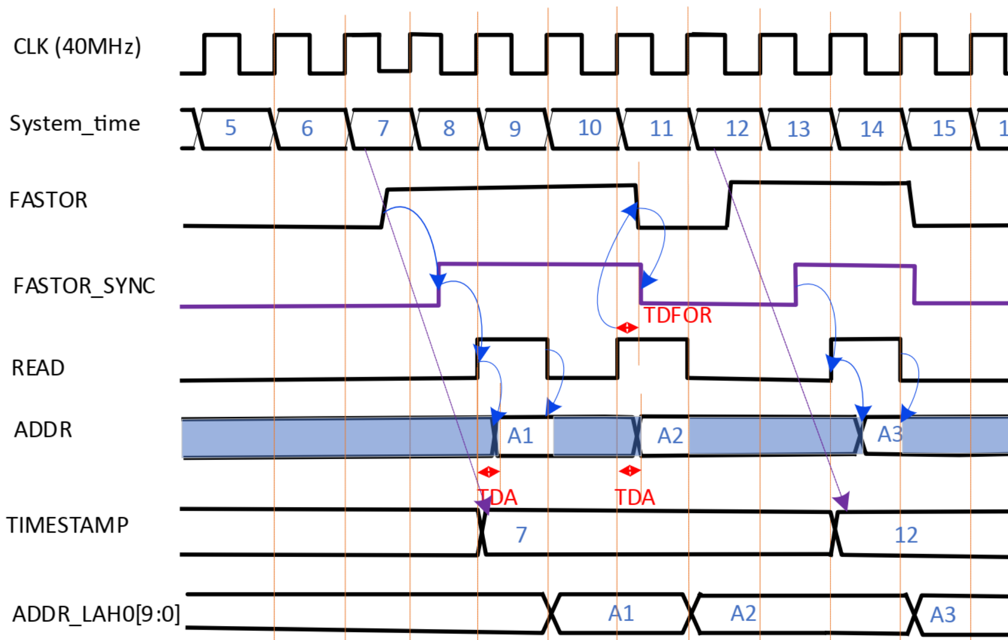


Figure 5.8 Readout timing diagram of TaichuPix1

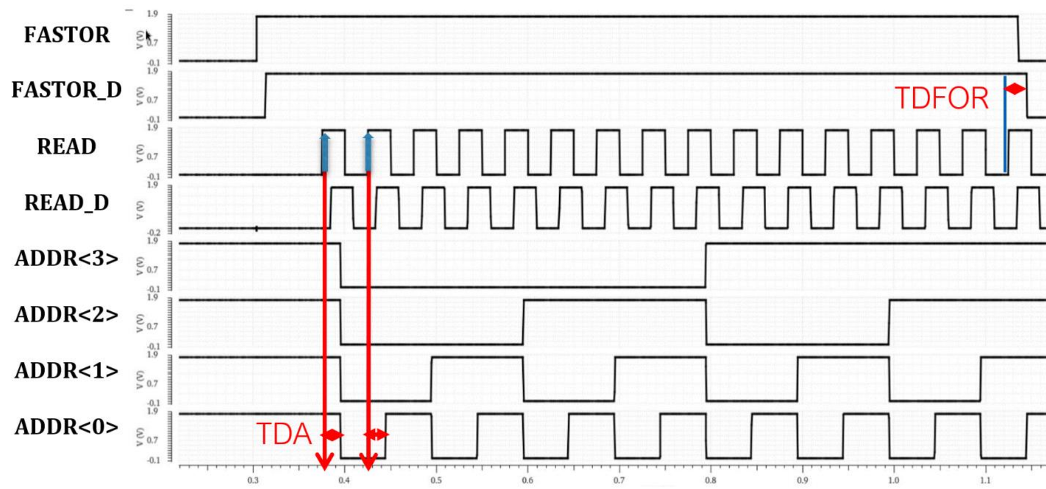
transmitted to the next stage. The system operating clock runs at 40 MHz, and thus the timestamp counter has 25 ns steps (see figure 5.8). The EoC will generate an internal synchronizing signal Fastor_sync, and the pixel state will be reset at the positive edge of READ. For the other readout scheme based on AERD, the reset

approach is different. The pixel state will be reset at the negative edge of the READ, and the TDA（Time of DAta）and TDFOR (Time of Data FORword) are set to a reasonable range to avoid the error from the delay of long metal lines.

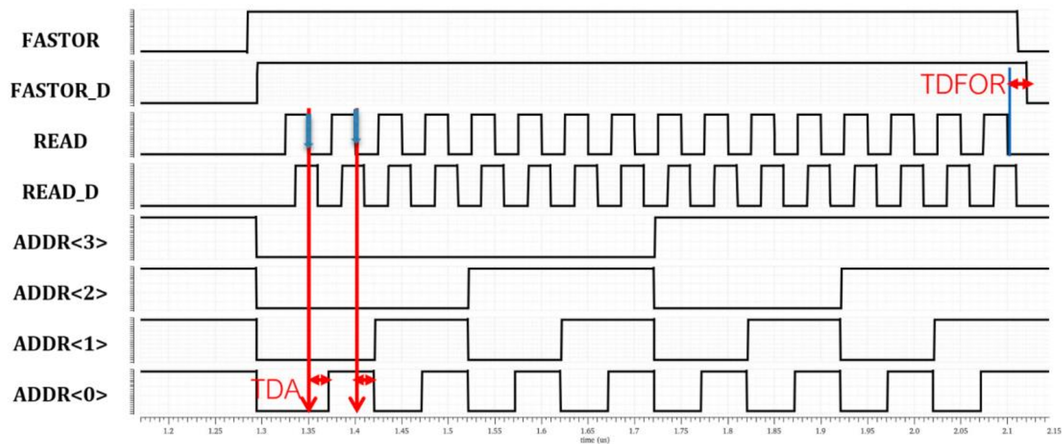
As previously mentioned, in the ALPIDE architecture, the peaking time of the front-end is matched with the STROBE signal latency, and the data will be written into the pixel state register only when the STROBE is asserted. However, when there is no STROBE signal provided to the chip, see the schematic simulated waveforms of figure 5.9, the READ signal for the first pixel (Pixel0) will be repeated many times. In the pixel design of TaichuPix1, this is improved. The pixel state registers are replaced by edged-triggered flip-flops, which can assert the READ signal at the falling edge of the output of discriminator OUT_D. The simulation waveforms are plotted in figure 5.10. Compared with figure 5.9, it is evident that the Pixel0 will only be read out once.

Following the readout timing diagram of figure 5.10, the delay simulation waveforms are depicted in figure 5.11. The long metal line brings a delay to the FASTOR and READ signal. These results are shown as FASTOR_D and READ_D in figure 5.11. Table 5.1 shows the delays on the nominal corner (TT) and the worst corner (SS). The digital periphery is designed to tolerate the case of the worst

corner.



(a)



(b)

Figure 5.11 The simulation waveforms based on RC delay from the long metal line of FE-I3 like scheme**(a)** and ALPIDE like scheme**(b)**.

Table. 5.1 Delay simulation of 2 corner，TT：nominal corner，VDD=1.8V，27℃
SS：slow corner VDD=1.6V，50℃

DELAY	TT[1]	SS[1]	TT[2]	SS[2]
FASTOR	7.7 ns	13.3 ns	7.7 ns	13.3 ns
READ	7.7 ns	13.3 ns	7.7 ns	13.3 ns
TDA	16.4 ns	26.1 ns	16.5 ns	26.4 ns
TDFOR	16.8 ns	26.7 ns	16.9 ns	24.9 ns

5.7 Power density evaluation and physical implementation

As stated above, the TaichuPix1 was designed with a 0.18μm CMOS process and the pixel size is 25×25 μm^2. Figure 5.12 presents the layout of four adjacent pixels in a double column. The main modules of the pixel cell, the charge collection diode, the analog front-end, in-matrix digital logic, and the sharing address encoder are highlighted. The charge collection diode is located in the middle of the top of each pixel.

In the case of the FEI3 for the ATLAS pixel detector the cell size is 50×400 μm^2 and the chip was fabricated in a 0.25 μm CMOS process. This cell size is much

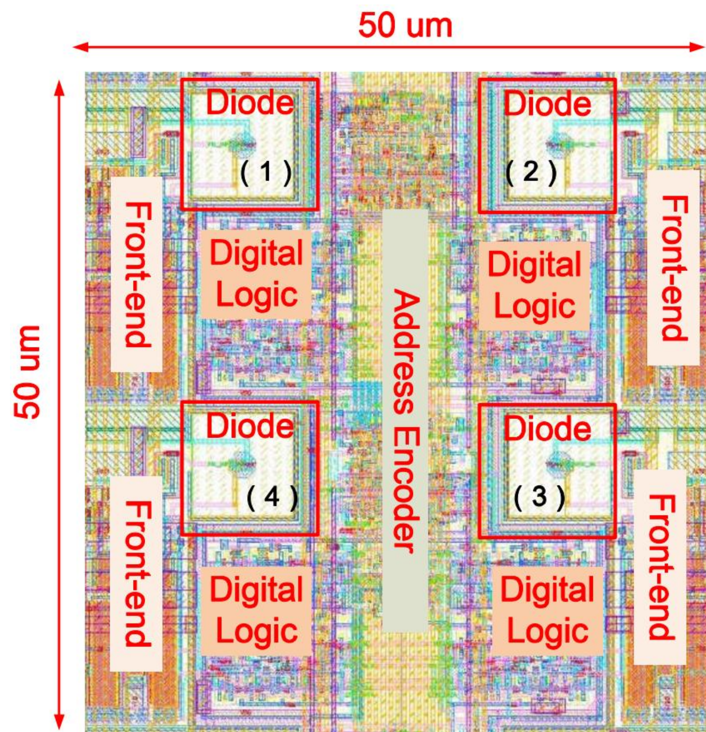


Figure 5.12 Four pixels layout

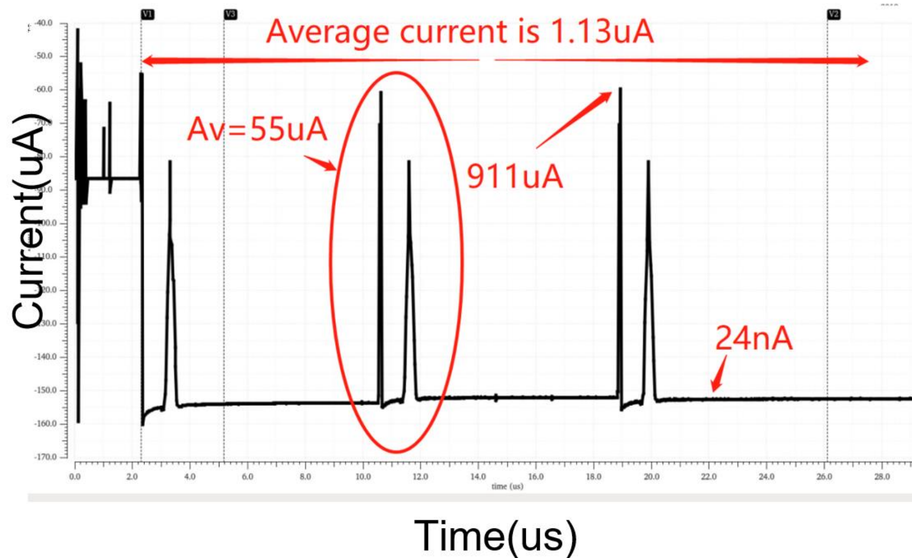


Figure 5.13 Transient current of the in-matrix digital logic with 3 hits.

bigger than the target size of the TaichuPix1. Thus, there is more space to design a complex readout circuit in the FEI3. In order to fit the limited area, the FEI3 readout approach was modified as presented above. The timestamp is not stored inside each pixel but at the EoC, and the address has been implemented by a pull-up and pull-down network matrix instead of the ROM memory. A dynamic D flip-flop was implemented to reduce the area further. With these modifications, enough space to place the in-matrix digital logic was obtained.

The region for in-matrix digital readout logic is shared by two columns. This avoids cross-talk between analog biasing lines and digital buses while it frees space for routing the address encoder. As it is shown in figure 5.12, in terms of the area used in the pixel cell, the size of the collection diode is 8.6×8.6 μm^2, the layout area for the analog front-end is 8.2×25 μm^2, and the rest of the space is reserved for the in-matrix readout logics and bus routing. It is obvious that in this approach, further reducing the pixel cell area is almost impossible. A possible solution is to look for a smaller technology, like TowerJazz 65 nm. The circuitry inside a pixel can be more complicated with smaller transistor dimensions.

The power density of the in-matrix digital logic has also been considered during the design of the TaichuPix1. The digital logic generates a considerable power consumption when the gates state is toggled and during the clock propagation to each sequential logic circuit. Thus, the dynamic power of the in-matrix digital logic is produced when hits arrive at the chip or the readout is being performed. The FEI3-like scheme will result in an average current of 55 µA during the readout phase in a double-column (see figure 5.13). This value converted to

power density is about 123 mW/cm^2. The static current is around 24 nA, so it is negligible. The average hit rate to each column is 120 kHz/column so that the mean current is about 1.13 µA. With the same evaluation method, in the ALPIDE-like scheme, the power density is around 49 mW/cm^2 during the readout phase. For the TaichuPix1, similar numbers in terms of power dissipation are expected.

5.8 Characterization of the in-matrix readout architecture

The function of the in-pixel digital readout electronics is to monitor the output of the discriminator. When this is high, it raises a flag which the EoC processes. Once the pixel has been read, the flag is set to low. This has already been explained above, this subsection is going to show the strategy for measuring and verifying the process.

As already mentioned, a DPULSE test port is used in the in-pixel readout electronics to bypass the discriminator and inject pulses directly to the pixel digital stage to test the pixel readout process. The DUPLSE injection can be read out from FIFO2 when the chip is set up in the debugging mode.

FIFO2 is a global buffer located at the periphery, which is used to match the read rate inside the chip and the data rate of the high-speed serial output device. Figure 5.14 presents the data readout from FIFO2. The measurement is under the condition when the chip is set to debug mode, the system clock is 40 MHz, the internal digital logic circuit of all pixels is turned on, a positive pulse DPULSE (see figure 5.5) is injected into each pixel from the outside, and it is received from the

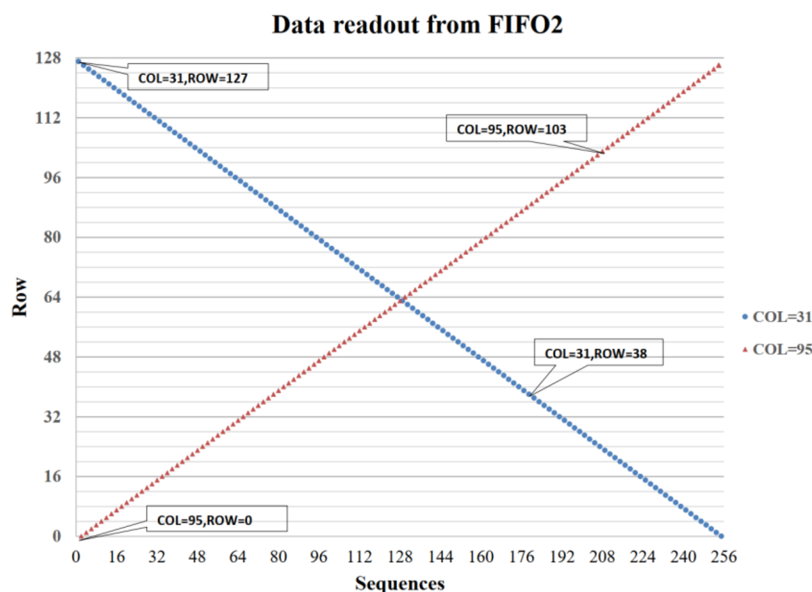


Figure 5.14 Data readout from FIFO2 in debug mode.

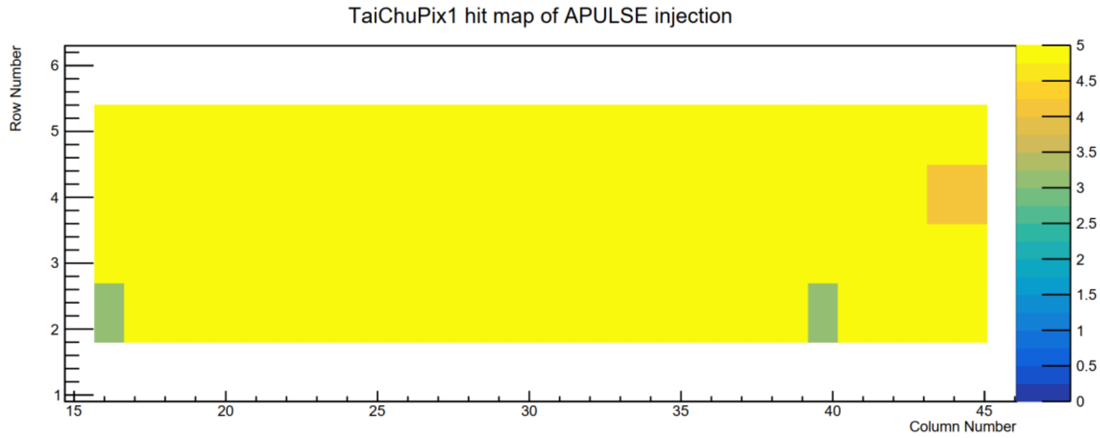


Figure 5.15 Hit map of a 4×30 region with 5 times APULSE injection.

global buffer FIFO2 through the Serial Peripheral Interface (SPI). Since the storage depth of FIFO2 is 256 bytes, only two complete double columns of data can be received at one time in this mode. In figure 5.14, the horizontal axis represents the storage address order of the FIFO2 data sequence (Sequences), and the vertical axis represents the row (ROW) address information of the hit pixel. The 31st column with the highest priority in FEI3-like scheme (COL=31) and the 95th column with the highest priority in ALPIDE-like scheme (COL=95) are read in order. Since the data is read out with a double column, each column will encode from rows 0 to 127. The row index of the pixel with the highest priority in the FEI3-like scheme is 127, while the ALPIDE-like scheme is index 0. This indicates that the digital logic inside the pixel of the TaichuPix1 works properly. It can convert the received test pulse into a digital signal and transfer the address information after the matching timestamp to the peripheral circuit. And the column drain-based priority arbitration readout meets the system requirements. In the case of simultaneous hits, the data can be read out in sequence according to its priority.

In addition to DPULSE, APULSE can be used to verify the function of in-matrix readout logic as well. As already mentioned, each pixel consists of a sensing diode and analog front-end surrounded by the in-matrix digital logic. As shown in figure 5.15, the analog front end is set with a proper value when the APULSE signal is injected into a specific region of pixels. Figure 5.15 shows the case for a 30×4 matrix with 120 pixels. The rest of the pixels are shielded by the one-bit shifting register chain (see figure 7.2). As the function of masking for the ALPIDE-like part is not operated well, so only FEI3-like pixels are measured. The hit map shows the results which read out from FIFO2. When APULSE is sent 5 times, most pixels in this region record the hit information correctly. A few pixels at the edge lost some

hit, since the threshold of each pixel is not the same (see figure 4.19 (a)), it overall agrees with expectations.

Summary

This chapter discussed two commonly used readout methods, the rolling shutter and the data-driven architectures. From the CDR of CEPC, the ultimate chip should meet the requirement of small pixel size and fast readout. This guides the design of in-pixel readout logic of the TaichuPix1. Two practical readout approaches, FEI3 and ALPIDE AERD, are good references to start the in-matrix logic design. But the initial circuits, do not fully satisfy the requirements of the CEPC vertex detector. Further optimizations were done to fulfill the target. The space for in-matrix logic is limited to a 25 ×25 μm^2 pixel size, the sensor and analog front-end area, already take around 55% of one pixel cell. In the FEI3-like approach, the address ROM has been replaced by a pull-up and pull-down network matrix due to these area limitations. The timestamp is not stored in-pixel but at the end of the column. In the ALPIDE-like scheme, the pixel cell structure is the same, but a dynamic edge-triggered flip-flop has replaced the hit storage registers in order to prevent reading out one hit repeatedly before the analog front-end resets. A boosting speed AERD was implemented. For the simulation and one-column test, both approaches meet the requirement of operating at 40 MHz.

Chapter 6

High data-rate peripheral digital readout logic

At the end of columns, the peripheral readout logic is designed to satisfy the data rate requirement of the CEPC vertex detector. This chapter discusses the design details of the high data-rate peripheral digital readout logic for the full-size chip (a matrix of 1024×512), and the peripheral readout logic implementation for TaichuPix1 is presented in section 6.6. Section 6.1 provides the motivation of the digital readout logic, explaining why a high data rate in the periphery is necessary. The design details are given in the rest of the sections, and it includes the design considerations, the architecture, the fast readout approach, and the power consumption considerations.

6.1 Motivation to the peripheral digital readout logic

The ALPIDE chip is a good start point for the CEPC vertex detector since, as mentioned in previous sections, it was developed for the ALICE-ITS upgrade and its performance is very close to meeting the requirements of the CEPC. However, the interaction rate for the application of ALPIDE is 100 kHz, and the interface data rate is 1.2 Gbps [87]. While for the CEPC vertex detector innermost layer, the maximum pixel hit rate is near 120 MHz, and the interface data rate can reach 3.84 Gbps, much higher than the design requirements for the ALICE-ITS. Therefore, a new readout architecture with a high data-rate readout logic has been proposed.

The beam-induced background will impact the occupancy of the vertex detector, which is a critical parameter for the innermost detector layer. At the center-of-mass energy of 240 GeV, the CEPC will be operated as a Higgs factory. It also will be possible to operate at 91 GeV as a Z factory and 160 GeV as a W factory. The bunch spacing of the CEPC colliding beams will be 680 ns, 210 ns, and 25 ns for the Higgs, W, and Z operations, respectively. And the expected hit density of the Higgs boson in the CEPC is around 2.4 hits/cm^2 per bunching crossing. For a 512×1024 pixel matrix with a 25 μm pixel pitch, the chip sensing active area will be around 3.28 cm^2. Assuming a conservatively large cluster size of 3 pixels, the hit density of Higgs for a chip will be:

$$2.4 \text{ hits/(bunch} \cdot \text{cm}^2) \times 3.28 \text{ cm}^2 \times 3 \text{ pixels/hit} \approx 24 \text{ pixels/bunch}$$

And the pixel hit frequency per chip is:

$$24 \text{ pixels/bunch} \times (1/680) \text{ bunch/ns} \approx 36 \text{ MHz} \cdot \text{pixels}$$

For the triggerless mode, the interface data rate per chip is

$$36 \text{ MHz} \cdot \text{pixels} \times 32 \text{ bits/pixel} = 1.152 \text{ Gbps}$$

Considering 32 bits of information to be transmitted per hit pixel and an average trigger rate of 50 kHz, the interface data rate per chip will be

$$24 \text{ pixels/trigger} \times 50(\text{trigger} \cdot \text{kHz}) \times 32 \text{ bits} = 38.4 \text{ MHz}$$

As for the Z boson, since the bunch spacing is 25 ns and a 175 ns (25 ns×7) timestamp error window is considered, the hits within 8 timestamps can be recorded. Then the interface data rate in trigger mode per chip is:

$$2.5 \text{ pixels/trigger} \times 50 \text{ trigger} \cdot \text{kHz} \times 8 \times 32 \text{ bits/pixel} = 32 \text{ MHz.}$$

The hit density and the chip data rate are summarized in table 6.1. In order to satisfy the stringent conditions, the readout speed aims to reach around 120 MHz per chip which can satisfy all of the configurations. At the same time, a data rate flexible interface is necessary to meet all of these requirements.

. **Table 6.1** The hit density of CEPC

Parameter	Unit	Higgs	W	Z
Bunch spacing	ns	680	210	25
Hit density	hits/(bunch·cm^2)	2.4	2.3	0.25
	hits/(bunch·chip)	7.87	7.541	0.82
	pixels/(bunch·chip)	24	24	2.5
Pixel hit frequency	MHz/cm^2	11	36	32
	MHz/chip	36	120	100
Chip data rate Triggerless	Gbps	1.152	3.84	3.2
Chip data rate Trigger	Mbps	38.4	38.4	32

6.2 Design considerations of the periphery readout

For the peripheral readout logic design, the hit rate and accepted dead time are the main considerations. The hit rate can be calculated based on the CDR of CEPC. As shown in table 6.1, the maximum hit data rate per chip is about 40 MHz for W boson, which assuming a conservative cluster size of 3 pixels, results in a maximum rate of 120 MHz. This data frequency leads to the need to design a fast interface. Supposing that the data to be read out from each hit pixel is re-encoded in a 32-bit word (timestamp: 8 bits, pixel address: 19 bits, others: 5 bits), the output data rate needs to be 3.84 Gbps. It is not easy to handle such high data rates in a data acquisition (DAQ) system. The general solution is to provide a trigger signal and only send data that matches the trigger signal to the DAQ system. This work assumes that the trigger delay and average trigger rate are 3~6 μs and 50 kHz, respectively. Considering the number of the firing pixels in each bunch, the bunch spacing, and a time error range of 0-7 clock cycles, the maximum data rate of the trigger mode is less than 40 Mbps. The data acquisition system is more likely to be based on a trigger mode. But since the design is not decided at this point, both the trigger and triggerless modes should be implemented in this prototype version of the CEPC vertex chip.

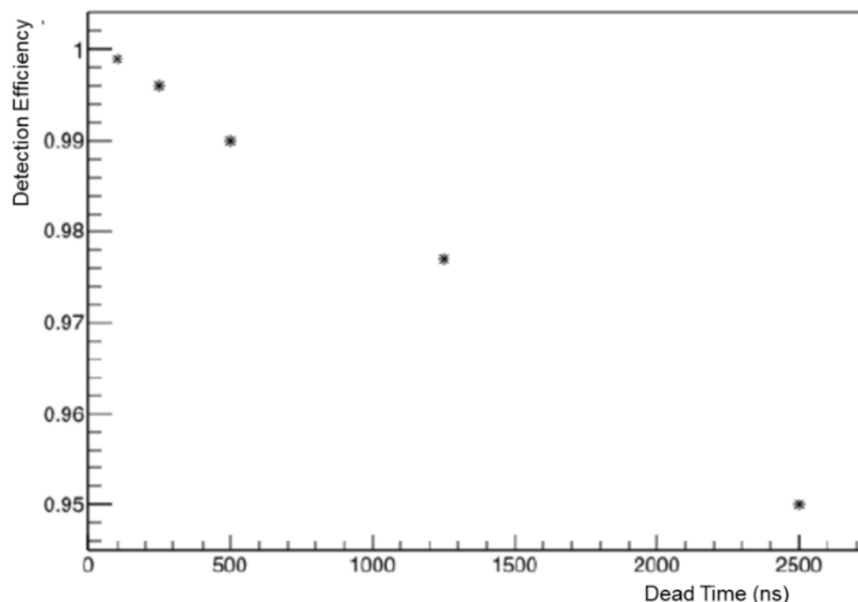


Figure 6.1 Simulation of detection efficiency vs. dead time. All columns are read out parallel in the simulation.

For pixel sensors, the dead time is expected to be short. A large dead time will

reduce detection efficiency. Different readout methods were adopted to evaluate the relation between detection efficiency and dead time. Figure 6.1 shows a simulation study. This simulation assumes that the array is in a double-column (DCOL) structure similar to ALPIDE. In this approach, the pixel array is read in parallel to reduce the reading time. Therefore, the total dead time of the chip is the time to read a DCOL, that is, the time to read the hits of a DCOL of 1024 pixels. As shown from the simulation diagram, to achieve a detection efficiency higher than 99%, the dead time should be less than 500 ns. This assumes that the array only reads out the hit pixels. The number of hit pixels can be evaluated according to the hit density in table 6.1. According to the Poisson distribution, it can be estimated that the number of hit pixels in a DCOL within 500 ns is less than 3. If the cluster is assumed to be 3, the number of pixels that need to be read should be less than 10. Therefore, the readout time for a pixel address is about 50 ns. So, with these modifications of the schemes mentioned above, the ALPIDE-like and FEI3-like readout schemes, can all meet the required readout time.

6.3 Design of the high data rate readout logic

As mentioned above, both data rate and dead time are taken into account in the digital readout logic design. The block diagram of the peripheral reading is shown in figure 6.2. Each DCOL of the pixel array is read in parallel. The timestamp is recorded at the end of the DCOL, and data with matching timestamps is buffered for output in trigger mode. In the triggerless mode, all data is buffered and sent to the output.

The overall structure of the peripheral readout includes a two-level FIFO. The first-level FIFO1 is used to temporarily store the pixel address of each DCOL, and given the data rate and dead time, the FIFO1 depth is 12 to 16. The second-level FIFO2 is used to match the readout speed of the chip interface. In total, there are four chip-level FIFO2s with a depth of 256. In the peripheral logic design, 32 DCOLs form a group for addressing priority readout, and the four 32 DCOLs (4×32=128 DCOLs) readout methods follow the token approach. Moreover, both trigger and triggerless modes are satisfied. The trigger mode uses the timestamp to remove unmatched data, while the triggerless mode reads all data.

In the preliminary design, for a 512×1024 pixel array (i.e., for the final chip for the CEPC vertex detector), the readout time of the pixel address would be 50 ns since the expected pixel pitch is less than 25 μm. In order to meet the dead time,

512 DCOLs would be read in parallel. The readout circuit of each DCOL mainly will include a DCOL reader, a double-column FIFO (FIFO1), and a trigger discrimination logic (Trigger and match). The DCOL reader provides synchronous read signals and receives pixel addresses from each DCOL. The data output by the DCOL reader is temporarily stored in the column-level FIFO (FIFO1).

The trigger discrimination logic determines whether the data will be sent to the chip level FIFO2. With trigger mode, only send data with matching timestamps will be sent while the unmatched data will be overwritten. The valid data frequency is 1~1.2 MHz/32 bits, as shown in table 6.1. The internal register can set the read frequency in the trigger mode according to the actual trigger frequency and the error of the recorded timestamp. As in the case above, the chip-level FIFO2 would be used to match the speed of the chip interface in trigger mode. The discrimination logic is bypassed in the triggerless mode, and all data in the 512 FIFO1 needs to be read. The average data frequency is 120 MHz as the hit pixel frequency, and this work uses a 160 MHz clock to read them to match the 40 MHz system clock. And all data is also buffered with FIFO2 in the triggerless mode. This design proposes

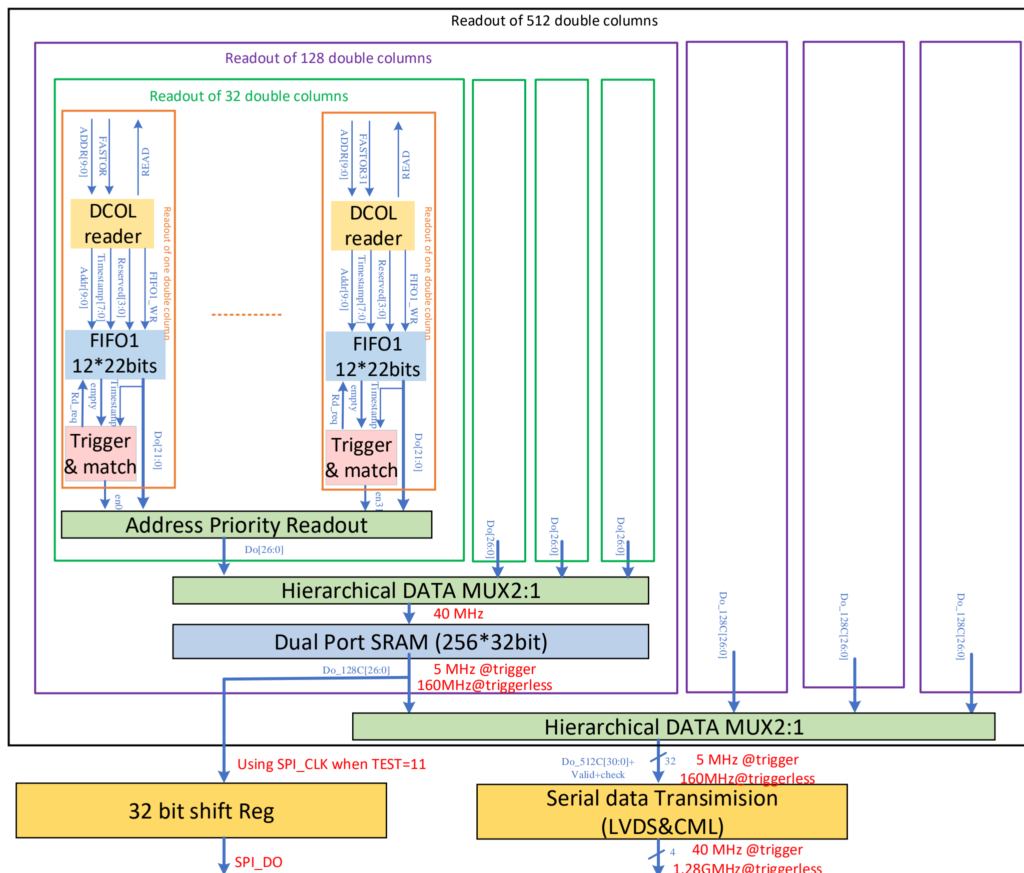


Figure 6.2 Block diagram of the readout architecture.

a fast readout structure for reading data from FIFO1 to FIFO2 and from FIFO2 to the chip interface.

6.4 Fast readout for the full matrix

The design for the full-size chip proposes a new architecture to do a fast read of 512 DCOLs, as shown in figure 6.2. Since the system clock runs at 40 MHz and the average data frequency has 120 MHz, the entire pixel matrix is divided into 4 blocks. FIFO2 is integrated into each block to match the speed of the system clock and the output interface clock. Each block contains 128 DCOLs. In trigger mode, the column FIFO (FIFO1) depth should be sufficient to read data without losing any data. Since the maximum trigger latency is 6 μs, the FIFO1 stores data for 10 μs. The amount of data that needs to be read in trigger mode is much smaller than that in triggerless mode. To implement a fast readout structure design, the challenge is the data rate in the triggerless mode. According to the hit density in table 6.1, each DCOL receives a hit every 4 μs on average. In order to read data quickly and avoid unnecessary readout cycles, it is a better choice to use a data-driven scheme at the bottom level of each group of 32 DCOLs. According to the address priority, only the non-empty FIFO1 is read. For 32 DCOL groups, the hit rate reached is 7.5 pixel/μs. Therefore, this work attempts to avoid data blocking by providing equal output opportunities among the read requests from the four sets of 32 DCOLs.

In the final chip, a hierarchical data multiplexer with special token control is envisioned to provide the average response to reading requests between two 32 DCOL groups. The state machine is shown in figure 6.3. When one group (A/B) is being read, the read request from the other group (B/A) will respond first. Thus, if both groups send read requests, the two groups respond alternately. A group can only be read continuously without a request from the other group. This work uses three units to realize the responsibilities of the four groups. The same hierarchical

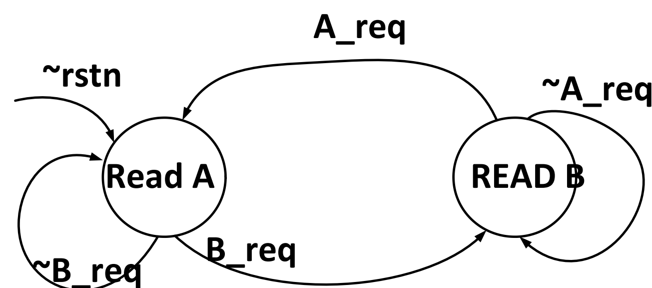


Figure 6.3 State machines for a data selector. Taken from [26].

data multiplier at the chip level is used to carry out the readout of the four chip-level FIFOs (FIFO2).

6.5 Simulation results of the peripheral readout logic

The readout logic of a 512×1024 pixel array (which would correspond to the final chip) is simulated on the test bench, including a hit generation module, a double-column pixels model, and a data analysis module. The hit data number is generated according to the Poisson distribution, and then the data is randomly assigned to a double column. Both FEI3-like timing and ALPIDE-like timing models are implemented. The pixel address can be set to random, increment, and decrement. By comparing the sent data and received data, the simulation results are analyzed. The actual data rate was calculated from the transmitted data.

The readout logic is simulated in trigger mode and triggerless mode. Different trigger delays, timestamp errors, random, increment, decrement, concession, and discontinuous data are considered. The simulation results show that all functions are well supported. In triggerless mode, the acceptable hit pixel is 120-130 MHz, and the main limitation is the readout frequency of 160 MHz. In the trigger mode, no data loss was found for the 160 MHz hit pixel (because most of the data was not readout), and the depth of FIFO1 was sufficient to meet the maximum trigger delay of 6 μs. In short, the hit pixel frequency of 120 MHz can be handled well in various situations.

The power consumption of the peripheral digital readout was also evaluated. Figure 6.4 shows the estimated power consumption of the peripheral readout logic

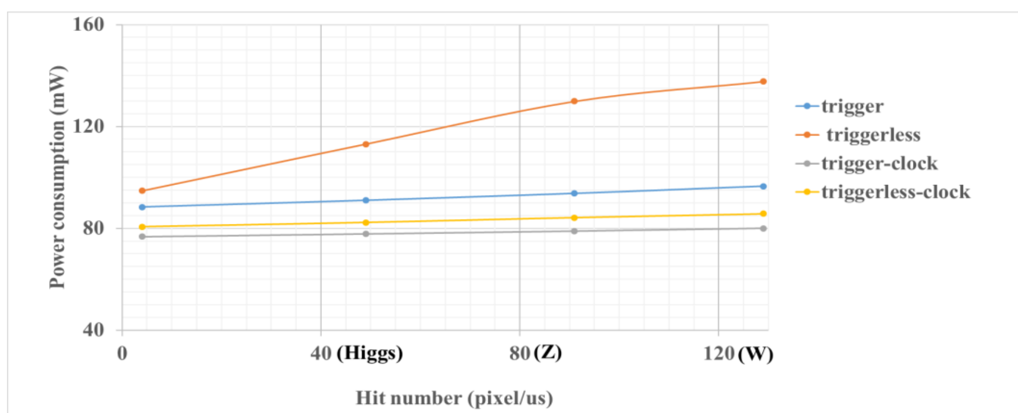


Figure 6.4 Power consumption of the periphery digital readout circuitry in different mode. Taken from[26].

in PrimeTime [91]. It is based on different average hit frequencies of 4 MHz, 49

MHz, 91 MHz, and 129 MHz. The post-simulation power consumption of these conditions ranges from 80 mW to 140 mW, and in trigger mode, the density is 25 to 30 mW/cm^2. At the same time, the triggerless value is 35~45 mW/cm^2. It is noted that the power consumption of the clock network accounts for 80%.

6.6 Small scale readout logic implementation for TaichuPix1

Since fabricating a chip with a full matrix of 512×1024 pixels directly are risky, so a small-scale Multi-Project Wafer (MPW) array with 64 ×192 pixels (the TaichuPix1) was implemented first. It includes all of the critical blocks to verify their feasibility. The high data rate peripheral readout logic discussed before was integrated inside the chip. For the TaichuPix1, 3 fast readout groups have been included, and each group contains 32 DCOLs. And every DCOL has 128 pixels. It includes a full architecture of the peripheral readout logic, DCOL reader, FIFO1, trigger and match logic, address priority readout, hierarchical data multiplex, dual-port SRAM (FIFO2), 32-bit shift register, and serial data transmission interface. A DCOL of 128 pixels, is enough to evaluate all the performance of the periphery readout logic. The difference from the full matrix is the significant bits of a data word. The data is still transmitted with a 32-bit word, but only 7 bits of significant LSB were used to record the address rows (9 bits in all) and columns (10 bits in all). The rest of the bits are forced to zero (connected to 0 V).

Summary

According to the CEPC vertex detector requirement, the bunch spacing of the CEPC colliding beams are 680 ns, 210 ns, and 25 ns, for the Higgs, W and Z operations, respectively. Among these requirements, the most stringent one is to satisfy W boson's hit density and bunch spacing. Assuming an average cluster size of 3 and the 512×1024 pixel matrix, the triggerless data rate is around 120 MHz/chip, and the interface speed for a 32-bit word needs to be 3.84 Gbps. A dedicated high data rate peripheral readout logic has been designed, including a DCOL reader, FIFO1, trigger and matches logic, address priority readout, hierarchical data multiplex, and dual-port SRAM (FIFO2). At the same time, a fast readout group of 32 DCOLs is designed. A trigger mode is also implemented to reduce the interface speed. Assuming a 3 μs to 6 μs trigger latency, and an average frequency of 50 kHz, the data rate for the output interface is below 40 Mbps. From the simulation, the speed of peripheral readout logic is sufficient, with a data rate of 120 MHz without any data loss. The power evaluation shows a density of 25~30 mW/cm^2 for trigger mode and 35~45 mW/cm^2 for triggerless mode. The characterization results will be discussed in the next chapters.

Chapter 7

Test platform based on Xilinx ZYNQ and TaichuPix1 Configuration

This chapter briefly introduces the test platform based on the Xilinx ZC706 Kit developed for the TaichuPix1 chip. Section 7.1 is a general introduction of the ZC706 Kit resources. Section 7.2 describes the embedded operating system PetaLinux, used for software development on the ARM processor. The pixel configuration method, the common readout configuration interface, and the serial data format are shown in sections 7.3 to 7.5. Section 7.6 illustrates the hardware platform designed for the TaichuPix1. Finally, the implementation of firmware and software are presented in sections 7.7 and 7.8.

7.1 Introduction of Xilinx ZC706 Kit

The ZC706 evaluation board [27] for the XC7Z045 SoC (System on Chip) provides a hardware environment for developing and evaluating designs targeting the Zynq-7000 XC7Z045-2FFG900C SoC. The ZC706 evaluation board features many embedded processing systems, including DDR3 SODIMM (Small Outline Dual In-line Memory Module) and a four-lane PCI Express interface, component memory, an Ethernet PHY (PHYsical Layer), and two UART general-purpose I/O interfaces. Other features can also be supported by using VITA-57 FPGA mezzanine cards

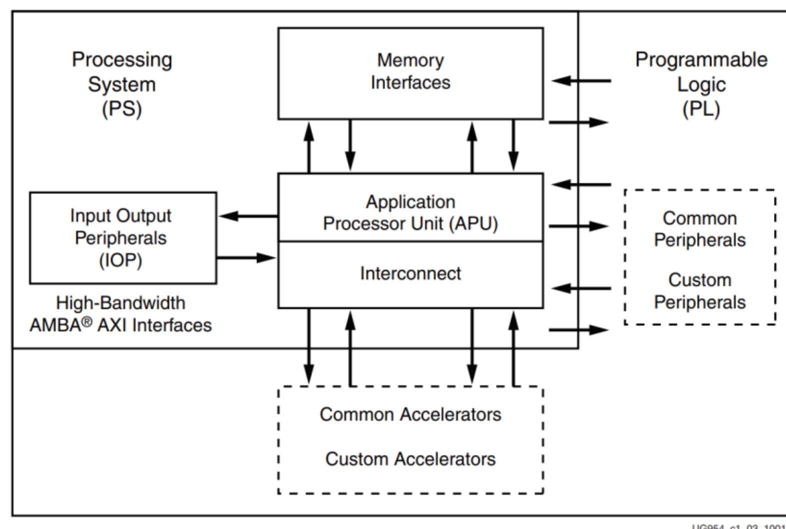


Figure 7.1 High level block diagram. Figure from [27].

(FMC) attached to the low pin count (LPC) FMC and high pin count (HPC) FMC connectors.

The XC7Z045 SoC includes an integrated processing system (PS) and programmable logic (PL) on a single die [92]. The top-level block diagram is shown in figure 7.1. The dedicated firmware customized for the chip should be designed at the FPGA side of the PL, and the controlling software should be compiled in the Application Processor Unit (APU) part of PS, which works like the typical file management functions of Linux. The communication between the ARM processor (APU of the ZC706) and the FPGA is performed using the AXI protocol. This is a data flow handler that offers several end-to-end stream pipes for the data transport of the applications. The AXI protocol is an interface of PetaLinux, which serves as a data transmission channel between the PS and the PL.

7.2 The embedded operating system of PetaLinux

PetaLinux [28] is an embedded Linux Software Development Kit (SDK) targeting FPGA-based system-on-a-chip (SoC) designs. It is a Linux distribution dedicated to ZedBoard or SoC Kit boards with Graphical User Interface (GUI). Also, it enables the peripheral management of the development board for an easy connection of devices through Ethernet, USB, and HDMI ports.

PetaLinux Reference Board Support Package (BSP) files are reference designs that automate many of the tasks required to boot and operate embedded Linux SoC. Besides, these designs can be used as a basis for creating new projects. PetaLinux BSP's are provided in installable BSP files and include all necessary design and configuration files required to start developing systems. Pre-built hardware and software images included in the BSP package are ready for download to the ZC706 board. This work is derived from the BSP by customizing IP blocks dedicated to the configuration of the TaichuPix1 to simplify the design procedure.

7.3 Pixel cell configuration

In order to debug the pixels one by one, every pixel has a MASK_EN and PULSE_EN latch (shown in figure 7.2). The latches, which can be set from the control interface, determine the pixel behavior. Both the PULSE_EN and the MASK_EN require their respective enable pins to be asserted to latch the data input. Each pixel is individually selectable, allowing the configuration of complex

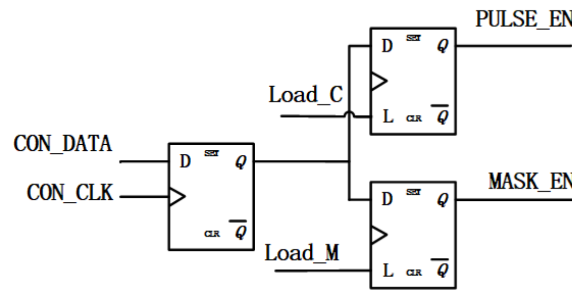


Figure 7.2 Schematic of the in-pixel latch.

patterns. The two latches share a common data select register, and only one can be selected at a time, thus for the chip calibration, it needs to configure twice, one for PULSE_EN, the other for the MASK_EN. The default state of PULSE_EN and MASK_EN should be set to low. Load_C/M can be generated by the internal configuration signals or from the external signal source. A 1-bit shifting chain controls the chip for each double column. To this long 1-bit register chain, the input data was configured to start from top to bottom, and the clock signal flowed in the opposite direction to induce the effect of the gate delay. The internal registers control both the input data and the clock.

7.4 Periphery readout configuration interface

The Serial Peripheral Interface（SPI) interface is used to write or read the internal control or status registers. A timing diagram is given in figure 7.3. The W/R bit in the 16-bit packet is used to define a write operation or a read operation ('0' means to write, '1' means to read) of the current packet. The A4-A0 bits define the address of the target register to be operated on. DI7-DI0 are the 8 bits data to be written in the control register during a write operation, and the DO7-DO0 are the 8 bits data returned to the SPI master during the read operation. All logic and registers in the SPI module will be reset when the SPI_CSB is set to 1. The control and status registers are kept as long as the power supply is maintained. The interface reset is released as soon as SPI_CSB is set to 0. SPI_CSB should keep low for the whole packet transmission period. With SPI_CSB=0, the first bit that is considered has to be logic 1. All incoming bits with a logic 0 that arrive prior the logic 1 are ignored. And the first bit at logic 1 is part of the first packet (first bit of 16 bits packet) and acts as a synchronization bit. Once the data is synchronized, the SPI interface keeps tracking the packet positions using a clock counter. Each group of 16 clock cycles

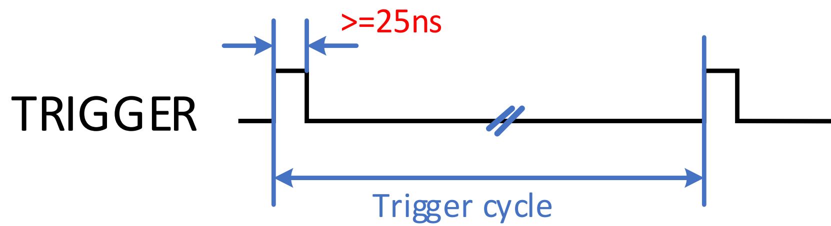


Figure 7.6 Timing of input signal TRIGGER.

Figure 7.3 Timing of SPI interface, it takes from Xiaomin Wei in TaichuPix1 user manual.

defines a new packet. The following packets are not re-synchronized and solely rely on the initial alignment. By checking SPI_MISO, the host can verify if the synchronization is still valid, starting with a pattern of 3-bit 1 followed by 4-bit 0 for each packet.

7.5 Data format and serializer

The output data (DATA_OUT [31:0]) from the periphery readout is defined in the following format (see figure 7.4): DATA_OUT [31] is the data available flag ('1' means data valid; '0' means data invalid). DATA_OUT [30:23] is the 8 bits timestamp, DATA_OUT [22:14] is the address of the double column. DATA_OUT [13:4] is the hit pixel row address in a double column, finally, the last 4 bits DATA_OUT [3:0] is the data compression pattern.

Figure 7.4 The output data DATA_OUT format.

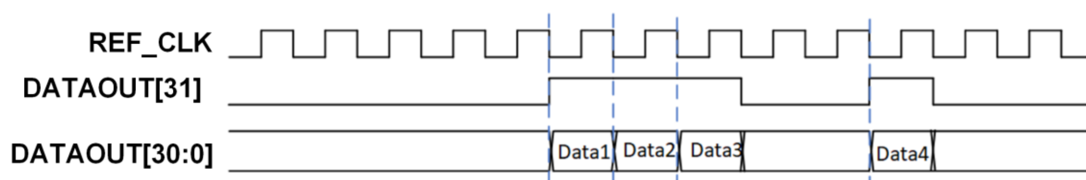


Figure 7.5 Timing of output data from the periphery.

The timing of output data from the periphery is shown in figure 7.5. The output data DATA_OUT is sent at the falling edge of REF_CLK. In the triggerless mode, the output frequency is 160 MHz/80 MHz. The external trigger start signal (as shown in figure 7.6) is synchronized (Trigger_syn) in the trigger mode by CLK_40MHz. The output data frequency is set by 2 bits register of DOFREQ [1:0]. The average cycle of TRIGGER is 20 μs. The pulse width of TRIGGER is larger than a clock cycle (25 ns). TRIGGER is synchronized to Trigger_syn with the positive edge of CLK. The TRIGGER arriving time is recorded at the positive edge of Trigger_syn.

In the TaichuPix1, a high-speed data interface is integrated to serially transmit the parallel data (DATA_OUT [31:0]) generated from the pixel array periphery readout. The total data rate is up to 3 Gbps in triggerless mode and 160 Mbps in trigger mode. The high-speed readout data is serially transmitted through the output data interface. A common high-speed data interface usually contains an encoder and a serializer. The function of the encoder is to encode the data for high-speed transmission and make the data logic DC-balanced, while the function of the

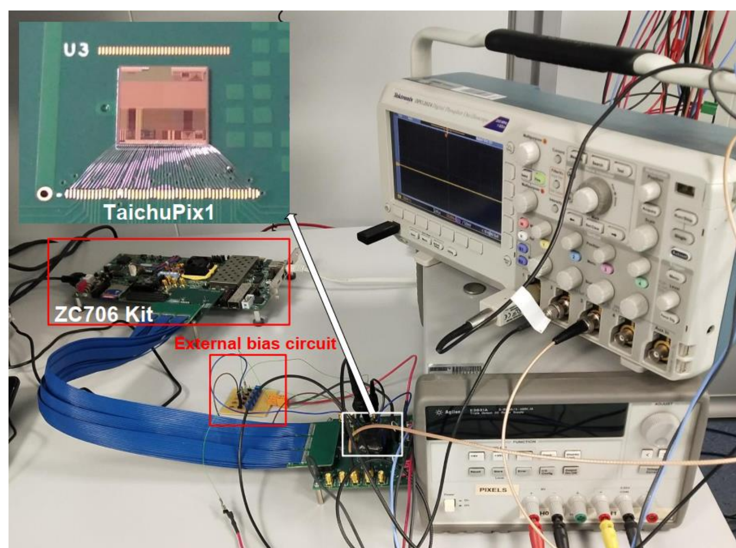


Figure 7.7 Test Platform for TaichuPix1

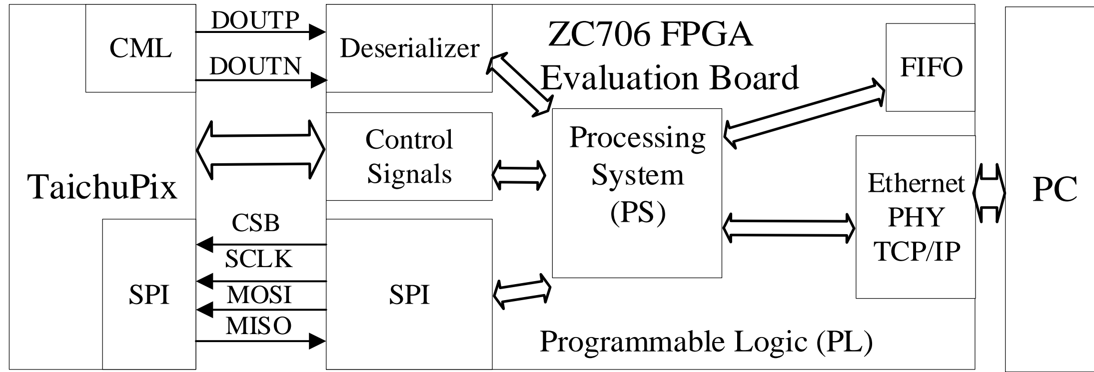


Figure 7.8 Setup system diagram based on ZC706 for TaichuPix1.

serializer is to serialize the parallel data from the pixel array and transmit the serial data out of the chip by single-end or differential pair. A serializer usually comprises three important parts: a phase-locked loop (PLL), a multiplexer, and a current mode logic (CML) driver.

7.6 Test platform designed for TaichuPix1

The test platform for the TaichuPix1 (shown in figure 7.7) includes a dedicated board where the device is wire bonded, a Xilinx ZC706 FPGA evaluation board, an adapter board with an FMC connector, an oscilloscope (Tektronix DPO 2024, 200 MHz, 1 GS/s), a DC power supply (Agilent E3631A, 6V/5A & ±25V/1A) and a PC. The ZC706 evaluation board is the main module to configure and communicate with the chip and transmit the readout data from the chip to the PC. In order to provide enough power to the chip, the TaichuPix1 is powered directly from an external DC power supply.

7.7 Firmware designed for TaichuPix1

The ZC706 evaluation board is the main module to configure the chip and transmit the readout data from the chip to the PC. As it is shown in figure 7.8, for the

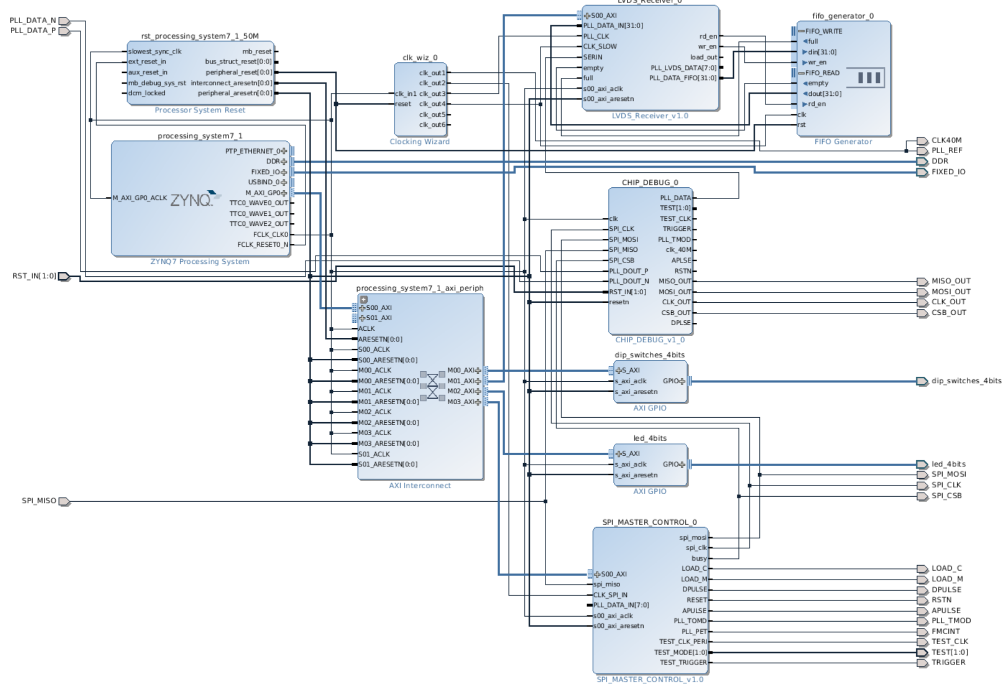
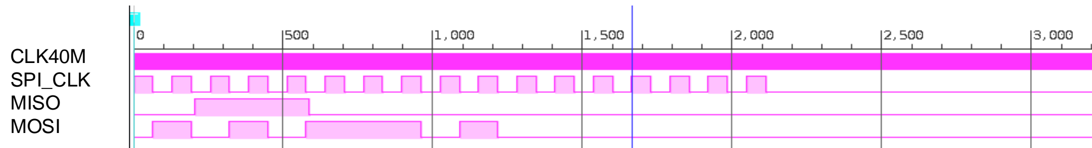
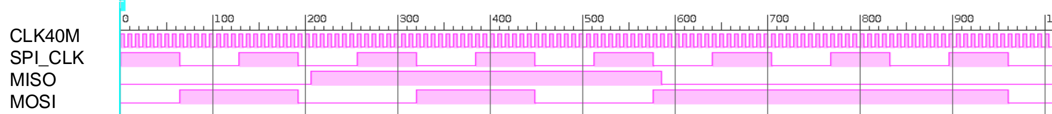


Figure 7.9 Setup system diagram based on ZC706 for TaichuPix1.



(a)



(b)

Figure 7.10 SPI interface waveforms zoon out (a) and zoom in(b) obtained from ILA core of Vivado.

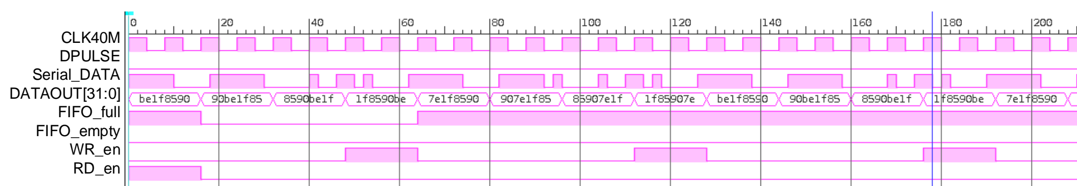


Figure 7.11 Serializer output timing obtained from ILA core.

firmware design, the system on the chip launches an SPI interface to communicate with the TaichuPix1 and deserializes all the data stores in an FPGA FIFO first, then sends all the data to the PC via Ethernet port. In this work, the main clock of the chip is set to 40 MHz, the speed of SPI is 10 MHz, and the frequency of the LVDS interface is set to 160 MHz.

Figure 7.9 shows the firmware blocks designed by Vivado, and it includes several necessary blocks for the basic configuration of the ARM processor. Besides, some customized blocks are designed as well. Like the SPI_MASTER_CONTROL, which is the main block to configure the TaichuPix1. This block generates an SPI interface, which can be read or written by the processing system (PS). The output of this block connects to the chip with some critical controlling signals. Figure 7.10 plots the timing of the SPI interface captured by the Integrated Logic Analyzer (ILA) core [93]. A CHIP_DEBUG block is designed to check the status of each internal signal. An LVDS data receiver block, together with a FIFO generator, is also designed to deserialize the data from the chip. The serial data acquisition timing from ILA is shown in figure 7.11. The different operating clocks are separated from one synchronized clock by the Clocking Wizard Intelligent Property (IP).

7.8 Software programming for TaichuPix1

After implementing the firmware in the FPGA, the next step is to build the PetaLinux system file and map the address with the user-defined blocks. For this test platform, all of the configuration files have been integrated into an SD card. The boot image (see BOOT.BIN in figure 7.12) usually contains a PDI (Platform

Name	Size
BOOT.BIN	13.7 MB
image.elf	11.2 MB
image.ub	7.7 MB
system.dtb	15.6 kB
System.map.linux	1.8 MB
u-boot.elf	1.6 MB
u-boot-s.bin	274.4 kB
zImage	7.7 MB
zynq_fsbl.elf	262.0 kB

Figure 7.12 Boot files to SD card for TaichuPix1

Device Image) file that is imported from hardware design, PLM (Platform Loader and Manager), PSM (PS Management) firmware, ARM trusted firmware, U-Boot, and DTB (Device Tree Blob). These files for the TaichuPix1 are listed in figure 7.12.

After the SD card boots in the ZC706 kit, it will start the board and load the firmware to the PL. Then the ZC706 kit turns to be an MCU (Microcontroller Unit) that includes several user-defined periphery blocks and runs on an ARM processor. The rest of the software has been developed and compiled with the SDK (Software Development Kit). Once the firmware is working correctly, the next step is to do the software programming and keep the firmware.

As mentioned already, each pixel could be selected and configured by a one-bit shifting register chain. Table 7.1 lists several register descriptions for pixel masking and data debugging. Figure 7.13 describes the flow diagram of the pixels masking and data readout in debug mode. For pixel masking, register "00110" is used to load the different level status to every pixel. And the register "00111" is used to latch the value into each pixel. After the pixels are configured, some of the pixels will be turned on, and some will be turned off. By injecting APULSE or DPULSE, from the data output of FIFO2, the region of the selected pixels can be used to verify the function of the architecture (by simulating the response to an impinging particle). Only when the data read out from the FIFO2 is the same as the pulse injected region the chip has been initialized correctly. The configuration

Table 7.1 Register description of TaichuPix1 debug

Bit range	Signal name	Reg. add.	Description
DB [7:0]	Pixelmask_data	00110	Configuration data for pixel mask or calibration
DB7	Loadc_e	00111	1'b0 -> disable the load_c_internal generation 1'b1 -> enable the load_c_internal
DB6	Loadm_e	00111	1'b0 -> disable the load_c_internal generation 1'b1 -> enable the load_c_internal
DB [5:0]	---	00111	---
DB [7:0]	FIFO2_READ	11010	This index is occupid by FIFO2 read command when TEST=11; unused when TEST !=11, default:0000 0000
DB [7:0]	FIFO2_DATA	11011	This index is occupid by FIFO2 data shift out command when TEST=11; unused when TEST !=11, default:0000 0000

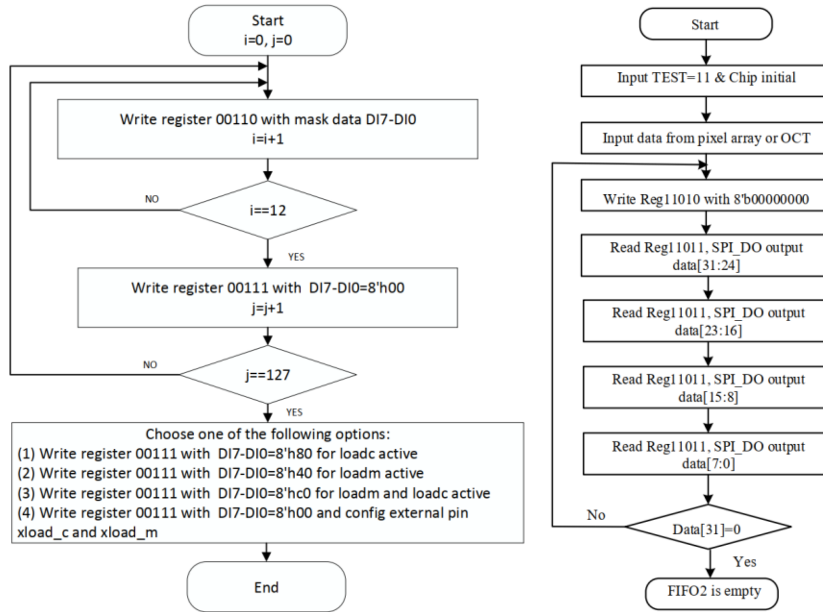


Figure 7.13 Pixel masking flow diagram(left side) and data debug(right side) for TaichuPix1.

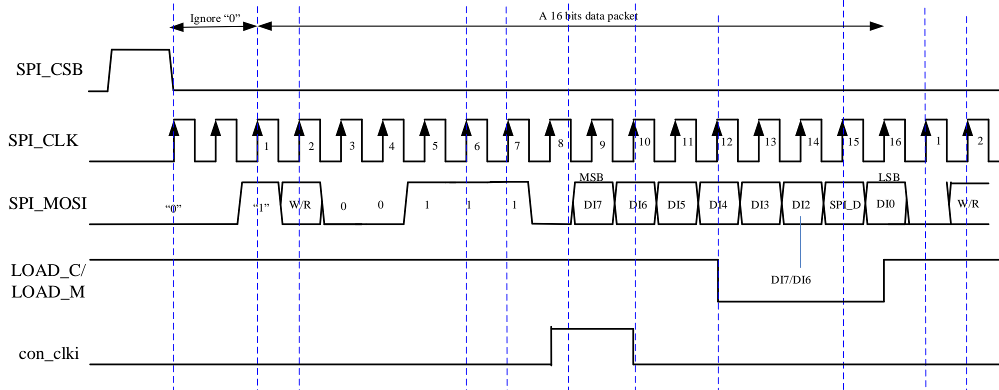


Figure 7.14 Waveforms for pixel masking configuration.

timing diagram of pixel masking is drawn in figure 7.14. Loading data from the shifting register chain to each pixel is done by the SPI interface. The configuration clock is divided by the SPI_CLK, and the signal Load_C /Load_M should be set to be logic "0" while the data loading and the value will be latched to each pixel when it goes to logic "1".

The controlling terminal is designed on the PC, which is based on a TCP/IP protocol, where the PC is set as a client while the ZC706 kit operates as a server. Before sending a command to the ZC706 kit, there will be a process for the server to create a socket and listen for connections on a well-known port number. Then the client would also create a socket and connect to the server address at the same port number. After the connection is successfully established, the PC can send write

and read instructions to the PS and modify the status of registers inside the TaichuPix1 chip.

Summary

The test platform designed for TaichuPix1 is based on the Xilinx FPGA ZC706 Kit. It consists of an integrated processing system (PS) and programmable logic (PL) on a single die. The user-defined firmware blocks have been implemented into the PL, to achieve communication with the PS via the AXI bus. The SDK was used to develop the software design, and the design environment is based on the embedded operating system PetaLinux.

Before characterizing the TaichuPix1 chip, it is critical to verify the initialization of the chip. The chip has a one-bit shifting register chain to configure every pixel on the whole matrix. A debug core was designed into the TaichuPix1 so that the data from FIFO2 can be read out directly, and this is an efficient way to check the output status of the pixel cell.

Chapter 8

Characterization of the TaichuPix Chip

This chapter describes the characterization of the TaichuPix1 chip in detail. It is a fully functional verification with a radioactive source, which tests all the components of the chip, including the analog front-end, the in-matrix digital readout logic, and the periphery circuitry. A setup to test the chip on the trigger mode using a scintillator is presented in section 8.2. In addition, the limitations of TaichuPix1 are discussed in section 8.3. Some improvements of the second prototype, TaichuPix2, and the preliminary laser test are shown in the rest of the sections.

8.1 Fully functional characterization with a radioactive source

As mentioned above, the main architecture of TaichuPix1 includes several blocks. The ^{90}Sr radiation imaging test is an effective method to verify the whole functionary of the chip. ^{90}Sr is a radioactive isotope of strontium produced by nuclear fission, with a half-life of 28.8 years. It undergoes β decay into yttrium-90, which in turn decays according to [94]:

$$^{90}\mathrm{Sr} \rightarrow {}^{90}\mathrm{Y} + e^- + \bar{\nu}_e \quad (8.1)$$

$$^{90}\mathrm{Y} \rightarrow {}^{90}\mathrm{Zr} + e^- + \bar{\nu}_e \quad (8.2)$$

The second reaction ends with the stable isotope ^{90}Zr of 68 hours half-life. Both of β decays result in the electron energy being within a continuous spectrum. The first decay is usually stopped before the detector (0.546 MeV electrons), while

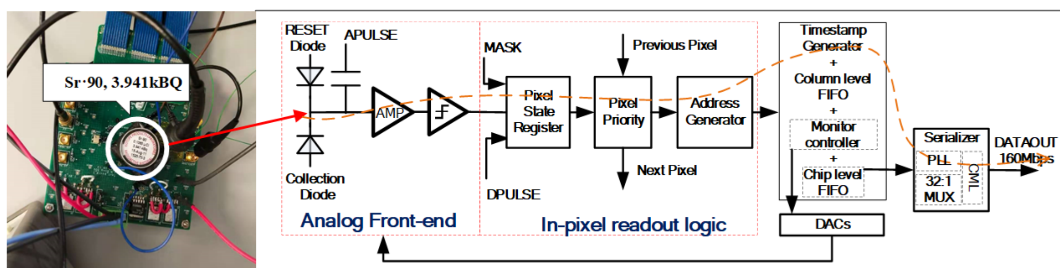


Figure 8.1 Signal flow of the TaichuPix1 under ^{90}Sr exposure.

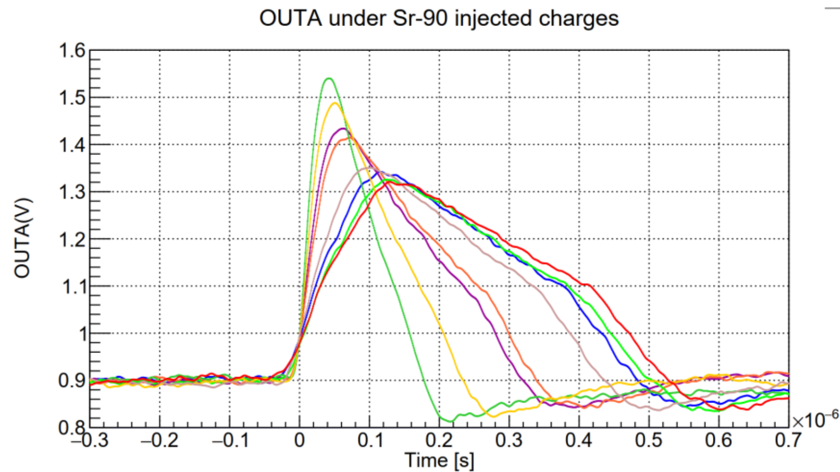


Figure 8.2 Analog front end output from oscilloscope under ^{90}Sr exposure.

the second one has maximum electron energy of 2.280 MeV, which is enough to travel through a typical 500 µm thick silicon sensor (effectively acting like a minimum ionizing particle).

As depicted in figure 8.1, the ^{90}Sr (3.941kBQ, 15-Aug-2011) radioactive source is placed on top of the chip, with a distance between the chip and source of around 1 cm. The analog front end is configured to a proper value by the on-chip DACs with the external bias reference, using the parameter setup Settings-2 in table 4.1. The source is placed over the chip, while the analog output of one of the pixels is monitored. The results are shown in figure 8.2. Since the time of arrival of the electrons into the chip is not known, the waveforms are used to qualitatively prove that the analog front-end is sensitive to the injected charges.

Only half of the pixels are turned on in this setting, the ones corresponding to the FEI3-like in-matrix readout logic. This has already been discussed in chapter 3, the digital periphery implements two different methods to process data (the FEI3 and the ALPIDE). Since it was explained before, the FEI3 is used in this thesis to make the measurements presented in this section. In addition to verifying the analog front-end of the FEI3-like matrix, the status of the in-matrix digital logic and periphery circuitry has also been tested. The debug mode was turned on to read out the data inside FIFO2 and a hit map, which is shown in figure 8.3, was obtained. The hit map proves that the main readout architecture of TaichuPix1 is working properly. The in-matrix readout logic works fine when the system clock runs at 40 MHz, and the periphery can encode the data and transmit it to the output interface.

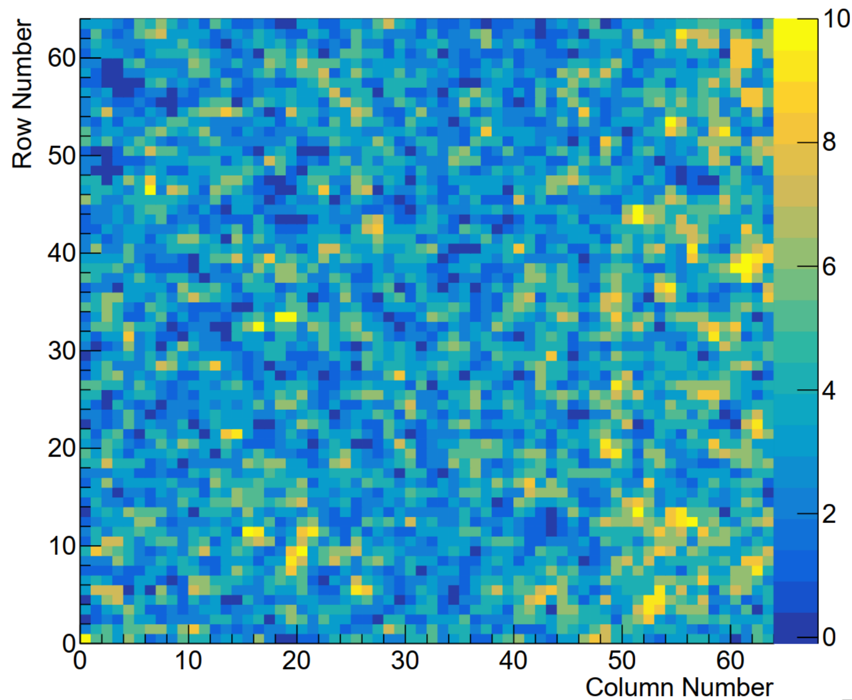
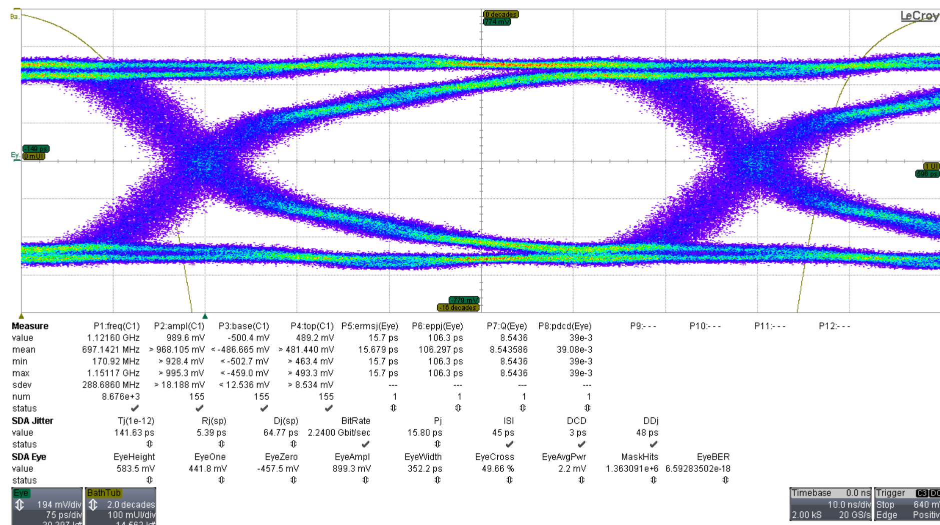


Figure 8.3 Hit map under ^{90}Sr exposure in debug mode.

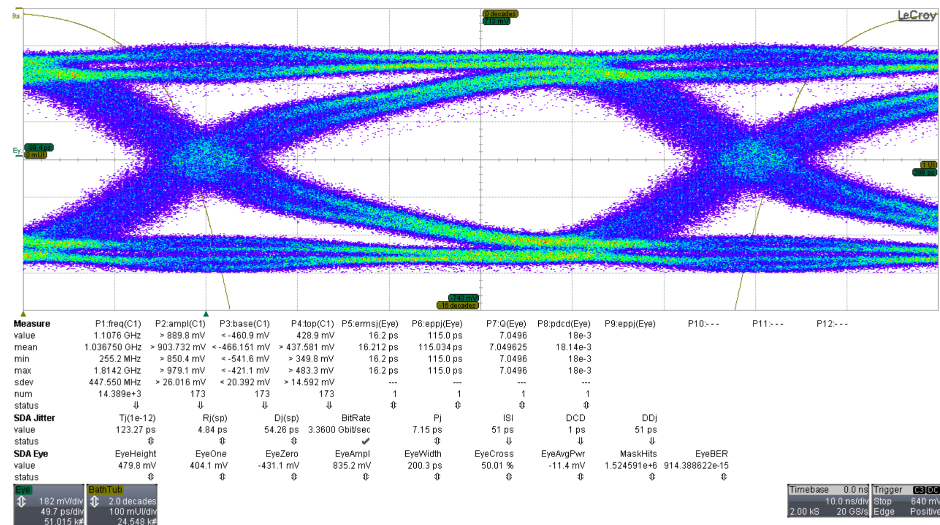
The serializer was also tested. The serializer is composed of a ring-oscillating PLL, a 32:1 multiplexer, and a CML driver. The system reference clock runs at 40 MHz. The measured frequency locking range of the PLL is from 320 MHz to 2.68 GHz. The highest average data rate of the detector is 3.84 Gbps, which agrees with the stringent average hit rate of the W boson in triggerless mode. The preliminary self-tests using an internal PRBS-27 (Pseudo-Random Binary Sequence) [95] generator as the data source of the serializer show that it is difficult for the system to work at about 4 Gbps due to limitations of the technology and the driving capability, but it can work up to 3 Gbps (see figure 8.4). Each pixel provides a 32-bit word in the following format (see figure 7.4). It has 1-bit data available flag ("1" means data valid, "0" means data invalid), 8 bits timestamp, 19 bits pixel address information, and 4 bits data compression pattern. A reference pattern of data has to be added to the data output to decode it. Otherwise, it is difficult to synchronize the data as it only relies on the 1-bit data available flag.

Figure 8.5 shows a hit map of the device exposed to the radioactive source for 12 hours, taking the data from the serializer. As already mentioned, the measurement corresponds to the FEI3-like part of the chip. The device is working in the triggerless mode, and the measurement setup is based on figure 8.1. For this basic electronics testing, the speed of the interface is set at 160 Mbps. The matrices

are divided into 3 fast readout groups with 64 columns in each group (the total number of columns is 192, half of them implement the FEI3-like scheme). In figure 8.5 it can be observed that columns 64 to 95 have a higher probability of detecting signals. According to the peripheral readout approach designed in the chip, as discussed in chapter 6, only one data group can be read out when hits arrive. Since group-2 is a mixed group with half ALPIDE-like-scheme, which noisy pixels cannot be masked, group-2 will always get a hit from the ALPIDE-like part and readout with a higher priority. On the one hand, only part of the events can be read out when too many hits arrive simultaneously, and later hits will be lost. On the other hand, the triggerless mode is used to record any hit above the threshold. Thus, it will



(a)



(b)

Figure 8.4 Eye diagrams of PLL at self-test mode with the speed of 2.24 GHz(a) and 3.36 GHz(b).

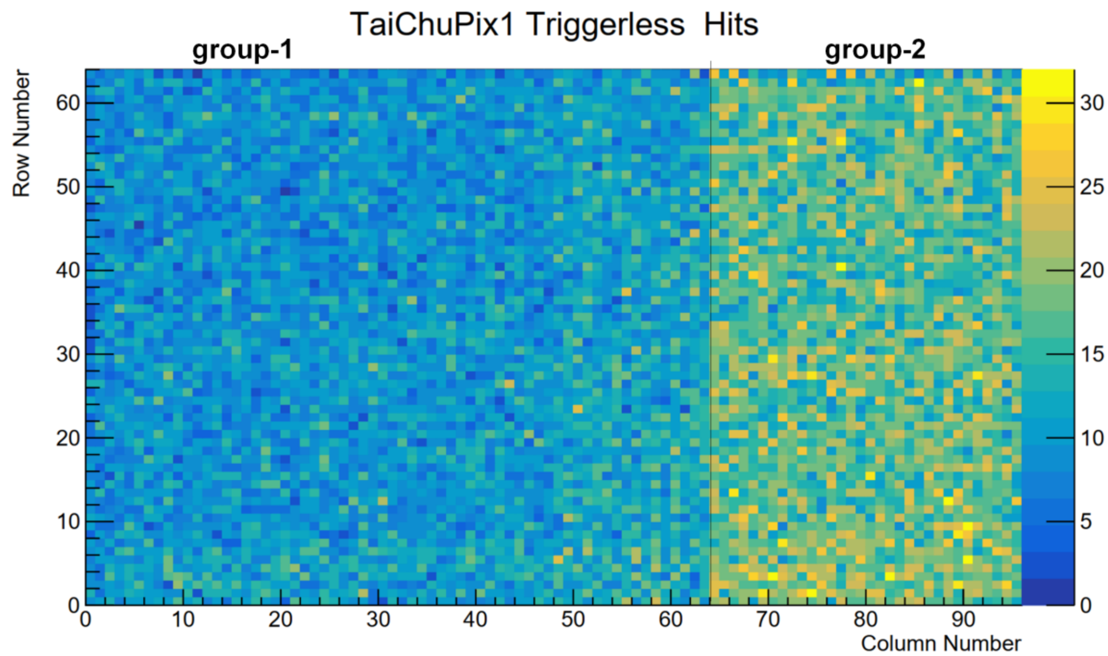


Figure 8.5 Hit map under ^{90}Sr exposure in triggerless mode.

record invalid data (due to hot pixels), which saturates the readout resources, resulting in the ^{90}Sr events being lost. After removing the noisy pixels, this leads to a relatively low event count (lower than 40 per pixel) even for 12 hours of exposure to the ^{90}Sr source.

8.2 Trigger mode with a scintillator setup

Besides the triggerless mode, the operation of the TaichuPix1 also has been verified in trigger mode using a scintillator coupled to a photomultiplier (PMT) to provide the external triggers. The TaichuPix1 is placed between the scintillator and the ^{90}Sr source, as illustrated in figure 8.6. A high voltage supply powers up the PMT to -900 V. The signal of the scintillator-PMT is connected to a discriminator board with a NIM (Nuclear Instrument Modules) level output. A level adapter board is used to covert the NIM signal to TTL (Transistor-Transistor Logic), which is used for triggering the readout system. The ^{90}Sr beta electrons travel through the chip and reaches the scintillator. The chip is operated in trigger mode with a latency of 3 μs. The uncertain data window is set to 175 ns, which can read out trigger data with the error range of 7 timestamps. The serializer is operating at 160 Mbps as well. In trigger mode, there are four different data rates can be selected with the peripheral

readout logic. In addition to the default 5 MHz data rate, 2 MHz, 10 MHz, and 20

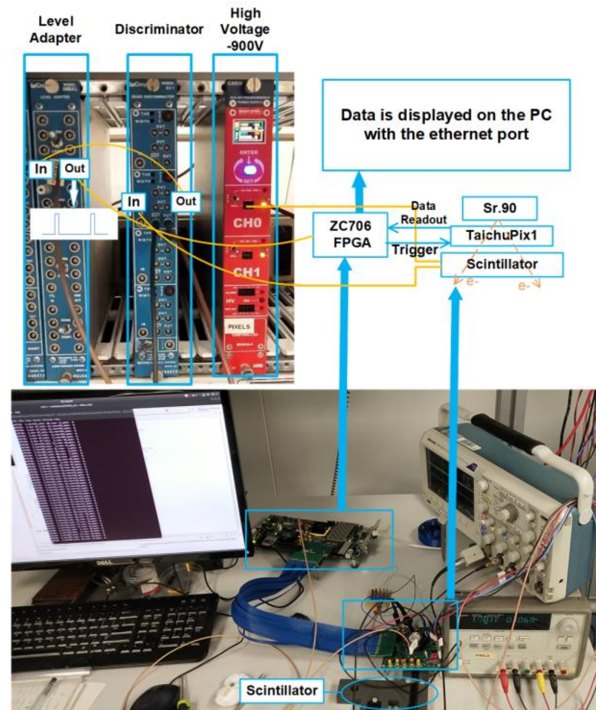


Figure 8.6 Trigger setup with the scintillator

MHz are available. For this measurement, the 160 Mbps serial interface was matched with a 5 MHz data rate.

Using the trigger settings above, a hit map with a scale of about 100 hits per pixel is obtained (see figure 8.7(a)). The higher number of hits in sector 2 is due to the threshold difference between sector 1 and sector 2. The pixels at the left and top sides of the matrix have a lower hit rate. This is due to the fact that these pixels have less neighbors than the other ones. The pixels at the right and bottom side have dummy pixels that recover their performance. In addition, the cluster size can be analyzed with the information of the timestamps and the hit addresses. The cluster distributions under the exposure to ^{90}Sr of these two sectors are shown in figure 8.7(b). Each sector equally calculates 16 columns. From the histogram result, it can be observed that, as expected, a lower threshold leads to a larger cluster size. The average cluster size of sector_3μm_spacing (sector 1) is around 2.43, while this value for sector_2μm_spacing (sector 2) is 2.99.

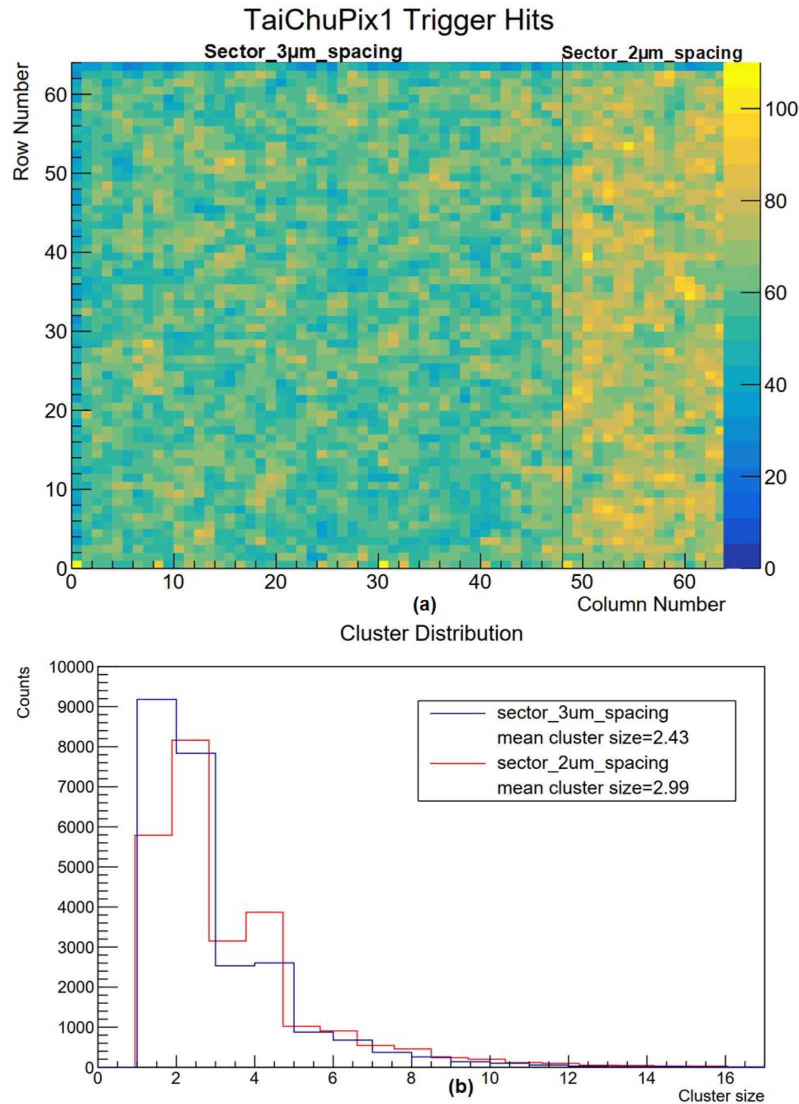


Figure 8.7 Trigger mode hit map(a) and cluster distribution(b).

8.3 Limitations of TaichuPix1

As discussed in chapter 4, the device threshold is limited by the sensor reversing bias. The PWELL connects to 0 V, which allows a threshold roughly of 300 e^-. Besides, the band-gap reference circuit designed for the DACs is not as good as expected, so the bias to the analog front-end does not allow to set all the chip parameters correctly. One possible solution, as described above, is to use the external reference voltage. The experimental results presented in the previous sections indicate that it is feasible to operate the analog front-end in a normal condition in this method.

The power consumption is another limitation of this prototype since the chip

operates with the same principle of the ALPIDE architecture, but with a faster timing performance, at the expense of increasing the power consumption (~200 mW/cm^2 while for the ALPIDE chip is around 35 mW/cm^2 [40]). In addition, the in-matrix readout logic also increases the power consumption. Since the TaichuPix1 is based on a column drain readout architecture, the data bus is critical to driving the circuitry at the end of the column. In order to fit the in-matrix readout logic into the pixel size of 25×25 μm^2, a pull-up and pull-down network matrix was used to encode the index information of each pixel. The output of this encoder may be an uncertain status when no hit arrives at the pixel, which is a high-impedance state condition. This can lead to an increase the power consumption of the digital circuitry. As shown in figure 8.8, if no signal lasts for a long time (~1 ms), the in-matrix readout logic quiescent current of a double column of pixels would soar from the initial 36 nA to 81.2 μA. To the digital logic, the static power consumption should be negligible while no pixel is firing. The high-impedance state may cause some issues on periphery data readout. As it is presented in figure 8.9, the whole matrix is divided into three groups evenly. GROUP3 has the top readout priority. GROUP1 and GROUP2 can be read out with the same priority in parallel. Following the fast readout approach of 32 DCOL, when all of the matrices receive hits, only one of the groups between GROUP1 and GROUP2 can be read out. The right-side column has a higher priority. As already mentioned, the left half is based on FEI3-like digital logic, and the right half is based on the ALPIDE-like pixel flavor. The GROUP2 in figure 8.9 is a mixed group with both in-matrix digital logics. Both schemes share the same readout timing in the digital peripheral readout circuitry. Due to the high-impedance state that existed in the ALPIDE-like scheme data bus, only the higher priority columns can be read out correctly inside the ALPIDE-like matrix. Since the readout timing of ALPIDE-like scheme is different from the FEI3-like one, a possible solution may be to design an individual readout timing for the ALPIDE-like scheme.

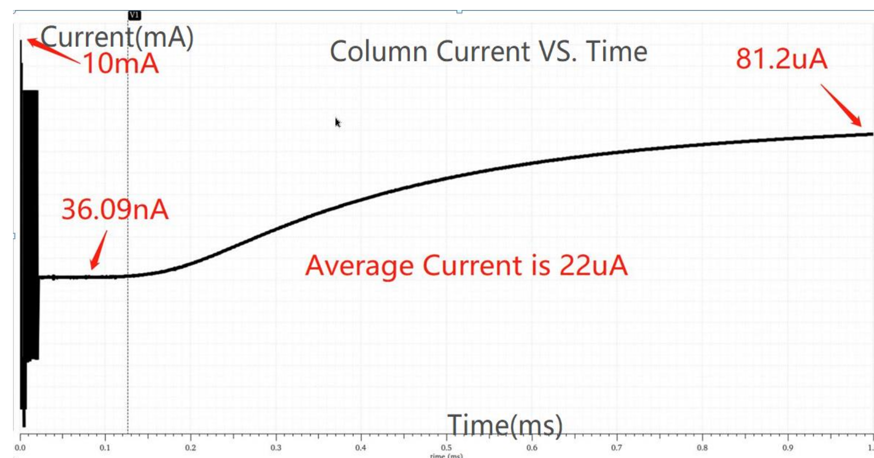


Figure 8.8 The quiescent current of one double column in TaichuPix1.

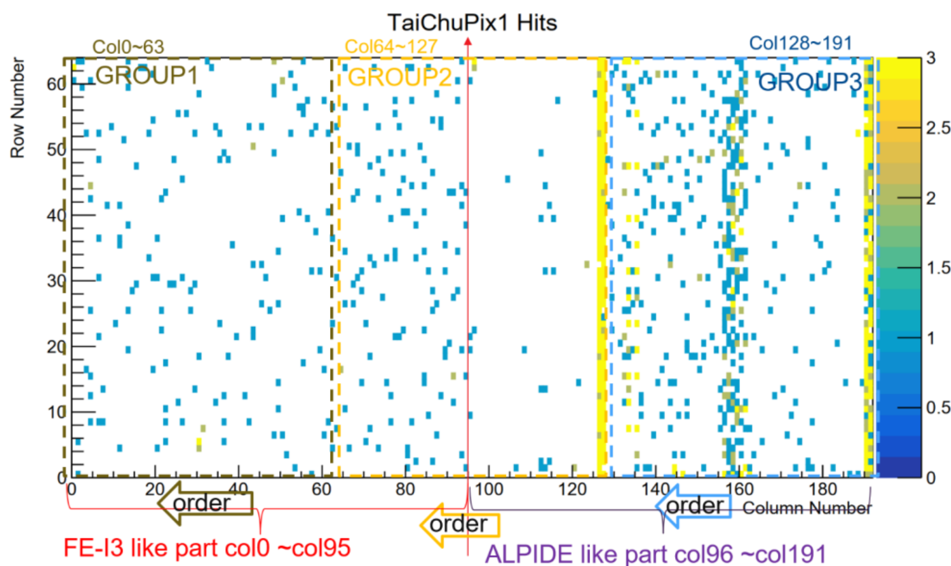


Figure 8.9 Hit map of the full matrix under ^{90}Sr exposure.

8.4 Improvements of TaichuPix2

The TaichuPix2 chip aims to remove the power errors found in the measurement of the TaichuPix1 and improve the performance indicators of some parameters of the chip, making it closer to the ultimate prototype. Below, the band-gap issue, the high impedance problem, and the high-power consumption of the chip are addressed.

From the experience of the TaichuPix1, a new band-gap reference voltage has been implemented in the TaichuPix2, to provide adequate voltage and current to the analog front-end.

As for the high-impedance state issue in the in-matrix readout logic, a state latch was designed at the end of the column. As shown in figure 8.10, the metal line length of one column with 512 rows is around 12.8 mm. The estimated loads in this technology are R=3.68 kΩ resistance and C=3.2 pF capacitance for a 12.8 mm metal line. The propagation delay (Td) is simply estimated as Td = 0.7×RC, where the delay is around 8.24 ns without any buffers. In order to optimize the delay of one column, the metal line is divided into 8 segments evenly. A buffer was inserted into each segment with a total delay of about 3.33 ns. Besides, a buffer can also enhance the drive strength of the signals. A pull-up transistor is implemented at the end of the column when no hits arrive at the pixel. The FASTOR keeps to be a state of low, so the source of the pull-up PMOS keeps a state of high, then the uncertain status can be removed. In the other case, during the readout phase, the FASTOR goes to the state of high, then the PMOS will be switched off, the state of the source is the same as the data bus. For each data bus, only one pull-up PMOS transistor is used for the latch of state. The timing diagram with this new structure is illustrated in figure 8.11, and the 3 pixels address index of ADDR<6:0> are "0000010", "0000001" and "0000000". Compared to the timing of the TaichuPix1, the READ_latch has a 12.5 ns delay to READ, to guarantee the data sampling can be done correctly at the rising edge of the READ_latch signal. Figure 8.12 draws the current of one column. During the initialization phase, the instantaneous

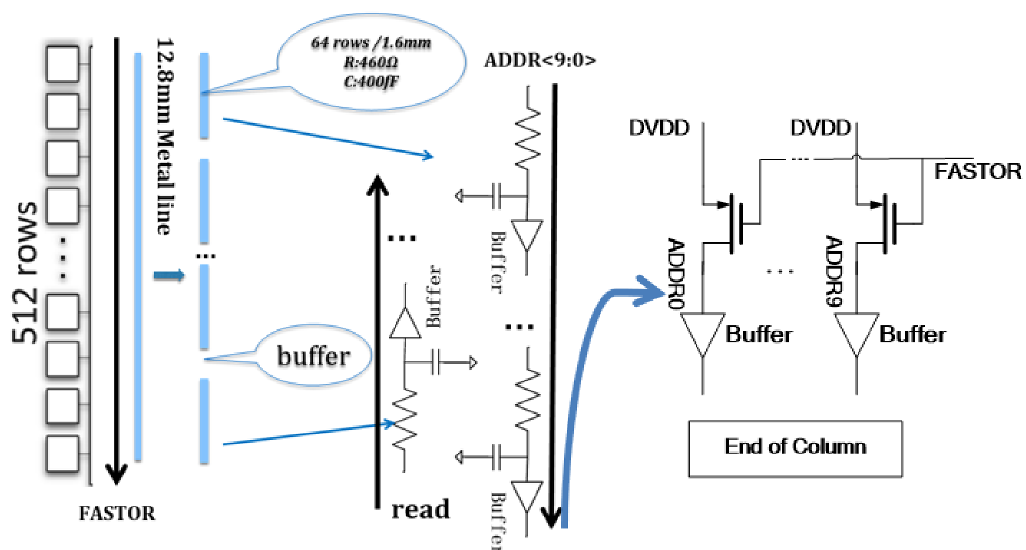


Figure 8.10 Pull-up transistors designed to each data bus

maximum current is about 10 mA. Still, after some time, the transient current of TaichuPix1 (see figure 8.8) would go up due to the high-impedance state, while the current of the TaichuPix2 will always remain stable with a low current level (around 32.5 nA). From the simulation results, the pull-up PMOS latch has played a key role in reducing the static power consumption of the chip.

The following table shows the power density comparison of a double column of these two prototypes. It is based on the schematic simulation where the chip operates in the initial and readout phases under the full array scale of 512 rows× 1024 columns. Simulation results of the static phase have been presented as well.

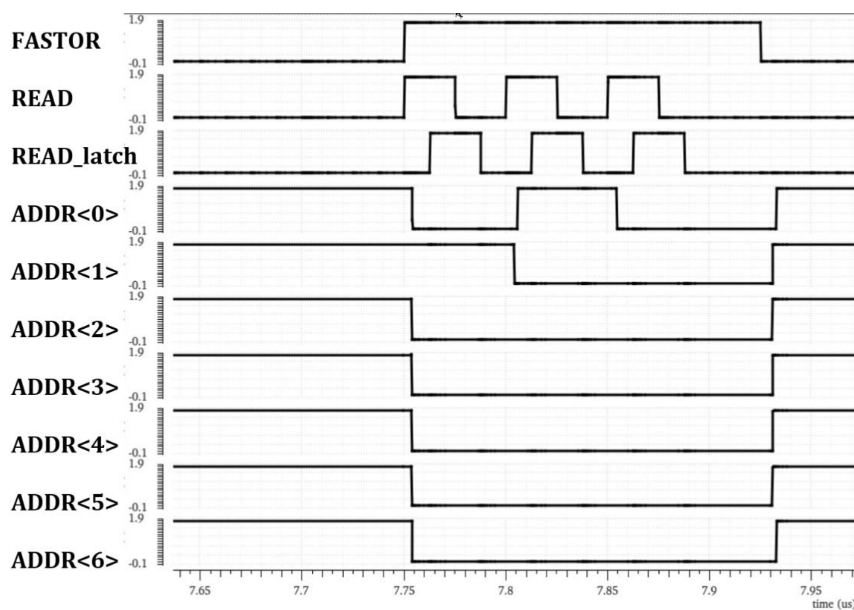


Figure 8.11 Timing diagram of post layout simulation with pull-up transistor.

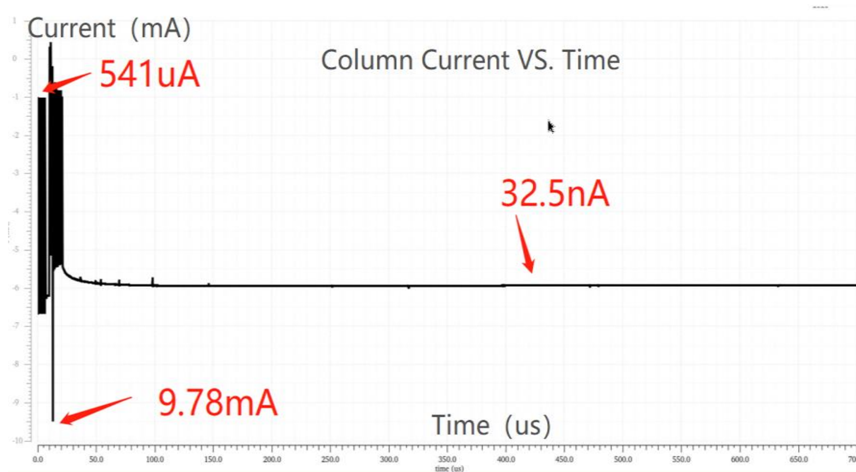


Figure 8.12 the quiescent current of one double column in TaichuPix2.

Table 8.1 Power density comparision of both prototypes

Average power of in-matrix readout logic	FE-I3 like scheme		ALPIDE like scheme	
	TaichuPix1	TaichuPix2	TaichuPix1	TaichuPix2
Initial phase	87 µA	161.37 µA	374 µA	211.13 µA
Readout phase	275.55 µA	271.52 µA	231.65 µA	353.08 µA
Static Phase	81.2 µA (max)	47.40 nA	155 µA(max)	3.43 µA
Average current	22.01 µA	8.79 µA	55.98 µA	12.85 µA
Readout power density	77.49 mW/cm^2	76.36 mW/cm^2	65 mW/cm^2	99.30 mW/cm^2
Average power density	6.15 mW/cm^2	2.46 mW/cm^2	15.73 mW/cm^2	3.61 mW/cm^2

For this evaluation, it is assumed that the average hit rate is 8.3 µs/hit/column, and the power consumption density of the entire chip is calculated based on this setting. Compared with the TaichuPix1 chip, the TaichuPix2 chip has been greatly improved in the static phase when there is no hit arrival, and the overall average power density has also been significantly improved. More tests for TaichuPix2 chips are still in progress, and the power consumption evaluation is also being carried out.

8.5 Physical implementation of TaichuPix2

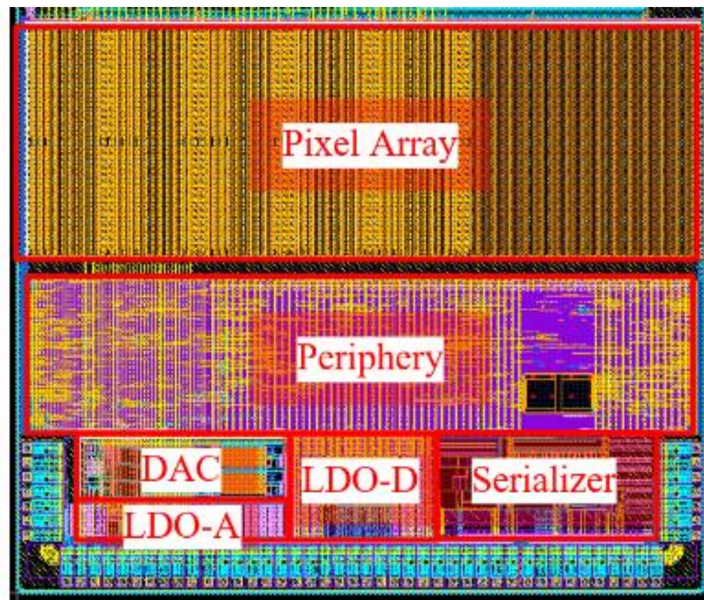


Figure 8.13 Overall layout of TaichuPix2

Figure 8.13 depicts the overall layout of the TaichuPix2 chip. This is also a small-

scale prototype with a matrix of 64 rows ×192 columns. The pixel size is the same as TaichuPix1 (25×25 μm^2). It is divided into two parts, pixel arrays, and periphery circuitry. The pixel array keeps the design of TaichuPix1, has two different pixel flavors with two different in-matrix digital logic schemes. It also includes several different sensor sizes, which are reflected on the analog front-end.

The digital readout periphery has three timing designs for the pixel array. It subdivided the whole matrix into 3 evenly groups, and each group has its delay parameters. The pixels of both group1 and group2 are based on the FEI3-like scheme, and group 3 is designed with an ALPIDE-like scheme.

The main difference with respect to the TaichuPix1 is the internal LDO (Low DropOut regulator) design. It is used to verify the feasibility of enhancing the strength of each chip's power supply while it is implemented to the vertex detector. The separation of analog and digital power is realized by placing two different LDOs on the bottom of the chip, LDO-A, and LDO-D.

8.6 Preliminary laser test of the TaichuPix2

Since the in-pixel electronics implementation of TaichuPix2 is almost the same as the TaichuPix1 described before, electronics characterization results will not be described here again. This section will show different experimental results based on a shifting laser. A laser setup from the IHEP (Beijing, China) group was used to characterize the TaichuPix2 (see figure 8.14). A basic data acquisition system is used to record the data and obtain the hit map.

The laser Transient Current Technique (TCT) [96] is a method used to measure the signal response (or waveforms) of silicon sensors through the deposition of photons in the particle sensing region by using a highly focused laser beam. The laser generates free charge carriers in the sensor. The transient signal from the drifting charge can be recorded and allows studies of the detector signal formation, charge collection, carrier drift velocity, and trapping mechanisms (after irradiation). The wavelengths used for testing silicon sensors are red (660 nm) and infrared (1064 nm) light. The results given in this study were obtained using the 1064 nm

infrared laser light. By shifting the laser in a specific direction, a hit map of the device being studied can be obtained. The step of the laser movement is around 200 μm in both X and Y directions. Figure 8.15 presents "CEPC" imaging results to prove that the TaichuPix2 is working properly. The sensing diode collects the charge carriers generated by the short laser pulse and the signal is amplified by the analog front-end. The in-matrix readout logic digitizes the signal. Then it will be encoded and processed by the peripheral readout circuitry, transmitted hits information to the serial interface.

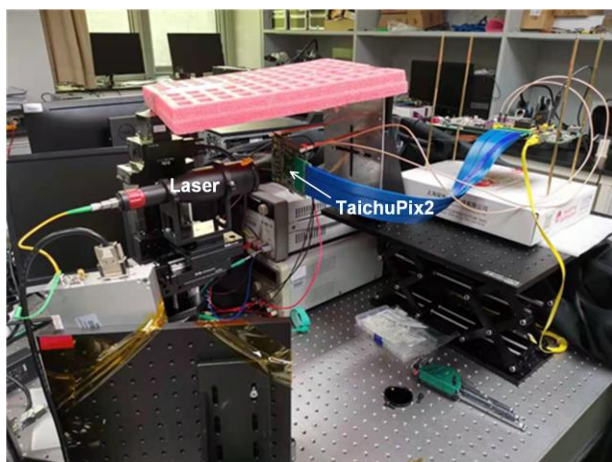


Figure 8.14 Laser setup of TaichuPix2

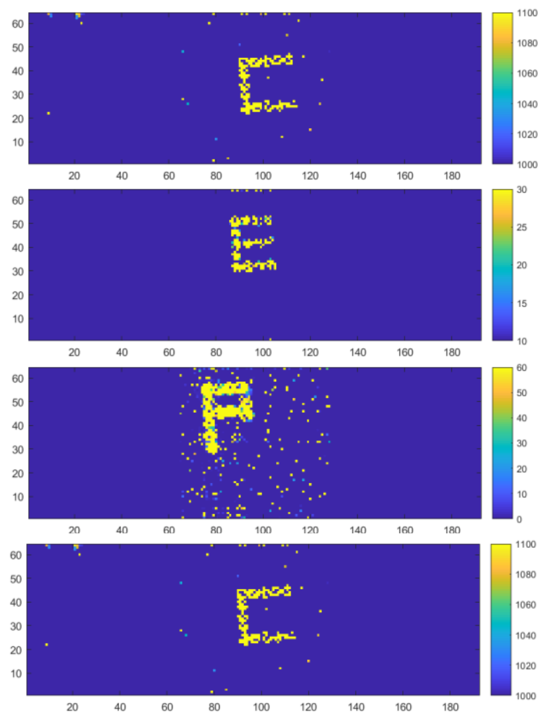


Figure 8.15 Character "CEPC" scan on the TaichuPix2

Summary

A fully functional monolithic pixel sensor prototype has been designed for the CEPC vertex detector. The TaichuPix1 is a small-scale prototype to verify the feasibility of implementing a pixel size of 25×25 μm^2, together with a column drain readout architecture. The results of the laboratory characterization using a radioactive source (^{90}Sr) have been discussed. The results prove that the analog front-end, the in-matrix digitization, the peripheral readout logic, and the serializer can correctly transmit the collected charges to the data interface. The trigger mode of the peripheral readout logic has also been verified, agreeing with the trigger data rate design. The TaichuPix1 builds on previous ASICs in some aspects (the FEI3 and ALPIDE for the readout schemes) but it implements a small pixel size and a fast readout speed. The full architecture was verified, and the results are valuable for implementing a full-scale prototype in the future.

This chapter also described some limitations of the TaichuPix1 and proposed some solutions to overcome the problems. A new prototype, the TaichuPix2, has been presented. Section 8.4 has focused on the enhancements implemented on the TaichuPix2. The main target of the TaichuPix2 is to improve power consumption. Compared to TaichuPix1, TaichuPix2 achieves a lower power consumption. At the same time, the charge collection and readout mechanism of the TaichuPix2 were verified, showing qualitatively that the sensor can successfully detect traversing charged particles.

Chapter 9

Summary and outlook

9.1 Summary

This dissertation presents and motivates the CEPC requirements for the vertex detector. It shows that the most promising solution is to use Monolithic Active Pixel Sensors (MAPS). It analyzes the current research status of monolithic pixel sensors at the domestic and international levels. It builds from the previous research experience to propose a dedicated fully functional pixel sensor chip, the TaichuPix1, that meets most of the needs of the CEPC vertex detector. It presents the design principles and simulation results of each part of the chip.

Furthermore, it shows the results of the electronics measurements and presents the tests performed using a radioactive beta source that verifies the full charge collection mechanism. The shortcomings and deficiencies of the chip are also discussed, and corresponding improvement methods are proposed. At the end of this dissertation, preliminary results of the improved second version of the small-scale chip, the TaichuPix2, are also presented. The two versions of the chip provide a valuable design experience for the next stage of the project, that is to fabricate a full-scale pixel sensor. It is expected that a baseline vertex detector prototype of the CEPC will be developed and tested in 2023.

In the context of this thesis, the TaichuPix1 has been designed and fabricated. The chip contains a pixel array of 192 columns and 64 rows with a pixel cell size of 25×25 μm^2. The features of the TaichuPix1 measured in this dissertation are summarized below:

Firstly, the in-pixel analog front-end circuit has a fast-rising time and a short time walk. The simulation results show that at the threshold of 182 e^-, the time walk is below 25 ns, corresponding to the injected charge from 400 e^- to 3000 e^-. And for a higher threshold of 300 e^-, this value is around 33 ns. Using the charge injection mechanism of the TaichuPix1, the measured peaking time is below 400 ns for a charge over ~100 e^-; for comparison, in the case of the ALPIDE chip, this value is about 2 µs. The time walk is around 57 ns at the threshold of 300 e^-, for which the injected voltage is from 350 mV (~390 e^-) to 1100 mV(~1220 e^-).

Secondly, two new fast in-matrix readout architectures have been designed,

but only the FEI3-like one was fully characterized. The FEI3 chip array uses data-driven readout and token priority to transfer data to the end of the column. However, the original FEI3 pixel size is 400×50 μm^2, so the complete readout logic is impossible to be realized in a 25×25 μm^2 area. Therefore, a column-drain-based readout architecture is proposed. The timestamp is not stored inside a pixel but at the end of the column, and the ROM that stores the hit information is changed to a direct address encoding MOS transistor matrix, and a double-column is used to share the readout bus. Thus, the area of the readout logic circuit is reduced to 13.7×25 μm^2.

Thirdly, the TaichuPix1 has implemented a high-data-rate digital peripheral readout circuit based on a 512×1024 array scale. The circuit has a two-level FIFO readout structure and supports two readout modes, trigger, and triggerless mode. To satisfy the vertex detector physical requirements, the trigger mode data rate can achieve a speed of 5 MHz/32bits, and the triggerless mode is capable of a speed of 120 MHz/32bits.

Fourthly, TaichuPix1 is the first fully functional prototype for the CEPC vertex pixel detector. It includes a fast-response analog front-end circuit, the high-speed digital logic circuit in the pixel, and a high data rate peripheral readout logic. At the same time, a serializer with an internal phase-locked loop (PLL) that can be operating from 160 MHz to 3 Gbps is also included.

The experimental characterization of TaichuPix1 has been presented, including the charge collection via the charge injection mechanism, the threshold dispersion (typical FPN of 24.4 mV) and the noise distribution (typical TN of 9.7 mV) of the pixels based on the FEI3-like scheme and the results of the laboratory measurement using a radioactive source (^{90}Sr). The results prove the functionary of the digital periphery and serializer are able to transmit the hit information to the data interface correctly. And it also demonstrates that the analog front-end presents a faster-rising edge with a short time walk (~57 ns) and that the area-limited FEI3 in-matrix digital logic is properly operating at the 40 MHz system clock.

Although the electronics measurement of TaichuPix1 has been verified, there still exist several limitations of the TaichuPix1 chip. The band-gap reference circuit designed for the DACs is not as good as expected, so the bias to the analog front-end has to be supplied with an external reference voltage. In addition, the in-matrix readout logic also suffers from high power issues. Following the experience of the TaichuPix1, the second prototype, the TaichuPix2, has been implemented. Early measurements show that the second prototype solved most of the previous power

issues. The band-gap voltage bias is strong enough to drive the analog front-end. The high-impedance issues of the data buses are also removed by adding an extra latch at the end of the column.

9.2 Outlook

The TaichuPix1 is a fully functional small-scale prototype designed for the CEPC vertex detector. Although the simulation optimized the analog front-end for a fast-rising edge and a time walk lower than 33 ns, the standard CIS process adopted in the TaichuPix1 cannot completely satisfy the speed requirement. In this process, the charge collection time would be much larger than 33 ns if the charge is generated in the non-depleted part of the pixel. A modification process that has a fully depleted epitaxial layer will be considered in the full-sized prototype. TaichuPix2 is an updated version to optimize several issues existing in TaichuPix1. The power consumption is another limitation of this prototype. A faster timing performance was achieved at the expense of increasing the power consumption (~200 mW/cm^2). Note that in the case of the ALPIDE chip, the power is around 35 mW/cm^2, while the signal peaking time is 5 times slower. The trade-off between fast timing and low power consumption will be addressed in follow-up research.

As for the in-matrix readout logic, two different schemes were designed in parallel, but this work only presented the experimental results of the FEI3-like because the ALPIDE-like scheme presented problems on the matrix scan readout and the high-impedance state that exists in the columns data bus. Only the top priority columns can be read out correctly. The ALPIDE-like readout architecture is based on the improved AERD structure while employing the same digital readout periphery as the FEI3-like one. The solution could be to design a new digital periphery readout dedicated to the ALPIDE-like scheme.

In order to discriminate the 25 ns bunching spacing, the timestamp is critical to arbitrate the hit information. The timestamp is recorded at the end of the column to achieve a small pixel size with a 25 μm pitch. However, due to the delay of the long metal line from the topmost pixel to the periphery digital readout, it is difficult to control the readout time for one pixel within 25 ns. If the delay of two hits for one pixel is less than 50 ns, they may be assigned to the same timestamp. A possible solution for this issue is to design a super-pixel to share an in-pixel timestamp generator or use a smaller CIS technology such as TowerJazz 65 nm to be able to integrate into the pixel a more complicated circuitry.

The TaichuPix1 was a fundamental step towards the final monolithic pixel sensor that will be the core of the CEPC vertex detector. Compared to previous prototypes, the TaichuPix1 made significant progress towards meeting the ultimate requirements of the final device. A thorough characterization was carried out, which demonstrated that the FEI3 matrix of the chip is fully functional. The lessons learned were incorporated in the full-size chip prototype that is about to be submitted at the time this dissertation is being finished.

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List of publications and activities

a) Publications with leading contributions

[1] *The TaichuPix1: A Monolithic Active Pixel Sensor with fast in-pixel readout electronics for the CEPC vertex detector*, T. Wu; W. Wei; S. Grinstein et al., Published in Journal of Instrumentation in 2021

[2] *A full functional Monolithic Active Pixel Sensor prototype for the CEPC vertex detector*, Tianya Wu; Raimon Casanova et al. Published in Proceedings of IEEE International Conference on Electronics, Circuits and Systems (ICECS) in 2019

[3] *High data-rate readout logic design of a 512 x 1024 pixel array dedicated for CEPC vertex detector*, X. Wei; W. Wei; T. Wu; Y. Zhang et al. Published in Journal of Instrumentation in 2019

[4] *A Monitoring 12-bits Fully Differential Second Order Incremental Delta Sigma Converter ADC for TimePIx4*, Raimon Casanova; Tianya Wu. Published in Proceedings of Topical Workshop on Electronics for Particle Physics - PoS(TWEPP2019) in 2019

b) Publications with direct contributions

[5] *Implementation Method of CORDIC Algorithm to Improve DDFS Performance*, Wenjun Chen; Tianya Wu; Wangwang Tang et al. Published in IEEE International Conference on Electronics Technology (ICET) in 2020.

[6] *An improved frequency meter for atomic magnetometer based on accurate time measurement*, Kai Jin, Wangwang Tang, Wenjing Deng, Yan Huang, Xiaoxia Ding, Tianya Wu et al., Published in IEICE Electronics Express in 2019.

[7] *Design of non-magnetic temperature control system for atomic vapor cell of atomic magnetometer*, Jin, K.; Hu, H.; Liang, Z.; Geng, X.X.; Wu, T.Y. et al., Published in Journal of Physics: Conference Series on February 01, 2021

c) Presentations

International conference talk:

[8] IEEE International Conference on Electronics, Circuits and Systems (ICECS 2019), *A full functional Monolithic Active Pixel Sensor prototype for the CEPC vertex detector*, Nov 2019 in Genova, Italy.

Internal talk:

[9] IFAE Pizza Seminar, *Overview of pixel chip for CEPC Vertex Detector*, June 2019 in Barcelona, Spain.

[10] CEPC Pixel detector satellite meeting at Oxford, *Status of chip design and characterization measurement plan for CEPC Vertex detector*, April 2019 at Oxford, UK.

Poster:

[11] Topical Workshop on Electronics for Particle Physics (TWEPP 2019), *A Monolithic Active Pixel Sensor for CEPC vertex detector*, September 2019 at Santiago de Compostela, Spain.

[12] 12th International "Hiroshima" Symposium on the Development and Application of Semiconductor Tracking Detectors (HSTD12), *A fully functional peripheral readout logic design for a CMOS pixel sensor prototype developed for the CEPC vertex detector*, December 2019 at Hiroshima, Japan

[13] 12th International "Hiroshima" Symposium on the Development and Application of Semiconductor Tracking Detectors (HSTD12), *Fast in-pixel readout for a CMOS pixel sensor prototype developed for the CEPC vertex detector*, December 2019 at Hiroshima, Japan

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十年求学时光一晃而过，桂子山日新月异。一路走来，有太多感谢难以言表。首先，我由衷感谢我最尊敬的导师——黄光明教授。仍记得 2011 年我和黄老师第一次近距离交流是在物理学院“教授面对面”，我向黄老师谈到了自己大学的焦虑和迷茫，黄老师语重心长地跟我说，“本科是打基础的阶段，首先要将自己的根基扎牢，才能确立自己未来的方向，掌握了本领就不会迷茫。”自那以后，我的重心就放在了专业课程的学习上。在 2014 年，我在黄老师的指导下非常积极地参加了电子设计大赛，从理论到实践的转换，收益良多，从此和“焊接坊”结下了不解之缘。那之后，我爱上了电路设计，并想在电路方面有所建树，于是毫不犹豫地报考了黄老师的研究生。起初，每周的例会，和超强的研究任务让我一度怀疑自己的能力，直到黄老师跟我说，学生的能力需要慢慢培养，不是导师的工具。这给了我巨大的信心，让我更加坚定了跟着黄老师读博的信念。严谨的治学态度，严格的电路设计要求常常让我备受打击，但也正是高标准才不断激励我迈向更大的成功。并教会我不畏惧挑战，迎难而上。在博士方向的十字路口，黄老师和杨苹老师推荐我参与重大科学工程项目，学习高能物理探测器与集成电路，并在 2018 年协助我前往西班牙巴塞罗那自治大学高能物理研究所联合培养。临行前，黄老师最大的嘱咐就是人身安全，并鼓励我一定要更加努力学习，在学术上不断提高自己的水平。

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For my study in Spain:

Thanks to the sponsorship of CCNU, IFAE, and CSC, I completed my study at IFAE under the supervision of Prof. S. Grinstein and Dr. R. Casanova. Not only did I improve my professional skills in high-energy physics and microelectronics design, but also I made a lot of progress on my language ability. I appreciate that I had such a wonderful journey to study at IFAE with excellent supervisors and kindly colleagues. I still remember the first day when I came to Barcelona, everything was unpredictable, and I was afraid I would have to deal with everything by myself. Luckily, I joined an enthusiastic group. They were friendly and helped me out when I had difficulties. Thanks to Prof. S. Grinstein, he allowed me to study outside China, assisted me with the financial problem, and did a lot of paperwork for me. Thanks to Dr. R. Casanova, he used to be patient in guiding me, often sitting along with me to solve my problems. Thanks to Emanuele for picking me up on the first day when I arrived in Barcelona. Thanks to Chiara, who helped me with the accommodation and accompanied me in the CM7 building for three years. Thanks to Giulia for bringing me to apply for the NIE. Thanks to Fabian, who always answered my questions patiently. Thanks to Stefano for instructing my experiments. Thanks to Lucia, who taught me a lot about Spanish culture. Thanks to Vagelis, who was always energetic to make fun with me. Thanks to Viveka, who gave me a lot of assistance, even after I left IFAE. Thanks to humorous Juan, who always shared good food with me. Of course, I appreciate all the friends I met in Barcelona. Thank you for the great time and the wonderful memories when we were together.

Tianya Wu
吴天涯
2021 年 12 月于武昌桂子山

Appendix A 中文摘要附录

A.0 研究内容与论文框架

本文从 CEPC 的顶点像素传感器的需求出发，结合前期的研究经验，提出了一种非零压缩事例驱动、按列收集读出的高速专用全功能 MAPS 像素传感器芯片 TaichuPix 的结构。重点介绍了第一次多项目晶圆（MPW）小阵列 TaichuPix1 芯片关键电路的设计原理以及仿真结果，同时展示了基于刻度电路与 β 放射源的实验结果。本文作者在课题研究过程中主要贡献为以下几个方面：

1） 根据 CEPC 概念设计报告中针对顶点探测器的物理需求，参与制定了全功能像素传感器技术原型 TaichuPix 的快速读出框架并承担阵列内数字逻辑电路的方案设计与论证。

2） 参与模拟前端放大电路的仿真，主要针对模拟电路与阵列内数字逻辑电路的读出接口的仿真。同时承担 TaichuPix1 模拟前端的测试验证工作，主要包括模拟电路工作点参数调试，像素阈值和噪声的优化，数据分析等工作。

3） 全面负责阵列内数字逻辑电路的构思，仿真，优化与验证。主要包括阵列内数字逻辑电路的方案选择与论证、电路原理设计与实现，撰写技术文档以及电路测试等相关工作。为了验证非零压缩事例驱动方案的可靠性，提出了两套不同的读出解决方案，分别是类 FEI3 和类 AERD 的读出编码。主要的攻关难点在于将高速读出的结构与小尺寸像素相结合。

4） 参与阵列外读出电路的接口时序仿真与论证。主要攻关的难点是解决顶端像素的击中信息到达底部阵列外读出电路的信号延时问题。为了确保正确的读出，所有的信号都需要满足时序要求并通过设定等待周期来最大化解决延时问题。

5） 全面负责开发基于 Xilinx ZC706 SoC FPGA 设计 TaichuPix1 芯片的读出测试系统。该读出系统采用 FPGA 片上内核 SoC 设计了两个主要的接口，一个是 SPI 协议接口，用于读写 TaichuPix1 芯片的寄存器和数据，另一个是串并转换接口，用于接收芯片的高速串行器的输出数据。FPGA 固件确定之后，只需要在 PetaLinux 操作系统建立的平台上修改顶层软件就可以实现多元化的读写控制。

6） 全面负责基于 β 放射源 ^{90}Sr 实验的芯片测试工作。主要搭建了触发（Trigger）和无触发（Triggerless）实验平台。并对芯片的总体读出架构与功能进行了测试，包括测量像素传感单元探测到 β 粒子电离沉积的电荷后，经过模拟前端电路放大的电压信号，从而验证了芯片在 40 MHz 的时钟下的读出性能，以及承担芯片数据解码与簇团分析等

工作。

本文的架构如下：

第一章， 介绍了 CEPC 的探测器主要设想以及顶点探测器的物理目标，同时讨论了可以应用于 CEPC 顶点探测器的潜在像素传感器技术。

第二章， 主要阐述了硅探测器的主要原理，首先介绍了 PN 结的基本原理与特性，再详细描述了单片有源像素传感器相关的 CMOS 工艺。同时介绍了现有的 MAPS 像素传感器芯片，论述了为什么要研发专用的 CEPC 顶点探测器像素传感器芯片。

第三章， 简要介绍了第一款 192 列×64 行小阵列全功能的像素传感器芯片 TaichuPix1 的设计原理与构架。主要包括快响应模拟前端电路，高速阵列内数字逻辑电路以及高数据率阵列外读出电路。

第四章， 详细描述了模拟前端放大电路的设计与仿真结果，同时给出了刻度电路的测试结果，该结果表明在 300 e^-的阈值条件下，模拟前端放大电路实现了小于 400 ns 的峰值时间以及 57 ns 的时间游走。

第五章， 深入介绍了两种不同的阵列内数字逻辑电路的设计与实现，为了同时满足小像素快读出的需求，参考 ATLAS 像素探测器的 FEI3 芯片的读出电路与 ALPIDE 芯片的 AERD 的读出结构，优化改进到 25×25 μm^2 的像素中。

第六章， 详细介绍了阵列外读出电路的设计需求与实现方法。针对 CEPC 的物理目标，阵列外读出逻辑需要同时满足 3 种不同的玻色子的读出需求，其中最严苛的是每微秒 120 个像素的 W 玻色子并且实现 500 ns 的死时间。

第七章， 简要描述了基于 Xilinx ZC706 FPGA 开发的 TaichuPix 的读出系统，包括芯片的配置流程，数据采集的接口设计，时序仿真与实现等。

第八章， 详细介绍了基于放射源 ^{90}Sr 的芯片验证工作。主要搭建了触发（Trigger）和无触发（Triggerless）实验平台，对芯片的总体读出架构与功能进行了验证。与此同时，对芯片的缺点和不足进行了分析，并提出了相应的改进方法。本章的最后，还提供了改进后的第二版 MPW 小规模尺寸芯片 TaichuPix2 的初步实验结果。

第九章， 全文的总结与对未来进一步研究的展望。

A.1 研究背景与课题来源

欧洲核子中心（CERN）在 2012 年正式宣布大型强子对撞机（LHC）的实验上发现了“上帝粒子”希格斯玻色子，以此验证粒子物理学家们设想的标准模型，该模型框架可以描述强力、弱

力、电磁力以及组成所有物质的基本粒子。为了更好地了解希格斯玻色子以及进一步推动基础物理学的发展，寻找新的物理突破口。由我国科学家在同年 9 月提出建造下一代环形正负电子对撞机（Circular Electron Positron Collider，CEPC）并在后期将其改造成高能质子对撞机（Super Proton Proton Collider， SPPC）的方案，在国际上引起了高度关注与巨大反响。CEPC 是一个需要全球科学家通力合作的超大科学工程，前期大量的研发实践方案论证必不可少。2016 年 11 月的 CEPC 指导委员会根据 CEPC 研究结果，并结合 SPPC 未来发展潜力，明确了 CEPC-SPPC 相互关系，确定 CEPC 周长为 100 km。2018 年 6 月以 CEPC 基准设计方案为主要设计目标的 CEPC 概念设计(Conceptual Design Report，CDR)通过国际评估。评估报告表明该项目基本可行并可以被批准进入技术设计报告(Technical Design Report，TDR)阶段。最新发布的 CEPC 概念设计中的物理目标和对撞环境对其探测器的设计提出了明确的要求。CEPC 上的物理事例率远低于大型强子对撞机，即便是事件率最高的 Z 玻色子区的频率也低于 100 kHz，而且基本没有事例堆积效应，这使得探测器记录下所有的事例变为可能，因此 CEPC 探测器需要有接近全空间角的覆盖能力，以记录尽可能全面的物理事例信息。围绕 CEPC 可能采用的探测器技术，工作组进行了大量的关键技术预研，硅像素探测器以其高分辨率、快时间响应、高计数率等优点，在多个方案中脱颖而出，成为 CEPC 顶点探测器设计研究的首选方案。CEPC 上为了重建 τ 轻子和鉴别 b-喷注、c-喷注和其他类型的喷注，对顶点探测器的冲击参数(impact parameter)测量精度提出了超高的要求——小于 5 μm；同时精确测量带电粒子的需求则要求探测器带来的物质量尽可能少，从而减少多次散射的影响。目前能满足如此高精度的技术只有采用硅像素探测器技术，而低物质量的需求则要求探测器灵敏层、读出电路、冷却系统和机械支撑尽可能轻薄。目前国内还没有完全掌握相关技术，针对这一需求，科技部重点研发计划分别于 2016 和 2018 年支持多个研究所和高校联合攻关，有望在 2023 年前制作出在精度、物质量、功耗等各方面能满足 CEPC 实验需求的硅像素探测器样机。

CEPC 面临的其中一项研究难点是其探测器内层的径迹探测器（或称为顶点探测器），用于实现出色的位置分辨，快速的读出和低物质量。CEPC 的径迹探测器必须有极高的空间分辨率来研究希格斯玻色子（Higgs boson）至底夸克（Bottom quark）或粲夸克（Charmed quark）等需要精确的径迹与顶点重建的衰变道。另外，其必须能承受电离辐照，以保证在 CEPC 的高亮度对撞环境中稳定工作，其性能好坏直接决定了 CEPC 实验的物理成果产出。像素传感器芯片是 CEPC 内层径迹探测器的研发重点。CEPC 的物理需求决定了其内层像素传感器的研制是一个前所未有的挑战。其中，为了精确测量希格斯玻色子的性质，它的空间分辨率必须高达 3~5 μm。目前在瑞士的大型强子对撞机（LHC）上最大的 ATLAS 与 CMS 实验发展出来的像素传感器的空间分辨率都在 10 微米或者以上；重离子实验 ALICE 实验升级中的 ALPIDE 像素传感器与 STAR 实验的 MIMOSA 像素传感器虽然可以达到 5 微米的位置分辨率，然而其传感器芯片的读出速度不够（10 kHz~100 kHz），无法满足 40 MHz 对撞环境与 500 ns 以下的死时间要求。综上

所述，现有的传感器均无法满足 CEPC 的物理要求。因此本课题需要根据 CEPC 的物理要求设计一款全新的专用像素传感器。

A.2 像素探测器方案选择

像素探测器对于精确确定轨迹和顶点非常重要，其难点是要实现高的位置分辨率与低物质的量，它可以通过识别 b-jets（b tagging）来选择特定的事件。随着原有加速器的不断升级（如 LHC）与未来加速器（如 CEPC）的提出以进一步探索高能物理的前沿，新的像素传感器技术用于提升探测器的性能势在必行。当前比较成熟的顶点探测器系统依赖于混合结构像素探测器，例如在 ATLAS 实验中的像素探测器就是混合结构像素探测器。它包含一个硅传感器，该传感器是一个 PN 二维阵列，每个像素的读出通道贴合连接到相同阵列规模的读出芯片（如 FEI3 读出芯片）。传感器和读出芯片上的通道通过小的（直径约为 25 μm）焊球经过复杂的对准，加热和压缩过程（称为触点邦定）进行连接。读出电路和探测传感器分开设计的优点是可以独立优化每个部分的技术。但是，混合探测器有一些局限性，例如传感器和读出电路的触点邦定使得探测器增加了一倍的装配成本，同时还引入了系统的电容，通常约为几百 fF。标准混合探测器设备的替代方案是单片传感器技术。在这种方法中，传感器和读出芯片集成在同一块硅基板上，从而避免了执行触点焊接工艺，并大大降低了器件的电容。单片器件应用于高能物理实验的研究已经有一段时间了，寻求开发一种用于高能物理对撞机实验的新型单片设备依然是研究的热点。在这几年的单片设备的研究中，已提出了用于成像应用的耗尽型 CMOS 探测器，该单片设备采用标准高压（HV）和高电阻率（HR）CMOS 技术来制造单片像素探测器。在这种标准工艺中，电子器件放置在深 N 阱内部，而耗尽区的有源部分在同一衬底上，以收集入射粒子辐射电离产生的电荷。这些传感器基于标准的商业技术，因此与典型的混合方法相比，它们在成本上非常具有吸引力。此外，它们还避免了昂贵的触点接合步骤。自将硅像素探测器用于高能物理实验以来，对其的研究与探索已经取得了相当大的进展。针对未来的高能物理实验应用方面，大量的研究设计工作正在进行，这些工作旨在探究用于顶点径迹探测的像素传感器的单点空间分辨率，抗辐照水平以及径迹探测密度。从发布的概念设计报告可知，CEPC 的探测器的挑战包括高冲击参数的分辨率，低物质量，较低的占空比和足够的抗辐照性能。为了在系统级别满足这些要求，必须选择能够实现像素尺寸小，低功耗和快速读数的传感器技术。这给 CEPC 顶点探测器提出了前所未有的挑战。CEPC 在希格斯（Higgs）玻色子工厂运行模式下要实现 0.68 μs 的击中间隔，对于 Z 玻色子工厂的运行模式要满足 25 ns 击中间隔，并且不能像国际直线对撞机（ILC）所计划的那样利用功率脉冲来降低平均功率。像 STAR 实验，BELLE II 实验和 ALICE 之类的实验不断升级的读出速度与 CEPC 的读出速度需求相当。但是，它们对冲击参数分辨率和物质量的要求不那么严格。单片有源像素传感器（MAPS）具有满足 CEPC 顶点探测器对低物质量和高分辨率要求的潜力。这项技术发展很快，用于 STAR HFT 升级的第一代基于 MAPS

的顶点探测器于 2016 年完成了为期 3 年的物理实验，而用于 ALICE ITS 实验的新一代高阻率 CMOS 像素传感器升级的相关研究成果正在大量产出。在早期的 0.35 μm 双阱工艺中，像素设计中只能使用 NMOS 晶体管。在新的 0.18 μm 四阱工艺中打破了此限制， NMOS 和 PMOS 晶体管均可用于像素设计。结合较小的特征尺寸，它成为一种非常热门的技术。ALPIDE 探测器芯片是 CEPC 顶点像素传感器的一个很好的参考，它是为上述 ALICE-ITS 升级而开发的，其性能特点非常接近 CEPC 的设计要求。为了实现最终所需的 2.8 μm 单点分辨率，需要进一步的研发以将像素间距缩小到大约 16 μm。另一个单片结构的选择是绝缘体上硅（SOI）像素传感器，经过十多年的发展，SOI 已进入成熟的新阶段。基本问题已得到解决，包括晶体管屏蔽和抗辐照性能，并且已经证明了晶圆减薄的可行性。同时，ILC 和 CLIC 的研发团队正在探索时间戳和模拟读出方案。 SOI 特点是具有完全耗尽的衬底作为有源区，它的 0.2 μm CMOS 工艺可提供较为密集晶体管数量，这与高阻率 CMOS 中的 0.18 μm CMOS 一样。因此，可以设想，CEPC 顶点探测器的读出设计可以同时研究参考这两种技术，并挖掘每种技术的发展潜力。耗尽的 P 沟道场效应晶体管（DEPFET）被称为半单片晶体管，因为只有第一级放大电路可以集成在传感器电路中，后续的处理电路则是通过单独的读出 ASIC 中集成到像素中，这一点与混合结构像素传感器类似。BELLE II 实验就是安装基于 DEPFET 技术的传感器来实现顶点探测器。读出电路的功耗相对于其他部分非常大，将单独设计的读出芯片放在探测器区域之外，可以实现传感器探测区域非常低的功耗以及较低的物质量。面临的挑战是要在所需的间隔（20 μs/帧或更小）时间内，周期性地对大像素阵列上的调制电流进行采样。混合结构像素传感器芯片在强子对撞机上已经使用了数十年，现在，CLIC 研发部门正在推动 50 μm 薄型传感器的开发，以 25 μm 的间距触点键合到 50 μm 的薄型 ASIC 上。混合探测器技术不断发展并受益于现代工业技术的发展持续向前推进。除了超深亚微米（VDSM）ASIC 技术具有出色的性能，可以实现复杂功能之外，纵向与横向互连技术的工业发展也有助于满足混合结构的物质量要求。

A.3 国内研究现状

自 CEPC 提出以来，先后有多款基于 MAPS 结构的技术原型芯片研发完成，但都只针对特定传感器结构和芯片读出电路的功能验证，无法满足高位置分辨率与快读出的需求。其中，JadePix-1 是为 CEPC 顶点探测器开发的第一个原型，用于研究不同传感器几何形状的性能。在同一芯片上实现了几个不同的像素扇区，因为电极面积和封装面积是传感器电荷收集二极管几何形状中的两个关键元素，并且对传感器电荷收集性能产生决定性影响。JadePix-1 二极管表面电极是一个面积从 4 μm^2 到 15 μm^2 不等的八边形。实验结果表明，更大的电极面积可以提高电荷收集效率，但会带来更大的传感器噪声。而较大的封装面积对传感器增益没有太大影响，但它可以提高电荷收集效率。JadePix-1 芯片总体尺寸为 7.9×3.9 mm^2，基于 180 nm CMOS 工艺设计了两种不同传感器尺寸的像素阵列，像素单元面积分别为 33×33 μm^2 和 16×16 μm^2。芯片的

读出方式是基于滚动快门（Rolling shutter）的方式。经过在德国电子同步加速器研究所（DESY）的束流实验，33×33 μm^2 和 16×16 μm^2 像素面积获得的空间分辨率分别为小于 5 μm 和小于 3.5 μm。除此之外，还有一款像素芯片 JadePix-2 用于研究不同阵列内数字读出逻辑对传感器性能的影响。JadePix-2 的芯片尺寸为 3×3.3 mm^2，包含 112×96 个方形像素，单个像素尺寸为 22×22 μm^2。该芯片提出了两种阵列内数字化电路，两种设计均采用高压偏置电荷收集二极管，并采用输出偏置存储技术的比较器来减少输出偏置和像素到像素的放大器数量。收集的电荷按比例转换为电压信号，然后将其交流耦合到比较器，电压信号被放大并与阈值电压进行比较。然后将命中结果"1"或"0"存储在锁存器中，并通过数字缓冲区逐行传输到列。两种设计之间的主要区别在于信号放大方案，一种采用差分放大器，另一种采用两级单端放大器架构。在滚动快门模式下读取像素阵列，两种设计的平均处理时间分别为 100 ns/row 和 80 ns/row。实验结果表明，两种结构单个像素的总等效电荷噪声（ENC）分别约为 29.5 e$^-$和 31 e$^-$，对应于单个像素的电流分别为 6.5 μA/pixel 和 3.7 μA/pixel。除 JadePix-1 和 JadePix-2 之外，还有一款基于事例击中（Data-driven）读出结构的像素传感器芯片 MIC4（MAPS in CCNU）设计完成。MIC4 芯片包含一个大小为 64 列×128 行的像素矩阵，每个像素的大小为 25 μm×25 μm，目的是研究高度集成的紧凑像素，像素内鉴别器连接到稀疏像素读出电路的可行性。与滚动快门的读出结构相比，事例击中的读出结构能够加快读出时间并降低功耗。经过测试，MIC4 的模拟前端电路能够达到 1 μs 以内的峰值上升时间，整形时间小于 3 μs，充电阈值为 100 e$^-$，平均时间噪声（TN）为 6 e$^-$，固定模式噪声（FPN）为 36 e$^-$。利用新的数据驱动读出电路架构，数字像素部分能够实现 30 MHz 的击中读出频率。在 2020 年，JadePix 芯片的研究团队在之前的基础上还研制了一款 JadePix3 芯片，其主要设计目标是研究低功耗小尺寸的前端电路。该芯片的总面积为 10.4 ×6.1 mm^2，共有 512 行 192 列像素，最小的像素尺为 16×23.11 μm^2。同样采用滚动快门的读出方式，每次读出一行，通过行分布的控制线打开一行的输出开关，同时对上一行的寄存器进行复位。若按每一行所用的读出时间和复位时间均为 200 ns 来评估，总共需要 102 μs 来完成 512 行的读出，实际测得积分时间为 98.3 μs，芯片的功耗小于 100 mW/cm^2。

按照 CEPC 研究组既定的建设规划，预期在 2023 年之前能够实现一个顶点探测器的样机雏形研发。但之前研发的像素探测器芯片都不能完全满足 CEPC 顶点探测器的物理目标，因此自 2018 年开始以来，由科技部支持的 CEPC 二期（MOST2）的关键技术研发计划启动，旨在研发和验证高精度径迹测量的硅像素探测器技术，研制出一个高精度、抗辐照、低物质量的硅径迹探测器原型机，验证其空间分辨率达到 3-5 微米。根据 2018 年发布的 CEPC 的概念报告中对顶点探测器的基准结构进行分析，顶点探测器将做成类似国际直线对撞机的结构，设计成直径 12 cm 高 25 cm 的圆柱桶状结构，内层按照三级台阶式的装配架构，每一级台阶的正反两面都贴置探测器芯片，计划在每一面放置 3 个芯片，每一个芯片的面积为 1.1 × 2.08 cm^2，预计每一面传感器贴合面积为 1.1×62.5 cm^2。根据以上需求进行计算，本课题组初步计划将芯片设

计成规模为 512 行×1024 列的像素阵列，参照前期的预研经验，单像素面积设定为 25×25 μm^2，加上必要的外围逻辑电路，单个芯片的面积大约为 1.4×2.56 cm^2。前期大量的电路设计与仿真工作都是围绕 512 行×1024 列全尺寸芯片展开。为了尽可能降低设计风险和节约成本，前两次的流片工作都是基于多项目晶圆（MPW）的 192 列×64 行的小规模阵列，用于验证和评估各个模块的性能指标。

A.4 快响应模拟前端电路的设计与实现

为了保证信号能够满足 CEPC 顶点探测器的快速读出，模拟前端放大电路除了考虑轻型结构来降低面积以实现高分辨率外，还应该考虑达峰时间以及时间游走（timewalk）问题。TaichuPix1 芯片沿用 ALPIDE 的模拟前端电路的设计思路，相对于 ALPIDE 的 2 μs 的达峰时间，通过提高增益将其改进到更快的达峰时间（<400 ns）以及更短的时间游走。时间游走是定义不同电荷量的注入引发的上升时间抵达固定阈值翻转时间的偏移量。导致时间精度偏差的因素主要有两个，一个是系统噪声引发的信号抖动（jitter），另一个是信号的幅度。探测器的时间是指确定粒子入射的电荷产生脉冲响应的发生时间。与幅度测量一样，信噪比很重要，但起决定因素的参数不是信噪比，而是过阈值时的斜率与噪声比。除了时间“抖动”之外，信号超过固定阈值的时间还取决于信号幅度。随着幅度的变化，时序信号会发生偏移，因此信号幅度的变化将加大过阈值的时间差。时间的精度受到抖动（由于噪声）和时间游走（由于幅度变化）的双重限制。如果信号的上升时间固定，则可以通过测量信号高度并校正时间测量值来逐个事件地补偿时间游走。在半导体传感器中，上升时间由电子和空穴的双重因素决定，因此斜率有两个成分。在不同电荷注入产生的幅度一定的情况下，可以通过降低阈值或使用幅度补偿电路来减少时间游走。在径迹探测器中，所有粒子都要穿过传感器，因此电子和空穴的相对贡献始终相同，因此无需进行上升时间补偿。虽然粒子穿越传感器电离结果沉积相同的平均能量，但是幅度变化特别大，因此时间游走是一个问题。为了实现 CEPC 顶点探测器的 40 MHz 的击中间隔，应考虑时间游走因素以实现可以满足最终要求的快速读出系统。仿真结果表明，注入电荷量为 400 e^-时（假定甄别器翻转的阈值电荷为 182 e^-），输出信号边沿翻转延时为大约 31 ns，而在注入电荷为 3000 e^-时，翻转延时则大约为 9 ns，二者相差的 22 ns 就是电路的时间游走。在衬底接 0V 的情况下，芯片的平均阈值测得大约在 300 e^-，在此阈值条件下，通过示波器测量输出信号过阈值点到刻度电容脉冲注入 APULSE 上升沿的时间，在 350 mV（约 390 e^-）至 1100 mV (约 1220 e^-) 刻度电压之间得到的时间游走大约为 57 ns。相比于 ALPIDE 芯片在同等阈值条件下几百纳秒的时间游走，减少了一个量级。

A.5 高速阵列内数字逻辑电路的设计与实现

为了避免探测器读出时的事例堆积，高速的阵列内读出逻辑必不可少，面临的挑战是如何将高速的阵列内读出应用在较小的像素面积中，同时提高位置分辨率。本文对于阵列内数字逻辑电路设计了两种快速的读出结构，并同时集成在前两次的小阵列验证芯片中（TaichuPix1，TaichuPix2）。这样两种方案性能的差异和各自的优势就可以非常直接的在测试中反映。第一种是基于 ATLAS 实验像素探测器中的 FEI3 读出芯片的数字读出结构，因为像素尺寸的限制，对该结构进行了相应的调整和改进，时间戳电路从单个像素内转移到了列端读出，存储击中地址信息的 ROM 改进为一个上下拉 MOS 管组成的地址编码阵列，大大降低了像素内数字逻辑电路的面积占比。之外，并行设计了一种基于 ALPIDE 中应用的增强型读出地址编码复位解码（AERD）的阵列内数字逻辑电路，仿真结果表明，这两种结构都实现了高速的读出逻辑(40 MHz)，优先编码，以及较小的像素面积(单个像素面积在 25×25 μm^2)。

LHC 中的 ATLAS 实验于 2012 年发现了上帝粒子希格斯玻色子，CEPC 的物理目标之一就是作为希格斯玻色子的工厂，对大量的希格斯玻色子进行精确测量。因此 ATLAS 实验的像素探测器具有一定的参考性。与 MAPS 结构的像素探测器不同，该实验采用的是混合结构的探测器芯片，即传感器部分和读出电路的芯片分离，因此单个像素的尺寸较大，约为 400 μm×50 μm。本设计的研究思路是将经过实践证明的 FEI3 的读出芯片的设计原理，通过一定的改进转化至 MAPS 的结构中。FEI3 读出芯片的读出模式是基于数据驱动的分布式处理，即有像素检测到信号击中后才开始启动读出。通过这种方法，可以将密集的传感器和稀疏化的读出电路相结合。为了提高时间分辨率，可以在每个像素单元内设计一个计数器，该计数器按照一定的频率不断循环计数，直到检测到击中信号才停止计数。如果计数器与实验的束流间隔时钟同步，则可以将击中像素和特定的束流匹配上。实现数据驱动读出的一种有效且简单的方法是在每列像素中采用稀疏扫描结构的令牌环。在第一个像素被允许发送数据之后，其令牌将在下一个时钟周期传递给另一个像素。FEI3 读出芯片就是每列像素共享一个令牌环和一个数据总线，其中持有令牌的像素将其命中信息放置在数据总线上，下一时刻，放置在数据总线上的信息将存储在芯片外围的击中信息缓存中，并将缓存通过最终的触发器触发读出，并且只读取带有与已触发事件相对应的时间戳匹配的数据，滤除不匹配的数据。令牌传递方案的主要问题是，读取速度受令牌传递的时间限制。改善时序的一种方法是除令牌传递逻辑外，添加额外的快速预读逻辑。FEI3 芯片就采用了优先级超前逻辑结构，快速优先级扫描路径通过最小化关键数据路径中的延迟来实现。该结构一列有 160 个像素，分成 10 个存储段，每个存储段由 16 个像素组成，分为三种不同类型。前两种类型的像素由 NAND 和 NOR 单元组成，用于在稀疏扫描期间降低优先级。像素在 NAND 和 NOR 版本之间交替，以最小化优先级稀疏扫描延迟，从而提高读取速度。在每个存储体的末尾，有第三种类型的像素单元连接到超前路径，以实现快速优先级传递。

另一种值得参考的阵列内数字逻辑研究方案就是应用于 ALPIDE 芯片的 AERD 读出结构，与混合结构像素相比，该结构是直接应用在 MAPS 的结构中，因此可以实现较小的像素面积。

AERD 读出电路是基于具有分层地址编码器和复位解码器的树型仲裁器方案实现。树型仲裁器的基本逻辑单元包含三个部分，FASTOR 链，地址编码器以及复位解码器。FASTOR 链用于生成 VALID 信号并将其传递到阵列外部。地址编码器接收优先级逻辑输出作为输入，生成每个基本块的地址信号。复位解码器（或非门）由优先级最高的编码器的输出产生，然后从阵列外读出电路产生的复位信号对优先级最高的像素进行读取和复位，再依次复位优先级低的地址单元。普通型的 AERD 结构是通过整个时钟周期来生成地址并将其传输到外围电路中，而读出速度增强型的 AERD 结构是采用半个周期来实现地址的编码和传递，则可以充分提高在 40 MHz 时钟下的读出速度。读出速度增强型逻辑块的主要区别在于，优先级高的模块输出一个信号用于使能优先级较低的地址编码器模块。这样复位阶段和解码阶段的时序就是分开的，提高了时钟利用率。为了确保仅通过具有最高优先级的像素来对地址进行编码，以避免在地址总线上发生冲突，需要额外的“或”门逻辑来处理使能信号上的优先级路径。地址编码器和复位解码器数据驱动的读出架构在读出时间和功耗方面均显示出显著优势。通过解码和复位阶段的分离，读出速度可以从 10 MHz 提高到 40 MHz。

将 FEI3 结构和 AERD 的阵列内数字逻辑电路应用到 CEPC 顶点探测器中具有各自的优势和不足，传统的 FEI3 结构可以实现非常出色的时间分辨率（25 ns 的击中间隔），但复杂的电路结构致使单个像素面积过大，无法满足要求。而对于 AERD 来说，ALICE 实验的击中间隔只有 100 kHz，因此只要阵列内数字逻辑足够快就可以满足需求。因此 TaichuPix1 芯片在设计过程中对读出速度与像素单元面积做出了一个权衡，第一种方案是将 FEI3 结构中的数字逻辑电路只保留令牌环的核心部分，并通过动态触发器代替传统触发器以降低晶体管的数量。时间戳电路从阵列内转移到列端处理，并通过上下拉 MOS 管的地址生成器代替阵列内存储器以进一步降低面积。对于第二种类似于 AERD 的方案来说，采用相同的列端电路匹配时间戳来甄别击中顺序，以提高时间分辨率。但由于时间戳没有存储在像素内部，受长信号线延时的影响导致目前时间分辨率上无法完全满足最终的设计要求。这一点将在未来通过更小尺寸的 CMOS 工艺（如 65 nm）来实现更小的像素尺寸和更高的时间分辨率。

A.6 高数据率数字外围读出电路的设计与实现

CEPC 概念设计给出的最严苛击中条件是满足 W 玻色子单芯片每微秒 120 个像素被击中的频率。如此高的数据率对外围读出电路来说是个不小的挑战，因此本文提出了两级 FIFO 架构的阵列外围读出方案，以解决大规模 1024×512 阵列芯片高数据率读出问题。

对于外围读出电路设计，主要考虑像素的击中率和可接受的死区时间。命中率是根据最近的 CEPC 概念设计报告给出的三个主要参数分别计算的。希格斯玻色子在 240 GeV 的质心能量模式下的击中间隔和击中密度为 680 ns 和 2.4 hits/cm^2/ event，W 玻色子在 160 GeV 质心能量下的参数为 210 ns 和 2.3 hits/cm^2/event，以及 Z 玻色子在 91 GeV 的质心能量下的参数为 25 ns 和

0.25 hits/cm^2/ event。按照单个像素面积为 25×25 μm^2，像素阵列规模为 512×1024，平均簇大小为 3 个像素来计算，得到最大的数据率大约为 120 MHz。高数据率使得外围读出电路要能够处理巨大的数据量。假设每个像素的击中信息都采用 32 位（时间戳：8 位，像素地址：19 位，其他：5 位）重新编码，则串行接口的输出速率要达到 3.84 Gbps。这会使得数据采集（DAQ）系统难以处理如此高的数据率，尤其是在多个芯片并行工作的情况下。通用解决方案是提供触发信号，仅将与触发信号匹配的数据发送到 DAQ 系统。本设计假定触发等待时间和平均触发频率分别为 3~6 μs 和 50 kHz。考虑到击中间隔和像素击中密度，触发模式提供 0~7 个时钟周期的时间误差窗口，则触发的最大串行数据率小于 40 Mbps。由于不确定当前是否会在系统中提供触发信号，因此在设计中同时考虑了触发模式和无触发模式。死区时间对于像素传感器来说需要足够短。太长的死区时间长会降低探测效率。假设像素以双列的形式组合排列，为了尽可能降低时间延迟，所有的双列都并行读出。因此，死区时间对应于在一个双列中像素读出的时间，即 1024 个像素。为了实现高于 99%的探测效率，死区时间应小于 500 ns。假设整个芯片仅输出击中像素，从给出的击中密度，根据泊松分布可知击中像素个数小于 3，乘以 3 个像素的平均簇，一个双列需要读取的像素应小于 10，单个像素读出时间约为 50 ns，这样 500 ns 的死区时间完全满足设计要求。同时，按照双列并行读出方式，每个击中像素以 32 位数据编码，击中信息用 40 MHz 的时钟频率先缓存在深度为 12 字节的列级 FIFO 中，再发送给 160 MHz 输出时钟的芯片级 FIFO，在无触发模式下以实现 120 pixel/μs 的数据读出频率需求。分别在触发模式和无触发模式下仿真数字外围电路。仿真过程中考虑了触发延迟，时间戳误差，随机数据，递增数据，递减数据，连续数据，非连续数据等因素的差异。仿真结果表明所有功能都得到了很好的验证，并且能够满足 120 pixe/μs 的读出速度。

A.7 基于放射源的芯片全功能测试

读出系统的设计对芯片的表征至关重要，本文以 Xilinx 片上操作系统 FPGA 开发板 ZC706 为主控核心设计固件程序并通过搭建 PetaLinux 系统来实现多元化的软件设计，通过 SoC 软核内部总线直接与外设通信大大提高了芯片的配置效率。本文主要采用 β 射线（核素 ^{90}Sr）来验证芯片的整体功能。首先基于 Xilinx ZC706 SoC 开发板设计了一个读出系统，该读出系统采用 FPGA 片上内核设计了两个主要的接口，一个是 SPI 协议接口，用于读写 TaichuPix1 芯片的寄存器和数据，另一个则是串并转换接口，用于接收芯片的高速串行器的输出数据。FPGA 固件写好之后，通过定制的 PetaLinux 操作系统将固件程序打包烧录于 SD 卡中，则可以直接通过 SD 卡启动 ZC706 开发板。同时，开发板上的以太网接口控制器是默认打开的，只要编译相应的驱动程序即可通过网线实现开发板与电脑主机的互联。本设计采用 VIVADO 软件自带的 SDK 开发套件编写顶层的控制程序，通过 TCP/IP 协议将编译好的执行文件传输至 SD 卡中，这样就不需要更改 FPGA 的固件即可实现多元化的软件设计。读出系统准备好之后，下一步就

是通过放射源发射的 β 射线来实现功能的验证。将芯片放入一个大小适中约 1cm 高的黑色盖子中，将放射源直接放置于黑盒之上，打开读出系统采集数据。顶层配置软件可以设置寄存器实现对芯片的触发和无触发模式配置。无触发模式下，直接就可以记录放射源的 β 射线的击中位置。当芯片配置在触发模式时，则需要通过一个闪烁体装置产生外部触发信号。TaichuPix1 芯片置于放射源与闪烁体之间，闪烁体探测到了 β 射线之后，经过电平转换板卡机箱产生一个正脉冲触发信号。该信号连接到 FPGA 上，加上触发延时，再连接到 TaichuPix1 芯片的外部触发引脚上，便可以实现芯片的触发功能。通过放射源实验，证明了 TaichuPix1 芯片的模拟前端电路，阵列内数字逻辑，阵列外数字读出逻辑与高速串行器的整体链路工作良好，实现了芯片的既定功能。

A.8 总结与展望

本文采用单片有源像素传感器（MAPS）技术，应用非零压缩事例驱动与按列收集的读出架构实现了能应用于 CEPC 顶点探测器的、高位置分辨率及快速读出的 TaichuPix 系列像素传感器原型芯片，该系列芯片包含像素传感单元，阵列内前端电路，阵列外围读出电路以及高速串行数据接口等模块。主要介绍了电路的设计原理以及第一版小规模阵列的 TaichuPix1 的测试情况，结果表明在 25×25 μm^2 的单像素面积下，实现了快速响应的模拟前端电路，高速的阵列内读出逻辑电路，高数据率的阵列外围读出电路。还验证了带有锁相环 3 Gbps 左右的串行编码器接口。为下一阶段的全规模大尺寸的像素传感器提供了非常有价值的设计经验，并有望在 2023 年实现 CEPC 顶点探测器样机的研发和测试。

尽管 TaichuPix1 芯片实现了高位置分辨、快速读出的目标，但是仍存在一些不足之处。由于模拟前端电路加快了峰值到达时间和减小了时间游走，因此带来了功耗的增加。单模拟前端的功耗密度就增大到了 130 mW/cm^2，而 ALPIDE 的整体功耗仅为 35 mW/cm^2。对于阵列内读出逻辑，类 FEI3 部分的读出结构基本符合预期，而增强型 AERD 读出结构的部分只有部分优先级最高的双列可以读出。这些问题将会在未来的研究中进一步优化和改进。