Universitat Autònoma de Barcelona

Integration of vertical Single Electron Transistor into CMOS technology

Alberto del Moral Cejudo

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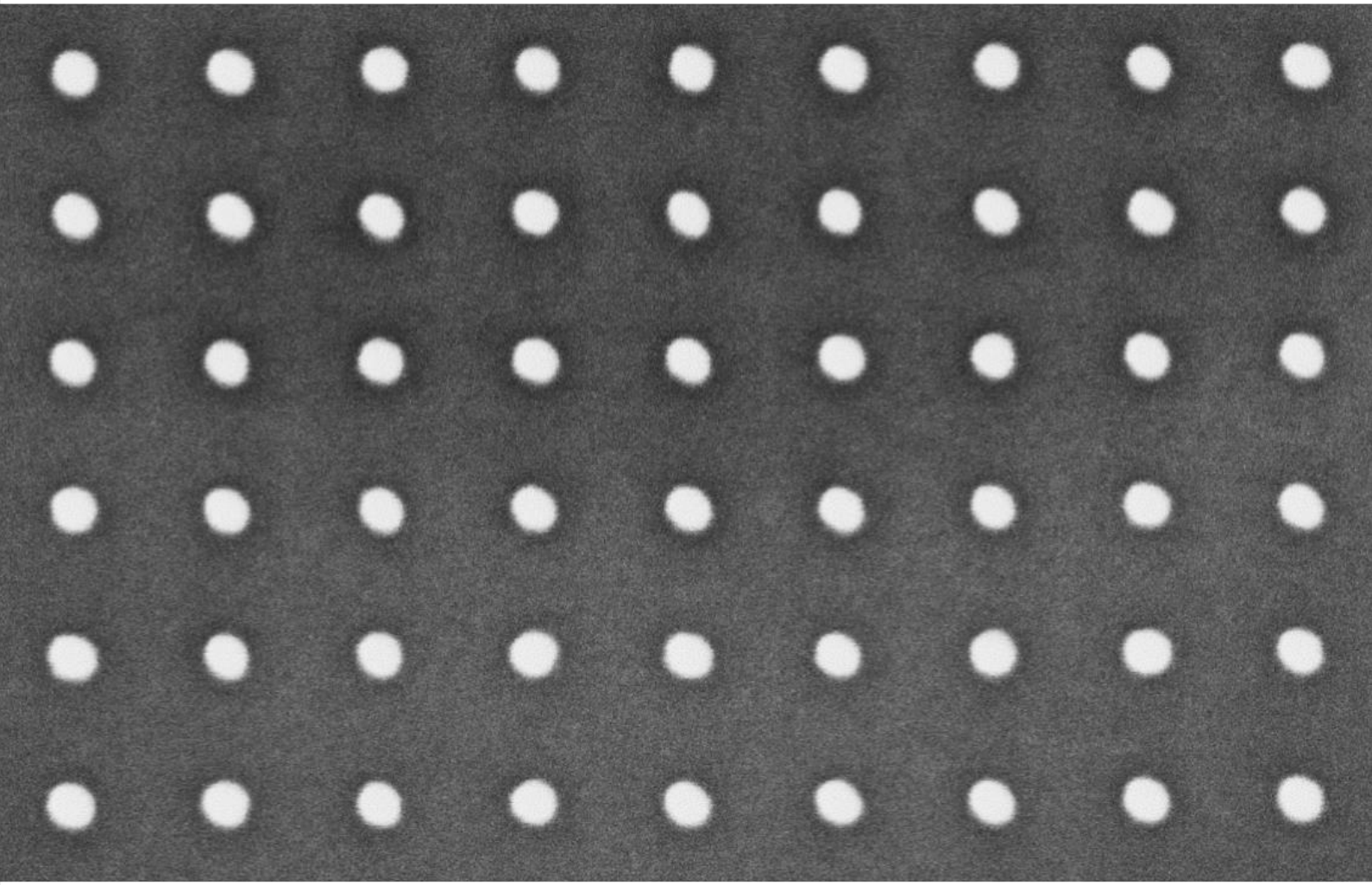

Institute of Microelectronics of Barcelona (IMB-CNM, CSIC)

Alberto del Moral Cejudo

Supervisors:

Dr. Esteve Amat Bertran
Prof. Francesc Pérez-Murano

Ph.D. in Electronic and Telecommunication Engineering

CSIC Consejo Superior de Investigaciones Científicas

CNM Centre Nacional de Microelectrònica IMB

UAB Universitat Autònoma de Barcelona

Integration of vertical Single Electron Transistor into CMOS technology

Ph.D. Thesis

Dissertation presented in partial fulfilment of the requirements for the degree of
Doctor in Electronic and Telecommunication Engineering

By

Alberto del Moral Cejudo

Directors:

Dr. Esteve Amat Bertran
&
Prof. Francesc Pérez-Murano

Department of Electronic Engineering
Universitat Autònoma de Barcelona

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This is to certify that the thesis entitled, "*Integration of vertical Single Electron Transistor into CMOS technology*" has been written by Alberto del Moral Cejudo and is submitted in partial fulfilment of the requirements to obtain the degree of Doctor of Philosophy in Electronic and Telecommunication Engineering under guidance and supervision of Dr. Esteve Amat Bertran and Prof. Francesc Pérez-Murano (IMB-CNM, CSIC)

Director
Dr. Esteve Amat Bertran

Director
Prof. Francesc Pérez-Murano

Author
Alberto del Moral Cejudo

Cerdanyola del Vallès, June 2021

"Solvitur ambulando"

Summary

Integration of vertical Single Electron Transistor into CMOS technology

This thesis presents the investigations performed towards the integration of Single Electron Transistor (SET) into Complementary Metal-Oxide-Semiconductor (CMOS) technology.

Two of the main drives in semiconductor industry are device miniaturization and power consumption reduction. In the most advanced nodes, three-dimensional architectures have gained significant importance to increase the integration density, being vertically arranged devices the most suitable candidates for the ultimate generations. On the other hand, single electron devices are examples of ultra-low power consumption circuits.

In this work, the fabrication of a SET based on a vertical nanowire and its co-integration with CMOS technology is addressed. The starting point is a $Si/SiO_2/Si$ nanopillar with Si nanodots in the intermediate SiO_2 layer, acting as quantum dot of the system. The subsequent gate and drain electrodes are placed all-around the embedded oxide and on contact with the pillar cap, respectively. Pillar integrity and its electrodes contacting are validated by structural characterization.

While SET integration in large-scale production is still challenging, its combination with CMOS technology benefits from the technological maturity of integrated circuits processing, overtaking SET intrinsic drawbacks as background noise or device instability. This work also reports the CMOS compatible and monolithic fabrication of a conventional planar transistor co-integrated with a vertical SET. The process fabrication is adapted to fulfil the restrictions imposed by the pre-fabricated SET, such as reduced thermal budget, protective layers and modified doping.

The monolithic fabrication of vertical SET and planar transistors is demonstrated; the pillar integrity is preserved, and the fabricated transistors operate at optimum conditions for SET compatibility.

Resumen

Integración de transistores verticales de un solo electrón en tecnología CMOS

Esta tesis presenta las investigaciones realizadas hacia la integración de transistores verticales de un solo electrón (SET) en tecnología metal-óxido-semiconductor complementario (CMOS).

Dos de las principales motivaciones de la industria de semiconductores son la miniaturización de dispositivos y la reducción de consumo de energía. En los nodos más avanzados, las arquitecturas tridimensionales han ganado una importancia significativa para aumentar la densidad de integración, siendo los dispositivos dispuestos verticalmente los candidatos más adecuados para las generaciones más recientes. Por otro lado, los dispositivos de un solo electrón son ejemplos de circuitos de bajo consumo energético.

En este trabajo, se aborda la fabricación de un SET basado en un nanohilo vertical y su co-integración con tecnología CMOS. El punto de partida es un nanopilar $Si/SiO_2/Si$ con nanopuntos de Si en la capa intermedia de SiO_2, que actúan como puntos cuánticos del sistema. Los electrodos de puerta y drenador se sitúan alrededor del óxido intermedio y en contacto con la parte superior del pilar, respectivamente. La integridad del pilar y el contacto de sus electrodos se validan mediante caracterización estructural.

Aunque la integración SET en producción a gran escala es todavía un reto, su combinación con tecnología CMOS se beneficia de la madurez tecnológica del procesamiento de circuitos integrados, superando al mismo tiempo los inconvenientes intrínsecos del SET como ruido de fondo o la inestabilidad del dispositivo. Este trabajo también presenta la fabricación monolítica y compatible con CMOS de un transistor planar convencional co-integrado con un SET vertical. La fabricación del proceso se adapta para cumplir las restricciones impuestas por el SET prefabricado, como presupuesto térmico reducido, capas de protección o dopaje modificado.

Se demuestra la fabricación monolítica de SET y transistores planares convencionales; se preserva la integridad del pilar y los transistores fabricados funcionan en condiciones óptimas para la compatibilidad SET.

Resum

Integració de transistors verticals d'un sol electró en tecnologia CMOS

Aquesta tesi presenta les investigacions realitzades cap a la integració de transistors verticals d'un sol electró (SET) en tecnologia metall-òxid-semiconductor complementari (CMOS).

Dues de les principals motivacions de la indústria de semiconductors són la miniaturització de dispositius i la reducció del consum d'energia. En els nodes més avançats, les arquitectures tridimensionals han guanyat una importància significativa per tal d'augmentar la densitat d'integració, sent els dispositius disposats verticalment els candidats més adequats per a les generacions més recents. D'altra banda, els dispositius d'un sol electró són exemples de circuits de baix consum energètic.

En aquest treball, s'aborda la fabricació d'un SET basat en un nanofil vertical i la seva co-integració amb tecnologia CMOS. El punt de partida és un nanopilar $Si/SiO_2/Si$ amb nanopunts de Si a la capa intermèdia de SiO_2, que actuen com a punt quàntic del sistema. Els elèctrodes de porta i drenador es situen al voltant de l'òxid intermedi i en contacte amb el cap del pilar, respectivament. La integritat del pilar i el contacte dels seus elèctrodes es validen mitjançant caracterització estructural.

Tot i que la integració SET en producció a gran escala és encara un repte, la seva combinació amb tecnologia CMOS es beneficia de la maduresa tecnològica del processament de circuits integrats, superant els inconvenients intrínsecs del SET com el soroll de fons o la inestabilitat del dispositiu. Aquest treball també presenta la fabricació monolítica i compatible amb CMOS d'un transistor planar convencional co-integrat amb un SET vertical. La fabricació del procés s'adapta per complir les restriccions imposades pel SET prefabricat, com ara un pressupost tèrmic reduït, capes de protecció i dopatge modificat.

Es demostra la fabricació monolítica de SET i transistors planars convencionals; es preserva la integritat del pilar i els transistors fabricats funcionen en condicions òptimes per a la compatibilitat SET.

Acknowledgements

The first words of this thesis must be addressed to acknowledge those who have play, in one way or another, a relevant role in its development. I would like to express my most sincere gratitude to both directors of this thesis. Francesc and Esteve, you have been extremely supportive from the very beginning, and your guidance and advices have been a key drive during this journey.

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Christian Pinto, my best wishes for whatever comes into your future; I am sure it would be the brightest of all.

Albert Doblas, we have shared pathways during this learning adventure from the very beginning: first degree, then master and now doctorate. I guess that almost ten years full of exams, lab practices and common difficulties have led to some kind of friendship. Future is always uncertain, but I keep my fingers crossed so we can share paths again.

This last year and a half has been extremely weird. Although I knew it before, it has helped me to realize how important family is. For that reason I want to express my most fond gratitude to my family, to those who are still here and those who are not, because any moment spent with you has become valuable and has defined in great measure how I am today. Thanks for everything.

Contents

Appendices

List of Figures

Abbreviations

AFM	**A**tomic **F**orce **M**icroscopy
APM	**A**mmonia-**P**eroxide **M**ixture
BOX	**B**uried **Ox**ide
BZK	**B**en**z**alkonium **C**hloride
cAFM	**C**onductive **A**tomic **F**orce **M**icroscopy
CCP	**C**apacitively **C**oupled **P**lasma
CGP	**C**ontacted **G**ate **P**itch
CMOS	**C**omplementary **M**etal **O**xide **S**emiconductor
CVD	**C**hemical **V**apour **D**eposition
DIBL	**D**rain-**I**nduced **B**arrier **L**owering
DSA	**D**irected **S**elf-**A**ssembly
EBDW	**E**lectron **B**eam **D**irect **W**riting
EBL	**E**lectron **B**eam **L**ithography
EDX	**E**nergy **D**ispersive **X**-rays Analysis
EFTEM	**E**nergy-**F**iltered **T**ransmission **E**lectron **M**icroscopy
EUVL	**E**xtreme **U**ltra**v**iolet **L**ithography
FD-SOI	**F**ully-**D**epleted **S**ilicon **o**n **I**nsulator
FIB	**F**ocused **I**on **B**eam
FET	**F**ield **E**ffect **T**ransistor
FinFET	**Fin** **F**ield **E**ffect **T**ransistor
GAA	**G**ate-**a**ll-**a**round
HF	**H**ydrofluoric **A**cid
HMDS	**H**exa**m**ethyl**dis**ilazane
HSQ	**H**ydrogen **S**ilses**q**uioxane
IBM	**I**on **B**eam **M**ixing
IC	**I**ntegrated **C**ircuit
IoT	**I**nternet **o**f **T**hings
IPA	**I**so**p**ropyl **A**lcohol

IRDS	**I**nternational **R**oadmap of **D**evices and **S**ystems
kMC	**K**inetick **M**onte-**C**arlo
LPCVD	**L**ow **P**ressure **C**hemical **V**apour **D**eposition
MIBK	**M**ethyl **i**so**b**utyl **k**etone
MOS	**M**etal-**O**xide-**S**emiconductor
MOSFET	**M**etal-**O**xide-**S**emiconductor **F**ield **E**ffect **T**ransistor
ND	**N**ano **D**ot
NDR	**N**egative **D**ifferential **R**esistance
NW	**N**ano**w**ire
NWFET	**N**ano**w**ire **F**ield **E**ffect **T**ransistor
PECVD	**P**lasma **E**nhanced **C**hemical **V**apour **D**eposition
PMMA	**P**oly**m**ethyl **m**eth**a**crylate
PVD	**P**hysical **V**apour **D**eposition
PVT	**P**rocess-**V**oltage-**T**emperature
QD	**Q**uantum **D**ot
RIE	**R**eactive **I**on **E**tching
RT	**R**oom **T**emperature
RTA	**R**apid **T**hermal **A**nnealing
RTCVD	**R**apid **T**hermal **C**hemical **V**apour **D**eposition
SCE	**S**hort **C**hannel **E**ffect
SED	**S**ingle **E**lectron **D**evice
SEM	**S**canning **E**lectron **M**icroscopy
SET	**S**ingle **E**lectron **T**ransistor
SiARC	**Si**licon **A**nti**r**eflective **C**oating
SOC	**S**pin **o**n **C**arbon
SOG	**S**pin **o**n **G**lass
SOI	**S**ilicon **o**n **I**nsulator
SS	**S**ubthreshold **S**wing
TCAD	**T**echnology **C**omputer **A**ided **D**esign
TEM	**T**ransmission **E**lectron **M**icroscopy
TEOS	**T**etraethyl **O**rthosilicate
TMAH	**T**etra**m**ethyl**a**mmonium **h**ydroxide
UTB-SOI	**U**ltra-**t**hin **b**ody **S**ilicon **o**n **I**nsulator

Thesis presentation

Motivation

The concept of Internet of Things (IoT) comprises all types of electronic devices, their functions, monitoring and communication with each other. It is an exponentially increasing network, mainly due to the convergence of multiple technologies such as wireless connection and embedded systems. The trend of this rapid expansion leads to a clear requirement for advanced computation and communication devices with significant low-power consumption.

Single Electron Transistors (SET) are extremely low-energy dissipation devices. However, SETs usually operate at cryogenic temperatures and present as well other challenging issues. In this context, SET and CMOS are complementary: SET outperforms in low-power consumption, while CMOS advantages like high-speed, driving, voltage gain and input impedance can compensate exactly for SET's intrinsic drawbacks. Therefore, unrivalled integration with high performance but low energy dissipation is expected for hybrid SET-CMOS architectures.

The roadblock for integrating SETs operable at room temperature into current CMOS technology is their controlled manufacturability. The needed technology to co-integrate SET and CMOS functions ultimately depends on the ability of new processes to address size and variation issues and to be costly affordable. For that reason, the development of novel methodologies to move forward the state-of-the-art technology is mandatory.

Device scaling has driven in semiconductor industry a continuous progress, first by reducing the dimensions of planar MOSFET and afterwards by exploiting the benefits of lateral configurations. A further increase in integration is given in vertically arranged transistors, which have been demonstrated with feasibility as an option for 15 nm technology nodes and beyond with sub-10 nm channel length devices. Hence, an additional impact is the combination of SET with vertical architectures.

Scope and objectives

The main part of this thesis has been performed in the framework of the IONS4SET EU project, whose main objective is to demonstrate the manufacturability of a room temperature operating SET in a CMOS compatible technology, and to fabricate a hybrid SET-CMOS demonstrator which can assess its potential for extremely low energy dissipation electronics. The SET component is based on a vertical configuration: a stacked $Si/SiO_2/Si$ nanopillar with a single Si nanodot in the oxide layer separating source and drain regions.

For the proper understanding of the work performed in this thesis, it is necessary to describe part of the work performed by the other partners of the project. Here, the main role of each partner is summarized, with detail of the section(s) that correspond fully to their work.

CEA-Leti:
Commissariat à l'énergie atomique et aux énergies alternatives, Laboratoire d'électronique des technologies de l'information

- All the processes related to pillar patterning and silicon nanodot self-assembly, both in bulk and in SOI substrates. In particular, all the processes described in sections 2.2.1 and 2.2.2.

HZDR:
Helmholtz-Zentrum Dresden-Rossendorf

- Predictive simulations for silicon nanodot implantation, as described in Appendix A.
- All the TEM structural characterization figures presented in this thesis were obtained at HZDR, including TEM-based EDX analysis.

FhG-IISB:
Fraunhofer Gesellschaft, Institut für Integrierte Systeme und Bauelementetechnologie

- Development of all the SET device simulators introduced in Appendix B.
- Managing the sacrificial oxidation for pillar size shrinkage described in section 2.2.3.
- Conductive AFM measurements presented in section 2.7.1.

CNR-IMM:
Consiglio Nazionale delle Ricerche, Istituto per la microelettronica e microsistemi

- Electrical characterization at room and low temperature presented in sections 2.7.2 and in Fig. 2.52 and Fig. 2.54 from section 2.7.3.

CSIC, IMB-CNM:

Consejo Superior de Investigaciones Científicas, Institut de Microelectrònica de Barcelona

- Integration of patterned vertical nanopillars towards fully contacted SETs.
- SET integration into CMOS technology.

The tasks of the IMB-CNM in the framework of the project are related to the main objectives of this thesis, which are described as follows.

(i) Development of an integration process for SET based on vertical silicon nanopillars, which can enable the effective generation of source, gate and drain electrodes.

(ii) Demonstrate the compatibility of the optimized CMOS processes with SET integration in terms of pillar integrity and nanodot stability.

(iii) Analysis of the different routes to address the integration of a hybrid SET-CMOS circuit, and adjustment of the available technology for monolithic fabrication of MOSFET and vertical SET.

(iv) Explore the suitability of vertically arranged transistors in terms of simulations.

Structure

The thesis is arranged as follows:

- **Chapter 1**: Introduction to the most relevant concepts regarding SET, FET and the nanofabrication techniques presented along the thesis.
- **Chapter 2**: Integration of SET in a vertical configuration, including the process optimization, the complete process sequence and the most significant electrical results.
- **Chapter 3**: Co-integration of the SET process in CMOS technology, including preliminary investigations in order to verify SET compatibility and the electrical characterization of FETs fabricated under these constraints.
- **Chapter 4**: Simulation of vertical nanowire-based FET and other vertically arranged configurations.

Chapter 1

Introduction

In this chapter a brief introduction to the evolution of microelectronic technology is presented, together with its milestone devices and main features. In this context, the exploration of new generation of devices is justified, and thus the devices studied in this thesis are described in terms of main characteristics and breakthrough potential. Physics and basic fundamentals for each device are introduced, followed by the fabrication techniques required for their process feasibility.

1.1 Overview of Moore's Law

Semiconductor industry has been strongly linked from the very beginning to the development of integrated circuits (IC) [1]. Since its invention in 1959, ICs were the basis for a wide new generation of functional devices which had the aim of improving quality of life in general by providing solutions to unsolved challenges. This has been remarkably expanded by adding more components in ICs, building in that way more complex and denser configurations. And the main drive for this trend is the miniaturization of its basic component: the Metal-Oxide-Semiconductor Field-Effect-Transistor (MOSFET). By reducing its dimensions, more efficient devices were obtained due to density enhancement, increasing significantly the economic benefit. In 1965, Goordon Moore envisioned the progression of this economic benefit in terms of integration density, stating the famous Moore's law [2]. Although it has been extensively reformulated along decades, originally the estimation was that increasing the integration density by a factor of two in a two-year period would reduce significantly the cost per transistor.

In order to maintain updated this economical tendency, new technology requirements for keeping MOSFET miniaturizing factor started to gain importance. Some scaling rules were proposed by

Dennard in 1974 [3], guidelines to obtain a gain in performance at the expense of size reduction on several transistor characteristics. These guidelines helped to scale the MOSFET gate length from 100 μm to 100 nm with a biennial factor of 0.7, which is known as the classical scaling.

Fig. 1.1 shows the progression of Moore's law and Dennard's scaling trend [4], along with the empirical data for minimum feature size and transistor density per microprocessor in each generation [5]. Note that the minimum feature size is commonly designated as process or technology node. Inset of the most relevant technology node devices are presented as well [6].

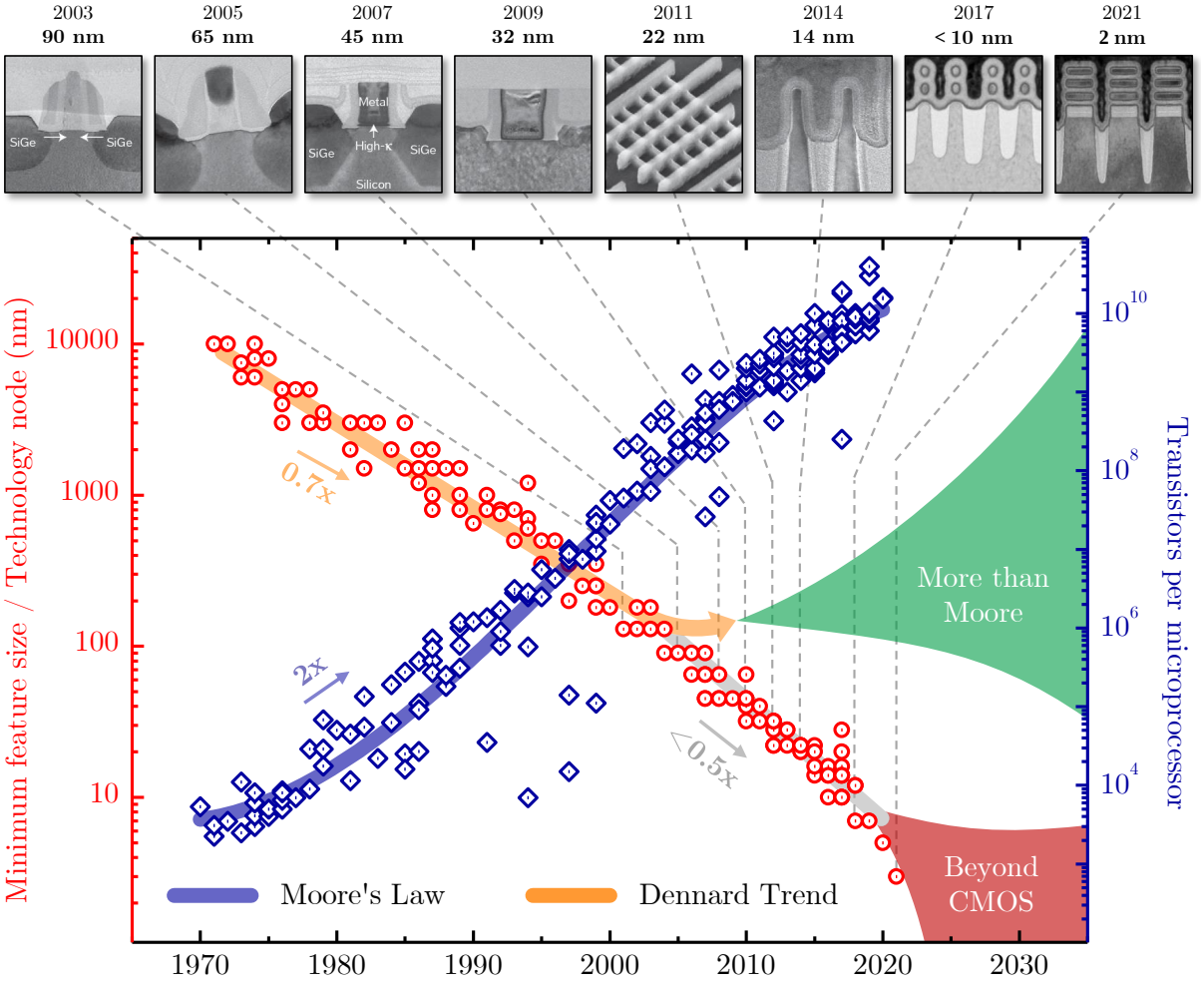


FIGURE 1.1: Evolution of number of transistor per microprocessor and their minimum feature size from 1970 to 2020; detail in the top row for the most significant technology nodes post-2000. Graph created with data from [5] and device images from [6].

From this representation, it can be observed that the original prediction of doubling the transistor counts every two years was a good estimation, still valid four decades later [7]. Regarding minimum feature size, the initial guidelines for device scaling were enough to keep the trend

until early-2000s; after that, new strategies had to be followed and different scaling rates were achieved, normally adjusted below a biennial factor of 0.5.

Transistors are essentially switches consisting of a source and drain electrodes and a gate that controls the electron flow in the channel through a thin oxide layer; this basic structure is the foundation of the Field Effect Transistor (FET), being the Metal-Oxide-Semiconductor (MOS) the most widely used configuration and the one depicted in Fig. 1.2.a. For the first decades, within the classical scaling, reducing the dimensions of gate length, channel width and effective oxide thickness was enough to satisfy the expected prediction.

However, in order to go beyond sub-100 nm nodes, relevant changes in terms of materials, processing technology and architecture designs started to become necessary. At this level, electrostatic integrity became a major issue which risked the continuity of classical scaling. One of the first attempts to increase MOSFET performance was to make the silicon channel as thin as possible. The approach was to build the channel on top of an insulating material, as Fig. 1.2.b shows. Ultimately, this lead to the creation of ultra-thin body silicon-on-insulator (UTB-SOI), known as well fully depleted SOI (FD-SOI) [8].

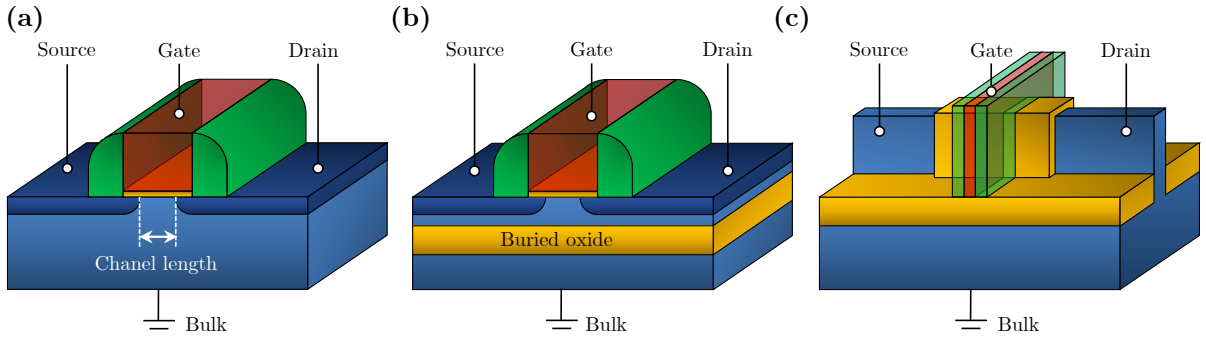


FIGURE 1.2: MOSFET scheme with its three main elements (a), in a FD-SOI substrate (b) and the FinFET evolution (c).

Some of the more notorious drawbacks that raised during sub-100 nm channel length scaling were: polysilicon gate depletion effects, increased gate leakage, high field mobility degradation or Short Channel Effects (SCE). Modern technology provided different approaches to address these challenges. For instance, by replacing polysilicon by metal as gate material, depletion effects were reduced; gate leakage was strongly mitigated by using high-k dielectric materials as gate oxide; and stressing layers were introduced in order to promote carrier mobility, compensating high field mobility degradation [9].

But regarding SCEs, it became very challenging to keep reasonable levels for gate lengths below 30 nm. This brought to a necessity for a change of paradigm in the MOSFET architecture,

in particular to keep effective gate control on the channel. An innovative solution was to turn the channel in a 3D structure, increasing the effective gate contact. This could be done by patterning a thin silicon structure shaped as a fin out of the plane of the device, in a way that then the gate could wrap over the three sides of the channel. This configuration is known as FinFET, depicted in Fig. 1.2.c, and provided a significant increment on control of the channel with respect previous generations [10].

The prediction of IRDS, a few years ago, defined at the end of the roadmap a gate length of 8 nm or less [11]. For maintaining good electrostatic integrity, channel width should be at least a third part of the channel length [9]; that is only a few nanometers. Therefore, the natural structure for the channel in the next generation of nanoelectronic devices will be most probably nanowires, either laterally or vertically arranged. Similar configuration than FinFET but using nanowires as conductive channel is the main core of lateral nanowire FET (Fig. 1.3.a). In this case, even higher gate control over the channel is achieved, due to its gate-all-around (GAA) configuration. Another related structure is the stacking of nanosheets for FET applications, which allows larger channel widths while keeping the GAA configuration [12], [13].

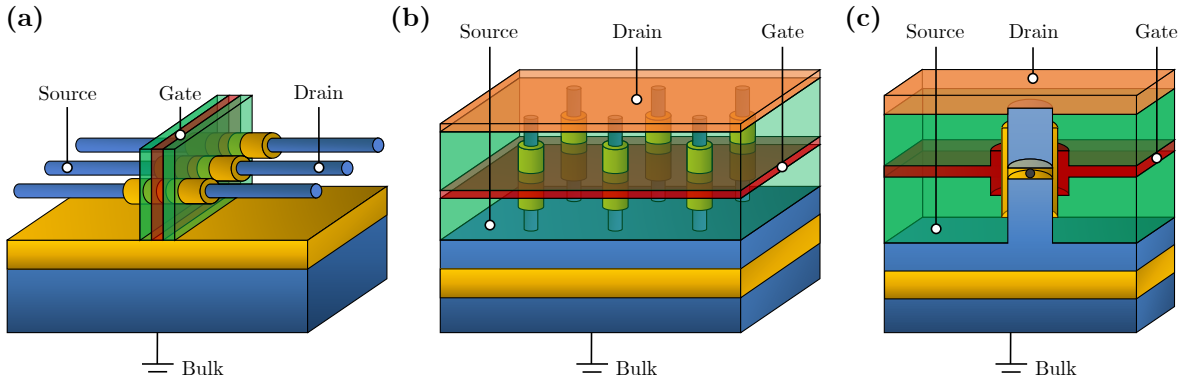


FIGURE 1.3: Schemes for laterally arranged nanowires FET (a), vertically arranged FET (b) and vertical SET (c).

Following the thrust of density enhancement, there is an obvious improvement by arranging nanowires in a vertical configuration instead of lateral (Fig. 1.3.b). In this framework, vertical architectures show a remarkable potential in terms of scalability and power consumption [14]. Note that in this configuration, with transistors being near the minimum feature size achievable, together with their maximum integration density, might represent a clear breakthrough in semiconductor industry. In addition, another benefit is the number of available methodologies for nanowire growth (e.g. epitaxial growth, vapour-liquid-solid process, directed self-assembly) [15], which do not always depend on lithography resolution limit or patterning selectivity.

Nowadays, semiconductor industry has already introduced some of these architectures into industrial production, such a FD-SOI and FinFET, and it is still exploring the viability of incorporating others as GAA-FET, either lateral or vertical. But as the achieved technology node is closer to the end of the roadmap, efforts have been focused on the development of new strategies and configurations which could move forward to further technologies [16].

As mentioned before, reducing gate length implies reducing the channel width; but reduced channel width entails lesser cross sectional area and hence lesser number of carriers. And lesser number of carriers means that the quantized nature of charge starts affecting the device characteristics. In the framework of conventional FET circuitry this represents a clear issue. However, by innovative device engineering this challenge could be turned into an advantage. In other words, this drawback can become an asset in devices whose functionality depends on the discreteness of the charge. And this is the case of Single Electron Transistor (SET), device proposed in 1986 [17] and widely studied since then. The main characteristic of this device is its charge transfer through single electron addition to the channel. The channel of the SET is a nanoscaled island separated from both drain and source by tunnel barriers; then the gate can control the electron tunnelling between these barriers, allowing conduction of single electron charges.

SET was initially proposed as a substitute for CMOS, representing the spearhead of the beyond-CMOS regime. However, as SET technology was developed, it started to be considered as a potential complement for CMOS elements, enabling a new generation of circuits and novel applications. Nevertheless, the low temperature required for its operation and the non-CMOS fabrication process have been major limitations for their complete integration. Another limiting factor is its intrinsic low output current, which forces SET to be implemented in hybrid circuit designs. An implementation of SET in vertical configuration can be given as well. Fig. 1.3.c represents a vertical silicon pillar, with a sandwiched thin oxide layer and a silicon nanocrystal embedded on it. This nanocrystal acts as a quantum island between source, the bottom part of the silicon pillar, and drain, the upper part [18].

In this work several of the already mentioned challenges are addressed. In Chapter 2, the integration of a SET in a vertical nanopillar is explored, paving the road for going beyond-CMOS once the end of the roadmap is achieved. Chapter 3 presents the cointegration of a SET-FET hybrid circuit device on state-of-the-art CMOS technology, exploring in that way the novel functionalities that lie within the more than Moore regime. In Chapter 4 vertical nanowire-based FET are studied by means of simulation and technology computer aided design. In that way, the elements for a complete vertically arranged SET-FET are separately analysed, with the final target of its future joined integration.

1.2 Field Effect Transistor

1.2.1 Metal-Oxide-Semiconductor

The modulation of the electrical conductivity of a semiconductor by the application of an external electric field was first described in 1930 [19], and it is the main element for the MOSFET operation [20]: a MOS capacitance between a body electrode and a gate electrode insulated from all other regions by a gate dielectric layer. As semiconductors have low density of electrons, when an electric field is applied it can penetrate into the material, modifying the conductivity near the surface. By adding two more electrodes connected to highly and equally doped regions, source and drain, separated by the body region, the complete MOSFET structure is described. These regions can be either p or n-type, but must be opposite to the body region. Fig. 1.4 shows the complete structure in the case of an n-type MOSFET (i.e. S/D regions doped as n-type). The combination of n and p-type is given in the design of Complementary Metal-Oxide-Semiconductor (CMOS), circuits in which both types of devices are fabricated and interconnected on the same substrate.

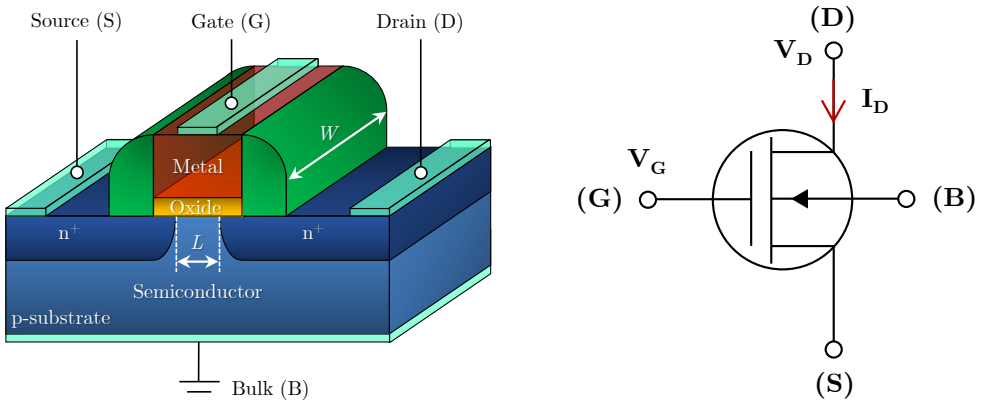


FIGURE 1.4: Scheme of an n-type MOSFET with all electrodes and corresponding circuit.

In order to understand MOSFET operation, first it is presented the behaviour when different bias are applied between gate and bulk electrodes in an ideal NMOS capacitor, with no trapped charge in the oxide and similar work functions for metal and semiconductor.

1. **Accumulation:** Positive bias is applied to the gate, $V_{GS} > 0$, and bulk is grounded. A large number of electrons are attracted to the oxide surface, and hence the concentration of electrons below the oxide is incremented with respect the rest of the semiconductor bulk. The Fermi level in the metal layer, E_{FM}, is pushed downwards bending the conduction band, allowing in turn the accumulation of majority carriers, electrons in this case.

2. **Depletion:** Negative bias applied to the gate, $V_{GS} < 0$. Electrons near the oxide layer are repelled, depleting the semiconductor below the gate. In this case there are not any free charges contributing to conductance; as the fixed donor charge remains in the depletion region, this region is positively charged.

3. **Inversion:** A larger negative bias applied to the gate, $V_{GS} \ll 0$. In this case electron concentration near the surface is still decreasing while the hole population increases; free holes are attracted near the oxide layer, which is named as inversion region.

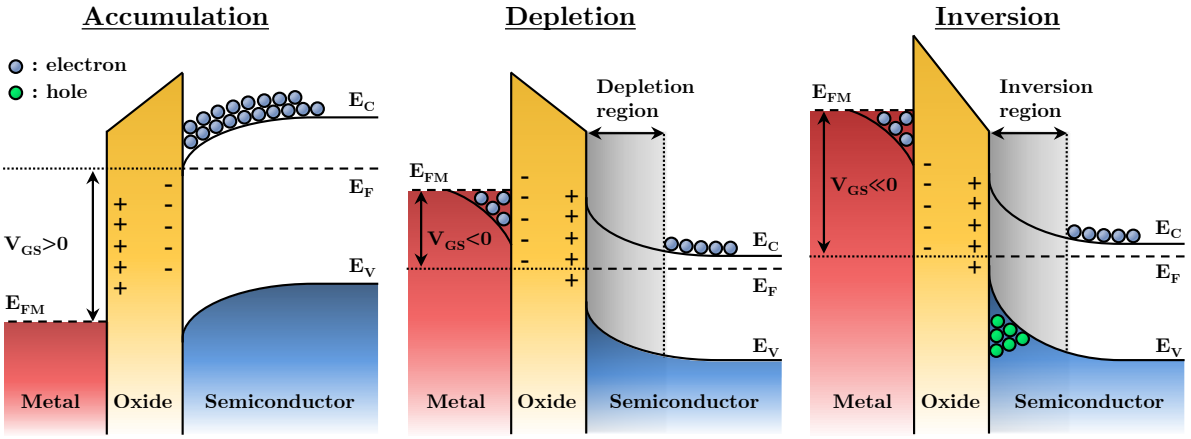


FIGURE 1.5: Schematic of the operation modes of an ideal NMOS capacitor: accumulation, depletion and inversion.

MOSFET operation modes are easily inferable from the MOS capacitor. If the drain is positively biased with respect source and bulk ($V_{DS} > 0$), then the current through the channel can be controlled. The minimum gate voltage (V_{GS}) required to create a conducting path between source and drain is known as threshold voltage (V_{Th}) and indicates the transition between weak and strong inversion. By controlling the gate and drain potentials, three operation modes can take place.

1. **Weak inversion:** When $V_{GS} < V_{Th}$, the inversion layer under the gate is not yet created and therefore the source-to-drain current is not enough to switch on the transistor.

2. **Linear region:** When a strong enough gate bias is applied $V_{GS} > V_{Th}$ and the drain voltage is $V_{DS} < (V_{GS} - V_{Th})$. In this case the inversion layer is created between source and drain; the conductance of this channel can be modulated by varying the gate voltage.

3. **Saturation region:** When $V_{GS} > V_{Th}$ and $V_{DS} > (V_{GS} - V_{Th})$. In this case the depletion region occupies the channel, allowing only a narrow path for the current. Beyond this point the current remains almost constant, independently of drain bias.

1.2.2 Current-voltage characteristics

From the current-voltage characteristics different parameters can be obtained, and these parameters describe in turn the overall performance of a MOSFET. Fig. 1.6 shows an example of output characteristics for a n-type MOSFET.

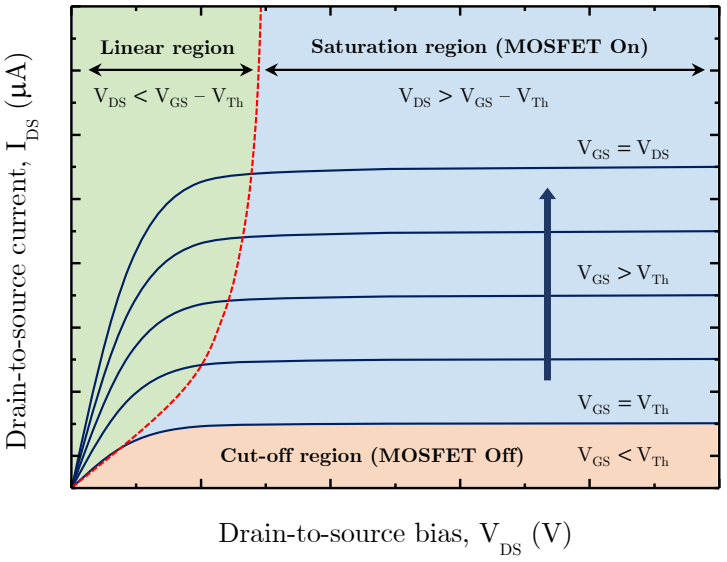


FIGURE 1.6: MOSFET $I_{DS} - V_{DS}$ curves with detail of the different operation modes.

The standard drain-to-source or I_{DS} current is described as follows

$$I_{DS} = \frac{W}{L} C_{ox} \mu_e \left(V_{GS} - V_{Th} - \frac{1}{2} V_{DS} \right) V_{DS} \tag{1.1}$$

for $0 \leq V_{DS} \leq V_{DSat}$, defined in saturation as $V_{DSat} \equiv V_{GS} - V_{Th}$. In the previous definition W/L is the ratio between channel width and length, μ_e the electron mobility and C_{ox} the oxide capacitance per unit area. Regarding the threshold voltage V_{Th}, it can be described as

$$V_{Th} = V_{FB} + 2\phi_F + \frac{\sqrt{2qN_A\varepsilon_{Si}\left(2\phi_F + V_{SB}\right)}}{C_{ox}} \tag{1.2}$$

where $2\phi_F$ is the surface potential, V_{SB} the source-to-body bias and $\sqrt{2qN_A\varepsilon_{Si}}/C_{ox}$ the body effect parameter. When V_{GS} is larger than V_{Th} the channel inversion charge is formed and the drain current increases with V_{DS}. If gate bias is incremented, a larger inversion charge density is created. In device saturation, $V_{DSat} = V_{GS} - V_{Th}$, the saturation current is then described as

$$I_{DSat} = \frac{W}{2L} C_{ox} \mu_e (V_{GS} - V_{Th})^2 \tag{1.3}$$

The transition from the ON state to the OFF state is gradual, and can be more clearly observed when plotting I_{DS} versus V_{GS} in logarithmic scale. Fig. 1.7 shows the transfer characteristics both in linear and logarithmic scale of drain current versus gate voltage when two different bias are applied at the drain electrode.

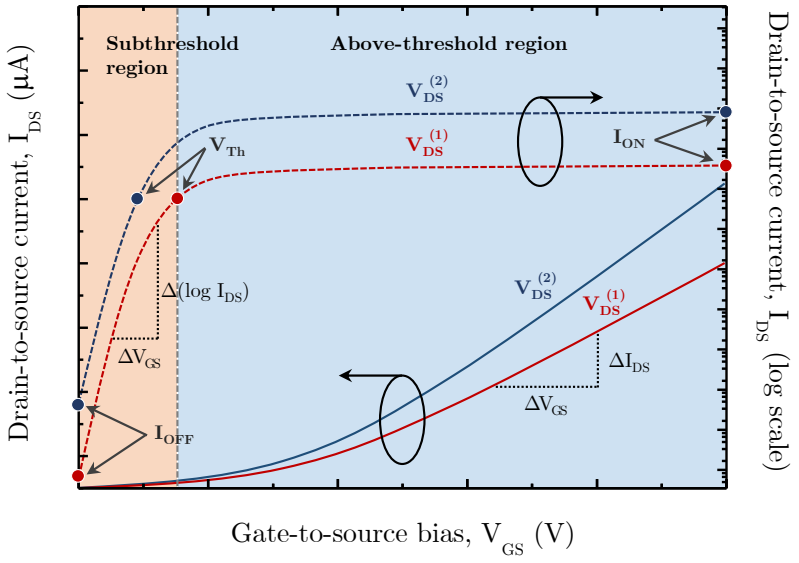


FIGURE 1.7: MOSFET $I_{DS} - V_{GS}$ curves with detail of the transfer characteristics in linear (left axis) and logarithmic scale (right axis) for two different drain bias.

Threshold voltage V_{Th} is one of the most significant parameters in a MOSFET performance; in simplified terms, it can be described as the gate voltage required to turn on the transistor. There are numerous methods to extract V_{Th}, being one of the most used the transconductance extrapolation method in the linear region [21], and the one used hereinafter.

The extraction of V_{Th} indicates the transition between two regions: subthreshold and above-threshold region. In the subthreshold region, drain current is described as

$$I_{DS} \propto \exp\left(\frac{qV_{GS}}{\kappa_B T}\frac{C_{ox}}{C_{ox}+C_{dep}}\right) \tag{1.4}$$

with the ratio $\kappa_B T/q$ being the thermal voltage, expressed in terms of the Boltzmann constant κ_B, the absolute temperature T and the electron charge q. And with C_{dep} as the depletion layer capacitance. A V_{Th} related parameter, the subthreshold swing (SS), describes how abruptly the transistor turns off with decreasing gate voltage; in other words, it describes how the channel surface potential can be controlled by the gate voltage.

$$SS = \ln(10)\frac{\kappa_B T}{q}\frac{C_{ox}+C_{dep}}{C_{dep}} \tag{1.5}$$

The minimum subthreshold swing can be obtained for $C_{ox} \to \infty$, $C_{dep} \to 0$ and $T = 300K$, giving a theoretical minimum value of 60 mV/dec at room temperature [22]. From the $\mathrm{I_{DS}} - \mathrm{V_{GS}}$ characteristics, SS can be empirically measured as the reciprocal value of the slope at subthreshold region in logarithmic scale.

$$SS = \frac{\partial V_{GS}}{\partial(\log I_{DS})} = \frac{\Delta V_{GS}}{\Delta(\log I_{DS})} \tag{1.6}$$

Another parameter that describes MOSFET performance is the transconductance g_m, described by the change in the drain current as small variations in the gate voltage occur while a constant drain bias is applied. Similarly to subthreshold swing, g_m can be extracted from current-voltage characteristics.

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}} = \frac{\Delta I_{DS}}{\Delta V_{GS}} \tag{1.7}$$

In a classical MOSFET (i.e. planar and with a channel long enough) the bottleneck in channel formation occurs far enough from the drain electrode, and hence originally V_{Th} is independent from drain voltage V_D. Nevertheless, for short-channel devices the drain is close enough to the channel, and therefore a high drain bias can modify the required voltage to create a conductive path between source and drain. This type of SCE is known as Drain-induced barrier lowering (DIBL), and can be described as the ratio between the differences of threshold and drain voltage in linear and saturation regime.

$$DIBL = -\frac{V_{Th}^{(2)} - V_{Th}^{(1)}}{V_D^{(2)} - V_D^{(1)}} \tag{1.8}$$

DIBL is one of the most common SCEs; other types of effects related with the reduction of effective channel length, and therefore accentuated during the MOSFET scaling, are described in the next section.

1.2.3 Short Channel Effects

The channel length is commonly taken as the gate length of the transistor. However, the actual channel length is obtained by subtracting the lateral diffusion of the source and drain junctions, and thus it cannot be accurately quantified. The limit from which SCEs start to appear is stated for channel lengths of comparable magnitude to the depletion layer widths of source and drain, δ_S and δ_D respectively. Hence, the behaviour of MOSFETS with $L \approx (\delta_S, \delta_D)$ used to differ significantly from long-channel transistors where $L \gg (\delta_S, \delta_D)$, effect which started to be extensively noticed beyond the 90 nm node [9].

Short channel effects occur when the depletion regions of source and drain invade the channel region. Fig. 1.8 illustrates this issue. There are two main reasons that explain the origin of this deformation of the depletion layer: the production of high electric fields in the channel region and the two dimensional potential distribution in the region.

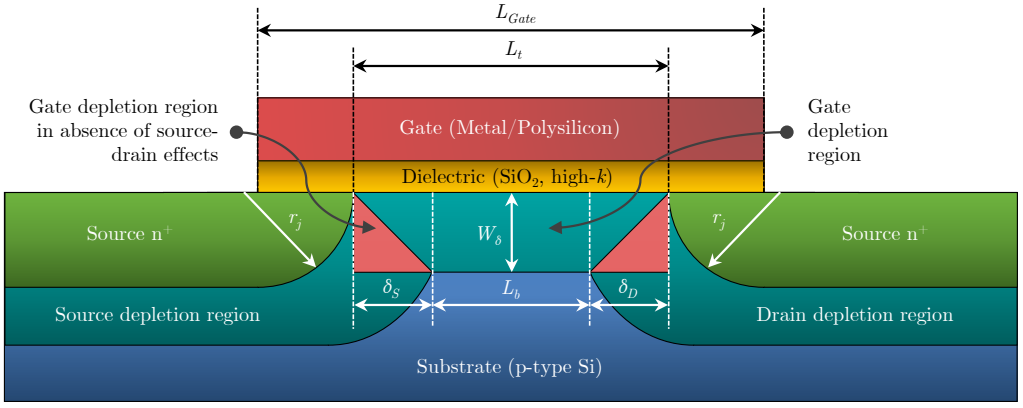


FIGURE 1.8: Scheme of the MOS interface with detail of effective geometry for short-channels.

SCEs may lead to a series of phenomena such as polysilicon gate depletion effect, velocity saturation, mobility reduction, threshold voltage roll-off, reverse leakage current rise, hot carriers effects or DIBL. Some of these effects are introduced as follows.

(i) Threshold Voltage Roll-off: The formation of an inversion layer below the gate dielectric is always preceded by the depletion of this region up to a certain depth W_δ, being source and drain voltage partially responsible of this depletion and gate voltage its main contributor. Small portions of the depletion layer charge are balanced by the charges in the source and drain regions. This effect increases the required charge for depleting the channel region, and thus the threshold voltage is also reduced by ΔV_{Th}. The already introduced DIBL is the drain voltage-induced decrement from coupling between drain and source, causing a depression in the potential barrier of the source-to-channel junction. And this depression at the source under the influence of a drain bias is the origin of this ΔV_{Th} difference.

In other words, if the barrier between source and channel is decreased, electrons move more freely in the channel region, and hence the transistor requires less voltage to achieve depletion and the transistor is switched on prematurely. In that process, V_{Th} is reduced and the gate loses control over the channel current. For that reason, the effective depletion region becomes trapezoidal instead of rectangular given no source-drain effects, as Fig. 1.8 shows.

For L_t and L_b being the parallel sides of the channel length under the contribution of source and drain to depletion, and r_j its diffusion curvature radius, it is obtained that

$$L_b = L_t - 2r_j \left(\sqrt{1 + 2W_\delta / r_j} - 1 \right) \tag{1.9}$$

And the induced variation in threshold voltage between a short-channel and a long-channel can be expressed as

$$\Delta V_{Th} \equiv |V_{Th}^{SC}| - |V_{Th}^{LC}| = - \left(\frac{qN_A W_\delta}{C_{ox}} \frac{r_j}{L_t} \right) \left(\sqrt{1 + 2W_\delta / r_j} - 1 \right) \tag{1.10}$$

where N_A is the substrate doping concentration. It can be observed that ΔV_{Th} can be compensated by modifying variables as doping concentration or oxide thickness, and therefore C_{ox}.

(ii) Polysilicon gate depletion: In the early stages of MOSFET technology, the metal electrode as gate material was replaced by a highly doped polysilicon layer [9]. But polysilicon, being a semiconductor, can deplete for electric fields high enough, and therefore the potential across the polysilicon becomes a large fraction of the supply voltage. This requires a further thinning of the oxide layer in order to maintain a constant electric field across the gate. Nevertheless, when the oxide thickness could not be reduced anymore, the only feasible solution was to increase the doping concentration of polysilicon, which implied as well other restrictions in terms of implantation. Another solution was the comeback of metal as gate electrode, which in turn resulted in lower gate resistance, absence of dopant penetration from gate into the channel and a reduced required thickness for gate insulator.

(iii) Velocity saturation: For reduced gate lengths the longitudinal electric field E_x increases. For low values of E_x the carrier velocity v_d respects a proportionality relation, but as E_x exceeds a certain value v_d saturates. This saturation is result of the increased scattering rate under high electric fields, and implies as well a lower V_{DSat} in short-channel MOSFETs.

(iv) Hot carrier effects: Hot carriers are defined as charged particles, either electrons or holes, which have acquired high kinetic energies upon the acceleration induced by the electric field present in the channel. As mentioned, as channel length is reduced the electric field in the channel is increased. And hence, due to their high energy, hot carriers might drift around other areas of the device such as gate dielectric or substrate, causing shift in the threshold voltage and degradation of the device transconductance.

(v) Random dopant fluctuations: The origin of this SCE is the statistical variations in dopant concentrations, which can become emphasized for reduced device areas. As a consequence, threshold voltage is influenced.

1.2.4 Non-ideal current-voltage characteristics

Besides SCEs, there are several non-ideal effects in the current-voltage characteristics of a MOSFET not intrinsically related with the channel length. Eventually, these effects can be deliberately forced to achieve a specific performance (e.g. low threshold voltage).

1. **Finite output resistance:** In an ideal MOSFET biased in the saturation region, drain current I_{DS} is independent of drain-to-source V_{DS}; in actual devices there is a nonzero slope between I_{DS} versus V_{DS} beyond the saturation point. For $V_{DS} > V_{DSat}$ the actual point in the channel at which the inversion charge goes to zero moves away from the drain terminal. In this case, the effective channel length decreases, and this effect is known as channel length modulation.

2. **Body effect:** It is assumed that the substrate or body terminal is always connected to source; however, in integrated circuits actually the substrate of all MOSFET channels is common. This means that a zero or reverse-bias voltage across the source-substrate junction exists, and thus a change in the source-substrate junction modifies as well the threshold voltage, in which is known as body effect.

3. **Subthreshold conduction:** For V_{GS} slightly below V_{Th} the drain current is not zero, in this case it is called subthreshold current. Although this effect is not significant when one single device is considered, if all the devices of an integrated circuit are biased just below the threshold voltage, then the power supply current will contribute significantly to power dissipation.

4. **Breakdown effects:** Different breakdown effects can take place in a MOSFET. If the applied drain voltage is too high, the drain-to-substrate junction may break and then avalanche multiplication occurs. For smaller devices, punch-through occurs when the drain voltage is large enough for the depletion region around the drain to extend completely through the channel to the source terminal. If the electric field in the oxide layer is large enough, then breakdown can also occur in the oxide.

5. **Temperature effects:** V_{Th} is a temperature dependant parameter since it decreases as temperature increases. Similarly, drain current increases with temperature.

1.3 Single Electron Transistor

Single electronics is based on the control and transport of single or small number of electrons. The main foundation of these devices is the quantization of electrical current by ultimately diminishing the channel dimensions into the nanoscale. Ideally, the channel can be considered as a small neutral metallic conductor, such as a sphere in vacuum. If two contacts are located close enough, they might act as electrons reservoirs to charge the sphere under a certain applied bias. In this case, the sphere is known as island and the contacts as source and drain. Note that there must be tunnel barriers between island and contacts, in order to confine the charge within the island while allowing electron transfer from the reservoirs [23]. If a third electrode is used to control the potential, as the gate terminal of a conventional FET does, then the Coulomb repulsion can be overcome and more electrons can be added into the island.

Then, a SET is a device which controls single electron transfer across an island by controlling the potential between source and drain through the tunnel barriers. Fig. 1.9 shows the scheme of a SET along with its equivalent circuit. Gate capacitance is represented as C_G; both source and drain tunnel junctions have capacitance and resistance denoted as C_S, R_S and C_D, R_D, respectively.

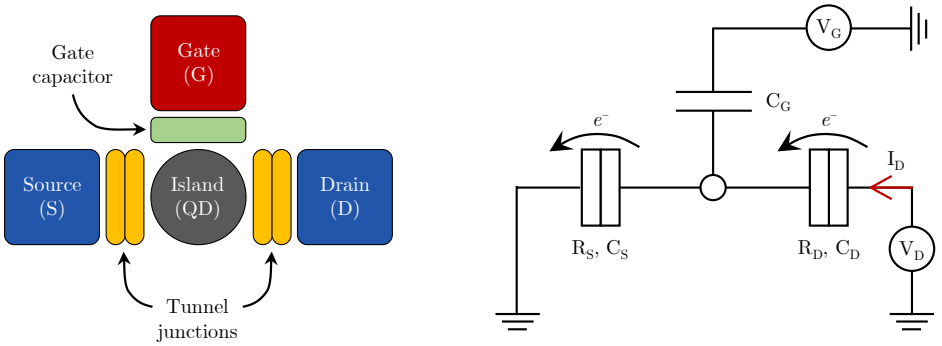


FIGURE 1.9: Scheme of the main parts of a SET and its corresponding electrical circuit.

1.3.1 Tunnel junction capacitor

A tunnel junction consists of two conducting terminals separated by a thin insulating space, acting as a tunnel barrier across which electrons can pass through by quantum mechanical transfer. It can be represented as an ideal capacitor with a tunnel resistance connected in parallel. Essentially, it is similar to a capacitor formed by two plates separated a certain

nanometric distance. In this case, the total capacitance is given by the amount of charge in the plates for an applied potential difference between them.

$$C = \frac{Q}{V} \tag{1.11}$$

The required energy to transfer an elementary charge dQ from one plate to another, compensating the repulsive force between them, is described by

$$dW = V dQ \tag{1.12}$$

And integrating the previous expression in the interval of the two plates charge, the next result is obtained.

$$W = \int_0^Q V dQ = \int_0^Q \frac{Q}{C} dQ = \frac{Q^2}{2C} \tag{1.13}$$

Which corresponds to the work done in order to transfer charge through plates. The parallel plate capacitor here introduced is a conventional configuration which can be used to illustrate the single electron transfer. It consists of two metallic plates of area A, separated by a dielectric material of dielectric constant ε_r a certain distance d. With ε_0 the permittivity in vacuum, the total capacitance is expressed as

$$C = \varepsilon_0 \varepsilon_r \frac{A}{d} \tag{1.14}$$

This expression can be used to estimate the order of magnitude of the required energy to transfer charges for different capacitor sizes. The energy required to transfer a single electron in a microscaled capacitor is much lower than in a nanoscaled capacitor. As a consequence, when a certain energy is applied in order to enhance electron transfer, a larger number of electrons will be transferred in the microscaled capacitor since single electron tunnelling requires a much lower energy. In summary, the required energy to transfer an elementary charge is extremely sensitive to the capacitor dimensions, being much more controllable in nanoscaled capacitors.

Thus, given a nanoscaled capacitor with a certain charge Q, if an electron tunnels across the dielectric the total charge on the second plate becomes $Q + e$. The energy stored in the electric field of the capacitor is then, from Eq. 1.13,

$$W = \frac{(Q+e)^2}{2C} \tag{1.15}$$

and the total change in energy in the capacitor system is

$$\Delta W = \frac{(Q+e)^2}{2C} - \frac{Q^2}{2C} = \frac{e}{C}(Q + e/2) \tag{1.16}$$

As it requires a certain energy to add a charge, $\Delta W < 0$; and thus $Q > -e/2$. With similar response for opposite polarity tunnelling, and combining with Eq. 1.11, it can be obtained the following requirement.

$$-e/2C < V < +e/2C \tag{1.17}$$

In that way, electron tunnelling is only possible if a bias large enough is applied between the plates of the capacitor, a voltage established in $|V| = |e|/2C$. For biases below this value there will be no electron transfer and thus current will stay zero.

1.3.2 Coulomb blockade

The cornerstone of single electronics is the concept of Coulomb blockade [24]. In simplified terms, the Coulomb blockade effect consists in the existence of a certain bias required to induce electron tunnelling between two conductive leads. In this context, the implementation of a Quantum Dot (QD) as quantum island becomes the ideal configuration for building the channel. Given its metallic/semiconducting behaviour and its few-nanometers size, the strong confinement of charges in these systems induces a discretization of the energy levels. Thus, the concept of a QD as quantum island is incorporated in the circuit depicted in Fig. 1.9 and in the following analysis.

SET is a Coulomb blockade structure in which gate action is provided; in other words, by controlling gate bias the single electron tunnelling can be modulated. Here, the single electron transfer due to Coulomb blockade event is described by means of energy band diagrams for different gate bias. Fig. 1.10.a illustrates the initial case in which no gate bias is applied ($V_G = 0$) and no electron tunnelling is possible from source into the QD neither from the QD into the drain. By applying a positive gate bias ($V_G > 0$), the Fermi energy levels of the QD are lowered. Otherwise, if a negative bias is applied, ($V_G < 0$) the Fermi levels are raised. Thus, by modifying the gate bias, the upper limit of the energy gap can be shifted above, below or aligned with the Fermi levels on the gate. An implication of this is the fact that the V_{DS} voltage required to induce current through a SET is dependent on the gate bias V_G.

If the V_G applied is not enough to align or surpass the Fermi level, there are no accessible energy levels for the electrons in the source; this is called the blocking state (Fig. 1.10.a). In this state, all levels on the island with lower energies are occupied; therefore, the number of electrons on the QD is fixed and it is in Coulomb blockade.

However, when a positive bias is applied on the gate the energy levels of the island are lowered, as mentioned. If $V_G < e/C$, but still enough to align with the Fermi level of the QD, then the electron from the source upper level can tunnel onto the island, occupying a previously vacant

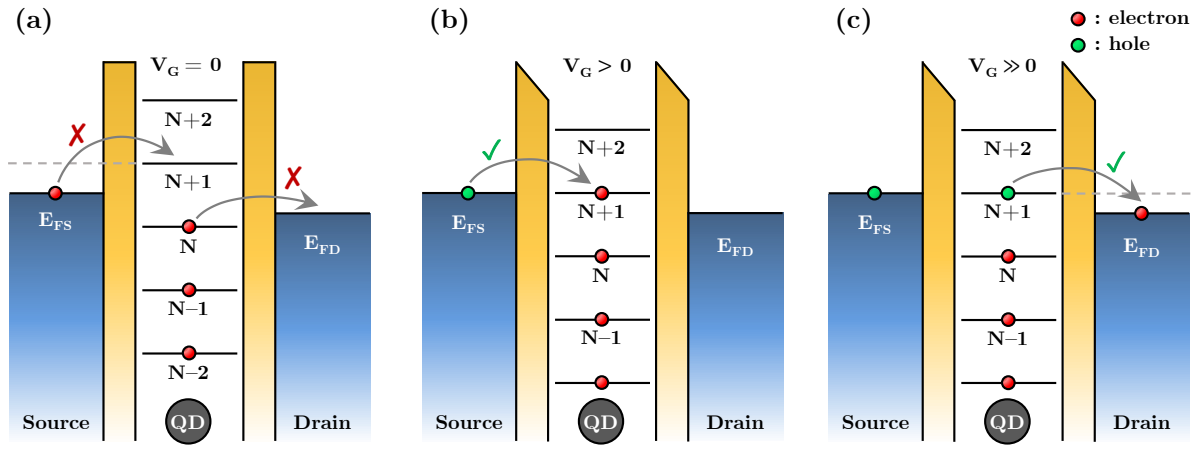


FIGURE 1.10: Energy band diagram of single electron transfer when no V_G is applied (a), a positive V_G is applied and thus electron transfer onto the QD takes place (b) and even a larger V_G is applied causing the previous charge to transfer onto the drain Fermi level (c).

level on the QD as Fig. 1.10.b shows. This opens the transmitting state. From the island, the electron can tunnel onto the drain where it inelastically scatters and reaches the upper Fermi level of the drain electrode (Fig. 1.10.c).

This intermittent electron tunnelling according to the gate bias applied, differs from the conventional continuous performance exhibited in standard MOSFET. In SET, the energy band diagram for small QD circuit presents a discretized behaviour, and thus electron tunnelling takes place in discrete voltage steps. This allows the detection of extreme low signals, and opens a wide variety of applications for single electronics [25].

1.3.3 Requirements for room temperature operation

As mentioned, the island must satisfy certain dimensionality boundaries in the nanoscale, so Coulomb blockade can be observed at room temperature [26]. In single electron devices the charging effect is measured by the electrostatic work required to move charges through the tunnel junction. If we consider again the example of a small neutral metallic conductor (e.g. a sphere in vacuum), when an electron is added then it raises its charge by $-e$; the recently adopted negative charge induces an electric field, which repels the addition of more electrons with a force $\vec{F} = -e\vec{E}$. Therefore, a certain work is required in order to add the next charge to the sphere.

$$W = \int \vec{F} = \frac{1}{2}CV^2 = \frac{e^2}{2C} \tag{1.18}$$

Which is essentially the same result than Eq. 1.13 for single electron transfer. This required work to add a charge is known as the charging energy E_c. Note that in the scale where single electron transfer can occur, quantum mechanical effects play as well a relevant role. For that reason, the kinetic energy E_k must be taken into account in addition to the charging energy. A third contributor must be considered: the thermal energy of source and island, denoted as $E_t = \kappa_B T$. Hence, the total energy for adding a single electron is described as follows.

$$E_a = E_c + E_k + E_t \tag{1.19}$$

It must be mentioned that for single electron transfer to take place, thermal energy must be always less than the charging energy, or otherwise the electron might transfer to the island via thermal excitation [27]. This is an important requirement for SET operation at room temperature.

$$\kappa_B T \ll \frac{e^2}{2C} \tag{1.20}$$

Note that the previous relation has implications in terms of the required dimensions of the island. Considering Eq. 1.14, Coulomb blockade effect will only occur in a capacitor with dimensions well within in the nanoscale. Therefore, this leads to the conclusion that Coulomb blockade is a phenomenon observable at room temperature only in nanoscaled devices.

In order to ignore higher order quantum processes such as co-tunnelling (i.e. multiple simultaneous tunnelling events), another requirement must be fulfilled. The first step to interpret these specifications derives from Heisenberg's uncertainty principle

$$\Delta E \Delta t \geq \frac{\hbar}{2} \tag{1.21}$$

where ΔE can be described as the charging energy obtained from Eq. 1.18. Regarding Δt, the charging time of the tunnel junction is given by $R_T C$, with R_T the resistance of the tunnel barriers. Therefore, the limit is established in a resistance for all the tunnel barriers much higher than the quantum resistance, in particular

$$R_T \geq \frac{\hbar}{e^2} \sim 4.1\, k\Omega \tag{1.22}$$

Leading to another requirement for the observation of Coulomb blockade effect at room temperature, a $R_T \gg 4.1\, k\Omega$. This is valid when considering the total time of electron tunnelling negligible with respect the other processes involved [28].

1.3.4 Current-voltage characteristics of SET

(i) $I_{DS} - V_{DS}$ characteristics

It is worth mentioning the current-voltage characteristics of multiple consecutive single-electron transfer through a QD in the discussed configuration (i.e. a QD separated by tunnel junctions from two electron reservoirs). After one electron has tunnelled from the reservoir through the tunnel barrier to the QD, then the energy of the QD is increased by $e^2/2C$, and thus the total energy becomes e^2/C. If then a second electron is to be added into the QD, it must compensate the repulsive force induced by the first one; in that case the required energy is $3e^2/2C$. This can be extended to any number of electron tunnelling events. A direct observable consequence is that the electric current flow occurs at discrete steps of voltage,

$$|V| > n\frac{|e^2|}{2C} \tag{1.23}$$

where n is the integer for a certain number of electrons. From this analysis it is observed a characteristic staircase behaviour when plotting $I_{DS} - V_{DS}$, as Fig. 1.11 shows, which is conveniently named Coulomb staircase.

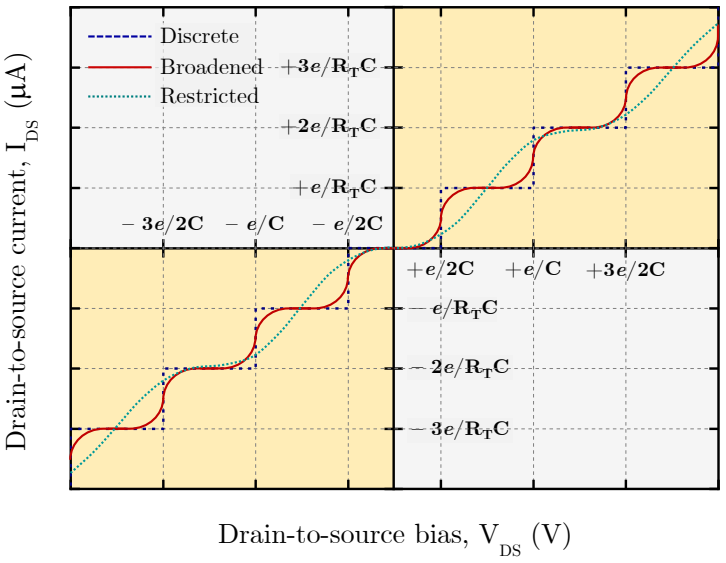


FIGURE 1.11: SET $I_{DS} - V_{DS}$ characteristics with the Coulomb staircase behaviour.

As already mentioned, the required work to add a charge is known as charging energy (Eq. 1.18). Tunnelling event takes place only when the energy level reaches the Fermi level, giving a sharp increase of current. Nevertheless, if the charging energy is larger, then the current increases gradually, broadening the steps of the staircase-like structure. Similarly, there is a restricted

limit for which the Coulomb blockade effect is still observable, before the coupling of tunnelling events affects the electrical characteristics [29]. All three cases are depicted in Fig. 1.11.

(ii) $I_{DS} - V_{GS}$ characteristics

If the applied drain-to-source voltage is very small or close to zero ($V_{DS} \approx 0$), then the application of a certain bias in the gate electrode can shift the charging energy levels of the island with respect the Fermi levels from source and drain. In that way, when the energy level reaches the source Fermi level, an electron can tunnel from source to island and consequently from island to drain. The SET is then in conduction or ON state. When the energy levels are not aligned anymore, there is no conduction and thus the OFF state is given.

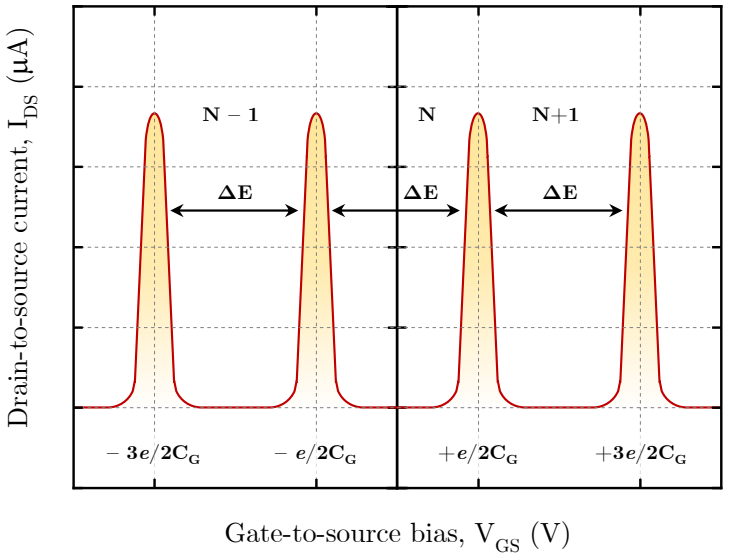


FIGURE 1.12: SET $I_{DS} - V_{GS}$ characteristics

Therefore, the $I_{DS} - V_{GS}$ characteristics of a SET show a periodically peaked curve where each peak represents the occupation number of the island by one single electron. This phenomenon is known as Coulomb blockade oscillations, and it is depicted in Fig. 1.12. In these oscillations, the peak has a separation defined as

$$\Delta V_{GS} = \frac{e}{C_G} \tag{1.24}$$

Therefore, when a bias $V_{GS} < e/C_G$ is applied, the periodic current peaks which are observed correspond to the tunnelling events taking place through the island from one stable region to another.

1.3.5 Stability diagram: Coulomb diamond plot

When both gate and drain bias are modified simultaneously, then the representation of drain current I_{DS} expressed as function of V_{GS} and V_{DS} is known as stability diagram.

As introduced in the previous section, I_{DS} becomes extremely sensitive of the gate voltage when the drain bias is fixed slightly above the threshold voltage for Coulomb blockade. Thus, the stability diagram representation becomes highly useful to illustrate the regions where there is no current through the device, given its capacitive characteristics.

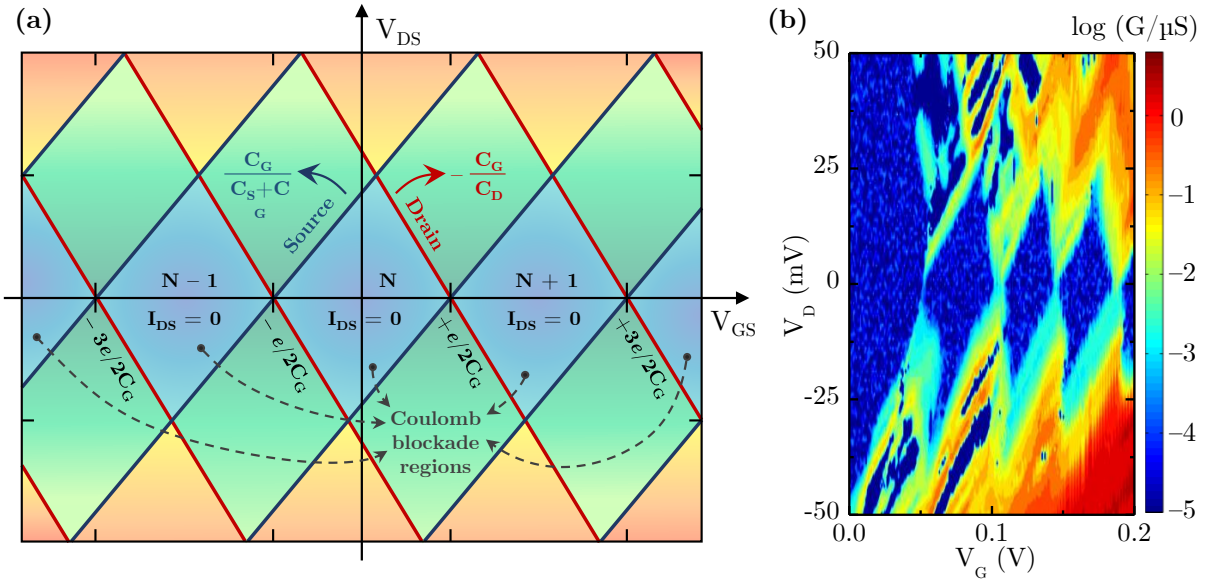


FIGURE 1.13: Schematic of the current stability diagram of a SET, or Coulomb diamond plot, with detail of the charging energy in V_{GS} and slope values calculation (a). Example of a Coulomb diamond plot experimentally obtained for a SET (b), from [43].

Triangular-shaped regions are formed defining the boundaries in which the island can be charged with a fixed number of electrons by the combination of drain and gate voltages. Considering the opposite sequence of tunnelling events, identical triangular regions are symmetrically obtained situated on opposite sides of the V_{GS} axis. Fig. 1.13 shows the combination of these regions with their symmetrical counterparts, defining diamond-shaped regions in the forbidden areas for tunnelling events; this representation is conveniently named Coulomb diamond plot.

The slopes that define the rhomboid regions are function of the capacitance of source, gate and drain [30]. Therefore, from the measured Coulomb diamond plot of a SET, the capacitance contribution of drain and source can be empirically calculated.

1.3.6 Fabrication requirements

Once the main fundamentals of SET operation are described, the next aspect that must be addressed is the requirements for it fabrication feasibility. There are some common requirements, independently from the architecture or materials properties, which must be properly fulfilled.

1. **Island:** The island size is the elementary factor that defines the right SET operation at room temperature. As it has been stated in previous sections, the QD must be below 5 nm in order to act as the SET island [31], [32].

2. **Tunnel barriers:** Tunnel resistance must be high enough to allow the quantization of the current in single electron transfer, and at the same time low enough to be surmountable by the applied gate bias. Tunnel resistance must be higher than the quantum resistance value of 4.1 $k\Omega$.

3. **Gate:** A good gate control over the channel is necessary. With that aim, materials which ensure good conductivity, usable as diffusion barrier and with good intermetal contact are specially alluring [33].

4. **Scalability:** In order to enable the further integration of room temperature SETs into CMOS technology, it is indispensable to develop and optimize reliable processes which can enable their fabrication at large scale.

5. **Hybrid circuits:** Although SET is operable at individual circuit level, most of its capabilities are based on hybrid circuits which could amplify its intrinsic low drive current [34]. For that reason, the design of hybrid circuits, and hence its CMOS compatibility, is another factor to be considered.

The potential of vertical arrangement with respect to planar structures has been already introduced. One specific requirement arise, mainly related to the necessity of defining thin planar intermetal layers. Conducting metal layers and insulating dielectric layers must be properly deposited, with controllable thickness, low roughness and suitable electrical characteristics. In addition, the deposition method must ensure the planarization around the nanostructure to be contacted.

1.4 Fundamentals of nanofabrication

In this section the main nanofabrication methods and techniques used during the development of this work are briefly introduced. The basic fundamentals and principles are presented for each technique, building the groundwork for the complete understanding of the following chapters. As a summary from [35], here the different methodologies used are classified in lithography, etching, material growth and characterization techniques.

1.4.1 Lithography

(i) Electron Beam Lithography (EBL)

Electron Beam Lithography (EBL) is an automated lithography technique used to directly write custom structures in an electron-sensitive resist previously deposited. The EBL equipment is formed by an electron writer, step motors for stage positioning, ampere-meters in the range of detectable pA for beam current measuring, and controlling software. Electron source are based either on thermionic emission (electrons excited by means of heat) or field emission (electrons excited by means of high voltages). Typical energy values for e-beam lithography are 10−100 keV, with beam current in the order of pA and spot size of few nm. Another critical factor influencing the pattern is the energy control and dose of the electron beam.

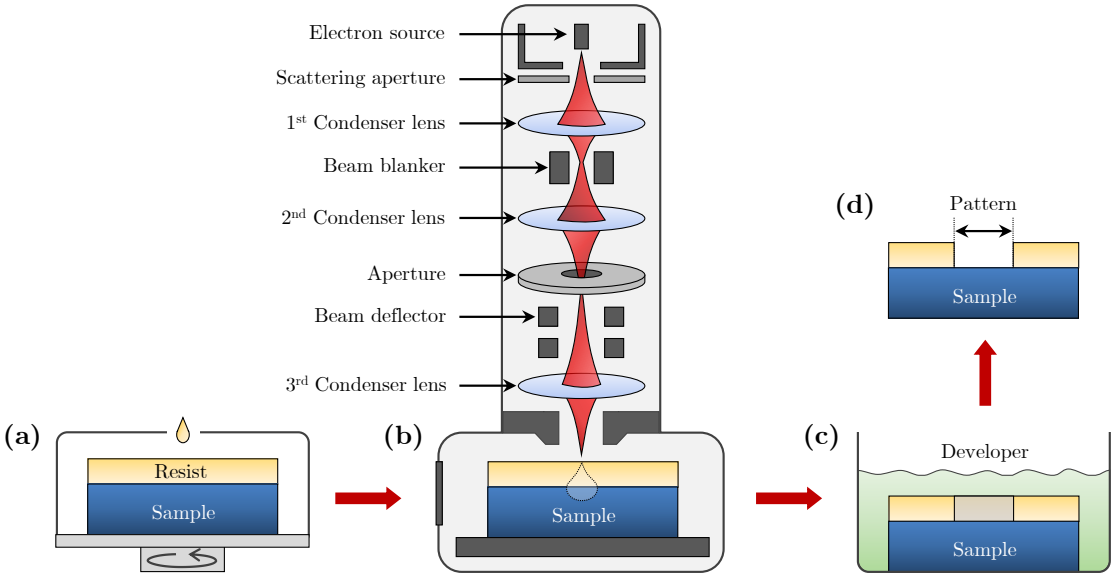


FIGURE 1.14: Scheme of the steps of an EBL lithography process: resist spin-coating deposition (a), electron exposure with detail of the main parts of the EBL equipment (b), developing (c) and resulting pattern (d).

The common way of procedure for EBL is: an electron-sensitive resist is deposited by means of spin-coating in a substrate (Fig. 1.14.a); a finely focused electron beam performs a planar scanning over the surface (Fig. .b), modifying the chemical bonds of the resist; finally, by immersion in a developer the patterned features can be either removed o maintained depending on the resist type (Fig. 1.14.c), resulting in a pattern designed on the resist (Fig. 1.14.d).

In positive tone resists, secondary electrons from inelastic collisions cause chain scission so that the exposed region dissolves in the developer. Negative tone resist, instead, react to electron exposure by cross-linking of the chain, and thus secondary electrons induce in turn a solid-state polimerization which endures the developer [36]. Polymethyl methacrylate (PMMA) is a commonly used positive resist with sub-10 nm resolution [37], usually followed by the deposition of a certain material or by an etching process. As negative tone resist, hydrogen silsesquioxane (HSQ) has shown a remarkable potential for the patterning of 5 nm structures [38], [39]. In this work, unless said otherwise, PMMA and HSQ are the resists used for positive and negative patterning, respectively.

(ii) Optical lithography

Optical lithography uses optical radiation to define patterns in a photosensitive material; chemical and physical properties are modified due to exposure, and therefore its solubility to a certain solvent is also affected (Fig. 1.15). The working principle is similar as in EBL, but in this case the exposure is performed by light radiation through prefabricated optical masks: a substrate usually made of glass or quartz, which is transparent for the wavelength of the optical radiation in the pattern design. Therefore, optical lithography resolution is limited by light diffraction.

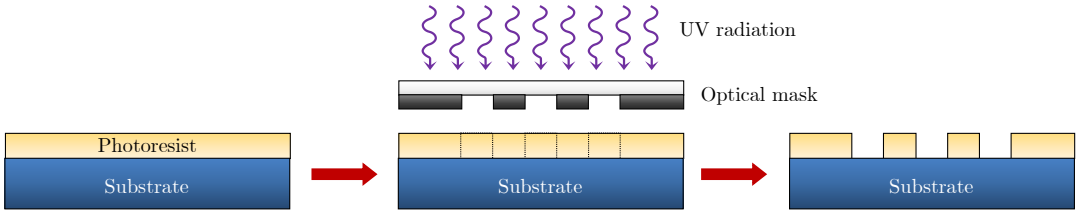


FIGURE 1.15: Scheme of a standard photolithography process.

In comparison with optical lithography, EBL achieves much higher resolution since it does not have the limiting factor of light wavelength dependence. However, EBL presents other limitations such as proximity effect (i.e. overlapping of backscattered and secondary electrons in the substrate, forming neighbouring features), or lower throughput with respect optical lithography.

1.4.2 Etching

(i) Wet etching

Wet etching is a material removal process that uses liquid chemical as etchant to remove or reduce a certain material from a substrate. If local etching is aimed, then a specific resist pattern or mesh must be previously defined by lithography process or similar. Wet etching consists in the chemical removal of surface material by means of chemical reactions. Once the reactant reaches the material surface, multiple chemical reactions take place, consuming both the original reactant and the etched material to form new products. Wet etching can be isotropic or anisotropic; when isotropic, etching material can penetrate underneath the mask. Fig. 1.16 illustrates a wet isotropic etching process on silicon through a mask.

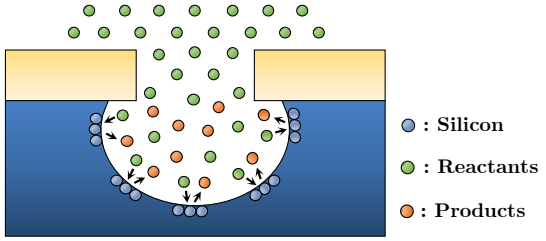


FIGURE 1.16: Scheme of a silicon substrate with patterned mask after wet etching process

(ii) Reactive Ion Etching (RIE)

In dry etching, the material removal is achieved by means of plasma or etchant gasses. The reaction can utilize high kinetic energy of particle beams, chemical reaction or a combination of both. Physical dry etching requires high kinetic energy particles to physically attack the atoms that constitute the surface material, which leave the substrate with no chemical reaction taking place. On the other hand, chemical dry etching does not use liquid chemical reactants as in wet etching, but involves a chemical reaction between etchant gasses and the surface.

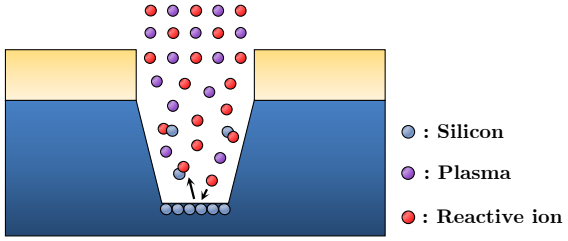


FIGURE 1.17: Scheme of a silicon substrate with patterned mask after RIE process.

Reactive Ion Etching (RIE) uses a combination of both physical and chemical mechanisms to remove materials. Fig. 1.17 illustrates a specific case of RIE process in a silicon substrate. RIE is much more anisotropic than wet etching, and therefore higher resolution can be obtained. Nevertheless it has the drawback of being much less selective.

1.4.3 Material growth

(i) Chemical Vapour Deposition (CVD)

Chemical Vapour Deposition (CVD) is a material processing technique used for the deposition of thin films on a substrate. The main process flow is as follows: one or more gaseous precursors are transported to the reactor chamber; by means of thermal activation or plasma discharge, the molecules of the gaseous reactants dissociate and react in vicinity of the substrate material. Thus, thin films are formed by chemical reaction on the substrate. Fig. 1.18 shows the scheme of a standard CVD equipment.

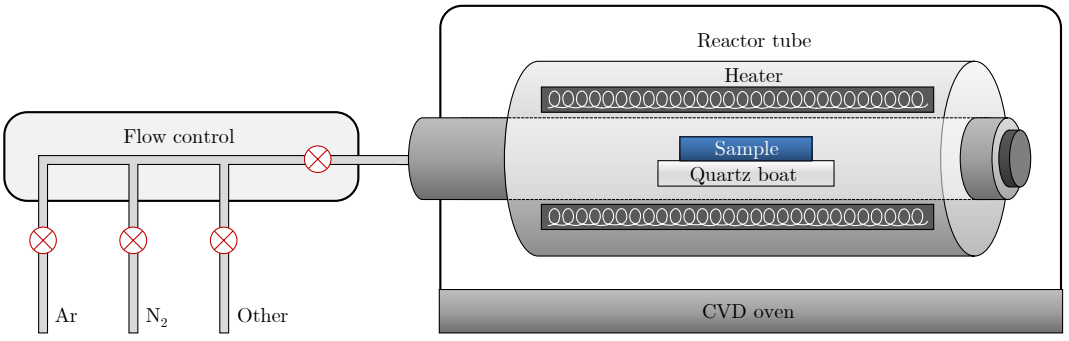


FIGURE 1.18: Components of a CVD equipment.

CVD can also be used for the deposition of high quality solid materials, such as silicon, oxides or oxynitrides. Moreover, it is a feasible methodology for the growth of nanowires, nanofibers [40] and carbon-based structures [41]. A wide variety of CVD equipments can be found. Some examples are: low-pressure CVD (LPCVD), performed at sub-atmospheric pressures; plasma-enhanced CVD (PECVD), which uses plasma in order to favour the chemical reaction rates of the precursors; and rapid thermal CVD (RTCVD), based on the fast heating ramps at the same time than the CVD process in order to reduce the gas-phase reaction that may lead to particle formation.

(ii) Physical Vapour Deposition (PVD)

Physical Vapour Deposition (PVD) is a group of processes used for the thin layer deposition of a wide variety of materials, such as metal, semiconductor, insulator or ceramic. This layer is achieved by means of condensation of the vapours of a given precursor on the substrate. The PVD deposition process is split in three main steps, usually performed under high to ultra-high vacuum environment: vaporization of the crucible which serves as material source, transport to the substrate location and condensation on the substrate.

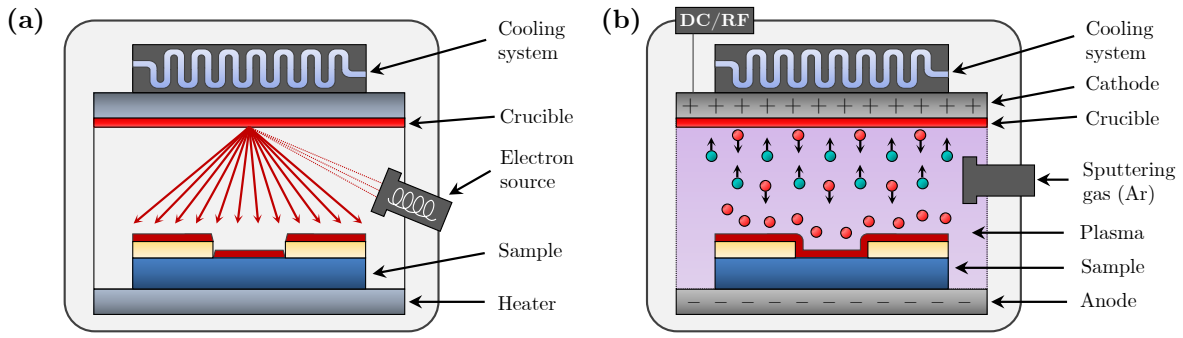


FIGURE 1.19: The two main PVD processes: thermal evaporation by electron source (a) and sputtering system (b).

There are two main forms of PVD process: thermal evaporation and sputtering. In the first, the energy is supplied either through resistive heating or electron beam source. Fig. 1.19.a shows the basic elements of a thermal evaporation equipment by electron source. Through resistive heating a solid material is evaporated in high vacuum chamber until vapour pressure is produced, and thin films are deposited over the substrate.

In the case of sputtering, vapours are originated from the physical bombardment of the crucible precursor. First, a certain amount of ions of an inert gas, such as argon, are admitted into the vacuum chamber. An inter-electrode voltage induces an electric field, which ionizes the sputtering gas and creates a plasma between the plates. The cathode in which the target material is placed is kept at a negative potential relative to the substrate, and thus the accelerated ions are targeted towards the crucible. The impacting ions cause the removal of atoms from the crucible, which rapidly travel to the substrate where, after condensation, form the thin film of the target material over the substrate. Fig. 1.19.b illustrates the sputtering system and process, with detail of the conformal layer deposited over the sample.

1.4.4 Characterization techniques

(i) Atomic Force Microscopy (AFM)

Atomic Force Microscopy (AFM) is a characterization technique based on recording the interaction of a very sharp tip with the surface of the sample, providing information of its topography with nanometer resolution. Typical vertical resolution is 0.1 nm, and lateral resolution around 3 nm [42]. The AFM probe is formed by a flexible cantilever usually made of silicon or silicon nitride, with a sharp tip in the extreme, which presents a conical or pyramidal shape and a 3−20 nm radius curvature.

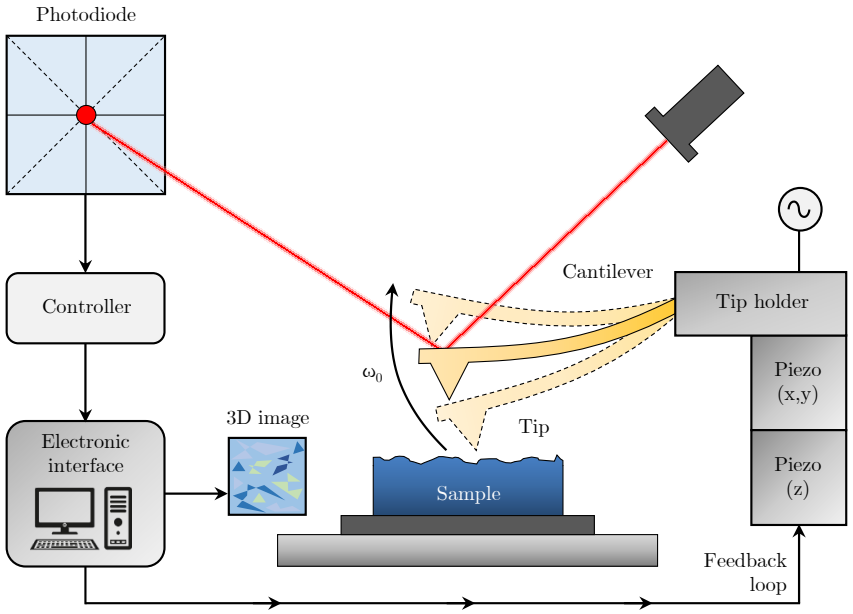


FIGURE 1.20: Diagram with the main parts of an AFM equipment in dynamic operation mode.

There are different operational modes for AFM. In this work, all measurements are performed in tapping or dynamic mode. Fig. 1.20 shows the main parts of an AFM for dynamic operation mode. A mechanical ac oscillation is forced in the cantilever, so it oscillates near its resonance frequency; a laser is focused on top of the tip, and its reflection is detected by a photodiode. When the tip approaches a topography change, the interaction force between tip and sample is modified, either in an attractive or repulsive way, and this variation is sensed by the tip which forces a change of the resonance frequency. By a feedback mechanism, the amplitude of oscillation is kept constant by piezoelectric controllers in the probe tip holder. In that way the distance between tip and surface is recorded at every point during the scanning, forming a surface map of the sample as Fig. 1.21.a illustrates.

(ii) Scanning Electron Microscopy (SEM)

Scanning Electron Microscopy (SEM) is a characterization technique based on the scanning of the sample by means of an electron beam. Similar as EBL (Fig. 1.14.b), but without the writing capabilities, SEM is essentially formed by a source of electrons, which are accelerated and pass through a combination of lenses and apertures. The resulting beam scans the sample, inducing the emission of high-energy backscattered and low-energy secondary electrons during its interaction with the sample. Fig. 1.21.b provides an example of tilted SEM image.

In addition, SEM equipments can be complemented by other characterization tools which enable further analysis, such as Energy Dispersive X-Ray Analysis (EDX). This technique is based on the observation of the X-rays emitted from the sample as a consequence of secondary electrons leaving the sample, and can provide information about its chemical composition.

(iii) Transmission Electron Microscopy (TEM)

While SEM creates an image by detecting reflected electrons, Transmission Electron Microscopy (TEM) uses the electrons that actually pass through the sample. For that reason, TEM provides more information about the inner structure of the sample, such as crystal structure or morphology. TEM uses a beam of high-energy electrons which are targeted to the sample, pass through the solid, and are collected again.

The sample must be thinned down to 100 nm or even less. This represents a clear issue for TEM imaging, which is often addressed by using mechanical polishing or Focused Ion Beam (FIB) for sample preparation. An additional challenge is to overcome the derived artifacts induced during the sample thinning. In the framework of this thesis, TEM becomes the cornerstone of the characterization analysis due to the small features of the SETs.

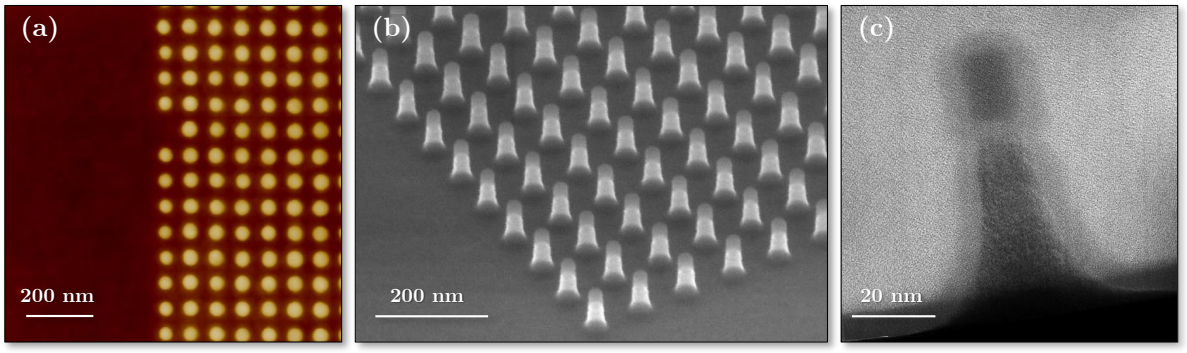


FIGURE 1.21: Example of AFM (a), SEM (b) and TEM (c) images of vertical nanopillars.

1.5 Conclusions

In this chapter the most relevant concepts of a vertical SET and its integration into CMOS technology have been presented, from a theoretical point of view, with the aim of stating the basis for the following chapters.

First, the potential of vertical structures in the framework of device scaling has been introduced: vertically arranged nanowires represents a potential candidate for future Moore's law, given its GAA and density enhancement. Moreover, SET shows a remarkable potential for the design of next generation of nanoelectronic devices beyond CMOS, and has as well great capabilities for its combination into hybrid circuits. Nevertheless, its integration into CMOS technology and its room temperature operation still give space for improvement.

With the perspective of enabling the process fabrication of vertically arranged FETs, the concepts of MOS capacitor and standard MOSFET current-voltage characteristics have been described. In addition, some of the most notorious short channel related effects are presented.

Regarding SET, the fundamental concepts of tunnel junction and Coulomb blockade have been presented. SET electrical characteristics are schematically shown as well. Afterwards, the main requirements for vertical SET fabrication are briefly discussed.

Finally, the most relevant fabrication methods used for the development of the mentioned devices are briefly overviewed.

Chapter 2

Integration of vertical Single Electron Transistor

In this chapter the integration process of a vertical Single Electron Transistor (SET) is presented. It starts with the patterning of a $Si/SiO_2/Si$ pillar and the Si nanodot (ND) assembly on the embedded oxide layer. Afterwards, the chapter is centred on the optimization of the integration process towards the fully contacted device.

2.1 Introduction

As introduced in Chapter 1, the core element of single electron devices (SED) is the quantum island. A quantum dot (QD) can act as a conductive island, since it can be charged by direct tunnelling of a single electron from the drain terminal. The electric field induced by this first electron causes a Coulomb force, which prevents from any further charge transfer. Through the application of a bias in the gate electrode, this electric field can be modified, and in turn the tunnelling from drain to the QD and from QD to the source can be controlled very sensitively. For that reason, SET has been extensively considered for low power consumption and signal amplification devices [43], [44]. Their power dissipation is several orders of magnitude lower than most advanced MOSFETs [45], mainly due to their reduced source-drain voltage and extremely low current operation.

In the past, single electron transfer was only observable at cryogenic temperatures [46]. The reason is that room temperature operation is restricted by the QD size. This was already described in section 1.3.3, and it is related to the charging energy of the island as capacitor. However, it

has been proved recently that for QDs smaller than 5 nm, SET can operate at room temperature [31], [32]. Additionally, the QD alignment with respect source and drain is another critical aspect. Tunnel junctions of 3 nm or less is another constraint for room temperature operation, in this case due to the required quantum resistance for single electron transfer. Tunnel junctions must be resistive enough to allow charge confinement in the QD, while allowing the overcoming of this tunnel barrier through gate bias manipulation. As observed, all these requirements pose extreme challenges on current semiconductor technologies. Thereby, it is clear that the roadblock for integrating SET into CMOS technology is its controlled manufacturability.

In this framework, an innovative solution is explored: a fabrication process based on the ion-irradiation-induced self-assembly of Si NDs embedded in a very thin thermally grown SiO_2 layer. In this configuration, the Si ND acts as QD, and the oxide layer in which it is confined stands for both tunnel junctions. This complex self-organization mechanism can be realized by phase separation of metastable SiO_x into Si and SiO_2 under a certain geometric constraint. And the geometric constraint is in this case achieved by embedding a SiO_2 layer into a Si nanopillar [18]. In that way, given a $Si/SiO_2/Si$ stack, by means of ion beam mixing a finite volume of SiO_2 is brought into a metastable SiO_x phase (with $x < 2$). Afterwards, after pillar patterning, this metastable phase undergoes a phase separation ($SiO_x \rightarrow Si + SiO_2$) during annealing at high temperatures (1050°C). Given the geometric constraints of the vertical nanopillar stack, the self-assembled generation of Si NDs takes place in the embedded SiO_2 layer [47]. Thereby, by reducing enough the nanopillar diameter, a single Si ND can be finally embedded in the oxide layer. Process conditions for pillar patterning will be presented in more detail in next sections, and Si ND implantation is summarized in Appendix A.

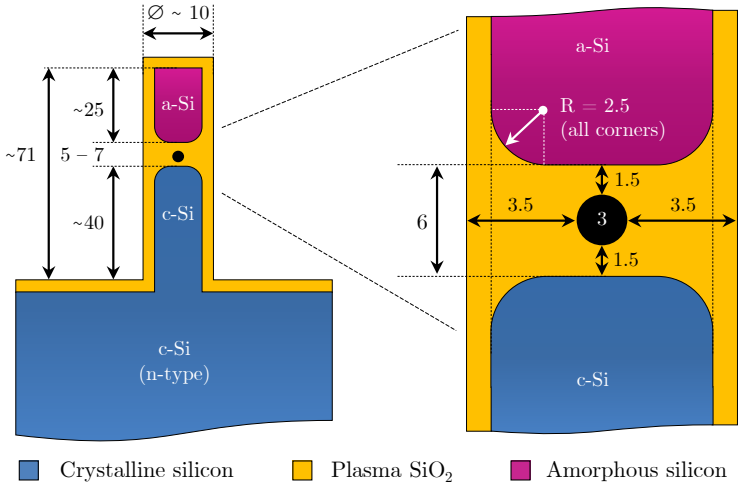


FIGURE 2.1: Sketch of the patterned $Si/SiO_2/Si$ pillar, with detail of the Si ND located within the embedded SiO_2 layer. All dimensions are in nanometers.

Fig. 2.1 illustrates the nominal dimensions in nanometers for the patterned pillar and the assembled ND located in the oxide layer. As mentioned, this vertical configuration fulfils the two main requirements towards the functional SET at room temperature:

- **QD size:** By varying the oxide thickness, the ion irradiation fluence and energy and the annealing conditions, the size of the ND can be controlled in the range of 2−4 nm.
- **Tunnel junction:** The tunnel junction thickness between the Si ND and the lower and upper part of the pillar can be tuned according to the ND size and the embedded SiO_2 thickness.

In order to study the feasibility of SETs based on the vertical configuration depicted in Fig. 2.1, device simulations are performed at FhG-IISB. These simulations consider different geometrical constrains such as pillar diameter, QD size, embedded oxide thickness and tunnel junction distances. More details of the device models and resulting electrical performance when modifying each parameter are presented in Appendix B. Results indicate that QD sizes around 3 nm are the most suitable for SET operation at room temperature, while tunnel junctions should not exceed the 2 nm. Concerning pillar diameters, it is observed that for values larger than 16 nm with just one single Si ND, the observation of Coulomb oscillations are significantly hindered. In next sections other considerations regarding pillar diameter and multiple Si NDs will be described.

Following pillar patterning and Si ND implantation, the next aspect to address is the complete integration process. Fig. 2.2 illustrates the resulting device: a fully contacted nanopillar where all electrodes are placed in a multiple planes arrangement, with insulating layers in between. The most challenging architecture features of the device are highlighted and described in more detail as follows:

(i) **Thin gate oxide around the pillar:** An oxide layer around the sides of the pillar is necessary for the SET operation. It must be thick enough to isolate from drain and source regions, and thin enough to allow gate control of the energy levels of the QD.

(ii) **Gate aligned with the embedded oxide:** A gate-all-around (GAA) surrounding the pillar must be properly defined, placed at the same height than the embedded oxide layer.

(iii) **Good electrical intermetal contact**

(iv) **Effective drain-gate separation:** The intermetal layer between electrodes must satisfy adequate insulating characteristics in order to prevent current leakage. At the same time, its thickness is limited by the dimensions of the upper part of the pillar.

(v) **Top oxide removal:** The oxide layer grown around the pillar must be locally removed on top of the pillar to obtain a good drain-pillar contact.

In view of all these requirements, some considerations regarding the process flow must be done. The material used as gate electrode is titanium nitride (TiN), due to its electrical conductivity, well established thin film deposition technology and CMOS compatibility [48]. Since in this case it is deposited by sputtering [49], and thus in a conformal way, TiN layer must be removed from top of the pillar in order isolate the gate terminal from the drain. Regarding the drain electrode material, for contacting n-type silicon nanowires nickel is the most suitable candidate to obtain good ohmic contact [50], [51]; in some cases, also Ni-alloys or Ni-silicides are used [52].

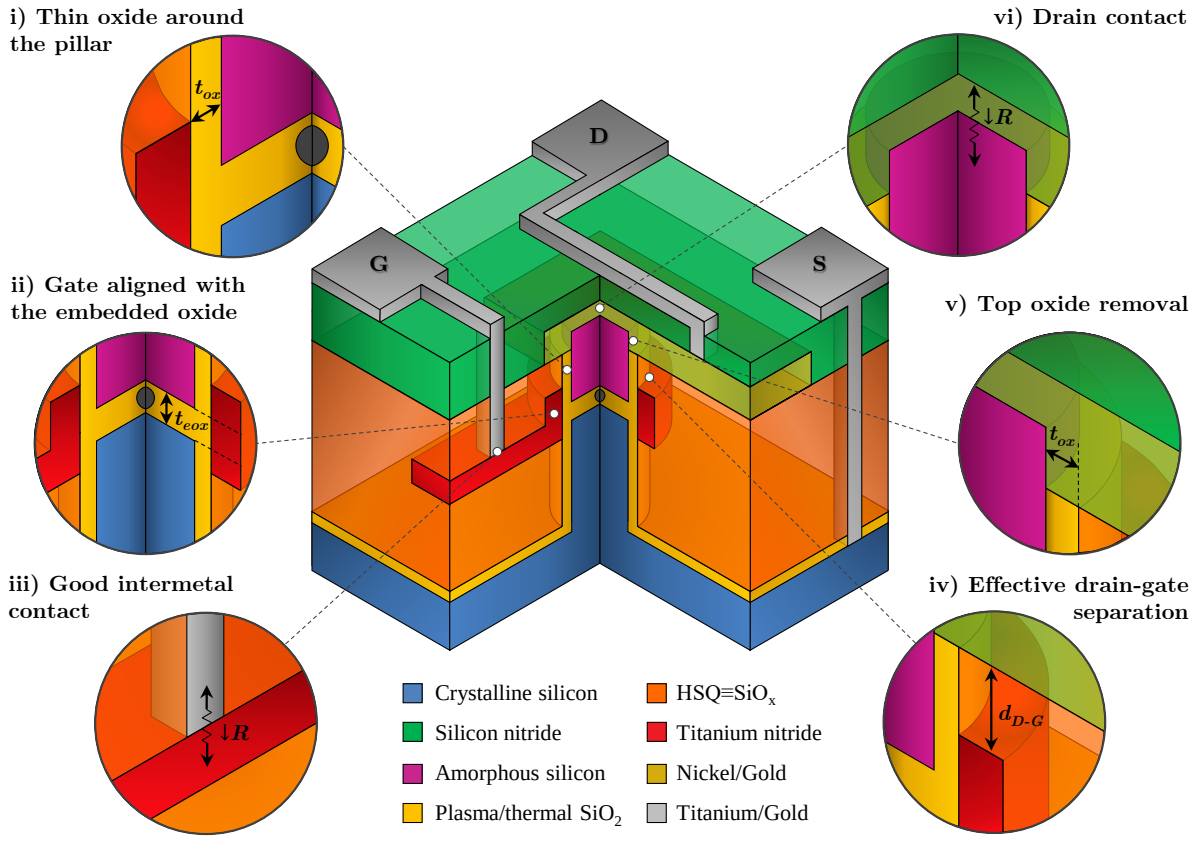


FIGURE 2.2: Sketch of the integrated SET with detail of the most relevant device features.

As indicated in Fig. 2.2, the gate electrode must be isolated from the bulk silicon substrate. And similarly, drain and gate must be separated by an insulating intermetal layer. This leads to additional requirements for the material to be used for that aim:

- **Accurate thickness control:** Given the vertical dimensions of the pillar, thickness controllability is extremely important. The upper part of the pillar is 25 nm high, and it is the only separation between gate and drain electrodes.
- **Good planarization:** The methodology used for intermetal deposition has to be adapted to the vertical device topology. It must be deposited so that no residues are remain in the pillar cap.
- **Electrical insulation**

In view of all these aspects, a spin-on-glass (SOG) material based on hydrogen silsesquioxane (HSQ) is chosen, provided by Dow Corning [53]. The material is well known for its excellent gap-filling and local planarization capabilities [54].

It is widely used as a negative tone resist for electron beam lithography [55]. Also, it can be converted into a SiO_x-like structure by means of thermal activation: through the scission of Si−H bonds, the formation of new Si−O chains is promoted [56]. In terms of dielectric characteristics, κ values in the range of 2.8−5.1 are reported [57], with annealing conditions playing a significant role in the quality of the resulting layer.

The layer topography and thickness in vicinity of nanostructures precludes a good planarization. In consequence, a method based on the etch-back by means of diluted hydrofluoric acid (HF) is used [58]. The final HSQ thickness control is limited by the precision of the etch-rate value.

The chapter is arranged as follows. First, the processes related to pillar patterning and Si NDs assembly are presented. Then, the overall integration process is introduced. Following this section, the process optimization of some of the most challenging issues in the SET integration is described. Afterwards, structural characterization of the fabricated devices is reported, followed by electrical measurements. And finally, fabrication and measurements will be correlated in form of conclusions.

2.2 Process sequence 1: Pillar patterning and Si NDs assembly

Stack preparation, pillar patterning and Si NDs assembly are performed at CEA-Leti. Rapid thermal annealing (RTA) conditions for NDs implantation are guided by predictive simulations carried out at HZDR. And plasma oxidation for pillar shrinkage and gate oxide formation is performed at FhG-IISB by the external company HQ-Dielectrics [59].

The first part of the process flow includes the nanopillar patterning, Si ND assembly, pillar size reduction and gate oxide fabrication. All these processes are depicted in Fig. 2.3. For stack preparation, on a crystalline Si substrate a SiO_2 layer is formed by thermal oxidation (a); then, amorphous silicon is deposited (b) by low-pressure chemical vapour deposition (LPCVD). Afterwards, electron beam direct writing (EBDW) lithography is followed by plasma dry etching for pillar patterning (c and d). An intermediate antireflective coating and spin on carbon (SiARC/SOC) hard mask is used to allow a better etching transfer to the a-Si/SiO_2/c-Si stack.

It has been proved that damage-free stacked nanopillars can be fabricated down to 18−20 nm in pillar diameter [60]. Nevertheless, even smaller diameters are necessary in order to ensure that only one single nanocrystal is formed. Since further shrinkage by resist trimming and more aggressive etching parameters would lower considerably the yield, a different approach is followed. A plasma oxidation at low temperature (<400°C) is performed in two steps with an intermediate HF etching, which ensures the diameter reduction down to ∼10 nm, while generating a 4−5 nm gate oxide all around the pillar (f).

Several technological challenges arise from the patterning of a vertical stack with an aspect ratio of 6:1, a single Si ND in the embedded oxide and a thin gate oxide on the sides of the pillar. In next sections the process conditions for achieving such features are respectively described.

2.2.1 Pillar patterning

The substrate is a crystalline silicon with resistivity values in the 8−22 $\Omega \cdot$ cm range. The SiO_2 layer is created by dry thermal oxidation after standard RCA cleaning. Afterwards, a 25 nm non-doped amorphous Si layer is deposited by LPCVD. Both thickness values are measured by ellipsometry. Then, a first level of alignment marks are patterned using EBDW and dry etching, with more than 200 nm etching depth checked by profilometer. These marks will be used for wafer/chip alignment in all the following lithography processes, including SET integration. Wafers are then implanted with Si ions at 50 keV and a dose of 1.2 x 10^{16} cm^{-2}. These conditions are chosen in order to allow Si/SiO_2 interface mixing and Si NDs formation after RTA treatment. Note that Si implantation is performed before pillar patterning, as a mitigation strategy to avoid any potential pillar shape change with ion erosion.

Regarding pillar patterning, initially both Directed self-assembly (DSA) and Electron Beam Lithography (EBL) were considered as suitable approaches at CEA-Leti. On one hand, DSA lithography is based on the phase separation of block co-polymers under geometric constrain, which can lead to the regular pattern of nanopillars below 15 nm diameter [61], [62]. Nevertheless, pillar location and pitch cannot be arbitrarily chosen and CMOS integration is still

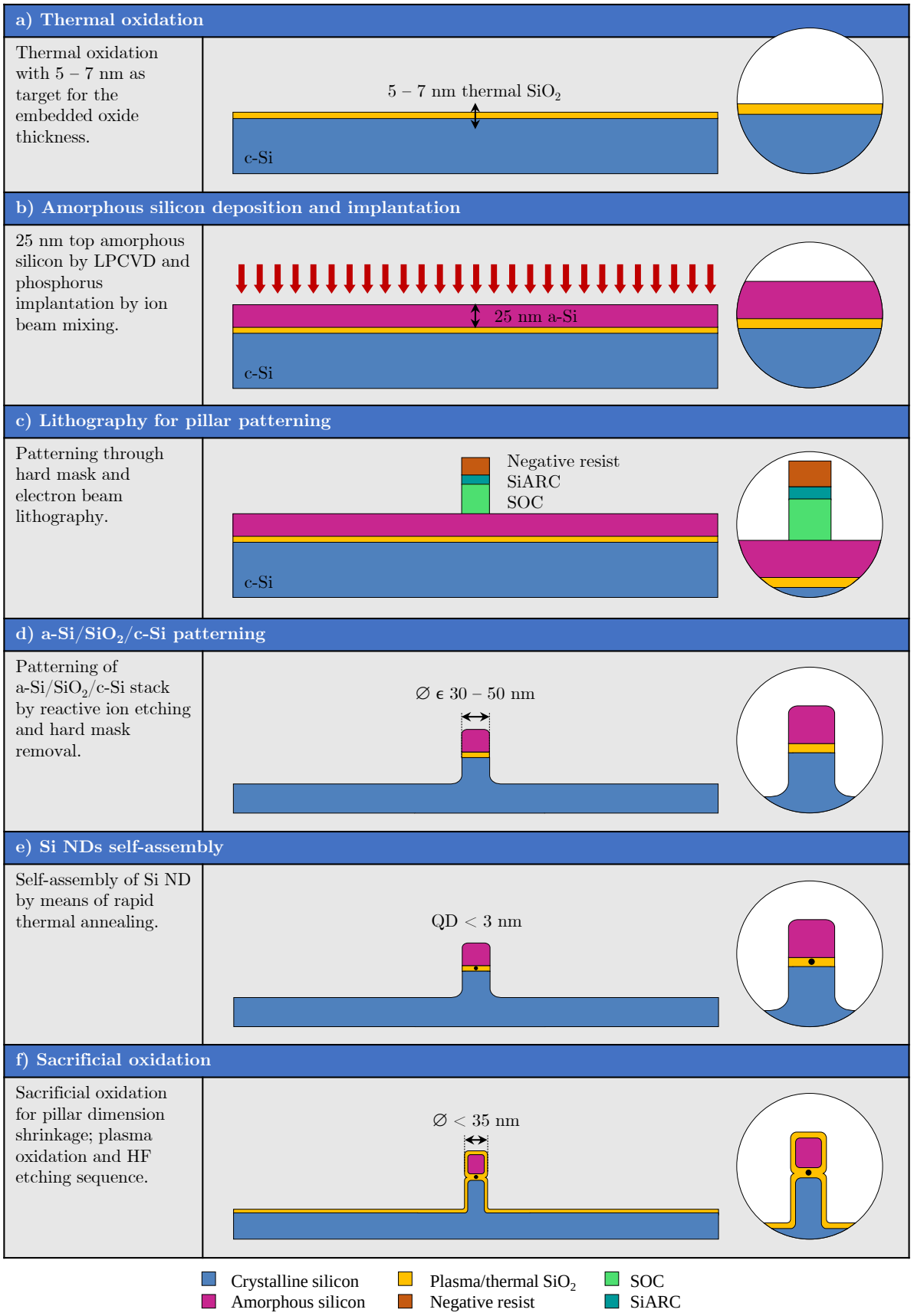


FIGURE 2.3: Schematic of the pillar patterning process.

an issue. On the other hand, the combination of EBL and reactive ion etching (RIE) is fully compatible with CMOS technology, and can be replaced by state-of-the-art optical lithography or future extreme ultraviolet lithography (EUVL). In that way, the use of EBL followed by RIE can provide cylindrical shaped nanopillars with sub-20 nm diameter and an aspect ratio >2:1 [60]. Two resist-based approaches were used: with only-resist and adding a SiARC/SOC as hard mask. In both cases, the pillar profile was characterized after etching using SEM with a tilted view angle of 52°, with results presented in Fig. 2.4. By using only resist, resist erosion occurs during etching to the a-Si/SiO_2/c-Si stack and a straight etch profile becomes difficult to obtain for smaller pillars. Hence, the resist trimming with the use of a hard mask approach allows to further decrease the final critical dimension down to 26 nm, while obtaining a sharper pillar profile.

The EBDW lithography was performed with a Vistec SB3054DW shaped E-beam tool working at an accelerating voltage of 50 kV and a current density of 20 A/cm^2. A chemically amplified negative tone resist was used with a film thickness of 85 nm. The intermediate hard mask is a SiARC/SOC of 30 nm and 95 nm, respectively. Resist development after exposure was done in tetramethylammonium hydroxide (TMAH) solution using a 200 mm ACT8 track from TEL Company. The plasma dry etching was carried out in a capacitively coupled plasma (CCP) chamber, using suitable gas chemistries for resist trimming, pillar etching transfer into SiARC/SOC and etching into the a-Si/SiO_2/c-Si stack, respectively. Finally, dry stripping by oxygen-based plasma was used to remove the remaining SOC, followed by wet cleaning steps to remove any organic residues and particles.

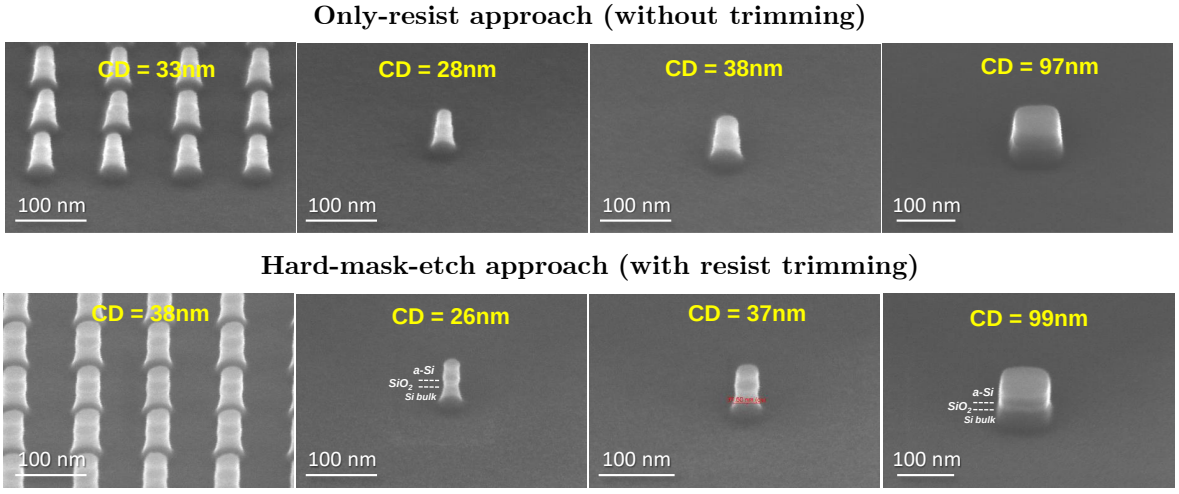


FIGURE 2.4: Tilted SEM images of pillars after a-Si/SiO_2/c-Si stack etching using only resist-etch approach without trimming (top) and hard-mask-etch approach with resist trimming (bottom).

Pillars of different diameter and pitch were structurally characterized by SEM after complete etching and resist stripping. The minimum critical dimension indicated in Fig. 2.4 is measured by top-down SEM, taken on a Hitachi HCG4000 CD-SEM tool. The profile characterization was carried out in a tilted view using a HELIOS SEM tool from FEI. Fig. 2.5 shows more tilted views after patterning by resist trimming; as visible, both isolated pillars and array configurations present similar diameters, with a slight yield reduction for arrays of lower pitch.

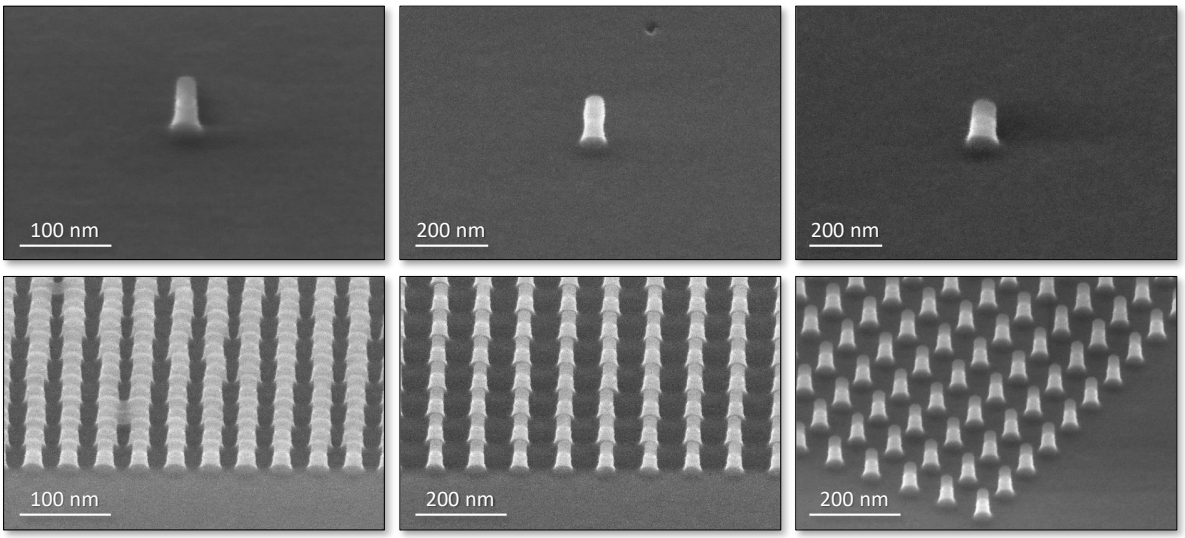


FIGURE 2.5: Tilted SEM images of isolated pillars (top) and arrays (bottom) after considered conditions for pillar patterning and resist removal.

2.2.2 Si NDs self-assembly

Predictive simulations for Si NDs formation in the embedded oxide thickness of nanopillars were performed at HZDR, and are described in Appendix A. NDs are formed as result of phase separation during annealing in a very small volume of a metastable mixture. The self-assembly process occurs via phase separation and its consequent interface energy minimization, also known as Ostwald ripening. These two mechanisms can be used to form a single Si ND in an embedded SiO_2 layer. The first step is the ion irradiation of the a-Si/SiO_2/c-Si stack, producing a far-from-equilibrium state in finite volumes (i.e. Si is mixed into SiO_2, forming SiO_x with $0 < x < 2$). The metastable volume must be very small for the subsequent self-assembly of a single ND. This is achieved by using very thin SiO_2 layers, in the 5−7 nm range, and reducing the maximum lateral extension down to 10 nm (i.e. pillar diameter). After the ion-irradiation-induced formation of $<10^3$ nm^3 volumes of the metastable compound SiO_x, Si ND self-assembly takes place by thermally activated phase separation.

Optimized ion beam mixing conditions for Si irradiation are determined at 50 keV and 1.5 x 10^{16} $Si^{+} \cdot cm^{-2}$. Similarly, thermal annealing is performed by means of 60s at 1050°C in N_2 atmosphere. It has been found that nanopillars change their shape during ion irradiation at fluences relevant for ion beam mixing; this is attributed to ion-irradiation-induced viscous flow, usually reported as hammering effect [63]. As mitigation strategy, the two steps necessary for Si NDs formation are separated: ion mixing is performed at stack level, while the annealing is carried out after nanopillar patterning. This process sequence is depicted in Fig. 2.3. This is feasible, as nanopillars withstand a thermal process up to 1100°C for 2 min without shape change. Note that, nevertheless, after Si ND formation this thermal budget is reduced, not to avoid pillar shape modification but Si ND dissolution.

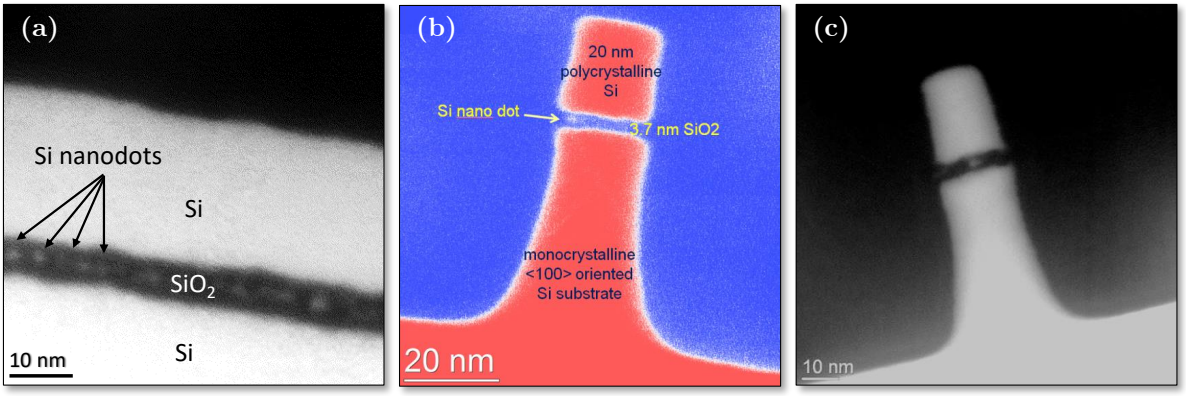


FIGURE 2.6: Si plasmon loss EFTEM image of a Si-irradiated and annealed a-Si/SiO_2/c-Si layer stack (a), a ⌀ 20 nm pillar with a Si ND close to the rim (b) and another example of Si ND in the 5.3 nm thick oxide layer of a ⌀ 20 nm pillar (c).

In order to optimize and validate the experimental conditions of ion beam mixing and thermal annealing, morphological characterization of Si NDs and its tunnelling distances is required. As there is almost no contrast between Si and SiO_2 in conventional Transmission Electron Microscopy (TEM) images, energy-filtered TEM (EFTEM) will be applied using the different valence-band plasmon excitation energies of Si and SiO_2. In addition, challenging TEM sample preparation using cross beam technology has to be used in order to allow the observation of such nanometer features. In all cases, all TEM characterization results presented in this thesis were obtained at HZDR.

By using the conditions mentioned above, Si NDs can be observable in non-patterned samples (Fig. 2.6.a) as well as in patterned pillars (Fig. 2.6.b and c). Note in that last example the relevance of oxide thickness for the single Si ND formation at the very center of the pillar.

2.2.3 Pillar size shrinkage and gate oxidation

In order to have one Si ND or a few only in the oxide layer of a nanopillar, its diameter has to be in the 10−12 nm range, as confirmed by the kinetic Monte-Carlo (kMC) simulations described in Appendix A. As shown in previous sections, the pillar patterning by means of EBL and RIE can only ensure a high yield of undamaged pillars for >20 nm diameters. A standard technique to reduce the thickness of Si fins or the diameter of Si pillars is through silicon oxidation: a certain thickness of the Si surface is oxidized and the oxide is subsequently removed by selective etching, usually with diluted HF.

The potential of sacrificial oxidation as pillar shrinkage and gate oxide formation is explored by means of two separate techniques: thermal oxidation at temperatures between 850°C and 1050°C, and by using low-temperature plasma oxidation. Results are presented in Fig. 2.7.

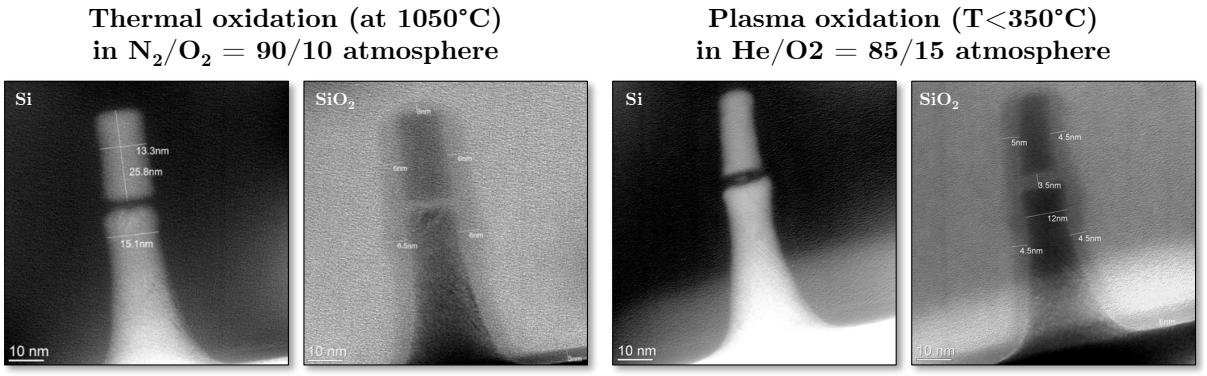


FIGURE 2.7: EFTEM images of Si and SiO_2 plasmon loss of pillars after thermal oxidation at 1050°C in $N_2/O_2 = 90/10$ atmosphere (left) and after plasma oxidation in $He/O_2 = 85/15$ atmosphere (right).

The effect of shrinking the pillar by thermal oxidation is clearly observed. However, EFTEM also shows that the Si NDs, whose existence were proved before, do not exist anymore after processing. By reducing temperature down to 850°C similar results are obtained. The situation is different if plasma oxidation is applied. Pillar diameter is shrunk while Si ND is maintained in the oxide layer. By applying a double sequence with intermediate oxide removal by diluted HF, reduction down to 10 nm can be achieved. As different diameters are considered in the pattern layout, not all nanopillars are reduced to that value. Therefore, pillars close to 20 nm present several Si NDs in the oxide layer. These NDs can be removed either by further oxidizing the pillar, or by increasing the thermal budget and thus promoting NDs dissolution. Nevertheless, the understanding is that there might be a self-selection of one specific ND according to the most symmetric position and the lowest tunnelling distance.

2.3 Process sequence 2: Pillar contacting

A major part of the work performed during this thesis has been centred on the development of a complete fabrication process in order to provide fully contacted SETs. The first part of the process is illustrated in Fig. 2.8, showing the nanopillars with a thin GAA oxide and Si NDs embedded in the oxide layer as the starting point (a). First, it is defined a dielectric intermetal layer to insulate the gate electrode from the substrate; it is done by means of spin-coating, back-etching and annealing of HSQ at 800°C (b). Afterwards, the gate oxide is locally removed from top of the pillar by Argon plasma (c). It is followed by the GAA definition: 10 nm TiN deposition by RF sputtering (d), and TiN wet etching on top of the pillar and outside the gate region through an etched-back HSQ mask (e to g).

Fig. 2.9 shows the continuation of the process flow. A second dielectric layer is deposited (h), again following the etch-back approach but in this case with an annealing at 400°C, in order to avoid crystallization effects on the TiN layer [64]. Then the definition of the drain electrode is performed by means of EBL with positive resist (i), e-beam evaporation of 30/20 nm Ni/Au (j) and lift-off (k).

In order to prevent oxidation of the drain terminal, by plasma-enhance chemical vapour deposition (PECVD) a 25 nm silicon nitride (Si_3N_4) is deposited as passivation layer (l). The remaining steps concern the contact windows etching and the metal routing definition, summarized in Fig. 2.10. Another lithography level is used to define the openings (m), which are etched by means of a combination of dry (n) and wet etching (o). Finally, again following the sequence EBL, metallization of 5/65 nm Ti/Au and lift-off (q to s), the metal stripes and contact pads are defined.

The process flow here described is the baseline for the work presented in this chapter. Thus, it will be further discussed in the forthcoming sections, including the optimization of the most demanding steps. All the related steps with nominal conditions, target thickness or etching time values, as well as the equipments used, are reported in Appendix C.

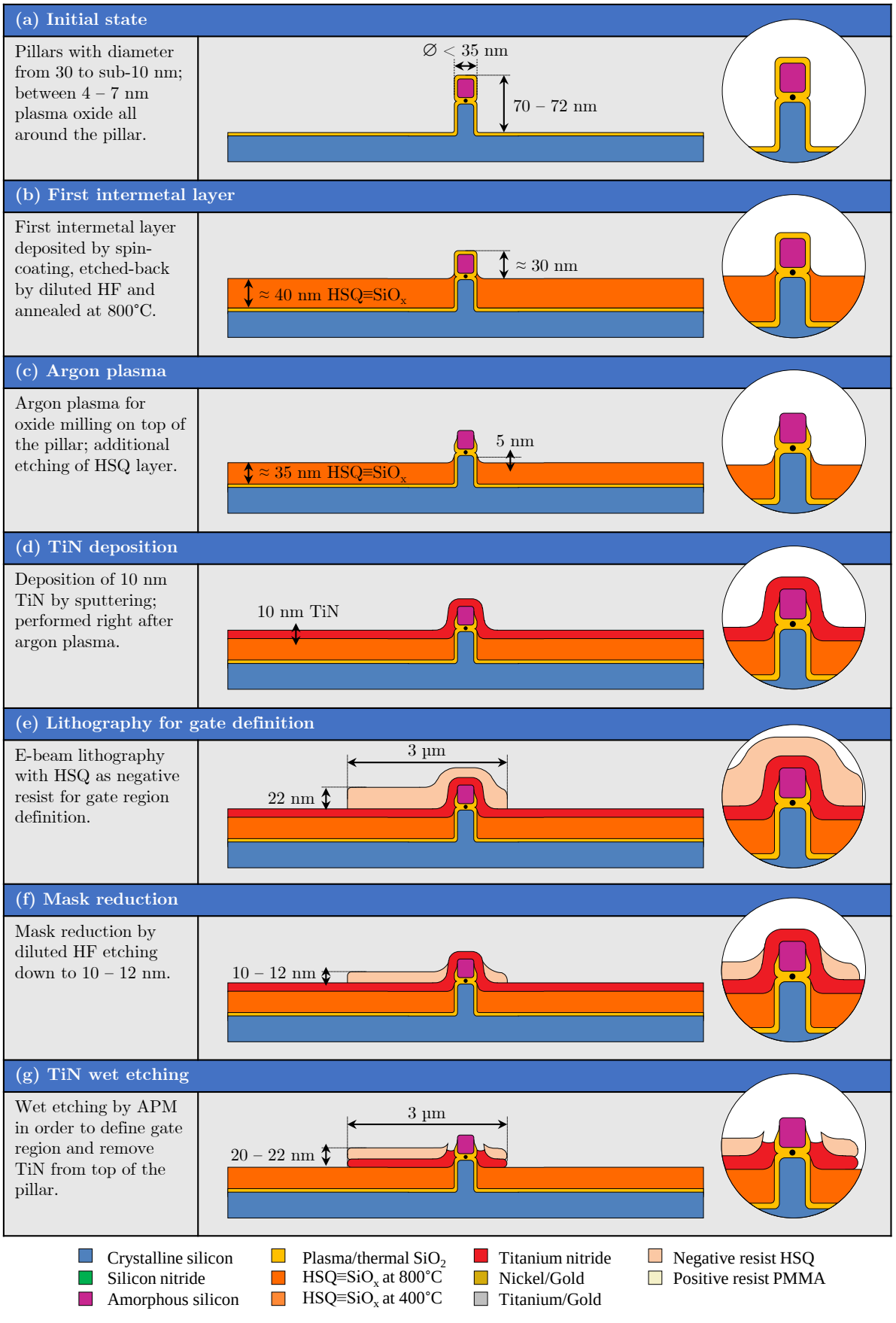


FIGURE 2.8: Schematic of integration process steps related to gate electrode definition.

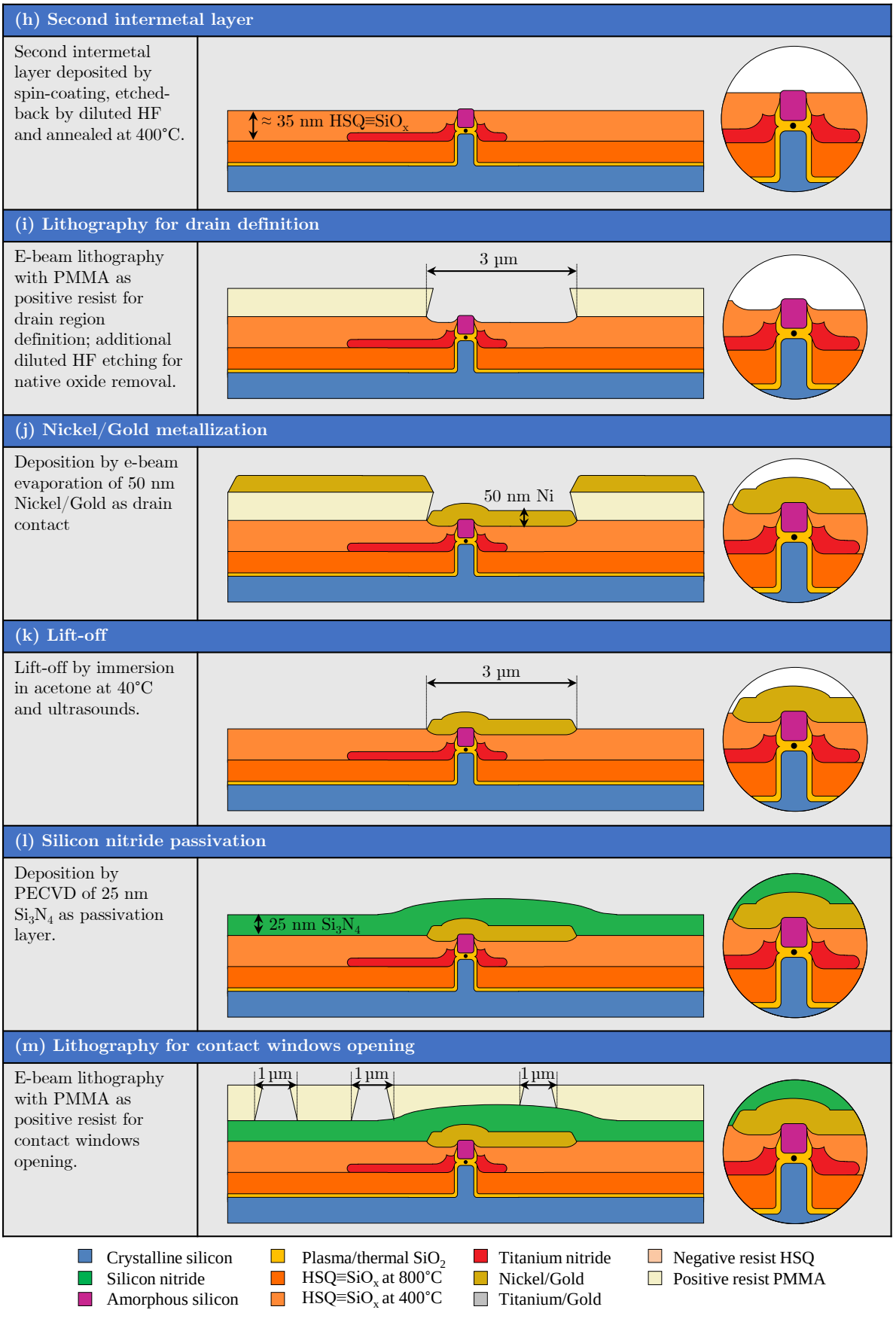


FIGURE 2.9: Schematic of integration process steps related to drain electrode definition.

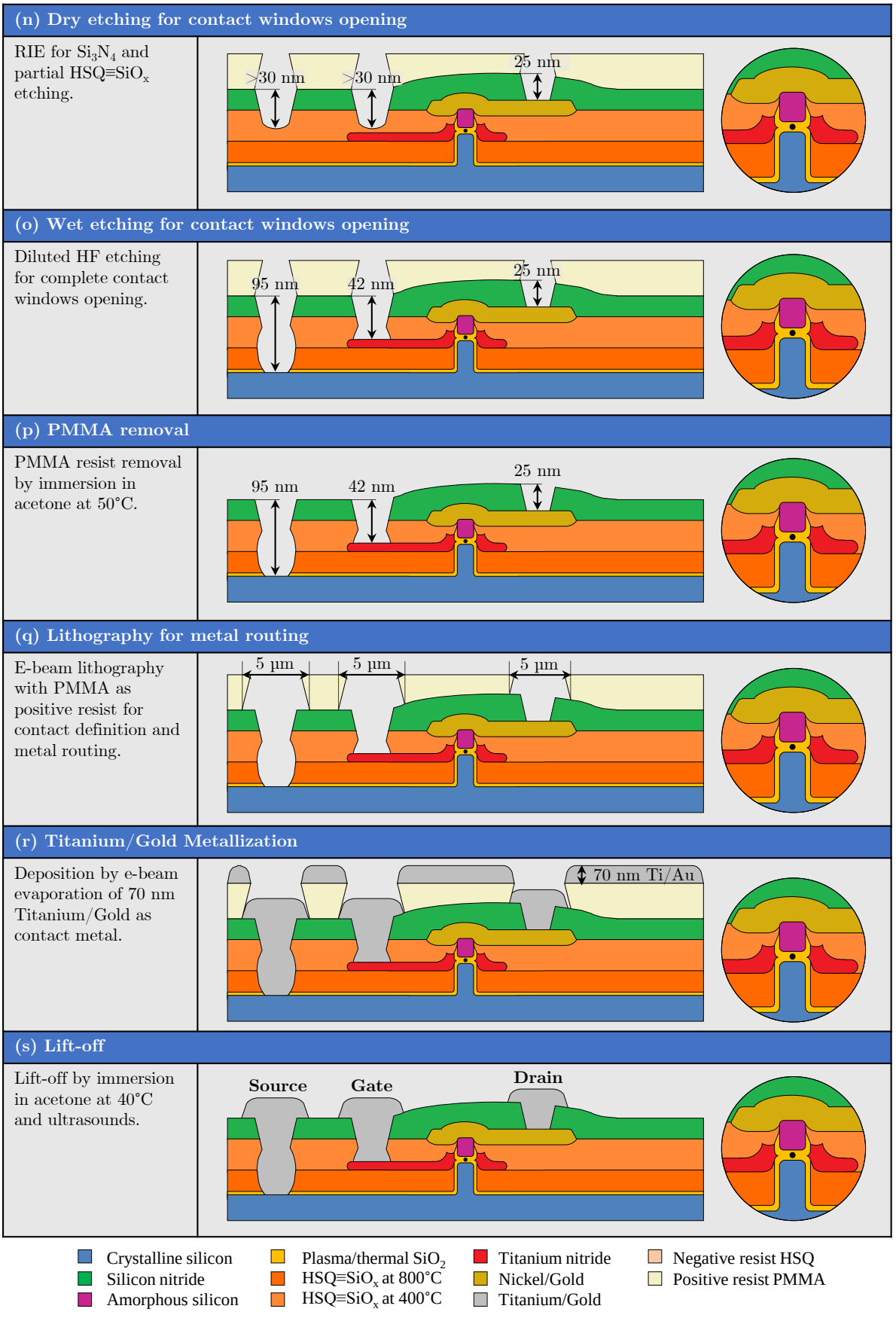


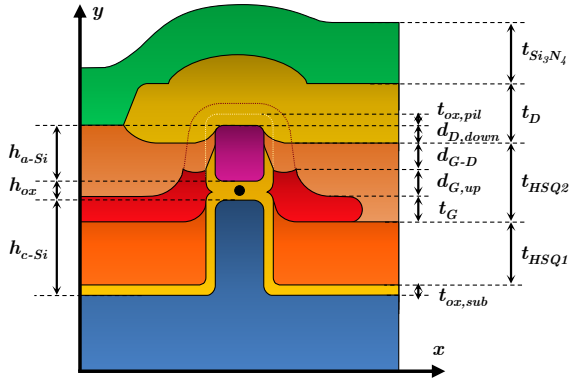
FIGURE 2.10: Schematic of integration process steps related to contacts definition.

2.3.1 Integration process simulator

The integration of a nanopillar into a fully contacted SET is compromised by several factors. As Fig. 2.2 introduced, there are a group of architectural constrictions which have to be considered. This is in close relation to the pillar dimensions (Fig. 2.1), including QD size and position, embedded oxide thickness, pillar height, diameter and surrounding pillar oxide thickness. As stated in previous section, the combined variability of all these variables reduces the process windows to obtain observable Coulomb blockade oscillations. Therefore, it is convenient to develop methodologies which can refine the integration process, improve its efficiency and make it more adaptable to the sample characteristics.

A process simulator is developed for all the steps described in section 2.3. There are some of these steps that can take significant profit from predictive simulations. For instance, it is known that temperature annealing has affectation on HSQ thickness [57]. As two different temperature annealing steps are performed (b and h), this effect has to be experimentally quantified. Moreover, there are several etching steps whose etch-rate and material selectivity must be calculated. The Argon plasma used to remove the oxide from top of the pillar (c), causes as well an additional milling on the intermetal layer. All these effects are empirically quantified and presented in next sections, and they are implemented in the process simulator.

In that way, a predictive process simulator is developed, providing guide conditions in order to fulfil the targeted dimensions depicted in Fig. 2.11. Experimental measurements from process monitoring can be implemented in the simulator, and the system provides feedback in order to readjust the conditions towards the optimum situation (e.g. a thinner second intermetal layer if the first one is thicker than targeted). For more information about the variables considered, their nominal values and statistical uncertainty, see Appendix D.



Symbol	Parameter	Nominal
$t_{ox,sub}$	Substrate oxide thickness	6.5 nm
t_{HSQ1}	First intermetal layer thickness	39.2 nm
t_G	Gate electrode thickness	9.5 nm
$d_{G,up}$	Rising in the gate around the pillar	7.0 nm
t_{HSQ2}	Second intermetal layer thickness	25.8 nm
$t_{ox,pil}$	Remaining top oxide thickness	0.0 nm
t_D	Drain electrode thickness	50.0 nm
$d_{D,down}$	Sinking in the drain over the pillar	5.0 nm
$d_{G\text{-}D}$	Effective Gate-Drain separation	12.0 nm
$t_{Si_3N_4}$	Silicon nitride thickness	20.0 nm

FIGURE 2.11: Sketch of the SET after integration, with detail of the most significant parameters monitored by the process simulator with its targeted values.

2.3.2 Layout description

The SET integration process requires four lithography levels: gate electrode definition, drain electrode definition, contact windows opening and top metal routing patterning. All levels are performed by EBL in a Raith-150 TWO equipment, at different exposure conditions depending on resist and related requirements. In all cases, the layout designs must be adapted to the layers of the process sequence performed at CEA-Leti: etched marks on the silicon substrate for allowing the alignment of all posterior lithographies; and stack patterning, which includes the definition of isolated nanopillars, test structures and array distributions. In this section the layout of all patterned structures is presented, followed by the lithography levels that constitute the SET integration.

Fig. 2.12 shows the distribution of four regions, where four groups of five pillars are patterned with nominal dimensions from 30 nm to 50 nm, in steps of 5 nm. Smaller diameters are achieved after etching and sacrificial oxidation, as already mentioned. These isolated pillars are the structures used for the SET integration.

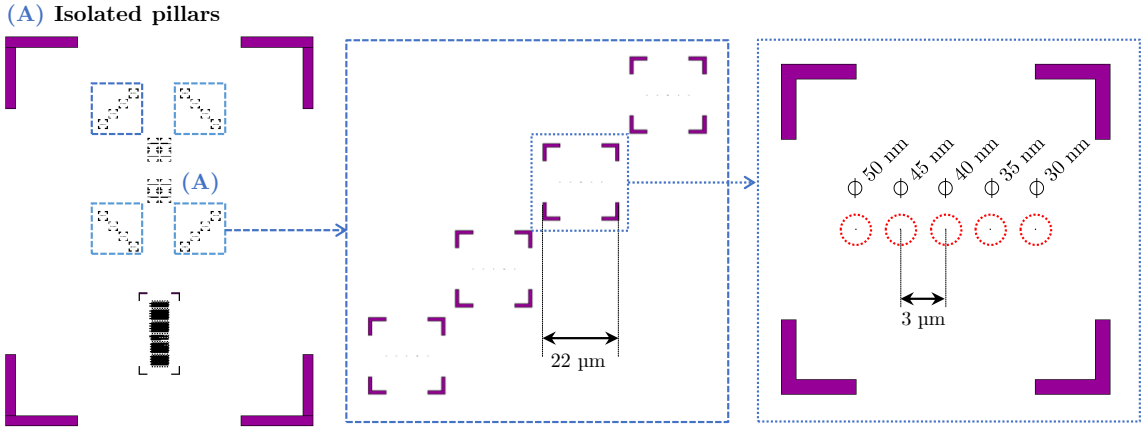


FIGURE 2.12: Layout of patterned pillars with nominal diameter from 30 nm to 50 nm (A).

A second group of structures contains squares 1 μm wide, 50 nm and 100 nm wide fins of different pitch and 50 nm dots. Fig. 2.13 provides more information about the distribution of such structures. These test structures are aimed to facilitate the characterization in the intermediate steps of the process: due to the small dimensions of the isolated pillars, structural characterization such as AFM or SEM cannot describe the required features.

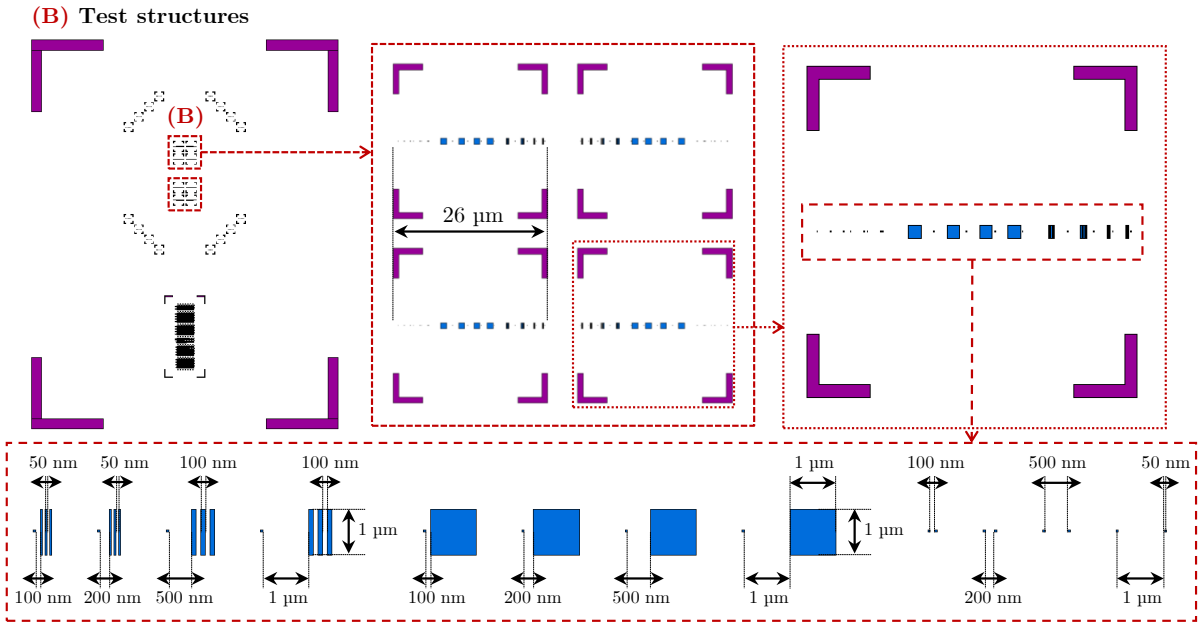
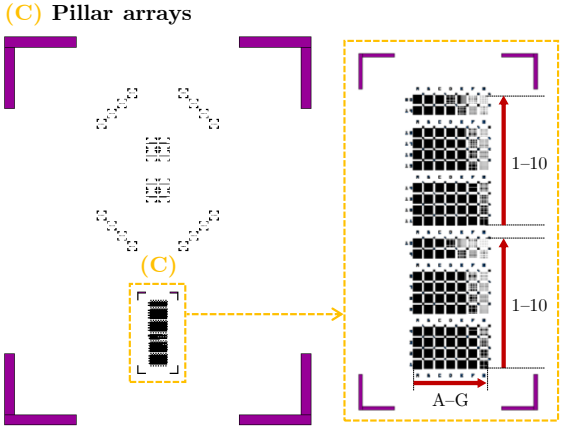


FIGURE 2.13: Layout of patterned test structures, including dots, fins and squares (B).

A third region in the layout contains arrays of pillars of different diameter and pitch. Fig. 2.14 shows the nominal values of critical dimension and pitch of pillars in this region; again, smaller dimensions than the nominal ones will be obtained. These arrays are used for two aims: (i) to analyse the influence of pillar density into the integration process (ii) and to contact simultaneously full arrays of pillars in order to obtain a larger drain-to-source current. In this second case, single electron effects are expected to be appreciable as well.



Row	CD	Pitch variation (nm) 2x CD	2.5x CD	3x CD	4x CD	5x CD	7x CD	10x CD
		A	B	C	D	E	F	G
10	100	200	250	300	400	500	700	1000
9	80	160	200	240	320	400	560	800
		A	B	C	D	E	F	G
8	65	130	162.5	195	260	325	465	650
7	60	120	150	180	240	300	420	600
6	55	110	137.5	165	220	275	385	550
5	50	100	125	150	200	250	350	500
		A	B	C	D	E	F	G
4	45	90	112.5	135	180	225	315	450
3	40	80	100	120	160	200	280	400
2	35	70	87.5	105	140	175	245	350
1	30	60	75	90	120	150	210	300
		A	B	C	D	E	F	G

FIGURE 2.14: Layout of patterned pillar arrays of different pitch and critical dimension (C).

Fig. 2.15 presents the layout for contacting single pillars. As observed, metal pads and stripes are connected to the inner regions of the device. A closer view shows the metal routing towards the gate and drain of one of the five isolated pillars, which are unevenly contacted. A third terminal goes to the source contact, which can also be enabled via backside of the chip, as standalone SETs are fabricated on bulk silicon. In total, eight pillars are contacted per chip.

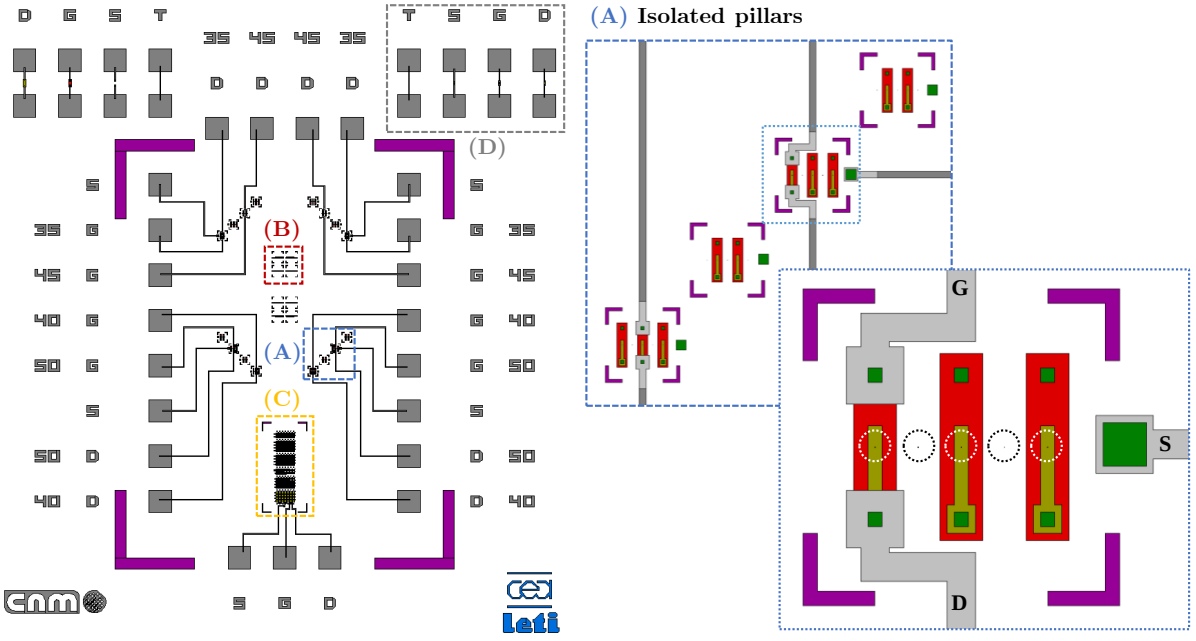


FIGURE 2.15: Layout of contacted isolated pillars of different nominal diameters (A).

The metal routing distribution includes three terminals for the contacting of one pillar array, as Fig. 2.16 shows. Additional pads are fabricated in the upper-outer region of the chip. These contacts are simple structures to test the contact windows etching and electrical continuity through drain, gate and source electrodes.

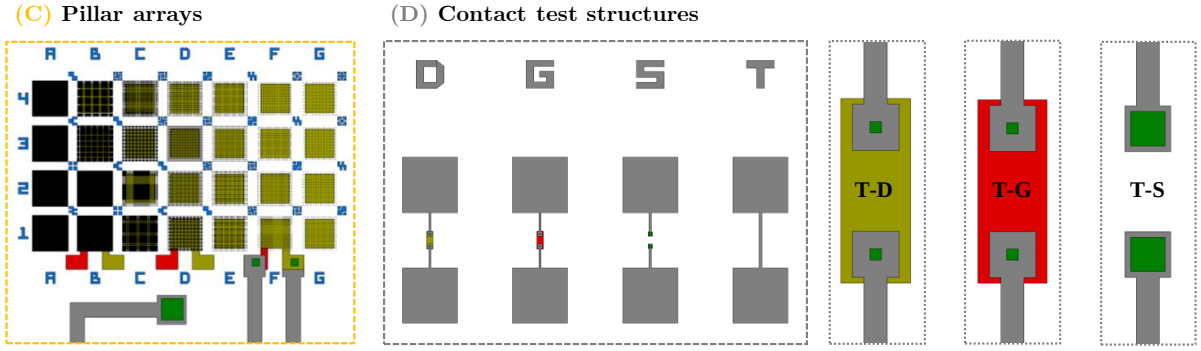


FIGURE 2.16: Layout of contacted pillar arrays of different pitch and critical dimension (C) and additional contact test structures for process monitoring (D).

2.4 Process optimization

2.4.1 HSQ planarization for contacting nanostructures

A process for creating HSQ intermetal layer, in fulfilment with the structural requirements described in Fig. 2.2, has been developed. The etch-rate is experimentally assessed for the etch-back process. The annealing temperature affectation to the resulting HSQ thickness [57] must also be considered, in order to control in more accuracy the resulting thickness.

First, a thick HSQ layer (∼200 nm) is deposited by spin-coating and measured by ellipsometry. Afterwards, it is etched-back by means of diluted HF. During this step, from the liberation of hydrogen gas during HSQ etching by the acid solution, bubbles appear all along the surface. This phenomena induces discrepancies in the etch-rate, as well as a rough topography in the resulting layer. However, it can be avoided by applying benzalkonium chloride (BZK) as cationic surfactant in the acid solution [58]. BZK affects the flow around a forming bubble by creating a tension gradient, and the tangential stress induces a convective flow towards higher surface tensions. When the tangential fluid motion reaches the area of bubble encroachment, these bubbles are pinched off and detached [65].

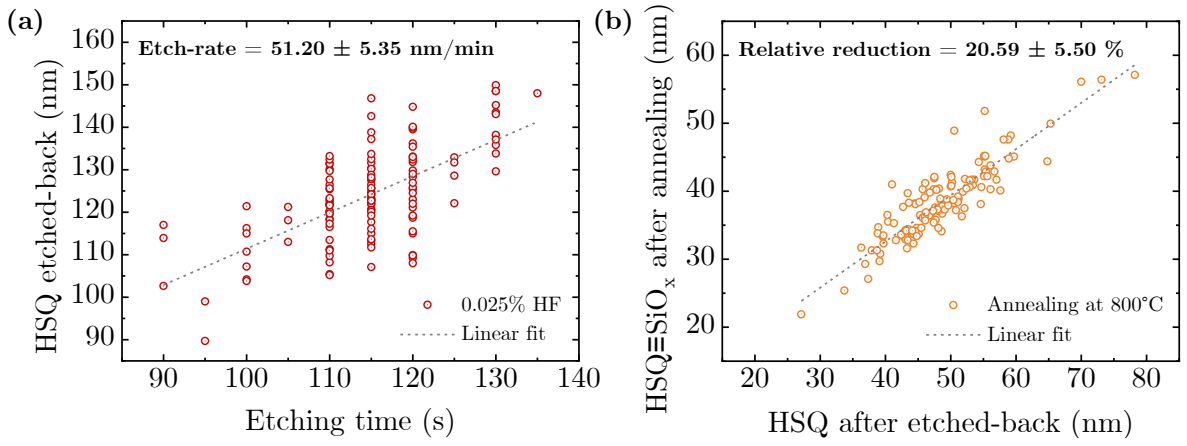


FIGURE 2.17: Etch-rate of HSQ to diluted HF (a) and affectation of temperature annealing on HSQ thickness (b).

In that way, a 2% BZK is added in the 0.025% diluted HF solution. The measured etch-rate is presented in Fig. 2.17.a, with an average value of 51.20 ± 5.35 nm/min. As mentioned, the required annealing at 800°C to turn the HSQ layer into a SiO_x-like material might affect the resulting thickness. Fig. 2.17.b illustrates this effect, in which a reduction around 21% from the etched-back layer is obtained after the annealing step.

Once the layer thickness has been controlled, the etched-back plus annealing sequence is tested in patterned nanostructures (i.e. isolated pillars and pillar arrays). Two specific aspects must be validated. First, obtaining an intermetal thickness that can facilitate the posterior alignment of the gate electrode with the embedded oxide, including the TiN electrode thickness and its ring elevation around the pillar. And second, ensure the flatness of this intermetal layer and its planarization around nanostructures; this second issue is necessary to ensure the proper electrical contact, as no HSQ residues must remain around the pillar.

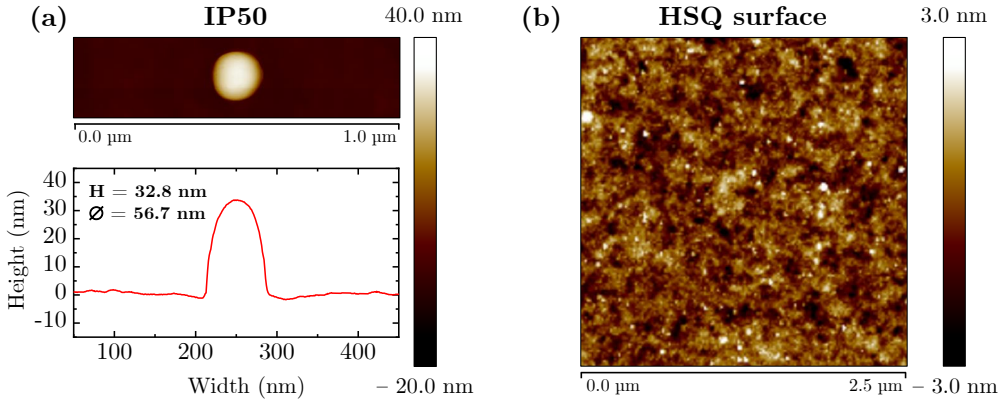


FIGURE 2.18: AFM profile after etched-back and annealing process on an isolated pillar (a) and topography of the HSQ surface (b).

Fig. 2.18.a presents the AFM profile of a pillar after performing the HSQ spin-coating, back-etching and annealing at 800°C, according to the conditions described above. The pillar was initially 71 nm high; after processing, a total height of 32.8 nm is measured. Therefore, it can be concluded that the intermetal layer covers almost all the base of the pillar, and leaves uncovered the embedded oxide and the pillar cap. These are optimum conditions for the proper gate electrode location, as a 10 nm TiN layer might land at the same height than the embedded oxide. In addition, the AFM pillar profile does not suggest the presence of HSQ residues around the structure, as a sharp slope is observed. Fig. 2.18.b shows an area of the HSQ surface after annealing, with a mean roughness value of 0.6 nm; this is indicative that a flat and low roughness layer can be created.

An additional concern regarding HSQ planarization is the affectation of its gap-filling capabilities in pillar arrays. For that reason, in Fig. 2.19 the AFM profiles of arrays of different pitch and same nominal diameter are gathered for comparison. As visible, the height difference from the outer region of the array to the pillar top is in the same range in all cases. However, the in-between pillars depth is smaller for lower pitch values. This is attributed to the reduced efficiency of the etched-back mechanism in more dense arrays, although the AFM tip convolution might be an additional contributor of the effect. The conclusion is that the deposition process is

dependant on the pillar pitch, although in less dense arrays the same behaviour than in isolated pillars is observed. This threshold is established in pitch values at least $< 4x\varnothing$.

In summary, the application of HSQ in the overall integration process has been successfully developed, as it fulfils the two structural requirements: a controlled thickness that enables the further placing of electrodes, and good planarization around isolated pillars and less-dense pillar arrays.

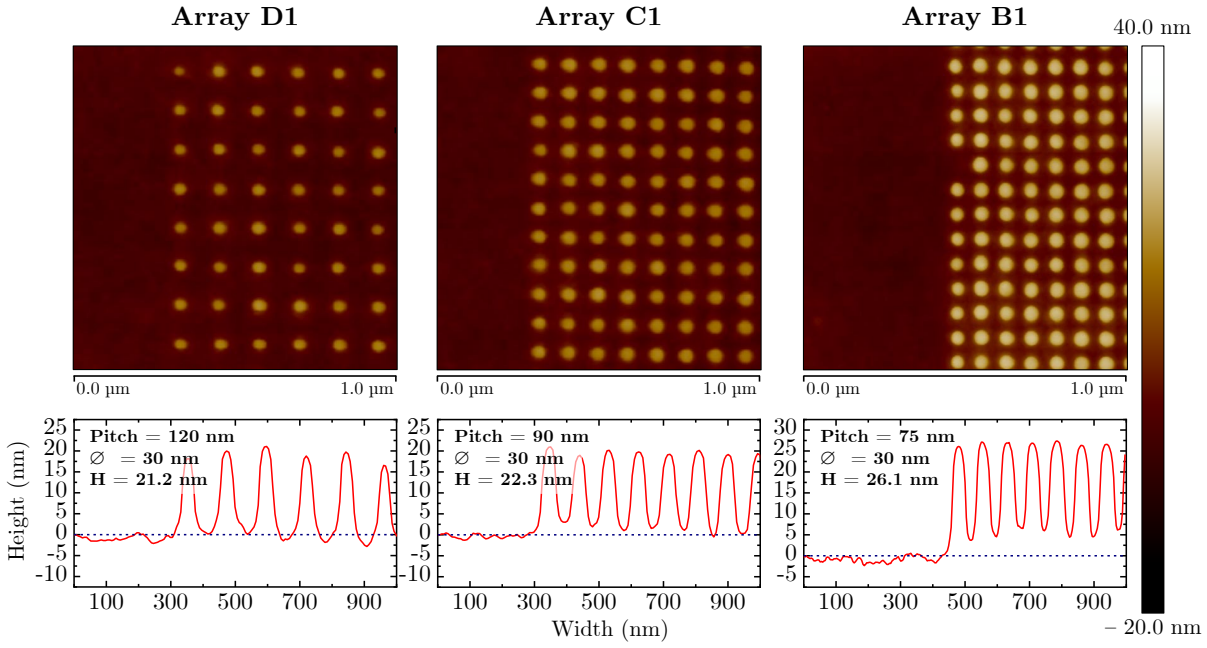


FIGURE 2.19: AFM profiles after etched-back and annealing on different pitch pillar arrays.

2.4.2 HSQ as electrical insulator

In addition to the already mentioned geometrical constraints, the use of HSQ as intermetal layer is subjected to adequate insulating capabilities. The following experiments validate the use of HSQ as intermetal between metal and a crystalline silicon substrate ($1-12\ \Omega \cdot \text{cm}$).

The etch-back process is used to obtain very thin HSQ layers. Two different temperature values are used for the annealing step, 400°C and 800°C, with resulting thickness in each case of 14.2 nm and 17.5 nm, respectively. Afterwards, metal pads are patterned by means of lithography, e-beam evaporation and lift-off. Fig. 2.20.a presents the resulting current-voltage characteristics, with capacitive measurements between the upper metal contact and the bulk silicon substrate. In both cases very low current is measured, well below 1 pA; this justifies the use of HSQ as intermetal layer between electrodes.

Similarly, conductivity measurements are performed on TiN contacts fabricated on top of HSQ annealed at 800°C, and again no current through the intermetal layer is measured. From Fig. 2.20.b and nominal dimensions for the patterned contacts, the calculated TiN resistivity in this configuration is 347.8 ± 14.5 $\mu\Omega \cdot$ cm.

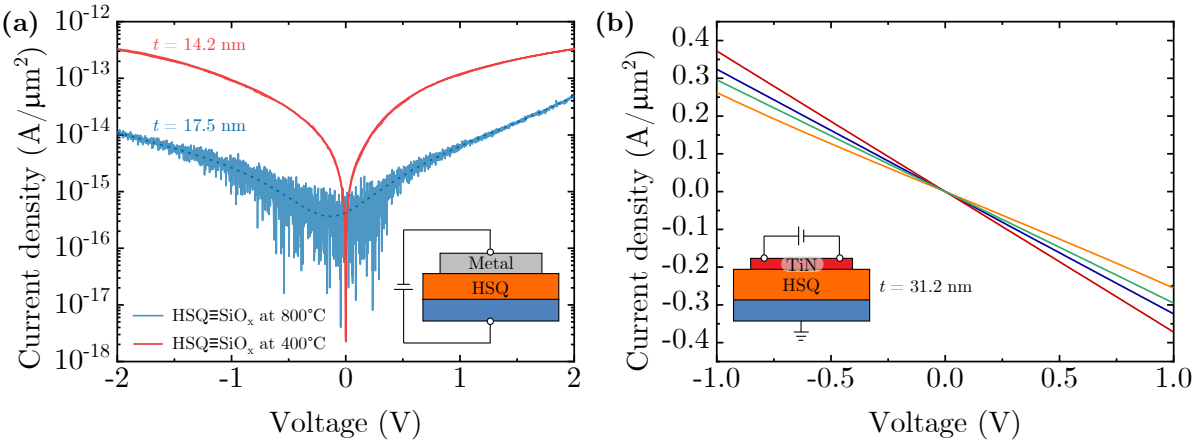


FIGURE 2.20: Current density of metal pads on top of thin HSQ at different annealing temperatures (a), and normalized current density of 10 nm thick TiN contact pads on top of HSQ annealed at 800°C (b).

2.4.3 Argon milling for top-oxide removal

The plasma oxide all around the pillar is necessary for the device operation. Nevertheless, it must be locally removed from top of the pillar in order to obtain a good electrical drain contact. This has been one of the most challenging issues of the integration process, as a thin layer of SiO_2 has to be etched without further damaging the a-Si pillar cap. Sketch (c) in Fig. 2.8 illustrates this process step. Note that if an isotropic wet etching is chosen, such as HF, then the integrity of the embedded oxide and the gate-all-around oxide would be compromised. Moreover, after top oxide removal, the uncovered silicon pillar cap might be easily oxidized again by atmospheric conditions.

For that reason, an Argon plasma is used as milling process performed right before the sputtering deposition of 9−10 nm TiN as gate electrode. In that way, the directionality of the process is expected to be enough to etch only the top oxide, if the process is controlled enough further damage on the pillar can be avoided, and the growth of a native oxide layer cannot take place as the already deposited TiN layer would cover the rest of the pillar. Note that the Ar plasma induces as well an additional etching in the first intermetal layer; this thickness reduction is quantified and implemented in the process simulator described in section 2.3.1.

Again, the only method that enables the precise observation of SiO_2 residues on top of the pillar is EFTEM structural characterization. Therefore, a batch of samples with the first intermetal layer is prepared with different time values for the Ar plasma performed, and it is characterized afterwards. Both Ar plasma and TiN sputtering are performed in a Kenosistec KS800H system. In the first case, power is fixed at 100 W and different etching times are tested. For the TiN sputtering, it is performed at 10 sccm of Ar, 10 sccm of N_2, 3 μbar and 1000 W.

Pillars arrays → Intermetal layer → 40s Ar plasma → TiN sputtering

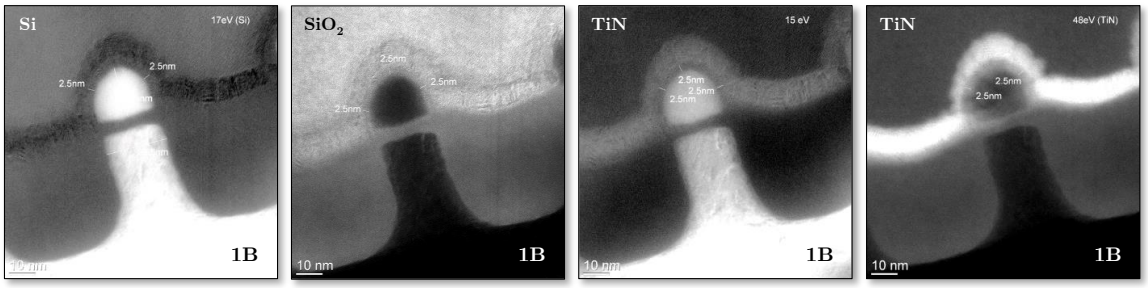


FIGURE 2.21: EFTEM plasmon loss images of pillar array 1B after 40s Argon plasma.

Fig. 2.21 presents the TEM results of the 1B pillar array (i.e. nominal ⌀ of 30 nm and pitch of 75 nm) after 40s of Ar plasma. As observed, a 2.5 nm thin oxide layer remains around the pillar cap, preventing the TiN-pillar contact. This is clear indicative that the etching time is insufficient.

Pillars arrays → Intermetal layer → 70s Ar plasma → TiN sputtering

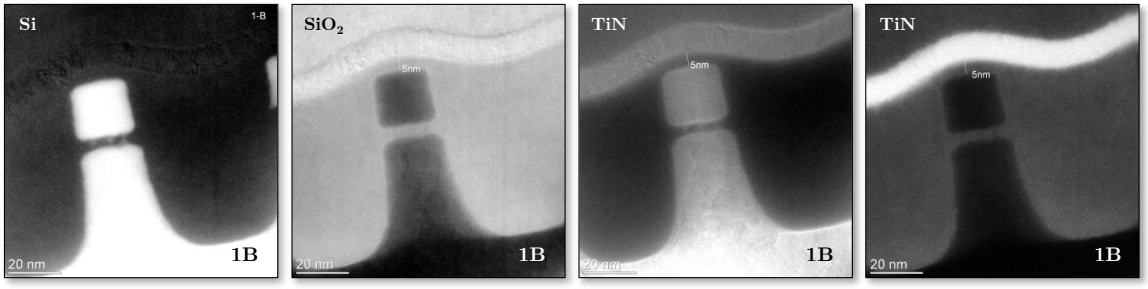


FIGURE 2.22: EFTEM plasmon loss images of pillar array 1B after 70s Argon plasma.

Results with a longer Ar plasma time of 70s are shown in Fig. 2.22. In this case a different approach was followed: by defining a thicker intermetal layer, in combination with a longer etching time, may result in the effective removal of the top oxide. However, not only there is still around 5 nm oxide on top of the pillar, but the first intermetal layer is located too high to place the gate electrode.

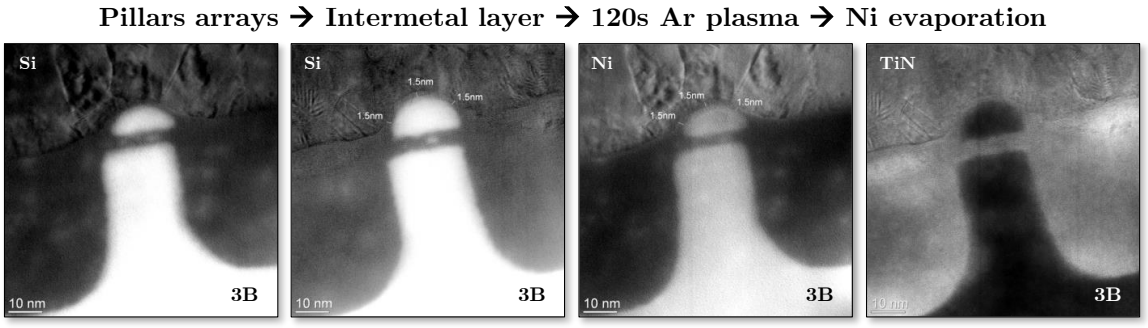


FIGURE 2.23: EFTEM plasmon loss images of pillar array 1B after 120s Argon plasma.

Next test is an Ar plasma of 120s, but in this case followed by the deposition of 50 nm Ni by e-beam evaporation (Fig. 2.23). The intention is to explore the viability of performing the top oxide etching right after drain electrode deposition, instead of the gate. Nevertheless, an Ar plasma of 120s is clearly too aggressive: the silicon cap is significantly reduced by more than a half part, making infeasible the integration of both drain and gate electrodes.

As previous experiments clearly indicate, the complete top oxide removal is a trade-off between two main parameters: first, the initial HSQ thickness, which is in close relation to the pillar density in the case of arrays; and secondly, the Ar plasma etching time. Fig. 2.24 presents the TEM characterization on isolated pillars, in which the intermetal layer thickness is targeted

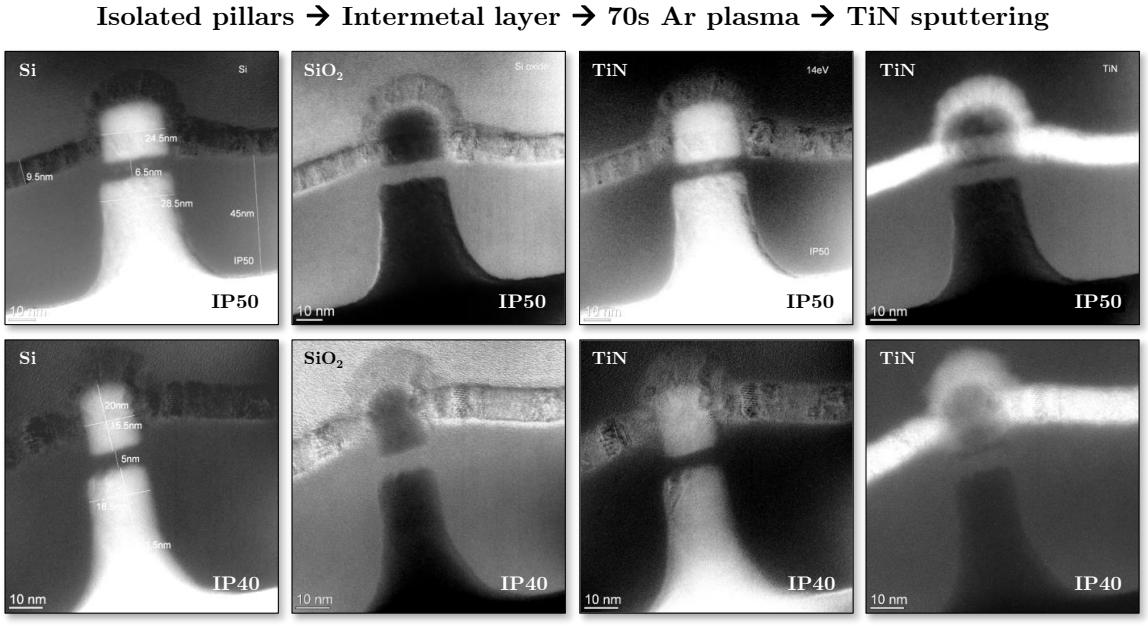


FIGURE 2.24: EFTEM plasmon loss images of isolated pillars IP50 (top) and IP40 (bottom) after optimized Ar plasma time.

up to the upper part of the embedded oxide. An Ar plasma of 70s is performed, followed by the TiN deposition by sputtering. Results show that there are not oxide residues between TiN and top of the pillar, in fulfilment of the requirements for drain-pillar contact. Therefore, these parameters are stated as baseline conditions for the integration process.

2.4.4 Gate definition

Another critical aspect is the definition of a GAA. A TiN ring all-around the pillar is necessary, located at the same height than the embedded oxide. As the TiN electrode is deposited by sputtering in a conformal way, several difficulties arise concerning the overall process. Two definition levels are required: TiN material must be removed from outside the gate region, defining the pre-contact electrode; and more importantly, it must also be etched from the upper part of the pillar, defining the already mentioned ring.

In the cases presented below, TiN removal is performed by means of wet etching in Ammonia-Peroxide Mixture (APM) at room temperature. The capabilities of HSQ as e-beam negative tone resist enable its use as mask during the etching. Here, HSQ is exposed in a Raith-150 TWO at 20 kV, a base dose of 550 μC/cm^2 and a beam current ~150 pA; the development is performed by immersion during 70s in TMAH 3% followed by rinse in flowing water.

Fig. 2.25 illustrates a preliminary approach for gate definition, in which a first lithography level is used to define the gate region through HSQ exposure (a) and TiN removal (b). After resist removal (c) a second intermetal layer is defined so the upper part of the pillar remains uncovered (d), so the TiN etching can be performed (e). However, this strategy induces two additional drawbacks indicated in (f). First, the mask removal is done by means of diluted HF; this etching reduces as well the first intermetal layer, and thus the electrical insulation of the complete stack might be affected. And second, the upper intermetal layer is used both for defining the gate as for supporting the drain. In that way, the material used as drain would fill the TiN-emptied ring all-around the pillar, resulting in a short-circuit that prevents from SET operation.

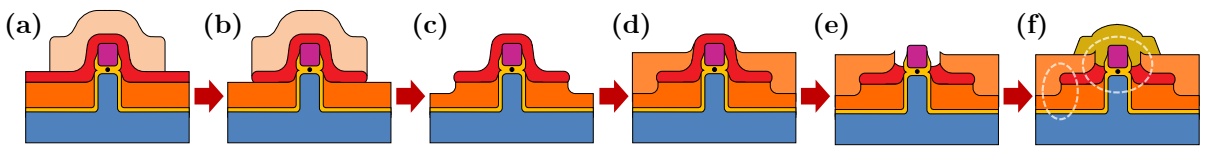


FIGURE 2.25: Sketch of the preliminary approach for gate definition.

A second approach is depicted in Fig. 2.26, in this case supported by AFM profiles of the very same pillar in all the related steps. The idea is to use the etch-back mechanism in the negative mask, lowering the exposed HSQ thickness down to 10−12 nm (b). In that way, the same mask can be used to efficiently remove the TiN from top of the pillar and from outside the gate region (c). A second intermetal layer could then fill the ring around the pillar and support at the same time the drain electrode, while keeping an effective distance between them. The insets in Fig. 2.26 are the measured heights from the AFM profiles, altogether with the theoretical values according to the process simulator. By immersion during 50−60s in 0.025% diluted HF, an initial step of 20.9 nm is reduced down to 13.4 nm. After 90s in APM solution, this value is increased up to 23.5 nm, very close to the +10 nm thickness for the TiN layer already removed. A closer inspection on the isolated pillars corroborates the measurements: after etch-back the pillar is more exposed, and after the TiN wet etching it is much less appreciable.

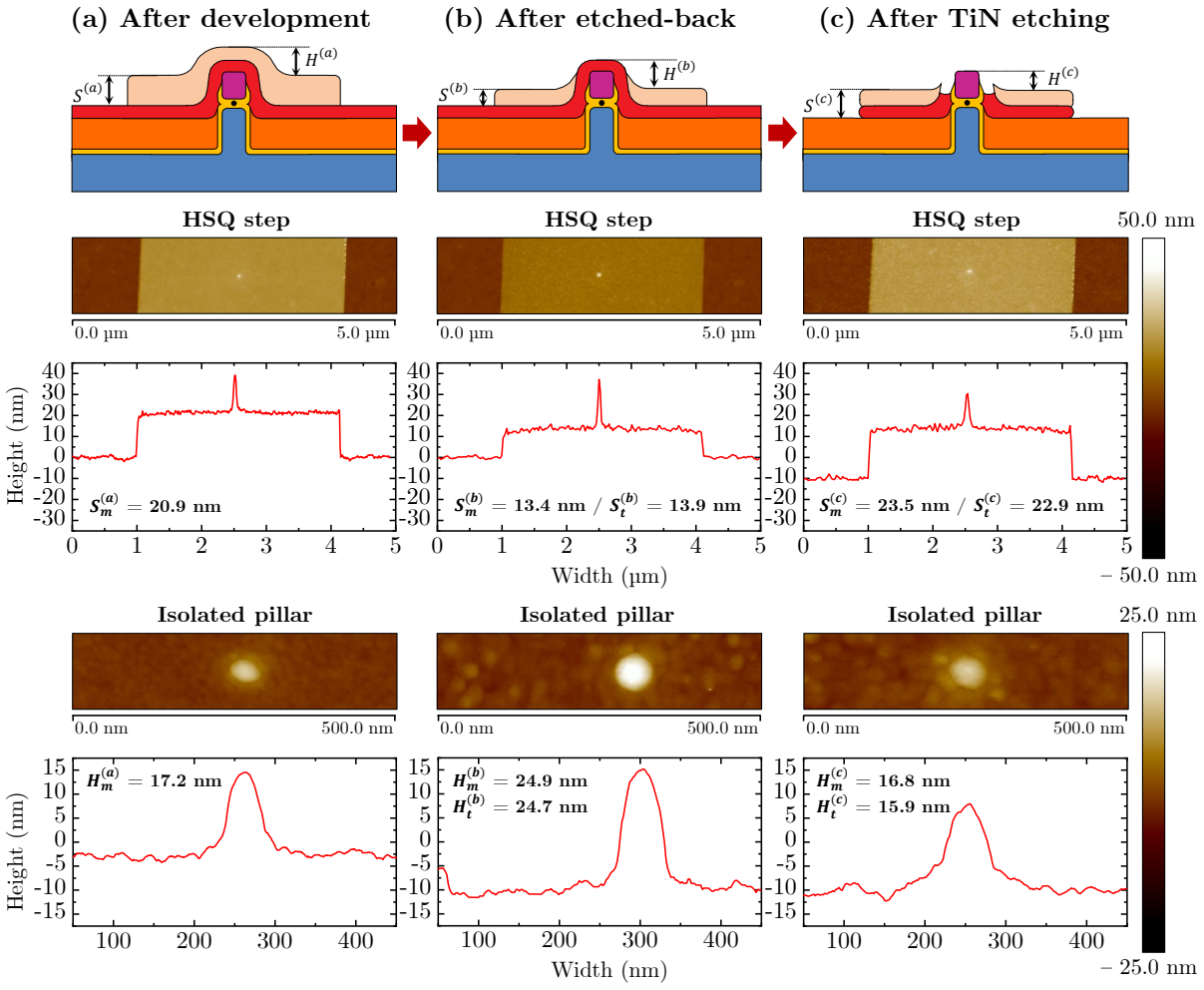


FIGURE 2.26: AFM profiles of the same pillar in all the process steps of gate definition.

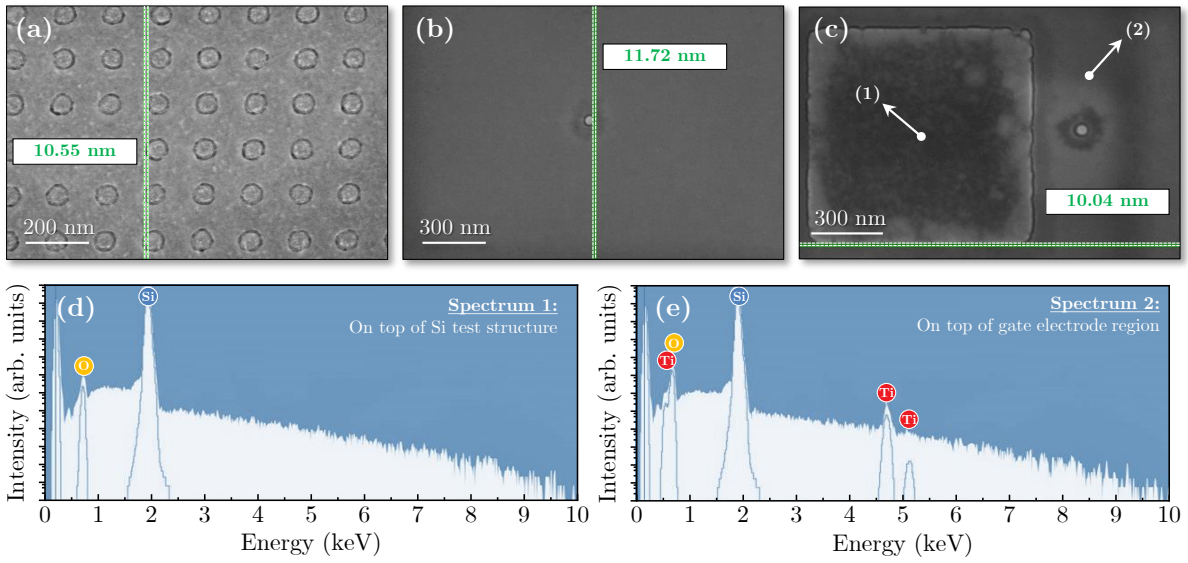


FIGURE 2.27: SEM images after gate definition of a pillar array (a), an isolated pillar (b), a test structure (c) and EDX analysis on top the structure (d) and on top of gate region (e).

Further analysis can be done in order to validate the second approach described for gate definition. In Fig. 2.27, SEM characterization of pillars right after TiN etching is presented. The dark ring observed around all the pillars, both isolated and in array configuration, is attributed to the remaining TiN region all-around the pillar; the measured distance is very near the 10 nm of the TiN thickness. In addition, the 1 μm test structure from Fig. 2.27.c can be used for Energy Dispersive X-Ray Analysis (EDX). Two positions are analysed: on top of the structure (d), with no peaks associated with Ti presence; and on top of the gate region (e), with three additional peaks indicating the presence of Ti material.

In summary, the method described is considered to be suitable for gate definition at pillar level. From AFM characterization of the same pillar at different steps, the expected height variation is measured; SEM figures show a ring around all pillars, indicative of a change in electrical conduction; and finally, EDX analysis on test structure proves the TiN removal from its chemical composition.

2.4.5 Ni/Au as drain electrode

Given the characteristic SET low output current, series resistance between drain and pillar must be minimized. Literature reports chromium, platinum or nickel as suitable materials for contacting silicon nanostructures [66], [67], [68]. In the case of the process flow designed for the SET contacting, the drain electrode definition is followed by deposition of 20−25 nm Si_3N_4

by PECVD at 350°C, and afterwards contact windows etching and metal routing definition. Therefore, a subsequent aim is to keep the low resistive contact after processing.

In a first batch of samples the drain electrode was formed by 15 nm Pt with 5 nm Cr as adhesion layer. Fig. 2.28.a shows the surface topography of the Cr/Pt layer deposited by e-beam evaporation. After completion of the process, electrical measurements on the contact test structures described in Fig. 2.16 were performed. The results indicated a too resistive behaviour. Further analysis pointed out a slight difference in the Cr/Pt topography (b), induced either by the PECVD process or by the posterior RIE for Si_3N_4 etching.

A feasible solution was to deposit Ni instead of Cr/Pt as drain electrode. A similar electrical behaviour was observed, and therefore the analysis was repeated. The AFM figures (c) and (d) show the Ni surface after evaporation and after the PECVD plus RIE sequence, respectively. The optimized method for contact windows etching is described in next section; nevertheless, it is convenient to note here that it includes a diluted HF etching. The affectation of this etching to the Ni layer is analysed as well, observing a significant variation in the topographic aspect as reported in (e).

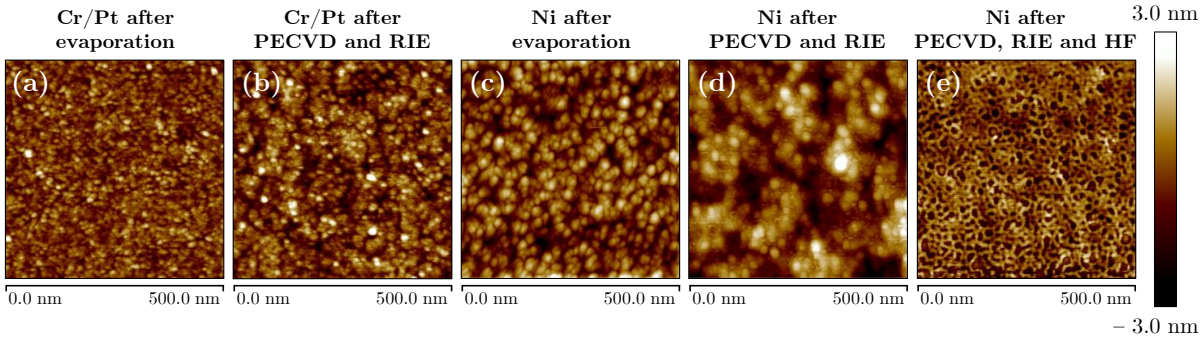


FIGURE 2.28: AFM topography of Cr/Pt after evaporation (a), Cr/Pt after PECVD and RIE (b), Ni after evaporation (c), Ni after PECVD and RIE (d) and after diluted HF (e).

The observations are in agreement with the next hypothesis. During the PECVD process, the upper part of the metal layer is oxidized. Hence, the HF wet etching that should not affect either Pt or Ni, does attack significantly their respective oxide forms. As mitigation strategy to solve this issue, a bilayer drain electrode is proposed. First, a 30 nm Ni layer is deposited, enhancing the drain-pillar contact in agreement with literature. In the same chamber and keeping the vacuum level, a 20 nm Au layer is deposited afterwards; in that way, as gold does not directly react with oxygen under standard conditions [69], it can endure the combination of PECVD, RIE and HF.

2.4.6 Contact windows etching optimization

The vertical architecture of the nanopillar-based device compels the electrode arrangement in form of multilayer stack. In that way, a 10 nm TiN electrode is buried between two intermetal layers, in order to isolate it from drain and bulk silicon. Similarly, the 50 nm Ni/Au drain pre-metal contact is covered by a silicon nitride for passivation issues. Therefore, in each of the contact windows to be opened (source, gate and drain), a different stack has to be etched; Fig. 2.29 illustrates the stack in each case. In order to shorten the duration of the complete integration process, the target is to fabricate all contact windows in just one lithography step.

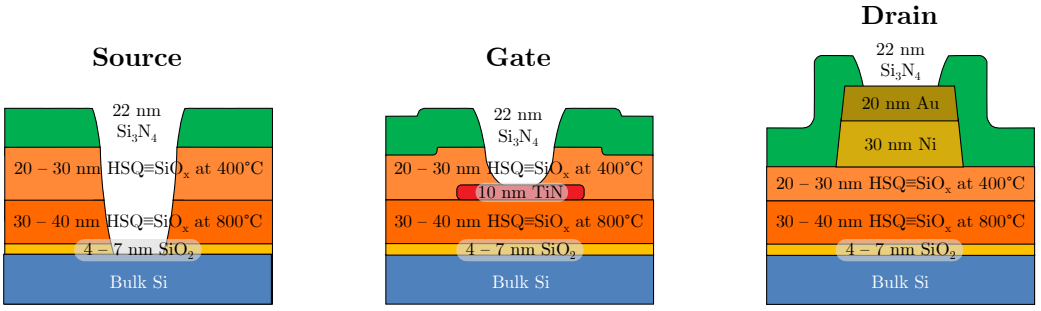


FIGURE 2.29: Sketch of the layers to be etched in each of the contact windows.

Regarding the drain electrode, just a ∼22 nm Si_3N_4 layer has to be etched. In the case of the gate, it is the Si_3N_4 layer plus a 20−30 nm HSQ≡SiO_x. And finally, source contact window stack is Si_3N_4, the 20−30 nm HSQ≡SiO_x annealed at 400°C, the bottom 30−40 nm HSQ≡SiO_x annealed at 800°C and the 4−7 nm SiO_2 formed by plasma oxidation.

The mask for contact windows patterning is defined by EBL. A ∼270 nm Polymethyl methacrylate (PMMA) is deposited by spin-coating; it is e-beam exposed at 10 kV, dose of 110 $\mu C/cm^2$ and a beam current of ∼210 pA. Development is performed in Methyl isobutyl ketone (MIBK) and Isopropyl alcohol (IPA) in a 1:3 concentration for 40s, followed by 20s in IPA.

The etching of Si_3N_4 is performed by RIE, at 30 sccm of C_4F_8, 20 sccm of CH_4 and 20 sccm of He and at 0°C. Power and time are optimized for the etching of 22 nm Si_3N_4, with values of 1200 W, 50 W as chuck power and 34s as etching time. Under these conditions, the drain contact window is expected to be open.

Same recipe is found to be effective for the etching of HSQ≡SiO_x annealed at 400°C, and thus it could be used for the opening towards the gate electrode. Nevertheless, the RIE recipe etches as well TiN with a relatively fast etch-rate. Therefore, there is the risk of opening too much the gate contact window, and even of going through it. The solution is to use the RIE recipe for

the complete Si_3N_4 and partial HSQ≡SiO_x etching. The rest of the stack is etched by means of diluted 0.1% HF. In this point, the process simulator provides approximation of the etching time required to etch the remaining layer, based on the measured thickness of the intermetal layers and the AFM characterization.

The remaining layers of the source contact window are too thick to be etched in the same lithography step and with no risk on the other two openings. Therefore, as the source contact can be done through backside of the sample in bulk silicon, the complete stack etching is discarded.

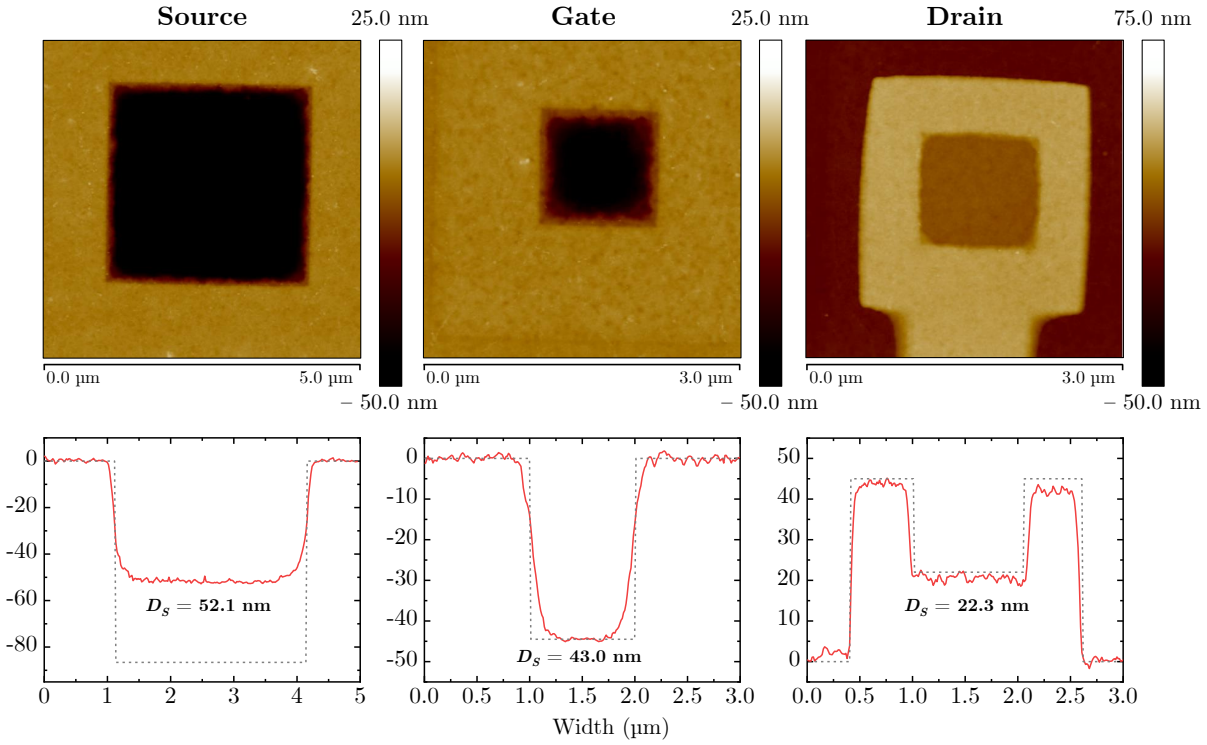


FIGURE 2.30: AFM figures of source, gate and drain contact windows etched at optimized conditions, with corresponding profiles (solid line) and simulated depth values (dashed line).

In Fig. 2.30 the AFM profiles of all three windows after processing are presented. Conditions in this particular case are: 37s RIE at the already described conditions, plus 30s in 0.1% HF. As observed, the source contact is very far from the expected value. Nevertheless, regarding the gate and drain openings, in both cases the measured depths are in the same order than the targeted ones provided by the simulator. Thus, the combination of RIE and wet etching is considered to be optimum for the opening towards drain and gate electrodes, while source contact can be established via bulk silicon substrate.

2.4.7 Options for metal routing

Once gate and drain pre-metals are properly located and in contact with the pillar, and after the conditions for their contact windows etching are optimized, the only remaining issue is the metal routing patterning. In the context of the SET operation, parasitic resistance and capacitance contributions must be minimized, and thus a good intermetal contact is necessary. In this section, the suitability of different metals for that aim is explored.

In early batches, before optimizing the utilization of the bilayer Au/Ni as drain electrode, 50 nm Ni was used both for drain as for top metal routing. The patterning was performed again by means of positive PMMA resist exposure by EBL, evaporation by e-beam evaporation and lift-off in acetone and ultrasounds at 40°C. A too resistive behaviour in electrical measurements induced the necessity of TEM structural analysis of the contact windows. Fig. 2.31 shows the cross section of drain (a) and gate (b) openings. As observed, and corroborated by EDX analysis (c), there is a residual 1.4 nm oxide layer between top Ni and Ni/TiN for drain/gate, respectively.

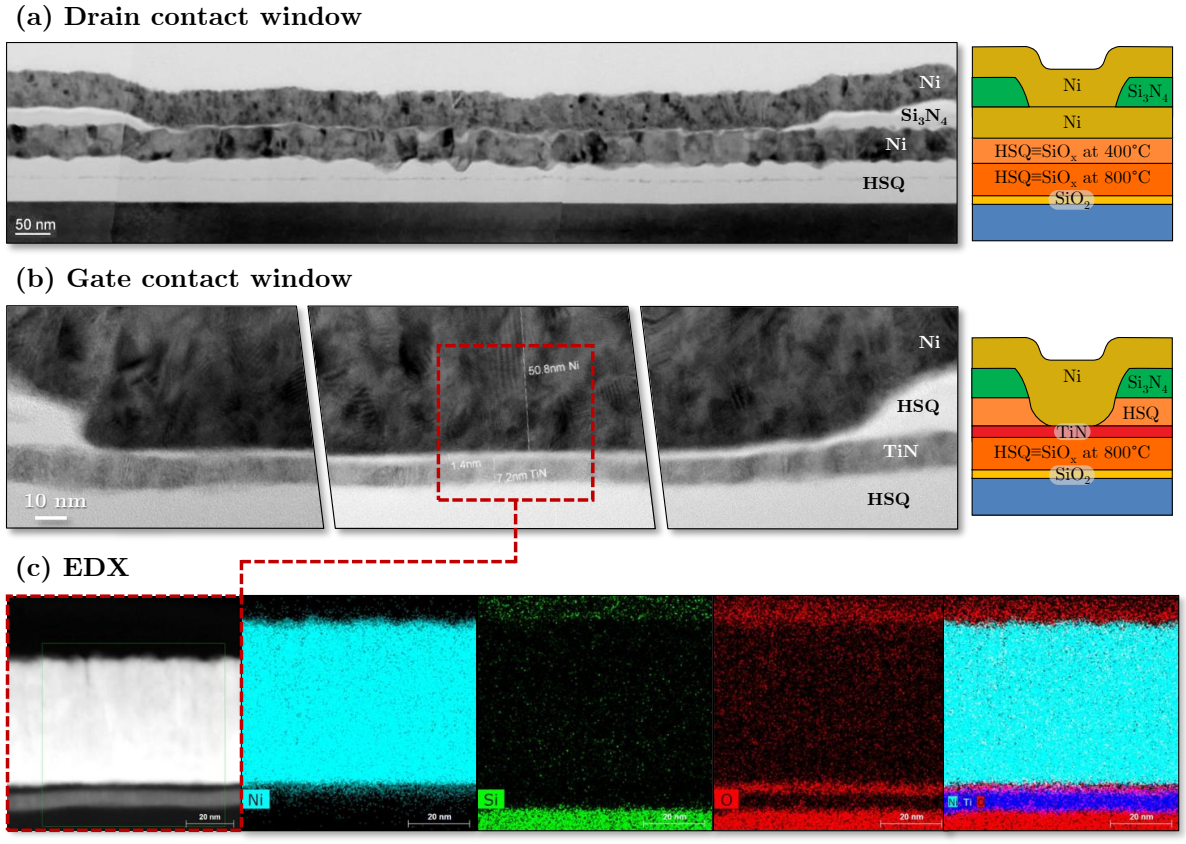


FIGURE 2.31: TEM images of the contact windows at the drain electrode (a) and the gate electrode (b) using Ni as top metal, with EDX analysis of the insulating layer in the gate.

In both cases, there is no Si in the composition of this layer, and therefore it cannot be residues of Si_3N_4/HSQ≡SiO_x caused by underetching. Nevertheless, it has a strong contribution of nickel and oxygen.

In a second attempt, 70 nm Al was used as top metal. Again, TEM analysis was performed in order to find the reason for the resulting high resistive measurements. Fig. 2.32 shows the contact windows etched, with a 3.5−7.0 nm thick layer between top metal and electrodes. In this case, this layer is rich in oxygen, aluminium and carbon. The presence of C and O can be justified as residues of the PMMA resist used in any of the lithography steps. The hypothesis is

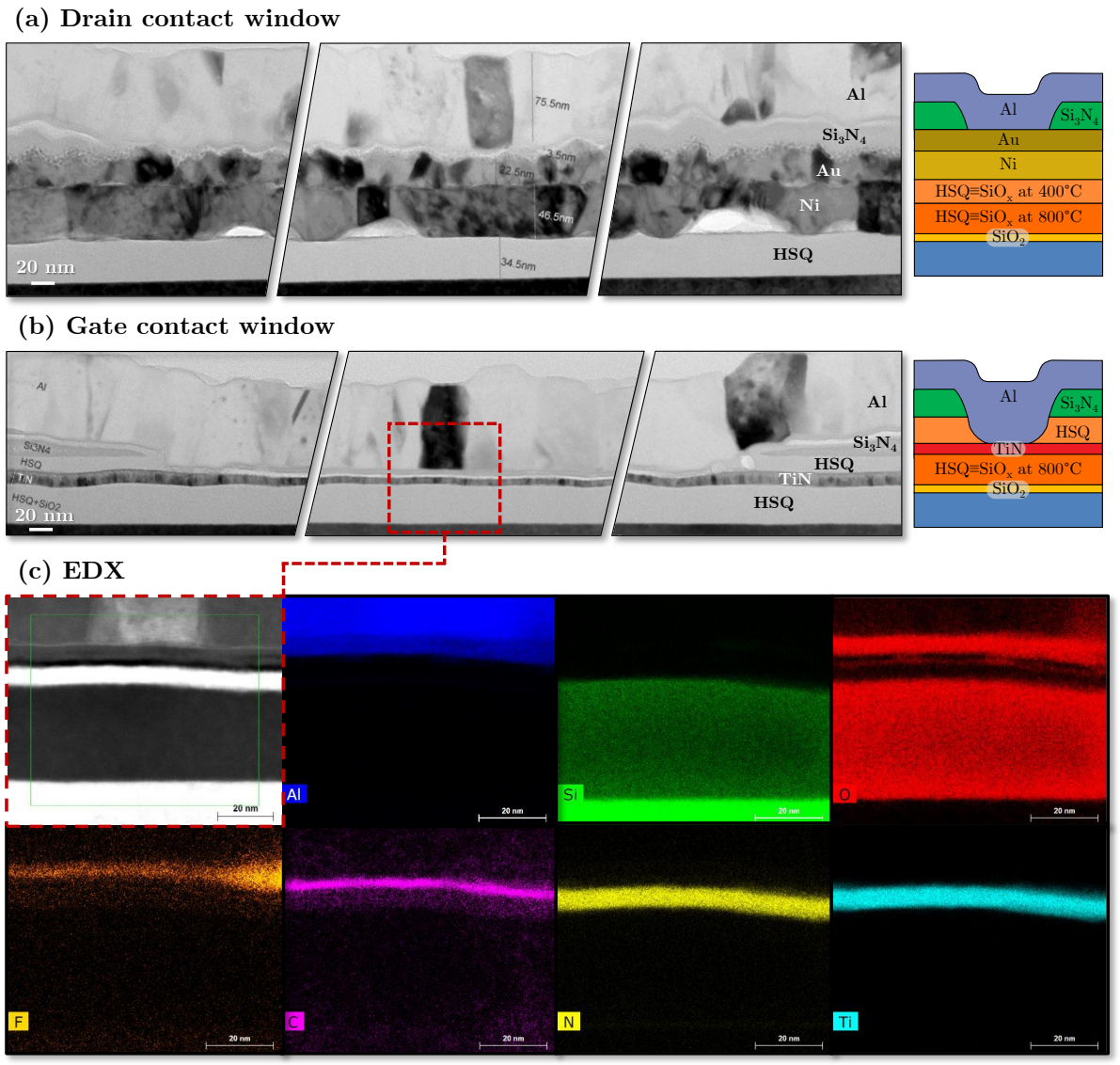


FIGURE 2.32: TEM images of the contact windows at the drain electrode (a) and the gate electrode (b) using Al as top metal, with EDX analysis of the insulating layer in the gate.

that, during the first moments of e-beam evaporation, metal atoms react somehow with these residues, forming the corresponding metal oxide forms.

Two mitigation strategies are followed. First, an additional glow discharge of Argon plasma is done right before any evaporation step; in that way, a slow etch-rate and controlled etching can be performed, removing any possible residue below the metal. And second, instead of Ni or Al

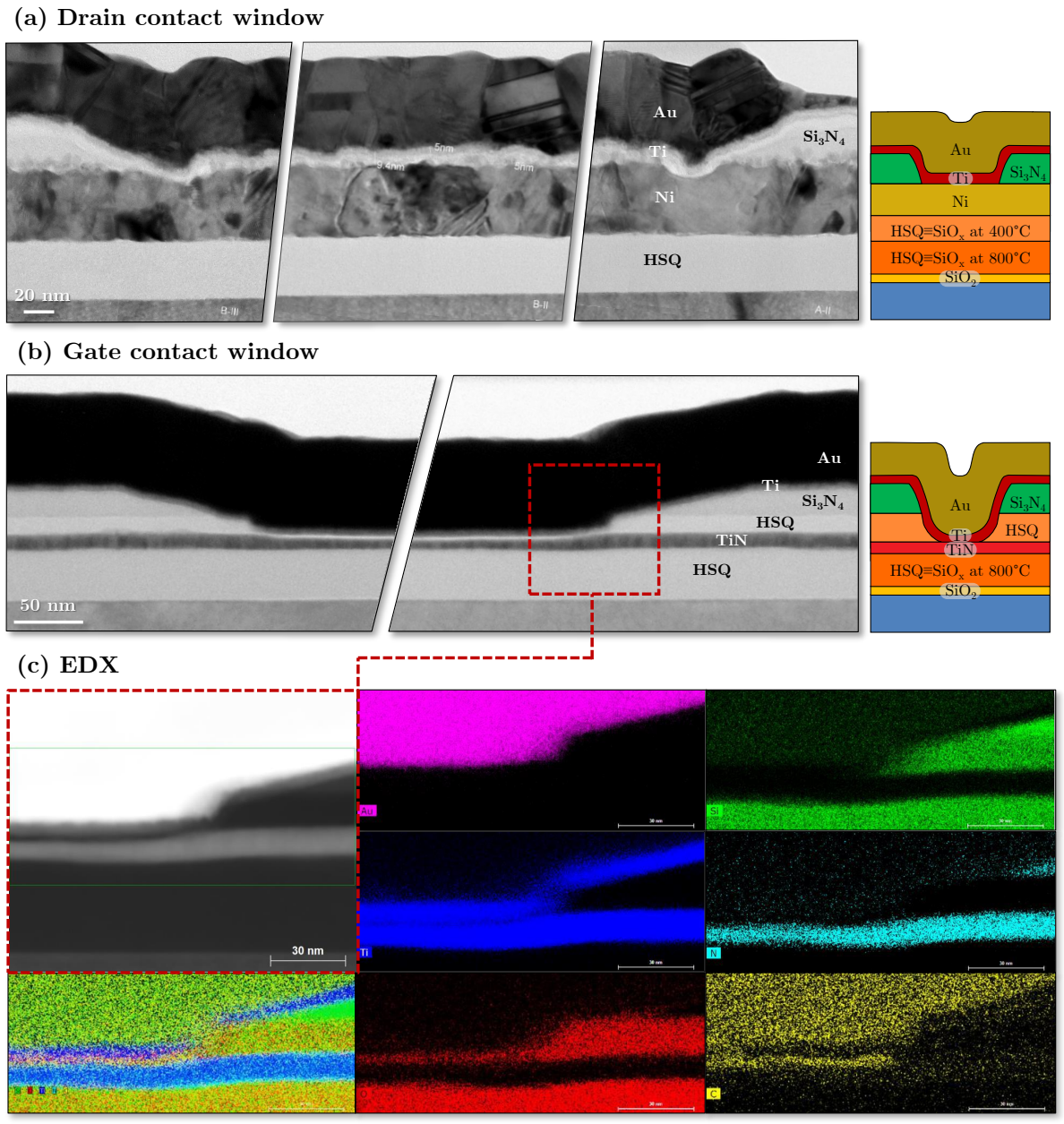


FIGURE 2.33: TEM images of the contact windows at the drain electrode (a) and the gate electrode (b) using Ti/Au as top metal, with EDX analysis of the insulating layer in the gate.

as top metal, a bilayer of 5 nm Ti and 65 nm of Au is used. It is well known that TiO_x with an excess of titanium behaves as n-type semiconductor [70]; therefore, if there is still the case for Ti oxidation, the assumption is that it would still be effective as electric contact.

Fig. 2.33 presents the cross section of the contact windows when using Ti/Au as metal routing. In this case, the thin layer which separates top metal from electrodes consists mainly of titanium, with minor contribution of oxygen. The electrical measurements described in Fig. 2.33 corroborates the suitability of Ti/Au as metal routing.

2.4.8 Summary of integration process optimization

Several of the issues that compromised the SET integration have been addressed in previous sections. First, the use of HSQ as intermetal layer has been proved: its thickness can be controlled through the etch-back mechanism, and insulating characteristics after annealing are ensured. Argon milling conditions for the removal of top oxide have been optimized, although its effectiveness can only be quantified by TEM analysis.

Afterwards, the method proposed for gate definition has been described and proved in terms of AFM measurements and EDX composition. Regarding the drain electrode, a Ni/Au bilayer solves the oxidation issues already described. Following the etching sequence for contact windows opening, a 70 nm Ti/Au bilayer as metal routing is deposited. Fig. 2.34 shows the current voltage characteristics of contact test structures for drain and gate electrodes, after processing with the already optimized parameters. In both cases a low resistive behaviour is observed, supporting the average feasibility of the integration process.

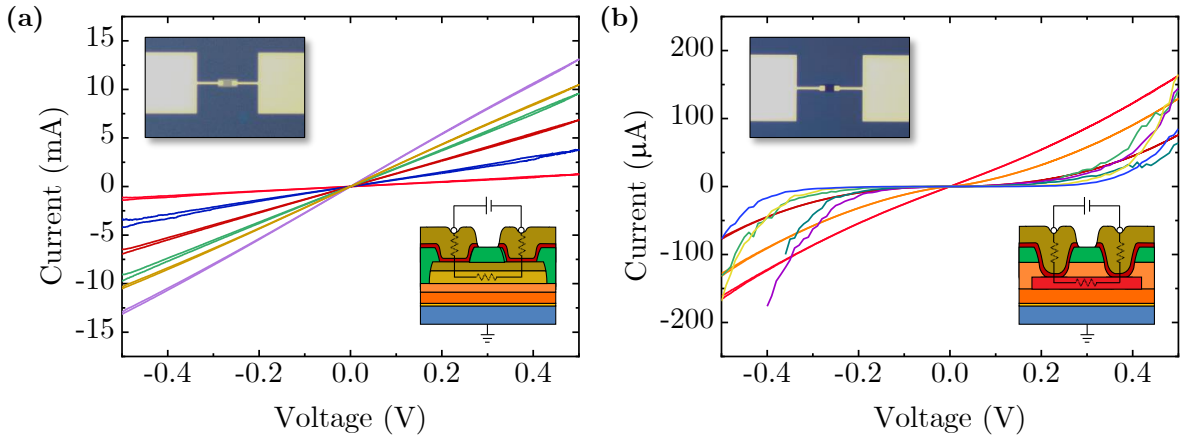


FIGURE 2.34: Current-voltage characteristics of contact test structures for drain (a) and gate electrodes (b), with inset of optical images and schemes of the corresponding stack in each case.

2.5 Final integration process

During the SET integration process, there are some parameters that can be properly quantified (intermetal layer thickness measured by ellipsometry, pillar height in intermediate steps measured by AFM); others that only can be validated by more exhaustive and time consuming methods (top oxide removal and gate definition can only be ensured by TEM analysis); and some others that can be verified just after completing the process (electric leakage between electrodes, only measurable after contact windows etching and metal routing patterning). For that reason, the number of iterations towards the fully contacted SET has been considerably increased. Some of these iterations were used to optimized most of the process steps, and have been described in previous sections. In this section, the application of the overall process described in 2.2 is presented, with more detail of its implication in the pillar structure.

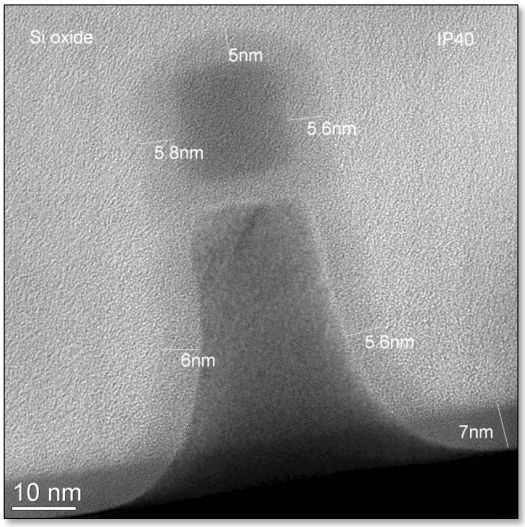


FIGURE 2.35: EFTEM SiO_2 plasmon loss image of a IP40 before integration process.

2.5.1 Initial state

The starting point is the a-Si/SiO_2/c-Si nanopillar patterned according to the conditions described in 2.2.1. In these pillars, the self-assembly of Si NDs takes place as described in 2.2.2, and afterwards plasma oxidation is performed for the generation of a thin oxide layer surrounding the pillar. This oxide is necessary to realize the GAA electrode, and it is used as well to shrink the pillar dimensions. This process step has been already introduced in 2.2.3.

Fig. 2.35 presents an example of an IP40 right before the integration process. As observed, pillar height is close to the nominal ∼71 nm value. A 5−6 nm oxide layer covers all the structure,

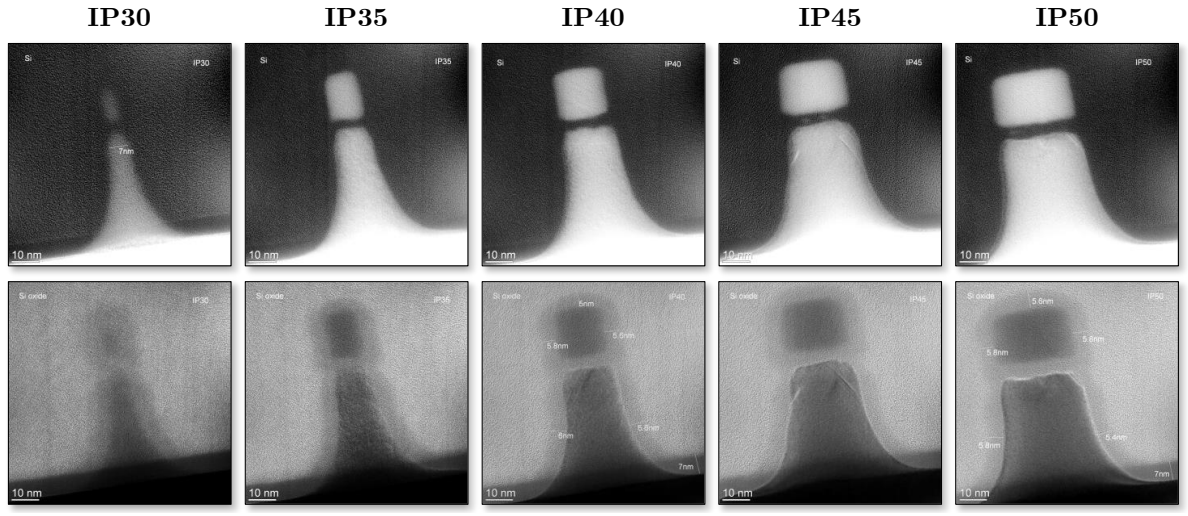


FIGURE 2.36: EFTEM Si (top) and SiO_2 (bottom) plasmon loss images of five pillars before integration.

being slightly thinner on top of the pillar. Similarly, Fig. 2.36 shows the initial aspect of pillars for all five nominal diameters. The fabrication of sub-10 nm structures is proved, as the IP30 is 7 nm wide. However, in this case Si NDs are only visible in larger structures ($\varnothing > 40$ nm).

In parallel, before beginning with the integration process, pillar integrity is validated by AFM measurements. Results are presented in Fig. 2.37. Height is in the same range of values than the ones provided by TEM characterization, subtracting the substrate oxide thickness. Regarding pillar diameter, AFM measurements cannot provide exact values for the critical dimensions. Nevertheless, the difference between pillar widths is again in agreement with Fig. 2.36.

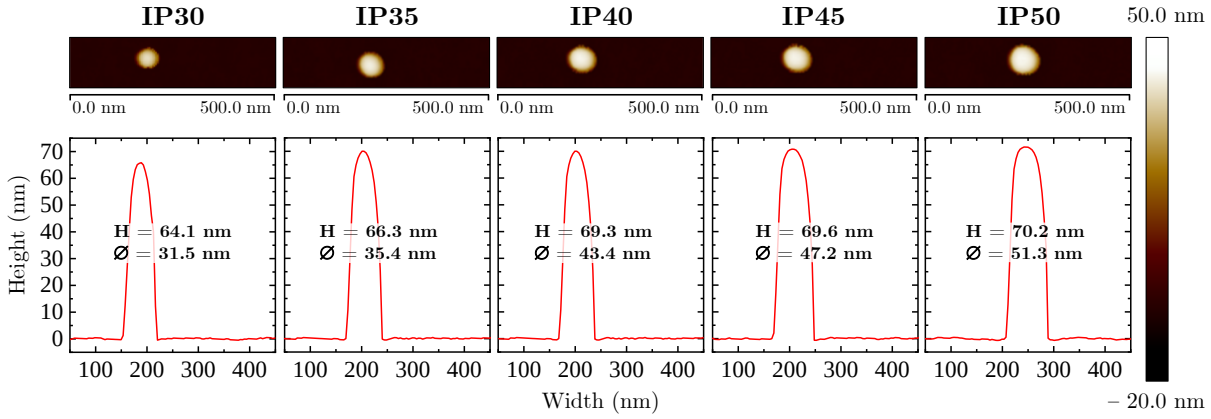


FIGURE 2.37: AFM profiles of five consecutive pillars of different diameter, right after pillar patterning and sacrificial oxidation.

2.5.2 First intermetal layer

Once pillar and Si NDs integrity is validated, the integration process is started. First step is the deposition of the first intermetal layer to insulate the bulk substrate and supporting the gate electrode. This is done according to the conditions described in 2.4.1.

The resist used is a solution of 6% HSQ in MIBK. In order to optimize the planarization of the resulting layer, HSQ resist is deposited in a multiple spin procedure: a 10s spin rotation at 1000 rpm, followed by 30s rotating at 6000 rpm. The first period determines the deposition of a thick layer (∼200 nm), while the second step is used to obtain a flat and low roughness surface. After spin-coating, a soft-bake of 4 min at 80°C is done to evaporate the solvent. The etch-back mechanism is performed by means of diluted 0.025% HF, reducing the thickness down to the targeted value, near the embedded oxide of the pillar. Finally, an annealing of 1h in N_2 at 800°C is performed; note that this annealing reduces around a 21% the resulting thickness.

Fig. 2.38 shows the AFM profiles of five pillars after the etched-back and annealing sequence. Here, the height of the uncovered part of the pillars is around 32 nm; note that this intermetal layer will be further reduced during the Argon plasma milling for top oxide removal. Therefore, these thickness values are considered to be optimum for gate location.

As Fig. 2.38 shows, the narrowest IP30 is not appreciable in this case. The hypothesis is that the sequence pillar patterning and plasma oxidation reduces too much the diameter, and thus the pillar cap either collapses or does not resist the HSQ spin-coating. Although the effect is not always observed, it must be considered in terms of yield throughput of the smallest pillars.

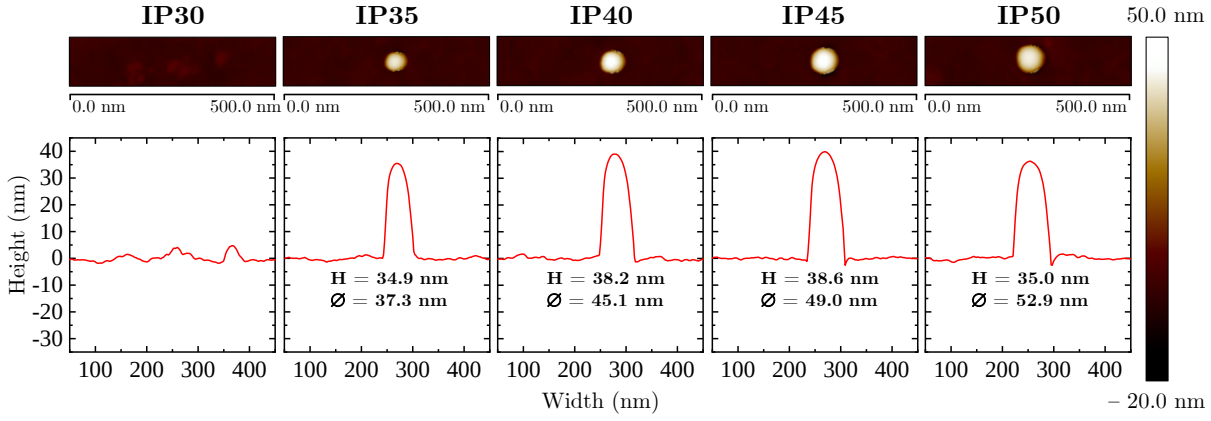


FIGURE 2.38: AFM profiles of five consecutive pillars of different diameter, after first HSQ layer deposition, etch-back and annealing process.

The plasma oxidation includes an intermediate HF etching, which reduces the resulting oxide thickness. In some samples, an additional 0.1% HF etching for 90s is performed right before starting the integration process. And then the first intermetal layer is defined according to the already described conditions. Results of both cases are presented in Fig. 2.39 for comparison; as observed, in the second case there is a significant reduction of the all-around oxide layer (e.g. a reduction in pillar diameter), with no consequent damage on the pillar integrity. This leads to the conclusion that an additional first HF etching may be useful for reducing the oxide on top of the pillar, and it represents no risk neither for the embedded or the gate oxide.

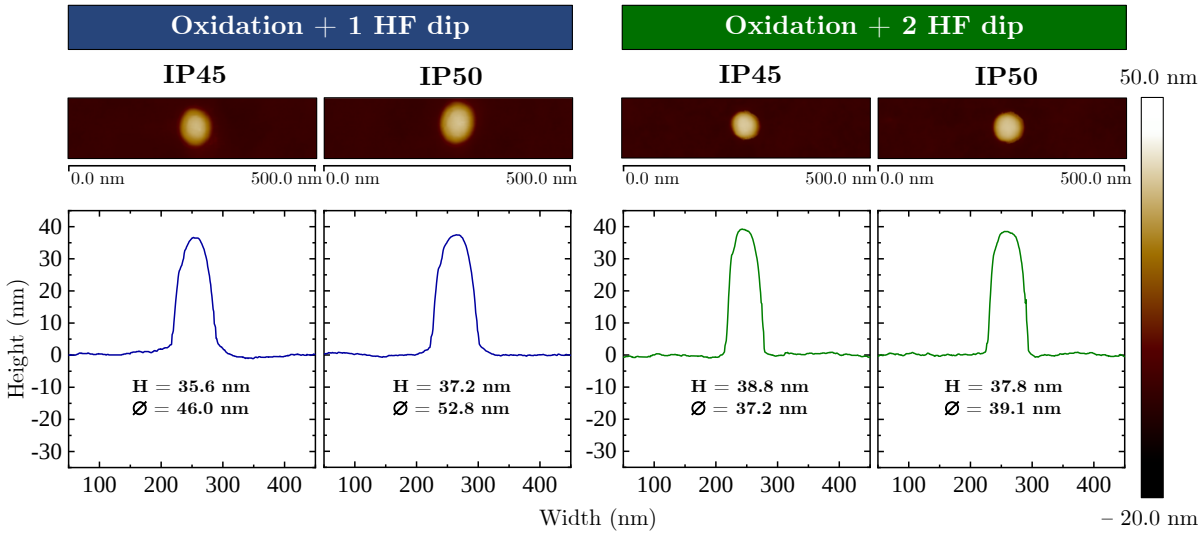


FIGURE 2.39: AFM profiles of two pillars for two conditions of oxidation-HF sequences.

2.5.3 Gate definition

An Argon plasma milling is performed to remove the gate oxide on top of the pillar. Afterwards, a 9−10 nm TiN layer is deposited by sputtering. Gate definition is then performed as in section 2.4.4: an exposed and etched-back HSQ mask protects the TiN from an APM etching, which removes the TiN from outside the region and from top of the pillar.

In Fig. 2.40 SEM micrographs after the gate definition sequence are presented. A rectangular electrode of 3 μm x 8 μm defines the gate region. A closer view of the pillar (c) shows a darker ring around the nanopillar, indicative of the definition of TiN GAA beneath the HSQ mask. In some samples, EDX analysis or AFM measurements in each step of the sequence are performed, leading to similar results as the ones reported in 2.4.4. TEM analysis in next stages of the integration process will be presented, being gate definition one of the key aspects to be validated.

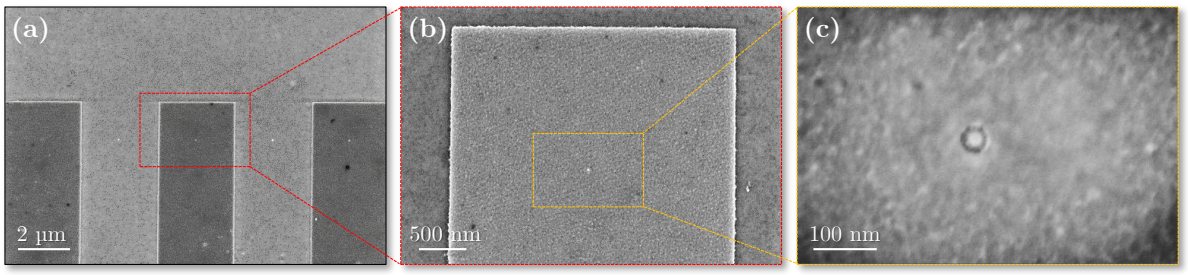


FIGURE 2.40: SEM figures after gate definition, with detail of the three contacted pillars per area (a), the gate region of the central one (b) and the TiN ring around the pillar (c).

2.5.4 Second intermetal layer

One of the most critical issues is to avoid short-circuit between gate and drain electrodes. For this purpose, a second insulating intermetal layer is deposited. The spin-coating and etch-back method is used again, now with an annealing of 1h at 400°C to avoid crystallization effects on the TiN layer. The available distance to place gate, drain and their insulating layer is given by the pillar cap height, barely 25 nm. For that reason, the thickness control in this stage results critical. Note that the process simulator can provide guidance of the target thickness for the second intermetal layer, a parameter function of the thickness of the first one and the pillar height. In this context, the new insulating layer must be between 10−15 nm thin after annealing.

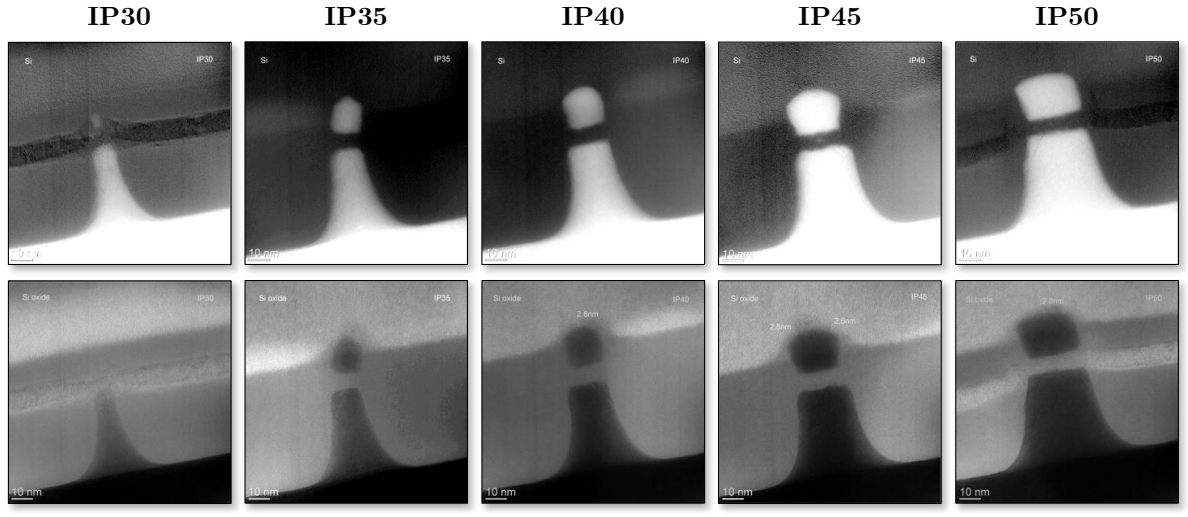


FIGURE 2.41: EFTEM Si (top) and SiO_2 (bottom) plasmon loss images of five consecutive pillars after second intermetal layer etch-back and annealing process.

In this point of the process, test samples are sent for TEM structural characterization with the aim of validating three main issues: top oxide removal, gate definition and proper intermetal layers thickness. In Fig. 2.41 the cross section of five consecutive pillars are presented.

Several aspects can be discussed. First, both HSQ layers are in the range of optimum thickness values: the first one supports the TiN layer right in the embedded oxide height, while the second one reaches almost top of the pillar. The absence of the IP30 pillar cap is in agreement with the AFM measurements from Fig. 2.38; and the bending of the upper part of the IP35 corroborates the affectation of HSQ spin-coating deposition in the smaller pillars.

In this row only IP30 and IP50 are contacted. In order to validate the feasibility of the process in smaller pillars, another IP30 is analysed. Fig. 2.42 presents in more detail the cross section of these two pillars. As it can be observed, in this case the IP30 cap has not been removed. Again, intermetal thickness are in the range of optimum values. TiN is completely removed from top of the pillar and kept all-around in a GAA ring that rises up in vertical about 7 nm. And finally, there is only a very thin oxide layer on top of the IP50, which could also be residues of HSQ originated during the processing. In summary, as Fig. 2.42 indicates, the proposed gate definition sequence can provide gate-contacted nanopillars suitable for SET measurements.

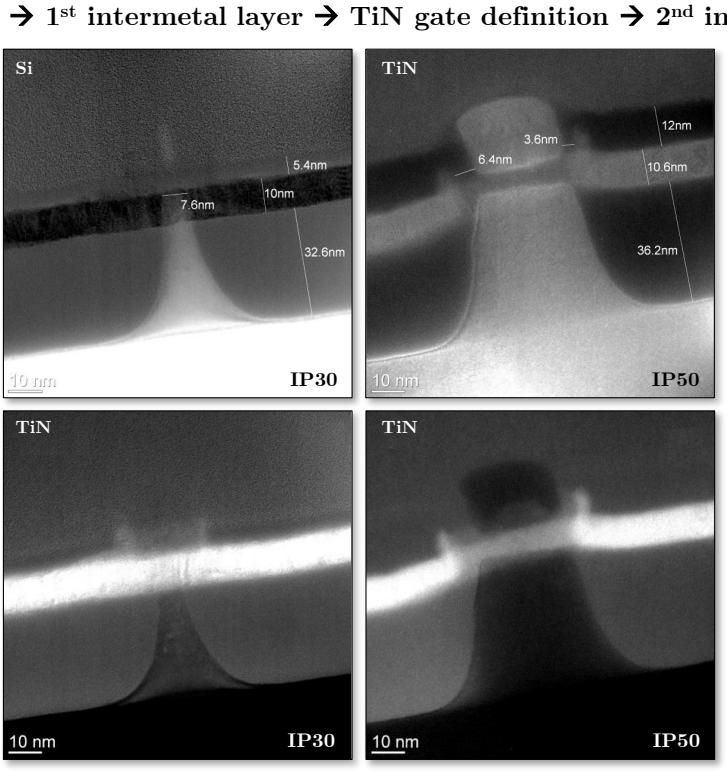


FIGURE 2.42: EFTEM plasmon loss images of IP30 (left) and IP50 (right) pillars after second intermetal layer etch-back and annealing process, with detail of dimensions.

2.5.5 Drain definition

Next step is the definition of a drain electrode with a 50 nm Ni/Au layer deposited by evaporation. The patterning is done by means of e-beam lithography with positive resist: a bilayer of PMMA of different concentrations is spin-coated; the bottom one becomes more reactive to the developer after exposure, and thus a wider opening than in the upper one is obtained, favouring in that way the contact definition by lift-off.

It results essential for the SET operation an effective drain-pillar contact. It is necessary, then, the removal of any remaining gate oxide, HSQ residues or native oxide that may have appeared in the uncovered silicon cap. With that aim, a short etching in 0.025% diluted HF is performed; etching time depends of first and second intermetal layer thickness, gate location with respect of the pillar, and assumption of the remaining oxide thickness on top. In addition to that HF etching, a glow discharge of Argon plasma is performed right before the evaporation, etching around 1−2 nm.

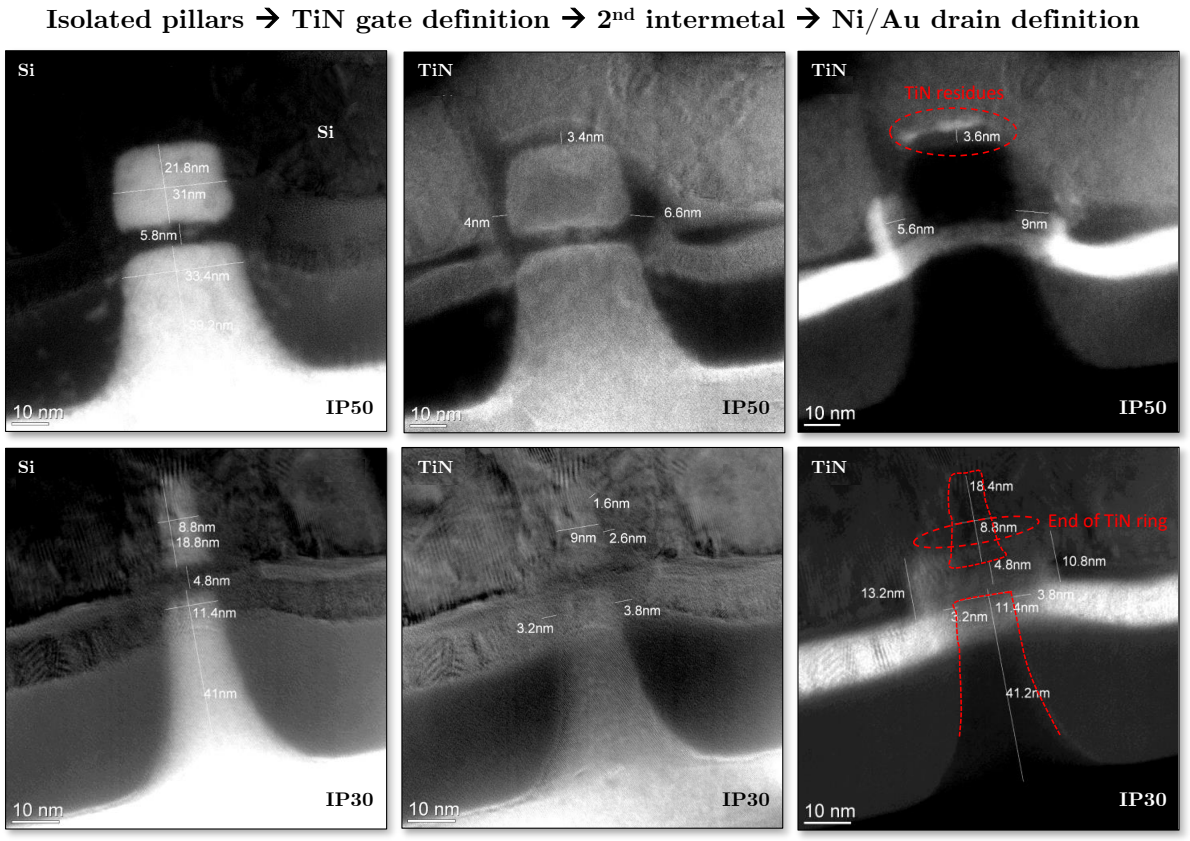


FIGURE 2.43: EFTEM plasmon loss images of IP50 (top row) and IP30 (bottom row) after drain contact definition.

In this stage, Fig. 2.43 presents the TEM cross section of IP50 and IP30 for different detectors. In both cases, the first insulating layer and the gate electrode location are properly adjusted. In the case of the IP50, there are TiN residues on top of the pillar and, below, there is still a 3.6 nm oxide layer. On the other hand, IP30 seems to have the GAA properly defined, with no TiN residues or oxide on top.

Nevertheless, the main issue is that the second intermetal layer is too thin to separate effectively gate from drain, and thus there is a clear short-circuit between them. This situation is consequence of a too aggressive etching before Ni/Au deposition, mainly attributed to the diluted HF contribution.

In a second attempt, a more conservative approach is followed and the diluted HF step is minimized. Fig. 2.44 presents the TEM characterization of an IP50 after drain definition. As it can be observed, in this case both gate and drain are properly defined: TiN is effectively removed from top of the pillar, there is no hint of the presence of top oxide, and apparently there is a good nickel-pillar contact. In addition, both insulating layers are thick enough, with a separation of 3.7−4.9 nm in the pillar between the rising up of the TiN electrode and the sinking of the Ni layer.

The conclusion is that, with a certain process variability, the definition of both gate and drain can be simultaneously provided according the SET requirements.

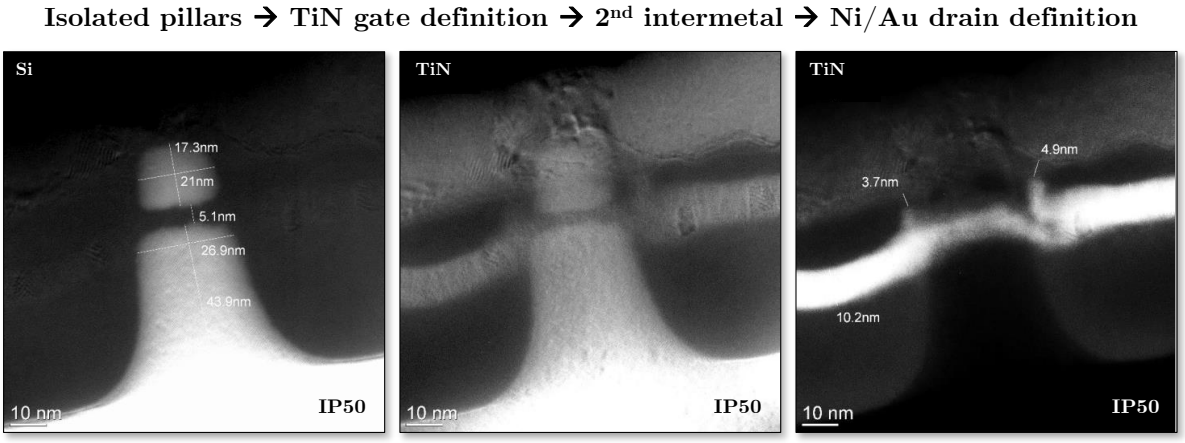


FIGURE 2.44: EFTEM plasmon loss images of IP50 after drain contact definition.

2.5.6 Contact windows and metal routing

After Ni/Au drain definition, a 20−25 nm Si_3N_4 layer is deposited by PECVD at 350°C. By means of another lithography level and a combination of RIE and diluted HF, contact windows are properly etched; AFM measurements are performed in most of the processed samples, with similar results as the ones presented in 2.4.6. Again, the process simulator provides values for the optimum etching time in each sample.

The last step consists in a fourth lithography level, followed by evaporation of 70 nm Ti/Au and lift-off. In Fig. 2.45 the contact pads distribution and the metal stripes are visible. A total of two isolated pillars with common source are contacted per each quadrant (b). In an inner view (c), gate region can be distinguished as the brownish area and drain electrode as the brighter one; contact windows and metal stripes are visible as well. In addition, one of the pillar less dense arrays is contacted (d), and contact test structures are fabricated to check electrical conductivity in each electrode type (e).

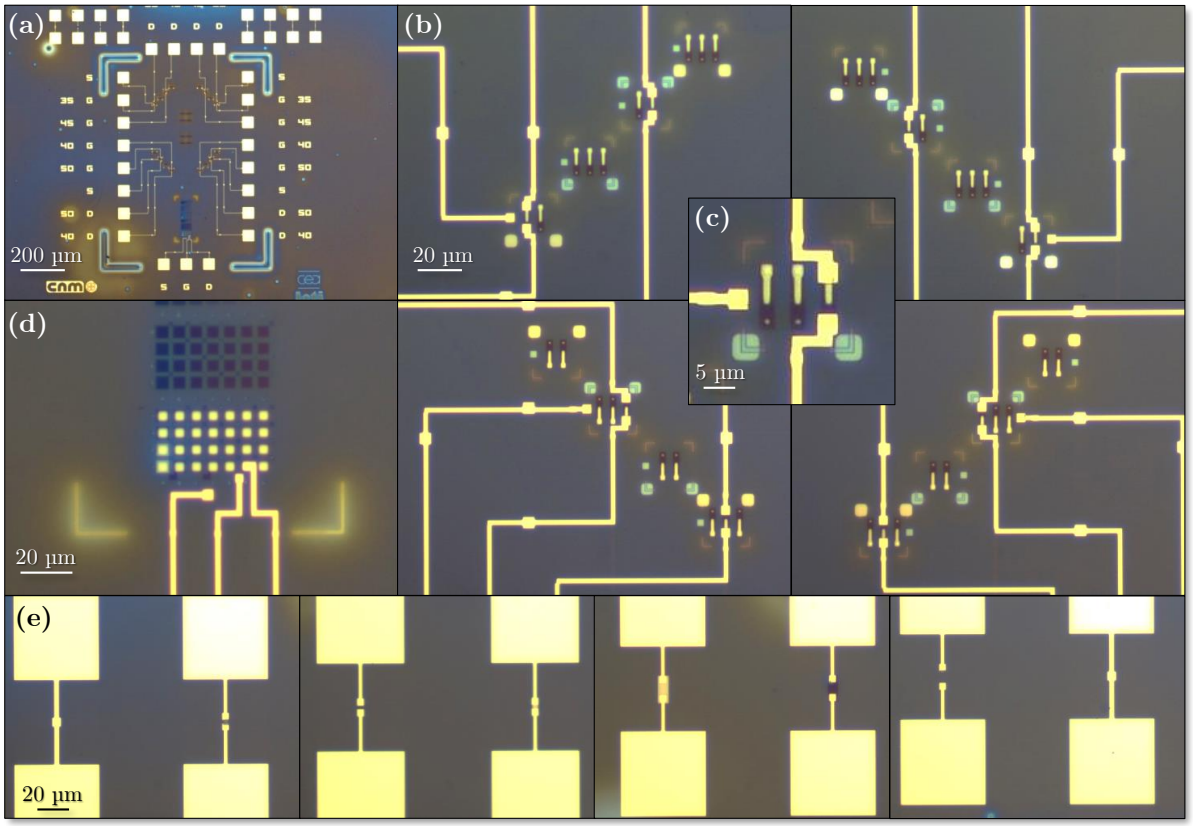


FIGURE 2.45: Optical images of one sample after completion of the process: overall chip (a), all four quadrants (b), example of one inner region (c), contacted array (d) and contact test structures (e).

2.6 Additional contacted structures

Besides the fully integrated SET device, several other structures and configurations are manufactured in order to analyse single electron transfer phenomena. In this section these configurations are briefly presented.

(i) Gate-contacted pillar arrays

As complementary tests, several batches of contacted arrays are developed. The intention is to fabricate the gate electrode in the less dense arrays. In this case, a 9 nm TiN electrode is defined by means of EBL, sputtering and lift-off.

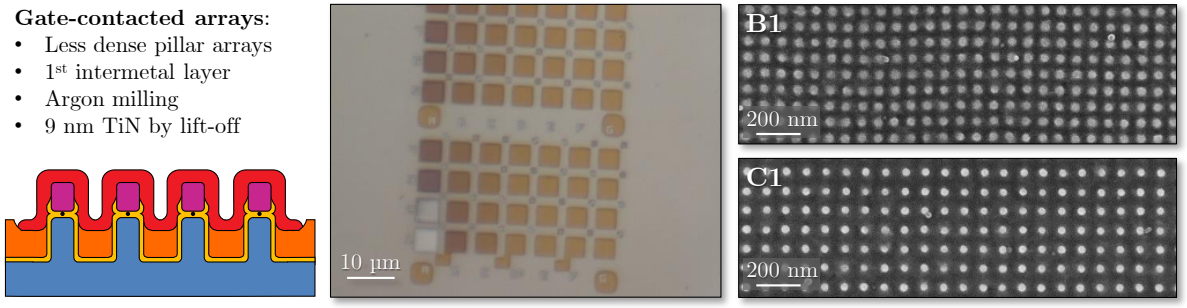


FIGURE 2.46: Sketch, optical image and SEM image of the gate-contacted pillar arrays.

(ii) Drain-contacted pillar arrays

Similarly, in some other samples only the drain electrode is fabricated. In this case, a thicker intermetal layer is defined, and the electrode-pillar surface contact is limited to the top of the pillar cap.

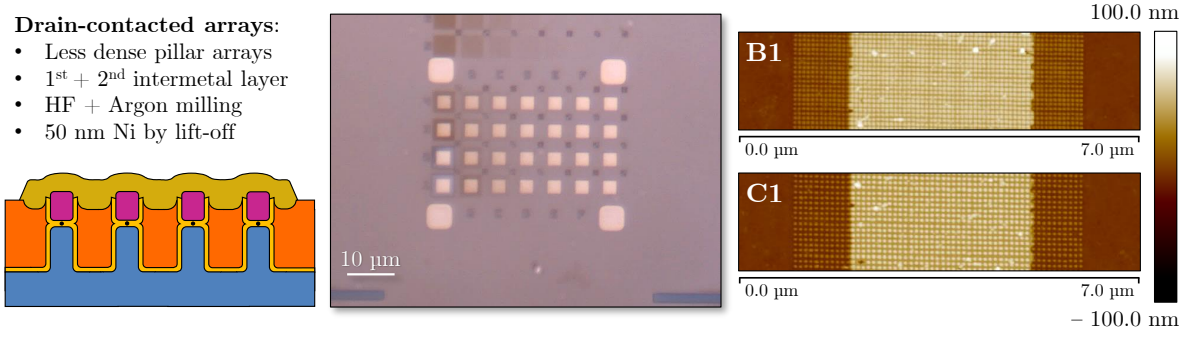


FIGURE 2.47: Sketch, optical image and AFM figures of the drain-contacted pillar arrays.

(iii) Test structure top contact

Among the patterned test structures, there are silicon squares 1 μm wide which are drain-contacted as well for conductive AFM measurements (cAFM). A set of 50 nm Ni pads of different size (from 200 nm to 800 nm) are patterned on top of the structures.

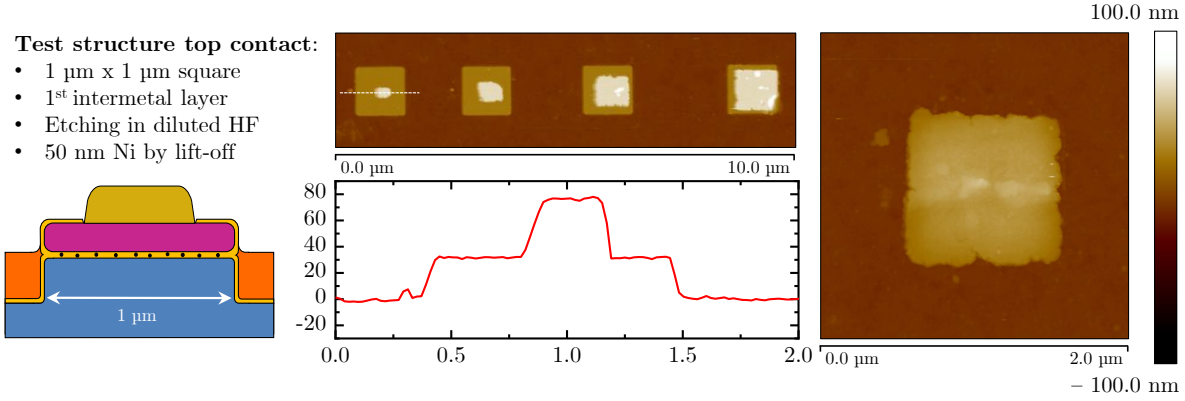


FIGURE 2.48: Sketch and AFM figure of the different top metal contacts fabricated on top of the 1 μm wide test structure.

(iv) Pseudo-pillar top contact

As part of the preparatory experiments for the fully integrated SET, early configurations to be contacted were pseudo-pillars in which only the top a-Si had been patterned; Si NDs were still self-assembled in the oxide layer. In this case the contacting process is similar: a first 20 nm Cr/Pt metal pad is deposited on top of 1 μm wide test structure and on 100 nm wide pseudo-pillars. In this point, cAFM measurements are already viable. Moreover, if the target is current-voltage characterization as in conventional probe station measurements, then the process includes passivation, RIE for contact windows etching and metal routing.

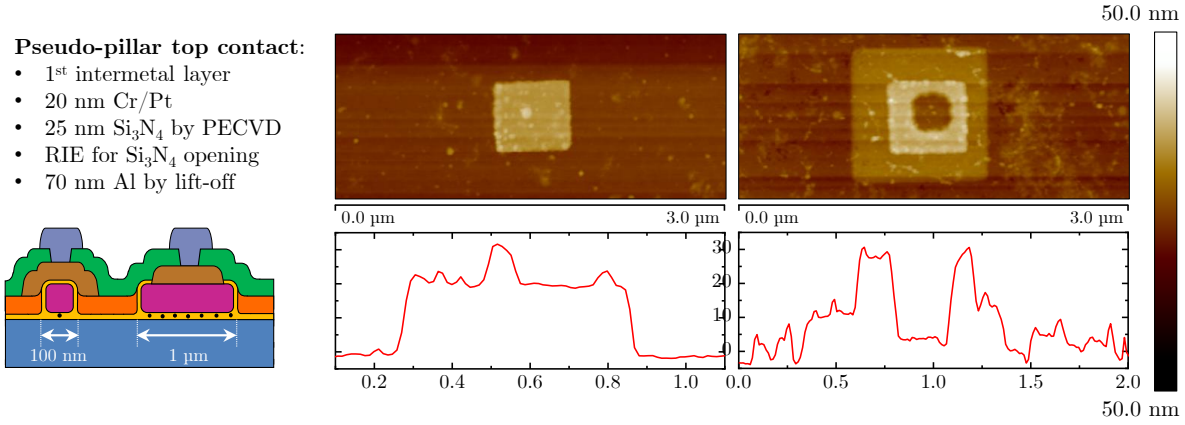


FIGURE 2.49: Sketch and AFM figures of the contacted pseudo-pillar and test structure.

2.7 Electrical characterization

In this section, the most relevant electrical measurements are presented. The cAFM characterization has been performed at FhG-IISB; the current-voltage characteristics from probe station measurements have been carried out at CNR-IMM; and electrical characterization on test structures has been performed at IMB-CNM.

2.7.1 Contacted test structures

The main objective for cAFM measurements is to electrically characterize the influence or success of specific processing steps and related parameters. However, cAFM investigations are usually complicated to evaluate because of several intrinsic issues (e.g. no full control on the measurement, contact between AFM tip and sample not fully reproducible due to local inhomogeneities, change of the tip area with time, etc.). Another relevant complication regarding cAFM, specially for an AFM operating in ambient, is the current sensitivity. Note that levels below 1 pA have to be sensitively measured for single pillars with functional Si NDs embedded in the oxide layer.

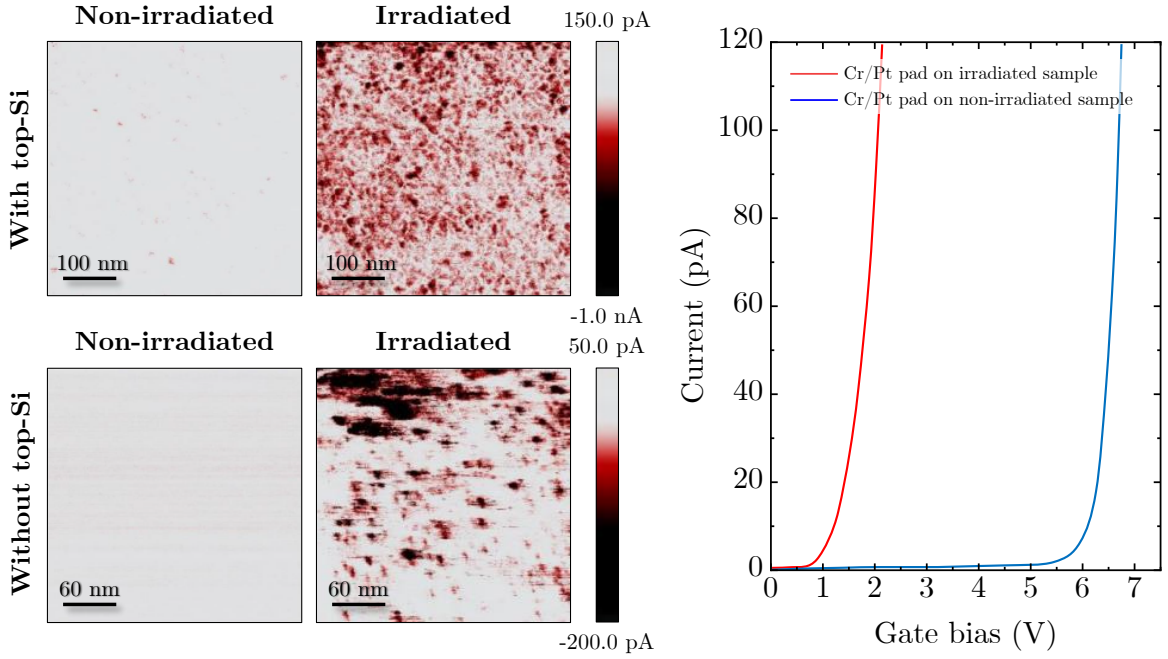


FIGURE 2.50: cAFM current maps for irradiated and non-irradiated samples, with top and without top silicon layer (left). Current-voltage characteristics obtained on Cr/Pt contacts on top of the structures.

From cAFM measurements on the pseudo-pillars and test structures described in Fig. 2.49, the difference between irradiated (with Si NDs) and non-irradiated (without Si NDs) samples can be demonstrated. From the maps in Fig. 2.50, clear evidence of significantly higher density of areas or even dots with much higher current levels for the irradiated samples are obtained. It should be noted that the current patterns observed for the irradiated samples with top Si also exhibit a partially granular structure, which could fit to the Si grains. On the other hand, the current maps for the irradiated sample without the top Si layer mostly shows dot-like spots with increased current level, which can be attributed to the Si NDs. Nevertheless, such patterns in a current map cannot be unambiguously attributed to Si NDs, as such weak features could also be due to defects in the irradiated SiO_x layer. Similarly, Fig. 2.50 shows as well cAFM current-voltage characteristics measured on top of the Cr/Pt pad contacts on the 1 μm^2 Si test structure for irradiated and non-irradiates samples. And clearly, the onset voltage for the irradiated sample is much smaller.

2.7.2 Contacted pseudo-pillar

During process optimization, samples with the already described pseudo-pillar configuration (Fig. 2.49) were fabricated. Among the processed samples, a few ones clearly showed conductance peaks; in the following specific case such peaks were present together with a negative differential resistance (NDR) region, which is generally ascribed to quantized conductance through a discrete level or distribution of levels.

In that way, one of the probed nano-sized structures displayed a behaviour that can be ascribable to the presence of Si NDs. The same behaviour was not shown by any similar non-implanted reference sample. The 4.2 K electrical characterization is presented in Fig. 2.51.a. It can be interpreted as standard resonant tunnelling diode characteristics [71], in which the peak superimposed to the monotonic trend is due to the tunnelling current across discrete levels present in the electron path, and separated by tunnelling barriers from the leads. Such behaviour is well defined and stable upon consecutive voltage scans and thermal cycling (Fig. 2.51.b), which is a first hint against the attribution of the tunnelling to traps due to defects in the structure. An effect of the tunnelling peak on the I−V curve shape can be traced up to room temperature, hence the discrete levels involved cannot be due to the energy levels of isolated shallow donors, impurities or defects which may be active only at low temperature. At 4.2 K the peak has a ∼400 pA amplitude, and the negative differential resistance region of ∼300 pA extends in a voltage range ∼150 mV broad. The tunnelling current peak is rather broad, without sharp edges, and it may be compatible with a distribution of discrete levels induced by the presence of several Si NDs of varying size on the oxide layer under the 100 nm top Si.

The very small ND size and the lack of a gate in the structure imply a reduced total capacitance, and a relatively high charging energy, which can explain why a single tunnelling current peak is evident in the investigated voltage range. However, a closer look to the calculated conductance (Fig. 2.51.c) allows the identification of further peaks when increasing voltage towards negative values. Upon increasing of the voltage, the peak spacing in the calculated conductance tends to reduce. The lack of the possibility to apply a gate voltage to tune the chemical potential levels hampers the extraction of further information from such sample. For that reason, different sources other than the Si NDs may represent the real origin of this quantized behaviour. However, simulations can associate the experimental behaviour to a single Si ND active in the oxide. In addition, the same sample showed also other peaks in the I−V curve, as outlined in Fig. 2.51.d. In this context, due to poor reproducibility with respect other samples, it was not possible either prove or disprove that the observed phenomena was related to single electron transfer through NDs.

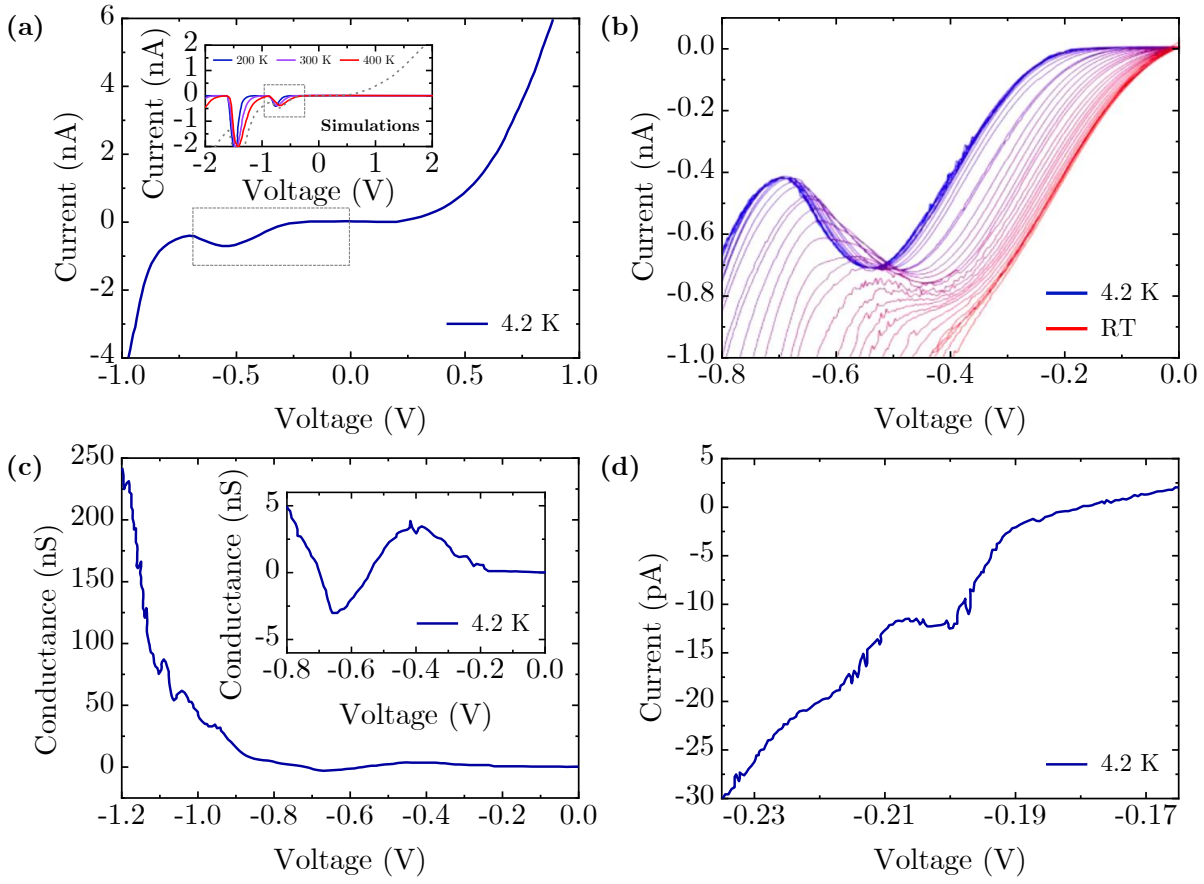


FIGURE 2.51: Current-voltage characteristics at 4.2 K of a 100 nm isolated pseudo-pillar (a), same behaviour as a function of temperature in the interval of interest (b), calculated conductance at 4.2 K and inset of the peak (c) and a particular example of additional small peaks in the conductance curve (d).

2.7.3 Fully integrated pillars

In the first batches of full integrated devices (i.e. with all three electrodes), it was noticed a relatively low yield in terms of gate-drain leakage. As already mentioned during the process description, the insulation between drain and gate is very delicate. To avoid any possible breakdown during measurements, which may have damage the device, large voltage difference between electrodes was avoided. Either only one of them was contacted (keeping the other floating) or they were shorted. In addition, by the latter method it was possible to probe the effect of the gate voltage, although at the same time a large drain bias smoothed the features in the I−V curves. In that way, the conductance calculated from such characterization was termed hybrid conductance, being an intermediate quantity between device conductance and transconductance.

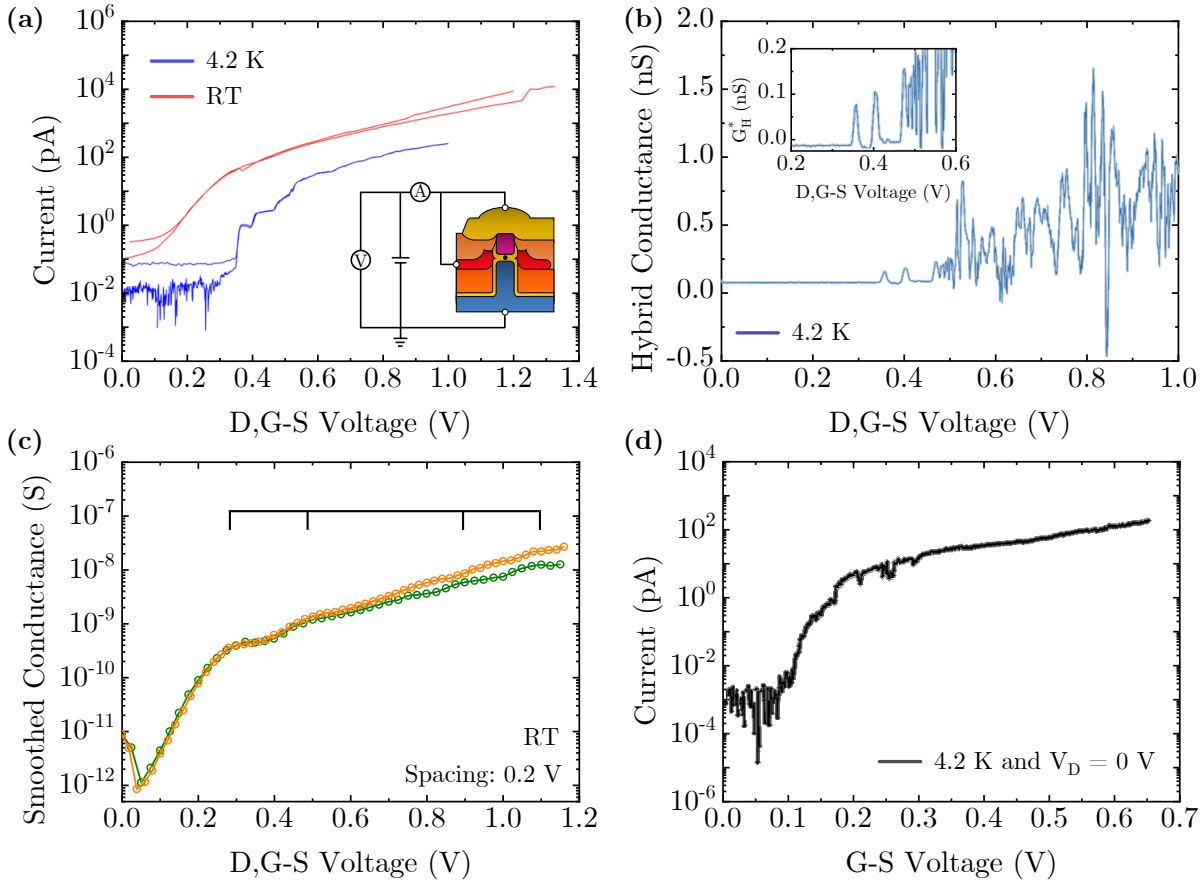
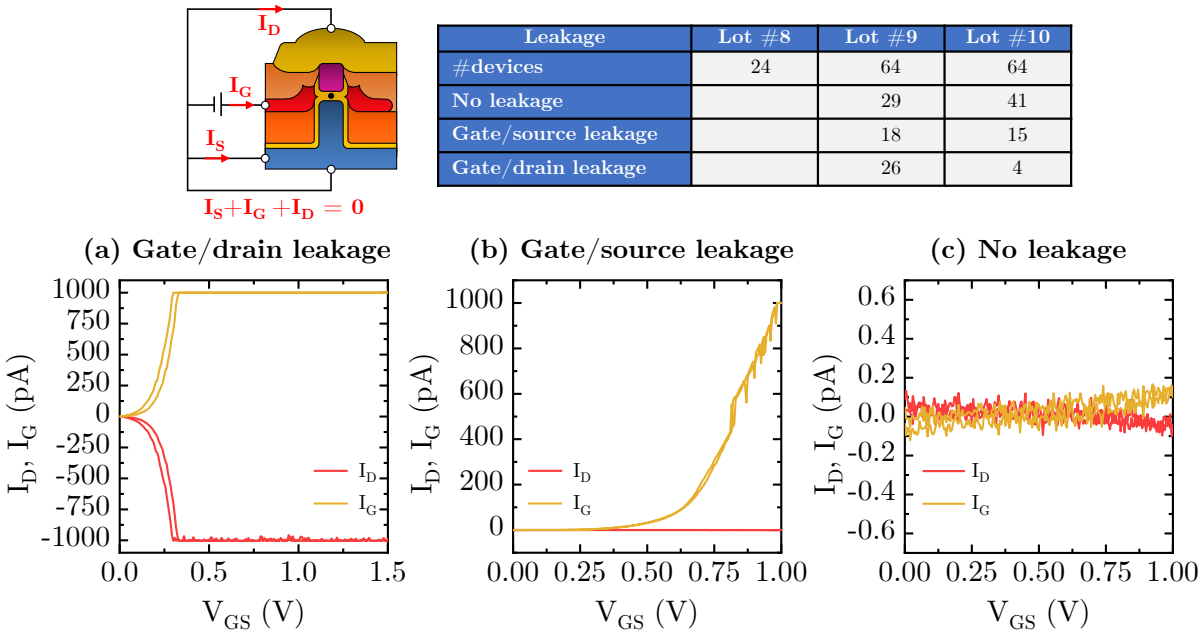


FIGURE 2.52: Current-voltage characteristics at room temperature and at 4.2 K of a pillar array (a), corresponding conductance (b), two consecutive measurements for smoothed conductance at room temperature (c) and current-voltage characteristics without drain bias applied (d).

Several of the measured devices showed Coulomb blockade oscillations in the hybrid conductance as a function of the applied voltage. This is valid both at room temperature and at low-temperature. However, only low-temperature investigations allowed the observation of clear cut oscillations, with conductance values dropping between consecutive peaks, while at room temperature thermal fluctuations intrinsically broaden the current peaks and reduce the peak visibility.

Fig. 2.52.a shows the current-voltage characteristics of one contacted array measured at room temperature and at 4.2 K, where several Coulomb oscillations are observed. Oscillations are more broadened at room temperature, because of the measurement method and of thermal fluctuations, as already mentioned. The hybrid conductance depicted in Fig. 2.52.b shows as well these Coulomb oscillations, with an increased complexity after the first peaks. Applying a flat smoothing of data points in two consecutive measurements, similar plateaus are obtained, as it can be observed in Fig. 2.52.c. Most of the current at high voltage values can be explained by pure gate leakage. Without any applied drain bias, as if drain and source were in parallel towards ground, the resulting current-voltage characteristics are presented in Fig. 2.52.d. Considering that the same current values of the first configuration are observed in the second one for halved voltage or even less, then the drain-gate leakage should be at least as high as the gate-source leakage. Hence, with this configuration it makes no sense to record a stability diagram for the presented device.



Leakage	Lot #8	Lot #9	Lot #10
#devices	24	64	64
No leakage		29	41
Gate/source leakage		18	15
Gate/drain leakage		26	4

FIGURE 2.53: Sketch of the SET with the different types of leakage and summary table of last lots. Example of gate drain leakage (a), gate/source leakage (b) and no leakage (c)

In this point, several new batches were provided in an iterative way, and some of the process optimization approaches described in section 2.4 were implemented. After identifying these leakage issues, in all the new batches preliminary measurements were performed in order to monitor the yield. Fig. 2.53 summarizes the types of leakage found in last lots, with an example in each case. It is important to mentioned here that the origin of these leakages is not the HSQ≡SiO_x intermetal layer, as in contact test structures similar insulation performance as in Fig. 2.20.a was observed. The hypothesis is that the leakage channel is located at the pillar. A too thin or too etched gate-all-around oxide, not enough insulation between gate electrode and the bottom part of the pillar, might explain the gate/source leakage. Similarly, the gate/drain leakage can be induced by a too thin junction in the upper part.

Nevertheless, the alternatives already described for process optimization led to improvements in terms of leakage mitigation. The last lot #10 presented no leakage in 64% of the devices. Hence, the investigation of stability diagrams is possible in such samples, and results are presented in Fig. 2.54. However, in most devices only negligible current is observed, both at room temperature and at 77 K. Note, again, that the efficiency of drain and gate electrodes are somehow opposite, as both electrodes must be placed in a reduced vertical distance of less than 25 nm (the height of the pillar cap), besides their insulating layer. In order to minimize the experienced gate-drain leakage from previous lots, in the last batches the drain electrode was targeted as far as possible from the gate, but still in contact with the very top of the pillar. In this approach, the risk of having a remaining insulating layer between drain and pillar is increased, and therefore it is also increased the possibility of having a configuration that prevents SET operation.

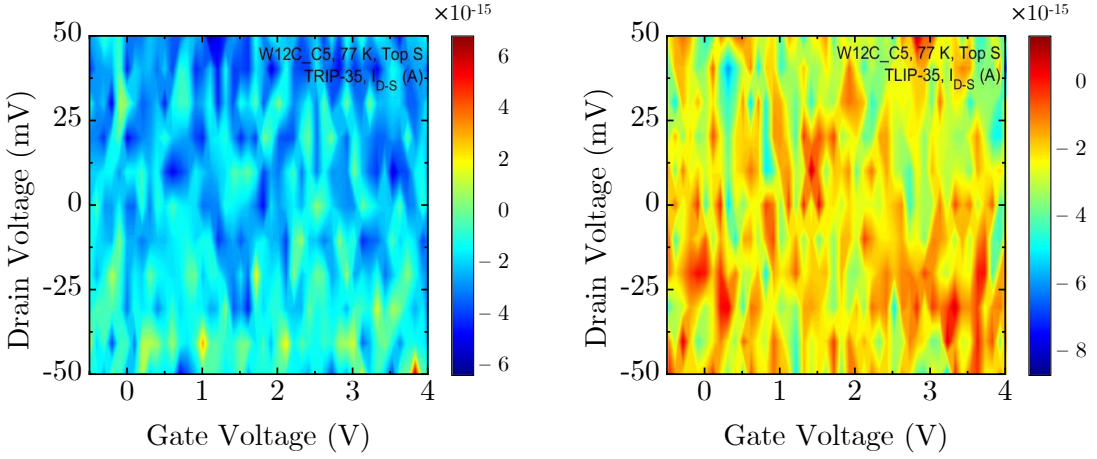


FIGURE 2.54: Stability diagram of an isolated pillar on the latest lot at 77 K.

In some of the latest samples some unexpected effects were observed: smooth oscillations in the negative resistance range, only observable when moving from positive to negative drain bias values. Results are presented in Fig. 2.55. A first preliminary analysis associated this effect with cyclic voltammetry features, consequence of the movement of ions or atoms within the structure due to the change of their oxidation states [72], [73].

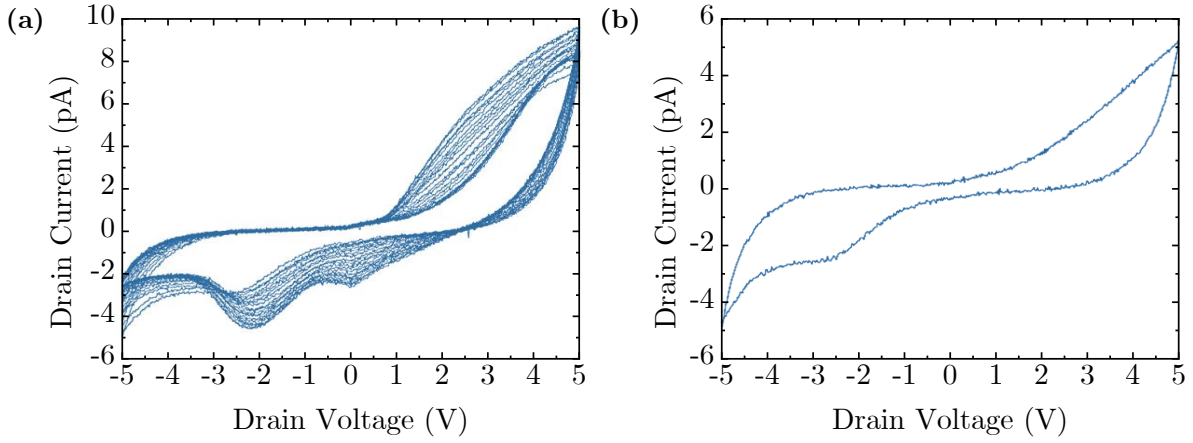


FIGURE 2.55: Current-voltage characteristics for some of the latest devices, in which the ion motion induced cyclic voltammetry features.

2.8 Conclusions

In this chapter the integration process for the fabrication of a SET based on a vertical $Si/SiO_2/Si$ nanopillar has been presented. First, the patterning of nanopillars and the self-assembly of Si NDs in the embedded oxide have been described in terms of modelling, and afterwards with more detail of the experimental conditions.

A process simulator has been built based on the SET requirements. Some of the process steps are based on innovative approaches and have been strongly optimized. One of them is the use of HSQ as intermetal layer; good dielectric characteristics and planarization capabilities around patterned nanostructures have been proved. In addition, most of the TEM analysis already presented show the intermetal layer supporting electrodes at the right height; this is an indicative of the precise thickness control during the HSQ etch-back process.

The combination of this asset, together with the rest of the processing optimization, has led to three main milestones regarding pillar contacting. Fig. 2.56 presents the corresponding TEM

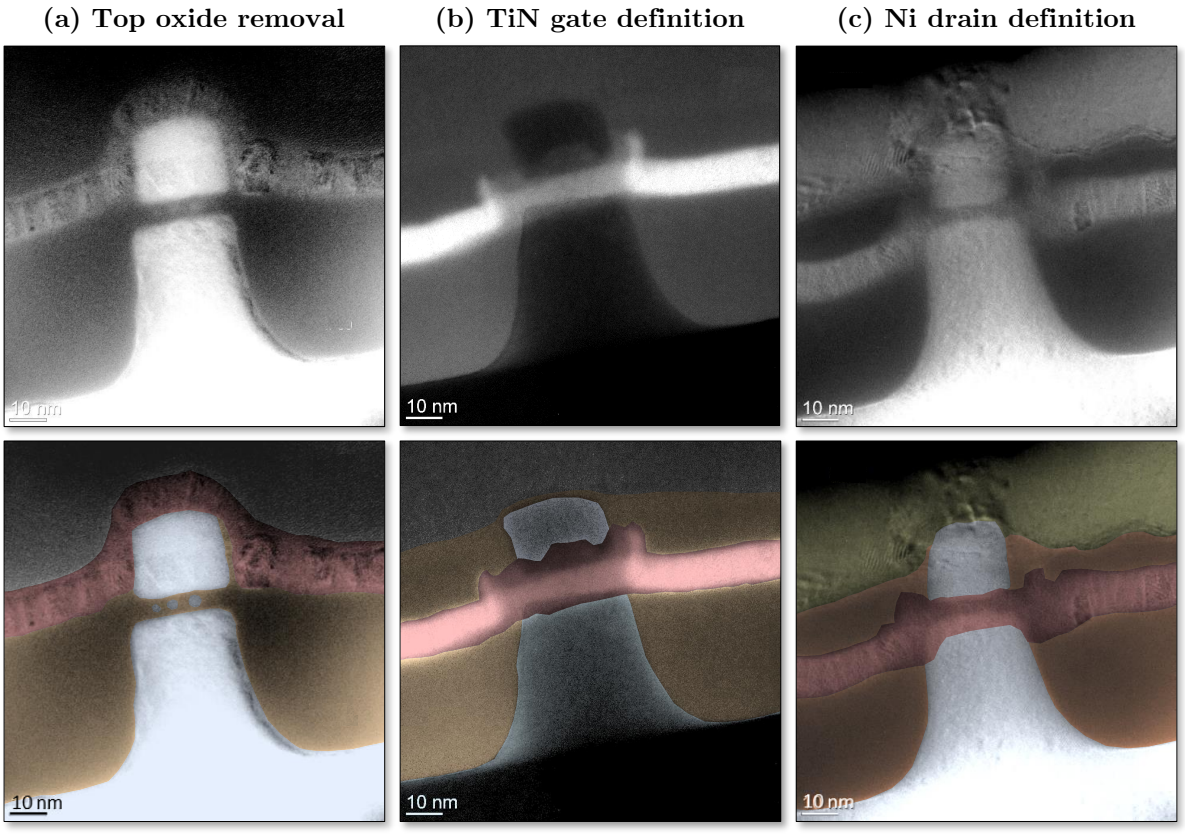


FIGURE 2.56: EFTEM plasmon loss analysis and corresponding coloured image for IP50 after top oxide removal (a), TiN gate definition (b) and Ni drain contact definition (c).

structural analysis for such features, with detail of a coloured version of each one to illustrate the material boundaries. First, the Argon plasma milling conditions have been adjusted to the proper removal of the top oxide from the pillar (a); note that this was not a conventional etching step, and the result is as important as ensuring the TiN-pillar contact. In this particular case, even Si NDs are visible. A second achievement is the success of the gate definition process (b). The available technology did not enable the non-conformal deposition of TiN as gate electrode, and therefore the TiN removal hampered the overall process. Given the available distance, extremely thin masks were necessary, which could protect the material in the gate region while allowing the removal from top of the pillar. A lithography with HSQ as negative resist and using again the etch-back mechanism led to masks around 10 nm thin, and a latter TiN etching resulted in a GAA properly defined at the embedded oxide layer, as visible in the TEM analysis. And finally, the most critical issue has been contacting the drain electrode to the top of the pillar (c). TEM characterization has proved that the simultaneous generation of gate and drain is feasible; very thin dielectric layers separate both electrodes, but nevertheless TiN is removed from top of the pillar while Ni is in contact.

The already mentioned requirement of having a short distance to place two contacts has been the most demanding issue. It consisted in a trade-off between placing the gate a little lower, or the drain slightly higher, and then the device is not operative. Moreover, if both contacts are placed at the targeted positions, the probability of having drain-gate electric leakage is strongly increased.

And this has been clearly observed in electrical measurements. The only results that can be ascribable to the presence of NDs have been either without gate (Fig. 2.51) or with gate-drain shorted (Fig. 2.52). Therefore, the observation of full SET behaviour at room temperature has not been completed, mainly due to a combination of a high level of dimensional constrains and a certain variability process.

In summary, in this chapter the set up of feedback cycles, based on TEM and electrical characterization, has led to the continuous improvement of the integration process. During this progress, negative differential resistance effects and hybrid conductance peaks have been observed, strong indicative of the future feasibility of the vertical SET device.

Chapter 3

SET integration into CMOS technology

After the description of the Single Electron Transistor (SET) integration process, in this chapter the manufacturability of a room temperature SET in a CMOS compatible technology is explored. The main objective is to develop a hybrid circuit demonstrator in order to appraise the SET potential for low power electronics, in particular through its combination with a Field Effect Transistor (FET). While the SET keeps the vertical configuration already described, the FET is a planar device. In addition, FET fabrication is compromised by factors as thermal budget, pillar integrity or output current. Based on these requirements, in this chapter the FET fabrication is optimized towards the SET-FET integration.

3.1 Introduction

The SET results from a vertically stacked $Si/SiO_2/Si$ nanopillar with silicon nanodots (NDs) in the embedded oxide layer [18]. These NDs are formed by ion beam mixing and cluster growth during annealing at elevated temperatures. In early stages SET could only operate at cryogenic temperatures [46], but recently it has been observed that for quantum islands below 5 nm it can be operative at room temperature [31], [32]. Therefore, as these NDs are under 3 nm, the SET operability at room temperature is achievable due to its Coulomb blockade low capacitance.

SETs present high potential in terms of device capabilities, since they can work with extremely low power consumption and high sensitivity [43], [44]. However, SET integration in large scale manufacturing is still challenging. In this framework, its combination with CMOS technology

could benefit from high integration as well as low power consumption [34]. For instance, FET presents advantages like high-speed, voltage gain and input impedance [74]. Thus, by combination with FET technology, a hybrid SET-FET circuit may benefit from SET advantages, while overtaking its intrinsic drawbacks as background noise or device instability [75].

On the other hand, the current technological maturity of CMOS devices is the result of many decades of investigations [76], [77]. Due to their electrical and mechanical robustness they have been widely implemented in integrated circuits. Nowadays, the extensive understanding of CMOS processing, modelling and integration opens a broad spectrum of possibilities for hybrid circuit designs. For all these reasons, here the fabrication of a hybrid SET-FET circuit is presented, along with the preliminary investigations for process conditions optimization and circuit design.

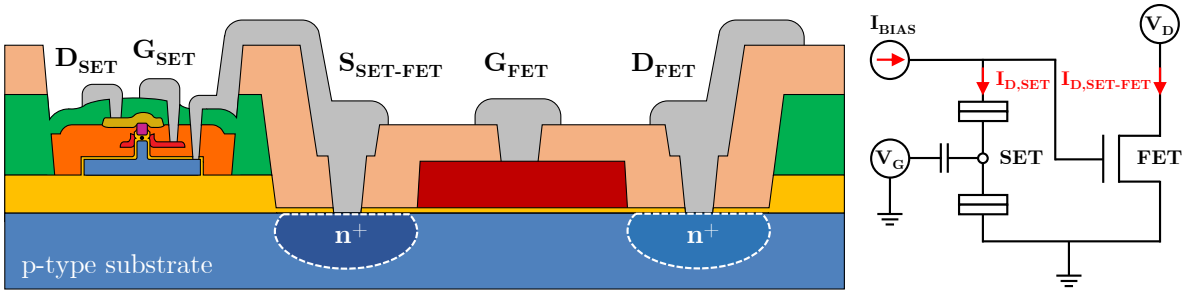


FIGURE 3.1: Sketch and corresponding circuit for the SET-FET hybrid device.

Fig. 3.1 shows the sketch for the hybrid SET-FET device to be developed. Regarding the SET, its integration process is explained in detail in Chapter 2. About the FET element, the starting point is the NMOS part of a reference CMOS technology available at IMB-CNM. Several aspects must be considered in view of the complete SET-FET integration. In particular, the thermal budget after Si NDs formation is limited, since a high temperature process might result in NDs dissolution and consequent SET inoperability. Therefore, the FET to be fabricated differs in several process steps from the standard conditions. Fig. 3.2 illustrates some of the most relevant changes from the reference CMOS with respect the FET to be fabricated. This table summarizes some of the results described along the chapter, and will be further discussed in next sections. The most notably difference modification incorporated in the process is that required temperature must be below 900°C.

Nevertheless, as the fabrication technology is very well established [78], [79], the possibility of tuning process conditions for specific aims is a significant drive towards the SET-FET integration. Moreover, the complete process must be preceded by preliminary investigations, guided as well by predictive simulations of physical processes and device characteristics.

Process	Reference CMOS		FET (SET-compatible)
Substrate	Epitaxial p-type (Boron) 22.5 µm silicon wafer, resistivity 6 – 30 mΩ cm (0.1 – 1.0 x 10^{15} at/cm^3)	≠	**Standalone FET:** p-type (Boron), 4 – 40 Ω cm **SET-FET:** p-type SOI wafers, resistivity 8 – 22 Ω cm (0.6 – 1.7 x 10^{15} at/cm^3)
Field oxide	Field oxidation: 7.5h at 950°C	≠	**Standalone FET:** N-well oxidation at 1050°C **SET-FET**: the SOI buried oxide acts as field oxide
	Implantation for increasing the doping below the field oxide in the p-type regions: BF_3 gas, 5.5x10^{12} at/cm^2, 150 keV		Not required
P and N well definition	Implantation in the N-well region: Phosphorus and Argon, 8.9x10^{12} at/cm^2, 90 keV		Not required
	Implantation in the P-well region: BF_3 gas, 5.0x10^{12} at/cm^2, 50 keV		Not required
	Well oxide annealing: at 1200°C		Not required
Gate oxide	Target of 36.5 nm as gate oxide: at 950°C	≠	Target of 36.5 nm as gate oxide: 114 min at 900°C
Channel implantation	Implantation for threshold voltage adjustment: BF_3 gas, 1.7x10^{12} at/cm^2, 50 keV	=	Implantation for threshold voltage adjustment (only in 2/4 wafers): BF_3 gas, 1.7x10^{12} at/cm^2, 50 keV
Polysilicon deposition	Polysilicon deposition by LPCVD: at 630°C	=	Polysilicon deposition by LPCVD: at 630°C
	Polysilicon doping by $POCl_3$: 21 min at 950°C	≠	Polysilicon doping by $POCl_3$: 16 min at 850°C
Source/Drain regions implantation	Implantation for Source/Drain regions in NMOS: Phosphorus and Argon, 4.2x10^{15} at/cm^2, 100 keV	=	Implantation for Source/Drain regions: Phosphorus and Argon, 4.2x10^{15} at/cm^2, 100 keV
	Implantation for Source/Drain regions in PMOS: BF_3 gas, 1.0x10^{15} at/cm^2, 50 keV		Not required
TEOS passivation layer	TEOS deposition by PECVD	=	TEOS deposition by PECVD
	TEOS interlevel fluidification: 2.25h at 1000°C	≠	TEOS interlevel fluidification: 30 min at 850°C
Metal routing	Al:Cu deposition by sputtering	=	Al:Cu deposition by sputtering
	Al:Cu annealing: at 350°C in N_2/H_2	≠	Al:Cu annealing: at 350°C in N_2

FIGURE 3.2: Comparison of some of the process steps in standard CMOS technology with respect the SET-compatible FET fabrication.

The chapter is arranged as follows. First, the overall description of the process sequence is presented, according to the requirements for each of the integrating parts. Afterwards, the SET-FET hybrid circuit is analysed in terms of threshold voltage and parasitic elements. It is followed by the process simulation of the standalone FET under the modified process conditions. Once simulations have defined the major requirements for fabrication, several experimental tests are performed in order to verify the feasibility of the process. Then, a batch of standalone FETs are fabricated and characterized. These devices serve as a pre-test for the final SET-FET fabrication.

3.2 SET-FET overall process

3.2.1 Process sequence

The purpose of the following investigations is to combine the SET integration process into CMOS technology, with the specific proof of concept of a hybrid SET-FET circuit device. With this aim, the requirements of both processes are considered in order to resolve the optimum sequence. Fig. 3.3 presents the work baseline for the SET-FET fabrication, with detail of the different partners involved.

The first target is to fabricate silicon pillars around 70 nm high with the already mentioned configuration (Fig. 2.3). That is a first 40 nm crystalline silicon layer, then a 5−10 nm thin SiO_2 layer and on top 25 nm of amorphous silicon. The nanopillar structure is achieved by patterning all three layers through a negative resist and SOC/SiARC mask by means of Reactive Ion Etching (RIE) [60]. Ion irradiation allows the atomic intermixing between layers, generating silicon NDs on the embedded oxide layer and thus forming the key element of the single electron device. The main difference with the structure described in Chapter 2 is that now the SET pillars must be fabricated on SOI substrates with a patterned top-silicon island; in that way, both SETs and FETs have independent source contacts. All these processes take place at CEA-Leti at 8" wafer level. It must be taken into consideration that temperatures above 900°C might compromise the pillars and NDs integrity. And besides, the FET-related fabrication processes may induce a mechanical stress on the pillar structures if no specific protection is applied.

In order to turn these structures into 10−30 nm wide pillars, thinning the silicon pillar is possible through a sacrificial oxidation. A sequence of silicon oxidation and wet etching is used, shrinking the pillar final dimension and generating at the same time a very thin oxide layer all around the pillar. This oxide layer is required to turn the pillar structure into a functional device: a thin oxide all around the pillar is needed so that it may act as gate oxide. This plasma oxidation and wet etching sequence is carried out at the facilities of FhG-IISB and a contracted external company, either at 8", 4" wafer or chip level.

This configuration is then integrated into a SET device by following the process depicted in Fig. 2.8, 2.9 and 2.10. This is realized in the cleanroom facilities of IMB-CNM, and is performed at chip level (1.5 cm x 1.5 cm), since this is the shape limitation of the high-temperature tube furnace optimized for the SET integration. Among the other requirements of this process there is the thermal budget. The temperature of the different annealing steps that are performed are tuned depending on which stage the samples are in, since after Titanium nitride (TiN)

deposition temperatures above 400°C must be avoided in order to prevent crystallization on the gate electrode [64].

Regarding the FET fabrication, the standard CMOS technology available at IMB-CNM includes the generation of field oxide, p-well implantation and annealings above 1100°C. These processes are performed in 4" wafer compatible equipments. The well implantations that define the CMOS structure will be avoided, since just the n-type MOSFET is required; instead of a specifically generated field oxide, the buried oxide (BOX) of the SOI substrate will be use, with consequent variations in terms of interfacial oxide charges; and annealing processes must be tuned to temperatures below 900°C. In addition, reshaping from the wafers patterned at CEA-Leti is necessary. And therefore, specific pillar protection during wafer cleaving and FET fabrication must be developed.

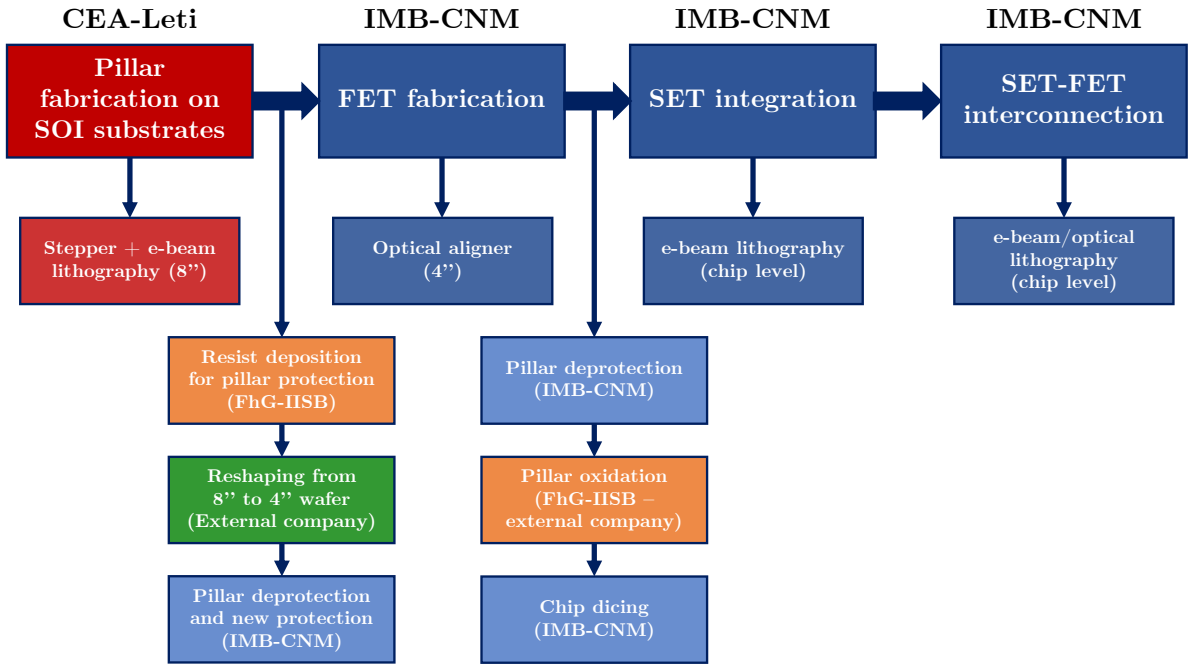


FIGURE 3.3: Process sequence for the complete SET-FET fabrication.

Thus, the parameters that define the optimum SET-FET process sequence are: the shape operability of each facility and equipment (8", 4" or chip level); the thermal budget (≤900°C); and the protection-deprotection methodology, which must ensure the pillar integrity during all processes. After pillar patterning and wafer reshaping, the first part of the FET is fabricated; once the SET integration is performed, the complete SET-FET interconnection takes place. Fig. 3.4 and 3.5 show in more detail the main steps of the complete process sequence and the implications for each of the SET or FET elements.

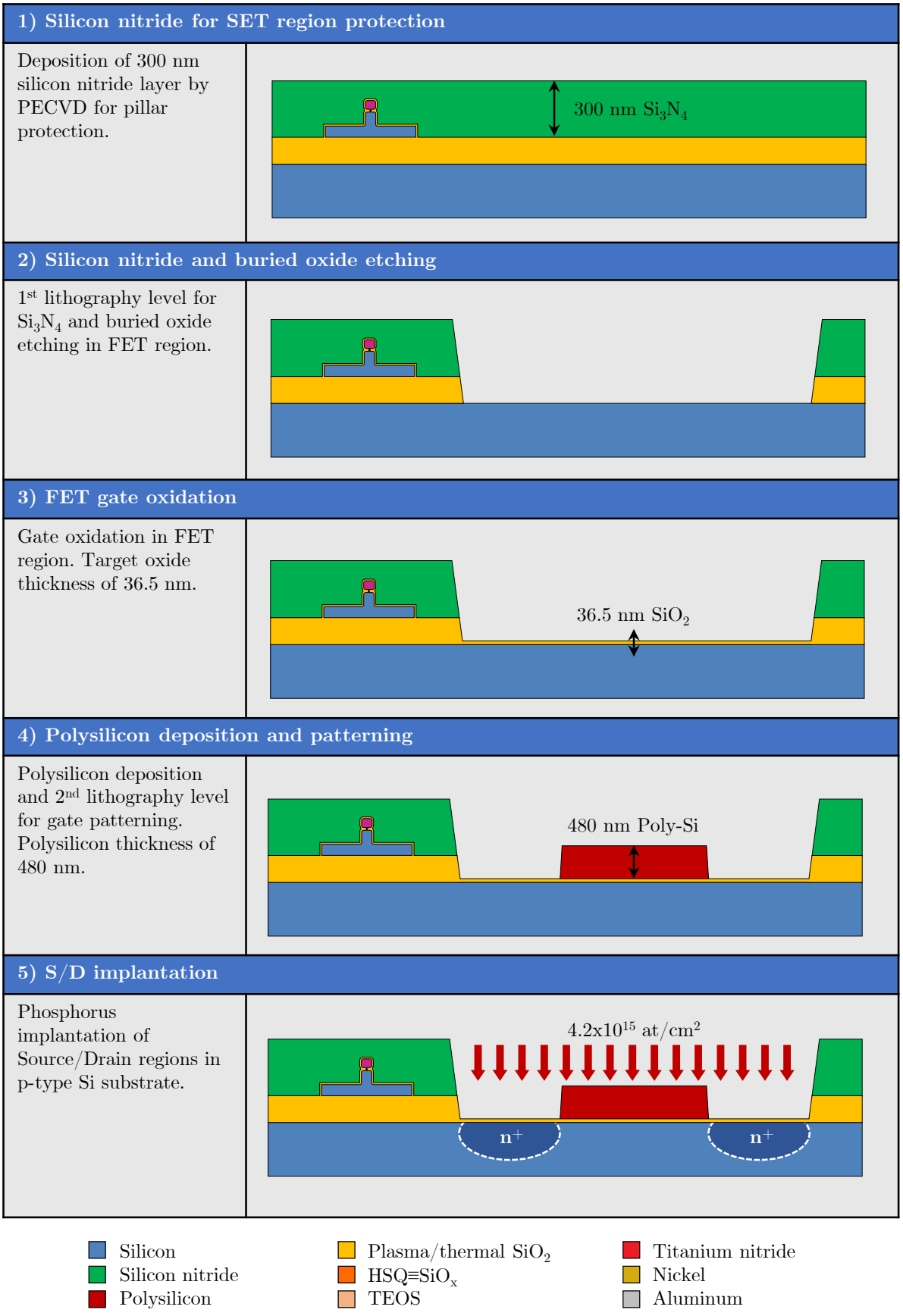


FIGURE 3.4: First part of the SET-FET overall integration process.

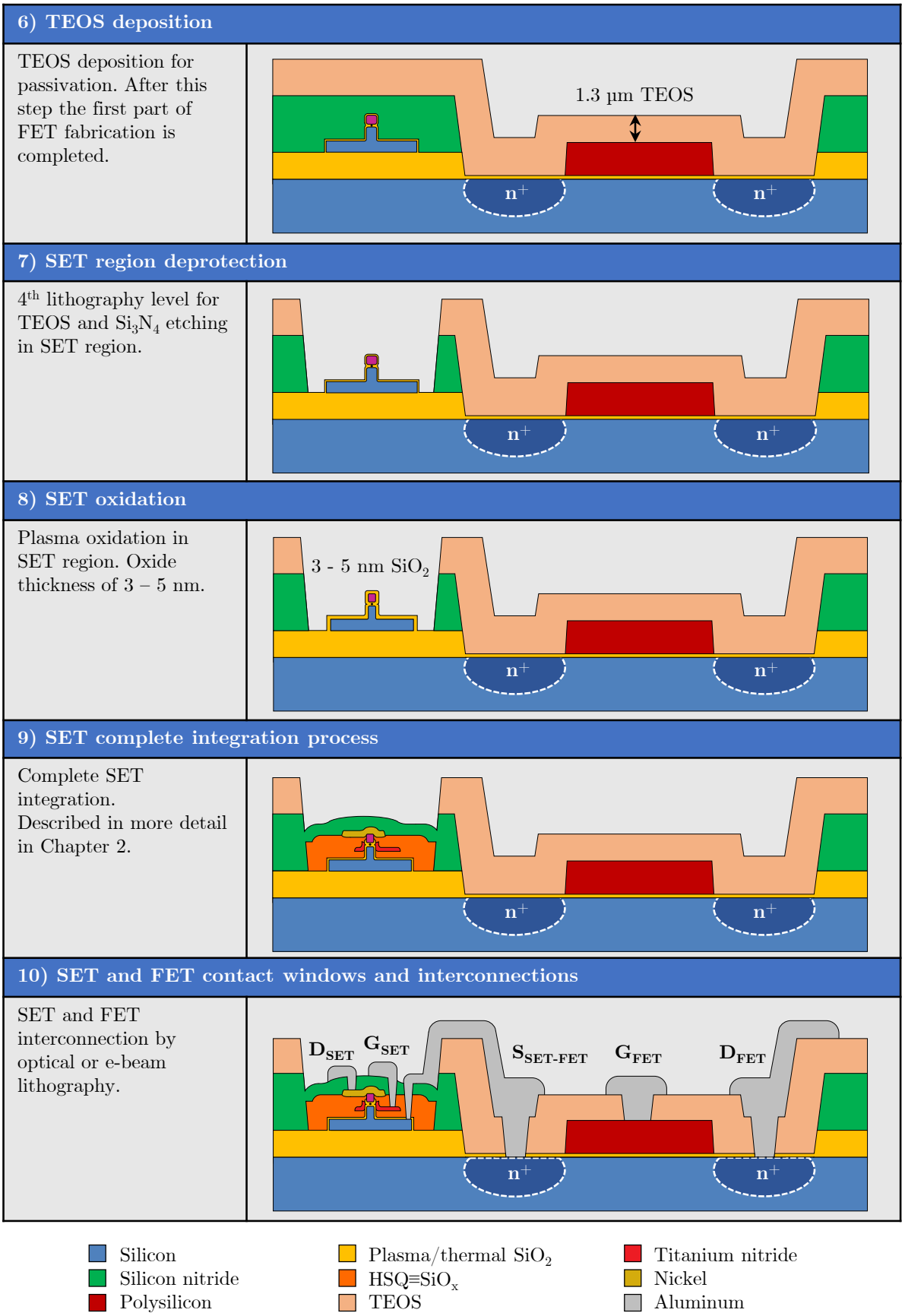


FIGURE 3.5: Second part of the SET-FET overall integration process.

3.2.2 Layout distribution

The first step is the pillar patterning on SOI substrates. Same layout that in the SET integration is used (Fig. 3.6): a pitch of 15 mm between chips and each chip with an inner region of 16 top-silicon islands. Each island has 5 pillars of different nominal dimensions (i.e. 50, 45, 40, 35 and 30 nm); these are the design dimensions, after silicon patterning and further oxidation thinner pillars are obtained.

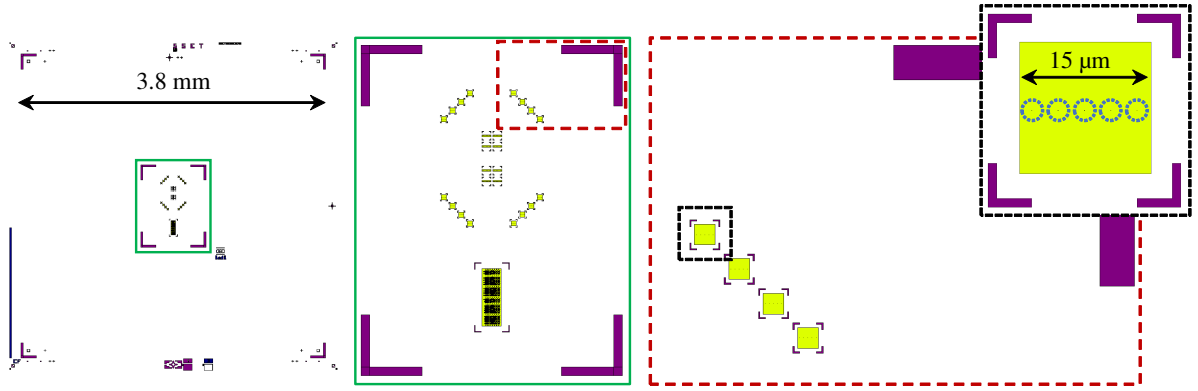


FIGURE 3.6: Initial lithography levels for the SET-FET integration.

After pillar and Si NDs fabrication, a thick resist is deposited in the 8" wafers; this is done at FhG-IISB. They are sent to MPE, Inc. [80] (Micro Precision Engineering), the external company in charge of their reshaping into 4" wafers. With the 4" wafers at IMB-CNM, the resist is removed and a 300 nm coating of silicon nitride (Si_3N_4) is deposited as pillar protection during the FET fabrication. The Si_3N_4 layer is locally etched in the first lithography level. As Fig. 3.7 shows, the FET is fabricated close to the top-silicon islands where the SET are to be integrated. The fabrication advances until passivation (steps 2 to 6 from Fig. 3.4 and 3.5).

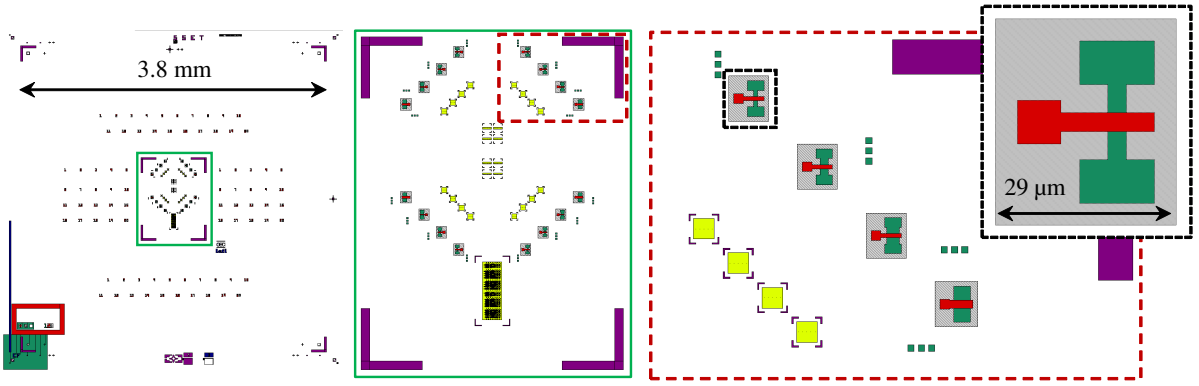


FIGURE 3.7: First three lithography levels related to the FET fabrication.

The next step after FET fabrication is the pillar deprotection to enable SET integration. Now it is required the etching of both passivation layer and the Si_3N_4 coating (step 7 from Fig. 3.5). Afterwards, the 4" wafers are sent again to FhG-IISB for their plasma oxidation at HQ-Dielectrics [59] (step 8 from Fig. 3.5) and sent back to IMB-CNM; there the wafers are cleaved into dices for the complete SET integration process (summarized in step 9 from Fig. 3.5).

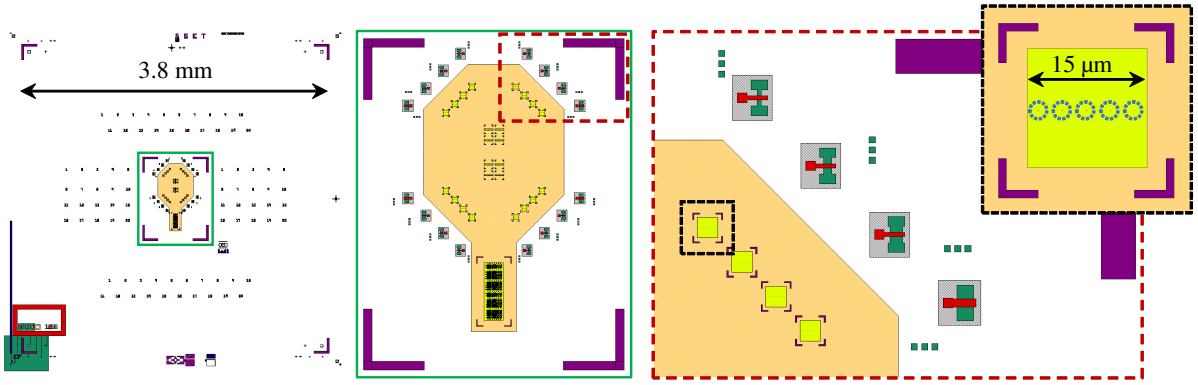


FIGURE 3.8: Fourth lithography level for the SET-FET integration; this level is related to the SET region opening.

The remaining processes to be carried out concern the contact windows opening and the metal routing for SET-FET interconnections, performed through photolithography and dry etching.

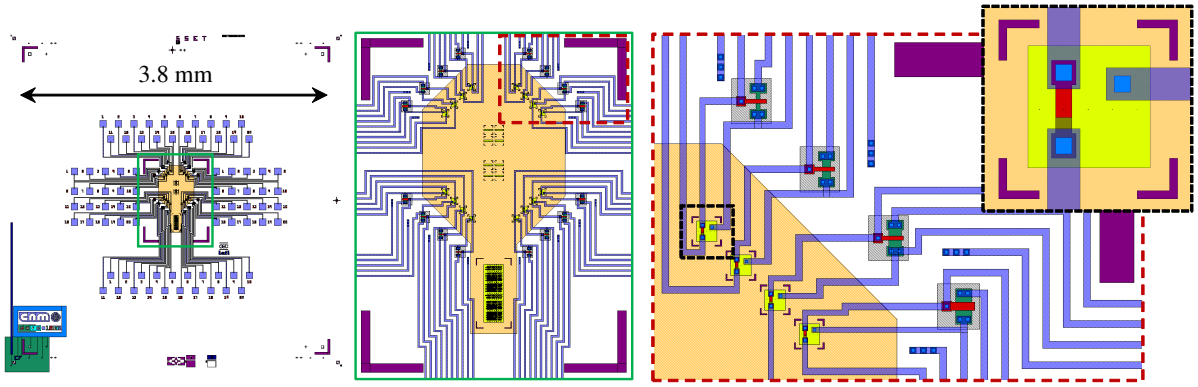


FIGURE 3.9: Fifth and sixth lithography levels for the SET-FET integration; these levels are related to the contact windows opening and the metal routing, respectively.

As previously mentioned, the SET-FET integration is preceded by the fabrication of standalone FETs, performed under specific conditions that can fulfil the described requisites. This results in an additional requirement for the layout design, since both FET and SET-FET operation must be simultaneously afforded. An approach based on different designs at wafer level is followed; it is described in more detail in next section.

3.2.3 Wafer distribution

The characteristics of the photolithography masks for the SET-FET integration are determined by some factors. First, they must be adapted to the pillar pattern layout used at CEA-Leti. Second, they must be usable for both fabrication runs, either the one whose target is the SET-FET hybrid circuit as the one aimed for the standalone FET device. And third, since the SET-FET interconnection is not trivial and might depend on the resulting status of both integrating elements, different routing conditions must be considered. In this section there are some further details about the masks designs that address their suitability for these issues.

The wafer reshaping and the 15 mm pitch of the SET layout limits the number of available chips in a 4" wafer. Moreover, the exclusion limit in the boundary of the wafer during photolithography processes reduces even more this number. There are two die positions that are aimed for the optical prealignment during the lithography step, and thus cannot be considered functional. In addition, 4 more positions contain a wide set of test structures which include capacitances, interdigitated capacitances and contacts for poly/metal characterization. In summary, as Fig. 3.10 depicts, there are a total of 15 functional dices per wafer; these dices are separated in three types of design for different aims.

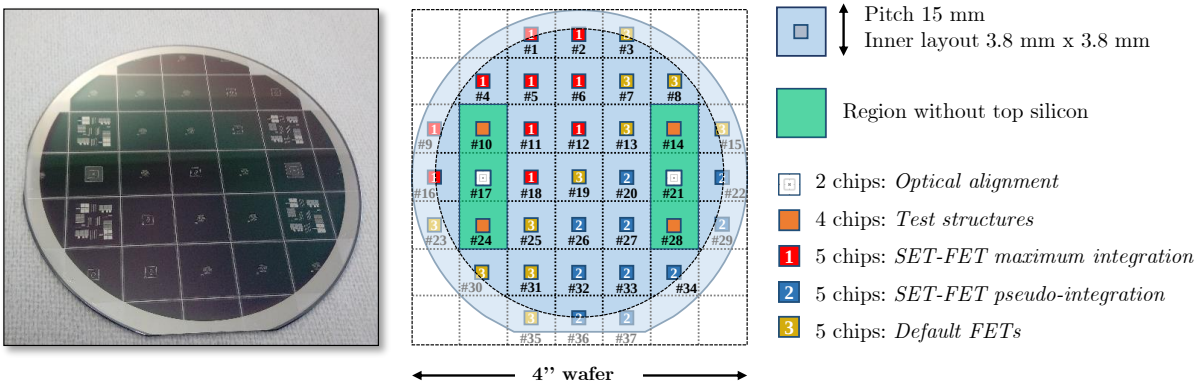


FIGURE 3.10: Wafer distribution for the SET-FET layout with detail of number of available chips for each design.

The first type of layout contemplates the SET-FET interconnection by photolithography. The design is described in Fig. 3.11, and connects the SET drain to the FET gate besides a common source contact. From the initial 80 isolated pillars available per chip, just one per top-silicon island can be contacted (i.e. 16 nanopillars); on the other hand, 16 FETs are fabricated in the same diamond configuration. Thereby, 16 pairs of SET-FET are targeted per chip. The contacted structure for the SET element is in all cases the nominal 45 nm pillar. Four types of FETs are fabricated with dimensions for WxL (μm x μm) of: 3x3, 6x3, 9x3 and 12x6.

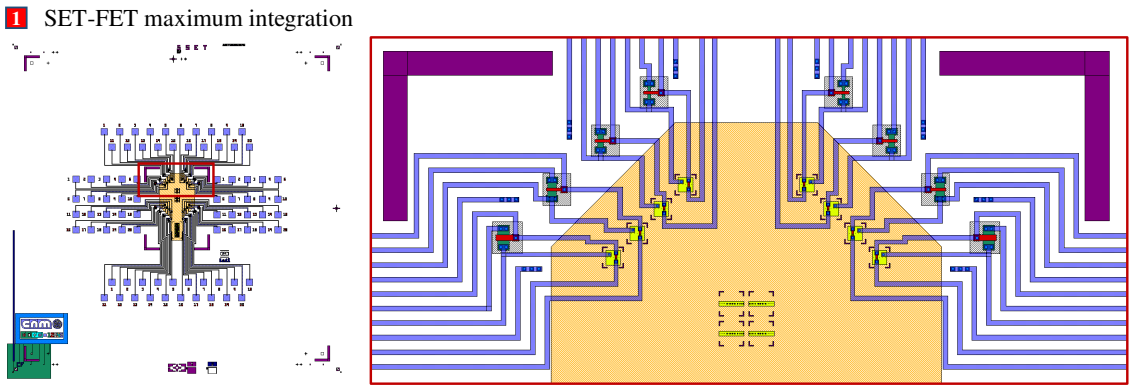


FIGURE 3.11: Layout design for SET-FET maximum integration.

The next type of configuration targets the SET-FET interconnection by e-beam lithography (Fig. 3.12). It follows a similar distribution than in the previous type: 16 FETs of different dimensions disposed close to the top-silicon islands where the SET are going to be fabricated. This design enables the further interconnection of the FET element with any of the contacted pillars, to be decided according to the process monitoring.

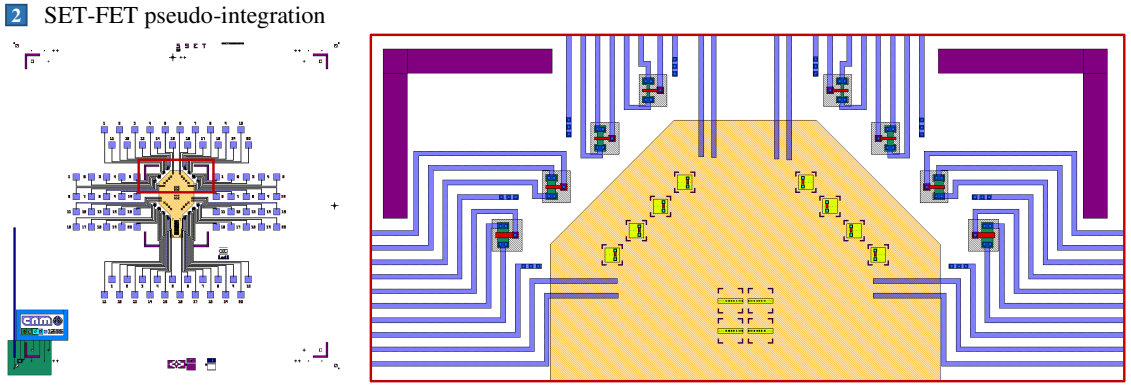


FIGURE 3.12: Layout design for SET-FET pseudo-integration.

And finally, a specific type of layout whose target is not the SET-FET interconnection is presented in Fig. 3.13. The main goal of this design is to enable the FET characterization on the specific SOI substrates for each of the wafers. In this case, four arrays of transistors of a wider interval of dimensions (WxL from 2.5 μm x 3 μm to 40 μm x 40 μm) are arranged, with common source and gate contact but individual drain electrode. In the inner area four isolated FETs are fabricated as well, near the SET region, in order to enable the SET-FET interconnection by wire bonding if necessary.

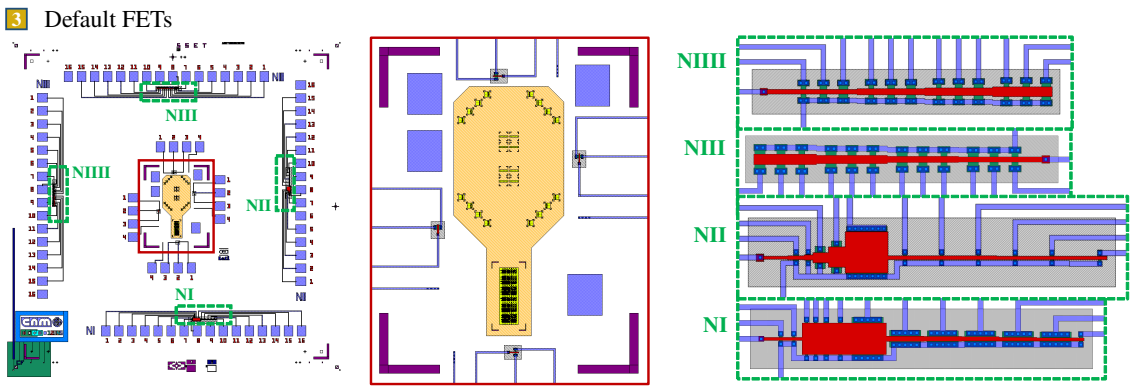


FIGURE 3.13: Layout design for default FETs fabrication.

In summary, a photolithography mask formed by six levels is presented. This design is in agreement with the characteristics of the layout used for pillar and SOI top-silicon patterning, and contemplates different routing possibilities for the final interconnected device.

3.3 SET-FET hybrid circuit modelling

3.3.1 SET implementation into FET circuit

As mentioned before, the SET main drawbacks in terms of low drive current are expected to be overcome by its combination with a FET. Here, in order to simulate the hybrid SET-FET circuit two different device electrical models are used. One specifically developed in the framework of the IONS4SET project for the SET device [81], which simulates the SET operation in a vertical topology and enables the ND location and size modification. Nominally, ND is considered to have a size of 3 nm and a fixed position in the very center of the embedded oxide layer. Concerning the FET element, a HSPICE device model based on the CMOS available at IMB-CNM is used.

Transient simulations have been performed to evaluate the effect of parasitic capacitances and the optimum dimensions for the FET element. According to the simulation results summarized in Fig. 3.14, parasitic capacitance and resistance do not conceal the observation of Coulomb blockade oscillations: in region 2 a constant V_G and I_{BIAS} are applied, with no Coulomb blockade oscillations; meanwhile, in region 1 the V_G is swept and a constant I_{BIAS} is applied, and at this region the characteristic Coulomb blockade oscillations are observed, as expected for the hybrid SET-FET circuit.

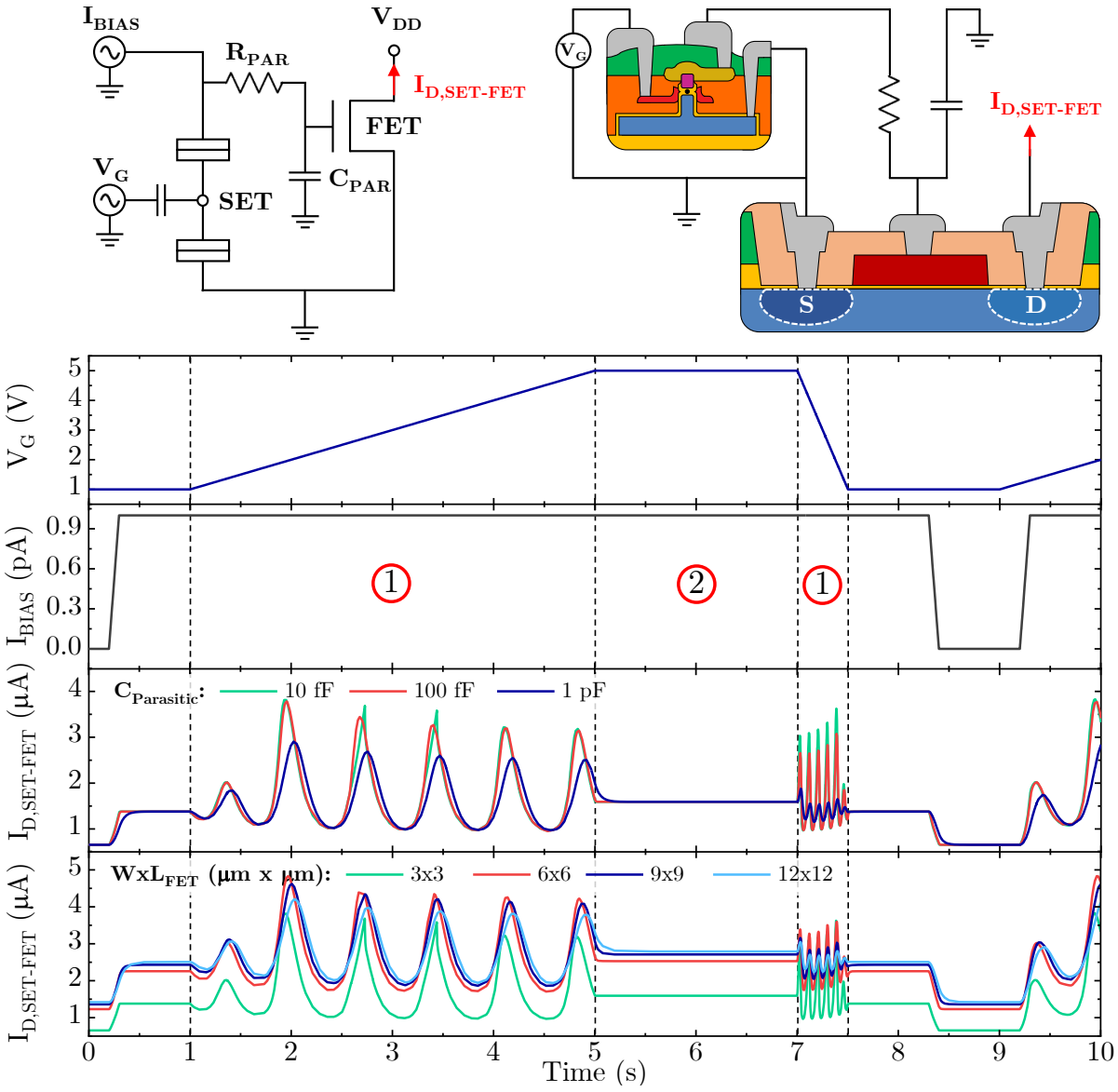


FIGURE 3.14: Hybrid SET-FET circuit and resulting simulations for different values of the parasitic elements at different regimes and conditions.

Additional resistance and capacitance introduced by the interconnections have been taken into account; to study the relevance of parasitic components in the circuit, their behaviour in dynamic mode is analysed. There is not a significant impact on the output current ($I_{D,SET-FET}$); it is noted that for parasitic capacitances up to 1 pF the hybrid SET-FET circuit would still work properly. It can also be deduced that FET dimensions in the range of few microns are adequate. Moreover, the simulations show a convenient amplification of the SET signal up to 4 μA at the drain of the FET element.

3.3.2 FET process simulation and V_{Th} adjustment

For the SET-FET to work properly, the FET element must have a threshold voltage low enough to be able to operate at subthreshold level. Thus, a V_{Th} in the order of 200−300 mV is required. As this value is well below the measured threshold voltage for the standard FET used as reference, some conditions in the fabrication process have to be modified. The standard CMOS technology used for the FET device includes an additional implantation step after gate oxidation. It consists in a boron implantation in a p-type substrate that allows the adjustment of threshold voltage by dopants activation. To find the dopant profile for which an optimum V_{Th} is obtained, Sentaurus TCAD process simulation [82] is used. Fig. 3.15 introduces the studied device, adapted from the reference FET.

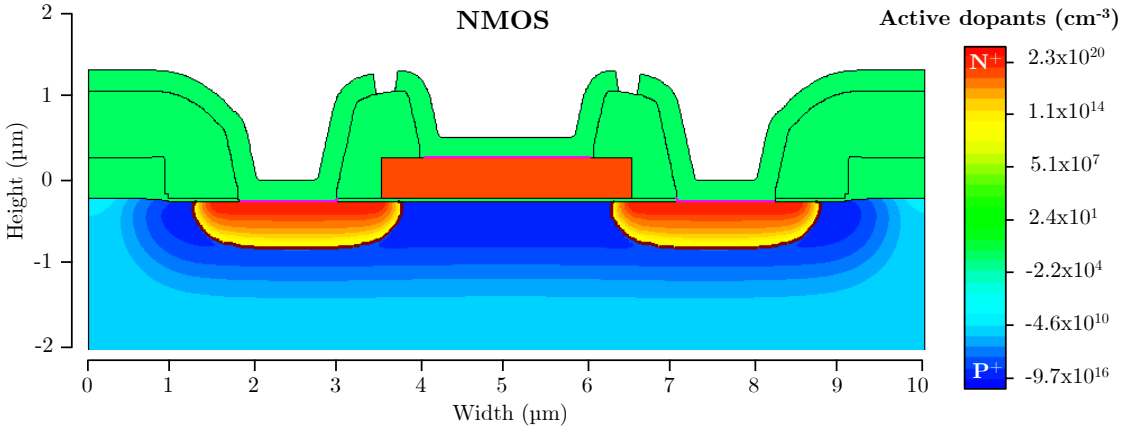


FIGURE 3.15: NMOS model for process simulations about implantation for V_{Th} adjustment.

The strategy to model the FET to be fabricated is as follows. First, the NMOS of a complete CMOS process is simulated according to its standard conditions (i.e. including the field oxidation, the n-well and p-well implantation and the rest of processes at nominal conditions). The result is compared with the electrical behaviour of the model with the nominal parameters of a CMOS. At this point, the interfacial oxide charge traps are adjusted by comparing experimental and simulated values for V_{Th}, calibrating the simulations. Finally, the NMOS device is simulated now without all the CMOS-related process steps.

As mentioned, the main parameter to be adjusted is threshold voltage. It is dependent on various parameters and conditions, as substrate doping, oxide thickness and quality, substrate bias or short channel effects. Analytically, V_{Th} is defined as the intersection in V_G of the tangent of I_D current at the transconductance peak position, as Fig. 3.16.a graphically describes.

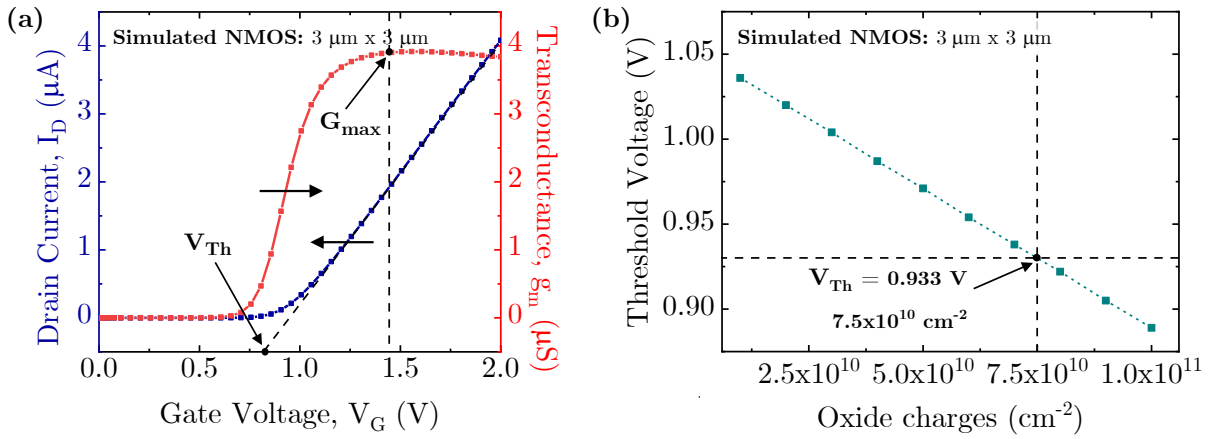


FIGURE 3.16: Example of $I_D - V_G$ (a) and V_{Th} as function of oxide charges (b).

In the reference NMOS model, interfacial charge traps are present between Si−SiO_2. Fig. 3.16.b shows the resulting V_{Th} as a function of oxide charge density. From experimental measurements, a reference value of $V_{Th} = 0.933$ mV is given for the standard CMOS. This corresponds to an oxide charge density of 7.5x10^{10} cm^{-2}.

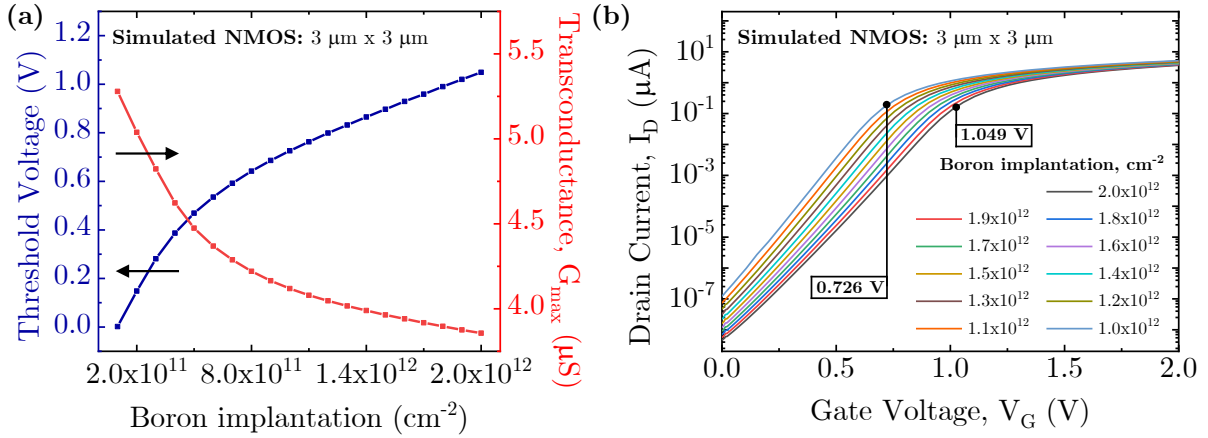


FIGURE 3.17: V_{Th} and g_m (b) and $I_D - V_G$ (a) for a certain interval of implantation values.

Now the simulations are focused again in the modified NMOS, this time without well implantation and with a fixed value of oxide charges. Channel length and width are 3 μm, and a drain bias of 50 mV is applied. A wide interval of implantation is explored, but as Fig. 3.17 shows, only by using very low values (below 3.0x10^{11} cm^{-2}) a threshold voltage below 0.3 V can be obtained.

3.4 Preliminary compatibility tests

In order to ensure the integrity of patterned pillars and Si NDs during the complete process sequence, several preliminary investigations had to be carried out. First, to secure that neither the resist for the wafer reshaping nor the Si_3N_4 protection for FET fabrication or their deprotection compromise the SET integration. Second, to verify that the maximum temperature of 900°C is adjusted to the thermal budget. And third, to find in which stage the pillar plasma oxidation results most convenient. The main process to monitor and validate the conditions is TEM structural analysis, performed in all cases at HZDR. These investigations are developed in parallel to the adjustment of two of the CMOS processes that must be performed at low temperature: polysilicon doping and gate oxidation.

3.4.1 Resist protection for wafer reshape

In a 8" SOI substrate wafer with pillars distributed in the already mentioned configuration (Fig. 3.6), a thick coating of photoresist is sprayed as protection for wafer reshaping. An adhesion promoter based on hexamethyldisilazane (HMDS) is applied; then a 6 μm thick layer of AZ 4999 resist is sprayed in a homogeneous and conformal coating. Following deposition, a soft bake at 110°C for 5 min on a hot plate is performed. Once the reshaping from 8" into a 4" wafers is done, from the remaining rings a few dices are used for testing the resist removal. The protective resist is thus removed by immersion in acetone and Isopropyl alcohol (IPA), 5 min each. Fig. 3.18.a shows the top view of the resulting status, where all five pillars are clearly visible with no apparent damage or resist residues around.

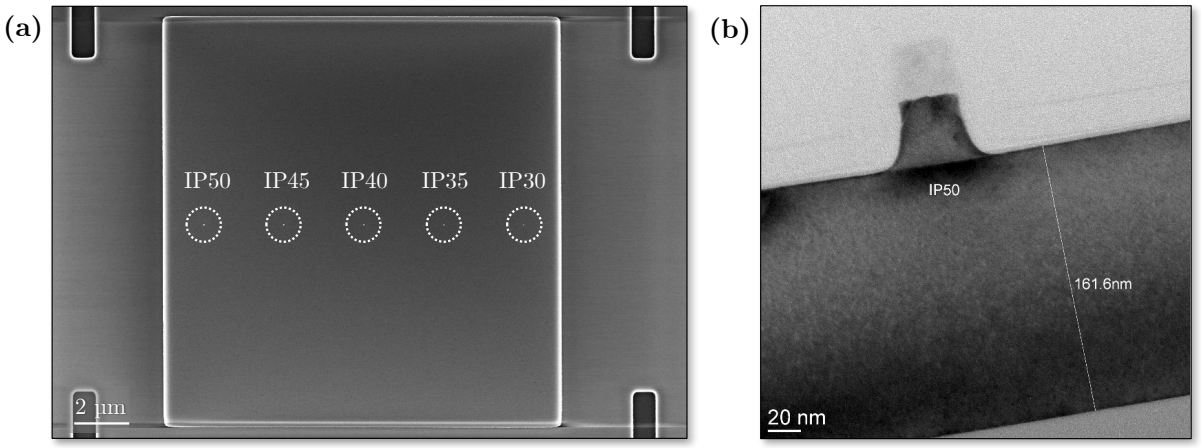


FIGURE 3.18: SEM top view of five pillars in a SOI island (a) and TEM cross section of one pillar with detail of top silicon thickness (b) after protective resist removal.

The TEM lamella is performed by means of FIB preparation using in situ electron and ion beam deposition. Fig. 3.18.b shows the largest isolated pillar on top of the top-silicon layer, with a thickness of 160 nm.

Fig. 3.19 presents the five pillars from the same top-silicon island. Several conclusions can be extracted. For instance, no pillar damage can be observed in any of the isolated positions. Besides, there is not significant difference in height for pillars of different diameter. The whole pillar is covered with a 2.4−3.4 nm thick layer of native oxide. Another relevant evidence is the presence of Si NDs in the embedded oxide; this phenomena is clearly visible in all pillars except the IP30, in which the oxide is too thin for Si ND formation. In terms of pillar diameter dimensions, the smallest one (IP30) shows a diameter of 15.6 nm, while the next one (IP35) is 21 nm wide; this observation proves the need of a sacrificial oxidation for pillar shrinkage in order to move towards the targeted sub-10 nm single electron device.

These results verify the resist protection, wafer reshaping and deprotection step as valid for the process sequence, since the integrity of isolated pillars and Si NDs is not affected.

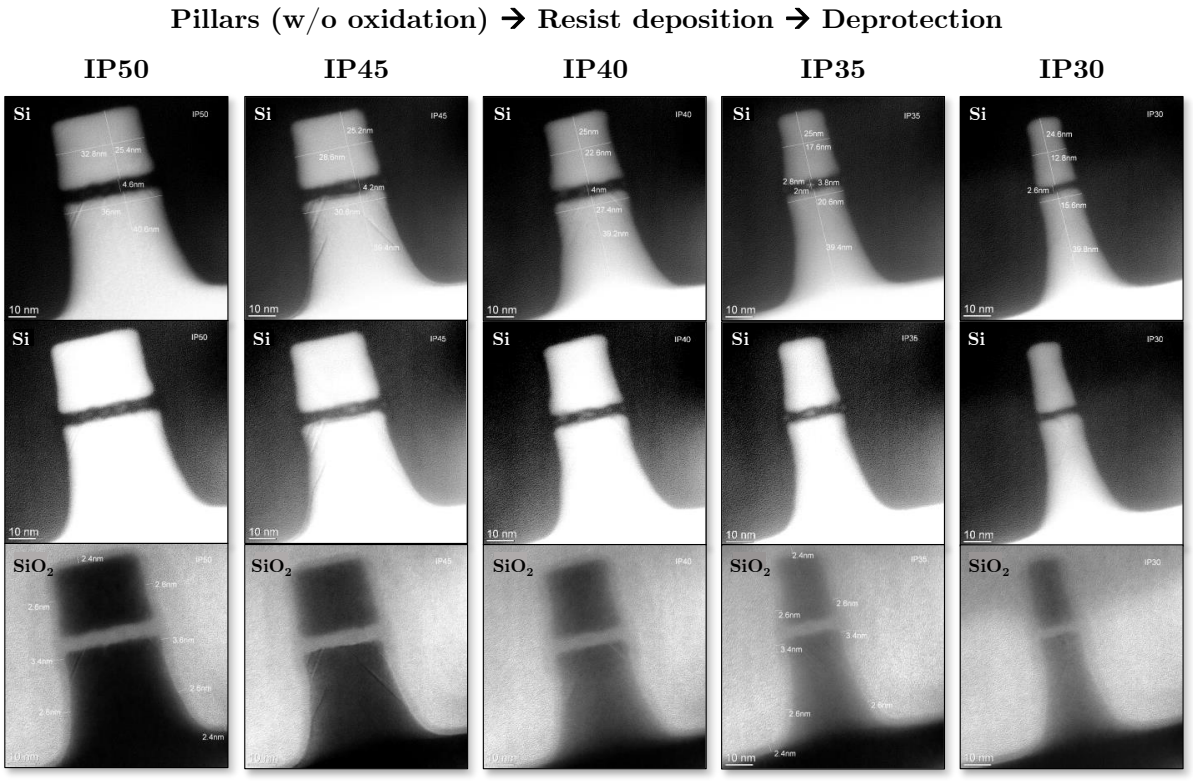


FIGURE 3.19: EFTEM Si and SiO_2 plasmon loss images of five pillars after resist deprotection.

3.4.2 Pillar protection during FET fabrication

A significant concern is the pillar protection during the FET fabrication. The requirements for such protection are: well known processes for deposition and etching; a safe deprotection procedure for maintaining the pillars integrity; and, to a lesser extent, an insulating and chemical barrier layer. The selected protection layer is 300 nm thick Si_3N_4 deposited by PECVD, which can be removed by immersion in phosphoric acid (H_3PO_4) for 15 min. From the TEM analysis presented in Fig. 3.20, Si NDs are visible in the embedded oxide and no apparent damage on any of the pillars is caused after the full protection/deprotection sequence.

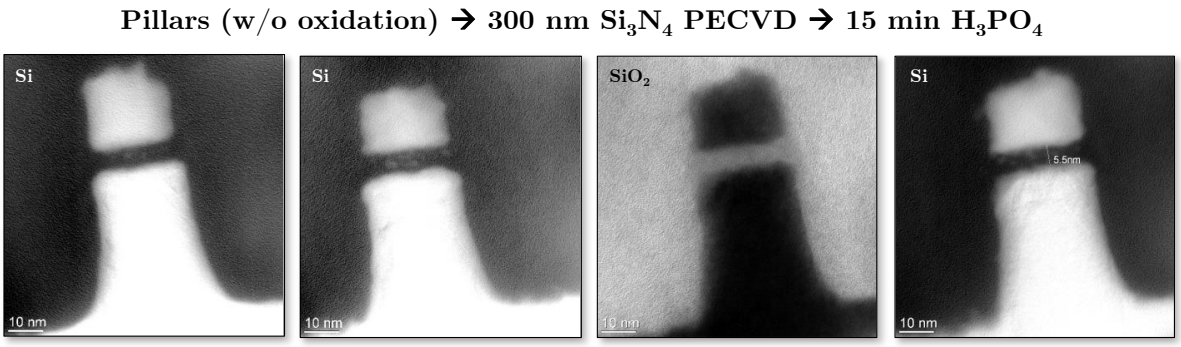


FIGURE 3.20: EFTEM plasmon loss images of pillars after Si_3N_4 deposition and etching.

3.4.3 Thermal budget

FET manufacturing requires process steps that include various annealing procedures. Here, it is analysed if a thermal budget of 900°C for 2h influences the pillar integrity, including Si ND stability. Fig. 3.21 shows that Si NDs are not affected, no pillar damage is observed and there is only a thin native oxide around the pillars.

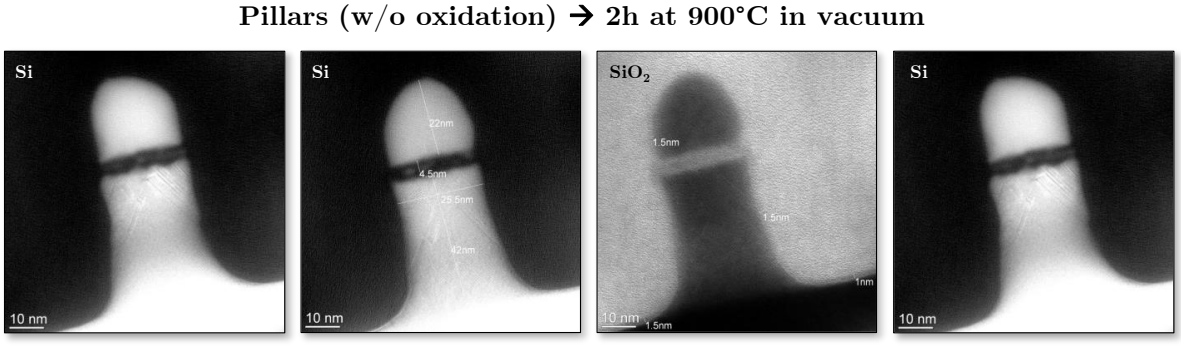


FIGURE 3.21: EFTEM plasmon loss images of pillars after 2h at 900°C in vacuum.

3.4.4 Plasma oxidation relevance

The objective of plasma oxidation is to reduce the pillar dimension by oxidizing the silicon, and to form the gate oxide. By doing so, smallest pillar diameter is expected to become sub-10 nm. Here, the relevance of performing this oxidation before or after FET fabrication is discussed, justifying the process path depicted in Fig. 3.3. If the sequence is Si_3N_4 deposition, annealing (as simulation for the FET fabrication) and Si_3N_4 removal, then an oxide bulge is formed all around the embedded oxide, as Fig. 3.22 shows.

Pillars (w/o oxidation) → 300 nm Si_3N_4 PECVD → 2h at 850°C N_2 → 45 min H_3PO_4

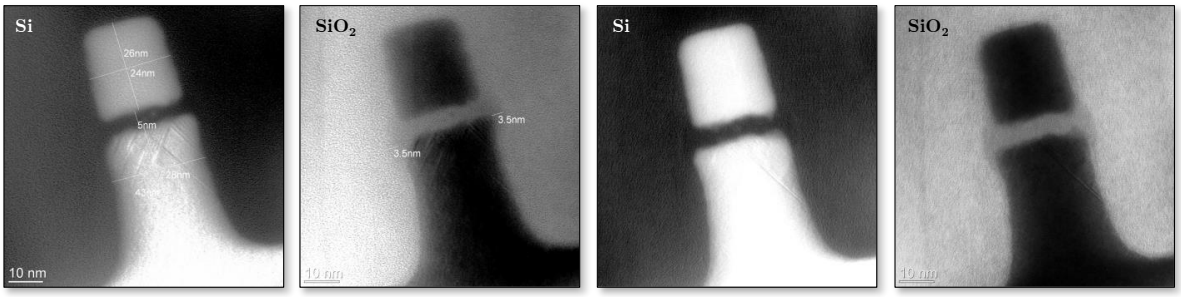


FIGURE 3.22: EFTEM plasmon loss images after Si_3N_4 deposition, annealing and deprotection.

Nevertheless, as Fig. 3.23 shows, if there is an initial thin oxide around the pillar this oxide bulge formation is strongly minimized. In this case the initial oxide thickness is in the same range of values than the native oxide present in the pillars from the SOI wafers (Fig. 3.19). This leads to the conclusion that performing the FET fabrication with a thin oxide layer around the pillars can prevent from any bulge formation, while the posterior SET oxidation can maintain its pillar size shrinkage function.

Pillars (w/ oxidation) → 300 nm Si_3N_4 PECVD → 2h at 900°C O_2 → 45 min H_3PO_4

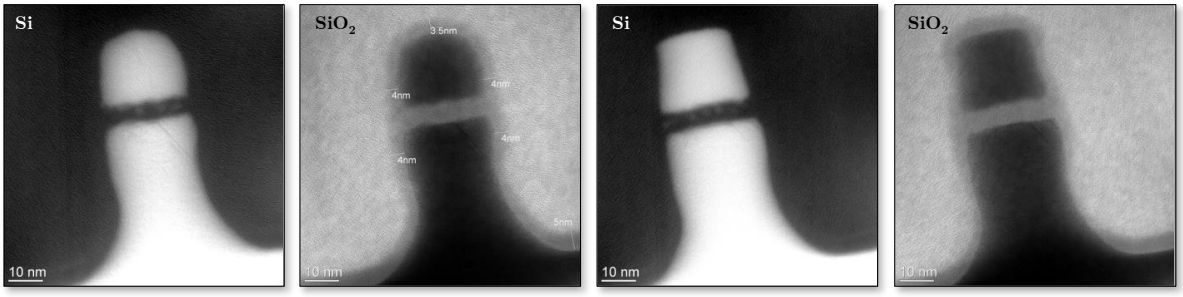


FIGURE 3.23: EFTEM plasmon loss images after oxidation, Si_3N_4 deposition, annealing and deprotection.

3.4.5 Polysilicon doping at low temperature

As already mentioned, all processes related to the FET fabrication which require temperatures above 900°C must be adapted towards the SET-FET integration. Thus, one of the steps that requires high temperature is the polysilicon doping; for the CMOS fabrication, it is performed by means of Phosphoryl chloride ($POCl_3$) diffusion, which usually requires temperatures near 950°C. In order to provide a balance of possible alternatives, here resistivity measurements are presented for both diffusion and implantation methods for an interval of temperatures from 800°C to 900°C.

In four 4" wafers a 100 nm SiO_2 and 480 nm polysilicon layers are deposited. In three of the wafers a $POCl_3$ diffusion is performed at different temperatures (800°C, 850°C and 900°C). In the fourth wafer an ion implantation and posterior dopants activation is done (at 850°C).

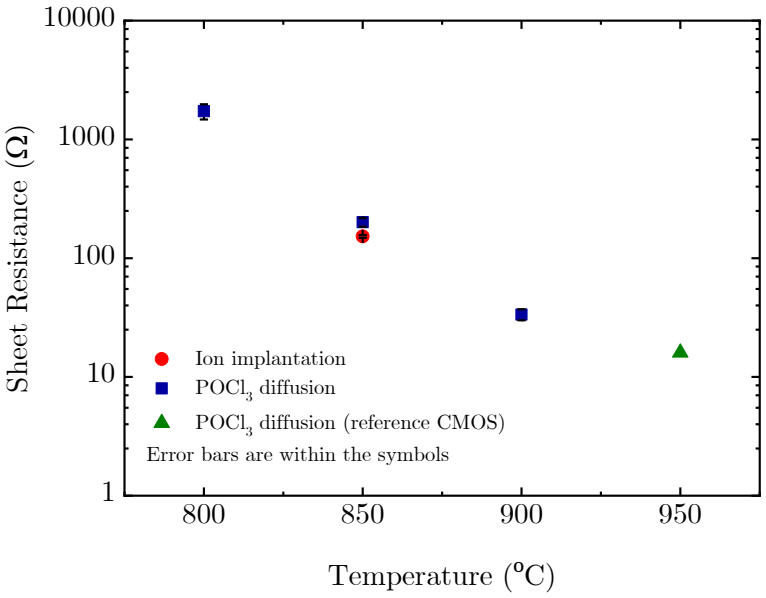


FIGURE 3.24: Electrical sheet resistance measurements after $POCl_3$ diffusion and ion implantation for temperatures from 800°C to 900°C.

Fig. 3.24 shows the sheet resistance of each wafer after processing, together with the reference value of the standard CMOS fabrication. It is clear that temperature reduction during diffusion leads to a more resistive behaviour for silicon substrates. It is deduced as well that there is no difference between ion implantation and $POCl_3$ diffusion at same temperatures. For these reasons, diffusion at 850°C is considered to be a suitable process in terms of resistance and thermal budget fitting.

3.4.6 Oxidation at low temperature

Another process which requires of optimization with respect its standard conditions is gate oxide formation. In the fabrication of the reference CMOS, temperatures near 950°C are used for the formation of a 36.5 nm gate oxide. In this case, the preliminary test consists in a set of oxidations performed at 900°C and at several times. Two different furnaces are used in parallel for these tests, named T2 and T7. The main difference is the level of contaminant acceptance for each one; while the one to be used both for the standalone FET and SET-FET fabrication is the T7, still T2 can be used as a reference. It is done at 4" wafer level, with ellipsometry measurements of 49 points across the wafer of the resulting oxide thickness in each case.

A well established model for one-dimensional thermal oxide growth is the Deal-Grove model [83], [84]. From the experimental values obtained, Deal-Grove parameters can be deduced, enabling thus an accurate prediction for oxide growth from the model fitting [85].

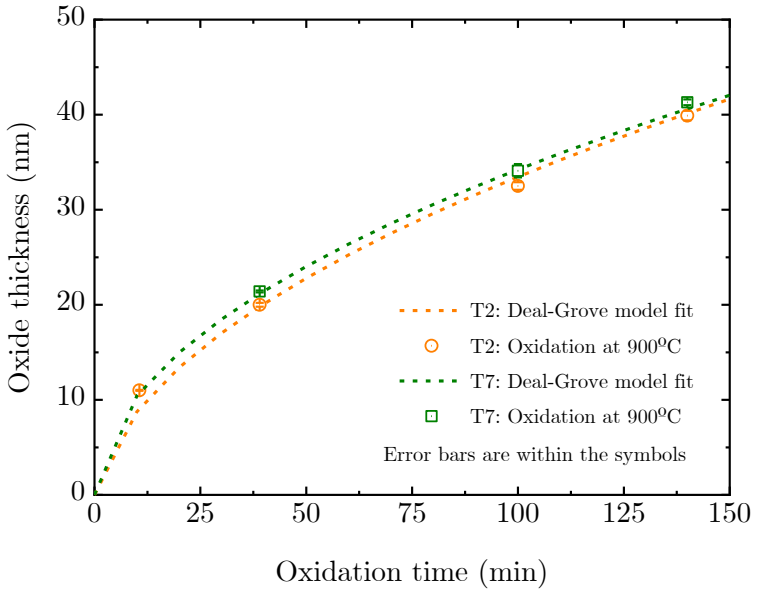


FIGURE 3.25: Measured oxide thickness after several time tests at 900°C; theoretical fitting of Deal-Grove model included for each of the thermal process equipments.

Fig. 3.25 describes the resulting experimental measurements and their corresponding theoretical prediction. It is deduced that the required oxidation time in order to obtain an oxide thickness of 36.5 nm at 900°C is 114 min in the thermal process equipment T7. These parameters are implemented in the conditions for the FET fabrication.

3.5 Standalone FET fabrication

Four p-type silicon wafers with resistivity values of 4 - 40 $\Omega \cdot$ cm are incorporated in the fabrication run. The first step is an oxidation of 440 nm performed at 1050°C; note that this temperature does not represent a problem, since in the actual SET-FET run the oxide used for well definition will be the BOX of the SOI substrate. Then a standard photolithography process is performed (i.e. a 1.2 μm thick 6512 resist is deposited and baked at 200°C for 30 min) with the first mask level of the design described in Fig. 3.7. It is followed by the dry etching of the SiO_2 layer and posterior resist stripping.

The 36.5 nm gate oxide is fabricated according to the conditions defined in the preliminary investigations of section 3.4.6. That is, an oxidation at 900°C for 114 min; ellipsometry measurements verify a thickness of 36.2 $\pm$ 0.5 nm. An additional aim for the standalone FET fabrication is the study of threshold voltage adjustment by ionic implantation after gate oxidation. In order to analyse its relevance, it is decided to perform this step in two of the four processed wafers and at standard conditions: boron implantation at 50 keV and 1.7 x 10^{12} at $\cdot$ cm^{-2}.

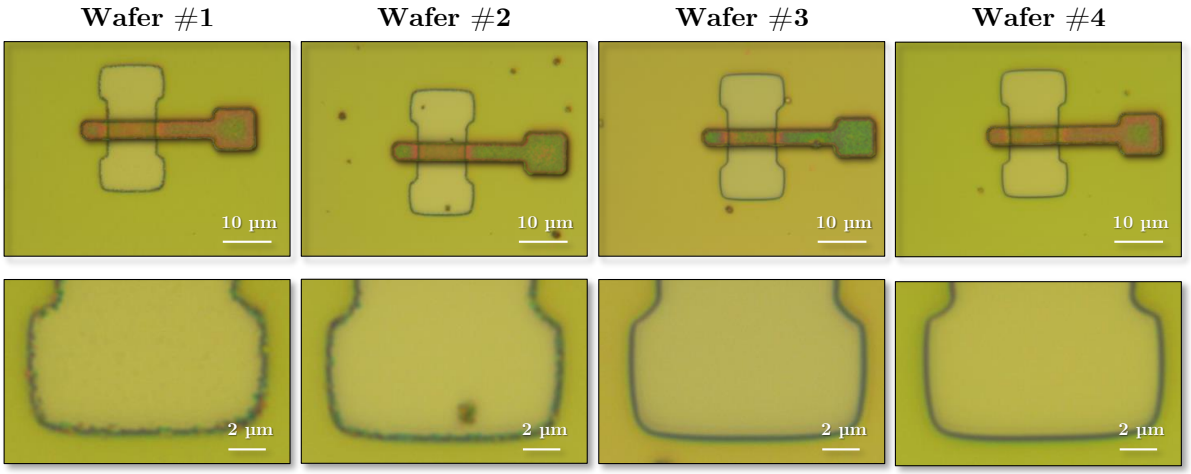


FIGURE 3.26: Example of one FET region (WxL of 9 μm x 3 μm) for each wafer after dry etching for polysilicon patterning.

Then a 480 nm thick polysilicon layer is deposited by LPCVD at 630°C. Afterwards, it is doped by $POCl_3$ diffusion at 850°C, again in agreement with the preliminary tests developed in section 3.4.5. This $POCl_3$ diffusion is done in an environment of 4000 sccm N_2, 600 sccm O_2 and 500 sccm $POCl_3$. Polysilicon is then patterned by another photolithography step followed by RIE, defining in that way the gate region.

At this point of the process, there is an unexpected difference in the etch-rate of the polysilicon layer. This explains the presence of polysilicon residues on the surface and on the spacers at the oxide edges, visible in wafer #1 and #2 from Fig. 3.26. An additional short overetching does not resolve significantly enough any of those aspects. Thus, in order to address both issues, an isotropic wet etching is done for 20s. As consequence, the polysilicon residues are removed (Fig. 3.27), but there are two additional drawbacks. First, it is measured by ellipsometry a relevant reduction on the gate oxide, as the nominal 36.5 nm thickness is reduced down to 12.0 nm and 14.6 nm for wafer #1 and #2, respectively. And second, by optical inspection it is observed a lateral etching of the polysilicon gate structure visible below the mask. For these reasons the wet anisotropic etching is not performed in wafer #3 and #4, where the oxide edges are not affected by the agglomeration of polysilicon residues.

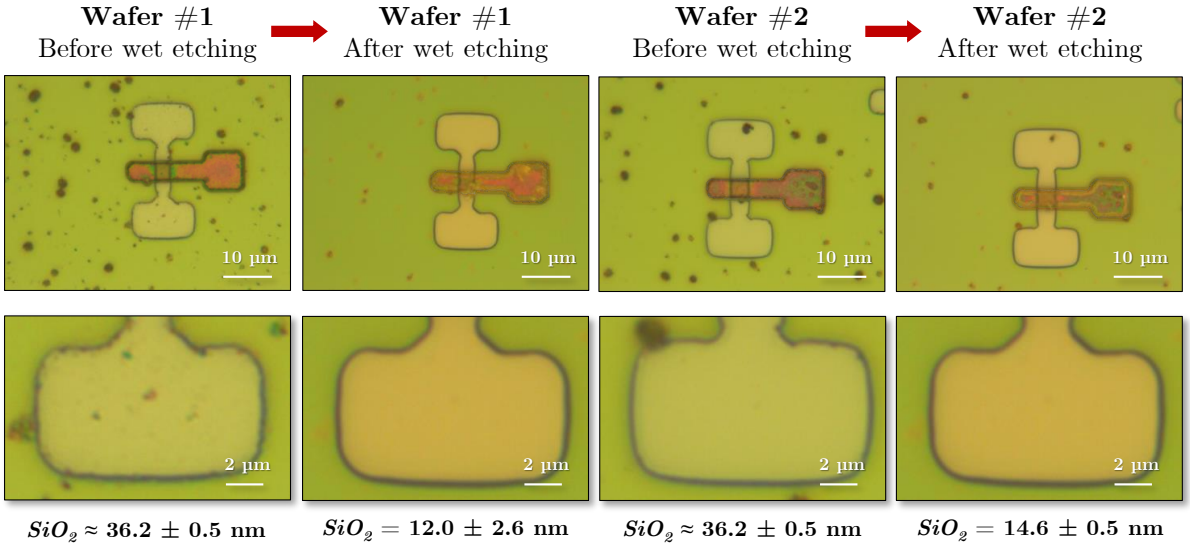


FIGURE 3.27: Example of one FET region (WxL of 3 μm x 3 μm) for wafer #1 and #2 before and after wet etching for polysilicon residues removal.

After polysilicon patterning a third lithography process takes place. In this case it is followed by a phosphorus implantation at 100 keV and 4.2 x 10^{15} at $\cdot$ cm^{-2} for Source/Drain regions activation.

In this point of the process it results convenient to check the actual channel width and length of the devices. As Fig. 3.28 indicates, similar dispersion is observed for the channel width of all transistors, independently of dimensions or position along the wafer. However, regarding the channel length, those wafers in which the additional polysilicon wet etching was performed present significant shorter channel lengths in the peripheral chips.

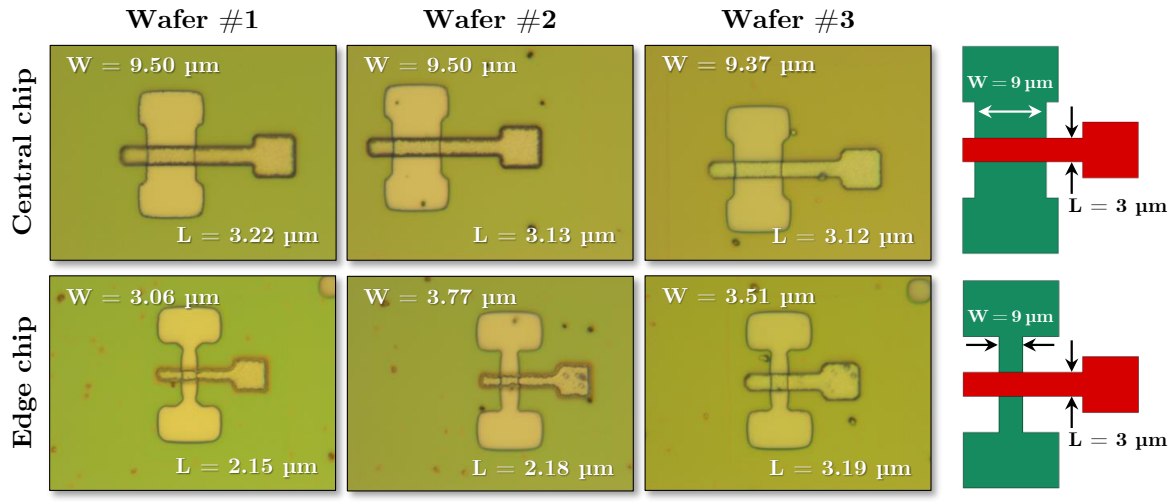


FIGURE 3.28: Comparison of two FET regions from different wafer location, with detail of measured channel length and width and nominal dimensions.

The next step is the deposition of a 1.3 μm thick Tetraethyl orthosilicate (TEOS) layer for passivation, followed by fluidification at 850°C for 30 min which serves as implants activation.

Through another lithography level the TEOS layer is locally etched by RIE, opening the contact windows. In this case, a slight overetch is aimed in order to ensure the complete material etching. Fig. 3.29.a shows an optical image of an example of FET in this step, and Fig. 3.29.b and Fig. 3.29.c the corresponding SEM top and tilted view of one of the contact windows. Since ellipsometry measurements are not reliable in features of such dimensions, top and bottom surface aspect and lateral etching analysis is the only way to verify the completion of the process.

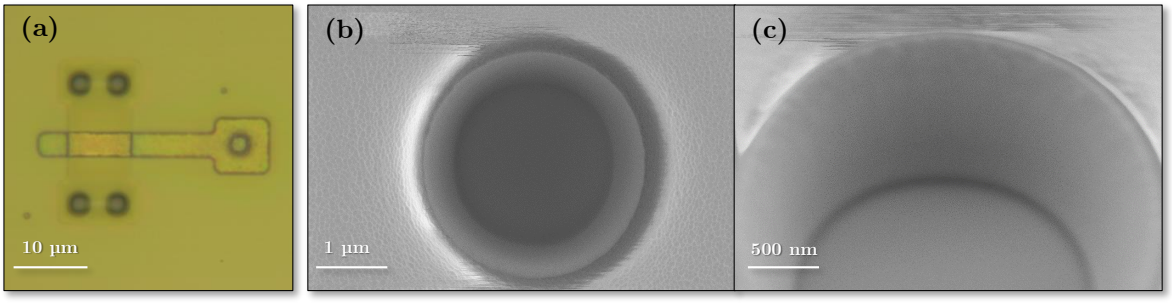


FIGURE 3.29: Optical image of one FET after contact windows opening (a); SEM images for the contact window in top view (b) and tilted section (c).

Finally, a 1.0 μm thick layer of Al:Cu is deposited by sputtering. A fifth lithography mask is used to pattern the metal layer by dry etching, achieving in that way the designed metal routing. Last process is an aluminium annealing at 350°C. Fig. 3.30 shows an example of each layout design after metal patterning; note that, as in this case no pillar patterning has been previously done and thus the SET integration is avoided, all designs are actual standalone FETs of different dimensions.

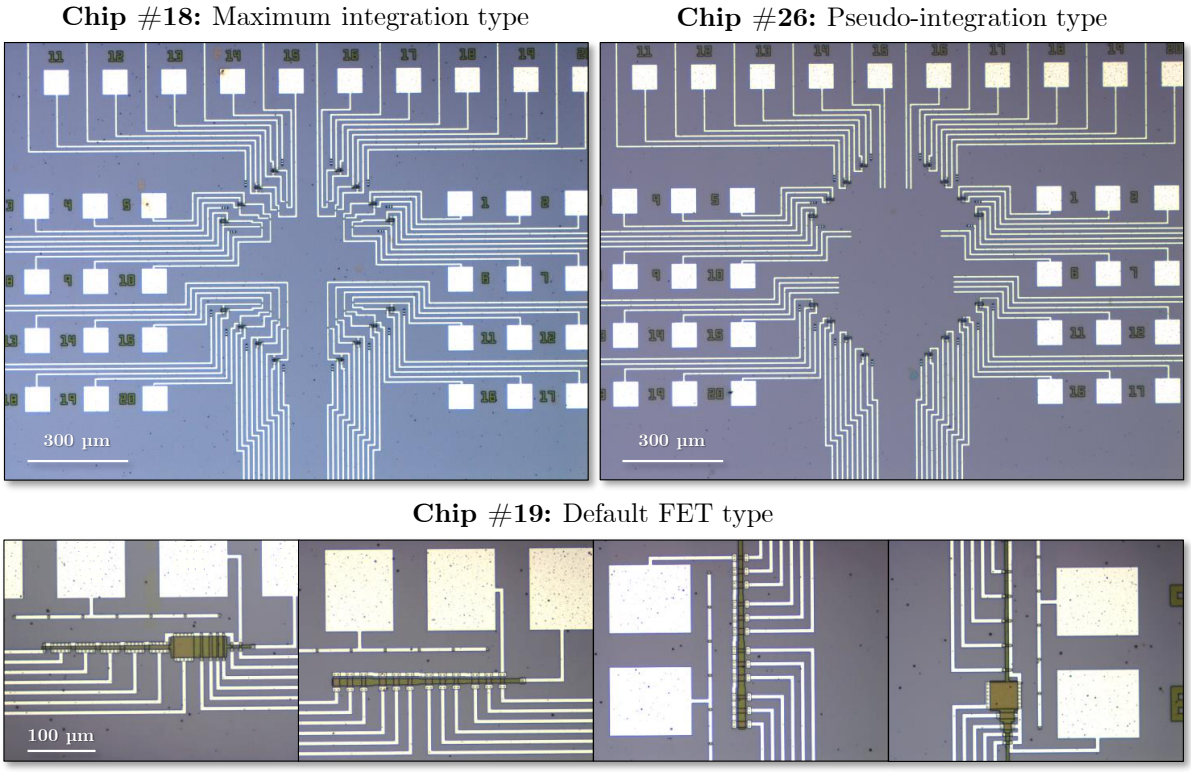


FIGURE 3.30: Optical images of one example of each of the designs after metal routing: maximum-integration, pseudo-integration and default FETs.

3.6 Summary of FET electrical characterization

After FET fabrication at specific predefined conditions, electrical characterization is necessary in order to validate the proper device performance. In this section, several of the aspects about the electrical characterization of the standalone FET are summarized. More details about the complete analysis are presented in Appendix E, but as a general overview Fig. 3.31 presents the current-voltage characteristics of all four wafers in linear regime.

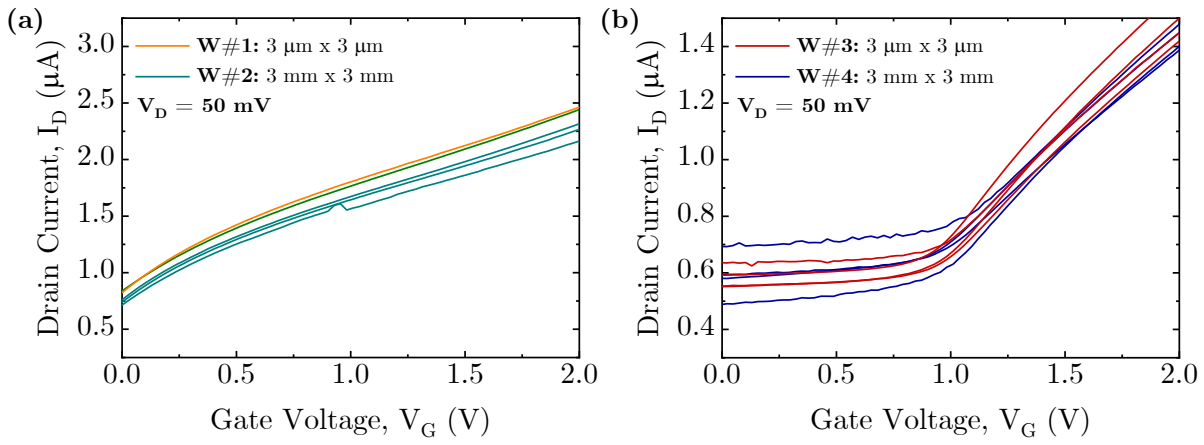


FIGURE 3.31: $I_D - V_G$ curves for all four wafers in linear regime.

First, from $I_D - V_G$ measurements a clear difference is observed from the implanted wafers (#3 and #4) with respect the non-implanted (#1 and #2): non-implanted wafers present a subthreshold region swept towards negative values, while the implanted ones present a threshold voltage near 0.3 - 0.6 V. Nevertheless, as reported during the fabrication, in wafers #1 and #2 an additional wet etching was performed. This overetching resulted in a reduction of the gate oxide thickness and a lateral etching of the gate structure. For that reason, comparison between the measurements of each pair of wafers cannot be fully attributed to the implantation.

Moreover, there is not current leakage through the gate electrode in any of the four wafers. This is indicative that the additional wet etching already mentioned was not aggressive enough to completely remove the oxide.

In wafer #3 and #4, threshold voltage has been measured as well. For larger FET devices, 30 μm x 30 μm, an average value of 607 mV is measured; in the 3 μm x 3 μm case it is 260 mV, within the required interval for SET-FET operation. In addition, body-bias application has prove itself as a useful method to modify the threshold voltage if needed.

Finally, capacitance measurements provide an approximation of the expected quantity of charges trapped in the oxide layer. The calculated amount is on the same level of magnitude than the one obtained from simulations. Nevertheless, the experimentally measured substrate dopant density is remarkably lower than the expected values for these types of wafers.

3.7 SET-FET fabrication

For the complete SET-FET integration the sequence depicted in Fig. 3.3 is followed: after pillar and SOI substrate patterning, all 8" inches wafers are reshaped into 4" for FET fabrication, then the complete SET integration process, including pillar oxidation, takes place; and finally the SET-FET interconnection completes the process.

In terms of pillar processing, the initial wafers present some characteristics that must be mentioned. Three parameters related to the Si NDs performance are considered: the embedded oxide thickness, ion beam mixing (avoided in one of the wafers, to be used as reference), and rapid thermal annealing (RTA) atmosphere conditions for Si NDs activation.

Wafer #	Embedded oxide thickness	Ion beam mixing (Si NDs)	RTA in mixed atmosphere (M1/M2)	First part of FET fabrication	Gate implantation (V_{Th} adjust.)	Plasma oxidation (3 – 5 nm)	Second part of FET fabrication
#1	6 nm	IBM	RTA-M2	1st run	Yes	Yes	2nd run
#2	6 nm	IBM	RTA-M1	2nd run		No	
#3	7 nm	IBM	RTA-M1	1st run	No	Yes	2nd run
#4	7 nm	IBM	RTA-M1	2nd run		Yes	
#5	7 nm	No	RTA-M1	1st run	No	Yes	1st run
#6	8 nm	IBM	RTA-M2	1st run	Yes	No	2nd run
#7	8 nm	IBM	RTA-M2	2nd run		Yes	
#8	8 nm	IBM	RTA-M2	2nd run		Yes	

FIGURE 3.32: Summary of processed wafers for SET-FET integration.

These parameters are treated as independent variables in the set of wafers to be incorporated in this fabrication run. First, thickness of 6, 7 and 8 nm are targeted for the embedded oxide; as mentioned, all wafers but one are Si NDs implanted; and two types of atmosphere conditions for RTA are performed. All this information is collected in Fig. 3.32. In order to minimize risks during FET fabrication, the eight wafers are separated in two batches to be processed at different velocities. Hence, the complete batch is split in two groups, keeping wafers of different characteristics in each separated lot. Moreover, in that way the process conditions for the latter run can be modified if needed.

The non-irradiated wafer #5, incorporated in the first run to be fabricated, follows a different pathway. Since there is no Si NDs in the embedded oxide of these pillars, the SET operation becomes ineffective and thus the SET-FET integration loses its purpose. Nevertheless, this wafer is used for two specific aims: first, validating once again the pillar integrity after the first part of the FET fabrication; and besides, it will lead the second part for the FET completion.

3.7.1 First part of FET fabrication

The starting point is four 4" wafers with patterned nanopillars, distributed in top-silicon islands in a SOI substrate. The resist deposited for pillar protection during reshaping is removed according to the preliminary tests described in section 3.4.1. After resist stripping the BOX and top-silicon thickness is verified by ellipsometry, with values of 404.0 ± 0.1 nm and 159.7 ± 1.6 nm, respectively. Fig. 3.33 shows that there are no resist residues along the wafer.

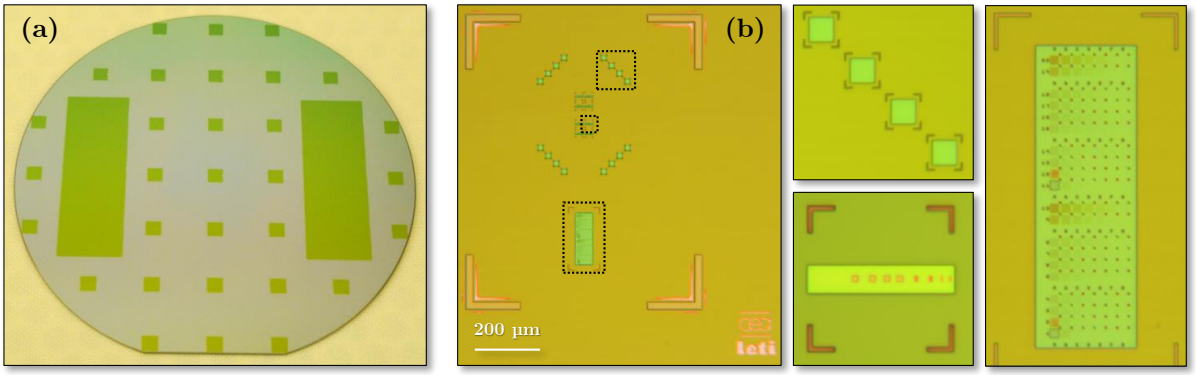


FIGURE 3.33: Wafer #3 after resist removal (a) with optical images of the inner regions (b).

Then a target thickness of 300 nm Si_3N_4 is deposited by PECVD, as pillar protection during the FET fabrication. The resulting Si_3N_4 thickness for all wafers are presented in Fig. 3.34. It is observed some inhomogeneity in the Si_3N_4 layer for wafer #6, with significant dispersion along the wafer position. It is decided to continue processing all four wafers, given that the Si_3N_4 is still fulfilling its protective function.

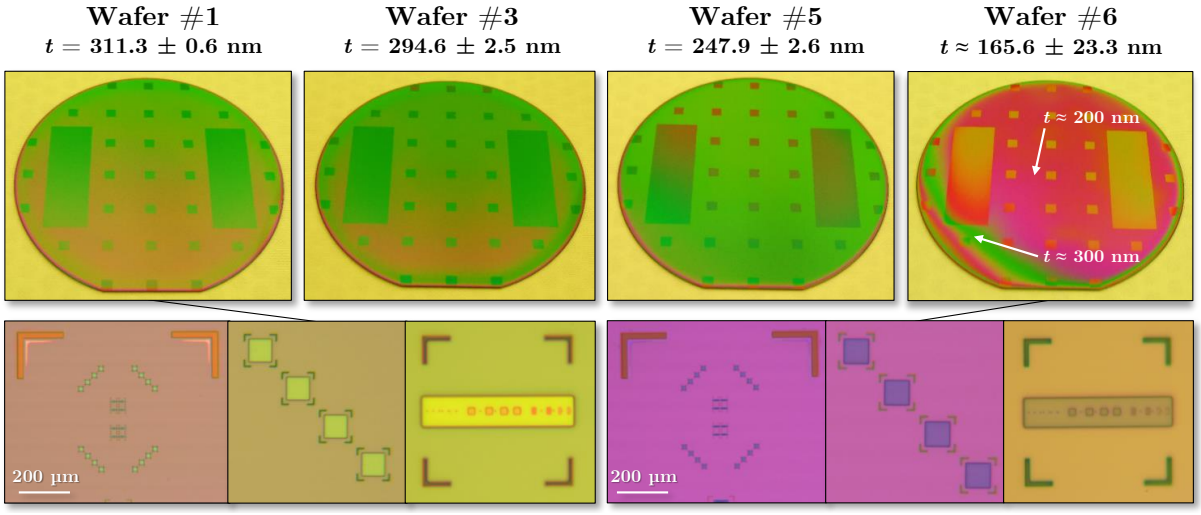


FIGURE 3.34: All wafers after Si_3N_4 deposition, with inner regions for wafer #1 and #6.

Now the first photolithography step is performed, with special attention in the positioning with respect the alignment marks patterned at CEA-Leti. Then the Si_3N_4 is locally etched by RIE. Gate oxidation is performed at the same conditions than previous tests and standalone FETs fabrication: a target thickness of 36.5 nm after 114 min at 900°C. Again, only two of the four wafers are boron-implanted for threshold voltage adjustment, in this case wafers #1 and #6.

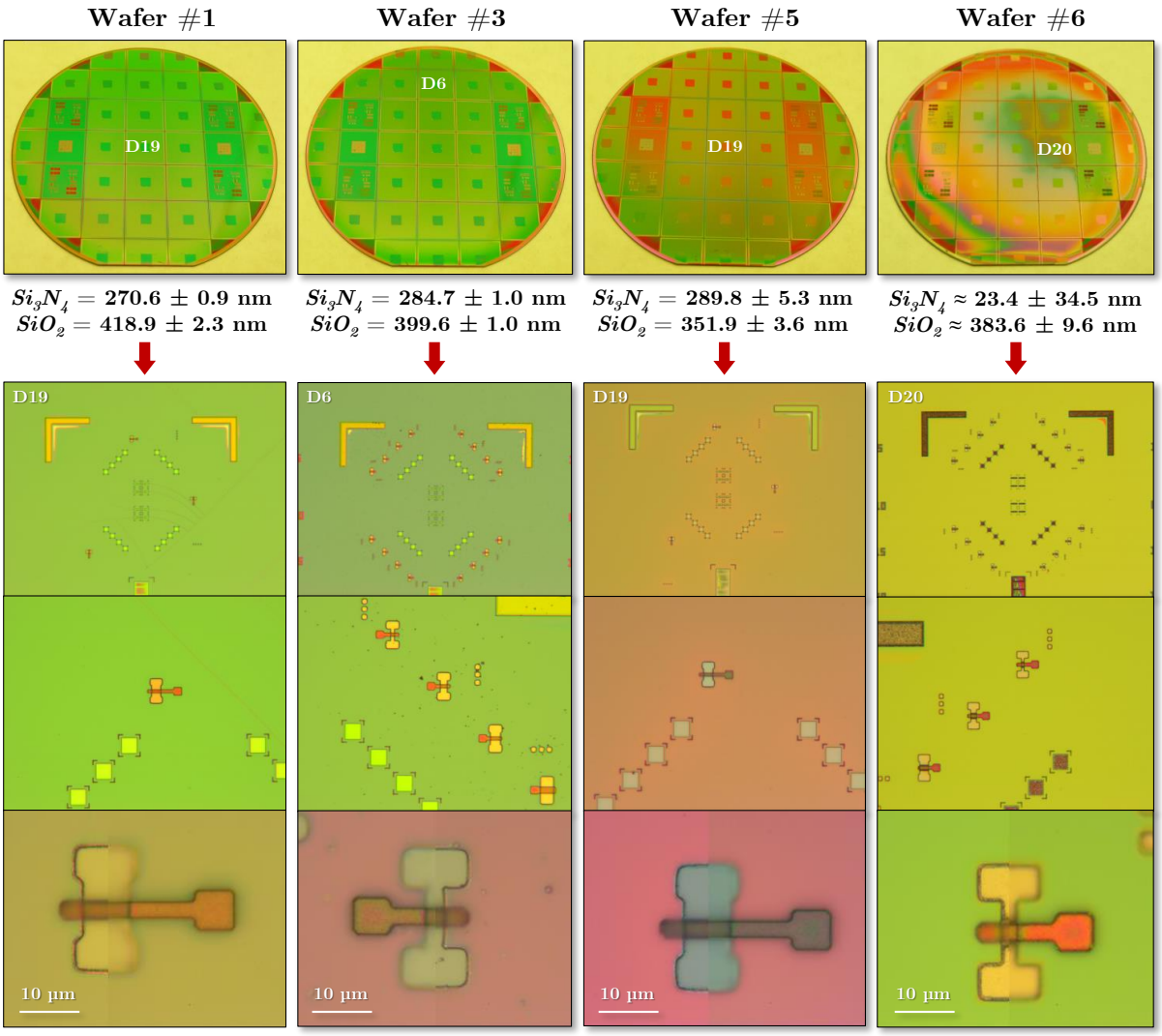


FIGURE 3.35: All four wafers after polysilicon dry etching for patterning, with optical images at different positions.

By LPCVD at 630°C a 480 nm thick polysilicon layer is deposited and doped by $POCl_3$ diffusion at 850°C for 16 min. Through a second lithography step followed by RIE, the polysilicon layer is patterned forming the FET gate. Fig. 3.35 summarizes the aspect of all wafers after dry etching. In this case no isotropic wet etching is performed, as it may cause some additional issues of lateral polysilicon etching, as experienced during the previous FET fabrication. In the

particular case of wafer #6, the dry etching has reduced significantly the Si_3N_4 layer. As a consequence, the inhomogeneity in the protective layer is propagated up to this stage, with very low thickness values in most of the wafer.

Fig. 3.36 presents more of the patterned features for all wafers after resist stripping. As visible, it can be observed the FET arrays located near the top-silicon islands where the SET is to be integrated afterwards.

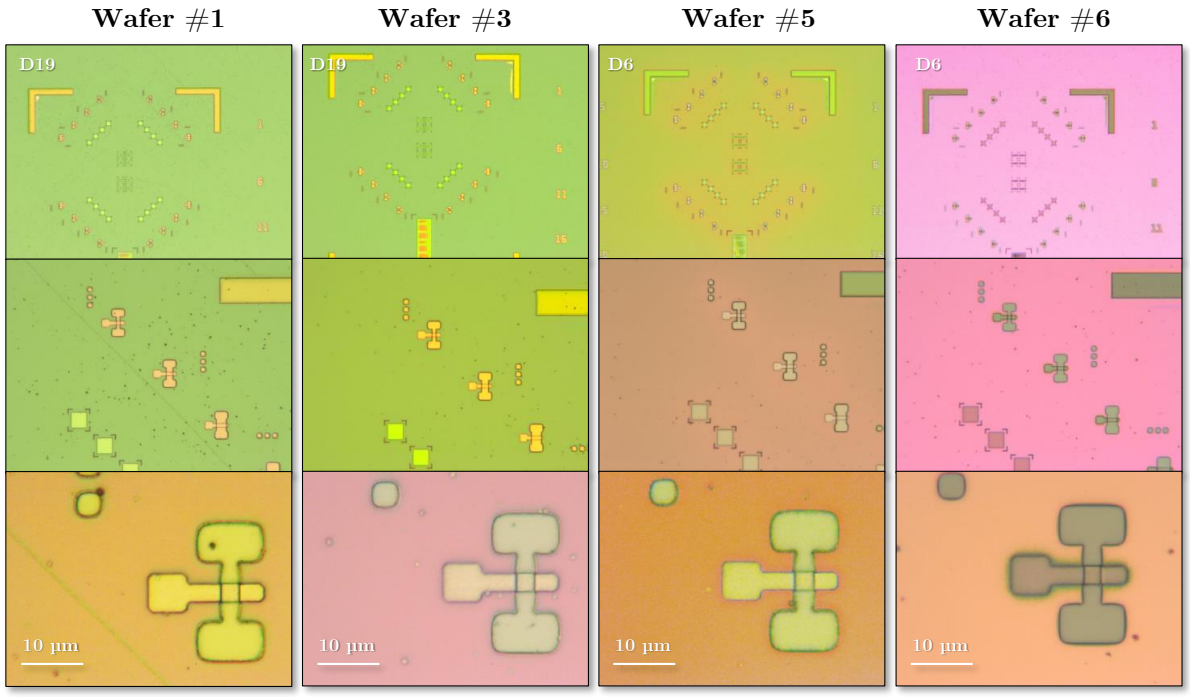


FIGURE 3.36: All four wafers after resist removal for second lithography step.

The next process is the Source/Drain implantation. Again, same standard values than in the standalone FET are used: phosphorus implantation at 100 keV and 4.2 x 10^{15} at $\cdot$ cm^{-2}. Afterwards, a 1.3 μm thick layer of TEOS is deposited by PECVD, followed by fluidification at 850°C for 30 min.

Then another photolithography step is performed. In this case the objective is to etch the TEOS layer in the inner regions where there are the protected pillars. After resist stripping, the Si_3N_4 layer initially deposited for pillar protection can be now removed by immersion in H_3PO_4, in agreement with the tests described in section 3.4.2. In this point, the first part of the FET fabrication is considered to be completed, summarizing the process up to step 7 in Fig. 3.5.

3.7.2 Plasma oxidation

The next step is sending the wafers for plasma oxidation. Note that wafer #6 is discarded from further processing, as the Si_3N_4 protection has been almost removed in most of the wafer, mostly due to its initial lower thickness. An HF dip is performed in the remaining wafers to remove their native oxide, so silicon can be oxidized. Then, plasma oxidation takes place by means of 110s in He/O_2 (15/85) ambient.

Before resuming the FET processing, efforts are focused again on the characterization of pillar integrity. Fig. 3.37 presents TEM measurements of three pillars of different diameter from wafer #3 after plasma oxidation. As it can be seen, the whole pillar is covered with a 3−4 nm SiO_2 layer, slightly thinner on top of the silicon cap. In addition, Si NDs can be observed in the larger pillars, where the embedded oxide is thick enough. In this case, NDs diameter are around 2.6−3.2 nm, and tunnel junction is about 1 nm in both directions.

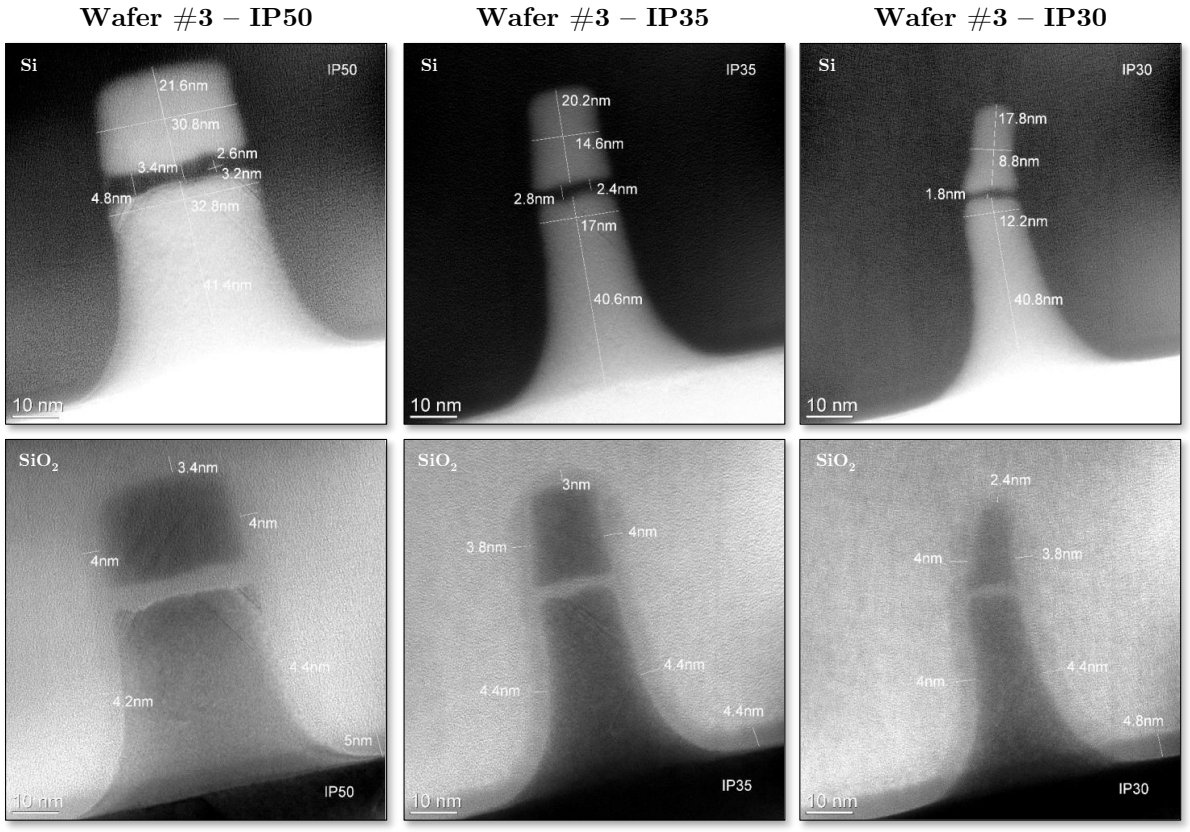


FIGURE 3.37: EFTEM Si (top row) and SiO_2 (bottom row) plasmon loss images of three pillars from wafer #3 after plasma oxidation.

As already mentioned, wafer #5 was not Si irradiated during the early stages of processing. Indeed, as Fig. 3.38 shows, pillars from this wafer do not present Si NDs at all, even the largest. Nevertheless, all pillars are still integer, to the point that even the silicon crystalline structure can be appreciated. Besides, a thin SiO_2 layer all around the pillar is observable as well.

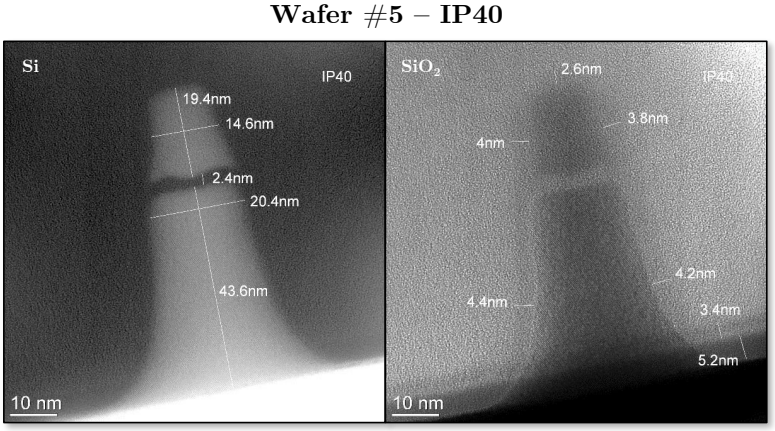


FIGURE 3.38: EFTEM plasmon loss images of IP40 from wafer #5 after plasma oxidation.

Therefore, wafer #5 is cleaved into quarters for further processing. Chips from one quarter are used for the TEM characterization depicted in Fig. 3.38. An entire quarter is aimed to continue the second part of the FET fabrication, described in the following section. Before starting the process, AFM measurements are performed. As Fig. 3.39 indicates, all five pillars present the proper shape and dimensions, as it was expected from TEM characterization. The conclusion is that the protection-deprotection methodology of both the resist during reshaping and Si_3N_4 during FET fabrication is effective.

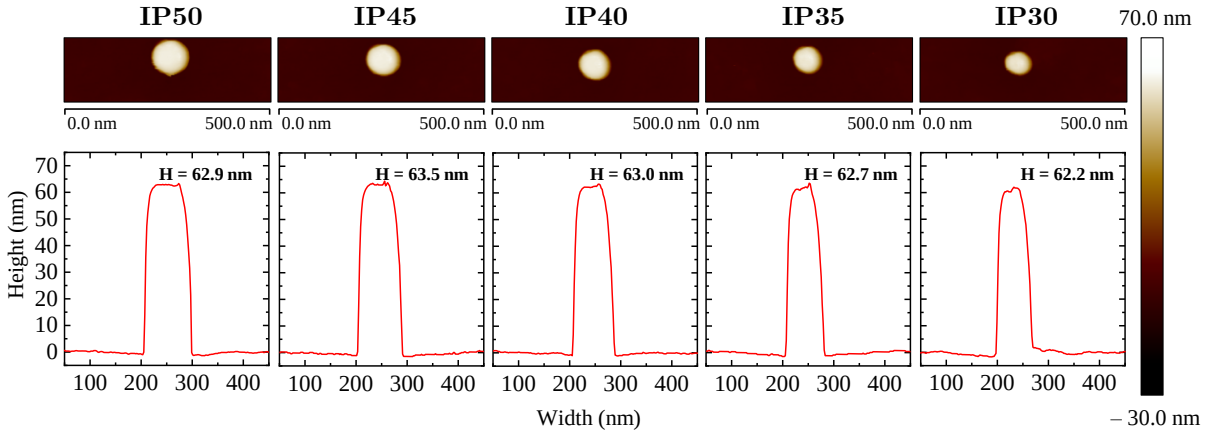


FIGURE 3.39: AFM measurements and profiles of five consecutive pillars from wafer #5 after FET fabrication and plasma oxidation.

3.7.3 Second part of FET fabrication

The remaining part of the FET fabrication concerns the contact windows etching and metal routing. First, a standard photolithography step is followed by the RIE of the TEOS layer. Afterwards, a 1.0 μm Al:Cu layer is deposited by sputtering. In this case the metal is patterned by wet etching, not dry etching as it was in the standalone FET. Wet etching is the only equipment-compatible solution, given the ¼ wafer shape operation and its contamination level after plasma oxidation.

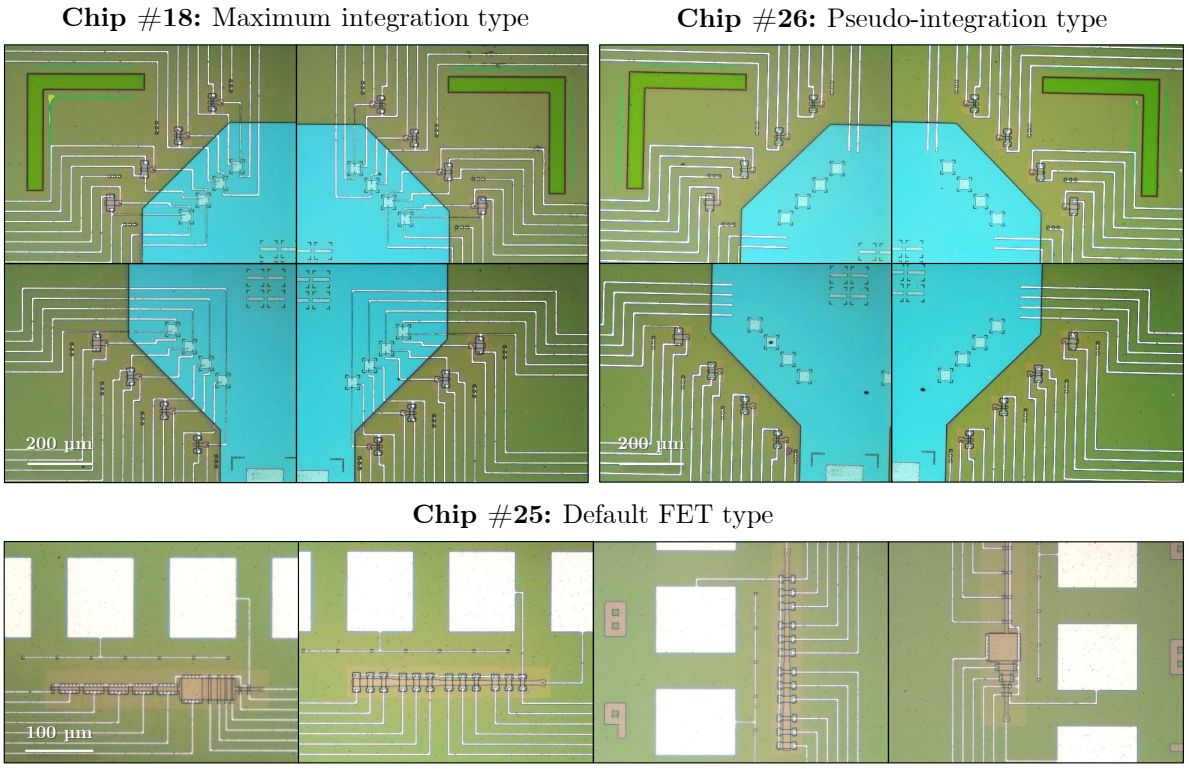


FIGURE 3.40: Optical images of one example of each of the designs after FET completion: maximum-integration, pseudo-integration and default FETs.

In Fig. 3.40, optical images after FET completion are presented for each of the aimed designs. With respect the previous standalone FET fabrication, in this ¼ wafer the pillar integrity has been strongly monitored and validated, providing with structural characterization in terms of AFM and TEM. Moreover, given the process requirements, some additional variations are found; for instance, narrower metal stripes are obtained in this case, due to the isotropy of its wet etching.

3.8 FET characterization

As Fig. 3.40 shows, there are three different layout designs in the processed ¼ from wafer #5. In all cases, there are inner regions with smaller FETs near the pillar top-silicon islands. The following measurements are focused on those devices, whose nominal dimensions range for WxL from 3x3, 6x3, 9x3 to 12x6 μm x μm; transistors are named T1, T2, T3 and T4, respectively.

3.8.1 I_D-V_D curves

Fig. 3.41 presents the I_D-V_D curves with gate bias applied from 0 to 2 V for all measured devices. As it can be observed, similar output current is obtained for each group of devices, being the FET T1 the one with larger dispersion.

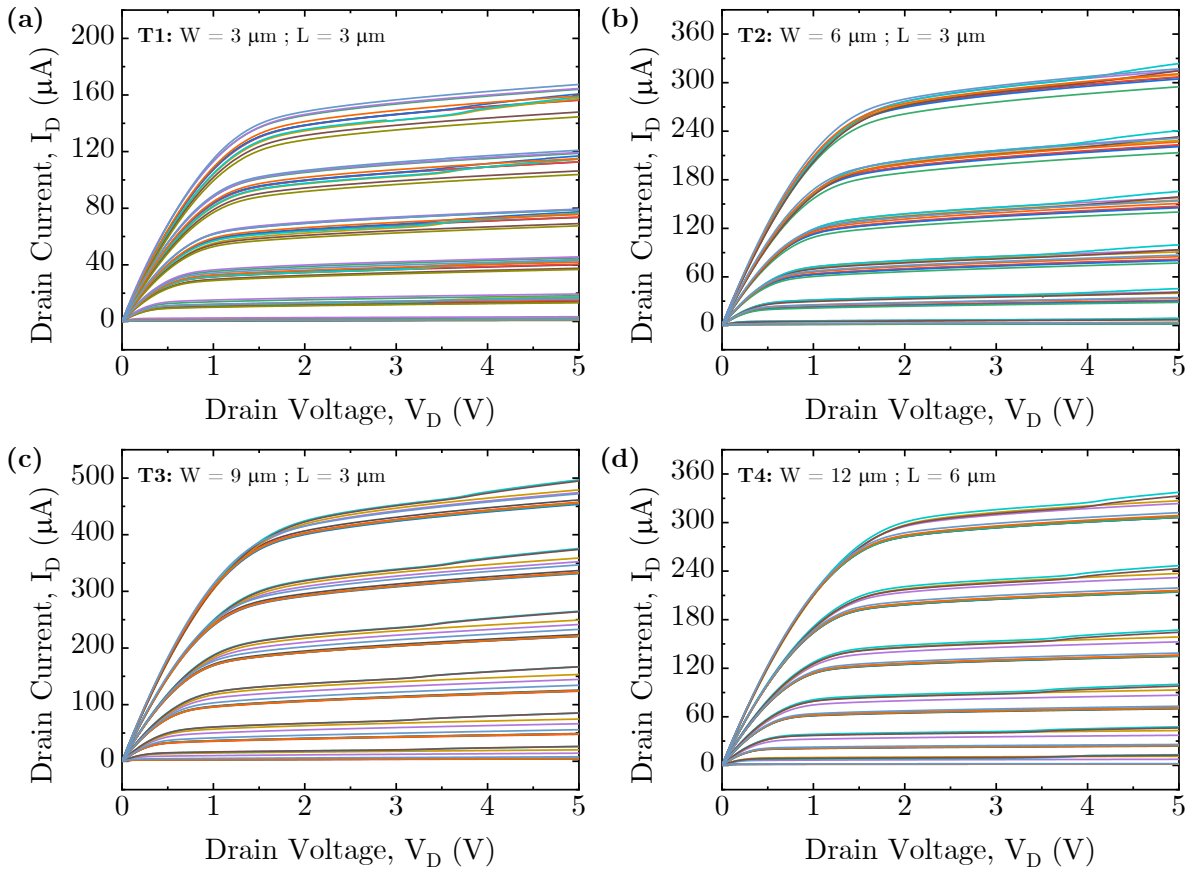


FIGURE 3.41: Summary of I_D-V_D curves for all devices in ¼ wafer #5 while applying gate bias from 0 to 2 V in six steps, ordered by dimensions.

3.8.2 I_D-V_G curves

Similarly, Fig. 3.42 presents the I_D-V_G measurements for T1 and T3 in linear and saturation regime (drain bias of 50 mV and 1 V, respectively). It can be observed that negative values for threshold voltage are measured. Note that this wafer was not boron-implanted for V_{Th} adjustment after gate oxidation, which justifies the on-state current.

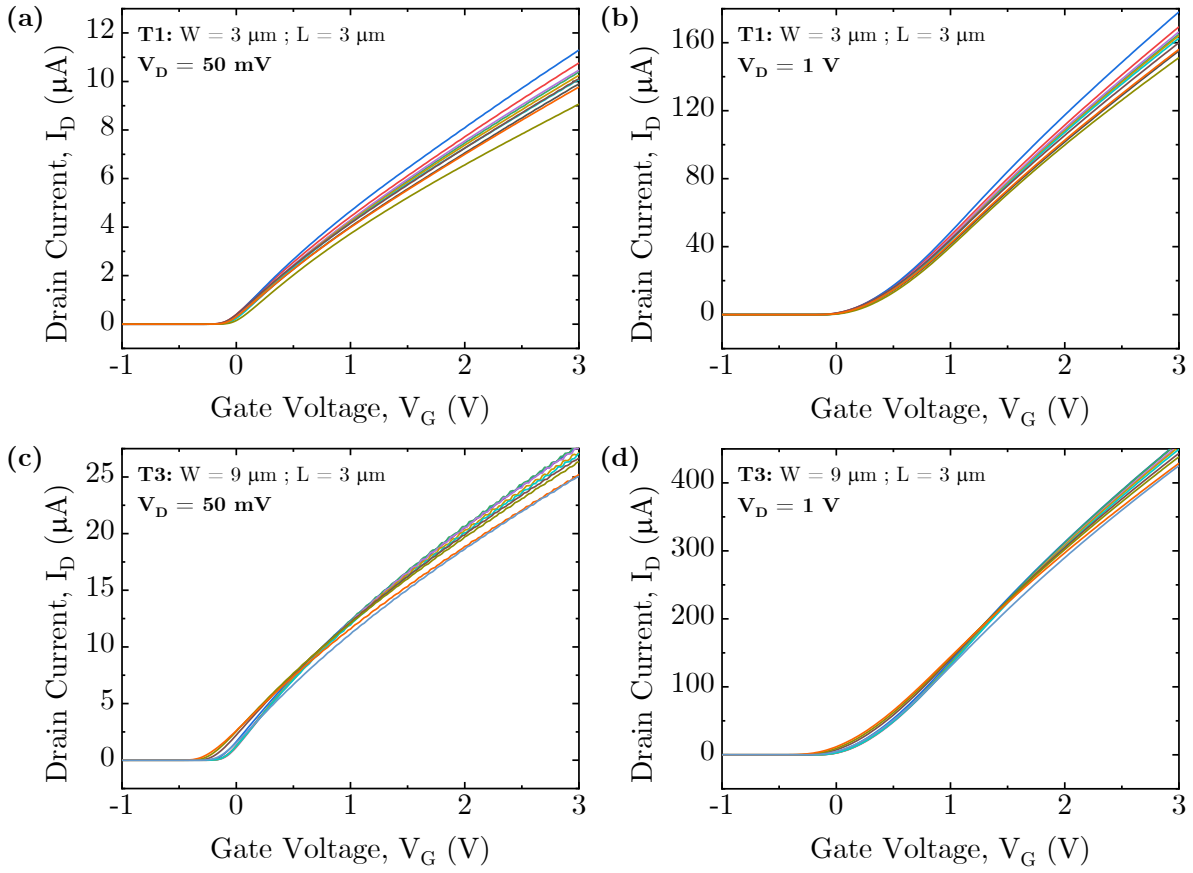


FIGURE 3.42: Summary of I_D-V_G curves for all T1 and T3 devices in ¼ wafer #5.

3.8.3 I_D-V_G curves with V_{BB}

As already proved during the characterization of standalone FET in the previous fabrication run, by applying a certain bias in the body terminal the I_D current can be swept towards higher voltage values. This is reflected in the current level and in the transconductance maximum, and as a consequence V_{Th} can be driven towards different values. Fig. 3.43 illustrates an example of this effect for the measured devices, with V_{BB} from 0.5 to −2 V.

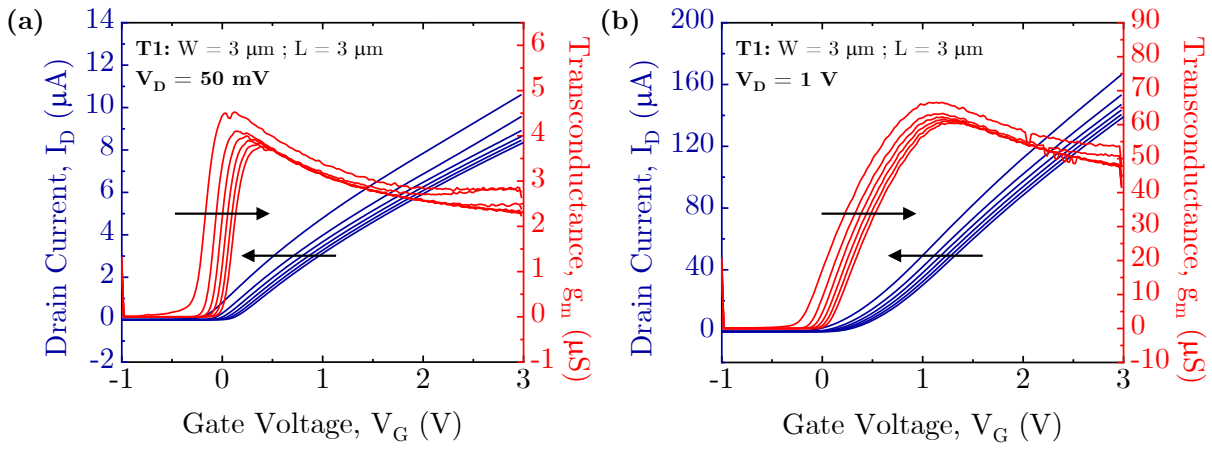


FIGURE 3.43: Example of I_D-V_G curve for one of the smallest FET with body bias V_{BB} applied from 0.5 to −2 V in linear (a) and saturation regime (b).

3.8.4 Normalized current

In order to normalize the output current represented in Fig. 3.42, an approximation for the real dimensions of channel length and width is required. With that aim, a third of the total number of devices is measured, with samples from all nominal dimensions and dies.

In Fig. 3.44 the average measured values for both parameters are presented, altogether with the nominal dimensions. In all devices a slightly shorter channel width is measured, while channel lengths are larger than expected. Nevertheless, low dispersion is obtained for both parameters, either regarding the FETs dimension or their die position along the wafer.

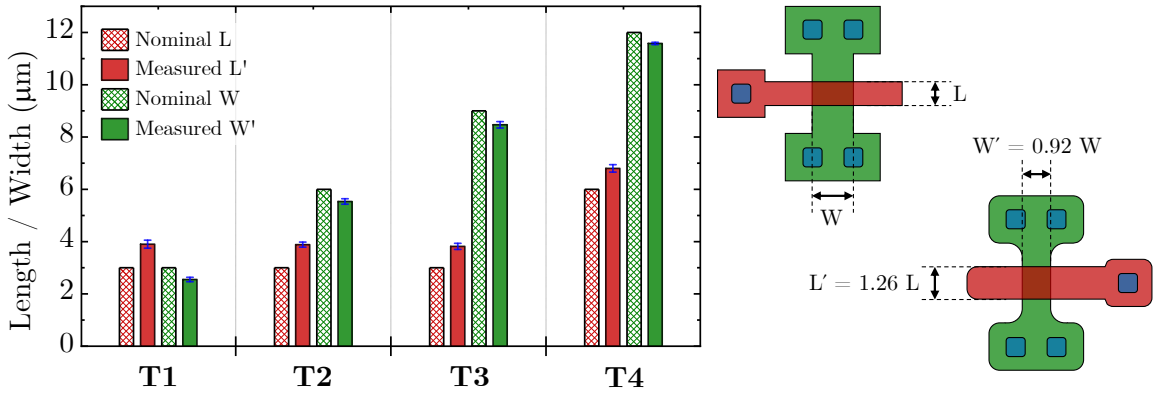


FIGURE 3.44: Statistics of the nominal and measured values for channel length and width with the corresponding dispersion and schematics of the resulting L and W factor.

Now, output current for all devices can be normalized by the corresponding W/L factor. As observable from Fig. 3.45, similar output current is obtained in all family of devices, both in linear (a) and saturation (b) regimes.

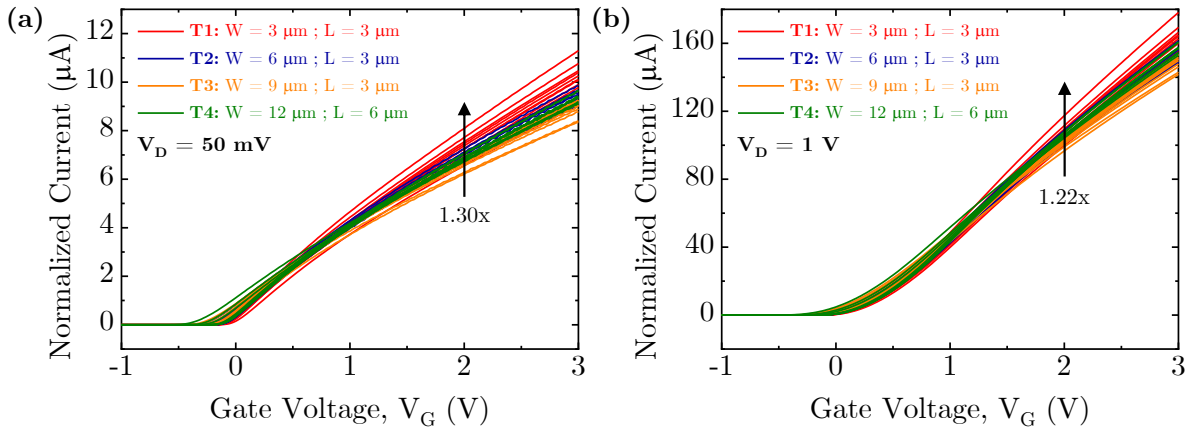


FIGURE 3.45: Normalized current for all devices in linear (a) and saturation regime (b).

3.8.5 C−V curves

Proceeding in the same way than in the C-V measurements presented in Appendix E regarding standalone FETs, an approximation of the interfacial oxide charges can be obtained for wafer #5. In this case, focusing in the measurements performed at 100 kHz, a total fixed charge density of 1.83×10^{10} cm^{-2} is calculated from the measurements depicted in Fig. 3.46.

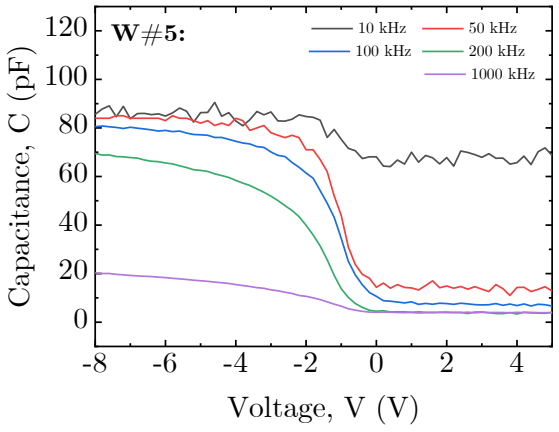


FIGURE 3.46: C−V measurements for ¼ wafer #5 between silicon and polysilicon at different frequencies.

3.8.6 Parameters extraction

In the following section the fabricated devices are parametrized in terms of DIBL, transconductance maximum, threshold voltage and subthreshold slope. The methodology to obtain these parameters is described in section 1.2.2 of Chapter 1.

(i) DIBL and transconductance maximum

As Fig. 3.47.a presents, the calculated DIBL presents an average value of 429.43 ± 15 mV/V, slightly higher for the T4 family of devices. This parameter already gives information about the threshold voltage and its dependence on drain bias. The drain current is not only controlled by the gate voltage, but also by the drain bias. This is in agreement with the lateral shift observed in the subthreshold region of the $I_D - V_G$ transfer curves. Fig. 3.47.b shows all the measured values for the transconductance peak; as it can be observed, G_{max} does depend on device dimension, and presents values very well fitted for each family of devices.

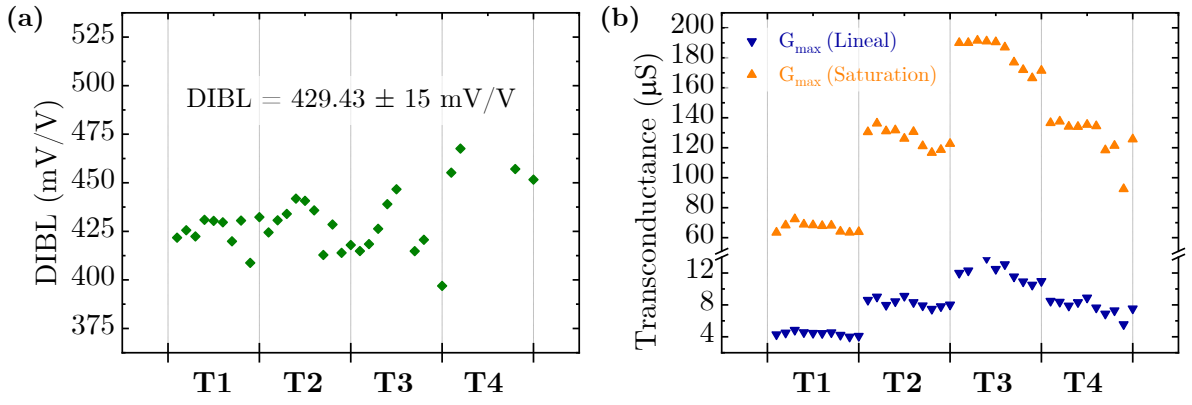


FIGURE 3.47: DIBL (a) and G_{max} (b) for all devices ordered by FET dimension.

(ii) Threshold voltage in linear regime

The main parameter to be monitored in view of the SET-FET hybrid circuit is the threshold voltage. As deduced from $I_D - V_G$ curves, negative values for V_{Th} are obtained. This was already expected, given the dopant concentration of the substrate wafer and the non-implantation for V_{Th} adjustment during the FET process. Moreover, it results clear that threshold voltage is independent from device dimension or die position, as Fig. 3.48 indicates. In linear regime, an average V_{Th} of -96.45 ± 25 mV is obtained.

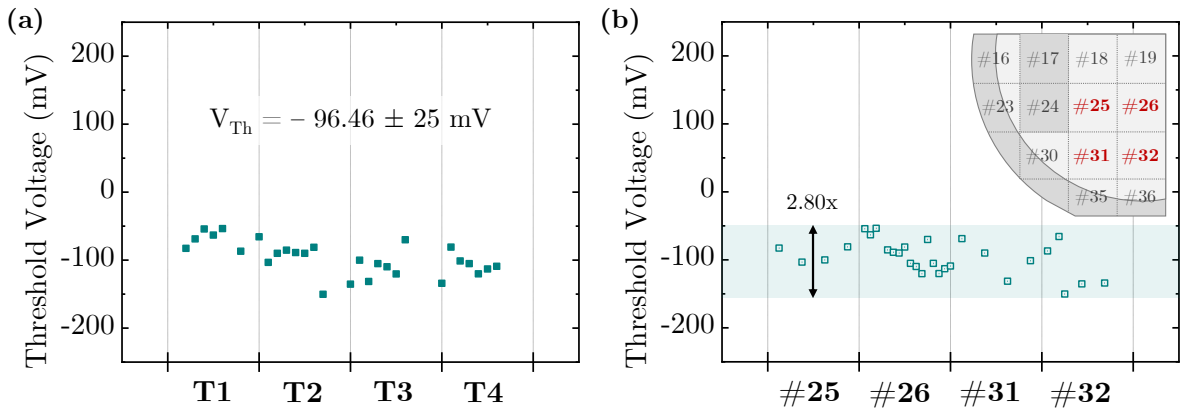


FIGURE 3.48: Measured threshold voltage for all devices ordered by FET dimension (a) and by die position (b).

(iii) Threshold voltage in saturation regime

In the context of the hybrid SET-FET circuit, the FET element is supposed to operate in saturation regime. For that reason, it results convenient obtaining the threshold voltage when a higher drain bias is applied. Fig. 3.49.a shows V_{Th} when $V_D = 1$ V; again, it is independent of device dimensions. An average value of 316.59 ± 38 mV is calculated. Moreover, this value can be even lowered by applying voltages at the body terminal. As Fig. 3.49.b indicates, a body bias of 0.5 V corresponds to a threshold voltage of 231.71 ± 29 mV. Therefore, it is proved that the required 200 - 300 mV for the FET operation can be achieved.

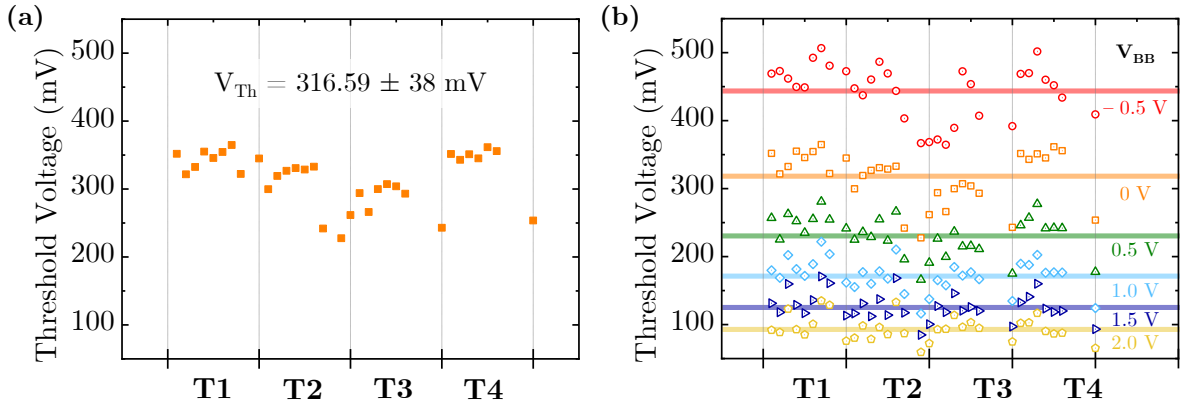


FIGURE 3.49: Measured threshold voltage for all devices in saturation regime (a) and while applying different body biases (b), in both cases ordered by FET dimensions.

(iv) Subthreshold swing

Similarly, also subthreshold swing results independent from transistor type or position along the wafer (Fig. 3.50). An average value of 73.3 ± 2 mV/dec is obtained, very much within the optimum range for device performance.

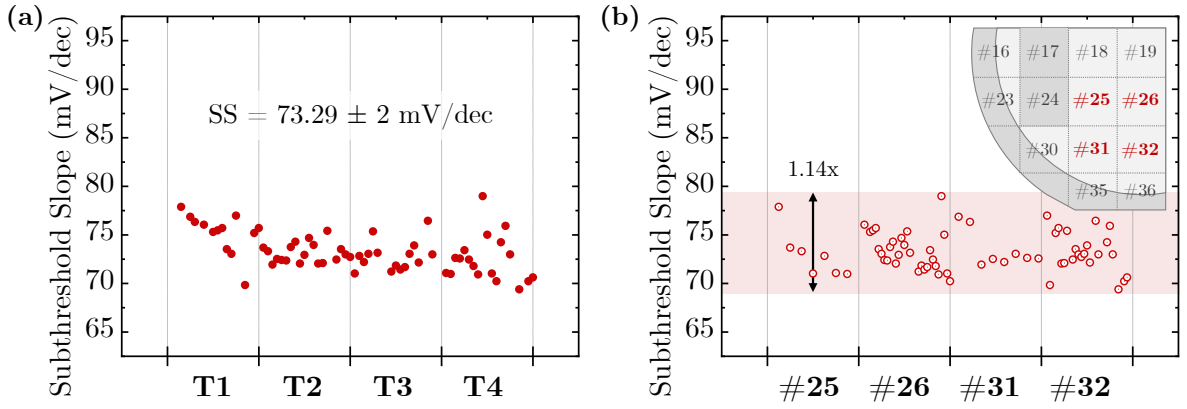


FIGURE 3.50: Measured subthreshold swing for all devices ordered by FET dimension (a) and by die position (b).

This value for the subthreshold swing can be compared with the expected one, according to substrate doping and oxide charges. In the subthreshold region the exponential behaviour of the I_D-V_G characteristic curve is described as follows.

$$I_D \propto e^{V_{GS}/(n\phi_t)} \tag{3.1}$$

Therefore, the slope is determined by $n\phi_t$, with ϕ_t being the thermal voltage which at room temperature is 0.026 V, and n a factor function of dopant concentration, oxide capacitance and Fermi potential.

$$n = 1 + \frac{1}{2\,C_{ox}}\sqrt{\frac{2qN_A\varepsilon_{Si}}{1.5\phi_F}} \tag{3.2}$$

The dopant concentration is in the interval $0.6 - 1.7 \times 10^{15}$ cm^{-3} for the processed wafer, and C_{ox} can be easily measured by Eq. E.1. The Fermi potential ϕ_F at room temperature and at a certain concentration is also known, 0.289 V. Therefore, the resulting theoretical value for the subthreshold slope is 69 mV/dec, very near the average 73 mV/dec measured in Fig. 3.50.a.

3.9 Conclusions

In this chapter the development of a hybrid SET-FET circuit has been designed and tested. First, the process sequence has been designed considering the requirements for each of the integrating elements. In this point, simulations of the SET implementation into a standard FET have been carried out, demonstrating an acceptable parasitic capacitance limit. In addition, the FET requirement in terms of threshold voltage has been studied as well by means of process simulation.

Thereafter, once the process sequence is assured, several preliminary investigations have been performed. First, the analysis focused on the nanopillars and Si NDs integrity after NMOS-related processes. TEM structural analysis showed that neither of these SET characteristics was compromised by any of the steps: resist application and wafer reshaping, silicon nitride deposition or deprotection, or thermal annealing processes. In parallel, two preparatory tests were performed to prove the feasibility of implantation and oxidation at low temperature, in order to adapt the standard CMOS processes to the SET requirements.

The fabrication of standalone FETs under predetermined conditions has been developed. From electrical characterization, threshold voltage values within the SET-compatible interval were measured.

Then, the fabrication of the SET-FET was performed in agreement with the conditions stated from previous experiments. After the first part of the FET fabrication, an exhaustive structural characterization was performed by means of TEM and AFM measurements. In all cases, the pillar integrity was ensured, same aspect-ratio was kept, and Si NDs were clearly visible.

Afterwards, the second part of the FET fabrication was completed in one of the wafers as a test sample. From the electrical characterization, a good device performance was observed, in spite of being a non-implanted wafer. In terms of subthreshold characteristics, the measured 73.3 mV/dec subthreshold swing is very near the theoretical 69 mV/dec, the expected value considering the substrate dopant concentration.

In summary, the issues arising from the SET-FET integration have been separately addressed and solved in a preparatory way, in particular in terms of thermal budget. Afterwards, these conditions were implemented in the fabrication of compatible FETs at the same level than patterned nanopillars. And finally, both pillar integrity and FET robust performance are proved, paving the road towards the SET-FET final integration.

Chapter 4

Modelling of vertical Nanowire Field Effect Transistor

In this chapter, the modelling of a vertical nanowire (NW)-based Field Effect Transistor (FET) is presented. The resulting output current from the modelled NWFET is optimized in terms of device dimensions, in order to optimize the behaviour at subthreshold regime for its implementation in a hybrid SET-FET circuit. Variability mitigation is analysed in order to improve the device performance and stability. Finally, the benefits of implementing vertical NWFETs in array configurations for these aims are investigated.

4.1 Introduction

The continuous demand for high performance and low power consumption has pushed CMOS technology to the ultimate nanoscale dimensions. As device dimensions are scaled down, relevant improvements in terms of power efficiency, reliability and device performance are attained. Nevertheless, for the 32 nm node technology and beyond the conventional planar MOSFET presents intrinsic drawbacks as leakage current and large device performance variability [86]. In order to overcome these effects, novel state-of-the-art architectures have been widely studied during last decades, as introduced in Chapter 1. FinFET architecture has been a clear breakthrough, as its 3D channel allows achieving more drive current per unit area than planar devices, while exhibiting larger device variability mitigation [87]. However, the continuous need for increased integration density brings FinFETs to the limit of their applicability for the most advanced nodes. In order to move forward to the end of the transistor roadmap [88], technology requires higher integration density enhancement.

In this framework, NW-based transistors are a promising candidate to continue beyond FinFET performance, since their full surrounding gate-all-around (GAA) arrangement allows better gate control of the channel conduction, and thus higher electrostatic stability, increased immunity against short channel effects (SCE) and low power consumption [66]. NWs can be arranged in a lateral or vertical configuration, presenting the first one the need of regular 2D layouts and hence with consequent physical limits in terms of device density and connection routing congestion. With vertically arranged NWs, it moves to a 3D layout configuration where the channel is defined vertically [89], [90]. In that way, vertical FETs have demonstrated larger scalability than lateral devices [14], outperforming FinFET and lateral architectures in terms of speed and power consumption [91], [92].

In addition, continuous scaling in planar and lateral devices inevitably requires the reduction of contacted gate pitch (CGP), resulting in a trade-off between gate length, S/D spacers and S/D metallic contacts. A gate long enough to maintain reasonable levels of SCEs is needed, as well as a minimum intermetal thickness defined by reliability requirements and capacitance between electrodes. In this context, vertical GAA devices are less restricted on gate length and insulating intermetal layers, as their vertical orientation allows certain design relaxation [66], [14]. Nevertheless, in vertical devices the channel width is defined as the diameter of the contacted structure. It is a parameter very susceptible to manufacturing variations; for this reason, Process-Voltage-Temperature (PVT) variations must be investigated in order to ensure good levels of device reliability [93], [94] and enable the comparison between lateral and vertical GAA devices.

Scalability is another remarkable advantage with respect to conventional planar architectures. By integrating vertical devices, the low footprint significantly reduces the area cost together with an improvement in the device performance [95]. As a consequence, array configuration is a potential option for circuit improvements.

Currently, vertical topologies are explored for their further implementation in different types of electronic devices. In Chapter 2 the integration process towards a vertical Single Electron Transistor (SET) has been presented [60], [81]. Similarly, the fabrication of vertical NW-based FETs is already demonstrated in the literature [66], [14].

The use of vertical devices in integrated circuits, such as CMOS inverters or hybrid circuits, presents as well remarkable potential. For instance, through its combination with low power consumption devices, such as the already introduced SET, a wide range of logic and storage applications can be enabled [75]. As already mentioned in Chapter 3, the co-integration of a hybrid SET-FET circuit might benefit from the SET advantages while overtaking its intrinsic

drawbacks, as background noise or device stability [96]. However, in the framework of the SET-FET hybrid circuit, the FET must operate at subthreshold regime, and therefore low threshold voltage values, good subthreshold characteristics and low leakage are required for optimum performance.

Vertical NWFET might represent a clear breakthrough in terms in terms of performance, integrability and scaling density. This innovation drives to new possibilities, but requires as well previous groundwork in process-design optimization. It has to be considered that the integration process of vertical transistors is not at the same level of technological maturity than conventional planar integration.

In this chapter, the modelling of a NWFET is presented as function of the device dimensions, nanowire diameter and channel length. Device performance and parameter characteristics are compared with FinFET, with particular focus on the subthreshold behaviour. Once the NWFET dimensions are optimized in terms of optimum subthreshold characteristics and variability mitigation, its implementation in circuits is investigated: first in CMOS inverters and second in hybrid SET-FET circuits. Finally, the benefits of using array arrangements is discussed.

4.2 Vertical NWFET and FinFET modelling

4.2.1 Model description

In this section the NWFET and FinFET models are described. Both devices have been simulated with the Synopsys Sentaurus TCAD software [82], an advanced 3D simulator suitable for silicon and non-silicon semiconductor devices. It is widely used for the design and characterization of current and future process technologies, as it provides information about carrier transport, velocity saturation, surface and bulk scattering and quantization effects.

Fig. 4.1 presents the model for NWFET simulation. It consist of a vertical nanopillar patterned from a bulk p-type silicon substrate, boron-doped at 1.0 x 10^{15} at $\cdot$ cm^{-3}. The diameter ($\varnothing_{NW}$) and height (H_{NW}) are input variables for the simulation. A thin SiO_2 layer with t_{ox} = 2 nm covers all the pillar. The surrounding gate is made of tungsten due to its well-known work function; it has a thickness of t_{GAA} = 6 nm, it is located at half the height of the pillar, and its height defines the channel length $L_{Channel}$.

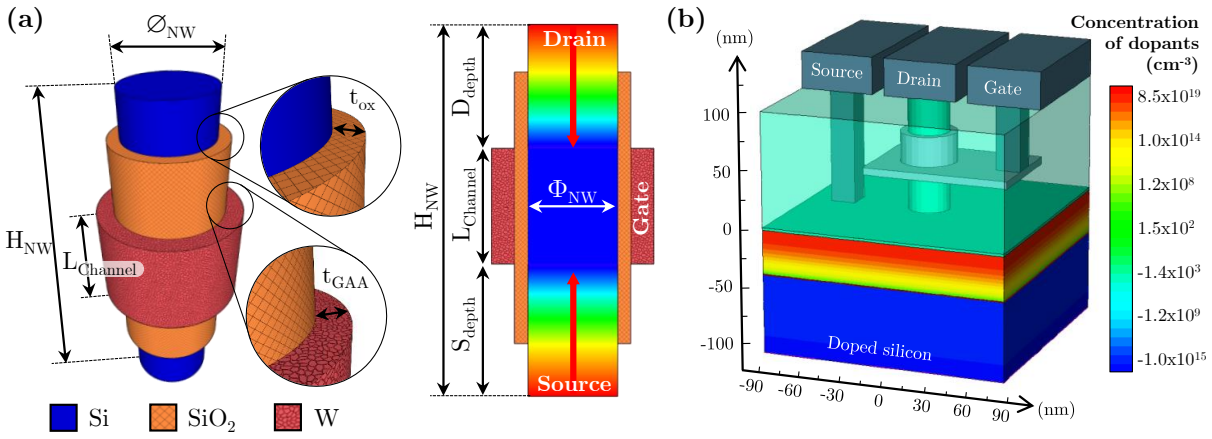


FIGURE 4.1: Scheme of the vertical NWFET, with detail of the dimensions, implantation parameters (a) and the resulting 3D model with dopants concentration (b).

Source and drain regions are equally doped with phosphorus at 1.0 x 10^{19} at $\cdot$ cm^{-2}; the junction depth is defined as $S/D_{depth} = (H_{NW} - L_{Channel})/2$, to ensure dopants diffusion up to the channel. Metal interconnections have been considered as well, with silicon nitride as insulating intermetal layers and aluminium as top metal routing.

Similar parameters are defined to model the FinFET, as presented in Fig. 4.2. A fin-shaped structure in a p-type silicon substrate with dimensions defined by fin length (L_{Fin}), height (H_{Fin}) and width (W_{Fin}). Same materials, implantation values and S/D junction depths as in the NWFET case are considered.

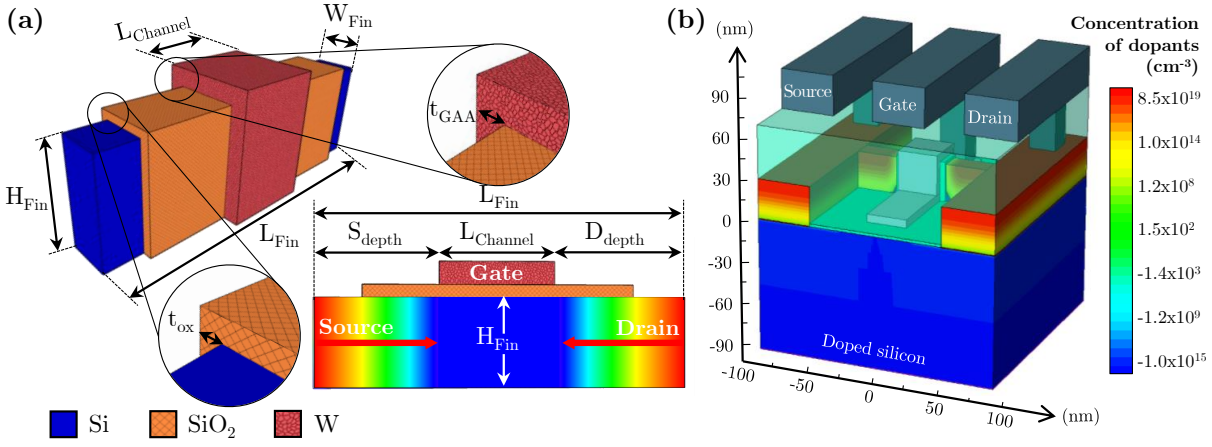


FIGURE 4.2: Scheme of the vertical FinFET, with detail of the dimensions, implantation parameters (a) and the resulting 3D model with dopants concentration (b).

4.2.2 Dimension optimization

In a first approximation $\varnothing_{NW}$ and $L_{Channel}$ are the two parameters investigated: one is fixed at 30 nm and the other one is modified from 10 nm to 50 nm. In that way, the role of each parameter can be deduced individually. FinFET simulations are performed in parallel for comparison; in both cases the total NW/Fin length is fixed at 100 nm.

Fig. 4.3 presents the resulting current-voltage characteristic at linear regime (V_D = 50 mV), for both FinFET and NWFET devices. As it can be observed, while an increment in $L_{Channel}$ corresponds to a higher output current in both cases, it is a much more pronounced increment in the case of FinFET. Moreover, a wider silicon channel (i.e. a larger $\varnothing_{NW}$ and H_{Fin}) corresponds to a higher output current, but in this case it is much more relevant in the case of NWFET. In other words, NWFET is more dependant on $\varnothing_{NW}$ than FinFET is on H_{Fin}. This behaviour is consistent with the expected: a reduction in the channel width is more critical for configurations in which the gate contact is intrinsically increased, as it happens in a full GAA configuration.

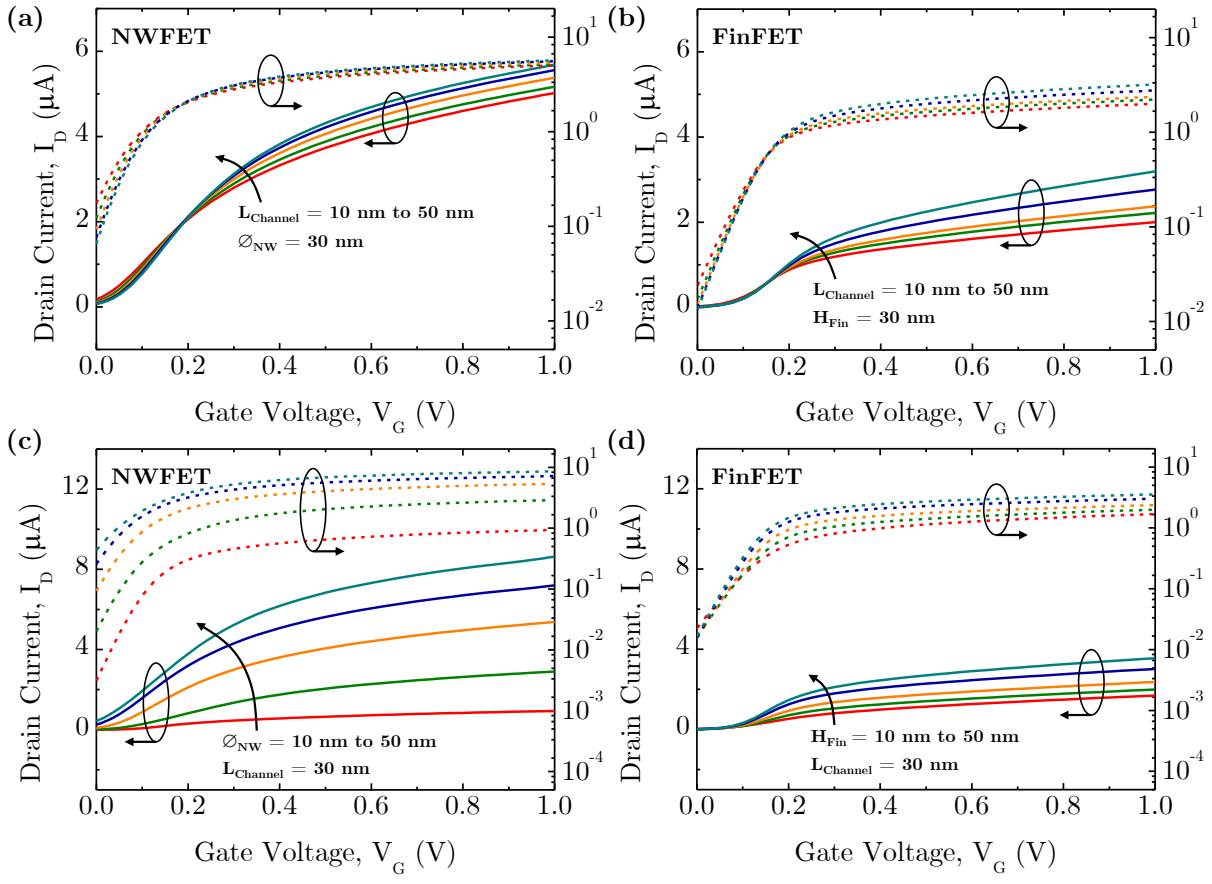


FIGURE 4.3: Current-voltage characteristics for NWFET (left) and FinFET (right) when modifying channel length (top) and channel width (bottom).

4.2.3 Electrical characteristics

Now the analysis is focused on the effects of dopants concentration on the electric performance of NWFET and FinFET. Nominal dimensions are stated at $L_{Channel}$ = 30 nm in both cases, $\varnothing_{NW}/H_{Fin}$ as 30 nm and H_{NW}/L_{Fin} again fixed in 100 nm. Implantation conditions are as described in previous section (i.e. phosphorus implantation at 1.0 x 10^{19} at $\cdot$ cm^{-2} in a p-type bulk silicon substrate), with a drain bias of 50 mV. The analysis is expressed in terms of electric field, electrostatic potential, electron mobility, density and velocity.

Fig. 4.4 shows the profile of each parameter along the NW/Fin, with detail of axial cross-sections. From (a) a constant electric field is observed along the channel, with two peaks of

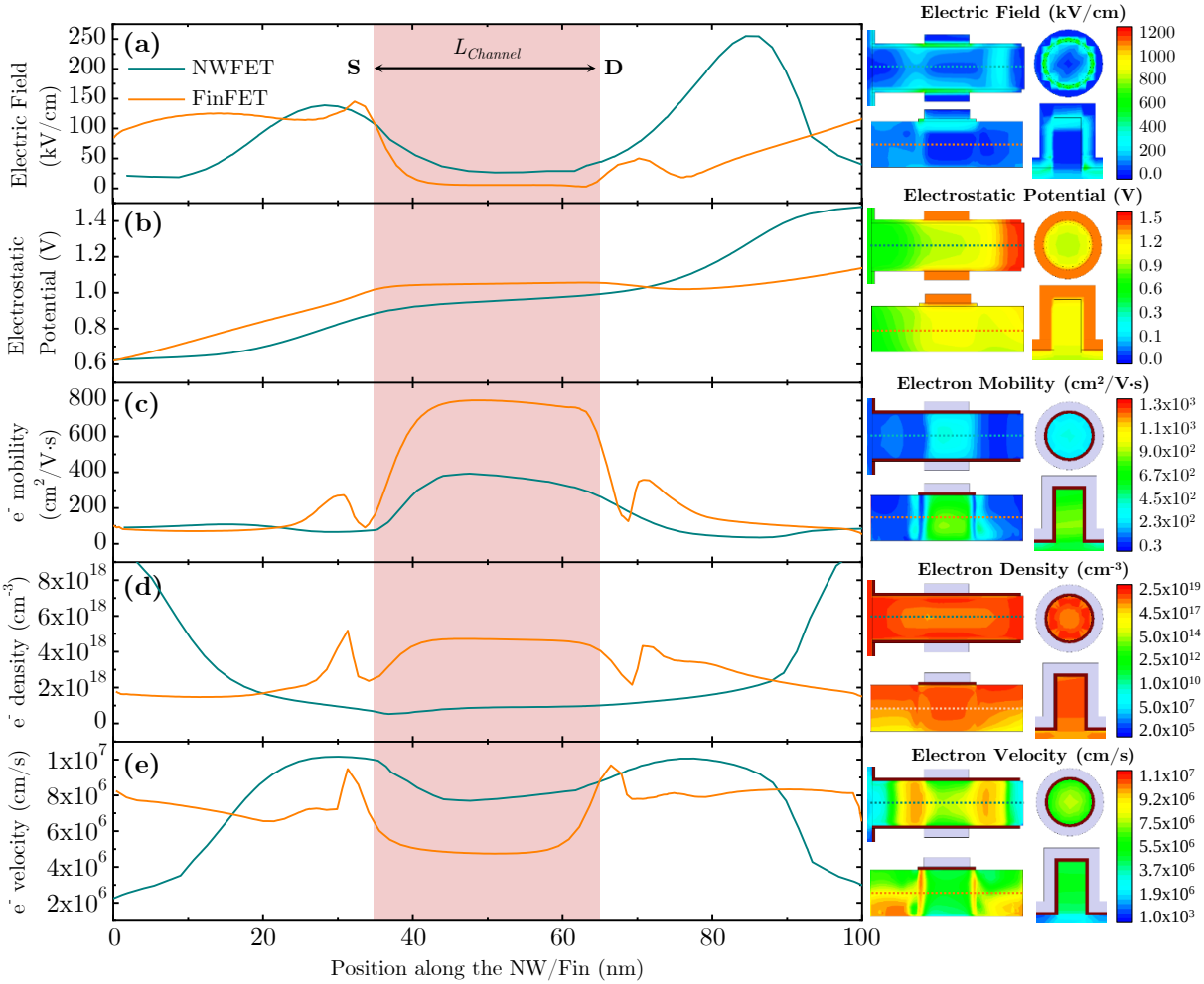


FIGURE 4.4: Profile along the NW/Fin for the electric field (a), electrostatic potential (b), electron mobility (c), density (d) and velocity (e) for NWFET and FinFET at nominal dimensions and 50 mV at drain bias.

different magnitude near source and drain. The peak near the drain is much more noticeable in the case of NWFET, in agreement with an increment in the electrostatic potential in this region (b). This electric field peak provides more acceleration to the electrons in the channel, enhancing thus saturation carrier velocity near the source. In terms of electron mobility, FinFET shows higher values in the channel region (c), a fact attributed to the random motion of the free electrons from the bulk substrate in vicinity of the channel. Similar aspect is observed in the electron density, with the additional point that in this case the NWFET inverts the FinFET tendency, with a significant reduction in electron density in the channel region and an increment near source and drain (d). Again, this is consistent with a difference in electron velocity for each device (e), as the increased gate control due to the GAA of the NWFET leads to a reduction of electron accumulation near the channel.

4.2.4 Subthreshold behaviour

The interest of good subthreshold behaviour for the integration of vertical NWFETs in hybrid circuits has been already mentioned. Here, simulations are performed in order to study the influence of device dimensions in the parameters that describe subthreshold operation: threshold voltage (V_{Th}), the gate-to-source bias required to switch on the transistor and extracted from the transconductance extrapolation method in the linear region [21]; subthreshold slope (SS), the parameter which describes the drain current behaviour when controlled by the gate terminal; and transconductance peak (G_{max}), the maximum slope of the current-voltage curve in linear regime. The dimensions whose affectation is studied are $L_{Channel}$ and $\varnothing_{NW}$. As in previous section, same simulations are performed for NWFET and FinFET models in order to enable their comparison.

Fig. 4.5 shows the V_{Th}, SS and G_{max} dependence on $\varnothing_{NW}$, H_{Fin} and $L_{Channel}$. It can be observed that in the NWFET case SS mostly stabilizes around tens of mV/dec; there is a region for larger channel lengths and small diameters where an almost ideal behaviour is obtained, with SS $\sim$ 60 mV/dec. As $L_{Channel}$ increases, SCEs are mitigated by improved gate controllability. On the other hand, when $\varnothing_{NW}$ increases, the electrostatic gate control degrades significantly. In the case of FinFET a different tendency is observed, with most favourable SS values for $H_{Fin}>$ 60 nm. In terms of threshold voltage, in the complete interval of dimensions investigated FinFET presents an average value of 80.9 mV, significantly higher than the 45.7 mV corresponding to NWFET. This is due to the fact that in the second case the maximum V_{Th} is very localized at $\varnothing_{NW} \sim$ 10 nm and larger $L_{Channel}$, while for FinFET a wider range of dimensions presents higher V_{Th}. Similar tendency is observed for both devices in the transconductance maximum, with slightly increased values in the case of NWFET.

It has been widely reported in the past that the use of high-κ materials such as HfO_2 as dielectric results in significant improvements in terms of output current and device performance [97]. Here, further investigations for NWFET are presented, implementing in the model the use of 2 nm of HfO_2 instead of SiO_2. Fig. 4.5.b and Fig. 4.5.c presents the resulting characteristics: the average SS is reduced a 13%, and similar tendencies are observed for V_{Th} and G_{max}, with higher values in both cases after implementing the use of HfO_2.

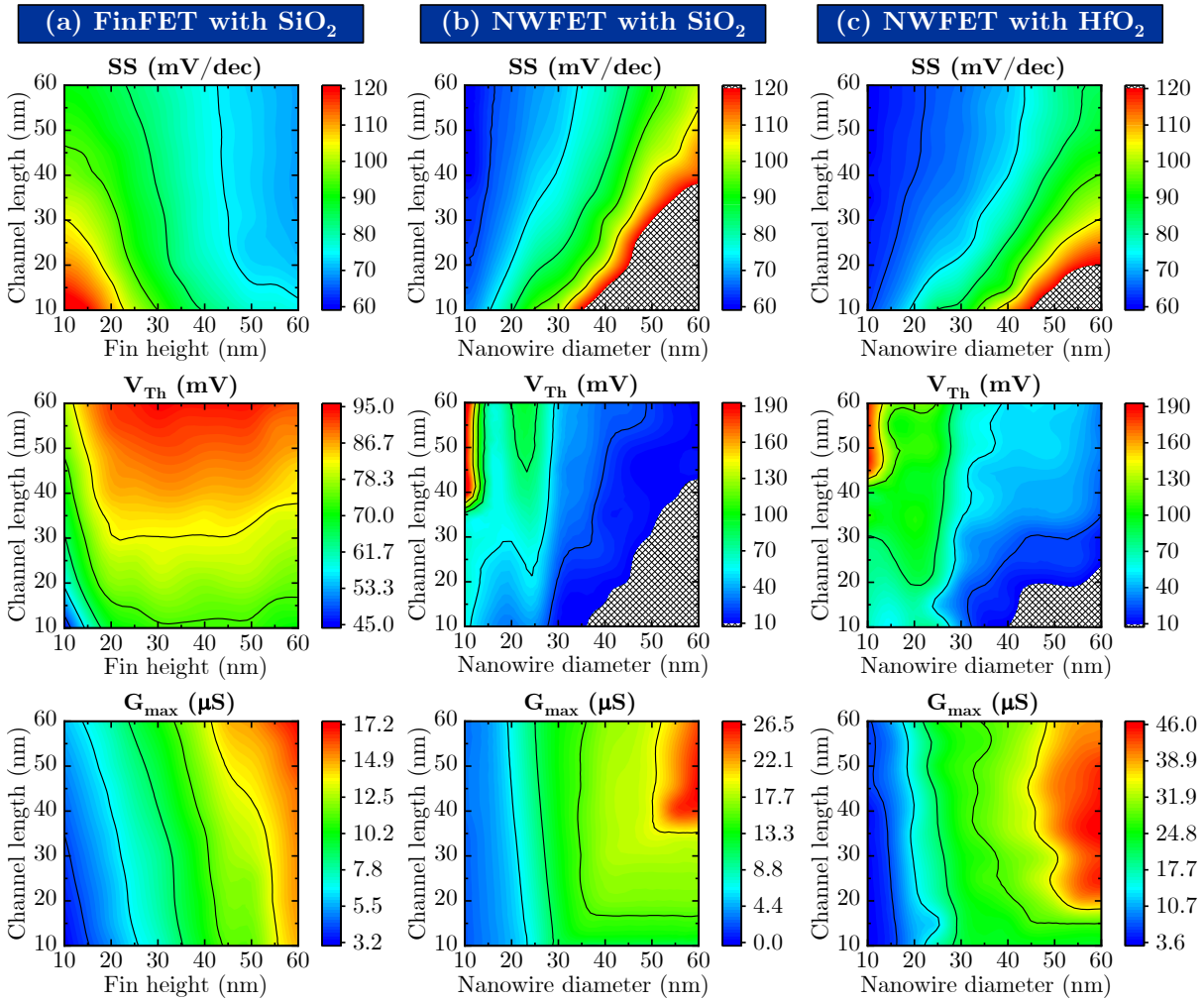


FIGURE 4.5: Subthreshold slope, threshold voltage and transconductance peak for FinFET with SiO_2 as dielectric (a) and NWFET with SiO_2 (b) and HfO_2 (c) as dielectric.

In summary, it can be concluded that NWFET outperforms FinFET in terms of subthreshold characteristics. This behaviour is ascribable to the increment of gate control over the channel and thus the reduction of SCEs [98]. Moreover, in the case of NWFET it is observed that for $L_{Channel} < 20$ nm the device characteristics are severely degraded, while good electrostatic integrity is achieved for $\varnothing_{NW} < 40$ nm. Hence, this interval of values is considered as most

optimal in terms of electrical performance, and thus baseline dimensions are fixed at 30 nm for both parameters. Finally, the benefits of using high-κ dielectrics as HfO_2 in vertical NWFET has been proved as well, with significant improvements in terms of subthreshold characteristics, and thus it has been implemented in the model hereinafter.

4.2.5 Variability tolerance

In order to analyse the variability tolerance for the NWFET, simulations with Synopsys HSPICE are performed. HSPICE is an optimizing analog circuit simulator used for electrical circuits modelling in steady-state, transient and frequency domains, as well as for circuit level performance by using Monte-Carlo worst-case analysis. In this case, it is used due to its accurate capabilities for Gaussian distribution iterability.

The Berkeley Spice Common Multi-gate FET (BSIM-CMG) compact model [99] can be calibrated into a vertical NWFET by directly modifying the parameters which define geometry, dimensions and orientation. Moreover, modifications of gate oxide thickness, SOI/bulk substrate, presence of self-heating effects or Vertical/Lateral NWs can be considered. In that way, same conditions and dimensions than in the model described in Fig. 4.1 are implemented.

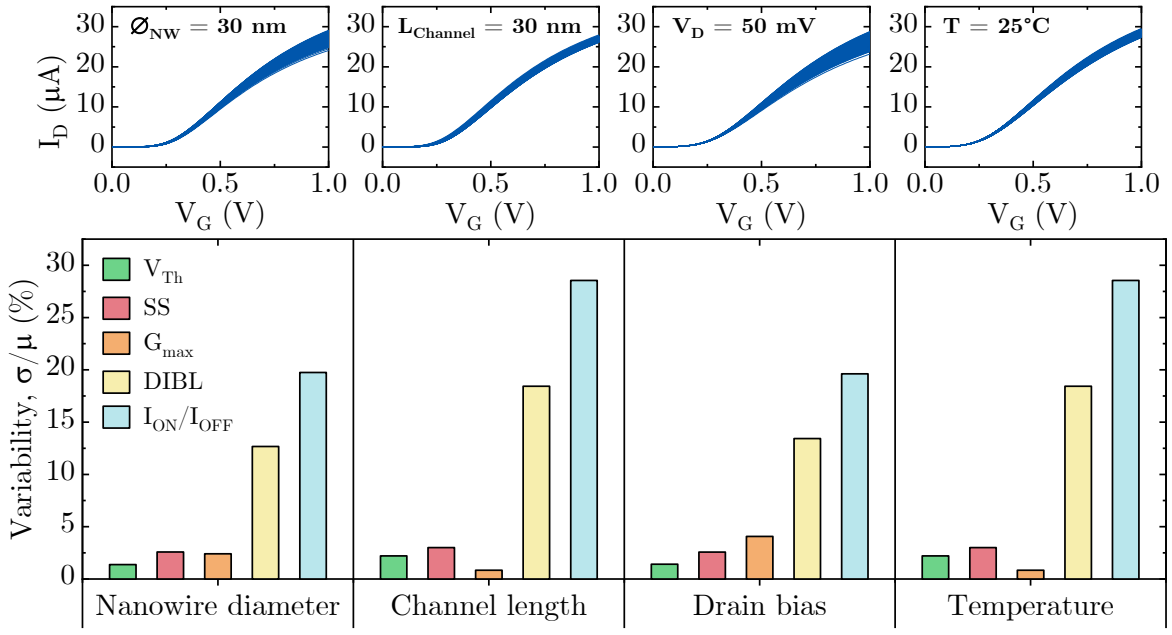


FIGURE 4.6: Variability level for each parameter when modifying $\varnothing_{NW}$, $L_{Channel}$, V_D and T, with detail of the associated current-voltage characteristics.

For the PVT analysis two scenarios are contemplated: first, influence of the environmental conditions of the parameters relevant for circuit performance (drain bias V_D and temperature T, fixed at 50 mV and 25°C, respectively); and secondly, the influence of the intrinsic characteristics of the device ($\varnothing_{NW}$ and $L_{Channel}$, fixed at 30 nm from baseline dimensions). In both cases, variability is evaluated from the ratio σ/μ expressed as a percentage, obtained from the standard deviation (σ) and the mean (μ) resulting from 10,000 Monte-Carlo iterations when introducing a 10% variation individually in each parameter.

The impact of these modifications on the following characteristics are investigated: V_{Th}, SS, G_{max}, Drain-induced barrier lowering (DIBL) and I_{ON}/I_{OFF} ratio. Results are presented in Fig. 4.6; it can be observed that the parameters that describe the subthreshold behaviour of the device (V_{Th}, SS, G_{max}) present values well below 5%. On the other hand, DIBL and I_{ON}/I_{OFF} ratio are more sensitive to variations, with values from 12% to 28%.

4.2.6 NWFET array configuration

The use of NWFET allows for a straightforward implementation in arrays, as it allows to place many devices with small footprint and incrementing the output current. Therefore, it is convenient to study the performance of this configuration in front of a device variability scenario. Nominal baseline dimensions and implantation values are implemented in several NWFETs, connected in parallel in array arrangements from 1x1 to 5x5, and the electrical performance is analysed in terms of SS and G_{max} and variability affectation.

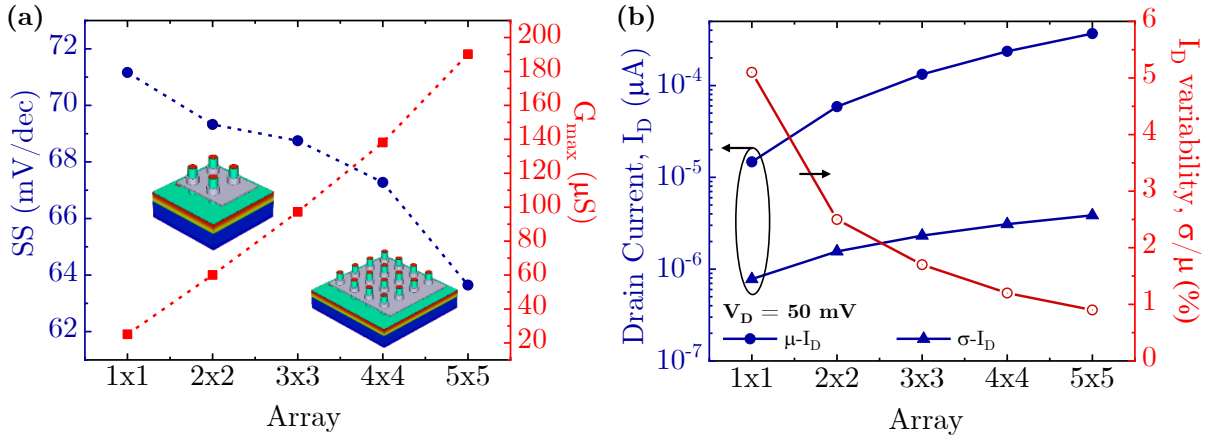


FIGURE 4.7: Resulting subthreshold slope and transconductance maximum for NWFET arrays from 1x1 to 5x5 (a). Impact on the output current of NWFET-based array configurations (b).

From Fig. 4.7.a, it can be observed that a tendency for lower SS and higher G_{max} is observed for larger arrays. From Fig. 4.7.b illustrates how the mean output current value ($\mu - I_D$) increases along with an overall reduction in variability up to x7 for the 5x5 array. This result comes from the fact that the I_D standard deviation (sigma $- I_D$) of an nxn array is only n-times bigger that of a single NWFET. This entails that, by using array configurations, a similar current level than for a single vNWFET can be obtained, but with a significant improvement in terms of variability mitigation.

4.3 Array arrangement in SET-FET hybrid circuit

The electrical performance of vertical NWFET has been presented in previous sections. First, in terms of subthreshold characteristics of standalone NWFET for its further integration in hybrid circuits, and afterwards the potential of array arrangement has been briefly introduced.

As already described in section B from Chapter 2, a SET compact model has been developed by FhG-IISB [100] in the framework of the IONS4SET project. This model has been used for the study of hybrid circuits through the combination of vertical SETs with standard MOSFET architectures, as described in section 3.3.1. Here, the objective is to analyse the performance of a fully vertically arranged SET-FET, and explore in this context the capabilities of array distributions. Simulations are performed considering the vertical SET model together with the BSIM-CMG calibrated in form of NWFET [99].

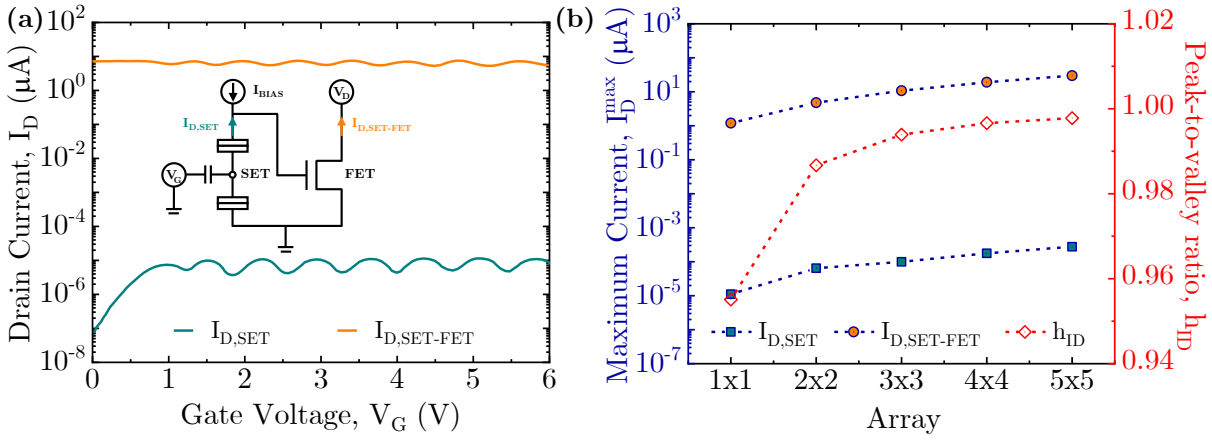


FIGURE 4.8: Current-voltage characteristics of the SET-FET hybrid circuit with single components (i.e. array 1x1), with the current level at the output of each element and inset of the corresponding circuit (a); maximum current and peak-to-valley ratio for the same circuit with array arrangement.

Fig. 4.8.a shows the schematic for the SET-FET hybrid circuit, with the corresponding current at the drain terminal of each element. The SET output current clearly shows Coulomb blockade oscillations; after the FET, these oscillations are still observable and in addition a larger current level is obtained. Hence, the amplification factor of the circuit is demonstrated.

The peak-to-valley current ratio (h_{ID}) between oscillations describes the SET contribution into the hybrid circuit current. Fig. 4.8.b indicates that a slight variation is observed when implementing array configurations. In other words, Coulomb blockade oscillations are not concealed in larger distributions. Moreover, an increment of more than one order of magnitude is observed at the output current of the overall SET-FET circuit.

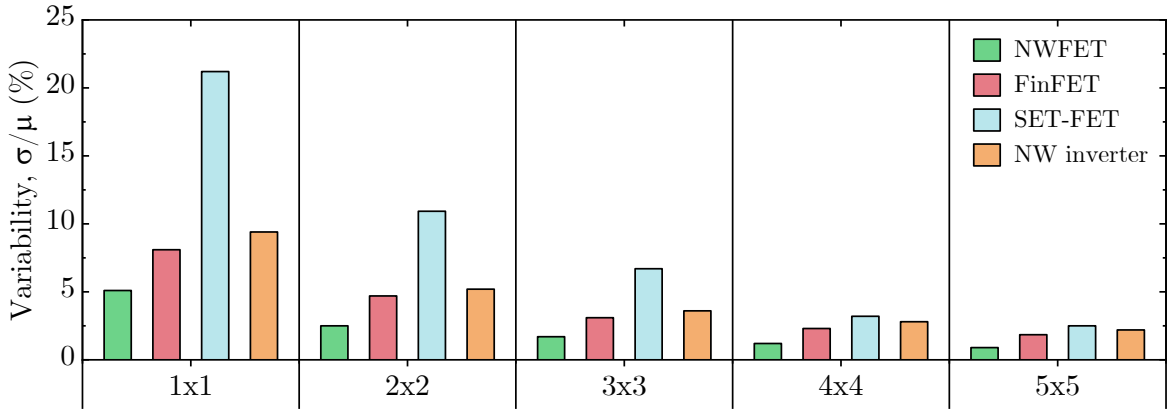


FIGURE 4.9: Device variability impact on different circuits with array arrangement: NWFET, FinFET, SET-FET and NW-based inverter.

Keeping reasonable levels of device variability is of significant concern at the nanoscale. For that reason, the level of variability mitigation obtained for different array configurations is studied here. Additionally, different architectures are investigated: NWFET and FinFET, from the BSIM-CMG model; the vertical SET-FET hybrid circuit described in this section; and finally the NW-based inverter device. Fig. 4.9 presents the results for all type of devices for arrays from 1x1 to 5x5. In terms of type of device, it results clear that SET-FET is the combination with higher variability, near 20% in the standalone configuration. Nevertheless, a remarkable level of mitigation is obtained for larger arrays, with all the configurations with values below 3% in the 5x5 array. Hence, it can be concluded that the use of matrix distributions can reduce significantly the impact of device variability on the electric performance.

4.4 Vertical NW-based inverter

A novel approach that can be derived from the concept of NWFET is the stacking of the different circuit components in the same vertical configuration. Similarly as the stacked c-Si/Si_2/a-Si described in Chapter 2, different layers can be deposited vertically. Among the benefits of this configuration, less area consumption and reducing the parasitic elements are worth mentioning. An example is the stacking of n- and p-type FETs in a single nanopillar or nanowire, forming the two main components of a NW-based inverter. Fig. 4.10.b illustrates the device, a nanopillar with $\varnothing_{NW} = 30$ nm and three GAA electrodes separated by insulating spacers.

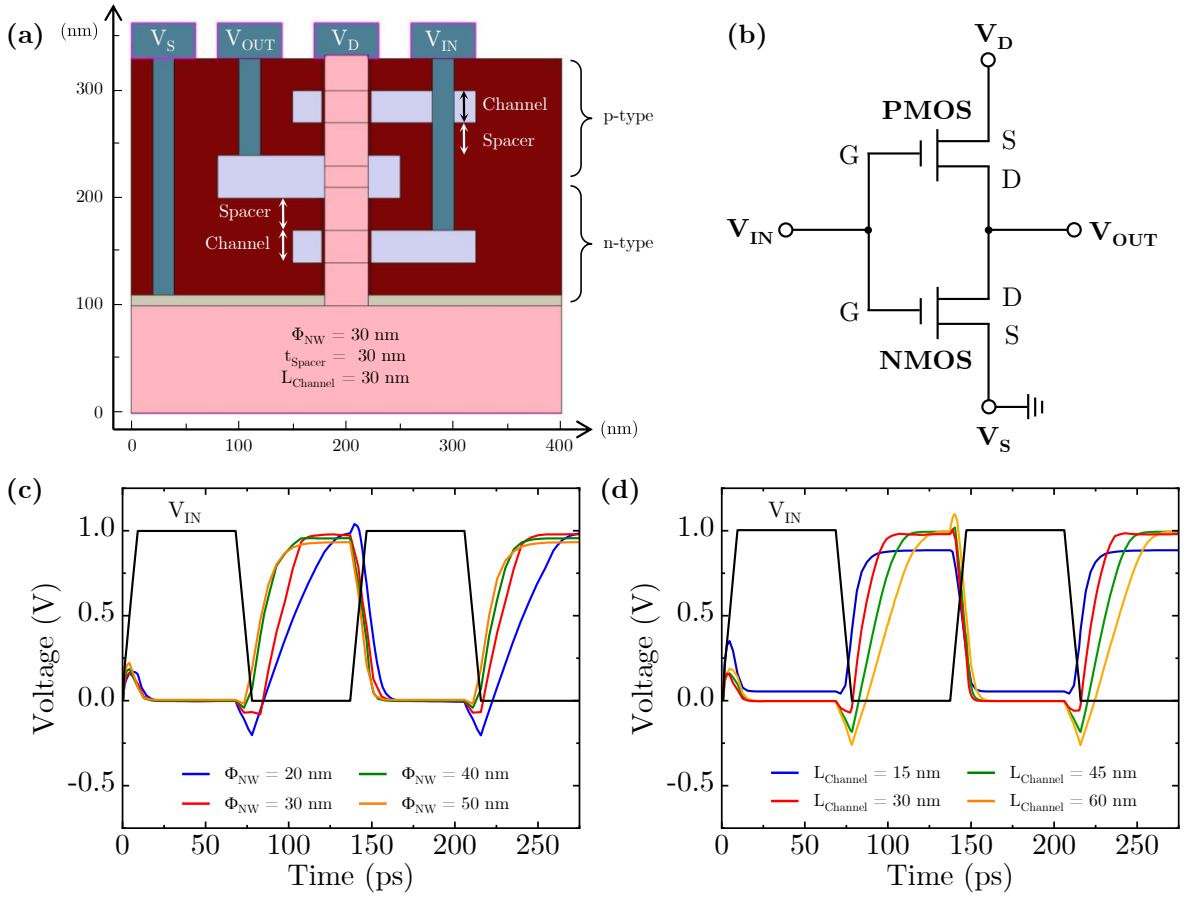


FIGURE 4.10: Model for the NW-based inverter (a), corresponding circuit (b) and voltage-time characteristics when modifying $\varnothing_{NW}$ (c) and $L_{Channel}$ (d).

Fig. 4.10.c shows the corresponding inverter behaviour for increasing $\varnothing_{NW}$; as it can be observed, dimensions near the $\varnothing_{NW} \sim 30$ nm are enough to reach the V_{IN} value of the square wave. Similarly, in Fig. 4.10.d the variation of $L_{Channel}$ is studied, with the best performance in the $L_{Channel} \leq 30$ interval.

4.5 Conclusions

The characteristics of standalone vertical NWFET have been investigated through 3D simulations. From comparison with FinFET, significant improvements in terms of electrostatic gate control and immunity against SCEs are observed. This observation is in agreement with the full GAA that characterizes NWFET with respect FinFET.

The electrical performance in subthreshold regime has been optimized according to the intrinsic device dimensions, NW diameter and channel length. Different tendencies are found for FinFET and NWFET, with a larger region near ideal SS values in the second case. Implementing HfO_2 as dielectric material in the NWFET model implies a further improvement on subthreshold behaviour. Moreover, variability analysis shows that subthreshold related parameters such as V_{Th}, SS and G_{max}, present tolerance to intrinsic and external variations below 5%.

Simulations of vertical NW-based devices in array distributions show larger output current and reduced variability. This is also observed for different electronic circuits, such as the NW-based inverter. In the particular case of the SET-FET hybrid circuit, the array arrangement involves a relevant increase in the output current with slight affectation on Coulomb blockade oscillations.

The capabilities of vertical configurations in other circuit architectures have been discussed. A particular example is the stacked NW-based inverter, with n- and p-type components arranged in a single vertical nanopillar. Its feasibility in terms of signal inversion has been proved.

In conclusion, the improvements in output current together with the benefits of higher integration due to its vertical configuration, indicate that NWFET has remarkable potential in terms of scalability and device integration. The suitability of vertical NWFET in array configurations to implement different integrated circuits has been analysed, resulting in higher output current and higher variability mitigation. This characteristic opens a wide range of possibilities for the implementation of alternative circuits with improved performance and efficiency.

Conclusions

The main objectives of the thesis, described in Scope and objectives, are briefly discussed here as the general conclusions of this work.

(i) **Development of an integration process for SET based on vertical nanopillars**
The integration process developed ensures the full contacting of a vertical nanopillar, with a gate-all-around located at the same level than the intermediate SiO_2 layer on the $Si/SiO_2/Si$ stack (Fig. 2.42) and the drain electrode on contact with the Si pillar cap (Fig. 2.44). Both metal layers are effectively separated by thin insulating spacers.
Although functional SET operation has not been proved, electrical phenomena ascribable to the presence of Si NDs have been observed (Fig. 2.51 and Fig. 2.52).
Several process steps required innovative approaches and have been subsequently optimized. For instance, the formation of thin intermetal layers by etch-back and annealing of HSQ layers has been necessary for contacting vertical nanostructures. Its suitability has been proved in terms of thickness control, planarization and electrical insulation capabilities (Fig. 2.17, Fig. 2.18 and Fig. 2.20, respectively).
The conformal TiN deposition as gate electrode required the accurate removal of TiN material from top of the pillar. A method based on the etch-back of the mask, leaving uncovered the pillar cap, has been designed. Its efficiency is demonstrated by AFM monitoring (Fig. 2.26) and EDX analysis (Fig. 2.27).

(ii) **Demonstrate the compatibility of CMOS processes with SET integration**
The thermal budget for FET fabrication was limited by the presence of Si NDs on the nanopillars. For this reason, two standard processes were tested and optimized: polysilicon doping (Fig. 3.24) and gate oxide formation (Fig. 3.25).
The compatibility of SET with CMOS processes has been validated by TEM characterization. Tests proved that the proposed methods were suitable for pillar protection during wafer reshaping (Fig. 3.19) and FET fabrication (Fig. 3.20).

Afterwards, the monolithic fabrication of FET and SET is proved. On one hand, FETs operate at optimum conditions: low threshold voltage, subthreshold swing around 73.3 mV/dec, low dispersion and good yield (Fig. 3.48, Fig. 3.50 and Fig. 3.44, respectively). On the other hand, the integrity of the nanopillars is validated by AFM (Fig. 3.39) and the embedded Si NDs are still observable by TEM analysis (Fig. 3.37).

(iii) **Analysis of the routes for the integration of a hybrid SET-FET circuit**
The monolithic fabrication of FETs and SETs is a significant improvement towards the hybrid SET-FET circuit. The simulations performed (Fig. 3.14) validate the feasibility of combining SETs based on vertical nanopillars with planar FETs fabricated under the described conditions.

(iv) **Explore the suitability of vertical transistors in terms of simulations**
Vertically arranged nanowires are suitable candidates for the integration of gate-all-around FETs. Simulations report an optimum interval of dimensions for channel length and nanowire diameter (Fig. 4.5). The potential of array arrangement in vertical configurations is complemented with significant improvements in terms of variability tolerance (Fig. 4.9).

In summary, the functionalities of standard CMOS technology have been extended via integration of new processes, establishing the groundwork towards the safe and reliable integration of vertical SETs in industrial CMOS technologies. First, it has been demonstrated in terms of structural characterization from fully contacted SET, and afterwards from the electrical measurements of the SET-compatible FETs. This two facts, along with the potential of vertical transistors in current semiconductor industry, represent a compelling drive towards new generation of nanoelectronic devices.

Appendix A

Ion beam irradiation for Si nanodots formation

Ion beam irradiation of pillars with thin SiO_2 embedded between two silicon layers is the first step for the creation of Si NDs inside the oxide layer. Although ion beam mixing has already been used in the past for device fabrication [101], [102], it still requires specific predictive simulations in order to build the groundwork towards SET operation. All simulations here presented were developed by HZDR in the framework of the IONS4SET project, and are described in more detail in the corresponding publications [103], [104].

Self-assembly can be observed during phase separation of metastable materials. For instance, metastable SiO_x decays under thermal activation into Si and SiO_2. Given a flat interface between Si and SiO_x, phase separation can be controlled [105]: all the Si excess in a small SiO_x layer parallel to the interface condenses onto the Si, forming thin regions denuded of Si excess. If the oxide is 10 nm thick or thicker, narrow layers with Si NDs are formed parallel to the upper and to the lower interface, at self-aligned distances of about 2 nm. These nanoclusters can be charged via direct, quantum mechanical tunnelling of electrons, thus producing the SET on and off states. If the phase separation is geometrically constraint in one dimension, such as an interface, self-assembly results in a 2D structure, a layer of nanoclusters. If phase separation is geometrically constraint in three dimensions, then theory predicts that a finite volume of Si nanocluster is formed. In this case, the size of the volume is equal or smaller than Brailsford's diffusional screening length, $\sim 1/\sqrt{4\pi nR}$, where n is the density of nanoclusters and R the their mean radius [106]. As both parameters are time-dependent during phase separation, the diffusional screening length is also time-dependent.

In order to predict efficiently Si NDs formation, ion beam implantation and of ion beam mixing have to be described with a high spatial resolution, since the total thickness of the SiO_2 layer is of a few nanometers in the targeted device. For that reason, molecular dynamics (MD) is the used method for simulating ion implantation. It includes modification of interatomic potential at small interatomic distances; as MD simulations are time consuming, calculations are improved by implementing existing well-tested MD codes with accelerating algorithms.

Taking the results of ion implantation simulations as initial conditions, now the formation of Si NDs in SiO_2 layers by phase separation is studied. The kinetic Monte-Carlo (kMC) allows the same atomic spatial resolution than MD, but it is much more time efficient; therefore, it is the method used for the modelling of thermal treatment on ion implanted samples. Moreover, the kMC simulations performed consider as well 3D architectures and boundary conditions, besides the already mentioned phase formation and dot self-assembly. Another motivation for the development of these simulations, is the investigation and optimization of the technological conditions required for the NDs formation with specified sizes and positions. With that aim, time and temperature dependence of phase separation and Si dot self-assembly will be studied for a wide variety of variables, such as layer thickness, pillar diameters and ion energies and fluence.

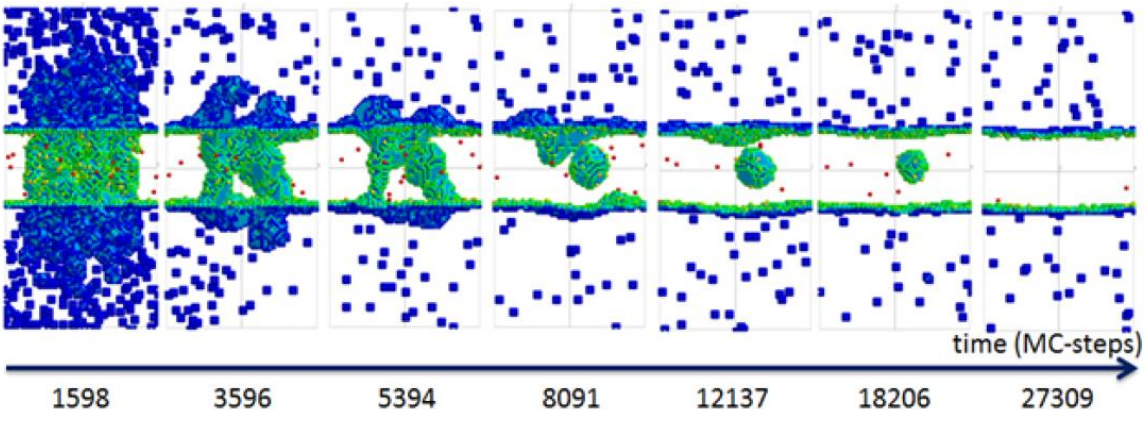


FIGURE A.1: Atomistic 3D kinetic Monte Carlo simulation of phase separation in an ion-beam-mixed SiO_2 layer embedded between Si.

Fig. A.1 shows the 3D kMC simulations of phase separation at different time-steps for a SiO_2 layer embedded between silicon. The figure depicts the excess of Si atoms in the oxide layer in green, and the O atoms in silicon as blue, while other Si and O atoms are transparent. As observed, as MC time-steps are increasing, the excess of Si atoms from the oxide layer move towards the Si/SiO_2 interfaces. After ~10,000 MC time-steps, a Si cluster is formed; after ~15,000 MC time-steps, the Si/SiO_2 interfaces have completely reconstructed and the Si dot

has an ideal size of 3 nm; for >27,000 MC time-steps, the Si ND is already dissolved. Therefore, the self-assembly of a single Si ND is determined by a finite volume of metastable SiO_x, and after formation it can be compromised by high-temperature processes.

The influence of pillar diameter in the phase separation and consequent Si NDs formation is presented in Fig. A.2. The selected examples displayed are subjected to significant statistical variations. From a large number of repeated kMC iterations with different random start conditions, probabilities of the formation of a single ND have been derived as function of the number of kMC steps. At increasing diameter, the maximum probability decreases to obtain a single ND, which only occurs for high kMC steps. Simulation results defining the relation between pillar diameter and number of formed Si NDs will be verified by comparison with experimental results in next sections. However, it is interesting to note that the fabrication of single Si ND in the oxide layer is not mandatory for SET operation. A pillar diameter of 12 nm could be sufficient, despite the multiple nanocluster formation. The reason is that, given several NDs in the embedded SiO_2 layer, a conductive filament through the oxide is formed in the specific ND with the lowest tunnelling barrier.

An additional result of the kMC simulations of Si ND formation during phase decomposition is the edge rounding of the top and bottom parts of the nanopillar. This edge rounding is beneficial for a sufficient reach-through of the GAA field to the QD region, which allows SET operation at reasonably low gate voltages.

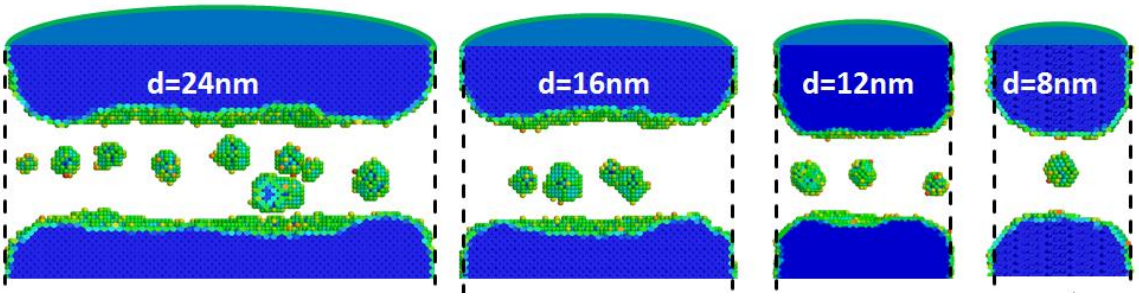


FIGURE A.2: Evolution of nanocluster morphology in pillars of different diameter predicted by kinetic Monte-Carlo simulations.

Appendix B

SET device simulator

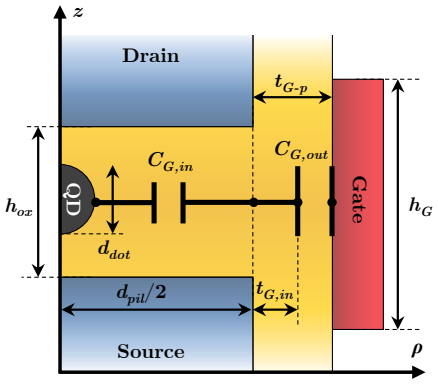
A three dimensional device simulator is necessary in order to provide information about the current-voltage characteristics of the targeted SET. The model must include the specific architecture of a vertical nanopillar with Si ND acting as QD, with the possibility of modifying its nominal dimensions as support for its further experimental fabrication. Given the absence of commercial solution for 3D SET device simulation, partners from FhG-IISB developed several consecutive models.

In a first version [81], electrostatics and bound quantum dot energy states were provided by the commercial 3D quantum simulator nextnano++, while the tunnelling current through the QD was calculated by Schrödinger-Poisson solver [107] implemented in a self-written post-processing software. In that way, a wide range of geometries could be simulated and evaluated, including dot diameter, tunnelling oxide thickness, pillar diameter, gate oxide thickness, dot doping and dot position. Parasitic leakage currents and capacitances between the SET electrodes were simulated as well with established tools like Sentaurus Device of Synopsys [108].

Next updates in the code improved stability of the system. For instance, the work was further extended in order to account for confinement effects in source/drain regions of the device. A compact model was developed based on previous works [44], allowing the analysis of circuit properties as function of geometry variation. An additional interest of this model was enabling the simulation of multiple SETs and their combination with other devices, which was necessary for the development and validation of the SET-FET hybrid circuit demonstrator [96].

The most recent SET compact model [109] included several significant improvements with respect its predecessors. In orthodox theory, the calculation of tunnelling current relies on an empirical tunnelling resistance for each junction, while electrostatics is described by the capacitance parameters. In this case, tunnelling currents are calculated using a master equation

approach with rates obtained via the transfer Hamiltonian formalism proposed by Bardeen [110]. Regarding the capacitance parameters of the circuit, they are redefined in detail according to the device geometry and characteristics. Fig. B.1 illustrates a close view of the embedded oxide region, with dimensions and contribution of gate-to-QD capacitance.



Symbol	Parameter	Nominal
d_{dot}	QD diameter	3.2 nm
d_{pil}	Pillar diameter	10 nm
h_{ox}	Pillar oxide thickness	5.6 nm
$t_{G\text{-}p}$	Gate-pillar oxide thickness	3 nm
h_G	Gate contact height	10 nm

FIGURE B.1: Schematic of the embedded oxide region and gate-to-QD capacitance contributions, with nominal values for the device dimensions.

An initial approximation considered a total QD capacitance as in a semiconductor ND in an infinite matrix of SiO_2. Nevertheless, comparison to numerical simulations shows that it is affected by the electrodes in vicinity of the dot. This geometry dependence is included in the new definition. The gate-to-QD capacitance C_{G-QD} describes the electrostatic coupling between the gate contact and the QD. Its analytic approximation is separated into a contribution within the nanopillar, described by $C_{G,in}$, and a contribution outside the nanopillar, denoted as $C_{G,out}$. Ideally one would simply connect both contributions in series to obtain the total capacitance. However, there are two further issues to be considered. First, the electrostatic influence of the source/drain contacts will extend somewhat over the pillar diameter. An empirical way to deal with this fact is to define a boundary between the inner and outer capacitance contributions, which is not at the pillar boundary but an additional distance t_{G-p} further towards the gate. And second, comparison with numerical simulation shows that the effective height of the outer capacitor is not simply given by h_{ox} as assumed beforehand, but it is influenced by pillar diameter and QD size as well.

Through incorporing all these considerations into the HSPICE simulator benchmark [111], an analytic SET model for circuit simulation is available [100]. Specific device characteristics for a SET with a semiconducting QD like the gate voltage threshold for the onset of current oscillations are reproduced. As in previous versions, device geometry and material properties enter the model directly as parameters. Thus, this model enables the investigation of circuits

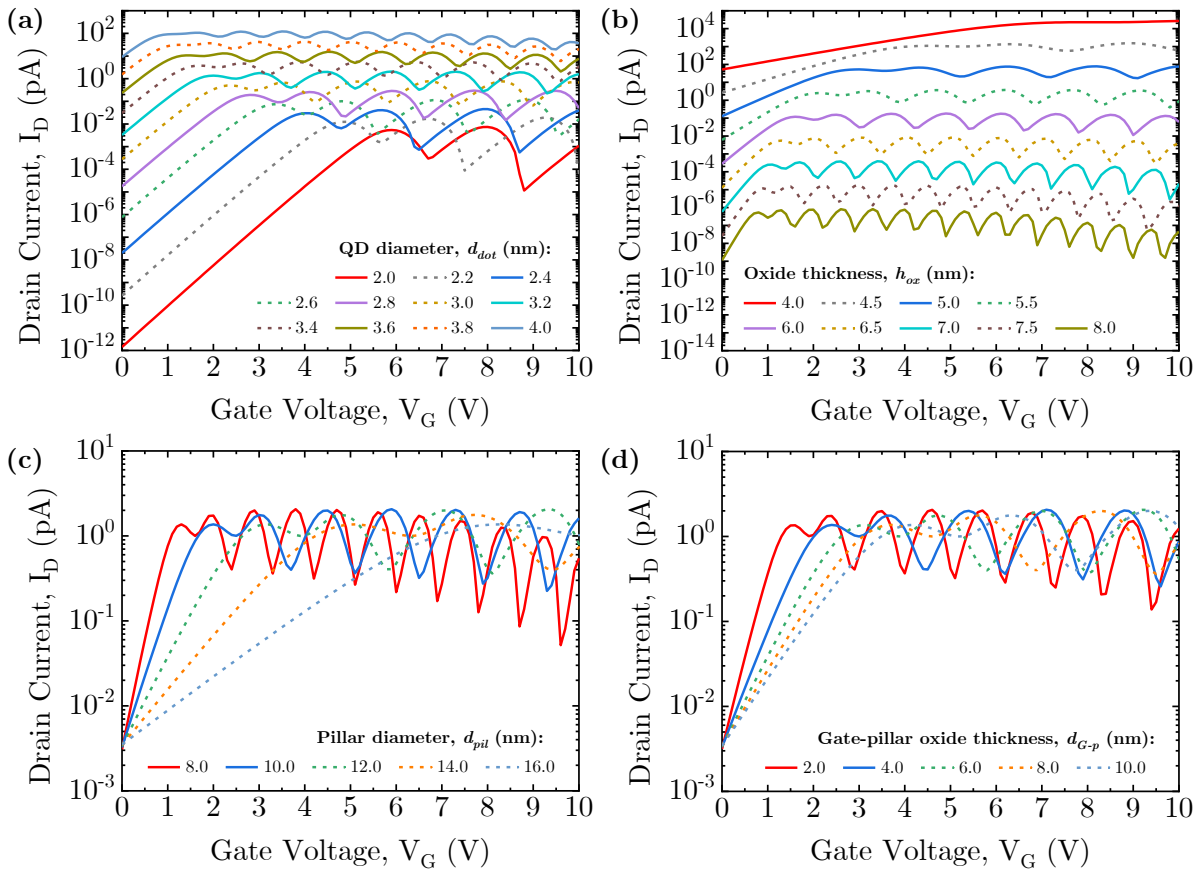


FIGURE B.2: Room temperature current-voltage characteristics of the SET model device for different variable modifications with respect nominal dimensions: while modifying QD diameter (a), oxide thickness (b), pillar diameter (c) and gate-pillar oxide thickness (c).

and application scenarios for specific SET technologies in dependence on geometry and material variations.

Fig. B.2 presents the resulting current-voltage characteristics for different geometry modifications. In these simulations, nominal dimensions as stated in Fig. B.1 are kept, while d_{dot}, h_{ox}, d_{pil} and d_{G-p} are individually modified. As observed, for $d_{dot} < 3$ nm Coulomb oscillations are only appreciable at high voltages. For that reason, QD around 3 nm are the most suitable for SET operation at room temperature. For obtaining measurably large currents, tunnel junctions between QD and source/drain should not exceed 2 nm. This provides a range of interest for the oxide thickness; note that tunnel junction distances are a relation between h_{ox} and d_{dot}. The pillar diameter d_{pil} should be as small as possible in order to allow good electrostatic control of the QD potential. Nevertheless, the fabrication of sub-10 nm pillars is compromised by manufacturing issues. On the other hand, for diameters larger than 16 nm the observation of Coulomb oscillations are strongly flattened. Similarly, a gate-pillar oxide thickness around

3 nm is found to be adequate for SET operation; otherwise, for larger values observation of oscillations is attenuated.

There are several effects not included in the model that might affect the device characteristics. Examples are confinement effects in the source and drain contacts, scattering by interface traps at the Si/SiO_2 boundaries, or depletion in low-doped source/drain contacts. However, only experiments on SETs with systematic variations in geometry and doping can give a solid answer on the question of what contributions would be really needed for describing real devices.

Appendix C

SET integration - Experimental conditions

Next table summarizes all the process steps, experimental conditions, target/nominal values and equipments that are part of the SET integration. Note that this version includes all the process already optimized as described in Chapter 2.

Process step		Conditions	Target	Equipment/Area
0.1	Wafer processed at CEA-Leti	Sub-30 nm c-Si/SiO_2/a-Si Pillar patterning by EBDW and RIE through SiARC/SOC hard mask	-	CEA-Leti
0.2	Wafer oxidation at FhG-IISB	Different RTA conditions and plasma oxidation + HF treatment for sub-10 nm pillar diameters	-	FhG-IISB
0.3	Wafer cleaving into chips at IMB-CNM	Wafer cleaving into chips 15 mm x 15 mm for SET integration processing	-	IMB-CNM
1.1	Initial substrate oxide	Measurement of the SiO_2 thickness present on the substrate	5–7 nm	Rudolph Auto EL IV
1.2	Diluted HF etching	Wet etching in 0.1% HF (5 ml H_2O + 100 µl HF 5%)	90s	Wet bench
1.3	Final substrate oxide	Measurement of the SiO_2 thickness present on the substrate	3–5 nm	Rudolph Auto EL IV
2.1	1st HSQ deposition	Thick layer HSQ 6% deposition (10s at 1000 rpm + 30s at 6000 rpm) + 4 min at 80°C	160–170 nm	Spinner Laurell WS-400B-6NPP
2.2	1st HSQ back etching	HSQ back-etching in 0.025% HF (20 ml H_2O + 100 µl HF 5% + 400 µl BZK)	110–120s	Wet bench
2.3	1st HSQ annealing	HSQ annealing at 800°C for 1h	30–38 nm	HOBERSAL CVD
3.1	Argon plasma	Argon milling for top oxide etching at 100 W	40–60s	KENOSISTEC KS800H
3.2	TiN deposition	TiN sputtering (10 sccm Ar, 10 sccm N_2, 3 µbar and 100 W)	9 nm	KENOSISTEC KS800H
4.1	L#1 resist deposition	Negative resist HSQ 2% deposition (60s at 6000 rpm + 4 min at 80°C)	20–22 nm	Spinner Laurell WS-400B-6NPP
4.2	L#1 exposure	EBL exposure (energy 20 kV, aperture 20 µm, beam current ~150 pA, base dose 110 µC/cm^2, dose factor 5)	-	RAITH 150 TWO
4.3	L#1 resist development	Immersion in diluted TMAH (3%, 70s) + water flow (15s)	70s	Wet bench
4.4	Resist soft-bake	Soft-bake at 180°C for 120s	120s	Hot plate
5.1	HSQ mask reduction	Wet etching in 0.025% HF (20 ml H_2O + 100 µl HF 5%)	55s	Wet bench
5.2	Gate region definition	TiN wet etching in ammonia-peroxide mixture (APM, 100 ml H_2O + 40 ml H_2O_2 + 10 ml NH_4OH)	120s	Wet bench
6.1	2nd HSQ deposition	Thick layer HSQ 6% deposition (10s at 1000 rpm + 30s at 6000 rpm) + 4 min at 80°C	160–170 nm	Spinner Laurell WS-400B-6NPP
6.2	2nd HSQ back etching	HSQ back-etching in 0.025% HF (20 ml H_2O + 100 µl HF 5% + 400 µl BZK)	155s	Wet bench
6.3	2nd HSQ annealing	HSQ annealing at 400°C for 1h	70 nm	HOBERSAL CVD
7.1	L#2 resist deposition	Positive resist deposition, EL6 (~200 nm, 60s at 1500 rpm) & PMMA A2 (~70 nm, 60s at 1500 rpm) + 1 min at 180°C each	270 nm	Spinner Laurell WS-400B-6NPP
7.2	L#2 exposure	EBL exposure (energy 10 kV, aperture 30 µm, beam current ~220 pA, base dose 110 µC/cm^2, dose factor 1)	-	RAITH 150 TWO
7.3	L#2 resist development	Immersion in MIBK:IPA 1:3 (40s) + IPA (20s)	60s	Fume hood
7.4	Wet etching	Wet etching in 0.025% HF (20 ml H_2O + 100 µl HF 5%)	20–120s	Wet bench
7.5	Argon plasma	Argon plasma with etch-rate of 0.4–0.5 nm/min	120s	UNIVEX 450 Leybold
7.6	Ni/Au deposition	30 nm Ni and 20 nm Au deposition by e-beam evaporation	50 nm	UNIVEX 450 Leybold
7.7	Lift-off	Bath in acetone and ultrasounds (5 min at 50°C)	5 min	Fume hood and sonicator
8.	Si_3N_4 deposition	25 nm Si_3N_4 deposition by PECVD at 350°C	20–25 nm	OXFORD Plasmalab 800
9.1	L#3 resist deposition	Positive resist deposition, EL6 (~200 nm, 60s at 1500 rpm) & PMMA A2 (~70 nm, 60s at 1500 rpm) + 1 min at 180°C each	270 nm	Spinner Laurell WS-400B-6NPP
9.2	L#3 exposure	EBL exposure (energy 10 kV, aperture 30 µm, beam current ~220 pA, base dose 110 µC/cm^2, dose factor 1)	-	RAITH 150 TWO
9.3	L#3 resist development	Immersion in MIBK:IPA 1:3 (40s) + IPA (20s)	60s	Fume hood
10.1	RIE	Si_3N_4 etching by RIE (C_4F_8 30 sccm, CH_4 20 sccm, He 20 sccm at 1200 W + 50 W and 0°C)	37s	ALCATEL AMS 110 DE
10.2	Wet etching	Wet etching in 0.1% HF (5 ml H_2O + 100 µl HF 5%)	90–120s	Wet bench
10.3	PMMA removal	Oxygen plasma (600 sccm O_2 at 500 W)	10 min	TEPLA GIGABATCH 360M
11.1	L#4 resist deposition	Positive resist deposition, EL6 (~200 nm, 60s at 1500 rpm) & PMMA A2 (~70 nm, 60s at 1500 rpm) + 1 min at 180°C each	270 nm	Spinner Laurell WS-400B-6NPP
11.2	L#4 exposure	EBL exposure (energy 10 kV, aperture 30 µm, beam current ~220 pA, base dose 110 µC/cm^2, dose factor 1)	-	RAITH 150 TWO
11.3	L#4 resist development	Immersion in MIBK:IPA (40s) + IPA (20s)	60s	Fume hood
12.1	Argon plasma	Argon plasma with etch-rate of 0.4–0.5 nm/min	120s	UNIVEX 450 Leybold
12.2	Ti/Au deposition	5 nm Ti and 65 nm Au deposition by e-beam evaporation	70 nm	UNIVEX 450 Leybold
12.3	Lift-off	Bath in acetone and ultrasounds (5 min at 50°C)	5 min	Fume hood and sonicator

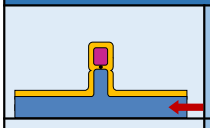
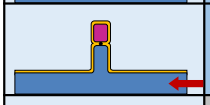
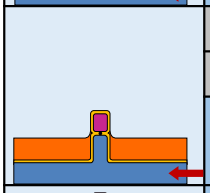
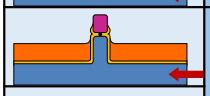
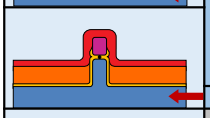
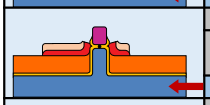
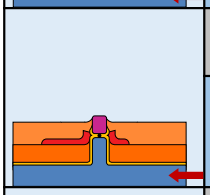
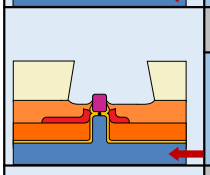
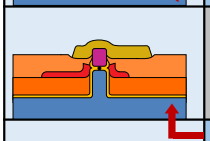
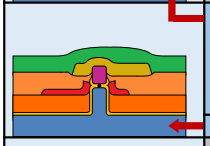
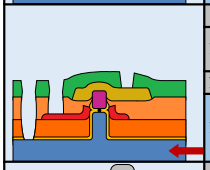
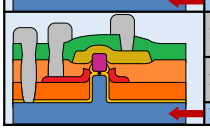
FIGURE C.1: Nominal conditions for the SET integration process.

Appendix D

SET integration - Process simulator

This appendix introduces the process simulator developed as support for the SET integration. All the steps described in Appendix C are considered. Deposition and etch-rates are experimentally measured and implemented in the simulator, altogether with nominal baseline dimensions for the patterned $Si/SiO_2/Si$ pillars.

The simulator differentiates four type of parameters: assumed values, corresponding to those dimensions that cannot be systematically measured (e.g. pillar dimensions, native oxide grown around the pillar); measured ones, those that can be experimentally verified (e.g. layer thickness); simulated values, approximation for the resulting characteristics (e.g. resulting thickness after a certain etching); and the process conditions that guide the integration towards the fully contacted device. The simulation is self-corrected through the implementation of measured values as input variables; in that way, the optimum process conditions are specifically defined for each sample according to its previous measurements.

Process step			Conditions	Nominal values		Samples in process					
Step		Description		Time (s)	Default (nm)	S1	S2	S3	S4	S5	S6
	0	Top pillar height			25.00	25.00	25.00	25.00	25.00	25.00	25.00
		Embedded oxide thickness			4.00	4.00	4.00	4.00	4.00	4.00	4.00
		Bottom pillar height			40.00	40.00	40.00	40.00	40.00	40.00	40.00
		Initial top plasma oxide on pillar			5.00	5.00	5.00	5.00	5.00	5.00	5.00
		Initial plasma oxide on substrate			6.50	6.90	6.50	7.10	7.00	6.70	6.50
	1.1	Initial diluted HF etching	0.1%	90		90.00	90.00	90.00	90.00	90.00	90.00
		Final top plasma oxide on pillar			1.01	1.01	1.01	1.01	1.01	1.01	1.01
		Final plasma oxide on substrate			2.51	2.91	2.51	3.11	3.01	2.71	2.51
		Final plasma oxide on substrate			2.00	2.30	2.40	2.70	2.70	2.70	2.90
	2.1	HSQ thickness after spin-coating			170.00	169.20	159.10	167.20	171.40	168.20	167.20
		Diluted HF for back-etching	0.025%	120		110.00	110.00	110.00	120.00	120.00	120.00
	2.2	HSQ thickness after etched-back			40.16	50.18	40.08	48.18	41.56	38.36	37.36
		HSQ thickness after etched-back			42.00	45.50	37.20	49.10	49.50	53.20	51.70
	2.3	HSQ thickness after annealing at 800°C			31.92	35.42	27.12	39.02	39.42	43.12	41.62
		HSQ thickness after annealing at 800°C			39.20	37.30	30.50	40.80	41.70	41.70	36.30
	3.1	Top-pillar HSQ thickness			1.50	1.50	1.50	1.50	1.50	1.50	1.50
		Argon milling time	100 W	40		30.00	30.00	40.00	40.00	40.00	40.00
		Top-pillar HSQ thickness			0.00	0.00	0.00	0.00	0.00	0.00	0.00
		Top plasma oxide on pillar			0.00	0.00	0.00	0.00	0.00	0.00	0.00
		Top pillar height			23.99	24.99	24.99	23.99	23.99	23.99	23.99
		HSQ thickness after argon plasma			36.10	35.80	29.10	36.80	37.80	38.67	33.27
		HSQ thickness after argon plasma			36.17	35.03	28.23	37.77	38.67	38.67	33.27
	3.2	TiN thickness			9.50	9.50	9.50	9.50	9.50	9.50	9.50
	4.4	HSQ mask thickness after EBL			22.00	22.00	22.00	22.00	22.00	22.00	22.00
	5.1	Diluted HF for HSQ mask etching	0.025%	55		55.00	55.00	55.00	55.00	55.00	65.00
		HSQ mask thickness after etch-back			14.32	14.32	14.32	14.32	14.32	14.32	12.92
	5.2	APM for TiN etching	1:4:20 RT	120		120.00	120.00	120.00	150.00	120.00	120.00
	5.3	Diluted HF for HSQ mask removal	0.025%	0		0.00	0.00	0.00	0.00	0.00	0.00
		Remaining HSQ mask thickness			14.32	14.32	14.32	14.32	14.32	14.32	12.92
		TiN stand-up height			7.00	7.00	7.00	7.00	4.00	4.00	7.00
	6.3	First + second HSQ after etch-back and annealing			65.00	73.70	61.10	68.90	71.10	66.10	65.80
		Top-pillar first + second HSQ thickness			2.00	2.00	2.00	2.00	2.00	2.00	2.00
		Second HSQ step over TiN electrode			4.00	2.00	2.00	4.00	4.00	4.00	4.00
	7.3	EBL for drain electrode									
		Native oxide on pillar			1.00	1.00	1.00	1.00	1.00	1.00	1.00
	7.4	Additional diluted HF	0.025%	60		120.00	20.00	50.00	50.00	50.00	50.00
		Top-pillar first + second HSQ thickness after etching			0.00	0.00	0.67	0.00	0.00	0.00	0.00
		Native oxide on pillar after etching			0.50	-0.50	1.00	0.67	0.67	0.67	0.67
		First + second HSQ after etching			65.00	67.70	61.77	69.57	71.77	66.77	66.47
	7.5	Argon milling before metallization	Glow discharge	120		120.00	120.00	120.00	120.00	120.00	120.00
		Top-pillar first + second HSQ thickness after milling			0.00	0.00	0.00	0.00	0.00	0.00	0.00
		Native oxide on pillar after milling			0.00	0.00	0.33	0.00	0.00	0.00	0.00
		First + second HSQ after milling			63.00	65.70	59.77	67.57	69.77	64.77	64.47
	7.6	Ni/Au metallization			50.00	50.00	50.00	50.00	50.00	50.00	50.00
		Ni/Au electrode sinking respect top of pillar			4.99	3.29	9.56	0.43	0.00	3.23	3.53
		TiN-Ni separation on complete stack			17.40	20.40	21.17	21.27	22.47	16.60	21.70
		TiN-Ni separation on pillar			10.40	13.40	14.17	14.27	16.69	12.60	14.70
	8	PECVD passivation			18.00	18.00	18.00	18.00	18.00	18.00	18.00
	9.3	EBL for contact windows									
	10.1	RIE for silicon nitride etching	1200W + 50W. 0°C	37		37.00	37.00	37.00	37.00	37.00	37.00
	10.2	Diluted HF for HSQ etching	0.1%	30		30.00	30.00	30.00	30.00	30.00	30.00
	10.3	Depth for Source contact window			83.00	91.70	79.10	86.90	89.10	84.10	83.80
		Depth for Drain contact window			18.00	18.00	18.00	18.00	18.00	18.00	18.00
		Depth for Gate contact window			41.40	48.40	42.50	44.60	45.80	39.93	45.03
	11.3	EBL for metal routing									
		Native oxide			1.00	1.00	1.00	1.00	1.00	1.00	1.00
	12.1	Argon milling	Glow discharge	120		120.00	120.00	120.00	120.00	120.00	120.00
		Native oxide after etching			0.00	0.00	0.00	0.00	0.00	0.00	0.00
	12.2	Ti/Au metallization			70.00	70.00	70.00	70.00	70.00	70.00	70.00

Assumed value	Measured value	Simulated value	Process conditions

FIGURE D.1: Caption of the process simulator developed as backup for the SET integration.

Appendix E

Standalone FET - Electrical characterization

In this appendix the complete electrical characterization of the standalone FET fabricated under pre-optimized conditions is presented. Measurements are performed on transistors distributed in arrays. As mentioned along Chapter 3, only wafer #3 and #4 were boron-implanted after gate oxidation in order to adjust threshold voltage. The electrical characterization is performed from different approaches:

- **I_D-V_G:** to obtain the I_{ON}, I_{OFF}, V_{Th}, G_m and SS.
- **I_D-V_G by applying V_{BB}:** to study the relevance of body bias in V_{Th}.
- **I_G-V_G:** to analyse the leakage current through the dielectric gate.
- **I_B-V_G:** to study current through the bulk contact.
- **I_D-V_D:** to observe the different operation modes.
- **C−V:** capacitance measurements on test structures for oxide charges quantification.

$I_D - V_G$ curves and V_{Th} analysis

Fig. E.1 presents the $I_D - V_G$ curves for the 3 μm x 3 μm FET in linear and saturation regime for all four wafers. A significant difference in electrical behaviour is observed from the implanted wafers and the non-implanted ones. With exception of wafer #2, there is no significant deviation in output current depending on different die positions.

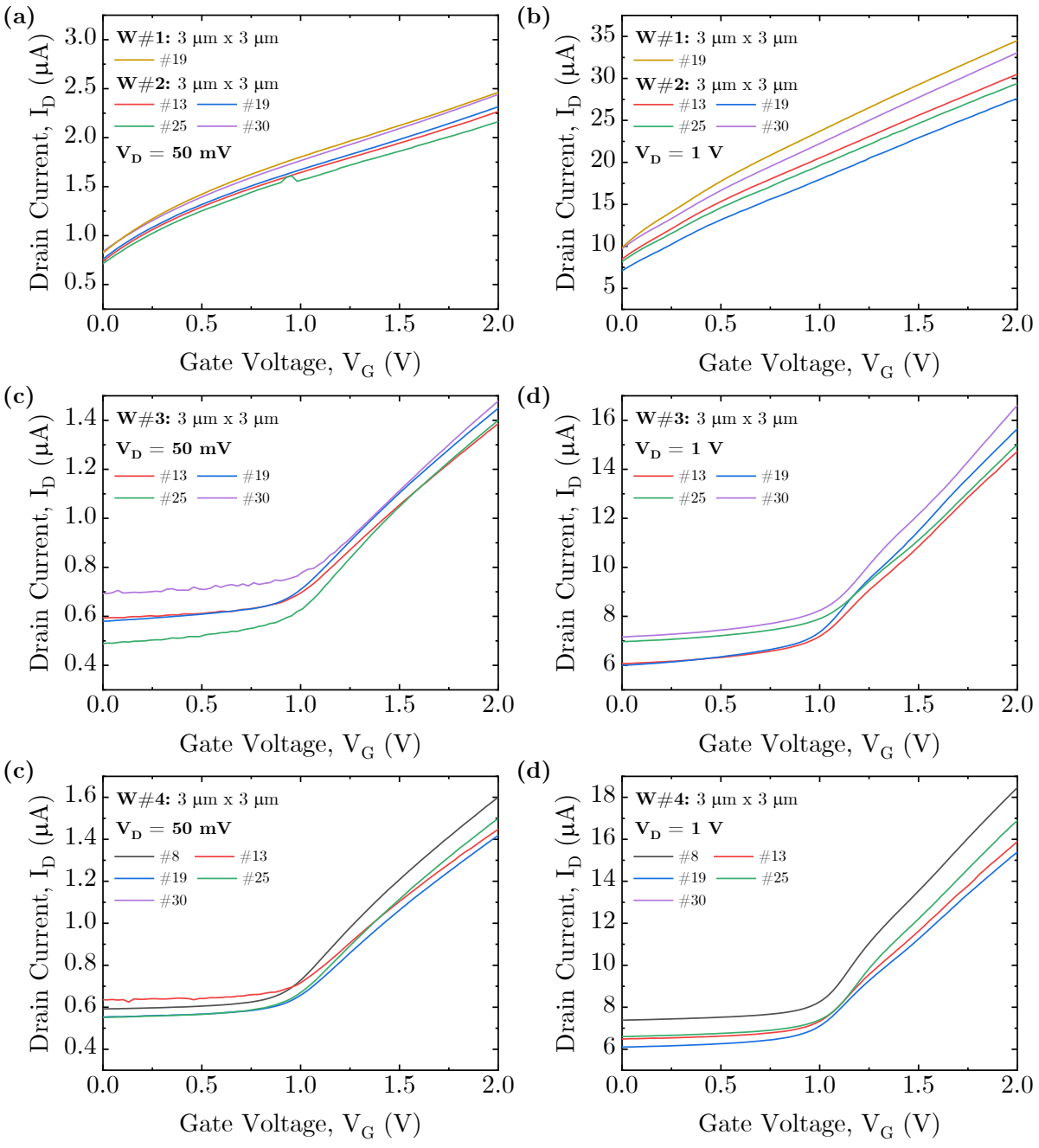


FIGURE E.1: $I_D - V_G$ curves for all four wafers in linear and saturation regime.

There is not observation of any clear cut-off region neither for linear or saturation regime, indicative that the FET is permanently on conduction. In terms of threshold voltage, as Fig. E.2 indicates, the FET of 30 μm x 30 μm presents less variability and higher V_{Th} values than the 3 μm x 3 μm. Threshold voltage values between 200 - 400 mV are measured in this second case, within the required interval for the SET-FET operability.

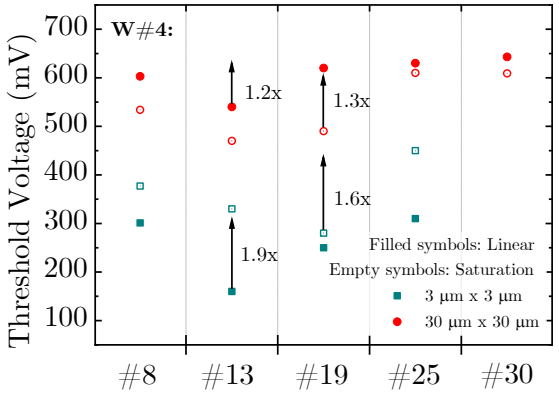


FIGURE E.2: V_{Th} for wafer #4 in linear and saturation regime.

$I_D - V_G$ curves with V_{BB}

An additional method to modify V_{Th} is by applying a bias at the body terminal. By doing so, a shift on the $I_D - V_G$ curve is observed, but again no cut-off region is noted. Similar behaviour is obtained from both implanted wafers.

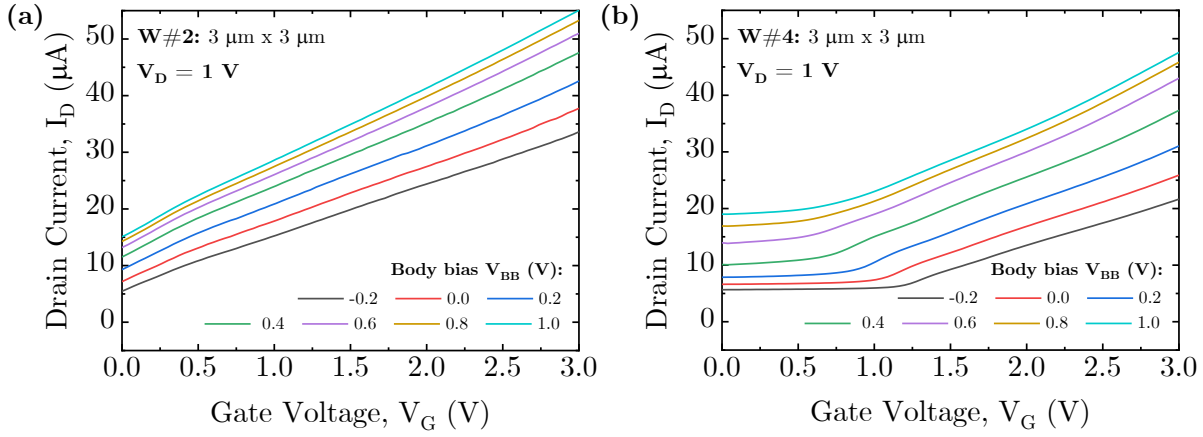


FIGURE E.3: $I_D - V_G$ curves for wafer #2 and #4 in linear regime with body bias V_{BB} applied.

Concerning threshold voltage, the tendency is that at higher body bias applied lower values are obtained. In saturation, similar level of V_{Th} reduction is observed in both cases for the transistors analysed, 3 μm x 3 μm and 30 μm x30 μm. It can be observed as well that V_{Th} measurements are very sensitive with respect wafer position, as it was already deducible from Fig. E.2.

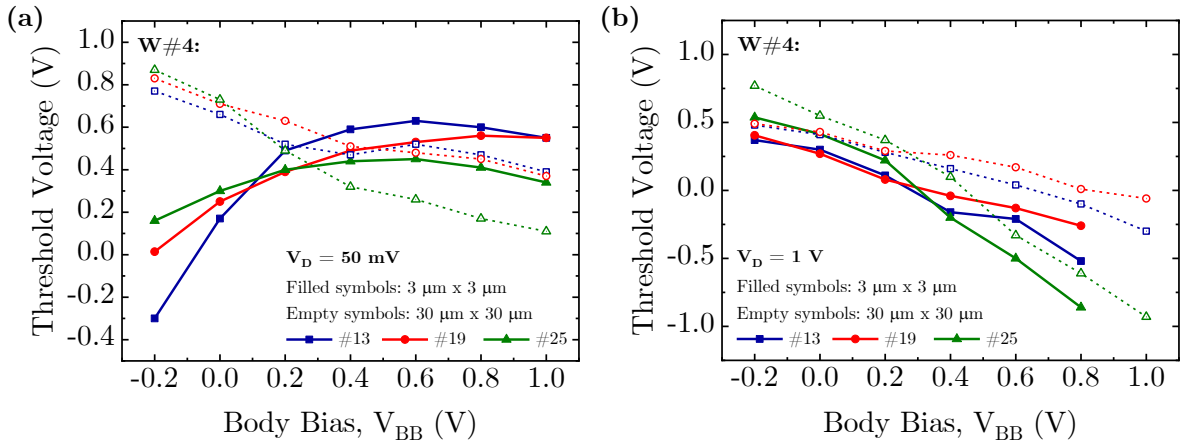


FIGURE E.4: V_{Th} for wafer #4 in linear and saturation regime with body bias V_{BB} applied.

$I_G - V_G$ curves

Similar $I_G - V_G$ curves are observed for all analysed wafers, both implanted and non-implanted. Fig. E.5 presents results for wafer #2 and #4 as one example of each. In all cases low current is observed, indicative that there is negligible leakage through the gate.

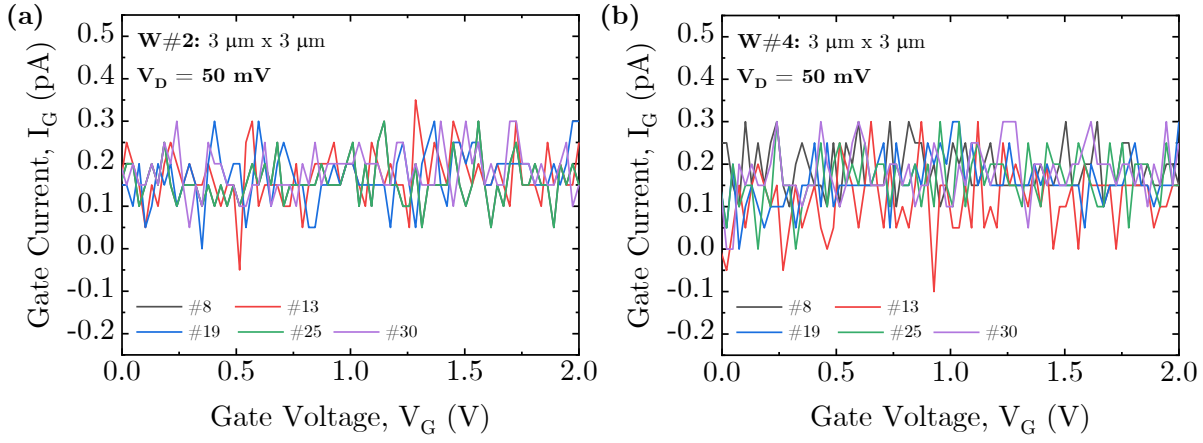


FIGURE E.5: $I_G - V_G$ curves for wafer #2 and #4 in linear regime.

$I_B - V_G$ curves

Low level of current is observed in wafer #1 and #2, in contrast of the higher current levels observed for wafer #3 and #4. It is observed a high level of current through the bulk terminal.

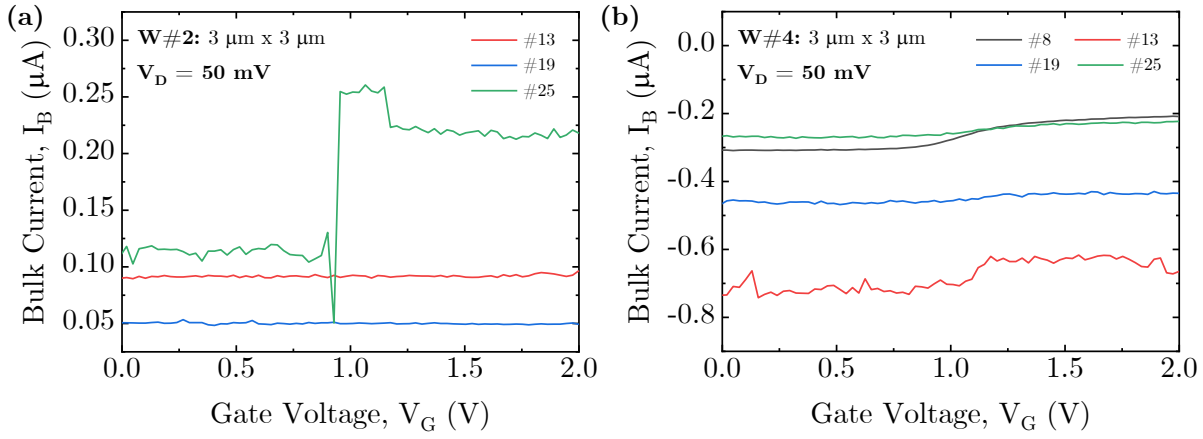


FIGURE E.6: $I_B - V_G$ curves for wafer #2 and #4 in linear regime.

$I_D - V_D$ curves

The $I_D - V_D$ curve is another typical characterization method from which it can be observed the different working regions of the transistor. For same FET dimensions and wafer position, a higher drain current is obtained in the non-implanted wafers when applying bias on the terminal; these wafers present a lower on-state resistance behaviour.

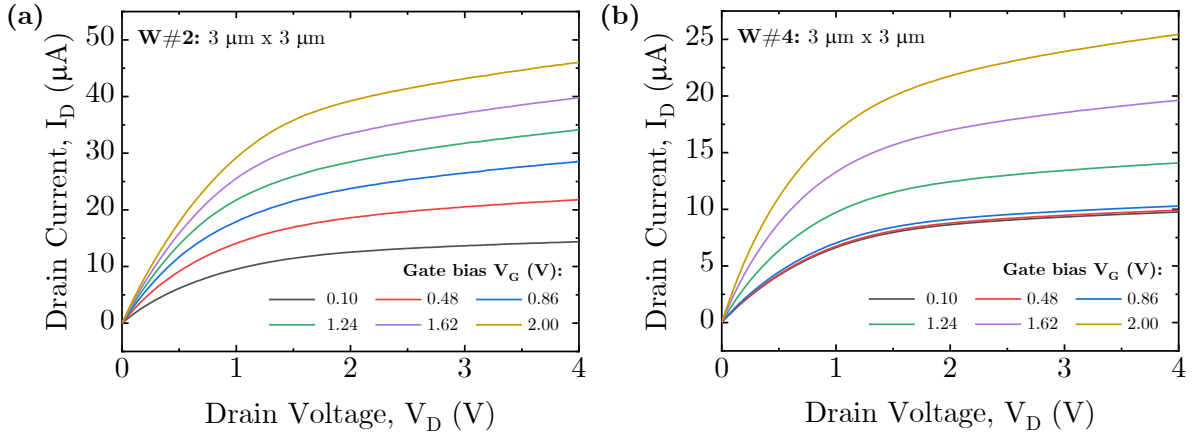


FIGURE E.7: $I_D - V_D$ for wafer #2 and #4.

C−V curves

One of the additional aims for standalone FET fabrication under specific process conditions, besides the process optimization, is the capacitance measurements in order to get an approximation of the number of oxide charges trapped in the Si/SiO_2 interface. A dc voltage is swept from negative to positive bias, superimposed by an ac signal of small amplitude. Fig. E.8 summarizes the C-V measurements for wafer #2 and #3 at low and high frequencies.

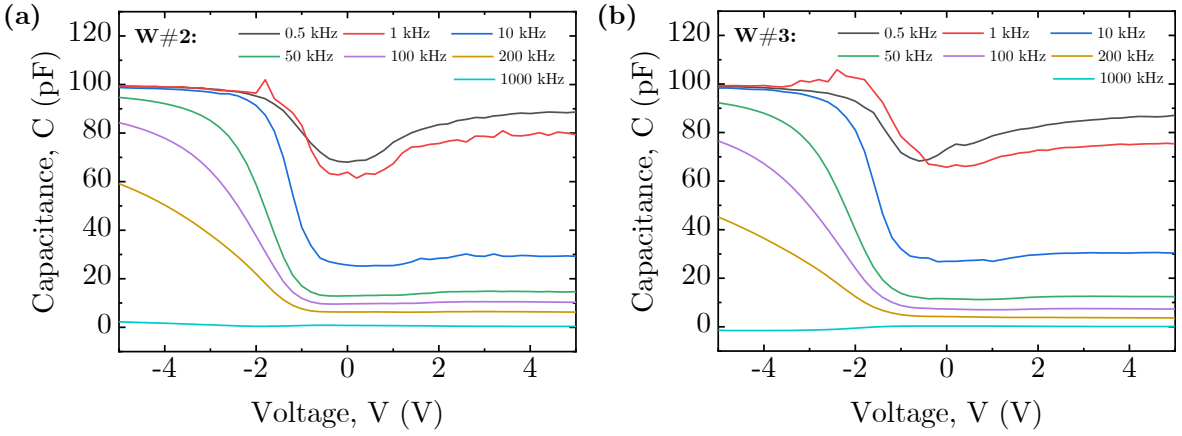


FIGURE E.8: C−V measurements for wafer #2 and #3 on test structures between silicon and polysilicon.

It can be qualitatively distinguished that for higher frequencies charges are not able to follow the signal, and then the capacitance is clipped to the maximum depletion depth. However, using low frequencies the measured capacitance does include the contribution from minority carriers such as oxide charges, and thus the total capacitance is increased.

The quantitative analysis of the oxide charges is focused on the 10 kHz measurement on wafer #2 and #3. From the structure plate area used for measurements and the oxide thickness in each case, the capacitance is described as follows.

$$C_G = \varepsilon_{ox} \frac{A}{t_{ox}} \tag{E.1}$$

Maximum and minimum values are obtained graphically from Fig. E.8. This parameters are summarized in the minimum depletion layer capacitance C_S.

$$C_S = \frac{C_{max}}{A} \frac{1}{(C_{max}/C_{min}) - 1} \tag{E.2}$$

The substrate dopant density is function of C_S; a concentration of $N_{sub} = 6.2 \times 10^{13}$ cm^{-3} is calculated, significantly below the expected value for the p-type wafers used. The total fixed charge density is defined as

$$N_{ox} = 6.24 \times 10^6 \frac{C_{max}}{A}(-V_{FB} - 4.7 + \phi_M - \phi_F) \tag{E.3}$$

where ϕ_F is the Fermi level pinned to the midgap, function of N_{sub}; ϕ_M is the vacuum work-function of the implanted polysilicon, 4.15 V; and the flatband voltage V_{FB} can be obtained from the C-V measurements. In summary, for wafer #2 (non-implanted) and #3 (implanted), values for oxide charges of 3.27×10^{10} cm^{-2} and 4.90×10^{10} cm^{-2} are obtained, respectively.

Appendix F

Scientific contributions

The scientific contributions performed during this thesis are presented as follows, separated by article publications and conference contributions.

Publication in scientific journals

Exploring Strategies to Contact 3D Nano Pillars
Published in NANOMATERIALS
E. Amat, A. del Moral, M. Fernández-Regúlez, L. Evangelio, M. Lorenzoni, A. Gharbi, G. Rademaker, M-L. Pourteau, R. Tiron, J. Bausells and F. Perez-Murano
2020, *Nanomaterials*, 10(4), 716.

Benefits of using arrays of vertical nanowire FETs in integrated circuits to mitigate variability
To be submitted
A. del Moral, E. Amat, J. Bausells and F. Perez-Murano

Conference contributions

Compatibility of CMOS technology with QD-based devices
Submitted for Oral presentation at the 47th International Conference on Micro and Nanoengineering (MNE), Sep 2021, Turin (Italy)
A. del Moral, E. Amat, D. Quirion, N. Torres, H-J. Engelmann, J. von Borany, K-H. Heinig, G. Rademaker, M-L. Pourteau, R. Tiron, J. Bausells and F. Perez-Murano

HSQ-based process to integrate vertical nanoscale devices
Submitted for Oral presentation at the 47th International Conference on Micro and Nanoengineering (MNE), Sep 2021, Turin (Italy)
E. Amat, A. del Moral, H-J. Engelmann, J. von Borany, K-H. Heinig, G. Rademaker, M-L. Pourteau, R. Tiron, J. Bausells and F. Perez-Murano

MEDUSA 82 as SiO_2-like thin-film generator through thermal curing
Submitted for Poster presentation at the 47th International Conference on Micro and Nanoengineering (MNE), Sep 2021, Turin (Italy)
D. Bricio, E. Amat, M. Fernández-Regúlez, J. Llobet, A. Alcacer, O. Muntada-López, A. del Moral, J. Bausells and F. Perez-Murano

Integration of Single Electron Transistor into CMOS technology
Oral presentation at the Quantum Information in Spain (ICE) workshop, May 2021
A. del Moral, E. Amat, D. Quirion, J. Bausells and F. Perez-Murano

Study of the manufacture uncertainty impact of the hybrid SET-FET circuit
Poster presentation at the 6th EuroSOI ULIS Conference, Sep 2020, Caen (France)
E. Amat, A. del Moral, F. Klüpfel, J. Bausells and F. Perez-Murano

Suitability of HSQ as fabrication material for vertical devices at nano scale
Oral presentation at the 45th International Conference on Micro and Nanoengineering (MNE), Sep 2019, Rhodes (Greece)
E. Amat, A. del Moral, H-J. Engelmann, A. Gharbi, G. Rademaker, M-L. Porteau, R. Tiron, J. Bausells and F. Perez-Murano

Self-assembly methods for nanoelectronics
Oral presentation at the NanoSpain Conference, May 2019, Barcelona (Spain)
F. Pérez-Murano, L. Evangelio, S. Gottlieb, M. Fernández-Regúlez, C. Pinto-Gómez, E. Amat, A. del Moral and J. Bausells

Benefits of matrix configuration to implement a SET FET circuit based on vertical topology
Poster presentation at the 5th EuroSOI ULIS Conference, Apr 2019, Grenoble (France)
E. Amat, F. Klüpfel, A. del Moral, J. Bausells and F. Perez-Murano

Vertical nanowire based FET modelling and electrical optimization
Poster presentation at the 5th EuroSOI ULIS Conference, Apr 2019, Grenoble (France)
A. del Moral, E. Amat, J. Bausells and F. Perez-Murano

NW-FET modelling to be integrated in a SET FET circuit
Oral presentation at the 12th Spanish Conference on Electron Devices (CDE), Nov 2018, Salamanca (Spain)
A. del Moral, E. Amat, J. Bausells and F. Perez-Murano

Quantum dot location relevance into SET-FET circuits based on FinFET devices
Poster presentation at the 33rd Conference on Design of Circuits and Integrated Systems (DCIS), Nov 2018, Lyon (France)
E. Amat, F. Klüpfel, A. del Moral, J. Bausells and F. Perez-Murano

Exploring nanofabrication strategies for contacting sub 100 nm vertical structures
Poster presentation at the 44th International Conference on Micro and Nanoengineering (MNE), Sep 2018, Copenhagen (Denmark)
A. del Moral, E. Amat, A. Gharbi, R. Tiron, J. Bausells and F. Perez-Murano

Impact of quantum dot characteristics on the hybrid SET FET circuit behavior
Poster presentation at the International Conference on Solid State Devices and Materials (SSDM), Sep 2018, Tokyo (Japan)
E. Amat, F. Klüpfel, A. del Moral, J. Bausells and F. Perez-Murano

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