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High performance readout circuits and devices for Lorentz force resonant CMOS-MEMS magnetic sensors

Tesi presentada per obtenir el títol de Doctor per la Universitat Politècnica de Catalunya dins del programa de doctorat en Enginyeria Electrònica.

Josep Maria Sánchez Chiva

Director: Daniel Fernández Martínez
Co-director: Jordi Madrenas Boadas

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Integrated Smart Sensors and Health Technologies group
Departament d'Enginyeria Electrònica
Universitat Politècnica de Catalunya

A la Júlia

"I would prefer not to."
Bartleby, the Scrivener

Resum

En les últimes dècades, tenint en compte els primers telèfons mòbils dels anys 90, les capacitats de sensat dels telèfons intel·ligents han millorat notablement. A més, la indústria automobilística i de *wearables* necessiten cada cop més sofisticació en el sensat. Els *Micro Electro Mechanical Systems* (MEMS) han tingut un paper molt important en aquest avenç tecnològic, ja que acceleròmetres i giroscopis varen ser els primers sensors basats en la tecnologia MEMS en ser introduïts massivament al mercat. En canvi, encara no existeix en la indústria una brúixola electrònica basada en la tecnologia MEMS, tot i que els magnetòmetres MEMS varen ser proposats per primera vegada a finals dels anys 90.

Actualment, els magnetòmetres MEMS basats en la força de Lorentz són el centre d'atenció donat que poden oferir una solució integrada a les capacitats de sensat actuals. Com a conseqüència, s'han aconseguit grans avenços encara que existeixen diversos colls d'ampolla que encara limiten la introducció al mercat de brúixoles electròniques MEMS basades en la força de Lorentz. Per una banda, els magnetòmetres MEMS actuals necessiten un consum de corrent i un voltatge de polarització elevats per aconseguir una bona sensibilitat. A més, tot i que a la literatura hi podem trobar dispositius amb rendiments i sofisticació excel·lents, encara existeix una manca de recerca en el circuit de condicionament, especialment de processat digital i control del llaç. Per altra banda, moltes publicacions depenen de processos de fabricació de MEMS fets a mida per fabricar els dispositius. Aquesta és la mateixa aproximació que s'utilitza actualment en la indústria dels MEMS, però té l'inconvenient que requereix processos de fabricació diferents pels MEMS i l'electrònica. Per tant, el cost de fabricació és alt i el rendiment del sensor queda afectat pels paràsits en la interfície entre els MEMS i l'electrònica.

Aquesta tesi presenta solucions potencials a aquests problemes amb l'objectiu d'aplanar el camí a la comercialització de brúixoles electròniques MEMS basades en la força de Lorentz. En primer lloc, es proposa un circuit de condicionament complet en llaç tancat controlat digitalment. Aquest s'ha implementat amb components comercials, mentre que el control digital del llaç s'ha implementat en una FPGA, tot com una prova de concepte de la viabilitat i beneficis potencials que representa l'arquitectura proposada. El sistema presenta un soroll de 550 $nT/\sqrt{Hz}$ quan el MEMS està polaritzat amb 300 μA_{rms} i $V = 1\ V$. En segon lloc, s'han dissenyat varis magnetòmetres CMOS-MEMS utilitzant la part BEOL dels processos CMOS estàndard de TSMC i SMIC 180 nm, que després s'han alliberat amb líquid i gas. La mesura i caracterització dels dispositius s'ha utilitzat per analitzar els beneficis i inconvenients de cada disseny i procés d'alliberament. D'aquesta manera, s'ha pogut realitzar un anàlisi de la viabilitat de la seva fabricació en massa. S'han obtingut valors de *yield* de fins al 86% per un dispositiu fabricat amb SMIC 180 nm en una oblia completa, amb una sensibilitat de 2.82 $fA/\mu T \cdot mA$ i un factor de qualitat $Q = 7.29$ a pressió ambient. Per altra banda, el dispositiu fabricat amb TSMC 180 nm presenta una $Q = 634.5$ i una sensibilitat de 20.26 $fA/\mu T \cdot mA$ a 1 $mbar$ amb $V = 1\ V$. Finalment, s'ha dissenyat un circuit integrat que conté tots els blocs per a realitzar el condicionament de senyal del MEMS. El MEMS i l'electrònica s'han fabricat en el mateix dau amb el procés estàndard de TSMC 180 nm per tal de reduir paràsits i millorar el soroll i el consum de corrent. Les simulacions mostren una resolució de 8.23 $\mu T/mA$ amb $V = 1\ V$ i $BW = 10\ Hz$ pel dispositiu dissenyat.

Abstract

In the last decades, sensing capabilities of smartphones have greatly improved since the early mobile phones of the 90's. Moreover, wearables and the automotive industry require increasing electronics and sensing sophistication. In such technological advance, Micro Electro Mechanical Systems (MEMS) have played an important role as accelerometers and gyroscopes were the first sensors based on MEMS technology massively introduced in the market. In contrast, it still does not exist a commercial MEMS-based compass, even though Lorentz force MEMS magnetometers were first proposed in the late 90's.

Currently, Lorentz force MEMS magnetometers have been under the spotlight as they can offer an integrated solution to nowadays sensing power. As a consequence, great advances have been achieved, but various bottlenecks limit the introduction of Lorentz force MEMS compasses in the market. First, current MEMS magnetometers require high current consumption and high biasing voltages to achieve good sensitivities. Moreover, even though devices with excellent performance and sophistication are found in the literature, there is still a lack of research on the readout electronic circuits, specially in the digital signal processing, and closed loop control. Second, most research outcomes rely on custom MEMS fabrication processes to manufacture the devices. This is the same approach followed in current commercial MEMS, but it requires different fabrication processes for the electronics and the MEMS. As a consequence, manufacturing cost is high and sensor performance is affected by the MEMS-electronics interface parasitics.

This dissertation presents potential solutions to these issues in order to pave the road to the commercialization of Lorentz force MEMS compasses. First, a complete closed loop, digitally controlled readout system is proposed. The readout circuitry, implemented with off-the-shelf commercial components, and the digital control, on an FPGA, are proposed as a proof of concept of the feasibility, and potential benefits, of such architecture. The proposed system has a measured noise of 550 $nT/\sqrt{Hz}$ while the MEMS is biased with 300 μA_{rms} and $V = 1\ V$. Second, various CMOS-MEMS magnetometers have been designed using the BEOL part of the TSMC and SMIC 180 nm standard CMOS processes, and wet and vapor etched. The devices measurement and characterisation is used to analyse the benefits and drawbacks of each design as well as releasing process. Doing so, a high volume manufacturing viability can be performed. Yield values as high as 86% have been obtained for one device manufactured in a SMIC 180 nm full wafer run, having a sensitivity of 2.82 $fA/\mu T \cdot mA$ and quality factor $Q = 7.29$ at ambient pressure. While a device manufactured in TSMC 180 nm has $Q = 634.5$ and a sensitivity of 20.26 $fA/\mu T \cdot mA$ at 1 $mbar$ and $V = 1\ V$. Finally, an integrated circuit has been designed that contains all the critical blocks to perform the MEMS signal readout. The MEMS and the electronics have been manufactured using the same die area and standard TSMC 180 nm process in order to reduce parasitics and improve noise and current consumption. Simulations show that a resolution of 8.23 $\mu T/mA$ for $V = 1\ V$ and $BW = 10\ Hz$ can be achieved with the designed device.

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Chapter 1

Introduction

1.1 Thesis motivation

In the last decades, smartphones have clearly consolidated their position in the consumer electronic market at the same time that their characteristics and sensing capabilities have greatly improved since the early mobile phones of the 90's. Nowadays, the concept of *wearables* is more than just a science fiction idea as smartwatches and activity trackers popularity is having a spectacular growth. Good proofs of those claims are the ever growing revenues of companies in the wearables and smartphone businesses or related. Also the automotive market is in a race to design and manufacture vehicles with improved electronics and sensing sophistication in order to increase security and allow the release of self-driving cars or, at least, with Advanced Driver-Assistance Systems (ADAS). All these products, among others that have not been mentioned, share the need of more and better sensing capabilities. The objective is clear: the need of harvesting information about the geographical position, movement, heading of the device, etc.

The rise of such markets has made researchers to focus their efforts in the design of low-cost, low-power and low-volume inertial sensors. Accelerometers and gyroscopes are examples of these research outcomes as they were the first sensors based on Micro Electro Mechanical Systems (MEMS) technology massively introduced in the market [1, 2]. In contrast, to the best of our knowledge, it still does not exist a commercial MEMS-based magnetometer even though Lorentz force based MEMS magnetometers were first proposed in the late 90's [3–6]. On the contrary, magnetometers and electronics compasses currently present in high volume products consist mostly in Hall sensors [7], Anisotropic Magnetoresistors (AMR) [8], Tunnel Magnetoresistors (TMR) [9] and Giant Magnetoresistors (GMR) [10]. Their main disadvantage, though, is their need of materials not compatible with standard manufacturing processes and their high current consumptions [11]. Hence, Wafer-to-Wafer, Chip-to-Wafer bonding, or System-in-Package solutions are needed to connect the sensors to a die containing the readout electronics.

In order to reduce volume and cost of electronic compasses, the solution lies in developing magnetometers that can be integrated with accelerometers and gyroscopes in the same die area. And this necessarily requires the design of MEMS magnetometers. Several MEMS magnetic sensors are reported in the literature with excellent performance. On the contrary, the electronic circuitry needed to readout the sensor signals have frequently been forgotten as most articles present the minimum electronic circuits needed to make device performance measurements and characterization. As a consequence, few articles have been found in the literature where full custom (both full-silicon or printed circuit board) electronic circuits is presented. And in that case, they suffer from low sensitivities, high noise, high power consumption or small bandwidth. For this reason, the switch from current e-compass magnetic sensors to MEMS compasses is not yet justified. Even

though it is a very promising field.

The potential solution proposed in the previous paragraph, though, is only a partial solution as accelerometers and gyroscopes currently available in the market are still being manufactured using custom MEMS processes not compatible with the electronics. One possible solution to this issue is the design of MEMS magnetometers taking advantage of the Back-End-Of-Line (BEOL) part of a standard CMOS process. This means designing the MEMS structures with the metal stack available in standard CMOS processes, typically used for the interconnection of electronic components. This solution has already been proposed by the research group with accelerometers and atmospheric pressure sensors with very promising results.

For all of the reasons presented above, the main objectives of this thesis are:

- Evaluation of current circuits, systems, and devices found in the literature.
- Proposition of a system to perform the MEMS resonant magnetometer signal readout to improve the currently reported readout circuits performance.
- Design and analyse a MEMS magnetometer using the BEOL metallizations of a standard CMOS process.
- Design an integrated circuit to perform the MEMS signal readout and manufacture it in the same die area of the MEMS.

1.1.1 E-compass market: present and future prospects

The effort of switching from current magnetometers to MEMS magnetometers in the same die area that the electronics has very interesting motivations from the commercial point of view due to the possibility of cost reduction that multiple sensors integration in the same die are offer [10]. Magnetic sensor market value was $1.64 billion in 2016, and with a 7% compound annual growth rate between 2016 and 2022, it is expected to reach $2.5 billion in 2022.

Automotive market represents the 50% of the overall market due to the inclusion of 20-30 sensors per car. However, hybrid cars would require up to 35, used for position and speed sensing, switching, and current sensing. Secondary markets include industrial plants, transportation, home appliances and consumer electronics. This market growth is expected to be led by the transition of brushless motors in industry and the Internet of Things (IoT). Finally, e-compass market is suffering a stabilization due to price erosion and smartphone market saturation. However, wearables, robots and drones are expected to be the main markets that will lead growth in the following years (even though it is important not to forget other applications either in research or yet to be introduced in the market [12, 13]). Current market stabilization, though, is not a problem as widespread Hall sensors are being replaced by a set of new technologies utilizing the magnetoresistive phenomenon: AMR, GMR, and TMR (xMR). As a consequence, such sensors market share will experience an increase from 27% to 33% in the same time period [10].

In the latest years, Lorentz force based MEMS magnetometers have been a hot topic with numerous publications because they are an alternative technology that offers good sensitivity with a relatively low current consumption. Hence, if MEMS magnetometers keep improving, it is not unlikely that they replace xMR sensors in the future. Moreover, MEMS magnetometers can be integrated using the same processes used to manufacture accelerometers and gyroscopes, which offers the possibility of integrating all of them in the same die area of the electronics. This would lead to a reduction of area, volume and fabrication cost, a key issue in 9-axis sensor combos [14].

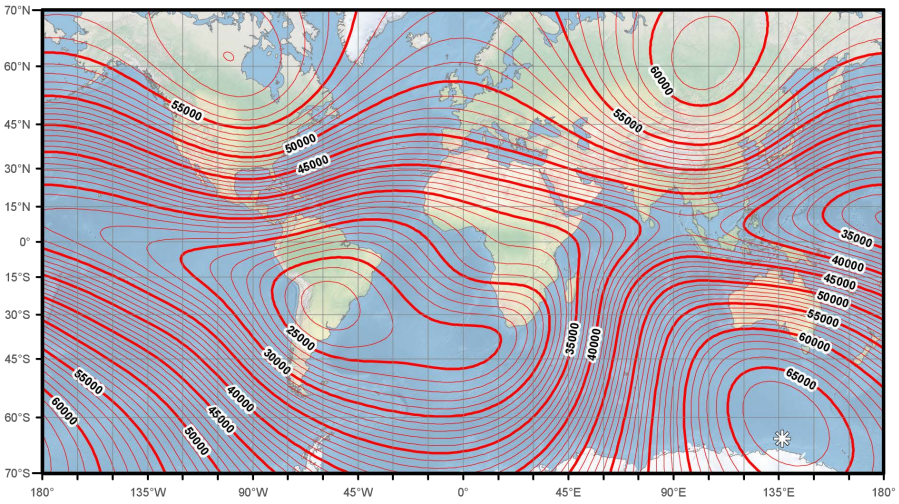


Figure 1.1.1: Earth surface magnetic field map from [15]. Magnetic field values are in nT and each contour interval is 1000 nT.

1.1.2 Earth magnetic field measurement

Earth magnetic field can be modelled as a magnetic dipole, whose poles are named geomagnetic poles. Over the earth surface, the magnetic field has three components, namely, the northerly intensity X, the easterly intensity Y (the weakest one) and the vertical intensity Z. From these components, horizontal and total magnetic field can be derived. Fig. 1.1.1 extracted from [15] shows the total magnetic intensity, which is the magnetic field we are interested to measure.

Such total magnetic field is not constant around all planet surface and, in fact, it ranges from around 23 μT to 66 μT [15,16], even though, for simplicity and to account for year to year variations, it is sometimes rounded to between 10 μT and 100 μT [11].

In order obtain the compass heading respect to the north geomagnetic pole, which corresponds to an angle of 0°, it is first necessary to know which is the maximum intensity of the field [17] as the horizontal component of the field always points to the north, while the vertical component points downwards the surface with an intensity that depends on the location. Once the maximum field B_{max} is known, it is possible to extract the heading angle ϕ using the following equation

$$\phi = \arctan\left(\frac{B_y}{B_x}\right) \tag{1.1}$$

Where B_y is the measured vertical component of the field and B_x is the horizontal component, as shown in Fig. 1.1.2, using the device as coordinates reference. Maximum field previously measured is $B_{max} = \sqrt{B_x^2 + B_y^2}$. In this example, only two axes have been required given that the e-compass has been considered to be parallel to the surface of the earth. This is not always the case, though. In real applications the device has to work even when it is rotated respect to its x (pitch) and y (roll) axes, while still being able to measure the heading angle (also known as yaw). This means that:

- An accelerometer is needed in order to know how the device is oriented respect to the gravity vector.
- A third magnetometer axis must be included to cope with the device orientation not being

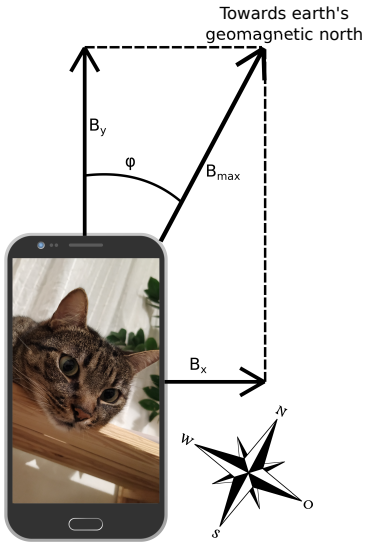


Figure 1.1.2: Diagram of the magnetic field vectors measured to obtain the heading angle.

Table 1.1: 3-axis magnetometer compatibility specifications for Android 9 [19]

	Units	Min.	Nom.	Max.
Resolution (ϕ_{min})	μT		0.6	
Sensitivity	$LSB/\mu T$		0.5	
Bandwidth	Hz	10	50	
Noise[a]	$nT/\sqrt{Hz}$		84.9[b]	189.7[c]
Hard iron offset	μT	200	700	
Minimum heading accuracy[d]	°			1.5
Maximum field before saturation	μT	-900		900
Power (@ 10 Hz)	mW		1.0	3.3

[a] Values extracted from resolution and bandwidth in the table.
[b] Noise value for bandwidth of $50Hz$.
[c] Noise value for bandwidth of $10Hz$.
[d] Heading accuracy from eq. 1.1 where $B_{earth} = 23\ \mu T$ is the worst case.

ideal.

The math behind the extraction of the angle from a 3-axis magnetometer data working together with an accelerometer has already been covered by companies producing e-compass chips [17, 18].

A useful reference to quantify the sensor specifications is the Android 9 compatibility definition document, which lists the requirements that any device must comply with in order to be compatible with Android 9 [19]. The most important characteristics have been summarized in table 1.1. As it can be seen, some figures are challenging. With this data in mind, we can now review the most common e-compasses used in smartphone, automotive and other high volume consumer electronics market.

1.2 Magnetic sensors in the market: an overview

As explained in previous sections, the Hall sensors dominate the magnetometer market, even though in the last years it has been suffering a replacement by xMR sensor [10]. Acronym xMR makes reference to a variety of sensors based on the manetoresistive properties of some materials, which is the tendency of a material to change its electrical resistance under the presence of a magnetic

field.

1.2.1 Hall effect magnetometers

Hall effect sensors exploit the phenomenon discovered in 1879 by Edwin H. Hall while he was working in his doctoral degree [20]. The discovery was published in an article under the name "On a New Action of the Magnet on Electric Currents" [21]. Hall observed that a thin gold rectangle plate crossed by an electric current and under the presence of a strong magnetic field perpendicular to the surface of the plate experiences a voltage difference perpendicular to the current direction. The explanation of the phenomenon is as follows: under the presence of a magnetic field, the charge carriers of the current experience a force perpendicular to the current direction due to the Lorentz force $\vec{F_L}$ which forces them to deviate from the straight line they would follow without the force.

$$\vec{F_L} = q\vec{E} + q\vec{v} \times \vec{B} \tag{1.2}$$

Where q is the electric charge, $\vec{E}$ is the electric field, $\vec{v}$ is the charge velocity, and $\vec{B}$ is the magnetic field. These charges, then, accumulate on one face of the gold plate, while opposite charges accumulate in the opposite face. As a consequence, the separation of opposite polarity charges generates an electric field. This voltage is the output signal of Hall effect sensors [11]. Inexpensive and low sensitivity silicon Hall effect sensors have been manufactured, but more sensitive devices can be obtained with III-IV semiconductors (being indium antimonide the most common), which achieve measurements of fields as low as 100 nT. Hall sensors are low cost, low area, low power sensors that work under a wide temperature range as long as some compensation is applied, and up to 1 *MHz* frequencies [11,22,23]. Unfortunately, Hall sensors have two main disadvantages First the need of flux concentrators in order to increase the sensitivity [24,25], which makes it difficult to manufacture using standard CMOS processes. And second, they suffer from a large offset [26,27].

A popular commercial magnetometers based on Hall sensors is [7].

1.2.2 xMR magnetometers

The odd name of xMR groups all magnetometers based on the magnetoresistive properties of a given material [10]. Magnetoresistance of a material is its ability to change its electrical resistance under the presence of an external magnetic field [28]. The phenomenon was first observed by William Thomson (popularly known as Lord Kelvin) in 1857, when he observed the anisotropic magnetoresistance in two ferromagnetic materials: iron and nickel [29]. It was not until the late 1980s when Giant Magnetoresistance (GMR) was simultaneously discovered by two different research groups [30,31]. Some years later Albert Fert and Peter Grünberg were awarded the Nobel prize of physics for the discovery [32].

But some decades before, Orso Mario Corbino [33] already established the mathematical basis of magnetoresistance. For the theoretical analysis, Corbino used an ideal conducting disc with a hole at its center and two ideal electrodes surrounding both inner and outer disc peripheries. Doing so, and without a magnetic field, a voltage between the electrodes generates a radial current that flows through the radial equivalent resistance between electrodes R_{radial}. A diagram of the disc is shown in Fig. 1.2.1. Under the presence of a magnetic field, current charges suffer the Lorentz force, making them experience a drift that generate a circular current. The equivalent resistance that circular current crosses is inversely proportional to the amount of magnetic field.

$$R_{circular} = \frac{\rho^2}{s^2 R_{radial}(1 + \mu^2 B^2)} \tag{1.3}$$

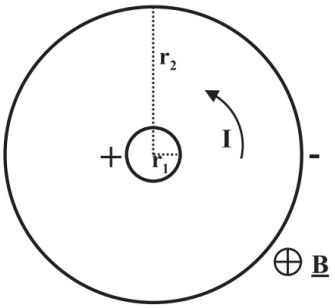


Figure 1.2.1: Diagram of Corbino disc as depicted in [34].

Where s is the disc thickness, ρ is the material resistivity, μ is the electron mobility, and B is the applied magnetic field. More detailed explanations of the phenomenon may be found in [34]. With this operation principle, different materials experiment magnetoresistance in different ways.

1.2.2.1 Anisotropic Magnetoresistance

Anisotropic Magnetoresistance (AMR) is the property of some materials to change their electrical resistance as a function of the angle between the material magnetization and the current flow [35]. The most commonly used material is permalloy, which is compatible with current fabrication processes. AMR sensors can detect minimum fields of 0.1 nT while still having a large dynamic range and being able to measure magnetic fields at frequencies of up to 1 GHz in a wide temperature range. Unfortunately, they have some important disadvantages. First, the fabrication of the sensors is done with sputtering, which results in highly mismatched devices. This mismatch causes an important amount of offset. To compensate the offset, on-chip coils are required to generate a periodic strong magnetic field, which increases power consumption [11]. Second, an intense magnetic field must be applied during the fabrication of the sensors in order to orient their magnetization, increasing the difficulty of the fabrication process. Third, too much intense magnetic fields may change the orientation of the sensors magnetization, destroying the device.

MEMSIC is one of the leading companies in AMR magnetometers [36, 37]

1.2.2.2 Giant Magnetoresistance

A very high change in resistance was observed when using very thin magnetoresistor, which ended being called Giant Magnetoresistances (GMR) [30,31]. Its practical application is as follows: GMR is achieved using four-layer structures made of two thin ferromagnets separated by a conducting layer. The remaining layer is an antiferromagnet that is placed next to one ferromagnetic layer in order to avoid the rotation of its magnetization vector. When the magnetizations of both ferromagnetic layers are parallel, electrons find less resistance in their path either in the parallel or perpendicular direction of the magnetization. This is due to the fact that electrons suffer less scattering moving to different electronic bands. When a magnetic field is applied, the ferromagnetic layer not touching the antiferromagnetic layer can change its magnetization vector direction, which changes resistance. Resistance change is around $\times 3$ larger than AMR counterparts.

Compared to AMR sensors, GMR ones do not need a periodic calibration, but suffer from a higher flicker noise and a minimum measured magnetic field two orders of magnitude larger: 10 nT [11]. Moreover, their manufacturing process is more complicated, which increases the cost.

GMR sensors can be found in mechanical computer hard disks drives (HDD), where they are used to read stored data [11].

1.2.2.3 Magnetic Tunnel Junction

Magnetic Tunnel Junction (MTJ) (also known as Tunnelling Magnetoresistance (TMR)) sensors have a very similar structure to GMR, but a different working principle. In MTJ, the conducting layer in GMR stack is replaced by a very thin insulator. Sensing is performed by tunnelling of the electrons across the insulating layer, which is a value that depends of the two ferromagnetic layers magnetization direction, which in turn, is proportional to the magnetic field strength.

MTJ sensors, being constructed with an insulating layer, have a higher resistance, which reduces power consumption. However, they present a high white noise as well as shot noise. On the other hand, manufacturing them is very difficult as very thin layers (insulator thickness must be of 1 nm) are needed, making it difficult to fabricate using standard processes and increasing cost. Plus, fabrication process must be accurate in order to avoid any short between the ferromagnetic layers separated by the thin insulator [11].

In 2017 TDK released the TAD2141, TMR angle sensor with an angle accuracy of $\pm 0.05^\circ$ ($\pm 0.2^\circ$ guaranteed over product lifetime) which is an important improvement respect current commercial devices [9]. The same year, NVE Corporation also released its TMR sensor with slightly worse angle detection [38].

1.2.2.4 Other magnetic sensors

There are plenty of other magnetic sensors that have not been covered yet because they are either still in the research and development phase or have a low market penetration. Below, some of them are going to be mentioned, even though this thesis state-of-the-art section is intended to give the reader just an overview of the magnetic sensors that have the most popularity in the market at the time of writing this document. For more information, the reader is encouraged to read the article of Lenz and Edelstein [11]. It offers a good introduction to magnetic sensors, both in the research or market phase; covering also sensors for different applications. It is a good starting point in the field of magnetic sensors.

In the market there are two magnetic sensors which still deserve to be mentioned, though. The first one is the Magneto Impedance (MI) sensor. Impedance (both real and imaginary) of MI sensors suffer changes under the presence of a magnetic field due to the different phenomenons depending on the sensor's working frequency [39]. Such sensors have been commercialized by Aichi Steel [40], but, again, require the use of material not natively present in a standard fabrication process, increasing the fabrication cost.

The second sensor worth mentioning are Fluxgate, which where introduced in the market with a very similar approach by Bosch under the name of Flip-Core [41]. A thin magnetic layer is used in the core of the sensor. This core is magnetically driven by one coil, while a second coil is used to detect when the magnetic layer magnetization reverses. Compared with other magnetic sensors, it has quite higher current consumption due to the need of coil driving. Moreover, current chip in the market requires a Hall sensor to detect Z-axis magnetic field, a good indication of the difficulty of manufacturing such sensors in planar technologies such as CMOS.

1.3 The competitor: MEMS magnetometers

In the previous section, a quick overview of the current state-of-the-art of popular magnetic sensors has been done. Each presented sensor has its own characteristics and advantages, but all of them share a common disadvantage: they require materials not present in current standard CMOS fabrication processes. To avoid that, the currently widespread and well know MEMS technology has been proposed to replace such sensors. It has the further advantage of offering sensors in a technology that is already being used to fabricate accelerometers and gyroscopes, which would represent an important impact in terms of area, volume, and cost reduction.

There exist two main types of MEMS magnetometers. First, MEMS magnetometers based on the Lorentz force, which are the most popular and widespread. They are based on the Lorentz force, that states that charged particles (current electrons) suffer a force under the presence of a magnetic field, which are used to generate a displacement of the movable structure of the MEMS. This kind of magnetometers are the ones used in this thesis. Second, electromagnetic induction MEMS magnetometers have recently been proposed. They are based on Faraday law of induction, that states that a variable magnetic field generates a voltage in a closed coil [42, 43].

In this section, various topics are being covered. First, the working principle of Lorentz force sensors. Second, the state-of-the art of MEMS Lorentz force devices, modulation strategies and readout systems and architectures. And third, a brief description of MEMS using the BEOL section of a standard CMOS process, as MEMS magnetometers in this thesis have been designed to be integrated within the same die area that the electronics using this strategy, also known as CMOS-MEMS.

1.3.1 MEMS Lorentz force magnetometers working principle

The Lorentz force states that a moving charged particle suffers a force under the presence of a magnetic field, as seen in equation (1.2). In the case of our MEMS magnetometers, those moving charged particles are the current electrons flowing through the MEMS structure. Given that a current I flows through a structure of length L, the resulting Lorentz force F_L can be described as

$$\vec{F_L} = I\vec{L} \times \vec{B} \tag{1.4}$$

where $\vec{B}$ is the magnetic field being measured. When electrostatically driven, the sensor response can be described with the second order mass-spring-damper function

$$m\ddot{z} + b\dot{z} + kz = F_E + F_L \tag{1.5}$$

where, m is the device rotor mass, b is the damping coefficient, and k is the spring constant. $F_E \approx V \cdot v \cdot C_s/g$ is the electrostatic driving force that is a function of the device dc voltage V, the electrostatic driving voltage v, the sensor capacitance C_s and its gap g [44]. Finally, F_L is the resulting Lorentz force when a magnetic field orthogonal to the current direction is applied to the device.

This mathematical model can be used as a starting point to analyse the different modulation strategies explained in following sections.

1.3.2 MEMS magnetometers introduction

MEMS magnetometers making use of Lorentz force were first proposed by Kádár et al. and Eyre et al. in the 90's [3–6]. Since then, the topic of MEMS magnetometers has received a warm welcome by researchers all over the world, who have pushed the boundaries of the first devices. In the

two decades that have passed since Kádár and Eyre works, MEMS magnetometer research has found two different areas to advance, strongly interrelated one to the other. The first topic is the improvement of MEMS devices in order to increase sensitivity. The second topic is the study of readout architectures to harvest magnetic field data.

As a consequence, the state-of-the-art review of MEMS magnetic field sensors is divided into two main subcategories: a brief review of MEMS devices to sense magnetic fields, and circuits and systems for the magnetic field signals readout.

1.3.3 MEMS magnetometers devices

As mentioned above, the first works on the topic of MEMS magnetometers were mostly devoted to MEMS device design [3–6]. Pushed by the advances of MEMS accelerometers of the early 90's, the MEMS were manufactured using single-crystal silicon structures with bulk micromachining techniques and metal lines deposited over it. Both devices were torsional, with current flowing in different directions in the two sides of the device. Doing so, first order cancellations of acceleration was achieved. The main difference was the use of capacitive [3, 4] or piezoresistive outputs [5, 6]. The main disadvantages were the high current consumption in the order of few tens of mA and the complex fabrication process. However, in the references it is possible to identify the main trends of future works: sensitivity increase by using the device in resonance, search of high Q values and the amplitude modulated output.

Some early MEMS magnetometers were designed using U-shaped clamped-free cantilevers. Manufactured in bulk micromachining, the current responsible of generating the Lorentz force flows along the U-shaped cantilever [45–48]. The current flows in three different directions, but only the current flowing parallel to the silicon stator does not cancel out the generated Lorentz force. An interesting advance of these works, is that various metal stripes are deposited over the U-shaped cantilever in order to reuse the current and increase the Lorentz force. Due to the low capacitance that can be obtained from these structures, piezoresistive readouts with a Wheatstone bridge is preferred. Using piezoresistors, unfortunately, has important drawbacks. First, current consumption is higher due to the need of biasing of the Wheatstone bridge. And in an inherently power hungry device, such as the ones based on the Lorentz force, this may be a critical factor. On the other hand, piezoresistors, due to their nature, have quite a high noise, increasing output noise floor. Finally on U-shaped magnetometers, [47] reports measurements using an optical readout. However, current consumption and manufacturing complexity are high.

More complex MEMS structures soon appeared in the literature. The first example is [49], that reports a capacitive output device with a collection of fixed and movable comb electrodes with a conducting micro beam for the driving current. The device was manufactured in a quite complex surface micromachining process with good resolution and low current driving. In [50], a differential capacitive output is achieved by means of interdigitated electrodes. Moreover, the BEOL part of a standard 0.35 μm CMOS process is used, followed by a three step release of the structures to etch away the surrounding oxide, top aluminium, and some die silicon.

A common practice found in the literature is the use of long beams that deflect under the Lorentz force. In [51] beams deflection change the resonator resonance frequency, which is detected capacitively with comb capacitors. However one important issue is the heat generated by Joule effect on the bars, which is a source of resonance frequency shift. In [52, 53] a similar structure is used (with similar heating issues), but the difference is that the device is electrostatically driven at the anti-phase mode, which has a higher Q than other modes due to the cancellations of the opposing stress waves in the bars end.

Torsional devices are commonly found in the literature due to their first order cancellation of

acceleration detection as mentioned above. One interesting example is [54], whose design is accurately simulated using finite element simulations in order to make the device first mechanical mode to be the torsional mode. Differential capacitive output is made with simple parallel plates unlike most differential output devices, which use comb capacitances prone to stiction during structure release. Similar to those in [5, 6], [55] proposed a torsional device capable of detecting magnetic fields at atmospheric pressure, but with high current driving of 22 mA. A similar device from the same research group has also been reported [56]. A special mention must be made to Kyynäräinen et al. work [57], where the three axes where obtained by a double-ended tuning fork and a torsional MEMS magnetometer with impressive sensitivity figures. Interestingly, the torsional device was designed with a coil on top of the movable structure. Doing so, the effective current carrying length is longer, increasing the Lorentz force and the sensitivity of the device. A similar sensor is reported in [58]. Finally, [59, 60] report MEMS magnetometers with a similar structure. However, the current on both sides of the device flow in the same direction, making the MEMS to work in a flapping mode instead than a torsional mode.

Few works on single-device multi-axis detection have been reported. The first examples of multi-axis devices are the works in [55, 57, 61–63], where both lateral axes are measured with a single structure, while z-axis requires a different MEMS. This is due to the simplicity of making symmetric devices that allow he driving current to flow across perpendicular directions. In this category, it is worth to mention the work of Elsayed et al. [64] due to its simple design, capable of measuring 2-axis lateral magnetic fields as well as acceleration in the out-of-plane axis using a single device. The work in [62] was later improved, and the same research group reported a single structure 3-axis magnetometer [65]. Recently, an interesting 3-axis MEMS magnetometer was reported [66, 67]. The device uses the same driving current to sense the three axes by using a coil where the current circulates. Moreover, lateral axes allow the device to work in torsional mode with two different torsion axes, while z-axis is detected by the MEMS expansions and contraction. Moreover, the resonance frequencies of the three modes have been designed to be very similar in order to simplify electronics.

Other mechanisms have been proposed in the literature in order to improve sensitivity in Lorentz force magnetometers. In [68], a leverage mechanism with long beams is proposed to amplify the force generated by the magnetic field. In [69] the mechanical tensions produced on the device by Lorentz force is amplified using a microleverage mechanism. In [70] the driving current is made to flow along the contour of the MEMS disk. A magnetic field generates a radial Lorentz force, which makes the MEMS to expand and contract. Such movement is then detected by using piezoelectric transduction. This same transduction principle is used in [60, 71].

Finally, an issue found in Lorentz force magnetometers is that driving current moving along the MEMS movable structure generates a voltage drop across it due to the material resistivity, which translates into an electrostatic force added to the magnetic field signal. Such signal, moreover, is at the device resonance frequency. Nevertheless, this issue is hardly mentioned in the literature. In [72] a p-n junction is proposed to reduce this signal, while Valle et al. proposed to shield the structures that carry the current with a metal cage connected to the electrostatic driving electrode [73, 74].

1.3.4 MEMS magnetometers readout modulations

MEMS magnetometers are resonant sensors that usually work at the MEMS mechanical resonance frequency. Doing so, device sensitivity is increased and low-frequency flicker noise is avoided. As a consequence, the baseband magnetic field signal is upconverted to the device resonance frequency. This upconversion has also been a topic of research, whose outcomes have been different modulation strategies that can be divided into two different categories: Amplitude Modulated (AM) and Frequency Modulated (FM) strategies.

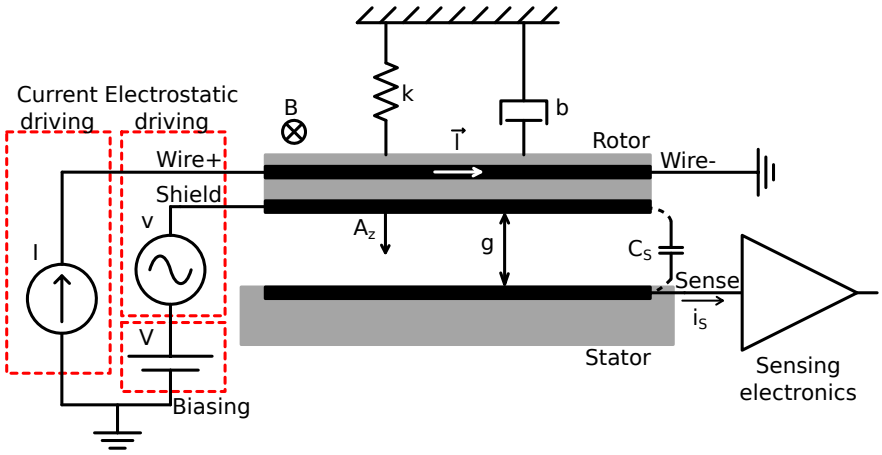


Figure 1.3.1: Simplified MEMS and readout electronics diagram with the device electromechanical model.

1.3.4.1 Amplitude Modulated (AM) readouts

Due to their simplicity, AM readout implementations have been widely used [6, 49, 57, 63, 75–78]. The working principle of AM readout circuits consists of a current flowing through the plate sensor at a frequency equal to the mechanical resonance frequency of the resonator. Electrostatic driving at the same frequency and phase may also be applied. Hence, baseband external magnetic fields are then upconverted to the current frequency by means of the Lorentz force, making the structure suffer an oscillation with an amplitude A_z than can be derived from (1.5)

$$A_z(f_r) = \frac{Q}{k}(F_L + F_E) \approx \frac{Q}{k}\left(I \cdot L \cdot B + Vv\frac{C_s}{g}\right) \tag{1.6}$$

where $Q = \sqrt{k\,m}/b$ is the device quality factor. Then, the capacitance variation ΔC_s due to the displacement in (1.6) can be obtained

$$\Delta C_s = \frac{\epsilon_r \epsilon_0 A}{g} - \frac{\epsilon_r \epsilon_0 A}{g + \frac{Q}{k}\left(I \cdot L \cdot B + Vv\frac{C_s}{g}\right)} \tag{1.7}$$

where A is the device equivalent capacitor area, ϵ_r is the air relative permittivity, and ϵ_0 is the absolute permittivity. When the MEMS sensor has a non zero dc voltage, the variation of the device capacitance due to both the current I and electrostatic v drivings generates a current $i_s = dq(t)/dt$

$$i_s \approx \frac{\epsilon_r \epsilon_0 A Q}{g^2 k} V \omega_r \left(\underbrace{I \cdot L \cdot B}_{\text{signal}} + \underbrace{Vv\frac{C_s}{g}}_{\text{offset}}\right) \tag{1.8}$$

as consequence of charge movement that is sensed by the readout electronics connected to the stator electrode as depicted in Fig. 1.3.1. Its sensitivity to magnetic field is

$$S_{AM}(B) = \frac{\partial i_s}{\partial B} = \frac{V \omega_r \epsilon_r \epsilon_0 A L Q}{g^2 k} I_{rms} \tag{1.9}$$

that is proportional to driving current and dc voltage, parameters that can be tuned on the manufactured MEMS. Moreover, the amplitude of the inertial mass displacement is further amplified by the effect of the quality factor. As a consequence, devices intended for AM readout are designed with large Q factors in order to increase sensitivity.

AM modulation has various disadvantages. First, given that bandwidth is inversely proportional to device Q, sensors with a very limited bandwidth are reported in [49,77,79]. Second, if only current

driving is applied to the device, when external magnetic field is very low, so does the output signal. In resonant sensors, this means that the Phase-locked loop (PLL) or the loop closed around the device to track its resonance frequency may lose locking as the carrier signal is too weak to be detected. As a consequence, magnetic field inversion may not be correctly detected, as well as the sensor being unable to work under certain conditions. This problem appears, of course, in closed-loop systems with a self-sustaining oscillation where the device fixes the loop resonance frequency. Open loop operation has been found in the literature, mainly with the objective of characterizing a device [4, 80, 81], but it is not a feasible solution for unsupervised solutions, as resonance frequency is a function of device damping, that changes with temperature.

In order to avoid this issue, in addition to the current driving, these devices are also electrostatically driven. Doing so, there is always a carrier at the resonance frequency, which allows the loop to work unconditionally. However, this carrier causes a large offset, whose drift along time is a cause of low frequency instabilities. Various solutions have been proposed to minimize the offset due to this carrier. On one hand, Horsley et al. have proposed current chopping [79] and bias chopping [44] strategies. These consist in upconverting the magnetic field signal to a frequency close to the resonance frequency $f_r - \Delta f$ but still within the device bandwidth. Doing so, the oscillation sustaining and offset generating signal at the mechanical resonance f_r is not added to the sensed signal. Then, a two step demodulation is required. First, with a mixing signal at f_r frequency. And then, after a low-pass filtering that filters out the offset component, a demodulation to baseband. These strategies, however, increase the power due to the need of a two step modulation. Moreover, effective bandwidth is halved, further reducing the bandwidth.

Another solution has been first proposed by Langfelder et al. consisting in off-resonance operation of the device [82–86]. This off-resonance operation consists in driving the sensor current at a frequency below the device mechanical resonance. Doing so, -3 *dB* bandwidth is importantly increased, as the device response is much flatter than when working at resonance. Moreover, signal is away from offset, and device variations are minimized. The price to pay is the reduction of the signal amplitude detected by the amplifier, but device Signal to Noise Ratio (SNR) remains unchanged, as noise and signal suffer the same gain reduction. However, amplifier SNR does not, which requires a more sensitive amplifier, increasing current consumption. Contrarily to most AM solutions, off resonance allows open loop driving, given that the system does not need to track device resonance frequency. This open loop driving is used in [85] to drive three sensors simultaneously with the same electronic circuitry by putting their current carrying paths in series, no matter if resonance frequency of each of them changes differently due to temperature, process variations, etc.

1.3.4.2 Frequency Modulated readouts

Frequency modulation strategies have been proposed in order to boost the sensor bandwidth beyond the limitation that poses a high quality factor [46, 53, 68, 69, 87–91]. Besides, an improved sensitivity stability over temperature can be obtained as sensitivity is not directly a function of Q, which varies with temperature [88], as well as an improved linearity because a fixed oscillation amplitude avoids nonlinearities that may arise with large oscillation amplitudes [89]. Furthermore, such strategies can be implemented in a low power fashion as conversion to the digital domain of the sensor data is more straightforward.

Frequency modulated readout circuits consist of a closed loop circuit where the sensor works as the resonator in a self sustaining oscillation. Once the loop is resonating at the sensor resonance frequency, the displacement of the movable plate generates a strain in the beams that change their

spring constant k, modulating frequency as a function of the external magnetic field [92].

$$f_r = \frac{1}{2\pi}\sqrt{\frac{k_{eff}}{m}} \tag{1.10}$$

where k_{eff} is the effective spring constant and m is the movable plate mass. In this readout strategy, the quality factor has less importance and, as a consequence, its value does not need to be boosted in order to improve sensitivity and resolution, even though a high Q helps to distinguish the signal from the noise [46]. In order to modulate the spring constant of the sensor as a function of the magnetic field, two different strategies have been proposed in the literature: 1) to generate an axial stress at the sensor springs and 2) to perform a quadrature frequency modulation (QFM).

Axially stressing the sensor springs [53, 69, 90] consists in applying a dc current to the sensor once it works in a self-sustained oscillation. Then, an external magnetic field generates a Lorentz force that twists the lever arms at dc. This twist applies an axial load to the beam resonator, shifting its resonance frequency by changing its effective spring coefficient and, thus, the resonance frequency. Axial stress sensors need a simple actuation circuitry as dc Lorentz current is used, but several disadvantages arise during the design of the device. First of all, sophisticated structures are required, with long beams to boost sensitivity. And second, these long beams increase resistance and Joule heating of the device.

On the other hand, QFM strategy consists in driving the sensor with a current at the same frequency of the electrostatic driving signal but shifted 90° in phase (in quadrature) [46, 87, 89]. Doing so, spring stiffness k changes with the magnetic field because the Lorentz force applied is in phase with the displacement (x) of the mass as shown in the resonator second order equation of motion

$$m\ddot{x} + b\dot{x} + (k - \underbrace{BA_IL}_{F_L})x = F_E \tag{1.11}$$

where b is the damping coefficient, k is the nominal spring constant, $A_I = I/x$ is the current gain, L is the effective length of the Lorentz force generation and F_E is the electrostatic force that drives the sensor into the self sustaining oscillation. Hence, MEMS resonance frequency from (1.10) is

$$f_r = \frac{1}{2\pi}\sqrt{\frac{k - BA_IL}{m}} \tag{1.12}$$

And the sensitivity, as derived in [89]

$$S_{FM}(B) \approx \frac{A_IL}{4\pi\sqrt{mk}} \tag{1.13}$$

where the approximation $k \gg BA_IL$ has been applied.

The main problem of FM modulated devices is that they present lower resolution than most AM modulated sensors and high noise floors.

1.3.5 MEMS magnetometers system architectures

System architectures used to perform the readout of magnetometers data is a topic that has been strongly related to the modulation strategies used and the purpose of the measurements. A good example of the latter are works that use open loop driving of the resonant sensor as a simple architecture that allows the characterisation of the MEMS devices [4, 80, 81]. These examples are not covered in this section.

Works using FM require driving the sensor in a self-sustained oscillation loop where the magnetometer sets the loop oscillation frequency. Good examples of that are [46, 89, 90], even though the

different blocks that make up the loop differ from work to work. For example, [46], after the first amplification stage, the loop is divided into two branches, each one processing the signal for current driving or electrostatic driving (thermal loop in the article). Loop in [90] has only one branch as current is applied in dc to axially stress the device beams. Finally, [89] makes use of two branches, where the current branch incorporates a 90° phase shifter in order to perform signals quadrature for QFM. These works are good examples of how different modulation and driving strategies make use of loops with similar blocks: amplification, low-pass filters (either in the form of a filter or a PLL), voltage and current limiters, and some kind of phase adjustment or control.

AM systems have more variety. First, closed loops for self sustained oscillation are used with topologies similar to the FM counterparts [76, 79]. However, [79] is slightly different: while electrostatic driving is made with a simple closed loop, current driving has an extra modulation step in order to perform the current chopping technique. Second, some AM works do not require, due to their characteristics, a closed loop so they can operate in open loop. These are the works driving the sensor in off-resonance [44, 82, 84, 85]: given that a frequency tracking is not a must, electronics can be simplified. Here it is worth to mention a few works. In [44], off-resonance is used in order to implement bias chopping with the objective of reducing the sensor offset. In [84] the frequency reference is generated with an off-chip resonator that feeds the on-chip current driving stage. Similarly, an integrated resonator is used in [85] as the reference of a single Howland current source for three different sensors, each of them having its own integrated amplifier. The main drawback of these topologies is the added complexity of generating the oscillation frequency.

Finally, two interesting works are [78, 91], where simple closed self-sustained oscillation loops are used to perform QFM and AM respectively. In both works, two identical sensors with identical electrostatic driving are used. The difference is that only one sensor has current driving, obtaining a differential measurement both in FM and AM that allow the offset removal and temperature compensation.

1.3.6 Back-End-Of-Line for MEMS-electronics co-fabrication

Most of the older references in section 1.3.3 make use of the silicon substrate to fabricate their MEMS sensors, commonly known as bulk micromachining. Later, surface micromachining was proposed to manufacture the MEMS devices by depositing the MEMS structural materials on a silicon or SOI wafer. These materials, are later selectively etched to release the MEMS. These technologies, though, require complex manufacturing processes and structure release [93]. Only few works have been reported where the MEMS structures are manufactured making use of the Back-End-Of-Line (BEOL) part of the standard CMOS manufacturing process. The BEOL manufacturing part consists in a set of metal layers and vias used for the interconnection of the electronic components on a chip. Concretely, the metal interconnection layers are made of Aluminium, while vias are mainly made of Tungsten [73].

The first MEMS making use of BEOL is [5], which was manufactured and later maskless released with a standard 2 μm CMOS process. Device in [50] makes use of polysilicon and 3 metal layers and their interconnections of a TSMC 0.35 μm process to make up the MEMS. A similar cross section is used in [94] with different process. In [95], not only magnetometers, but also accelerometers where designed using the BEOL part and using some layer present in the process as etching masks. In [63], a complex structure was designed using the BEOL part of the standard TSMC 2 Poly-4 Metal 0.35 μm. The main drawback of all of these sensors is that they require to etch some part of the bulk in order to release the MEMS structures.

In this thesis, the use of CMOS-MEMS for the development of magnetometers is proposed, where the MEMS devices are manufactured only using the BEOL part of a standard CMOS process. This means that both the stator and the rotor of the MEMS magnetic field sensor are designed using the

metallization of the BEOL. This allows an easy post-process consisting of either dry or wet etching with the purpose of etching away the silicon oxide that surrounds the metallizations. No silicon or other materials are etched and a single etching process is required. The two etching processes work as follows. Dry etching consists in the use of vapor hydrofluoric (vHF), which provides good metal to silicon oxide selectivity. This process has been previously used by the research group [96,97]. On the other hand, wet etching consists in the use of Silox-Vapox III, which is a commercial product from Transcene Inc. containing a hydrofluoric acid buffered solution as main etchant. Again, Silox-Vapox III has been successfully used by the research group at the university cleanroom [98–102].

For more details on the various MEMS manufacturing strategies, the reader is encouraged to read [103], which is a fantastic review of the state of the art. Also, [104] is an interesting reference to know more about the research group wet etching procedure.

Chapter 2

Amplitude modulated magnetic field sensor with off-chip readout electronics

2.1 Introduction

In previous section the state of the art of MEMS devices, and specifically, MEMS magnetometers have been explained [49,57,68,79]. Also, some words have been said regarding the integration of the MEMS structures using the BEOL part of the CMOS manufacturing process and their release from the surrounding SiO_2 [96,97,99,104,105]. Once these challenges have been faced and solved, there still exist important aspects to take into account if MEMS magnetometers are to be introduced in the market. First, the design of readout systems for resonant MEMS sensors such as Lorentz force magnetometers, which require to run at the resonance frequency in order to obtain a maximum sensitivity. To do so, closed-loop with phase locking is needed. Second, offset minimization is a key parameter as well.

In this chapter, a mixed-signal closed-loop control system for Lorentz force resonant MEMS magnetometers is presented. The control system contributes to 1) the automatic phase control of the loop, that allows start-up and keeps self-sustained oscillation at the MEMS resonance frequency, and 2) output offset reduction due to electrostatic driving by selectively disabling it. The proposed solution proof-of-concept has been tested with a Lorentz force-based MEMS magnetometer. The readout electronic circuitry has been implemented on a printed circuit board with off-the-shelf components. Digital control has been implemented in an Field-Programmable Gate Array (FPGA) coded with VHDL.

2.1.1 Phase locking

Given that MEMS magnetometer driving is performed at the mechanical resonance frequency, which changes with temperature, it is of utmost importance to track it in order to get maximum and constant gain. To do so, various strategies have been found in the literature. In [44, 79] digital lock-in amplifiers are used to close the loop. This solution has been used as a proof-of-concept of the modulation strategies proposed, but it requires bulky commercial devices that can not be integrated on a chip. In [84] a Pierce oscillator coupled to an off-chip Tang resonator has been used to track the resonance frequency. This solution requires off-chip components and does not provide resonance frequency tracking with temperature variations. Similarly, in [85] an on-chip Tang resonator was especially designed for this purpose. Even though it proved to track the resonance frequency with

temperature variations, it requires extra design effort and the use of important chip area. Another approach is to set the MEMS magnetometer in a self-sustained oscillation by placing it in a closed loop with an overall 0° phase. In this case, the MEMS resonator works as an LC tank, setting the loop oscillation frequency to its resonance frequency. This strategy is used in [46, 90] with low phase-noise and good frequency stability. However, manual phase adjustments are required, which are not acceptable for high-volume applications. The same strategy was used in [76], but a low frequency stability may be expected when output signal is low due to unfiltered wideband noise. In this work, a robust self sustained oscillation loop implemented in the digital domain is proposed. This adds flexibility to the signal processing and provides a low power consumption compared with analog strategies given that digital circuits may be driven with a lower supply voltage. Moreover, phase adjustment has been implemented, which allows to automatically tune the phase for each device, making it Process-Voltage-Temperature (PVT) variation tolerant.

2.1.2 Offset minimization

In some cases, electrostatic driving is also used in order to keep the self-sustained oscillation when the sensor output signal is low. When frequency modulation techniques are used, where the amplitude of the sensor output does not carry information, having such high output signals is not problematic unless they carry extra phase noise [89, 90]. When magnetic field is amplitude modulated, though, electrostatic driving feedthrough introduces an important amount of offset that must be removed [44, 79]. In order to avoid this offset, some works do not drive the MEMS electrostatically and track frequency with on- and off-chip oscillators [84, 85], but requiring extra area consumption and design time. In [79], current chopping is proposed to get rid of this offset, but magnetic field requires an extra modulation step, which increases power consumption. Given that electrostatic driving is not necessary to perform an AM in current-driven Lorentz force magnetometers, it may be disabled when the output signal is large enough to sustain oscillation. For example, when the sensor suffers hard iron effects or when it is measuring large magnetic fields. Then, when this signal is low, such as when measuring small magnetic fields, it could be enabled again. In this work, an electrostatic driving control system is proposed, enabling it when sensor output is dangerously low to sustain oscillation, and disabling it when hard-iron effects are present or large magnetic fields are measured. Doing so, offset can be greatly minimized in some cases and the range of maximum measurable field is increased.

2.2 Device description

The MEMS magnetometer used in this part of the thesis was designed by Mr. Juan Valle as part of his PhD. It was built using the BEOL metal and oxide layers of a Global Foundries (GF) 6-Metal 0.18 μm CMOS-MEMS process [96, 97]. Vapor hydrofluoric (vHF) acid, which provides both good metal to silicon oxide selectivity [106] and uniformity [96], was used to release the MEMS structures by etching the sacrificial oxide at wafer-level. The passivation layer was modified by the foundry to be vHF resistant by increasing its silicon content [96, 107]. It was then used as a masking layer during the release process, protecting the regions that were not to be etched. Passivation windows were open in the MEMS areas to allow vHF penetration and subsequent sacrificial oxide removal. After the release, the devices were vacuum sealed at $1 - 10$ $mbar$ approximately using a thin Aluminium sputtered layer that covered the MEMS magnetometers. Finally, the wafers were diced and the devices wire-bonded in QFN packages.

Many Lorentz-force magnetometers have a single current-carrying wire. However, the Lorentz-force magnetometer used in this chapter is formed by 20 parallel current-carrying wires, so the current needed to achieve a given sensitivity is significantly reduced. A simplified diagram of

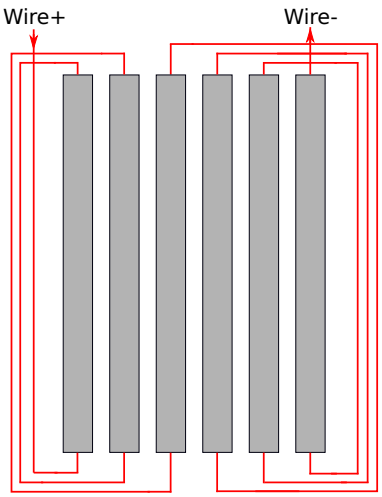


Figure 2.2.1: MEMS magnetometer Wire structure sketch.

the current-carrying wires is depicted in Fig. 2.2.1. Firstly, ten clamped-clamped cantilevers are mechanically coupled so they resonate at a single frequency. Secondly, two parallel current-carrying wires run along each cantilever. In addition, in order to further improve sensitivity, the clamped cantilevers are designed as long as possible (600 μm), without jeopardizing their mechanical reliability. This allows to both minimize the system stiffness and to maximize the Lorentz-force, linearly dependent on cantilever length. The sensing electrodes are disposed on the side of the clamped-clamped cantilevers, so the capacitance changes only when there is lateral movement in first approximation. Lateral displacement is only caused by an out-of-plane magnetic field, which is perpendicular to the Lorentz current. Therefore, the tested magnetometer is single-axis as it detects magnetic field only in the out-of-plane direction.

The sensing gap between rotor and stator is $g = 0.5\ \mu m$ and the total sensing area is around $A \approx 30000\ \mu m^2$. The approximate system stiffness is $k \approx 175\ N/m$, referred to an uniform load and the displacement at the central part of the cantilever. The resonating bridges were made of a combination of oxide and metal layers 2, 3, 4, and 5.

Finally, it is important to note that the current-carrying Lorentz wires were completely surrounded by a single metal electrode which acts as an electrical shield and as the external part of the clamped-clamped cantilever [74]. This way, the changing electrical potential of the Lorentz wires can be isolated from the sensing electrodes, greatly simplifying interference filtering. In the electronic domain, depicted in Fig. 2.3.2, it means that Wire and Sense nodes parasitic capacitance is virtually 0 fF, even though it was measured to be 30 fF after packaging.

As depicted in Fig. 2.3.2, the sensing electrode connected to the driving circuitry has been named Shield because it is also connected to the shielding structure of the current carrying wires. Sensing electrode connected to the amplifier is referenced as Sense. Finally, the electrodes giving off-chip access to the sensor current carrying wires will be named Wire+ and Wire-.

2.3 Sensing electronics

The proposed system block diagram is shown in Fig. 2.3.2. A series of printed circuit boards (PCB) has been designed in order to implement a modular system and perform the measurements. The boards have been designed with the same form factor of the microcontroller board that provides connectivity with the host computer: Arduino Due [108]. The stack of boards is shown in Fig. 2.3.1 and it consists of: 1) Arduino Due, that communicates with the FPGA using I^2C protocol and

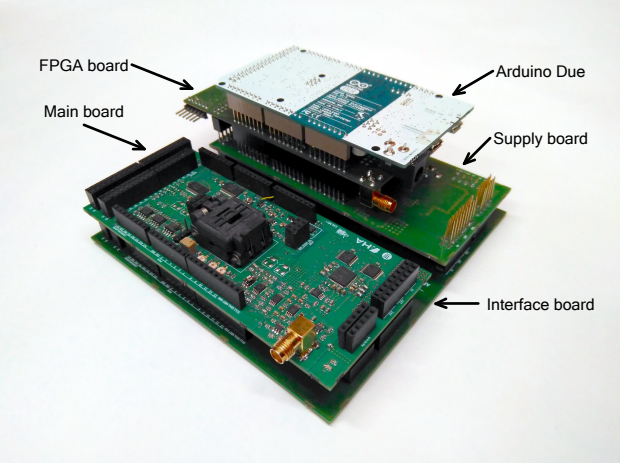


Figure 2.3.1: Stack of designed PCBs.

reads data from the commercial reference magnetometer LSM303C (from ST) and thermometer LM95071 (from Texas Instruments), 2) Supply board, that contains DC-DC converters and linear regulators to generate the needed voltage rails, 3) FPGA, used to read the Analog to Digital converter (ADC), control the Digital to Analog Converters (DAC) that generate the electrostatic and current drivings and the loop necessary digital blocks, 4) the main board, where the MEMS under test has been placed within a clamp-type socket, as well as the readout circuit, and 5) an interface board, that is used to separate the Arduino and FPGA boards from the sensor in order to minimize digital noise.

Given that the readout electronics has been implemented off-chip, PCB has been accurately designed to cope with the associated limitations. First, Sense node has been routed as short as possible to minimize this node capacitance, which increases Low Noise Amplifier (LNA) noise [109]. Second, this node has also been shielded with ground in order to minimize noise pickup of this high impedance node. And third, even though the device has the current carrying Wires shielded, packaging and PCB routing add some Wire to Sense parasitic capacitance. For this reason a block has been designed to compensate this parasitics.

2.3.1 Half bridge

In order to allow single-ended to differential conversion of the sensor signal, as well as reducing feedthrough from the electrostatic driving, a half Wheatstone bridge has been used. This bridge capacitance has been implemented with precision capacitor trimmers. Even though the sensor was designed and packaged to have a very low Wire to Sense parasitic capacitance, socket and PCB routing are expected to create some parasitics. For this reason, a capacitive network has also been designed and implemented in order to reduce feedthrough due to the current driving. Both compensation nets have been connected as the sensor differential capacitance, as depicted in Fig. 2.3.2 and further detailed in Fig. 2.3.3. Adjusting capacitance C_{W-C} allows to compensate the feedthrough due to the current driving. It is worth to mention that CMOS-MEMS integrated designs having the sensor and the readout electronics in the same die area may make this trimming unnecessary: Wire to Sense parasitic capacitance may be importantly reduced by having shorter and shielded nodes.

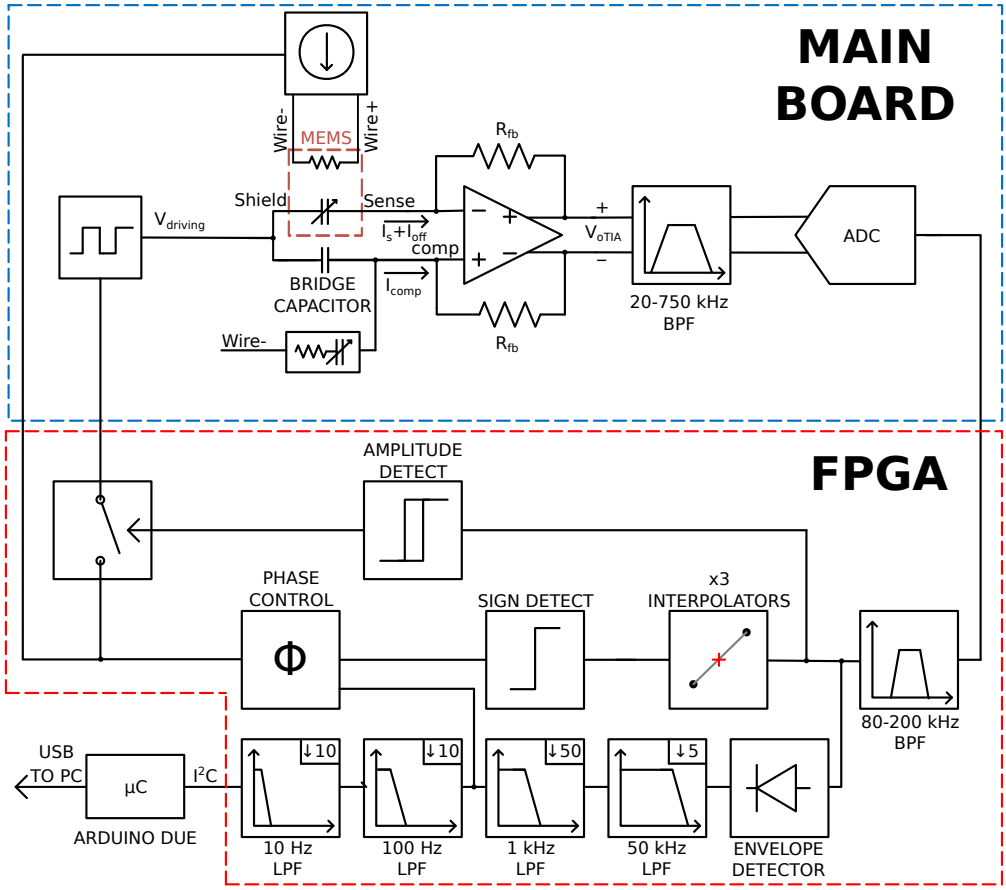


Figure 2.3.2: System block-level schematic.

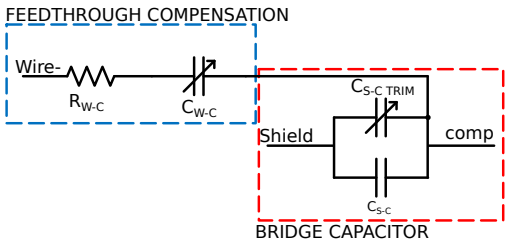


Figure 2.3.3: Wire to Sense parasitic capacitance compensation net (blue box) connected between Wire- and the comp node ("Feedthrough compensation" block in Fig. 2.3.2). Wheatstone half-bridge compensation capacitance (red box) connected between Shield node, where $V_{driving}$ is injected, and comp node, the Sense complementary node in the differential branch ("Bridge capacitor" block in Fig. 2.3.2).

2.3.2 Amplification and filtering

A Transimpedance Amplifier (TIA) has been used to sense and amplify the sensor output current

$$\begin{aligned} V_{o\ TIA}(t) &= R_{fb}(i_s + i_{off} - i_{comp}) \\ &= R_{fb}(S \cdot B + i_{off} - i_{comp}) \end{aligned} \tag{2.1}$$

where R_{fb} is the TIA feedback resistance, i_s is the sensor current in (1.8), i_{off} is the offset due to current driving feedthrough depicted in Fig. 2.3.2, and i_{comp} is the current from the bridge capacitor and the current feedthrough compensation network in Fig. 2.3.3. The expression is also shown as a function of sensitivity S in (2.1) and the magnetic field B. Next, the signal is filtered using a bandpass filter with 20 dB gain. This filter has been implemented with a low-pass and a high-pass multi-feedback filters in series. This topology has been preferred over a bandpass filter due to the high phase variation in the pass-band of high order band-pass filters. Next, an ADC

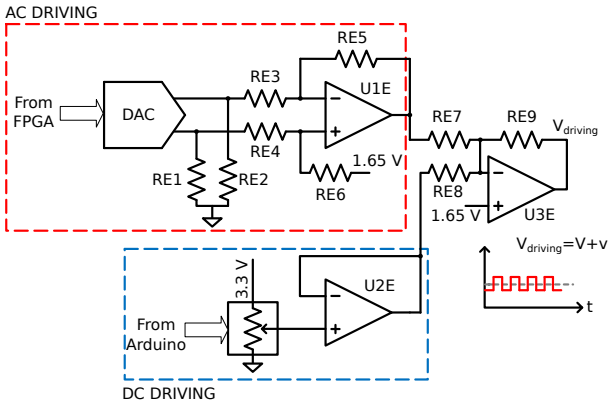


Figure 2.3.4: Electrostatic driving schematic ("Electrostatic driving" block in Fig. 2.3.2).

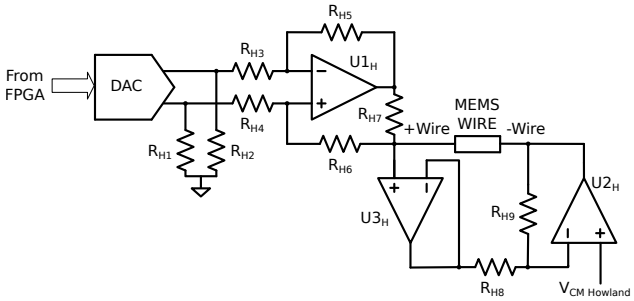


Figure 2.3.5: Current-driving block for the MEMS Wire, based on an improved floating Howland current source [111] ("Current driving" block in Fig. 2.3.2).

working at 5.55 *MHz* sampling frequency digitizes the signal and sends it to the FPGA. Finally, right at the ADC input, a differential to single ended conversion operational amplifier driving an SMA connector has been included for debugging purposes.

2.3.3 Electrostatic and current driving

Sense node voltage is set by the TIA common-mode voltage at mid-supply and Shield voltage is set by a digital potentiometer. A DAC has been used to generate the AC part of the electrostatic driving. AC driving has been designed to be much lower than DC driving in order to make the MEMS device to work in the linear region and to avoid common-mode issues affecting the device gain [110]. Both AC and DC voltages are then added with an operational amplifier (opamp) and driven to the sensor Shield node, as shown in Fig. 2.3.4. An improved Howland floating current source driven by a high speed DAC has been implemented to perform the MEMS current driving, allowing a maximum output current of 5 mA_{rms} [111]. It has been implemented with floating load in order to minimize supply rails noise, and to control the center DC voltage of the signal [57].

2.4 Noise analysis

Implementing the electronics with off-the-shelf components does not allow the best performance due to the various parasitics that appear in the sensor connection with the TIA. From all the components that introduce noise to the system, the following have been considered: the TIA, the Howland current source and the ADC quantization noise as well as the MEMS sensor Brownian noise. Given that the sensor resonates well beyond the noise corner frequency, only white noise has been considered in the analysis.

2.4.1 Sensor thermomechanical noise

Spectral noise density equivalent force for MEMS sensors was described in [112], where MEMS noise is associated with its damping coefficient b. In order to obtain an equivalent output noise current for a force noise, first, sensitivity to a force has been obtained by deriving (1.8) as a function of force

$$S_F = \frac{\partial i_s}{\partial F} = \frac{\epsilon_r \epsilon_0 A Q V \omega_r}{g^2 k} \tag{2.2}$$

Then, (2.2) is multiplied by the noise force

$$\bar{i}_s = \frac{\epsilon_r \epsilon_0 A Q V \omega_r}{g^2 k} \sqrt{4 k_B T b} \approx 1.33 \ pA/\sqrt{Hz} \tag{2.3}$$

where k_B is the Boltzmann constant, $T = 300\ K$ the device temperature, sensing area $A \approx 30000\ \mu m^2$, gap $g = 0.5\ \mu m$, spring constant $k \approx 175\ N/m$, damping coefficient $b \approx 1.5 \cdot 10^{-6}\ Ns/m$, quality factor $Q = 1500$, resonance frequency $f_r = 146\ kHz$, and $V = 1\ V$.

2.4.2 Amplifier noise

The opamp used to implement the TIA is the low noise, low bias current Texas Instruments THS4121 [113]. Only opamp input-referred noise and feedback resistors' noise have been considered. First, from its equivalent input voltage noise $\overline{v_{OA}}$, the equivalent current noise referred to the sensor is

$$\overline{i_{s\ OA}} = \sqrt{2} \overline{v_{OA}} \omega_r (C_s + C_p + C_{U-W-C}) \tag{2.4}$$

where C_p is the parasitic capacitance between Sense node and ground, C_{U-W-C} is the resulting parasitic capacitance between Wire and Sense after compensation by circuit in Fig. 2.3.3, and C_s is the sensor capacitance. Note that the $\sqrt{2}$ factor corresponds to the translation of the differential noise into a single ended noise referred to the MEMS. In this work, C_p is expected to be in the order of tens of pF [85, 110] due to the chip pad, packaging, through-hole socket pin, PCB routing and the opamp input capacitance. Considering a rough estimate of $C_p = 50\ pF$ results in a noise of $\overline{i_{s\ OA}} = 0.368\ pA/\sqrt{Hz}$. Moreover, this is a high impedance node, so even tough PCB tracks have been shielded and accurately routed, through hole socket pads and wire bonding are still prone to noise pick up.

The second important noise source in the TIA are feedback resistors $R_{fb} = 1\ M\Omega$ noise (2.5).

$$\overline{i_{s\ R_{fb}}} = 2\sqrt{\frac{4 k_B T}{R_{fb}}} = 0.257\ pA/\sqrt{Hz} \tag{2.5}$$

2.4.3 Howland current source noise

Howland current sources typically use relatively high value resistances in order to reduce power consumption [114]. Taking into account this limitation for future integrated approaches, in this work resistor values have been kept low (around 10 $k\Omega$) in order to match resistors and opamp noise [115]. Doing so, the dominating noise sources of the circuit in Fig. 2.3.5, which are $U1_H$,

$U3_H$ opamps and R_{H3}, R_{H4}, R_{H5}, R_{H6} resistors are below 70 $pA/\sqrt{Hz}$ at the output of the Howland circuit. As a consequence, total output current noise of the improved Howland current source is $\overline{i_H} = 163.1\ pA/\sqrt{Hz}$. This current noise is translated in two ways to the sensor output current. First, it is converted to sensor output current noise by means of Lorentz force as described in (1.8), which results in a negligible noise. Second, this noise is coupled to the sensor output current through the parasitic capacitance between Wire and Sense nodes which results in a noise feedthrough directly to the Sense node. Even though the exact value of this capacitance is unknown, a rough estimate of $C_{U-W-C} < 2\ pF$, together with MEMS current carrying wires resistance of around $R_{Wire} = 3\ k\Omega$, results in an output noise of

$$\overline{i_{s\ Hpar}} = \overline{i_H} R_{Wire} 2\pi f C_{U-W-C} < 0.90\ pA/\sqrt{Hz} \tag{2.6}$$

2.4.4 Quantization noise

Quantization rms noise due to the analog to digital conversion [116] can be expressed as sensor equivalent output noise by dividing it by the gain stages of the amplification chain. In this case, gain is a transimpedance $Z_C = 10\ M\Omega$ which accounts for the TIA transimpedance and the filters gain.

$$\overline{i_{s\ q}} = \frac{\sqrt{2} V_{LSB}}{\sqrt{12}\ Z_C\ \sqrt{BW}} = 1.33\ fA/\sqrt{Hz} \tag{2.7}$$

where $V_{LSB} = 54.3\ \mu V$ is the voltage of one LSB and $BW = 2.775\ MHz$ is the ADC bandwidth.

2.4.5 Neglected noise sources

The avid reader may have noticed that there are some noise sources that have not been yet considered in the analysis. First of them is electrostatic driving noise. Noise due to electrostatic driving is proportional to the bridge mismatch ΔC that manual trimming imposes. If this trimming mismatch is approximated to $\Delta C = 100\ fF$. The main noise sources of this circuit in Fig. 2.3.4 are the potentiometer (2.8) and the two opamps (2.9).

$$\overline{i_{n\ pot}} = \Delta C \sqrt{4 k_B T \alpha R_{pot}} = 575 \cdot 10^{-9}\ fA \tag{2.8}$$

$$\overline{i_{n\ U2_E,U3_E}} = \Delta C \overline{v_{bufferU2_E,U3_E}} = 700 \cdot 10^{-9}\ fA \tag{2.9}$$

$$\overline{i_{n\ U5}} = \Delta C \overline{v_{bufferOA2}} \tag{2.10}$$

where $\alpha = 0.2$ is the voltage divider attenuation value of potentiometer $R_{pot} = 10\ k\Omega$ needed in order to obtain a dc voltage of 0.65 V from a 3.3 V supply. Moreover, $\overline{v_{bufferU2_E,U3_E}} = 7\ nV/\sqrt{Hz}$ is the opamps input referred noise. Hence, noise from this stage is negligible as far as a good capacitive matching is achieved in the bridge.

The second noise source that has been neglected is oscillator phase noise. Phase noise is a topic that has been largely covered by a wide range of publications, each of them proposing different models and root causes to describe the phase noise of a resonator [117–121]. From the various models, the most widely accepted is the Lee-Hajimiri model [120], which is an improvement of

the old Leeson model [117]. The Lee-Hajimiri model [120] claims that phase noise is due to the upconversion of base-band noise (in our case, amplifier flicker noise) and the downconversion of noise (white noise) at harmonic frequencies of oscillator frequency, the resonance frequency in our case. While upconverted flicker noise results in $1/f^3$ close-in noise, up- and downconverted white noise results in $1/f^2$ noise around the carrier frequency. Moreover, [120] also predicts that upconverted noise is proportional to the signal rise and fall time asymmetry. In our case, though, the use of an off-the-shelf component with sufficient slew rate makes this noise source not a concern. Some years later, van Beek et al published a review in the topic of oscillator phase noise after a frequency translation in [118, 119] among others. They found that phase noise around a given frequency f_1 is scaled when frequency is divided or multiplied to a frequency f_2

$$\Gamma_{f_2} = \Gamma_{f_1}(f) \left(\frac{f_2}{f_1} \right)^2 \tag{2.11}$$

Where Γ is the phase noise. Hence, from eq. 2.11 it can be seen that a downconversion to $f_2 = 0\ Hz$ makes the phase noise negligible.

There may be, of course, some gain noise derived from resonator phase noise due to the fact that quality factor Q is not constant along frequency. However, this noise source has not been observed in the experimental results.

2.4.6 Total expected noise

With the noise figures obtained for each sub-circuit, and the measured sensor sensitivity, total noise is expected to be around 171 $nT/\sqrt{Hz}$. It must be taken into account, though, that various approximations have been done during the process, such as Wire to Sense, and Sense parasitic capacitances which have been described throughout the section.

2.5 Digital implementation

The block diagram of the digital part has been included in Fig. 2.3.2. Once the signal is in the digital domain, it is filtered again with a 120 *kHz* bandwidth finite-impulse response (FIR) bandpass filter. Doing it in the digital domain allows the use of more selective filters. Then, the signal follows two paths: the path to demodulation and the path to close the loop. In the first one, the signal is demodulated with an envelope detector followed by four FIR low-pass filters of 50 *kHz*, 1 *kHz*, 100 *Hz* and 10 *Hz*. The purpose of applying four filters is twofold. First, by decimating the signal, the filters can be designed to have a lower set of coefficients, being more area efficient. Second, the 1 *kHz* filter output is used by the phase control block, while the 10 *Hz* filter output is stored in the registers of an I^2C slave block before being sent to the processor.

In the second path, i.e. the path to close the loop, the signal is used to generate a clock at the same frequency that is injected back into the device to achieve phase locking in the loop and sustain oscillation. After the bandpass filter, the signal is interpolated with three cascaded linear interpolators. These interpolators have two objectives. First, given that during zero crossing, signal is expected to have the highest slope, each interpolator improves the resolution of the zero-crossing detector by a factor of two, improving time resolution of zero-crossing detector from 180 *ns* (sampling period) to 22.5 *ns* when assuming a linear signal. Second, increasing the number of samples per period also increases the resolution of the phase adjustment by reducing the minimum phase step.

Next, a zero-crossing detector is implemented by taking the sign bit of the two's complement

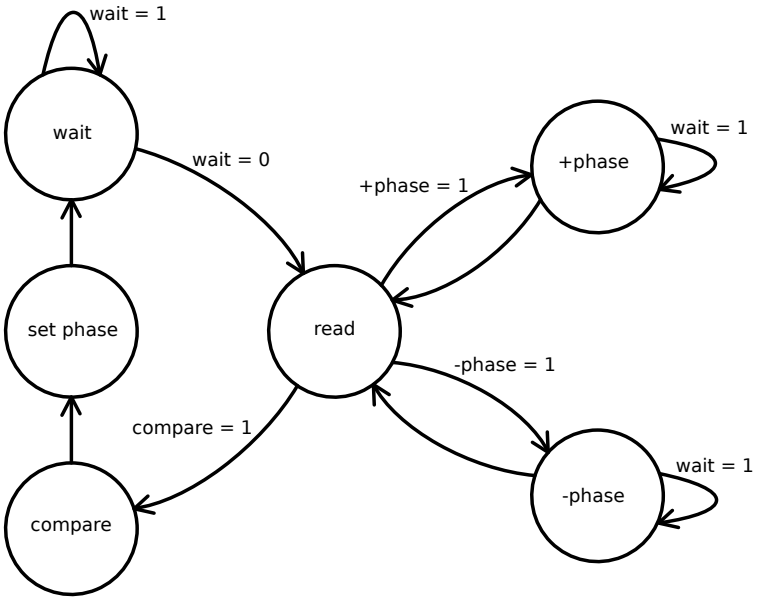


Figure 2.5.1: Phase control state diagram.

signal. Zero-crossings of the signals are used to generate a square signal that tracks the MEMS resonance frequency. This square signal is introduced to the phase control block, a 1024-bit shift register that is used to adjust the signal phase prior to using it to drive the sensor. The phase control block points to a shift register position. Changing the register position read changes the output signal phase, and thus the overall loop phase. This strategy to adjust phase and close the loop, though, has a drawback. Given that oscillation frequency changes with temperature, so does the phase step between two consecutive shift register bits. As an example, consider that the MEMS resonates around $f_r = 146$ *kHz* at $35°C$ while having a temperature frequency coefficient of -200 $Hz/°C$. With a sampling frequency of $f_{sampl} = 5.55$ *MS/s* and three interpolators ($\times 8$ interpolation), a single period uses $8f_{sampl}/f_r = 304$ consecutive bits of the register, having a phase resolution of $360°/304 = 1.184°/bit$. Now, if temperature decreases $10°C$, resonance frequency would increase 2 *kHz* and use 300 consecutive register bits. This means that phase resolution would be $1.200°/bit$. As a consequence, if the shift register bit read is kept unchanged, in this case of a 1024-bit shift register, in the worst case (this is, reading the 1024^{th} bit), phase error can be up to 16.4°, that would be observed with an important reduction of the output signal. Possible solutions may be reducing the length of the shift register in order to allow space only for a single period. However, in order to allow measurements in all the temperature range of, for example, automotive applications ($-40°C$ - $125°C$), register may only be reduced to 512 bits, being the higher temperature (with the lowest resonance frequency of 128 *kHz*) the limit. On the other temperature limit, this is, when resonance frequency is maximum, the number of samples per period would be minimum and hence the phase step would be maximum. In this case, a small temperature variation will have an increased impact in phase. The phase error $|\phi_\epsilon|$ associated with a variation in temperature if the register bit reading remains unchanged can be expressed as

$$|\phi_\epsilon| = \frac{360° N TC_f}{2^M f_S} |\Delta T| \tag{2.12}$$

where N is the read shift register position, TC_f is the resonance frequency temperature coefficient, f_S is the sampling frequency, M is the number of interpolators and ΔT is the temperature difference. For this reason, a periodic phase adjustment is necessary. This phase issue may not be found in systems implementing a PLL instead. However, in case of using a PLL other difficulties such as complexity, design time and power consumption would arise.

MEMS phase at resonance frequency is 0°, while at lower frequencies it approaches to 90° and at higher frequencies it goes to −90°. If the phase of the other loop blocks is also 0°, the entire loop, comprising the electronics and the MEMS, would be locked at that phase and the device would work at resonance. In this situation, output amplitude is maximum. If loop phase deviates from the ideal value of 0°, the device would work at a shifted phase and its amplitude would decrease. For this reason, the phase control block operates with the principle that when the correct phase is set, output signal is maximum. This block has two modes of operation: 1) Burst mode and 2) normal mode. In the burst mode, the phase is not locked (for example, during start-up) and the phase adjustment is performed at high speed. In normal mode, the phase is already locked but it is checked anyway in case some thermal or mechanical variation has made the loop phase to change. In both cases, the same algorithm is run, depicted in Fig. 2.5.1. The states in the diagram are:

- wait: the system is measuring and phase adjustment is stopped.
- read: in this state, 8 samples of the filter output data are read, averaged and stored. In order to provide a trade-off between noise data and phase adjustment speed, the signal read by the algorithm is the 1 *kHz* LPF output signal. Doing so, after each data change settling time is much shorter than taking signal from the 10 *Hz* output filter.
- +phase: increments output phase and waits until filter output signal settles. The increment is made by increasing the shift register read address. In normal mode, steps are unitary while in burst mode the increment is 8 register positions.
- -phase: same as the previous state but in the other direction.
- compare: this state compares the three stored samples and decides which phase provides the higher output.
- set phase: new phase is set.

In burst mode, phase is checked every 20 *ms* and no averaging is performed as a fast phase locking is preferred over accuracy. Here, the main time limiting factor is the filter settling time. In normal mode, phase adjustment is made every 30 *ms*, even though slower adjustment can be made.

2.5.1 Inversion and amplitude control

To the best of our knowledge, with few exceptions [84, 85], articles found in the literature with closed-loop sensing permanently drive the sensor with both current and electrostatic driving. While the first is indispensable to generate the Lorentz force and detect magnetic field, the second can be disabled if signal at the output of the bandpass filter is large enough to allow the zero-crossing detector to work properly. In this system, electrostatic driving is selectively enabled when signal is dangerously low to keep oscillation working, while it is disabled if output signal increases, resulting in an offset reduction and range increase. This electrostatic driving control has been implemented digitally with some hysteresis as shown in Fig. 2.5.2. Furthermore, it is depicted in Fig. 2.3.2 named as "Amplitude detect". The algorithm works as follows: at start up, electrostatic driving is enabled by default. During operation, the algorithm is aware of the output signal value. If the signal is larger than an upper threshold, then electrostatic driving is switched off, making signal to still be large enough to sustain oscillation again. On the other way around, if output signal is low enough to reach the lower threshold, it means that output magnetic field makes output signal low enough to sustain oscillation without electrostatic driving. When electrostatic driving is disabled, both because output magnetic field is positive or negative enough, two new thresholds are set in order to enable again electrostatic driving if necessary.

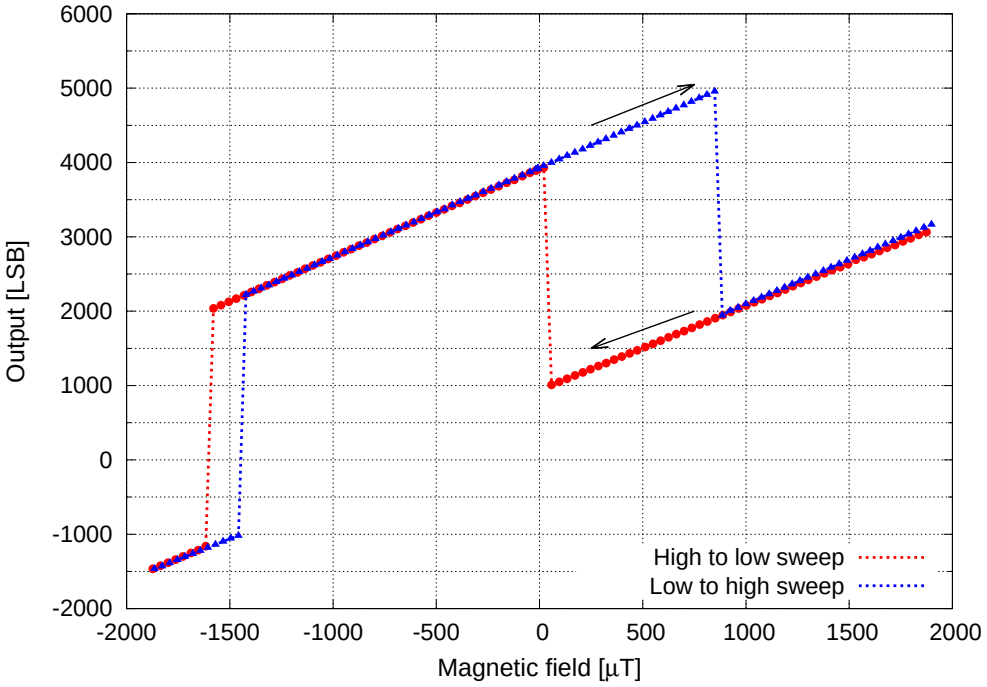


Figure 2.5.2: Raw data output in LSB after digital processing but before offset compensation. Each value is the average of 8 measurements. It is possible to observe the offset added when electrostatic driving is enabled.

2.6 Experimental results

In order to perform the measurements, the sensor was placed inside a custom Helmholtz coil. Sensor voltage biasing was set to 1 V and electrostatic driving rms amplitude, when enabled, was set to 6 mV_{rms}. Temperature has not been controlled during measurements, but few hours have been left between start-up and measurements in order to allow temperature to settle. Moreover, a custom Faraday cage has been user to shield external noise and interferences as well as keeping temperature stable during measurements.

2.6.1 Sensor sensitivity and offset

Magnetic field sweeps were performed for various driving currents ranging from 50 μA_{rms} to 300 μA_{rms}. From this data, the sensor sensitivity was first extracted, which is shown in Fig. 2.6.1 in $pA/\mu T$ units. As it can be seen, sensitivity as a function of current driving shows a linear response for the values shown, helping to make sure that the final current driving value used in subsequent measurements (300 μA_{rms}) makes the MEMS resonator to work in the linear region.

Sensor offset for the cases where electrostatic driving is enabled and disabled is shown in Fig. 2.6.2. Offset is shown in sensor output current units (pA) and in magnetic field units (μT). Showing the offset in both units helps to identify the offset source and behaviour as a function of driving current. In Fig. 2.6.2a offset with electrostatic driving enabled and disabled increases with the same slope, which suggests that this offset is a consequence of parasitic feedthrough between Wire and Sense nodes. This is demonstrated by the fact that, when offset due to current driving only is suppressed from the offset when electrostatic driving is enabled, it results in an approximately flat line representing the offset due to electrostatic driving only. Given that this driving is constant, so is the offset in current units. Analysing offset in magnetic field units in Fig. 2.6.2b shows that offset due to current feedthrough is 793 μT in all cases, being constant along current driving because both

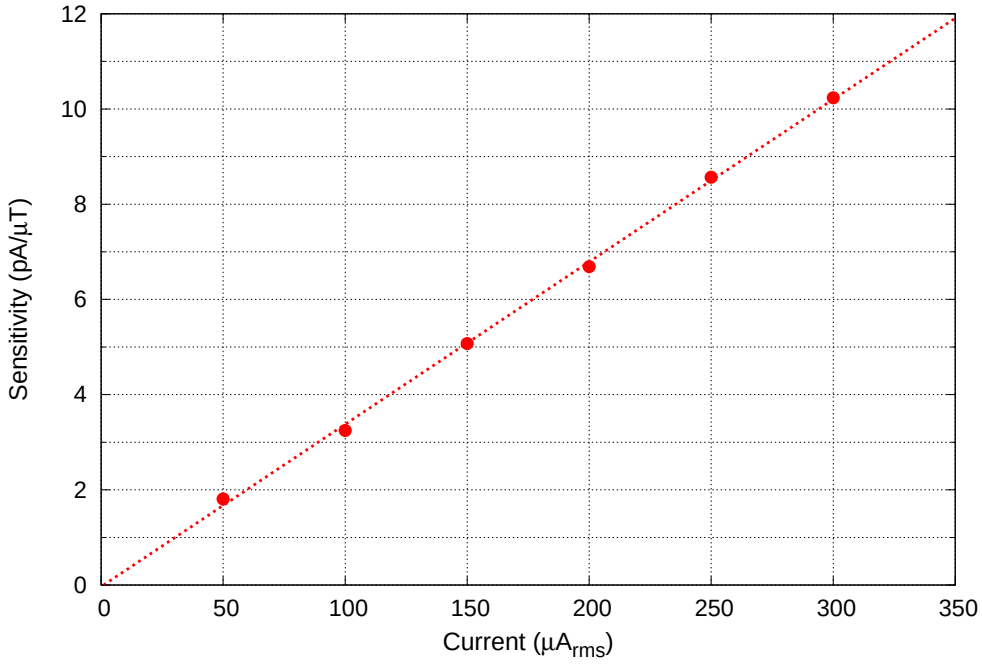


Figure 2.6.1: Sensor sensitivity for currents ranging from 50 μA_{rms} to 300 μA_{rms}.

current feedthrough offset and sensitivity depend on current driving, a dependence that cancels out. Moreover, most offset is due to electrostatic driving. In the best case analysed, i.e. with 300 μA_{rms} and sensitivity $S = 9.75$ $pA/\mu T$, offset due to electrostatic driving is only 1324 μT. In integrated approaches where the sensor and the readout electronics are in the same die area, the Wire to Sense parasitic capacitance would be much lower, which would reduce offset when electrostatic offset is disabled. The same would happen with the electrostatic driving, as trimming bridge differential capacitance with a capacitance bank would allow a finer tuning.

2.6.2 Bias instability and noise

In order to analyse offset instability, Overlapping Allan deviation has been used due to the smoother curve it provides compared with Allan deviation [122]. The Overlapping Allan deviation obtained with the sensor data is shown in Fig. 2.6.3 with measurements made at a sampling frequency of 10 Hz. Offset instability has been obtained from the region where the Allan deviation is flat [123]. When electrostatic driving is enabled, offset instability is 125 nT, with an integration time of 23.4 s. On the other case, when electrostatic driving is not used, offset instability is 104 nT with an integration time of 15.5 s. As it can be seen, in both cases bias instability is similar, and removing electrostatic driving does not worsen this figure.

Noise spectrum density has been used to analyse sensor noise, shown in Fig. 2.6.3 inset. In both cases noise spectrum is almost flat, although in the case when electrostatic driving is enabled, there is some low frequency noise increase. This is thought to be caused by a slow temperature drift during the measurement. In both cases, dominant white noise is 550 $nT/\sqrt{Hz}$, which is larger than the estimated noise in section 2.4. It must be taken into account, though, that various approximations are done during the noise estimation which may be the cause of this 2-3 times mismatch. This is reasonable given that some parasitic capacitances can not be measured, either at the device packaging level and at the chip-PCB interface.

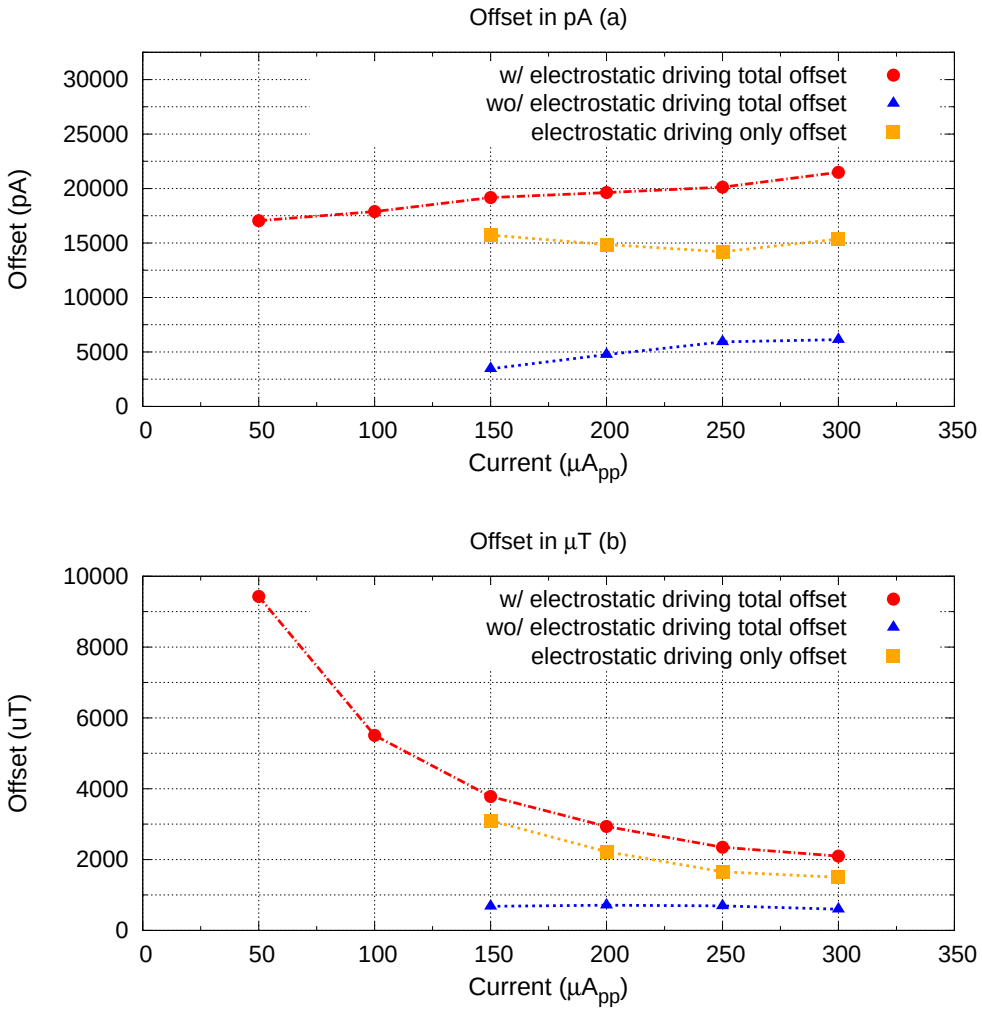


Figure 2.6.2: Sensor offset as a function of current driving in pA (a) and μT (b). Offset with electrostatic driving enabled (red line) is much higher than when disabled (blue line). Electrostatic driving only offset is represented by the orange line.

2.6.3 Sweep and measurement error

Finally, a magnetic field sweep between ± 1 mT with 35 μT steps has been performed in order characterize the sensor. The result is shown in Fig. 2.6.4. Along the measured range, there is a transition around -400 μT between measurements made with the electrostatic driving enabled and disabled. As it can be seen, the nonlinearity at this point is -1.5%. Some nonlinearity is observed when electrostatic driving is disabled. Its main source is thought to be a combination of ADC gain error and MEMS nonlinearity. The latter, though, may be minimized by reducing the driving current: this would reduce sensitivity and, as a consequence, MEMS rotor oscillation amplitude, making the device to work with lower nonlinearity.

In principle, MEMS measuring range is unlimited if current driving is conveniently reduced. A wider magnetic field sweep has been performed with a driving current of 25 μA_{rms} with a maximum measurement range of ± 13 mT, being the Helmholtz coil maximum magnetic field the limiting factor, not the sensor.

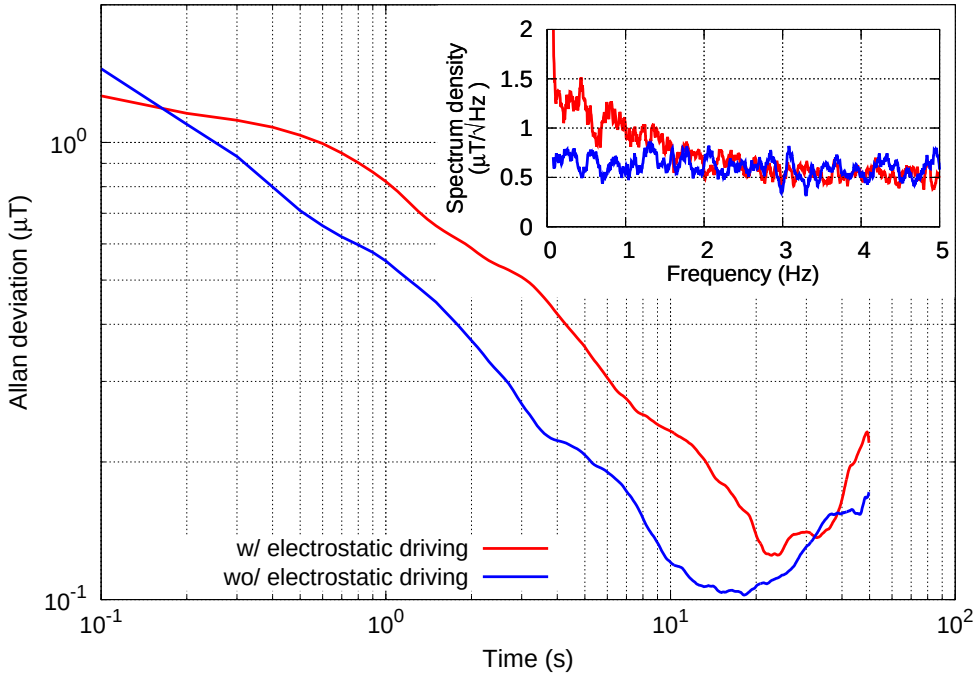


Figure 2.6.3: Overlapping Allan deviation and noise spectral density (inset) of output signal with (red) and without (blue) electrostatic driving.

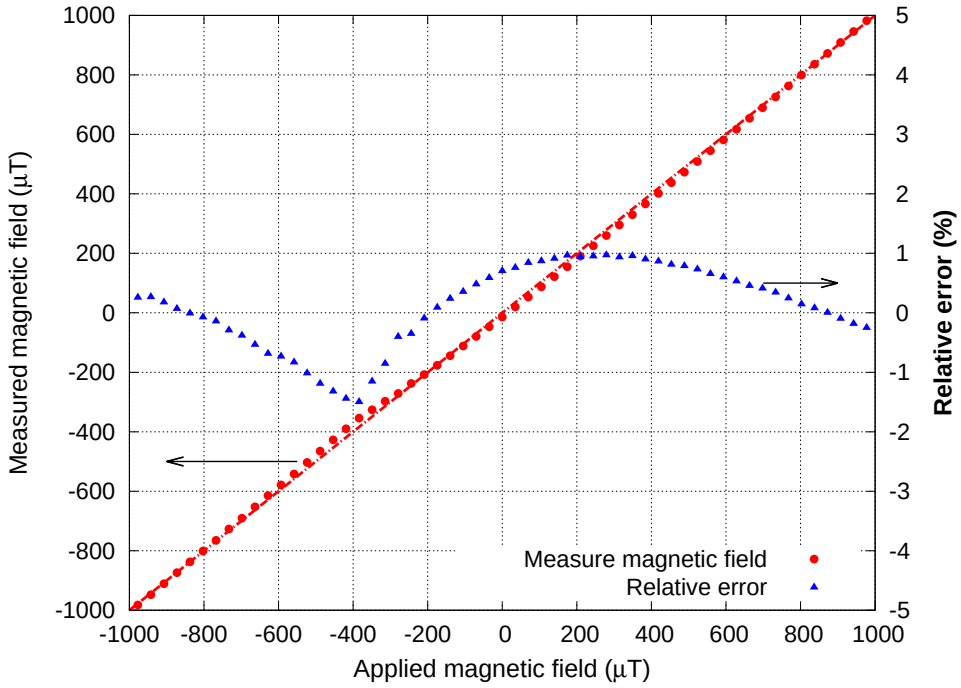


Figure 2.6.4: Sensor measured magnetic field versus applied magnetic field (red) and relative error (blue) for a driving current of $300\mu A_{rms}$. Data shown is an average of 4 samples.

2.7 Comparison with previous works

In table 2.1 the most relevant figures to evaluate state-of-the-art magnetometers have been included from both commercial devices and academic MEMS magnetometers. In order to allow comparison, only MEMS magnetometers with AM output have been included.

Offset is one of the main concerns in any sensor output. For this reason, commercial devices offer offset removal capabilities [16, 41, 124], but its offset tend to be large and unpredictable. Nevertheless, at least in AMR technology, offset is not constant as it changes value if applied magnetic field is larger than a given parameter specified in the datasheet. This offset change was observed with device in [125] that was intended to be used as a reference sensor for this work. This is an important disadvantage, as periodic calibration is required in order to prevent important measuring errors to the end user. Some works [44, 79] propose strategies to reduce offset and improve biasing instability. Such strategies, though, require the use of electrostatic driving, which is an important source of offset itself. Our work presents an analysis of the driving offsets. This knowledge will be very useful during the integration of the MEMS and the electronics in the same die area. Similarly, some works [82,84,85] do not quantify offset, and when they do, it is very low. This is a consequence of not using electrostatic driving, which is the same approach proposed in our work. However, these works use bulky lock-in amplifiers or other instruments to drive the sensor in closed loop, or drive it in open-loop. Hence, our work explores the benefits and disadvantages of using different driving strategies while, at the same time, proposing a resonator loop.

In terms of noise, the best figures in the literature are those in [57, 82]. In both cases, an accurate design of the device results in excellent sensitivities and the lowest noise figures to the best of our knowledge. However, commercial instruments were used to close the loop and perform the measurements, meaning that there is still work to be done until the total integration of the system. Our work shows noise higher than most works, but using relatively low current driving and DC voltage across the MEMS device. This is important because most works use high biasing voltages from 4 V up to 8 V [44, 79, 85]. While this is a way to increase device sensitivity and SNR without increasing power consumption, maximum voltages that the technology can safely withstand must be taken into account. Hence, biasing voltage should be compatible with 3.3 V and even 1.5 V supplies in order to require voltage boosters such as dc-dc converters or charge pumps: while the former needs inductances difficult to integrate on chip, the latter requires large area for capacitors.

As briefly presented above, most works make use of lock-in amplifiers to close the loop and only a few close the loop either on-chip or using electronics on a PCB [46,89,90]. Moreover, no previous works have been found where the loop control and data processing are performed digitally, which is one of the key advantages presented in this work and the first step for the introduction of MEMS magnetometers into the market.

Table 2.1: Comparison of AM magnetometers in the literature

Device	Offset (μT)	Current (μA_{rms})	Biasing (V)	FSR (mT)	Noise ($nT/\sqrt{Hz}$)	Nonlinearity %	Type
LIS3MDL [125]	± 100	270^a	n/a	$\pm 1,6$	$320^{b,c}$	± 0.12	AMR
MAG3110 [16]	± 100	137.5^a	n/a	$\pm 1,0$	250^b	± 0.3	MTJ
AK8963 [7]	± 75	5000^a	n/a	$\pm 4,912$	n/a	n/a	Hall sensor
BMC150 [41]	± 40	4900^a	n/a	± 2.5	300^b	1.0	Flip Core and Hall sensor
[57]	30^d	100	n/a	0.3	10	1.0	MEMS AM
[82]	n/a	300	1	$\pm 2,0$	10	n/a	MEMS off-resonance
[79]	31 (25000^e)	900	4	± 0.4	400	n/a	MEMS Current chopping
[84]	n/a	107	2	$\pm 2,4$	380	2.0	MEMS multi-loop
[85]	2	100	6	± 5.5	200	<0.2	MEMS multi-loop off-resonance
[44]	15 (310^e)	4600	8	± 0.4	70	n/a	MEMS bias chopping
This work	1324 w/, 793 wo/	300	1	± 1.0	550	± 1.5	MEMS with digitally closed loop

[a] Current for highest resolution mode.
[b] Noise is in rms units.
[c] Noise for X/Y axis. For Z axis it is 410 μT_{rms}
[d] Extrapolated from article Fig. 13.
[e] Initial offset.

2.8 Conclusion

In this chapter a mixed-signal processing chain for a Lorentz force based resonant MEMS magnetometer has been presented. The system proposed keeps the MEMS device in a self-sustained oscillation loop at its resonance frequency.

Doing so, loop phase locking is achieved and correct locking can be periodically controlled. Moreover, a strategy to reduce sensor offset has been proposed which allows the system to keep oscillation when the measured magnetic field is low by selectively enabling and disabling electrostatic driving.

The proposed digital system has been coded in VHDL and implemented in an FPGA as a proof of concept prior to its integration in a System-on-Chip. A 550 $n\mathit{T}/\sqrt{Hz}$ total output noise has been obtained with an offset of $793\mu\mathit{T}$ when electrostatic driving is disabled, which represents a 40.1% reduction. However, a better offset figure is expected to be achieved in an integrated implementation.

Chapter 3

MEMS magnetometers experiments: design and characterization

3.1 Introduction

The previous chapter describes the first proposal of a complete readout system for MEMS resonant magnetometers. The system, though, can be considered as a first approximation and proof-of-concept. In order to achieve low noise figures, it is important to minimize parasitic capacitance at the MEMS-amplifier interface [109]. This can be achieved, not only by integrating the MEMS and the electronics in a System-in-Package, but by integrating everything in the same die area. For such purpose, using the CMOS BEOL step to manufacture the MEMS devices is an interesting strategy to lower these parasitics. As a consequence of the noise reduction achieved with integration, both the MEMS magnetometer and amplifier power consumption can be reduced. Moreover, the MEMS and electronics integration in the same die area will also satisfy the low area specifications. To reach this objective, the following two chapters focus on the two different aspects to take into account for such purpose: 1) in the current chapter, MEMS magnetometers are proposed, manufactured and measured to analyse their feasibility for high volume applications, and 2) in the next chapter, the complete integrated system is proposed, consisting of the integrated electronics and MEMS device in the same die area.

For this reason, this chapter focuses on the design, measurement and characterization of various MEMS magnetometers. These sensors have been designed using the metal layers available in the BEOL part of a standard CMOS manufacturing stage. As a consequence, the proposed MEMS magnetometers can be manufactured in the same die area of the electronics, requiring a simple post-process to release them, paving the road to the sensor integration. CMOS-MEMS integration, though, is not a novel idea as there already exist works in the literature that explore CMOS-MEMS sensors [99,100,126,127]. But there is an important lack of study of the feasibility of such sensors in terms on yield and wafer variability. Some approximations of such analysis were reported in [96,97], that may be useful for anybody designing CMOS-MEMS sensors, but there is no data on how wafer variability can affect MEMS mechanical characteristics and electrical performance.

This chapter is a first trial to fill the gaps of missing knowledge in the CMOS-MEMS batch manufacturing. For such purpose, this chapter presents CMOS-MEMS magnetometers manufactured and released using different strategies: 1) devices manufactured in 180 nm TSMC 6 metal layers process and wet-etching release of the mechanical structures at the Electronic Engineering Department of the Universitat Politècnica de Catalunya, and 2) devices manufactured using 180 nm SMIC 6 metal layers process and dry etching of mechanical structures by Memsstar.

3.2 Lorentz force MEMS magnetometers characteristics

There are numerous characteristics that a MEMS magnetometer may or must have depending on the device specifications or final application. In the following sections, some of the most important characteristics taken into account during their design are analysed. At the end of each section, the general characteristics of the proposed devices are presented and justified prior to a deeper description.

3.2.1 Current driving and capacitive driving/sensing electrodes isolation

Unlike other MEMS sensors, MEMS Lorentz force magnetometers require more complex structures (even though all MEMS devices may end up being quite complex due to the metal layers residual stress [128]). This is due to the fact that the MEMS movable plate must have some type of current carrying structure in addition to the driving electrode. The current-carrying structure is required for the current to pass along the plate, which, under the presence of a magnetic field, generate the Lorentz force as previously stated in (1.4). This force, applied to the MEMS rotor, generates a displacement that is then capacitively or resistively sensed. Various solutions have been proposed in the literature regarding this topic. In some works, no electrostatic driving is used, so there is no need to isolate the current driving with the sensing electrode [82, 84, 85]. Other works provide electrostatic driving using a comb-like structure divided into two isolated identical combs: being one part dedicated to driving and the other to sensing [79, 89, 90]. Similar to this approach, some works achieve the electrostatic driving isolated of the current driving, but without using a comb-like structure: in [46] a heating resistor is used, and the device described in chapter 2 has the current carrying path isolated from the driving electrode as shield and wire nodes are separated by the unreleased SiO_2 surrounding the latter, being the drive electrode a low impedance node that acts as a Faraday cage for the wire signal. Finally, there is a group of devices that make the current carrying path and the sense or driving electrodes to share the same structure [44, 64].

The MEMS designed meet various of the aforementioned categories: two of them take advantage of the various metal layers of the CMOS process, and their separation with SiO_2 to obtain isolated (or semi-isolated) current driving structures and voltage driving and sensing. On the other hand, one device uses the current as the only driving signal.

3.2.2 Readout strategy

Due to its simplicity, the devices presented in this chapter, as well as the one depicted in chapter 2, make use of capacitive readout. Various reasons justify this decision. First, being manufactured using CMOS processes, the devices are inherently capacitive. Second, simple bridge adjustment can be done with an on-chip programmable capacitance. And third, no further post-processing is required to manufacture alternative piezoresistive devices. Finally, and most importantly, capacitive readouts are far less noisy and power hungry that resistive ones.

3.2.3 Magnetic field sensitivity

In order to make justified decisions of the devices structure, the AM and FM sensitivities in eq. (1.9) and (1.13) are repeated for convenience in (3.1) and (3.2) respectively.

$$S_{AM}(B) = \frac{V\omega_r\epsilon_r\epsilon_0 ALQ}{g^2 k} I_{rms} \qquad [A/T] \tag{3.1}$$

$$S_{FM}(B) \approx \frac{A_I L}{4\pi\sqrt{mk}} \qquad [Hz/T] \tag{3.2}$$

where V is the dc voltage, ω_r is the resonance frequency, ϵ_r is the air relative permittivity, ϵ_0 is the absolute permittivity, A is the equivalent capacitive area, L is the device effective length, Q is the quality factor, g the gap, k the spring constant, I_{rms} the rms current, $A_I = I_{rms}/x$ is the current gain (where x is the plate displacement), and m the rotor mass.

In both expressions it is possible to see that there are limited ways to increase the sensitivity during the design stage. First, increasing the injected current, which is not always feasible (or wanted) in low power systems. Second, increasing device length to increase the effect of Lorentz force. Doing so may result in two different outcomes: large devices, or complex devices where the same current is recirculated numerous times. However, the longer the path that the current has to travel, the higher the resistance and the power consumption. And third, reducing the spring stiffness k, this is, making the MEMS springs soft. Doing so, by Hooke's law the spring restoring force is weaker, making it easier for the Lorentz force to generate a plate displacement and a capacitance variation.

In AM readouts, increasing the dc voltage is usually used in the literature [44, 79, 85], but in integrated solutions, this means the use of integrated area (switched capacitors) or volume (boost converters requiring inductors) hungry dc-dc converters, as CMOS newer nodes tend to lower biasing voltage. Moreover, the device gap g is a parameter that depends on technology Inter Metal Dielectric (IMD) and the rotor displacement due to metal residual stress. Finally, the greater the quality factor the better, both in AM and FM readouts. In the latter, even though sensitivity does not depend on it, it makes it easier for the electronics to discriminate between signal and noise. Which lowers PLL requirements.

Taking into account the analysis performed in previous paragraphs, some key decisions had to be made during the design of the devices, not always entirely related to the devices performance themselves.

- The stiffness of most of the devices were designed to be very low, resulting in very low resonance frequencies. This is not the best strategy for the readout circuit, as low frequency flicker noise may reduce the SNR. However, this provides a low spring force, which may be easily overcome electrostatically, allowing the measurement of the device resonance at ambient pressure. This decision was taken to allow resonance measurements of full wafer samples without the need of vacuum, as measurements were performed using probes.
- Device size was limited to a maximum of 200 μm per side including MEMS frame. This is translated into MEMS structures of approximately 100 μm per side. Larger devices would provide better sensitivities, but electronics area would be limited, as well as space for different MEMS variants. Moreover, all devices designed are two axis symmetrical square devices, meaning that increasing side by a factor of $2\times$ increases area by a factor of $4\times$.
- Voltage biasing of MEMS devices should be limited between 1 V and 2 V in order to ease electronic circuit designed in the utilized nodes: both SMIC and TSMC nodes are limited to 3.3 V. MEMS characterization, though, may be done with higher voltages in order to ease measurements using probes.

3.2.4 Manufacturing processes characteristics

In order to be able to make an informed design of the MEMS devices, it is of utmost important to know the details of the processes used to manufacture them. This information will be essential during the modelling of the devices.

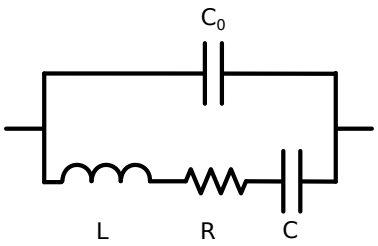


Figure 3.3.1: Second order RLC MEMS model used to fit the data.

3.2.4.1 SMIC 180 nm

The 180 nm SMIC process offers a BEOL with 6 metal layers. Metals from M1 up to M5 are 550 nm thick, while M6 is 900 nm thick. All metal layers are made up of alumnium. Inter-Metal-Dielectric (IMD) is 850 nm thick, except between M5 and M6 where distance is 1 μm. Vias are made up with Tungsten.

SMIC DRC (Design Rule Checking) rules are more demanding than for TSMC process, as long vias are not allowed to cross. Moreover, several rules must be followed related to residual metal stress, otherwise, it may result in big continuous metal pieces breaking during the manufacturing process, as informed by direct interaction with SMIC staff. This metals curvature due to residual stress, though, may be compensated by stacking metal layers (the more stacked layers the flatter the structure) with vias in between.

3.2.4.2 TSMC 180 nm

TSMC 180 nm process is very similar to the SMIC one. There are, of course, some differences between them. First, the availability of a much thicker top metal layer of 2.34 μm. Second, metals from M1 to M5 have a 530 nm thickness with an IMD in between of 1.38 μm. Metal M5 to top metal IMD distance is 1.72 μm. In this case, TSMC allowed long vias in MEMS to be crossed to create via meshes. Finally, residual stress demands for this process are much more relaxed.

3.3 MEMS parameters modelling

MEMS measurements using the impedance analyser usually consist in measuring the resulting conductance G and susceptance B. Doing so, it is possible to extract the MEMS parameters of the typical second order series RLC resonator model, which is shown in Fig. 3.3.1. The RLC model admittance has been derived in (3.3)

$$Y = \underbrace{\frac{R}{R^2 + \left(\omega L - \frac{1}{\omega C}\right)^2}}_{\text{Conductance, G}} + j \underbrace{\left(\omega C_0 + \frac{\omega L - \frac{1}{\omega C}}{R^2 + \left(\omega L - \frac{1}{\omega C}\right)^2}\right)}_{\text{Susceptance, B}} \tag{3.3}$$

Where R, L, and C are the MEMS equivalent resonator components, C_0 is the feedfordward MEMS capacitance, and $\omega = 2\pi f$ is the angular frequency. The real part of the admittance is the conductance G, whereas the imaginary part is the susceptance B. A Python script has been written that fits the measurement data to the G model in (3.3) and extracts the resonator parameters RLC. Then, the needed MEMS parameters, can be extracted: resonance frequency f_r, and quality factor

Q:

$$f_r = \frac{1}{2\pi}\sqrt{\frac{1}{LC}} \tag{3.4}$$

$$Q = \frac{1}{R}\sqrt{\frac{L}{C}} \tag{3.5}$$

3.4 Proposed MEMS

Various MEMS magnetometers have been designed, some of them having improved versions in subsequent runs and manufacturing processes and etching strategies that helped learn the needs of each one and the characteristics of each process step. Below, the different MEMS are detailed and analysed.

3.4.1 The Quadspring device

The first device to be described is the Quadspring. Its name comes from the fact that it looks like it has four springs (even though it has eight in four spring pairs). This device has been included in three different runs. The initial version was included in a full wafer SMIC run, while the second and improved version of this device was included both in a second full wafer SMIC run and a Multi Project Wafer (MPW) Europractice TSMC run (named Recollection) with few differences between them. The following explanation is for the first version of the first full wafer run. Improvement will be explained in the measurements section as observed problems and potential solutions are detailed.

The device is a parallel plate MEMS device with a square shaped suspended structure supported by four springs. Its diagram and dimensions are shown in Fig. 3.4.1. Each spring pair consists of two identical springs in parallel that are not electrically connected. The spring is made of M2, and it is connected to the MEMS frame and plate to the device driving electrode. The upper spring is made of M4, where the current flows. On one side, the M4 spring is connected to a column inside the frame, which provides an endured mechanical structure and connection to M1, where the current enters the device. A cross-section diagram of the M4 spring frame anchor is depicted in Fig. 3.4.2. On the other spring side, the M4 path goes into the central plate shape, consisting in a cross-like structure that surrounds M4 path isolated from the rest of the plate. Here, M4 path flows in parallel to a M5 path connected with vias that reduces the path resistance. Using one void metal (M3) between both springs reduces the probability of springs stiction during structure release. The cross-shape current path allows the current to flow horizontally and vertically, which allows a 2-axis magnetic field measurement as both resulting Lorentz forces generate an out-of-plane displacement of the MEMS rotor.

The 100 $\mu m \times 100$ μm suspended plate is made with a metal stack from M2 to M6. In each quadrant, a hole matrix allows the acid to descend and release the structure. Holes dimensions are 3.56 $\mu m \times 3.56$ μm and have a 5 μm pitch. Each hole is surrounded by long vias with a square shape that hold the different plate metal layers together. However, the plate periphery does not have vias around it, so plate mass reduction is expected due to the release acid flow on the periphery.

The stator consists in a 80 $\mu m \times 80$ μm M1 plate. It has been designed smaller than the rotor in order to reduce the parasitic capacitance between the current carrying M4 path and the sense electrode. In order to meet process DRC, M1 stator plate has a matrix of 2 $\mu m \times 2$ μm holes with 10 μm pitch.

Finally, the MEMS is surrounded by a metal frame that stops lateral etching. It consists of

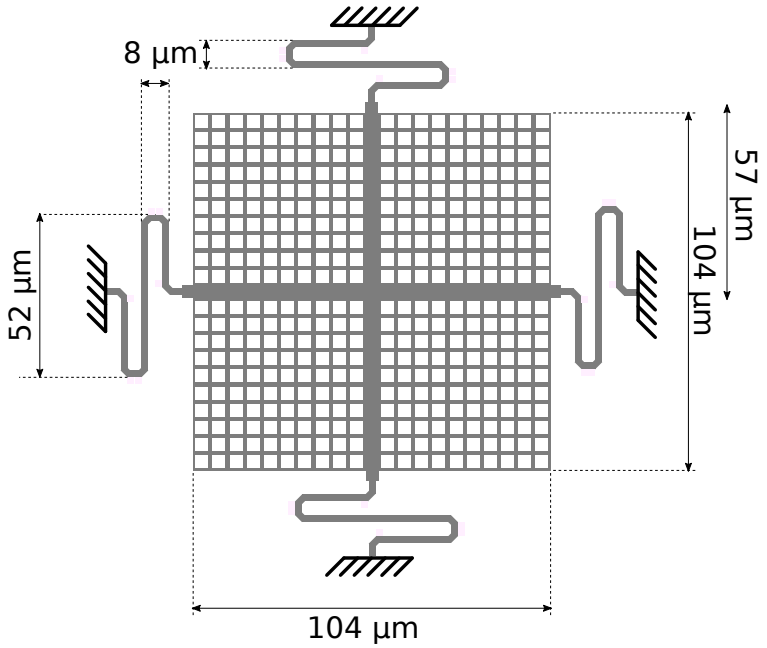


Figure 3.4.1: Quadspring simplified top metal diagram.

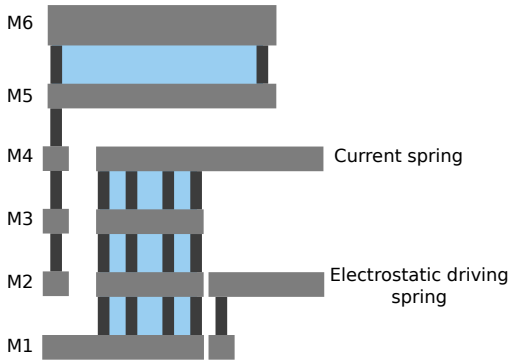


Figure 3.4.2: Quadspring device spring anchoring column cross section diagram.

a stack of M1-M6 metal layers and long vias strategically open to connect the MEMS with the outside without allowing the acid to leave.

With these characteristics, this device is expected to have very soft springs and thus a very low resonance frequency. Even though current does not recirculate, resulting in a low effective device length in terms of the Lorentz force, the low spring constant would compensate for this fact and keep sensitivity high. On the other hand, such soft device may be prone to stiction during oxide release: H_2O, which is a subproduct of this process, has a very high surface tension. If this water appears in its liquid state, stiction of M2 and M4 springs one to each other, and MEMS rotor to stator is probable. This happened with the Quadspring device included in the Recollection run, as after wet etching it was found collapsed. For this reason, dry etching using vapour hydrofluoric acid (vHF) is preferred for the release of this device.

3.4.2 The Medusa device

This device's name comes from the fact that the MEMS, with its very long springs, resembles the Medusa gorgon of Greek mythology. Similarly to the previous device, it has been included in two

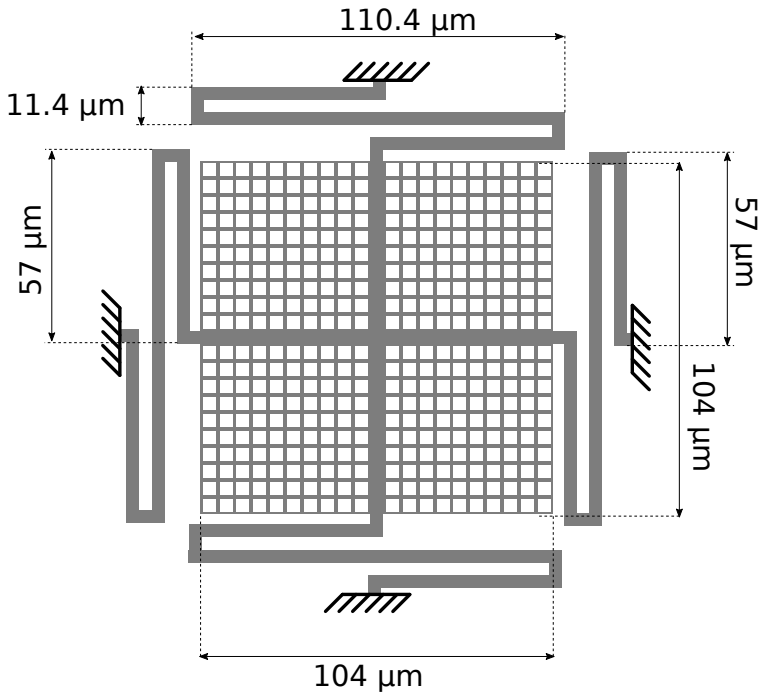


Figure 3.4.3: Medusa device M5 diagram with design dimensions.

SMIC full wafer runs and one MPW TSMC run.

As previously mentioned, one of the issues of Lorentz force MEMS magnetometers is the offset generated by the current path coupling with the sense electrode. In order to avoid such issue, the device used in chapter 2, and designed by PhD student Mr. Juan Valle, consists of various clamped-clamped cantilevers where the current path is totally shielded by the driving electrode. Doing so, the low-impedance drive electrode isolates the wire and the sense electrodes and avoids such issue. The Medusa device has been designed following the same shielded objective, but with a parallel plate approach.

The device is also a parallel plate MEMS device with a square suspended structure supported by four springs. A simplified diagram with the shapes dimensions is shown in Fig. 3.4.3. The springs length is increased and they are made up of a stack of M3-M5 and 3.6 μm width. The springs consist in an upper M5 and lower M3 metal pieces electrically connected by a stack of vias V34, V45 and M4 that surround the current carrying path inside made of M4, with a 2.1 μm width. For a better understanding, Fig. 3.4.4 shows the cross section of the spring. The inside of the spring is not reached by the acid, and as a consequence M4 current carrying path is surrounded by SiO_2, making the spring stiffer than in Quadspring MEMS device. The rest of the 104 $\mu m \times 104$ μm plate has the same structure that Quadspring.

The stator is a M2 plate connected with vias to M1, where the sense electrode goes to the outside crossing the frame.

As previously mentioned, this device is expected to have stiffer springs, due to their bulkier cross section as well as the presence of SiO_2 inside. For this reason, and to allow an easy measurement without the need of vacuum, the springs have been designed much longer. Moreover, this device is still prone to plate stiction during the release, as it was found collapsed in wet etched Recollection run, so vHF is preferred.

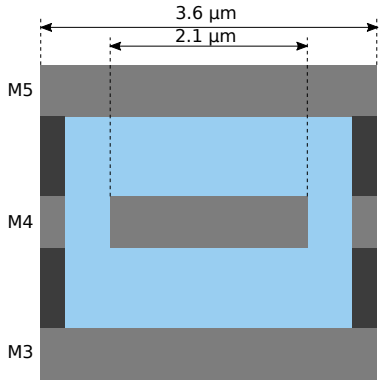


Figure 3.4.4: Medusa device spring cross section.

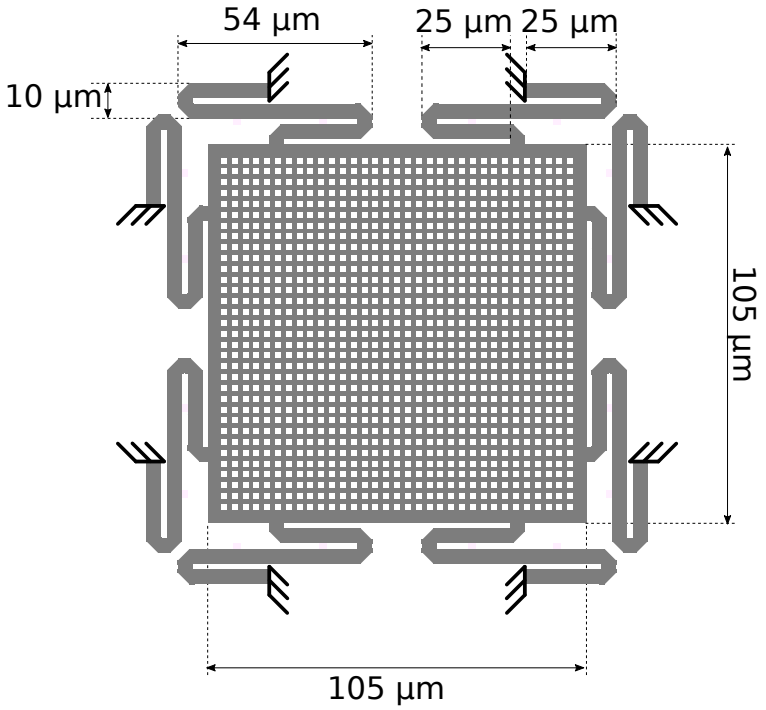


Figure 3.4.5: Octo spring device simplified diagram and dimensions.

3.4.3 The Octospring device

Finally, the Octospring device is the most conservative device design. Its name comes from the fact that its plate is suspended by eight springs. It consists in a 105 $\mu m \times 105$ μm M6 only suspended plate. The plate is full of 1.5 $\mu m \times 1.5$ μm holes with a 3 μm pitch, except the periphery, where the boundary rows and columns of holes have not been placed in order to provide the spring-plate attachment greater strength and to minimize the probability of metal cracking due to residual stress. The stator is at M5, which is connected by a set of long vias down to M1. A simplified diagram of the device top view is shown in Fig. 3.4.5.

The device has two springs per side, made of M6 and attached to the die substrate with three capacitive anchors. One anchor cross section diagram is shown in Fig. 3.4.6. The springs are 4 μm wide and they are much smaller than the ones in Medusa device and eve the Quadspring device. Moreover, using the top metal makes the spring thickness greater than springs in lower metals. Finally, more springs increase the total k, resulting in an equivalent hard spring with higher

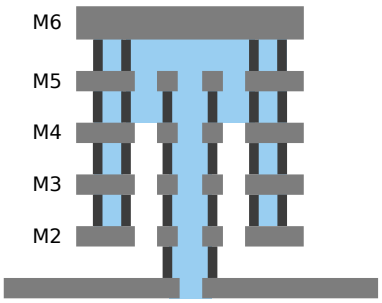


Figure 3.4.6: Diagram of the cross section of one of the three anchors that supports each spring.

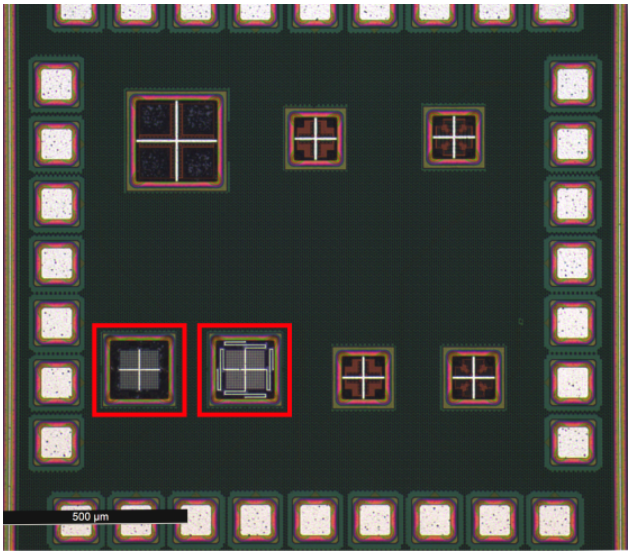


Figure 3.4.7: Die included in first full wafer run with some MEMS designs. First version of the Quadspring and Medusa designs are in die lower left corner.

resonance frequency, but lower sensitivity.

This device has been included in the second SMIC run, and the MPW TSMC run. In the first one, top metal is only 900 nm thick, resulting in much softer springs, but also smaller mass. On the second run, the top metal is 2 μm, resulting in much stiffer springs. In any case, this device is expected to be wet etching resistant due to the higher force needed to pull-in the plate.

3.4.4 Tape-outs with MEMS

3.4.4.1 First full wafer run

The first die with MEMS magnetometers was included in a SMIC 180 nm BEOL only full wafer. The wafer was divided into 56 reticles. An optical microscope photograph of the die is shown in Fig. 3.4.7. The first version of the Quadspring, and the Medusa designs are on the lower left part of the die.

3.4.4.2 Recollection

The Recollection die was taped out to TSMC 180 nm process using the Europractice MPW services. This die included three devices: 1) the first version of the Octospring device, 2) the second version

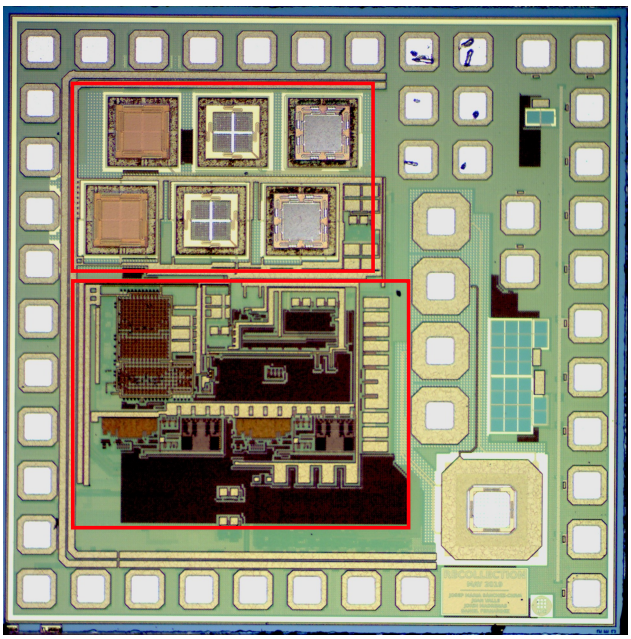


Figure 3.4.8: Recollection die manufactured with TSMC 180 nm. On the top, two rows of Medusa, Quadspring, and Octospring are depicted. The upper row is intended for probes measurement while lower is connected to the electronics below.

of the Quadspring device, with wider (4 μm compared with the 2 μm in the previous version) and, as a consequence, stiffer springs, and 3) the second version of the Medusa device. Of the latter two, two main changes were made with the previous version. First, the device was made wet etching resistant by increasing the number of long vias in the device, as well as crossing them. This results in smaller plate holes, higher mass (due to higher density of Ti/TiN vias), and a lower probability of metals detaching due to liquid acid filtering between vias and metals, a phenomenon observed during wet etching trials of previous chapter device. Second, via meshes were included in the plate and the MEMS frame taking advantage of TSMC which allowed long via crossings.

An image of the Recollection chip is shown in Fig. 3.4.8. On the top of the chip there are two rows of MEMS devices. First row MEMS are connected to pads and measured in this chapter. Second row MEMS are connected to the electronics below and analysed in chapter 4.

3.4.4.3 Second full wafer run

The final devices versions were included in a second SMIC full wafer run. The wafer was divided into 56 reticles. An image of the die is shown inf Fig. 3.4.9. The devices included are: 1) the Octospring second version, identical to the previous one but meeting SMIC DRC requirements, 2) third version of Quadspring, with 4 μm wide springs, and 3) the third version of the Medusa MEMS. on the latter, the only difference with the previous design is that long vias surrounding the plate hole do not create a square. Doing so, SiO_2 can penetrate homogeneously the entire plate (in previous versions the oxide was only released in the periphery of the plate), achieving a constant oxide uniformity across the plate. Moreover, via meshes have been removed again in order to meet SMIC DRC rules.

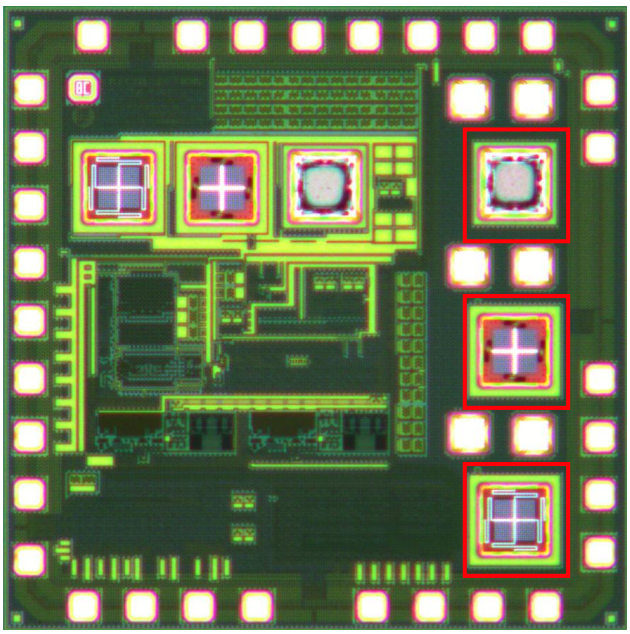


Figure 3.4.9: Die included in the second full wafer run with some MEMS designs. Third version of the Quadspring and Medusa designs, and second version of the Octospring MEMS were included.

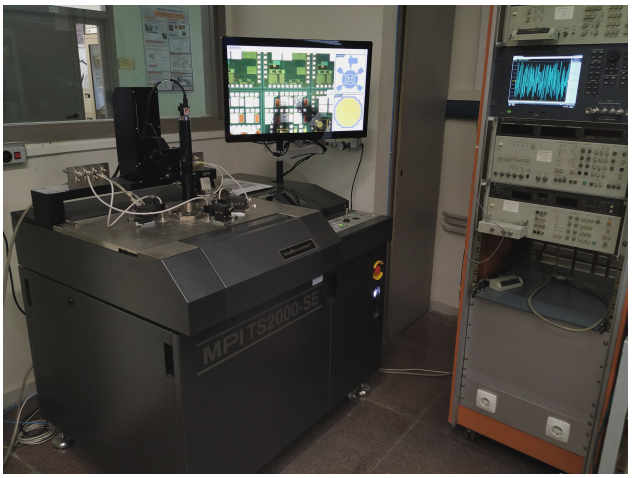
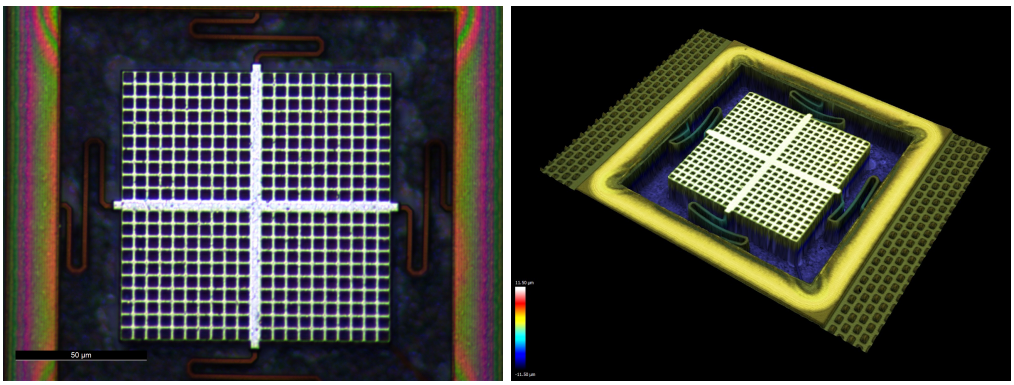


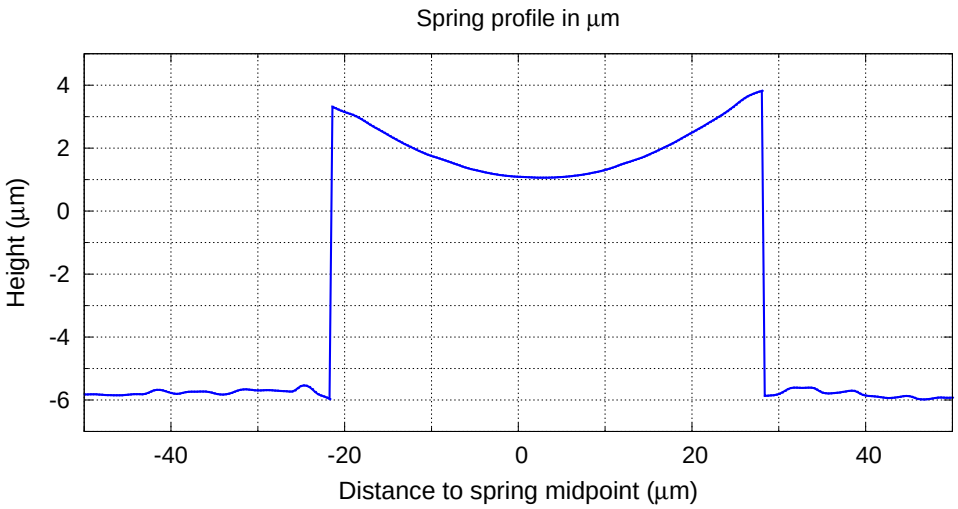
Figure 3.5.1: Image of the semi automatic probe machine available at IMB-CNM facilities during the calibration of probes position.

3.5 Experimental results

The devices described so far have been measured with probes, both manually at Electronic Engineering Department at Universitat Politècnica de Catalunya and using the semi automatic probe system MPI TS2000, shown in Fig. 3.5.1, available at Institut de Microelectrònica de Barcelona (IMB-CNM). All device measurements have been done with the Keysight 4990A impedance analyser.



(a) (b)



(c)

Figure 3.5.2: Quadspring first full wafer run version optical image (a), confocal image (b), and height profile along device spring (c).

3.5.1 The Quadspring device

3.5.1.1 First full wafer run version

An optical microphotograph of the Quadspring device is shown in Fig. 3.5.2 (a). Giving the picture an analytic look it is possible to see that spring meanders look a bit blurrier than the rest of the spring, a sign that that part may be at a different height. This observation is confirmed by the picture made with the confocal microscope Leica DCM 3D, shown in fig 3.5.2 (b), where it can be seen that due to metal residual stress M4 spring has an important curvature. The measured profile along the M4 spring is depicted in Fig. 3.5.2 (c), where it is possible to see that the spring edge is almost 3 μm above the spring lowest point around the middle of it.

Having such curvature is always cumbersome in MEMS design. In this case, however, if M2 spring underneath is equally curved, then both springs may not touch each other. Unfortunately, this is not the case, as it can be seen in the SEM image in Fig. 3.5.3. Even in a zenithal picture of the device it can be seen that M2 and M4 springs are touching. This means that current and electrostatic driving electrodes are shorted, making the device to not work as expected.

Nonetheless, capacitance measurements with an impedance analyser at 0 V dc voltage were performed. The resulting histogram after removing four outliers (two collapsed samples with ca-

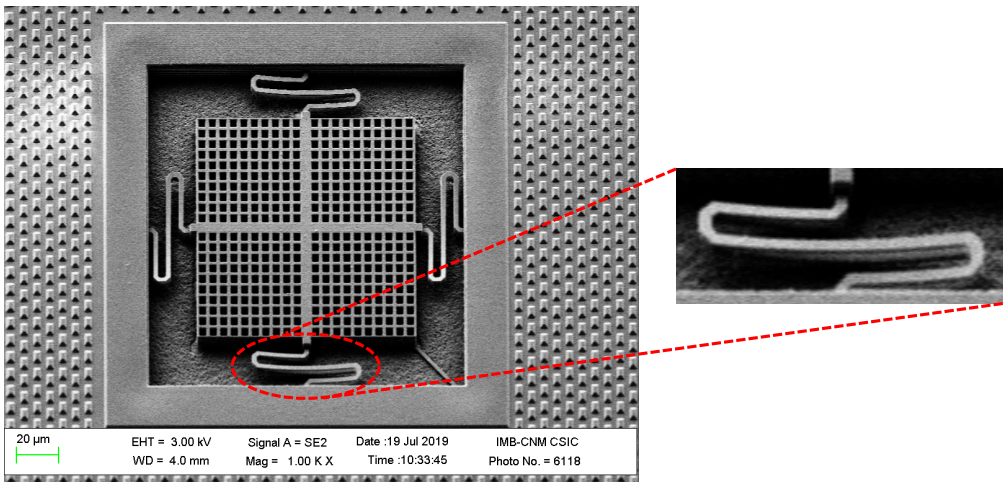


Figure 3.5.3: SEM photograph of the Quadspring device. A detail of the stitched M2 and M4 springs is depicted.

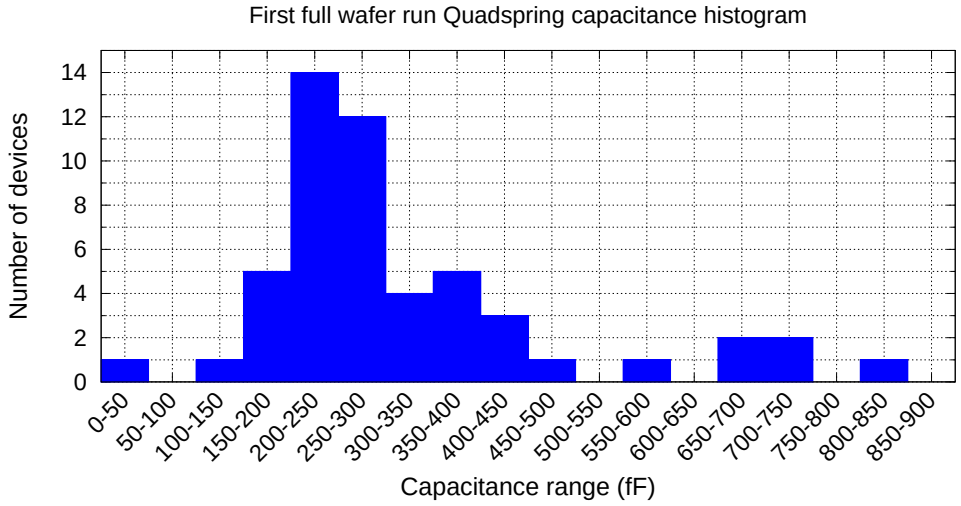
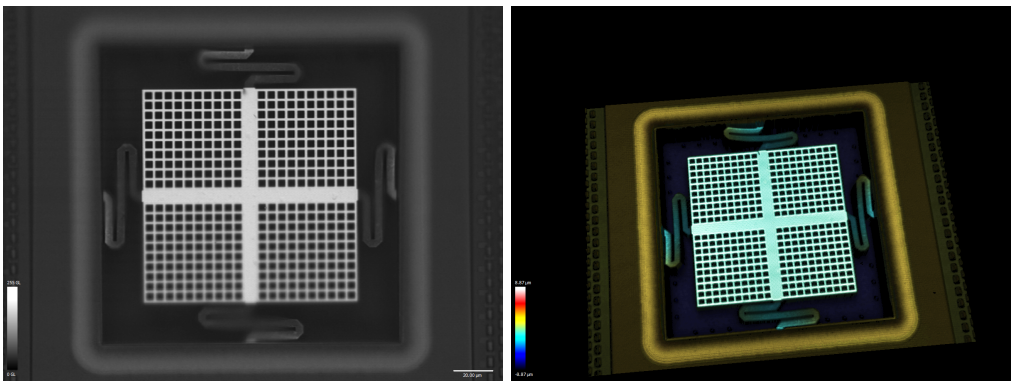


Figure 3.5.4: First full wafer run Quadspring capacitance histogram of 52 devices.

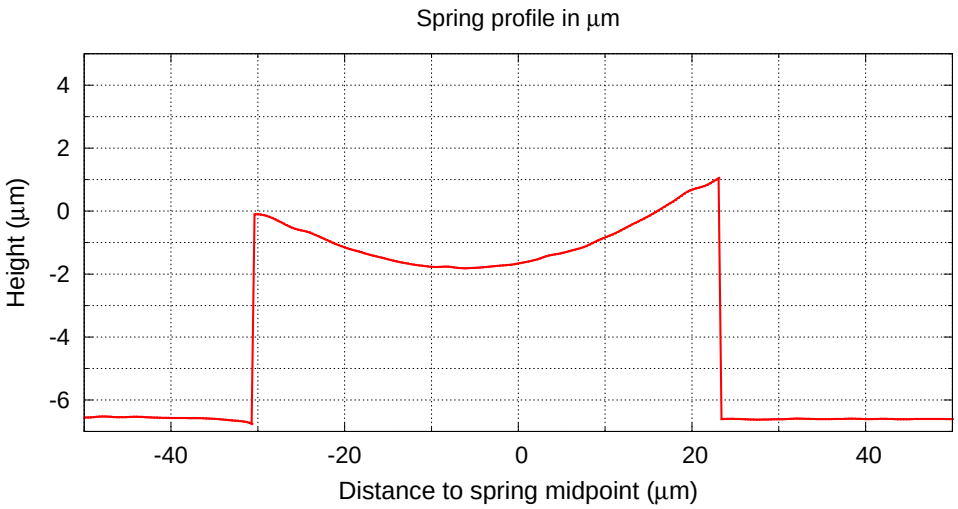
pacitances ranging some pF, and two with negative capacitances, probably destroyed devices) is shown in Fig. 3.5.4.

As it can be seen, the capacitance variability is huge, with an average capacitance of 323 fF and a standard deviation of 163 fF. This very large variability is clearly a consequence of spring stiction, which causes an important gap variability. Further evidence of this stiction problem are the resonance measurements performed on the device: few devices resonance was found.

As expected, SMIC process provides a BEOL metallization with an important amount of residual stress. And MEMS structures must cope with such issue in order to be able to obtain working devices. In the specific case of this device, the main consequence of metal residual stress is the important curvature of the MEMS spring, which causes their curvature. Possible solutions to reduce the curvature may be designing shorter springs, and designing springs consisting in a stack of metals. The second solution is not feasible in this type of devices as distance between springs would shrink and be more prone to stiction. The first solution would keep the radius of curvature unchanged, but reduce the relative height difference. A good point of this second solution is that making shorter springs make them stiffer, being equally affected by residual stress curvature, but more resistant to spring-to-spring stiction. A similar solution has been carried out in the second



(a) (b)



(c)

Figure 3.5.5: Quadspring second full wafer run version SEM image (a), confocal image (b), and curvature along one of its springs (c).

version of this device by making the springs wider: in a first-order approximation, the spring k constant is proportional to spring width [129]. For this reason, in the second Quadspring version the springs width have been increased from 2 μm to 4 μm.

3.5.1.2 Second full wafer run version

A SEM image as well as a confocal image of the second version of the Quadspring MEMS are shown in Fig. 3.5.5 (a) and (b). As expected, the spring curvature of this version is similar, as shown in (c) of the same figure.

MEMS sense to drive capacitance measurement has been used as a starting point to check whether the spring modification has proven successful to reduce spring stiction. Such measurement histogram in shown in Fig. 3.5.6, where six measurements have been removed as they show broken devices. In this version of the device, average capacitance value is 1196 fF and the standard deviation is 57 fF. From this data various observations can be made. First, the capacitance value is approximately 3 times larger than in the previous version. This is due to the fact that M1, electrically connected to the driving electrode, has been used as etching stopper, which increases the sense to drive capacitance. Moreover, observations made with the confocal microscope show that the plate is (at least in the photographed device) 0.5 μm below the spring height side anchored

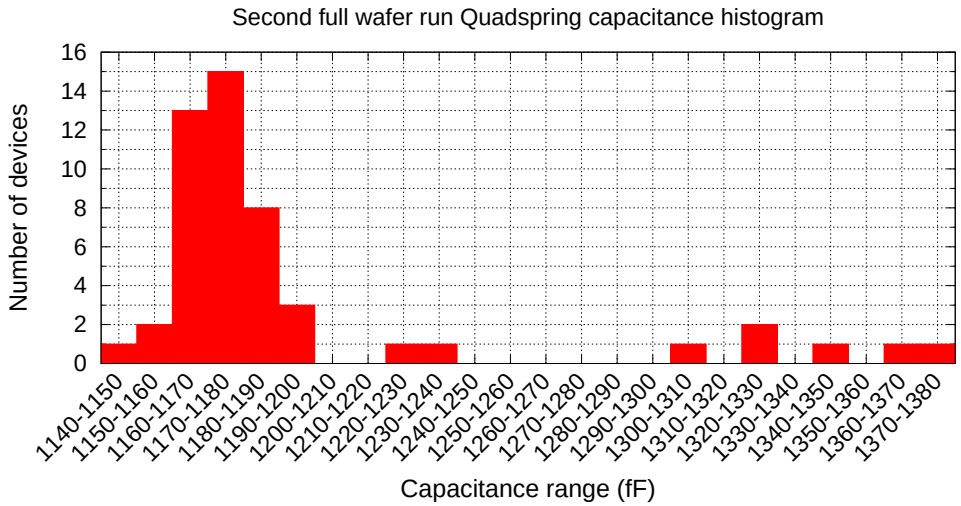
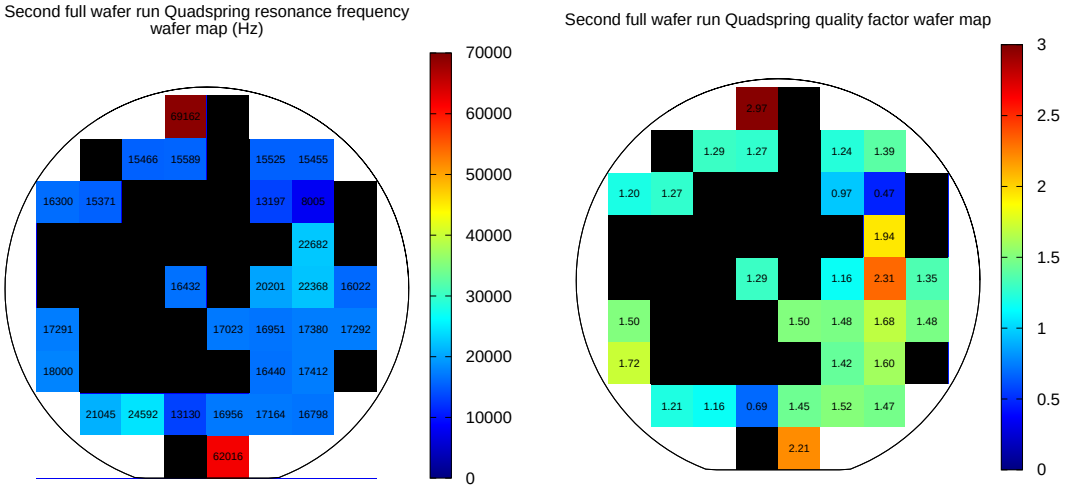


Figure 3.5.6: Second full wafer run version Quadspring capacitance histogram of 50 devices.

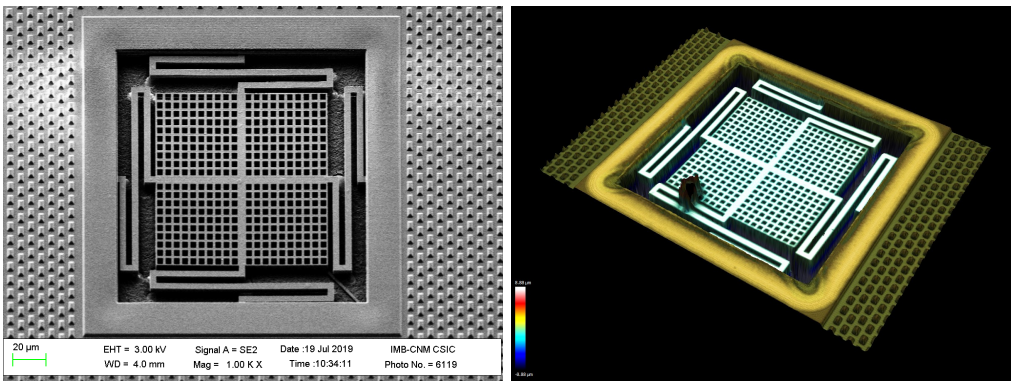


(a) (b)

Figure 3.5.7: Second full wafer run Quadspring resonance frequency (a) and quality factor (b) distribution on the measured wafer. Each square represents a reticle, while black reticles are non-working devices.

at the frame, a phenomenon not observed in the previous device. This is thought to be caused by batch-to-batch residual stress variations of big structures, something that has been observed in other devices in this run. A good example of this phenomenon will be observed again in following sections. Second, the proposed spring improvement seems to be useful to reduce device capacitance variations, both in absolute and relative terms.

Unfortunately, resonance measurements show quite different results, as only 52% of the devices on the wafer show a resonance in the measured frequency range between 1 *kHz* and 100 *kHz*. The resonance of the rest of devices has been found to be at higher frequencies or no resonance at all. Fig. 3.5.7 depicts the resonance frequency and quality factor distribution on the measured wafer. Average resonance frequency is 20.4 *kHz* with a standard deviation of 12.9 *kHz*, while quality factor average is 1.48 with a deviation of 0.48. It is possible to see that most resonating devices are found in the wafer periphery, were curvature of single metal structures tend to be larger as observed in [97] due to differences in residual stresses.



(a) (b)

Figure 3.5.8: Medusa first full wafer run version SEM image (a), and confocal image (b).

Finally, some conclusions may be drawn of Quadspring device. First, increasing spring width has been partially successful in terms of increasing the device yield as a consequence of having stiffer springs. Second, devices whose resonance has not been found, probably have parallel springs collapsed, a fact that does not seem substantially affect capacitance values. Third, devices on the periphery of the wafer, with more curved springs regarding [97], better withstand spring stiction. Probably due to the strongest residual stress that compensates forces that cause stiction. Fourth, parallel springs are not a good structure choice. Some alternatives may be better solutions to this issue, such as a springs stack made of M2-M3 in parallel with a spring stack of M4-M5, that would show much lower curvature, but also a lower spring-to-spring gap, that may be, again, prone to stiction.

3.5.2 The Medusa device

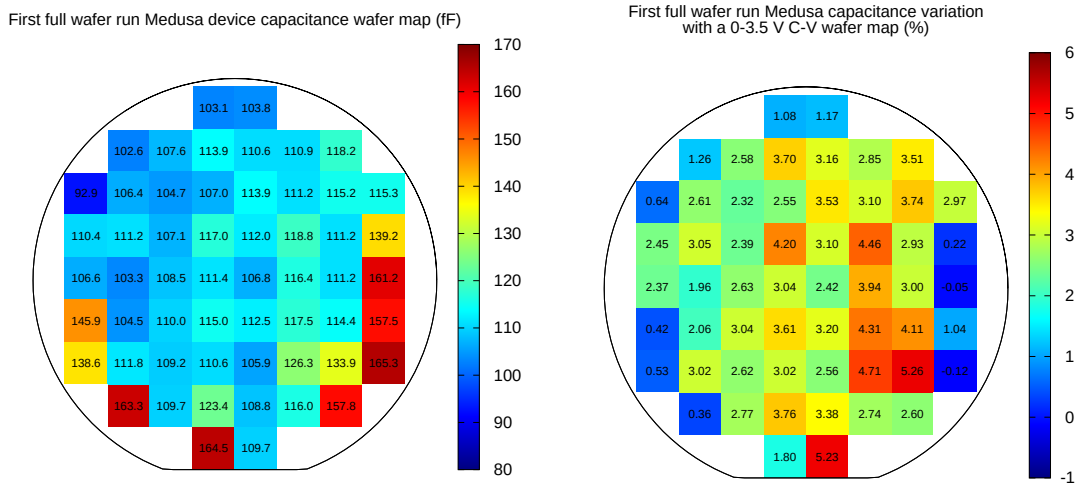
3.5.2.1 First full wafer run version

SEM and confocal images of the first full wafer run version of the Medusa device are shown in fig 3.5.8. As expected, this device presents a much lower spring curvature, as shown in 3.5.8 (b). This fact is due to the springs design: consisting in a metal and via stack from M3 up to M5, spring maximum height difference is around 290 nm along all its length, 90% lower spring maximum to minimum curvature height compared with Quadspring springs. The unreleased oxide inside the springs also helps to compensate the metal residual stress that causes the curvature.

The spring curvature measurement, though, has been performed on a single device so, to test the performance of all the devices across the wafer electrical measurements have been done. First, capacitance variations has been measured during a dc voltage sweep (C-V measurement). From this measurement, device capacitance with 0 V dc voltage and capacitance variation are extracted. Both measurements are shown in Fig. 3.5.9. These preliminary results show that capacitance across the full wafer is very uniform with an average of 118 fF and a standard deviation of 18 fF. Moreover, C-V results show a promising capacitance variation 2.33% (2.66 fF) on average with a standard deviation of 1.1% (1.27 fF), being lower in the periphery of the wafer. Fig. 3.5.10 shows the histogram of both measurements confirming the low standard deviation of the measurements.

It is possible to see that there exists some correlation between the devices with higher capacitance in the wafer periphery in Fig. 3.5.9 (a) and devices with lower capacitance variation in Fig. 3.5.9 (b), showing that these devices may be either partially collapsed or not fully released.

To further check the feasibility of the Medusa device, resonance measurement is carried out in



(a) (b)

Figure 3.5.9: Medusa first full wafer run version device capacitance wafer map (a), and maximum capacitance variation for a voltage sweep between 0 V and 3.5 V (b).

all wafer devices. The MEMS resonance and quality factor distribution across the wafer are shown in Fig. 3.5.11.

In the figures, it is possible to see that wafer periphery devices, that showed a larger capacitance and lower C-V variation, are effectively not working as their resonance was not found. This fact may be explained by various reasons: 1) metals of devices on the periphery suffer a larger residual stress that may not be completely compensated by the springs stack of metals and vias filled with SiO_2. This may cause the device to be partially collapsed. 2) Etching non-uniformity across all wafer may cause the device to be partially unetched and anchored somewhere with SiO_2. Maybe a slightly longer etch time would be needed. 3) A more simple explanation may be an incorrect wafer manipulation. These devices were the last ones to be measured, meaning that several people have previously handled the wafer in different places and setups, so it is not unlikely that these devices had been accidentally touched. This hypothesis is further supported by the fact that broken devices are placed close to where wafers are typically hold. In any case to verify any of the hypothesis new wafers with different etching times may be required.

Nevertheless, working devices show a good uniformity across the wafer. Fig. 3.5.12 shows the histogram of resonance frequency and quality factor measured with 3 V of biasing and 100 mV of ac driving: for resonance frequency $f_{r\ avg} = 56.783\ kHz$, $\sigma_{f_r} = 5.076\ kHz$, and quality factor $Q_{avg} = 7.29$, $\sigma_Q = 1.59$. Yield, considered as the ratio of resonating vs. non-resonating devices is 85.7%, a pretty good result being a first attempt. Unfortunately, this figure would decrease if more stringent specifications are used.

Finally, three more measurements have been performed to this device that have not on the rest: current carrying path resistance, capacitance between sense and current input electrodes, and magnetic field sensitivity. In second full wafer run and Recollection devices the remaining die area was very limited, so only the drive and sense nodes were connected to pads. On the other hand, in first full wafer run, current carrying input and output electrodes where connected to pads. Due to springs shorts in Quadspring device, this measurement is not reliable. In Medusa first full wafer run version, the resistance of the current carrying path is $R_I = 47.5\ \Omega$, lower than the lowest value found in the literature [89]. Such resistance value has some benefits that may be interesting to consider in futures designs: 1) lower power consumption, 2) the possibility of putting various turns in series

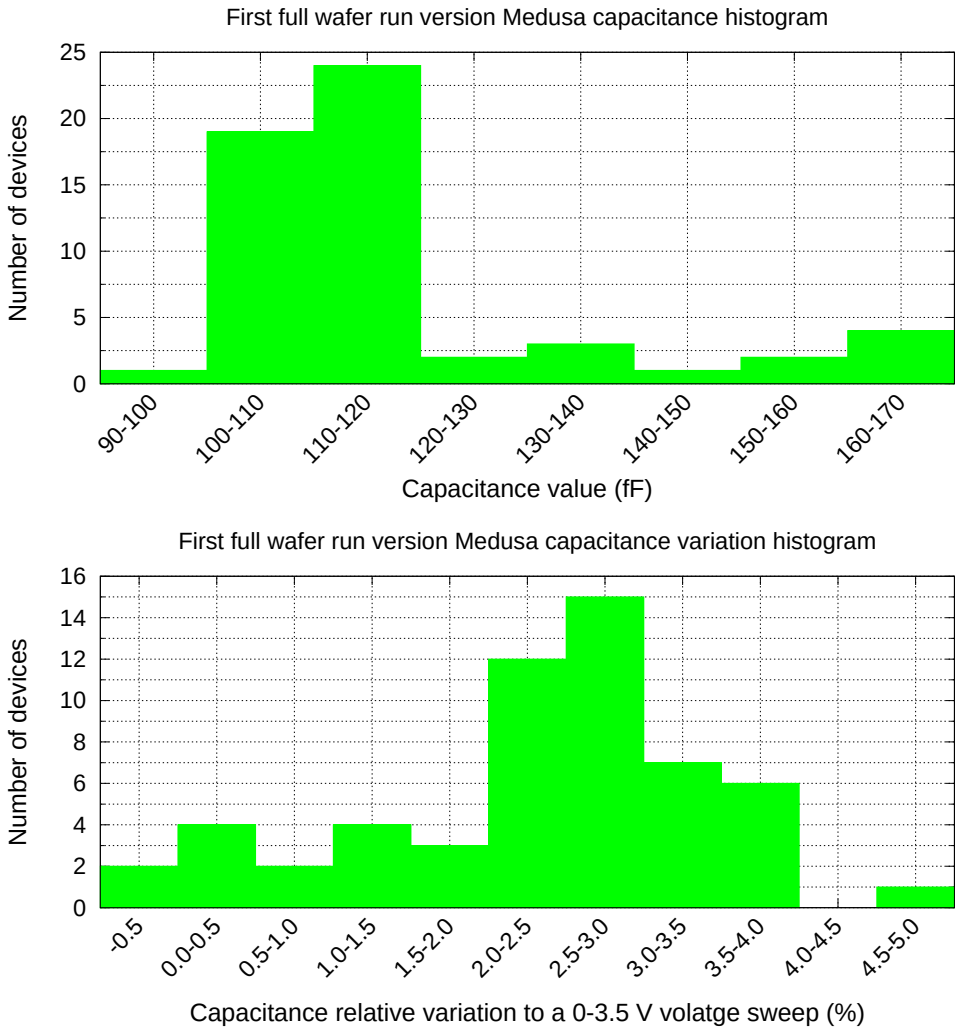
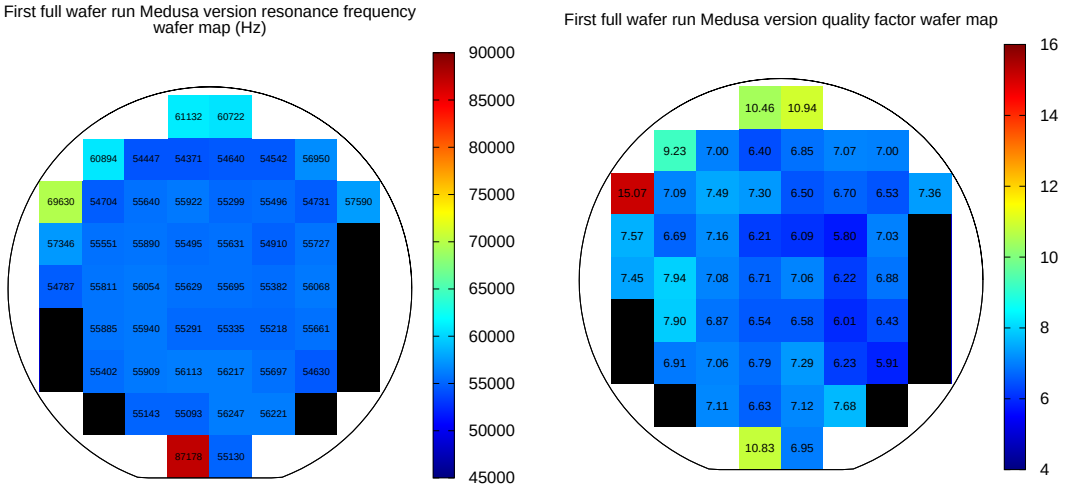


Figure 3.5.10: First full wafer run Medusa device capacitance value histogram on top and capacitance variation histogram below for all wafer devices.

in order to make the current recirculate and increase device sensitivity with a low power increase price. Finally, the current input to sense parasitic capacitance is, on average, $C_{C2S} = 4\ fF$. Such a low capacitance is difficult to distinguish from measured noise and instrument stray capacitance calibration. Hence, the shielding that the drive electrode provides is proven to work as expected and provides a virtually 0 fF capacitance between these nodes.

3.5.2.1.1 Magnetic field sensitivity measurements After performing all wafer level measurements, the wafer was cut and some devices encapsulated and wirebonded to a JLCC44 package. Unfortunately, manual cutting of samples from a wafer is a quite aggressive process that not all devices withstand. Nevertheless, a Medusa device of a reticle at the wafer center (reticle number 28) survived and was measured. The measurement setup schematic used is shown in Fig. 3.5.13. The driving node of the sensor was connected to a 4.65 V dc voltage, while the sense electrode was connected to the input of the LNA of board in chapter 2, at 1.65 V, resulting in a 3 V MEMS biasing. Current driving was done with a signal generator, sweeping frequency around the resonance frequency. Current carrying wire capacitive coupling with the sense electrode due to the PCB and the wiring was compensated with various precision capacitive trimmers in parallel. The setup was put inside a vacuum chamber at 0.3 $mbar$ pressure. The signal generator trigger was used to trigger the oscilloscope, while this latter time scale was configured in order to see the full frequency sweep.



(a) (b)

Figure 3.5.11: First full wafer run version Medusa device resonance frequency (a), and quality factor (b) wafer map.

Doing so, the oscilloscope effectively worked as a spectrum analyser.

The sensor sensitivity has been characterized by performing resonance measurements for various current drivings and the same constant magnetic field, applied with a permanent magnet next to the sensor. This method has been previously used in the literature [68, 77]. Unfortunatelly, it was not possible to know the applied magnetic field. The measured sensor output current as a function of injected current for a constant magnetic field is shown in Fig. 3.5.14. It can be seen how resonance peak increases as a function of current increase until a current value where the sensor saturates, probably due to the fact that the sensor enters the nonlinear region.

3.5.2.2 Second full wafer run version

Given the good results of this device, no changes have been performed of the MEMS suspended structure. On the other hand, some changes where done on the MEMS frame in order to improve the springs anchors and increase its resilience to etching. Moreover, a M1 etching stopper has been placed below all MEMS area. Doing so, vHF is unable to reach the silicon, which may cause some nasty subproducts in a full CMOS run with manufactured Front-End-Of-Line (FEOL).

As few changes separate this device version with the previous one, this run has been used to analyse how batch-to-batch manufacturing variability affects the Medusa device.

A C-V measurement from 0 V to 3 V show that the M1 stopper increases nominal capacitance importantly compared with the first full wafer run version of this same device: average capacitance is 1244.3 fF with a capacitance standard deviation of 24.2 fF. This latter value is very similar to the standard deviation found in first full wafer run version. Both measurements wafer distribution are shown in Fig. 3.5.15, while histograms are depicted in Fig. 3.5.16. Capacitance variation average is 0.56% with $\sigma_{\Delta C} = 0.36\%$. Obviously, given the larger sense to drive capacitance, this is a much lower variation in % than in the first full wafer run counterpart, but in absolute terms it has increased: 6.98 fF and a deviation of 4.55 fF. The C-V variation increase is explained as followed: similar to Quadspring device, this device also shows a downward curvature of the springs and plate due to the different metal residual stress of second full wafer run compared with first full wafer run. This concave curvature of the MEMS reduces the gap, which in turn increases the electrostatic force

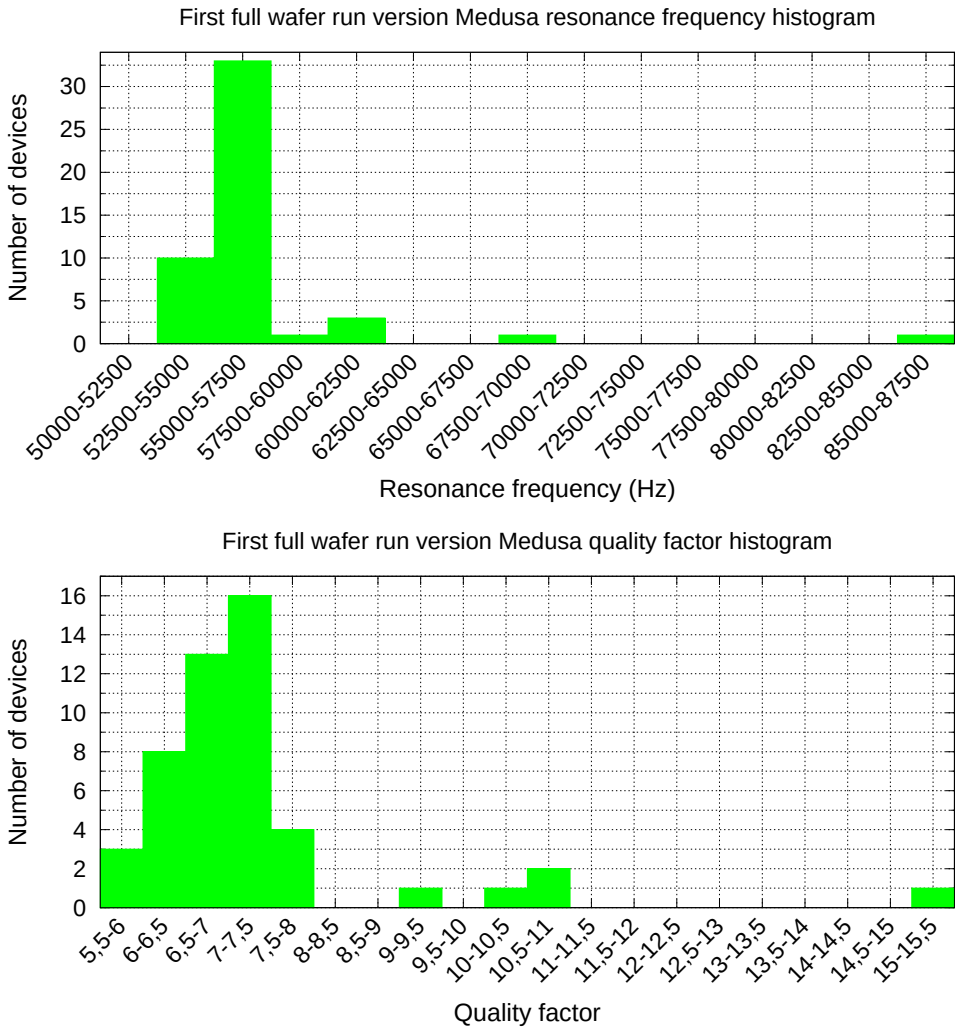


Figure 3.5.12: First full wafer run Medusa resonance frequency and quality factor histograms for 49 devices.

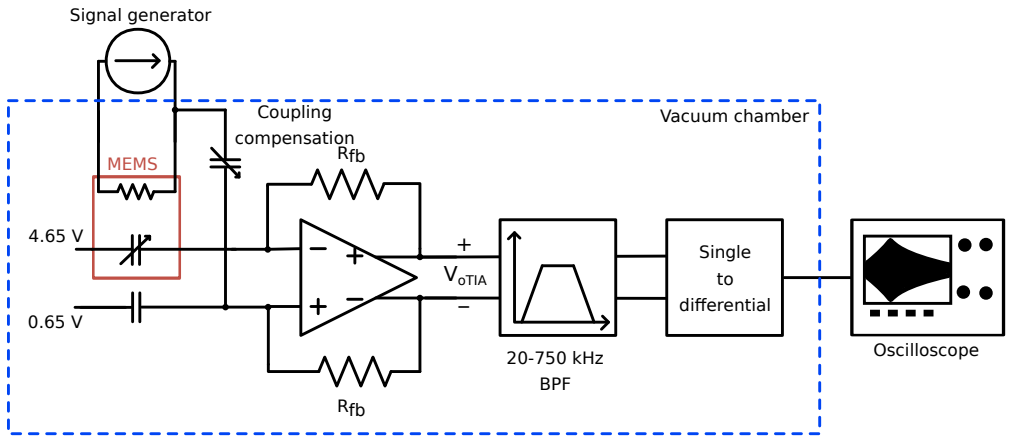


Figure 3.5.13: Magnetic field sensing sensitivity measurements setup schematic.

generated by a voltage drop between MEMS electrodes, further displacing the plate and increasing the capacitance. This batch-to-batch residual stress change can be an important root of variability in high volume manufacturing. However, in this case, the height difference between the spring anchor and the lower plate height is 0.42 μm, lower than in the first full wafer run. Hence, it seems

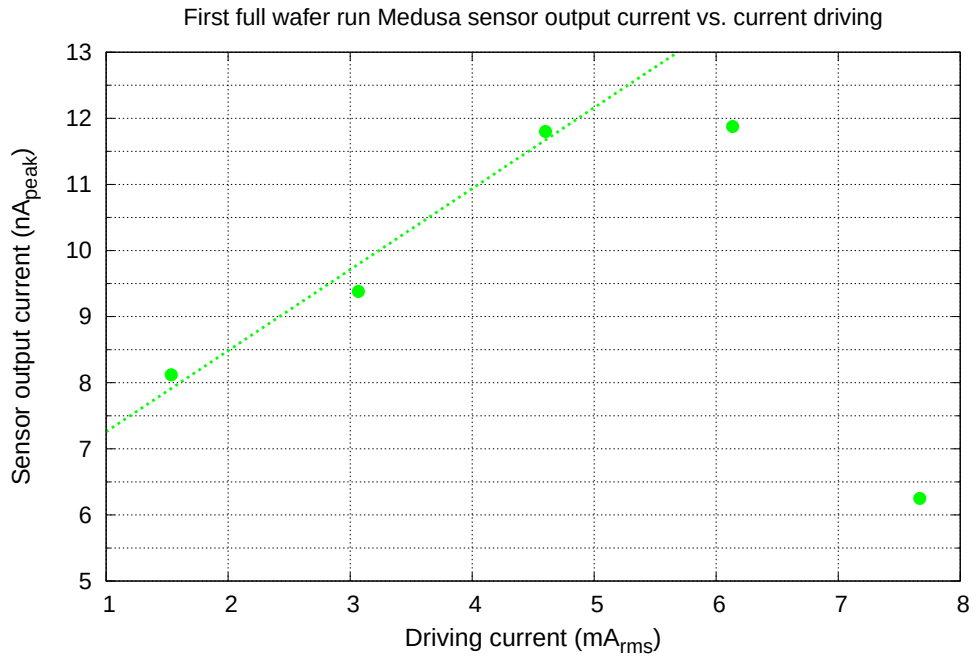
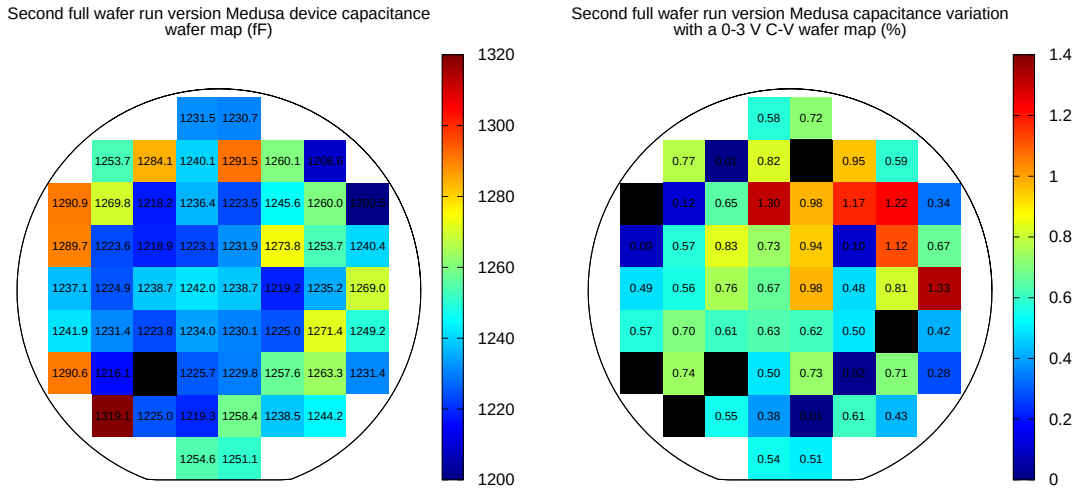


Figure 3.5.14: Sensor output current as a function of sensor current driving with a sensor biasing of 3 V and a permanent magnet placed next to it



(a) (b)

Figure 3.5.15: Second full wafer run version Medusa device capacitance (a) and capacitance variation during a C-V measurement from 0 V to 3 V (b).

that metal stacking along the springs helps reducing the curvature.

Resonance measurements were performed at ambient pressure with 3 V dc biasing and 100 mV ac driving with an impedance analyser and then analysed using the Python script to extract the MEMS mechanical parameters. Resonance frequency and quality factor across all devices in second full wafer run are shown in Fig. 3.5.17. Measurement histograms are shown in Fig. 3.5.18. As it can be seen, devices in eleven reticles were found not to resonate, plus one outlier device that was

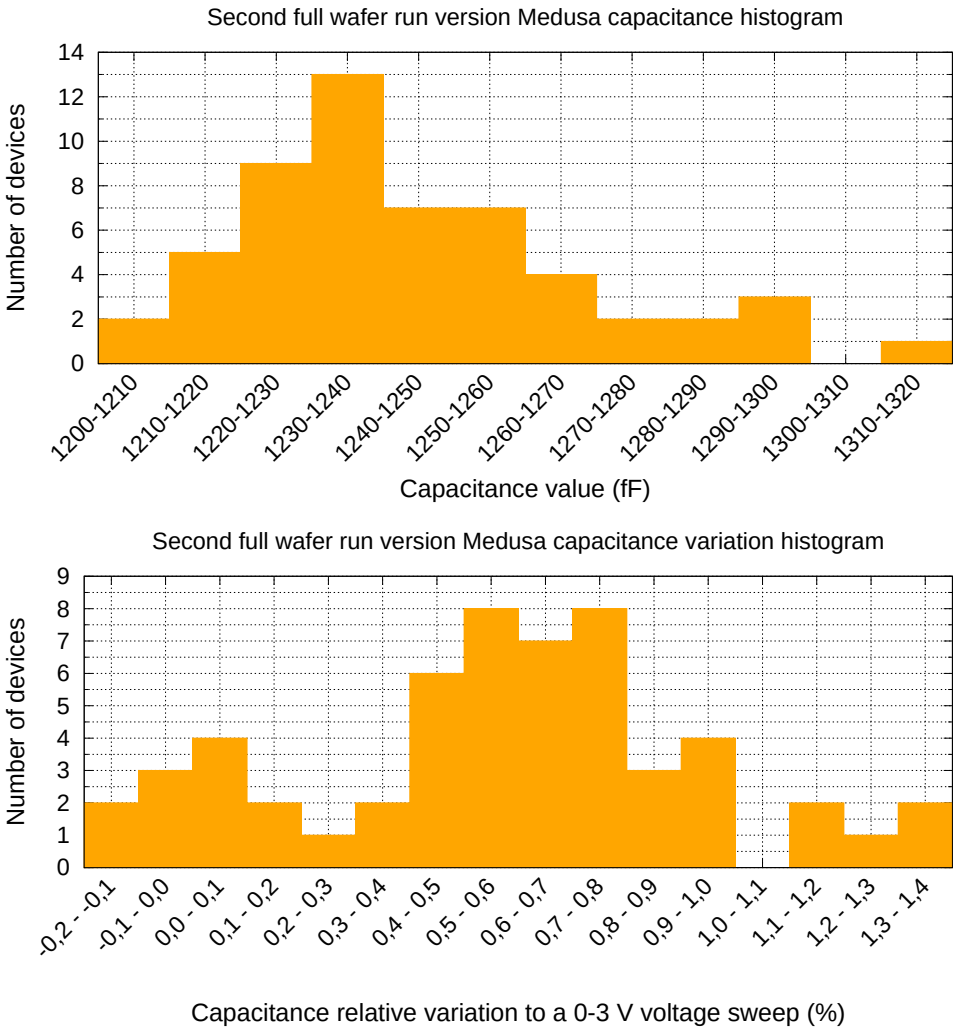
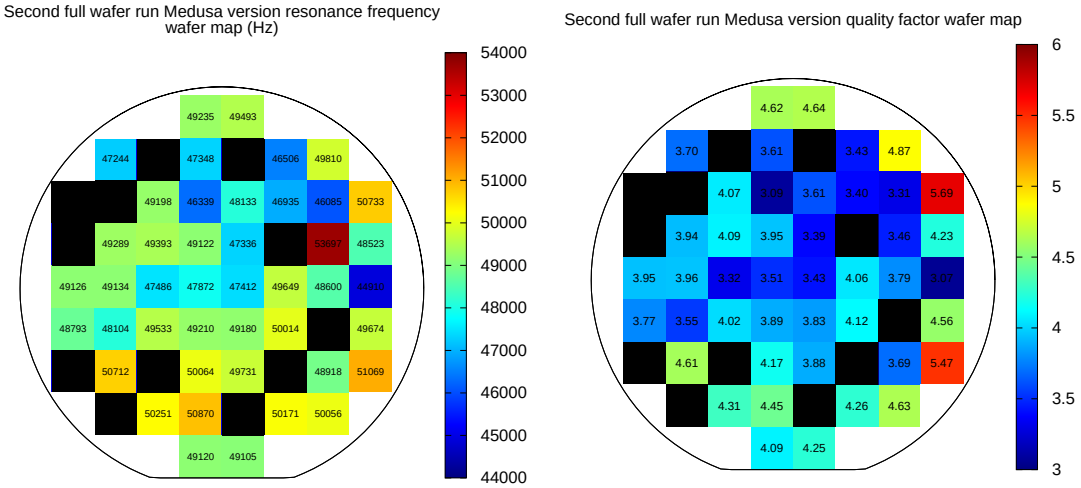


Figure 3.5.16: Second full wafer run version of the Medusa device capacitance value and capacitance variation for a C-V measurements between 0 V and 3 V for 55 and 50 devices respectively.

discarded as it resonated at a frequency 80% higher than the rest of devices. Hence, resulting in a 78.6% yield. This value is very similar to the first full wafer run Medusa device. However, the non-working devices are spread in a circumference-like shape similar to the non-working Quadspring devices in the same wafer, with an approximate center slightly shifted left above from the center of the wafer. This circumference is approximately a line where, outwards, resonance frequency and quality factor are higher. A possible explanation could be a non-uniformity of metal residual stress or metal thickness during the wafer fabrication at SMIC foundry that causes spring thickness or mass variations, or a non-uniform etching rate at Memsstar, that also causes mass variations as vHF also attacks aluminium (but at a much slower rate), or springs close to anchors slightly less etched.

3.5.3 The Octospring device

Due to the important residual stress in SMIC process metals, the Octospring device ended up with an important plate deformation in second full wafer run. As a consequence, the device drive and sense electrodes (this is, the rotor and stator of the MEMS) got short circuited. A confocal image where the mentioned curvature is shown is in Fig. 3.5.19 (a). Fortunately, TSMC process provides a BEOL metallization with much less residual stress, resulting in much flatter MEMS structures



(a) (b)

Figure 3.5.17: Second full wafer run version Medusa device resonance frequency (a), and quality factor (b) wafer map.

after release. As a consequence, the Octospring included in the Recollection chip proved to be wet etching resistant. An optical image of the device is shown in Fig. 3.5.19 (b).

The etching of Recollection samples was performed at the Universitat Politècnica de Catalunya Electronic Engineering department clean room using Hydrofluoric acid (HF) as the etchant. Silox Vapox III (from Transcene Company, Inc.) was used, which is a commercial product that provides HF diluted for semiconductor use in a concentration between 1% and 5%. After the etching step with Silox Vapox III, the samples were rinsed along several steps using first H_2O to stop the etching, and then acetone, Iso-Propylene Alcohol, and Methanol in order to finish with a low surface tension liquid that minimizes plate stiction during the baking step. This method has been successfully used several times in the research group [110, 130, 131].

The manufacturer claims that Silox Vapox III etching rate is 4000 $\AA/min$. However, previous works report experimental etching rate measurements of 960 $\AA/min$ in TSMC 0.35 μm [132] and IHP 0.25 μm [110]. Nevertheless, etching rate has an important dependency of the structures geometry [110]. For this reason, various etching times have been used ranging from 20 up to 50 minutes, etching two samples for each time. 20 minutes proved not being enough as one sample did not resonate while the other one did, but at a much higher frequency than the rest, indicating a potential partial etching. Similarly, times above 50 minutes resulted in collapsed devices. However, the rest of etching times resulted in working devices. Fig. 3.5.20 shows the histogram of the device capacitance with a 0 V biasing. As it can be seen, there is an important dispersion of values, with two different ranges with maximum devices. One possible explanation may be that, during the baking step, water droplets between the MEMS stator and rotor generate a force that pushes the MEMS plate downwards, causing a plastic deformation on the MEMS springs at two different height equilibrium points. Another explanation may be effect of the Cassimir force, as proposed in [64].

As this device's springs are quite stiff, vacuum was needed to measure the resonance frequency. Fig. 3.5.21 shows the devices resonance frequency and quality factor measured with a biasing voltage of 3 V and a pressure of 1 $mbar$.

It is possible to see that there exists a correlation between the etching time and the resonance frequency. It is important to take into account that these samples were manufactured in a TSMC

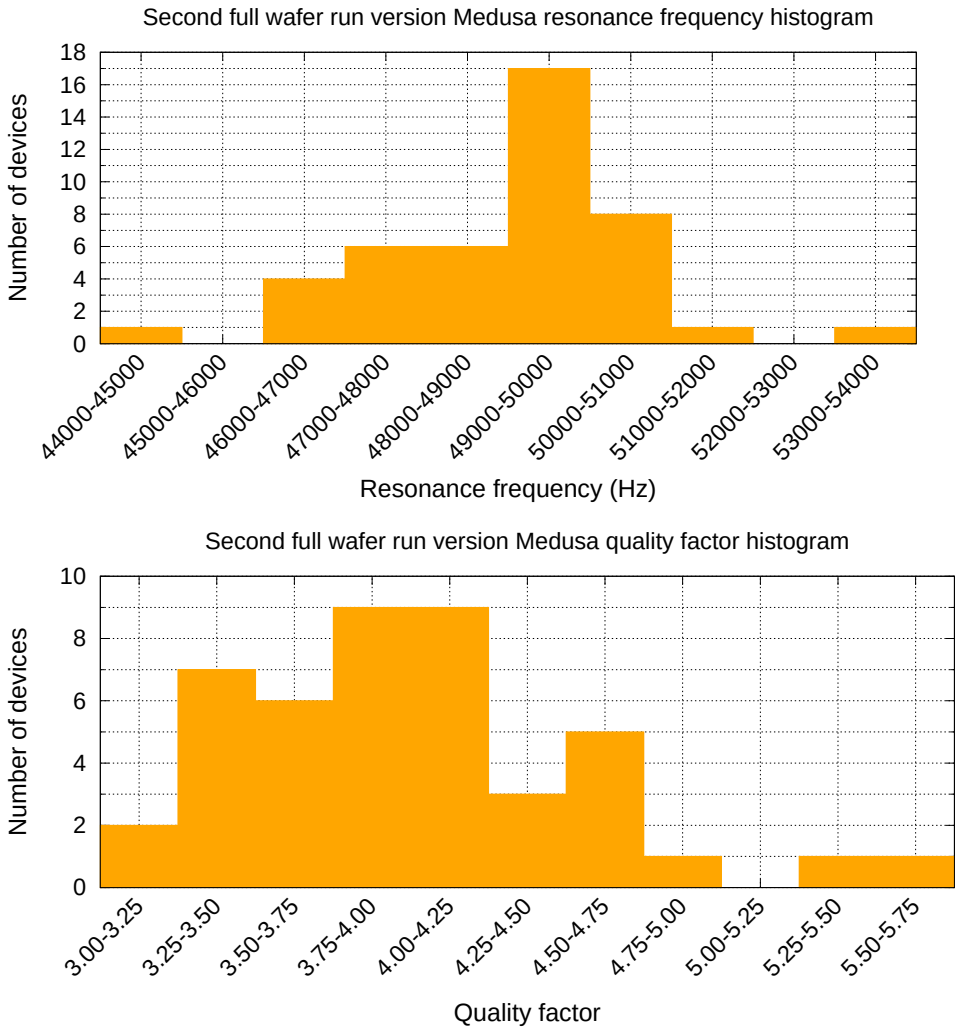
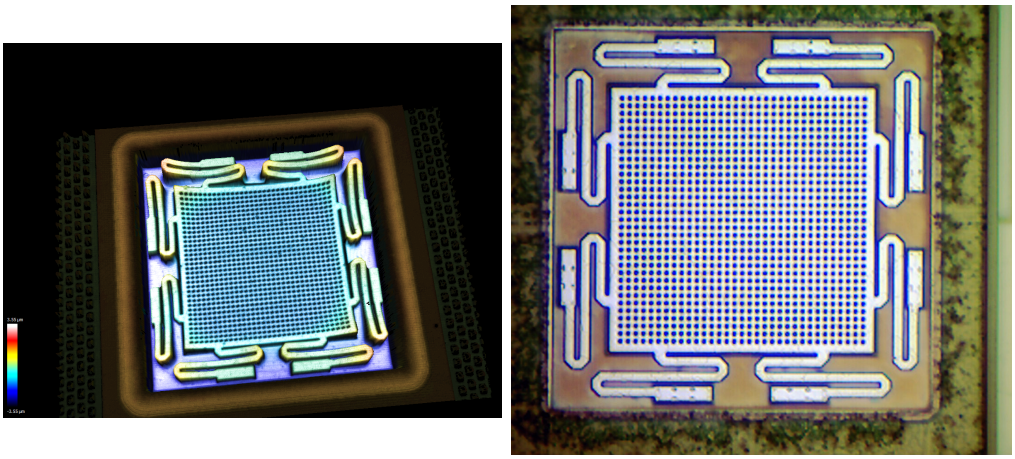


Figure 3.5.18: Second full wafer run version of the Medusa device resonance frequency, and quality factor wafer measurements histogram for 44 devices.



(a)

(b)

Figure 3.5.19: Octospring device in second full wafer run confocal image that shows the important plate curvature (M6) (a), and optical image of the Recollection chip Octospring MEMS.

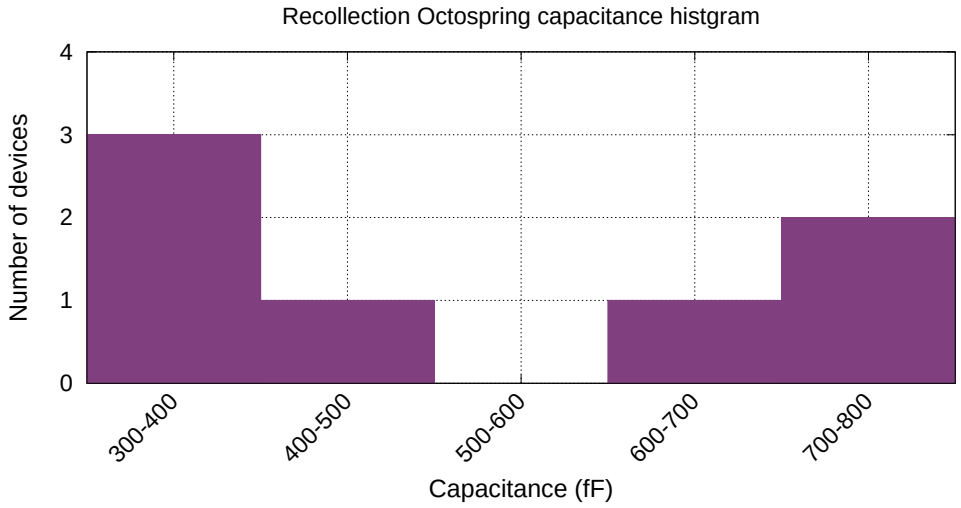


Figure 3.5.20: Recollection Octospring device capacitance histogram of 7 devices when biased with 0 V.

MPW run, so it is not possible to know the position of each sample in the wafer. Nevertheless, among process variations, etching time seems to impose in these measurements. A possible reason of this frequency reduction with increasing etching time may be the etching around the springs anchors, which increases its effective length and reduces the spring factor [131]. Another possible explanation may be that HF Aluminium selectivity may still not be high enough to prevent etching some nanometres of the springs and mass structures. This slight springs aluminium etching reduces the spring cross sectional area. As spring k factor is a function of width raised to 3 [129], it can easily overcome plate mass reduction and produce an effective resonance frequency lowering.

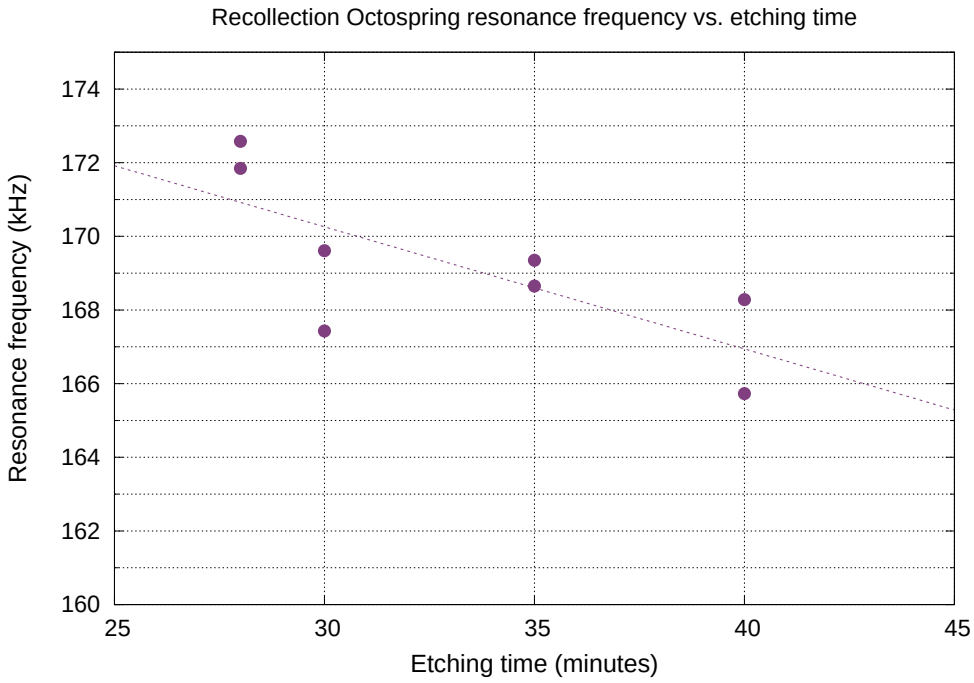
3.6 Devices comparison

Table 3.1 shows a summary of the designed MEMS magnetometers characteristics. To compute AM sensitivity and device noise, some things have to be taken into account:

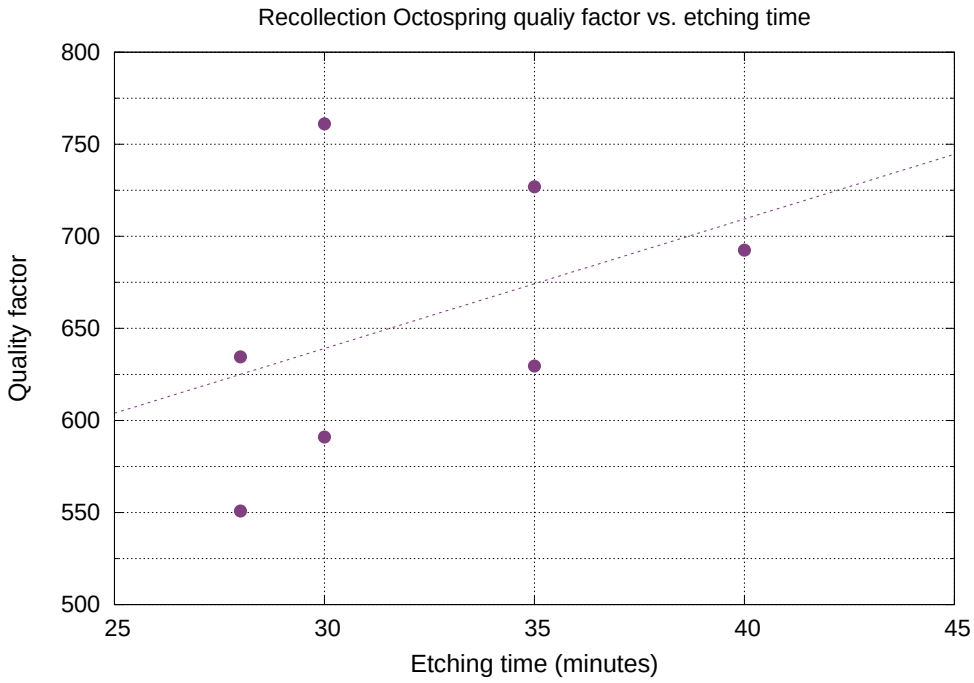
- MEMS rotor mass (m) has been roughly estimated from layout as 100 ng for all devices.
- Equivalent spring stiffnes is $k = (2\pi f_r)^2 m$.
- Nominal IMD distance has been used as the gap distance.
- A biasing voltage of $V = 1\ V$ is considered.
- Damping (b) inside noise has been computed with $b = \sqrt{km}/Q$.

For this reason, sensitivity figures must be handled with care.

Using Octospring as a comparison (as it is the only device measured at vacuum), it can be seen that sensitivity figure is much lower than chapter 2 device sensitivity. The main consequence is the fact that devices in chapter 2 recirculate tens of times the driving current (as shown in fig. 2.2.1), making the device effective length to be much longer than its real, physical length. In contrast, Octospring device does not allow the recirculation of current as it is made up of a single metal piece. On the contrary, Medusa device can be easily modified to allow the recirculation of current. Regarding this latter device, its longer and softer springs also provide a lower k factor compared



(a)



(b)

Figure 3.5.21: Recollection Octospring measured resonance frequency (a), and quality factor (b). Note that resonance for one 40 minutes device was to faint to get Q.

with Octospring, making it to be even more sensitive.

Unfortunately, table 3.1 can not be used to compare the devices presented in this chapter with other devices reported in the literature. The reason is that in all cases, sensitivity values are given in $V/\mu T$ units, measured at the output of the amplification chain without describing the amplifiers gain. Doing so, the MEMS sensitivity to magnetic field is multiplied by the gain, making

it impossible to know the real device sensitivity.

Table 3.1: Comparison of MEMS devices presented in this chapter

Device	Quadspring (1^{st} full wafer run)	Quadspring (2^{nd} full wafer run)	Medusa (1^{st} full wafer run)	Medusa (2^{nd} full wafer run)	Octospring (Recollection)
C (fF)	323 ± 163	1197 ± 57	118 ± 18	1244 ± 24	869
ΔC(fF)	n/a	2.5 ± 4.8	2.7 ± 1.3	7.0 ± 4.5	10.7
ΔC(%)	n/a	0.21 ± 8.56	2.3 ± 1.1	0.56 ± 0.36	1.23
f_r(kHz)	n/a	20.39 ± 12.94	56.78 ± 5.08	48.94 ± 1.56	172.58
Q[a]	n/a	1.48 ± 0.48	7.29 ± 1.59	3.85 ± 1.29	634.5
Estimated sensitivity[b] ($fA/\mu T \cdot mA$)	n/a	1.59	2.82	1.73	20.26
Estimated noise[c] ($fA/\sqrt{Hz}$)	n/a	5.77	7.68	6.01	10.23

[a] Quality factor at ambient pressure excepting Octospring, measured at 1 $mbar$.
[b] AM sensitivity using equation (3.1).
[c] MEMS output current noise using equation (2.3).

3.7 Conclusions

In this chapter various 2-axis Lorentz-force MEMS magnetometer devices have been proposed, manufactured and measured. Various MEMS topologies have been investigated in different technologies and etching processes.

SMIC 180 nm process offers a BEOL metallization with an important residual stress that curves metal structures made with a single metal layer. This has been repeatedly observed in Quadspring device, whose springs have suffered an important curvature. In order to compensate this residual stress, MEMS devices in this technology must be designed with stacks of metals. A good example of this approach improvement is the Medusa device, whose springs are a stack of M3 up to M5 metals and vias that importantly minimize the metal curvature: Quadspring 52 μm long M4 springs show a maximum to minimum height of 3 μm, while Medusa 110.4 μm long springs present a maximum to minimum spring height of 290 nm. The good point of SMIC demanding MEMS characteristics is that devices must be designed to be very robust. It is good in terms of technology migration, as it ensures a good success ratio when the destination technology offers flatter metallizations, such as TSMC 180 nm.

Quadspring device in SMIC, with parallel M2 and M4 springs resulted in very curved springs prone to M2 to M4 springs stiction. As a consequence, this device presents a very poor yield that requires an important redesign of the springs. In Recollection run, this device showed to collapse when wet etched, probably due to their very soft springs that do not support stiction during baking step. However, it would be interesting to test dry etching, using vHF, in using some TSMC samples of this device. As TSMC offer flatter metals when released, it is very likely that devices show a good yield and performance.

Medusa device presented in this chapter offers a yield around the 80%. Such good result is partly due to the spring nature of this device, consisting in a stack of various metals and vias that surround SiO_2 and minimize the curvature. Various strategies may be followed in order to increase the yield to values closer to currently industry demands: 1) making the springs shorter to have stiffer devices less likely to collapse, 2) increase the metal stack by including M2 in order to further minimize the MEMS curvature, 3) increase gap distance to reduce collapse probability. Another interesting aspect of this device is that it offers a shielding of the current signal that may couple to the sense electrode, reducing the sensor offset. For this reason, it seems to be a good starting point for a CMOS-MEMS commercial compass solution.

Finally, the Octospring device has shown to be very dependent on the process curvature. Given that this is a simple parallel plate design, though, curvature may be easily compensated by converting the current M6 plate to a plate made up of a stack of metals.

Chapter 4

CMOS-MEMS magnetometer sensor

In chapter 2 a complete system was proposed for the readout of MEMS magnetometers. It was implemented with off-the-shelf components on a PCB that allowed the measurement of a CMOS-MEMS magnetometer fabricated using the BEOL part of a standard CMOS process. AM readout was demonstrated as a feasible solution, even using commercial components on a PCB, which provides large parasitics that worsen performance. In chapter 3, different CMOS-MEMS magnetometer devices were designed, manufactured and measured. For each one, problems were identified and potential solutions were proposed. Also the consequences of wafer level variability on devices performance was studied.

The remaining step is the integration of both parts of the complete system: the MEMS and the electronic circuitry, side-by-side on a single chip area. Doing so would bring plenty of benefits to the complete system: low parasitics and improved noise figure, low area and volume, and lowest manufacturing cost. Moreover, if the integration of CMOS-MEMS compasses, accelerometers, and gyroscopes in the same die area that the electronics is achieved, the volume of a 9 Degrees Of Freedom (DOF) sensing system would greatly shrink.

To fill this gap, in this chapter an integrated signal readout for Lorentz force MEMS magnetometers is proposed. The circuit consists in both electrostatic and current driving of the integrated MEMS magnetometer, the low noise amplification stage, as well as an integrated thermometer and basic digital communications. Further signal processing, such as analog to digital conversion and digital signal processing have been performed off-chip in order to speed up design and to allow easy reconfigurability. Doing so, a flexible platform is achieved, which serves as the idea proof-of-concept. However, it is important to take into account that the off-chip circuitry can easily be integrated on-chip in the final product.

4.1 Design challenges

In chapter 2, the design of a CMOS-MEMS readout circuit design was detailed using commercial off-the-shelf components. The problems that arise using this approach were identified and, when possible, solutions to avoid them were proposed and implemented. Also, the benefits of the electronics integration on a chip were forecast. While it is true that the integration provides several benefits to the readout circuitry, during the process novel problems appear that are not present in the design of a PCB based circuit. This section discusses these problems and solutions.

4.1.1 Sensor noise

One of the main concerns when designing sensors is noise, as it limits the maximum resolution of the system. In MEMS readout systems, there exist two main noise sources that must be carefully analysed and designed in order to get as much resolution as possible. These main noise sources are the MEMS device itself, and the LNA. There are, obviously, other noise sources in the system. However, these two are the most important ones given that they are at the very beginning of the amplification chain. Hence, regarding the Friis formula for noise factor, they are the blocks that contribute the most to the system noise, as sensed signal is not amplified yet.

4.1.1.1 MEMS noise

MEMS devices noise is a consequence of the Brownian motion, which is the agitation of, in this particular case, the MEMS movable plate by the surrounding air particles. This particles have, in turn, a random movement due to the thermal vibration [112]. The resulting MEMS output current noise has been previously derived in section 2.4.1, which is repeated in (4.1) for convenience.

$$\bar{i}_s = \frac{\epsilon_r \epsilon_0 AQV\omega_r}{g^2 k}\sqrt{4k_B T b} \tag{4.1}$$

where k_B is the Boltzmann constant, T the device temperature in Kelvin, sensing area A, gap g, spring constant k, damping coefficient b, quality factor Q, resonance frequency f_r, and biasing voltage V.

4.1.1.2 LNA noise

Amplifier noise is a consequence of the different noises that CMOS transistors experiment. In low frequency CMOS amplifiers there mainly exist two dominant noise sources: flicker (or 1/f) and white (or thermal) noise [133].

Flicker noise dominates at frequencies up to some tens of *kHz* (depending on the amplifier white noise), and has a noise spectrum shaped as $1/f^{\alpha}$. The phenomenon explaining this noise origin is still unknown, even though there are contradicting theories with experimental evidence [134, 135]. A good in depth discussion on flicker noise can be found in [136]. No matter the physical modelling, there exists an empirical transistor input-referred model that describes this noise:

$$\overline{v_{1/f}} = \sqrt{\frac{K_F}{C'^2_{ox} WLf}} \tag{4.2}$$

where K_F is a technology dependent parameter, larger for P- than NMOS transistors, C'^2_{ox} is the oxide capacitance per unit area, W and L are the transistor width and length, and f is the frequency.

White noise, on the other hand, has a well-known origin: it is caused by the random Brownian motion of electrons in the transistor medium. For strong inversion operation transistors, the equivalent input-referred noise is

$$\overline{v_w} = \sqrt{\frac{8}{3}\frac{k_B T}{g_m}} \tag{4.3}$$

where k_B is the Boltzmann constant, T the temperature and g_m the transistor transconductance. As it can be seen in (4.3), white noise has a flat spectrum.

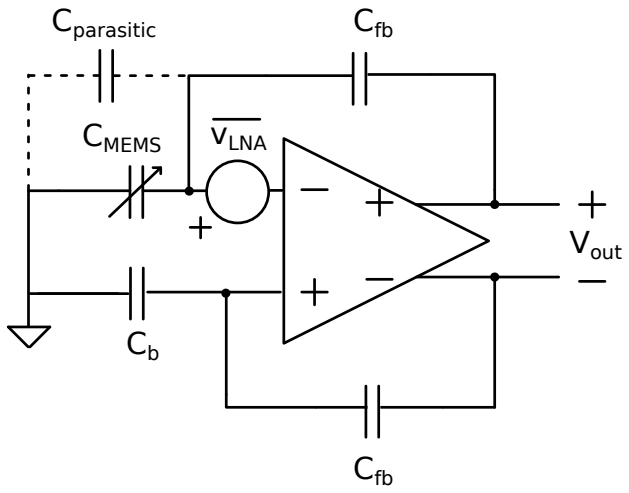


Figure 4.1.1: Simplified diagram of the LNA-MEMS interconnection. From the noise point of view, capacitive driving is a virtual ground. $C_{parasitic}$ on the top of the figure represents MEMS output parasitic capacitance as well as routing and LNA input transistor gate capacitance. C_{fb} are the LNA feedback capacitors, C_b is the bridge capacitance of the MEMS C_{MEMS}. Finally, $\overline{v_{LNA}}$ represents the LNA input referred noise.

4.1.1.3 Flicker vs. white noises trade-off

Given that flicker noise decays with frequency, there exists a frequency where both flicker and white noise equal. It is called the corner frequency. Below this point, flicker noise dominates, while beyond, white noise does. In MEMS sensors that do not work at a resonance frequency, chopping technique is usually used, which consists in driving the MEMS at a frequency where flicker noise is not dominant. Doing so, baseband signal of interest is up-converted avoiding flicker noise. Previous works of the research group used this technique [99, 100, 109]. The chopping frequency can be set to be the same that the corner frequency. Doing so, noise is still 3 *dB* larger than white noise, but frequency requirements of the amplifier are not further increased. However, if amplifier has enough bandwidth, working at a frequency slightly higher than corner frequency results in a total noise equal to the amplifier white noise (this is, 3 *dB* lower that at the corner frequency). Moreover, corner frequency variations due to process or temperature are also avoided. As a drawback, though, increasing chopping frequency increases power consumption.

This chopping frequency selection has the advantage of giving flexibility to the amplifier design. For example, if there is enough die area, big transistors may be used to reduce corner frequency (by reducing flicker noise) and allow working at lower frequencies (see the section below to know why this is not always a good idea). Or the other way around. However, in resonant MEMS sensors the working frequency is no longer a design (in terms of electronic readout design) decision. Moreover, if device resonance frequency is too low, this may set impossible design constraints to the LNA, requiring to greatly increase LNA input transistors area to shrink flicker noise or having to accept working with an important amount of such noise. Medusa and Quadspring devices are good examples of low resonance frequency devices. For this reason, device and electronics design must be strongly interrelated.

4.1.1.4 Effect of capacitance in sensing node

It has been mentioned previously that parasitic capacitance at the MEMS-LNA sensing node increases system noise. And that it was one of the main advantages of CMOS-MEMS sensors integrated in the same die. The reason of why this is an important thing comes from the analysis of output-referred noise of the input referred LNA noise $\overline{v_{LNA}}$ in Fig. 4.1.1. LNA noise at the output

follows equation (4.4)

$$\overline{v}_{out} = \overline{v_{LNA}} \left(1 + \frac{C_{MEMS} + C_{parasitic}}{C_{fb}} \right) \tag{4.4}$$

where C_{MEMS} is the MEMS capacitance and $C_{parasitic}$ represents all the parasitic capacitances that hang from the MEMS-LNA node: MEMS output parasitic capacitance, LNA input transistors gate capacitance, and wiring capacitance. Putting together equation (4.4) with (4.3) (considering that the system works beyond the corner frequency) creates an important trade-off between transistor dimensions and parasitics where it is possible to make the amplifier work in a noise minimum by properly sizing LNA transistors. This topic is beyond the scope of this work, but the reader is referred to [137] where this trade-off is analysed with strongly inverted transistors, and [109] for an all-region model analysis.

4.1.2 MEMS driving

Another important aspect to take into account during the design of this circuit is the MEMS driving. Contrary to other MEMS such as accelerometers, MEMS magnetometers require both electrostatic and current drivings. Design implications are analysed in the sections below.

4.1.2.1 Electrostatic driving

Electrostatic driving circuit is not complicated, but must take into account a couple of important items. First, the block must be capable of driving quite large capacitances: both the MEMS and bridge capacitance. And integrating the MEMS importantly reduces parasitics at the driving node. Doing so, a good slew-rate can be achieved without the need of increasing buffer current driving capability (as it usually comes with increased power consumption).

Second, electrostatic driving of MEMS resonators provides one relaxed specification. Due to the filtering nature of the MEMS, which is equivalent to a high selectivity RLC bandpass filter, any voltage driving the MEMS will see its harmonics filtered out. For this reason, the actual shape of the driving signal is not important, as no significant driving difference will be observed. Bridge capacitance does not have this filtering skill, which results in a sine and a square signals added up at the output of LNA. However, the resulting harmonics can easily be filtered later on the amplification chain.

4.1.2.2 Current driving

In chapter 2, current driving was performed using an improved Howland current source. While it is an interesting circuit for off-chip precision current driving, so many resistors require an important amount of area that integrated designs can not always satisfy. However, current mirrors, with a proper switching, are a good alternative for square-shaped current driving with some degree of current amplitude selection.

Similar to electrostatic driving, the shape of the driving current is not important. And that is good news if switched current mirrors are used because of design simplicity. However, an important drawback arise: driving a square shaped current to a sensor that only takes profit of the sinusoidal component is an important waste of power (this also applies for electrostatic driving). This is an aspect to take into account if these sensors are to be included in commercial, low power solutions. However, for research purposes, simplicity have been preferred.

4.1.3 MEMS characteristics

Finally, prior to the design of the electronics, it is important to know the characteristics of the MEMS that the circuit is going to perform the readout of. The specifications of the electronics described throughout this chapter took into account the characteristics of a MEMS magnetometer that is a variation of the MEMS in chapter 2 designed by Mr. Juan Valle. Unfortunately, the measurements of this device integrated with the electronics was not possible: the die samples were vHF released by Memsstar, but the process was unsuccessful as device measurements concluded that the device was collapsed. Due to the long time needed to 1) tape out a new design, 2) manufacture it, and 3) do the etching step at Memsstar (the longest step), it was decided that the most conservative option was to adapt the devices in chapter 3 to be wet etching resilient (Quadspring and Medusa) as well as to design a very conservative device (Octospring). From these three devices, only Octospring survived the wet etching. In table 4.1 the main specifications of the modified device from chapter 3 and Octospring are shown.

Table 4.1: MEMS characteristics for the design of the electronics

	Device in chapter 2 variation	Octospring
Sensor capacitance (C_0) (fF)	1400	869[a]
Output capacitance (C_p) (fF)	1200	500[b]
Sensitivity ($pA/\mu T \cdot mA \cdot V$)	28.88	0.02[c]
Noise ($fA/\sqrt{Hz}$)	77	10.23[c]
Wire resistance (Ω)	3000	0.3[b]
Resonance frequency (kHz)	130	170

[a] Measured value from chapter 3.
[b] Value from post-layout simulation.
[c] Estimated value from table 3.1

As custom electronics was not designed for the Octospring, both devices will be taken into account during the chapter.

4.2 Designed readout circuit

The MEMS readout circuit was designed and manufactured in the Recollection test chip. The simplified top level integrated circuit is shown in Fig. 4.2.1. The circuit can be divided into four parts consisting of blocks with similar functions:

- MEMS sensor: this block consists in the various MEMS included in the chip, as well as the various multiplexing stages designed to select the MEMS under test.
- MEMS driving: it contains the electrostatic driving circuit and the MEMS current driving.
- Amplifier: this category includes the programmable bridge capacitance, the LNA and the buffers driving the chip pads.
- Auxiliary blocks: a register bank used for basic circuit reconfigurability and a bandgap reference that generates biasing current references as well as temperature sensing.

Throughout this section, the different blocks will be described, and their functionalities and design decisions will be justified.

4.2.1 MEMS sensor

As explained in chapter 3, the Recollection test chip includes various MEMS magnetometers: the Quadspring second version, the Medusa second version, and the Octospring first version. The first

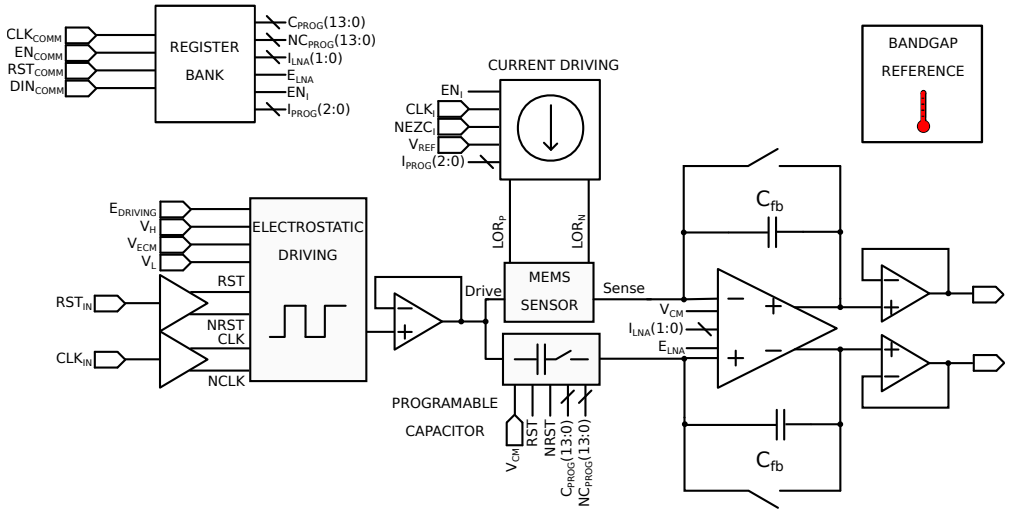


Figure 4.2.1: Recollection chip top level simplified schematic.

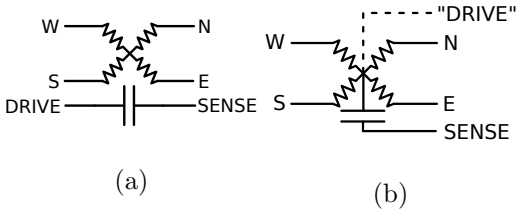


Figure 4.2.2: Quadspring and Medusa (a) and Octospring (b) equivalent electrical model.

two are designed to allow independent electrostatic and current driving, as both are electrically isolated in the MEMS. Octospring, on the contrary, cannot be electrostatically driven. The equivalent electrical model of the Quadspring and the Medusa devices is shown in Fig. 4.2.2 (a). The resistor network represents the spring and plate resistance of the current carrying paths, all of them meeting in the middle of the device. Electrically isolated, the drive to sense nodes capacitance is shown below.

Octospring model is slightly different, as shown in Fig. 4.2.2 (b). In this device, the rotor is a single aluminium metal plate where the current circulates. Hence, no electrostatic driving is possible. As a consequence, the equivalent circuit shows that the "driving" node of the MEMS is in the middle of the resistive network. It is a lumped model simplification, as in reality, it is a distributed capacitance across all the MEMS plate. In the ideal case where the total resistance of the plate is 0 Ω, the plate does not suffer any voltage drop and its voltage is constant. As MEMS sensing plate is also a dc voltage, there is a dc voltage drop V_{MEMS} between MEMS rotor and stator. Lorentz force generated by current crossing the MEMS generates a plate displacement and a consequent capacitance variation $C(t)$, generating a charge movement resulting in an output current as shown in (4.5).

$$i_{MEMS}(t) = \frac{dq_C(t)}{dt} = C\frac{dV_{MEMS}(t)}{dt} + V_{MEMS}\frac{dC(t)}{dt} = V_{MEMS}\frac{dC(t)}{dt} \tag{4.5}$$

Where q_C is the charge movement due to the capacitance variation $C(t)$ produced by the Lorentz force.

In reality, the plate resistance is not zero, and hence the first term of the derivative will not be null. The resulting current of this term, as it does not have magnetic field information, generates an offset. In order to minimize this offset, it is important to avoid any voltage difference across the plate. In the case where the device is driven, for instance, from N to S, there exists a voltage difference between N and S. This may drive the sensor in a different resonance mode if the loop

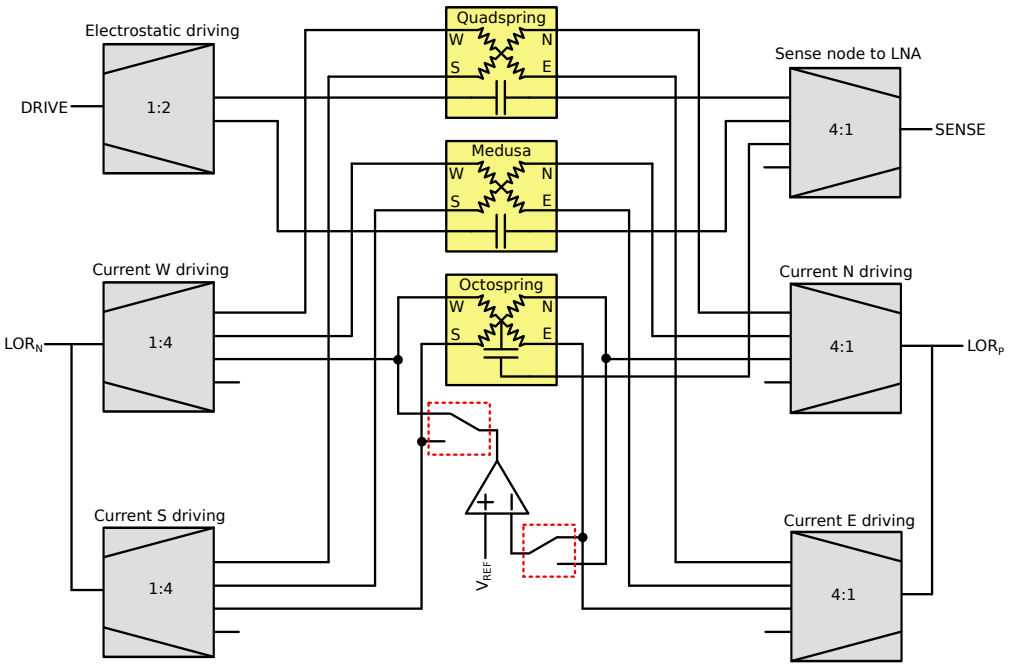


Figure 4.2.3: MEMS electrostatic and current driving circuit schematic. The sensing electrode multiplexing, and the Octospring unity gain buffer are also depicted.

is not correctly locked at the out-of-plane resonance mode. However, plate regions close to E and W, if left unattended, may lead to other unwanted modes. Specifically during start up when the complete closed loop system locks to a resonance mode. In order to avoid this problem, when two electrodes are not used, instead of leaving them at a high impedance, they are connected one to each other with a unity gain amplifier. Doing so, both non-driven sides of the plate are driven at the plate ideal dc voltage. This buffer, as well as all the multiplexing circuitry implemented in the Recollection chip is shown in Fig. 4.2.3.

4.2.2 MEMS driving

Electrostatic driving is applied at the Drive node depicted in Fig. 4.2.3, while Sense is conveyed to the LNA input (as explained above, the former does not apply to the Octospring device). Current driving is performed between $\mathrm{LOR_P}$ and $\mathrm{LOR_N}$. The circuits associated with these nodes are explained in the following two sections.

4.2.2.1 Electrostatic driving

The main objective during the design of this block was to allow the possibility of modifying the driving voltage common mode and amplitude values without the need of an integrated DAC. As a consequence, all these voltages (Drive common mode, and maximum and minimum values) are provided from off-chip circuitry to the block through chip pads (same with Sense common mode, that is controlled by V_{CM} signal and sets LNA common mode). Hence, this block has been designed as a network of switches that provide the following functionalities:

- Independent electrostatic and current driving frequencies (and phases).
- Driving disable in case electrostatic driving is not necessary. Doing so sets the driving voltage to the input common mode dc voltage.
- Easy off-chip change of both common mode and driving amplitude (using Arduino DACs, for

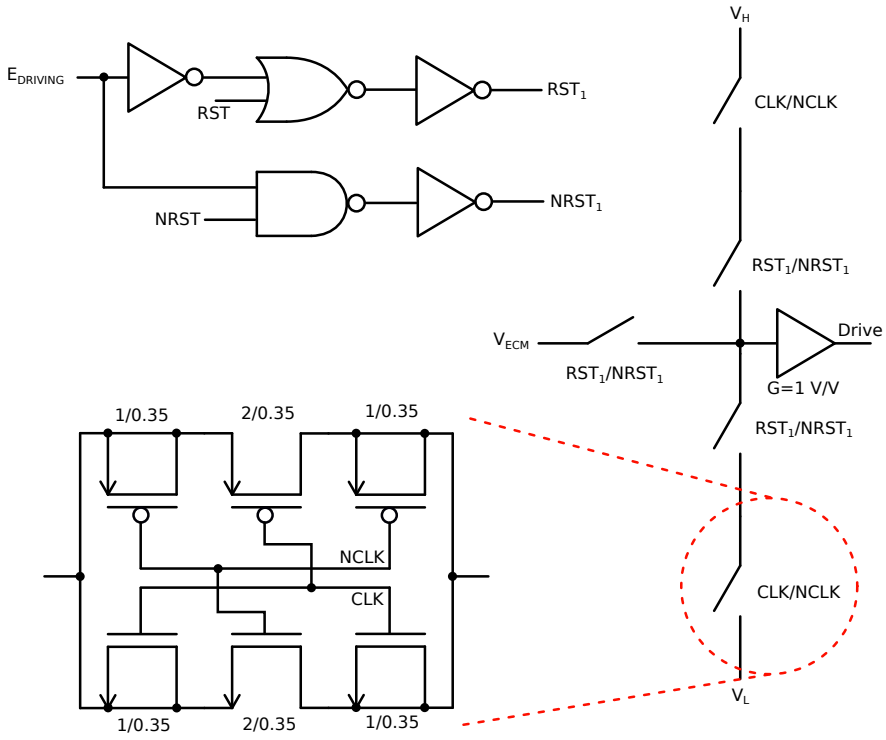


Figure 4.2.4: Electrostatic driving circuit. Switch transistor dimensions are shown as width/length in μm next to each transistor.

example).

The circuit implemented is shown in Fig. 4.2.4. As this block is intended to work at a quite high frequency (at resonance), switches have been designed to have small transistors in order to minimize parasitic capacitances and improve slew rate. Hence, all transistors (both N- and PMOS) have been designed with a very short length of 350 nm and a width of 2 μm. One important problem with CMOS switches is that transistor gate capacitance stores charge. This charge, during a switch transition generates charge injection at the drain and source nodes, generating a voltage spike. In order to minimize this charge injection, switch topology have been designed following the technique proposed in [138]: with the assumption that gate capacitance charge redistributes equally between transistor source and drain, placing one shorted (shorted source and drain) half sized (as each transistor only has to absorb half the charge) transistor at each side of the switch transistor, charge injection is absorbed and voltage peaking is minimized.

Logic gates on the top left part of the circuit translates the driving electrostatic driving enable signal $E_{DRIVING}$ into the reset signals. Hence, when $E_{DRIVING}$ = HIGH, electrostatic driving is enabled and drives the MEMS with a square wave whose voltage ranges between V_H and V_L at CLK frequency, unless RST_1 is enabled by RST. Otherwise, when $E_{DRIVING}$ = LOW, electrostatic driving is disabled and MEMS is biased with the dc voltage in V_{ECM}. The RST and $E_{DRIVING}$ may seem to have the same function, but the two signals have been used in order to allow 1) electrostatic driving disable without affecting the other circuit blocks (i.e. LNA and current driving), and 2) allow low duty cycle reset of LNA, a feature that will be explained below.

4.2.2.2 Current driving

Current driving block has been implemented with complementary positive and negative programmable current sources. In between these two current sources, an H bridge has been implemented that changes the direction of the currents polarity that drive the MEMS magnetometer, similar to

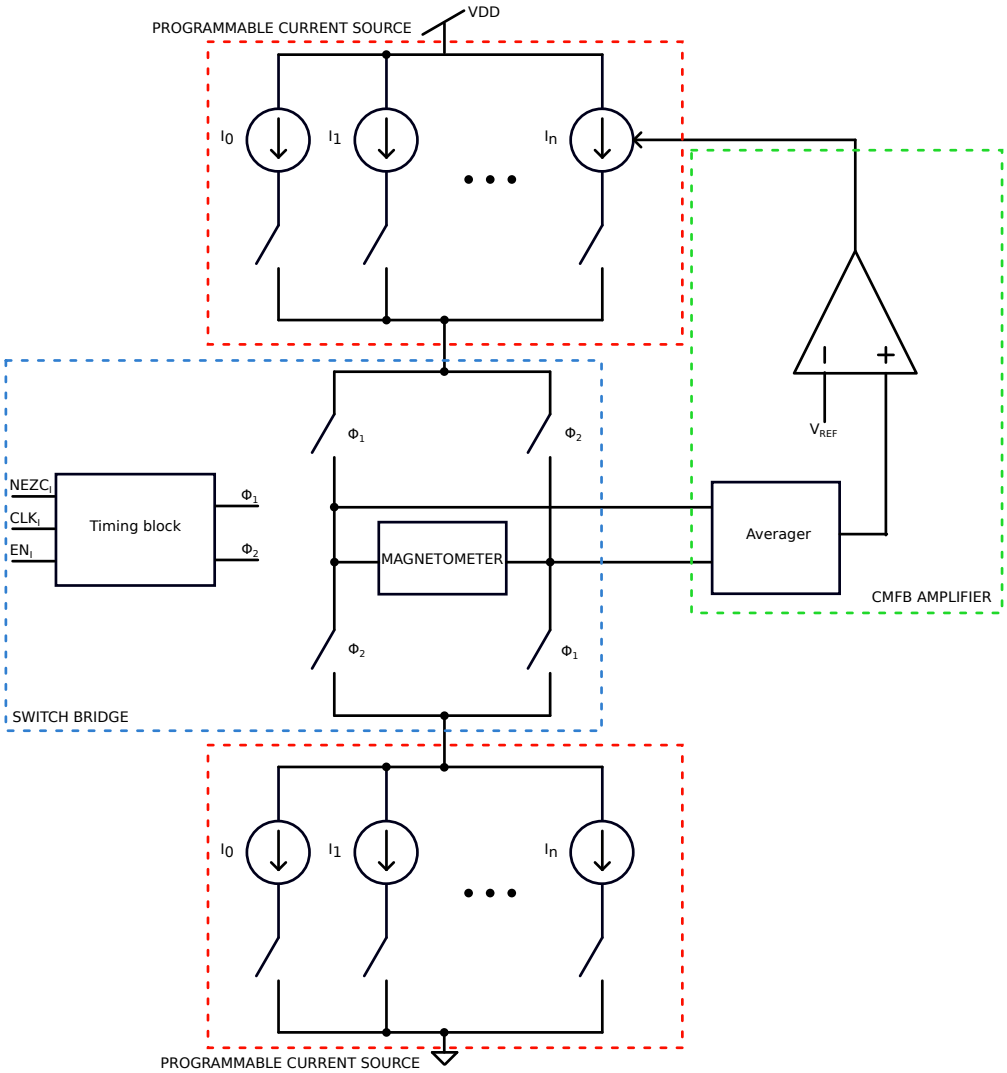


Figure 4.2.5: Block level of the implemented current source. It mainly consists in three sub-blocks, namely, the programmable current source (made up of P- and NMOS programmable current sources) inside red box, the switch bridge inside blue box, and the CMFB amplifier inside the green box.

those used to drive dc motors. Finally, a Common-Mode FeedBack (CMFB) amplifier extracts the common mode voltage of the current source output and, by adjusting the current of the PMOS programmable current source, it is capable of fixing the output common mode voltage to a given voltage. This, however, makes the transistors change their drain to source voltage as the sink current is forced by the NMOS current source. A block level schematic of the current source is shown in Fig. 4.2.5. More details of each sub-block are described below.

4.2.2.2.1 Programmable current sources Programmable current sources were designed to allow 3 bit programmability (8 current values) in order to adapt to the different resistive loads and sensitivities of different sensors. The designed current values are 16, 32, 64, 128, 256, 500, 1000, and 2000 μA_{pp}. These values do not change with temperature, as thanks to the bandgap reference design that will be explained in section 4.2.4.1, the reference current used for this block has a minimum change with temperature. The different currents are implemented with a set of current mirrors that are turned on and off depending on the selected current. To do so, a binary to thermometer encoder has been implemented that converts the 3-bit binary current selection into 8 bits that drive the current sources.

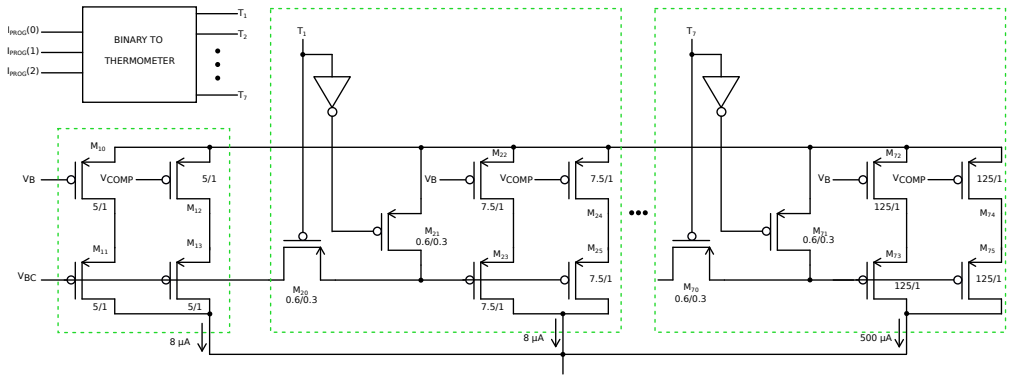


Figure 4.2.6: Simplified diagram of the PMOS current programmable current source. Inside green boxes, first two and last current sources are shown. Transistor dimensions W/L are in μm. In order to simplify the diagram, enable circuitry has not been included.

The current source is made of low-voltage cascoded current mirrors. As a consequence, voltage headroom required for the current sources to work at saturation region is very low, which maximizes the current source dynamic range and the resistive load it is able to drive. A simplified diagram of the PMOS current source is shown in Fig. 4.2.6. Inside the leftmost green box, the first current source, for 8 μA is shown. It can only be turned off by disabling the entire current source. V_B and V_{BC} are current source biasing signals, while V_{COMP} is the output of the CMFB. On its right, the second current source is shown. The control signal T_1 comes from the binary to thermometer encoder, which enables it for current selections of 32 μA_{pp} and above. When T_1 = LOW, transistor M_{20} is turned off, stopping V_{BC} propagation, while M_{21} is turned on, making the gate of M_{23} to be at the supply voltage and turning second stage off. Otherwise, when T_1 = HIGH, this second stage works identically to the first one, sinking 8 μA, which is added to the first stage current. Following stages work similarly, each one of them providing the required current to sink, in total, the designed current values listed before. Finally, binary to thermometer block has been designed with digital gates in order to turn on the blocks in Fig. 4.2.6. The block truth table is shown in table 4.2

Table 4.2: Binary to thermometer encoder truth table

B(2:0)	T(7:1)	Output current (μA)
000	0000000	16
001	0000001	32
010	0000011	64
011	0000111	128
100	0001111	256
101	0011111	500
110	0111111	1000
111	1111111	2000

NMOS counterpart is equivalent to the PMOS excepting that there is no CMFB control.

4.2.2.2.2 Common Mode Feedback amplifier The CMFB amplifier has been implemented in order to set the MEMS current driving around a given adjustable dc voltage, providing a constant dc biasing to the MEMS capacitance. This CMFB amplifier is very similar to the one implemented in the LNA. For this reason, the CMFB is explained in section 4.2.3.2.1.

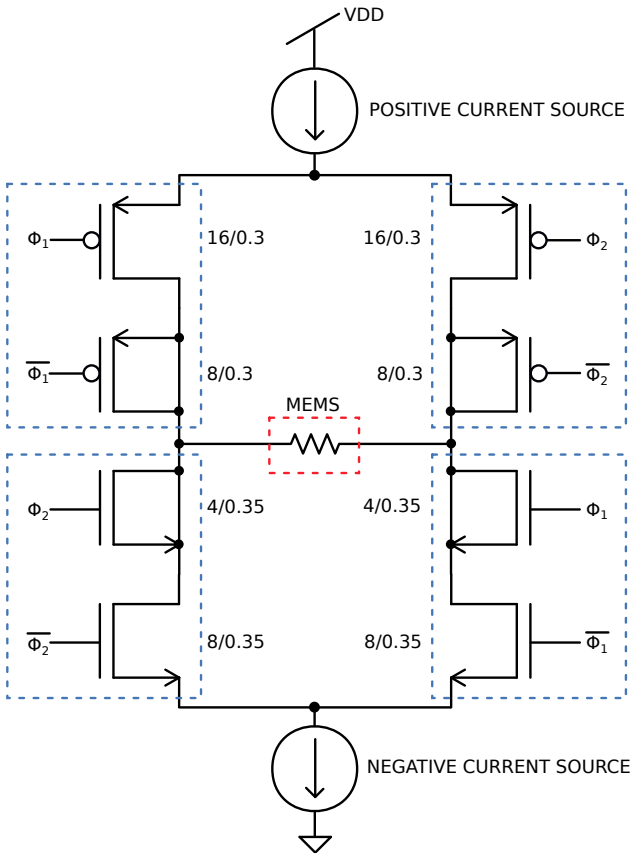


Figure 4.2.7: Bridge detailed diagram where transistors in each switch are shown. Each transistor size W/L is shown in μm.

4.2.2.2.3 Switch bridge The switch bridge that alternates the direction in which current flows into the MEMS resistance has been implemented as an H bridge. This block consists of four switches, two PMOS at the top and two NMOS at the bottom of the bridge. During the design of these switches, an important trade-off appears: the use of transistors as wide as possible is important in terms of reducing as much as possible the switch on resistance and to minimize voltage drop. However, doing so increases transistor gate capacitance, increasing charge injection during source disable transient. Given that current source headroom is limited in the case device variation of chapter 2 is used (a load resistance of $R_{wire} = 3\ k\Omega$ driven with 1 mA (during first period half when driven with 2 mA_{pp}) only leaves 300 mV for the upper and lower current sources assuming a zero switch resistance), minimizing transistor on resistance has been prioritized. However, in order to minimize charge injection to the MEMS, a half-sized, shorted transistor has been serially connected to each switch, close to the MEMS, as it is detailed in Fig. 4.2.7. Final switch resistance with the dimensions shown in the figure is 263 $m\Omega$ for PMOS switches and 169 $m\Omega$ for NMOS counterparts.

Finally, the bridge timing block has the important task of generating the bridge switches' driving signals. Two complementary signals need to be highly aligned, as any misalignment would lead to a bridge short. Even though it would not create a VDD to GND short thanks to the current sources, it may be an important source of common mode voltage variation if a large load is combined with a bridge short. Bridge timing block schematic is shown in Fig. 4.2.8. First, the CLK signal is divided into two paths. One is inverted, while the other one goes through a delay stage tuned with the inverter by simulations. Second, two anti-parallel inverting gates help force both signals to be equal by mutual feedback of each other's input. Next, after a buffering, a latch finishes the complementary signals alignment before the dual clock enters a selection block with switches (with adjusted delays) where four driving signals are generated: Φ_1, $\overline{\Phi_1}$, Φ_2, and $\overline{\Phi_2}$. During normal

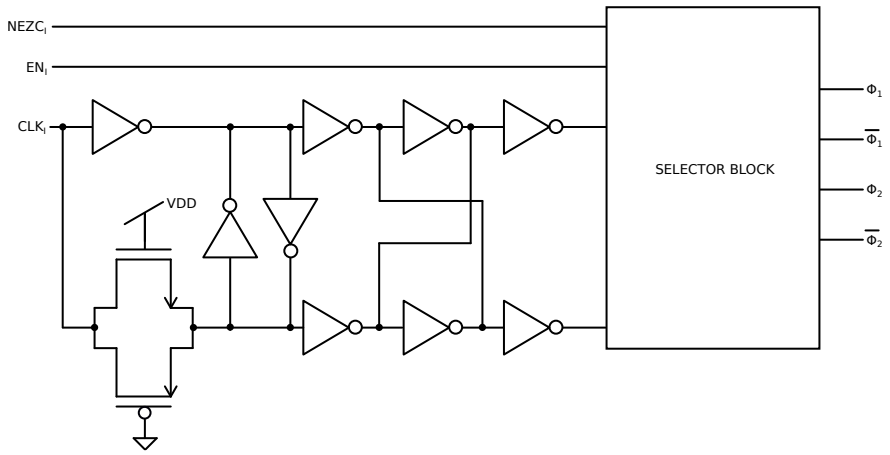
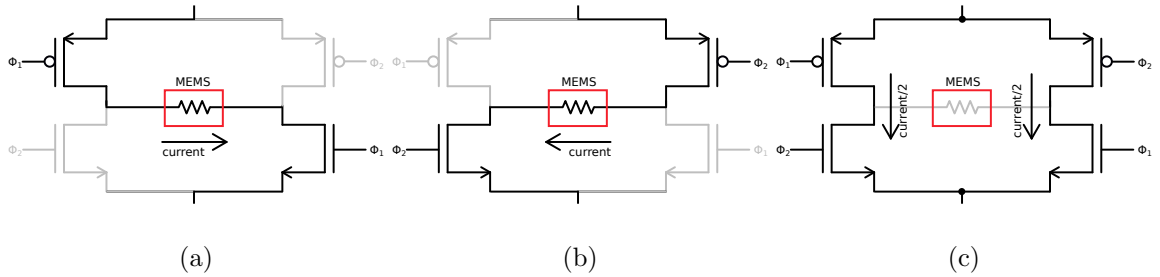


Figure 4.2.8: Bridge timing block schematic.



(a) (b) (c)

Figure 4.2.9: During normal current driving, switches state in (a) and (b) are intercalated to generate a square MEMS current driving, while (c) shows the switches state during MEMS zero current. Dummy charge injection absorption switches have not been included for simplicity.

operation, $\Phi_1 = \overline{\Phi_2}$ and $\Phi_2 = \overline{\Phi_1}$. However, four signals are required in order to be able to turn all switches on at the same time. Doing so, generated current goes through them and not through the MEMS ($I_{MEMS} = 0\ \mu A$), allowing the implementation of the current chopping modulation [79]. This implementation may not be the most efficient in terms of current consumption, but it responds to an important issue found during design: opening all bridge switches leaves the MEMS resistance electrodes at some voltage levels due to the parasitic capacitance of the MEMS and the circuitry, the latter being unknown before layout design and RC parasitic extraction. Discharging such charge through off switches is very slow, leading to discharging times comparable to the signal period. Moreover, if layout design generates a discharge mismatch between nodes, it may lead to some current flowing through the MEMS. Hence, signal characteristics where preferred over current consumption. In future designs this issue could be solved with an accurately designed switch connecting the MEMS electrodes to V_{REF}. The three working modes of the switch bridge are shown in Fig. 4.2.9.

4.2.3 Amplifier

The LNA is a critical block, as it is the first gain stage of the readout circuit. It must have enough bandwidth and sufficient gain at the working frequency. Moreover, LNA noise should not limit the MEMS resolution while, at the same time, have a stable input common mode in order to have a constant MEMS dc biasing.

Following these objectives, the implemented LNA in the Recollection chip is shown in Fig. 4.2.10. The LNA consists in a half bridge, one arm being the MEMS capacitance and the other a programmable capacitance capable of fine tuning its value in order to set a value as close as possible

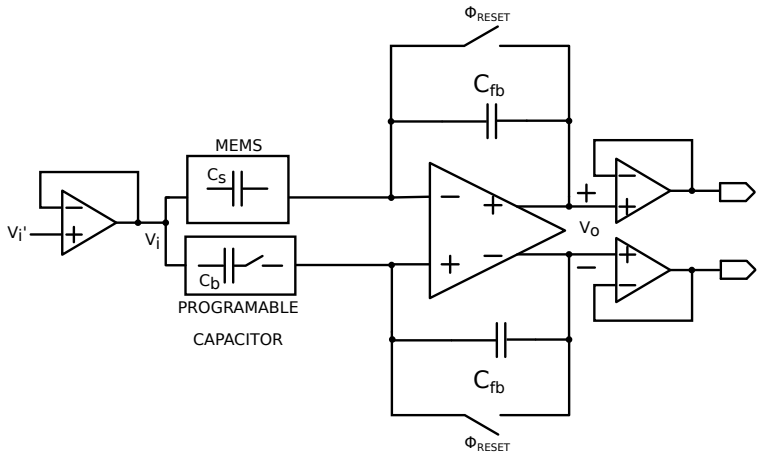


Figure 4.2.10: MEMS readout amplifier simplified schematic.

to the MEMS and minimize electrostatic signal feed-through. Next, a fully differential amplifier sets the input nodes common mode voltage and amplifies the signal. The LNA is fed back with capacitors in parallel with a switch intended for low duty cycling reset. Using capacitors instead of resistors greatly reduces area and power requirements.

During normal operation of the readout circuit, this is, when feedback switches are off, the LNA differential output V_o can be obtained. First, when the MEMS is subject to electrostatic force

$$v_o = v_i \frac{\Delta C_s}{C_{fb}} \tag{4.6}$$

where v_i is the electrostatic driving and C_{fb} is the feedback capacitance. $\Delta C_s = \Delta C_{driving} + \Delta C_{unbalance}$ is the bridge capacitance difference, that contains two sources of difference: capacitance variation due to the MEMS driving $\Delta C_{driving}$, and bridge unbalance $\Delta C_{unbalance}$. The first term is the MEMS capacitance variation due to 1) the Lorentz force, and 2) slight gap variations generated by electrostatic driving, both dependencies inside the denominator parenthesis of equation (1.7), derived in chapter 1.3.4.1. The $\Delta C_{unbalance} = C_s - C_b$ term is due to the difference between the MEMS capacitance C_0 and the programmable (or bridge) capacitance C_b. Such value should be as small as possible because it contributes to sensor offset. However, when driving the MEMS inside a closed loop, some amount of this offset is beneficial, as when sensed magnetic field is low, it avoids the loss of loop locking.

Without electrostatic driving, the LNA works as a charge sensitive amplifier that senses the MEMS output current

$$v_o = \frac{2 i_s}{2\pi f_r C_{fb}} \tag{4.7}$$

where f_r is the resonance frequency and i_s is the MEMS output current. The latter term has already been broken down in equation (1.8), and it is a function of the sensed magnetic field. In this case though, the electrostatic driving effect should be ignored as it is already in (4.6). The total final output voltage is then

$$v_o = \frac{2\epsilon_0 \epsilon_r A Q}{g^2 k C_{fb}} V \cdot I \cdot L \cdot B + \frac{v_i}{C_{fb}} \left(\frac{\epsilon_0 \epsilon_r A}{g} - \frac{\epsilon_0 \epsilon_0 A}{g + \frac{Q}{k}(ILB + V v_i \frac{C_s}{g})} \right) \tag{4.8}$$

where $\Delta C_{unbalance} = 0fF$ for simplicity. In the equation, ϵ_0 is the vacuum permittivity, ϵ_r is the relative permittivity of air, A is the MEMS capacitance equivalent area, Q is the quality factor, g the device gap, k is the spring coefficient, C_{fb} is the LNA feedback capacitance, V is the MEMS dc biasing voltage, I is the driving current at the resonance frequency, L is the device effective

length, B is the magnetic field, v_i is the electrostatic ac driving, and C_s is the MEMS equivalent capacitance.

As it can be seen in Fig. 4.2.10, LNA inputs are only connected to capacitors and, hence, they are high impedance nodes without a dc biasing. As a consequence, this node suffers from two types of variations. First, using a half bridge means that there exists a capacitive voltage divider consisting in the MEMS/bridge capacitance and parasitic capacitance at the LNA input nodes and feedback capacitances. As a consequence, these nodes tend to follow the electrostatic driving voltage as found in [110]. This effect also reduces MEMS voltage biasing, with the consequent reduction in sensitivity. Compared with [110], electrostatic driving in this work is much lower, making these problems unimportant. Second, leakage discharge these nodes capacitances and modify common mode voltage. In order to avoid that, periodical resetting these nodes voltage is required such as done in [110, 133]. This reset has been implemented with feedback switches that periodically short LNA input and outputs. As a consequence, LNA outputs, whose common mode is controlled by the CMFB amplifier, drive the inputs at the common mode, restoring the original voltage. Given that restoration is fast and leakage slow, only a low frequency, low duty cycle reset is needed.

Finally, two class AB opamps in buffer configuration drive the chip pads, providing a controlled capacitance at the output of the fully differential amplifier, simplifying its stability compensation design, and providing enough strength to drive large capacitive loads of chip pads, package pads, and PCB routing. Given that, at this stage, signal is modulated at the resonance frequency, opamp offset is not important.

In the following sections, the design of the presented sub blocks is described.

4.2.3.1 Programmable capacitor

Programmable capacitor was designed to deal with MEMS with a wide range of capacitances in case it was used with different devices in the future. For this reason, it was designed to provide up to 12.7 pF. Moreover, fine tuning is also important in order to be able to get rid of offset. For this reason, a minimum capacitance step of 1 fF was specified for a 14 bit programmability.

Its implementation has been done following the successful designs in [110, 137]. These consist in a fine-coarse capacitive DAC ladder implemented with a capacitor bank followed by a capacitive divider in parallel to a capacitor bank without divider. Doing so, fine tuning is achieved without the need of using a large amount of area to reach the maximum capacitance. The implemented simplified schematic is shown in Fig. 4.2.11. TSMC 0.18 μm process allows the use of Metal-Insulator-Metal (MIM) capacitors as small as 10 fF. However, in order to minimize process variations, 50 fF capacitor have been used instead. Fine tuning bank consists of a set of 7 binary weighted capacitors from 50 fF to 3.2 pF. This bank is followed by a capacitive network that divides the capacitance value. That allows a minimum step of 0.956 fF in post-layout typical corner simulation. Hence, fine tuning has a dynamic range of 122 fF. Coarse tuning bank consists in 7 binary weighted capacitors from 100 fF to 6.4 pF. Hence, programmable capacitor is non-monotonic but it has no missing codes. Maximum achievable capacitance is 12.7 pF. Programmable capacitance value is expressed as

$$C_b = \underbrace{\frac{\sum_{i=0}^{6} b_i C_i}{C_{A1} + \sum_{i=0}^{6} C_i} \left(\frac{C_{A2} C_{A4}}{C_{A2} + C_{A3}} \right)}_{\text{Fine tuning}} + \underbrace{\sum_{i=7}^{13} b_i C_i}_{\text{Coarse tuning}} \tag{4.9}$$

where b_i is a binary value indicating if a given capacitor C_i is connected to the input or GND, and C_{Ai} are the divider network capacitors.

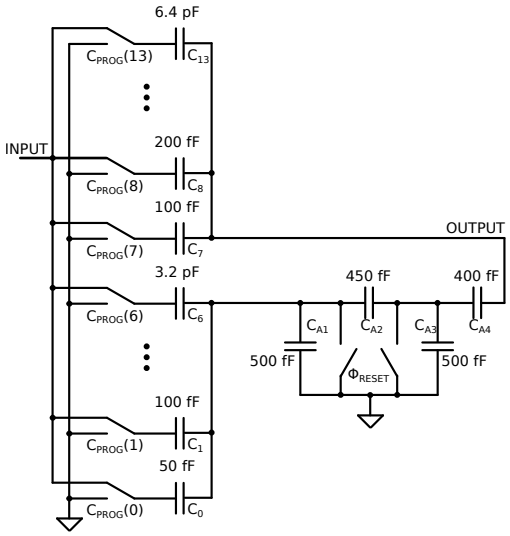


Figure 4.2.11: Programmable capacitor simplified schematic.

Table 4.3: Transistor dimensions of Fig. 4.2.12

Transistor	Type	Width (μm)	Length (μm)
M1	Native NMOS	96	1.2
M2	Native NMOS	96	1.2
M5	NMOS	360	3
M10	NMOS	288	3
M11	NMOS	288	3
M8	NMOS	72	3
M9	NMOS	72	3
M3	PMOS	343.2	0.8
M4	PMOS	343.2	0.8
M6	PMOS	52.8	0.8
M7	PMOS	52.8	0.8

4.2.3.2 LNA

The basic required specifications of the LNA are:

- Minimum open loop gain of 60 dB at 130 kHz to guarantee a good closed loop gain.
- Previous specification sets minimum Gain-Bandwidth product to 120 MHz.
- The amplifier must withstand an output capacitive load of $C_L = 800\ fF$ (input capacitance pad buffer) and provide a phase margin of at least 60°.
- Single ended output voltage swing of up to 1 V_{pp} to allow large offsets.
- Maximum input referred noise of 45 $nV/\sqrt{Hz}$ (obtained from device noise). However, this figure does not take into account the LNA input capacitance, that will further increase noise as detailed in (4.8).

The implemented LNA is a fully differential, single stage folded cascode operational transconductance amplifier (OTA). Its simplified schematic is shown in Fig. 4.2.12. Transistor dimensions are listed in table 4.3. This topology has been chosen as it provides large gains using a single stage.

Input pair transistors M_1 and M_2 tail current has been fixed to 100 μA. Taking into account that single pole approximation GBW is defined by [139]

$$GBW = \frac{g_{m1}}{2\pi C_L} \tag{4.10}$$

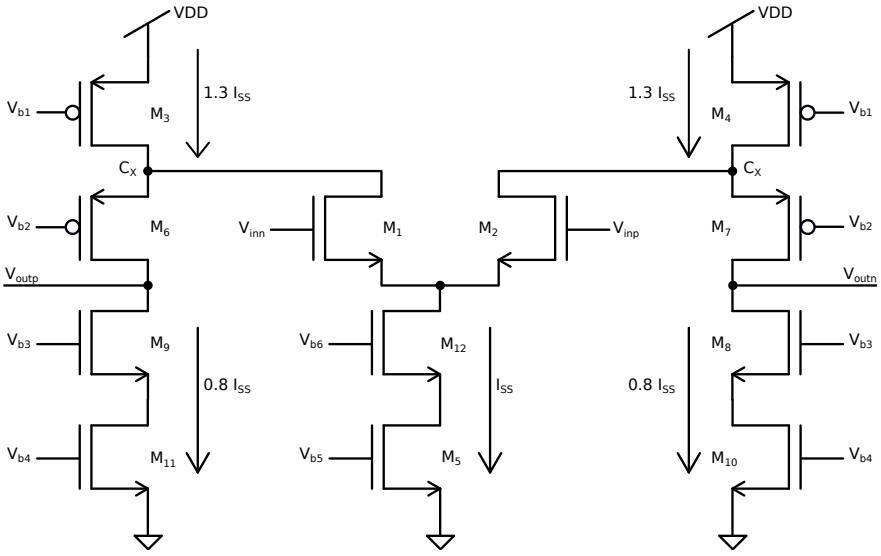


Figure 4.2.12: Simplified transistor level schematic of the implemented LNA. V_{b1} up to V_{b6} are current mirrors biasing voltages.

where g_{m1} is input transistor transconductance. As $C_L = 800\ fF$ is a given by buffering opamps input capacitance, sizing of input transistors have been done to meet GBW figure: $g_{m1} = 708.5\ \mu S$ (slightly larger to meet minimum gain for all corners), resulting in $GBW = 136\ MHz$.

Folded cascode branches have been designed taking into account that opamp gain A_v is

$$A_v = g_{m1} R_{OUT} \tag{4.11}$$

where R_{OUT} is the amplifier output impedance

$$R_{OUT} = ((r_{DS1} || r_{DS3}) r_{DS6} g_{m6}) || (r_{DS1} g_{m9} r_{DS9}) \tag{4.12}$$

where r_{DSi} are the transistor channel resistance and g_{mi} the transconductance. Before sizing transistors, though, biasing current at each branch has been fixed. The followed criteria is that if input pair tail current is completely sunk by one of the transistors (opamp saturation), some current must be left in the opposite folded branch to keep biasing. For this reason, input pair tail current is $I_{SS} = 100\ \mu A$, while $M_{3,4}$ drain, each one, $I_{3,4} = 1.3 I_{SS}$ and each folded branch sinks $0.8 I_{SS}$. Doing so, if all tail current I_{SS} flows through M_1, M_9 and M_{11} still have a $0.3 I_{SS}$ current that keep them biased. This current scheme has already been depicted in Fig. 4.2.12. Then, properly sizing M_6 adjusts its transconductance g_{m6} allowing the setting of opamp gain. Setting here a $g_{m6} = 540\ \mu S$ results in a dc gain of 74.8 dB and a $BW = 25.74\ kHz$ with a current consumption of 260 μA.

Sizing M_6 transistor with a large aspect ratio is also beneficial in terms of stability because it moves the non-dominant pole away

$$f_{p2} = \frac{g_{m6}}{2\pi C_X} \tag{4.13}$$

by increasing transconductance, where C_X is the capacitance at the folded branch to input transistor node, annotated in Fig. 4.2.12.

To achieve enough output dynamic range, all design current sources have been implemented with low voltage current mirrors. This topology, described in [139] has the benefit of having increased impedance, but it needs two current branches to bias the transistors, increasing the power consumption. A simplified schematic is shown in Fig. 4.2.13. If properly biased M_2 and M_4 are saturated, and minimum output voltage is the addition of both overdrive voltages $V_o = V_{OD2} + V_{OD4}$.

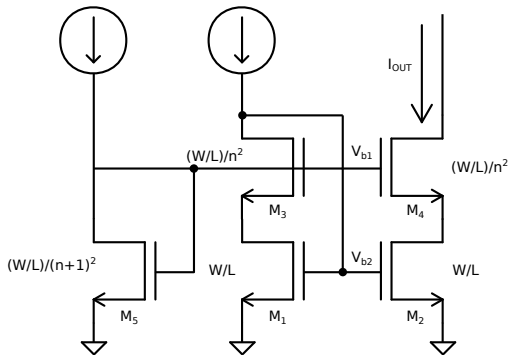


Figure 4.2.13: Simplified transistor level schematic the implemented NMOS low voltage current mirror. In this design, $n = 2$ has been used.

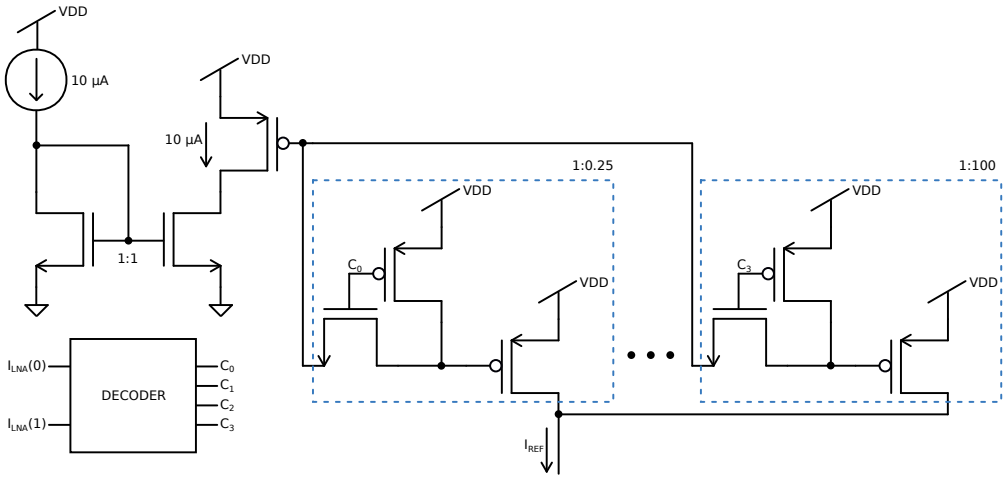


Figure 4.2.14: Simplified diagram of the LNA current reference selection.

Transistor sizing proposed in [139] has been used. It is intended to provide enough biasing voltages at each transistor gate.

In terms of noise, the main contributors are the input pair transistors M_1 and M_2, as well as transistors close to power rails M_3, M_4, M_{10}, M_{11} as described in [140]. M_1 and M_2 were implemented with native transistors because they have lower noise levels in this technology. Moreover, due to gain specifications, they already have a large aspect ratio, also beneficial in terms on noise (but increasing C_X and worsening phase margin). NMOS transistors M_{10}, M_{11} could be designed with lower aspect ratio but higher area because they do not worsen the non-dominant pole. On the contrary, M_3 and M_4 do. For this reason, they are the dominant noise sources. Final simulated LNA input referred noise is 9.55 $nV/\sqrt{Hz}$, a value obtained from the standalone LNA simulation. This noise value is lower than the specified, but gives some room to the LNA input capacitance to amplify noise as in (4.8).

During normal operation, the LNA is input two 10 μA current references from the bandgap. However, in the case that LNA noise needs to be reduced, an easy solution that does not require amplifier redesign is to increase its power consumption. This can be easily done by increasing the reference current. Hence, in case this noise figure is not enough, an extra block was designed to allow the LNA to work with higher currents. Its schematic is shown in Fig. 4.2.14. It consists in four current mirrors that allow to select the LNA reference current as shown in table 4.4.

Table 4.4: Current selection block output currents

A(1:0)	C(3:0)	Current (μA)
00	0001	2.5 μA
01	0010	10 μA
10	0100	50 μA
11	1000	100 μA

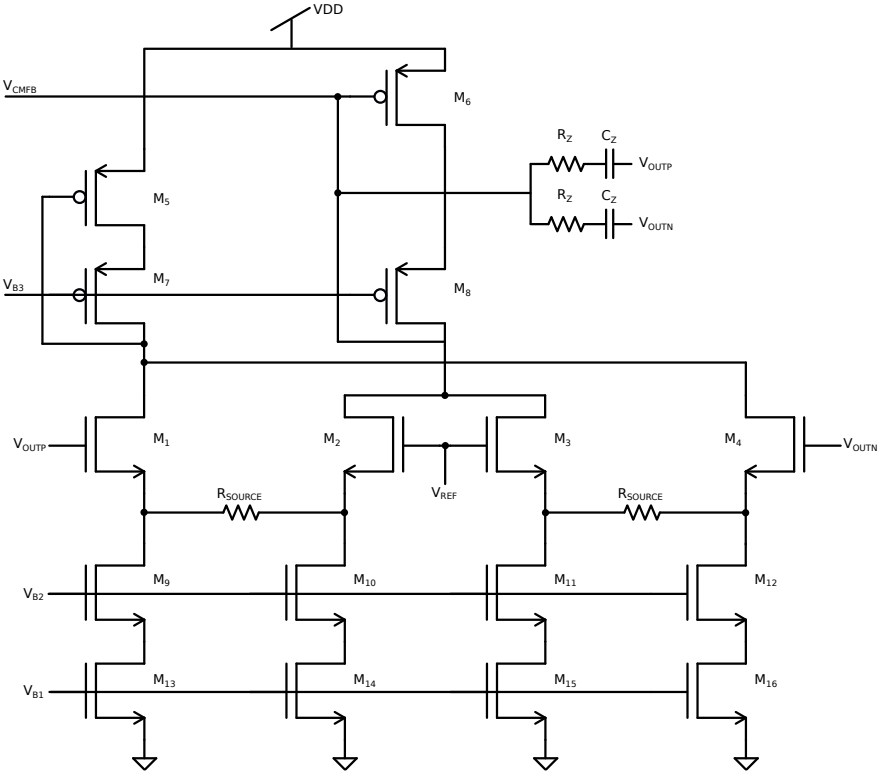


Figure 4.2.15: Simplified transistor level diagram of the LNA CMFB amplifier. V_{Bi} are the current mirrors biasing voltages, V_{OUTP} and V_{OUTN} are the amplifier outputs, V_{REF} is the common mode voltage reference and V_{CMFB} is CMFB output sent to the folded cascode PMOS current mirror.

Table 4.5: CMFB amplifier in Fig. 4.2.15 transistor dimensions

Transistor	Type	Width (μA)	Length (μA)
M_1, M_2, M_3, M_4	Native NMOS	8	1.2
M_5, M_6	PMOS	70.4	1
M_7, M_8	PMOS	17.6	1
M_9, M_{10}, M_{11}, M_{12}	NMOS	12	3
M_{13}, M_{14}, M_{15}, M_{16}	NMOS	48	3

4.2.3.2.1 LNA CMFB As any fully differential amplifier, a CMFB amplifier has been designed to control the output common mode at the externally controlled voltage value (mid-supply by default). In [137], both input and output CMFB amplifiers are implemented. While using an input CMFB would be beneficial in terms of avoiding the need of periodic LNA inputs reset, its implementation increases LNA input capacitance, and as a consequence, noise. For this reason only output common mode is controlled with a CMFB amplifier, while input common mode is low duty cycle, periodically reset. The CMFB amplifier designed is shown in Fig. 4.2.15. Transistors dimensions are shown in table 4.5.

The amplifier topology is the classical differential difference amplifier [141] with the particular

feature that each differential pair has source degeneration resistors. Moreover, the complete CMFB loop contains three poles: opamp dominant and non-dominant poles, and CMFB high impedance node pole. In order to improve CMFB loop stability, a nulling resistor compensation as in [142] has been implemented as shown in Fig. 4.2.15.

Finally, LNA output dynamic range is a quite demanding specification: differential 2 V_{pp}. Such range, makes typical CMFB amplifiers input pair current to drain only from one half of the pair. As a consequence, output signal saturates. Input range in which input pair transistors work normally, this is, when there is enough current in both halves of the input differential pair to keep transistor saturated (using long channel strong inversion model) is described as

$$\Delta V_{INmax} = \sqrt{\frac{2I_{SS}}{\mu_n C'_{OX}(W/L)}} \tag{4.14}$$

where I_{SS} is the input pair tail current, μ_n is the carrier mobility, C'_{OX} is the oxide capacitance per unit area and W, L are input pair width and length respectively. However, this equation changes when using source degeneration

$$\Delta V_{INmax} = \sqrt{\frac{2I_{SS}}{\mu_n C'_{OX}(W/L)}} + \frac{R_{SOURCE}I_{SS}}{2} \tag{4.15}$$

where R_{SOURCE} is the degeneration resistance. It can be seen that with degeneration, maximum range is proportional to both the tail current and the resistor value, while without degeneration is a function of the square root of current. This increase is due to the fact that excess input voltage drops across the resistor, leaving the transistor saturated during a larger voltage range. This technique has the advantage of allowing a linearity improvement by increasing the resistor while, at the same time, allowing the reduction of current. This trade-off has been thoroughly analysed during design in order achieve a low current CMFB amplifier that generates little distortion at the LNA output.

4.2.4 Auxiliary blocks

After the description of all the critical blocks of the MEMS readout circuit, it is important to mention a couple of blocks that also have an important task.

4.2.4.1 Bandgap reference and thermometer

A bandgap reference has been implemented with multiple objectives: 1) current reference generation for general blocks, 2) current reference generation for current driving block, and 3) temperature sensing. The implemented bandgap is shown in Fig. 4.2.16. The bandgap reference is a well-known block that has been thoroughly research in the last decades. And, even though plenty of solutions have been proposed to improve the reference stability over second-order temperature effects [143–150], only first-order temperature compensation is performed in the presented design. The output reference voltage expression is

$$V_O = V_{G0} + \frac{mk_BT}{q} ln\left(\frac{T_0}{T}\right) + \frac{k_BT}{q} ln\left(\frac{J_{D1}}{J_{D2}}\right) \tag{4.16}$$

where V_{G0} is the bandgap voltage at $T = 0\ K$, m is a temperature constant, k_B is the Boltzmann constant, q an electron charge, T_0 is the temperature the bandgap voltage has its maximum output, and T is the circuit temperature. Finally, J_{D1} and J_{D2} are diodes current density. This voltage has been used to generate the current source in 4.2.2.2 current reference: it is depicted in Fig. 4.2.16,

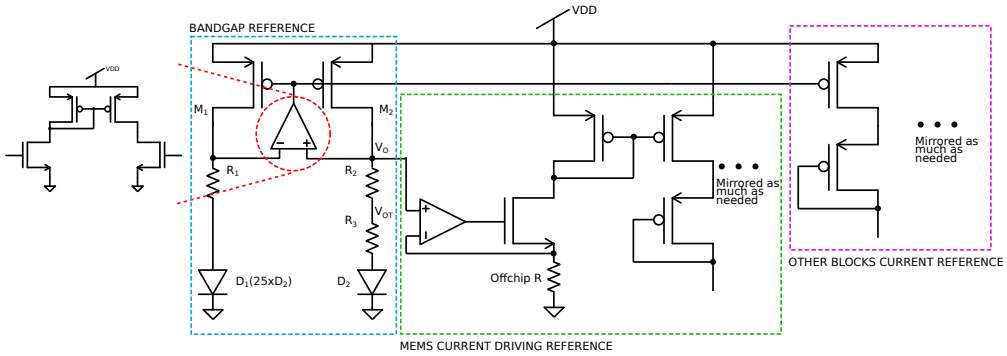


Figure 4.2.16: Simplified transistor level diagram of the bandgap reference. Bandgap reference is inside the blue box, current reference for current source block is inside green block, and rest of blocks current reference is inside pink box.

where an opamp and a transistor are used to make a voltage to current conversion using off-chip, very-low temperature coefficient resistors.

Next, node V_{OT} contains the temperature information. Considering V_O constant, a change in temperature changes diodes voltage difference ΔV_D proportionally following

$$\Delta V_D = \frac{k_B T}{q} ln\left(\frac{J_{D1}}{J_{D2}}\right) \tag{4.17}$$

This change is translated to V_{OT} as a voltage lowering with increasing temperature. This output has been buffered and sent to the a chip pad.

Finally, bandgap PMOS gate voltage has been used to generate the rest of the electronics current references. Doing so, voltage changes with temperature in a Complementary to Absolute Temperature (CTAT) manner, doing a first order compensation of temperature effects on the rest of blocks.

4.2.4.2 Register bank

Finally, a register bank has been used to digitally control the different block configurations available in the chip. The register bank is a 36 bit shift register (more than needed because this block has also been used in other designs of the research group) made of positive edge triggered, D flip flops with asynchronous enable and reset. The register is serially written using four pins COMM_{CLK}, COMM_{DIN}, COMM_{RST}, and COMM_{EN}. A COMM_{CLK} rising edge stores the data in COMM_{DIN} inside the first register as long as COMM_{EN} is high. At the same time, data at the output of first register is stored in the second one, and so on. After the registers are written, setting COMM_{EN} low enables the shadow register, making the written data to be deployed in the following COMM_{CLK} rising edge. Doing so, potential malfunction of the chip during register writing is avoided. A simplified schematic is shown in Fig. 4.2.17.

4.3 Simulation results

The blocks described in the previous sections were validated by simulations for different process corners, working temperatures and supply voltage variations. The layout of all the blocks was done and validated using DRC and LVS (Layout Versus Schematic) tool, as well as post-layout simulations. The chip was taped out and post-process was carried out at the department clean room, as measurements of Recollection devices in chapter 3 demonstrate. Unfortunately, measurements

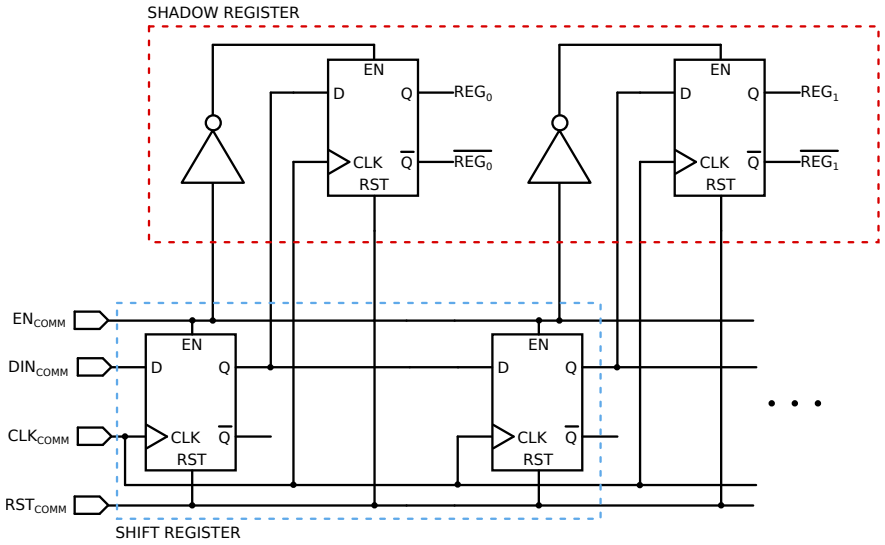


Figure 4.2.17: Simplified diagram of the implemented shift register. Only the first two 1 bit registers are shown.

of this chip were not carried out due to a lack of time. For this reason, in the following pages the designed chip is verified by means of the simulations performed with the Cadence Virtuoso design tools used.

4.3.1 MEMS driving

4.3.1.1 Electrostatic driving

Due to the robust design of this block (whose schematic is depicted in Fig. 4.2.4), input common mode and high and low driving voltages can easily be adjusted off-chip. Moreover, due to the use of a rail to rail class AB opamp buffer, the only driving limit is the voltage supply: as load is fully capacitive, opamp can reach the rails when driving the capacitive bridge. In Fig. 4.3.1 an example of a typical use case is shown: driving common mode at 0.65 V (that, with an LNA common mode at mid-supply (1.65 V) biases the MEMS with 1 V) with various amplitudes of electrostatic driving: 20 mV_{pp}, 200 mV_{pp}, and 400 mV_{pp}.

As it can be seen, enable = LOW and reset = HIGH have, in this block, the same consequence to output signal: setting it to the selected input common mode voltage. The difference is that reset is a global signal used to reset various nodes of the readout circuit to common-mode voltage, while the enable signal is unique for this block. This latter allows to disable electrostatic driving while the rest of the readout circuit is working and resetting as usual.

4.3.1.2 Current driving

First, common mode feedback amplifier implemented with this block (in Fig. 4.2.5) does not have rail-to-rail input, but a single NMOS differential pair. As a consequence, common mode reference voltage has, as a lower limit, the voltage at which the CMFB amplifier input transistors leave saturation region (this includes both dc and ac output signals). The upper limit is set by the current amplitude injected to the device, that may require setting voltages higher than voltage supply, thus generating nonlinear output around a deviated common mode. Hence, both limits will be more stringent for higher currents and higher resistive loads. In Fig. 4.3.2 an example of such behaviour is shown for a load of 1.6 $k\Omega$ (around mid-range of both wire resistance values) that

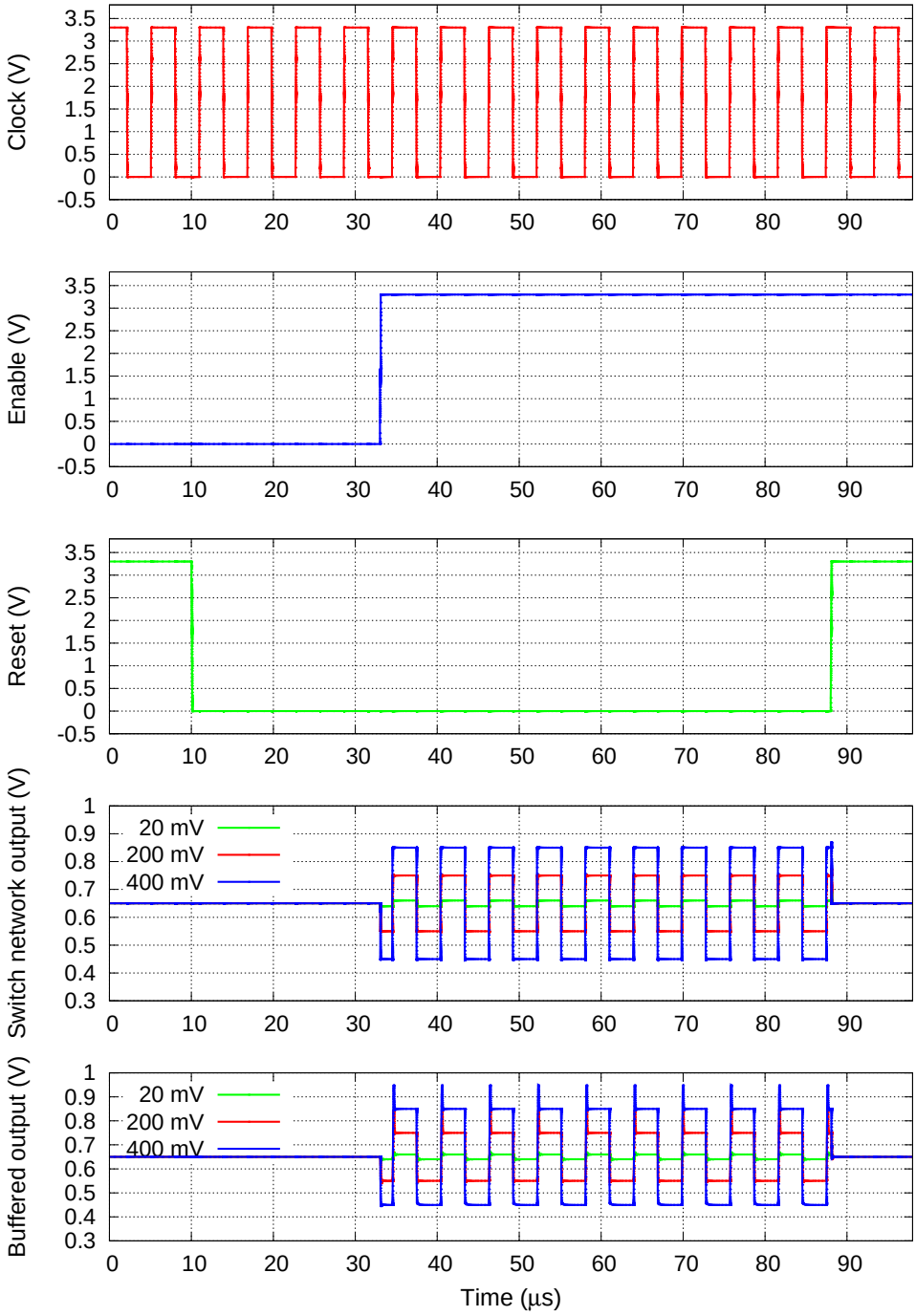


Figure 4.3.1: Simulation of the electrostatic driving plot. The shown signals are, from top to bottom: clock, block enable, reset, switch network output, and switched network output after opamp buffering. Simulation has been performed with the buffer loaded with a capacitive load of 20 pF.

shows how the common mode estimation degrades for lower and higher values, and that it worsens for higher currents.

On the other hand, current driving amplitude works perfectly within a wide range of load resistances if common mode is kept at mid supply (this is, 1.65 V). In Fig. 4.3.3 all current drivings are shown for a resistive load of 1.6 $k\Omega$ and 1.65 V common mode. However, simulations confirm a precise current driving with loads as high as 3 $k\Omega$ (where the limiting factor is voltage supply), and as low as 300 $m\Omega$ when common mode is set to mid-supply. This means that resistive load dynamic range is of 4 orders of magnitude.

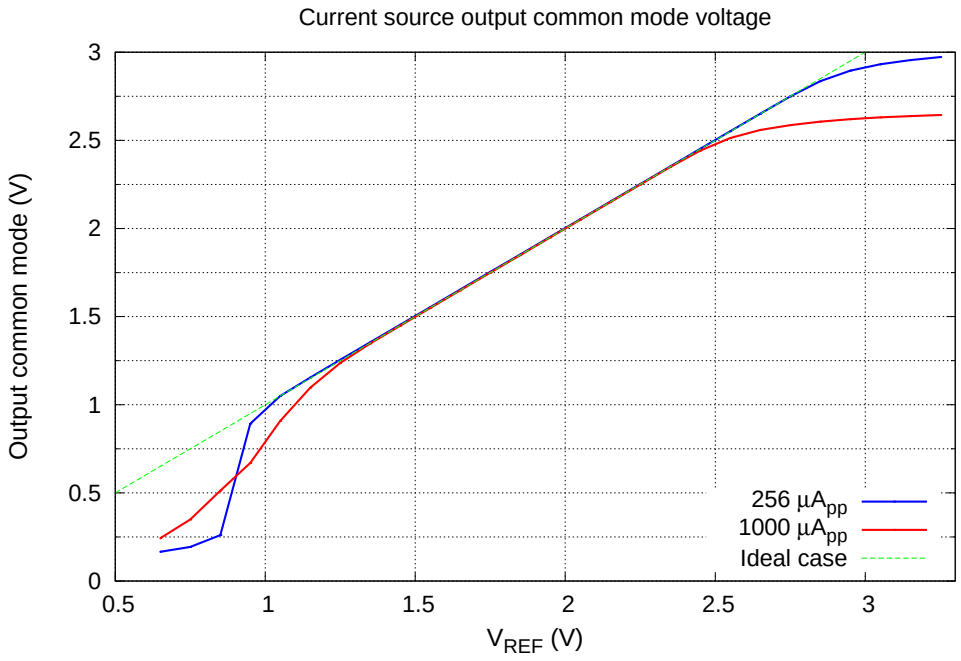


Figure 4.3.2: Simulated current source output common mode voltage for 256 mA_{pp} and 1000 mA_{pp} output currents on a 1.6 $k\Omega$ load.

The advantages of the proposed current driving circuit are numerous. First, when MEMS common mode is not important, such as Medusa and Quadspring (because their biasing is set by electrostatic driving block), driven resistance can be quite high, meaning that plenty of current re-circulations may be implemented, increasing wire resistance (but also sensitivity) and still being able to drive with a mid-supply common mode. Second, in Octospring, where common mode is controlled by this block, common mode can be adjusted to different values because of its low resistance. Hence, a wide variety of MEMS typologies can be driven with this block.

Moreover, in Fig. 4.3.3, normal enable current spike previously mentioned can be seen around 18 μs. In addition, the current takes a stabilization time of around half clock period. For this reason, the zero current enable signal was required, which is shown to work as expected around 158 μs.

4.3.2 LNA

4.3.2.1 Gain and stability

The LNA (in Fig. 4.2.12) gain at the device working frequencies must be, at least, around 60 *dB* in order to provide a good gain accuracy. However, the LNA reference current selection is also a source of specification worsening not taken into account during initial design. For this reason, some of these specifications are not met, but they are very close.

Fig. 4.3.4 shows the LNA open loop gain and phase for a standard current reference of $10\mu A$. As it can be seen, gain is 58.3 *dB* at 130 *kHz* and 56.2 *dB* at 170 *kHz*, lower than specified but still very close. Obviously, current reference changes affect the gain, that reaches a minimum of 46.7 *dB* when LNA current consumption is divided by 4. In any case, phase margin is higher than 61°. In Fig. 4.3.4 open loop gain and phase is shown for a standard current reference of 10 μA.

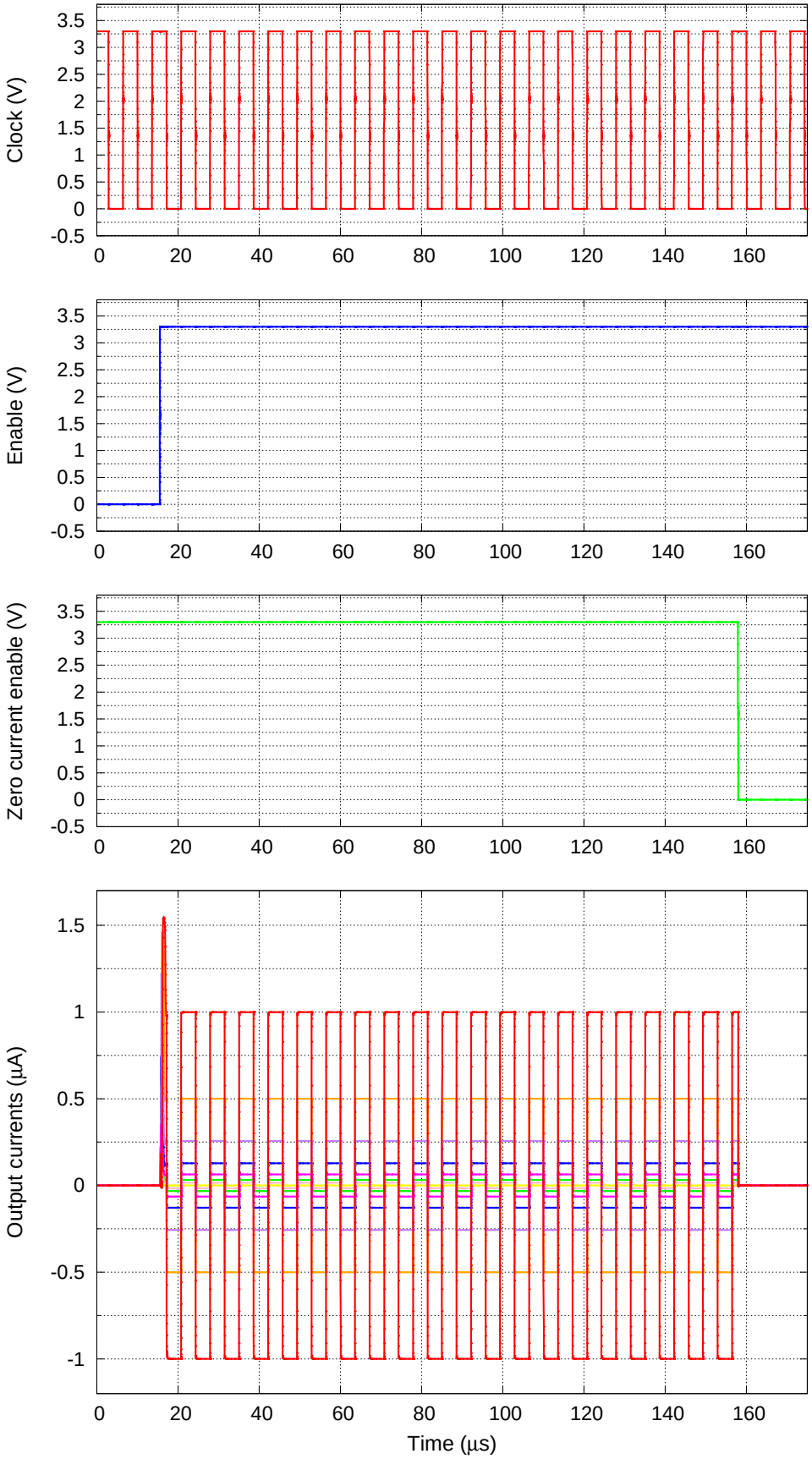


Figure 4.3.3: Simulated current source for a 1.6 $k\Omega$ resistive load. All current values have been plotted.

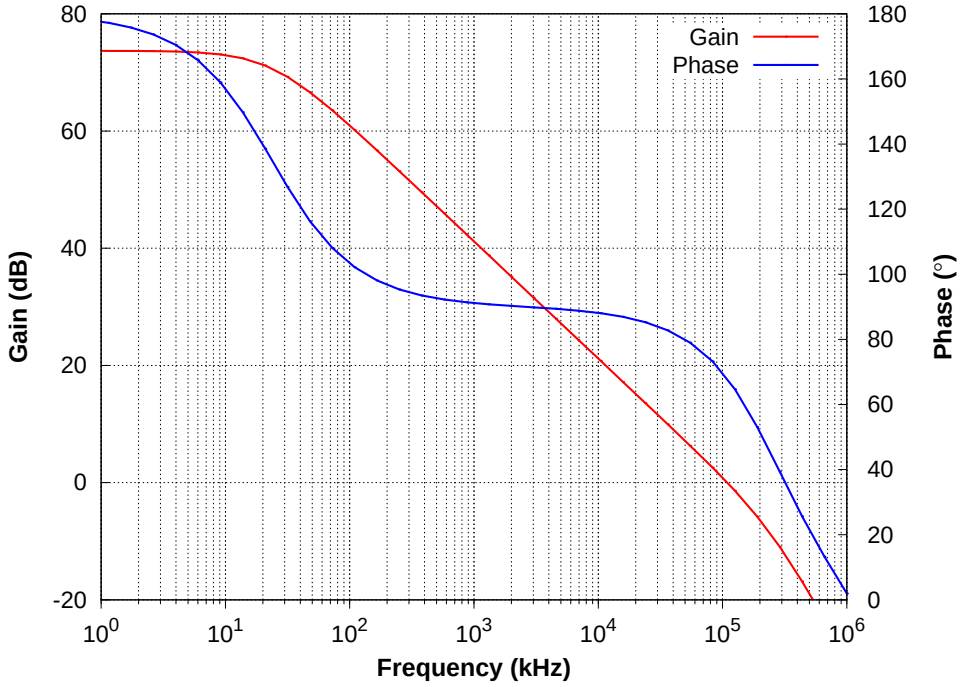


Figure 4.3.4: Simulated Bode plot of the LNA with a current reference of 10 μA.

Table 4.6: LNA simulation results summary

Reference current (μA)	$G_{130\ kHz}$ (dB)	$G_{170\ kHz}$ (dB)	Phase margin (°)	GBW (MHz)
2.5	48.5	46.7	73.0	35.3
10	58.3	56.2	68.0	110.8
50	66.1	64.5	62.7	293.7
100	67.3	66.2	61.0	417.9

A summary of the main LNA specifications for all possible reference currents is depicted in table 4.6.

4.3.2.2 Noise

Thanks to the high gain provided by the folded cascode topology, it has been possible to design a fully differential amplifier with a noise that is much lower than expected. However, noise is considered for all LNA current consumption modes. In Fig. 4.3.5 the LNA input referred noise is shown for a wide frequency range for all currents. It can be seen that some second order effect makes flicker noise to increase proportionally to amplifier current. However, the interesting values are found at the devices working frequencies, that have been included in table 4.7. White noise has also been included in the table to show that remnant flicker noise is not important for 2.5 and 5 μA currents, but its importance increases as current does, as observed in Fig. 4.3.5.

4.3.2.3 CMFB Amplifier

Total Harmonic Distortion (THD) has been chosen as a figure of merit for the evaluation of the CMFB amplifier. In order to check the evidence in eq. (4.15), Fig. 4.3.6 shows the CMFB amplifier THD when tail current and degeneration resistance are swept for a differential output voltage of 2 V_{pp}. It can be seen that, as expected, increasing the tail current marginally improves the linearity,

Table 4.7: LNA input referred simulated noise

Reference current (μA)	@ 130 kHz (nV/$\sqrt{\text{Hz}}$)	@ 170 kHz (nV/$\sqrt{\text{Hz}}$)	White (nV/$\sqrt{\text{Hz}}$)
2.5	15.2	15.1	14.6
10	9.5	9.3	8.4
50	7.74	7.3	5.4
100	7.79	7.2	4.5

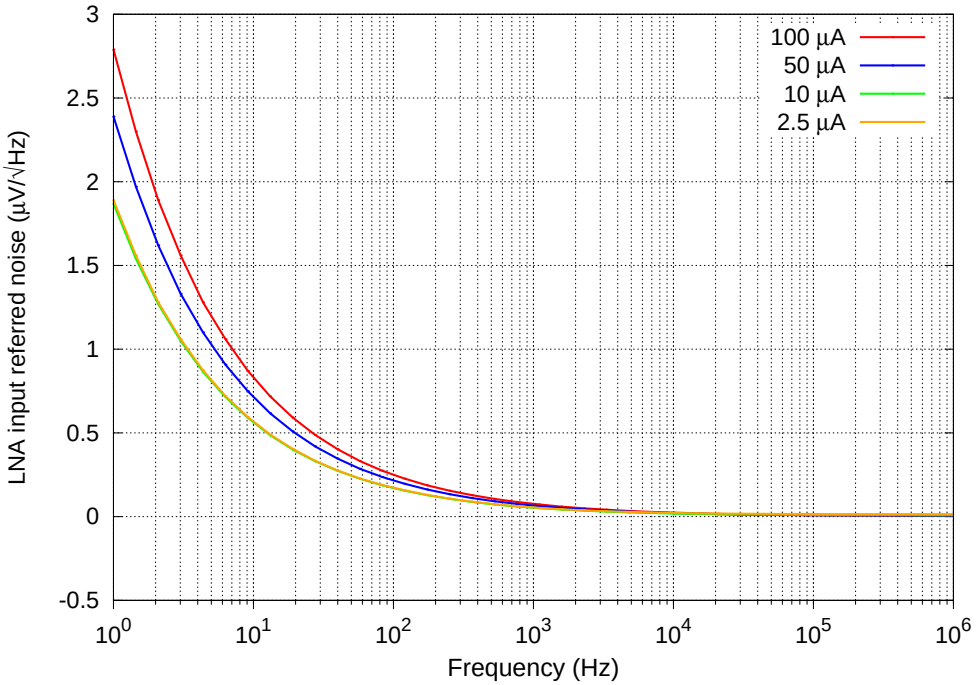


Figure 4.3.5: LNA input referred noise spectrum for all current references.

while source degeneration resistance has a stronger effect. Moreover, for each curve, there exists a combination of current and resistance that provides a minimum THD. This is explained because increasing the resistance allows larger drops between the input pair transistor sources, improving linearity. However, if degeneration is very large, the differential pair starts acting as a voltage follower, removing any achieved improvement. This is a consequence of gain reduction due to degeneration.

As a example of the improvement provided by this technique, in a first attempt, the CMFB amplifier linearization was performed by increasing tail current without including source degeneration. The best THD achieved was 0.217% with a tail current of 853 μA. The equivalent Spurious Free Dynamic Range was $SFDR = 53.7\ dB$. Fig. 4.3.7 shows the THD and SFDR improvement during the current sweep, while Fig. 4.3.8 (a) shows the obtained SFDR.

On the other hand, when using a degeneration of $R_S = 48\ k\Omega$ and a current of 53 μA, a THD one order of magnitude lower was obtained ($THD = 0.026\%$) and a $SFDR = 76.7\ dB$. Again, Fig. 4.3.7 shows the THD and SFDR improvements during the current and R_S sweep, while Fig. 4.3.8 (b) shows the obtained SFDR. As a drawback, though, CMFB amplifier gain is only 42 dB at 130 kHz, a value that is quite low and generates some offset at the output common mode (around 50 mV). However, this is not a critical problem.

These results have been compared with similar works in the literature in table 4.8, and as it can be seen, both current consumption and linearity are remarkably better.

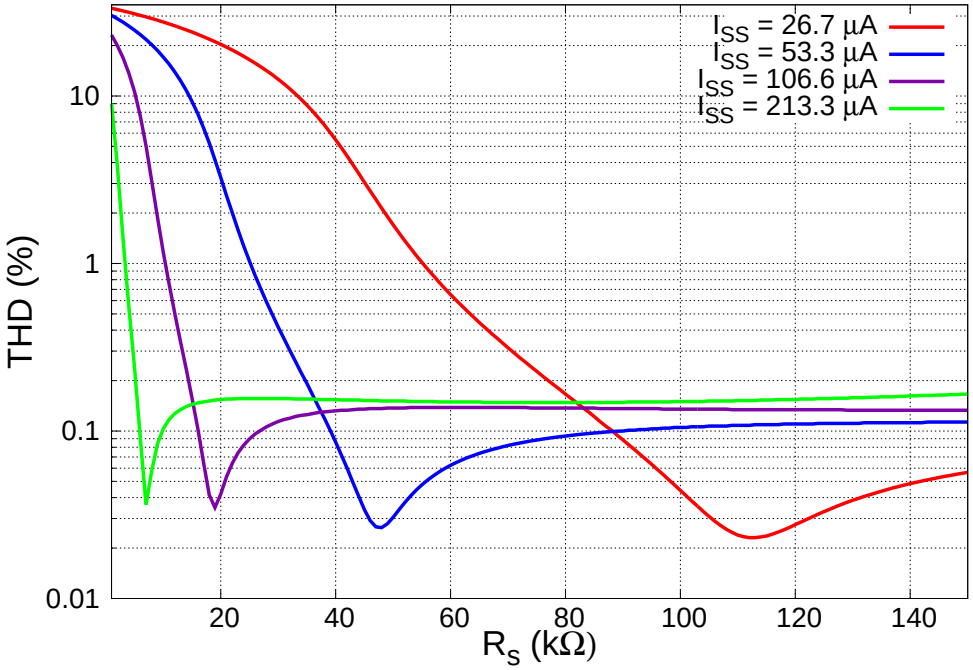


Figure 4.3.6: Output common mode THD for an output voltage of 2 V_{pp} while performing a sweep of both tail current and degeneration resistance.

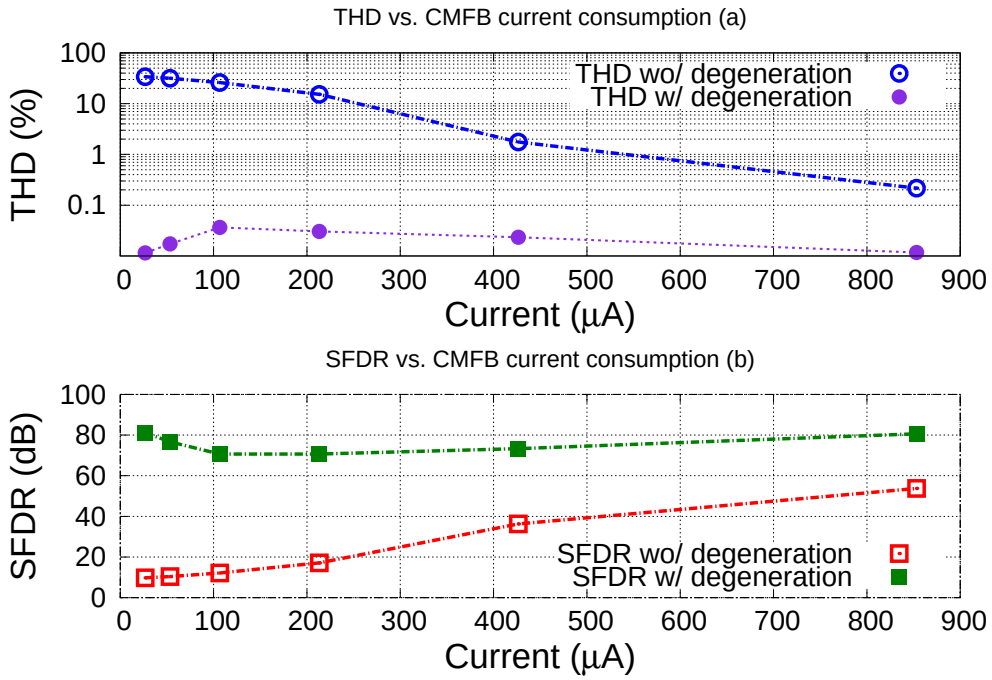


Figure 4.3.7: Output common mode THD and SFDR values when performing a tail current sweep (without degeneration), and best degeneration resistance for the given current.

4.3.2.4 Programmable capacitance

A standalone simulation of the programmable capacitor is shown in Fig. 4.3.9. To perform this simulation, a test bench where both input and output of the capacitor bank are connected to ideal dc voltage sources that fix these nodes voltages. When implemented in the readout circuit, though,

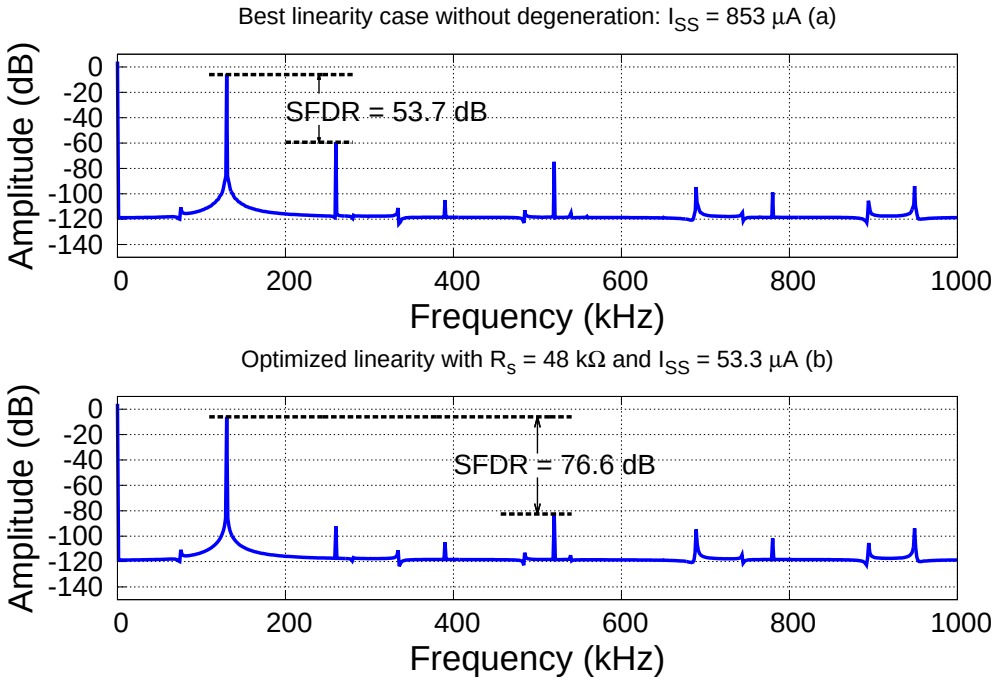


Figure 4.3.8: Best SFDR value found in each case shown in a plot of the output signal spectrum.

Table 4.8: Linearity comparison with the literature

Work	I_{SS} (μA)	SFDR (dB)	THD (%)
Carrillo et al. [151]	155	-	0.01
Zhang et al. [152]	200	43.86	-
Lin et al. [153]	-	-	0.22
This CMFB	53.3	76.7	0.026

output node is connected to LNA input, which is not an ideal dc voltage. As a consequence, this node capacitance, works as a further dividing stage, which makes the fine tuning steps much smaller: 0.018 *fF* in front of the designed 1 *fF* steps. This issue was found during PCB debugging. As a consequence, effective minimum capacitance step is 100 *fF* (coarse tuning bank resolution), which will result as increased electrostatic driving generated offset due malfunctioning of the fine tuning part of the programmable capacitance.

In order to avoid this same issue in future designs, during the design of divider stage, capacitance at the output of the programmable capacitor must be taken into account. This capacitance is easy to know because it mainly depends on the LNA input and feedback capacitance.

4.3.2.5 Readout circuit

Finally, once the blocks that make up the entire readout circuit have been simulated and validated, the last step is to check whether the top level circuit works as expected. For such purpose, these simulations have been divided into three parts: electrostatic driving signal amplification, MEMS output current signal, and total output noise.

4.3.2.5.1 Electrostatic signal amplification Electrostatic driving will be used in order to keep a relatively high output signal at the resonance frequency in order to ease loop locking when magnetic field signal is low. One of the main concerns of this signal is that, due to its relatively

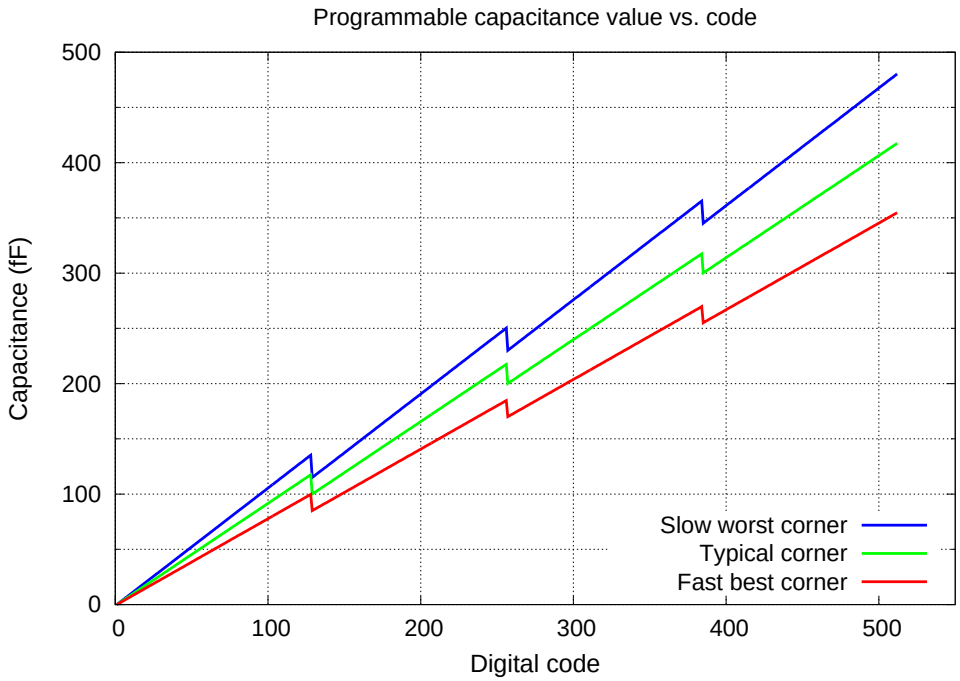


Figure 4.3.9: Simulated programmable capacitance value for the following corners: typical, slow worst, and fast best. Periodic downward jumps are due to the transition between the maximum fine and coarse tune banks. Only the first 512 codes are shown.

high value at the input half bridge, it may cause LNA input common mode to change. This fact was observed in [110] and, to solve the problem, a full bridge was used. Nevertheless, accelerometer driving in such work is around 2 V, while here it is of some tens or hundreds of millivolts. In Fig. 4.3.10 the simulation of the complete readout system is shown when a 1.4 pF sensor is used and it is driven with a voltage of 20 mV_{pp}. As it can be seen, low duty cycle reset works correctly as, when active it disables the electrostatic driving and resets the nodes at the input and output of the LNA. Doing so, the slow drift observed at the LNA output is reset and common mode is preserved. This drift is equally observed at the LNA input, this is thought to be caused by current leakages that move these voltages at a rate of 0.16 $\mu V/\mu s$ (upwards at LNA positive input, and downwards at the negative input). The voltage drift is so low it does not importantly affect the sensor dc biasing and could allow more time between reset times. Both input (in the picture) and output common mode voltages are stable.

A more detailed view is shown in Fig. 4.3.11, where details of the signals moving at the resonance frequency can be seen. Two deviations from the ideal case can be observed. First, reset dc value of common mode voltage in LNA input is around 1.6 V. This offset is due to the relatively low gain of the CMFB amplifier. However, as far as it is a known value it is not a problem, as input common mode can be adjusted in order to make the MEMS to have the proper dc biasing. Second, LNA input common mode, as expected, tries to follow the input driving signal. Common mode variation is less than 20 mV, which means a MEMS biasing error of less than 2%. This error, though, is low enough to not being important. Moreover, in the case where electrostatic driving is not used this MEMS gain error would disappear.

4.3.2.5.2 MEMS output current signal amplification To test how the readout amplifier would amplify the MEMS output current signal, in the following simulations the MEMS has been replaced by an ideal current source providing a current of 20 pA_{pp}. This current value is in the lower order of magnitude of currents that the MEMS can provide. The simulation is shown in Fig.

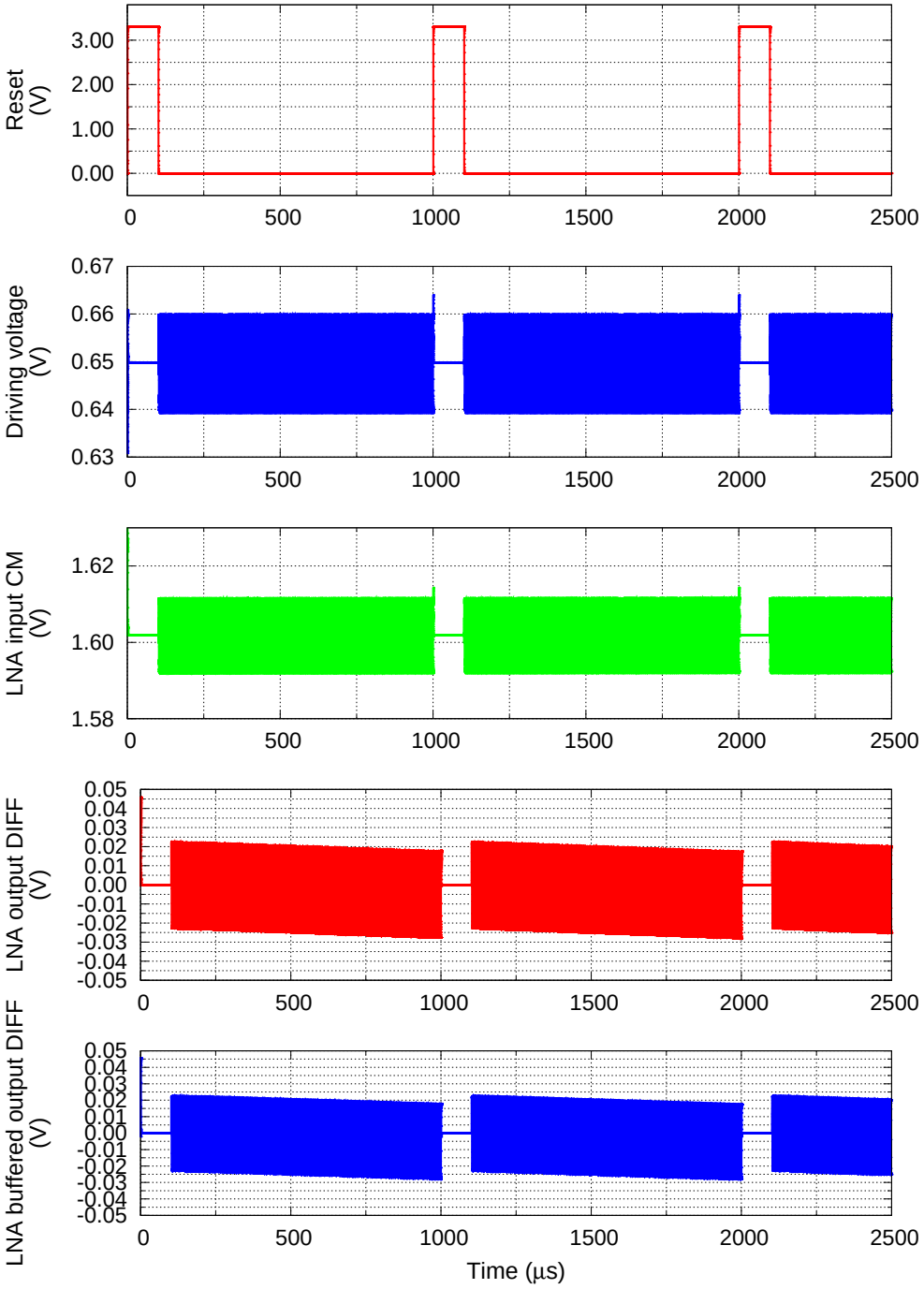


Figure 4.3.10: Simulated readout circuit with electrostatic driving. From top to bottom signals are: system reset, driving voltage at the output of electrostatic driving block, LNA input common mode voltage, LNA output differential voltage, and LNA buffered output signal.

4.3.12. It can be seen that the current leakage at the LNA input is not important enough to drain all MEMS current. As a consequence, amplifier transimpedance is, as expected, the LNA feedback capacitance impedance. Note that the LNA input common mode is now constant, providing a constant MEMS sensitivity. However, LNA input signals suffer a larger drift of around 5.7 $\mu V/\mu s$. This drift difference is though to be caused by the feedback network: when LNA inputs deviate from the common mode due to electrostatic driving, there exists some current that flows from the LNA outputs to the inputs through the off switches that partly compensates the drift.

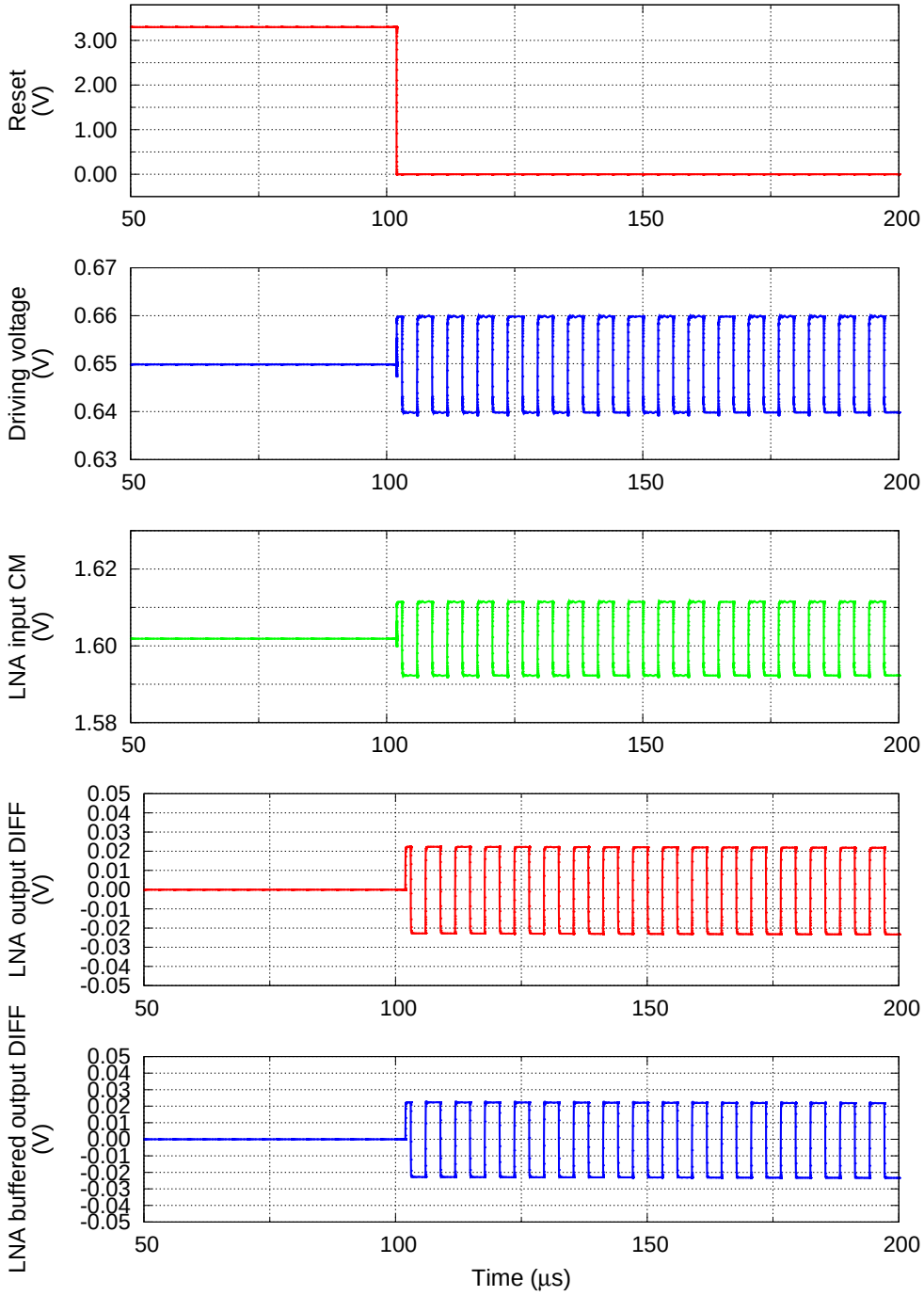


Figure 4.3.11: Simulated readout circuit with electrostatic driving: detailed view.

4.3.2.5.3 Total output noise Finally, noise has also been simulated and shown in Fig. 4.3.13. Two noise simulations have been performed. First, one with the Octospring drive to sense capacitance of 869 fF measured in the previous chapter, and a parasitic capacitance at the sense node of 500 fF, a value obtained in the post-layout simulation of the device. The second simulation of noise uses the TSMC version of device in chapter 2, with a capacitance of 1.4 pF and a parasitic of 1.2 pF.

As it can be seen, noise for Octospring device is 484.0 $nV/\sqrt{Hz}$, lower than the other device noise (840.4 $nV/sqrtHz$) as it presents a lower capacitance at the input nodes of the LNA. This effect has been previously predicted in the equation (4.4) at the beginning of this chapter. To compare

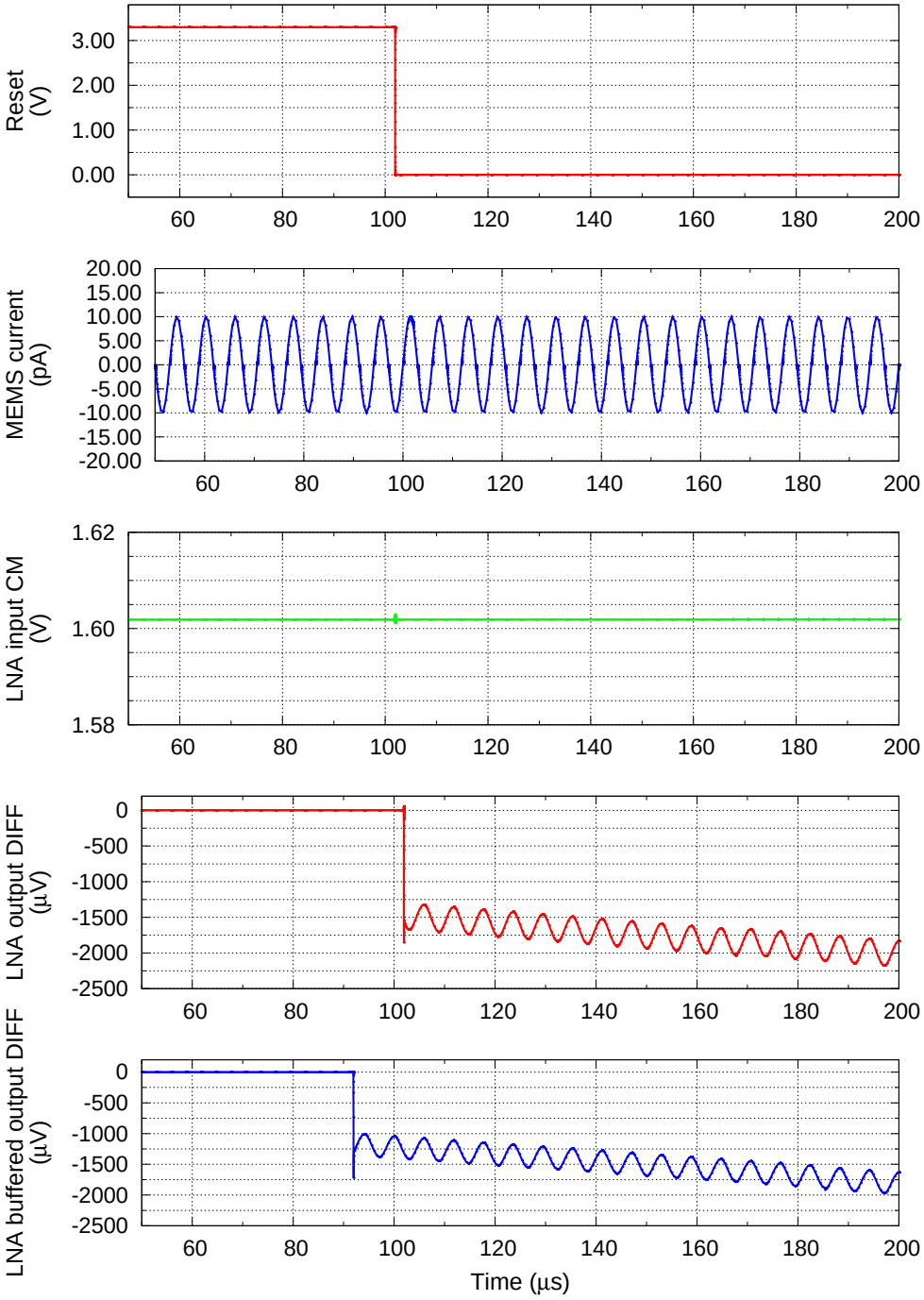


Figure 4.3.12: Simulated readout circuit with MEMS current: detailed view.

LNA output referred noise with MEMS Brownian noise, it is necessary to translate MEMS output current equivalent noise to the LNA output using

$$\overline{v_{oMEMS}} = \overline{i_s} \cdot \frac{1}{2\pi f_r C_{fb}} \tag{4.18}$$

where $\overline{i_s}$ is the MEMS noise in current units, and the fraction is the feedback capacitance C_{fb} impedance. Using the Octospring noise in table 4.1, LNA output referred MEMS noise is 95.8 $nV/\sqrt{Hz}$, much lower than LNA noise and, thus, making the LNA noise dominant. Hence, in terms of mag-

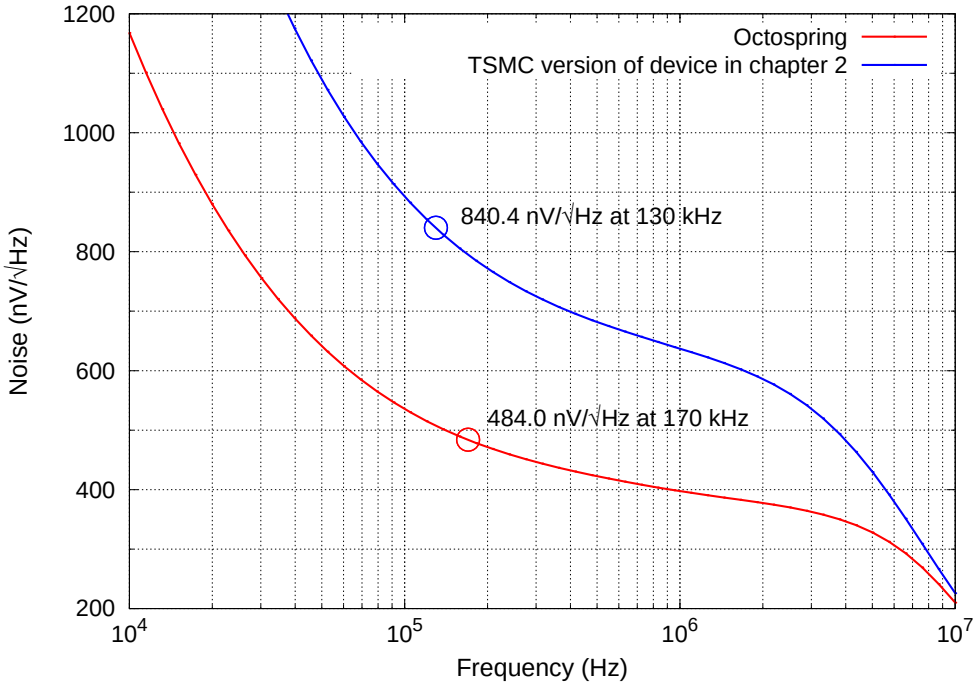


Figure 4.3.13: Simulated readout noise for two different devices: 1) Octospring device (red), and 2) TSMC version of device in chapter 2 designed by Mr. Juan Valle.

netic field, the LNA noise for this device is

$$\overline{B_{MEMS}} = \frac{\overline{v_o}}{S\frac{1}{2\pi f_r C_{fb}}} = 2.60\frac{\mu T}{\sqrt{Hz}\cdot mA} \tag{4.19}$$

were $\overline{v_o} = \sqrt{\overline{v_{o\ LNA}}^2 + \overline{v_{o\ MEMS}}^2}$ is the output referred total noise. This noise limits sensor resolution to 8.23 $\mu T/mA$ for a bandwidth of 10 Hz and $V = 1\ V$. Comparing this value with the Android 9 requirements in table 1.1 of chapter 1, it can be seen that Octospring device noise and resolution is a bit high, requiring a current consumption of around 13 mA to meet the resolution requirements to be introduced into an Android phone (although failing consumption specification).

On the other hand, LNA output referred MEMS noise for modified version of device in chapter 2 is 942.7 $nV/\sqrt{Hz}$, while output referred LNA noise is 840.4 $nV/\sqrt{Hz}$, two very similar values that end up being an equivalent output referred noise of 1.26 $\mu V/\sqrt{Hz}$, and an equivalent magnetic field noise of 3.57 $nT/\sqrt{Hz}\cdot mA$, allowing a magnetic field resolution of 0.6 μT with a current consumption as low as 6 μA. These figures must be handled with care as they are only theoretical. Real measurement would, for sure, show much higher voltages due to further layout parasitics.

4.4 Conclusions

In this chapter, the readout circuit for the Octospring and variation of device in chapter 2 devices has been proposed and described. The proposed circuit includes both the MEMS current and electrostatic driving, as well as the signal amplification. Even though it still needs external circuitry and signal processing (that can be implemented digitally with an FPGA, as demonstrated in chapter 2), the integrated circuit includes the most critical and specification demanding blocks. Plus, the remaining off-chip circuitry is easy to integrate. The circuit has been designed and manufactured using the TSMC 180 nm technology, and includes the Octospring device in the same

die area without the need of extra manufacturing steps excepting oxide etching. An imatge of the manufactured die is shown in Fig. 3.4.8 of chapter 3.

The readout circuit, has been designed taking into account the TSMC version of device in chapter 2, which has very demanding noise figure. However, Octospring measurements in chapter 3 and simulations show that the circuit also proves to be useful for implementing the readout of the Octospring device with some specification limitations. This is due to the fact that Octospring device has a much lower sensitivity. Combining circuit simulations with device parameters estimated from measurements, it has been possible to see that the proposed CMOS-MEMS Octospring sensor provides a total noise of around 2.6 $\mu T/\sqrt{Hz}$ if a biasing current of 1 mA is injected into the MEMS and a biasing voltage of 1 V is used. Moreover, with the mentioned current biasing, a resolution of around 8.23 μT can be achieved for a bandwidth of 10 Hz. These figures are worse than those required by Android 9 specifications, meaning that device needs further improvement to be introduced into a smartphone.

Unfortunately, due to a lack of time, it has not been possible to measure the proposed the sensor described in this chapter. This is the reason that simulations have been presented instead of measurement results. However, the chip has already been manufactured, so measurements are expected to be performed in the near future.

An interesting future work would be the design of the full CMOS-MEMS system in the same chip. That would mainly include, the proof-of-concept circuit described in this chapter, an ADC to translate data to the digital domain, a simple DAC for electrostatic driving control, and the digital circuitry (for example, the implemented in the FPGA in chapter 2).

Final conclusions

In this dissertation, MEMS magnetometers limitations to take into account prior to its commercialization have been identified, analysed, and addressed. To do so, in the introductory chapter the state of the art has been analysed in order to identify the limitations of current MEMS magnetometers and the research trends. From this analysis, some bottleneck are identified:

- Devices with good sensitivities are reported in the literature. However, high currents and high biasing voltages are used for such purpose. Doing so, sensor consumption is still too high to compete with magnetometers currently used in mass production, as well as high biasing voltages that complicate the design of the electronics.
- There is still a lack of research in complete readout circuits, including the loop control and digital signal processing. Instead, bulky instruments are used to do proof of concept test of novel devices or new modulations.
- Most works require custom processes to design the MEMS devices, making their production expensive and have important parasitics.

Hence, in the following chapters of the dissertation, potential solutions to these limitations have been implemented and put under test.

Chapter 2 covers the lack of complete readout architectures in the literature. For this reason, a complete readout system has been proposed and implemented with off-the-shelf components on a printed circuit board. At the same time, a digital circuit is proposed to implement the loop control and further signal processing by means of VHDL code in a FPGA. All the proposed electronics have been designed with their integration in a SoC in mind. Moreover, an offset reduction strategy has been proposed in order to minimize the offset of amplitude modulated MEMS magnetometers. In the proof of concept system, an offset reduction of 40.1% has been obtained by selectively turning the electrostatic driving on and off, increasing the output dynamic range. Moreover, a total noise of 550 $nT/\sqrt{Hz}$ has been achieved, a quite good value taking into account the typically large parasitics at the MEMS-amplifier interface of PCB implemented readout circuits.

In chapter 3, various MEMS magnetometers have been proposed, manufactured, and measured. The devices have been designed using the BEOL part of a standard CMOS process, allowing the fabrication of the MEMS in the same die area of the electronics without extra post-processing but the mechanical structure release. Of the various devices, theirs pros and cons have been analysed, as well as their high volume manufacturing viability, performance after both wet and vapor etching of the structures, and potential improvements.

Finally, in chapter 4 an integrated solution of the most critical blocks for the readout of CMOS-MEMS magnetometers is proposed. This solution has been designed and manufactured using the standard TSMC 180 nm process, where both the proposed MEMS and electronic circuitry share the same chip area. The designed electronics has been designed with the specifications of a variation of device in chapter 2, but noise performance has also been analysed for its use with the Recollection device: device referred noise is dominated by the LNA, and is 2.60 $\mu T/\sqrt{Hz}$ with a biasing of 1 mA and 1 V.

However, this work leaves some open doors for pending future works. First, it would be interesting to further improve the Medusa device, as it is the most promising one in terms of yield, as well as it offers to possibility of recirculating the biasing current due to the nature of their springs. Moreover, MEMS design does not finish at the design of the resonator itself, but it would be interesting to further work on the vacuum sealing and packaging, and see how these processes affect device yield. Second, the electronic circuit included in the Recollection chip in chapter 4 could not be tested due to a lack of time. Hence, measuring the chip and comparing its performance against the simulated figures should be in the top of the future work list. Moreover, this chip only includes the most critical blocks for the MEMS readout. Hence, the next task would be to keep integrating the electronics in chapter 2 until everything that is needed is on-chip.

Appendix A: MEMS parameters extraction Python code

In this appendix, the Python code used to extract the MEMS RLC model is shown and explained. Given that the complete code is quite long and contains all the necessary instructions to batch analyse all reticles data, only the essential part of the code to perform the conductance data fitting and parameters extraction is included.

To do the data fitting, the *Model* function inside library *lmfit* is used. Hence, it is necessary to import it with

```
from lmfit import Model
```

Next, the conductance model in eq. 3.3 must be defined in order to tell the function which is the mathematical expression the function has to fit the data to. In order to simplify the code, it has been implemented with a function:

```
def conductance(omega, R, L, C):
        return R/(R**2 +((omega*L)-(1/(omega*C)))**2)
```

Then, the model is called

```
fitG = Model(conductance)
```

and the data fitting is performed by giving the function the measurement data

```
out_G = fitG.fit(G, omega = omega, R = Rinit, L = Linit, C = Cinit)
```

where G is the measured conductance by the impedance analyser, and omega is the angular frequency. This data is obtained from the impedance analyser *.csv file they are stored in. The extraction process followed is: 1) use Panda's dataframe to read it from the file, 2) convert G and omega to Numpy arrays. Next, in order to ensure a correct data fitting, approximate initial values for R, L, and C must be given to the function.

Plotting of the data fitting is highly recommended to ensure the fit is correct:

```
# Plot the measured data
plt.plot(omega, G, 'bo')
# Plot the data fitting with the proposed R, L, C values
plt.plot(omega, out_G.init_fit, 'k- -', label='initial fit')
# Plot the fit
plt.plot(omega, out_G.best_fit, 'r-', label='best fit')
plt.legend(loc='best')
plt.show()
```

Finally, MEMS resonance frequency and quality factor are obtained with the R, L, C parameters from the fit

```
fres = 1/(2*math.pi*math.sqrt(out_G.params['L'].value*out_G.params['C'].value))
Q = (1/out_G.params['R'].value)*math.sqrt(out_G.params['L'].value/out_G.params['C'].value)
```

Appendix B: published articles

During the thesis, the following journal article has been published with the results reported in chapter 2:

J. M. Sánchez-Chiva, J. Valle, D. Fernández and J. Madrenas, "A Mixed-Signal Control System for Lorentz-Force Resonant MEMS Magnetometers," in IEEE Sensors Journal*, vol. 19, no. 17, pp. 7479-7488, 1 Sept.1, 2019.*

Abstract: This paper presents a mixed-signal closed-loop control system for Lorentz force resonant MEMS magnetometers. The control system contributes to 1) the automatic phase control of the loop, that allows start-up and keeps self-sustained oscillation at the MEMS resonance frequency, and 2) output offset reduction due to electrostatic driving by selectively disabling it. The proposed solution proof-of-concept has been tested with a Lorentz force-based MEMS magnetometer. The readout electronic circuitry has been implemented on a printed circuit board with off-the-shelf components. Digital control has been implemented in an FPGA coded with VHDL. When biased with 1 V and a driving current of 300 μA_{rms}, the device shows 9.75 $pA/\mu T$ sensitivity and total sensor white noise of 550 $nT/\sqrt{Hz}$. Offset when electrostatic driving is disabled is 793 μT, which means a 40.1% reduction compared when electrostatic driving is enabled. Moreover, removing electrostatic driving does not worsen bias instability, which is lower than 125 nT in both driving cases.

Conference publications and talks also related to CMOS-MEMS and readout circuits:

C. Bauzá, J. M. Sánchez-Chiva, J. Madrenas and D. Fernández, "Optimizing Power Consumption vs. Linearization in CMFB Amplifiers with Source Degeneration," in 2018 25th IEEE International Conference on Electronics, Circuits and Systems (ICECS)*, Bordeaux, 2018, pp. 269-272.*

Abstract: In this work, a low power consumption approach to achieve linear Differential Difference Amplifier CMFB circuits is introduced. A solution based on source degeneration in the input differential pairs is proposed to reduce input range linearity limitations as well as CMFB input pair large current consumption by accurately selecting both current and degeneration resistance to maximize linearity. The proposed technique has been implemented in a CMFB amplifier of a fully differential OTA, resulting in a THD of 0.026% when using degeneration resistances of 48 $m\Omega$ and 53.3 μA of bias current. Moreover, linearity improvement using the proposed technique has shown better figures than increasing only the bias current.

J. M. Sánchez Chiva, S. Banerji, "Under pressure? Dont lose direction! Smart Sensors: Development of CMOS and MEMS on the same platform," in 4th Jornada d'Investigadors Predoctorals Interdisciplinaria*, Feb. 2016.*

Abstract: Micro Electro Mechanical Systems (MEMS) are movable structures fabricated on the surface of silicon chips by selectively depositing and etching away materials and silicon. Such movement allows the measurement of a wide range of parameters. In the recent years, the integration of MEMS devices and electronics on the same chip i.e. CMOS-MEMS integration, has allowed the improvement of sensors performance and fabrication costs, extending their integration in all types of devices. In the Advanced Hardware Architectures research group at the UPC, we are currently conducting research on system-on-chip CMOS-MEMS magnetic field and pressure sensors.
Contrary to pressure sensors using other technologies, resonant pressure sensors allow direct coupling to digital electronics without requiring analog to digital converters (ADCs). This feature enhances their resolution and reliability by providing more immunity to noise and interference. Recently, monolithically integrated CMOS-MEMS resonant pressure sensors have been extensively used in atmospheric pressure monitoring and altitude sensing due to their low cost, small size and high reliability. Presently, the pressure sensors integrated in the smartphones and wearable devices suffer from poor sensitivity. The primary purpose of our study is to develop an optimized CMOS-MEMS resonant pressure sensor with enhanced sensitivity at atmospheric pressure which can be utilized in a vertical GPS enhancement system.
Magnetic field sensors are key in the development of electronic compasses integrated in smartphones and other devices. Currently, magnetic sensors used in smartphones do not use MEMS technology but sensors that require materials incompatible with the fabrication of CMOS electronics. Our objective is to improve the performance of MEMS based electronic compasses by using Lorentz force based MEMS magnetic sensors. Such sensors, are compatible with CMOS process and could substitute actual sensors by reducing fabrication cost.

As a side project, some research has been done on integrated light energy harvesting:

J. Madrenas, J. M. Sánchez-Chiva, D. Fernández and J. Cosp, "Design Considerations for Analog LCMOS Harvest-Use Integrated Signal Processing," in 2019 IEEE International Symposium on Circuits and Systems (ISCAS)*, Sapporo, Japan, 2019, pp. 1-5.*

Abstract: Optical energy harvesting enables the development of autonomous microsensor networks. The harvest-use approach applied to monolithic standard bulk CMOS is simple but suffers from the low-voltage issue of single photodiode as a voltage supply. It is overcome by using the LCMOS approach with complementary voltage generation, thus achieving a usable supply around 900 mV. Guidelines to develop analog circuits with this approach are provided. Power supply, references and folded cascode amplifier design are introduced. Simulation results for TSMC 0.18 μm are provided and applications in the area of integrated sensors are pointed out.

Finally, some works have been published in the topic of CMOS-MEMS accelerometers and readout circuits. These publications are a consequence of the participation in the research performed by the research group during the Master thesis.

J. M. Sánchez-Chiva, P. Michalik, D. Fernández and J. Madrenas, "A CMOS BEOL accelerometer low-noise readout amplifier with 4.2 $zF/\sqrt{Hz}$ *total noise floor," in* 2015 IEEE SENSORS*, Busan, 2015, pp. 1-4.*

Abstract: This article describes a low-noise readout amplifier for a post-CMOS BEOL (Back End Of Line) surface micromachining capacitive accelerometer. Simulations show 300.0 $zF/\sqrt{Hz}$ acceleration and 4.2 $zF/\sqrt{Hz}$ capacitance noise floors while chopping at 1 MHz and having a power consumption of 1.38 mW. The performed noise minimization is described, comprising input transistor pair type election, optimum input pair inversion region and dimensions using an all-region EKV model and equations describing parasitics and loop characteristics of the circuit. Simulations have been included that verify the theoretical model accuracy and demonstrate final circuit noise performance. The circuit layout has been taped out and testchip availability is expected soon for experimental measurements.

P. Michalik, J. M. Sánchez-Chiva, D. Fernández and J. Madrenas, "CMOS BEOL-embedded lateral accelerometer," in 2015 IEEE SENSORS*, Busan, 2015, pp. 1-4.*

Abstract: In this paper we present to the best of our knowledge a first ever reported CMOS BEOL-embedded lateral acceleration sensor obtained by simple isotropic inter-metal dielectric etching without any additional substrate etching steps. The device leverages the availability of thick metal and via layers of a 0.25 μm RF CMOS technology, featuring 7.36 kHz resonance frequency and differential capacitive sensitivity 0.2 fF/G. The accelerometer is monolithically integrated with on-chip sensing electronics exhibiting 200 $\mu G/\sqrt{Hz}$ total noise floor at 2.5 V power supply and 550 μA current consumption.

P. Michalik, J. M. Sánchez-Chiva, D. Fernández and J. Madrenas, "CMOS BEOL-embedded z-axis accelerometer," in Electronics Letters*, vol. 51, no. 11, pp. 865-867, 28 5 2015.*

Abstract: A first reported complementary metal-oxide semiconductor (CMOS)-integrated acceleration sensor obtained through isotropic inter-metal dielectric (IMD) etching of a back-end-of-line (BEOL) integrated circuit interconnection stack, without any additional substrate etching steps, is presented. The mechanical device composed of a CMOS-process 8 μm-thick metal-via-metal stack of 135 μm diameter and suspended 2.5 μm over a bottom fixed electrode, has a resonance frequency of 20 kHz, a sensing capacitance of 50 fF with sensitivity 14 aF/G and it is integrated on the same substrate with a simple low-noise amplifier reaching 25 mG of RMS noise measured from 0.25 to 100 Hz bandwidth.

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