PHYSICAL BEHAVIOUR ANALYSIS AND COMPACT TEMPERATURE-DEPENDENT MODELING IN ORGANIC AND IGZO TFTS

Harold Cortes Ordoñez

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Physical behaviour analysis and compact temperature - dependent modeling in Organic and IGZO TFTs

DOCTORAL THESIS

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Nano-Electronic and Photonic Systems(NePhoS)

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I STATE that the present study, entitled "Physical behaviour analysis and compact temperature - dependent modeling in Organic and IGZO TFTs ", presented by Harold CORTÉS ORDOÑEZ, for the award of the degree of Doctor in Technologies for Nanosystems, Bioengineering and Energy, has been carried out under my supervision at the Departament d'Enginyeria Electrònica,Elèctrica i Automàticaof this university and it satisfies all requirements to be eligible for the International Doctorate Award.

Dr. Benjamin IÑIGUEZ NICOLAU
Doctoral Thesis Supervisor

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Declaration of Authorship

I, Harold CORTÉS ORDOÑEZ, declare that this thesis titled, "Physical behaviour analysis and compact temperature - dependent modeling in Organic and IGZO TFTs " and the work presented in it are my own. I confirm that:

- This work was done wholly or mainly while in candidature for a research degree at this University.
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- Where I have consulted the published work of others, this is always clearly attributed.
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- I have acknowledged all main sources of help.
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"Everything is theoretically impossible, until it is done"

Robert A. Heinlein

"No es cierto que la gente deje de perseguir sus sueños porque envejece, más bien envejece cuando deja de perseguir sus sueños"

Gabriel García Márquez

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Abstract

Departament d'Enginyeria Electrònica,Elèctrica i Automàtica

Escola Técnica Superior d'Enginyeria

Doctor in Technologies for Nanosystems, Bioengineering and Energy

Physical behaviour analysis and compact temperature - dependent modeling in Organic and IGZO TFTs

by Harold CORTÉS ORDOÑEZ

In this thesis, we target the drain current modeling for organic thin film transistors (OTFTs) and Indium-Gallium-Zinc-Oxide thin film transistors (IGZO TFTs) from 150K to 370K. Using the current models developed, we analyse the temperature dependences by applying direct parameter extraction methods to experimental $I-V$ characteristics applying temperatures from 150K up to 370K for OTFTs and IGZOs. In addition, we analyse the gate capacitance behaviour ranging the temperature from 200K up to 300K. Most parameters of the gate capacitance model are extracted from $I-V$ characteristics. We successfully validated our models by comparison with experimental $I-V$ characteristics of both OTFTs and IGZO TFTs from 150K up to 370K and $C-V$ characteristics at different frequencies for OTFTs.

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List of Abbreviations

TFT	**T**hin **F**ilm **T**ransistor
OTFT	**O**rganic **T**hin **F**ilm **T**ransistor
IGZO	**I**ndium- **G**alium- **Z**inc- **O**xide
DOS	**D**ensity **O**f **S**tates

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Physical Constants

Boltzmann constant	$kb = 1.38064852x10^{-23}\ m^2kgs^{-2}K^{-1}$
Vacuum permittivity	$\epsilon_0 = 8.854x10^{-12}\ CV^{-1}m$
Electric charge	$q = 1.602x10^{-19}\ C$

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List of Symbols

I_{DS}	Drain to source current	A
W	TFT width channel	m
C_i	Insulator capacitance	Fm^{-1}
V_{GS}	Gate to source voltage	V
V_T	Threshold voltage	V
L	TFT length channel	m
R	Channel resistance	Ω
V_{DS}	Drain to source voltage	V
I_0	Leakage current	A
$V_{DS_{sat}}$	Saturation drain to source voltage	V
m	Sharpness of the knee region	
V_{FB}	Flat band voltage	V
V_{AA}	DOS fitting parameter	V
T	Transistor operation temperature	K
V_{Gte}	Effective gate voltage	V
V_{Dte}	Effective drain voltage	V
$S_{V_{Gte}}$	Fitting parameter	C^{-1}
S	Subthreshold swing	$VDecade^{-1}$
d_i	Insulator thickness	m
Q_{CH}	Total channel charge	C
C_{CH-G}	Channel to gate capacitance	F
C_{G-G}	Gate to gate capacitance	F

W_D	Depletion width	m
N_B	Non intentional doping	cm^{-3}
C_D	Depletion capacitance	F
C_{EQ}	Equivalent capacitance	F
C_{G-D}	Gate to drain capacitance	F
I_{DSo}	Current at $V_{GS} = 0V$	A
R_{CO}	Constant resistance	Ω
E_A	Activation energy	eV
g_{ato}	Maximum trap density	cm^{-3}
D_{it}	Interface states density	$cm^{-2}eV^{-1}$
E_{FO}	Fermi level	eV
E	Valence band energy	eV
μ_{FET}	Effective mobility	$cm^2V^{-1}s^{-1}$
μ_{FET_0}	Low per and long mobility	$cm^2V^{-1}s^{-1}$
λ	Channel length modulation	V^{-1}
μ_0	Mobility at $V_{GS} = 1V$	$cm^2V^{-1}s^{-1}$
γ	Deviation from crystalline behaviour	
α	Saturation modulation	
ω	Angular frequency	Hz
ϵ_i	Dielectric constant	Fm_{-1}
ϵ_s	Semiconductor permittivity	$CV^{-1}m^{-1}$

Dedicated to my mother, Adela Ordoñez Torres (RIP).

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Introduction

Before the first transistors appeared (Edgar, 1930)(fig.1) in 1947, electron tubes were used to control the electric current. This component required high voltage, high power consumption, the efficiency was lower and even, it was bulky. This electronic component was called the vacuum tube. Since the Bell Labs in 1946, a group of scientific started to research in a new device that gave solution to fundamental limitations of the vacuum tubes.

The transistor is an electron semiconductor device able to conduct and stop current. This component is used to control the flow current thorough a electronic pulses (Edgar, 1930). This semiconductor device can be P and N type. The transistor has a very long life, smaller in size, and it works at low voltages and currents. The first transistor worked using semiconductor junctions instead of heated electrodes in vacuum chamber. The first semiconductor transistor was manufactured with Germanium (Edgar, 1930) (Heil, 1935) (Arns, 1998).

Over the years have new technologies of transistors and their performance is enhanced every time. There are different types of transistors for different engineering applications. Bipolar

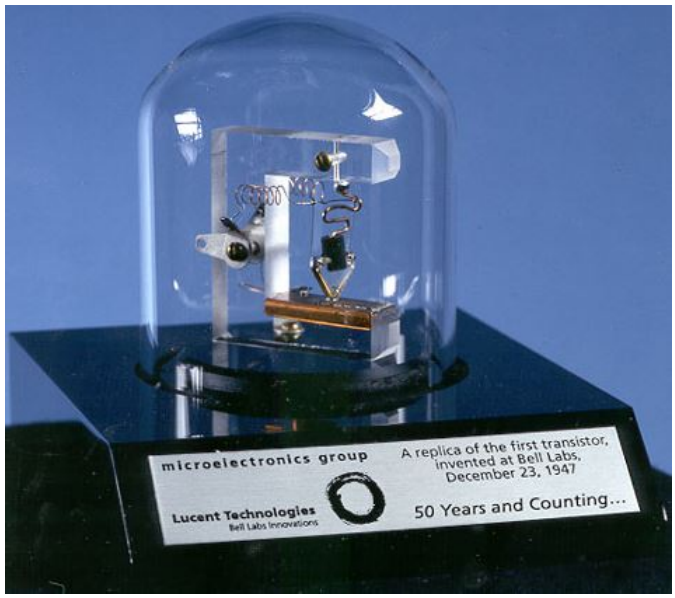

FIGURE 1: First transistor invented by John Bardeen, Walter Brattain and William Shockly at Bell Labs in 1947

junction transistors(BJT) (Palmour and Edmond, 1990), heterojunction bipolar transistors(HBT) (Cressler and Niu, 2003), Darlington transistors (Colman and Cotton, 1986), Schottky transistors (Shockley, 1956) are some of the most important types of transistor developed through the years.

One of the most important types of transistors is the field effect transistor (FETs). The majority of the transistors used in integrated circuit are FETs. Some of their advantages are their lower consumption and small size (Bischoff and Krusius, 1985). Also FET transistors are used in RF technologies as amplifier switch (Choi et al., 2009).

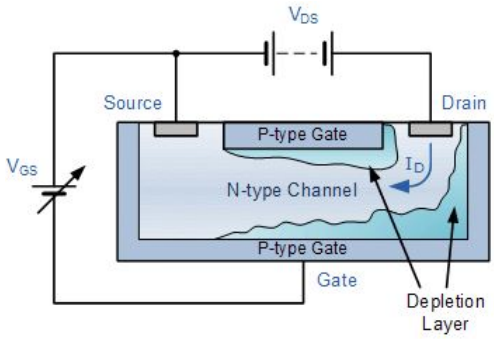

FIGURE 2: Example of a field effect transistor structure

The field effect transistor is composed of three electrode terminals called gate , drain and source. The gate controls the electron or hole carriers located in the semiconductor channel that flow from the source to the drain. This channel can be n-type(electron carriers) or p-type(hole carriers) (Yabuta et al., 2010).

The metal-oxide-semiconductor-field-effect transistor (MOSFET) is fabricated by the controlled oxidation of the silicon. This silicon oxide layer is p or n type. The metal oxide semiconductor structure works as a parallel plate capacitor where the gate and the substrate are the plates and the silicon oxide is the insulator (Wodarczyk et al., 1992).

One type of transistor are the thin film transistors(TFTs). This transistors are FET devices where the active semiconductor region is a thin film amorphous, nanocrystalline or polycristalline semiconductor,and as in MOSFETs, there is a dielectric between the gate gate and the active semiconductor layer. This

mentioned layers are made by depositing thin film of an amorphous or polycrystalline materials (Tokunaga, 2010).

The amorphous silicon (a-Si:H) TFT nowadays the most used TFT for large area electronic application (Powell, 1989). This a-Si:H TFT is used in displays due to the possibility to depositing over big areas with a high resolution (Nathan et al., 2004). The low cost and their mass manufacturing make a-Si:H transistors a suitable devices for displays and large area electronic applications (Carlson and Wronski, 1976).

Two of the most promising new technologies of TFTs are the Indium-Gallium-Zinc-Oxide thin film transistors (IGZO TFTs) and the organic thin film transistors (OTFTs) (Ito et al., 2008b). Recently, the research community is taking interest in these TFTs technologies and researchers have been considerably improving the performances of these transistors.

The IGZO TFTs and OTFTs are deposited or printed in flexible substrates due to their low deposition temperature(similar to the environment temperature). Thus, these transistor technologies are becoming very interesting in the development of new technologies as flexible and printed electronics (Wong and Salleo, 2009).

An IGZO TFT has in their semiconductor layer a material based in Indium-Gallium-Zinc-Oxide. This transistor technology was developed by Hideo Hosono in Tokio- Japan in 2003 (Hosono, 2018). This device has an optimal behaviour in display applications. The IGZO devices have a low consumption. The electron mobility of this device is higher than other TFTs technologies. As the electron mobility is high in this

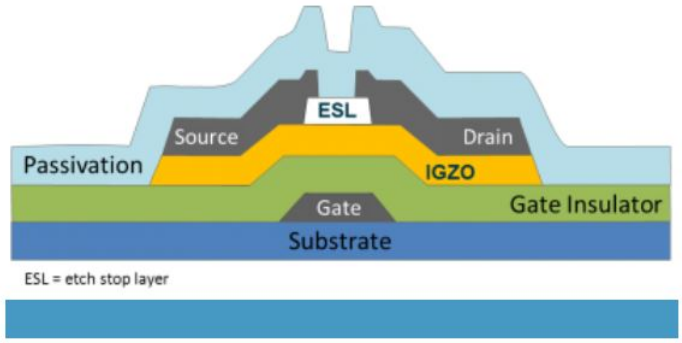

FIGURE 3: Indium-Gallium-Zinc-Oxide thin film transistor structure

kind of transistors, these devices reach higher performances than other TFTs. (Ito et al., 2008a) (Kim et al., 2012) (Ito et al., 2008b). The IGZO TFTs are manufactured by different deposition techniques such as Pulsed Laser Deposition, Solution processing and combustion synthesis. Nowadays, the combustion synthesis technique best known is the Spin coating. In this process, a coating material is applied on the center of the substrate and the coating material is spread due to a centrifugal force applied to the substrate. The substrate rotate at 10000 rpm (Park et al., 2010).

The OTFTs has as semiconductor active layer an organic or small molecule material (Horowitz, 2004). The main advantage of this device is their manufacturing processes. This fabrication methods are low cost and simple (Hirai, 2004) (Klauk, 2006). One important feature of this technology is that its mechanical flexibility makes them compatible with

flexible displays. Other promising applications of this devices are the biosensors (Roberts, Sokolov, and Bao, 2009) (Sheraw et al., 2002) and electronic papers circuitry.

Much effort has been dedicated to the development of electronic devices based on both main types of organic materials: oligomers and polymers. These two kinds of organic materials present important differences related to both their properties and methods of preparation. While oligomers are usually obtained by vacuum deposition techniques, polymers are most frequently deposited by spin coating or inkjet printing. Concerning their properties, conductivity and non-intentionally doping is usually lower for polymers than for oligomers; polymers also present a more disordered structure than oligomers. In polymers, P3HT is the one that has presented highest mobility values, above $5x10^{-2}\frac{cm^2}{Vs}$ (Lyuleeva et al., 2018). Another feature of organic materials that can vary significantly from one material to another is the energy distributions of localized states (DOS), which, in addition, can be further modified with annealing processes.

Currently, the OTFTs can be manufactured using printing methods such as inkjet printing process. But, the roll to roll printing process is taking advantage over other printing processes. In this process, a roll with the OTFT structure template spreads the semiconductor ink over another roll that contains the substrate(fig.5). By means of the roll to roll process the OTFTs can be manufactured in mass and their effective manufacturing cost is low.

There are different OTFTs manufacturing processes such as

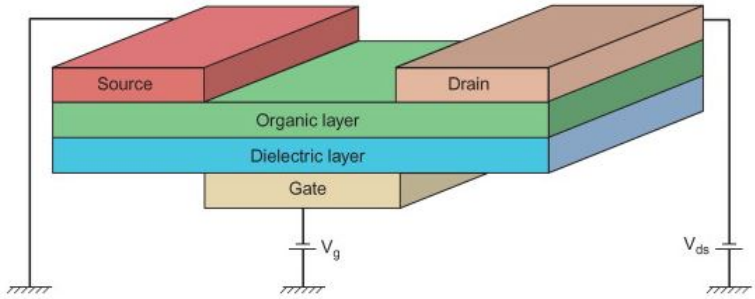

FIGURE 4: Organic thin film transistor structure

sputtering, chemical and physical vapor deposition, organic evaporation and another solution-based processes.In the sputtering process, energetic ions are accelerated towards a target(substrate or glass). This ions strike the target and atoms are sputtered from the surface. The atoms advance until the substrate and incorporate into the growing film (Lee et al., 2013). The chemical vapor deposition is a process in which precursor gases react to form film deposits on a substrate. The advantage of this manufacturing method is that this process can be carry out at atmospheric pressure and temperature (Chou et al., 2017).

Organic material deposition requires uniform and precise heating with excellent temperature and deposition rate control. This is commonly achieved using a source similar to an effusion furnace (also known as a knudsen cell or k-cell). In this type of source, evaporation of the target material occurs via electrical (Joule) heating of a refractory metal filament

coiled around a metal, ceramic, or quartz crucible. The crucible is heated above the melting or sublimation point of the source material to create adequate vapor pressure for deposition (Taylor, 2015).

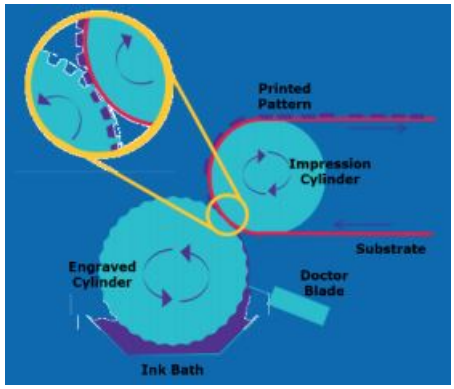

FIGURE 5: OTFT Roll to roll manufacturing process

The structure, manufacturing process and performance of the transistor has been evolving over the years, for this reason the used of models that describes relevant physical phenomena, mobility, current, voltage and capacitance in transistors plays a fundamental role in this technological evolution. Without these models, it would be impossible to analyse the behaviour of these devices and then improvements would impossible. Since the first transistor appeared, the physical behaviour models have been evolving as transistor technology evolved.

Nowadays, the models used in circuit simulators are called compact models. This compact models are composed of analytical equations using physical and fitting parameters used to reproduce accurately physical phenomena.

An example of parameter extraction and compact model is the Unified Model and Parameter Extraction Method (UMEM) applied to thin film transistor. The UMEM extracts the main electrical parameters (mobility, threshold voltage, temperature characteristic of density if states, etc) from the experimental measurements of the TFT under study. Also, the method works at different transistor geometries, allowing the comparison between two or more device technologies be possible (Estrada et al., 2005).

As mentioned before, the compact models have played an important role for the research community in the evolution and new applications of transistors, and the same can be expected for IGZO TFTs and OTFTs.

This doctoral thesis presents the development and improvement of temperature-dependent capacitance and drain current models in OTFTs and IGZO TFTs taking into account different physical phenomena existing in these devices. These models are developed to ease the incorporation of these electron devices in large area and flexible electronics applications.

This document is divided in 4 chapters that show the development of compact models and its validation. In the first part of this work, we present a gate capacitance compact model for OTFTs transistors and the verification of this model by comparison with experimental results from OTFTs manufactured by CEA-Liten (France). In the two next chapters, a compact drain current model for OTFTs transistor valid for both the above and subthreshold regimes is developed. The validation of this model was carried out at different temperatures

from 150K up to 350K. The devices under analysis was manufactured by CEA-Liten. An analysis of the model parameters extracted with different temperatures model is carried out.

Finally, the compact drain current model used for OTFTs is adapted to IGZO devices and validated in IGZO transistors manufactured by TNO Netherlands. We also present an analysis of parameters behaviour at temperatures from 200K to 370K.

Chapter 1

Gate capacitance compact model in Organic Thin Film Transistor

In the past years, important research has been made in OTFT modeling (Marinov, Deen, and Iniguez, 2006) (Estrada et al., 2005) (Horowitz and Delannoy, 1991) (Zaki et al., 2014), giving emphasis to develop an accurate $I - V$ model for these devices. However, little attention has been given to model the $C - V$ characteristics of the device (Marinov, Deen, and Iniguez, 2005) (Calvetti, Colalongo, and Kovacs-Vajna, 2005) (Fadlallah et al., 2006) (Li et al., 2010) (Marinov, 2015) (Marinov et al., 2006).

Regarding $C - V$ modeling, there are a few models of capacitance in accumulation regime; some models apply different functions for the accumulation regime and the subthreshold regime (Castro-Carranza et al., 2012). Also, there

are capacitance models which consider the frequency dependence. These models can be used for low, medium and high frequencies (Castro-Carranza et al., 2014). Nevertheless, to the best of our knowledge, there is no capacitance model that works over a wide range of frequencies and valid up to the first capacitance derivative using a analytical expression.

A compact capacitance model has to describe every physical effects present in the capacitance of OTFTs. For example, the compact capacitance model presented by (Horowitz and Delannoy, 1991) reproduces very well the experimental gate to gate capacitance data and it considers each physical behaviour presented in the subthreshold regime, as well, in the accumulation regime, but it is composed of many physical parameter being that the simulation softwares and circuits simulation becomes complicate.

In this chapter, we present a compact capacitance model developed for OTFTs valid from depletion to accumulation regime with continuous and smooth transition as well as for the first order capacitance derivative. This model takes into account the mobility and current at different frequencies. The compact capacitance model uses the UMEM parameter extraction procedure presented in (Estrada et al., 2005); parameters are extracted from $I - V$ data.

The compact capacitance model developed is used to analyze the effect of the parameter related to the density of states (DOS) in the capacitance. In accordance to (Castro-Carranza et al., 2012), OTFTs show a high crystallinity degree when this parameter is close to 0. At the same time, this parameter

describes the manufacturing quality and it is used to characterize phenomena that affect the OTFTs devices.

The first order capacitance derivative has been considered as a method to extract the threshold voltage (V_T) and the flat-band voltage (V_{FB}) in crystalline field effect transistors (equivalent to the second derivative method) (Rudenko et al., 2013) (Rudenko et al., 2014) (Rudenko et al., 2005) (Rudenko et al., 2012). Here we study it in OTFTs and from it we discuss the information provided regarding V_T, V_{FB} and the operating regimes in OTFTs.We demonstrate that our model reproduces very well the experimental results of the first order capacitance derivative.

1.1 Capacitance model

The capacitance model developed in this work is based on (Castro-Carranza et al., 2014) with specific improvements in depletion regime.To extract the parameters, we model the I-V characteristics by means of the expression

$$I_{DS} = \frac{-WC_i\mu_{FET}(V_{GS}-V_T)}{L(1+R\frac{W}{L}C_i\mu_{FET}(V_{GS}-V_T))} \frac{V_{DS}(1+\lambda V_{DS})}{[1+[\frac{V_{DS}}{V_{DSsat}}]^m]^{\frac{1}{m}}} + I_0 \tag{1.1}$$

where W and L are the channel width and length respectively, Ci is the insulator capacitance,V_{DS} and V_{GS} correspond

to drain to source voltage and gate to source voltage respectively. R is the resistance between source and drain, I_0 is the leakage current, λ and m control the channel length modulation and the sharpness of the knee region respectively (Estrada et al., 2005). The field effect mobility dependence is modeled as

$$\mu_{FET} = \mu_{FET_0}(V_{GS} - V_T)^{\gamma} \tag{1.2}$$

$$\mu_{FET_0} = \frac{\mu_0}{V_{AA}^{\gamma}} \tag{1.3}$$

being μ_{FET_0} related to the value of the mobility for low perpendicular and longitudinal electric field(Cerdeira et al., 2001).μ_0 correspond to the band mobility for the OTFT under study and V_{AA} is related to the density of states (DOS) (Estrada et al., 2008a) and it is extracted using the UMEM procedure (Estrada et al., 2005).The saturation voltage calculated by 1.5 depends of the saturation modulation parameter (α).The γ parameter indicates the deviation from crystalline mobility behaviour. This parameter is related to DOS by means of the characteristic temperature (T_0) (Estrada et al., 2008a).This parameter is also extracted through the UMEM procedure.In particular γ parameter is given by eq.1.4.

$$\gamma = 2\frac{T}{T_0} - 2 \tag{1.4}$$

On the other hand, the saturation voltage is calculated as

$$V_{DSsat} = \alpha(V_{GS} - V_T) \tag{1.5}$$

As discussed in (Castro-Carranza et al., 2014), to obtain an

expression of the total channel charge(Q_{CH}), it is necessary to use the non linearized equation of the drain to source current. This current is written as

$$I_{DS} = \frac{-WC_i}{L}\frac{\mu_{FET_0}}{Vaa^{\gamma}} \frac{((V_{GTe} - V_{DSe})^{2+\gamma} - V_{GTe}^{2+\gamma})(1 + \lambda V_{DSe})}{2+\gamma} \tag{1.6}$$

where the effective drain to source voltage (V_{DSe}) is given by the expression

$$V_{DSe} = \frac{V_{DS}}{[1 + (\frac{V_{DS}}{\alpha V_{GTe}})^m]^{\frac{1}{m}}} \tag{1.7}$$

Actually eq.1.1 is the linearized (in terms of V_{DS})version of eq.1.6. It is important to use an effective gate voltage expression (V_{GTe}) because this extends the current model shown in the expression eq.1.6 to subthreshold regime. This equation allows to calculate the drain current in both subthreshold and accumulation regimes making this model more accurate. V_{GTe} is calculated as

$$V_{GTe} = S_{V_{GTe}} k_b T ln[1 + e^{(\frac{V_{GS} - V_T}{S_{V_{GTe}} k_b T})}] \tag{1.8}$$

where, $S_{V_{GTe}}$ is a fitting parameter, k_b is Boltzmann constant, T is the operation temperature of device.

The insulator capacitance(Ci) is calculated considering gate

insulator thickness (d_i), the vacuum permittivity (ε_0) and dielectric constant (ε_i) as

$$Ci = \frac{\varepsilon_0 \varepsilon_i}{d_i} \tag{1.9}$$

The above expression considers the frequency dependence, according to the formula proposed by Cole and Cole (Cole and Cole, 1941) (Castro-Carranza et al., 2014).The dielectric constant as a function of the frequency can be obtained by

$$\varepsilon_i = \varepsilon_{i\infty} + \frac{\varepsilon_{i0}\varepsilon_{i\infty}}{1 + (\frac{w}{2\pi\eta})^{1.78p}} \tag{1.10}$$

where $w = 2\pi f$, $\varepsilon_{i\infty}$ and ε_{i0} correspond to the permittivity at low and high frequency respectively, η is a fitting parameter has frequency units and p is a fitting parameter with value between 0 and 1 (Castro-Carranza et al., 2014).

The total channel charge expression was derived in (Castro-Carranza et al., 2012)

$$Q_{CH} = \frac{-WC_i^2}{I_{DS}} \mu_{FET} \frac{(V_{GTe} - V_{DSe})^{3+\gamma} - V_{GTe}^{3+\gamma}}{3+\gamma} \tag{1.11}$$

By differentiating eq.1.6 with respect to V_{GS}, we obtain the channel to gate and the gate to gate capacitances in accumulation regime as

$$C_{CH-G} = -\frac{\partial Q_{CH}}{\partial V_{GS}} = \frac{\partial Q_G}{\partial V_{GS}} = -C_{GG} \tag{1.12}$$

The depletion capacitance depends on the depletion width as

$$W_D = -\frac{\varepsilon_S}{Ci} + \sqrt{\frac{\varepsilon_S^2}{Ci^2} + \frac{2\varepsilon_S|V_{GS} - V_T|}{qN_B}} \tag{1.13}$$

where, ε_S represents the permittivity in the semiconductor layer, q is the electron charge and N_B corresponds to the non intentional doping concentration which is in order of $10^{14} cm^{-3}$ (Kim et al., 2013). If the film gets the full depletion, W_D takes the W value.

$$C_D = \frac{\varepsilon_S LW}{W_D} \tag{1.14}$$

In the gate capacitance model we consider that the capacitance in the deep subthreshold regime (C_D)is due to the film depletion (Castro-Carranza et al., 2014). It is modeled in eq.1.14.

$$C_{EQ} = \begin{cases} \dfrac{C_D CiWL}{(C_D + Ci)(WL)} & \text{if } V_{GS} < V_T \\ CiWL & \text{if } V_{GS} \geq V_T \end{cases} \tag{1.15}$$

Then, the final gate capacitance model is the result of a sum of the capacitance in accumulation regime given by the equation eq.1.12 and the depletion capacitance shown in the expression eq.1.15.The complete capacitance model can be calculated by

$$C_{TOT} = [|C_{EQ}|\frac{1 - tanh(\beta)}{2}] + [|C_{GG}|\frac{1 + tanh(\beta)}{2}] \tag{1.16}$$

where $\beta = (V_{GT} + \Delta V_T)Q2$, being ΔV_T a correction of the threshold voltage for capacitance in $C - V$ measurements. $Q2$

correspond to a transition parameter and has units of V^{-1} . The function *Tanh* gives a smooth transition between regimes.

Capacitances can be calculated as

$$C_{ij} = -\frac{\partial Q_i}{\partial V_j} \tag{1.17}$$

when i is different to j and

$$C_{ij} = \frac{\partial Q_i}{\partial V_j} \tag{1.18}$$

when i is equal to j

i and j can be any of the three terminal electrodes(drain-D, source-$S$and gate-G). In a 3-terminal device such as an OTFT there are 9 independent non reciprocal capacitances.

The gate to drain capacitance (C_{GD})for small signal simulation can be calculated from the Q_{CH} eq.1.11 (Castro-Carranza et al., 2012).C_{GD} is given by

$$C_{GD} = \frac{\partial Q_{CH}}{\partial V_D} \tag{1.19}$$

Finally, the gate to source capacitance (fig.1.1)(C_{GS}) eq.1.20 can be calculated as the difference between C_{TOT} and C_{GD} shown in the expressions eq.1.16 and eq.1.19 respectively (Castro-Carranza et al., 2012).

$$C_{GS} = C_{GG} - C_{GD} \tag{1.20}$$

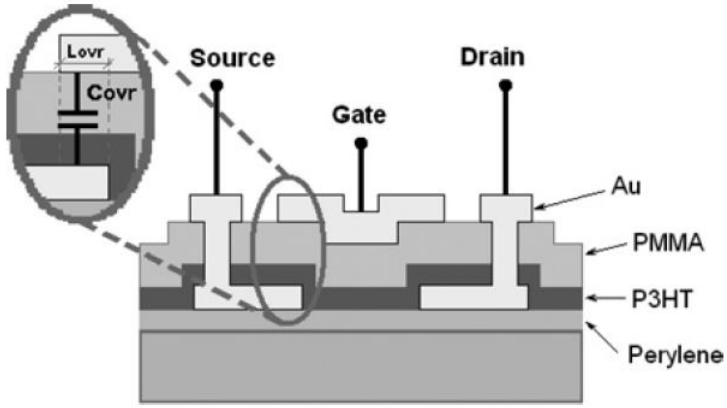

FIGURE 1.1: Capacitance between gate and source terminals in PMMA on P3HT thin film transistor structure

1.2 Capacitance compact model validation

To validate the developed capacitance model, we performed measurements on a polymer p-type polymeric MIS capacitor. Also,to carry out the parameter extraction, we performed $I-V$ measurements (tab.1.1) in OTFTs manufactured in CEA-Liten (Grenoble-France), the layers of which were of the same materials and had same thickness as the targeted MIS capacitors. The semiconductor organic layer is based in the SP400 polymer and the organic dielectric layer is fluorinated. According to eq.1.2 and eq.1.3 μ_{FET} is not directly extracted, since it depends on V_{GS}. Using our extracted parameters we obtained $\mu_{FET} = 0.418\frac{cm^2}{VS}$ at $V_{GS} = 30V$.The bias voltage applied to the capacitance measurement was $\pm 100mV$.

TABLE 1.1: Model parameters extracted from $I-V$ measurements. They have been used fro drain to source current, charge channel and gate to capacitance models.

Parameter	**Value**
α	0.663
γ	0.386
$\lambda[V^{-1}]$	-0.029
$\Delta V_T[V]$	-0.7
m	4.487
$Q_2[V^{-1}]$	0.8
$S_{V_{GTe}}[C^{-1}]$	5.5
$T[K^o]$	300
$V_{aa}[V]$	5.10^4
$V_T[V]$	3.09
$\eta[Hz]$	392
p	0.47

The MIS capacitor used in the measurements had as $L = 20\mu m$ and $W = 7860\mu m$. At low frequencies, we can apply our OTFT capacitance model to organic MIS capacitors with the same layer structure, materials and quicknesses. The charge and capacitance equations of the organic MIS capacitors are calculated from the gate charge and capacitance equations presented in the capacitance model for OTFT, and applying $V_D = 0V$, which requires to apply the L'Hopital rule to find the analytical expressions which are indicated in (Iñiguez and Moldovan, 2010)(for 3-terminal FETs). We will show in this section that our approach is valid at least up to 10kHz

The OTFT used to extract the parameters thorough UMEM

procedure from the $I - V$ curves were top gate bottom contact multifingers with 13 fingers, which corresponds to 13 parallel channels with $W_F = 665\mu$m each. The final channel dimensions are $W = 7980\mu m$ and $L = 20\mu m$. The source and drain have a width of $20\mu m$. The relative permittivity of the dielectric is approximately $2Fm^{-1}$ and the thickness is $700nm$. The semiconductor thickness is $40nm$ with a relative permittivity close to $4Fm^{-1}$. This wafer was manufactured by the roll to roll printing process.

It is important to highlight that we inverted the polarity of the model equations, voltages and the results obtained because the device used are P-type. Therefore, they were treated with the polarity of an N-type device. The manufacturer has not disclosed to the authors the chemical formulas and processing details by the fabrication of the samples.

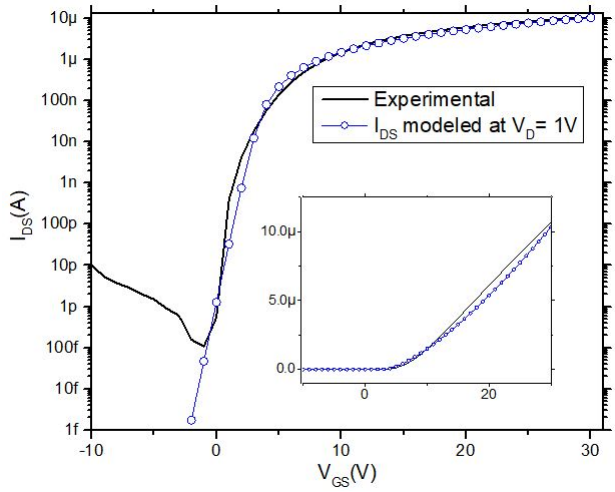

FIGURE 1.2: Modeled and experimental drain to source current(I_{DS}) as function of V_{GS}.

The measurements of the capacitor were taken at three different frequencies: 500Hz, 1kHz and 10kHz in parallel equivalent circuit mode. The equipment used for take this measurements is Agilent 4284A LCR Meter available in IMEP-LAHC Grenoble laboratories. As it can be seen in fig.1.2, the non-linear drain current model calculated data is in excellent agreement with experimental data.

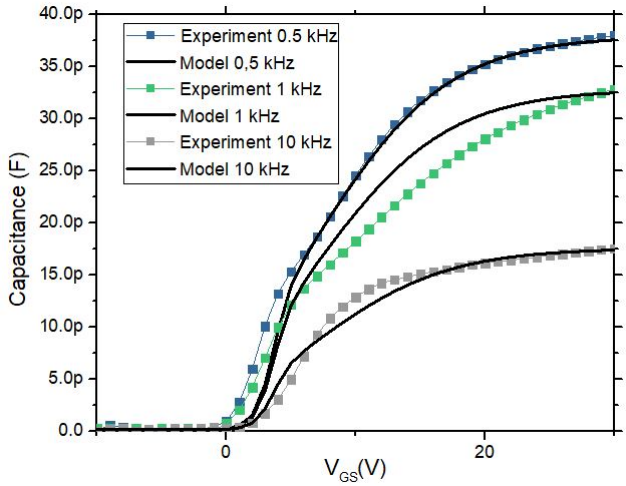

FIGURE 1.3: Modeled and experimental capacitance at 500Hz, 1kHz and 10kHz frequencies.

At 500Hz , the capacitance model reproduces from depletion to accumulation regime the measurement data very well as shown in fig.1.3 .A good agreement between the experimental and modeled values is obtained at 1kHz and 10kHz. This validates the capacitance model presented in this work. Following eq.1.10, $\epsilon_{i1} = 1.989$, $\epsilon_{i2} = 1.704$ and $\epsilon_{i3} = 1.182$ are

the values of the permittivity at 500Hz, 1kHz and 10kHz frequencies respectively.

1.3 First Order Capacitance Derivative

We apply the first order derivative to the gate capacitance obtained by our OTFT model and measurements. It was applied at the three targeted frequencies. The fig.1.4 shows the first derivative of C_{TOT} against V_{GS} applied to both measurements and model at 500Hz. Our model reproduces reasonably well the experimental results including the position of the observed two peaks taking into account that in every differentiation process usually some accuracy is lost.

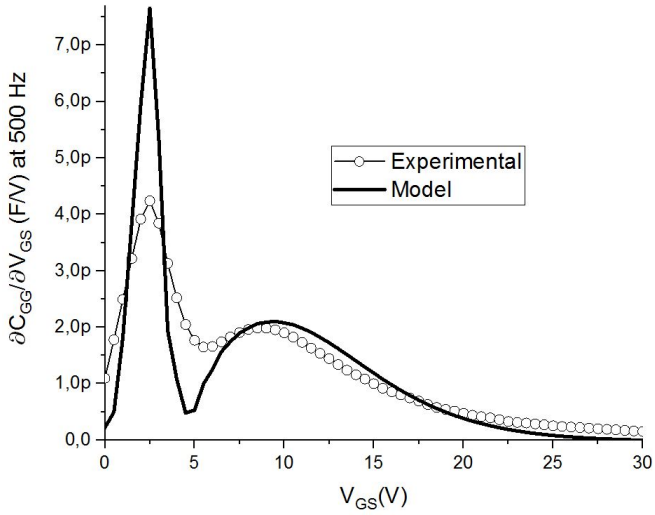

FIGURE 1.4: First derivative of C_{TOT} vs V_{GS} at 500 Hz

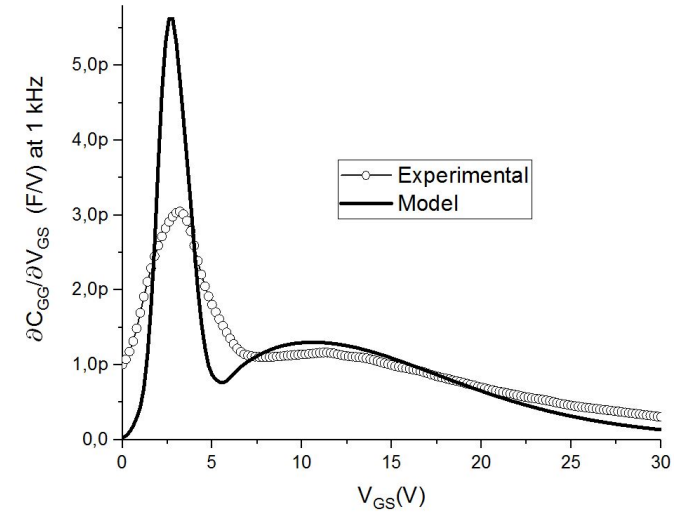

FIGURE 1.5: First derivative of C_{TOT} vs V_{GS} at 1 kHz

In fig.1.5, we analyzed the derivative of the gate capacitance at 1kHz. The agreement between model and experimental data is quite good, including the position of the two peaks.

At 10kHz, the agreement between experiment and model is still accurate. At higher frequencies, when non quasi static effects are very significant, we will need to account for them in a more accurate way that just by means of ϵ_i (Estrada et al., 2013).Anyway, we still observe in fig.1.6 only traces of the second peak.

The first peak corresponds to V_T defined as the transition voltage from full to partial depletion. The second peak is related to the transition between the partial depletion and the accumulation regime, which start at flat bland voltage(V_{FB})

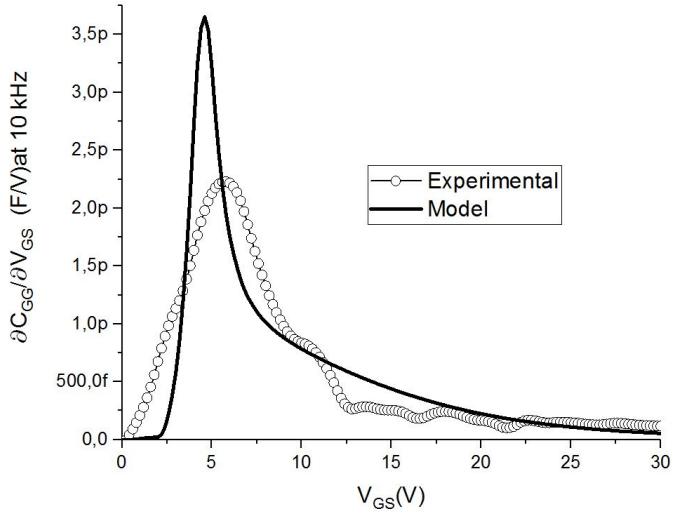

FIGURE 1.6: First derivative of C_{TOT} vs V_{GS} at 10 kHz

as it happens in crystalline accumulation mode (or depletion) SOI MOSFETs in accumulation mode (Rudenko et al., 2014). Our model reproduces quite well the transition between these operating models.

1.4 Review

We presented a compact OTFT capacitance model which shows good agreement with experimental $C-V$ data, and their derivatives, for frequencies up to 10kHz, and from the depletion to accumulation regimes. The capacitance model is derived from expressions of total charges compatibles with our previously presented drain current model. Most parameters of

the capacitance expressions were extracted from $I - V$ measurements.

We found that the C_{TOT} takes the C_i values in the accumulation regime. We observed that C_{TOT} decreases as the frequency increases, and we demonstrated that the theory proposed by (Cole and Cole, 1941) is fulfilled. i.e , ε_i is frequency dependent up to 10kHz in our manufacturing OTFT technology under study.

The analysis of the experimentally obtained first order capacitance derivatives shows clear transition behaviours between full and partial depletion, and between partial and accumulation behaviours. The second peak of the plots of the first order derivatives of the gate capacitance versus the gate voltage indicates in which voltage there is not electrical charge in the organic material. In other devices this voltages is called flat band voltage (V_{FB}). Our model reproduces quite well the results of the first order derivative of the gate capacitance(including the positions of both peaks) up to $10kHz$.

Chapter 2

Compact modeling of OTFTs at temperatures from 150K up to 300K

As explained in the Introduction and in Chapter.1, Organic TFTs are very promising devices for flexible and printed electronics. OTFT performances are already comparable to a-Si:H TFTs (fig.2.1). Therefore, OTFTs can be applied not only as sensors in flexible substrates, but also in circuits for sensor driving and interfacing. In order to design OTFTs circuits, physically-based current models for OTFT DC, AC and transient characteristics are needed. This requires a correct understanding of the physical effects affecting OTFT behaviour.

The behavior of I–V characteristics of organic thin film transistors, has been frequently represented using the same expressions as for MOSFETs (Horowitz et al., 1998), to which

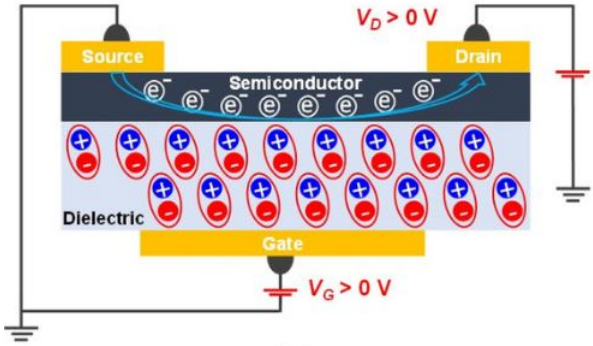

FIGURE 2.1: Representative structure of electron transporting of a n-channel thin film transistor

specific effects present in OTFTs as ohmic or non-ohmic resistance at drain and source contacts are added (Necliudov et al., 2003) (Klauk et al., 2003). The presence of leakage current through the dielectric (Shur et al., 2007), or across the channel are other features that have also been considered. The work presented by (Estrada et al., 2005) shows some pentacene OTFTs that can be very accurately modeled using the same expression for mobility as for amorphous silicon TFTs. The transistor model also included series resistance and non-ohmic contacts. Among the advantages of this method are the simple and precise extraction procedures that can be used to determine all model parameters from the electrical characteristics of the devices. At the same time, model parameters are related to physical properties of the device.

In general, mobility in OTFTs increases with gate voltage, although the law of growth may vary from one material to another. Some authors have reported also a dependence of mobility with V_{DS}, which has been related to a Frenkel–Poole type effect associated to traps in the material (Gupta, Jeon, and Yoo, 2008), as well as to the lowering of the emission barrier in traps located at the boundaries between crystals in polycrystalline materials (Verlaak, Arkhipov, and Heremans, 2003).

Material properties of polymers as molecular weight, regioregularity and in general its microstructure (Verilhac et al., 2006) (Sirringhaus et al., 2000), diluents in the case of spin casting deposition techniques (Joung et al., 2005), as well as involuntary or controlled doping (Jiang et al., 2002) (Arkhipov et al., 2003) can significantly modify not only the value of mobility at low fields, but its variation with temperature and voltage. In addition, processing conditions as thermal annealing will affect the properties of the materials and therefore mobility (Joung et al., 2005).

For the above reasons, the electrical behavior of organic devices may vary significantly for different materials and structures, which is something that must be taken into account when models are implemented.

From the theoretical point of view several expressions to model

mobility as function of different parameters have been obtained. For example, in (Arkhipov et al., 2003), the dependence of mobility with regioregularity in P3HT was reproduced, calculating mobility as function of charge carrier concentration, considering hopping as main transport mechanism and a double Gaussian DOS. Adjustment with experimental data was achieved by just fitting DOS parameters until agreement was met. In (Arkhipo et al., 2004), the same approach was used to model the dependence of mobility with doping concentration.

Since, the final goal of these studies is to model the behavior of the transistor, expressions representing the behavior of mobility must be previously obtained to be included in the transistor models.

Nowadays, new research in transistors semiconductor at low temperatures appears with the purpose to study the behaviour of different materials operating at temperatures lower than 300K. For this, it is necessary to develop current models able to analyse physical effects with temperature dependences (Jonscher, 1964).

Very few models have considered the temperature dependence, although temperature analysis is useful to identify relevant physical mechanisms. Most of those temperature studies have been carried out only for I-V characteristics at high temperatures and do not address all parameters. The work by (Estrada et al., 2013) only targets mobility in polymeric transistors.

A recent paper presents results of low temperature I-V characteristics in OTFTs and the temperature dependence of some parameters within a range of low temperatures (Haddad et al., 2018) (Wang, Register, and Dodabalapur, 2019) (Wang and Dodabalapur, 2018). However, the parameter extraction method used is based on crystalline devices, and as a result, parameters which are related to the OTFT Density Of States (DOS) are not studied. Currently, to improves the performance of this devices since the physical point of view, have been developing different manufacturing process to manage the physical parameters explained before in OTFTs (Lodha and Singh, 2001).

In the first part of this second chapter, we present a complete analysis of the current in an OTFTs manufacturing technology for temperatures ranging from 150K to 300K. Parameters were extracted using a physically based unified model and extraction method (UMEM), specific for OTFTs, based on assuming an exponential DOS and variable range hopping (Estrada et al., 2008a) (Zaki et al., 2014). The dependence of model parameters with temperature are determined. Lastly, we analyze the C-V behavior at low temperatures from 200K to 280K using the compact capacitance model able to work in both, depletion and accumulation regime (Cortes-Ordonez et al., 2019).

The parameters used in the I-V characteristics are extracted as (Estrada et al., 2005) (Kim et al., 2013). Using the extracted

values of the parameter, our model shows very good agreement with the experimental I-V and C-V curves in both technologies for temperatures ranging from 150K to 300K in two manufacturing technologies and from 200K to 280K respectively.

2.1 OTFT drain current model and parameter extraction

In OTFTs, as in inorganic amorphous TFTs, the μ_{FET} as function of V_{GS} is modeled by the following expression

$$\mu_{FET} = \mu_0 \frac{(V_{GS} - V_T)^{\gamma}}{(V_{aa})^{\gamma}} \tag{2.1}$$

rewriting the last expression,

$$\mu_{FET} = \frac{\mu_0}{V_{aa}^{\gamma}} (V_{GS} - V_T)^{\gamma} \tag{2.2}$$

the term $\frac{\mu_0}{V_{aa}}^{\gamma}$ is extracted from the UMEM procedure.

Eq.2.1 and eq.2.2 can be derived in terms of physical parameters following the works by (Estrada et al., 2008a) and (Vissenberg and Matters, 1998). The model developed by (Vissenberg and Matters, 1998) derived the following expression

of the field effect mobility considering the variable range hopping(VRH) mechanism of carries between localized states.

$$\mu_{FET} = \frac{\sigma_0}{q}\left(\frac{\pi\left(\frac{T_0}{T}\right)^3}{(2\alpha_0)^3 B_C \gamma\left(1-\frac{T}{T_0}\right)\gamma\left(1+\frac{T}{T_0}\right)}\right)^{\frac{T_0}{T}} \ldots \qquad (2.3)$$
$$\ldots \frac{(C_i)^{\left(2\frac{T_0}{T}-2\right)}}{(2k_b T_0 \epsilon_s)^{\frac{T_0}{T}-1}} (V_{GS})^{2\frac{T_0}{T}-2}$$

where σ_0 is a fit parameter, q is the electric charge , T_0 is the characteristic temperature of the localized states, α_0 corresponds to the effective overlap describing hopping, B_C is around 2.8. C_i, ϵs and k_b are the dielectric capacitance per unit area, the dielectric constant of the dielectric layer and the Boltzmann's constant respectively. The flat band voltage (V_{FB}), defines the onset of accumulation, and in OTFTs can be identified with the threshold voltage, V_T.

The expression of the μ_{FET} model was obtained from

$$\mu_{FET} = \frac{L}{W}\frac{1}{C_i V_{DS}}\frac{\partial I_{DS}}{\partial V_{GS}} \qquad (2.4)$$

The drain current model was calculated from:

$$I_{DS} = \frac{W}{L} V_{DS} \int_0^t dx \sigma[\delta(x), T] \qquad (2.5)$$

being t the channel thickness.

The work presented by (Vissenberg and Matters, 1998) shows

the calculation of the conductivity ($\sigma[\delta(x), T]$), where $\delta(x)$ represents the carrier occupation for a given Fermi level. The mobility model shown in eq.2.3 depends on the characteristic temperature T_0 of the exponential DOS described as

$$g_d(E) = g_{d0} exp(-\frac{E}{k_b T_0}) \tag{2.6}$$

being σ_0 and α_0 fitting parameters.

The temperature characteristic (T_0) is calculated from the γ model as

$$\gamma = 2(\frac{T_0}{T} - 1) \tag{2.7}$$

where T is the operation temperature of the OTFT under study.The γ parameter should indicate the quality of the device technology. Following (Estrada et al., 2005), $\gamma > 0$ indicates that the behaviour is typical of amorphous and nanocrystalline devices and is related to the trap conduction mechanism.

In order to obtain an analytical expression, the localized charge density in the organic semiconductor layer was considered to be much larger than the free charge density. The resulting expression of the drain current current in the above threshold regime is

$$I_{DS} = \beta(T, T_0) C_i \frac{W}{L} \frac{T}{2T_0} ... \tag{2.8}$$
$$...[(V_{GS} - V_{FB}) \frac{2T_0}{T} - (V_{GS} - V_{DS} - V_{FB}) \frac{2T_0}{T}],$$

where

$$\beta(T,T_0) = \frac{\sigma_0}{[B_c(2\alpha_0)^3]\frac{T_0}{T}}\left(\frac{k_bT}{(1-\frac{T}{T_0})}\right)... \quad (2.9)$$
$$...\left[\frac{sin(\frac{\pi T}{T_0})}{2k_bT_0}\right]\frac{T_0}{T}\frac{(C_i)^{\frac{2T_0}{T}-2}}{(\epsilon_s)^{\frac{T_0}{T}-1}}$$

The expression of μ_{FET} (eq.2.3) is obtained by applying eq.2.4 to the expression of current in eq.2.8.

Eq.2.8 and eq.2.9 has the same form as the expression of the drain current derived by (Shur and Hack, 1984) for a-Si:H TFTs

$$I_{DS} = P(T,T_0)C_i\frac{W}{L}\frac{T}{2T_0}... \quad (2.10)$$
$$...[(V_{GS}-V_{FB})^{\frac{2T_0}{T}} - (V_{GS}-V_{FB}) - V_{DS})^{\frac{2T_0}{T}}]$$

where

$$P(T,T_0) = P'(T,T_0)\frac{(C_i)^{\frac{2T_0}{T}-2}}{(\epsilon_s)^{\frac{T_0}{T}-1}} \quad (2.11)$$

and

$$P'(T,T_0) = \frac{qk_bTN_Vexp^{-\frac{E_{Fo}-E_V}{k_bT}}}{[\pi qk_bg_{d0}exp^{-\frac{E_{Fo}-E_V}{k_bT_0}}\frac{T_0}{T}} ... \\ ...[\frac{sin(\frac{\pi T}{T_0})}{2k_bT_0}]\frac{T_0}{T} \tag{2.12}$$

being E_{Fo} and E_V the Fermi level and the valence band energy respectively.Therefore, we can make equivalences between parameters in eq.2.8 and eq.2.9 and those in eq.2.10, eq.2.11 and eq.2.12. Equating eq.2.8 and eq.2.10 and replacing $\beta T, T_0$ for $P(T,T_0)$, the drain current model when $V_{DS} << V_{GS} - V_{FB}$ is

$$I_{DS} = \frac{W}{L}C_i\mu_{FET}(V_{GS}-V_{FB})V_{DS} \tag{2.13}$$

and the μ_{FET} is modeled as

$$\mu_{FET} = P'(T,T_0)\frac{(C_i)\frac{2T_0}{T}^{-2}}{(\epsilon_s)\frac{T_0}{T}^{-1}}(V_{GS}-V_{FB})\frac{2T_0}{T}^{-2} \tag{2.14}$$

The expression of μ_{FET} (eq.2.14) has the same form of $(V_{GS} - V_{FB})$ dependence as eq.2.3. By equating both equations we can write the μ_{FET} parameters in eq.2.3 in terms of the physical parameters appearing in the expression of eq.2.14.

$$P'(T,T_0)\frac{(C_i)\,\dfrac{2T_0}{T}^{-2}}{(\epsilon_S)\,\dfrac{2T_0}{T}^{-2}} = \frac{\mu_0}{Vaa^{\gamma}} \tag{2.15}$$

In OTFTs, $\mu_0 = 1cm^2/V.s$.

The external voltage applied along drain and source is calculated as

$$V_{DS} = V_{ds} + I_{DS}R \tag{2.16}$$

being V_{ds} and R the voltage applied to the channel and R the series resistance.

Taking into account the effect of the voltage drop at the series resistance up to first order, the general continuous analytical expression for drain current is modeled as

$$I_{DS} = \frac{-WC_i\mu_{FET}(V_{GS}-V_T)}{L(1+R\frac{W}{L}C_i\mu_{FET}(V_{GS}-V_T))}... \tag{2.17}$$

$$...\frac{V_{DS}(1+\lambda V_{DS})}{(1+(\frac{V_{DS}}{V_{DSsat}})^m)^{\frac{1}{m}}} + I_0$$

where L and W are channel length and channel width respectively. C_i is the insulator capacitance, R is series resistance and it is extracted as in (Cerdeira et al., 2016), m is a fitting parameter related to the sharpness of the knee region. I_0 is the

leakage current.The channel length modulation dependence with the drain source voltage (V_{DS}) is given by λ parameter.

To extract the key parameters in the above threshold regime, we calculate the integral function for the current in OTFTs in linear regime (eq.2.19) from the integral function $H(V_{GS})$ (eq.2.18) shown in (Estrada et al., 2005) and (Kim et al., 2013).

$$H(V_{GS}) = \frac{\int_0^{V_{GS}} I_{DS}(X)dx}{I_{DS}(V_{GS})} \tag{2.18}$$

$$H_1(V_{GS}) = \frac{1}{2+\gamma}(V_{GS} - V_T) \tag{2.19}$$

Applying eq.2.19 to the experimental transfer characteristics at low drain-source voltage, and carrying out linear regression of resulting values, we extract V_T from the intercept and γ from the slope . We obtain the Ss slope from $(I_{DS})^{\frac{1}{1+\gamma}}$ vs $(V_{GS} - V_T)$ and the V_{aa} parameter is extracted as:

$$V_{aa} = [\frac{(\frac{W}{L})\mu_0 C_i V_{DS}}{Ss^{1+\gamma}}]^{1+\gamma} \tag{2.20}$$

The parameter α controls the saturation voltage. The saturation voltage is given by:

$$V_{D_{Sat}} = \alpha(V_{GS} - V_T) \tag{2.21}$$

To calculate the α parameter it is necessary to calculate the

S_{sat} slope from $I_{DS_{sat}}^{\frac{1}{1+\gamma}}$ vs $(V_{GS} - V_T)$. The parameter α in saturation regime is extracted by

$$\alpha = \frac{S_{sat}^{2+\gamma} V_{aa}^{\gamma} \sqrt{2}}{(\frac{W}{L})\mu_0 C_i} \tag{2.22}$$

In the subthreshold regime, the drain current is modeled as (Kim et al., 2013):

$$I_{Dsb} = I_{DS_0} e^{\frac{2.3(V_{GS} - V_T)}{S}} \tag{2.23}$$

where S is the subthreshold swing, and is extracted as:

$$S = \frac{2.3}{Slope(I_{Dsb})} \tag{2.24}$$

I_{DS_0} corresponds to the current when $V_{GS} = 0V$.

The non-linear resistance is applied when the output characteristics are deformed at low V_{DS} by effects of the non-ohmic contact. The non-linear resistance is modeled by

$$R_C = R_{CO} e^{-\eta V_{DS}} = [\frac{nkT}{q} ... \\ ...(\frac{\frac{log(I_{DS}(V_{GS_{max}}))}{I_{do}}}{I_{DS}(V_{GS_{max}}}))] e^{\frac{-qV_{DS}}{nkT}} \tag{2.25}$$

$R_{CO} = 0$ when the non-linear contact is not present. To calculate the parameters n and I_{do}, it is necessary to plot $log(I_{DS}) vs V_{D1}$.

V_{D1} is the drain voltage where the non-ohmic phenomenon is present. The slope and the intercept of the curve plotted are calculated and these are rename as S_{diode} and Int_{diode} respectively.

The parameter n is calculated following

$$n = \frac{log(e)}{S_{diode}\frac{kT}{q}} \tag{2.26}$$

and the parameter I_{do} as

$$I_{do} = 10^{Int_{diode}} \tag{2.27}$$

Having all the parameters extracted, we use a unified expression of the drain current, which tends to eq.2.23 in subthreshold and to eq.3.4 above threshold (Kim et al., 2013). The total drain current is modeled as:

$$I_{DS_T} = |I_{DS}|[\frac{1 + tanh(V_{GS} - (V_T + DV)Q)}{2}]... \tag{2.28}$$
$$... + |I_{Dsb} + I_0|[\frac{1 - tanh(V_{GS} - (V_T + DV)Q)}{2}]$$

Q is a fit parameter and the leakage current(I_0) is the minimum current value of the experimental data. DV is extracted as:

$$DV = (V_{aa}^{\gamma} I_{DS_0} \frac{L}{WC_i V_D})^{\frac{1}{1+\gamma}} \tag{2.29}$$

The activation energy is given by:

$$E_A = T_0 kb \tag{2.30}$$

where kb is the Boltzmann constant.

The maximum trap density (g_{d0}) is calculated following (Hernandez-Barrios et al., 2018) and it is apply to calculate an estimate value to g_{d0} in OTFTs.

$$g_{d0} = \frac{N_C \frac{2}{\sqrt{\pi}}((\int_0^{\infty} \frac{\sqrt{x}}{1+e^{x-\frac{\varphi_s-\varphi_f}{\varphi_t}}} dx)}{(kbT_T)((\int_0^1 \frac{1}{1+Z^{\frac{T_T}{T}}} dz.e^{\frac{\varphi_f}{kbT_0}})} ... \tag{2.31}$$

$$... \frac{-(\int 0^{\infty} \frac{\sqrt{x}}{1+e^x} dx.e^{\frac{-\varphi_f}{kbT_0}}))}{-(\int 0^{\frac{\varphi_f-\varphi_s}{e^{\varphi_{TT}}}} \frac{1}{1+Z^{\frac{T_T}{T}}} dz.e^{\frac{\varphi_f}{kbT_T}}))}$$

where, φ_f is the fermi level potential, φ_s is the surface potential, φ_t is the thermal potential and φ_{TT} is the characteristic potential. N_C is the density of the states in the equivalent conduction band in OTFTs. $T_T = 2T_0 - T$. The eq.2.31 is used for IGZO devices, and in this case, it is used to calculate an estimated g_{d0} in OTFTs.

The density of interface states(D_{it}) is calculated from S and is given by:

$$D_{it} = \frac{\frac{SqC_i}{kbTln(10)} - C_i - C_D}{q} \tag{2.32}$$

where C_D is the depletion capacitance of the organic film layer calculated as (Castro-Carranza et al., 2014).

Keeping the parameters obtained through UMEM procedure, the gate capacitance is calculated following the procedure explained in the chapter 1. In this case, the total gate charge model in accumulation regime is given by

$$Q_{CH} = \frac{-WC_i^2}{I_{DS}}\mu_{FET}\frac{(V_{GTe} - V_{DSe})^{3+\gamma} - V_{GTe}^{3+\gamma}}{3+\gamma} \tag{2.33}$$

where V_{GTe} is the effective gate voltage overdrive and it is used to model the transition of the non linearised expression of the current between the subthreshold and the accumulation regimes (Chapter 1,(Cortes-Ordonez et al., 2019)). V_{DSe} is the effective drain voltage,(a continuous function tending to V_{DS} in the linear regime and to V_{DSat} in saturation).

The unified expression of the gate capacitance is explained in (Chapter 1 ,(Cortes-Ordonez et al., 2019)) and it is given by:

$$C_{TOT} = [|C_{EQ}|\frac{1 - tanh(\beta)}{2}] + [|C_{GG}|\frac{1 + tanh(\beta)}{2}] \tag{2.34}$$

C_{EQ} and C_{GG} correspond to the depletion and accumulation capacitance, respectively. $\beta = (V_{GT} + \Delta V_T)Q2$, being ΔV_T a correction of the threshold voltage for capacitance in $C - V$

measurements. $Q2$ corresponds to a transition parameter and has units of V^{-1} . The function *Tanh* provides a smooth transition between regimes (Cortes-Ordonez et al., 2019). C_{GG} is calculated from the Q_{CH} derivative respect to V_{GS}.

Applying the eq.2.33 is calculated the gate charge as,

$$Q_G = -Q_{CH} \tag{2.35}$$

2.2 Parameter extraction from I-V characteristics

In the first manufacturing technology, we performed measurements on polymeric p-type based in SP500 polymer OTFTs manufactured in CEA-Liten(Grenoble- France). The OTFTs under study were top gate bottom contact multifingers with $L \cong 20\ \mu$m and $W \cong 2000\ \mu$m. The total channel length of the transistor consists of 13 parallel fingers with $W_F \cong 154\ \mu$m. The dielectric thickness is 700 nm and the relative permittivity is close to 2. The thickness of the organic semiconductor layer(the active layer of the OTFT) is 40 nm and the estimated relative permittivity is 3.

The fig.2.2 shows the experimental and modeled $I_{DS} - V_{GS}$ characteristics at $V_{DS} = 1V$(linear regime), and fig.2.3 at $V_{DS} = 20V$(saturation regime) in both linear and logarithm scale .A reasonably good agreement between the experimental data and the I_{DS} model is observed, at least for V_{GS} lower than $25V$. I_{DS} increases with temperature due to the field effect mobility increase caused by a carriers increase (Kim et al.,

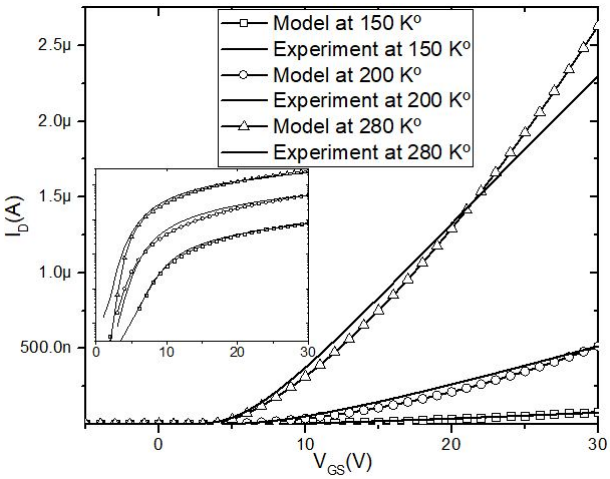

FIGURE 2.2: Modeled and experimental drain to source current(I_{DS}) as a function of V_{GS} at $V_{DS} = 1V$ in linear and logarithmic scales

2013). A good accuracy between the experimental data and the I_{DS} model is presented at logarithm scale in the subthreshold regime in both $V_{DS} = 1V$ and $V_{DS} = 20V$.

Fig.2.4, fig.2.5 and fig.2.6 show a good agreement between experimental data and the I_D modelled in the output characteristic at different V_G changing the temperature from 150K up to 300K . We can observe also that at low temperatures the I_D model is accurate enough, and it predicts the temperature behaviour very well at different V_D .

In tab.2.1, we can see the values of the extracted parameters. As seen in fig.2.7, the mobility increases with the temperature within the targeted low temperature range(150K - 300K). As explained above, we associate this phenomenon to the fact

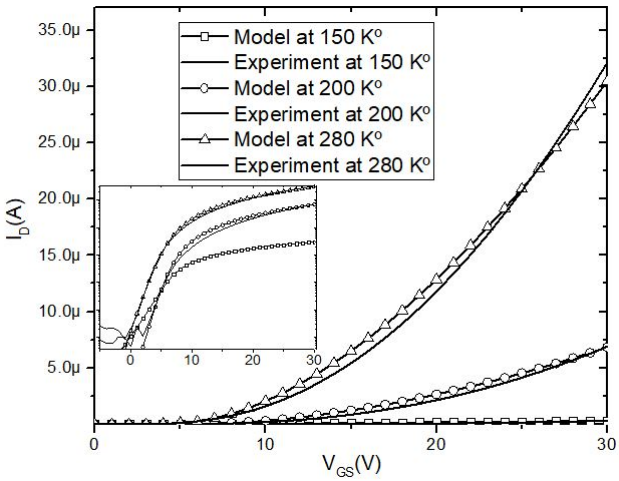

FIGURE 2.3: Modeled and experimental drain to source current(I_{DS}) as a function of V_{GS} at $V_{DS} = 20V$ in linear and logarithmic scales

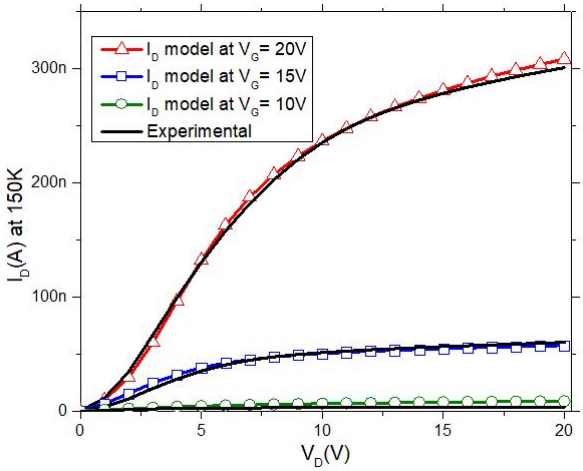

FIGURE 2.4: Output characteristics in different V_G at 150K

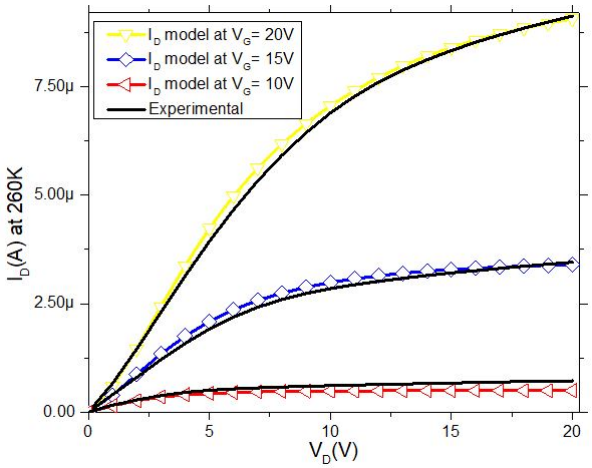

FIGURE 2.5: Output characteristics in different V_G at 260K

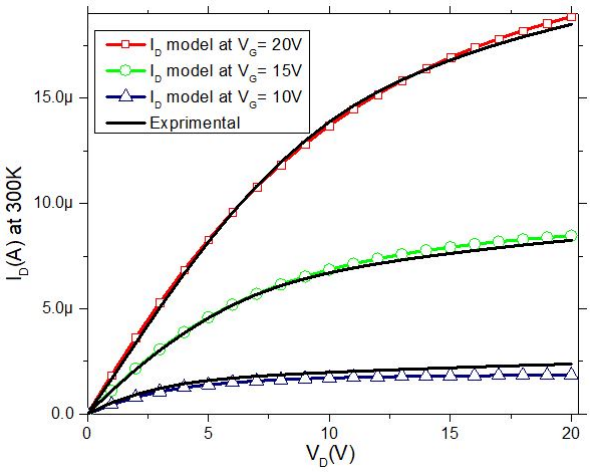

FIGURE 2.6: Output characteristics in different V_G at 300K

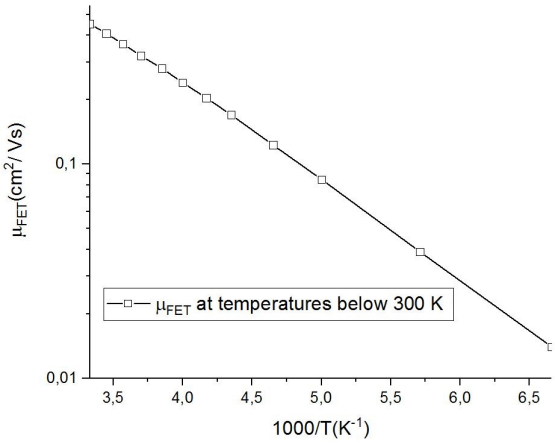

FIGURE 2.7: μ_{FET} vs Temperature from 150K up to 300K

that mobile carrier density increases with increasing temperature. The fig.2.8 shows the dependence of γ for this technology. Usually, γ in OTFTs ranges from 0 to 1, being 0 the value of a crystalline devices (Kim et al., 2013). We observe that γ decreases with increasing temperature, indicating a more crystalline like behavior. If γ is nearly to 0 as in crystalline devices, the generated charge is free.

Overall, the S parameter increases with increasing temperature (fig.2.9). The density of states (DOS) at the interface increases very lightly with increasing the temperature (values shown in fig.2.10 and tab.2.1 as D_{it}).S depends monotonically on the interface trap density, and its increase with increasing the temperature is mostly due to the fact that the subthreshold current in mostly due to diffusion, which increases with temperature. The values of g_{d0} are indicated in tab.2.1.

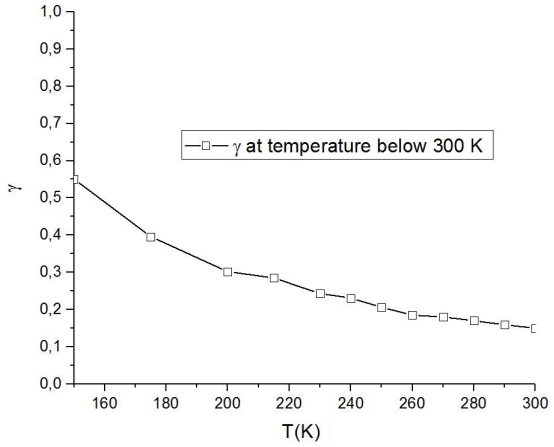

FIGURE 2.8: γ vs Temperature from 150K up to 300K

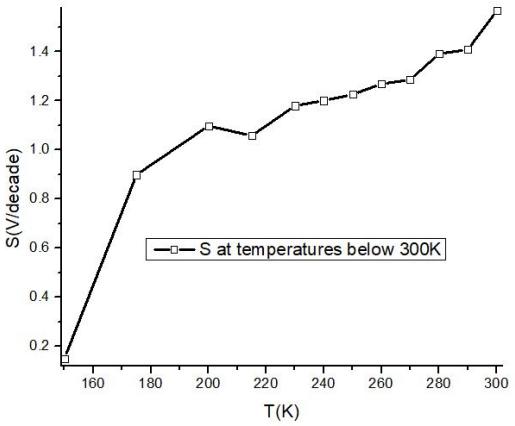

FIGURE 2.9: S vs Temperature from 150K up to 300K

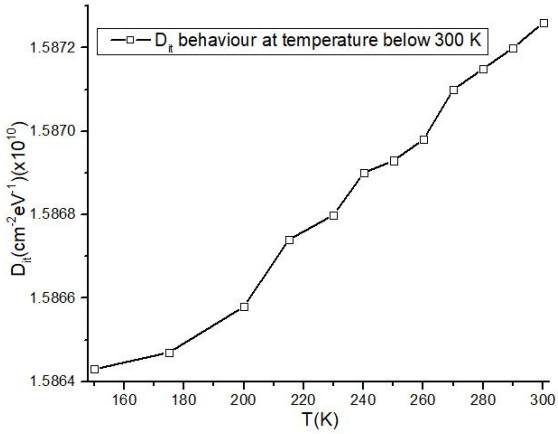

FIGURE 2.10: D_{it} vs Temperature from 150K up to 300K

The temperature dependence of T_0 (DOS characteristic temperature) is shown in the fig.2.11. T_0 usually is constant, in this case we observed that it increases almost linearly with temperature, this effect seems to be the same as for the increase of the characteristic energy of the tail DOS with temperature observed in a-Si:H materials (Cody et al., 1981), which was attributed to the temperature dependence of the dynamic phonon disorder.

Parameter V_{aa} is related to the mobility and it is extracted using eq.2.20. We can observe in fig.2.12 that the V_{aa} increases with the temperature. Finally, as seen in fig.2.13, to analyze the behavior of V_T, we used the expression $VT(T) - V_T(300K)$;it is shown that it decreases with increasing temperatures, which can be related to the change of the trapped charge density.

The maximum trap density (fig.2.14) decreases with increasing temperature.

TABLE 2.1: Extracted model parameters from $I-V$ measurements. They have been used for modeling of OTFTs in the range from 150K to 300K.

	150K	**215K**	**260K**	**280K**	**300K**
γ	0.551	0285	0.185	0.17	0.15
$S[V/decade]$	0.149	1.058	1.269	1.392	1.567
$\mu_{FET}[cm^2/Vs]$	0.14	0.123	0.28	0.364	0.452
$V_T[V]$	6.05	5.28	4.76	4.45	4.25
$T_0[K]$	191	246	284	304	322
$g_{do}[cm^{-3}][10^{18}]$	3.493	1.913	1.444	1.331	1.227
$D_{it}[\frac{cm^{-2}}{eV}]$	=	=	$1.5968x10^{10}$	=	=

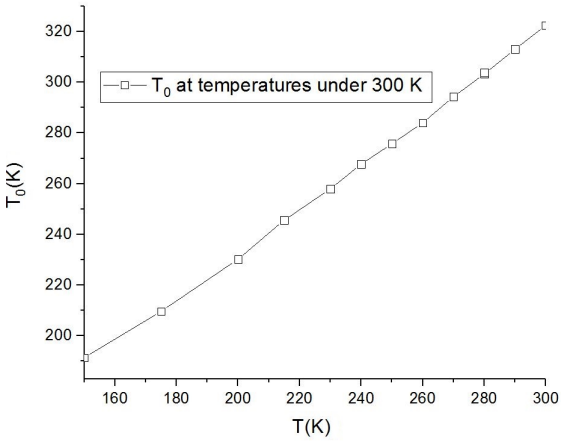

FIGURE 2.11: T_0 vs Temperature from 150K up to 300K

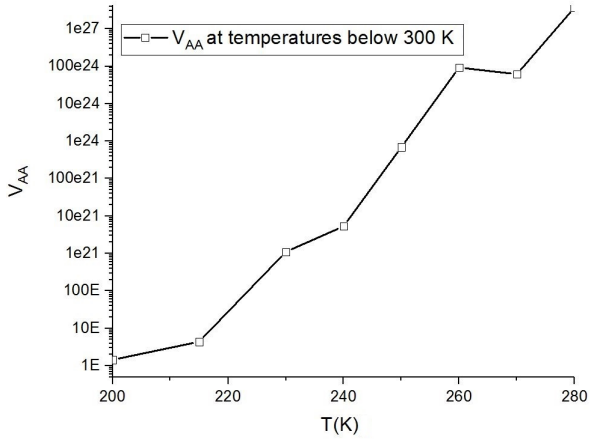

FIGURE 2.12: V_{aa} vs Temperature from 150K up to 300K

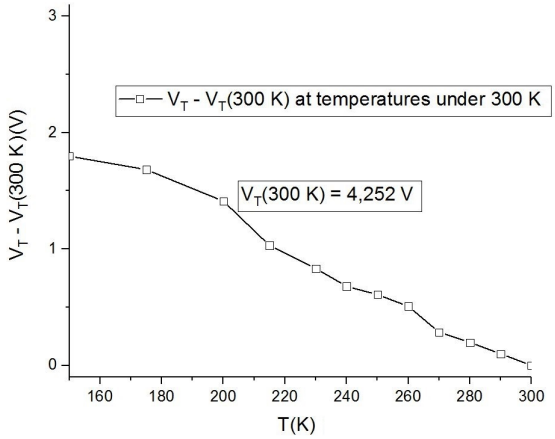

FIGURE 2.13: V_T vs Temperature from 150K up to 300K

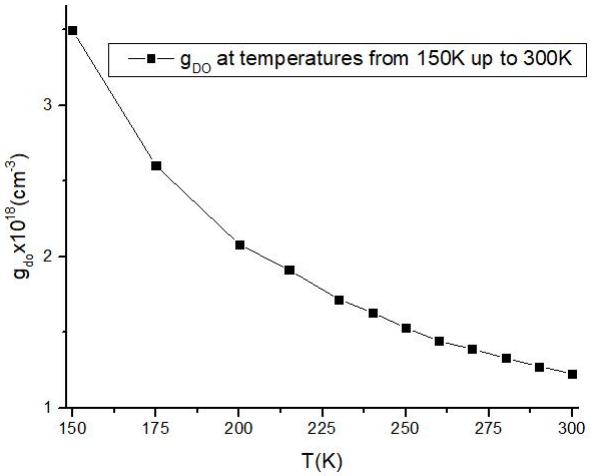

FIGURE 2.14: G_{do} vs Temperature from 150K up to 300K

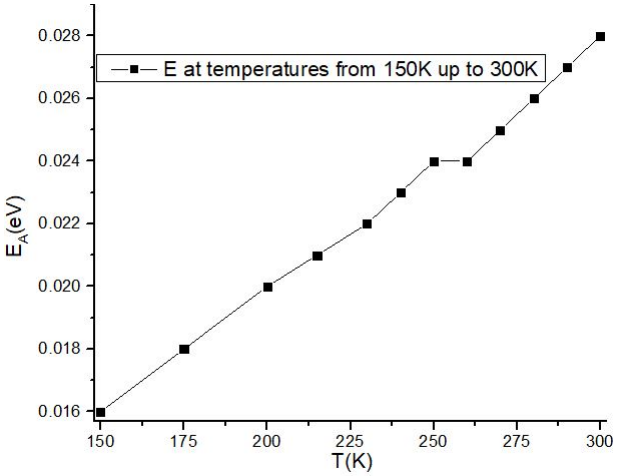

FIGURE 2.15: E_A vs Temperature from 150K up to 300K

On the other hand, in the fig.2.15 the activation energy increasing with temperature. As T_0 increases almost linearly with temperature. The E_A is directly proportional to this temperature. The maximum value of E_A reached at environment temperature (300K) is around $0.30eV$.

2.3 Analysis of the temperature dependence in the gate capacitance

Analyzing the same device for which we performed the parameter extraction, we studied the temperature dependence of the gate capacitance. The capacitance measurements were done using the Agilent 4284A LCR Meter. To carry out the measurements at different temperature of the capacitance in OTFTs, we used the cryostat station with temperature ranging from 200K up to 280K.

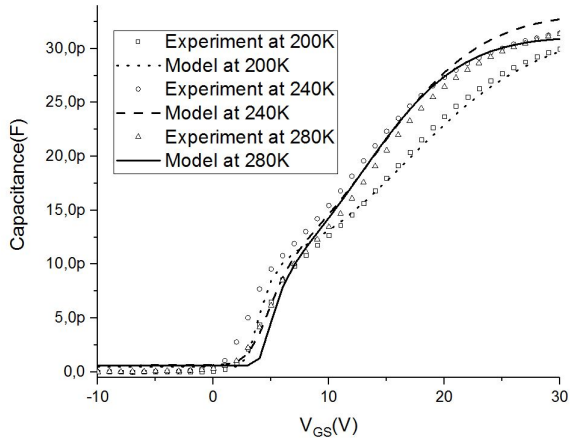

FIGURE 2.16: Capacitance vs Frequency at temperatures from 200K up to 280K

In fig.2.16, we show the total gate capacitance calculated from eq.2.34. We can see in fig.2.16 that the temperature affects the capacitance at low V_{GS}, i.e the temperature affects the depletion capacitance and the capacitance values at the transition between the depletion and accumulation regimes. In the strong accumulation regime, the gate capacitance is the same as the dielectric capacitance and the temperature does not affects its value. Our capacitance model reproduces well the experimental C-V characteristics.

2.4 Review

We analyzed the temperature dependencies in the I-V and C-V characteristics for polymeric OTFTs in the temperature range from 150K to 300K. We adapted and applied the unified model and parameter extraction method (UMEM) specific for OTFTs, obtaining a reasonable good agreement between the modeled and the experimental I-V characteristics within the targeted temperature range.

For the output characteristics, we obtained a good agreement between the modeled and experimental I-V data. At low V_{DS} at low temperature, we observed that the non-linear R_C affects the current. It is to highlight that our model reproduces very well this physical phenomenon at low temperatures as seen in fig.2.4

Furthermore, the temperature dependence of model parameters has been studied in detail, observing that both, the threshold voltage and the subthreshold swing increase with increasing temperature, whereas the characteristic temperature and the field effect mobility increase as temperature is risen.

The γ parameter decreases with increasing temperature,as well as the field effect mobility, due to the increase of the mobility charge density. As a result, the performance of the OTFT becomes higher with rising temperatures.

D_{it} is almost constant, the value of this parameter variate between $1.5944x10^{10}$ and $1.5972x10^{10}$. The average value of $D_{it} = 1.5968x10^{10}$.

As the material of the semiconductor is unknown, the calculation of g_{do} and E_A considering the electrical behaviour is very important. The $g_{do} = 1.227cm^{-3}$ at 300K, being this density a good calculated value for OTFTs devices ((Estrada et al., 2008a).

Also, we used the extracted parameters from I-V characteristics to analyze the temperature and frequency behavior in the capacitance. We demonstrated theoretically and experimentally that the temperature does not affect the capacitance in accumulation regime but it affects the transition from depletion to accumulation. We obtain good agreement with experimental results.

UNIVERSITAT ROVIRA I VIRGILI
PHYSICAL BEHAVIOUR ANALYSIS AND COMPACT TEMPERATURE-DEPENDENT MODELING IN ORGANIC AND IGZO TFTS
Harold Cortes Ordoñez

Chapter 3

Unified compact modeling for OTFTs at different temperatures

In this chapter, we analyze the OTFT bahavior from low to high temperatures, in particular from 200K up to 350K. After extracting parameters following UMEM procedure described and adapted to OTFTs in Chapter 2, we apply our OTFT model reproduce the experimental I-V characteristics from 200K to 300K. Besides, we study and provide physical explanations of the behaviour of the key parameters from 200K to 350K, in particular mobility, threshold voltage, characteristic temperature, subthreshold swing, saturation parameter, and density of states.

3.1 Modeling and calculation of physical parameters

To model the drain current in OTFTs, we used the UMEM procedure adapted to OTFTs. It is based on a power law mobility model (Estrada et al., 2005) explained in the Chapter 2 as:

$$\mu_{FET} = \mu_0[\frac{(V_{GS} - VT)}{V_{aa}}]^{\gamma} = \mu_{FET_0}(V_{GS} - V_T)^{\gamma} \tag{3.1}$$

μ_0 corresponds to the effective band mobility of the OTFT material under analysis. V_T is the threshold voltage. The V_{aa} parameter controls the μ_{FET} (Kim et al., 2013). As mentioned in the previous chapter, the γ parameter is related to the density of states (DOS) and indicates the deviation from the crystalline mobility behavior. This parameter is calculated as

$$\gamma = 2\frac{T_0}{T} - 2 \tag{3.2}$$

The UMEM procedure explained in previous chapters can be used to extract the key mobility parameters as V_T, S, V_{aa} and R_C through the integral function $H_1(V_{GS})$ for the current in OTFTs at linear regime(eq.3.3).

$$H_1(V_{GS}) = \frac{1}{2+\gamma}(V_{GS} - V_T) \tag{3.3}$$

The model of the drain current in both linear and saturation regimes (above threshold) is given by:

$$I_{DS} = \frac{-WC_i\mu_{FET}(V_{GS}-V_T)}{L(1+R\frac{W}{L}C_i\mu_{FET}(V_{GS}-V_T))}... \\ ...\frac{V_{DS}(1+\lambda V_{DS})}{(1+(\frac{V_{DS}}{V_{DSsat}})^m)^{\frac{1}{m}}} + I_0 \tag{3.4}$$

where L and W are channel length and channel width respectively. C_i is the insulator capacitance, R is series resistance and it is extracted as in (Cerdeira et al., 2016), m is a fitting parameter related to the sharpness of the knee region. I_0 is the leakage current.The channel length modulation dependence with the drain source voltage (V_{DS}) is given by λ parameter.

The rest of parameters are calculated following the procedure explained in the chapter 2.

3.2 Results

We performed measurements on polymeric p-type OTFTs also manufactured in CEA-Liten(Grenoble- France). The OTFTs were top gate bottom contact with $L = 80$ μm and $W = 1000$ μm. The dielectric thickness is 900 nm and the relative permittivity is close to 3. The thickness of the organic layer(fluorinated) is 40 nm.

fig.3.1 shows the experimental and modeled $I_{DS} - V_{GS}$ characteristics at $V_{DS} = 1V$(linear regime), and fig.3.2 at $V_{GS} = 20V$(log regime).A reasonably good agreement between the

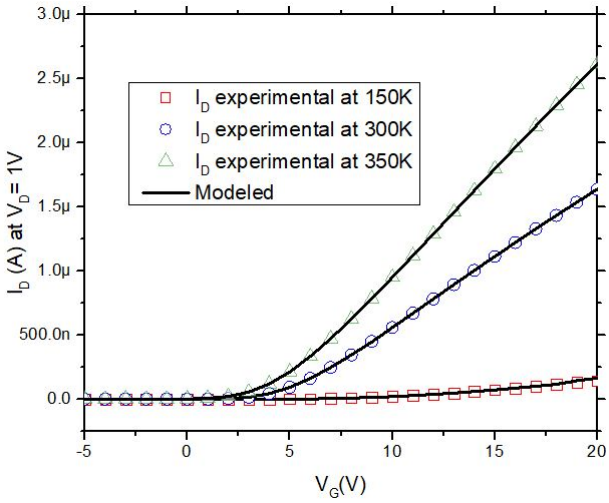

FIGURE 3.1: Modeled and experimental drain to source current(I_{DS}) as a function of V_{GS} in linear regime

experimental data and the I_{DS} model is observed. I_{DS} increases with temperature due to the field effect mobility increase caused by a carriers increase (Estrada et al., 2005).

The fig.3.3, fig.3.4 and fig.3.5 shows the I_D as function of V_D at different temperatures from 200K to 350K. As seen for manufacturing technology addressed in the last chapter, the I_D model reproduces very well the transfer and output characteristics at different temperatures. For temperatures higher than 300K, the model yields a very good agreement with the experimental data.

In table.3.1, we can see the values of the extracted parameters. As seen in fig.3.6, the mobility increases with the temperature. As explained above, we associate this phenomenon

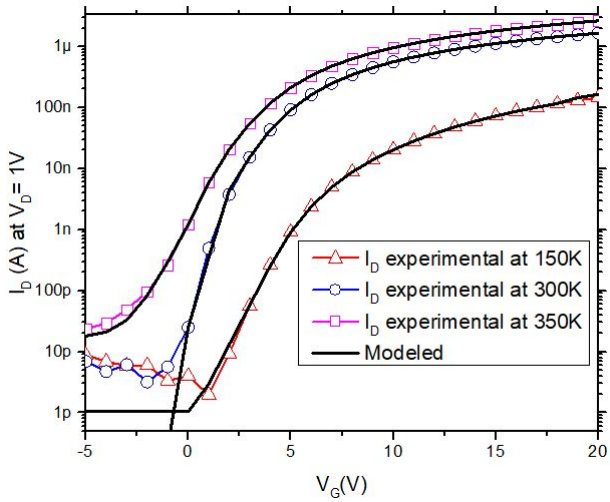

FIGURE 3.2: Modeled and experimental drain to source current(I_{DS}) as a function of V_{GS} in logarithm scale

to the fact that mobile carrier density increases with increasing temperature. The fig.3.7 shows the dependence of γ for this technology. Usually, γ in OTFTs ranges from 0 to 1, being 0 the value of a crystalline device (Kim et al., 2013). In this case, γ decreases with increasing temperature until 300K like in the technology analysed in the chapter 2. Also, we observed a saturation in this parameter, then γ increases with increasing the temperature after it get the 310K proximally.

The S parameter increases with increasing temperature until 300K(fig.3.8). The density of states (DOS) at the interface increases with increasing the temperature.S depends monotonically on the interface trap density, and its increase with increasing the temperature can be due to the displacement of the Fermi level through band edges where the trap density is

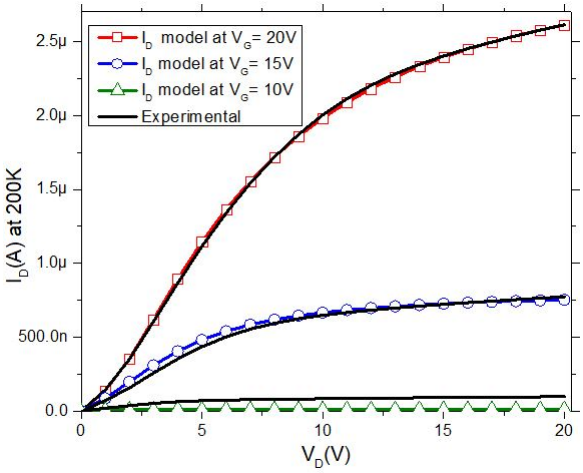

FIGURE 3.3: Modeled and experimental drain to source current(I_{DS}) as a function of V_{GS} in logarithm scale

higher (Estrada et al., 2008a). The temperature dependence of T_0 (DOS characteristic temperature) is shows in fig.3.9 T_0 is not constant. It increases with the temperature. It is due to the increase of the characteristic energy. The effect was also reported in a-Si:H TFTs and explained in (Cody et al., 1981).

Parameter E_A is related to the DOS and it is calculated using eq.2.16 in the last chapter. We can observe in fig.3.9 that the E_A increases with the temperature. Finally, as seen in fig.3.11, we analyze the behavior of V_T,it is shown that it decreases with increasing temperatures, which can be related to the change of the trapped charge density.

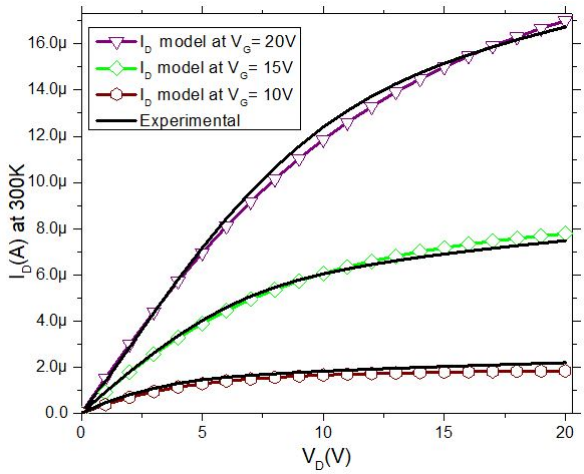

FIGURE 3.4: Modeled and experimental drain to source current(I_{DS}) as a function of V_{GS} in logarithm scale

3.3 Review

The temperature dependence analysis of the I-V characteristics of polymeric OTFT was performed from 150K to 350K. Applying the UMEM procedure adapted to OTFTs(as explained in Chapter 2) and adding the non-ohmic effect model proposed in the chapter 2, we obtained very good agreement between experimental and modeled I-V characteristics within the targeted temperature range in logarithmic and linear scales. Also, the non ohmic effect was reproduced very well at temperature 200K at low V_{DS}, as seen in chapter 2.

As seen in the results, the current increases with increasing the temperature due to the carrier density increases, which, in turn, causes an increase of μ_{FET} the temperature. Regarding the γ parameter, we can observed that it decreases with

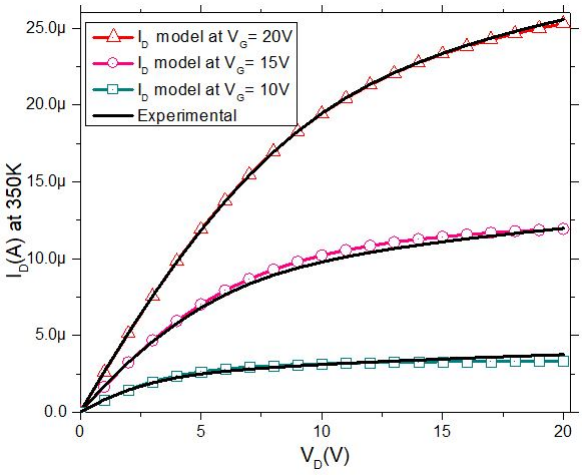

FIGURE 3.5: Modeled and experimental drain to source current(I_{DS}) as a function of V_{GS} in logarithm scale

increasing temperature. This parameter evolution indicates that at high temperature, the device behaviour approaches a quasi-crystalline regime.

Overall, subthreshold swing parameter (S) increases with increasing temperature. Above 330K we observed a change of trend due to the saturation of the trapped charge density. Other parameters such as, T_0 , V_T, E_A were analysed, and we observed a decrease of V_T with increasing the temperature, and an increase of T_0(and therefore E_A) as the temperature is raised from 200K to 350K. Physical explanations have been provided for these effects. In general our model reproduced quite well the transfer and output characteristics in the temperature range between 150K and 350K.

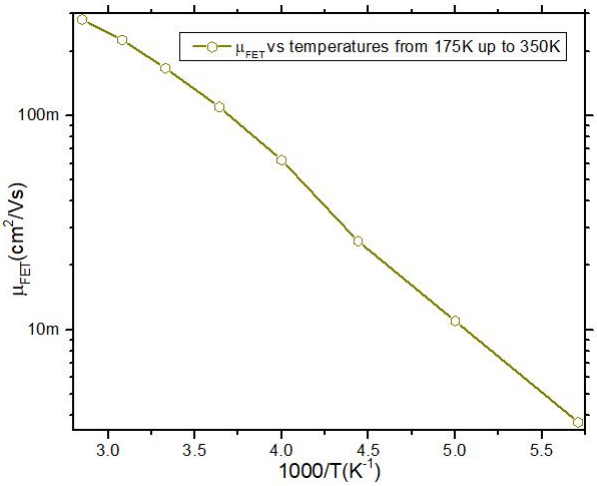

FIGURE 3.6: μ_{FET} vs Temperature from 150K up to 350K

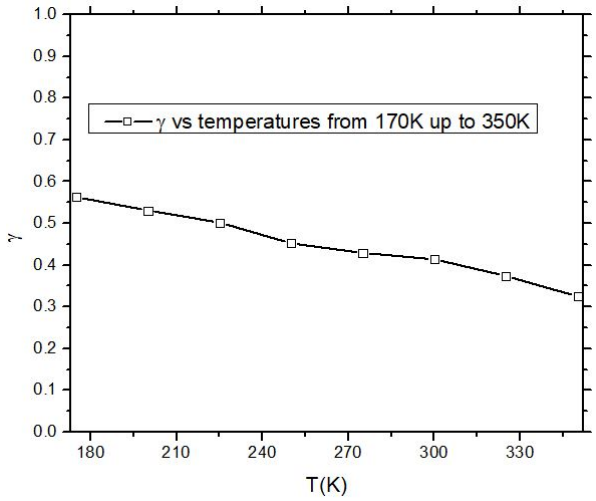

FIGURE 3.7: γ vs Temperature from 150K up to 350K

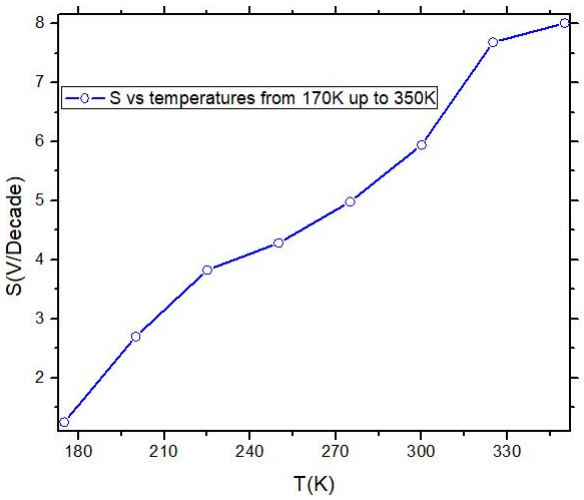

FIGURE 3.8: S vs Temperature from 150K up to 350K

TABLE 3.1: UMEM parameters extracted from $I-V$ measurements. They have been used for modeling of OTFTs in the range from 150K to 350K

$UMEM$	$175K$	$250K$	$300K$	$325K$	$350K$
γ	0.5636	0.452	0.0.414	0.374	0.325
$S[V/Decade]$	1.251	4.285	5.946	7.683	8.006
$\mu_{FET}[cm^2/Vs]$	0.0037	0.062	0.167	0.226	0.282
V_T	7.22	4.351	2.747	1.821	0.985
$E_A[eV]$	0.019	0.026	0.031	0.033	0.035
$T_0[K]$	224.26	306.5	362.1	385.77	406.87

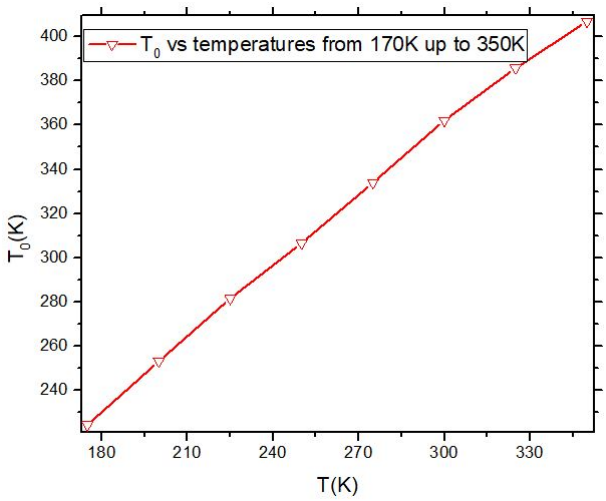

FIGURE 3.9: T_0 vs Temperature from 150K up to 350K

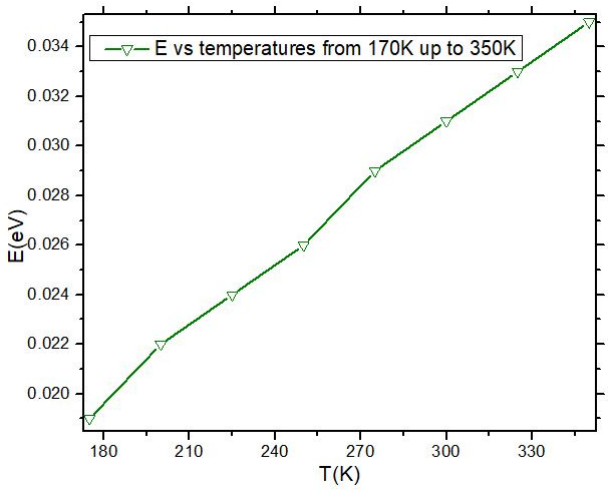

FIGURE 3.10: E_A vs Temperature from 150K up to 350K

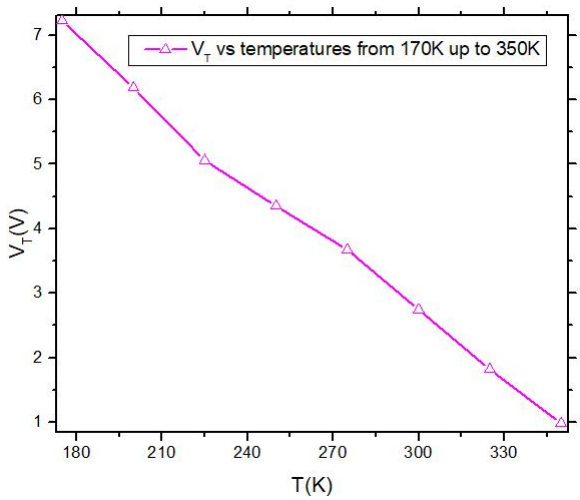

FIGURE 3.11: V_T vs Temperature from 150K up to 350K

Chapter 4

Parameter extraction and compact drain current model for IGZO transistor from 210K up to 370K

Since IGZO TFTs appeared in the technological market as a promising device for large area electronics, the research community has been interested in understanding their physical mechanisms, enhancing the performance of these devices and extending their applications (Zou et al., 2011) (Yabuta et al., 2006).

Several works analysing the temperature behavior of IGZO TFTs have been published. However, only a few parameters such as field-effect mobility or threshold voltage have been studied as a function of temperature (Lee et al., 2011) (Abe et al., 2014). Besides, no complete compact model for IGZO TFT has been validated from low to high temperatures,

which limits circuit design using these devices in applications with variable temperatures.

In this chapter, we study and discuss the temperature dependence of the key physical parameters of IGZO TFTs, and using the extracted values, and we extend our previous IGZO TFT compact model to the temperature range from 210K to 370K.

Our physically-based compact IGZO TFT model was described in (Hernandez-Barrios et al., 2018). It was developed by assuming a negligible density of deep states and an exponential density of tail states, and by considering both free and localized charges.The localized density of states at conduction band edge and the characteristic temperature of the density of states (DOS) are fundamental parameters in this model. It was shown (Hernandez-Barrios et al., 2018) (Moldovan et al., 2016) (Estrada et al., 2008a) that the so-called Unified Modelling and Extraction Method (UMEM) adapted to IGZO TFTs can be used to directly extract the physical parameters using this model from the I-V characteristics.

Using our model and direct extraction methods, we obtain the values of the key physical parameters of IGZO TFTs from 210 K to 370 K. We analyzed and discussed the observed temperature behavior of these parameters, in particular the characteristic temperature, tail states density at the bottom edge of the conduction band, threshold voltage, mobility and subthreshold swing. We found that as temperature increases the

characteristic temperature of the DOS increases, therefore refuting the extended assumption that it is temperature independent. We provided an explanation for this effect.

Finally, using the extracted parameter values, we successfully applied our drain current model to reproduce both the transfer and output I-V characteristics of IGZO TFTs from 210K to 370K. The agreement with experimental data is very good from the subthreshold to the above threshold regimes, and from the linear to the saturation regimes

4.1 IGZO modeling and parameter extraction

The distribution of the acceptor-type localized states (g_a) present in the mobility band of the amorphous n-type inorganic TFT is calculated through the sum of the tail and deep states with E dependence as

$$g_a = g_{ato} exp^{-\frac{E_C - E}{kT_1}} - g_{ado} e(-\frac{E_C - E}{k_b T_2}) \tag{4.1}$$

being g_{ato} and g_{ado} the tail and deep acceptor densities extrapolated at $E_C = E$ respectively. E is rge conduction band energy, T_1 and T_2 are the characteristic temperatures of the tail and deep states respectively. k_b is the Boltzmann constant.

In the above threshold regime, the field effective mobility in amorphous TFTs is represented by the power law (Shur,

1984) (Engl, Dirks, and Meinerzhagen, 1983).

$$\mu_{FET} = \frac{\mu_0}{Vaa^{\gamma_a}}(V_{GS} - V_T)^{\gamma_a} \tag{4.2}$$

being V_T the threshold voltage, the parameters Vaa and γ_a defining the variation of the mobility with gate bias in the above threshold condition. The parameter μ_0 is equal to $1cm^2/Vs$ and it is used for dimensional purposes.

The λ parameter is related to the channel length modulation and this coefficient defines the non-ideal output curve at high V_{DS}.

The asymptotic current in the saturation regime (at very high drain voltage)can be calculated as $I_{as} = I_{sat}(1 + \lambda V_{DS})$, being I_{sat} the current when V_{DS} is equal to the saturation voltage. The I_{as} defines a higher current than the actual one, which gradually tends to the asymptotic current as V_{DS} becomes sufficiently high. The critical point of this approach is that the current I_{as} and the I_{DS} experimental current are distant from each other and this gives rise to an not accurate prediction of the low voltage output conductance (Turin et al., 2010).

To solve the problem presented in the last paragraph and following (Kim et al., 2013) report, the real drain current in the saturation regime is modeled as

$$I_{as1} = I_{Sat}[1 + \lambda(V_{DS} - V_{Sat})] \tag{4.3}$$

where the saturation voltage is calculated by $V_{Sat} = \alpha_S(V_{GS} - V_T)$ and α_S is the parameter that defines the saturation voltage. Calculating I_{as1} using eq.4.3 yields values closed the

measured I_{DS} and the prediction of the output conductance is very accurate. This method prevents unexpected overestimation of low V_{DS} conductance by reducing the contribution of the asymptotic term in the linear regime.

The effective drain-source voltage (V_{DSe}) function is used to smooth the transition between linear and saturation regimes and it is equal to V_{DS} when $V_{DS} \ll V_{sat}$ and equal to $V_{sat} \gg V_{sat}$.

$$V_{DSe} = V_{DS}[1+ \mid \frac{V_{DS}}{V_{sat}} \mid^{m}]^{-\frac{1}{m}} \tag{4.4}$$

being m a fitting parameter in the sharpness of the knee region in the I_{DS} current between linear and saturation regions.

In our model, the drain current in the above threshold regime has the same form as the current in organic TFTs (see Chapter 2 and Chapter 3). We added the corrected channel modulation term explained above. The I_{DS} in IGZO devices is modeled as

$$\begin{aligned} I_{DSab} = K\frac{\frac{\mid V_{GS}-V_T \mid^{1+\gamma_a}}{Vaa^{\gamma_a}}}{1+KR\frac{\mid V_{GS}-V_T \mid^{1+\gamma_a}}{Vaa^{\gamma_a}}}... \\ ...[\frac{V_{DS}[1+\lambda(\mid V_{DS} \mid -V_{DSe})]}{[1+ \mid \frac{V_{DS}}{\alpha_S(V_{GS}-V_T)} \mid^{m}]^{\frac{1}{m}}}] \end{aligned} \tag{4.5}$$

where $K = \frac{W}{L}\mu_0 C_i$, being W and L the width and length channel of the device under study respectively. R is the contact resistance and C_i is the gate capacitance per unit area.

In the subthreshold regime, the drain-source current is modeled as

$$I_{DSsb} = K\frac{(V_{GS} - V_{FB})^{1+\gamma_b}}{Vbb^{\gamma_b}}V_{DSe1} \tag{4.6}$$

being V_{FB} the flat band voltage and V_{DSe1} is a transition voltage and it is calculated as

$$V_{DSe1} = V_{DS}[1 + (\frac{V_{DS}}{\alpha(V_{GS} - V_{FB})})^m]^{-\frac{1}{m}} \tag{4.7}$$

The parameters V_{bb} and γ_b control the variation of the mobility with the gate bias in the subthreshold regime. γ_b depends on the temperature T and on the characteristic temperature of the deep states distribution (T_2) as shown in eq.4.1.

$$\gamma_b = 2(\frac{T_2}{T} - 1) \tag{4.8}$$

In the deep subthreshold regime the dominant transport mechanism is charge diffusion and, as a result, the drain current shows as exponential dependence with the gate voltage overdrive. The subthreshold current is modeled as

$$I_{DSdsb} = exp\frac{2.3[V_{GS} - (V_{FB} + V_1)]}{S_1} \tag{4.9}$$

the V_1 is a fitting voltage used to smooth the transition between I_{Ssb} and I_{DSdsb}. S_1 is the deep subthreshold slope of the experimental I_{DS} in the subthreshold regime. The extraction of this parameter is explained in the chapter 2.

To calculate the total subthreshold current it is necessary to use an expression accounting for the transition between both subthreshold regimes(the regime where the deep states dominate and the regime where the current is dominated by diffusion). In our model we use an interpolation function based on hyperbolic tangent functions.The subthreshold current I_{DSst} is modeled as

$$I_{DSst} = \mid I_{DSsb} \mid [\frac{1 - tanh[(V_{GS} - (V_{FB} + 1))Q_1]}{2}] + \mid I_{DSdsb} \mid [\frac{1 + tanh[(V_{GS} - (V_{FB} + 1))Q_1]}{2}] \tag{4.10}$$

where, the Q_1 parameter control the transition between both subthreshold regimes.

To obtain the full drain-source current model, it is necessary to use an expression which includes both the above subthreshold and the subthreshold currents as well as a leakage current (flow through the non-depleted portion of the IGZO film); this curren is called off-current (I_0). Considering the drain current expression in each regime, as well as interpolation functions based on hyperbolic tangents, the unified drain current expression is modeled as

$$I_{DS} = \pm[\mid I_0 \mid + I_{DSab}[\frac{1 - tanh[(V_{GS} - (V_T + V_0))Q_0]}{2}] + \mid I_{DSst} \mid [\frac{1 + tanh[(V_{GS} - (V_T + V_0))Q_0]}{2}]] \tag{4.11}$$

V_0 is used to sew the subthreshold and above threshold regimes.

Q_0 is the weight on the *tanh* function. It is important to highlight that the positive sign (+) in eq.4.11 correspond to n-channel TFTs and the negative sign (−) to p-channel devices.

The parameter extraction procedure that we use for this IGZO TFT model is based on the UMEM method described before. The key parameters are extracted by means of the integral function method applied separately to the above threshold and the subthreshold regimes In the above threshold regime, the integral function used is

$$H(V_{GS}) = \frac{\int_0^{V_{GS}} I_{DS}(x)dx}{I_{DS}(V_{GS})} = \frac{1}{2+\gamma_a}(V_{GS} - V_T) \qquad (4.12)$$

The parameter V_T, γ_a and α_S are extracted following (Moldovan et al., 2016). Once these parameters are extracted, the field effect mobility is calculated using eq.4.2. The upper limit is the maximum gate voltage used for the transfer characteristic in the linear regime measurements. When the device is biased up to high voltage values, the exact value of the upper limit is given by the V_{GS} where the maximum slope happens. Another form to extract the upper limit is using the maximum peak of the transconductance (g_m). In some experiments, the non ohmic effect appears at high V_{GS}. In this case, to model it and extract the non-ohmic contact effect parameters, we apply the model and extraction method described in Chapter 1 for OTFTs

In the subthreshold regime, the parameters Vbb and γ_b have temperature T_2 and g_{ado} dependences. The physical parameters T_2 and g_{ado} corresponding to the subthreshold regime

(deep states DOS) are calculated following (Moldovan et al., 2016). In subthreshold regime the integral function is defined as

$$H(V_{GS}) = \frac{\int_0^{V_{GS}} I_{DS}(x)dx}{I_{DS}(V_{GS})} = \frac{1}{2+\gamma_b}(V_{GS} - V_{FB}) \tag{4.13}$$

being V_{FB} calculated from the intercept, γ_b from the slope of the eq.4.13 integral function where its shows linear dependence.

The density of the deep states is calculated as

$$g_{F0} = g_{ado} exp^{-\frac{E_C - E_{F0}}{kT_2}} \tag{4.14}$$

where E_{F0} is the fermi level.

4.2 Model validation and parameter extraction

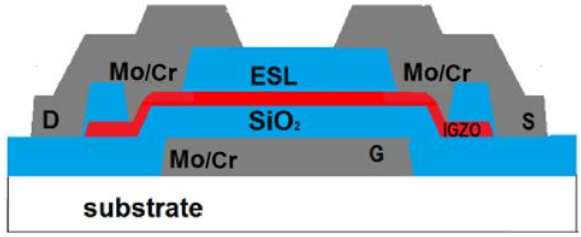

FIGURE 4.1: Cross section of the IGZO transistor under study

We performed measurements on an IGZO thin film transistor manufactured by TNO (The Netherlands). These transistors

have a top Etch Stop Layer (ESL) (fig.4.1). The device under study has $L = 20\mu m$, $W = 100\mu m$. The relative dielectric constant is $\epsilon_r = 4.7$, the insulator thickness is $t_i = 200nm$ and the thickness of the ESL is $t_d = 100nm$. We performed measurements of the $I - V$ characteristics at temperatures from 210K up to 370K using equipment available in IMEP-LAHC (Grenoble, France).

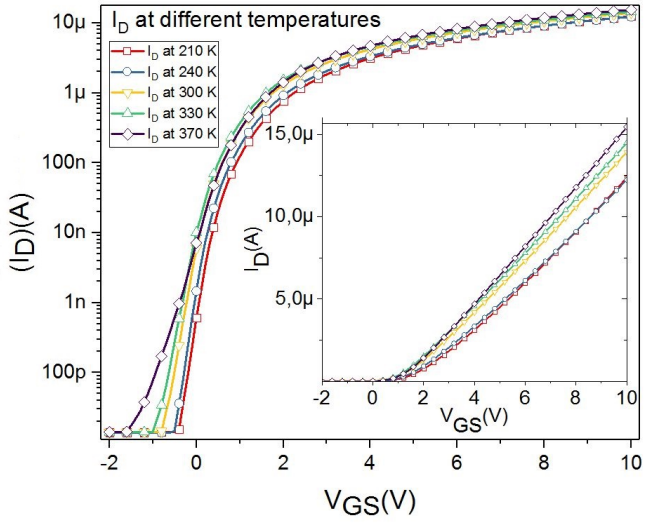

FIGURE 4.2: Experimetal and modeled I_D at different temperatures in linear and logarithm scale

As we can see in fig.4.2, the drain current ID increases with increasing temperature in all operating regimes.

We applied our extraction procedure to the I-V characteristics from 210 to 370 K. The γ parameter (fig.4.3) decreases with increasing temperature. This indicates that when the temperature increases, the device presents a more crystalline-like behavior. This is consistent with the Fermi level of the

TABLE 4.1: Extracted model parameters from $I-V$ measurements

	210K	**270K**	**300K**	**350K**	**370K**
γ	0.187	0.139	0.079	0.017	0.008
$\mu_{FET}(cm^2/Vs)$	15.57	16.67	17.58	20.174	21.29
$V_T(V)$	1.201	0.632	0.25	0.109	0.03
$S(V/Decade)$	0.196	0.211	0.234	0.265	0.291
$T_0(K)$	229.63	288.76	311.85	352.97	371.48
$E_A(eV)$	0.02	0.025	0.027	0.0305	0.032
$g_{ato}(cm^{-3})x10^{18}$	1.752	1.327	1.137	0.947	0.901
$D_{it}(cm^{-2}eV^{-1})$			$1.307x10^{11}$		

semiconductor moving toward the bottom of the conduction band and causing an increase in the ratio of free to localized carriers (Hernandez-Barrios et al., 2018).

μ_{FET} and μ_{FET_0} (fig.4.4 and fig.4.5 respectively) increase with temperature due to the increase of mobile carrier concentration (Cerdeira et al., 2016). As seen in fig.4.6,V_T decreases with increasing temperature, as observed in other TFT devices (Estrada et al., 2008b). In the case of IGZO TFTs, this can be explained by the increase of oxygen vacancies with increasing temperature, which in turns leads to the generation of free electrons. This phenomenon was observed in (Estrada et al., 2016) for high temperatures. We see in fig.4.6 that it happens from temperatures as low as 210K to 370K. As we can see in fig.4.7, the subthreshold swing S increases with increasing temperature from 210 K. From S we extracted the

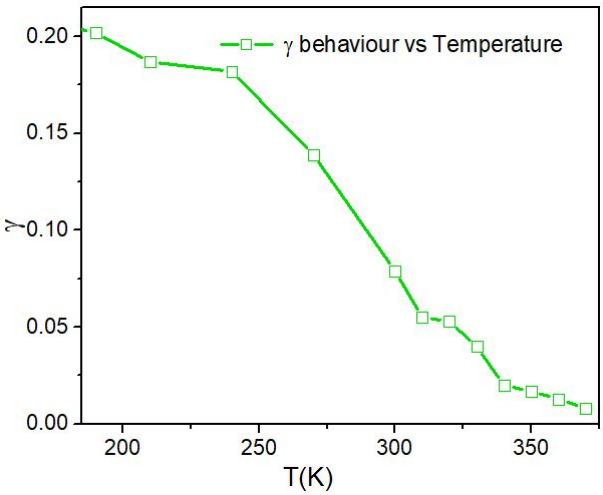

FIGURE 4.3: γ vs Temperature

density of interface states, D_{it} following (Su et al., 2011),

$$D_{it} = \frac{\frac{SqC_i}{kTln(10)} - C_i - C_D}{q} \tag{4.15}$$

where C_D is the depletion capacitance of the IGZO layer, calculated as in (Su et al., 2011). The extracted values of D_{it} show a negligible temperature dependence.

We observe in fig.4.8 that the characteristic temperature of the tail DOS, T_0, is not constant as usually assumed, but increases near linearly with T. The explanation of this effect seems to be the same as for the increase of the characteristic energy of the tail DOS with T observed in a-Si:H materials (reported by (Cody et al., 1981)) from measurements of the optical absorption coefficient: increase of the dynamic phonon disorder. Actually, the model for this effect presented in (Cody et

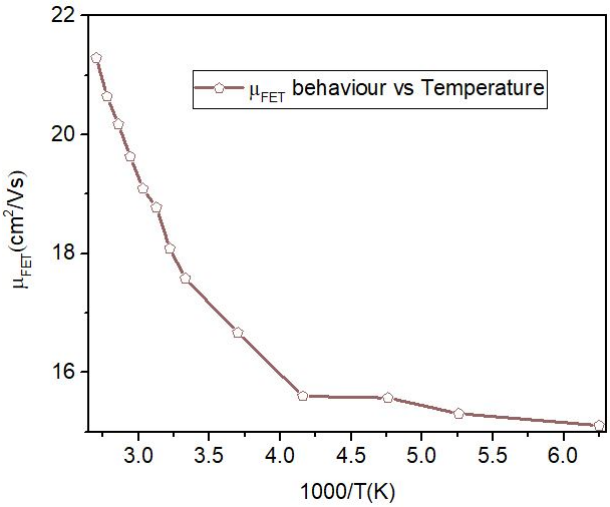

FIGURE 4.4: $\mu_{FET}(V_{GS} = 10V)$ vs Temperature

al., 1981) for a-Si:H materials also predicts a near linear increase of the characteristic energy for temperatures between 150K up to at least 350 K, as we observe in our IGZO TFTs.

In addition (table.4.1), the values of T_0 are lower than others reported before (Estrada et al., 2008b). Obviously, E_A (fig.4.9) shows the same temperature behavior as T_0.

In fig.4.10 we show that the tail state density and the conduction band edge, g_{ato} decreases with temperature, despite it is commonly assumed that it is constant with temperature. This can be considered as a correction of the assumed exponential behavior of the tail DOS in IGZO materials.

The extracted parameter values were incorporated to our IGZO TFT model, which was validated by comparison with the measured $I - V$ characteristics. In the fig.4.11, we observed

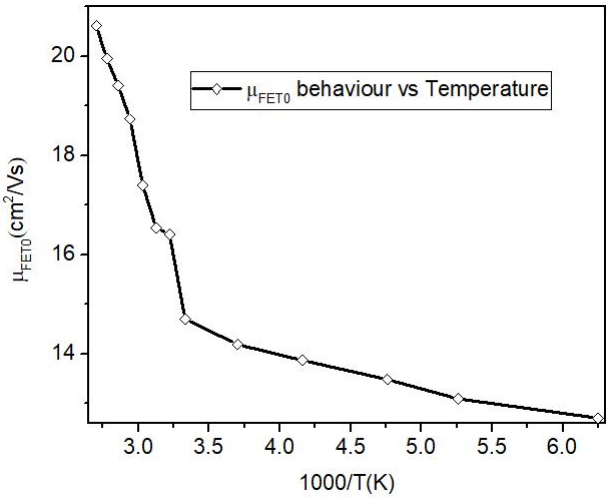

FIGURE 4.5: μ_{FET_0}, which has units of $cm^2/V^{\gamma+1}$ gives the numerical value of μ_{FET} when $V_{GS} - V_T = 1V$

the experimental and modeled transfer and output characteristics at different low and high temperatures. A very good agreement between the experimental I_D data and the modeled I_D is observed from 210K up to 370K.

4.3 Review

We analyzed the behavior of the I-V characteristics for IGZO TFT devices from 210 to 370K. Using a physically-based I-V model and a direct extraction method we obtained the values

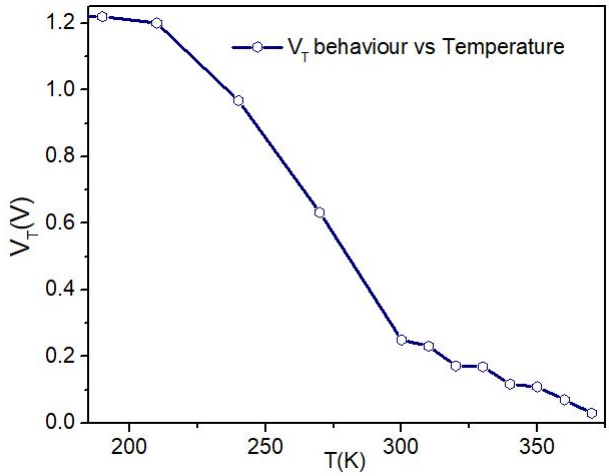

FIGURE 4.6: V_T vs Temperature

of the key physical parameters and we studied their temperature dependence. We found that the characteristic temperature of the DOS and the total trap density vary with temperature, we explained these effects. Using the extracted parameter values in our I-V model, very good agreement was observed with the experimental data from 210 to 370K.

Considering the γ analysis, the behaviour of this IGZO TFT technology is similar to crystalline technologies at high temperatures. Another very good result was the behaviour of the μ_{FET}, at high temperatures this device techology reaches the $22cm^2/Vs$ being it a high value in this kind of IGZO device.

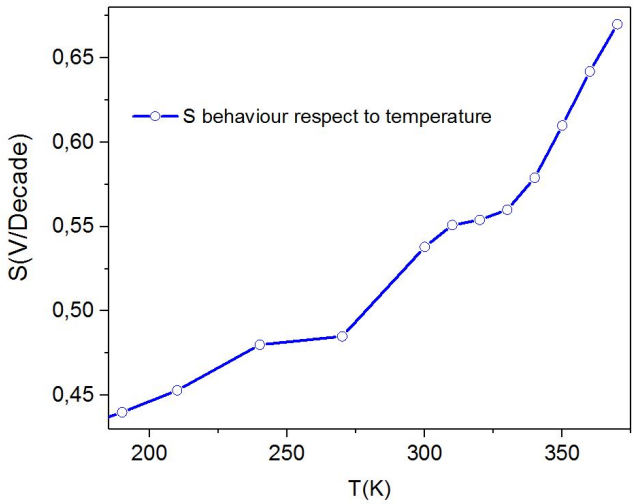

FIGURE 4.7: S vs Temperature

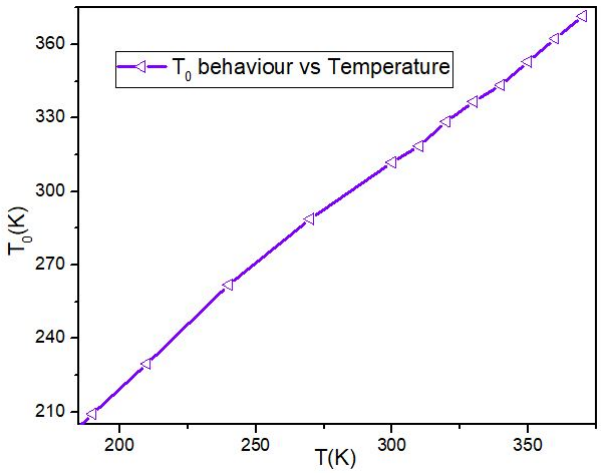

FIGURE 4.8: T_0 vs Temperature

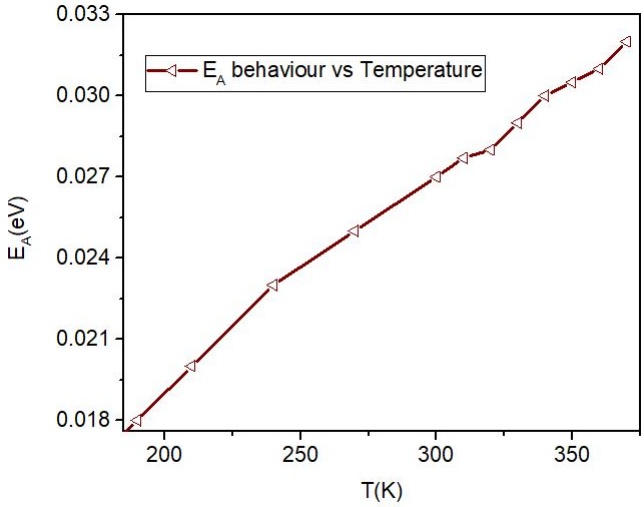

FIGURE 4.9: E_A vs Temperature

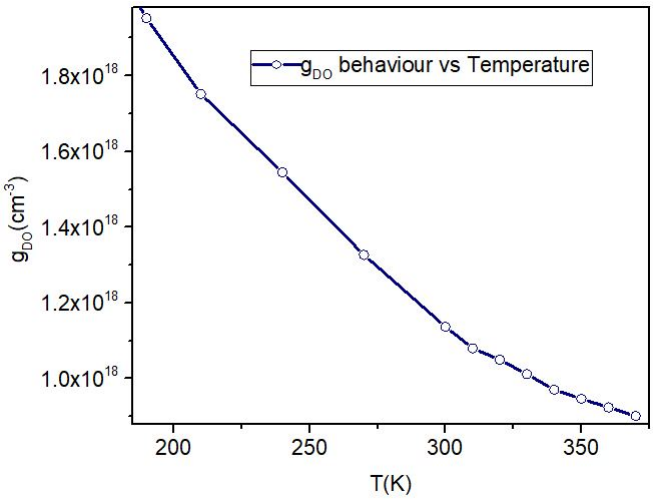

FIGURE 4.10: g_{ato} vs Temperature

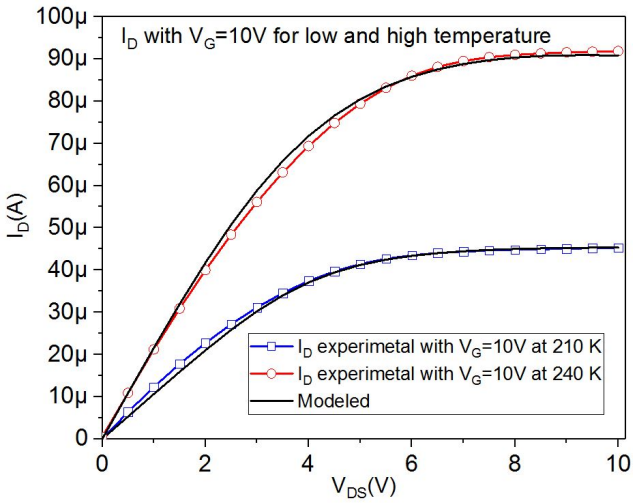

FIGURE 4.11: Experimental and modeled $I_D vs V_{DS}$ for low and high temperatures

Conclusion

In this thesis, we presented drain-source current compact models for OTFTs and IGZO TFTs valid within a range temperature. Also, we developed a gate to gate capacitance compact model that reproduces the regimes observed in the capacitance in OTFTs. To validate each of these models, we extracted parameters from I-V and C-V characteristics at different temperatures and frequencies in OTFTs. For IGZO devices, the parameter extraction was performed at different temperature from I-V characteristics. Generally, we obtained very good agreement between experimental data and models in I-V and C-V characteristics in both organic and IGZO devices. We observed several physical effects which were not reported before and we succeeded in explained physically this effects.

In the chapter 1, we presented a new compact capacitance model for OTFTs. This model shows a good agreement with experimental C-V data at different frequencies. The plot of the first order gate capacitance derivative versus the gate voltage shows two peaks, the first one between the full and partial depletion regimes, the second one between the partial depletion and the accumulation regimes. These peaks are

the result of these transitional behaviours. The presented capacitance model reproduces very well the position of those peaks. It was found that the total capacitance C_{TOT} decreases with increasing frequency. This behaviour is accounted for by using a frequency-dependent dielectric permittivity. In the strong accumulation regime, the model predicts that C_{TOT} takes the C_i values, as observed. The temperature variation does not affect the C_{TOT} values in accumulation, but only in the transition between depletion and accumulation, and this is well reproduced by the model.

The Chapter 2 and 3 we analysed the temperature dependences of the drain current model of two different OTFTs manufacturing technologies between 150K and 350K, and we presented an I-V model showing good agreement with experimental data at both low and high temperatures, using the extracted parameters. The OTFT technology targeted in Chapter 2 was studied at low temperatures(from 150K to 300K), and the OTFT technology addressed in Chapter 3 was analysed from 200K to 350K. The extracted parameters show similar temperature dependencies in both technologies. Both manufacturing technologies show similar temperature dependence considering the physical parameter analysis. We observed for the first time in OTFTs that the characteristic temperature increases almost linearly with increasing temperature and we provided a physical explanation for this effect (increase of the dynamic phonon disorder). We found that the effect of the non-linear contact injection cannot be neglected at low temperatures and we accurately modeled it. The device described in Chapter 2 shows at room temperature μ_{FET}

values higher than other organic transistor technologies published. It was found that as temperature increases above 300K, the mobility tends to become constant with respect to the gate voltage, therefore showing a quasi-crystalline behaviour.

Finally, in the Chapter 4 we addressed the compact modelig of IGZO TFTs at different temperatures. This IGZO technology shows very high values of μ_{FET} compared with other IGZO TFTs technologies. We improved a previous compact IGZO TFT model to accurately account for channel length modulation, and we carried out parameter extraction from IGZO TFT I-V characteristics measured at temperatures ranging from 210K up to 370K. Very good agreement was observed between experimental I-V characteristics and modeled. The temperature dependence of the different parameters was analysed. As in OTFTs, it was found that the characteristic temperature increases almost linearly with the temperature, and we provided the same explanation as in OTFTs(increase of the dynamic photon disorder). For the first time, we also studied the temperature dependence of the maximum trap density, and we provided a qualitative explanation for it(correction of the exponential behaviour of the tail trap of the DOS in OTFTs).

In general, the main conclusions obtained in this doctoral thesis project are the following:

• Gate to gate capacitance compact model for OTFTs was improved and validated at frequencies and temperatures from 500 Hz up to 10 kHz and 150K up to 300K respectively

• Drain to source current compact model for OTFTs was extended and validated for temperatures from 150K up to 350K

• Drain to source current compact model for IGZO TFTs was extended and validated from temperatures from 200K up to 370K

• Very good agreement between experimental and modeled gate to gate capacitance

• The model reproduces accurately the operation regimes changes At 500 Hz, 1 kHz and 10 kHz

• The gate to gate capacitance takes the C_i values in the accumulation regime

• The gate to gate capacitance decreases with increasing frequency

• The OTFT dielectric constant decreases with increasing frequency

• The temperature affects the capacitance at low gate voltage

• Reasonable good agreement between the modeled and experimental data over the targeted range of temperatures in OTFTs and IGZO devices

• The subthreshold swing increases with increasing temperature

• The threshold voltage decreases with increasing temperature in OTFT devices

• The threshold voltage decreases with increasing temperature in IGZO devices

• The characteristic temperature increases as temperature is risen in both OTFTs and IGZO transistors due to the dynamic phonon disorder

• The field effect mobility increases with increasing temperature in both OTFT and IGZO TFT devices, due to the increasing concentration of mobile carriers.

• In both the IGZO TFT and OTFTs technologies the drain current increases with increasing temperature due to the field effect mobility increase

• At high temperatures the OTFTs and IGZO transistors behaviors is similar to crystalline device

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PHYSICAL BEHAVIOUR ANALYSIS AND COMPACT TEMPERATURE-DEPENDENT MODELING IN ORGANIC AND IGZO TFTS
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