Universitat Autònoma de Barcelona

Low-Power High-Resolution CMOS Switched-Capacitor Delta-Sigma Analog-to-Digital Converters for Sensor Applications

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Dr. Michele Dei, Científic amb contracte "Torres Quevedo" a X-Ray Imatek S.L. i adscrit a l'Institut de Microelectrònica de Barcelona pertanyent al Centro Nacional de Microelectrónica del Consejo Superior de Investigaciones Científicas, Dr. Carles Ferrer Ramis, Catedràtic del Departament de Microelectrònica i Sistemes Electrònics, i Dr. Francesc Serra Graells, Professor Titular del Departament de Microelectrònica i Sistemes Electrònics,

Certifiquen

que la Memòria de Tesi *Low-Power High-Resolution CMOS Switched-Capacitor Delta-Sigma Analog-to-Digital Converters for Sensor Applications* presentada per Stepan Sutula per optar al títol de Doctor en Microelectrònica i Sistemes Electrònics s'ha realitzat sota la seva direcció a l'Institut de Microelectrònica de Barcelona pertanyent al Centro Nacional de Microelectrónica del Consejo Superior de Investigaciones Científicas i ha estat tutoritzada en el Departament de Microelectrònica i Sistemes Electrònics de la Universitat Autònoma de Barcelona.

Directors	Dr. Michele Dei	.....
	Dr. Carles Ferrer Ramis	.....
	Dr. Francesc Serra Graells	.....

....., a ..... de ..... de .....

to the bright memory of Salvador Martín Rubio

Resum

Aquesta tesi doctoral explora mètodes per augmentar tant l'eficiència energètica com la resolució de convertidors analògic-digital (ADCs) Delta-Sigma de condensadors commutats mitjançant innovadors circuits CMOS de baix consum. En aquest sentit, s'ha prioritzat un alt rendiment, fiabilitat i baixos costos de fabricació dels circuits, així com un flux de disseny simple per ser reutilitzat per la comunitat científica.

S'ha escollit l'arquitectura Delta-Sigma per la seva simplicitat i la tolerància a les imperfeccions dels seus blocs bàsics. La recerca de circuits presentada utilitza tècniques de condensadors commutats per aconseguir un aparellament adequat entre els dispositius i per tenir dependència només de la fluctuació del rellotge extern.

Les tècniques de disseny de circuits analògics de baix corrent desenvolupades tenen com a objectiu l'eficiència energètica, aprofitant les regions d'inversió feble i moderada d'operació del transistor MOS. També s'investiguen nous amplificadors operacionals Classe AB com a elements actius, tractant d'utilitzar energia només durant les transicions dinàmiques, el que redueix el consum de potència a nivell de circuit. Els circuits no utilitzats durant un determinat període de temps es desactiven, reduint així el consum de potència a nivell de sistema i minimitzant el nombre de dispositius de commutació en el camí de senyal.

S'ha millorat la fiabilitat dels circuits proposats evitant els elevadors de tensió o altres tècniques que poden incrementar els voltatges d'operació més enllà del d'alimentació nominal de la tecnologia CMOS utilitzada. A més, per incrementar el rendiment de producció dels ADCs resultants, s'ha enfocat la recerca de disseny sobre noves topologies de circuits amb una baixa sensibilitat a les variacions tant del procés de fabricació com de la temperatura.

Un modulador Delta-Sigma de 96.6 dB de SNDR, 50 kHz d'ample de banda, 1.8 V i 7.9 mW per a ADCs s'ha implementat en una tecnologia estàndard CMOS de 0.18 µm basat en les novetats proposades. Els resultats de les

mesures indiquen la millora de l'estat de l'art d'ADCs d'alta resolució sense elevadors de tensió del senyal de rellotge, calibratge o compensació digital, fet que beneficia una àmplia gamma d'aplicacions de sensors intel·ligents.

Una altra contribució en el marc d'aquest treball de recerca és la millora dels amplificadors operacionals de Classe AB d'una sola etapa exclusivament MOS. Els amplificadors commutats de mirall variable desenvolupats, amb la seva remarcable eficiència de corrent i compensació intrínseca de freqüència juntament amb un fons d'escala i un guany de llaç obert grans, són adequats per a un ample ventall d'aplicacions de baix consum i d'alta precisió més enllà de l'àmbit específic dels ADCs, com a convertidors digital-analògic (DACs), filtres o generadors.

Abstract

This PhD thesis explores methods to increase both the power efficiency and the resolution of switched-capacitor Delta-Sigma analog-to-digital converters (ADCs) by employing novel CMOS low-power circuits. A high circuit performance, reliability, low manufacturing costs and a simple design flow to be reused by the scientific community are prioritized.

The Delta-Sigma architecture is chosen because of its simplicity and tolerance for its basic block imperfections. The presented circuit research makes use of switched-capacitor techniques to achieve an appropriate matching between the devices and to be dependent only on the external clock jitter.

The developed low-current analog circuit techniques target power efficiency, taking advantage of the weak- and moderate-inversion regions of the MOS transistor operation. Novel Class-AB operational amplifiers are also investigated as active elements, trying to use energy only for dynamic transitions, thus reducing power consumption at the circuit level. The circuits unused during a certain period of time are switched off, thus reducing power consumption at the system level and minimizing the number of signal-path switching devices.

The circuit reliability is improved by avoiding bootstrapping or other techniques which may increase the operation voltages beyond the nominal supply of the target CMOS technology. Furthermore, the design research also focuses on new circuit topologies with a low sensitivity to both process and temperature deviations in order to increase the yield of the resulting ADCs.

A 96.6-dB-SNDR 50-kHz-BW 1.8-V 7.9-mW Delta-Sigma modulator for ADCs is implemented in a standard 0.18-µm CMOS technology based on the proposed novelties. The measurement results indicate the improvement of the state of the art of high-resolution ADCs without clock bootstrapping, calibration or digital compensation, benefiting a wide range of smart sensing applications.

Another contribution made in the scope of this research work is the improvement of MOS-only single-stage Class-AB operational amplifiers. The

developed switched variable-mirror amplifiers, with their remarkable current efficiency and intrinsic frequency compensation together with high full-scale value and open-loop gain, are suitable for low-power high-precision applications extending beyond the specific area of ADCs, such as digital-to-analog converters (DACs), filters or generators.

Acknowledgements

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For being at my side through highs and lows, I thank my girlfriend Cristina, family and friends.

Finally, I thank those teachers and mentors I had over the past two decades, who took me on this amazing journey to the Land of Electronics.

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ACM Advanced Compact MOSFET . . . 2
ADC analog-to-digital converter . . . 1
BEC bubble error correction . . . 6
BW bandwidth . . . 5
CMFB common-mode feedback . . . 42
CMOS complementary metal-oxide-semiconductor . . . 1
DEM dynamic element matching . . . 24
DR dynamic range . . . 27
DSP digital-signal processing . . . 4
DUT device under test . . . xxiv
EDA electronic design automation . . . 3
EKV C. C. Enz, F. Krummenacher and E. A. Vittoz . . . 2
FFT Fast Fourier Transform . . . 26
FIFO first-in, first-out . . . 125
FOM figure of merit . . . 14
FPGA field-programmable gate array . . . 125

FS full scale . . . 81
HDL hardware-description language . . . 101
JTAG Joint Test Action Group . . . 125
LVDS low-voltage differential signaling . . . 135
LSB least significant bit . . . 4
MASH multi-stage noise-shaping . . . 22
MOSFET metal-oxide-semiconductor field-effect transistor . . . 2
MSB most significant bit . . . 7
NTF noise transfer function . . . 11
OpAmp operational amplifier . . . 2
OSR oversampling ratio . . . 10
PC personal computer . . . 125
PSD power spectral density . . . 4
SAGE System for Algebra and Geometry Experimentation . . . 72
SAR successive-approximation-register . . . 9
SC switched-capacitor . . . 2
SDR signal-to-distortion ratio . . . 101
SFDR spurious-free dynamic range . . . 105
S/H sample and hold . . . 4
SNDR signal-to-noise-plus-distortion ratio . . . 14
SNR signal-to-noise ratio . . . 30
SQNDR signal-to-quantization-noise-plus-distortion ratio . . . 105
SQNR signal-to-quantization-noise ratio . . . 27
STF signal transfer function . . . 11
SVMA switched VMA . . . 60
TCL Tool Command Language . . . 126
USB Universal Serial Bus . . . 125
VMA variable-mirror amplifier . . . 37

Introduction | 1

1.1 Motivation

The growing market of smart sensing applications demands high-resolution analog-to-digital converters (ADCs) to interface as precisely as possible the physical world of transducers with the digital world of signal processing in a number of fields such as environmental monitoring, child education, surveillance, micro-surgery, and agriculture [1, 2]. Although featuring a reduced bandwidth, typically lower than 1 MHz, these ADCs may exhibit dynamic-range values exceeding 90 dB [3–21]. Generally, to achieve such a high resolution, power consumption needs to be increased. This design approach reduces circuit noise and signal distortion, but also limits the battery life of portable applications. Instead of increasing the battery capacity to compensate for this loss, research into low-power techniques may be a promising strategy, until the point when traditional contaminating power sources can be replaced by environment-friendly energy scavengers, which are currently limited in terms of supply capability with respect to the former.

The trend is to integrate ADCs together with the sensor network and the post-processing digital circuitry on the same integrated-circuit die [22–25], which is fundamental to achieve a higher level of smartness of the network itself for a better use of the sensing units and the local-node signal processing and communication. Therefore, the idea of achieving state-of-the-art results using a standard inexpensive complementary metal-oxide-semiconductor (CMOS) technology is attractive. However, with the continuous downscaling of feature sizes of the CMOS technologies, devices are

suffering more degradation of their analog characteristics [26]. A solution to compensate for this issue can be provided by the Delta-Sigma ($\Delta\Sigma$) architecture because of their high tolerance for the imperfections of the basic building blocks [27], especially for the amplifier non-idealities.

Although continuous-time ADCs currently represent an active research field, their performance is severely affected by clock jitter [28]. On the other hand, discrete-time implementations using switched-capacitor (SC) techniques strongly alleviate this problem and decrease matching errors between devices, as well, resulting in stable filter coefficients.

One of the most power-hungry blocks in these SC $\Delta\Sigma$ ADCs is the operational amplifier (OpAmp). Traditional Class-A OpAmps drain a large static current, which has no useful contribution to the discrete-time signal processing itself since the signal samples are significant at the end of the sampling period only, regardless of their previous transient, provided the required settling error is met. Research into Class-AB OpAmps may shift the energy usage preferably towards useful dynamic transitions, thus reducing power consumption at the circuit level [29–35]. Classically, OpAmps are powered on even during the time periods when they are not used. Switching them off may help to save energy at the system level and, also, to minimize the number of signal-path switching devices, thus alleviating distortion-related problems [36].

Power-consumption optimization is one of the most important topics of this PhD thesis, and it has been faced at both the device and system levels.

At the device level, traditional design equations describe the operation of the metal-oxide-semiconductor field-effect transistor (MOSFET) only in the strong-inversion region, whose choice leads to power inefficiency in many designs. The C. C. Enz, F. Krummenacher and E. A. Vittoz (EKV) and Advanced Compact MOSFET (ACM) models [37, 38] are good choices to take advantage of the weak and moderate inversion regions, managing the reduction of power consumption by the handmade estimations of transistor performances.

At the system level, some of the state-of-the-art high-resolution-ADC designs use driving voltages that might surpass the technology supply limits, in this way undermining reliability of the integrated circuit. Thus, it is ad-

visable to reject techniques such as bootstrapping, whose implementation also requires complex schemes. Furthermore, some of the $\Delta\Sigma$-ADC design proposals rely on calibration, achieving high-resolution performance, but increasing the manufacturing and operation costs. Therefore, calibration-free circuits are of interest for most smart-sensing applications.

Finally, since using proprietary tools for electronic design automation (EDA) usually prevents from inspecting and modifying their code to meet particular needs, there is a motivation to use open-source programs whenever it is possible [39, 40]. Also, the independence from any closed computational environment may improve workflow automation, which plays a key role in increasing scientific productivity [41]. Hence, it would be desirable to extend the use of the open-source EDA tools to the full-custom integrated-circuit CMOS designs obtained in this research work.

The motivation factors described above led to the inception of this PhD thesis during the research activities on the CMOS read-out integrated circuits for the arrays of long-wave infrared thermal sensors [42–45]. These activities were followed by the development of the potentiostatic $\Delta\Sigma$ ADC for smart electrochemical sensors [22, 23]. Finally, the work on the high-resolution ADCs for space missions in the scope of the project funded by the European Space Research and Technology Centre (ESTEC) under the contract 40000101556/10/NL/AF, provided the main contributions of this PhD thesis, resulting in [29] and other publications in the process of dissemination.

1.2 Analog-to-Digital Conversion Techniques

A typical ADC system is illustrated in Fig. 1.1. It converts the continuous-time analog signal $V_{\text{in}}(t)$ to the discrete-time digital signal $\delta_{\text{out}}(n)$, which is a digital number measuring the analog value of $V_{\text{in}}(t)$ with the introduction of some error.

At the input, the anti-aliasing filter, which usually has a low-pass transfer function, limits the input-signal bandwidth, preventing the overlapping in the base band of the out-of-band signal and input-noise spectrums around multiples of the sampling frequency f_{s} in the next stage [46]. After that,

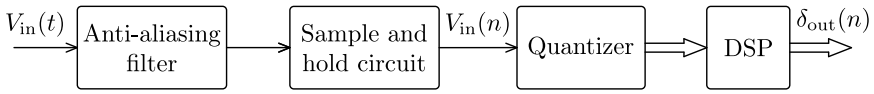

Figure 1.1 | General ADC system.

the sample and hold (S/H) circuit performs the signal discretization in the time domain, and, then, the quantizer carries out the discretization in the amplitude, feeding the obtained digital signal to thedigital-signal processing (DSP) system for an additional treatment such as digital filtering and decimation. The number of discrete values M which an ADC can produce at the output determines the resolution parameter, which is usually expressed in the bits number N:

$$N = \log_2(M). \tag{1.1}$$

Fig. 1.2 presents an example of the transfer curve and the error function of a uniform ADC quantizer with $M = 4$, and thus, according to (1.1), yielding a 2-bit resolution. Here, V is the analog input voltage with the full scale $V_{\text{min}} < V < V_{\text{max}}$, and δ_{q} is the quantized output. The least significant bit (LSB) of an ADC is defined by the quantization step Δ:

$$\Delta = \frac{V_{\text{max}} - V_{\text{min}}}{2^N - 1}. \tag{1.2}$$

The quantization error ϵ_{q} is always present during the normal operation of an ADC with values ranging from $-\Delta/2$ to $\Delta/2$, as can be seen in Fig. 1.2. It has been assumed that the ϵ_{q} probability distribution is uniform across this range. As a consequence, ϵ_{q} is treated like a white noise, referred to as the quantization noise, with its power evently distributed between the sampling-frequency halves $-f_{\text{s}}/2$ and $f_{\text{s}}/2$ and the power spectral density (PSD) given by [47]:

$$S_{\varepsilon}(f) = \frac{1}{f_{\text{s}}} \left[\frac{1}{\Delta} \int_{-\Delta/2}^{\Delta/2} \epsilon_{\text{q}}^2 \, d\epsilon_{\text{q}} \right] = \frac{\Delta^2}{12 f_{\text{s}}}. \tag{1.3}$$

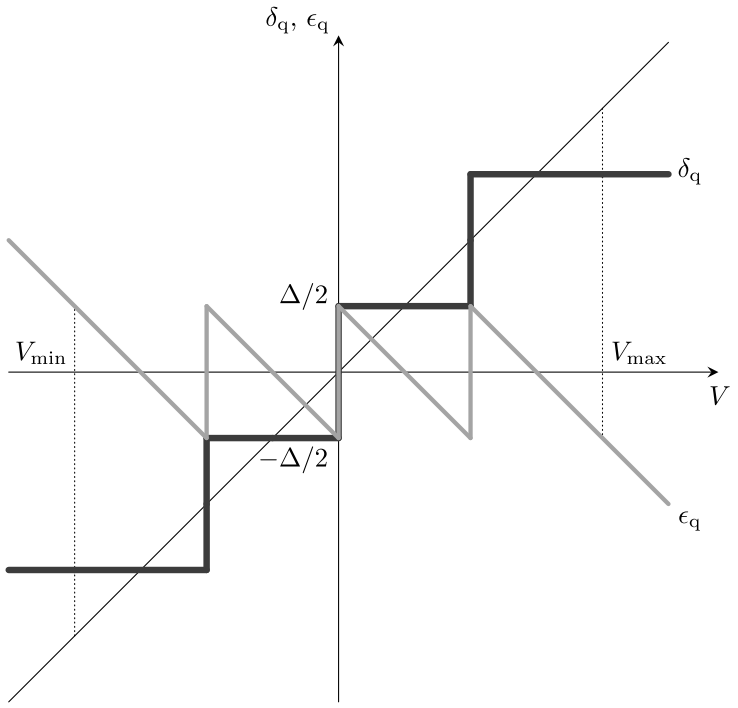

Figure 1.2 An example of the transfer curve and the error function of a 2-bit ADC quantizer.

All fundamental ADC architectures used today had been discovered and published in one form or another by the mid-1960s [48]. They will be reviewed below. In all cases, it will be supposed that the input analog signal is processed by the anti-aliasing filter and the resulting output digital signal is fed into the DSP circuit which has no feedback path to the ADC core.

1.2.1 Flash ADC

The flash-ADC principle, shown in Fig. 1.3, is common to all fundamental ADC architectures in some degree. The input signal $V_{in}(t)$ is first sampled and held at the Nyquist rate of two times the input bandwidth (BW) to avoid aliasing. Then, each sample is sensed by the array of compara-

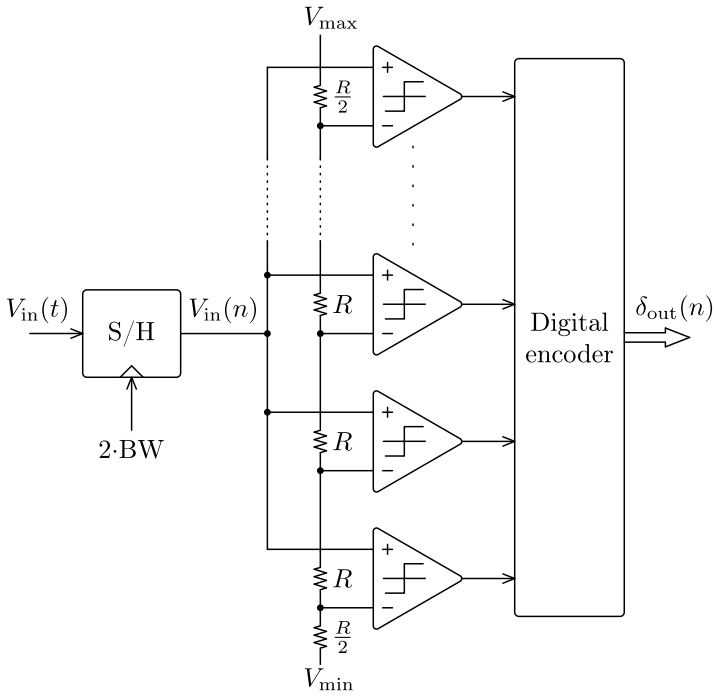

Figure 1.3 | General flash-ADC architecture.

tors, which are triggered at the beginning of each conversion cycle. Each comparator generates a logical high- or low-level output signal depending on whether $V_{\text{in}}(n)$ is above or below the comparator reference voltage, respectively. The reference voltages are typically generated by a ladder of matched resistors, as in Fig. 1.3, connected between the full-scale positive $V_{\max}$ and negative $V_{\min}$ references. In SC applications, sampling capacitors can be also employed instead of resistors as voltage dividers, thus reducing the static power consumption. If f_{s} is high enough, the charge leakage from the capacitors can be neglected.

From the point of view of a whole block, the comparator array generates a thermometric-like code, which is converted into a binary code $\delta_{\text{out}}(n)$ by the digital encoder. Usually, the encoding algorithm also incorporates the bubble error correction (BEC) to prevent one of the erroneously tripped

comparators from corrupting the entire output code [49]. The linearity of the flash ADC is improved if the input-equivalent offset of the comparators is reduced by means of individual preamplifiers. These preamplifiers also isolate the reference ladder from the kick-back noise generated by a high-swing activity of the comparators. However, the use of preamplifiers increases power consumption.

To obtain a resolution of N bits, the number of comparators which the flash ADC needs to employ is $2^N - 1$. It means that to reach even a modest 8-bit resolution, as much as 255 comparators are required, drastically increasing circuit power consumption and area. Moreover, the input load is also increased, reducing the input-signal bandwidth. This makes the flash ADCs inappropriate for high-resolution applications. As will be shown in Section 1.4, there are no state-of-the-art stand-alone flash ADCs surpassing an 8-bit resolution. To achieve a higher resolution, fabrication trimming or digital calibration are needed. However, these techniques boost the circuit manufacturing and operation costs.

1.2.2 Folding ADC

The number of required components is reduced with respect to the flash ADC of Fig. 1.3 if it is split into two parallel subADCs, as illustrated in Fig. 1.4: the first, for a coarse quantization, determining the most significant bits (MSBs) $\delta_{\text{coarse}}(n)$; and, the second, for a fine quantization, determining the LSBs $\delta_{\text{fine}}(n)$. A folding circuit is used at the input of the fine ADC to transform the input signal into a signal which is repeated in the intervals

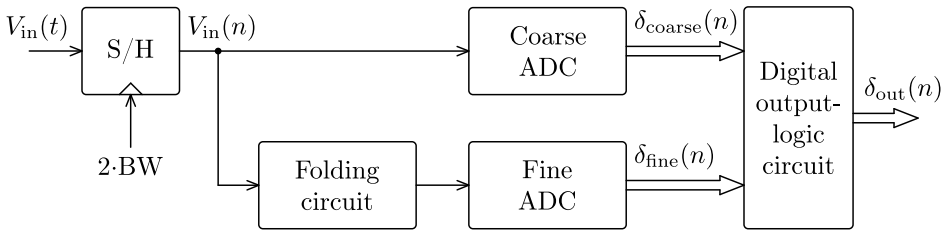

Figure 1.4 | General folding-ADC architecture.

marked by the MSBs. Therefore, the same reduced set of components can be reused in all intervals. For this reason, this type of ADCs is called the folding ADC. For example, in order to obtain the same 8-bit resolution, using 4-bit coarse and 4-bit fine ADCs, only $2^4-1+2^4-1 = 30$ comparators are needed, in contrast with $2^8-1 = 255$ comparators required for the flash ADC.

The area and power-consumption savings, obtained employing this architecture, can be invested in the accuracy increase. Thus, the state-of-the-art folding ADCs report resolution values up to 14 bits [50], still however below the target performance of this PhD thesis.

1.2.3 Pipeline ADC

The pipeline ADCs further improve the resolution feature and minimize the integration area by splitting the data-conversion processes into two or more sequential steps of subranging, as shown in Fig. 1.5. Each stage of subranging consists of a S/H operated at a 2-BW rate, an analog-to-digital conversion providing a portion of bits to a digital post-processing circuit, a digital-to-analog reconstruction, a subtraction of the reconstructed analog signal from the previously sampled input signal and a subtraction-result amplification to adapt the residual-signal amplitude to the input full scale of the following stage. The first stage is responsible for the MSBs, and the following stages refine the measurement, reaching the LSBs. Since the conversion of the same input sample is produced by each stage at different points of time, a time-alignment function is implemented in the post-processing circuit, which may also incorporate a digital error correction to relax the precision requirements of the individual stages [51].

Although a high bandwidth can be easily achieved using the pipeline ADC architecture, the need for sequential signal processing introduces an L-cycle latency with respect to the flash ADCs, where L is the number of pipelined stages. This ADC type offers one of the best trade-offs between the power consumption and the achievable resolution. However, most of the practical resolution values of the reported designs are located below 13 bits [52]. This resolution limitation is derived from the blocks marked with A in Fig. 1.5, since they are responsible for the residue propagation of each stage: any

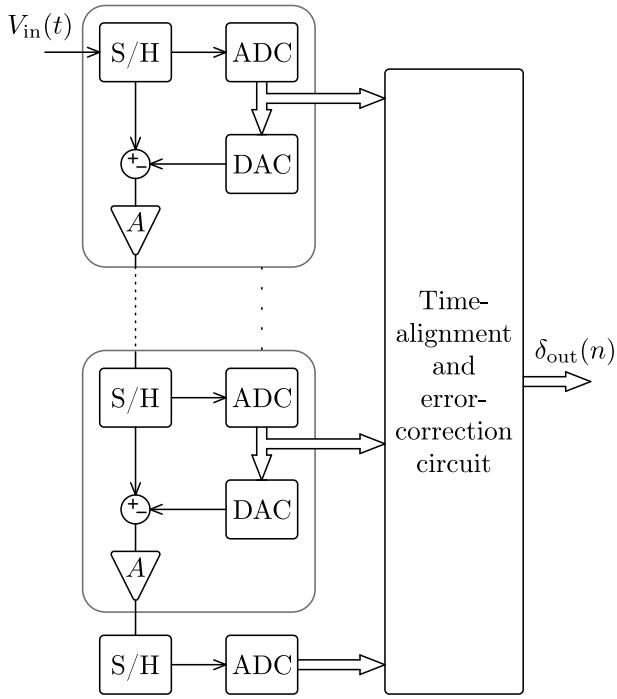

Figure 1.5 | General pipeline-ADC architecture.

deviation from the ideal value of the amplification A will result inevitably in a non-linearity of the conversion, thus limiting the achievable resolution.

1.2.4 Successive-approximation ADC

Instead of pipelining stages, the same stage can be reused in a successive-approximation closed loop, as shown in Fig. 1.6. During one conversion cycle, the sampled input signal is successively compared to the feedback signal $V_{\text{fb}}(n)$. The feedback DAC updates $V_{\text{fb}}(n)$ according to the successive-approximation-register (SAR) binary search algorithm, which consists in tracking the input signal with an increasing precision for each succession and providing the resulting digital output $\delta_{\text{out}}(n)$ with a maximum resolution at the end of the conversion cycle. Since the same blocks are used during

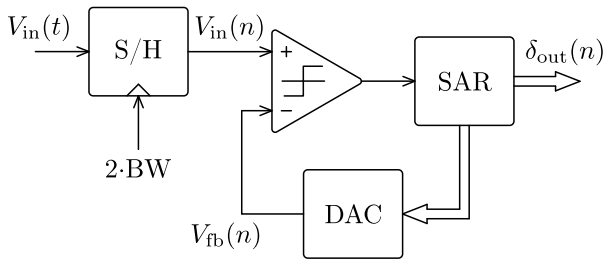

Figure 1.6 | General SAR-ADC architecture.

the whole conversion process, the resolution limitation which affects the pipeline-ADC architecture is less stringent here. This allows to further minimize integration area and to reduce latency to one cycle, but at the cost of a reduced bandwidth due to an overclocking with respect to the final data rate. This overclocking is needed to enable the required number of converging iterations to be performed in the same conversion cycle.

As the number of analog blocks is reduced, SAR ADCs also exhibit lower power consumption. However, the achievable practical resolution values are limited by the non-linearity of the feedback DAC and still do not surpass 14 bits, according to the reported state-of-the-art designs [52].

1.2.5 Oversampling ΔΣ ADC

The ADC types discussed above operate providing the output samples at the data rate f_{s} of two times the input-signal bandwidth. For this reason, they are called Nyquist-rate ADCs. According to the Nyquist-Shannon sampling theorem, f_{s} must be at least as high as the Nyquist frequency f_{N}, which is defined as

$$f_{\mathrm{N}} = 2 \cdot \mathrm{BW}. \tag{1.4}$$

If f_{s} is increased with respect to f_{N}, a feature is added to the ADC performance called oversampling, introducing the oversampling ratio (OSR)

as [27]:

$$\mathrm{OSR} = \frac{f_\mathrm{s}}{f_\mathrm{N}} = \frac{f_\mathrm{s}}{2 \cdot \mathrm{BW}}. \tag{1.5}$$

Using (1.3) and (1.5), the quantization-noise in-band power P_ε can be found as

$$P_\varepsilon = \int_{-\mathrm{BW}}^{\mathrm{BW}} S_\varepsilon(f)\, df = \frac{\Delta^2}{12 \cdot \mathrm{OSR}}. \tag{1.6}$$

From (1.6), it can be seen that the oversampling feature allows to reduce P_ε by 3 dB by each OSR doubling. For an oversampling ADC, this implies a resolution increase of 0.5 bit/octave.

An additional advantage of oversampling is that the specifications of the input continuous-time anti-aliasing filter are relaxed if compared to that of Nyquist-rate ADCs. This is because there is no need for a sharp transition band, which may also introduce phase distortion [53]. A drawback of oversampling is that, an overclocking is needed with respect to the final data rate, as in the case of SAR ADCs, and this results in a reduced bandwidth.

The resolution of oversampling ADCs can be further improved through additional P_ε attenuation using an ADC architecture based on a $\Delta\Sigma$-modulator ($\Delta\Sigma$M) loop, shown in Fig. 1.7. Here, the analog version of δ_l, generated by the feedback DAC, is subtracted from the sampled input signal and processed by the discrete-time high-gain loop filter, so that most of the quantization-noise power is shifted to the outside of the signal band and the equivalent P_ε is attenuated. This processes is called noise shaping. The noise transfer function (NTF) of the modulator is usually of high-pass or band-stop type, while the signal transfer function (STF) is of all-pass type. This difference plays the key role in increasing the resolution of $\Delta\Sigma$-ADCs and will be discussed in detail in the next chapter. It will be shown how the basic-block imperfections have little or no impact on the $\Delta\Sigma$-ADC performance, which serves as a determining factor in selecting this ADC type as an object of research in this PhD thesis. A comparative study of the

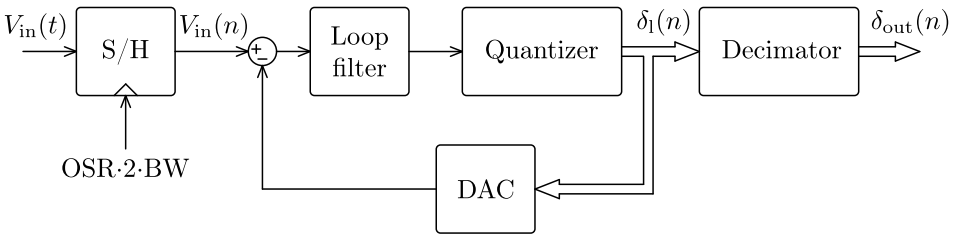

Figure 1.7 | General ΔΣ-ADC architecture.

state-of-the-art ADCs in Section 1.4 will also show that, up to date, no other ADC type can achieve better performance than that of ΔΣ ADCs.

As it can be seen in Fig. 1.7, an additional digital circuit block called decimator is needed to reduce the data-output rate of ΔΣM to the Nyquist frequency and to remove the quantization noise outside the band of interest. This digital block requires some extra dynamic power, which is however scaling down with CMOS technologies.

1.3 Low-Current versus Low-Voltage Design in Nanometer CMOS Technologies

The current trend of CMOS technologies adapting nanometer device lengths suggests that ADCs will be implemented using nodes below 10 nm by the year 2020 [54]. The digital parts of an ADC greatly benefit from this trend as their sizes and response times are decreased. However, the analog parts cannot fully take advantage of this scaling due to various arising issues. First, a shrinking length makes CMOS devices more sensitive to its variations due to process and mismatch effects. This challenges the modeling of nanometer CMOS devices and requires more design effort. Additional issues arise from the voltage supply decrease, which must be applied when scaling down the CMOS devices to prevent the transistor breakdown. On the other hand, the device threshold voltage is not scaled at the same rate as the supply voltage, resulting in a degradation of device characteristics and a reduction of the internal signal full scale. This voltage-swing reduction

directly affects the CMOS ADCs as their resolution depends on the noise floor, which is due to different physical phenomena and does not decrease with the technology downscaling. Therefore, the only means to reduce this noise floor is an increased power consumption, making the research into new low-power circuit topologies of substantial interest [55].

To improve the power efficiency and resolution of an ADC the maximum attention must be paid to its most power-hungry and distorting blocks such as OpAmps and switches in SC applications. In general, low-power design techniques can be classified into two different strategies: low-voltage and low-current circuits. In the first approach, power savings are obtained by scaling down the nominal supply voltage of the overall circuit. The consequent reduction of available voltage room between power rails is then compensated by specific circuit techniques, which try to optimize the allocation of internal signal headroom against device non-linearities. Examples of low-voltage design strategies are: rail-to-rail OpAmps [56–59], bulk-driven OpAmps [59, 60], internal supply multipliers to drive critical switches [61–63], comparator-based OpAmps [64–70], and switched-OpAmps (SOAs) for replacing critical switches [36]. In practice, low-voltage techniques only achieve moderate power saving ratios, in the order of a single octave due to technology limitations (e.g. MOSFET threshold voltage) or even to the increase of current consumption (e.g. extra biasing circuits).

When stronger power reduction is needed, low-current circuit techniques are mandatory. In this sense, the low-current OpAmp designs reported in literature exploit Class-AB operation, like: telescopic differential pairs with local common mode feedback (LCMFB) [31], dynamic biasing through RC bias tees [32], hybrid Class-A/AB operation [33], cascaded self-biased inverters [34] and adaptive biasing [35]. Unfortunately, most of the above circuit techniques rely on multi-stage OpAmp architectures, with the consequent power penalties imposed by frequency compensation, or their Class-AB performance tends to suffer from strong technology sensitivity. In this PhD thesis, low-current circuit techniques are explored in Chapter 3, focusing on SC Class-AB OpAmps.

1.4 State-of-the-Art Low-Power High-Resolution ADCs

The ADCs of different types and specifications cannot be directly compared. For this reason, their comparison is performed by combining the most important common parameters into a single figure of merit (FOM). The Walden FOM [71] is extensively used and defined as

$$\mathrm{FOMW} = \frac{P}{2 \cdot \mathrm{BW} \cdot 2^{\mathrm{ENOB}}}, \tag{1.7}$$

where P is the static power consumption and ENOB is the effective number of bits, which is derived from the signal-to-noise-plus-distortion ratio (SNDR) of the ADC in dB:

$$\mathrm{ENOB} = \frac{\mathrm{SNDR} - 1.76}{6.02}. \tag{1.8}$$

In comparing high-resolution ADCs, the Walden FOM is not appropriate as it is based on a circuit power model where each quantization level adds a constant amount of extra consumption, like in the flash-ADC architecture of Fig. 1.3. In our case, the best choice is the Schreier FOM [27], which also takes into account the thermal-noise limits:

$$\mathrm{FOMS} = \mathrm{SNDR} + 10 \log \left(\frac{\mathrm{BW}}{P} \right). \tag{1.9}$$

The performance comparison of the state-of-the-art ADCs of different architectures [52] is illustrated in Fig. 1.8. This type of performance analysis will be used in Chapter 5 when comparing with the results of this PhD thesis. Other key circuit parameters not included in FOMS like silicon area, calibration requirements or the use of the internal supply bootstrapping will be also taken into account there. By now, it can be seen that the SC $\Delta\Sigma$ architecture is of the best choice for high-resolution ADC designs. Other qualitative parameters which are not included in Fig. 1.8, such as latency and area, are compared for all ADC groups in Table 1.1 [51]. From this comparison, it follows that, if a lower bandwidth and a higher latency

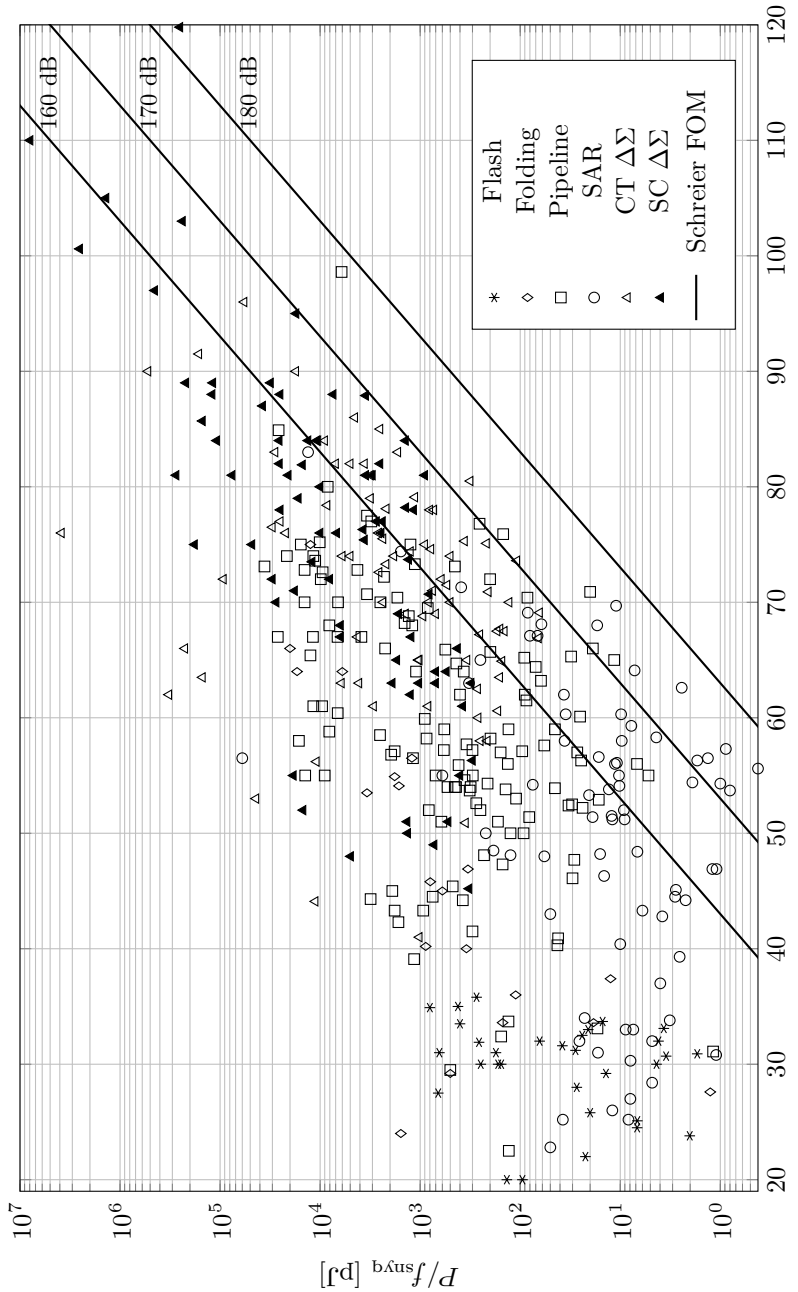

Figure 1.8 | Performance comparison of the state-of-the-art ADCs reported from 1997 to 2015 [52]. The lines of 160-, 170-, and 180-dB Schreier FOMs are plotted as a visual reference.

Architecture	Resolution	Bandwidth	Latency	Area
Flash	Low	High	Low	High
Folding	Medium	Medium-high	Low	High
Pipeline	Medium-high	Medium-high	High	Medium
SAR	Medium-high	Low-medium	Low	Low
$\Delta\Sigma$	High	Low	High	Medium

Table 1.1 | Comparison of ADC architectures [51].

are allowed, as in the case of sensor applications, $\Delta\Sigma$ remains the most attractive ADC architecture.

1.5 Objectives and Scope

The initial working hypotheses accepted as a basis of the research activities in this PhD thesis can be summarized in the following statements of expectation:

- Using a standard CMOS technology without special features, a low-cost calibration-free state-of-the-art ADC can be obtained, featuring low power consumption and high resolution.
- Employing the circuit topologies which are as simple as possible, saves the design time and effort and can be invested in the research for their improvement and adaptation to high-performance microelectronics.
- When designing low-power circuits, low-current design techniques are preferred over low-voltage design techniques and can provide higher power savings.
- A complex mixed-signal research can be conducted using open-source tools only.

To test and demonstrate these hypotheses, the research work presented in this PhD thesis is focused in obtaining a low-power high-resolution ADC integrated in a standard CMOS technology, including the following points:

- The advantage of the $\Delta\Sigma$-architecture simplicity and the tolerance for its basic block imperfections is taken.
- Switched-capacitor techniques are used to achieve a good matching between the devices and to be dependent only on the external clock jitter. Their side effects, as charge injection, are taken into account and canceled.
- Low-current techniques are employed in the circuit research, taking advantage of the weak- and moderate-inversion regions of the CMOS-device operation, thus reducing the power consumption by orders of magnitude at the device level.
- Alternative Class-AB OpAmps are investigated as active elements, trying to use energy only for dynamic transitions, thus reducing the power consumption at the circuit level.
- The circuits unused during a certain period of time are powered off, thus reducing the power consumption at the system level and minimizing the number of signal-path switching devices.
- The circuit reliability is improved by avoiding the use of bootstrapping techniques, which may shorten the operation life of integrated devices.
- The open-source programs are used whenever it is possible, bringing no limits in inspecting and modifying their code to meet special needs of this research.
- Scientific multi-programming-language environment is developed to remain independent from any closed computational environment.

In the scope of this thesis, low-power high-resolution $\Delta\Sigma$ modulators are explored. The anti-aliasing input analog filter and the decimation output digital filter are out of the scope of this work. As a core contribution, an attempt to improve the analog integrated-circuit design field is made. A high-FOM modulator test vehicle is obtained using a standard CMOS technology without clock bootstrapping nor calibration needs. Several applications, such as a high-precision industrial and scientific measurement or high-quality audio recording and processing, can benefit from the presented results.

High-Resolution ΔΣ Architectures | 2

This chapter explores the basic variations of ΔΣM architectures from the perspective of maximization of power efficiency and resolution at the system level.

First, the analysis of a ΔΣM basic structure based on only one integrator stage is performed and the fundamental property of its signal-versus-noise performance is discussed. Then, this structure is enhanced by introducing additional integrators.

The signal-headroom specifications of the integrator outputs are relaxed by introducing a feedforward path in the ΔΣM loop. This makes the design of integrators to not require low-voltage circuit techniques. The design of the ΔΣM quantizer is also simplified employing a single-bit implementation, which provides an inherent linearity and immunity to the quantizer systematic offset.

The equivalent analytical and behavioral models are used to study the trade-offs between the ΔΣM parameters and the effects of non-idealities. As a result, the design effort is reduced. The behavioral simulation of ΔΣM architectures and the extraction of the most important parameters is discussed in detail.

At the end of this chapter, the target specifications for the ΔΣM implemented in this PhD thesis are defined at the circuit level.

2.1 Modulator Selection Methodology

2.1.1 First-Order ΔΣM

The basic structure of a ΔΣM is shown in Fig. 2.1. The input signal $V_{\text{in}}(z)$ and the output signal $V_{\text{out}}(z)$ are the Z-transforms of the time-domain sampled input and output signals, respectively. The structure of Fig. 2.1 is called the first-order ΔΣM because only one integrator is used to implement the transfer function $H_1(z)$ of the discrete-time filter. Typically, taking into account a one-sample delay of the integrator:

$$H_1(z) = \frac{z^{-1}}{1 - z^{-1}}. \tag{2.1}$$

As will be shown below, the number of integrators can be increased, steepening the NTF and improving the resolution.

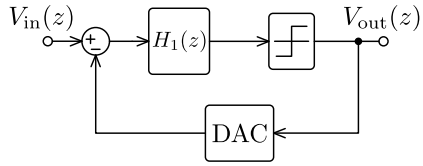

Figure 2.1 | First-order ΔΣM architecture.

Due to the quantization effects, the system of Fig. 2.1 is non-linear. In order to simplify its mathematical analysis, the quantizer and DAC blocks are replaced by their equivalent linear models as shown in Fig. 2.2 [27], where V_{qn} is the quantization-error signal and a_{q} is the quantizer gain.

The characteristic equation of the ΔΣM linear model of Fig. 2.2 can be found as:

$$V_{\text{out}}(z) = a_{\text{q}} H_1(z)\Big(V_{\text{in}}(z) - V_{\text{out}}(z)\Big) + V_{\text{qn}}(z). \tag{2.2}$$

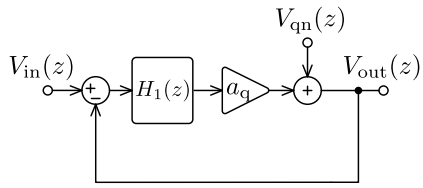

Figure 2.2 | Linear model of the first-order ΔΣM of Fig. 2.1.

Using (2.2), $V_{\mathrm{out}}(z)$ can be found as a function of $V_{\mathrm{in}}(z)$ and $V_{\mathrm{qn}}(z)$:

$$V_{\mathrm{out}}(z) = \frac{1}{1 + (a_{\mathrm{q}} H_1(z))^{-1}} V_{\mathrm{in}}(z) + \frac{1}{1 + a_{\mathrm{q}} H_1(z)} V_{\mathrm{qn}}(z). \tag{2.3}$$

Eq. (2.3) can be grouped as

$$V_{\mathrm{out}}(z) = \mathrm{STF}(z) V_{\mathrm{in}}(z) + \mathrm{NTF}(z) V_{\mathrm{qn}}(z). \tag{2.4}$$

Thus, from (2.3) and (2.4), it follows that the STF of the ΔΣM is

$$\mathrm{STF}(z) = \frac{1}{1 + (a_{\mathrm{q}} H_1(z))^{-1}}, \tag{2.5}$$

and the corresponding NTF is

$$\mathrm{NTF}(z) = \frac{1}{1 + a_{\mathrm{q}} H_1(z)}. \tag{2.6}$$

At this point, the fundamental property of the signal-versus-noise selectivity of ΔΣMs can be seen from (2.5) and (2.6). If the integrator is implemented so that it has a high gain in the signal band, the transfer functions in this band tend to: $\mathrm{STF}(z) \to 1$ and $\mathrm{NTF}(z) \to 0$. Therefore, increasing the gain of the integrator improves the resolution of the ΔΣM.

2.1.2 *L*th-order ΔΣM.

Employing first-order ΔΣMs, modest-resolution ADCs can be obtained [22]. To achieve high-resolution features, P_ε can be minimized only by means of an excessive OSR increase, as the resolution improves at a moderate rate of 1.5-bit/octave [53]. This problem is solved by introducing the additional integrators $H_{2-\mathrm{L}}$ in the filter loop as shown in the diagram of Fig. 2.3 for an L^{th}-order ΔΣM. The gain coefficients $a_{1-\mathrm{L}}$ are included to prevent the integrators from overloading and to ensure the loop stability. In this case, the number of bits added to the resolution by doubling the OSR is given by $L+0.5$ [27], making high-order ΔΣMs attractive for high-resolution and low-OSR ADCs. In practice, increasing the loop order, the loop stability is weakened in front of gain-coefficient mismatch due to technology process deviations. This hinders the implementation of the ΔΣMs with a loop order higher than 5 and requires careful robustness verification even for lower-order ΔΣMs.

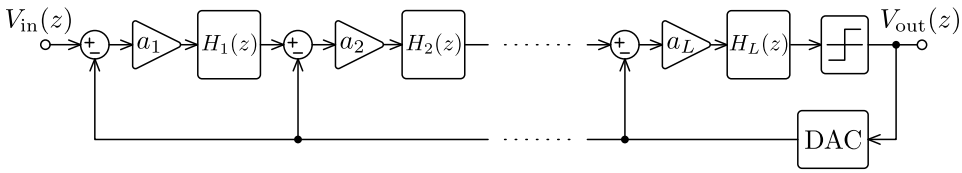

Figure 2.3 | L^{th}-order single-loop ΔΣM architecture.

The multi-stage noise-shaping (MASH) architectures are not discussed here because they suffer from analog integrator non-idealities in a similar way as the pipeline ADCs discussed in Chapter 1.

2.1.3 Feedforward ΔΣM

As illustrated in Fig. 2.4, a feedforward path can be incorporated in the basic ΔΣM scheme of Fig. 2.1 to relax signal headroom specifications of the integrator output [72].

Replacing the quantizer and DAC blocks by their equivalent linear models,

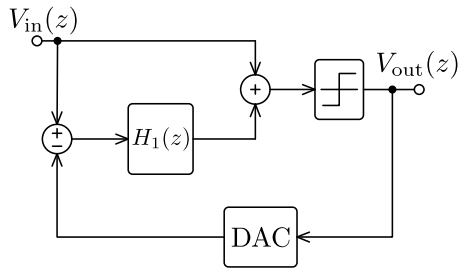

Figure 2.4 | First-order feedforward ΔΣM architecture.

as in Fig. 2.2, the analysis of Fig. 2.4 provides:

$$\text{STF}(z) = 1, \tag{2.7}$$

$$\text{NTF}(z) = \frac{1}{1 + a_{\text{q}} H_1(z)}. \tag{2.8}$$

Comparing (2.7) with (2.5), it can be noted that the STF of the feedforward ΔΣM is improved, while the NTF of (2.8) remains the same as in (2.6). The main advantage of this ΔΣM type is that its integrator only processes the quantization-error signal, whose amplitude is smaller than that of the input signal. Therefore, the integrator design becomes a less challenging task in terms of low-voltage operation.

A similar approach of inserting additional integrator stages, as in Fig. 2.3, can be applied to the first-order feedforward ΔΣM of Fig. 2.4. The resulting L^{th}-order feedforward ΔΣM is shown in Fig. 2.5. In contrast with Fig. 2.3, a single negative feedback path is enough to ensure the loop stability, which simplifies the feedback-DAC implementation. The feedforward-path coefficients $c_{1-\text{L}}$ are incorporated for the summation-operation control before the quantizer.

Given the same L^{th} order, the feedforward ΔΣM topology of Fig. 2.5 is more power efficient than that of Fig. 2.3 [73]. This is due to two main reasons: the relaxation of the specifications of the integrator amplifiers and the reduction of the sampling components following the first integrator.

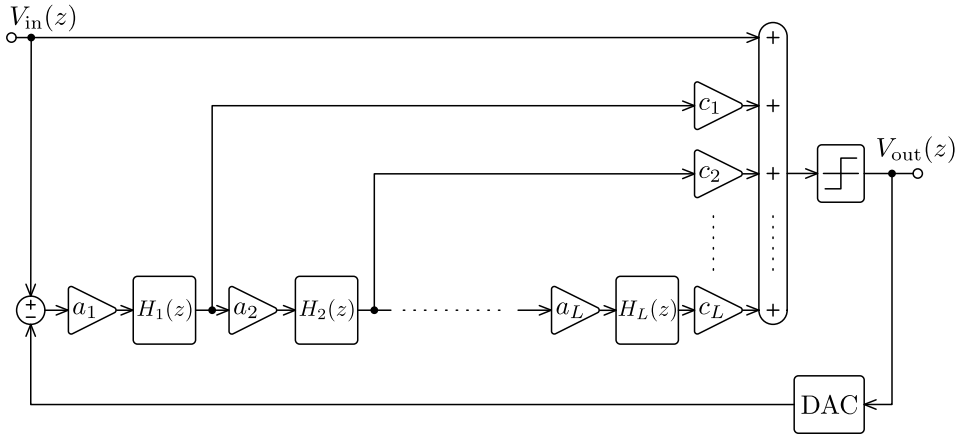

Figure 2.5 | L^{th}-order feedforward ΔΣM architecture.

2.2 Single-Bit versus Multi-bit Quantization

The ΔΣM architecture is selected for the ADC development in this PhD thesis because of its robustness in achieving high-resolution features by increasing the loop order, while needing moderate OSR values. Following the discussion on the basic types of ΔΣMs in the previous section, the feedforward variation in Fig. 2.5 is chosen due to its power efficiency.

The power of the in-band noise P_{ε} can be further attenuated by increasing the number of quantizer levels, whose ENOB is ideally added to the resolution of the whole ΔΣM. However, in circuit implementations where the number of quantizer bits is higher than one, several issues appear. One of them is the loop performance degradation caused by the non-linearity in the multi-bit quantization and the feedback-DAC operation. This makes multi-bit ΔΣMs to require additional techniques such as calibration or dynamic element matching (DEM) [46], resulting in increased integration area, manufacturing costs, power consumption and design effort. In contrast, single-bit ΔΣMs avoid these problems due to an inherent linearity of the quantizer, as shown in Fig. 2.6 for the transfer curve and the error function of a single-bit quantizer. Here, V is the analog input voltage without a clearly defined full scale, if compared to the transfer curve of a multi-bit

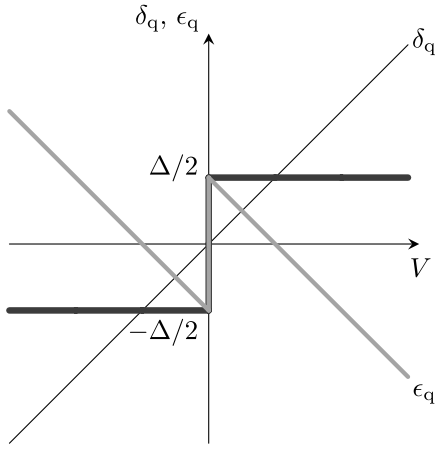

Figure 2.6 An example of the transfer curve and the error function of a single-bit quantizer.

quantizer of Fig. 1.2, and δ_q is the quantized output. Only one quantization step Δ is present and this is the source of an additional immunity to the quantizer systematic offset [6]. Thus, the design of the quantizer can be relaxed because no preamplifier is needed to reduce the input-referred offset. As a result, the speed of the single-bit quantizer can be increased, which is especially important in feedforward $\Delta\Sigma$Ms.

The feedforward path introduces timing constraint issues, especially in multi-bit implementations [74], where an active adder before the quantizer is needed to adapt the quantizer input scale. If a single-bit quantizer is chosen, the adder can be build using passive components, as the signal attenuation is of low importance, following from the nature of single-bit quantization discussed above.

Multi-bit $\Delta\Sigma$Ms are useful in wide-band ADCs because they allow to reduce the OSR values. However, in high-resolution designs this may cause an undesired size increase of the sampler elements, whose sizing methodology will be discussed in the next section and practical implementation will be presented in Chapter 4.

It can be concluded from this section that, when low integration area and

power consumption are desired and lower bandwidth is acceptable, a single-bit high-order feedforward ΔΣM is of optimum choice in order to maximize resolution.

2.3 Modeling of Circuit Non-Idealities

The transistor-level simulations of complete ΔΣM circuits tend to consume an important amount of CPU time [75, 76]. If they are required at the initial stages of the design, the development of a ΔΣM takes longer and costs more effort than in the case when equivalent analytical and behavioral-simulation ΔΣM models can be used instead. These models prove to be suitable in selecting the ΔΣM architecture and most important parameters to comply with specifications. They can also be employed to model the circuit non-idealities.

2.3.1 Quantization Noise

As it has been explained above, the mathematical analysis of a ΔΣM is a complex task due to its non-linear nature. Other analytical difficulties arise from the ΔΣM dynamic properties because of the memory of the integrators. To solve this problem, a behavioral simulation can be performed in the discrete-time domain, which is well-suited for the modeling of uniform-sampling systems such as SC ΔΣM. Fig. 2.7 shows a second-order feedforward ΔΣM. If a single-bit quantizer is selected, the behavior of this ΔΣM can be modeled using a simple flow illustrated in Fig. 2.8. Here, V_{in} is employed as a sine-wave test signal of the frequency f_{in}, which is normally chosen to be lower than BW/3 to allow evaluation of the distortion at the second and third harmonics. Therefore, the number of samples to be simulated n_{samp} is defined as

$$n_{\text{samp}} = n_{\text{p}} \cdot \text{OSR} \frac{2 \cdot \text{BW}}{f_{\text{in}}}, \tag{2.9}$$

where n_{p} is the number of sine-wave periods of V_{in}. The PSD of the obtained V_{out} sequence is estimated by the use of the Fast Fourier Transform (FFT).

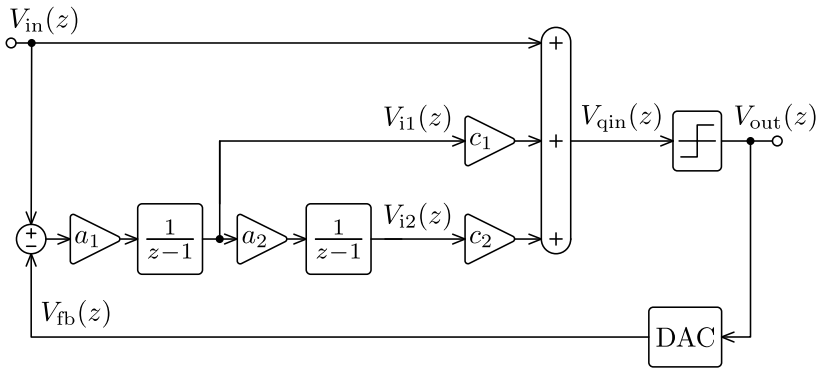

Figure 2.7 | Second-order feedforward ΔΣM.

An example of the output spectrum of the ΔΣM high-level model of Fig. 2.7, with $a_1 = 0.3$, $a_2 = 0.7$, $c_1 = 2$ and $c_2 = 1$ from [77], is shown in Fig. 2.9 for a -6-dB_{FS} 13.28-kHz sinusoidal input at a 13.6-MHz f_{s} and employing a 64-period n_{p}. The signal-to-quantization-noise ratio (SQNR) is calculated in dB using

$$\text{SQNR} = 10 \log \frac{P_{\text{s}}}{P_{\varepsilon}}, \tag{2.10}$$

where P_{s} is the signal power and P_{ε} is the in-band noise power. For the case of Fig. 2.9, if a BW of 50 kHz is required, (2.10) provides an SQNR of 85.9 dB, and the OSR is 136 according to (1.5).

Iteratively, the SQNR is evaluated for a range of the V_{in}-amplitude values. Fig. 2.10 plots the results of this sweep for the same ΔΣM high-level model of Fig. 2.7. It can be seen that the maximum SQNR value SQNR_{max} is not located at the full-scale input (0 dB_{FS}). This is due to the intrinsic ΔΣM-loop overload. The dynamic range (DR) of the ΔΣM is evaluated as ratio between the maximum input-signal power for which the SQNR is degraded by -3 dB and the minimum detectable input-signal power [77]. Increasing the feedback-DAC gain coefficient a_{fb} shifts SQNR_{max} closer to the full-scale input value of V_{in}. However it may result in the DR loss if the -3-dB SQNR limit is surpassed.

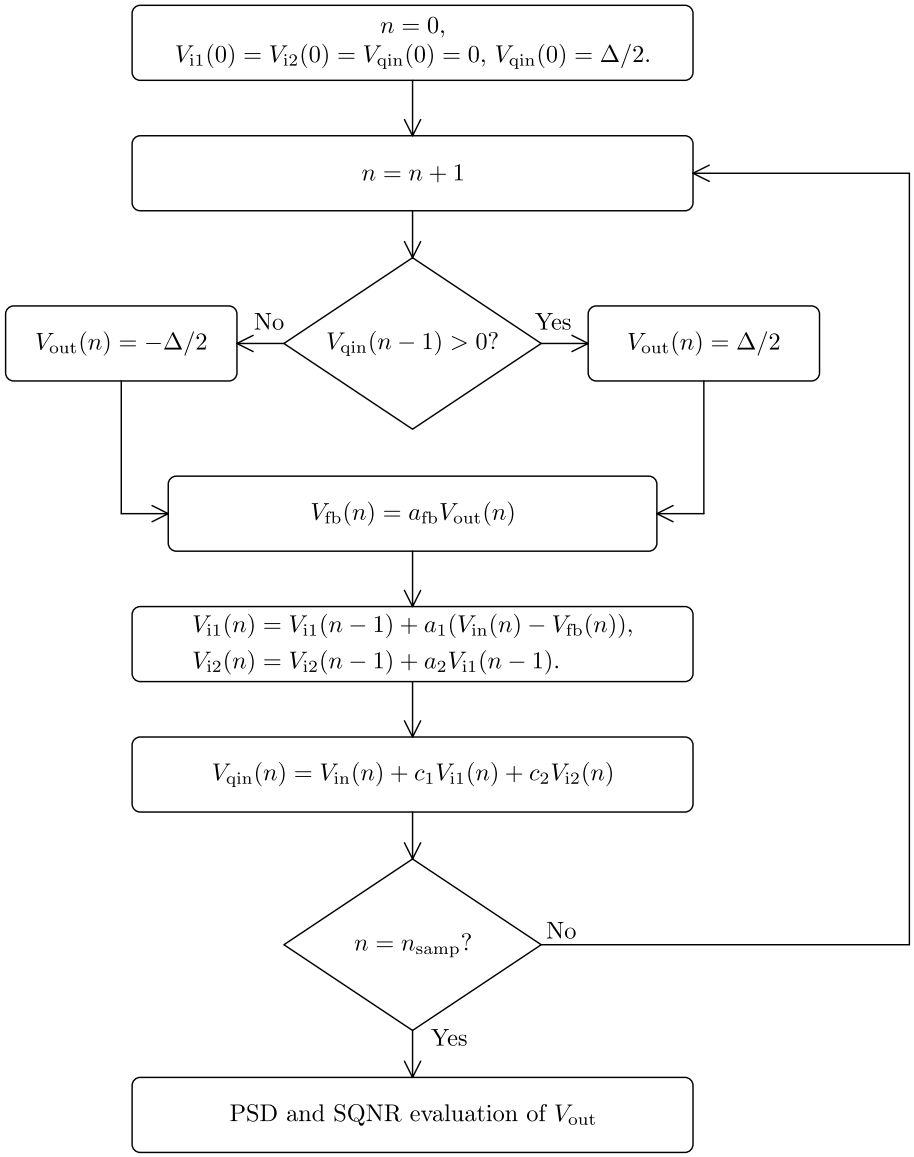

Figure 2.8 | Flow diagram for the behavioral modeling of the second-order feedforward ΔΣM of Fig. 2.7.

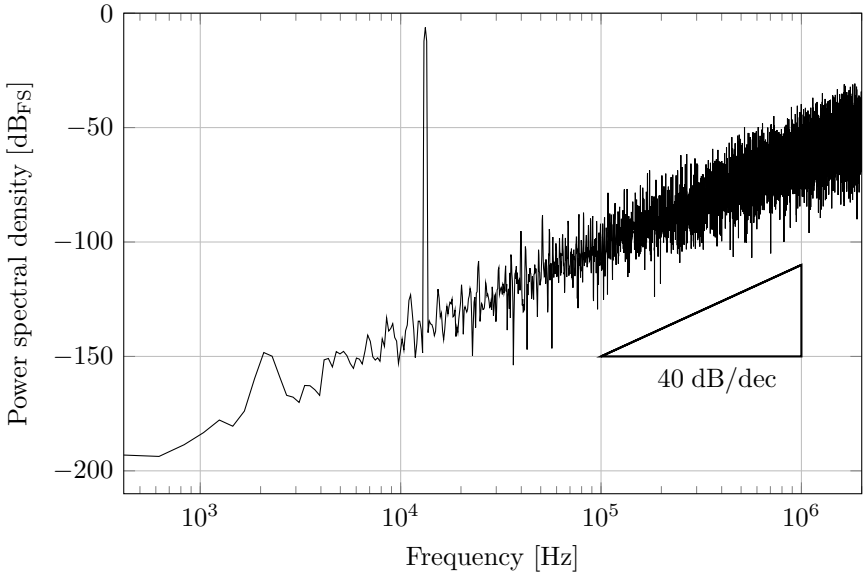

Figure 2.9 | Output spectrum of the ΔΣM high-level model of Fig. 2.7 for a -6-dB_{FS} 13.28-kHz sinusoidal input.

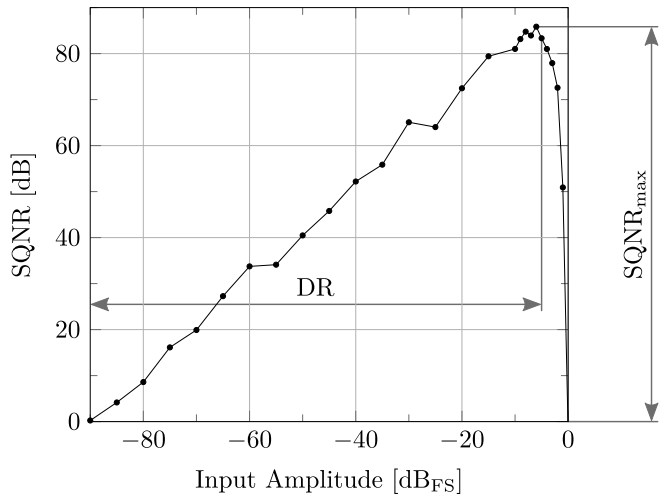

Figure 2.10 | Simulated SQNR versus input amplitude of the ΔΣM high-level model of Fig. 2.7.

The behavioral-simulation flow of Fig. 2.8 can be enhanced to include the effects of the ΔΣM component non-idealities as will be shown below. In order to discern the effects of each non-ideality on the ΔΣM performance, the non-idealities are modeled separately or in small groups derived from the same ΔΣM component.

As it has been already explained in Chapter 1, SC implementation for ΔΣMs is preferred over continuous-time implementation in this PhD thesis since a very robust ADC is persued. Thus, the discussed modeling will continue to be concerned with SC ΔΣMs only. In order to maximize the noise rejection, a fully-differential implementation of ΔΣM circuits will be also assumed in what follows.

2.3.2 Sampling Thermal Noise

The capacitors of a SC sampler act as a filter of the thermal noise produced by the switch resistance [78]. This noise is limited in band by the time-constant of the equivalent RC circuit and, thus, its total power does not depend on the equivalent resistor value, but on the sampling capacitor value C_{s}, the OSR and the absolute temperature T. This imposes minimum-size limits on the sampling capacitors, once the ΔΣM OSR and resolution are fixed by design. For a fully differential implementation, the input capacitor value is [27]:

$$C_{\mathrm{s1}} = \frac{2k_{\mathrm{B}}T}{\overline{V_{\mathrm{n}}^2} \cdot \mathrm{OSR}}. \tag{2.11}$$

Here, $\overline{V_{\mathrm{n}}^2}$ is the maximum allowed noise power:

$$\overline{V_{\mathrm{n}}^2} = \frac{\overline{V_{\mathrm{s}}^2}}{10^{(\mathrm{SNR_t}+\mathrm{SNR_m})/10}}, \tag{2.12}$$

where $\overline{V_{\mathrm{s}}^2}$ is the maximum signal power, $\mathrm{SNR_t}$ is the required ΔΣM signal-to-noise ratio (SNR) and $\mathrm{SNR_m}$ is the safe SNR margin in dB.

The sizing of C_{s1} of the first integrator does not depend on the ΔΣM architecture because C_{s1} is located outside the ΔΣM closed signal loop. Nev-

ertheless, due to the noise suppression at each ΔΣM stage, the sampling capacitors of the following integrator stages $i > 1$ can be scaled down according to [73]:

$$C_{si} = C_{s1} \frac{\pi^{2i-2}}{\mathrm{OSR}^{2i-2}\,(2i-1)} \prod_{k=2}^{i} \frac{1}{a_{k-1}^2}. \tag{2.13}$$

Fig. 2.11 shows an example of the output spectrum of the ΔΣM high-level model of Fig. 2.7 with and without sampling thermal noise, for the same -6-$\mathrm{dB_{FS}}$ 13.28-kHz sinusoidal input at a 13.6-MHz f_s. It can be observed that the high-frequency part of the spectrum is preserved, but, in the case of accounting the sampling thermal noise, a noise floor is added to the low-frequency portion of the spectrum. Increasing C_{s1} lowers this noise floor

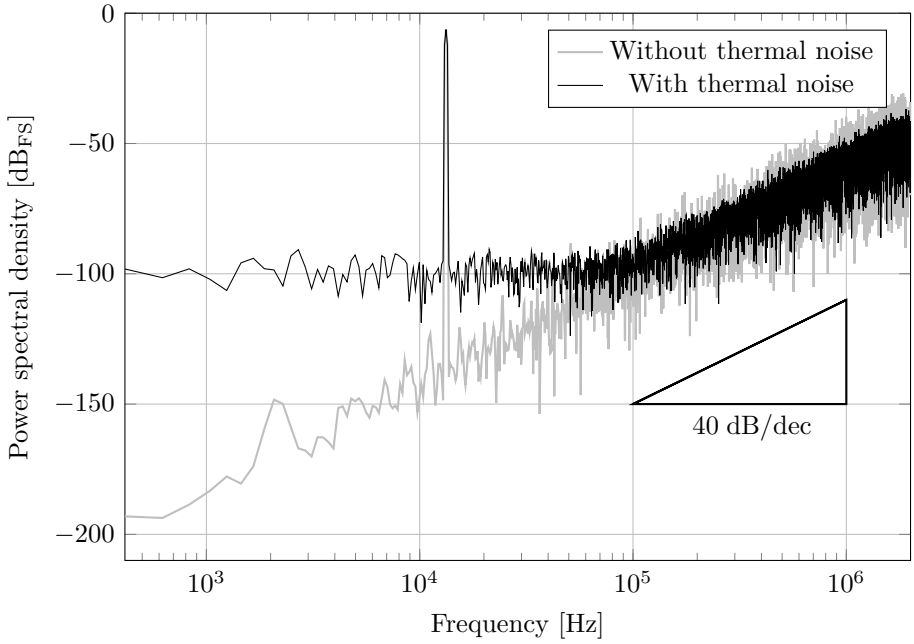

Figure 2.11 Output spectrum of the ΔΣM high-level model of Fig. 2.7 for a -6-$\mathrm{dB_{FS}}$ 13.28-kHz sinusoidal input with and without sampling thermal noise.

moving the corner frequency (where the quantization and thermal noise are of the same order) leftwards and downwards, but at the same time increases the amount of charge to be transferred per sample and, hence, the total power consumption. Thus, the optimum corner frequency is found in the vicinity of the ADC BW frequency.

2.3.3 Component Mismatch

Integrated circuit components are subject to their characteristic modifications due to technology process variations. As a result, gain coefficients also vary with respect to those defined by high-level design, and the stability of a ΔΣM is more difficult to ensure when increasing loop order.

It is proposed to verify the robustness of a ΔΣM using behavioral simulation. Using the example of the second-order ΔΣM of Fig. 2.7, its stability can be tested under different coefficient-mismatch conditions, as listed in Table 2.1. For a given worst-case coefficient mismatch ϵ_{mism}, as there are 4 coefficients, $2^4 = 16$ combinations are needed to include the minimum and maximum values of each coefficient.

In each new case, the coefficient values $a_{1,\mathrm{r}}$, $a_{2,\mathrm{r}}$, $c_{1,\mathrm{r}}$ and $c_{2,\mathrm{r}}$ are updated according to the corresponding row of the Table 2.1 and are used instead of a_1, a_2, c_1 and c_2 in the flow of Fig. 2.8. Thus, 16 input-amplitude sweeps must be performed and the worst $\mathrm{SQNR}_{\mathrm{max}}$ ($\mathrm{SQNR}_{\mathrm{max,worst}}$) is provided as a result. Fig. 2.12 plots an example of this sweep for the ΔΣM high-level model of Fig. 2.7 with ϵ_{mism}=5 %. As a result, the obtained $\mathrm{SQNR}_{\mathrm{max,worst}}$ is 83.5 dB. In the case of higher-order ΔΣMs with an increased number of coefficients, randomly chosen variations can be employed using Monte Carlo simulations, which are also useful for the estimation of the integrated-circuit manufacturing yield.

2.3.4 Integrator Settling Error

The settling error at the outputs of the integrators ϵ_{sett} is due to several non-idealities such as integrator amplifier finite gain, limited bandwidth and slew rate. This error is treated here as a random noise and it has been

Case	$a_{1,r}$	$a_{2,r}$	$c_{1,r}$	$c_{2,r}$
0	a_1	a_2	c_1	c_2
1	$a_{1,\min}$	$a_{2,\min}$	$c_{1,\min}$	$c_{2,\min}$
2	$a_{1,\max}$	$a_{2,\min}$	$c_{1,\min}$	$c_{2,\min}$
3	$a_{1,\min}$	$a_{2,\max}$	$c_{1,\min}$	$c_{2,\min}$
4	$a_{1,\max}$	$a_{2,\max}$	$c_{1,\min}$	$c_{2,\min}$
5	$a_{1,\min}$	$a_{2,\min}$	$c_{1,\max}$	$c_{2,\min}$
6	$a_{1,\max}$	$a_{2,\min}$	$c_{1,\max}$	$c_{2,\min}$
7	$a_{1,\min}$	$a_{2,\max}$	$c_{1,\max}$	$c_{2,\min}$
8	$a_{1,\max}$	$a_{2,\max}$	$c_{1,\max}$	$c_{2,\min}$
9	$a_{1,\min}$	$a_{2,\min}$	$c_{1,\min}$	$c_{2,\max}$
10	$a_{1,\max}$	$a_{2,\min}$	$c_{1,\min}$	$c_{2,\max}$
11	$a_{1,\min}$	$a_{2,\max}$	$c_{1,\min}$	$c_{2,\max}$
12	$a_{1,\max}$	$a_{2,\max}$	$c_{1,\min}$	$c_{2,\max}$
13	$a_{1,\min}$	$a_{2,\min}$	$c_{1,\max}$	$c_{2,\max}$
14	$a_{1,\max}$	$a_{2,\min}$	$c_{1,\max}$	$c_{2,\max}$
15	$a_{1,\min}$	$a_{2,\max}$	$c_{1,\max}$	$c_{2,\max}$
16	$a_{1,\max}$	$a_{2,\max}$	$c_{1,\max}$	$c_{2,\max}$

Table 2.1 Gain coefficients generated for the mismatch-sensitivity test of the second-order feedforward ΔΣM of Fig. 2.7. The minimum and maximum coefficient values are obtained from the nominal coefficient values $\mp\epsilon_{\text{mism}}$, respectively.

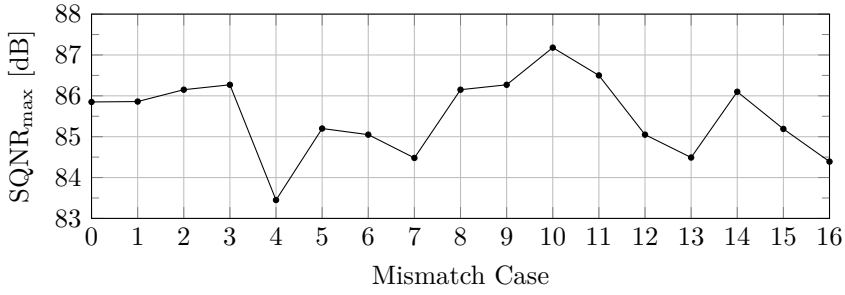

Figure 2.12 Simulated $\text{SQNR}_{\max}$ versus coefficient-mismatch cases of Table 2.1 for the ΔΣM high-level model of Fig. 2.7 with ϵ_{mism}=5 %.

modeled using the behavioral-simulation flow proposed above by adding this noise contribution at the outputs of the integrators. For the example of the second-order ΔΣM of Fig. 2.7, the modeling of the integrator outputs $V_{\mathrm{i}1-2}$ will be modified with respect to that of Fig. 2.8 as

$$\begin{aligned} V_{\mathrm{i}1}(n) &= V_{\mathrm{i}1}(n-1) + a_1(V_{\mathrm{in}}(n) - V_{\mathrm{fb}}(n)) + V_\epsilon(n), \\ V_{\mathrm{i}2}(n) &= V_{\mathrm{i}2}(n-1) + a_2 V_{\mathrm{i}1}(n-1) + V_\epsilon(n), \end{aligned} \tag{2.14}$$

where $V_\epsilon(n)$ is a random noise signal generated with uniform distribution between $-\epsilon_{\mathrm{sett}}$ and ϵ_{sett}. In Chapter 4, it will be shown how this type of modeling is used to determine the maximum ϵ_{sett} allowed at the outputs of the integrators, for which the required ΔΣM performance is preserved.

2.4 External Non-Idealities

Several non-idealities extrinsic to the ΔΣM circuit itself, but which degrade its performance, must be taken into account when designing the biasing and communicaton interface circuits.

Jitter noise is due to uncertainties in the sampling-clock transitions σ_{j} and considerably degrades the performance of ΔΣM ADCs if its resulting in-band power P_{j} injected at the input S/H is higher than the in-band noise power of other intrinsic contributions. For given ΔΣM OSR, BW and maximum input-signal power $\overline{V_{\mathrm{s}}^2}$, P_{j} can be expressed as a function of σ_{j} [79]:

$$P_{\mathrm{j}} = \frac{\overline{V_{\mathrm{s}}^2}}{8} \frac{(2\pi \cdot \mathrm{BW} \cdot \sigma_{\mathrm{j}})^2}{\mathrm{OSR}}. \tag{2.15}$$

Eq. (2.15) is recalled in Chapter 5 to select the clock generator for the laboratory setup, which is build to test the ΔΣ ADC developed in this PhD thesis.

The real voltage sources employed as analog references for the feedback DAC must present an in-band noise lower than that of the ΔΣM intrinsic contributions. Thus, the performance of the ΔΣM is not degraded. The analog and digital supplies are preferred to be decoupled using separate

rails. If large noise-decoupling capacitors cannot be integrated on chip, they must be placed externally as close as possible to the ΔΣM pins. The generation of low-noise references and supply voltages for test purposes will be discussed in Chapter 5, as well as the on-package noise decoupling.

2.5 Target Specifications

This PhD thesis targets the Schreier FOM expressed by (1.9). The ΔΣM BW is selected to 50 kHz to cover most of the practical smart-sensing applications. Therefore to achieve a high FOM, the SNDR is to be maximized and the power consumption P to be minimized. The target ENOB is 16 bits, which corresponds to an SNDR of 98 dB according to (1.8), and the wanted static power consumption is sought to be smaller than 10 mW.

Additional restrictions are self-imposed to reduce the ΔΣM manufacturing costs and integration area. They are:

1. Circuit integration using a standard CMOS technology only.
2. No bootstrapping or other techniques which may increase the operation voltages beyond the nominal supply levels of the target technology.
3. No calibration during manufacturing process.
4. No digital post compensation when in normal operation.

In Chapter 3, the design of the integrator amplifier will be explored and it will lead to the definition of the input full-scale for the entire ΔΣM in the following Chapter 4.

The minimum OSR is chosen to be 136, which sets the maximum sampling-capacitor size allowed by the available integration area, according to (2.11).

The second-order ΔΣM of Fig. 2.7, operated at an OSR of 136, provides and SQNR of 85.9 dB, which is far from the target 98 dB plus a 15-dB margin, which is commonly employed in industrial designs [27]. To improve the resolution of this ΔΣM, values of three parameters can be increased:

1. OSR.
2. Number of quantizer bits.
3. Loop order.

The OSR increase, conducting to high sampling frequencies, is limited as the parasitics of the components also increase their contributions to the circuit non-idealities. This results in difficulties in achieving circuit operation precision and is associated with the loss of power efficiency. The multi-bit quantizer implementations are discarded because they introduce a number of issues, discussed in Section 2.2. Finally, the only way to improve the ΔΣM resolution left is to increase the loop order. As it will be shown in Chapter 4, a forth-order single-bit feedforward architecture is capable of achieving an SQNR of 117 dB operated at the same 136 OSR.

Low-Power CMOS Switched-Capacitor ΔΣM Circuits

3

This chapter introduces novel CMOS circuits specifically developed for low-power SC ΔΣMs and other techniques used to achieve a high-precision operation at the same time as a low-current consumption and a low sensitivity to both technology and temperature deviations, which may undermine the circuit reliability.

The first section contains a theoretical framework used in the circuit development. The EKV [37] and ACM [38] MOSFET-model equations are presented, covering all regions of the device operation. The ACM-model equations are written using the EKV-model notation for the purpose of unification.

The second section introduces a new family of Class-AB single-stage OpAmp circuits based on variable-mirror amplifiers (VMAs) [29] using dynamic-ratio current mirrors with a partial positive-feedback loop. The proposed architecture is characterized by generating all Class-AB currents in the output transistors only without affecting the polarization of the input differential pair. It exhibits low sensitivity to technology and temperature variations. Since it is based on a single-stage topology, the amplifier is autocompensated by the load capacitors without the need for any extra compensation devices.

In the last section, the developed continuous-time Class-AB single-stage OpAmp is transformed into a SOA for SC applications, focusing on the operation precision. Issues such as charge injection at the switch level are analyzed and solutions are proposed. Additional circuits for a fast on-off operation and a high open-loop DC gain are presented.

3.1 Advanced Analog MOSFET Modeling

MOSFET modeling is a complex topic far beyond the scope of this thesis. Thus, this section resumes the most important aspects of the employed theoretical framework.

A several-decade process of slight changes in the existing MOSFET models has yielded them inappropriate for the circuit design in the present due to complex equations describing the MOSFET behavior, excessive number of parameters and lack of physical meaning of these parameters [37, 38]. In this sense, the EKV and ACM models are the result of a new approach to the problem of the MOSFET modeling, connecting real physics with the former semi-empirical models.

In modern analog circuits, biasing simple amplifier stages near the weak- or moderate-inversion region leads to maximum voltage gain, low device dissipation, and minimum total harmonic distortion [80]. The square-law variation of the MOSFET drain current I_{D} with the gate-to-source voltage V_{GS} has been traditionally used to describe the MOSFET behavior in saturation and strong inversion [81]:

$$I_{\mathrm{D}} = \frac{1}{2}\mu C_{\mathrm{ox}} \frac{W}{L} \left(V_{\mathrm{GS}} - V_{\mathrm{T0}}\right)^2 \left(1 + \lambda V_{\mathrm{DS}}\right). \tag{3.1}$$

Here V_{T0} is the threshold voltage, V_{DS} is the resulting drain-to-source voltage, λ is the channel-length modulation, μ is the mobility of charge carriers in the channel, C_{ox} is the oxide capacitance per unit area, W and L are the effective width and length of the channel, respectively.

Because (3.1) assumes I_{D} to be zero when V_{GS} is less than V_{T0}, it cannot be employed in the weak- or moderate-inversion region. Even for small

positive $V_{GS} - V_{T0}$ values, it presents significant accuracy issues. The EKV and ACM models solve these problems and offer other useful features such as continuous transition from saturation to linear mode and symmetry between the source and drain terminals. According to these all-region models,

$$I_D = I_F - I_R, \tag{3.2}$$

where I_F and I_R is the forward and reverse saturation currents, respectively. In order to numerically evaluate the level of inversion, the inversion coefficients for the forward saturation IC_F and the reverse saturation IC_R are introduced and defined by

$$IC_{F,R} = \frac{I_{F,R}}{I_{spec}}. \tag{3.3}$$

Here, I_{spec} is the specific current

$$I_{spec} = 2n\beta {U_T}^2, \tag{3.4}$$

where n is the slope factor, $\beta = \mu C_{ox} \frac{W}{L}$ is the transfer parameter, and U_T is the thermal voltage defined by

$$U_T = \frac{k_B T}{q}. \tag{3.5}$$

Here, $k_B = 1.38 \times 10^{-23}$ J/K is the Boltzmann constant, T is the absolute temperature, and $q = 1.6 \times 10^{-19}$ C is the elementary positive charge.

If $IC_{F,R} \gg 1$, it is said that the forward- or reverse-saturation component is in strong inversion; if $IC_{F,R} \approx 1$, it is in moderate inversion; and, if $IC_{F,R} \ll 1$, it is in weak inversion.

3.1.1 Strong Inversion

The EKV model expresses (3.2) for the MOSFET device in linear mode and strong inversion,where $V_G > V_{T0}$ and the channel is fully depleted, as

$$\begin{aligned} I_D &= \frac{\beta}{2n}\left[\overbrace{(V_G - V_{T0} - nV_S)^2}^{\text{Forward component}} - \overbrace{(V_G - V_{T0} - nV_D)^2}^{\text{Reverse component}}\right] \\ &= \beta\left[V_G - V_{T0} - \frac{n}{2}(V_D + V_S)\right](V_D - V_S), \end{aligned} \tag{3.6}$$

where V_G, V_S, V_D are the gate-, source- and drain-terminal voltages referred to the substrate, respectively. Eq. (3.6) clearly identifies the forward and reverse components.

In forward saturation, the reverse current I_R can be neglected, thus, from (3.2), $I_D = I_F$. Consequently, (3.6) becomes

$$I_D = \frac{\beta}{2n}(V_G - V_{T0} - nV_S)^2. \tag{3.7}$$

3.1.2 Weak Inversion

Similarly, for the device in linear mode and weak inversion, where no channel is formed and the diffusion of carriers is the only means providing a relatively small current, the EKV model provides

$$I_D = I_{spec} e^{\frac{V_G - V_{T0}}{nU_T}}\left(e^{-\frac{V_S}{U_T}} - e^{-\frac{V_D}{U_T}}\right). \tag{3.8}$$

Eq. (3.8) accepts V_G values lower than V_{T0}, producing valid results in the weak-inversion region. In forward saturation, (3.8) is simplified as

$$I_D = I_{spec} e^{\frac{V_G - V_{T0}}{nU_T}} e^{-\frac{V_S}{U_T}}. \tag{3.9}$$

The forward-saturation inversion coefficient from (3.3) is reduced to

$$IC = \frac{I_D}{I_{spec}}. \tag{3.10}$$

3.1.3 All-Region Approximation

Although (3.6) and (3.8) provide good approximation in the strong- and weak-inversion regions, they fail to cover the moderate-inversion region, where many devices can find the best trade-off between their parameters. The ACM model deals with this issue and offers an expression, which relates the MOSFET terminal voltages and inversion coefficients in all regions of MOSFET operation [82, 83]. It is reported here using the EKV notation as

$$\frac{V_{\mathrm{G}} - V_{\mathrm{T0}} - nV_{\mathrm{S,D}}}{nU_{\mathrm{T}}} = \sqrt{1 + 4\mathrm{IC}_{\mathrm{F,R}}} - 2 + \ln\left(\sqrt{1 + 4\mathrm{IC}_{\mathrm{F,R}}} - 1\right). \quad (3.11)$$

In manual analysis of complex circuits, the use of (3.11) may may result in cumbersome equations, however it proves useful in simple-circuit research such as biasing of the OpAmp cascode transistors, which will be discussed in the next section.

3.2 Variable-Mirror Amplifier Family

This section introduces a new family of Class-AB OpAmp circuits, which are based on single-stage topologies with variable current mirrors called variable-mirror amplifiers (VMAs) [29]. The proposed topology allows investing all Class-AB dynamic peak currents in the output transistors only. In addition to the inherent power savings, this single-stage design approach avoids the need for any internal compensation, resulting in low-current and low-area overheads, multi-decade load-capacitance capability, and compatibility with SOA fast on-off operation in low-voltage SC circuits. From the manufacturing and operation-condition viewpoints, the proposed topology does not introduce any dependency on technology-parameter and temperature variations. This is of special interest when designing in deep-submicron CMOS technologies. The introduced Class-AB principle can be extended to a wide range of device operating conditions.

3.2.1 Single-Stage Class-AB Architecture

The proposed VMA architecture is shown in Fig. 3.1. All MOSFET bulk terminals are connected to their respective supply rail and are hidden for simplicity. The input transconductor consists of two complementary differential pairs, splitting the input signal into two paths for a separate Class-AB control of NMOS and PMOS output transistors. The dynamic current mirrors, boxed in Fig. 3.1, are the core of the novel OpAmp. They can be understood as fully-differential V_{cp} and V_{cn} voltage-controlled current amplifiers, where the differential input current is represented by the $(I_{\mathrm{inp}}, I_{\mathrm{inn}})$ pair, while the differential output current is represented by the $(I_{\mathrm{onp}}, I_{\mathrm{onn}})$ pair (for the NMOS paths). Their gain is dynamically and symmetrically changed by a cross-coupled partial positive local feedback, which is created by introducing the V_{cp} dependence on I_{inn} and the V_{cn} dependence on I_{inp}.

To improve the open-loop voltage gain A_{open}, cascode transistors are inserted in the OpAmp output branches. The optimum biasing of these stacked devices for a maximum output voltage full scale will be discussed in Section 3.2.4. Finally, for fully-differential applications, the control of the common-mode feedback (CMFB) is introduced through the tail bias current of the NMOS-input transconductor (I_{cmfb}), whose SC implementation will be presented in Section 3.3.

The VMA architecture of Fig. 3.1 features two main advantages. First, there is no need for Miller-compensation capacitors, resulting in silicon-area reduction and operation-speed improvement at the same time. Second, only the output-branch transistors are actually draining high-peak Class-AB currents, while the rest of the OpAmp devices are operated in Class-A, with the consequent benefits in terms of dynamic-to-static power consumption ratios.

For simplicity, the equations only for the NMOS paths will be discussed below. The PMOS-path behavior is symmetric, and its equations can be easily derived using the same methodology from the developed NMOS-path analysis. All transistors enclosed in a box are matched devices and use the same unitary element, but owning specified multiplicities, like the transistors with the multiplicities A and B in Fig. 3.1.

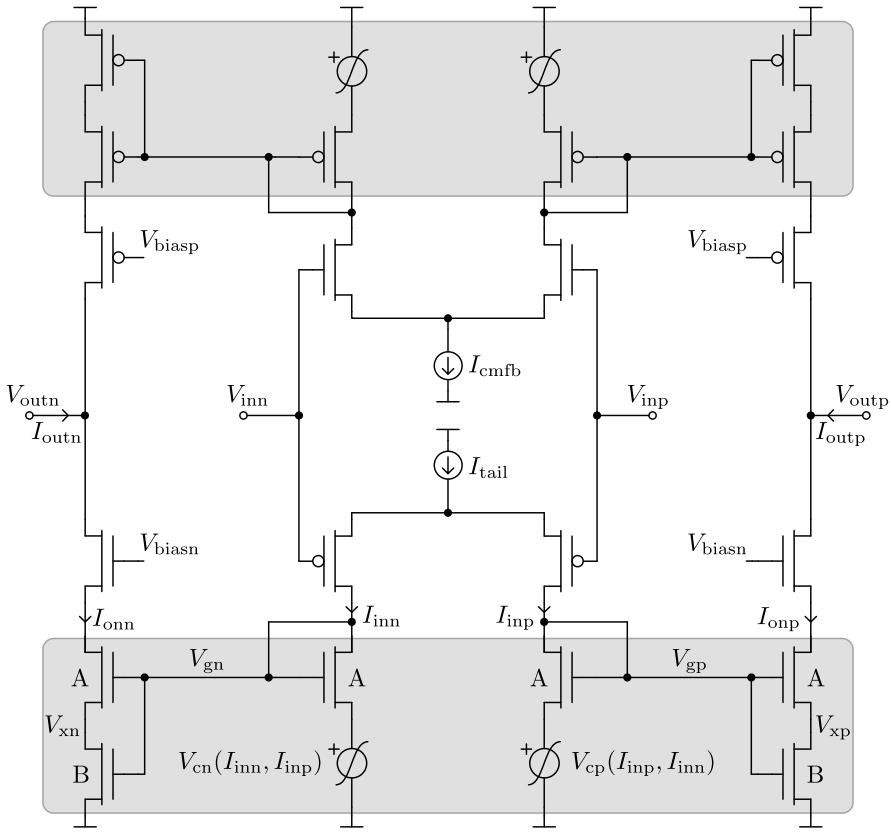

Figure 3.1 | Proposed Class-AB single-stage OpAmp architecture for the VMA family.

For all circuits presented in this section, the A-sized transistors are supposed to be in saturation, and the B- and C-sized transistors are supposed to be operated in linear mode. The analysis of each circuit will be performed twice using two different assumptions: the first, supposing all transistors operating in strong inversion; and the second, supposing all transistors operating in weak inversion. This approach will help to predict the circuit behavior in the intermediate moderate-inversion region, which will be of interest in the next chapter.

In the case of the NMOS positive path, the desired Class-AB behavior of

the variable-gain current mirrors boxed in Fig. 3.1 is

$$\begin{cases} I_{\text{outp}} \equiv 0 & V_{\text{cp}} \equiv V_{\text{xp}} & I_{\text{onp}} \equiv I_{\text{inp}} \equiv \frac{I_{\text{tail}}}{2} & \text{Bias point,} \\ I_{\text{outp}} \not\equiv 0 & V_{\text{cp}} \not\equiv V_{\text{xp}} & \begin{cases} I_{\text{onp}} \ll I_{\text{inp}} \\ I_{\text{onp}} \gg I_{\text{inp}} \end{cases} & \text{Class-AB operation.} \end{cases} \tag{3.12}$$

Eq. (3.12) can be interpreted as follows. For the bias point, when there is no I_{outp}-current demand at the output, the static power consumption is expected to be minimized. Thus, the output branch should be placed in the same low-current Class-A region as the input branch. This can be accomplished by driving the controlled voltage source V_{cp} closer to the voltage drop V_{xp}, setting the bias point of the VMA output-branch component I_{onp} to $I_{\text{tail}}/2$ automatically by the $1:1$ geometrical ratio. On the contrary, when I_{outp} is required, this equality must be broken, so that, depending on the polarity of I_{outp}, the Class-AB operation can attenuate or boost I_{onp} with respect to the input-branch counterpart I_{inp}.

Supposing all transistors of Fig. 3.1 to be biased in strong inversion, (3.7) can be used to find the input-branch currents I_{inp} and I_{inn}:

$$\begin{cases} I_{\text{inp}} = \text{A}\frac{\beta}{2n}\left(V_{\text{gp}} - V_{\text{T0}} - nV_{\text{cp}}\right)^2, \\ I_{\text{inn}} = \text{A}\frac{\beta}{2n}\left(V_{\text{gn}} - V_{\text{T0}} - nV_{\text{cn}}\right)^2; \end{cases} \tag{3.13}$$

and, the output-branch currents I_{onp} and I_{onn}:

$$\begin{cases} I_{\text{onp}} = \frac{\text{A}\cdot\text{B}}{\text{A}+\text{B}}\frac{\beta}{2n}\left(V_{\text{gp}} - V_{\text{T0}}\right)^2, \\ I_{\text{onn}} = \frac{\text{A}\cdot\text{B}}{\text{A}+\text{B}}\frac{\beta}{2n}\left(V_{\text{gn}} - V_{\text{T0}}\right)^2. \end{cases} \tag{3.14}$$

Solving (3.13) and (3.14), the output currents I_{onp} and I_{onn} are found as the desired functions of the controlled voltage sources V_{cp} and V_{cn} and the

input currents $I_{\rm inp}$ and $I_{\rm inn}$:

$$\begin{cases} I_{\rm onp} = \frac{\rm B}{\rm A+B}\left(\sqrt{\frac{{\rm A}n\beta}{2}}V_{\rm cp} + \sqrt{I_{\rm inp}}\right)^2, \\ \\ I_{\rm onn} = \frac{\rm B}{\rm A+B}\left(\sqrt{\frac{{\rm A}n\beta}{2}}V_{\rm cn} + \sqrt{I_{\rm inn}}\right)^2. \end{cases} \tag{3.15}$$

Eq. (3.15) demonstrates that $V_{\rm cp}$ and $V_{\rm cn}$ can be effectively used to perform the requested Class-AB current boosting and attenuation, as well as the setting of the output bias points. Although a dependence of (3.15) on the process parameters n and β is observed, it can be canceled by proper $V_{\rm cp}$ and $V_{\rm cn}$ implementations, two types of which will be studied in the next sections.

On the other hand, if all transistors of Fig. 3.1 are supposed to be biased in weak inversion, (3.9) can be employed to find $I_{\rm inp}$ and $I_{\rm inn}$:

$$\begin{cases} I_{\rm inp} = {\rm A}I_{\rm spec}{\rm e}^{\frac{V_{\rm gp}-V_{\rm T0}}{nU_{\rm T}}}{\rm e}^{-\frac{V_{\rm cp}}{U_{\rm T}}}, \\ \\ I_{\rm inn} = {\rm A}I_{\rm spec}{\rm e}^{\frac{V_{\rm gn}-V_{\rm T0}}{nU_{\rm T}}}{\rm e}^{-\frac{V_{\rm cn}}{U_{\rm T}}}; \end{cases} \tag{3.16}$$

and, $I_{\rm onp}$ and $I_{\rm onn}$:

$$\begin{cases} I_{\rm onp} = \frac{\rm A\cdot B}{\rm A+B}I_{\rm spec}{\rm e}^{\frac{V_{\rm gp}-V_{\rm T0}}{nU_{\rm T}}}, \\ \\ I_{\rm onn} = \frac{\rm A\cdot B}{\rm A+B}I_{\rm spec}{\rm e}^{\frac{V_{\rm gn}-V_{\rm T0}}{nU_{\rm T}}}. \end{cases} \tag{3.17}$$

Solving (3.16) and (3.17), the output currents $I_{\rm onp}$ and $I_{\rm onn}$ are also found as the functions of $V_{\rm cp}$, $V_{\rm cn}$, $I_{\rm inp}$ and $I_{\rm inn}$:

$$\begin{cases} I_{\rm onp} = \frac{\rm B}{\rm A+B}{\rm e}^{\frac{V_{\rm cp}}{U_{\rm T}}}I_{\rm inp}, \\ \\ I_{\rm onn} = \frac{\rm B}{\rm A+B}{\rm e}^{\frac{V_{\rm cn}}{U_{\rm T}}}I_{\rm inn}. \end{cases} \tag{3.18}$$

Eq. (3.18) shows that V_{cp} and V_{cn} can be still used to perform the requested Class-AB current boosting and attenuation, as well as the setting of the output bias points. Despite the exhibited dependence of (3.18) on the operation temperature ($U_{\mathrm{T}} = \frac{k_{\mathrm{B}}T}{q}$), it will be proved in the next sections that specific V_{cp}- and V_{cn}-source implementations can compensate it.

3.2.2 Type-I Current Amplifier

Fig. 3.2 presents the first proposal of a Class-AB circuit for the VMA architecture of Fig. 3.1. The cross-coupled matched pair of B-sized transistors is introduced here to supply the local positive feedback, which is responsible for emphasizing Class-AB behavior. However, in order to prevent the excess of the positive-feedback gain, which may latch the OpAmp circuit, the additional crossed C-sized transistor is incorporated, providing some amount of local negative feedback. In practice, the optimum balance between the positive and negative feedback can be simply achieved by the design of the device matching ratios B and C. Finally, the required gate-bias voltage V_{bias} of the C-sized transistor is directly obtained from the matched composite diode-connected load biased with a current equal to I_{tail}.

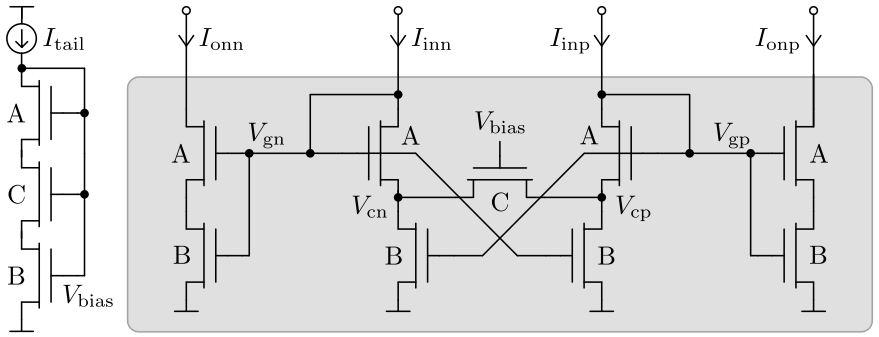

Figure 3.2 Type-I Class-AB current amplifier for the VMA architecture of Fig. 3.1.

The A- and B-sized transistors connected in series in the output branches can be simplified and viewed as a single transistor in saturation with the

equivalent multiplicity D defined by

$$\mathrm{D} \doteq \frac{\mathrm{A} \cdot \mathrm{B}}{\mathrm{A} + \mathrm{B}}. \tag{3.19}$$

Similarly, for the diode-connected load:

$$\mathrm{E} \doteq \frac{\mathrm{A} \cdot \mathrm{B} \cdot \mathrm{C}}{\mathrm{A} + \mathrm{B} + \mathrm{C}}. \tag{3.20}$$

Thus, supposing all transistors in Fig. 3.2 to be biased in strong inversion, (3.14) is rewritten here as

$$\begin{cases} I_{\mathrm{onp}} = \mathrm{D}\frac{\beta}{2n}\left(V_{\mathrm{gp}} - V_{\mathrm{T0}}\right)^2, \\ \\ I_{\mathrm{onn}} = \mathrm{D}\frac{\beta}{2n}\left(V_{\mathrm{gn}} - V_{\mathrm{T0}}\right)^2, \end{cases} \tag{3.21}$$

and using (3.7), I_{tail} is expressed by

$$I_{\mathrm{tail}} = \mathrm{E}\frac{\beta}{2n}\left(V_{\mathrm{bias}} - V_{\mathrm{T0}}\right)^2. \tag{3.22}$$

For the input branches, I_{inp} and I_{inn} are defined by (3.13) and also as the sums of the currents flowing through the B- and C-sized transistors in linear mode, which can be found using (3.6):

$$\begin{cases} I_{\mathrm{inp}} = \mathrm{B}\beta\left[V_{\mathrm{gn}} - V_{\mathrm{T0}} - \frac{n}{2}V_{\mathrm{cp}}\right]V_{\mathrm{cp}} \\ \qquad\qquad + \mathrm{C}\beta\left[V_{\mathrm{bias}} - V_{\mathrm{T0}} - \frac{n}{2}\left(V_{\mathrm{cp}} + V_{\mathrm{cn}}\right)\right]\left(V_{\mathrm{cp}} - V_{\mathrm{cn}}\right), \\ \\ I_{\mathrm{inp}} = \mathrm{B}\beta\left[V_{\mathrm{gp}} - V_{\mathrm{T0}} - \frac{n}{2}V_{\mathrm{cn}}\right]V_{\mathrm{cn}} \\ \qquad\qquad + \mathrm{C}\beta\left[V_{\mathrm{bias}} - V_{\mathrm{T0}} - \frac{n}{2}\left(V_{\mathrm{cp}} + V_{\mathrm{cn}}\right)\right]\left(V_{\mathrm{cn}} - V_{\mathrm{cp}}\right). \end{cases} \tag{3.23}$$

Solving the set of equations formed by (3.13), (3.21), (3.22) and (3.23), the characteristic equation inluding the input and output currents can be derived:

$$\begin{cases} I_{\text{inp}} = \text{B}\left(2\sqrt{\frac{I_{\text{onn}}}{\text{D}}} - \sqrt{\frac{I_{\text{onp}}}{\text{D}}} + \sqrt{\frac{I_{\text{inp}}}{\text{A}}}\right)\left(\sqrt{\frac{I_{\text{onp}}}{\text{D}}} - \sqrt{\frac{I_{\text{inp}}}{\text{A}}}\right) \\ \qquad + \text{C}\left(2\sqrt{\frac{I_{\text{tail}}}{\text{E}}} - \sqrt{\frac{I_{\text{onp}}}{\text{D}}} - \sqrt{\frac{I_{\text{onn}}}{\text{D}}} + \sqrt{\frac{I_{\text{inp}}}{\text{A}}} + \sqrt{\frac{I_{\text{inn}}}{\text{A}}}\right) \\ \qquad \left(\sqrt{\frac{I_{\text{onp}}}{\text{D}}} - \sqrt{\frac{I_{\text{onn}}}{\text{D}}} - \sqrt{\frac{I_{\text{inp}}}{\text{A}}} + \sqrt{\frac{I_{\text{inn}}}{\text{A}}}\right), \\ I_{\text{inn}} = \text{B}\left(2\sqrt{\frac{I_{\text{onp}}}{\text{D}}} - \sqrt{\frac{I_{\text{onn}}}{\text{D}}} + \sqrt{\frac{I_{\text{inn}}}{\text{A}}}\right)\left(\sqrt{\frac{I_{\text{onn}}}{\text{D}}} - \sqrt{\frac{I_{\text{inn}}}{\text{A}}}\right) \\ \qquad + \text{C}\left(2\sqrt{\frac{I_{\text{tail}}}{\text{E}}} - \sqrt{\frac{I_{\text{onn}}}{\text{D}}} - \sqrt{\frac{I_{\text{onp}}}{\text{D}}} + \sqrt{\frac{I_{\text{inn}}}{\text{A}}} + \sqrt{\frac{I_{\text{inp}}}{\text{A}}}\right) \\ \qquad \left(\sqrt{\frac{I_{\text{onn}}}{\text{D}}} - \sqrt{\frac{I_{\text{onp}}}{\text{D}}} - \sqrt{\frac{I_{\text{inn}}}{\text{A}}} + \sqrt{\frac{I_{\text{inp}}}{\text{A}}}\right). \end{cases} \tag{3.24}$$

Although (3.24) is a non-explicit equation, it demonstrates that the transfer function between the output currents I_{onp} and I_{onn} and the input currents I_{inp} and I_{inn} is independent from the technology parameters n and β, which have previously appeared in (3.15), since now only the currents and the geometrical factors are left.

If the transistors in Fig. 3.2 are biased in weak inversion, (3.17) is rewritten here using (3.19) as

$$\begin{cases} I_{\text{onp}} = \text{D}I_{\text{spec}}\text{e}^{\frac{V_{\text{gp}}-V_{\text{T0}}}{nU_{\text{T}}}}, \\ I_{\text{onn}} = \text{D}I_{\text{spec}}\text{e}^{\frac{V_{\text{gn}}-V_{\text{T0}}}{nU_{\text{T}}}}, \end{cases} \tag{3.25}$$

and, employing (3.9) and (3.20), I_{tail} is expressed by

$$I_{\mathrm{tail}} = \mathrm{E} I_{\mathrm{spec}} \mathrm{e}^{\frac{V_{\mathrm{bias}} - V_{\mathrm{T0}}}{n U_{\mathrm{T}}}}. \tag{3.26}$$

For the input branches, I_{inp} and I_{inn} are defined by (3.16) and also as the sums of the currents flowing through the B- and C-sized transistors in linear mode using (3.8):

$$\begin{cases} I_{\mathrm{inp}} = \mathrm{B} I_{\mathrm{spec}} \mathrm{e}^{\frac{V_{\mathrm{gn}} - V_{\mathrm{T0}}}{n U_{\mathrm{T}}}} \left(1 - \mathrm{e}^{-\frac{V_{\mathrm{cp}}}{U_{\mathrm{T}}}}\right) \\ \qquad\quad + \mathrm{C} I_{\mathrm{spec}} \mathrm{e}^{\frac{V_{\mathrm{bias}} - V_{\mathrm{T0}}}{n U_{\mathrm{T}}}} \left(\mathrm{e}^{-\frac{V_{\mathrm{cp}}}{U_{\mathrm{T}}}} - \mathrm{e}^{-\frac{V_{\mathrm{cn}}}{U_{\mathrm{T}}}}\right), \\ I_{\mathrm{inn}} = \mathrm{B} I_{\mathrm{spec}} \mathrm{e}^{\frac{V_{\mathrm{gp}} - V_{\mathrm{T0}}}{n U_{\mathrm{T}}}} \left(1 - \mathrm{e}^{-\frac{V_{\mathrm{cn}}}{U_{\mathrm{T}}}}\right) \\ \qquad\quad + \mathrm{C} I_{\mathrm{spec}} \mathrm{e}^{\frac{V_{\mathrm{bias}} - V_{\mathrm{T0}}}{n U_{\mathrm{T}}}} \left(\mathrm{e}^{-\frac{V_{\mathrm{cn}}}{U_{\mathrm{T}}}} - \mathrm{e}^{-\frac{V_{\mathrm{cp}}}{U_{\mathrm{T}}}}\right). \end{cases} \tag{3.27}$$

Solving the set of equations formed by (3.16), (3.25), (3.26) and (3.27), the characteristic equation including the input and output currents can be derived:

$$\begin{cases} I_{\mathrm{inp}} = \dfrac{\mathrm{B}}{\mathrm{D}} I_{\mathrm{onn}} \left(1 - \dfrac{\mathrm{D}}{\mathrm{A}} \dfrac{I_{\mathrm{inp}}}{I_{\mathrm{onp}}}\right) + \dfrac{\mathrm{C} \cdot \mathrm{D}}{\mathrm{A} \cdot \mathrm{E}} I_{\mathrm{tail}} \left(\dfrac{I_{\mathrm{inp}}}{I_{\mathrm{onp}}} - \dfrac{I_{\mathrm{inn}}}{I_{\mathrm{onn}}}\right), \\ I_{\mathrm{inn}} = \dfrac{\mathrm{B}}{\mathrm{D}} I_{\mathrm{onp}} \left(1 - \dfrac{\mathrm{D}}{\mathrm{A}} \dfrac{I_{\mathrm{inn}}}{I_{\mathrm{onn}}}\right) + \dfrac{\mathrm{C} \cdot \mathrm{D}}{\mathrm{A} \cdot \mathrm{E}} I_{\mathrm{tail}} \left(\dfrac{I_{\mathrm{inn}}}{I_{\mathrm{onn}}} - \dfrac{I_{\mathrm{inp}}}{I_{\mathrm{onp}}}\right). \end{cases} \tag{3.28}$$

Eq. (3.28) is also non-explicit. However, it reveals that the transfer function between the output currents I_{onp} and I_{onn} and the input currents I_{inp} and I_{inn} is no longer dependent on the thermal voltage U_{T}, and thus on the temperature, as it has been the case in (3.18).

The maximum Class-AB output current I_{max} of the type-I VMA can be found for all inversion levels by analyzing one of two completely unbalanced

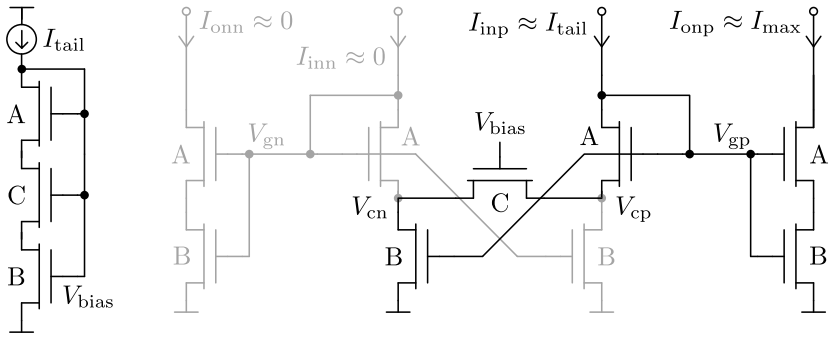

Figure 3.3 Circuit used for I_{max} evaluation of the Type-I Class-AB current amplifier of Fig. 3.2. The dimmed circuit parts are treated as inexistent.

input conditions. The circuit illustrated in Fig. 3.3 is derived from Fig. 3.2 for the case of the positive-path $I_{inp} \approx I_{tail}$ and its analysis yields:

$$I_{max} \simeq \left(1 + \frac{D}{C}\right) I_{tail}. \tag{3.29}$$

An excessive positive local feedback in the circuit of Fig. 3.2 may result in the VMA instability, or even a self-latch if enough differential input amplitude is applied. In order to prevent this unwanted behavior, the built-in smoother of Fig. 3.4 is proposed. This mechanism injects the low-level common-mode currents I_{min} into the input branches. Due to this minimum bias level ($I_{inp,n} \geq I_{min}$), the cut-off state is avoided in both sides of the differential structure and the VMA transient operation is smoothed.

At this point, the desired Class-AB functionality is achieved using the proposed type-I circuit. The possibility of an alternative V_{bias} tuning opens this topology for the exploration of further enhancements. However, it needs additional bias circuits for the V_{bias} and, optionally, I_{min} generation. These blocks increase the quiescent currents and lower the VMA power efficiency. The power consumption of the V_{bias}-generation circuit can be reduced by scaling down its polarization current and, proportionally, the width of the A-, B- and C-sized devices conneted in series, as the strict matching is not necessary.

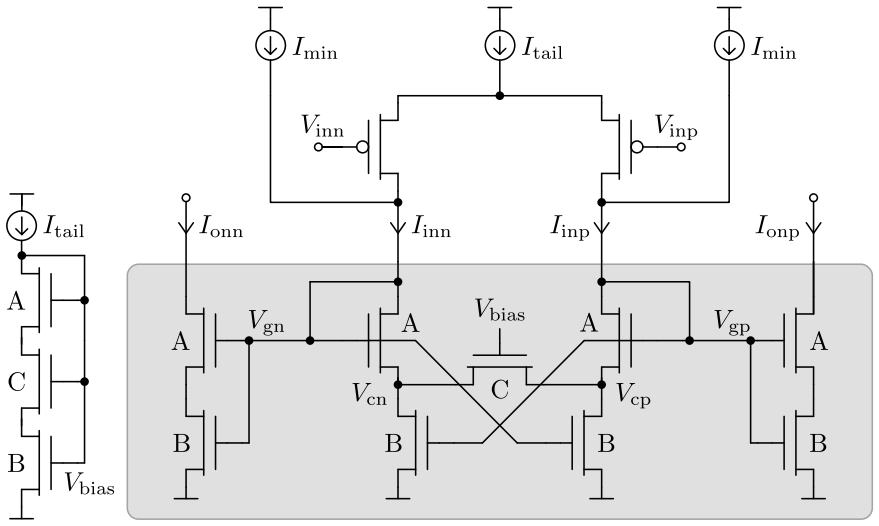

Figure 3.4 Type-I current amplifier with an additional Class-AB smother.

Further research into type-I circuit improvement has been performed, trying to overcome the necessity for additional biasing blocks and yielding the type-II circuit presented in the next section.

3.2.3 Type-II Current Amplifier

Fig. 3.5 introduces the second proposal of a Class-AB current amplifier for the boxed parts of Fig. 3.1. Here, the C-sized negative-feedback transistor of Fig. 3.2 is replaced by two split counterparts in Fig. 3.5, which are autobiased and also prevent the VMA self-latch. Thus, no extra reference circuits are needed and the power efficiency is slightly improved at the cost of a non-electrically-tunable circuit.

In order to comply with the required behavior expressed by (3.12) for the bias point, the B-sized output transistors of Fig. 3.1 is replaced by the (B+C)-sized counterparts in Fig. 3.5. Thus, under no differential input current, the equalities $V_{xp} = V_{xn} = V_{cp} = V_{cn}$ and $I_{onp} = I_{onn} = I_{inp} = I_{inn}$

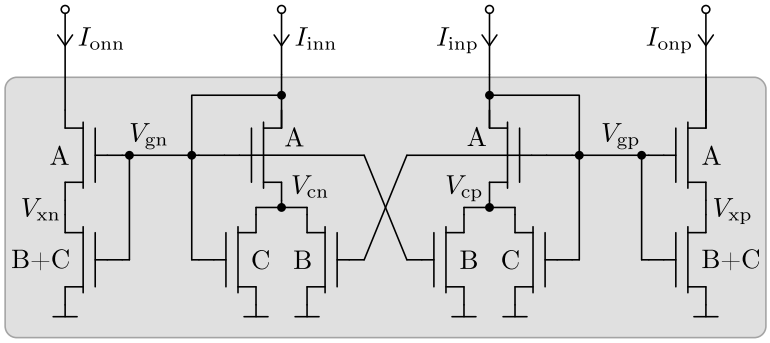

Figure 3.5 | Type-II Class-AB current amplifier for the VMA architecture of Fig. 3.1.

are achieved. The A- and (B+C)-sized transistors connected in series in the output branches can be simplified and viewed as a single transistor in saturation with the equivalent multiplicity F defined by

$$\mathrm{F} \doteq \frac{\mathrm{A}\,(\mathrm{B}+\mathrm{C})}{\mathrm{A}+\mathrm{B}+\mathrm{C}}. \tag{3.30}$$

Thus, taking into account the output-transistor substitution B→B+C and supposing all transistors to be biased in strong inversion in Fig. 3.5, (3.14) is rewritten here as

$$\begin{cases} I_{\mathrm{onp}} = \mathrm{F}\,\frac{\beta}{2n}\,(V_{\mathrm{gp}} - V_{\mathrm{T0}})^2\,, \\ I_{\mathrm{onn}} = \mathrm{F}\,\frac{\beta}{2n}\,(V_{\mathrm{gn}} - V_{\mathrm{T0}})^2\,. \end{cases} \tag{3.31}$$

For the input branches, I_{inp} and I_{inn} are defined by (3.13) and also as the sums of the currents flowing through the B- and C-sized transistors operat-

ing in linear mode, which can be found using (3.6):

$$\begin{cases} I_{\text{inp}} = \text{B}\beta\left(V_{\text{gn}} - V_{\text{T0}} - \dfrac{n}{2}V_{\text{cp}}\right)V_{\text{cp}} + \text{C}\beta\left(V_{\text{gp}} - V_{\text{T0}} - \dfrac{n}{2}V_{\text{cp}}\right)V_{\text{cp}}, \\ I_{\text{inn}} = \text{B}\beta\left(V_{\text{gp}} - V_{\text{T0}} - \dfrac{n}{2}V_{\text{cn}}\right)V_{\text{cn}} + \text{C}\beta\left(V_{\text{gn}} - V_{\text{T0}} - \dfrac{n}{2}V_{\text{cn}}\right)V_{\text{cn}}. \end{cases} \tag{3.32}$$

Solving the set of equations formed by (3.13), (3.31) and (3.32), the characteristic equation including the input and output currents can be derived:

$$\begin{cases} I_{\text{inp}} = \left[2\left(\text{B}\sqrt{\dfrac{I_{\text{onn}}}{\text{F}}} + \text{C}\sqrt{\dfrac{I_{\text{onp}}}{\text{F}}}\right) - (\text{B}+\text{C})\left(\sqrt{\dfrac{I_{\text{onp}}}{\text{F}}} - \sqrt{\dfrac{I_{\text{inp}}}{\text{A}}}\right)\right] \\ \qquad \left(\sqrt{\dfrac{I_{\text{onp}}}{\text{F}}} - \sqrt{\dfrac{I_{\text{inp}}}{\text{A}}}\right), \\ I_{\text{inn}} = \left[2\left(\text{B}\sqrt{\dfrac{I_{\text{onp}}}{\text{F}}} + \text{C}\sqrt{\dfrac{I_{\text{onn}}}{\text{F}}}\right) - (\text{B}+\text{C})\left(\sqrt{\dfrac{I_{\text{onn}}}{\text{F}}} - \sqrt{\dfrac{I_{\text{inn}}}{\text{A}}}\right)\right] \\ \qquad \left(\sqrt{\dfrac{I_{\text{onn}}}{\text{F}}} - \sqrt{\dfrac{I_{\text{inn}}}{\text{A}}}\right). \end{cases} \tag{3.33}$$

Eq. (3.33) is a non-explicit equation. Nevertheless, it demonstrates that the independence from both the technology parameters n and β and from the operative temperature of the current transfer function is preserved.

The analytical expressions of (3.33) can be solved numerically. To verify the results, the I_{inp}-I_{inn} DC sweep of the circuit in Fig. 3.5 is simulated, employing long-channel transistors biased in strong inversion with IC_F=16. Fig. 3.6 plots the analytical and simulated Class-AB normalized current transfer curves for different B/C ratios. It demonstrates the flexibility of the proposed current mirror when designing a VMA with a particular Class-AB

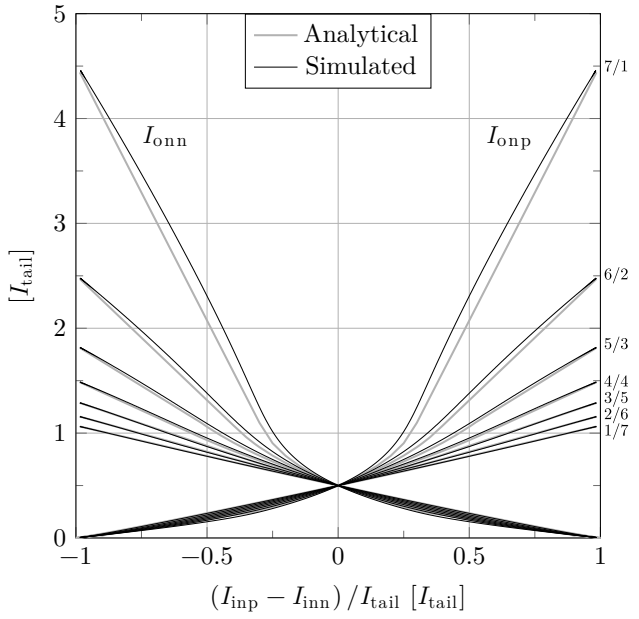

Figure 3.6 Analytical and simulated type-II Class-AB normalized current transfer curves for different B/C ratios (on the right), using A=B+C=8 and all transistors biased in strong inversion.

modulation index. In practice, a wide range of OpAmp responses can be chosen, from strong Class AB to almost Class A, by changing the relative weights between the A, B and C variables.

If the transistors in Fig. 3.5 are biased in weak inversion, and taking into account the output-transistor substitution B→B+C, (3.17) is rewritten here using (3.30) as

$$\begin{cases} I_{\mathrm{onp}} = \mathrm{F} I_{\mathrm{spec}} \mathrm{e}^{\frac{V_{\mathrm{gp}} - V_{\mathrm{T0}}}{nU_{\mathrm{T}}}}, \\ I_{\mathrm{onn}} = \mathrm{F} I_{\mathrm{spec}} \mathrm{e}^{\frac{V_{\mathrm{gn}} - V_{\mathrm{T0}}}{nU_{\mathrm{T}}}}. \end{cases} \tag{3.34}$$

For the input branches, I_{inp} and I_{inn} are defined by (3.16) and also as the

sums of the currents flowing through the B- and C-sized transistors in linear mode using (3.8):

$$\begin{cases} I_{\mathrm{inp}} = \mathrm{B} I_{\mathrm{spec}} \mathrm{e}^{\frac{V_{\mathrm{gn}}-V_{\mathrm{T0}}}{nU_{\mathrm{T}}}} \left(1-\mathrm{e}^{-\frac{V_{\mathrm{cp}}}{U_{\mathrm{T}}}}\right) + \mathrm{C} I_{\mathrm{spec}} \mathrm{e}^{\frac{V_{\mathrm{gp}}-V_{\mathrm{T0}}}{nU_{\mathrm{T}}}} \left(1-\mathrm{e}^{-\frac{V_{\mathrm{cp}}}{U_{\mathrm{T}}}}\right), \\ I_{\mathrm{inn}} = \mathrm{B} I_{\mathrm{spec}} \mathrm{e}^{\frac{V_{\mathrm{gp}}-V_{\mathrm{T0}}}{nU_{\mathrm{T}}}} \left(1-\mathrm{e}^{-\frac{V_{\mathrm{cn}}}{U_{\mathrm{T}}}}\right) + \mathrm{C} I_{\mathrm{spec}} \mathrm{e}^{\frac{V_{\mathrm{gn}}-V_{\mathrm{T0}}}{nU_{\mathrm{T}}}} \left(1-\mathrm{e}^{-\frac{V_{\mathrm{cn}}}{U_{\mathrm{T}}}}\right). \end{cases} \tag{3.35}$$

Solving the set of equations formed by (3.16), (3.34) and (3.35), the characteristic equation including the input and output currents can be derived:

$$\begin{cases} I_{\mathrm{inp}} = \left(\dfrac{\mathrm{B}}{\mathrm{F}} I_{\mathrm{onn}} + \dfrac{\mathrm{C}}{\mathrm{F}} I_{\mathrm{onp}}\right)\left(1 - \dfrac{\mathrm{F}}{\mathrm{A}} \dfrac{I_{\mathrm{inp}}}{I_{\mathrm{onp}}}\right), \\ I_{\mathrm{inn}} = \left(\dfrac{\mathrm{B}}{\mathrm{F}} I_{\mathrm{onp}} + \dfrac{\mathrm{C}}{\mathrm{F}} I_{\mathrm{onn}}\right)\left(1 - \dfrac{\mathrm{F}}{\mathrm{A}} \dfrac{I_{\mathrm{inn}}}{I_{\mathrm{onn}}}\right). \end{cases} \tag{3.36}$$

Again, (3.36) is also non-explicit. However, it reveals that the transfer function between the output currents I_{onp} and I_{onn} and the input currents I_{inp} and I_{inn} is independent from the thermodynamic voltage U_{T}, and thus from the temperature.

Like for the strong inversion, (3.36) can be solved numerically. To verify the results, the I_{inp}-I_{inn} DC sweep of the circuit in Fig. 3.5 is simulated, employing long-channel transistors biased in weak inversion with $\mathrm{IC_F}$=0.01. Fig. 3.7 plots the analytical and simulated Class-AB normalized current transfer curves for the same conditions as in Fig. 3.6. It can be seen that the circuit design flexibility is maintained.

The results presented above prove that the desired Class-AB performance for the VMA devices in the strong- and weak-inversion regions is achieved. Consequently, it can be deduced that the performance in the intermediate moderate-inversion region will be conserved, as will be demonstrated in the next chapter. Here, the maximum output current of the type-II VMA can

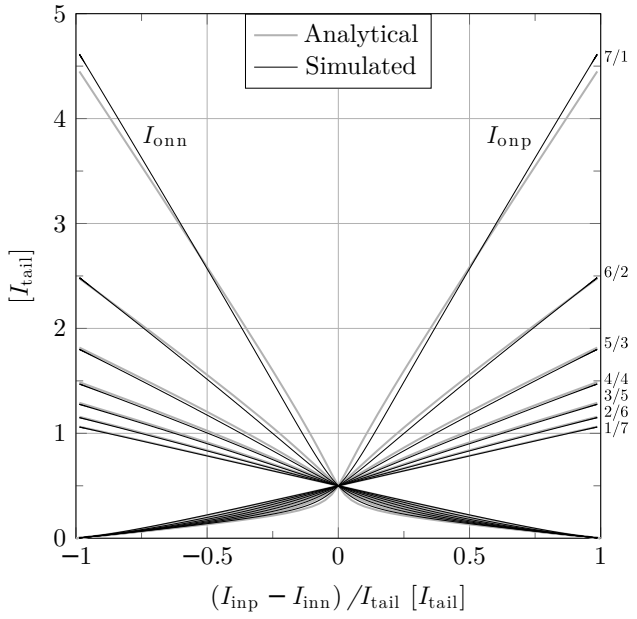

Figure 3.7 Analytical and simulated type-II Class-AB normalized current transfer curves for different B/C ratios (on the right), using A=B+C=8 and all transistors biased in weak inversion.

be approximated for all inversion-level regions in the same way as for the type-I VMA, completely unbalancing the input. The circuit illustrated in Fig. 3.8 is derived from Fig. 3.5 for the case of the positive-path $I_{inp} \approx I_{tail}$ and its analysis provides:

$$I_{max} \simeq \frac{1+\frac{A}{C}}{1+\frac{A}{B+C}} I_{tail} > I_{tail}, \tag{3.37}$$

where it can be seen that I_{max} is greater than I_{tail} and the Class-AB behavior is present for any sizing. Also, a good agreement is obtained between (3.37) and the analytical and simulated transfer curves for different B/C ratios, which have been presented in Fig. 3.6 and Fig. 3.7.

This type-II current amplifier is selected for the development of the ΔΣM-

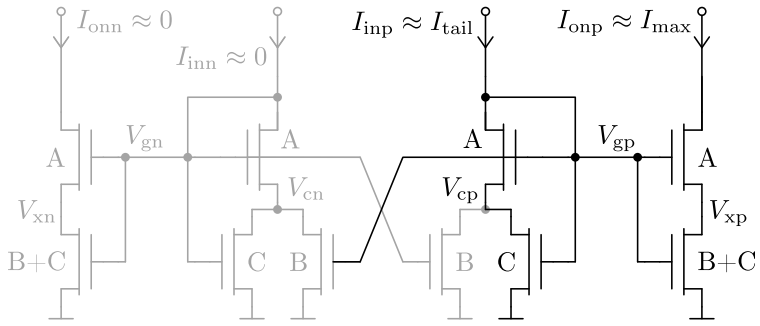

Figure 3.8 Circuit used for I_{max} evaluation of the Type-II Class-AB current amplifier of Fig. 3.5. The dimmed circuit parts are treated as inexistent.

integrator SOA, which will be presented in Section 3.3

3.2.4 Full-Scale Cascode Biasing

Probably, the main disadvantage of using a single-stage approach for the proposed VMA-family architecture is the limited open-loop gain A_{open}. As shown in Fig. 3.1, the cascode transistors are used for the purpose of increasing A_{open} and, thus, reducing the $\Delta\Sigma$M-integrator settling error, as already discussed in the previous chapter. However, these additional stacked transistors also decrease the VMA output voltage full scale. In order to minimize this loss, the transistors should be biased at the edge of saturation. Traditional bias circuits used for this purpose are relatively complex, resulting in area or power consumption increase, and are not valid for all MOSFET inversion levels, hindering the design process. As illustrated in the basic example of Fig. 3.9, the cascode-bias circuit implementation based on [83] solves these issues by using a diode-connected transistor as the bias circuit with a specific sizing rule. Here, the transistor M1 can be viewed as a saturated equivalent of the A- and B-sized transistors connected in series in the output branches for the type-I current amplifier in Fig. 3.2, or the A- and (B+C)-sized transistors in series for the type-II current amplifier in Fig. 3.5. The gate of the cascode transistor M2 is biased by the voltage V_b,

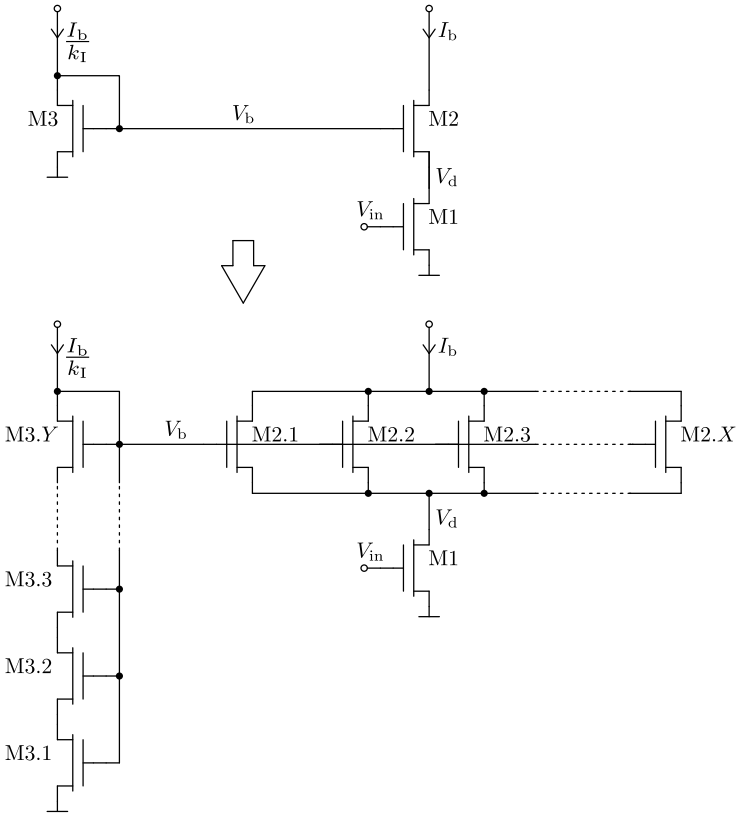

Figure 3.9 | Cascode series/parallel-association biasing circuit: folded (top) and unfolded (bottom) views.

generated by the diode-connected M3.

Using (3.11), the analysis of the circuit in Fig. 3.9 provides the characteristic equation including the inversion coefficients IC_{1-3} of M1-3 [83]:

$$\sqrt{1+4\mathrm{IC}_3}-\sqrt{1+4\mathrm{IC}_2}-\sqrt{1+4\mathrm{IC}_1}+\ln\left(\frac{\sqrt{1+4\mathrm{IC}_3}-1}{\sqrt{1+4\mathrm{IC}_2}-1}\right) = \ln\left(A_1\right)-1+\frac{V_{\mathrm{m1}}}{U_{\mathrm{T}}}, \tag{3.38}$$

where $A_1 = \frac{\partial V_\mathrm{d}}{\partial V_\mathrm{in}}$ is the M1 intrinsic gain and $V_\mathrm{m1} = V_\mathrm{d} - V_\mathrm{sat1}$ is the M1-saturation-voltage safety margin. Choosing $A_1 = 100$ and $V_\mathrm{m1} = 2U_\mathrm{T}$, (3.42) is simplified as

$$\sqrt{1+4\mathrm{IC}_3} - \sqrt{1+4\mathrm{IC}_2} - \sqrt{1+4\mathrm{IC}_1} + \ln\left(\frac{\sqrt{1+4\mathrm{IC}_3}-1}{\sqrt{1+4\mathrm{IC}_2}-1}\right) = 5.6. \quad (3.39)$$

Solving (3.39) numerically, IC_3 can be found. Assuming an independence from the M2-3 V_T0, which is guaranteed by the series/parallel association [83] in Fig. 3.9, the M3 aspect ratio $\left(\frac{W}{L}\right)_3$ can be expressed as

$$\left(\frac{W}{L}\right)_3 = \frac{\left(\frac{W}{L}\right)_2}{k_\mathrm{I}} \frac{\mathrm{IC}_2}{\mathrm{IC}_3}, \quad (3.40)$$

where $\left(\frac{W}{L}\right)_2$ is the M2 aspect ratio and k_I is the M3 bias-current reduction factor with respect to I_b of M2. The M3 total effective width W_3 is set to the width of the unitary element of M2, thus the total effective length of M3 can be found as

$$L_3 = \frac{W_3}{\left(\frac{W}{L}\right)_3}. \quad (3.41)$$

Finally, the number of required series unitary elements Y in Fig. 3.9 is

$$Y = \frac{L_3}{L_2}, \quad (3.42)$$

and the number of required parallel unitary elements X is

$$X = k_\mathrm{I} \frac{\mathrm{IC}_3}{\mathrm{IC}_2} \frac{L_2}{L_3}. \quad (3.43)$$

In order to minimize the number of elements connected in series, it is proposed to adopt a solution for the fixed $Y = 1$. In this case, X, L_2 and IC_2

are used as input constants, and the variables k_{I} and IC_3 are adjusted so that the equalities $L_3 = L_2$ and $Y = 1$ are produced, according to (3.42) and (3.43). The implementation of this solution in the context of the full SOA will be presented in the next section.

3.3 Switched-VMA Realization

In this section, the continuous-time type-II Class-AB single-stage VMA introduced in Section 3.2.3 is transformed into a SOA [36] for SC applications. In the next chapter, this switched VMA (SVMA) will be used as an active element of the ΔΣM integrators.

Fig. 3.10 illustrates three types of a SC-integrator fully-differential stage: the first two, employing a traditional OpAmp; and, the last, employing a SOA. The complete operation cycle of the SC integrator is split in two main phases: the sampling phase ϕ_{A} and the integration phase ϕ_{B}. In what follows, all switches being reconfigured by these phases are CMOS transmission gates operating at the nominal voltage supply. Their implementation will be discussed in Chapter 4.

In all three cases of Fig. 3.10, the first-half-cycle phase ϕ_{A} configures the switches to sample the integrator input voltage into C_{si}, and the second-half-cycle phase ϕ_{B} configures the switches and uses the OpAmp or the SOA to transfer the C_{si} charge into $C_{\mathrm{i}i}$, thus integrating the input signal and scaling it according to the $C_{si}/C_{\mathrm{i}i}$ ratio, ideally. The traditional switching scheme of Fig. 3.10 (a) assumes that the preceding and following integrator stages perform their sampling and integration operations in the same phases as the stage under discussion. Therefore, while in the sampling phase ϕ_{A}, the OpAmp is used to precharge the sampling capacitor of the next stage $C_{\mathrm{s}(i+1)}$ to the voltage resulting from the previous-cycle integration operation in ϕ_{B}. Consequently, the OpAmp is always enabled and there are no time slots to switch it off for the purpose of power-consumption reduction.

The switching scheme of Fig. 3.10 (b) paves the way for the reduction of the OpAmp duty-cycle by applying the stage half-cycle interleaving. This means that, while the stage under discussion is in the sampling phase, the preceding and following stages are in the integration phase and vice versa.

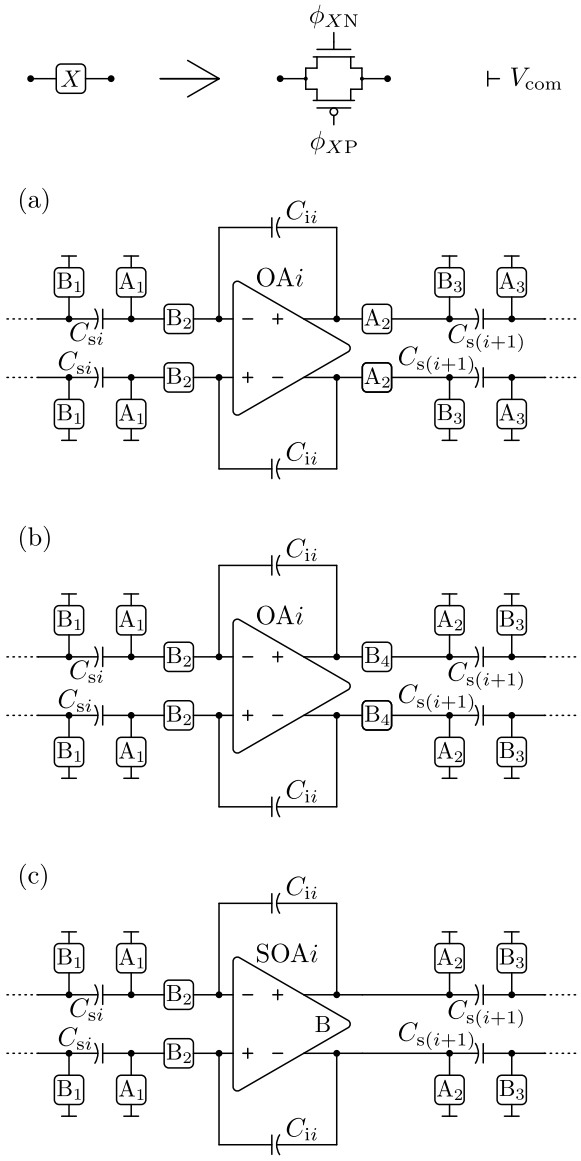

Figure 3.10 SC-integrator stage: (a) with a traditional OpAmp; (b) with an OpAmp in interleaving; (c) with a SOA.

Thus, the OpAmp is not used in ϕ_A and can be switched off. Only in ϕ_B, it is employed for both the C_{si}-charge transfer into C_{ii} and the simultaneous update of $C_{s(i+1)}$. If the OpAmp is not turned off during ϕ_A, the switches B_4 are needed to isolate the OpAmp outputs from the $C_{s(i+1)}$-charge transfer in the next stage. These switches are the source of distortion due to the fact that the transmission-gate on resistance under the supported input-output voltage fluctuations is not constant. Their use can be avoided by employing the SOA, as shown in Fig. 3.10 (c).

The SOA-integrator operation is illustrated in Fig. 3.11 for both phases. In the sampling phase ϕ_A shown in Fig. 3.11 (a), the SOA is turned off, only sensing the common-reference voltage V_{com} for the CMFB circuit, whose implementation and operation will be discussed below. For this purpose, just few bias circuits of the SOA remain active in ϕ_A, approaching the overall static-power savings to 50 %.

When in ϕ_B, the SOA is turned on to perform the integration operation, as shown in Fig. 3.11 (b). At the same time, the SOA senses the output common-mode voltage and corrects it with respect to V_{com} stored in the preceding ϕ_A. Parasitic charge injections produced by the switch- and SOA-device disconnection at the end of ϕ_B may cause distortion of the processing signal and the consequent loss of the ΔΣM resolution. In order to minimize them, two additional delayed counterparts ϕ_{AD} and ϕ_{BD} of ϕ_A and ϕ_B, respectively, are employed, shown in Fig. 3.12 (a) [84]. Thus, the switches B_2 and B_3 in Fig. 3.10 (c) and simplified as B in Fig. 3.12 (b) are opened first on the falling edge of ϕ_B. Since, at the end of ϕ_B, their input-output terminals are close to V_{com} for the positive and negative paths, when disconnected, they inject constant and equal charge, whose effects are decoupled by the differential operation and the SOA CMFB in the next cycle. After a short delay, the switches B_1 in Fig. 3.10 (c) and simplified as B_D in Fig. 3.12 (b) and the SOA are then turned off on the falling edge of ϕ_{BD}. The charge injections which may be caused by the SOA disconnection are not equal for the positive and negative paths because they depend on the output signal and their effects cannot be decoupled by the differential operation. Therefore, the phase sequence in Fig. 3.12 ensures that there is no path for the parasitic charge to follow from the SOA output through any capacitor at the moment when the SOA is turned off. Thus, all parasitic charge of

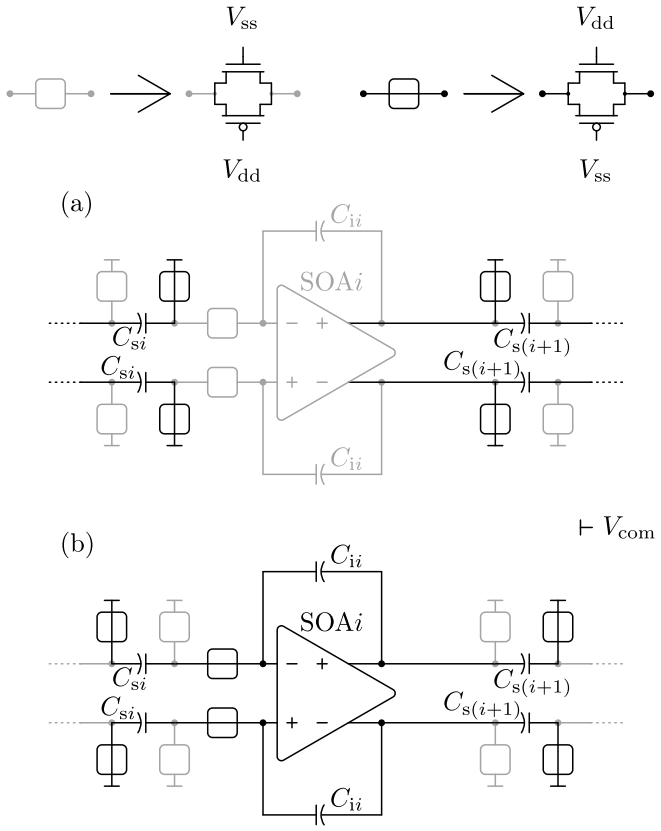

Figure 3.11 SOA-integrator stage in two phases: (a) sampling phase ϕ_A; (b) integration phase ϕ_B.

the SOA output branches is absorbed by the supply rails and no distortion in the SC circuit is produced. The phase ϕ_{AD} is used for the same purpose as ϕ_{BD}, but for the preceding and following stages.

The complete SVMA schematic using the type-II Class-AB current amplifier is shown Fig. 3.13. In case of the SOA-integrator stage operation discussed in Fig. 3.12, the SVMA off state ϕ_{off} and on state ϕ_{on} correspond to the integrator phases ϕ_{AD} and ϕ_{BD}, respectively. The transmission gates are not needed for the switch implementation because their normal-operation input-output voltages are located in narrow regions close to the voltage

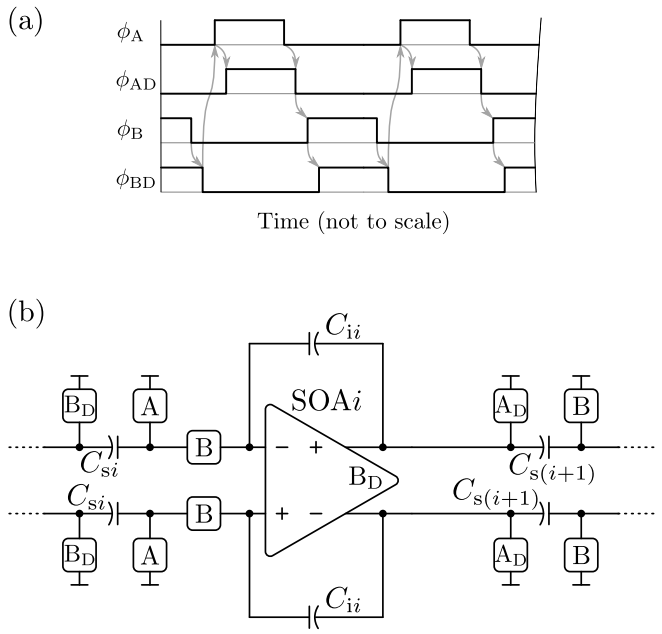

Figure 3.12 SC-integrator phase chronogram (a) for the transmission-gate NMOS devices and scheme (b) derived from Fig. 3.10 (c).

supply rails, where the performance of a single PMOS or NMOS switch is acceptable.

During the off state ϕ_{off}, illustrated in Fig. 3.14, the switches are configured in a way the tail currents of the input pairs are cut off, powering down most of the SVMA. Only the CMFB circuit and few bias references remain in operation to guarantee the following fast-switch-on operation. The diode-connection of the transistors MB1-2 generates the CMFB offset voltage V_{cmfb0}, which is sampled in the CMFB capacitors C_{cmfb} with respect to the output voltages V_{outp} and V_{outn} shorted to V_{com} during ϕ_{off}, as can be recalled from Fig. 3.11 (a).

The SVMA is turned on in ϕ_{on} by the switches connecting the gates of the tail transistors MT1-2 to the voltage references provided by the bias circuits including MB1-3, as shown in Fig. 3.15. The CMFB operation is performed

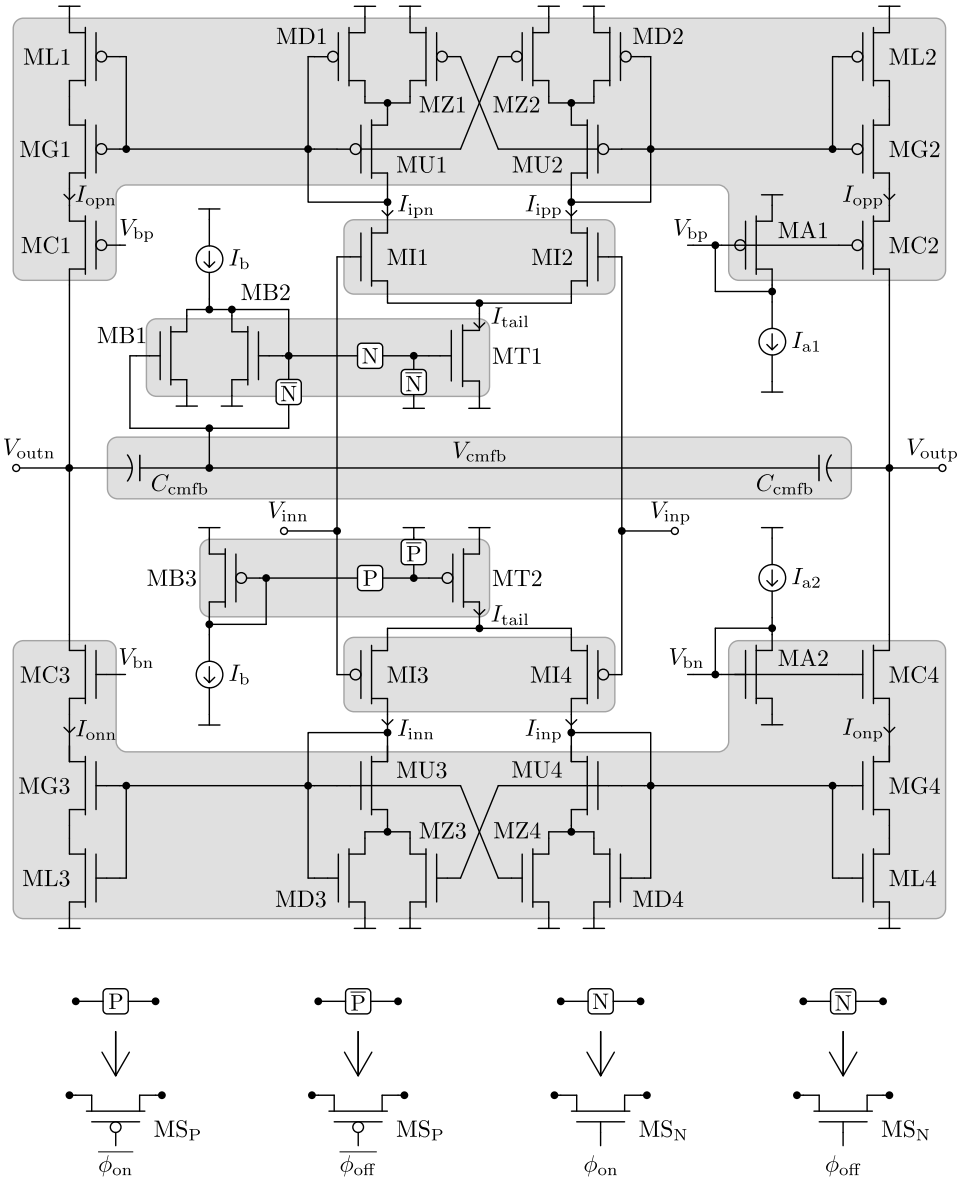

Figure 3.13 | Type-II-SVMA proposal and practical switch implementation.

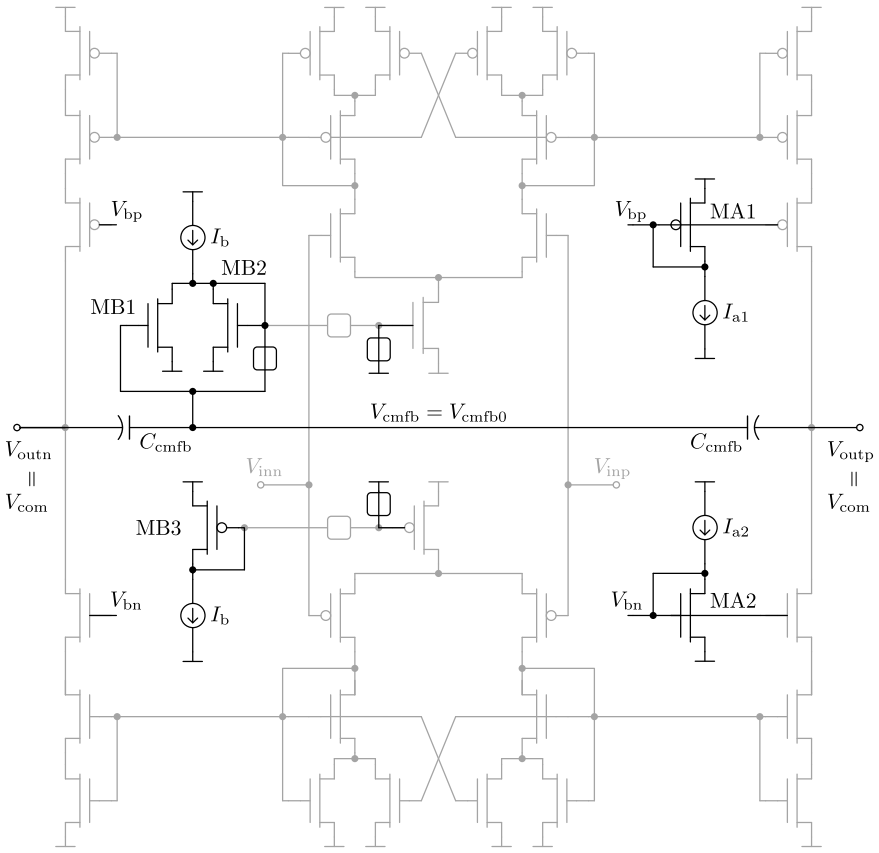

Figure 3.14 | SVMA in the off state ϕ_{off}.

by the control of the tail current of the NMOS input pair through the MT1 gate voltage, which in turn depends on

$$V_{cmfb} = V_{cmfb0} + \frac{V_{outp} + V_{outn}}{2} - V_{com}. \tag{3.44}$$

This implementation allows a zero startup time for the full SVMA. The CMFB needs only one idle SVMA half-cycle time to start operating properly.

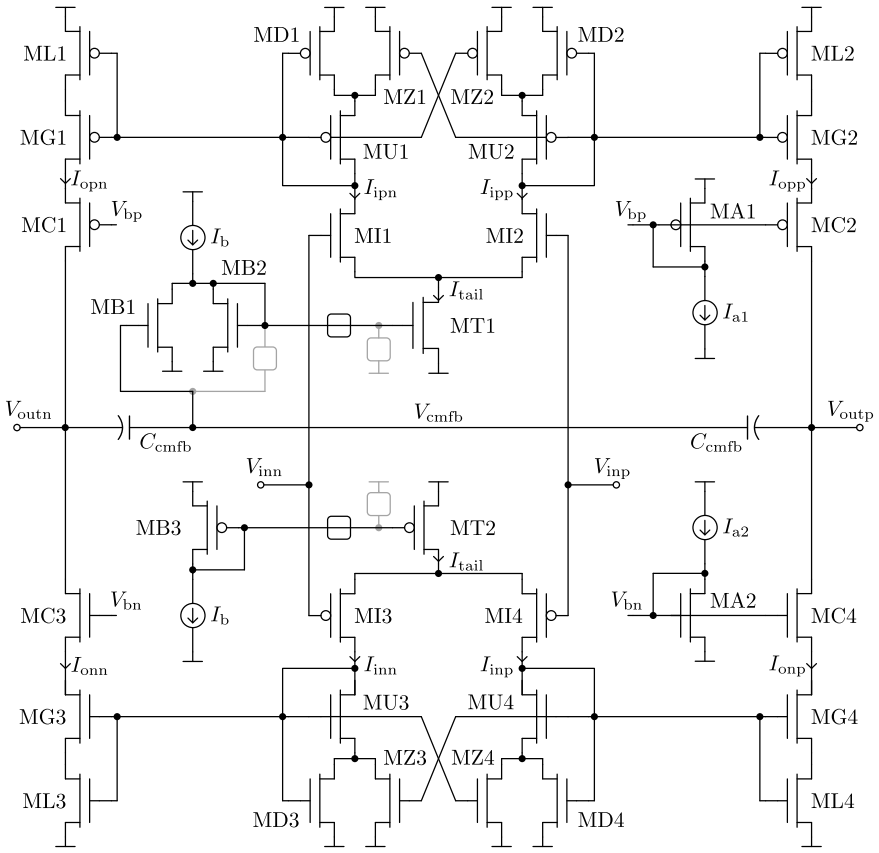

Figure 3.15 | SVMA in the on state ϕ_{on}.

The matched devices grouped in each of the boxes in Fig. 3.13 are arranged to use the same unitary element but with different multiplicities. The multiplicity ratio between the transistors MZ and the transistors MD m_Z/m_D is defined as k_z and corresponds to the ratio B/C in Fig. 3.5 controlling the Class-AB behavior:

$$k_z = \frac{B}{C} = \frac{m_Z}{m_D}. \tag{3.45}$$

In order to minimize the number of design variables, as a rule of thumb,

the multiplicity of MU m_{U}, corresponding to A in Fig. 3.5, is set to the empirically chosen sum of m_{Z} and m_{D}:

$$m_{\mathrm{U}} = \mathrm{A} = \mathrm{B} + \mathrm{C} = m_{\mathrm{Z}} + m_{\mathrm{D}}. \tag{3.46}$$

The multiplicity ratio between the transistors MG and the transistors MU $m_{\mathrm{G}}/m_{\mathrm{U}}$ is introduced here as k_{b} and can be viewed as the ratio between the output- and input-branch bias currents:

$$k_{\mathrm{b}} = \frac{m_{\mathrm{G}}}{m_{\mathrm{U}}} = \frac{m_{\mathrm{L}}}{m_{\mathrm{Z}} + m_{\mathrm{D}}}. \tag{3.47}$$

Therefore, using (3.37), (3.45), (3.46) and incorporating k_{b}, expressed by (3.47), the maximum slewing current $I_{\max}$ which can be provided to the load is found as

$$I_{\max} = \left(1 + \frac{k_{\mathrm{z}}}{2}\right) k_{\mathrm{b}} I_{\mathrm{tail}}. \tag{3.48}$$

It is decided to use the same unitary elements for the cascode transistors MC as for the rest of the load transistors and set their multiplicity m_{C} to the equivalent multiplicity of MG and ML connected in series:

$$m_{\mathrm{C}} = \frac{m_{\mathrm{G}} m_{\mathrm{L}}}{m_{\mathrm{G}} + m_{\mathrm{L}}}. \tag{3.49}$$

From (3.46) and (3.47), it follows that $m_{\mathrm{L}} = m_{\mathrm{G}}$. Thus, (3.49) can be simplified as

$$m_{\mathrm{C}} = \frac{m_{\mathrm{G}}}{2}. \tag{3.50}$$

The bias voltage of MC is provided by the circuits consisting of the transistors MA, which are build using a single unitary element in diode connection and the current sources I_{a1} and I_{a2} which are scaled so that the number of elements in series Y is equal to one, as explained in Section 3.2.4.

The relationship between the SVMA design variables proposed above and illustrated in Fig. 3.16, simplifies the optimization process, which will be discussed in the next chapter. Given the specifications, the only variables which need to be swept are k_z, k_b, I_{tail}, and the inversion coefficients of the transistor groups IC_{mirr}, IC_{tail}, and IC_{in}.

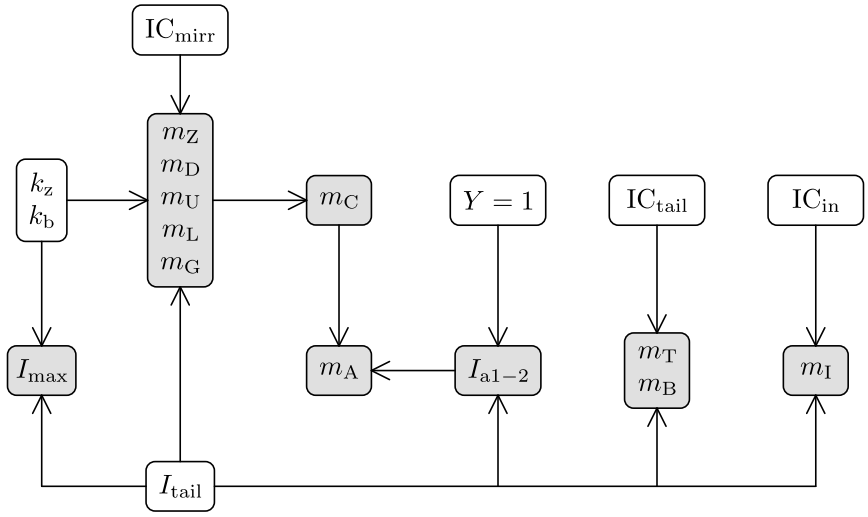

Figure 3.16 Relationship between the input variables (boxed in white) and the output parameters (boxed in gray) for the design of the type-II SVMA of Fig. 3.13.

A Calibration-Free High-Resolution Non-Bootstrapped 1.8-V Low-Power ΔΣM in a Standard 0.18-µm CMOS Technology

4

This chapter focuses on the application of the low-power CMOS SC circuits, developed in the previous chapter, to the target high-resolution ΔΣM, whose specifications have been defined in Section 2.5.

In the beginning, the selected ΔΣM-architecture high-level modeling is performed, extracting the specifications for the ΔΣM basic circuit blocks. Then, the SC implementation is proposed. The switching scheme is reviewed and the capacitors are sized. Following, the optimization techniques for the integrator SVMAs and the feedforward switches are introduced. The simulation results for the schematic and post layout of the full ΔΣM are provided. Finally, a test vehicle for experimental measurements of the optimized circuits is presented.

4.1 Design Framework

As it is explained in Chapter 1, there is a motivation to work in an open design environment. Instead of commonly used proprietary MATLAB [85], open-source System for Algebra and Geometry Experimentation (SAGE) [86] is chosen as an analytical and numerical equation solver, a high-level-model simulator and an electrical-simulator design interface. SAGE is based on the Python programming language [87], supporting procedural, functional and object-oriented constructs. Also, it is employed in the software application developed for the measurement setup, which is presented in the next chapter.

The circuit research is performed using tools from the open-source gEDA project [88] such as gschem for the schematic entry, gnetlist for the netlist extraction, and ngspice with XSPICE for the circuit simulation.

The only steps which are completed using proprietary software are the layout design and the post-layout simulations. They are performed with the Cadence Virtuoso environment [89], employing the Spectre simulator, the Verilog-A hardware description language and the Skill and Ocean scripting languages.

As a result, a multi-programming-language environment is developed with the custom SAGE scripts on the top execution level, as illustrated in Fig. 4.1.

4.2 High-Level Modeling

Following the discussion on the optimum architecture for the target resolution and bandwidth from the Chapter 2, a forth-order single-loop architecture based on [90] is chosen for the ΔΣM, shown in Fig. 4.2. A unique feedback loop with multiple feedforward paths are incorporated here to relax signal-headroom specifications at the output of each integrator [72]. The use of single-bit quantization not only avoids typical distortion issues of multi-bit alternatives caused by device mismatch, but it also allows to use a passive adder for the feedforward signal summation, with the resulting advantages in terms of power consumption and clock timing [17]. This archi-

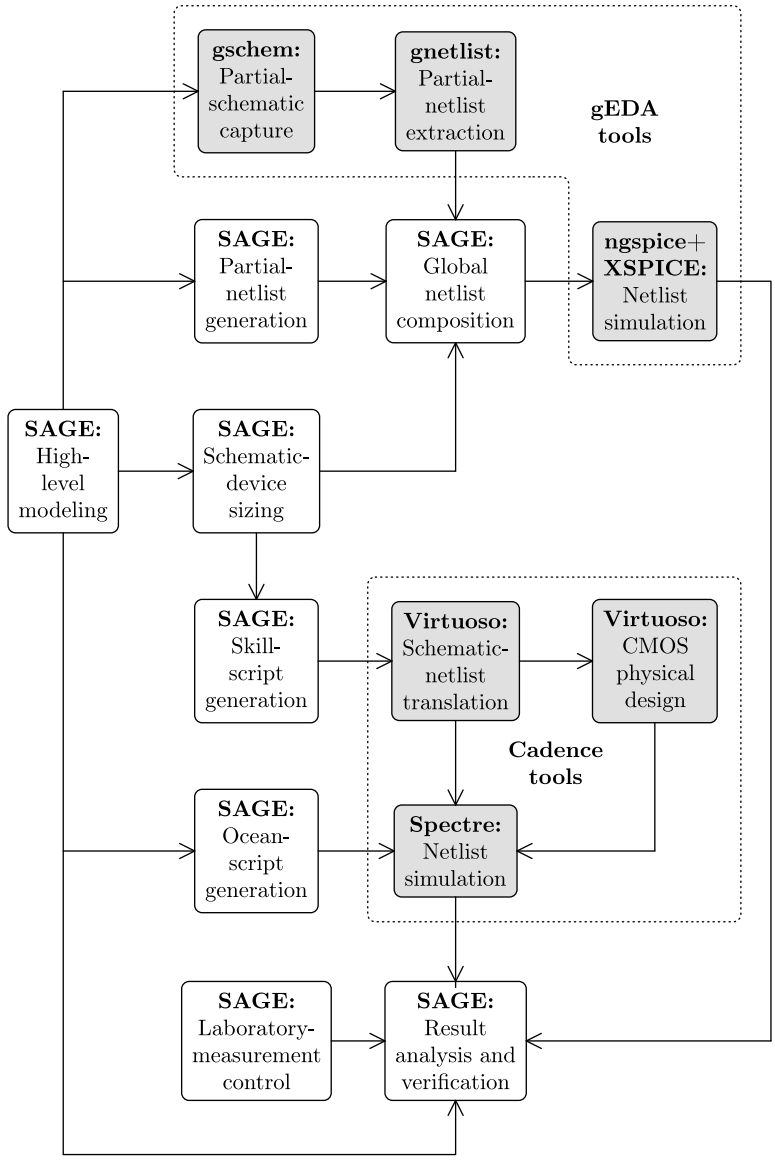

Figure 4.1 Design environment employed for the ΔΣM research. The scripts developed using SAGE are boxed in white, and the external tools directed by these scripts are boxed in gray.

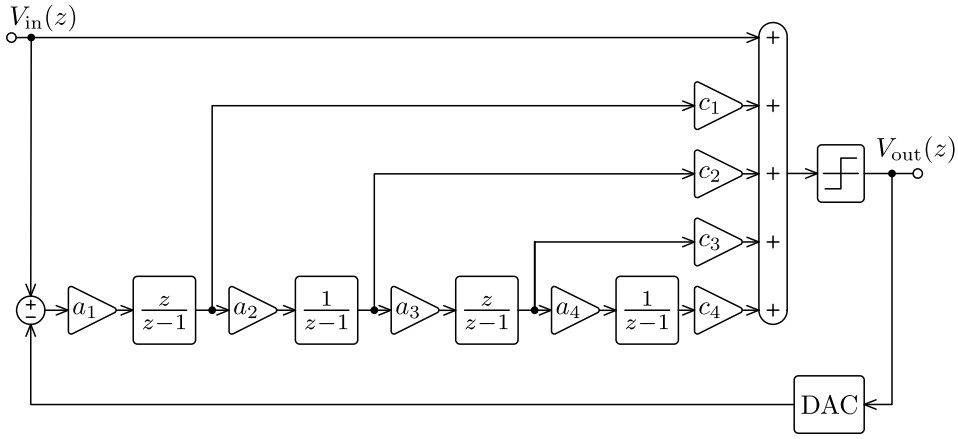

Figure 4.2 | High-level model of the ΔΣM architecture.

tecture differs from the architecture in [90] by the absence of the z^{-1} delay in the first and third stages because of the SVMA half-cycle operation-time alternation. Thus, it must be checked whether this resulting architecture is still stable for a certain coefficient mismatch.

First, it is checked whether the ΔΣM STF is of all-pass type, presenting the ΔΣM-architecture feedforward attributes discussed in Section 2.1. Replacing the quantizer and DAC blocks by their equivalent linear model as in Fig. 2.2, the characteristic equation of diagram in Fig. 4.2 is

$$V_{\text{out}}(z) = V_{\text{in}}(z) + \frac{a_1 z}{z-1}\left(\frac{a_2 a_3 z}{(z-1)^2}\left(\frac{a_4 c_4}{z-1} + c_3\right) + \frac{a_2 c_2}{z-1} + c_1\right) \cdot \left(V_{\text{in}}(z) - V_{\text{out}}(z)\right). \tag{4.1}$$

It can be simplified as

$$V_{\text{out}}(z) = V_{\text{in}}(z) + H(z)\left(V_{\text{in}}(z) - V_{\text{out}}(z)\right), \tag{4.2}$$

where $H(z)$ is defined by

$$H(z) = \frac{a_1 z}{z-1}\left(\frac{a_2 a_3 z}{(z-1)^2}\left(\frac{a_4 c_4}{z-1} + c_3\right) + \frac{a_2 c_2}{z-1} + c_1\right). \tag{4.3}$$

The resulting STF is

$$\mathrm{STF}(z) = \frac{V_{\mathrm{out}}(z)}{V_{\mathrm{in}}(z)} = \frac{1 + H(z)}{1 + H(z)} = 1. \tag{4.4}$$

As expected, the STF in (4.4) corresponds to the wanted profile of a feed-forward ΔΣM architecture. To find the NTF, a modification of the block diagram in Fig. 4.2 is employed, shown in Fig. 4.3, assuming the quantizer and DAC linear models as in Fig. 2.2.

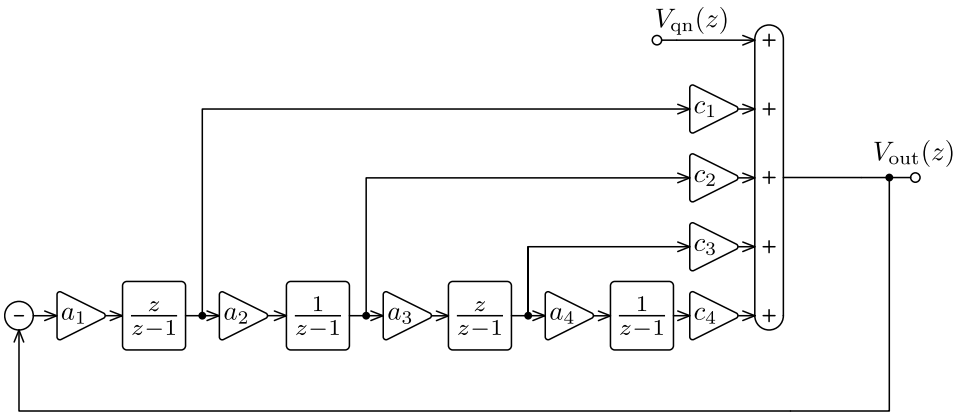

Figure 4.3 High-level model of the ΔΣM architecture for the NTF estimation.

The NTF is found as

$$\mathrm{NTF}(z) = \frac{V_{\mathrm{out}}(z)}{V_{\mathrm{qn}}(z)} = \frac{N_{\mathrm{zeros}}(z)}{D_{\mathrm{poles}}(z)}, \tag{4.5}$$

where $N_{\text{zeros}}(z)$ is the numerator

$$N_{\text{zeros}}(z) = (z-1)^4, \tag{4.6}$$

showing that all zeros of the NTF are at $z = 1$; and D_{poles} is the denominator

$$\begin{aligned} D_{\text{poles}}(z) = {} & a_1 c_1 z^4 + a_1 \left(3c_1 - a_2 \left(c_2 + a_3 c_3\right)\right) z^3 \\ & + a_1 \left(3c_1 - 2a_2 c_2 - a_2 a_3 \left(c_3 - a_4 c_4\right)\right) z^2 + a_1 \left(a_2 c_2 - c_1\right) z + 1. \end{aligned} \tag{4.7}$$

Finding the poles of the NTF from (4.7) results in long expressions, which are inappropriate for manual design. Therefore, a high-level discrete-time simulation is used to check the loop performance and stability. Although the architecture differs from the architecture reported in [90], the same coefficients are adopted (Table 4.1) and their robustness is verified as will be explained below.

Coefficient	a_1	a_2	a_3	a_4	c_1	c_2	c_3	c_4
Value	0.4	0.4	0.1	0.1	1	1	1	2

Table 4.1 | Gain coefficients for the ΔΣM architecture of Fig. 4.2.

Time-domain simulations are run using several sine-wave input amplitudes and OSRs for a fixed input frequency of 13.28 kHz and the specified bandwidth of 50 kHz. The chosen input frequency of 13.28 kHz will allow to evaluate the second and third harmonics in the required 50-kHz bandwidth when dealing with circuit non-idealities in the next sections. Each simulation provides its own output sequence. The PSD is estimated by the use of the FFT, and the SQNR is evaluated for all sequences. Fig. 4.4 shows the spectrum of a -2-dB_{FS} sinusoidal input using an OSR of 136, which is selected for the further design as the minimum OSR to achieve a reasonable SQNR margin with respect to the required SNDR. The SQNR for these parameters is maximum (SQNR_{max}) and of 117 dB, corresponding to the SQNR margin higher than 15 dB, which is commonly employed in

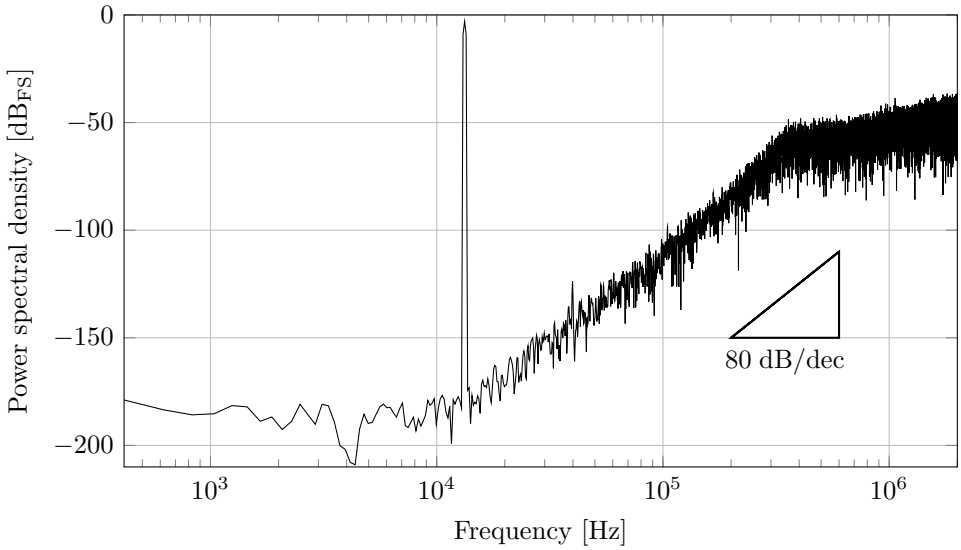

Figure 4.4 | Output spectrum of the ΔΣM high-level model of Fig. 4.2 for a -2-dB_{FS} sinusoidal input.

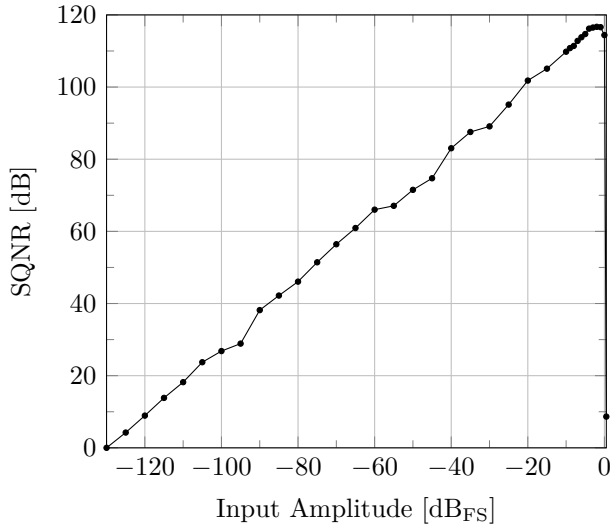

Figure 4.5 | Simulated SQNR versus input amplitude of the ΔΣM high-level model of Fig. 4.2.

industrial designs [27]. An 80-dB/dec noise-shaping slope in the spectrum of Fig. 4.4, certifies the ΔΣM fourth-order transfer function.

The complete input-amplitude sweep is shown in Fig. 4.5. The input full scale is optimized using the feedback-DAC gain of 0.45, so that the modulator is stable and provides the target performance up to 0-dB_{FS} input amplitude.

Following the procedure proposed in Section 2.3, the stability of the ΔΣM is verified under different coefficient-mismatch conditions. For a given worst-case coefficient mismatch ϵ_{mism}, as our architecture has eight coefficients, $2^8 = 256$ combinations are needed to include the minimum and maximum values of each coefficient. Thus, 256 input-amplitude sweeps must be performed and the worst $SQNR_{max}$ ($SQNR_{max,worst}$) is provided as a result. Fig. 4.6 shows the simulation results for ϵ_{mism} ranging from 0 to 15 %. It can be seen that, although slightly decreasing the SQNR, the ΔΣM is stable and complaint with the specifications up to ϵ_{mism} of 8.25 %, which is much larger than the typical capacitor mismatch-error values in a practical SC ΔΣM design. Therefore, the robustness of the chosen coefficients is proved.

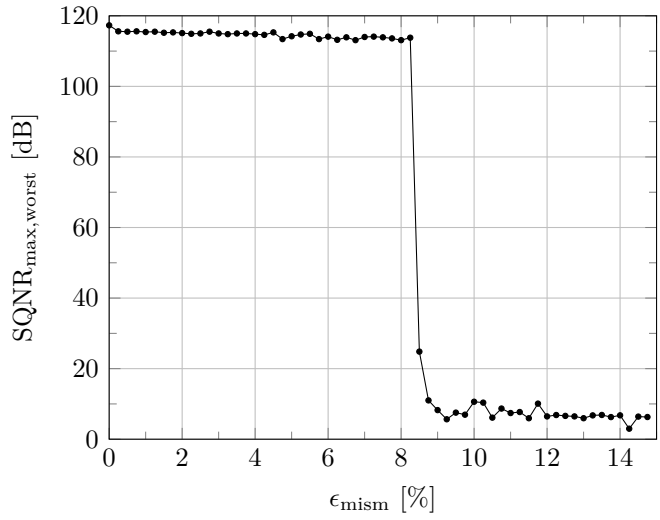

Figure 4.6 | Simulated $SQNR_{max,worst}$ versus coefficient mismatch for the ΔΣM high-level model of Fig. 4.2.

Next step is to determine the maximum settling error ϵ_{sett} allowed at the outputs of the integrators, for which the $\Delta\Sigma$M performance is preserved. Fig. 4.7 shows the simulation results for ϵ_{sett} ranging from 0 to 0.2 %, using the algorithm proposed in Section 2.3. It can be seen that SQNR_{max} is a stronger function of ϵ_{sett} at smaller errors. To comply with the specifications, ϵ_{sett} of 0.035 % is chosen. In Section 4.4.1, ϵ_{sett} will be used to estimate the minimum open-loop DC gain and the minimum GBW of the integrator SVMAs.

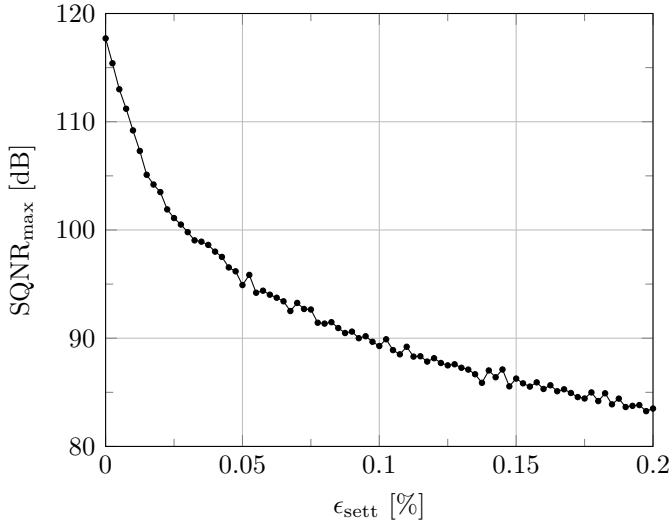

Figure 4.7 Simulated SQNR_{max} versus settling error ϵ_{sett} for the $\Delta\Sigma$M high-level model of Fig. 4.2.

4.3 Switched-Capacitor Implementation

Fig. 4.8 introduces the SC fully-differential circuit of the $\Delta\Sigma$M architecture presented in Fig. 4.2. The switches are implemented using complementary transmission gates without employing any bootstrapping techniques, thus operating at the nominal supply voltage of the target CMOS technology. Because of the SVMA usage in all stages, power consumption is reduced

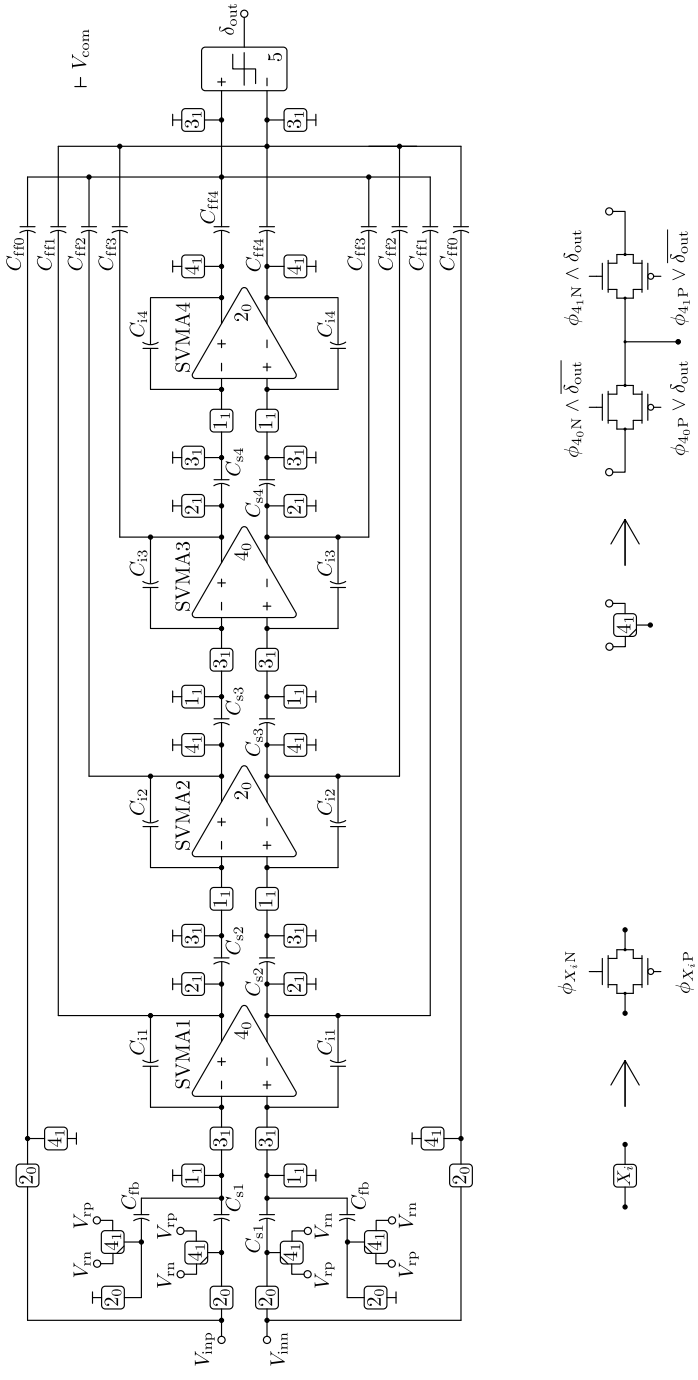

Figure 4.8 | SC schematic for the ΔΣM high-level model of Fig. 4.2.

and there is no need for critical switches at the outputs of the integrators, as discussed in Section 3.3. The feedforward switches are one of the main sources of distortion due to a high supported signal swing [77]. Their optimization will be closely inspected in Section 4.4.2.

The capacitors are implemented using MIM devices. The value of the input sampling capacitors C_{s1} is derived from the $k_B T/C$ noise specifications using (2.11). For the maximum operation temperature, the chosen OSR value of 136 and the SNR margin of 9 dB with respect to the target resolution, C_{s1} results in 41 pF. According to (2.13), the sampling capacitors of the following integrator stages C_{s2-4} must be at least 181 fF for the second stage, 362 aF for the third stage and 14 aF for the forth stage. These values are much smaller than the values the employed technology allows. For this reason and taking into account power-consumption minimization, we choose $C_{s2} = C_{s1}/12$ and $C_{s3-4} = C_{s2}/4$. The final capacitor values are listed in Table 4.2. The integrating capacitor values C_{i1-4} are derived from their sampling counterparts C_{s1-4} and the corresponding integrator coefficients a_{1-4}.

Capacitance	**Value**	**Capacitance**	**Value**	**Capacitance**	**Value**
C_{fb}	21.16			C_{ff0}	0.92
C_{s1}	42.32	C_{i1}	211.6	C_{ff1}	0.92
C_{s2}	3.68	C_{i2}	9.2	C_{ff2}	0.92
C_{s3}	0.92	C_{i3}	9.2	C_{ff3}	0.92
C_{s4}	0.92	C_{i4}	9.2	C_{ff4}	1.84

Table 4.2 Capacitance values in pF for the ΔΣM SC schematic of Fig. 4.8.

The feedforward capacitors C_{ff0-4} are chosen according to the minimum 0.92-pF capacitor in the design and meeting the ratios of the c_{1-4} feedforward coefficients fixed in Table 4.1. These capacitors form the summation elements of the passive adder.

Ideally, the 1.8-V standard supply of the employed CMOS technology can provide up to a 3.6-V_{pp} differential full scale (FS). However, due to the SVMA single-stage topology of the integrators with the cascode transistors

limiting the output swing, the differential FS of the full ΔΣM is limited to 2.4 V_{pp}. For this reason, the single-bit feedback DAC is implemented by a voltage references V_{rn} of 0.36 V, V_{rp} of 1.44 V and the partial feedback capacitors C_{fb} of 21.16 pF, which are sized for the feedback-DAC gain of 0.45. Also, the switching scheme discussed below reuses the sampling capacitors C_{s1} as the main part of the feedback summation element, thus reducing the overall circuit area [77].

The clock generator in Fig. 4.9 is designed to implement the ΔΣM-phase switching scheme in Fig. 4.10. It consists of a specific phase-splitter circuit in charge of generating dedicated phases for each NMOS and PMOS device used, as shown in Fig. 4.8, in four switch and SVMA locations of the integrators plus the quantizer. The generated control sequence of Fig. 4.10 ensures that the right-hand switches of the sampling capacitors C_{s1-4} are opened before their left-hand counterparts. As it is discussed in Section 3.3, no differential signal-dependent charge injection is sampled, but only a constant amount is rejected by the SVMA CMFB. Thus, signal distortion is reduced.

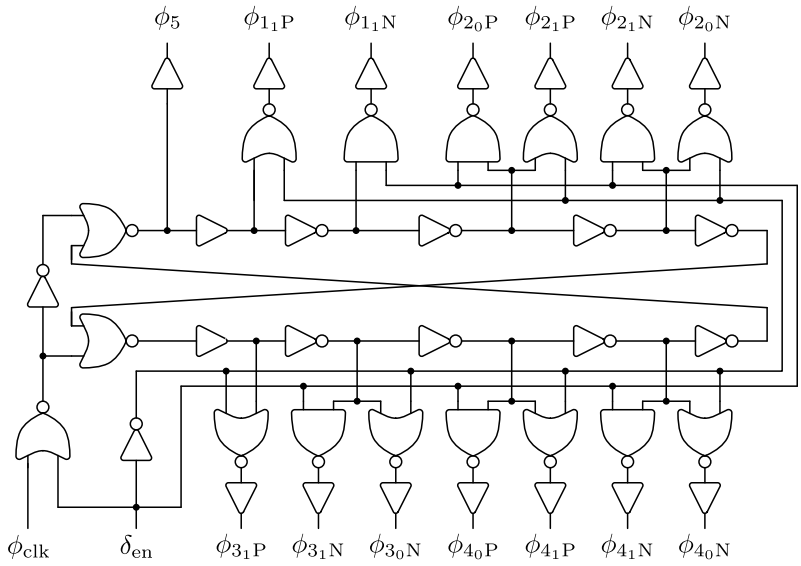

Figure 4.9 | Clock generator for the control of the phases in the ΔΣM SC schematic of Fig. 4.8.

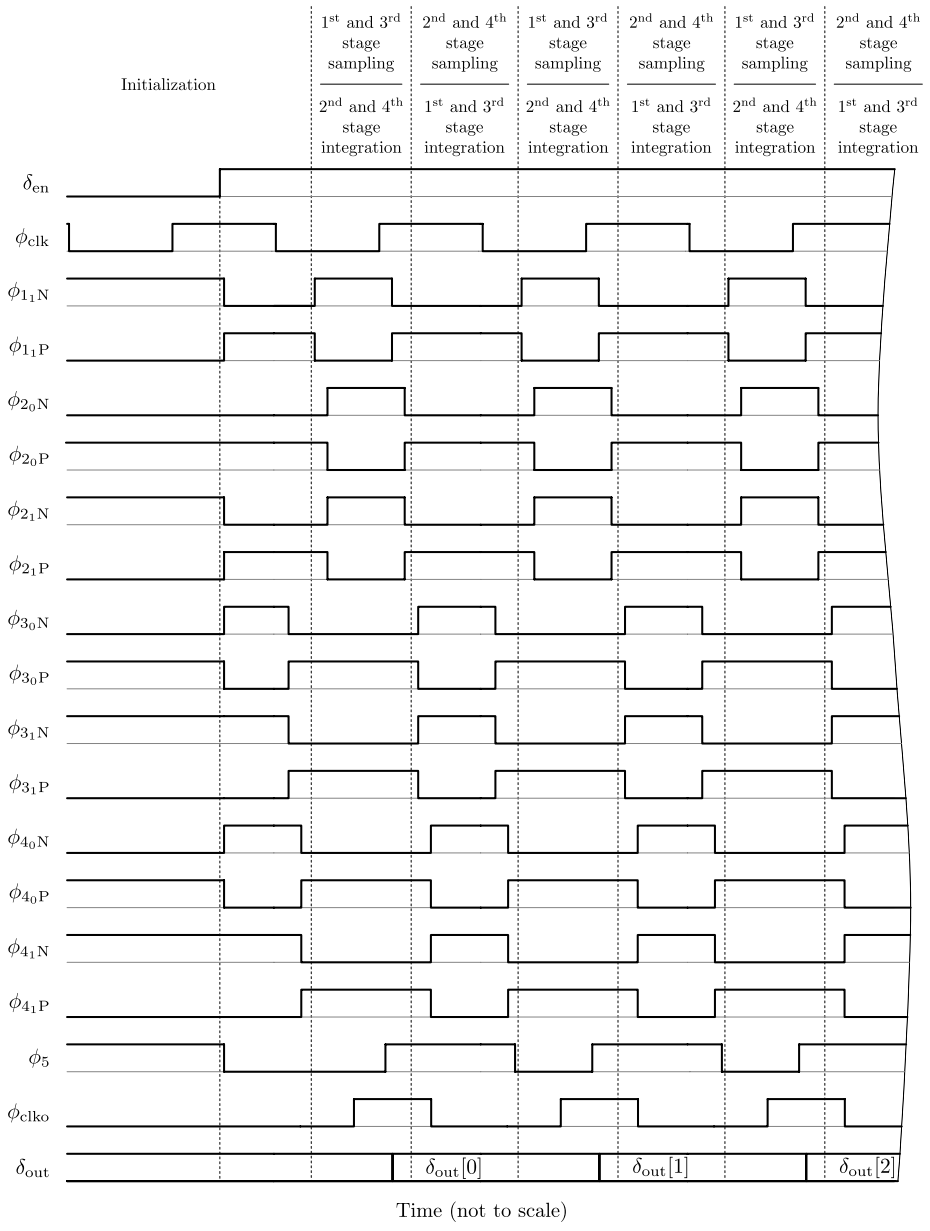

Figure 4.10 | Operation chronogram obtained from the generator of Fig. 4.9 for the ΔΣM SC schematic of Fig. 4.8.

The clock-generator masking scheme employs the enable input δ_{en} to force a determined position of all phases during the initialization state, so that all capacitors are precharged to the known voltage, the SVMAs are disabled and the shortcircuits through the switches between the input and reference voltage sources are prevented, as shown in Fig. 4.11. After the initialization is completed, the first-half-cycle phases ϕ_1 and its delayed copy ϕ_2 configure the switches to perform the following operations, as illustrated in Fig. 4.12:

- C_{fb} discharge;
- sampling operation into C_{s1} and C_{s3} in the first and third stages;
- integration operation in the second and forth stages;
- summation operation of the feedforward signals.

The phase ϕ_5 triggers the quantization operation slightly before the end of of the ϕ_1, so that the feedback DAC has its output updated for the next half-cycle period.

Fig. 4.13 shows the ΔΣM schematic in the second half-cycle period. The phases ϕ_3 and its delayed copy ϕ_4 configure the switches to perform:

- C_{ff0}, C_{ff2} and C_{ff4} discharge;
- sampling operation into C_{s2} and C_{s4} in the second and forth stages;
- integration operation in the first and third stages;
- summation operation of the previously obtained feedback-DAC result.

The digital output of the ΔΣM δ_{out} can be sampled by the successive stages either on the rising or falling edge of the synchronization clock output $\phi_{2_0\text{clko}}$, which is derived from $\phi_{2_0\text{N}}$ and delayed by a buffer chain for this purpose, as shown in the chronograph of Fig. 4.10.

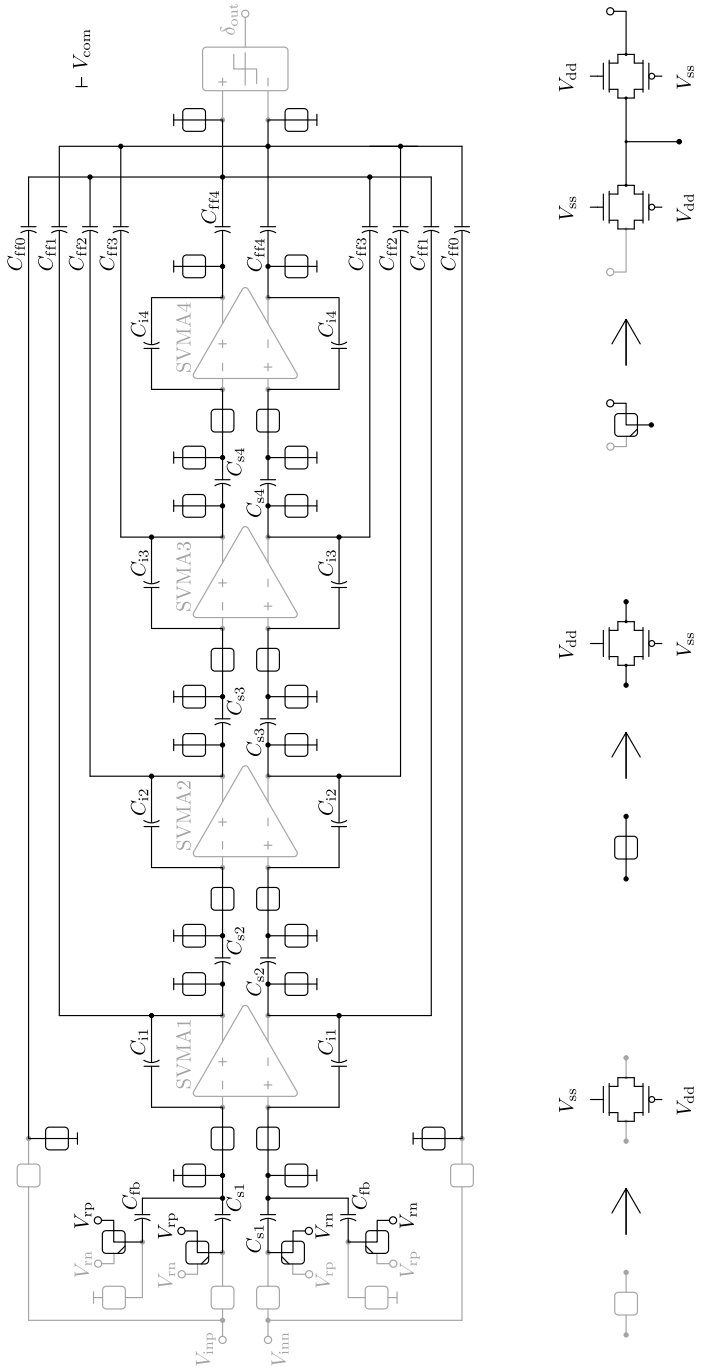

Figure 4.11 | Initialization state, when $\delta_{\mathrm{out}}\,(t=0) = V_{\mathrm{dd}}$, for the $\Delta\Sigma$M SC schematic of Fig. 4.8.

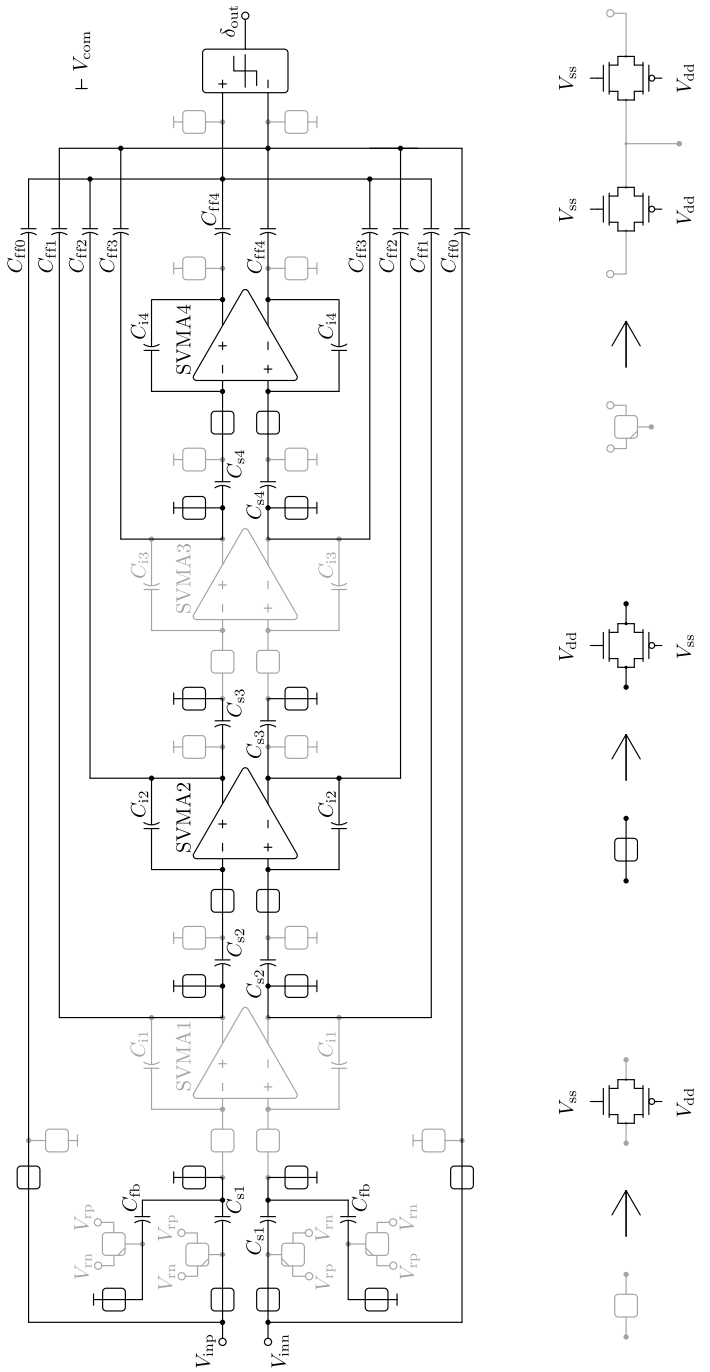

Figure 4.12 | The $\phi_{1,2,5}$ state for the ΔΣM SC schematic of Fig. 4.8.

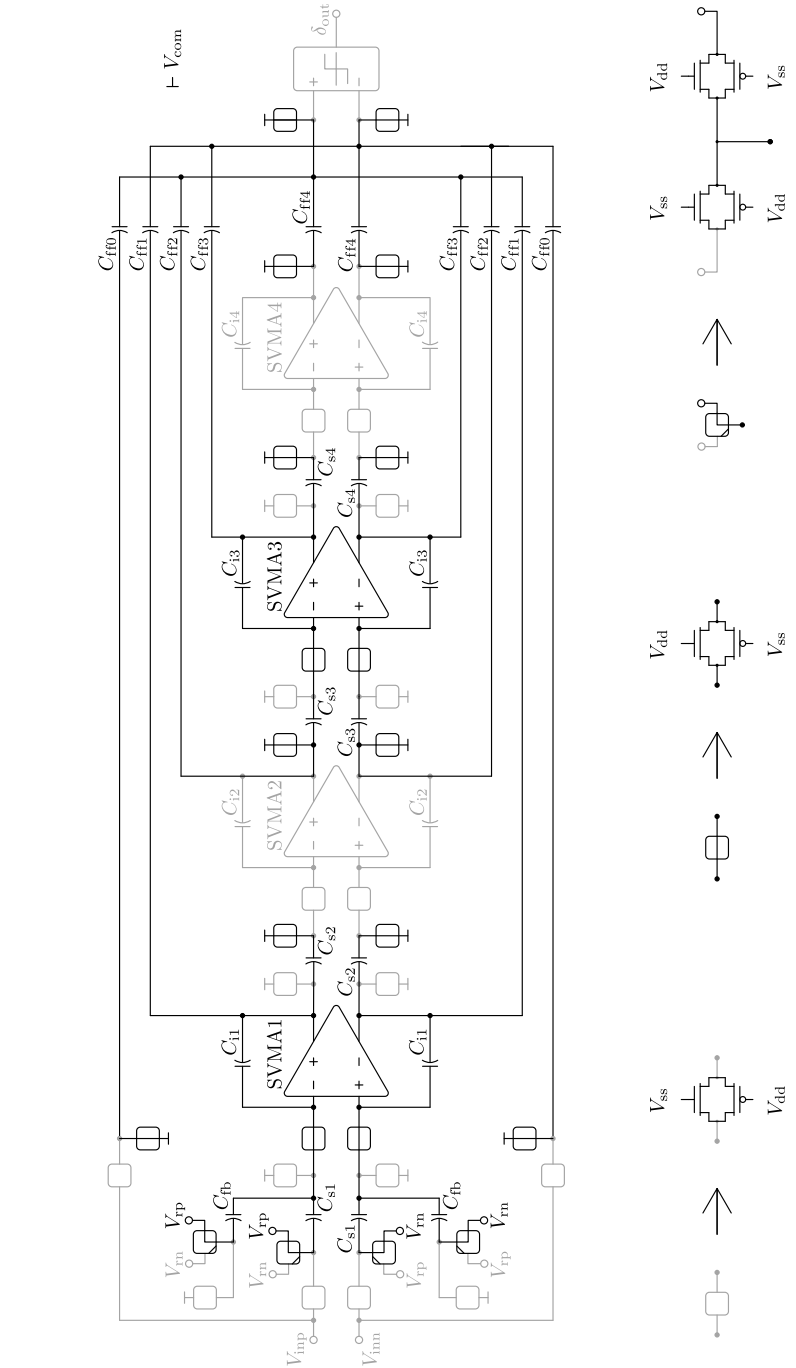

Figure 4.13 | The $\phi_{3,4}$ state, when $\delta_{out}(t = 0) = V_{dd}$, for the $\Delta\Sigma$M SC schematic of Fig. 4.8.

4.4 Mixed-Mode Electrical Simulation

This section discusses the ΔΣM electrical optimization. It starts with the optimization of the circuit blocks such as the integrator SVMAs and finishes with the simulation of the complete ΔΣM mixed-mode model.

4.4.1 Switched VMA Optimization

In the previous sections of this chapter, the switched-operation timing parameters and capacitors have been defined according to the ΔΣM high-level model and non-ideality constrains. Here, they are used to derive the integrator SVMA specifications.

In order to optimize each SVMA separately, its equivalent load conditions need to be extracted. The schematic for the SVMA-optimization transient measurements is shown in Fig. 4.14. The ΔΣM capacitor network is simplified for each SVMA as follows, with the results listed in Table 4.3.

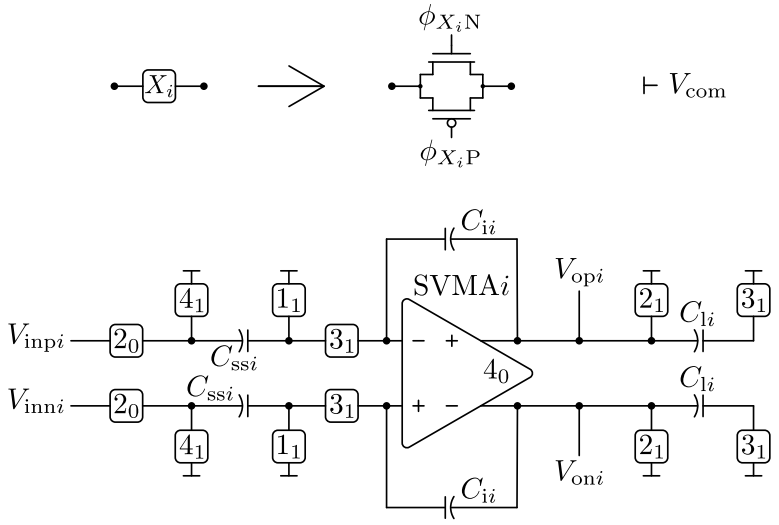

Figure 4.14 Test schematic for the integrator-SVMA optimization transient measurements.

Parameter	SVMA1	SVMA2	SVMA3,4	Units
$C_{\mathrm{ss}i}$	63.48	3.68	0.92	pF
$C_{\mathrm{i}i}$	211.6	9.2	9.2	pF
$C_{\mathrm{l}i}$	4.6	1.84	1.84	pF

Table 4.3 Equivalent capacitors derived from the ΔΣM SC network of Fig. 4.8 for individual SVMA optimization.

The equivalent sampling capacitor $C_{\mathrm{ss}i}$ is the sum of C_{s1} and C_{fb} for the SVMA1. For the SVMA2-4, it is equal to the corresponding $C_{\mathrm{s}i}$. The integrating capacitor $C_{\mathrm{i}i}$ is the same as in the ΔΣM SC network of Fig. 4.8. The equivalent load capacitor $C_{\mathrm{l}i}$ is the sum of the following-stage sampling capacitor $C_{\mathrm{s}(i+1)}$ and the corresponding $C_{\mathrm{ff}i}$ for the SVMA1-3. For the SVMA4, $C_{\mathrm{l}i}$ is equal to C_{ff4}. As the SVMA3 and the SVMA4 exhibit the same load and timing conditions, the number of SVMAs to optimize is reduced to three.

The optimization circuit in Fig. 4.14 employs the same clock generator presented in Fig. 4.9. First, the half-cycle phases ϕ_1 and its delayed copy ϕ_2 configure the switches to precharge $C_{\mathrm{ss}i}$ to the maximum voltage which can occur during ΔΣM operation. And then, the following half-cycle phases ϕ_3 and its delayed copy ϕ_4 configure the switches to perform the integration operation. The transition of the differential output voltage $V_{\mathrm{op}i} - V_{\mathrm{on}i}$ is analyzed, extracting the integration time t_{int} as a period from the start of the operation until the output is settled within the specified error margin. The resulting t_{int} must be smaller than the maximum operation time available for the integration t_{op}, given for the SC scheme by

$$t_{\mathrm{op}} = \frac{1}{4 \cdot \mathrm{BW} \cdot \mathrm{OSR}} - t_{\mathrm{m}}, \tag{4.8}$$

where t_{m} is the time margin including the idle periods between the non-overlapping phases and the clock rise and fall delays. Choosing t_{m} of 8.7 ns for the specified BW of 50 kHz and the OSR of 136, t_{op} of 28 ns is obtained. The switches in Fig. 4.14 are implemented using the same transmission gates as in full ΔΣM scheme to account for their parasitic effects in simulation. For the analytical simplicity, however, the open switches will be assumed as

inexistent and the closed switches will be assumed as ideal shorts. Analyzing the circuit of Fig. 4.14 in the integration phase, the feedback factor β_{fb} is found as

$$\beta_{\mathrm{fb}} = \frac{C_{\mathrm{i}i}}{C_{\mathrm{ss}i} + C_{\mathrm{i}i}}. \tag{4.9}$$

The effective load capacitor $C_{\mathrm{leff}i}$ for the open-loop AC analysis of the circuit of Fig. 4.15 is

$$C_{\mathrm{leff}i} = C_{\mathrm{l}i} + (1 - \beta_{\mathrm{fb}})C_{\mathrm{i}i}. \tag{4.10}$$

The dummy transmission gates in Fig. 4.15 are also used in series with $C_{\mathrm{leff}i}$ in electrical simulations. For the manual analysis, they are replaced by ideal shorts. The SC CMFB in this configuration is replaced by a continuous-time resistive equivalent, which will be reviewed in detail in Section 5.1.1. The ratio between the effective and equivalent load capacitors $C_{\mathrm{leff}i}/C_{\mathrm{l}i}$ is found to be important while optimizing the SVMAs. For smaller $C_{\mathrm{leff}i}/C_{\mathrm{l}i}$, the simulation results are in closer accordance with the proposed analytical approximation, due to the fact that the unaccounted parasitics of the $C_{\mathrm{ss}i}$ and $C_{\mathrm{i}i}$ nodes have less impact on the poles and zeros of the transfer function. Thus, the approximation (4.10) implies the dominant pole at the output of the SVMA to be close to the origin and the rest to be at frequencies higher than the GBW.

The minimum open-loop gain A_{open} required to reach the desired settling precision can be approximated by

$$A_{\mathrm{open}} = \frac{1}{\beta_{\mathrm{fb}}\epsilon_{\mathrm{sett}}}. \tag{4.11}$$

Two periods can be distinguished during t_{op} [91]:

$$t_{\mathrm{op}} = t_{\mathrm{slew}} + t_{\mathrm{sett}}, \tag{4.12}$$

where t_{slew} is the slewing period and t_{sett} is the settling period. During t_{slew}, the SVMA operates in the Class-AB region and provides the maximum

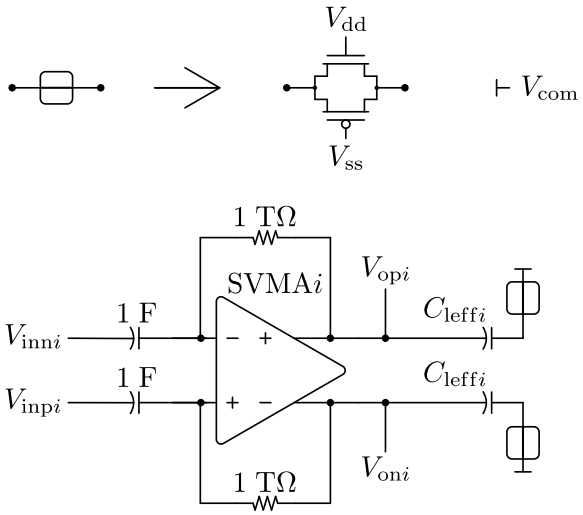

Figure 4.15 | Test schematic for the SVMA-optimization AC measurements.

slewing current $I_{\max}$ to the load according to (3.48). At the transition from t_{slew} to t_{sett}, the SVMA enters the Class-A region and the output settles according to the AC parameters for the balanced condition such as A_{open} and GBW. The ratio between t_{sett} and t_{slew} is variable during the optimization process until the best trade-off between the SVMA parameters is reached. It is decided to start the optimization with $t_{\mathrm{slew}}/t_{\mathrm{sett}}$=3. For the given t_{slew}, the minimum slew rate (SR) needed to linearly and ideally reach the highest possible voltage step V_{step} occurring during ΔΣM operation is

$$\mathrm{SR} = \frac{V_{\mathrm{step}}}{t_{\mathrm{slew}}}. \tag{4.13}$$

Thus, the minimum slewing current $I_{\max}$ needed to charge $C_{\mathrm{leff}i}$ to V_{step} is

$$I_{\max} = \mathrm{SR} \cdot C_{\mathrm{leff}i}. \tag{4.14}$$

During t_{sett}, the maximum time constant τ to settle with the required pre-

cision ϵ_{sett} can be approximated as

$$\tau = \frac{t_{\text{sett}}}{\ln \epsilon_{\text{sett}}^{-1}}. \tag{4.15}$$

The minimum SVMA output transconductance G_{m} needed to reduce τ to the desired value is

$$G_{\text{m}} = \frac{C_{\text{leff}i}}{\beta_{\text{fb}}\tau}. \tag{4.16}$$

The GBW for the presented analytical approximation is

$$\text{GBW} = \frac{G_{\text{m}}}{2\pi C_{\text{leff}i}}. \tag{4.17}$$

Substituting (4.15) and (4.16) into (4.17), the minimum required GBW is obtained:

$$\text{GBW} = \frac{\ln \epsilon_{\text{sett}}^{-1}}{2\pi\beta_{\text{fb}} t_{\text{sett}}}. \tag{4.18}$$

The SVMA specifications extracted according to the equations discussed above are tabulated in Table 4.4.

Once all specifications are defined, it is proceeded to the optimization process. All SVMAs are implemented using the schematic presented in Fig. 3.13. The channel lengths of all transistors are fixed, setting them to the minimum length allowed by the employed CMOS technology L_{min}, except $L_{\text{MB1}-3}$ and $L_{\text{MT1}-2}$, which are $2 \times L_{\text{min}}$.

As explained in Section 3.3, the SVMA design variables which are swept during the optimization are the k_{b} ratio between the output and input branches, the tail current of the input pairs I_{tail}, the inversion coefficients of the transistor groups, and the k_{z} ratio controlling the Class-AB behavior.

Initially, k_{b}, k_{z} and all inversion coefficients are set to the value of 1. For the inversion coefficients, this value from the moderate inversion region is chosen

Parameter	SVMA1	SVMA2	SVMA3,4	Units
β_{fb}	0.77	0.71	0.91	
$C_{\mathrm{leff}i}$	53.4	4.47	2.68	pF
$C_{\mathrm{leff}i}/C_{\mathrm{l}i}$	11.6	2.43	1.46	
A_{open}	71.4	72	69.9	dB
SR	46	61.3	15.3	$\frac{\mathrm{V}}{\mu\mathrm{s}}$
I_{max}	2.46	0.274	0.041	mA
GBW	77.9	83.9	65.9	MHz

Table 4.4 SVMA specifications for the ΔΣM SC schematic of Fig. 4.8.

as a minimum limit yielding the maximum acceptable silicon area. The current I_{tail} is set to twice I_{max} from the extracted specifications, dismissing Class-AB behavior for the first optimization iterations.

During the optimization process, k_{b}, k_{z} and all inversion coefficients are maximized and I_{tail} is minimized, maintaining an adequate phase margin (PM), A_{open} close to the specified value and t_{int} lower than t_{op}, as illustrated in Fig. 4.16. The SR and the GBW are allowed to vary together with the floating $t_{\mathrm{slew}}/t_{\mathrm{sett}}$ ratio. The CMFB capacitors C_{cmfb} are sized proportionally to the gate-channel capacitance C_{gch} of the transistor MT1 in Fig. 3.13, which is approximated by [84]:

$$C_{\mathrm{gch}} = C_{\mathrm{gd}} + C_{\mathrm{gs}}, \tag{4.19}$$

where C_{gd} is the gate-drain capacitance and C_{gs} is the gate-source capacitance. For the transistor MT1 operating in saturation,

$$C_{\mathrm{gd}} = WC_{\mathrm{ov}}, \tag{4.20}$$

where C_{ov} is the source/drain overlap capacitance per unit of the channel

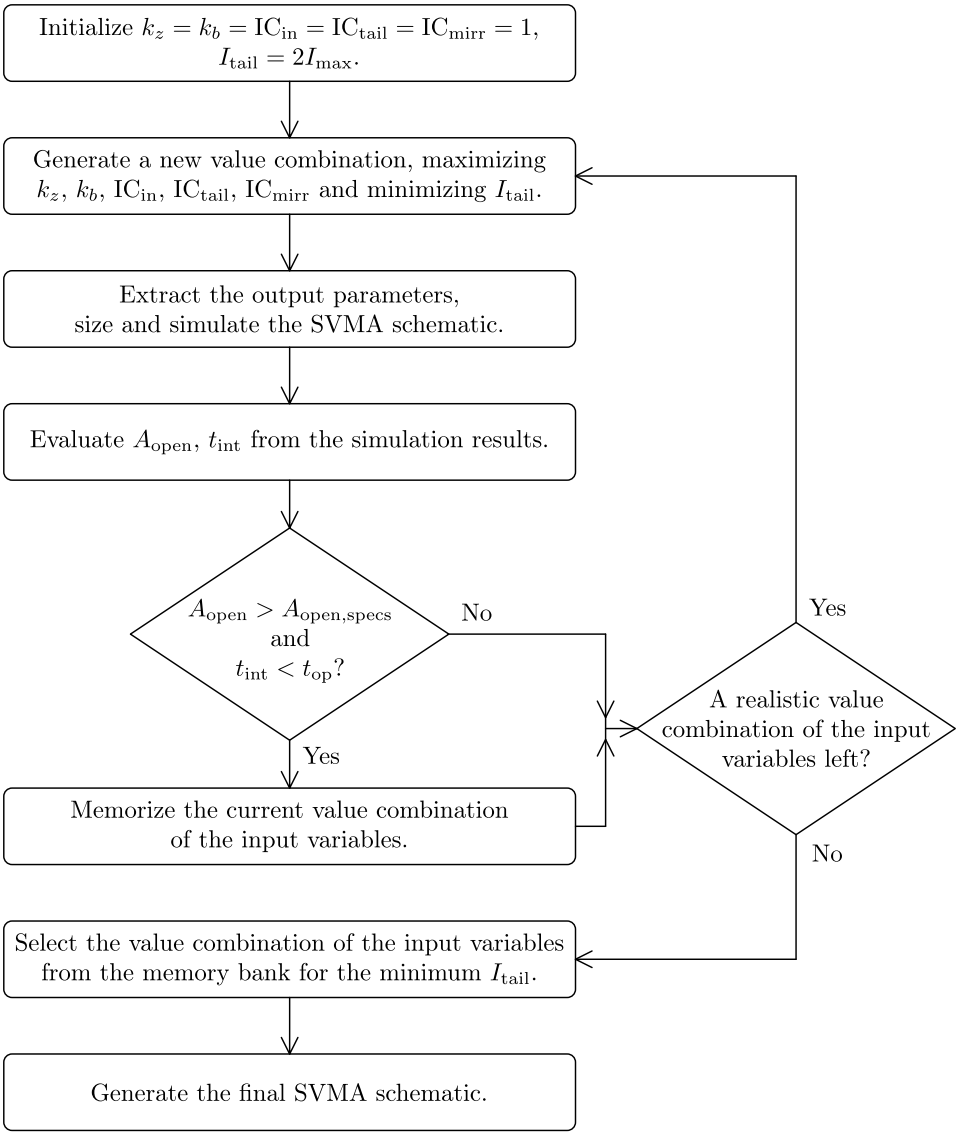

Figure 4.16 | Optimization flow diagram of the integrator SVMAs for the ΔΣM SC schematic of Fig. 4.8.

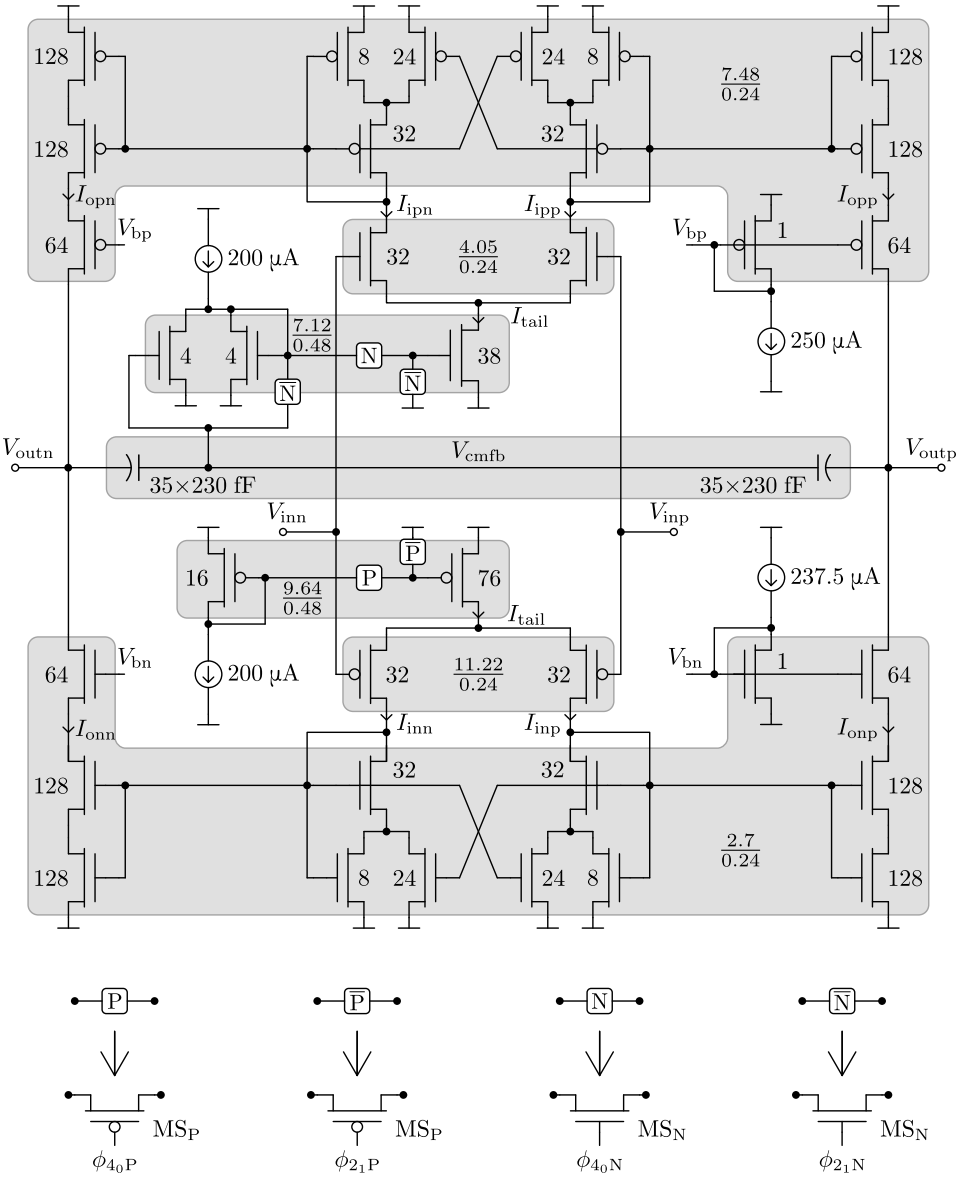

Figure 4.17 | SVMA optimal sizing for the first integrator of the ΔΣM SC schematic of Fig. 4.8.

width W; and,

$$C_{\mathrm{gs}} = \frac{2}{3} W L C_{\mathrm{ox}} + W C_{\mathrm{ov}}, \tag{4.21}$$

where C_{ox} is the oxide capacitance per unit area. Substituting (4.20) and (4.21) into (4.19), C_{gch} is obtained as

$$C_{\mathrm{gch}} = 2W \left(\frac{1}{3} L C_{\mathrm{ox}} + C_{\mathrm{ov}} \right). \tag{4.22}$$

Following the optimization diagram in Fig. 4.16, an example of the sized schematic for the SVMA1 is presented in Fig. 4.17. Excluding switches, the full design employs only six types of transistor unitary element, thus simplifying the optimization process. In the case of SVMA1, the optimum combination of the design variables is found to be $k_{\mathrm{b}} = 4$, $k_{\mathrm{z}} = 3$, $\mathrm{IC_{in}}$=2, $\mathrm{IC_{tail}}$=4, $\mathrm{IC_{mirr}}$=6, and I_{tail}=950 µA.

Fig. 4.18 shows the k_{z} variable sweep for these values. It can be compared with the analytical and simulation sweeps of Fig. 3.6 and Fig. 3.7. To make the comparison easier, the k_{z} values in Fig. 4.18 are expressed in the same format and the output currents are normalized to I_{tail} as in Fig. 3.6 and Fig. 3.7. It is seen that, due to short-channel effects, I_{max} is decreased with respect to the expected value. For the selected k_{z} of 3, this deviation is plotted in absolute terms in Fig. 4.19. This is the reason why I_{tail} is chosen as an optimization variable instead of I_{max}.

Despite the I_{max} short-channel-effect decrease, the I_{max} deviation under different process corners and temperatures is minimal, as shown in Fig. 4.20. Here, two worst combinations are chosen: fast PMOS/NMOS at -40 °C; and, slow PMOS/NMOS at 80 °C. They are contrasted with the typical corner at 20 °C.

The Table 4.5 lists the final parameters of the optimized SVMA1 under different corner conditions. The most important parameters, the open-loop gain A_{open} and the integration time t_{int}, are complaint with the specifications. The phase margin is given for two different fulfillment conditions: $\mathrm{PM_1}$,

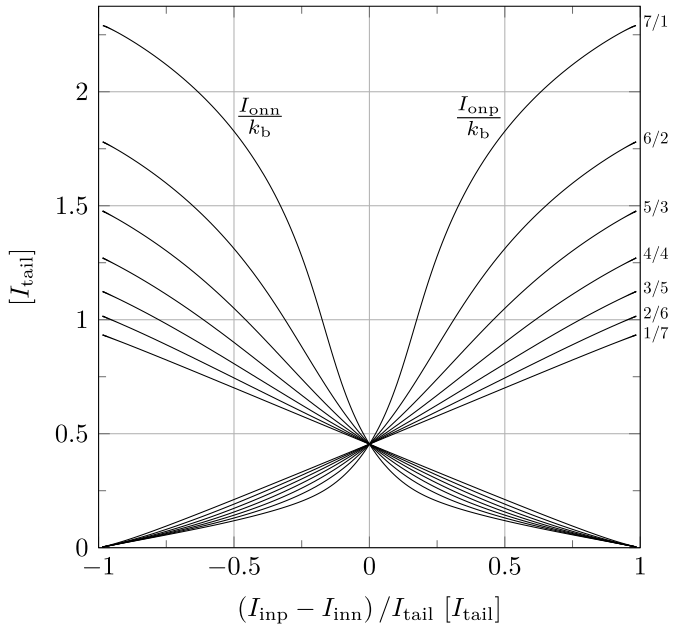

Figure 4.18 Example of simulated SVMA Class-AB current transfer curve for different k_{z} (on the right), with the same format as in Fig. 3.6 and Fig. 3.7.

Parameter	**typical 20 °C**	**fast -40 °C**	**slow 80 °C**	**Units**
A_{open}	74.1	74.7	73.9	dB
SR	139	146	133	$\frac{\mathrm{V}}{\mu\mathrm{s}}$
I_{max}	7.41	7.8	7.1	mA
GBW	221	250	206	MHz
PM_1	54	46.9	60.7	°
PM_β	55.8	48.9	62.8	°
$\mathrm{t}_{\mathrm{int}}$	16.41	14.24	19.57	ns

Table 4.5 Final parameters of the optimized SVMA1 under different process and temperature corner conditions.

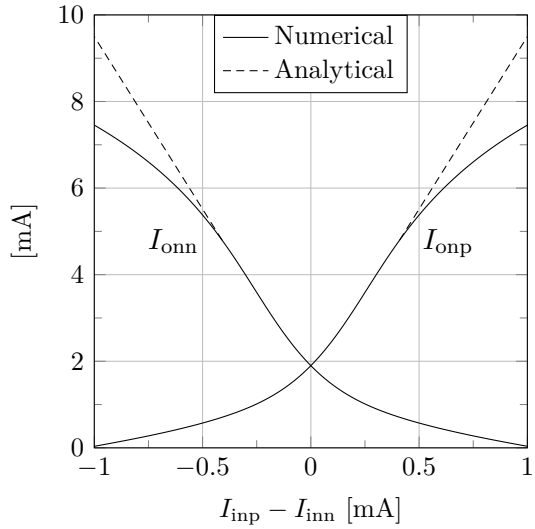

Figure 4.19 | SVMA1 simulated Class-AB DC current transfer curve.

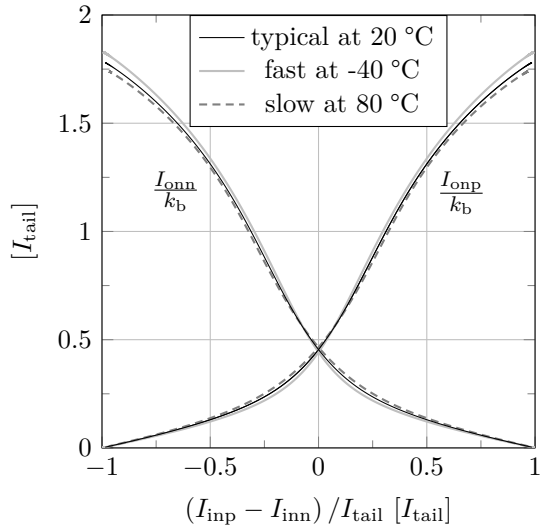

Figure 4.20 | SVMA1 simulated Class-AB DC normalized current transfer curve under corner conditions.

supposing the feedback factor β_{fb} of 1; and, PM_β, for the target β_{fb} value specified in Table 4.4. The phase margin PM_β should be fulfilled not at the frequency equal to the GBW, as in the case of PM_1, but at the frequency at which the gain is $1/\beta$ [91].

Because of a high ratio between the effective and equivalent load capacitors $C_{\text{leff}i}/C_{\text{l}i}$ for the SVMA1, the SR and the GBW have had to be increased more than twice the specified values. However, for the SVMA2-4, as $C_{\text{leff}i}/C_{\text{l}i}$ is much smaller, the SR and the GBW have not experienced much deviation from the analytical prediction. As listed in Table 4.6 of the final parameters for all SVMAs in typical conditions, the SR of the SVMA2 can be even more relaxed than the specified value, compensated by a slight increase in the GBW. It means that the ratio $t_{\text{slew}}/t_{\text{sett}}$ should not be maintained fixed during the optimization process. The designer should mainly focus on minimizing the power consumption and the area and maximizing the speed and the gain.

Parameter	**SVMA1**	**SVMA2**	**SVMA3,4**	**Units**
A_{open}	74.1	72.1	70.5	dB
SR	139	36.2	26	$\frac{\text{V}}{\mu\text{s}}$
I_{max}	7.41	0.162	0.07	mA
GBW	221	95.4	70.9	MHz
PM_1	54	77.8	83.1	°
PM_β	55.8	80.2	83.6	°
t_{int}	16.41	25.75	19.82	ns

Table 4.6 Final parameters of the optimized SVMAs, fulfilling the specifications of Table 4.4.

The device sizes for all SVMAs are listed in Table 4.7. Later in this chapter, the robustness of the designed SVMAs will be also demonstrated on the scale of the full $\Delta\Sigma$M circuit, allowing to achieve the target resolution under different process and temperature corner conditions.

Parameter	SVMA1	SVMA2	SVMA3,4	Units
C_{cmfb}	8050	437	218	fF
I_{a1}	250	50	50	µA
I_{a2}	237.5	50	50	µA
I_{b}	200	50	50	µA
$(W/L)_{\mathrm{MA1}}$	7.48/0.24	1.58/0.24	1.58/0.24	µm/µm
$(W/L)_{\mathrm{MA2}}$	2.7/0.24	0.57/0.24	0.57/0.24	µm/µm
$(W/L)_{\mathrm{MB1,2}}$	28.48/0.48	7.12/0.48	7.12/0.48	µm/µm
$(W/L)_{\mathrm{MB3}}$	154.24/0.48	38.56/0.48	38.56/0.48	µm/µm
$(W/L)_{\mathrm{MC1,2}}$	478.72/0.24	12.64/0.24	6.32/0.24	µm/µm
$(W/L)_{\mathrm{MC3,4}}$	172.8/0.24	4.56/0.24	2.28/0.24	µm/µm
$(W/L)_{\mathrm{MD1,2}}$	59.84/0.24	3.15/0.24	3.16/0.24	µm/µm
$(W/L)_{\mathrm{MD3,4}}$	21.6/0.24	1.14/0.24	1.14/0.24	µm/µm
$(W/L)_{\mathrm{MG1,2}}$	957.44/0.24	25.2/0.24	12.64/0.24	µm/µm
$(W/L)_{\mathrm{MG3,4}}$	345.6/0.24	9.12/0.24	4.56/0.24	µm/µm
$(W/L)_{\mathrm{MI1,2}}$	129.6/0.24	6.8/0.24	3.4/0.24	µm/µm
$(W/L)_{\mathrm{MI3,4}}$	359.04/0.24	18.96/0.24	9.44/0.24	µm/µm
$(W/L)_{\mathrm{ML1,2}}$	957.44/0.24	25.2/0.24	12.64/0.24	µm/µm
$(W/L)_{\mathrm{ML3,4}}$	345.6/0.24	9.12/0.24	4.56/0.24	µm/µm
$(W/L)_{\mathrm{MS_N}}$	16/0.18	0.96/0.18	0.48/0.18	µm/µm
$(W/L)_{\mathrm{MS_P}}$	144/0.18	8.64/0.18	4.32/0.18	µm/µm
$(W/L)_{\mathrm{MT1}}$	270.56/0.48	14.24/0.48	7.12/0.48	µm/µm
$(W/L)_{\mathrm{MT2}}$	732.64/0.48	38.56/0.48	19.28/0.48	µm/µm
$(W/L)_{\mathrm{MU1,2}}$	239.36/0.24	12.6/0.24	6.32/0.24	µm/µm
$(W/L)_{\mathrm{MU3,4}}$	86.4/0.24	4.56/0.24	2.28/0.24	µm/µm
$(W/L)_{\mathrm{MZ1,2}}$	179.52/0.24	9.45/0.24	3.16/0.24	µm/µm
$(W/L)_{\mathrm{MZ3,4}}$	64.8/0.24	3.42/0.24	1.14/0.24	µm/µm

Table 4.7 Device sizing parameters used for the SVMAs of the ΔΣM SC schematic of Fig. 4.8.

4.4.2 Feedforward Switches

As it has been pointed out in Section 4.3, the feedforward switches of Fig. 4.8 are one of the main sources of distortion due to a high supported signal swing [77]. In order to optimize them in the context of the target ΔΣM, but decoupling the effects of non-idealities deriving from other ΔΣM blocks, the fully-differential circuit in Fig. 4.21 is proposed. It is a simplified version of the circuit presented in Fig. 4.8.

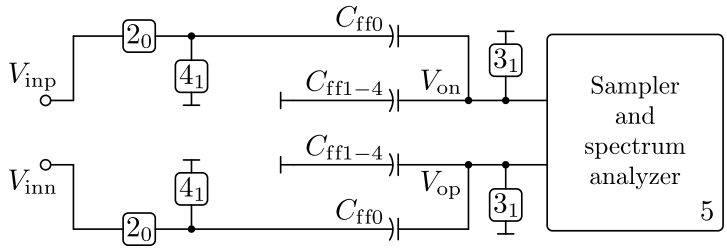

Figure 4.21 | Feedforward-switch optimization schematic.

The feedforward path of C_{ff0} is preserved and $C_{\mathrm{ff1-4}}$ is the sum of the rest of the feedforward capacitors, emulating the complete load seen at the passive-adder output. The optimization circuit in Fig. 4.21 employs the same clock generator presented in Fig. 4.9. First, the phases ϕ_3 and its delayed copy ϕ_4 configure the switches to discharge all capacitors, and then, the next half-cycle phase ϕ_2 configure the switches to perform the charge redistribution for the summation operation. The transition of the differential output voltage $V_{\mathrm{op}} - V_{\mathrm{on}}$ is sampled at the end of ϕ_2 by an ideal analog sampler implemented in XSPICE hardware-description language (HDL).

A ΔΣM-SQNR$_{\mathrm{max}}$ sinusoidal signal of a -2-dB$_{\mathrm{FS}}$ amplitude and the previously-chosen 13.28-kHz frequency is used at the input. The transient time is equivalent to several input sine-wave periods. The spectrum of the accumulated sampled sequence is analyzed using the FFT and the signal-to-distortion ratio (SDR) of the feedforward path is extracted. The resulting SDR must be higher than the target SNDR of the ΔΣM.

Initially, the NMOS-device width W_{n} and length L_{n} of the feedforward-switch transmission gates are set to the minimum W_{min} and L_{min} allowed

by the target CMOS technology. It is found that the best performance is achieved when the PMOS-device width W_p is scaled according to

$$W_\mathrm{p} = \frac{\mu_\mathrm{n}}{\mu_\mathrm{p}} W_\mathrm{n}, \tag{4.23}$$

where μ_n is the mobility of charge carriers in the N channel, and μ_p is the mobility of charge carriers in the P channel. It can be viewed as an improvement of symmetry between the NMOS- and PMOS-device operation by the mobility-mismatch compensation.

During the optimization, the device widths are being increased until the optimum performance is achieved. The optimum point is located where the devices are sufficiently wide, conducting the expected charge redistribution in the allocated operation time t_op, and are of sufficiently small area, so that the charge redistribution errors caused by the device parasitic capacitances have negligible impact on the final result. For this reason, the device length is always kept at minimum value. Despite the subthreshold leakage increase in this case, the area minimization proves to be more beneficial.

The Fig. 4.22 shows the output spectra of a -2-$\mathrm{dB_{FS}}$ 13.28-kHz sinusoidal input under different process and temperature corner conditions, employing an optimized switch transmission gate with low-V_T0 devices. The NMOS device is sized $16 \times L_\mathrm{min}$ and the PMOS device is sized according to (4.23). It is demonstrated that, even in the worst case, an SDR better than 126 dB can be achieved for the target CMOS technology, without using any bootstrapping techniques, and thus, without deteriorating the circuit reliability.

The proposed optimization idea simplifies the design effort, reducing the simulation time and number of optimization variables. It can be applied for sizing of any switch in the design. For this purpose, the circuit of Fig. 4.21 should be modified to emulate the environment of the target switch.

Although regular switches allow to achieve the required full scale at all differential pairs of nodes of the ΔΣM, any techniques which help to minimize their number and thus the design effort, such as SVMA approach, are welcomed. As has been discussed in Section 3.3, the SVMAs also save up to 50 % of the static power consumption with respect to the continuous VMAs.

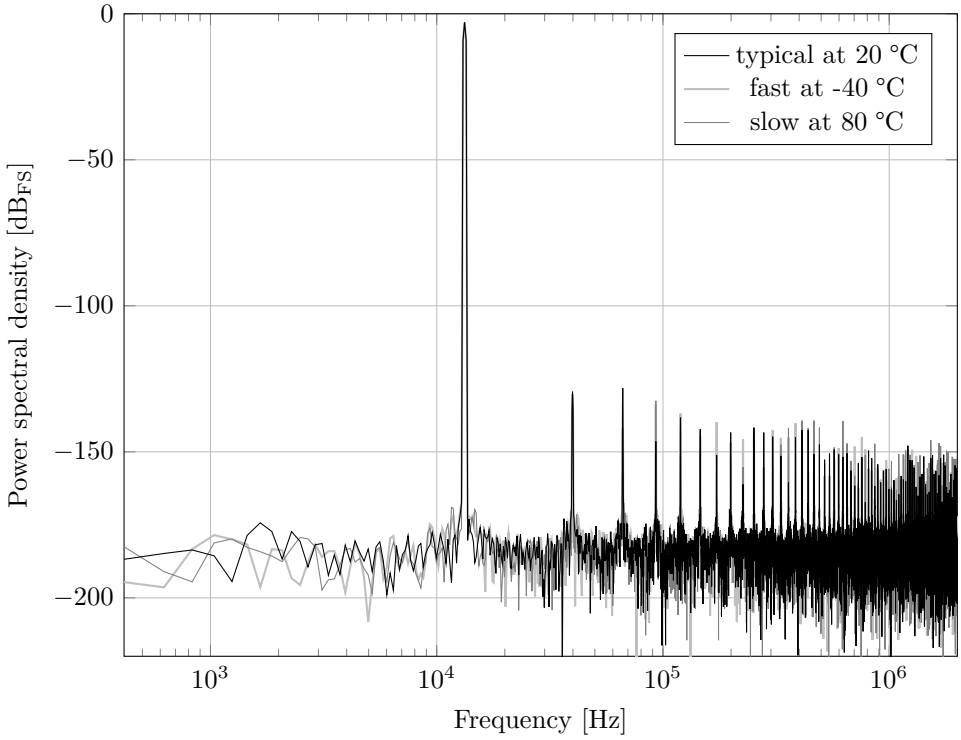

Figure 4.22 Output spectra of the feedforward-switch optimization schematic of Fig. 4.21 for a -2-dB$_{FS}$ 13.28-kHz sinusoidal input under different process and temperature corner conditions.

4.4.3 Single-Bit Quantizer

As discussed in Chapter 2, the single-bit ΔΣM architecture relaxes the design of the quantizer. It is due to the fact that the quantizer non-idealities, such as the systematic offset voltage, are largely suppressed by the single-bit ΔΣM loop [77]. Therefore, a simple circuit, illustrated in Fig. 4.23, can be employed from [92], but without the preamplifier stage.

The most stringent parameter is the quantization operation time t_q imposed by the chosen feedforward ΔΣM topology. As the quantization operation

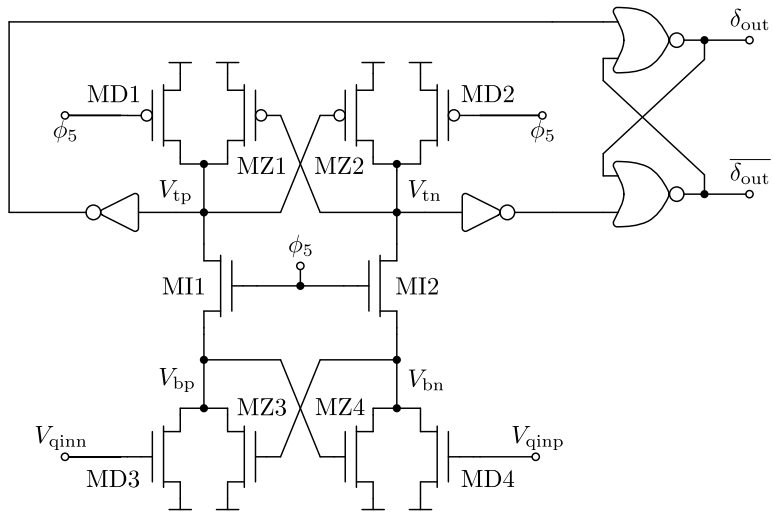

Figure 4.23 | Single-bit quantizer selected for the ΔΣM SC schematic of Fig. 4.8.

can be only triggered at the end of the feedforward summation operation ($\phi_{1,2}$), t_q must be small enough to have the result of quantization available at the beginning of the following feedback-DAC summation operation ($\phi_{3,4}$). For this reason, avoiding the use of the preamplifier also increases the speed of quantization, reducing t_q.

The circuit of Fig. 4.23 operates alternating between two different states directed by ϕ_5. When ϕ_5 is low, the transistors MD1-2, acting as switches, precharge the nodes V_{tp} and V_{tn} to the power-supply voltage, and, as the paths through the transistors MI1-2 are cut off, the nodes V_{bp} and V_{bn} are discharged to the ground level through MD3-4. The quantization operation is triggered at the ϕ_5 rising edge. The channels of MI1-2 are open, and the currents start flowing from the PMOS-device side to the NMOS-device side. Depending on the input voltages V_{qinp} and V_{qinn}, the currents flowing through MD3-4 differ. When one of the nodes V_{bp} or V_{bn} reaches the MZ3-MZ4 threshold level, a large voltage difference is obtained and further amplified. The analog outputs V_{tp} and V_{tn} are translated to the digital domain by the inverters and latched by a 2-NOR-gate SR flip-flop. The digital output δ_{out} and its complementary counterpart $\overline{\delta_{out}}$ are made avail-

able for the feedback-capacitor switching scheme and the data readout. The readout is performed by the user in synchrony with ϕ_{clko}, according to the chronogram in Fig. 4.10.

For the target ΔΣM, the quantizer circuit of Fig. 4.23 is designed achieving t_{q} of 0.5-ns in the worst case of slow PMOS/NMOS at 80 °C.

4.4.4 Full ΔΣ Modulator

Once the schematic design of all basic ΔΣM blocks is finished, the full-loop circuit is assembled, following the previously proposed schematic of Fig. 4.8.

In order to reduce the simulation time, the clock generator and the quantizer are implemented as behavioral components. Previously, their electrical circuits are simulated separately using transient times equivalent to several ϕ_{clk}, which are enough to verify their proper function. The extracted behavior is coded in XSPICE HDL and the resulting blocks are incorporated into the ngspice netlist for a mixed-mode simulation.

During the ΔΣM circuit verification, the developed framework allows any of the basic building blocks to be replaced by their behavioral counterparts. Thus, their effect on the full system can be decoupled and studied with less analytical and simulation effort [39, 40].

The mixed-mode simulation output spectra of a -2-dB_{FS} 13.28-kHz sinusoidal input under different process and temperature corner conditions is shown in Fig. 4.24. In the worst case, a signal-to-quantization-noise-plus-distortion ratio (SQNDR) of 105.7 dB and a spurious-free dynamic range (SFDR) of 106 dB are exhibited in the specified 50-kHz bandwidth.

The average simulation time t_{sim} for 64 input-sine-wave periods is 16.5 hours, using the Intel ® Core™ CPU i7-2600 @ 3.40 GHz. This time is kept within acceptable limits because of the proposed circuit-abstraction strategy. On the other hand, in the full-circuit post-layout transient-noise simulations, t_{sim} is greatly increased, as will be shown later in this chapter.

Until this point, the open software has been used to perform all research activities, which account for approximately three quarters of the effort invested in this PhD thesis. It allowed to avoid the use of professional EDA

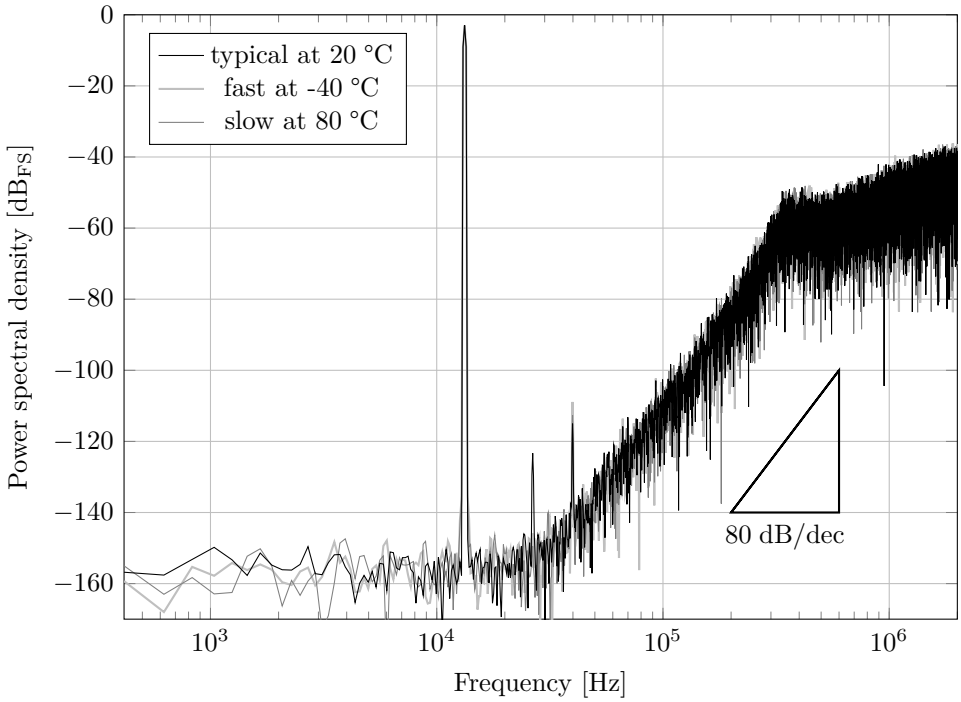

Figure 4.24 Output spectra of the mixed-mode-simulation of the full ΔΣM SC schematic of Fig. 4.8 for a -2-dB$_{FS}$ 13.28-kHz sinusoidal input under different process and temperature corner conditions.

tools, which involve expensive licenses, heavy hardware requirements and complex administrator tasks [39, 40]. Once the desired ΔΣM schematic has been obtained, it is translated to be used in the proprietary Cadence Virtuoso environment for the layout design and physical verification and the post-layout validation through transient-noise simulations. The Spectre simulator is employed instead of ngspice, the Verilog-A is used instead of XSPICE HDL, and the Skill and Ocean scripting languages substitute a part of the SAGE design-interface libraries. Nevertheless, SAGE is maintained at the top execution level for most of the design tasks, allowing to reuse much of the previously developed scripts, as has been shown in Fig. 4.1.

4.5 CMOS Physical Design

The full-custom analog layout design is carried out following mostly the traditional techniques [91, 93]. For the wide-channel MOSFETs operating in saturation, special attention is paid to minimize their gate resistance, which is the source of thermal noise increase. In order to decrease it, multiple fingers are used [84]. The gate noise can be expressed as

$$\overline{V_{\mathrm{n,g}}^2} = \frac{4k_{\mathrm{B}}T}{3m^2}\frac{W}{L}R_{\square}, \tag{4.24}$$

where m is the finger number and $R_{\square}$ is the gate sheet resistance. In low-noise applications, as a rule of thumb, $V_{\mathrm{n,g}}$ must be at least one-fifth of the input-referred channel noise $V_{\mathrm{n,ch}}$ [84]:

$$\overline{V_{\mathrm{n,ch}}^2} = \frac{8k_{\mathrm{B}}T}{3g_{\mathrm{m}}} = \sqrt{5}\cdot\overline{V_{\mathrm{n,g}}^2}. \tag{4.25}$$

Hence, using (4.24) and (4.25), for $V_{\mathrm{n,ch}}/V_{\mathrm{g,ch}} = 5$, the minimum finger number m is approximated as

$$m = 3.5\sqrt{\frac{W}{L}R_{\square}g_{\mathrm{m}}}. \tag{4.26}$$

To reduce the effects of the substrate noise, the provided CMOS-technology option of triple well for isolation of the regular NMOS devices is used. Only in the case of the switch transmission gates, as they use the low-V_{th} option, the technology does not allow the triple well to be employed for these NMOS devices.

All $\Delta\Sigma$M capacitors of Fig. 4.8 are fragmented into the same unitary elements of 230 fF. Their matching arrays are formed by five main groups:

1. Capacitors C_{s1}, C_{fb} and C_{i1}, matched to decrease the a_1- and feedback-DAC coefficient errors.

2. Capacitors C_{s2} and C_{i2}, matched to decrease the a_2-coefficient error.

3. Capacitors C_{s3} and C_{i3}, matched to decrease the a_3-coefficient error.
4. Capacitors C_{s4} and C_{i4}, matched to decrease the a_4-coefficient error.
5. Capacitors C_{ff0}, C_{ff1}, C_{ff2} , C_{ff3}, C_{ff4}, matched to decrease the adder-operation error.

In each array, preference is given to the corresponding-element matching of the positive and negative paths, thus improving the fully-differential operation. No global layout symmetry is needed because the maximum operation frequency found in the circuit does not surpass 13.6 MHz and does not arise the RF-related issues.

4.5.1 Post-Layout Simulation

As it has been explained in the previous section, starting from the layout-design activities, the Cadence Virtuoso environment is used. In addition, to the layout input, it allows to perform AC and transient-noise simulations for the purpose of the design verification.

The next section will present the integrated test vehicle. Here, the post-layout simulations of its blocks of the main interest, the first-stage integrator SVMA1 and the full ΔΣM, are presented.

The SVMA1 post layout is simulated using a unity-gain resistive-inverter configuration in continuous time, which will be reviewed in detail in Section 5.1.1 and used for the comparison with experimental results. Fig. 4.25 plots the step response for the load values ranging from 650 pF to 650 µF with the input frequencies scaled inversely and normalized. It demonstrates how the SVMA single-stage property, discussed in detail in Chapter 3, allows to have stability for a wide range of load conditions. It means that the designed SVMA, just as it is, can be reused in a variety of high-precision low-power applications, where a high DC gain and a Class-AB behavior are desired. The only requirement is to keep the operation frequency in accordance with the load conditions. The AC open-loop simulation with 200 pF load in Fig. 4.26 shows that the DC gain is maintained higher than the A_{open} value, which has been specified in Table 4.4.

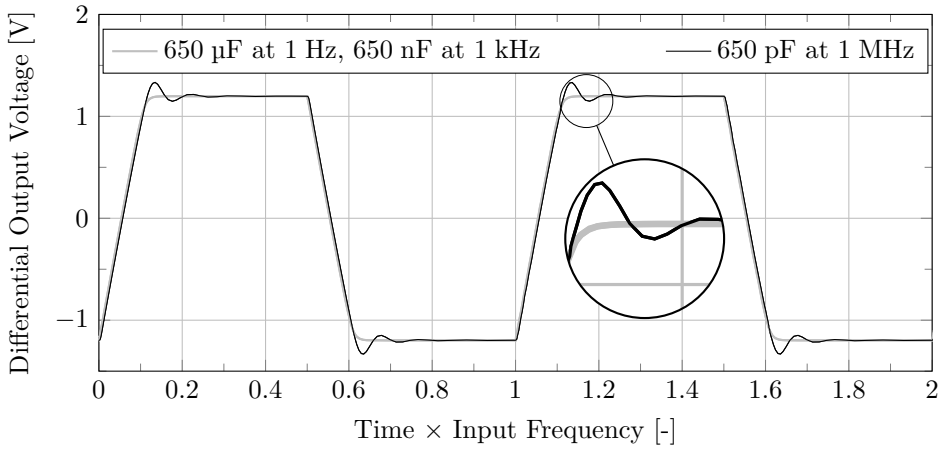

Figure 4.25 Simulated SVMA1 post-layout step response at a 2.4-V_{pp} differential input under scaled frequency and load.

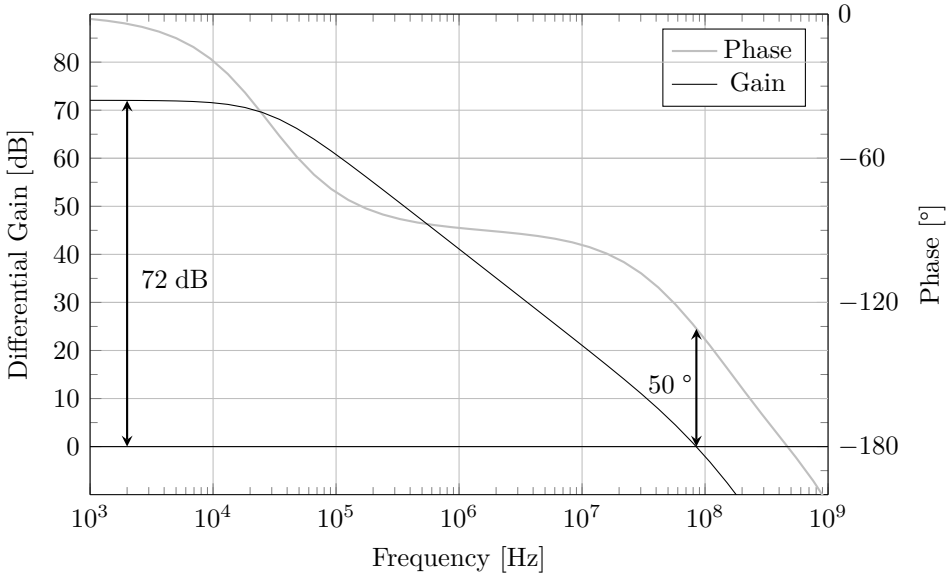

Figure 4.26 Simulated SVMA1 post-layout frequency response with a 200-pF load.

The full-ΔΣM post-layout simulation is run in two modes: first, with the transient-noise option disabled and, then, with transient-noise option enabled. The simulation output spectra of a -2-dB_{FS} 13.28-kHz sinusoidal input are plotted in Fig. 4.27. As it can be seen in the case of the simulation with the transient-noise option enabled, the noise floor in the 50-kHz bandwidth of interest is increased due to the circuit-device thermal-noise contribution, resulting in a 103-dB SNDR. This SNDR decrease has been expected and accounted for during the C_{s1} sizing in Section 4.3.

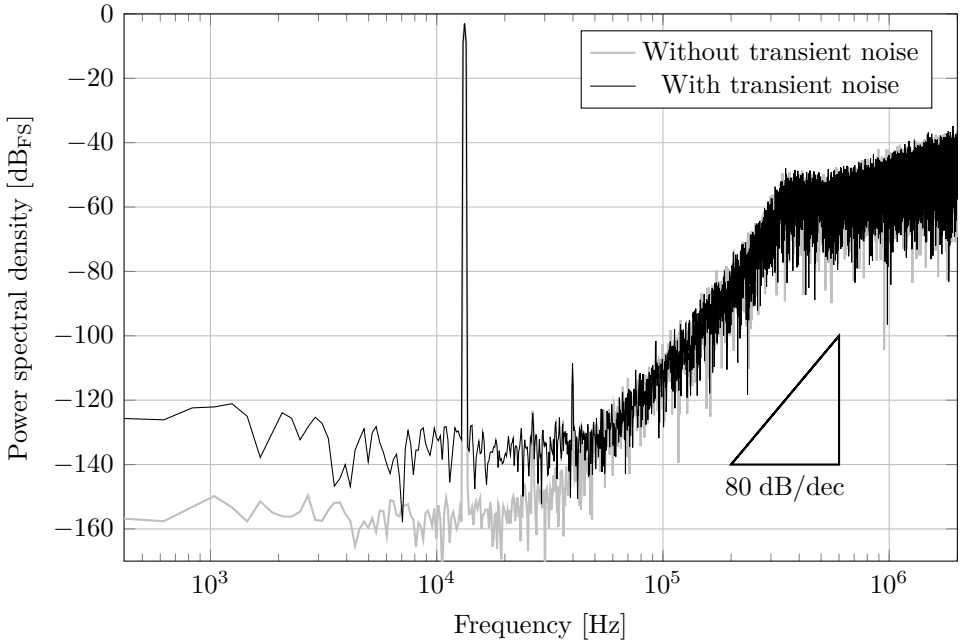

Figure 4.27 Post-layout simulation output spectra of the full ΔΣM SC schematic of Fig. 4.8 for a -2-dB_{FS} 13.28-kHz sinusoidal input.

Simulations are also run to verify whether the ΔΣM is functioning properly under the zero-input condition. Their output spectra are plotted in Fig. 4.28 for the same simulation modes, which have been introduced above. In the case of the simulation with the transient-noise option enabled, the resulting DR is 108.7 dB.

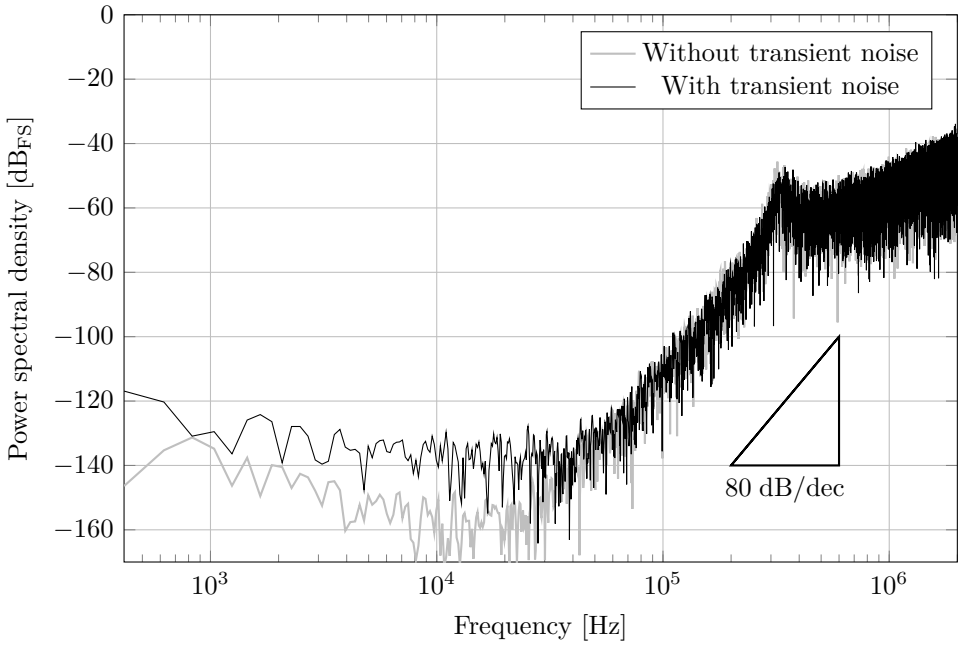

Figure 4.28 Post-layout simulation output spectra of the full ΔΣM SC schematic of Fig. 4.8 for a zero input.

The average simulation time t_{sim} for 64 input-sine-wave periods is 1480 hours, using the Intel® Xeon® CPU E5-2640 @ 2.50 GHz. The reported t_{sim} is equivalent to a two-month period, which is unacceptable by the typical industry-driven short-time-to-market schedule. Therefore, a t_{sim} reduction strategy need to be applied. The first proposed technique is to decrease the number of input-sine-wave periods, proportionally shortening t_{sim}. In order to determine the minimum number of cycles needed to evaluate the SNDR with certain precision, sequences of different lengths extracted from the same post-layout transient-noise output sequence, the spectrum of which has been presented in Fig. 4.27, are analyzed. Table 4.8 presents the SNDR results for sequences of lengths ranging from 1 to 64 input-sine-wave periods. It can be seen that, in order to obtain a 0.1-dB SNDR-evaluation precision, a 24-period simulation is the best candidate. In this case, t_{sim} is reduced by 62.5% to 555 hours (equivalent to more than 3 weeks). Even in the case

of one-period simulation, approximately lasting 23 hours, a rough idea of the ΔΣM performance can be obtained. For this reason, the simulation environment is built so that the access to the output sequence is guaranteed before the simulation run is ended.

Number of periods	1	2	4	8	16	24	32	64
Evaluated SNDR [dB]	102.3	103.8	101.4	102.6	103.7	103.1	103	103

Table 4.8 Example of the simulated SNDR results for the full ΔΣM schematic of Fig. 4.8 under sequences of different length, but the same simulation configuration.

Another t_{sim} reduction technique is to loose the Spectre-simulator absolute tolerances for voltages (vabstol) and for currents (iabstol) until the simulation results are kept similar to those for most conservative settings. Table. 4.9 lists the SNDR and t_{sim} results for different combinations of these configuration parameters. No clear pattern of t_{sim} reduction is found. Thus, the Spectre default conservative tolerances vabstol of 1 µV and iabstol of 1 pA are used throughout the verification phase.

4.6 Test Vehicle

For the purpose of experimental measurements of the circuits developed in this PhD thesis, the test vehicle of Fig. 4.29 is integrated using a standard 0.18-µm 1P6M CMOS technology. This test chip is composed of four independent circuit blocks:

1. First-stage-SVMA block, implementing the SVMA1 circuit of Fig. 4.17.
2. Transmission-gate (TG) block, implementing the switch of a maximum width found in the current ΔΣM design.
3. Full-ΔΣM block, implementing the ΔΣM circuit of Fig. 4.8 with the clock generator of Fig. 4.9.

Parameters		Results	
vabstol [µV]	**iabstol [pA]**	**SNDR [dB]**	$t_{\mathbf{sim}}$ **[h]**
100	100	100.7	469
10	100	104.3	535
100	10	101.1	467
10	10	104.5	540
1	10	102.3	620
10	1	104.8	539
1	1	103.1	555
0.1	1	104.5	523
1	0.1	102.7	436
0.1	0.1	103.9	523

Table 4.9 Results for a 24-period simulation of the full ΔΣM SC schematic of Fig. 4.8 running on the Intel® Xeon® CPU E5-2640 @ 2.50 GHz.

4. Partial-ΔΣM block, implementing the ΔΣM circuit of Fig. 4.8 without any internal clock generator and with external clock-phase inputs.

The experimental results of the first-stage-SVMA block and the full-ΔΣM block will be presented in the next chapter. The TG block and the Partial-ΔΣM are out of the scope of this thesis.

Fig. 4.30 shows microscope photography of the first-stage-SVMA block with an overall area of 0.07-mm^2. The transistor groups are indicated according to their function purpose. Some of them include more than one matching array. To allow continuous-time measurements, an extra input is provided for the external control of the CMFB voltage V_{cmfb}.

Fig. 4.31 shows the full-ΔΣM block. The capacitor matching groups, discussed in the previous section, can be clearly observed. The mentioned absence of need for a global symmetry is translated here to a compact area filling. The resulting area is 1.8 mm^2. In order to reduce the interference in the power-supply rail, the digital- and analog-supply voltages are provided separately.

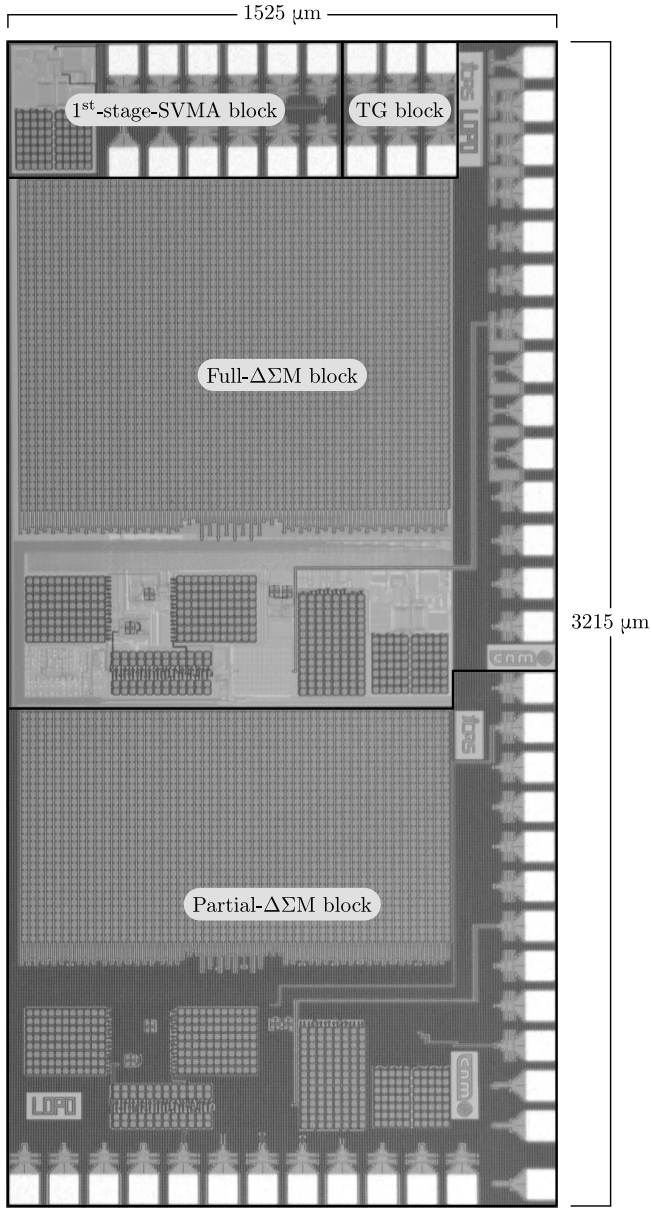

Figure 4.29 Microscope photography of the test vehicle. The overall area is 4.9 mm^2.

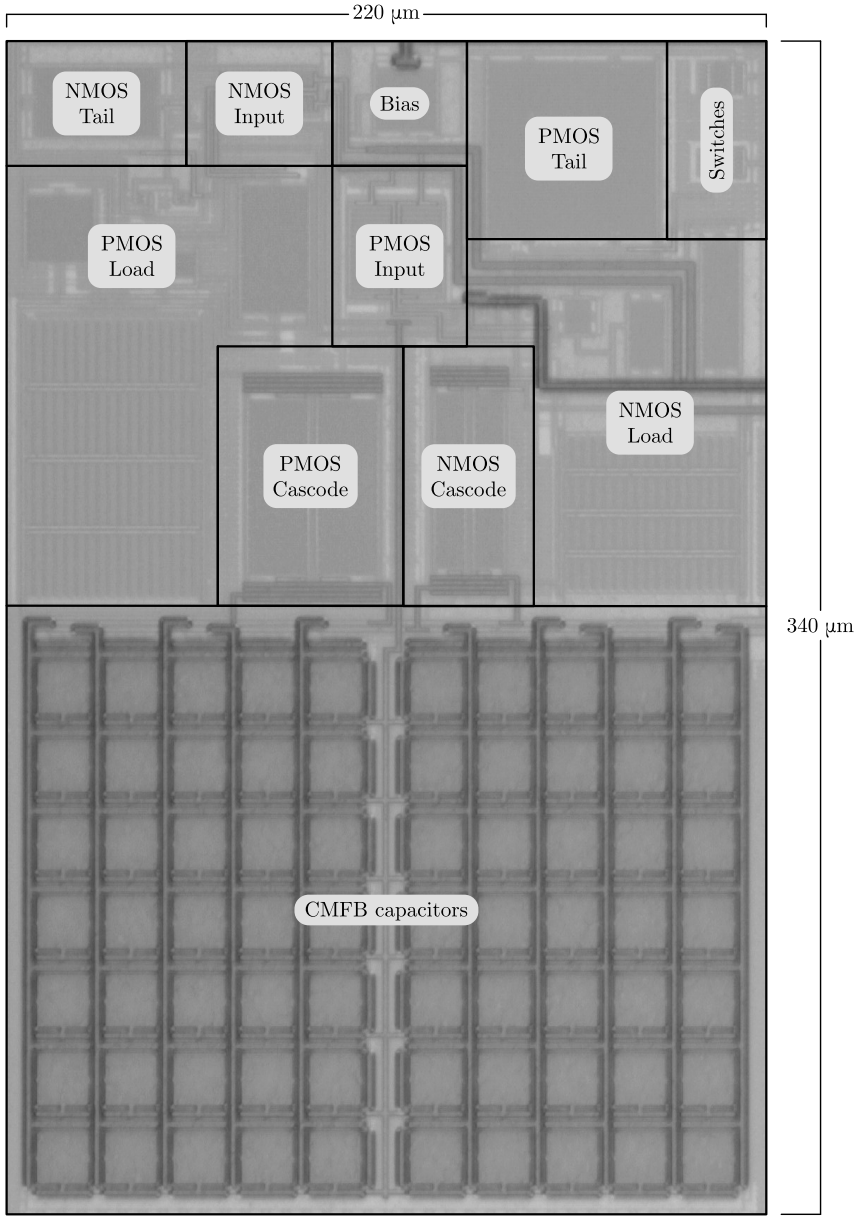

Figure 4.30 Microscope photography of the first-stage SVMA. The overall area is 0.07 mm^2.

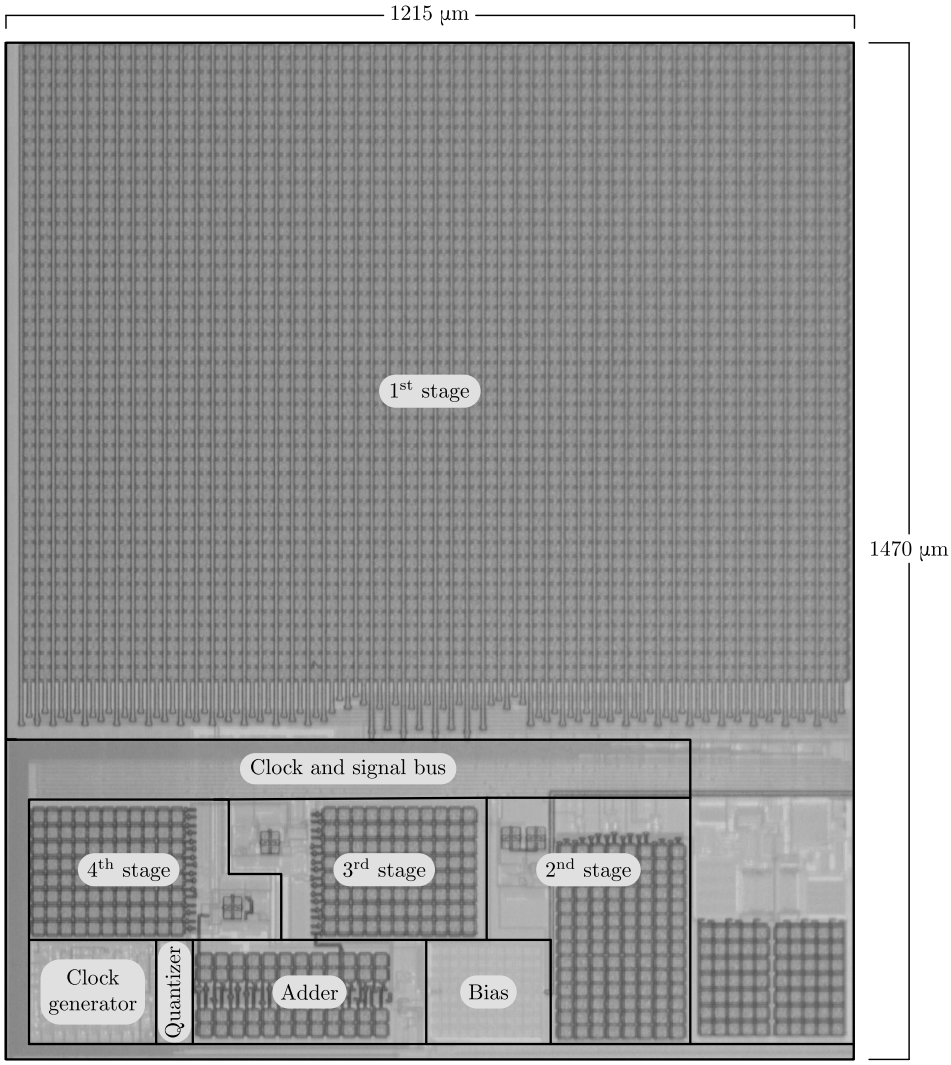

Figure 4.31 | Microscope photography of the full ΔΣM. The overall area is 1.8 mm^2.

Experimental Results | 5

This chapter presents the laboratory setup and the experimental results for the first-stage SVMA and the full ΔΣM implemented in a standard 0.18-µm 1P6M CMOS technology and described in the previous chapter. Special attention is paid to a low-noise measurement environment. The obtained performance is compared with performances in reported state-of-the-art works [3–20] using the FOM discussed in Section 1.4 and the compliance with other target features. The adopted comparison criterion will lead to the conclusion that the state of the art of high-resolution ADCs without clock bootstrapping, analog calibration or digital compensation has been improved.

5.1 A 1.25-V/µs · pF/µW-FOM Switched VMA

The most power-hungry basic circuit block of the developed ΔΣM is the first-stage SVMA (SVMA1). Previous chapters have dealt with its power consumption reduction and improvement of other important parameters. The results indicate that the proposed SVMA can be used in a number of low-power high-precision applications where the achieved performance may be required. At this point, separate test implementation and measurement are of particular interest.

The SVMA1 of Fig. 4.30 is integrated with separate pads on the same die of the test chip of Fig. 4.29 in a standard 0.18-µm 1P6M CMOS technology. The basic-architecture SVMA schematic of Fig. 3.13 is shown sized for the

SVMA1 in Fig. 4.17. An extra input pin is added to control the CMFB voltage V_{cmfb} for continuous-time measurements.

5.1.1 Measurement Setup

Fig. 5.1 shows the schematic of the resistive inverter configuration used for the measurement of the unity-gain transient response, setting the ratio between the feedback and input resistors $R_{\mathrm{fb}}/R_{\mathrm{in}} = 1$ for R_{fb}=18 kΩ.

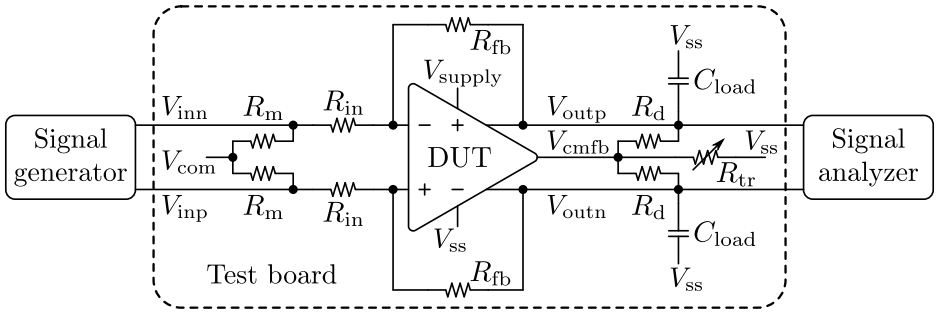

Figure 5.1 | SVMA measurement schematic.

A dual-in-line 16-pin ceramic package is employed for the test vehicle. The 50-Ω resistors R_{m} match the output impedance of the external signal generator. The SVMA is tested in continuous time. Therefore, its internal capacitive CMFB circuit, designed for a discrete-time operation, cannot be used. Instead, an external resistive network is implemented to adjust the common mode output voltage $\frac{V_{\mathrm{outp}}+V_{\mathrm{outn}}}{2}$ through the V_{cmfb} extra input provided to the SVMA DUT. The CMFB resistive network consists of two 100-kΩ averaging resistors R_{d} and the shifting potentiometer R_{tr} adjusted to about 76.8 kΩ.

5.1.2 Measurement Results

Fig 5.2 shows the step response at a 1-kHz 2.4-V_{pp} differential input and a 650-nF load. The currents of the PMOS output transistors I_{opp} and I_{opn},

from Fig. 3.13, are simulated to demonstrate the composition of the measured supply current I_{supply}. The currents of the NMOS output transistors I_{onn} and I_{onp} are not plotted for simplicity and are similar to I_{opp} and I_{opn}, respectively.

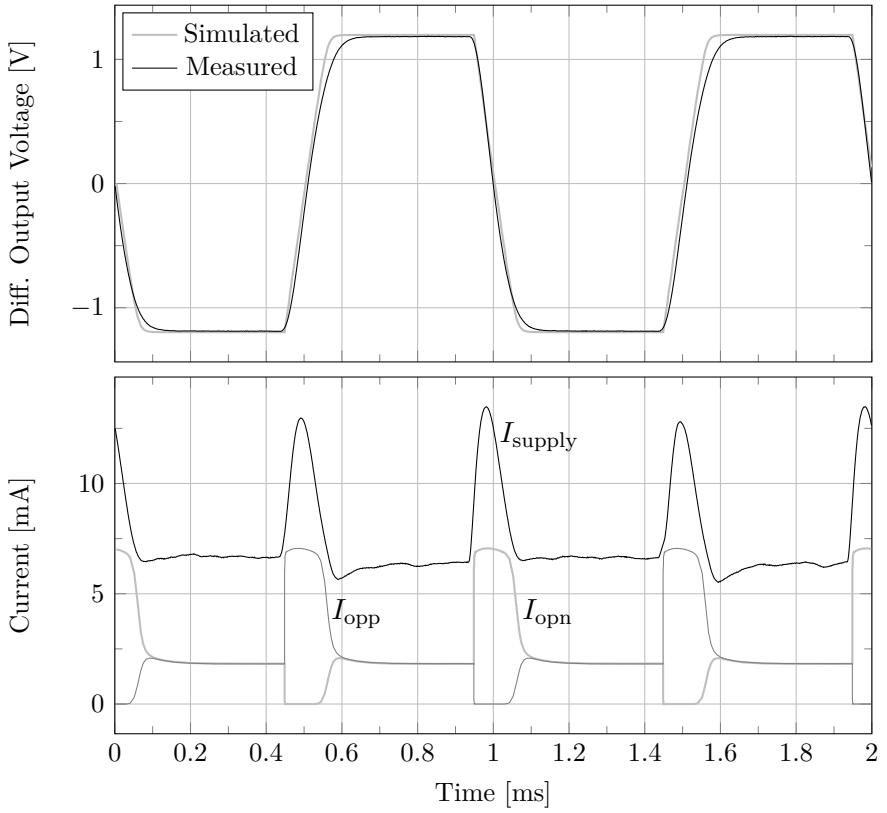

Figure 5.2 | Experimental step response of SVMA1 for a 2.4-V_{pp} differential input and a 650-nF load.

As can be seen in Fig 5.2, high Class-AB current peaks are produced at each step transition. Depending on the polarity of the transition, each peak is mostly composed of the sums $I_{\text{opp}} + I_{\text{onn}}$ or $I_{\text{opn}} + I_{\text{onp}}$ provided to the output load.

Under a zero-input excitation, operating at a 1.8-V power supply, the av-

erage I_{supply} equals 6.6 mA, resulting in a static power consumption of 11.9 mW. Considering an application in a SC $\Delta\Sigma$M, these figures will be approximately halved because of a 50-% duty cycle of the SVMA integration operation.

Fig 5.3 shows a transient response at a 3.6-V_{pp} triangular-wave differential input and the same 650-nF load. The input frequency is lowered to 10 Hz in order to evaluate the SVMA full scale more accurately. The simulated and measured results are in good agreement. They exhibit a differential full scale of 3.3 V_{pp}, which is remarkable for a cascode output using a 1.8-V power supply.

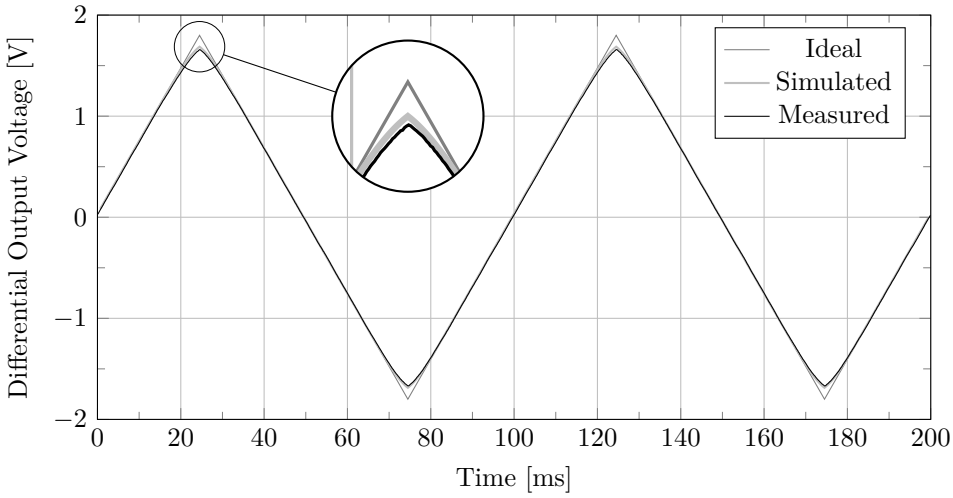

Figure 5.3 Experimental transient response of SVMA1 for a 3.6-V_{pp} triangular-wave differential input and a 650-nF load.

5.1.3 Comparison with the State of the Art

To compare the performance of the proposed SVMA with the performances of other published Class-AB amplifiers [31–35], a FOM is adopted from [35]

given by

$$\mathrm{FOM} = \frac{\mathrm{SR} \cdot C_{\mathrm{load}}}{P} \quad \left[\frac{\mathrm{V}}{\mu\mathrm{s}}\frac{\mathrm{pF}}{\mu\mathrm{W}}\right], \tag{5.1}$$

where SR is the slew rate in $\frac{\mathrm{V}}{\mu\mathrm{s}}$, C_{load} is the capacitance of the output load in pF, and P is the static power consumption in µW. The value of P is taken from the measurement results presented in the previous section, and the value of SR is taken for a 200-pF C_{load} from the post-layout simulations. Table 5.1 summarizes the extracted parameters and the resulting FOMs.

Parameter	**[31]**	**[32]**	**[33]**	**[34]**	**[35]**	**This work**	**Units**
Technology	0.5	0.5	0.25	0.13	0.18	0.18	µm
Supply	2	2	1.2	1.2	0.8	1.8	V
DC gain	43	45	69	70	51	72	dB
C_{load}	80	25	4	5.5	8	200	pF
GBW	0.725	11	165	35	0.057	86.5	MHz
Phase margin	89.5	N/A	65	45	60	50	°
Slew rate	89	20	329	19.5	0.14	74.1	V/µs
Static power	0.12	0.04	5.8	0.11	0.0012	11.9	mW
Area	0.024	0.012	N/A	0.012	0.057	0.07	mm^2
FOM	59.33	12.50	0.28	0.98	0.93	1.25	$\frac{\mathrm{V}}{\mu\mathrm{s}}\frac{\mathrm{pF}}{\mu\mathrm{W}}$

Table 5.1 | Class-AB-OpAmp comparison.

The works [31] and [32] report higher FOMs, but at the cost of the resistor device implementation, which makes them more sensitive to technology parameter variations, and at the cost of a considerable lowering of their DC gain, which may be incompatible with high-precision applications. On the other hand, the works using MOS-only devices [33–35] present lower FOMs and DC gain. Therefore, a contribution to the improvement of MOS-only Class-AB OpAmps is demonstrated. Along with its high full-scale value and DC gain, the presented SVMA circuit is suitable for high-precision applications, such as low-power high-resolution ΔΣ ADCs, which are the aim of this thesis.

5.2 A Calibration-Free 96.6-dB-SNDR 1.8-V 7.9-mW ΔΣM

The full-ΔΣM block of Fig. 4.31 is integrated with separate pads on the same die of the test chip of Fig. 4.29 in a standard 0.18-µm 1P6M CMOS technology with MIM capacitors following Table 4.2. It occupies an overall silicon area of 1.8 mm^2 without the pads. The schematic is shown in Fig. 4.8. This ΔΣ-ADC test block also includes the circuit in Fig. 4.9 used for an internal generation of the clock phases.

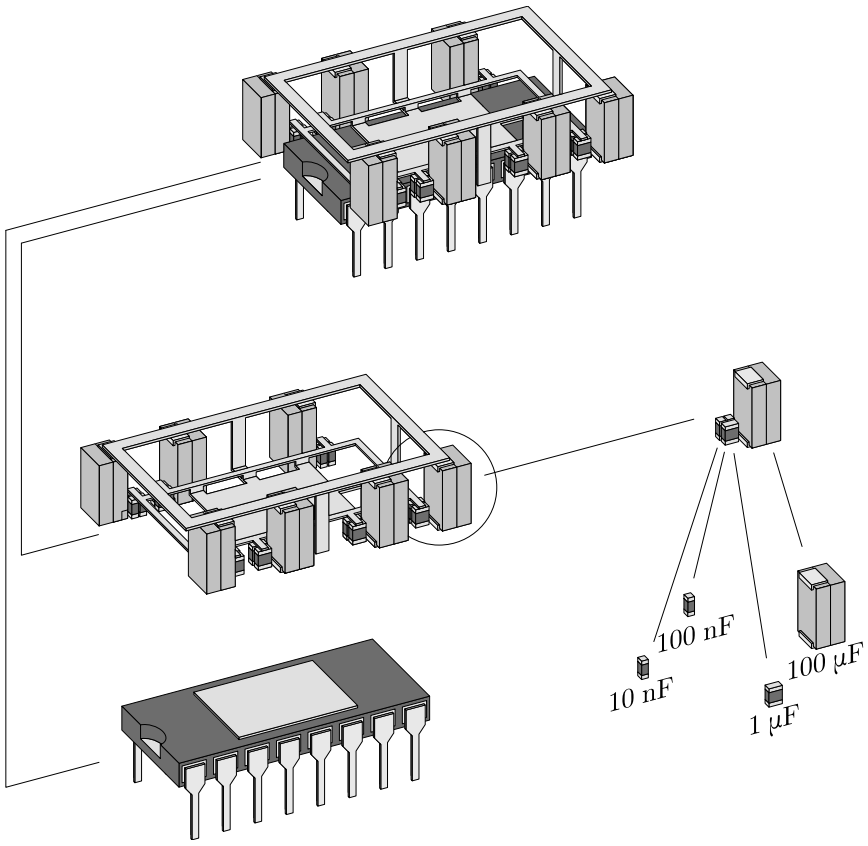

Figure 5.4 Packaging and decoupling scheme for the ΔΣ-ADC DUT.

5.2.1 Packaging and Measurement Setup

Fig. 5.4 illustrates the ΔΣ-ADC DUT employing a dual-in-line 16-pin ceramic packaging with top and bottom shielding ground layers. In addition to the integrated noise-decoupling capacitors, each power-supply and reference pin has four external capacitors of different values mounted on the same package, thus reducing the noise-decoupling-path parasitic resistance. The chosen values are of 10 nF, 100 nF, 1 µF and 100 µF. As a result,

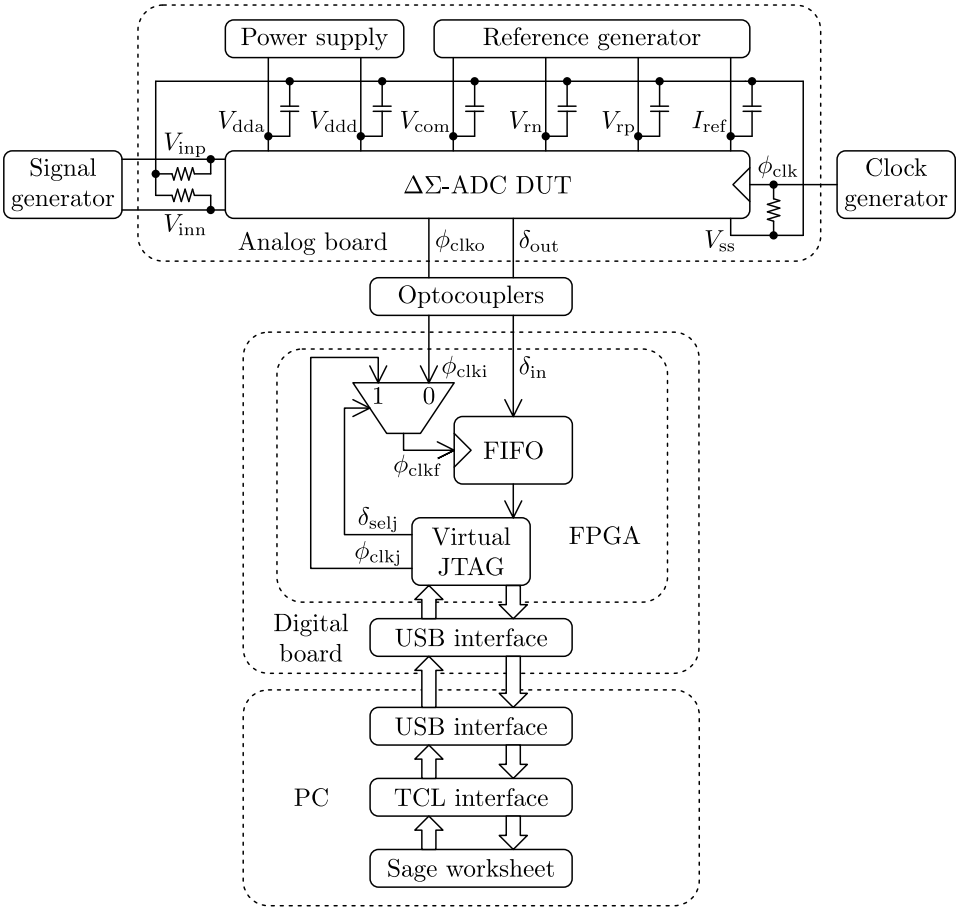

Figure 5.5 | Schematic of the ΔΣ-ADC measurement setup.

the individual frequency responses of the capacitors are combined, and the noise-decoupling band is widened.

The ΔΣ-ADC measurement setup is shown in Fig. 5.5. The Stanford Research Systems ultra-low-distortion function generator DS360 with a precision 20-bit DAC is used to generate the differential sinusoidal input signal $V_{\text{inp}} - V_{\text{inn}}$, and the Thurlby Thandar Instruments pulse generator TG5011 is used to generate the input clock signal ϕ_{clk}. The pulse-transition jitter uncertainty of the clock generator σ_{j} is of 0.5 ns, which is enough to perform testing of the oversampling ADCs of the required OSR and BW with SNDR values of up to 106 dB, according to (2.15). The analog board matches the output impedance of these external generators and provides biasing and extra shielding to the DUT. In what follows, each noise-decoupling capacitance is composed of three capacitors of 100 nF, 47 µF and 470 µF.

The analog and digital power supplies V_{dda} and V_{ddd} are generated separately by employing a low-noise circuit shown in Fig. 5.6. The input voltage V_{ref} is taken from an on-board voltage reference of 1.8 V. It is passed through the low-pass filter $(RC)_{\text{in}}$ and buffered by a voltage follower consisting of the Intersil ICL7621 low-noise OpAmp, used as an error amplifier, and the gate-controlled Siemens BSS92 p-channel MOSFET, providing an output drain current of up to 150 mA. The follower feedback loop cancels the MOSFET noise. Also, separate 6-V batteries power each device and each circuit to avoid interference in the supply rail. The dummy 10-kΩ resistor R_{out} is used to prevent the C_{out} charge accumulation because of the MOSFET leakage

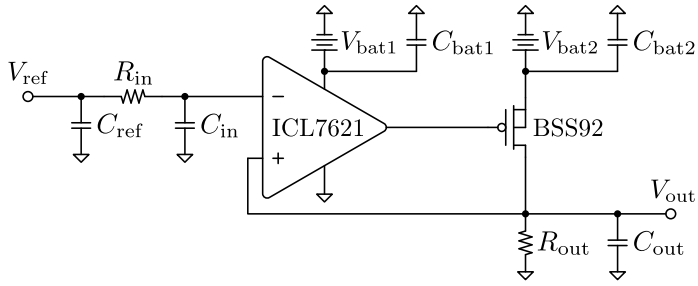

Figure 5.6 Low-noise circuit used separately for each power supply on the analog board of Fig. 5.5.

when the DUT is disconnected. As a result, V_{out}, providing the global V_{dda} and V_{ddd}, never surpasses 1.8 V, which would otherwise damage the DUT.

The common voltage references V_{com} of 0.9 V and the feedback-DAC voltage references V_{rn} of 0.36 V and V_{rp} of 1.44 V, in Fig. 5.5, are also generated separately by employing a low-noise circuit shown in Fig. 5.7. The same on-board voltage reference V_{ref} of 1.8 V is scaled adjusting the potentiometers R_{in} and R_{div}, reusing R_{in} in the low-pass filter $(RC)_{\text{in}}$, and then buffered by a simple unity-gain amplifier based on the same Intersil ICL7621 low-noise OpAmp. The resulting DC output voltage is

$$V_{\text{out}} = V_{\text{ref}} \frac{R_{\text{div}}}{R_{\text{div}} + R_{\text{in}}}. \tag{5.2}$$

A 6-V battery separately powers the OpAmp, improving immunity to interference coming from shared voltage sources.

The digital board in Fig. 5.5 is a high-speed data interface between the DUT and the Universal Serial Bus (USB) of the personal computer (PC). To prevent any electrical parasitic disturbance from affecting the measurement, the analog and digital boards are optocoupled using the Avago Technologies HCPL0930 high-speed digital isolator. Thus, the synchronizing output ϕ_{clko} and the ΔΣM data output δ_{out} are translated to ϕ_{clki} and δ_{in}, respectively, maintaining the same relative timing as indicated in Fig. 4.10. The Altera Cyclone III EP3C25 field-programmable gate array (FPGA), which allows sampling frequencies of up to 300 MHz, is used to implement three main blocks, as shown in Fig. 5.5: the clock selector multiplexer; the 65536-bit first-in, first-out (FIFO) buffer; and, the Virtual Joint Test Action Group

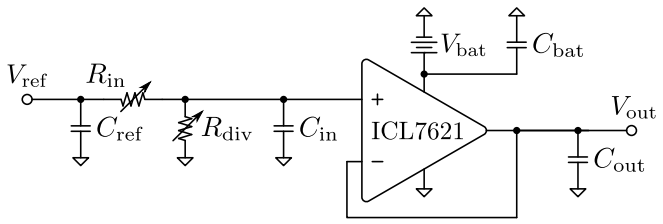

Figure 5.7 Low-noise circuit used separately for each analog voltage reference of Fig. 5.5.

(JTAG) interface block. By default, the Virtual JTAG output δ_{selj} is low. The multiplexer forwards ϕ_{clki} to the FIFO clock input ϕ_{clkf}, capturing and buffering the δ_{in} values on the rising edge, and the Virtual JTAG interface interprets the PC commands coming from the USB. At a 13.6 MHz sampling frequency, the buffer is completely updated every 4.8 ms. In contrast, the analysis of this update by the PC takes several seconds. Thus, the entity designated to govern a continuous-measurement operation is the PC. When a read-out command arrives from the PC, the Virtual JTAG raises δ_{selj}. Instead of the $\Delta\Sigma$M-paced ϕ_{clki}, the JTAG-paced clock ϕ_{clkj} is forwarded to ϕ_{clkf} and the buffered array is retrieved by the Virtual JTAG, which then delivers the data to the PC. A flowchart in Fig. 5.8 illustrates an equivalent algorithm. According to the algorithm and depending on the PC request, the buffer switches between two states, either enqueuing the data coming from the DUT on the ϕ_{clki} rising edge, or dequeuing the buffered data on the ϕ_{clkj} rising edge.

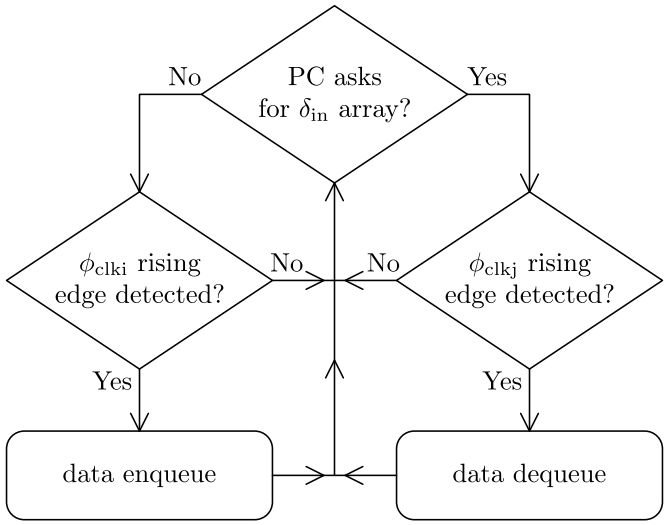

Figure 5.8 | FPGA-firmware flowchart used in Fig. 5.5.

As shown in Fig. 5.5, on the PC side, the Tool Command Language (TCL) is used to program the communication layer between the USB interface and the SAGE interpreter. The SAGE control and analysis software uses

the same libraries developed for the optimization worksheets presented in Chapter 4. Thus, the comparison between the simulated and measured results is more accurate and direct.

5.2.2 Measurement Results

The ΔΣ-ADC DUT of Fig. 5.5 is tested with the same sinusoidal input of 13.28 kHz as in the simulations presented in Chapter 4, allowing to incorporate the second and third distortion harmonics in the SNDR evaluation for a 50-kHz bandwidth. Several output spectra are obtained sweeping the input amplitude. One of them, of a -2-dB_{FS} input amplitude for a 2.4-Vpp differential full scale, is shown in Fig. 5.9. An 80 dB/decade noise-shaping slope is observed, which corresponds to a forth-order ΔΣM. The measured

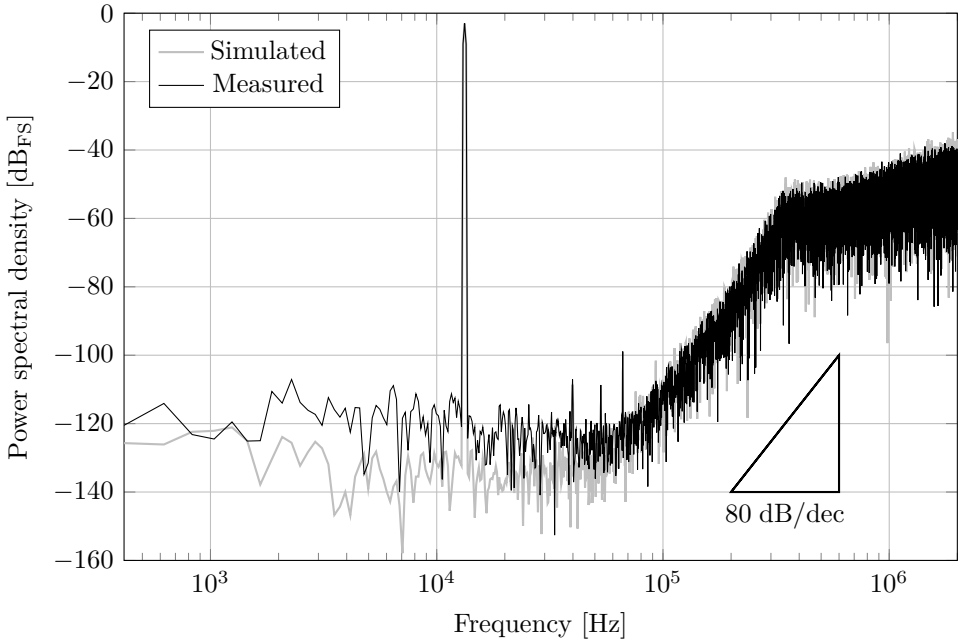

Figure 5.9 Measured and simulated output spectra of the ΔΣ-ADC DUT of Fig. 5.5 for a -2-dB_{FS} 13.28-kHz sinusoidal input.

noise floor in the band of interest is slightly higher than the simulated noise floor because of packaging and other parasitic effects unaccounted in the simulation. In addition to the SNDR, the SFDR and the SNR are also evaluated for each spectrum.

Measured results for the input-amplitude sweep in Fig. 5.10 show that the $\Delta\Sigma$ ADC achieves a 96.6-dB peak SNDR, a 105.3-dB peak SFDR and a 97-dB DR for a 50-kHz bandwidth. The plot reveals a remarkably low distortion at high amplitudes, which proves that the strong SNDR degradation caused by the feedforward path reported in [77] is avoided. Operating at 1.8 V, the measured power consumption is 7.9 mW.

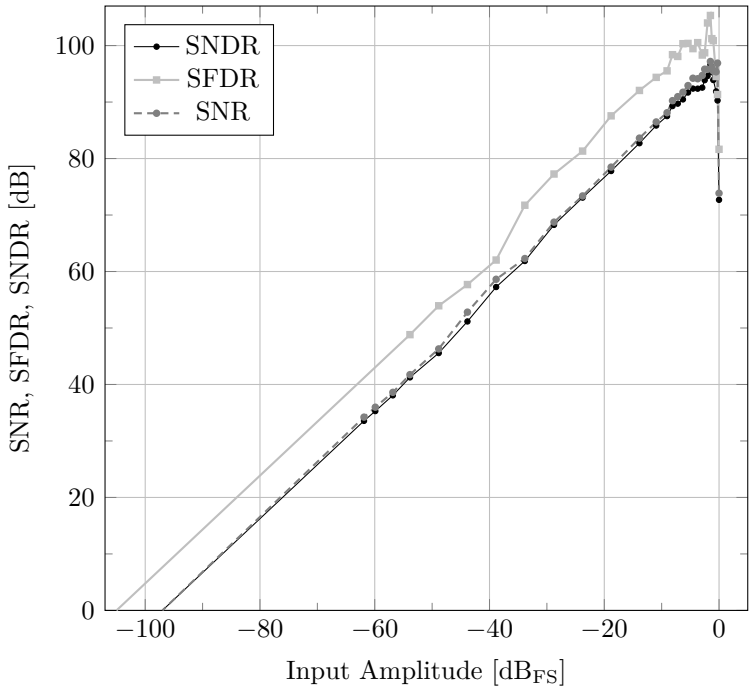

Figure 5.10 Measured SNDR, SFDR and SNR versus input amplitude of the $\Delta\Sigma$-ADC DUT of Fig. 5.5 for a 13.28-kHz-sinusoidal-input amplitude.

	[9]	[10]	[11]	[12]	[13]	[14]	[15]	[16]	[17]	[18]	[19]	[20]	[21]	**This work**	
Architecture	ΔΣ SC	ΔΣ CT+SC	ΔΣ SC	ΔΣ CT+SC	ΔΣ CT×2	ΔΣ SRC	ΔΣ SC	ΔΣ SC	ΔΣ SC	INC	ΔΣ CT	Pipe+ SAR	ΔΣ SC	ΔΣ SC	
Technology	0.35	0.35	0.25	0.18	0.18	0.13	0.18	0.18	0.35	0.16	0.18	0.18	0.18	0.18	µm
Supply voltage	5			3.3	1.8	0.9	1.8	0.7	1.5	1.8		5, 1.8	5	1.8	V
Diff. full scale			6.6	5.7	1.4	1.1				1.8		10	4.4	2.4	V_{pp}
Sampling rate	5.12	6.14	20	6.14	41.7	6.14	45.2	5	2.4	0.05	57.5	5	0.15	13.6	$\frac{MS}{s}$
Bandwidth	20	20	1000	20	200	24	500	25	20	0.0125	600	2500	0.1	50	kHz
Supply power	55	18	475	37	210	1.5	38	0.87	0.14	0.0063	21	30.5	0.505	7.9	mW
Area	5.6	0.82	20.2	0.65	6	1.44	3.5	2.16	0.21	0.38	0.99	5.74	0.8	1.8	mm^2
DR	111	106	103	102	98	92	90.1	100	92.6			100.2		97	dB
$SFDR_{max}$							97				90		100.8	105.3	dB
$SNDR_{max}$	105	97		95	90	89	86.3	95	87.9			98.6	100.6	96.6	dB
FOMW	9458	7776	2057*	20122	20311	1357	2251	378.5	173	314.8†	678.2‡	87.7	28825	1429	$\frac{fJ}{conv}$
FOMS	160.6	157.5	166.2*	152.3	149.8	161.0	157.5	169.6	169.5	182.8†	164.6‡	177.7	153.6	164.6	dB
Bootstrap-free	Yes	Yes	Yes	Yes	Yes	Yes	No	No	No	Yes	Yes	Yes	Yes	Yes	
Calibration-free	Yes	No	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	Yes	No	Yes	Yes	

Table 5.2 Comparison of the CMOS ADCs with a dynamic range exceeding 90 dB and published in 2001-2014.
* Derived from DR.
† Derived from SNR.
‡ Derived from SFDR.

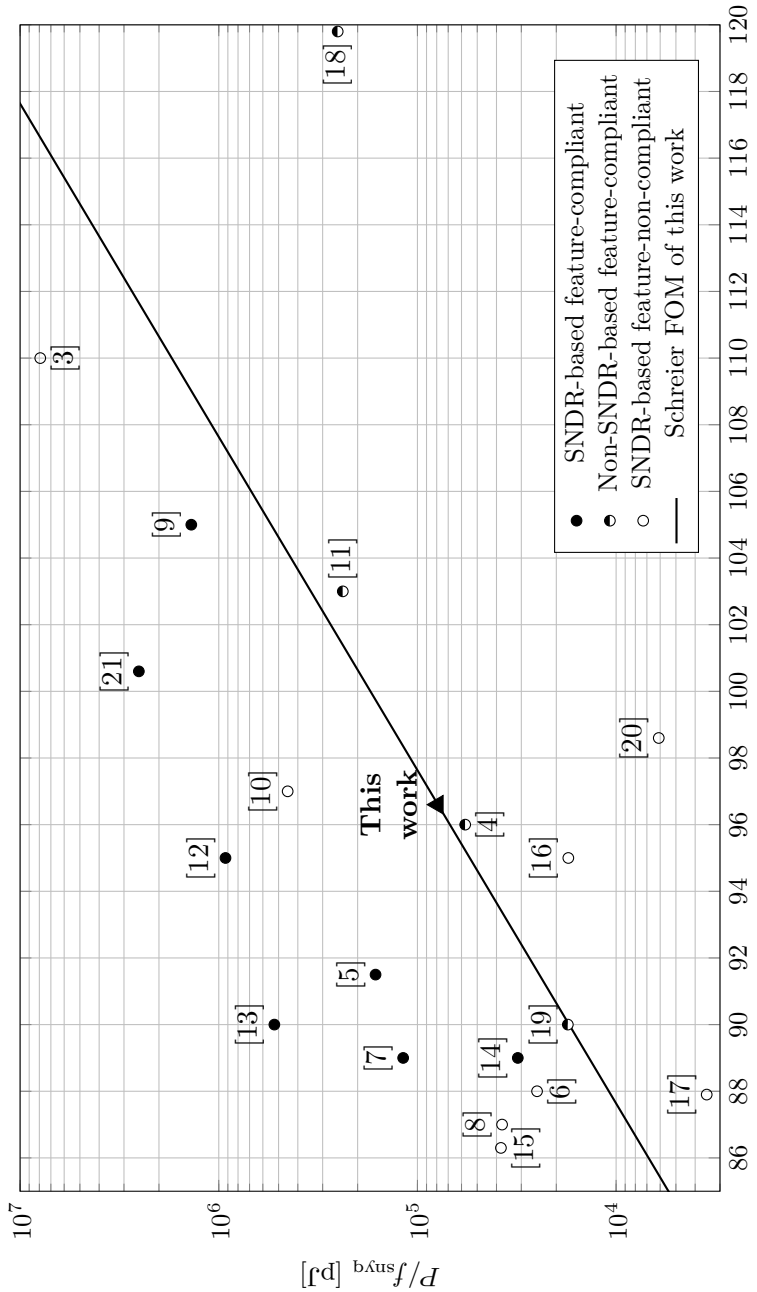

Figure 5.11 Performance comparison of the CMOS ADCs with a dynamic range exceeding 90 dB and published in 1997-2002 [3–8] and 2003-2015 [9–21].
Note: feature-compliant stands for bootstrapping- and calibration-free circuits.

5.2.3 Comparison with the State of the Art

As proposed in Section 1.4, the Schreier FOM, defined as FOMS = SNDR + $10\log(\mathrm{BW}/P)$, is preferred here for the comparison of the obtained ΔΣ ADC with other state-of-the-art high-resolution ADCs. The ADCs only exceeding a chosen 90-dB DR threshold are eligible here as high-resolution and included in the comparison [3–21]. As summarized in Table 5.2 and plotted in Fig. 5.11, the performance achieved for this ADC cannot be directly compared with the performances reported in all selected works because of SNDR unavailability [4, 11, 18, 19] or non-compliance with the bootstrapping-free or calibration-free features [3, 6, 8, 10, 15–17, 20, 21]. The measured ΔΣ ADC reaches the Schreier FOM of 164.6 dB. Regarding SNDR-based and feature-compliant works [5, 7, 9, 12–14], this FOM presents the highest value, surpassing the nearest competitor [14] by 3.6 dB. Thus, we conclude that the state of the art of high-resolution ADCs without clock bootstrapping, analog calibration or digital compensation has been improved.

Conclusions | 6

6.1 Contributions

As a result of the research activities presented in this PhD thesis, the initial working hypotheses, firstly stated in Chapter 1, have been successively tested and confirmed:

> By the use of novel analog design techniques both at the system and circuit levels, high-resolution and low-power state-of-the-art ADCs can be integrated in a low-cost standard CMOS technologies without needing any clock bootstrapping, analog calibration or digital post-compensation.

In order to achieve the above milestone in the field of analog and mixed integrate-circuit design, this PhD thesis presents the following contributions:

- A selection guide of the most suitable SC architecture for $\Delta\Sigma$ ADCs in the therms of low-power circuit implementation.
- An efficient design framework based on open-source EDA tools for the optimization of $\Delta\Sigma$ ADCs at the SC architectural level, but including the modeling of CMOS-circuit non-idealities.
- A new family of single-stage Class-AB OpAmps called variable-mirror amplifiers (VMAs), which invests dynamic peak currents at the output transistors only and does not require any internal frequency-compensation capacitor.

- Two types of Class-AB circuit sections for VMAs with very low sensitivity to both technology deviations and operational temeperatures.
- VMA circuit modifications to incorporate CMFB control and switched-OpAmp operation, as switched-VMA (SVMA), to save further power consumption.
- A mathematical analysis and algorithm for the sizing of SVMAs in SC circuits to optimize current consumption given the sampling-rate and dynamic-range specifications.
- A 1.25-$\frac{\text{V}}{\mu\text{s}}\frac{\text{pF}}{\mu\text{W}}$-FOM SVMA circuit example integrated in a standard 0.18-µm 1P6M CMOS technology and experimental results.
- A 96.6-dB-SNDR 1.8-V 7.9-mW $\Delta\Sigma$M circuit example integrated in a standard 0.18-µm 1P6M CMOS technology and experimental results.
- The best FOMS published for high-resolution (DR>90 dB) ADCs without supply bootstrapping nor analog calibration.

Apart from the publication of my PhD studies about low-power CMOS read-out ICs for smart sensors [22, 23, 42–45], the specific contributions of this PhD thesis are being disseminated through the following publications:

- S. Sutula, M. Dei, L. Terés, and F. Serra-Graells, "Class-AB Single-Stage OpAmp for Low-Power Switched-Capacitor Circuits," in *Proceedings of the IEEE International Symposium on Circuits and Systems*, pp. 2081–2084, 2015.
- S. Sutula, M. Dei, L. Terés, and F. Serra-Graells, "Variable-Mirror Amplifier: A New Family of Process-Independent Class-AB Single-Stage OpAmps for Low-Power SC Circuits," submitted to *the IEEE Transactions on Circuits and Systems I.*
- S. Sutula, M. Dei, L. Terés, and F. Serra-Graells, "A Calibration-Free 96.6-dB-SNDR Non-Bootstrapped 1.8-V 7.9-mW Delta-Sigma Modulator with Class-AB Single-Stage Switched-OpAmps," submitted to *the IEEE International Symposium on Circuits and Systems*, Montreal, 2016.

In conclusion, the improvement of the state of the art of high-resolution low-power and low-cost ADCs presented in this PhD thesis will benefit a wide range of smart-sensing applications such as high-precision industrial and scientific measurements or high-quality audio processing.

6.2 Future Work

The developed $\Delta\Sigma$-ADC integrated circuit can be used as a standalone product. Nevertheless, its integration on the same die with the sensor array is of interest to reduce the manufacturing and packaging costs and will be explored in the future.

The new version of the $\Delta\Sigma$ ADC will be supplied with low-voltage differential signaling (LVDS) circuitry for digital communication and increased decoupling capacitors. The influence of these new features on the ADC performance will be also evaluated.

Although the single-bit $\Delta\Sigma$ topology avoids the need for the ADC calibration or digital compensation, a research will be conducted into the multi-bit $\Delta\Sigma$ topology to explore whether other useful parameter trade-offs can be achieved.

Concerning the developed low-current design proposals, they can be also reused in the low-voltage circuit design realm. The idea would be to provide more compatibility with low-voltage energy sources such as button cells and other non-standard alternatives like energy harvesters.

Finally, the usage of open-source software derived from the presented framework will be broaden to the layout design stages with contributions to the scientific community.

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