Chapter 5

Electrical characterization of a cryogenic module

5.1 Electrical module description

A first electrical prototype module was assembled (Figure 5.1) using a large size silicon microstrip sensor. The 50 μm pitch silicon microstrip sensors have an active area of 32.5 cm^2 and they were processed both on Czochralski and Float Zone silicon [43][44]. The first module with real components was assembled using one of the Fz sensors (Section 5.2).

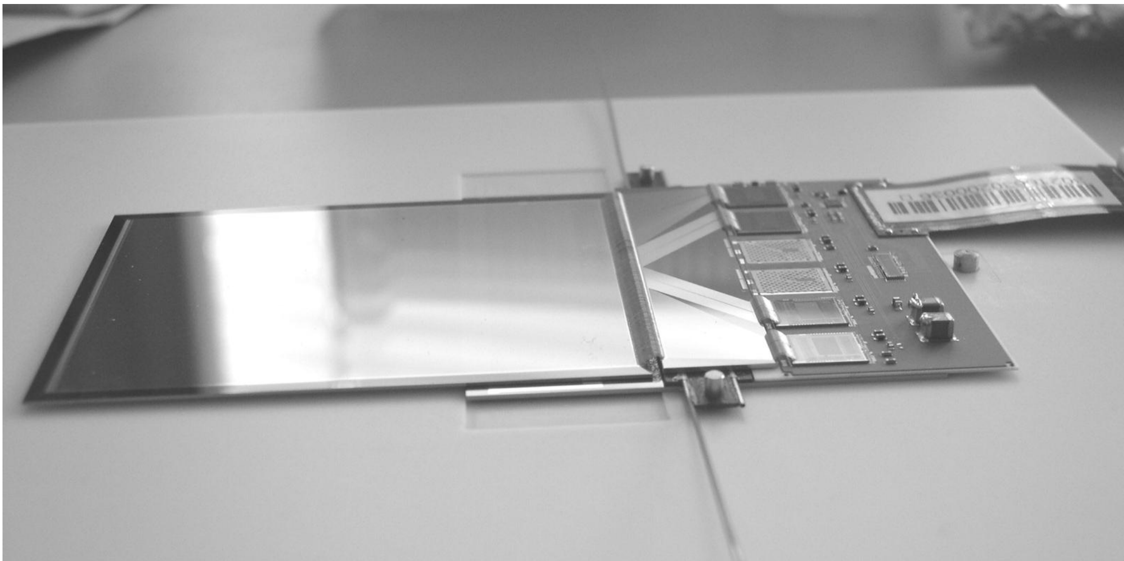

Figure 5.1 Full electrical module prototype.

The module components were adapted to the larger sensor size. The CFC spacer, the support plate and pitch adapter were made larger than in the original design (Section 5.3). The photo-mask design for the pitch adapter and support plate was done at CERN and processed on silicon at the Microelectronics Center of Helsinki University of Technology.

The readout electronics remained the same as in the first prototype: ceramic CMS hybrid with APV25 chips. The APV25 chip had been characterized at low temperature by COMPASS [45]. However, no characterization of the CMS hybrid down to 130 K had been done. A special setup was designed and built at the Central Cryogenic Laboratory of CERN to perform this characterization, which was done in

collaboration with the Université Catholique de Louvain and the Helsinki Institute of Physics (Section 5.4). High voltage filters were designed and processed on a ceramic support to bias the sensor.

Table 5.1 Large module component dimensions and materials.

Element	Dimensions (mm^3)	Material
Sensor	55.9 x 65.7 x 0.38 mm^3	Czochralski silicon
	55.9 x 65.7 x 0.5 mm^3	Float Zone silicon
Support Plate	60 x 50 x 0.3 mm^3	Silicon
Pitch Adapter	60 x 12 x 0.3 mm^3	Silicon
Hybrid	60 x 28 x 0.3 mm^3	Alumina
Pipe	0.6 mm OD / 0.5 mm ID	CuNi
Spacer	60 x 9 x 0.55 mm^3	Carbon Fiber Composite
Glue Layers	100 µm thickness	Araldite® 2011

Because of these geometry changes, a new assembly tooling was also designed and produced. The tooling consisted in this case of four jigs and the gluing had to be done in three steps (Chapter 2).

The thickness of the proposed module with a sensor of 32.5 cm^2 is 1.107 % of the radiation length. The contributions of the components has been calculated as if their material was smeared uniformly over the area of the silicon active area. In order to be able to compare to the silicon microstrip modules used in the trackers of the LHC experiments, the thickness of a similar module with a larger sensor was also calculated, as show in Table 5.2. The thickness of such a module is 0.753 %.

Table 5.2 Contributions of the components to the total thickness of the cryogenic module holding a sensor of 32.5 cm^2 and a ficticious sensor of 65 cm^2.

Component	**Material density** ρ **(g/cm^3)**	**Total mass** (g)	**Radiation length** (cm)	**Thickness % of rad length**
Silicon sensor (32.5 cm^2)	2.33	0.599	9.36	0.406
Silicon sensor (65 cm^2)	2.33	1.198	9.36	0.406
Silicon support plate	2.33	0.386	9.36	0.131
Pitch adapter	2.33	0.093	9.36	0.031
Readout electronics	3.97	0.127	4.85	0.141
Cooling pipe	8.94	0.046	1.43	0.017
Spacer	2.1	0.141	25	0.016
Glue layers	1.05	0.232	34.4	0.009
TOTAL, sensor 32.5 cm^2		**1.625**		**1.107**
TOTAL, sensor 65 cm^2		**2.224**		**0.753**

The thickness of the ATLAS baseline double-sided module with similar active area is 2.704 % of the radiation length [46]. To compare this number to ours, we must substract the contributions of the support elements and cables, also included in the quoted number. Finally it must be divided by two, in

order to compare with our single-sided module. The result is 1.1094 % of the radiation length, about 45 % thicker than our module.

5.2 Silicon sensor

The silicon microstrip sensors were designed and processed at the Microelectronics Center of Helsinki University of Technology [43]. The starting material was Okmetic Czochralski silicon (Cz-Si) and the wafers were 380 µm thick with a crystal orientation <1 0 0>. The nominal resistivity was 900 Ω cm. Float Zone (Fz-Si) sensors were processed using Topsil material. The wafers were 500 µm thick and had a resistivity of 2 kΩ cm to 3 kΩ cm.

Sensor processing

The sensor fabrication process contained four mask levels and consisted of two thermal oxidations, two ion implantation and three sputter depositions. The first processing step was the growth of a 250 nm layer of silicon dioxide (SiO_2). This oxide layer acts as a mask for the ion implantation of the p-type strips. The oxidation was done in dry oxygen atmosphere at a temperature of 1050 °C for about 8 h. Next, the openings for the front side p+ strips were patterned to the oxide by photolithography using the first level photo-mask. The strips were implanted by 30 keV boron ions. The width of the strip is 10 µm and the length 6.159 cm, the pitch being 50 µm. There are 1024 strips in the sensor. Since sharp edges may potentially cause high electric fields during the reverse bias operation of the sensor, the ends of each strip were rounded.

The sensor back surface (n^+) area was implanted by 70 keV phosphorus ions. The implantation doses for both boron and phosphorous ions were 10^{15} cm^{-2}. After the implantations the remaining front-side SiO_2 mask was removed by buffered hydrogen fluoride (HF) solution. Before the following oxidation the wafers were RCA cleaned.

Dielectric SiO_2 film for isolating the AC-coupled signal strips was grown by dry thermal oxidation at a temperature of 1050 °C. In these conditions 200 nm thick oxide layer grows in 5 h. Simultaneously the implanted boron and phosphorous diffuse from the contact layers.

The second photo-mask was used in order to pattern the sputtering mask to produce the resistors needed for biasing the strips (Figure 5.2), which are made by sputtering tungsten nitride. The third photo-mask level was used to provide an etching mask for opening contact holes through the SiO_2 layer. The fourth photo-mask level was used to pattern the aluminium metallisation. A 2 µm overhang of Al metallisation on the strip implants was designed. It influences the electric field near the strips thus decreasing the possibility of breakthrough at high bias potential. This in turn results in higher breakdown potential of the silicon sensor.

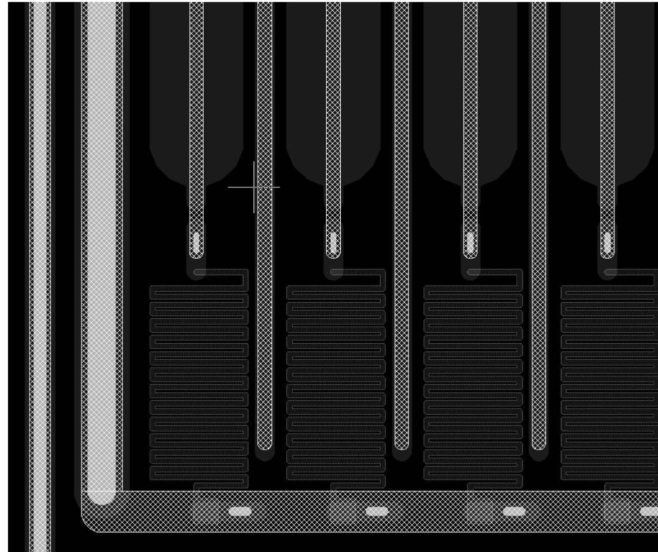

Figure 5.2 Detail of the resistors needed for biasing the strips.

After patterning the front side metallisation, the Al contact is sputter deposited on the rear side of the sensor wafers. The final process step is the sintering of the metal contacts, which was carried out at 350 °C for 15 min in N_2 atmosphere.

Characterization of the sensors

Sensor current-potential (I-V) characteristics up to 900 V were measured (Figure 5.3). The leakage current of the 32.5 cm^2 Cz-Si sensor is 3 µA at 900 V. For Fz-Si sensors the leakage current is about 1.2 µA at 1000 V. Cz-Si and Fz-Si sensor breakdown did not take place below 900 and 1000 V, respectively.

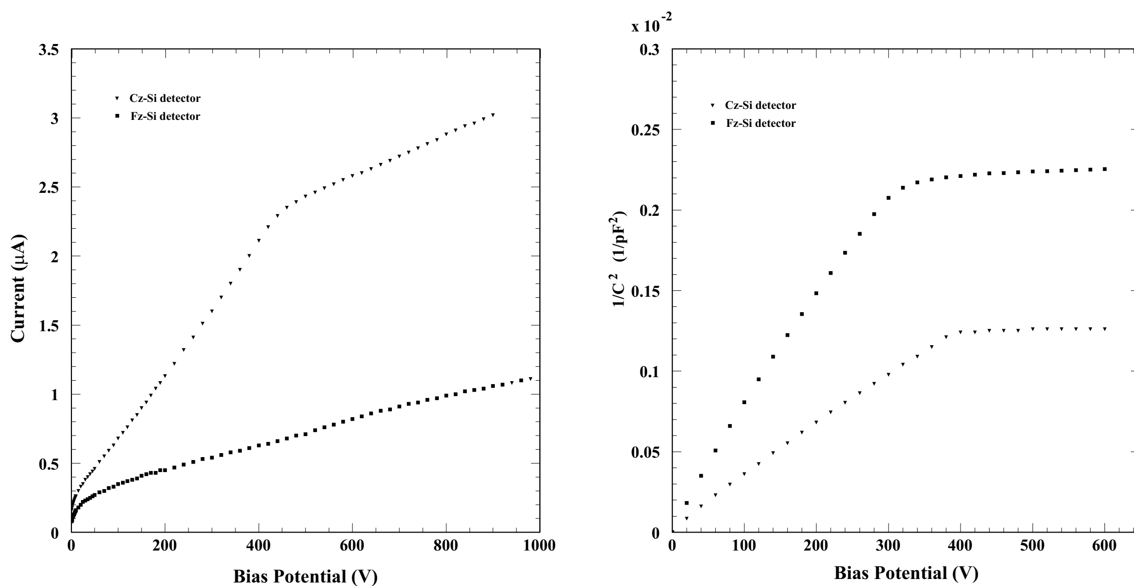

Figure 5.3 I-V and C-V characteristic curves of Cz-Si and Fz-Si sensors at room temperature [43][44].

The depletion potential of the devices was extracted from the capacitance-potential (C-V) measurement (Figure 5.3). The capacitance is defined as the incremental change in the depletion layer charge for an incremental change in the applied potential and is defined by:

$$C(V) = \varepsilon\varepsilon_0 \frac{A}{W(V)} = A\sqrt{\frac{\varepsilon\varepsilon_0 q_0 |N_{\mathrm{eff}}|}{2(V+V_{\mathrm{bi}})}} \qquad \text{for } W \le d \ , \tag{5.1}$$

where A is the area of the diode, W is the depletion depth, ε_0 the dielectric constant of vacuum (8.85 10^{-14} F/cm), ε is the dielectric constant of silicon (1.19), q_0 is the elementary charge (1.60 10^{-19} C), N_{eff} is the effective doping concentration, V is the bias potential, V_{bi} is the built-in potential and d is the thickness of the substrate.

Therefore, the capacitance decreases with the applied bias potential $C \propto \frac{1}{\sqrt{V}}$ and reaches with full depletion a final value of:

$$C = \frac{\varepsilon\varepsilon_0 A}{d} \ . \tag{5.2}$$

This capacitance is called the geometrical capacitance since it only depends on the geometrical size of the diode. The plateau of the curves shown in Figure 5.3 starts at about 420 V for the 380 µm thick substrate. For the Fz-Si device the depletion occurs at about 320-340 V for the 500 µm thick substrate. The doping concentration and resistivity can be calculated from the expression of the full-depletion potential:

$$V_{\mathrm{fd}} = \frac{q_0 |N_{\mathrm{eff}}| d^2}{2\varepsilon\varepsilon_0} \quad . \tag{5.3}$$

where the built-in potential has been neglected.

For a 380 µm thick Cz-Si substrate the full-depletion potential of about 420 V would result into a resistivity of about 1150 Ω cm, which is slightly higher than the 900 Ω cm measured before the device processing. If the wafers were thinned down to 300 µm, which is frequently the sensor thickness in particle physics applications, the resistivity of 1150 Ω cm would result in the sensor being fully depleted at about 265 V (Equation 5.3).

5.3 Pitch adapter and support plate

The pitch adapter is an intermediate piece that matches the silicon microstrip sensor pitch to that of the APV25 readout chip. In our design, the pitch adapter lies on top of a carbon fiber composite (CFC) spacer which holds the capillary cooling pipe. The support plate is just a base plate where the sensor and the readout electronics are sitting and is also used to bring the high voltage to bias the sensor from its back side. For thermo-mechanical reasons (see Chapter 2), both the pitch adapter and support plate were made out of silicon.

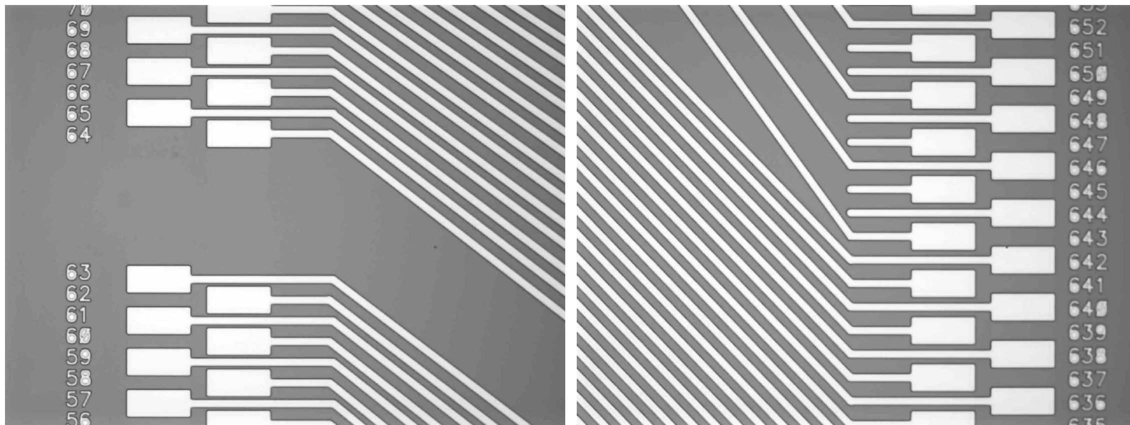

Figure 5.4 Pitch adapter magnification of the 44 μm pitch pads on the APV25 side (left) and the 50 μm pitch pads on the sensor side (right).

Before the module assembly, bonding tests were carried out with dummy pieces in order to understand if there were problems arising from the particular geometry of the pitch adapter and to determine the sintering needed for a good adhesion of the bonding wires at the bonding pads.

A first test was performed with unsintered pieces while another one was carried out with pieces sintered 15 min at 400 °C. It was observed that the bonding on the unsintered pieces was not possible since the bonded wires did not stick well on the pads. The bonding on the sintered pieces was possible but weak. After these bonding tests, the sintering time for the final components was increased from 15 min to 40 min and the temperature from 400 °C to 450 °C. In that case, the thickness of the SiO_2 insulator is about 1000 nm and the metal thickness about 400 nm.

The processing of the support plate and the pitch adapter involved one photo-mask level and both components were produced in the same silicon wafer. The metalization was done with aluminium. Details of the pitch adapter are shown in Figure 5.4 and of the bonding in Figure 5.5.

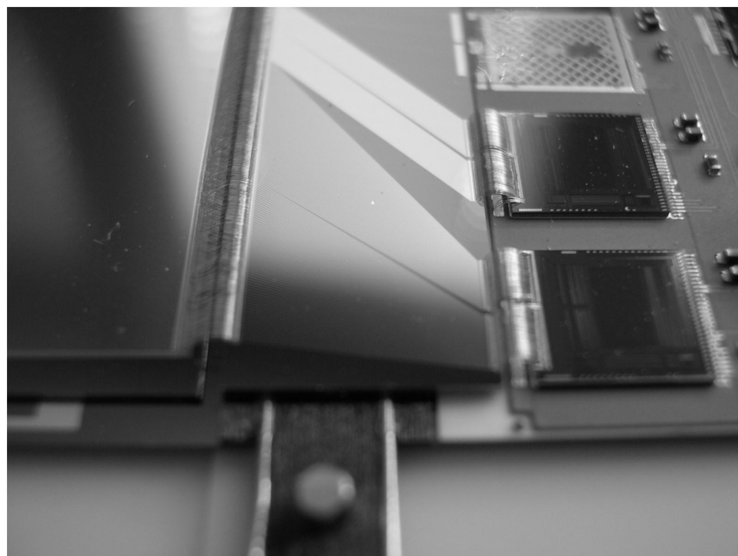

Figure 5.5 Detail of the bonding between the sensor, the pitch adapter and APV25, from left to right.

5.4 Readout Electronics

The CMS readout electronics with APV25[1] chips is used for the cryogenic module. The APV25 is an analogue pipeline Application Specific Integrated Circuit (ASIC) intended for readout of silicon microstrip sensors in the CMS tracker. The chip contains 128 channels of preamplifier and shaper driving 192 columns of analogue storage into which samples are written at the 40 MHz frequency of LHC bunch crossings. Therefore, the memory always contains a record of the hits resulting from the most recent beam crossing. A data access mechanism allows the marking and queuing of requested memory locations for output. Requested samples from the memory can then be processed with a finite impulse response (FIR) filter. This is a switched capacitor network which deconvolves the shaping function of the preamplifier and shaper stages to give a pulse shape confined to one 25 ns period. Afterwards, the filter data is held in a further buffer until it can be read out through a multiplexer. Silicon strip signals are amplified into 50 ns shaped pulses of magnitude 100 mV for 25000 electrons charge signals.

The chip has three modes of operation and two rates of read-out. The *deconvolution* mode is used in normal operation when data rates are sufficiently high, such that the effects of pile-up are significant. The *peak* mode is used when the pile-up is not significant and a larger signal to noise ratio is required. The third mode of operation is the *multi* mode, which is used for pulse-shape calibration.

For our cryogenic silicon microstrip sensor module, the performance of the readout at low temperature needed to be characterized. While the APV25 chip had been shown to operate down to 110 K by COMPASS [45], the full CMS hybrid had never been studied at such low temperatures. Preliminary results are presented here down to 210 K. Further tests are foreseen down to 100 K temperature.

Experimental setup

The hybrid was cooled down in a cryostat vessel with an open bath of liquid nitrogen. The hybrid was sitting on top of a copper vacuum chuck. This copper plate was attached to the cryostat vessel cover, where the vacuum lines and instrumentation feedthroughs were located (see Figure 5.6).

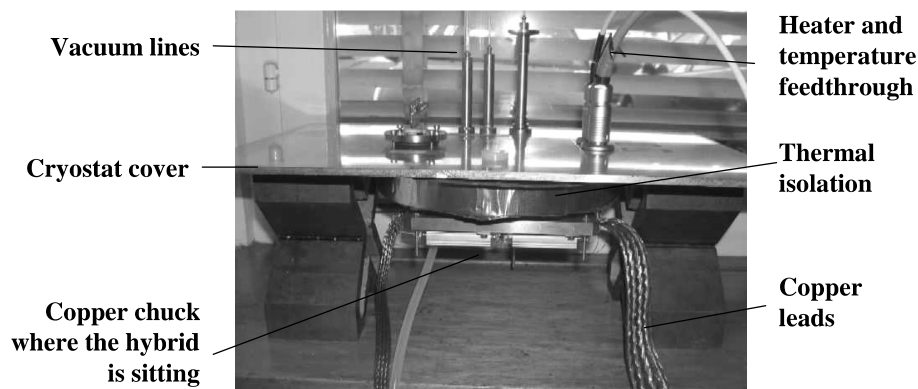

Figure 5.6 Detail of the cryostat cover used in the low temperature hybrid tests.

1 APV25 User Guide, v.2.2, 2001 (http://www.te.rl.ac.uk/med).

On the bottom of the vacuum chuck, PT100 thermometers and heaters were fixed in order to control the hybrid temperature using a commercial temperature controller. Two long copper leads extend to the liquid N_2 in order to be able to reach 130 K at the hybrid, which remains in nitrogen atmosphere. The dry boil-off gas prevents the humidity from reaching the hybrid, avoiding condensation or frosting on the component surfaces.

Figure 5.7 Experimental setup for low temperature readout electronics tests.

The CMS hybrid was read using CMS DAQ software written for the qualification of the hybrids. The hardware consisted of a PC housing a series of electronic cards (FED, FEC). The full setup can be seen in Figure 5.7.

Readout electronics performance at low temperature

When the temperature (T) decreases, the mobility of the electrons in silicon (μ) increases following the expression [47]:

$$\mu(T) = \mu(T_{\mathrm{nom}})\left(\frac{T}{T_{\mathrm{nom}}}\right)^{X} , \tag{5.4}$$

where T_{nom} is a reference temperature and X is a factor which takes into account lattice and impurity scattering in silicon. Typical values of X are found around $X = -1.5$, though this value is process-dependent and needs to be derived for each impurity concentration [48][49].

The transconductance (g) of the CMOS transistors is proportional to the mobility. The noise (S) is related to the temperature (T) and the transconductance by

$$S \propto \sqrt{\frac{T}{g}} . \tag{5.5}$$

Therefore the variation of the noise due to a temperature change from T_{nom} to T can be calculated as:

$$S(T) = S(T_{nom})\sqrt{T^{1-X}T_{nom}^{X-1}} \quad , \tag{5.6}$$

and a decrease in noise is expected when the junction is cooled down.

Pedestal, noise and pulse shape at low temperature

A series of measurements at low temperature were carried out on Kapton® and ceramic hybrids. The results presented here are for one Kapton® hybrid, and concentrate on the pedestal, noise and pulse shape.

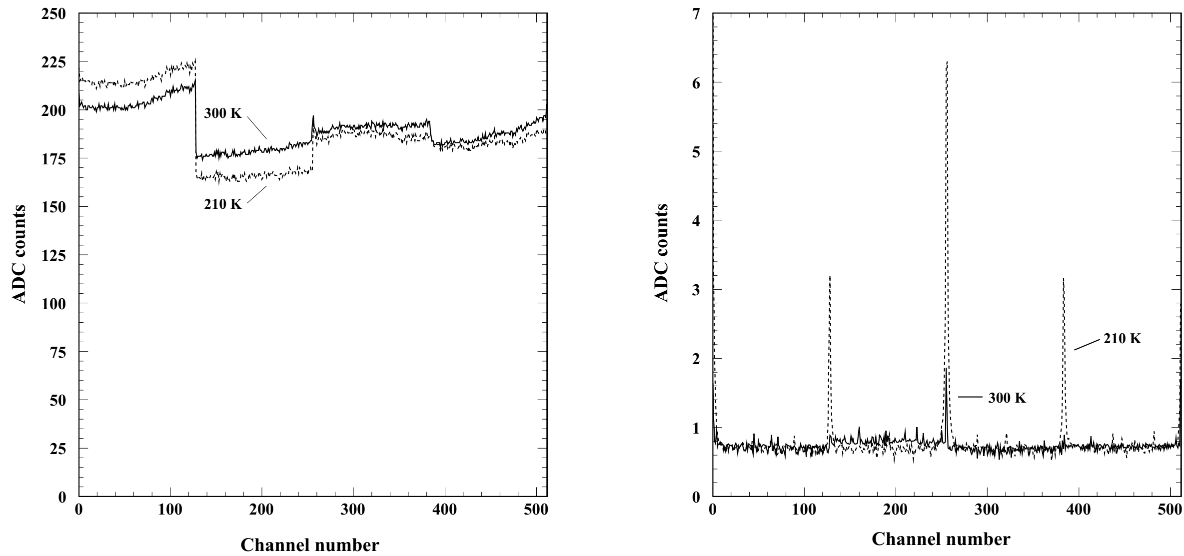

Figure 5.8 APV25 pedestal (left) and common mode subtracted noise (right) at 300 and 210 K.

Figure 5.8 shows the pedestal and the common mode subtracted noise at 300 K and 210 K in the peak mode for the 4 APVs. The pedestal increases for the first chip, while it decreases for the other three, as expected. Regarding the noise, it does not show significant variations with temperature. The channels at the borders of the APV show more noise at lower temperature.

In Figure 5.9 the pulse shape in deconvolution and peak mode at 300, 273, 245 and 210 K for one channel are plotted. It can be observed how the rise time[1] decreases and the gain increases with decreasing temperature. A decrease of several nanoseconds in the rise time is observed for a ΔT of 90 K, while the pulse shape peak height is increased by 34 % for the same temperature difference. The rise time at different temperatures and for the two operation modes are summarized in Table 5.3.

1 The rise time is defined here as the time required for the signal to change from 10 % to 90 % of its height.

Table 5.3 Rise time as a function of temperature in peak and deconvolution mode with inverter off.

Temperature	Peak mode, inverter off	Deconvolution mode, inverter off
300 K	21 ns	16 ns
273 K	19 ns	15 ns
210 K	16 ns	14 ns

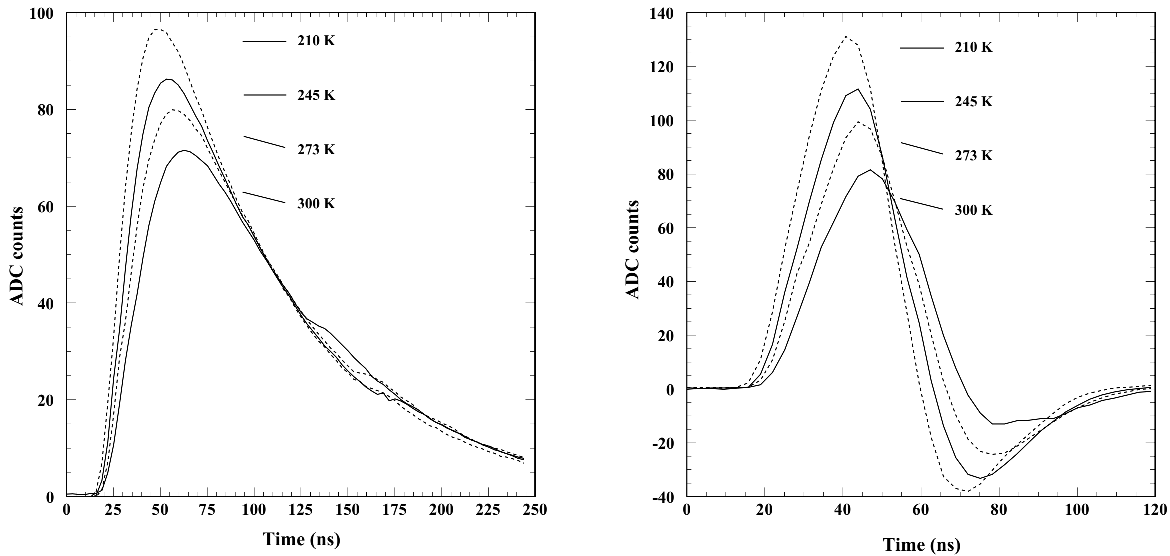

Figure 5.9 APV25 pulse shape in peak mode with inverter off (left) and deconvolution mode with inverter off (right) at 300, 273, 245 and 210 K, for a Kapton hybrid laminated on ceramics.

5.5 Discussion on the results

A first electrical prototype module was assembled using a 50 µm pitch silicon microstrip sensor with an active area of 32.5 cm^2. Pitch adapter and support plate were processed on silicon.

The CMS ceramic hybrid with APV25 readout chips was characterized at low temperature. First results were shown down to 210 K, showing a decrease of the rise time and an increase of the pulse peak height with respect to the room temperature behaviour. The decrease of the rise time implies an increase of the band width. This explains why the integrated noise remains constant with temperature, while we see a decrease in the pedestal with decreasing temperature. Further tests are ongoing to characterize the electronics down to cryogenic temperatures.