

Chapter 8.

CONCLUSIONS AND FUTURE RESEARCH

8.1. Conclusions

This dissertation has comprehensively addressed the issues of modulation and control in multilevel converters. The main contributions and conclusions are summarized below.

- Phase models and line-to-line models of a generic n-level diode-clamped converter have been presented in this work. An averaged small-signal model of the three-level converter has been developed in the dq coordinates, which is applied to the design of optimal control loops. Since the modulation stage takes care of NP voltage balance the model is simplified; hence, the order of the multivariable controller can be reduced. This strategy guarantees optimal NP voltage control besides alleviating the control algorithm.

- A computationally efficient SV-PWM algorithm has been developed. Its short processing time hinges on the dq-gh transformation and on the fact that all of the calculations are processed in the first sextant. The equivalent vector in the first sextant has the property that interchanging the final states of the phase legs automatically generates the original reference vector. The switching frequencies of the devices are minimized due to applying optimal sequences of vectors. This modulation algorithm has been checked both by simulation and experimentally.

- NTV and symmetric modulation are compared and discussed. NTV can achieve best NP current control, while producing larger switching-frequency NP-voltage ripple. Symmetric modulation results in almost constant switching frequencies in the

devices, but at greater values than with NTV. In addition, the third-order harmonic in the NP ripple becomes more significant. The main advantage of symmetric modulation is that the amplitude of the NP voltage ripple due to the switching frequency is very small. This property makes symmetric modulation interesting for low-switching-frequency applications.

- The generic modulation algorithm presented in Chapter 3 for the three-level converter is extended to converters with a high number of levels in Chapter 4. Special attention is paid to the voltage-balancing issue, which becomes much more difficult than in the three-level converter. Two balancing criteria are analyzed for the selection of proper redundant vectors; both of them are based on minimizing a quadratic parameter related to the voltages in the capacitors. The modulation scheme is applied to the four-level converter, demonstrating that both criteria can achieve the same voltage-balancing results. The inability of the four-level converter to achieve voltage balance for some operating conditions is corroborated and the charge-balancing limits are described. These conditions involve large modulation indices and the existence of active AC currents.

- The low-frequency oscillation that appears in the NP of the three-level diode-clamped converter for some operating conditions can produce significant distortion in the output voltages. A novel feedforward SV-PWM is proposed to compensate for that distortion. The feedforward modulation is capable of generating a balanced set of three-phase voltages despite any imbalance in the NP, including constant imbalances. The algorithm takes advantage of symmetry in the unbalanced SV diagram, so that long operations are avoided. The processing time required is only 50% longer than for the algorithm that assumes balanced voltages in the DC-link capacitors. Static and dynamic voltage imbalances have been analyzed in the SMES prototype in order to validate the feedforward modulation experimentally.

- When the system operates as a rectifier with feedforward modulation, some NP voltage offset appears, which can degenerate into instability. The origin of this problem is justified and a solution is proposed, based on limiting the maximum modulation index to 0.95 for those operating conditions.

- Load imbalances produce negative effects on the NP voltage balance. Linear imbalances produce fundamental-frequency oscillations in the NP voltage, while the effects of nonlinear imbalances are summarized in the following. Odd-order current harmonics also cause low-frequency oscillations in the NP voltage; nevertheless,

their averaged value can be kept at one-half the level of the DC-link voltage. In addition to the low-frequency oscillation, even-order harmonics produce the NP voltage to shift. The fourth-order harmonic may cause the system to be unstable. The amount of fourth-order harmonic that the system can stand in the steady-state condition is graphically described. Only fundamentals and fourth-order harmonics are assumed in the analysis. In such condition, instability may appear for modulation indices beyond 0.8 and the worst cases are given for low PFs.

- Two multilevel converters connected back-to-back can share the NP balancing task; thus, they can achieve better balancing results than a single converter operating with a passive front-end. The limits within which two three-level diode-clamped converters can achieve NP voltage balance have been described. The low-frequency oscillation can be removed for an extended operating area and, in addition, it is significantly attenuated for all other operating conditions.

- An LQR with integral actuation is implemented for controlling a boost rectifier system based on the NPC converter. The NP voltage balancing is carried out by the modulation stage, releasing the controller from this task. Efficiency of the feedforward modulation is also tested in this controlling diagram, which is shown to be interesting for non-unity PF operation, when significant NP voltage oscillations may appear. Simulated and experimental results of the LQR show very good static and dynamic performance of the system.

8.2. Future Research

There are several interesting topics suggested for further research in multilevel converters, some of which have been already initiated and are expected to obtain some results soon. These topics are described in the following.

- Further comparison between NTV modulation and symmetric modulation when operating at very low switching frequencies can be made. The inconvenience of the third-order harmonic in the NP voltage may be less significant compared with the switching-frequency ripple in such conditions, rendering some advantages to symmetric modulation. A modified symmetric modulation that can achieve better balancing performance can also be investigated. In the symmetric modulation described in this dissertation Region 2 and Region 4 have been graphically split into 2L-2H and 4L-4H. A dynamic boundary for those regions can be redefined in accordance with a new criterion. This criterion would take into consideration which pair of redundant vectors have more NP current control at any time, so that both of them will be included in the sequence. As a result, while the reference vector is in Region 2 and Region 4, the sequences would not depend on the exact position of the reference vector, but on a NP current control criterion.

- Significant voltage-balancing improvements are obtained by the back-to-back connection of three-level diode-clamped converters. It might be interesting to find out the limits of voltage balancing for converters with a higher number of levels in this connection. The proposed strategies for minimizing voltage errors in the capacitors in Chapter 4 can be used; however, the entire back-to-back system must be considered in order to define optimal selection of redundant vectors.

- More research should be done on the floating-capacitor and cascade converters in order to clarify and quantify advantages and drawbacks compared with diode-clamped converters. The results of the analysis will suggest the best topology to be used depending on specifications in each application.

Some additional future research topics are described in the following sections.

8.2.1 Correction of Narrow Pulses

Dead time must be given to the turn-on signal of a switch for compensating for different switching timings. Since the turn-on time of a power device is faster than its

turn-off time, its activation must be delayed in order to avoid short circuits. This task is usually performed in the same driver.

As a consequence of the natural switching delays and the required dead time, narrow pulses generated in the modulator are filtered and they may not affect the output voltages of the converter. Furthermore, pulses that make a switch commute only for a very short time can slightly alter the AC variables, while producing additional switching losses. On the other hand, narrow pulses become an important problem for soft-switching operation, since the resonant process involved in the soft-switching transition requires a minimum time for proper operation. Thus, a minimum value of duty cycle for the control signals of the switches must be defined to avoid these problems.

From the standpoint of SVM, when a duty cycle of a vector is too small, it may not result in a small duty cycle for the switches. Evaluation of the conditions in which a vector duty cycle needs to be corrected and the consequences of its correction in the output voltages of a multilevel converter should be investigated. Some ideas for the analysis are suggested in the following.

When dealing with NTV modulation in the three-level converter, for instance, a potentially small duty cycle in the switch can be produced when the first or the last vector of a sequence have assigned a small duty cycle. The problem may appear when two consecutive sequences of vectors change. For example, when changing from sequence 100-200-210 to 200-210-211, if the duty cycle assigned to the vector 210 in the first sequence is too small, a narrow pulse will be applied to two switches in phase *b*. Also, a small duty cycle of a switch may appear in phase *b* within the sequences 100-210-221 and 100-111-221. The potentially critical duty cycles of vectors are indicated in bold format in Table 8.1.

Table 8.1. Duty cycles that may produce narrow pulses in the devices.

Region	Short Vectors	Sequences
1	100	100-200-210
	211	200-210-211
2	100-110	100-110-210
	100-221	100-210-221
	211-110	110-210-211
	211-221	210-211-221
3	110	110-210-220
	221	210-220-221
4	100-110	100-110-111
	100-221	100-111-221
	211-110	110-111-211
	211-221	111-211-221

Fig. 8.1 indicates in gray the areas in which small duty cycles of vectors are produced.

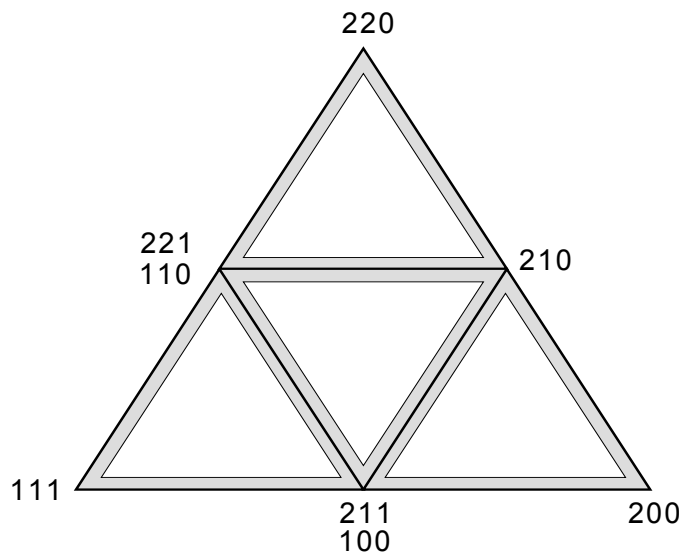


Fig. 8.1. Concerned areas for small duty cycles of vectors in the first sextant.

A generic sequence of vectors is defined as \vec{v}_1 , \vec{v}_2 and \vec{v}_3 and their duty cycles are d_1 , d_2 , and d_3 , respectively. The reference vector can be expressed as follows:

$$\vec{m} = d_1\vec{v}_1 + d_2\vec{v}_2 + d_3\vec{v}_3. \tag{8.1}$$

When one of these duty cycles is too small and needs correction, for example d_1 , a minimum value should be defined for this duty cycle ($d_1=D_{min}$). The remainder duty cycles must be also corrected in order to keep the constant modulation period. A proportional distribution is suggested, as follows:

$$d_1' = D_{\min}, \quad d_2' = k d_2, \quad \text{and} \quad d_3' = k d_3. \quad (8.2)$$

Taking into account that $d_1' + d_2' + d_3' = 1$, the distributing parameter is:

$$k = \frac{1 - D_{\min}}{1 - d_1}. \quad (8.3)$$

The new duty cycles are:

$$d_1' = D_{\min}, \quad d_2' = \frac{1 - D_{\min}}{1 - d_1} d_2, \quad \text{and} \quad d_3' = \frac{1 - D_{\min}}{1 - d_1} d_3, \quad (8.4)$$

and the modified reference vector becomes:

$$\vec{m}' = d_1' \vec{v}_1 + d_2' \vec{v}_2 + d_3' \vec{v}_3 = \frac{1 - D_{\min}}{1 - d_1} \vec{m} + \frac{D_{\min} - d_1}{1 - d_1} \vec{v}_1. \quad (8.5)$$

The error produced in the reference vector as a result of this correction is:

$$\vec{\varepsilon} = \vec{m}' - \vec{m} = -\frac{D_{\min} - d_1}{1 - d_1} (\vec{m} - \vec{v}_1). \quad (8.6)$$

Equation (8.6) reveals that the new vector \vec{m}' is on the straight line that joins the tips of the vectors \vec{v}_1 and \vec{m} and it is outside of the critical area (Fig. 8.2).

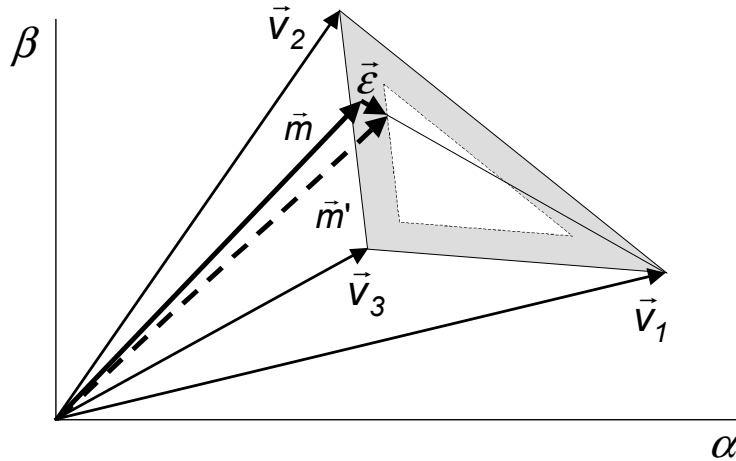


Fig. 8.2. Displacement of the reference vector due to small duty-cycle correction ($d_1 < D_{\min}$).

Distortion produced in the output voltages and currents as a result of this correction should be evaluated.

The critical areas in which small duty cycles are produced can be avoided by redefining the regions in the SV diagram as in [A57-A59]. Consequently, no error is produced in the reference vector, although the switching frequencies of the devices will increase.

8.2.2 Complete NP-Balancing Modulation Strategies

Optimal utilization of nearest vectors to the reference vector can guarantee good output voltage spectra and minimum switching frequencies. However, the low-frequency ripple that appears in the NP voltage of the three-level converter is an inconvenience. Although feedforward modulation can compensate for some of the effects of this oscillation, i. e. distortion in the output voltages, the voltages applied to the devices are higher than if the NP voltage is kept constant at one-half the level of the DC-link voltage. If utilization of nearest vectors is not a constraint, the NP voltage oscillation can be removed but at the price of worsening output voltage spectra and increasing the switching frequencies of the devices. An extreme example of this is when the only vectors that do not use the NP connection are used for generating the reference vector. In this case, no current would flow into the NP, and hence, no NP voltage imbalance would be produced at all. In such condition, the three-level converter is being used as a two-level converter; therefore, this modulation would not have the benefits of multilevel conversion. Other intermediate solutions in between this modulation and the nearest-vector modulation can be found.

Zero-averaged NP current over a modulation period can be achieved by using certain combinations of vectors that produce opposite effects on the NP current. Accordingly to this idea, an interesting zero-NP-current modulation is exposed in [B5] which is briefly described in the following.

The short vectors of a set of redundant vectors produce opposite NP-current directions. Hence, if the time assigned to a pair of vectors is shared 50% between both of them, the averaged NP current will be zero. In accordance with this use of the redundant vectors, the pairs 100-211 and 110-221 can be understood as zero-NP-current vectors. Similarly, when the vectors 100, 210 and 221 are applied by assigning equal time to each of them (33,33%). As a result, a new SV diagram composed of only zero-NP-current vectors is obtained, which is shown in Fig. 8.3(b). Calculation of duty cycles should be made in the new regions. The method of projections explained in Chapter 3 can be used for this purpose.

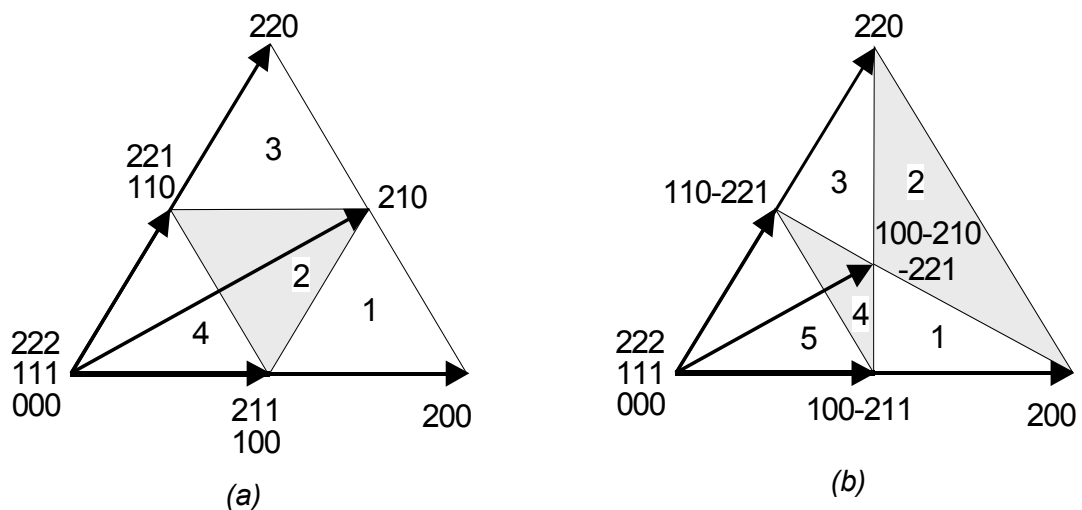


Fig. 8.3. First-sextant regions:
 (a) standard nearest-vector distribution and
 (b) new regions based on zero-NP-current vectors.

Since this modulation method is able to eliminate the low-frequency NP oscillation, the DC-link capacitors can be significantly reduced. Nevertheless, slight NP voltage control should be included in order to compensate for possible imbalances. Implementation of this SV-PWM strategy in a computationally efficient algorithm, and the evaluation of switching frequencies and output-voltage spectra may be an interesting area of future research. The results of the analysis will point out which applications and under which conditions this modulation will be most useful.

