Chapter 6.

IMBALANCES AND ADDITIONAL MODULATION ISSUES

6.1. Introduction

In this chapter, some practical modulation and NP voltage-balancing aspects in the three-level diode-clamped converter have been taken into consideration.

The consequences of different values in the capacitors are analyzed from the standpoint of the NP balance and the DC link.

Loading conditions have a profound impact on the design and performance of power converters. In most cases, a power converter is designed under the assumption of a balanced load-source; however, in reality imbalances and nonlinearities are quite frequent. The effects of linear and nonlinear load imbalances on the NP voltage balance are described.

Although feedforward modulation can avoid low-frequency distortion in the AC voltages, the maximum voltages applied to the devices increase due to the NP voltage oscillation. Two back-to-back-connected converters can perform a unity-power-factor application with the additional benefit of improving NP voltage balancing. The balancing limits of such a connection are investigated.

Finally, overmodulation is also addressed in this chapter.

6.2. Different Values of the DC-Link Capacitors

So far, the values of the DC-link capacitors have been assumed equal. However, the capacitors can be different due to, for instance, tolerances. The consequences of this imbalance in the three-level converter are evaluated in this section.

The dynamic circuit of the NP connection is shown in Fig. 6.1. In this model, the DC-link voltage is assumed to be constant, which can be achieved by either a DC-power supply or by controlling this voltage by a proper control loop.

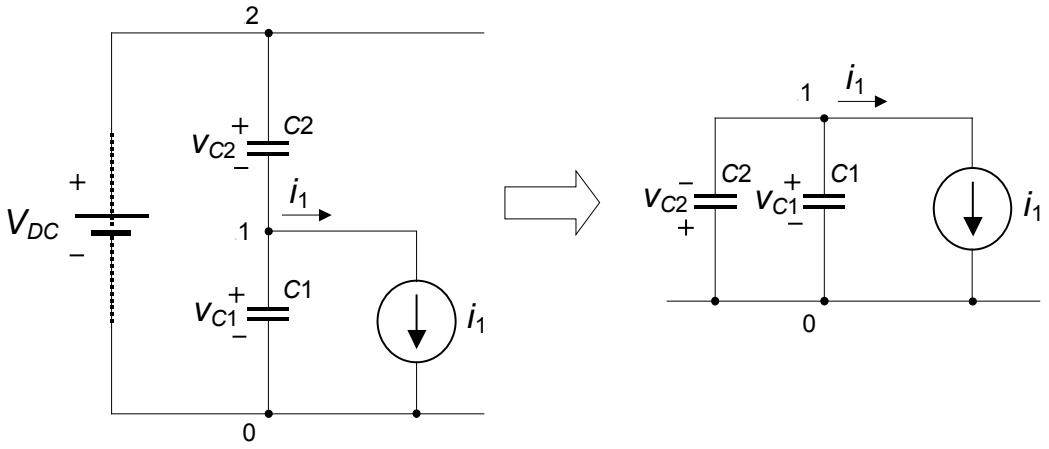


Fig. 6.1. *Dynamic model of the NP in the three-level converter.*

The values of each of the capacitors are not important from the standpoint of NP voltage balance since they are virtually connected in parallel. Therefore, the equivalent value is:

$$C_{NP\,equiv} = C1 + C2 . \tag{6.1}$$

On the other hand, the capacitors are connected in series from the DC-link standpoint, therefore:

$$C_{DC\,equiv} = \frac{C1 \cdot C2}{C1 + C2} . \tag{6.2}$$

In conclusion, slightly different values of the capacitors hardly affect the dynamics of the NP voltage. Nevertheless, they should not be much different; otherwise their filtering effect on the DC-link voltage will be diminished due to the series connection.

6.3. AC-Side Imbalances

In this section, linear load imbalances are presented from the standpoint of symmetrical components theory. Furthermore, nonlinear loads are analyzed by modeling the output currents as harmonic current sources. Their effects on the NP voltage balancing are described.

6.3.1. Linear Imbalances

6.3.1.1. Symmetric Components

The symmetric-component representation was first proposed by C. L. Fortescue in 1918 and became a textbook method for analyzing unbalanced conditions in power systems.

An arbitrary unbalanced three-phase current (or voltage) is expressed as:

$$\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \begin{bmatrix} \hat{I}_a \sin(\omega t + \varphi_a) \\ \hat{I}_b \sin(\omega t + \varphi_b) \\ \hat{I}_c \sin(\omega t + \varphi_c) \end{bmatrix}, \tag{6.3}$$

or it can also be represented by phasor notation with six variables $\mathbf{I}_a = I_a \angle \varphi_a$, $\mathbf{I}_b = I_b \angle \varphi_b$, and $\mathbf{I}_c = I_c \angle \varphi_c$. According to the symmetrical components theory, these variables can be represented by three sets of balanced three-phase currents; positive sequence $\mathbf{I}_p = I_p \angle \varphi_p$, including $\mathbf{I}_{ap}$, $\mathbf{I}_{bp}$, and $\mathbf{I}_{cp}$; negative sequence $\mathbf{I}_n = I_n \angle \varphi_n$, including $\mathbf{I}_{an}$, $\mathbf{I}_{bn}$, and $\mathbf{I}_{cn}$; and zero sequence $\mathbf{I}_o = I_o \angle \varphi_o$, which is the same for all of the three phases. The transformation from abc variables into symmetrical components is:

$$\begin{bmatrix} \mathbf{I}_p \\ \mathbf{I}_n \\ \mathbf{I}_o \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & \vec{a} & \vec{a}^2 \\ 1 & \vec{a}^2 & \vec{a} \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} \mathbf{I}_a \\ \mathbf{I}_b \\ \mathbf{I}_c \end{bmatrix}, \tag{6.4}$$

where $\vec{a} = e^{j2\pi/3}$. The inverse transformation is as follows:

$$\begin{bmatrix} \mathbf{I}_a \\ \mathbf{I}_b \\ \mathbf{I}_c \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ \vec{a}^2 & \vec{a} & 1 \\ \vec{a} & \vec{a}^2 & 1 \end{bmatrix} \begin{bmatrix} \mathbf{I}_p \\ \mathbf{I}_n \\ \mathbf{I}_o \end{bmatrix}. \tag{6.5}$$

From (6.4) and (6.5), the abc currents can also be obtained by

$$\begin{bmatrix} \mathbf{I}_a \\ \mathbf{I}_b \\ \mathbf{I}_c \end{bmatrix} = \begin{bmatrix} \mathbf{I}_{ap} + \mathbf{I}_{an} + \mathbf{I}_{ao} \\ \mathbf{I}_{bp} + \mathbf{I}_{bn} + \mathbf{I}_{bo} \\ \mathbf{I}_{cp} + \mathbf{I}_{cn} + \mathbf{I}_{co} \end{bmatrix}. \tag{6.6}$$

An example of symmetrical component decomposition of an arbitrary unbalanced load is shown in Figure 6.2.

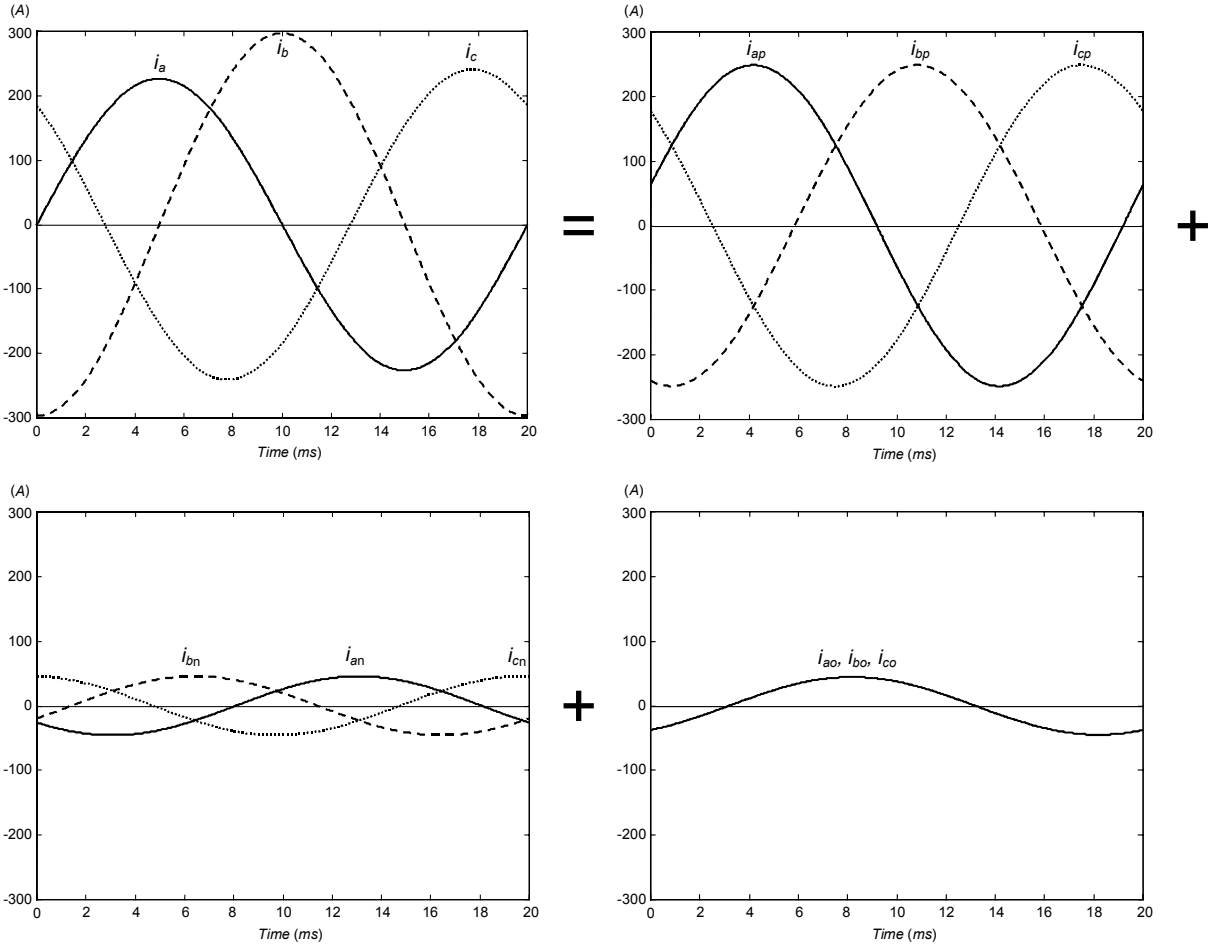


Fig. 6.2. *Example of symmetrical component decomposition.*

There is no zero-current sequence operating with delta- or star-load connection with the neutral open, since $i_a + i_b + i_c = 0$. This loading condition is assumed in the system analyzed in this dissertation, therefore only negative sequences of currents are considered as linear imbalances.

6.3.1.2. Effects of Linear Imbalances on the NP Balance

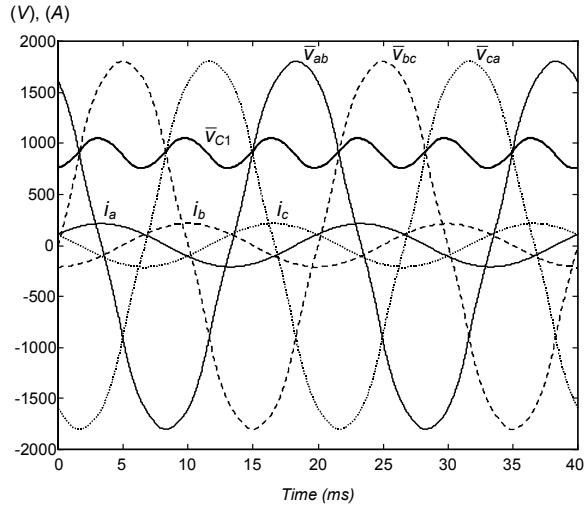
There are infinite possibilities of linear imbalances. The following analysis is based on some simulated examples and describes the main effects of a negative sequence of output currents on the NP voltage.

For these examples, the converter is supplied by a DC source of V_{DC}=1800 V, the DC-link capacitors are C=550 μF and the output currents are provided by a set of three-phase current sources whose frequency is f=50 Hz. Maximum modulation index is considered (m=1), since this is the worst case for the NP voltage to achieve balance (the short vectors have less influence on the NP current).

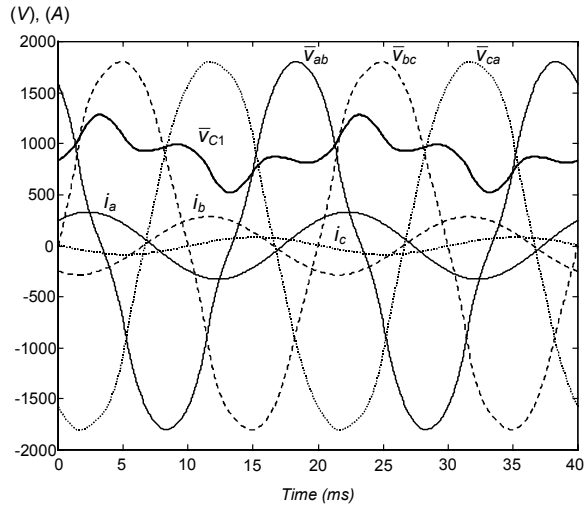
Fig. 6.3 shows the averaged voltage of the lower capacitor (v_{C1}), the averaged line-to-line voltages (v_{ab}, v_{bc} and v_{ca}) and the AC currents (i_a, i_b and i_c). Case (*a*) only considers positive sequences of currents with RMS value I_{RMSp}=150 A and phase φ_p=-60°. In case (*b*), a negative sequence of currents with I_{RMSn}=100 A and phase φ_n=-15° is added to the positive sequence. Finally, this negative sequence is the only one considered for case (*c*).

The amplitude of the NP-voltage ripple increases when a negative sequence of currents exits (linear imbalance). In addition, the frequency of this ripple is the same as that of the fundamentals of the output voltages; thus, requiring larger capacitors for attenuation.

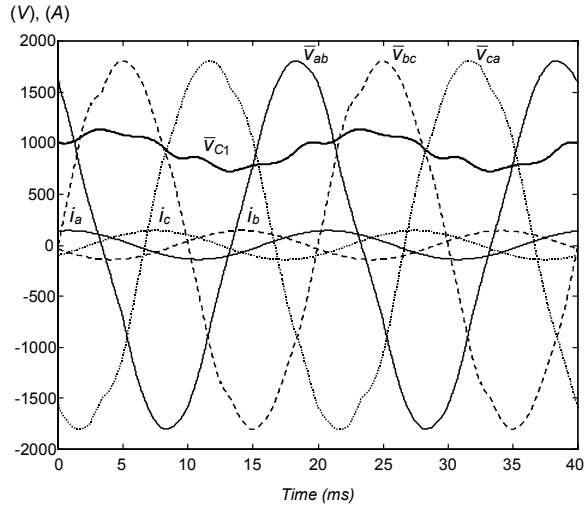
Nevertheless, no NP-voltage instability has been observed when operating with linear imbalances.



(a)



(b)



(c)

Fig. 6.3. *Averaged variables for different loading conditions:*
(a) balanced linear load,
(b) positive and negative sequences of currents, and
(c) only negative sequence of currents.

6.3.2. Nonlinear Loads

Nonlinear loads are characterized by the existence of some order harmonics in the spectra of the currents that do not exist in the voltages applied to the load. Systems that contain power devices in switching mode operation are the most common nonlinear loads (diode and thyristor rectifiers, switching mode power supplies, etc.). There are also some other typical nonlinear loads, such as arc furnace, or saturated magnetic cores.

A balanced set of three-phase voltage sources can be expressed as follows:

$$\begin{bmatrix} v_a \\ v_b \\ v_c \end{bmatrix} = \begin{bmatrix} \hat{V}\sin\omega t \\ \hat{V}\sin(\omega t - 2\pi/3) \\ \hat{V}\sin(\omega t + 2\pi/3) \end{bmatrix}, \tag{6.8}$$

where $\hat{V}$ is the amplitude of the line-to-neutral voltage. The resulting currents through a nonlinear load can be represented by

$$\begin{bmatrix} i_a \\ i_b \\ i_c \end{bmatrix} = \begin{bmatrix} \hat{I}_1\sin(\omega t + \varphi_1) + \sum_{h=2}^{\infty}\hat{I}_h\sin(h\omega t + \varphi_h) \\ \hat{I}_1\sin(\omega t + \varphi_1 - 2\pi/3) + \sum_{h=2}^{\infty}\hat{I}_h\sin(h\omega t + \varphi_h - 2\pi/3) \\ \hat{I}_1\sin(\omega t + \varphi_1 + 2\pi/3) + \sum_{h=2}^{\infty}\hat{I}_h\sin(h\omega t + \varphi_h + 2\pi/3) \end{bmatrix}. \tag{6.9}$$

The nonlinearity performance of the load can be quantified according to the magnitude of harmonics by the THD defined in (3.40). This parameter, however, does not provide information about how the components are distributed in the spectra.

6.3.2.1. Effects of Nonlinear Loads on the NP Balance

Nonlinear loads produce negative effects on the NP voltage balance [A36]. The following analysis shows some of the consequences produced in the NP voltage by positive sequences of low-frequency current harmonics.

Fig. 6.3 shows how the NP voltage oscillates as a consequence of some h-order current harmonics. In these simulations, the currents are generated by current sources and no fundamental has been included. The modulation index is the maximum (m=1).

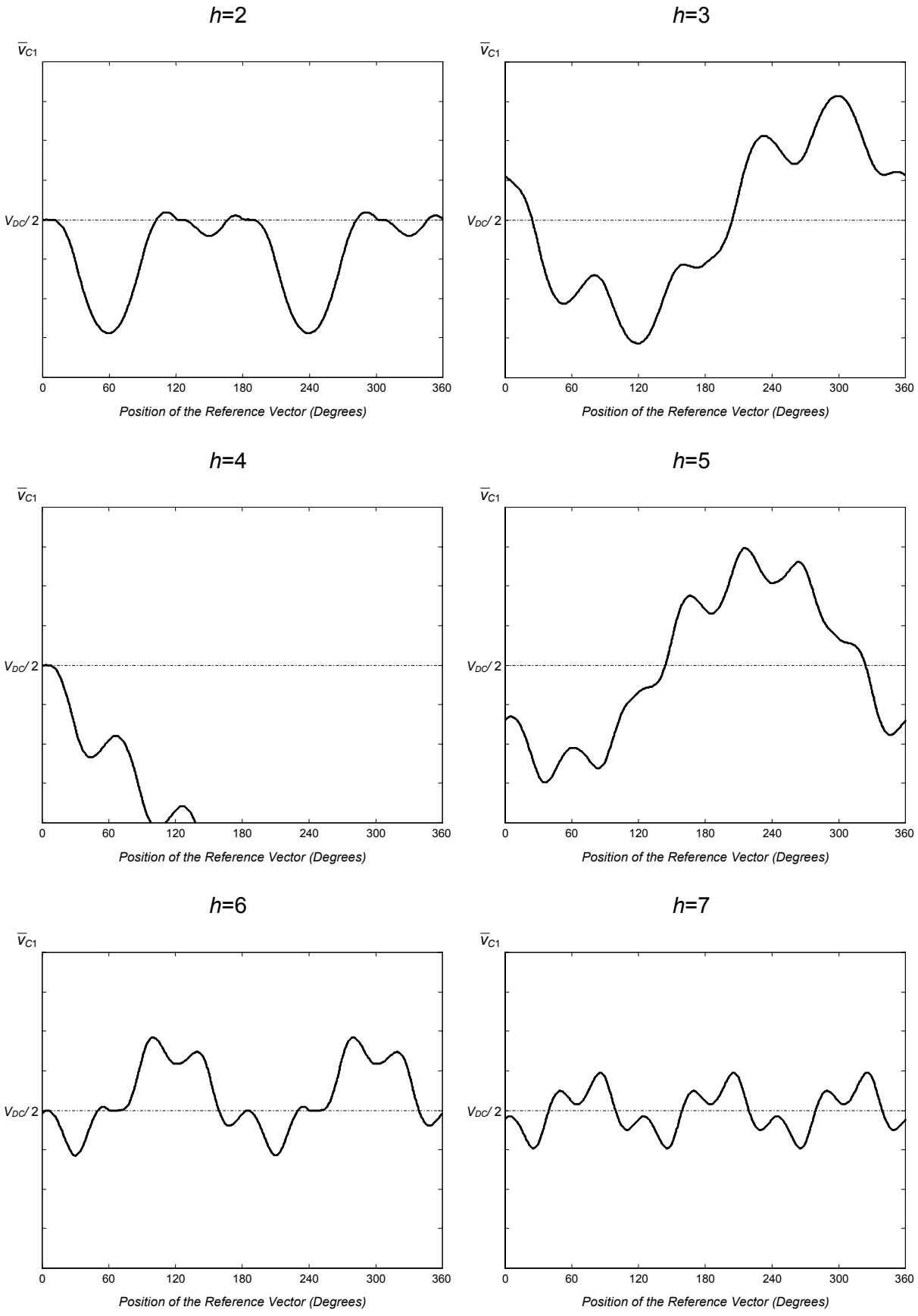


Fig. 6.4. *Low-frequency NP voltage oscillation produced by some h-order current harmonics.*

Odd-order current harmonics produce low-frequency oscillations in the NP voltage; however, their averaged value can be maintained at a half the level of the DC-link voltage. In addition to the low-frequency oscillation, even-order current harmonics cause the NP voltage to shift. The fourth-order harmonic (h=4) may cause the system to be unstable. The reason why this harmonic is so critical is explained in the following.

Fourth-order current harmonics with an initial phase of ±90º is the worst case regarding system stability. The medium vectors produce NP current that mostly has the same direction because of this harmonic. For example, if the initial phase of this harmonic is +90º, the current i_b is mostly positive during the time that the reference vector is in the first sextant (Fig. 6.5). As a result, when vector 210 is applied, the NP current is generally positive as well. A similar phenomenon happens in the other sextants when using the medium vectors; thus, producing the same polarity in the NP current. In the case of large modulation indices, the medium vectors take high values of duty cycles and the short vectors cannot take over the NP current. As a result, NP voltage balance cannot be achieved, making the system unstable.

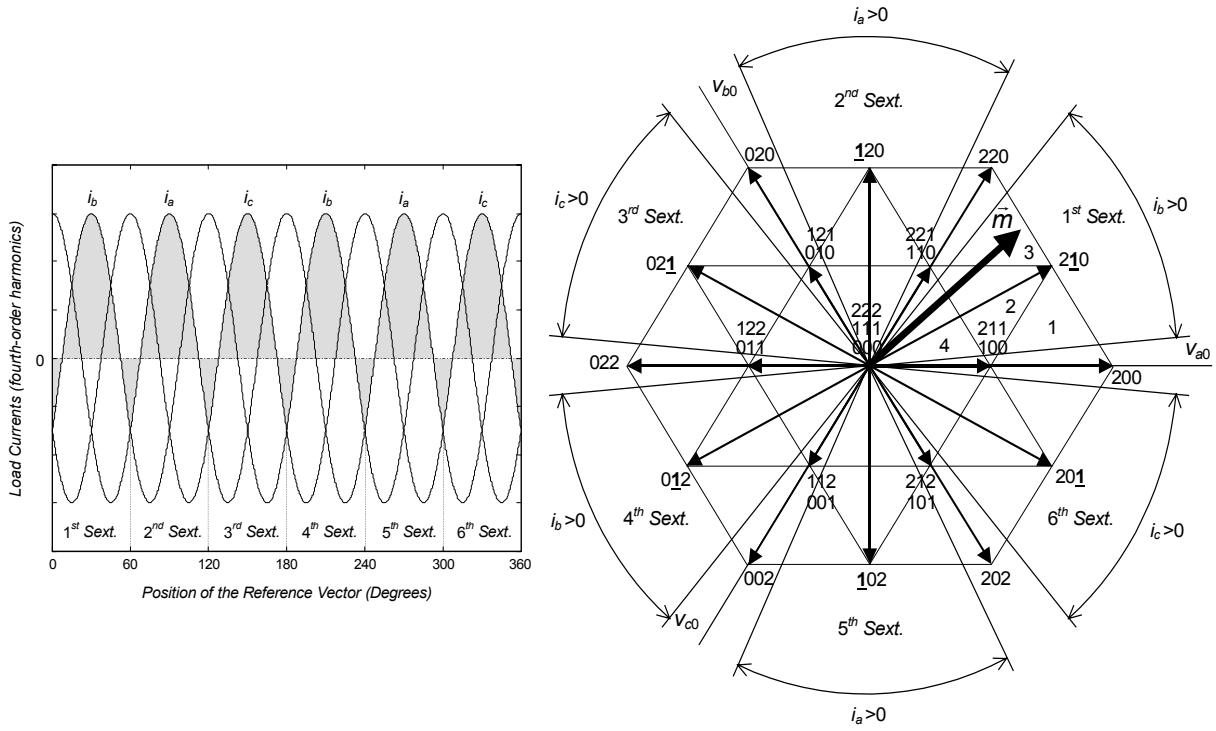
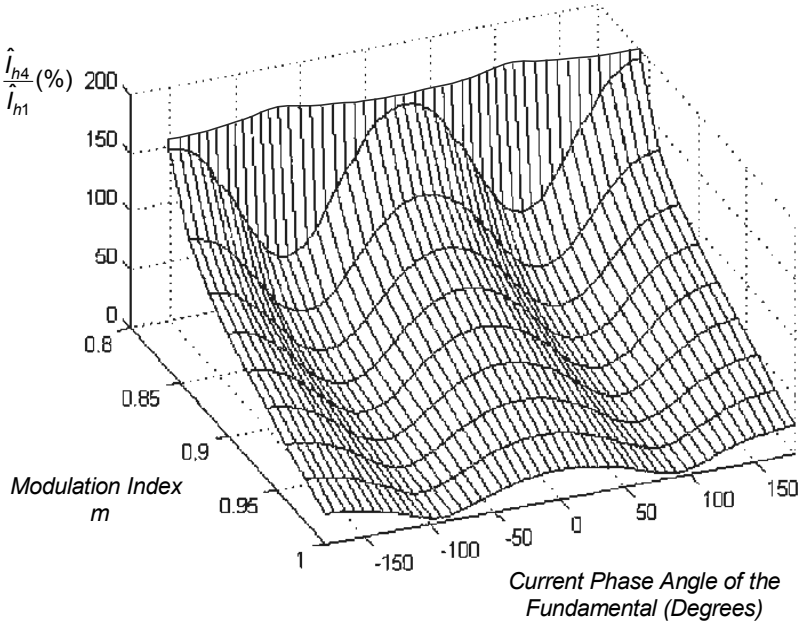


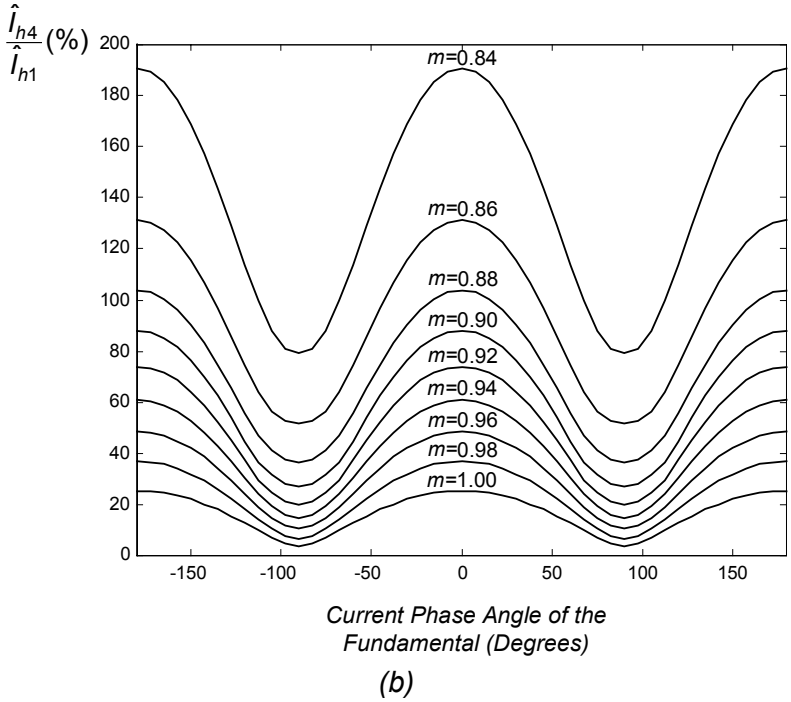
Fig. 6.5. *Direction of the currents in the SV diagram as a consequence of a set of fourth-order current harmonics.*

Although the fundamentals of the load currents help to achieve NP balance, the existence of fourth-order harmonics may still produce instability. The maximum

amplitude acceptable for this harmonic is represented in Fig. 6.6. Amplitude ratios between the fourth-order harmonic and the fundamental ($\hat{I}_{h4}/\hat{I}_{h1}$) that have values under the surface in Fig. 6.6(a) guarantee stability of the system in the steady-state condition operating with high switching frequencies. The modulation index and the phase of the fundamentals play a part in the representation. The analysis assumes the worst phase condition for the fourth-order harmonic (φ_4= ±90º).



(a)



(b)

Fig. 6.6. *Maximum amplitude of the fourth-order harmonic in the steady-state condition.*

It can be observed that the most critical case for the fundamentals is when they have a phase of ±90º. In such conditions, and for a modulation index of m=1, the maximum amplitude acceptable for the fourth-order harmonic is only 3.4 % of the fundamental. It is important to remark that modulation indices below or equal to 0.8 guarantee stability of the system from the fourth-order harmonic.

Nonlinear loads usually produce an infinite number of current harmonics; thus, evaluation of their effects on the NP balance must be made for each specific case.

6.3.3. Experimental Results

Some linear imbalances and nonlinear loads are applied to the three-level converter of the SMES prototype in order to certify their negative effects on the NP voltage balance. For the experimental results, the DC-link voltage is maintained to V_{DC}=50 V by a DC-power source and an asynchronous motor is always connected as a linear load. The output frequency is f=60 Hz and the modulation index is maximum m=1.

Fig. 6.7 shows the circuit used in the analysis. A two-ohm resistance is connected between phases *a* and *b* in order to produce a linear imbalance. In the case of nonlinear loads, a diode is added in series with the resistance. The polarity of the diode is changed in order to verify the consequences on the voltages of the DC-link capacitors.

Fig. 6.8 shows two of the output currents (i_a and i_c) and the voltages of the capacitors (v_{C1} and v_{C2}) when the asynchronous motor is the sole connected load. The effect on the NP potential when the resistor is connected is presented in Fig. 6.9. This linear imbalance produces additional low-frequency voltage ripple in the NP voltage. The ripple reaches considerable amplitude due to its low frequency; however, it is centered at a half of the DC-link voltage. Lastly, the diode is connected in series with the resistor (Fig. 6.10 and Fig. 6.11). This nonlinearity not only produces low-frequency NP voltage ripple, but also the voltages of the capacitors are shifted from their operating points. The signs of the offsets depend on the position of the diode. As a result of this nonlinear load the capacitors and the devices of the bridge must support higher voltage.

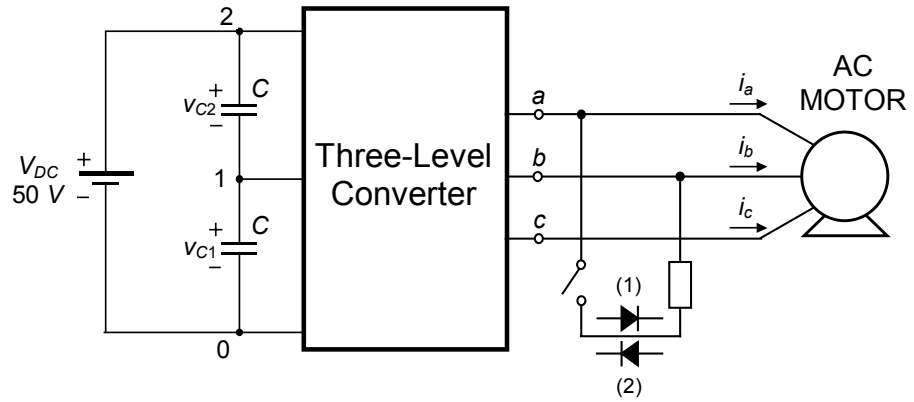


Fig. 6.7. *Connection used for the analysis of linear imbalances and nonlinear loads.*

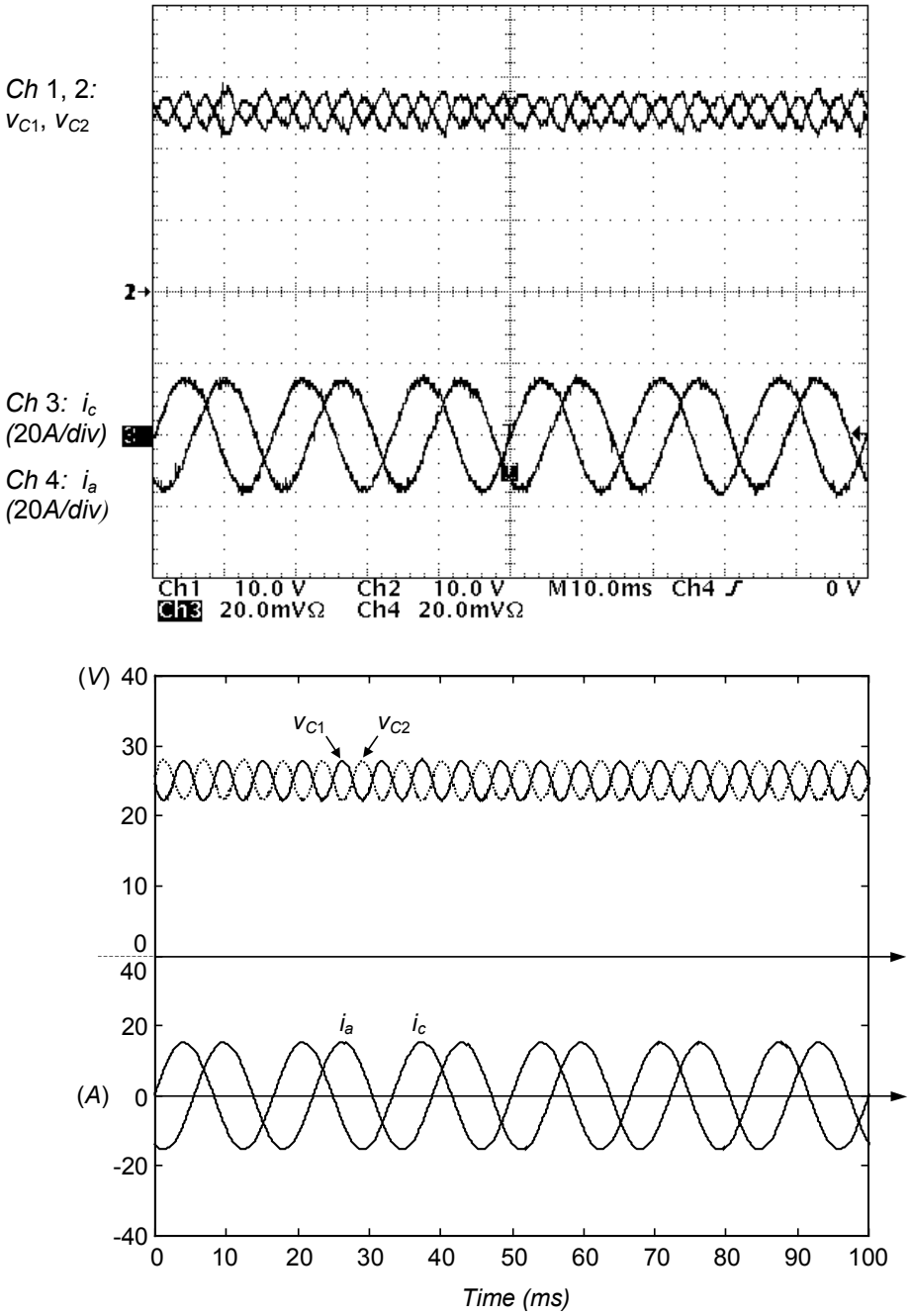


Fig. 6.8. *Balanced linear load.*

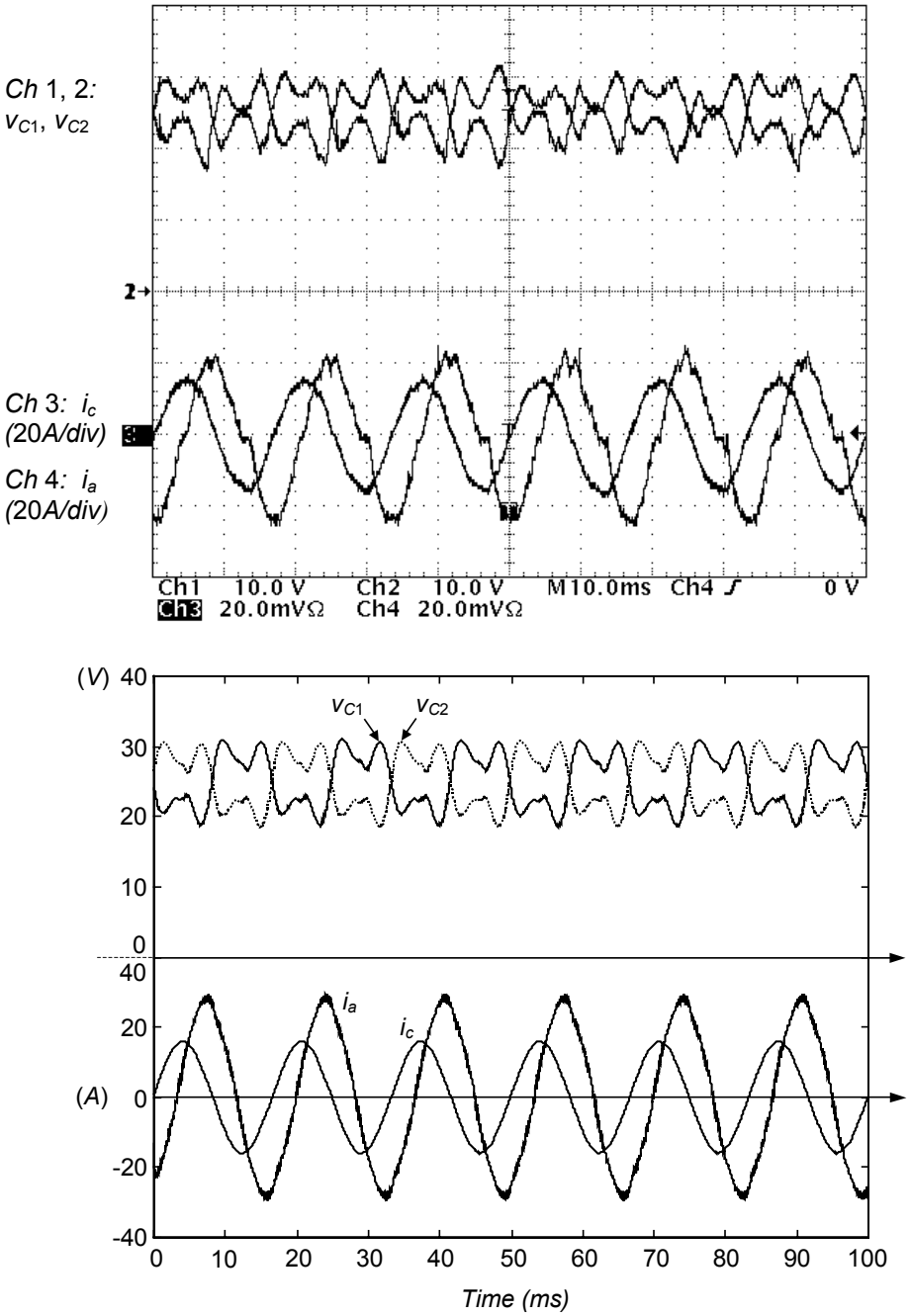


Fig. 6.9. *Unbalanced linear load.*

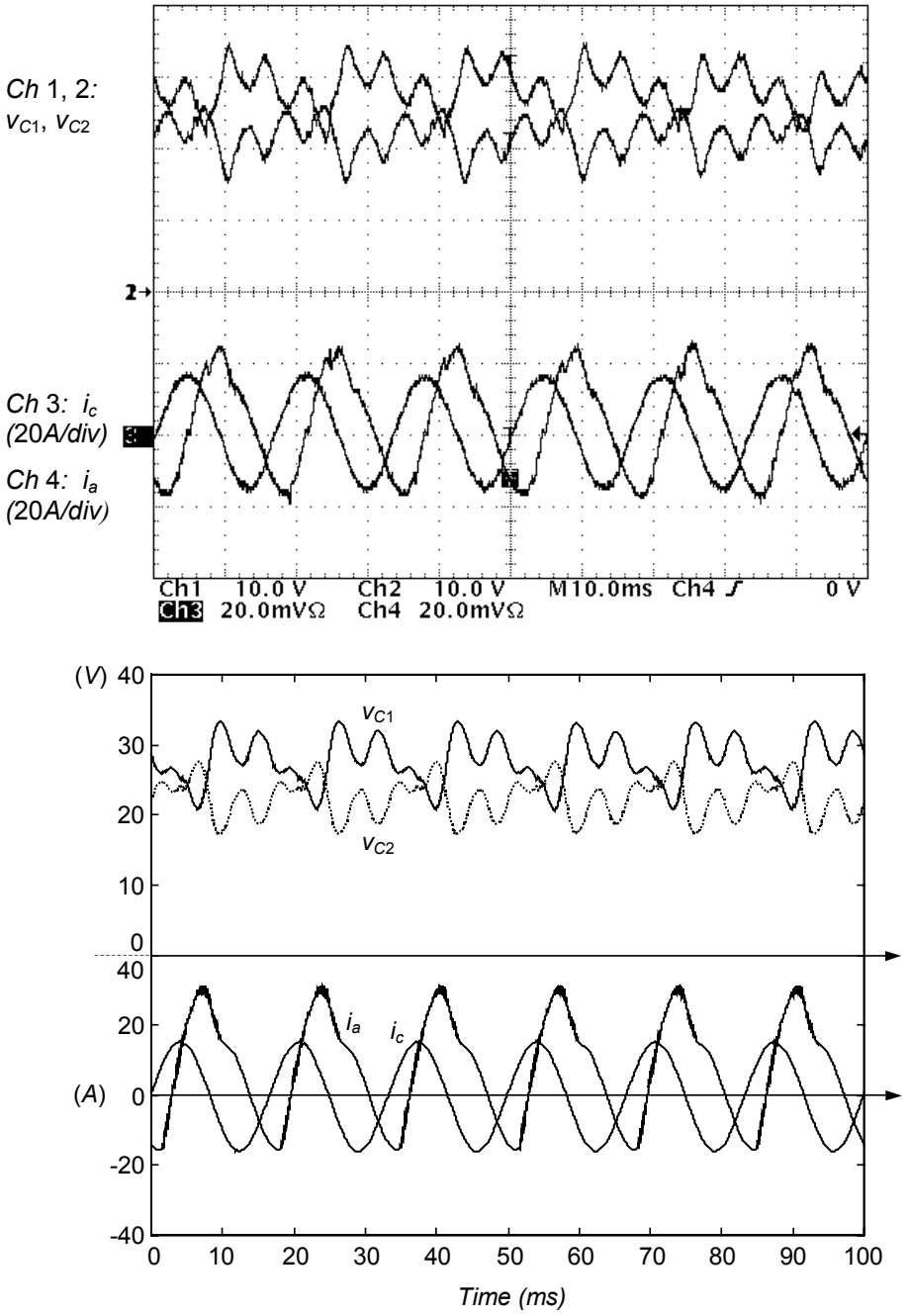


Fig. 6.10. *Nonlinear load (case 1).*

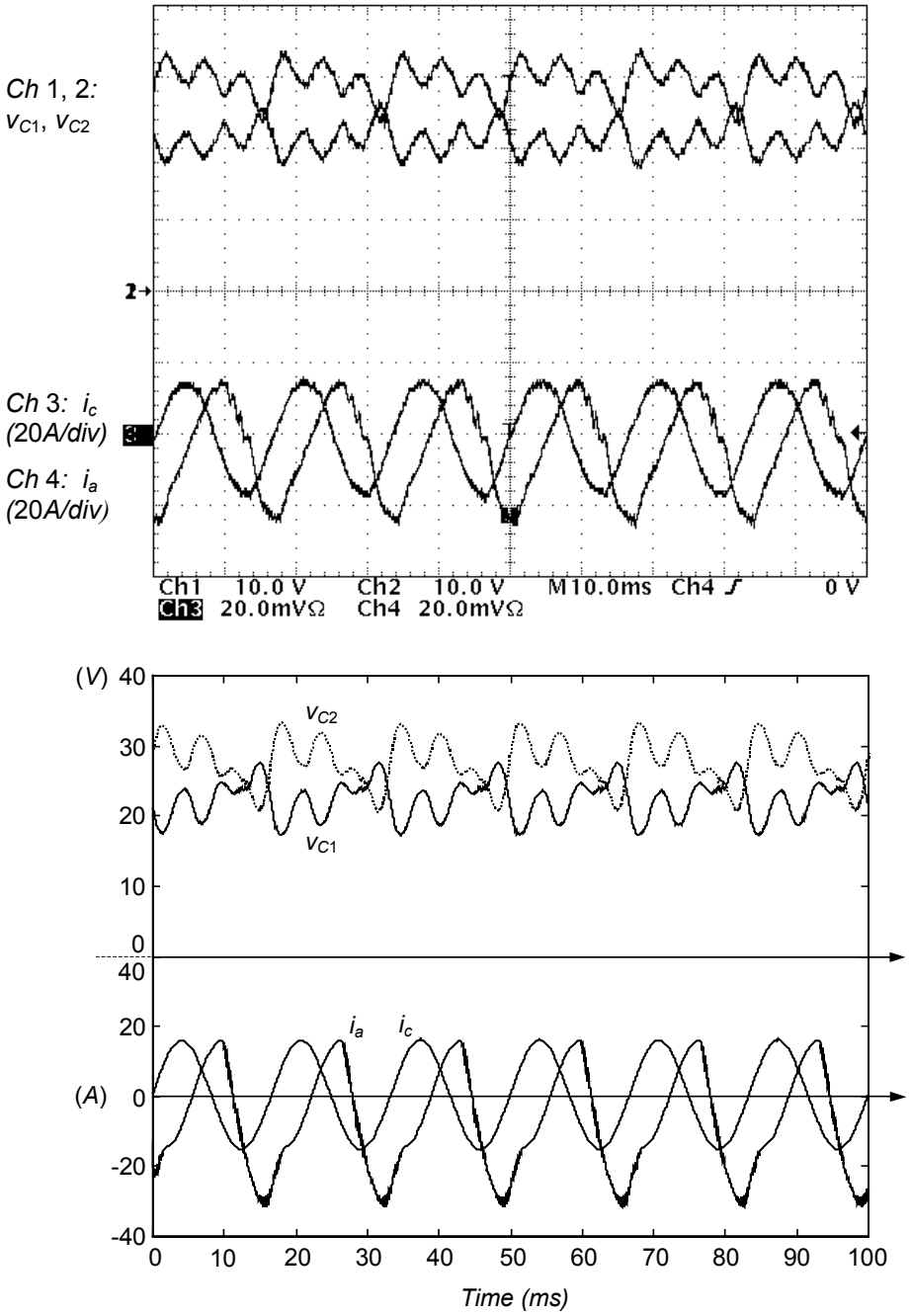


Fig. 6.11. *Nonlinear load (case 2).*

6.4. Back-to-Back Connection

NTV modulation cannot remove the low-frequency NP voltage for the entire operating area of the converter; however, significant improvements can be achieved if more than one converter are connected back-to-back to the same DC-link. A bi-directional motor drive application is a practical example in which two converters can be connected back-to-back. Nevertheless, the following analysis is general and it is not restricted to this application.

Fig. 6.12 shows a bi-directional motor drive system based on two three-level converters. In this connection, the converters can share the NP balancing task, so that each converter can supply current to the NP for the voltage balance, and thus, they can contribute much more efficiently to the balance.

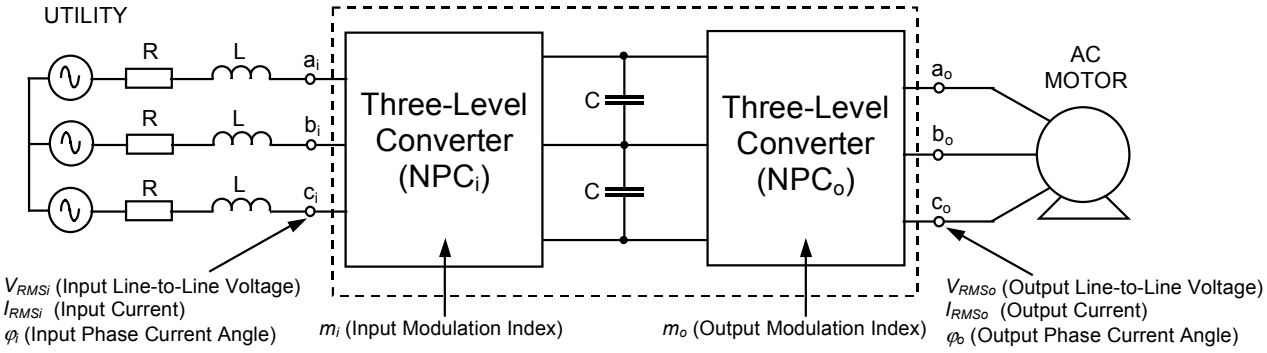


Fig. 6.12. *Three-level motor drive application with active front end.*

The main assumptions for this analysis are that:

- each converter is independently controlled;

- the NTV modulation technique is applied; and

- only the fundamentals for the input and output currents are considered.

The active power from the utility and the active power given to the motor can be respectively expressed as:

$$P_i = \sqrt{3}\, V_{RMSi}\, I_{RMSi} \cos\varphi_i \quad \text{and} \quad P_o = \sqrt{3}\, V_{RMSo}\, I_{RMSo} \cos\varphi_o \,. \tag{6.20}$$

Taking into account the total efficiency of both converters (η), and that the modulation indices are the ratio between the amplitude of the line-to-line voltages and the DC-link voltage, $m_i = \hat{V}_i / V_{DC}$ and $m_o = \hat{V}_o / V_{DC}$, the RMS input current can be expressed as

$$I_{RMSi} = \frac{I_{RMSo}}{\eta \cos\varphi_i} \frac{m_o \cos\varphi_o}{m_i}. \tag{6.21}$$

Two mathematical models of the NP current (3.43) are used to determine the balance limits in the back-to-back connection. Since the fundamental frequency of the output currents is not constant, the NP-current waveforms are not synchronized and they cannot fit into each other to achieve better balancing performance. Therefore, their minimum values (i_{1min}) must be considered in the analysis.

Fig. 6.13 has been obtained assuming an efficiency of 100% (η=1) and a unity input PF ($|PF_i|$=1). The RMS value of the output current in the inverter is defined as constant, and (6.21) provides the input current in the rectifier. The curves in this figure have been determined when the rectifier supplies the minimum NP current required for the balance, compensating for the defect of NP current from the inverter. Therefore, such curves define the limits for the control of the NP balance.

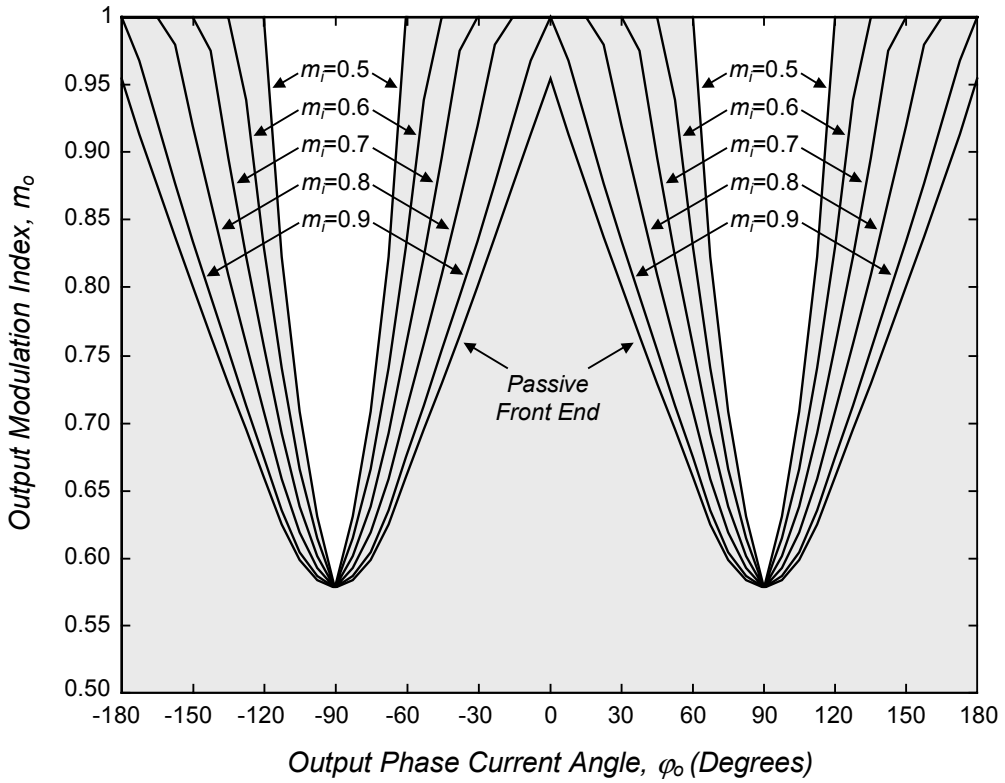


Fig. 6.13. *Limits of the NP current control for constant output current (I_{RMSo}=ct.), unity input PF (φ_i=0°, 180°) and 100% efficiency (η=1).*

The gray area is where balance can be achieved while avoiding any low-frequency harmonic in the NP voltage. This operating area has been greatly extended beyond that which is obtained with either a passive front end, or when a simple three-level converter operates alone.

The best case for the balance is when the input-modulation index is 0.5. However, the input current increases as this modulation index decreases according to (6.21). The knowledge of the output PF in steady-state conditions will define the best input-modulation index for each application. Modulation indices that are lower than m_i=0.5 not only increase the input currents, but also provide less NP current control. For these practical reasons they have not been considered.

The input currents can be larger than the output currents for some operating conditions. This factor should be considered if the converters are built using the same devices, in order to not surpass their maximum current ratings.

The input PF in Fig. 6.13 has been defined to be unity because this situation offers the best conditions for NP balance. However, if consideration were given to the input impedance, which involves the inductance required for the boost rectifier and the utility impedance (Fig. 6.12), the input current would include a small phase displacement. This is because the input currents must be in phase with the utility voltage sources, not with the voltages at the input of the rectifier. Thus, according to the definition given to the input PF for this analysis, it will not be unity, although it will be close to it. Therefore, the limits given in Fig. 6.13 are the maximum theoretical limits for NP balance when the efficiency of the whole system is considered to be 100%.

If a real efficiency value is taken into account, the rectifier can better contribute to the NP balance. This is because the input currents would be higher, and the rectifier could provide more current to the NP. Therefore, the lower the efficiency of the system, the more extended is the balancing operation area; nevertheless, it increases the input currents.

Fig. 6.14 shows the limits of the NP balance versus the DC-link voltage. The lowest curve is determined considering the same output and input voltage amplitudes; hence, the AC voltage specifications of the system are independent of the DC-link voltage. For this curve, both modulations indices are lower than unity, even though the output voltages can be larger taking advantage of raising the DC-link voltage. The upper curve is drawn for the limiting case of unity output modulation index, in which the output voltages are the maximum achievable according to the DC-link voltage. However, despite these benefits, the balancing issue is more difficult then. Some other intermediate curves are also given for different ratios of output and input voltages.

As an example of application, assuming a V_{DC} voltage 40% larger that the input voltage amplitude ($V_{DC} / \hat{V}_i = 1.4$), the minimum $|PF_o|$ for NP balance is 0.437 if the output voltage amplitude is limited to the input voltage amplitude. However, as the output voltage can be 40% larger when m_o=1, the minimum $|PF_o|$ required for NP voltage balance is then 0.837.

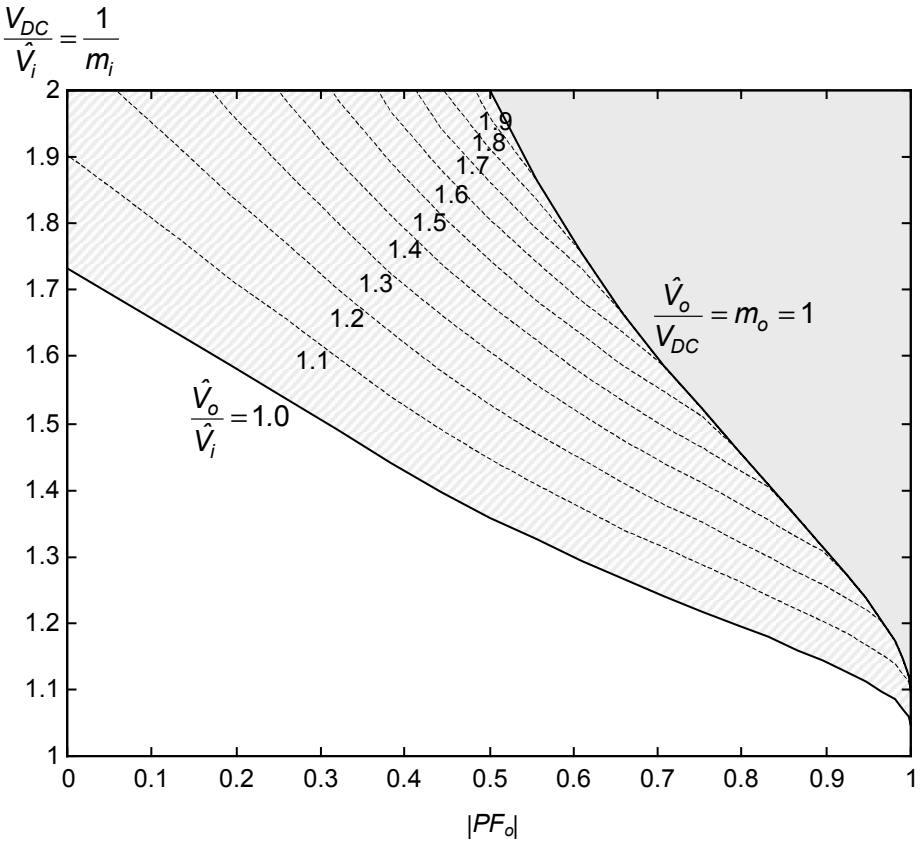
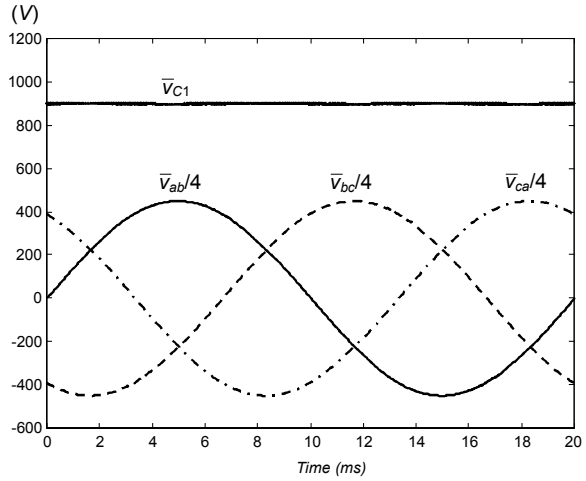


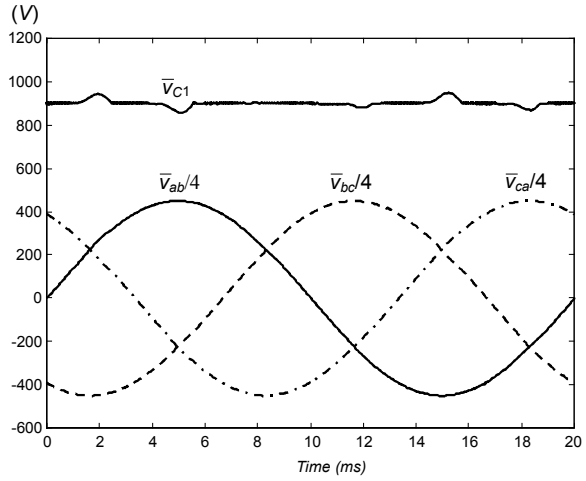
Fig. 6.14. *Limits of the NP balance versus the DC-link voltage.*

The back-to-back connection based on two three-level converters has been modeled by Matlab-Simulink to validate the previous analysis. For this example the reference DC-link voltage is V_{DC}=1800 V, the capacitors C=550 μF, and the RMS output currents I_{RMSo}=400 A with angle φ=-30º, and are provided by AC current sources. The input frequency is 60 Hz and the output frequency is 50 Hz. The output modulation index is fixed to be maximum (m_o=1), so that the worst case is considered for NP balance.

Fig. 6.15 shows the voltage of the lower capacitor (v_{C1}) as well as the AC output line-to-line voltages; all are local averaged variables in order to avoid switching-frequency distortion.



(a)



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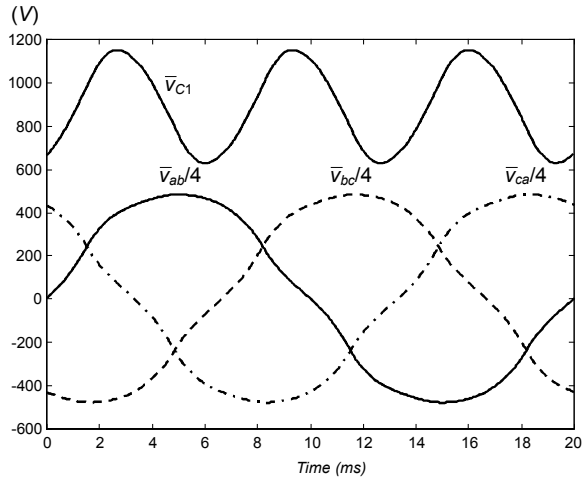


(c)

Fig. 6.15. *Local averaged variables: NP voltage (v_{C1}), and line-to-line output voltages for the case φ_o=-30º: (a) m_i=0.7 and (b) m_i=0.8 with active front end, and (c) m_i=0.8 with passive front end.*

The NP oscillation no longer exists for case *(a)* in this figure. This is because the operation point belongs to the area below the curve m_i=0.7 in Fig. 6.13. On the other

hand, there is a low-frequency ripple for case *(b)*, which is an operating point out of this area.

The ripple is much larger for the case of a passive front end *(c)*, where the rectifier is not providing any current to the NP. Significant low-frequency distortion exists at the output voltages due to this NP voltage oscillation. Additionally, the devices of the converter and capacitors themselves must support nearly 1200 V instead of a voltage value of around 900 V.

Therefore, when there is an active front end, not only can the NP voltage ripple be removed beyond the limits of a single NPC converter, but also when this ripple exists, its amplitude is much smaller.

6.5. Overmodulation

Overmodulation is a special operation mode that involves modulation indices larger than 1. With overmodulation, the fundamental amplitudes in the output voltages can be larger than when operating with linear modulation ($m \leq 1$), but at the price of low-frequency distortion. When the reference vector points outside the hexagon, no set of vectors can generate the reference vector by modulation. This case would result in meaningless negative duty cycles. However, an equivalent reference vector for the output-voltage fundamentals can be obtained outside of the hexagon by settling the reference vector on the boundary (Fig. 6.16).

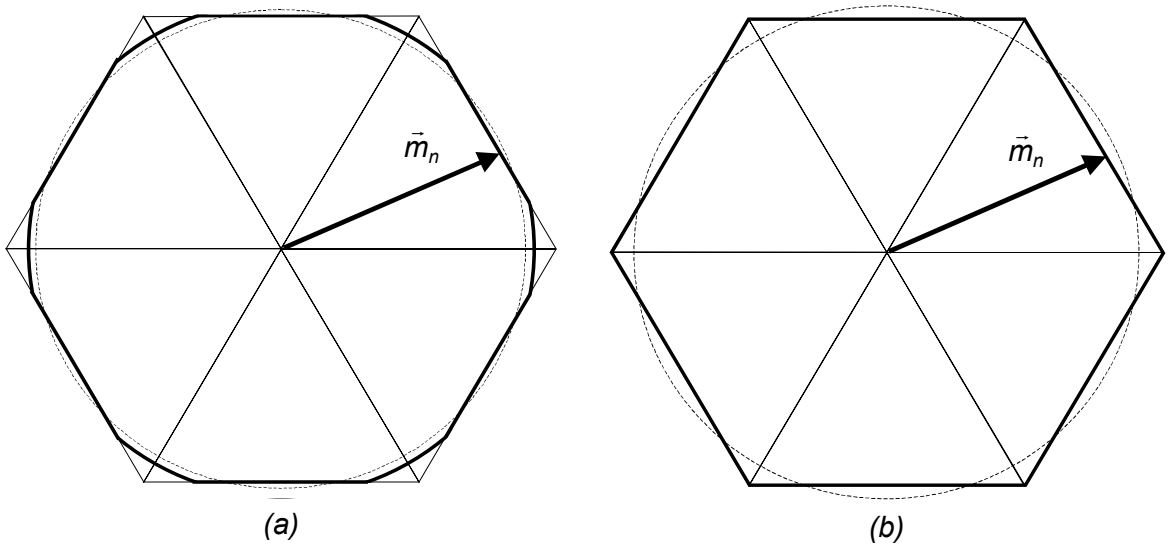


Fig. 6.16. *Examples of overmodulation: (a) general case and (b) maximum amplitude*.

Overmodulation is produced in an n-level converter when the sum of the normalized components of the reference vector reaches:

$$m_1 + m_2 > n - 1; \tag{6.35}$$

then, the following corrections for components m_1 and m_2 must be made:

$$m_{OV1} = \frac{n-1}{m_1 + m_2} m_1, \quad \textit{and} \quad m_{OV2} = \frac{n-1}{m_1 + m_2} m_2. \tag{6.36}$$

The new reference vector preserves the same phase as the original, and, since the condition $m_{OV1} + m_{OV2} = n - 1$ is met, its tip is on the boundary of the hexagon.

Fig. 6.17 shows the benefits of overmodulation. The maximum amplitude of the line-to-line output voltage fundamentals can be up to 4.91% greater than with linear modulation.

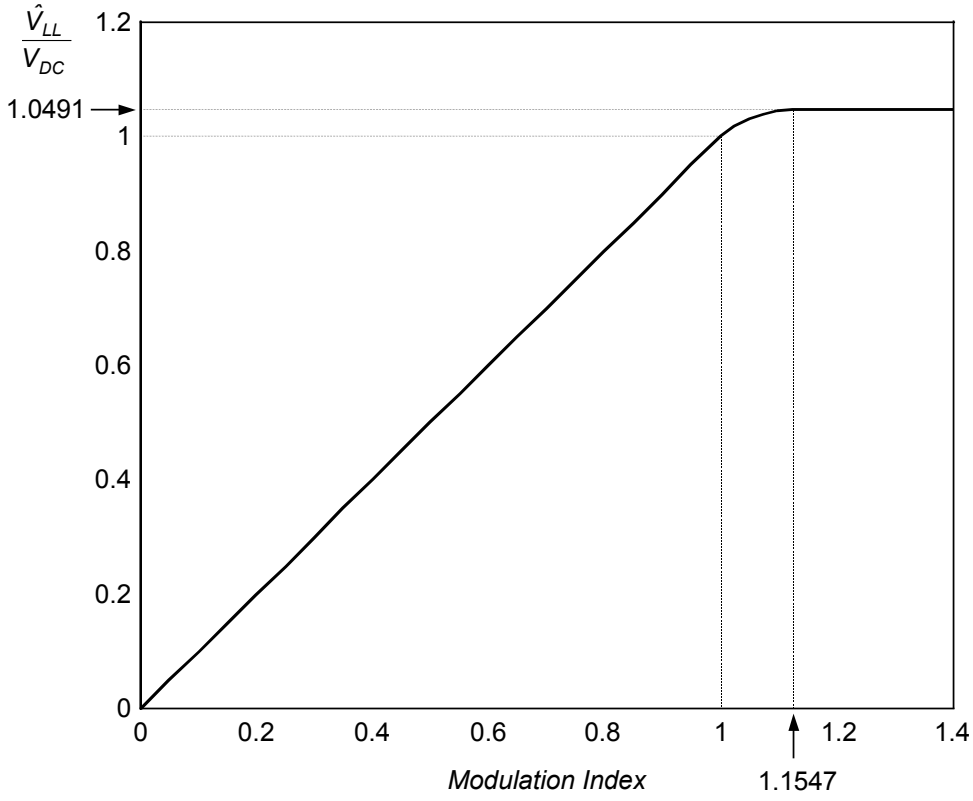
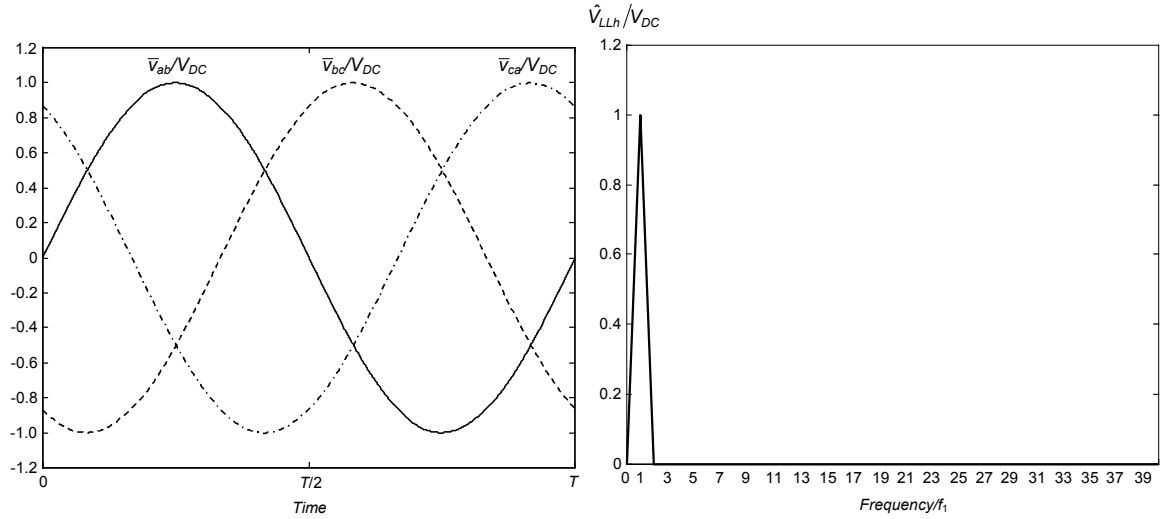


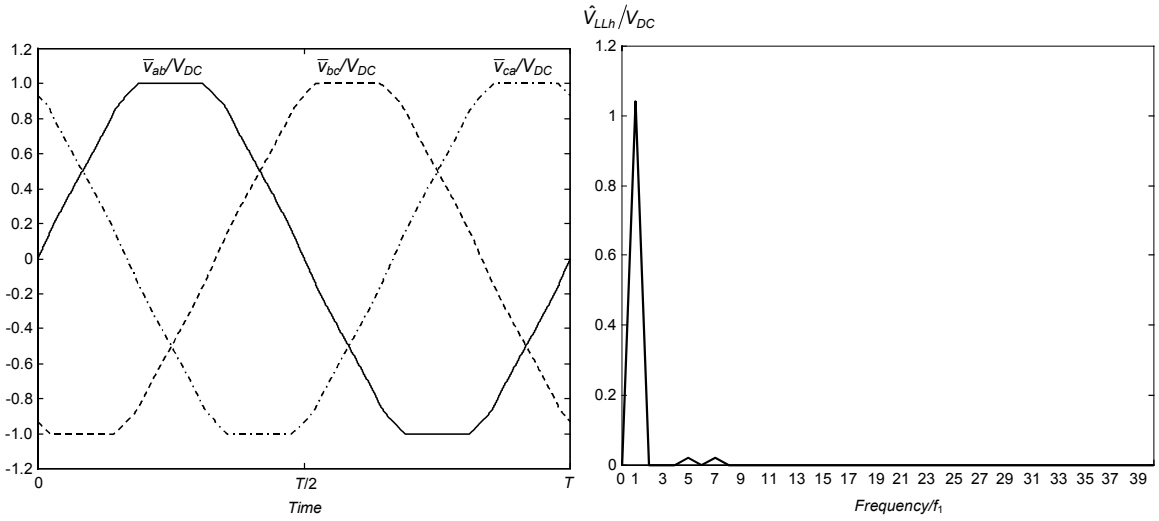
Fig. 6.17. *Amplitude of the output voltage fundamentals versus the modulation index.*

Even though the fundamentals of the output voltages can be larger than when dealing with linear modulation, its amplitude is not proportional to the modulation index. This is why overmodulation is also called nonlinear modulation. However, by adjusting the nonlinear portion of the curve to a polynomial equation or by using a pre-calculated table, this nonlinearity can be compensated for. The worst drawback of overmodulation is the low-frequency distortion that appears in the line-to-line output voltages. Some examples from the three-level converter are presented in Fig. 6.18, in which the waveforms of the voltages are local averaged variables.

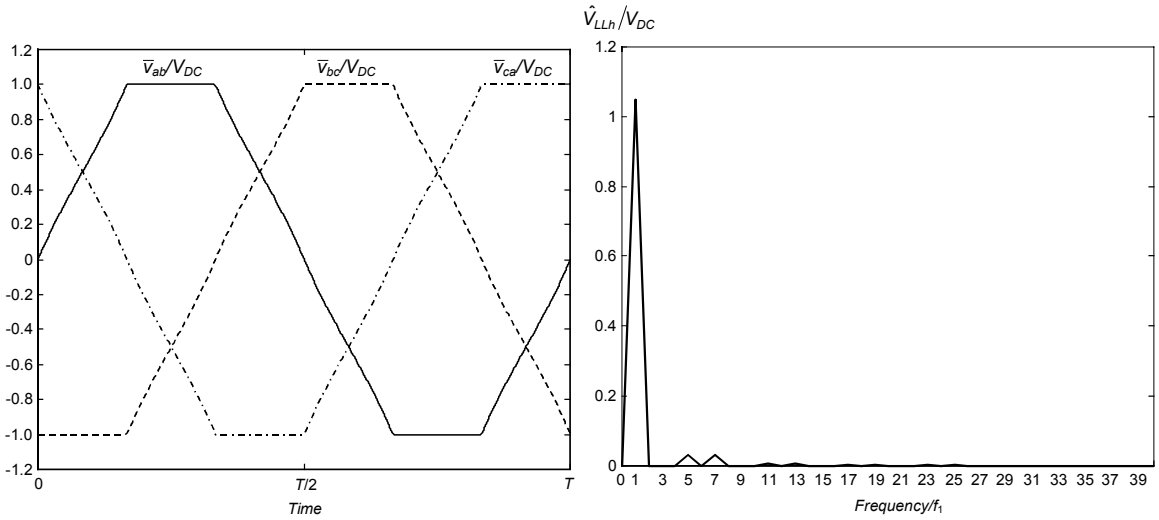
The THD of the output voltages is shown in Fig. 6.19 when operating in the overmodulation range. Since the waveforms have been obtained from the local averaged model, switching frequency distortion has not been considered in the THD calculation. Only low-frequency distortion is included.



(a)



(b)



(c)

Fig. 6.18. *Line-to-line local averaged output voltages and spectra for: (a) m=1; (b) m=1.08; and (c) m≥1.1547.*

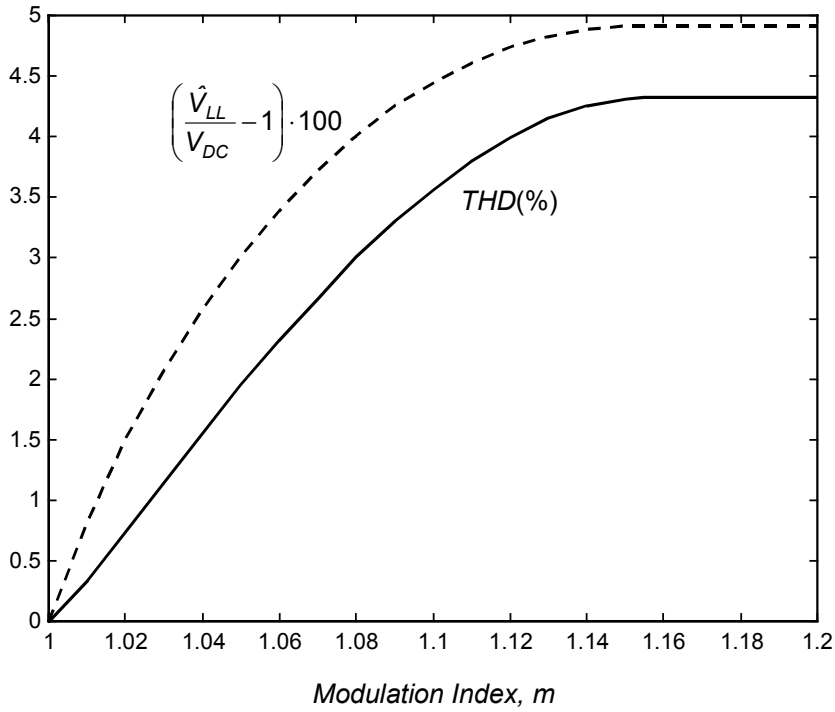


Fig. 6.19. *Low-frequency THD in overmodulation.*

Since the duty cycles of the redundant vectors are very small or even zero during overmodulation, the NP current control margins become insignificant. As a result, overmodulation allows little control over the voltages of the capacitors. In the three-level converter, a large low-frequency oscillation appears in the NP voltage, which eventually increases the low-frequency distortion in the output voltages.

The overmodulation mode discussed in this section is called overmodulation mode I [A53-A55] which can achieve an equivalent modulation index up to 1.0491, independently of the number of levels of the converter. This overmodulation strategy maintains the phase of the reference vector while modifying its length. Overmodulation Mode II, which is based on non-uniform angular velocity of the reference vector, can obtain greater amplitudes of the fundamentals. In this mode, the modified reference vector follows the entire hexagon and changes the phase of the original reference vector. The non-uniform velocity is consequence of holding the reference vector for some time in the positions of the large vectors in the SV diagram. This strategy can achieve modulation indexes up to 1.1027.

6.6. Conclusions of the Chapter

If the values of the DC-link capacitors in the three-level diode-clamped converter are different, the dynamics of the NP voltage do not undergo significant consequences. However, they should not be very different; otherwise their filtering effect on the DC-link voltage will be diminished due to the series connection.

Loading conditions have a profound impact on the design and performance of power converters. In reality imbalances and nonlinearities are quite frequent. The amplitude of the NP-voltage ripple increases when a negative sequence of AC currents exits (linear imbalance). In addition, the frequency of this ripple is the same as the fundamental of the output voltages; thus, requiring large capacitors for attenuation. Nevertheless, no NP voltage instability has been observed when operating with linear imbalances.

Nonlinear loads usually generate an infinite number of current harmonics; thus, evaluation of their effects on the NP balance must be made for each specific case. In general terms, odd-order current harmonics can generate low-frequency oscillations in the NP voltage. Additionally, even-order harmonics can cause the NP voltage to shift. The fourth-order harmonic may produce instability in the NP voltage. The maximum amplitude tolerable of this harmonic superposed to the current fundamentals is described. The analysis shows that modulation indices up to 0.8 guarantee stability of the system in the steady-state condition from the fourth-order harmonic.

Although feedforward modulation can avoid distortion in the AC voltages, the maximum voltages applied to the devices increase due to the low-frequency NP voltage oscillation. Two back-to-back-connected converters can perform a unity-power-factor application with the additional benefit of improving NP voltage balancing. The limits within this connection can remove the low-frequency NP voltage oscillation have been graphically described.

Dealing with components m_1 and m_2, overmodulation can be easily handled in multilevel converters. Overmodulation allows larger amplitudes of the output voltages to be obtained, but at the price of low-frequency distortion. Very low NP voltage control exists when operating in this mode.