Chapter 4.

SPACE-VECTOR MODULATION IN HIGH-ORDER MULTILEVEL CONVERTERS

4.1. Introduction

This chapter deals with diode-clamped multilevel converters with a number of levels larger than three. Compared with the three-level version, the voltage-balancing task is more complicated in these converters. For this reason they have been analyzed in a separated chapter.

Multilevel converters with a large number of levels cannot achieve voltage balance for some operating conditions [A37] that involve large modulation indices and active load currents. In fact, the charge-balancing problem already appears in the four-level converter [A38-A41]. Since the capacitors are either completely charged or discharged for some operating conditions, this circumstance severely limits practical application of these topologies. Nevertheless, a general modulation strategy should be defined in order to obtain good performance of the system for operating points where voltage balance can be achieved. Therefore, the NTV SV-PWM method explained in Chapter 3 is now extended to these converters paying special attention to the voltage balancing issue. The modulation strategy is applied to the four-level converter, in which the voltage-balancing limits are explored.

4.2. Modulation Strategy for High-Order Multilevel Converters

A method of generating modulation in a generic n-level converter is explained in the following. The method follows the same scheme presented for the three-level converter; application of the dq-gh transformation, projection into the first sextant, calculation of duty cycles, selection of redundant vectors and application of vectors in accordance with the original sextant of the reference vector. Since most of the steps are the same as in the three-level converter, the following sections are focused on those which need some particular analysis; i. e., calculation of duty cycles and selection of redundant vectors.

4.2.1. Calculation of Duty Cycles

After normalizing the reference vector by the dq-gh transformation (3.24), the duty cycles of the vectors can be calculated by the method of projections explained in Section 3.1.5. Assuming balanced voltages in the DC-link capacitors, the SV diagram can be divided into triangular regions with unity-length sides. Only two kinds of triangular regions must be considered (Fig. 4.1).

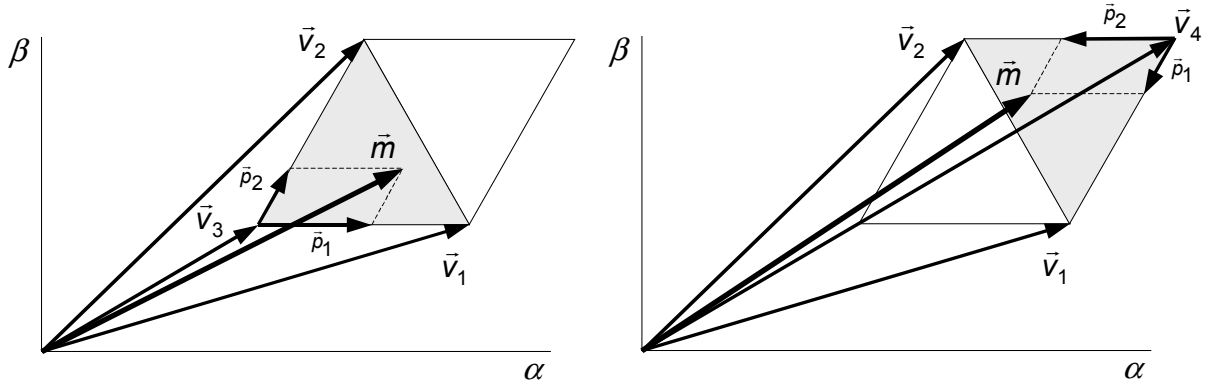

Fig. 4.1. *Possible triangular regions: (a) up triangle and (b) down triangle.*

The length of projections $\vec{p}_1$ and $\vec{p}_2$ are the duty cycles of the vectors $\vec{v}_1$ and $\vec{v}_2$, respectively. The remaining value up to 1 is the duty cycle of either $\vec{v}_3$ or $\vec{v}_4$, depending on the kind of region in which the reference vector lies (up triangle or down triangle, respectively).

Similar processes for calculating duty cycles in multilevel converters are also presented in [A26] and [A27].

4.2.2. Voltage-Balancing Criteria

Two voltage-balancing criteria for selecting redundant vectors in the modulation are analyzed in this section. Both methods are based on minimizing a quadratic parameter that depends on the voltages of the capacitors. The parameter is defined as follows.

The electrical energy stored in the chain of DC-link capacitors (Fig. 4.2) is

$$\varepsilon_C = \frac{1}{2} C \sum_{p=1}^{n-1} v_{Cp}^2 \,. \tag{4.1}$$

Minimization of this energy moves away the voltages of the capacitors from their operating points; hence, a parameter G [A44] is defined as follows:

$$G = \frac{1}{2} C \sum_{p=1}^{n-1} \Delta v_{Cp}^2 \,, \text{ where } \Delta v_{Cp} = v_{Cp} - \frac{V_{DC}}{n-1} \,. \tag{4.2}$$

This quadratic parameter is positively defined and reaches zero when all of the capacitors have the voltage reference $V_{DC}/(n-1)$.

4.2.2.1. Method 1: Derivate Minimization

In order to minimize (4.2), its derivate must be negative or zero, as follows:

$$\frac{dG}{dt} = C \sum_{p=1}^{n-1} \Delta v_{Cp} \frac{dv_{Cp}}{dt} = \sum_{p=1}^{n-1} \Delta v_{Cp} i_{Cp} \le 0 \,. \tag{4.3}$$

The MP currents (i_p) can be calculated by (3.44); thus, the currents in the DC-link capacitors (i_{Cp}) in (4.3) should be related to them. In accordance with Fig. 4.2, and by application of the superposition principle, the currents in the DC-link capacitors can be expressed as follows:

$$i_{Cp} = \sum_{x=1}^{p-1} \frac{x}{n-1} i_x - \sum_{x=p}^{n-2} \frac{n-x-1}{n-1} i_x \,,$$

or

$$i_{Cp} = \frac{1}{n-1} \sum_{x=1}^{n-2} x\, i_x - \sum_{x=p}^{n-2} i_x \,. \tag{4.4}$$

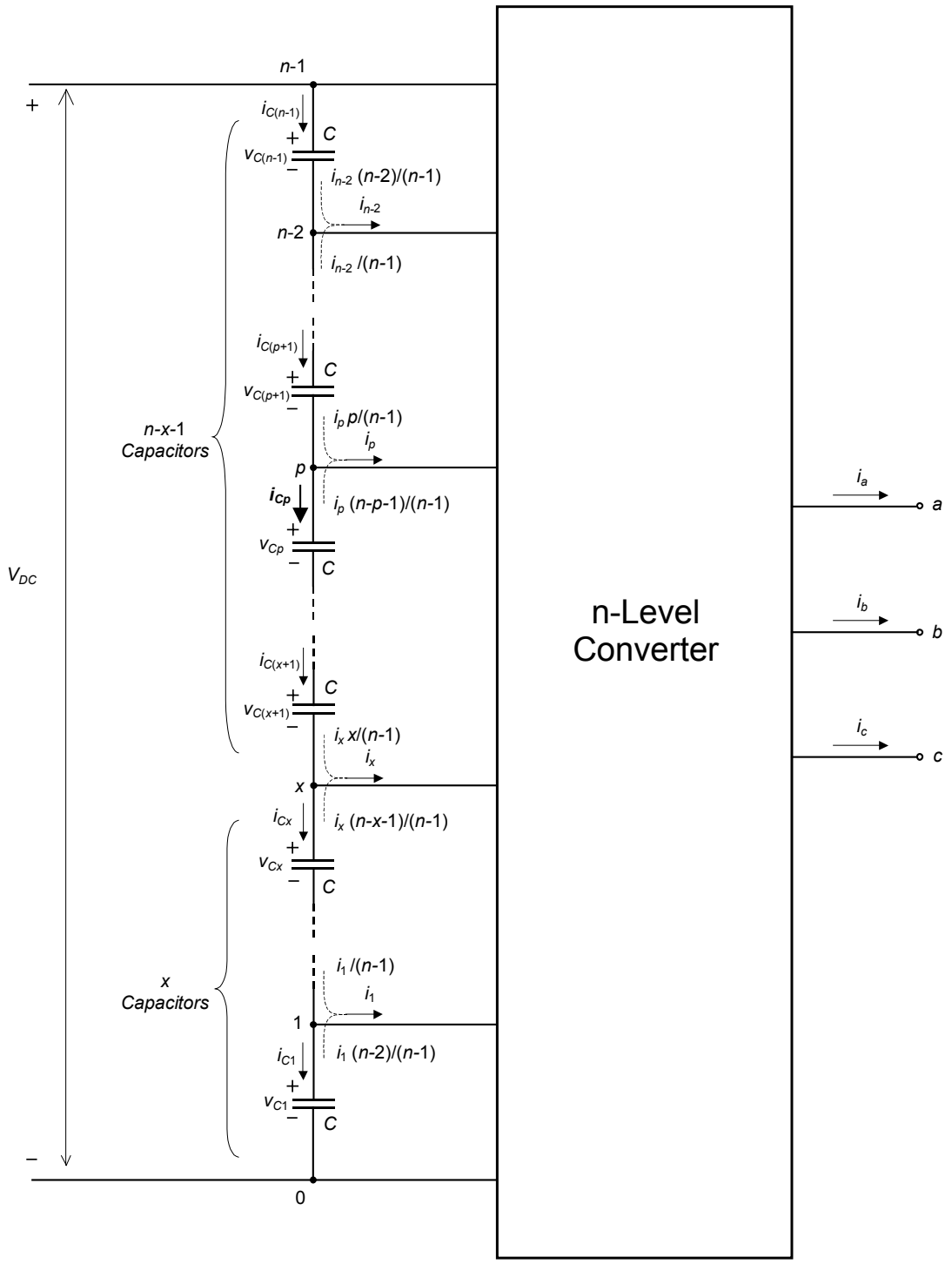

Fig. 4.2. *Distribution of the MP currents in the capacitors.*

The common current through all of the capacitors has not been considered in (4.4) since this current does not affect charge balancing among capacitors; thus, only MP currents are taken into account. Substituting (4.4) into (4.3), the following balancing condition is obtained:

$$\sum_{p=1}^{n-1} \Delta v_{Cp} \left[\sum_{x=1}^{n-2} x\, i_x - (n-1) \sum_{x=p}^{n-2} i_x \right] \leq 0 . \tag{4.5}$$

Taking account of

$$\sum_{p=1}^{n-1} \Delta v_{Cp} = 0 , \tag{4.6}$$

and replacing the voltage of the upper capacitor $\Delta v_{C(n-1)}$ in (4.5) from (4.6), the balancing condition is simplified as follows:

$$\sum_{p=1}^{n-2} \Delta v_{Cp} \left(\sum_{x=p}^{n-2} i_x \right) \geq 0 . \tag{4.7}$$

The discrete local averaging operator can be applied to (4.7), such that

$$\frac{1}{T_m} \int_{kT_m}^{(k+1)T_m} \sum_{p=1}^{n-2} \Delta v_{Cp} \left(\sum_{x=p}^{n-2} i_x \right) dt \geq 0 . \tag{4.8}$$

If T_m is very small when compared with the dynamics of voltages in the DC-link capacitors, these voltages can be assumed to be practically constant during a single modulation period. Therefore, the integral operator will be only applied to the discontinuous MP currents, as follows:

$$\sum_{p=1}^{n-2} \Delta v_{Cp(k)} \left(\sum_{x=p}^{n-2} \frac{1}{T_m} \int_{kT_m}^{(k+1)T_m} i_x dt \right) \geq 0 ,$$

or

$$\sum_{p=1}^{n-2} \Delta v_{Cp(k)} \left(\sum_{x=p}^{n-2} \bar{i}_{x(k)} \right) \geq 0 , \tag{4.9}$$

where $\Delta v_{Cp(k)}$ is the error of the voltages at the beginning of the modulation period *k*, and $\bar{i}_{x(k)}$ is the averaged value of the x-point current calculated over that period. These currents can be determined by (3.44) and used to check different combinations of nearest redundant vectors in order to fulfill that condition. Therefore, the best combination of vectors is such that maximizes the following expression

$$\sum_{p=1}^{n-2} \Delta v_{Cp(k)} \left(\sum_{x=p}^{n-2} \bar{i}_{x(k)} \right) . \tag{4.10}$$

4.2.2.2. Method 2: Direct Minimization

The discrete version of the parameter (4.2) is given as follows:

$$G_{(k)} = \frac{1}{2} C \sum_{p=1}^{n-1} \Delta v_{Cp}{}^{2}{}_{(k)}, \text{ where } \Delta v_{Cp(k)} = v_{Cp(k)} - \frac{V_{DC}}{n-1}. \tag{4.11}$$

The voltages of the DC-link capacitors are sensed at the beginning of a modulation period *k*. They can be extrapolated to the next period by the following equation:

$$v_{Cp(k+1)} = v_{Cp(k)} + \frac{1}{C} \int_{kT_m}^{(k+1)T_m} i_{cp} dt \quad , \tag{4.12}$$

or

$$v_{Cp(k+1)} = v_{Cp(k)} + \frac{T_m}{C} \bar{i}_{cp(k)} . \tag{4.13}$$

Equation (4.13) can be expressed in terms of voltage errors $\Delta v_{Cp} = v_{Cp} - V_{DC}/(n-1)$, as follows:

$$\Delta v_{Cp(k+1)} = \Delta v_{Cp(k)} + \frac{T_m}{C} \bar{i}_{cp(k)} . \tag{4.14}$$

Therefore, $G_{(k+1)}$ is given as

$$G_{(k+1)} = \frac{1}{2} C \sum_{p=1}^{n-1} \Delta v_{Cp(k+1)}^2 = \frac{1}{2} C \sum_{p=1}^{n-1} \left(\Delta v_{Cp(k)} + \frac{T_m}{C} \bar{i}_{cp(k)} \right)^2 . \tag{4.15}$$

Voltage errors in the DC-link capacitors at the beginning of the modulation period k+1 should be minimized during period k; thus, from (4.15) and considering (4.4), the best combination of redundant is the one that minimizes the following expression

$$\sum_{p=1}^{n-1} \left[\Delta v_{Cp(k)} + \frac{T_m}{C} \left(\frac{1}{n-1} \sum_{x=1}^{n-2} x \bar{i}_{x(k)} - \sum_{x=p}^{n-2} \bar{i}_{x(k)} \right) \right]^2 . \tag{4.16}$$

4.2.2.3. Compensating for One-Period Modulation Delay

Either of the expressions (4.10) or (4.16) can be used for selecting redundant vectors from the SV diagram. The voltages and currents involved in these expressions are given for the current period *k*; however, in a practical application, the processor calculates modulation for the next period *k*+1 during period *k*. Therefore, one-cycle delay should be taken into consideration in order to improve voltage

balancing results. Therefore, both of the proposed balancing expressions must be evaluated for period *k*+1, as follows:

$$\max\left\{\sum_{p=1}^{n-2}\Delta v_{Cp(k+1)}\left(\sum_{x=p}^{n-2}\bar{i}_{x(k+1)}\right)\right\} \text{ or} \tag{4.17}$$

$$\min\left\{\sum_{p=1}^{n-1}\left[\Delta v_{Cp(k+1)}+\frac{T_m}{C}\left(\frac{1}{n-1}\sum_{x=1}^{n-2}x\,\bar{i}_{x(k+1)}-\sum_{x=p}^{n-2}\bar{i}_{x(k+1)}\right)\right]^2\right\}. \tag{4.18}$$

The voltages at the beginning of the following modulation period *k*+1 and the averaged currents for that period must be estimated.

The voltages can be extrapolated from period *k* to *k*+1 as follows:

$$\Delta v_{Cp(k+1)}=\Delta v_{Cp(k)}+\frac{T_m}{C}\left[\frac{1}{n-1}\sum_{x=1}^{n-2}x\,\bar{i}_{x(k)}-\sum_{x=p}^{n-2}\bar{i}_{x(k)}\right], \tag{4.19}$$

in which the averaged currents $\bar{i}_{x(k)}$ can be calculated by (3.44), since the duty cycles of the vectors and the AC currents are clearly known during the present modulation period *k*.

Currents $\bar{i}_{x(k+1)}$ in (4.17) and (4.18) can also be determined by (3.44). However, they must be calculated several times for each modulation cycle because of the reiterative process that involves evaluation of nearest redundant vectors.

4.3. The Four-level Converter

The SV-PWM method explained for a generic n-level converter is now applied to the particular case of the four-level converter (Fig. 4.3).

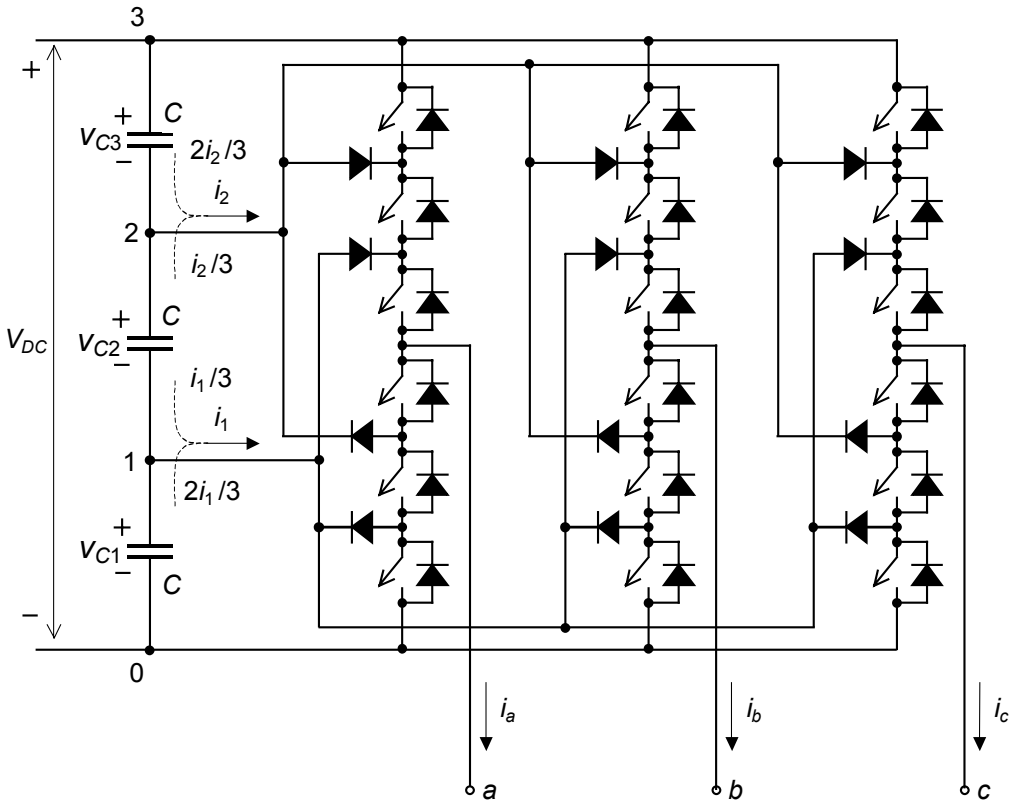

Fig. 4.3. *Distribution of currents in the DC-link capacitors of a four-level converter.*

The vector diagram in Fig. 4.4 is obtained when assuming balanced voltages in the DC-link capacitors. Each sextant of the diagram is divided into nine regions in order to show the vectors nearest to the reference vector.

Although the redundant vectors in the diagram are produced by different states of the converter, they generate the same output line-to-line voltages. However, the currents in the MPs depend on which particular vector is applied from a set of redundant vectors.

The NTV modulation technique uses only one vector from each set of redundant vectors per modulation period. This choice should be made according to the objective of maintaining balanced voltages in the DC-link capacitors, that is to say, minimizing voltage errors in the capacitors quantified by (4.2).

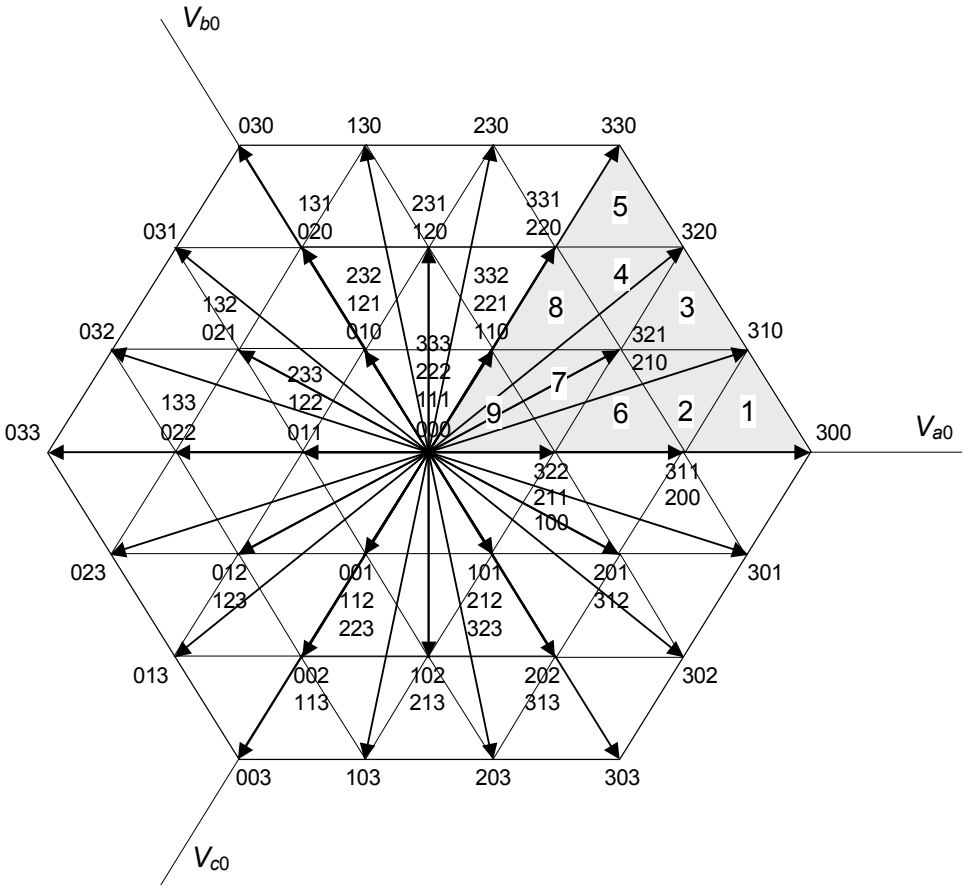

Fig. 4.4. *Four-level vector diagram divided into regions.*

4.3.1. Calculation of Duty Cycles

The dq-gh transformation (3.24) translates the control variables m_d and m_q into gh components (m_g and m_h). Additionally, this transformation normalizes the reference vector to fit into a three-unit-per-side hexagon. Table 3.2 shows the equivalent components in the first sextant (m_1 and m_2) that are used for calculation of duty cycles.

The theoretical maximum amplitude of the normalized reference vector in the four-level converter is the three-unity value. However, in the steady-state condition, its length is limited to 2.5981 ($=3\sqrt{3}/2$) due to the fact that if this vector had a larger amplitude it would be out of the vector-diagram hexagon (Fig. 4.5), and therefore could not be generated by linear modulation.

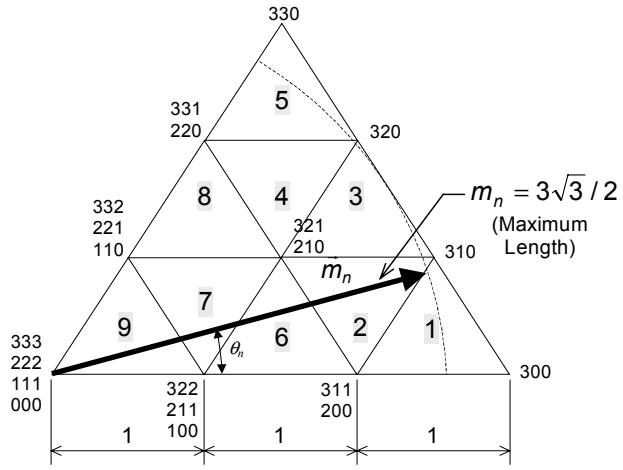

Fig. 4.5. *Maximum amplitude of the normalized reference vector in steady-state conditions.*

If the modulation index m considers values in the interval $m \in [0, 1]$ for linear modulation, the length of the normalized reference vector is:

$$m_n = \frac{3\sqrt{3}}{2} m \qquad \left(0 \le m_n \le \frac{3\sqrt{3}}{2} \right). \tag{4.20}$$

In accordance with the general method revealed in Section 3.1.5, and in the case of a balanced SV diagram (Section 4.2.1), the components m_1 and m_2 define the duty cycles of the vectors. For example, in Fig. 4.6(a) the reference vector lies in Region 6 (up triangle), therefore:

$$d_{200/311} = m_1 - 1, \quad d_{210/321} = m_2, \quad \text{and} \quad d_{100/211/322} = 2 - m_1 - m_2. \tag{4.21}$$

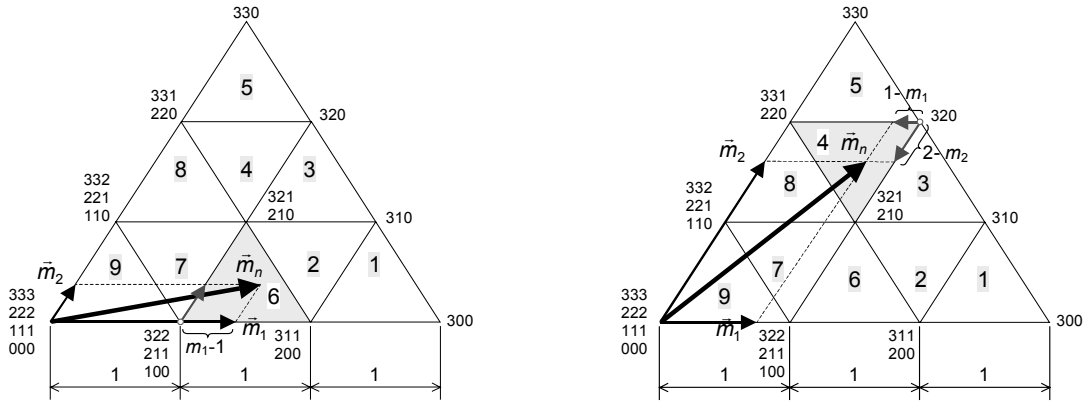

Fig. 4.6. *Examples of reference vector lying in (a) up-triangle region and (b) down-triangle region.*

Fig. 4.6(b) shows the case in which the reference vector is located in Region 4 (down triangle). In this case, the duty cycles of the vectors are:

$$d_{210/321} = 2 - m_2, \quad d_{220/331} = 1 - m_1, \quad \text{and} \quad d_{320} = m_1 + m_2 - 2. \tag{4.22}$$

Table 4.1 summarizes the information needed to calculate duty cycles in the first sextant.

Table 4.1. *Regions and duty cycles of vectors in the first sextant.*

Case	Region	Duty Cycles
$2<m_1\leq 3$ $m_2\leq 1$ $m_1+m_2\leq 3$	1	$d_{200/311}=3-m_1-m_2$ $d_{300}=m_1-2$ $d_{310}=m_2$
$1<m_1\leq 2$ $m_2\leq 1$ $m_1+m_2>2$	2	$d_{310}=m_1+m_2-2$ $d_{200/311}=1-m_2$ $d_{210/321}=2-m_1$
$1<m_1\leq 2$ $1<m_2\leq 2$ $m_1+m_2\leq 3$	3	$d_{210/321}=3-m_1-m_2$ $d_{310}=m_1-1$ $d_{320}=m_2-1$
$m_1\leq 1$ $1<m_2\leq 2$ $m_1+m_2>2$	4	$d_{320}=m_1+m_2-2$ $d_{210/321}=2-m_2$ $d_{220/331}=1-m_1$
$m_1\leq 1$ $2<m_2\leq 3$ $m_1+m_2\leq 3$	5	$d_{220/331}=3-m_1-m_2$ $d_{320}=m_1$ $d_{330}=m_2-2$
$1<m_1\leq 2$ $m_2\leq 1$ $m_1+m_2\leq 2$	6	$d_{100/211/322}=2-m_1-m_2$ $d_{200/311}=m_1-1$ $d_{210/321}=m_2$
$m_1\leq 1$ $m_2\leq 1$ $m_1+m_2>1$	7	$d_{210/321}=m_1+m_2-1$ $d_{100/211/322}=1-m_2$ $d_{110/221/332}=1-m_1$
$m_1\leq 1$ $1<m_2\leq 2$ $m_1+m_2\leq 2$	8	$d_{110/221/332}=2-m_1-m_2$ $d_{210/321}=m_1$ $d_{220/331}=m_2-1$
$m_1\leq 1$ $m_2\leq 1$ $m_1+m_2\leq 1$	9	$d_{111/222}=1-m_1-m_2$ $d_{100/211/322}=m_1$ $d_{110/221/332}=m_2$

For all cases, it is assumed that the sum of m_1 and m_2 is not greater than 3; otherwise, the reference vector would be outside of the hexagon, and thus could not be reproduced by modulation.

4.3.2. Voltage-Balancing Control

Both of the voltage-balancing expressions (4.10) and (4.16) have been checked in the four-level converter. In the particular case of n=4 those expressions become:

$$\max\left\{\Delta v_{C1(k)}\bar{i}_{1(k)}-\Delta v_{C3(k)}\bar{i}_{2(k)}\right\}, \tag{4.23}$$

and

$$\min\left\{\left[\Delta v_{C1(k)}+\frac{T_m}{3C}\left(-2\bar{i}_{1(k)}-\bar{i}_{2(k)}\right)\right]^2+\left[\Delta v_{C2(k)}+\frac{T_m}{3C}\left(\bar{i}_{1(k)}-\bar{i}_{2(k)}\right)\right]^2+\right.$$
$$\left.+\left[\Delta v_{C3(k)}+\frac{T_m}{3C}\left(\bar{i}_{1(k)}+2\bar{i}_{2(k)}\right)\right]^2\right\}. \tag{4.24}$$

In Section 4.3.4, these conditions are used for finding the theoretical limits of voltage balance assuming a very small modulation period ($T_m \to 0$). If the modulation period is not valueless and one-period processing delay is taking into account, (4.23) and (4.24) respectively become

$$\max\left\{\Delta v_{C1(k+1)}\bar{i}_{1(k+1)}-\Delta v_{C3(k+1)}\bar{i}_{2(k+1)}\right\}, \tag{4.25}$$

and

$$\min\left\{\left[\Delta v_{C1(k+1)}+\frac{T_m}{3C}\left(-2\bar{i}_{1(k+1)}-\bar{i}_{2(k+1)}\right)\right]^2+\left[\Delta v_{C2(k+1)}+\frac{T_m}{3C}\left(\bar{i}_{1(k+1)}-\bar{i}_{2(k+1)}\right)\right]^2+\right.$$
$$\left.+\left[\Delta v_{C3(k+1)}+\frac{T_m}{3C}\left(\bar{i}_{1(k+1)}+2\bar{i}_{2(k+1)}\right)\right]^2\right\}, \tag{4.26}$$

in which the voltages in the capacitors at the beginning of the k+1 period can be calculated as follows:

$$\begin{aligned}\Delta v_{C1(k+1)}&=\Delta v_{C1(k)}-\frac{T_m}{3C}\left[2\bar{i}_{1(k)}+\bar{i}_{2(k)}\right],\ \text{and}\\ \Delta v_{C3(k+1)}&=\Delta v_{C3(k)}+\frac{T_m}{3C}\left[\bar{i}_{1(k)}+2\bar{i}_{2(k)}\right].\end{aligned} \tag{4.27}$$

The averaged MP currents in (4.25), (4.26) and (4.27) for periods k and k+1 can be determined by (3.44) that for the four-level converter is:

$$\left[\bar{i}_2 \quad \bar{i}_1\right]^{\mathrm{T}}=\mathbf{D}\,\mathbf{S}_T\,\mathbf{i}_{dq}, \tag{4.28}$$

with $\mathbf{D}=\begin{bmatrix} d_{200}+d_{210}+d_{211}-d_{322} & d_{320}+d_{321} & d_{332}-d_{220}-d_{221} \\ d_{100}-d_{211}-d_{311} & d_{310}+d_{210} & d_{321}+d_{331}+d_{221}-d_{110}\end{bmatrix}$.

4.3.3. Simulated Results

Simulated results are obtained from the four-level converter controlled by the described NTV SV-PWM strategy. For these examples, the converter is supplied by a DC source V_{DC}=1500 V and the output currents are provided by a balanced set of three-phase current sources with RMS value $I_{RMS}=100/\sqrt{2}$ A and a frequency f=50 Hz. The DC-link capacitors are C=1000 μF and the modulation period T_m=0.25 ms (f_m=4 kHz).

Fig. 4.7 shows the voltages of the DC-link capacitors (v_{C1}, v_{C2} and v_{C3}), a line-to-line voltage (v_{ab}) and the output currents (i_a, i_b and i_c) when the converter operates with unity PF. The voltages of the DC-link capacitors tend to be equal when the modulation index is 0.4 and 0.5, whereas the system is unstable for a modulation index of 0.6. Both of the proposed voltage-balancing modulation strategies result in a similar behavior of the converter.

The same variables are presented in Fig. 4.8 when the converter operates with 0.5 inductive PF. In this case, the values given to the modulation index are 0.5, 0.7, and 0.9. Again, the results are almost identical for both voltage-balancing strategies. In this case, the system is unstable for a modulation index of 0.9.

Some observations from the simulated results are:

- the NTV SV-PWM strategy cannot guarantee stability of the system despite optimal selection of redundant vectors,

- when the voltages of the DC-link capacitors are uncontrollable, the middle capacitor is discharged if the energy flux goes from the DC side to the AC side, and it is charged if the flux goes in the opposite direction,

- for modulation indices close to the limits of stability, the voltages of the capacitors are shifted from their operation points, and

- since both voltage-balancing strategies can practically achieve the same results, method 1 (derivate minimization) is preferred because it requires less calculation.

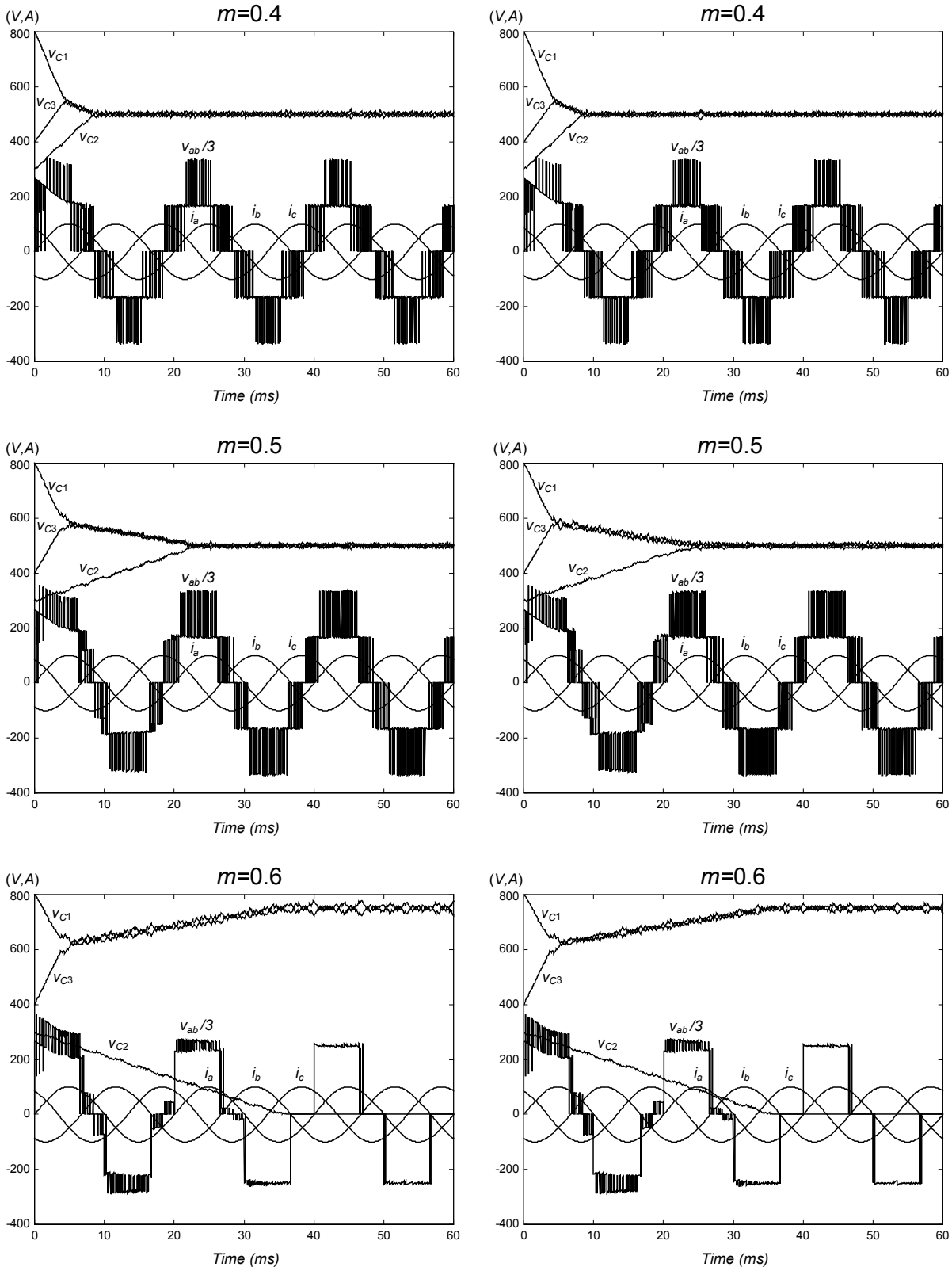

Fig. 4.7. *Analysis of voltage-balancing strategies operating with unity PF.*
Left graphics: method 1 (derivate minimization).
Right graphics: method 2 (direct minimization).

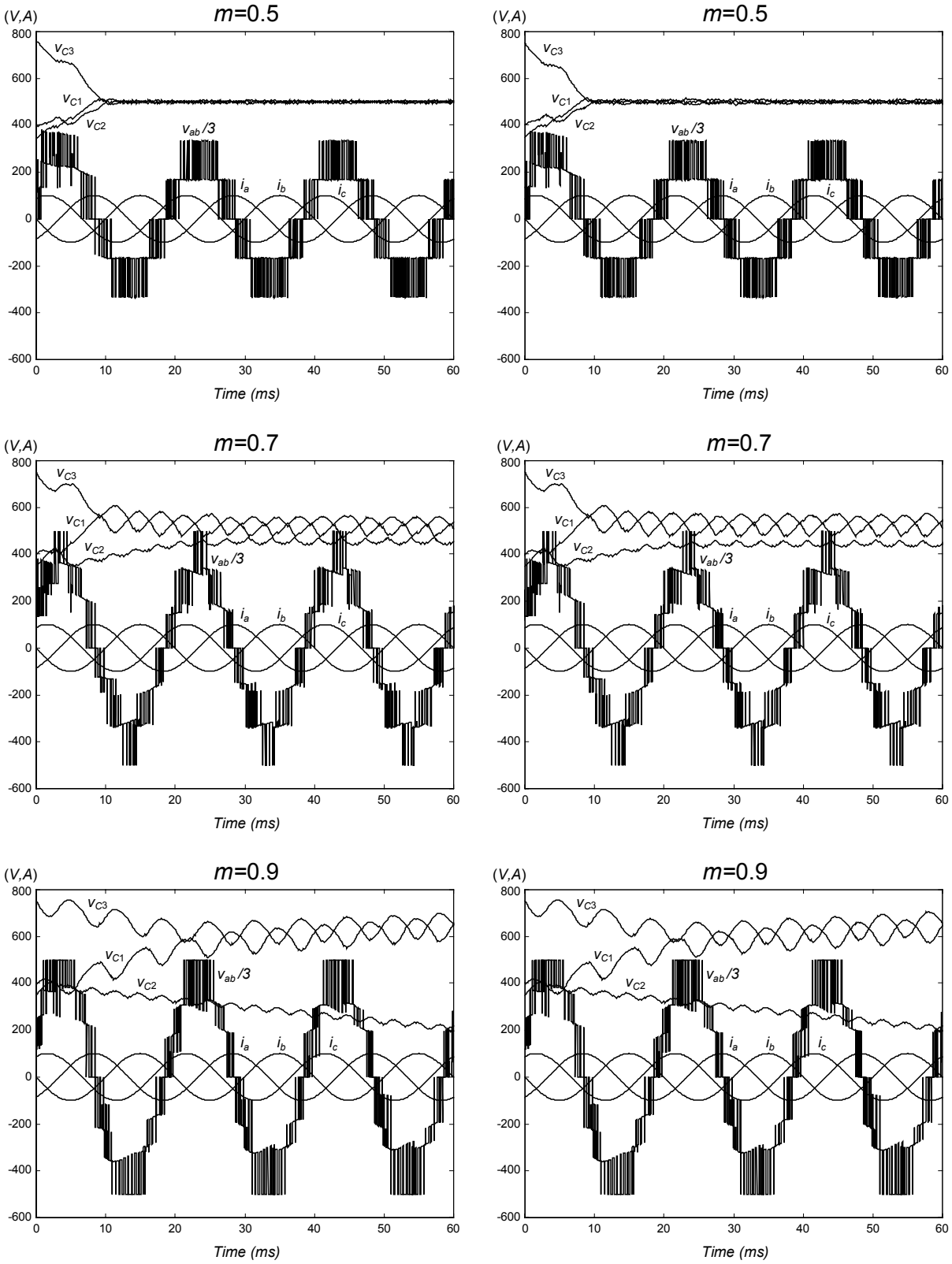

Fig. 4.8. *Analysis of voltage-balancing strategies operating with 0.5 inductive PF.*
Left graphics: method 1 (derivate minimization).
Right graphics: method 2 (direct minimization).

4.3.4. Limits of Voltage Balance

The NTV SV-PWM strategy cannot guarantee stability of the system despite optimal selection of redundant vectors. Fig. 4.9 indicates the limits within which the converter cannot achieve voltage balance. These limits are determined under sinusoidal output currents, and should be understood as theoretical limits, since a very small modulation period is assumed ($T_m \rightarrow 0$). Both of the voltage-balancing strategies have been used in order to verify the limits. Since there is no restriction for the selection of redundant vectors, the best voltage-balancing results are achieved. Any NTV modulation technique based on redundant vectors of the triangular regions cannot achieve voltage balance above the solid line (white area). Nevertheless, this is not an optimal modulation strategy from the standpoint of the switching frequencies of the devices.

A modulation strategy that reduces switching frequencies of the devices is also evaluated in this approach. This strategy only considers adjacent vectors within each sequence. For example, the sequence 100-311-321 is not optimal from the standpoint of switching frequency, since transition from vector 100 to 311 requires more than one leg to switch, and additionally, the phase *a* has to increase two basic voltage levels (this is called a two-step jump). Therefore, this set of vectors should not be available for the modulation. On the contrary, the sequence 100-200-210, for instance, achieves minimum switching frequency because only one leg changes, and therefore, only a single-step jump is required when switching from one vector to the next. Minimization of the number of jumps between consecutive sequences has not been considered, though. This modulation strategy nearly achieves the limits of voltage balancing shown in Fig. 4.9; however, it requires a longer time to stabilize the voltage balance.

On the other hand, Fig. 4.9 also shows in a dashed line the theoretical limits in which the DC-link capacitors cannot achieve voltage balance in multilevel converters with very high order of levels ($n \rightarrow \infty$) [A37]. This boundary is mathematically defined by:

$$m = \frac{\sqrt{3}}{\pi \left|\cos\varphi\right|}. \tag{4.29}$$

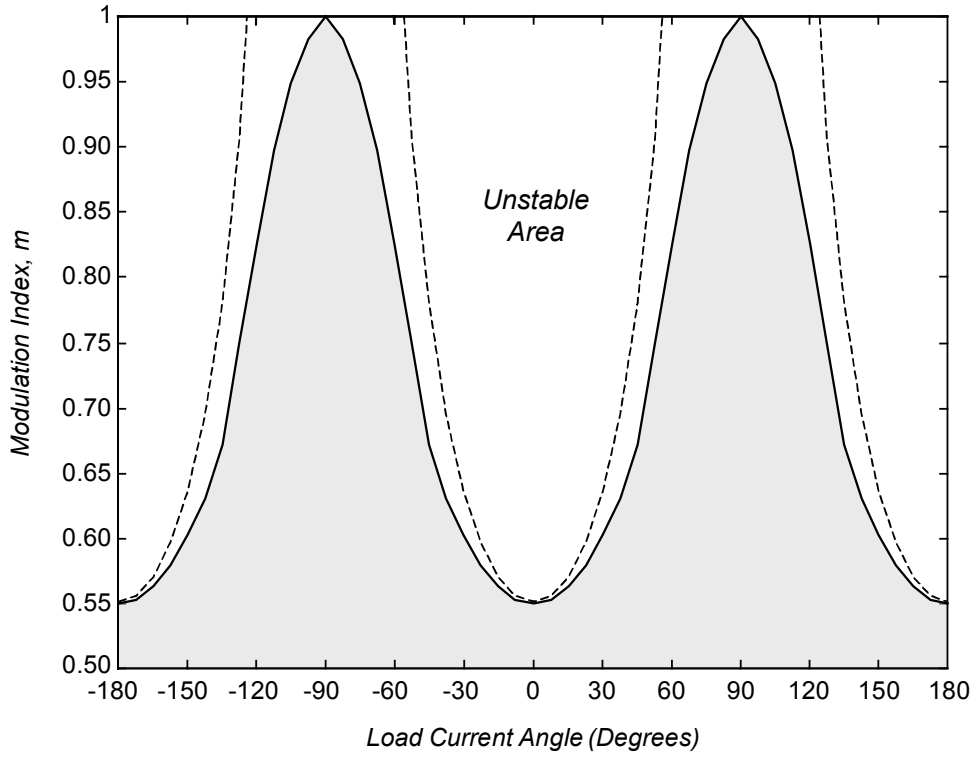

Fig. 4.9. *Limits of voltage balance in the four-level diode-clamped converter.*

4.4. Conclusions of the Chapter

This chapter analyzes SVM for generic n-level multilevel converters. The modulation strategy follows the same scheme as the presented in the three-level converter in Chapter 3. However, the voltage-balancing issue in multilevel converters with more than three levels requires special attention, not only due to the larger number of capacitors, but also because the use of nearest redundant vectors to the reference cannot control balance for some operating conditions. Two balancing strategies have been described, which are based on minimizing a defined quadratic parameter that considers voltage errors in the DC-link capacitors. This parameter is evaluated for each modulation period so that the best sequence of NTV is selected.

The proposed modulation scheme has been verified in the four-level converter. Both of the balancing strategies can achieve the same results and the theoretical limits are found assuming a very small modulation period. The process has no restriction for the selection of redundant vectors. However, this method is not optimal from the standpoint of switching frequencies of the devices. Thus, another strategy that considers only adjacent vectors within the sequences is also evaluated. This low-switching frequency strategy can almost achieve the same limits of charge balance, but it slows down the balancing dynamics of the system.

The results show that multilevel converters with a number of levels larger than three have practical limitations when they are used in applications in which active current components exist. For those cases, voltage balance among capacitors is shown to be impossible if large AC voltages are required; this inhibits the most interesting applications of multilevel converters. They can be considered for cases in which non-active current exists such as with active filtering or static VAR compensation. On the other hand, voltage-balancing improvements can be obtained when two or more converters are connected back-to-back, such as in motor drive applications. Obviously, applications in which the voltages of the capacitors are provided by DC power supplies, or are controlled by auxiliary circuits, release the converter from this task and the modulation strategy can be focused on reducing switching frequencies and improving output voltage spectra.