

Chapter 1.

INTRODUCTION

1.1. Motivation and Objectives

In recent years, there has been a growing interest in power electronics systems. One reason for this is the increasing utilization of electric and electronic equipment, not only for industrial but also for commercial and residential applications. Another reason is the interest in improving the efficiency of systems, besides the expansion of the application of renewable energies. This growing demand has favored the development of new power electronics devices, as well as novel power converter topologies.

For high power applications, voltages and currents must be pushed up. Hence, maximum ratings of power semiconductors become a real handicap. Paralleling devices, subsystems or systems leads to higher current levels. On the other hand, series connections are the solution for dealing with larger voltages. Nevertheless, given a chain of devices connected in series, achieving static and dynamic voltage sharing among switches becomes a problem. The best method for stabilizing voltages applied to the devices is by clamping those using DC voltage sources; or large capacitors, which transitorily behave as voltage sources. Multilevel topologies are based on this principle, and therefore, the voltages applied to the devices can be controlled and limited. An advantage of multilevel converters compared with the classical two-level topology, is that the output voltage spectra are significantly improved due to having a greater availability of voltage levels. Hence, the output voltages can be filtered with smaller reactive components, and additionally, the switching frequencies of the devices can be reduced. These two benefits, together with

the ability to deal with high voltage levels, confer on multilevel converters a very important role in the field of high power applications.

The neutral-point-clamped (NPC) converter was the earliest multilevel topology. Each of the legs of the NPC can provide one additional output voltage level to that of the classical two-level inverter. The neutral-point (NP) voltage, which must be confined to one-half the DC-link voltage, is also available at the AC side of the converter. Since this connection is achieved by clamping diodes, the name given to a generic n -level converter based on this topology is diode-clamped converter.

Nowadays, there are some other multilevel topologies, such as the floating-capacitor converter and the cascade H-bridge converter. The first is based on a bridge structure with series connection of devices, like the diode-clamped converter, but with some capacitors connected between nodes along the connection instead of clamping diodes. The cascade H-bridge converter is based on the connection of basic two-level structures in series.

The diode-clamped converter has become the most used and analyzed multilevel topology so far. Nevertheless, there are still some aspects that require further insight. The main research topics are the design of computationally efficient modulation algorithms, the analysis of voltage balancing in the DC-link capacitors, and the study of control strategies for systems based on this multilevel structure. For these reasons, this dissertation has focused attention on the analysis of this converter.

1.2. Review of Previous Research

In 1980, early interest in multilevel power conversion technology was triggered by the work of Navae et al. [A1] who introduced the NPC topology. It was immediately realized that this new converter had many advantages over the more conventional two-level converter. Subsequently, in the early nineties the concept of the three-level converter was extended further and some new multilevel topologies were proposed.

The floating- or flying-capacitor multilevel converter is a more recent alternative topology where capacitors are used directly to clamp the voltages of the switch-chain nodes. Present interest in the circuit stems from the work of Meynard et al. [A2, A3] in the early 1990s.

The configuration based on cascade H-bridge inverters presents another alternative in the design of multilevel converters. One of the earliest applications of this topology was for plasma stabilization [A4]; and later it was extended to three-phase applications [A5]. The modularity of this multilevel configuration is the main advantage; however, utilization of isolated DC-buses makes this a rather expensive application when active currents are required.

Nowadays, the majority of multilevel high-power practical applications still use the NPC structure. In [A6] two back-to-back-connected NPC converters perform a 10-MVA rolling-mill motor-drive application based on integrated gate-commutated thyristors (IGCTs). Unity power factor (PF) and low harmonic distortion of grid currents are major advantages of this technology compared to cycloconverters. A second example is the drive system used to transport ore from the mine to the concentrator plant in the Los Pelambres copper mine, Chile [A7]. The mine is located at 1,700 meters and the belt conveyor system transports the material downhill. Eight 2.5-MVA motors are driven by NPC converters with gate turn-off thyristors (GTOs). The use of three-level active front ends permits regeneration of energy to the electrical network with nearly unity PF. The system transports 5,800 Tons per hour and generates a total power of 15 MW. A remarkable future project of application of the NPC structure is the Swissmetro [A8, A9] in which some back-to-back connected converters will perform in an 8.5-MVA system to feed synchronous linear motors for propulsion. This underground public transportation will connect the main cities in Switzerland. It is designed for a speed up to 500 km per hour in two tunnels under partial vacuum. The vehicle will move without contact with infrastructure, levitated and guided by electromagnets.

A superconducting magnetic energy storage (SMES) prototype [A10] is also based on three-level converters. This power-processing system consists of a three-level voltage-source inverter and a three-level chopper based on insulated gate bipolar transistors (IGBTs). The inverter of this structure is used for the experimental results of this dissertation and is further explained in Chapter 2.

The modulator stage must determine the gate timings of the power electronic switches. The first NPC modulator scheme was offline calculated to cancel the 5th and 7th harmonics [A1]. Soon after, all the classical modulation strategies applied to the two-level structure were extended to multilevel converters.

Multilevel converters can generate staircase voltage waveforms [A11-A15]. This modulation strategy is equivalent to the six-step operation in the two-level converter; however, the more levels the converter can produce, the closer the output voltages are to sinusoidal waveforms. The main advantage of this modulation strategy is the extremely low switching frequency of the devices, since the modulation period is the same as the line period. Nevertheless, a high number of levels is required for achieving good output voltage spectra and a fast dynamics of the system.

Bang-bang modulators based on controlling maximum current errors have been applied to multilevel converters [A16-A19]. In general terms, these strategies provide fast dynamic response to the system; nevertheless, the switching frequencies of the devices are not constant and reach high values. This is an important consideration for high power applications. For this reason, calculated patterns are preferred.

Sinusoidal pulsewidth modulation (SPWM) is obtained by comparing sine waves with two or more triangular carriers. The number of carriers depends on the number of levels of the converter. A variety of waveforms, sample instants and relative positions of the carriers have been proposed and investigated [A20-A22]. Generally, SPWM techniques obtain very good output voltage spectra because of the symmetry that exists in the process of generating modulation.

The most extended modulation strategies for three-phase multilevel converters are space-vector modulation (SVM) techniques based on PWM (SV-PWM) [A23-A27]. These strategies can achieve larger amplitude of the output voltages than the basic SPWM. Another advantage is that the vector variables of a three-phase load are better controlled with SVM, and, in addition, low switching frequencies can be achieved if optimal sequences of vectors are used [A24].

SVM strategies require long calculations to be made in real time. Therefore, fast modulation algorithms are needed in order to fit the entire processing time within a modulation period, leaving enough time to other tasks such as sensing variables and control calculations. A computationally efficient algorithm is presented in [A26], which takes advantage of translating the reference vector into a non-orthogonal base in the stationary coordinate frame (gh axes). The components of the reference vector in the new base provide useful information for calculating duty cycles of vectors. This algorithm, though, does not apply optimal sequences of vectors for each modulation period, and consequently, non-minimum switching frequencies of the devices are achieved. The algorithm considers the entire SV diagram for carrying out calculations and uses a pointed table for selecting vectors. These two facts make difficult the generation of optimal sequences. On the other hand, a direct transformation from the dq variables given by the controller into the new base may also be useful for speeding up the modulation process.

In the NPC topology, the voltages of the two series-connected DC-link capacitors must be confined to one-half the level of the DC-link voltage to take full benefit of the converter. Springmeier et al. [A28] were some of the early contributors to deal with this balancing problem in 1990, and in [A29] the NP potential variation is analyzed for AC motor drives and static volt-ampere reactive (VAR) compensators.

In general terms, introducing a zero-sequence to the reference voltages can control the NP voltage. In SPWM, this is equivalent to shifting up or down the phase signals of the modulator within a limited interval [A30]. This interval is quite large for low modulation indices, providing sufficient control margin. However, smaller control or even no control exists when dealing with deep modulation indices. In the case of SV-PWM, the redundancy of vectors provides the degree of freedom for NP voltage control [A31]. Similarly to SPWM, voltage balance cannot be achieved when operating with high modulation indices, mainly when a low PF load is connected [A32]. Under such conditions, the averaged value of the NP current calculated over a modulation period cannot be maintained at zero. Therefore, a low-frequency ripple in the NP potential appears, the frequency of which is three times that of the output voltages. This ripple produces low-frequency distortion in the output voltages, and additionally, the devices of the converter have to tolerate larger voltages.

Modulation strategies that do not use the nearest vectors to the reference vector [B5] can withdraw the NP voltage oscillation, but at the price of worsening output

voltage spectra and increasing the switching frequencies of the devices. Hence, these modulation techniques may not be interesting for high power applications.

Assuming the existence of a low-frequency NP voltage oscillation in the three-level structure, a solution for compensating for its effects on the output voltages has been proposed for SPWM [A33]. However, this modulation does not have the benefits of the SV-PWM. In [A34] an SV-PWM approach for obtaining balanced AC-output voltages when the DC-link capacitors have permanent voltage imbalance is presented. This algorithm requires four vectors for each modulation period, and their duty cycles are corrected after being calculated in a balanced SV diagram. The feedforward SV-PWM method proposed in this dissertation and published in [A35] is based on obtaining the duty cycles directly from the unbalanced SV diagram, and therefore requires no subsequent corrections. This process takes advantage of symmetry in the unbalanced diagram to simplify long operations so that the approach can be implemented in a real-time digital processor. Additionally, since only three vectors are used for each modulation period and the sequences of vectors are optimized, the switching frequencies of the devices are reduced.

Even order harmonics in the AC currents have been proven to produce negative effects on the NP balance [A36]. Asymmetric nonlinear loads are the origin of these kinds of harmonics, which may cause instabilities to the NP voltage if they have significant amplitude. This subject requires further insight in order to define critical harmonics and their maximum acceptable amplitudes.

Some contributions tackle modulation in generic n-level converters. The same fast SVM algorithm applied to the three-level converter [A26] is extended to high order converters with insignificant increase of processing time. A similar modulation methodology is presented in [A27]. Both of these strategies are restricted to the calculation of duty cycles and they do not attempt voltage balance.

Balancing voltages of the DC-link capacitors in diode-clamped converters with a number of levels larger than three is a real challenge. Indeed, Marchesoni et al. [A37] have theoretically demonstrated that no balancing strategy does exist that is able to guarantee a correct functioning in all the operating conditions in converters with a large number of levels. Since those conditions include deep modulation indices and high PFs, this inconvenience greatly limits practical application of these converters.

The charge-balancing constraint has already been reported for the four-level converter [A38], in which an auxiliary circuit is proposed to achieve shared voltages among capacitors. The circuit is intended for imbalance compensation when the multilevel converter operates in inverter mode. In such conditions, the voltage of the mid DC-link capacitor tends to steadily decrease. The auxiliary circuit must bring energy from the outer capacitors in order to maintain balance. A similar solution is presented in [A39] in which the auxiliary circuit can manage charge redistribution for bi-directional operation (inverter and rectifier modes) of the multilevel converter. Even though utilization of supplementary circuits can improve the operation of multilevel converters, the devices of these circuits have to handle high current and voltage ratings, sometimes higher than ratings in the devices of the main multilevel converter.

The charge-balancing problem in the four-level converter is also reported in [A40]. Nevertheless, the limits in which this converter cannot achieve voltage balance by using redundant vectors have never been shown. A modified SV-PWM scheme is proposed [A41] which can improve voltage balance. This strategy is applied for large modulation indices, when voltage balance cannot be achieved by standard modulation. Modified regions that do not follow low-switching frequency patterns are used; as a result, the switching frequencies of the devices increase.

Significant balancing improvements can be achieved when two multilevel converters are connected back-to-back [A42-A47]. An optimal controller for voltage balance and power losses reduction in AC/DC/AC converters is proposed [A47]. This general strategy uses, in fact, three different modulation techniques. Defining threshold limits to the application of each of these techniques faces the tradeoff between balancing efficiency and switching losses.

There are several contributions in the area of modeling the NPC converter for controlling purposes. In [A48], the model was developed in the phase switching functions in order to include the dynamics of the split DC-link capacitors. The linear model is obtained by linearizing the averaged model in the rotating coordinate frame around the operating point. Since this model is a multi-input multi-output (MIMO) structure, a state-space treatment is given to the controller. A linear quadratic regulator (LQR) is applied [A49] paying attention to the control of the power flux between the utility and the superconducting coil in an SMES system.

A similar modeling process is presented in [A50], in which a NPC converter operates as a boost rectifier. In this case, however, the control variables of the state-

space model are the coordinates of the reference vector and the NP current rather than duty cycles. Obviously, the modulator stage must translate this information into duty cycles, and eventually, switching functions. If the control variables are accurately applied to the converter, optimal response is expected. Nevertheless, the modulator stage cannot guarantee the NP current reference given by the controller due to its intrinsic nonlinearity. In spite of that, the NP current can be regulated and good general behavior of the system is obtained.

1.3. Major Results

This dissertation provides an insight into modulation and control of multilevel diode-clamped converters. The work is divided into the following major parts:

Chapter 2. Multilevel Topologies. Prototype Description and Modeling.

This chapter is, in essence, an extended introduction that describes and discusses the main multilevel converter topologies. At the same time, it describes the prototype used for the experimental results presented in this dissertation, which is a part of an SMES system. In addition, the diode-clamped multilevel converters are modeled so that commutated and averaged models can be used for simulations. An averaged small-signal model of the three-level converter is described for the design of control loops. Since the task of balancing voltages in the capacitors will be assigned to the modulation stage, the model used for controlling purposes is simplified.

Chapter 3. Space-Vector Modulation.

This chapter begins with some general concepts of SVM. Subsequently, some important contributions are presented in order to achieve efficient SV-PWM algorithms able to be implemented in a digital signal processor (DSP). The dq-gh transformation is used for direct translation from dq components given in the rotating coordinates by the control stage, into gh components in a non-orthogonal stationary frame. An equivalent reference vector in the first sextant is found so that duty-cycle calculation can be directly processed in this sextant. The equivalent vector has the property that interchanging the final states of the phase legs automatically generates the original reference vector. As a result, if the sequences of vectors defined in the first sextant are optimal from the standpoint of switching frequencies, the new sequences in the corresponding sextant will be also optimal. Two modulation strategies for balancing voltages in the DC-link capacitors of the three-level converter are analyzed; NTV modulation and symmetric modulation. These techniques base NP voltage control on proper utilization of redundant vectors, and the sequences of vectors are defined so that minimum switching frequencies in the devices are achieved. The ability for removing the low-frequency NP voltage oscillation is described, and the amplitude of this oscillation is evaluated. Simulated and experimental results are shown for validation of the entire modulation scheme.

Chapter 4. Space-Vector Modulation in High-Order Multilevel Converters.

This chapter explores SVM strategies for diode-clamped converters with a number of levels larger than three. The modulation strategy follows the same scheme presented in Chapter 3 for NTV modulation. The analysis is focused on the voltage-balancing issue, since this is a very difficult task in high-order multilevel converters. Two strategies for selecting redundant vectors in the SV diagram are explained; both of them are based on minimizing a quadratic parameter related with voltage imbalance in the capacitors. Simulated results show similar behavior of the four-level converter for both modulation strategies. As expected, voltage balance cannot be achieved for some operating conditions that involve deep modulation indices and the existence of active currents. The limits in which the four-level converter cannot achieve charge balance by NTV modulation are revealed in this chapter.

Chapter 5. Feedforward Space-Vector PWM.

As a result of the low-frequency oscillation in the NP, the AC output voltages of the three-level converter will contain low-frequency distortion. A new fast feedforward SV-PWM algorithm that can remove distortion in the output voltages is presented. This modulation considers the instantaneous voltages in the capacitors, and the duty ratios are directly calculated from the unbalanced SV diagram. The process takes advantage of symmetry in the unbalanced diagram in order to simplify long operations. The result is a balanced set of three AC output voltages despite NP voltage oscillation or any other cause for imbalance. Simulated and experimental results verify the effectiveness of the feedforward algorithm under static and dynamic imbalances. Furthermore, the maximum time required for processing the algorithm is only 50% longer than in the case of assuming a balanced SV diagram.

Chapter 6. Imbalances and Additional Modulation Issues.

Some additional modulation issues concerning the three-level converter are explored in this chapter. Slightly different values in the DC-link capacitors hardly affect dynamics of the NP voltage. On the other hand, the study of load imbalances reveals that a negative sequence of AC currents (linear imbalance) may produce additional low-frequency NP voltage ripple. Similar consequences are produced by odd-order current harmonics from a nonlinear load, while even-order harmonics can cause the

NP voltage to shift. A positive sequence of fourth-order harmonics may produce instability to the NP voltage. The maximum amplitudes of this harmonic superposed to the current fundamentals that the system can tolerate are described. Simulated and experimental examples are presented for linear imbalances and nonlinear loads. Another important contribution in this chapter is the analysis performed for two back-to-back-connected three-level converters. A bi-directional motor drive application is a practical example, in which one converter operates as a unity-power-factor rectifier and the other as an inverter. Since both converters can share the task of balancing the voltages of the capacitors, the third-order NP voltage oscillation can be removed for an extended operating area. Finally, overmodulation is also addressed in this chapter.

Chapter 7. Optimal Multivariable Control

Some applications of multilevel converters are discussed in this chapter. An LQR with integral actuation is applied to the control of a three-level converter operating as a boost rectifier. Since the task of controlling the NP voltage is assigned to the modulator stage, the simplified model of the converter presented in Chapter 2 is used in the controller. Reduced orders for the matrices are obtained as a consequence. Simulated and experimental results are presented, which show very good behavior of the system.

Chapter 8. Conclusions and Future Research

The main conclusions of this dissertation are summarized in this chapter and some recommendations for future research topics are provided.

