

4.3.2.3.2.3 Layout

Figure 4-41 shows the MARID1 Top layout including the CheckSum and ByteCount parameters which are necessary to validate the design to be fabricated through MOSIS:

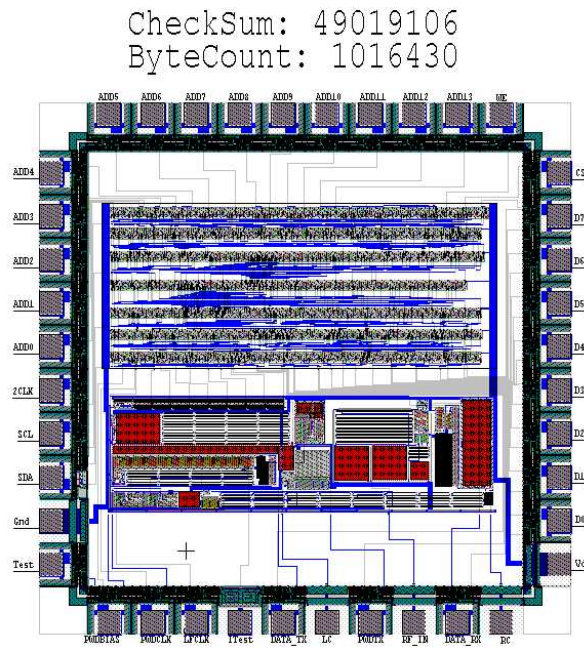


Figure 4-41. MARID2 Top Layout

Overall mask dimensions are $2.2 \times 2.2 \text{mm}^2$ fitting within the maximum dimension of a TinyChip defined within the MOSIS program. In total there were 40 pads: (2) power, (1) analog inputs, (3) analog outputs, (3) digital inputs, (17) digital outputs (13) digital IO and (1) I2Cpad.

4.3.2.4 RESULTS

The results of this system will be shown in two levels. First the experimental results of the designed circuits at IC level, without including the telemetry modules already presented in previous chapters. Second, at prototype board level with all the components, an “in-vitro” test using a real ISE sensor (see introduction section 4.3.1.1) will be presented and the data will be analyzed.

4.3.2.4.1 ASICs test

The chips were fabricated and tested with very successful results. Figure 4-42 and 4-43 show a photograph of both ASICs, fabricated with AMI technology through the MOSIS program:

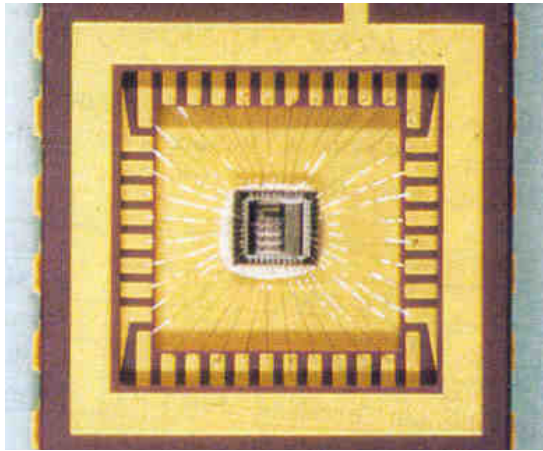


Figure 4-42. MARID1 photograph

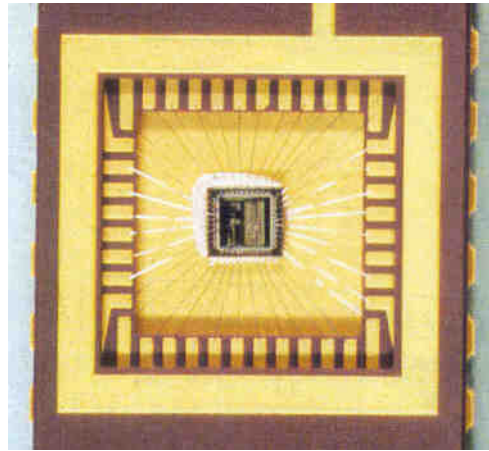


Figure 4-43. MARID2 photograph

4.3.2.4.2. "In-vitro" board-level results

The two custom chips, the memory chip, the PIC controller a coil and a battery are all the components of the system. Next picture shows a photograph of the prototype board.

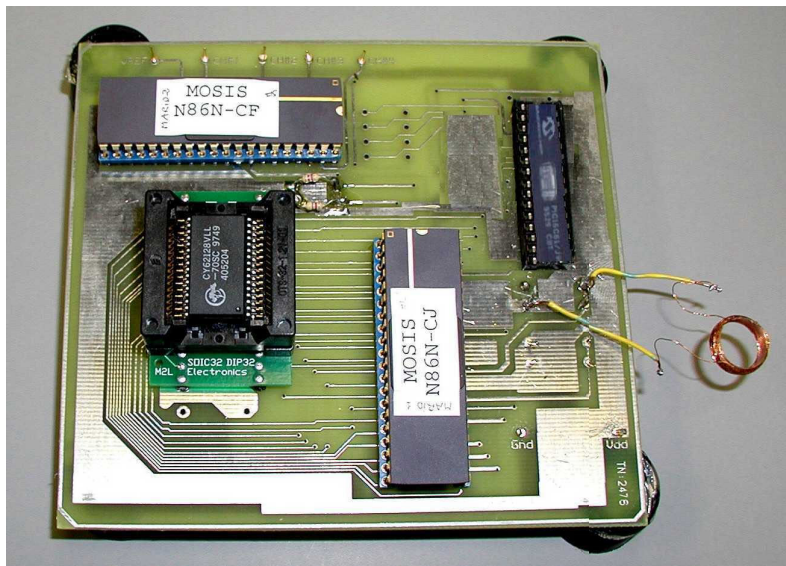


Figure 4-44. MARID implant system prototype board

External boards to verify the telemetry link were also build. The design is described in section 3.2.1.2.2 for the transmitter and in section 3.2.2.2.2 for the receiver. Next photograph shows a prototype board of the complete external reader:

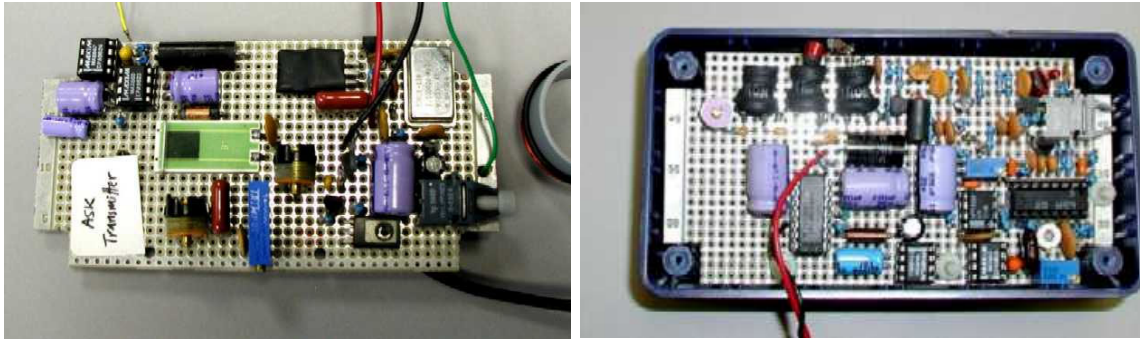


Figure 4-45. External reader with Transmitter board (left) and receiver board (right)

The system provided full functionality. The main validated functional specifications were:

➔Functional Downlink: Communication from the external reader to the implant was established with very low Bit Error Rate (BER) up to 5cm using a 1MHz OOK modulated field. The I2C interface with the PIC controller was fully functional.

➔Functional Uplink: Communication from the implant to the external reader was established with low BER for shorter distances than the Downlink (up to 1cm). The VCO + modulator scheme proved to be fully functional with a range of programmability between 13 to 36MHz. The I2C interface with the PIC controller was fully functional.

➔Functional Memory reading: The SRAM to PIC reading interface through I2C bus was fully functional.

➔Functional Memory reading: The PIC to SRAM writing interface through I2C bus was fully functional.

►►Functional analog front-end: The four channel analog front-end circuits were fully functional. That included very high impedance, programmable gain and adjustable DC offset. The interface with the PIC AD converter was fully functional.

Once all modules were validated, an “in-vitro” test interfacing the circuits with an ISE sensor was performed. Figure 4-19 (section 4.3.1.1) shows a photograph of the potassium ion-selective electrode sensor used in the experiments. A group of four sensors were connected to the respective inputs, and measurements were made through the system in test solutions of potassium chloride that had known potassium activity. In total six different solutions with different known concentration of K^+ (potassium ion) were obtained to validate the sensor interface. Data was recorded through the MARID board with the established protocol going from the high-impedance amplifier, AD converter, and sent through the I2C bus to the telemetry module that transmits to the external reader the recorded information. Table 4-6 shows the recorded values for different K^+ solutions for a particular channel.

Table 4-6. “In-vitro” MARID recordings

Solution #	Log Ak ⁺	MEAS#1	MEAS#1	MEAS#1	MARID (mV)	STDEV (mV)
1	-0.7024	64.72	65.68	65.76	65.39	0.58
2	-1.2609	39.12	39.92	38.32	39.12	0.80
3	-1.5454	20.64	20.56	18.40	19.87	1.27
4	-2.0399	-7.44	-7.68	-8.56	-7.89	0.59
5	-2.5164	-36.08	-30.80	-34.72	-33.87	2.74
6	-3.0835	-63.36	-60.08	-59.04	-60.83	2.25

The same procedure was repeated, now using a standard instrumentation device used routinely to validate sensor technology (ORION) instead of using the MARID electronics. Next graph (figure 4-46) shows the results of both instruments. We see undistinguishable results.

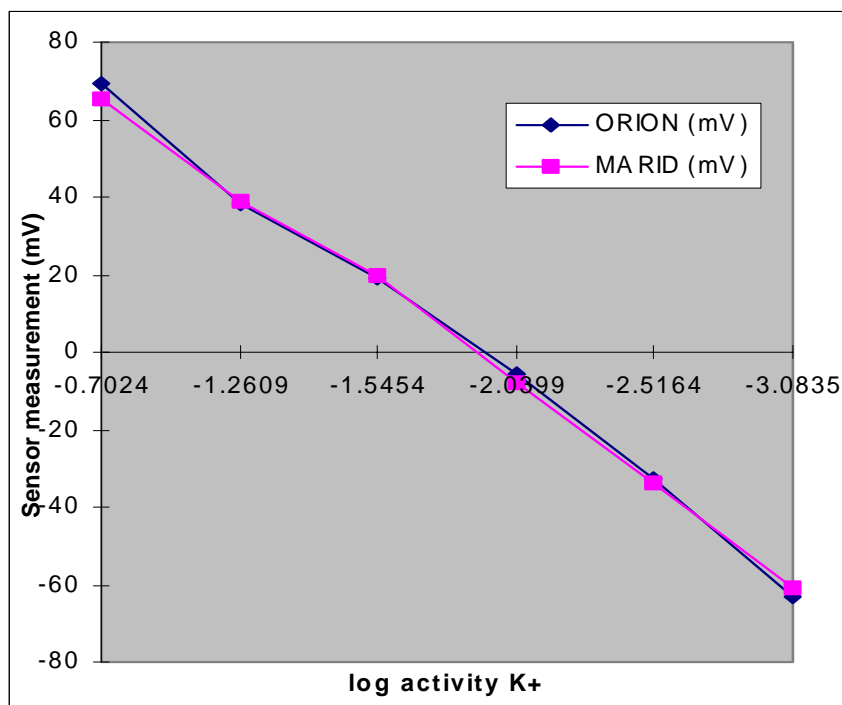


Figure 4-46. MARID device versus standard ORION instrument

From these results the log activity of potassium versus input voltage was extracted. We see a fairly linear response typical of the Nernstian region (see section 4.3.1.1) with a measured slope in the central region of 57.64 mV/logAK⁺ and a standard error of 1.21 mV/logAK⁺. This corresponds quite well with the theoretical value of 59 mV/logAK⁺ at 25 degree C^[8].

4.4 GENERAL PURPOSE TELEMETRY CHIP

So far two system level demonstrators have been exposed. The Pressure sensor ITUBR project with a complete system development all the way down to obtain a functional implantable device reporting “in-vivo” results and the chemical sensor MARID project with results involving board prototype with “in-vitro” sensor testing. The following system is actually a single chip so called TIC (Telemetry Integrated Circuit). The development effort was much smaller than the former systems. The main concept was to re-use the know-how and pieces of telemetry design done, to have a versatile

general purpose IC solution to provide RF energy and bi-directional data to any batteryless implant.

4.4.1 Introduction

The National Center of Microelectronics (CNM) of Spain, and in particular the Biomedical Applications Group (GAB) as part of an R&D public funded organization within the CSIC (Consejo Superior de Investigaciones Cientificas) is striving to combine research and outsource funding. Following this line of thought, after acquiring an important know-how in the field of bio-telemetry implants (thanks mainly to the development of the European project ITUBR) the possibility of re-using existing designs into a customized ASIC to provide a data and energy solution for any battery-less implant became clear to the candidate as a market-driven integrated circuit. This section describes the design of a single chip, called TIC (Telemetry Integrated Circuit) developed within the GAB-CNM with internal funding. What is described here is the first generation of TIC (TICv1.0). Later other researchers did further corrections and refinements to the chip. The work presented in this section will be related to the first generation of TIC chips.

4.4.2 System design and development

The intend behind the design of the TICs chip was to create a telemetry platform, easily adaptable to almost any implant system that had a micro-controller on board. So any research center or company interested in implantable batteryless and wireless devices would not require a big development effort to build in a short-time and cost-effective manner an implantable device.

4.4.2.1 Architecture

The Telemetry Integrated Circuit (TIC) will be designed to either interface by means of a wireless energy and data link with the external world (external controller like

the one developed in chapter three) or with several on-board chips capable of supporting the standard interface that the TIC provides. Figure 4-47 shows an interface diagram of the TIC chip.

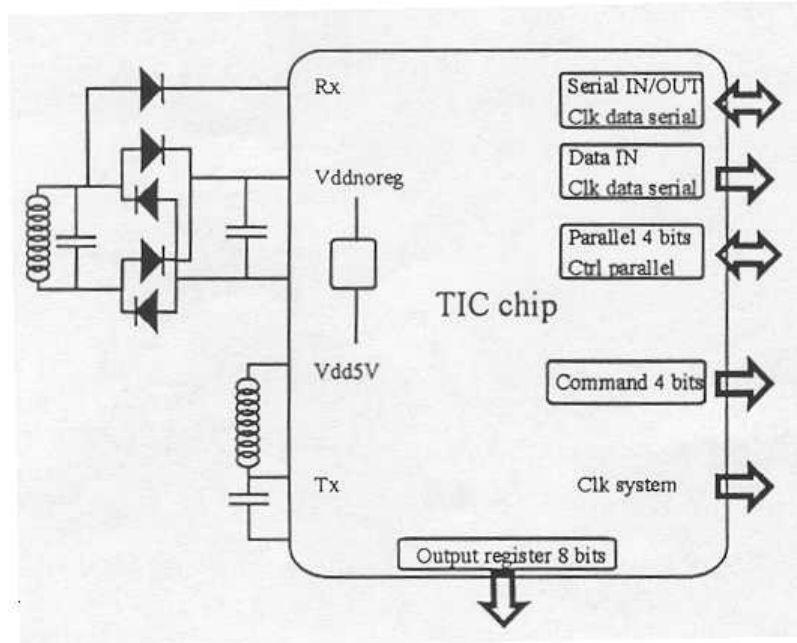


Figure 4-47. Interface diagram of a TIC chip

A key concept is that the TIC chip is mainly another peripheral, slave of the master controller (see MARID architecture chapter four section 4.3.2.2). So the data flow and directionality is entirely controlled by the processor (preferably a PIC micro-controller) with a high-level interface. Therefore the controller is relieved of detailed telemetry tasks, with the possibility of full dedication to the rest of the system needs. The protocol was mostly designed to interface with a PIC microchip controller or similar. We used in the prototype development a PIC16C71.

As we can see in Figure 4-47 the main interface with the micro-controller (PIC) was a 4-bit parallel port. But additional interfaces were added to the chip to increase the flexibility and possible configurations. In that line there is a serial bi-directional port, a 8-bit parallel output port and finally a 4-bit output command port. Table 4-7 summarizes the multiple data interfaces that were implemented.

Table 4-7. TIC system Data interface

Description of the interface	Data flow
8 bits from ETU to PIC (4+4) using a 4-bit parallel bus	ETU \Rightarrow TIC \Rightarrow PIC
4 bits command to program other circuitry	PIC \Rightarrow TIC \Rightarrow 4bits Command
8 bits (4+4) from PIC to ETU	PIC \Rightarrow TIC \Rightarrow ETU
8 bits parallel bus (to control other devices, i.e. DACs)	PIC \Rightarrow TIC \Rightarrow 8bits Output
Single serial port to send data to ETU	Serial \Rightarrow TIC \Rightarrow ETU
8 bits from ETU to PIC using a serial bus	ETU \Rightarrow TIC \Rightarrow Serial

The chip also had a build-in oscillator that not only was used in the telemetry part but also could be a source of external clocking for the controller. Details on the implementation will be presented in next section. In addition to that, the communication protocol includes an acknowledge response that feeds-back to the external controller information on the induced secondary voltage (B-field). This circuit (described in chapter two section 2.3.4.1) makes possible the minimization of the field that the external controller must generate to send the proper energy to the implant.

4.4.2.2 ASIC design

The TIC chip was divided in three main blocks. The wireless data interface (telemetry block), the energy management interface (energy block) and the micro-controller interface (digital block). Figure 4-48 shows of the block diagram of the chip.

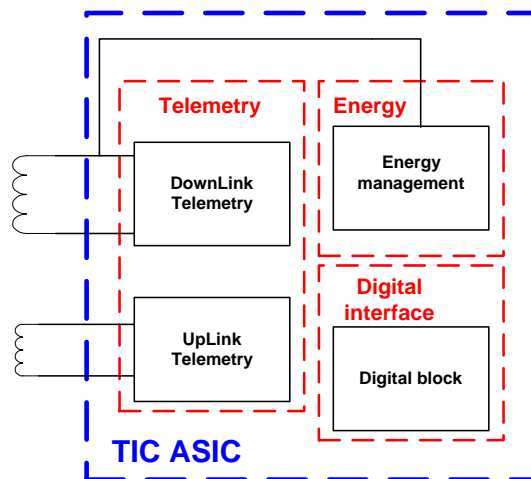


Figure 4-48. TIC block diagram

4.4.2.2.1 Telemetry block

As mentioned in the TIC system introduction, the driving concept was to re-use existing telemetry circuits implemented in other projects. In fact the telemetry block of the TIC contained all circuits described in the batteryless system chapter three. Due to the intrinsic flexible nature of the concept here developed, several Uplink schemes (that had been investigated before) were included in the chip. Among them, BPSK modulators with different drive capabilities (see chapter 3 section 3.2.2.2.1.3), OOK modulator (see chapter three section 3.2.2.3.1) and also a LC modulator (see chapter three section 3.2.2.3.2). The Downlink scheme had only one possible modulation: Amplitude Shift Keying –ASK (see chapter three, section 3.2.1.1).

4.4.2.2.2 Energy block

Again following the telemetry example most of the energy management circuits were identical to the ones described for the RF-powered application (chapter two). That also includes the feedback circuit to regulate the magnetic field generated by the external unit (see chapter two section 2.3.4.1).

4.4.2.2.3 Digital block

The digital interface to an embedded controller (described in the architecture section) was implemented linking the external unit with the master implant. Described bellow the communication protocols between the TIC with the external unit (ETU) and with the micro-controller (PIC), as well as with a general-purpose application unit (AU).

i) Start sequence:

Before any data transaction occurs, the TIC must be configured for a certain interface architecture, data transaction speed and output clock. In order to do so, five bits

following a hard-coded global reset define the directionality of the serial port, the Uplink bit-rate and the frequency of the clock supplied to the controller. The startup sequence is as shown in figure 4-49.

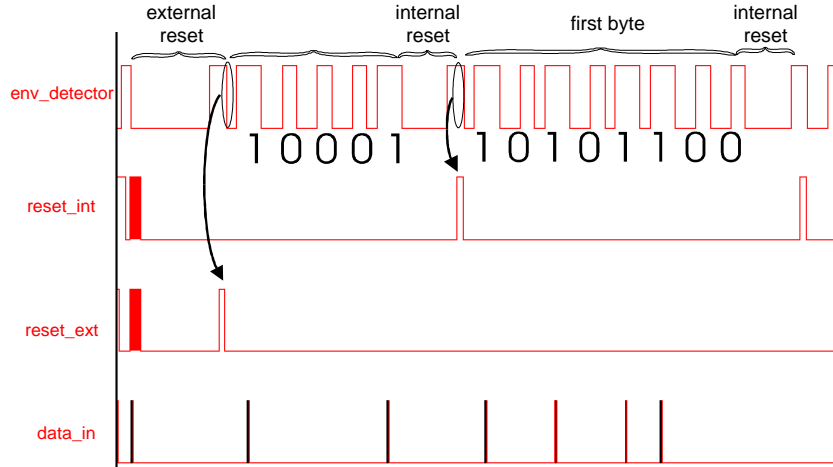


Figure 4-49. Startup sequence

There is global reset (ext_reset), which resets all the internal memories. The next five bits programs the chip. First bit (**bit1**) is *serialIO* which controls the directionality of the *serial* pad. Bit1='1' means serial line in output mode (read). Second bit (**bit2**) is *coderCK*, which codifies the OutLink bit-rate. If bit2='0' then 234kbps. If bit2='1' then 468kbps. The last three bits set the output clock supplied to the controller (see table 4-8).

Table 4-8. Output Clock programmability

CLK	bit3	bit4	bit5
234kHz	0	0	0
468kHz	0	0	1
3.75MHz	0	1	0
7.5MHz	0	1	1
7.5MHz	1	0	0

ii) Data flow sequence

Data flow is codified through the use of three bits: CS1, CS2 and bit1(serialIO). (See table 4-9). CS1 and CS2 are lines provided by the PIC. The PIC must have a reset startup to set these lines to low. Bit1 is sent during the TIC programmability (after

external reset decoder). It cannot be reprogrammed excepted by sending a new external reset.

Table 4-9. Data flow programmability

CS1	CS2	bit1	Data flow
0	0	X	ETU ⇒ TIC ⇒ PIC
0	1	X	PIC ⇒ TIC ⇒ 4bits Command
1	0	X	PIC ⇒ TIC ⇒ ETU
1	1	X	PIC ⇒ TIC ⇒ 8bits Output
X	X	0	Serial ⇒ TIC ⇒ ETU
X	X	1	ETU ⇒ TIC ⇒ Serial

ETU ⇒ TIC ⇒ PIC

The ETU to PIC data transference is codified by CS1=CS2='0'. The inter-medium TIC-PIC transference is a 4bits parallel interface (P1 to P4) controlled by *IOctrl* line. The 4bits parallel data transference is synchronized by *ctrl_parallel*. At every positive edge of *ctrl_parallel* the P1 to P4 lines can make the data transference to the PIC. Figure 4-50 shows an ETU to TIC to PIC data transference.

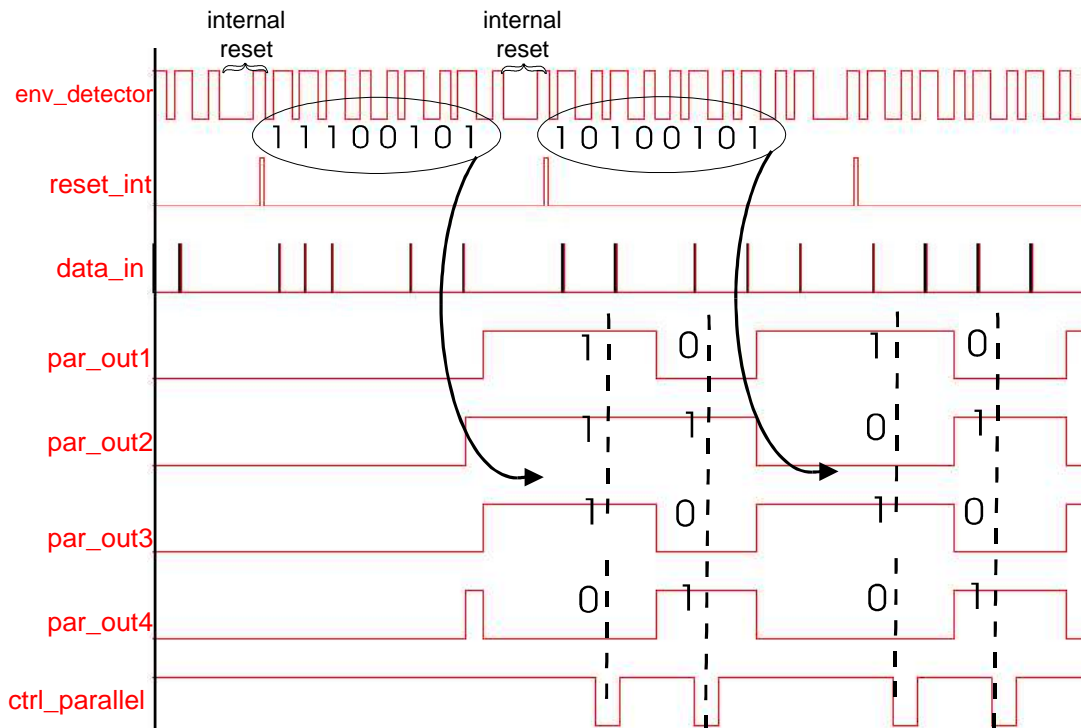


Figure 4-50. ETU to PIC data transference

PIC ⇒ TIC ⇒ 4bits Command

This 4bits data transference is used to interface a general purpose Application Unit (AU). Depending on the AU design this interface could be ignored. The data going to the AU is clocked by *busCK* which is directly sent by the PIC. There is no sense to use this interface without the PIC.

PIC ⇒ TIC ⇒ ETU

Through the 4bits line interfacing the PIC with the TIC data can be sent to the outside. PIC to TIC data is sent as usual (see figure 4-51). Then a parallel to serial conversion places the data (after codification) to the on-chip transmitter.

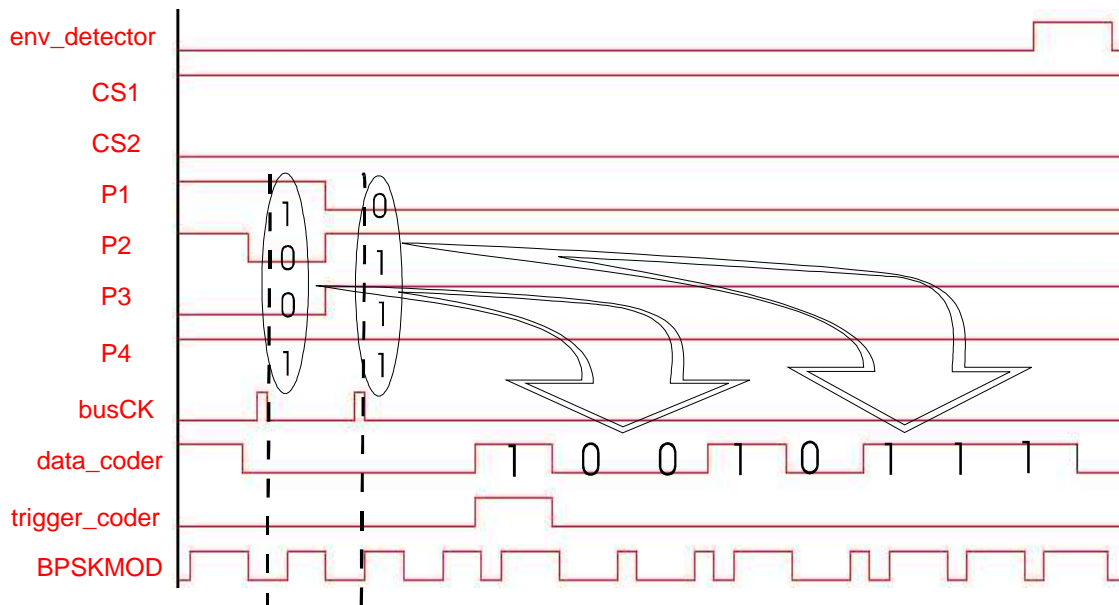


Figure 4-51. PIC to ETU data transference

PIC ⇒ TIC ⇒ 8bits Output

The protocol used is identical to the 4bits Command transference. Now the data (clocked by *busCK*) is sent to the AU through the 8bits line named OutX. Figure 4-52 shows a 8bits line transference. Again it makes no sense to use this interface without the micro-controller.

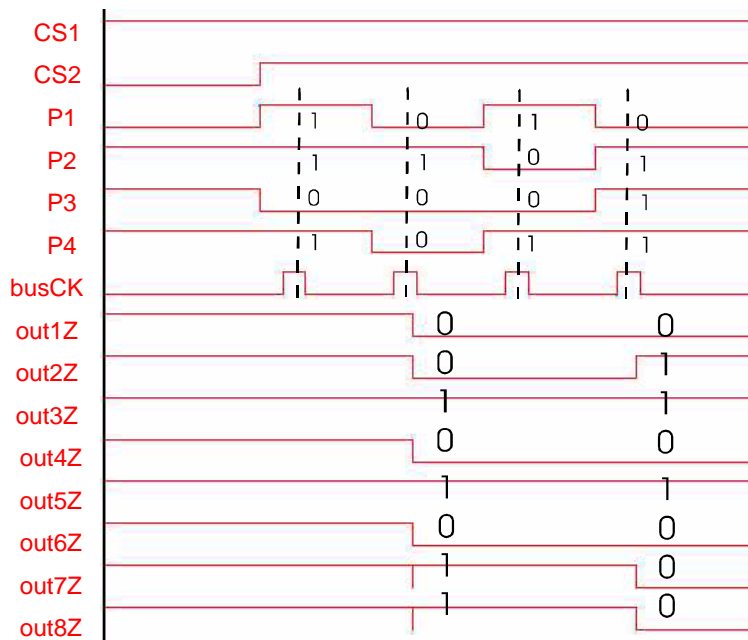


Figure 4-52. PIC to TIC to 8bits Command data transference

Serial ⇒ TIC ⇒ ETU

The data transference to the outside through the use of the serial interface (eventually with the AU) is presented now. Independently of the CS's values if bit1='0' then the on-chip transmitter sends to the ETU the codified data coming from the serial input (pad named *serial*) and clocked by *busCK*.

ETU ⇒ TIC ⇒ Serial

Changing the Bit1 to '1' the IO serial pad is programed as output pad. Thus the data sent by the ETU and decodified by the TIC is sent to the AU through the serial pad. Data is clocked by the base-clock (234kHz). Every 8bits, a header is announced by a pulse in the *ctrl_serial* line. See figure 4-53.

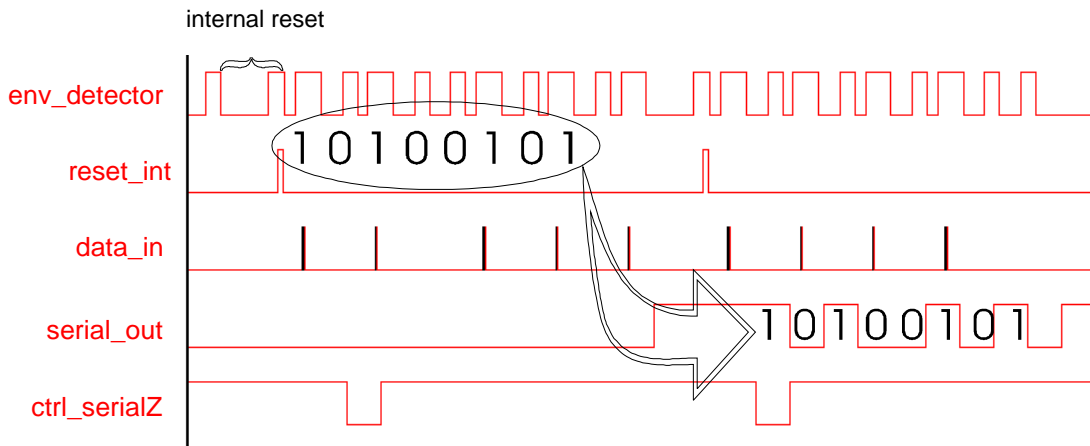


Figure 4-53. ETU to TIC to serial data transference

4.4.2.2.4 Layout

Figure 4-54 shows the TICv1.0 Top layout fabricated through Europractice program:

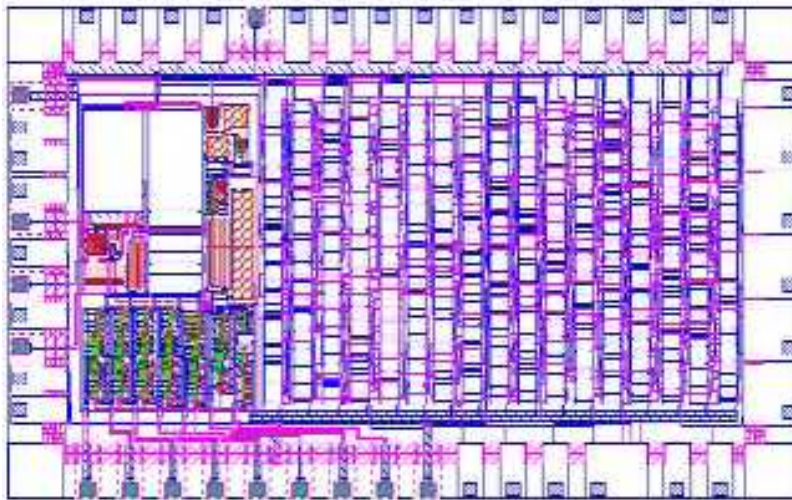


Figure 4-54. TICv1.0 Top Layout

Overall mask dimensions are $5.4 \times 3.5 \text{ mm}^2$. In total there were 48 pads: (9) power, (2) analog inputs, (3) analog outputs, (4) digital inputs, (24) digital outputs and (6) digital IO pads.

4.4.3 Results

The results of this section will not involve any particular application as opposed to the other two systems already shown. A TIC chip and a prototype board including a PIC controller were obtained. The work here presented has to be understood not as a system demonstrator but as a system design concept. This represented the first generation of a general-purpose telemetry chip that the CNM-GAB pursued to develop. Further efforts of colleagues in the center have made possible the development of system demonstrators using the concept outlined in this section, like a four channel micro-stimulator or a bladder control prototype^[9].

4.4.3.1 ASIC fabrication

The chip was fabricated using the same technology as the ITUBR project (see section 4.2.2.2.1) therefore using MIETEC-HBIMOS technology. Figure 4-55 shows a microphotograph of the TIC ASIC.

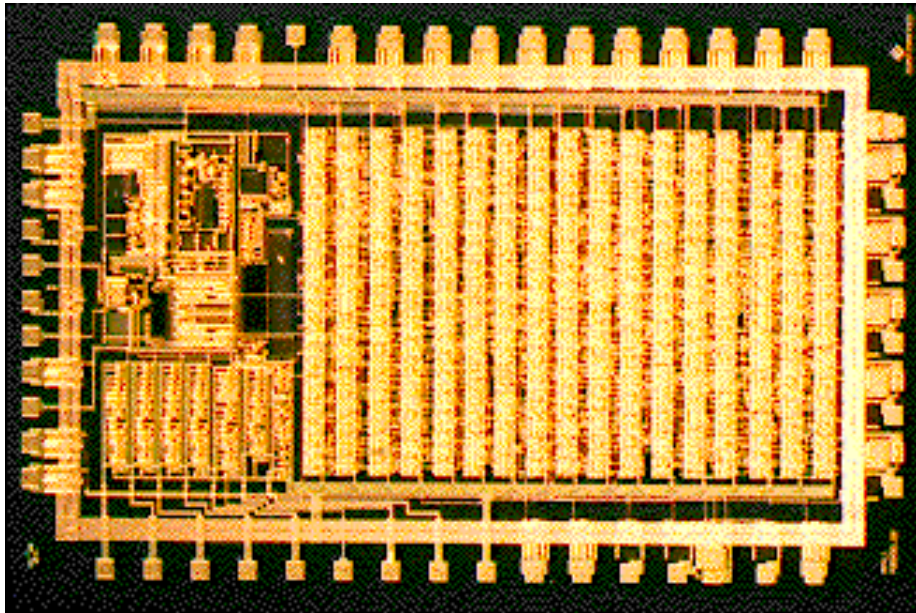


Figure 4-55. TIC microphotograph

4.4.3.2 Digital interface results

The telemetry sections were identical to the design and results already shown in previous chapters two and three. The new test involved mainly the verification of the digital interface. Major accomplished milestones were:

- ➔ Verification of Downlink and Uplink circuits (refer to chapter three).
- ➔ Verification of system clock configuration through link (see figure 4-56)
- ➔ Verification of ETU \Rightarrow TIC \Rightarrow Serial communication (see figure 4-57)
- ➔ Verification of Serial \Rightarrow TIC \Rightarrow ETU communication (see figure 4-58)
- ➔ Verification of ETU \Rightarrow TIC \Rightarrow PIC communication (see figure 4-59)
- ➔ Verification of PIC \Rightarrow TIC \Rightarrow ETU communication

Next follows some oscilloscope waveforms related to the digital interface.

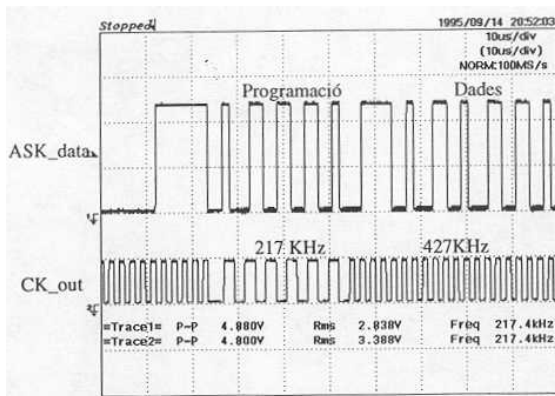


Figure 4-56. Clock setting to 427kHz

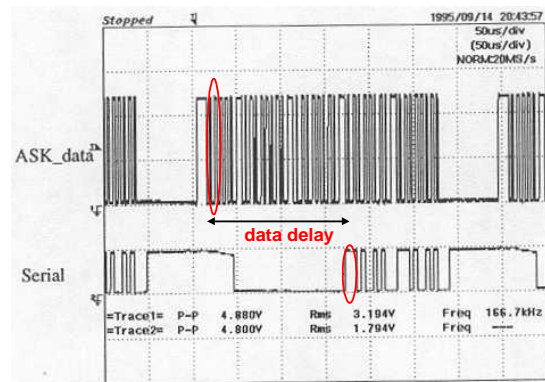


Figure 4-57. ETU \Rightarrow TIC \Rightarrow Serial delay

When the five start-up bits are received the clock will be set to the programmed value. For example in figure 4-56 a 427kHz clock is set after the 5 bits are received. In

figure 4-57 we see a ETU to TIC to Serial port transfer. There is some delay between the input data (ASK data) and the serial output of around 150us.

In figure 4-58 a serial to TIC to ETU transfer is performed. In the upper waveform we see the serial input data to be transmitted to the outside (10000111 frame). In the bottom the pulse width modulated data (*MOD* line) ready to be sent to the modulator and ultimately transmitted to the ETU. Figure 4-59 shows an ETU to TIC to PIC transfer. The four parallel outputs are used to send data to the micro-controller. As we see in figure 4-59, the upper signal is the parallel clock (*parallel_ctrl*) that informs the PIC when the data is ready in the 4-bit bus. The lower signal is an example of a bit-1 activity (*p1*).

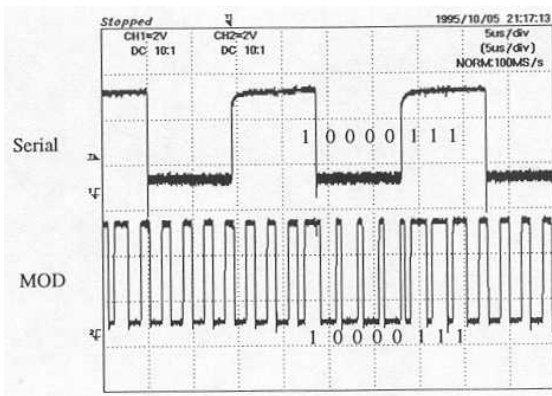


Figure 4-58. Serial \Rightarrow TIC \Rightarrow ETU

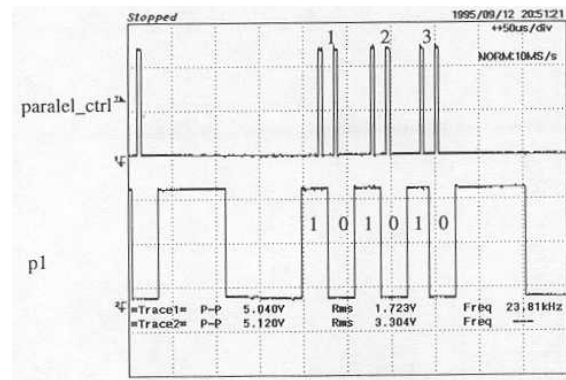


Figure 4-59. ETU \Rightarrow TIC \Rightarrow PIC

4.5 REFERENCES

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- ⁷ Buck, R. P.; Toth, K.; Graf, E.; Horvai, G.; Pungor, E. *J. Electroanal. Chem.* 1987, 223, 51.
- ⁸ E. Lindner, R. Buck, “Micro-fabricated potentiometric electrodes and their in vivo applications” American Chemical Society, May 1, 2000; pp. 336 A-345 A
- ⁹ Internal CNM-GAB documentation.

CHAPTER FIVE

CONCLUSIONS

In this thesis we described different solutions to a variety of key needs within the implantable electronics world, introducing a number of novel techniques and implementations from module to system level.

First a novel high-bandwidth RF link was presented. It was the first of its kind (by the time to be developed) to allow short-range bi-directional full duplex communication with data rates up to 500kbps requiring a high frequency inductive link. This system opened the possibilities of high bandwidth applications for implantable devices that will become more and more dominant in the future as device complexity grows. Downlink was implemented using ASK at 10Mhz and Uplink was done with a BPSK 30Mhz channel.

In addition to that, several new telemetry techniques were also investigated. Among others the ultra-low-power Uplink so-called “LC-modulation” technique that uses the self-resonance of a parallel tuned tank to burst wide-band magnetic signals that can be picked-up by the external receiver. With a PPM coding scheme this technique allows transmitters bellow 1uW of power operation to send signals a few centimeters away.

Continuing with low power solutions, especially important for battery operated devices, a novel ultra-low-power narrow-band low-energy-field receiver was also investigated showing current consumption in continuous operation bellow 1uA. For complex implants with embedded microprocessor hibernating in low-power state this is a perfect implementation for a system wake-up solution without requiring a strong magnetic field.

In the line of getting something as close as possible to a System-on-chip solution a novel digitally tunable BPSK transmitter was also introduced. The build-in VCO allows successful data link for a variety of coils without requiring any external tuning capacitor. In addition to that a fully integrated receiver was also explored, again with only a coil as off-chip component. The concept introduced is that for primary battery-operated devices where transcutaneous energy is not required, a short-range telemetry scheme can be implemented without requiring the coil to be properly tuned (highly detuned high impedance receiver) thus removing the need of a tuning capacitor. Conceptually the trade-off is between signal-to-noise ratio and complexity. The more S/N the simpler you can build your system, and for short-range implants where S/N can be significantly large the option presented above complies with today's integration needs. Therefore the only non-integrated component would be the coil. This also opens the door to future fully integrated solutions (including on-chip coils) resulting in low cost and miniaturized implants.

In terms of the RF energy transfer, several novel concepts have been investigated. First, due to bandwidth requirements already mentioned above, we had to design an efficient power link at 10MHz. That involved mainly design effort in the external transmitter (where state-of-the-art transmitters were around 1Mhz), obtaining a high-efficiency high-frequency Class-E coil driver. A second novel technique introduced in the RF section is the concept of modulating the magnetic field with a close loop control of the energy transferred and using a coding scheme that will not require any extra bandwidth. Within the communication protocol the acknowledge will carry embedded the information whether the B-field that the implant "sees" is too strong, too weak or just fine. This can improve dramatically the power requirements of the external controller (very important if portability is required and therefore battery life or time between recharge in case of secondary batteries is critical) because it generates only the field necessary, no more no less. At the same time this decreases the risk associated to long-term high field exposures. A second technique to optimize the B-field generated has been also presented: sensing the primary-coil current the transmitter can evaluate the reflected impedance and therefore the coupling factor (k) if the secondary load as well as the rest of the network parameters (inductances and quality factors) are known. With the coupling number the transmitter can either increase or decrease the

field without requiring any “active” feed-back” from the implant. This is valid as long as the coupling is large enough to make possible the sensing of the reflected impedance in the primary. If this is not possible (low k scenario) the active telemetered feed-back will be the only feasible choice.

In the area of modeling, a Mathematica program capable of calculating Mutual Inductance (M) versus geometry parameters of the link (coil diameters, distances ,etc.) was written resulting as an effective tool to coil design. This was not novel but very useful nevertheless. A novel theoretical analysis was performed for a very-low-coupling system. This is of great importance for a new generation of implants that will be soon a reality which are so small (eventually injectable) that the coupling factor between the implant and the external controller is dramatically low. This fact makes power transfer even more critical. An extension of the existing theoretical models was performed including the non-idealities of the coil (finite Q). This proved to be very important to analyze the dependence of the power transfer with the frequency. With an infinite Q the frequency does not matter but with a real coil model there is an optimum frequency point per inductance value. That will allow link optimization for low-coupling systems. In order to generate the model a Matlab script was also created and it showed to be much faster than using traditional spice tools.

Moving forward to system level it is important to mention that most of the solutions presented above have been implemented in silicon and in most of the cases within a real application.

The system level developments have been presented in the framework of three different systems. The first one was an implantable pressure sensor. The second one was an implantable chemical sensor and the third one a general purpose telemetry chip to be applicable to a variety of implantable devices.

For the pressure sensor application a simple conclusion, but probably the most difficult to achieve, is the completion of the development process, going all the way from system level design, communication protocols, implementation, implantation and actual bio-recording while implanted. This represented the first completed wireless and

batteryless implant developed in Spain. Even though the resolution of the AD converter was a problem (due to large DC offset in the sensor decreasing the effective resolution) real vascular pressure recordings were performed and identified as clear blood pressure signals by the physicians assisting to the experiment. This result is by far the one I feel more satisfied. Particular techniques to solve very specific problems are just part of the research effort. Showing that the research done can lead to real devices in this multi-disciplinary engineering field is something of major importance. Additional features of the pressure sensor device are its high level of integration, with an overall volume of less than 4cm^3 and a System-on-Chip implementation with only 5 SMD capacitors, one diode, one flat coil, one small solenoid and the custom mixed-mode ASIC. The development of the ASIC was a major milestone involving a coordinated working effort between the CNM and the UCL-Belgium. Even though the sensory interface was designed by the Belgium university, the PhD candidate took ownership of all telemetry (Uplink and Downlink channels) and power management circuits (energy receiver, regulator, voltage protection, etc.) as well as the complete state-machine-based digital section and final chip layout and verification. The final silicon was manufactured through the Europractice program.

For the chemical sensor application with massive data recording capabilities there are novel techniques that were related to system-level design. Among others the high level of integration: the system was implemented without using any off-chip passive component except a single coil. The use of low-power techniques in both modular level and system level was mandatory to combine miniaturization with long battery lifetime. For example the capability of the system to have a very low-power stand-by mode with an asynchronous (no need to have a clock running in the processor) wake-up signal collected from the $1\mu\text{A}$ receiver was a big part of it. The customized I2C interfaces embedded in the two ASICs were necessary in order to get the proposed Master-Slave architecture using a I2C bus. In terms of memory, one of the custom chips had a build-in I2C interface to a standard memory chip with up to 20 address bits. For the demonstrator purposes only 14 bits of address were used. The functionality of the system at board level was demonstrated including “in-vitro” results when the device was hooked up to an ion-selective electrode sensor. The readings of the device were compared to the ones using standard instrumentation with identical results.

For a system design perspective two different approaches have been presented. The architecture of the Pressure sensor-ITUBR device was based on a state-machine with a very limited degree of flexibility. The interaction between the control unit and the sensor front-end or with the telemetry was done in a rather non-standard way. As opposed to that, in the chemical sensor-MARID system the level of flexibility in the architecture was much higher. A micro-controller took the Master control of the unit and interacted with the peripherals (like analog front-end, telemetry or memory chip) through the standard I2C bus. This allowed a rather easy expandability of the system, but without losing much integration capabilities.

The last system level implementation is the so-called Telemetry Integrated Circuit (TIC). This is a chip solution aiming to cover a niche market within the batteryless implantable devices. The main concept was to re-use the “know-how” and pieces of telemetry design already implemented, to have a versatile general purpose IC solution to provide RF energy and short-range bi-directional data to any batteryless implant. Hence this chip should allow building implantable devices in a short-time and cost-effective manner without worrying about the power and wireless data system. The work presented in this document represented the first generation of these TICs developed in the CNM.

In terms of ASICs, a total of four mixed-mode custom integrated circuits were developed. The RF-powered chips (ITUBR and TIC) were fabricated with MIETEC-HBIMOS technology through Europractice (Europe MPW program). The battery-powered chips (MARID1 and MARID2) were fabricated with AMI-1.2 technology through MOSIS (US MPW program).

In terms of system, a complete implant system (including not only the RF-powered implantable bio-compatible device but also the external reader) was developed to monitor blood pressure. A board-level prototype of both battery-powered implant and external reader was developed to monitor chemical concentrations.

