ANALYTICAL PREDICTIVE 2D MODELING OF PINCH-OFF BEHAVIOR IN NANOSCALE MULTI-GATE MOSFETS

Michaela Weidemann

Dipòsit Legal: T-1801-2011

Michaela Weidemann

DOCTORAL THESIS

Analytical Predictive 2D Modeling of Pinch-off Behavior in Nanoscale Multi-Gate MOSFETs

Supervisor:
Dr. Benjamin Iniguez
Dr. Alexander Kloes

Department
of Electronic, Electrical and Automatic Control Engineering

Universitat Rovira i Virgili

Tarragona, 12th January 2011

List of Symbols

A list of symbols used in this work is given.

C	parameter of conformal mapping
C_{ox}	oxide capacitance
D	absolute term for integration
$\mathcal{E}$	electric field
$\vec{\mathcal{E}}$	vector of an electric field
$\mathcal{E}_0$	electric field at Silicon-SiliconOxide interface
$\mathcal{E}_c$	critical electric field (saturation voltage)
$\mathcal{E}_p$	electric field when entering high field saturation region
$\mathcal{E}_x$, $\mathcal{E}_y$	components electric field
$\mathcal{E}_\perp$	normal component of the electric field
$\vec{e}_x$	unit vector in x-direction
$\vec{e}_y$	unit vector in y-direction
f	conformal mapping function
F	inverse conformal mapping function, also standard (Lagrange) elliptic integral
I_{ds}	source-drain current
I_{dsat}	saturated source-drain current
i	imaginary unit $\sqrt{-1}$
K	complete elliptic integral of the first kind
L, L_{ch}	channel length
ld	channel length shortening
N	number of edges of a polygon
N_A	acceptor doping concentration
N_B	donor doping concentration
N_D	doping concentration
n	mobile charge density

n_i	intrinsic charge density
P	complex potential function
Q_{dep}	depletion charge
Q_{inv}	inversion charge
q	elementary charge
q_i	inversion charge per unit volume
r	gradient
t	coordinate in complex plane
t_{ox}	oxide thickness
$t_{ox}^{\sim}$	transformed oxide thickness
T_{ch}, W_{ch}	channel thickness
u	coordinate in complex plane
V	voltage
V_{bi}	build-in voltage
$V_{d'}$	virtual defined voltage
V_{ds}	drain-source voltage
V_{dsat}	saturated drain-source voltage
V_{fb}	flat band voltage
V_{ge}	equals $(V_{gs} - V_{th})/\alpha_i$
V_{gs}	gate-source voltage
$V_{gs-bottom}$	gate-source voltage applied to bottom gate
V_{gs-top}	gate-source voltage applied to top gate
V_{gs+}	virtual gate-source voltage
V_{gs-}	virtual gate-source voltage
V_{ox}	voltage along the oxide
V_t	thermal voltage
V_{th}	threshold voltage
v	coordinate in complex plane
w	coordinate in complex plane
W_{ch}, T_{ch}	channel thickness
x	coordinate in complex plane
x_m	position of the potential minimum along the center line
y	coordinate in complex plane
z	coordinate in complex plane
Δ	Laplace operator
∇	Del operator
ϵ_0	dielectric permittivity
ϵ_{Si}	dielectric permittivity of Silicon
ϵ_{ox}	dielectric permittivity of Silicon Oxide
θ	fitting parameter for the mobility

μ_0	maximum mobility of charge carriers
μ_{eff}	effective mobility of charge carriers
ρ	charge density
Φ	electric potential
Φ_{2D}	2 dimensionally electric potential
$\Phi_{1'2} \cdots \Phi_{71''}$	electric potential caused by the corresponding boundary piece
Φ_{dg}	electric potential within DG FET
ϕ_{1D}	1 dimensionally solution of Poisson's equation
ϕ_{2D}	1 dimensionally Laplace equation
ϕ_i	inversion potential
$\phi_f it$	fit parameter for the inversion potential
ϕ_s	surface potential
φ_{2D}	2 dimensionally solution of Poisson's equation
Ξ	imaginary part of the solution of the complex potential

Contents

Chapter 1

Introduction

"The complexity for minimum component costs has increased at a rate of roughly a factor of two per year ... Certainly over the short term this rate can be expected to continue, if not to increase. Over the longer term, the rate of increase is a bit more uncertain, although there is no reason to believe it will not remain nearly constant for at least 10 years. That means by 1975, the number of components per integrated circuit for minimum cost will be 65,000. I believe that such a large circuit can be built on a single wafer."
– Gordon Moore, 1965

1.1 History

In 1958 the first integrated circuit (IC) was invented. Only 5 years later Fairchild introduced CMOS circuits [1] and "Silicon Valley" was born. Ever since researchers try to increase performance, energy efficiency and size. Fulfilling Moores law [2] is the official goal of semiconductor industry. Defined are those goals in the International Technology Roadmap for Semiconductors (ITRS) [3]. Fundamentally is the Metal-Oxide-Semiconductor-Field-Effect-Transistor (MOSFET), which is shrunken down to allow a exponentially

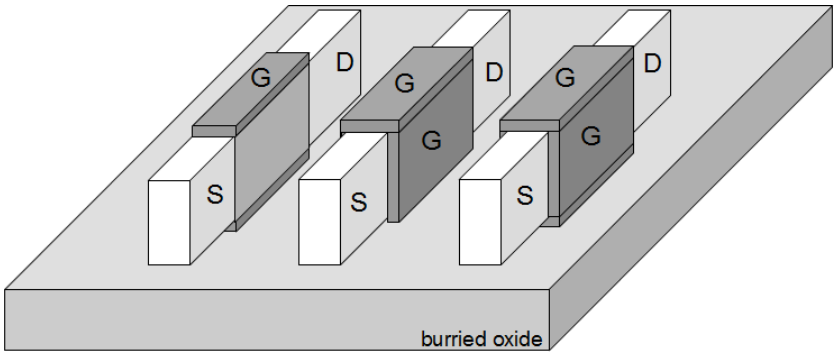


Figure 1.1: Ideal schematic device structures of a DoubleGate FET, TripleGate FET and a QuadrapuleGate FET.

grown number of devices on a chip.

As scaling is expected to reach the 20nm barrier in a few years, MultiGate FETS become more and more important. A few of the most promising and popular are the DoubleGate FET (DG FET), the TripleGate FET and the QuadrupleGate FET, shown in Fig. 1.1 from left to right. They idea was published by [4]. Since then, other multiple-gate SOI MOSFETs have been introduced [5], [6] such as Triple-Gate (TG), FinFET, Pi-Gate (PG), Quadruple-Gate (QG), Surrounding-Gate (SGT), also called Gate-All-Around (GAA), Omega-Gate (Ω-G), etc. Those structure ideas are still challenging to manufacture so studies of them base mainly on numerical device simulations. Scaling SingleGate MOSFET below 100nm (the current record is 3nm gate length [7]) requires high doping and steep doping gradients, which is detrimental for the charge carrier mobility. With MultiGate devices a fully depleted body can be used with low doping [8]. On the other hand it makes the understanding and modeling of the devices more difficult. Due to more gates, field lines are influenced more dimensionally compared to the single gate transistor. Even though there is a lot of research around these different types of multiple-gate MOSFETs, until now, only the DG MOSFET is predicted to be introduced in 2011 due to its advantages [3].

1.2 Circuit Design and Modeling

Increasing number of transistors require increasing performance of design tools. Designing new integrated circuits involves the use of several electronic design automation (EDA) tools for high-level digital design, mask level synthesis, and simulation and modeling of discrete devices. Digital as well as analog systems are simulated uncountable times to ensure their function in any possible case. Those cases can be variation of the environment like temperature changing, hydration variation or power supply variation.

1.2.1 Device Simulations

Discrete devices simulators, such as ATLAS [9], TCAD (Technology Computed Aided Design) Sentaurus [10] or Minimos-NT [11], use a grid on 2D surface or 3D volume and solve each point with the help of a partial differential equation solver on a iterative way. Depending on the number of point a simulation can take several hours.

Beside a wide variation of materials, such as Silicon, Metal, etc. a device simulator offers to vary a wide variety of parameter to change, such as temperature, pressure and so forth. Also the variability of models such as carrier statistics, and current continuity seems endless.

Nevertheless, in addition to the wealth of details necessary for an accurate treatment of complex processes, numerical simulations often offer unparalleled insight into the understanding of physics problems. They can analyze and predict the behavior of novel devices and reduce development costs. Nevertheless, for circuit simulations this is this not applicable.

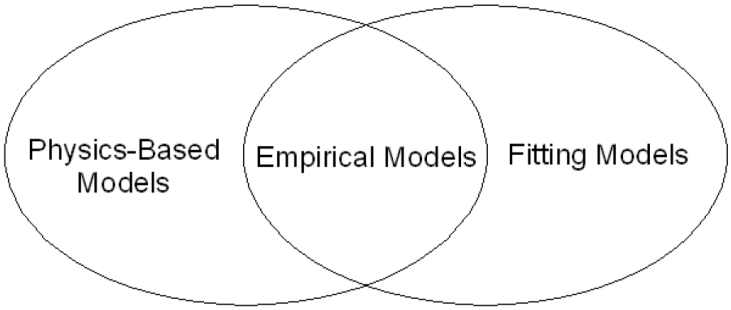


Figure 1.2: Model types for circuit simulator

1.2.2 Circuit Simulations

The circuit simulators SPICE [12] and Eldo [13] are two of the most famous circuit simulators. For that a wide kind of models for devices exist, older models such as BSIM 3v3 [14],PCIM [15], Motorola Model [16] and EKV [17] and models for more advanced devices like the BSIM 4 [18], BSIM 5 [19, 20], PSP [21, 22] or HiSim [23, 24, 25, 26]. Choosing the most effective or most exact model for the circuit simulation is a difficult task and often leaves the circuit designer with a dilemma, whether to choose a time-consuming precise model or a more simplified and quick model for simulation and parameter extraction.

1.2.3 Models for Circuit Simulators

In general such models for circuit simulators can be divided in three types of models [27], [28]:

- physical based models
- empirical models
- numerical models

Figure 1.2 shows a diagram of how they are related to each other. Physical-based models try only to use the physics-based equation to describe the behavior of the transistor. These models have the advantage that they can describe the behavior of scaled devices. However the equations are often not continuous for all transistor states and several equations are used. Their accuracy is not that good described to other model-types [29], [30].

Physical-based models without introduction of empirical fitting parameters. Those models are often introduced in literature to describe the behavior of transistors with relative long channel length or single electric device characteristics like threshold voltage [31].

Empirical models are the model type in-between physical-based and numerical-fit model. Those models use the physical-based equation and introducing some fitting parameters to simplify and improve the models. Unfortunately these fitting parameters reduce the ability to predict behavior of transistors with changed physical characteristics.

Numerical-fit models use expressions without any relation to the basic principals of the device. Equations for a numerical fit models have an uncountable number of fitting parameters and every change of physical device parameters requires a complete new set of fitting parameters.

For all models count the same requirements [31], [32]:

- The model must describe the behavior of the device as exact as possible. The difference between model and real device depends on the application; analogue systems needs higher accuracy compared to digital systems [33].
- Circuit simulators work with iterative methods to solve electrical connections within a design. This needs a lot of time and according to save calculation power and time the model should consist of analytical closed form equation or similar equation like look-up tables. These models

are called compact models. However a good compact model is always a compromise between accuracy and efficiency.

- Convergence reasons require models which are constantly differentiable in first derivative.

- Modern circuit designs consist of a wide variation of devices. It is desirable to use one set of parameters [34].

1.3 State of the Art

This chapter gives an introduction about current modeling ideas for the DoubleGate MOSFET. For all MOSFETs Poisson gives the basic equation

$$\Delta\Phi(x,y) = -\frac{\rho}{\epsilon} = -\frac{q}{\epsilon_{Si}}\left(N_S + n\right), \tag{1.1}$$

rewritten to fit an n-channel device. q the electron charge, ϵ_{Si} the permittivity of silicon, N_S and n are the acceptor doping and mobile charge density, respectively.

For compact modeling of the drain current there are three main strategies

- **drift-diffusion**, carriers experience a considerable amount of collisions in the conducting channel [35]

- **ballistic**, carriers have enough energy to cross the barrier before being subjected to significant scattering [36]

- **quasi-ballistic**, which is a ballistic transport with a statistical ballistic carrier scattering quotient included as a model parameter [37]

1.3.1 Long Channel DG MOSFET

Most models presented for DG MOSFETs so far are for undoped devices with a long enough channel to assume that the transport is due to the drift-diffusion transport mechanism [38, 39, 40, 41]. A lot of approaches are for long-channel modeling. Hereby electric field associated with charge carriers terminate mainly underneath the gate oxide. The device has a long channel behavior and the Poisson equation needs only to be solved 1D in transversal direction to the channel to capture the main body effects. Short channel effects are taken into account by suitable approximations. In the case of a long-channel symmetrical undoped device, an analytical solution of 1D Poisson's equation is obtained [39], [40]. Making some approximations, a charge control model based on this solution can be derived [42].

A 1D transversal approach of Poisson's equation is not suitable, when the device is heavily doped. Assuming that the light doping represents relatively few carriers in a thin device, the electrostatic effect from the dopants can be regarded as negligible in strong inversion. Some approximations have been made to find an analytical solution in moderate or weak inversion [43]. It is assumed that in sub-threshold when the mobile charge density is much less than the body doping concentration, it is found that $\phi_S - \phi_0$ is constant. Poisson can be reduced to its depletion form, taking only into account the fixed charges. Another approach is the modeling presented in [44], a model which is valid from weak to moderate inversion. Modeling of doped devices can be thought of by having two single gate transistors, with two inversion channels close to the gates. This implicitly assumes that the current flowing through the device center is negligible compared to the inversion carrier current found at the body/insulator interfaces.

1.3.2 Short Channel DG MOSFET

In so-called short-channel devices, the length/height aspect ratio is so small that the 2D effects contribute so much to the device behavior that they become non-negligible when modeling. This manifests itself through various short-channel effects (SCEs), such, for example drain-induced barrier lowering (DIBL) [45]. If the transport mechanism is drift-diffusion, a compact analytical solution seems difficult to obtain, since it has to be determined self-consistently with the current continuity equation, which includes the quasi-Fermi potential. An exception is the subthreshold regime where the quasi-Fermi potential is constant in most of the channel [46]. A threshold based short-channel model was be found by solving Poisson's equation with only the mobile charge term. Nevertheless, to take into account short-channel effects in those devices a 2D approach is needed, where both the capacitive coupling between the electrodes (source, drain and gates) and the electrostatic effects of the space charge are self-consistently included.

To calculate a 2D Poisson approach different mathematical methods are used. In lightly doped DoubleGate devices the potential follows in principal $V_{gs} - V_{fb}$, whereby V_{gs} is the gate-source voltage and V_{fb} is the flatband voltage. By disregarding doping dependent and free carriers Frank [47] and Liang [48] managed to use a infinite series of sinh and sin functions. For an aspect ratio (length/height) larger than 2, the modeling yields good results retaining only a couple of terms of the series. With a higher V_{ds} (drain-source voltage) free carriers need to be taken into account.

Munteanu [49] uses an empirical function to model the electrostatic potential. The electrostatic potential is divided into separate transversal and lateral solutions,

$$\phi(x, y) = \phi_S x A(x, y). \tag{1.2}$$

ϕ_S is the surface potential on the body/insulator interface, and $A(x, y) = \frac{B(x,y)}{B(x,y=0)}$ is an envelope function, modulating the surface potential. Empirical approaches uses often an parabolically shaped profile in sub-threshold.

Francois publishes an empirical approach with a power law for above threshold regime in [41], whereby the profile is

$$\phi(x, y) = a + b(x)y + c(x)y^n. \tag{1.3}$$

With this approach it is possible to calculate a channel length modulation of a DG FET. In general empirical functions are suitable candidates a few adjustable parameters to account for some intricate modeling details. Nevertheless, those approaches are rather quasi-2D than fully 2D and due to the complexity in the terms often simplified.

A new idea for solving 2D Poisson is to split it up in a Laplace equation, which represents the capacitance part

$$\Delta\phi_{2D}(x, y) = 0 \tag{1.4}$$

and a 1D Poisson part, which represents the mobile charges

$$\Delta\Phi(x, y) = \Delta\phi_{(2D)}(x, y) + \Delta\phi_{(1D)}(x). \tag{1.5}$$

This has the advantage that both parts are self-consistent and it results in a more flexible way to solve Poisson's equation. With the re-introduction of conformal mapping technique it was possible to solve 2D Poisson more physics related. The approach was successfully applied to bulk MOSFETs [50], [51] and [52], as well as DG FETs [53], [38].

In further work the Schottky-Barrier in DG MOSFET was calculated by Schwarz, [54, 55, 56].

1.3.3 Asymmetrially biased Double Gate MOSFET

In a DG MOSFET structure a asymmetrically biased structure is possible. DG MOSFETs have in addition to the inherent suppression of short-channel effects and naturally steep subthreshold slope, a high drive current (I_{on})

and transconductance, generally attributed to the two channel property of the symmetrical device [57]. Nevertheless, a electrical coupling is assumed between both gates. This charge coupling of the two gate structures underlies the noted features of the device, which translates into a high I_{on}/I_{off} ratio when threshold voltage is proberly controlled [58].

To gain such a control, it has been shown that asymmetric gates of n^+ and p^+ polysilicon are a first approach [59] and [60]. Nevertheless, with such an approach, the device has only one predominate channel, which might undermines the current drive.

For independently biased DG MOSFETs only few models exists. The first model was developed by Taur in 2001 [61]. A one-dimensional (1-D) analytic solution is derived for an undoped (or lightly doped) double-gate (DG) MOSFET by incorporating only the mobile charge term in Poisson's equation. The solution is applied to both symmetric and asymmetric DG MOSFETs to obtain closed forms of band bending and inversion charge as a function of gate voltage and silicon thickness.

In [62] a model for asymmetrically biased DG MOFETs with long channels was published. Unfortunately this model offers no numerical solution and was derived from a Bulk MOSFET approach. Also, in [63] Nakagawa published an improved almost closed-form version to his previous model in [64], this model covers short-channel effects with a rather weak description.

M. Chan [65] ignores in his approach the vertical carrier distribution, which maybe valid in bulk MOSFETs. According to him, it cannot fully account for the behaviors observed in DG MOSFETs such as volume inversion and quantum confinement by the dielectric barriers. This requiers a fully 2D approach, here a quasi-2D approach is used. Nevertheless, Chan offers a quasi-2D model for the saturation characteristics of the DG MOSFET. The channel of the device is divided into gradual channel approximation (GCA) region and velocity saturation region (VSR).

1.3.4 Multi-Gate MOSFET

With more gates, the modeling approaches become more and more challenging. The model in [66] by Chevillon accounts for all major small geometry effects and allows accurate simulations of both n- and p-type FinFETs. The model core is physics-based (long-channel model) and has some semiempirical corrections.

So far, mostly sub-threshold or near-threshold models for FinFETs are published. As in [67] for subthreshold conditions, the electrostatics is assumed to be dominated by capacitive coupling between the body electrodes, thus the potential is obtained as a solution of the 2D Laplace equation with the help of conformal mapping techniques. In the near-threshold regime, Poisson's equation is solved using quantum-mechanical charge density, in the gate-to-gate direction to model the total potential.

Recently with an idea how to introduce of third dimension to the conformal mapping technique it was possible to adapt a more physics-based approach to FinFETs [68, 69, 70], which resulted in a closed-form current equation [71], [72].

More often approaches to solve Gate-All-Around (GAA) MOSFET can be found. In [38] the approach to solve a DG MOSFET with the help of conformal mapping technique is extended to meet the requierments of GAA MOSFETs. A lot of approaches use conformal mapping technique to come to more physics-related models, [73, 74]

1.4 Outline of the Thesis

In this thesis a new way to find a saturation point in a DoubleGate MOSFET is presented. This saturation point is identified when the electric potential maximum, which is at the beginning of the channel located underneath the

Silicon-SiliconOxide interface, moves into the middle of the channel. Based on this definition a fully 2D model is created to calculate the position of the saturation point. Throughout this thesis all results are compared to a numerical device simulator TCAD Sentaurus [10].

After the introduction in chapter one, chapter two primarily deals with the mathematical basics that are used in here. The conformal mapping technique is explained, which is used to solve a 2D integration system in analytical closed form. With the help of the Schwarz-Christoffel [75], [76] approach a z-plane is transformed into the upper half of w-plane and the equations can be determined.

Chapter three presents a channel length model for a Single Gate MOSFET.

Chapter four explains the device physics of a symmetrical biased DoubleGate FET in saturation. Whereby a new method, used in this thesis, to identify the saturation point is presented. Afterwards the model is explained with all necessary approaches.

Introducing an extension of the DG model in chapter five, the saturation points of an asymmetrically biased DG FET can be calculated. Whereby at the beginning of chapter four first the physical characteristics of the pinch-off point are explained.

In chapter six the saturation-point in a FinFET is analyzed. Also it gives an idea about a model approach for a FinFET.

Chapter seven draws a conclusion.

In the appendix the closed form solution to solve the integration system for the 2D Laplacian is described.

Chapter 2

Mathematical Basics

In general in MOSFETs with very small geometries, the potential distribution and therefore the electrical field lines are more-dimensional. In order to take as many effect into account as possible and to come to a closed solution for the equations later, the complex potential theory was used to solve the partial differential equations. In this work a so called conformal mapping technique was applied to solve a 2D Laplace integration system. This idea comes from [75], [77], and [78].

2.1 Harmonic Functions

The general definition of the Poisson equation is

$$\nabla \cdot \mathcal{E}(r) = \frac{\rho(r)}{\varepsilon}. \tag{2.1}$$

This partial differential equation, based on Maxwell, is valid for electrostatic and mechanical engineering as well as theoretical physics problems. In a partial differential equation the charge density ρ along a gradient r results in the electric field $\mathcal{E}$. Since the permittivity ε depends on the material, the

equation for silicon is

$$-\nabla \cdot \mathcal{E}(r) = \Delta\Phi(r) = -\frac{\rho(r)}{\varepsilon_0 \cdot \varepsilon_{Si}}. \tag{2.2}$$

Written in a 3-dimensionally Cartesian:

$$\Delta\Phi(x,y,z) = -\frac{\rho(x,y,z)}{\varepsilon} = \left(\frac{\partial^2}{\partial x^2} + \frac{\partial^2}{\partial y^2} + \frac{\partial^2}{\partial z^2}\right)\Phi(x,y,z). \tag{2.3}$$

With no space charge it results in a special case of the Poisson equation,

$$\Delta\Phi(x,y,z) = 0 \tag{2.4}$$

a so called Laplace's equation. Using proper boundary conditions this equation can be solved. Solution of Laplace's equation are called harmonic functions with some specific properties [75], [77], [79], [80].

- Principle of superposition holds
- A function Φ that satisfies Laplace's equation in a closed volume and satisfies one of th following type of boundary conditions on the enclosing boundary is unique.
  - the value of the function is specified on the whole boundary (Dirichlet condition)
  - the value of the normal derivative, $n \cdot \nabla\Phi$, is specified on the whole boundary (Neumann condition), whereby n is the (outward-pointing) unit normal vector
  - the function Φ is specified on part of the boundary and $n \cdot \nabla\Phi$ on the rest.
- If Φ satisfies Laplace's equation in a region, bounded by the surface, Φ can attain neither a maximum nor a minimum within the region. Extreme values occur only on the surface.

2.2 Complex Potential Theory

A Laplace's equation is adaptive to several different coordinate systems like the rectangular or Cartesian, the spherical and the cylindrical. Conformal mapping is one method to transform a 2D system from one geometry to another. Usually the way to solve Laplacian is to choose a coordinates system wherein the boundary surface coincides with the surface and one of the coordinates is constant. For using conformal mapping the problem has to be 2D and boundary conditions have to contain only two variables (x and y).

Giving every complex number of the variable z the value of a variable w, using $w = u(x,y) + iv(x,y)$, then it w a complex function of the complex variable. A complex function eventually maps all points within a volume of an area z into points in an area w.

Assuming an equation $z = x + iy$ and a function $f(z)$ [80], [81]

$$f(z) = u(z) + iv(z) = u(x,y) + iv(x,y) \tag{2.5}$$

The variables x and y are real valued and u and v are real valued functions of these variable. As derivation results

$$f'(z) = \lim_{\Delta z \to 0} \frac{f(z_0 - \Delta z) - f(z_0)}{\Delta z}. \tag{2.6}$$

To fulfill the Cauchy-Riemann-Condition it is necessary that the derivatives of $f(z)$ exist in a point z. The partial derivatives of u and v obey the following condition

$$\frac{\partial u}{\partial x} = \frac{\partial v}{\partial y} \qquad \text{and} \qquad \frac{\partial u}{\partial y} = -\frac{\partial v}{\partial x}. \tag{2.7}$$

On the other hand, if the continuous, partial derivatives of u and v fulfill the Cauchy- Riemann condition, $f'(z)$ at that point exists. With a second derivation of u and v the result is

$$\frac{\partial^2 u}{\partial x^2} + \frac{\partial^2 u}{\partial y^2} = 0 \qquad \text{and} \qquad \frac{\partial^2 v^2}{\partial x^2} + \frac{\partial v}{\partial y^2} = 0. \tag{2.8}$$

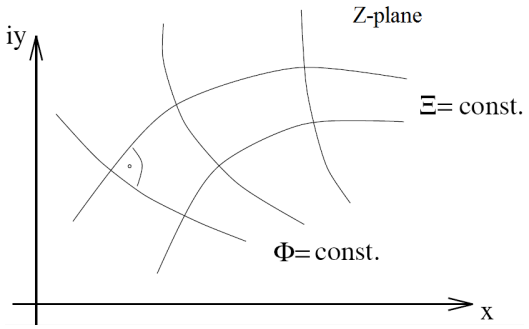


Figure 2.1: In electrostatics the real part of $P = \Phi(x, y) + i\Xi(x, y)$ is defined as electric field, the imaginary part is called the stream function. Here both functions are exemplary plotted and cross each other in a right angle.

Until those derivations exist and are continuous, they are harmonic functions; Because they are solutions of the Laplacian. In electrostatics the real part u of the complex harmonic solution of Laplace's equation $f(z)$ is defined as electric potential. The imaginary part v is called the stream function. Its level curves are called stream lines. The name comes from the analogy in fluid flow. This equation is called complex potential function. [75], [77]

$$P = \Phi(x, y) + i\Xi(x, y) = u(x, y) + iv(x, y) \tag{2.9}$$

Assume, then, in the complex harmonic function $w = u + jv$, the real part $u(x, y) = \Phi$ as the potential function; the field strength vector $\mathcal{E}$ follows as greadient in the real x, y-plane,

$$\vec{\mathcal{E}} = \mathcal{E}_x \vec{e}_x + \mathcal{E}_y \vec{e}_y \tag{2.10}$$

with

$$\mathcal{E}_x = \frac{\partial \Phi}{\partial x} \qquad \text{and} \qquad \mathcal{E}_y = \frac{\partial \Phi}{\partial y}. \tag{2.11}$$

By using Eqn. (2.7) and Eqn. (2.11) and the Cauchy-Riemann condition

it results in

$$\mathcal{E} = \mathcal{E}_x + i\mathcal{E}_y = -\frac{\partial \Phi}{\partial x} - i\frac{\partial \Phi}{\partial y} = -\frac{\partial u}{\partial x} + i\frac{\partial v}{\partial x} = -\left(\frac{df\bar{}(z)}{dz}\right), \tag{2.12}$$

the absolut value of the complex derivative as a direct measure of the field strength

$$|\mathcal{E}| = \left|\frac{df\,(z)}{dz}\right| \tag{2.13}$$

and the the conjungate complex derivative is the equivalent of the two-dimensional gradient of the vector analysis.

The so called potential function

$$P = \Phi\,(x, y) + i\Xi\,(x, y) \tag{2.14}$$

can be used to calculate either the characteristics of the equipotential lines ($\Phi\,(x, y) = constant$) or the characteristics of the field lines ($\Xi\,(x, y) = constant$) as shown in Fig. 2.1.

2.3 Conformal Mapping

Two complex planes are given

$$z = x + iy \qquad \text{and} \qquad w = u + iv. \tag{2.15}$$

Assumed the function is analytic at the point $z = z_0$, where $f'(z_0) \neq 0$, there exists a neighbourhood of the point w_0 in the w-plane in which the function $w = f(z)$ has a unique inverse

$$z = F(w). \tag{2.16}$$

The functions f and F defines a change of variables from (x, y) to (u, v) and from (u, v) to (x, y), respectively. When this change of basis is defined

through an analytic function all curves in the z-plane that cross each other at an angle are mapped into curves in the w-plane that cross each other at exactly the same angle. This is why the mapping is called conform. The curves can be the boundaries or equipotential curves, electric field lines or any curves.

In particular since the set of curves that are horizontal in the z-plane are perpendicular to the set of curves that are vertical the two sets will be mapped into perpendicular sets in the w-plane. Of course the opposite is also true. To be noted is that in points where f or its inverse is not analytical the transformation is not conform.

2.3.1 Transformation of a Potential

With the proper transformation of function Eqn. (2.9) to a w-plane [75]:

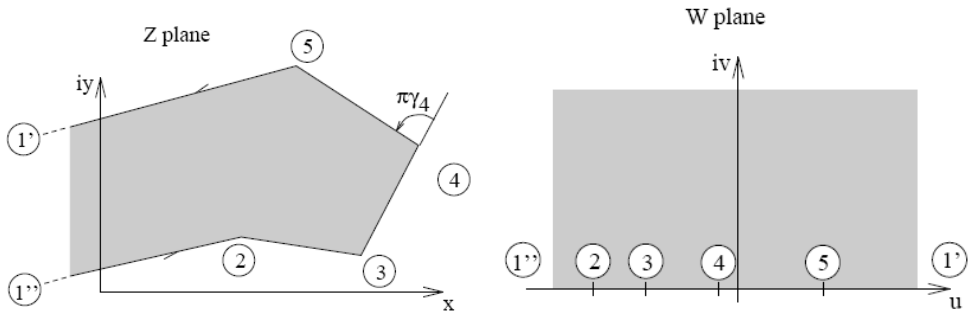
$$\tilde{P}(u,v) = \tilde{\Phi}(u,v) + i\tilde{\Xi}(u,v) \tag{2.17}$$

the partial solutions of $\tilde{P}$ ($\tilde{\Phi}$ and $\tilde{\Xi}$) are harmonic functions and therefore solutions of a scalar potential problem. They also give the value of the electric field with respect to the geometry

$$|\mathcal{E}|(z) = |\mathcal{E}|(w) \cdot \left|\frac{dw}{dz}\right|. \tag{2.18}$$

This means an integration along a line in the z-plane has the same result as an integration along the transformed function in w-plane. From that the charge for Poisson's equation $\rho(z) \neq 0$ needs a scaling as well

$$\rho(w) = \frac{\rho(z)}{\left|\frac{dw}{dz}\right|^2} \tag{2.19}$$



(a) (b)

Figure 2.2: Area wherein 2D Laplacian is solved in z-plane. b.) Area transformed with Schwarz-Christoffel upon w-plane. All points are now located on the real axis.

2.3.2 Mapping the Insides of Closed Polygons

Transforming an area with polygon shaped boundaries it is possible to use Schwarz-Christoffel for this [75], [76]. After mapping the function $z = f(w)$ in the w-plane the function is placed in upper region of the w-plane as shown in Fig. 2.2. The polygon shaped boundary conditions lay then flat on the real axis. The differential $\frac{dz}{dw}$ is calculated by

$$\frac{dz}{dw} = C\,(w - w_1)^{\gamma 1}\,(w - w_2)^{\gamma 2} \ldots (w - w_n)^{\gamma n} = C \prod_n (w - w_n)^{\gamma n} \qquad (2.20)$$

The vertexes of the polygon are represented by $z_n = f(w_n)$. Whereby each angle change is given by $\pi\gamma_n$. The angle change is measured with the enclosed region on the left hand. Points which change during transformation to $w = \pm\infty$ are not considered. The transformed function is Eqn. (2.21) with the integration constant D. This constant gives the origin of the coordinate system z-plane.

$$f\,(w) = C \int \prod_n (w - w_n)^{\gamma n}\, dw + D \qquad (2.21)$$

To find all parameters for the conformal mapping still some relations with the z-plane are necessary. The distance of two parallel polygon components

is given with $\gamma_n = +1$ and the point $z_n = \infty$

$$z'_n - z''_n = -i\pi C \prod_{a \neq n} (w_n - w_a)^{-\gamma a} \tag{2.22}$$

Additionally with $w_n = \pm 1$ Eqn. (2.22) can be simplified

$$z'_n - z''_n = -i\pi C \tag{2.23}$$

A polygon with N vertexes has w_a points. Together with the integration constants C and D we have $N+2$ unknown parameter. Just three parameters can be chosen, so $N-1$ parameters have to be solved with Eqn. (2.22) and Eqn. (2.23).

2.4 Decomposition Strategy

Depending on the complexity of the structure, in where the Laplace Equation will be calculated, a closed-form solution might not be found. The Poisson Equation needs an additional scaling of the space charge ρ with Eqn. (2.19). Also, for some models it might be necessary to include the inversion charge, which needs a scaling as well. That can result in an iterative process to find a solution for the potential.

Throughout this work the idea is to divide the Poisson Equation into an one-dimensional, particular part $\Phi_{1D}(x)$ and and a two-dimensional part $\Phi_{2D}(x, y)$. Whereby the two-dimensional part represents the solution of the Laplacian,

$$\Delta\Phi(x, y) = -\frac{\rho}{\epsilon} = \Delta\Phi_{1D}(x) + \Delta\Phi_{2D}(x, y). \tag{2.24}$$

The one-dimensional part $\Phi_{1D}(x)$ might contains the space charge or the inversion charge. This makes it possible to add these charges without a complex scaling process. Unfortunately, the effects, which can be included can only depend on x or y direction.

2.5 Potential Solution of Boundary Conditions

The strategies to solve 2D boundary conditions here presented are for Laplace Euqations. With the before explained decomposition idea only potential solutions for Laplace Equations are necessary, because this strategy makes it possible apply those to Poisson's Equations.

The, in this thesis, used structures only require Dirichlet boundary conditions and since the law of superpositioning holds, all types of boundary conditions can be solved.

2.5.1 Discontinuous Points

A region is conformally mapped with Eqn. (2.20) together with the enclosing polygon [78], [82]. However the vertexes z_n are not. These points are isolated singularities or $F(w_a) = 0$. For that it is possible to converge very close to those points. Whenever the potential solution within w-plane is continuous the points can be handled as conformally mapped [75]. Figure 2.3 shows in a.) two points on the u-axis with potential φ with an infinitesimal small distance u. This infinitesimal distance at $w = u$ leads to

$$P = \Phi + i\Xi = d\varphi + i\frac{d\varphi}{\pi} \cdot \ln(w - \bar{u}). \tag{2.25}$$

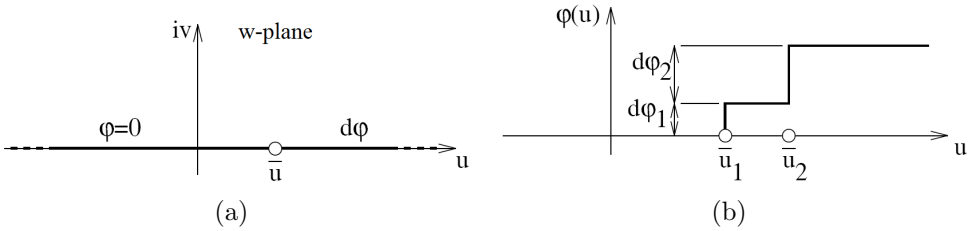


Figure 2.3: The solution for two electrodes along the real u-axis is well known. a.) Two electrodes having a potential difference $d\varphi$ and an infinitesimal gap between them at position u. The potential solution of this problem will be used to calculate the solution of a problem with boundary conditions as shown in b.). This is done by superposition of two electrode formations with different u and $d\varphi$.

2.5.2 Boundary Integral

The normal component of the electric field of two electrodes, which shows a difference of $d\varphi$ in potential (Figure 2.3 a.)), can be calculated by [82], [50]:

$$d\mathcal{E}_{\perp}(w) = -\frac{\partial \Phi}{\partial v} = \frac{\partial \Xi}{\partial u} = \frac{\partial}{\partial u}\frac{d\varphi}{\pi} \cdot \ln(u - \bar{u}) = \frac{d\varphi}{\pi}\frac{1}{u - \bar{u}} \tag{2.26}$$

because of the Cauchy-Riemann condition. Additional with the scaling, necessary because the electric field is within the closed polygon, it comes to

$$d\mathcal{E}_{\perp} = d\mathcal{E}_{\perp}(z) = \left|\frac{dw}{dz}\right| \frac{d\varphi}{\pi} \cdot \frac{1}{u - \bar{u}}. \tag{2.27}$$

If more than one boundary condition is present in a way shown in Fig. 2.3 a.) and the infinitesimal small gap $\bar{u}$ is on different positions, it will result in a cascaded alignment of potential difference $d\varphi$, Fig. 2.3 b.). For the infinitesimal small distance at the vertex point $\bar{u}$, the potential can be calculated with

$$d\varphi = \left.\frac{d\varphi(u)}{\partial u}\right|_{\bar{u}} d\bar{u}. \tag{2.28}$$

Finally the normal component of the electric field along the boundaries can be calculated with [78], [82]

$$\mathcal{E}_{\perp}(u) = \mathcal{E}_{\perp(z)}(w) = \int_{-\infty}^{+\infty} d\mathcal{E}_{\perp(z)} = \frac{1}{\pi}\left|\frac{dw}{dz}\right| \int_{-\infty}^{+\infty} \frac{1}{u-\bar{u}} \left.\frac{d\varphi}{du}\right|_{\bar{u}} d\bar{u} \qquad (2.29)$$

2.5.3 General Laplacian Potential Problems and Conformal Mapping

Since Riemann states [83] that any simply connected region bounded by rectangular curves can be mapped into the interior of a unit circle in a one-to-one manner, the general potential problem should be solved for a unit circle [75]. The function $z = re^{(j\phi)}$ is assumed to have boundary problems of the first kind or Dirichlet. So, the Poisson integral can be used to solve the complex potential function as shown in Figure 2.4:

$$P = \frac{1}{2\pi}\int_0^{2\pi} \frac{e^{j\phi'}+z}{e^{j\phi'}-z}\Phi(\phi')\,d\phi' \equiv \Phi + j\Xi. \qquad (2.30)$$

The real part has the form

$$\Phi = \frac{1}{2\pi}\int_0^{2\pi} \frac{1-r^2}{^{-}2r\cos(\phi-\phi')+r^2}\Phi(\phi')\,d\phi'. \qquad (2.31)$$

Coordinate (r, ϕ) defines a point A within the unit circle and ϕ' a point on the unit circle. However, most mapping problems are mathematically easier when mapped into the upper half of a w-plane instead of mapped into the unit circle, see Figure 2.5. With the mapping function

$$w = j\frac{1-z}{1+z} \qquad (2.32)$$

a unit circle can be mapped into the upper half of w-plane by Schwarz-Christoffel. The corresponding parameters for this are represented by

$$z = j\frac{w-j}{w+j}, \qquad e^{j\phi'} = j\frac{u'-j}{u'+j}, \qquad d\phi' = j\frac{2du'}{1+u'^2}. \qquad (2.33)$$

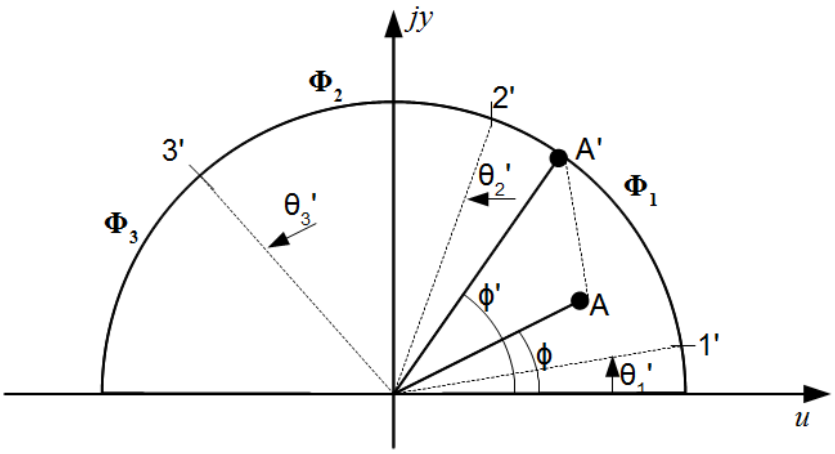


Figure 2.4: Solution of first boundary value along the unit circle.

When placed into

$$P = \frac{j}{\pi}\int_{-\infty}^{+\infty} \frac{1+u'w}{(1+u'^2)(w-u')}\Phi(u')\,du' = \Phi + j\Xi \tag{2.34}$$

it results in the general solution of the first boundary value problem. In (2.34) u' is the integration variable along the real u-axis and w is the arbitrary point where the potential P exists. Taking only the real part of the equation, it leads to the equivalent of Poisson's integral on the unit circle,

$$\Phi = \frac{1}{\pi}\int_{-\infty}^{+\infty} \frac{v}{(u-u')^2+v^2}\Phi(u')\,du'. \tag{2.35}$$

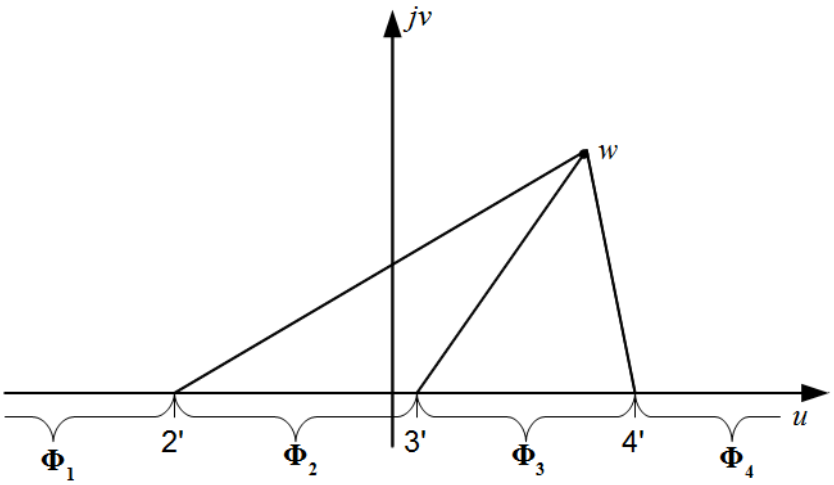


Figure 2.5: Solution of first boundary value problem of the unit circle transformed into upper half of w-plane.

2.6 Transforming the Structure

In this work a 2-corner structure is used in where 2D Poisson is solved. The 2-corner structure has the advantage, that it is relatively simple to solve in terms of mathematical effort compared to for instance a 4-corner structure. This structure includes the SiliconOxide in order define simple boundary conditions. In this section, the transformation of the oxide as well as the transformation of the structure from z into w-plane and back, is explained.

2.6.1 Transformation of the Oxide

In order to keep the approach for the conformal mapping technique as simple as possible the discontinuity of the electric field caused by the different permittivities of the gate oxide and the Silicon must be neglected. This can be done by scaling the oxide according to the relationship of the permeability of SiO_2 and Si. Because of the small thickness of the oxide the electric field

in the oxide is assumed to be homogeneous and can be written as

$$D_{ox} = \epsilon_0 \cdot \epsilon_{Si} \cdot \mathcal{E}_0 = \epsilon_0 \cdot \epsilon_{ox} \cdot \mathcal{E}_{ox} = \epsilon_0 \cdot \epsilon_{ox} \cdot \frac{V_{ox}}{t_{ox}} \tag{2.36}$$

Whereby D_{ox} is the dielectric displacement and V_{ox} the voltage drop across the oxide and $\mathcal{E}_0$ is the electric field right underneath the Silicon-SiliconOxide interface in the Silicon. With

$$t_{ox}^{\sim} = \frac{\epsilon_{Si}}{\epsilon_{ox}} \cdot t_{ox} \tag{2.37}$$

as thickness for the oxide, the electric field $\mathcal{E}_0$ is continuous at the interface

$$D_{ox} = \epsilon_0 \cdot \epsilon_{Si} \cdot \mathcal{E}_0 = \epsilon_0 \cdot \epsilon_{Si} \frac{V_{ox}}{t_{ox}^{\sim}}, \tag{2.38}$$

because the voltage drop along the oxide stays unchanged.

2.6.2 Conformal Mapping of the Structure

Before defining the boundary conditions, the equations for transforming a 2-corner structure from z- plane to w-plane and backwards must be defined. For this just a plane 2-corner structure is used. This rectangular shaped basic element has three pieces, A, B and C as shown in Figure 2.6. Transferring it from z-plane into w-plane Poisson's equation can be solved in there.

With Schwarz-Christoffel this simple structure, can be converted easily. Table 2.1 shows the relation between points in z-plane and w-plane as well as the relevant angle change [78].

Together with Eqn. (2.20) the simple defined structure leads to

$$\frac{dz}{dw} = \frac{C}{\sqrt{w-1}\sqrt{w+1}} \tag{2.39}$$

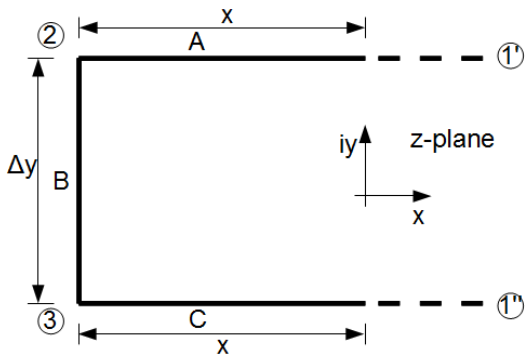


Figure 2.6: Basic element as transformed from z-plane to w-plane to solve Poisson's equation.

Table 2.1: Definition of the points of the basic element transformed by Schwarz-Christoffel

n	w_n	z_n	$\pi\gamma_n$	γ_n
1	$\pm\infty$	$+\infty$	$+\pi$	$+1$
2	-1	z_2	$+\frac{\pi}{2}$	$\frac{1}{2}$
3	$+1$	z_3	$+\frac{\pi}{2}$	$\frac{1}{2}$

and after integration

$$z = f(w) = 2C \cdot \ln\left(\sqrt{w-1} + \sqrt{w+1}\right) + D \tag{2.40}$$

For D is chosen 0, because the absolute coordinates are not relevant. Constant C can be calculated by Eqn. (2.23):

$$z_1' - z_2'' = i\Delta y = i\pi C \qquad \Longleftrightarrow \qquad C = \frac{\Delta y}{x} \tag{2.41}$$

Now all parameters for the conformal mapping are solved.

To transform a boundary condition of a potential problem from the z-plane into the w-plane and for the transformation of the solution calculated in the w-plane back into the z-plane it is important to know the transformation function for a point on the boundary. Eqn. (2.40) gives the conformal

mapping function from z into w-plane

$$w = F(z) = \cosh\left(\frac{\pi z}{\Delta y}\right) \tag{2.42}$$

and the inverse function give the re-transformation. So, for the electrodes the solutions are:

$$\begin{aligned}
&\text{Electrode A:} && u(x) = w(x,0) = \cosh\left(\tfrac{\pi x}{\Delta y}\right) \\
&\text{Electrode B:} && u(y) = w(0,y) = \cos\left(\tfrac{\pi y}{\Delta y}\right) \\
&\text{Electrode C:} && u(x) = w(x,\Delta y) = -\cosh\left(\tfrac{\pi x}{\Delta y}\right)
\end{aligned} \tag{2.43}$$

Chapter 3

Single Gate Bulk MOSFET

In this chapter a modelling approach for a Single Gate bulk MOSFET is presented.

The basic idea of the model is to define a rectangular area from the pinch-off to the drain region wherein Poisson's equation is solved in 2D. The area includes the oxide as shown as gray rectangle in Figure 3.1. The oxide is drawn in brown and the inversion charge in blue.

For this approach the Poisson equation is solved in 2 dimensions. After that the equation is decomposed in an 1D Poisson and a homogeneous 2D Laplacian part. From here the 2D Laplacian is transformed with conformal mapping

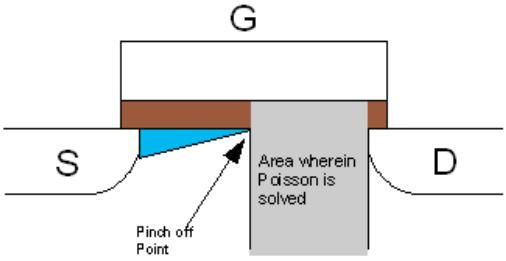


Figure 3.1: Structure of the bulk single gate MOSFET as used in this approach. The oxide is drawn in brown and the inversion charge in blue. Area wherein Poisson is solved in gray.

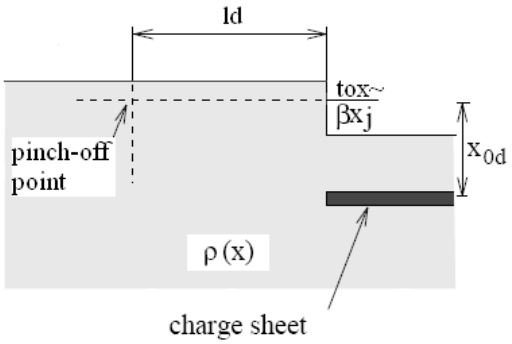


Figure 3.2: Cut-out of the region wherein Poisson is solved with the space charge region and charge sheets.

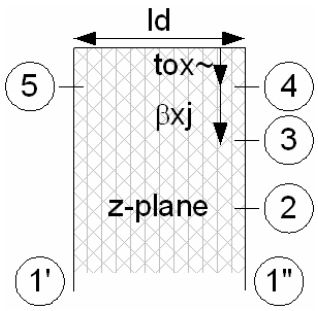


Figure 3.3: Rectangle area wherein Poisson is solved in the z-plane with numbered points for the charge sheets and corners.

technique in w-plane. Now the 2D Laplacian can be solved and retransformed in z-plane. As a last step this solution must be re-superpositioned with the 1D Poisson particular solution to receive the final solution as shown in Figure 3.5.

Figure 3.1 to Figure 3.4 show the chosen area wherein Poisson equation is solved. Figure 3.1 shows where the structure is located in the MOSFET.

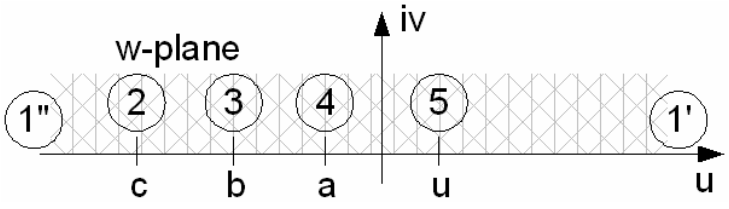


Figure 3.4: Rectangle area wherein Poisson is solved transformed into upper w-plane. All point lay on the u-axis.

Figure 3.2 shows the cut-out with the charge sheets and the space charge. The charge sheets are explained in section 3.3. In Figure 3.3 is shown the cut-out in z-plane with all important points. Finally in Figure 3.4 is the same region shown conformally mapped in w-plane. All point lay on the u-axis.

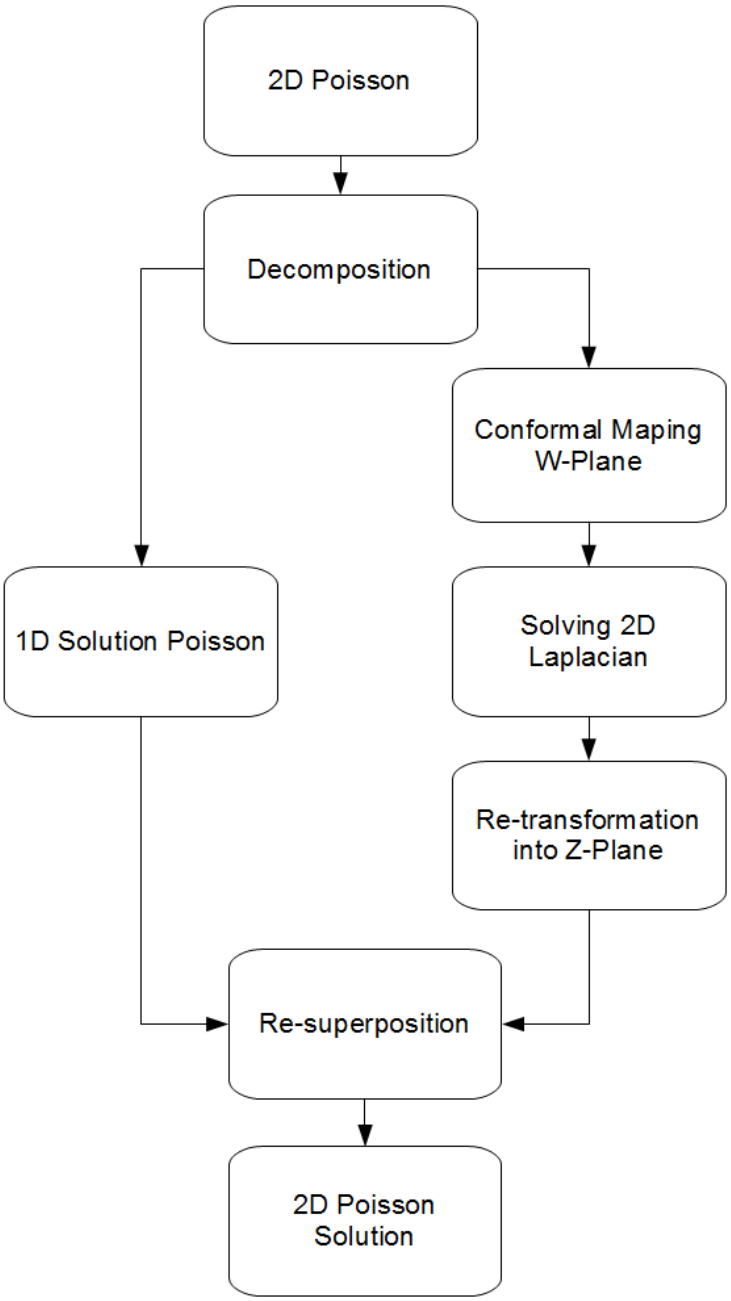


Figure 3.5: Strategy to Solve 2D Poisson

3.1 Decomposition of Poisson's Equation

As mentioned before the conformal mapping technique is limited to two dimensional systems and the Laplace equation. In this case the problem is 2D; nevertheless the Poisson includes the space charge density, see section 2.1. By decomposing the equation the space charge can be neglected. However the effect of the space charge has to be added later on again [84, 85, 86].

$$\Delta\Phi(x,y) = -\frac{\rho}{\epsilon} = \Delta\Phi_p(x) + \Delta\varphi(x,y) \tag{3.1}$$

Whereby the decomposed parts are

$$\Delta\Phi_p(x) = -\frac{\rho(x)}{\epsilon} \qquad \text{and} \qquad \Delta\varphi(x,y) = 0 \tag{3.2}$$

which leads to

$$\varphi(x,y) = \Phi(x,y) - \Phi_p(x) \tag{3.3}$$

3.2 Simplification of Drain Region

In order to get an analytical closed-form of the solution the drain region needs to be modified to simplify the geometry with a rectangular approximation. For that the pn junction in drain region is considered as elliptic:

$$\left(\frac{\gamma x_j}{\alpha x_j}\right)^2 + \left(\frac{\beta x_j}{x_j}\right)^2 = 1 \tag{3.4}$$

Whereby α is a technological factor, which describes the relation between overlap or diffusion and channel region. While fitting an rectangle into the elliptical pn-junction the connection point I appears as shown in Fig. 3.6.

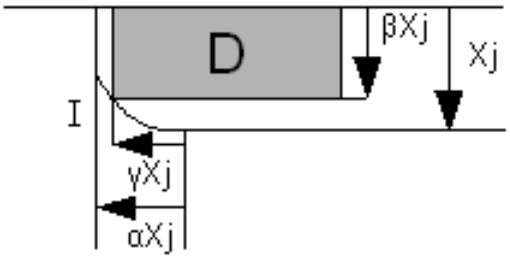


Figure 3.6: Simplification of the drain region

Following that condition is

$$\gamma = \alpha\sqrt{1-\beta^2}. \tag{3.5}$$

Assuming parameter β has a range between 0 and 1, the connection point of the rectangle follows the border of the ellipse. Is $\beta > 1$ the channel length is longer

$$L' = L + 2x_j\left(\alpha - \gamma\right), \tag{3.6}$$

3.3 Charge Sheets

In Fig. 3.7 a charge sheet is introduced underneath the drain region. With the before introduced decomposition strategy, a one-dimensionally distributed depletion region is necessary. At drain end this is not the case, because of the different depth of the depletion region. By extending the depletion charge into the entire substrate, the depletion charge would be one-dimensional. In order to capture the 2-dimensionally effect of the depletion charge, it is necessary to introduce a charge sheet.

The charge sheet represents part of the depletion charge and is at the position when the 1D partial solution and the 2D Poisson's solution have the same value. As a result the 2D Laplacian is 0, see Fig. 3.8. The distance between charge sheet and drain region is wide enough to avoid interference.

The advantage is, that the 2-dimensionally influence of the depletion region can be covered [78], [82], [50], [87] and [88], [89].

3.4 Boundary Conditions of the Basic Element

The applied boundary conditions along the electrodes A, B and C (indicated by blue letters) are shown in Fig. 3.7. The 2D Poisson solution Φ_k and Φ_d and 1D particular solution Φ_p (both sides the same). Electrode B is zero. These conditions were chosen with respect to the already introduced strategy [90], [91].

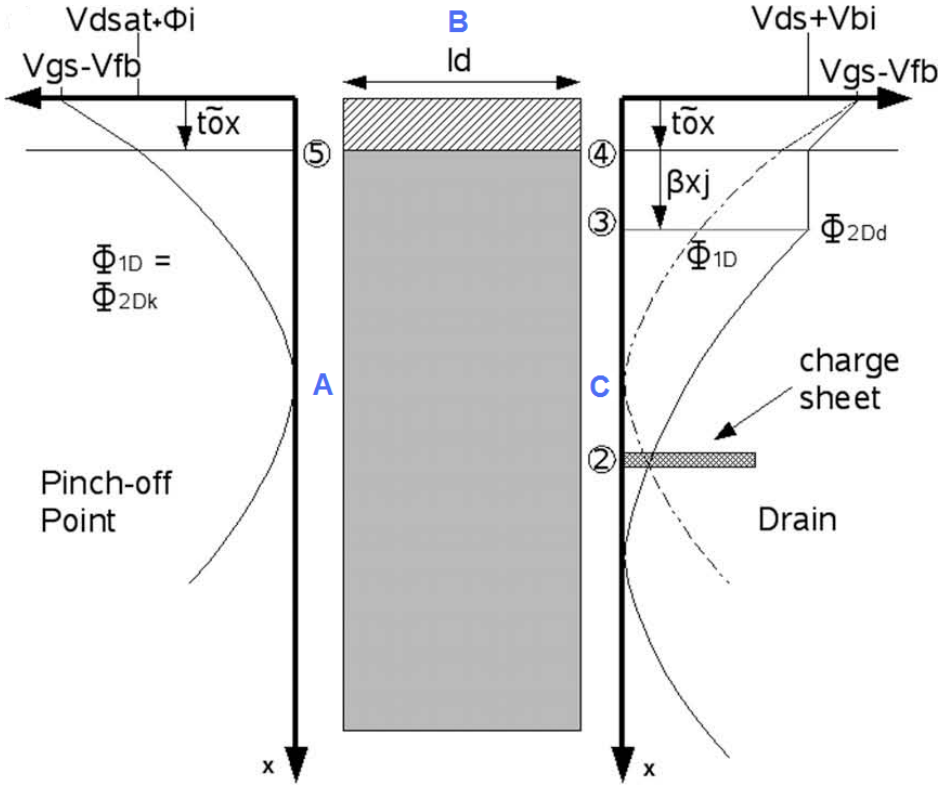


Figure 3.7: Boundary conditions of the basic element; 2D Poisson solution Φ_k (electrode A) and Φ_d (electrode C) and 1D particular solution Φ_p (both sides the same). Electrode B is zero.

3.4.1 Solution of Parabolically Shaped Boundaries

The basic boundary conditions along the electrodes A and C are parabolically shaped in Fig. 3.7 or as special case linear functions

$$\varphi = B_1 x^2 + B_2 x + B3 \tag{3.7}$$

From that the differential in the z-plane is

$$\frac{d\varphi}{dx} = 2 \cdot B_1 x + B_2. \tag{3.8}$$

Transformed into w-plane:

$$\left.\frac{d\varphi}{du}\right|_{\bar{u}} = \left(2 \cdot B_1 \bar{x}(\bar{u}) + B_2\right) \left.\frac{\partial x}{\partial u}\right|_{\bar{u}} \tag{3.9}$$

For the electric field between the point a and b this equation must be put into Eqn. (2.29):

$$\mathcal{E}_{\perp a,b}(u) = \frac{1}{\pi} \left|\frac{dw}{dz}\right| \int_{ua}^{ub} \left(2 \cdot B_1 \bar{x}(\bar{u}) + B_2\right) \left.\frac{\partial x}{\partial u}\right|_{\bar{u}} \frac{d\bar{u}}{u - \bar{u}}. \tag{3.10}$$

To come to a closed-form solution the equation (2.43)

$$\bar{x}(\bar{u}) = \frac{\Delta y}{\pi} \operatorname{arccosh}(\bar{u}) \tag{3.11}$$

must be replaced by an series expression $\exp(x) = \sum_{k=0}^{\infty} \frac{x^k}{x!}$. The corresponding function is

$$\bar{u} \cosh\left(\frac{\pi \bar{x}}{\Delta y}\right) = \frac{1}{2}\left(\exp\left(\frac{\pi \bar{x}}{\Delta y}\right) + \exp\left(-\frac{\pi \bar{x}}{\Delta y}\right)\right) = \frac{1}{2} \sum_{k=0}^{\infty} \left(1 + (-1)^k\right) \frac{1}{k!} \frac{\pi \bar{x}}{\Delta y}. \tag{3.12}$$

3.4.1.1 1. Approximation

For a first good approximation three elements of (3.12) are necessary

$$\bar{u} \approx \frac{1}{2}\left(2+\left(\frac{\pi\bar{x}}{\Delta y}\right)^2\right) = 1+\frac{1}{2}\left(\frac{\pi\bar{x}}{\Delta y}\right) \quad \Longrightarrow \quad \bar{x}(\bar{u}) \approx \frac{\Delta y}{\pi}\sqrt{2\left(\bar{u}-1\right)} \tag{3.13}$$

3.4.1.2 2. Approximation

A better approximation are four elements

$$\bar{u} \approx \frac{1}{2}\left(2+\left(\frac{\pi\bar{x}}{\Delta y}\right)^2+\frac{1}{12}\left(\frac{\pi\bar{x}}{\Delta y}\right)^4\right) \quad \Longrightarrow \quad \sqrt{24\left(\bar{u}-1\right)} \approx \frac{\pi\bar{x}}{\Delta y}\sqrt{12+\left(\frac{\pi\bar{x}}{\Delta y}\right)^2} \tag{3.14}$$

Now replacing $\left(\frac{\pi\bar{x}}{\Delta y}\right) \approx 2\left(\bar{u}-1\right)$ from Eqn. (3.13)

$$\sqrt{24\left(\bar{u}-1\right)} \approx \frac{\pi\bar{x}}{\Delta y}\sqrt{12+2\bar{u}-2} \tag{3.15}$$

That equation leads later on to some important simplifications.

In [78] is done an error estimation about this approximation. For realistic devices with a the potential solution $\frac{\bar{x}}{\Delta y} \leq 1$ the second approximation of Eqn. (3.13) leads to an error of maximum 12%.

Assemble Eqn. (3.10) with Eqn. (3.15):

$$\mathcal{E}_{\perp a,b}(u) = \frac{1}{\pi}\sqrt{1-u^2}\int_{ua}^{ub}\left(2\sqrt{3}B_1\frac{\Delta y}{\pi}\sqrt{\frac{\bar{u}-1}{\bar{u}+5}}+B_2\right)\frac{d\bar{u}}{(u-\bar{u})\sqrt{\bar{u}-1}\sqrt{\bar{u}+1}} \tag{3.16}$$

The result can be split up in two parts

$$\mathcal{E}_{\perp a,b}(u) = g(u,u_a,u_b,B_1)+h(u,u_a,u_b,B_2). \tag{3.17}$$

This equation gives the possibility to solve 2D Poisson by put in the Laplacian conditions. The two part are

$$g(u,u_a,u_b,B_1) = 2\sqrt{3}B_1\frac{\Delta y}{\pi}\sqrt{\frac{\bar{u}-1}{\bar{u}+5}}\cdot \\ \ln\left(\frac{uu_b+3(u+u_b)+5+\sqrt{(u^2+6u+5)(u_b^2+6u_b+5)}}{uu_a+3(u+u_a)+5+\sqrt{(u^2+6u+5)(u_a^2+6u_a+5)}}\frac{u_a-u}{u_b-u}\right) \tag{3.18}$$

and

$$h(u,u_a,u_b,B_2) = \frac{B_2}{\pi}\left(\arcsin\left(\frac{u_bu-1}{u-u_b}\right)-\frac{u_au-1}{u-u_a}\right) \tag{3.19}$$

3.4.2 Boundary Condition Along A

The basic approach for the boundary conditions along electrode A is

$$\varphi_k = \Phi_k - \Phi_p. \tag{3.20}$$

For the particular 1D solution Φ_p it is necessary to define a a boundary condition through the oxide ($0 \le x < t_{ox}^{\sim}$) and through the channel region ($t_{ox}^{\sim} \le x$),

$$\Phi_p = \begin{cases} V_{gs} - V_{fb} - \frac{V_{gs}-V_{fb}-V_{dsat}-\phi_i}{t_{ox}^{\sim}}\cdot x & \text{for } 0 \le x < t_{ox}^{\sim}, \\ V_{dsat}+\phi_i+V_{sb}+\frac{qN_B}{2\epsilon_0\epsilon_{Si}}\left(x-t_{ox}^{\sim}\right)^2-\mathcal{E}_{0k}\left(x-t_{ox}^{\sim}\right) & \text{for } t_{ox}^{\sim} \le x. \end{cases} \tag{3.21}$$

The gate-source voltage is V_{gs}, V_{fb} is the flatband voltage, V_{dsat} is the saturation voltage. The inversion potential is represented by ϕ_i and the transformed oxide thickness by $t_{ox}^{\sim}$. q is the elementary charge and the (in this case) donor acceptor concentration is N_B.

The electric field $\mathcal{E}_{0k}$ comes from the first derivation at beginning of each part. The first part through the oxide of the particular solution is a linear function, so there is no need to add this field. The second part is a

parabolically shaped function with

$$\mathcal{E}_{0k} = \frac{\frac{1}{C_{ox}}\sqrt{2\epsilon_0\epsilon_{Si}qN_B}}{\epsilon_0\epsilon_{Si}} \cdot C_{ox}\sqrt{V_{dsat}+\phi_i} \tag{3.22}$$

Along electrode A, the particular solution and the 2D Poisson solution are equal, $\Phi_p = \Phi_p$,

$$\Phi_k = \Phi_p = \begin{cases} V_{gs} - V_{fb} - \frac{V_{gs}-V_{fb}-V_{dsat}-\phi_i}{t_{ox}^{\sim}} \cdot x & \text{for } 0 \le x < t_{ox}^{\sim}, \\ V_{dsat} + \phi_i + V_{sb} + \frac{qN_B}{2\epsilon_0\epsilon_{Si}}\left(x - t_{ox}^{\sim}\right)^2 - \mathcal{E}_{0k}\left(x - t_{ox}^{\sim}\right) & \text{for } t_{ox}^{\sim} \le x. \end{cases} \tag{3.23}$$

Therefore,

$$\varphi_k = \Phi_k - \Phi_p = 0. \tag{3.24}$$

3.4.3 Boundary condition along B

The boundary condition on top of the oxide at the gate material - gate oxide interface is

$$\Phi_g = V_{gs} - V_{fb}. \tag{3.25}$$

When subtracting the particular solution at position $x = 0$,

$$\Phi_k|_{x=0} = V_{gs} - V_{fb} \tag{3.26}$$

the resulting boundary condition is

$$\varphi_g = \Phi_k - \Phi_g = 0. \tag{3.27}$$

3.4.4 Boundary condition along C

The same basic approach as for electrode A is used for electrode C,

$$\varphi_d = \Phi_d - \Phi_p. \tag{3.28}$$

The particular 1D solution Φ_p has to be always the same,

$$\Phi_p = \begin{cases} V_{gs} - V_{fb} - \frac{V_{gs}-V_{fb}-V_{dsat}-\phi_i}{t_{ox}^{\sim}} \cdot x & \text{for } 0 \leq x < t_{ox}^{\sim}, \\ V_{dsat} + \phi_i + V_{sb} + \frac{qN_B}{2\epsilon_0\epsilon_{Si}} \left(x - t_{ox}^{\sim}\right)^2 - \mathcal{E}_{0k} \left(x - t_{ox}^{\sim}\right) & \text{for } t_{ox}^{\sim} \leq x. \end{cases} \tag{3.29}$$

On the drain end, the 2D Poisson solution has to take the drain region into account ($t_{ox}^{\sim} \leq x < \beta x_j + t_{ox}^{\sim}$) and the charge sheet, located at depth x_d:

$$\Phi_d = \begin{cases} V_{gs} - V_{fb} - \frac{V_{gs}-V_{fb}-V_{ds}-V_{bi}}{t_{ox}^{\sim}} \cdot x & \text{for } 0 \leq x < t_{ox}^{\sim}, \\ V_{ds} + V_{bi} + V_{sb} & \text{for } t_{ox}^{\sim} \leq x < \beta x_j + t_{ox}^{\sim}, \\ V_{ds} + V_{bi} + V_{sb} + \frac{qN_B}{2\epsilon_0\epsilon_{Si}} \left(x - \beta x_j - t_{ox}^{\sim}\right)^2 \cdots & \\ \cdots - \mathcal{E}_{0d} \left(x - \beta x_j - t_{ox}^{\sim}\right) & \text{for } \beta x_j + t_{ox}^{\sim} \leq x < x_d, \\ \Phi_p(x) & \text{for } x_d \leq x. \end{cases} \tag{3.30}$$

The build-in voltage is given by V_{bi}, the drain source voltage by V_{ds}. Again an electric field is introduced when leaving the drain junction into the channel with

$$\mathcal{E}_{0d} = \frac{\frac{1}{C_{ox}}\sqrt{2\epsilon_0\epsilon_{Si}qN_B}}{\epsilon_0\epsilon_{Si}} \cdot C_{ox}\sqrt{V_{ds} + V_{bi} + V_{sb}}. \tag{3.31}$$

To define the position x_d of the charge sheet

$$x_d = \frac{\frac{qN_B}{2\epsilon_0\epsilon_{Si}}\beta x_j + \mathcal{E}_{0d} + V_{ds} + V_{bi} + V_{sb} - V_{dsat} - \phi_i}{\frac{qN_B}{2\epsilon_0\epsilon_{Si}}\beta x_j + \mathcal{E}_{0d} - \mathcal{E}_{0k}} \tag{3.32}$$

is used.

Since electrode A and B are defined to be 0, only electrode C needs to be solved. The estimated solution is drawn in Fig. 3.8.

As first the important points needs to be transformed. The upper right corner of the structure is defined as 0 point in z-plane, which is the point 1

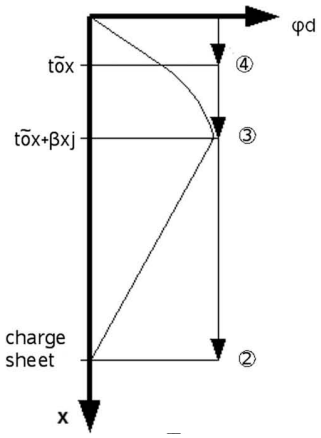


Figure 3.8: Resulting Laplacian φ_d boundary conditions for electrode C.

in w-plane. The end of the oxide, marked as point ④ in Fig. 3.7 is

$$a = \cosh\left(\frac{\pi t_{ox}^{\sim}}{ld}\right). \tag{3.33}$$

The end of the drain region, marked with ③ is

$$b = \cosh\left(\frac{\pi\left(\beta xj + t_{ox}^{\sim}\right)}{ld}\right). \tag{3.34}$$

And the position of the charge sheet ② is

$$c = \cosh\left(\frac{\pi\left(x_d + t_{ox}^{\sim}\right)}{ld}\right). \tag{3.35}$$

As last the point at the position where the electric field should be calculated must be chosen. In this case it is the point ⑤ at the Si-SiO2 interface at the pinch-off point side

$$u = -\cosh\left(\frac{\pi t_{ox}^{\sim}}{ld}\right). \tag{3.36}$$

In a next step the parameters need to be placed in equation (3.18) and (3.19).

The first part goes from 0 in z-plane to the Si-SiO2 interface and is linearly

shaped as shown in Fig. 3.8 on the previous page. Therefore:

$$\mathcal{E}_1 = h\left(u, 1, a, \frac{V_{ds} + V_{bi} - V_{dsat} - \phi_i}{t_{ox}^{\sim}}\right) \tag{3.37}$$

The second part goes from the Si-SiO2 interface to the end of the drain junction and is parabolically shaped

$$\mathcal{E}_2 = g\left(u, a, b, -\frac{qN_B}{\epsilon_0\epsilon_{Si}}\right) + h\left(u, a, b, \mathcal{E}_p + \frac{qN_B}{\epsilon_0\epsilon_{Si}}t_{ox}^{\sim}\right) \tag{3.38}$$

The third part goes from the end of the drain junction to the charge sheet and is linearly shaped

$$\mathcal{E}_3 = h\left(u, b, c, \mathcal{E}_p - \mathcal{E}_d - \frac{qN_B}{\epsilon_0\epsilon_{Si}}\beta x_j\right) \tag{3.39}$$

From all parts the electric field with a real and an imaginary part is given. In the pinch-off point is only the lateral electric field of interest. Therefore the imaginary part of all three solutions are re-superpositioned.

$$\mathcal{E}_k = \mathcal{E}_1 + \mathcal{E}_2 + \mathcal{E}_3 \tag{3.40}$$

It is not necessary to calculate an electric field from the 1D particular solution, because it has only a vertical component [91].

3.5 Calculation of the Channel Length Shortening

As described before it is possible to calculate the electric field at the pinch-off point in a analytical closed-form. To come from the electric field to the actual channel length shorting it necessary to know the electric field at that point and vary the length until this value is reached [90].

With the fit parameter $\mathcal{E}_p$, the electric field at the pinch-off point, the

model gets a start condition to calculate the saturation voltage at pinch-off point [31], [92]

$$V_{dsat} = \frac{V_{ge} + L\mathcal{E}_p}{\frac{\mathcal{E}_p}{\mathcal{E}_c} - 1} \left(\sqrt{1 + \frac{2V_{ge}L\mathcal{E}_p\left(\frac{\mathcal{E}_p}{\mathcal{E}_c} - 1\right)}{\left(V_{ge} + L\mathcal{E}_p\right)^2}} - 1 \right) \tag{3.41}$$

with

$$V_{ge} = \frac{V_{gs} - V_{th}}{\alpha_i}. \tag{3.42}$$

The channel length is given by L and the critical electric field by $\mathcal{E}_c$. V_{gs} is the gate-source voltage. As threshold model for V_{th} is used a 2D closed-form model with conformal mapping technique from [78]. The body factor α_i can be calculated by

$$\alpha_i = 1 + \frac{1}{C_{ox}\sqrt{2\epsilon_0\epsilon_{Si}qN_B}2\sqrt{\phi_i + V_{sb}}} \cdot \left(1 - \frac{1}{1.744 + 08634\left(\phi_i + V_{sb}\right)}\right). \tag{3.43}$$

For the model must $V_{dsat} \leq V_{ds}$, which can be done by a smoothing function with $Ats = 10$:

$$V_{dsat-model} = V_{dsat} - V_{dsat}\frac{\log\left(1 + \exp\left(Ats \cdot \left(1 - \frac{V_{ds}}{V_{dsat}}\right)\right)\right)}{\log\left(1 + \exp\left(Ats\right)\right)} \tag{3.44}$$

While applying an constant electric field at pinch-off point, the model always over predicted the channel length shortening l_d. Using Eqn. (3.41) the saturation voltage is calculated independently of the applied V_{ds}. With increasing drain-source voltage the pinch-off point moves source-wards. Keeping V_{dsat} at pinch-off point still constant the electric field $\mathcal{E}_p$ has to increase. To include this effect in the model, the electric field is recalculated and receives a V_{dsat} and V_{ds} dependency. With increasing V_{dsat} and V_{ds} the electric field at pinch-off point increases in this approach. The 2D model for the channel length shortening became with $\mathcal{E}_p(V_{dsat}, V_{ds})$ more accurate [91].

With the initial electric field $\mathcal{E}_p$ is calculated a V_{dsat}. From that an I_{ds}

model is used which avoids the explicit calculation of the channel length shortening l_d and need no special mobility model in GCA [78], [87]. Because it is a first order approximation, this model does not predict the output conductance precisely. For that it is no substitute for a current equation taking into account a channel length shortening.

$$I_{dsat} = \frac{\mu_0 C_{ox} W}{L + \frac{\mu_0}{v_{sat}} V_{ds}} \left(\left(V_{gs} - V_{th} - \frac{1}{\alpha_i} V_{dsat} \right) V_{dsat} + \left(V_{gs} - V_{th} - \alpha_i V_{dsat} \right) \left(V_{ds} - V_{dsat} \right) \right) \tag{3.45}$$

While setting the current obtained by (3.45) equal to the current at pinch-off point

$$I_{dsat} = \mu_0 C_{ox} W \frac{\mathcal{E}_p}{1 + \frac{\mathcal{E}_p}{\mathcal{E}_c}} \left(V_{gs} - V_{th} - \alpha_i V_{dsat} \right) \tag{3.46}$$

a closed-form equation results to recalculate the electric field $\mathcal{E}_p$ as function of V_{dsat} and V_{ds}:

$$\mathcal{E}_{p-model} = \frac{-v_{sat}\mathcal{E}_c(\alpha_i V_{dsat}^2 + 2V_{gs}V_{ds-model}(1 - V_{th}) - 2\alpha_i V_{dsat}V_{ds-model})}{2\mathcal{E}_c(Lv_{sat}(V_{th} - V_{gs}) + \mu_{eff}V_{ds-model}(V_{th} - V_{gs}))} \frac{1}{+2\mathcal{E}_c\alpha_i V_{dsat}(Lv_{sat} + \mu_{eff}V_{ds-model})} \frac{1}{+v_{sat}\alpha_i V_{dsat}^2 + 2v_{sat}V_{ds-model}(V_{gs} - V_{th} - \alpha_i V_{dsat})} \tag{3.47}$$

3.6 Results

In this chapter the results of the model are compared to simulation results of TCAD Sentaurus [10]. In that simulations a drift-diffusion model with high field saturation is used. To compare the simulation results with the model,

Table 3.1: Parameters of the simulated MOSET.

Parameter	Value
channel width	100nm
oxide thickness	7nm
substrate doping concentration	10^{16}cm^{-3}
source drain doping profile	Gauss
max. source/drain doping concentration	10^{20}cm^{-3}

the model for l_d is put into a simple current equation

$$I_{ds} = \frac{\mu C_{ox} W}{L - ld + \frac{\mu}{v_{sat}} V_{dss}} \left(V_{gs} - V_{th} - \frac{\alpha}{2} V_{dss} \right) V_{dss} \tag{3.48}$$

In order to make that model continuous from sub to above threshold V_{dss} is a smooth value between V_{ds} and V_{dsat}

$$V_{dss} = V_{dsat} - V_{dsat} \frac{\log\left(1 + \exp\left(Ats \cdot \left(1 - \frac{V_{ds}}{V_{dsat}}\right)\right)\right)}{\log\left(1 + \exp\left(Ats\right)\right)} \tag{3.49}$$

with $Ats = 10$.

3.6.1 Channel Length Modulation for Long Channel Devices

With a modern fabrication process bulk MOSFETs with a channel length of 700nm down to 500nm can be easily produced. Here the model is compared to simulation results of devices with this channel length, whereby the junction depth x_j is varied. The size of the MOSFET is described in Table 3.1

3.6.1.1 Channel Length 500nm and Junction Depth 200nm

Figures 3.9 and 3.10 on the next page show the output characteristics and the output resistance for a channel length of 500nm and a junction depth of

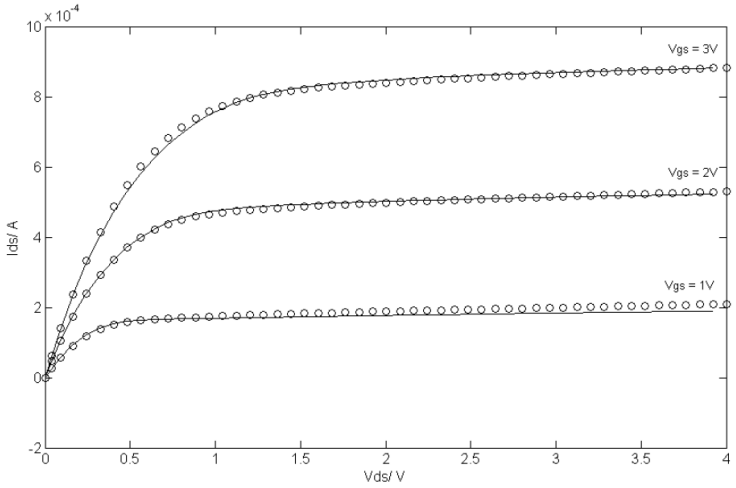


Figure 3.9: Output characteristics with a channel length of 500nm and an junction depth xj of 200nm; $\mathcal{E}_p = 10^5$V/cm; Model - lines; Simulation - symbols.

200nm. The total value of the output resistance is not that good predicted, however the relative variation of V_{ds} with respect to V_{gs} is accurately described. Fitting parameter $\mathcal{E}_p$ for the model is 10^5V/cm. The lines represent the model and the symbols the simulation results.

3.6.1.2 Channel Length 500nm and Junction Depth 100nm

In Figures 3.11 and 3.12 are shown the output characteristics and the output resistance for a channel length of 500nm and a junction depth of 100nm. Lines stand for the model and the symbols for the simulation results. The fitting parameter for the electric field in the pinch-off point $\mathcal{E}_p$ stayed unchanged. Compared to the results in Figures 3.9 and 3.10 the model gives better results.

3.6.1.3 Channel Length 700nm and Junction Depth 100nm

Output characteristics and the output resistance for a channel length of 700nm and a junction depth of 100nm are shown in Figures 3.13 and 3.14. The lines

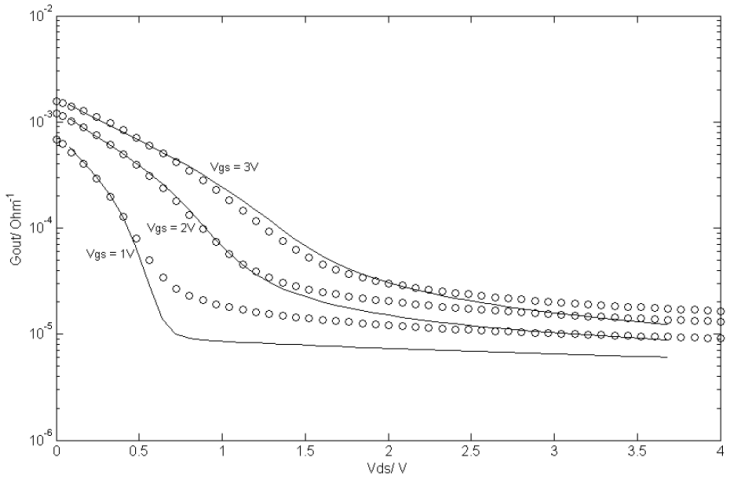


Figure 3.10: Output conductance with a channel length of 500nm and an junction depth xj of 200nm; $\mathcal{E}_p = 10^5$V/cm; Model - lines; Simulation - symbols.

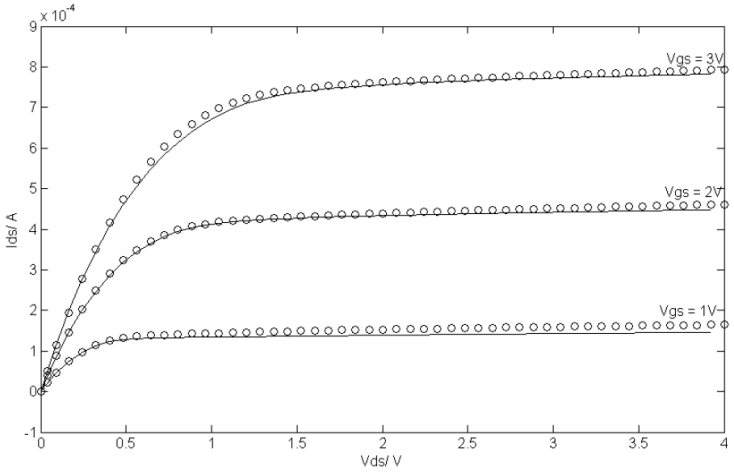


Figure 3.11: Output characteristics with a channel length of 500nm and an junction depth xj of 100nm; $\mathcal{E}_p = 10^5$V/cm; Model - lines; Simulation - symbols.

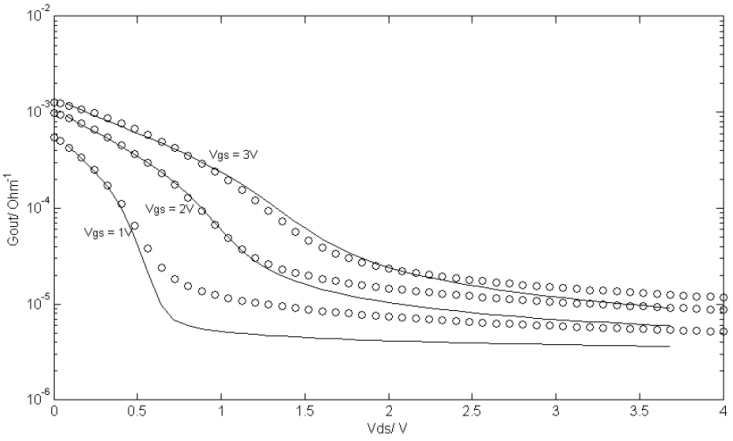


Figure 3.12: Output conductance with a channel length of 500nm and an junction depth xj of 100nm; $\mathcal{E}_p = 10^5$V/cm; Model - lines; Simulation - symbols.

represent the model and the symbols the simulation results. The predicted drain-source current looks very good. Also the total value for the output characteristics fit very well. Again the fitting parameter for the electric field in the pinch-off point stayed unchanged, which shows the good scalability of the model.

3.6.2 Channel Length Modulation for Short Channel Devices

In this section smaller device geometries are chosen. The effective channel length is here between 50nm and 100nm. Compared to the results in section 3.6.1 here the fitting parameter $\mathcal{E}_p$ changed to $2 \cdot 10^5$V/cm. Even so the field stays unchanged for 100nm and 50nm. This profs the second order influence of this fitting parameter and the very good scalability of the model.

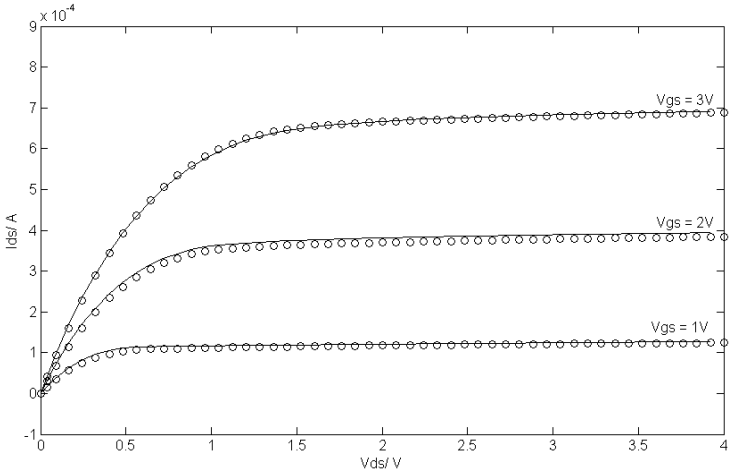


Figure 3.13: Output characteristics with a channel length of 700nm and an junction depth xj of 100nm; $\mathcal{E}_p = 10^5$V/cm; Model - lines; Simulation - symbols.

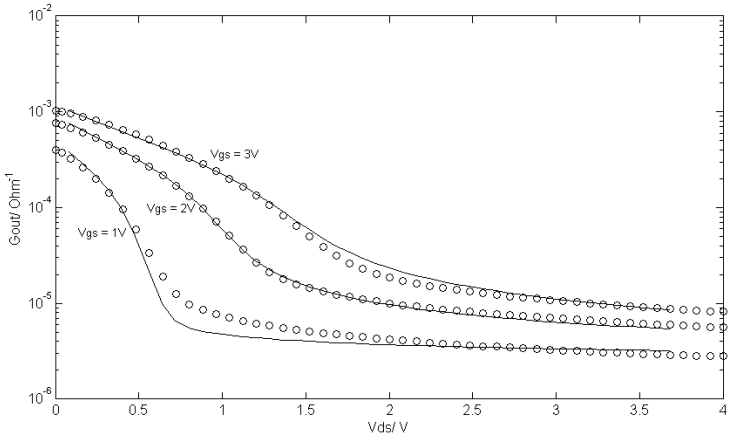


Figure 3.14: Output conductance with a channel length of 700nm and an junction depth xj of 100nm; $\mathcal{E}_p = 10^5$V/cm; Model - lines; Simulation - symbols.

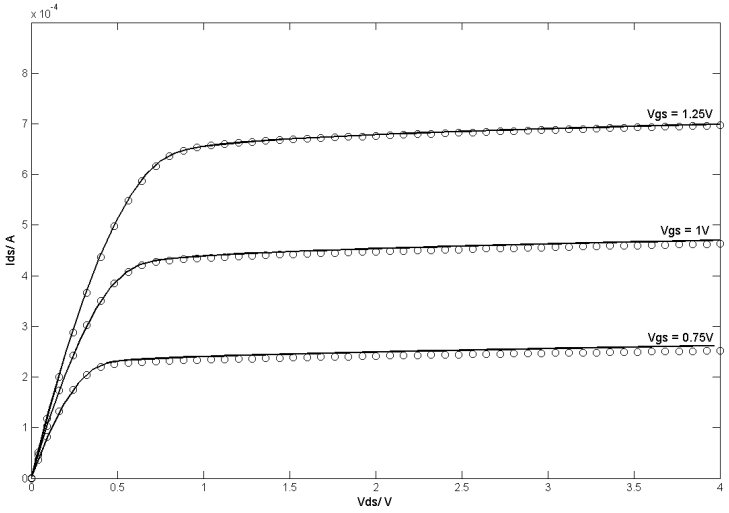


Figure 3.15: Output characteristics with a channel length of 100nm; $\mathcal{E}_p = 2 \cdot 10^5$V/cm; Model - lines; Simulation - symbols.

3.6.2.1 Channel Length 100nm

Figure 3.15 and 3.16 show the output characteristics and the output conductance of the model and the simulator [10]. Even the in Figure 3.16 described output conductance shows a very good behavior considered it is the first derivation of the output characteristics. For these results the drain-source resistance are taken into account by using

$$V_{ds} = V_{ds} - R_{ds} \cdot I_{ds}, \tag{3.50}$$

whereby R_{ds} was used as a fitting parameter.

3.6.2.2 Channel Length 50nm

In Figure 3.19 the by the model predicted channel length shortening of a bulk MOSFET with 50nm are given. As expected the model shows a fast increase while entering the saturation region. The output characteristics and the output conductance are shown in Figure 3.17 and 3.18. The model prognosticates the output conductance very precisely. Fitting parameter

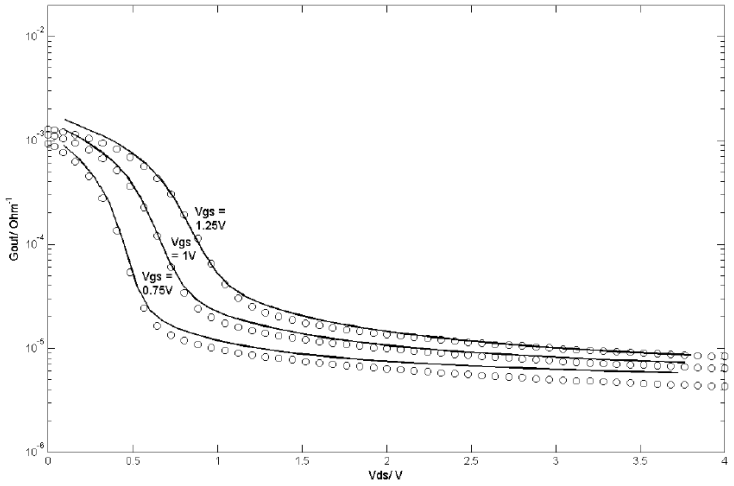


Figure 3.16: Output conductance with a channel length of 100nm; $\mathcal{E}_p = 10^5$V/cm; Model - lines; Simulation - symbols.

$\mathcal{E}_p = 2 \cdot 10^5$V/cm is the same as for 100nm channel length. Source-drain resistance are taken into account by

$$V_{ds} = V_{ds} - R_{ds} \cdot I_{ds}, \tag{3.51}$$

whereby R_{ds} was used as a fitting parameter.

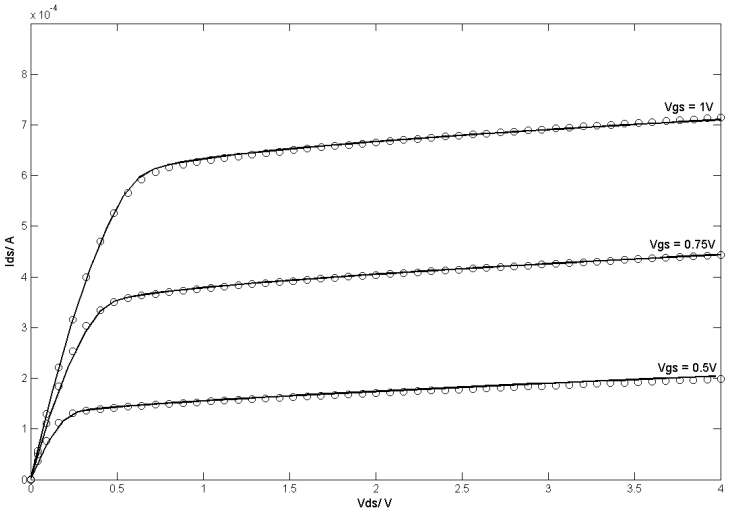


Figure 3.17: Output characteristics with a channel length of 50nm; $\mathcal{E}_p = 2 \cdot 10^5$V/cm; Model - lines; Simulation - symbols.

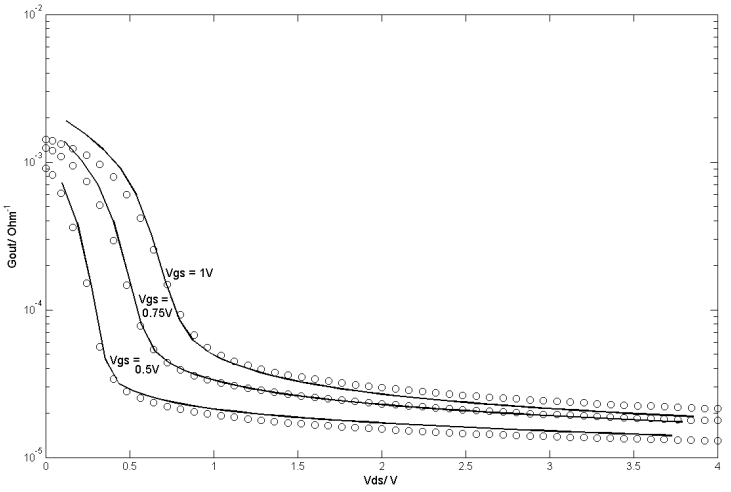


Figure 3.18: Output conductance with a channel length of 50nm; $\mathcal{E}_p = 2 \cdot 10^5$V/cm; Model - lines; Simulation - symbols.

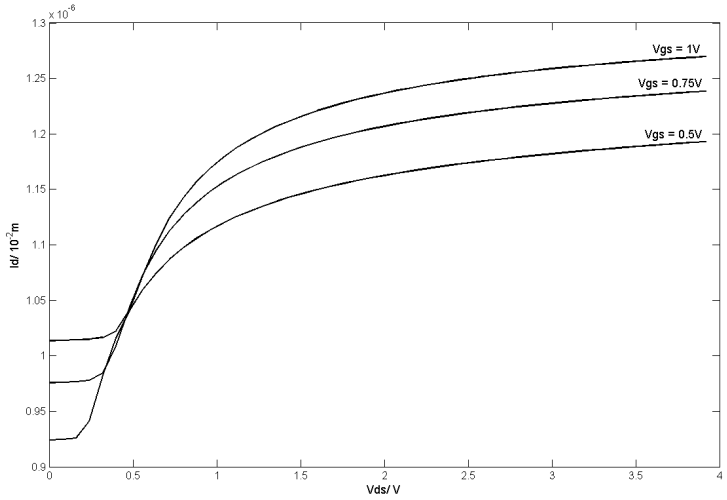


Figure 3.19: Predicted channel length shortening of the model with a channel length of 50nm of the Bulk MOSFET; $\mathcal{E}_p = 2 \cdot 10^5 \mathrm{V/cm}$.

Chapter 4

Symmetrically Biased Double Gate MOSFET

In this chapter the model for a symmetrically biased DoubleGate (DG) MOSFET is presented. For this a simple DG structure as shown in Fig. 4.1 was used. It has source and drain region attached an either side as well as two gates. The oxide, drawn in gray, has the thickness t_{ox} and the channel has the length L_{ch} and the width T_{ch}.

Both gates are biased with the same voltage in this chapter.

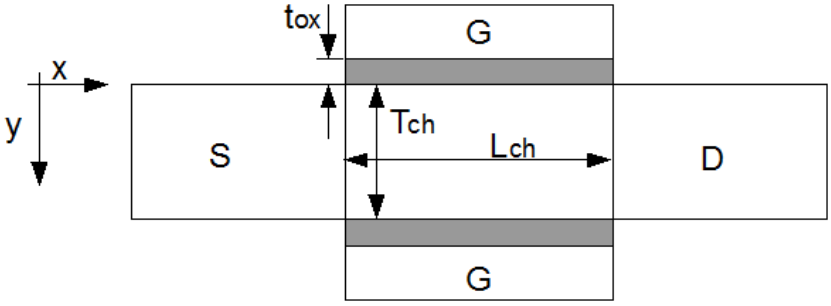


Figure 4.1: Simplified structure of a DG MOSFET as used in this approach. The oxide, drawn in gray, has the thickness t_ox and the channel has the length L_{ch} and the width T_{ch}.

4.1 Device Physics

As described in [39] and [93] for long channel devices or a low source-drain voltage in accumulation the electric field created by the electrons underneath the gate oxide dominates the device electrostatics. The influence of source-drain voltage is reduced with increasing gate voltage. With downscaling the device or increasing source-drain voltage this voltage begin to effect the device in accumulation. Like in standard single MOSFETs short channel effects take place as shown in Fig. 4.2.

Comparing the potential contour plot of a DG in strong inversion with no applied drain-source voltage (V_{ds}) to a device with applied drain-source voltage, the influence can be seen on the contour lines. For all plots source and drain region as well as the gate material are omitted. In Fig. 4.3 with no applied V_{ds} the contour lines are all symmetrical and straight for a short channel device with a channel thickness of 30nm and a channel length of 30nm. A long channel device can be assumed and a model for such can be applied. In Fig. 4.4, L_{ch} = 50nm and T_{ch} = 10nm, the contour lines are parabolically shaped due to the applied $V_{ds} = 1.4V$ and a $V_{gs} = 1V$. Also at the source side of the channel the contour lines are much more bended, whereby at the drain end the contour lines of the potential become straight again [94, 95]

Looking at the E-current density distribution within channel region, Fig. 4.5 of the same device, it shows underneath the gate oxide the channel as expected. Additionally the channel becomes smaller towards the drain end and suddenly there is no longer charge directly located underneath the gate oxide. Instead the charge is spread equally over the whole channel. This behavior is very similar to the pinch-off behavior of standard single gate MOSFETs.

Searching for the path of the electric potential maximum, the maximum is located at source end at both $Si - SiO_2$ interfaces. In Fig. 4.6 the path of

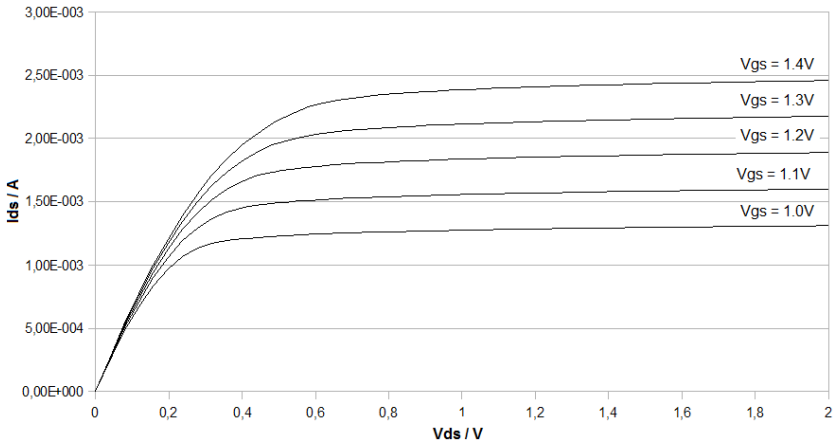


Figure 4.2: Drain-Source voltage vs. drain current for a DG MOSFET with $L_{ch} = 50$nm and $T_{ch} = 10$nm. After reaching saturation voltage, short channel effects take place.

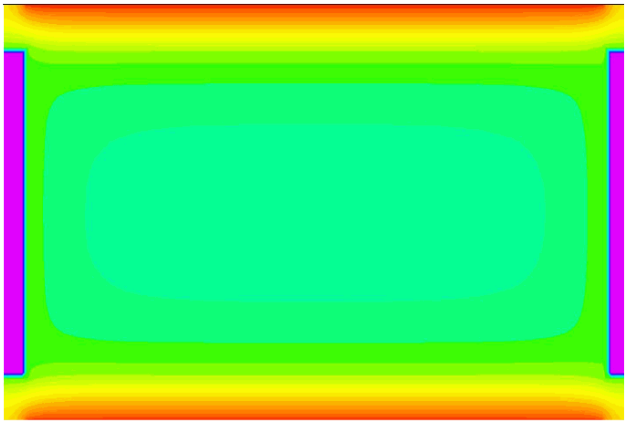


Figure 4.3: Potential contour plot showing strong inversion conditions for the double-gate device whereby $(V_{ds}) = 0$; Channel thickness of 30nm and a channel length of 30nm. The flat region close to the gates (red) indicates that long-channel modeling can be applied. The source and drain contacts in purple. [93]

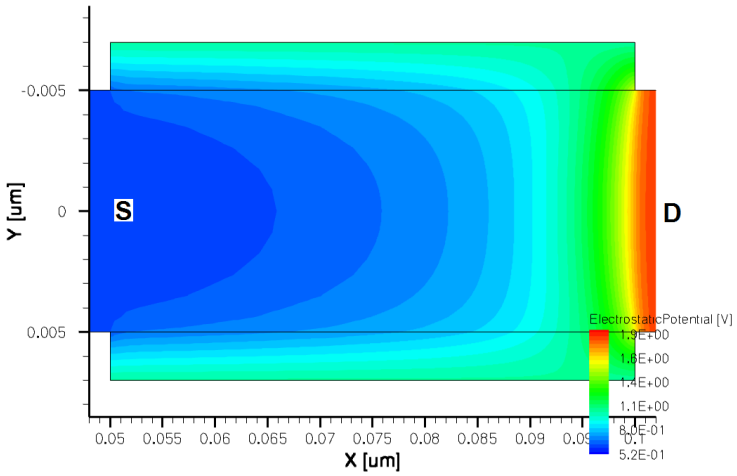


Figure 4.4: Electric potential distribution within channel region and gate oxide of DG MOSFET with an applied $V_{ds} = 1.4$V and $V_{gs} = 1$V, $L_{ch} = 50$nm and $T_{ch} = 10$nm. Drain and source region are cut out as well as the gate material.

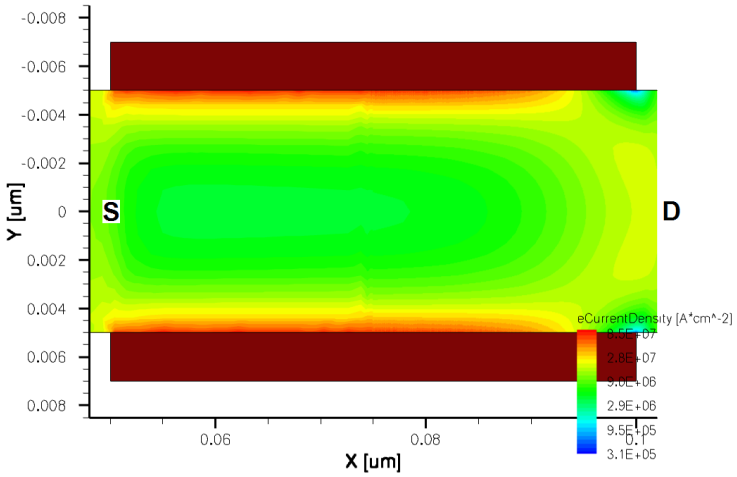


Figure 4.5: E-current density distribution within channel region and gate oxide of DG MOSFET with an applied $V_{ds} = 1.4$V and $V_{gs} = 1$V, $L_{ch} = 50$nm and $T_{ch} = 10$nm. Drain and source region are cut out as well as the gate material.

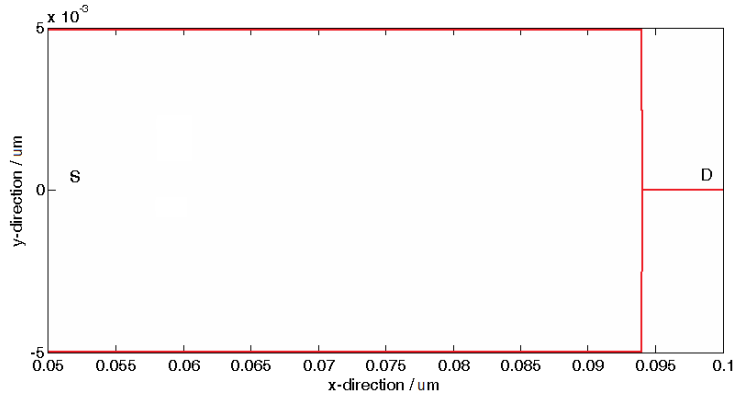


Figure 4.6: Path of the electric potential maximum along the channel drawn in red. $V_{ds} = 1.4$V and $V_{gs} = 1$V, $L_{ch} = 50$nm and $T_{ch} = 10$nm. Drain and source region are cut out as well as the gate material and oxide.

the electric potential maximum is drawn along the channel in red. Source and drain region, as well as the gate and gate oxides are omitted. Going in drain direction along the channel the maximum changes location from the gate oxide interface into the middle of the channel with a sudden move.

That point is defined as pinch-off point. After hitting this point the whole channel appears to be in saturation.

4.2 Model

The position of the saturation point is influenced by the gate voltage V_{gs} and the applied drain voltage V_{ds}. Of course manufacturing parameters, such as doping, influence the saturation point as well. However, during operation mostly V_{gs} and V_{ds} change and have a 2-dimensionally influence on the saturation point. Therefore a 2D approach to calculate the channel length shortening is necessary [96, 97].

The approach of solving an Poisson's equation system with conformal mapping technique is the same as in Fig. 3.5 in the previous section. For this

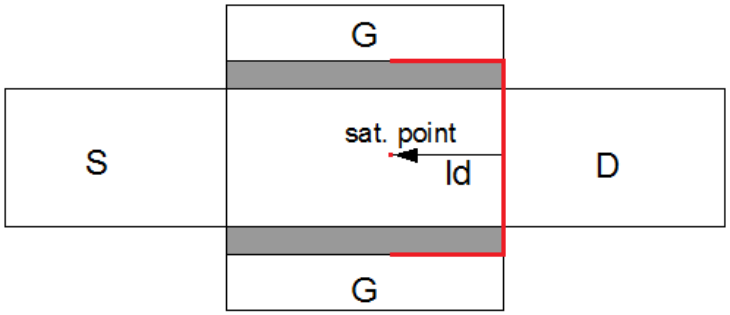


Figure 4.7: Definition of the area wherein 2D Poisson is solved in red lines. Th area has length l_d and includes both oxides.

approach the 2D Poisson solution is decomposed in a 1D Poisson solution and a 2D solution of a Laplacian part. In a next step conformal mapping technique was applied to the 2D Lapace equation. This equation is transformed into w-plane to find a solution easier. Afterwards a re-transform of everything back into z-plane was done and re-superpositioning with the 1D Poisson part. This results in a 2D Poisson solution.

The definition of the area, wherein 2D Poisson's equation is solved, is a 2-corner structure with a rectangular shape. It is drawn in Fig. 4.7 in red lines. This structure goes from the pinch-off point to the drain end and includes both silicon oxides. The length of the rectangle was defined as length l_d, what represents the channel length shortening. The 2-corner structure was chosen to simplify the mathematical effort to solve it.

Fig. 4.8 shows the cut out of the region wherein 2D Poisson is solved. The electric field goes simplified from the drain end in direction of the pinch-off point end. The E-field lines are drawn in a simplified way in straight lines. Initially the introduction of a 4-corner problem is necessary to define the saturation point boundary. Instead the 2-corner structure was mirrored to force an electrical field of 0 in the saturation point even if some E-field lines go into the direction of the gate, see Fig. 4.9. The electric field $Ep \neq 0$ at pinch off point will later be achieved by superposition with the 1D solution, which will be defined below. So, a quasi 4-corner structure was created. Since the structure is symmetrical only half of the problem needs to be solved,

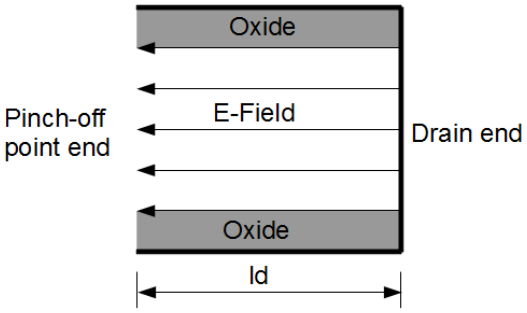


Figure 4.8: Cut-out of the rectangular shaped are in where 2D Poisson is solved. The E-field is drawn in simplified straight lines.

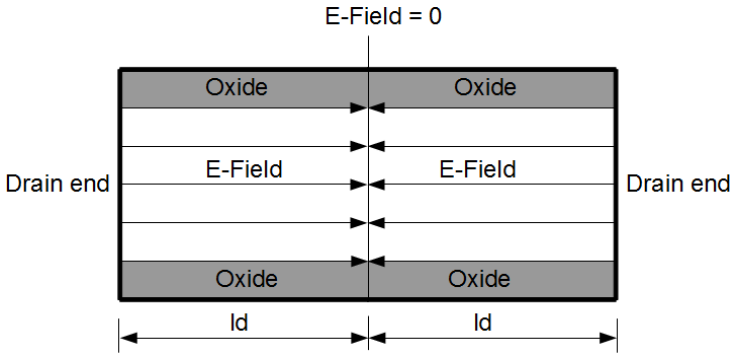


Figure 4.9: Mirroring of the area wherein 2D Poisson's equation is solved to create a quasi 4-corner structure. On both ends V_{ds}, therefore the electric field in the saturation point is 0.

which allows it to use conformal mapping technique with a 2-corner structure approach.

Along this structure several important points are marked, which are shown in Fig. 4.10. Then the structure was placed in a coordinate system and a practical origin for the structure was set, refer to Fig. 4.11. For that the structure was turned, to define the origin in the left lower corner. Nevertheless, actually a quasi 4-corner structure is solved as shown in Fig. 4.9. Finally the absolute coordinates for each point are defined.

- (1') lays in infinity.
- (2) gives the upper right end of the structure with the coordinates $\left(l_d | (T_{ch} + 2 \cdot t_{ox}^{\sim})\right)$.

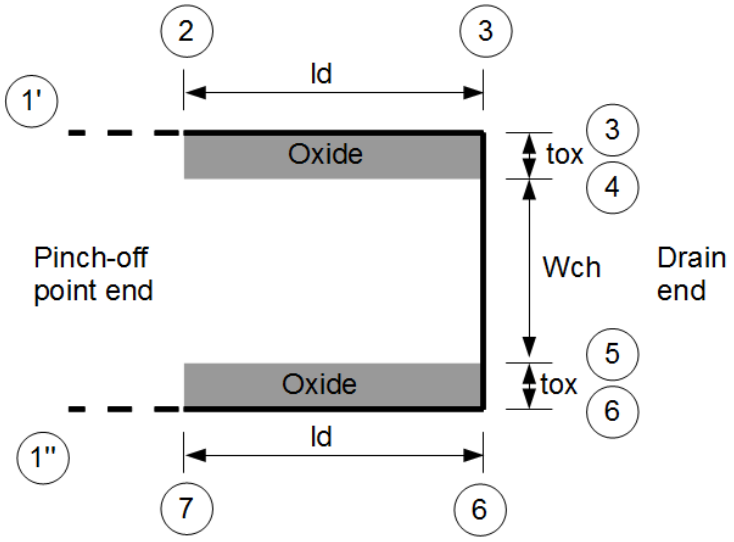


Figure 4.10: Several important points along the boundary of the area are marked.

- ③ is the left upper corner with the coordinates $\big(0|(T_{ch}+2\cdot t_{ox}^{\sim})\big)$.
- ④ represents the end of the upper oxide or the upper left end of the channel with $\big(0|(T_{ch}+t_{ox}^{\sim})\big)$.
- ⑤ represents the end of the lower oxide or the begin of the channel area with $\big(0|(t_{ox}^{\sim})\big)$.
- ⑥ is the origin of the structure with $\big(0|0)\big)$.
- ⑦ gives the lower right end of the structure with the coordinates $\big(l_d|0)\big)$.
- ①" lays in infinity.

4.2.1 Decomposition of Poisson's Equation

Considering a lightly doped device, no depletion charge $Q_{dep} \approx 0$ is assumed. So far a solution for Poisson's equation is needed in the high field saturation

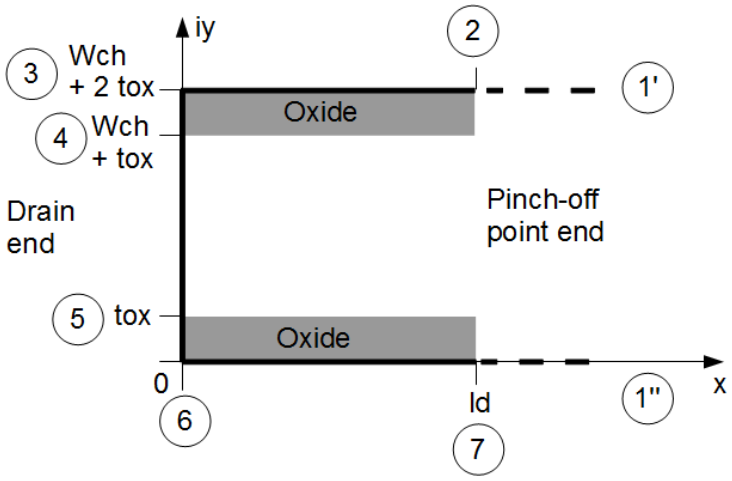


Figure 4.11: The area wherein 2D Poisson is solved is turned around and set into a (x, iy)-coordinate system to assign the points along the boundary with absolute coordinates.

region of the device. From the analyses of the device, the channel charge is neglected in this region and the inversion charge is assumed to be $Q_{inv} \approx 0$.

$$\Delta\Phi_{2D} = -\frac{\rho}{\epsilon} = -\frac{Q_{dep} + Q_{inv}}{\epsilon}. \tag{4.1}$$

With the above mentioned assumptions

$$\Delta\Phi_{2D} \approx 0. \tag{4.2}$$

is received.

So a 2D Laplacian problem is formed. Schwarz-Christoffel [75] can be used to solve the 2D problem in an analytical closed form by using a nonlinear conformal mapping technique.

When assuming in a standard single MOSFET, some formulation often overestimate the output conductance, which is mainly given by the channel length shortening effect. This is because the approaches often ignore the presence of the gate electrode and treat the field problem along the channel the same as that of an pn junction between the substrate and the drain regions

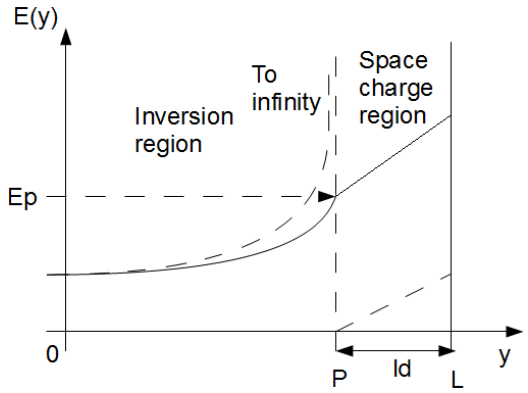


Figure 4.12: Electric field along the channel in a standard single gate MOSFET. Assuming field at a point P is infinite (very large) (dotted line) and finite value $\mathcal{E}_p$(continuous line) [101]

[98]. Further, simple approaches to calculate the output conductance result in a discontinuity of the field at saturation point $y = L - l_d$, [99], [100]. Assuming the electrical field at saturation point $\mathcal{E}_y = 0$ at the position $y = L - l_d$, a discontinuity of the field at that point is discovered [31]. That means also, that $Q_i = 0$ in the pinch-off region which means that at $y = L - l_d$, the field $\mathcal{E}_y$ becomes infinite, as shown in Fig. 4.12. According to Baum-Beneking [101] the discontinuity in the field at $y = L - l_d$ (or $y' = 0$) can be removed by removed by assuming that at the pinch-off point the saturation voltage is $V = V_{dsat}$ and the field is $\mathcal{E}_y = \mathcal{E}_p$ [101].

In the DG MOSFET the inversion charge in the space region is neglected when solving 2D Poisson's equation. Nevertheless for the basic idea of the model it is necessary to keep the inversion charge in mind.

In order to imprint the electrical field into the boundary conditions of the approach for solving the 2D Laplacian from Eqn. (4.2) is split up:

$$\Delta\Phi_{2D} = \Delta\varphi_{2D} + \Delta\phi_{1D}. \tag{4.3}$$

With that a possibility is given to include the electrical field $\mathcal{E}_p$ in the 1D Poisson solution, ϕ_{1D}. The electric field in the high field saturation region is constant, which results in a linearly shaped voltage as assumed in Fig. 4.12.

As basic approach a voltage is defined, that is depending on l_d and $\mathcal{E}_p$,

$$V_{d'} = ld \cdot \mathcal{E}_p + V_{gs} - V_{fb}. \tag{4.4}$$

The flatband voltage is V_{fb} and V_{gs} is the gate source voltage.

With this the 1D solution of Poisson equation is defined:

$$\phi_{1D} = \begin{cases} V_{d'} - \mathcal{E}_p \cdot l_d & \text{for } x > l_d, \\ V_{d'} - \mathcal{E}_p \cdot x & \text{for } x \leq l_d. \end{cases} \tag{4.5}$$

Following that idea straight forward it is necessary to apply for Fig. 4.9 the below written boundary conditions

- ① **to** ② Coming from infinity and approach the structure ($x > l_d$), here having
$$\varphi_{2D}(x) = V_{gs} - V_{fb} - \phi_{1D}(x) = 0. \tag{4.6}$$

- ② **to** ③ Going from point $z = (T_{ch} + 2 \cdot t_{ox}\sim) + j \cdot ld$ to $z = (T_{ch} + 2 \cdot t_{ox}^{\sim}) + j0$ over the distance l_d in x direction of the geometry ($x \leq l_d$) in Fig. 4.9,
$$\varphi_{2D}(x) = V_{gs} - V_{fb} - \phi_{1D}(x). \tag{4.7}$$

- ③ **to** ④ Since this is the boundary condition through the oxide, the equation
$$\varphi_{2D}(y) = V_{gs} - V_{fb} - \frac{V_{gs} - V_{fb} - V_{ds} - V_{bi}}{t_{ox}^{\sim}} \cdot y - \phi_{1D}(x = 0). \tag{4.8}$$
is necessary. As drain-source voltage was defined V_{ds} and V_{bi} is the built in potential. The thickness of the transformed oxide is $t_{ox}^{\sim}$.

- ④ **to** ⑤ Along the drain junction is defined
$$\varphi_{2D}(y) = V_{ds} - V_{bi} - \phi_{1D}(x = 0). \tag{4.9}$$

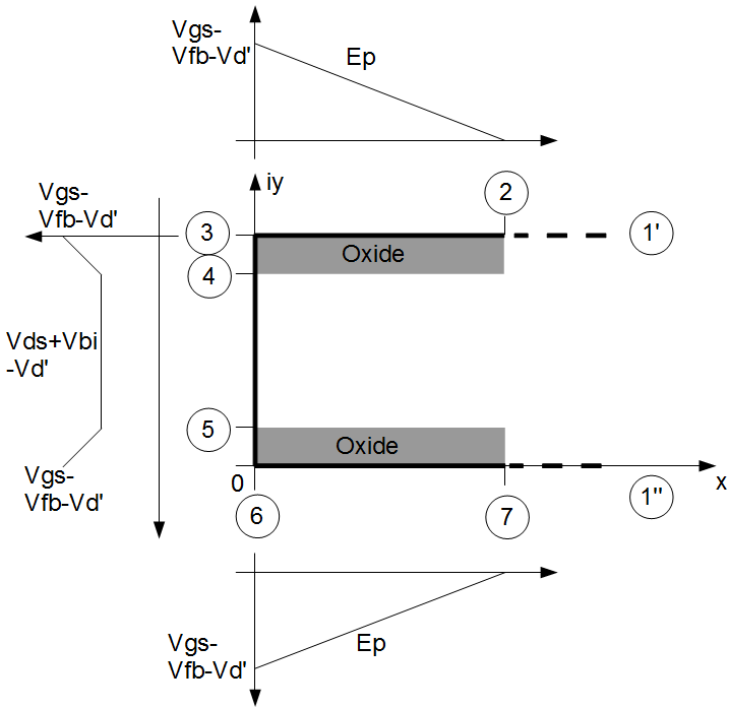


Figure 4.13: Estimated characteristics of boundary conditions in z-plane.

- ⑤ **to** ⑥ The second oxide need the equation

$$\varphi_{2D}(y) = V_{gs} - V_{fb} - \frac{V_{gs} - V_{fb} - V_{ds} - V_{bi}}{t_{ox}^{\sim}} \cdot y - \phi_{1D}(x = 0). \quad (4.10)$$

- ⑥ **to** ⑦ Going along the x-axis back to the point $z = 0 + jl_d$ with

$$\varphi_{2D}(x) = V_{gs} - V_{fb} - \phi_{1D}(x). \quad (4.11)$$

- ⑦ **to** ①" And finally following the boundary conditions again away from the 2-corner structure back into infinity, $(x > l_d)$, with

$$\varphi_{2D}(x) = V_{gs} - V_{fb} - \phi_{1D}(x) = 0. \quad (4.12)$$

In Fig. 4.13 the estimated characteristics resulting from equations (4.6) to (4.12) are drawn. Again it is necessary consider the quasi 4-corner structure

as shown in Fig. 4.7. That means that the potential Φ_{2D} calculated with the above boundary conditions needs to be multiplied by 2.

In here the length l_d is not given, but the saturation voltage V_{dsat} can be determined. To come to l_d the length l_d is varied until the calculated 2D potential Φ_{2D} matches a given saturation voltage V_{dsat}. As next V_{dsat} and $\mathcal{E}_p$ needs to be defined.

4.3 Solving 2D Poisson

With the definition of the boundary conditions the potential can be determined with Eqn. (2.35). To transform the boundary conditions from z-plane to w-plane Eqn. (2.43) is used.

- **①' to ②**

$$\varphi_{2D}(x) = V_{gs} - V_{fb} - \phi_{1D}(x) = 0 \tag{4.13}$$

$\Longrightarrow$

$$\Phi_{1'2}(u, v) = 0 \tag{4.14}$$

- **② to ③**

$$\varphi_{2D}(x) = V_{gs} - V_{fb} - \phi_{1D}(x) = \mathcal{E}_p \cdot (x - ld) \tag{4.15}$$

$\Longrightarrow$

$$\Phi_{23}(u, v) = \frac{1}{\pi} \int_{x=ld}^{x=0} \frac{v}{v^2 + (u - \overline{u})^2} \cdot \mathcal{E}_p \cdot (\operatorname{arccosh}(\overline{u}) \frac{\triangle\, y}{\pi} - ld) d\overline{u} \tag{4.16}$$

- **③ to ④**

$$\begin{aligned}\varphi_{2D}(x=0,y) &= V_{gs} - V_{fb} - \frac{V_{gs}-V_{fb}-V_{ds}-V_{bi}}{t_{ox}^{\sim}} \cdot y - \phi_{1D}(x=0) \\ &= V_{gs} - V_{fb} - \frac{V_{gs}-V_{fb}-V_{ds}-V_{bi}}{t_{ox}^{\sim}} \cdot y - \mathcal{E}_p \cdot ld\end{aligned} \tag{4.17}$$

$\Longrightarrow$

$$\Phi_{34}(u,v) = \frac{1}{\pi}\int_{y=0}^{y=t_{ox}^{\sim}} \frac{v}{v^2+(u-\overline{u})^2} \cdot \left(\frac{V_{gs}-V_{fb}-V_{ds}-V_{bi}}{t_{ox}^{\sim}} \cdot \operatorname{arccosh}(\overline{u})\frac{\triangle\, y}{\pi} - \mathcal{E}_p \cdot ld\right) d\overline{u}. \tag{4.18}$$

- **④ to ⑤**

$$\begin{aligned}\varphi_{2D}(x=0,y) &= V_{ds} + V_{bi} - \phi_{1D}(x=0) \\ &= V_{ds} + V_{bi} - \mathcal{E}_p \cdot ld\end{aligned} \tag{4.19}$$

$\Longrightarrow$

$$\Phi_{45}(u,v) = \frac{1}{\pi}\int_{y=t_{ox}^{\sim}}^{y=T_{ch}+t_{ox}^{\sim}} \frac{v}{v^2+(u-\overline{u})^2} \cdot (V_{ds}+V_{bi}-\mathcal{E}_p \cdot ld)\, d\overline{u} \tag{4.20}$$

- **⑤ to ⑥** This solution is similar to $\Phi_{45}(u,v)$ in Eqn. (4.20), whereby $\Phi_{56}(u,v) = \Phi_{45}(-u,v)$.

- **⑥ to ⑦** This solution is similar to $\Phi_{23}(u,v)$ in Eqn. (4.16), whereby $\Phi_{67}(u,v) = \Phi_{23}(-u,v)$.

- **⑦ to ①"** This solution is similar to $\Phi_{1'2}(u,v)$ in Eqn. (4.14), whereby $\Phi_{71''}(u,v) = \Phi_{1'2}(-u,v)$.

As next all potential solutions need to be added up and due to the mirroring of the structure to create a quasi 4-corner structure the result is

multiplied by 2

$$\begin{aligned}\Phi(u,v) = \big(&\Phi_{1'2}(u,v) + \Phi_{23}(u,v) + \Phi_{34}(u,v) + \Phi_{45}(u,v) \\ &+ \Phi_{56}(u,v) + \Phi_{67}(u,v) + \Phi_{71''}(u,v)\big) \cdot 2\end{aligned} \tag{4.21}$$

This integration system (4.21) can be solved in analytical closed form solution, which is done in the appendix A.

4.4 Definition of the Saturation Point

As described before it is possible to calculate the electric potential at the pinch-off point in an analytical closed-form. To come from the electric potential to the actual channel length shorting it necessary to know the electric field $\mathcal{E}_p$ at that point and vary the length until this value is reached.

For the calculation of the electric field at saturation point $\mathcal{E}_p$ and the voltage at saturation point V_{dsat}, have a look at Fig. 4.4. It shows that the channel is right underneath the oxide and vanishes when saturation point is reached. With the assumption that up to saturation point each gate controls half of the channel and the influence of the gate is one-dimensional. So at saturation point is

$$V_{gs} - V_{fb} = V_{ox} + \phi_i + V_{dsat}, \tag{4.22}$$

whereby V_{ox} is the voltage across the oxide and V_{fb} is the flatband voltage. The inversion potential at saturation point is given by ϕ_i. Since in saturation region the inversion charge is approximately 0, the voltage drop across the oxide is assumed to be $V_{ox} \approx 0$. So the expression

$$V_{dsat} = V_{gs} - V_{fb} - \phi_i. \tag{4.23}$$

for V_{dsat} can be used. To calculate $\mathcal{E}_p$ the current can be described at the

saturation point as [31]

$$I_{dsat} = q_i \cdot T_{ch} \cdot W_{ch} \cdot \mu_0 \frac{\mathcal{E}_p}{1 + \frac{\mathcal{E}_p}{\mathcal{E}_c}}. \tag{4.24}$$

q_i is the inversion charge per unit volume while assuming that the charge in pinch-off region is uniformly distributed along the film thickness, μ_0 the mobility of the electrons and $\mathcal{E}_c$ the critical electric field. This equation only calculates the current in the saturation point. In this point $V_{ox} = 0$, so mobility μ_0 is independent from the gate bias is used. The inversion charge density is

$$q_i = q \cdot \frac{n_i^2}{N_B} \cdot exp\left(\frac{\phi_i}{V_t}\right). \tag{4.25}$$

The elementary charge is given by q and V_t is the thermal voltage.

Furthermore defining the current in the saturation point with [31]

$$I_{dsat} = \frac{\mu_{eff} \cdot C_{ox} \cdot 2 \cdot T_{ch}}{L\left(1 + \frac{V_{dsat}}{L \cdot \mathcal{E}_c}\right)} \cdot \left(V_{gs} - V_{th} - \frac{V_{dsat}}{2}\right) \cdot V_{dsat}. \tag{4.26}$$

C_{ox} represents the gate oxide capacitance per unit area, L is the gate length and the effective mobility μ_{eff} is given by [31]

$$\mu_{eff} = \frac{\mu_0}{1 + \theta \cdot (V_{gs} - V_{th})} \tag{4.27}$$

With Eqn. (4.24) = Eqn. (4.26),

$$\mathcal{E}_p = \frac{1}{\frac{1}{\frac{\mu_{eff} \cdot C_{ox}}{q_i \cdot \frac{T_{ch}}{2} \cdot \mu_0 \cdot L\left(1 + \frac{V_{dsat}}{L \cdot \mathcal{E}_c}\right)} \cdot \left(V_{gs} - V_{th} - \frac{V_{dsat}}{2}\right) \cdot V_{dsat}} - \frac{1}{\mathcal{E}_c}} \tag{4.28}$$

the electric field $\mathcal{E}_p$ depending on V_{ds} and V_{gs} can be calculated. This is necessary because the saturation voltage is calculated independently of V_{ds}. With increasing drain-source voltage the saturation point moves source-wards. Keeping V_{dsat} at saturation point still constant the electric field $\mathcal{E}_p$ has to increase, which is shown in 4.14. For various V_{gs} and V_{ds} the electric field at

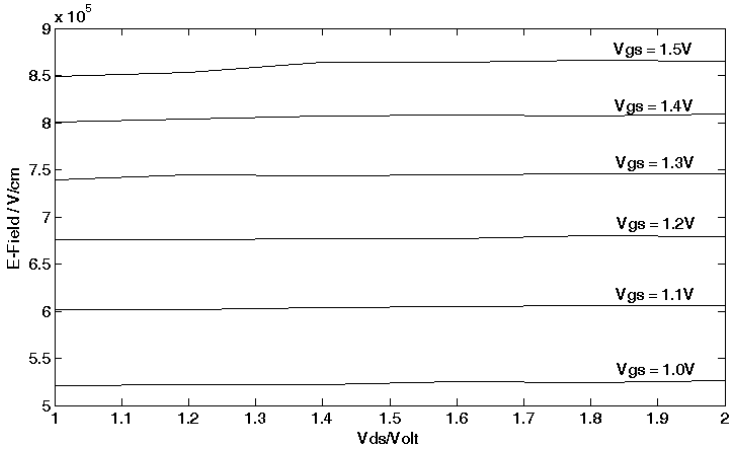


Figure 4.14: Electric field at the pinch off point extracted from TCAD Sentaurus [10] simulations for various V_{gs} and V_{ds}. The E-field slightly increases with V_{ds}.

pinch-off point extracted from TCAD Sentaurus [10]. The electric field slightly increases with V_{ds}, which actually has an influence on l_d. To include this effect in the model, it is necessary to calculate the electric field at described above. After the definition of V_{dsat} and $\mathcal{E}_p$ it is possible to calculate l_d. For this the geometry is varied with the boundary conditions from section 4.2.1, with the here calculated $\mathcal{E}_p$ included in the boundary conditions. When the potential Φ_{2D} matches the defined $V_{dsat} + \phi_i$ the length l_d of the geometry is the length of the high field saturation region.

4.4.1 Threshold Voltage Model

In order to make the model as good as possible as threshold voltage V_{th} model the approach published by [102] and [103]. It uses conformal mapping technique as well from that an expression for the potential barrier in undoped channels of DG MOSFETs including the DIBL effect has been derived. This model was also used to calculate the threshold voltage in a FinFET by [104].

In a DoubleGate MOSFET the most leaky path in cross-section below threshold is on a center line in the middle of the device, see Fig. 4.15. The

potential barrier minimum is located on that part.

For multigate devices often a certain electron concentration, i.e. an inversion potential ϕ in the most leaking path, resulting from a specific gate biased is defined. The corresponding gate bias is stated as threshold voltage. An increasing gate voltage, before strong inversion at the Silicon-SiliconOxide interface takes place, results in an increasing electron concentration on the most leaking path.

The analytic expression to map a 4-corner structure of a DoubleGate cross section to w-plane is

$$\begin{aligned}\phi(u,v) = \frac{1}{\pi}\Bigg[&(V_{gs}-V_{fb})\left[\pi - \arctan\left(\frac{1-ku}{kv}\right) - \arctan\left(\frac{1+ku}{kv}\right)\right] \\ &+ (V_{gs}-V_{fb})\left[\arctan\left(\frac{1-u}{v}\right) + \arctan\left(\frac{1+u}{v}\right)\right] \\ &+ V_{bi}\left[\arctan\left(\frac{1-ku}{kv}\right) - \arctan\left(\frac{1-u}{v}\right)\right] \\ &+ (V_{bi}+V_{ds})\left[\arctan\left(\frac{1+ku}{kv}\right) - \arctan\left(\frac{1+u}{v}\right)\right]\Bigg].\end{aligned} \tag{4.29}$$

The 4-corner structure is drawn in Fig. 4.15. The middle of the device in y-direction is 0. Drawing a center line from source to drain and map this upon a circle of radius $\frac{1}{\sqrt{k}}$ in upper w-plane as shown in Fig. 4.16. The parameters to calculate the position $w = u + iv$ are

$$u = \frac{1}{\sqrt{k}}\cos\theta_{angle} \tag{4.30}$$

and

$$v = \frac{1}{\sqrt{k}}\sin\theta_{angle}. \tag{4.31}$$

Whereby θ_{angle} is the angle along a half circle of radius $\frac{1}{\sqrt{k}}$ in w-plane.

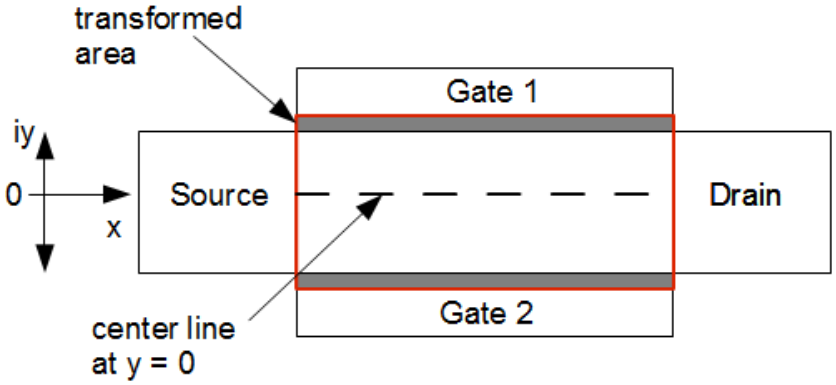


Figure 4.15: DG MOSFET with marked 4-corner area which will be mapped with Schwarz-Christoffel into w-plane. Here the minimum of the potential of center line is searched.

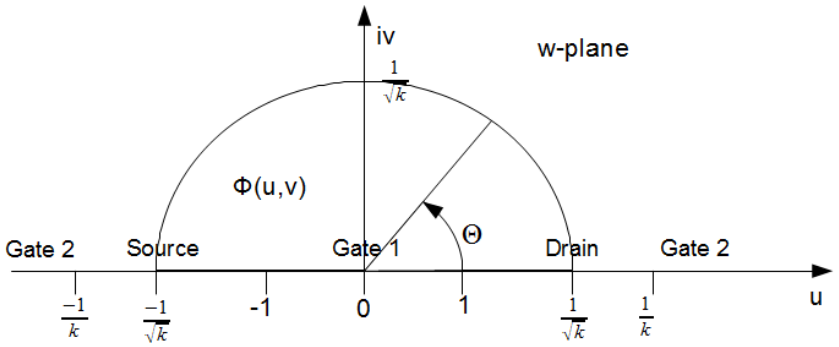


Figure 4.16: A 4-corner structure mapped with Schwarz-Christoffel [75] on a circle with radius $\frac{1}{\sqrt{k}}$ into upper half of w-plane. All boundaries lay flat on the real axis.

At the position of the potential minimum the conditions

$$\left.\frac{\partial \phi_{dg}(x,y)}{\partial x}\right|_{x_m} = 0 \qquad \text{and} \qquad \left.\frac{\partial \phi_{dg}(x,y)}{\partial y}\right|_{y=0} = 0 \tag{4.32}$$

have to be fulfilled. x_m is a position in x-direction on the center line. Conformal mapping scales the electric field by the derivatives of the mapping function [75]:

$$\left|\frac{\partial \phi_{dg}(x,y)}{\partial z}\right| = \left|\frac{\partial \phi_{dg}(u,v)}{\partial w}\right| \cdot \left|\frac{\partial w}{\partial z}\right| \tag{4.33}$$

To obtain the position of the potential barrier along the center line of the channel Eqn. (4.30) and (4.31) are inserted in (4.29). Solving everything for the root of the derivatives with respect to θ_{angle}

$$\left.\frac{\partial \phi_{dg}(\theta_{angle})}{\partial \theta}\right|_{\theta_m} = 0 \tag{4.34}$$

Written in a closed form solution,

$$\theta_m = \pi - \arccos\left[\frac{\frac{1}{2}(k+1)V_{ds}}{\sqrt{k}\,(2V_{gs} - 2V_{fb} - 2V_{bi} - V_{ds})}\right] \tag{4.35}$$

Finally mapping it back into z-plane to obtain the coordinates of the potential minimum

$$x_m = \frac{\frac{L}{2}\mathrm{F}\left(\frac{2\sqrt{k}}{1+k}, \cos(\theta)\right)}{\mathrm{K}\left(\frac{2\sqrt{k}}{1+k}\right)} \tag{4.36}$$

where F is the standard (Lagrange) elliptic integral of the first kind and K is the complete elliptic integral of the first kind [75], [93]. These integrals can be approximated by generalized power series or iteration methods and have been tabulated.

The actual potential of the minimum can be calculated by putting Eqn. (4.36) into (4.29). To calculate the threshold voltage V_{th} two different gate voltages below threshold are placed in the equation system. The mobile charge in cross-section is neglected while solving 2D Poisson's equation. With an

extrapolation using a linear function the point when the potential minimum reaches a specific electron concentration, means ϕ_i, is calculated in a closed form solution. For details about this procedure refer to [104].

For the modeling of the channel length shortening in a DG MOSFET the threshold voltage model was set to a fixed electron concentration of $5 \cdot 10^{18}$cm, which corresponds to $\phi_i = 0.793$V and never changed. The model fitted and described the DIBL effect perfectly well for the channel length shortening presented in this thesis.

4.5 Model Results

It is interesting to see, how the model predicts the pinch-off point boundary. In Fig. 4.17 is the structure shown in which Poisson's equation is solved. The red line shows the boundary where we extracted the results for the Laplacian $\varphi_{2D}(x, y)$ from the model. We varied l_d and received various results, shown in Fig. 4.18. To come to the 2D potential at pinch-off point, it is necessary to add the inversion charge, with $\phi_{1D}|_{x=l_d} = Vgs - Vfb$. The transformed oxide $t_{ox}^{\sim}$ has a thickness of 3.37nm. The channel width is 10nm and applied voltages are $V_{ds} = 1.4$V and $V_{ds} = 1$V. We varied l_d from the pinch off point at 7.6nm in 10 steps to 8.6nm.

In the channel a parabolically shaped voltage is predicted. Since we transformed the oxide, at the $Si - SiO_2$ interface we have a continuous electric field. Through the oxide the voltage increases again and reaches 0. According to Eqn. (4.7), we assume at the pinch-off position an applied oxide voltage of 0V for the Laplace solution.

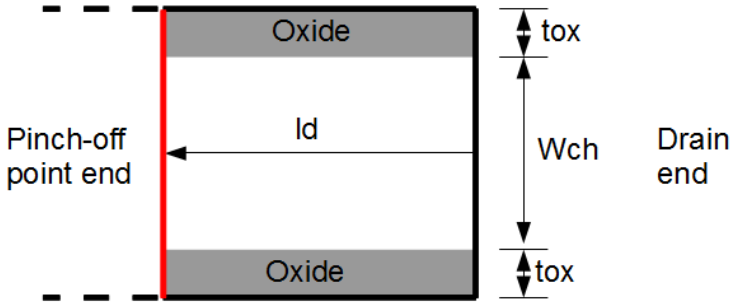


Figure 4.17: Structure in where 2D Poisson is solved. In red: The boundary where the model results were extracted.

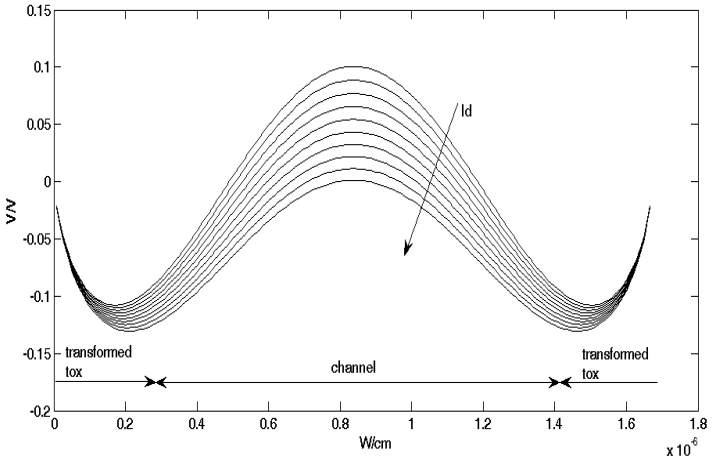


Figure 4.18: Results of the model for the 2D Laplacian $\varphi(x, y)$ along the pinch-off point boundary. Transformed oxide $t_{ox}^{\sim}$ thickness ix 3.37nm, channel width is 10nm and applied voltages are $V_{ds} = 1.4$V and $V_{ds} = 1$V. We varied l_d from the pinch off point at 7.6nm in 10 steps to 8.6nm.

4.6 Closed Form Solution

In the appendix the closed-form solution for the integrals of the 2D Poisson's equation are introduced. With this it is possible to calculate the voltage along l_d as shown in Fig. 4.19 in a closed-form condition. In Fig. 4.20 the characteristics of V_{dsat} with increasing l_d are calculated by the model for various V_{ds}. However, we need to find our defined V_{dsat} along those characteristics, which is done so far by approximation procedure. This takes to long and is not suitable for a model.

In Eqn. (4.22) on page 69 saturation voltage is defined, whereby $V_{ox} \approx 0$. The voltage at the saturation point calculated by 2D Poisson's equation is

$$\Phi_{2D}|_{pinchoffpoint} = V_{dsat} - \phi_i \tag{4.37}$$

On page 64 we describe the splitting of the 2D Poisson's equation. The splitting has to be done for every point within the region wherein Poisson's equation is solved. At position $x = l_d$ the 1D poisson solution is

$$\phi_{1D}|_{x=l_d} = V_{gs} - V_{fb} \tag{4.38}$$

The 2D Laplace solution in Eqn. (4.21) is by

$$\varphi_{2D} = \Phi_{2D} - \phi_{1D} = 0 \tag{4.39}$$

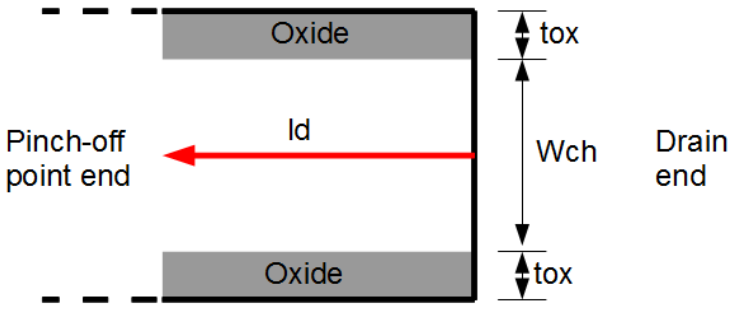


Figure 4.19: Path where the voltage can be calculated in a closed-form condition by solving 2D Poison.

Even with this simplification it is not possible to solve Eqn. (4.21) in a closed-form, because of all the tangent terms in it.

Of course the characteristics extracted along l_d in Fig. 4.20 look like they can be described as a *exp*-function with a linear boundary. Nevertheless a *exp*-function does not really fit and the complexity of the function is limited due to the goal of a closed-form solution. Furthermore no begin or end point of the characteristics can be determined. A not well fitting function will result in a different slope at each point and might gives very different results with different devices structures.

A polynomial function of 4 grade was used instead

$$N = x^4 + ax^3 + bx^2 + cx + d. \tag{4.40}$$

For the fitting it was assumed that a channel length shortening over 20nm is not possible. 5 points on the curve were extracted with Eqn. (4.21) and with linear algebra the components a, b, c and d were solved.

Fig. 4.21 shows the comparison between the fitted function (symbols) and the actual results (lines). Both curves are in very good agreement. Assuming only one reasonable result for the channel length shortening coming from the four results given by a quartic expression, the fitting polynomial function Eqn. (4.40) can be solved in a closed form solution.

To calculate the zero point of a polynomial function of 4 grade, we substitute

$$x = z - \frac{a}{4} \tag{4.41}$$

we have

$$0 = z^4 + \left(b - \frac{3}{8}\cdot a^2\right)\cdot z^2 + \left(-\frac{3}{256}\cdot a^4 + \frac{1}{16}\cdot a^2 b - \frac{1}{4}\cdot ac + d\right). \tag{4.42}$$

Introducing the symbols p, q, r the equation is easier to read

$$0 = z^4 + pz^2 + qz + r. \tag{4.43}$$

With elimination of the term of 3rd grade, we can use the idea of Ferrari [105],

$$0 = \left(z^2 + P\right)^2 - \left(Qz + R\right)^2. \tag{4.44}$$

The coefficients can be calculated by

$$\begin{aligned} I. \quad & p = 2P - Q^2 \\ II. \quad & q = -2QR \\ III. \quad & r = P^2 - R^2 \end{aligned} \tag{4.45}$$

and the corresponding equations to find the positions where $N = 0$ are,

$$\begin{aligned} z_{1,2} &= +\frac{Q}{2} \pm \sqrt{\left(\frac{Q}{2}\right)^2 - P + R} \\ z_{3,4} &= -\frac{Q}{2} \pm \sqrt{\left(\frac{Q}{2}\right)^2 - P - R}. \end{aligned} \tag{4.46}$$

A value for the channel length shortening can neither be an imaginary value nor longer than the channel is. Therefore only

$$z_2 = +\frac{Q}{2} - \sqrt{\left(\frac{Q}{2}\right)^2 - P + R} \tag{4.47}$$

gives a reasonable value. The final equation is very long, however it is in closed form.

Fig. 4.22 shows the channel length shortening of the closed form solution (lines) and the exact calculated value by the model (symbols) for a DG MOSFET with $L = 50$nm and a channel thickness of $T_{ch} = 10$nm. Even with variation of V_{gs} and V_{ds} no difference is shown. In the following section the results of the closed-form solution are compared to TCAD Sentaurus [10]

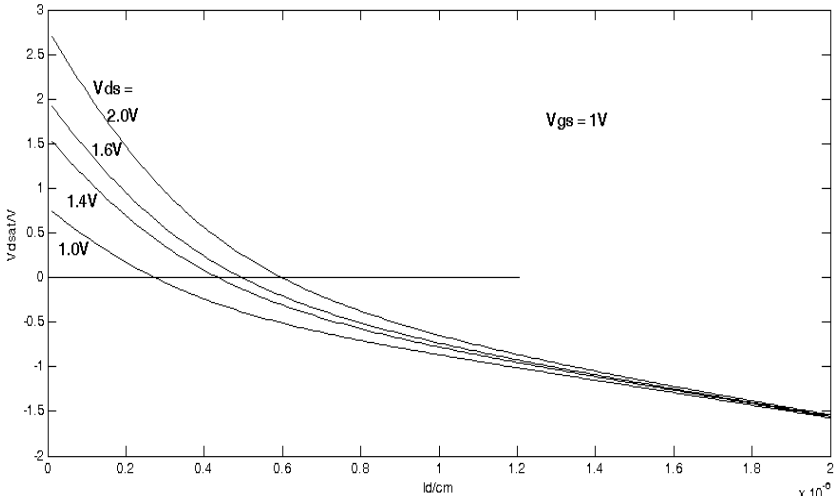


Figure 4.20: Characteristics of V_{dsat} in the pinch-off point with increasing l_d as calculated by the model. The pinch-off point is reached when $V_{dsat} = 0$.

simulation results.

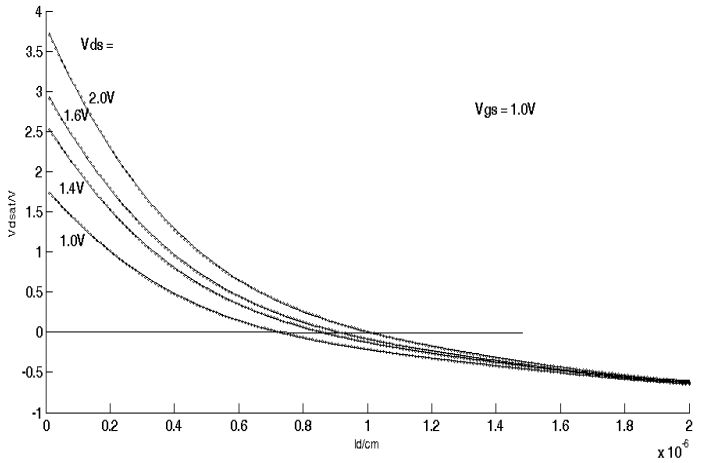


Figure 4.21: Characteristics of V_{dsat} in the pinch-off point with increasing l_d as calculated by the model in lines and with a polynomial function of 4th grade in symbols. With this it is possible to calculate the pinch-off point in closed form solution.

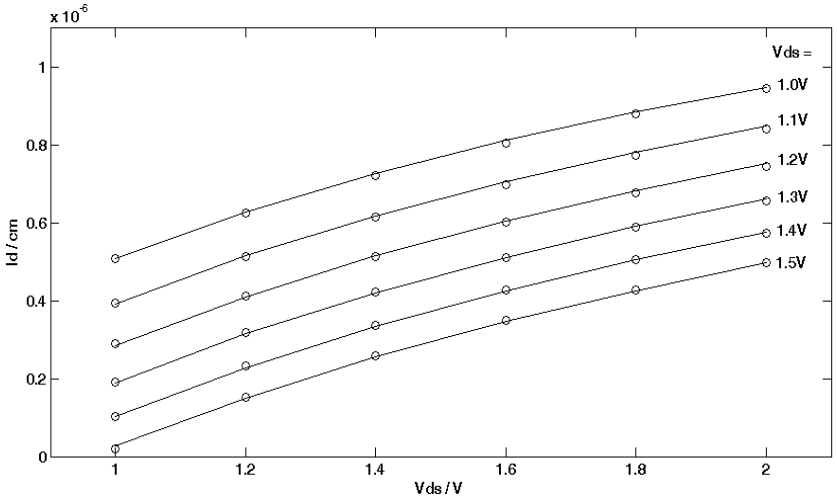


Figure 4.22: Comparison between the channel length shortening of the closed-form solution (lines) and the exact calculated value by the model (symbols) for a DG MOSFET with $L = 50$nm and a channel thickness of $T_{ch} = 10$nm for various V_{gs} and V_{ds}. Practically no difference is shown.

4.7 Results

In Fig. 4.23, 4.24 and 4.25 are shown l_d as function of V_{ds} for various V_{gs} for different devices. The device in Fig. 4.23 has a channel length of $L = 50$nm and a channel thickness of $T_{ch} = 10$nm, Fig. 4.24 has a channel length of $L = 20$nm. As third device for Fig. 4.25 a channel channel length of $L = 50$nm and a channel thickness of $T_{ch} = 20$nm was simulated. Comparing the model to TCAD Sentaurus software and l_d has been measured from the drain end to the point when the electric potential maximum moves from the underneath the gate oxide into the middle of the channel. The model is drawn in black lines and the TCAD Sentaurus in symbols.

A critical electric field $\mathcal{E}_c = 10^6 \frac{V}{cm}$ has been used for all plots. With $\mathcal{E}_c$ the curves can be shifted in y-direction of the graphs in Fig. 4.23 to Fig. 4.25. It has no influence on the slope of the curves. So it was set to a reasonable value. The inversion potential is with

$$\phi_i = 2 \cdot V_t \ln\left(\frac{N_B}{n_i}\right) + \triangle\, \phi_{fit} \tag{4.48}$$

a good starting point for the fitting. It still needs some adjustment with $\phi_{fit} = -0.141$V for $L = 50$nm; $\phi_{fit} = -0.125$V for $L = 20$nm and $\phi_{fit} = -0.11$V for $L = 50$nm and $T_{ch} = 20$nm. This value has the same influence as $\mathcal{E}_c$, a shift of the curves in y-direction. Again, it has no influence on the shape of the curve.

With the mobility model in Eqn. (4.27) the distance or gap between all curves can be influenced. The mobility μ_0 itself has no influence, since it cancels in the calculation of $\mathcal{E}_p$ due to equating Eqn. (4.24) = Eqn. (4.26). Nevertheless, θ for the influence of V_{gs} is set to 0.01 for $L = 50$nm and 0.5 for $L = 20$nm. The third device in Fig. 4.25 with $L = 50$nm and $T_{ch} = 20$nm needed $\theta = 0.5$ as well for a reasonable fit.

The model is in good agreement with the simulation results. Also with

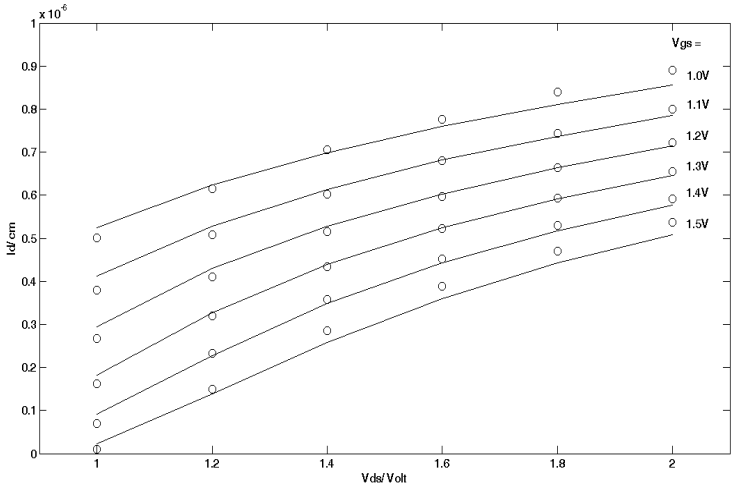


Figure 4.23: Results for l_d vs. V_{ds} for various V_{gs} calculated with a geometry with $L = 50$nm and $T_{ch} = 10$nm. The lines represent model and the symbols the results from TCAD Sentaurus.

$V_{gs} = 1$V to 1.5V with a $V_{th} \approx 0.45$V the results cover up to almost 15nm channel length modulation. All three plots show quite similar values for channel length shortening. Indeed channel length shortening depends mainly on drain site of the device, that is why Fig. 4.23 and 4.24 show very similar results. For plot 4.25 the channel was twice as thick, which results in a longer channel length shortening. Only with very short devices the source end starts to affect the channel length shortening and the distance between drain junction and saturation point becomes shorter.

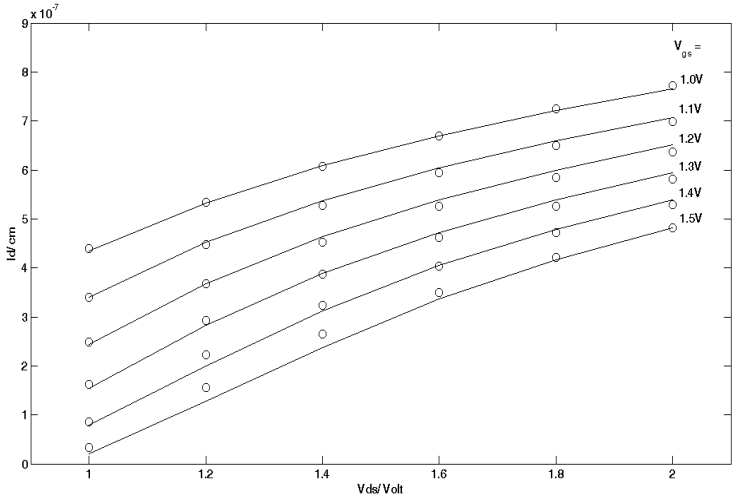


Figure 4.24: Results for l_d vs. V_{ds} for various V_{gs} calculated with a geometry with $L = 20$nm and $T_{ch} = 10$nm. The lines represent model and the symbols the results from TCAD Sentaurus.

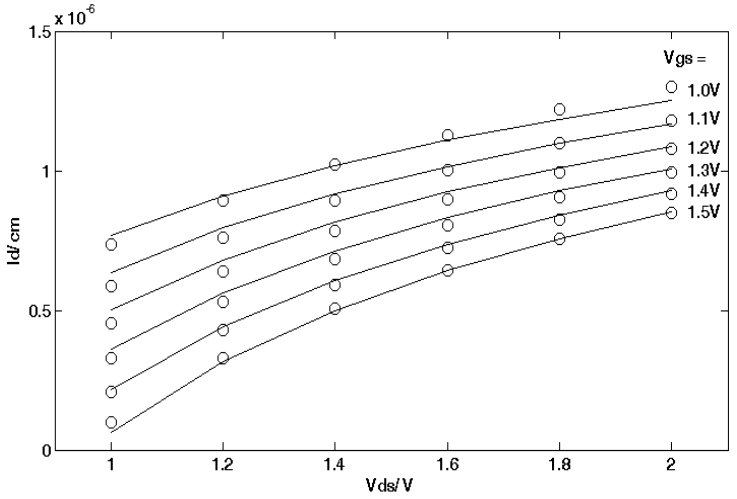


Figure 4.25: Results for l_d vs. V_{ds} for various V_{gs} calculated with a geometry with $L = 50$nm and $T_{ch} = 20$nm. The lines represent model and the symbols the results from TCAD Sentaurus.

4.8 Quantum Mechanics

In a device with a length of 20nm and a channel thickness of 10nm quantum mechanics effects take place. it is expected that for channel thicknesses below 10nm a model has to take quantum mechanics into account. In this chapter is shown if this approach is extendable so that it covers quantum mechanics.

4.8.1 Device Physics including Quantum Mechanics

Fig. 4.26 shows the electric potential distribution of a device with $V_{ds} = 1\text{V}$ and $V_{gs} = 1\text{V}$ and a channel length of 20nm and a channel width of 10nm. In the eletric potential distribution is between quantum and no quantum effect no difference, see Fig. 4.4. Nevertheless in the E-current distribution for the same device, shown in Fig. 4.27 the channels are not longer located directly at the Silicon-SiliconOxide interface when comparing the figure to Fig. 4.5. Instead a so called quantum well is formed between gate oxide and channel.

However going along the channel, the behavior of the current changes. At source end two strings of current were formed. At drain end those two strings are widening and come together. The current is equally spread over almost the whole channel. The path of the electric potential maximum is drawn in Fig. 4.28 for $V_{ds} = 1\text{V}$ and $V_{gs} = 1\text{V}$. Drain and source region are cut out as well as the gate material and oxide are in this figure omitted. The electric potential maximum is at source end still at the Silicon-SiliconOxide interface. When hitting saturation point the maximum moves into the middle of the channel. So it is with quantum mechanic effects possible to define a saturation points.

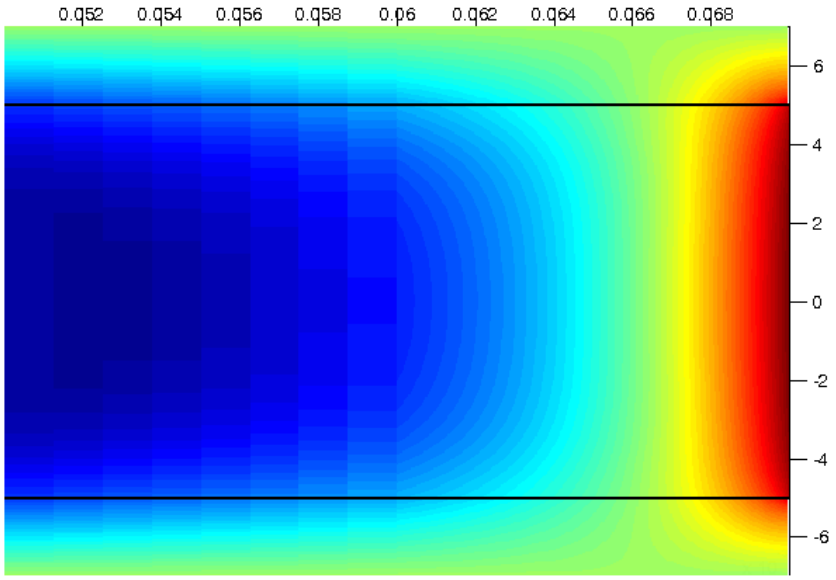


Figure 4.26: Electric potential distribution within channel region and gate oxide of DG MOSFET with an applied $V_{ds} = 1$V and $V_{gs} = 1$V. Drain and source region are cut out as well as the gate material. Quantum mechanics effects have almost no influence on the electric potential distribution.

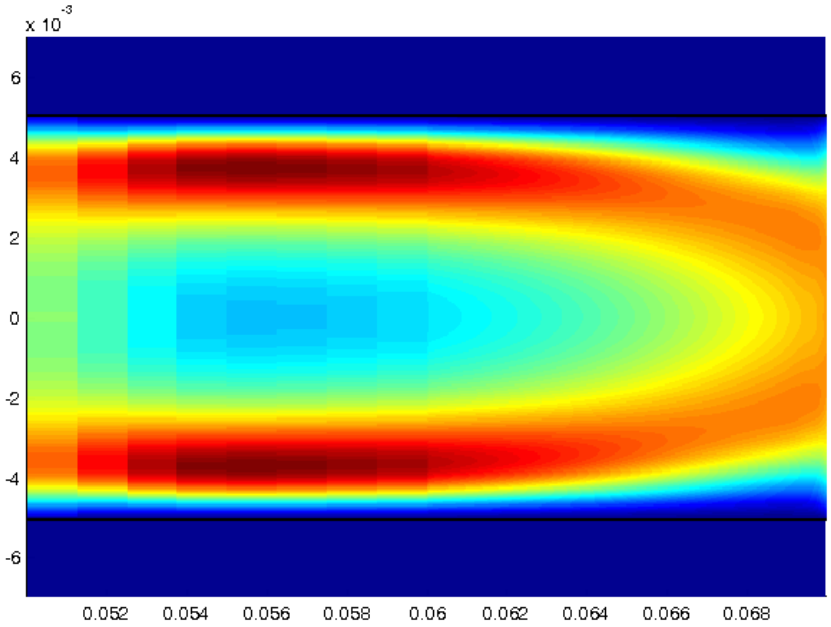


Figure 4.27: E-current density distribution within channel region and gate oxide of DG MOSFET with an applied $V_{ds} = 1$V and $V_{gs} = 1$V. Drain and source region are cut out as well as the gate material. Quantum mechanics effects take place.

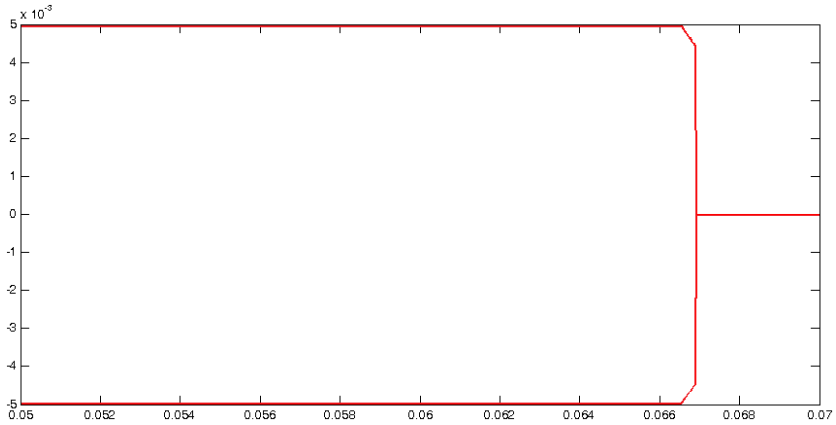


Figure 4.28: Path of the electric potential maximum along the channel drawn in red with an applied $V_{ds} = 1$V and $V_{gs} = 1$V. Drain and source region are cut out as well as the gate material and oxide are omitted. The maximum is even with included quantum mechanic effects at the beginning of the channel still at the silicon-siliconoxide interface.

4.8.2 Results including Quantum Mechanics

For a channel length of $Lch = 20$nm and a channel thickness $T_{ch} = 10$nm some simulations with TCAD Sentaurus [10] including a quantum mechanics model were done. The results are plotted in Fig. 4.29, the channel length modulation l_d versus the drain source voltage V_{ds} for various gate source voltage V_{gs}. The lines represent model and the symbols the results from TCAD Sentaurus.

As model was used the model presented for the symmetrical DoubleGate MOSFET in chapter 4 without further adjustments. The fitting parameters are $\phi_{fit} = -0.1145$V, $\mathcal{E}_c = 4 \cdot 10^5 \frac{\text{V}}{\text{cm}}$ and $\theta = 0.99$. The results are in very good agreement for a higher V_{ds}. It can not be denied that for lower V_{ds}, close to the saturation voltage the model gives a rather weak description of the pinch-off point position. It can be assumed that the definition of the saturation voltage, given in section 4.4 is not accurate enough for a quantum mechanics case. It would be a good approach for future work.

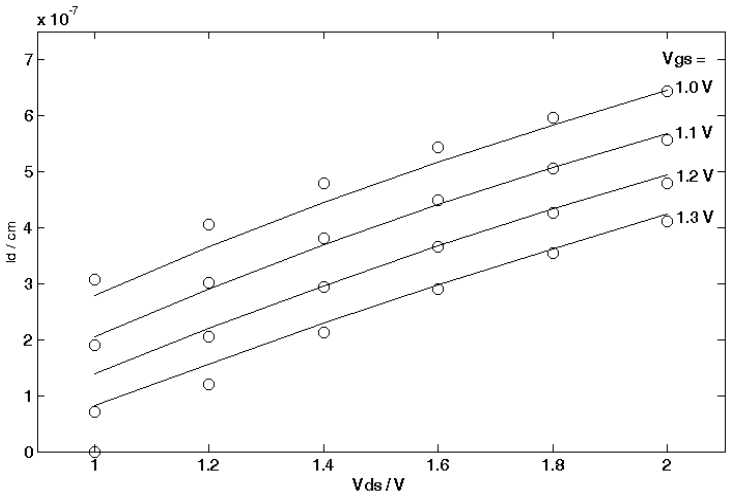


Figure 4.29: Results for l_d vs. V_{ds} for various V_{gs} calculated with a geometry with $L = 20$nm and $T_{ch} = 10$nm including quantum mechanic effects. The lines represent model and the symbols the results from TCAD Sentaurus.

Chapter 5

Asymmetrically Biased Double Gate MOSFET

Additionally to symmetrically biased DG FET the idea came up to independently bias both gates. In a Double Gate structure is it easily doable. The advantage would be for instance to gain more control about the threshold voltage. Due to the fluctuation in factory this parameter can vary. In theory it would also be possible to reduce the drain induced barrier lowering effect or temperature variation.

In this chapter is shown that the channel length modulation of both gates in strong inversion is not independent of each other. In theory it would be possible to control for instance a driver output very accurate.

As basic we use the same simplified structure as used for the symmetrically biased DG as shown in Fig. 5.1. Also the model of the channel length modulation for symmetrically biased DG FETs referees as reference.

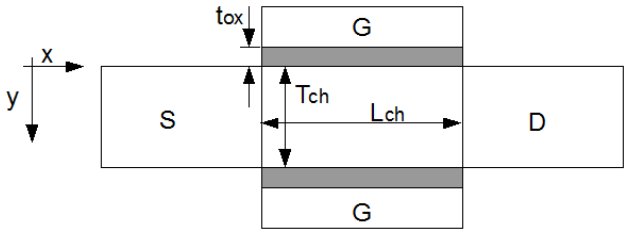


Figure 5.1: Simplified structure of a DG FET as used in this approach.The two gates can be biased independently of each other.

5.1 Device Physics

In chapter 4 was explained that an increasing source-drain voltage begins to effect the electrostatic behavior of symmetrically biased DG in accumulation. Truly this must count for an independently biased DG FET, too.

Having a look on the E-current density distribution of a DG MOSFET in Fig 5.2 with applied $V_{gs-top} = 1\text{V}$, $V_{gs-bottom} = 0.7\text{V}$ and $V_{ds} = 1.6\text{V}$ we see again two channels at the Silicon-SiliconOxide interface. The dimensions of the DG MOSFET are channel thickness $T_{ch} = 10\text{nm}$ and length $L_{ch} = 50\text{nm}$. Going along the channel both channels vanish when reaching saturation. However the lower biased bottom gate hits saturation point earlier. Compared to previous results this behavior is expected. With the E-potential distribution in Fig. 5.3 for the same device we see that the potential contour is parabolically shaped at the beginning of the channel. Hitting the first saturation point at the bottom of the DG MOSFET, the parable of the contour of the plot looks deformed and with reaching the second saturation point of the higher biased top gate, the contour looks even *s*-shaped.

The next question would be, if and how are the two saturation points related. For this a constant top gate voltage of 1V was applied and the voltage of the bottom gate was varied from $0.7 \cdots 1.4\text{V}$. The channel length shortening for both gates was extracted.

With no influence between both gates the channel length shortening for the top gate would be constant. Additionally the gap between the curves in

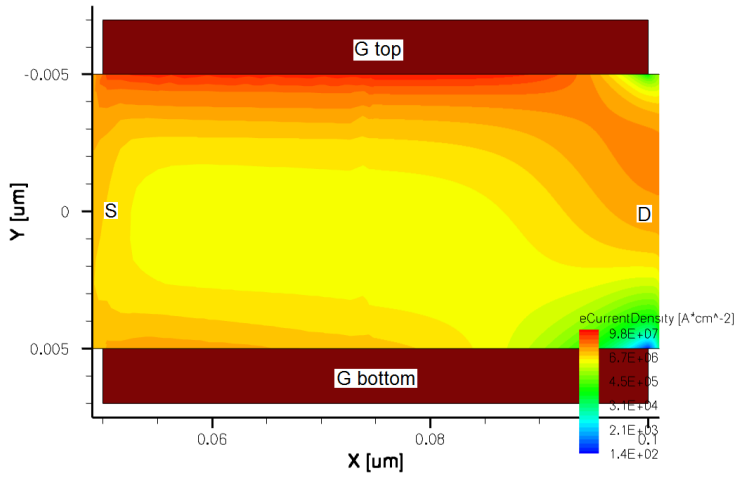


Figure 5.2: E-current density distribution within channel region and gate oxide of DG MOSFET with an applied $V_{gs-top} = 1$V, $V_{gs-bottom} = 0.7$V and $V_{ds} = 1.6$V. Drain and source region are omitted.

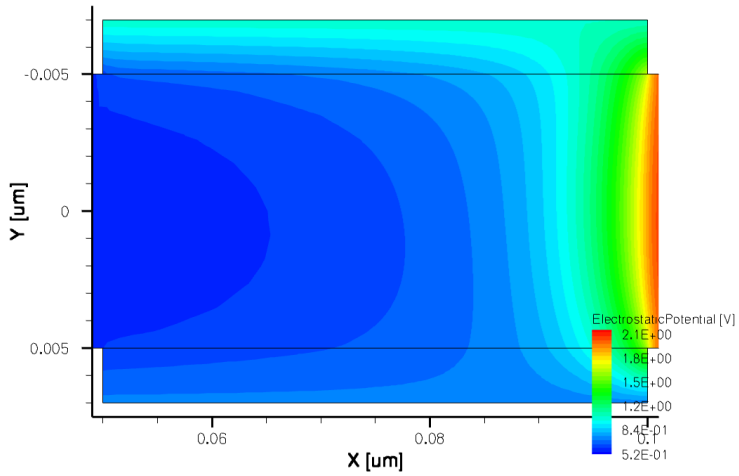


Figure 5.3: Electric potential distribution within channel region and gate oxide of DG MOSFET with an applied $V_{gs-top} = 1$V, $V_{gs-bottom} = 0.7$V and $V_{ds} = 1.6$V. Drain and source region are omitted as well as the gate material.

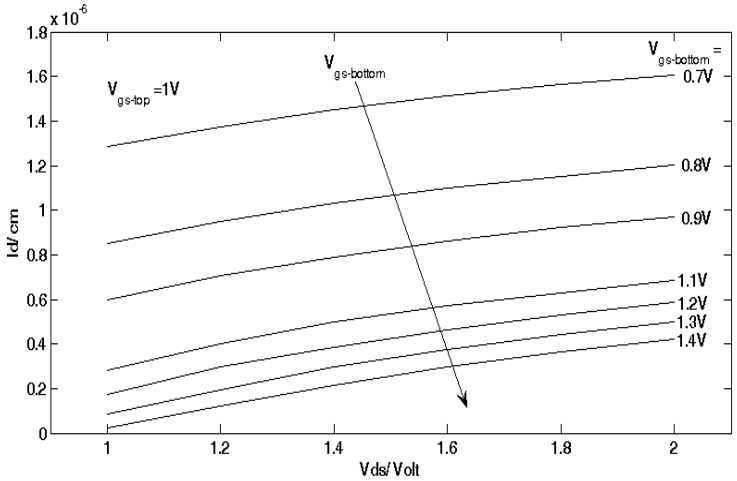


Figure 5.4: Channel length shortening extracted from TCAD Sentaurus simulation for the bottom gate, where $V_{gs-bottom} = 0.7 \cdots 1.4$V and constant $V_{gs-top} = 1$V. With increasing $V_{gs-bottom}$ l_d decreases.

Fig. 5.4 for each gate voltage step would be relatively even. Since the channel length shortening of the top gate varies with each voltage variation of the bottom gate (refer to Fig. 5.5) the bottom gate affects the top gate. On the other hand the curve gap in Fig. 5.4 of the channel length modulation of the bottom gate is very uneven. That means the top gate influences the bottom gate somehow too.

The idea is that the electric field issued by the drain region vectors partly into the direction of the top gate and the bottom gate, exaggerated version drawn in Fig. 5.6 and 5.7. Both figures show the drain end, with the gate oxide in gray. The inversion charge is drawn in blue. This partitioning of the E-field is influenced by the potential of the gates and by the inversion charge underneath the gates. It shields the gate from the drain issued E-field. Considering that at the bottom gate with increasing $V_{gs-bottom}$ l_d decreases, more and more electric field lines effect the top gate. On the opposite at the top gate with increasing $V_{gs-bottom}$ l_d increases (Fig. 5.5 and 5.4). That means more and more electric field lines influence the saturation behavior of this gate. In Fig. 5.6 less E-field lines of the drain end go into the direction of the bottom gate, because it has a higher voltage than the top gate. Therefore

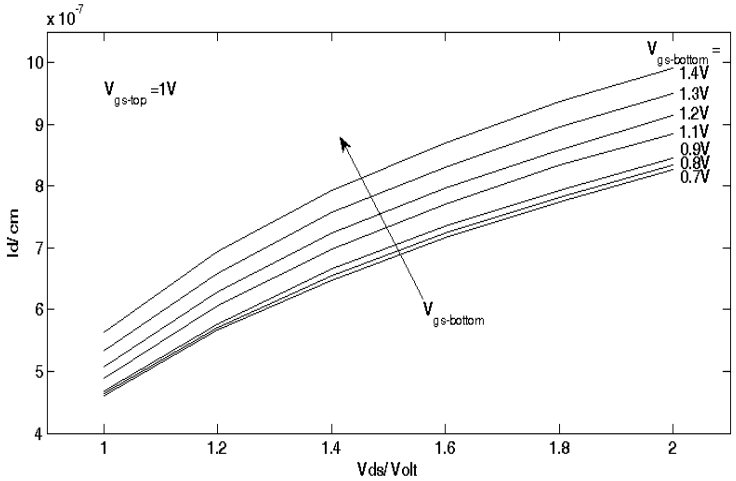


Figure 5.5: Channel length shortening extracted from TCAD Sentaurus simulation for the top gate, where $V_{gs-top} = 1$V constant and $V_{gs-bottom} = 0.7 \cdots 1.4$V. With increasing $V_{gs-bottom}$ l_d increases.

the saturation point of the top gate is located a little but further away from the drain. With a lower bottom gate voltage (Fig. 5.7) more field lines into the direction of the bottom gate. Which results in a saturation point at the top gate located closer to the drain end. We assume an imaginary border, which separates the electric field lines going into the direction of the top gate and the bottom gate.

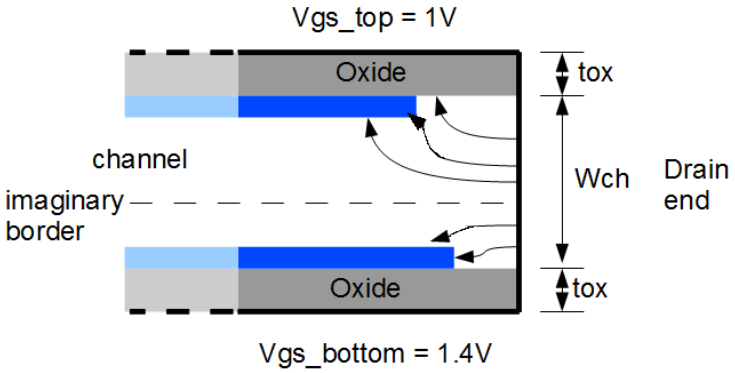


Figure 5.6: Drawing of the drain end, whereby the inversion charge is drawn in blue. Because the top-gate has a lower voltage more E-field lines influence the saturation behavior of the that channel.

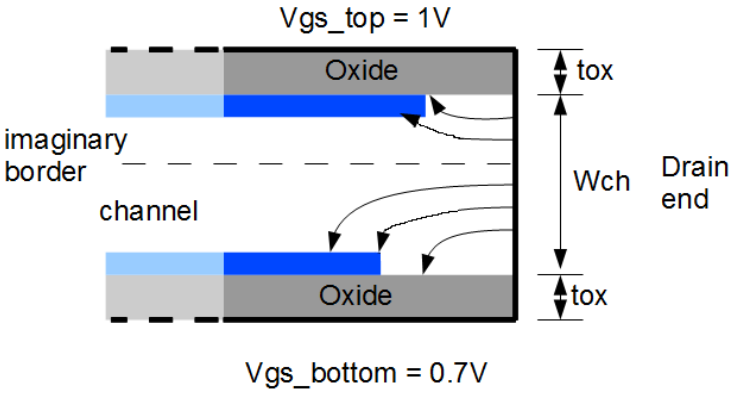


Figure 5.7: Drawing of the drain end, whereby the inversion charge is drawn in blue. Because the top-gate has a higher voltage more E-field lines influence the saturation behavior of the bottom-gate channel.

5.2 Model

The outline of our approach how we calculate the channel length modulation is shown in Fig. 5.11. We split the DG MOSFET in an even and odd mode [106].

even $V_{ds} = V_{ds}$

$$V_{gs-even} = \frac{V_{gs-bottom} + V_{gs-top}}{2}. \tag{5.1}$$

odd $V_{ds} = 0$

$$\begin{aligned} V^{+}_{gs-odd} &= V_{gs-bottom} - \frac{V_{gs-bottom} + V_{gs-top}}{2} \\ V^{-}_{gs-odd} &= V_{gs-top} - \frac{V_{gs-bottom} + V_{gs-top}}{2} \end{aligned} \tag{5.2}$$

Whereby V_{ds} is the drain-source voltage, $V_{gs-bottom}$ and V_{gs-top} are the gate-source voltages of bottom and top gate, respectively. $V_{gs-even}$ is the average gate voltage of bottom and top and V^{+}_{gs-odd} and V^{-}_{gs-odd} are two virtual parameters to calculate the odd mode.

With the even mode we calculate an initial ld_{guess} by using the approach described in section 4 for the symmetrically biased DG MOSFET. Here we assume a parabolically shaped electric potential at this saturation point (refer to Fig. 5.8). For this we simply take two points slightly beside the middle of the channel of the device and calculate the potential Φ with Eqn. (4.21)

$$\Phi_{even} = y^2 + ay + b \tag{5.3}$$

With the odd mode we assume a linearly shaped function for the electric potential as shown in Fig. 5.9

$$\Phi_{odd} = \frac{V^{-}_{gs-odd} - V^{+}_{gs-odd}}{2 \cdot t^{\sim}_{ox} + T_{ch}} \cdot y + V^{+}_{gs-odd}. \tag{5.4}$$

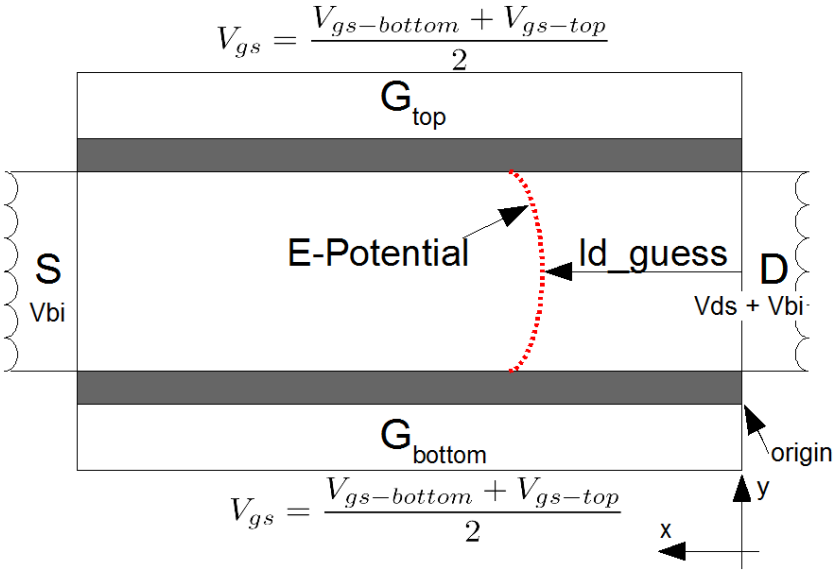


Figure 5.8: For an asymmetrically biased DG MOSFET we split up in an even and odd mode. With the even mode one pinch-off point between the two real pinch-off points is calculated as first guess.

In the odd mode is $V_{ds} = 0$, therefore no influence of the drain end needs to be calculated.

After re-superpositioning of even and odd mode we can calculate the minimum of this deformed parabolically shaped function. The position of the minimum of the potential along the channel gives a theoretically existing drain effect border as drawn in Fig. 5.10

$$\frac{d\left(\Phi_{even} + \Phi_{odd}\right)}{dy} = 0. \tag{5.5}$$

With this border we can determine what part of the drain region effects which gate. To come to the channel length shortening the device is split up at this border and two virtual DG MOSFETs are created, each with a new channel thickness. Now we apply the initial two gate voltages and can calculate two different pinch-off points from two virtual devices having different channel thickness T_{ch}.

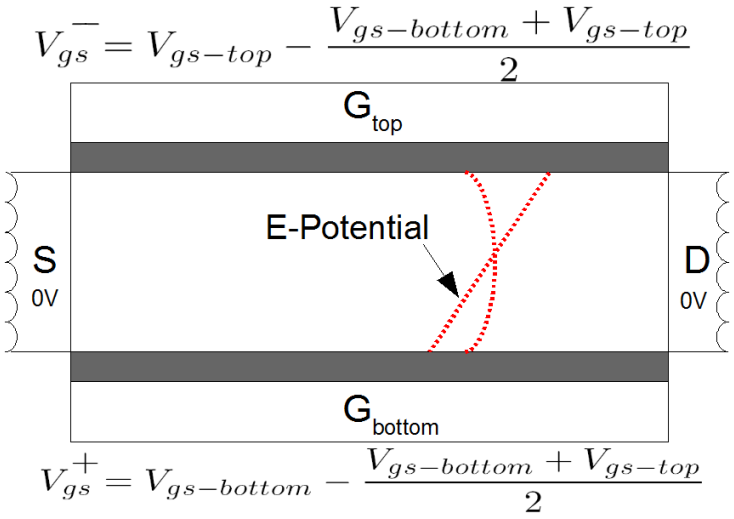


Figure 5.9: With the odd mode a linear function for the electric potential is calculated.

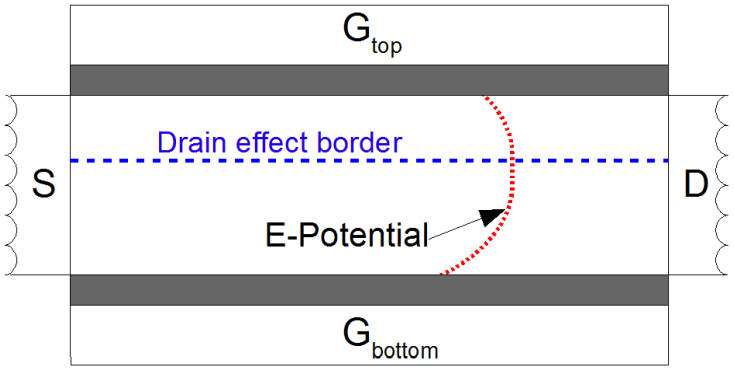


Figure 5.10: The superposed electric potentials calculated by even and odd mode create a shifted parabolic function, whereby the lowest point creates a virtual border for the impact area of the drain onto each gate. With this border the device is split up into two devices with individual channel width so the two pinch-off points can be calculated.

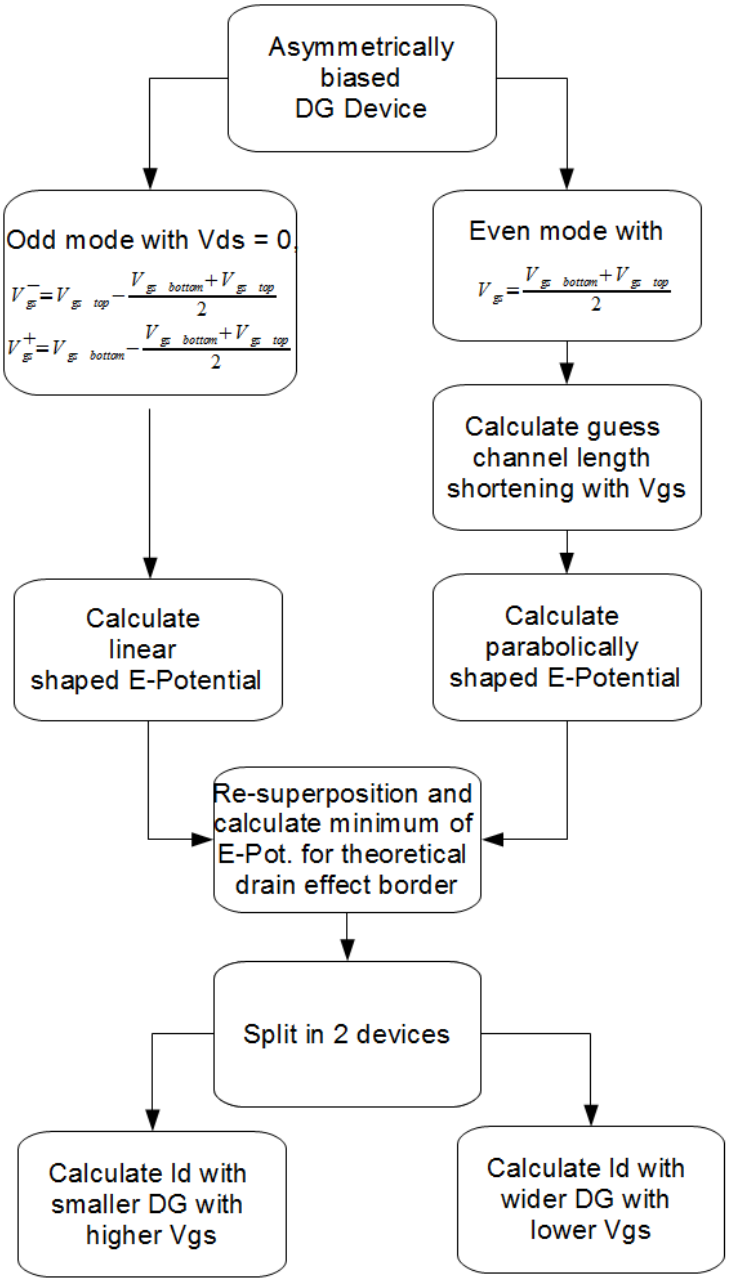


Figure 5.11: Outline of the calculation of channel length modulation of a asymmetrical biased DG MOSFET. The device is parted in an even and odd mode. With that a virtual drain effect border can be determined to create two new devices, each with a different channel length modulation.

5.3 Results

To compare our model results from TCAD Sentaurus [10] were extracted. The simulated DG MOSFET has a channel thickness $T_{ch} = 10$nm and length $L_{ch} = 50$nm. In Fig. 5.12 the results of TCAD Sentaurus for the bottom gate are drawn in symbols, $V_{gs-bottom} = 0.8 \cdots 1.3$V and constant $V_{gs-top} = 1$V. Our model is drawn in lines. Fig. 5.13 represents the same conditions for the top gate.

Considering that the model is fitted with a fixed critical electrical field of $\mathcal{E}_c = 10^6 \frac{V}{cm}$, a $\theta = 0.057$ for influence of V_{gs} on the mobility and a inversion potential $\phi_i - 0.123$V for all plots, which are the fitting parameters already introduced for the symmetrically biased DG MOSFET, our model describes the channel length shortening very well. The disagreement between model and TCAD Sentaurus is in maximum about 0.1nm, which is a good result.

Fig. 5.14 and 5.15 show the virtual channel width of the corresponding DG for the bottom and top gate, respectively. The virtual DG with the wider channel relates to the gate with the lower applied voltage. Interesting to see, that the model predicts, that the with increasing drain-source voltage this effect is stronger.

This proofs the strong physical relation of our model. Also our theory that the pinch-off point of an asymmetrically biased DG FET can be calculated with two individual devices was proven.

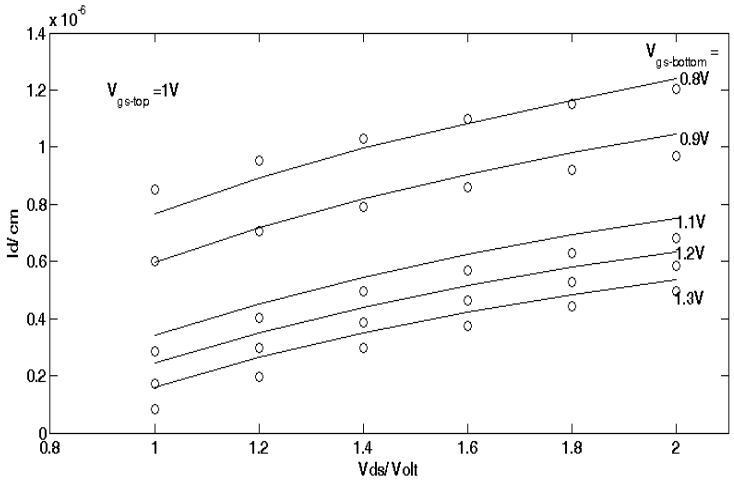


Figure 5.12: Channel length shortening extracted from TCAD Sentaurus simulation for the bottom gate, where $V_{gs-bottom} = 0.8 \cdots 1.3$V and constant $V_{gs-top} = 1$V in symbols. Our model is drawn in lines. The model describes the behavior very well.

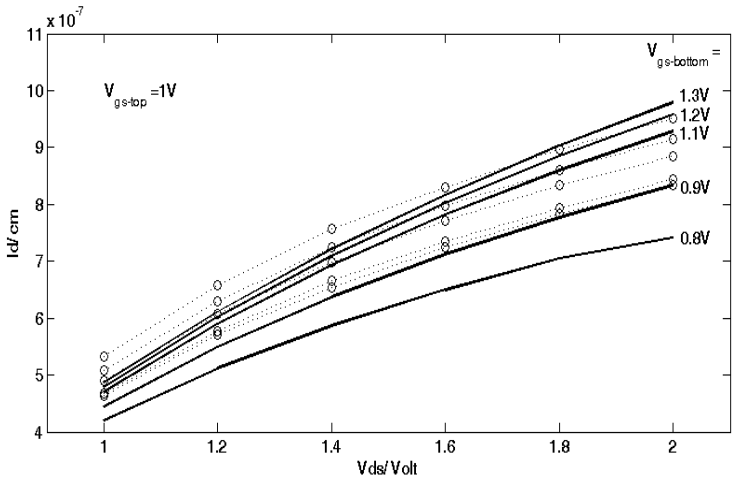


Figure 5.13: Channel length shortening extracted from TCAD Sentaurus simulation for the top gate, where $V_{gs-top} = 1$V constant and $V_{gs-bottom} = 0.8 \cdots 1.3$V in symbols with dotted lines. Our model is drawn in solid lines. The disagreement between model and TCAD Sentaurus is in maximum about 0.1nm, which is a good result.

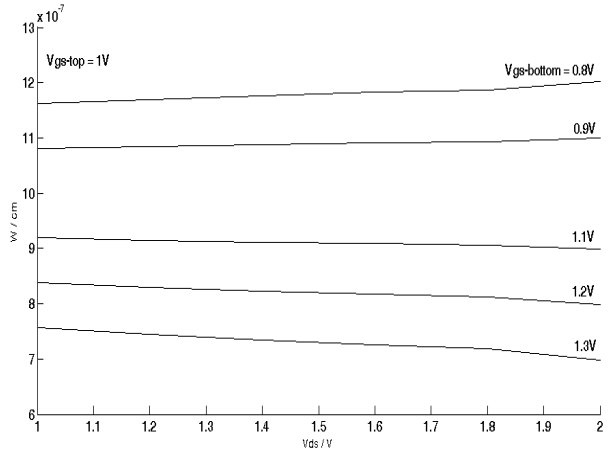


Figure 5.14: Calculated virtual channel width of the DG corresponding to the bottom gate, where $V_{gs-bottom} = 0.8 \cdots 1.3$V and constant $V_{gs-top} = 1$V. The wider channel relates to the gate with the lower applied voltage and this effect increases with higher V_{ds}.

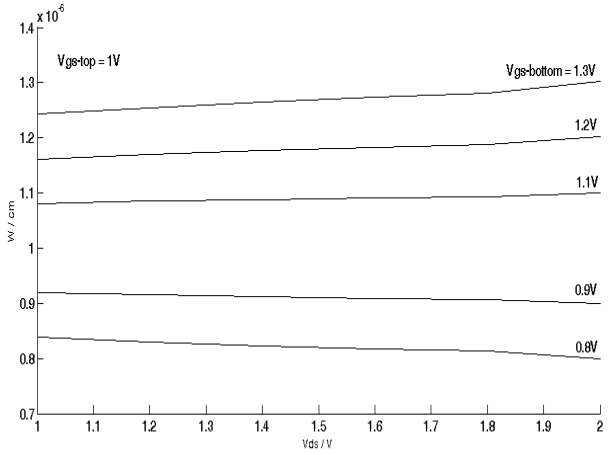


Figure 5.15: Calculated virtual channel width of the DG corresponding to the top gate, where $V_{gs-bottom} = 0.8 \cdots 1.3$V and constant $V_{gs-top} = 1$V. The wider channel relates to the gate with the lower applied voltage and this effect increases with higher V_{ds}.

Chapter 6

FinFET

In this chapter simulation results for a FinFET will be given. These simulations are done in three dimensions in order to take the effect of the gate corner correctly into account. Nevertheless the device is symmetric along the z-axis as shown in Fig. 6.1(a), out of it the FinFET is cut into half in order to save simulation time. The cut position is shown in Fig. 6.1(b). For the results the FinFET is mirrored again to receive the full device. In Table 6.1 the parameters are listed. Again the simulations are done with Sentaurus [10], whereby a drift-diffusion model with high field saturation is used. The here presented results are obtained by analyzing the complete 3D data set.

Table 6.1: Parameters for the simulated FinFET

Parameter	Value
channel width	10nm
channel length	50nm
channel height	20nm
oxide thickness	2nm
ϵ_{ox}	7
substrate doping concentration	10^{15}cm^{-3}
source drain doping profile	constant
source/drain doping concentration	10^{20}cm^{-3}

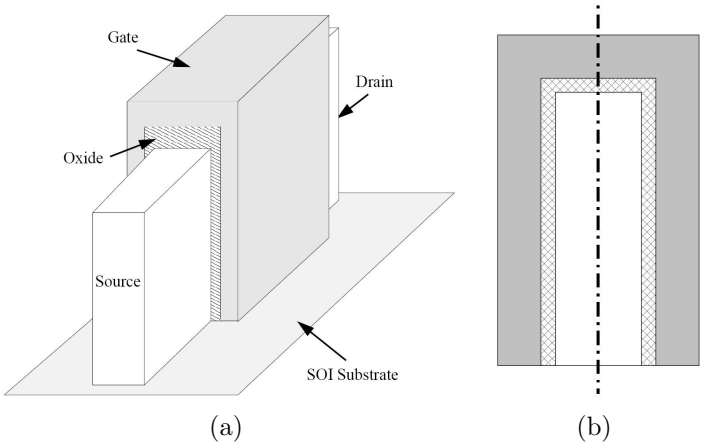


Figure 6.1: In (a) is shown the structure which is used for the FinFET simulation. The gate surrounds the fin at three sides. In (b) the front view of the FinFET is drawn. The line indicates the cut-position at which the device is halved [104], [107].

6.1 Point of Saturation

Figure 6.2 shows the path of the maximum electron current density. Here a cut-out of the channel is presented with a width of 10nm in z-direction, a length of 50nm in x-direction and a height of 20nm. The electron current density maximum is located first in the corners underneath the gate oxide. While going along the channel the electron current density maximum suddenly moves into the middle of the channel.

With a look on Fig. 6.3 it turns out that at this point the maximum electric potential moves from the top of the channel to the bottom. It can be assumed that here the whole channel is in saturation and therefore the current flow expands through the whole channel. At this point the pinch-off point is considered to be. The slow movement of the electric potential minimum from the bottom of the device to the top let assume that saturation starts at the bottom region of the channel. With less distance to the drain side more and more of the channel region comes to saturation. A reason might be that a surrounding gate in the upper region of the channel has a stronger control and the lower region has just a gate at the two sides. The device might be

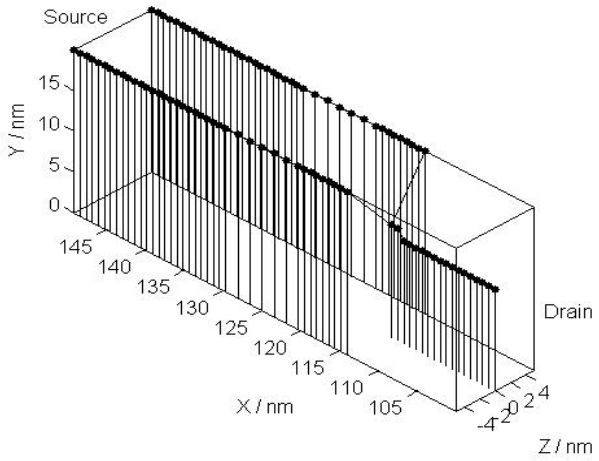


Figure 6.2: Path of the electron current density maximum. At source side above threshold the maximum is within the corners underneath the gate oxide. Going in drain direction the maximum moves to the middle of the channel[108, 109, 110]. Bias conditions: $V_{gs} = 0.05$V; $V_{ds} = 1.4$V.

treated as DoubleGate MOSFET in saturation on the bottom with a FinFET on top.

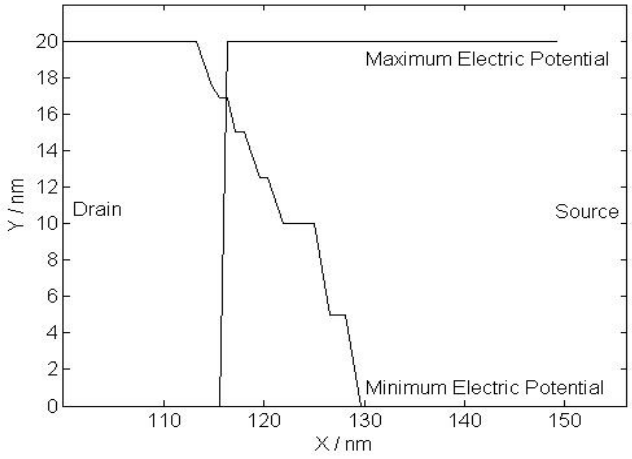


Figure 6.3: Maximum and minimum electric potential along the x-y coordinates [29]. Bias conditions: $V_{gs} = 0.05$V; $V_{ds} = 1.4$V

6.2 Saturation Voltage and Channel Length Shortening

As mentioned before the point when the electric field maximum moves suddenly from the top of the channel to the bottom of the channel is considered as pinch-off point. In the following results for the channel length shortening and the saturation voltage at pinch-off point are presented. Figure 6.4 and 6.5 show the channel length shortening l_d and the saturation voltage V_{dsat} at the bottom of the device, when the electric potential maximum moves from the top gate to the bottom of the device, for several gate-source voltages V_{gs}.

As already known from the Bulk MOSFET geometry the channel length shortening increases with higher drain-source voltage V_{ds}. Also a higher V_{gs} reduces l_d, because the higher gate voltage has a higher control on the current flow. The corresponding V_{dsat} is static for one V_{gs}.

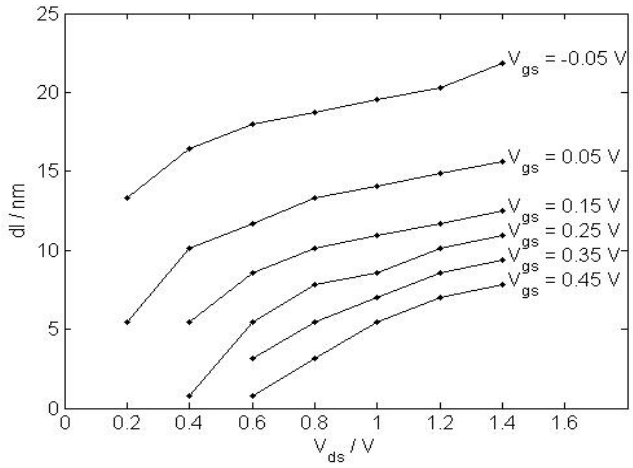


Figure 6.4: Channel length shortening l_d for various V_{gs} and V_{ds} is shown extracted with [10].

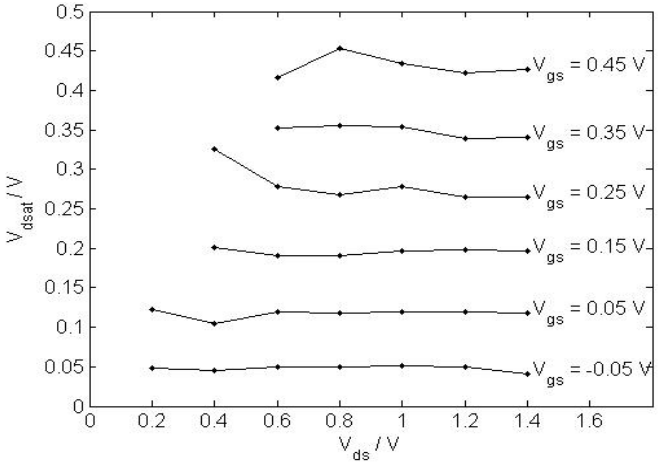


Figure 6.5: Saturation voltage for the channel length shortening in Fig. 6.4 for various V_{gs} and V_{ds} is shown extracted with [10].

6.3 Ideas for Modeling Approaches

In [69], [104] and [107] the modeling approach for the threshold voltage is a DoubleGate device in the bottom, which defines the most leaky path. For the saturation point, the saturation start at the bottom area (it can be defined as DG MOSFET with no applied source-bulk voltage) and goes up until it reaches top gate. The question is now, is such a preceise calculation necessary or is it just fine to use a saturation point inbetween to have a reasonable value for the channel length shorting?

The Schwarz-Christoffel conformal mapping technique [75] is limited to 2 dimensional problems. It will not be possible to include all three gates and the drain side into one approach. The idea so far is to place a 2-corner structure as shown in Fig. 6.6. The 2 corner structure includes the top oxide, goes a long the drain interface and then along the bottom of the device at the buried oxide interface as shown in Fig. 6.7.

The big advantage is, the bulk-source voltage V_{sb} is included. On the drain side, the already known boundary conditions from chapter 4 are used, except one oxide is missing. The issue might be the definition of the upper boundary condition with

$$V_{upper-boundary} = V_{gs-top} + Vd'. \tag{6.1}$$

The virtual voltage Vd' has to include the effects the side gates have on the saturation point. Assuming all three gates have the same voltage applied, Vd' can not be 0, because the electric field in the upper corners of the device is much higher compared to everywhere else. The advantage of the approach is, it includes the influence of the source-bulk voltage V_{sb}. Furthermore, the exact location of the saturation point will be given by the minimum of the calculated boundary at the saturation point side. An approximation of the characteristics are given in Fig. 6.7. If $V_{gs-top} + Vd' \neq V_{sb}$ the minimum of the boundary will not be in the middle of the channel. Therefore, probably, a

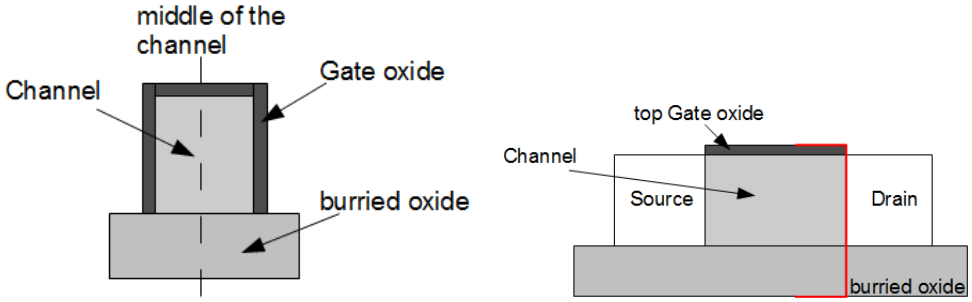


Figure 6.6: In (a) is shown the structure which is used for the FinFET simulation. The gate surrounds the fin at three sides. In (b) the cut of the FinFET in the middle of the channel is drawn. The line indicates the cut-position at which the device is halved [30], [31]

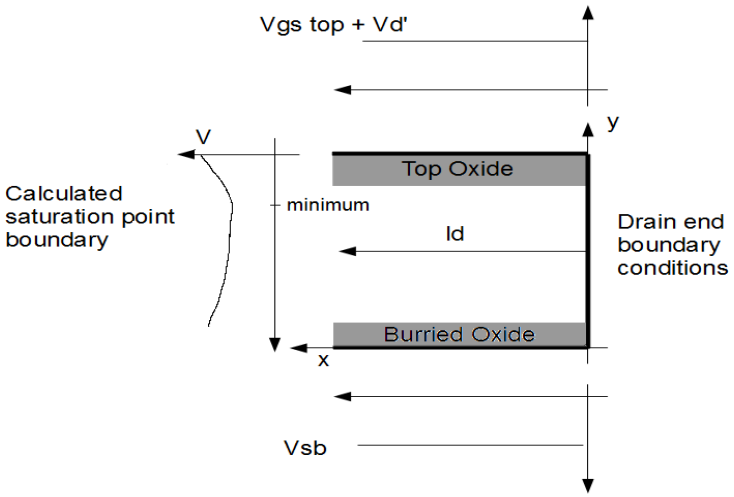


Figure 6.7: The cut out of the channel length shortening in the middle of the channel is drawn, as indicated in red lines in Fig. 6.6b. With $V_{gs-top} + Vd' \neq V_{sb}$ the saturation point will not occur in the middle of the channel first. The voltage along the saturation point border on the left side will not be symmetrically shaped, instead a quadratic function with a minimum will occur. This minimum indicates the position of the saturation point along the z-direction of the FinFET.

reasonable value inbetween saturation point for the bottom of the device and the top of the device can be obtained.

The saturation point can either be defined by a voltage, what might be difficult to define or if a certain slope of the calculated saturation point boundary conditions is reached.

Chapter 7

Conclusion

7.1 Single Gate Bulk MOSFET Channel Length Shortening

The presented model calculates the electric field in a closed-form at the pinch-off point by solving 2D Poisson. To come to the channel length shortening the saturation voltage Vd_{sat} is calculated with a given electric field in the pinch-off point $\mathcal{E}_p$. By recalculating the electric field at the pinch-off point by taking into account the drain source voltage Vds and the saturation voltage, the model varies the channel length shortening until the solution of the 2D Poisson equation agrees with the recalculated electric field in the pinch-off point. To receive a fully closed-form analytical model a few values of the channel length modulation can be calculated and connected by a polyfit function. The only fitting parameter in this model is the given electric field at the pinch-off point $\mathcal{E}_p$ from that the saturation voltage V_{dsat} is calculated. This fitting parameter has a second order influence on the model results, as shown in chapter 3.6. Todays channel length shortening models so far have fitting parameter with a huge influence on the model.

With this model a new way of calculating the channel length is shown. in general the simulation results simulated with TCAD Sentaurus [10] fit with the model results. For 700nm down to 500nm the total value of the output conductance is in a not that good agreement, but the the relative variation of V_{ds} with respect to V_{gs} is accurately described, particular if considered that the fitting parameter $\mathcal{E}_p$ is not changed. Applying the model to smaller device geometries with 50nm up to 100nm the total value of the output conductance is very well predicted. Considering the fitting parameter $\mathcal{E}_p$ is changed from $\mathcal{E}_p = 10^5$V/cm for 700nm down to 500nm to $\mathcal{E}_p = 2 \cdot 10^5$V/cm for 100nm down to 50nm the model proofs its excellent scalability.

7.2 DG MOSFET Channel Length Shortening

To calculate the channel length shortening in the DG MOSFET a fully 2D model was created. This model calculates the saturation voltage at pinch-off point with Schwarz-Christoffel conformal mapping technique [75]. This point is compared to a defined saturation voltage. The model is in closed form and contains only two fitting parameters with minor influence to adjust the critical electric field in high field saturation region and the inversion charge. Those parameters move the entire curve set of the model in a $x - y$-graph up and down and have no influence on the slope of the curve. In order to compare the channel length shortening to TCAD Sentaurus [10] simulation results, a new method to define the saturation point was developed. Hereby the saturation point is determined, when the electric potential maximum moved from the Silicon-SiliconOxide interface into the middle of the channel. Also some simulations including quantum mechanics were done. It showed, that with quantum mechanics the same effect occurs and therefore a saturation point exists.

The model fits very well to simulation results for a channel length of 50nm

and a channel width of 10nm. The fitting parameter for the critical electric field $\mathcal{E}_c = 10^6\text{V/cm}$ stayed unchanged for all devices. The results fit very well. Also for a smaller device channel length of 20nm and a channel width of 10nm the model described the channel length shortening very well. For the shorter device, the inversion charge needed to be adjusted. With a wider channel of 20nm and a channel length of 50nm the model shows equally good results.

In a next step a asymmetrically biased DG MOSFET was simulated with a channel length of 50nm and a channel width of 10nm. It turned out, that two channels with different saturation points occur at the Silicon-SiliconOxide interface. After evaluating the position of the saturation point, it was found, both gates influence each other. To include the effect in the model, the asymmetrically biased DG MOSFET has to be split into two separate symmetrically biased DG MOSFET with two different channel widths according to the applied voltages. An even and odd mode was created, which enabled the possibility to define the two virtual DG MOSFETs.

The model describes the asymmetrically biased DG MOSFET very well. Considering one gate as constantly biased with 1V and the other one with $0.7\text{V} \cdots 1.3\text{V}$, the model describes the small influence the variation of the gate voltage has on the channel length shortening at the constantly biased gate. Also the model creates a very good description for the huge changes of the saturation point position for the gate applied with $0.7\text{V} \cdots 1.3\text{V}$.

7.3 FinFET Channel Length Shortening

As shown in the 3D analysis of the pinch-off point in FinFET in chapter 6 the pinch-off point in this geometry moves from the bottom of the device to the top until the whole channel is in saturation, if no source-bulk voltage is applied. This makes a more dimensionally modeling approach necessary.

Since the conformal mapping technique is limited to 2 dimensions, it will

not be possible to include a FinFET as entire device. Having in mind, that it might be unnecessary to calculate the exact way the saturation point has from the bottom to the top of the device, an idea for an modeling approach was presented. With that, a pinch-off point location can be determined, whereby the location not only depends on the drain-source/gate-source voltage, but also depends on the applied source-bulk voltage and gate voltage in terms of vertical position.

Overall it can be said, that 2D models created by nonlinear mapping technique are very difficult to develop and the mathematical effort is huge. Nevertheless, because of their close relation to the semiconductor physics they often have very few fitting parameters and those fitting parameter have minor influence.

Appendix A

Closed Form Solution of 2D Poisson's Equation

In here is shown that the integration system to calculated 2D Poisson equation presented in section 4.2.1 can be solved in analytical closed form solution.

Basically three integrals need to be solved, since the boundary conditions are symmetrically and therefore the equations are similar. Those integrations are

- **② to ③**

$$\Phi_{23}(u,v) = \frac{1}{\pi}\int_{x=ld}^{x=0} \frac{v}{v^2+(u-\overline{u})^2} \cdot \mathcal{E}_p \cdot (\operatorname{arccosh}(\overline{u})\frac{\triangle\, y}{\pi} - ld)d\overline{u} \quad \text{(A.1)}$$

- **③ to ④**

$$\Phi_{34}(u,v) = \frac{1}{\pi}\int_{y=0}^{y=t_{ox}^{\sim}} \frac{v}{v^2+(u-\overline{u})^2} \cdot \left(\frac{V_{gs}-V_{fb}-V_{ds}-V_{bi}}{t_{ox}^{\sim}} \cdot \operatorname{arccosh}(\overline{u})\frac{\triangle\, y}{\pi} - \mathcal{E}_p \cdot ld\right) d\overline{u}. \quad \text{(A.2)}$$

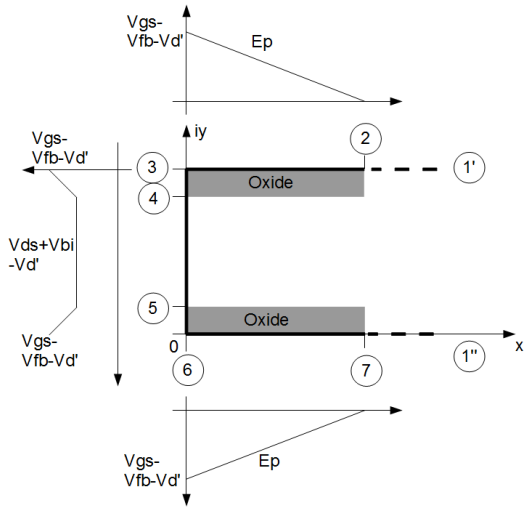


Figure A.1: Boundary conditions in z-plane.

- **④ to ⑤**

$$\Phi_{45}(u,v) = \frac{1}{\pi}\int_{y=t_{ox}^{\sim}}^{y=T_{ch}+t_{ox}^{\sim}} \frac{v}{v^2+(u-\overline{u})^2}\cdot\left(V_{ds}+V_{bi}-\mathcal{E}_p\cdot ld\right)d\overline{u} \quad \text{(A.3)}$$

In Fig. A.1 the estimated characteristics of the boundary conditions in z-plane are printed. After transforming those into w-plane constant boundary conditions stay constant by, whereby linearly shaped functions in z-plane become a cosine hyperbolic function, see Fig. A.2.

Essentially this hyperbolic cosine term can be replaced by a Taylor series. Fig. A.2 shows that hyperbolic cosine terms occur when going along ld and through the oxide. Looking at other results in Fig. 4.23 for a channel length of 50nm and a channel width of 10nm a maximum ld of 9nm is given. In a small range like this an arc hyperbolic cosine function can be replaced by a square-root approximation. The advantage here, beginning and end point of the interesting part of the square-root approximation are defined by the corners of the structure. The inaccuracy increases with a higher ld and $t_{ox}^{\sim}$. With $ld = 9$nm difference between integral along the function and the approximation of less than 1% is reached.

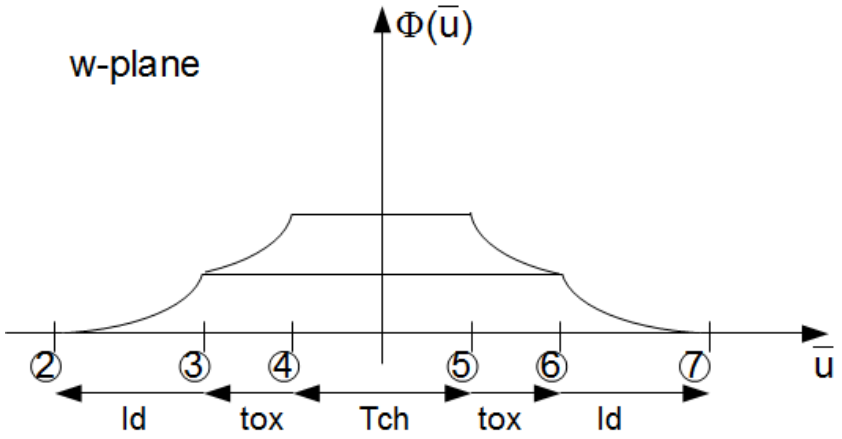


Figure A.2: Estimated characteristics of the transformed boundary potential $\Phi(\overline{u})$. It is shown that constant boundary conditions stay constant by transforming those from z-plane to w-plane, whereby linearly shaped functions in z-plane become a cosine hyperbolic function, which can be substituted by a parabolically shaped function.

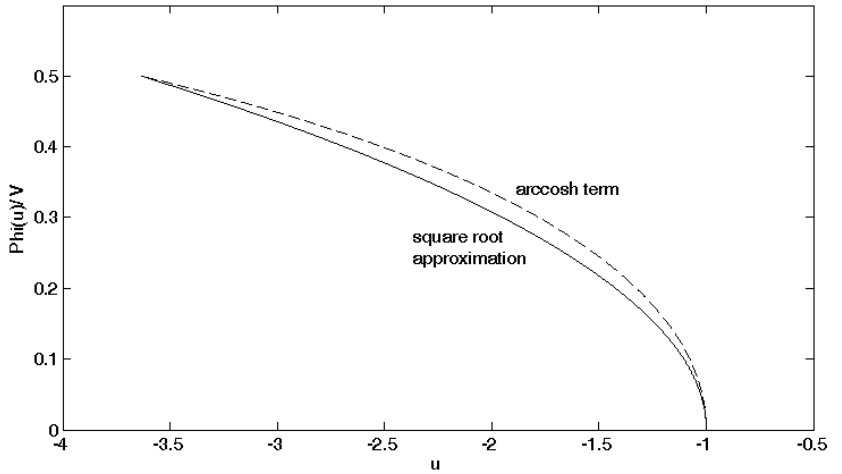


Figure A.3: Comparison between real value of $\Phi(\overline{u})$ of the arc hyperbolic cosine function and a square root approximation along the boundary u over a length of transformed 10nm.

Fig. A.3 shows the comparison between real value of $\Phi(u)$ of the arc hyperbolic cosine function and a square root approximation along the boundary u over a length of transformed 10nm. Since the oxide even when transformed into $t_{ox}^{\sim}$ is less than 5nm the results have no noticeable difference.

② to ③ To solve the potential coming from $\Phi_{23}(u,v)$ in Eqn. (A.1), the Eqn. Is split into an constant

$$\Phi_{23-const}(u,v) = \frac{1}{\pi}\int_{x=ld}^{x=0} \frac{v}{v^2+(u-\overline{u})^2}\cdot\left(-\mathcal{E}_p\cdot ld\right)d\overline{u} \tag{A.4}$$

and the arc hyperbolic cosine term

$$\Phi_{23-square}(u,v) = \frac{1}{\pi}\int_{x=ld}^{x=0} \frac{v}{v^2+(u-\overline{u})^2}\cdot\mathcal{E}_p\cdot\operatorname{arccosh}(\overline{u})\frac{\triangle\, y}{\pi}d\overline{u}. \tag{A.5}$$

For the constant part the result is simply

$$\Phi_{23-const}(u,v) = -\frac{1}{\pi}\cdot\mathcal{E}_p\cdot ld\cdot\left(\arctan\left(-a+u\right)/v\right) - \arctan\left((u+1)/v\right)\right). \tag{A.6}$$

The first arc tangent term $\arctan\left(-a+u\right)/v)$ defines the upper boundary with

$$a = \cosh\left(\pi\cdot\frac{ld+j\cdot(2\cdot t_{ox}^{\sim}+T_{ch})}{2\cdot t_{ox}^{\sim}+T_{ch}}\right). \tag{A.7}$$

The lower boundary is defined by the other arc tangent term $\arctan\left((u+1)/v\right)$, whereby here the lower boundary transformed into w plane is -1, as explained in section 2.6.2.

The arc hyperbolic cosine term $\mathcal{E}_p\cdot\operatorname{arccosh}(\overline{u})\cdot\frac{\triangle y}{\pi}$ needs to be replaced with a square root approximation. First the beginning point of this part

$$z = (T_{ch}+2\cdot t_{ox}^{\sim}) + j\cdot(ld) \tag{A.8}$$

and the end point

$$z = (T_{ch}+2\cdot t_{ox}^{\sim}) + j\cdot(0) \tag{A.9}$$

needs to be defined. As well as the corresponding transformation into w-plane

$$w = \cosh\left(\frac{(ld + j\cdot \triangle\, y)\cdot\pi}{\triangle\, y}\right) \tag{A.10}$$

and

$$w = \cosh\left(\frac{j\cdot \triangle\, y\cdot\pi}{\triangle\, y}\right), \tag{A.11}$$

with $\triangle\, y = T_{ch} + 2\cdot t_{ox}^{\sim}$. As square-root approximation function is used,

$$\sqrt{\frac{x - \cosh\left(\frac{j\cdot\triangle y\cdot\pi}{\triangle y}\right)}{p}} \tag{A.12}$$

with the slope of

$$p = \frac{\cosh\left(\frac{(ld+j\cdot\triangle y)\cdot\pi}{\triangle y}\right) - \cosh\left(\frac{j\cdot\triangle y\cdot\pi}{\triangle y}\right)}{(\mathcal{E}_p\cdot ld)^2}. \tag{A.13}$$

Putting this in Eqn. (A.5) we have

$$\Phi_{23}(u,v) = \frac{1}{\pi}\int_{x=ld}^{x=0}\frac{v}{v^2+(u-\overline{u})^2}\cdot\left(\sqrt{\frac{x-\cosh\left(\frac{j\cdot\triangle y\cdot\pi}{\triangle y}\right)}{p}} - \mathcal{E}_p\cdot ld\right)d\overline{u} \tag{A.14}$$

The result for the square root part of the integration system is more complicated,

$$\begin{aligned}\Phi_{23-square}(u,v) =& \frac{1}{(4\cdot\pi)}\cdot(1/p)^{(1/2)}\cdot(\\ & 4\cdot\arctan((2\cdot(a+1)^{(1/2)} + K_+(u,v))/K_-(u,v))\cdot v^2\\ & -4\cdot\arctan((-2\cdot(a+1)^{(1/2)} + K_+(u,v))/ + K_-(u,v))\cdot v^2)/v/K_-(u,v))\end{aligned} \tag{A.15}$$

with

$$K\pm(u,v) = \left(2\cdot\left(u^2+2\cdot u+v^2+1\right)^{(1/2)} \pm 2\cdot u \pm 2\right)^{(1/2)}. \tag{A.16}$$

The constant a in Eqn. (A.15) is the same as in Eqn. (A.6), because the points where the boundaries are located do not change, $a = \cosh\left(\pi \cdot \frac{ld+j\cdot(2\cdot t_{ox}^{\sim}+T_{ch})}{2\cdot t_{ox}^{\sim}+T_{ch}}\right)$.

③ to ④ This equation is very similar to the problem in the previous section. It contains an $\mathcal{E}_p \cdot \operatorname{arccosh}(\overline{u}) \cdot \frac{\triangle y}{\pi}$ term, that is replaced by a square root approximation

$$\Phi_{34}(u,v) = \frac{1}{\pi}\int_{x=ld}^{x=0} \frac{v}{v^2+(u-\overline{u})^2} \cdot \left(\sqrt{\frac{y-\cosh\left(\frac{j\cdot\triangle y\cdot\pi}{\triangle y}\right)}{q}} - \mathcal{E}_p \cdot ld\right) d\overline{u} \tag{A.17}$$

with

$$q = -\frac{\cosh\left(\frac{(0+j\cdot\triangle y)\cdot\pi}{\triangle y}\right) - \cosh\left(\frac{j\cdot(T_{ch}+t_{ox}^{\sim})\cdot\pi}{\triangle y}\right)}{(V_{gs}-V_{fb}-V_{ds}-V_{bi})^2}. \tag{A.18}$$

Again the equation can be split up in an constant part with

$$\Phi_{34-const}(u,v) = -\frac{1}{\pi}\cdot\mathcal{E}_p\cdot ld\cdot\left(\arctan\left(-b+u\right)/v\right) - \arctan\left((u+1)/v\right)) \tag{A.19}$$

and b defined as

$$b = \cosh\left(\pi\cdot\frac{ld+j\cdot(t_{ox}^{\sim}+T_{ch})}{2\cdot t_{ox}^{\sim}+T_{ch}}\right). \tag{A.20}$$

And the expression for the square root part of the integration system,

$$\begin{aligned}\Phi_{34-square}(u,v) =& \frac{1}{(4\cdot\pi)}\cdot(1/q)^{(1/2)}\cdot(4\cdot\arctan((2\cdot(b+1)^{(1/2)} \\ &+ K_+(u,v))/K_-(u,v))\cdot v^2 - 4\cdot\arctan((-2\cdot(a+1)^{(1/2)} \\ &+ K_+(u,v))/ + K_-(u,v))\cdot v^2)/v/K_-(u,v)\end{aligned} \tag{A.21}$$

with

$$K\pm(u,v) = \left(2\cdot\left(u^2+2\cdot u+v^2+1\right)^{(1/2)} \pm 2\cdot u \pm 2\right)^{(1/2)}. \tag{A.22}$$

④ to ⑤ This part only contains constant parts. So the result is without

any approximation:

$$\Phi_3 = -\frac{1}{\pi} \cdot \left(V_{ds} + V_{bi} - \mathcal{E}_p \cdot ld\right) \cdot \left(\arctan\left(-c + u\right)/v\right) - \arctan\left(\left(-d + u\right)/v\right)\right). \tag{A.23}$$

For c and d the upper and lower boundary of the integration system are used,

$$c = \cosh\left(\pi \cdot \frac{ld + j \cdot (2 \cdot t_{ox}^{\sim} + T_{ch})}{2 \cdot t_{ox}^{\sim} + T_{ch}}\right) \tag{A.24}$$

and

$$d = \cosh\left(\pi \cdot \frac{ld + j \cdot (t_{ox}^{\sim})}{2 \cdot t_{ox}^{\sim} + T_{ch}}\right). \tag{A.25}$$

References

[1] G. Moore, "The role of fairchild in silicon technology in the early days of silicon valley," in *Proceedings of the IEEE*, vol. 86, no. 1, 1998, pp. 53–62.

[2] G. Moore, "Cramming more components onto integrated circuits," *Electronics*, vol. 38, no. 8, p. 114ff, April 1965.

[3] [Online]. Available: www.itrs.net

[4] J.-P. Colinge, M.-H. Gao, A. Romano, H. Maes, and C. Claeys, "Silicon-on-insulator 'gate-all-around' mos device," in *IEEE SOS/SOI Technology Conference 1990*, 1990, pp. 137–138.

[5] J.-P. Colinge, "Evolution of soi mosfets: from single gate to multiple gates," in *2003 Spring Meetings Proceedings, MRS Proceedings*, 2003.

[6] S. Cristoloveanu, "Silicon on insulator technologies and devices: from present to future," *Solid-State Electronics*, vol. 43, pp. 1403–1411, 2001.

[7] C. Hu, M. Dunga, C.-H. Lin, D. Lu, and A. Niknejad, "Compact modeling for new transistor structures," in *Conference on Simulation of Semiconductor Devices and Processes (SISPAD)*, 2007, pp. 285–288.

[8] J.-P. Colinge and C.-A. Colinge, *Physics of Semiconductor Devices*. Springer Verlag/ Wien, 2002.

[9] *ATLAS User's Manual DEVICE SIMULATION SOFTWARE*, SILVACO, Inc., 4701 Patrick Henry Drive, Bldg. 1, Santa Clara, CA 95054, September 2010.

[10] *TCAD Sentaurus*, X-2005.10 ed., Synopsys, Inc., 2005.

[11] K.-T. Grasser, *Minimos-NT Device and Circuit Simulator*, Institute for Microelectronics, TU Vienna, September 2002.

[12] Berkley, *SPICE3 Version 3e Users Manual*, University of California, 1991.

[13] *ELDO User's Manual*, Anacad GmbH.

[14] Y. Cheng, M.-C. Jeng, Z. Liu, J. Huang, M. Chan, K. Chen, P. K. Ko, and C. Hu, "A physical and scalable i-v model in bsim3v3 for analog/digital circuit simulation," *IEEE Trans. Electron Devices*, vol. 44, no. 2, pp. 277–287, 1997.

[15] N. D. Arora, R. Rios, C.-L. Huang, and K. Raol, "Pcim: a physically based continuous short-channel igfet model for circuit simulation," *IEEE Trans. Electron Devices*, vol. 41, no. 6, pp. 988–997, 1994.

[16] K. Joardar, "An improved analytical model for collector currents in lateral bipolar transistors," *IEEE Trans. Electron Devices*, vol. 41, no. 3, pp. 373–382, 1994.

[17] C. C. Enz, F. Krummenacher, and E. A. Vittoz, "An analytical mos transistor model valid in all regions of operation and dedicated to low-voltage and low-current applications," *Analog Integr. Circuits Signal Process.*, vol. 8, no. 1, pp. 83–114, 1995.

[18] C. Hu, X. Xi, M. Dunga, J. He, W. Liu, K. M. Cao, X. Jin, J. Ou, M. Chan, and A. Niknejad, *BSIM4.3.0 MOSFET Model*, Department of Electrical Engineering and Computer Sciences University of California, Berkeley, 2003.

[19] J. He, J. Xi, M. Chan, H. Wan, M. Dunga, B. Heydari, A. Niknejad, and C. Hu, "Charge-based core and the model architecture of bsim5," in *Sixth International Symposium on Quality of Electronic Design, 2005. ISQED 2005*, 2005, pp. 96 – 101.

[20] X. Niu, Y. Song, B. Li, W. Bian, Y. Tao, F. Liu, J. Hu, Y. Chen, and F. He, "Tests on symmetry and continuity between bsim4 and bsim5," pp. 263–268, 2007. [Online]. Available: http://dx.doi.org/10.1109/ISQED.2007.157

[21] G. Smit, R. Langevelde, A. Scholten, D. Klaassen, G. Gildenblat, and X. Li, "Psp 102.0," *model documentation*, 2006.

[22] G. Gildenblat, X. Li, W. Wu, H. Wang, A. Jha, R. van Langevelde, G. Smit, A. Scholten, and D. Klaassen, "Psp: An advanced surface-potential-based mosfet model for circuit simulation,," *IEEE Trans. Electron Devices*, vol. 53, no. 9, pp. 1979 – 1993, 2006.

[23] H. Mattausch, M. Miyake, D. Navarro, N. Sadachika, T. Ezaki, M. Miura-Mattausch, T. Yoshida, and S. Hazama, "Hisim2 circuit simulation - solving the speed versus accuracy crisis," *IEEE Circuits and Devices Magazine*, vol. 22, no. 5, pp. 29 – 38, 2006.

[24] H. Mattausch, M. Miura-Mattausch, H. Ueno, S. Kumashiro, T. Yamaguchi, K. Yamashita, and N. Nakayama, "Hisim: The first complete drift-diffusion mosfet model for circuit simulation," in *6th International Conference onSolid-State and Integrated-Circuit Technology, 2001. Proceedings.*, vol. 2, 2001, pp. 861 – 866.

[25] M. Miura-Mattausch, H. Ueno, J. Mattausch, S. Kumashiro, T. Yamaguchi, K. Yamashita, and N. Nakayama, "Hisim: Self-consistent surface-potential mos-model valid down to sub-100nm technologies," in *Technical Proceedings of the 2002 International Conference on Modeling and Simulation of Microsystems*, 2002, pp. 678 – 681.

[26] M. Miura-Mattausch, H. Ueno, M. Tanaka, H. Mattausch, S. Kumashiro, T. Yamaguchi, K. Yamashita, and N. Nakayama, "Hisim: a mosfet model for circuit simulation connecting circuit performance with technology," in *Digest. International Electron Devices Meeting, 2002. IEDM '02*, 2002, pp. 109 – 112.

[27] D. Vasileska and S. Goodnick, *Computational Electronics*. Morgan & Claypool, 2006.

[28] T. Grasser, *Advanced Device Modeling and Simulation (Int. J. High Speed Electron. and Systems)*. World Scientific, 2003.

[29] S. Selberherr, *Analysis and Simulation of Semiconductor Devices*. Wien: Springer-Verlag, 1984.

[30] C. Galup-Montoro and M. Schneider, *Mosfet Modeling for Circuit Analysis And Design*. World Scientific, 2007.

[31] N. Arora, *MOSFET Models for VLSI Circuit Simulation*. Springer-Verlag/ Wien, 1993.

[32] Y. Tsividis, *Operational Modeling of the MOS Transistor*. New York: McGraw-Hill, 1999.

[33] Y. P. Tsividis and K. Suyama, "Mosfet modeling for analog circuit cad: problems and prospects," *IEEE Journal of SSC*, vol. 29, no. 3, pp. 210–216, 1994.

[34] J.-P. Colinge, *Silicon-on-Insulator Technology: Materials to VLSI*, 3rd, Ed. Springer Verlag/ Wien, 2004.

[35] T. A. Fjeldly and M. Shur, "Threshold voltage modeling and the subthreshold regime of operation of short-channel mosfets," *IEEE Trans. Electron Devices*, vol. 40, no. 1, pp. 137–145, 1993.

[36] K. Natori, "Ballistic metal-oxide-semiconductor field effect transistor," *Journal of Applied Physics,*, vol. 76, no. 8, pp. 4879–4890, 1994.

[37] M. S. Lundstrom and Z. Ren, "Essential physics of carrier transport in nanoscale mosfets," *IEEE Trans. Electron Devices*, vol. 48, no. 1, pp. 133–141, 2002.

[38] B. Iniguez, T. A. Fjeldly, A. Lazaro, F. Danneville, and M. J. Deen, "Compact-modeling solutions for nanoscale double-gate and gate-all-around mosfets," *IEEE Trans. Electron Devices*, vol. 53, no. 9, pp. 2128–2142, 2006.

[39] Y. Taur, X. Liang, W. Wang, and H. Lu, "A continuous, analytic drain-current model for dg mosfets," *IEEE EDL*, vol. 25, no. 2, pp. 107–109, 2004.

[40] A. Ortiz-Conde, F. Garcia Sanchez, and M. J., "Rigorous analytic solution for the drain current of undoped symmetric dual-gate mosfets," *Solid State Electronics*, vol. 49, no. 4, pp. 640–647, 2005.

[41] L. François, B. Iniguez, and O. Moldovan, "A quasi-two-dimensional compact drain-current model fior undoped symmetrci double-gate mosfets including short channel effects," *IEEE Trans. Electron Devices*, vol. 55, no. 6, pp. 1441–1448, 2008.

[42] J.-M. Sallese, F. Krummenacher, F. Pregaldiny, C. Lallement, A. Roy, and C. Enz, "A design oriented charge-based current model for symmetric dg mosfet and its correlation with the ekv formalism," *Solid State Electronics*, vol. 49, no. 12, pp. 485–489, 2004.

[43] P. Francis, A. Terao, D. Flandre, and F. van de Wiele, "Modeling of ultrathin double-gate nmos/soi transistors," *IEEE Trans. Electron Devices*, vol. 41, no. 5, pp. 715–720, 1994.

[44] G. Baccarani and S. Reggiani, "A compact double-gate mosfet model comprising quantum-mechanical and nonstatic effects," *IEEE Trans. Electron Devices*, vol. 46, no. 8, p. 8, 1999.

[45] T. Fjeldly, T. Ytterdal, and M. Shur, *Introduction to Device Modeling and Circuit Simulation.* New York: John Wiley & Sons, 1998.

[46] Q. Chen, E. M. Harrell, and J. Meindl, "A physical short-channel threshold voltage model for undoped symmetric double-gate mosfets," *IEEE Trans. Electron Devices*, vol. 50, no. 7, pp. 1631–1637, 2003.

[47] D. J. Frank, R. H. Dennard, E. Nowak, P. M. Solomon, Y. Taur, and P. Hon-Sum, "Device scaling limits of si mosfets and their application dependencies," *Proceedings of the IEEE*, vol. 89, pp. 259–288, 2001.

[48] X. Liang and Y. Taur, "A 2-d analytical solution for sces in dg mosfets," *IEEE Trans. Electron Devices*, vol. 51, no. 9, pp. 1385–1391, 2004.

[49] D. Munteanu, J. L. Autran, and S. Harrison, "Quantum short-channel compact model for the threshold voltage in double-gate mosfets with high-permittivitty gate dielectrics," *Journal of Non-Crystalline Solids*, vol. 351, no. 21-23, pp. 1911–1918, 2005.

[50] A. Kloes and A. Kostka, "A new analytical method of solving 2d poisson's equation in mos devices applied to threshold voltage and subthreshold modeling," *Solid-State Electronics*, vol. 39, no. 12, pp. 1761 – 1775, 1996.

[51] M. Weidemann, A. Kloes, and B. Iniguez, "Compact model of output conductance in nanoscale bulk mosfet based on 2d analytical calculations," *Solid-State Electronics*, vol. 52, no. 11, pp. 1722 – 1729, 2008.

[52] T. A. Fjeldly, S. Kolberg, and B. Iniguez, "Precise 2-d compact modeling of nanoscale dg mosfets based on conformal mapping techniques," in *Tech. Proc. NSTI-Nanotech.*, vol. 2, 2006, pp. 669–673.

[53] S. Kolberg and T. A. Fjeldly, "2d modelling of nanoscale double gate silicon-on-insulator mosfets using conformal mapping," *Physica Scripta*, vol. T126, pp. 57–60, 2006. [Online]. Available: http://stacks.iop.org/1402-4896/T126/57

[54] M. Schwarz, M. Weidemann, A. Kloes, and B. Iniguez, "2d analytical calculation of the electrostatic potential in lightly doped schottky barrier double-gate mosfet," *Solid State Electronics*, vol. 54, no. 11, 2010.

[55] M. Schwarz, M. Weidemann, A. Kloes, and B. Iniguez, "2d analytical solution of potential in lightly doped schottky barrier double-gate mosfet," in *ESSDERC Fringe 2009, Athens, Greece*, 2009.

[56] M. Schwarz, M. Weidemann, A. Kloes, and B. Iniguez, "Two-dimensional model for the potential profile in a short channel schottky barrier dg-fet," in *ISDRS 2009, Maryland*, 2009.

[57] H.-S. Wong, D. Frank, and P. Solomon, "Device design considerations for double-gate, ground-plane, and single-gated ultra-thin so1 mosfet's at the 25 nm chiannel length generation," *IEDM Tech. Dig.*, vol. 12, pp. 407 – 410, 1998.

[58] K. Keunwoo and J. Fossum, "Double-gate cmos: symmetrical- versus asymmetrical-gate devices," *IEEE Transactions on Electron Devices*, vol. 48, no. 2, pp. 294 – 299, 2001.

[59] T. Tanaka, K. Suzuki, H. Horie, and T. Sugii, "Ultrafast operation of v_{th}-adjusted p^+ - n^+ double-gate soi mosfet's," *IEEE Electron Device Letters*, vol. 15, no. 10, pp. 386 – 388, 1994.

[60] J. Fossum and Y. Chong, "Simulation-based assessment of 50 nm double-gate soi cmos performance," in *MIXDES-16th International Conference Mixed Design of Integrated Circuits & Systems, 2009. MIXDES '09*, 2009, pp. 55 – 60.

[61] Y. Taur, "Analytic solutions of charge and capacitance in symmetric and asymmetric double-gate mosfets," *IEEE Transactions on Electron Devices*, vol. 48, no. 12, pp. 2861 – 2869, 2001.

[62] A. Kammula and B. Minch, "A long-channel model for the asymmetric double-gate mosfet valid in all regions of operation," in *Southwest Symposium on Mixed-Signal Design, 2003*, 2003, pp. 156 – 161.

[63] T. Nakagawa, T. Sekigawa, T. Tsutsumi, M. Hioki, E. Suzuki, and H. Koike, "Improved compact model for four-terminal dg mosfets," in *NSTI-Nanotech 2004*, 2004, pp. 159–162.

[64] T. Nakagawa, T. Sekigawa, T. Tsutsumi, M. Hioki, E. Suzuki, and H. Koike, "Primary consideration on compact modeling of dg mosfets with four-terminal operation mode," *Tech. Digest Nanotech 2003*, vol. 2, pp. 330–333, 2003.

[65] M. Chan, T.-Y. Man, J. He, X. Xi, C.-H. Lin, X. Lin, P. Ko, A. Niknejad, and C. Hu, "Quasi-2d compact modeling for double-gate mosfet," in *NSTI-Nanotech 2004*, vol. 2, 2004, pp. 108–113.

[66] N. Chevillon, F. Mingchun Tang Pregaldiny, C. Lallement, and M. Madec, "Finfet compact modeling and parameter extraction," in *MIXDES-16th International Conference Mixed Design of Integrated Circuits & Systems, 2009. MIXDES '09*, 2009, pp. 55 – 60.

[67] U. Monga, T. Fjeldly, and S. Vishvakarma, "Modeling of quantum mechanical effects in ultra-thin body nanoscale double-gate finfet," in *2nd International Workshop on Electron Devices and Semiconductor Technology, 2009. IEDST '09*, 2009, pp. 1–4.

[68] A. Kloes, M. Weidemann, and B. Iniguez, "Analytical 3d approach for modeling the electrostatic potential in triple-gate soi mosfets," in *EDSSC 2007, Tainan, Taiwan*, 2007.

[69] A. Kloes, M. Weidemann, D. Goebel, and B. T. Bosworth, "Three-dimensional closed-form model for potential barrier in undoped finfets resulting in analytical equations for v_T and subthreshold slope," *IEEE Trans. Electron Devices*, vol. 55, no. 12, pp. 3467–3475, Dec. 2008.

[70] A. Kloes and M. Weidemann, "Compact modeling of nanoscale multiple-gate fets," in *MOS-AK Meeting, MiPlaza, High Tech Campus Eindhoven*, 2008.

[71] A. Kloes, M. Weidemann, and M. Schwarz, "Closed-form current equation for short-channel triple-gate fets," in *MOS-AK Workshop at ESSDERC 2009*, 2009.

[72] A. Kloes, M. Weidemann, and M. Schwarz, "Analytical current equation for short-channel soi multigate fets including 3d effects," *Solid State Electronics*, vol. 54, no. 11, 2010.

[73] B. Ray and S. Mahapatra, "Modeling and analysis of body potential of cylindrical gate-all-around nanowire transistor," *IEEE Transactions on Electron Devices*, vol. 55, no. 9, pp. 2409 – 2416, 2008.

[74] H. Borli, S. Kolberg, and T. Fjeldly, "Physics based current and capacitance model of short-channel double gate and gate-all-around mosfets," in *2nd IEEE International Nanoelectronics Conference, 2008. INEC 2008*, 2008, pp. 493–489.

[75] Weber, *Electromagnetic Fields*, 3rd ed. Wiley, 1950.

[76] D. Crowdy, "The schwarz-christoffel mapping to bounded multiply connected polygonal domains," in *Proceedings of The Royal Society*, 2005, pp. 2653–2678.

[77] Z. Nehari, *Conformal Mapping*. McGraw-Hill, New York, 1952.

[78] A. Kloes, "Analytische modellierung mehrdimensionaler effekte in submikron-mosfet's," Ph.D. dissertation, Technische Hochschule Darmstadt, 1997.

[79] K. Simonyi, *Theoretische Elektrotechnik*. Deutscher Verlag der Wissenschaften, 1976.

[80] K. Binns and P. Lawrenson, *Analysis and Computation of Electric and Magnetic Field Problems*, 2nd ed. Pergamon Press/ New York, 1973.

[81] R. Churchill, *Complex Variables and Applications*, 2nd ed. McGraw-Hill/ New York, 1960.

[82] A. Kloes, *Solid State Semiconductor Electronics Research Advance, chapter 2D compact modeling of semiconductor devices by conformal mapping technique*, S. Kobadze, Ed. Nova Science Publisher Inc., 2009.

[83] B. Riemann, "Inaugural dissertation," Ph.D. dissertation, Goettingen, 1851.

[84] M. Weidemann, M. Jung, and A. Kloes, "Closed-form model of barrier height in bulk mosfet including 2d effects and electron statistics," in *Proc. 8th International Conference on Solid-State and Integrated Circuit Technology ICSICT '06*, 2006, pp. 1278–1280.

[85] A. Kloes and M. Weidemann, "Fem-simulation von nanoscale-mosfets," in *Fachtagung Nanotage 2006*. TUV SUD Akademie GmbH, Muenchen, 2006.

[86] A. Kloes and M. Weidemann, "Analytical modeling of the electrostatic potential in mos devices by conformal mapping," in *MIXDES 2008, Invited paper to special session on compact modeling, Poznan, Polen*, 2008.

[87] A. Kloes and A. Kostka, "Predictmos - a predictive compact model of small-geometry mosfets for circuit simulation and device scaling calculations," *Solid-State Electronics*, vol. 44, no. 7, pp. 1145 – 1156, 2000.

[88] A. Kloes and M. Weidemann, "Self-consistent 2d compact modeling of nanoscale bulk mosfets," *Solid-State Electronics*, vol. 51, no. 5, pp. 739 – 748, 2007. [Online]. Available: http://www.sciencedirect.com/science/article/B6TY5-4NH6CW4-6/2/27ef5c0b214e3ef029ab54fb7ae92898

[89] M. Weidemann, M. Jung, and A. Kloes, "Analytical, physics-based 2d model for the barrier height in nanoscale mosfets valid from sub to above threshold," in *Proceedings IEEE EDS Workshop on Advanced Electron Devices*, 2006.

[90] M. Weidemann, A. Kloes, and B. Iniguez, "Compact model for electric field at pinch-off and channel length shortening in bulk mosfet," in *Proc. IEEE Conference on Electron Devices and Solid-State Circuits EDSSC 2007*, 2007, pp. 1147–1150.

[91] M. Weidemann, A. Kloes, and B. Iniguez, "Physics-based modeling of output conductance in nanoscale bulk mosfet by analytically solving 2d poisson," in *Proc. International Semiconductor Device Research Symposium*, 2007, pp. 1–2.

[92] S. Sze, *Physics of Semiconductor Devices*, 3rd ed. John Wiley & Sons Inc., 2007.

[93] S. Kolberg, "Modeling of electrostatics and drain current in nanoscale double-gate mosfets," Ph.D. dissertation, University Graduate Center at Kjeller Norwegian University of Science and Technology, July 2007.

[94] M. Weidemann, A. Kloes, M. Schwarz, and B. Iniguez, "Two-dimensional analytical model for channel length modulation in lightly-doped dg fets," *Electronics and Telecommunications Quarterly published by Committee of Electronics and Telecommunication of the Polish Academy of Sciences*, vol. 55, no. 4, 2009.

[95] M. Weidemann, A. Kloes, M. Schwarz, and B. Iniguez, "Analysis and modeling of the pinch-off point in a lightly doped asymmetrically biased double gate mosfet," in *ISDRS 2009, University of Maryland*, 2009.

[96] M. Weidemann, M. Schwarz, A. Kloes, and B. Iniguez, "Analytical 2d modelling of channel length modulation in dg fets," in *ESSDERC Fringe 2008*, 2008.

[97] M. Weidemann, A. Kloes, M. Schwarz, and B. Iniguez, "2d physics-based compact model for channel length modulation in lightly doped dg fets," in *MIXDES 2009*, 2009.

[98] V. Reddi and C. Sah, "Source to drain resistance beyond pinch-off in metal-oxide-semiconductor transistors (most)," *IEEE Trans.*, vol. 12, no. 3, pp. 139 – 141, 1965.

[99] D. Frohman-Bentchkowsky and A. Grove, "Conductance of mos transistors in saturation," *IEEE Trans. Electron Devices*, vol. 16, no. 1, pp. 108 – 113, 1969.

[100] F. Jenkins, E. Lane, W. Lattin, and W. Richardson, "Mos-device modeling for computer implementation," *IEEE Trans. Circuit Theory*, vol. 20, no. 6, pp. 649 – 658, 1973.

[101] G. Baum and H. Beneking, "Drift velocity saturation in mos transistors," *IEEE Trans. Electron Devices*, vol. 17, pp. 481–482, 1970.

[102] S. Kolberg and T. A. Fjeldly, "2d modeling of nanoscale double gate soi mosfets using conformal mapping," *Physica Scripta*, vol. T126, pp. 57–60, 2006.

[103] S. Kolberg and T. Fjeldly, "2d modeling of nanoscale dg soi mosfets in and near the subthreshold regime," *Journal Comput Electron*, vol. 5, pp. 217–222, 2006.

[104] A. Kloes, M. Weidemann, D. Goebel, and B. T. Bosworth, "Closed-form physics-based models for threshold voltage and subthreshold slope in finfets including 3d effects," in *Proc. International Semiconductor Device Research Symposium*, 2007, pp. 1–2.

[105] G. Cardano, *chapter 'Vita Ludovici Ferrarii Bononiensi' in Opera Omnia Hieronymi Cardani. cura Caroli Sponii, Lyon, 1663.* Reprinted by Johnson Reprint Corporation, New York, 1967, vol. 10.

[106] M. Weidemann, A. Kloes, M. Schwarz, and B. Iniguez, "2d physics-based compact model of channel length modulation for asymmetrically biased double-gate mosfets," in *ESSDERC Fringe 2009, Athens, Greece*, 2009.

[107] A. Kloes, M. Weidemann, and B. Iniguez, "Analytical 3d approach for modeling the electrostatic potential in triple-gate soi mosfets," in *Proc. IEEE Conference on Electron Devices and Solid-State Circuits EDSSC 2007*, 2007, pp. 103–106.

[108] A. Kloes, M. Weidemann, and M. Schwarz, "Analytical current equation for short channel soi multigate fets including 3d effects," *Solid-State Electronics*, vol. 54, no. 11, pp. 1408–1415, November 2010.

[109] A. Kloes, M. Weidemann, M. Schwarz, and T. Holtij, "Design considerations for undoped finfets based on a 3d compact model for the potential barrier,," in *ULIS 2009, Aachen*, 2009.

[110] A. Kloes, M. Weidemann, and M. Schwarz, "Analysis of 3d current flow in undoped finfets and approaches for compact modeling," in *MIXDES 2009*, 2009.