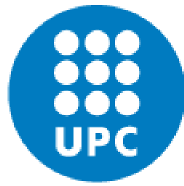

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Design exploration and measurement benchmark of integrated-circuits based on graphene field-effect-transistors : towards wireless nanotransceivers

Mario Enrique Iannazzo Soteras

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N3Cat
Nanonetworking Center
in Catalunya

Design Exploration and Measurement Benchmark of Integrated-Circuits based on Graphene Field-Effect-Transistors: Towards Wireless Nanotransceivers

Thesis submitted in partial fulfilment of the requirement for the PhD Degree issued by the Universitat Politècnica de Catalunya, in its Electronic Engineering Program.

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To my parents and friends, thanks for your endless support and love

To Eva Pradas (1973-2017)

To Eduard and Max, thanks for this unique opportunity

It is perfectly true, as the philosophers say, that life must be understood backwards. But they forget the other proposition, that it must be lived forwards

Søren Kierkegaard

Never let schooling interfere with your education

Grant Allen

English Abstract

This doctoral thesis approaches the design requirements for future high / ultra-high data rate (from 100 Mbps to 100 Gbps) nanotransceivers (nanoTRx) applied to wireless nanonetworks which imply short/ultra-short distance ranges (3 cm – 3 m). It explores graphene field-effect-transistors (GFET), by simulation against measurement benchmarks, as a potential solution for implementing large-signal high-frequency circuits, by virtue of graphene's one-atom thickness and high carrier-mobility extraordinary properties. Finally, the thesis discusses the challenges faced by GFETs, such as zero-bandgap and high metal-graphene contact-resistance, to be able to propose improvements for achieving the initial proposed goals. Chemical-Vapour-Deposition (CVD) GFET fabrication is considered, which is very promising for large-scale manufacturing (CMOS process compatible), and for that fast-computing large-signal compact modeling for complex circuit design is analysed in depth and optimized, and consequently a set of diverse large-signal static and dynamic GFET circuits are simulated and benchmarked against available measurements assessing the accuracy of the proposed models and deriving scaling prospects. An optimization of the current-to-voltage (I-V) characteristic of a GFET compact model, based upon drift-diffusion carrier transport, is presented. The improved accuracy at the Dirac point extends the model usability for GFETs when scaling parameters such as voltage supply (V_{dd}), gate length (L), dielectric thickness (t_{ox}) and carrier mobility (μ) for large-signal design exploration in circuits. The model accuracy is demonstrated through parameters fitting to measurements taken from CVD GFETs fabricated in the University of Siegen and Technical University of Milan. The script has been written in a standard behavioural language (Verilog-A), and extensively run in a commercial analog circuit simulator (Cadence environment) demonstrating its robustness. Besides a simple capacitance-to-voltage model (C-V), a small-signal parasitic capacitance model fitted to dynamic measurements for self-aligned CVD GFETs available in the literature is added, enabling to forecast maximum-frequency-of-oscillation (f_{max}) trends for future scaling. A design-oriented characterization of complementary inverter circuits (INV) based on GFETs is presented as well. Our proposed compact model is benchmarked at the circuit level against another compact model based on a virtual-source approach. Furthermore, a benchmark between simulations and measurements of already fabricated CVD GFET INVs is performed, and performance trends when scaling are derived. The same process is repeated for a more complex circuit, namely GFET ring-oscillators (RO). The transient regime simulations yield performance metrics in terms of oscillation frequency (f_{osc}) and dynamic voltage range (ΔV_{osc}), and consequently, against these metrics, a comprehensive design space exploration covering as input design variables parameters as t_{ox}, L, and V_{dd} is carried out. Being aware of the lack of voltage amplification shown by existing GFETs, the design exploration of a cascode amplifier (CAS) targeted to increase voltage gain (A_v) by decreasing its output conductance (g_o) is presented. GFET CAS are simulated to provide design guidelines, they are accordingly fabricated and consequently measured. Performance metrics are provided in terms of g_o, transconductance (g_m) and hence A_v. Against these metrics, a quantitative comparison between CAS and GFETs is performed and conclusions are derived. Finally, conclusions on GFETs suitability for future nanoTRX are elaborated. The derived publications come

from international collaborations with the Royal Institute of Technology (KTH) in Sweden from 2012 to 2014, and the University of Siegen in Germany from 2014 to 2016.

Resumen en Español

Esta tesis doctoral trata de identificar los requisitos de diseño para nano-transceptores (nanoTRx) para datos de alta velocidad (de 100 Mbps a 100 Gbps) aplicados a nano-redes inalámbricas que implican rangos de alcance cortos u ultra-cortos (3 cm - 3 m). Se exploran transistores de efecto de campo basados en grafeno (GFET), mediante simulaciones y mediciones, como una solución potencial para la implementación de circuitos de alta frecuencia de gran señal, gracias a las extraordinarias propiedades del grafeno como son su espesor de un solo átomo y sus portadores de alta movilidad. Finalmente, se discuten los desafíos a los que se enfrentan los GFETs, como la falta de banda prohibida y la alta resistencia del contacto entre metal y grafeno, para lograr proponer alternativas y poder alcanzar los objetivos iniciales propuestos. Se introducen la técnica CVD como un proceso de fabricación de GFETs a gran escala, compatible con tecnología CMOS. Se introduce el modelado compacto de gran señal y computación veloz para el diseño de circuitos complejos, que es optimizado y analizado en profundidad, y consecuentemente se proponen diversos circuitos de gran señal (estáticos y dinámicos) basados en GFET, que son simulados y comparados con las mediciones disponibles para evaluar la precisión de los modelos propuestos y derivar prospecciones de escalado. Se propone una optimización de la característica corriente-voltaje (I-V) de un modelo compacto GFET basado en el transporte de portadores difusión-deriva. La precisión mejorada en el punto de Dirac extiende la usabilidad del modelo para GFETs cuando se dimensionan parámetros para la exploración en diseños de circuitos de gran señal, tales como el voltaje de alimentación (V_{dd}), la longitud de puerta (L), el espesor dieléctrico (t_{ox}) y la movilidad de portadores (μ). La precisión del modelo se demuestra a través de parámetros que se ajustan a mediciones tomadas a partir de CVD GFETs fabricados en la universidad de Siegen y en la universidad politécnica de Milán. El programa se ha escrito en un lenguaje estándar (Verilog-A) y se ejecuta extensivamente en un simulador de circuitos analógico comercial (entorno Cadence) donde se demuestra su robustez. Además, se lleva a cabo la parametrización de un modelo capacidad-voltaje (C-V) añadiendo un modelo de capacidades parásitas de pequeña señal que son ajustados a las mediciones de alta frecuencia de CVD GFETs disponibles en la literatura científica, lo que permite la predicción de la frecuencia máxima de oscilación (f_{max}) para el escalado de futuros GFETs. También se presenta una caracterización orientada al diseño de circuitos inversores (INV) basados en GFETs. Nuestro modelo compacto propuesto se compara a nivel de circuito con otro modelo compacto basado en un enfoque diferente (fuente-virtual). A continuación, se lleva a cabo una comparación a nivel de circuito entre las simulaciones y las medidas de INVs ya fabricados basados en CVD GFET, y se obtienen las tendencias de comportamiento al escalarlos. Se repite el mismo proceso para un circuito más complejo, los llamados osciladores-en-anillo GFET (RO). Las simulaciones basadas en transitorios producen métricas de rendimiento en términos de frecuencia de oscilación (f_{OSC}) y rango dinámico de voltaje (ΔV_{OSC}), por lo tanto, contra estas métricas, se lleva a cabo una exploración exhaustiva de diseño que abarca parámetros de variables de diseño como t_{OX}, L y V_{dd}. Al ser conscientes de la falta de amplificación de voltaje mostrada por los GFETs existentes, se presenta la exploración del espacio de diseño de un amplificador cascodo (CAS) diseñado para incrementar la amplificación de voltaje (A_v) disminuyendo su

conductancia de salida (g_o). Los GFET CAS son simulados para proporcionar guías de diseño, luego fabricados y finalmente medidos. Se proporcionan métricas de rendimiento en términos de g_o, transconductancia (g_m), y consecuentemente Av. Frente a estas métricas, se realiza una comparación cuantitativa entre CAS y GFETs y se derivan las conclusiones. Finalmente, se elaboran las conclusiones sobre la idoneidad de los GFET para futuros nanoTRx. Las publicaciones derivadas provienen de colaboraciones internacionales con el Instituto Real de Tecnología (KTH) en Suecia de 2012 a 2014, y la Universidad de Siegen en Alemania de 2014 a 2016.

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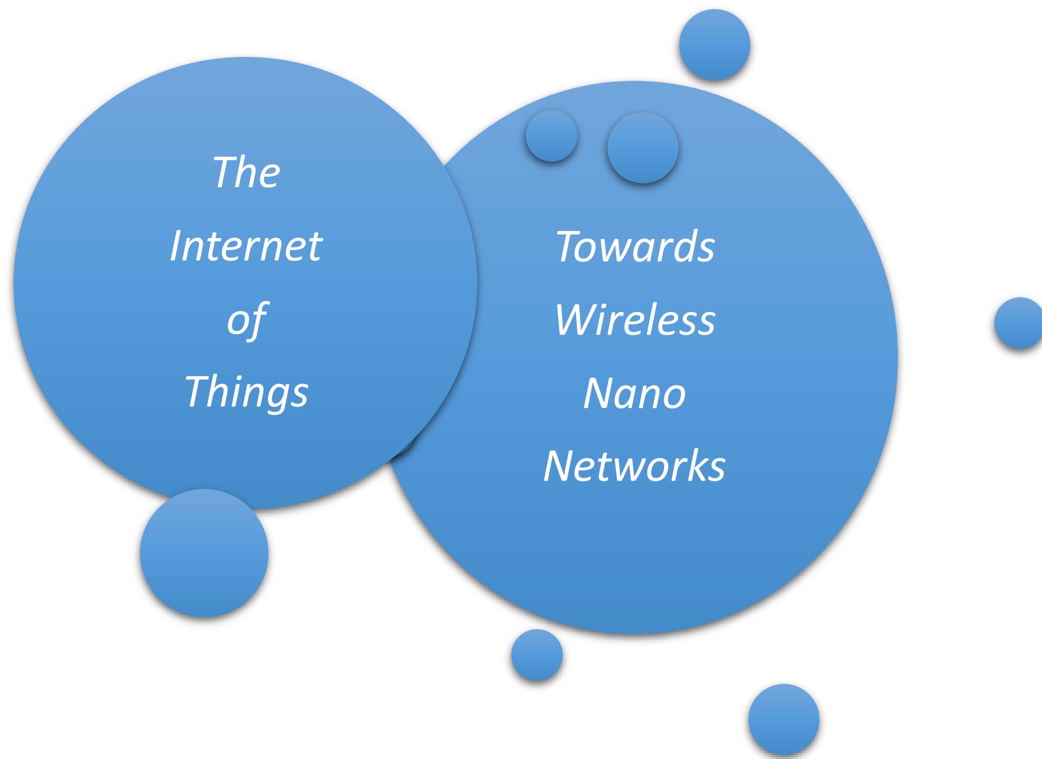
1 Nanonetworks



Information and communication technology achieved its major breakthrough in human history with the foundation of telecommunications in the 19th century, although the invention of electronics in the 20th century was the key enabler for transforming our past industrial society, mainly sustained by manufactured goods, to our present information society, mainly sustained on services. In the short run, our future as humans lies on building up a knowledge society [1] where raw information is transformed into usable knowledge for improving and creating more valuable services, and in the long run, humanity might foresee a rather utopian wisdom society where the existing and newly generated wisdom is applied and equally distributed between all members of society. Without any kind of doubts the future of our civilization will be a more interconnected one, with ever increasing person-to-person, person-to-machine/machine-to-person and machine-to-machine (M2M) connections through ubiquitous networks. To make this vision a reality, M2M communication modules cost, size, and power consumption need to be reduced further more than actual technologies allow. Nanotechnology, first envisioned by Richard Feynman in 1959 [2], is giving rise to devices and systems in a scale ranging from one to a few hundred nanometers, and will be fundamental in overcoming the future challenges. This thesis is trying to interconnect and shed a bit of light on two rather new and disrupting nanotechnology disciplines that have gained momentum among the researchers during the last decade: two-dimensional materials [3] and nanonetworks [4]. This chapter briefly introduces a few concepts on networking as wireless sensor networks (WSN) that are just starting to be deployed, and wireless nanonetworks (WNN) that could become the main objective for the research work presented through the following chapters.

1.1 The Internet of Things

The human population estimations for 2017 are around 7.5 billion. Figure 1.1a is showing that by 2020 there will be 1.5 mobile devices per capita which will translate into 11.6 billion mobile devices including phones, M2M modules, tablets and others [5]. These devices will be connected through computer networks with different distance-ranges and data-rates depending on their target-applications: mobile networks like for example 4G, 5G; wireless local-area-networks (WLAN) like for example WiFi; wireless personal-area-networks (WPAN) like for example Bluetooth, Zigbee and Ultra-Wide-Band; wireless body-area-networks (WBAN) like for example the IEEE 802.15.6 standard; low-power wide-area-networks (LPWAN), and new types of networks to be developed in the near future.

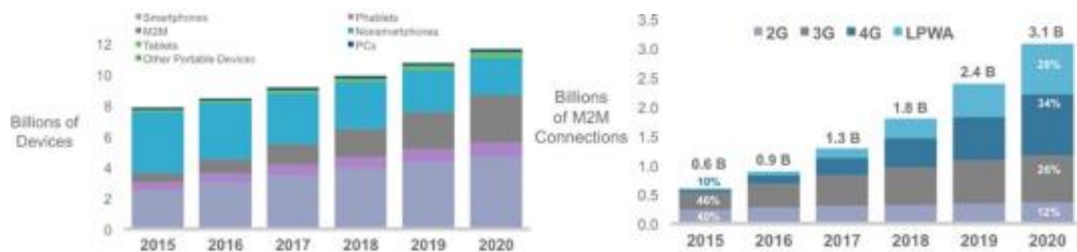


Figure 1.1 (a) Global mobile devices and connections growth. (b) Global machine-to-machine growth and migration from 2G to 3G and 4G [5].

As seen in Figure 1.1b, the number of M2M modules are expected to grow five-fold in only 5 years, reaching 3.1 billion connections. In a few years, the amount of M2M modules will surpass all the mobile phones around the planet. Low-power wide-area will be the second most common M2M connection by 2020 [5]. M2Ms modules are the core of the internet of things IoT, defined as the worldwide network of interconnected machines uniquely addressable based on standard communication protocols. The applications are endless: home automation, smart metering and maintenance, assisted driving, logistics tracking, environment monitoring, healthcare bio-sensing, and many more [6]. From all plethora of existing wireless networks, this thesis will focus on high-speed short-range networks.

1.1.1 Wireless Sensor Network

WSN consist of hundreds of interconnected sensor-modules that are able to retrieve and process information while consuming low power, such networks are already starting to gain relevance on the complex IoT ecosystem [7]. An example of WSN based applications are the indoor-location solutions provided by Decawave Inc., a small start-up company where the author had the opportunity to work with. A low-rate WPAN LR-WPAN, fully IEEE 802.15.4-2011 compliant, is implemented to locate tags with unprecedented resolutions under 10 cm, this new application is already revolutionizing the logistics sector [8]. The communication module, i.e. transceiver (TRx) + antenna, is a low-power innovative impulse-radio/ultra-wide-band (IR/UWB) solution and the

achieved specifications are shown in Table 1.1 to pinpoint the state-of-the-art (SoA) and to compare with the module specifications for WNNs introduced in next section 1.2.

Distance Range (m)	Data Rate (Mbps)	Power Consumption (mW)	Energy Efficiency (nJ/bit)	Module Size (mm^2)
50 - 200	0.11 - 6.8	115.5 - 415.8	61.15 – 1005	36[a] – 299[b]

Table 1.1 Communication module specifications for a wireless sensor network. Energy efficiency = Power consumption / Data rate. [a] Integrated circuit (IC), [b] Printed circuit board (PCB).

Shrinking further the footprint of these tags would be beneficious for improving the location accuracy, increasing the data rate, reducing the power consumption and bringing down fabrication costs. As seen in Figure 1.2, the biggest component of the tag is the external dielectric-chip antenna radiating at the 3.5 - 6.5 GHz frequency range. Reducing the antenna size will force the TRx to work at higher frequencies and to make this happen transistors need to operate faster. With existing complementary-metal-oxide-silicon (CMOS) technologies, the straightforward way to achieve higher operation frequencies is reducing the gate length L, that implies jumping from 90 nm node to smaller ones (65 nm, 45 nm, 32 nm, 22 nm, 14 nm or 10 nm). The challenge ahead is that the physical limit for device scaling is already approaching: shrinking metal-oxide-silicon field-effect-transistors (MOSFET) gates below 3 nm theoretically (5 nm practically) will not be possible due to direct-tunnelling current appearing between drain and source [9], therefore new disruptive technologies are a must to overcome silicon limitations in nanoelectronics.

Figure 1.2 An indoor-location tag: DWM1000 module is based on a 90 nm CMOS IC TRx, integrated with a dielectric-chip antenna, DC/DC converter and xOSC on-board. Edited figure from [10].

1.2 Towards Wireless Nanonetworks

A WNN, defined as an interconnection of nanomachines, are expected to expand the capabilities of single nanomachines by allowing them to cooperate and share information. A nanomachine is a device consisting of nanoscale components able to perform a specific task at nanolevel, such as communicating, computing, data storing, and sensing. The tasks performed by one nanomachine are very simple and restricted to its close environment due to its low complexity and small size. A nanomachines (Figure 1.3) consists of the following modules shown below: Nanotransceiver (nanoTRx) [11], Nanoprocessor [12], Nanomemory [13], Nanosensor [14] / Nanoactuator [15], and Nanobattery [16] / Nanoharvester [17]. Many breakthroughs in several branches of science (chemistry, physics, mechanics, electronics, telecommunications and computing) will be needed to make this vision reality in the long run. Examples of potential applications are: intra human-body monitoring, biodiversity control, biodegradation assistance, harmful chemicals monitoring, biological weapons monitoring, on chip networking, home/office organization, and many more [4].

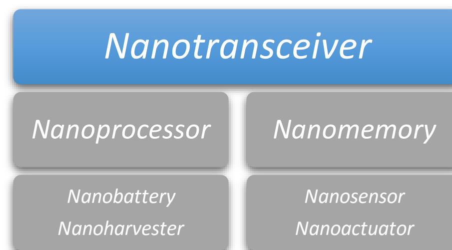


Figure 1.3 Nanomachine modules. First prototypes are envisioned beyond 2030. The scope of this thesis is the nanoTRx module.

In the next sections, three different types of WNNs are presented: wireless nanomedia network (WnMN) targeted to multimedia applications, wireless nanosensor network (WnSN) targeted to ubiquitous-sensing applications, and wireless network-on-chip (WNoC) targeted to parallel-computing applications.

1.2.1 Wireless Nanomedia/Nanosensor Network

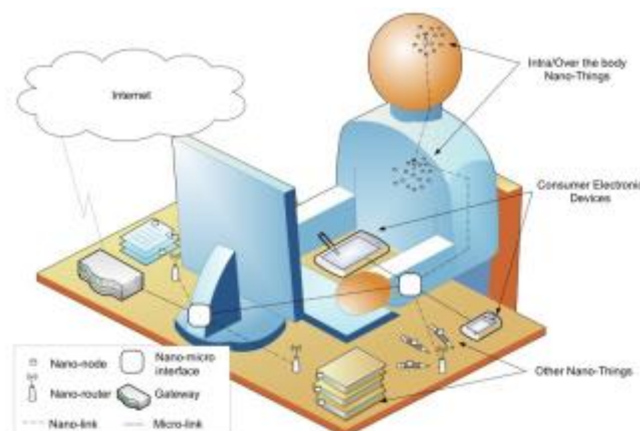


Figure 1.4 Wireless nanomedia / nanosensor networks [18].

In Figure 1.4, an example of WnMN and WnSN are depicted. For WnMN, small office-utensils (pencils, papers, books) are able to communicate multimedia data between them. For WnSN, fixed nanomachines over the body are able to communicate health-monitoring data between them or even mobile nanomachines inside the body are able to measure low chemical concentrations and drugs are delivered locally if needed. The design specifications of the communication module are shown below:

	Distance Range (cm)	Data Rate (Gbps)	Power Consumption (mW)	Energy Efficiency (pJ/bit)	Module Size (mm^2)
WnMN	30 - 300	1 - 10	10 – 100	10	10 - 100
WnSN	10 - 30	0.1 - 1	1 – 10	10	1 - 10

Table 1.2 Wireless nanomedia/nanosensor networks communication module specifications.

1.2.2 Wireless Network on Chip

A network-on-chip (NoC) consists in a mesh of wireline-routed interconnections and has been proposed as a solution to the very-limited scalability of the buses used in multi-core processors. However, as the number of cores per chip increases, traditional NoCs suffer from fundamental issues that will render them impractical in future multi-processors. The concept of WNoC (Figure 1.5) is proposed to reduce communication latency and power consumption, by reducing the number of hops between any pair of cores, thanks to the implementation of broadcast and multicast data-traffic through antennas integrated on the same die [19].

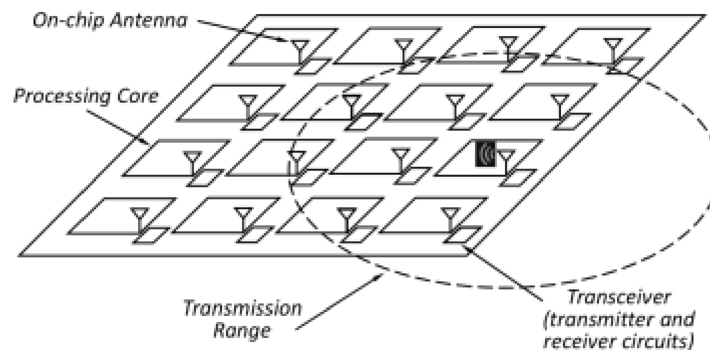


Figure 1.5 Wireless network-on-chip schematic [20].

The targeted communication module specifications for WNoCs are shown below:

Distance Range (cm)	Data Rate (Gbps)	Power Consumption (mW)	Energy Efficiency (pJ/bit)	Module Size (mm^2)
3 - 10	10 – 100	1 – 10	0.1	0.1 - 1

Table 1.3 Wireless network-on-chip communication module specifications.

1.3 Conclusions

In Figure 1.6, a power consumption against data rate graph is shown [21]. The four types of wireless networks (UWB, WnMN, WnSN, and WNoC) already presented are pinpointed and compared to other types of networks (WLAN, 5G, Bluetooth and Zigbee). WLAN and 5G are considered ‘high-power’ wireless networks; and Bluetooth, Zigbee and UWB are considered ´long-distance´ wireless networks, therefore both types are discarded as targeted applications for this thesis. Our aim is paving the way for new networks concepts as WnMN, WnSN, and WNoC.

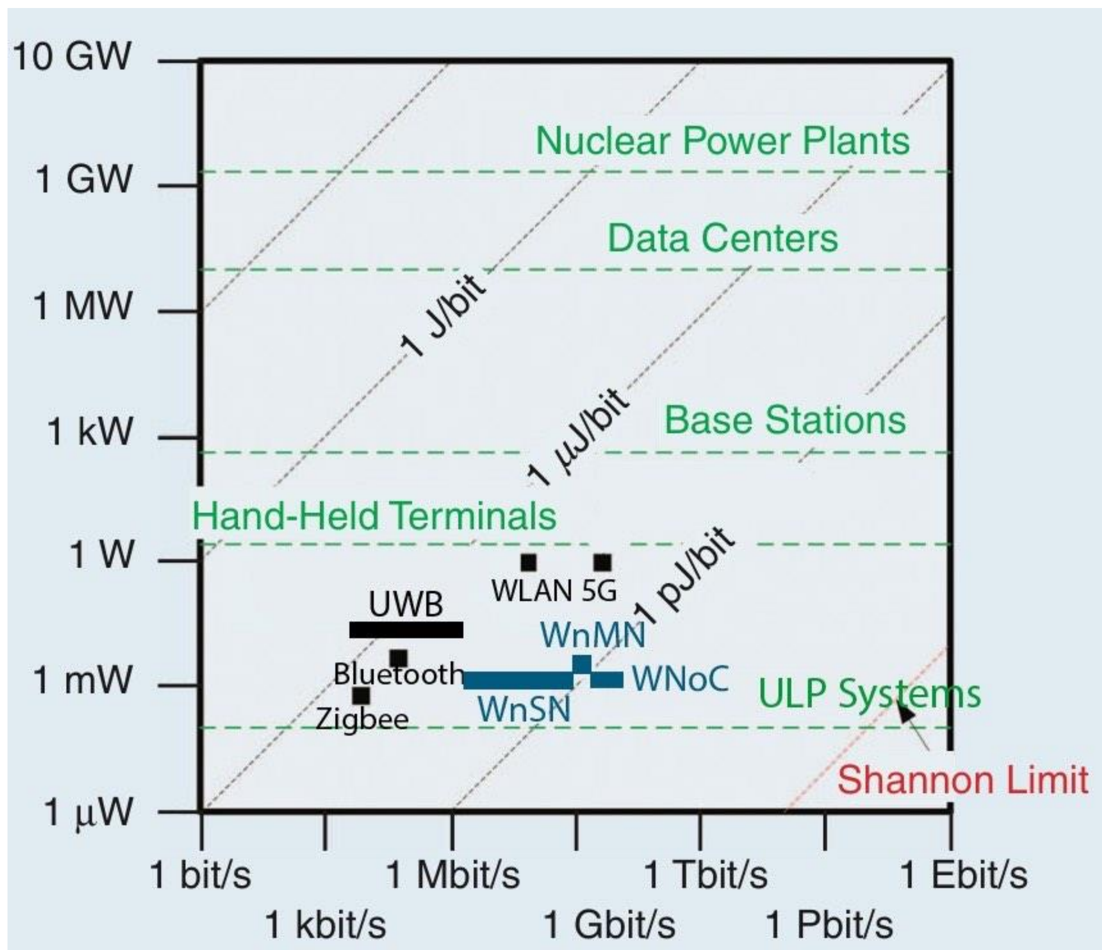


Figure 1.6 Power consumption versus data rate for the communication module of different wireless networks. The blue boxes are the targeted requirements. Edited figure from [21]

.

UWB is consuming more power than Bluetooth because is a wideband (500 MHz) network that delivers more data rate and also needs longer ranges to locate tags in large indoor buildings (like for example in warehouses). Our particular interpretation of WnSN is consuming less power than Bluetooth and its data rates are similar to WLAN. WNoC is consuming more power than Zigbee and it is offering faster data rates than 5G. WnMN are consuming the same power as Bluetooth but the offered data rates are a bit less

than 5G. Below a final summary of all the networks regarding their distance range and data rate is presented to highlight the characteristics of the targeted new WNNs:

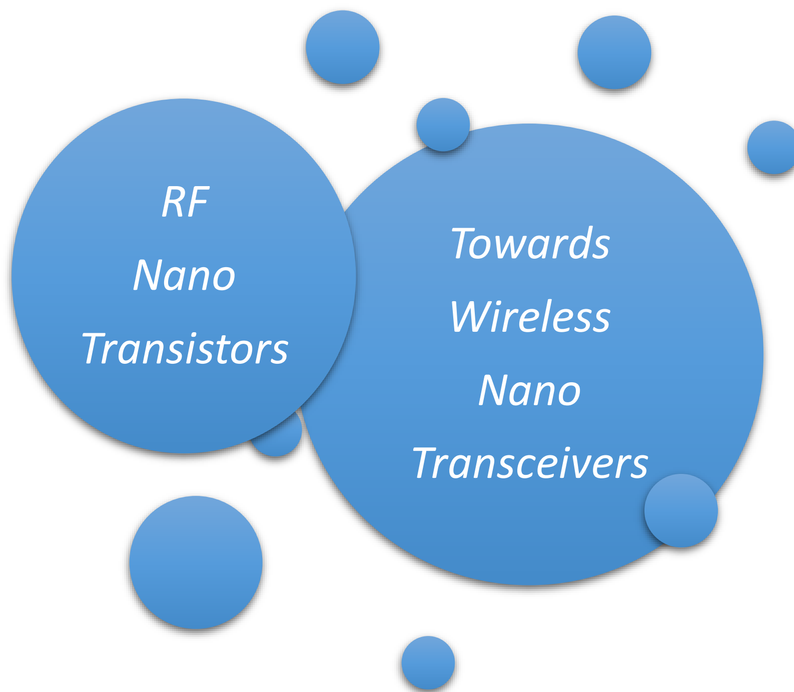
	5G	WLAN	UWB	Bluetooth	Zigbee
Distance Range	Very Long	Long	Long	Short	Short
Data Rate	Ultra High	High	Very Low /Low	Low	Very Low

	WnMN	WnSN	WNoC
Distance Range	Very Short	Very Short	Ultra Short
Data Rate	Very High	High	Ultra High

Table 1.4 Wireless networks vs communication module´s data rate and distance range. The targeted wireless networks for this thesis are highlighted in green colour.

Future high/ultra-high data rate TRx applied to WNN which imply short/ultra-short distance ranges (3 – 300 cm) requirements have been detected. WNN need smaller (0.1 - 100 mm^2), faster (0.1 - 100 Gbps), more energy efficient (0.1 – 10 pJ/bit) and less power hungry (1 - 100 mW) TRx than classical wireless networks to become a reality. We are talking about 2 - 3 orders of magnitude reduction in size, data rate and power consumption which is **not** possible with commercial technologies available at the present. This enormous challenge will be discussed in detail in chapter 2 and new proposals will be introduced.

2 Nanotransceivers



Analysing the requirements for our targeted WNN applications, it becomes clear that faster and more energy efficient TRx will be needed to implement the communication modules, consequently miniaturisation at device level and architecture level is a must to target future wireless nanoTRx introduced in section 2.1. In section 2.2, the SoA of radio-frequency (RF) nanotransistors is analysed; once it is shown that with existing transistors is extremely challenging if not impossible to design the architectures required, recently discovered two-dimensional (2D) materials are proposed as channels for future nanotransistors. Chapter 3 will focus on Graphene [22] which is exhibiting extraordinary carrier-mobilities and could fulfil the speed demands for future front-end (FE) nanocircuits.

2.1 Towards Wireless Nanotransceivers

A wireless nanoTRx is defined as an ultra-small communication module targeted to WNN, which it is fully integrated on a common insulator substrate consisting of five modules: analog FE, digital back-end (BE), antenna, energy management, and crystal oscillator schematized in Figure 2.1. What marks out a nanoTRx from a classical communication module is: (1) the small size which lies in the range from 0.1 mm^2 to 100 mm^2 which requires a high level of compatibility between the technology used by the different modules to integrate all of them on the same die; (2) the low power consumption which lies in the range from 1 mW to 100 mW due to the tiny amount of energy available for them; and (3) the short access distance which lies in the range from 3 cm to 3 m constrained by their size and power limitations. Both transmitter (Tx) and

receiver (Rx) are divided into a FE implemented with RF circuits and a BE implemented with digital circuits. The antenna is the transductor that is adapting the metal-guided RF signals of the Tx to the shared medium (air), and from the air to the Rx. The function of a Rx is to amplify and filter the ultra-low RF signals sensed by the antenna that arrive from the air, also it is able to discern between the targeted signal and the discarded noise/interference signals. The Tx amplifies and filters the RF signal to power levels that are enough to overcome attenuation/noise/interferences which may arise on the air during the communication. The xOSC is needed for generating a stable and accurate clock reference. The analog power module efficiently provides clean direct-current (DC) supply-voltage for both FE and BE modules.

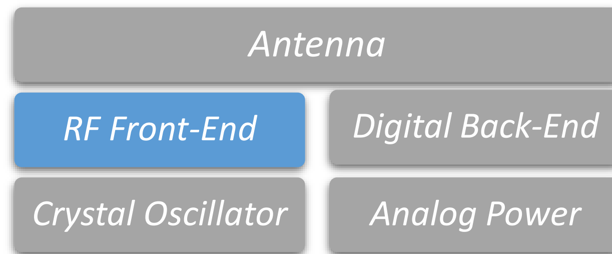


Figure 2.1 Diagram of the nanoTRx modules integrated on a common substrate. The target of this thesis is the RF FE.

In the following section, the SoA wireless TRx for high-speed at short-range communication is reviewed and analysed. Once it is shown that with existing TRx architectures is extremely challenging if not impossible to comply with the specifications defined for the targeted WNN, a potential solution is proposed based on the combination of two arising wireless communication technologies: terahertz (THz) [23] and IR/UWB technologies [24], which will imply a change of paradigm for future nanotransistors technology as explained in section 2.2.

2.1.1 High Data Rate Transceivers for Short Distance Ranges

A wide variety of wireless TRx solutions can be found in the literature covering many alternatives in terms of technology, modulation, or architecture. For transmission ranges of up to a few meters, these provide multi-gigabit data rates, and it is expected that these figures will keep increasing as technology evolves **(Conference C)**. In Table 2.2 and Table 2.3, the most relevant high-speed and short-range TRx are presented. They are classified in 3 groups depending on their frequency-band operation: super high-frequency SHF (1 cm < λ[1] < 10 cm), extremely high-frequency EHF (1 mm < λ < 10 mm), and tremendously high-frequency THF (100 μm < λ < 1000 μm). The following TRx characteristics are defined: frequency band, center frequency (f_C) in GHz, chip partitioning, transistor technology, digital modulation, power consumption (mW), data rate (Gbit/s), energy efficiency = power consumption / data rate (pJ/bit), distance range (cm), FOM_{com} = energy efficiency / distance range (pJ/bit.$\sqrt{}$cm) introduced by [25],

[1] Electromagnetic Wavelength

integration level, module size (mm^2), antenna type, n (bit-error-ratio BER = 10^{-n}) and maturity factor = (data rate / center frequency) x 100 (%). A new figure of merit is introduced: The maturity factor (MF), not to be confused with the concept of spectral efficiency = data rate / bandwidth (BW), tries to evaluate the efficiency of implementing a given modulation and BW in order to yield a target data rate operating at a target frequency band. As technology matures, highly optimized TRx are expected leading to increasing MFs, that is, higher data rates for similar area and energy values **(Journal III)**. The maximum MF value observed is 26.3 % at 190 GHz [26] which is really an outstanding value for electronics at such high frequencies considering that the average for all shown TRx is 12.9 %. The MF can be interpreted as a 'digitalization' of the fractional BW concept for antennas (FB = BW / f_C), where data rate is used instead of BW to include the impact of digital modulation. While the frequency-band operation is increased, the antenna size becomes smaller which is beneficious for integrating them on chip. We can classify antennas in four different types from bigger to smaller sizes: external (red), on-board (yellow), on-package (blue) and on-chip (green). As it can be noticed, from 8 GHz to 135 GHz is not possible to integrate antennas on-chip due to their excessive dimensions. The aim in this thesis is to target on-chip antennas that is why it is **so important** to build nanoTRx beyond 200 GHz bands. The highest frequency band achieved by a digital TRx is 400 GHz, and this is happening thanks to the improved carrier mobility offered by SiGe heterojunction-bipolar-transistors (HBT) compared to CMOS FETs [27]. The highest integration is achieved at 8 GHz, where RF FE and digital BE are integrated on the same 90 nm CMOS process [28]. The ultimate goal of our vision is to achieve similar level of integration at hundreds of GHz with a common process (including different kinds of devices with specific functionalities), this is **not** possible with existing technologies. The lowest power consumption 13.3 mW and longest distance range 1.2 m is achieved at 8 GHz [29], this is achievable due to the use of the most simple digital modulation on-off-keying *OOK*; this case seems suitable for WnSN specifications, nevertheless the main problem is that the antenna is not integrated, so it is not feasible to keep the module size under 100 mm^2. The highest data rate 50 Gbps is achieved at 190 GHz [26], which seems suitable for WNoC although power consumption is exceeding the 10 mW limit by far. The lowest energy efficiency 5.3 pJ/bit is also achieved at 190 GHz [26] and the lowest FOM_{com} 1.98 pJ/bit is achieved at 60 GHz [30], the first TRx seems suitable for WnMN, but its short distance range fall behind the minimum 10 cm required; and the second TRx seems suitable for WnSN, nevertheless its distance range also fall behind the minimum 30 cm required. The smallest module-size achieved is 0.31 mm^2 at 142 GHz [31], which seems appropriated for WNoCs, although the drawback is the used technology (BiCMOS) which does not scale properly for integrating the massive number of gates required to fabricate nanoprocessors. The lowest BER 10^{-12} is achieved at 210 GHz [32], which seems adequate for WNoC that needs very reliable transmission to be competitive against wired connections, but the problem is the power consumption that is well above the 10 mW allowed limit.

For these reasons, it becomes clear that to comply with **all** the specifications at the **same** time for each one of our targeted WNNs is not possible with the available technology, new semiconductor processes and architectures need to be developed for the long run. As a summary, the suitability of actual TRx to specified WNN is shown in Table 2.1. The most demanding specifications come clearly from WNoCs, and in terms of requirements lowering power-consumption is the most pressing challenge.

	Maximum Distance (mm)	*Data Rate (Gbps)*	*Power Consumption (mW)*	*Energy Efficiency (pJ/bit)*	*Module Size (mm^2)*
SoA TRx	*0.6 – 1200*	*0.5 - 50*	*13.3 - 1900*	*5.3 – 117.3*	*0.31 - 26.64*
WnMN					
WnSN					
WNoC					

Table 2.1 WNN feasibility vs high-speed short-range wireless TRx specifications. Green colour stands for 'partially achievable', yellow colour for 'very challenging' and red colour for ´not possible'.

<table>
<tr><th></th><th>Geng et al. [29]</th><th>Abe et al. [28]</th><th>Chen et al. [33]</th><th colspan="2">Kawasaki et al. [34]</th><th colspan="2">Okada et al. [35]</th><th>Byeon et al. [30]</th><th colspan="2">Pang et al. [36]</th><th colspan="2">Lee et al. [37]</th></tr>
<tr><td>Year</td><td>2015</td><td>2012</td><td>2009</td><td colspan="2">2010</td><td colspan="2">2013</td><td>2016</td><td colspan="2">2017</td><td colspan="2">2015</td></tr>
<tr><td>Frequency Band</td><td>SHF</td><td>SHF</td><td>EHF</td><td colspan="2">EHF</td><td colspan="2">EHF</td><td>EHF</td><td colspan="2">EHF</td><td colspan="2">EHF</td></tr>
<tr><td>Center Frequency (GHz)</td><td>8</td><td>8</td><td>43</td><td colspan="2">56jj</td><td colspan="2">60</td><td>60</td><td colspan="2">60</td><td colspan="2">80</td></tr>
<tr><td>Chip Partitioning</td><td>Front-End</td><td>Front-End + Back-End</td><td>Front-End</td><td colspan="2">Front-End</td><td>Front-End</td><td>Back-End</td><td>Front-End</td><td colspan="2">Front-End</td><td colspan="2">Front-End</td></tr>
<tr><td>Transistor Technology</td><td>65 nm CMOS</td><td>90 nm CMOS</td><td>180 nm SiGe BiCMOS</td><td colspan="2">40 nm CMOS</td><td>65 nm CMOS</td><td>40 nm CMOS</td><td>90 nm CMOS</td><td colspan="2">65 nm CMOS</td><td colspan="2">65 nm CMOS</td></tr>
<tr><td>Digital Modulation</td><td>OOK</td><td>BPSK</td><td>ASK</td><td colspan="2">ASK</td><td colspan="2">16 QAM</td><td>OOK</td><td colspan="2">128 QAM</td><td colspan="2">OOK</td></tr>
<tr><td rowspan="2">Power Consumption (mW)</td><td rowspan="2">13.3</td><td rowspan="2">150</td><td rowspan="2">117</td><td>29</td><td>41</td><td>271</td><td>311.5</td><td rowspan="2">67</td><td>169</td><td>139</td><td>18</td><td>46</td></tr>
<tr><td colspan="2">70</td><td colspan="2">582.5</td><td colspan="2">308</td><td colspan="2">64</td></tr>
<tr><td>Data Rate (Gbit/s)</td><td>0.5</td><td>2</td><td>6</td><td colspan="2">11</td><td colspan="2">6.3</td><td>10.7</td><td colspan="2">12.32</td><td colspan="2">12</td></tr>
<tr><td rowspan="2">Energy Efficiency (pJ/bit)</td><td rowspan="2">26</td><td rowspan="2">75</td><td rowspan="2">19.5</td><td>2.64</td><td>3.73</td><td>43.02</td><td>49.4</td><td rowspan="2">6.26</td><td>13.7</td><td>11.28</td><td>1.5</td><td>3.83</td></tr>
<tr><td colspan="2">6.37</td><td colspan="2">92.42</td><td colspan="2">24.98</td><td colspan="2">5.33</td></tr>
<tr><td>Distance Range (cm)</td><td>120</td><td>3.4</td><td>2</td><td colspan="2">1.4</td><td colspan="2">50</td><td>10</td><td colspan="2">30</td><td colspan="2">1.2</td></tr>
<tr><td rowspan="2">FOM_{com} (pJ/bit.vcm)</td><td rowspan="2">2.37</td><td rowspan="2">40.67</td><td rowspan="2">13.79</td><td rowspan="2" colspan="2">5.41</td><td>6.08</td><td>6.99</td><td rowspan="2">1.98</td><td>2.5</td><td>2.06</td><td>1.37</td><td>3.5</td></tr>
<tr><td colspan="2">13.07</td><td colspan="2">4.56</td><td colspan="2">4.87</td></tr>
<tr><td>Integration Level</td><td>Tx+DCO+Rx+PR</td><td>Tx+Rx+PLLs+ Analog+Digital +PR</td><td>Rx+Tx</td><td>Tx+VCO+ PR</td><td>Rx+VCO+ PR</td><td>Rx+Tx+ PLL+PR</td><td>Analog+ Digital+ PLL+PR</td><td>Rx+Tx+ VCO+PR</td><td colspan="2">Rx+Tx+ PLL+PR</td><td>Tx+ VCO+PR</td><td>Rx+PR</td></tr>
<tr><td rowspan="2">Module Size (mm^2)</td><td rowspan="2">2.25</td><td rowspan="2">5.6</td><td rowspan="2">0.62</td><td>0.54</td><td>0.54</td><td>17.64</td><td>9</td><td rowspan="2">1.92</td><td rowspan="2" colspan="2">6</td><td>0.5</td><td>0.84</td></tr>
<tr><td colspan="2">1.08</td><td colspan="2">26.64</td><td colspan="2">1.34</td></tr>
<tr><td>Antenna Type</td><td>External</td><td>External</td><td>In-Package Bonding-Wire</td><td colspan="2">In-Package Bonding-Wire</td><td colspan="2">In-Package Slab-Waveguide</td><td>On-Board Yagi-Uda</td><td colspan="2">External Horn</td><td colspan="2">On-Board</td></tr>
<tr><td>n ($BER=10^{-n}$)</td><td>3</td><td>3</td><td>8</td><td colspan="2">11</td><td colspan="2">4</td><td>12</td><td colspan="2">3</td><td colspan="2">12</td></tr>
<tr><td>Maturity Factor (%)</td><td>6.2</td><td>25</td><td>13.9</td><td colspan="2">19.6</td><td colspan="2">10.5</td><td>17.8</td><td colspan="2">20.5</td><td colspan="2">15</td></tr>
</table>

Table 2.2 SHF and EHF high-speed short-range wireless TRx. Green colour = Antenna integrated on-chip. Blue colour = Antenna integrated in-package. Yellow colour = Antenna integrated on-board. Red color = External antenna. PR = Pad Ring.

<table>
<tr><th></th><th colspan="2">Fujishima et al.
[38]</th><th colspan="2">Foulon et al.
[31]</th><th colspan="2">Fritsche et al.
[26]</th><th colspan="2">Moghadami et al.
[32]</th><th colspan="2">Sarmah et al.
[39]</th><th colspan="2">Park et al.
[40]</th><th colspan="2">Hu et al.
[27]</th></tr>
<tr><td>Year</td><td colspan="2">2013</td><td colspan="2">2014</td><td colspan="2">2017</td><td colspan="2">2015</td><td colspan="2">2016</td><td colspan="2">2012</td><td colspan="2">2012</td></tr>
<tr><td>Band Frequency</td><td colspan="2">EHF</td><td colspan="2">EHF</td><td colspan="2">EHF</td><td colspan="2">EHF</td><td colspan="2">EHF</td><td colspan="2">EHF</td><td colspan="2">THF</td></tr>
<tr><td>Center Frequency (GHz)</td><td colspan="2">135</td><td colspan="2">140</td><td colspan="2">190</td><td colspan="2">210</td><td colspan="2">240</td><td colspan="2">260</td><td colspan="2">400</td></tr>
<tr><td>Chip Partitioning</td><td colspan="2">Front-End</td><td colspan="2">Front-End</td><td colspan="2">Front-End</td><td colspan="2">Front-End</td><td colspan="2">Front-End</td><td colspan="2">Front-End</td><td colspan="2">Front-End</td></tr>
<tr><td>Transistor Technology</td><td colspan="2">40 nm
CMOS</td><td colspan="2">130 nm SiGe BiCMOS</td><td colspan="2">130 nm SiGe BiCMOS</td><td colspan="2">40 nm CMOS</td><td colspan="2">130 nm SiGe BiCMOS</td><td colspan="2">65 nm
CMOS</td><td colspan="2">130 nm SiGe BiCMOS</td></tr>
<tr><td>Digital Modulation</td><td colspan="2">ASK</td><td colspan="2">QPSK</td><td colspan="2">BPSK</td><td colspan="2">OOK</td><td colspan="2">QAM</td><td colspan="2">OOK</td><td colspan="2">ASK</td></tr>
<tr><td rowspan="2">Power Consumption (mW)</td><td>17.9</td><td>80.5</td><td>66</td><td>14</td><td>32</td><td>122</td><td colspan="2" rowspan="2">421</td><td>1033</td><td>866</td><td colspan="2" rowspan="2">1173</td><td>117.9</td><td>~0</td></tr>
<tr><td colspan="2">98.4</td><td colspan="2">80</td><td colspan="2">154</td><td colspan="2">1899</td><td colspan="2">117.9</td></tr>
<tr><td>Data Rate (Gbit/s)</td><td colspan="2">10</td><td colspan="2">10</td><td colspan="2">50</td><td colspan="2">10.7</td><td colspan="2">23.2</td><td colspan="2">10</td><td colspan="2">10</td></tr>
<tr><td rowspan="2">Energy Efficiency (pJ/bit)</td><td>1.8</td><td>8</td><td>6.6</td><td>1.4</td><td>3.1</td><td>2.2</td><td colspan="2" rowspan="2">39.3</td><td>44.5</td><td>37.33</td><td colspan="2" rowspan="2">117.3</td><td>11.79</td><td>~0</td></tr>
<tr><td colspan="2">9.8</td><td colspan="2">8</td><td colspan="2">5.3</td><td colspan="2">81.83</td><td colspan="2">11.79</td></tr>
<tr><td>Distance Range (cm)</td><td colspan="2">10</td><td colspan="2">0.06</td><td colspan="2">0.6</td><td colspan="2">1</td><td colspan="2">15</td><td colspan="2">4</td><td colspan="2">6</td></tr>
<tr><td rowspan="2">FOM_{com} (pJ/bit.vcm)</td><td>0.57</td><td>2.53</td><td>26.94</td><td>5.72</td><td>4</td><td>2.84</td><td colspan="2" rowspan="2">39.3</td><td>11.49</td><td>9.64</td><td colspan="2" rowspan="2">58.65</td><td>4.81</td><td>~0</td></tr>
<tr><td colspan="2">3.1</td><td colspan="2">32.66</td><td colspan="2">6.84</td><td colspan="2">21.28</td><td colspan="2">4.81</td></tr>
<tr><td>Integration Level</td><td>Tx+PR
+VCO</td><td>Rx+PR</td><td>Tx+VCO+
PR+Ant</td><td>Rx+PR
+Ant</td><td>Tx+PR
+Ant</td><td>Rx+PR
+Ant</td><td>Tx+PR
VCO+Ant</td><td>Rx+PR
+Ant</td><td>Tx+PR
+Ant</td><td>Rx+PR
+Ant</td><td colspan="2">Tx+Rx+PR
VCOs+Ant</td><td>Tx+Ant+
VCO+PR</td><td>Rx+PR
+Ant</td></tr>
<tr><td rowspan="2">Module Size (mm^2)</td><td>0.32</td><td>1.68</td><td>0.17</td><td>0.14</td><td>0.7</td><td>1.2</td><td>1.9</td><td>0.81</td><td>1.695</td><td>1.568</td><td colspan="2" rowspan="2">6</td><td>1.74</td><td>0.33</td></tr>
<tr><td colspan="2">2</td><td colspan="2">0.31</td><td colspan="2">1.9</td><td colspan="2">2.71</td><td colspan="2">3.263</td><td colspan="2">2.07</td></tr>
<tr><td>Antenna Type</td><td colspan="2">External
Horn</td><td colspan="2">On-chip
Dipole</td><td colspan="2">In-package
Bonding-Wire</td><td colspan="2">On-chip
Dipole</td><td colspan="2">On-chip
Ring</td><td colspan="2">On-chip
Leaky-
Wave</td><td colspan="2">On-chip
SIW-Microstrip</td></tr>
<tr><td>n (BER=10^{-n})</td><td colspan="2">11</td><td colspan="2">4</td><td colspan="2">-</td><td colspan="2">12</td><td colspan="2">9</td><td colspan="2">-</td><td colspan="2">-</td></tr>
<tr><td>Maturity Factor (%)</td><td colspan="2">7.4</td><td colspan="2">7.1</td><td colspan="2">26.3</td><td colspan="2">5.1</td><td colspan="2">9.7</td><td colspan="2">3.8</td><td colspan="2">2.5</td></tr>
</table>

Table 2.3 EHF and THF high-speed short-range wireless transceivers. Green colour = Antenna integrated on-chip. Blue colour = Antenna integrated on-package. Yellow colour = Antenna integrated on-board. Red colour = External antenna. PR = Pad Ring.

2.1.2 Impulse-Radio Front-Ends at Low Terahertz Frequencies

As seen in previous chapters, to integrate ultra-small antennas on-chip for our future nanoTRx require circuits operating at hundreds of GHz. The current electromagnetic spectrum allocation is only regulated up to 300 GHz, so it makes all the sense to explore THF frequency bands (300 GHz – 3 THz) for digital communications [41]. At such high frequencies, the communication channel attenuation is extremely high because it is inversely proportional to the distance and the frequency as states Friis transmission equation (free-path conditions):

$$\frac{P_r}{P_t} = G_t G_r \left(\frac{c_0}{4\pi d f_C}\right)^2 \quad (1)$$

where G_t and G_r are the transmitting and receiving antenna gains, f_C is the center frequency, d is the distance range, and c_0 is the speed of light [42]. This high attenuation can be alleviated if short distances are kept between Tx and Rx to maintain power consumption under reasonable levels, which is exactly the case for WNN. For WnMNs, a maximum distance range of 3 m is assumed and the highest channel attenuation happen at 3 THz where values above 90 dB are achieved. Nevertheless, for WNoCs, a reduced maximum distance range of 10 cm is assumed and at 3 THz the attenuation is above 60 dB, as it can be seen in Figure 2.2:

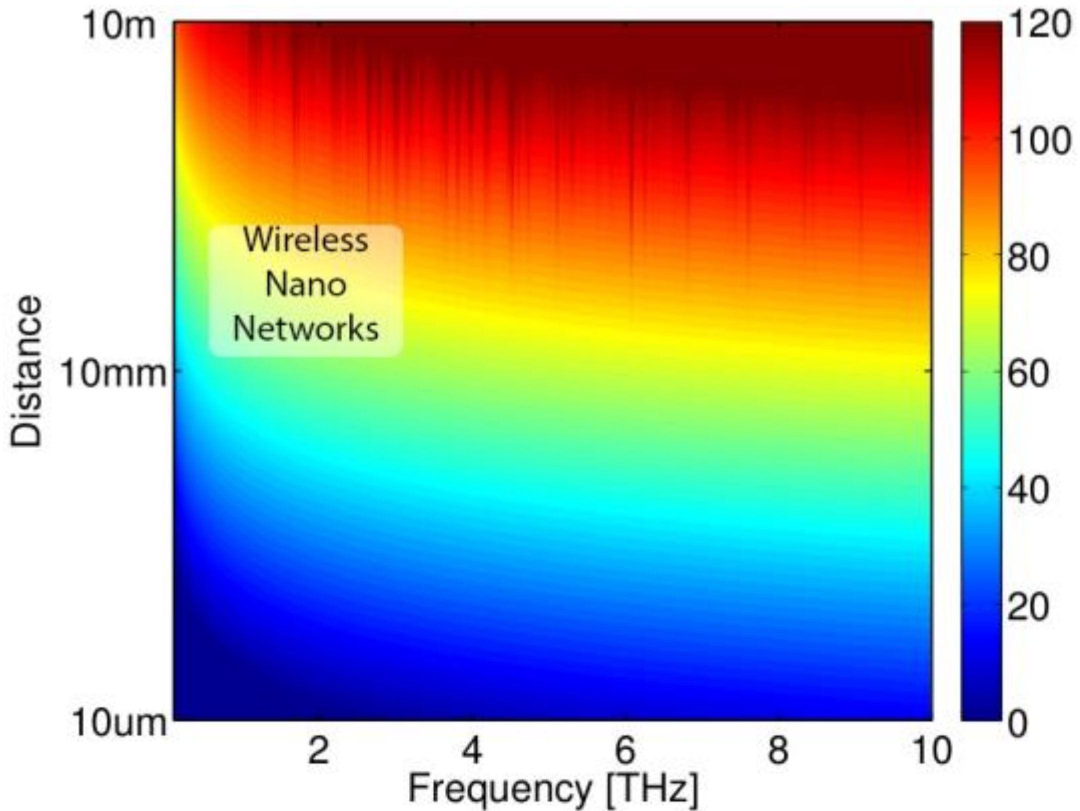


Figure 2.2 Total path-loss in dB as a function of frequency & distance for our targeted WNNs. Edited figure from [18].

In summary, nanoTRxs imply ultra-small antennas, ultra-small antennas involve high-frequency transmissions, high-frequency transmissions entail high channel-attenuation if distance ranges are long, therefore distance ranges must be kept short to reduce channel attenuation and maintain power consumption at sensible levels. Albeit, what about TRx data rate? Data rate (or capacity C) can be related to bandwidth B and signal to noise ratio (SNR) thanks to the Shannon theorem [43]:

$$C \approx B \log_2\left(1 + \frac{S}{N}\right) \tag{2}$$

During the 20th century, the TRx bandwidth was very limited (narrowband communication) due to large-size transistor technology, consequently the only way to increase data rate was to improve the SNR which allowed the implementation of more sophisticated modulations. During the beginning of the 21th century, the situation changed dramatically thanks to the aggressive transistor scaling trend driven by the mobile industry which allowed to conquer the SHF band-frequency, implying more bandwidth and the chance for the first time in history of improving C without increasing the complexity of the modulations. Impulse-Radio/Ultra-Wide-Band (IR/UWB) TRxs have been explored in [10][29][30][37], usually their architecture is simple and energy efficient. IR/UWB Rxs can be classified into coherent (complex but efficient) and non-coherent (simple but not that efficient) where an oscillator may be spared, and the latter case can be divided into autocorrelation and energy-detection (mixer not needed) types. Non-coherent energy-detection Rxs and classic pulse-generator/modulator transmitters Txs are extremely attractive for implementing at low-THz where the architecture is kept as simple as possible [44].

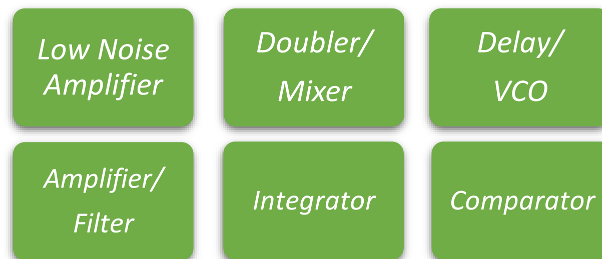


Figure 2.3 Diagram of the IR/UWB Rx-FE main modules integrated on a common substrate.

The main circuits forming an IR/UWB Rx-FE are: low-noise-amplifiers (LNAs), doublers/mixers, delay cells, variable-gain-amplifiers VGAs, integrators, and comparators shown in Figure 2.3. LNAs are fundamental blocks located just after the antenna in any Rx, especially at THz frequencies where the attenuation is really high even for short distance ranges, FoMs like power gain (G), noise-figure (NF), compression-point (CP_{-1dB}) and intermodulation-interception-point (IIP_3) need to be optimized to minimize noise and distortion. Mixer/Doubler circuits are a must for demodulating/modulating signals to baseband/RF frequencies, attenuation, noise and distortion must be minimized. Delays and voltage-controlled-oscillators (VCOs) might be also used for mixing with the RF/baseband(BB) signal. VGAs are used through the Rx BB

to increase or reduce channel sensitivity, thanks to a programmable gain. Integrators can be implemented on the digital back-end if needed as well. Comparators are fundamental blocks for analog to digital conversion. The main circuits forming an IR/UWB Tx-FE are (Figure 2.4): power-amplifiers (PAs), doublers/mixers, VCOs, and pulse generators (PGs) shown below. PAs need to maximize their gain and power efficiency. PGs usually are designed to generate Gaussian monocycles pulses to comply more easily with frequency plans.

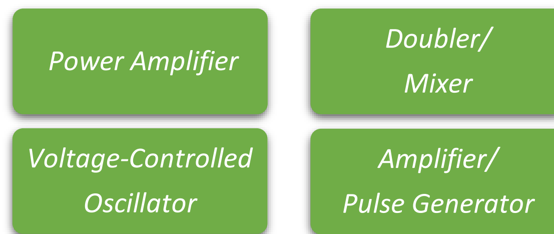


Figure 2.4 Diagram of the IR/UWB FE-Tx main modules integrated on a common substrate.

The IR/UWB TRx-BE is implemented with digital circuits: physical (PHY) layer (filters, spreaders, decoders, encoders, gain control, etc.) and sometimes medium-access-control MAC layer [10] are included.

2.2 Radio-Frequency Nanotransistors

The FET has been the most successful semiconductor device in microelectronics history: first as a switch for digital signal processing, and after several optimizations, as an amplifier for analog/RF signal processing. The outstanding scalability, driven by MOS technology, has provided increasing integration (lower price), increasing BW (higher data rate), and decreasing power consumption (lower energy intake) for ICs. Related to digital circuits, commercial MOSFETs are already entering the realm of nanoelectronics with the 10 nm node probably to be ramped-up by Intel before the end of 2017, although on-going scaling will face a halt until new disrupting technologies overcome the already predicted short-channel effects: shrinking MOSFET gates below 3 nm theoretically (5 nm practically) will not be possible due to direct-tunnelling current arising between drain and source contacts [9]. Digital circuits are out of the scope in this thesis, therefore transistors will be approached from an amplifier (not switch) point of view. Related to analog circuits, the most important design parameter is the intrinsic voltage gain Av (for baseband amplifiers), and the maximum frequency of oscillation f_{MAX} (for RF amplifiers).

2.2.1 Maximum Frequency of Oscillation

Well established FET devices based on bulk semiconductors as silicon (Si), silicon-germanium (SiGe), silicon-carbide (SiC), gallium-arsenide (GaAs), gallium-nitride (GaN), indium-phosphide (InP), and others are already facing scaling limitations. The device techniques used to reduce their size and increase their speed, as strained channel,

silicon-on-insulator (SOI), and three-dimensional (3D) gates, will be effective only in the short term. SoA high-electron-mobility-transistors (HEMTs) based on InP and GaAs, plus MOSFETs based on Si are already facing f_{MAX} capping when scaling channel length (L) below 25 nm due to short-channel effects as shown in Figure 2.5. The fastest transistors are InP HEMTs showing an astounding f_{MAX} of 1.5 THz for L = 25 nm with a channel width (W) of 2 x 10 µm [45], which would be enough to implement nanoTRx beyond 300 GHz. Unfortunately, this technology is not compatible with CMOS processes, therefore it is not possible to integrate digital BE and analog FE circuits on the same die which is a must for our vision. Record-high CMOS f_{MAX} is 420 GHz for L = 29 nm and W = 48 x 2.5 µm [46], in this case the main limitation is the quite low carrier mobility shown by silicon. As seen in Table 2.2 and Table 2.3, there is a niche group of fast transistors specifically targeted for monolithic-microwave-integrated-circuits MMICs: Silicon-Germanium SiGe BiCMOS which are not shown below, even though this technology offers digital transistors its scalability it is not enough to implement massive digital BEs for nanoTRx, besides analog transistors based on bipolar junctions (BJTs) (although fast and powerful) **do not** scale as well as the FET architecture. This is the reason why the research community is relentlessly investigating for new and scalable semiconductor processes that allow massive integration of different devices on the same die.

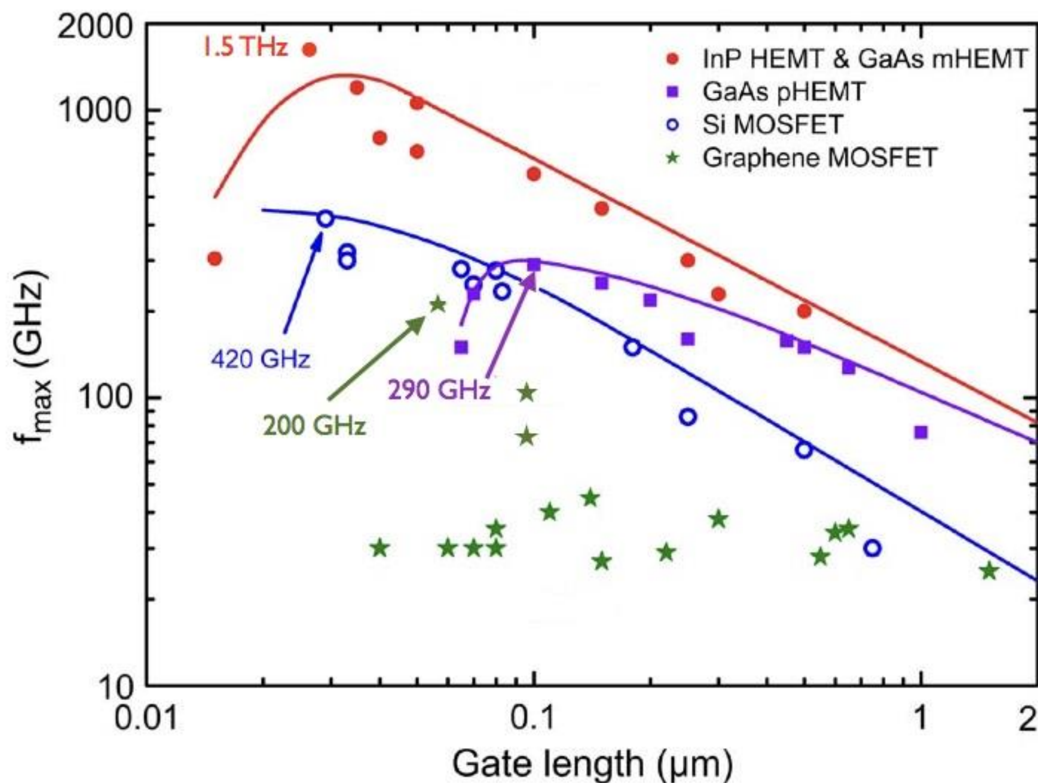


Figure 2.5 f_{MAX} (L) for different types of transistors: InP and GaAs HEMTs, MOSFETs, and graphene FETs. Edited from [47].

2.2.2 Two-Dimensional Semiconductors

Miniaturization is a mandatory requirement to implement WNN, therefore more in-depth research is needed to comprehend materials at the atomic level, which implies mastering the laws of quantum physics for developing future nanoTRx. An effective way to extend FET scaling could be the use of 2D materials (one-atom thick) as channels and dielectrics to improve the electrostatic gate-control [48]. For quite a long time 2D materials thought to be invariably unstable but in 2004 graphene was discovered by chance and it proved that the previous assumption was wrong [49]. Nowadays hundreds of different 2D materials are being studied as potential nanotransistor channel/gate-dielectrics by the research community: **graphene**, molybdenum-disulphide (MoS_2), tungsten-diselenide (WSe_2), boron-nitride (BN), germanane, etc. All of them have their benefits and drawbacks, but graphene thanks to its extremely high carrier mobility and saturation velocity keeps leading the quest as a channel for future RF nanotransistors that do not need to switch-off, even though it is losing momentum due to its inherent lack of bandgap which precludes strong current saturation. Germanane is quite promising offering high mobilities (but lower than graphene) although having a bandgap, therefore a better intrinsic gain theoretically, nevertheless it is too early to draw plausible conclusions on this new device yet [50]. The exhibited low mobility in MoS_2 discards them as a plausible option for RF circuits [51].

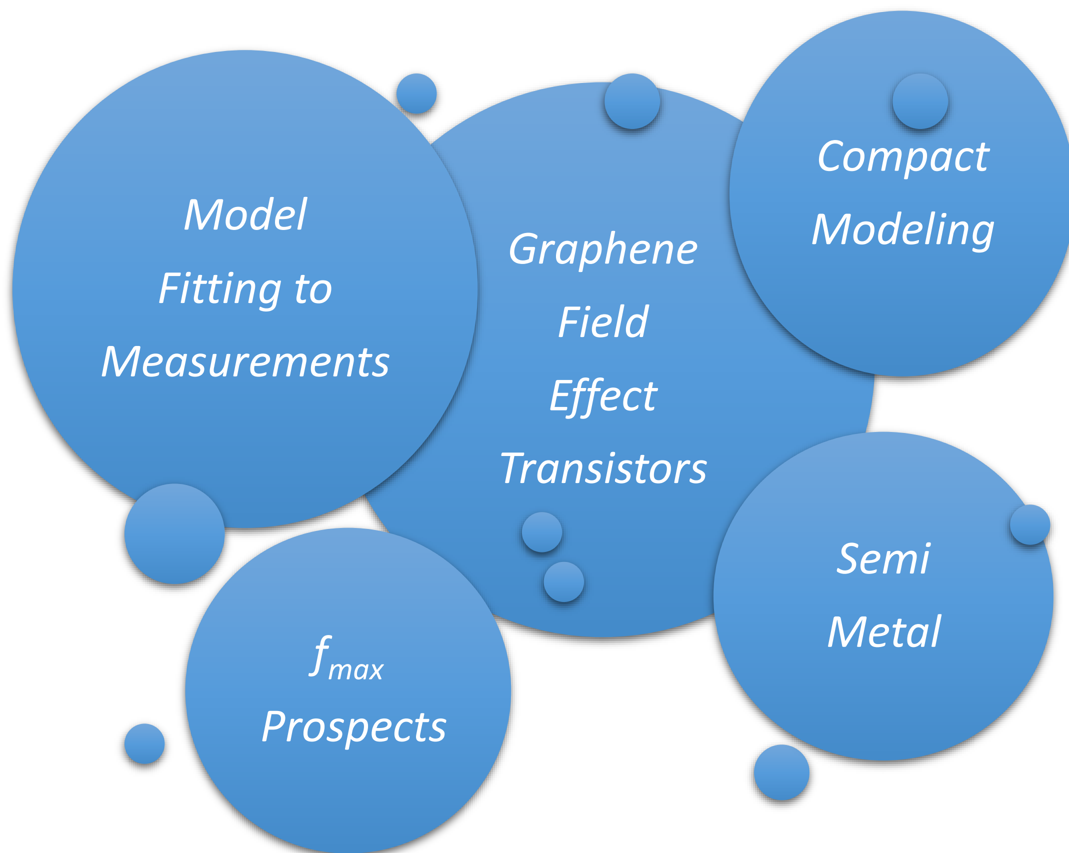
2.3 Conclusions

After realizing a careful analysis of the existing SoA TRx in literature, we conclude that miniaturisation at device level and simplification at architecture level is a must to target future wireless nanoTRx **(Journal III & Conference C)**. It has been shown that with existing RF transistors is extremely challenging to design the architectures required due to the impossibility of scaling further to achieve the required speeds and/or their impossibility of being integrated with digital transistors. Hypothetically speaking there is an urgent need for FETS that are able to scale with a f_{MAX} beyond 2 THz, consequently new discovered 2D materials are proposed as channels for future nanotransistors (Table 2.4). IR/UWB techniques need to be carefully inspected at much higher frequencies as they may reduce the complexity of the nanoTRx, although this subject is out of the scope for this thesis. New materials to fabricate innovative transistors are needed to achieve such high levels of speed and integration to achieve THz-IR TRx. Chapter 3 is rigorously analysing graphene FETs (GFETs), and chapter 4 present very basic circuits based on this new technology.

	f_{MAX}	CMOS Compatible
MOSFET		
SiGe HBT		
III-V HEMT		
GFET		

Table 2.4 RF nanotransistors against f_{MAX} and digital CMOS compatibility. Green colour stands for 'very high', Blue colour stands for 'high', yellow colour for 'medium' and red colour for ´low'

3 Nanotransistors: Graphene FETs



Graphene, the first 2D material discovered in history, is introduced and its extraordinary electronic properties explained in detail. Consequently, it is proposed as a plausible channel for RF nanotransistors thanks to its high carrier mobility and one-atom thickness which should imply very fast and small transistors. This chapter will concentrate on graphene FETs (GFETs) among other graphene transistors approached by the research community, and the importance of chemical-vapor-deposition (CVD) techniques for GFET fabrication will be highlighted. The main challenge for GFETs, the weak current saturation due to its lack of bandgap, is analysed and discussed as well. Compact models for transistors are necessary tools for circuit simulators, an optimized model for GFETs based on a drift-diffusion approach is presented and its benefits and limitations commented. The model parameters are fitted to different relevant GFET technologies and a scaling study for f_{max} based on simulations is derived to assess their potential for future nanoTRx.

3.1 Graphene Semimetals

Graphene is a very promising 2D material that has many chances to make an impact into the next post-silicon era for nanoelectronics [3]. Wallace first explored the theory of graphene in 1947 [52], but Mouras didn't coin the term until 1987 [53], and Novoselov isolated it for the first time in 2004 [49]. Since this important achievement was recognized with the Nobel Prize in 2010, an overwhelming interest has aroused on

graphene due to its outstanding properties in many aspects of solid-state physics. In 2013, the European Union secured 1 billion € grant for graphene research. Graphene is a semimetal or zero-bandgap semiconductor, one-atom-thick layer of carbon structured in a honeycomb lattice as seen in Figure 3.1a with (1) extraordinary mechanical and thermal properties: transparency, flexibility, strength, high temperature conductivity [54]; and (2) very interesting electronic and optical properties: ambipolar carrier transport, high carrier mobility, high carrier saturation velocity [55], high current density, broadband optical absorption, and last but not least, **compatible** with silicon technologies. Future graphene applications are endless: nanophotonics, nanoelectronics, nanomaterials, etc. This thesis is analysing graphene from a nanoelectronics perspective paving the way towards future nanoTRX as introduced in chapter 2.

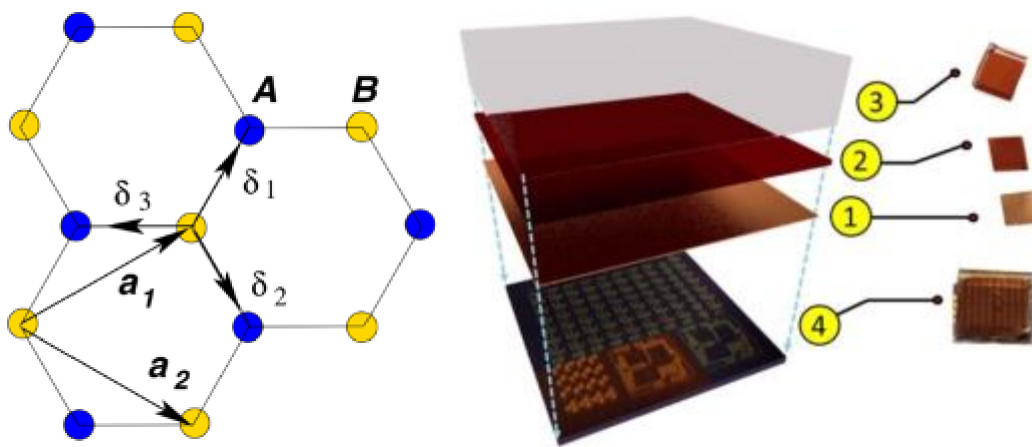


Figure 3.1 (a) Graphene is made of carbon atoms arranged in hexagonal structure, made out of two interpenetrating triangular lattices (a_1, a_2 are the lattice unit vectors, and ∂_1, ∂_2, ∂_3 are the nearest neighbour vectors) [56]. *(b) Process flow for the dry transfer of graphene using both a polymer layer as well as a photoresist layer* [58].

3.1.1 Large-Scale Fabrication Techniques

A high quality, scalable, silicon compatible and economical lithography process is the first requirement in order to fabricate graphene nanotransistors for nanoTRx. The predominant graphene synthesis techniques include: (1) mechanical exfoliation, (2) epitaxial growth, and (3) CVD. The first method is not scalable and suffers from random orientation, shape and size of the flake despite pristine quality of the produced graphene. In the second, the main challenge is its incompatibility with CMOS processes, besides it is difficult to control the uniformity and number of graphene layers grown over a wafer, along with resulting surface roughness. The third technique is CVD, our targeted technology, which seems the most promising for large scale production, scope for scaling, and compatibility with silicon technologies [57]. The main issue with CVD graphene is its quality, its intrinsic polycrystalline characteristic diminishes the carrier-mobility (μ) and this should be solved to remain competitive against III-V semiconductors. The transfer process from copper foils to silicon dioxide (SiO_2) substrates needs also improvement to minimize impurities and be fully mass producible.

In Figure 3.1b: (1) shows the copper foil with graphene grown on both sides using CVD; (2) shows the photoresist layer which is deposited on the graphene likewise; (3) shows the silicone elastomer layer; and (4) shows the chip [58]. If CVD issues can be solved, hybrid process platforms will be enabled where digital circuits could be implemented with ultra-low-power MOSFETs, and BB/RF circuits with ultra-fast GFETs, reducing production costs dramatically.

3.1.2 High Mobility and Saturation Velocity Carrier Transport

The main reason that has driven so many researchers to investigate graphene is its high mobility and saturation velocity for **both** electrons and holes, both figures are fundamental for RF nanotransistors to achieve high f_{max}. A record-high intrinsic carrier mobility μ = 80000 cm^2 / V.s has been achieved by CVD graphene on a exfoliated h-BN substrate [59], unfortunately CVD h-BN process is not mature yet for mass production, although this value is very close to InSb mobility as shown in Table 3.1:

	Electron Mobility	*Saturation Velocity*	*Energy Bandgap*
	μ (cm^2/V.s)	*v_{sat} (cm/s)*	*E_g (eV)*
Indium Antimonide	*88×10^3*	*4×10^7*	*0.18*
CVD Graphene on hBN	*80×10^3*	*3.6×10^7*	*0*
Exfoliated Graphene on WS_2/SiO_2	*38×10^3*	*3.6×10^7*	*0*
Indium Arsenide	*33×10^3*	*3.5×10^7*	*0.36*
Exfoliated Graphene on SiO_2	*24×10^3*	*3.6×10^7*	*0*
Germanane	*20×10^3*	*-*	*1.5*
CVD Graphene on SiO_2	*16×10^3*	*3.6×10^7*	*0*
Epitaxial Graphene on C-face SiC	*8.7×10^3*	*3.6×10^7*	*0*
Gallium Arsenide	*8×10^3*	*0.9×10^7*	*1.43*
Germanium	*3.6×10^3*	*0.7×10^7*	*0.66*
Epitaxial Graphene on Si-face SiC	*2×10^3*	*3.6×10^7*	*0*
Gallium Nitride	*1.6×10^3*	*2.4×10^7*	*3.4*
Silicon	*1.4×10^3*	*1×10^7*	*1.12*
Molybdenum Disulphide	*0.3×10^3*	*0.3×10^7*	*1.8*

Table 3.1 Electron μ, v_{sat}, and E_g for several types of graphene, 2D and conventional semiconductors [60][48][61].

Exfoliated graphene on SiO_2 substrate has shown μ = 24000 cm^2 / V.s, a value superior to Ge μ, the drawback is that exfoliated graphene is not mass producible. And a μ = 16000 cm^2 / V.s has been measured by CVD graphene on SiO_2 substrate, a lower value than in Ge, but a solution well-suited for industrial fabrication. Mobility is a parameter measured at low electric-fields therefore is more adequate for describing long-channel transistors, while saturation velocity is measured at high electric fields and it is more suited for short-channel transistors. A measured intrinsic saturation velocity of $v_{sat} = 3.6 \times 10^7$ cm/s has been demonstrated by a suspended CVD graphene channel [62], only InSb offers a higher value.

3.1.3 The Zero-Bandgap Challenge

A zero-bandgap for graphene implies for nanotransistors: (1) Ambipolar carrier transport, (2) Low on-off current (I_{on}/I_{off}) ratio and (3) low current saturation. (1) means that in monolayer graphene transport may be dominated by electrons or holes depending on the voltage biasing, so theoretically it does not need external doping to generate P-type or N-type transistors as shown in Figure 3.2a. (2) is a must feature for digital transistors the ability to switch on and off, and to show off-currents I_{off} below nanoamperes, this is the reason why large-area graphene is already discarded for logic -circuit applications. (3) is fundamental for analog circuits, a high current saturation is needed in transistors in order to have high amplification. Other variants of graphene transistors with improved current saturation have been proposed in the research literature. The most notable ones are: Bernal-stacked bilayer GFETs (BSBGFETs) which enable a small bandgap induced through a vertical electric field [63], graphene-nano-ribbon FETs (GNRFETs) where quantum confinement leads to a bandgap [64], and graphene-base-transistors (GBTs) where graphene is used as the base contact for vertical hot electron transistors [65], and BiGFETs where two CVD graphene layers are artificially stacked **(Conference E)**. BSBGFETs main drawback is that a second gate is needed to induce a bandgap and that the two layers need to be Bernal-stacked which precludes its compatibility with a CMOS process because large-area CVD growth of Bernal stacked bilayer graphene is still in its infancy, mostly because of the polycrystalline nature of growth which leads to mixed orientations of the graphene layers. GNRFETs have narrow widths ($W < 5$ nm), where bandgap is inversely proportional to W, although μ worsens dramatically due to edge disorders which implies severe challenges in manufacturability and process control. GBTs offer a great on-off current ratio even though they are not as scalable as GFETs due to their bipolar architecture. BiGFETs devices show enhanced tendency to current saturation, which leads to reduced minimum output conductance values. This results in improved intrinsic voltage gain of the devices when compared to monolayer GFETs. The improvement in current saturation may be attributed to increased charge carrier density in the channel and thus reduced v_{sat} due to carrier-carrier scattering **(Journal IV)**. In Figure 3.2b the band structure differences GFET devices are summarized.

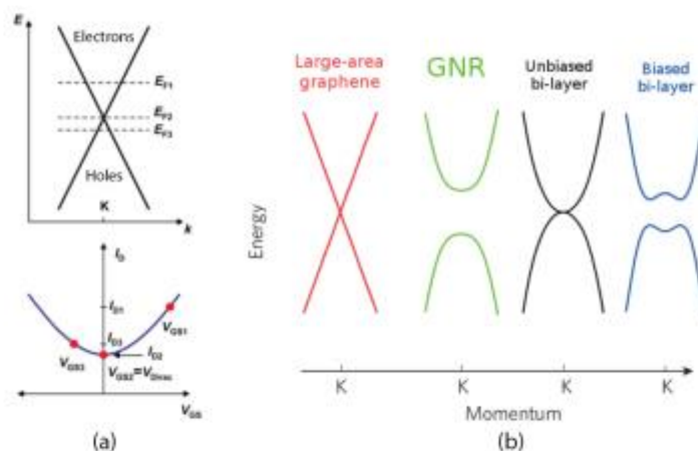


Figure 3.2 Graphene bandgap. (a) GFET ambipolar conduction, where E_f is the Fermi energy level, I_d is the drain-to-source current, and V_{gs} is the gate to source voltage. (b) Different graphene band structures. Edited from [47].

3.2 Graphene FETs

GFETs are promising devices for future RF nanotransistors compatible with CMOS processes. The first graphene device to be implemented was a back-gate GFET in 2004 [49]. After 2 years, a side-gate GFET was built [66], and only one year later, the first top-gate GFET was demonstrated [67]. These device show high carrier µ and v_{sat} which usually imply high transconductance (g_m) even at high bias voltage, and has translated into a record-high cut-off intrinsic frequency (f_t) of 427 GHz for L = 67 nm shown by exfoliated graphene channel on SiO_2 substrate [68]. f_t is the frequency at which the magnitude of h_{21} (current gain) has dropped to unity, and f_{max} is the frequency at which the magnitude of U (Mason's unilateral power gain) equals unity. For most RF circuits, power gain and f_{max} are more important than current gain and f_T [47]. As seen before in Figure 2.5, a recently published record-high f_{max} = 200 GHz for L = 60 nm and W = 2 x 10 µm has been achieved for a GFET fabricated with a CVD graphene channel on SiO_2 substrate [69]. Unfortunately, last figure is more than 3 times below the very recent record-high InP HEMT f_{max}, but almost equal to record-high CMOS f_{max} when extrapolated to the same L. It should be noted that this comparison is between mature technologies and a rather new one which it is not mastered yet, therefore GFET f_{max} is expected to improve faster than the rest of semiconductors during next years. Figure 3.3a is showing a typical GFET cross-section layout, where L is the channel length, t_{ox} is the gate dielectric thickness, L_{acc} is the channel access length, V_{gs} is the gate-to-source voltage, V_{ds} is the drain-to-source voltage, and I_{ds} the drain-to-source current.

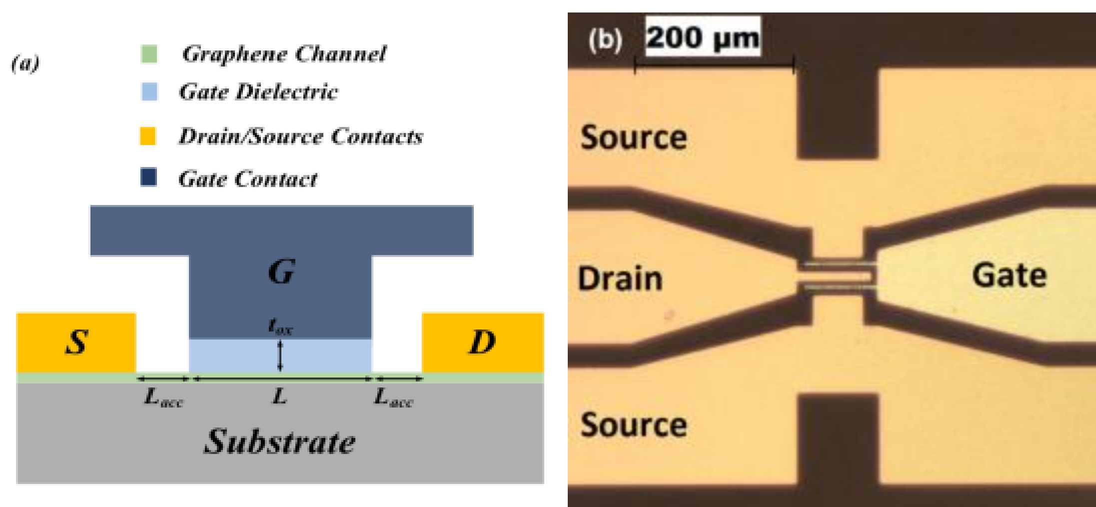


Figure 3.3 GFET device. (a) Cross-section layout. (b) Top-section optical image of a device processed in University of Siegen

3.2.1 Fabrication based on CVD Monolayer Graphene

The GFET fabrication process developed by University of Siegen goes as follows: thermally oxidized (85 nm) p-Si <100> wafers with a boron doping concentration of 3 x 10^{15} cm^{-3} were used as starting substrates in Figure 3.3b; the samples were cleaned in acetone, followed by isopropyl alcohol and finally rinsed with de-ionized water; followed by this in-house grown CVD graphene monolayer was transferred using an electro-

delamination method with poly-methyl-methacrylate (PMMA) support layers; the PMMA layers were then dissolved in acetone; channels were defined using optical lithography and patterned using oxygen plasma based reactive ion etching; thermal evaporation of a 10 nm / 90 nm Cr/Au stack followed by a lift-off in warm acetone was used to define source/drain contact pads; 10 nm SiO_2 was e-beam evaporated as the top-gate oxide; thermal evaporation of 100 nm Al gate metal and another subsequent lift-off in acetone completed the device fabrication. Another similar set of devices was fabricated using atomic layer deposition of Al_2O_3 gate dielectrics with an effective-oxide-thickness (EOT) of approximately 10 nm, with all other fabrication steps remaining the same as above **(Conference E)**.

3.2.2 Transconductance, Output Conductance and Voltage Gain

The GFET transconductance must be as high as possible:

$$g_{m_max} = \left| \frac{\partial I_{ds}}{\partial V_{gs}} \bigg|_{V_{ds=cons.}} \right| \tag{3}$$

and the output conductance, as low as possible:

$$g_{o_min} = \left| \frac{\partial I_{ds}}{\partial V_{ds}} \bigg|_{V_{gs=cons.}} \right| \tag{4}$$

to maximize the voltage gain for the most extensive V_{gs} and V_{ds} voltage ranges:

$$A_{v_max} = \left| \frac{g_{m_max}}{g_{o_min}} \right| \tag{5}$$

At the present GFET g_{m_max} values found in literature are usually below 1 mS/µm, although there are exceptions to this trend: the five best g_{m_max} values ever measured for top-gate GFETs to our knowledge are collected in Table 3.2. The parameters described in this table are: V_{gs} is the gate to source voltage, V_{ds} is the drain to source voltage, I_{ds} is the drain to source current, µ is the average carrier mobility, L is the channel length, W is the channel width, EOT is the silicon equivalent oxide thickness, K is the dielectric constant, t_{ox} is the gate dielectric thickness, $R_{d/s}$ is the drain/source contact resistivity, $L_{d/s}$ is the ungated channel length, and ђω is the surface phonon energy of the substrate. It is shown that the highest g_{m_max} achieved is 2.9 mS/µm for L = 100 nm, demonstrated by quasi-free-standing epitaxial bilayer GFETs [70]. Extremely low contact resistances $R_{d/s}$ < 42.5 Ω.µm are paramount to achieve such figure thanks to bilayer graphene and gold contacts interaction, but also a smooth interface between the graphene channel and its 4H-SiC substrate which reduces carriers scattering. Nevertheless, that GFET g_{m_max} value is still below the record-value 3.45 mS/µm for L = 70 nm achieved by InGaAs quantum-well MOSFETs [71]. Epitaxial GFETs are suited for batch fabrication at wafer level, although they are not CMOS compatible, therefore reducing costs technology will be a challenge. Two exfoliated GFETs [68][72] are also showing high g_{m_max}, mainly due to the excellent µ exhibited, the drawback is that is not possible to mass-produce them. Finally a CVD GFET [73] is showing a remarkable g_{m_max}

value thanks to its extremely thin EOT and embedded gate approach. These GFETs are mass producible and CMOS compatible, although they need to increase their g_{m_max} beyond 2.7 mS/µm for L = 37 nm to be competitive against other CMOS-friendly arising technologies like SiGe FinFETs [74]. The main challenges to achieve higher g_{m_max} figures in GFETs are: (1) the quantum capacitance (C_q), due to the density-of-states (DOS) bottleneck occurring in graphene, which is impairing the benefit of decreasing EOT for improving the electrostatic control over the channel, and the degraded µ due to crystal imperfections and impurities in synthesized graphene compared to exfoliated graphene; (2) the un-optimized interface between gate dielectrics and graphene channels which are degrading the electrostatic control, encapsulating graphene between h-BN layers [75] has been demonstrated to bring improvement, but again, the use of exfoliated h-BN crystals makes it ill-suited for mass production; (3) the un-optimized graphene-metal contacts (R_{con}) which are impairing the benefit of using ultra-low resistance channels, that is why choosing the right metal for contacting the graphene channel is a must [76]–[78], and gate alignment is also needed to reduce the ungated graphene channel to the minimum minimizing access resistances (R_{acc}) [79]; and (4) the low surface-phonon energy substrates which increase carrier scattering. Nevertheless, the most challenging issue for GFETs is to reduce the high g_{o_min} shown in a channel where charge cannot be fully depleted due to the lack of a bandgap. Consequently, a lot of research effort is put into achieving current saturation through different techniques: artificially stacked-bilayer GFETs **(Conference E & Journal IV)**, graphene-on-silicon FETs (GoSFET) [80], oblique double-gate GFETs [81], graded-potential gate GFETs [82], GFETs based on nano-perforated graphene [83], and dual-gate GFETs [84]. Nowadays the g_{o_min} values for single-gate GFETs found in literature are usually over 100 µS/µm, although there are exceptions: the five best g_{o_min} values ever measured for top-gate GFETs are shown in Table 3.3 where negative-differential-resistance (NDR) behaviour (g_o crossing zero at one or more bias voltages) has been observed in [70][85][86]. These record values are well below InGaAs quantum-well MOSFETs g_o = 100 µS/µm for L = 70 nm and SiGe FinFETs g_o = 20 µS/µm for L = 37 nm. The mechanisms involved in current saturation for GFETs are various and complex: (1) the partial (due to graphene ambipolarity) depletion of the charge close to the drain at specific voltage bias (V_{gs}, V_{ds}); (2) the saturation of carrier velocity (v_{sat}) due to phonon scattering induced by impurities and surrounding materials; (3) charge traps due to defects of the gate dielectric; and (4) self-heating of the channel [87]. Having (1) is necessary but not sufficient to achieve full saturation, (2) helps to reduce g_o but at the same time increases g_m, so there is a clear trade-off, (3) is a non-desired effect that should be minimized as much as possible by improving the quality of the channel and the dielectric, and (4) is an unavoidable effect. Discerning the dominant (if any) mechanism attributed is still under debate in the research community, and that is paramount to learn how to control current saturation for GFETs, i.e. achieving g_{m_max} and g_{o_min} values at the same bias range to maximize amplification.

Graphene FETs		Bias Voltages V_{gs} (V), V_{ds} (V)		Graphene Channel			Gate Dielectric			Drain/Source Contacts		Substrate
Author	Year	g_{m_max} (μS/μm)	I_{ds} (μA/μm)	μ (cm²/V.s)	L (nm)	W (nm)	EOT (nm)	K [88]	t_{OX} (nm)	$R_{d/s}$ (Ω.μm)	$L_{d/s}$ (nm)	ħω (meV) [89]
Yu et al. [70]	2016	-0.2, -0.5		Epitaxial Bilayer			Al_2O_3			Au		4H-SiC
		2900	1750	3000	100	2f x 15000	4.3	9	10	< 42.5	240	116
Liao et al. [72]	2010	0.1, 1		Exfoliated Monolayer			GaN Nanowire			Ti/Pt/Au		SiO_2
		2300	4500	> 11200	90	1f x 2000	7.1	10	18.3	< 260	10	58.9
Wu et al. [90]	2011	0.8, 2.2		Epitaxial Monolayer			Si_3N_4			Pd/Au		SiC
		2200	1300	> 3000	2500	2f x 500	8.4	7	15	< 250	40	116
Cheng et al. [68]	2012	0.9, 1		Exfoliated Monolayer			Al_2O_3			Pd/Au		SiO_2
		1300	-2500	> 10000	67	1f x 8000	5.6	9	13	100	10	58.9
Han et al. [73]	2011	-0.1, -1		CVD Monolayer			HfO_2			Pd/Au		Air
		1200	600	n.d.	500	6f x 5000	1.75	8.9	4	< 560	< 100	n.a.

Table 3.2 Extrinsic transconductance record-high values g_{m_max} for top-gate GFETs fabricated by different research groups. n.a: Parameter non-applicable.

Graphene FETs		Bias Voltages V_{gs} (V), V_{ds} (V)		Graphene Channel			Gate Dielectric			Drain/Source Contacts		Substrate
Author	**Year**	g_{o_min} (µS/µm)	I_{ds} (µA/µm)	µ (cm^2/V.s)	L (nm)	W (nm)	EOT (nm)	K [88]	t_{OX} (nm)	$R_{d/s}$ (Ω.µm)	$L_{d/s}$ (nm)	ħω (meV) [89]
Yu et al. [70]	2016	-1, -0.7		Epitaxial Bilayer			Al_2O_3			Au		4H-SiC
		0	4000	3000	100	2f x 15000	4.3	9	10	< 42.5	240	116
Han et al. [86]	2012	-2, -1.3		CVD Monolayer			HfO_2			Ti/Pd/Au		Air
		0	400	n.d.	500	2f x 10000	1.75	8.9	4	< 1150	< 100	n.a.
Bianchi et al. [85]	2015	-1.4, -2.5		CVD Monolayer			Al_2O_3			Au		SiO_2
		0	-400	750	2000	2f x 5000	2.5	6.2	4	250	250	58.9
Song et al. [80]	2016	-3, -3.5		CVD Monolayer			Al_2O_3			Pd/Au		Si
		0.4	30	2700	20000	1f x 10000	8.7	9	20	100	n.d.	63
Bai et al. [91]	2011	0.2, -1.3		CVD Monolayer			HfO_2			Pd/Au		SiO_2
		2	-294	n.d.	5600	1f x 3400	8.2	19	40	< 1360	< 100	58.9

Table 3.3. Extrinsic output conductance record-low values g_{o_min} for top-gate GFETs fabricated by different research groups. n.d: Data non-available. n.a: Parameter non-applicable.

3.3 GFET Compact Models

Numerical models are a must to predict the performance of graphene transistors through computer simulations. These models are based on two different approaches: semi-classical transport or quantum transport. Quantum transport models based on non-equilibrium Green's function are very time consuming in computation terms, but they are able to model very accurately band-to-band tunnelling and ballistic transport [92]. Semi-classical models are based on drift-diffusion transport, being less accurate but faster when running simulations. Nevertheless, numerical models are still too complex and resource consuming for circuit simulators, and their scalability to circuits with large numbers of transistors is not appropriate. Hence compact models, also called analytical models, come into play. Several compact models, most of them based on semi-classical transport, have been proposed for monolayer GFETs in the research literature. The first GFET semi-analytical model was proposed by Meric et al. in [93]. Thiele et al. [94] improved Meric's model by modeling the quantum capacitance C_q dependence on the channel potential. Fregonese et al. proposed a compact solution (circuit simulator compatible) for Thiele model in [95]. Rodriguez et al. [96] simplified this model to ease hand calculations for circuit design, but restricting its use only to small-signal design. The main advantage of the model proposed by the University of Bordeaux [95] over other compact and numerical GFET models is that it captures the main physical characteristics of GFETs in a simple mathematical form (i.e. a small set of equations without self-contained solutions). This model demands very low computational load for a circuit simulator, a characteristic of paramount importance for instance when designing complex circuits, therefore a Verilog-A version has been implemented. However, during the model parameter fitting to experimental measurements, non-desired artefacts were observed on the simulations when scaling parameters, precluding further exploration for circuits. Consequently, an optimized compact-model is proposed to improve the model accuracy and scalability and to allow large-signal circuit design which is the main purpose of this thesis **(Journal I & II)**.

3.3.1 Drift-Diffusion against Quasi-Ballistic Carrier Transport

Under practical conditions for common dielectric substrates, room temperature and ambient environment, a carrier mean-free-path (MFP) of a few hundreds of nanometers have been registered for GFETs [97]. However, the MFP limiting factors are under debate yet [98][99]. The drift-diffusion (DD) carrier transport theory, used up to today to simulate microelectronic transistors is applicable while L is bigger than the MFP, otherwise the carrier transport is ruled by quantum-ballistic physics law. Qualitatively speaking, standing to the common MFPs values, for L > 1 µm the drift-diffusion theory is working with great accuracy, while in the L < 10-100 nm range ballistic transport starts to dominate [100]. Theoretically, for 10-100 nm < L < 1 µm, transistors work under the so-called "quasi-ballistic regime" where the drift-diffusion description is losing accuracy due to the weak scattering condition. Nevertheless, if L ~ MFP very recent study has shown how the current-to-voltage characteristic of nanoscale devices is still well described by DD models if mobility and saturation velocity are treated as fitting parameters [101]. The GFETs fabricated and measured by the University of Siegen have channel lengths above hundreds of nanometers. At that sizes DD transport applies, that

is why since the beginning a model based on that assumption has been selected and developed. It is true that during the last years, other research groups have succeeded in fabricating GFETs below 100 nm in which quasi-ballistic carrier transport should be dominating. Although, after successfully fitting many short-channel GFETs with our DD model, we have decided to keep on with the DD approach thanks to its simplicity and flexibility for scalability despite the potential loss of accuracy. In chapter 4.1.1 a comparison between a drift-diffusion compact model and a virtual-source (hybrid ballistic/drift-diffusion) compact model is performed.

3.3.2 Current-to-Voltage Model Optimization for Device Scaling

A GFET symbol and its correspondent current-to-voltage (I-V) compact-model are shown in Figure 3.4. The metal-graphene high contact-resistance at the drain and the source is a non-desired effect that abruptly degrades the device extrinsic transconductance g_m.

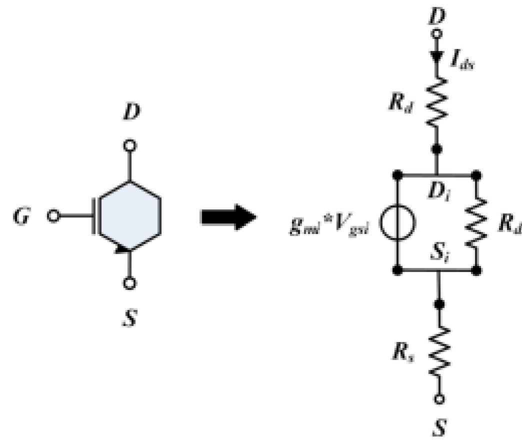


Figure 3.4 GFET symbol and I-V compact model, including extrinsic parasitics (R_s and R_d) modeling graphene-metal contact and non-gated graphene resistances.

Usually values for contact resistivity are above $R_{d/S}$ = 100 Ω.µm (Table 3.2 and Table 3.3), therefore contacts need to be taken into account until they are optimized and made negligible for graphene transistors. The non-gated graphene between gate and drain/source contacts is also modelled as an access resistance (R_{acc}). Therefore, the extrinsic resistances R_d and R_s are just the sum of the metal-graphene contact and the non-gated graphene resistances [102]:

$$R_{d/s} = \frac{R_{con} + R_{acc}L_{acc}}{W} \quad (6)$$

where R_{con} is the metal-graphene contact resistivity in Ω.µm units, R_{acc} is the graphene sheet resistance in Ω/□ units, L_{acc} is the channel access length. The GFET drain-to-source current I_{ds} can be described as in [94] when assuming drift-diffusion transport:

$$I_{ds} = \mu W \frac{NUM}{DEN} \quad (7)$$

where the numerator NUM is defined by:

$$NUM = NUM_1 + NUM_2 = \int_0^{V_{dsi}} |Q_{net}| dV + en_{pud}V_{dsi} \tag{8}$$

wherein Q_{net} is the net-mobile charge density, e is the electron charge, n_{pud} is the residual charge density:

$$n_{pud} = \frac{\Delta^2}{\pi \hbar^2 v_f^2} \tag{9}$$

where Δ represents the spatial inhomogeneity of the electrostatic potential, ħ is the reduced Planck constant and v_f is the Fermi velocity. Q_{net} is calculated as follows:

$$|Q_{net}| = \beta \left(\frac{-C_{top} + \sqrt{C_{top}{}^2 + 4\beta \left| C_{top}(V_{gsi} - V) + eN_f \right|}}{2\beta} \right)^2 \tag{10}$$

where β is a constant factor and C_{top} is the top-gate capacitance:

$$\beta = \frac{e^3}{\pi \hbar^2 v_f^2} \qquad C_{top} = \frac{\varepsilon_r \varepsilon_{ox}}{t_{ox}} \tag{11}$$

wherein ε_{ox} is the vacuum permittivity, ε_r is the relative permittivity, t_{ox} is the dielectric thickness, V_{gsi} is the intrinsic gate-to-source voltage, V is the potential variation along the channel due to V_{ds}, and N_f is the net substrate doping. As shown in [96], two expressions are obtained when performing the change of variable z with V_{eff}:

$$z = C_{top}(V_{eff} - V) \qquad V_{eff} = V_{gsi} + \left(\frac{eN_f}{C_{top}} \right) \tag{12}$$

to calculate an exact solution for the integral in equation (8). If z is taking positive values:

$$NUM_{1(z>0)} = -\frac{1}{\beta^2 C_{top}} \left[\frac{C_{top}{}^4}{32} - \frac{C_{top}\left(C_{top}{}^2 + 4\beta z\right)^{\frac{3}{2}}}{12} + \frac{(\beta z)^2}{2} + \frac{\beta C_{top}{}^2 z}{2} \right]_{z_1}^{z_2} \tag{13}$$

where z_1, and z_2 are:

$$z_1 = C_{top} V_{eff} \qquad z_2 = C_{top}(V_{eff} - V_{dsi}) \tag{14}$$

If z is taking negative values:

$$NUM_{1(z<0)} = -\frac{1}{\beta^2 C_{top}} \left[-\frac{C_{top}{}^4}{32} + \frac{C_{top}\left(C_{top}{}^2 - 4\beta z\right)^{\frac{3}{2}}}{12} - \frac{(\beta z)^2}{2} + \frac{\beta C_{top}{}^2 z}{2} \right]_{z_1}^{z_2} \tag{15}$$

On the other hand, the denominator DEN in equation (7) is calculated as:

$$DEN = L + |DEN_2| = L + \left|\int_0^{V_{dsi}} \frac{\mu}{v_{sat}} dV\right| \tag{16}$$

where v_{sat} is the carrier saturation velocity:

$$v_{sat} = \frac{\omega}{\sqrt{\left(\frac{\pi Q_{net}}{e} + \pi n_{pud}\right)}} \tag{17}$$

wherein ђω is the surface phonon energy of the substrate. In [95], v_{sat} is approximated by considering an average charge density $Q_{net\text{-}AV}$, which it is carried out to simplify the calculation of DEN_2. This is done at the cost of introducing distortion at the Dirac point when scaling down L and t_{ox}, and/or scaling up V_{ds} and μ. A new exact solution for DEN_2 is proposed to overcome this drawback. The following expression is obtained when performing again the change of variable in equation (13) to calculate an exact solution of the integral below **(Journal I & II)**:

$$\begin{aligned} DEN_2 &= \frac{\mu}{\omega}\sqrt{\frac{\pi}{e}}\int_0^{V_{dsi}} \sqrt{|Q_{net}| + en_{pud}}\ dV \\ &= \frac{-\mu}{2\omega C_{top}}\sqrt{\frac{\pi}{e\beta}}\int_{z_1}^{z_2} \sqrt{\left(\frac{4\beta en_{pud} + C_{top}{}^2 - 2C_{top}\sqrt{C_{top}{}^2 + 4\beta|z|}}{C_{top}{}^2 + 4\beta|z|}\right)}\ dz \end{aligned} \tag{18}$$

If z is taking positive values, another change of variable x is applied in:

$$x = \sqrt{C_{top}{}^2 + 4\beta z} \tag{19}$$

and the integral can be solved analytically as:

$$\begin{aligned} DEN_{2\,(z>0)} &= \frac{-\mu}{4\omega\beta C_{top}}\sqrt{\frac{\pi}{e\beta}}\int_{x_1}^{x_2}\left(x\sqrt{x^2 + bx + c}\right)dx \\ &= \frac{-\mu}{192\omega\beta C_{top}}\sqrt{\frac{\pi}{e\beta}}\Big[2\sqrt{x^2 + bx + c}\left(-3b^2 + 2bx + 8(c + x^2)\right) \\ &\quad + 3(b^3 - 4bc)\ln\left(b + 2x + 2\sqrt{x^2 + bx + c}\right)\Big]_{x_1}^{x_2} \end{aligned} \tag{20}$$

where b, c, x_1, and x_2 are:

$$b = -2C_{top} \qquad c = 4\beta en_{pud} + C_{top}{}^2$$
$$x_1 = \sqrt{C_{top}{}^2 + 4\beta z_1} \qquad x_2 = \sqrt{C_{top}{}^2 + 4\beta z_2} \tag{21}$$

If z is taking negative values, the change of variable y:

$$y = \sqrt{C_{top}{}^2 - 4\beta z} \tag{22}$$

is applied in equation (19), and the integral can be solved analytically as:

$$\begin{aligned} DEN_{2(z<0)} &= \frac{\mu}{4\omega\beta C_{top}}\sqrt{\frac{\pi}{e\beta}}\int_{y_1}^{y_2}\left(y\sqrt{y^2+by+c}\right)dy \\ &= \frac{\mu}{192\omega\beta C_{top}}\sqrt{\frac{\pi}{e\beta}}\Big[2\sqrt{y^2+by+c}\left(-3b^2+2by+8(c+y^2)\right) \\ &+ 3(b^3-4bc)\ln\left(b+2y+2\sqrt{y^2+by+c}\right)\Big]_{y_1}^{y_2} \end{aligned} \tag{23}$$

where y_1, and y_2 are:

$$y_1 = \sqrt{C_{top}{}^2 - 4\beta z_1} \qquad\qquad y_2 = \sqrt{C_{top}{}^2 - 4\beta z_2} \tag{24}$$

The proposed model has been fitted against measured data of CVD GFETs fabricated at University of Siegen, shown in Figure 3.5, where the fitting parameters are: W = 40 µm, L = 4 µm, t_{OX} = 20 nm, ε_R = 3.9, µ = 500 cm²/V.s, $R_{d/s}$ = 200 Ω, N_f = -20 x 10^{15} cm^{-2}, ђω = 56 meV, and Δ = 150 meV. The model describes the I_{ds} of the measured GFETs with good accuracy.

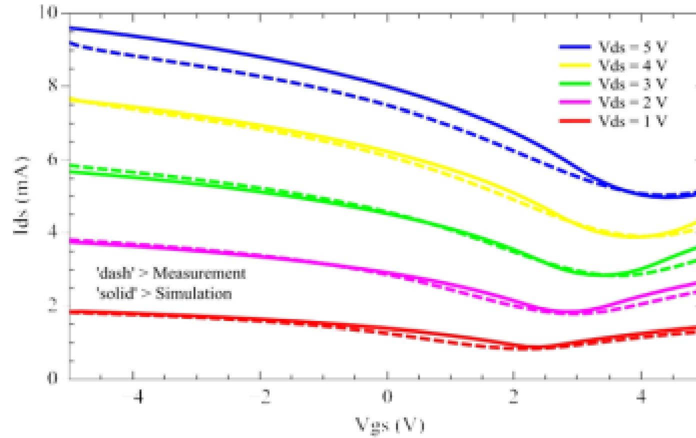


Figure 3.5 I_{ds} (V_{gs}) for selected V_{ds}. Our model proposal (solid) has been fitted to the data (dash) measured from a CVD GFET fabricated in University of Siegen. The device dimensions are: W = 40 µm, L = 4 µm, and t_{OX} = 20 nm

In Figure 3.6a, a comparison between Bordeaux model (dash lines) and our model (solid lines), is performed, where I_{ds} (V_{gs}) for selected V_{ds} is depicted. If V_{ds} is increased from 1 V to 5 V, a distortion at Dirac point starts to appear with Bordeaux model. Both models are fitted to [103] with the following parameters: W = 1 µm, L = 440 nm, t_{OX} = 8.5 nm, ε_R = 3.5, µ = 7000 cm²/V.s, R_{con} = 172 Ω.µm, L_{acc} = 0 µm, N_f = 0 cm^{-2}, ђω = 56 meV, and Δ = 66.8 meV, where GFET devices are fabricated with an exfoliated graphene channel, an h-BN gate dielectric and Au drain/source contacts. In Figure 3.6b, a second comparison is performed. If L is decreased from 2.94 µm to 294 nm, and V_{ds} is increased from 1 V to 5 V, the same type of distortion starts to appear as well. This time,

both models are fitted to [104] with the following parameters: W = 4 µm, L = 294 nm, t_{OX} = 28 nm, ε_R = 3.9, µ = 6800 cm^2/V.s, R_s = 1.2 Ω.µm, R_d = 768 Ω.µm, N_f = 250 x 10^9 cm^{-2}, ℏω = 370 meV, and Δ = 0 eV, where GFET devices are fabricated with an epitaxially grown graphene channel, a SiO_2 dielectric, and Ti/Pt/Au drain/source contacts. As it can be seen, the problem is solved with our model in both cases due to a more accurately calculated solution for the current denominator DEN_2.

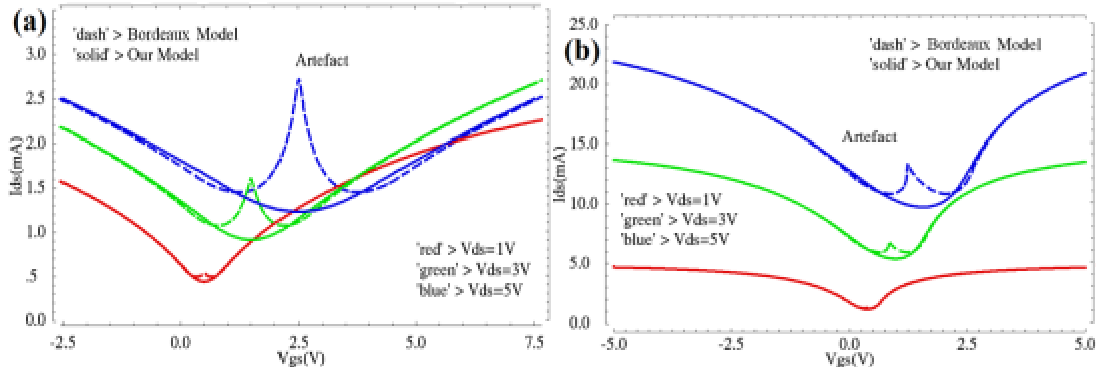


Figure 3.6 GFET I_{ds} (V_{gs}) for selected V_{ds}. A comparison between Bordeaux model (dash-lines) and our model proposal (solid-lines). (a) Fitted to an exfoliated GFET with W = 1 µm, L = 440 nm, and t_{OX} = 8.5 nm. (b) Fitted to an epitaxial GFET with W = 4 µm, L = 294 nm, and t_{OX} = 28 nm.

The proposed GFET compact model has been implemented in Verilog-A language, a standard language which was first conceived to address high-level analog circuit simulations, and nowadays it has been optimized for transistor modeling as well. In order to establish further the benefits of our model, two large-signal circuits have been simulated. A complementary inverter (INV) implemented with two GFETs as shown in Figure 4.1a. In Figure 3.7a, the output voltage (V_{out}) is plotted against the input voltage (V_{in}) for different supply voltages (V_{dd}). A comparison between Bordeaux model and our model is carried out. Both models are fitted to the already presented exfoliated GFET with h-BN back-gate which was the technology that provided better current saturation of the three GFETs analysed. The circuits parameters are $(W/L)_{N-P}$ = 1 µm / 440 nm and t_{ox} = 8.5 nm. At the transition of V_{out} from high voltage to low voltage, the Bordeaux model results in substantial artefacts. These discontinuities disappear in the optimized model presented in this section. Also, a cascode amplifier (CAS) shown in Figure 4.16a has been chosen because it is a potential solution for increasing the current saturation in actual GFETs, this cell is also implemented with two GFETs. The output current (I_{out}) is plotted against V_{out} for different V_{in} in Figure 3.7b, again showing artefact-free characteristics after optimizing the model. The circuit parameters are $(W/L)_{1-2}$ = 1 µm / 440 nm, t_{OX} = 8.5 nm and V_{bias} = 2.5 V.

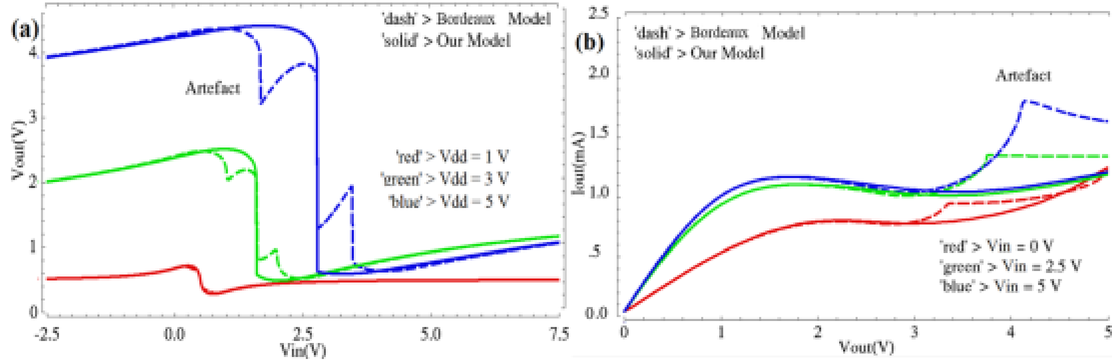


Figure 3.7. Circuit-level comparison between Bordeaux model (dash lines) and our model proposal (solid lines). (a) INV V_{out} (V_{in}) for selected V_{dd}. (b) CAS I_{out} (V_{out}) for selected V_{in} with V_{bias} = 2.5 V. Model fitted to an exfoliated GFET with W = 1 µm, L = 440 nm, and t_{OX} = 8.5 nm.

Going back to our compact I/V model, the definition of intrinsic/extrinsic transconductance g_{mi}/g_m and intrinsic/extrinsic output conductance g_{oi}/g_o are described below in (25). This means that g_m gets degraded with high $R_{d/s}$ and high g_{oi}, while g_o gets improved with high $R_{d/s}$ and high g_{mi} [105]:

$$g_{mi} = \frac{\partial I_{ds}}{\partial V_{gsi}}\bigg|_{V_{dsi=cons.}} \qquad g_{oi} = \frac{1}{R_{ds}} = \frac{\partial I_{ds}}{\partial V_{dsi}}\bigg|_{V_{gsi=cons.}}$$

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} = \frac{g_{mi}}{1 + g_{mi}R_s + g_{oi}(R_s + R_d)} \tag{25}$$

$$g_o = \frac{\partial I_{ds}}{\partial V_{ds}} = \frac{g_{oi}}{1 + g_{mi}R_s + g_{oi}(R_s + R_d)}$$

3.3.3 Capacitance-to-Voltage Model Including Extrinsic Parasitics

With a GFET I-V model (Figure 3.4) is only possible to run large-signal simulations for DC circuits as already introduced briefly. Nevertheless, to be able to simulate large-signal AC/RF circuits a capacitance-to-voltage model (C-V) is a must. There are several alternatives on how to model GFET capacitances for a DD model: in [106] a compact model with a capacitance model proposed by Zebrev in [105] is presented, besides electron and hole currents are treated independently to reflect their slight differences in µ values; in [107], a charge-conservation Wart-Dutton capacitance model is proposed, although a saturation velocity model (17) is not included. As seen in Figure 3.8, the intrinsic voltage-controlled current g_{mi}*V_{gsi}, the intrinsic output resistance R_{ds}, and the extrinsic resistances $R_{d/s}$ conform the already presented I-V model in chapter 3.3.2.

The GFET C-V model is formed by the following components: (1) the intrinsic capacitances C_{gs} and C_{gd} that are function of bias and size based on Thiele [94]:

$$C_{gs} = -\left.\frac{\partial Q_{ch}}{\partial V_{gsi}}\right|_{V_{dsi=cons.}} \qquad C_{gd} = -\left.\frac{\partial Q_{ch}}{\partial V_{dsi}}\right|_{V_{gsi=cons.}} \tag{26}$$

To calculate the capacitances introduced above, the total charge in the channel Q_{ch} can be approximated based on the Bordeaux model [95] as follows:

$$Q_{ch} = \mathrm{W}\int_0^L \left(Q_{net}(x) + en_{pud}\right)dx \approx \frac{\mathrm{W}}{E_{AV}}\left(\int_0^{V_{dsi}} |Q_{net}|dV + en_{pud}V_{dsi}\right) = \frac{\mathrm{W}}{E_{AV}}(NUM_1 + NUM_2) \tag{27}$$

where NUM_1 and NUM_2 are already calculated in equations (8), (13) and (15), and the average electric field within the channel E_{AV} is defined as:

$$E_{AV} \approx \frac{dV}{dx} \approx \frac{V_{dsi}}{L} \tag{28}$$

; (2) the extrinsic gate resistance R_g as a function of size, the intrinsic gate-to-source resistance R_i. At very high frequencies the assumption of instantaneous g_m does not apply, that is why an **R_i parameter** is added to our model to simulate the delay between changing V_{gs} and this affecting to I_{ds} [108]. And the extrinsic capacitances C_{gso}, C_{gdo} and C_{dso} as a function of channel width:

$$R_g = R_{g'} \times \frac{\mathrm{W}}{L} \tag{29}$$

$$C_{gso} = C_{gso'} \times \mathrm{W} \quad C_{gdo} = C_{gdo'} \times W \quad C_{dso} = C_{dso'} \times W$$

; and finally (3) the extrinsic components C_{gsp}, C_{gdp}, C_{dsp}, L_{gb}, L_{db}, and L_{sb} that are constant, which are parasitics caused by pads and bonding wires. The complete GFET compact model is shown in Figure 3.8:

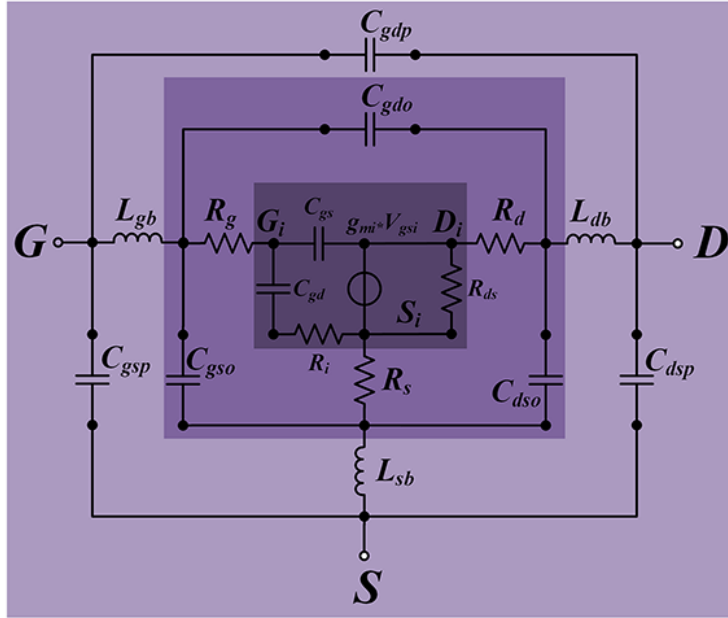


Figure 3.8 GFET model (I/V + C/V) where the intrinsic model is based on our large-signal drift-diffusion model, the extrinsic model is based on lumped components which scale with size, and the test model is based on lumped components that do not scale.

3.4 Fitting GFET Model Parameters to GFET Measurements

In chapter 3.3.2, our I-V compact model has already been fitted to three different GFETs: (1) a CVD GFET with silica top-gate, fabricated in the University of Siegen (Figure 3.5); (2) an GFET epitaxially grown on SiC with silica top-gate, fabricated in Hughes Research Laboratories (HRL) [104]; and (3) an exfoliated GFET with a h-BN back-gate, fabricated in Columbia University [103]. The drawback in (1) is the poor A_v obtained due to high access and contact resistances, in (2) the process is not CMOS friendly, and in (3) exfoliated graphene is not a scalable technology besides it is a back-gate GFET which precludes its use for circuit design with multiple transistors. That is why in this chapter we are concentrating in fitting scalable, CMOS friendly, low contact resistance top-gate GFETs: (1) a CVD GFET with alumina top-gates fabricated in Technical University of Milan [85], and (2) a self-aligned CVD GFET with alumina top-gates fabricated in Nanjing Electronic Device Institute [69].

3.4.1 CVD GFET based on Alumina Top-Gates

Our I-V model is fitted to the measurements of a CVD GFET with alumina top-gate fabricated in [85]. The model parameters values are: W = 10 µm, L = 2 µm, t_{OX} = 4 nm, ε_R = 6.24, µ = 700 cm^2/V.s, R_{con} = 1000 Ω.µm, R_{acc} = 0 Ω, L_d = 250 nm, N_f = -50 x 10^{15} cm^{-2}, ħω = 56 meV, and Δ = 100 meV. As seen in Figure 3.9, the similarities between

simulation and measurement results are quite good. The expected typical ambipolar I_{ds}/W (V_{gs}), where the Dirac point increases with V_{ds}, is observed.

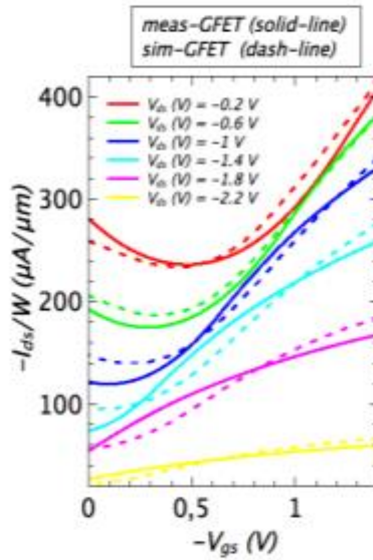


Figure 3.9 I_{ds}/W (V_{gs}) for selected V_{ds}. Parameter model fitting between a measured CVD GFET with alumina top-gate (solid-line) and our simulated GFET model (dash-line). The GFET dimensions are: W = 10 µm, L = 2 µm, t_{OX} = 4 nm.

In Figure 3.10, C_{gs} (V_{gs}) and C_{gd} (V_{gs}) are simulated for specific V_{ds} values. In both cases, minimum capacitance values are observed at Dirac point. For C_{gs} the minimum is wider along Dirac point compared to C_{gd}, besides C_{gs} values are twice the C_{gd} values.

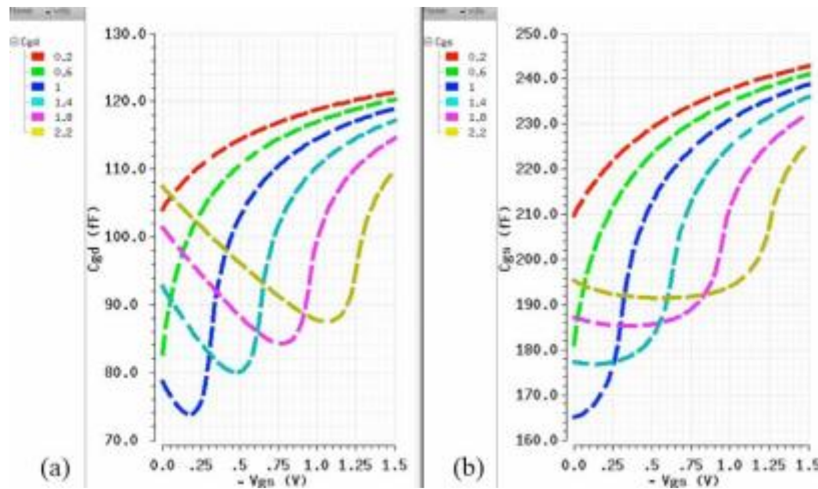


Figure 3.10 Simulated GFET capacitances against voltage. (a) C_{gd} (V_{gs}) for selected V_{ds}. (b) C_{gs} (V_{gs}) for selected V_{ds}. Model fitted to a measured CVD GFET with alumina top-gate and W = 10 µm, L = 2 µm, t_{OX} = 4 nm.

3.4.2 Self-aligned CVD GFET based on Alumina Top-Gates

A simulated GFET with model parameters fitted against **DC and RF measurements** of a self-aligned CVD GFET fabricated by Nanjing Electronic Device Institute [69] is performed. In Figure 3.11a, I_{ds}/W (V_{ds}) for selected V_{gs} is fitted against measurement results (not shown) with the following values are: W = 2 x 10 µm, L = 60 nm, t_{OX} = 10 nm, ε_R = 5.6, µ = 500 cm^2/Vs, $R_d = R_s$ = 52.5 Ω.µm, N_f = -30 x 10^{15} cm^{-2}, ħω = 56 meV, and Δ = 300 meV. The minimum g_o/W achieved is 900 µS/µm which is a high value compared to the record ones shown in Table 3.3.

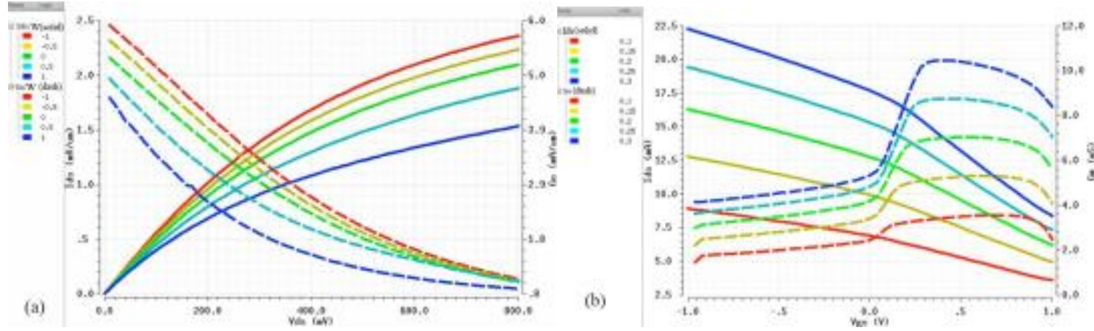


Figure 3.11 GFET DC simulations (a) I_{ds}/W (V_{ds}) (solid-line) and g_o/W (V_{ds}) (dash-line) for selected V_{gs}. (b) I_{ds} (V_{gs}) and g_m (V_{gs}) for selected V_{ds}. Model fitted to the measurements of a self-aligned CVD GFET with W = 2 x 10 µm, L = 60 nm, t_{OX} = 10 nm.

In Figure 3.11b, I_{ds} (V_{gs}) and g_m (V_{gs}) for selected V_{ds} is fitted against measurements (not shown) with the same values as in Figure 3.11 but Δ = 170 meV. The maximum g_m/W achieved is 590 µS/µm which is a quite low value compared to the record values shown in Table 3.2. We rely on the embedded and de-embedded f_{max} and f_t values measured in [69] to fit the external components (R_g, R_i, C_{gsp}, C_{dsp}) of our GFET test model shown in Figure 3.8. f_t is defined as the cut-off frequency, that is the frequency at which short-circuit current gain h_{21} = 1 (0 dB). f_{max} is defined as the maximum frequency of oscillation, that is the frequency at which Mason's unilateral power gain U = 1 (0 dB) [109], the open-circuit voltage gain A_v can be defined through Z and S parameters for mid and high frequencies respectively:

$$h_{21} = \frac{-2S_{21}}{(1-S_{11})(1+S_{22})+S_{12}S_{21}}$$

$$U = \frac{|S_{21}/S_{12}-1|^2}{2k|S_{21}/S_{12}|-2Re(S_{21}/S_{12})} \quad (30)$$

$$A_v = \frac{Z_{21}}{Z_{11}} = \frac{2S_{21}}{(1+S_{11})(1-S_{22})+S_{12}S_{21}}$$

where S_{21} is the gain, S_{11} is the input return loss, S_{12} is isolation, S_{22} is the output return loss, and k is the Rollett stability factor. The simulator calculates the S parameters of our modeled GFET, then h_{21} and U, and finally f_t and f_{max}, where the simulation setup is shown in Figure 3.12:

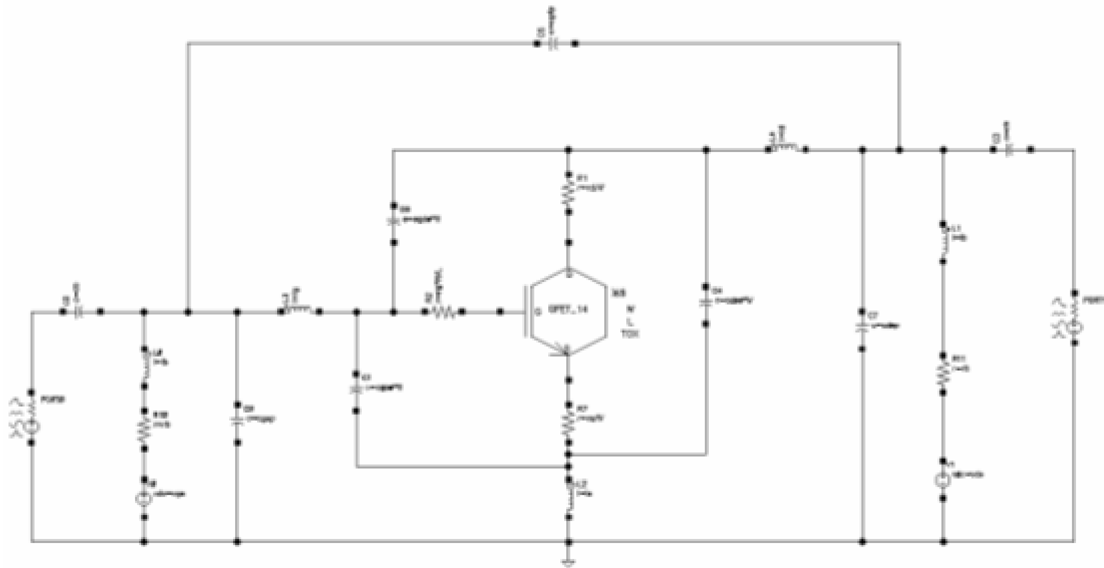


Figure 3.12 GFET S-parameters simulation setup.

As seen in Figure 3.13a, the de-embedded f_t value is 255 GHz at V_{gs} = 0.6 V and V_{ds} = 0.35 V. Assuming as a start the parameters from Figure 3.11, we start fitting the embedded f_t parameter to 70 GHz with C_{gsp} = C_{dsp} = 19 fF, which are the parasitic values due to the extrinsic capacitances and the probing pads for taking measurements.

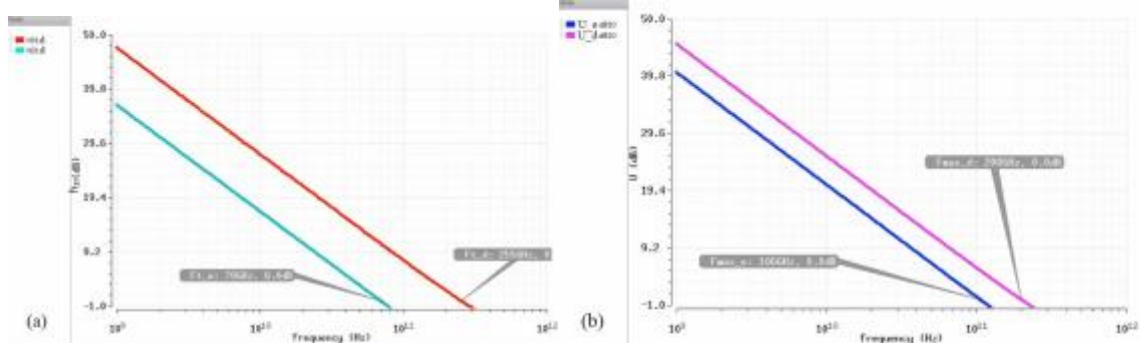


Figure 3.13 f_T and f_{MAX} simulations. (a) Embedded (light blue) h_{21e} (f) and de-embedded (red) h_{21d} (f). (b) Embedded (blue) U_e (f) and de-embedded (violet) U_d (f). Model fitted to the measurements of a self-aligned CVD GFET with W = 2 x 10 µm, L = 60 nm, t_{OX} = 10 nm.

Assuming the fitted parameters in Figure 3.13b, the de-embedded f_{max} is 200 GHz at V_{gs} = 0.6 V and V_{ds} = 0.35 V if we set R_i to 23.7 Ω. Then we fit the embedded f_T value to 106 GHz with R_g = 124 mΩ.

3.5 GFET Maximum Frequency of Oscillation

From a RF circuit point of view, maximizing $A_v = g_m/g_o$ is necessary but not sufficient:

$$A_v = \frac{g_m}{g_o} = \frac{g_{mi}}{g_{oi}} \tag{31}$$

For RF transconductors circuits, f_t should also be maximized as much as possible, so this implies maximizing g_m and minimizing the rest of parameters [110]:

$$f_t \approx \frac{\frac{g_{mi}}{2\pi(C_{gs}+C_{gd})}}{1+g_{oi}(R_s+R_d)+\left(\frac{g_{mi}C_{gd}}{C_{gs}+C_{gd}}\right)(R_s+R_d)} \tag{32}$$

To represent a more realistic f_t, we are assuming the following parameter values: R_i = 23.7 Ω, $R_{g'}$ = 124 mΩ, $C_{gso'}$ = 198 pF/m and $C_{gdo'}$ = 151 pF/m (values extracted for a GFET in [111]). As seen in Figure 3.14a, the f_T can be maximized to 231 GHz at V_{gs} = 1 V and V_{ds} = 1.2 V, this value is lower than the 255 GHz predicted in Figure 3.13a because is including $C_{gso'}$ and $C_{gso'}$. This value is achieved thanks to the maximum g_m value achieved at V_{gs} = 1 V and V_{ds} = 1.2 V. Two local minima are observed at V_{gs} = 1.5 V, 2 V due the collapse of g_m at the Dirac point.

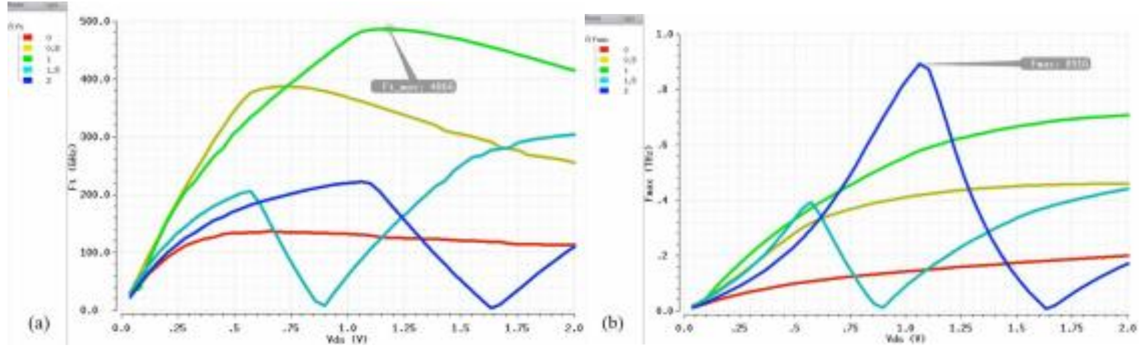


Figure 3.14 GFET FoMs optimization (a) f_t (V_{ds}) for different V_{gs}. (b) f_{max} (V_{ds}) for different V_{gs}. The compact-model parameters are fitted to the measurements of a self-aligned CVD GFET with W = 2 x 10 µm, L = 60 nm, and t_{OX} = 10 nm.

For RF amplifying circuits, the FoM to maximize is f_{max}, which implies maximizing g_m and minimizing the rest of parameters. Compared to f_t there are two extra parameters to minimize which are R_g, and R_i [110]:

$$f_{max} \approx \frac{\frac{g_{mi}}{4\pi C_{gs}}}{\sqrt{g_{oi}(R_i+R_s+R_g)+\frac{g_{mi}}{C_{gs}+C_{gd}}R_g C_{gd}}} \tag{33}$$

As seen in Figure 3.14b, the f_{max} can be maximized to 453 GHz at V_{gs} = 2 V and V_{ds} = 1.1 V. This is better than the record 420 GHz predicted for CMOS in [46]. Unfortunately, the V_{ds} voltage range above 400 GHz is only of 125 mV. Two local minima are observed

at V_{gs} = 1.5 V, 2 V due the collapse of g_m at the Dirac point. In Figure 3.15a, we are calculating U (f) for W/L = 20 µm/15 nm, and several f_{max} values are shown for different bias voltages.

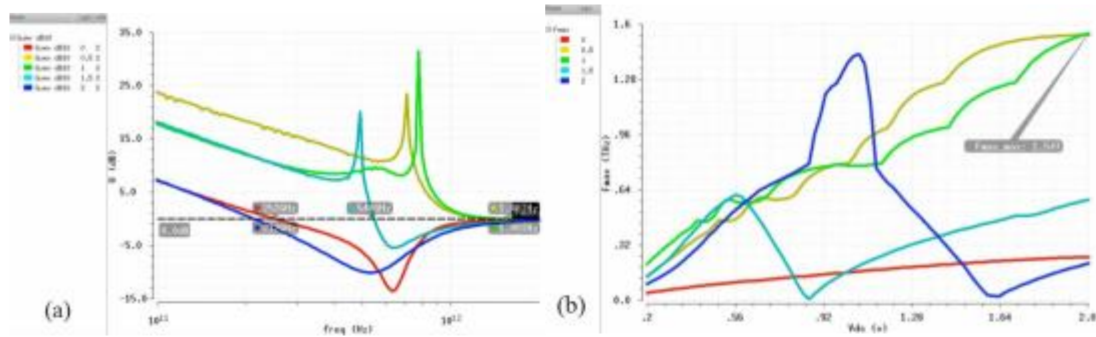


Figure 3.15 GFET FoMs prospects (a) U(f) for different V_{gs} and V_{ds} = 2 V. (b) f_{MAX} (V_{ds}) for different V_{gs}. The compact-model parameters are fitted to the measurements of a self-aligned CVD GFET with W = 2 x 10 µm, L = 15 nm, and t_{OX} = 10 nm.

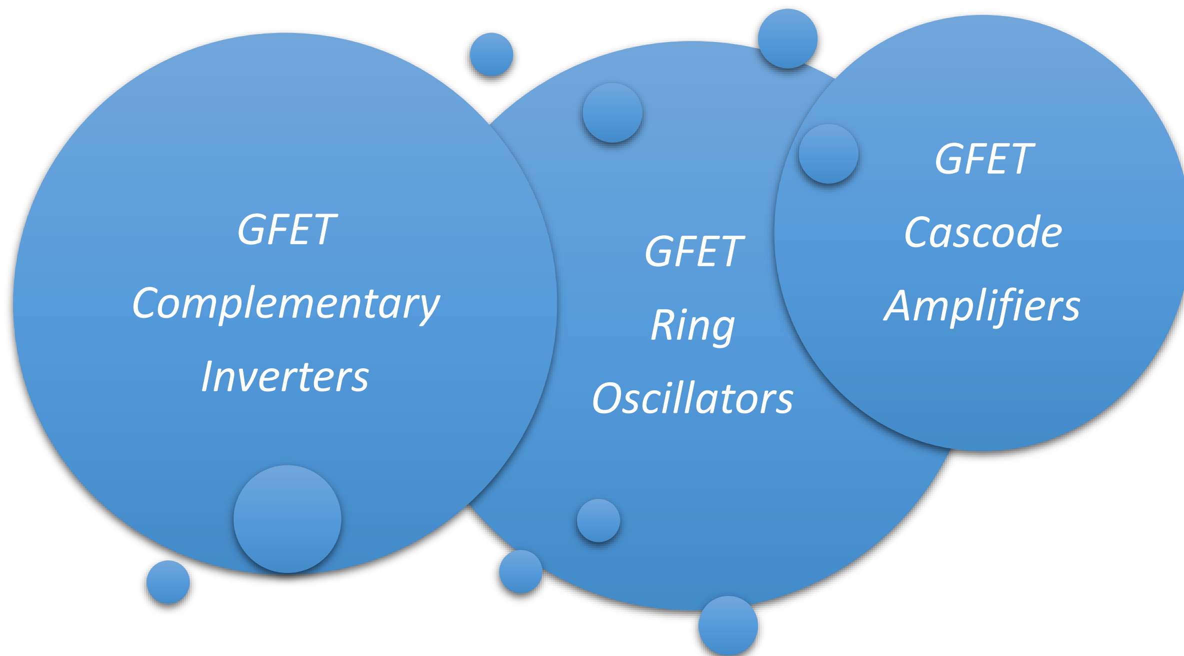
In Figure 3.15b, we are calculating f_{max} where a value of 1.54 THz should be achievable. Nevertheless, let's keep in mind that f_{MAX} does **not** represent a realistic scenario for circuit design, because of this GFET circuits will be simulated to get more reliable results.

3.6 Conclusions

Graphene has been introduced and its extraordinary electronic properties explained. Consequently, it is proposed as a plausible channel for RF FETs thanks to its high carrier µ values (2000 - 80000 cm^2/V.s) and one-atom thickness which should imply high g_m which is a must for achieving high f_t, and excellent electrostatic control which is needed for overcoming short-channel effects when scaling. GFETs (among other graphene transistors) are chosen because FETs are scalable-friendly transistor architectures, and scaling capacitances is a must to conquer high frequencies. It is shown that rather high g_m (1.2 - 2.9 mS/µm) are achievable for GFETs. We choose the CVD technique for their fabrication because it is compatible with CMOS technology, the drawback is that CVD GFET g_m figures (< 1 mS/µm) need improvement. An optimization of metal/graphene contact and gate self-alignment to reduce $R_{d/s}$, an increase in CVD graphene quality to increase µ, and smoother (higher ђω) substrates contribute to increase g_m. Although all these measures are not enough, we suspect that the key factor lays on the optimization of the interface between graphene and the gate dielectric to minimize the undesired C_q effect and improve its electrostatic control. Achieving high f_{max} only with high g_m is not enough either, low g_o is required as well to get A_v > 1. Monolayer GFETs face an enormous challenge, namely its weak current saturation (high g_o) due to graphene's lack of bandgap. Nevertheless, extremely low g_o (0 – 2 µS/µm) have been measured in GFETs. NDR has been predicted by GFET models and measured in GFET devices, this is a phenomenon that should be explored further to fully understand the mechanisms behind it and being able to increase A_v. Another promising alternative to reduce g_o could be the use of bilayer graphene: artificially stacked bilayer

CVD graphene have shown improved A_v figures **(Conference E & Journal IV)**. Compact models for transistors are necessary tools for circuit simulators. We choose a drift-diffusion approach due to its simplicity and acceptable accuracy when parameterizing measurements even for GFETs with $L < 100$ nm. An optimized model for GFETs is proposed where a new solution for the I-V transfer of a GFET compact-model is provided **(Journal I & II)**. The exact analytical calculation of the current denominator ensures improved accuracy around the Dirac point, thus avoiding undesired distortions when designing large-signal circuits. This allows the scaling of the model and its circuit parameters such as V_{dd}, L, t_{ox} and μ. The model has been implemented in Verilog-A and its parameters fitted to the measurements of experimental GFETs. The improved model has been carefully characterized through several simulations at device and circuit level, proving its robustness for different design parameters. Besides, a C-V model for GFET plus a small-signal model for extrinsic parasitics is presented and successfully fitted against the fastest CVD GFET technology fabricated nowadays to our knowledge. Furthermore, f_{max} is calculated by simulating S-parameters and a bias optimization to maximize f_{max} is performed where a value of 454 GHz is achieved for W/L = 20 µm / 60 nm and t_{OX} = 10 nm. Besides a f_{max} scaling prospect is derived to assess their real potential for future nanoTRx. For a GFET with W/L = 20 µm / 15 nm and t_{OX} = 10 nm, f_{max} = 1.54 THz values should be achievable upon our simulations.

4 Nanocircuits: GFET Circuits



RF circuits based on GFET devices implementing transconductors or diodes where only high f_T is required have already been demonstrated in research literature: 17 GHz frequency multipliers [112], 90 GHz (data rate = 4 Gbps) Rx and Tx [113], 200 GHz frequency mixers [114], 210 GHz detectors [115], and 600 GHz integrated antenna detectors [116]. The progressive improvement of f_{max} in GFETs has paved the way for active circuits where voltage amplification ($A_v > 1$) is a must: 4.3 GHz (data rate = 20 Mbps) Rx [117], 14.3 GHz LNAs [118], 2.5 GHz PAs [119], and 4.3 GHz ring oscillators [85]. In mature IC technologies, the interaction among devices and circuits is mainly bottom-up; only devices provide performance constraints and hence design guidelines to circuits. The situation is quite different in emerging technologies like in graphene, which benefit upfront from device-circuit co-design techniques. In them, there is a concurrent top-down and bottom-up interaction from circuit design to device model and vice-versa. As already seen, most promising applications for GFET devices are small-signal (AC/RF) circuits, but large-signal/non-linear circuits deserve thorough exploration as well. It is fundamental to provide a design-oriented characterization of basic multi-transistor circuit cells through the simulation of GFET large-signal compact models, as an intermediate step ultimately aiming full GFET-based ICs. The essence of this chapter is to explore such type of circuits based on GFETs, namely: complementary inverters (INV), ring oscillators (RO), and cascode amplifiers (CAS). Taking advantage of the ambipolar behaviour of GFET $I_{ds}(V_{gs})$, an INV is designed with two GFETs and simulated to explore its large-signal behaviour for static and transient conditions **(Conference B)**. Furthermore, a RO based on three GFET INVs is designed and simulated to explore its large-signal behaviour for dynamic conditions and future circuit scaling **(Conference B)**. Finally, a CAS based on two GFETs is designed, simulated and fabricated to explore its large-signal behaviour for static conditions with the purpose of improving the voltage gain impaired by the intrinsic weak current saturation observed in monolayer GFETs **(Conference A)**.

4.1 GFET Complementary Inverters

GFET INVs, with back-gates [120], with top-gates [121], with side-gates for electrostatic doping [122], with top-gate and local back-gates for electrostatic doping [123], and cascaded inverters [124] have already been physically implemented. This chapter will focus on INVs based on top-gates monolayer GFETs. The INV can be regarded from a digital perspective as a delay logic gate, or from an analog point of view as a large-signal/non-linear circuit. A schematic of an INV implemented with two GFETS is shown in Figure 4.1a, and its correspondent cross-section layout in Figure 4.1b, where the depicted back-gate will not be used for our designs.

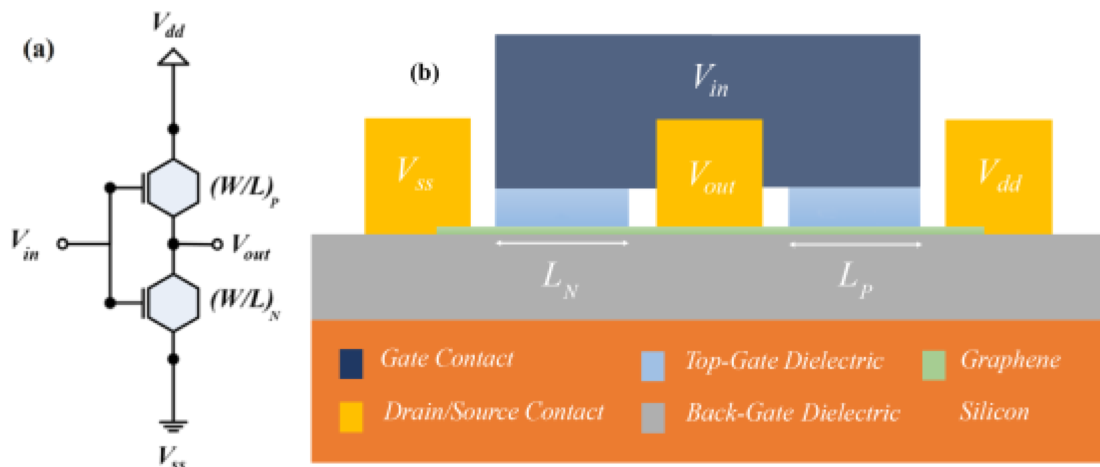


Figure 4.1. GFET INV. (a) Circuit schematic. (b) Cross-section layout.

As it can be seen, the $GFET_P$ source and the $GFET_N$ drain are merged to minimize extrinsic contact resistance between them. $L_{N/P}$ are the channel lengths, and $W_{N/P}$ are the channel widths. The voltage inversion is achieved thanks to the distinctive ambipolar characteristic of graphene and the broken symmetry (Dirac point split) induced by the channel potential, so that no additional electrostatic doping is considered here [121]. In other words, the Dirac point voltages of $GFET_N$ and $GFET_P$ have different values. An INV design exploration comparison between our compact model introduced in chapter 3 and a model based on a virtual-source approach [125], both fitted to exfoliated GFETs, is carried out. Besides a new simulation/measurement benchmark for INVs based on a CVD GFET, and a new design exploration for INVs based on self-aligned CVD GFETs are performed.

4.1.1 GFET Compact Models Benchmark based on Exfoliated GFETs

A device-level comparison between our optimized compact model based on drift-diffusion transport and another compact model based on the virtual-source approach presented in [125] by the Massachusetts Institute of Technology (MIT), both fitted to an h-BN back-gate exfoliated GFET developed in [103] by Columbia University, is carried out **(Conference B)**. The correspondent values of our model parameters are the ones already used in chapter 3.3: W = 1 µm, L = 440 nm, t_{OX} = 8.5 nm, µ = 7000

$cm^2/V.s$, R_{con} = 172 Ω.µm, ђω = 56 meV, and Δ = 66.8 meV. A Verilog-A script of the MIT compact model has been uploaded on nanoHUB for free access to the research community. The fitted parameters values are: W = 1 µm, L = 440 nm, C_{top} = 3.6 x 10^{-7} F/cm^2, µ = 7 x 10^3 $cm^2/V.s$, R_{elec} = R_{hole} = 172 Ω.µm, Q_{dis} = 5 x 10^{-7} C/cm^2, v_{x0} = 7 x 10^6 cm/s, ΔV = 0 V, V_{min_0} = 0 V, ζ = 82.5 x 10^{-3}, β = 1.8, n = 2, and α = 6 where R_{elec} is the electron-branch resistance, R_{hole} is the hole-branch resistance, Q_{dis} is the disorder induced charge, v_{x0} is the virtual-source injection velocity, ΔV is the shift in Dirac voltage due to traps, $V_{min,0}$ is the Dirac point voltage, ζ is the energy transfer factor, β is a saturation parameter, n is a non-ideality factor, and α is the shift in threshold voltage.

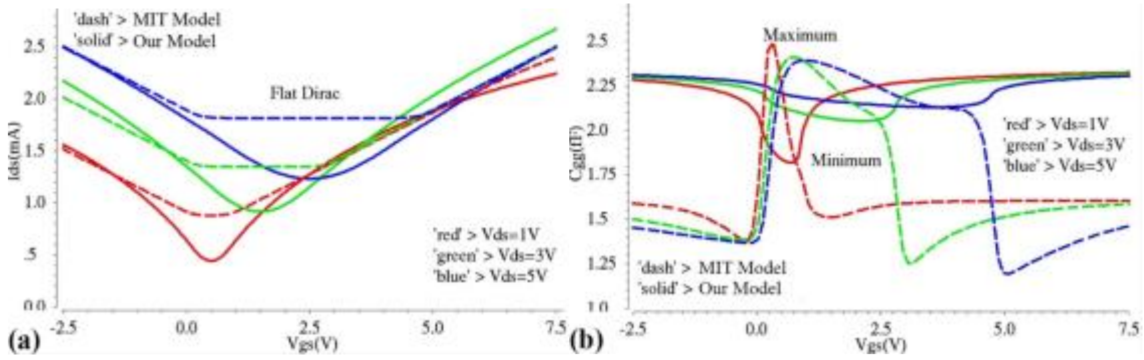


Figure 4.2. GFET comparison between a drift-diffusion compact model (solid) and a virtual-source compact model (dash), where the exfoliated GFET dimensions are W = 1 µm, L = 440 nm, and t_{OX} = 8.5 nm. (a) $I_{ds}(V_{gs})$ for selected V_{ds}. (b) C_{gg} (V_{gs}) for selected V_{ds}.

In Figure 4.2a, the expected typical ambipolar I_{ds} (V_{gs}), where the Dirac voltage increases with V_{ds}, is observed for both models. The main difference among them is at the already mentioned Dirac region, which is flatten for the virtual-source model, generating an artificial distortion for the corresponding g_m; at this specific case, the drift-diffusion model fits better the experimental measurement results. In Figure 4.2b, the top-gate capacitance defined as C_{gg}:

$$C_{gg} = C_{gs} + C_{gd} \tag{34}$$

is calculated against V_{gs} for different V_{ds} values. A clear minimum at Dirac point, which widens while V_{ds} increases, is observed for the drift-diffusion model. On the contrary, a clear maximum at Dirac point, that widens while V_{ds} increases, is observed for the virtual-source model. We suspect this striking difference is due to the different method of calculating the capacitances in both models. Our model is using the Meyer capacitance model as explained in chapter 3.3.3, and the MIT model is using the Wart-Dutton capacitance model, which is more complex but ensures charge conservation [125]. A thoughtful benchmark against experimental non-linear capacitance measurements is needed to confirm which model approaches better reality. This is specially challenging due to the technical difficulties faced for measuring GFET capacitances against voltage (chapter 3.4).

4.1.2 INV Simulation Benchmark based on Exfoliated GFETs

In Figure 4.3a, the INV output voltage (V_{out}) is plotted against the input voltage (V_{in}) for different supply voltages (V_{dd}). The V_{out} transition from high voltage V_{dd} to low voltage V_{ss} and vice-versa is much steeper when our model is used. We observe a discontinuity at the end of the slope for V_{dd} > 1V. For the MIT model, the slope is more realistic (finite gain), although we observe a small bump at the middle of the curve that might be related with the distortion generated by the flattened region at the Dirac point. The GFET dimensions are $(W/L)_{N\text{-}P}$ = 1 µm / 440 nm and t_{OX} = 8.5 nm.

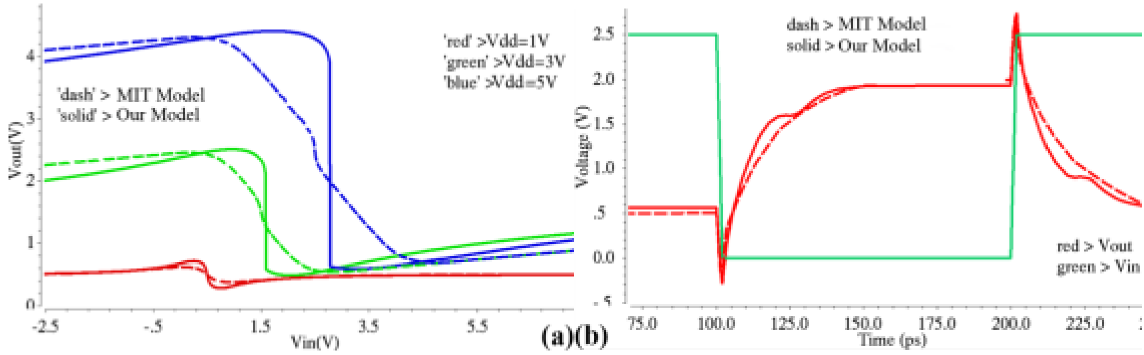


Figure 4.3. GFET INV comparison between a drift-diffusion compact model (solid) and a virtual-source compact model (dash) with $(W/L)_{N\text{-}P}$ = 1 µm / 440 nm, t_{OX} = 8.5 nm, f_{CLK} = 5 GHz, and V_{dd} = 2.5 V as circuit parameters. (a) V_{out} (V_{in}) for selected V_{dd}. (b) V_{out} (t) and V_{in} (t) transient simulations.

In Figure 4.3b, V_{out} and V_{in} transient simulations are shown. Both compact model V_{out} waveforms look rather alike, where our model shows a double-bump in the transition from V_{dd} to V_{ss} and vice-versa, which is not captured by the virtual-source model. The circuit parameters used are: GFETs aspect-ratio $(W/L)_{N\text{-}P}$ = 1 µm / 440 nm, t_{OX} = 8.5 nm, input clock-frequency f_{CLK} = 5 GHz, and supply voltage V_{dd} = 2.5 V. Input voltage dynamic range (ΔV_{in}) is 2.5 V and output voltage dynamic range (ΔV_{out}) is smaller 1.3 V as expected. This test simulation is not assuming a load at the INV output, therefore both frequency and voltage achieved ranges are best case figures.

4.1.3 INV Simulation against Measurement Benchmark based on CVD GFETs

In Figure 4.4, a fitting of V_{out} (V_{in}) transfer **at circuit level** between our simulated INV and a measured INV fabricated with CVD GFETs based on alumina top-gates [85] is carried out. The circuit parameters are: W = 5 µm, L = 800 nm, t_{OX} = 4 nm, ε_R = 6.24, µ = 600 $cm^2/V.s$, $R_{d/s}$ = 15 Ω, N_f = -5 x 10^{15} cm^{-2}, $\hbar\omega$ = 56 meV, Δ_N = 150 meV, and Δ_P = 200 meV. As it is shown the fitting is very good, and the maximum A_v achieved is -6.

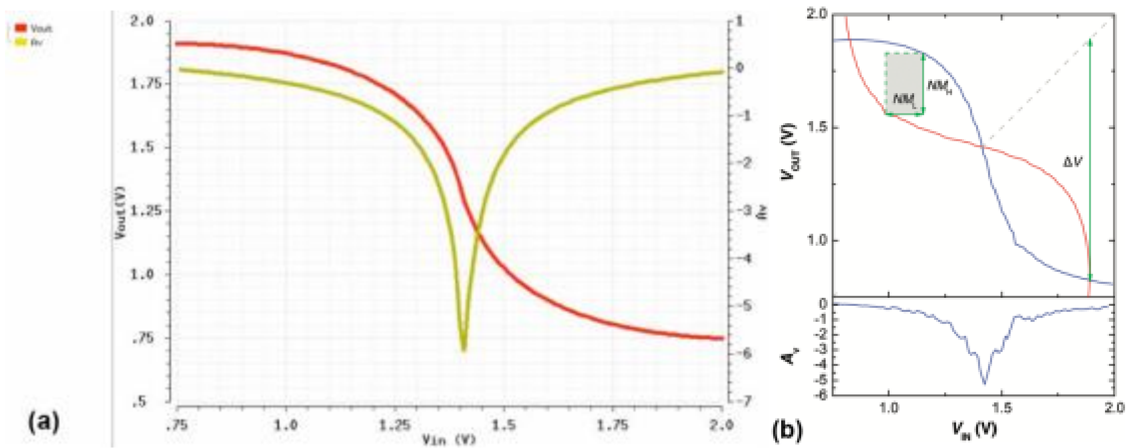


Figure 4.4. GFET INV V_{out} (V_{in}) and A_v (V_{in}). (a) Simulated INV with model parameters fitted to (b) Measured INV fabricated with CVD GFETs, edited from [85]. *The circuit parameters are $(W/L)_{N-P}$ = 5 µm / 800 nm, t_{OX} = 4 nm and V_{dd} = 2.5 V.*

In Figure 4.5, V_{out} and V_{in} transient simulations are shown. The circuit parameters are the same as above with a f_{CLK} = 1.7 GHz, and a ΔV_{out} = 1 V. ΔV_{out} is defined as the difference between the maximum and minimum V_{out} stabilized values, this is to ensure a minimum noise margin (NM) as seen in Figure 4.4b.

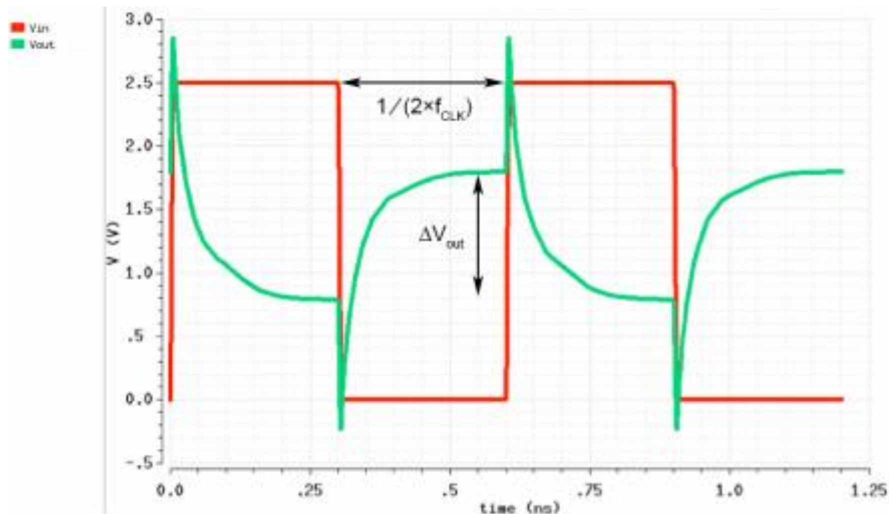


Figure 4.5 GFET INV V_{out} (t) and V_{in} (t) transient simulations. The circuit parameters are: $(W/L)_{N-P}$ = 5 µm / 800 nm, t_{OX} = 4 nm, f_{CLK} = 1.7 GHz, and V_{dd} = 2.5 V.

The simulated INV is loaded with another INV to represent a more realistic situation as it is shown by the circuit schematic from Figure 4.6.

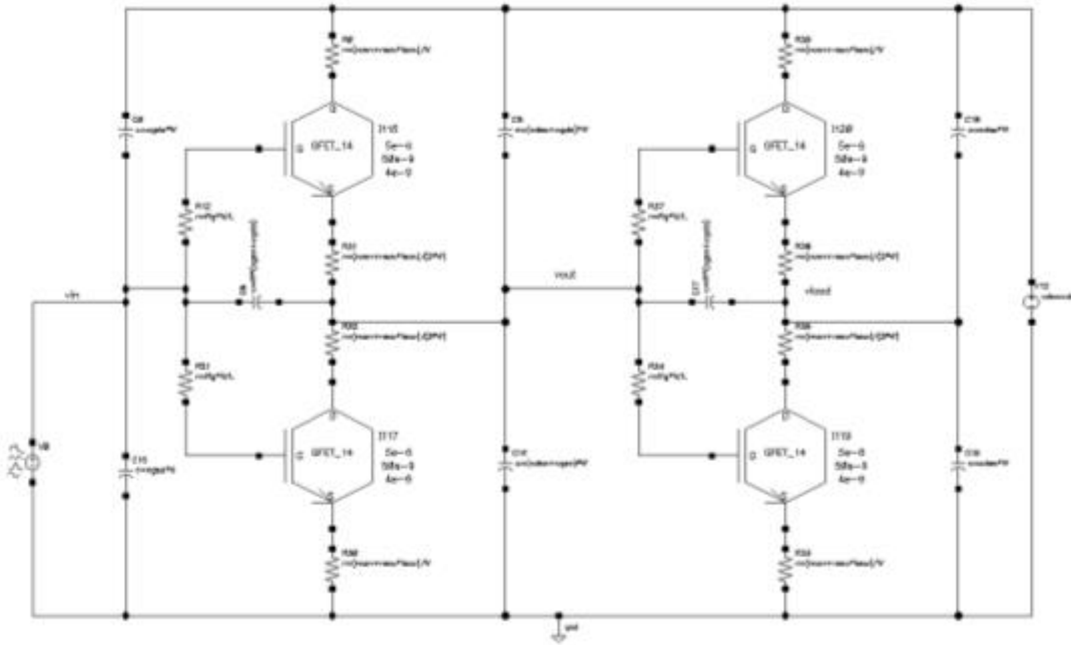


Figure 4.6 Two cascaded INVs schematic for transient simulations

Table 4.1 shows the maximum f_{CLK} and ΔV_{out} (V) achieved for different Ls. As expected the maximum f_{CLK} achieved is increasing while L is decreasing. The extrinsic parameters $R_{g'}$ = 1.22 and $C_{gso'}$ = $C_{gdo'}$ = $C_{dso'}$ = 100 pF taken from **(Conference B)** are starting to reduce the f_{CLK} (from 40 to 28.6 GHz) for L = 50 nm. It is demonstrated how important are the extrinsic parasitics at such high frequencies.

<table>
<tr><th colspan="2"></th><th>f_{CLK} (GHz)</th><th>ΔV_{out} (V)</th><th>$R_{g'}$ (Ω)</th><th>$C_{gso'}$ (pF/m)</th><th>$C_{gdo'}$ (pF/m)</th><th>$C_{dso'}$ (pF/m)</th></tr>
<tr><td colspan="2">L = 800 nm</td><td>1.7</td><td>1</td><td rowspan="5">0</td><td rowspan="6">0</td><td rowspan="7">0</td><td rowspan="8">0</td></tr>
<tr><td colspan="2">L = 400 nm</td><td>4</td><td>1.1</td></tr>
<tr><td colspan="2">L = 200 nm</td><td>10</td><td>1.2</td></tr>
<tr><td colspan="2">L = 100 nm</td><td>16.7</td><td>1.4</td></tr>
<tr><td rowspan="5">L = 50 nm</td><td>red</td><td>40</td><td rowspan="5">1.6</td></tr>
<tr><td>yellow</td><td>36.4</td><td rowspan="4">1.22</td></tr>
<tr><td>blue light</td><td>33.3</td><td rowspan="3">100</td></tr>
<tr><td>blue</td><td>30.8</td><td rowspan="2">100</td></tr>
<tr><td>violet</td><td>**28.6**</td><td>100</td></tr>
</table>

Table 4.1 GFET INV f_{CLK} and ΔV_{out} (V) achieved for different L_{N-P} = L. The circuit parameters are fitted to the measurements of a fabricated INV based on CVD GFETs with the following values: W_{N-P} = 5 µm, t_{OX} = 4 nm, and V_{dd} = 2.5 V.

V_{out} and V_{in} transient simulations are shown in Figure 4.7. The circuit parameters are: W_{N-P} = 5 µm, L_{N-P} = 50 nm, t_{OX} = 4 nm, f_{CLK} = 40 GHz, V_{dd} = 2.5 V, and different combinations of $R_{g'}$, $C_{gso'}$, $C_{gdo'}$, and $C_{dso'}$ values.

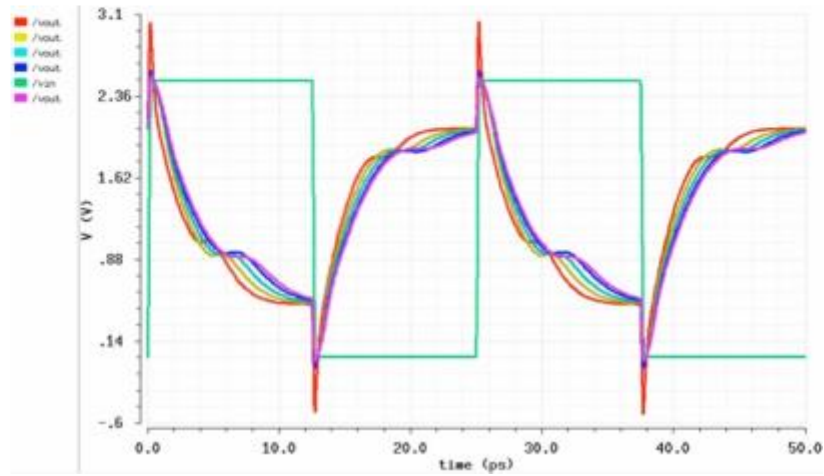


Figure 4.7 GFET INV V_{out} (t) and V_{in} (t) transient simulations. The circuit parameters are: $(W/L)_{N\text{-}P}$ = 5 µm / 50 nm, t_{OX} = 4 nm, f_{CLK} = 40 GHz, and V_{dd} = 2.5 V.

As more parasitics are added the rising/falling slopes are getting slower so a lower f_{CLK} is chosen to give more time for V_{out} to settle down.

4.1.4 INV Design Exploration based on Self-Aligned CVD GFETs

The main difference with the previous section is that the fitted GFET is more than an order of magnitude smaller which implies smaller overall capacitance, and the drain/source contacts are self-aligned which implies lower contact resistance, both characteristics are a must if we want to reach out the 100 GHz range. In Figure 4.8a, a INV simulation of V_{out} (V_{in}) with our model fitted to a self-aligned CVD GFETs based on alumina top-gates [69] is carried out. The model parameters used are: W = 2 x 10 µm, L = 60 nm, t_{OX} = 10 nm, ε_R = 5.6, µ = 500 cm^2/V.s, R_{con} = 52.5 Ω.µm, ħω = 56 meV, and Δ = 170 meV. The maximum voltage gain A_v achieved is -3.5.

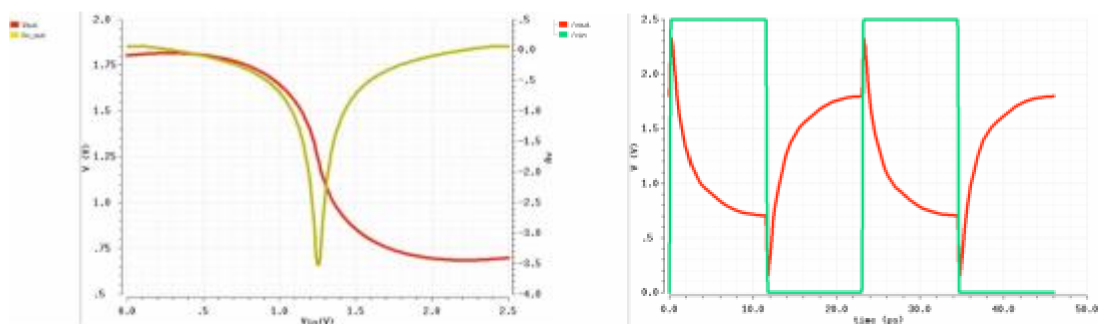


Figure 4.8 GFET INV DC and transient simulations. (a) V_{out} (V_{in}) and A_{v_out} (V_{in}). (b) V_{out} (t) and V_{in} (t) transient simulations. The circuit parameters are fitted to the measurements of a fabricated self-aligned CVD GFET with the following values: $(W/L)_{N\text{-}P}$ = 2 x 10 µm, t_{OX} = 10 nm, and V_{dd} = 2.5 V.

In Figure 4.8, V_{out} and V_{in} transients are shown, where the circuit parameters are the same as above and a f_{CLK} = 44.4 GHz and a ΔV_{out} = 1.4 V are achieved. Table 4.2 shows the maximum f_{CLK} and ΔV_{out} (V) achieved for different Ls. As expected the maximum f_{CLK} achieved is increasing while L is decreasing, and it is even able to exceed 100 GHz for L = 15 nm with $R_{g'}$ = 124 mΩ, and $C_{gso'}$ = $C_{gdo'}$ = 0. Nevertheless if we are assuming more realistic values for extrinsic capacitances as the ones extracted in [111] $C_{gso'}$ = 198 pF/m and $C_{gdo'}$ = 151 pF/m, the reduction in f_{CLK} is huge from 111.2 to 36.4 GHz. This means that all the benefit achieved from reducing L is getting killed by parasitics.

	f_{CLK} (GHz)	ΔV_{out} (V)	$C_{gso'}$ (pF/m)	$C_{gdo'}$ (pF/m)
L = 60 nm	44.4	1.4	0	0
	25	1.1	198	151
L = 30 nm	80	1.4	0	0
	30.8	1.4	198	151
L = 15 nm	133.3	1.7	0	0
	36.4	1.7	198	151

Table 4.2 Self-aligned CVD GFET INV maximum f_{CLK} and ΔV_{in} (V) achieved for different channel lengths L_P = L_N = L. The circuit main parameters are fitted to the measurements of a fabricated self-aligned CVD GFET with the following values: W_{N-P} = 2 x 10 µm, t_{OX} = 10 nm, R_g = 124 mΩ and V_{dd} = 2.5 V.

4.2 GFET Ring-Oscillators

GFET ROs based on GFET INVs are perfectly suited to characterize future graphene fabrication processes, since they are able to assess the gate delay of the technology under characterization through the measurement of the RO oscillation frequency f_{OSC}, besides they can be used as voltage-controlled oscillators to generate different frequency carriers. Additionally, this results in a simple measurement, thereby reducing the cost of the RF equipment to be used during subsequent experimental tests. The outcome of this chapter is three-fold: (1) a RO simulation benchmark between our proposed model against the MIT virtual-source model based on exfoliated GFETs with hBN back-gate, (2) a RO simulation against measurement benchmark based on CVD GFETs with alumina top-gates, and (3) a RO design exploration, based on self-aligned CVD GFETs with alumina top-gates, against different metrics for proposing techniques to enhance circuit performance. The first physical implementation of a GFET RO based on top-gate devices is presented in [126], and a second GFET RO based on local back-gate devices is developed in [127].

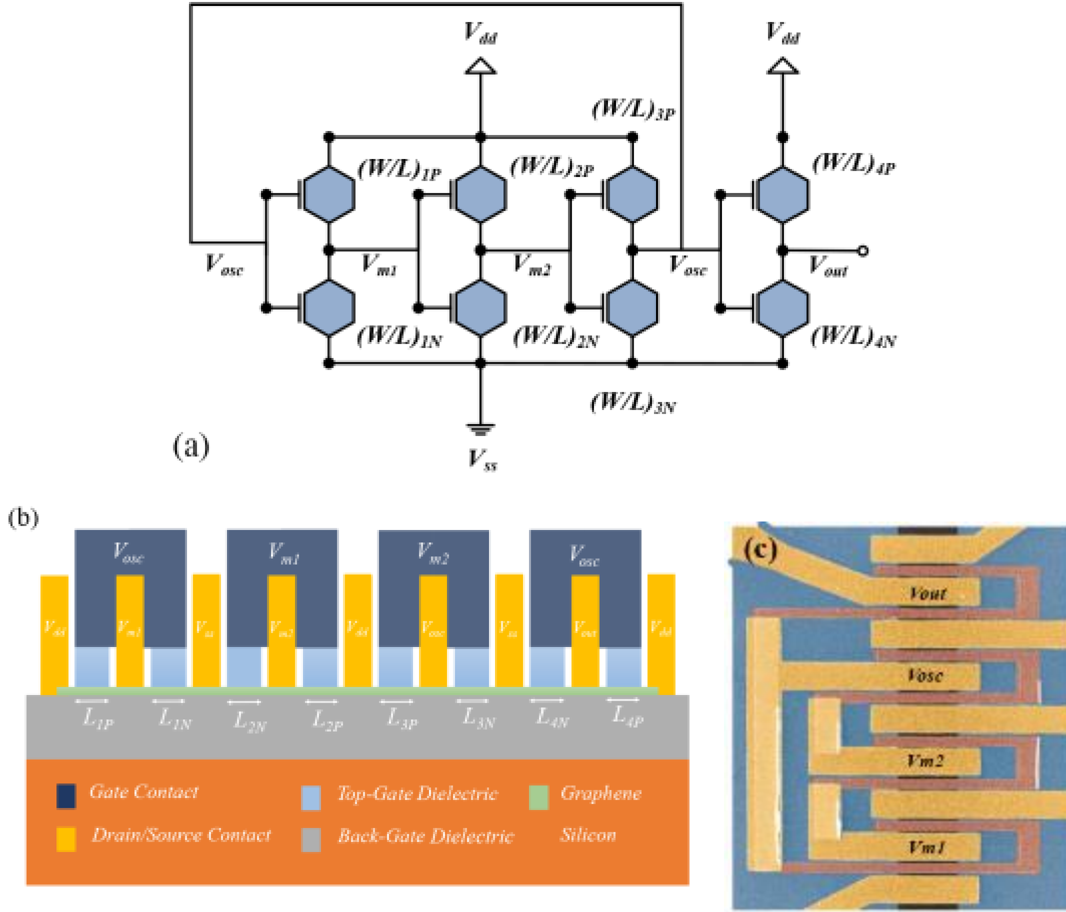


Figure 4.9 GFET RO based on three GFET INVs acting as delay stages and one GFET INV acting as an output buffer. (a) Circuit schematic (b) Cross-section layout. (c) Top-section layout fabricated by the Technical University of Milan with W = 5 µm, L = 800 nm, t_{OX} = 4 nm. Edited from [85].

A GFET RO consists of a chain of INVs connected in a loop, whereby the input-output voltage V_{osc} autonomously oscillates. This circuit must comply with Barkhausen's criterion for oscillation, thus needing an odd number of INVs, 3 in our case as seen in Figure 4.9. A set of performance metrics and design parameters are chosen when performing a design space exploration for any circuit. The RO advantage is that only two metrics, namely the oscillation frequency f_{osc} and the voltage dynamic range ΔV_{osc}, are enough to carry out a basic characterization of the circuit performance. The parametric variables chosen are the GFET L and t_{OX}. The loop makes a RO unstable and therefore induces oscillation if all INVs are identical, exhibit signal matching (chapter 4.1.3) and voltage gain A_v, where $n \geq 3$ is the odd number of INVs in the loop (here n = 3 and $|Av| > 2$). Since each INV is both driven and loaded by another one, f_{OSC} can be expressed as, and τ represents the INV delay [128]:

$$|A_v| > \frac{1}{\cos\left(\frac{\pi}{n}\right)} \qquad f_{OSC} = \frac{1}{2n\tau} \qquad (35)$$

4.2.1 RO Simulation Benchmark based on Exfoliated GFETs

Based on the lessons learned from the DC and transient analysis for GFET INVs presented in chapter 4.1.2, a GFET RO is simulated in Figure 4.10. Our compact model parameters are fitted to an exfoliated GFET fabricated with a back-gate h-BN. The circuit parameters are $(W/L)_{N\text{-}P}$ = 3 µm / 300 nm, t_{OX} = 20 nm, and V_{dd} = 5 V. The achieved V_{osc} and f_{osc} are 4.3 V and 13.1 GHz respectively, at these frequencies extrinsic parameters as $R_{g'}$, $C_{gso'}$, and $C_{gdo'}$ are negligible (Figure 3.8). Ideal conditions are assumed: no pads, no bonding wires, no output buffer for measurements.

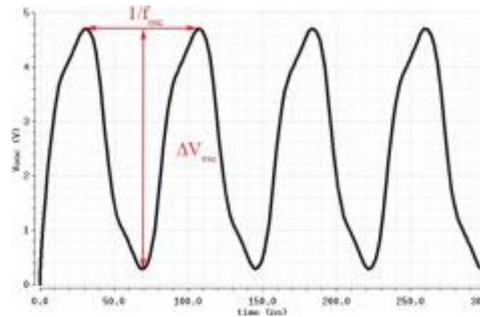


Figure 4.10 GFET RO $V_{osc}(t)$ transient simulation. Our compact model parameters are fitted to a fabricated exfoliated GFET. The circuit parameters are $(W/L)_{N\text{-}P}$ = 3 µm / 300 nm, t_{OX} = 20 nm, and V_{dd} = 5.

In Figure 4.11a, transient simulations are run for several GFET ROs with the following parameters: $(W/L)_{1N\text{-}3N} = (W/L)_{1P\text{-}3P}$ = 10, and V_{dd} = 5 V **(Conference B)**. The design exploration consists in calculating f_{OSC} against an L range that goes from 300 nm to 3 µm, for selected t_{OX} values. t_{OX} is usually fixed by the technology process therefore is not a circuit design variable, although sweeping it as a parameter provides an insight on how it affects to f_{OSC}. As expected for both models, f_{OSC} increases while L decreases, drastically when L < 500 nm. f_{OSC} increases while t_{OX} increases for the GFET drift-diffusion model, but this trend weakens for t_{OX} > 20 nm. f_{OSC} also increases while t_{OX} increases for the GFET virtual-source model, although the increments are smaller, until t_{OX} = 20 nm is reached where f_{OSC} is decreasing instead. All this is suggesting that there is an optimum t_{ox} to maximize f_{OSC}, and we suspect this is due to the role play by the distinctive graphene quantum-capacitance which is in series with the gate capacitance.

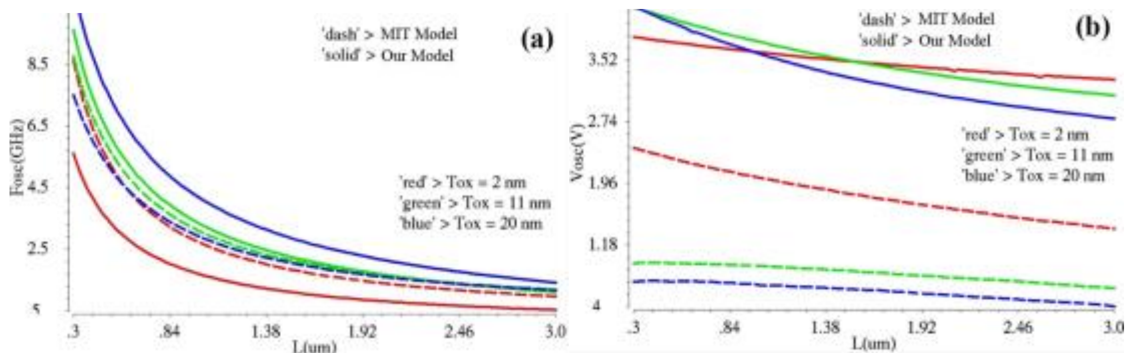


Figure 4.11 GFET RO comparison between a drift-diffusion compact-model (solid) and a virtual-source compact-model (dash) with $(W/L)_{1N\text{-}3N} = (W/L)_{1P\text{-}3P}$ = 10, and V_{DD} = 5 V as circuit parameters. (a) $f_{OSC}(L)$ for different t_{OX}. (b) $\Delta V_{osc}(L)$ for different t_{OX}.

In Figure 4.11b, the dynamic voltage-range ΔV_{osc} is calculated against L for selected t_{OX} values. ΔV_{osc} values are higher for our model because it provides more A_v for the INV than in MIT model (Figure 4.3). For both models, ΔV_{osc} increases while L decreases. ΔV_{osc} also increases while t_{OX} decreases for the GFET drift-diffusion model, but this trend weakens for $t_{OX} < 2$ nm. For the GFET virtual-source model, ΔV_{osc} also increases while t_{OX} decreases, but the increments are smaller, until t_{OX} = 6.5 nm is reached where ΔV_{osc} is decreasing instead. As a conclusion, considering our model, thicker dielectric increases substantially the frequency while maintaining the voltage dynamic-range. On the contrary, considering the MIT model, thinning the dielectric does not affect much to the frequency but increases effectively the voltage dynamic-range.

4.2.2 RO Simulation against Measurement Benchmark based on CVD GFETs

A model parameter fitting at circuit level between a fabricated CVD GFET RO in Technical University of Milan and a simulated GFET RO based on our compact model is performed. The circuit parameters for Figure 4.12 are $(W/L)_{N-P}$ = 10 µm / 1.1 µm, t_{OX} = 4 nm, ε_R = 6.24, µ = 690 $cm^2/V.s$, $R_{d/s}$ = 75 Ω. µm, N_f = -5 x 10^{15} cm^{-2}, $\hbar\omega$ = 56 meV, Δ_N = 150 meV, and Δ_P = 200 meV, C_{load} = 20 pF, and V_{dd} = 2.5. The output pads capacitance, and an output buffer are assumed in the simulations to replicate a realistic test environment.

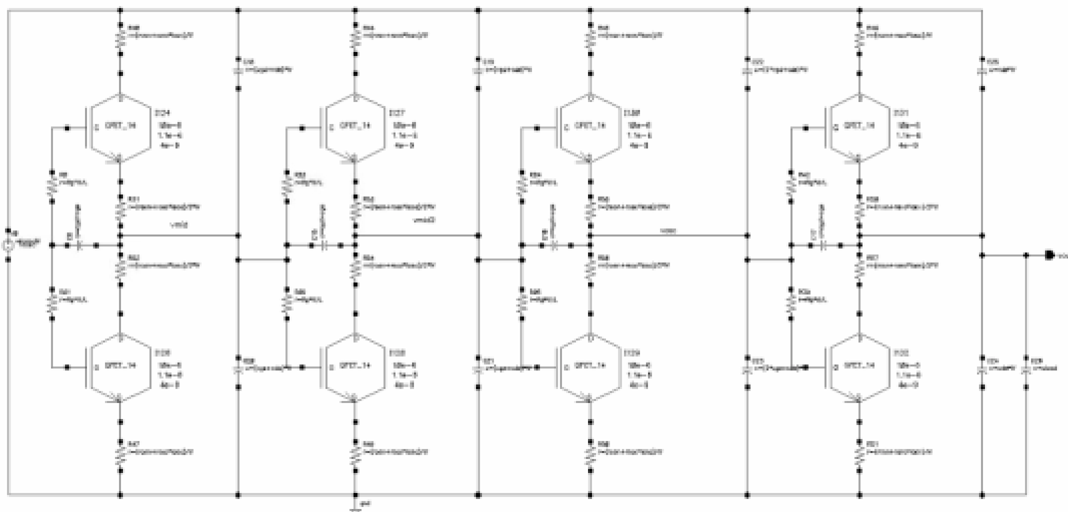


Figure 4.12 Simulator schematic of a GFET RO based on three GFET INVs acting as delay stages and one GFET INV acting as an output buffer and its correspondent pad load.

In Figure 4.13, the achieved ΔV_{out} and f_{out} are 40 mV and 1.3 GHz respectively, at these frequencies extrinsic parameters as $R_{g'}$, $C_{gso'}$, and $C_{gdo'}$ are considered zero.

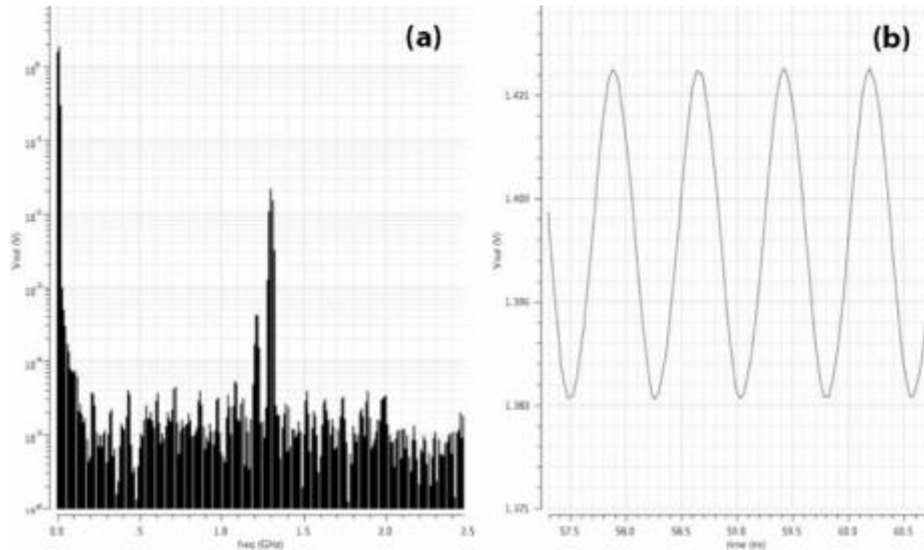


Figure 4.13 GFET RO simulation. (a) V_{out} (f) spectrum. (b) V_{out} (t) transient. Our compact model parameters are fitted to a measured CVD GFET RO (not shown). The circuit main parameters are $(W/L)_{N\text{-}P}$ = 10 µm / 1.1 µm, t_{OX} = 4 nm, and V_{dd} = 2.5.

4.2.3 RO Design Exploration based on self-aligned CVD GFETs

A design exploration based on the transient simulations of a RO with the model parameters of a self-aligned CVD GFET (chapter 4.1.4) is performed, trying to predict FoMs in the most realistic manner. The model parameters in Figure 4.14 are: W = 2 x 10 µm, L = 60 nm, t_{OX} = 10 nm, ε_R = 5.6, µ = 500 cm^2/V.s, R_{con} = 52.5 Ω.µm, ħω = 56 meV, Δ = 170 meV, R_g = 124 mΩ, $C_{gso'}$ = 198 pF/m and $C_{gdo'}$ = 151 pF/m. For V_{dd} = 1.5 V, the achieved ΔV_{osc} and f_{OSC} are 263 mV and 39 GHz respectively. Comparing with the INV from Table 4.2, f_{osc} is increased by reducing V_{dd}, at the cost of reducing ΔV_{osc} dramatically.

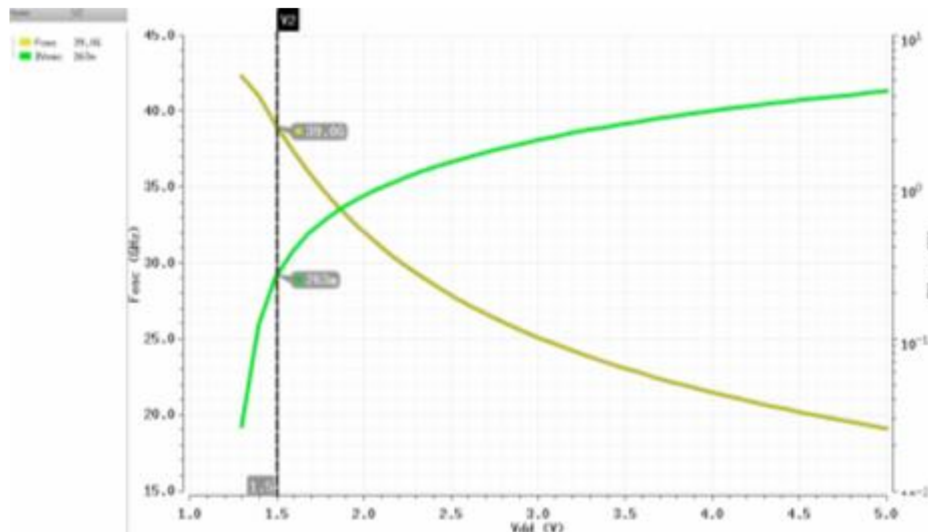


Figure 4.14 GFET RO f_{osc} and ΔV_{osc} against V_{dd}. Our compact model parameters are fitted to a self-aligned CVD GFET. The circuit main parameters are $(W/L)_{N\text{-}P}$ = 20 µm / 60 nm and t_{OX} = 10 nm.

In Figure 4.15, we are calculating f_{osc} (L) and ΔV_{osc} (L) for specific t_{OX} values. Interestingly, the reduction of t_{OX} is only effective for increasing f_{OSC} when L < 30 nm. On the other hand, if L and t_{OX} are reduced ΔV_{osc} is always increasing, a value of 105 GHz and 0.6 V respectively should be achievable for W/L = 1 µm / 15 nm, t_{OX} = 2 nm and V_{dd} = 0.9 V.

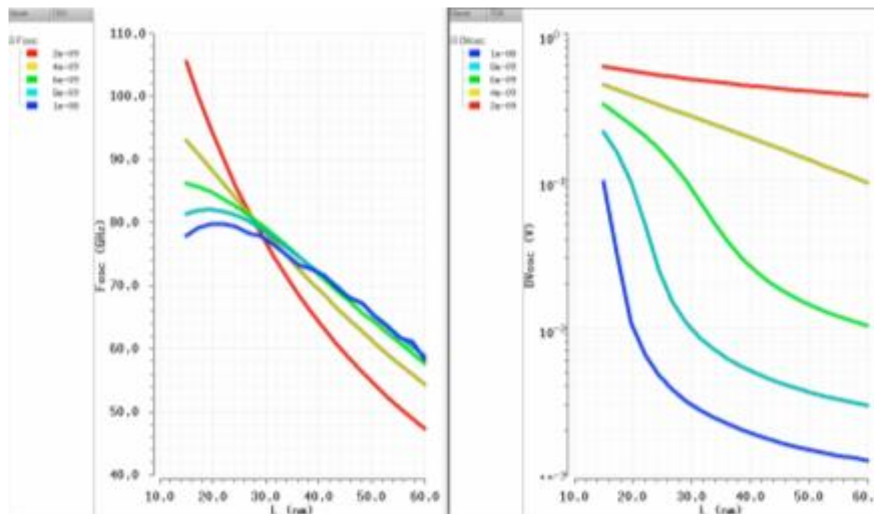


Figure 4.15 GFET RO FoMs simulations. (a) f_{OSC} (L) and (b) ΔV_{OSC} (L) for different t_{OX} values. The compact-model parameters are fitted to the measurements of a self-aligned CVD GFET with W = 1 µm and V_{dd} = 0.9 V.

4.3 GFET Cascode Amplifiers

As already mentioned in section 3.2.2, the most challenging issue for GFETs is yet to reduce g_o in a channel where charge cannot be fully depleted. There are some approaches discussed in the literature that try to modulate g_o for GFETs. In [129], a current source built with two GFETs connected in a feedback-configuration is proposed, although the circuit is simulated with a simplified compact model that precludes the understanding of its behaviour at bias close to Dirac point, and additionally the extrinsic parasitic resistances are not considered. In [130], a GFET negative-differential-resistance (NDR) circuit is proposed, in this case the drain of a GFET is connected to its gate through an inverter implemented with other two GFETs. The circuit is fabricated and is able to provide a g_o < 0. The purpose of this chapter is to improve by circuit techniques, the poor A_v exhibited by CVD GFETs. The cascode amplifier (CAS) is a basic circuit with the aim of reducing g_o as much as possible while maintaining g_m. This cell consists of stacking a second GFET with a fixed gate-bias to the main GFET. A large signal compact model, fitted to two different CVD GFETs, the first fabricated at University of Siegen in Germany, and the second at Polytechnic University of Milan in Italy, is used to perform the circuit simulations. Three CAS circuits are designed based on such technologies and the third one is also fabricated by University of Siegen in cooperation with the Institute of Electronics, Microelectronics and Nanotechnology in France **(Conference A)**.

4.3.1 CAS Simulation based on CVD GFETs Fabricated with Silica Top-Gates

First, the parameter values of our optimized compact model shown in section 3.3.2 are fit to measurements carried on a GFET fabricated and measured at University of Siegen. The channel is fabricated with CVD graphene (W = 40 µm, L = 4 µm, $L_{s/d}$ = 3 µm), the source/drain contacts with Cr/Au (thickness = 10/90 nm), the top-gate with e-beam evaporated SiO_2 (t_{OX} = 20 nm), the Si<100> substrate with 85 nm thermally grown SiO_2, and the top-gate contact with Al (thickness = 100 nm). Second, a comparison between a GFET device and a CAS circuit is performed through simulations. The CAS consists of cascading a common-source $GFET_1$ and a common-gate $GFET_2$ as shown in Figure 4.16, where $W_{1/2}$ are the channel widths, $L_{1/2}$ are the gated channel lengths, $L_{s/m/d}$ are the ungated channel-lengths, and $t_{OX1/2}$ are the gate-dielectric thicknesses. $GFET_2$ is acting as a voltage follower, so its drain voltage is following V_{bias} instead of V_{out}, this node decoupling improves the final current saturation of the circuit:

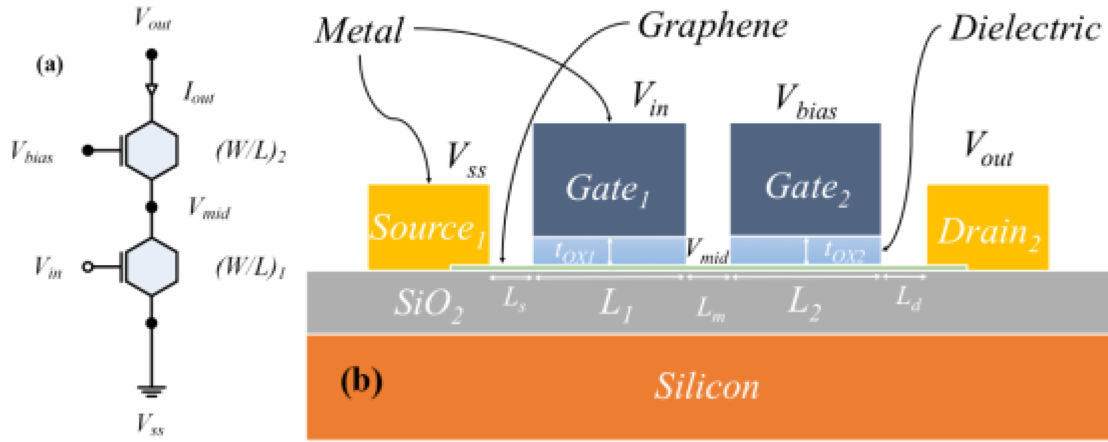


Figure 4.16 GFET CAS. (a) Circuit schematic. (b) Cross-section layout. A common-gate $GFET_2$ is cascaded to a common-source $GFET_1$ to increase its A_v by tuning V_{bias}.

This can also be interpreted as a GFET device with a much-decreased output conductance:

$$\frac{\partial I_{out}}{\partial V_{out}} = g_o \approx \frac{g_{o1} \times g_{o2}}{g_{m2}} \tag{36}$$

and similar transconductance:

$$\frac{\partial I_{out}}{\partial V_{in}} = g_m \approx g_{m1} \tag{37}$$

deriving into a substantial increase in intrinsic gain:

$$A_v \approx \frac{g_{m1} \times g_{m2}}{g_{o1} \cdot g_{o2}} \tag{38}$$

In other words, assuming both GFET sizes are equal, the CAS voltage-gain upper limit should be the square of the GFET intrinsic-gain [128]:

$$A_{v_CAS} \approx A_{v_GFET}{}^{2} \quad (39)$$

As shown in Figure 4.17a, the GFET output current I_{out} saturation is weak, which is a typical signature of monolayer graphene. The compact model is fit to measurements carried on a GFET device fabricated at University of Siegen and its corresponding parameter values are: W = 40 µm, L = 4 µm, t_{OX} = 20 nm, ε_R = 3.9, µ = 500 cm^2/V.s, $R_{d/s}$ = 8000 Ω.µm, N_f = -20 x 10^{15} cm^{-2}, ħω = 56 meV, and Δ = 150 meV. For the CAS circuit, R_m = 8000 Ω.µm and there is an additional design parameter (V_{bias}) to tune in. The best I_{out} saturation is achieved for V_{bias} = 10 V when both GFETs are working in the N-type region (positive g_m). This saturation can be quantified in Figure 4.17b, where the minimum g_o (V_{in}, V_{out}) achieved is 4 µS/µm for CAS at (6 V, 9.5 V), and 10 µS/µm for GFET at (8 V, 8.5 V), meaning that the CAS is dividing the GFET g_o by 2.5. Besides, it is shown that CAS provides always better g_o, for most of V_{in} and V_{out} voltage ranges. But the CAS situation is less favourable in terms of g_m which, due to graphene ambipolarity, can also be negative (P-type region).

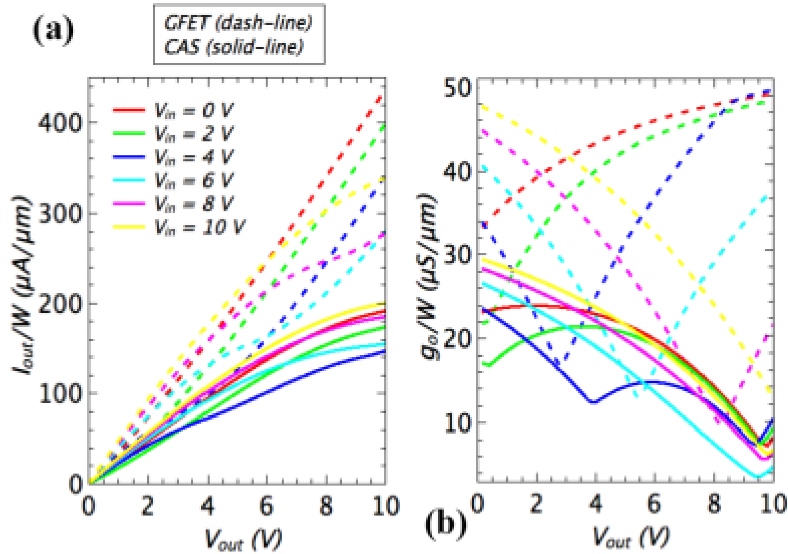


Figure 4.17 A simulated comparison between a graphene-FET device (dash-line) and a GFET cascode-amplifier (solid-line), where W = 40 µm, L = 4 µm, t_{OX} = 20 nm and V_{bias} = 10 V. (a) I_{out}/W (V_{out}) for selected V_{in}. (b) g_o/W (V_{out}) for selected V_{in}.

Figure 4.18a is showing that the GFET maximum absolute g_m (V_{in}, V_{out}) is 38 µS/µm at (4 V, 8.5 V), and for CAS is 22 µS/µm at (6 V, 9 V). Now the CAS circuit is dividing GFET g_m by 1.7, so the benefit of reducing g_o is slightly masked by the drawback of decreasing g_m. To maximize A_v, a maximum g_m and minimum g_o must occur at the same bias point. In Figure 4.18b is depicted that the maximum A_v (V_{in}, V_{out}) achieved for CAS is 6 at (6 V, 9 V), and for GFET is 3.5 at (8 V, 8 V). Therefore, it is demonstrated that the CAS circuit is offering an increase in terms of amplification (almost the double) at specific bias points, but still far away of the theoretical 12.25 squared gain.

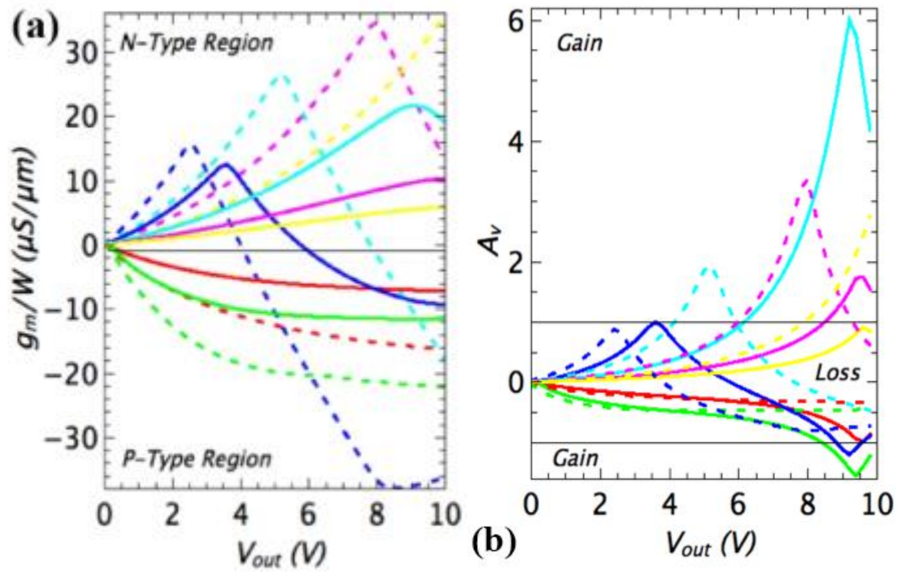


Figure 4.18 A simulated comparison between a GFET device (dash-line) and a GFET CAS (solid-line), where W = 40 µm, L = 4 µm, t_{OX} = 20 nm and V_{bias} = 10 V. (a) g_m/W (V_{out}) for selected V_{in}. (b) A_v (V_{out}) for selected V_{in}.

The aforementioned degradation of g_m is the main cause of the problem. As it can be seen in Figure 4.19, if a hypothetical case where R_m = 0 Ω.µm is considered, the g_m improves and hence A_v. Although this implies that there is no ungated graphene channel L_m between Gate$_1$ and Gate$_2$ at Figure 4.16b, which physically is unfeasible, anyways this gap should be reduced as much as possible to minimize non-desired extrinsic resistance.

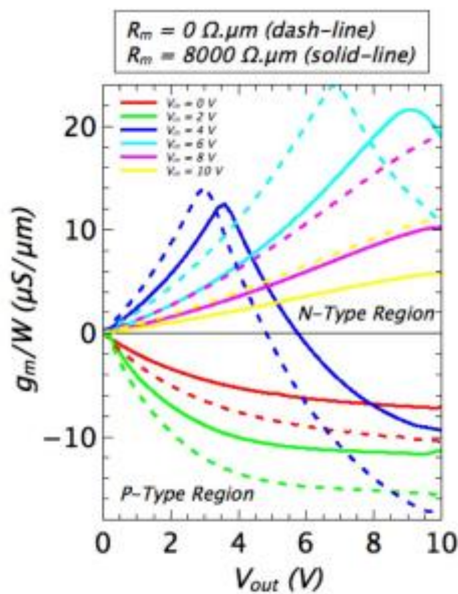


Figure 4.19 A comparison between the normalized transconductance of a GFET CAS with R_m = 8000 Ω.µm (solid-line) and R_m = 0 Ω.µm (dot-line), where W = 40 µm, L = 4 µm, t_{OX} = 20 nm and V_{bias} = 10 V.

It is also important to point out that the $GFET_1$ is acting as a source-follower (not common-source) when it is working in the P-type region so the circuit proposed is not working as a CAS configuration anymore, therefore the improvement in A_v compared to a GFET, as seen in Figure 4.18b, is marginal.

4.3.2 CAS Simulation based on CVD GFETs fabricated with Alumina Top-Gates

The parameter values of the compact-model shown in Figure 3.4 are extracted from the measurements of a GFET fabricated at Technical University of Milan. The channel is fabricated with CVD graphene (W = 10 µm, L = 2 µm, $L_{d/s}$ = 500 nm), the source/drain contacts with Au (thickness = 75 nm), the top-gate dielectric with AlO_x, (t_{OX} = 4 nm), the substrate with SiO_2 (thickness = 300 nm) and the top-gate contact with Al/Ti/Au (thickness = 32/1/9 nm) [85]. Compared to GFETs fabricated at University of Siegen, the top-gate dielectric is 5 times thinner and its ε_R is 1.6 times higher, both features improve the electrostatic control of the graphene channel. Besides, $L_{s/d}$ is just the 50% of L, which in section 4.3.1 is almost 150%, which obviously implies bigger extrinsic resistance. For the CAS circuit, the best current saturation is also achieved for V_{bias} = 10 V when both GFETs are working in the N-type region (positive g_m). In Figure 4.20a, a simulated GFET I_{out} is compared to its correspondent CAS I_{out}, the latter generally showing better current saturation, specifically when $V_{in} < 4$ V. As shown Figure 4.20b, g_o is crossing the zero value several times for specific bias-points in both cases. This is another distinctive feature of GFET devices compared to silicon devices [131]. It is shown that CAS provides always smaller maximum absolute values for g_o. Although another interesting improvement is that there is a clear trend for CAS g_o decreasing while V_{out} is increasing which does not happen always for the GFET.

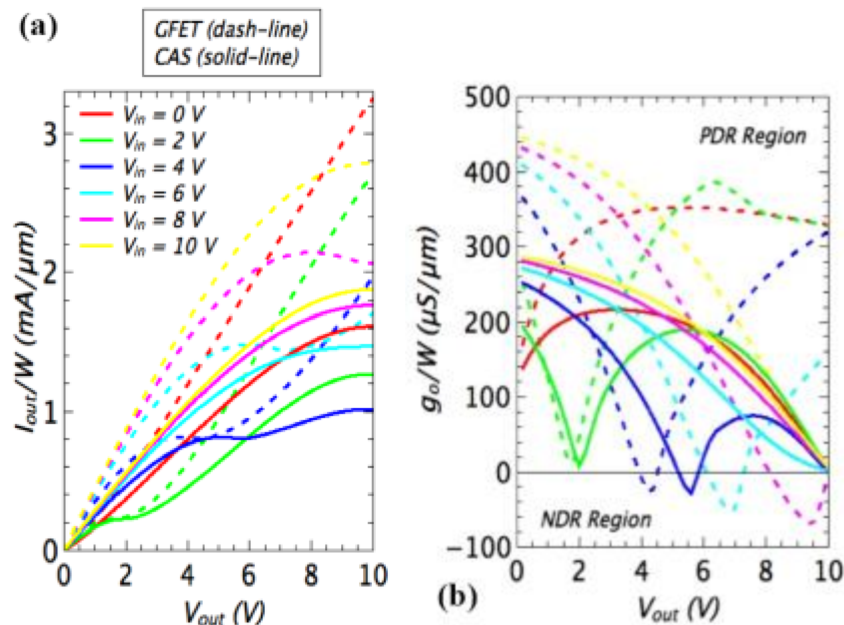


Figure 4.20 A simulated comparison between a GFET device (dash-line) and a GFET CAS (solid-line), where W = 10 µm, L = 2 µm, t_{OX} = 4 nm and V_{bias} = 10V. (a) I_{out}/W (V_{out}) for selected V_{in} values. (b) g_o/W (V_{out}) for selected V_{in} values, where NDR/PDR stands for negative/positive differential resistance.

Figure 4.21a is showing that the GFET maximum absolute g_m (V_{in}, V_{out}) is 450 µS/µm at (2 V, 5.9 V), and for CAS is 350 µS/µm at (4 V, 5.5 V). The CAS circuit is again degrading GFET g_m, as it is in the case of devices fabricated at University of Siegen. Unfortunately, the fact that g_m and g_o may adopt positive and negative values is making the final A_v analysis rather complex. In Figure 4.21b&c, it is shown that there are several bias points where infinite A_v (V_{in}, V_{out}) is achieved for both GFET and CAS. In fact, these infinite values at the discontinuities are shown truncated due to the finite resolution-step of the data. The CAS is clearly improving the A_v for V_{in} < 2 V, where GFET is not able to provide any gain at all when V_{in} = 0 V. Besides, the largest continuous V_{out_range} = 4 V where there is positive amplification (A_v > 1) is shown when V_{in} = 6 V. For negative amplification (A_v < 1), V_{out_range} = 5 V when V_{in} = 2 V. In GFET case, V_{out_range} = 2.5 V when V_{in} = 10 V and V_{out_range} = 1.5 V when V_{in} = 8 V, respectively.

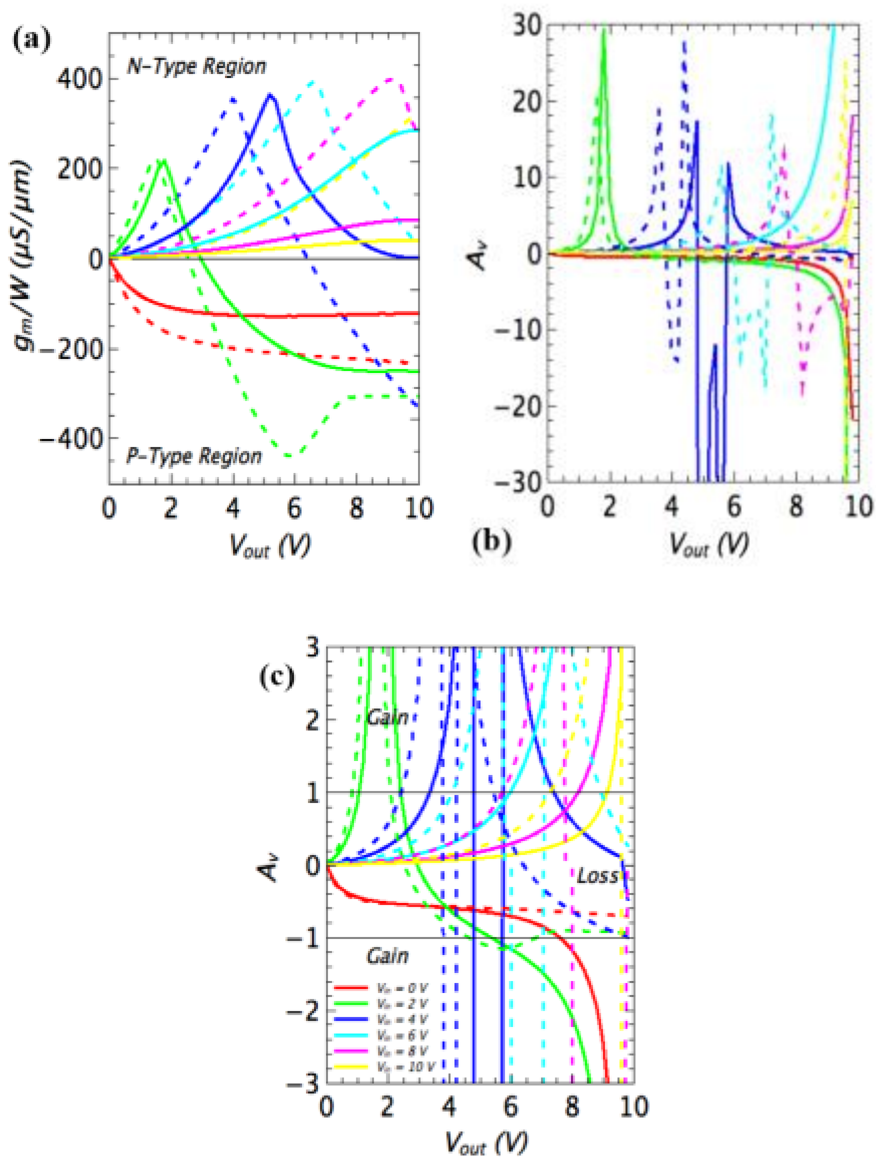


Figure 4.21 A simulated comparison between a GFET device (dash-line) and a GFET CAS (solid-line) where W = 10 µm, L = 2 µm, t_{OX} = 4 nm and V_{bias} = 10V. (a) g_m/W (V_{out}) for different V_{in}. (b) A_v (V_{out}) for different V_{in}. (c) A zoom-in of A_v.

4.3.3 CAS Fabrication based on CVD GFETs with Silica/Alumina combined Top-Gates

GFET devices and CAS circuits are fabricated at the Institute of Electronics Microelectronics and Nanotechnology in Lille as shown in Figure 4.22, where $W = W_{1/2}$ are the channel widths, $L_{1/2}$ are the gated channel lengths, and $L_{s/m/d}$ are the ungated channel-lengths. The channel is CVD graphene synthesized at University of Siegen ($W = 20$ µm, $L = 1.5$ µm, $L_{d\text{-}s} = 200$ nm, $L_m = 5.4$ µm), the gate/source/drain contacts with Ni/Au (thickness = 15 / 35 nm), the top-gate dielectric with SiO_2/AlO_x (t_{OX} = 25 / 15 nm), and the substrate with SiO_2 (thickness = 85 nm). V_{bias} = 0 V for the CAS circuit.

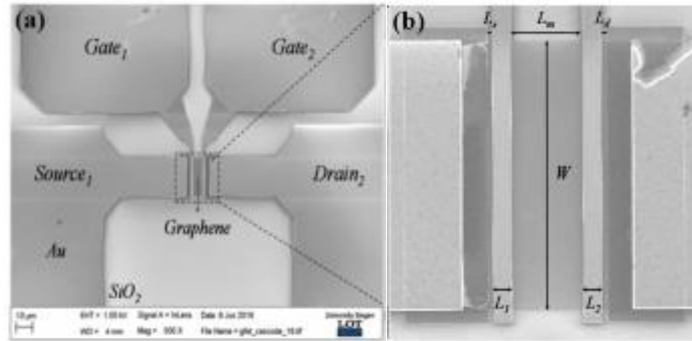


Figure 4.22 (a) A scanning electron microscopy image of a GFET CAS fabricated in the Institute of Electronics Microelectronics and Nanotechnology in Lille with graphene synthesized at University of Siegen. (b) Zoom-In.

In Figure 4.23a, a measured GFET I_{out} is compared to its correspondent CAS I_{out}, the latter showing better current saturation. The improvement in saturation is quantified in Figure 4.23b. The minimum g_o (V_{in}, V_{out}) achieved is 18 µS/µm for CAS at (8/10 V, 7 V), and 112 µS/µm for GFET at (8 V, 6.5 V) with noisy measurement-data being disregarded. It is shown that CAS is providing better g_o for the whole voltage range.

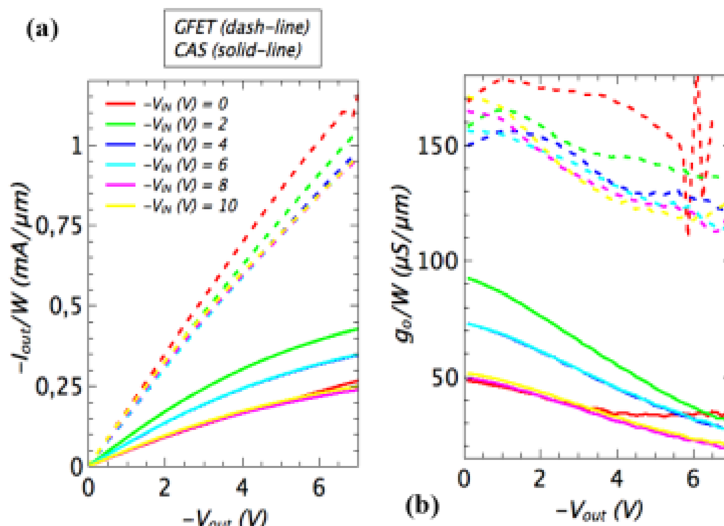


Figure 4.23 A measured comparison between a GFET device (dash-line) and a GFET CAS (solid-line) where $W = 20$ µm, $L = 1.5$ µm, t_{OX} = 25 / 15 nm and V_{bias} = 0 V. (a) I_{out}/W (V_{out}) for selected V_{in}. (b) g_o/W (V_{out}) for selected V_{in}.

Figure 4.24a is showing that the GFET maximum absolute g_m (V_{in}, V_{out}) is 45 µS/µm at (2 V, 7 V), and for CAS is 120 µS/µm at (0 V, 6 V). For V_{in} = 0/2/6 V, the CAS circuit is offering the highest g_m values, even when fabricated with a L_m that is 270% of its L. In Figure 4.24b, it is shown that the CAS is able to achieve a gain of 6.5 at (0 V, 5 V), generally improving A_v compared to GFET which is not able to provide gain at all, see Figure 4.24c.

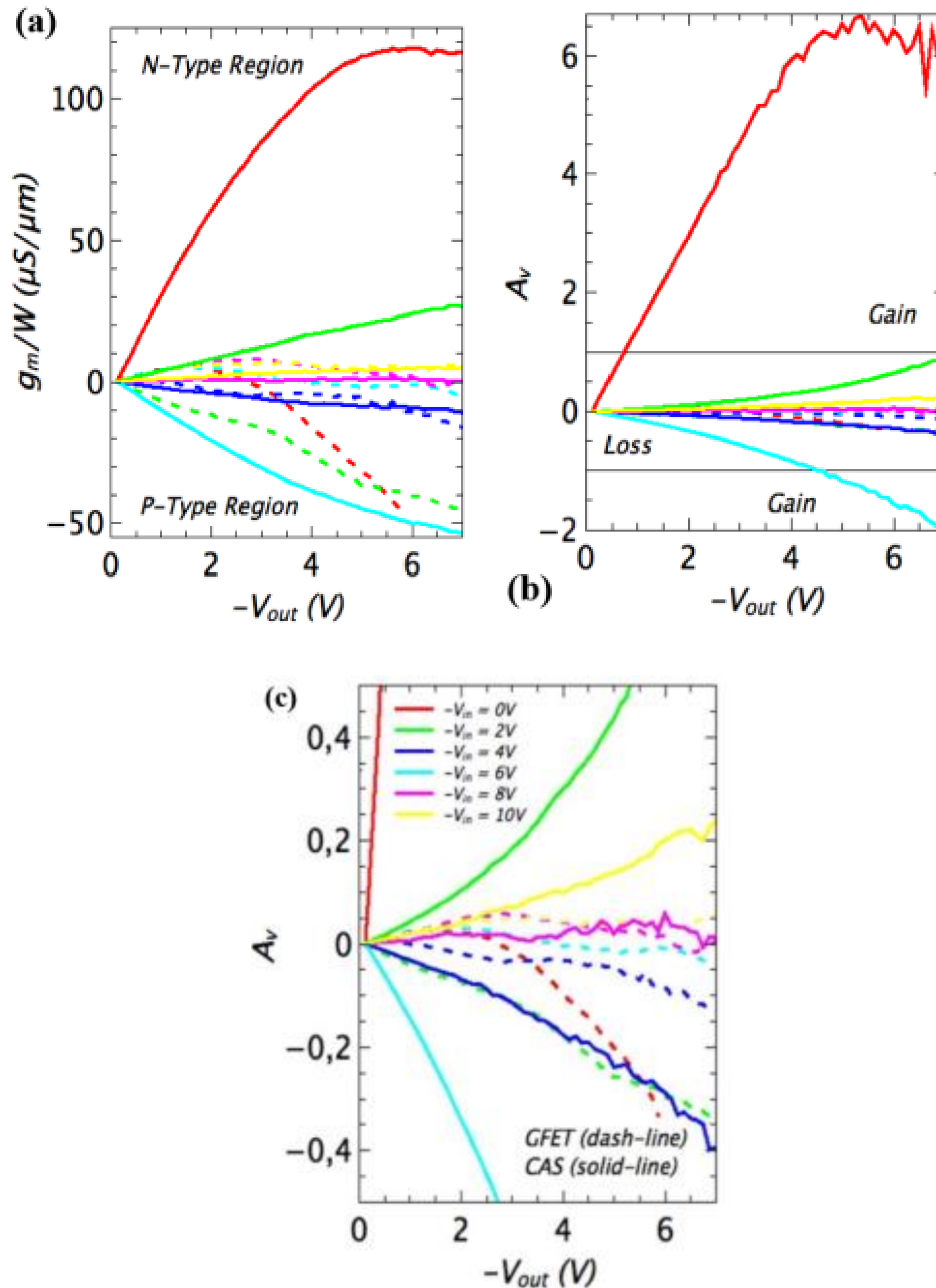
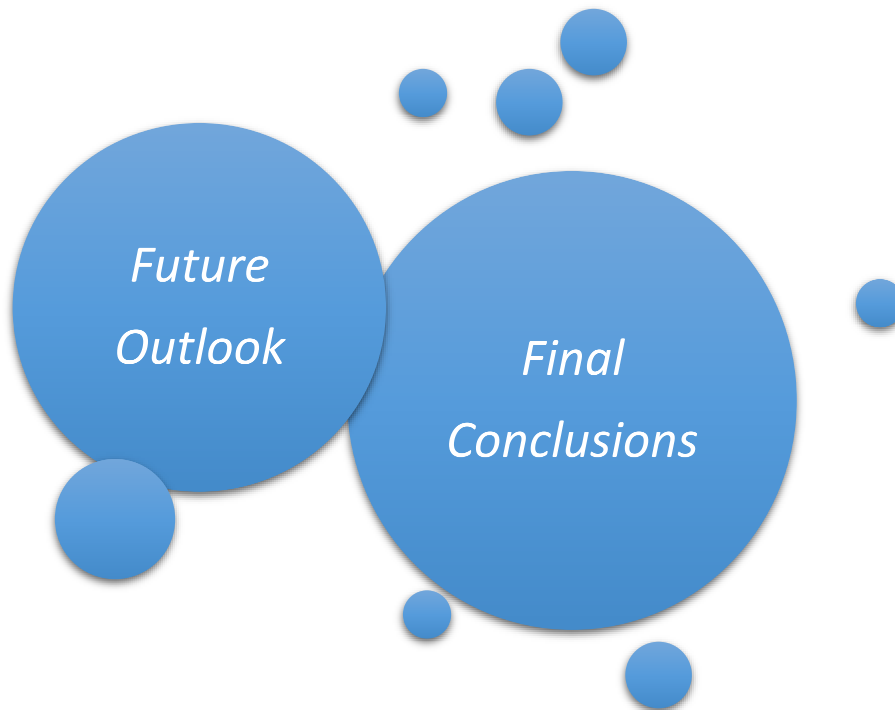


Figure 4.24 A measured comparison between a GFET device (dash-line) and a CAS circuit (solid-line) where W = 20 µm, L = 1.5 µm, t_{OX} = 25 / 15 nm and V_{bias} = 0 V. (a) g_m/W (V_{out}) for selected V_{in}. (b) A_v (V_{out}) for selected V_{in}. (c) A zoom-in of A_v.

4.4 Conclusions

Most common applications for GFET devices are small-signal (AC/RF) circuits, although large-signal/non-linear circuits as already said deserve thorough exploration as well. This chapter has explored three different types of circuits based on GFETs namely: INVs, ROs, and CAS. Taking advantage of the ambipolar behaviour of the GFET I_{ds} (V_{gs}) transfer, an INV has been designed with two GFETs and simulated to explore its behaviour for static and transient conditions. An INV design exploration comparison between our compact model base on drift-diffusion transport introduced in chapter 3 and a model based on the virtual-source approach, both fitted to exfoliated GFETs with h-BN back gate dielectric is carried out, we decide to carry out with our model due to its easier and faster parameterization **(Conference B)**. Besides a measurement benchmark against a INV based on CVD GFETs is performed where the suitability of our model for DC fitting is proved. At the end, a design exploration for GFET INV fitted to a self-aligned CVD GFET is performed where a f_{clk} = 36.4 GHz and ΔV_{out} = 1.7 V should be achievable for W/L = 20 μm/ 15 nm, t_{ox} = 10 nm and V_{dd} = 2.5 V assuming external parasitics. A RO based on three GFET INVs is designed and simulated to explore its large-signal behaviour for dynamic conditions and future circuit scaling. First a RO simulation benchmark between our proposed model against the MIT virtual-source model based on exfoliated GFETs is performed; second a RO simulation against measurement benchmark based on CVD GFETs with alumina top-gates where our GFET model suitability for dynamic transients is proven; and third a RO design exploration, based on self-aligned CVD GFETs with alumina top-gates, is carried out where a f_{osc} = 105 GHz with ΔV_{osc} = 0.6 V is achieved for W/L = 1 μm / 15 nm, t_{ox} = 2 nm and V_{dd} = 0.9 V. For GFET dynamic circuits, it is clear that external parasitics, specifically $C_{gso'}$ and $C_{gdo'}$ start to dominate for L < 100 nm, therefore new techniques to minimize them are a must if we want to get benefit of reducing L and increasing μ. Finally, a CAS based on two GFETs is designed, simulated and fabricated to explore its large-signal behaviour for static conditions with the purpose of improving the A_v impaired by the intrinsic weak current saturation observed for monolayer GFETs. This work has demonstrated the design of CAS circuits based on CVD GFET devices, through an established co-design approach based on compact-model simulation and nano-device fabrication. According to simulations, the CAS circuit is improving current saturation at most bias voltages. If g_m values are not degraded, the g_o reduction is increasing A_v and V_{out} range compared to GFET devices. Reducing L_m helps keeping g_m by minimizing undesired extrinsic resistances in CAS circuits. The fabricated CAS seems to confirm the simulation predictions. For GFET static circuits, the reduction of metal/graphene $R_{d/s}$ and the increase of CVD graphene μ are a must to be able to scale them properly without losing their amplifying capability.

5 Final Conclusions: Future Outlook



The requirements for future high/ultra-high data rate nanoTRx applied to WNN which imply short/ultra-short distance ranges (3 – 300 cm) have been defined in chapter 1. To become a reality, WNN need smaller (0.1 - 100 mm^2), faster (0.1 - 100 Gbps), more energy efficient (0.1 – 10 pJ/bit) and less power hungry (1 - 100 mW) TRx than in existing wireless networks. We are talking about 2 - 3 orders of magnitude reduction in size, data rate and power consumption which is not possible with the present technologies available. After realizing a careful analysis of the existing SoA TRx in literature, we conclude that miniaturisation at device level and simplification at architecture level is a must to target future wireless nanoTRx **(Journal III & Conference C)**. It has been shown that with existing RF transistors is extremely challenging to design the architectures required due to the impossibility of scaling further to achieve the required speeds and/or their impossibility of being integrated with digital transistors. Hypothetically speaking there is an urgent need for FETS that are able to scale with a f_{max} beyond 2 THz, consequently new discovered 2D materials are proposed as channels for future nanotransistors. IR/UWB techniques need to be carefully inspected at much higher frequencies as they may reduce the complexity of the nanoTRx. New materials to fabricate innovative transistors are needed to achieve such high levels of speed and integration to achieve THz-IR TRx (nanoTRx). Graphene has been introduced and its extraordinary electronic properties explained. Consequently, it is proposed as a plausible channel for RF FETs thanks to its high carrier μ values (2000 - 80000 cm^2/V.s) and one-atom thickness which should imply high g_m which is a must for achieving high f_t, and excellent electrostatic control which is needed for overcoming short-channel effects when scaling. GFETs (among other graphene transistors) are chosen because FETs are scalable-friendly transistor architectures, and scaling capacitances is a must to conquer high frequencies. It is shown that rather high g_m (1.2 - 2.9 mS/μm) are

achievable for GFETs. We choose the CVD technique for their fabrication because it is compatible with CMOS technology, the drawback is that CVD GFET g_m figures (< 1 mS/µm) need improvement. An optimization of metal/graphene contact and gate self-alignment to reduce $R_{d/s}$, an increase in CVD graphene quality to increase µ, and smoother (higher ħω) substrates contribute to increase g_m. Although all these measures are not enough, we suspect that the key factor lays on the optimization of the interface between graphene and the gate dielectric to minimize the undesired C_q effect and improve its electrostatic control. Achieving high f_{max} only with high g_m is not enough either, low g_o is required as well to get $A_v > 1$. Monolayer GFETs face an enormous challenge, namely its weak current saturation (high g_o) due to graphene's lack of bandgap. Nevertheless, extremely low g_o (0 – 2 µS/µm) have been measured in GFETs. NDR has been predicted by GFET models and measured in GFET devices, this is a phenomenon that should be explored further to fully understand the mechanisms behind it and being able to increase A_v. Another promising alternative to reduce g_o could be the use of bilayer graphene: artificially stacked bilayer CVD graphene have shown improved A_v figures **(Conference E & Journal IV)**. Compact models for transistors are necessary tools for circuit simulators. We choose a drift-diffusion approach due to its simplicity and acceptable accuracy when parameterizing measurements even for GFETs with L < 100 nm. An optimized model for GFETs is proposed where a new solution for the I-V transfer of a GFET compact-model is provided **(Journal I & II)**. The exact analytical calculation of the current denominator ensures improved accuracy around the Dirac point, thus avoiding undesired distortions when designing large-signal circuits. This allows the scaling of the model and its circuit parameters such as V_{dd}, L, t_{ox} and µ. The model has been implemented in Verilog-A and its parameters fitted to the measurements of experimental GFETs. The improved model has been carefully characterized through several simulations at device and circuit level, proving its robustness for different design parameters. Besides, a C-V model for GFET plus a small-signal model for extrinsic parasitics is presented and successfully fitted against the fastest CVD GFET technology fabricated nowadays to our knowledge. Furthermore, f_{max} is calculated by simulating S-parameters and a bias optimization to maximize f_{max} is performed where a value of 454 GHz is achieved for W/L = 20 µm / 60 nm and t_{OX} = 10 nm. Besides a f_{max} scaling prospect is derived to assess their real potential for future nanoTRx. For a GFET with W/L = 20 µm / 15 nm and t_{OX} = 10 nm, f_{max} = 1.54 THz values should be achievable upon our simulations. Most common applications for GFET devices are small-signal (AC/RF) circuits, although large-signal/non-linear circuits as already said deserve thorough exploration as well. This chapter has explored three different types of circuits based on GFETs namely: INVs, ROs, and CAS. Taking advantage of the ambipolar behaviour of the GFET I_{ds} (V_{gs}) transfer, an INV has been designed with two GFETs and simulated to explore its behaviour for static and transient conditions. An INV design exploration comparison between our compact model base on drift-diffusion transport introduced in chapter 3 and a model based on the virtual-source approach, both fitted to exfoliated GFETs with h-BN back gate dielectric is carried out, we decide to carry out with our model due to its easier and faster parameterization **(Conference B)**. Besides a measurement benchmark against a INV based on CVD GFETs is performed where the suitability of our model for DC fitting is proved. At the end, a design exploration for GFET INV fitted to a self-aligned CVD GFET is performed where a f_{clk} = 36.4 GHz and ΔV_{out} = 1.7 V should be achievable for W/L = 20 µm/ 15 nm, t_{ox} = 10 nm and V_{dd} = 2.5 V assuming

external parasitics. A RO based on three GFET INVs is designed and simulated to explore its large-signal behaviour for dynamic conditions and future circuit scaling. First a RO simulation benchmark between our proposed model against the MIT virtual-source model based on exfoliated GFETs is performed; second a RO simulation against measurement benchmark based on CVD GFETs with alumina top-gates where our GFET model suitability for dynamic transients is proven; and third a RO design exploration, based on self-aligned CVD GFETs with alumina top-gates, is carried out where a f_{osc} = 105 GHz with ΔV_{osc} = 0.6 V is achieved for W/L = 1 μm / 15 nm, t_{ox} = 2 nm and V_{dd} = 0.9 V considering parasitics. For GFET dynamic circuits, it is clear that external parasitics, specifically $C_{gso'}$ and $C_{gdo'}$ start to dominate for L < 100 nm, therefore new techniques to minimize them are a must if we want to get benefit of reducing L and increasing μ. Finally, a CAS based on two GFETs is designed, simulated and fabricated to explore its large-signal behaviour for static conditions with the purpose of improving the A_v impaired by the intrinsic weak current saturation observed for monolayer GFETs **(Conference A)**. This work has demonstrated the design of CAS circuits based on CVD GFET devices, through an established co-design approach based on compact-model simulation and nano-device fabrication. According to simulations, the CAS circuit is improving current saturation at most bias voltages. If g_m values are not degraded, the g_o reduction is increasing A_v and V_{out} range compared to GFET devices. Reducing L_m helps keeping g_m by minimizing undesired extrinsic resistances in CAS circuits. The fabricated CAS seems to confirm the simulation predictions. For GFET static circuits, the reduction of metal/graphene $R_{d/s}$ and the increase of CVD graphene μ are a must to be able to scale them properly without losing their amplifying capability.

5.1 Future Outlook

When doing research in nanoelectronics, working at the sweet-spot where technology is not too mature but not too innovative either is paramount. Now we feel that for GFETs it was too early to encompass circuit design but at the time we were confidents that technologists could solve the lack of current saturation challenge which has not occurred yet, although we insist that there is more research needed in that aspect, it is obvious that our knowledge in manipulating 2D materials is still in its infancy. We think that to contrast our simulations to actual real measurements when possible was critical to be able to assess reliable prospects, therefore my stage during a year in University of Siegen collaborating with Prof. Lemme's group helped me into realizing how difficult is to manipulate graphene and fabricate FETS out of it. Using early transistor models for circuit design brings lots of unexpected challenges that a commercial circuit designer never faces, specially discontinuities issues and converging problems are slowing the design process. The model parameter fitting to measurements has been an extremely tedious task needed to be performed hundreds of times, although we think that doing this manually would bring more perspective and deep understanding than if we were using automated fitting scripts. Future work will encompass the fabrication of ultra-short monolayer/multi-layer CVD GFETs (L < 60 nm) to prove that the forecasted RO figures are achievable in reality. A systematic study of double-gate monolayer GFETs should be performed. A new focus on reducing capacitance parasitics in FET structures in general should be started. More investigations

will be conducted to align simulations with measurements and fully comprehend the CAS benefits over monolayer/bilayer GFETs when scaling.

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Appendix A: Graphene FET Compact Model Verilog-A

```
/*****************************************************************************************
**************
*                                                                    *
* I-V and C-V compact-model for monolayer-graphene field-effect-transistors              *
* Editors: Mario Iannazzo (UPC), Valerio Lo Muzzo (ST) and Saul Rodriguez (KTH)          *
* Date: 22-February-2017                                             *
* GFET9 = Our own Verilog-A of the graphene-FET model published in DOI: 10.1109/TED.2013.2257832  *
* GFET14 = Our own Verilog-A of the graphene-FET model published in DOI: 10.1109/TED.2015.2479036
*
* GFET14 = GFET9 with a modified I-V compact-model to eliminate artifacts at Dirac Point       *
*                                                                    *
*****************************************************************************************
*************/

// GFET14 model start

`include "constants.vams"
`include "disciplines.vams"

module GFET_5(D, G, S);

inout D;
electrical D;
inout G;
electrical G;
inout S;
electrical S;
electrical Gi;

// Constants

`define e 1.6021765e-19    // Electron charge [C]
`define hs 1.054571726e-34 // Planck constant (reduced) [J.s]
`define hs_eV 6.582119e-16 // Planck constant (reduced) [eV.s]
`define vf 1e6             // Fermi velocity [m/s]
`define Eo 8.854e-12       // Vacuum permittivity
`define pi 3.14159265

// Parameters taken from CVD-GFET implemented in DOI: 10.1021/acsami.6b05791

parameter real L = 60e-9;      // Length (m)
parameter real W = 20e-6;      // Width (m)
parameter real Nf = 29e15;     // Net acceptor and donnor doping [1/m^2]
parameter real TOX = 8e-9;     // Top dielectric thickness (m)
parameter real ER =  5.65;     // Top dielectric relative permittivity
parameter real U = 450.0;      // Low field mobility [cm^2/V]
parameter real hs_w = 56e-3;   // Surface phonon energy of the substrate [eV]
parameter real delta = 200e-3; // Inhomogeinity of electrostatic potential [V]
parameter real Rgs = 0;        // Charging resistance (ohm)

// Functions
```

```
analog function real integ_1;
	input z,B,C,sig;
	real z,B,C,sig;

	begin
		integ_1 = -1.0/C*(   3.0*pow(C,4)  -  8.0*C*pow(  (  pow(C,2.0)  +  4*B*z*sig  )  ,  1.5  )  +
48.0*pow(B,2.0)*pow(z,2.0) + 48.0*B*pow(C,2.0)*z*sig  )/(96.0*pow(B,2.0)*`e*sig);
	end

endfunction

analog function real integ_2;
	input z,B,C,sig;
	real z,B,C,sig;

	begin
		integ_2   =   -(3.0*pow(C,4.0)   -   8*C*pow(   (pow(C,2.0)   +   4*B*z*sig),   1.5   )   +
48.0*pow(B,2.0)*pow(z,2.0) + 48*B*pow(C,2.0)*z*sig)/(96*pow(B,2.0)*C*`e);
	end

endfunction

// Main function

real b;
real c;
real x_0;
real x_ds;
real x_b;
real F_0;
real F_ds;
real F_b;

real U_m;
real B;
real C;
real n_puddle;
real vgs;
real vds;
real z1;
real z2;
real sig;
real out_z1,out_z2;
real res_z1,res_z2;
real integral,area;
real n_puddle_vds;
real NUM,DEN,DEN2;
real w;

real Eav;
real QCH;

real ids;
real ids_w;

real Cgs;
real Cgd;
```

```
real Cgg;
real gm_int;
real gds_int;
real ft_int;

	analog begin

		U_m = U/10000.0;
		B = pow(`e,3.0)/( `pi*pow((`hs*`vf),2.0) );
		C = `Eo*ER/TOX;
		n_puddle = pow(delta,2.0)/( `pi*pow(`hs_eV,2.0)*pow(`vf,2.0) );
		vgs = V(G,S);
		vds = V(D,S);

		if (abs(vds) == 0) begin
			vds = vds + 1e-6;
		end

		if (abs(vgs) == 0) begin
			vgs = vgs + 1e-6;
		end

		// IDS current calculation

		z1 = C*(vgs) + `e*Nf;
		z2 = C*(vgs - vds) + `e*Nf;

		if (z1 >= 0) begin
			sig = 1.0;
		end else begin
			sig = -1.0;
		end

		out_z1 = integ_1(z1,B,C,sig);
		res_z1 = integ_2(z1,B,C,sig);

		if (z2 >= 0) begin
			sig = 1.0;
		end else begin
			sig = -1.0;
		end

		out_z2 = integ_1(z2,B,C,sig);
		res_z2 = integ_2(z2,B,C,sig);
		integral = out_z2 - out_z1;
		area = res_z2 - res_z1;
		n_puddle_vds = n_puddle*vds;
		NUM = integral + n_puddle_vds;

		// Denominator calculation

		w = hs_w/`hs_eV;
		b = -2*C;
		c = pow(C,2.0)+ `e*n_puddle*4*B;
		x_0 = sqrt(pow(C,2.0)+4*B*C*abs(vgs));
		x_ds = sqrt(pow(C,2.0)+4*B*C*abs(vgs-vds));
		x_b = C;
```

```
		F_0			=			2*sqrt(pow(x_0,2.0)+b*x_0+c)*((-
3)*pow(b,2.0)+2*b*x_0+8*(c+pow(x_0,2.0)))+3*(pow(b,3.0)-
4*b*c)*ln(abs(b+2*x_0+2*sqrt(pow(x_0,2.0)+b*x_0+c)));
		F_ds			=			2*sqrt(pow(x_ds,2.0)+b*x_ds+c)*((-
3)*pow(b,2.0)+2*b*x_ds+8*(c+pow(x_ds,2.0)))+3*(pow(b,3.0)-
4*b*c)*ln(abs(b+2*x_ds+2*sqrt(pow(x_ds,2.0)+b*x_ds+c)));
		F_b			=			2*sqrt(pow(x_b,2.0)+b*x_b+c)*((-
3)*pow(b,2.0)+2*b*x_b+8*(c+pow(x_b,2.0)))+3*(pow(b,3.0)-
4*b*c)*ln(abs(b+2*x_b+2*sqrt(pow(x_b,2.0)+b*x_b+c)));

		if (vds>0) begin

			if (0<vgs && vgs<vds) begin
			DEN = L + U_m*sqrt(`pi/(4*B*`e))/(2*B*C*w*48)*abs(F_0 + F_ds -2*F_b);
			end else  begin
			DEN = L + U_m*sqrt(`pi/(4*B*`e))/(2*B*C*w*48)*abs(F_0 - F_ds);
			end

		end if(vds<0) begin

			if (vds<vgs && vgs<0) begin
			DEN = L + U_m*sqrt(`pi/(4*B*`e))/(2*B*C*w*48)*abs(F_0 + F_ds -2*F_b);
			end else  begin
			DEN = L + U_m*sqrt(`pi/(4*B*`e))/(2*B*C*w*48)*abs(F_0 - F_ds);
			end

		end

		DEN2 = DEN - L;
		ids = (`e*U_m*W*NUM/DEN);
		ids_w = ids/W;

		// Intrinsic capacitances calculation

		Eav = vds/L;
		QCH = `e*W/Eav*(-area + n_puddle_vds);

		// Assignment of results

		Cgs = abs(ddx(QCH, V(G)));
		Cgd = abs(ddx(QCH, V(D)));
		Cgg = Cgs + Cgd;
		V(G,Gi) <+ I(G,S)*Rgs;

		I(D,S) <+ ids;
		I(G,S) <+ Cgs*ddt(V(Gi,S));
		I(G,D) <+ Cgd*ddt(V(G,D));

		// Figures of Merit

		gm_int = ddx(ids, V(G));
		gds_int = ddx(ids, V(D));
		ft_int = abs(gm_int/Cgg)/(2*`pi);
	end
endmodule

// GFET14 model end
```

Appendix B: Derived Publications and Theses

Below all the publications where the author has been contributing during this PhD are enlisted:

Journal Publications =>

Attention¡¡

For copyright reasons, pages 96 to 133 of the thesis, containing the texts mentioned above, should be consulted at the editor's web

I. **M. Iannazzo**, V. Lo Muzzo, S. Rodriguez, H. Pandey, A. Rusu, M. C. Lemme, and E. Alarcon, "Optimization of a Compact I-V Model for Graphene-FETs: Extending Parameter Scalability for Circuit Design Exploration," *IEEE Transactions on Electron Devices (TED)*, vol. 62, no. 11, pp. 3870–3875, November 2015.

http://ieeexplore.ieee.org/document/7302127/

II. **M. Iannazzo**, M. C. Lemme, and E. Alarcon, "Correspondence Author's Reply to 'Comments on "Optimization of a Compact I-V Model for Graphene-FETs: Extending Parameter Scalability for Circuit Design Exploration"' S. Frégonèse and T. Zimmer," *IEEE Transactions on Electron Devices (TED)*, vol. 63, no. 5, p. 2226, May 2016.

http://ieeexplore.ieee.org/document/7448391/

III. S. Abadal, **M. Iannazzo**, M. Nemirovsky, A. Cabellos-Aparicio, H. Lee, and E. Alarcon, "On the Area and Energy Scalability of Wireless Network-on-Chip: A Model-based Benchmarked Design Space Exploration," *IEEE/ACM Transactions on Networking (TON)*, vol. 23, no. 5, pp. 1501–1513, October 2015.

http://ieeexplore.ieee.org/document/6847751/

IV. H. Pandey, J. D. Aguirre Morales, S. Kataria, S. Fregonese, V. Passi, **M. Iannazzo**, T. Zimmer, E. Alarcon, M. C. Lemme, "Enhanced Intrinsic Voltage Gain in Artificially Stacked Bilayer CVD Graphene Field Effect Transistors," *Annalen der Physik Journal*. Submitted and under review.

http://onlinelibrary.wiley.com/doi/10.1002/andp.201700106

V. R. Jove-Casurellas, C. Araguz, P. Via, A. Solanellas, A. Amezaga, D. Vidal, J. F. Muñoz, M. Marí, R. Olive, A. Saez, J. Jane, E. Bou-Balust, **M. Iannazzo**, S. Gorreta, P. Ortega, J. Pons-Nin, M. Dominguez, E. Alarcon, J. Ramos, A. Camps, "3Cat-1 Project: A Multi-payload CubeSat for Scientific Experiments and Technology Demonstrators," *European Journal of Remote Sensing*, vol. 50, no. 1, p. 1274568, February 2017.

http://www.tandfonline.com/doi/abs/10.1080/22797254.2017.1274568

Conference Publications =>

A. **M. Iannazzo**, E. Alarcón, H. Pandey, V. Passi, and M. C. Lemme, "CVD Graphene- FET based Cascode Circuits: A Design Exploration and Fabrication towards Intrinsic Gain Enhancement," *Proceeding of the 46th European Solid-State Device Research Conference (ESSDERC)*, pp. 244–247, September 2016.

http://ieeexplore.ieee.org/document/7599631/

B. **M. Iannazzo**, V. Lo Muzzo, S. Rodriguez, A. Rusu, M. C. Lemme, and E. Alarcon, “Design Exploration of Graphene-FET based Ring-oscillator Circuits: A Test-Bench for Large-Signal Compact Models,” *Proceedings of the 2015 IEEE International Symposium on Circuits and Systems (ISCAS)*, pp. 2716–2719, May 2015.

http://ieeexplore.ieee.org/document/7169247/

C. S. Abadal, A. Mestres, **M. Iannazzo**, J. Sole-Pareta, E. Alarcon, and A. Cabellos-Aparicio, “Evaluating the Feasibility of Wireless Networks-on-Chip Enabled by Graphene,” *Proceedings of the 2014 International Workshop on Network on Chip Architectures*, pp. 51–56, December 2014.

https://dl.acm.org/citation.cfm?id=2685345

D. F. Pasadas, D. Jimenez, **M. Iannazzo**, and E. Alarcon, “Capacitance Compact Modelling of Four-terminal Graphene-FETs Preserving Charge Conservation: A Circuit-oriented Device Model Benchmark,” *2015 Imagine Nano Conference*, March 2015.

E. H. Pandey, S. Kataria, V. Passi, **M. Iannazzo**, E. Alarcon, and M. C. Lemme, “Improved Voltage Gain in Mechanically Stacked Bilayer Graphene FETs,” *Proceedings of the 2016 Joint International EUROSOI Workshop and International Conference on Ultimate Integration on Silicon (EUROSOI-ULIS),* pp. 143–146, January 2016.

Co-Supervised Master Theses =>

[α] Alberto Saez, “Dual Payload Low-Power Embedded System for Characterization of Space Effects in Wireless-Power-Transfer (WPT) and Graphene-FET Technologies,” Defended in July 2015. Supervised by Elisenda Bou, **Mario Iannazzo** and Prof. Eduard Alarcón.

[β] Valerio Lo Muzzo, “Graphene-FET Large-Signal Modeling for Analog-Circuit Design,” Defended in December 2014. Supervised by **Mario Iannazzo** and Prof. Eduard Alarcón.