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To my mother for teaching me everything, making mathematics beautiful, and for all she has done for me,
and
To my father for believing me, motivating me and for being there in every step I took.

The sun will shine someday.

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Abstract

The increasing demand for wireless products to be part of our daily lives brings the need for longer battery lifetime, smaller size and lower cost. To increase battery lifetime, high efficiency power amplifiers (PAs) are needed; To make them smaller, integration or reconfiguration is aimed and to reach lower costs, technologies such as CMOS are final goals. However integration of high efficiency PA in CMOS is challenging due to the technology limitations which restricts the achievable output power and efficiency of the PA. In order to bring solutions for the above-mentioned requirements, in this thesis novel reconfigurable class-F PAs, frequency-reconfiguration, CMOS integration, impedance-reconfiguration and CMOS-MEMS implementation are addressed.

Starting with a single frequency operation, a novel class-F PA for mobile applications is proposed in which with a proper harmonic tuning structure the need for extra filtering sections is eliminated, achieving an excellent harmonic-suppression level. This topology uses transmission lines and is developed to cover multiple frequency bands for purpose of global coverage with aim of size reduction. Three novel frequency reconfigurable PAs are proposed using MEMS and semiconductor switches to accomplish class-F operation at two frequencies. The main novelty of this structure is that the reconfiguration is done not only at fundamental frequency but also at harmonics with reduced number of tuning elements. Moreover, by proper placement of the switches in the stubs, the maximum voltages over the switches are minimized. The proposed structure overcomes the narrow band performance of class-F, giving an efficiency more than 60% over a 225 MHz and 175 MHz bandwidth at 900 MHz and 1800 MHz respectively. Measurement results showed high performance at both frequency bands giving 69.5% and 57.9% PAE at 900 MHz and 1800 MHz respectively.

A novel CMOS class-F PA is proposed that controls up to the 3^{rd} harmonic and can adapt to load variations due to the effect of the human body on mobile phones. It enables the integration of the PA with other devices in a single chip leading to better matching, higher performance, lower cost and smaller size. In addition, it achieves load impedance reconfigurability by using impedance tuner in its output network and by proper tuning of the network, effects of load variation on the performance are compensated. Two designs at 2.4 GHz have been done using either MOS varactors or MEMS variable capacitors as tuning devices. The design using MOS varactors show a maximum measured values of 26% PAE and 19.2 dBm output power for 50Ω load. For loads other than 50Ω an improvement of 15% for PAE and 4.4 dB for output power is obtained in comparison to non-tuned one. The second design is done using MEMS variable capacitors integrated in CMOS technology through a mask-less post-processing technique. Simulations results for 50Ω load show a peak PAE of 32.8% while delivering 18.2 dBm output power.

Contents

1

Chapter 1

Introduction

This chapter describes the motivation of the study that was carried out within this doctoral activity and the main objectives to be fulfilled. The structure of this doctoral dissertation is presented to point out specifically what are the main contributions of each chapter and how they are linked to the fundamental goals.

1.1 Motivation

There is an ever-increasing demand for wireless communication products such as cellular phones, wireless local area networks (WLAN), and wireless computer peripherals to be part of our daily lives. Among the whole transmitter building blocks, power amplifiers (PAs) are the most critical blocks because of their high power consumption. Advances in wireless systems demand longer battery lifetime, smaller size and lower cost, bringing a great need for PAs to be highly efficient, work under different conditions and in the case of mobile handsets, to be integrated with other devices in a single chip [1]. If the efficiency of the PA is not high, it results in short battery lifetime of the device. In addition, dissipated power transforms to heat, which can bring reliability issues and degrade the lifetime of the PA itself.

High efficiency is achieved at the expense of linearity and finding a trade-off between the two is one of the most challenging aspects of the PA design. In wireless Global Systems for Mobile Communications (GSM) standard, nonlinearity of amplifiers is not an issue since it uses Gaussian Minimum Shift Keying (GMSK) constant envelope modulation. With advances in wireless systems, the usage of Quadrature Amplitude Modulation (QAM) or Orthogonal Frequency Division Multiplexing (OFDM) are essential to maximize data rates in a limited bandwidth. However, in both cases the transmitted signal exhibits both amplitude and phase information, which are normally amplified by linear and inefficient amplifiers. In addition to that, transmitted signal exhibits high peak-to-average power ratio (PAPR) which hampers the efficiency of linear amplifiers and results in PAs operating at an average output power well below its optimum value. One method to increase the efficiency of a linear PA is envelope tracking (ET) technique where it maximizes the efficiency versus output power by constantly adjusting the power supply voltage. Alternatively, Kahn envelope elimination and restoration (EER) technique [2] is a method for linearity enhancement of a high efficiency PAs which enables the use of high efficiency PAs in linear systems.

In mobile communication networks, it is desired that RF front ends and consequently PAs can adapt to different conditions that arise in wireless applications such as a change in bias, frequency, load impedance or power. The increasing demand of wireless devices for global coverage results in the need for systems to cover multiple frequency bands. To achieve the multi-band coverage, multi-band transceivers, and consequently multi-band PAs are needed. Another condition is load impedance variation which happens when a user holds the mobile phone and the strong interaction between head, hand, and antenna causes a change in antenna impedance [3, 4] leading to a reduced performance. Using reconfigurable matching networks (MN) instead of a fixed matching network brings new opportunities to recover the performance in terms of efficiency and power while operating

under different conditions. The reconfiguration is usually achieved by use of varactors or switches.

To enable integration of all mobile circuitry in a single unit, the use of complementary metal oxide semiconductor (CMOS) is inevitable. CMOS technology offers high integration level with low cost. Although most handset components are integrated in CMOS technology, the PA is still the most difficult block to implement in CMOS [5] due to the low breakdown voltage, the conductive substrate, and the sheet-resistance of the poly silicon that limit the output power and efficiency of the PA. However, by integration of a PA with other devices on a single chip better matching and higher performance will be achieved in addition to lower cost and smaller size.

Reconfigurable matching networks incorporate integrated varactors or switches which can be implemented either using CMOS components or microelectromechanical system (MEMS). RF MEMS devices have an intrinsically low loss and are compatible with high-frequency fabrication methods. Reconfigurable MNs that incorporate MEMS switches or variable capacitors show the least degradation of overall performance in the PA and are most widely used in hybrid circuits. To use MEMS devices in CMOS technology, they can be fabricated on a different substrate and flip-chip bonded onto a CMOS chip [6], however, flip-chip bonding involves relatively high costs. A single-chip implementation of MEMS devices integrated in CMOS [7] eliminates the problems of hybrid bonding and packaging parasitics hence improving performance and lowering the cost.

In order to achieve high efficiency, the switching PAs [8] have a minimum overlap between the drain current and voltage waveforms, resulting in lower power dissipation than linear amplifiers. Among the high efficiency PA classes, the class-E PA is attractive due to its simple load network. In addition, class-E overcomes the device parasitic capacitance problem of class-D. However, class-E PA suffers from voltage stress in the device output which, depending on the application might be harmful. The voltage swing on the drain of a class-E PA can reach up to 3.6 times the drain supply voltage V_{DD}, while only 2 times V_{DD} is possible for a class-F PA, therefore, for the implementation on low breakdown technologies such as CMOS, a class-F PA is more suitable despite having a more complex load network.

1.2 Objectives

The focus of this dissertation is to provide different topologies to implement a reconfigurable high efficiency class-F PA. After a general review of different classes of PAs and its fundamentals, high efficiency class-F PAs are studied and a new topology is proposed. The major focus of this thesis is on reconfiguration techniques provided for class-F PAs. The work has focused on two reconfiguration types: *frequency* and *load*

impedance. The proposed reconfigurable structures control up to 3^{rd} harmonic with a proper harmonic tuning network. The integrated and reconfigurable PA design in CMOS is intended for Bluetooth application which brings new opportunities for PAs to be integrated with other components in the handset. The works of this research include:

- **Design, development, and fabrication of novel single frequency high efficiency class-F PA:** A single frequency class-F PA topology is proposed and designed to meet requirements of high efficiency, high power, and high harmonic rejection while matched to 50Ω input and output impedance. The proposed topology provides a very low total harmonic distortion (THD) which eliminates the need for extra filtering section. Two boards are designed and fabricated at two different frequencies and high performance was achieved from each board while they fulfilled the matching requirement of $|S_{11}|$ and $|S_{22}|$ being less than -10 dB for 50Ω source and load impedance.

- **Design, development, and fabrication of novel frequency reconfigurable class-F PAs:** A complete study of frequency reconfiguration and its structure is developed for class-F PA with the requirements of providing high efficiency and high power at each frequency band. The proposed dual-band frequency PA switches between two different frequency bands while maintaining high efficiency and power at each band. Frequency-reconfiguration is achieved by input and output reconfiguration using Single Pole Single Throw (SPST) and Single Pole Double Throw (SPDT) switches. Three different reconfigurable circuits are developed using semiconductor either Hittite switches or MEMS switches. The MEMS switches showed higher power capability and lower loss resulting in a higher performance of the PA.

- **Design, development, and implementation of a novel impedance reconfigurable class-F PA in standard CMOS technology:** A new reconfigurable class-F PA is proposed and designed at 2.4 GHz to meet several requirements such as adjustment of a variable load impedance, small size, high efficiency and enough power for the Bluetooth application. This PA addresses the effect of load variation which is caused by proximity effect of head and hand on the cellphones. Impedance-reconfiguration is achieved by reconfiguring the output network using an impedance tuner. The impedance tuner incorporates two MOS variable capacitors and also provides the proper harmonic termination at fundamental frequency and harmonics. The proposed structure proves the ability of the PA to compensate for the drop of the overall performance by means of tuning varactors.

- **Design, development, and implementation of a novel impedance reconfigurable class-F PA in CMOS-MEMS technology:** This reconfigurable class-F PA has the same topology as the previous reconfigurable class-F PA and is intended for impedance load variation. However, this design incorporates MEMS analog variable capacitors instead of MOS variable capacitors with the intention to compare the PA with two different kinds of variable components. The MEMS capacitors are monolithically integrated in CMOS without the need for extra mask layer. The results of this PA are unavailable since it is under post processing. It is expected that this PA gives higher output power since MEMS switches have lower loss compared to MOS varactors.

1.3 Thesis Outline

This doctoral dissertation is organized in seven chapters. The **first chapter** introduces the motivation, objective and outline of this thesis. **Chapters 2** to **7** contain the main contributions of this doctoral research as following:

- **Chapter 2** provides state of the art of power amplifiers. It focuses on class-F PA structures, multi-band operation, and impedance reconfiguration. A literature review of class-F PAs in CMOS is also provided.
- **Chapter 3** gives a general overview of PA fundamentals, definitions and different classes of operation, going into detail on class-F PA.
- **Chapter 4** new structure for class-F PA is proposed and two fixed single frequency class-F PAs are designed, fabricated and measured, one at 900 MHz and one at 1800 MHz.
- **Chapter 5** focuses on the change in the frequency band. It describes and presents the topology for three different frequency-reconfigurable class-F PAs working at two frequencies, 900 MHz and 1800 MHz. The discrete PAs are designed and fabricated on a PCB which can switch between two frequencies independently. Measurement results and comparison with simulations are provided.
- **Chapter 6** describes and presents a topology for impedance reconfiguration. The change in load impedance is done aiming Bluetooth application and the reconfigurable PA is designed and integrated in TSMS 0.18μ-CMOS technology.
- **Chapter 7** describes and presents a topology for impedance reconfiguration. The change in load impedance is done aiming Bluetooth application and the reconfigurable PA is designed and integrated in TSMS 0.18μ-CMOS technology.

The capacitors in this design are CMOS-MEMS capacitors that are released by post-processing without the need for extra mask.

And finally, the document is concluded in **chapter 8**, summarizing the main results and contributions presented.

2

Chapter 2
State of The Art

This chapter is dedicated to the state of the art in power amplifiers, with special focus on reconfigurability, both on frequency and on power.

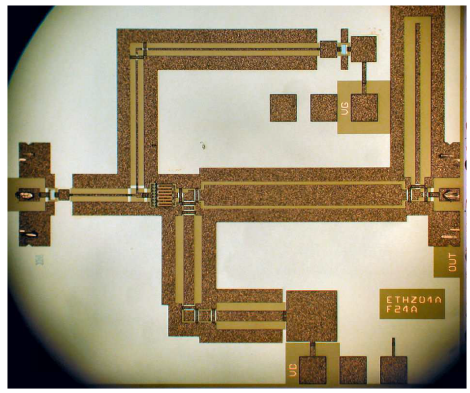


Figure 2.1: Chip microphotograph of the class-F PA MMIC using GaAs pHEMT presented in [9].

2.1 High Efficiency Class-F PAs

The choice of PA class and also design components depends on the operating frequency and the active device technology. At microwave frequencies, transmission line (TL) networks are preferred because implementing lumped element multi-resonators at these frequencies is difficult. Alternatively, for integration approaches, lumped elements should be used since TL networks consume a large area at this frequency. However, reaching up to millimeter-wave frequency, even integrated matching networks (MN) are preferred to be implemented using TL [9], not only because lumped elements exhibit important parasitics but also because TL can be very small due to the wavelength at these frequencies (Fig. 2.1).

Class-E and Class-F (and their inverse classes) have been the main core of high efficiency PAs in recent years. As explained before in introduction, class-E has a simple load network compared to class-F PA, but it suffers from high voltage swing at its drain, which can reach up to 3.6 times V_{DD} while this value is only 2 times V_{DD} for class-F PAs. This high voltage swing brings reliability concerns for low breakdown technologies. Therefore high breakdown technologies such as GaN and LDMOS can be used for both class-E and class-F PAs, but for implementation on low breakdown technologies such as CMOS a class-F PA is a better option. Therefore, in this thesis the focus has been on class-F PAs and with the aim of integration on CMOS technology, the following state of the art is presented. The literature review is focused on single frequency class-F PAs based on TL/discrete implementation and lumped element integration in CMOS technology. In section 2.2 multi-band class-F PAs are divided into three groups of *concurrent multi-band PAs*, *Broadband PAs*, and *Frequency reconfigurable PAs*. Since part of this thesis is devoted to PA design and load effect compensation using

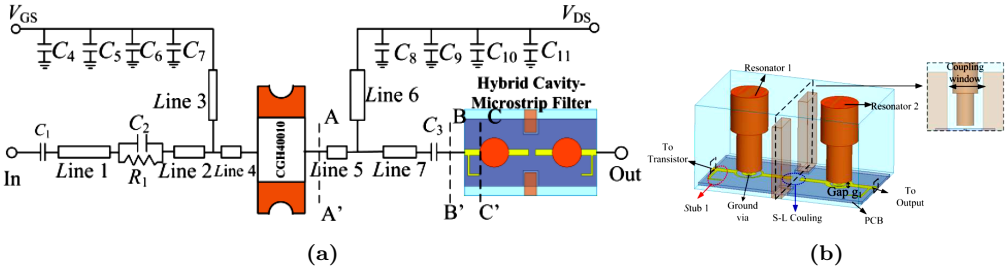


Figure 2.2: (a) A class-F PA incorporating hybrid cavity-microstrip band pass filter, and ((b)) 3D structure of Hybrid cavity-microstrip BPF configuration [10].

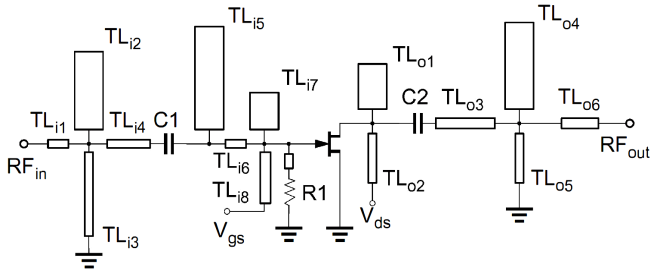


Figure 2.3: Schematic of the class-F PA presented in [11].

reconfigurable output matching network (OMN) using an impedance tuner, in section 2.3 impedance tuners and different structures have been explained.

Class-F and its dual, inverse class-F (Class-F^{-1}), have been the focus of many works with high efficiency requirements resulting to many reported high efficiency class-F PAs with hybrid implementation in the literature [10–20]. The output filter of the class-F PA has also been proposed by using hybrid cavity-microstrip band-pass-filters (BPF) [10] bringing advantages such as heat sinking and easy integration with transistors or by generalized-Chebyshev bandpass filter [11] to work over a particular bandwidth. Both approaches are shown in Fig. 2.2 and Fig. 2.3 respectively. A full study of the two classes in terms of the optimum load impedance, output power, and efficiency according to the conduction angle are provided by [12] and [13].

As the RF front-end is continuing to grow in complexity, there is a great need to integrate the PAs with other devices on a single chip. Conventional PAs for GSM cell phones tend to be designed using separate chips made of GaAs pHEMT [9, 21, 22], SiGe bipolar transistors [23, 24] or GaN MMIC [25] with additional discrete components that do not integrate well and increase cost notably. Nowadays, most handset components from baseband to receiving path are implemented in CMOS technology, except PA block.

To enable integration of all mobile circuitry in a single unit, the use of CMOS [26–34]

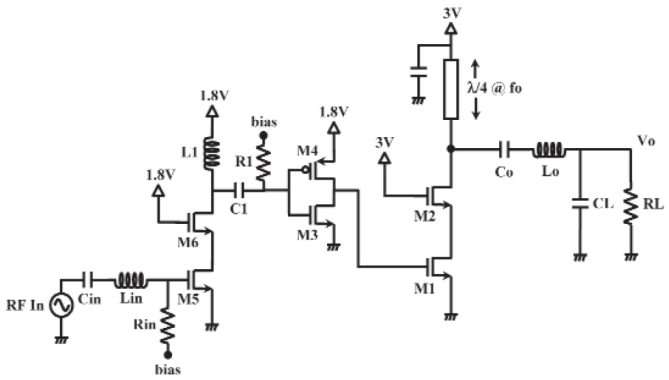


Figure 2.4: A lumped element class-F PA fully integrated in CMOS, using combination of thin and thick transistors to increase the power capability [29].

or BiCMOS technology [35, 36] are ultimate goals because of their low cost and high level of integration. However, the PA is considered the most difficult block to implement in CMOS both as a component and as part of the final application due to inherent limiting technology characteristics from CMOS, to say: low breakdown voltage, the conductive substrate and the high sheet-resistance of the poly silicon. These characteristics pose a challenge that limits the output power, efficiency, linearity, and gain of the PA.

The low-resistivity of the substrate in CMOS technology is the main factor for having a low quality factor (Q) of on-chip inductors and transformers thus increasing the power losses and lowering the performance at higher operating frequencies [37]. An alternative approach is to implement low loss MNs using off-chip components such as discrete passives [26], transformers [38, 39] or bond wires as high-Q inductors [26–28]. However, these are not fully integrated solutions and are not suitable for the purpose of fully monolithic handsets.

In integrated circuit (IC) design under millimeter-wave, lumped element MNs are inevitable for reducing the die area and cost. As CMOS works under low supply voltage, techniques such as power combining [40, 41] and stacked transistors [42] are used to increase the output power. To overcome the low breakdown voltage issue of CMOS transistors, a cascode structure using a mixture of thin and thick gate oxide transistors is presented in [29]. The combination of a thin and a thick transistor, shown in Fig. 2.4, enables the PA to achieve higher output power in deep sub-micron CMOS technology without having issues with breakdown voltage.

For better results of CMOS designs, layout parasitics, specifically the ones from metal interconnections, should be calculated in advance [30]. The circuit diagram of a fully integrated 5 - 6 GHz class-F PA in 0.18μm CMOS presented in [33] and its fabricated

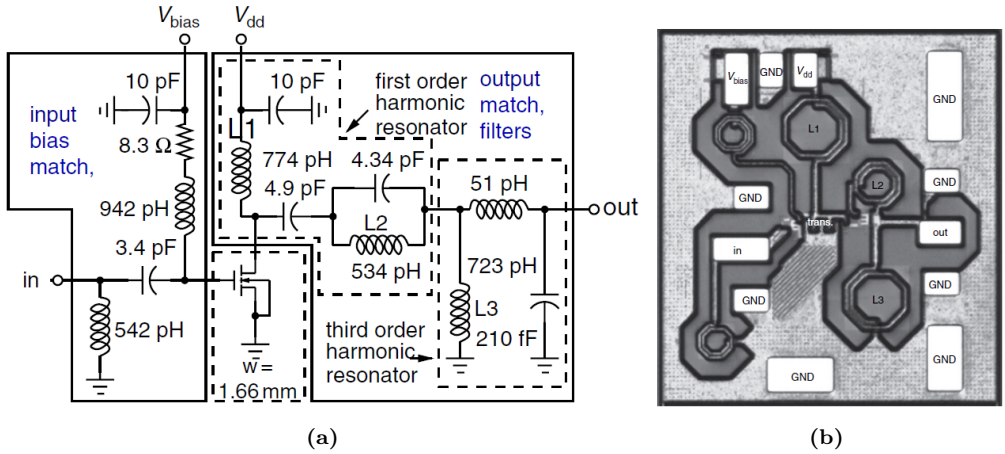


Figure 2.5: ((a))A lumped element class-F PA for CMOS integration, and ((b)) fabricated circuit [33].

circuit is shown in Fig. 2.5.

2.2 Multi-band Operation

The increasing demand of wireless devices for global coverage results in the need for systems to cover multiple frequency bands. To achieve the multi-band coverage, multi-band transceivers and multi-band PAs are needed. There are several works on multi-band operation in envelope tracking amplifiers [43, 44] and Doherty amplifiers [39, 45–47] where they incorporate high efficiency multi-band PAs in their configurations. A power amplifier is an important part of RF systems and it is desired that the PA could be adjusted according to the application and external conditions.

Achieving multi-band operation for highly efficient amplifier circuits such as class-F is more challenging than in linear ones because in highly efficient PAs not only correct fundamental load matching is needed, but also a proper harmonic impedance termination should be provided for each of the bands. In this section literature addressing that topic will be reviewed.

A conventional approach for multi-band operation is to use multi-branch designs which use multiple circuits in parallel, each of them designed at a single-frequency. However, due to the passive and active elements redundancy, this approach results in a large area and thus becomes more expensive. The occupied area is a critical requirement for PA either in the base station or handsets and it is desired to have as small area as possible, not only for cost reasons but also for miniaturization purposes. To avoid a costly and

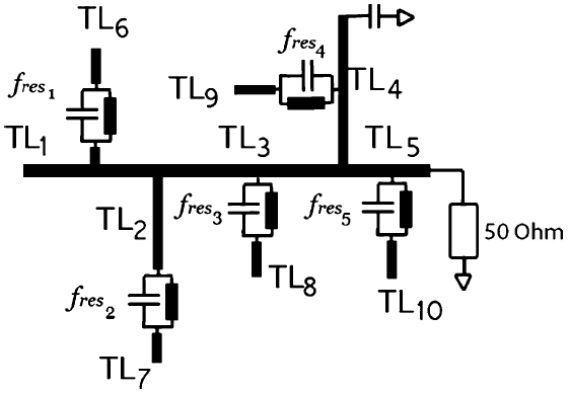


Figure 2.6: Concurrent dual-band class-F PA proposed in [53].

large multi-branch design, there are three ways to realize multi-band systems, namely *Concurrent multi-band PAs*, *Broadband PAs*, and *Reconfigurable PAs*.

2.2.1 Concurrent Multi-band PAs

Concurrent multi-band MNs achieve matching concurrently in multiple individual frequency bands without the use of neither switch nor reconfigurable elements. The reported high efficiency concurrent PAs are often dual band [48–50] or triple band [51] PAs. The methodology for a multi-band passive network is well explained by Colantonio in [52] where also a dual-band PA design that matches the impedance at fundamental frequency and harmonics is provided.

There are different multi-band class-F PAs reported using slightly different approaches [53–55]. Negra in [53] uses resonators at different frequencies to obtain concurrent dual-band and multi-harmonic operation. The termination network, shown in Fig. 2.6, requires 5 resonators. Nikandish in [54] proposes a harmonic termination ladder technique which can be used for termination of an arbitrary number of harmonics in single-band or concurrent multi-band class-F PAs, shown in Fig. 2.7. Kui Zhu in the other hand, in [55] proposes to simplify the termination network, at the expense of reduced generality.

The proposed class-F PA in [56], depicted in Fig. 2.8, operates at two frequencies simultaneously by using a combination of class-F mode for one band and inverse class-F mode for the other band. Although this is a very interesting approach, its main limitation is on the band-frequencies ratio, where a ratio of 1:1.5 is required.

Another dual-band class-F PA is implemented in [57] using composite right/left-handed transmission line (CRLH-TL). The illustrated approach in Fig. 2.9

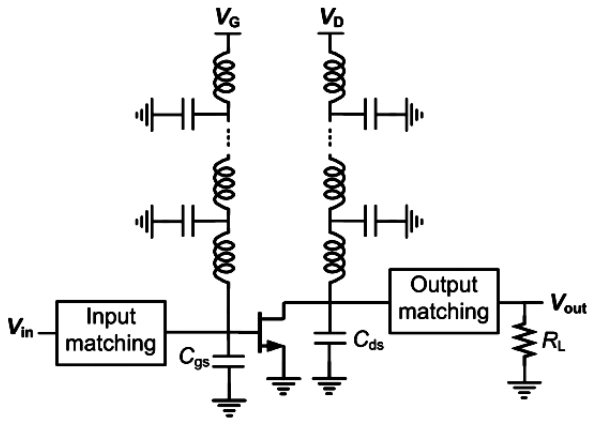


Figure 2.7: High-efficiency class-F PAs proposed in [54].

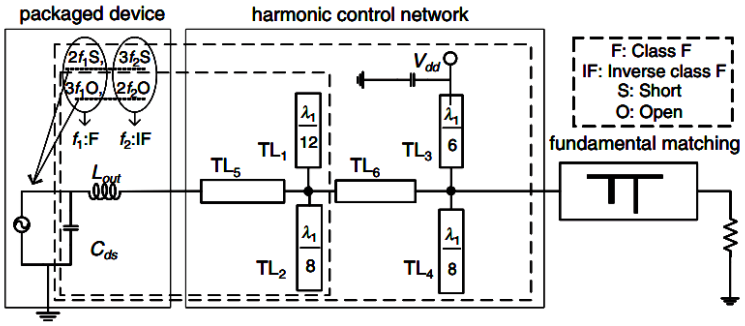


Figure 2.8: Dual-band approach by combination of class-F mode for one band and inverse class-F mode for the other band proposed in [56].

shows an interesting characteristic as it can create dual-band harmonic trap which can be used in dual-band PAs.

2.2.2 Broadband PAs

Broadband saturated power amplifiers have been reported as part of multi-band [44, 58, 59] and wide-band [60] Envelope Tracking Transmitters and in Doherty amplifiers [45, 46]. A methodology for designing broadband PAs based on second-harmonic impedance manipulation is provided in [61].

A concept called continuous-mode PA often called class-J or recently continuous class-F [62–64] and continuous inverse class-F [65] enhances the bandwidth through the use of various voltage waveforms that deliver a constant RF performance across a desired frequency band. A broadband Doherty PA based on the continuous-mode technique has

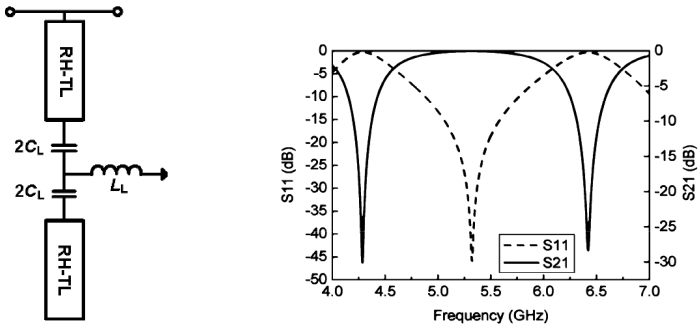


Figure 2.9: composite right/left-handed transmission line (CRLH-TL): ((a)) Model, ((b)) S-parameter response [57].

also been reported [45]. The more detailed explanation of the continuous-mode approach can be read in [66, 67].

2.2.3 Frequency Reconfigurable PAs

Concurrent multi-band and broadband circuits show a reduced performance compared to the narrow-band ones. Alternatively, reconfigurable circuits achieve working at multiple frequency bands while maintaining a good performance of narrow-band circuits. So by developing a reconfigurable structure, one can take benefits of the narrow band performance and multi-band operation at the same time.

RF PAs with reconfigurable impedance tuning networks that are aimed for multi-band operation are presented in [40, 41, 68–71]. Frequency Reconfigurable PAs are designed often for dual or triple band operation. A design methodology for multi-band reconfigurable OMN has been presented in [72]. The proposed PA depicted in Fig. 2.10 consists of two sections, one for power reconfiguration and one for frequency reconfiguration, for practical handset applications.

There have been works toward integration of multi-band transmitter and therefore multi-band PAs in CMOS [68, 73–75] and BiCMOS technologies [76–79]. With both linearity and efficiency becoming a simultaneous requirement of the PAs, more works have been done in the linearization of the class-F PA at a single frequency of operation [38, 80–83] and at multi-band operation [68, 73, 84, 85].

In [73] a partial CMOS multi-band WCDMA/LTE PA incorporating class-F PA is reported. However, the good performance is subject to implement reconfiguration via external Integrated Passive Device (IPD) in a technology that overcomes CMOS passive structure limitations.

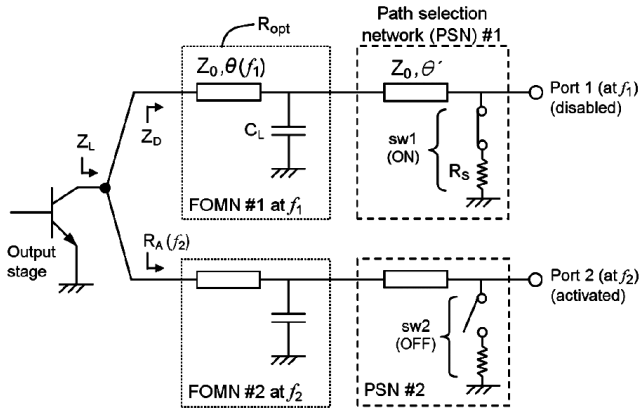


Figure 2.10: Fully integrated multi-band class-F PA presented in [72].

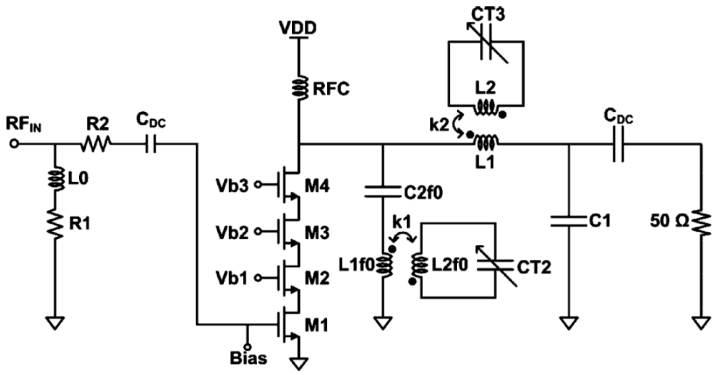


Figure 2.11: Fully integrated multi-band class-F PA presented in [68].

Recent works covered in section 2.1 show that the class-F PA can be integrated in CMOS technology, yet, among the limited number of reconfigurable class-F PAs of the current section, mostly a fully monolithic approach is not used. For example, Yin [84] proposes a class-F PA integrated in CMOS technology where the harmonic control is done off-chip, or Kim [85] incorporates off-chip OMN and feedback. One fully integrated multi-band class-F PA is presented by Sessou in [68]. The proposed class-F PA is illustrated in fig. 2.11, the reconfigurability is achieved through the use of integrated transformers and parallel capacitors.

2.3 Impedance Tuners

Another condition that is interesting in RF systems is that the PA could be adjusted according to the application and external conditions such as load impedance variation.

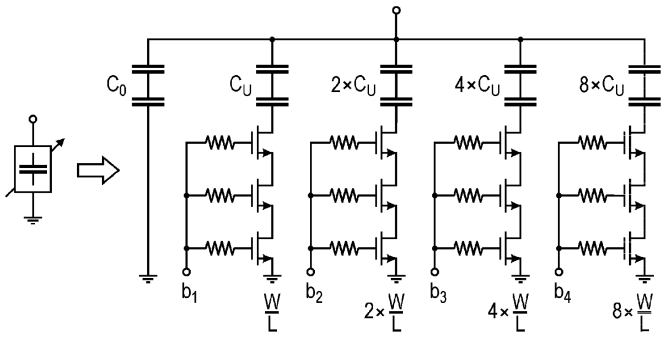


Figure 2.12: Circuit implementation of a variable capacitor presented in [86].

When a user holds the mobile phone there is a strong interaction between hand, head, and antenna which causes a change in antenna impedance [3, 4] leading to a reduced performance. As the input and output impedances of transistors vary with operating condition, it is necessary to have a tunable impedance MN. Impedance tuners on this application lead to higher efficiency and wider bandwidth, therefore, they can be found in the reconfigurable amplifiers, smart telecommunication systems, millimeter-wave instrumentation, noise parameter measurements and load-pull measurements of active devices.

Impedance tuners [40, 40, 86–96] convert the impedance values at their output to a known impedance value at their input. The tunable MN for reconfigurable RF frontends presented in [97] includes a harmonic tuning, the feature demanded in high efficiency PA design. Some other topologies for adaptive impedance tuners are presented in [86, 98]. Other works that aimed for output power control use on-chip power combiners [99], bondwires and switched capacitors [100], or a combination of an adaptive power supply and impedance tuning using varactor diodes [101]. Techniques for adaptive control of impedance MNs which provide automatic compensation of antenna mismatch are presented in [102].

Many impedance tuners achieve tuning typically using MOS varactors [88], diodes [92, 96], switches [91], and more recently MEMS devices [7, 87, 90, 95]. Semiconductor varactors have acceptable impedance coverage and handle high power up to 30 dBm at frequencies up to 5 GHz. MEMS have the lowest insertion loss and a large tuning range at frequencies up to 40 GHz, but they need a high actuation voltage and have larger switching times. A circuit implementation of capacitor bank by means of transistors presented in [86] is shown in Fig. 2.12. Different structures for an impedance tuner from the literature are provided in Fig. 2.13 and Fig. 2.14.

RF-MEMS technology is particularly attractive for the tuner integration because of

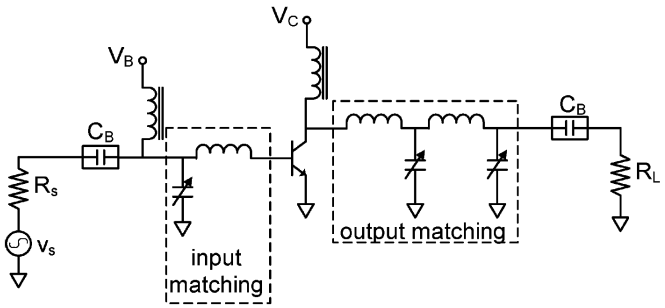


Figure 2.13: Adaptive power amplifier using impedance tuner in its input and output MNs presented in [89].

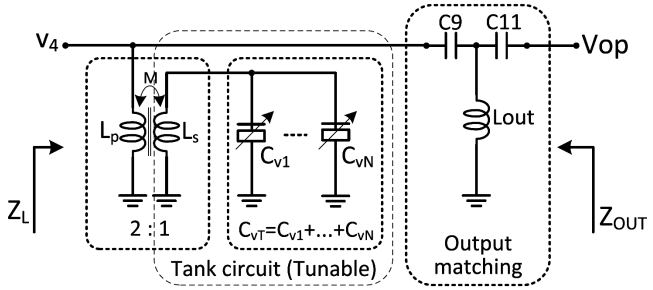


Figure 2.14: Tunable load comprising transformer and MOS-varactor bank presented in [88].

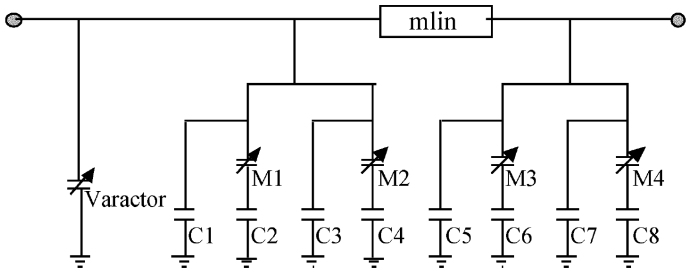


Figure 2.15: Double stub impedance tuner with four MEMS switches (M_1-M_4) of a varactor presented in [90].

the available reconfigurable devices and the high performances they exhibit. A higher impedance span can be achieved by using stubs and the higher number of stubs results in a higher impedance coverage and bandwidth. Impedance tuning MNs have been demonstrated based on double-stub [95], quad-stub [90], up to ten-stub [96]. Examples are shown in Fig. 2.15 for double stub and Fig. 2.16 for ten stub impedance tuner.

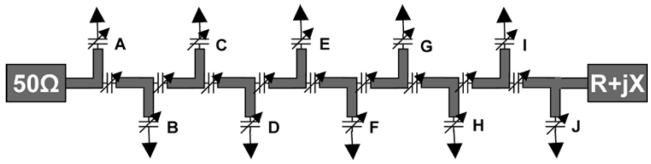


Figure 2.16: Adaptive power amplifier using impedance tuner in its input and output MNs presented in [96].

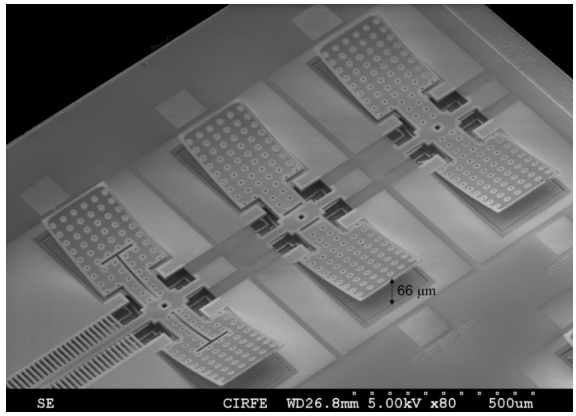


Figure 2.17: Scanning Electron Microscope (SEM) image of the fabricated CMOS RF MEMS switches in [103].

Many reconfigurable networks based on RF MEMS capacitive switches have been proposed. An example of MEMS switch fabricated in CMOS technology is shown in Fig. 2.17. An impedance tuner incorporating eight MEMS switches built in 0.35μm CMOS technology is presented in Fig. 2.18.

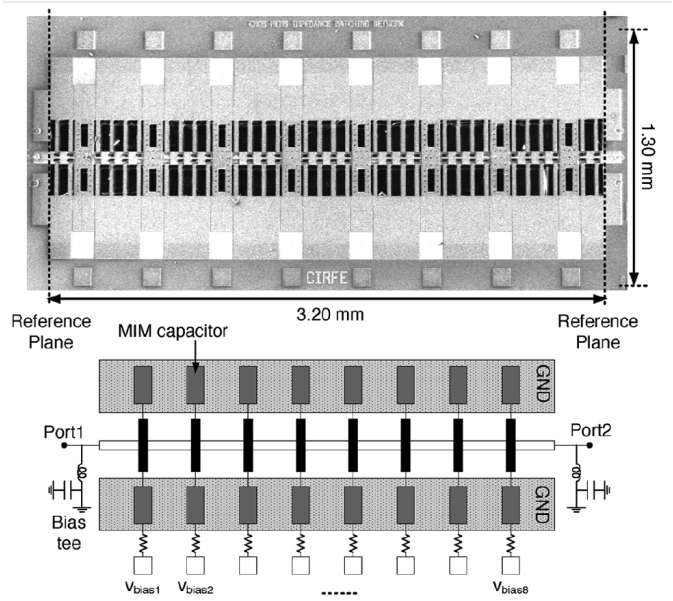


Figure 2.18: (*top*) Photograph and (*bottom*) diagram of a tunable MEMS impedance-matching network integrated in a standard 0.35μm CMOS technology [104].

3

Chapter 3

Power Amplifier Fundamentals

This chapter provides RF power amplifier fundamentals. General metrics of amplifier such as power, gain, efficiency, linearity, and stability are explained. Different classes of power amplifiers consisting linear and switched mode amplifiers are briefly described with a more detail explanation on class-F power amplifiers.

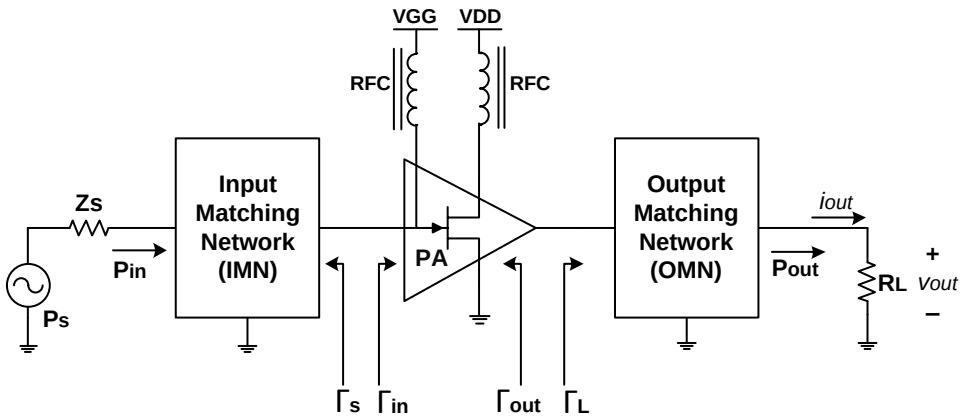


Figure 3.1: Basic power amplifier diagram.

3.1 Power Amplifier Metrics

The performance of amplifiers in this thesis are evaluated according to the metrics such as power, efficiency, and gain. Therefore it is important to define the evaluation metrics before studying the objective amplifier. For this purpose the basic circuit of Fig. 3.1 should be considered.

3.1.1 Power

Output Power (P_{out}): One of the most important characteristics of a power amplifier is to be able to deliver a certain amount of power into a load. This power is called output power or delivered power and is usually measured in dBm or watt. There are two ways to measure the power, instantaneous power and average power, which are defined in equations (3.1) and (3.2) respectively.

$$P_{ins} = p(t) = v(t) \cdot i(t) \tag{3.1}$$

$$P_{avg} = \langle P \rangle = \frac{1}{T} \int_0^T p(t)dt \tag{3.2}$$

Output power delivered at fundamental frequency can be calculated from the phasors as the following:

$$P_{fund} = \frac{1}{2} \Re \left[V_{out}|_{fund} \cdot I^*_{out}|_{fund} \right] \tag{3.3}$$

However, there are different definitions specified for it due to the behavior of amplifiers changing from linear to saturation region. Amplifier's output power is considered to have

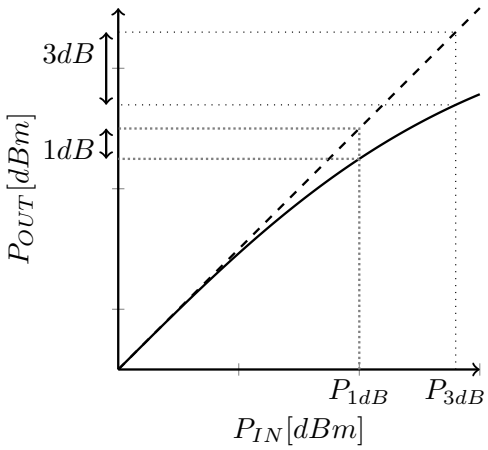


Figure 3.2: P_{1dB} and P_{3dB} definition.

a linear relation to its input power until P_{1dB}, which is the power at which output power drops 1 dB below its linear expected value. This is shown in Fig. 3.2. With the same idea, P_{3dB} is defined as the input power where the output power drops 3 dB below its linear expected value. P_{1dB} is used in literature as the point where amplifier starts to be nonlinear, while P_{3dB} is commonly used in practice to define final stage power in high power amplifiers[1].

When the amplifier has to operate with modulated signals, also the *average* power is specified.

DC Power (P_{DC}) is the power used from the power supply, in all DC terminals (for a typical MOSFET: drain and gate). By a proper implementation of bias feeding networks with RF chokes or $\lambda/4$ TL, the power supply only has to provide the average current and average voltage. The DC power is calculated as in equation 3.4.

$$P_{DC}(W) = \langle V_{drain} \rangle \cdot \langle I_{drain} \rangle + \langle V_{gate} \rangle \cdot \langle I_{gate} \rangle \tag{3.4}$$

In the case of single stage PA like the PAs in this thesis, only one gate and one drain supply are considered. Gate DC power can be neglected, as it accounts lower than 0.1% of drain power[2].

[1] Using P_{1dB} instead of P_{3dB} would lead to bigger devices (barely twice) and lower efficiency.

[2] GaN transistors have a typical maximum gate current below 1 mA/mm and gate voltage of -2V to -3V, in contrast with a drain current capability of more than 100 mA/mm and a drain voltage higher than 28V.

Input Power (P_{in}) is the RF power that is used to drive the amplifier. When using high gain linear amplifiers (gain stages typically) the input power can be neglected for efficiency calculation, as 20 dB gain means less than 1% of overall power. On the other hand, when considering high power amplifiers with a modest gain (final stages) input power is higher and it is important to consider this power, not only for efficiency calculations but also for driving requirements.

3.1.2 Gain

Gain is the ratio between output power and input power in watts or their difference in dB:

$$G(dB) = 10\log_{10}\left(\frac{P_{out}(W)}{P_{in}(W)}\right) = P_{out}(dBm) - P_{in}(dBm) \tag{3.5}$$

Gain is constant at low input power and as the input power is increased, the amplifier starts compressing and gain starts decreasing. Hence two gain calculations can be made, and they are used differently.

Small signal gain corresponds to $|S_{21}|^2$ parameter, and it is often used in signal amplifiers such as Low Noise Amplifiers (LNA) and receiving sections. As it is measured under very low input power (deep back-off) the behavior is linear, and hence cannot be extrapolated for high power amplifiers where compression effects and non-linear parasitics play a key role in amplifier's behavior.

Large signal gain (G_p) is obtained with the PA working at higher power, where non-linear effects such as non-linear capacitances and amplifier saturation take place. At low power levels, the gain is linear, but as power increases the gain decreases. Due to the non-linear behavior, simulation of G_p should be done by Harmonic Balance.

3.1.3 Efficiency

The efficiency of the PA defines how well it can deliver the required output power with minimum power dissipated in the device. So ideally it is desired to deliver all the supply power (DC power) and input power to the output. There are three different ways to define amplifier efficiency:

Drain Efficiency (η_D, DE) measures the efficiency of the amplifier in converting DC power into output RF. It neglects the power which is lost by driving the amplifier.

$$\eta_D = \frac{P_{RFout}(W)}{P_{DC}(W)} \tag{3.6}$$

Power Added Efficiency (PAE) measures amplifier efficiency considering DC power and also the input power used to drive it. Note that with high gain amplifiers ($G > 20dB$) the difference between η_D and PAE is smaller than 1%, but for a modest gain of 10 dB, the difference reaches up to 10%.

$$PAE(\%) = 100 \cdot \frac{P_{RFout}(W) - P_{RFin}(W)}{P_{DC_{tot}}(W)} = \eta_D \cdot \left(1 - \frac{1}{G}\right) \tag{3.7}$$

Overall Efficiency (OE) measures overall amplifier efficiency. It is more flexible compared to PAE because it can incorporate other supporting circuits, such as voltage regulators or digital pre-distortion (DPD).

$$\eta_O = \frac{P_{out}(W)}{P_{DC}(W) + P_{in}(W)} = \frac{P_{out}(W)}{\sum\limits_{k \neq out} P_k(W)} \tag{3.8}$$

3.1.4 Stability

Stability is one of the most important factors in the PA that should be addressed from the early stage of the design. Stability issues occur in amplifiers due to different reasons. Physically, an amplifier is unstable when it has positive feedback, or in other words, when input or output resistances are negative ($\Gamma_{in} > 1$ or $\Gamma_{out} > 1$) [105]. Oscillation can happen at low frequency or at RF frequency. If PA is unstable at low frequency this usually can be fixed by choosing a proper decoupling capacitor in the supply of the PA, for both drain and gate. However, the RF instability comes from the circuit design, therefore making it stable means changing the input and output matching networks structure and components.

Typically, the Rollett's stability factor (K), defined by equation 3.9, is used to evaluate amplifier stability. By sweeping the input signal from DC to higher frequencies, and plotting the K factor, the stability of the device can be determined.

$$\begin{cases} K = \frac{1-|S_{11}|^2-|S_{22}|^2+|\triangle|^2}{2|S_{12}S_{21}|^2} \\ \triangle = |S_{11}S_{11} - S_{12}S_{21}| \end{cases} \tag{3.9}$$

There is one stability circle for Γ_L called output stability circle and one for Γ_S called input stability circle. If $|S_{11}| < 1$ and $|S_{22}| < 1$, then the area which includes the center of the Smith Chart is stable. The μ-factor is the distance from the center of the Smith Chart to the nearest point of instability on the stability circles. The μ-factor of the load (μ') and source (μ)are respectively derived from equations 3.10 and 3.11.

$$\mu' = \frac{1 - |S_{11}|^2}{|S_{22} - S_{11}\triangle| + |S_{12}S_{21}|} \tag{3.10}$$

$$\mu = \frac{1 - |S_{22}|^2}{|S_{11} - S_{22}\triangle| + |S_{21}S_{12}|} \tag{3.11}$$

Unconditional stability: For the amplifier to be unconditionally stable it should meet $|\Gamma_{in}| < 1$ and $|\Gamma_{out}| < 1$ for all possible combination of source and load impedances and frequencies. In unilateral amplifiers ($S_{12} = 0$) fulfilling only $|S_{11}| < 1$ and $|S_{22}| < 1$ signify unconditional stability. For non-unilateral amplifiers, $K > 1$ and $|\triangle| < 1$ for all range of frequencies and all impedance values is the way to determine unconditionally stable amplifier. However the value of k-factor can not be used directly on the degree of stability, But μ' and μ have a direct relationship with how stable is the circuit. $\mu' > 1$ and $\mu > 1$ is an indication of unconditional stability and the higher value of μ' and μ means a more stable circuit.

Conditional stability: If the above conditions are met for only a certain range of frequencies or impedance values, the amplifier is called *conditionally stable*. A conditionally stable amplifier can become unstable by interactions of the bias network, and careful design is mandatory in those cases.

Stability improvement techniques: Typically when the PA is unstable, it needs a more lossy matching network in order to become stable which lowers the gain and efficiency of the amplifier. Stability can be improved by adding series or shunt resistor in the input of the active device. Stability circles that are on the left side of Smith Chart suggest stability improvement by series resistance, while stability circles placed on the right side of Smith Chart suggest adding shunt resistance. Stability circles on the top or bottom are best solved with both a series and shunt resistance. In integrated designs, the use of lossy substrate lead to components (inductors) with lower Q and hence improved stability.

3.2 Power Amplifier Classes and Topologies

An RF power amplifier can be realized in numerous different ways, depending on the topology and biasing conditions. In the following, the different amplifier classes [8] are summarized.

3.2.1 Linear PAs: Classes A, B, AB, and C

Consider the general amplifier of Fig. 3.3. In the case of linear amplifiers, the active device is used as a current controlled source. The class of operation is defined by the biasing point, which states the quiescent current (I_{dq}).

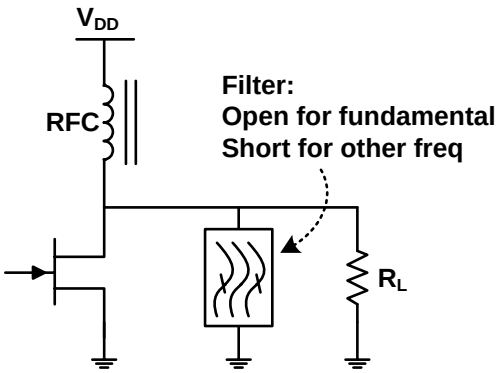


Figure 3.3: General Amplifier Scheme.

Class-A power amplifier places the bias point in the middle of the curve, at $I_{max}/2$. That ensures that full voltage excursion is available without clipping. Therefore, linearity is excellent, only posing issues at very high power when clipping occurs. However, as the transistor is biased in middle point (2π conduction angle) the efficiency is limited to 50%.

Class-B power amplifier places the bias point exactly at zero, limiting voltage excursion to half period. The output signal is recovered filtering the fundamental. Due to the conducting angle of π, efficiency reaches up to 78.5% ($\pi/4$), boosting more than 50% efficiency of class-A. However, as conduction angle is π, the gain is 3 dB lower than in Class-A.

Class-AB power amplifier places the bias point at some point between zero and $I_{max}/2$, leading to a performance between class-A and class-B. The exact bias point will determine

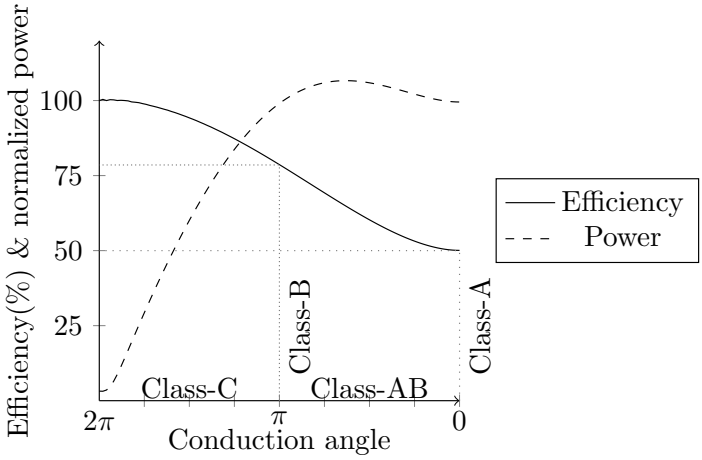


Figure 3.4: Efficiency depending on conduction angle.

the behavior of the amplifier. However, due to the change in operating mode from class-A to class-B, it exhibits a soft gain compression characteristic in the transition, which is not desired to preserve linearity. Biasing in deep class-AB is referred when the amplifier is biased with I_{dq} about 5% to 10% of I_{max}.

Class-C power amplifier places the bias point at cut-off, reducing conduction angle below π. However, the cost of a reduced conduction angle is a lower usage of the transistor, lower gain, and lower output power, depending on how deep in class-C the amplifier is operated. As conduction angle is completely dependent on the signal amplitude, the gain is also non-constant.

3.2.2 Switching PAs: Classes D, E, and F

In order to decrease power dissipation in the amplifier, the overlap of voltage and current in the transistor should be minimal. One straightforward method for achieving that is to use the transistor as a switch instead of as a current controlled source. By operating the transistor either in cut-off (open circuit) or triode region (short circuit), either current or voltage are zero respectively.

Class-D power amplifiers are composed of two switches, creating a square voltage. In an ideal case, as depicted in Fig. 3.5, switches create a square-wave voltage, which contains the fundamental along with the odd harmonics. Then a filter tuned at fundamental removes other harmonic components, providing a high efficiency amplification.

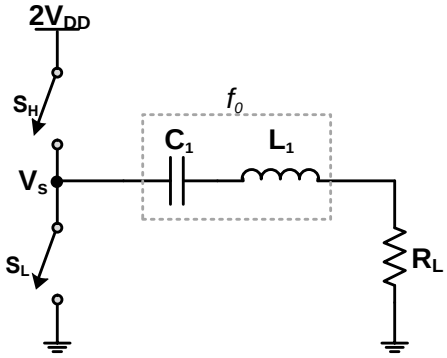


Figure 3.5: Class-D PA basic scheme.

However, in real applications, there are several non-idealities that limit its performance. For instance: transistor output capacitance is charged and discharged every switching cycle. To overcome that limitation, Zero Voltage Switching (ZVS) should be adopted. A straightforward way of achieving that is by swapping voltage and current waveforms, implementing what is called current mode class-D (CMCD) [106]. Nonetheless, even in current mode operation, several non-idealities still are important and the topology is used up to UHF frequencies.

Class-E power amplifier (Fig. 3.6) also uses the transistor as a switch, but in their output shaping network design they include the transistor output capacitance. The shaping network not only provides correct voltage shaping but also creates ZVS conditions and zero current turn-on. Compared with Class-D, it has lower switching loss but higher conduction loss due to the increased current in the active device. However, its main drawback is the high drain voltage and lower transistor utilization factor compared with other classes.

Class-F power amplifier contains certain harmonic terminations in the active device's load impedance [107]. It uses an infinite number of resonators in the output matching network (OMN) and creates drain voltage and current waveform with no overlap between them, resulting in low power consumption and high efficiency. If the current and voltage shapes are swapped, an inverse class-F (class-F^{-1}) is created. Implementing a class-F or inverse class-F with a GaN transistor results to a higher output power level compared to class-E. However, a complex load network is needed for a proper harmonic termination in class-F PA, increasing the complexity of the design. Class-F amplifiers are explained in detail in section 3.3.

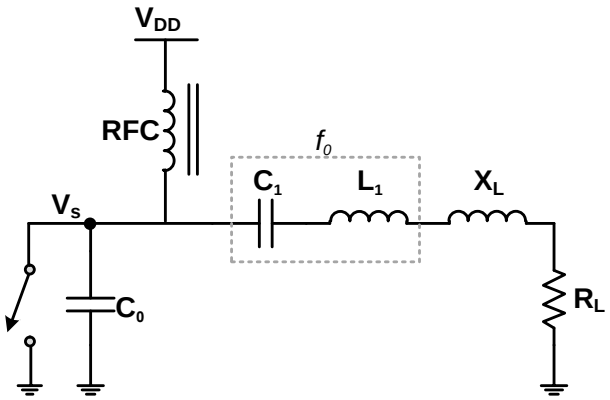


Figure 3.6: Class-E amplifier basic scheme.

However, it should be pointed that there is a limitation on the number of harmonics that can be tuned from device output. Not only due to the increasing complexity as harmonics are added, but also due to parasitic capacitance on active device output [8]. A large capacitance will become a short circuit at higher harmonic orders at microwave operating frequencies. Therefore at 900 MHz and higher frequencies, device technologies such as Gallium Arsenide (GaAs) or Gallium Nitride (GaN) are required in order to make a full harmonic tuned Class-F.

3.3 The Class-F Power Amplifier Basics

Previously the different classes of amplifiers have been introduced. In current section, the operation and design of Class-F PAs will be addressed in detail.

An ideal class-F PA should have no overlap between the drain voltage and current. This is achieved by having a square drain voltage and half-sinusoidal current as depicted in Fig. 3.7 and described by equations 3.12 [108].

$$\omega t\big|_0^{\pi} \begin{cases} v(\omega t) = 2V_{cc} \\ i(\omega t) = 0 \end{cases} \quad \omega t\big|_{\pi}^{2\pi} \begin{cases} v(\omega t) = 0 \\ i(\omega t) = 2I_R \sin(\omega t) \end{cases} \tag{3.12}$$

Expanding the waveforms in their general Fourier terms leads to equation 3.13. It can be seen that with an unlimited number of harmonic tuners, ideal waveforms and consequently 100% efficiency will be obtained. However, that is not feasible in practice since only a limited number of harmonics can be tuned effectively, lowering the maximum achievable efficiency. Studies show that termination of harmonics higher than 3^{rd} order has little effect on efficiency improvement and it increases the complexity of the circuit

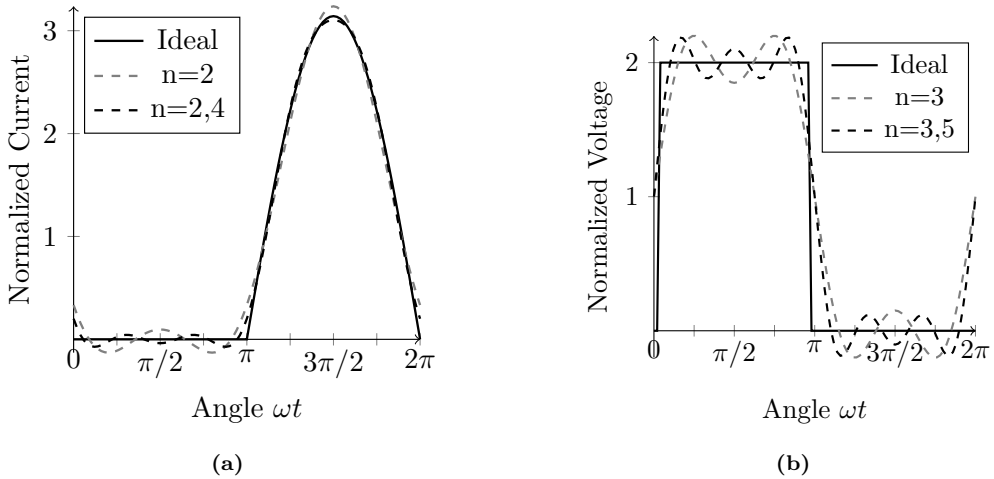


Figure 3.7: Normalized class-F drain waveform for ideal case and number of harmonics taken into account: (a) Current, and (b) Voltage.

[109].

$$\begin{cases} v(\omega t) = V_{cc} + V_1 \sin(\omega t) + \sum\limits_{n=3,5,7\ldots}^{\infty} V_n \sin(n\omega t) \\ i(\omega t) = I_0 - I_1 \sin(\omega t) + \sum\limits_{n=2,4,6\ldots}^{\infty} I_n \cos(n\omega t) \end{cases} \tag{3.13}$$

3.3.1 Maximally Flat Waveforms

One of the different methods to achieve Class-F operation is by the usage of *maximally flat waveforms*[3]. The goal of this approach [108] is to maximize efficiency by ensuring that voltage is as low as possible during the current peak at $\omega t = 3\pi/2$. To achieve Class-F operation by the usage of *maximally flat waveforms* and to maximize efficiency, the voltage should be as low as possible during the current peak at $\omega t = 3\pi/2$. The implementation of *maximally flat* voltage requires the even-order derivatives of voltage to be zero at $\omega t = 3\pi/2$. The general flat voltage equation 3.14 allows extracting a set of equations depending on the number of harmonics N considered (3, 5, 7, ...). Similar process can be carried out for currents, at $\omega t = \pi/2$ for even harmonics, leading to

[3]The term "Maximally Flat Waveforms" is used by Raab in [110], later on by Grevenikov and Sokal in [108] and many other academic sources refer to this concept with the same term. Although there is not wave in the drain of transistor, which makes using the term "Waveform" partially incorrect, in this thesis it has been used the same as used by the authors to preserve the Nomenclature and consistency with academic texts.

Table 3.1: Performance of class-F PA for various combinations of harmonics considered in current and voltage [108, 110].

Current Harmonics	Voltage Harmonic				
	1	1,3	1,3,5	1,3,5,7	1,3,5,...,∞
1	0.500	0.563	0.586	0.598	0.637
1,2	0.667	0.750	0.781	0.798	0.849
1,2,4	0.711	0.800	0.833	0.851	0.905
1,2,4,6	0.731	0.823	0.857	0.875	0.931
1,2,4,...,∞	0.785	0.884	0.920	0.940	1.000

equation 3.15.

$$\forall_{n=2,4,\ldots}^{N-1} \left\{ \frac{d^n v}{d(\omega t)^n} = (-1)^{n/2} \left(\sum_{m=1,3,5\ldots}^{N} m^n V_m \sin(m\omega t) \right) = 0 \right. \tag{3.14}$$

$$\forall_{n=2,4,\ldots}^{N} \left\{ \frac{d^n i}{d(\omega t)^n} = (-1)^{\frac{n-1}{2}} \left(I_1 \sin(\omega t) + \sum_{m=2,4,6\ldots}^{N} m^n I_m \cos(m\omega t) \right) = 0 \right. \tag{3.15}$$

The system of equations comprised by both equations 3.14 and 3.15 should be solved, obtaining the different voltages and currents needed. As a result, a fast analysis can be done to obtain the impact of the number of ternubared harmonics on the drain efficiency, provided in table 3.1 [108, 110].

So the summary is that from the voltage and current shape description in equation 3.13, it can be observed that voltage has all of the odd harmonics while current has all of the even harmonics. By preserving the odd harmonics in the drain voltage and preserving even harmonics in drain current, an ideal square voltage and half-sine current waveform are shaped respectively. Having them maximally flat with no overlap between them leads to the best compromise between efficiency and output power. This is the basic requirement of the class-F OMN, a harmonically matched network that provides open circuit (OC) at odd harmonic and short circuit (SC) at even harmonics. In the following, the conventional practical implementation of a class-F PA is explained.

3.3.2 Quarter-wave Transmission Line Class-F

A conventional way to implement class-F PA (and preferred for high frequencies) is depicted in Fig. 3.8. Such implementation, provided by Raab in 1976 [111], uses a $\lambda/4$ TL and an LC tank in parallel to the load. The purpose of the LC tank is to provide a low impedance at all harmonics except fundamental. The $\lambda/4$ TL acts as an impedance

converter, inverting the impedance at the odd harmonics, where $L = \lambda/4 + n\lambda/2$ and propagating the low impedance at even harmonics where $L = n\lambda/2$.

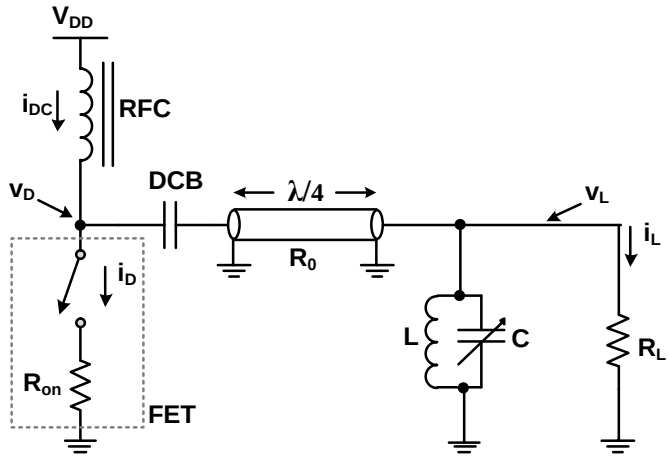


Figure 3.8: Class-F PA implementation using a $\lambda/4$ TL.

3.3.3 Multi-Harmonic Resonator Implementation of Class-F

Another method to achieve class-F operation is illustrated in Fig. 3.9, showing the implementation of series of LC tank circuits, each tuned at a different odd harmonic, providing a high impedance in the drain (hence low current). To ensure full current at even harmonics, a low output impedance is provided via a capacitor, which is shunted with an inductor at the fundamental. This methodology was widely used with vacuum tubes [108, 111].

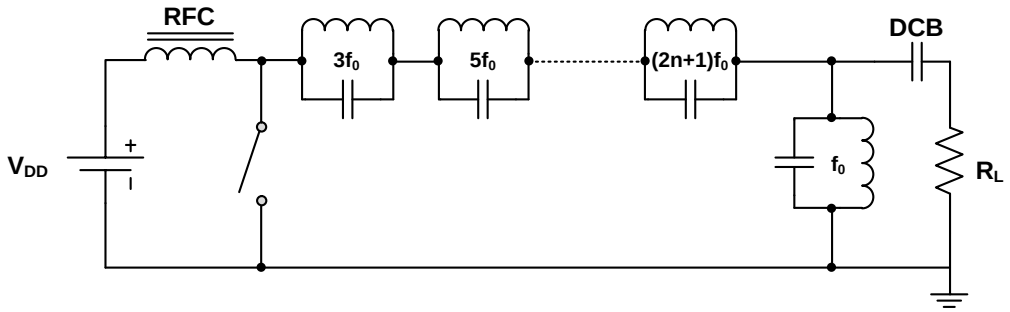


Figure 3.9: General class-F PA implementation using multi-harmonic resonators.

A conventional class-F PA with limited harmonic resonator proposed by Raab [110]

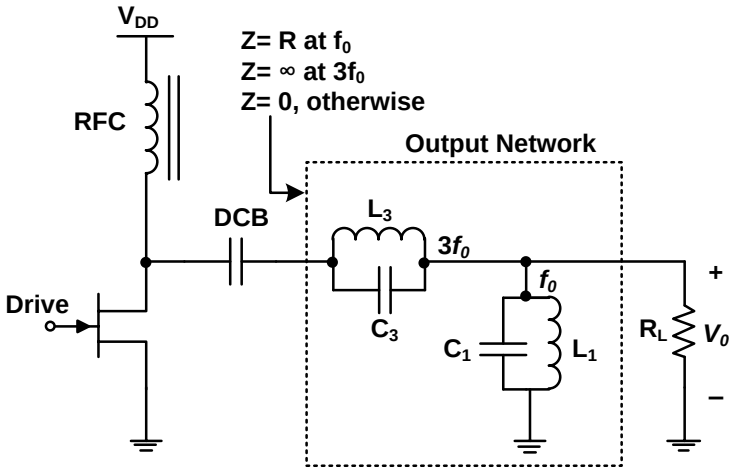


Figure 3.10: Conventional Class-F PA OMN configurations using multi-harmonic resonators of 3^{rd} order [110].

is shown in Fig. 3.10, where only 3^{rd} order harmonics is considered in the OMN. This reference provides calculations for predicting the voltage and current shape depending on the different combination of harmonics. It assumes an ideal LC filter and ideal current source as the active device with no on-resistance nor output capacitance. It can be seen that by increasing the number of harmonics to infinite an ideal square shape and an ideal half-sine shape will be generated.

3.3.4 Fully Transmission Line Implementation of Class-F

Transmission lines have unique properties that give them the advantage over lumped elements. The periodic structure of the TL reduces the complexity in the design of harmonic tuning and helps to achieve the required behavior of a class-F PA at multiple resonant frequencies. Also, a widely used concept for biasing the power amplifiers is using quarter-wave TL stub at fundamental frequency as a *biasing line*. This $\lambda/4$ line serves a dual purpose of providing DC path from power supply to transistor gate/drain and blocks the RF at a fundamental frequency. To do so, the TL is loaded by a high-value capacitor, acting as a SC at RF, and inverted to OC at the transistor gate/drain. The open presented at the gate/drain has no effect at fundamental frequency and odd-harmonics, providing SC at second harmonic. The ability to match two complex impedances with a single TL of prescribed length and characteristic impedance is another advantage [112].

An example of a class-F OMN using transmission lines is shown in Fig. 3.11 [113]. It incorporates the quarter wavelength for bias and second harmonic termination. The

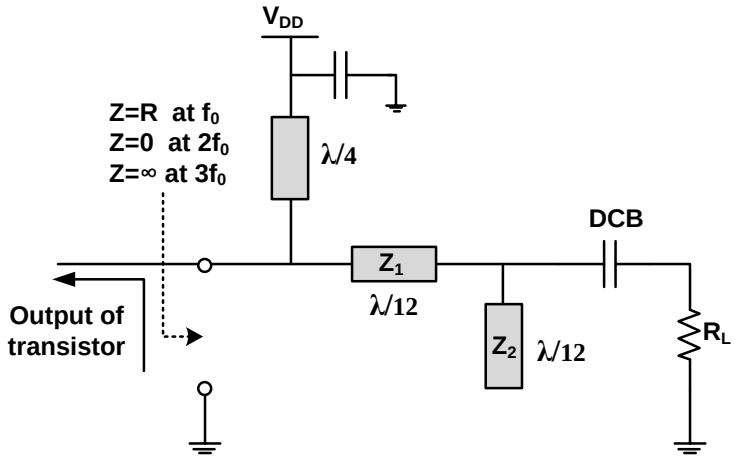


Figure 3.11: Conventional Class-F PA OMN configurations using transmission lines [113].

two $\lambda/12$ stubs provide the third harmonic peaking. Load network design techniques, the frequency response of load networks and related equations, the effects of shunt capacitance in class-F and the effect of series inductance in inverse class-F are well explained by Grebennikov in [113].

3.4 Load-Pull Technique

Load-pull is an essential technique in the design and development of amplifiers. While the methods described in section 3.3 provide good results considering the ideal operation of amplifiers, the real performance of the PA is reduced due to the parasitics and non-ideal behavior of the active device. To achieve optimal practical performance, a load-pull based design should be carried out, to fully characterize the active device regarding output power, efficiency, power gain and PAE considering the non-linear behavior of the active device.

In load-pull technique a set of load impedances, defined by a certain VSWR in the Smith chart, are varied and the transistor performance is evaluated accordingly for each of these load impedance values. In linear power amplifiers, the load optimum value can be obtained directly from S-parameters of the device and the maximum power is transferred when the matching network is conjugate matched to the active device. However, as explained for the case of high efficiency PAs, a certain harmonic tuning is needed and the conjugate match does not necessarily lead to the maximum efficiency. For the particular case of class-F PA, ideal short and open circuits do not necessarily lead to the best results and a load-pull analysis should be performed to achieve the impedance load for a trade-off

between maximum efficiency and maximum power.

A complete explanation of basics of the load-pull technique is provided in [114]. The load-pull measurement of the device needs advanced setups, one example is provided in [115]. However, in this thesis, the nonlinear model of the active device was available and therefore the load-pull simulations are done using the Advanced Design System (ADS) simulator. In some cases, source-pull is also performed in addition to load-pull in order to find the optimum input impedance for a specific load impedance. The typical design process using ADS simulator is the following:

1. Set an arbitrary initial value for load impedance at fundamental frequency (Z_{L1}) and harmonics (Z_{L2}, Z_{L3}, Z_{L4}, Z_{L5}...). For class-F, the value of harmonics can be 1Ω for Z_{L2},Z_{L4}, and 100Ω for Z_{L3},Z_{L5}.
2. Set Z_S to the conjugate of transistor S_{11} at fundamental frequency.
3. Run load-pull analysis in ADS at fundamental frequency (f_0). For obtaining Z_{L1} in simulations, all the other values are the initial values except the Z_{L1} which is the load that is varying.
4. Set the impedance value obtained from the load-pull analysis for Z_{L1}.
5. Run source-pull analysis at fundamental frequency (f_0). For obtaining optimum source impedance, Z_s is the impedance that is varying.
6. Set the impedance value achieved from the source-pull analysis for source impedance (Z_S).
7. Run load-pull analysis in ADS at 2^{nd} harmonic ($2f_0$). For obtaining Z_{L2} in simulations, Z_{L2} is the load that is varying.
8. Set the impedance value achieved from the load-pull analysis for Z_{L2}.
9. Run load-pull analysis in ADS at 3^{rd} harmonic ($3f_0$). For obtaining Z_{L3} in simulations, Z_{L3} is the load that is varying.
10. Set the impedance value achieved from the load-pull analysis for Z_{L3}.
11. Do the iteration (Vary the load and obtain the impedance) for how many harmonics that is considered in the design.
12. After obtaining load at harmonics (Z_{L2}, Z_{L3}, Z_{L4}, Z_{L5}), run load-pull analysis at fundamental frequency (f_0) again to achieve the final optimum load impedance at fundamental frequency for best trade-off between PAE and P_{out}.

In the process explained above, the impedance value achieved from the load-pull analysis at each frequency depends on the requirements of the design. In class-F, the 2^{nd} harmonic load is chosen close to be SC and 3^{rd} harmonic load is chosen to be OC to fulfill the class-F requirements. In addition, the load impedance at fundamental

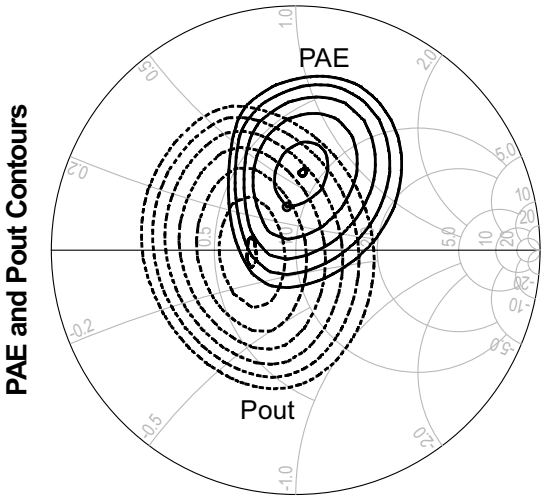


Figure 3.12: An example of power and PAE contours obtained from load-pull analysis.

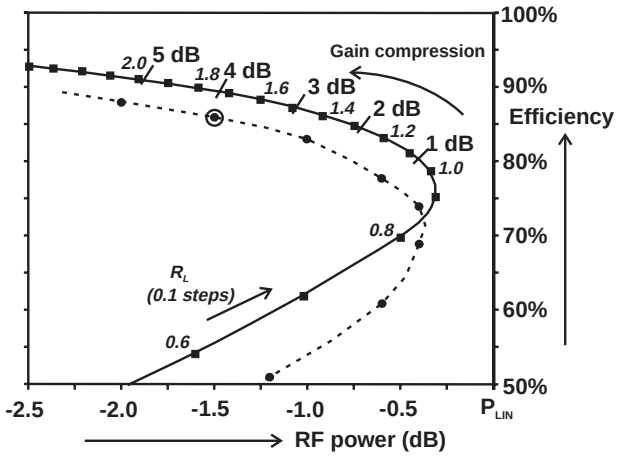


Figure 3.13: An example of power-efficiency contour for a varying RF load resistance, for a clipping Class-B amplifier having an even harmonic output short [8].

frequency (Z_{L1}) can be chosen for maximum PAE or maximum power or a trade-off between the two. This depends on the requirements of the PA. An example of the power and PAE contours obtained from load-pull analysis are shown in Fig. 3.12. Each set of contours are related to PAE or P_{out}, being maximum in the center and descending as it goes to outside circles. A typical figure of PAE versus P_{out} is illustrated in Fig. 3.13 from Cripps [8] which shows the maximum point and the trade-off values between them.

4

Chapter 4

Class-F Power Amplifier Basic Operation and Analysis

This chapter explains the basic operation of a class-F power amplifier along with a detailed explanation of the proposed class-F PA for single frequency operation. Different configurations are compared. Two power amplifiers are designed and fabricated at 900 MHz and 1800 MHz. The complete simulation of each amplifier is presented and is compared to the measurement results.

4.1 Proposed Class-F Power Amplifier Topology

The input and output matching networks are designed based on transmission lines (TL) and they match the power device to 50Ω load. The proposed output matching network (OMN) shown in Fig. 4.1 consist of 7 stubs. It provides an open circuit (OC) to the third harmonic through TL1 and TL2, with lengths of $\lambda/12$ at fundamental frequency. At second harmonic, TL3 delivers low impedance to the right-hand side of TL4 (electrical length of θ_1), as shown in Fig. 4.3b. Transmission lines TL1, TL2 and TL4 together provide short circuit (SC) at second harmonic. TL5, TL6 and TL7 create a π-shape matching network which increases the design freedom for matching at fundamental frequency, thus helping the designer to improve the PA performance in terms of efficiency and output voltage waveform. The stub with the highest effect on the output waveform is TL7. This stub improves the output voltage waveform presenting a perfect sinusoidal shape without any distortion.

The proposed input matching network (IMN) is illustrated in Fig. 4.2. It consists of 5 stubs: 1 quarter wavelength stub and 4 subs forming a double low pass network. Transmission line TL10 grounded through a bypass capacitor is $\lambda/4$ at fundamental frequency which provides an OC for RF signal, and is $\lambda/2$ at second harmonic which provides a SC to the second harmonic component of the input signal. This second harmonic termination at input signal provides a better harmonic cancellation at the output of the amplifier. This topology gives freedom to the designer to make the 3rd harmonic termination at input signal through TL8 and TL9. Resistors R_1, R_2 and R_3 ensure that the circuit works under stable conditions.

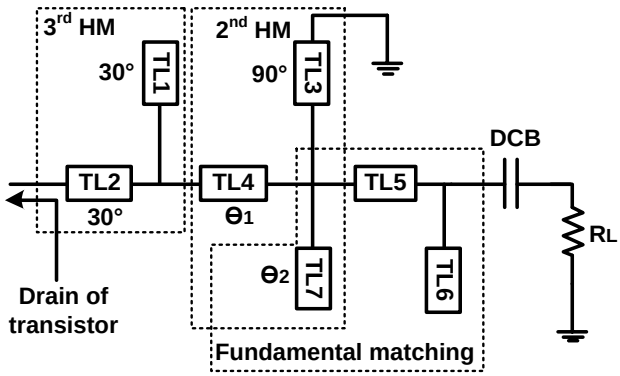


Figure 4.1: The proposed output matching network.

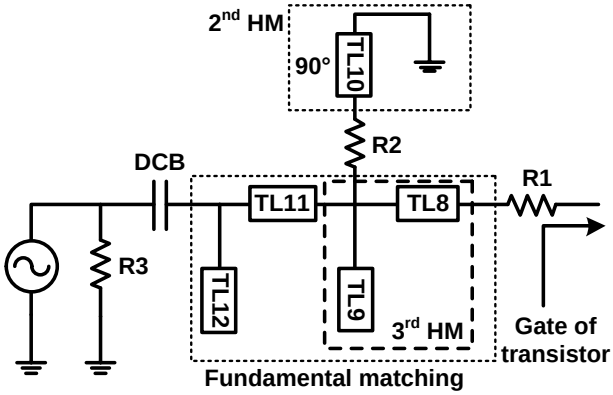


Figure 4.2: The proposed input matching network.

The full schematic of the proposed circuit for the class-F PA is shown in Fig. 4.3. The equivalent circuit seen from the drain of the transistor is shown in Fig. 4.3b at second harmonic and in Fig. 4.3c at third harmonic. The proposed OMN structure allows the control of harmonics simultaneously but independent of each other.

4.2 Design at 900 MHz Operating Frequency

The first step in designing a power amplifier is to know the characteristics of the active device. The active device used in this design is a Cree transistor (CGH40006P), an unmatched GaN HEMT offering high efficiency, high gain, and wide bandwidth capabilities. The electrical characteristics of the device are available from its datasheet provided by the company. The high breakdown voltage of 120V of this device allows to fulfill the high power requirements of the proposed power amplifier.

4.2.1 Load Pull Analysis

The procedure of choosing the load impedance at fundamental and harmonics is a compromise of efficiency and power and it highly depends on the requirements. The output power and PAE contours obtained from load-pull analysis at 900 MHz are shown in Figure 4.4. The PAE and Delivered Power Contours at second and third harmonic are shown in Fig. 4.4b and Fig. 4.4c respectively. The marker in Fig. 4.4b shows the load impedance of $0.3 - j12.7$ at second harmonic. It is on the contour of 81.6% and output power of 39.1 dBm and it is chosen close to SC in order to fulfill class-F PA requirements at second harmonic. Similarly the marker in Fig. 4.4c shows the load impedance of $1 + j121$ at third harmonic. This point is in the contour of 81.5% and

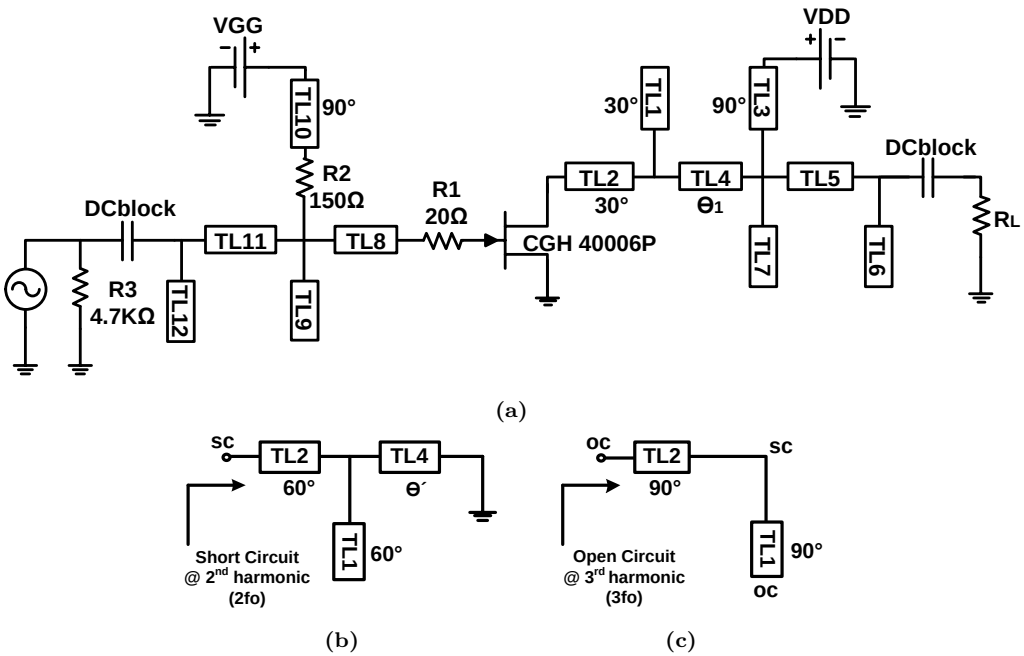


Figure 4.3: (a) Proposed class-F PA, (b) equivalent circuit seen by active device at 2^{nd} harmonic and (c) equivalent circuit seen by active device at 3^{rd} harmonic.

output power of 39.1 dBm and it is chosen close to OC in order to fulfill class-F PA requirements at third harmonic. Finally, the simulation results at fundamental frequency in Fig. 4.4a show that a maximum PAE of 82% and output power higher than 39.25 dBm can be achieved with a drain voltage of 28 V.

The contours of harmonics in Fig. 4.4b show a PAE between 79.5 and 81.8%. At 2^{nd} harmonic, PAE at ideal SC is 80.5% while at chosen 2^{nd} harmonic load is 81.6%. This shows that by proper harmonic load termination at $0.3 - j12.7$ an improvement of 1.1% for PAE was achieved compared to ideal SC termination. The same is valid for 3^{rd} harmonic. The contours of harmonics in Fig. 4.4b show a PAE between 80 and 82.4%. At third harmonic, PAE at ideal OC is 80% while at chosen 3^{rd} harmonic load is 81.5%. This shows that by choosing the load impedance at $1 + j121$ an improvement of 1.5% was achieved compared to ideal OC termination.

Different plots for PAE versus output power corresponding to each load impedance in smith chart is plotted in Figure 4.5. Each plot is obtained by changing the magnitude of load values with constant phase. This has been done for all phases to cover the entire Smith Chart. The marker dot in this figure corresponds to the marker in Fig. 4.4a and shows the optimum point at the input power of 25 dBm. Since high PAE was desired, the impedance value of $40 + j20.5$ which gives a PAE of 82% and output power of 39.25 dBm

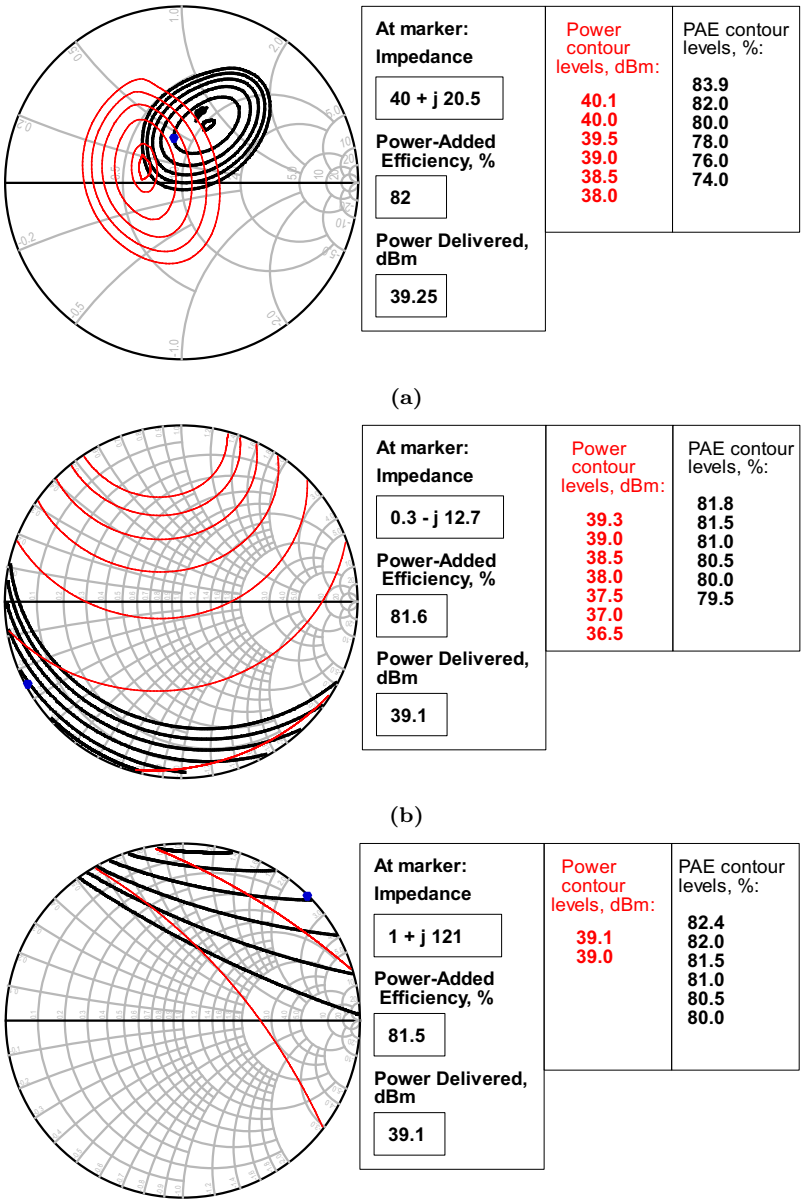


Figure 4.4: Output power (thin) and PAE (thick) contours from load-pull analysis at (a) fundamental frequency (900 MHz), (b) 2^{nd} harmonic (1800 MHz) and (c) 3^{rd} harmonic (2700 MHz). (V_{DS} = 28 V, V_{GS} = -2.8 V, P_{in} = 25 dBm)

is chosen. Z_{L1}, Z_{L2} and Z_{L3} given in Table 4.1 are load impedances that result in an optimum performance at fundamental, second and third harmonics respectively. Using

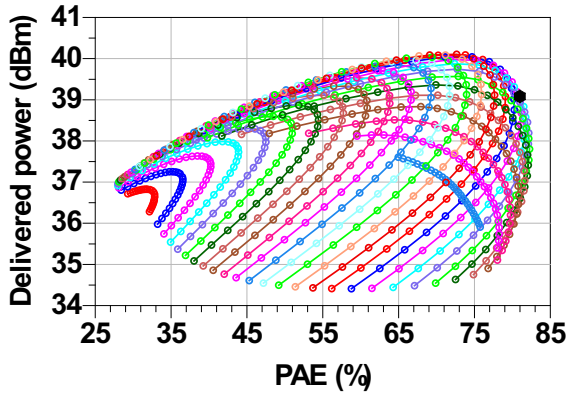


Figure 4.5: Load pull results for PAE (%) versus output power (dBm) at 900 MHz.

Table 4.1: Load Impedances (Ω) at fundamental frequency (Z_{L1}), 2^{nd} harmonic (Z_{L2}) and 3^{rd} harmonic (Z_{L3}) obtained from load-pull analysis.

	Load Impedance (Ω)
	f_0 = 900 MHz
Z_{L1}	40 + j20.5
Z_{L2}	0.3 - j12.7
Z_{L3}	1 + j121

these optimum impedance values, the OMN and IMN of the PA are designed.

4.2.2 Stability

Stability is a very important parameter in amplifier design that should be considered at an early stage of the design. Before starting the design of matching networks, the active device should be checked for stability. It is desired that the amplifier be unconditionally stable and in case this requirement cannot be achieved, then it should at least be stable in all frequencies (in-band and out-of-band) for the source and load impedances selected in the design. Primary simulation of the active device in Fig. 4.6a shows that the stability factor K is bigger than 1 in a small bandwidth between 3 GHz and 8 GHz while the operating frequency is at 0.9 GHz. There is a need for a lossy matching network in order to make it stable and the solution to increase stability in this design is adding resistors R_1, R_2 and R_3 to the gate and bias circuit of the IMN of the amplifier. This improves the stability of the transistor making K $>$ 1 in a wider frequency range. The results of the stable active device are shown in Fig. 4.6b.

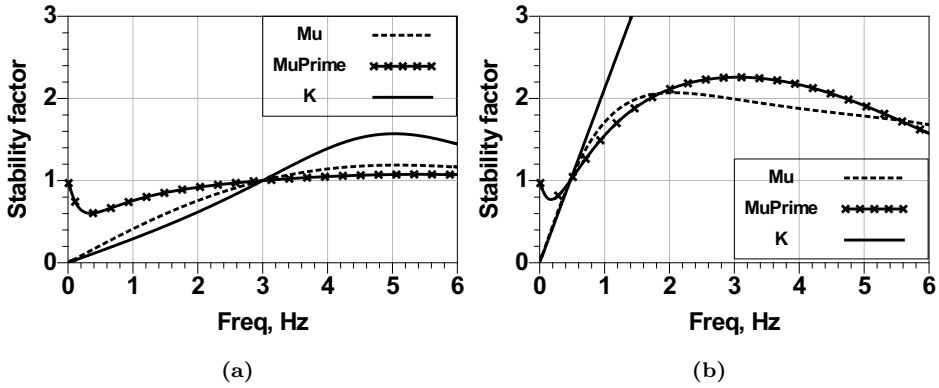


Figure 4.6: Stability of the active device (a) before and (b) after applying stability techniques.

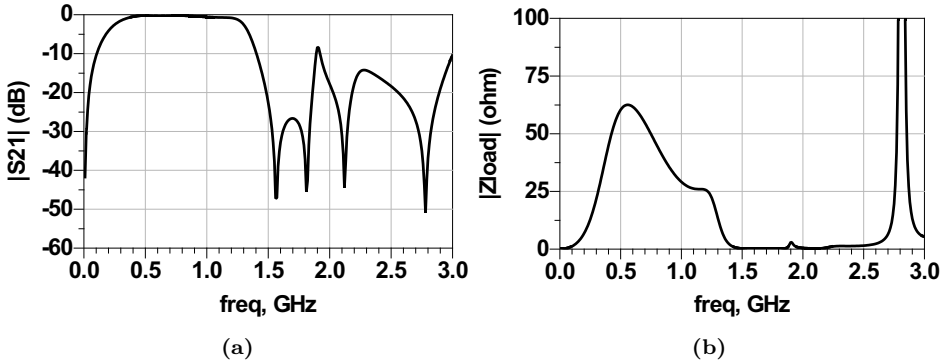


Figure 4.7: Frequency response of the output matching network of Fig. 4.1 designed at 900 MHz and with second and third harmonic terminated: (a) the S-parameter and (b) the load impedance.

4.2.3 Simulation Results

To evaluate the performance of the proposed topology in Fig. 4.3, Large Signal S-parameter (LSSP), Harmonic Balance (HB), and Electromagnetic (Method of Moments) simulations are performed using Keysight Advanced Design System (ADS) simulator.

The frequency response of the designed OMN with second and third harmonic tuning is shown in Fig. 4.7a. It demonstrates the fundamental matching at 900 MHz and corresponding second and third harmonic tuning at 1.8 GHz and 2.7 GHz, respectively. The corresponding impedance values are presented in Fig. 4.7b.

The power amplifier of Fig. 4.3 is designed at 900 MHz and is driven into saturation region with an input power of 25 dBm. The performance of the amplifier is simulated

versus both input power and frequency. The simulation results versus input power in Fig. 4.8a shows that a peak PAE of 80.43%, drain efficiency of 83.6% and gain of 14.2 dB are obtained at an output power of 39.2 dBm. The maximum drain efficiency of 84.6% is achieved at an input power of 27 dBm.

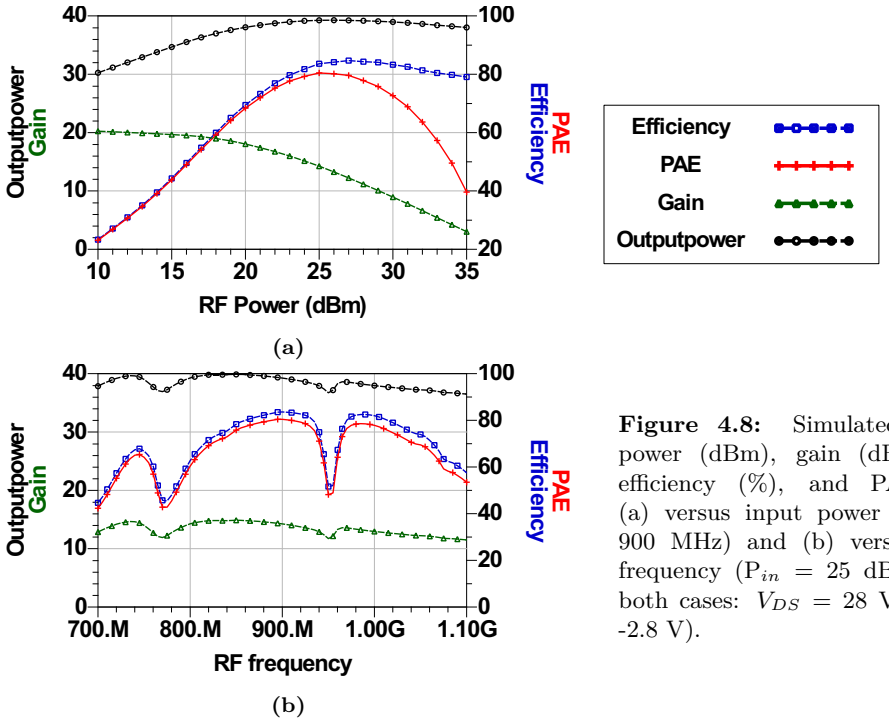


Figure 4.8: Simulated output power (dBm), gain (dB), drain efficiency (%), and PAE (%): (a) versus input power ($freq$ = 900 MHz) and (b) versus input frequency (P_{in} = 25 dBm). (In both cases: V_{DS} = 28 V, V_{GS} = -2.8 V).

The performance versus RF frequency in Fig. 4.8b shows that the amplifier is designed for the optimum value at the operating frequency of 900 MHz. The amplifier achieves a drain efficiency higher than 60% in the frequency band from 805 MHz to 950 MHz.

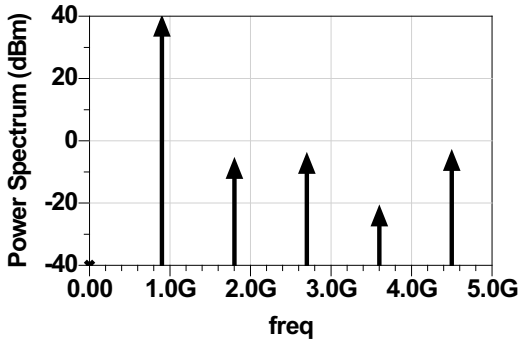


Figure 4.9: Output power spectrum.

Table 4.2: Simulation results for harmonic rejection up to fifth order.

		Harmonic rejection (dBc)			
Freq	P_{in}	2^{nd}	3^{rd}	4^{th}	5^{th}
900 MHz	25 dBm	-46.8	-46.3	-66.2	-48

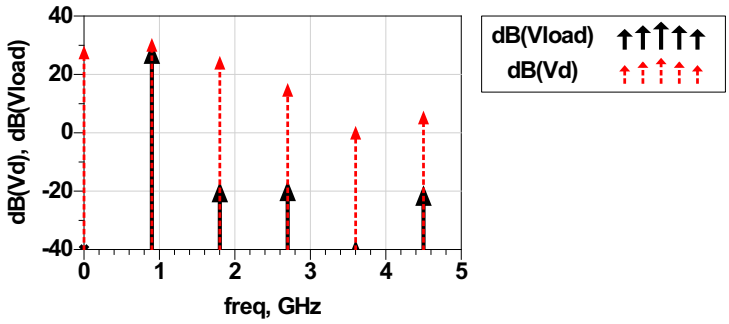


Figure 4.10: The spectrum comparison of drain voltage (V_d) and load voltage (V_{load}) of the amplifier indicating harmonic suppression by the OMN.

Output Spectrum of the simulated class-F PA is shown in Fig. 4.9. There is a 46 dBc and more difference between the desired output signal and harmonics which proves the proposed topology has the ability to reject harmonics while maintaining the high performance of the class-F PA without the need for an extra filtering section. Simulated harmonic rejection values are presented in Table 4.2. The spectrum illustrated in Fig. 4.10 shows the comparison of fundamental and harmonic components in drain voltage (V_d) and load voltage (V_{load}) of the amplifier proving that harmonics are properly removed by the output filter.

The performance of the proposed topology in Fig. 4.3 is compared to that of three class-F structures proposed in the literature and shown in Fig. 4.11. The IMN is kept the same as in Fig. 4.2 and only the OMNs are different. The output matching networks shown in Fig. 4.11 (a), (b) and (c) are retrieved from [113], [116] and [16] respectively. These circuits have been designed at 900 MHz for the best performance with the same power device under the same condition as the proposed PA in Fig. 4.3.

The comparison of the results are shown in Table 4.3 and Table 4.4, from which it can be seen that the structure proposed in Fig. 4.3 has the highest PAE, gain, and output power. But the main reason for the victory of the proposed topology over the literature is that it exhibits a good harmonic rejection with good input and output match. Input and output return loss are simulated to be less than -13 dB and -10 dB respectively. It also gives an extra freedom for 2^{nd} harmonic termination using stub TL7. Finally, this

topology results in a perfect sinusoidal signal at the output of the amplifier.

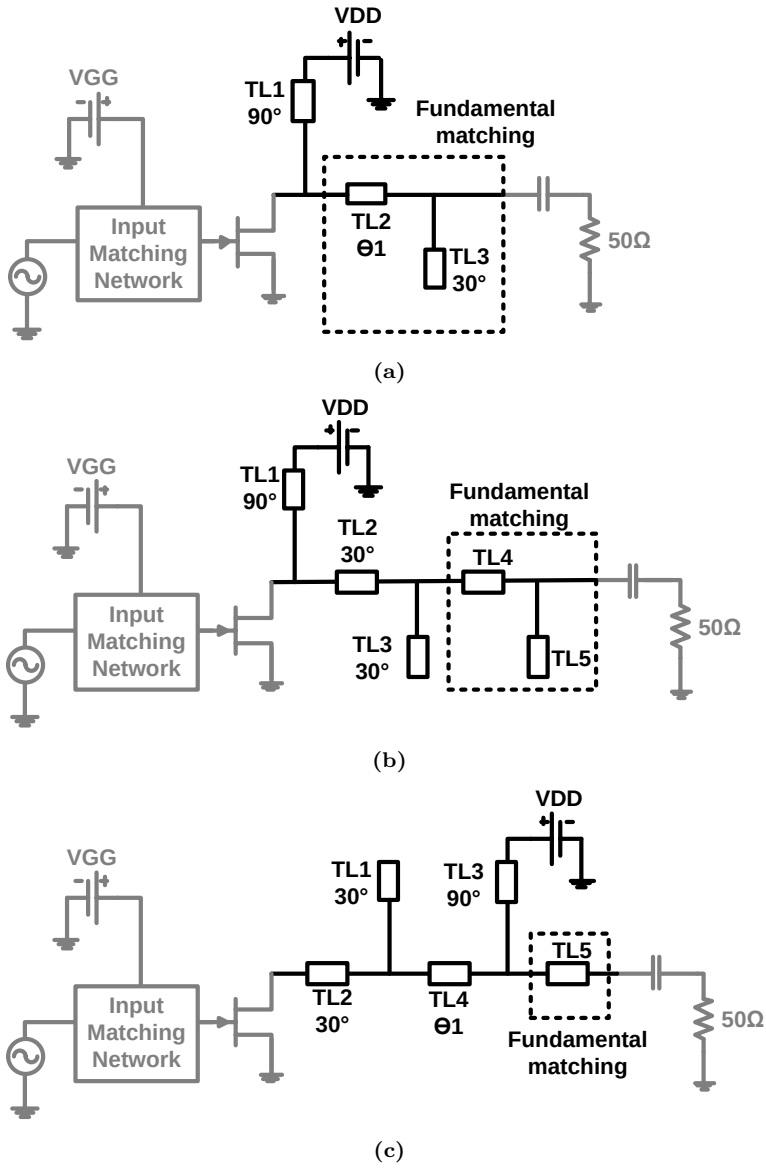


Figure 4.11: Three class-F PAs, The output matching networks are retrieved (a) from [113], (b) from [116] and (c) from [16].

Table 4.3: Comparison of performance simulation results for the three circuits of Fig. 4.11 and proposed PA in Fig. 4.3.

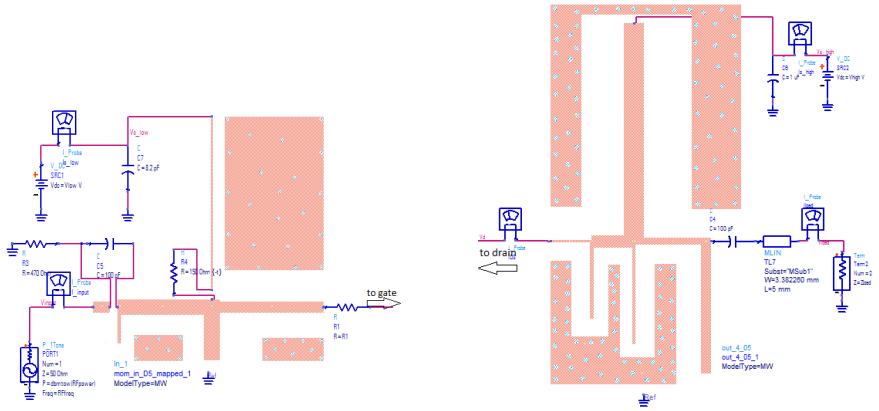
	PAE (%)	η (%)	Gain (dB)	Pout (dBm)	DC power (W)	Thermal dissipation (W)	$\mid S_{11} \mid$ (dB)	$\mid S_{22} \mid$ (dB)
[113]	73.2	75.4	15.4	40.4	14.6	3.9	-21	-6.8
[116]	79.5	83.2	13.5	38.5	8.5	1.7	-18	-16.5
[16]	78.3	81.6	14	38.9	9.7	2.1	-17	-19
Fig. 4.3	80.3	83.5	14.1	39	9.7	1.9	-14.6	-23.8

Table 4.4: Comparison of harmonic rejection simulation results for the three circuits of Fig. 4.11 and proposed PA in Fig. 4.3.

	Harmonic rejection (dBc)			
	2^{nd}	3^{rd}	4^{th}	5^{th}
[113]	-39	-39.5	-45	-45.6
[116]	-48.5	-48.3	-48.3	-59
[16]	-49	-29.7	-61.5	-48.5
Fig. 4.3	-46.7	-46.8	-68.6	-49.2

4.2.4 Fabrication

The experimental results of a fabricated prototype are quite sensitive to the circuit layout and implementation due to parasitics and couplings between lines. Therefore an electromagnetic simulation (using the method of moments in Agilent Momentum^{TM} tool) of the IMN and OMN layouts has been carried out in order to take into account all the real effects that happen in practice and are not considered in the schematic simulation. From the Momentum simulation of the IMN and OMN, their corresponding electromagnetic models (Momentum components) are obtained. The IMN and OMN Momentum components are then used in the PA schematic replacing the corresponding IMN and OMN transmission line elements, as shown in Fig. 4.12, to perform a co-simulation of the PA. The remaining elements are modeled using the S-parameter data, as well as capacitors and resistors that are modeled according to ADS library elements. This simulation setup and its components take into account all parasitic effects, giving a more realistic simulation of the PA. Then using this setup, the layout of the circuit is optimized to achieve the same performance as simulated schematic. The designed PA is fabricated on a 1.5 mm Rogers RO4003 substrate and is shown in Fig. 4.13. The dimension of the fabricated board is 94.3 mm x 120 mm.



(a) (b)

Figure 4.12: (a) Input and (b) output matching components created using momentum placed on the schematic.

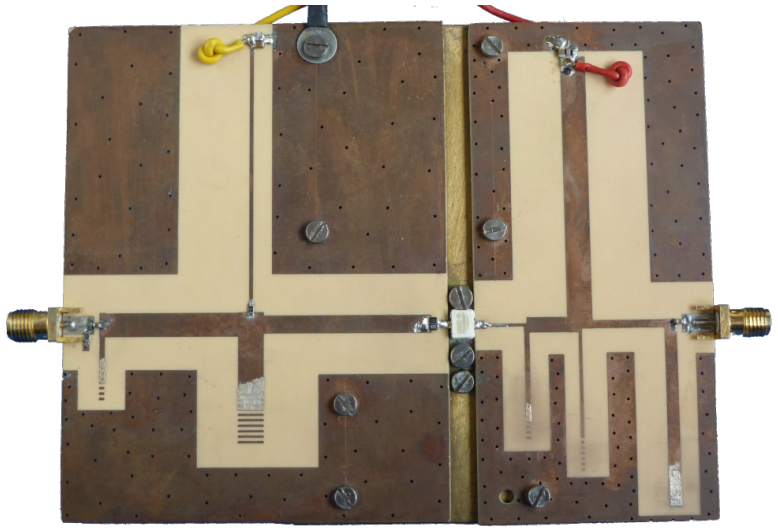


Figure 4.13: Fabricated class-F PA at 900 MHz.

4.2.5 Measurement Results

To validate the design against simulation results, the fabricated amplifier is measured using 2 setups depicted in Fig. 4.14. The input signal is generated using a synthesizer and is amplified by an available pre-amplifier with a gain of 43 dB. This amplifier is required in order to increase the maximum available input power to the device under test (DUT), since the maximum output power of the synthesizer is 20 dBm. A calibrated attenuator and a power meter are used to measure the exact output power values at

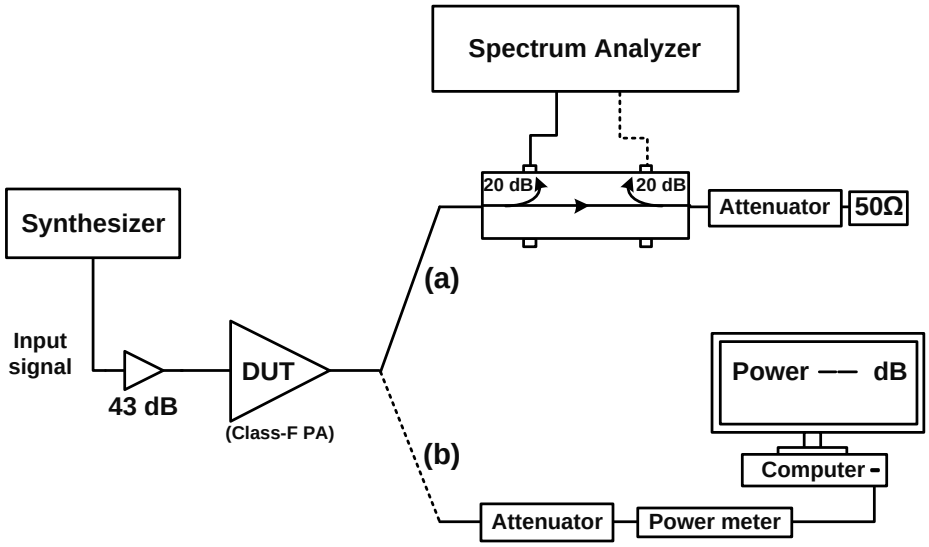


Figure 4.14: Setups for power and output spectrum measurement.

certain input powers at each frequency Fig. 4.14 (b).

To see the total output power spectrum a directional coupler, attenuator, and spectrum analyzer are used as shown in Fig. 4.14(a). For S-parameter measurement of the DUT, the configuration in Fig. 4.15 is used to measure the modulus of input and output reflection coefficient and the transmission coefficient. The dual directional coupler used is a Hewlett-Packard HP778D.

Using the test setup of Fig. 4.15, the modulus of the input and output coefficient and transmission are measured and compared to the LSSP simulation results in Fig. 4.16. It demonstrates a good agreement between simulation and measurements. Measurements versus frequency were carried out at the following bias point: gate voltage V_{GS} = -2.8 V and drain voltage V_{DS} = 28 V. Drain efficiency, PAE, output power and gain results versus frequency are shown in Fig. 4.17. The circuit has a wide bandwidth of 225 MHz (805 MHz - 1030 MHz) giving efficiency higher than 60%. It is interesting to note that there is a bandwidth of 105 MHz where the amplifier provides higher than 70% efficiency. The efficiency versus frequency measurement results for the 900 MHz amplifier showed that the fabricated amplifier has the maximum efficiency at a frequency of 875 MHz. Therefore, f_o = 875 MHz was considered the operating frequency of this circuit when performing measurements versus input power. The biasing of the circuit was also optimized for the best performance. Several measurements at different drain voltage were carried out and the comparison is illustrated in Fig. 4.18. The one that has the best compromise of the

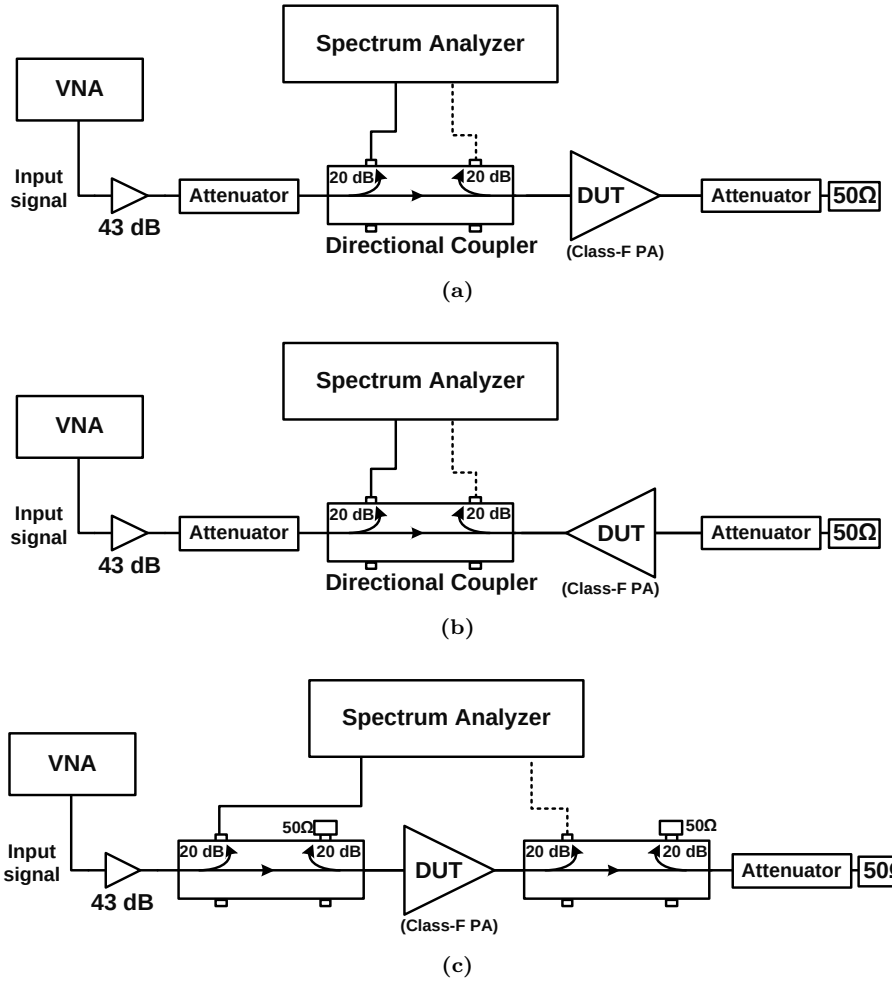


Figure 4.15: Experimental setup for (a) | S_{11} |, (b) | S_{22} | and (c) | S_{21} | measurement.

performance between efficiency and power is at drain voltage V_{DS} = 30.2 V and gate voltage V_{GS} = -2 V.

The full comparison of experimental and simulation results versus input power is illustrated in Fig. 4.19. The amplifier features a peak PAE of 80.3% and a drain efficiency of 84% at an input power level of 25 dBm. This amplifier gives a peak drain efficiency of 85.5% at an input power of 28 dBm.

Output power and gain results versus input power depicted in Fig. 4.19b show a gain of 13.5 dB and an output power of 38.5 dBm (7.2 W) measured at 875 MHz for an input power level of 25 dBm. The summary of the measurement and simulation results at the input power which gives the highest PAE is provided in Table 4.5.

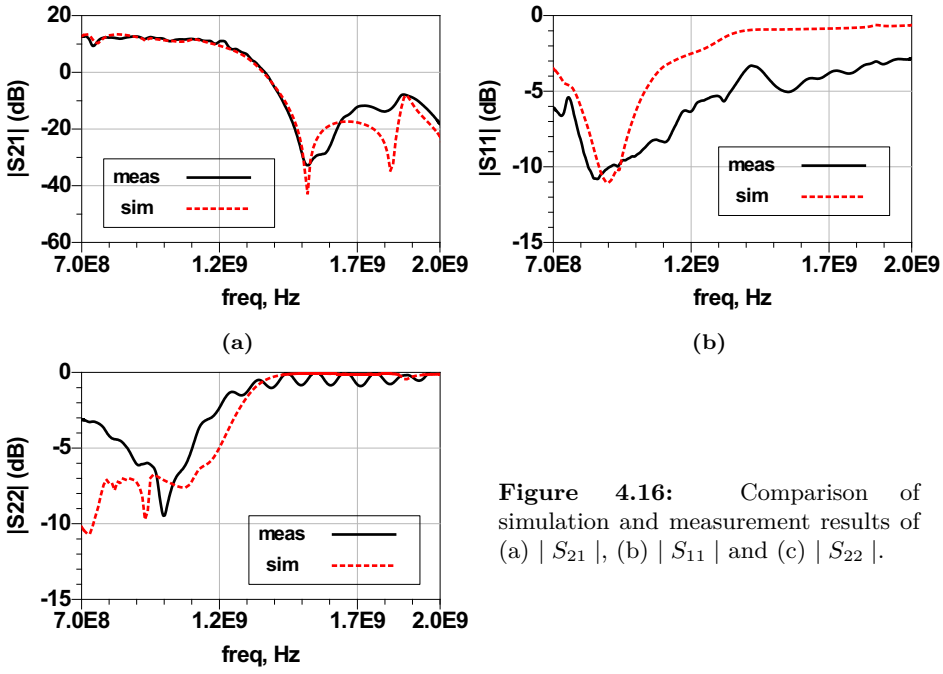


Figure 4.16: Comparison of simulation and measurement results of (a) | S_{21} |, (b) | S_{11} | and (c) | S_{22} |.

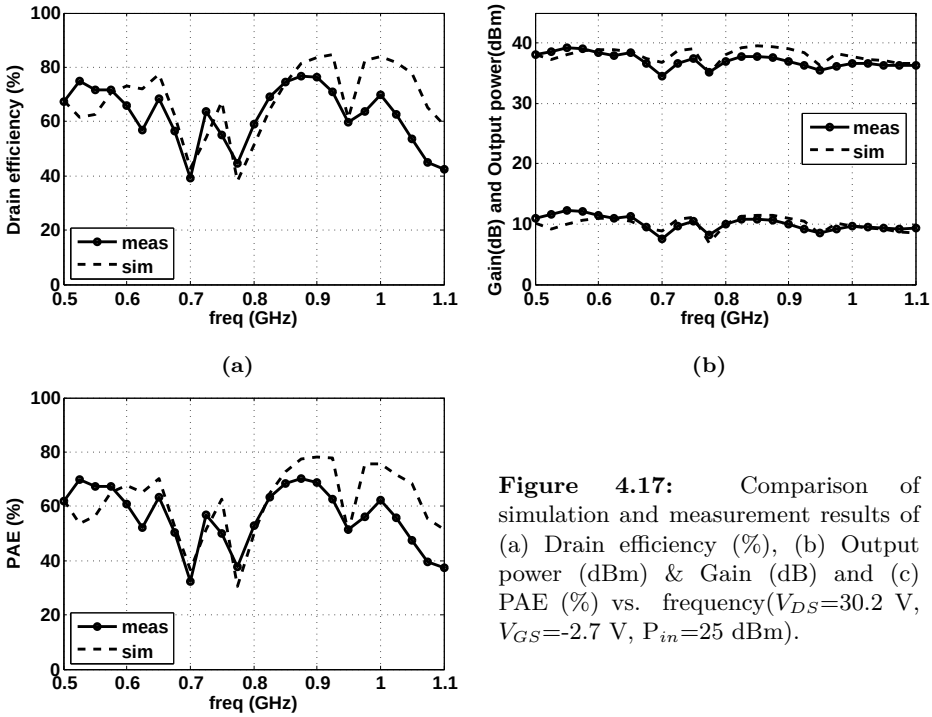


Figure 4.17: Comparison of simulation and measurement results of (a) Drain efficiency (%), (b) Output power (dBm) & Gain (dB) and (c) PAE (%) vs. frequency(V_{DS}=30.2 V, V_{GS}=-2.7 V, P_{in}=25 dBm).

Table 4.5: Measured and simulated values for the PA at the maximum PAE.

Freq (MHz)		V_D (V)	V_G (V)	P_{in} (dBm)	PAE_{max} (%)	η (%)	P_{out} (dBm)
900	Sim	28	-2.5	25	80.2	83.4	39.2
	Meas	28	-2.5	25	80.3	84	38.5

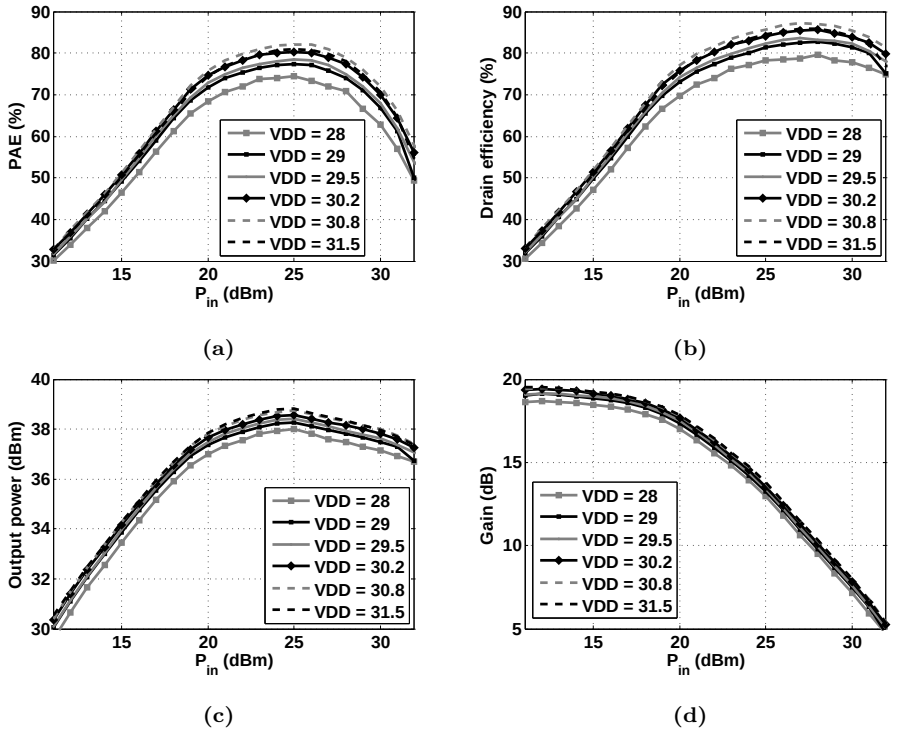
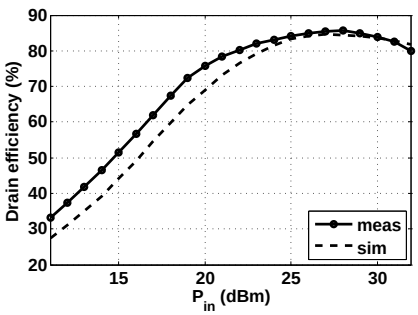
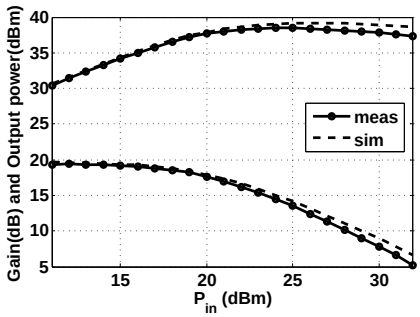


Figure 4.18: Comparison of measurement results for different bias point of the amplifier (a) PAE (%), (b) Drain efficiency (%), (c) Output power (dBm) and (d) Power gain (dB).

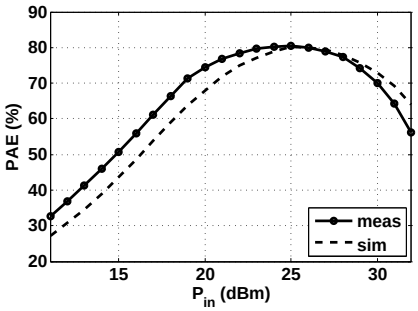
The output power spectrum is measured for the 900 MHz PA and is shown in Fig. 4.20. The measured harmonic distortion is 33.4 dBc for second harmonic ($2f_o$) and 42.3 dBc for third harmonic ($3f_o$), showing that the proposed topology has the ability to reject harmonics while maintaining the high performance of the class-F PA without the need for an extra filtering section. A low harmonic distortion is achieved and the total harmonic distortion (THD) is 1.2%. An Infrared Camera is used to capture the thermal behavior of the circuit and the image is shown in Fig. 4.21. It can be seen that the circuit is thermally stable and the transistor temperature is not high and is within the rated values. The only hot place is the resistor R_1 which gets hot but it is still in the acceptable range.



(a)



(b)



(c)

Figure 4.19: Comparison of simulation and measurement results of (a) Drain efficiency (%), (b) Output power (dBm) & Gain (dB) and (c) PAE (%) vs. input power (V_{DS}=30.2 V, V_{GS}=-2 V, f_o=875 MHz).

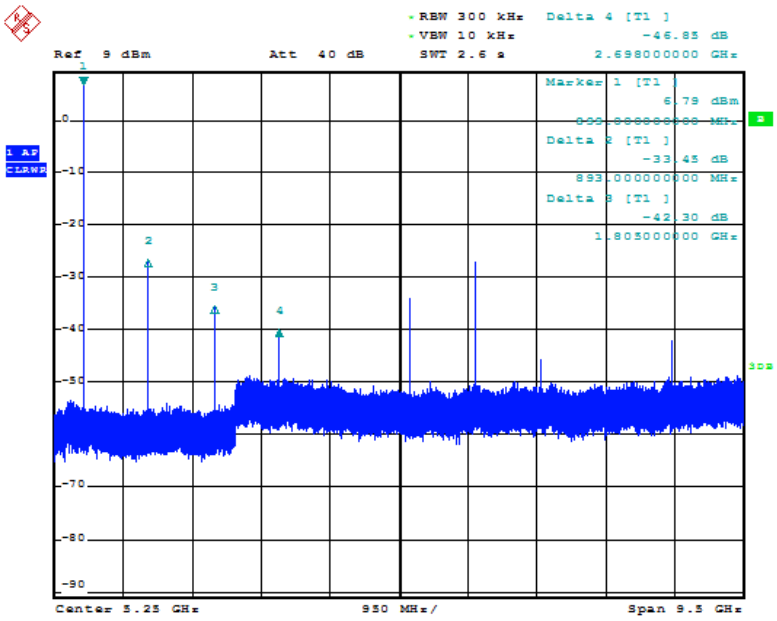


Figure 4.20: Measured output power spectrum.

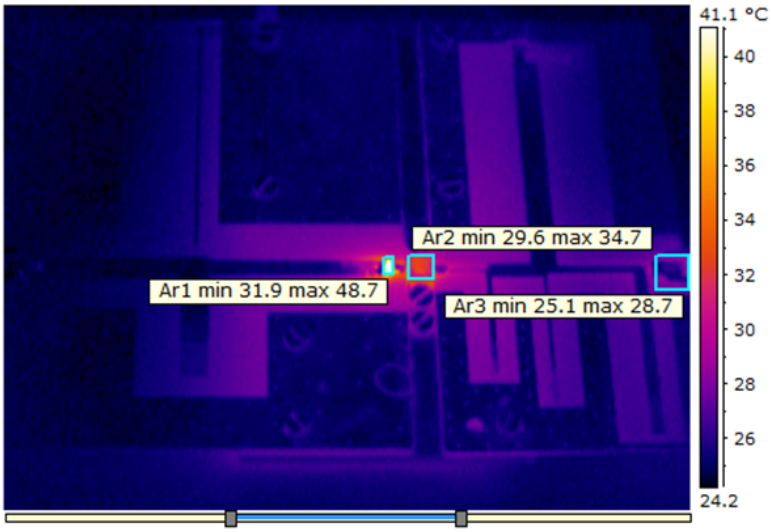


Figure 4.21: Infrared measurement of the circuit heating.

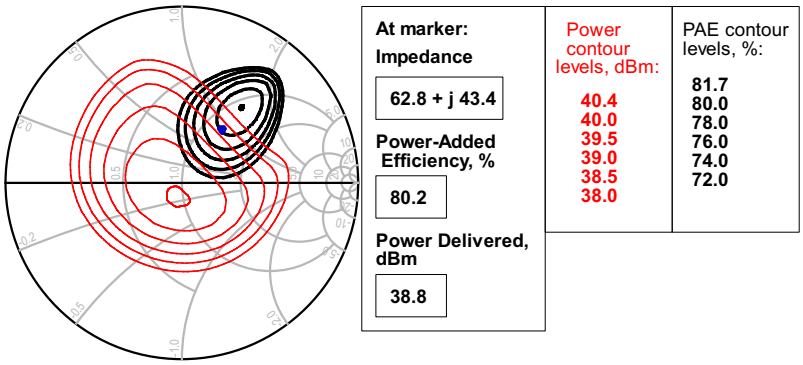
4.3 Design at 1800 MHz Operating Frequency

The second amplifier is designed at 1800 MHz and its design is done with the ultimate aim of a dual-band power amplifier design. Taking into account the final goal, the lengths and widths of the stubs in the main signal path from input to output remain unchangeable. The active device used in this design is also a CreeCGH40006P transistor.

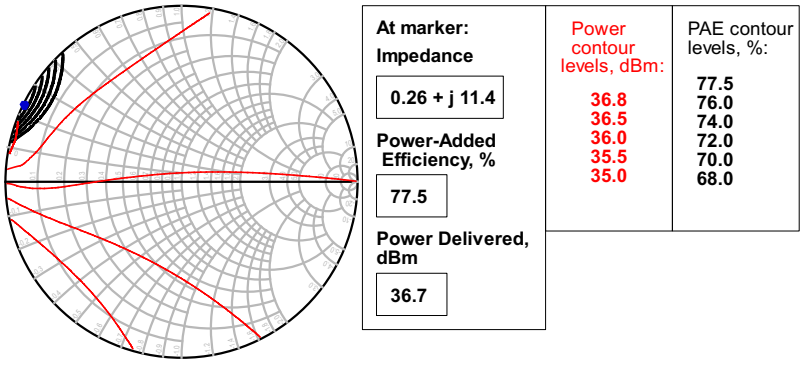
4.3.1 Load Pull / Source Pull Analysis

Similar to what was done for 900 MHz, a load-pull simulation analysis is performed at 1800 MHz and the output power and PAE contours are shown in Figure 4.22. The PAE and Delivered Power Contours at second and third harmonic are shown in Fig. 4.22b and Fig. 4.22c respectively.

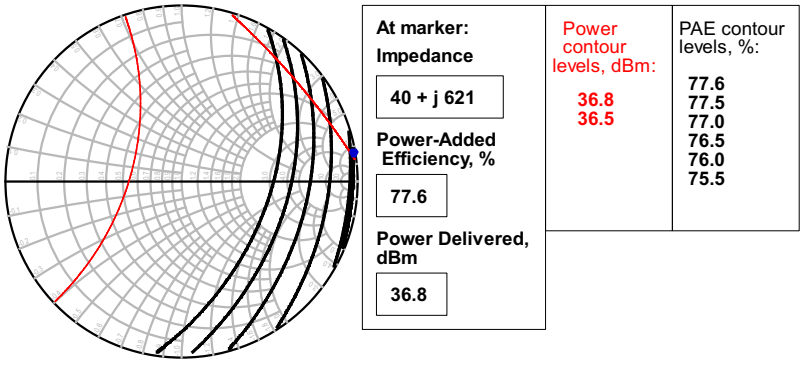
The marker in Fig. 4.22b shows the load impedance of $0.26+j11.4$ at second harmonic. It is on the contour of 77.5% and output power of 36.7 dBm and is chosen close to SC in order to fulfill class-F PA requirements at second harmonic. Similarly the marker in Fig. 4.22c shows the load impedance of $40 + j621$ at third harmonic. This point is in the contour of 77.6% and output power of 36.8 dBm and is chosen close to OC in order to fulfill class-F PA requirements at third harmonic. Finally, the simulation results at fundamental frequency in Fig. 4.22a show that a maximum PAE higher than 80.2% and output power of 38.8 dBm can be achieved.



(a)



(b)



(c)

Figure 4.22: Output power (thin) and PAE (thick) contours from load-pull analysis at (a) fundamental frequency (1800 MHz), (b) 2^{nd} harmonic (3600 MHz) and (c) 3^{rd} harmonic (5400 MHz). (V_{DS} = 28 V, V_{GS} = -2.8 V, P_{in} = 28 dBm)

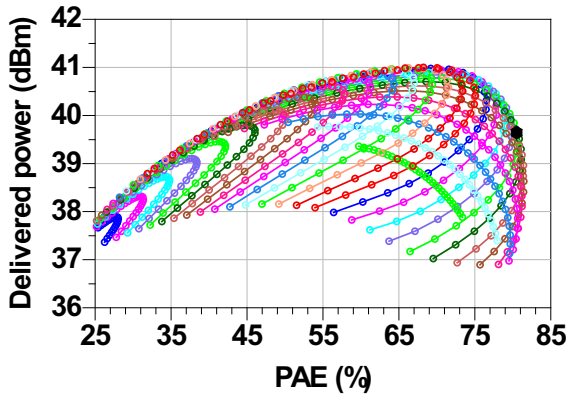


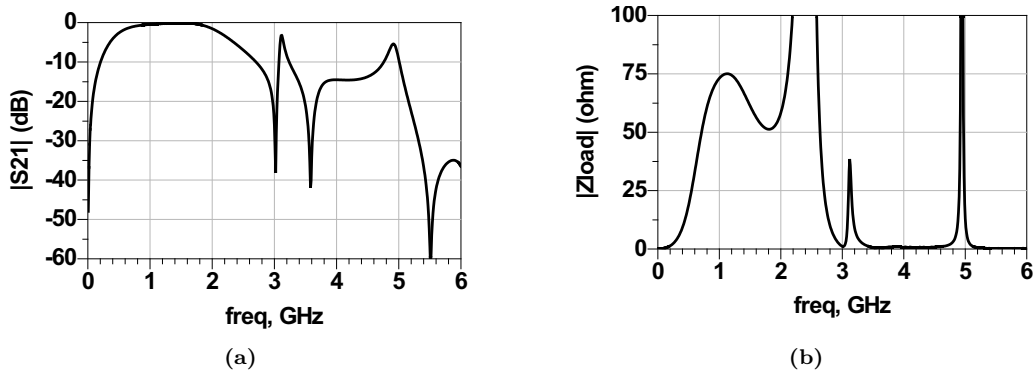
Figure 4.23: Load pull results for PAE (%) versus output power (dBm) at 1800 MHz.

Table 4.6: Load Impedances (Ω) at fundamental frequency (Z_{L1}), 2^{nd} harmonic (Z_{L2}) and 3^{rd} harmonic (Z_{L3}) obtained from load-pull analysis.

	Load Impedance (Ω)
	f_0 = 1800 MHz
Z_{L1}	62.8 + j43.4
Z_{L2}	0.26 + j11.4
Z_{L3}	40 + j621

The contours of harmonics in Fig. 4.22b show a PAE between 68% and 77.5%. At 2^{nd} harmonic, PAE at ideal SC is 55% while at the chosen load of $0.26 + j11.4$ is 77.5%. This shows that by proper harmonic load termination at $0 + j12$ an improvement of 22.5% for PAE was achieved compared to ideal SC termination. For 3^{rd} harmonic there is little difference between PAE and power at ideal OC and the chosen load of $40 + j621$ since they are both on very close contours.

A plot of PAE versus output power for different load values is demonstrated in Figure 4.23. Each trace is obtained by changing the magnitude of the load impedances keeping the phase constant, and this has been done for different phases to cover the whole Smith Chart. The marker dot in this figure corresponds to the marker in Fig. 4.22a and shows that the optimum point is at an input power of 28 dBm. The impedance value of this point is $62 + j43.4$ which gives a PAE of 80.2% and an output power of 38.8 dBm. Z_{L1}, Z_{L2} and Z_{L3} given in Table 4.6 are load impedances that result in an optimum performance at fundamental, second and third harmonics respectively. Using these optimum impedance values, the OMN and IMN of the PA are designed.



(a) (b)

Figure 4.24: Frequency response of the output matching network of Fig. 4.1 designed at 1800 MHz and with second and third harmonic terminated: (a) the S-parameter and (b) the load impedance.

4.3.2 Stability

As it was shown previously in section 4.2.2, there is a need to make the amplifier stable by adding resistors (R_1, R_2 and R_3) to the gate and bias circuit of the IMN of the amplifier. The results of the stable active device are previously shown in Fig. 4.6b.

4.3.3 Simulation Results

The frequency response of the designed OMN with second and third harmonic tuning is shown in Fig. 4.24a. It demonstrates the fundamental matching at 1.8 GHz and corresponding second and third harmonic tuning at 3.6 GHz and 5.4 GHz, respectively. The corresponding impedance values are presented in Fig. 4.24b.

The power amplifier is designed at 1800 MHz. The complete amplifier in Fig. 4.3 is biased in deep class-AB with $V_{GS} = -2.7V$ and is driven into saturation region with an input power of 28 dBm.

The performance of the amplifier is simulated versus both input power and frequency. The simulation results of output power, gain, drain efficiency and PAE versus input power are presented in Fig. 4.25a. With $V_{GS} = -2.7V$ and $V_{DD} = 28V$, a peak PAE of 72%, drain efficiency of 81% and gain of 9.5 dB are obtained at output power of 37.5 dBm at 1800 MHz. The performance versus RF frequency in Fig. 4.25b shows that the amplifier at 1800 MHz achieves a drain efficiency of more than 60% for the frequency band from 1760 MHz to 1940 MHz and it exhibits a very wide response for an efficiency more than 50%.

Output Spectrum of the simulated class-F PA is shown in Fig. 4.26. There is a 47

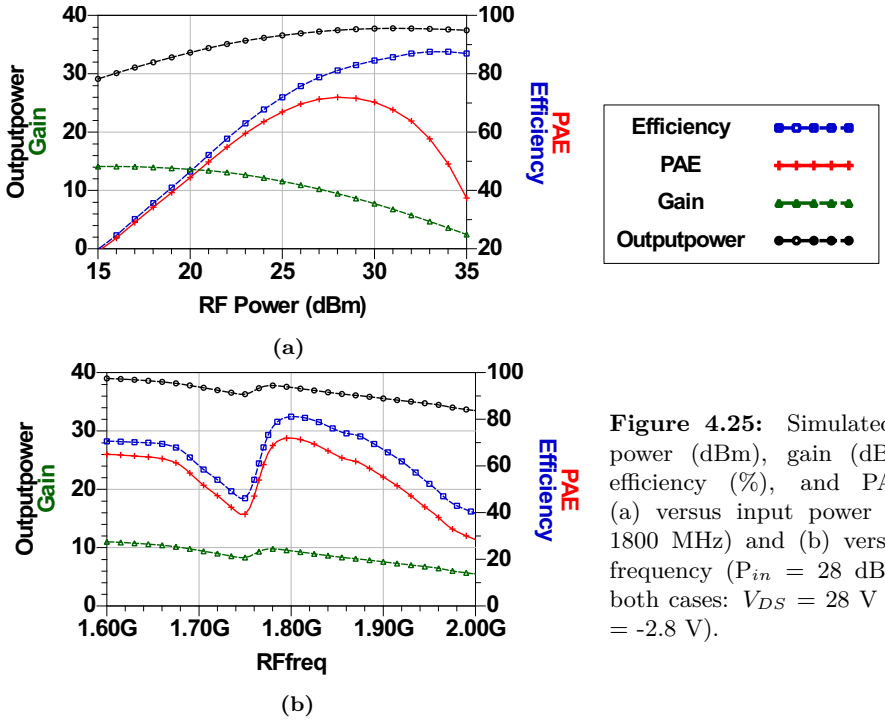


Figure 4.25: Simulated output power (dBm), gain (dB), drain efficiency (%), and PAE (%): (a) versus input power ($freq$ = 1800 MHz) and (b) versus input frequency (P_{in} = 28 dBm). (In both cases: V_{DS} = 28 V and V_{GS} = -2.8 V).

dBc and more difference between the desired output signal and harmonics. Simulated harmonic rejection values are presented in Table 4.7. The spectrum illustrated in Fig. 4.27 shows the comparison of fundamental and harmonic components in drain voltage (V_d) and load voltage (V_{load}) of the amplifier proving that harmonics are properly removed by the output filter.

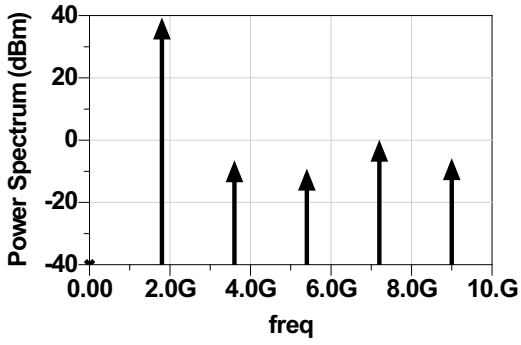


Figure 4.26: Output power spectrum.

Table 4.7: Simulation results for harmonic rejection up to fifth order.

		Harmonic rejection (dBc)			
Freq	P_{in}	2^{nd}	3^{rd}	4^{th}	5^{th}
1800 MHz	28	-47.6	-50.8	-47.6	-47.8

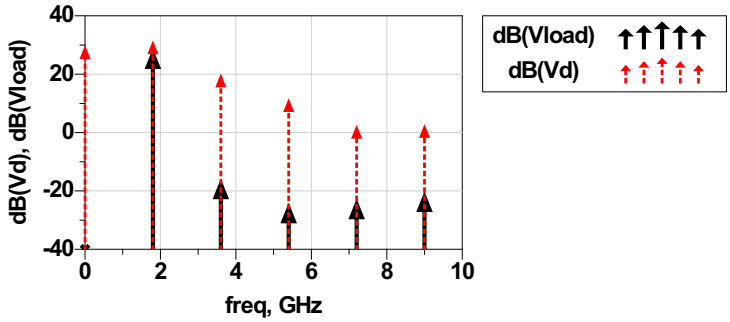


Figure 4.27: The spectrum comparison of drain voltage (V_d) and load voltage (V_{load}) of the amplifier indicating harmonic suppression by the OMN.

4.3.4 Fabrication

An electromagnetic simulation of the IMN and OMN layouts has been carried and corresponding Momentum components are then used to perform a co-simulation of the PA in order to take into account all real effects, giving a more realistic simulation of the PA. The designed PA is fabricated on a 1.5 mm Rogers RO4003 substrate and is shown in Fig. 4.28. The dimension of the fabricated board is 65.3 mm x 120 mm.

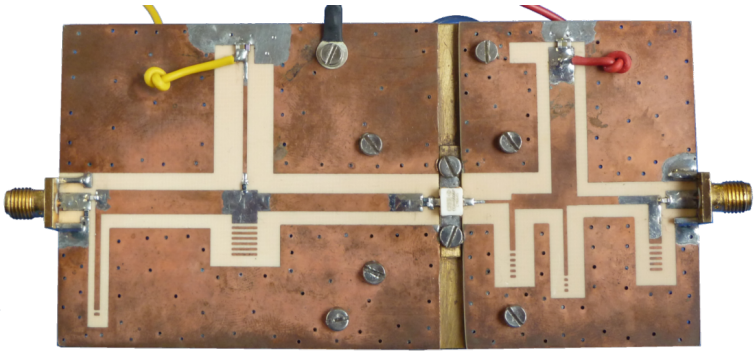


Figure 4.28: Fabricated class-F PA at 1800 MHz.

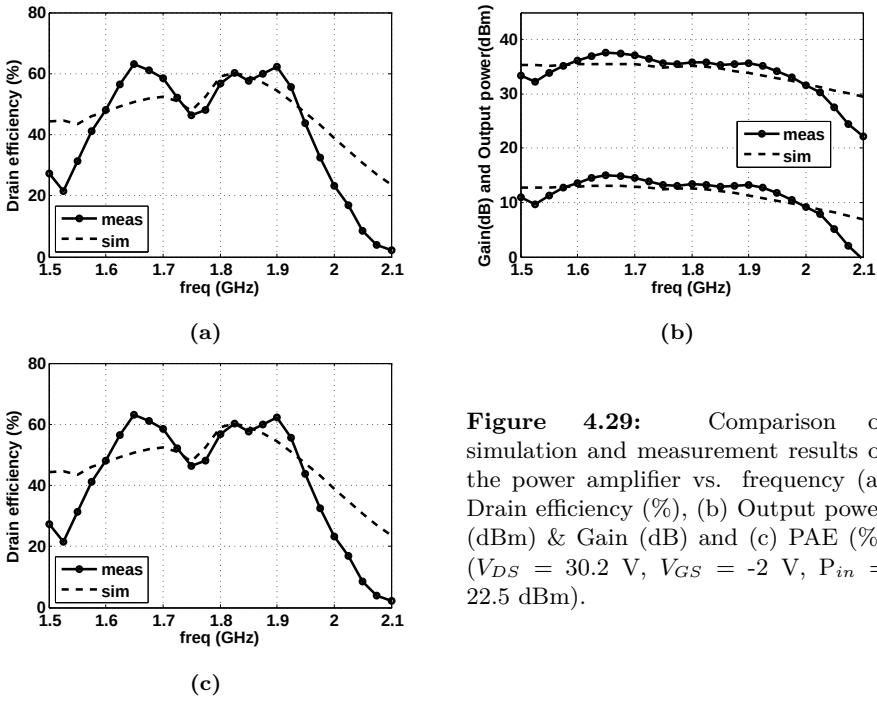


Figure 4.29: Comparison of simulation and measurement results of the power amplifier vs. frequency (a) Drain efficiency (%), (b) Output power (dBm) & Gain (dB) and (c) PAE (%) (V_{DS} = 30.2 V, V_{GS} = -2 V, P_{in} = 22.5 dBm).

4.3.5 Measurement Results

The fabricated amplifier is measured using same setups depicted in Fig. 4.14. To see the total output power spectrum, setup (a) and to measure the exact output power values at certain input powers, setup (b) was used. Measurements versus frequency were carried out at the following bias point: gate voltage V_{GS} = -2 V and drain voltage V_{DS} = 30.2 V. Drain efficiency, PAE, output power and gain results versus frequency are shown in Fig. 4.29. The 1800 MHz amplifier was measured at a back-off power of 22.5 dBm, and it shows a high efficiency of 50% from 1600 MHz - 1730 MHz and 1780 MHz - 1930 MHz.

The biasing of the circuit was optimized for the best performance. Several measurements at different drain voltage were carried out and the one that has the best compromise of the performance between efficiency and power is at drain voltage V_{DS} = 30 V and the gate voltage V_{GS} = -2 V for measurement of amplifiers versus input power.

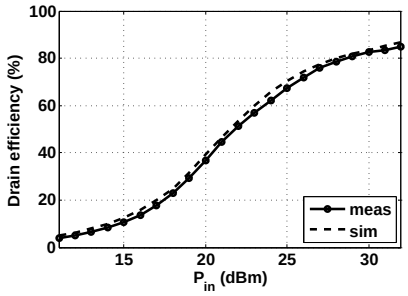
The full comparison of experimental and simulation results versus input power is illustrated in Fig. 4.30. The amplifier features a peak PAE of 72.1% and a drain efficiency of 80.9% achieved for an input power of 29 dBm. The maximum experimental drain efficiency obtained at this frequency is 84.7% at an input power level of 32 dBm.

Output power and gain results versus input power depicted in Fig. 4.30b show a gain of 9.6 dB and output power of 38.66 dBm (7.3 W) is measured for the 1800 MHz amplifier

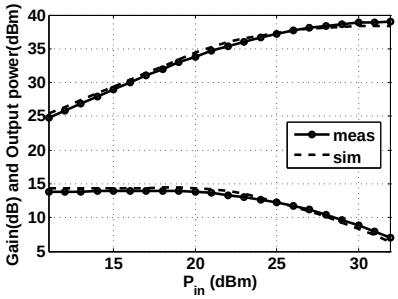
for an input power level of 29 dBm. The summary of the measurement and simulation results at the input power which gives the highest PAE is provided in Table 4.8.

Table 4.8: Measured and simulated values for the PA at the maximum PAE.

Freq (MHz)		V_D (V)	V_G (V)	P_{in} (dBm)	PAE_{max} (%)	η (%)	P_{out} (dBm)
1800	Sim	30	-2	29	72.1	81.7	38.3
	Meas	30	-2	29	72.1	81	38.6



(a)



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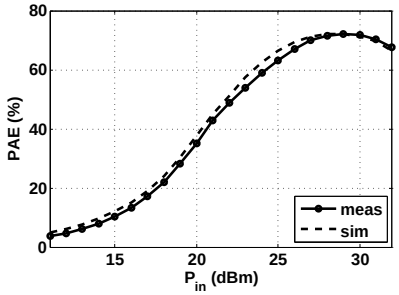


(c)

Figure 4.30: Comparison between simulation and measurement results (a) Drain efficiency (%), (b) Output power (dBm) & Gain (dB), and (c) PAE (%) vs. input power (dBm) (V_{DS} = 30 V and V_{GS} = -2 V).

5

Chapter 5

Dual-Frequency Reconfiguration Class-F Power Amplifier

This chapter presents design process for reconfigurable, high-efficiency class-F power amplifier structure, that achieves dual-band reconfiguration not only at fundamental frequency but also at harmonics. Three prototypes are designed using Hittite SPST and Radant MEMS SPDT and Radant MEMS SPST switches.

5.1 Proposed Dual-Frequency Reconfiguration Concept

The ever-increasing demand of wireless devices for global coverage results in an increasing need for systems to cover multiple frequency bands. To achieve the multi-band coverage, multi-band transceivers and consequently multi-band power amplifiers are needed. A conventional way to achieve dual-band class-F PA is shown in Fig. 5.1. The conventional way is to operate at two different frequency bands of f_1 and f_2. This is done by switching between two different matching networks (MN) where each MN is designed to work at a certain frequency band [110].

This type of reconfiguration is more common for lumped-element output matching networks (OMN) where a compact solution exists. However, this is not interesting for transmission line OMNs because increasing the number of frequency bands leads to a bigger size and higher cost. For transmission line PAs, the approach shown in Fig. 5.2 is proposed. In this concept, the fundamental matching and harmonic matching networks switch between different frequencies (n·f_1 and n·f_2, n:1,2,3) independently. The selection between the two frequency bands is done by switching between two paths of P_1 and P_2. This selection for each block can be implemented in different ways depending on the type of switching device. In this work, two types of single pole single throw (SPST) and single pole double throw (SPDT) switches are intended for use. Hence the selection for each block can be implemented in two ways as shown in Fig. 5.3.

The function of SPST switch to control the length of a single stub is illustrated in Fig. 5.3b. At f_1, the length is equal to L_1 having the switch in OFF state. At f_2 the length is

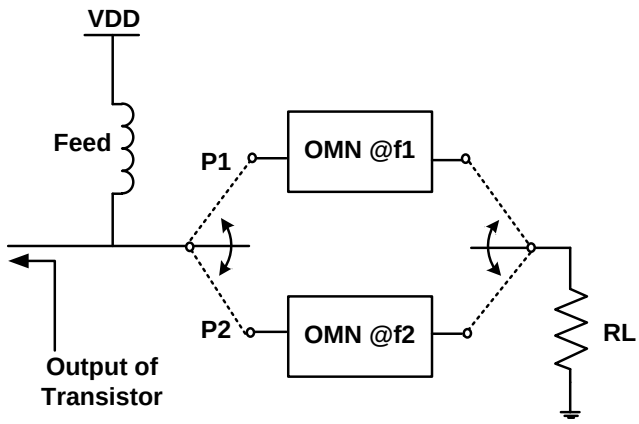


Figure 5.1: The proposed output matching network.

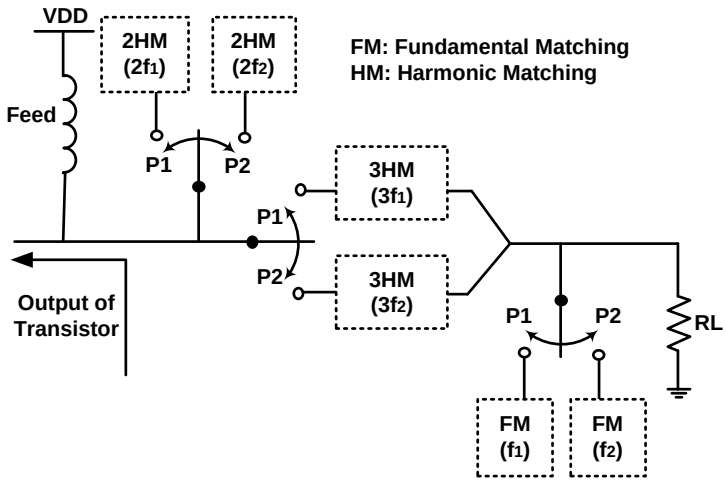


Figure 5.2: The proposed output matching network.

increased to L_2 by adding a length of L_2' at f_2 frequency, having the switch in ON state. The SPDT switches can select between two independent stubs with widths and lengths of W_1/L_1 at f_1 and W_2/L_2 at f_2. This is illustrated in Fig. 5.3c.

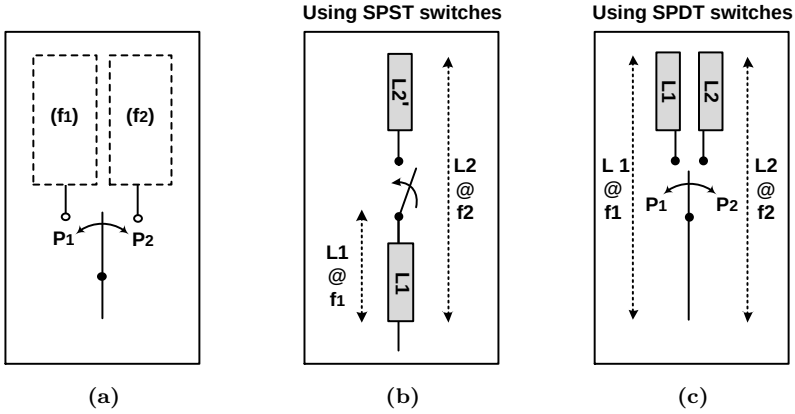


Figure 5.3: (a) Selection between two different path of P_1 and P_2 by incorporation of (b) SPST switches and (c) SPDT switches.

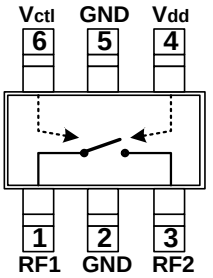


Figure 5.4: Functional diagram of the Hittite switch (HMC550 / 550E).

For a proper switch selection for the mentioned PA application, key parameters that should be considered are maximum power capability, configuration, isolation and leakage, on resistance, and capacitance. The following switches are chosen for the reconfiguration implementation in this thesis:

1. **HMC550/550E**: GaAs MMIC SPST switch from Hittite
2. **RMSW100HP**: MEMS SPST switch from Radant MEMS
3. **RMSW220HP**: MEMS SPDT switch from Radant MEMS

5.2 Frequency Reconfigurable PA using Hittite SPST Switches

5.2.1 Introduction to Hittite Switches

The proposed PA configuration explained in the previous chapter will be used as the base configuration for this design. With the aim of operation at two frequency bands, $f_1 =$ 900 MHz and $f_2 = 1800$ MHz, the first and simplest adaption of the two single frequency PAs into a reconfigurable PA is to use SPST switches as shown in Fig. 5.3b. This idea is the best effective when the switch is ideal, i.e adds no significant loss to the circuits. The SPST used in this design is a GaAs MMIC switch (HMC550/550E) from Hittite and from this point in this thesis, it is referred to as Hittite switch. The functional diagram of the Hittite switch and its operating conditions are shown in Fig. 5.4 and Table 5.1 respectively.

5.2.2 Input and Output Matching Network Design

Due to the non-idealities and parasitics of Hittite switch, placing it in the circuit changes the total electrical length of stubs at each frequency, hence not matching the total expected

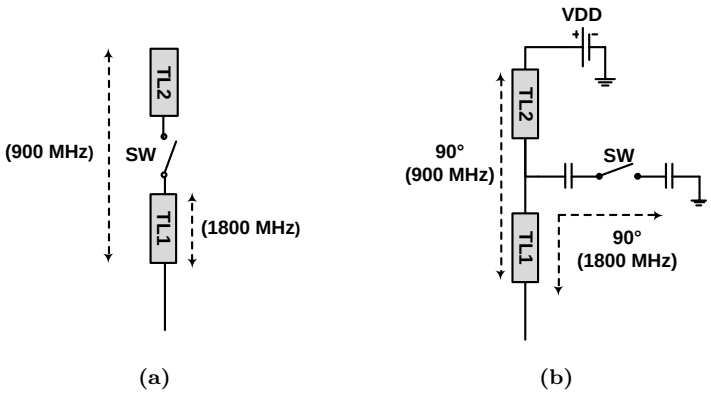


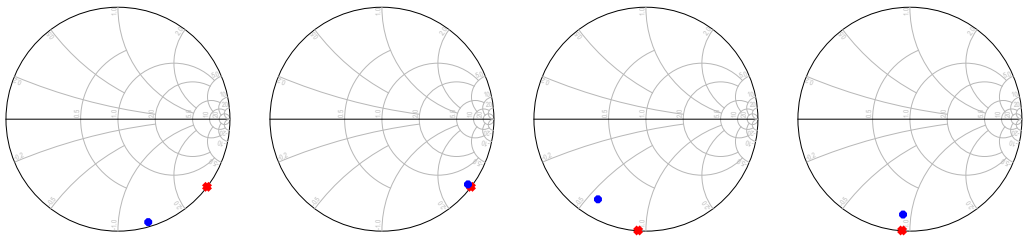
Figure 5.5: The circuit for reconfiguration of (a) open circuit stubs and (b) biasing stubs.

length. This indicates that the length of each stub should be re-tuned at OFF and ON states. The configuration of all open circuit stubs in this design is shown in Fig. 5.5a. The tuning procedure of each open circuit stub is done by calculating the length of TL_1 at 1800 MHz with the switch in OFF state. After the expected length at 1800 MHz is achieved, this length is kept fixed and the length of TL_2 is tuned at 900 MHz with the switch in ON state. The effect of adding a switch is illustrated in Fig. 5.6a and Fig. 5.6c for OFF and ON state respectively, where the red cross is the ideal desired length and the blue square shows the total length of stub including the switch before tuning is applied. The results after tuning are shown in Fig. 5.6b and Fig. 5.6d for 1800 MHz and 900 MHz respectively. It should be noted that the simulated stub including switch shows more loss due to the parasitics of the switch.

Table 5.1: Hittite switch (HMC550 / 550E) operating conditions. V_{dd} & V_{ctl} = 0 V - 5 V, $V_{ctlmax} = V_{dd}$ + 0.2 V, I_{dd} and I_{ctl} = 0.1 μA.

Conditions	$V_{dd} - V_{ctl} \geq 1.2V$	$-0.2V < V_{dd} - V_{ctl} < 0.4V$
$RF_1 - RF_2$	OFF	ON

The reconfiguration is more complex for the biasing sections since the long stubs are the means of transistor biasing and a switch cannot be placed in the middle of the stub. The proposed configuration of Fig. 5.5b is a proper configuration for stub switching and bias at the same time. Unlike reconfiguration for open stubs of Fig. 5.5a, the switch is not placed in cascade between TL_1 and TL_2 but in parallel to ensure a proper path for the gate biasing specifically when the switch is in OFF state. When the switch is ON, the TL_1 is grounded at RF while TL_2 is providing the DC path. The stub length of TL_1 is equal to the expected length of $\lambda/4$ at 1800 MHz with the switch at ON state. When the switch is at OFF state, the stub length is equal to $TL_1 + TL_2$ with an electrical length



(a) **(b)** **(c)** **(d)**

Figure 5.6: The electrical length of stub after adding switch shown in Fig. 5.5a: (a) no-tuning at 1800 MHz (SW=OFF), (b) tuned at 1800 MHz (SW=OFF), (c) no-tuning at 900 MHz (SW=ON), and (d) tuned at 900 MHz (SW=ON).

Table 5.2: Switch configuration of the amplifier in Fig. 5.7 at each operating frequency.

freq (MHz)	SW1	SW2	SW3	SW4	SW5	SW6	SW7
900	ON	ON	OFF	OFF	ON	ON	ON
1800	OFF	OFF	ON	ON	OFF	OFF	OFF

of $\lambda/4$ at 900 MHz providing an open circuit for RF signal, and has an electrical length of $\lambda/2$ at second harmonic providing a short circuit at this frequency. This configuration is used for both gate and drain biasing.

Taking into account the periodic behavior of the transmission-line and the concept for reconfiguration explained above, the proposed reconfigurable class-F PA structure based on only SPST switches is illustrated in Fig. 5.7. This PA works at two frequency bands, $f_1 = 900$ MHz and $f_2 = 1800$ MHz. In the IMN there are three SPST Hittite semiconductor switches (SW1, SW2, and SW3). In the OMN there are four SPST Hittite semiconductor switches (SW4, SW5, SW6, and SW7). The combination of the switches for each frequency is stated in Table 5.2. DC blocking capacitors are required for each switch.

5.2.3 Simulation Results

The power amplifier in Fig. 5.7 is designed to work at 900 MHz and 1800 MHz with switch configuration given in Table 5.2. It is biased with $V_{GS} = -2.7V$ and $V_{DD} = 28V$ and is driven into saturation region with input power of 25 dBm at 900 MHz and 28 dBm at 1800 MHz. The simulation results versus input power and versus frequency are illustrated in Fig. 5.8 for both 900 MHz and 1800 MHz. The simulation results versus input power exhibited in Fig. 5.8a for 900 MHz show a peak PAE of 69.2%, drain efficiency of 72.5% and gain of 13.5 dB are obtained at an output power of 38.5 dBm. At 1800

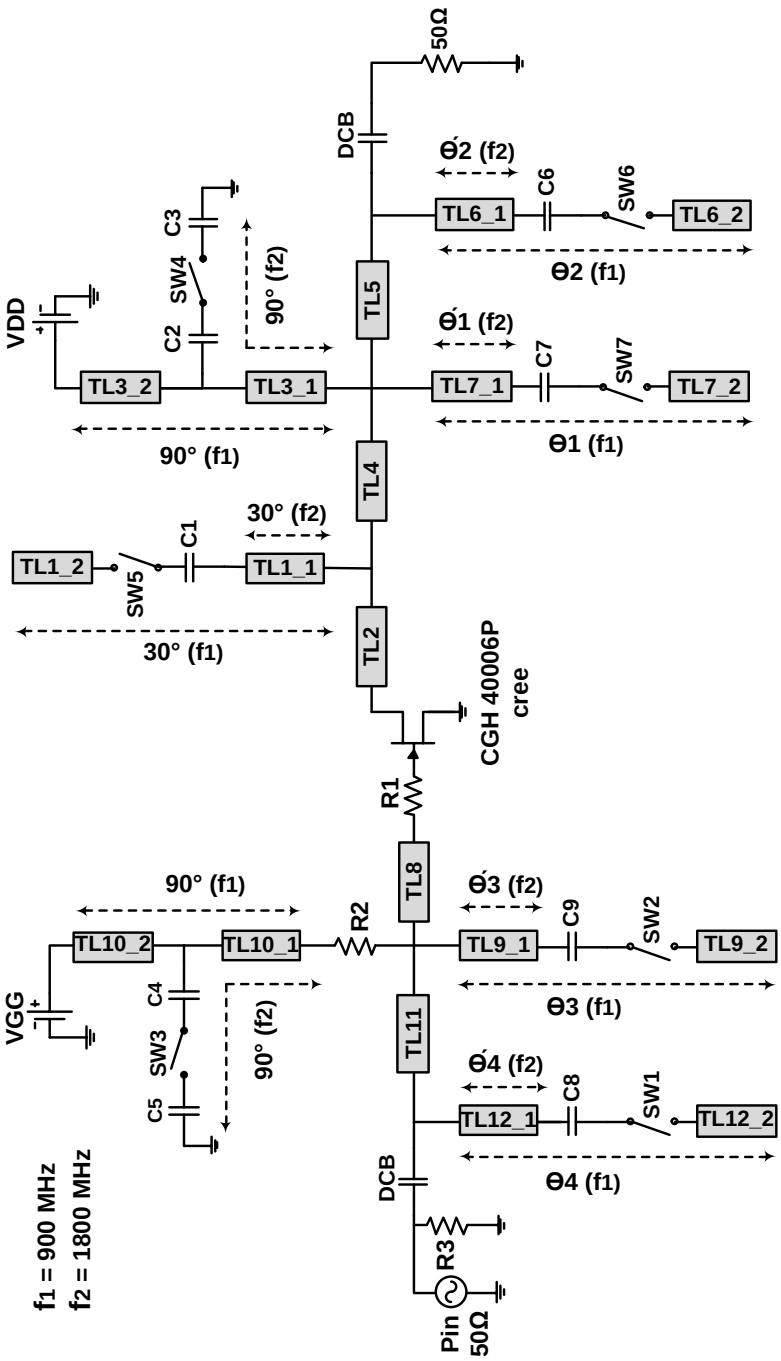


Figure 5.7: The proposed reconfigurable class-F PA using Hittite SPST switches.

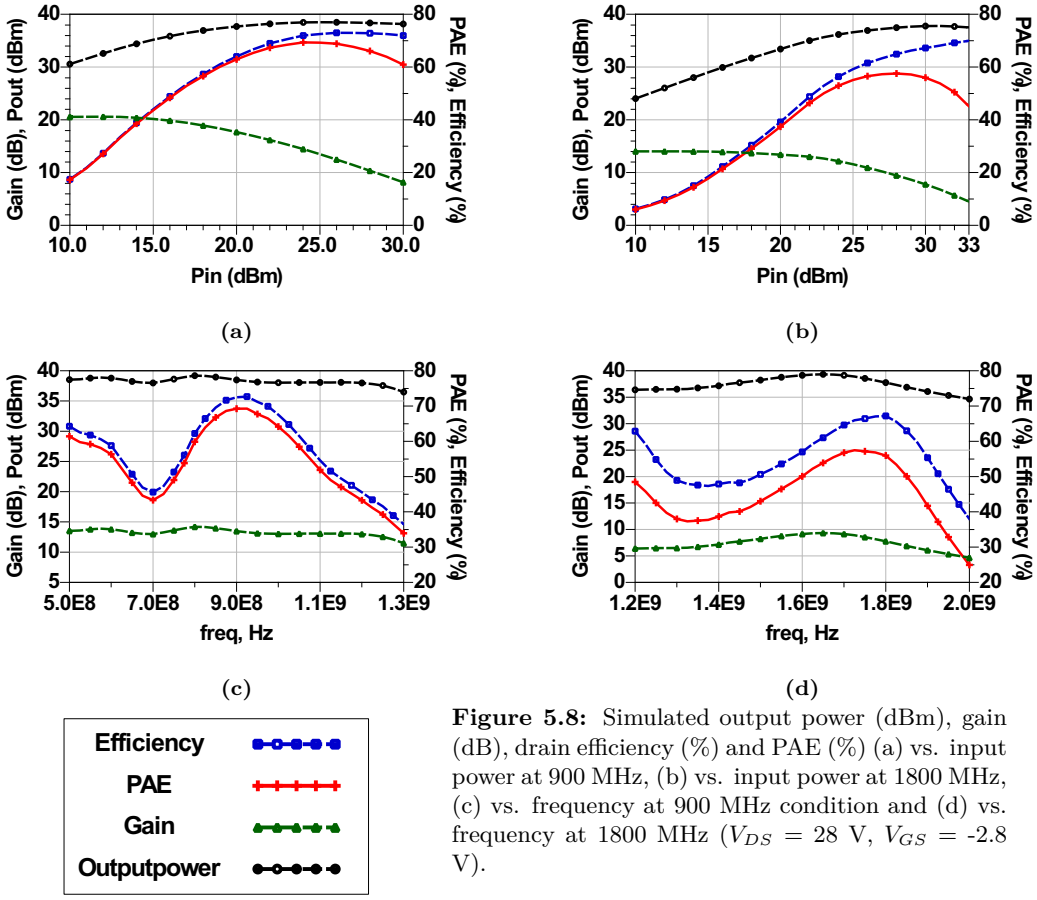
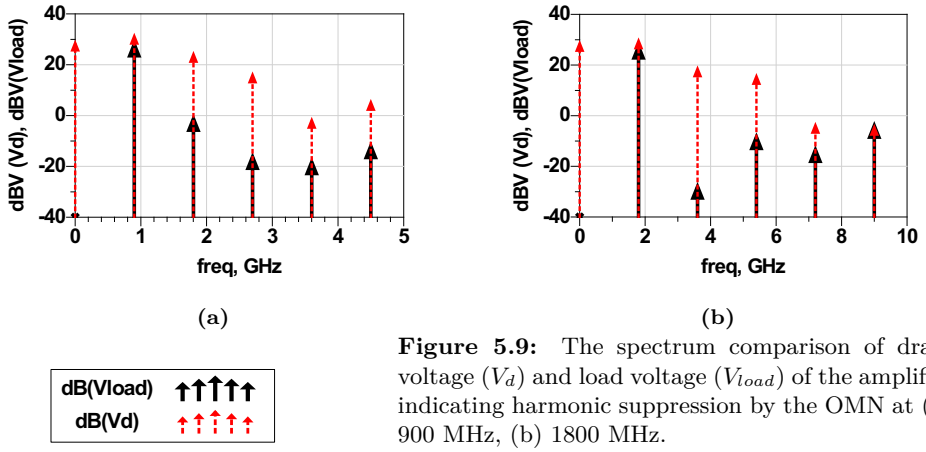


Figure 5.8: Simulated output power (dBm), gain (dB), drain efficiency (%) and PAE (%) (a) vs. input power at 900 MHz, (b) vs. input power at 1800 MHz, (c) vs. frequency at 900 MHz condition and (d) vs. frequency at 1800 MHz (V_{DS} = 28 V, V_{GS} = -2.8 V).

MHz simulation results are shown in Fig. 5.8b. A peak PAE of 57.5%, drain efficiency of 64.9% and gain of 9.5 dB are obtained at an output power of 37.5 dBm.

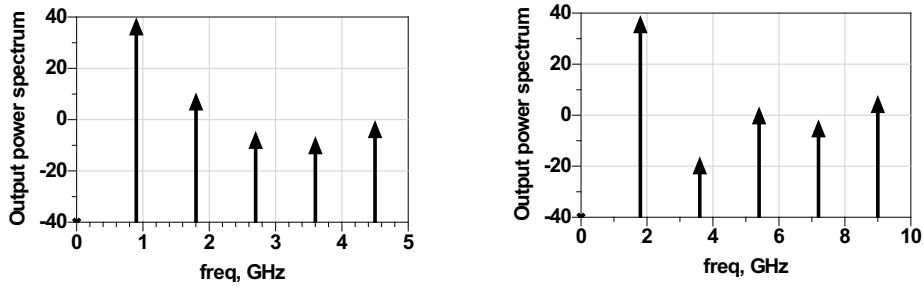
The performance versus RF frequency is illustrated in Fig. 5.8c for 900 MHz and Fig. 5.8d for 1800 MHz. At 900 MHz operating condition, the amplifier achieves a PAE higher than 60% in the frequency band from 805 MHz to 1035 MHz. At 1800 MHz operating condition, the amplifier achieves a PAE higher than 55% in the frequency band from 1690 MHz to 1830 MHz.

The comparison of fundamental and harmonic components in drain voltage (V_d) and load voltage (V_{load}) of the amplifier illustrated in Fig. 5.9a at 900 MHz condition and in Fig. 5.9b at 1800 MHz condition show proper harmonic removal from V_d resulting in a high harmonic rejection. The output power Spectrum of the simulated class-F PA is shown in Fig. 5.10. Simulated harmonic rejection values are presented in Table 5.3.



(a) (b)

Figure 5.9: The spectrum comparison of drain voltage (V_d) and load voltage (V_{load}) of the amplifier indicating harmonic suppression by the OMN at (a) 900 MHz, (b) 1800 MHz.



(a) (b)

Figure 5.10: Output power spectrum at (a) 900 MHz, (b) 1800 MHz.

Table 5.3: Simulation results for harmonic rejection up to fifth order.

		Harmonic rejection			
Freq	P_{in}	2^{nd}	3^{rd}	4^{th}	5^{th}
MHz	dBm	dBc			
900	25	-29.3	-44.3	-46.3	-36
1800	28	-55.3	-35.7	-34.7	-31.2

5.2.4 Fabrication

The switch application diagram and footprint are illustrated in Fig. 5.11a and Fig. 5.11b respectively. Pin 1 is input signal (RF_1), Pin 2 and 5 are RF ground (GND), Pin 3 is output signal (RF_2), Pin 4 is supply voltage (V_{dd}), and Pin 6 is control voltage (ctl). The RF pins are DC coupled, supply is fed through a 100Ω resistor and control voltage is fed through a 100Ω resistor and a 1 nF shunt capacitor to ground. The designed PA

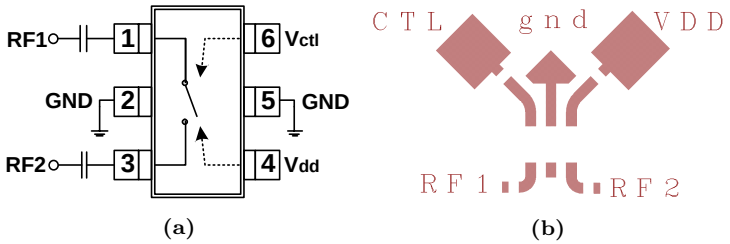


Figure 5.11: (a) The application diagram and (b) the footprint of hittite semiconductor SPST switch.

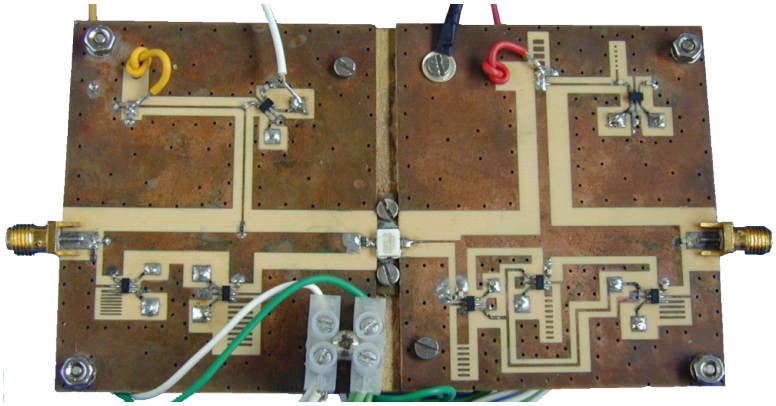


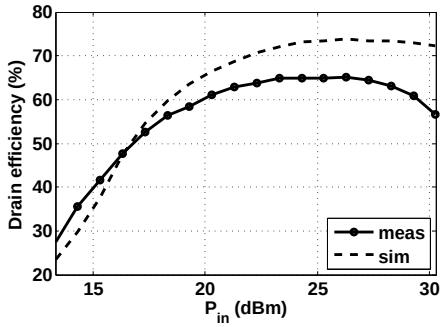
Figure 5.12: Fabricated dual-frequency reconfigurable class-F PA at 900 MHz and 1800 MHz using SPST Hittite switches.

is fabricated on a 1.5 mm Rogers RO4003 substrate and it is shown in Fig. 5.12. The dimension of the fabricated board is 72 mm x 125 mm.

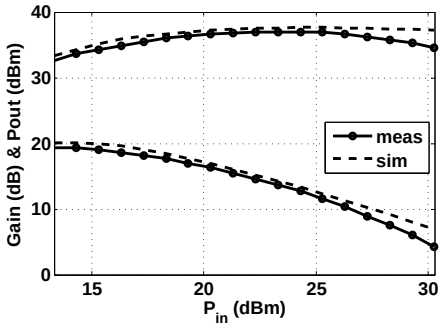
5.2.5 Measurement Results

To validate the design against simulation results, the fabricated amplifier is measured using the setups depicted in chapter 4, Fig. 4.14. The measurements were carried out at the following bias point: drain voltage V_{DS} = 25 V and gate voltage V_{GS} = -2.2 V. The results versus input power for 900 MHz shown in Fig. 5.13 exhibit that amplifier features a peak PAE of 62.1% and drain efficiency of 64.9% at an input power level of 23.3 dBm, while this amplifier gives a peak drain efficiency of 73.7% at an input power of 26 dBm. Output power and gain results versus input power depicted in Fig. 5.13b show a gain of 13.7 dB and a measured output power of 37 dBm (5 W) at 900 MHz for an input power level of 23.3 dBm.

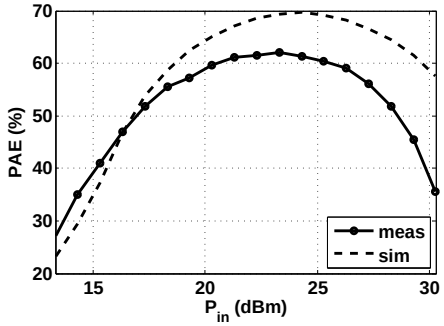
After 900 MHz measurements, the amplifier was measured at 1800 MHz with the



(a)



(b)



(c)

Figure 5.13: Comparison of simulation and measurement results of (a) Drain efficiency (%), (b) Output power (dBm) & Gain (dB) and (c) PAE (%) vs. input power (V_{DS} = 25 V, V_{GS} = -2.2 V, freq = 900 MHz).

corresponding switch configuration given in Table 5.2. The measurement results are illustrated in Fig. 5.14. At this frequency, the amplifier did not accomplish the expected performance and after input power of 25 dBm, most of the switches in the output matching network were burnt. At 900 MHz, output switches were in ON state, they broke when they were in OFF state at 1800 MHz. It was concluded that either the Voltage or current in the stubs are higher than the maximum rating value given by the manufacturer. This is studied in next section.

5.2.6 Study for Device Reliability

Maximum voltage over switch occurs in OFF state and can be calculated from equation 5.1.

$$V_{pk} = 10^{\frac{P_{dBm}-10}{20}} \tag{5.1}$$

From Hittite switch datasheet, the maximum RF input power of the switch is 34 dBm for a 50Ω matched impedance.According to equation 5.1, the maximum voltage for

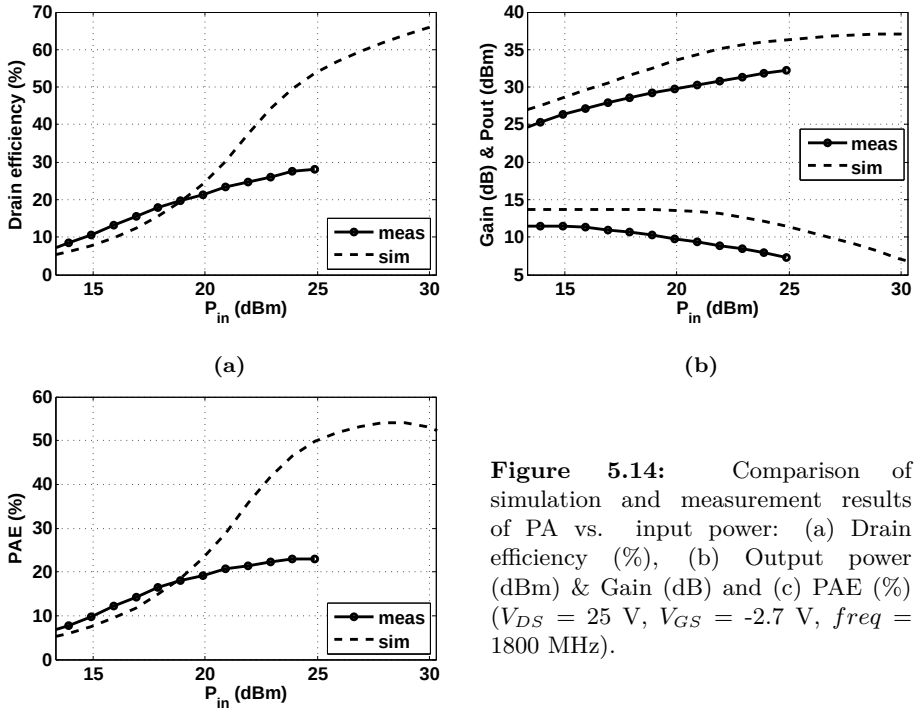


Figure 5.14: Comparison of simulation and measurement results of PA vs. input power: (a) Drain efficiency (%), (b) Output power (dBm) & Gain (dB) and (c) PAE (%) (V_{DS} = 25 V, V_{GS} = -2.7 V, $freq$ = 1800 MHz).

a power of 34 dBm at 50Ω is calculated to have a peak of 15.8 V. Further simulations of the amplifier for input powers ranging from 10 dBm to 30 dBm show that the peak voltage over the switch SW5 in OFF state is higher than the maximum rated value. It can be confirmed from simulation results presented in Fig. 5.15b that the voltages over the switch are high when they are in OFF state. With a drain voltage of 25 V this voltage value goes from 9.5 V for P_{in} = 10 dBm to 50 V for P_{in} = 30 dBm. The switch reaches to 15 V at an input power of 14 dBm indicating that for input powers higher than 14 dBm, the switch breaks down. The voltage over the switches for a single input power of 20 dBm are illustrated in Fig. 5.16. The simulation results in Fig. 5.17 show a value of 25 V on the DC capacitor located before switches for powers from 10 dBm to 30 dBm at both frequencies.

The function of the switch is illustrated in Fig. 5.18. With $v_{RF} = \mathrm{V}_{pk}\cos(\omega t)$:

at DC: $\mathrm{V}_{A_{DC}} = \mathrm{V}_{B_{DC}} = \mathrm{V}_{dd}$

at AC: $v_A = \mathrm{V}_{A_{DC}} + v_{in}$

For v_{in} = 0 V:

$v_A = \mathrm{V}_{A_{DC}}$,

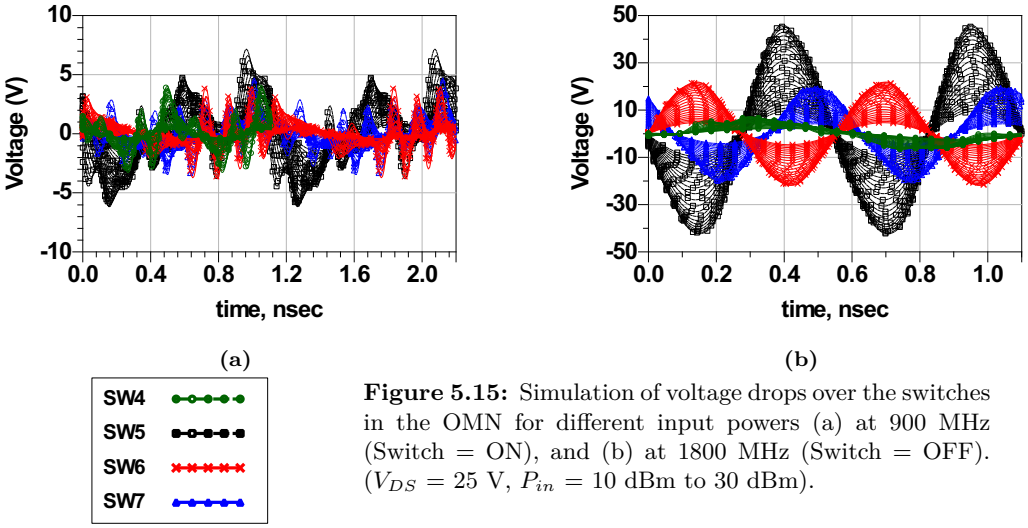


Figure 5.15: Simulation of voltage drops over the switches in the OMN for different input powers (a) at 900 MHz (Switch = ON), and (b) at 1800 MHz (Switch = OFF). (V_{DS} = 25 V, P_{in} = 10 dBm to 30 dBm).

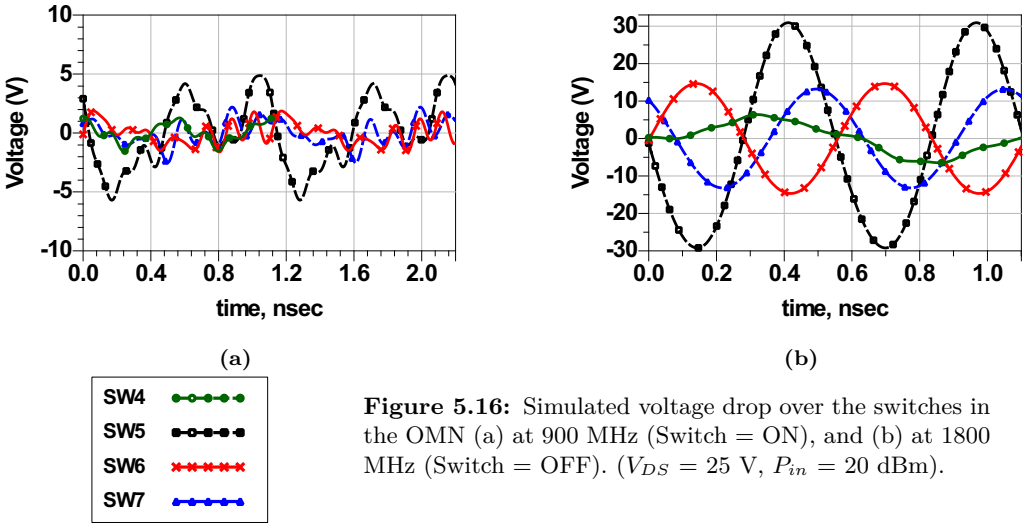


Figure 5.16: Simulated voltage drop over the switches in the OMN (a) at 900 MHz (Switch = ON), and (b) at 1800 MHz (Switch = OFF). (V_{DS} = 25 V, P_{in} = 20 dBm).

Else for $v_{in} = v_{RF} \neq 0$ V:

$v_{A_{max}} = v_{RF} + \mathrm{V}_{A_{DC}}$

$v_{A_{min}} = \text{-}v_{RF} + \mathrm{V}_{A_{DC}}$.

When $\mathrm{V}_{pk} = \mathrm{V}_{A_{DC}}$, then $v_{A_{max}} = 2\mathrm{V}_{A_{DC}}$ and $v_{A_{min}} = 0$.

In order to increase the voltage capability and avoid switch breakdown, two switches can be used in series connection to reduce the voltage over the switches to half compared to a single switch.Although using two switches in series reduces the voltage stress on the switch and is an option to overcome the breakdown voltage of the switch in this PA

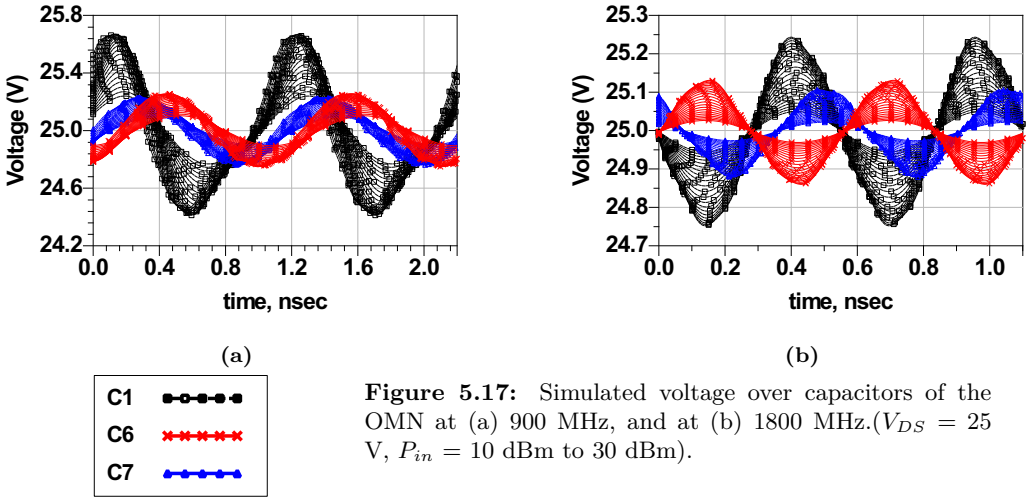


Figure 5.17: Simulated voltage over capacitors of the OMN at (a) 900 MHz, and at (b) 1800 MHz.(V_{DS} = 25 V, P_{in} = 10 dBm to 30 dBm).

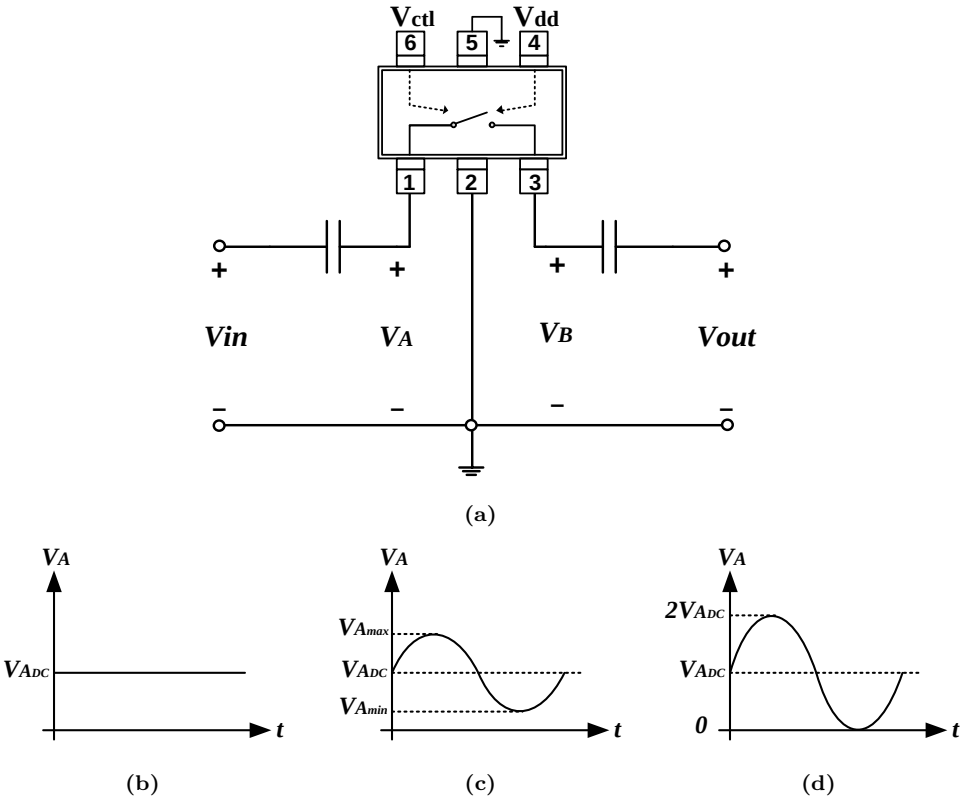


Figure 5.18: (a) Function of switch, (b) $v_{in} = 0$, (c) $v_{in} = v_{RF}$, and (d) $v_{in} = v_{RF}$ with $V_{pk} = V_{ADC}$.

design, it doubles the number of switches and hence the losses and leads to much more complication of switch control and PA design. In this PA design, the aim is to achieve the reconfiguration with the minimum number of switches possible. Hence new switches with higher power capabilities are chosen for the PA design explained in the next section.

5.3 Frequency Reconfigurable PA using MEMS Switches - Design A

5.3.1 Introduction to MEMS Switches

RF switches in MEMS technology with higher power capabilities deliver high linearity, high isolation, and low insertion loss in a chip-scale package configuration. The absolute maximum voltages for these switches are ±110 V of Gate-Source and Drain-Source. This indicates that the maximum voltage over the switch can be 110 V. The functional diagram of the MEMS switches of this design are presented in Fig. 5.19. In SPST MEMS switch exhibited in Fig. 5.19a, drain is where the input signal (RF_1) is connected, source is where the output signal (RF_2) is connected and gate is the control voltage for turning switch ON or OFF. In the SPDT MEMS switch in Fig. 5.19b, drain is where input signal (RF_1) is connected, source 1 is one output signal (RF_2), and source 2 in the other output signal (RF_3). The voltage applied to gate 1 controls the path from RF_1-RF_2 and gate 2 controls the path from RF_1-RF_3. The operating conditions of SPST MEMS and SPDT MEMS are shown in Table 5.4 and Table 5.5 respectively.

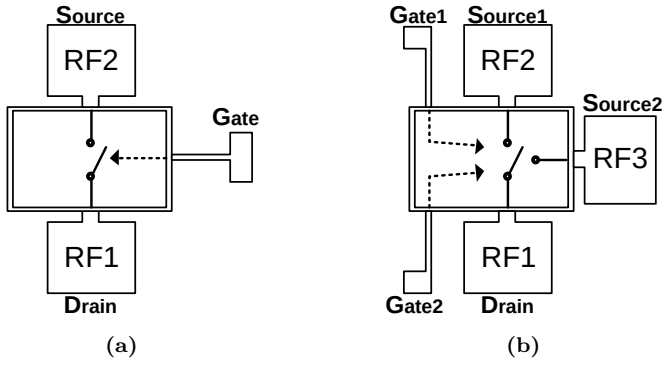


Figure 5.19: Functional diagram of the (a) MEMS SPST switch (RMSW100HP), and (b) MEMS SPDT switch (RMSW220HP).

Table 5.4: MEMS SPST switch (RMSW100HP) operating conditions.

	Gate-gnd Voltage	Signal Path State
State 1	±90 V	ON
State 2	0 V	OFF

Table 5.5: MEMS SPDT switch (RMSW200HP) operating conditions.

	Voltage to ground		Signal Path State	
	$Gate_1$	$Gate_2$	RF_1-RF_2	RF_1-RF_3
State 1	±90 V	0 V	ON	OFF
State 2	0 V	±90 V	OFF	ON

5.3.2 Input and Output Matching Network Design

The input matching network is designed using SPST RMSW100HP from Radant MEMS as indicated in Fig. 5.20a. The output matching network incorporates SPDT switches in open circuit stubs as indicated in Fig. 5.20b. For the gate and drain biasing of the device, SPST switches are used with the configuration shown in Fig. 5.20c for the same reason as explained in the previous section, to assure a proper DC path for drain and gate biasing. Otherwise, if the same configuration of Fig. 5.20a is used by placement of SPST in the middle of stub or by the configuration of Fig. 5.20b to use an SPDT switching between two stubs, there will be no current path to bias the gate or drain to activate the transistor. From the proposed configuration in Fig. 5.20c, TL_1 is grounded at RF with the switch in ON state while TL_2 still provides the DC path. The stub length of TL_1 is equal $\lambda/4$ at 1800 MHz with the switch in ON state. When the switch is in OFF state, the stub length is equal to $TL_1 + TL_2$ with an electrical length of $\lambda/4$ at 900 MHz providing an open circuit for RF signal, and has an electrical length of $\lambda/2$ at second harmonic providing a short circuit at this frequency. This configuration is used in both gate and drain of the transistor.

The proposed frequency reconfigurable class-F PA structure based on MEMS switches is illustrated in Fig. 5.21. This PA works at two frequency bands, $f_1 = 900$ MHz and $f_2 = 1800$ MHz. The IMN consists of two SPST MEMS switches (SW1, and SW2) and one SPST Hittite semiconductor switch (SW3). To reduce the complexity of the PA only SPST switches are used in the IMN. In addition, the proposed PA performance is more sensitive to output matching filter than the input. However, there is a need of more design freedom for OMN hence SPDT switches are used in the stubs with an exception for the biasing line as explained before. The OMN consists of one SPST MEMS switch (SW4) and three SPDT MEMS switches (SW5, SW6, and SW7). The combination of the switches for each frequency is stated in Table 5.6.

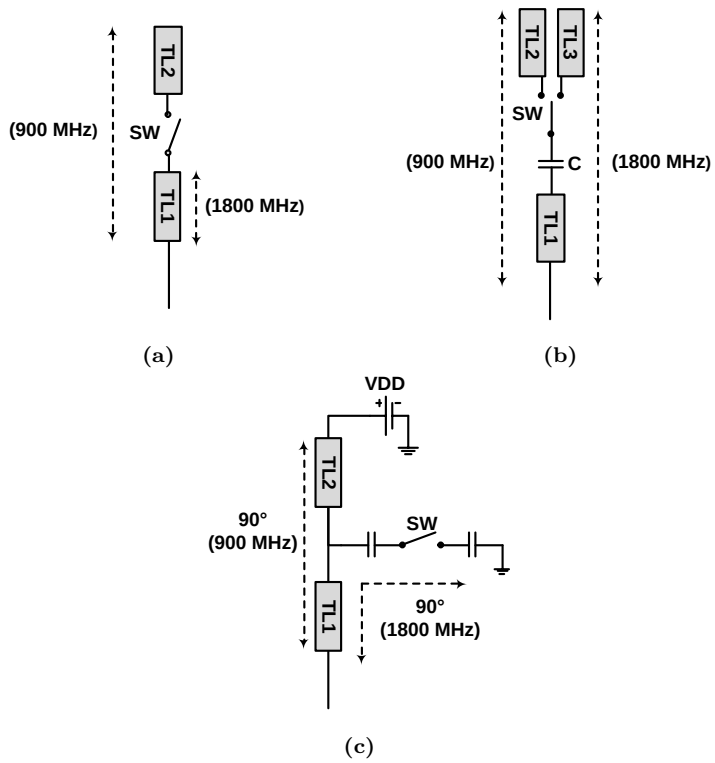


Figure 5.20: The circuit for reconfiguration of (a) input open circuit stubs, (b) output open circuit stubs, and (c) biasing stubs.

The design procedure for the amplifier starts with tuning the stubs at each frequency. In the IMN only SPST switches are used therefore it starts with design at 1800 MHz, and once the length of TL1 in Fig. 5.20a is calculated for the switch in OFF state, the switch is turned ON and TL2 is calculated in a way that TL1 + switch + TL2 has a length equal to the stub length at 900 MHz. The design procedure for the OMN is different since it incorporates SPDT switches. According to the configuration of open stubs in the OMN indicated in Fig. 5.20b, at 900 MHz the length of TL_{900} (TL1 + TL2) and at 1800 MHz the length of TL_{1800} (TL1 + TL3) are calculated. Depending on the performance of the PA, TL1 which is a common stub for both frequencies can be calculated and hence the length of TL2 and TL3.

For drain and gate sections from Fig. 5.20c, at 1800 MHz the length of TL1 is calculated for this switch in ON state. Once the lengths of these stubs are calculated at 1800 MHz, the length of TL2 is calculated at 900 MHZ for the switch in OFF state in a way that TL1 + TL2 be equal to the required length at this frequency.

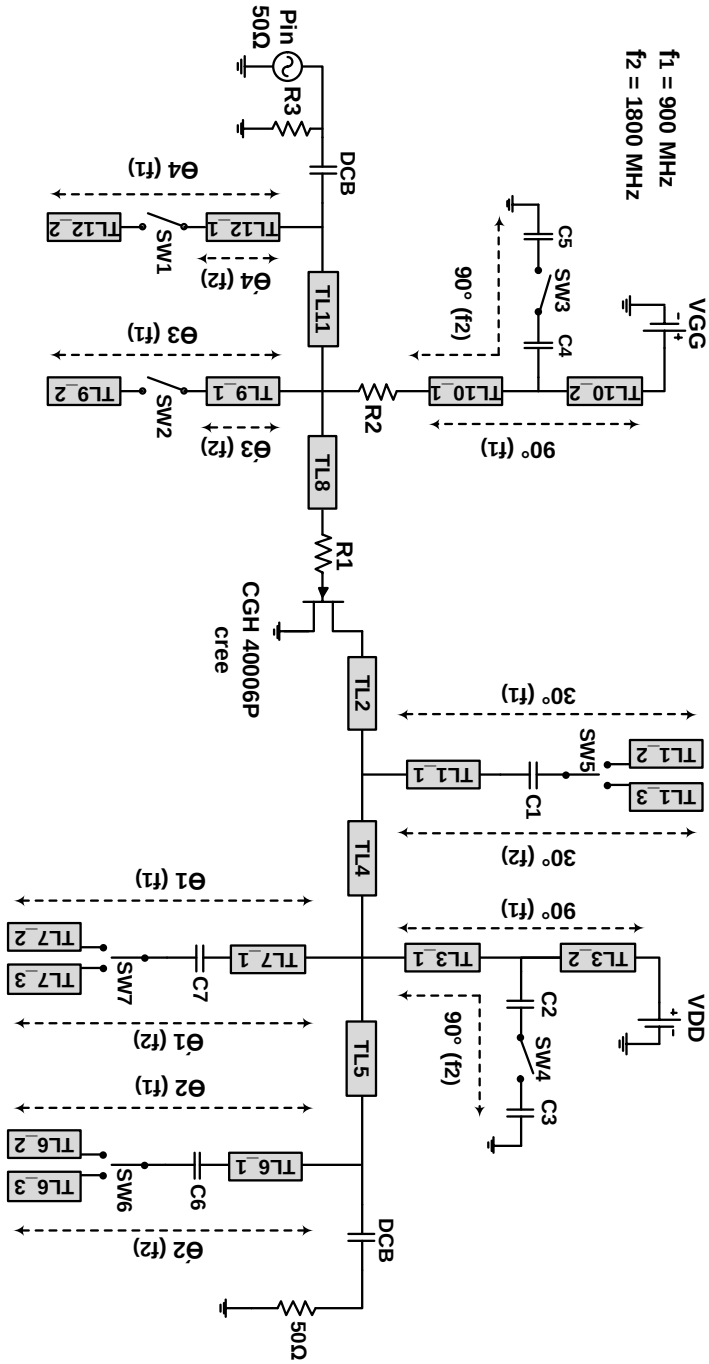


Figure 5.21: The proposed frequency reconfigurable class-F PA using MEMS SPST and SPDT switches (Design A).

Table 5.6: Switch configuration of the amplifier in Fig. 5.21 at each operating frequency.

freq (MHz)	SW1	SW2	SW3	SW4	SW5	SW6	SW7
900	ON	ON	OFF	OFF	RF_1-ON	RF_1-ON	RF_1-ON
1800	OFF	OFF	ON	ON	RF_2-ON	RF_2-ON	RF_2-ON

5.3.3 Simulation Results

The power amplifier in Fig. 5.21 is designed to work at 900 MHz and 1800 MHz with switch configuration given in Table 5.6. It is biased with $V_{GS} = -2.5V$ and $V_{DD} = 28V$ and is driven into saturation region with an input power of 24 dBm at 900 MHz and 29 dBm at 1800 MHz.

5.3.3.1 PA Reliability

It is desired to have a minimum voltage over switches for reliability issues. The length of TL1 in the reconfiguration concepts shown in Fig. 5.20 is critical in the OMN design since it defines the voltage standing wave at the point where the switch is placed. Considering a length of TL_{900} = TL1 + TL2 at 900 MHz and TL_{1800} = TL1 + TL3 at 1800 MHz, the length of TL1 can have any value from 0 mm to TL_{1800}. This length has a direct effect on the maximum voltage on the switch.

The voltage and current at each point of a TL with length z terminated with a load Z_L in Fig. 5.22, can be calculated as the sum of an incident V^+ and a reflected V^- wave:

$$V(z) = V^+ e^{-j\beta_c z} + V^- e^{+j\beta_c z} \tag{5.2}$$

$$I(z) = I^+ e^{-j\beta_c z} + I^- e^{+j\beta_c z} = \frac{1}{Z_0}\left[V^+ e^{-j\beta_c z} - V^- e^{+j\beta_c z}\right] \tag{5.3}$$

Where β_c and Z_0 are the phase constant and characteristic impedance of the TL respectively. Now when the TL is terminated with an open circuit such as in this design, by moving back from $z = 0$ toward the beginning of the TL, the corresponding current and voltage can be calculated. At $z = 0$, there is an open circuit and therefore there is no current at this point (I^- = -I^+), but there is twice voltage ($V^- = V^+$). Moving back toward the beginning of the TL an amount of $z = \lambda/4$, Γ reaches to -1 and $z = 0$. This point of TL has the minimum voltage and maximum current. Since in the case of this design there are two operating frequencies where one of them (1800 MHz) is exactly twice the other one (900 MHz), the length of $\lambda/4$ is twice at 900 MHz compared to $\lambda/4$ at 1800 MHz. This brings more complexity on choosing the right length of TL1 since where the TL has the minimum voltage at 900 MHz, it has the maximum voltage at 1800 MHz,

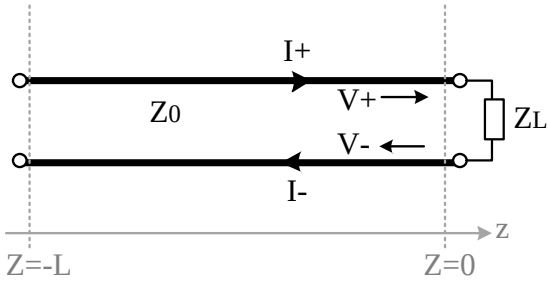


Figure 5.22: Transmission line terminated with a load Z_L.

exhibited in Fig. 5.23. Therefore the TL1 values that result in TL2 = $\lambda/4$ at 900 MHz and TL3 = $\lambda/4$ at 1800 MHz should be avoided to reduce the risk of switch breakdown.

Since the OMN switches are SPDT switches, the corresponding switch state at each frequency of operation is presented in Table 5.7. At 900 MHz, drain and source 1 are connected (RF_1-ON or RF_1-RF_2-ON) and drain and source 2 are not connected (RF_2-OFF or RF_1-RF_3-OFF). At 1800 MHz, drain and source 2 are connected (RF_2-ON or RF_1-RF_3-ON) and drain and source 1 are not connected (RF_1-OFF or RF_1-RF_2-OFF). The voltages over the switches have been simulated for each of these states and the results are provided in Fig. 5.24 for input power ranging from 10 dBm to 30 dBm. By having a capacitor before the switches, the DC component of the voltage is removed, hence the maximum voltage over the switch is reduced, increasing the switch reliability. The simulated voltages over the capacitors go over 50 V (Fig. 5.25), bringing a requirement on the capacitor maximum operating voltage. The capacitors in this design have a maximum voltage capability of 100 V.

The simulated voltages over the switches at the input power that gives the maximum PAE are presented in Fig. 5.26. Maximum voltage appears on the switches in the OFF state, seen over switch SW5 on RF_1-OFF and over the switch SW6 on RF_2-OFF. As expected the voltage over the switch in ON state is minimal, less than 6 V. The maximum voltage that can be placed over the switch drain-source and gate-source is 110 V. These simulations show that the switch works under reliable conditions.

5.3.3.2 PA Performance

Fig. 5.27 illustrates the simulation results versus input power and versus frequency for both 900 MHz and 1800 MHz. At 900 MHz, peak PAE of 79% is obtained at input power of 24 dBm. At this power, the PA demonstrates a drain efficiency of 81.5% and a gain of

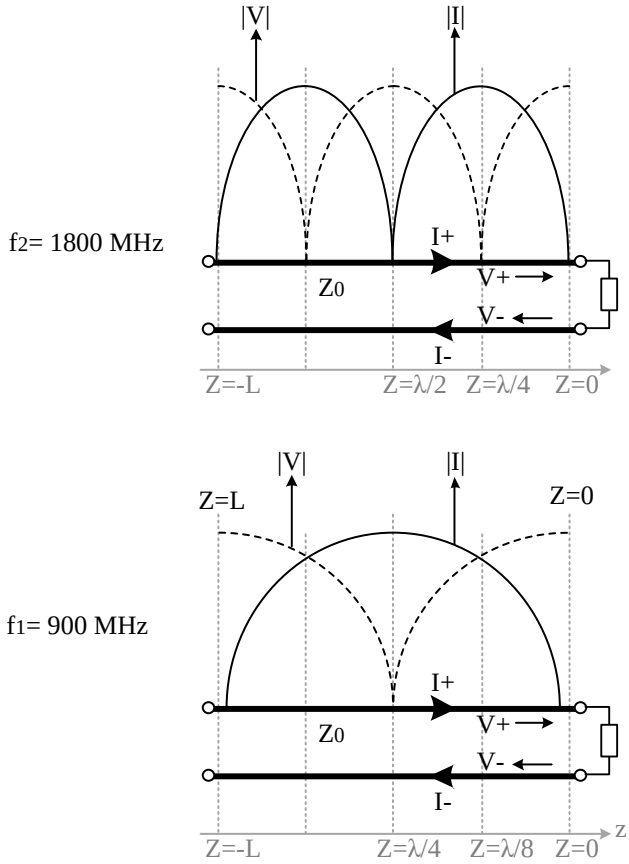


Figure 5.23: Theoretical voltage and current along the length of transmission line terminated by an open load for 900 MHz and 1800 MHz.

Table 5.7: Switch configuration of the amplifier in Fig. 5.21 at each operating frequency.

				switch states	
freq (MHz)		Port 1	Port 2	Drain-Source 1	Drain-Source 2
900	RF_1-ON	Drain	Source 1	ON	OFF
	RF_2-OFF	Drain	Source 2	ON	OFF
1800	RF_2-ON	Drain	Source 2	OFF	ON
	RF_1-OFF	Drain	Source 1	OFF	ON

15 dB while delivering an output power of 39 dBm. At 1800 MHz a peak PAE of 68.3% is obtained at an input power of 29 dBm, a drain efficiency of 76.2% and a gain of 9.8 dB while delivering an output power of 38.8 dBm.

The performance versus RF frequency is illustrated in Fig. 5.27c for 900 MHz and in

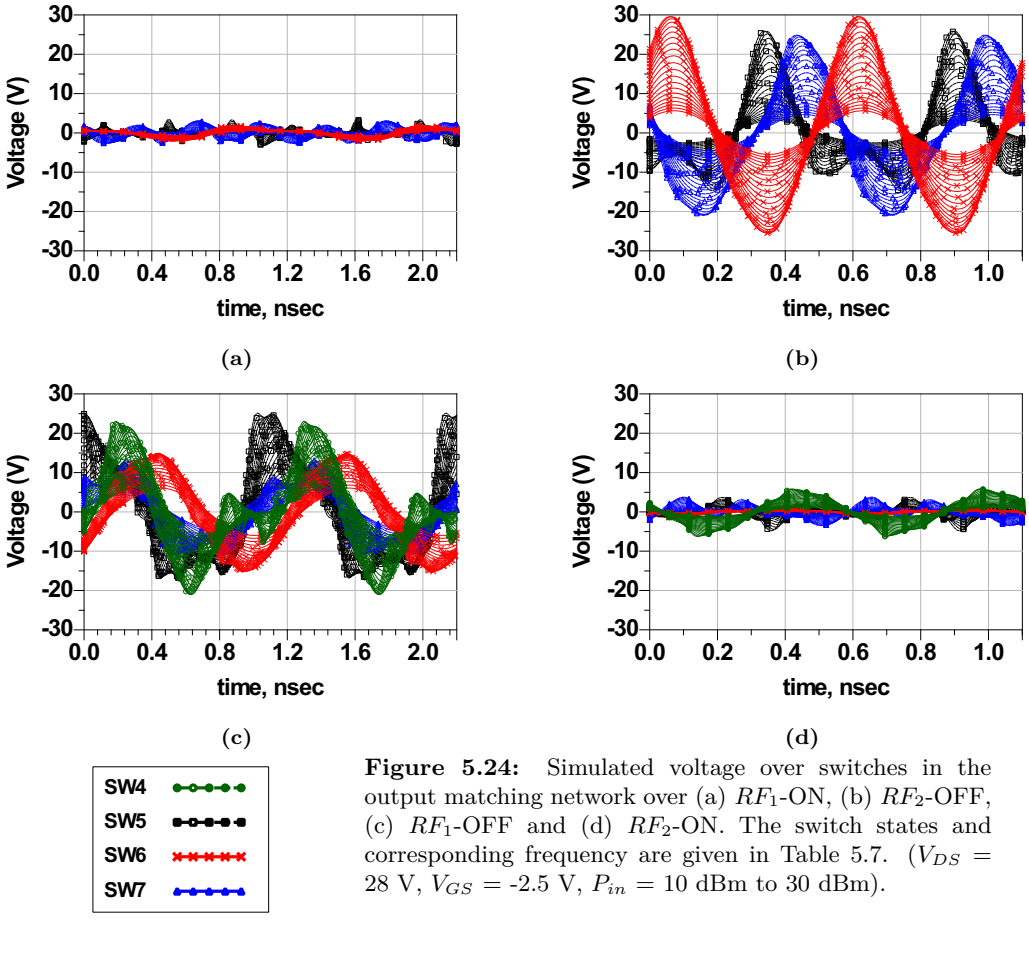


Figure 5.24: Simulated voltage over switches in the output matching network over (a) RF_1-ON, (b) RF_2-OFF, (c) RF_1-OFF and (d) RF_2-ON. The switch states and corresponding frequency are given in Table 5.7. (V_{DS} = 28 V, V_{GS} = -2.5 V, P_{in} = 10 dBm to 30 dBm).

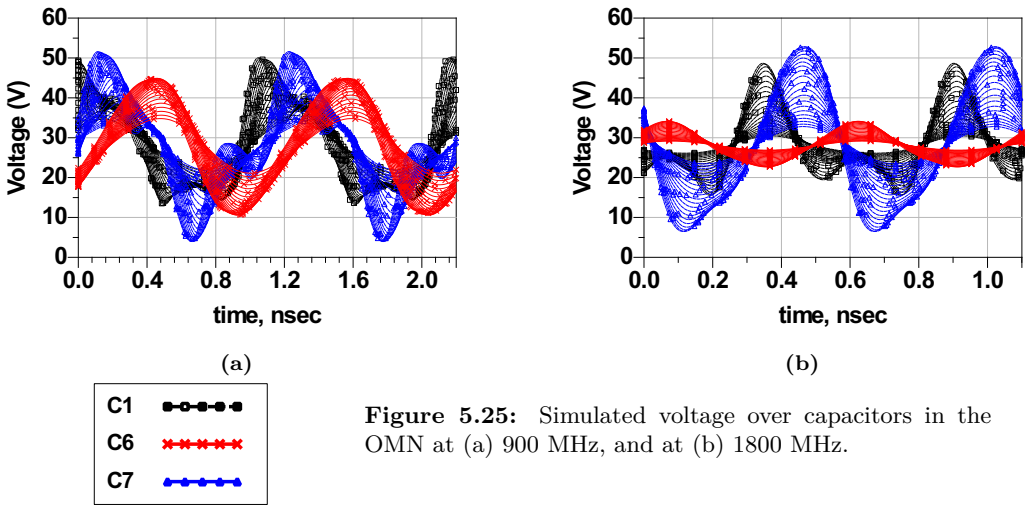


Figure 5.25: Simulated voltage over capacitors in the OMN at (a) 900 MHz, and at (b) 1800 MHz.

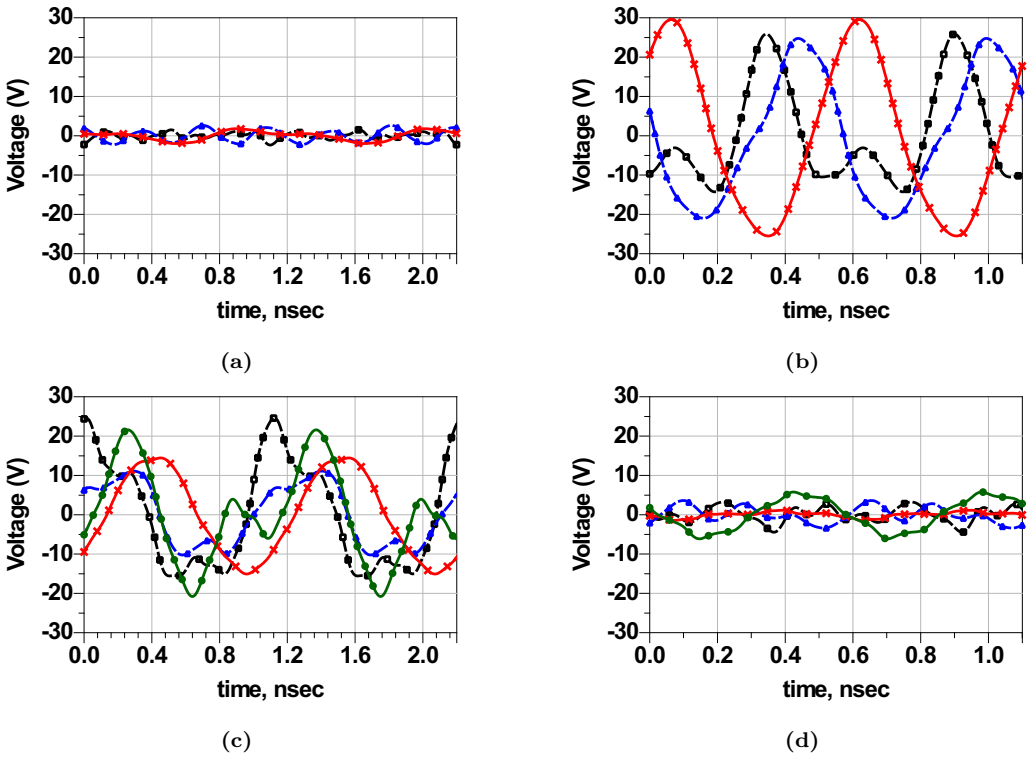


Figure 5.26: Simulated voltage over switches in the output matching network at input power that gives maximum PAE: (a) RF_1-ON, (b) RF_2-OFF, (c) RF_1-OFF and (d) RF_2-ON. The switch states and corresponding frequency are given in Table 5.7. (V_{DS} = 28 V, V_{GS} = -2.5 V, P_{in} = 25 dBm at 900 MHz, P_{in} = 28 dBm at 1800 MHz).

Fig. 5.27d for 1800 MHz, showing that the PA is designed for the best performance at the operating frequency. At 900 MHz operating condition, the amplifier achieves a PAE higher than 60% in a bandwidth of 225 MHz, from 815 MHz to 1040 MHz, reaching to 79% at 900 MHz, providing an output power in the range from 38.5 dBm at 815 MHz to 38 dBm at 1040 MHz. At 1800 MHz operating condition, the amplifier achieves a PAE higher than 60% in a bandwidth of 170 MHz, from 1730 MHz to 1900 MHz, reaching to 68.6% at 1810 MHz. The output power at this frequency band goes from 38.9 dBm at 1730 MHz to 37.1 dBm at 1900 MHz.

The comparison of fundamental and harmonic components in drain voltage (V_d) and load voltage (V_{load}) of the amplifier illustrated in Fig. 5.28a at 900 MHz condition and in Fig. 5.28b at 1800 MHz condition shows how harmonics are removed from V_d by

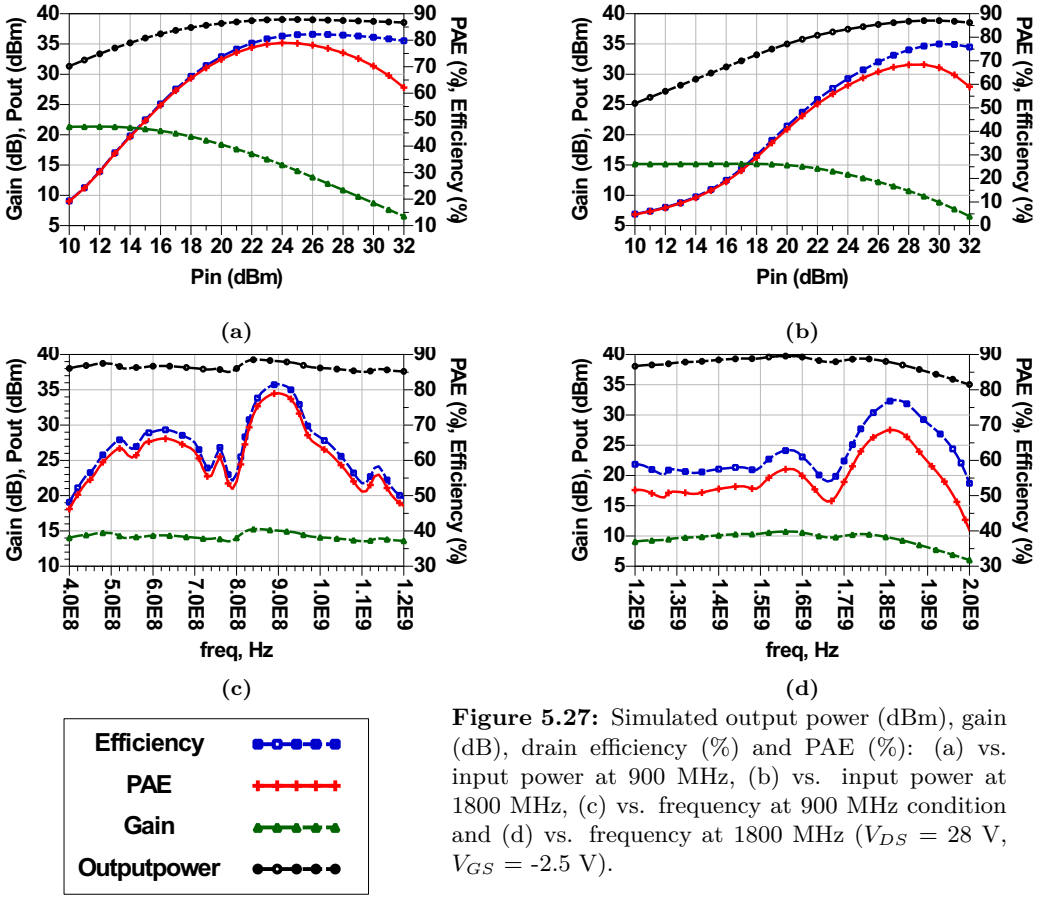
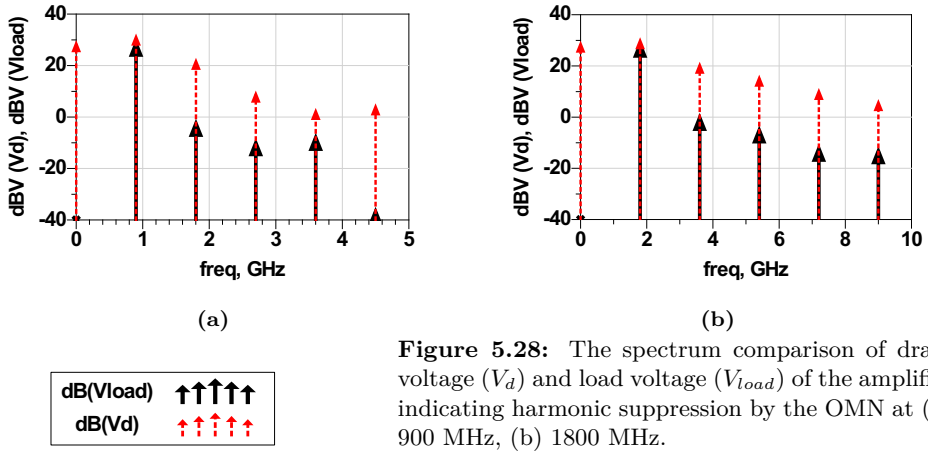


Figure 5.27: Simulated output power (dBm), gain (dB), drain efficiency (%) and PAE (%): (a) vs. input power at 900 MHz, (b) vs. input power at 1800 MHz, (c) vs. frequency at 900 MHz condition and (d) vs. frequency at 1800 MHz (V_{DS} = 28 V, V_{GS} = -2.5 V).

Table 5.8: Simulation results for harmonic rejection up to fifth order.

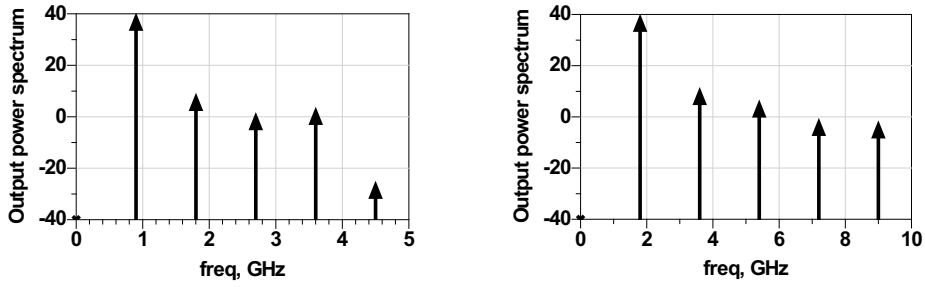
		Harmonic rejection			
Freq	P_{in}	2^{nd}	3^{rd}	4^{th}	5^{th}
MHz	dBm	dBc			
900	24	-31.1	-38.6	-36.5	-65.3
1800	29	-28.6	-33.5	-40.6	-41.6

the output filter of the amplifier, resulting in a good harmonic rejection. The output power Spectrum of the simulated class-F PA is shown in Fig. 5.29 and the corresponding harmonic rejection values are presented in Table 5.8.



(a) (b)

Figure 5.28: The spectrum comparison of drain voltage (V_d) and load voltage (V_{load}) of the amplifier indicating harmonic suppression by the OMN at (a) 900 MHz, (b) 1800 MHz.



(a) (b)

Figure 5.29: Output power spectrum at (a) 900 MHz, (b) 1800 MHz.

5.3.4 Fabrication

The electromagnetic simulations of the IMN and OMN layouts have been carried out by the method of moments in Agilent Momentum^{TM} tool and the corresponding electromagnetic models (Momentum components) are used to simulate the real performance of the PA. This simulation setup, which is shown in Fig. 5.30, takes into account the physical behavior of the PA and the parasitics. The switch application diagram and footprint are illustrated in Fig. 5.31. The general application diagrams of MEMS switches are exhibited in Fig. 5.31a. According to the manufacturer, V_G may be of either polarity with a rise-time at least 10 μs for the optimal lifetime. Resistors R_S and R_D (or inductors L_S and L_D) should be used to provide a path to DC ground from Source and Drain of the switch. The gold backside metallization of the switches allowed them to be assembled on the PCB using silver epoxy. Bond pads on the die are made of gold and gold bondwires were utilized to attach the PCB to the die pads. The designed

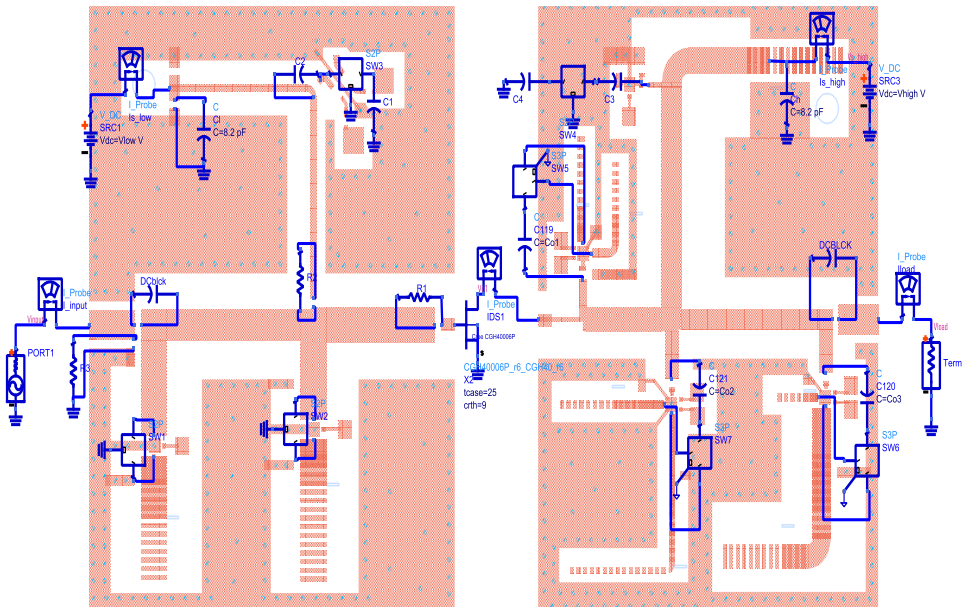


Figure 5.30: Input and output matching components created using momentum placed on the schematic.

PA is fabricated on a 1.5 mm Rogers RO4003 substrate and is shown in Fig. 5.32. The dimension of the fabricated board is 70 mm x 112 mm. The PA uses a backside PCB for voltage distribution of the switches and its layout is shown in Fig. 5.32b. This PCB is designed using Altium Designer software. There is a metallic plate below the PA to act as a heatsink for the transistor.

5.3.5 Measurement Results

The fabricated amplifier in Fig. 5.32 is measured using the setups depicted in chapter 3, Fig. 4.14. The optimal performance is achieved for drain voltage V_{DS} = 29.5 V and gate voltage V_{GS} = -1.9 V for 900 MHz operation and drain voltage V_{DS} = 33 V and gate voltage V_{GS} = -2.2 V for 1800 MHz. The results versus input power for 900 MHz are shown in Fig. 5.33. Amplifier features a peak PAE of 69.5% and drain efficiency of 72.5% at an input power level of 25.5 dBm. The measured output power and gain versus input power are compared to simulation in Fig. 5.33b showing a measured gain of 13.8 dB and output power of 39.1 dBm (8.1 W) at 900 MHz for an input power of 25.5 dBm.

The measurement of the amplifier at 1800 MHz was performed with the corresponding configuration given in Table 5.6. The first measurement was performed with the same DC voltage of 29.5 V as in 900 MHz. It gives a maximum PAE of 50.1% at an input power

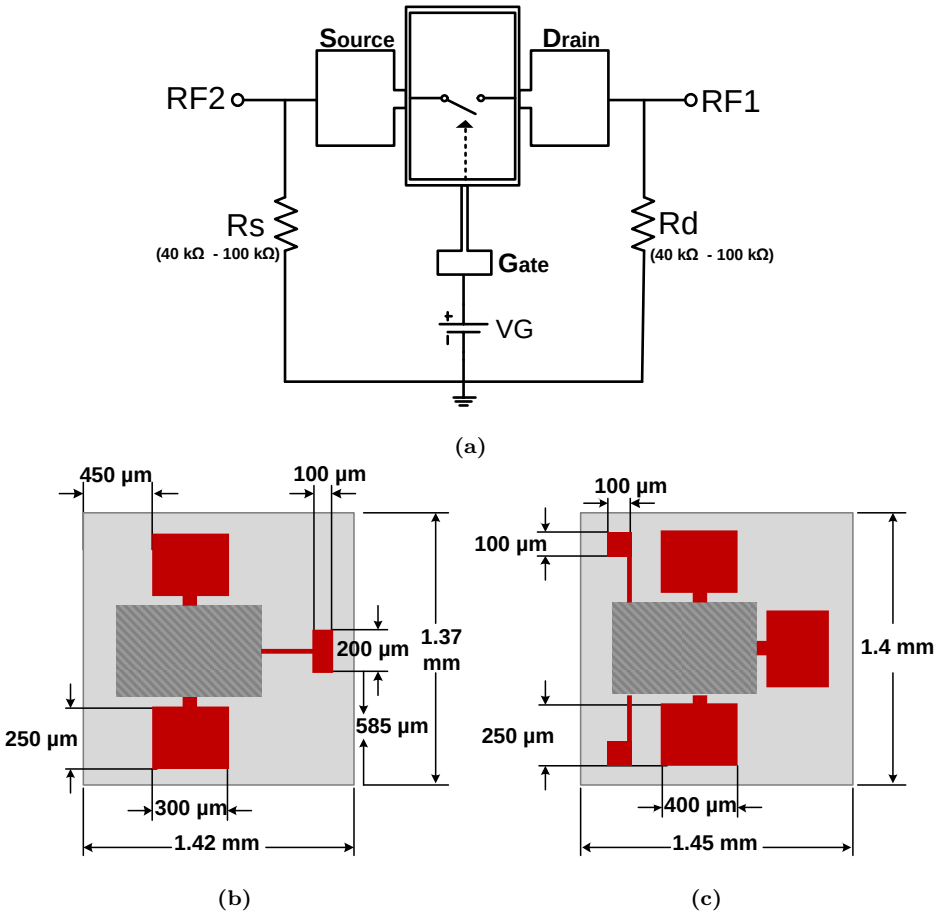
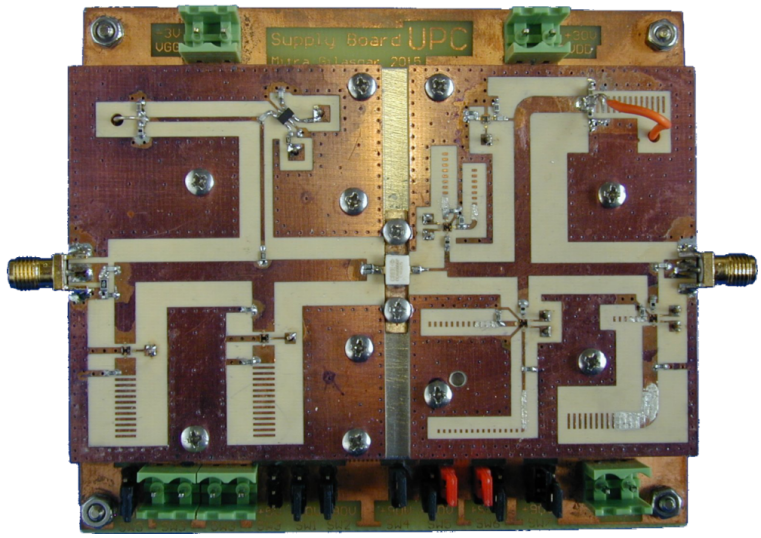
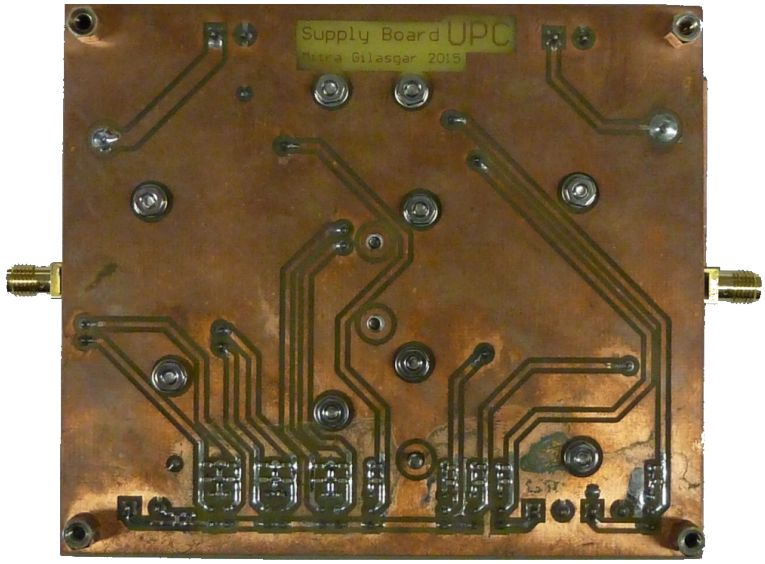


Figure 5.31: (a) The general application diagram of MEMS switches, (b) the footprint of MEMS SPST switch, and (c) the footprint of MEMS SPDT switch.

of 26 dBm. At this input power, the efficiency of the PA is 55.7% and Gain is 10.6 dB while delivering 36.6 dBm power. However, the optimum performance of the PA at 1800 MHz is achieved with a drain voltage of 33 V and a gate voltage of -2.2 V. The measured results at this biasing point are depicted in Fig. 5.34. The PA delivers an output power of 38.5 dBm (7 W) at an input power of 28 dBm where it achieves a maximum PAE of 57.9% and an efficiency of 63.5%. The measurement results compared to the simulation results of the PA are given in Table 5.9.



(a)



(b)

Figure 5.32: (a) Fabricated dual-frequency reconfigurable class-F PA at 900 MHz and 1800 MHz using 3 SPST and 3 SPDT MEMS switches and 1 SPST Hittite switch, and (b) the backside PCB for voltage distribution of the switches.

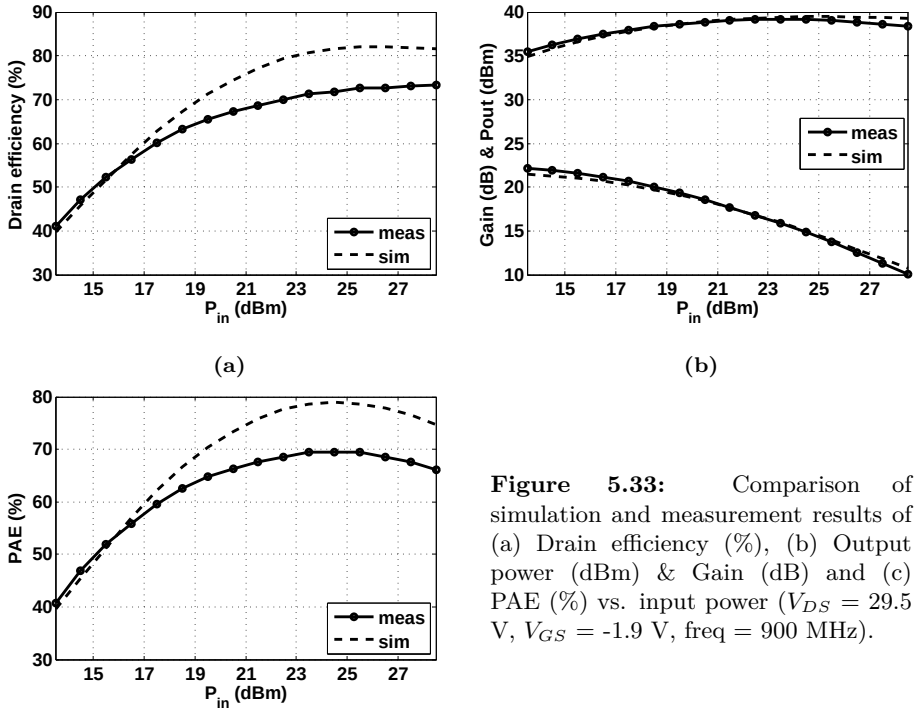


Figure 5.33: Comparison of simulation and measurement results of (a) Drain efficiency (%), (b) Output power (dBm) & Gain (dB) and (c) PAE (%) vs. input power (V_{DS} = 29.5 V, V_{GS} = -1.9 V, freq = 900 MHz).

Table 5.9: Measured and simulated values for the PA at the maximum PAE.

Freq (MHz)		P_{in} (dBm)	PAE_{max} (%)	η (%)	P_{out} (dBm)	V_D (V)	V_G (V)
900	Sim	24	79	81.6	39.5	29.5	-1.9
	Meas	25.5	69.5	72.5	39.1	29.5	-1.9
1800	Sim	29	68.3	74	40	33	-2.2
	Meas	28	57.9	63.5	38.5	33	-2.2

5.4 Frequency Reconfigurable PA using MEMS Switches - Design B

This design has a slightly different OMN to increase the design freedom and consequently the performance of the PA. The proposed reconfigurable class-F PA working at two frequency bands, f_1 = 900 MHz and f_2 = 1800 MHz is presented in Fig. 5.35.

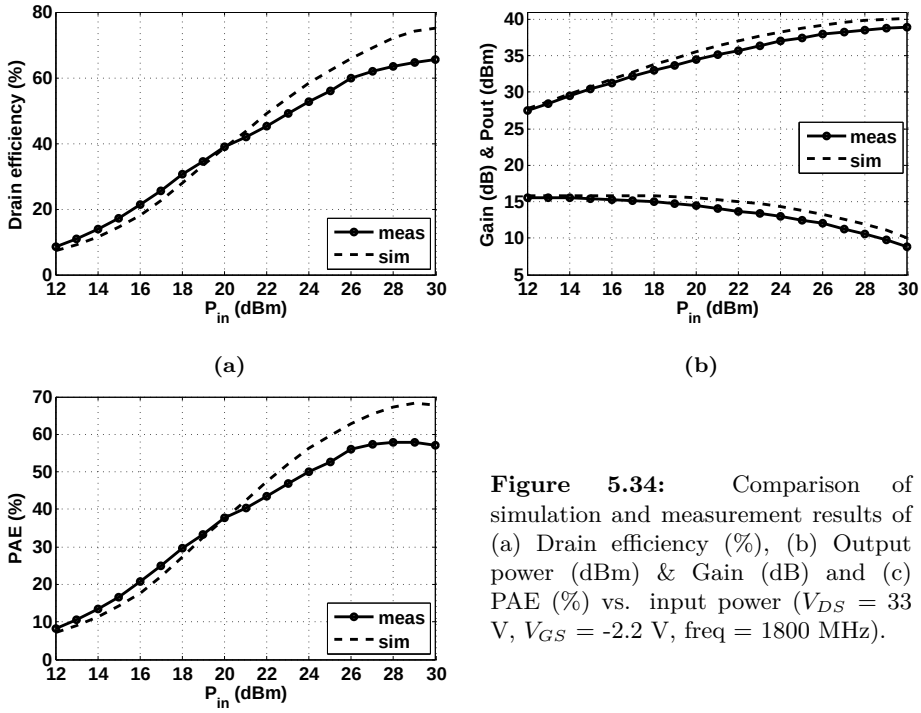


Figure 5.34: Comparison of simulation and measurement results of (a) Drain efficiency (%), (b) Output power (dBm) & Gain (dB) and (c) PAE (%) vs. input power (V_{DS} = 33 V, V_{GS} = -2.2 V, freq = 1800 MHz).

5.4.1 Input and Output Matching Network Design

The IMN has the same structure as in design A, with the only difference that all 3 SPST switches (SW1, SW2, and SW3) are RMSW100HP Radant MEMS. The output matching network is designed using only SPDT switches of RMSW200HP from Radant MEMS (SW4, SW5, SW6, and SW7). In this design unlike design A, drain voltage is applied through an RF choke and the SW4 is not an SPST but an SPDT switch. With an SPDT switch, the length of this stub at each frequency is independent of the other frequency. This increases the design freedom and hence performance since this is a very sensitive stub for the PAE of the amplifier. There are two capacitors placed before each switch in the OMN, a 100 pF capacitor in order to remove the dc component of voltage and an RF capacitor in order to achieve the required electrical length without the need for a very long transmission line. The combination of the switches for each frequency is stated in Table 5.10. For the switch state at each frequency of operation, refer to the Table 5.7. The design procedure is the same as explained for design A.

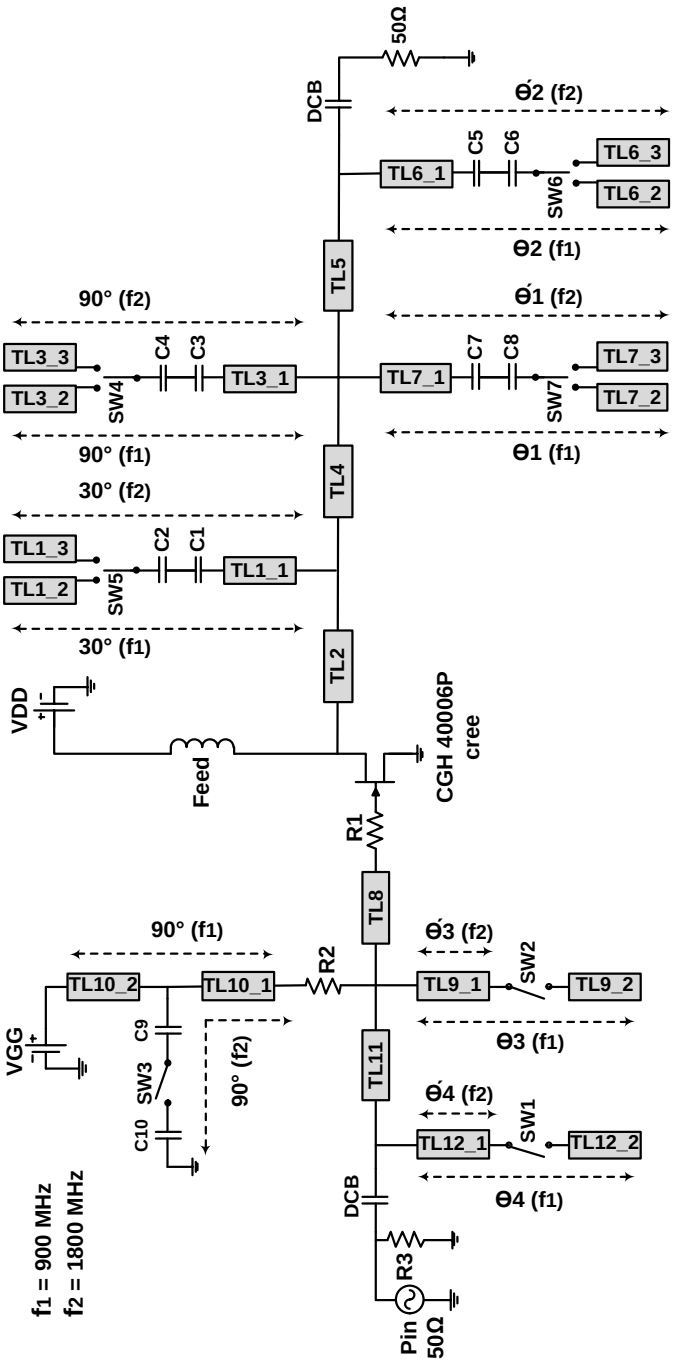


Figure 5.35: The proposed frequency reconfigurable class-F PA using MEMS SPST and SPDT switches (Design B).

Table 5.10: Switch configuration of the amplifier in Fig. 5.21 at each operating frequency.

freq (MHz)	SW1	SW2	SW3	SW4	SW5	SW6	SW7
900	ON	ON	OFF	RF_1-ON	RF_1-ON	RF_1-ON	RF_1-ON
1800	OFF	OFF	ON	RF_2-ON	RF_2-ON	RF_2-ON	RF_2-ON

5.4.2 Simulation Results

The power amplifier in Fig. 5.35 is designed to work at 900 MHz and 1800 MHz with switch configuration given in Table 5.10. It is biased with $V_{GS} = -2.5V$ and $V_{DD} = 28V$ and is driven into saturation region with input power of 25 dBm at 900 MHz and 28 dBm at 1800 MHz.

5.4.2.1 PA Reliability

To make sure the switch works under reliable conditions in this design, the voltage over the switches in ON and OFF state have been simulated. The simulation results are illustrated in Fig. 5.36 for input power from 10 dBm to 30 dBm. With the maximum of $P_{in} = 30$ dBm, the maximum voltage appears over SW4 switch reaching to 30 V. These simulations show that the switch works under reliable conditions. The voltages over the capacitors are presented in Fig. 5.37. The voltage over these capacitors go over 50 V, bringing a requirement on the capacitor maximum operating voltage. The capacitors in this design are working with 100 V maximum voltage rating.

5.4.2.2 PA Performance

Fig. 5.38 illustrates the simulation results versus input power and versus frequency for both 900 MHz and 1800 MHz. A peak PAE of 75.5% is obtained at an input power of 25 dBm. At this input power level, the PA demonstrates a drain efficiency of 78.5% and a gain of 14.2 dB while delivering an output power of 39.2 dBm. At 1800 MHz a peak PAE of 66.8% is obtained at an input power of 28 dBm, a drain efficiency of 74.5% and a gain of 9.8 dB while delivering an output power of 37.8 dBm.

The performance versus RF frequency is illustrated in Fig. 5.38c for 900 MHz and Fig. 5.38d. It shows that the PA is designed for the best performance at the operating frequency. At 900 MHz operating condition, the amplifier achieves a PAE higher than 60% in a bandwidth of 245 MHz, from 835 MHz to 1080 MHz, reaching to 76% at 900 MHz, providing an output power in the range from 38.8 dBm at 835 MHz to 38.2 dBm at 1080 MHz at this frequency band. At 1800 MHz operating condition, the amplifier achieves a PAE higher than 60% in a bandwidth of 120 MHz, from 1745 MHz to 1865

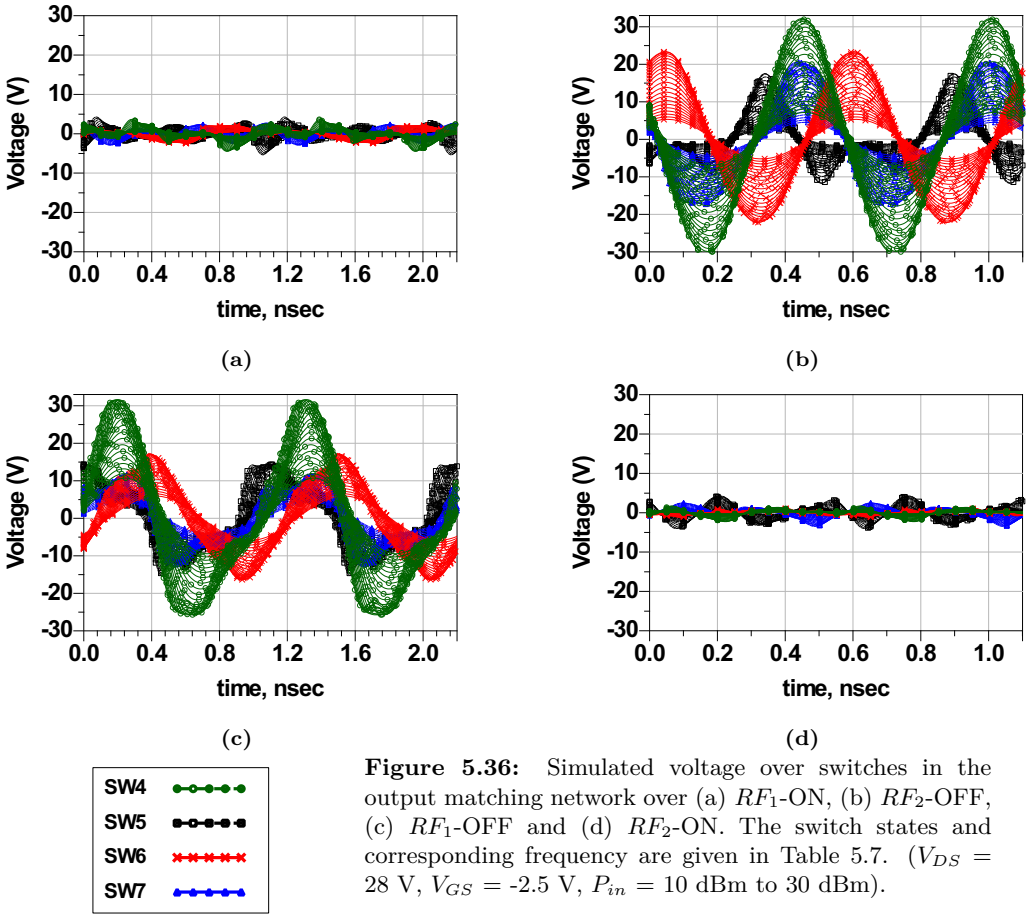


Figure 5.36: Simulated voltage over switches in the output matching network over (a) RF_1-ON, (b) RF_2-OFF, (c) RF_1-OFF and (d) RF_2-ON. The switch states and corresponding frequency are given in Table 5.7. (V_{DS} = 28 V, V_{GS} = -2.5 V, P_{in} = 10 dBm to 30 dBm).

MHz, reaching to 66.8% at 1800 MHz. The output power at this frequency band goes from 38 dBm at 1745 MHz to 37 dBm at 1865 MHz.

The comparison of fundamental and harmonic components in drain voltage (V_d) and load voltage (V_{load}) of the amplifier illustrated in Fig. 5.39a at 900 MHz condition and in Fig. 5.39b at 1800 MHz condition shows how harmonics are removed from V_d by the output filter of the amplifier. The output power Spectrum of the simulated class-F PA is shown in Fig. 5.40 and the corresponding harmonic rejection values are presented in Table 5.11.

5.4.3 Fabrication

The designed PA is fabricated on a 1.5 mm Rogers RO4003 substrate and is shown in Fig. 5.41. The dimension of the fabricated board is 71.6 mm x 112 mm. The PA uses a

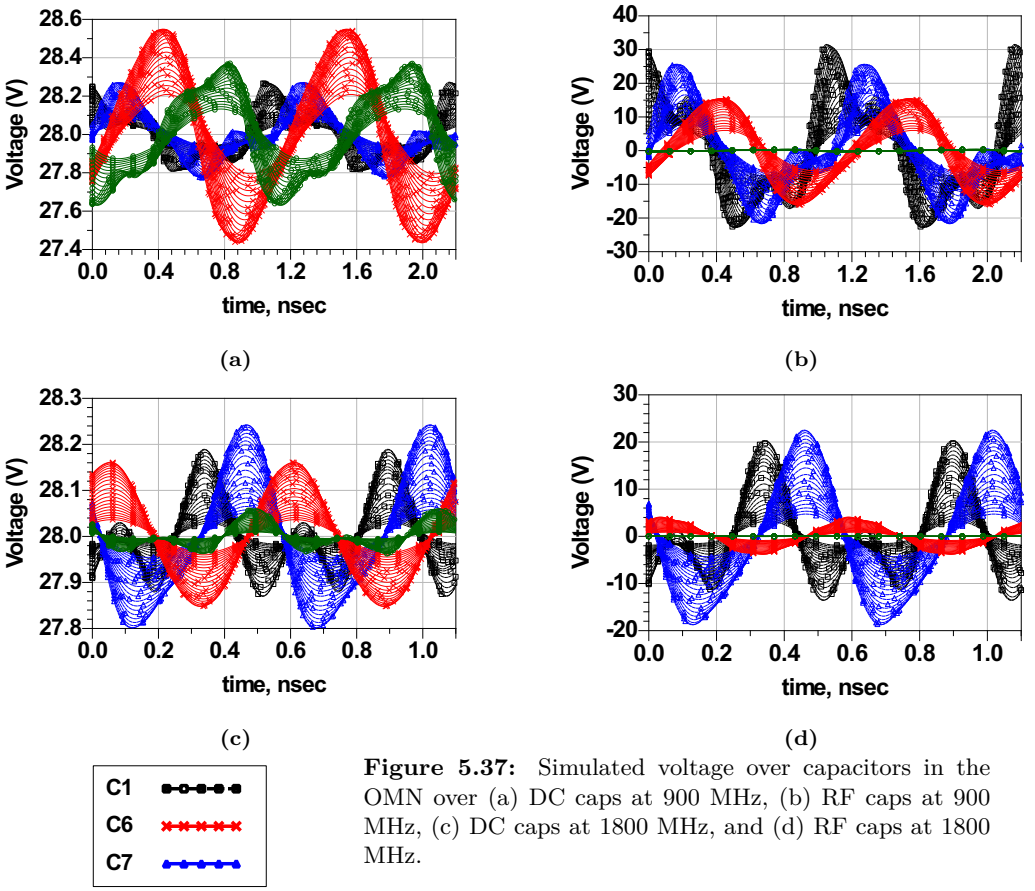


Figure 5.37: Simulated voltage over capacitors in the OMN over (a) DC caps at 900 MHz, (b) RF caps at 900 MHz, (c) DC caps at 1800 MHz, and (d) RF caps at 1800 MHz.

Table 5.11: Simulation results for harmonic rejection up to fifth order.

		Harmonic rejection			
Freq	P_{in}	2^{nd}	3^{rd}	4^{th}	5^{th}
MHz	dBm	dBc			
900	25	-27.4	-29	-38.5	-55.4
1800	28	-35.2	-49.6	-50.1	-55.7

backside PCB for voltage distribution of the switches and its layout is provided in Fig. 5.41b. This PCB is designed using Altium Designer software.

5.4.4 Measurement Results

The fabricated amplifier in Fig. 5.41 is measured using the setups depicted in Fig. 4.14. The optimized performance is achieved for gate voltage V_{GS} = -2.5 V and drain voltage

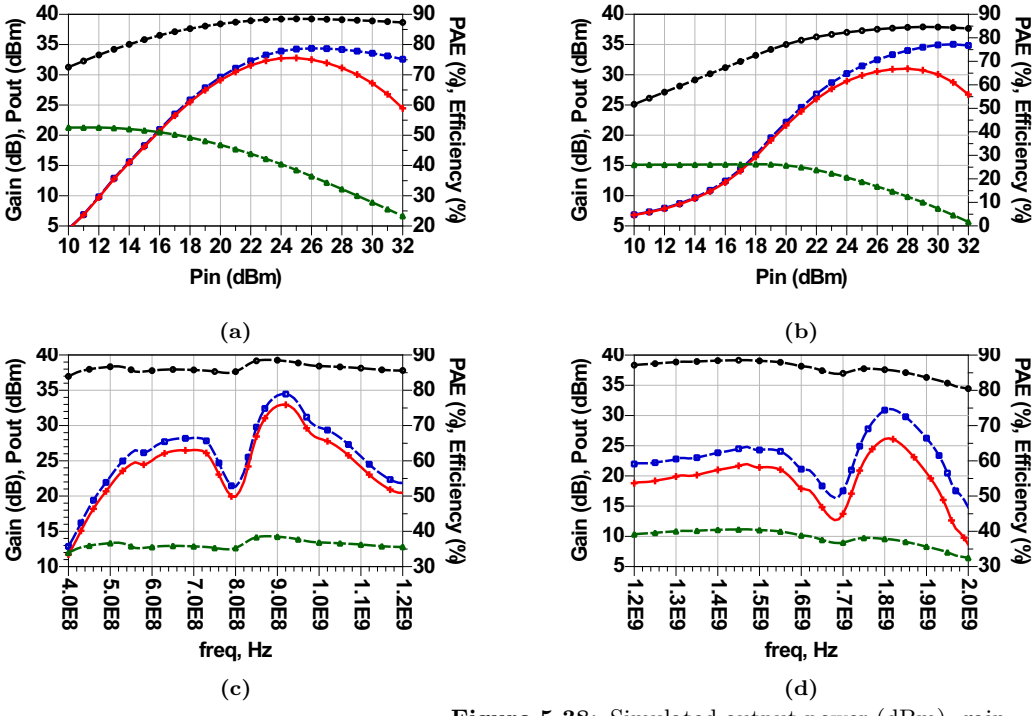


Figure 5.38: Simulated output power (dBm), gain (dB), drain efficiency (%) and PAE (%) (a) vs. input power at 900 MHz, (b) vs. input power at 1800 MHz, (c) vs. frequency at 900 MHz condition and (d) vs. frequency at 1800 MHz (V_{DS} = 28 V, V_{GS} = -2.5 V).

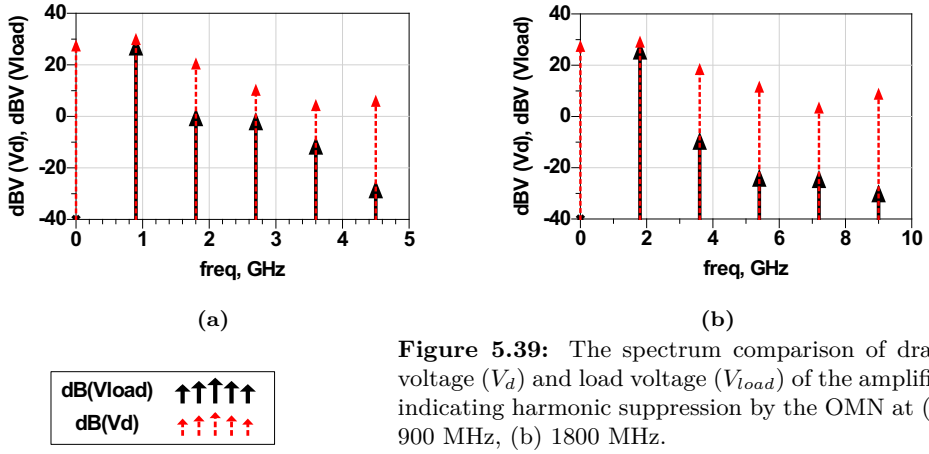
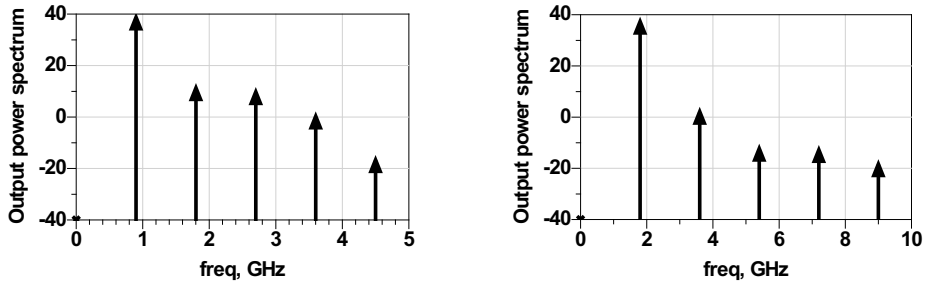


Figure 5.39: The spectrum comparison of drain voltage (V_d) and load voltage (V_{load}) of the amplifier indicating harmonic suppression by the OMN at (a) 900 MHz, (b) 1800 MHz.



(a) **(b)**

Figure 5.40: Output power spectrum at (a) 900 MHz, (b) 1800 MHz.

Table 5.12: Measured and simulated values for the PA at the maximum PAE.

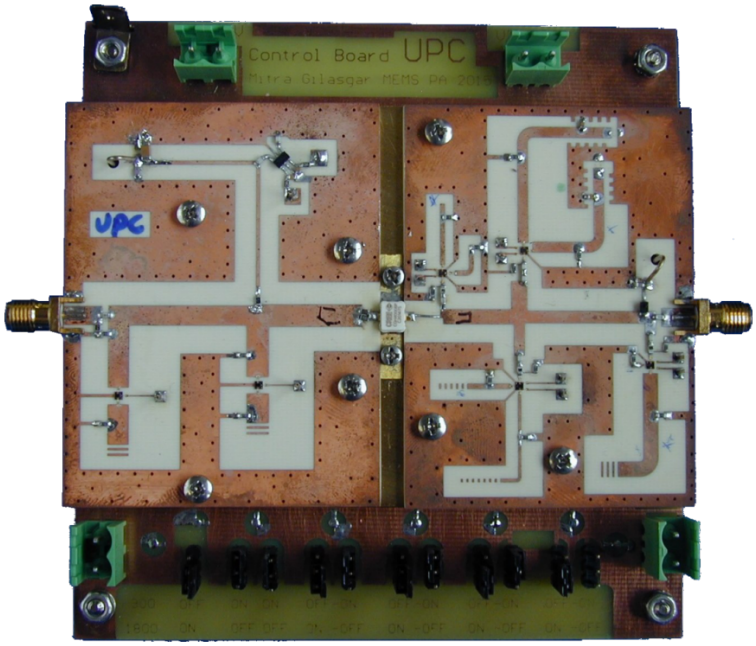
Freq (MHz)		P_{in} (dBm)	PAE_{max} (%)	η (%)	P_{out} (dBm)	V_D (V)	V_G (V)
900	Sim	25	75.2	78.1	39.2	28	-2.5
	Meas	25.5	70.2	74	38.4	28	-2.5
1800	Sim	29	66.2	74.3	38.8	32.5	-2.5
	Meas	28	44.6	55.9	35	32.5	-2.5

$V_{DS} = 28$ V at 900 MHz operation and drain voltage $V_{DS} = 32.5$ V at 1800 MHz operation. The results versus input power for 900 MHz are shown in Fig. 5.42. The amplifier features a peak PAE of 70.2% and a drain efficiency of 74% at an input power level of 25.5 dBm. The measured output power and gain versus input power are compared to simulation in Fig. 5.42b showing a gain of 12.9 dB and an output power of 38.4 dBm (6.9 W) is measured at 900 MHz for an input power level of 25.5 dBm. If the drain supply DC voltage is raised to 30 V, the PA achieves a max PAE of 68% at 25.5 dBm input power and at this input power level, it provides 38.8 dBm (7.6 W) output power.

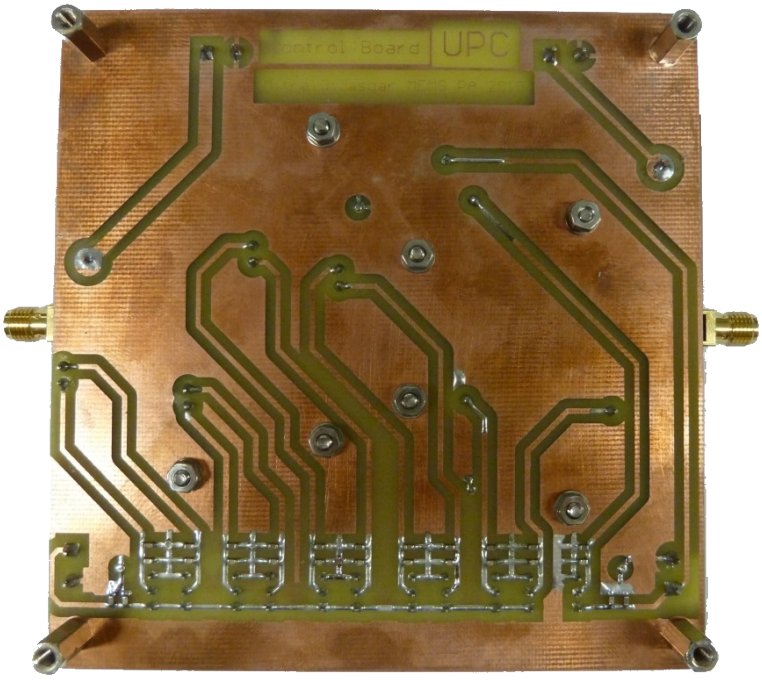
The measurement of the amplifier at 1800 MHz was performed with the corresponding configuration given in Table 5.10. The optimum performance of the PA at 1800 MHz is achieved with a drain voltage of 32.5 V and a gate voltage of -2.5 V and the measured results are illustrated in Fig. 5.43. The PA delivers an output power of 34.5 dBm at an input power of 24 dBm where it achieves a maximum PAE of 51% and an efficiency of 56%. The measurement compared to the simulation results of the PA is given in Table 5.12.

5.4.5 Summary

The comparison of the three designs are illustrated in Table. 5.13. Hittite switch was incapable of handling high power over the switch and the design of Hittite PA did not



(a)



(b)

Figure 5.41: (a) Fabricated dual-frequency reconfigurable class-F PA at 900 MHz and 1800 MHz using SPST and SPDT MEMS switches, and (b) the backside PCB for voltage distribution of the switches.

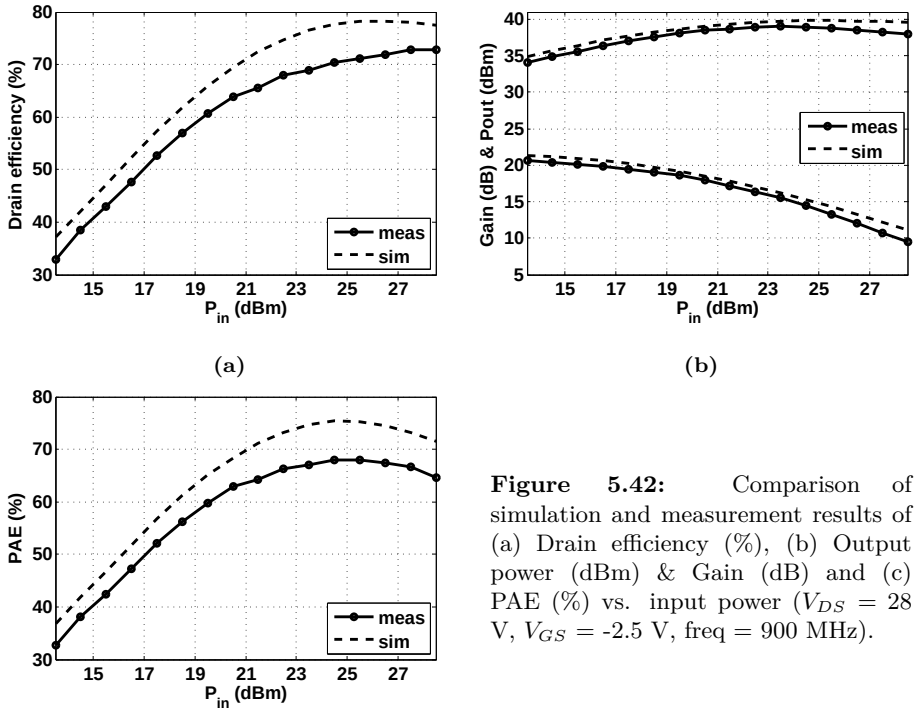
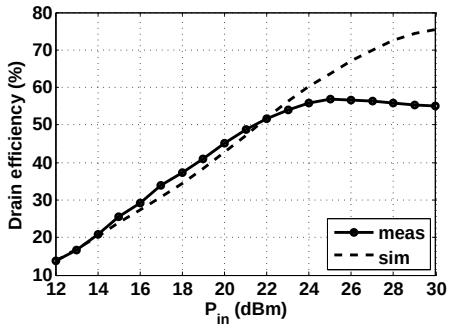
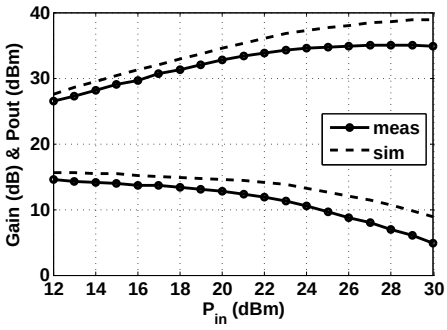


Figure 5.42: Comparison of simulation and measurement results of (a) Drain efficiency (%), (b) Output power (dBm) & Gain (dB) and (c) PAE (%) vs. input power (V_{DS} = 28 V, V_{GS} = -2.5 V, freq = 900 MHz).

perform successfully at 1800 MHz. On the other hand, designs with MEMS switches showed better performance and higher power capability. It can be observed that although Design B achieves higher performance at 900 MHz compared to other fabricated circuits, Design A achieves the highest performance in both bands. The fabricated result of Design A reaches a good performance in both bands using the proposed structure in this chapter. By choosing the right point to place the switches in the stub, the maximum voltage over the switches are minimized and hence the reliability of the PA is improved. It should be noted that in some occasions MEMS switches burned not because of the design but because of their reliability issues. Since it is a mechanical device, it can break and stay in open or closed position which will influence the performance of the design.



(a)



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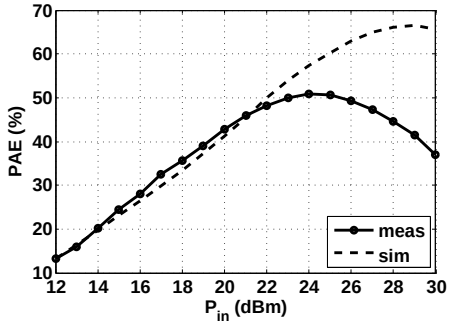


(c)

Figure 5.43: Comparison of simulation and measurement results of (a) Drain efficiency (%), (b) Output power (dBm) & Gain (dB) and (c) PAE (%) vs. input power (V_{DS} = 32.5 V, V_{GS} = -2.5 V, freq = 1800 MHz).

Table 5.13: Measured and simulated values for the PA at the maximum PAE.

Freq (MHz)	Design	P_{in} (dBm)	PAE_{max} (%)	η (%)	P_{out} (dBm)	V_D (V)
900	Hittite	23.3	62.1	64.9	37	25
	Design A (MEMS)	25.5	69.5	72.5	39.1	29.5
	Design B (MEMS)	25.5	70.2	74	38.4	28
1800	Hittite	24	23	27.5	31.8	25
	Design A (MEMS)	28	57.9	63.5	38.5	33
	Design B (MEMS)	28	44.6	55.9	35	32.5

6

Chapter 6

Power Reconfigurable class-F PA Integrated in CMOS Technology

In this chapter a novel reconfigurable class-F PA is proposed which can adapt to different impedance values presented to its load. The proposed amplifier is intended for handsets and WiFi application. The PA is designed at 2.4 GHz and implemented in CMOS technology. The proposed structure controls up to 3^{rd} harmonic and with a proper harmonic tuning network the need for an extra filtering section is eliminated. The design incorporates MOS varactors as the tuning device and the effect of the load variation is compensated by reconfiguring the output network using two independent variable capacitors. Simulation and measurement results are presented and compared.

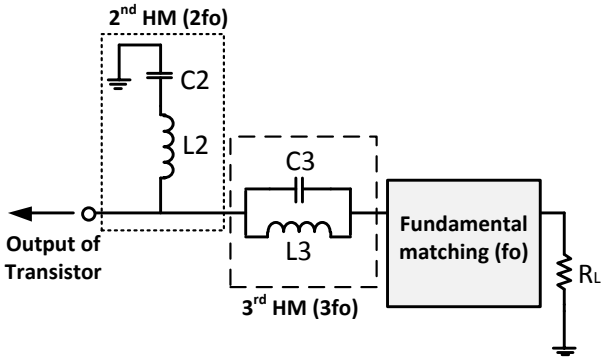


Figure 6.1: Basic output matching network for harmonic termination required in the class-F PA using lumped-elements.

6.1 Simple Output Matching Network for a Class-F PA using Lumped-Elements

Complementary metal oxide semiconductor (CMOS) technology offers high integration level and low cost. To enable low cost integration of all mobile circuitry in a single unit, use of CMOS technology is inevitable. With the intention of high efficiency power amplifier (PA) design for handsets and WiFi application and integration using CMOS technology, transmission line matching networks (MN) are not practical due to their large size at this frequency. Therefore lumped element MNs are used in order to reduce the die area and cost. For a lumped-element class-F PA, harmonic tuning is limited mostly to 2^{nd} and 3^{rd} harmonics. The proposed matching network to achieve class-F operation using lumped-elements is presented in Fig. 6.1. At 3^{rd} harmonic the resonator L_3C_3 provides an open circuit and at 2^{nd} harmonic frequency the resonator L_2C_2 provides a short circuit at the output of the transistor.

6.2 Study of Different PA Configuration and Voltage Capability

There are several important design consideration that should be taken into account for the design of an integrated PA in CMOS technology. The output power is a critical parameter in power amplifiers, and it puts a lot of limitation on the integrated PAs. The high peak voltage at the output of a class-F PA brings breakdown concerns for transistors. One way to minimize the risk of breakdown is to reduce the supply voltage (V_{DD}), but this leads to a lower output power.

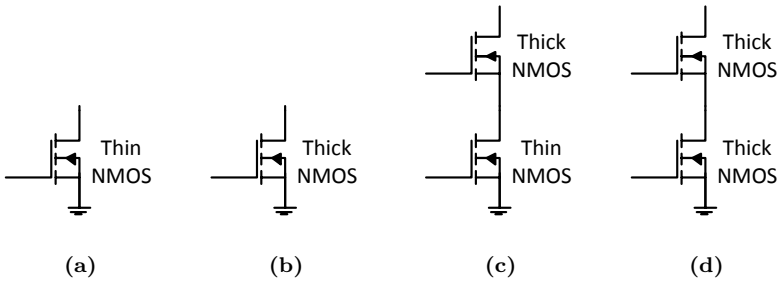


Figure 6.2: The four configurations considered for the core of the PA shown in Fig 6.3: (a) single thin-oxide transistor (SN), (b) single thick-oxide transistor (ST), (c) cascode thin-thick-oxide transistors (CNT), and (d) cascode thick-thick-oxide transistors (CTT).

Stacking transistors is another way to reduce the voltage over each transistor. In this way, the supply voltage gets divided over the total number of stacked transistors. The third option is taking device physics into account. There are two types of transistors in the CMOS technology used for this work, a thin-oxide transistor and a dual-oxide thick transistor. Dual-oxide thick transistors can handle twice the supply voltage (3.3 V) compared to the thin-oxide transistor (1.8 V). This puts a limitation on the design of the PA and more attention is needed during the design procedure, for the reason that sometimes in simulation, a high output power can be achieved but in practice, the transistor would burn at that power level or even much lower than that. Therefore in order to choose a proper configuration, a comprehensive study was carried out considering single transistor and cascode transistors structures incorporating the aforementioned types of transistors (thin-oxide and thick-oxide). The following four configurations shown in Fig. 6.2 were studied as a core of the PA:

1. Single thin-oxide transistor (SN)
2. Single thick-oxide transistor (ST)
3. Cascode thin-thick-oxide transistors (CNT)
4. Cascode thick-thick-oxide transistors (CTT)

The proposed topology for the comparison of these configurations is provided in Fig. 6.3. The output matching network (OMN) and input matching network (IMN) were designed using ideal lumped elements. A low pass LC network is chosen for the fundamental matching network of Fig. 6.1 and for the IMN. The parameters that were taken into account during the design procedure are maximum voltage over transistor(s), stability, and proper bias for maximum PAE and maximum power.

Design process of each configuration is a constant trade-off between power and PAE of the PA, while taking into account for maximum voltage over transistor(s), stability, and

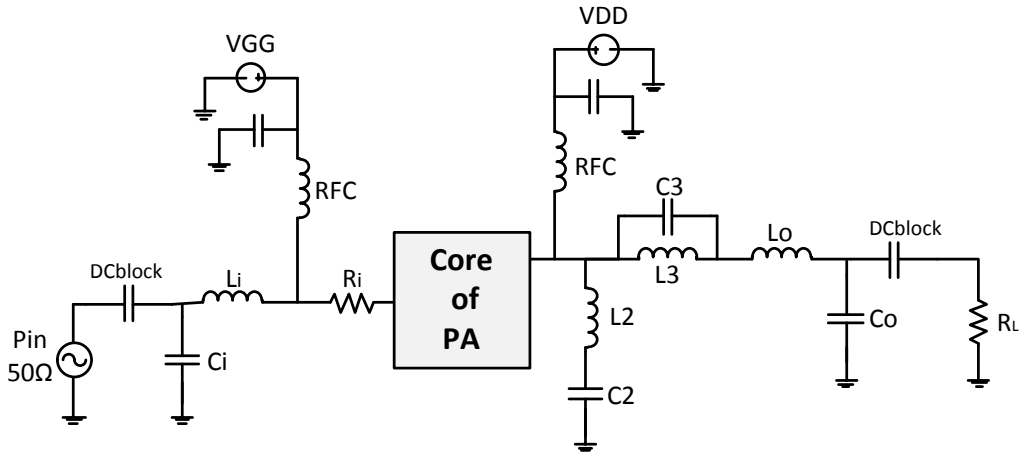


Figure 6.3: The proposed topology for the comparison of the configurations illustrated in Fig. 6.2.

Table 6.1: The summary of PAE (%) and delivered power (dBm) for each of the configurations presented in Fig. 6.2. The bold values correspond to the regions of input power that device can work under reliable condition. (V_{dd} = 3.3 V)

	$P_{in}=-5$		$P_{in}=0$		$P_{in}=3$		$P_{in}=5$		$P_{in}=7$		$P_{in}=10$	
PA core	P_o dBm	PAE %	P_o dBm	PAE %	P_o dBm	PAE %	P_o dBm	PAE %	P_o dBm	PAE %	P_o dBm	PAE %
SN	**9.7**	**8.3**	**14.3**	**24.5**	16	35.4	16.7	39.7	17.2	41.6	17.8	42.5
ST	**8.6**	**2.7**	**13.3**	**8**	**16.1**	**15**	**17.8**	**22**	19.1	29	20	33
CNT	**10.6**	**4.3**	**15.3**	**12**	17.5	21.4	18.5	27.4	19.1	32	19.6	32
CTT	**11**	**4.8**	**15.2**	**12.6**	**17.3**	**20.3**	**18.7**	**27.1**	**19.8**	**34**	20.8	39

proper bias of common source transistor at each step of design. For each design P_{imax} is obtained as the maximum input power that does not lead the voltage over transistor(s) to go beyond the maximum reliable operating voltages. This P_{imax} is the parameter that defines the achievable maximum output power P_{omax} of device. The summary of the PAE and delivered powers for some input powers -5 dBm, 0 dBm, 3 dBm, 5 dBm, 7 dBm and 10 dBm are shown in Table 6.1 for each of the configurations. The bold values correspond to the regions of input power that device can work under reliable condition. It was observed that the SN configuration gives the highest PAE in simulation but its V_{DS} is higher than safety range. It also delivers lower power compared to the other configurations. For each design, P_{imax}, $P_o|_{P_{imax}}$, $PAE|_{P_{imax}}$, linear gain (G) and P_{1dB} (1 dB compression point) is calculated and the results are shown in Table 6.2.

Due to their physics nature, breakdown issues are more severe in configurations which incorporates thin-oxide transistor (SN and CNT). The other two configurations

Table 6.2: Simulation result comparison for each of the configurations presented in Fig. 6.2.

PA core	P_{imax} dBm	$P_o\|_{P_{imax}}$ dBm	$PAE\|_{P_{imax}}$ %	linear gain (G) dB	$G\|_{P_{1dB}}$ dB	$G\|_{P_o=15}$ dB
SN	2	15.6	32	14.7	13.6	14
ST	5	18	22.5	13.6	12	13.2
CNT	2	16.9	18.3	15.6	14.9	15.3
CTT	8	20.2	36.6	16	12.2	15.2

Table 6.3: Figure of merit (FOM) of different configuration PA design.

	FOM
Single-thin-oxide-transistor (SN)	0.5
Single-thick-oxide-transistor (ST)	7.4
Cascode-thin-thick-oxide-transistors (CNT)	1.3
Cascode-thick-thick-oxide-transistors (CTT)	**21.4**

incorporating thick-oxide transistors, ST and CTT, both are capable of reaching to a higher output power without surpassing the maximum voltage over drain-source (V_{DS}) allowed by the foundry. A figure of merit (FOM) from equation 6.1 is calculated for each configuration and the results are provided in Table 6.3. Due to this study and obtained results, it is clear that the best configuration for the purpose of PA is the CTT. Hence a cascode structure using two thick-oxide transistors is chosen as the core of this design. Further advantages of the cascode structure are good isolation between input and output, increased stability, higher gain and voltage stress reduction on the CMOS transistor.

$$FOM = {P_o}^3|_{P_{imax}} \cdot PAE^2 \cdot G_p \cdot P_{1dB} \tag{6.1}$$

P_o is the output power obtained when the maximum input power (P_{imax}) allowed by the technology is applied. Above P_{imax}, the high voltage breaks down the power amplifier. PAE represents the power added efficiency, G_p represents the power gain and P_{1dB} represents the 1 dB compression point.

6.3 Proposed Reconfigurable Class-F Power Amplifier

The proposed OMN of Fig. 6.1 is developed for proper class-F PA implementation by taking into account the intrinsic drain capacitance (C_d) of the active device (NMOS transistor) in the design process. Matching block at fundamental frequency (f_0) will be

explained later in this section. The series LC resonator built by L_2 and C_2 resonates at $2f_0$, providing a short circuit at second harmonic. The third harmonic peaking is done by resonator L_3C_3, providing an open circuit to the drain at $3f_0$. At frequencies well below its respective resonant frequency, resonator L_2C_2 behaves as a capacitor, and resonator L_3C_3 behaves as an inductor, giving a low pass filter that will have a small influence on the matching network behavior. Since the optimum load impedances at harmonics are not short or open circuits because of the nonlinear behavior of the active device and its parasitics, the harmonics filter is modified to the developed topology shown in Fig. 6.4, by adding a parallel inductance L_d and a series capacitor C_s.

A further advantage of adding series capacitor C_s to the drain is that it removes the

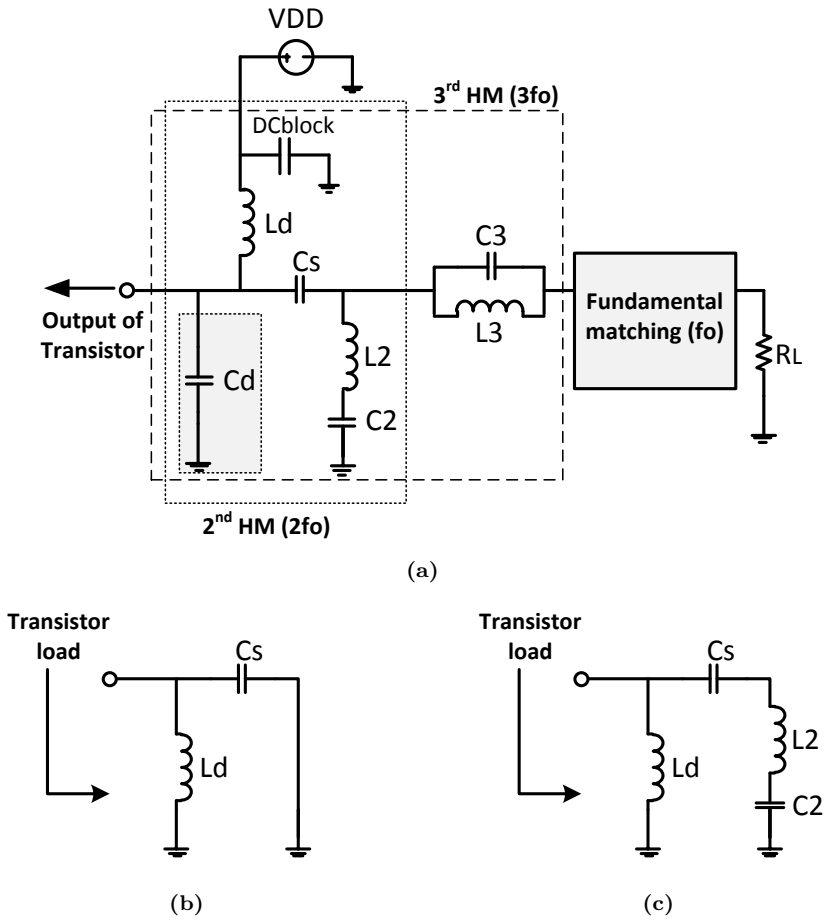


Figure 6.4: (a) The Proposed output matching network for harmonic termination required in the class-F PA using lumped elements (C_d is transistor drain capacitance), (b) equivalent at second harmonic, and (c) equivalent at third harmonic.

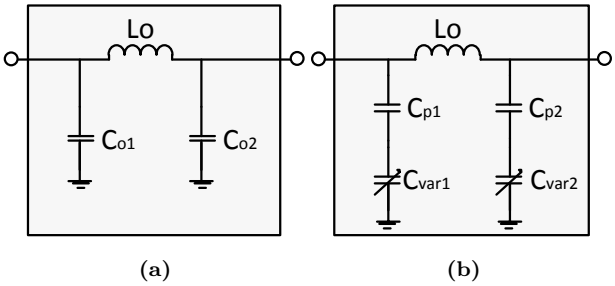


Figure 6.5: Fundamental matching network: (a) Fixed, (b) Reconfigurable.

DC component from the output network which results in a reduction of the peak voltage over the parallel components, reducing from 6.6 V to 3.3 V which is an acceptable value according to design rules. Otherwise the peak voltage at the drain of a class-F PA which can reach up to $2V_{DD}$ (more than 6 V here) is too high exceeding the maximum acceptable value according to design rules and will damage the parallel capacitors and inductors in the OMN. By adding the inductance L_d between the drain and the voltage supply, in addition to being an element of OMN, it will provide DC current path for the transistor. L_d in parallel with C_d resonates at second harmonic providing an open circuit at $2f_0$.

From the equivalent circuit at $2f_0$, shown in Fig. 6.4b, it can be observed that the filter for the 2^{nd} harmonic is uncoupled from the matching network, thus adjusting the variable capacitors will not have any effect on the 2^{nd} harmonic load. The equivalent circuit at $3f_0$ is presented in Fig. 6.4c, which is also uncoupled from the matching network section.

The fundamental matching network can be a low-pass LC or a the pi-shaped matching network for single frequency operation. For this design, the structure shown in Fig. 6.5a is chosen, a CLC pi-shaped network to convert the 50Ω load impedance to the required load in the drain of the transistor. However, there is an increasing demand for the PAs to adapt to different conditions that arise in wireless applications. Load impedance variation happens when a user holds the mobile phone and the strong interaction between head, hand, and antenna causes a change in antenna impedance leading to a reduced performance. An impedance tuner concept can be used in this network to convert a range of impedance values in the output to a known impedance value in the drain.

This impedance tuner is implemented as shown in Fig. 6.5b. While C_{o_1} and C_{o_2} are fixed capacitances, C_{var_1} and C_{var_2} are MOS varactors (MOScaps) that use the gate capacitance of a MOS transistor and their capacitance value can be controlled by applying a voltage to the gate of it (V_{ctl_1}, V_{ctl_2}). Fixed capacitors, C_{P_1} and C_{P_2} must be connected in series before the variable capacitors in order to block the gate DC voltage, thus preventing it from going to the output of the PA. Another advantage of using two

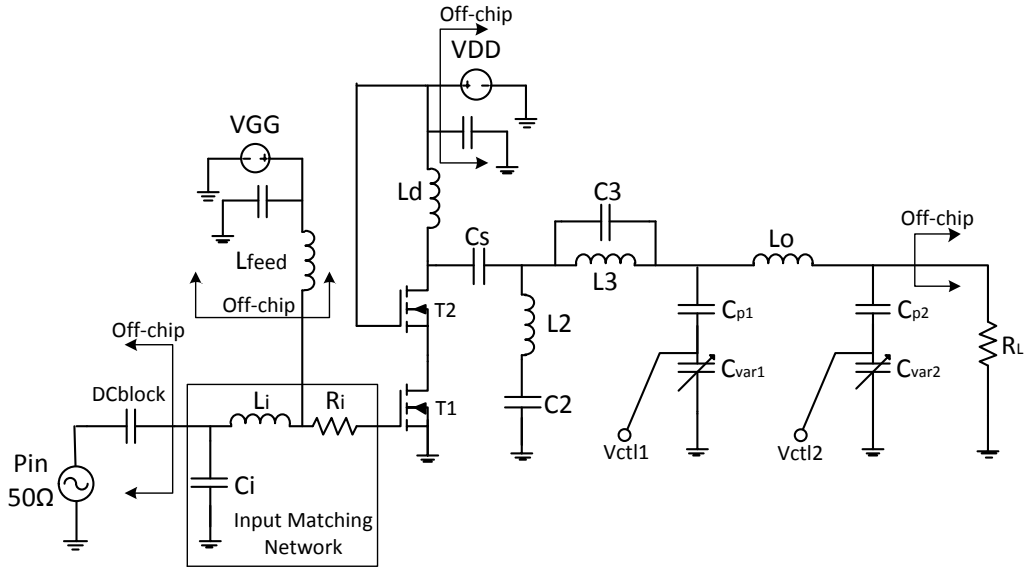


Figure 6.6: Proposed reconfigurable class-F PA.

capacitors in series is that the peak voltage at the output divides (approximately) by two, hence minimizing the risk of breakdown.

The full schematic of the proposed integrated reconfigurable class-F power amplifier is presented in Fig. 6.6. Input matching network is a low pass configuration composed of a series inductor L_i and a parallel capacitor C_i to match the power device to a 50Ω input impedance. In theory, assuming that any values of C_{P_1}, C_{var_1}, C_{P_2}, C_{var_2}, and L_o are possible, any arbitrary load impedance can be transformed into the optimal transistor load impedance at fundamental (Z_{L1}) with such a circuit topology. However, in practice there is a limitation on the range of values exhibited by these components on the chip.

Special attention is paid to the sizing and I-V characteristic of the active device with a trade-off between the current handling and parasitic capacitances. The small-signal model of a MOS transistor, the physics and RF performance of MOS devices are discussed in details in [117]. The active device in this design is a 3.3 V thick oxide 0.18μm NMOS transistor available in TSMC^{TM} 0.18μm 1P6M CMOS technology with ultra thick top metal (UTM) layer. The equivalent small-signal model of a CMOS transistor is shown in Fig. 6.7 where R_g is the effective gate resistance, and C_{gs}, C_{dg} and C_{ds} are the effective gate-to-source, gate-to-drain and drain-to-source nonlinear capacitances of the transistor. Parameters g_{ds} and g_m represent the output conductance of the transistor and the device transconductance, respectively.

As will be described in section 7.4, the width of the transistors was chosen big

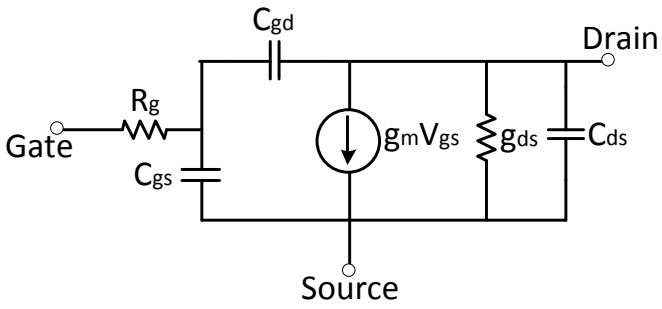
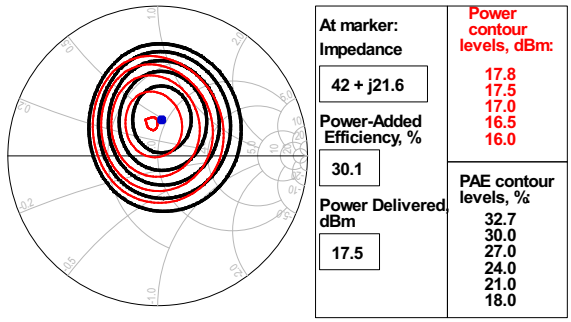


Figure 6.7: Equivalent model of MOS active device.

enough (64 × 8 μm) to handle the required power but not too big to produce an excess of parasitic capacitances. The applied voltages were carefully chosen in order to avoid junction breakdown across the drain-substrate reverse biased junction and the oxide breakdown across the drain-gate overlap area, which are critical issues in CMOS devices.

6.4 Load-pull Analysis

The load impedance values at the output of transistor at fundamental and harmonic frequencies which give highest PAE or highest output power or a trade-off between them can be derived from a load-pull analysis using the nonlinear model of the transistor. The active device in this design is a 3.3 V thick oxide 0.18μm NMOS transistor available in TSMC^{TM} CMOS technology. The output power and PAE contours at fundamental frequency and its harmonics are shown in Fig. 6.8 and the corresponding load impedance values retrieved from this analysis are given in Table 6.4. The results of load-pull analysis of the active device at fundamental frequency (2.4 GHz) are shown in Fig. 6.8a. It shows that a maximum PAE of 30.1% can be achieved for a load impedance of $Z_{L1} = 42 + j21.6$ Ω, which has been selected for the PA design. The same procedure is done for second harmonic and third harmonic and the results are shown in Fig. 6.8b and Fig. 6.8c respectively. To reduce distortion (harmonic content at the amplifier output), harmonic loads near to those of an ideal class-F operation (open circuit for odd harmonics and short circuit for even harmonics) were chosen, even though (from Fig. 6.8b) the 2nd harmonic load does not show optimal value for PAE and output power. With the above criteria, the selected load impedance values at second and third harmonics are $Z_{L2} = 2.5 - j3.7$ Ω and $Z_{L3} = 11.3 + j53$ Ω respectively. The above simulations take into account the loss of the matching networks.



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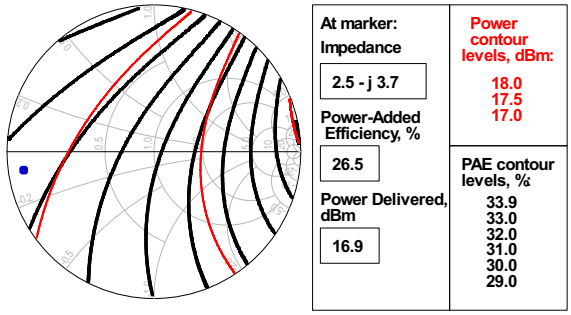

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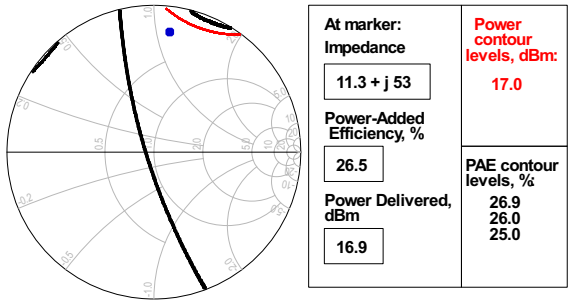


(c)

Figure 6.8: Constant PAE (thin) and output power (thick) contours obtained from load-pull analysis at (a) fundamental frequency (2.4 GHz), (b) 2^{nd} harmonic (4.8 GHz) and (c) 3^{rd} harmonic (7.2 GHz).

Table 6.4: Load Impedance values for fundamental, second and third harmonic obtained from load-pull analysis.

	Load-Pull Impedance (Ω)
Z_{L1} *(at 2.4 GHz)*	42 + j30.5
Z_{L2} *(at 4.8 GHz)*	0 - j22.6
Z_{L3} *(at 7.2 GHz)*	0 - j135

6.5 Design in CMOS Technology

The final proposed power amplifier is illustrated in Fig. 6.6. A cascode structure is chosen for the core of the PA, as the result of the previous study explained in section 6.2. In the input matching network, C_i is a MOS capacitor of 610 fF and L_i is a spiral inductor of 4.6 nH with Q of 11. Although using a cascode structure improves the stability, adding a resistor R_i to the gate of T_1 makes the design stable at the expense of reducing the PAE. However due to the losses that the matching components and layout parasitics introduced to the final circuit implementation this resistor was eliminated.

In the output matching network, C_s is a MIM capacitor of 9 pF and C_2 and C_3 are MOS capacitors of 700 fF and 1.2 pF respectively that are used without biasing. L_d, L_3 and L_o are spiral inductors of 2.3 nH, 850 pH, and 3 nH respectively. Both MOS variable capacitors of C_{var_1} and C_{var_2} have a gate width of 2.5 μm and length of 500 nm per finger. Capacitance range of 1.1 pF$-$2.4 pF has been obtained for C_{var_1} by using 6 groups of 50 fingers each. For C_{var_2} a capacitance range of 540 fF$-$1.1 pF is obtained by using 4 groups of 35 fingers each. Primarily, C_{P_1} and C_{P_2} were MIM capacitors of 10 pF and 6.1 pF respectively. However, achieving these values using MIM capacitors results to a large area in the chip, that is why in this design MOS variable capacitors with zero biasing gates are used instead. Proper simulations were done to get the same results for MOScaps with zero gate voltage give and fixed MIM capacitors.

6.6 Power Amplifier Implementation

The proposed class-F PA is designed in the aforementioned TSMC^{TM} 0.18 μm CMOS technology with 1 poly and six metal layers (M1 to M6) 1P6M with an ultra thick top metal layer. The cross section of CMOS technology from bottom to top consists of Substrate, Poly, M1, M2, M3, M4, M5, M6 and three passivation layers where poly and metal layers are covered in silicon dioxide. A picture of the fabricated chip is shown in Fig. 6.9.

Using UTM for metal 6 layer (M6) results in a higher output power, a higher

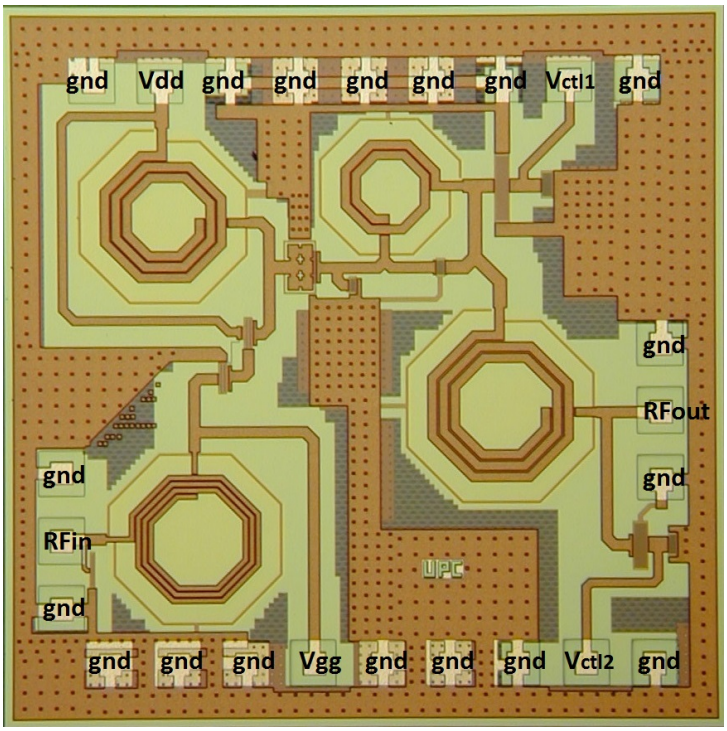


Figure 6.9: Fabricated circuit in TSMC^{TM} 0.18 μm 1P6M CMOS technology. Die size is 1.6 mm $\times$ 1.6 mm.

efficiency and twice the quality factor for inductors. Also this metal layer allows four times higher J_{max} (maximum DC current density allowed per μm of metal line width) in comparison to other metal layers at 110 °C. J_{max} is provided by process specifications to avoid electromigration and its rating factor goes higher as the temperature goes down and vice-versa. In this design, the minimum width of the signal path is calculated at 110 °C. The width of interconnecting metal lines is 25 μm which is wide enough to avoid electromigration. By placing many vias in parallel in the interconnections, their parasitic resistance is minimized and the maximum current capability is maximized.

The design of RF passive components (inductors and capacitors) in CMOS technology is challenging in PA design because high-Q lumped elements are difficult to achieve. The losses of these components affect the output power and efficiency of the PA. On-chip inductors suffer from ohmic losses (due to metal resistance), capacitive losses (due to electric coupling from the metal line to the substrate) and inductive losses (due to eddy currents generated by magnetic fields going through the substrate). Inductive losses come from skin effect and proximity effect in inductors. To reduce these losses, a one layer inductor using UTM is preferred in order to increase the dielectric layer thickness

between metal and substrate. In this design octagonal structure is chosen for inductors and a Q between 10 and 12 is achieved for each inductor. Guard rings are used in the design to suppress cross-talking. Except the feeding inductor L_{feed}, which is an off-chip RF choke, the rest of the inductors are integrated on chip. The MIM capacitors are without shield structure and their capacitance is 2 fF per μm^2. Cross-talk and antenna effect are avoided by proper layout design.

Transistors T1 and T2 connected in cascode in Fig. 6.6 have the same width of 64 $\times$ 8 μm. The final chip has 24 pads, of which 3 are used for input RF signal (input pads) and 3 are used for output RF signal (output pads). The RF input and output pads are contacted using ground-signal-ground (GSG) RF probes. The DC-bias voltages are delivered to the transistor drains and gates and to the MOS varactor gates through two rows of 9 pads on the top and at the bottom of the chip. This pad arrangement is compatible with the multi-contact probes used for DC-bias. The pads are stacks of metal layers with a size of 50 μm $\times$ 50 μm to increase robustness and to decrease resistance.

6.7 Simulation Results

The PA of Fig. 6.6 is deigned and simulated using Keysight ADS and Cadence Spectre RF softwares. The drain voltage and current waveform of the PA simulated for different input powers are shown in Fig. 6.10. It can be observed that for input drives bigger than 2 dBm the proper class-F voltage and current waveforms is achieved.

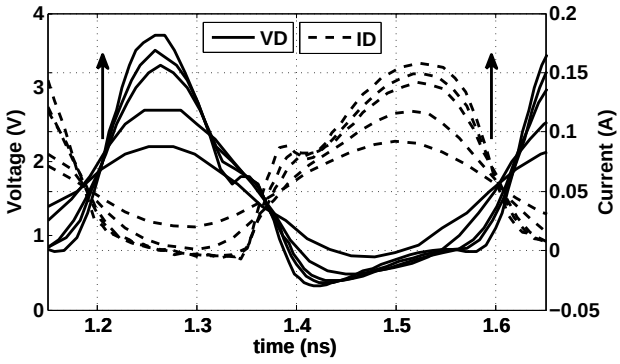


Figure 6.10: Simulated drain voltage (V_{DS}) and current waveforms (I_D) of T2 in the proposed class-F PA for different input powers (-5 dBm, 0 dBm, 5 dBm, 7 dBm, 10 dBm).

Simulations are performed under three assumptions: (i) ideal (lossless) elements in matching networks; (ii) lossy inductors but ideal capacitors; (iii) lossy inductors and lossy capacitors (including MOS varactors). The results for output power (P_{out}) and PAE versus input power (P_{in}) are presented respectively in Fig. 6.11 and Fig. 6.12 for

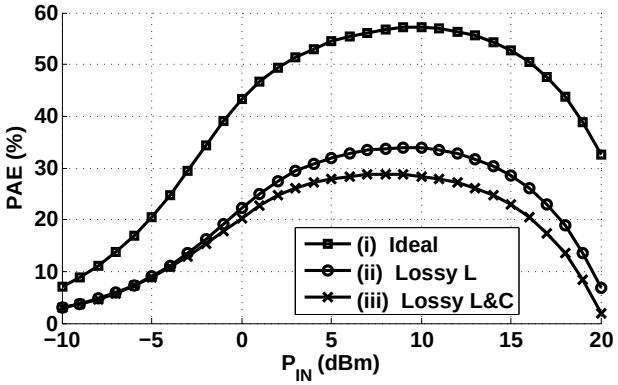


Figure 6.11: Simulated PAE versus input power for three different cases of loss in network with $V_{DD} = 3$ V.

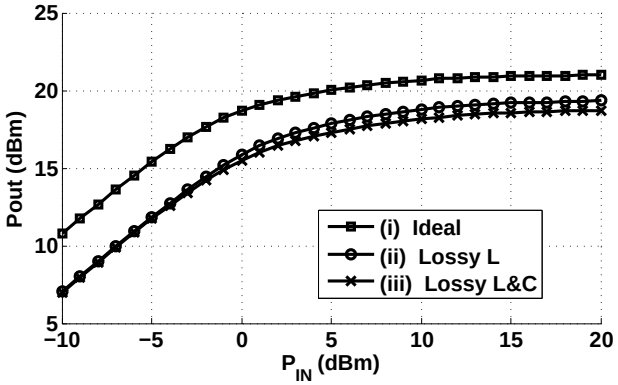


Figure 6.12: Simulated output power versus input power for three cases of loss in network applied to the circuit with $V_{DD} = 3$ V.

$V_{DD} = 3$ V and respectively in Fig. 6.13 and Fig. 6.14 for $V_{DD} = 4$ V. In case (iii) the complex models provided by foundry are used for the inductors and capacitors which take into account loss and couplings.

From Fig 6.13 and Fig. 6.14 it can be observed that the inductor loss is the main limitation for Pout and PAE, whereas loss associated to capacitors has a smaller contribution. A maximum output power $P_{out} = 21.1$ dBm is obtained for a bias point $V_{DD} = 3$ V in the ideal case (i), but this figure is reduced to 19.4 dBm and 18.7 dBm when the losses are taken into account in cases (ii) and (iii) respectively. These results agree with the predictions from the load-pull analysis in Fig. 6.8a. For the same bias point, an optimal PAE of 57% is obtained in the ideal case (i) but reduces to 34% and 28.9% in cases (ii) and (iii) respectively. In later case, the 1 dB compression point is obtained to be $P_{out_{1dB}}$ equal to 14.5 dBm, and the power gain (G_P) and P_{in} for optimal

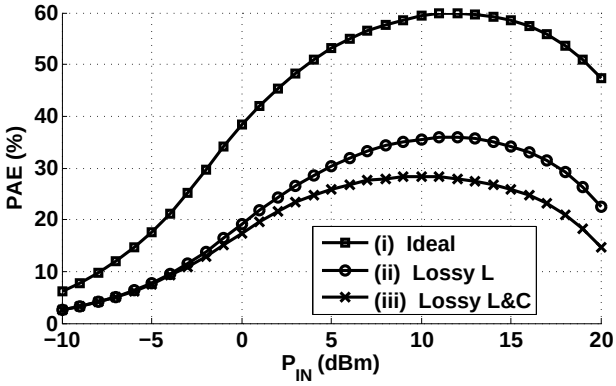


Figure 6.13: Simulated PAE versus input power for three cases of loss in network applied to the circuit with $V_{DD} = 4$ V.

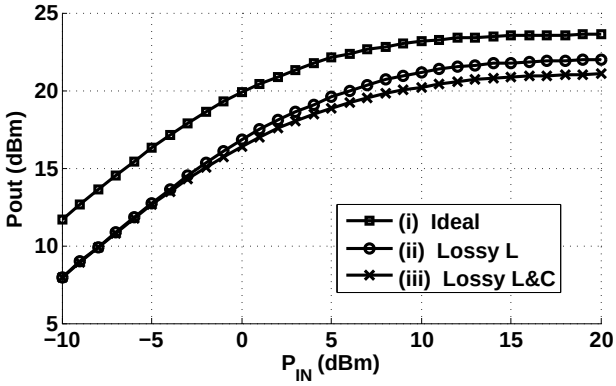
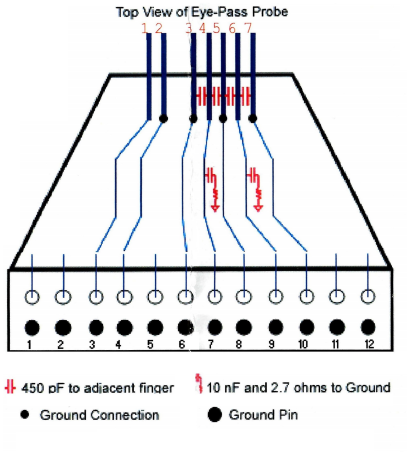


Figure 6.14: Simulated output power versus input power for three cases of loss in network applied to the circuit with $V_{DD} = 4$ V.

PAE are G_P equal to 10.2 dB and P_{in} equal to 8 dBm respectively. For $V_{DD} = 4$ V, the maximum Pout for cases (i), (ii), and (iii) are 23.7 dBm, 22 dBm, and 21.1 dBm respectively, and the optimal PAE are 60%, 35.8%, and 28.2% accordingly. In case (iii), $P_{out_{1dB}} = 15$ dBm, and for optimal PAE, $G_P = 10$ dB, $P_{in} = 10$ dBm. As a conclusion, P_{out} is increased 2.4 dB using $V_{DD} = 4$ V, but PAE does not improve compared to $V_{DD} = 3$ V in a realistic simulation including losses (case (iii)).

6.8 Measurement setup

To measure the fabricated chip of Fig. 6.9, 4 probes were used, one 9-pin probe and three 3-pin probes. At the input, 3-pin GSG probe is used for providing an input signal to the circuit as well as gate bias. For transistor and MOS varactor1 (Var_1), biasing



Config Code: LGXG'P'G'P'G			
Pin #	**Contact**	**Type**	**Code**
1		No Contact	
2		No Contact	
3	1	Logic/Signal	L
4	2	Ground	G
5		No Contact	X
6	3	Ground	G
7	4	Eye-Pass Power	P
8	5	Ground	G
9	6	Eye-Pass Power	P
10	7	Ground	G
11		No Contact	
12		No Contact	

Figure 6.15: Probe configuration used for biasing the Drain and Var1.

is performed using a 9-pin Eye-Pass-Probe^{TM} from Cascade-Microtech with a specific configuration shown in Fig. 6.15. In this probe, there is 450 pF capacitor implemented between V_{DD} and GND pins and 10 nF plus 2.7Ω from V_{DD} to ground. This provides the perfect ground in the Pin of V_{DD} and hence L_d of Fig. 6.6. The probe structure for Var_1 and Var_2 are different since an OC is required at these pins at RF frequency. Therefore it is required that Var_1 and Var_2 pins be biased with a bias Tee.

Since the 9-pin probe is used for Var_1, there is no capacitor connected from the Var_1 pin of 9-pin probe to ground and this OC should be provided in a different way. A specific printed circuit board (PCB) in the Fig. 6.16 was designed for delivering the DC supply to the wafer. The flat tape of 24-pins was used for biasing the Drain and Var_1 pin. Using a vector network analyzer (VNA), a perfect OC at Var_1 pin is obtained by moving the inductor choke along the slot lines of PCB. For Var_2 pin, this OC was achieved by moving a tuning line termination at the OC side of the bias Tee. The complete measurement setup is presented in Fig. 6.17.

6.9 Measurement Results

S-parameter measurements are performed using a vector network analyzer (VNA) Agilent N5245A. For power and nonlinear measurements, spectrum and adjacent channel leakage ratio (ACLR), a vector signal generator Agilent E4438C and a spectrum analyzer Agilent E4448A are respectively used. The signal generator is connected to the input RF probe and the spectrum analyzer to the coupled port of a directional coupler. The basic measurement setup is shown in Fig. 6.17.

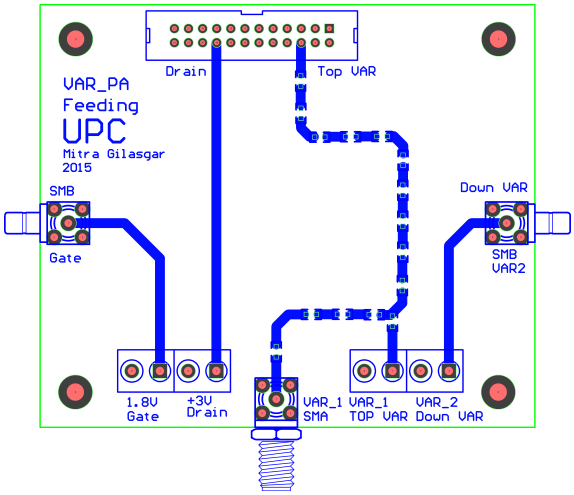


Figure 6.16: A specific PCB designed for delivering the DC supply to the wafer.

The gate of transistor T1 is biased at 1.5 V and the gate and drain of T2 are biased at 3 V. A safe voltage value of $V_{DD} = 3$ V and $V_{GG} = 1.3$ V is used as nominal bias point, though a higher bias voltage of $V_{DD} = 4$ V and $V_{GG} = 1.5$ V has also been tested since it showed improved output power during measurements. The measured DC drain current ranges are 44 mA to 63 mA and 63 mA to 96 mA, respectively, for input powers from -10 dBm to +15 dBm.

The measurements have been performed for two cases. In a first case, a nominal load impedance of 50Ω is considered and the measurement results are provided in section 6.9.1. Then in order to test the effect of antenna load variation on the PA performance, the measurements for loads other than 50Ω PA is measured and the results for tuned and non-tuned cases are provided in section 6.9.2.

6.9.1 50Ω Load

The measurements for a fixed load of 50Ω is performed using the measurement setup of Fig. 6.17 while having the MOS varactors fixed to their nominal values $C_{var1} = 1.6$ pF and $C_{var2} = 0.64$ pF. The large signal S-parameters of the fabricated circuit are measured and compared to simulation in Fig. 6.18, showing a good agreement. For an input power of 5 dBm, the measured gain is 11.5 dB and the simulated gain is 12.3 dB at 2.4 GHz.

The measured performance of the power amplifier regarding PAE and drain efficiency versus input power are compared with simulations in Fig. 6.19 and Fig. 6.20 respectively. At an input power of 9 dBm, a maximum PAE of 26% is obtained from measurement which is close to the value of 28.7% obtained from simulations. Drain efficiency at this power is

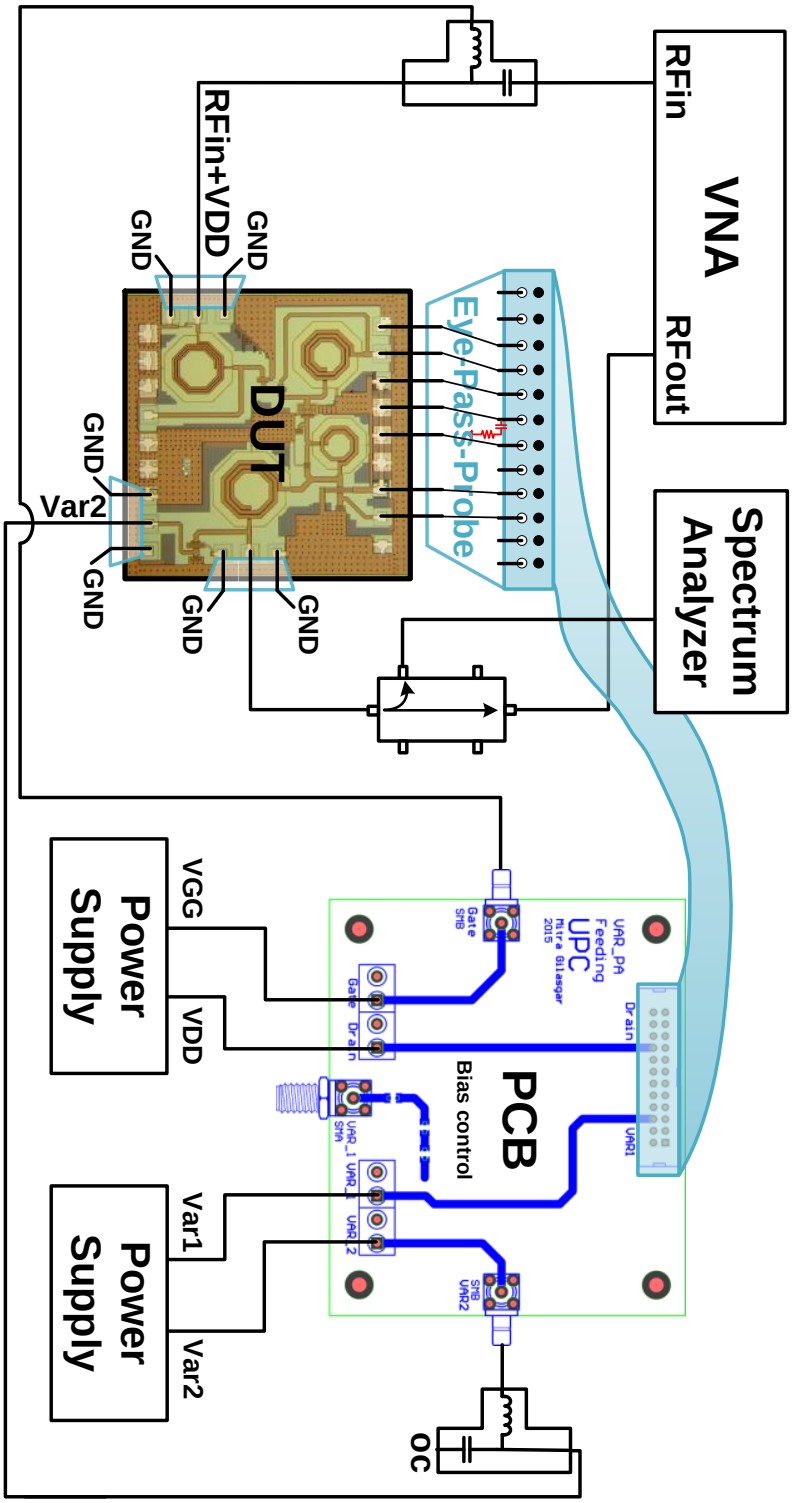


Figure 6.17: Measurements setup.

29.1%. However, it should be noted that while the simulated results were obtained for a drain voltage of 3 V, the measured results at 3 V were lower than simulations.

After measuring for different bias conditions, the best measurement results were achieved with a drain voltage of 4 V. The simulated and measured output power and power gain versus input power are provided in Fig. 6.21 and Fig. 6.22 respectively. For an optimal input power of 9 dBm (with maximum PAE), the output power is 18.7 dBm and the gain is 9.7 dB. A maximum measured output power of 19.2 dBm is obtained.

The PA performance regarding PAE and G_P versus output power are measured for the two biasing voltages of $V_{DD} = 3$ V and $V_{DD} = 4$ V, and compared to simulations in Fig. 6.23 and Fig. 6.24. For $V_{DD} = 3$ V, a maximum measured PAE of 22% for $P_{out} =$ 16.8 dBm with $G_P = 7.9$ dB is obtained. For $V_{DD} = 4$ V, the maximum measured PAE increases to 26.5% for P_{out} equal to 18.7 dBm with G_P of 9.7 dB, and a maximum output power of 19.2 dBm is obtained with a PAE of 20%. In both cases, the measured output

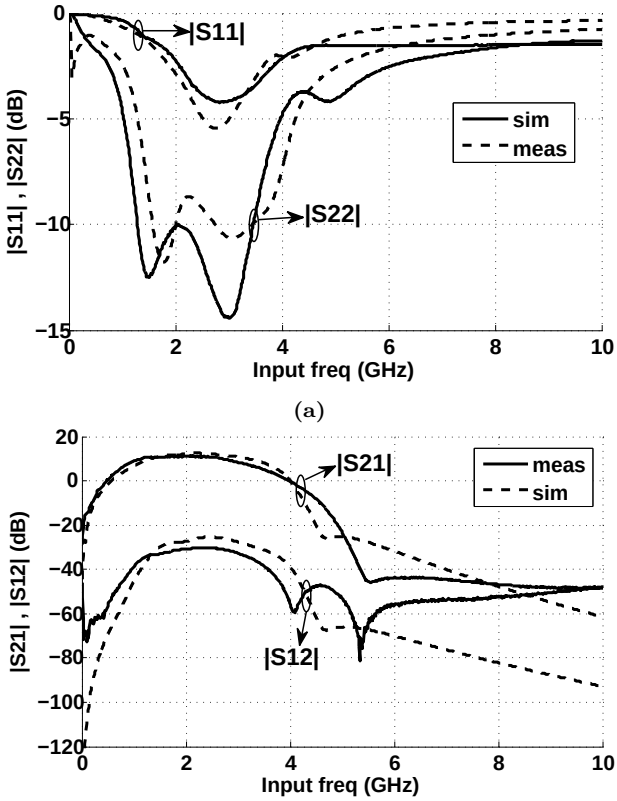


Figure 6.18: Simulated (dash) and measured (solid) Large Signal S-parameter results of the proposed class-F PA: (a) $|S_{11}|$ and $|S_{22}|$, (b) $|S_{21}|$ and $|S_{12}|$.

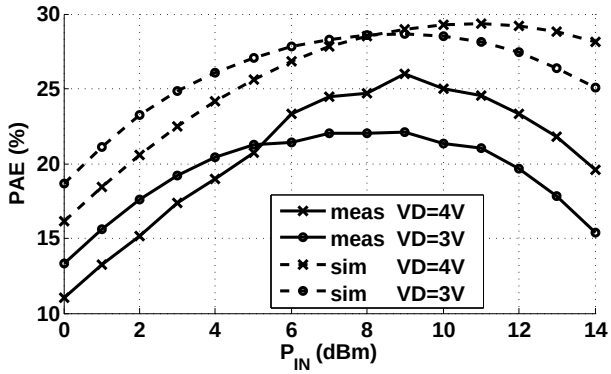


Figure 6.19: Simulated and measured PAE versus input power for 50Ω load impedance at 2.4 GHz for $V_{DD} = 3$ V and $V_{DD} = 4$ V.

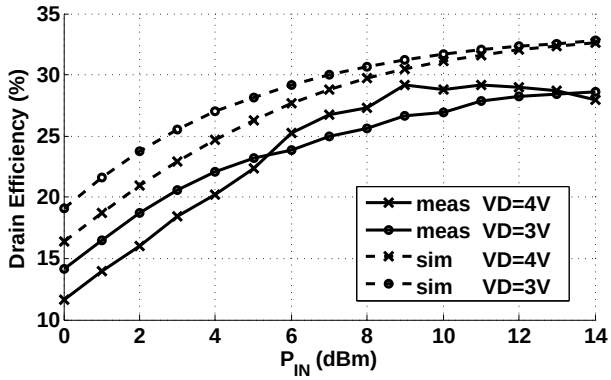


Figure 6.20: Simulated and measured drain efficiency versus input power for 50Ω load impedance at 2.4 GHz for $V_{DD} = 3$ V and $V_{DD} = 4$ V.

power is shifted down 2 dB with respect to the simulated output power, which in turn decreases the PAE. This difference is mainly attributed to the quality factor of fabricated inductors and capacitors (including MOS varactors) which may have been overestimated in simulation. If slightly smaller values ($Q_L = 8$ and $Q_C = 15$) are considered, then G_P decreases 1.5 dB. An additional 0.5 dB loss is attributed to a non-ideal decoupling produced by the multi-contact probe in the contact pins supplying control voltage to the MOS varactors.

The simulation and measurement results of the output power spectrum are shown in Fig. 6.25. The measured harmonic rejection for second ($2f_o$) and third ($3f_o$) harmonics are 28 dBc and 32.6 dBc respectively. The output spectrum shows a high harmonic suppression up to 5^{th} harmonic which shows that the proposed topology has the ability to reject harmonics without an extra filtering section. The measured total harmonic

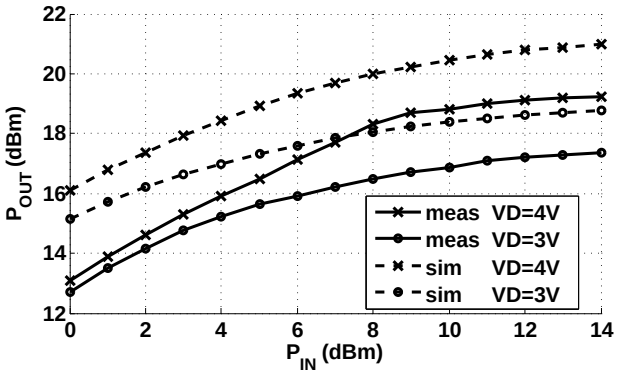


Figure 6.21: Simulated and measured PAE versus input power for 50Ω load impedance at 2.4 GHz for V_{DD} = 3 V and V_{DD} = 4 V.

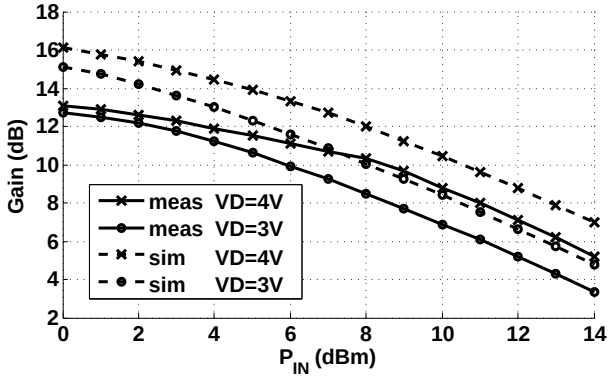


Figure 6.22: Simulated and measured drain efficiency versus input power for 50Ω load impedance at 2.4 GHz for V_{DD} = 3 V and V_{DD} = 4 V.

distortion is 4.9%.

To assess the PA nonlinear behavior under real operating conditions ACLR measurements have been performed using dedicated software (Keysight N7617B) to control the vector generator. A specific configuration is defined to deliver complex IEEE 802.11g WiFi signals (OFDM-64 QAM with maximum data rate of 54 Mbps) to the PA input. Fig. 6.26 shows the measured spectrum regrowth at the output of the amplifier for Pout = + 2 dBm and Pout = + 18.5 dBm. The later corresponds to the maximum PAE. The bias condition is V_{DD} = 4 V. It can be observed that the PA meets WiFi specifications (trace below the blue limit line) for $P_{out} \leq 18$ dBm. The measured ACLR values (in dBc) at 2.412 GHz (WiFi channel #1) for different output powers are presented in Table 6.5. As expected, ACLR degrades with increasing P_{out}, but even at highest P_{out} levels (with optimum PAE) ACLR is better than -26.6 dBc.

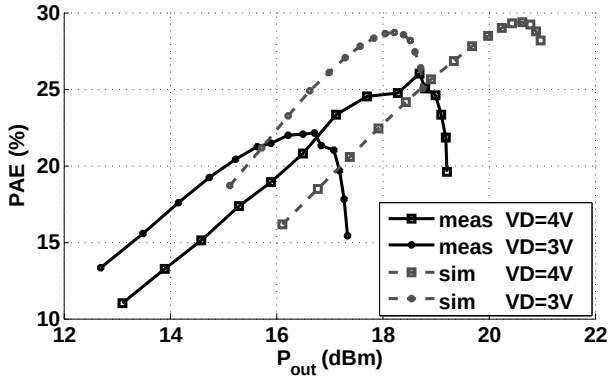


Figure 6.23: Simulation and measurement comparison of PAE (%) as a function of output power for bias voltages $V_{DD} = 3$ V and $V_{DD} = 4$ V.

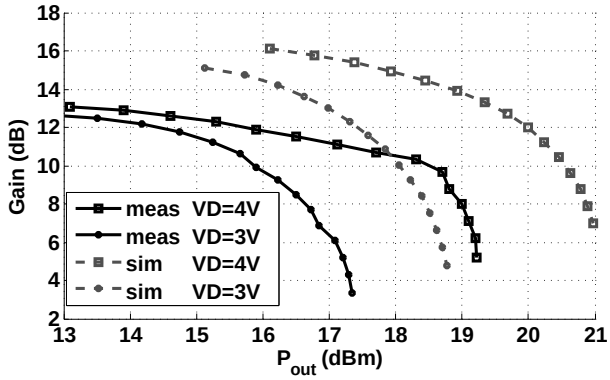


Figure 6.24: Simulation and measurement comparison of gain (dB) as a function of output power for bias voltages $V_{DD} = 3$ V and $V_{DD} = 4$ V.

Table 6.5: Measured ACLR (dBc) for different load impedance and output powers. (U: Upper WiFi channel, L: Lower WiFi channel)

	P_{out} (dBm)					
*L*oad impedance (Ω)	12		16		18 (highest PAE)	
	Not-Tuned	Tuned	Not-Tuned	Tuned	Not-Tuned	Tuned
50 (L)		-38.2		-30.3		-26.6
50 (U)		-39.9		-31.4		-26.9
19.9 - j7.1 (L)	-35	-38.4	-26.3	-29.7	-23.3	-26.4
19.9 - j7.1 (U)	-39.7	-43.1	-31.2	-35	-25	-26.9
145.5 - j18.5 (L)	-37.8	-42.4	-28.3	-33	-25	-29.8
145.5 - j18.5 (U)	-38.3	-42	-29.9.	-33.5	-25.5	-29.3

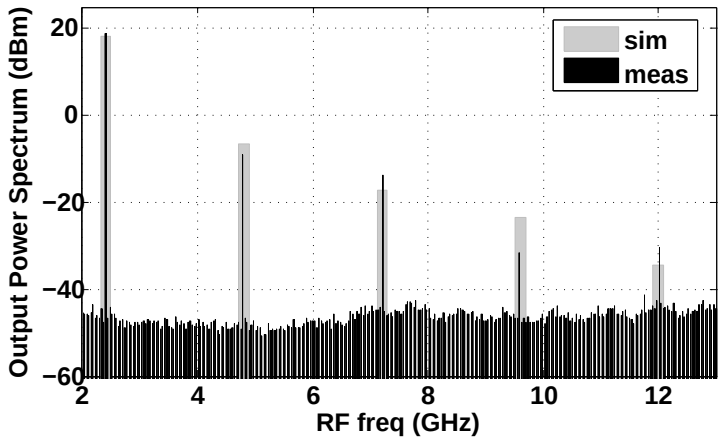


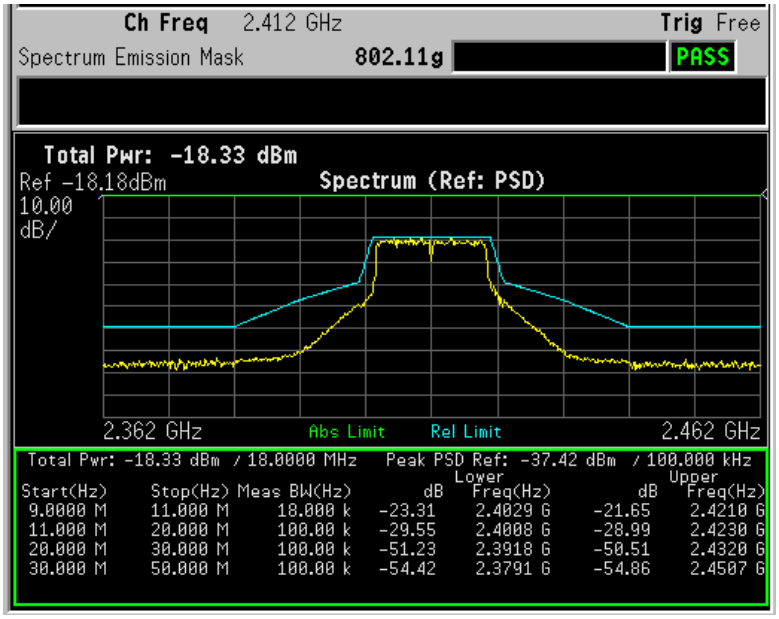
Figure 6.25: Simulated (grey) and measured (black) output power spectrum for 50 Ω load impedance.

6.9.2 Variable Load

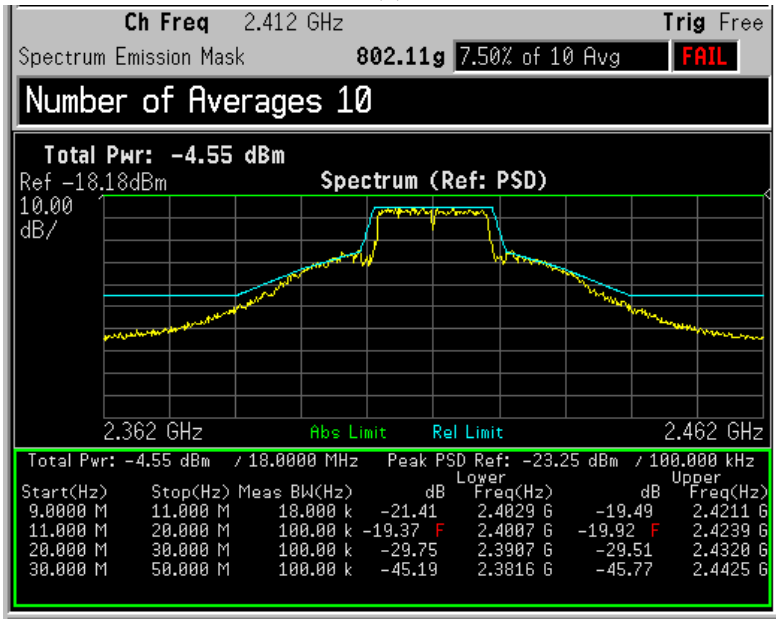
In order to test the effect of antenna load (Z_{LA}) variation, which can occur by the hand effect on the mobile phone, the PA is measured with different mismatched loads and tuned accordingly. The mismatched PA loads have been implemented using a coaxial tuner, composed of a sliding transmission line in cascade with a 25Ω line and appropriate attenuators, inserted in the amplifier output path between the output RF on-wafer probe and the directional coupler. This manual tuner is able to synthesize any load reflection coefficient with a magnitude up to 0.5 and arbitrary phase. The VNA must be re-calibrated for each desired PA load, corresponding to a position of the sliding transmission line.

Eight load impedances covering the theoretical load impedance region which is transformed within a circle of PAE = 27% have been synthesized at 2.4 GHz. These impedances are listed in Table 6.6. For each load impedance, first the performance is measured without applying any voltage to the MOS varactors (C_{var_1} and C_{var_2} in Fig. 6.6). This case is referred as not-tuned performance. Then these MOS varactors are tuned manually by changing the DC voltage applied to their gate ranging from -3 V to 3 V. This case is referred as tuned performance.

Three tuning conditions are considered: not-tuned, tuned using only C_{var_1} and tuned using both C_{var_1} and C_{var_2}. The performance of the PA regarding measured gain S_{21} are shown in Fig. 6.27 under different tuning conditions for these four load impedances. For each of the load impedances, it can be observed that when using C_{var_1} as tuning element the gain increases around 1-2 dB, and when using both C_{var_1} and C_{var_2} as tuning elements



(a)



(b)

Figure 6.26: Measured spectrum regrowth of a WiFi IEEE 802.11g signal produced by the PA with a matched 50Ω load. (a) $P_{out} = +\ 2$ dBm. (b) $P_{out} = +\ 18.5$ dBm (corresponding to maximum PAE). The indicated absolute power levels are not actual PA output power because of the measurement setup couplers and attenuators.

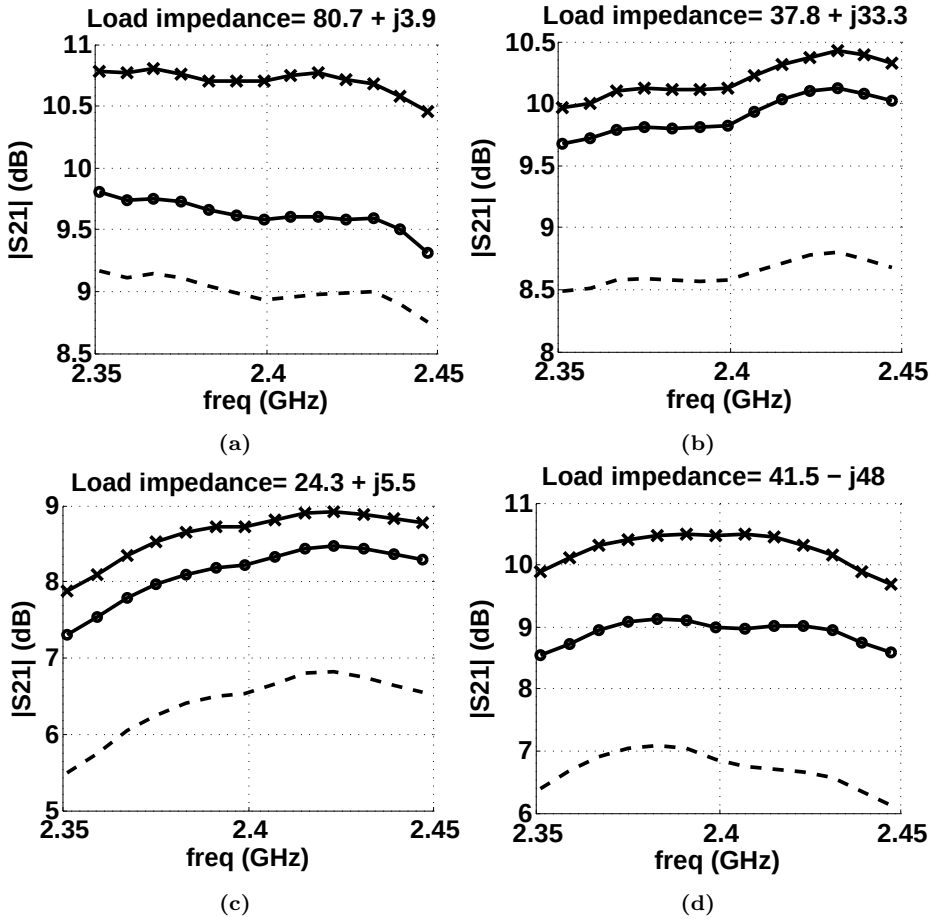


Figure 6.27: Measured $|S_{21}|$ (dB) with Pin= +5 dBm for different load impedances of (a) 80.7 + j3.9 Ω, (b) 37.8 + j33.3 Ω, (c) 24.3 + j5.5 Ω, and (d) 41.5 - j48 Ω compared in 3 different condition of no tuning (dashed), one varactor (Var_1) tuned (circle), and both varactors (Var_1 and Var_2) tuned (cross).

a total gain increase of 2 dB to 4 dB is achieved.

The performance of the PA regarding measured PAE, efficiency, and gain versus output power for four loads are demonstrated in Fig. 6.28, Fig. 6.29 and Fig. 6.30 respectively. The results are also compared in Table 6.6 showing that at each load impedance a significant increase in PAE, efficiency and output power is obtained. It can be observed that at 41.5 - j48 Ω an increase of 15% in PAE and DE and 4.4 dB in output power is achieved. This shows that the proposed circuit successfully compensates the effect of load variation on the power amplifier.

The performance of the PA regarding measured PAE and gain versus output power

Table 6.6: Measured results for different load impedances compared in default and tuned states.

Z_{LA_i} (Ω),	Not-Tuned		Tuned Var_1		Tuned Var_1 and Var_2	
(i=0,...,8)	PAE (%)	P_{out} (dBm)	PAE (%)	P_{out} (dBm)	PAE (%)	P_{out} (dBm)
50	-	-	-	-	**26**	**18.7**
80.7+j3.9	10	15.4	12	16	**18.6**	**17.5**
37.8+j33.3	11	15.7	17.1	17.2	**19.3**	**17.6**
24.3+j5.5	5	13.5	10.3	15.5	**12.4**	**16.1**
41.5-j48	4.7	13.3	10.7	15.6	**19.7**	**17.7**
19.1-j7.1	5.2	13.7	12.7	16.8	**15.3**	**17.5**
145.5-j18.5	6.5	13.4	16.2	16.4	**19.9**	**18.9**
18.8-j20.5	3.8	15.5	12	16.9	**13**	**17.5**
65.2-j66.4	4.7	18	13.1	19.2	**19.4**	**19.2**

for four selected loads are shown in Fig. 6.31 and Fig. 6.32 respectively. From Fig. 6.31 it can be observed that when using C_{var1} as tuning element, the gain and output power increase around 1-2 dB, and when using both C_{var1} and C_{var2} as tuning elements, a total gain and output power increase of 2 dB to 4 dB is achieved. The tuning results compared in Table 6.6 show a significant increase in PAE in the tuned condition with respect to not-tuned for each load impedance. For Z_{LA1}, Z_{LA2}, Z_{LA4}, Z_{LA6} and Z_{LA8}, the tuned PAE is close to 19%, in contrast to very low values for the not-tuned condition. The highest tuned PAE is 19.9% for Z_{LA6}, and the highest P_{out} is 19.2 dBm for Z_{LA8}, same as in the matched load condition. Z_{LA4} = 41.5 + j48 Ω reaches a tuned PAE of 19.7%. This shows that the proposed circuit successfully compensates the effect of PA load variation.

By tuning varactors C_{var1} and C_{var2} the nonlinear distortion is reduced with respect to not-tuned condition. As an example, Fig. 6.33 shows the measured spectrum regrowth for the mismatched load Z_{LA6} = 145.5 - j18.5 Ω before and after tuning. In the tuned state, the PA is delivering an output power P_{out} = 16 dBm. It can be observed that in tuned condition the spectrum regrowth is highly reduced, which is also confirmed by the ACLR data presented in Table 6.5. For Z_{LA6} the lower channel ACLR is reduced by 5 dB. A similar reduction can be observed for other mismatched loads. At highest Pout levels (optimum PAE) it can be observed that ACLR is -29.8 dBc, a better value than matched output load. These results show that the OMN tuner is able to not only match the switch-mode PA to antenna variations but also improves distortion and back-off characteristics.

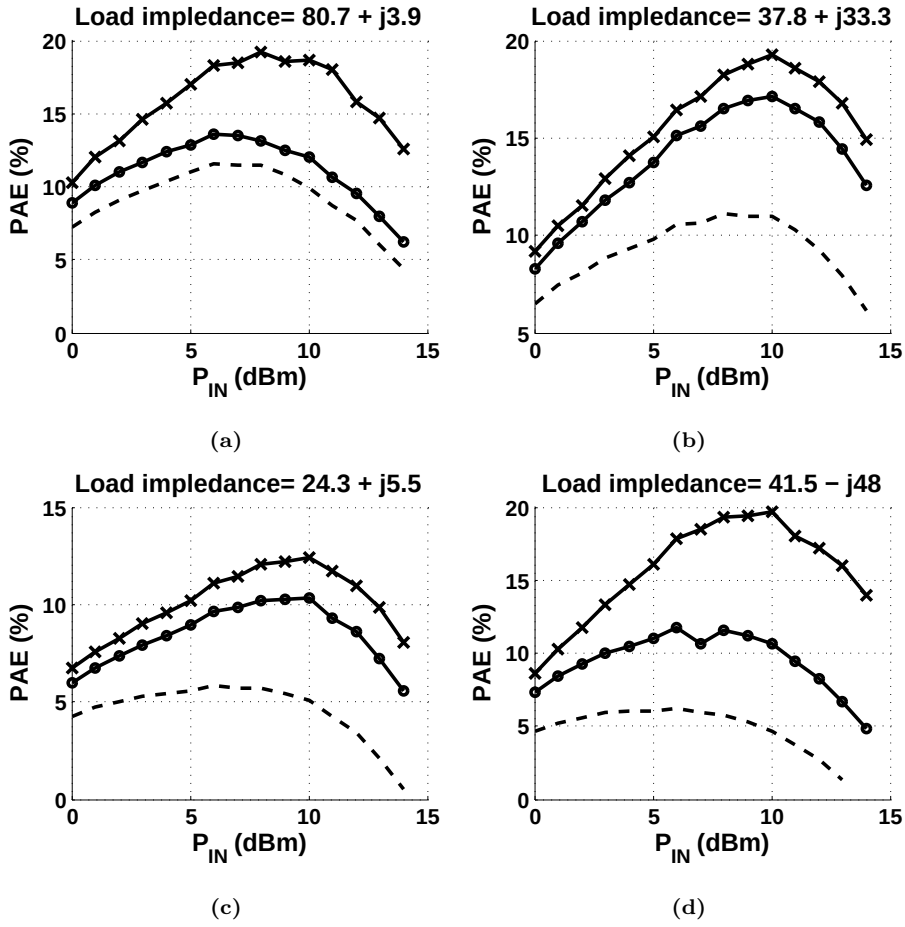


Figure 6.28: Measured PAE (black) and Drain Efficiency (grey) for different load impedances of (a) 80.7 + j3.9 Ω, (b) 37.8 + j33.3 Ω, (c) 24.3 + j5.5 Ω, and (d) 41.5 - j48 Ω compared in 3 different condition of no tuning (dashed), one varactor (Var_1) tuned (circle), and both varactors (Var_1 and Var_2) tuned (cross).

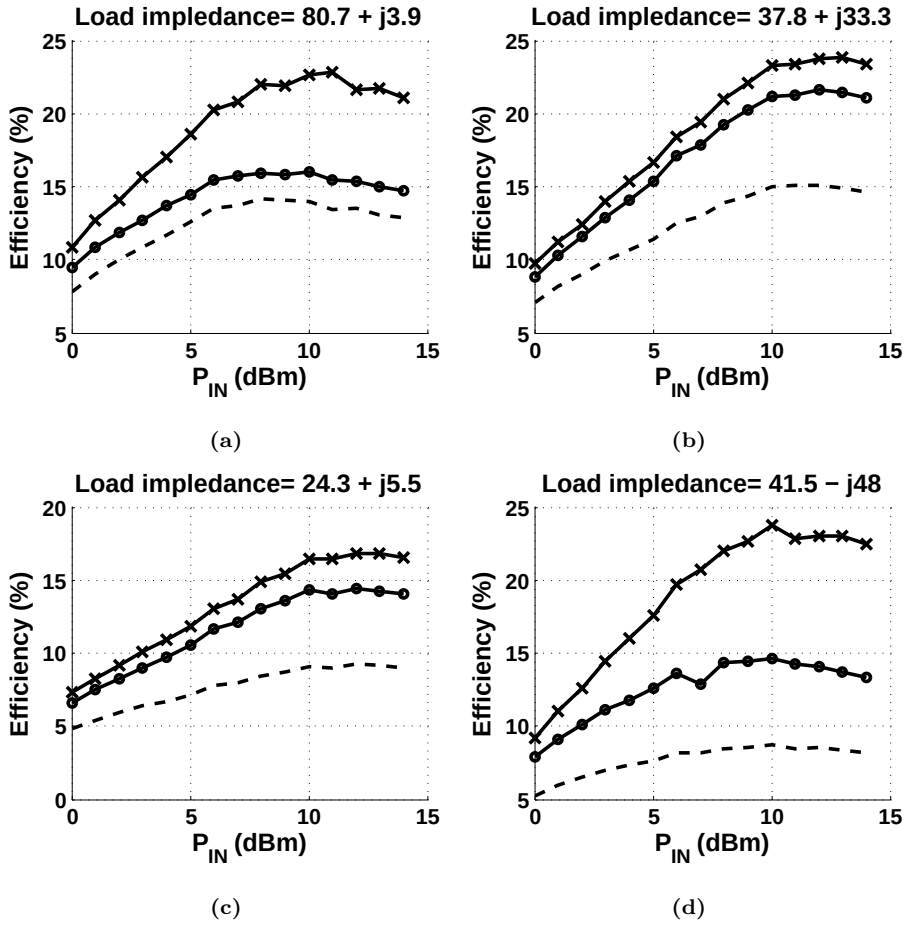


Figure 6.29: Measured PAE (black) and Drain Efficiency (grey) for different load impedances of (a) 80.7 + j3.9 Ω, (b) 37.8 + j33.3 Ω, (c) 24.3 + j5.5 Ω, and (d) 41.5 - j48 Ω compared in 3 different condition of no tuning (dashed), one varactor (Var_1) tuned (circle), and both varactors (Var_1 and Var_2) tuned (cross).

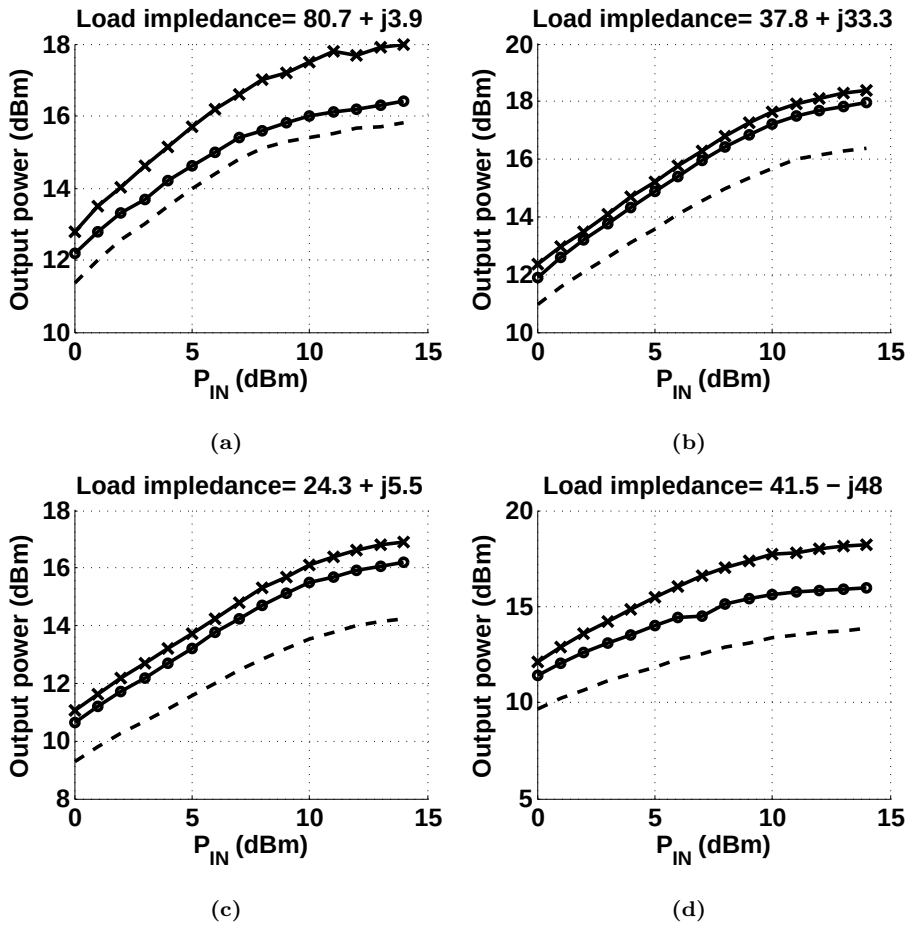


Figure 6.30: Measured output power for different load impedances of (a) 80.7 + j3.9 Ω, (b) 37.8 + j33.3 Ω, (c) 24.3 + j5.5 Ω, and (d) 41.5 - j48 Ω compared in 3 different condition of no tuning (dashed), one varactor (Var_1) tuned (circle), and both varactors (Var_1 and Var_2) tuned (cross).

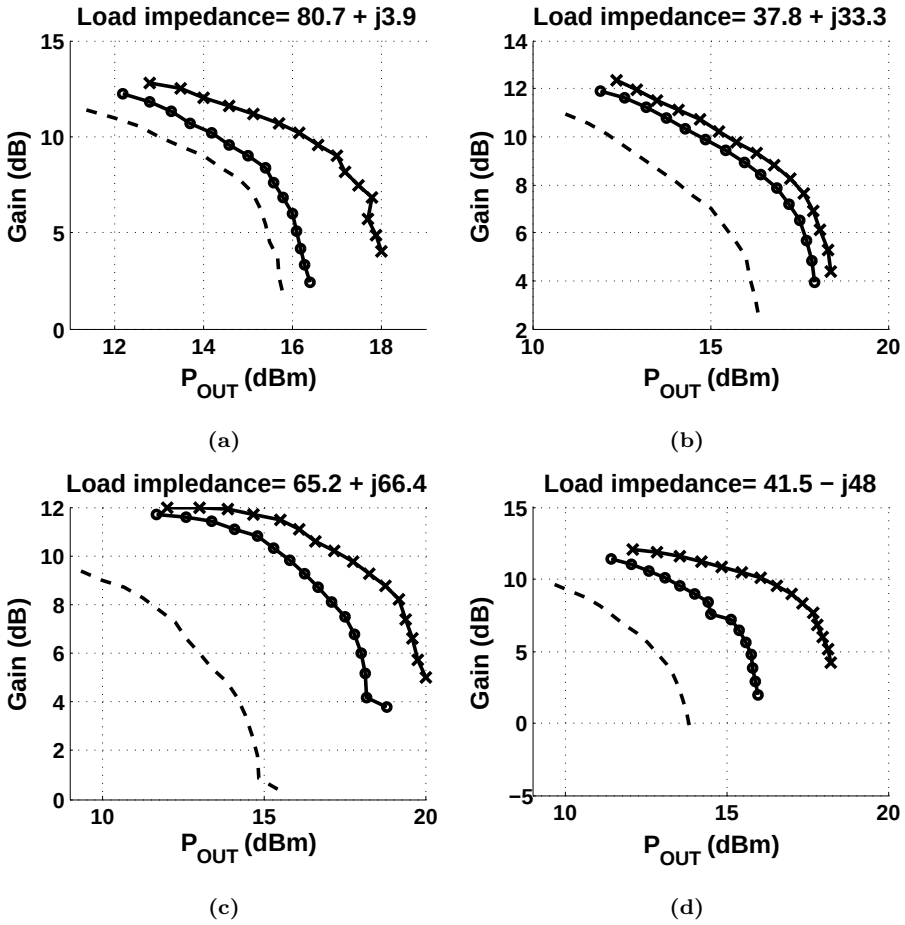


Figure 6.31: Measured Gain versus output power for different load impedances of (a) 80.7 + j3.9 Ω, (b) 37.8 + j33.3 Ω, (c) 65.2 + j66.4 Ω, and (d) 41.5 - j48 Ω compared in 3 different condition of no tuning (dashed), one varactor (Var_1) tuned (circle), and both varactors (Var_1 and Var_2) tuned (cross).

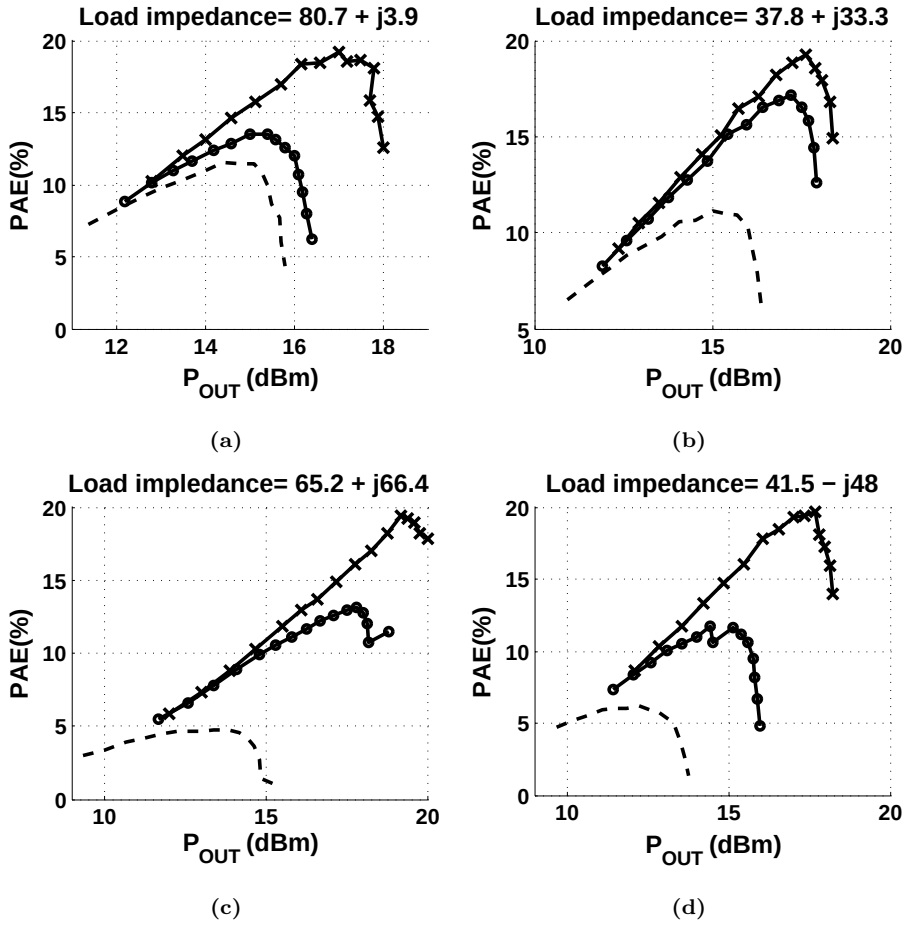
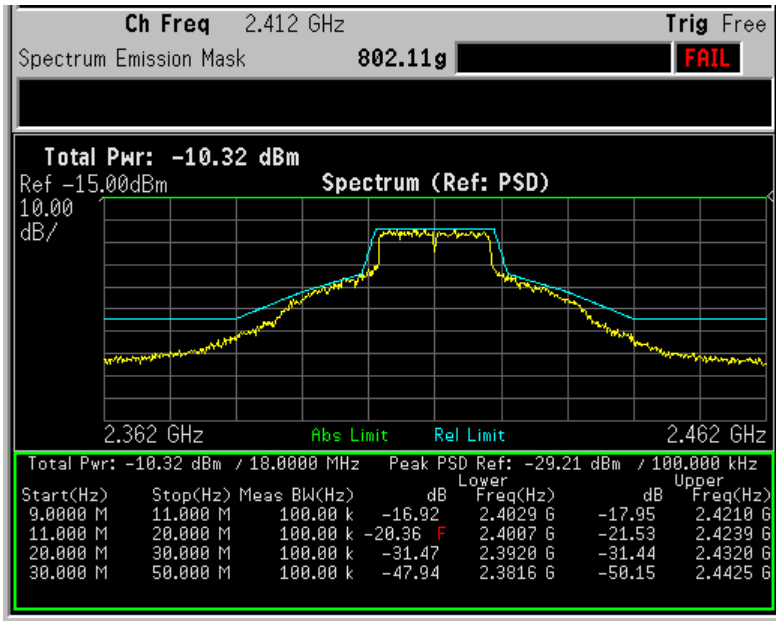
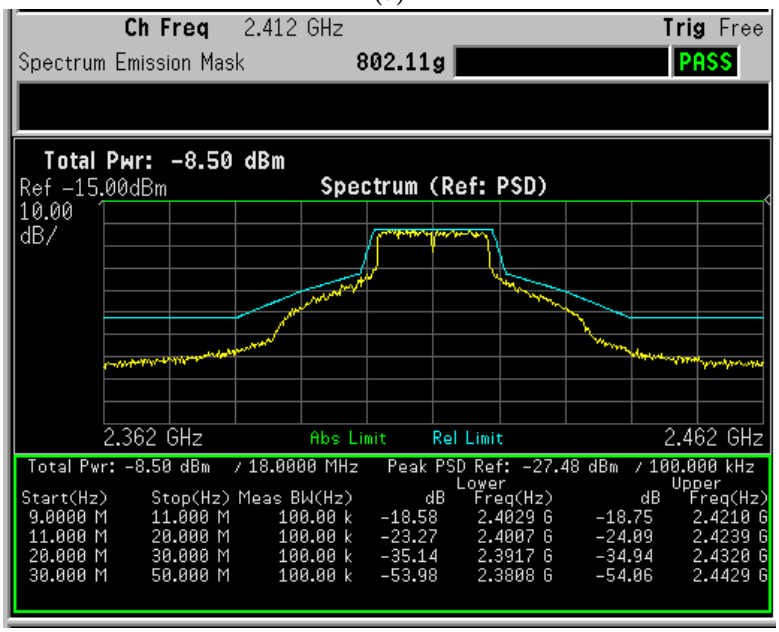


Figure 6.32: Measured PAE versus output power for different load impedances of (a) 80.7 + j3.9 Ω, (b) 37.8 + j33.3 Ω, (c) 65.2 + j66.4 Ω, and (d) 41.5 - j48 Ω compared in 3 different condition of no tuning (dashed), one varactor (Var_1) tuned (circle), and both varactors (Var_1 and Var_2) tuned (cross).



(a)



(b)

Figure 6.33: Measured spectrum regrowth of a WiFi IEEE 802.11g signal produced by the PA with a matched 50Ω load: (a) Not-tuned state and (b) Tuned state with $P_{out} = 16$ dBm.

7

Chapter 7

CMOS Power Reconfigurable Class-F PA using MEMS Variable Capacitor

In this chapter, a novel reconfigurable class-F PA is proposed. The proposed PA can adapt to different impedance values presented to its load and is intended for handsets and WiFi application. The amplifier is designed at 2.4 GHz and the implementation is carried out in CMOS technology. The design incorporates MEMS capacitors as the tuning device. This MEMS capacitor is fabricated in CMOS technology without further mask step and is released with post-processing technique. The proposed structure controls up to 3^{rd} harmonic and it includes a proper harmonic tuning network which removes the requirement of an extra filtering section. The effect of the load variation is compensated by reconfiguring the output network using a configuration of impedance tuner which consists of two independent variable capacitors.

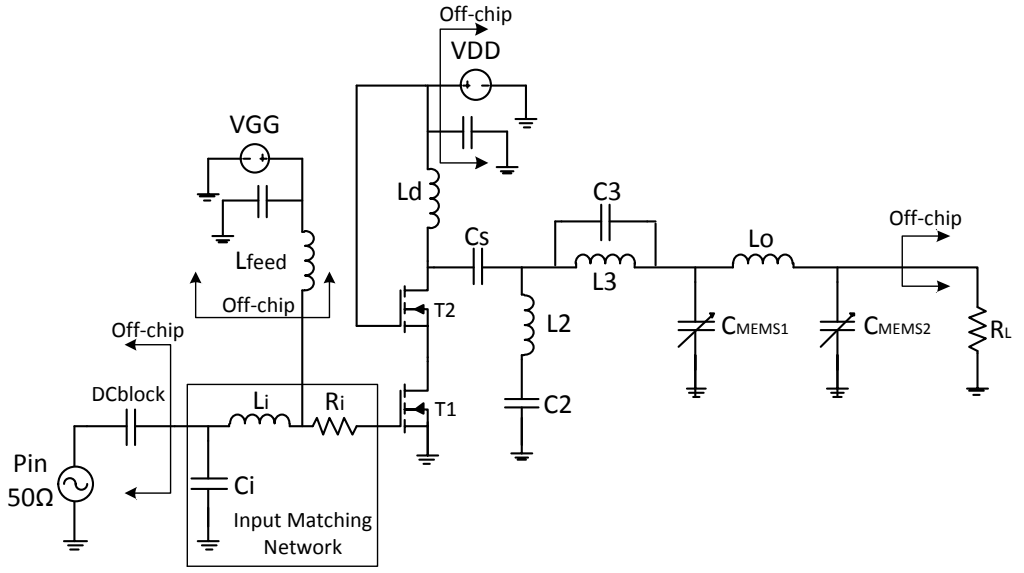


Figure 7.1: Proposed reconfigurable class-F PA using MEMS switches as reconfiguring element.

7.1 Proposed Reconfigurable Class-F Power Amplifier

The proposed integrated reconfigurable class-F power amplifier is illustrated in Fig. 7.1. The active device in this design is a 3.3 V thick oxide 0.18 μm NMOS transistor available in TSMC^{TM} 0.18 μm 1P6M CMOS technology with ultra thick top metal (UTM) layer. The same explanation for input and output matching network explained in the previous chapter, section 6.1 is valid for this design. The only difference is that the reconfiguring element is a MEMS variable capacitor and inductors are designed with multi-layer stacking approach which will be explained in the following.

7.2 Microelectromechanical Systems (MEMS) in CMOS Technology

MEMS variable capacitors are electrical devices whose capacitance value is controlled through mechanical actuation. Capacitance can be tuned by mechanically changing the gap or overlap area. Depending on the actuation voltage, the capacitance value can vary continuously or discretely. Devices with continuous tuning range are called variable capacitors and devices with on-off states, are referred to as switched capacitors. MEMS devices have demonstrated low insertion loss compared to semiconductor switches, good

RF performance, low DC consumption and better linearity. There have been several studies to integrate MEMS devices in CMOS technology [118–120]. A complete overview of the approaches of MEMS devices integration in CMOS has been given in [121].

The utilized RF MEMS capacitors in this design are designed using the 0.18 μm CMOS Back End of Line (BEOL) metallization. The MEMS capacitor design is based on the maskless CMOS-MEMS post-processing technique which was developed at the University of Waterloo [7, 122]. For MEMS capacitor implementation using this concept, the technology should include at least four Metal layers. In MEMS implementation, going from the bottom metal layer (M1) to the top metal layer (M4):

- M1 is the bottom plate of the capacitor
- M2 is the sacrificial layer
- M3 is the top plate of the capacitor
- M4 is the mask layer in the post processing

The MEMS structure before post processing is presented in Fig. 7.2, taken from [123]. The steps of the aforementioned special post processing technique to release the MEMS capacitors in CMOS technology are the following:

1. **First dry etching**: Anisotropic Reactive Ion Etching (RIE) of the silicon dioxide. The areas that are not covered by the mask layer (one of the top metal layers), will be etched away and what is below the mask will stay untouched. Fig. 7.3 shows the CMOS metal stack after 1^{st} dry etching.
2. **Wet etching**: By removing the dielectrics in the previous step, the sacrificial layer and silicon substrate are now unprotected. Hence in this step by isotropic and anisotropic wet etching, the Aluminum of the exposed metal layers (sacrificial and mask layers) and the silicon substrate are etched away. To provide a better etching of the substrate below MEMS structure, an isotropic RIE can be performed prior to wet etching Fig. 7.4. The CMOS metal stack after wet etching is shown in Fig. 7.5. The mask layer is extended 2 μm over the MEMS plates in order to protect them during wet etching. A trench of 100 μm is created in the silicon substrate to improve the quality factor of the capacitor and enhance the RF performance.
3. **Second dry etching**: This step is used to remove the dielectric on the top of input/output pads, the biasing pads, and from the top of MEMS capacitor's top plate in order to reduce stiffness. The figure of CMOS metal stack after 2^{nd} dry etching is provided in Fig. 7.6. At this point the MEMS structure is released.

A 0.18 μm CMOS consists of six metal layers, hence 3 different combinations of metal layers can be used to implement the MEMS capacitor as shown in Fig. 7.7. Choosing

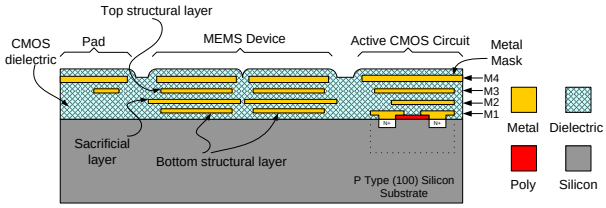


Figure 7.2: The MEMS structure before post processing. Figure taken from [123].

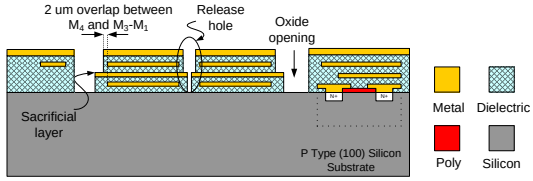


Figure 7.3: First RIE removal of CMOS dielectric layer. Figure taken from [123].

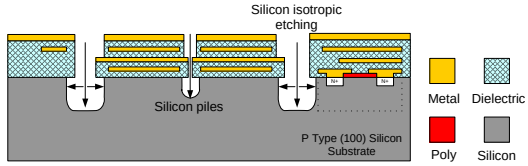


Figure 7.4: Isotropic dry etching. Figure taken from [123].

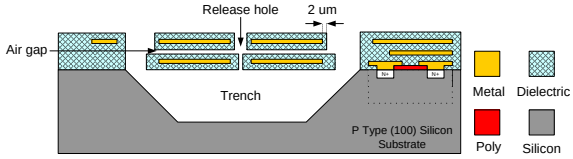


Figure 7.5: Wet etching of the sacrificial layer and the silicon substrate. Figure taken from [123].

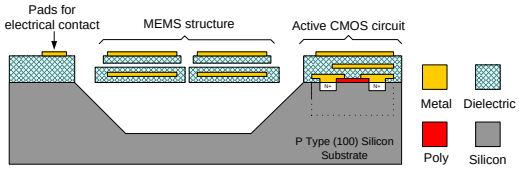


Figure 7.6: CMOS chip after the second RIE of the CMOS dielectric layer. Figure taken from [123].

the metal plates depends on the layout requirements and capacitor performance in the whole design including other CMOS components. In this design MEMS capacitors are implemented by M3 as the bottom plate and M5 as the top plate, having M4 as the sacrificial layer and M6 as the mask layer. Metal 6 extends 2 μm over metal 5 and metal 3 to protect the capacitor's plates from being etched away. The MEMS capacitor is later released by etching away the silicon substrate and one or more metal layers as the sacrificial layer.

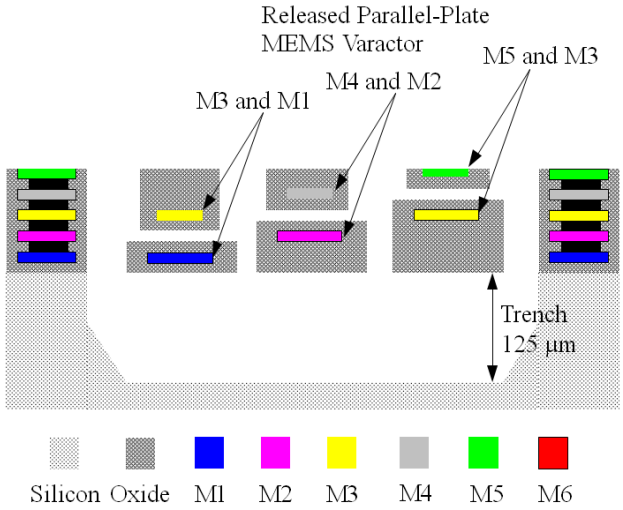


Figure 7.7: Cross-section of MEMS-CMOS post-processing technique in TSMC 0.18 μm CMOS process. Figure taken from [124].

The proposed MEMS varactor is illustrated in Fig. 7.8. To validate its performance a simulation is performed in HFSS (High Frequency Electromagnetic Field Simulation) for fixed plates. The simulation setup and the results are given in Fig. 7.9 showing 1.7 pF is achieved on this capacitor when there is no voltage applied. Two different sizes of the MEMS analogue continuous capacitor [7] are designed to achieve targeted values of 0.9 - 1.8 pF for CMEMS1 and 0.9 - 1.5 pF for CMEMS2. The quality factor at 2.4 GHz exceeds 100 [7].

7.3 Inductor Implementation

The design of RF passive components (inductors and capacitors) in CMOS technology is challenging in PA design because high-Q lumped elements are difficult to achieve. The losses of these components affect the output power and efficiency of the PA. On-chip inductors suffer from ohmic losses (due to metal resistance), capacitive losses (due to

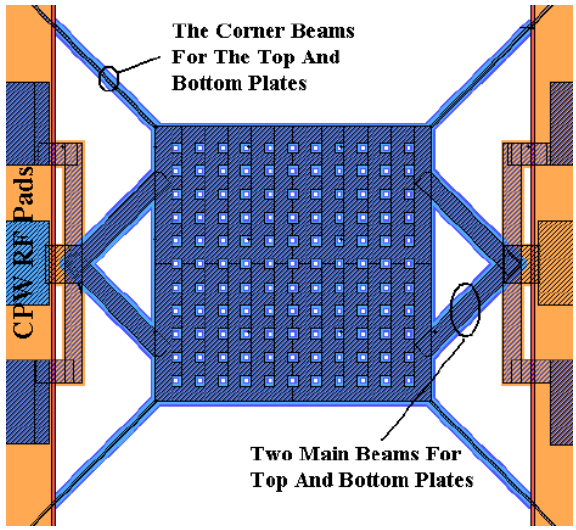
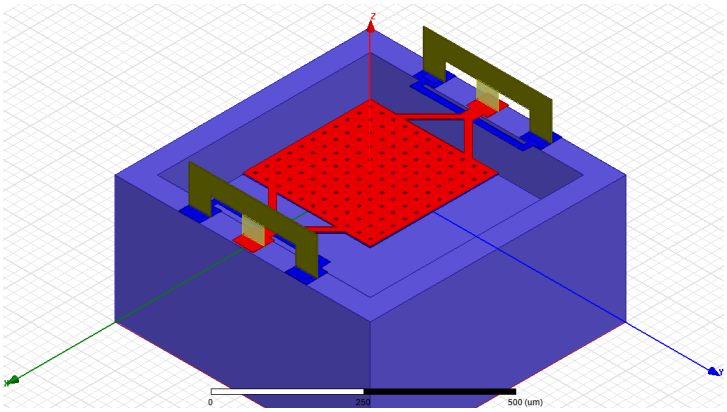


Figure 7.8: Proposed analog MEMS continuous capacitor in [7].

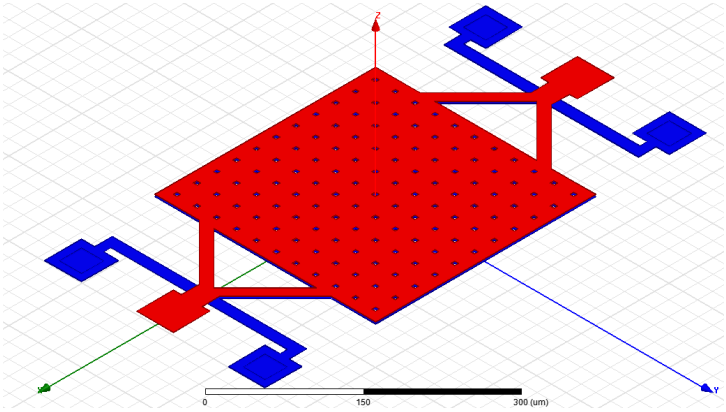
electric coupling from the metal line to the substrate) and inductive losses (due to eddy currents generated by magnetic fields going through the substrate). Inductive losses come from skin effect and proximity effect in inductors. To reduce these losses, the thickest layer and highest metal layer is preferred. The higher the top layer of the inductor, the thicker dielectric between and the lower parasitic capacitance to the substrate will be achieved. However, since for this design M6 which is an UTM layer is used as the mask layer for MEMS capacitors, inductors should be fabricated in lower metal layers. These lower metal layers have smaller thickness compared to UTM, hence much higher resistance and lower current handling capability.

The two-dimensional inductor types are shown in Fig. 7.10 [125]. A spiral inductor is made of a top metal layer for spiral structure and the bottom metal layer which is an underpass to connect to the rest of the circuit. Meander line has the advantage of low eddy current loss but it has the lowest inductance and Self Resonant Frequency (SRF). The rectangular inductor has a simple layout but it has a low SRF as well. The circular and octagonal inductors both have higher SRF but their layout is more difficult to implement. The best performance is achieved by circular inductors, however, due to design rules of utilized CMOS technology, circular inductors cannot be implemented. Hence octagonal ones are chosen because they have the best performance after circular ones.

The utilized inductor in this design is an octagonal spiral inductor shown in Fig. 7.11. The inductor value and its Q-factor depend on the geometry of the inductor, more precisely: the width of metal (W), the space between metals (s), the number of turns (n), the radius of the inductor (D) and the thickness of the metal layer. The width of



(a)



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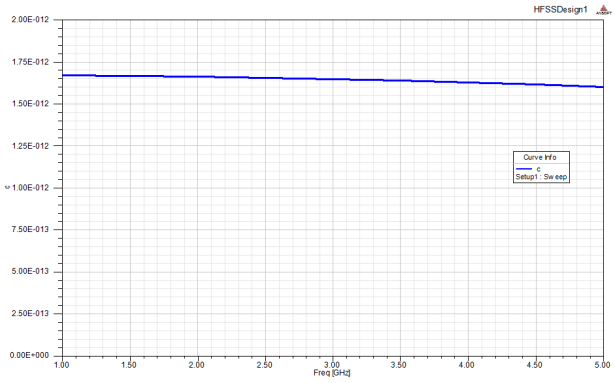


(c)

Figure 7.9: (a) HFSS test setup for MEMS capacitor, (b) MEMS structure in 3D, and (c) simulated capacitance value for fixed plates.

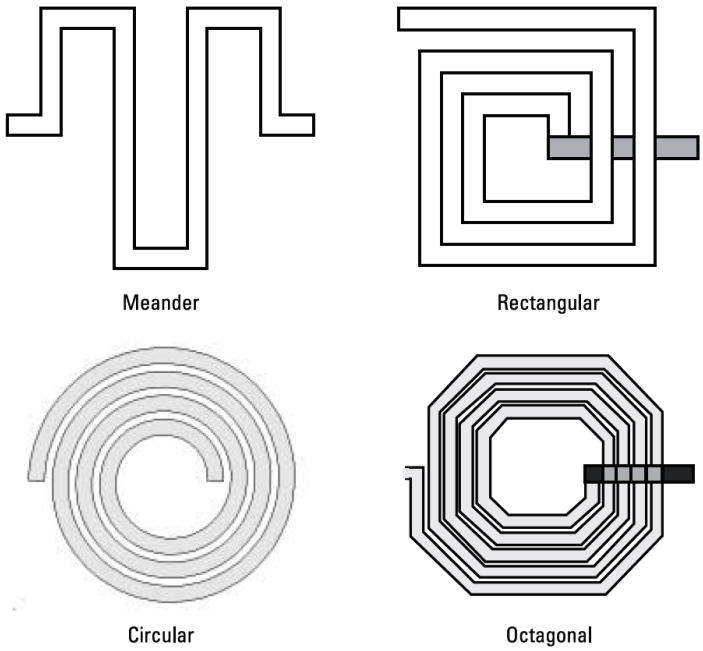


Figure 7.10: Two dimensional inductor types [125].

the inductor should not be too wide in order to achieve an optimum Q, with a typical value of 10 μm to 15 μm for a frequency range of 1-3 GHz [126]. The spacing between the metals should be the minimum allowed by technology in order to increase the magnetic coupling and therefore the Q-factor of inductor.

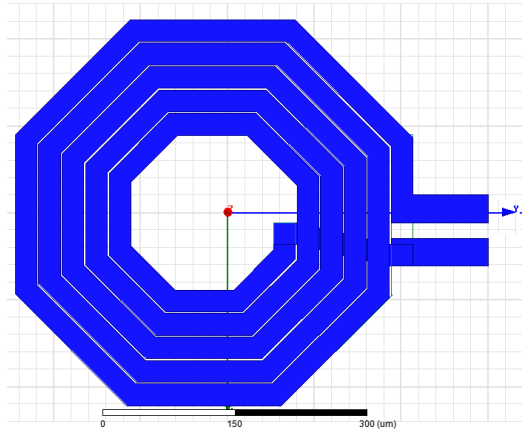


Figure 7.11: Top view of the utilized inductor.

The final proposed structure is parallel stacking the inductor of Fig. 7.11 in different

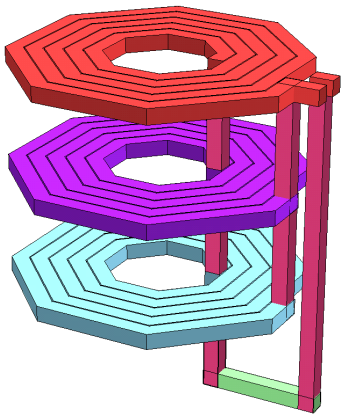


Figure 7.12: The 3D view of the parallel stacked octagonal indcutor.

metal layers (M2 to M5) in order to increase current capability while occupying a small area, which is an advantage in integrated designs. The final inductor structure is illustrated in Fig. 7.12. Electromagnetic simulation results show that a Q of 7.3 for L_3, 10 for L_d, 7.8 for L_i, and 10.7 for L_o are achieved. Using the post processing technique, a trench will be created beneath to further increase the Q and decrease the losses from the substrate.

7.4 Power Amplifier Implementation

The proposed class-F PA is designed in the aforementioned TSMC^{TM} 0.18 μm with 1 poly and six metal layers (M1 to M6) 1P6M CMOS technology with UTM layer. A picture of the fabricated chip is shown in Fig. 7.13. Transistors T1 and T2 connected in cascode in Fig. 7.1 have the same width of 64 $\times$ 8 μm. The final chip has 24 pads, three for input RF signal (input pads) and three for output RF signal (output pads). The circuit is under post processing at the moment of writing this thesis and the post processing steps are not completed. There are figures available after first dry etching and second wet etching which are illustrated in Fig. 7.14 and Fig. 7.15 respectively. The measurement will be performed as soon as the post-processing is finished.

7.5 Simulation Results

To evaluate the performance of the proposed PA design, simulations are performed using Keysight ADS and Cadence Spectre RF. The simulated drain voltage and current waveform of the PA are shown in Fig. 7.16. The power spectrum for the case of 50Ω

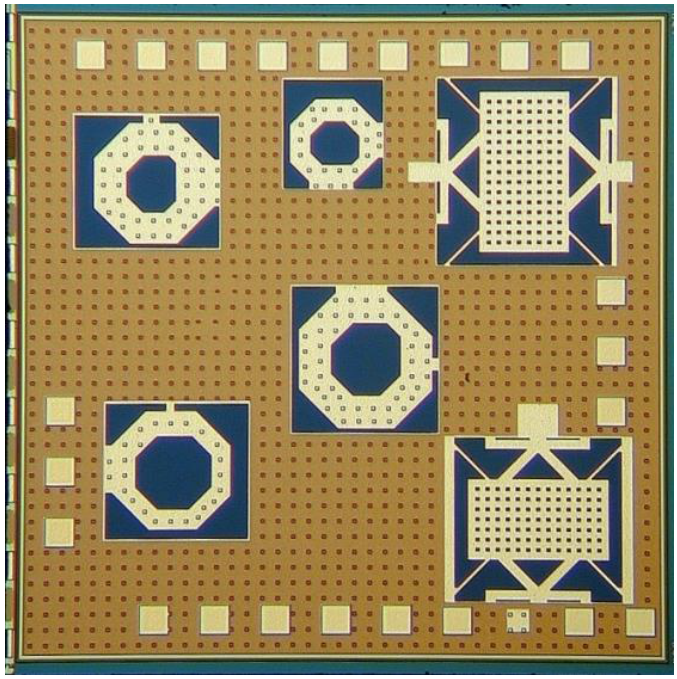
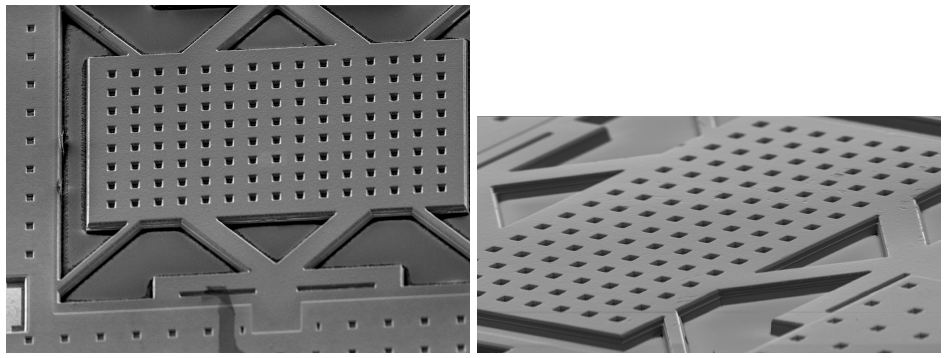


Figure 7.13: Fabricated circuit in TSMC^{TM} 0.18 μm 1P6M CMOS technology. Die size is 1.6 mm $\times$ 1.6 mm.

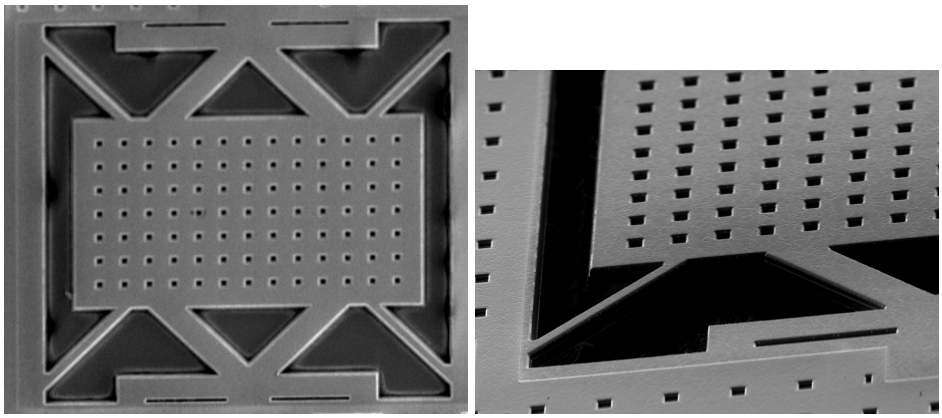


(a) **(b)**

Figure 7.14: Upper MEMS capacitor (MEMS1) after first dry etching.

load impedance is shown in Fig. 7.17. The proposed PA achieved a 2^{nd} and 3^{rd} harmonic rejection of 26.9 dBc and 44.8 dBc respectively.

The simulated results of power added efficiency (PAE) and efficiency versus input power are shown in Fig. 7.18. The output power and gain simulation results versus input power are presented in Fig. 7.19. For an output load impedance of 50Ω and an input



(a) (b)

Figure 7.15: Lower MEMS capacitor (MEMS2) after wet etching.

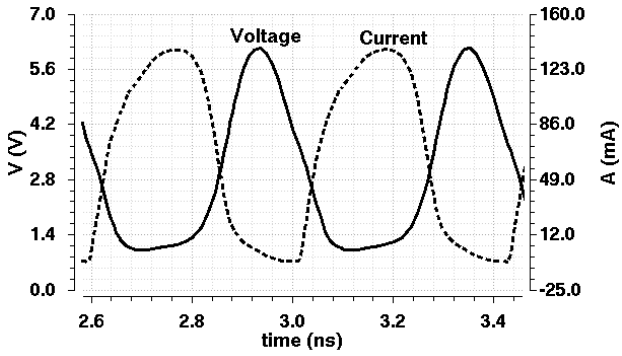


Figure 7.16: Drain voltage (solid) and current waveforms (dash) of the proposed class-F PA.

power of 7 dBm, a peak PAE of 32.8%, a drain efficiency of 34.6% and a gain of 12.9 dB are obtained while delivering an output power of 18.2 dBm. Values of C_{MEMS1} and C_{MEMS2} are 1.7 pF and 1 pF for this case.

To test the effect of load variation, other impedance values are considered for the load and the MEMS capacitors are tuned accordingly. The results are compared to a case where there has not been any tuning (meaning that the C_{MEMS1} and C_{MEMS2} remained the same values of 1.7 pF and 1 pF respectively). The results are shown in Table 7.1. In all of the cases, a higher PAE and a higher output power are achieved by tuning the circuit.

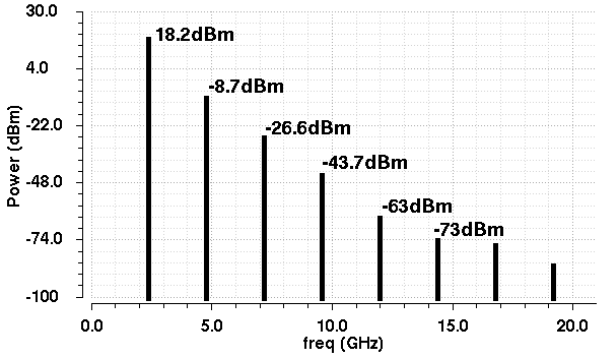


Figure 7.17: Output power spectrum for 50 Ω load impedance. It shows a 2^{nd} and 3^{rd} harmonic rejection of 26.9 dBc and 44.8 dBc respectively.

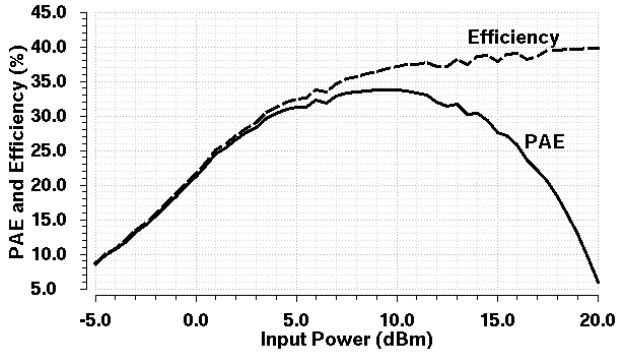


Figure 7.18: Simulation results for drain efficiency % (dash) and PAE % (solid) versus input power.

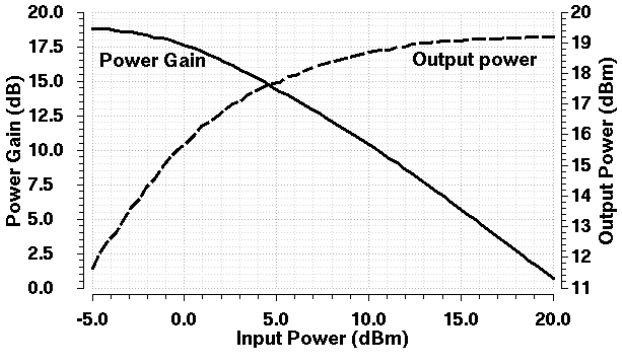


Figure 7.19: Simulation results for delivered output power (dash) and power gain (Solid) versus input power.

Table 7.1: Simulated results for different load impedances compared in default and tuned states.

Load Impedance(Ω)	PAE(%)	P_{out}(dBm)	Case
50	32.8	18.2	Default
50 + j75	24	16.7	Tuned
	17.4	15.8	not-Tuned
75 + j50	29.8	17.5	Tuned
	23.3	17	not-Tuned
75 + j100	20.4	16.4	Tuned
	13.8	15.1	not-Tuned
100	27	17.7	Tuned
	24	17.3	not-Tuned
100 + j50	26.1	17.6	Tuned
	21.1	16.8	not-Tuned
30 + j75	21	16	Tuned
	13.6	14.7	not-Tuned

8

Chapter 8

Conclusion

This chapter describes the conclusion of this doctoral thesis. It summarizes the work that have been done.

8.1 Main Conclusions

This thesis was focused on providing solutions for the most critical block of transmitters i.e. power amplifiers (PAs). Power amplifiers are the most power hungry devices in the whole transceiver blocks and if the efficiency of the PA is not high, it results in a short battery lifetime of the device. In addition, the dissipated power transforms to heat, which can bring reliability issues and degrade the lifetime of the PA itself. Therefore the main objective of this thesis was reliable high efficiency PA design. Among the different classes of the PA, class-F PA has been used as main efficiency enhancement technique.

Therefore this thesis discussed reconfigurability approaches that are suitable for high efficiency class-F radio frequency power amplifiers, proposed new structures and aimed to solve two fundamental issues of wireless transmitter devices: change of frequency and change of antenna load.

1. **High Efficiency Low Harmonic Distortion Class-F PAs**: A detailed study of high efficiency class-F power amplifiers following a comparison of different structures from the literature was performed and finally a novel highly efficient class-F PA topology for mobile applications has been proposed. The proposed structure focuses on the topology requirements to have low harmonic distortion in the output signal and overcomes the narrow band performance of the class-F structure. It provides a contribution in the transmission line class-F PA designs in which with a proper harmonic tuning structure a low total harmonic distortion was achieved and the need for extra filtering sections were eliminated. Two proof of concept class-F PAs were designed employing a GaN HEMT device with the focus on high efficiency, high power and matched to input and output 50Ω loads. The fabricated PAs showed the state of the art performance with a PAE of 80.3% and 72.1% for 900 MHz and 1800 MHz PA respectively.
2. **Dual-band Frequency Reconfigurable High Efficiency Class-F PAs**: A detailed study of frequency reconfigurability of a class-F power amplifier was performed. The proposed single frequency class-F topology was then developed to cover multiple frequency bands for purpose of global coverage with main requirements of high efficiency, high power, and low harmonic distortion, all with the aim of size reduction. Three novel dual-band frequency reconfigurable PA configurations have been proposed using MEMS and semiconductor switches. The main contributions are proposing solutions for a proper reconfigurability implementation depending on the type of the switch and its power capability. Three different topologies have been proposed for this purpose which accomplish class-F operation at two frequencies. The main novelty of this structure is that the

reconfiguration was done not only at fundamental frequency but also at harmonics which resulted in a high performance and low distortion in both frequency bands, with a reduced number of tuning elements. Moreover, by proper placement of the switches in the stubs, the maximum voltage over the switches was minimized. The measurement results of the three fabricated PAs showed that the PA with special consideration on the placement of the switch achieved the highest performance among all three, showing a 69.5% PAE, 72.5% efficiency and 39.1 dBm output power at 900 MHz and 57.9% PAE, 63.5% efficiency and 38.5 dB output power at 1800 MHz. The proposed PA overcame the narrow band nature of class-F power amplifiers, giving an efficiency more than 60% over a bandwidth of 225 MHz and 175 MHz, at 900 MHz and 1800 MHz bands respectively.

3. **CMOS Impedance Reconfiguable High Efficiency Class-F PAs**: A detailed study of load impedance reconfiguration of a class-F power amplifier and its integration in CMOS technology was performed. The integration of class-F PA in CMOS technology is a challenge due to the low breakdown voltage of the CMOS and high power requirement of the PA. The main contribution of this work is a novel impedance reconfigurable structure suitable for class-F amplifiers. It also brings a solution for monolithic integration of PA with other components in the handset, improving performance and reliability and reducing cost. This CMOS power amplifier was designed at 2.4 GHz for WiFi applications. The main goal is to compensate the effect of load impedance variation on the PA performance. The load variation is produced by the effect of hand and head over the handset. The load impedance reconfiguration capability is achieved by using an impedance tuner in its output network. The proposed amplifier uses a proper harmonic tuning network up to 3^{rd} harmonic, eliminating the need for an extra filtering section and providing a good trade-off between distortion, PAE and output power.

   Two designs have been presented using MOS varactors or MEMS variable capacitors as tuning device. The first design of a reconfigurable class-F power amplifier using MOS varactors showed a maximum measured values of 29.2% efficiency, 26% PAE and 19.2 dBm output power for a load of 50Ω. The performance for loads other than 50Ω showed an increase of 15% in PAE and 4.4 dB in output power compared to non-tuned one. The second design of reconfigurable class-F power amplifier was implemented using MEMS devices. The main contribution was the integration of reconfigurable class-F PA in CMOS technology while incorporating MEMS switches that were compatible with CMOS technology and did not need extra mask layers. With a special post-processing technique, the MEMS capacitors were released. Solutions for integrating high-Q

inductors in this process have been provided. This PA brings a solution for single-chip implementation of MEMS devices in CMOS reconfigurable PAs which eliminates the problems of hybrid bonding hence improving performance and lowering the cost. Simulation results for a load impedance of 50Ω showed that the PA achieves a PAE of 32.8% and a gain of 12.9 dB while delivering peak output power of 18.2 dBm.

8.2 Future Research Lines

While this thesis tackled different key aspects of wireless communication, it also opened the door for future research in the following aspects:

- **First,** expanding the work of frequency reconfigurable class-F PA from hybrid implementation to CMOS integration with the possibility of a multi-band implementation. The topology and the design procedure would be slightly different than the one provided in chapter 5 because for CMOS integration, lumped-elements should be used instead of transmission lines. This research topic has a special interest in the framework of software defined radio, as it would provide a truly multi-standard application, being able to use different frequency bands. The next step would be to extend the load impedance tuning structure proposed in this thesis to multi-band operation. This means providing a structure that reconfigures frequency and also compensates the impedance load variation in the selected band. Also one can consider frequency reconfiguration of more than two frequency bands.
- **Second,** study the operation at higher frequencies. Due to increasing communication frequencies, it is of great interest to study reconfigurability and integration at 5 GHz and beyond, targeting not only 4.5G but 5G communications. Even in the cases where millimeter-wave is considered, the key aspects pointed in this thesis still hold and can be used as a reference, albeit passive components should be replaced by transmission lines.
- **Third,** study the algorithm and auxiliary circuits to provide adaptive load tuning. In this thesis, a novel tuner has been presented as a proof of concept, however, in the application, a tuning method would be required to adapt the operating conditions to the optimal point. In that sense, a perturbation and observation algorithm could be implemented, as impedance changes are produced by user movements, hence expected to be relatively slow.
- **Fourth,** study the application of high efficiency amplification by adding envelope

tracking or polar amplification. By using envelope tracking, the efficiency of the amplifier is expected to increase, while load impedance reconfiguration would still be available.

Acronyms

AC Alternating Current

ACLR Adjacent Channel Leakage Ratio

ADS Advanced Design System

ACPR Adjacent Channel Power Ratio

BEOL Back End Of Line

BiCMOS Bipolar Complementary Metal Oxide Semiconductor

CMCD current Mode Class-D

CMOS Complementary Metal Oxide Silicon

CNT Cascode Thin-Thick-Oxide Transistors

CTT Cascode Thick-Thick-Oxide Transistors

DC Direct Current

DE Drain Efficiency

DUT Device Under Test

EER Envelope Elimination and Restoration

EM Electromagnetic

ET Envelope Tracking

FET Field Effect Transistor

GaAs Gallium Arsenide

GaN Gallium Nitrite

GHz Gigahertz

GMSK Gaussian Minimum Shift Keying

GND Ground

GSG Ground-Signal-Ground

GSM Global System For Mobile Communication

HEMT High Electron Mobility Transistor

HB Harmonic Balance

HFSS High Frequency Electromagnetic Field Simulation

HP Hewlett-Packard

IC Integrated Circuit

IMN Input Matching Network

IPD Integrated Passive Devices

LDMOS laterally Diffused Metal Oxide Semiconductor

LNA Low Noise Amplifier

LSSP Large Signal S-parameter

LTE Long Term Evolution

MEMS Microelectromechanical System

MHz Megahertz

MIM Metal-Insulator-Metal

MN Matching Network

MMIC Microwave Monolithic Integrated Circuit

MOS Metal Oxide Semiconductor

MOSFET Metal Oxide Semiconductor Field Effect Transistor

NMOS N-type Metal Oxide Semiconductor

OC Open Circuit

OFDM Orthogonal Frequency Division Multiplexing

OMN Output Matching Network

PA Power Amplifier

PAE Power Added Efficiency

PAPR Peak-to-Average Power Ratios

PCB Printed Circuit Board

pHEMT pseudomorphic High Electron Mobility Transistor

PM Phase Modulation

QAM Quadrature Amplitude Modulation

RIE Reactive Ion Etching

RF Radio Frequency

RFC Radio Frequency Choke

rms Root Mean Square

SC Short Circuit

SEM Scanning Electron Microscope

Si Silicon

SiGe Silicon Germanium

SN Single Thin-Oxide Transistor

SP Scattering Parameters

S-parameters Scattering Parameters

SPDT Single Pole Double Throw

SPST Single Pole Single Throw

ST Single Thick-Oxide Transistor

SW Switch

THD Total Harmonic Distortion

TL Transmission line

TSMC Taiwan Semiconductor Manufacturing Company

UTM Ultra Thick Top Metal

VNA Vector Network Analyzer

WiFi Wireless Fidelity

WLAN Wireless Local Area Networks

WCDMA Wideband Code Division Multiple Access

ZVS Zero Voltage Switching

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List of Publications

1. **Mitra Gilasgar**, Antoni Barlabe, Lluis Pradell , "A very low distortion high efficiency class-F power amplifier at 900 MHz," *XXVIII Simposium Nacional de la Union Cientifica Internacional de Radio (URSI)*, vol. 45, pp. 2007-2012, Sep 2013.
2. **Mitra Gilasgar**, Antoni Barlabe, Lluis Pradell , "Highly Efficient Class-F RF Power Amplifiers with Very Low Distortion," *The Radio Science Bulletin*, vol. 347, pp. 21-31, Dec 2013.
3. **Mitra Gilasgar**, Antoni Barlabe, Lluis Pradell , "High Efficiency Reconfigurable Class-F Power Amplifier at 2.4 GHz in CMOS-MEMS Technology," *16th edition of the International Symposium on RF-MEMS and RF-MICROSYSTEMS, MEMSWAVE 2015*, pp. 92-95, June 2015.
4. Paper under review: **Mitra Gilasgar**, Antoni Barlabe, Lluis Pradell , "2.4 GHz Reconfigurable Class-F Power Amplifier Integrated in 0.18μm CMOS Technology," *submitted for publication to IEEE Transactions on Microwave Theory and Techniques*, July 2016.