Universitat Autònoma de Barcelona

Micro and Nano-Electro-Mechanical Devices in the CMOS Back End and Their Applications

Martínn Riverola Borreguero

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Philosophy Doctoral Thesis

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Una tesis doctoral per
Martín Riverola Borreguero

En cumpliment dels requisits per optar al grau de
Doctor en Enginyeria Electrònica i de Telecomunicació

Realitzada sota la direcció de
Prof. Núria Barniol i Beumala

Departament d'Enginyeria Electrònica – Escola d'Enginyeria
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Agraïments

Durant aquest quatre últims anys de completa dedicació a la realització de la tesis doctoral, he conegut a un munt de gent amb els que he compartit conversacions, experiències, i m'han ajudat i recolzat en tots els sentits, tant a la universitat com a casa. A tots ells, voldria dedicar aquesta petit treball, i sobretot, agrair tot el que han fet per mi.

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Martín Riverola, 22 de Setembre de 2017

Resum

RECENTMENT, l'escalat de la tecnologia complementaria metall-òxid-semiconductor (CMOS) està arribant a límits fonamentals, principalment degut a les fuites de corrent no nul·les que el transistor presenta. És per això que s'està investigant una nova branca que va més enllà dels límits de la llei de Moore la qual s'anomena "Més que Moore" i està atraient l'interès per nous dispositius de processat de la informació i memòries, noves tecnologies per integració heterogènia de múltiples funcions, i nous paradigmes d'arquitectures de sistemes. Una d'aquestes tecnologies prometedores per processat de la informació és la tecnologia de relés micro- i nano electromecànica, perquè presenta fuites de corrent pràcticament nul·les i una commutació entre dos estats molt abrupta.

Aquesta tesi proposa explorar les possibilitats d'aprofitar les capes disponibles de la tecnologia CMOS comercial AMS 0.35 μm per implementar relés micro i nano electromecànics. En concret, s'exploren dos conceptes diferents: un són relés actuats en el pla i definits usant solament la capa d'interconnexió anomenada via, i l'altre són relés actuats torsionalment i formats amb metalls i vies (sovint anomenat com compost) a la vegada que suportat per vies. Ambdós conceptes es basen en la capa de tungstè VIA3, la qual inclou característiques claus tals com gran duresa, alt punt de fusió, poc estrès, i gran resistència a l'àcid fluorhídric (HF), ja que les estructures mecàniques s'alliberen mitjançant un procés post-CMOS sense màscares basat en una solució d'HF.

Gràcies a les característiques excepcionals de la plataforma de VIA3, també s'han fabricat ressonadors MEMS basats en l'esmenada plataforma, el que ha permès contribuir al disseny i la caracterització d'un oscil·lador de doble freqüència que consisteix en ressonadors torsionals de tungstè i en un amplificador de transimpedància ultra-compacte, de baix consum i amb un alt guany.

Finalment i paral·lel al principal fil de la tesi, també s'han desenvolupat capacitats commutables en col·laboració amb l'empresa SilTerra Malaysia Sdn. Bhd. Aquests dispositius es caracteritzen per estar totalment integrats en el procés d'una tecnologia comercial CMOS de 180 nm de baix

cost (usant la plataforma SilTerra MEMS-on-CMOS).

Summary

RECENTLY, several new emerging devices are starting to be explored because the traditional down-scaling approach of the complementary metal-oxide-semiconductor (CMOS) technology (often called "More Moore") is reaching fundamental limits; mainly due to non-zero transistor off-state leakage. This brand-new domain that goes beyond the boundaries of Moore's law is commonly named "More than Moore" and is driving interest in new devices for information processing and memory, new technologies for heterogeneous integration of multiple functions, and new paradigms for system architecture. One of these new promising technologies for logic and information processing is the micro- and nanoelectromechanical (M/NEM) relay technology, because of its immeasurably low off-state leakage current and super-steep switching behavior.

This dissertation proposes to explore the possibilities of leveraging the available layers of the commercial CMOS technology AMS 0.35 μm to implement M/NEM relays. Specifically, two different approaches are explored: in-plane actuated relays defined using solely the via layer, and torsional actuated relays formed with metal and via layers (usually named composite) while supported by vias. Both approaches are supported by the tungsten VIA3 layer, which includes key features such as high hardness, high melting point, low stress and resistance to hydrofluoric (HF) acid, since the mechanical structures are released in a maskless post-CMOS process based on a wet HF enchant.

Based on the key structural features that the developed relays showed, MEMS resonators based on the VIA3 platform were also fabricated. In this thesis, we also present a particular contribution involving the design and characterization of a dual-frequency oscillator that consist of such reliable torsional tungsten resonators and a high gain, low power and ultra-compact transimpedance amplifier (TIA).

Finally and parallel to the main thread of this dissertation, RF MEMS switched capacitors are developed as a result of the collaboration with the semiconductor manufacturing enterprise SilTerra Malaysia Sdn. Bhd. These devices has the particularity of being fully integrated into the pro-

cess flow of a low cost, commercial 180 nm CMOS technology (using the SilTerra MEMS-on-CMOS process platform).

Contents

Thesis Presentation

This phD dissertation has been realized in the group Electronics Circuits and Systems (ECAS) of the Department of Electronic Engineering of the Universitat Autònoma de Barcelona. This work has been supervised by Prof. Núria Barniol i Beumala.

Introduction

We are now clearly moving towards a new digital era surrounded by plenty of electronic devices such as smartphones, tablets and laptops that have become a pervasive part of our daily lives. This fact has been possible thanks to the rapid growth of the integrated circuit (IC) technology over the last five decades. The main block contained into these electronic devices with which IC's are built is the planar bulk Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET), which was the precursor of such a rapid technology advancement by steady miniaturization on itself since 1960. It was already in 1965 that, Gordon Earle Moore predicted that the number of transistors on a chip approximately will double every two years [1]. This trend became known as "Moore's Law" and set the pace for innovation.

Fig. 1 show the evolution of transistor gate length scaling-down [2]. As the transistor density has been increased with each new generation of technology due to higher-resolution patterning capability, the transistor functionally has increased and the transistor cost has decreased exponentially over time. This has been possible due to the fact that the number of steps in the microchip fabrication process does not increase proportionately with the transistor density. The first commercially available microprocessor was the Intel 4004. Introduced in 1971, it was comprised of 2'300 transistors operating with a clock frequency of 108 kHz. Today's top-of-the-line microprocessor for consumer products, the Intel Core i9-7900X (2017 edition), has more than 3.2 billion transistors spread over ten processing cores, each operating with a clock frequency of up to 4.3GHz [3].

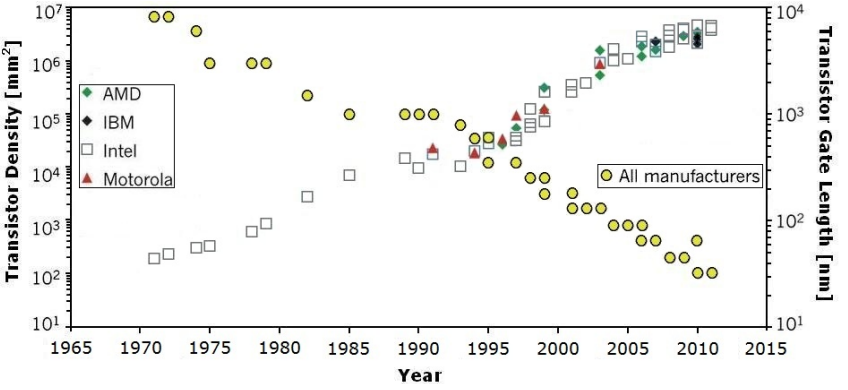


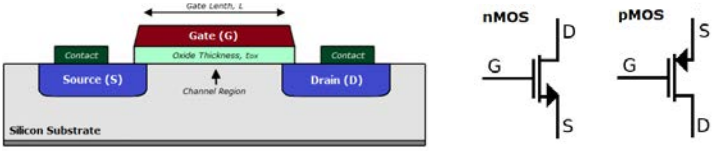
Figure 1: The evolution of transistor gate length (minimum feature size) and the density of transistors in microprocessors over time [2].

Although there is still some "room at the bottom"–talk presented by Richard P. Feynman to the American Physical Society in Pasadena on December 1959, which explores the immense possibilities afforded by miniaturization [4]–to manipulate and control matter at even smaller scales, this fact is becoming increasingly difficult in the deep-submicron region. Lithography for printing sub-wavelength features, short-channel effects, increased static leakage current with voltage threshold reduction, or increased variability in transistor performance are among the new challenges that makes transistor scaling increasingly complex. In order to continue the technology scaling, the use of new materials (low-resistivity conductors as tungsten and copper and high-K dielectrics), new structures and process techniques becomes a necessity [5]. While such series of solutions have so far been able to alleviate these challenges, a power crisis has emerged due to a more fundamental issue inherent in the operating principle of the MOSFET itself.

The CMOS Power Scaling Limit

MOSFET is a four-terminal device with source (S), gate (G), drain (D), and body (B) terminals (Fig. 2(a)). The body of the MOSFET often is connected to the source terminal, making it a three-terminal device (Fig. 2(b)). Basically, MOSFET operation is based on creating a conductive channel between the source and drain applying a voltage sufficiently large (greater than *threshold voltage*, V_T) in the gate terminal. This channel can

contain electrons (called nMOS) or holes (called pMOS), opposite in type to the substrate; so nMOS is made with a p-type substrate and pMOS with an n-type substrate.



(a) (b)

Figure 2: Illustration of (a) the MOSFET structure (b) and nMOS/pMOS circuit symbols.

Complementary metal-oxide-semiconductor (CMOS) transistor technology is predominantly used for digital computing and uses symmetric pairs of p-type and n-type metal oxide semiconductor field effect transistors (MOSFETs) to achieve complementary switching behavior.

When the MOSFET is in the off-state, i.e. when the gate-to-source voltage $V_{GS} < V_T$, a current so-called subthreshold leakage current I_{off} flows between source and drain. This current is an exponential function of the V_{GS} as follows,

$$I_{DS} \equiv I_{off} \approx I_0 \cdot e^{\left(\frac{V_{GS} - V_T}{n\frac{kT}{q}}\right)} \tag{1}$$

where, I_0 is the current when $V_{GS} = V_T$, k is the Boltzamnn constant, T is the temperature in Kelvin, q is the elementary charge and n is the roll-off factor given by,

$$n = 1 + \frac{C_D}{C_{ox}} \tag{2}$$

where, C_D is the depletion capacitance and C_{ox} is the oxide capacitance.

In most digital applications, the presence of subthreshold current is undesirable as it detracts from the ideal switch-like behavior when I_D is plotted on a logarithmic scale vs. V_G as we can see in Fig. 3. We would rather have the current drop as fast as possible once the gate-source voltage falls below V_T. To measure as fast as dropped from V_T to 0, the

subthreshold swing S is defined as,

$$S = \left(\frac{d \log_{10} I_{off}}{dV_{GS}} \right)^{-1} \tag{3}$$

From Eq. 1, we find,

$$S = \left(\frac{d \log_{10} I_{off}}{dV_{GS}} \right)^{-1} = \frac{d}{dV_{GS}} \log_{10} \left(e^{\frac{V_{GS} - V_T}{n \frac{kT}{q}}} \right)^{-1} = \tag{4}$$

$$= \left(\frac{I_0 e^{\frac{V_{GS} - V_T}{n \frac{kT}{q}}} \cdot \left(\frac{1}{n \frac{kT}{q}} \right)}{I_0 e^{\frac{V_{GS} - V_T}{n \frac{kT}{q}}} \ln(10)} \right) = \left(\frac{1}{\ln(10) n \frac{kT}{q}} \right)^{-1} = n \frac{kT}{q} \ln(10)$$

If $n = 1$ (sharpest possible roll-off factor), $T(K) = 300$ K (room temperature), $k = 1.38 \cdot 10^{-23}$ J/K and $q = 1.6 \cdot 10^{-19}$ C, the subthreshold swing S is,

$$S = n \frac{kT}{q} \ln(10) = \tag{5}$$

$$= (1) \cdot \frac{300 \text{ K} \cdot 1,38 \cdot 10^{-23} \text{ J/K}}{1,6 \cdot 10^{-19} \text{ C}} \cdot \ln(10) \approx 60 \,\text{mV/dec}$$

Therefore, using MOSFETs with n-type and p-type source/drain regions to achieve complementary switching behavior (CMOS) in digital applications has a technology limit: the steepest slope possible to achieve (considering n=1) is 60 mV/dec at room temperature. In practice, S is typically 100 mV/dec (with a roll-off factor n=1,67).

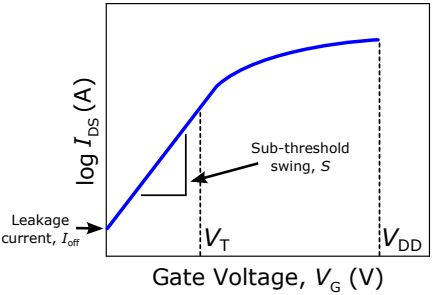
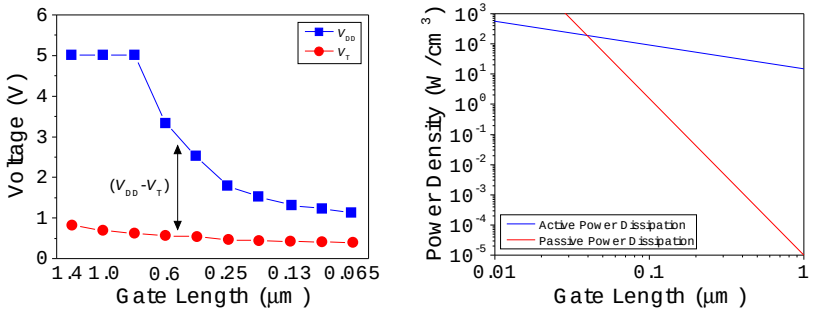


Figure 3: Typical transfer characteristic plot I_{DS} (in logarithmic scale) vs. gate voltage V_G.

Fig. 4(a) shows how the CMOS supply voltage (V_{DD}) and threshold voltage (V_T) have been scaled down in each technology node. As CMOS has been scaled to smaller dimensions, the supply voltage V_{DD} has been reduced to maintain reasonable active power consumption P_{on} (proportional to ${V_{DD}}^2$), and the threshold voltage V_T has needed to be scaled down the same rate as V_{DD} in order to achieve the desired performance [6]. However, the supply voltage is not expected to be further scaled down at 90 nm and below due to the aforementioned nonscaling subthreshold swing S (which is set by the thermal voltage). As a result of this fact, the static power consumption P_{off} increases rapidly becoming the dominant factor in the total power dissipation at small channel lengths as shown in Fig. 4(b), thus threatening the dominance of CMOS technology itself.



(a) (b)

Figure 4: (a) Dynamic and static power densities (W/cm^2) vs. gate length [6]. (b)Plot of V_{GS} and V_T scaling with each technology node [7].

Why Mechanical Switches

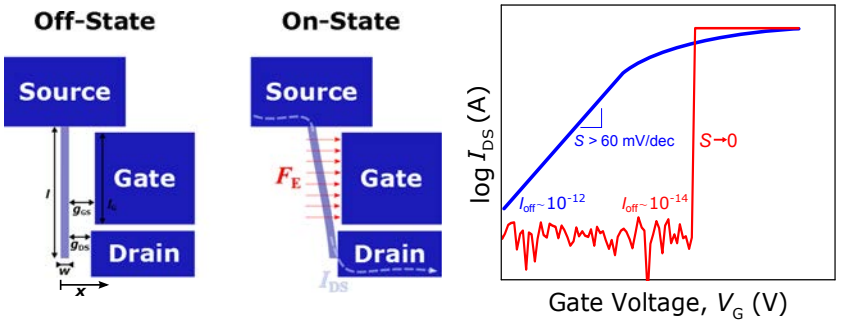
In view of traditional dimensional scaling of CMOS (often called "More Moore") is reaching fundamental limits, several new emerging devices are starting to be explored. This brand-new domain that goes beyond the boundaries of Moore's law is commonly named "More than Moore" and is driving interest in new devices for information processing and memory, new technologies for heterogeneous integration of multiple functions, and new paradigms for system architecture [8]. One of these new emerging technologies for logic and information processing is the micro- and nano-electromechanical (M/NEM) relay technology.

In fact, the use of mechanical switches for computing is not a new idea [9]. One of the first examples is the abacus, a frame with beads sliding on wires, probably invented by Sumerians around 2400 B.C. Later, during the Renaissance (15th-16th century), B. Pascal built the first automatic mechanical computer based on a complex wheel mechanism. Eventually, it reached its zenith when complex machines for cryptographic applications were developed during the World War II. From the 1950s to today, the idea of mechanical computing was considered to be anecdotal. Yet, due to impressive advances in manufacturing techniques and photolithography of bulk-planar processing technology over the past few decades, the interest in the development of surface micromachining processes for micro- and nanoelectromechanical systems (M/NEMS) has been renewed for ultra-low power computing applications [9, 10].

M/NEM relays are usually electrostatically actuated because compared with other types of actuation mechanisms such as piezoelectric or magnetic solutions that require non-standard IC processes and materials, they can be relatively easy to manufacture using conventional planar processing techniques and materials being CMOS compatible [9]. Also, they may be aggressively down-scaled without degrading much the on-off current ratio because the electrostatic forces scale inversely with the square of the gap between the movable element and the actuation electrode [11].

The basic idea behind micro-relays can be understood from Fig. 5(a), which shows an illustration of a generic 3-terminal relay structure actuated electrostatically in the in-plane direction. Analogous to a metal-oxide-semiconductor field-effect transistor (MOSFET) device, the terminals named gate (G), source (S) and drain (D) refer to the actuation electrode, the contact electrode and the mechanical element itself respectively. Initially an air gap separates the movable structure from the contact elec-

trode and thus, no current can flow. As the gate-to-source voltage difference V_{GS} increases, the electrostatic force F_E (due to attraction between oppositely charged electrodes) attracts the movable mechanical element towards the actuation electrode. This force is always attractive regardless of the polarity of the applied voltage (i.e. it is ambipolar), and its strength depends on the area of the electrodes and the separation between them (the actuation gap, g_{GS}). When the movable element is brought into contact with the drain electrode, the relay turns on abruptly with a supersteep (ideally nearly zero) subthreshold swing. Therefore, in contrast to a transistor (as shown in Fig. 5(b)) a mechanical switch exhibits almost zero I_{off} leakage current and supersteep (nearly zero) subthreshold swing S. For this reason, mechanical switches are suitable for ultra-low power applications.



(a) (b)

Figure 5: Schematic illustrations of a generic 3-terminal relay structure in the off-state and the on-state. (b) Typical $I_{DS} - V_{GS}$ characteristic of a relay compared with the typical $I_{DS} - V_{GS}$ of a MOS transistor.

Integration of Mechanical Relays into CMOS Technology

So far, we have seen that there is a fundamental performance limit for CMOS that we will eventually run into. Additionally, with unprecedented market growth in an emerging trend of networked smart objects, or what is now termed the "Internet of Things", low power consumption has increasingly demanded [12]. In this context, an obvious solution is to use the mechanical switch, which can achieve zero leakage current and a very steep switching transition. Even more, hybrid NEM-CMOS systems such

as static random static random access memory [13], relay power gating for CMOS logic [14], mechanical logic circuits [15], and field-programmable gate array (PPGA) [16] applications are already being pursued as a way to maintain or improve CMOS performance while continuing to be scaled down. This fact pushes towards monolithic integration of MEMS switches into CMOS technology, which indeed can provide for improved energy efficiency and enhanced functionality.

There are several approaches for integrating MEMS devices with CMOS electronics in a single chip. The main classification used in relation to the CMOS-MEMS integration is based on the moment in which the MEMS process is performed: 1) pre-CMOS or MEMS-first, 2) Intra-CMOS, 3) post-CMOS or MEMS-last, and 4) post-processing of bak end of line (BEOL) layers. The main advantage of 1) and 2) is that the MEMS fabrication processes are not restricted to the available layers and materials unlike 3) and 4), as long as thermal budget and process compatibility are ensured. By contrast, the use of the inherent layers of the CMOS process as in 3) and 4) offers a vast variety of advantages such as fast turnaround fabrication time, reproducibility, yield, reliable MEMS dimensions definition due to the strict CMOS technology tolerance and good matching with the interfacing circuitry minimizing the parasitic effects and optimizing the signal-to-noise ratio [17]. The section bellow provides a deeper view on the post-processing of CMOS-BEOL layers approach. For further detail related with the other monolithic integration approaches, please refer to [18].

Post-Processing of CMOS-BEOL Layers Approach

The existing BEOL metallization layers of already fabricated CMOS chips can be used as MEMS structural layers using a set of post-processing dry, wet etching and releasing steps that do not affect the CMOS electronics. Several research groups have developed MEMS devices by post-processing such BEOL layers of existing CMOS technologies during the last 30 years.

The first true CMOS-MEMS integration of this genre was reported in 1989 [19]. By stacking via-cuts and omitting the metal layer, openings in the dielectric stack were created which allowed a wet etch to release the microstructures. In 1996, a set of maskless dry-etchings steps to create relatively high aspect ratio beams and gaps were established by G.

K. Fedder [20]. The key of this process relied on the use of the CMOS metallization layers as an etch-resistant mask. This versatile technique led to the development of multiple RF MEMS front-end components such as high-Q inductors [21], resonant mixer-filters [22] and tunable capacitors [23]. Such a technique was adopted and extended by the University of Waterloo which allowed the creation of RF MEMS capacitive switches that can have vertical actuation [24, 25].

Within the framework of CMOS-MEMS resonators, two research groups have carried out an extensive work on developing capacitively-transduced resonators monolithically integrated in standard CMOS technology (both being wet-release-based approaches), paving a technological pathway for the monolithic integration of MEMS resonators with CMOS circuitry. The first one, the National Tsing University of Taiwan (NTHU) approach uses as a platform the CMOS technology TSMC 0.35 μm. By stacking metal and dielectric layers using vias as stack walls, which protect the inner SiO_2 from being attacked by the sacrificial oxide etchant solution, thicker metal-oxide composite resonators are developed [26]. Lately, instead of using the intermetallic dielectric layers as sacrificial layers, dedicated metal layers are etched and electrical routings are protected by oxide structures, achieving in this way oxide-rich metal composite resonators with higher quality factors [27]. The second one, the research group ECAS at the Universtitat Autònoma de Barcelona to which I belong has used as a platform different CMOS techologies: AMS 0.35 μm [28], UMC 0.18 μm [29] and ST 65 nm [30], scaling down the CMOS technological node for reduced dimensions. Our group approach is based on the use of the available conducting layers (metals, vias and polysilicon) as structural layers and the intermetallic dielectric layers as a sacrificial layers. A passivation window and via layers strategically placer over the area of the MEMS structure allows the surrounding SiO_2 to be etched away by using a simple one-step maskless wet etching based on a buffered HF solution.

Back End Embedded Mechanical Relays

To the best of our knowledge, the majority of integrable relays reported in the state of the art can be fabricated directly on top of the CMOS technology following the MEMS-last approach, because indeed they are formed at CMOS-compatible temperatures (i.e. below 400°C) [31–34].

An exception to be highlighted is the Nanomech technology developed by Cavendish Kinetics [35], which employ an intra-CMOS approach for

the fabrication of MEMS switches within a micro-cavity embedded in the CMOS back end metallization layer by using standard CMOS materials, deposition and etching techniques [36].

If one look at how the number of layers used for interconnecting transistors has evolved as CMOS technology nodes have been scaled down over time, it turns out that it has progressively being increased. For instance, there are more than a dozen back end of line (BEOL) layers in the most advanced CMOS manufacturing process reported to date, featuring air gaps incorporated in-between the wires to reduce undesirable capacitive coupling [37]. This trend offers a rich resource for implementing MEMS relays embedded in the available BEOL layers of the standard CMOS technologies by following the post-processing of CMOS-BEOL layers approach.

Nonetheless, none of the previous works has explored the idea of implementing M/NEM relays in such a way. While it is true that the University California at Berkeley has recently proposed a theoretical analysis of how the computational functionality and energy efficiency of microchips can be enhanced by integrating MEM switches in such a way [38, 39], there is no evidence of any experimental demonstration yet. In this sense, initial investigations were lately started on micro- and nano-electromechanical relays following the post-processing of CMOS-BEOL layers approach, which has given rise to part of the work presented in this thesis.

Scope of the Thesis

The objective of this thesis is to explore the possibilities of those available BEOL-CMOS metal layers following the post-processing of BEOL layers approach for the development of contact micro- and nano-electromechanical relays. The know-how acquired in the integration of MEMS resonators into CMOS technologies by the ECAS group during the last years has been taken as a starting point to the work developed in this phD thesis. For this reason, the AMS 0.35 μm CMOS technology has been utilized for such purpose. The specific objectives of this thesis and their implications are:

- **Design and Fabrication:** Design and fabrication of micro- and nano-electromechanical relays using as a platform the commercial AMS 0.35 μm CMOS technology. In this step, a profound knowledge of the CMOS technology is primarily to succeed in the implementation. The selection of the available layers which will constitute the relay structure is also critical and have their individual

constraints. Thus, the selection and evaluation of available materials are discussed. Challenges encountered are addressed by material optimization and design improvements.

- **Measurement:** Characterization of fabricated micro- and nano-electromechanical relays. This implies releasing, physical characterization and the electrical characterization of fabricated structures.

- **Investigation of the properties of fabricated devices:** Study of the characteristics of the fabricated micro- and nano-electromechanical relays from the characterization results.

- **Investigation of the potential applications:** This step proposes potential applications for the developed beol-embedded micro- and nano-electromechanical relays based on the obtained results.

Research Framework

The present thesis has been performed under the framework of the two following national projects:

- "NEMS-in-CMOS" Dispositivos Nanoelectromecanicos (NEMS) Integrados en CMOS: Exploración de las Propiedades no Lineales de los Resonadores NEMS en Aplicaciones Lógicas y Sensores.
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- "CMOS-MENUTS" Sistemas CMOS-MEMS/NEMS Resonantes para Sensado Inteligente y Nuevos Transductores de Ultrasonidos.
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In addition, the research group ECAS to which I belong maintains a collaboration contract with the semiconductor manufacturing enterprise SilTerra Malaysia Sdn. Bhd. As a result of this collaboration, I was also involved during the pHD in a project with the aim of developing tunable MEMS capacitors using the SilTerra MEMS-on-CMOS platform.

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Thesis Outline

The present document consist of 5 chapters and 3 appendices:

Chapter 1 is devoted to introducing the basic modeling and design considerations of micro- and nano-electromechanical relays. An overview of the basic structure and operation is first reviewed in detail. The dynamic behavior is then studied with a focus on the relay switching time. Next, a brief description of how to design and model mechanical flexural and torsional beams is presented. Finally, the last part deals with a basic theoretical description of the physics behind the relay contact.

Chapter 2 starts with a description of the CMOS-MEMS fabrication approach giving to the reader a general view of the actual state of the art. Next, the fabrication process for developing M/NEM relays is described in detail, endowing the reader with the necessary tools for the design of either vertical or torsional relays using the available layers of the standard CMOS technology AMS 0.35 μm.

Next two **Chapter 3** and **Chapter 4** are entirely dedicated to the description of the experimental results. Two different approaches were followed: the laterally-actuated nanoelectromechanical (NEM) relays based on tungsten VIA3 layer is presented in Chapter 3, and the torsional composite microelectromechanical relays based on the MET4-VIA-MET3 stack is presented in Chapter 4.

As a result of the collaboration with SilTerra Malaysia Sdn. Bhd., **Chapter 5** is exclusively devoted to present the design and experimental results of developed MEMS switched capacitors fabricated with the SilTerra MEMS-on-CMOS platform. The motivation and objectives of this collaboration are first stated in order to put the reader in context.

To finalize, some general conclusions intend to recapitulate the contributions of the present thesis as well as to offer some suggestions for future research. Additionally, this document includes two appendices:

Appendix A includes the description of each IC RUN designed during the development of the thesis.

Appendix B contains a list of peer-reviewed publications and contributions to scientific conferences that are result of this thesis.

Chapter 1

Design and Modeling of Micro- and Nano-electromechanical Relays

Chapter 1 deals with the design and basic modeling of micro- and nano-electromechanical relays with the objective to serve as a basis for the measurement and study of these devices. An overview of the basic structure and operation is first reviewed in detail. The dynamic behavior is then studied with a focus on the relay switching time. Next, the mechanical element, which is the active element of the relay is analyzed with a brief description of how to design and model mechanical flexural and torsional beams. It is of paramount importance an understanding of contact mechanics in order for the contact resistance of micro-relays to be predicted. Thus, we shall then review how the contact material deforms, which will help to determine the effective contact area and based on this, what is the resulting contact resistance related to that effective contact area. Finally, different relay configurations and potential applications are identified.

1.1 Basic Relay Structure and Operation

For the sake of simplicity, let us first consider a two-terminal (2-T) architecture (Fig. 1.1(a)) for the analysis of the basic operation principle of mechanical relays. As its name indicates, the 2-T relay structure is composed of two elements: (i) an active element source and (ii) a common single gate/drain electrode.

Fig. 1.1(c) shows the typical $I_{DS} - V_{GS}$ characteristic curve of a 2-T relay. In the off-state, e.g., when zero gate-to-source voltage difference V_{GS} is applied, an air gap g separates the movable structure from the contact electrode so that no leakage current can flow between them.

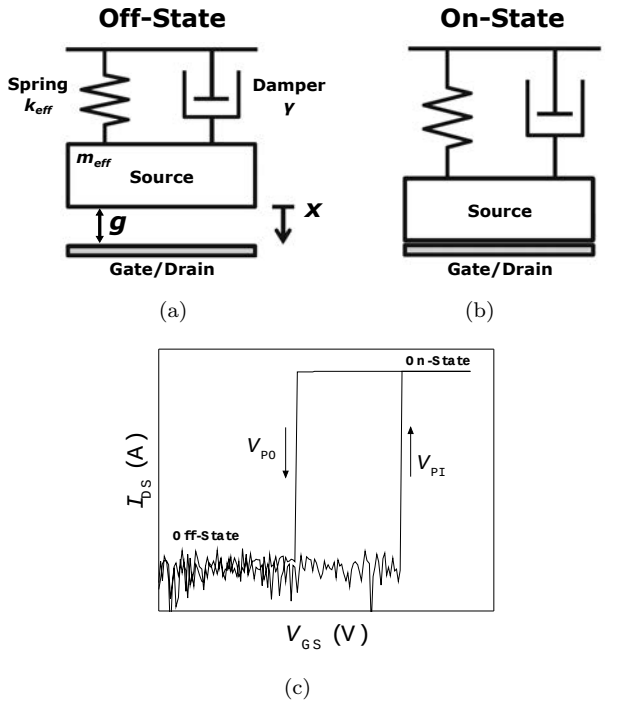


Figure 1.1: Schematic of a micro-relay based on a 2-terminal configuration in (a) off-state and (b) on-state. (c) $I_{DS} - V_{GS}$ characteristic curve of a micro-relay that commutes between the on- and off-state as the pull-in V_{PI} and pull-out V_{PO} event occurs.

When a positive V_{GS} voltage is applied, an electrostatic force pulls the active element towards the actuation (or gate/drain) electrode. Based on the stored energy in the parallel-plate capacitor formed between the source and the gate/drain electrode, one can derive the electrostatic force F_E acting on the plate (or active element) as

$$F_E = \frac{1}{2}\frac{dC_{GS}(x)}{dx}{V_{GS}}^2 = \frac{1}{2}\epsilon_0 A {V_{GS}}^2 \frac{d}{dx}\frac{1}{g-x} = \frac{1}{2}\frac{\epsilon_0 A {V_{GS}}^2}{(g-x)^2} \tag{1.1}$$

where A is the actuation area, ϵ_0 is the vacuum permittivity, g is the air-gap separation, and x is the displacement of the active element.

In static equilibrium, the total force acting on the mechanical structure is canceled out ($F_{total} = 0$). So, by balancing the F_E and the spring

restoring force F_k, the equilibrium position can be thus derived

$$k_{eff}x = \frac{1}{2}\frac{\epsilon_0 A {V_{GS}}^2}{(g-x)^2} \tag{1.2}$$

where k_{eff} is the effective spring constant of the active element.

Fig. 1.2 shows the force versus normalized tip displacement characteristics for both electrostatic and spring restoring force. As evidenced from Eq. 1.2, the electrostatic force increases quadratically whereas the spring restoring force increases linearly with decreasing x-position. At low V_{GS}, there exists two solutions for x, but only the one indicated with a circle symbol is a stable position. Then, it exists a maximum V_{GS} voltage beyond which the electrostatic force is always larger than the spring restoring force, and the movable structure becomes unstable. This results in the well-known pull-in phenomenon, wherein the gap closes abruptly as the actuation voltage increases beyond a critical pull-in voltage, V_{PI}. In order to solve the pull-in voltage V_{PI} and critical pull-in displacement x_{PI}, let us to rewrite Eq. 1.2 as

$$V_{GS} = \sqrt{\frac{2k_{eff}x}{\frac{dC_{GS}(x)}{dx}}} = \sqrt{\frac{2k_{eff}x(g-x)^2}{\epsilon_0 A}} \tag{1.3}$$

Plotting the solution of Eq. 1.3 by linking V_{GS} to the plate displacement yields a concave curve as shown in Fig. 1.3. The absolute maximum of the function indicates both the V_{PI} and the x_{PI} given by

$$x_{PI} = 0.33\,g \quad \text{and} \quad V_{PI} = \sqrt{\frac{8}{27}\frac{k_{eff}g^3}{\epsilon A}} \tag{1.4}$$

When considering a cantilever as the active element, the approximation of the parallel plate capacitor is no longer valid. By assuming that the cantilever relay sustains a linear deformation shape, one can derive an approximate solution of the capacitance between the beam and the actuation electrode as [40]

$$C_{GS}(x) = \frac{\epsilon_0 A}{x}\ln\left|\frac{g_{GS}}{g-x}\right| \tag{1.5}$$

where A and g are the area and air-gap separation between the beam and the actuation electrode respectively, and x is the displacement of the beam.

By linking the applied voltage V_{GS} to the beam displacement tip as previously done in Eq. 1.3, it turns out that the critical displacement x_{PI} and the pull-in voltage V_{PI} for a cantilever beam is

$$x_{PI} = 0.44\,g \quad \text{and} \quad V_{PI} = \sqrt{\frac{22}{25}\frac{k_{eff}g^3}{\epsilon A}} \tag{1.6}$$

which exceeds the $0.33\,g$ of the parallel-capacitor approximation.

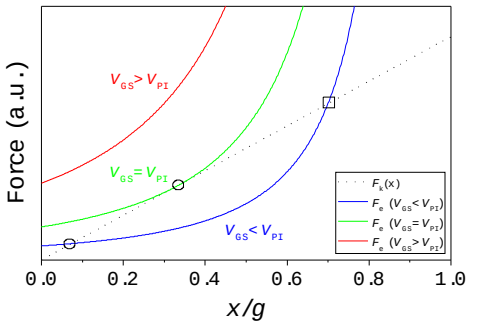


Figure 1.2: Force versus normalized-displacement (z/g) characteristics of spring restoring force (F_k) and electrostatic force (F_E) with $V_{GS} < V_{PI}$, $V_{GS} = V_{PI}$, and $V_{GS} > V_{PI}$. Circle symbols indicate stable states and square symbol indicates a non-stable state.

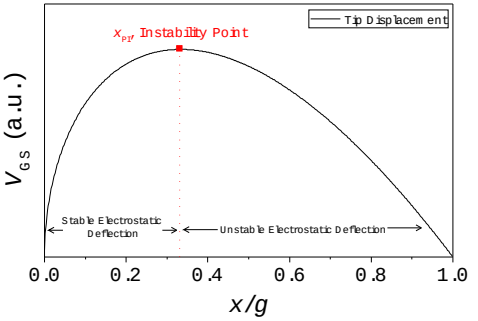


Figure 1.3: Applied V_{GS} voltage versus normalized displacement over the air-gap separation g. V_{PI} is extracted from the absolute maximum of the function.

Once in the on-state (see Fig. 1.1(b), although the V_{GS} voltage is reduced back to 0 V, the switch remains stuck due to the adhesion forces F_A (mainly van der Waals forces predominate [41]) acting on the contacting region and does not return to its off-state position until it reaches the pull-

out voltage V_{PO}, which occurs when F_k overcomes F_E plus F_A. In this way, the typical I-V response describes a hysteretic behavior as shown the experimental measurement plotted in Fig. 1.1(c).

It is important to highlight that there are devices designed such that F_k is not big enough to overcome F_A and thus, the relay remains stuck even after the driving voltage is turned off. These devices are known to operate in a non-volatile mode compared to its volatile counterpart, which indeed recover its off-state position [10].

Let us now introduce an expanded relay architecture (3-terminal) which utilizes an actuation electrode (gate) to bring the relay (source) into contact with an independent readout electrode (drain) as shown in Fig. 1.4(a). In this way, the voltage difference between the gate and source terminals can be high without affecting the current flowing through the contact since it is determined by the drain-to-source voltage difference.

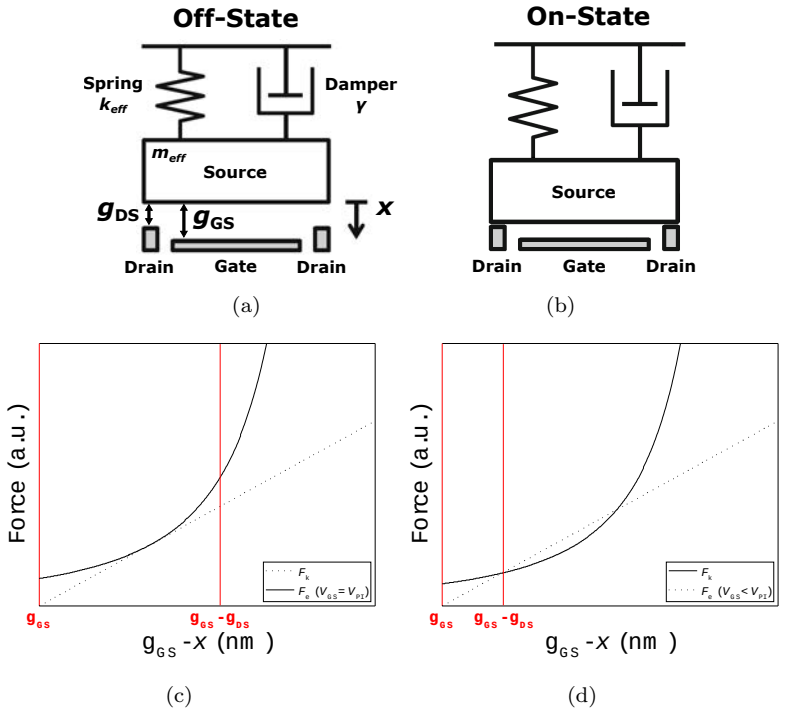


Figure 1.4: Schematic of a micro-relay based on a 3-T configuration in (a) off-state and (b) on-state. Force vs. x-position curves for (c) a relay designed for non-pull-in mode operation, and (d) a relay designed for pull-in-mode operation.

The switch turns on when the drain-to-source gap g_{DS} closes and the beam touches the drain electrode, as illustrated in Fig. 1.4(b). The g_{DS} thereby limits the maximum displacement of the relay. So, it will be said that the relay is pulled in provided that $g_{DS} > x_{PI}$ (see Fig 1.4(c) for reference). Instead, if $g_{DS} < x_{PI}$, then F_E does not overtake F_k before the x-position decreases to g_{GS}-g_{DS} and the relay is said to operate in non-pull-in mode (see Fig 1.4(d)).

The hysteresis voltage (V_{PI}–V_{PO}) depends on the relative sizes of contact gap (g_{DS}) and actuation gap (g_{GS}) [41], as explained with the aid of Fig. 1.4. If g_{DS} is designed such that the relay is operated in non-pull-in mode (less than $g_{GS}/3$), then F_E does not overtake F_k before the x-position decreases to g_{GS}-g_{DS}; in other words, at V_{GS}=V_{PI} $\rightarrow$ F_E=F_k so that V_{GS} only needs to be reduced slightly to reduce F_E by F_A in order to turn off the relay. Then, the pull-out voltage is given by

$$V_{NPI} = \sqrt{\frac{2k_{eff}g_{DS}(g_{GS} - g_{DS})^2}{\epsilon_0 A}} \tag{1.7}$$

In contrast, if g_{DS} is designed such that the relay is operated in pull-in mode (greater than $g_{GS}/3$), F_E exceeds F_k when the relay is on (and the relay is said to be "pulled in"), so that F_E needs to be reduced by more than F_A to turn off the relay. Therefore, the hysteresis voltage is larger for a relay designed to operate in pull-in mode, and the pull-out voltage is given by

$$V_{PO} = \sqrt{\frac{2k_{eff}g_{DS}(g_{GS} - F_A)(g_{GS} - g_{DS})^2}{\epsilon_0 A}} \tag{1.8}$$

Finally, it is important to note that since electrostatic attractive force is ambipolar, a relay can be turned on either by applying a positive or negative V_{GS} voltage.

1.2 Dynamic Behavior and Switching Time

In addition to the static voltages, an important dynamic parameter that should be taken into account is the mechanical switching time. As a first order approximation, one can use the spring-mass-damper model depicted in Fig 1.1(a) to estimate the mechanical switching time. When a bias

voltage is applied between the actuation electrode (gate) and the movable structure (source), the motion of the actuation plate is governed by Newton's Second Law of Motion, which yields the following second-order differential equation

$$m\frac{d^2x}{dt} + \gamma\frac{dx}{dt} + kx = F_e = \frac{1}{2}\frac{\epsilon_0 A}{(g-x)^2}{V_{GS}}^2 \tag{1.9}$$

where,

k,	is the spring constant,
x,	is the displacement,
m,	is the effective mass,
F_e	is the applied electrostatic force and
γ,	is the damping coefficient defined as $\gamma = \frac{k}{\omega_0 Q}$

being $\omega_0 = \sqrt{k/m}$ the resonant frequency in radiants (i.e. $\omega_0 = 2\pi\, f_0$) and Q a dimensionless parameter known as quality factor that describes how underdamped is the system under consideration and it will be analyzed with further detail in next subsection.

Owing to switch inertia, the switch moves initially slowly and it spends the majority of the time reaching the half-way point. Later, the final half of the gap the damping limits the switch velocity. So, a good general approximation for the mechanical switching time is obtained by summing the inertial and damping limited switching times given by [42]

$$t_s = t_m + t_\gamma \tag{1.10}$$

where t_m is the inertia limited switching time given by

$$t_m = \sqrt{\frac{27}{32}}\frac{\pi}{\omega_0}\frac{V_{PI}}{V_{GS}} \tag{1.11}$$

and t_γ is the damping limited switching time that can be written as

$$t_\gamma = \frac{{V_{PI}}^2}{Q\omega_0 {V_{GS}}^2}\left(2.25 + 1.52\frac{{V_{PI}}^2}{{V_{GS}}^2} + 1.22\frac{{V_{PI}}^4}{{V_{GS}}^4}\right) \tag{1.12}$$

Fig. 1.5 shows the plot of the solution of Eq. 1.10 as a function of the

Q-factor, taking $V_{PI} = 8$ V, $V_{GS} = 1.5V_{PI}$ and f_0=223 kHz from [43]. As it can be clearly seen, the optimal operation regime is $0.5 < Q < 2$ in order to have a short settling time after the pull-out, as well as an optimal tip bouncing behavior after the pull-in. For lower quality factors $Q < 0.5$, the damping significantly increases the switching time, which results in a slow switching time whereas a $Q > 2$ results in a long settling time when the switch is released.

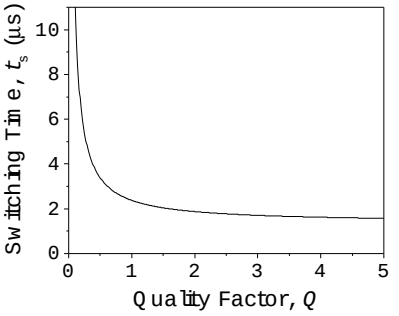


Figure 1.5: Calculated t_s as a funtion of the Q-factor using the values of the switch from [43].

Once the contact is established, a certain time t_{RC} or RC delay associated with charging the capacitance C_L of the output node through the load resistor R_L is added to the total contribution of the relay switching time. Let us now derive the t_{RC} with the aid of the equivalent electrical schematic shown in Fig. 1.6, which is basically comprised of a switch with a series resistance that models the M/NEM relay of which an output RC circuit is hanging in parallel.

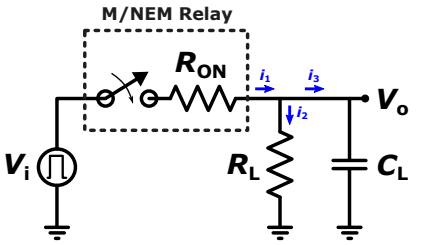


Figure 1.6: Schematic of the equivalent circuit used for the derivation of the RC time constant.

When the switch closes, by applying the Kirchhoff's current law (KCL)

at the center "tee" node, the currents i_1, i_2 and i_3 are related as

$$i_1 = i_2 + i_3 \tag{1.13}$$

From the Ohm's law, i.e. $i{=}V/R$, we can express Eq. 1.13 as a funtion of the input V_i and output V_o voltage as

$$\frac{V_i - V_o}{R_{ON}} = \frac{V_o}{R_L} + C_L \frac{dV_o}{dt} \tag{1.14}$$

By rearranging, we can get then

$$\frac{R_L}{R_{ON} + R_L} V_i = V_o + \frac{R_{ON} R_L}{R_{ON} + R_L} C_L \frac{dV_o}{dt} \tag{1.15}$$

Eq. 1.15 is a first order differential equation, whose solution can be written as

$$V_o = \frac{R_L}{R_{ON} + R_L} V_i \left\{ 1 - \exp\left(\frac{-t}{\frac{R_{ON} R_L}{R_{ON} + R_L} C_L} \right) \right\} \tag{1.16}$$

where the RC time constant, which is the time required to charge the capacitor C_L, through the equivalent resistor R_{eq}, by $\sim 63.2\%$ of the difference between the initial value and final value, can be straightforwardly identified as

$$t_{RC} = R_{eq} C_L = (R_{ON} || R_L) \cdot C_L = \frac{R_{ON} R_L}{R_{ON} + R_L} C_L \tag{1.17}$$

and it is related to the cutoff frequency f_c as

$$f_c = \frac{1}{2\pi R_{eq} C_L} \tag{1.18}$$

where resistance in ohms (Ω) and capacitance in farads (F) yields the time constant in seconds or the frequency in Hz.

1.2.1 Damping Mechanisms

The quality factor Q is a dimensionless parameter that describes how underdamped is the system under consideration and it can be defined as

$$Q = \frac{\text{Total Energy Stored}}{\text{Energy Dissipated per Cycle}} \times 2\pi \tag{1.19}$$

The quality factor of a system is determined via several dissipation mechanisms such as air-squeezing, anchor losses, surface contribution and thermoelastic damping (TED). We can write the total quality factor as the sum of all these dissipation mechanisms as [44]

$$\frac{1}{Q} = \frac{1}{Q_{air-squeezing}} + \frac{1}{Q_{anchor}} + \frac{1}{Q_{surface}} + \frac{1}{Q_{TED}} \tag{1.20}$$

so that the total Q-factor contribution is dominated by the smallest Q-factor component.

Most of the damping in relays which employ micron-scale actuation gaps, Q is limited by squeeze-film damping [45], coming from the air gas underneath the movable structure which experiment several collisions. Yet, if the relay is operated under vacuum conditions, the damping is dominated by internal friction (bulk and surface effects) and support or clamping loss [44].

Let us now define two parameters.

The **mean-free path** is the distance covered by a molecule in a gas between successive collisions and is given by [46]

$$\lambda = \frac{1}{\sqrt{2}\pi N \sigma^2} \frac{\rho}{m_0} \tag{1.21}$$

where, σ is the diameter of the gas molecule, ρ is the gas density in kg/m^3 and m_0 is the mass of a single molecule.

The **Knudsen number** is a dimensionless number defined as the ratio of the molecular mean free path length λ to a representative physical length scale, which is in this case the gap height g of a MEMS beam and is given

by [46]

$$K_n = \frac{\lambda}{g} \tag{1.22}$$

If the Knudsen number is small, it means that there are many collisions in the gap and that the gas (or fluid) is viscous. When the gap height is on the order of the mean free path (near or slightly greater than one), particle-wall interactions become important, reducing the flow resistance or viscosity, through a *slip effect* where particles can have fewer interactions before escaping.

Thus, the quality factor of nanometer-scale relays with actuation gaps smaller than the mean free path of an air molecule (i.e. 68 nm [47]) will be dominated by surface-related energy-loss mechanisms and not by squeeze-film damping which will be negligible.

1.3 Design and Modeling of Mechanical Flexural Beams

Simply structures such as cantilever (also known as clamped-clamped beam) or bridge (also known as clamped-clamped beam) structures are commonly used as springs in MEMS systems. Fig. 1.7 shows a illustration of the deflection from its rest position of a clamped-free and a clamped-clamped beam to which an external point force F is being applied. The Hooke's law describes a linear dependence between the force F with the defection of the beam z. Thus, one can define the spring constant k_{eff} as $k_{eff} \equiv F/z_{max}$.

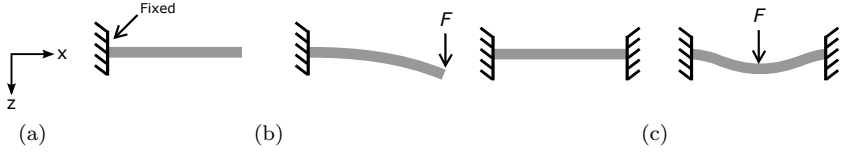


Figure 1.7: (a) Axis and sign convention. Fixed point is defined as the origin (0,0). Beam deflection of (a) a clamped-free beam and (b) a clamped-clamped beam with a point load F.

To find the z-displacement, we first note that the shape of the beam

deflection can be found by solving the beam equation [48]

$$EI\frac{d^2z}{dx^2} = -M(x) \tag{1.23}$$

where E is the Young's modulus of the beam material, which is concerning with the material elasticity, I is the moment of inertia that for a rectangular cross-section beam is

$$I = \frac{w^3 t}{12} \tag{1.24}$$

and $M(x)$ is the bending moment at position x.

Considering that a punctual point force perpendicular to the cantilever beam is acting on the free end at position $x = l$, the bending moment $M(x)$ is given by

$$M(x) = -F(l - x) \tag{1.25}$$

where the boundary conditions for a cantilever beam impose that the displacement and the velocity in the fixed end must be zero

$$z(0) = 0 \tag{1.26}$$

$$\left(\frac{dz}{dx}\right)_{x=0} = 0 \tag{1.27}$$

By integrating twice Eq. 1.23 and applying the above boundary conditions to the integrating constants obtained in each of the integrals, the displacement for a cantilever is then given by

$$z(x) = \frac{F}{6EI}(3lx^2 - x^3) \tag{1.28}$$

so that Eq. 1.28 at the tip end ($x = l$) which gives z_{max} combined with the Hooke's law as previously stated, results in the spring constant of a cantilever beam k_{cfb} given by

$$k_{cfb} = \frac{3EI}{l^3} = \frac{Etw^3}{4l^3} \tag{1.29}$$

Same procedure can be followed for a clamped-clamped beam, in which imposing that the displacement and velocity in both ends are zero and considering the moment M(x) of Eq. 1.30, the displacement for a bridge is obtained as given by Eq. 1.31

$$M(x) = \begin{cases} -\dfrac{Fl}{8} + \dfrac{Fx}{2} & 0 < x < l/2 \\ \dfrac{3Fl}{8} - \dfrac{Fx}{2} & 0 < x < l/2 \end{cases} \tag{1.30}$$

$$z(x) = \begin{cases} \dfrac{F}{EI}\left(\dfrac{x^3}{12} - \dfrac{x^2 l}{16}\right) & 0 < x < l/2 \\ \dfrac{F}{EI}\left[\dfrac{x^3}{12} - \dfrac{x^2 l}{16} - \left(x - \dfrac{l}{2}\right)^3\right] & l/2 < x < l \end{cases} \tag{1.31}$$

Thus, the maximum displacement z_{max} which is given by Eq. 1.28 at $x = l/2$ combined with the Hooke's law results in the clamped-clamped beam spring constant k_{ccb} given by

$$k_{ccb} = \frac{192EI}{l^3} = \frac{16Etw^3}{l^3} \tag{1.32}$$

1.4 Design and Modeling of Mechanical Torsional Beams

In addition to the mechanical flexures beams, torsional spring designs are also very attractive for implementing micro-relays [49]. Fig. 1.8 shows a schematic 3D view of a torsional structure which consist of one main beam anchored by two torsion beams, which allow the end of the main beam to move up and down by electrostatic actuation with the aid of the underneath driving electrode.

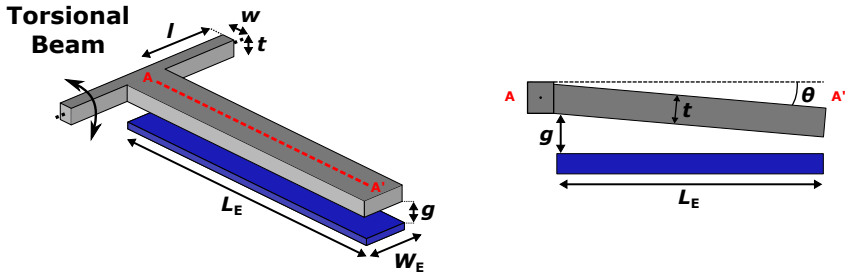


Figure 1.8: Schematic 3D and cross-sectional view of a torsional relay with indication of the key design parameters.

In general, the torque T_θ of a torsional beam with rectangular cross-section is given by [50]

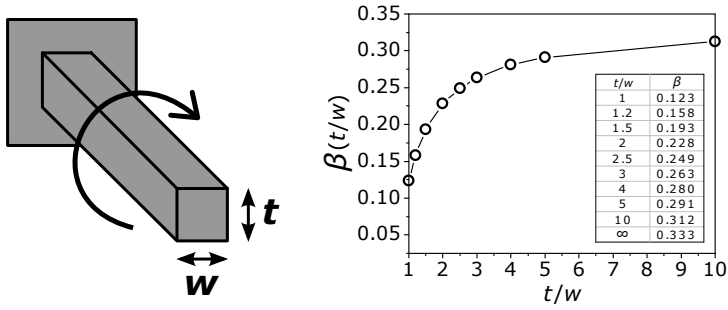
$$T_\theta = k_T \cdot \theta \tag{1.33}$$

where k_T is the torsional spring constant in N·m/rad, and θ is the rotation angle that the beam makes as it rotates. The torsional spring stiffness for the structure in Fig. 1.8 which comprises two springs in parallel is given by

$$k_T = 2\beta G \frac{tw^3}{l} \tag{1.34}$$

where $G = E/2(1-\nu)$ is the shear modulus, ν is the Poisson's ratio, and β is a function that depends on the aspect ratio t/w and is given by

$$\beta = \frac{1}{3} - 0.21 \left(\frac{w}{t}\left(1 - \frac{w^4}{12t^4}\right) \right) \tag{1.35}$$



(a) (b)

Figure 1.9: (a) Solid rectangular section of thickness t and width w under torsional stress, being $t \geq w$. (b) β-function that depends on the aspect ratio t/w [50].

The electrostatic torque applied on the beam about y axis can be computed by integrating the incremental torque over the actuation plate as [51]

$$T_\theta = \int_0^{L_E} \frac{\epsilon_0 W_E {V_{GS}}^2 y}{(g-\theta y)^2} dy = \\ = \frac{\epsilon_0 W_E {V_{GS}}^2}{\theta^2} \left[\frac{\theta L_E}{g - \theta L_E} + \ln\left(1 - \frac{\theta L_E}{g}\right) \right] \tag{1.36}$$

where W_E and L_E are the width and length of the actuation area $A = W_E \times L_E$ (see Fig. 1.8).

In static equilibrium, the torsional mechanical torque is equal to the electrostatic torque

$$k_T \theta = \frac{\epsilon_0 W_E {V_{GS}}^2}{\theta^2} \left[\frac{\theta L_E}{g - \theta L_E} + \ln\left(1 - \frac{\theta L_E}{g}\right) \right] \tag{1.37}$$

Analogous to the derivation of the pull-in displacement for mechanical beams, the pull-in angle θ_{PI} for torsional structures can be derived by

differentiating Eq. 1.37 with respect to θ as given in Eq. 1.38

$$k_\theta = \frac{\epsilon_0 W_E {V_{GS}}^2}{{\theta_{PI}}^2}\left[\frac{gL_E}{(g-\theta_{PI}L_E)^2} - \frac{\frac{L_E}{g}}{1-(\frac{\theta_{PI}L_E}{g})}\right] + \left[\frac{\theta_{PI}L_E}{g-\theta_{PI}L_E} + \ln\left(1-\frac{\theta_{PI}L_E}{g}\right)\right]\left(\frac{-2\epsilon_0 W_E {V_{GS}}^2}{{\theta_{PI}}^2}\right) \tag{1.38}$$

and substituting Eq. 1.37 into Eq. 1.38, the angle of rotaition at which the torsional beam is pulled in can be obtained

$$\theta_{PI} = 0.446\,\frac{g}{L_E} \tag{1.39}$$

Thus, substituting Eq. 1.39 into Eq. 1.37, the torsional pull-in voltage can be found

$$V_{PI} = \sqrt{0.414\left(\frac{k_T}{{L_E}^2}\right)\frac{g^3}{\epsilon_0 A}} \tag{1.40}$$

For example, for a tungsten (G=162 GPa) torsional beam with t=1 μm, w=0.5 μm and l=3.5 μm, the calculated k_T is X N·m/rad and for g=1 μm, and $L_E = W_E$ =10 μm, the V_{PI} results in X V.

1.5 Contact Resistance

An understanding of contact mechanics is necessary to design ohmic contacting switches in order for the contact resistance created through the relay contact to be predicted. For such a purpose, two primary considerations have to be considered. First, when two surfaces are pressed together, a model to the study how the deformation of solids is being subjected is required. Knowing that, the second step is to determine the effective contact area based on the deformation model under consideration, which leads to determine the relay contact resistance.

1.5.1 Contact Resistance and Electron Transport

When the relay is turned on, a resistive path is created through the relay contact, which is largely limited by the contact resistance R_C at the contacting regions. Due to surface roughness, only a small fraction of the apparent area is in physical contact across multiples asperities of radius a. Thus, current flow through these circular narrow micro-contact asperities as shown in Fig. 1.10.

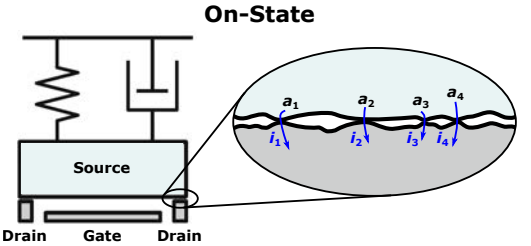


Figure 1.10: A resistive path is created through the relay contact, which is largely limited by the contact resistance R_C at the contacting regions.

The electrical contact resistance (ECR) at each microcontact spot of radius a (contact radius), between two materials of resistivity ρ is given by

$$R_C = R_H + \gamma R_{SH} \tag{1.41}$$

where R_H is the Holm constriction resistance in the diffusive regime (see Fig. 1.11(a))in which the radius of the asperity a is much larger than the mean free path of electron λ ($a >> \lambda$), and it can be modeled analytically as [52]

$$R_H = \frac{\rho}{2a} \tag{1.42}$$

If the asperity radius a is much smaller compared to the electron mean free path λ ($a << \lambda$) of the material, which occurs in ultra-scaled relay technology [11], the resistance of the contact spot is dominated by the Sharvin's mechanism in which the electrons are projected ballistically through the contact spot (see Fig. 1.11(a)). The resulting contact resis-

tance is derived in [53]

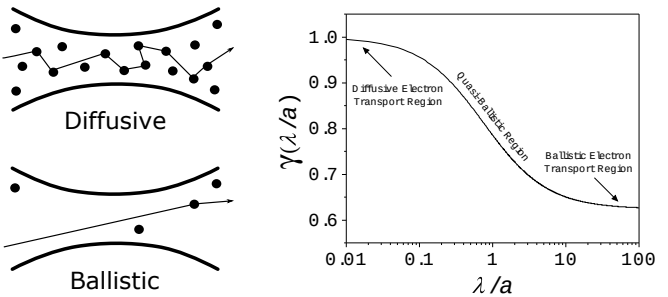
$$R_{SH} = \frac{4\rho\lambda}{3\pi r^2} \tag{1.43}$$

Finally, the γ-function is a fitting function [54] for transitioning between ballistic and diffusive transport regions in which $\lambda \sim a$

$$\gamma = \frac{1 + 0.83\lambda/a}{1 + 1.33\lambda/a} \tag{1.44}$$

and it is shown in Fig. 1.11(b); it depicts complete diffusive transport ($\gamma \approx 1$) for small λ/a ratio ($\lambda/a < 0.02$) and approximately 68.3% ballistic transport for large λ/a ratio ($\lambda/a > 7.0$).

Therefore, based on the size of the effective conducting area and how it compares with the mean free path of an electron, current flow is described as being ballistic, quasi-ballistic, or diffusive [55].



(a) (b)

Figure 1.11: (a) Schemtaic illustration of diffusive and ballistic electron transport in a conductor. (b) The dependence of γ-function in Eq. 1.44 on the ratio λ/a [54].

1.5.2 Material Deformation Models

Determining the nature of the contact area at the interface necessitates a model of the surface profile of the contact between the movable structure and the contact electrode. The surface profile between each asperity across the rough surface can be modeled as two colliding spheres of radius R_1 and R_2 as we can see in Fig. 1.12.

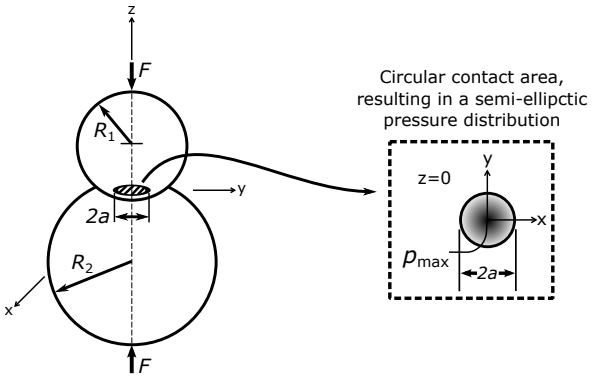


Figure 1.12: Contact between two colliding spheres of radius R_1 and R_2.

1) *Elastic*: When two spheres are initially brought into contact with a low force F, surface asperities (i.e., a-spots) undergo elastic deformation. The contact area A and contact force F_{C_E} under elastic deformation are given by [56]

$$A = \pi R \alpha \tag{1.45}$$

$$F_{C_E} = (4/3) E^* \alpha \sqrt{R\alpha} \tag{1.46}$$

where α is the vertical deformation; R and E^* are the effective radius and effective modulus of elasticity respectively given by

$$\frac{1}{R} = \frac{1}{R_1} + \frac{1}{R_2} \tag{1.47}$$

$$\frac{1}{E^*} = \frac{1 - {\nu_1}^2}{E_1} + \frac{1 - {\nu_2}^2}{E_2} \tag{1.48}$$

where E_1 and E_2 are the elastic Young modulus and v_1 and v_2 are the Poisson's ratio associated to each sphere respectively.

For a circular area, i.e. $A = \pi a^2$, Eq. 1.45 and 1.46 are related to the radius of the asperity a as [56]

$$a = \left(\frac{3FR}{4E^*} \right)^{1/3} \tag{1.49}$$

When the applied load is increased to approximately three times the

yield point (Y) at which the plastic deformation starts to occur, material deformation is no longer reversible and ideal plastic material deformation begins [52]

2) *Plastic*: To account for the asperity contact area and force under plastic deformation, the well known model from Abbot and Firestone that assumes sufficiently large contact pressure and no material creep is used [57]. Single asperity contact area A and contact force F_{C_P} under plastic deformation are given by [57]

$$A = 2\pi R\alpha \tag{1.50}$$

$$F_{C_P} = HA \tag{1.51}$$

where H is the hardness of the softer material.

By using Eq. 1.51 and considering a circular contact area, the asperity radius can be expressed as

$$a = \sqrt{\frac{F_{C_P}}{H\pi}} \tag{1.52}$$

3) *Elastic-Plastic*: An updated elastic-plastic contact model with a linear interpolation introduced by Chang *et al.* [58] is suitable for plastically deformed asperities from the onset of plastic deformation to a fully plastic contact. Based on their model, the contact area A and the contact force $F_{C_{EP}}$ for a plastically deformed asperity are

$$A = \pi R\alpha\left(2 - \frac{\alpha_c}{\alpha}\right) \tag{1.53}$$

$$F_{C_{EP}} = \left[1.062 + 0.354\left(\frac{2}{3}K_Y - 3\frac{\alpha_c}{\alpha}\right)\right] \tag{1.54}$$

where α_c is the critical vertical deformation at the inception of elastic-plastic deformation (which is assumed to occur when the maximum pressure at the contact interface exceeds $0.6H$ [59]), and is given by

$$\alpha_c = \left(\frac{\pi\, 0.6H}{2E^*}\right) R \tag{1.55}$$

and $K_Y = 1.282 + 1.158\nu$, being ν the Poisson's ratio.

Then, considering a circular contact area, Eq. 1.54 can be used to relate the asperity radius a and the contact force $F_{C_{EP}}$ as

$$a = \left(\frac{F_{C_{EP}}}{H\pi \left[1.062 + 0.354 \left(\frac{2}{3} K_Y - 3\frac{\alpha}{\alpha_c} \right) \right]} \right)^{1/2} \tag{1.56}$$

Therefore, the contact area radius depends on the contact force generated by the micro-relay and it can be determined through the former material deformation models. However, it exists a vast variety of works in the state-of-the-art that account for added effects such as surface contamination, adhesives forces, and even dealing with quantum theory in ultra-scaled relays. For further detail, you should refer to [55].

1.5.3 Contact Force and Area

After pull-in, the relay's electric contacts are in physical contact with minimum force and it can be increased by overdriving the device with increased actuation V_{GS} voltages beyond the V_{PI}. Let us now model the switch as a beam with a fixed end at $x = 0$, a simply supported end at $x = l$, and an intermediate external load (F_E) at $x = a$ as illustrated in Fig. 1.13 [60].

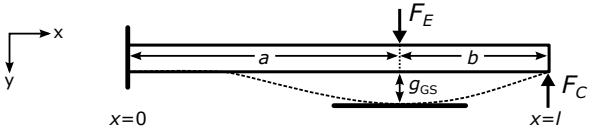


Figure 1.13: Cantilever beam model with a fixed end at $x = 0$ and a simply supported end at $x = l$, and an intermediately placed external load F_E at $x = a$ [60].

The contact force F_C causes the relay to buckle towards the actuation electrode and it is given by [60]

$$F_C = \frac{\epsilon_0 A V_{GS}^2 a}{4l^3 (g_{GS} - g_{DS})^2} (3l - a) \tag{1.57}$$

where A, V_{GS}, g_{GS}, and g_{DS} were already defined in section 1.1. Notice

that Eq. 1.57 is valid until the beam collapses onto the driving electrode.

Thus, contact force is thus exclusively determined by mechanical switch design, but real contact area A_C is determined by contact geometry, surface roughness, and material properties. Fig. 1.14 shows a typical micrometer scale contact with an apparent contact area A in which multiple asperities come into contact, resulting in multiple contact spots of varying sizes. The effective contact resistance arising from the contact spots depends on the radius of the spots (given by the considered circular contact area) and the distribution of the spots on the contact surface as already explained in previous sections 1.5.1 and 1.5.2. A simplified model which considers a circular spot of radius a_{eff} and of area equal to the total area of all the individual contact spots combined (see Fig. 1.14) can be used for obtaining an upper bound calculation of the contact resistance [61]. On the other hand, a lower bound can be also obtained on the contact resistance by assuming that contact spots are independent and conduct in parallel [61].

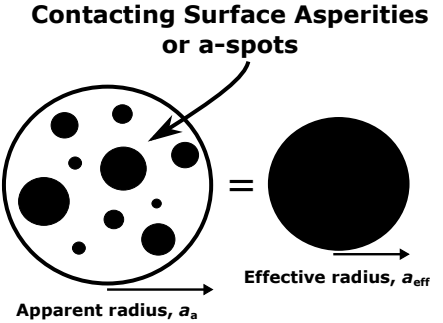


Figure 1.14: Apparent area of radius r_a with multiple spots of varying sizes as an equivalent a-spot effective radius a_{eff}

1.6 Relay Topologies

Various relay implementation topologies are possible either using lateral or vertical actuation schemes as summarize Tab. 1.1. As formerly presented, the simplest configuration is the two-terminal architecture in which a voltage difference is applied between the source and a common single gate/drain electrode, producing an electrostatic force that pulls the active element into contact with the gate/drain electrode [62–67]; and a three-terminal architecture is designed such that the movable structure is electrically connected to the source electrode and it is brought into contact

by the voltage difference between the gate and source terminals, which can be high without affecting the current flowing through the contact since it is determined by the drain-to-source voltage difference [32, 33, 43, 68, 69].

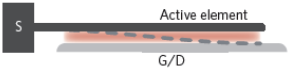
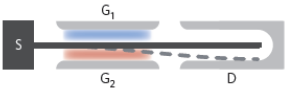
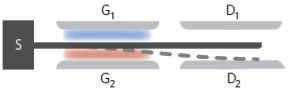
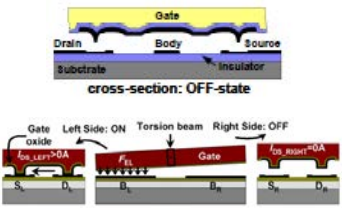
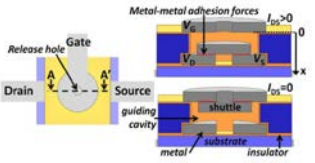
More complex architectures can be easily implemented by adding opposite lateral gate and drain electrodes. For instance, a 3-terminal device with an opposite pair drain and gate electrodes [70, 71], a 4-terminal architecture with a pair of gates and a common drain [72, 73] or even a 5-terminal device with opposite pair of gate and drain electrodes [13, 31, 49, 74]. Thus, the relay can be actuated bidirectionally overcoming thereby possible stiction issues in the contacting region [75, 76].

Additional functionality can be achieved by connecting two or more NEM switches to make a logic gate. For example, two NEM switches are only required to make a four-terminal XOR gate, whereas at least ten CMOS transistors are necessary to implement such a gate which opens a new logic minimization paradigm for NEMS-based digital logic circuits [73].

Dedicated custom fabrication process enables additional features. By adding an isolation layer between a metallic conducting channel and a movable gate electrode, a novel concept of body-bias configuration can be implemented. The relay is actuated by applying a voltage difference between the movable gate electrode and a body electrode beneath it, whereas an independent pair of source/drain electrodes are interconnected through a metallic conducting channel attached to the movable electrode via an insulating gate dielectric layer, once the movable structure is pulled in either vertically [77–79] or torsionally [76] actuated. Such a concept of body-biasing allows the relay to operate in a complementary fashion, e.g. as in a simple inverter circuit; and also gives the ability to precisely tune the pull-in (or threshold) voltage of the relay, which has led to the recent demonstration of sub-100-mV operation representing a significant milestone toward ultra-low-power mechanical computing [34, 80].

Finally, apart from the conventional anchored MEM structures, a three-terminal anchor-free structure is proposed in [81], in which a guiding cavity ensures that the free-flying shuttle electrode under vacuum is mechanically switched upon the two on and off state positions.

Table 1.1: Schematics of various topologies of NEM devices showing the source (S), gate (G), drain (D), body (B) and active element. Figures are extracted from [10, 76, 78, 81].

Topologies	Schematic
Two-Terminal Architecture	
Three-Terminal Architecture	
Two-Terminal Architecture with Opposite Pair G/D Electrodes	
Four-Terminal Architecture (with Common D Electrode)	
Five-Terminal Architecture	
Body-Biased Complementary Logic Architecture	
Anchor Free Architecture	

1.7 Properties and Potential Applications

As stated in the thesis presentation, the advantages of nanoelectromechanical (NEM) switches over transistors, which make them attractive for ultralow-power digital logic applications, include zero off-state leakage and

supersteep (nearly zero) subthreshold swing [34, 79, 82, 83]. The characteristic hysteresis response of NEM relays also makes them suitable for memory applications such as in SRAM devices [13, 84], for non-volatile memories [81, 85, 86] and for self-programmable routing elements in FPGA's [16]. Monolithic integration of NEM relays into CMOS technology paves a technological pathway towards hibrid NEM-CMOS relay circuits [15, 72]. They can be placed on top of the CMOS routing layers with the use of CMOS-compatible processes or directly implemented into the interconnect BEOL layers as the present work proposes. With the use of low-thermal budget processes, NEM relays can be integrated in flexible plastic substrates for reduced cost and with prospects of use in biochemical sensors [87]. Also, high-temperature-compatible materials such as silicon carbide can be used for relay operation in harsh environments [69, 88]. Alternatively, surface functionalization of NEM relays allows to explote such devices for ultra-low power sensors. For instance, N. A. Gilda *et al.* take advantage of the temperature-dependent contact resistance to detect TNT molecules [89]. In this thesis, we will show that the stiffness-dependent pull-in voltage can be leveraged to implement a mass-stiffness sensors. Tab. 4.2 summarizes the mentioned properties and their corresponding applications.

Properties	**Applications**
Zero leakage current Abrupt subthreshold slope	Ultra-low-power logic applications
Hysteresis Stiction	SRAM, non-volatiles memories and FPGA routing
Monolithic integration	Hybrid NEM-CMOS relay circuits
High temperature operation Extreme radiation hardness	Harsh environments
Flexible substrates	Low-cost circuits Biochemical sensors
Surface functionalization	Ultra-low-power sensors

Table 1.2: Properties of M/NEM relays and their potential applications

Chapter 2

CMOS/BEOL-MEMS Platform

Chapter 2 presented the design and modeling of micro-relays. In this chapter, we first provide an overall image of the actual of state of the art of the M/NEM relay technology, which serves us to discuss the fabrication approach followed in this thesis. Thus, it is next presented a detailed description of the monolithic approach for fabricating electrostatically actuated MEMS relays in a low cost, conventional CMOS technology.

The relays are embedded in the back end of line of a commercial CMOS technology and released following a post-processing strategy based on a simple one-step maskless wet etching. The selected platform, provided by Austriamicrosystems, features a minimum gate length of 0.35 μm, four metal layers (MET1-MET4) interconnected through via layers (VIA1-VIA3) and a capacitance module composed by two polysilicon layers (POLY1-POLY2).

Two different approaches have been explored for designing BEOL-embedded CMOS-MEMS relays; in-plane actuated relays defined using solely the via layer and torsional actuated relays formed with metal and via layers (usually named composite) while supported by vias will be presented and discussed, giving the necessary tools for the design of such relays with the AMS 0.35 μm CMOS technology.

2.1 Micro- and Nano-Relay Technologies

Next four tables (Tab. 2.1, 2.2, 2.3, 2.4, and 2.5) aim to provide an overall image of the actual state of the art of the MEMS/NEMS relay technology. We refer to NEMS when at least two of their dimensions are on the order of hundreds of nanomenters. Otherwise, we refer to MEMS. These tables

include the structural description, primary materials and main characteristics of M/NEM relays and they are arranged according to the fabrication method.

In general, two different approaches can be employed to fabricate micro- and nanorelays [90]. (i) Top-down techniques in which the mechanical structure is patterned with the use of high-resolution lithographic processes and etching techniques [63, 68, 70, 71, 91, 92]; and (ii) bottom-up techniques in which smaller structures such as carbon nanotubes (CNTs) or silicon nanowires (SiNWs) are fabricated by growth techniques (from tables: devices [31–34, 62, 64, 66, 67, 69, 74, 76, 78, 83, 93, 94]).

Bottom-up techniques can provide outstanding results when fabricating structures of small dimensions. In this sense, extensive studies have been carried out on NEMS relay applications based on CNTs [70, 71, 91, 92] and NWs [63], due to their superior mechanical properties, low power consumption and operating frequencies in the gigahertz range; being postulated as potential candidates for switch, memory and sensor applications.
Although such existing devices based on the bottom-up approach have shown relatively low operating voltages, they are still far from realization due to many obstacles such as non-reproducible fabrication, poor reliability, and huge contact resistances. Nonetheless, in the line of achieving high density and reproducible CNTs wafers, bottom-up along with top-down approaches were combined in [68], demonstrating diverse 3D functional nanodevices.

In contrast, top-down techniques which are well controlled and widely used in IC fabrication, offer good resolution and repetitivity for relatively large structures; but continuous advancements in nanofabrication techniques have led to the development of top-down ultra-scaled NEM relays seeming bottom-up NWs. For instance, X. L. Feng *et al.* used a nanomachining process based on a hydrogen silsesquioxane (HSQ) negative mask that yielded low voltage NWs featuring widths thinner than 50 nm and gaps thinner than 30 nm [64].

Let us now focus on NEM relays based on top-down approaches, in which representative milestones can be highlighted. Sub-1 V operation has been recently demonstrated by means of a novel pipe-clip structure featuring an air-gap of only 4 nm. In addition, the electrical characterization has shown an abrupt subthreshold swing less than 10 mV/dec with a on-off current ratio exceeding 10^5, but an endurance of only 20 cycles [69]. A silicon carbide (SiC) NEMS-based inverter has shown to operate more than $2 \cdot 10^9$ at 500 °C, although it may not be integrated with CMOS circuitry [66].

Since NEM relay technology is intended to complement or selectively replace conventional CMOS technology, the majority of top-down NEM relays seek to be easily integrated into CMOS technology. This is why most of the reported NEM relays in the state of the art are formed at CMOS-compatible temperatures [31, 33, 62, 69, 74]. In this way, they can be placed on top of the CMOS routing layers following therefore a MEMS-last or post-CMOS monolithic integration approach. However, none of them dealt with CMOS circuitry; rather, they focus on the electrical characterization of standalone devices. Different materials have been explored such as Pt [74], TiN [62], Ru [31], and SiGe [33]. Among these four, the most promising results have been obtained in the Pt-coated relay [74], which has shown a life time of 10^8 switching cycles in dry N_2 ambient.
In fact, experimental demonstrations of interaction between an integrated MOSFET and an electrostatically actuated NEM relay were presented for the first time by S. Chong *et al.*. They fabricated laterally actuated 3-T Pt NEM relays using e-beam lithography on top of a nMOS transistor, showing successful functionally of both nMOS transistor and NEM relay. However, poor results were obtained concerning the contact resistance and reliability issues [32].

Focusing now on MEMS relays, two different relays based on the same concept of a curved beam design that results in a robust configuration able to sustain a high actuation voltage were reported in [83, 93]. Both relays are fabricated on a silicon on insulator (SOI) substrate, although in [93] the relay is encapsulated in an ultra-clean vacuum environment created as part of the epi-seal process proposed by Robert Bosh [95] and brought into commercial production by SiTime Inc. [96]. This fact helps to increase the device reliability through prevention of oxidation, showing in this way an endurance of 10^5 cycles at room temperature. However, epi-seal process involves high temperature steps ($> 900°C$) which means that it is no CMOS compatible. On the other hand, in [83] the authors opt for coating with Pt the contact so as to reduce the contact resistance and try to circumvent oxidation issues, but there is no data on the device endurance.

In addition to those SOI-based relays, let us now introduce the Berkeley 4-terminal folded-flexure body-biased relay with poly-SiGe structure and tungsten contacts [78]. The 4-terminal (body-biased) relay design provides a convenient way of electrically adjusting the gate switching voltages via body biasing for low-voltage operation. The process used to fabricate such relays involves neither exotic materials nor very high substrate temperatures, and therefore, it is CMOS compatible. Fabricated 4T relays exhibit

an abrupt switching characteristic with a inverse subthreshold slope < 6.25 mV/dec, an on-off ratio between 10^8-10^{10}, a low pull-in voltage (< 2) via body-biasing ($V_B = -11$ V), and a great endurance exceeding 10^9 on-off switching cycles. Therefore, the Berkeley relays present a series of characteristics that make them a promising candidate to realize relay-based integrated circuits.

The same research group reported a torsionally actuated MEM relay structure named dual-ended seesaw relay [76], which was based on the same fabrication process than the previous one [78]. Both designs exhibit similar switching characteristics. Yet, in this case, complementary switching behavior can be achieved with the use of only one structure.

Despite the fact that tungsten is a conductive metal, the authors showed that W-contact relays forms an insulating oxide that reforms readily during testing, which causes the contact resistance to be unstable [78]. In the line of improving such contact instability, further improvements were addressed by examining alternative contact materials. Ruthenium contacts showed superior stability when compared to such W-contact relays [97].

Recently, with a new relay design (high-stiffness 6-terminal relay operated in non-pull-in mode) and further process optimization, the same research group led by T.-J. King Liu has demonstrated the operation of a relay-based inverter circuit below sub-100-mV operation representing a significant milestone toward ultra-low-power mechanical computing [34]. Despite of all these precedents, the Berkeley relays are significantly larger than CMOS devices. Hence, the mechanical delay becomes a time-limiting factor in relay-based circuit operation. In order for such relays to be attractive as CMOS replacement device, a further scaled technology is required, from which switching speed and operating voltage is expected to be improved.

Coming back to NEM relays, but this time focusing on the BEOL-embedded ones, two different works can be already found in the state of the art [67,94]. These works were developed previously to the present thesis by J. L. Muñoz Gamarra in the ECAS group led by N. Barniol. He posed as a constraint try to minimize the relay dimensions for low voltage and high frequency operation. To do so, two different approaches were tackled. In [94], the advanced ST 65 nm CMOS technology was used as a platform to take advantage of the reduced dimensions of the available BEOL layers. In this way, 2-terminal BEOL-embedded NEM relays were succesfully fabricated using the METAL1 layer, whose primary material is copper. The electrical characterization showed an abrupt switching transition of only 4.3 mV/dec with a low V_{PI} of 6 V, although the device endurance did not

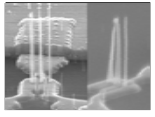
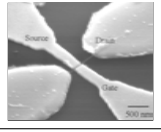
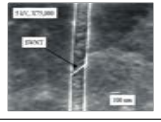
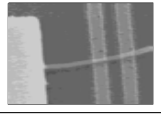
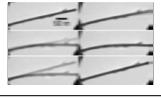
exceed tens of cycles. In [67], the metal-insulator-metal (MIM) module of the AMS 0.35 μm CMOS technology was used as a platform for the development of 2-terminal cantilevers which featured air-gaps of only 27 nm. It showed a switching transition of 5 mV/dec with a V_{PI} of 20 V, and an on-off ratio exceeding 10^4. However, even coating the samples with an ultra-thin insulating Al_2O_3 layer, the device endurance again did not exceed tens of cycles.

In general, all the mechanical relays have shown to exhibit almost zero leakage current and abrupt switching characteristics with near zero sub-threshold swing. Pull-in voltages ranging a wide spectrum of values have been reported, since it relies on how switch is engineered. On the one hand, NEMS relays boasts smaller dimensions but in general poorer reliability. On the other hand, MEMS relays boast better endurance. In particular, the Berkeley relay with tungsten contacts has shown promising results as early mentioned.
In view of these precedents, this thesis poses to develop BEOL-embedded NEM relays with relaxed dimensional constraints using as a platform the tungsten VIA3 layer of the AMS 0.35 μm technology. In addition, tungsten VIA3 layer presents a series of characteristics that suits for NEM relays:

- **High hardness:** A high hardness material is desirable for reliable operation; being resistant to wear and plastic deformation.
- **High melting point:** Tungsten exhibits the highest melting point (3422 °C); being in this sense resistant to welding-induced failure due to Joule heating at the contact.
- **HF resistant:** Tungsten is a highly resistant material to HF. Therefore, the structural material will not be affected by the wet etching process used to release the structures.
- **Low stress:** Low stress is desirable since it can be affect the curvature (and hence the actuation and contact gap) of the released structure. We will show in this thesis that the VIA3 module exhibits low stress.
- **Short releasing time:** The top BEOL layers are less buried of SiO_2, which implies less releasing time, and thus increased yield.

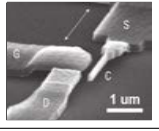
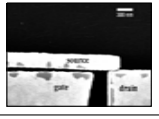
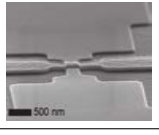
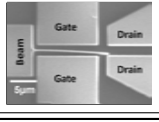
Two different approaches have been explored: in-plane actuated relays defined using solely the via layer, and torsional actuated relays formed with metal and via layers (usually named composite) while supported by vias.

Table 2.1: State of the art 1/5

	SEM Image	Structure	Dimensions	Primary Materials	V_{PI} (V)	ON-OFF Ratio	S (mV/dec)	R_{ON} (Ω)	Endurance (cycles)	CMOS Integration
[70]		Vertically actuated 3-terminal cantilever	l=2μm d=70nm	CNT, Nb	22.5	$\sim 10^4$	-	$\sim$ 500K[a]	1	Bottom-up no CMOS compatible
[71]		Laterally actuated 3-terminal c.-c. beam	l=800nm d=20-40nm g=40-60nm	CNT, Nb and Cr/Au	3.6	$\sim 10^4$	-	33M	3	Bottom-up no CMOS compatible
[91]		Vertically actuated 2-terminal c.-c. beam	l=250-500μm d=2nm g=10-40nm	CNT, Nb and Au/Ti	2.5-5	$\sim 10^4$	-	200K[a]	3	Bottom-up no CMOS compatible
[92]		Vertically actuated 3-terminal cantilever	l=2-2.5μm d=20-100nm g=80nm	CNT, Pt	20	$\sim 10^6$	-	$\sim$ 13K[a]	-	Bottom-up no CMOS compatible
[63]		Vertically actuated 2-terminal cantilever	l=3μm d=60nm g=250nm	Ge NWs, Au	19	$\sim 10^1$	-	$\sim$ 10G	$\sim$ 10	Bottom-up no CMOS compatible

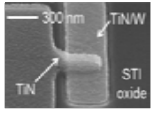
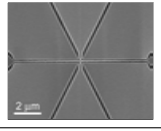
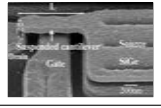
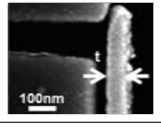
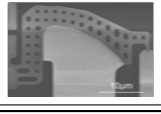
[a] The contact resistance R_{ON} is not explicitly mentioned in the article. For comparison purpose, it is calculated as V_D/I_D.

Table 2.2: State of the art 2/5

	SEM Image	Structure	Dimensions	Primary Materials	V_{PI} (V)	ON-OFF Ratio	S (mV/dec)	R_{ON} (Ω)	Endurance (cycles)	CMOS Integration
[68]		Laterally actuated 3-terminal cantilever	l=3.6μm w=170nm t=500nm g=650nm	CNT	$\sim$ 50	$\sim 10^7$	-	$\sim$ 50K[a]	23	Bottom-up and top-down processes
[64]		Laterally actuated 3-terminal c.-c. beam	l=5μm w=55nm t=50nm g=60nm	SiC	1-1.5	-	-	$\sim$10M[a]	$\sim$ 10	Top-down no CMOS compatible
[69]		Laterally actuated 3-terminal cantilever	l=8μm w=200nm t=400nm g=150nm	SiC	6	-	-	-	$2{\cdot}10^9$ at 500°C	Top-down No CMOS compatible
[66]		Vertically actuated 2-terminal pipe-clip structure	l=1.4μm w=300nm t=40nm g=4nm	TiW/W	0.4	$\sim 10^5$	$<$ 10	$\sim$ 4M[a]	20	Top-down CMOS compatible process
[74]		Laterally actuated 3-terminal cantilever	l=16μm w=500nm t=1.2μm g=600nm	PolySi with Pt sidewall coating	12	$\sim 10^5$	-	3K	10^8 in N_2	Top-down CMOS compatible process

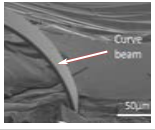
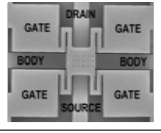
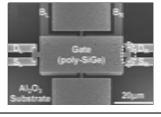
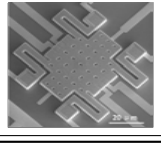
[a] The contact resistance R_{ON} is not explicitly mentioned in the article. For comparison purpose, it is calculated as V_D/I_D.

Table 2.3: State of the art 3/5

	SEM Image	Structure	Dimensions	Primary Materials	V_{PI} (V)	ON-OFF Ratio	S (mV/dec)	R_{ON} (Ω)	Endurance (cycles)	CMOS Integration
[62]		Vertically actuated 2-terminal cantilever	l=300nm w=200nm t=35nm g=15nm	TiN	13.43	$\sim 10^5$	3	$\sim$ 1G[a]	$\sim$ 400 in air	Top-down CMOS compatible process
[31]		Laterally actuated 5-terminal c.-c. beam	l=5μm w=100nm g=50nm t=10nm	Ru	13	10^8	-	-	Yield=1,5% (12/800 functional switches)	Top-down CMOS compatible process
[33]		Vertically actuated 3-terminal cantilever	l=3μm w=1μm g=200nm t=300nm	Poly-SiGe	$\sim$ 18	$\sim 10^5$	-	$\sim$ 5M	$\sim 10^3$	Top-down CMOS compatible process
[32]		Laterally actuated 3-terminal cantilever	l=3.5μm w=80nm g=100nm t=65nm	Pt with thin Ti adhesion layer	4.3	10^5	0.8	$\sim$ 10M	$\sim$ 10	Top-down CMOS compatible process
[83]		Laterally actuated 3-T curved cantilever	l=29.5μm w=4.5μm t=800nm g=50nm	Si with PtSi contact coating	14.3	10^6-10^8	-	4.4K	-	SOI substrate

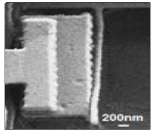
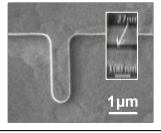
[a] The contact resistance R_{ON} is not explicitly mentioned in the article. For comparison purpose, it is calculated as V_D/I_D.

Table 2.4: State of the art 4/5

	SEM Image	Structure	Dimensions	Primary Materials	V_{PI} (V)	ON-OFF Ratio	S (mV/dec)	R_{ON} (Ω)	Endurance (cycles)	CMOS Integration
[93]		Vertically actuated 3-T cruved cantilever	r=75μm w=3μm t=40μm g=1-1.5μm	Si	20	10^4-10^7	6.25	28K	10^5 in vacuum	SOI/epi-seal process no CMOS compatible
[78]		Vertically actuated 4-terminal body-biased plate	A=810μm^2 t=1μm g=200nm	Poly-SiGe, TiO_2 coated W contact	< 2	10^8-10^{10}	< 1	1K (Fresh)	10^9	Top-down CMOS compatible
[76]		Torsional body-biased dual-ended seesaw	A=1680μm^2 t=1μm g=200nm	Poly-SiGe	7.14	10^{10}	< 0.1	800	10^9 in N_2	Top-down CMOS compatible process
[34]		Vertically actuated 6-terminal body-biased plate	A=1460μm^2 g=220nm t=1.75μm	Poly-SiGe with W contacts	0.92[b]	10^7	0.3	4.8K	-	Top-down CMOS compatible process

[a] The contact resistance R_{ON} is not explicitly mentioned in the article. For comparison purpose, it is calculated as V_D/I_D.
[b] V_{PI} lowered by body biasing $V_B = -11$ V.

Table 2.5: State of the art 5/5

	SEM Image	Structure	Dimensions	Primary Materials	V_{PI} (V)	ON-OFF Ratio	S (mV/dec)	R_{ON} (Ω)	Endurance (cycles)	CMOS Integration
[94]		Laterally actuated 2-terminal cantilever	l=3.5μm^2 w=100nm t=180nm g=100nm	Copper (Metal1)	~ 6	10^3	4.3	$\sim$ 6G[a]	< 10	BEOL-Embedded (65nm CMOS Technology)
[67]		Vertically actuated 2-terminal cantilever	l=1.7μm w=580nm t=150nm g=27nm	TiN (MIM module)	~ 20	10^4	5	$\sim$ 20G[a]	< 10 with Al_2O_3 coating	BEOL-Embedded using CMOS-MIM Capacitor

[a] The contact resistance R_{ON} is not explicitly mentioned in the article. For comparison purpose, it is calculated as V_D/I_D.

2.2 AMS 0.35μm CMOS Technology

The EUROPRACTICE IC Service [98] offers low-cost ASIC prototyping through Multi Project Wafer (MPW) from different IC technologies such as ON semiconductors, Austriamicrosystems (AMS), IHP, TSMC, UMC, XFAB and Globalfoundries. In previous projects, the ECAS research group has worked with three different foundries: AMS, UMC and STMicroelectronics. In this thesis, the whole of the designs presented are fabricated in the AMS foundry due to the previous experience in the framework of the ECAS research group.

2.2.1 Process Description

The AMS foundry offers a family of CMOS processes which have in common a core module called C35. This core module is mainly composed by a p-type substrate, a polysilicon gate layer with a minimum feature size of 0.35 μm and a bias voltage of 3.3 V, and three back end metals layers. Then, there are several available modules which add additional layers modifying the main core module. These modules are:

- **CPOLY:** Additional polysilicon layer POLY2 above the POLY1 and a thin dielectric layer layer to form integrated capacitances.
- **5-Volt:** 5 V mid-oxide for MOSFET's instead of 3.3 V of core module.
- **High resistivity poly module:** High resistivity poly module for integrated resistances (low doped polysilicon).
- **Thick metal module:** This module add an extra thick fourth metal layer to increase the interconnect capability between devices.
- **MIM module:** Acronym comes from metal-insulator-metal. This module form a METAL2-METCAP capacitor.

The family process used for the fabrication is the C35B4C3 process, which includes the CPOLY module, 4 metal layers and it is also one of the processes with more runs scheduled (seven times a year).

The cross-section of the AMS 0.35 μm CMOS technology is shown in 2.1. In general, the IC process flow can be divided into to main categories. The front end of line (FEOL) is the first portion of the IC fabrication

where the individual devices (transistors, capacitors, resistors, etc...) are patterned, i.e. generally covers everything up to (but not included) the back end of line (BEOL) processes. Thus, the BEOL is the second portion of the IC fabrication which is composed by the deposition of different metal layers separated by intermetallic dielectric layers (IMD) that allow the individual devices to be interconnected. Finally, two passivation layers protects the circuitry from the external environment and onle the electrical contacts are uncovered. Relevant dimensions and material properties of each BEOL layer are summarized in Tab. 2.6.

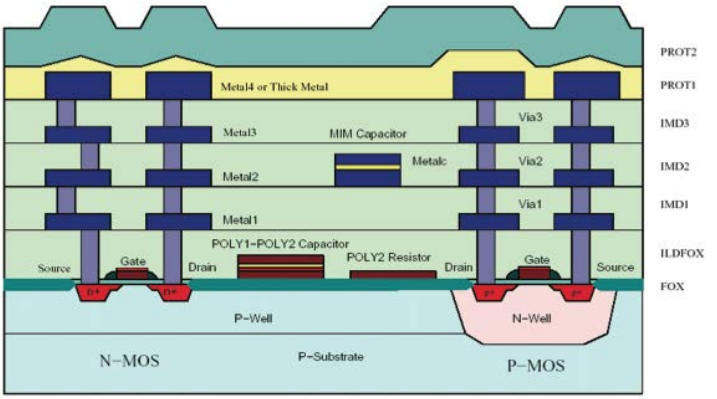


Figure 2.1: AMS-C35 CMOS Technology

	M1	**VIA1**	**M2**	**VIA2**	**M3**	**VIA3**	**M4**
Material	Al	W	Al	W	Al	W	Al
Thickness [nm]	665	1	640	1	640	1	925
Mass Density [g/cm^3]	3	19.3	3	19.3	3	19.3	3
Young's modulus [GPa]	131	410	131	410	131	410	131

Table 2.6: Relevant technology dimensions of AMS-C35 for the considered design

2.2.2 VIA Technology

In this section, we describe the CMOS process flow through BEOL layers in order to understand the VIA3 platform used to fabricate NEM relays. We cannot provide an exact recipe of the AMS 0.35 μm process flow since this information is confidential. Rather, we briefly review a general explanation

given in [99].

Electrical coupling between MET4 and MET3 is achieved by the VIA3 module. Fig. 2.2 shows the process steps followed to form W-VIA3. First, the METAL3 stack is deposited and patterned. Basically, it consist in a metal stack of Ti/TiN/Al/TiN. The Ti provides adhesion of the TiN and reduction in electromigration problems. The bottom TiN serves primarily as a diffusion barrier to $TiAl_3$ formation. The topmost TiN acts as an anti-reflective coating for the metal photolithography as well as an etch stop for the subsequent via formation. Second, the intermetalic dielectirc layer IMD3, which serves as isolation layer between MET3 and MET4, is deposited and subsequently planarized (Fig. 2.2(a)). Over the planarized IMD3, openings for interconnecting metal lines are defined via plasma etching (Fig. 2.2(b)). Next, a thin Ti/TiN stack layer of tens of nanometers is deposited, which acts also as a diffusion barrier metal in the contact hole prior to tungsten (W) plug (Fig. 2.2(c)). Then, tungsten is deposited (overfilled) as seen in Fig. 2.2(d). Finally, the overfilled W is planarized by chemical mechanical polishing (CMP) as shown in Fig. 2.2(f).

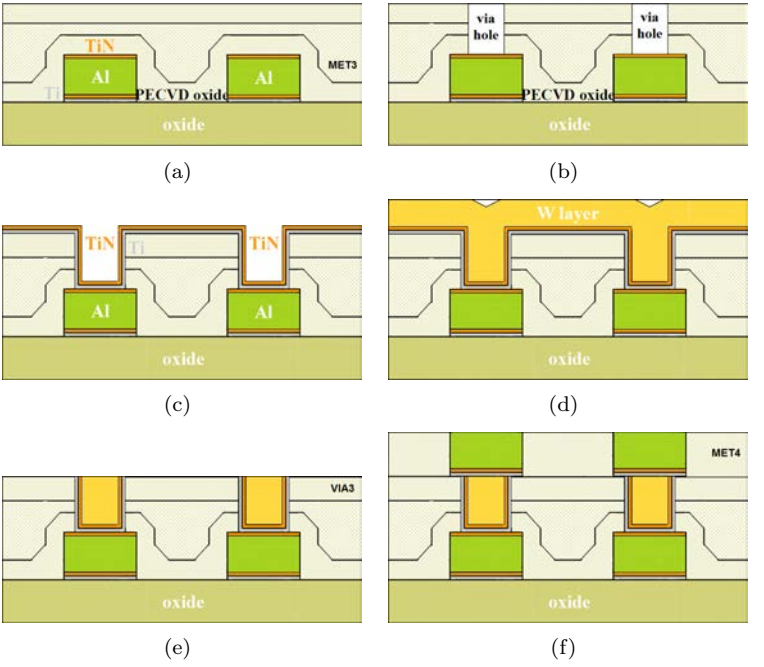


Figure 2.2: W-plug technology

In a similar manner as the METAL3 process, the MET4 is then deposited. In this case, notice that the MET4 plays the role of top metal. Thus, to favor electrical contact, the MET4 stack not includes the top TiN layer, i.e., the MET4 stack consist of Ti/TiN/Al.

2.2.3 CMOS-MEMS Design in AMS 0.35 μm

The CMOS foundry defines a series of design rules that have to be accomplished in order to ensure the proper IC fabrication. Following, we show the BEOL layers of the AMS 0.35 μm CMOS technology and their main design rules that are mandatory for CMOS IC prototyping:

- **PAD:** Define the bond pad opening on the passivation layer. The opening hole has a minimum square size of $15x15$ μm^2 and all metals and vias must be placed below them.
- **MET4-MET1:** The metal lines are intended to interconnect transistors and circuits between them and with the output bond pads. Each metal has their own design rules related with minimum width, spacing and enclosure for subsequent vias.
- **VIA3-VIA1:** Metal lines are isolated by means of intermetalic dielectric layers (IMD) of thickness 1 μm. Via's open a direct vertical path through IMDs to interconect metal lines. Via's have a fixed square shape of $0.5x0.5$ μm^2, a minimun spacing of 0.45 μ and, in principle, via's without metals are not allowed.
- **CONT:** It is a via intended to interconnect MET1 and FEOL layers (polysilicon or active regions).

Nevertheless, it is needed to skip or modify some of the design rules so as to enable MEMS prototyping through such available BEOL layers. The following design rules have been established throughout a trial and error learning process carried out by the ECAS group:

- **PAD:** This layer is intended to define a passivation apperture over the MEMS area so that the structure can be released bu means of a one-step maskless wet etching process (described later).
- **VIA3:** This layer is used as the structural MEMS layer. We omit the fixed square shape of the via. Regardless, it is mandatory to keep the width of the VIA3 to 0.5 μm. Otherwise, it is not properly defined, resulting in a via divided into to halves.

- **VIA2-VIA1:** It can also be engineered to be used as structural MEMS layer, but at expense of longer releasing time. In this thesis, we have only dealt with VIA3 as structural layer. Regardless, it can be used for its traditional interconnecting purpose.
- **MET4-MET1:** These layers are intended to be used as contact or actuation electrodes as well as for anchoring the structural VIA3 layer.

Electrical contacts to the output bond pads are realized by defining the necessary contacts and metal lines from the MEMS electrodes towards bond pads. A grounded N-well under the MEMS area is also defined to prevent unfortunate short-circuits between an electrode and the chip substrate. Silicon oxide (SiO_2) that surrounds metal and contact lines is used as sacrificial layer. Next, we introduce the post-CMOS releasing process used in this work.

2.2.4 Post-CMOS Releasing Process

After the CMOS process is finished, a releasing process is required in order to etch the $SiO_2$2 sacrificial layer which surrounds the movable structure. This step is characterized to be out-foundry and it is based on a simple one-step maskless wet etching process performed by means of a buffered hydrofluoric (BHF) solution. This BHF solution is composed by ammonium flouride, acid acetic and HF acid which slows down the etch rate of the aluminium while preserves the etch rate of the SiO_2.

The releasing process sequence consists in 3 main steps as depicted in Fig. 2.3:

1. The first step is the etching of the sacrificial oxide layers. The duration of the etching depends on the oxide thickness to be removed. The effective time of the BHF solution is 18 minutes, so the releasing of thicker oxide requires more than one etch step.
2. After the etching step, the sample is submerged in water (maintaining a constant water flow) in order to remove the reactive agent.
3. Following, the sample is brought into an isopropyl alcohol bath.
4. After the cleaning process, the sample is put into an oven for an approximated time of 10 min in order to dry it.

5. The chip is now ready to be characterized whether by electrical measurements or scanning electron microscope (SEM) imaging.

Figure 2.3: Schematic sequence of the wet etching process based on a BHF solution.

2.3 Relay Integration Approaches

As formerly stated, two different approaches have been explored for fabricating NEM relays using the VIA3 module of the AMS 0.35 μm: laterally actuated relays defined using solely the via layer, and torsionally actuated relays formed with metal and via layers (usually named composite) while supported by vias. In the next two subsections, results involving the fabrication of NEM relays using this two different approaches are presented and discussed.

2.3.1 Lateral NEM Relays based on Tungsten VIA3 Layer

This approach enables the fabrication of laterally actuated beams using the VIA3 layer provided by the AMS 0.35 μm CMOS technology as structural layer. An illustration of a 3-terminal configuration schematic and its cross-section view is shown in Fig. 2.4. As we can see, the relay is defined using solely the VIA3 layer, whereas the electrodes are composed of MET4/VIA3/MET3. The sacrificial layer is the surrounding SiO_2 corresponding to the different inter-metal oxides (i.e. IM3 and IM2). The minimum lateral gap that can be achieved (experimentally checked) is 450

nm. A passivation aperture strategically defined over the relay area allows the sacrificial layer to be etched by following the releasing process described previously in Subsection 2.2.4. Finally, the design is complemented by a grounded n-well to avoid parasitic electrical signal in the device performance.

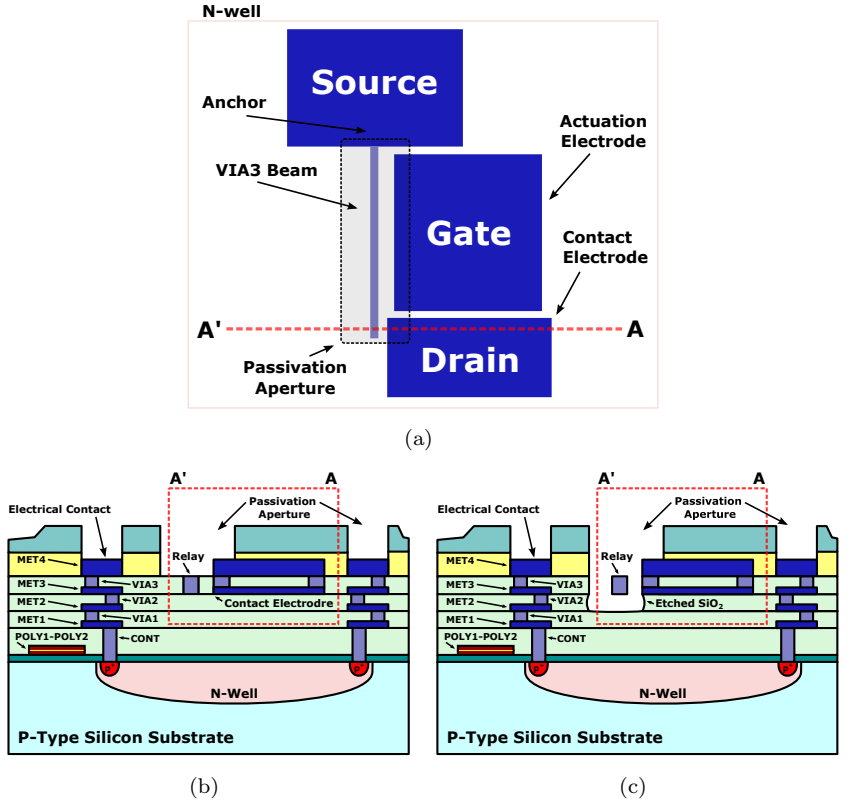
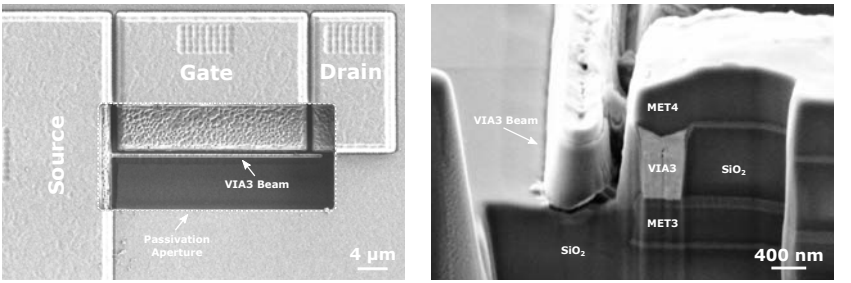


Figure 2.4: (a) Schematic of the 3-T relay design layout which consists of a suspended beam fixed by one side, an actuation electrode and a contact electrode. A detailed zoom of the tip is shown on the right side. (b) Non released and (c) released cross-section schematic along the red line A'-A in (a).

Fig. 2.5 shows the top view and cross-sectional view SEM images of a 3-terminal relay of length 30 μm. As can be seen, the structures have been properly mechanized during the standard CMOS process and that the sacrifical layer is only present underneath the relay enabling a fast releasing with only immersing the chips in the BHF solution for approximately 4–6 minutes.



(a) (b)

Figure 2.5: (a) Top view and (b) cross-sectional view SEM images of a 3-terminal relay fabricated after the standard CMOS process (i.e. without being released).

In fact, compared to previously developed polysilicon resonators using the poly-silicon-insulator-polysilicon (PIP) module of the AMS 0.35 μm [100], the lateral tungsten VIA3 NEM relays do not require the placement of the vias around the MEMS structure in order to reduce the amount of SiO_2 and thus reducing the amount of required etching time. Rather, it only requires the passivation aperture that allow the releasing of such structures. In addition, tungsten is a highly resistant materials to HF, so that they are less prone to get overetched than previously developed aluminium MET4 resonators [101].

2.3.2 Torsional Composite MEM Relays based on MET4-VIA3-MET3 Layer Stack

This approach enables the fabrication torsionally actuated relays formed with metal and via layers (also known as composite) while supported by vias. In this way, the coupling area is not limited by the thickness of the layer as occurs in the lateral relays so that it can be optimized through design engineering. However, the air-gap will be larger than the lateral one, since it is determined by the thickness of the IMD layers.

Fig. 2.6 shows the first relay design that consists of one simple main beam anchored by two torsion beams (called source, S), defined with tungsten VIA3 layer, which allows the ends of the main beam move up and down by actuating electrostatically the underneath located gate electrodes (G_R and G_L) of MET2, which are sandwiched layers of titanium nitride-aluminium- titanium nitride (TiN-Al-TiN). Such mentioned endings are

made of a stack of MET4-VIA3-MET3 layers and make contact with the drain electrodes (D_R and D_L) also of MET2. The sacrificial layer that has to be etched is the whole IMD3 and IMD2 layers up to reach the MET2 electrode.

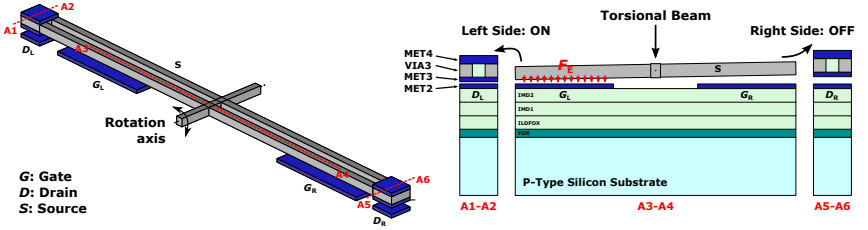
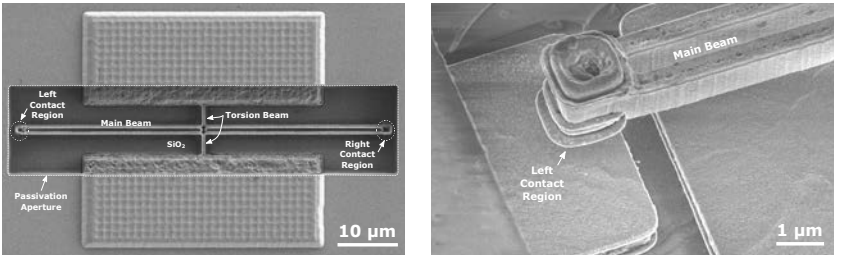


Figure 2.6: Three-dimensional schematic of the designed torsional relay including cross-sectional views.

Fig. 2.7(a) shows a top view SEM image of an unreleased torsional relay. The relay can be directly observed whereas the contact electrodes are burried in SiO2. The etching time required for releasing these structures is 12 minutes, resulting in a contact electrode completely free of SiO_2 as shown in Fig. 2.7(b).



(a) (b)

Figure 2.7: (a) Top view SEM image of a 5-terminal torsional relay fabricated after the standard CMOS process (i.e. without being released). (b) SEM image of the left contact side of a fabricated and released relay for 12 minutes.

Fig. 2.8 shows the second relay design (named seesaw relay) whose operation mode is identical to the previous one, but several particular design characteristics should be highlighted. The coupling area along the structure is maximized with a main plate made of MET4-VIA3-MET3 stack which allows to further reduce the actuation voltage. To avoid early collapse with the gate electrode, the actuation electrode is defined with higher separation with the use of MET1-VIA1. Regarding the contact

electrode, different contact interfaces are designed as indicates the cross-sectional view shown in Fig. 2.8: (i) MET4-VIA3-MET3, and (ii) MET4-VIA3 which make contact with the drain electrodes (D_R and D_L) of MET2; and (iii) MET4-VIA3 that makes contact with the drain electrodes (D_R and D_L) of MET1-VIA1.

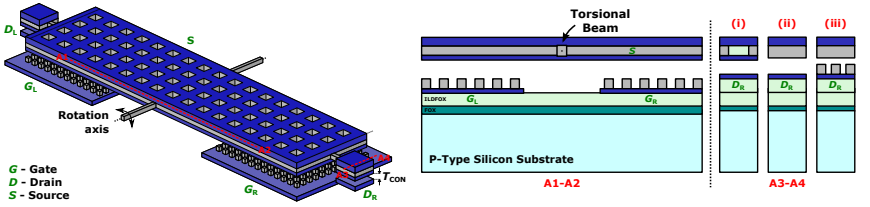


Figure 2.8: Three-dimensional schematic of the designed see-saw relay including cross-sectional views. Three different types of contact are designed: (i) MET4-VIA3-MET3, (ii) MET4-VIA3 and (iii) MET4-VIA3.

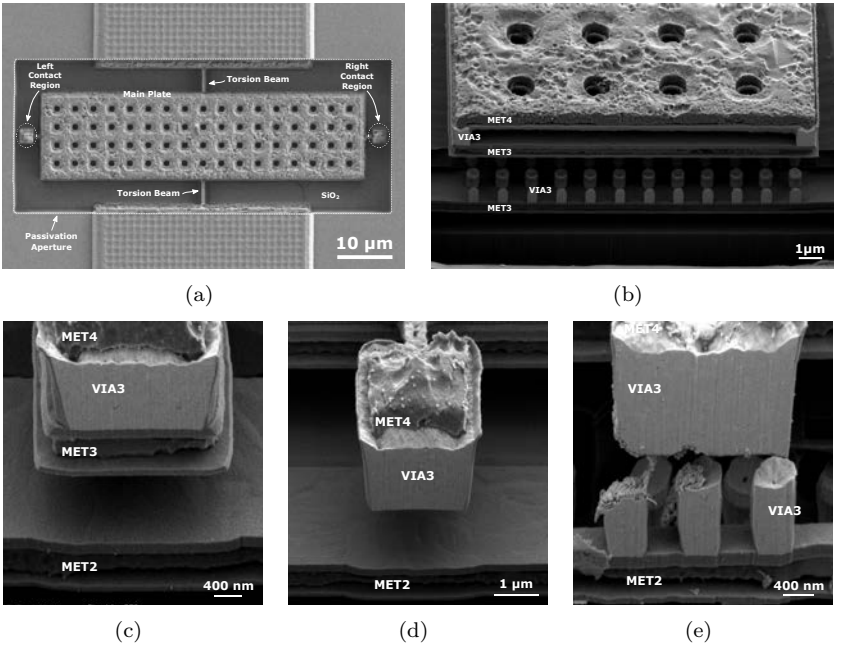


Figure 2.9: (a) Top view SEM image of a 5-terminal seesaw relay fabricated after the standard CMOS process. Released cross-sectional view SEM images of (b) the actuation electrode and the three different types of designed contacts: (c) MET4-VIA3-MET3, (d) MET4-VIA3 and (e) MET4-VIA3.

Fig. 2.9(a) shows a top view SEM image of a unreleased seesaw relay. Again, the relay can be directly observed whereas the contact electrodes are burried in SiO_2. For releasing these structures, it is required immerse the chips in BHF for 18 min. SEM images of the actuation electrode of MET1-VIA1 (cross-section A1-A2) as well as the different types of contact (cross-section A3-A4) are shown in Fig. 2.9(b) and Fig. 2.9(c), 2.9(d) and 2.9(e) respectively.

The key of the presented designs is that the backbone of the MEM structure is based on the VIA3 layer platform, which is made of tungsten, a very hard material that provides excellent mechanical strength to support the torsional relay. Moreover, it has a high melting point that makes it suitable to stand high current and temperature. In contrast, tungsten is highly susceptible to oxidation and exhibits poor formability. For this reason, the source-to-drain conductive path is formed with TiN that forms the sandwiched layers MET3 and MET2. TiN presents low electrical resistivity, better formability and an excellent chemical inertness [**?**]. In this sense, the proposed approach fully exploits the available resources of the selected CMOS technology for fabricating micrometer scale CMOS-MEMS resistive switches.

Chapter 3

Lateral VIA3-based Nanoelectromechanical Relays

In this chapter, laterally-actuated nanoelectromechanical (NEM) relays based on tungsten VIA3 layer are presented. The three first sections follow a chronological order; in this sense, each series of fabricated devices are sorted as first generation, second generation, and third generation. Each section corresponding to each generation of fabricated devices gives a layout scheme of each structure, as well as a detailed description of the physical and electrical characterization results. The next section proposes a post-CMOS coating method for covering the sidewalls of fabricated relays involving alternative materials that either does not oxidize in ambient air or forms a conductive native oxide. The last section aims to present a fully electrical resonant cold-switching characterization of a fabricated tungsten relay based on the capacitive detection of its nonlinear tapping mode.

3.1 First Generation

As formerly stated, the guiding thread follows a chronological order. So, results involving first generation (1G) are then presented in this section. The section is divided into three main subsections, giving a detailed look on the design, physical and electrical characterization results.

3.1.1 Design

The 1G of designed relays are based on the electrostatic in-plane actuation of a cantilever beam defined using a three terminal (3-T) topology. These 3T's are denoted as source (S), gate (G) and drain (D) like in a MOSFET device. An illustration of the designed layout and its cross-section view is

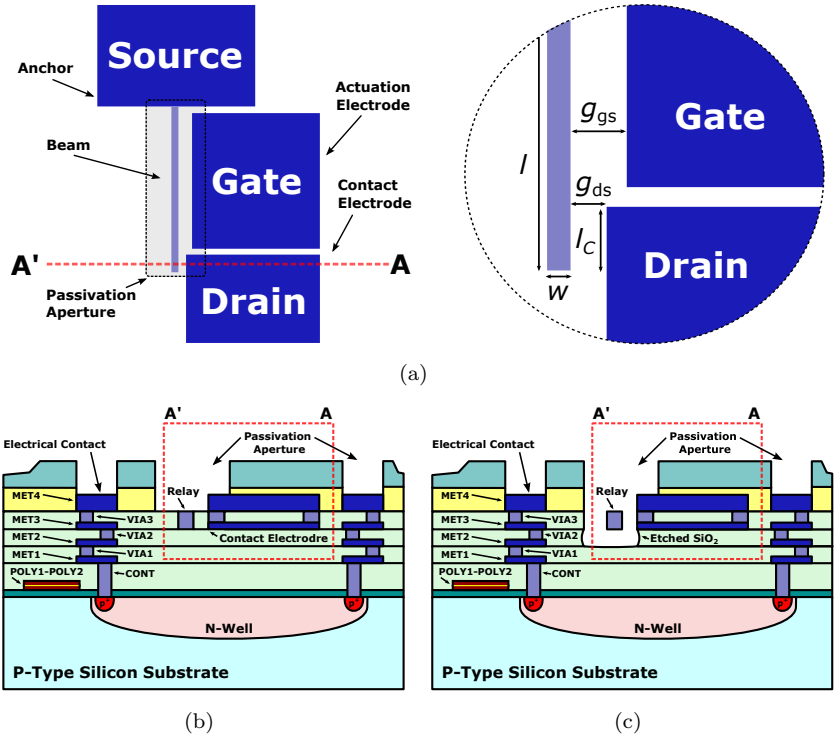


Figure 3.1: (a) Schematic of the 3-T relay design layout which consists of a suspended beam fixed by one side, an actuation electrode and a contact electrode. A detailed zoom of the tip is shown on the right side. (b) Non released and (c) released cross-section schematic along the red line A'-A in (a).

		Layout	Measured
length	l	20, 30, 40, 50 μm	19.3, 27.9, 37, 47.6 μm
width	w	500 nm	490 nm
thickness	t	1 μm	1.3 μm
gate-to-source gap	g_{gs}	550 nm	520 nm
drain-to-source gap	g_{ds}	450 nm	410 nm
contact length	l_c	1.5 μm	1.3 μm

Table 3.1: 3-terminal relay geometric parameters: layout versus fabricated dimensions.

shown in Fig. 3.1(a) and 3.1(b), respectively. In Table 3.1, the design parameter values are summarized. As it can be observed, the presented relay

is defined using solely tungsten VIA3 layer, which interconnects MET4 with MET3, whereas the electrodes (i.e. source, gate and drain terminals) are composed of a stack of MET4-VIA3-MET3. A passivation aperture defined over the relay area allows the sacrificial layers to be etched, while the rest of the chip is protected by the passivation layer as shown in Fig 3.1(c). The design is finally complemented with a grounded n-well to avoid parasitic electrical signal on the device performance.

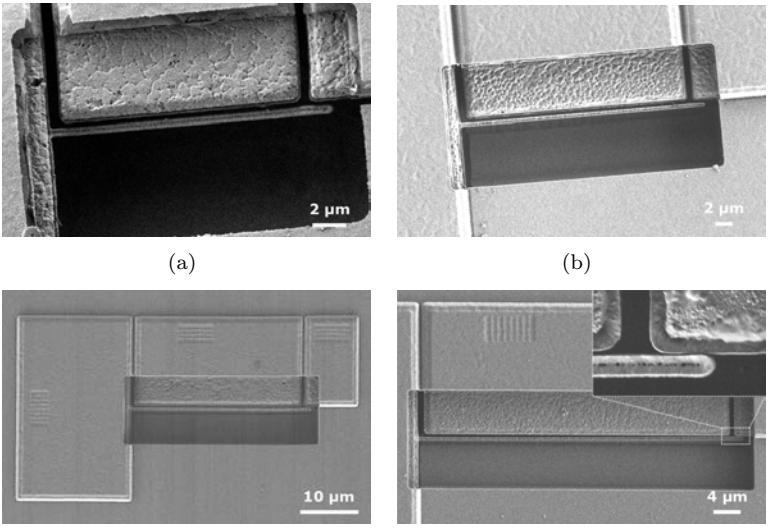
3.1.2 Physical Characterization

Different relay designs of varying lengths (20, 30, 40 and 50 μm) were successfully fabricated and released as shown in the SEM images grouped in Fig. 3.2. However, most of the released cantilevers with lengths of 40 μm and 50 μm were found to be prone to stiction just after the releasing process (see zoom of the cantilever tip provided in Fig. 3.2(d)).

Stiction during release is caused primarily by surface adhesive forces such as van der Waals, Casimir force, electrostatic force and hydrogen-bond force, but capillary force is typically the dominant one during release [102]. A way to avoid stiction during release is to use solutions such as critical-point drying to eliminate surface tension [103] but add to process complexity and do not solve the problem completely. Incorporating a dual actuation, which will thereby provide bidirectionality for more reliable operation, is contemplated for next generation.

A critical element of the relay structure is the contact electrode since it determines the on-resistance (R_c) of the relay as well as contact reliability. A series of FIB cuts were made at the tip of several relays (see Fig. 3.3(a)) in order to check the contact profile as shown in Fig. 3.3(b). As can be seen, the two TiN layers that forms the MET3 stack protrudes more than the rest of the layers which a priori will reduce the expected effective contact area. In this sense, a flatter contact profile without any protrusion is desirable.

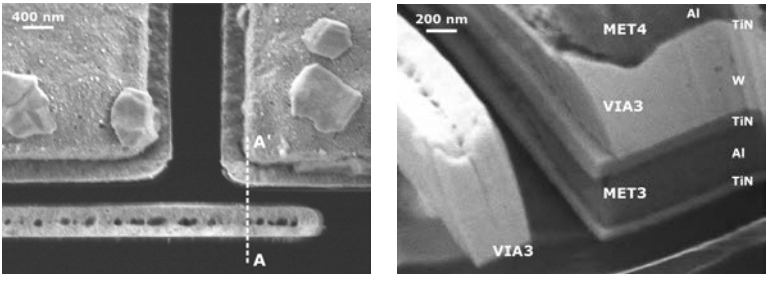
Finally, measured dimensions from SEM imaging, which differ a bit from the ones drawn at the layout, are incorporated in Table 3.1 for comparison purposes. Notice that the expected thickness of the relay was the IMD3 thickness which is 1 μm. However, a thickness of 1.3 μm is achieved basically due to the fact that no MET3 was defined below the relay. We will take advantage of this feature to fabricate contact electrodes likewise the cantilevers in next generation.



(a) (b)

(c) (d)

Figure 3.2: SEM images of fabricated and released 1G 3-T relays of lengths (a) 20 μm, (b) 30 μm, (c) 40 μm and (d) 50 μm.



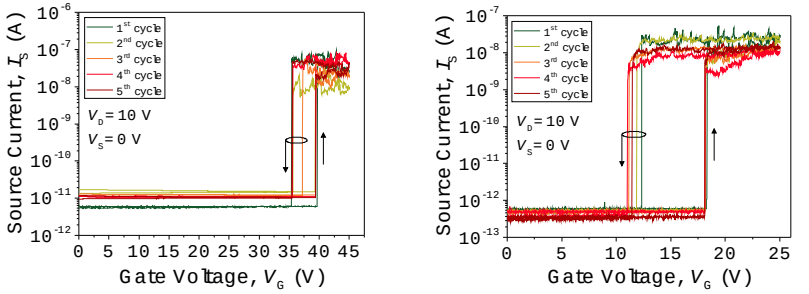
(a) (b)

Figure 3.3: (a) Top view SEM image showing the cut line A-A' where (b) the FIB cut is performed.

3.1.3 Electrical Characterization

I/V Characterization

The switching behavior of the fabricated relays is evaluated using an Agilent B1500A semiconductor analyzer equipped with 3 high-resolution source meter units (HRES-SMU), as described in appendix B. The gate



(a) (b)

Figure 3.4: First five I-V switching characteristics in ambient conditions of relays with (a) length of 20 μm and (b) length of 30 μm.

voltage V_G is swept from 0 V up to a voltage level $V_G > V_{PI}$ and then back to 0 V. The drain-to-source voltage V_{DS} is fixed to 10 V and the source voltage V_S to 0 V; and we record the gate current I_G, source current I_S and drain current I_D simultaneously throughout the sweeping of V_G. An external resistance of 10 MΩ is used to protect the devices form microwelding-induced failure. The chips are in this case exposed to air conditions.

Fig. 3.4(a) and 3.4(b) show five consecutive cycles of hysteretic characteristics of relays with lengths of 20 μm and 30 μm, respectively. We observe two clear states (on and off states) in the switch operation with an on-off ratio $I_{ON}/I_{OFF} > 10^4$. The V_{PI} and V_{PO} voltages are $\sim$ 39.6 V and $\sim$ 35.4 V for the 20 μm-long relay, and $\sim$ 18.3 V and $\sim$ 12.3 for the 30 μm-long relay. The initial on-resistance R_c in both relays is $\sim 10^8$ Ω.

Fig. 3.5 shows the evolution of R_c, V_{PI} and V_{PO} over a total of 20 I-V switching cycles taken in both 20μm and 30μm-long relays. Notice that V_D is kept constant to 10 V. In both relays tested, we observe that V_{PI} is constant and repetitive, which confirms the robustness of the tungsten VIA3. Regarding V_{PO}, it shows a decreasing behavior which leads to a wider hysteretic window. The most critical is that R_c reaches rapidly values over 1 GΩ where starts being unstable.

Fig. 3.6 shows the effect of varying the V_{DS} in a relay 40 μm long. With increasing V_{DS} the beam exercises higher force on the contact and more asperities come into contact. Thus, larger contact area results in higher current level and wider hysteresis window. Note also that the V_{PI} is reduced by also increasing V_{DS} because an extra electrostatic force is

produced at the tip of the relay which also attracts it towards the contact electrode.

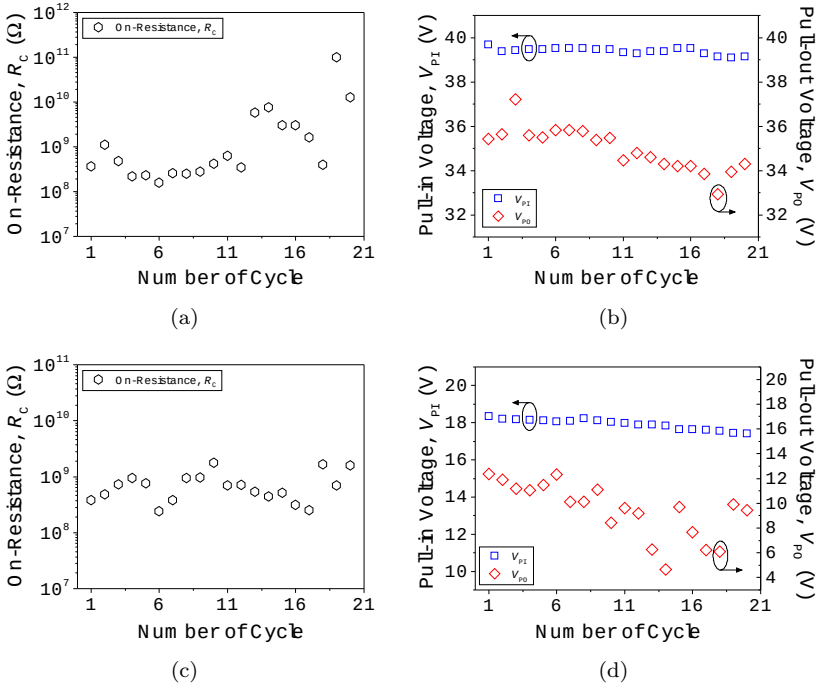


Figure 3.5: Evolution of (a) R_c and (b) V_{PI} and V_{PO} of the 20μm-long relay, and (c) R_c and (d) V_{PI} and V_{PO} of the 30μm-long relay over a total of 20 I-V switching cycles with V_D=10 V. The chips are exposed to ambient conditions.

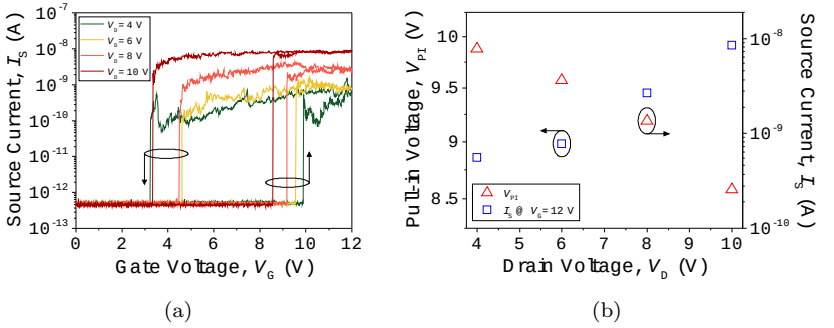
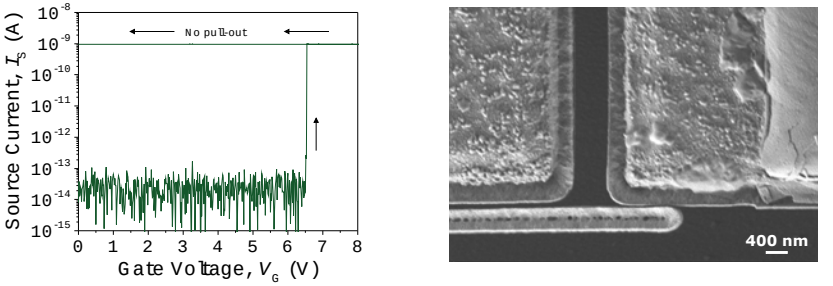


Figure 3.6: I-V characterization in ambient conditions of a relay with a length of 40 μm biased with different V_D voltages.



(a) (b)

Figure 3.7: (a) I-V characteristics in ambient conditions of a relay relay with a length of 50 μm showing stiction after turning off V_G. (b) Top view SEM image of a 50 μm long relay showing stiction.

Fig. 3.7 shows the I-V curve for the relay with a length of 50 μm. This particular relay exhibits the lowest V_{PI}. However, even after the driving voltage is turned off, the relay remains stuck on the contact electrode, thereby being not able to overcome the adhesion forces unlike the rest of the relays. In this sense, a trade-off between low V_{PI} voltage (i.e. low stiffness) and reliable relay device has to be considered.

The experimental V_{PI} measured in a total of 30 devices is summarized in Fig. 3.8 and is also compared to finite element method FEM simulations (CoventorWare MEMS design software) and to an analytical expression which assumes that the cantilever sustains a linear deformation shape deflection [104], which follow as

$$V_{PI} = \sqrt{\frac{0.88kg^3}{\epsilon_0 A_C}} \tag{3.1}$$

where k is the spring constant of the cantilever, g is the gap separation between the movable beam and the actuation electrode, ϵ_0 is the vacuum permittivity and A_C is the actuation area.

Overall, the experimental V_{PI} voltage shows good agreement with the analytical model and the FEM simulations. An absolute error between 0.1 V and 3.54 V is confirmed with the devices tested which may be due to manufacturing tolerances.

Long Cycles of Hot Switching Recorded in Real Time

A long cycling test was performed in order to to explore the lifetime of

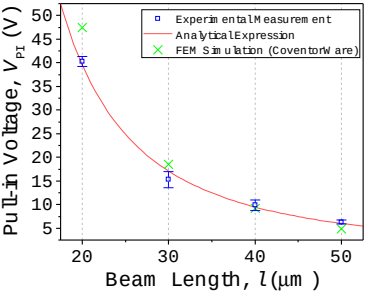


Figure 3.8: Comparison between the measured experimental V_{PI} voltages in relays of length 20, 30 40 and 50 μm vs. an analytical pull-in model [104] and FEM solver simulations performed by means of CoventorWare software. Error bars in the experimental data indicate the standard error between individual samples.

the relays by using the set-up described in appendix B. A 30μm-long relay exposed to air conditions is actuated continuously during 1800 s applying a pulse signal of amplitude 20 Vpp, frequency 1 Hz and rising/falling time 200 ns. V_{DS} is fixed at 10 V and the compliance current limited to 1 μA with an external resistor of 10 MΩ. Then, the source current I_S is amplified using a low noise current preamplifier (LNA SR570) with a gain of 0.1 nA/V and, finally the output voltage V_O is recorded with a conventional oscilloscope. Over 1'800 switching cycles were recorded in real-time as shown in Fig. 3.9. The output amplitude V_O over these long cycles is changing in each cycle, which indicates that the R_{ON} is not the same in each cycle. We attribute this phenomenon to the fact that tungsten is highly susceptible to oxidation [105], which leads to an undesirable increase in the R_{ON} over the device operating lifetime. To address this issue, device testing should be conducted under vacuum to slower native oxide formation or consider alternative contact materials.

Frequency Response and Switching Time

The frequency response of the different relays was measured in ambient conditions as illustrated in appendix B. By biasing the gate electrode with an AC + DC signal through a bias tee and then measuring the capacitively coupled output signal at the source electrode using the Agilent E5100A network analyzer, the resonant frequency f_0 corresponding to the first vibrating mode of the beam was successfully measured for different V_G bias voltages, showing in this way an electro-softening effect from the voltage-dependent electrical stiffness (Fig. 3.10(a)). The experimental f_0 (which correspond to the extrapolated value at 0V), are in accordance with the

values provided by Coventor FEM simulations as summarized in Tab. 3.2.

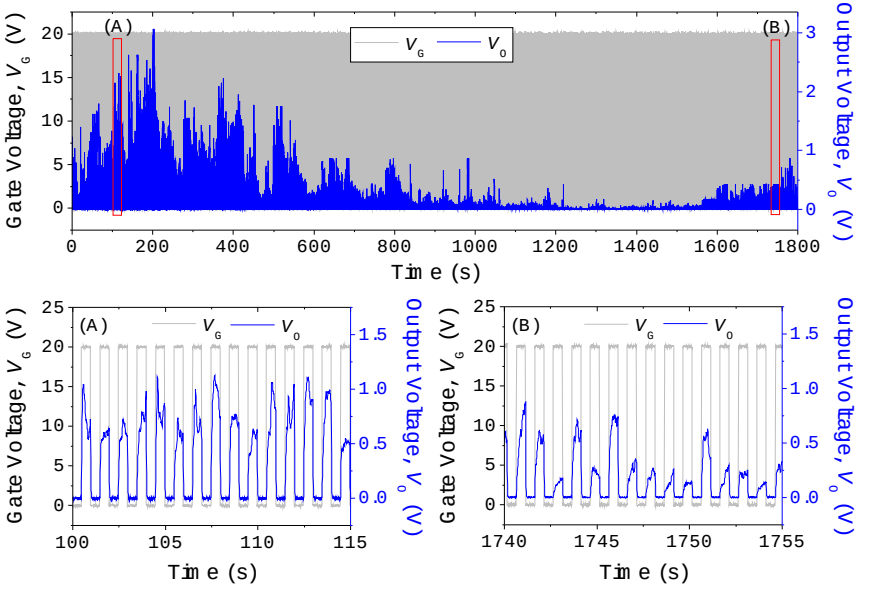
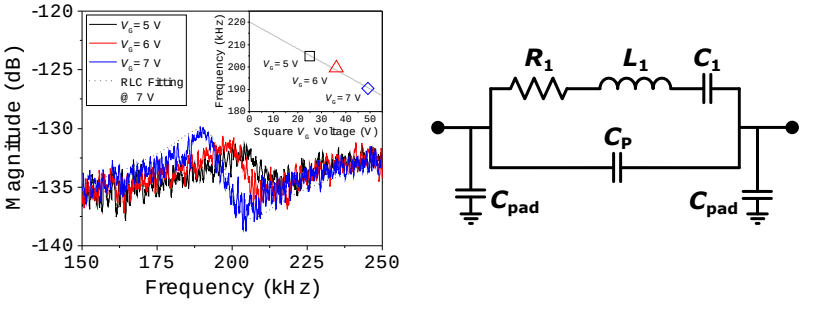


Figure 3.9: Time domain evolution of the actuated switch of length 30 μm. Over 1'800 switching cycles were recorded in real time.



(a) (b)

Figure 3.10: (a) Measured frequency response (in ambient conditions) under different bias voltages (V_G=5, 6 and 7 V) of a fabricated relay 40 μm long. The inset shows the spring softening behavior due to the voltage-dependent stiffness. (b) LCR//C equivalent electrical circuit. Lumped-element values are: $R_m = 500$ MΩ, $L_m = 4.985$ kH, $C_m = 0.135$ fF and $C_{pad} = 1$ pF.

By fitting the experimental response to an LCR equivalent electrical

circuit (see circuit in Fig. 3.10(b)), the Q-factor was found to be 12. According to [45], for beams with small damping ($Q \geqslant 2$) the switching time can be calculated as,

$$t_S \cong 3.67 \frac{V_{PI}}{\omega_0 V_G} \tag{3.2}$$

where V_G and ω_0 are the gate voltage and the resonant frequency in radiants, respectively. Thus, assuming that $V_G = 1.5 V_{PI}$ and taking into account the obtained experimental values of V_{PI} and f_0, the t_S of each relay design can be calculated as is given in Tab. 3.2.

Relay Design	**Beam Stiffness,** k	**Pull-in Voltage,** V_{PI}	**Resonant Frequency,** f_0	**Switching Time,** t_S
l=20 μm	1.601 N/m	47.5 V (Sim.) 40.3 V (Meas.)	932 kHz (Sim.) 812 kHz (Meas.)	557 ns
l=30 μm	0.474 N/m	18.5 V (Sim.) 15.3 V (Meas.)	414 kHz (Sim.) 367 kHz (Meas.)	1.253 μs
l=40 μm	0.200 N/m	9.2 V (Sim.) 9.87 V (Meas.)	233 kHz (Sim.) 220 kHz (Meas.)	2.23 μs
l=50 μm	0.103 N/m	4.875 V (Sim.) 6.30 V (Meas.)	149 kHz (Sim.)	3.482 μs

Table 3.2: Summary of the characterized parameters (V_{PI} and f_0) and the estimated switching time t_S of each relay design.

3.2 Second Generation

This section presents the results obtained in second generation (2G) relays. Throughout the three following subsections, two new features and the subsequent results are described in detail.

3.2.1 Design

The 2G of fabricated relays incorporates two new design features which try to solve the main issues found in the 1G: (i) 5-terminal (5-T) topology and (ii) improved sidewall contact profile. Unlike the 3-T, a 5-T relay which includes two gates and two drains can be actuated bidirectionally

overcoming thereby possible stiction issues in the contacting region. Moreover, an improved sidewall contact profile is expected to be obtained by excluding the MET3 below the VIA3 that forms the contact electrode. An illustration of the designed 5-T layout and its cross-section view is shown in Fig. 3.11.

Same design procedure is followed in the 2G except for the definition of the contact electrode. In this case, no MET3 is defined beneath the VIA3 electrode sidewall so that the VIA3 and METAL3 thicknesses are filled by the W-plug, resulting in a final contact electrode thickness equal to the relay thickness.

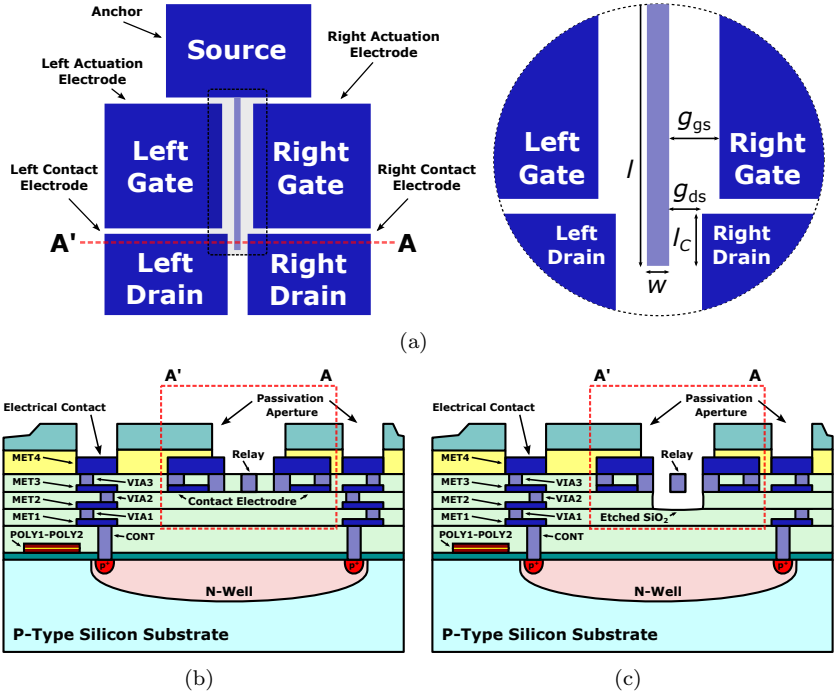
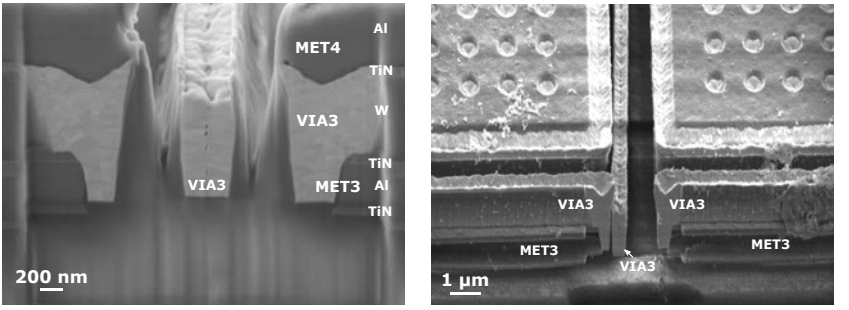


Figure 3.11: (a) Schematic of the 5-T relay design layout which consists of a suspended beam fixed by one side, two actuation electrode and two contact electrodes. A detailed zoom of the tip is shown on the right side. (b) Non released and (c) released cross-section schematic along the red line A'-A in (a).

3.2.2 Physical Characterization

Fig. 3.12 shows SEM images of a FIB cut performed at the tip of a relay which incorporates the two new design features: (i) 5-terminal topology and (ii) modified sidewall contact profile. As expected, the w-via that forms the contact electrode grows downwards as the w-via that forms the relay does, since no MET3 is defined beneath them. In this way, an improved flatter contact area has been achieved compared to the 1G. Notice that as we go from the upper part of the contact profile to the lower part the gap is slightly increased from a value of 410 nm up to 570 nm. Measured width of 491 nm and thickness of 1.363 μm are similar to the 1G, being in this sense reproducible.



(a) (b)

Figure 3.12: SEM images of FIB cuts performed at the tip of a relay with the improved contact sidewall being (a) unreleased and (b) released.

3.2.3 Electrical Characterization

I/V Characterization

The switching behaviour of the 2G fabricated relays is also evaluated using the Agilent B1500A semiconductor analyzer as described in appendix B. A voltage sweep is applied to the left gate while the source and the left drain are fixed to a determined voltage, as in a 3-T topology. The current is then measured in the three terminals. An external resistance of 10 MΩ protects the device against micro-welding induced failure. The right side of the 5-T switch can be tested afterwards.

Fig. 3.13 shows the I/V characterization of a 2G generation 5-T relay of length 20 μm exposed to air conditions. We need first to perform a forming procedure in order to break down the native oxide formed on the Tin/W

surfaces. To do so, the relay is subjected to several on-off cycling cycles with a progressively increased V_{DS} up to achieving an abrupt transition as shown in Fig. 3.13(a). Next, fifteen I/V hysteretic curves are recorded with $V_{DS} = 5$ V as shown in Fig. 3.13(b). The evolution of R_c , V_{PI} and V_{PO} with the number of switching cycles are shown in Fig. 3.13(c) and 3.13(d) respectively. It can be seen that R_c shows an initial value of 15.6 MΩ which is an order of magnitude lower than the R_c found in 1G. However R_c stability degradation is exacerbated compared to 1G. We attribute the exacerbation of the oxidation problem to the fact that since effective contact area is increased with the improved design, the volume of material heated due to current flow increases which accelerates the rate of oxidation exponentially with increasing temperature [105].

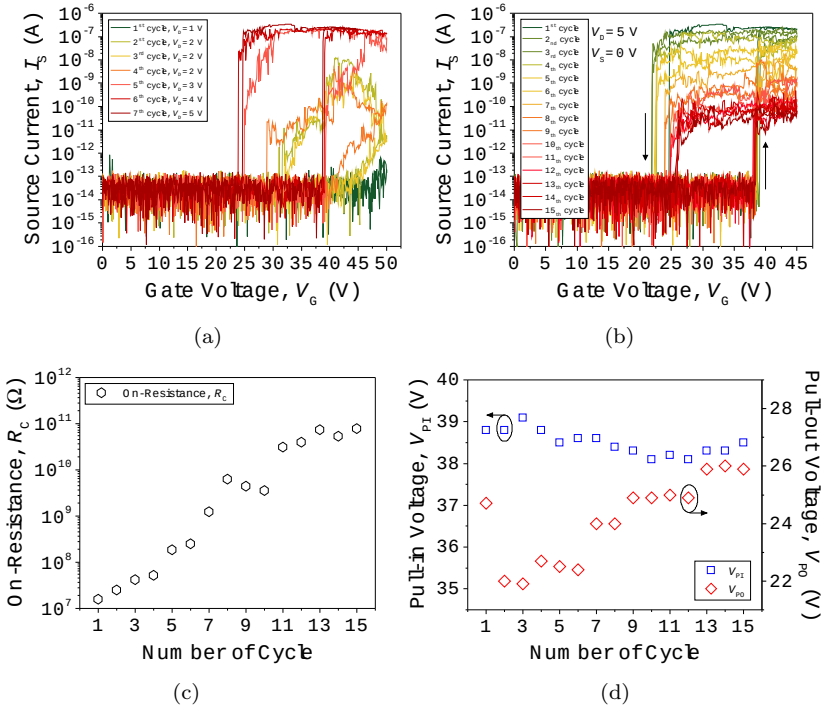


Figure 3.13: I-V characteristics in ambient conditions of a relay with a length of 20 μm: (a) forming procedure, (b) firsts fifteen switching cycles after forming, (c) evolution of the R_c and (d) evolution of the V_{PI} and V_{PO}.

3.3 Third Generation

With the last generation of fabricated relays, an improved contact behavior is obtained through a new feature: a hammer shape. In this section, the device design, physical characterization and experimental results of such a novel hammer-shaped relay are presented and thoroughly analyzed.

3.3.1 Design

The 3G of designed relays are based on a novel hammer shape structure as depicted in Fig. 3.14. In Tab. 3.3, the design parameter values are summarized. Such a hammer-shaped tip allows better contact profile while prevents catastrophic pull-in towards the actuating gate for an in-plane configuration in comparison with previously fabricated BEOL-embedded NEMS relay.

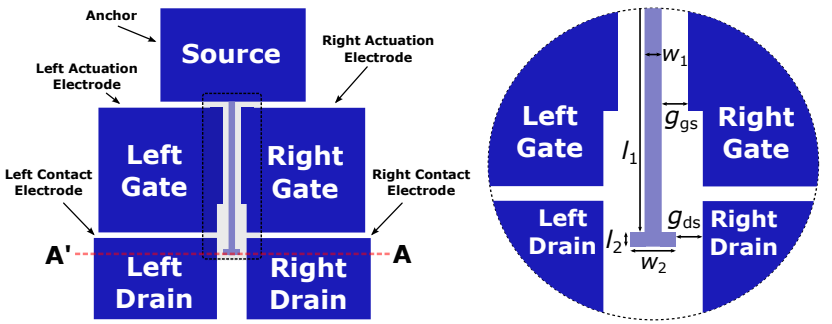


Figure 3.14: (a) Schematic of the 5-T hammer-shaped relay design layout which consists of a suspended beam fixed by one side with a hammer shape at the tip, two actuation electrodes and two contact electrodes. A detailed zoom of the tip is shown on the right side.

		Layout	Measured
beam length	l_1	27.5 μm	27.5 μm
tip length	l_2	0.5 μm	0.5 μm
beam width	w_1	500 nm	556 nm
tip width	w_2	500 nm	1.43 μm
thickness	t	1 μm	1.22 μm
gate-to-source gap	g_{gs}	600 nm	545 nm
drain-to-source gap	g_{ds}	450 nm	425 nm

Table 3.3: Hammer-shaped 5-T relay geometric parameters: layout versus fabricated dimensions.

The spring constant or stiffness of this particular topology under consideration can be written as

$$k = \frac{1}{3}\frac{1}{EI_2}l_2 + \frac{1}{EI_1}(\frac{1}{3}{l_1}^3 + l_1\,{l_2}^2 + l_2\,{l_1}^2) \tag{3.3}$$

where E is the Young's modulus of the material and, I_1 and I_2 are the moment of inertia of the two different segments with rectangular cross section, the beam and the tip respectively

$$I_1 = \frac{{w_1}^3 t}{12} \tag{3.4}$$

$$I_2 = \frac{{w_2}^3 t}{12} \tag{3.5}$$

since $l_1 \gg l_2$, the first term of Eq. 3.3 can be neglected so that the spring constant is reduced to

$$k = \frac{1}{EI_1}(\frac{1}{3}{l_1}^3 + l_1\,{l_2}^2 + l_2\,{l_1}^2) \tag{3.6}$$

Notice that if $l_2 \to 0$, Eq. 3.3 becomes the cantilever spring constant, which is coherent since the hammer tip is being omitted.

3.3.2 Physical Characterization

Hammer-shaped relay designs including both MET4-VIA3-MET3 and MET4-VIA3 contact electrodes were fabricated in the same run (see appendix X for further reference). Fig. 3.15 shows SEM images of the two versions

of fabricated relays. The "hammer-like" tip has a round shape with a radius of curvature of 230 nm. At the center of the tip, W-via dishing is more exacerbated when compared with the w-via dishing along the beam. Cross-sectional views provided by FIB cuts performed at the tip (A-A' in Fig. 3.15(d) and B-B' in 3.15(f)) shows that contact electrodes are fabricated as expected from previously fabricated 1st and 2nd generation lots. Measured dimensions (form SEM images) are summarized in Tab. 3.3, which also show good reproduciblity based on previous results.

3.3.3 Electrical Characterization

The I-V characterization of the hammer-shaped relay was carried out by means of the Agilent B1500A semiconductor analyzer setup described in appendix B, keeping the samples this time inside a home-made vacuum chamber pumped down to 10^{-4} mbar.

Fig. 3.16 shows the firsts 20 I-V curves of a of a hammer-shaped relay with MET4-VIA3-MET3 electrodes which shows immeasurably low off-state leakage, abrupt turn-on/turn-off behavior, and an improvement of 1-2 orders of magnitude in the on-resistance compared with previous generations. The nominal switching voltages for this relay are $V_{PI} = 31.25$ V and $V_{PO} = 20.25$ V.

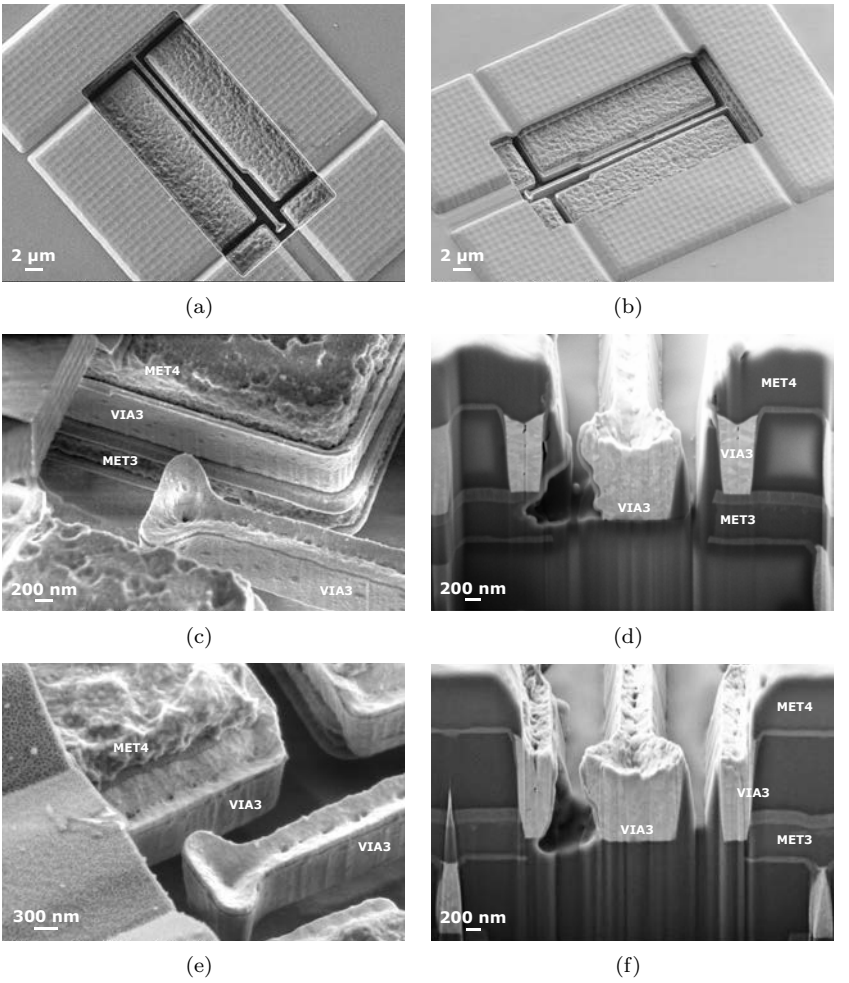


Figure 3.15: SEM images of fabricated and released 3rd generation 5-terminal hammer-shaped relays. (a) and (b) show top views. (c) Lateral view of a relay with MET4-VIA3-MET3 contact electrode. A-A' indicate the location along FIB cut is performed. (d) Cross-sectional view of an unreleased relay with MET4-VIA3-MET3 contact electrode. (e) Lateral view of a relay with MET4-VIA3 contact electrode. B-B' indicate the location along FIB cut is performed. (f) Cross-sectional view of an unreleased relay with MET4-VIA3 contact electrode.

A recent upgrade in the Agilent B1500A semiconductor analyzer allowed us to capture the hyper-abrupt subthreshold slope SS that charac-

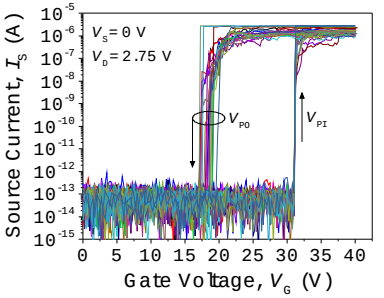


Figure 3.16: Measured first 20 I-V characteristics of a hammer-shaped relay with MET4-VIA3-MET3 contact electrode, showing zero off-state leakage and abrupt switching behavior with improved on-resistance.

terize NEM relay technology. With a very fine voltage step size (2 mV), a SS of only 285 μV/dec was measured as shown in Fig. 3.17.

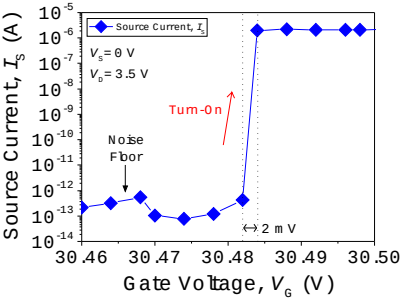
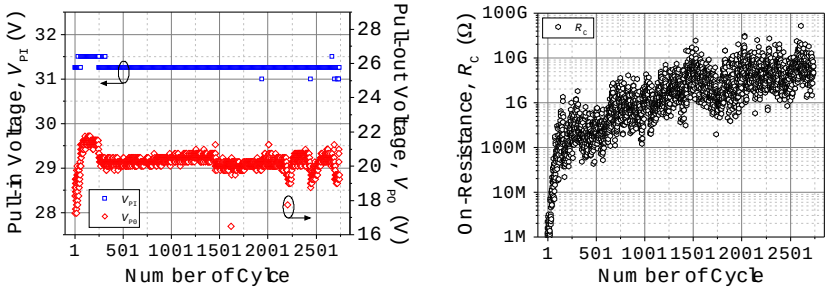


Figure 3.17: Measured I-V characteristic with a very fine (2 mV) voltage step used to examine the turn-on characteristics. Note that I_{DS} is at the noise floor level in the off-state and switching is very abrupt, with 7 orders of magnitude jump for a 2 mV step, leading to a SS of only 286 μV/dec.

A total of 2800 I-V curves where taken to investigate the evolution of V_{PI} and V_{PO} as shown in Fig. 3.18(a). The results shows a very stable V_{PI} of 31.25 V with a variation of only $\pm$0.25 V, which confirms the robustness of the structural material.

Fig. 3.21(b) shows the evolution of the R_c over these 2800 cycles. In contrast with previous relay generations, an improved initial R_c of $\sim$ 1 MΩ with a reduced V_{DS} of only 2.75 V is obtained. R_c degradation is not as exacerbated as when exposed to room ambient conditions, which indicates much slower native oxide formation in low oxygen environment (at $\sim 10^{-4}$ mbar); although R_c shots up from 1 MΩ to 100 MΩ in $<$ 200 cycles. These

measurements therefore confirm that native oxide continuously forms at the contact and needs to be broken down.



(a) (b)

Figure 3.18: Evolution of the (a) V_{PI}, V_{PO} and (c) R_c over 2800 I-V cycles.

A more thorough investigation of the contact behavior is conducted by measuring the $I_{DS} - V_{DS}$ characteristic of the hammer-shaped relay as shown in Fig. 3.19. For this purpose, the relay is first brought into contact with $V_G = 45$ V. Then, the V_{DS} is swept from 0 to 5 V and the current I_{DS} flowing through the contact is measured in both source and drain terminals. A first region in which I_{DS} current shows an exponential (tunneling) dependence due the presence of native dielectric oxide is observed and, after a hard dielectric breakdown event, an ohmic behavior is achieved as shown in Fig. 3.19(a).

Schottky emission is one of the most observed conduction mechanism in dielectric films, in which if the electrons can obtain enough energy provided by thermal activation, the electrons in the metal will overcome the energy barrier at the metal-dielectric interface to go to the dielectric. The expression of Schottky emission is

$$I = A^* \cdot T^2 \cdot a_c \cdot \exp\left\{ \frac{-q\phi_b}{k_B T} + \sqrt{\frac{q}{4\pi\epsilon_0\epsilon_r t_{ox}}}\sqrt{V} \right\} \tag{3.7}$$

where I is the current, A^* is the effective Richardson constant, a_c is the effective contact area, ϕ_b is the barrier height, V is the potential across the dielectric, t_{ox} is the oxide thickness, q is the electron charge, K_B is the Boltzmann's constant, ϵ_0 and ϵ_r are the vacuum and relative dielectric permittivity, and T is the absolute temperature.

Eq. 3.7 can be linearized as follow

$$\ln(I/T^2) = R(T) \cdot \sqrt{V} + S(T) \tag{3.8}$$

$$R(T) = \sqrt{q/4\pi\epsilon_0\epsilon_r t_{ox}} \tag{3.9}$$

$$S(T) = -q\phi_b/k_B T + \ln(C) \tag{3.10}$$

where $R(T)$ and $S(T)$ are the slope and y-intercept, respectively.

The tunneling region in Fig. 3.19(a) is re-plotted using Eq. 3.9 in terms of $\ln(I/T^2)$ versus $V^{1/2}$ as shown in Fig. 3.19(b). As can be seen, the experimental data shows a straight-line characteristic with an slope $R(T) = 6.08$ and an y-intercept $S(T) = -42.46$, confirming thereby Schottky emission when the electric field has increased sufficiently ($V_D{}^{1/2} > 0.5$). The extracted ϕ_b is 1.32 eV, which is coherent with the reported ones **??**.

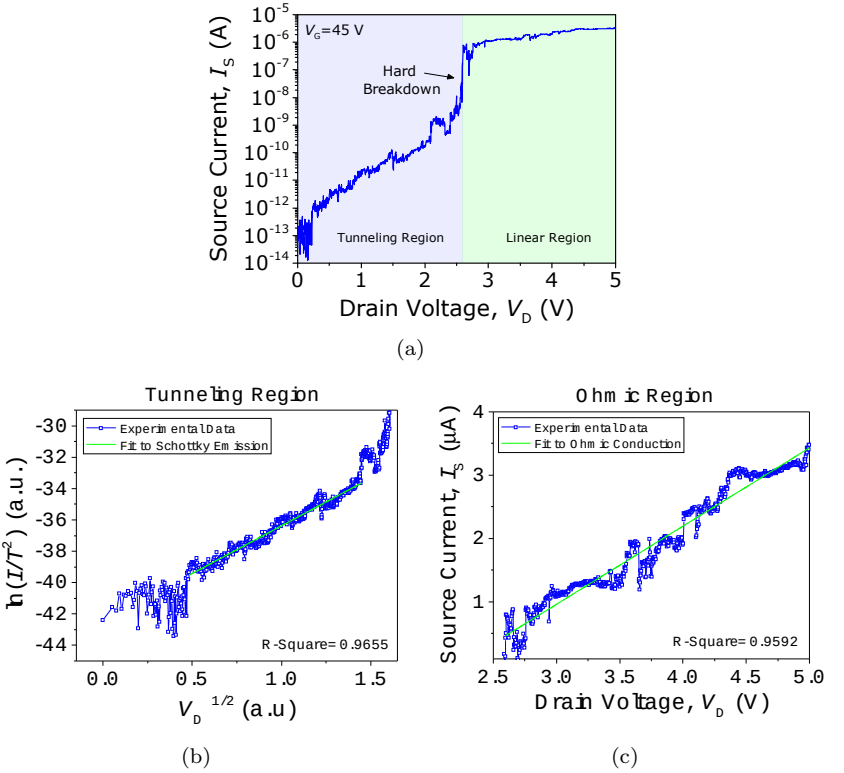


Figure 3.19: Measured $I_{DS} - V_{DS}$ characteristic of the hammer-shaped relay with $V_G = 45$ V showing a transition between tunneling to ohmic conduction.

When applying a high drain voltage ($V_D \sim 3$ V), a drain current spike is detected, indicating native oxide breakdown. After this hard dielectric breakdown event, an ohimc behavior is observed as shown in Fig. 3.19(c). It should be noted that measurements conducted with high drain bias ($V_D > 3$V) increase the probability of welding induced failure, as I_{DS} levels gets too high. It is therefore important to find the optimal drain voltage that would be able to minimize native oxide formation, but is still low enough to not cause welding over the device lifetime. $V_D \sim 3$ V is optimum for this type of contact.

Fig. 3.20 shows the firsts 20 I-V curves of a of a hammer relay with in this case MET4-VIA3 electrodes which shows an abrupt turn-on/turn-off behavior with sharp V_{PI} and V_{PO} events of 32.8 V and 26.6 V.

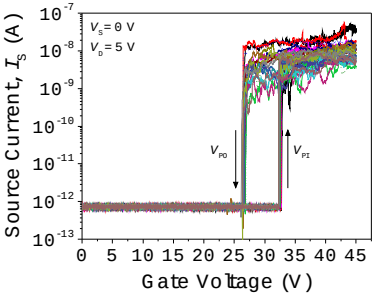
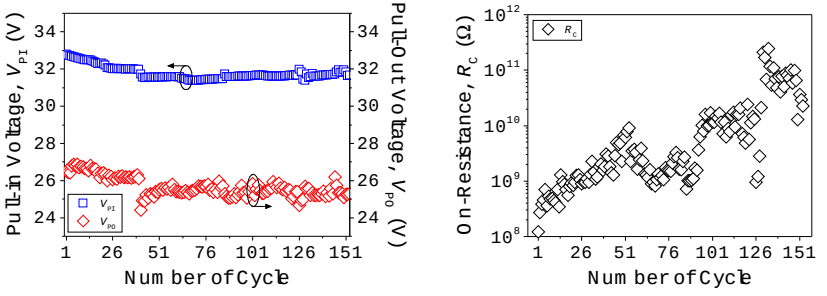


Figure 3.20: Measured first 20 I-V characteristics of a hammer-shaped relay with MET4-VIA3 contact electrode, showing zero off-state leakage and abrupt switching behavior.



(a) (b)

Figure 3.21: Evolution of the (a) V_{PI}, V_{PO} and (c) R_c over 2800 I-V cycles.

Fig. 3.21 shows the evolution of the R_c, V_{PI} and V_{PO} over 150 cycles. In this case, the initial R_c worsen to 10^8 Ω, similar to previous generations.

Then, R_c rapidly shots up to $> 10^{11}$ Ω over these 150 cycles. The V_{PI} resulted to be also very stable, having a median of 31.78 and an absolute error of ±0.71 V.

3.4 Post-CMOS Coating Process

In order for relays to have an extended lifetime, R_c should be stable within a certain operating range. The primary cause that fabricated relays have shown to lead to R_c instability is the formation of an insulating native oxide at the contacting surfaces. Therefore, a contacting material that either does not oxidize in ambient air or forms a conductive native oxide is desirable for relay technology. In this section, potential candidates for overcoming the present issue are identified and examined. Next, a post-CMOS coating process flow for covering fabricated relays with alternative contact materials is proposed and described in detail.

3.4.1 Material Selection

Several works have shown contact performance improvement by covering the contacts with platinum (Pt), titanium nitride (TiN) and ruthenium (Ru) [97]. These metals are selected due to their high melting temperature and stability in air and oxidizing environments. Also, due to its availability in clean room facilities. Tab. 3.4 summarizes relevant bulk material properties for metals under consideration. As a reference, W is also listed in Tab. 3.4. W-via was in fact quite attractive as the contacting material for building BEOL-embedded relays since it is the metal with highest known melting point, minimizing potential micro-welding and contact vaporization issues [106]. However, W oxidizes in air and forms a native oxide layer that consists of WO3 and other WOx compounds [107]. For this reason, the selected candidates (Pt, TiN and Ru) will be examined in depth following.

Platinum is a widely used metal in MEMS applications due to its high chemical resistance, relatively high temperature stability and high Young's modulus [108]. It can sustain high current conduction for long periods of time with relatively low contact resistance and it can provide improved reliability [74, 80] due to its high hardness when compared to widely used gold (Au) or aluminium (Al) structures. Pt forms PtO and PtO_2 in air at room temperature [109], which are semi-conductive compounds with resistivity values of $\sim 10^{-5}$ Ω·m and $\sim 10^{-2}$ Ω·m for PtO and PtO_2

respectively [110]. In addition, Pt is resistant to liquid and vapor HF, which makes the process more flexible in terms of structural and sacrificial layer material choices [74].

Ruthenium has shown to be a very promising contacting material for relay-based logic circuits [31, 97] thanks to its high melting point, high hardness, and its capacity of growing a thin conductive oxide (RuO_2). Ru has also been investigated in advanced CMOS manufacturing processes [111] which can be leverage to implement miniaturized BEOL-embedded relays with the excellent properties of Ru contacts.

	W	**Pt**	**Ru**	**TiN**
Resistivity [nΩ·m]	55	117	71.6	25-160·10^3
Melting Point [°C]	3390	1773	2500	2950
Young's Modulus [GPa]	410	168	447	251
Mass Density [g/cm^3]	19.3	21.4	11.56	5.22
Brinell Hardness [GPa]	350	40	193	-
Native Oxide	WO_x	PtO_x	RuO_2	TiO_2

Table 3.4: Bulk material properties of selected metals.

Titanium nitride is an extremely hard ceramic material often used as a protective coating material for its high melting point (~ 2950 °C), relatively low resistivity ($\sim 50 - 150$ pΩ·cm), extreme hardness, excellent inertness and thermodynamic stability. Such excellent properties have made TiN to be a very interesting candidate for many microelectronics applications. For instance, thin film layers of TiN are common used in CMOS manufacturing processes as a diffusion barrier to block the diffusion of the metal into the silicon, as an anti-reflective coating for the metal photolithography as well as an etch stop for the subsequent via formation [99].

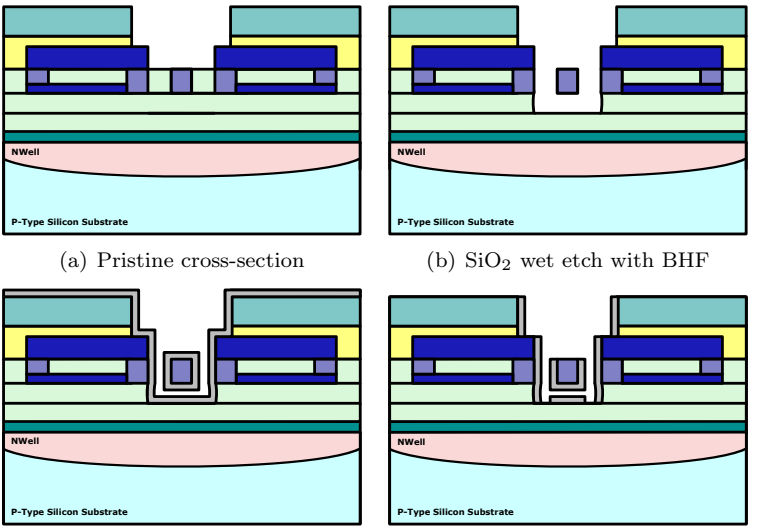
TiN has also been intensely investigated as a structural and contact material for implementing NEMS switches. W. W. Jang *et al.* fabricated a cantilever-type NEM switch with a 15-nm-thick suspension air gap and a 35-nm-thick TiN beam by using a conventional CMOS process [62]. M. Ramenazi *et al.* showed an important reliability improvement of a poly-SiGe nano-relay by coating the relay with a TiN thin film [112]. M. Shavezipur *et al.* demonstrated contact improvement by hollowing the tip of a relay, which leads to a flexible sidewalls formed also from a thin film TiN layer [113]. All of them utilizing TiN have demonstrated excellent on-off current characteristics and repetitive switching operation.

In fact, the fabricated relays using VIA3 layer are composed of mainly W but also of a thin film of TiN on the walls as has been explained in

detail in chapter 2. Despite the promising precedents of TiN, measured results in air conditions has shown a rapid on-state resistance degradation. The use of alternative contacting material such as Pt and Ru that offers stable R_c is important to realize the full potential of relay technology.

3.4.2 Coating Process Description

Pt and Ru have been identified as the two selected candidates for coating the fabricated relays and thus improve the contact stability. The post-CMOS coating process carried out for incorporating such materials into the fabricated relays is shown in Fig. 3.22. Starting from a pristine sample, the structures are first released in BHF as explained in chapter 2. Next, a 50-nm-thick layer of Pt or Ru is deposited all over the sample. Two different deposition methods were used: sputtering and evaporation. Finally, an anisotropic argon sputter etch (RIE Oxford 80Plus: PSource=1000 W, Pchuck=100 W, p=1 Pa, flow=20 sccm Ar, time=60 s) is performed in order for the Pt to be removed from the bottom and top surfaces, leaving thereby the sidewalls intact.



(a) Pristine cross-section

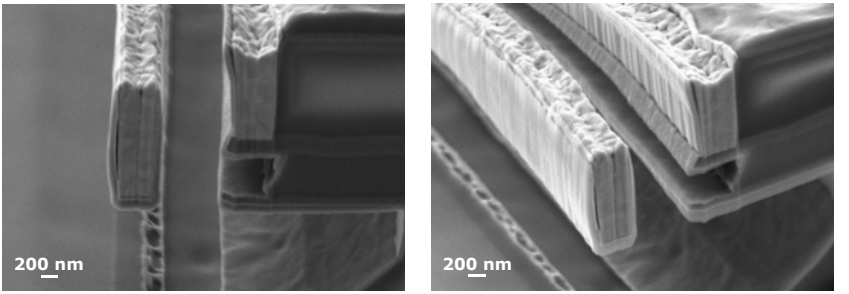
(b) SiO_2 wet etch with BHF

(c) Pt/Ru deposition

(d) Pt/Ru directional etch, leaving Pt/Ru on sidewalls only

Figure 3.22: 2-D cross-sectional view of process flow used for coating fabricated relays with Pt and Ru.

Fig. 3.23 shows SEM images of FIB cuts performed at the tip of a Pt-coated relay by sputtering. As it can be clearly seen, bottom and top surfaces have been removed whereas the sidewalls are intact. Notice that the sputtering method resulted quite conformal, covering the entire underetch. This fact led the device terminals to be short circuited as it was electrically checked, impeding the proper switch operation.



(a) (b)

Figure 3.23: SEM images of FIB cuts performed at the tip of a Pt-coated relay by sputtering after RIE process. (a) Frontal view and (b) lateral view.

A less conformal deposition method was then explored in order to overcome the former issue. Fig. 3.24 shows SEM images of a FIB cut performed at the tip of a relay in which a 50-nm-thick layer of Pt was deposited by evaporation. Since evaporation is not as conformal as sputtering method, the underetch below the electrode was not covered as can be seen in Fig. 3.24(b). However, the thickness of the deposited Pt on the sidewalls is much less than the deposited on the bottom and top surfaces. In spite of it, SEM images after RIE process shows there is still a thin layer of Pt on sidewalls which might be thicker enough to prove contact improvement (see Fig. 3.24(c) and 3.24(d)). Unfortunately, testing results showed that device terminals were also short circuited between them, impeding again the proper switch operation.

It is worth mentioning that a different method than the described formerly was employed first which unfortunately yielded poor results. First, 1-μm thick photoresist layer was deposited and patterned with a Durham Magneto Optics LTD laser micro writer. The photolithography was realized in the ICMAB (CSIC). Next, the samples were released with BHF and sent to Oxford Boston to deposit Ru and Pt by ALD. Finally, the last step which consisted in the metal lift-off patterning did not succeed. FIB cuts performed on both samples showed that the samples were only

covered by the deposited metals. Any trace of photoresist was not found in the samples which led to the impossibility of pattering the deposited metal.

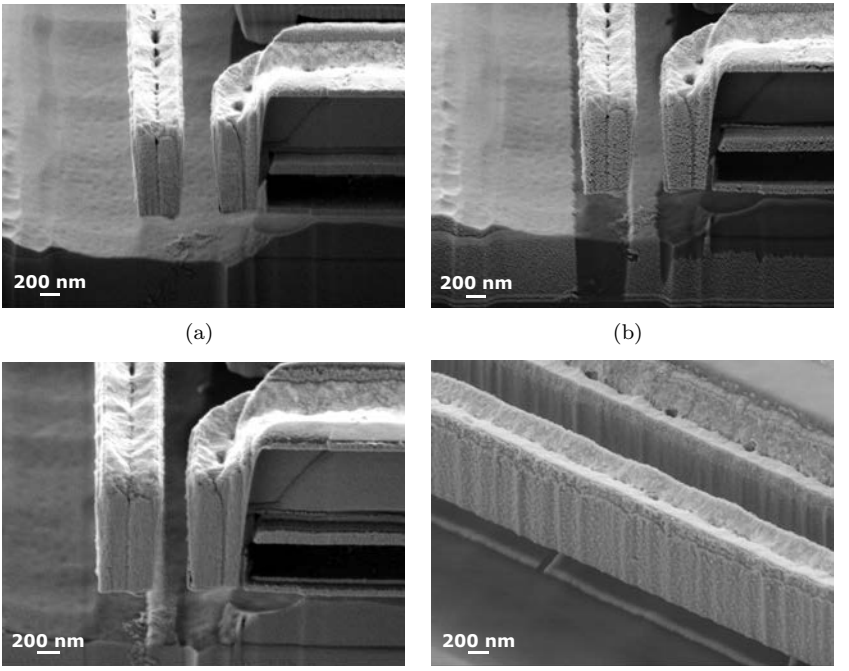


Figure 3.24: SEM images of FIB cuts performed at the tip of a Pt-coated relay by evaporation. (a) Pristine corss-section. (b) Evaporation. (c) Evaporation + RIE (frontal view) (d) Evaporation + RIE (lateral view).

3.5 Dynamic Properties under Nonlinear Tapping Mode

One of the main difficulties of M/NEM relay technology is to achieve a reliable device. We need the device endurance to exceed 10^{16} cycles, so that a relay-based microcontroller for embedded sensor applications could operate reliably for ten years at a clock frequency of up to 100 MHz [9]. Therefore, the cycle lifetime of these switching devices becomes one of the most important parameters to be characterized and further improved

before being commercialized.

The lifetime characteristics of microrelays can be evaluated, generally, in two ways. The first is the so-called cold-switching test, in which the switches are continuously actuated with no current flowing through the contact since there is not any voltage difference applied. Thus, this test focuses on evaluate uniquely mechanical degradation phenomena such as pitting and hardening. Pitting and hardening occur when two metals make contact repeatedly at the same location [55]. The repeated actuation create cavities at the surface which can be filled with corrosion products over time causing the operation failure [114]. Complementarily, the second one is the hot-switching test, in which the switches are also continuously actuated but current flows through the contact since a voltage difference is applied. In this case, in addition to having mechanical degradation, electrical failure mechanisms also may occur such as arcing, material transfer, and localized high temperature spots [55, 114].

Commonly, switches are actuated by means of a slow quasi-static or kHz pulsed testing over long cycles in a hot or cold-switching scenario [115]. However, switches can also be actuated in tapping mode, i.e., driving them near its resonance and making its vibrational amplitude large enough to tap or contact periodically the contact electrode [116–119]. Operating relays in such a way offers a clear advantage over pulsed quasistatic testing as pointed out in [116]: it is possible to approach the device intrinsic speed ratio allowing an accelerated assessment of MEMS relay lifetime characteristics.

Tapping mode has been reported in MEMS devices using electrical [117, 118] and optical [116, 119] transduction set-up's. In [117], Quévy *et al.* measured capacitively the "linear" tapping mode of a silicon free-free beam, i.e., specifically the case when the displacement is large and the tapping occurs in the linear frequency response region. In [118], Lin *et al.* presented an impact micromechanical switch operating in such a "linear" tapping frequency response regime known as "resoswitch" for implementing switched power amplifiers and converters. Besides, He *et al.* also measured the linear tapping mode in silicon carbide relays in cold-switching conditions using an interferometric optical system [116]. On the other hand, dealing with tapping that occurs in the nonlinear frequency response region, Zhang *et al.* measured such a phenomenon optically using a micro-scanning-laser-vibrometer system in a cantilever [119].

In this section, we present a fully electrical resonant cold-switching characterization of a three-terminal tungsten NEM relay under nonlinear conditions based on the capacitive detection of its tapping mode, which

none of the previous works has dealt with. One of the key benefits of the nonlinear tapping behavior is that the sensitivity of such a response to variations in interaction parameters can be harnessed to establish a change on the mechanical adhesion between the NEM relay and the contact electrode due to the change on the hysteretic cycle of the frequency response (right bifurcation [119]). Investigations of the nonlinear tapping mode were also previously performed in dynamic-force-microscope (DFM) applications using piezoelectric actuation and optical external setups [120]. We show that the capacitive readout offers simplicity against the complexity of an optical setup, and that it provides on-chip testing capabilities, which will be an advantage for fully-integrated NEM relays. To do so, the evolution of the on-state contact resistance and the variations of pull-in and pull-out voltages at certain parts of the test are studied by measuring I-V curves and frequency responses when we drive our device in such a nonlinear dynamic impact regime over long cycles.

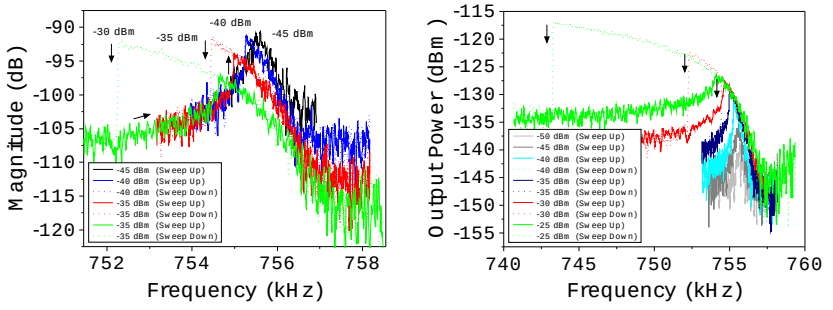
3.5.1 Nonlinear Tapping Mode: Electrical Characterization

The measurement setup for probing the dynamic properties of the relays operated in the nonlinear tapping mode is illustrated in appendix B. The switch is electrically excited through the gate electrode by combining a DC voltage V_G and a RF signal V_{RF} from the Agilent E5100A network analyzer. Notice that V_G is polarized to a fixed voltage during the entire experiment. Both source and drain electrodes are forced to ground. Then, the motional current of the cantilever V_{OUT} is capacitively detected at the source electrode. Measurements are carried out inside a vacuum chamber, pumped down to an initial pressure of 10^{-5} mbar.

First, we drive the cantilever with a very small RF signal V_{RF} of -45 dBm, maintaining V_G to 25 V during the entire experiment. In this case, the magnitude of the frequency response shows a linear behavior as can be observed in Fig. 3.25. The extracted Q in the linear regime is 1700.

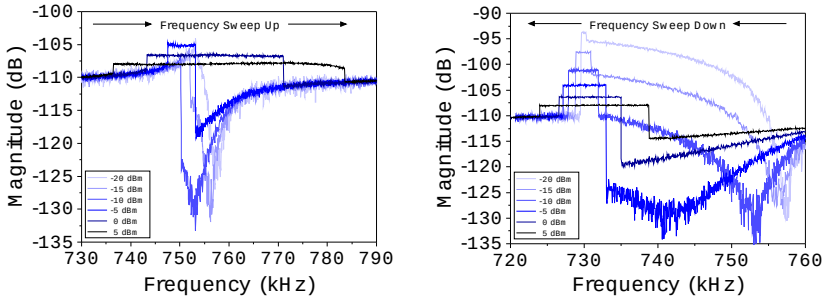
Increasing V_{RF} to -40 dBm, the magnitude of the frequency response starts to curve leftwards due to the presence of quadratic and cubic nonlinearity [121]. Then, as the drive level V_{RF} increases, the nonlinear contribution also increases, eventually showing hysteresis (see -35 dBm in Fig. 3.25, with a hysteretic cycle around 1 kHz). Notice that although the magnitude (in dB) saturates at -92 dB, the amplitude signal and thus the displacement of the cantilever is increased as the actuation power is increased even in the nonlinear regime (see Fig. 3.25(b) in which we use

dBm instead of dB to clarify this point).



(a) (b)

Figure 3.25: Experimental magnitude-frequency responses for different V_{RF} powers showing the transition from the linear regime to the start of the nonlinear regime. (a) Magnitude in dB showing linear behavior at -45 dBm, nonlinear behavior with no hysteresis at -40 dBm, and increased hysteretic cycle at -35 dBm and -30 dBm.(b) Magnitude in dBm to show the increased cantilever movement with higher actuation power.



(a) (b)

Figure 3.26: Experimental magnitude-frequency responses for different V_{RF} powers showing the nonlinear tapping regime. The flattened plateau takes place at different frequency regions (a) for the frequency sweep up and (b) for the frequency sweep down.

Increasing significantly V_{RF}, the vibration amplitude of the cantilever is large enough to impact against the drain electrode. At this moment, the reached regime is called nonlinear tapping mode and the maximum amplitude of the electrical frequency response starts to be limited, showing a flattened plateau for a defined frequency region as shown in Fig. 3.26. It should be noted that the phenomenon takes places at different frequency

regions for both frequency sweep up and down responses under different actuation powers (Fig. 3.26(a) and 3.26(b) respectively). In the frequency sweep down response, the amplitude starts to flatten at -20 dBm while it does not occur in the frequency sweep up response until -5 dBm. Note also that the higher the driving voltage, the wider the flat contact region.

In fact, the displacement under dynamic actuation at the resonance frequency would be, roughly, Q times smaller than the displacement under static actuation [118]. In our case, the tungsten relay of length 20 μm presents a V_{PI} equal to 44 V and a Q-factor of 1700, with V_G equal to 25 V. Computing the dynamic and static electrical actuation forces to achieve the same displacement (i.e., to close the switch), the needed actuation would shrink from this 44 V to only 23 mV, which is very close to the experimental actuation voltage, causing the tapping of the relay against the contact electrode (-20 dBm, which is 22.5 mV).

3.5.2 Long-Driving Tapping Test

Our purpose here is to bring the relay in the nonlinear tapping mode over long cycles and study the switching dynamics of the presented switch. We evaluate the changes produced in the on-state contact resistance and the characteristic switching voltages throughout such a measurement. To do so, we fix V_{RF} to 5 dBm and we set the driving frequency to 738 kHz, maintaining V_G to 25 V. We select these operating conditions because the flat region of both frequency sweep up and down responses overlap. Thus, we ensure there will be contact in each resonant motion cycle, since the same magnitude is obtained for the sweep up and down in the selected frequency. Then, we drive the cantilever for 16'000 seconds (which is more than 4 hours) at the fixed frequency using the zero-span mode (span=0 Hz) of the network analyzer under the former mentioned conditions as illustrates the same Fig. 3.27(a). In this way, the switch operates more than 10 billion (10^{10}) of cycles in tapping mode (1.35 μs per cycle for more than 4 hours of test) without failure, as reveal the I-V curves and the frequency responses showed in Fig. 3.27(b) and 3.27(c) respectively. The I-V curves and also the frequency responses are taken at the beginning of the cold-switching test, in the middle and at the end of the test as indicate the letters (A), (B), and (C).

The I-V curves shown in Fig. 3.27(b) were obtained by sweeping up and down V_G from 0 to 50 V and setting the V_D at 5 V (with a semiconductor analyzer Agilent B1500A equipped with four high-resolution HRES SMU as described in appendix B). We clearly observe, by one hand, a consistent

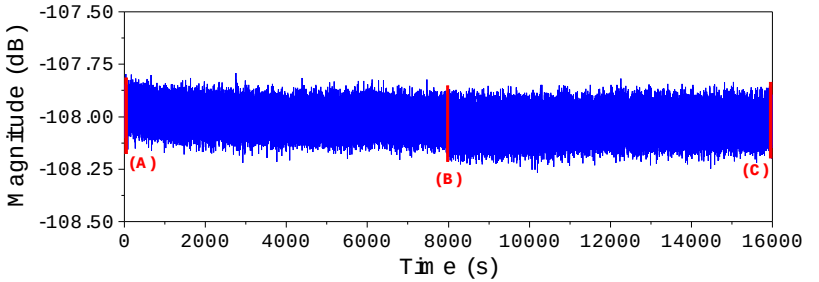
and repetitive pull-in voltage of 44 V and, that the pull-out voltage is slightly decreased, consequently causing an increasing hysteresis window. On the other hand, the on-state resistance, which is initially around 2 GΩ and very unstable, is reduced to 735 MΩ, becoming much more stable after the long cycling test (see inset in Fig. 3.27(b)). These results can be explained if a change on the contact material surface is considered. In fact, it is well known that tungsten is a highly resistant material to mechanical wear and tear [55] which is corroborated with the repetitive measured pull-in voltage (no change in the elastic properties of the cantilever beam). By contrast, tungsten is chemically reactive and grows easily an insulating native oxide thin film in air [55]. This oxide increases the expected on-resistance and can change the adhesion forces between the relay and the contact electrode considering that the adhesion energy strongly depends on the surface termination [40]. As the pull-out voltage is dependent on the adhesion forces [122]

$$V_{PO} = \sqrt{\frac{2(kg_{ds} - F_A)(g_{gs} - g_{ds})}{\epsilon_0 A_c}} \tag{3.11}$$

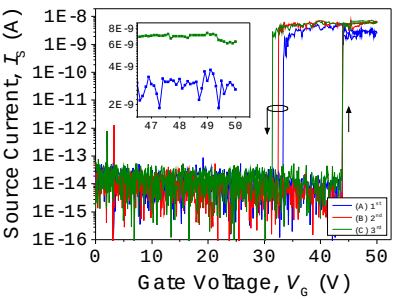
where k is the spring constant of the cantilever, g_{gs} is the actuation gap, g_{ds} is the contact gap, F_A is the adhesion force, A_C is the coupling area and ϵ_0 is the vacuum permittivity; a reduction of the pull-out voltage means that the adhesion forces between the source and the drain of the NEM relay become greater requiring less electrical field (less voltage between source and gate) to switch off the relay. These surface changes have been previously reported. For example, Chen et al [105] needed to actuate their fresh switches during 10^4 cycles at 100 Hz to break down the formed native oxide to achieve a stable contact resistance. In our case, the long tapping test performed also in vacuum conditions shrinks the contact resistance and the pull-out voltage, which confirms that the presented tungsten relays also has such an insulating film in their surfaces and that, it is broken down over the cold-switching tapping cycles.

Regarding the results of the measured frequency responses during the tapping test shown in Fig. 3.27(c), we clearly observe that there is an abrupt transition that reaches the flat region when sweeping the frequency up and down. Also, it can be observed that there is a perfect overlap in the measured responses along the test offering the same hysteretic behavior with a flattened plateau at 738 kHz. The only appreciable difference is in the right boundary of the discontinuity of the frequency sweep up. There, the relay is released from the drain contact at different frequencies. In fact,

as pointed out by Zhang *et al.*, the left boundary is mainly devoted to the quadratic and cubic nonlinearity due to the electrostatic softening while the right boundary is limited by the mechanical tapping [119]. This shift in the right frequency boundary can be also explained due to a change of the adhesion forces between the cantilever and the contact electrode during the tapping test, which is also in accordance with the previous discussion of the pull-out voltage change.



(a)



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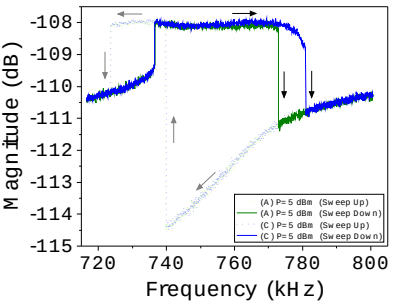


(c)

Figure 3.27: Long-driving tapping test. (a) Measured magnitude versus time during the tapping test. Letters (A), (B) and (C) indicate the part of the test were I-V curves and frequency responses were taken. (b) I-V curves (with $V_D = 5$ V). Inset shows a zoom of the I-V curve during contact before (blue line) and after (green line) the long-driving tapping test. (c) Frequency responses (with $V_{RF} = 5$ dBm and $V_G = 25$ V).

In summary, we have electrically characterized the nonlinear tapping mode behavior of a three-terminal tungsten CMOS-NEM relay revealing a previously non-reported double-side frequency dynamic-contact characteristic. To do so, we have actuated electrostatically the switch near its

resonance and then, by increasing the driving power we have caused that the tip of the cantilever to make contact periodically against the contact electrode. Simultaneously, the dynamic motion of the relay has been sensed by capacitive detection. In this way, we have demonstrated that the presented device can stand easily more than 10 billion of cold-switching cycles. Furthermore, I-V curves and frequency responses have been taken during the switching test. By one hand, the measured I-V curves have shown a consistent and repetitive pull-in voltage, a slight decrease of the pull-out voltage, and a diminution in the contact resistance up to 735 MΩ being much more stable than the initial 2 GΩ. On the other hand, the frequency responses have shown a non-variant nonlinear tapping phenomenon, in which an abrupt transition and consecutively a flattened plateau are produced when the vibration amplitude of the switch is large enough to contact dynamically against the contact electrode. These frequency responses show a decrease in the right boundary of the discontinuity of the frequency sweep up. The resistance change along with the decrease in pull-out voltage and right frequency corners are attributed due to the fact that the superficial oxide is broken down due to the continuous tapping on the contact region. After all the tests mentioned formerly, the device is still alive without showing stiction or any other kind of failure mechanism.

Chapter 4

Torsional Composite Microelectromechanical Relays

Chapter 4 presents the results involving torsional composite MEM relays. For each different relay design, a layout scheme is depicted, and the physical and electrical characterization are described and thoroughly discussed. We first show the results regarding the more conservative approach: the torsional free-free (TFF) relay based on simple tungsten beams. Next, we show the results concerning the seesaw relay. Parallel to the main thread of this thesis, MEMS resonators based on the VIA3 platform were also developed as a result of the work done. These resonators has the particularity of exhibiting two symmetric resonances, the torsional mode and the vertical mode. In this line, we eventually show the use of such developed dual-mode resonators for implementing single-resonator dual-frequency oscillators.

4.1 Torsional Free-Free Relay: Design and Fabrication

Figure 4.1 shows the relay design that consists of one main beam anchored by two torsion beams (called source, S), defined using tungsten VIA3 layer, which allows the ends of the main beam move up and down by actuating electrostatically the underneath located gate electrodes (G_R and G_L) of MET2, which are sandwiched layers of titanium nitride-aluminium-titanium nitride (TiN-Al-TiN). Such mentioned endings are made of a stack of MET4, VIA3 and MET3 layers and make contact with the drain electrodes (D_R and D_L) also of MET2. Thereby, the contact gap T_{CON}, which is the distance that separates MET3 and MET2, is determined by the technology to be nominally 1 μm. The design parameter values and the material properties of the switch are listed in Table 1 and 2, respectively.

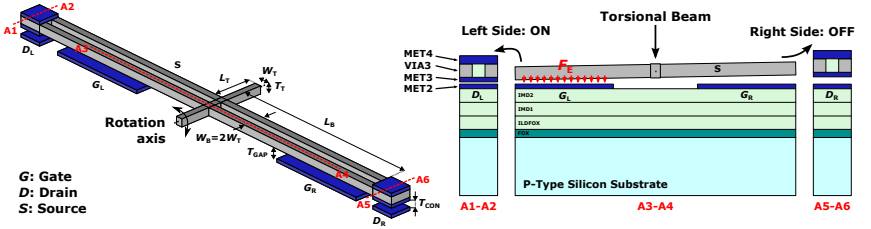


Figure 4.1: Three-dimensional schematic of the designed torsional relay including cross-sectional views and the definition of design parameters.

The key of the presented design is that the backbone of the MEM structure is based on the VIA3 layer [**?**], which is made of tungsten, a very hard material that provides excellent mechanical strength [114] to support the torsional relay. Moreover, it has a high melting point that makes it suitable to stand high current and temperature [114]. In contrast, tungsten is highly susceptible to oxidation and exhibits poor formability [**?**,114]. For this reason, the source-to-drain conductive path is formed with TiN using the sandwiched layers MET3 and MET2, since it presents low electrical resistivity, better formability and an excellent chemical inertness [**?**]. In this sense, the proposed novel design fully exploits the available resources of the selected CMOS technology for fabricating micrometer scale CMOS-MEMS resistive switches.

Table 4.1: Torsional relay design parameters and their values

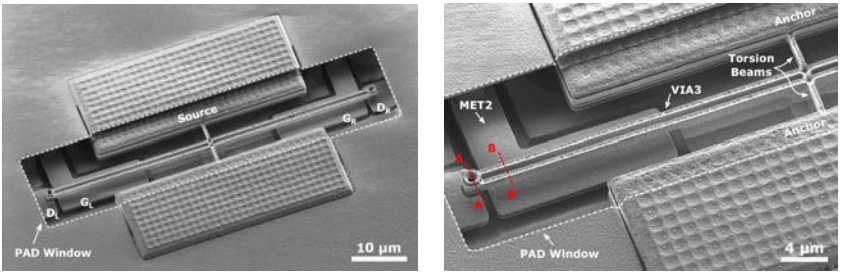
Design Parameters		Value (μm)
torsion beam length	L_T	3.5
torsion beam width	W_T	0.5
torsion beam thickness	T_T	1
main beam length	L_B	30
main beam width	W_B	2 x 0.5
contact gap	T_{CON}	1
actuation gap	T_{GAP}	1.25

Table 4.2: Material properties

Material Properties			W	Al	TiN
Young's modulus	E	[GPa]	410	70	600
mass density	ρ	[kg/m^3]	19'300	2'700	5'430

Figure 4.2(a) shows a 30-degree tilted SEM image of a fabricated and

released torsional relay. A detailed zoom in the left side of the relay is shown in figure 4.2(b), which indicates the cross-section views A-A' and B-B'. The PAD window defined over the relay area prevents the passivation deposition and allows to release the resonator from the silicon oxide SiO_2 around it just by using a simple one-step maskless wet etching based on a buffered HF solution. Figure 4.3 shows the cross-section views A-A' (see figures 4.3(a) and 4.3(b)) and B-B' (see figures 4.3(c) and 4.3(d)) taken before and after performing the releasing process. The measured contact gap T_{CON} is 1 μm and the actuation gap T_{GAP} is 1.25 μm.



(a) (b)

Figure 4.2: SEM image of a (a) 30-degree tilted view of a fabricated and released torsional relay and (b) zoom in the left beam showing the cross-sections views A-A' and B-B'.

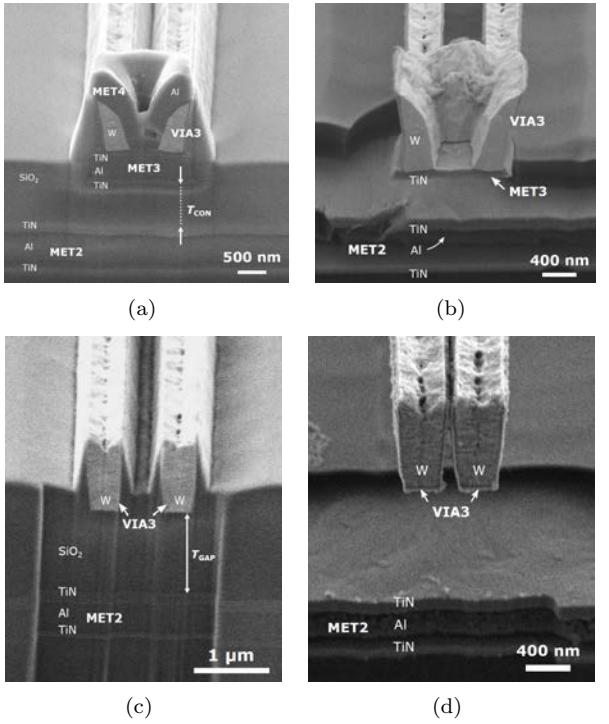
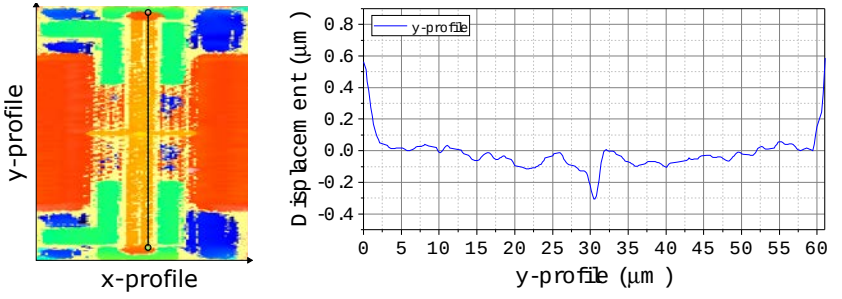


Figure 4.3: Cross-section views A-A' (a) non-released and (b) released; B-B' (c) non-released and (d) released. The cross-section is performed as indicates the red dotted line A-A' and B-B' in figure 4.2(b) by using focused ion beam (FIB) in milling mode.

In order to quantify the total beam curling, measurements using a Leica DCM 3D confocal microscopy were performed. Results show that the maximum curl-up for the y-profile is approximately 100 nm (see Fig. 4.4), which confirms that the mechanical structure is slightly affected by residual stress.



(a) (b)

Figure 4.4: Measured y-profile of the curl up in the relay. (a) Top view of the relay indicating the y-profile. (b) 2-D profile of the y-axis of the relay.

4.2 Experimental Results and Discussion

The fabricated switch was tested under two different conditions: at room temperature $\sim$ 25 °C 1) in air at atmospheric pressure, and 2) in vacuum at 10^{-5} mbar. In ambient conditions, the chips were exposed to air and tested in a Cascade Microtech probe station (PM8). In vacuum conditions, the chip was mounted and bounded onto a PCB and placed inside a home-made vacuum chamber. The I-V characterization was performed with an Agilent semiconductor analyzer B1500A equipped with four high resolution HRES-SMU units. The resonance frequency was measured with a network analyzer Agilent B5100A. Finally, the lifetime characterization was carried out with a standard oscilloscope and a DC voltage source.

4.2.1 Current-Voltage (I-V) Characteristic Curves

Figure 4.5(a) shows the typical pull-in and pull-out curve I_{DS}-V_G in linear scale of the presented torsional CMOS-MEMS relay. For more detail, the same data is represented in logarithmic scale in figures 4.5(b) and 4.5(c). I-V characterization was carried out in vacuum conditions.

As the right gate voltage V_{G_R} is increased from 0 to 80 V, the right side of the torsion beam turns on abruptly at 71.3 V while the left side remains off. Thus, a conductive path is formed between the contact electrode (or drain) and the movable structure (or source) by fixing the drain-to-source voltage V_{DS} to 3 V. This current is kept to a value of 30 nA using an external resistance of 100 MΩ to minimize the possibility of microwelding-

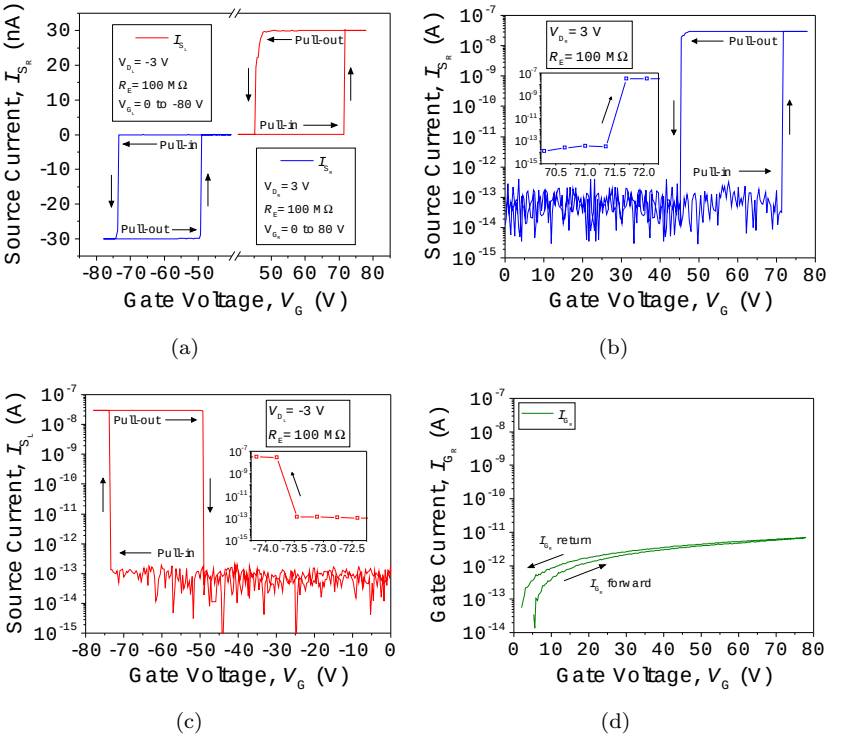
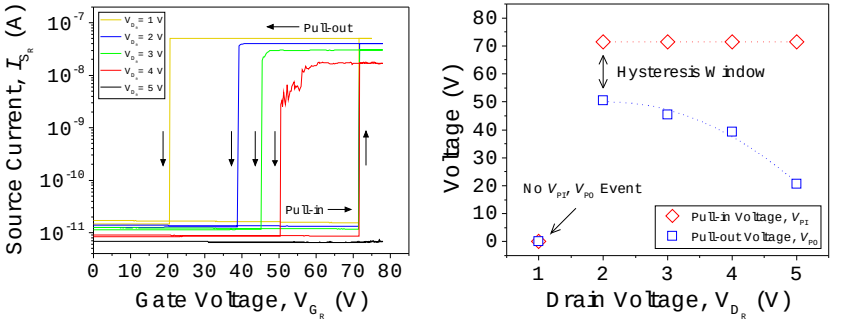


Figure 4.5: (a) Measured I_{DS}-V_G characteristic of the torsional relay. In red is represented the measurement of the left beam and, in blue the measurement of the right beam in linear scale. For more detail, the measurement of the (b) right beam and (c) the left beam is represented in logarithmic scale. The inset shows a zoom at the V_{PI} range. (d) Measured gate current I_{G_R} throughout the measurement.

induced failure. As V_{G_R} is decreased back to 0 V, the right torsion beam recovers its off-state position at 45.2 V, describing in this way a hysteretic behaviour. Such a phenomenon is due to the pull-in mode operation [41] and the adhesion forces that are acting on the contact electrode [**?**]. Complementary, the left side of the relay is also actuated by sweeping up and down the left gate voltage V_{G_L} from 0 to -80 V, because of the ambipolar nature of the electrostatic attraction, and fixing the left drain voltage V_{D_L} to -3 V (also protected using 100 MΩ). In this case, the left side turns on abruptly at 73.4 V and turns off at 48.9 V. For both sweeps, the measured on-off current ratio is 10^6 and, the subthreshold slope (based on the

voltage step of 348 mV) is 58 mV/dec as can be seen in the inset shown in figures 4.5(b) and 4.5(c). It should be noticed that a low gate current I_{G_R} is measured throughout the measurement as shown in figure 4.5(d) demonstrating a 5-terminal device operation [**?**].

Figure 4.6(a) shows measured I_{DS}-V_G characteristic curves for different drain bias voltages. It was experimentally observed that with increasing V_{DS}, the pull-in voltage remains almost constant and the pull-out voltage is decreased. Since the beam exercises higher force on the contact and more asperities come into contact, a larger contact area is formed [79], which results into larger hysteresis window due to stronger adhesion forces as shown in figure 4.6(b). So, higher V_{DS} leads to wider hysteresis window and ultimately may result in permanent stiction. As aforementioned, this fact does not represent a problem since the presented relay can be actuated bidirectionally, thereby overcoming such possible stiction issues in the contacting region.



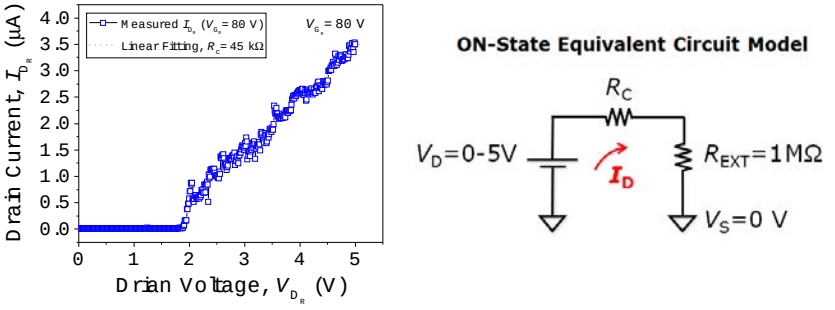
(a) (b)

Figure 4.6: (a) Measured I_{DS}-V_G characteristic curves for different V_{DS} voltages. (b) Measured hysteresis window versus V_{DS}. Notice that for V_{DS}=1 V, neither V_{PI} nor V_{PO} event is measured.

4.2.2 On-State Contact Resistance

The on-state contact resistance R_C was also studied by measuring the I_{DS}-V_{DS} characteristic as shown in figure 4.7(a). For this purpose, the relay was firstly brought into contact with a V_{G_R} voltage above the pull-in (i. e. for V_G=80 V). Then, by sweeping up the V_{DS_R} from 0 to 5 V, and placing an external resistance R_{EXT} of 1 MΩ (also to protect the device form microwelding-induced failure), the I_{D_R} current was measured, which showed an ohmic dependence from 2 V to upwards. From the equivalent

electrical model shown in (figure 4.7(b)), the on-state resistance R_C was extracted and found to be 45 kΩ.



(a) (b)

Figure 4.7: (a) Measured I_{DS}-V_{DS} characteristic of the torsional relay for V_G=80 V. The extrapolated R_C is 45 kΩ. (b) On-state equivalent circuit model used to fit the R_C.

In Table 4.3, a summary of reported TiN-contact based M/NEM relays in the state of the art is presented. It can be observed that using a fabrication process based on a commercial CMOS technology, a similar on-state resistance is obtained compared to a TiN-coated poly-Si relay fabricated using a full-custom process [113], since relay dimensions and apparent contact area are more resemblance to the presented relay. Instead, smaller NEM relays [**?**]- [**?**], present much larger contact resistances which is attributed to their smaller size and limited contact area.

4.2.3 Resonance Frequency and Switching Time

Figure 4.8(a) and 4.8(b) show the measured resonance frequency in ambient and vacuum conditions of the presented relay, respectively. Characterizing the frequency response is useful for determining the switching time of the relay [45]. To do so, the torsional mode is excited electrostatically by applying a RF signal P plus a DC-bias voltage V_{DC} through a bias tee in one of the gate electrodes. In ambient conditions, P=-5 dBm, and V_{DC}=27, 29 and 31 V. In vacuum conditions, P=-35 dBm, and V_{DC}=40, 41 and 42 V. Then, the movement of the switch is capacitively sensed through the source electrode. Notice that the quality factor Q is 90 in ambient conditions and 2500 in vacuum conditions, improved in the last case due to the reduction of the air damping [**?**].

The natural frequency of the movable structure can be found by a linear

Table 4.3: Comparison among TiN-contact based M/NEM relays in the state of the art. (l is length, g is actuation gap, V_D is drain voltage and I_D is drain current)

Ref.	Material and Dimensions	Contact Resistance, R_C
[113]	TiN-Coated Poly-Si l=24 μm, g=0.5 μm	4 kΩ–15 kΩ with V_D=2 V
[?]	MOCVD TiN/PVD TiN l=700-900 nm, g=40 nm	500 MΩ [a] with V_D=5 V, I_D=10 nA
[112]	TiN-Coated Poly-SiGe l=900 nm, g_G=100 nm	1 MΩ with V_D=2 V
[?]	TiN/W l=300 nm, g=35 nm	1.35 GΩ [1] with V_D=13.5 V, I_D=10 nA
[?]	TiN (MIM Module) l=1.5-2.5 μm, g=27 nm	1 GΩ with V_D=11.6-19 V
This work	TiN (MET3-MET2) l=30 μm, g=1.25 μm	20 kΩ–45 kΩ with V_D=3 V

[a]The on-state contact resistance R_C is not explicitly mentioned in the article. For comparison purpose, it is calculated as V_D/I_D.

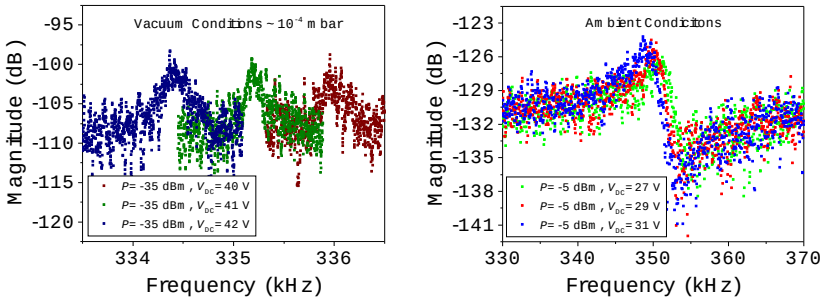
fitting of the experimental data as shown figure **??**, since the resonance frequency depends on the DC-bias voltage to the square [**?**]. The extrapolated natural frequency at V_{DC}=0 V, taking into account the measured resonant frequency in both two different test conditions, is 364.37 kHz. This result shows a very good agreement with the simulated resonance frequency of the torsional mode (f_0=347.0326 kHz) computed with the CoventorWare MEMech solver [**?**]. The inset shown in figure 4.8(a) presents the 3-D model of the simulated torsional mode.

The switching time t_S is defined as the time that takes the movable structure to travel from its equilibrium position to the contact or read electrode. For inertial limited systems (assuming small damping, i.e. Q>2), the t_S can be calculated as [42]

$$ts = \sqrt{\frac{27}{2}} \frac{V_{PI}}{V_{ACT}} \frac{1}{\omega_0} \tag{4.1}$$

where V_{PI} is the pull-in voltage, V_{ACT} is the actuation voltage and ω_0 is the natural frequency in radians.

As the extracted Q-factor in air is 90 and in vacuum 2500 (see figure 4.8(a) and 4.8(b)), we can assume a small damping scenario (Q>2) and calculate the switching time of the presented relay in accordance with equation (4.1). Considering the following values: V_{PI}=71.3 V, V_{ACT} =



(a) (b)

Figure 4.8: Experimental measurement of the torsional mode of the presented relay under different DC bias voltages (a) in ambient conditions and (b) in vacuum conditions. The measured data is smoothed using a moving average over two data points.

$1.1 \cdot V_{PI}$ and f_0=351 kHz, the switching time of the presented torsional CMOS-MEMS relay would be roughly 1.5 μs.

4.2.4 Cycling Test

Finally, a real-time measurement was performed using the electrical setup shown in figure ?? in order to monitor the on-state contact resistance of the relay and evaluate the the lifetime of the relay. Such an experiment was carried out in ambient conditions.

A square-wave voltage waveform V_G is applied to the gate, which causes the relay to turn on and off periodically. The V_G amplitude is 78 V, which is 1.1 times the pull-in voltage of the presented relay (V_{PI}=71.3 V) and the frequency is 0.5 Hz. The drain is connected to the power supply V_D through a resistor R_E, whereas the source is grounded. When the relay is off, the drain voltage is at V_D. When the relay is on, the output voltage V_O, which is monitored in the CH2 of the oscilloscope. Thus, the evolution of R_C with the number of on/off cycles is determined by the voltage divider formula with each switching cycle as follows,

$$R_C = \frac{V_O \cdot R_E}{V_O + V_D} \tag{4.2}$$

Figure 4.10(a) shows the evolution of R_C with the number of switching

cycles. Figure 4.10(b) shows the real-time measurement of several cycles at the beginning and at the end of the test.

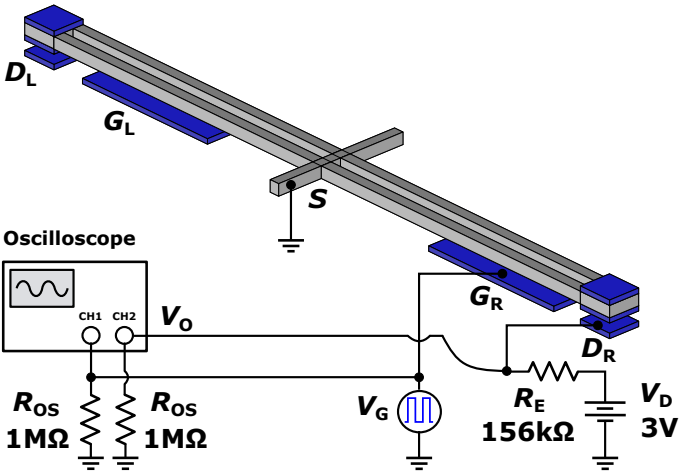
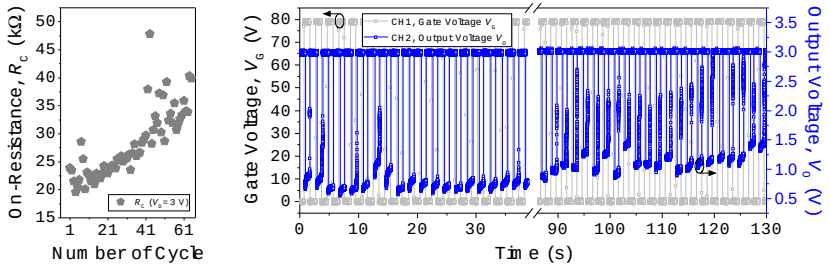


Figure 4.9: Schematic showing the setup for monitoring MEM-relay on-state resistance.



(a) (b)

Figure 4.10: (a) Evolution of R_C with the number of on/off switching cycles. (b) Real-time measurement of multiple cycles at the beginning (left) and at the end (right) of the test.

4.3 Conclusions

The feasibility of fabricating contact-mode MEM relays using the CMOS-MEMS approach (or intra-CMOS) which exploits the full foundry inherent characteristics enabling drastic reduction of the fabrication costs and batch

production is demonstrated in this work. To proof the concept, a torsional relay design has been proposed. In particular, such a relay has been fabricated using the BEOL of a commercial standard CMOS technology (AMS 0.35 μm) and released by means of a simple one step mask-less wet etching. I-V characterization has shown that the relay has the capability of performing the functionality of two relays, which can be bidirectionally actuated for more reliable operation, showing a steep and symmetric switching operation. As stated, this fact is a clear advantage to implement more compact-relay based digital logic circuits. An on-state contact resistance of 20 kΩ has been measured. Such an obtained value is comparable among the reported TiN-contact based M/NEM relays in the state-of-the-art. From the measured frequency response, the natural resonance of the mechanical structure has been extrapolated, which shows very good agreement with the 3-D FEM simulations. Eventually, the relay has shown to operate up to 65 cycles in the kΩ-range. Further improvements have to be addressed to solve reliability issues of the switch.

4.4 See-saw Relay: Design and Fabrication

Fig. 4.11 shows the see-saw relay design that consists in a sandwiched MET4-VIA3-MET3 main plate anchored by two W-VIA3 torsional beams (called source, S) which allow the ends of the main beam move up and down by electrostatically actuating the relay with the underneath located gate electrodes (G_R and G_L) of MET1-VIA1. Such mentioned endings are made of: (i) MET4-VIA3-MET3, (ii) MET4-VIA3 which make contact with the drain electrodes (D_R and D_L) of MET2; and (iii) MET4-VIA3 and makes contact with the drain electrodes (D_R and D_L) of MET2-VIA2. The design parameter values and the material properties of the relay are listed in Tab. 1 and 2, respectively.

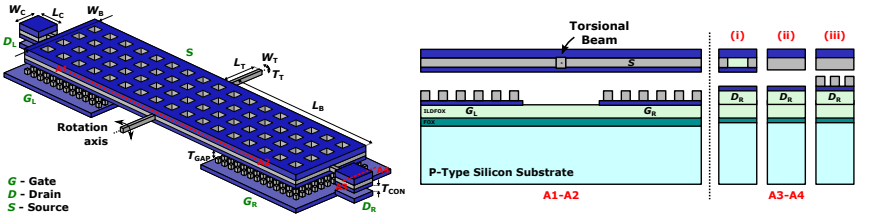


Figure 4.11: Three-dimensional schematic of the designed see-saw relay including cross-sectional views and the definition of design parameters. Three different contact type are designed: (i) MET4-VIA3-MET3, (ii) MET4-VIA3 and (iii) MET4-VIA3.

Table 4.4: See-saw relay design parameters and their values

Design Parameters		Value [μm]
torsion beam length	L_T	4.7
torsion beam width	W_T	0.5
torsion beam thickness	T_T	1.3
body length	L_B	59.6
body width	W_B	16
contact length	L_C	2.5
contact width	W_C	2.5
actuation gap	T_{GAP}	1.95
contact gap (i)	T_{CON_i}	1
contact gap (ii)	$T_{CON_{ii}}$	1.3[a]
contact gap (iii)	$T_{CON_{iii}}$	0.45[1]

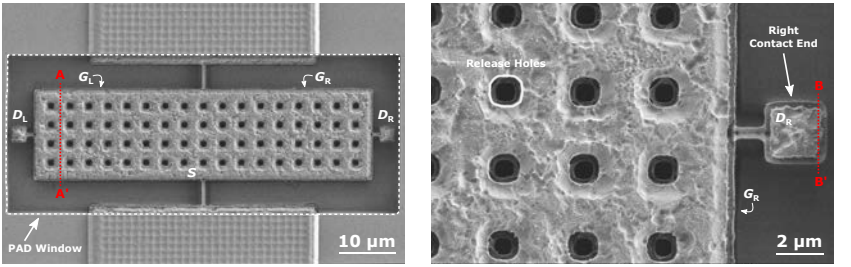
[a]The gap is measured after fabrication, since design rules are being violated.

Table 4.5: Material properties

Material Properties			W	Al	TiN
Young's modulus	E	[GPa]	410	70	600
mass density	ρ	[kg/m^3]	19'300	2'700	5'430

The key of such a see-saw design compared to the previous approach, besides the previously stated benefits of the use of VIA3 platform, is that the coupling area along the structure plate is maximized with the main plate which allow us to further reduce the actuation voltage; thus, it give us an extra degree-of-freedom to deal with larger actuation gaps or lets say contact and actuation gaps with different height.

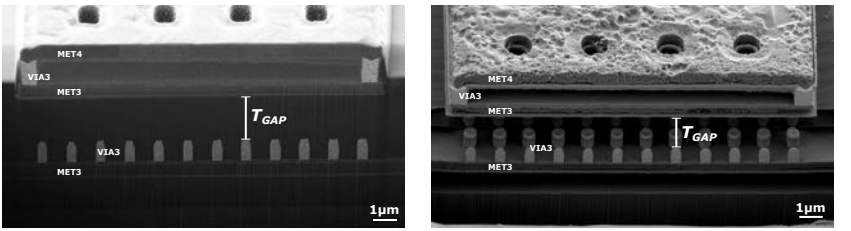
Fig. 4.12(a) shows a top view SEM image of a fabricated see-saw relay. A detailed zoom of the right contact end (right drain) of the relay is shown in Fig. 4.12(b). The PAD window defined over the relay area prevents the passivation deposition and allows the releasing of the relay from the silicon oxide SiO_2 around it just by using a simple one-step maskless wet etching based on a buffered HF solution. In this case, release holes are required to facilitate the wet etching of the sacrificial SiO_2 layer underneath the main plate.



(a) (b)

Figure 4.12: SEM image of a (a) top view of a fabricated see-saw relay indicating the cut-line A-A' and (b) zoom in the right contact end indicating the cut-line B-B'.

Fig. 4.13(a) and 4.13(b) show the focused-ion-beam (FIB)-cut cross-section view A-A' (in Fig. 4.12(a)) before and after being released, respectively. The measured actuation gap T_{GAP} is 1.95 μm. Notice that discrete VIA1's over the MET1 lead to a reduced T_{GAP}, although not all the area can be leveraged.



(a) (b)

Figure 4.13: (a) Non-released and (b) released FIB-cut cross-section views A-A' taken along the red dotted line shown in Fig. 4.12(a).

Fig. 4.14 show the focused-ion-beam (FIB)-cut cross-section view B-B'

(in Fig. 4.12(b)) of the three different types of fabricated contacts before and after being released. The measured contact gap T_{CON} for each type of contact is: $T_{CON_i} = 1$ μm, $T_{CON_{ii}} = 1.3$ μm and, $T_{CON_{iii}} = 450$ nm. Notice that different materials are involved at the contact interfaces of the different fabricated types of contact: (i) TiN vs TiN, (ii) W vs TiN and (iii) W vs W.

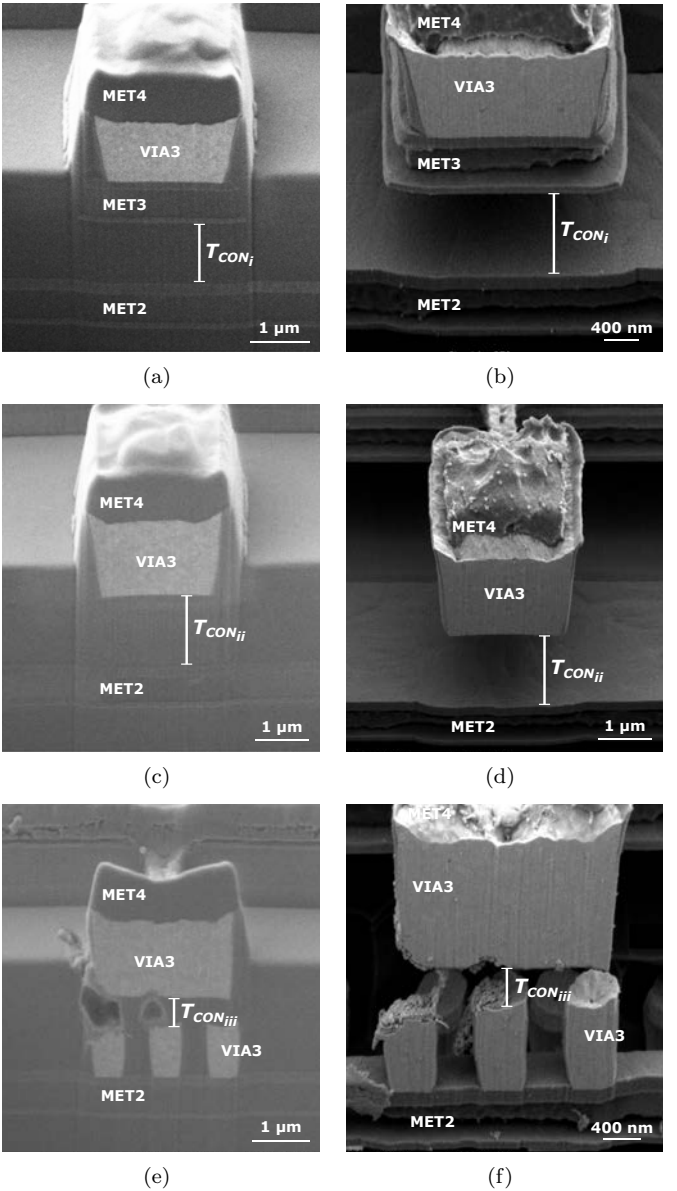


Figure 4.14: FIB-cut cross-section views B-B' taken along the red dotted line shown in Fig. 4.12(b) of the (a), (b) contact type (i); (c), (d) contact type (ii); and (e), (f) contact type (iii) being non-released and released respectively.

4.5 Experimental Results and Discussion

The fabricated see-saw was tested under two different conditions: at room temperature $\sim$ 25 °C 1) in air at atmospheric pressure, and 2) in vacuum at 10^{-5} mbar. In ambient conditions, the chips were exposed to air and tested in a Cascade Microtech probe station (PM8). In vacuum conditions, the chip was mounted and bounded onto a PCB and placed inside a home-made vacuum chamber. The I-V characterization was performed with an Agilent semiconductor analyzer B1500A equipped with four high resolution HRES-SMU units. The resonance frequency was measured with the Agilent B5100A network analyzer.

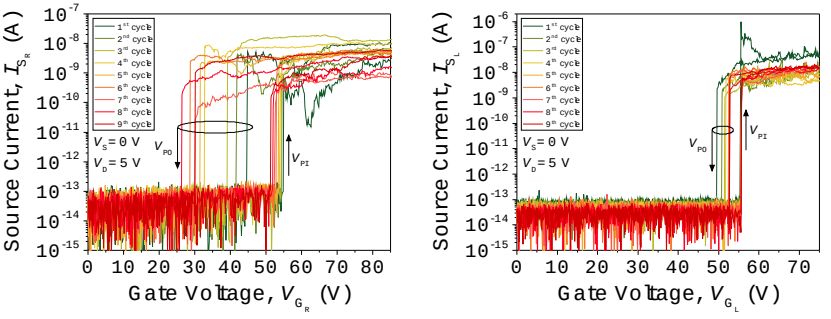
4.5.1 Current-Voltage (I-V) Characteristic Curves

Current-voltage I-V curves were first taken in both ambient and vacuum conditions in order to extract the switching characteristics (V_{PI}, V_{PO} and R_c) of the three types of fabricated contacts.

4.5.1.1 See-saw Relay with contact type (i)

Fig. 4.15(a) and 4.15(b) show the first nine I-V curves taken in both left and right ends of a see-saw relay being exposed to air conditions. As the V_{G_R} is increased from 0 to 85 V, the right side of the torsion beam turns on abruptly at 54.82 V while the left side remains off. Thus, a conductive path is formed between the right contact electrode (or right drain) and the movable structure (or source) by fixing the drain-to-source voltage V_{DS} to 5 V. Complementary, the left side of the relay is also actuated by sweeping up and down the left gate voltage V_{G_L} from 0 to 85 V, and fixing the left drain voltage V_{D_L} also to 5 V (protected with 1 MΩ). In this case, the left side turns on abruptly at 55.5 V. For both sweeps, the measured on-off current ratio is $\sim 10^5$ and, the R_c is $\sim 10^8$ Ω. Instead, an asymmetric behavior is observed comparing the V_{PO} of both tested sides. Since the V_{PO} and thus the hysteresis window is strongly related with the adhesion forces at the contact interface, this would mean that different contact scenarios are involved in both contact ends. SEM images were taken to confirm the hypothesis as shown in Fig. 4.16. As can be observed, the bottom thin TiN layer that forms the sandwiched MET3 layer of TiN-Al-TiN fall over the MET2 layer due to the large time required for the release of the structure (12' + 5' min), causing such an observed

asymmetry in the hysteresis window.



(a) (b)

Figure 4.15: First nine I-V switching characteristics in ambient conditions of the bottom (a) and (b) top electrodes of a contact-type-(i) see-saw relay.

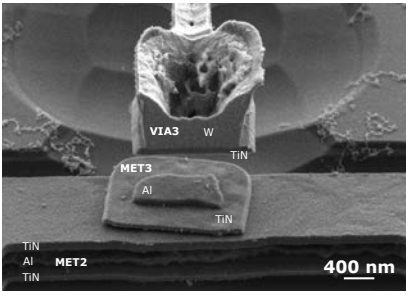


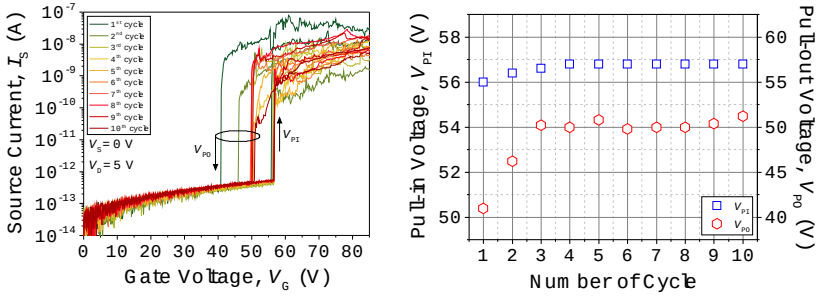
Figure 4.16: SEM image taken in the contact region of the see-saw relay with contact type (i) showing the over-etch of the aluminium layer contained in the sandwiched MET3 layer of TiN-Al-TiN.

4.5.1.2 See-saw Relay with contact type (ii)

Fig. 4.17 shows the first ten I-V curves taken in a contact-type-(ii) see-saw relay being exposed to air conditions, exhibiting a similar Rc of $\sim 10^8$ and a I_{ON}/I_{OFF} ratio of 10^4. Fig. 4.17(b) shows how V_{PI} and V_{PO} evolve over these ten cycles. V_{PI} is fairly stable, but V_{PO} increases gradually with exposure to air. This phenomenon can be explained by the reduced surface adhesive force from metallic surfaces to oxide surfaces. Therefore, the hysteresis window reduces over time due to oxide formation.

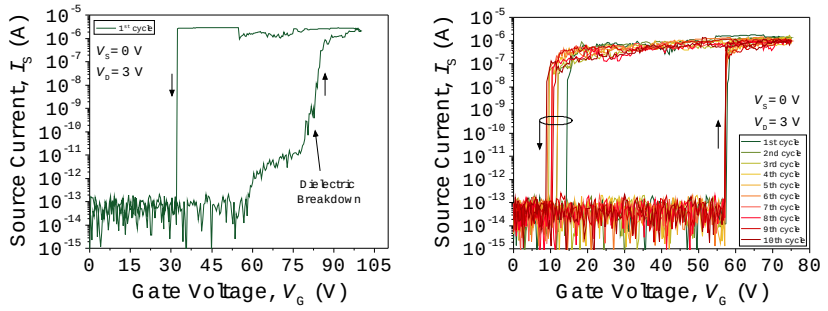
Fig. 4.18 shows the I-V characterization conducted in vacuum condi-

tions at 10^{-4} mbar. The first I-V curve shows no abrupt transition due to the break down of the native oxide at the TiN/W contact interface (see Fig. 4.18(a)). Next, ten I-V curves are taken as shown in Fig. 4.18(b), which already show the typical hysteretic behavior with initial sharp V_{PI} and V_{PO} voltages of 57.4 V and 14.6 V, respectively. The R_c is ~ 1 MΩ, 500 times better than compared to air conditions, which leads to an increased I_{ON}/I_{OFF} ratio of 10^7. Recall that a wider hysteresis window means that adhesion forces are exacerbated in the contacting region due to an increased effective contact area from the larger levels of current obtained.



(a) (b)

Figure 4.17: (a) First ten I-V switching characteristics in ambient conditions of the bottom of a contact-type-(ii) see-saw relay and (b) evolution of V_{PI} and V_{PO} over these ten cycles.

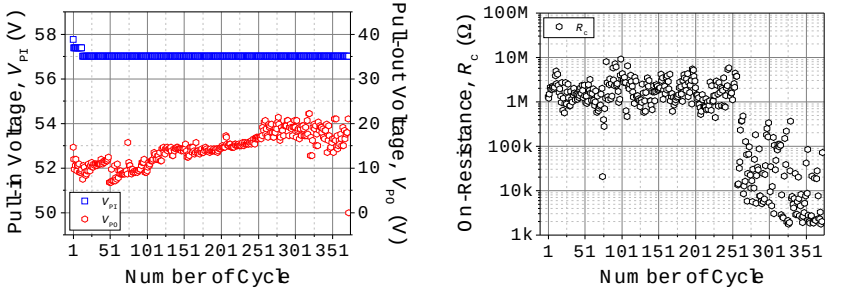


(a) (b)

Figure 4.18: (a) First taken I-V curve showing no abrupt transition due to the break down of the native oxide. (b) Next 10 I-V switching characteristics. Measurements conducted under vacuum conditions.

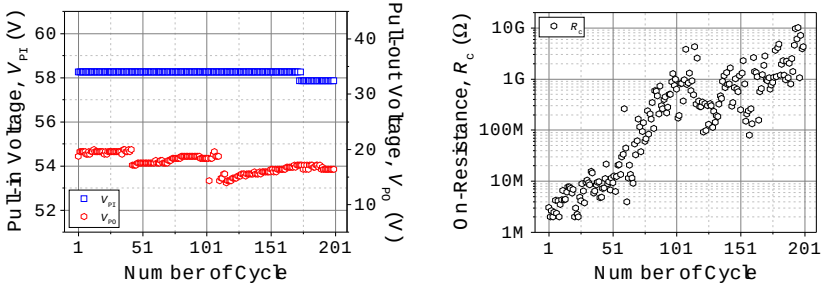
Fig. 4.19(a) and 4.19(b) show how evolve V_{PI}, V_{PO} and R_c over a total of 351 switching cycles. A nominal V_{PI} of 57 V is found to be very stable over these cycles with an absolute error of only 0.75 V. V_{PO} shows to increase over these cycles. This phenomenon can be explained by the reduced surface adhesive force from metallic surfaces to oxide surfaces as previously happened with the contact-type-(i) see-saw relay. However, the R_c drops from the cycle 251 to upwards which could not explain it. As the *Rc* drop, the adhesion force increases ultimately leading to permanent stiction.

The V_{PI}, V_{PO} and R_c are recorded over 200 cycles using a new fresh relay, but this time keeping the compliance limit to 1 μA as shown Fig. 4.20(a) and 4.20(b), respectively. The V_{PI} shows a nominal value of 58.245 V with an absolute error of only 0.4 V over these cycles, demonstrating again the great stability of the VIA3 platform. Regarding the R_c, it shows to increase with the switching cycles. So, limiting the pass of the current favors the insulating native-oxide formation at the contacting interface.



(a) (b)

Figure 4.19: Evolution of the (a) V_{PI}, V_{PO} and R_c over 355 switching cycles in vacuum conditions. V_{DS} is fixed to 3 V.



(a) (b)

Figure 4.20: Evolution of the (a) V_{PI}, V_{PO} and R_c over 355 switching cycles in vacuum conditions. Compliance limit is fixed to 1 μA and V_{DS} to 3 V.

Fig. 4.21 highlights that by applying higher V_{DS} voltages ($V_{DS} > 3$ V), contact performance can be restored after breaking down the formed oxide. This indicates that the contact reliability is not intrinsically degraded but strongly affected by the environment in which the device operates.

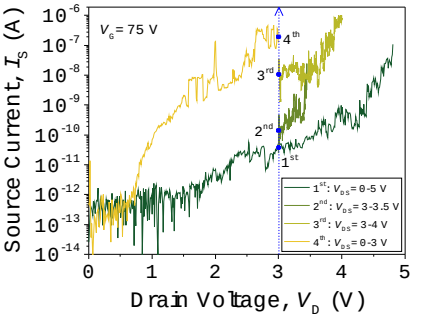
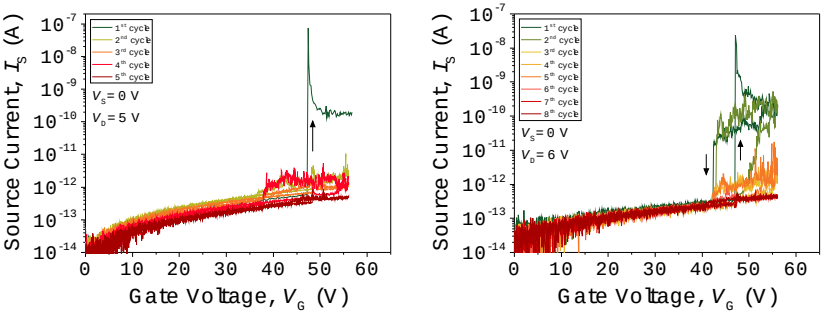


Figure 4.21: Succesive V_{DS} sweeps showing the restoring of the contact performance after breaking down the formed insulating native oxide. VGS is fixed to 75 V to keep the switch in the on-state.

4.5.1.3 See-saw Relay with contact type (iii)

Fig. 4.22(a) and 4.22(b) show the I-V characterization of both left and right ends of a contact-type-(iii) see-saw relay being exposed to air conditions. It can be observed an initial V_{PI} of X and X V in the left and right ends respectively, although the current degrades to the noise level in only 5 cycles. So, contact-type-(iii) see-saw relay involving a W-to-W contact interface exhibits the most exacerbated degradation when cycling is done

in air.



(a) (b)

Figure 4.22: (a) First five I-V switching characteristics in air of the left contact end. V_{DS} is fixed to 5 V. (b) Firsts eight I-V curves in air of the right contact end. V_{DS} is fixed to 6 V.

In contrast, the contact performance of the contact-type-(iii) see-saw relay is found to behave completely different when it is operated in vacuum conditions. First, the initial native oxide break is done by switching the device on (with $V_{GS} = 75$ V) and then, by sweeping up the V_{DS} the drain current is monitored and when a drain current spike is detected the V_{DS} bias is automatically stopped, indicating native oxide breakdown (see Fig. 4.23). Fig. 4.24(a) shows the I-V characteristics of the same relay after the oxide breakdown for four different V_{DS} bias voltages (V_{DS}=0.1, 0.2, 0.75 and 1 V). The on-state contact resistance is found to be 51.4 kΩ as shown Fig. 4.24(b).

An attempt is then made to monitor the evolution of contact properties after each cycle by taking continuous I-V curves with $V_{DS} = 1$ V (see Fig. 4.25(a)). Notice that the compliance limit is fixed to 4 μA. By doing so, it is found that the V_{PI} is stable as precedent characterization revealed but it is found the relay to stuck after 16 cycles (see Fig. 4.25(b)) even with a low bias V_{DS} of 1 V.

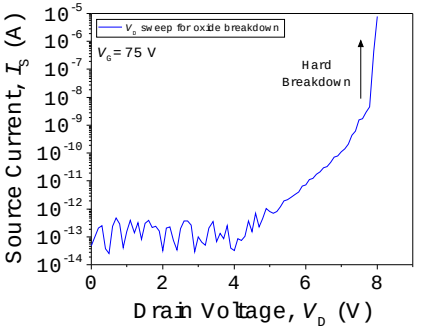
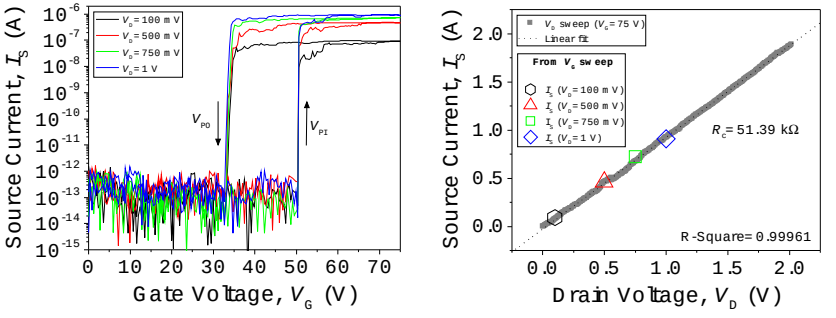
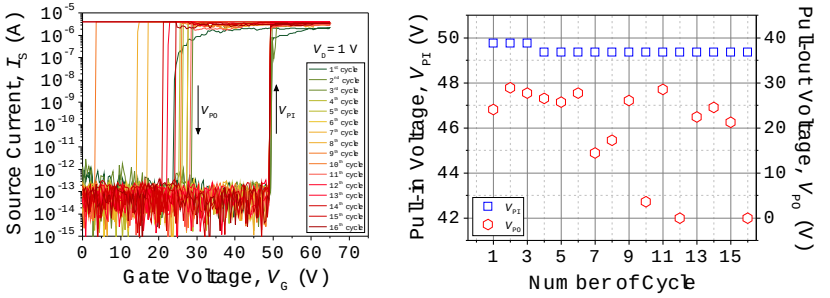


Figure 4.23: First nine I-V switching characteristics in ambient conditions of the bottom (a) and (b) top electrodes.



(a) (b)

Figure 4.24: First nine I-V switching characteristics in ambient conditions of the bottom (a) and (b) top electrodes.

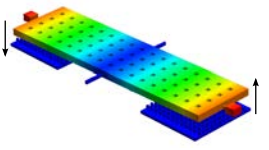
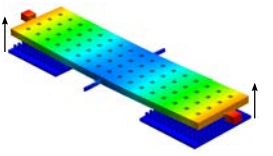


(a) (b)

Figure 4.25: First nine I-V switching characteristics in ambient conditions of the bottom (a) and (b) top electrodes.

4.5.2 Frequency Response and Switching Time

Table 4.6: Resonant frequency and mode shape of the see-saw relay.

	Torsional Mode	**Vertical Mode**
Mode Shape		
Resonant Frequency, f_0	152 kHz	1.5 MHz
Spring Constant, k	1.28 N/m	69.6 N/m

4.6 MEMS Resonators based on the VIA3 Platform

Parallel to the main thread of this thesis, MEMS resonators based on the VIA3 platform were also developed as a result of the work done. Next, we present the design and characterization of a dual-frequency oscillator that consist of these reliable torsional tungsten resonators and a high gain, low power and ultra-compact transimpedance amplifier (TIA). The circuitry was developed by G. Sobreviela et al.. Further detail related with the circuitry design and performance can be found in [123, 124]. A brief

introduction and motivation of this work are first stated in order to put the reader in context.

4.6.1 Introduction

We are now clearly moving towards a new era of always-on, real-time access mobile experiences, plenty of sensors in the vehicles we drive, the clothes we wear, and the buildings we live in. Almost everything will have connectivity. The Internet of Things (IoT) has created new challenges for the design of reference oscillators. Multi- frequency references as well as low power consumption have increasingly been demanded [125]. To further optimize such parameters, as well as miniaturization, production cost and large-scale integration, significant efforts are being devoted to developing a CMOS-MEMS oscillator platform [17] or a less-cost efficient MEMS-on-CMOS approach [126]. The extra-challenge and main contribution of the presented work is the demonstration of a single-resonator dual-frequency BEOL-Embedded CMOS-MEMS oscillator which none of the previous works in the CMOS-MEMS field has dealt with. The proposed dual-frequency oscillator features a significantly better performance compared with previous works [126], enabled by a simple and ultra-compact TIA core which consumes less than 10 μW operated with reduced supply voltage (V_{DD}=1.65 V) and under moderate dc MEMS bias voltage (V_{DC}=18 V).

4.6.2 Resonator and Oscillator Circuit

Fig. 4.26 shows optical photos of the fabricated dual-frequency CMOS-MEMS oscillator. The oscillator circuitry along with the MEMS resonator are monolithically integrated and manufactured utilizing a low cost, conventional 0.35 μm CMOS service provided by the semiconductor company Austria Microsystems (AMS).

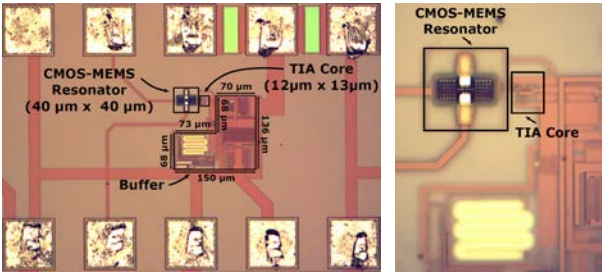


Figure 4.26: Optical images of the presented single-resonator dual-frequency BEOL-Embedded CMOS-MEMS oscillator fabricated in AMS 0.35 μm standard CMOS technology.

Fig. 4.28 shows a scanning electron microscope (SEM) perspective view of the resonator and its cross-sectional view with the post-CMOS releasing process flow. The passivation aperture defined over the resonator allows the in-house post-CMOS releasing process to be done directly. In this sense, the BHF solution can penetrate though the resonator area while the same passivation layer, named PROT1 in Fig 4.27(b), protects the chip and the transistor circuits.

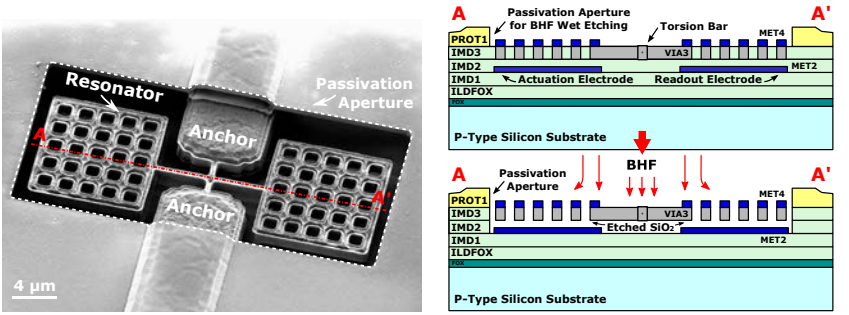
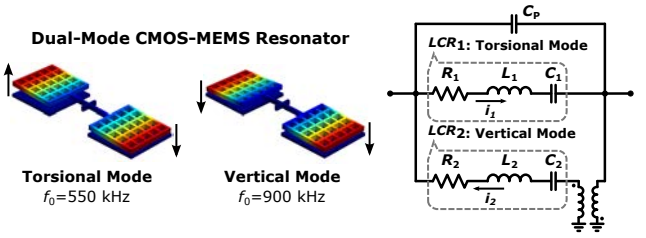


Figure 4.27: (a) SEM image of a fabricated resonator and (b) cross-sectional view describing the post-CMOS releasing process. The dimensions of the resonator are: l_T=1.5 μm, l_V=5 μm, w=0.5 μm and l_P=10.5 μm.

The fabricated resonator, which is built in the same VIA3 platform used for the relays, is electrostatically actuated applying an ac voltage to the driving electrode plus a dc bias voltage to the resonator. These voltages combine to produce a force that can excite two mechanical modes, the torsional (TM) and the vertical mode (VM) with natural frequencies f_0 of 553 and 906 kHz, respectively. The mode shapes (from finite ele-

ment method FEM simulations) and the equivalent electrical circuit of the resonator are illustrated in Fig. 4.28.

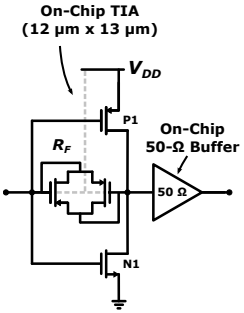


LCR PARAMETERS FOR V_{DC}=18 V

	TM	VM	
f_0	550.9	904.7	kHz
Q	2'000	1'750	-
R_m	0.93	2.1	MΩ
L_m	537	646.5	H
C_m	155.4	47.87	aF
C_p	240		aF

Figure 4.28: Mode shapes and equivalent electrical circuit of the proposed dual-mode MEMS resonator. Table shows the LCR parameters for V_DC=18 V

In order to overcome the high impedance that the CMOS-MEMS resonators usually present [17] while preserving low power consumption, and compactness in terms of layout area, this work adopts a very simple inverter TIA topology with a feedback pseudo resistor R_F implemented by a PMOS transistor operating in the subthreshold region as depicted in Fig. 4.29. Certainly, a differential amplifier presents better power supply rejection ratio (PSRR) and robustness due to elimination of common mode effects, but as pointed out by [127], a two-transistor inverter topology can provide better noise performance and lower power consumption. The simulated performance of the TIA amplifier (from extracted layout) is summarized in the table shown in Fig. 4.29. The overall area of the circuit (including the integrated 50-Ω buffer) is 15'660 μm^2.



SIMULATED TIA PERFORMANCE

Parameters @ 1MHz	V_{DD}=1.65 V
TIA Core Power	8.5 µW
TIA Gain	157 dBΩ
Output Voltage Noise	48.1 nV·Hz$^{-1/2}$
Input-Referred Current Noise	0.67 fA·Hz$^{-1/2}$
PSRR	53 dB

Figure 4.29: Schematic of the proposed TIA topology and the simulated performance of the TIA amplifier for V_{DD}=1.65 V.

An off-chip switching network with inverting and non-inverting stages provides the required 0° or 180° phase shift needed for oscillation in the

two different modes. The phase mismatch is externally corrected to close the loop. This dual-frequency feature combined with the low power and ultra-compact TIA core is the key novelty of the presented work, as we will present and discuss in next subsection.

4.6.3 Experimental Results and Discussion

Prior to the oscillator measurement, the open loop characterization is performed with an Agilent E5100A Network Analyzer. Fig. 4.30 shows open-loop curves measured under vacuum conditions (~10^{-4} mbar) and over a voltage range of V_{DC}=4-29 V. The f_0 of each resonant mode can be found by a linear fitting of the experimental data as shown in Fig. 4.31 due to the electro-spring softening effect [17]. The extrapolated f_0 at V_{DC}=0 V is 553.47 kHz and 906.19 kHz, for the TM and the VM respectively, which is in accordance with the CoventorWare FEM simulations. As V_{DC} varies from 4 to 29 V, a substantial tuning coefficient of -14.14 ppm·V^{-2} and -5.4 ppm·V^{-2} is achieved for the TM and the VM, respectively. The computed R_m as a function of the applied voltages (see Fig. 4.31) are -12.83 kΩ·V^{-2} and -28.12 kΩ·V^{-2} for the TM and VM, respectively. Note that the TM exhibits an almost two times smaller R_m while the Q-factor is in the same range. With V_{DC}=18 V, the Barkhausen conditions (gain $\geqslant$ 1) are fulfilled for oscillation for the two resonances. The extracted LCR parameters along with the softened resonant frequency and the Q of both resonances in such conditions are summarized in the table shown in Fig. 4.28.

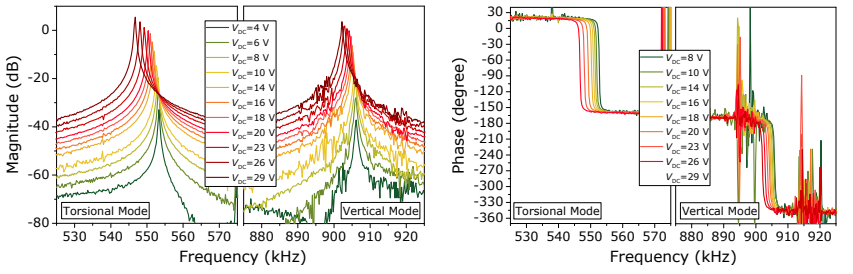


Figure 4.30: Measured (a) magnitude and (b) phase open-loop frequency response sweeping the resonator bias (V_{DC}=4-29 V) in vacuum conditions.

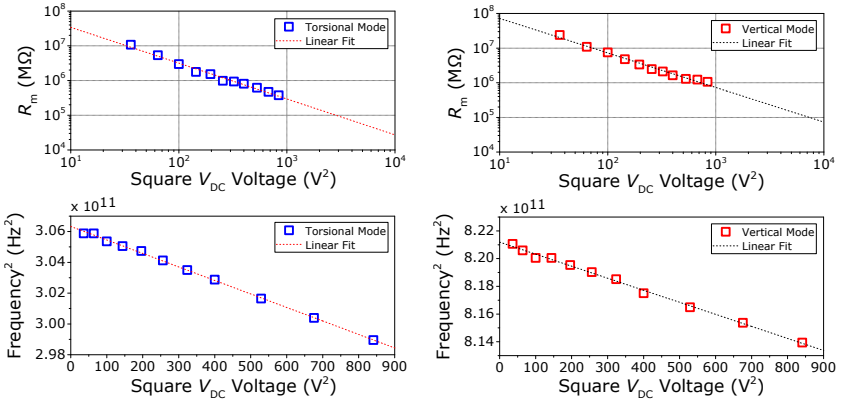
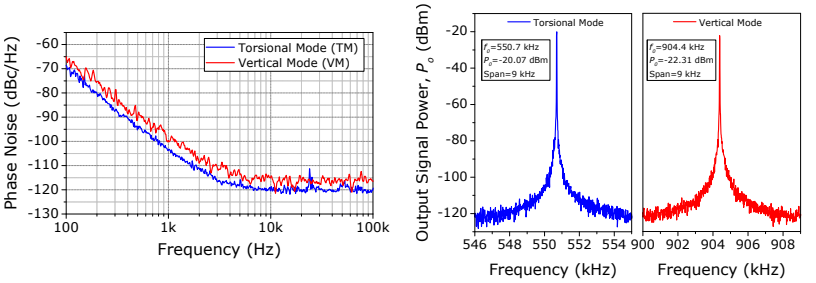


Figure 4.31: Extracted R_m and f_0 for (a) the TM and (b) the VM.

The oscillator performance is then evaluated by the Keysight PXA Signal Analyzer N9030A with the addition of the off-chip 0°/180° phase-shift stage to close both modes. Fig. 4.32(a) presents the measured phase noise (PN) curves of the oscillator, with V_{DC}=18 V and V_{DD}=1.65 V. The PN of the oscillator when operating the TM at 1 kHz offset is -103.8 dBc/Hz with floor noise reaching -121 dBc/Hz. By switching the 0°/180° stage, the oscillation frequency changes to the VM. In this mode, the PN at 1 kHz offset is -99.6 dBc/Hz with floor noise reaching -117 dBc/Hz. Fig. 4.32(b) shows the output power spectrum of the two possible oscillator output signals, under the same conditions of V_{DC}=18 V and V_{DD}=1.65 V. The power consumption of the TIA core is only 8.5 μW with a supply voltage V_{DD} of 1.65 V (excluding the on-chip buffer and off-chip circuitry).



(a) (b)

Figure 4.32: (a) Measured phase noise of the dual-frequency CMOS-MEMS oscillator under V_{DC}=18 V and V_{DD}=1.65 V. (b) Measured output spectrum of the dual-frequency CMOS-MEMS oscillator under V_{DC}=18 V and $_{DD}$=1.65 V.

The comparison of the proposed oscillator with the state of the art [100, 125–130] is tabulated in Fig. 4.33. A normalized figure of merit (FOM) is used to evaluate the performance at close to carrier, which is defined as [131]

$$FOM = 10\log\left(PN(1\text{ kHz})\right) - 20\log\left(\frac{f_s}{10\text{ MHz}}\right) + 10\log\left(\frac{P\,[\text{mW}]}{1\text{ mW}}\right) \tag{4.3}$$

where PN is the phase noise, f_s is the frequency and P is the power consumption

Thanks to the reliable VIA3 platform for designing MEMS resonators [49], the proposed oscillator shows unique dual-frequency operation enabled by the aforementioned torsional tungsten resonator, compared with previous reported BEOL-embedded CMOS-MEMS oscillators [100, 130]. Also, it shows a comparable and competitive normalized FOM of -99.24 dBc·Hz^{-1} ·mW^{-1} among the other oscillators. Furthermore, the presented work achieves a significantly better performance with more than 176X power saving under moderate dc MEMS bias voltage compared with the dual-frequency system based on a MEMS-on-CMOS approach [126]. Even compared with the sub-150μW oscillator developed by [130], this work still attains more than 7X power saving. Regarding the layout area and the compactness of the system, the TIA core only occupies a very small area of 12 μm x 13 μm, which is even smaller than the ultra-compact pixel

NEMS-CMOS oscillator [128], revealing the effectiveness of the presented TIA core for low power and ultra-compact area constrains.

Reference	Berkeley 2013 [7]	Georgia Tech 2015 [1]		CEA LETI 2014 [8]	Berkeley 2008 [9]	UAB 2015 [2]		NTHU 2016[10]	UAB 2013 [11]	This work	
Implementation	Two-Chip Solution			Pre-CMOS	MEMS-on-CMOS			BEOL-Embedded			
Dual-Frequency	NO	YES		NO	NO	YES		NO	NO	YES	
CMOS Process	0.35 µm	0.5 µm		ST 0.35 µm	TSMC 0.35 µm	SilTerra 0.18 µm		TSMC 0.35 µm	AMS 0.35 µm	AMS 0.35 µm	
Circuit Integration	Wirebond	Wirebond		Monolithic	Monolithic	Monolithic		Monolithic	Monolithic	Monolithic	
Resonator (Trans. Type)	Disk Resonator (Capacitive)	Width-Extensional (Piezoelectric)		CFB (Capacitive)	9-Disk Array (Capacitive)	CCB (Capacitive)		DETF (Capacitive)	DETF (Capacitive)	Seesaw (Capacitive)	
Resonator Material	Poly-Si	AlN		Silicon	Nickel	Bimetallic Nitride		Metal-Oxide Composite	Poly-Si	Tungsten-Al Composite	
Mode Type	Bulk	Bulk		Flexural	Flexural	Flexural	Torsional	Flexural	Flexural	Torsional	Flexural
f_0 **[Hz]**	61M	35M	175M	7.8M	10.92M	11.9M	24.5M	1.23M	11M	551k	905k
***Q*-factor**	130'000 (Vacuum)	1'800 (Vacuum)	3'200 (Vacuum)	NA (Vacuum)	1'092 (Vacuum)	1'500 (Vacuum)		1'900 (Vacuum)	147 (Air)	2'000 (Vacuum)	1'750 (Vacuum)
MEMS DC Bias (V)	7.45	Not required		24	5	15	20	20	1.5	18	
***R*m [Ω]**	14k	1.36k	0.26k	NA	5.8k	NA	NA	2M	8M	930k	2.1M
Supply Vol. [V]	1.7	2.5	4	3.3	3.3	1.8		1.3	3.3	1.65	
PN @ 1 kHz [dBc/Hz]	-119	-112	-103	NA	-80	-70	-55	-110	-50	-103.8	-99.6
PN Floor [dBc/Hz]	-139	-142	-140	NA	-96	-120		-113	-109	-121	-117
Power [µW]	78	3'800	13'500	NA	350	687.6		65	1'500	8.5	
FOM [dBc/Hz mW]	-145.79	-117.08	-116.56	NA	-85.3	-73.14	-64.41	-103.67	-49	-98.57	-99.24
System Area											
▪ **MEMS**	100 µm x 100 µm*	170 µm x 80 µm*		16 µm x 19 µm*	302 µm x 60 µm	95 µm x 180 µm		260 µm x 120 µm	50 µm x 50 µm	42 µm x 40 µm	
▪ **TIA Core**	60 µm x 45 µm#	NA		44 µm x 48 µm**	50 µm x 50 µm	50 µm x 40 µm		50 µm x 40 µm	54 µm x 66 µm	12 µm x 13 µm	

* Not explicitly mentioned in the article. Area estimated from SEM image. ** The buffer stage is also included. #Capacitor area of 200 µm x 100 µm not included.

Figure 4.33: Comparison of the proposed oscillator with the state of the art.

4.6.4 Conclusion

In conclusion, this work demonstrates a dual-frequency BEOL-Embedded CMOS-MEMS oscillator. A simple inverter TIA topology with high gain, low power, and ultra-compactness features along with a very reliable tungsten resonator operated with moderated dc MEMS bias are the keys to enable such performance with dual-frequency operation. The proposed oscillator contributes to the emerging IoT scenario in which low-power and ultra-compactness are indispensable features, being fully integrated with CMOS and compatible with other on-chip MEMS sensors.

Chapter 5

SilTerra RF MEMS-on-CMOS Tunable Capacitors

During the phD I had the opportunity to collaborate with the semiconductor manufacturing enterprise SilTerra Malaysia Sdn. Bhd. SilTerra was developing a commercial MEMS technology characterized to be deposited on top of its 180 nm CMOS technology. Initially, SilTerra started developing MEMS resonators based on a bimetallic alloy of aluminium titanium nitride (TiALN) and with vertical gaps of up to 25 nm. A low cost, low profile zero-level vacuum package (ZLP) covered the MEMS cell, which ensured vacuum sealing and avoid external contamination. Under such conditions, the developed SilTerra MEMS resonators achieved great performance with quality factors higher than 1000.

Resonators are characterized to operate at the resonance frequency. Nevertheless, we may think in operating the resonators outside the resonance frequency, where we only see the static capacitance created between the resonator and the actuation electrode and then, take advantage of the electrostatic force to actuate the movable MEMS element achieving thus a tunable capacitor. This chapter focuses on the evaluation of such resonators developed with the SilTerra MEMS-on-CMOS platform as a tunable capacitors.

As a brief summary, a rigorous study of the parameters of interest of the variable RF MEMS tunable capacitors is conducted in order to be extracted from the carried-out pertinent measurements. We will see that the extracted initial capacitance is too small to be useful in the frequency range of interest. For this reason, new devices with larger coupling areas were designed and combined in an array (capacitors in parallel) to achieve the usual capacitances values required in such a frequency band of interest.

5.1 Why RF MEMS Tunable Capacitors?

We are now clearly moving towards a new era of always-on, real-time access mobile experiences, driven largely by smartphones, tablets, and video streaming which are flooding the wireless networks of massive data usage [132]. In fact, overall mobile data traffic is expected to grow to 40 exabytes per month by 2021 (see Fig. 5.1). With the proliferation of multiband wireless systems, reconfigurable systems have increasingly been demanded. Most recent solutions for the implementation of such multiband solutions employ RF MEMS switches and tunable capacitors since they offer low loss, high quality factor, high tuning range, very low power consumption, and superior linearity compared to their solid-state counterpart [45].

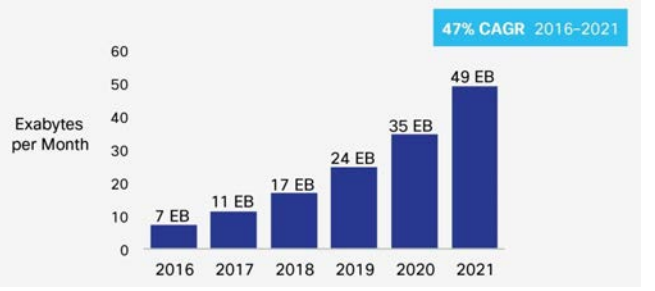


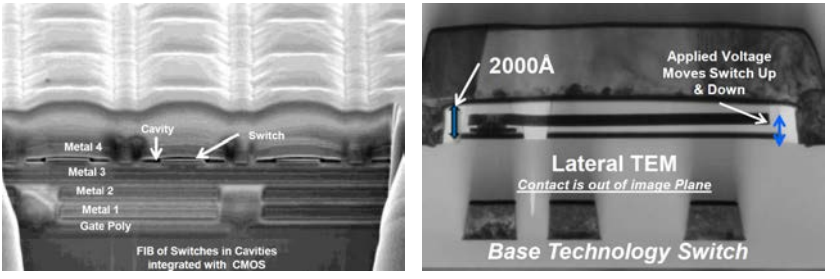
Figure 5.1: Cisco forecast: 49 exabytes per month of mobile data traffic by 2012. Mobile data traffic will grow at a compound annual grow rate (CARG) of 47 % from 2016 to 2021. Image extracted from [132].

Traditionally, MEMS devices and CMOS circuitry have been fabricated in separate chips eventually wire-bonded together, which resulted to be large and very expensive. As the semiconductor manufacturing process has become mature, the monolithic integration has been made possible. In fact, monolithic integration of RF MEMS with standard CMOS processes has been crucial to further optimizing key elements for its commercialization such as cost, size and easiness of integration, which has boosted the interest in the technology from the mobile handset companies [133].

Integrating MEMS devices into CMOS processes, yielding a miniature monolithic system solution, can be done in various ways as already explained in chapter X. We can distinguish three major principles according to when the MEMS device is implemented: pre-CMOS or MEMS-first, intra-CMOS and post-CMOS or MEMS-last.

It is of paramount importance to highlight that there are only two enterprises in direct competition in a market with a potential revenue growth: Cavendish Kinetics [35] and Wispry [134]. Both of them are selling commercial tunable digital capacitor arrays for (i) impedance matching with the purpose of maximizing the power transfer to the antenna and, (ii) for antenna tuning with the purpose of allowing to dynamically change its electrical length for a precise and more efficient tune to any available frequency band.

The Nanomech technology developed by Cavendish Kinetics employ an intra-CMOS approach for fabricating MEMS capacitive structures within a micro-cavity embedded in the CMOS back end metallization layer by using standard CMOS materials, deposition and etching techniques [36] (see Fig. 5.2(a)). Inside the cavity, the mechanical moving structures are fabricated from refractory metals which are also standard in the back end of line (see Fig. 5.2(b)).



(a) (b)

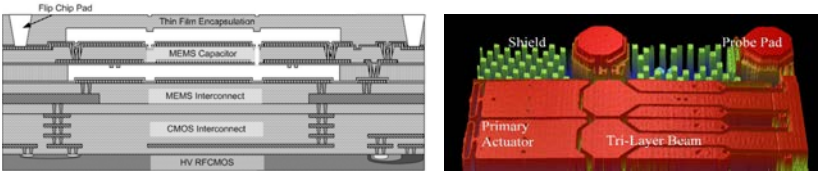
Figure 5.2: (a) FIB cross-section SEM image of 3rd generation Nanomech^{TM} MEMS switches embedded in the back end of a standard CMOS technology. (b) TEM cross-section image of a Nanomech^{TM} cantilever MEMS switch. Images extracted from [36].

A similar non-commercial approach is based on post-processing the back end of line (BEOL) layers of the CMOS technology is followed by [23, 25]. In fact, the use of the inherent layers of the CMOS process offers a good matching with the interfacing circuitry, fast turnaround fabrication time, reproducibility and yield, although some limitations arising from the design rules established by the CMOS IC process and the material properties are present [17].

Wispry developed RF MEMS switched capacitors using a HV 0.18 μm 50-V-LDMOS process following a post-CMOS approach. The CMOS elec-

tronics are initially integrated into the wafer, whereas the MEMS capacitor is fabricated separately on a fully planarized wafer with exposed vias for a subsequent interconnection to the CMOS circuits [135] (see Fig. 5.3(a)). The MEMS beam shown in Fig. 5.3(b) is comprised of a tri-layer heterogeneous composite and the air gap that separates the movable structure and the actuation electrode is formed by a 2 μm thick sacrificial layer, which is removed using a dry process before sealing the MEMS device in a cavity.

The structures evaluated in this chapter are based on miniature RF MEMS capacitive structures [136–139], which are fully integrated into the process flow of a low cost, commercial 180 nm CMOS technology (using the SilTerra MEMS-on-CMOS process platform). This method, in our view, is the most flexible and compact form of putting MEMS and CMOS together since it opens new possibilities for material selection and it can be easily exported to smaller CMOS technological nodes without affecting the MEMS on top of it. Furthermore, a low cost, low profile ZLP covers the MEMS cell, which ensures that it is never contaminated; avoiding thus reliability concerns.



(a) (b)

Figure 5.3: (a) Cross-section of the complete Wispry MEMS capacitor technology. (b) Optical profilometer (Wyko) image of a fabricated Wispry MEMS capacitor. Images extracted from [135].

5.2 Miniature Switched Capacitor

5.2.1 Device Design

The miniature MEMS-on-CMOS switched capacitor is based on a conventional serpentine flexure [45], similar to standard capacitive switches, but with highly reduced dimensions in order to attain larger spring constant for higher resonant frequency and increased restoring force (see Fig. 5.4). Tab. 5.1 summarizes the dimensions and material properties of the structure.

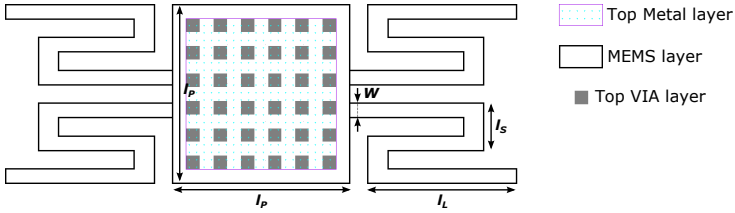


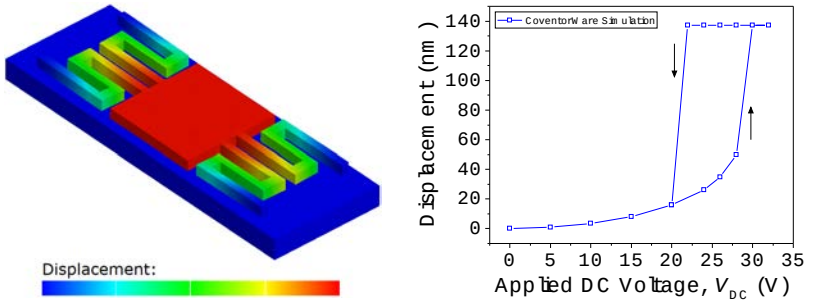
Figure 5.4: Illustration of the layout of the serpentine flexure MEMS structure.

Table 5.1: Dimensions and material properties of the designed structure.

	serpentine flexure width	w	0.35 μm
	serpentine flexure short length	l_S	1.2 μm
	serpentine flexure long length	l_L	2.5 μm
	plate length	l_P	4.6 μm
	thickness	t	500 nm
	actuation gap	g	135 nm
TiAlN	Young's modulus	E	165 GPa
	mass density	ρ_m	3860 kg/m^3
	electrical resistivity	ρ_e	332 $\mu\Omega$·cm

The proposed switched capacitor is electrostatically actuated by using the last layer of the CMOS technology as actuation electrode, which is located beneath the movable plate. When a voltage is applied, the movable plate is pulled down and the capacitance is increased. It is worth mentioning that even though the spring constant is higher than conventional designs, the pull-in voltage is kept at a relative low value (∼30 V) thanks to the nano-gap feature enabled by the SilTerra MEMS-on-CMOS technology as we will show in the next section.

Coventorware, a software based on the finite element method (FEM), was used to simulate the mechanical behavior. Fig. 5.5 shows the simulated mechanical response of the proposed capacitive switch. As the V_{DC} bias voltage is increased, the movable plate collapses at 30 V. By sweeping down the V_{DC}, the movable plate is released at 20 V. The simulated tuning ratio was found to be 6, from 1.46 fF to 7.9 fF. The parasitic inductance and the losses, which mostly arise from the serpentine flexures, were also simulated. The parasitic inductance I_S was found to be 12 pH at 1 GHz. The simulated losses led an equivalent resistance R_S of 207 Ω at 1 GHz.



(a) (b)

Figure 5.5: (a) 3D model of the switched capacitor actuated with V_{DC}=32 V. (b) Simulation result of the pull-in and release voltages.

5.2.2 Fabrication

The fabrication process flow of the switched capacitor, based on a similar process for MEMS resonators [17], is shown in Fig. 5.6. First, the electrodes are fabricated using the last via layer of the CMOS technology. Next, a polymer layer is deposited, patterned and thinned down to 90 nm. After that, the structural layer, which is a bimetallic nitride layer of 500 nm thick, is defined. Then, a nano-gap is formed by ashing the sacrificial layer. Finally, a thin-film metallic cover (also called ZLP) is deposited on top of the structural layer which is used as a protective shell for the structure.

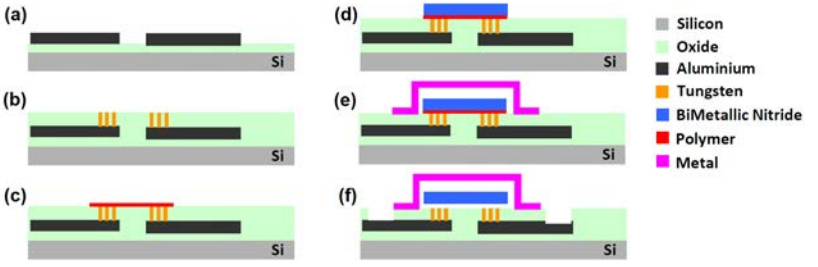
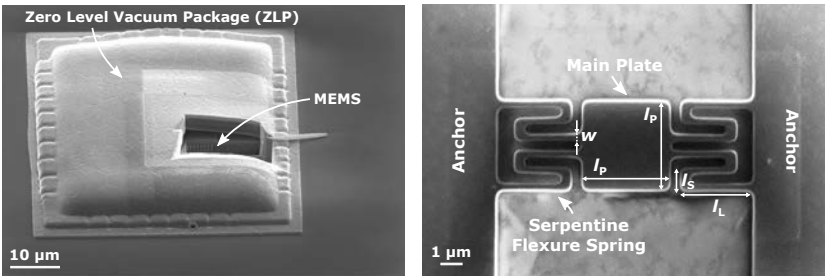


Figure 5.6: (a) Deposit and pattern CMOS top metal layer. (b) Via plug process. (c) Sacrificial polymer coat, pattern and etch. (d) Deposit and pattern resonator layer. (e) Release and zero-level packaging. (f) Release and bond pad.

Fig. 5.7 shows a focused ion beam (FIB) cut cross-sectional view of the packaged switched capacitor and a top view scanning electron microscope

(SEM) image of the structure indicating its dimensions. The active area is only 37 x 48 μm^2 including package.



(a) (b)

Figure 5.7: (a) Top view SEM image of the packaged MEMS-on-CMOS capacitor with a FIB cut showing the ZLP and the MEMS device. (b) Top view SEM image of a fabricated switched capacitor.

5.2.3 Experimental Results and Discussion

An Agilent E5071B NA was used to measure two-port S-parameters of the device from 100 MHz to 6 GHz. Short-Open-Load-Through (SOLT) calibration was done before the measurement to move the reference plane of the VNA to the probe tips. Open-short de-embedding was used to remove the effects of the on-chip probe pads. A script that performs an automated de-embedding and parameter extraction was developed with Matlab and it can be found in Appendix X.

The equivalent electrical circuit of the proposed capacitor can be modeled as series LCR circuit with two shunt capacitors as shown in Fig. 5.8. The capacitor C_S is the coupling capacitance between the actuation electrode and the movable plate. R_S and L_S are parasitic parameters associated to the capacitor. The shunt capacitances C_{1P} and C_{2P} model the coupling with the silicon substrate.

Fig. 5.9 presents the measured and modeled data summarizing the RF performance at up- and down-state of the switch along with equivalent scheme modeling using the equivalent electrical circuit shown in Fig. 5.8. Notice that the applied incident power is 0 dBm. The electrical characteristics of the capacitor are summarized in Tab. 5.2. Inductance and resistance has been extracted from simulation since it is not possible to experimentally measure the self-resonance with the available instruments.

Table 5.2: Electrical characteristics of the switched capacitor.

State	C_S (fF)	L_S (pH)	R_S (Ω)	C_{1P} (fF)	C_{2P} (fF)	Q @ 1GHz
Up-State	1.65	11.98[a]	207[a]	14.78	15.13	437
Down-State	3.2	11.98[a]	207[a]	11.97	11.42	239

[a]Inductance and resistance has been extracted from simulation.

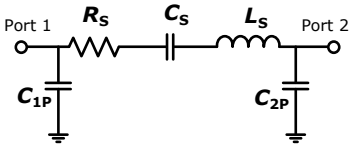


Figure 5.8: Equivalent electrical circuit model of the series switched capacitor. Parameter values are summarized in Tab. 5.2.

The measured Q-factor corresponding to the maximum capacitance (down-state position) is plotted as a function of the frequency in Fig. 5.10. The raw Q data, which is often noisy since accurately measuring a small real impedance in series with a large imaginary impedance is difficult [23], has been smoothed using a moving average over 10 data points. Extrapolation of the Q is performed using the theoretical formula, $Q = 1/\omega R_S C_S$, which results in a Q of 229 at 1 GHz.

The capacitance extracted from the measurement from 0 to 32 dc-bias voltage and over a frequency range of 1–6 GHz is plotted in Fig. 5.11, which shows to be almost constant. At 1 GHz, the achievable tuning of the proposed capacitor is found to be 1:1.9. The tuning response is plotted in Fig. 5.12. The plate is pulled-down at 30 and released at 16 V, which shows good agreement with CoventorWare simulations.

The switch was cycled 1700 times (pull-up and pulled-down consecutively) showing neither dielectric charging nor degradation 5.13, demonstrating thus a reliable performance; although failure mechanisms such as fatigue, dielectric charging, etc., may appear for a much larger number of actuation cycles [140].

The mechanical resonance of the capacitive switch was also characterized as shown in Fig. 5.14. The natural frequency (extrapolated at V_{DC}=0 V) is 6.28 MHz, which is also in accordance with 7.46 MHz obtained by CoventorWare mechanical simulations. From a standard resonant model [45], the switching time can be computed, which results in only 77.5 ns, being faster compared to traditional capacitive switches [45]. Tab. 5.3 summarizes the experimental results.

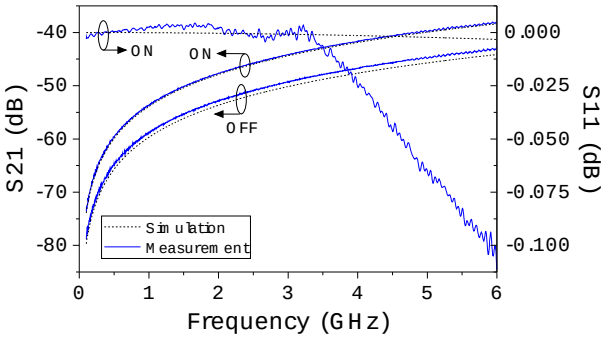


Figure 5.9: Measured (solid line) and equivalent electrical scheme (dashed line) responses of the fabricated switch when is off (V_{DC}=0 V) and on (V_{DC}=36 V).

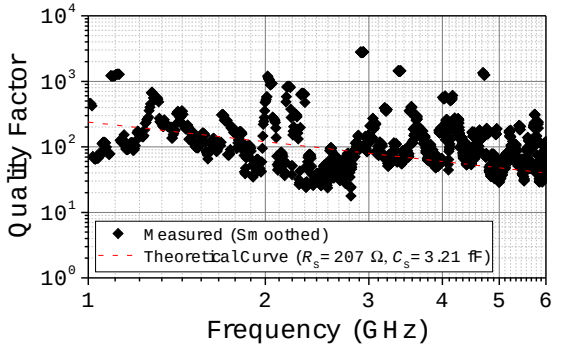


Figure 5.10: Measured Q-factor as a function of the frequency, corresponding to the on-state. Theoretical curve fit with $R_S = 207\ \Omega$ and $C_S = 3.21$ fF.

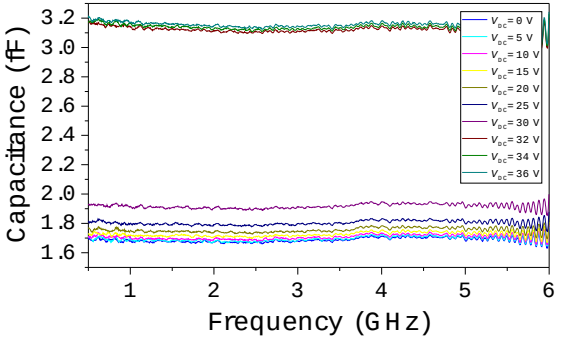


Figure 5.11: Measured extracted capacitance versus frequency for different actuation voltages V_{DC} from 0 to 36 V.

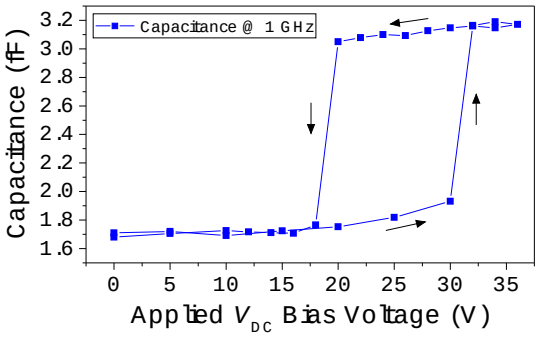


Figure 5.12: Measured extracted capacitance at 1 GHz over an actuation voltage V_{DC} from 0 to 36 V.

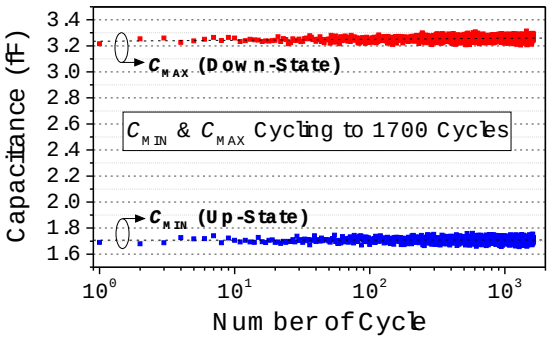


Figure 5.13: Preliminary reliability test for 1700 cycles showing neither dielectric charging nor degradation.

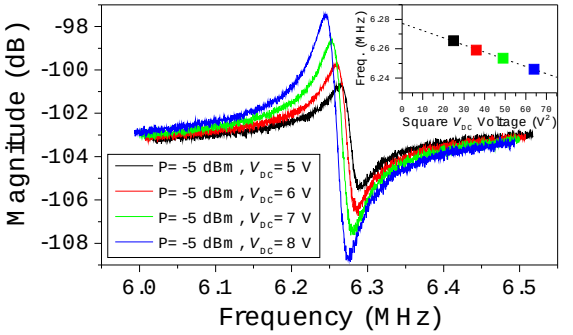


Figure 5.14: Mechanical frequency response of the capacitive switch. The inset shows the resonance versus applied V_{DC} voltage to the square.

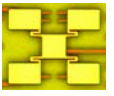
Table 5.3: Summary of the electrical characteristics of the switched capacitor.

Pull-in/Pull-out Voltage, V_{PI}/V_{PO}	30 V/18 V
Mechanical Resonant Frequency, f_0	6.28 MHz
On-State/Off-state Capacitance, C_{ON}/C_{OFF}	3.2 fF/1.65 fF @ 1 GHz
Quality Factor, Q	239 @ 1 GHz

5.3 Miniature MEMS-on-CMOS Array

The capacitance of a single miniature MEMS-on-CMOS switched capacitor is too small to be useful at RF frequencies (C_{MIN}-C_{MAX}=1.65-3.21 fF). The capacitance target ranges from 0.1 fF up to 5 pF [35, 134]. So, in order to obtain higher capacitance values, new MEMS devices with larger coupling areas were designed (see Tab. 5.4 for further details) and placed in paral-

Table 5.4: New designed switched capacitors targeting larger coupling areas.

	Layout	Dimensions	$C_{MIN} - C_{MAX}$	R_S [Ω]	f_0 [MHz]
VFFS01		l=5 μm w=0.75 μm A_C=10x10 μm^2	5.65 - 10.735 fF	100	5.26
VFFS02		l=4.9 μm w=1.25 μm A_C=20x20 μm^2	22.64 - 43.02 fF	100	2.3
VSS01		l_L=5 μm l_S=2 μm w=0.75 μm A_C=10x10 μm^2	5.65 - 10.735 fF	100	4.46
VSS02		l_L=4.25 μm l_S=3.25 μm w=1.25 μm A_C=20x20 μm^2	23.14 - 43.97 fF	100	1.7
TP01		Membrane-like anchoring A_C=25.4x25.4 μm^2	40.1-76.19 fF	100	2.7
TP02		Membrane-like anchoring A_C=25.4x25.4 μm^2	49.14 - 93.37 fF	100	2.26
TP03		Membrane-like anchoring A_C=30x30 μm^2	58.7 - 111.53 fF	100	2

lel forming an array of N elements. Tab. 5.5 shows the different implemented arrays indicating the different expected capacitance ranges of operation.

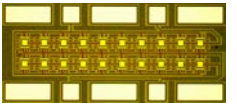
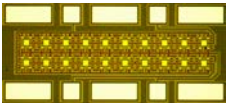
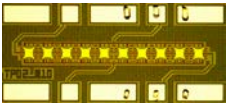
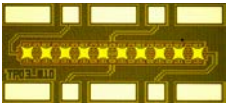
A space-limiting technological restriction has to be first considered for the design of new structures. The maximum ZLP area allowed is a square area of 30 μm x 30 μm. So, the designed structures, including coupling area and spring spaces, must not be larger than such a areal restriction.

A trade-off between low pull-in and high Q has to be also considered when designing spring suspended parallel-plate varactors. First, its Q is limited by the series resistance of the supporting springs. Second, achieving low actuation voltage requires the use of long springs, thus imposing such a conflicting trade-off.

Taking into account the former, three different spring shapes designs with different coupling areas were fabricated: vertical fixed-fixed spring

(VFFS) (see Fig. 5.15(a) and 5.15(b)), vertical serpentine spring (VSS) (see Fig. 5.15(c) and 5.15(c)), and tent plate spring (TP) (see Fig. 5.15(d)). Fixed-fixed springs present higher Q but higher V_{PI}, whereas the contrary to serpentine spring designs. Tent plate spring design is engineered such that it presents higher Q thanks to its membrane-like anchoring and relatively low actuation voltage due to its larger coupling area.

Table 5.5: New designed switched capacitors arrays.

	Layout	**Number of Elements**	Tuning Range ($C_{MIN} - C_{MAX}$)
VFFS02_N20		20	453 - 860 fF
VSS02_N20		20	462.8 - 880 fF
TP02_N10		10	491.4 - 934 fF
TP03_N10		10	587-1120 fF

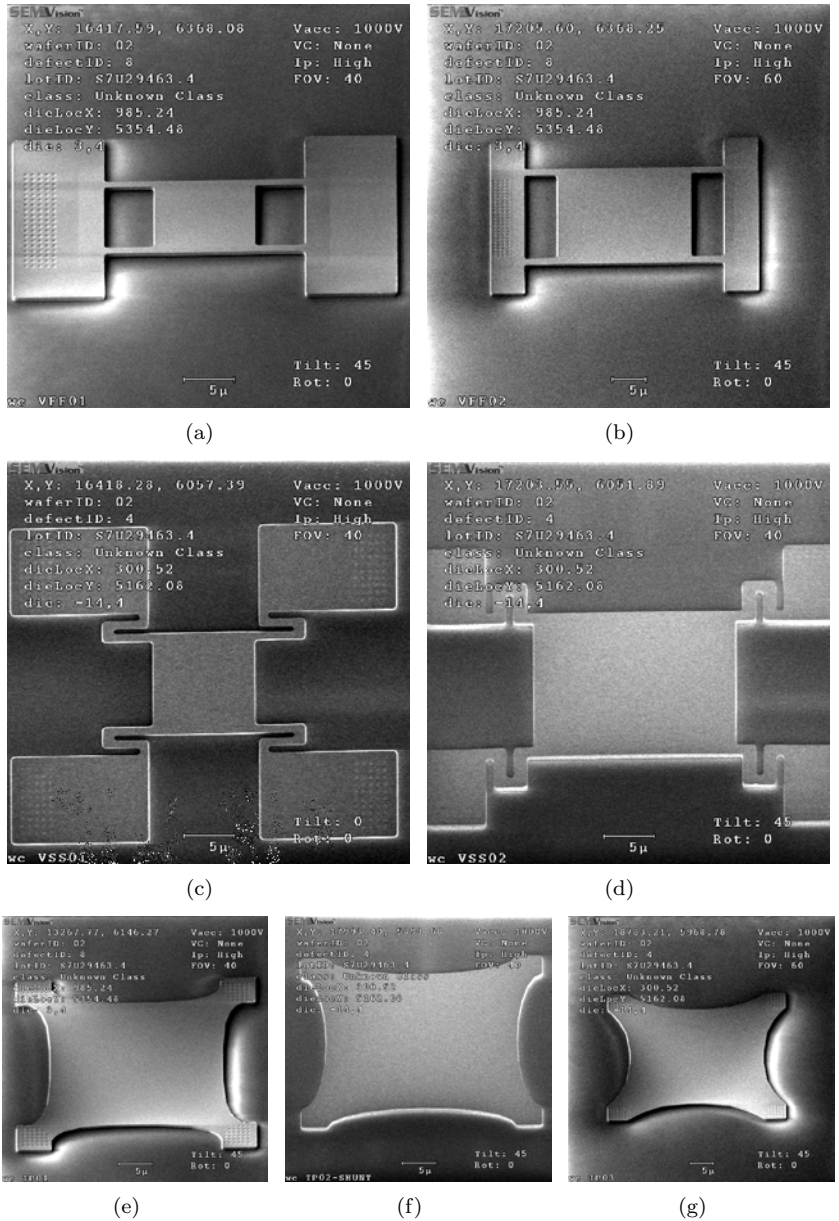
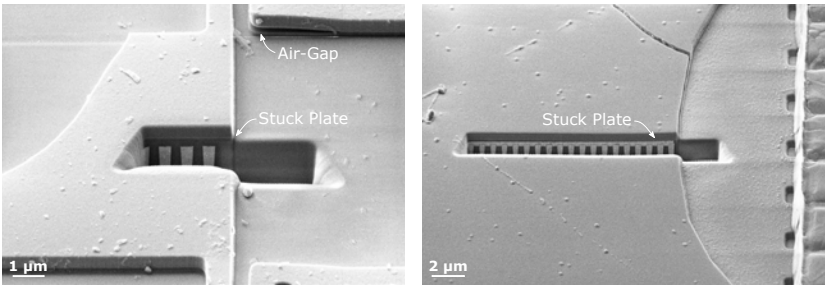


Figure 5.15: Top view SEM images of fabricated switched capacitors targeting larger coupling areas: (a) VFFS01, (b) VFFS02, (c) VSS01, (d) VSS02, (e) TP01, (f) TP02 and (g) TP03.

The first lot of fabricated devices were fabricated following the same fabrication process used for resonators, with a nominal air-gap of 90 nm. Preliminary SEM inspection showed a proper fabrication (see Fig 5.15). However, it was found the fabricated devices to be stuck on the bottom surface as shown in Fig. 5.16. In fact, the fabrication of such a large-area varactors supposed a challenge since SilTerra ESR technology was optimized for resonators of smaller dimensions.



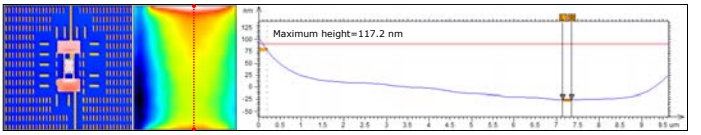
(a) (b)

Figure 5.16: FIB-cut cross-sectional SEM images taken in (a) VFFS01 and (b) TP01 of the first lot of fabricated devices.

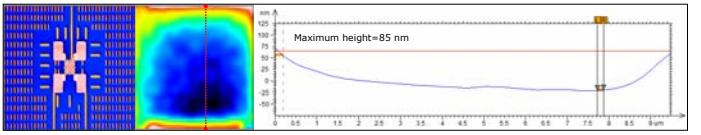
In order to overcome the former issue, a second lot of devices was fabricated with an increased nominal gap of 300 nm. The structures were not stuck this time although it was found an important curvature on the plates. The direct cause of such a bending in the plate of the capacitors is the presence of residual stresses or stress gradients. This bending causes the measured off-capacitance to be higher than the initially designed one, thus reducing the expected tuning range. For this reason, it is very important to study the severity of this effect.

The curvature of each structure was then analyzed by the Leica DCM 3D confocal microscopy, measuring a 2-D profile in punctual structures at the center of the wafer as shown Fig. 5.17. The maximum curvature measured in each structure is summarized in Tab. 5.6.

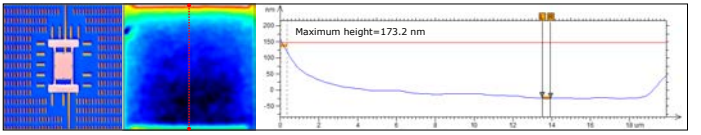
A parametric study was conducted by CoventorWare in order to study the resonant frequency dependence applying residual stress σ ranging from -500 to 500 MPa on the two smallest structures (VFFS01 and VSS02). We found that the f_0 of the serpentine spring compared to the fixed-fixed one changes only a 3.52 % versus a 68.75 % over the simulated range (see Fig. 5.18 and 5.19). Thus, serpentine spring design is more robust against residual stress since it releases the residual stress by expansion.



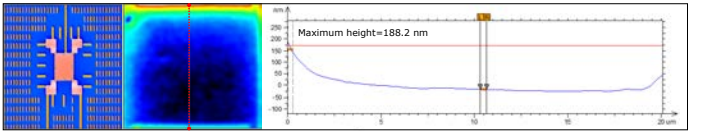
(a) VFFS01 2-D Profile



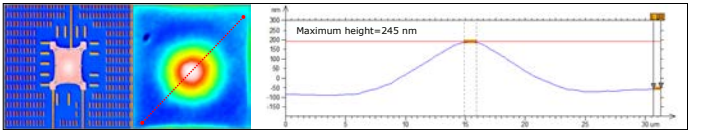
(b) VSS01 2-D Profile



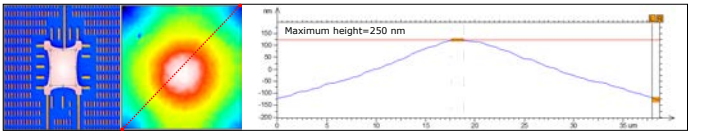
(c) VFFS02 2-D Profile



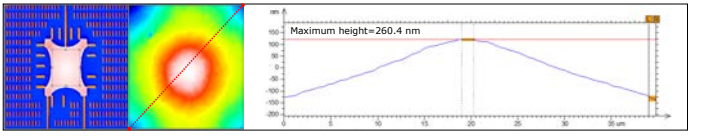
(d) VSS02 2-D Profile



(e) TP01 2-D Profile



(f) TP02 2-D Profile



(g) TP03 2-D Profile

Figure 5.17: Measured profile with a Leica DCM 3D confocal microscopy of the different fabricated capacitors: top view and 2-D profile-line.

Table 5.6: Summary of measured maximum curvature on each fabricated structure with a Leica DCM 3D confocal microscopy.

MEMS Structure	Maximun Curvature
VFFS01	117.2 nm
VSS01	85 nm
VFFS02	173.2 nm
VSS02	188.2 nm
TP01	245 nm
TP02	250 nm
TP03	260.4 nm

Fig. 5.20 shows the experimentally measured resonant frequency of both VFFS01 and VSS01 structures. The extrapolated f_0 of both VFFS01 and VSS01 structures at V_{DC}=0 V is 6.394 MHz and 4.145 MHz (see insets in Fig 5.20(a) and 5.20(b) respectively). We observe a higher experimental f_0 respect to the simulated f_0 with no stress. This means that the plate exhibits a tensile stress causes an increase in the bending stiffness and thereby a higher f_0.

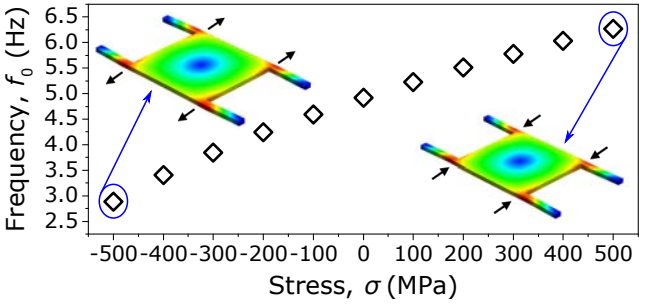


Figure 5.18: Simulated f_0 of the VFFS01 for different residual stress σ.

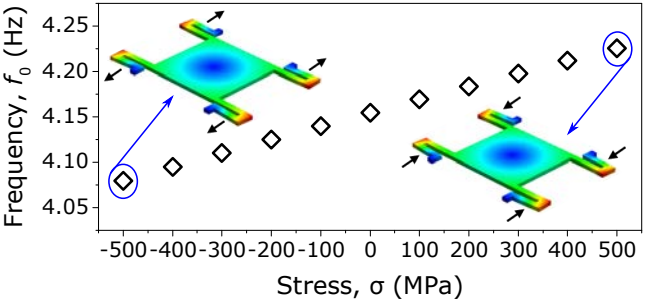
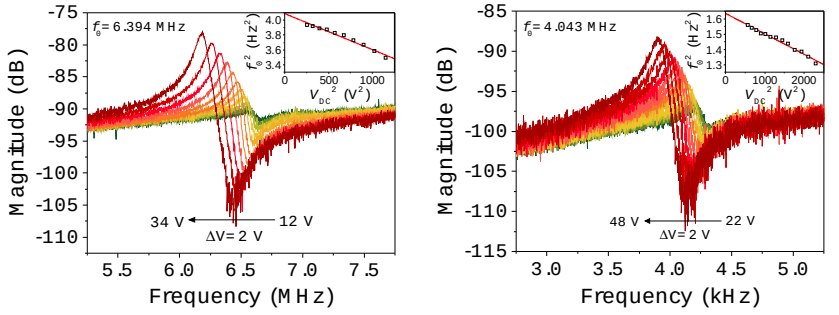


Figure 5.19: Simulated f_0 of the VSS01 for different residual stress σ.



(a) (b)

Figure 5.20: Experimental magnitude-frequency response for different V_{DC} bias voltages of the VFFS01.

The new fabricated devices were electrically characterized following the same experimental measurement procedure as for the single miniature switched capacitor described formerly.Even though having experimental evidence that the standard VIA-electrode avoid early breakdown, achieving a tuning range of 1:1.9 with the single miniature capacitor; it was found the capacitors to burn out once the plate is pulled in towards the actuation electrode by applying a sufficiently high DC-bias voltage. In fact, the VIA-electrode is exposed, i. e. it is not covered by an insulating oxide as shown in Fig. 5.21. We believe that the large plate area causes to have an increased contact area once the plate is pulled in, thus irremediably provoking catastrophic breakdown.

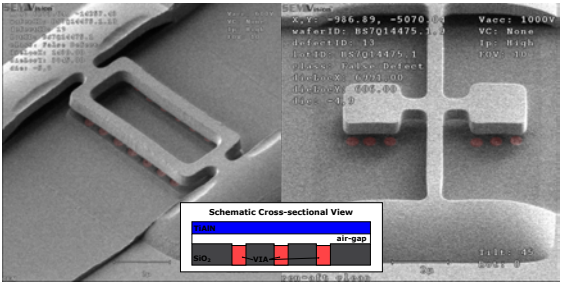


Figure 5.21: SEM images of two different fabricated resonators in which the standard VIA-electrode can be apreciated (colored in red).

As a conclusion, a miniature zero-level packaged switched capacitor fully integrated into the standard process flow of a 180 nm CMOS technology was firstly electrically characterized, showing good performance: a

capacitance change between 1.65 fF and 3.2 fF (TR=1:1.9) with a high Q-factor of 239 at 1 GHz. Thus, the characterized device was an attractive candidate for implementing compact digital-like variable capacitor with a S2P/I2C interface. However, the capacitance of such a single miniature switched capacitor is too small to be useful at RF frequencies. So, new capacitors targeting larger areas for higher capacitance were designed and fabricated, which resulted quite challenging. Two critical issues worsened the performance and made them uncompetitive. First, residual stress present in the structural material caused an important bending on the plates, which makes measured off-capacitance to be higher than the initially designed one, thus reducing the expected tuning range. Second, once the plate is pulled in towards the actuation electrode by applying a higher DC-bias voltage than the pull-in voltage, the capacitor is burned out. Thus, limiting even more the expected tuning range.

So, towards developing varactors with the ESR-MEMS Silterra technology, it is needed to "re-think" or optimize the platform by i) putting an effort on further reducing the residual stress that the bigger structures exhibit, and ii) defining an insulating dielectric layer on top of the standard VIA-electrode to avoid catastrophic breakdown. We may also think in improving even more the tuning range by (iii) leveraging the ZLP as upper actuation electrode.

Conclusions

Herein, the general conclusions of this thesis are given, followed by some some suggestions for future research upon potential applications to the MEMS field.

General Conclusions

The main contributions of the present dissertation are summarized below.

- **Design, fabrication and characterization of micro- and nano-electromechanical (M/NEM) relays.**

  Back end embedded M/NEM relays were succesfully fabricated using the available BEOL layers of the conventional AMS 0.35 μm CMOS technology.

  Two different approaches were explored:

  - Laterally actuated NEM relays based on tungsten VIA3 layer.
  - Torsionally actuated composite MEM relays based on MET4-VIA3-MET3 stack while supported by tungsten VIA3 layer.

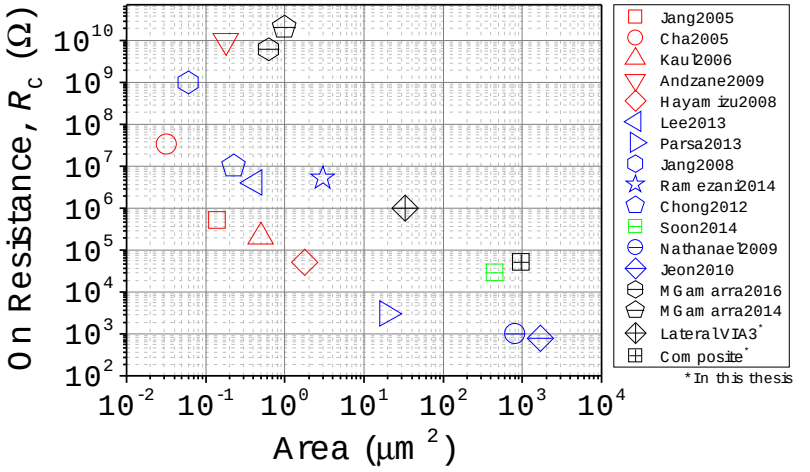
  In particular, both approaches are supported by the tungsten VIA3, which has shown to be a versatile platform. Regarding the fabrication, various novel characteristics have been demonstrated, which can be incorporated as new design rules for future CMOS-MEMS integration:

  - The minimum VIA3-to-VIA3 lateral gap achievable is 400 nm.
  - Long beams up to 50 μm have been successfully fabricated.
  - Flatter lateral sidewalls can be defined if MET3 is not defined below VIA3.
  - Out-of-plane vertical gaps of approximately 400 nm can be achieved if VIA3 is used as structural MEMS material and VIA2 is used as electrode.

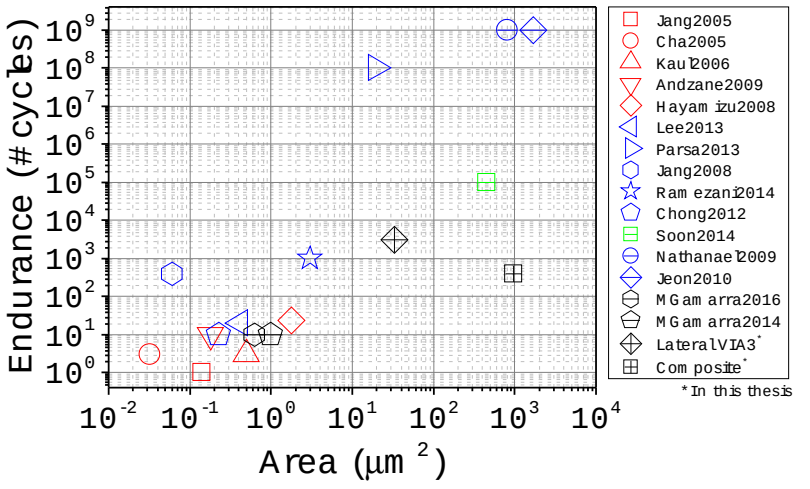
– Tungsten VIA3 platform has shown low residual stress. An horizontal beam of 30 μm has shown a curl up of about 100 nm (characterized with a confocal microscope).

Regarding the device performance, the third generation of lateral VIA3-based NEM relays showed an abrupt jump of 7 orders of magnitude with a super-steep switching transition of only 285 μV/dec, and a very stable pull-in voltage of 31.25 V with an absolute variation of only 0.5 V (over $3 \cdot 10^3$ cycles), demonstrating in this sense a very robust platform. Even though an initial R_C of less than 1 MΩ was obtained, it shots up from this 1 MΩ to 100 MΩ in less than 200 cycles, which becomes a major challenge in implementing logic circuits.
On the other hand, torsional MEM relays has also shown an abrupt jump of up to 10^8 with a subthreshold swing of 58 mV/dec (based on the voltage step of 348 mV), and a nominal V_{PI} of 57 V over 355 cycles with an absolute variation of 0.75 V. Even though exploring different contact interfaces such as TiN vs. TiN, W vs. TiN and W vs W with the same structure, the results showed in general lower R_C (of the order of tens of kΩ) but again poor endurance (up to $4 \cdot 10^2$ cycles).

Fig. 5.22 shows a representative view of the actual state of the art of the M/NEM relay technology. According to the coupling area versus the on-state contact resistance (see Fig. 5.22(a)) and the device endurance (see Fig. 5.22(b). Compared to bottom-up approaches, the developed relays show superior performance. Compared to top-down approaches with similar dimensions, the developed relays show competitive on-state contact resistance being fully integrated in a standard CMOS process, although lower endurance. Notice though that, depending on the final applications, such reliability issues would not be as critical as in those relays intended for logic applications. It has also to be highlighted that the switches developed in this thesis show superior performance to previously developed back-end embedded NEM relays at expense of an obvious increase of the device area.



(a)



(b)

Figure 5.22: Representative state of the art of the M/NEM relay technology. (a) On-state contact resistance R_C versus coupling area and (b) device endurance (number of cycles) versus coupling area. Devices in red color are developed using a bottom-up approach. Devices in blue color are top-down full-custom approaches. Device in green color is based on a SOI process. Devices in black color are CMOS/BEOL-embedded. *Indicates the devices developed in this thesis.

- **Design and fabrication of a dual-mode MEMS resonators based on the relays' platform for implementing a dual-frequency oscillator.**

  A dual-mode MEMS resonator based on the VIA3 platform used for the development of the torsional MEM relays was also fabricated. This dual-mode resonator was used for implementing a dual-frequency oscillator with the use of a transimpedance (TIA) amplifier developed by G. Sobreviela. The oscillator can be operated with reduced TIA supply voltage (V_{DD}=1.65 V) and moderated dc MEMS bias (V_{DC}=18 V) while consuming only 8.5 μW and maintaining satisfactory performance. The measured phase noise is -103.8 dBc/Hz and -99.6 dBc/Hz at 1-kHz offset for the first and second operating frequencies, respectively, which is comparable and competitive with the state of the art. In this sense, the proposed oscillator contributes to the emerging IoT scenario in which low-power and ultra-compactness are indispensable features, being fully integrated with CMOS and compatible with other on-chip MEMS sensors.

- **Study and characterization of RF MEMS switched capacitors using the SilTerra MEMS-on-CMOS platform.**

  A miniature zero-level packaged switched capacitor fully integrated into the standard process flow of a 180 nm CMOS technology was electrically characterized, showing a capacitance change between 1.65 fF and 3.2 fF (TR=1:1.9) with a high Q-factor of 239 at 1 GHz. However, the capacitance a single miniature switched capacitor is too small to be useful at RF frequencies. So, new capacitors targeting larger areas for higher capacitance were designed and fabricated with the SilTerra MEMS-on-CMOS platform. Unfortunately, those devices yielded poor results, mainly due to the residual stress present in the structural material and the early breakdown of the capacitor after being pulled-in. Therefore, towards developing MEMS tunable capacitors with the ESR-MEMS Silterra technology, it is needed to "re-think" or optimize the platform by (i) putting an effort on further reducing the residual stress that the bigger structures exhibit, and (ii) defining an insulating dielectric layer on top of the standard VIA-electrode to avoid early catastrophic breakdown. We may also think in improving even more the tuning range by for instance (iii) leveraging the ZLP as upper actuation electrode.

Suggestions for Future Research

- **Identification of potential application for the developed BEOL-embedded NEM relays.**

Regarding the most promising results obtained, the third generation of lateral VIA3-based NEM relays (the hammer-shaped relay) showed an initial R_C of 1 MΩ, with a super steep transition of only 286 μV/dec and a I_{ON}/I_{OFF} jump of 7 orders of magnitude. However, the R_C shots up from the initial 1 MΩ to 100 MΩ in less than 200 cycles, and finally reaches values above 10 GΩ when cycled $3 \cdot 10^3$ times (see Fig. 3.21(b)). Note that we need the device endurance exceed 10^{16} cycles, so that a relay-based microcontroller for embedded sensor applications could operate reliable for ten years at a clock frequency of up to 100 MHz [141]. We worked in the line of improving the device performance by coating the contact with Pt and Ru, although it did yield poor results. Therefore, we are far form being able to apply the developed relays for logic applications. For this reason, we may think in other potential applications for the developed relays. We encourage the future research line towards applying the developed BEOL-embedded NEM relays in the field of mass sensing, which has been a main stream during the last years [142].

In general, resonant mass sensing is based on detecting a change in the mass of the resonator as a change in the resonance frequency of the resonator [143]. However, adsorbate stiffness and surface stress effects can also change the overall stiffness of the resonator [144]. Hence, the assertion $\Delta m = R^{-1} \cdot \Delta\omega_0$, where $\Delta\omega_0$ is the frequency shift in the resonance frequency, Δm is the change in mass and R^{-1} is the inverse mass responsivity, is no longer valid.

A way to decouple mass and stiffness effects, within the framework of the nanoelectromechanical systems (NEMS), is by taking advantage of the electrostatic pull-in instability [145]. Since the pull-in voltage, V_{PI}, only depends on the stiffness and not on the mass, one can directly determine changes in bending stiffness by carefully looking for a change in the V_{PI}. The occurrence of the V_{PI} can be determined by optical methods through an external setup comprised by an optical microscope with a charge-coupled device (CCD) camera, which has been shown to be a versatile and robust method [145, 146].

We suggest that both pull-in and frequency shift changes can be determined fully electrically, which none of the previous works has dealt with.

The key benefit of this method is its simplicity against the complexity of an optical setup because it provides on-chip testing capabilities, which will be an advantage for fully-integrated systems. For this purpose, we could use the third generation of lateral VIA3-based NEM relays, which features a very stable pull-in voltage of 31.25 V (see Fig. 5.23(a) and 5.23(b)) and a resonant frequency of 457 kHz (see Fig. 5.23(c)), which can be easily determined via electrical measurements.

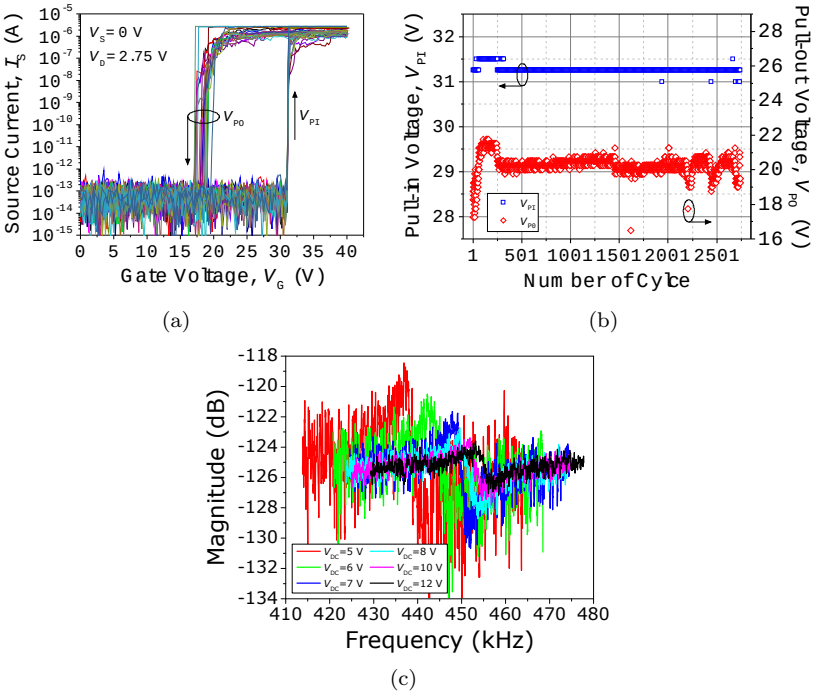


Figure 5.23: (a) Measured first 20 I-V switching characteristics of the hammer-shaped relay. (b) Evolution of the V_{PI}, V_{PO} over 2800 cycles. (c) Measured frequency response of the hammer-shaped relay for different dc bias voltages.

To show the applicability of the characterized device, successive mechanical simulations of depositions of thin layers of magnesium fluoride (MgF_2) over the entire length of the relay have been performed by means of CoventorWare (considering a mass density ρ=3180 kg/m^3 and a Young's modulus E=138 GPa). Fig. 5.24 presents the simulation results of the shift in the V_{PI} and the resonant frequency f_0 of the presented device versus the ratio of thicknesses of the added thin film layer t_a and the cantilever t_h. This result clearly confirm that the shifting in the V_{PI} starts to be

significant at a ratio of 0.05.

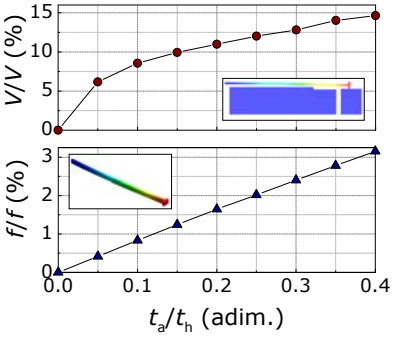


Figure 5.24: Simulated shift in the V_{PI} and the f_0 versus ratio between the thickness of the added mass t_a and the relay t_h.

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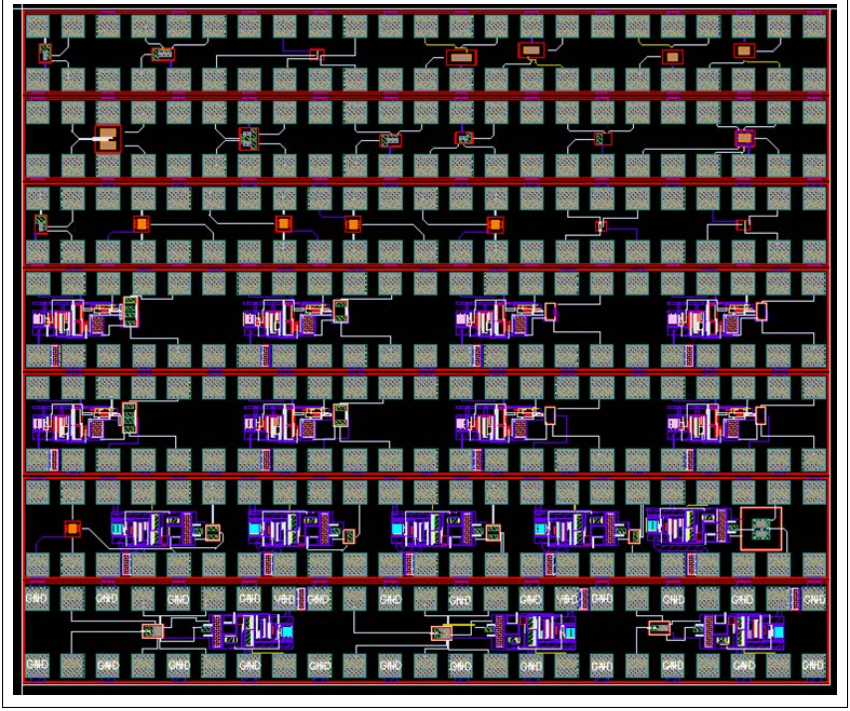
Appendices

Appendix A

RUNs Description

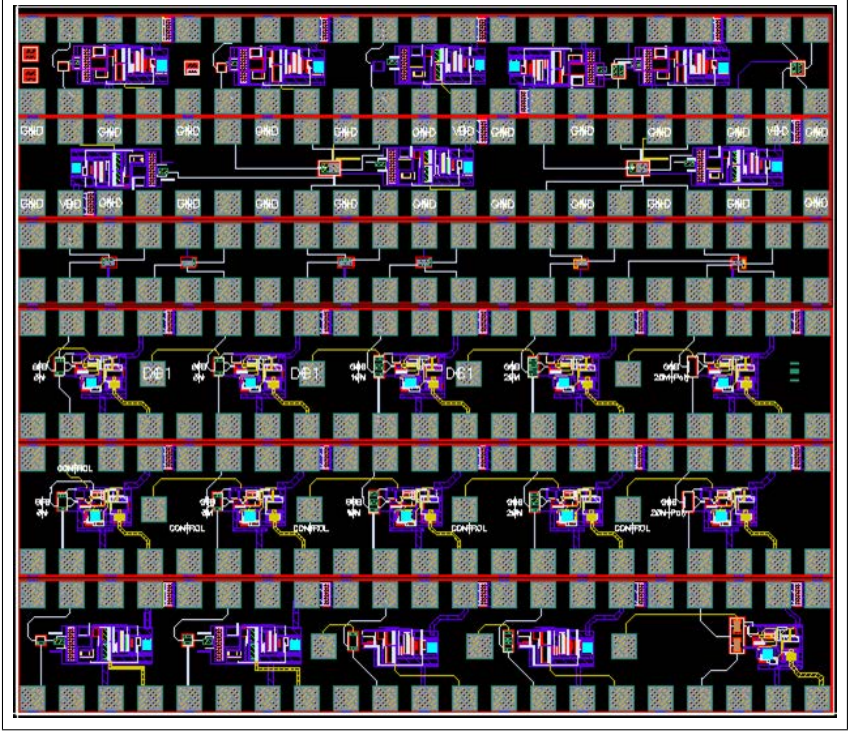
B.1 RUN March 2013

Technology: AMSC35B4C3	**Area:** 2795 x 3320 μm^2	**#chips:** 40
MEMS devices: 1G lateral tungsten VIA3-based NEM relays		



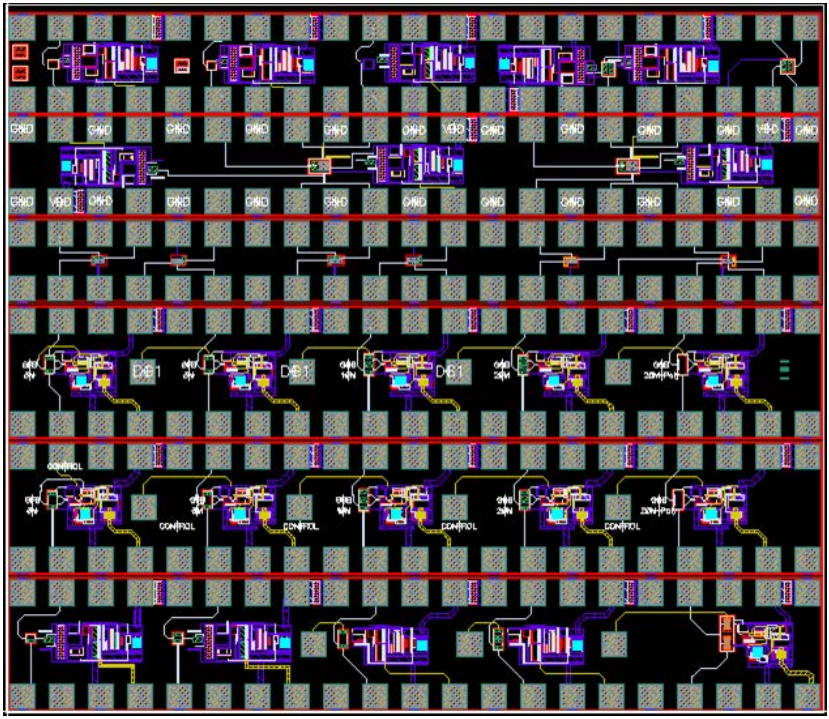
B.2 RUN February 2014

Technology: AMSC35B4C3	**Area:** 2328 x 3110 μm^2	**#chips:** 40
MEMS devices: 2G lateral tungsten VIA3-based NEM relays 1G Torsional Composite MEM Relays		



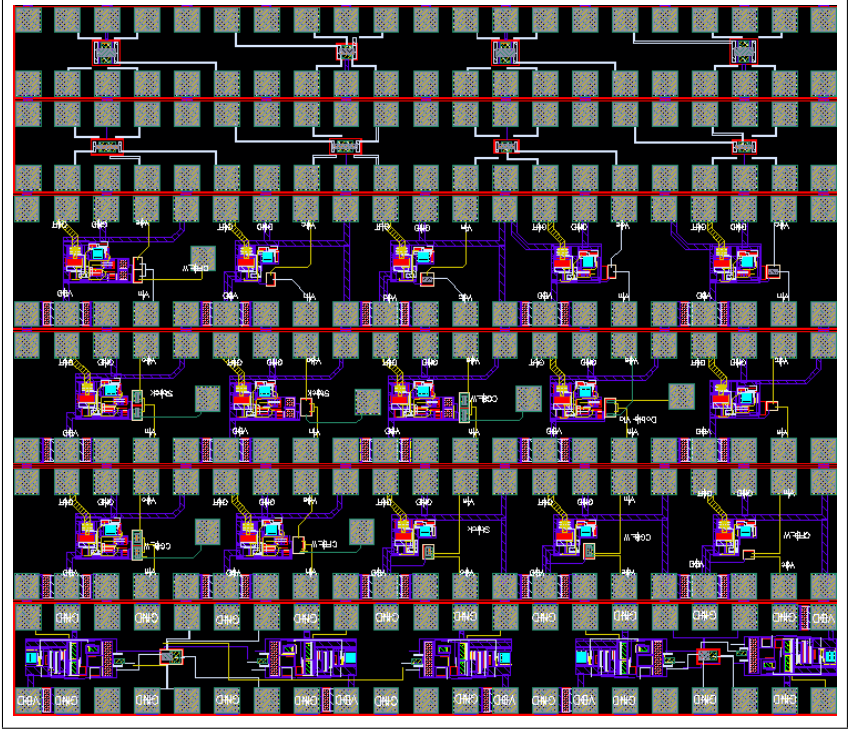
B.3 RUN July 2014

Technology: AMSC35B4C3	**Area:** 2670 x 3110 μm^2	**#chips:** 42
MEMS devices: 3G lateral tungsten VIA3-based NEM relays		



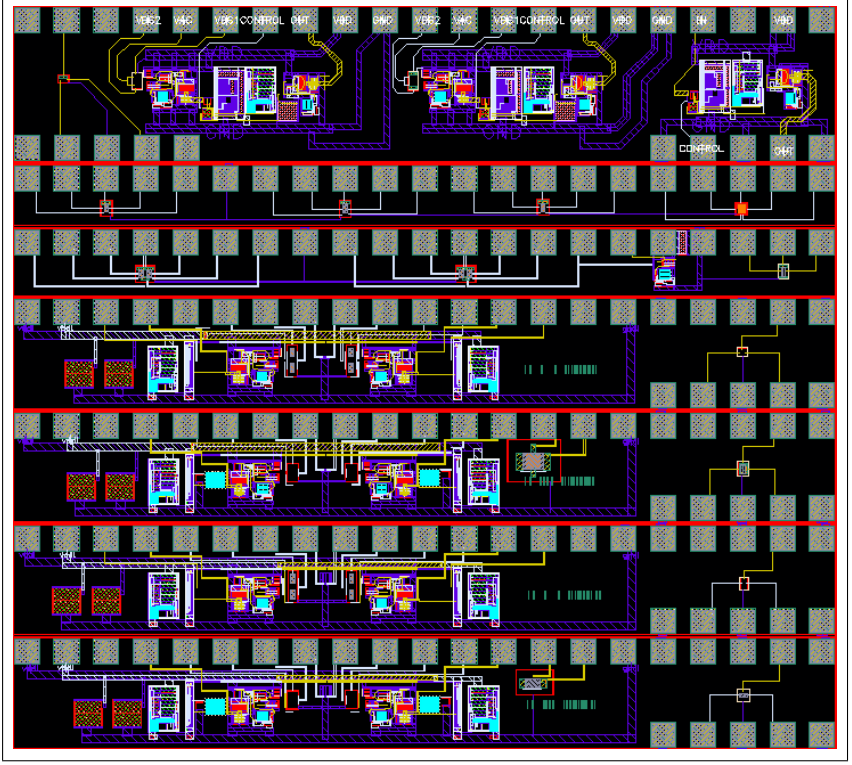
B.4 RUN May 2015 (1)

Technology: AMSC35B4C3	**Area:** 3120f x 3280 μm^2	**#chips:** 40
MEMS devices: 3G of lateral tungsten VIA3-based NEM relays 2G Torsional Composite MEM Relays Torsional VIA3 platform-based resonators		



B.4 RUN May 2015 (2)

Technology: AMSC35B4C3	**Area:** 2765 x 3110 μm^2	**#chips:** 42
MEMS devices: 3G lateral tungsten VIA3-based NEM relays 2G Torsional Composite MEMS Relays Torsional VIA3 platform-based resonators		



Appendix B

Author Contributions

C.1 Peer-Reviewed Publications

M. Riverola, G. Sobreviela, F. Torres, A. Uranga, and N. Barniol, "Single-Resonator Dual-Frequency Oscillator with Low-Power and Ultra-Compact TIA Core", *IEEE Electron Device Letters*, vol. 38, no. 2, pp. 273–276, 2017.

G. Sobreviela, **M. Riverola**, F. Torres, A. Uranga, and N. Barniol, "Optimization of the Close-to-Carrier Phase Noise in a CMOS–MEMS Oscillator Using a Phase Tunable Sustaining-Amplifier", *IEEE Transactions on Ultrasonics, Ferroelectrics, and Frequency Control*, vol. 64, no. 5, pp. 888–897, 2017.

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C.2 Contributions to Scientific Conferences

M. Riverola, A. Uranga, F. Torres, and N. Barniol, "Fabrication and Characterization of a Hammer-Shaped BEOL-Embedded CMOS-Nano-Electro-Mechanical Relay", in *43rd International Conference on Micro and Nanoengineering*, Braga, Portugal, 2017.

M. Riverola, A. Uranga, F. Torres, N. Barniol, E. Marigó, and M. Soundara-Pandian, "A Reliable Fast Miniaturized RF MEMS-on-CMOS Switched Capacitor with Zero-Level Vacuum Package", in *IEEE MTT-S International Microwave Workshop Series on Advanced Material and Processes*, Pavia, Italy, 2017.

G. Sobreviela, **M. Riverola**, F. Torres, A. Uranga, and N. Barniol, "Ultra Compact CMOS-MEMS Oscillator based on a Reliable Metal-Via MEMS Resonators with Noise-Matched High-Gain Transimpedance CMOS Amplifier", *proc. 19th International Conference on Solid-State Sensors, Actuators and Microsystems (TRANSDUCERS)*, Kaohsiung, Taiwan, 2017, pp. 1943–1946.

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M. Riverola, G. Sobreviela, A. Uranga, and N. Barniol, "Intrinsic Feedthrough Current Cancellation in a Seesaw CMOS-MEMS Resonator for Integrated Oscillators", *proc. IEEE International Frequency Control Symposium (IFCS)*, New Orleans, LA, USA, 2016, pp. 1–4.

G. Sobreviela, **M. Riverola**, A. Uranga, N. Barniol, E. Marigó, and M. Soundara-Pandian, "Passive Temperature Compensation Method in Nonlinear NEMS Resonators based on the Nunlinear Duffing Effect", *proc. IEEE International Frequency Control Symposium (IFCS)*, New Orleans, LA, USA, 2016, pp. 1–4.

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