Two-Dimensional Analytical Modeling of Tunnel-FETs

Michael Gräf

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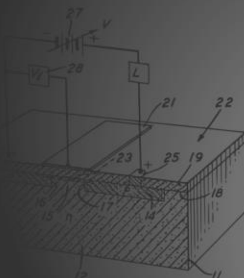

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TWO-DIMENSIONAL ANALYTICAL MODELING OF TUNNEL-FETS

DOCTORAL THESIS

Supervised by Prof. Dr. Benjamín Iñíguez
and Prof. Dr.-Ing. Alexander Klös

Department of Electronic,
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Universitat Rovira i Virgili

Tarragona
2017

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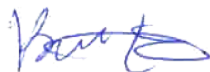

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"An investment in knowledge always pays the best interest."

Benjamin Franklin

List of Publications

Journals

- M. Graef, T. Holtij, F. Hain, A. Kloes, B. Iñíguez, "A 2D Closed Form Model For The Electrostatics in Hetero-Junction Double-Gate Tunnel-FETs for Calculation of Band-to-Band Tunneling Current", Microelectronics Journal, Vol. 45, No. 9, 2014

Conferences

- M. Graef, F. Hain, F. Hosenfeld, F. Horst, A. Farokhnejad, B. Iñíguez, A. Kloes, "Comparative Numerical Analysis and Analytical RDF-Modeling of MOSFETs and DG Tunnel-FETs", MIXDES 2016, Lodz, Poland, 2016
- M. Graef, T. Holtij, F. Hain, F. Hosenfeld, B. Iñíguez, A. Kloes, "Numerical Analysis and Analytical Modeling of RDF in DG Tunnel-FETs", EuroSOI-ULIS 2016, Vienna, Austria, 2016
- M. Graef, F. Hain, F. Hosenfeld, B. Iñíguez, A. Kloes, "Advanced Analytical Modeling of Fabricated Nanowire Tunnel-FETs", Nanoelectronic Days 2015, Juelich, Germany, 2015
- M. Graef, F. Hain, F. Hosenfeld, B. Iñíguez, A. Kloes, "Analytical Approach to Consider Gaussian Junction Profiles in Compact Models of Tunnel-FETs", EuroSOI/ULIS 2015, Bologna, Italy, 2015
- M. Graef, T. Holtij, F. Hain, A. Kloes, B. Iñíguez, "Improved Analytical Potential Modeling in Double-Gate Tunnel-FETs", MIXDES 2014, Lublin, Poland, 2014
- M. Graef, T. Holtij, F. Hain, A. Kloes, B. Iñíguez, "Two-Dimensional Modeling of an Ultra-Thin Body Single-Gate Si Tunnel-FET", ULIS 2014, Stockholm, Sweden, 2014
- M. Graef, T. Holtij, F. Hain, A. Kloes, B. Iñíguez, "2D Analytical Modeling of the Trap-Assisted-Tunneling Current in Double-Gate Tunnel-FETs", EuroSOI 2014, Tarragona, Spain, 2014

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- M. Graef, T. Holtij, F. Hain, A. Kloes, B. Iñíguez, "A Generic Analytical Current Model for Hetero-Junction Double-Gate Tunnel-FETs Including Two-Dimensional Effects", ISDRS 2013, Washington, USA, 2013
- M. Graef, T. Holtij, F. Hain, A. Kloes, B. Iñíguez, "Two-dimensional Physics-based Modeling of Electrostatics and Band-to-Band Tunneling in Tunnel-FETs", MIXDES 2013, Gdynia, Poland, 2013
- M. Graef, M. Schwarz, T. Holtij, F. Hain, A. Kloes, B. Iñíguez, "Two-dimensional Bias Dependent Model for the Screening Length in Double-Gate Tunnel-FETs", ULIS 2013, Warwick, UK, 2013
- M. Graef, M. Schwarz, T. Holtij, F. Hain, A. Kloes, B. Iñíguez, "Two-dimensional Analytical Model for Performance Evaluation of Double-Gate Tunnel-FETs", EuroSOI 2013, Paris, France, 2013

Co-Authorship

- A. Farokhnejad, M. Graef, F. Horst, C. Liu, Q.T. Zhao, B. Iñíguez, F. Lime and A. Kloes: Compact Modeling of Intrinsic Capacitances in Double-Gate Tunnel-FETs, EuroSOI/ULIS 2017, 2017.
- F. Horst, M. Graef, F. Hosenfeld, A. Farokhnejad, G. V. Luong, Q. T. Zhao, B. Iñíguez and A. Kloes: Static Noise Margin Analysis of 8T TFET SRAM Cells Using a 2D Compact Model Adapted to Measurement Data of Fabricated TFET Device, EuroSOI/ULIS 2017, 2017.
- F. Hosenfeld, F. Horst, M. Graef, A. Farokhnejad, A. Kloes, B. Iñíguez and F. Lime: Rapid NEGF-Based Calculation of Ballistic Current in Ultra-Short DG MOSFETs for Circuit Simulation, Microelectronics Journal, Vol. 7, No. 2, 2017
- F. Horst, M. Graef, F. Hosenfeld, A. Farokhnejad, F. Hain, G. V. Luong, Q. Zhao, B. Iñíguez, A. Kloes: Implementation of a DC Compact Model for Double-Gate Tunnel-FET Based on 2D Calculations and Application in Circuit Simulation, ESSDERC/ESSCIRC 2016, Lausanne, 2016.
- A. Kloes, F. Hain, M. Graef, B. Iñíguez: Closed-Form Charge-Based Current Model of Organic TFT Including Non-Linear Injection Effects, MOS-AK ESSDERC/ESSCIRC Workshop, Lausanne, 2016.
- A. Kloes, F. Hain, M. Graef, S. Jacob, B. Iñíguez: Charge-Based Current Model of Organic TFT for All Operation Regions with a Close Link to Electrical Device Parameters, Workshop on Flexible Electronics 2016, Tarragona, 2016.

- F. Hosenfeld, M. Graef, F. Horst, B. Iñíguez, Francois Lime, A. Kloes: Modeling Approach for Rapid NEGF-Based Simulation of Ballistic Current in Ultra-Short DG MOSFETs, MIXDES, Lodz, 2016.
- F. Hosenfeld, M. Graef, F. Horst, B. Iñíguez, Francois Lime, A. Kloes: Semi-Analytical Model for Leakage Current in Ultra-Short DG MOSFET Based on NEG Formalism, MOS-AK, Dresden, 2016.
- F. Hosenfeld, M. Graef, F. Hain, B. Iñíguez, F. Lime, A. Kloes: Dynamic Look-up Table for Increased Numerical Efficiency of Multi-Scale Simulation Approaches in Circuit Simulations, MOS-AK, Graz, 2015.
- A. Farokhnejad, M. Graef, A. Kloes: Wavelet-Based Calculation of the Transmission Coefficient for Tunneling Events in Tunnel-FETs, accepted for publication at MIXDES 2015.
- F. Hain, C. Lammers, M. Graef, A. Kloes, B. Iñíguez: Physics-based Model for the Threshold Voltage in Organic Field Effect Transistors Including Dynamic Trap Filling, ISFOE 2014, Thessaloniki, Greece, 2014.
- F. Hain, M. Graef, C. Lammers, A. Kloes, B. Iñíguez: Charge Based, Continous Current Model for Organic Field Effect Transistors, ICOE 2014, Modena, Italy, 2014.
- T. Holtij, M. Graef, A. Kloes, B. Iñíguez: 3-D Compact Model for Nanoscale Junctionless Triple-Gate Nanowire MOSFETs, accepted for presentation at ESSDERC/ESSCIRC 2014, Venice, Italy, 2014.
- T. Holtij, M. Graef, A. Kloes, B. Iñíguez: Modeling and Performance Study of Nanoscale Double Gate Junctionless and Inversion Mode MOSFETs Including Carrier Quantization Effects, accepted for publication in Microelectronics Journal, 2014.
- T. Holtij, M. Graef, F. Hain, A. Kloes, B. Iñíguez: Modeling of Quantization Effects in Nanoscale DG Junctionless MOSFETs, EuroSOI 2014, Tarragona, Spain, 2014.
- T. Holtij, M. Graef, F. Hain, A. Kloes, B. Iñíguez: Compact Model for Short-Channel Junctionless Accumulation Mode (JAM) Double Gate MOSFETs, IEEE Trans. Electron Devices, Vol. 61, No 2, 2014.
- F. Hain, M. Graef, T. Holtij, A. Kloes, B. Iñíguez: Metall - Investigation of the Influence of the Source/Drain Barrier Height on the I/V Characteristics of OFETs by Using a 2D Analytical Model for the Injection Current, ISDRS, Maryland, USA, 2013.
- A. Kloes, M. Graef, F. Hain, T. Holtij, M. Schwarz: COMON: SOI Multigate Devices Modeling, Spring MOS-AK/GSA Workshop, Munich, 2013.

- A. Kloes, M. Schwarz, T. Holtij, A. Navas: Quantum Confinement and Volume Inversion in MOS^3 Model for Short-Channel Tri-Gate MOSFETs, IEEE Trans. Electron Devices, Vol. 60, No. 8, 2013.
- F. Hain, M. Graef, M. Schwarz, T. Holtij, A. Kloes, B. Iñíguez: Metal - Organic Interfaces: Two-Dimensional Analytical Modeling of non-linear Charge Injection in Bottom-Contact Organic Field-Effect Transistors, SPIE Organic Photonics + Electronics Conferences, San Diego, USA, 2013.
- F. Hain, M. Graef, T. Holtij, A. Kloes, B. Iñíguez: Analytical Model for the Potential in Bottom Contact OFETs and Approach for Calculation of the Tunneling/Thermionic Source/Drain Injection Current, ICOE 2013, Grenoble, France, 2013.
- F. Hain, M. Graef, M. Schwarz, T. Holtij, A. Kloes, B. Iñíguez: Two-Dimensional Analytical Modeling of non-linear Charge Injection in Bottom-Contact Organic Field-Effect Transistors, LOPE-C 2013, Munich, Germany, 2013.
- T. Holtij, M. Schwarz, M. Graef, F. Hain, A. Kloes, B. Iñíguez: Unified Charge Model for Short-Channel Junctionless Double Gate MOSFETs, MIXDES 2013, Gdynia, Poland, 2013.
- T. Holtij, M. Schwarz, M. Graef, F. Hain, A. Kloes, B. Iñíguez: Model for investigation of Ion/Ioff ratios in short-channel junctionless double gate MOSFETs, ULIS 2013, Warwick, UK, 2013.
- T. Holtij, M. Schwarz, M. Graef, F. Hain, A. Kloes, B. Iñíguez: 2D Current Model for Junctionless DG MOSFETs, EuroSOI 2013, Paris, France, 2013.

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List of Symbols

Symbol	Description	Unit
$\Delta\Phi_d$	parabolic boundary condition drain	[V]
$\Delta\Phi_s$	parabolic boundary condition source	[V]
ΔE	energy difference	[eV]
ΔE_g^0	band-gap reduction	[eV]
$\Delta x, \Delta y$	rdf meshgrid parameter	[nm]
α	angle	[deg]
β	slope degradation factor	[-]
λ	screening length	[nm]
λ_{fit}	screening length fitting factor	[-]
λ_d	drain screening length	[nm]
λ_s	source screening length	[nm]
μ	mobility	[cm^2/Vs]
μ_{tun}^n	electron tunneling mobility	[cm^2/Vs]
μ_{tun}^p	hole tunneling mobility	[cm^2/Vs]
μ_n	electron mobility	[cm^2/Vs]
μ_p	hole mobility	[cm^2/Vs]
Φ	potential	[V]
Φ_0	boundary condition	[V]
Φ_{bi}^d	built-in potential drain	[V]
Φ_{bi}^s	built-in potential source	[V]
Φ_{const}	constant boundary condition	[V]
Φ_g	gate boundary condition	[V]
Φ_{lin}	linear boundary condition	[V]
Φ_s	source boundary condition	[V]
Φ_v	volume boundary	[V]
Ψ	wave function	[-]
Ψ^-	reflected wave	[-]
Ψ^+	incoming/transmitted wave	[-]

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ρ	charge density	[As/cm^3]
$\sigma(r)$	radius depending surface charge	[As/cm^2]
σ	doping profile standard deviation	[nm]
σ_E	electric field standard deviation	[V/cm]
σ_{I_d}	drain current standard deviation	[A]
σ_N	dopant standard deviation	[-]
σ_Q	gate charge standard deviation	[As]
σ_{V_g}	gate voltage standard deviation	[V]
ϵ	relative permittivity	[-]
ϵ_0	permittivity	[As/Vcm]
ϵ_{ch}	permittivity channel	[As/Vcm]
ϵ_d	permittivity drain	[As/Vcm]
ϵ_{in}	permittivity insulator	[As/Vcm]
ϵ_s	permittivity source	[As/Vcm]
φ	potential	[V]
$\varphi_{ideal}, \tilde{\varphi}$	potential for ideal and non-ideal doping profile	[V]
φ_{const}	potential solution for constant boundary	[V]
φ_d	drain potential solution	[V]
φ_d^x	drain potential solution in x-direction	[V]
φ_j^d	drain junction potential	[V]
φ_j^s	source junction potential	[V]
φ_{lin}	potential solution for linear boundary	[V]
φ_n	doping profile potential difference drain	[V]
φ_p	doping profile potential difference source	[V]
φ_{para}	potential solution for parabolic boundary	[V]
φ_s	source potential solution	[V]
φ_s^x	source potential solution in x-direction	[V]
φ_{sp}	long channel surface potential	[V]
a, b	constants for square root approxmation	[-]
a, b	constants for doping profile adjustment	[-]
a, b	positions for tunneling length calculation	[-]
A, B, C, D, E, F	wave function constants	[-]
A^*	Richardson constant	[A/cm^2K^2]
C, E	conformal mapping constants	[-]
c_{bar}	constant for minimum barrier height	[-]
C_{in}	insulator capacitance	[As/V]
D	Domain	[-]
D*	Mapped Domain	[-]
D	dielectric flux	[As/cm^2]

D_{in}	dielectric displacement at insulator	[As/cm^2]
$d\varphi$	potential difference	[V]
d_d	potential bending distance drain	[nm]
d_s	potential bending distance source	[nm]
E	energy	[eV]
e	carrier emission rate	[s^{-1}]
$\overrightarrow{E}$	electric field	[V/cm]
E_A	Fermi-level for p-type doping	[eV]
E_c	conduction band energy	[eV]
E_{car}	carrier energy for tunneling	[eV]
E_D	Fermi-level for n-type doping	[eV]
E_d	degeneration in drain	[eV]
E_F	Fermi level	[eV]
E_{Fi}	intrinsic Fermi level	[eV]
E_g	band-gap	[eV]
E_g^0	intrinsic band-gap	[eV]
E_p	doping profile electric field	[V/cm]
E_s	degeneration in source	[eV]
E_v	valence band energy	[eV]
E_{vac}	vacuum energy level	[eV]
f	Fermi-Dirac distribution function	[-]
F	compley function	[-]
$\widetilde{F}$	complex potential in w-plane	[V]
f_d	drain-related Fermi statistic	[-]
f_s	source-related Fermi statistic	[-]
$h, \hbar$	Planck constant	[eVs]
h_{bar}	tunneling barrier height	[eV]
I	device current	[A]
I_{amb}^{b2b}	b2b current in ambipolar-state	[A]
I_{dAvr}	average device current	[A]
I_{on}^{b2b}	b2b current in on-state	[A]
I_{tat}^{amb}	tat current at drain/channel junction	[A]
I_{tat}^{on}	tat current at source/channel junction	[A]
J_{tat}	tat current density	[A/cm^{-3}]
k	wave vector	[-]
k	Boltzmann constant	[eV/K]
l_{b2b}^{amb}	b2b tunneling length for ambipolar-state	[nm]
l_{b2b}^{on}	b2b tunneling length for on-state	[nm]
l_{ch}	channel length	[nm]

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l_{sd}	source/drain length	[nm]
l_{tun}	tunneling length	[nm]
m	effective carrier mass	[kg]
m_0	rest mass	[kg]
M_C	conduction band minima	[-]
m_e	effective electron mass	[kg]
m_h	effective hole mass	[kg]
N	doping concentration	[cm^{-3}]
n	electron concentration	[cm^{-3}]
n	constant for trap distribution	[-]
N_A	acceptor doping concentration	[cm^{-3}]
N_C	density of states at conduction band	[cm^{-3}]
N_{ch}	channel doping concentration	[cm^{-3}]
N_{count}	number of dopants	[cm^{-1}]
N_d	drain-sided doping profile	[cm^{-3}]
N_D	donor doping concentration	[cm^{-3}]
N_d^0	drain doping concentration	[cm^{-3}]
n_i	intrinsic carrier concentration	[cm^{-3}]
N_{ideal}	ideal doping profile	[cm^{-3}]
N_{lin}	linear doping profile	[cm^{-3}]
N_p	source delta doping	[cm^{-3}]
N_{peak}	peak doping concentration	[cm^{-3}]
N_s	source-sided doping profile	[cm^{-3}]
N_s^0	source doping concentration	[cm^{-3}]
N_{Sano}	discrete doping profile	[cm^{-3}]
N_T	trap distribution	[$eV^{-1}cm^{-2}$]
N_{Tc}	trapped carrier density	[$eV^{-1}cm^{-2}$]
N_{Tmax}	maximum trap concentration	[$eV^{-1}cm^{-2}$]
N_V	density of states at valence band	[cm^{-3}]
p	hole concentration	[cm^{-3}]
q	elemetary charge	[As]
Q_{fit}	charge fitting factor	[-]
r	radius	[nm]
r_0	rdf cell vector	[-]
S	subthreshold slope	[mV/dec]
S_{avr}	average subthreshold slope	[mV/dec]
T	temperature	[K]
T	tunneling probability	[-]
t	tunneling barrier thickness	[nm]

$t(w)$	transformation function	[-]
$t^{-1}(z)$	inverse transformation function	[-]
T_{b2b}	band-to-band tunneling probability	[-]
t_{ch}	channel thickness	[nm]
t_{dev}	device thickness	[nm]
t_{in}	insulator thickness	[nm]
$\tilde{t}_{in}$	effective insulator thickness	[nm]
T_{tat}	tat probability	[-]
U	tunneling barrier energy	[eV]
u, v	w-plane coordinates	[-]
U_0	constant tunneling barrier height	[eV]
V	voltage	[V]
V	volume	[cm^3]
V_d	drain voltage	[V]
V_{fb}	flat-band voltage	[V]
V_g	gate voltage	[V]
V_{in}	insulator voltage drop	[V]
V_s	source voltage	[V]
V_{th}	threshold voltage	[V]
w	width	[nm]
w	complex variable for w-plane	[-]
x	x-coordinate	[nm]
X	electron affinity	[eV]
x, y	z-plane coordinates	[-]
x_{int}	b2b overlap position	[nm]
x_m	potential barrier position	[nm]
x_{peak}	peak position	[nm]
x_{shift}	doping diffusion potential shift	[nm]
y	y-coordinate	[nm]
z	complex variable for z-plane	[-]

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Acronyms

Symbol	**Description**
1D	One Dimensional
2D	Two Dimensional
3D	Three Dimensional
B2B	band-to-band
BGN	Band-Gap Narrowing
CMOS	Complementary Metal Oxide Semiconductor
DG	Double-Gate
FEM	Finite Elemente Method
FN	Fowler-Nordheim
HS	Hetero-Structure
IFM	Impedance Field Method
ITRS	International Technology Roadmap for Semiconductors
MOSFET	Metal Oxide Semiconductor Field Effect Transistor
RDF	Random Dopant Fluctuation
SCE	Short Channel Effect
SPICE	Software Process Improvement and Capability dEtermination
TAT	Trap-Assisted-Tunneling
TCAD	Technology Computer-Aided Design
TFET	Tunneling Field Effect Transistor
WKB	Wentzel-Kramers-Brillouin

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CHAPTER 1

Introduction

The development and technological improvement of all different kinds of electronic devices in the 20th century is, without a doubt, extraordinary. One mayor aspect of this rapid enhancement belays in the discovery of the semiconductor and the following inventions based on these semiconducting materials. They lead from a mechanically operating society in the early 1900th to a highly versatile technically based society today. Electronic devices are in such a way integrated in our everyday live, that a day without them almost seems impossible. In this world of logic and numbers, voltage and currents, protons and electrons, this work is fitting.

1.1 The Rising of Semicondutor Devices

First over it all a brief passage in semiconductor device history is not only necessary but astonishing. In this section the timeline of the rising of semiconductor devices is shown with all important discoveries and inventions.

It all started with the discovery of semiconducting materials. According to Busch [1] the phrase "semiconductor" was firstly mentioned in a letter from Alessandro Volta in 1782. He observed that the speed with which an electrometer is discharged by touching its knob with different materials varies. Metals did it instantaneously, semiconductors slowly and insulators not at all. A more scientific experiment to capture the semiconducting effect was done by Michael Faraday [2] in 1833. He was interested in the influence of the temperature on the conductivity of different materials. One material of particular interest and surprising behavior was a "sulphuret of silver" like Ag_2S. It showed a very low conductivity at room temperature, but at 175 °C an abrupt rise in conductivity occurred to nearly metallic magnitude.
The first time the term "semiconductor" was published in today's sense of the word was in 1910 by Weiss [3]. In his work he measured the thermoelectric power, Thomson heat and Peltier coefficient of various combinations of different materials with oxides and sulfides of iron and titanium. During that time the poor reproducibility of results is the main reason for the bad

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reputation semiconductor research suffered for the upcoming years [1].
In 1931 Wilson published his famous papers on semiconductors [4] and distinguished between "intrinsic" and "extrinsic" semiconductors and mentioned the presence of donors and acceptors. It was also him, who introduced the band theory of solids, which explains the difference between metals and insulators based on the idea of filled and empty energy bands. His contributions dominate solid state physics up to date.

It was years later in 1940 when Russel Ohl accidentally created the first p-n junction [5]. During his work on radio wave detectors, he realized that the problems with the cat's whisker detectors belay in the bad quality of the semiconductor. So he remelted the silicon in quartz tubes and cooled it down. The result was still polycrystalline but the properties were much more uniform. Based on that improvement, he identified the impurities, which lead to the p-n junction, the basic principle of so many following inventions.
In 1945 a concept of a semiconductor amplifier based on the field-effect principle was firstly introduced by William Shockley [6]. His basic idea was to change the conductance of a semiconducting layer by only applying a transverse electric field. At this point the effect could not be reproduced experimentally due to surface states. However, based on these creative failures Shockley's colleagues Bardeen and Brattain were able to discover the point-contact transistor in 1947 [6]. These were the first transistors to be produced but they were extremely unstable and their electrical characteristics were hard to control. This unpredictable behavior strongly depends on the purity of the sample.
With the junction transistor, a much more reliable device was introduced by Shockley in 1951 [6]. This device is later known as the n-p-n bipolar transistor. One year later the first devices were produced. The fabrication, however, was much more difficult compared to the point-contact transistor. Due to the complicated doping procedure, the crystal consisted of three layers forming the n-p-n regions. These layers had to be cut and contacts had to be added to get the actual devices. The first silicon devices with grown junctions were manufactured by Gordon Teal in 1954.

Due to the achieved reliability, speed and heat reduction it was imaginable to build large systems with the bipolar transistor. To minimize delays between the single devices caused by the interconnects the distance had to be kept very short. Based on this dilemma the first integrated circuit for an oscillator was fabricated by Kilby in 1958 [7]. In this first circuit the single devices were still connected via bonding. One year later the first modern diffused transistor was announced by Hoerni [7]. It combined the photolithographic techniques and a compatible set of diffusion processes previously developed by Noyce and Moore to produce dished junctions extending to the surface. The surface and contacts were protected with an oxide passivation, which also assured more consistency and reproducibility in comparison to the prior techniques. This was the beginning of the "planar" process [7].

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In 1957 the first concept for the tunneling diode was presented by Esaki [8]. He was experimenting with heavily doped junctions in order to find out how high the bipolar transistor base could be doped before the injection at the emitter junction became inadequate. He was aware of the backward Zener tunneling at p-n junctions and could adjust the breakdown voltage in dependency of the applied doping concentration. The device is highly resistant to environmental conditions since the current transport is not depending on minority carriers or thermal effects. With that the first device utilizing the tunneling effect was created.

The most important device which now dominates the 21st century was firstly introduced 20 years before the invention of the bipolar transistor by Julius Lilienfeld in 1930 (MESFET) and following in 1933: the metal-oxide-semiconductor field-effect transistor (MOSFET) [9, 10]. It took almost 30 years to realize the idea and so it was in 1959 when a group lead by Atalla at Bell Labs used thermal oxidation to achieve a silicon dioxide layer to stabilize the silicon surface [11]. In 1960 this technology lead to the first fabrication of a MOSFET [12].

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1.2 MOSFET Technological Improvement

In this section the technological improvement of the MOSFET is shown chronologically. It is important to know the state-of-the-art technological possibilities for fabricating MOSFET devices, since all possible upcoming technologies or devices do not only profit, but also have to be based on them. A complete technological change in terms of fabricating semiconducting devices is highly unlikely (costly) due to the size and complexity of the established semiconductor industry.

The first MOSFET mentioned in a patent, shown in figure 1.1 was designed by Dawon [13] in 1963. The general structure could be fabricated using the standard planar process [14]. Based on this structural design, the MOSFET was industrially fabricated for almost 50 years. One of the leading companies, which is focused on MOSFET based processor technology right from the beginning is the Intel® Corporation founded in 1968. Therefore, the following shown MOSFET technology optimization will be orientating on the Intel® product line.

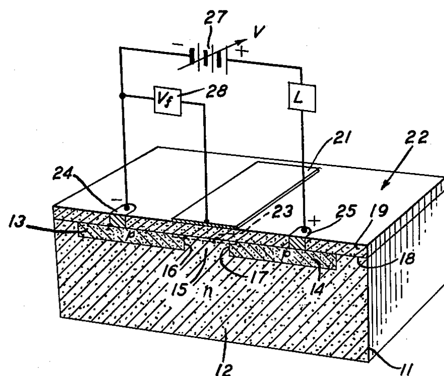

Figure 1.1: Geometric structure of the first MOSFET from its patent [13].

From 1963 till 2003 the main focus of MOSFET technology optimization lay on device scaling [14]. Reducing the device's geometrical structure in size has versatile advantages in switching speed, energy consumption and packing density. This scaling process was firstly captured by Gordon Moore in 1964, who foretold that the number of transistors on a single chip will double every year [15]. This prediction later became Moore's law and somewhat a self-fulfilling prediction since the future processor development was orientating on it. In 1975 Moore corrected his prediction and slowed the future rate of increase in complexity to a doubling every two years [16]. This rate could be held till 2012 where signs of a saturation occurred.

The scaling could not only be continued by simply shrinking the device's geometric structure. One of the last technology only based on scaling was the 70 nm node in 2001 [17] (see fig. 1.2 (a)). At this point the scaling continued using new methods and technologies. To gain switching

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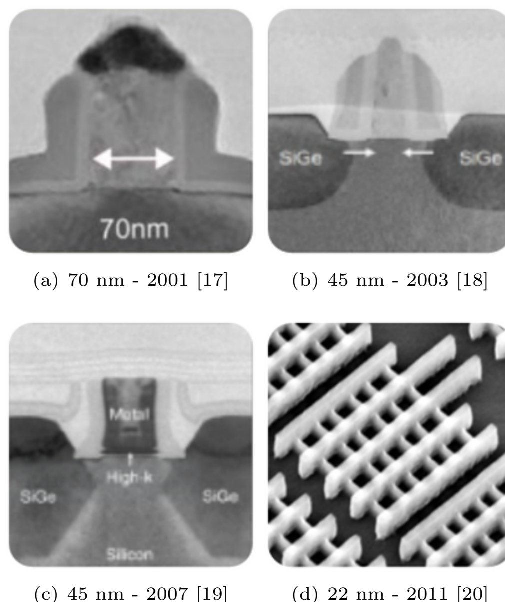
speed an increase in carrier mobility was achieved by firstly using strained silicon technology in the 45 nm node in 2003 [18] (see fig. 1.2 (b)). A further increase in switching speed could be realized by using a high-κ insulator and a metal gate in addition to the strained silicon technology in the 45 nm node in 2007 [19] (see fig. 1.2 (c)). Finally, in 2011 a revolutionary step in the industrial processor development was done by introducing the first processor using 22 nm tri-gated MOSFETs [20] (see fig. 1.2 (d)).



(a) 70 nm - 2001 [17] (b) 45 nm - 2003 [18]

(c) 45 nm - 2007 [19] (d) 22 nm - 2011 [20]

Figure 1.2: Intel® MOSFET technology development (a) 70 nm standard MOSFET 2001 (b) 45 nm strained silicon technology 2003 (c) 45 nm high-κ metal-gate technology 2007 (d) 22 nm tri-gate technology 2011.

Now the state-of-the-art transistor structure is the 2nd generation of the FinFET structure with the 14 nm logic technology, shown in fig. 1.3 [21]. In order to look beyond this point the international technology roadmap for semiconductors (ITRS) tries to predict the course of future technologies and guides the industry and research community to reach these goals. It is written by an international group of semiconductor industry experts. Regarding the future of scaling, the ITRS 2015 says: "*The combination of 3D device architecture and low power device will usher the (Third) Era of Scaling, identified in short as "3D Power Scaling". Increase in the number of transistors per unit area will eventually be accomplished by stacking multiple layers of transistors... In the next decade ITRS 2.0 predicts that the advent of the third phase of scaling "3D Power Scaling" will become the driver of the rejuvenated semiconductor industry*" [22]. Also, a significant part of the research for further improvement in device performance is concentrated on semiconducting materials from the third and fifth group of the periodic ta-

ble (III-V materials) and germanium, due to their higher mobilities in comparison to silicon [22].

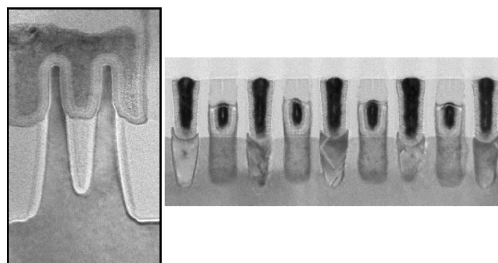


Figure 1.3: Most recent 14 nm FinFET structure [21]. Fin and gate-cut images.

Challenging aspects for the complementary-MOS (CMOS) technology are low power applications at 0.5 V to 0.4 V. Due to the thermionic-emission based current transport mechanism in these devices their minimum subthreshold slope (S) is physically limited to 60 mV/dec at room temperature [23]. Reducing the supply voltage with a constant slope leads to an increase in leakage current of the MOSFET and a worsening of the on/off ratio (see fig. 1.4). So called "steep slope devices" fill the gap and are able to provide a low leakage current while maintaining a sufficient on-current.

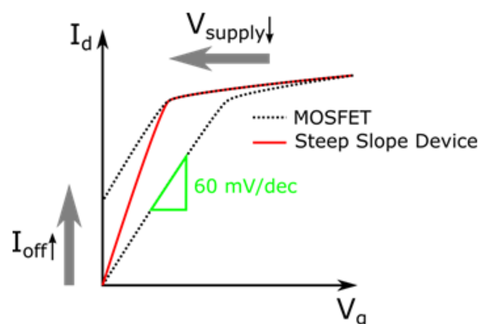


Figure 1.4: Increase in leakage current caused by supply voltage reduction and constant subthreshold slope in MOSFETs. Introduction of steep slope devices.

The focus of this work belays on one of the most promising devices to continuously overcome the 60 mv/dec slope limitation of MOSFETs, and with that, be its successor for at least low power applications. Based on its band-to-band (b2b) tunneling current transport mechanism in the on-state, the tunneling field-effect transistor (TFET) provides this possibility [24–26].

1.3 Tunnel-FET Development

With the invention of the tunneling diode in 1976 the mechanism of band-to-band tunneling was firstly commercialized [8]. Years later the same effect could be used to fabricate a gated p-i-n tunneling diode to be used as a transistor: the TFET. In 2004 the first transistor with a subthreshold slope of 40 mV/dec was fabricated by Appenzeller using a carbon nanotube channel [27]. Inspired by this achievement several groups started working with TFETs as well (CEA-Leti, IMEC, UC Berkeley, Stanford). They soon published positive results (slopes below 60 mV/dec) using widely used semiconducting materials like silicon and germanium [24]. One of the mayor benefits and also requirements is the similarity of TFETs to the MOSFET in terms of its basic configuration with source, drain, gate, insulator and it shows a similar electrical behavior as well. With the ability to provide full CMOS compatibility the TFET has the necessary set of abilities to be the successor of the MOSFET.

The biggest challenge so far with these new devices is the trade-off between a steep subthreshold slope and a sufficient on-current. The praised tunneling effect, which enables these steep slopes has a weak spot in indirect band-gap semiconductor materials like silicon and germanium. Here, in addition to direct transient from one band to another, the electrons have to absorb some extra energy from vibrations in the materials crystal lattice. This detour significantly lowers the tunneling probability of the carriers, which reflects badly on the achievable on current in comparison to MOSFET devices. The logic consequence of this dilemma is the introduction of direct band-gap materials for TFETs, like III-V semiconductors. The first III-V TFET was introduced by Datta in 2009, showing a significant increase in on-current in that time [28]. Nowadays the full potential of technological possibilities is used for fabricating TFETs: From conventional to III-V semiconductors, hetero-structures, straining techniques, high-κ gate insulators and a wide range of different 2D and 3D structures are investigated. So far a specific selection regarding material combination and structure has not been made, although the greatest potential show 3D structures using III-V semiconductors and high-κ gate dielectrics [24–26]. In 2011 Dewey published a III-V TFET using InGaAs hetero-junctions with high on-current and a subthreshold slope below 60 mV/dec [29]. In 2013 Knoll published results of a complementary TFET inverter using strained silicon nanowire TFETs [30]. The devices showed a minimum subthreshold slope of 30 mV/dec and high on-currents of >10 μA/μm at V_{ds}=0.5 V. In 2015 Sarkar has shown the first TFET with subthermal swing in a 2D channel. The device consisted of a p-Ge source, MoS_2 channel and an electrolytic polymer gate ($PEO:LiClO_4$) [31]. An extremely low subthreshold slope is achieved (<10 mV/dec).

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1.4 Modeling and Simulation Needs

Today's microprocessor transistor count per single chip is already above 1.000.000.000. This number is so incomprehensibly large, that it is impossible to capture a circuit build from so many transistors with the human brain. In spite of that, the commercially available transistors seem to be working without any problems at all. In order to understand the development process of such processors, this section gives a brief introduction in circuit simulation and device modeling.

The requirements for circuit simulators differ from the application area. There are different kinds of simulators depending on the simulation level. Figure 1.5 shows the different simulation levels with a simulation example. On top is the system level which simulates digital circuits containing logic blocks. The next level is the circuit level for analog circuit simulations like a static random-access memory (SRAM) cell or an oscillator. These circuits contain several transistors, which are simulated using device simulators in the device level. In order to fabricate these devices process simulators are used in the lower process level. The most mathematically complex simulations are quantum simulations, which contain only several atoms.

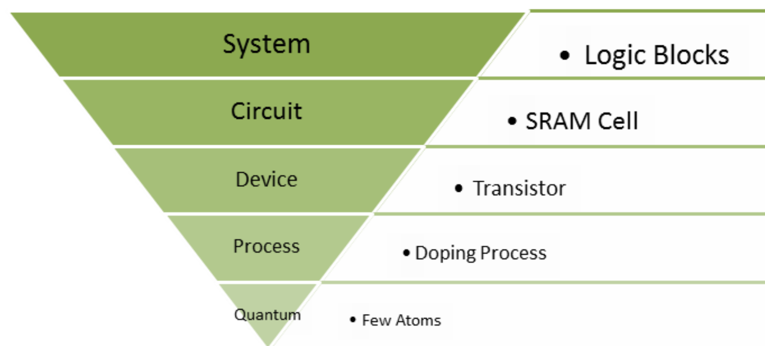


Figure 1.5: Simulation levels with application example.

Between these simulation levels, versatile abstractions are made in order to simplify the computational complexity. On system level only logic states between blocks are calculated (0 and 1). The transition between circuit simulator and system level is the coupling of an analog voltage to a logic state (e.g. 5 V = 1). The circuit level uses compact models for different devices to calculate the circuit output. These compact models are mathematical equations which describe the electrical behavior of a single device depending on the applied voltages and currents. The transition between circuit and device level is a compact model. The developer uses the gained knowledge from single device simulations on device level to find simple mathematical equations, describing the observed effects. On device level single transistor simulations are done using the finite elemente method (FEM). This method is a valued versatile numerical approach to

simulate electrical, physical, optical and many other operations in diverse devices. In the context of this work it is used to calculate the output and transfer characteristics of a TFET including all necessary physical effects occurring in these devices.

Since the TFET is gaining interest in the research community and first inverters are fabricated [30], the need for accurate compact models to be implemented in circuit simulators is clearly visible. There are different possibilities for modeling such devices. The model's complexity correlates to the desired accuracy, whereas one-dimensional models are easy to calculate, they often lack accuracy regarding device variability. The next step is to include two-dimensional effects, making the model more variable and accurate for short-channel effects (SCE). The most complex models also include three-dimensional influences making them applicable for 3D devices such as short-channel FinFETs.
Not only the complexity varies between the compact models but also the general approach to solve the device current. Some models are based on an electrostatics solution (like this work) and others use a charge-based approach. So far first model approaches have been published. In 2010 Bardon published a pseudo-two-dimensional analytical model for double-gate (DG) TFETs [32]. The potential, electric field and tunneling generation rate are calculated analytically with a numerically extraction of the tunneling current. The potential solution includes the depletion regions inside source and drain. Due to the numerically calculated current this model is unfit to adapt in a circuit simulator. In 2014 Zhang published a 1D compact model implemented in SPICE [33]. The potential solution also includes the depletion regions in source and drain region and provides accurate results. However, two dimensional short-channel effects are not captured. In 2015 Biswas introduced a DG TFET compact model for Verlog-A implementation [34]. This approach is also 1D and does not include the influence of the depletion regions in source and drain, making it not adaptable for hetero-junction devices.

In this thesis an extensive two-dimensional, physics-based, analytical model for the overall device current in double-gate n-TFETs is introduced. The model is based on 2D compact solutions for the device potential and electric field, including different material combinations. Potential adjustments have been included to consider doping profiles at the channel junctions. The band-to-band and trap-assisted-tunneling probability are calculated separately using a quasi two-dimensional Wentzel-Kramers-Brillouin (WKB) approximation. By applying Landauer's transmission theory, the tunneling current is calculated. The model can be used for short-channel hetero-junction TFET simulations, including all important physical effects occurring within the TFET.

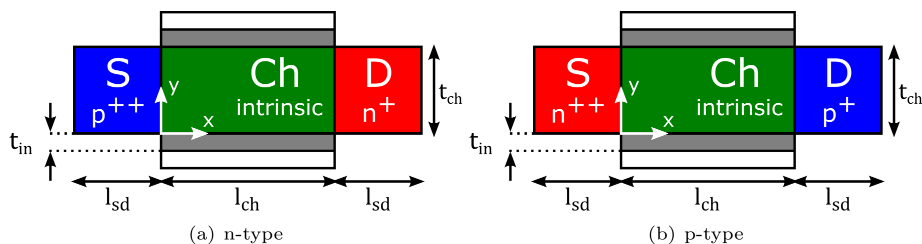
CHAPTER 2

Device Physics

In this chapter all basic physical effects occurring within the TFET are explained. Beginning in section 2.1, the geometry of the device, including all important parameters, is shown. Because of the highly doped regions within the TFET, the influence of high doping on semiconductor materials and the consequences in band-structure, as well as different material combinations are shown in section 2.2. How to calculate accurate carrier concentrations within the highly doped regions is explained in section 2.2.5. Since the current transport mechanism in TFETs is the tunnel effect, this effect is generally introduced and explained in section 2.3. The step from a general description to the occurring tunneling events within the TFET is carried out in section 2.4. In order to understand the electric behavior of the TFET, the device working principle is investigated in section 2.5.

2.1 Tunnel-FET Geometry

In this section the investigated TFET geometry is introduced. As mentioned before in chapter 1, the ongoing TFET research is highly versatile and dynamic regarding the device geometry, since no optimum has been found so far. However, the general trend seems to be heading towards multiple gate 3D devices. Keeping this dynamic development in mind, a device geometry for the model derivation has to be, on one hand, adaptable to different geometries and on the other hand kept plane to simplify the calculations. For this work the DG structure in figure 2.1 is chosen. It is more complex than the basic single-gate bulk device and it can be adapted to cover even Fin-structures, making it a perfect compromise between geometric complexity and mathematical simplicity. Figure 2.1 (a) shows the modeled silicon n-type DG TFET. Source and drain region have a length of l_{sd}, the channel region length is l_{ch} and their thickness is t_{ch}. The high-κ insulator consists of HfO_2 and has a thickness of t_{in}. The width of the device is defined as w.



(a) n-type (b) p-type

Figure 2.1: Schematic geometry of an (a) n-type ((b) p-type) DG Tunnel-FET, showing its structural parameters and doping profiles.

The TFET is basically a gated p-i-n diode. An electron on-state current occurs for an n-type device (figure 2.1 (a)). For a p-type device (figure 2.1 (b)) the on-state current is hole-carrier based. For the n-type device, the source is highly p-doped, the channel stays intrinsic and the drain has a reduced n-doping. In the p-type device the doping types for source and drain are switched.

The most simplest homo-junction devices only contain silicon as semiconductor material in source, channel and drain region. This setup is also used for the model derivation in chapter 4. However, the possibilities of different material combinations to create hetero-junction TFETs are versatile [26]. These alternative materials, mostly III-V semiconductors, provide high carrier mobilities and small direct band-gaps, which enhance the tunnel effect, and with that, device performance.

Not only the semiconductor material is important for device performance. The gate insulator material has a major influence as well. Thereby, the permittivity of the insulator ϵ_{in} directly correlates to its ability to improve the electrostatic influence of the gate electrode on the channel region. The usage of high-κ gate insulators, like HfO_2, serves as a common tool for performance enhancement.

2.2 Band-Structure

The band-structure of semiconductor devices enables a deep insight into their physical behavior and working principles. It also is the basis of many different calculations like carrier concentrations and tunneling probabilities. Because of these possibilities it is important to understand the band-structure calculation and learn to interpret it. The main influences are the applied biases, device geometry, used materials and doping types/concentrations.

2.2.1 Energy Bands and Band-Gap

In the first step the derivation of the simplified band-structure from its complex energy-band-structures is explained. Two materials are considered, one with a direct band-gap: GaAs

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and one with an indirect band-gap: silicon. Figure 2.2 shows the energy-band-structures of (a) silicon and (b) GaAs in dependency of the wave vector k. In semiconductors the upper bands (conduction bands) are energetically separated from the lower bands (valence bands), the resulting space between them is the band-gap. Electrons are able to move freely in the conduction band (minus signs in fig. 2.2) and holes in the valence band (plus signs in fig. 2.2). The curvature of the bands indicates the carrier mass. The higher the curvature, the lower the mass [35]. For silicon the valence-band maximum E_v occurs at Γ and the conduction band minimum E_c is misaligned in k-space, therefore indicating an indirect band-gap with

$$E_g^0 = E_c - E_v. \tag{2.1}$$

In GaAs the band-edges are aligned and indicate a direct band-gap material. In the following plots of the device band-structure, only the band-edges E_c and E_v are shown.

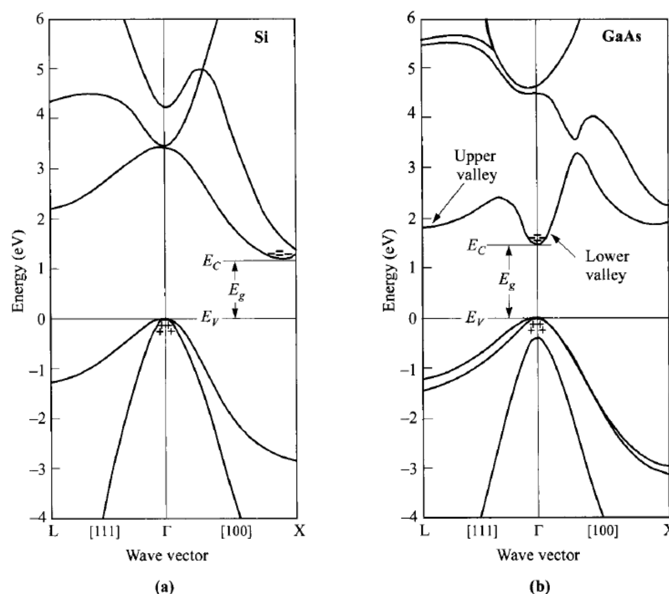

Figure 2.2: Energy-band-structures of (a) silicon and (b) GaAs. E_g is the band-gap, plus signs (+) indicate holes in the valence band, minus signs (-) indicate electrons in the conduction band [35].

2.2.2 Carrier Concentration and Fermi Level

One of the most important properties of a semiconductor is the possibility to vary its resistivity through doping with different types and concentrations of impurities. Figure 2.3 shows the three basic bonding types: (a) the intrinsic state without any impurities, (b) n-type Si using phosphor as doping material adding a free electron to the lattice and a fixed positive charged

P-Ion, (c) p-type Si using boron as doping material adding a free hole to the lattice and a fixed negative charged B-Ion. These ionized impurities often lead to a depletion of carriers and leave behind a charge density that can result in an electric field and sometimes a potential barrier inside the semiconductor [35].

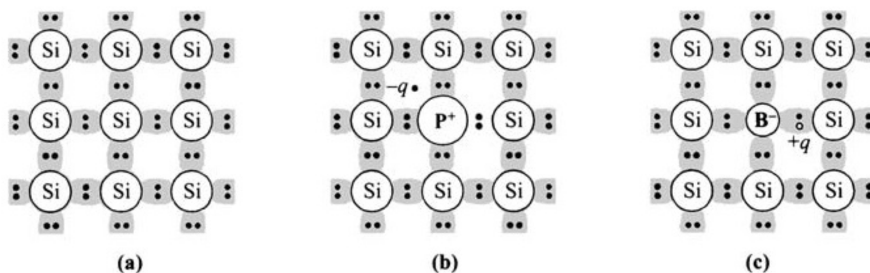

Figure 2.3: Three basic bond illustrations of silicon. (a) Intrinsic Si without impurities, (b) n-type Si with donor (phosphor) and (c) p-type Si with acceptor (boron) [35].

The effective density of states at the conduction band N_C and valence band N_V describe the maximum number of carriers, that can occupy the bands in the intrinsic state of the semiconductor. For silicon the values are given through [35]:

$$N_C = 2 \cdot \left(\frac{2\pi m_e kT}{h^2} \right)^{\frac{3}{2}} M_C, \tag{2.2}$$

$$N_V = 2 \cdot \left(\frac{2\pi m_h kT}{h^2} \right)^{\frac{3}{2}}. \tag{2.3}$$

with the number of equivalent conduction band minima M_C, the effective electron mass m_e, effective hole mass m_h, Boltzmann constant k, temperature T and the Planck constant h. The Fermi level E_F describes the energy level, where charge neutrality is given. For an intrinsic (undoped) semiconductor the Fermi level is often described with E_{Fi}. This description is also used to indicate the intrisic Fermi level of an already doped semiconductor. With it the band-structure from a given potential distribution can be evaluated. The Fermi level is the basis for calculating the carrier occupancy probability, which is represented by the Fermi-Dirac distribution function f [35]:

$$f(E) = \frac{1}{1 + \exp[(E - E_F)/kT]}. \tag{2.4}$$

By using the effective density of states and the Fermi level, the carriers at the conduction and valence band can be estimated using Boltzmann statistics. For the electron concentration in the conduction band n stands [35]

$$n = N_C \cdot \exp\left(-\frac{E_c - E_F}{kT}\right) \text{ or } E_c - E_F = kT \cdot \ln\left(\frac{N_C}{n}\right) \tag{2.5}$$

and for the hole concentration in the valence band p

$$p = N_V \cdot \exp\left(-\frac{E_F - E_v}{kT}\right) \text{ or } E_F - E_v = kT \cdot \ln\left(\frac{N_V}{p}\right). \tag{2.6}$$

For semiconductors at room temperature electrons are continuously excited to the conduction band through thermal agitation, leading to an intrinsic carrier concentration n_i for each semiconducting material. For each electron in the conduction band a hole is created in the valence band, therefore stands $n = p = n_i$ at steady state. The Fermi level for an intrinsic semiconductor E_{Fi} can be calculated with the help of the effective density of states [35]:

$$E_{Fi} = \frac{E_c + E_v}{2} + \frac{kT}{2} \cdot \ln\left(\frac{N_V}{N_C}\right). \tag{2.7}$$

Therefore, the intrinsic Fermi level almost lies in the middle of the semiconductor band-gap. The intrinsic carrier concentration can be calculated with [35]

$$n_i^2 = n \cdot p = N_C \cdot N_V \cdot \exp\left(-\frac{E_g}{kT}\right). \tag{2.8}$$

By applying an outer (positive) bias to the semiconductor the Fermi level is shifted (downwards) in energy scale. If in the intrinsic state stands $E_F = 0\ eV$, then an applied bias V shifts the Fermi-level to

$$E_F(V) = -q \cdot V, \tag{2.9}$$

with the elementary charge q.

2.2.3 Doping Influence

In this section the influence of impurity types and concentrations on the band-structure are calculated. The n-type donor doping concentration is described with N_D and the p-type acceptor doping concentration with N_A. The general calculations are simplified due to the assumption, that only one doping type per region is applied and the doping concentration is much higher than the intrinsic carrier concentration ($N_{D/A} \gg n_i$). Figure 2.4 illustrates the effects of different impurity doping types on the band-structure, whereby in fig. 2.4 (a) the intrinsic state is shown. The amount of carriers in conduction and valence band in equilibrium is ($n = p = n_i$) and the Fermi-level is located in the middle of the band-gap.
By doping a donor impurity concentration N_D, additional states within the band-gap of the semiconductor near the conduction band are created in figure 2.4 (b). The additional electrons in the conduction band cause a shift of the Fermi-level towards a higher energy level. Vise versa, the hole concentration in the valence band is reduced. E_D stands for the energy of the Fermi-level for n-type doping. The energy difference of the conduction band and the Fermi-level ($E_c - E_F$) can be calculated by using the Boltzmann statistics from equation (2.5) with $n \approx N_D$ for low doping concentrations.
For a doped p-type impurity concentration N_A the Fermi-level is shifted towards a lower energy level and increases the hole concentration within the valence band, shown in figure 2.4 c). E_A is the energy of the Fermi-level for p-type doping. For this doping type the energy difference of the Fermi-level and the valence band ($E_F - E_v$) can also be calculated using Boltzmann statistics from equation (2.6) with $p \approx N_A$, if the doping concentration is not too high.

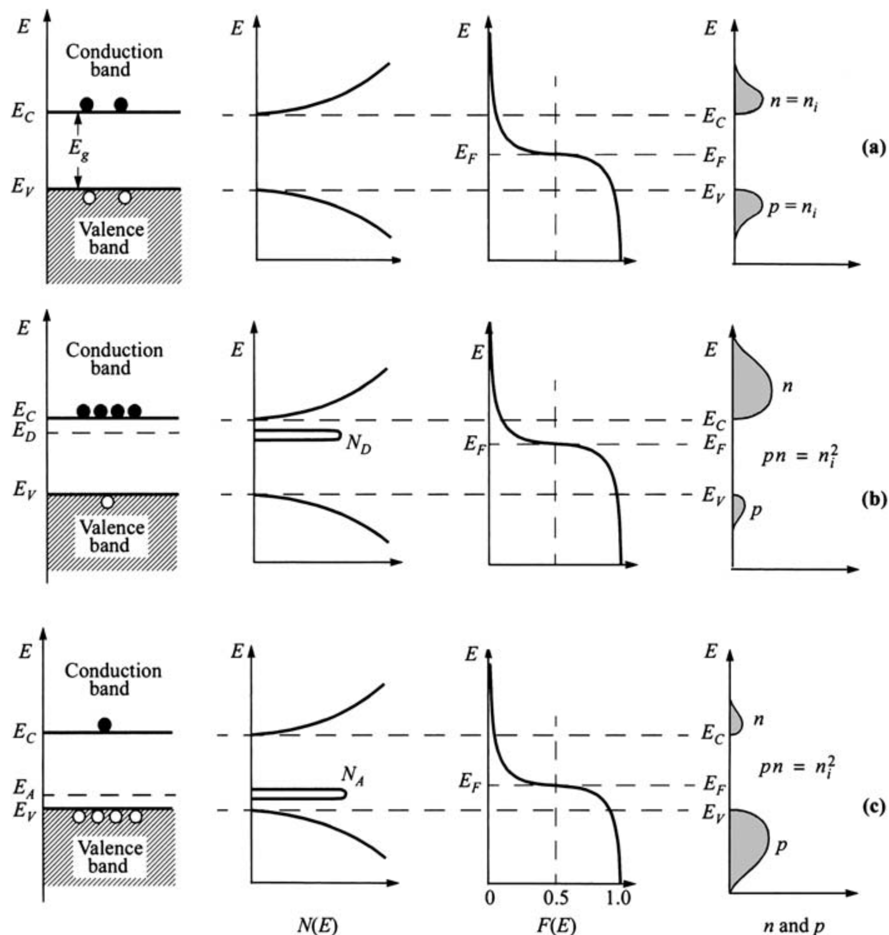

Figure 2.4: Effects of impurity doping on the band-structure, Fermi-Dirac distribution and carrier concentrations. (a) intrinsic state, (b) n-type doping and (c) p-type doping [35].

2.2.4 Doping Profiles

Doping profiles occur between regions of different doping concentrations or doping types. In the n-TFET that is the case at the source/channel (p^{++} to intrinsic) and drain/channel (n^{+} to intrinsic) interface. The abrupt doping profile at the source/channel junction, as shown in figure 2.1, is the best achievable result to enhance the performance of the TFET. However, in reality such a high doping gradient is physically not realistic. During the fabrication of a device in the annealing step directly after the ion-implantation, the dopants diffuse from the highly doped region in the region with less doping [36]. This effect results in characteristic doping profiles at the channel junctions, which can be described with Gaussian distributions or error-functions [37].

In the TFET two Gaussian distributions are declared for the doping profiles at the source/channel and drain/channel interface. The Gaussian distributions are described using a peak concentration from the highly doped area N_{peak} and a peak position x_{peak}. The extension into the channel region is described using a standard deviation σ for which stands at the source/channel interface $N(x_{peak} + \sigma) = N_{peak}/2$. The general profile $N(x)$ is given with

$$N(x) = N_{peak} \cdot \exp\left(-\frac{1}{2} \cdot \left[\frac{x - x_{peak}}{\sigma}\right]^2\right). \tag{2.10}$$

Figure 2.5 illustrates the Gaussian doping distributions in the channel region. The constant doping concentrations in source/drain region $N^0_{s/d}$ are used for the peak concentration N_{peak} in equation (2.10). The doping profile at the source/channel junction for $x \geq 0$ is given with $x_{peak} = 0\ nm$:

$$N_s(x \geq 0) = N^0_s \cdot \exp\left(-\frac{1}{2} \cdot \left[\frac{x}{\sigma}\right]^2\right). \tag{2.11}$$

In the drain region the doping concentration is constant with $N_d = N^0_d$. In the channel region the doping profile for $x \leq l_{ch}$ and $x_{peak} = l_{ch}$ is given with

$$N_d(x \leq l_{ch}) = N^0_d \cdot \exp\left(-\frac{1}{2} \cdot \left[\frac{x - l_{ch}}{\sigma}\right]^2\right). \tag{2.12}$$

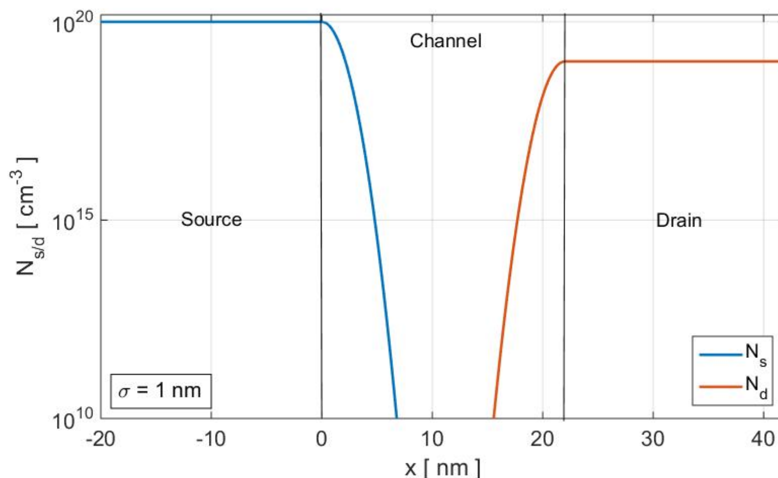

Figure 2.5: Realistic doping concentrations along the TFET. Constant doping in source and drain region with $N^0_s = 10^{20}\ cm^{-3}$, $N^0_d = 10^{19}\ cm^{-3}$. Doping profiles at the channel junctions with $\sigma = 1\ nm$.

2.2.5 Semiconductor Degeneration

If the doping concentration of a semiconductor is near or higher than the effective density of states, the semiconductor degenerates and the Boltzmann statistic are getting invalid. The exact value of the Fermi-Dirac integral has to be considered [35]. To simplify the model, the values describing the degeneration energy of the p-doped source region E_s and the n-doped drain region E_d, shown in figure 2.6, are extracted from TCAD Sentaurus. They are described with

$$E_s = E_v(-l_{sd}) - E_F(-l_{sd}), \quad (2.13)$$

$$E_d = E_c(l_{ch} + l_{sd}) - E_F(l_{ch} + l_{sd}). \quad (2.14)$$

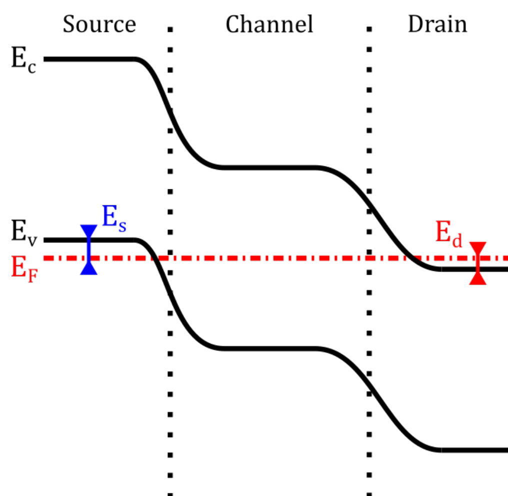

Figure 2.6: Values E_s and E_d describing the degeneration of the semiconductor in source and drain region.

In table 2.1 the extracted degeneration values for all used doping types and concentrations are listed. The accuracy of these values is assured because in the simulator the Fermi-Dirac integral is solved to obtain them [37].

Table 2.1: Degeneration values for different doping types and doping concentrations.

doping [cm^{-3}]	E_d [meV]	E_s [meV]
10^{20}	−62.94	58.47
$5 \cdot 10^{19}$	−30.07	
10^{19}	23.97	
$5 \cdot 10^{18}$	43.47	

2.2.6 Band-gap Narrowing

Through experiments it is observed, that a particularly high impurity concentration within a semiconductor leads to a shrinkage of the band-gap, called band-gap narrowing (bgn) [38–40]. The impurity states within the band-gap of the device overlap and form an additional impurity band (indicated in figure 2.4), thus reducing the intrinsic band-gap of the semiconductor E_g^0. For p-type doped semiconductors, the valence band is shifted upwards, and for an n-type doping the conduction band is shifted downwards. This reduction of the conduction band minimum and the valence band maximum can have a significant influence on the device behavior and has to be modeled carefully. There are different models available for different doping types.

The first band-gap narrowing model for p-type silicon is introduced by Slotboom in 1976 [38]. It describes the band-gap reduction ΔE_g^0 in dependency of the acceptor doping concentration N_A (see fig. 2.7 [a])

$$\Delta E_g^0 = 6.92 \cdot 10^{-3} \cdot \sqrt{\ln\left(\frac{N_A}{1.3 \cdot 10^{17}}\right)^2 + \frac{1}{2}}, \tag{2.15}$$

whereby the model is valid for doping concentrations above $1.3 \cdot 10^{17}\ cm^{-3}$.

For n-type silicon and SiGe the Del Alamo model, introduced in [39], which is implemented for donor doping concentrations N_D above $7 \cdot 10^{17}\ cm^{-3}$

$$\Delta E_g^0 = -14.07 \cdot 10^{-3} + 18.7 \cdot 10^{-3} \cdot \ln\left(\frac{N_D}{7 \cdot 10^{17}}\right). \tag{2.16}$$

For n-type InGaAs the Jain and Roulsten model is used for the band-gap narrowing calculations [41]

$$\Delta E_g^0 = \left(15.5 \cdot N_D^{1/3} \cdot 10^{-9} + 1.95 \cdot N_D^{1/4} \cdot 10^{-7} + 159 \cdot N_D^{1/2} \cdot 10^{-12}\right) 10^{-3} \tag{2.17}$$

and for p-type InGaAs stands

$$\Delta E_g^0 = \left(9.2 \cdot N_A^{1/3} \cdot 10^{-9} + 3.57 \cdot N_A^{1/4} \cdot 10^{-7} + 3.56 \cdot N_A^{1/2} \cdot 10^{-12}\right) 10^{-3}. \tag{2.18}$$

The effective band-gap E_g can be calculated with

$$E_g = E_g^0 - \Delta E_g^0. \tag{2.19}$$

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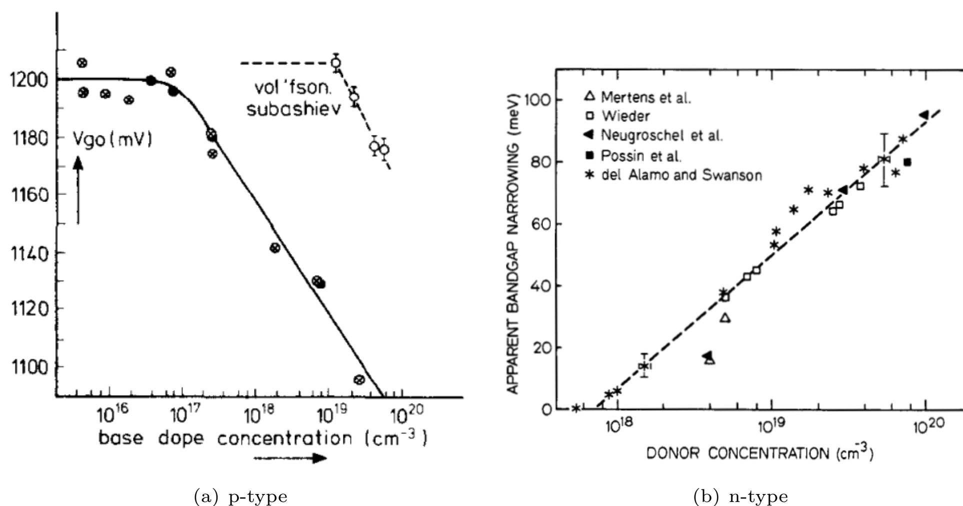

(a) p-type (b) n-type

Figure 2.7: Bandgap narrowing models for [a] p-type silicon: Slotboom [38] and [b] n-type silicon: Del Alamo [39].

The band-gap narrowing of the heavily doped regions in source and drain in combination with steep doping profiles leads to kinks in the band-structure of the TFET. Figure 2.8 schematically illustrates these influences.

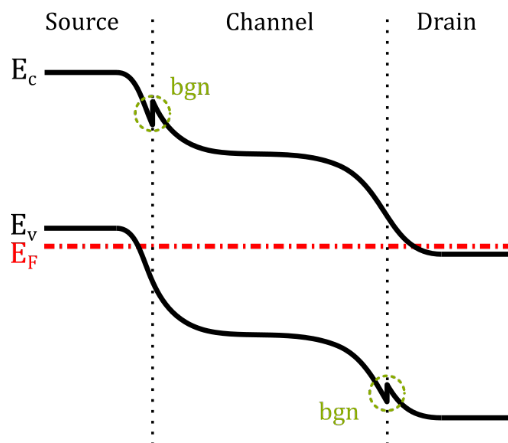

Figure 2.8: Influences of band-gap narrowing on the band-structure in the TFET.

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2.2.7 Hetero Structures

A hetero structure describes the combination of different semiconducting materials in order to form a specific band-structure and enhance device performance. Thereby, material combinations are chosen which differ in carrier mobility and band-gap size. These differences manifest themselves in a distorted band-structure at the material interface (see figure 2.9).

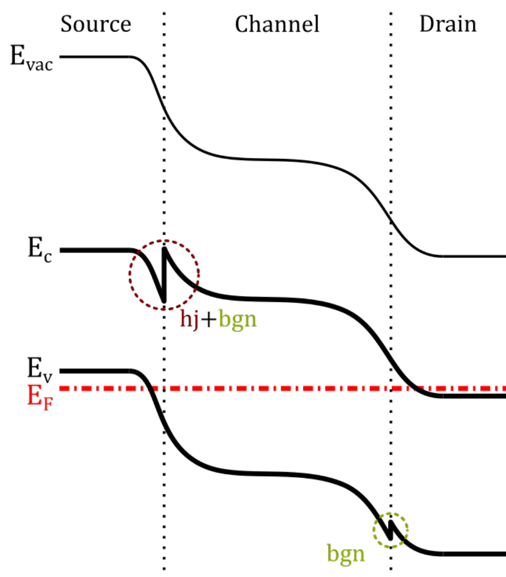

Figure 2.9: Schematic band-structure of an n-TFET, including band-gap narrowing and hetero structures. Small band-gap material in source.

2.2.8 Screening Length

The screening length λ is a commonly used simple expression which grants insight into the quality, and with that, the performance of a device. It is a rough estimation of the band-bending distance at the source/channel λ_s and drain/channel junction λ_d of the TFET (see fig. 2.10). The most simplest 1D models are using this value to estimate the tunneling distance of a TFET. In case of a double-gate device $\lambda_{s/d}$ can be estimated quasi two-dimensionally in a mathematically more complex form [42]

$$\lambda(y) = \lambda_{fit} \cdot \sqrt{\frac{\epsilon_{ch} \cdot t_{in} \cdot t_{ch}}{2 \cdot \epsilon_{in}} \left(1 + \frac{\epsilon_{in} \cdot y}{\epsilon_{ch} \cdot t_{ch}} - \frac{\epsilon_{in} \cdot y^2}{\epsilon_{ch} \cdot t_{in} \cdot t_{ch}}\right)}, \tag{2.20}$$

with the material dependent relative permittivity $\epsilon_{in/ch}$ and a fitting factor λ_{fit}.

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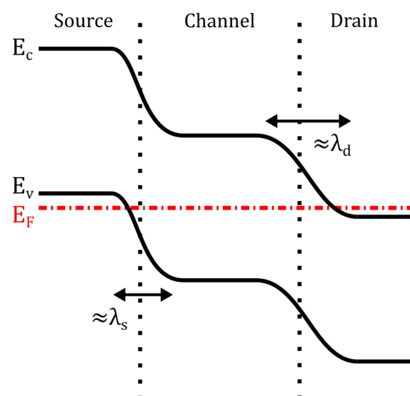

Figure 2.10: Screening length estimation at source/channel junction λ_s and drain/channel junction λ_d.

2.3 Tunnel Effect

In this section the basics of the tunnel effect are explained since it is the core of the new current transport mechanism within the TFET. The tunnel effect describes the phenomenon in which a carrier is able to transmit a finite energy barrier even though its energy is smaller than said barrier. This effect can not be captured with classical physics and is based on the wave-particle dualism in quantum electronics. The wavefunction does not end abruptly at a limited barrier and if the barrier thickness is short enough, the wavefunction is not negligible anymore on the other side. As a first approach the tunneling probability T is calculated for a simple rectangular barrier as shown in figure 2.11.

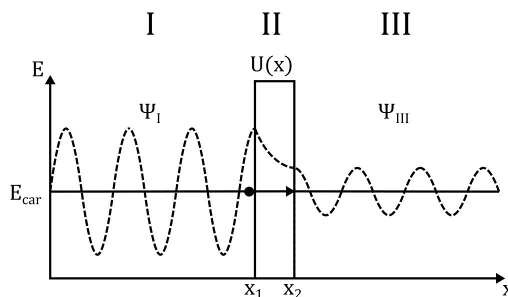

Figure 2.11: Rectangular barrier tunneling.

The wavefunction within the barrier Ψ_{II} has to be determined from the general Schrödinger equation [35]

$$\frac{d^2\Psi}{dx^2} + \frac{2m}{\hbar^2}[E_{car} - U(x)]\Psi = 0, \tag{2.21}$$

with the carrier energy E_{car}, the barrier $U(x)$, the effective carrier mass m and the reduced Planck constant $\hbar$. For a constant barrier height $U(x) = U_0$ and thickness t, the wavelength solution has the form

$$\Psi_{II} = \Psi_{II}^{+} - \Psi_{II}^{-} = C \cdot e^{+ikx} - D \cdot e^{-ikx} \tag{2.22}$$

with $k = \sqrt{2m(E_{car} - U(x))}/\hbar$. Outside the barrier ($U(x) = 0$), the waveforms have the solution

$$\Psi_{I} = \Psi_{I}^{+} - \Psi_{I}^{-} = A \cdot e^{+ikx} - B \cdot e^{-ikx} \tag{2.23}$$

$$\Psi_{III} = \Psi_{III}^{+} - \Psi_{III}^{-} = E \cdot e^{+ikx} - F \cdot e^{-ikx} \tag{2.24}$$

In figure 2.12 Ψ_{I}^{+} represents the incoming wave, Ψ_{I}^{-} the reflected wave and Ψ_{III}^{+} the transmitted wave. Ψ_{III}^{-} is 0 since the wave does not reflect in region III.

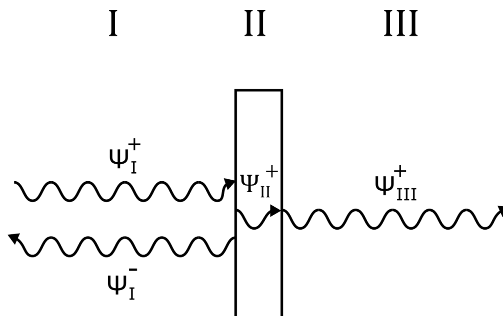

Figure 2.12: Wave components for the rectangular barrier tunneling calculation.

Therefore, the tunneling probability T is the ratio of the transmitted carrier probability in region III $|\Psi_{III}|^2$ and the carrier probability $|\Psi_I|^2$

$$T = \frac{|\Psi_{III}|^2}{|\Psi_I|^2}. \tag{2.25}$$

The constants A, B, C, D, E, F can be calculated by applying boundary conditions to assure continuity:

$$\begin{aligned}
\Psi_I(x_1) &= \Psi_{II}(x_1) \\
\frac{d\Psi_I(x_1)}{dx} &= \frac{d\Psi_{II}(x_1)}{dx} \\
\Psi_{II}(x_2) &= \Psi_{III}(x_2) \\
\frac{d\Psi_{II}(x_2)}{dx} &= \frac{d\Psi_{III}(x_2)}{dx} \\
\Psi_{II}^{-} &= 0 \\
\Psi_{III}^{-} &= 0
\end{aligned}$$

With the solution of the wavefunction, the tunneling probability is calculated to be [35]

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$$
\begin{aligned}
T &= \left(1 + \frac{U_0^2 \sinh^2(|k|t)}{4E_{car}(U_0 - E_{car})}\right)^{-1} \\
&\approx \frac{16E_{car}(U_0 - E_{car})}{U_0^2} \exp\left(-2|k|t\right). \qquad (2.26)
\end{aligned}
$$

This solution is only valid for a rectangular tunneling barrier. In reality though, the tunneling barriers have a more complex form. Therefore, in a next step the tunneling probability is estimated for a triangular barrier profile, where $U(x)$ is reduced linearly as shown in figure 2.13. This approach is firstly introduced by Wentzel, Kramers and Brillouin and hence called the WKB approximation [43–45]. This method is applicable if the potential barrier $U(x)$ does not vary rapidly due to the assumption of a partially constant barrier in the carrier wavelength scale [35].

A closer look on equation 2.26 shows, that the prefactor $16E_{car}(U_0 - E_{car})/U_0^2$ is not negligible but weakly dependent on the energy, whereas $\exp\left(-2|k|t\right)$ has a strong dependency. The WKB approximation shows a similar expression but here the area of the constant barrier $|k|t$ is replaced with an integral over the barrier [35]

$$
\begin{aligned}
T = \frac{|\Psi_{III}|^2}{|\Psi_I|^2} &\approx \exp\left(-2\int_{x_1}^{x_2} |k(x)|dx\right) \\
&\approx \exp\left(-2\int_{x_1}^{x_2} \sqrt{\frac{2m}{\hbar^2}(U(x) - E_{car})dx}\right). \qquad (2.27)
\end{aligned}
$$

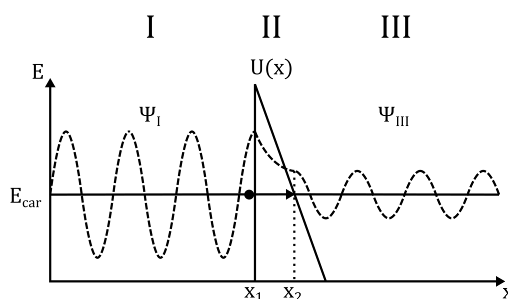

Figure 2.13: WKB approximation for triangular barrier tunneling.

The triangular tunneling barrier is used to calculate the occurring tunneling events within the TFET. The resulting current density can be calculated with the amount of carriers in region I and the amount of free states in region III [35]

$$J = \frac{qm}{2\pi\hbar^3} \int f_I N_I T (1 - f_{III}) N_{III} dE, \tag{2.28}$$

with the Fermi-Dirac distributions $f_{I/III}$ and the density of states $N_{I/III}$ in the respective regions.

2.4 Tunnelling Events

There are several possible tunneling events that can occur in semiconductors. In this section a short overview is given with a more detailed description of the tunneling events happening within the TFET.

Figure 2.14 illustrates the occurring events to pass a energy barrier. The first one is the conventional overcoming of the barrier due to thermionic emission. The carrier gains more energy than the energy barrier and passes above it. The following events are all linked to single-band barrier tunneling, like gate insulator tunneling. The most simplest form is the direct barrier tunneling at low energy levels, where the barrier thickness is the largest. If defect states (traps) are present in the forbidden region of the barrier a trap-assisted tunneling (tat) is possible, therefore the carrier gains energy till it has the same energy-level as the trap, which enables a tunneling into it. From the trap, a second tunneling step happens to the other side of the barrier. If the carrier gains enough energy to reach the region where the energy barrier thickness decreases (triangular area) and a tunneling event occurs, this is called Fowler-Nordheim (FN) tunneling [35]. Through the decreasing barrier thickness for higher energy levels, the tunneling probability is increasing successively, which enables the tunneling. Additionally, there is a combination of FN and trap-assisted tunneling.

In the TFET no single-band events occur, but instead band-to-band tunneling dominates. Figure 2.14 also illustrates the two important band-to-band tunneling events. Direct tunneling is possible in the region, where the bands overlap and a tunneling through the forbidden region occurs. Similar to the single-band tunneling, here also a trap-assisted tunneling is possible for carriers with the same energy level as the trap. They can emit into the trap and subsequently tunnel onto the right-hand band.

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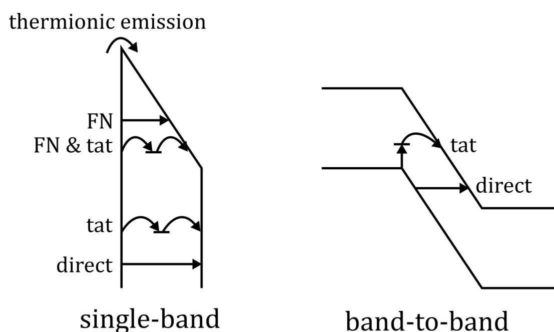

Figure 2.14: Single- and band-to-band tunneling events: Fowler-Nordheim (FN), trap-assisted tunneling and direct tunneling. Carriers can overcome the barrier with thermionic emission.

2.4.1 Trap-Assisted-Tunneling

In order to calculate the trap-assisted tunneling probability, it is important to know where the traps occur and how they are distributed at this position. Within the TFET, the traps are located at the source/channel and drain/channel junction of the device [46]. One of the reasons for that is the transition of the heavily doped source and drain region to the undoped channel. The lattice mismatch in this transition regions generates defects, which lead to states within the band-gap of the semiconductor where carriers are allowed to emit into. The different trap types can be occupied by electrons, holes or no carriers at all. The carrier amount that can emit to a defect in a specific time is described with the carrier emission rate e [37].

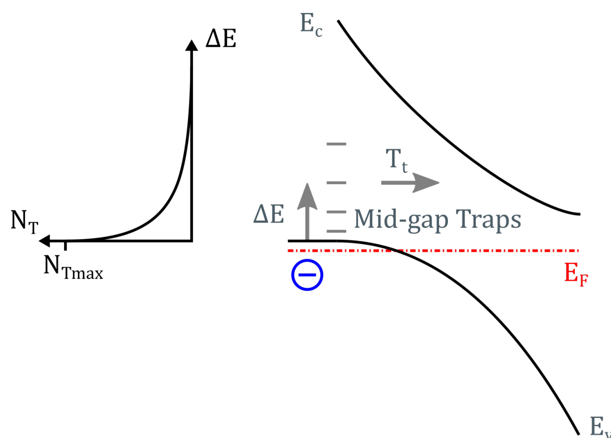

Figure 2.15: Schematic band-structure at the source/channel junction showing the trap distribution for the trap-assisted tunneling mechanism.

Figure 2.15 shows the exponential trap distribution N_T with the maximum trap concentration N_{Tmax}. For the distribution within the band-gap ($0 \leq \Delta E \leq E_g$) stands [47]

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$$N_T = N_{Tmax} \cdot \exp\left(-\frac{\Delta E}{n \cdot kT}\right), \tag{2.29}$$

with a positive integer number n. To show the density of trapped carriers N_{Tc}, the trap distribution can be coupled with the Fermi distribution (either electrons or holes) [47]

$$N_{Tc} = N_T \cdot f. \tag{2.30}$$

For calculating the trap-assisted tunneling probability T_{tat}, the WKB-approximation from equation (2.27) can be used. In the last step, the trap-assisted tunneling calculation differs from the band-to-band based one due to the limited trap states and emission rate on one side of the barrier [48]. The tat current density J_{tat} is given with

$$J_{tat} = q \int_{E_v}^{E_c} N_t \cdot e \cdot T_{tat} \cdot f_{II} \cdot dE. \tag{2.31}$$

2.5 Working Principle

The working principle of the TFET can be explained by means of its band-structure. Therefore, the bands along the x-cross-section, shown in figure 2.16 (a), are investigated. The cross-section is chosen to be directly below the gate insulator since here the electrostatic influence of the gate electrode on the channel region is the biggest, which results in the highest current density in the device. Figures 2.16 (b) - (d) show the three different states of the n-TFET.
Before explaining the working principle, some remarks regarding the band-structure are necessary. The high p-doping in source region leads to a degradation of the semiconductor, therefore the bands are shifted in such a drastic way, that even the valence band E_v is energetically above the Fermi level E_F. A similar behavior can be seen in the drain region, only here the degradation is smaller due to the reduced drain doping and the conduction band E_c is shifted below the Fermi level for n-type doping. Because of the intrinsic channel region, here the Fermi level is directly in the middle of the band-gap.

The first band-structure in figure 2.16 (b) shows the operating regime of the n-TFET: the on-state. A positive gate bias V_g shifts the bands in the channel region downwards. At the source/channel interface an overlap of the valence band in source region and the conduction band in the channel region occurs. The higher the gate voltage, the bigger the overlap and the smaller becomes the horizontal distance between the bands. This small distance and the steepness of the bands correlate directly with the probability of electron band-to-band tunneling, and with that, the on-state current.

By reducing the gate voltage, the band overlap at both channel junctions disappears and

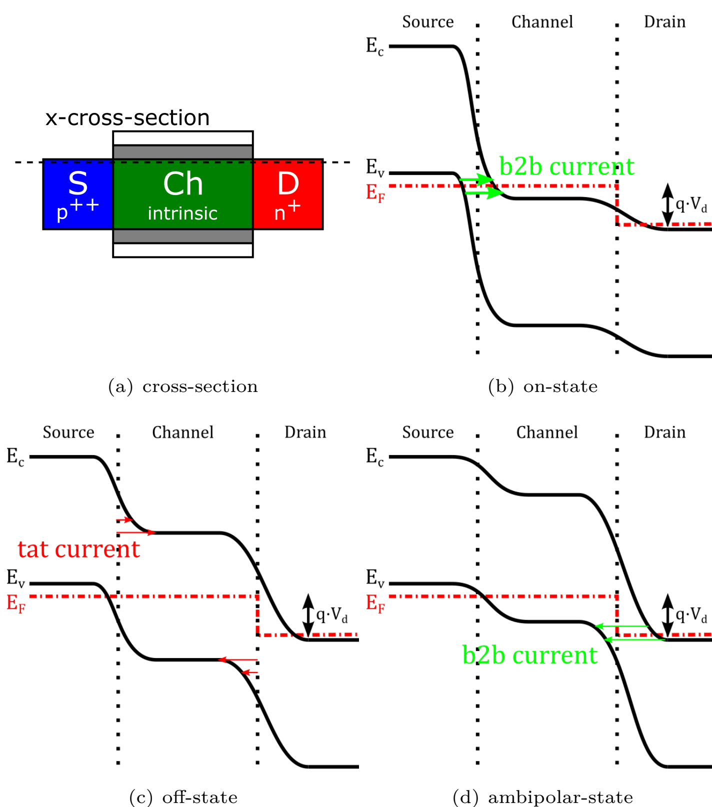

Figure 2.16: (a) x-cross-section for band-structure illustration. Schematic band-structure of a n-TFET in (a) on-state, (b) off-state and (c) ambipolar-state. On-state: b2b-current at source/channel interface. Off-state: tat-current at channel interfaces. Ambipolar-state: b2b-current at drain/channel interface.

the device enters the off-state shown in figure 2.16 (c). For an idealistic device the current would be 0 in this state. However, in fabricated devices an off-current occurs, which worsens the subthreshold slope and the on/off-ratio. During the fabrication of the device, interface defect states (traps) occur at the channel junctions due to the lattice mismatch caused by the doping. These defects express themselves as traps in the bandgap, which can be occupied by carriers with the help of thermionic emission. Once a trap is occupied by a carrier, it has the possibility to horizontally tunnel along to the channel region of the device, thus creating a leakage trap-assisted-tunneling current. This effect firstly occurs with electrons for higher gate biases at the source/channel junction and then is superseded by holes at the drain/channel junction for lower gate biases.

The last band-structure in figure 2.16 (d) shows a typical TFET effect caused by the symmetry

of the device: the ambipolar-state. Similar to the on-state a band overlap occurs at the drain/channel junction of the device. Only here the conduction band of the drain region overlaps with the valence band of the channel region. Another difference is the tunneling carrier type. Here holes are enabled for direct band-to-band tunneling. This ambipolarity of the TFET is an undesired effect, since it does not occur in the MOSFET and it causes problems in circuit development and design. Different approaches already are investigated to suppress the ambipolar behavior of the TFET [49]. The easiest way to do so, is the reduction of the drain doping concentration, because no changes in the devices geometry have to be made. A reduction of the drain doping results in an increased tunneling distance at the drain/channel junction as shown in figure 2.16 (d) and hence, a reduced ambipolar current. Other possibilities introduced in [49] are the implementation of a gate-underlap to reduce the electrostatic influence of the gate on the drain/channel junction to increase the tunneling distance. The implementation of low-κ gate insulators on the drain-related half of the channel also leads to a reduction of the gate influence in this region and does not require a change in device geometry. Another way to suppress the ambipolar current is by using lateral hetero-structures with wide band-gaps, although this method is too complicated compared to the alternative approaches [49].

Another distinctive behavior of the TFET is the asymmetric source/drain conduction [50]. As a result of the different drain doping type, the source and drain contact are not interchangeable like in the MOSFET. For a positive drain voltage the drain/channel diode is reversed biased, providing a tunneling current at the source/channel interface depending on the gate voltage. By reducing the drain bias the drain/channel diode is forward biased, showing a conventional diode behavior, where the gate bias has an influence on the barrier conduction. This effect leads to an unidirectional behavior of the TFET as shown in figure 2.17. Therefore, some of the conventional MOSFET circuit designs (like the 6T SRAM cell design) are not feasible with the TFET. However, this alternative behavior gives access to new circuit design approaches [51, 52].

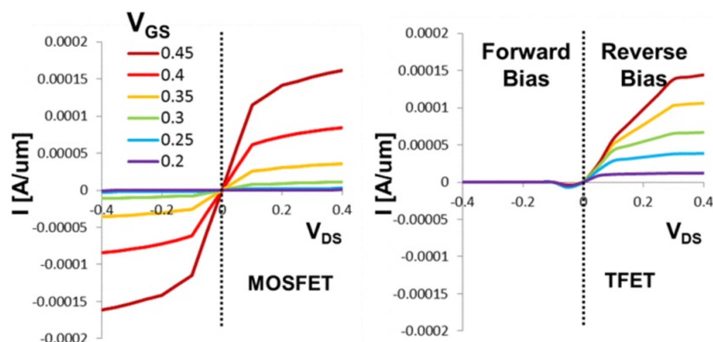

Figure 2.17: Comparison of the MOSFET and TFET output characteristics. The asymmetric structure of the TFET leads to an unidirectional behavior for negative V_{ds} [50].

CHAPTER 3

Mathematical Basics

The potential and electric field solution of the TFET form the basis of the current calculation and have to be modeled accurately. There are different approaches to calculate the potential in a given structure but with increasing complexity of the structure, the calculation gets more complicated and may even not be solvable in a closed form. In this work, the method of conformal mapping is applied to simplify a given structure by transforming it into a different plane, where a potential solution can be obtained more easily.

In this chapter the mathematical basics for the potential and electrical field calculation are explained. In section 3.1 the Poisson and Laplace equation are introduced. They form the basis of the complex potential theory, introduced in section 3.2, where the complex potential is spited in a real potential part and an imaginary dielectric flow part. The theory of conformal mapping of a complex potential is introduced in section 3.3. Finally the potential determination is explained in section 3.4.

3.1 Poisson's and Laplace's Equation

The basic equation to achieve a potential solution for a given electrostatic problem is a partial differential equation based on the Maxwell equations: The Poisson equation. It gives the relation between a potential Φ and electric field E with a charge density ρ, which causes the potential and electric field. For a charge density in a given material (here Si) the electric field stands with [53]

$$\nabla E(x,y,z) = \frac{\rho(x,y,z)}{\epsilon_0 \epsilon_{Si}}. \tag{3.1}$$

The potential and electric field also have a divergence relationship, which can be expressed with [53]

$$\Delta\Phi(x,y,z) = -\nabla E(x,y,z) = -\frac{\rho(x,y,z)}{\epsilon_0 \epsilon_{Si}}. \tag{3.2}$$

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∇ and Δ stand for the derivations in all directions:

$$\nabla = \frac{d}{dx} + \frac{d}{dy} + \frac{d}{dz} \tag{3.3}$$

$$\Delta = \frac{d^2}{dx^2} + \frac{d^2}{dy^2} + \frac{d^2}{dz^2}. \tag{3.4}$$

Based on equation (3.2) the Poisson solution can be obtained by integrating over the charge density ρ in a defined volume V and adding the surface charge σ at the boundary of this volume [53]

$$\Phi(x,y,z) = \frac{1}{4\pi\epsilon} \oiiint_V \frac{\rho(r)}{r} dV + \frac{1}{4\pi\epsilon} \oiint_S \frac{\sigma(r)}{r} \, dS. \tag{3.5}$$

If there is no charge density within the volume $\rho = 0$, Poisson's equation becomes Laplace's equation [53]

$$\Delta\Phi(x,y,z) = 0. \tag{3.6}$$

Functions $\Phi(x,y,z)$ which satisfy the Laplace equation in a defined space (3.6) are called harmonic functions in this space [53]. These harmonic functions have specific properties. They are able to be superposed and the Dirichlet and Neumann conditions are valid [54].

The Dirichlet condition says, that a harmonic function Φ in a defined volume V reaches the boundary condition Φ_v, when approaching the volume boundary. This means there are no kinks in potential in the transition of volume and boundary. The boundary condition is clearly solvable.

The Neumann condition says, that the derivation of a harmonic function Φ in normal direction at the surface S of a defined volume V has to match a predefined value $(d\Phi/dn)_{|S}$. This means there are no kinks in the normal components of the electric field in the transition of volume and boundary. This boundary condition is clearly solvable as well.

It is important to know, that these boundary conditions can be mixed for a single Volume, where in one area Dirichlet boundaries are applied and in another area Neumann conditions are valid.

3.2 Complex Potential

This section explains the basics of the complex potential theory. With the help of complex analysis, it is possible to calculate potential solutions for a simple geometry and to illustrate equipotential lines and lines of force for a given problem. The basic idea is to find an expression for a complex function F, where the real and imaginary part both fulfill the Laplace's equation (3.6) and are perpendicular to each other (like equipotential lines $\Phi = const$ and $\vec{E}$-field). By applying boundary conditions for a given problem, the potential can be solved and the equipotential lines illustrated [53]. Firstly a complex function F is introduced.

$$w = F(z) = \Phi(x,y) + j\Psi(x,y), \tag{3.7}$$

where z is a complex variable $z = x + jy$, Φ and Ψ are real functions. With this complex function a curve in z-plane is directly mapped to another curve in the new w-plane. This mapping is conform or vise versa and the angle is preserved during mapping. Figure 3.1 illustrates a mapped equipotential line. Since Ψ is perpendicular to the equipotential line and for the electrical field stands: $\vec{E} = -\nabla\Phi$. Therefore, Ψ_0 stands for an $\vec{E}$-field line.

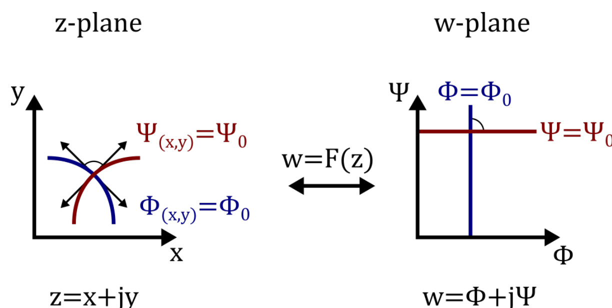

Figure 3.1: Mapping of a complex potential from z-plane to w-plane. Perpendicularity in both planes is given for Φ and Ψ.

If specific boundary conditions are defined in z-plane, the same conditions are valid in w-plane. Furthermore, the curve behavior has to be mapped as well. If a curve in z-plane changes continuously Δz, the corresponding curve in w-plane has to change accordingly Δw.

The necessity of the perpendicularity of the functions Φ and Ψ is granted if the complex function F is analytic [53]. This implies, that F is also differentiable, meaning that the limit

$$\frac{\partial F}{\partial z} = \lim_{\Delta z \to 0} \frac{F(z + \Delta z) - F(z)}{\Delta z} \tag{3.8}$$

$$= \lim_{\Delta x, \Delta y \to 0} \frac{\left(\frac{\partial \Phi}{\partial x} + \frac{\partial \Psi}{\partial x}\right)\Delta x + j\left(-\frac{\partial \Phi}{\partial y} + \frac{\partial \Psi}{\partial y}\right)\Delta y}{\Delta x + j\Delta y} \tag{3.9}$$

is unique and independent of the direction of Δz. This can be achieved by setting $\Delta y = \alpha \Delta x$, thus α identifies as direction of Δz. The limit from equation (3.9) then reduces to [53]

$$\frac{\partial F}{\partial z} = \lim_{\Delta x \to 0} \frac{\left(\frac{\partial \Phi}{\partial x} + \frac{\partial \Psi}{\partial x}\right) + j\left(-\frac{\partial \Phi}{\partial y} + \frac{\partial \Psi}{\partial y}\right)\alpha}{1 + j\alpha}. \tag{3.10}$$

Independency from α is only given if the bracket terms from equation (3.10) are equal [53]:

$$\frac{\partial \Phi}{\partial x} + \frac{\partial \Psi}{\partial x} = -\frac{\partial \Phi}{\partial y} + \frac{\partial \Psi}{\partial y} \tag{3.11}$$

or

$$\frac{\partial \Phi}{\partial x} = \frac{\partial \Psi}{\partial y} \quad , \quad \frac{\partial \Phi}{\partial y} = -\frac{\partial \Psi}{\partial x} \tag{3.12}$$

The equations (3.12) are the Cauchy-Riemann differential equations. They grant perpendicularity between Φ and Ψ and indicate an analytic function. They also fulfill Laplace's equation (3.6).

3.3 Conformal Mapping

In this section the conformal mapping is introduced. It is used to transform a rather complicated domain D in z-plane onto a simpler domain D^* in w-plane with the help of an analytic transformation function $t^{-1}(z)$. In w-plane the complex potential $\tilde{F}(w)$ can be solved more easily:

$$\tilde{F}(w) = \tilde{\Phi}(w) + j\tilde{\Psi}(w), \tag{3.13}$$

whereby the real $\tilde{\Phi}$ and imaginary $\tilde{\Psi}$ parts have to satisfy Laplace's equation (3.6) and boundary conditions in w-plane [55]. Figure 3.2 illustrates the mapping of D in z-plane onto D^* in w-plane with the help of $t^{-1}(z)$. The boundary condition Φ_0 is mapped as well.

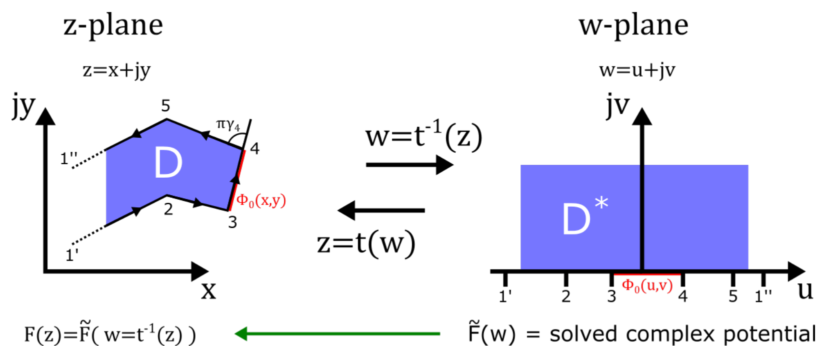

Figure 3.2: Conformal mapping of a domain D in z-plane onto a domain D^* in w-plane with help of the complex transformation function $w = t^{-1}(z)$. The boundary condition Φ_0 is mapped as well. The complex potential $\tilde{F}(w)$ is easily solvable in w-plane. The complex potential $F(z)$ in z-plane from equation (3.7) is derived by the inverse transformation $F(z) = \tilde{F}(w = t^{-1}(z))$.

After solving the complex potential $\tilde{F}(w)$ in w-plane, the complex potential $F(z)$ in z-plane can be derived by the inverse transform [55]

$$F(z) = \tilde{F}(w)|_{w=t^{-1}(z)}. \tag{3.14}$$

The real potential is given within the real-part of the complex potential $F(z)$

$$\Phi(x,y) = \mathrm{Re}(F(z = x + jy)). \tag{3.15}$$

3.3.1 Mapping of a Closed Polygon

After describing the general purpose of the conformal mapping technique in section 3.3, this section is focused on the complex transformation function $t(w)$, which is the key of this technique.

Depending on the geometry which is going to be mapped, the transformation function differs. Since the focus in this thesis lays on a double gate TFET structure, the transformation function should be valid for a closed polygon. Figure 3.2 shows such a closed polygon in z-plane with the assumption that the points $1'$ and $1''$ extend to infinity (meet in infinity) [55]. The transformation function, which can be used for such a case, is called Schwarz-Christoffel transformation. The mapping is firstly done from w- to z-plane, since the complex potential solution is calculated in w-plane. The desired link from a position in z-plane to the complex potential solution $\tilde{F}(w)$ follows later in section 3.3.2.
Firstly, at this point, the transformation maps a domain D^* in the upper half of the w-plane, where a potential solution can be easily determined onto the domain D of a closed polygon in z-plane, for which a potential solution should be obtained, thereby the real axis in w-plane is directly mapped onto the edges of the polygon. Therefore, the derivation dz/dw of the transformation function $t(w)$ is calculated [55]

$$\frac{dz}{dw} = C(w - w_1)^{-\gamma_1}(w - w_2)^{-\gamma_2}...(w - w_n)^{-\gamma_n} = C\prod_i (w - w_i)^{-\gamma_i}. \tag{3.16}$$

The corner points of the polygon from figure 3.2 are given with $z_i = t(w_i)$, whereby $\pi\gamma_i$ describes the change of angle at said corner. The closed region always has to be on the left side [55]. The points $1'$ and $1''$ are not considered by the mapping function. In order to obtain the transformation function $t(w)$, equation 3.16 is integrated

$$t(w) = C\int\prod_i (w - w_i)^{-\gamma_i} dw + E. \tag{3.17}$$

E describes the origin of the z-plane. The paramters of the conformal mapping function $t(w)$ can be calculated by finding relations with the z-plane. The distance of the two parallel edges of the polygon in figure 3.3 can be calculated by defining the angle for the last factor $\gamma_n = 1$ ($\hat{=}180^\circ$), for which $z_n = \infty$ [53]

$$z_n^{'} - z_n^{''} = j\pi C\prod_{i\neq n} (w - w_i)^{-\gamma_i}. \tag{3.18}$$

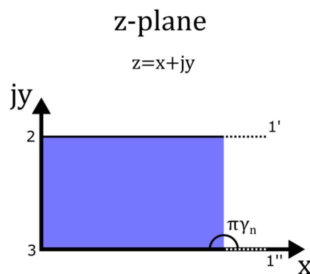

Figure 3.3: Angle definition for an infinite rectangle.

In the case for point 1 in figure 3.2 $w_n = \pm\infty$ on the real axis in w-plane is defined, therefore the distance can be calculated by [55]

$$z_n^{'} - z_n^{''} = j\pi C. \tag{3.19}$$

With N corner points of a polygon, the integration constants C, E from the transformation function (3.17) and the points in w-plane w_n, there are $N+2$ unknown parameters, from which three are freely selectable. The remaining $N-1$ parameters can be calculated with the help of equation (3.18) and (3.19) [55].

When all paramters in w-plane are chosen in a way that the integral expression from equation (3.17) is integrateable in closed form, then the inverse function from $t(w)$ enables the desired calculation of a w-plane position with z-plane coordinates:

$$w = t^{-1}(z). \tag{3.20}$$

3.3.2 Double-Gate Structure Mapping

Firstly, the double-gate structure has to be decomposed from a four corner problem into two two corner problems, namely source- and drain-related case. With the Schwarz-Christoffel-transformation from equation (3.17), the transformation function of an unlimited expanding double-gate structure can be found. Therefore, the corner points of the structure in z-plane are linked to specific locations on the u-axis in w-plane: $z_1 = \infty$ to $w_1 = \pm\infty$ with $\gamma_1 = 1$, z_2 to $w_2 = -1$ with $\gamma_2 = 1/2$, z_5 to $w_5 = +1$ with $\gamma_5 = 1/2$. The boundary conditions Φ_s and Φ_g are mapped as well. Over the insulator, between points 2/3 and 4/5, the boundaries are assumed to be linear Φ_{lin}. Figure 3.4 illustrates the original and mapped geometry. Here only the decomposed source-related case is shown but the mapping for the drain-related case is also done later in this section.

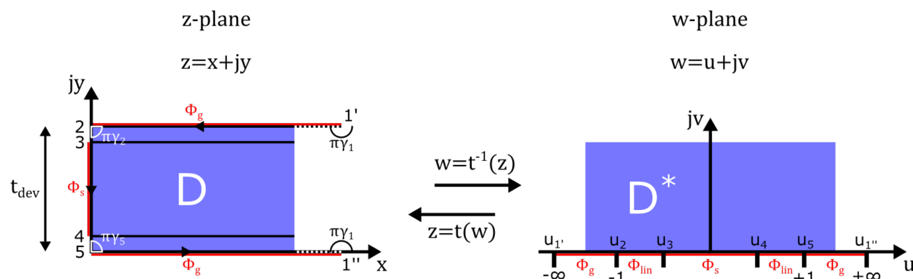

Figure 3.4: Mapping of the source-related double-gate structure from z- to w-plane, including boundary conditions Φ_g, Φ_s. The boundaries over the insulator between points 2/3 and 4/5 are assumed to be linear Φ_{lin}. Specific points in w-plane are chosen for the mapping of the edges of the structure: $z_1 = \infty$ to $w_1 = \pm\infty$ with $\gamma_1 = 1$, z_2 to $w_2 = -1$ with $\gamma_2 = 1/2$, z_5 to $w_5 = +1$ with $\gamma_5 = 1/2$.

With the chosen point definition, the derivative of the transfer function $z = t(w)$ can be expressed

$$\frac{dz}{dw} = \frac{C}{\sqrt{w-1}\cdot\sqrt{w+1}}. \tag{3.21}$$

Through integration, the transformation function reads

$$z = t(w) = C\cdot\cosh^{-1}(w) + E \tag{3.22}$$

The origin of the coordinate system is irrelevant and therefore $E = 0$. The factor C can be calculated with the distance of the parallel lines (device thickness t_{dev} from fig. 3.4) from equation (3.19)

$$C = \frac{z_1^{'} - z_1^{''}}{j\pi} = \frac{t_{dev}}{\pi}. \tag{3.23}$$

With all constants solved, the transformation function is expressed with

$$z = t(w) = \frac{t_{dev}}{\pi}\cdot\cosh^{-1}(w). \tag{3.24}$$

At this point the domain D^* in w-plane from figure 3.4 can be linked with D in z-plane. Now only a function $w = t^{-1}(z)$ is missing, mapping D in z-plane to D^* in w-plane, so all boundary conditions and the original structure given in z-plane can be mapped as well. Only if this function exists, the mapping is truly conform. It can be calculated with the inverse function t^{-1} of the transformation function t:

$$w = t^{-1}(z) = \cosh\left(\frac{\pi\cdot z}{t_{dev}}\right) \tag{3.25}$$

With the help of the inverse transformation function $t^{-1}(z)$ from equation (3.25), the corner points of the structure in figure 3.4 are mapped. For the drain-related case, the structure in z-plane is mirrored at the y-axis and the point definition is vice versa, since the mapped area always has to be on the left hand side. In w-plane the positions on the u-axis stay the same. For mapping the points in $z = \infty$ a distance was chosen to fulfill the $l_{ch} > t$ condition: $z = 3\cdot l_{ch}$.

Table 3.1: Conformal mapping of source- and drain-related DG-structures

z–Plane Point	Source – Related	Drain – Related	w–plane Point
$1^{'}$	$(3\cdot l_{ch} \mid t_{ch} + 2\cdot\tilde{t}_{in})$	$(-2\cdot l_{ch} \mid 0)$	$u_{1'}$
2	$(0 \mid t_{ch} + 2\cdot\tilde{t}_{in})$	$(l_{ch} \mid 0)$	u_2
3	$(0 \mid t_{ch} + \tilde{t}_{in})$	$(l_{ch} \mid \tilde{t}_{in})$	u_3
4	$(0 \mid \tilde{t}_{in})$	$(l_{ch} \mid t_{ch} + \tilde{t}_{in})$	u_4
5	$(0 \mid 0)$	$(l_{ch} \mid t_{ch} + 2\cdot\tilde{t}_{in})$	u_5
$1^{''}$	$(3\cdot l_{ch} \mid 0)$	$(-2\cdot l_{ch} \mid t_{ch} + 2\cdot\tilde{t}_{in})$	$u_{1''}$

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The points on the u-axis are used in section 4.4 as integration borders for the Poisson integral. An arbitrary point within the channel region in z-plane for the source-related case can be expressed with the mapping function $t^{-1}(z)$ from equation (3.25)

$$w_s(z) = u + jv = \cosh\left(\frac{\pi(x + j(\tilde{t}_{in} + y))}{t_{dev}}\right) \tag{3.26}$$

and for the drain-related case stands

$$w_d(z) = u + jv = \cosh\left(\frac{\pi((l_{ch} - x) + j(\tilde{t}_{in} + y))}{t_{dev}}\right). \tag{3.27}$$

3.4 Potential Determination

This section explains the calculation of a complex potential solution in w-plane. As mentioned before in section 3.3, a potential solution in closed form for a transformed geometry in w-plane should be easier to obtain than for the original geometry in z-plane. In general, mixed boundary condition problems (Dirichlet and Neumann) occur for the potential solution of a double-gate structure. In this work, the boundary conditions are chosen in a way, that only Dirichlet boundary conditions are used for the potential solution [56].

One method to calculate the desired potential in the D^* domain of the w-plane (see figure 3.2) for an arbitrary boundary condition $\Phi_0(\overline{u})$ is with the help of the Poisson's integral [53]

$$\varphi(u,v) = \frac{1}{\pi}\int_{-\infty}^{+\infty} \frac{v}{(u-\overline{u})^2 + v^2}\Phi(\overline{u})\, d\overline{u}. \tag{3.28}$$

The mapped boundary conditions $\Phi(\overline{u})$ are linked with the z-plane by the inverse transformation function

$$\Phi(\overline{u}) = \Phi(t^{-1}(z)). \tag{3.29}$$

If the boundary condition is located on the u-axis in w-plane between two points $\overline{u}_1$ and $\overline{u}_2$ then the integral is reduced to:

$$\varphi(u,v) = \frac{1}{\pi}\int_{\overline{u}_1}^{\overline{u}_2} \frac{v}{(u-\overline{u})^2 + v^2}\Phi(\overline{u})d\overline{u}. \tag{3.30}$$

The resulting potential solution $\varphi(u,v)$ can also be directly linked to z-plane coordinates with the inverse transformation function:

$$\varphi(x,y) = \varphi(w = t^{-1}(z)) \tag{3.31}$$

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3.5 Electric Field Determination

Determining the potential solution is only one part of the necessary electrostatic solution for the device. Another important part is the calculation of the electric field. The following section shows the development of a closed form solution of said electric field starting with the basic idea of a summation of small potential differences using the single-vertex approach followed by the closed form boundary integral.

Since the boundary conditions only apply on parts of the u-axis in w-plane and superposition is possible, the following solution is a general approach for two different boundary conditions on the u-axis with an infinitesimal gap between them. Figure 3.5 illustrates the potential difference $d\varphi$ at the infinitesimal gap $\overline{u}$ and shows the possibilities of superposing numerous boundary conditions to realize versatile boundary conditions.

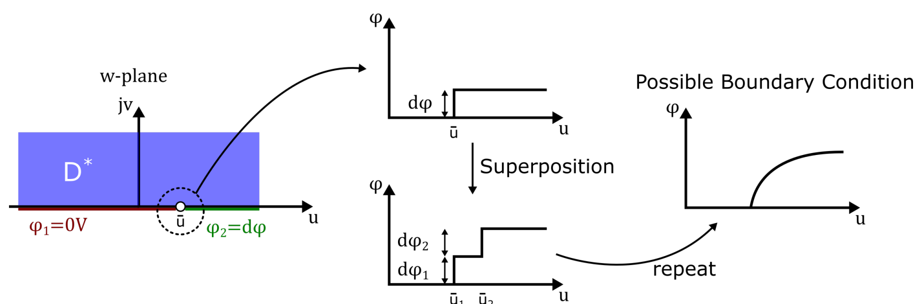

Figure 3.5: Applied boundary conditions in w-plane φ_1 and φ_2 with an infinitesimal gap in between at $u = \overline{u}$. With the help of superposition of many $d\varphi$ at different positions $\overline{u}$, versatile boundary conditions are implementable.

The single vertex approach describes the complex potential solution $\tilde{F}$ in the desired domain D^* for the simplest case of a potential difference $d\varphi$ in one point $\overline{u}$ [53]

$$\tilde{F} = \tilde{\Phi} + j\tilde{\Psi} = d\varphi + j\frac{d\varphi}{\pi}\ln(w^* - \overline{u}). \tag{3.32}$$

Hereby the electric field component $d\vec{E}$ caused by the potential difference $d\varphi$ is described by the imaginary part of the complex potential $\tilde{F}$:

$$d\vec{E}(w) = j\frac{d\varphi}{\pi}\ln(w^* - \overline{u}). \tag{3.33}$$

Note that w^* describes the complex conjugated coordinate of a point in D^* domain in w-plane. The link to z-plane coordinates is given by scaling the absolute values of the electric field with the absolute differential value of the mapping function (3.16)

$$d|\vec{E}|(z) = \left|\frac{dw}{dz}\right| \cdot \left|\frac{d\varphi}{\pi}\ln(w^* - \overline{u})\right|, \tag{3.34}$$

with $\left|\frac{dw}{dz}\right| = \left|\frac{dz}{dw}\right|^{-1}$. For an increasing amount of potential differences $d\varphi$ at different positions on the u-axis $\overline{u}$ with an infinitesimal distance between these points $d\overline{u}$ the potential difference can be written as

$$d\varphi = \left.\frac{\partial\varphi(u)}{\partial u}\right|_{\overline{u}}. \tag{3.35}$$

At this point the electric field at any position within domain D^* can be calculated by integrating the electric field derivative over the potential change on the u-axis

$$\left|\vec{E}\right|(z) = \frac{1}{\pi}\left|\frac{dw}{dz}\right|\left|\int_{-\infty}^{+\infty}\frac{1}{w^* - \overline{u}}\left.\frac{\partial\varphi(u)}{\partial u}\right|_{\overline{u}}\, d\overline{u}\right|. \tag{3.36}$$

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CHAPTER 4

Electrostatic Model

With the fundamental basics given in chapter 2 and especially in chapter 3, now the development of the TFET's electrostatic model stands in focus. All following calculations of the tunneling probability and device current require an accurate solution of the potential and electric field, not only within the channel region of the device, but also in the source and drain extensions.

4.1 Overview

In the beginning of this chapter, an overview of the single calculation segments seems appropriate, due to the superposition of several potential solutions in different device regions with versatile boundary conditions. There are some requirements for the electrostatics model that have to be met. Closed form expressions for the potential in source, channel and drain region are needed to properly model hetero structure TFETs, thereby it is important that there are no constant boundary conditions at the channel junctions (overestimation of the current in channel mid) but a parabolic condition which reflects the smaller gate influence on a deeper channel region. The same is expected on the other ends of the channel junctions, the source/drain potential extensions. Figure 4.1 illustrates these requirements. A continuous potential solution in source, channel and drain region (smooth black line) with parabolic boundaries at the channel junctions (blue and red line). To achieve this result, the potential solution is separated in six parts in section 4.3 plus one additional model to implement Gaussian-shaped doping profiles at the channel junctions in section 4.4.3. Four of those six parts are needed for the calculation of the channel potential, which is split into two source-related and two drain-related solutions. These are again split in solutions with constant (section 4.4.1.1) and parabolic boundary conditions (section 4.4.1.3). The source/drain potential extensions are introduced in section 4.4.2. Based on the device's potential solution, the band-structure is estimated in section 4.5. The electric field is obtained for the channel region of the device in section 4.6.

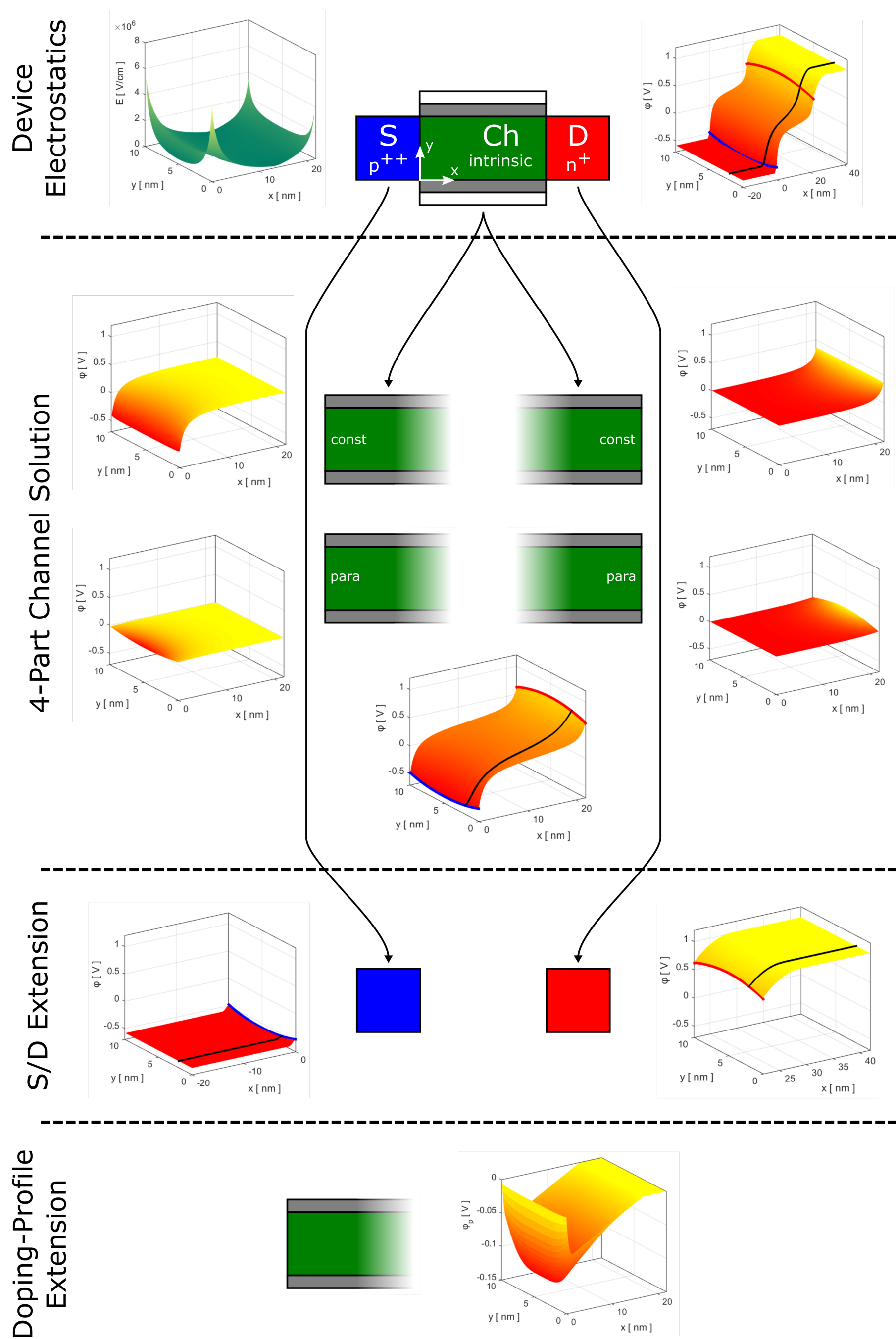

Figure 4.1: Composition of the device's potential solution including the 4-part channel potential with constant and parabolic boundary conditions for source- and drain-related cases respectively as well as source/drain extensions. E-field solution for the channel region. Additional potential adjustment to consider Gaussian-shaped doping profiles at the channel junctions.

4.2 Preliminary Considerations

Some preliminaries are made to keep mathematics as simple as possible. The intrinsic channel of the TFET allows the consideration of the absence of channel charges. In a first step the inversion and depletion charges are neglected as well which leads to the simplification of Poisson's equation (3.2) to Laplace's equation (3.6) [55]:

$$\Delta\varphi \approx 0. \tag{4.1}$$

The second simplification relates to the discontinuity of the electric field caused by the gate insulator. This discontinuity can be neglected by scaling the insulator thickness according to the relation of the permittivity of the insulator ϵ_{in} and the permittivity of the channel material ϵ_{ch}. The discontinuity in electric field at the insulator/channel interface ($E_0 = const$) has to be avoided, with [55]

$$D_{in} = \epsilon_0 \epsilon_{ch} \cdot E_0 = \epsilon_0 \epsilon_{in} \cdot E_{in} = \epsilon_0 \epsilon_{in} \cdot \frac{V_{in}}{t_{in}}. \tag{4.2}$$

D_{in} stands for the dielectric displacement and V_{in} is the voltage drop over the insulator. By scaling t_{in} to

$$\tilde{t}_{in} = \frac{\epsilon_{ch}}{\epsilon_{in}} \cdot t_{in} \tag{4.3}$$

the electric field E_0 has no discontinuity

$$D_{in} = \epsilon_0 \epsilon_{ch} \cdot E_0 = \epsilon_0 \epsilon_{ch} \cdot \frac{V_{in}}{\tilde{t}_{in}}. \tag{4.4}$$

The next assumption is linked to the Fermi-level near the channel junctions. Since tunneling takes place within the first few nanometers at the channel junctions and the Fermi level is almost constant in that region, the simplification of a constant Fermi-level near the channel junctions is made. This assumption affects the calculation of the carrier distributions in the channel region of the device.

Since the device's electric field is calculated within the channel region, the Richardson constant (A^*) for the current calculation is replaced with [35]

$$A^* = \frac{\mu_{n/p} \cdot N_{C/V} \cdot q \cdot |E|}{T^2}, \tag{4.5}$$

with electron/hole mobility $\mu_{n/p}$, effective density of states in conduction/valence band $N_{C/V}$ and the temperature T.

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4.3 Boundary Conditions

In this section the boundary conditions for the different parts of the potential solution are introduced. Figure 4.2 illustrates the boundary conditions and their decomposition of an n-TFET with the applied voltages V_g, V_s and V_d. A direct solution of the channel potential with applied parabolic boundaries on both junctions plus the gate voltages is mathematically too complex, hence the calculation has to be simplified. As mentioned before in section 3.1 the potential solution is a harmonic function and fulfills the Laplace's equation. With that the method of superposition is possible. Therefore, the boundary conditions of the channel region can be decomposed to simplify the potential solution. This is done in a way, that two infinitely expanding regions for the channel are created, a source-related (fig. 4.2 (a,c)) and drain-related region (fig. 4.2 (b,d)). The parabolic boundary condition at the source/channel interface, is then again separated in a constant boundary (fig. 4.2 (a)) and a parabolic boundary (fig. 4.2 (c)). The same is the case in the drain-related region (fig. 4.2 (b,d)). One difference for the constant boundaries in source- and drain-related case is visible. Since the gate potential is applied in fig. 4.2 (a), the potential in $x = \infty$ equals the gate voltage V_g. If the different potential solutions are now superposed V_g would appear on the drain-side of the channel if it is not subtracted beforehand like in fig. 4.2 (b). The built-in potentials at source and drain can be calculated with the help of the intrinsic band structure parameters

$$\Phi_{bi}^{s} = -\left(-V_s + E_s + \frac{E_{g0}^{s}}{2}\right), \quad (4.6)$$

$$\Phi_{bi}^{d} = -\left(-V_d + E_d - \frac{E_{g0}^{d}}{2}\right), \quad (4.7)$$

with the degeneration $E_{s/d}$ and the intrinsic band-gap $E_{g0}^{s/d}$ in source/drain. The built-in potentials at source and drain serve as one part of the boundary conditions for the source/drain potential extension in section 4.4.2.
Regarding the boundaries of the channel region, a more complex approach is needed, for which four potential points have to be calculated accurately: $\varphi(0,0)$, $\varphi(0,{}^{t_{ch}}/_{2})$, $\varphi(l_{ch},0)$ and $\varphi(l_{ch},{}^{t_{ch}}/_{2})$, whereby $\varphi(0,0)$ and $\varphi(l_{ch},0)$ are directly used for the source/drain-related potential solutions for a constant boundary (fig. 4.2 (a,b)).

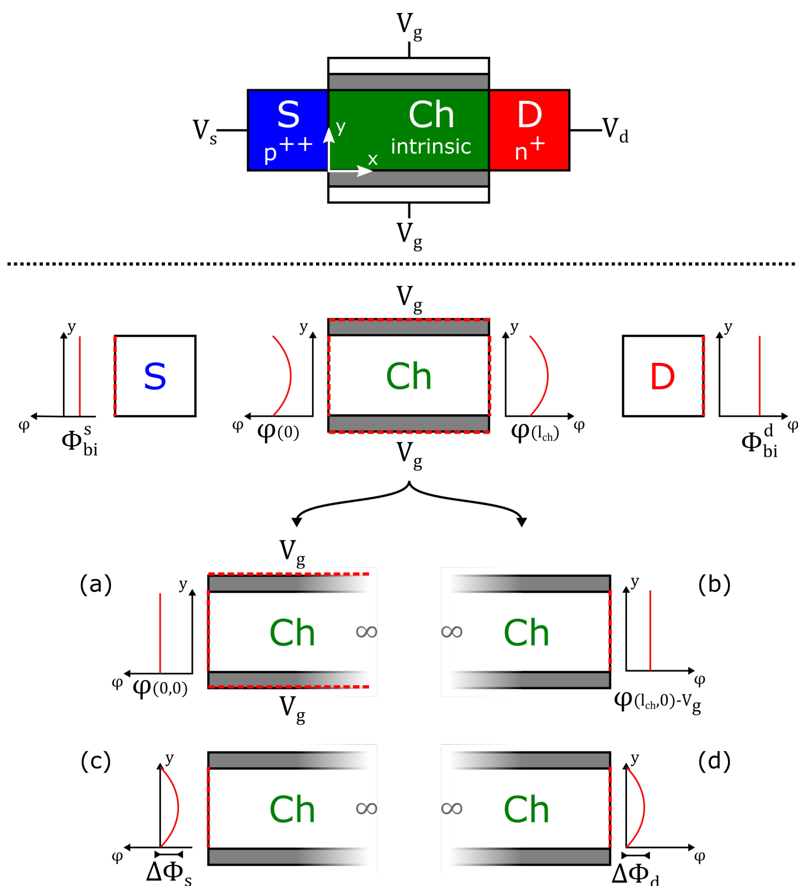

Figure 4.2: Boundary conditions of an n-TFET with built-in potential at source Φ_{bi}^{s} and drain Φ_{bi}^{d} side with the applied voltages V_g, V_s and V_d. The channel region including parabolic boundaries is decomposed into two source-sided cases (a,c) and two drain-sided cases (b,d), with two constant boundary conditions (a,b) and two solutions with parabolic boundaries (c,d).

The potential distribution at the source/channel junction of the device $\varphi(0,y)$ can be calculated using the screening length $\lambda(y)$ from equation (2.20) with an effective built-in potential model introduced in [57]. In a first step, the long-channel potential at the surface φ_{sp} is calculated

$$\varphi_{sp} = -(V_g - V_{fb} - V_{in}), \tag{4.8}$$

with the flat-band voltage V_{fb} and the voltage drop over the insulator V_{in}, given with

$$V_{in} = \frac{q \cdot N_{ch} \cdot t_{ch} \cdot t_{in}}{2 \cdot \epsilon_{in}}. \tag{4.9}$$

N_{ch} represents the doping concentration within the channel region. Based on equations (2.20), (4.6) and (4.8) the source/channel junction potential $\varphi(0,y)$ can be calculated [57]

$$\varphi(0,y) = \Phi_{bi}^{s} + (\Phi_{bi}^{s} - \varphi_{sp}) + \lambda(y)^2 \cdot \frac{qN_s}{\epsilon_s}\left(1 + \sqrt{1 + \frac{2(\Phi_{bi}^{s} + V_s - \varphi_{sp})}{\lambda(y)^2 \frac{qN_s}{\epsilon_s}}}\right) \tag{4.10}$$

At the drain/channel interface the junction potential $\varphi(l_{ch},y)$ can be calculated based on equations (2.20), (4.7) and (4.8) [57]

$$\varphi(l_{ch},y) = \Phi_{bi}^{d} - \left[(\Phi_{bi}^{d} - \varphi_{sp}) + \lambda(y)^2 \cdot \frac{qN_d}{\epsilon_d}\left(1 + \sqrt{1 + \frac{2(\Phi_{bi}^{d} + V_d - \varphi_{sp})}{\lambda(y)^2 \frac{qN_d}{\epsilon_d}}}\right)\right]. \tag{4.11}$$

The delta potentials $\Delta\Phi_{s/d}$ for the parabolic boundaries (fig. 4.2 (c,d)) are calculated with the four potential points:

$$\Delta\Phi_s = \varphi(0,0) - \varphi\left(0,\frac{t_{ch}}{2}\right) \tag{4.12}$$

$$\Delta\Phi_d = \varphi\left(l_{ch},\frac{t_{ch}}{2}\right) - \varphi(l_{ch},0) \tag{4.13}$$

4.4 Electrostatic Potential

With all boundary conditions described in section 4.3, the different potential solutions in all regions of the device are calculated in this section. Starting with the 2D source- and drain-related channel potential for constant boundary (sec. 4.4.1.1), linear boundary (sec. 4.4.1.2 and parabolic boundary conditions (sec. 4.4.1.3). Following with the potential extensions in source and drain (sec. 4.4.2). The last adjustment of the potential due to doping profiles at the channel junctions is calculated in section 4.4.3. Based on these solutions the band-structure is evaluated later on in section 4.5.

4.4.1 Channel Potential...

Within this section the potential solution of the decomposed channel structure is explained and calculated. After the decomposition in source- and drain-related case for constant and parabolic boundaries in section 4.3, the separated structures are conformally mapped as explained in section 3.3.2. The potential is firstly solved with constant boundary conditions φ_{const} in section 4.4.1.1, then follows the solution for linear boundaries over the gate insulator φ_{lin} in section 4.4.1.2 and at last the solution for parabolic boundaries φ_{para} in section 4.4.1.3. The general approach is to apply Poisson's integral from equation (3.28) for the different boundary conditions to obtain a closed form expression for the potential. When all solutions are obtained, they can be superposed to the closed form 2D channel potential solution

$$\varphi_{ch} = \varphi_{const} + \varphi_{lin} + \varphi_{para}. \tag{4.14}$$

After mapping all important points of the structure in section 3.3.2, where the boundary conditions are changing, these points are used as integration borders in the Poisson integral (3.28) with a defined boundary condition between them. Depending on the boundary condition, different potential solutions are obtained.

4.4.1.1 ...for a Constant Boundary

Constant boundary conditions can be expected if a single voltage is applied to one of the electrodes of the device (like V_g at the gate). However, they also can be a part of a more complex boundary, like the constant part of another function (offset of a parabola). All constant boundaries within the TFET are shown in figure 4.2.

For a constant boundary condition Φ_{const} between two points on the u-axis in w-plane, $\overline{u}_a$ and $\overline{u}_b$, the Poisson integral (3.28) is reduced to

$$\varphi_{const}(w(x,y)) = \frac{1}{\pi} \int_{\overline{u}_a}^{\overline{u}_b} \frac{v}{(u-\overline{u})^2 + v^2} \Phi_{const} \, d\overline{u} = -\frac{\Phi_{const}}{\pi} \tan^{-1} \left(\frac{u - \overline{u}}{v} \right) \Bigg|_{\overline{u}_a}^{\overline{u}_b} . \tag{4.15}$$

with a direct link to z-plane through the transformation function $w(z)$. This calculation is done for all applied constant boundaries shown in table 4.1.

Table 4.1: Potential solutions φ_{const} for applied constant boundaries Φ_{const} between two points on the u-axis $\overline{u}_a$ and $\overline{u}_b$.

Potential	Φ_{const}	$\overline{u}_a$	$\overline{u}_b$
φ_{const}^{g1}	V_g	$u_1{}'$	u_2
φ_{const}^{g2}	V_g	u_5	$u_1{}''$
φ_{const}^{s}	$\varphi(0,0)$	u_3	u_4
φ_{const}^{d}	$\varphi(l_{ch},0) - V_g$	u_3	u_4

The different solutions for constant boundaries are superposed, forming the first part of the 2D channel potential from equation (4.14)

$$\varphi_{const} = \varphi_{const}^{g1} + \varphi_{const}^{g2} + \varphi_{const}^{s} + \varphi_{const}^{d}. \tag{4.16}$$

4.4.1.2 ...for a Linear Boundary

A linear potential drop appears at the insulators of the device, hence a potential solution has to be obtained for linear boundaries as well. They appear between points 2/3 and 4/5 in the original structure (see fig. 3.4). For a linear potential drop over the insulator, the electric field E_{in} is constant and the potential can be described with $\Phi_{lin} = E_{in} \cdot y$ in z-plane. Mapping this boundary condition leads to $\varphi(\overline{u}) = E_{in} \frac{t_{dev}}{\pi} \cosh^{-1}(\overline{u})$. There is no closed form solution of the Poisson integral with this boundary, so the $\cosh^{-1}$ function is approximated with a square root [56]

$$E_{in} \frac{t_{dev}}{\pi} \cdot \cosh^{-1}(\overline{u}) \approx \pm\sqrt{\frac{\overline{u}-b}{a}}, \tag{4.17}$$

which leads to the integral with a closed form solution

$$\varphi_{lin}(w(z)) = \frac{1}{\pi} \int_{\overline{u}_a}^{\overline{u}_b} \frac{v}{(u-\overline{u})^2 + v^2} \pm \sqrt{\frac{\overline{u}-b}{a}}\, d\overline{u}. \tag{4.18}$$

The potential is solved for the linear boundaries listed in table 4.2. The different solutions for

Table 4.2: Potential solutions φ_{lin} for applied linear boundaries Φ_{lin} between two points on the u-axis $\overline{u}_a$ and $\overline{u}_b$.

Potential	Φ_{lin}	$\overline{u}_a$	$\overline{u}_b$
φ_{lin}^{s1}	$\frac{V_g - \varphi(0{,}0)}{t_{in}} \cdot y + \varphi(0{,}0)$	u_4	u_5
φ_{lin}^{s2}	$\frac{\varphi(0{,}0) - V_g}{t_{in}} \cdot y + \varphi(0{,}0)$	u_2	u_3
φ_{lin}^{d1}	$\frac{\varphi(l_{ch}{,}0)}{t_{in}} \cdot y + \varphi(l_{ch}{,}0)$	u_2	u_3
φ_{lin}^{d2}	$-\frac{\varphi(l_{ch}{,}0)}{t_{in}} \cdot (y - t_{ch}) + \varphi(l_{ch}{,}0)$	u_4	u_5

linear boundaries are superposed, forming the second part of the 2D channel potential from equation (4.14)

$$\varphi_{lin} = \varphi_{lin}^{s1} + \varphi_{lin}^{s2} + \varphi_{lin}^{d1} + \varphi_{lin}^{d2}. \tag{4.19}$$

4.4.1.3 ...for a Parabolic Boundary

Parabolic boundaries occur due to the decreasing electrostatic influence of the gate-electrode on deeper channel regions at the channel interfaces. They have to be modeled accurately to not overestimate the device current in later calculations. Figure 4.2 shows the applied parabolic boundaries for source- and drain-related case. The potential solution for this kind of boundary is adapted from [58] and is valid for $t_{ch} << l_{ch}$. In w-plane the parabola is approximated using

an elliptical shaped function [58]

$$\varphi(\overline{u}) = \Delta\Phi \cdot \sqrt{1-\overline{u}^2}. \tag{4.20}$$

Then the Poisson integral reads as

$$\varphi_{para}(w(x,y)) = \frac{1}{\pi}\int_{\overline{u}_a}^{\overline{u}_b} \frac{v}{(u-\overline{u})^2+v^2}\Delta\Phi \cdot \sqrt{1-\overline{u}^2}\, d\overline{u} \tag{4.21}$$

and can be solved to

$$\varphi_{para}(w(x,y)) = \Delta\Phi\left[\frac{1}{2}\left(\sqrt{1-(u-jv)^2}+\sqrt{1-(u+jv)^2}\right)-v\right]. \tag{4.22}$$

This solution is applied for source- and drain-related case as shown in table 4.3.

Table 4.3: Potential solutions φ_{para} for applied parabolic boundaries $\Delta\Phi$ between two points on the u-axis $\overline{u}_a$ and $\overline{u}_b$.

Potential	$\Delta\Phi$	$\overline{u}_a$	$\overline{u}_b$
φ^s_{para}	$\varphi(0,0)-\varphi(0,{}^{t_{ch}}\!/2)$	u_3	u_4
φ^d_{para}	$\varphi(l_{ch},{}^{t_{ch}}\!/2)-\varphi(l_{ch},0)$	u_2	u_3

The two solutions for parabolic boundaries are superposed, forming the last part of the 2D channel potential from equation (4.14)

$$\varphi_{para} = \varphi^s_{para} + \varphi^d_{para}. \tag{4.23}$$

With that, the 2D channel potential is complete, and the calculations for the source/drain potential extensions begin.

4.4.2 Source/Drain Potential Extension

The potential extensions in source and drain area of the TFET are one of the most important modeling parts. Only with them, an exact tunneling distance can be calculated and they provide the possibility to model hetero-junction devices. Depending on the applied biases, the potential drop in source and drain region can easily reach up to 0.5 V. This impact has to be modeled as accurately as possible. In [59] a model is introduced, which satisfies all these requirements and hence, is adapted to the TFET.

Firstly, the calculations are done in the source region of the device and then transferred to obtain the drain potential. Basically, the potential solution is build up on two parabolas along the x-direction at the surface $\varphi_s(x,0)$ and the middle of the source region $\varphi_s(x,{}^{t_{ch}}\!/2)$. Figure 4.3

illustrates these two parabolas in green and blue. They are used to model several parabolas in y-direction, forming the source potential extension.

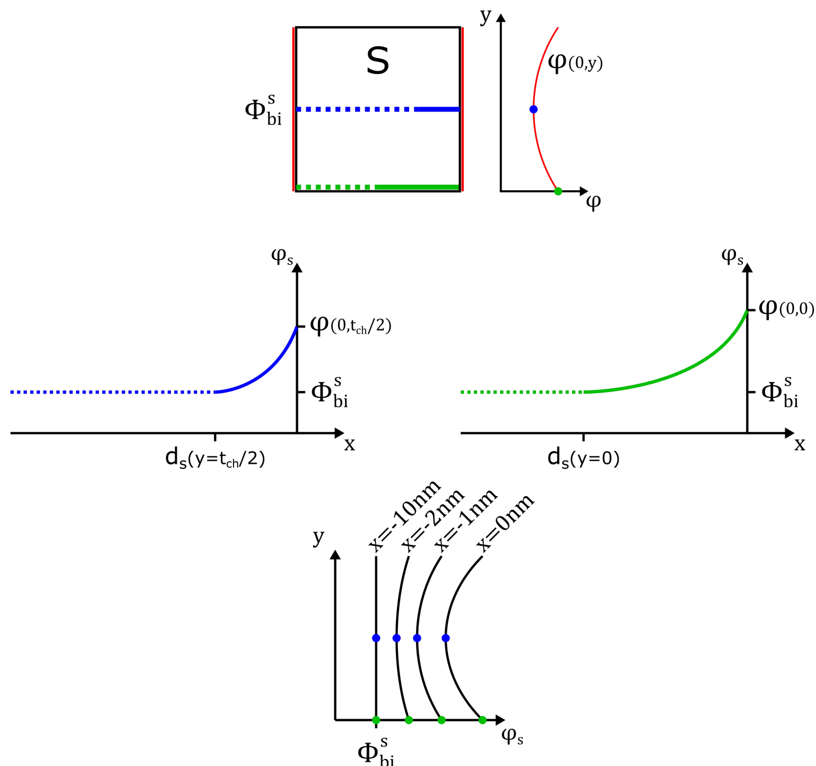

Figure 4.3: Calculation of the source potential extension based on two parabolas in x-direction. Scheme of parabolic potential modeling in y-direction at different positions x.

The first step is the calculation of the potential bending distance in source d_s and drain region d_d. In [59] an equation for an effective built-in potential model is introduced

$$-\frac{qN_{s/d}}{2\epsilon_{s/d}}d_{s/d}^2 - \frac{qN_{s/d}\lambda}{\epsilon_{s/d}}d_{s/d} + \Phi_{bi}^{s/d} - \varphi_{lc} + V_{s/d} = 0, \tag{4.24}$$

which can be solved for $d_{s/d}$

$$d_s = -\lambda + \sqrt{\lambda^2 + \frac{(\Phi_{bi}^s - \varphi_{sp} + V_s)2\varepsilon_s}{qN_s}} \tag{4.25}$$

and

$$d_d = -\lambda + \sqrt{\lambda^2 + \frac{(\Phi_{bi}^d - \varphi_{sp} + V_d)2\varepsilon_d}{qN_d}}, \tag{4.26}$$

with the screening length λ from equation (2.20) and the long channel surface potential φ_{sp} from equation (4.8). With the distances $d_{s/d}$, the built-in potentials $\Phi_{bi}^{s/d}$ and the potentials

at the channel junctions $\varphi_j^s = \varphi(0,y)$ and $\varphi_j^d = \varphi(l_{ch},y)$, the general parabolic equations in x-direction can be described by

$$\varphi_s^x(x,y) = \frac{\varphi_j^s(y) - \Phi_{bi}^s}{d_s^2(y)} \cdot (x - d_s(y))^2 + \Phi_{bi}^s, \tag{4.27}$$

$$\varphi_d^x(x,y) = \frac{\varphi_j^d(y) - \Phi_{bi}^d}{d_d^2(y)} \cdot (x - (l_{ch} + d_d)(y))^2 + \Phi_{bi}^d. \tag{4.28}$$

For $-l_{sd} \leq x < d_s(y)$ the potential in source region is given with $\varphi_s = \Phi_{bi}^s$ and for $d_s(y) \leq x < 0$ stands

$$\varphi_s(x,y) = \frac{\varphi_s^x(x,0) - \varphi_s^x(x,{}^{t_{ch}}/_2)}{{}^{t_{ch}}/_2{}^2} \cdot (y - {}^{t_{ch}}/_2)^2 + \varphi_s^x(x,{}^{t_{ch}}/_2). \tag{4.29}$$

For $(l_{ch} + d_d(y)) \leq x < (2l_{sd} + l_{ch})$ the potential in drain region is given with $\varphi_d = \Phi_{bi}^d$ and for $l_{ch} \leq x < (l_{ch} + d_d(y))$ stands

$$\varphi_d(x,y) = \frac{\varphi_d^x(x,0) - \varphi_d^x(x,{}^{t_{ch}}/_2)}{{}^{t_{ch}}/_2{}^2} \cdot (y - {}^{t_{ch}}/_2)^2 + \varphi_d^x(x,{}^{t_{ch}}/_2). \tag{4.30}$$

4.4.3 Doping-Profile-Based Potential Adjustment

For a high on-current an abrupt doping profile at the source tunneling barrier is necessary but technologically difficult to achieve. Therefore, a model is introduced, which captures the impact of the doping profile steepness on the electrostatics and hence, the device current. The basic idea is to calculate a potential difference of an abrupt and non-abrupt profile at the tunneling barrier, in order to adjust the ideal potential solution afterwards. Therefore, the additional channel charges from the dopants are included into Poisson's equation.
The definition of the doping profiles is already done in section 2.2.4. By considering the given boundary conditions expressions for the potential change and the associated electric field have been found. The resulting parameters from the idealized 1D calculations are adjusted based on an extensive simulation analysis to include 2D effects. In the following steps, the derivation of the model is focused on the doping profile at the source/channel junction of the device. The results are easily transferable to the drain side.

The first step is the definition of a doping profile for the simulation, which is set to a realistic Gaussian shaped type (see fig. 4.4 a)). In the model the doping profile is assumed to be linear, depending on the parameter a (see fig. 4.4 a)). The delta doping of donators in source N_p is shown in fig. 4.4 b) and can be described for $0 \leq x \leq a$ through

$$N_p(0 \leq x \leq a) = N_{lin} - N_{ideal} = N_s^0 \cdot \frac{a - x}{a}. \tag{4.31}$$

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Two-Dimensional Analytical Modeling of Tunnel-FETs
Michael Gräf

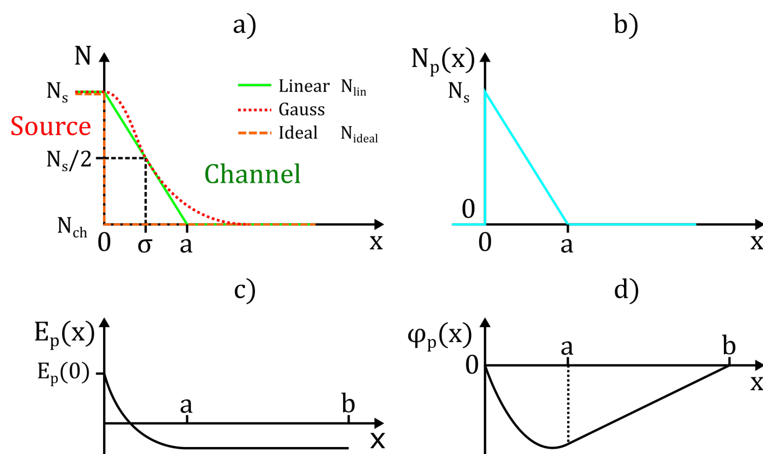

Figure 4.4: a) Gaussian-shaped (red dots), linear N_{lin} (green line) and ideal doping profile N_{ideal} (orange dashed line) at the source/channel junction, showing the standard deviation σ and model parameters a, b. b) Delta doping profile $N_p = N_{lin} - N_{ideal}$, describing the difference between an linear- and the ideal doping profile c) Schematic change of the electric field E_p due to additional charges in the channel region. d) Schematic potential difference φ_p calculated by the model.

In order to find the potential solution, Poisson's equation is decomposed to

$$\Delta\tilde{\varphi} = -\frac{\varrho(x)}{\varepsilon} = \Delta\varphi_{ideal} + \Delta\varphi_p, \tag{4.32}$$

with the potential for a non-ideal ($\tilde{\varphi}$) and ideal (φ_{ideal}) doping profile, note that Δ stands for the Laplace operator. The potential difference is given with $\varphi_p = \tilde{\varphi} - \varphi_{ideal}$. Figure 4.5 shows the decomposition of the potential distribution for the non-ideal doping profile.

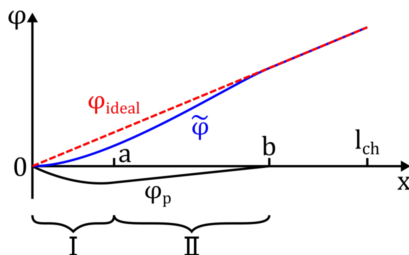

Figure 4.5: Decomposition of the potential for non-ideal doping profiles $\tilde{\varphi}$ into ideal φ_{ideal} and delta potential φ_p, showing intervals for model derivation.

The potential difference originates from the additional dopants within the channel and can be described through

$$\Delta\varphi_p = -q \cdot \frac{N_p(x)}{\varepsilon}, \tag{4.33}$$

with the linear delta doping profile N_p from equation (4.31). In the next step, the boundary

conditions are defined in order to calculate the potential and electric field differences. The potential difference has to be zero at the junction, and at a certain point within the channel region b (see fig. 4.4 d))

$$\varphi_p(0) = 0, \quad (4.34)$$

$$\varphi_p(b) = 0. \quad (4.35)$$

Furthermore, φ_p is continuous and has a smooth transition between interval I and II (see fig. 4.5). The electric field is considered constant in interval II (see fig. 4.5 c))

$$\varphi_{pI}(a) = \varphi_{pII}(a), \quad (4.36)$$

$$E_{pI}(a) = E_{pII}. \quad (4.37)$$

For solving Poisson's equation in interval I the electric field change is calculated

$$-E_{pI}(x) = \frac{d\varphi_p(x)}{dx} = -\frac{q \cdot N_s}{\varepsilon \cdot a}\left(a \cdot x - \frac{x^2}{2}\right) + E_p(0), \quad (4.38)$$

with the electric field offset value $E_p(0)$. In interval II the doping difference is $N_p(x) = 0$. Therefore, stands

$$-E_{pII}(x) = \frac{d\varphi_p(x)}{dx} = -E_{pI}(a). \quad (4.39)$$

The Poisson's equation can be solved, assuming the electric field and the potential to be continuous over the channel length. Therefore, the potential difference in interval I (see fig. 4.4 d)) is given through

$$\varphi_p(x) = -\frac{q \cdot N_s}{\varepsilon \cdot a}\left(\frac{a}{2} \cdot x^2 - \frac{1}{6} \cdot x^3\right) + E_p(0) \cdot x \quad (4.40)$$

and in interval II a linear potential drop can be calculated with

$$\varphi_p(x) = \varphi(a) - \left(\frac{q \cdot N_s}{2 \cdot \varepsilon} \cdot a - E_p(0)\right)(x - a). \quad (4.41)$$

The electric field at $x = 0$ can be evaluated by applying the boundary conditions mentioned in equations (4.34) to (4.37):

$$E_p(0) = q \cdot N_s/(\varepsilon \cdot b) \cdot (ab/2 - a^2/6). \quad (4.42)$$

Due to the 2D influence of the gate electrode on the channel region the closer the additional dopants N_p are to the gate insulator, the more they are gate-controlled. An extensive TFET simulation analysis showed, that this effect can be captured by coupling parameter a with the doping profile standard deviation σ and the position y in the channel [60]:

$$a \approx -\frac{\sigma \cdot (c_1 - 1)}{(t_{ch}/2)^4} \cdot (y - t/2)^4 + c_1 \cdot \sigma, \quad (4.43)$$

with $1 < c_1 < 1.5$. The analysis also revealed a dependency of the channel and insulator thickness on b

$$b \approx t_{ch} \cdot \pi/4 + \tilde{t}_{in}, \tag{4.44}$$

with the scaled insulator thickness $\tilde{t}_{in}$ from equation (4.3). Additionally, to the idealized calculations a shifting of φ_p is needed in order to capture the existing potential drop in source region. Therefore, stands

$$\varphi_p(x) = \varphi_p(x - x_{shift}). \tag{4.45}$$

The doping profile at drain region φ_n can be captured by substituting N_s with N_d and mirroring at $x = {}^{l_{ch}}/_{2}$

$$\varphi_n(x) = \varphi_p(l_{ch} - x) \ \big|_{N_s = N_d}. \tag{4.46}$$

The overall device potential φ can now be put together with different solutions for the channel potential from section 4.4.1, the source and drain potential extension from section 4.4.2 and doping-profile-based potential adjustment from this section

$$\varphi = (\varphi_s + \varphi_{ch} + \varphi_d) + \varphi_p + \varphi_n. \tag{4.47}$$

At this point the electrostatic potential for the whole device is complete and includes 2D effects, as well as doping profiles at the channel junctions. The next step is the calculation of the band-structure in section 4.5.

4.5 Band-Structure

The band-structure of the device is needed to properly calculate the tunneling probability and hence, the device current. Especially for hetero-junction devices it is important to consider the band structure, since here kinks may occur due to different material dependent parameters. For the calculation, the potential solution from section 4.4 forms the basis. With the material dependent parameters: electron affinity X, band-gap E_g including bgn and the intrinsic band-gap E_g^0 for each region, the band structure can be calculated. At this point, it is necessary to consider band-gap narrowing, since source and drain region are heavily doped. If the doping density exceeds a specific limit, the dopants have influence on the band-gap of a semiconductor depending on the semiconductor material, doping element and doping concentration. The implemented bgn models are introduced in section 2.2.6.
With the given potential φ of the device the valence band E_v and conduction band E_c in each region is calculated (see fig. 4.6).

$$
\begin{aligned}
E_v^s &= -\varphi - {}^{E^0_{g,s}}/_2 \;\Big|_{-l_{sd}<x<0} \\
E_c^s &= E_{v,s} + E_{g,s} \;\Big|_{-l_{sd}<x<0} \\
E_v^{ch} &= -\varphi + X_s - X_{ch} - {}^{E^0_{g,ch}}/_2 \;\Big|_{0<x<l_{ch}} \\
E_c^{ch} &= E_{v,ch} + E_{g,ch} \;\Big|_{0<x<l_{ch}} \\
E_c^d &= -\varphi + X_s - X_d + {}^{E^0_{g,d}}/_2 \;\Big|_{l_{ch}<x<(l_{ch}+l_{sd})} \\
E_v^d &= E_{c,d} - E_{g,d} \;\Big|_{l_{ch}<x<(l_{ch}+l_{sd})}
\end{aligned} \tag{4.48}
$$

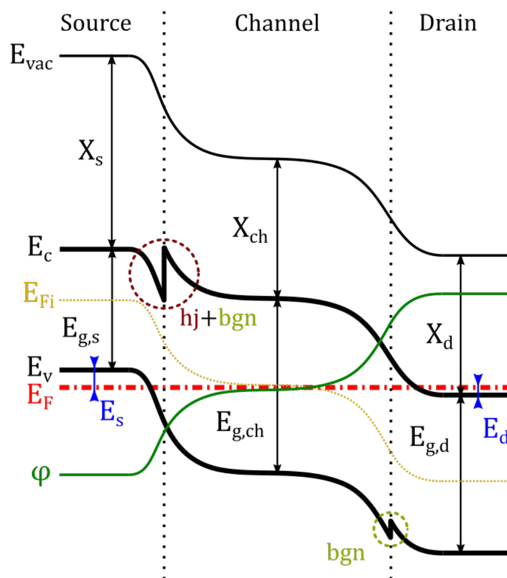

Figure 4.6: Schematic band structure of a DG n-TFET showing the potential solution φ, Fermi level E_F, intrinsic Fermi level E_{Fi}, valence band E_v, conduction band E_c, vacuum level E_{vac} and the different device parameters. A hetero-junction at the source/channel interface leads to a kink in the conduction band (+bgn). band-gap narrowing in the drain region causes the kink at the drain/channel junction.

4.6 Electric Field

This section shows the closed form calculations of the electric field, based on the single-vertex approach firstly introduced in section 3.5, which leads to an expression for the electric field based on non-constant boundary potentials in equation (3.36). There are four boundary conditions which fulfill these requirements. The linear potential boundaries over the top and bottom gate insulators for source- and drain-related case are introduced in section 4.4.1.2.

Firstly, the definition of the potential change in equation (3.36) has to be replaced with the given potential distribution within the insulator [56]

$$\left.\frac{\partial\varphi(u)}{\partial u}\right|_{\overline{u}} d\overline{u} = \frac{\partial y}{\partial \overline{u}}\frac{\partial \varphi}{\partial y} d\overline{u}, \tag{4.49}$$

whereby $\frac{\partial y}{\partial \overline{u}}$ can be replaced by using the conformal mapping function (3.24):

$$\frac{\partial y}{\partial \overline{u}} = \frac{t_{dev}}{\pi}\frac{1}{\sqrt{1-\overline{u}^2}} \tag{4.50}$$

and since the potential change over the insulator is linear a constant electric field $\vec{E}_y$ is present, which is used as boundary condition for the later calculations

$$\frac{\partial \varphi}{\partial y} = \vec{E}_y = const. \tag{4.51}$$

The integration of equation (3.36) over a linear boundary with the substitutions from (4.50) and (4.51) leads to the electric field solution [56]

$$\left|\vec{E}\right|(z) = \frac{1}{\pi}\left|\frac{dw}{dz}\right|\left|\vec{E}_y\int_{\overline{u}_a}^{\overline{u}_b}\frac{1}{w^*-\overline{u}}\frac{t_{dev}}{\pi}\frac{1}{\sqrt{1-\overline{u}^2}}\,d\overline{u}\right| = \frac{1}{\pi}\left|\frac{dw}{dz}\right|\left|\vec{E}_y\left[-\frac{t_{dev}}{\pi}\frac{C}{\sqrt{1-(w^*)^2}}\right]_{\overline{u}_a}^{\overline{u}_b}\right| \tag{4.52}$$

with

$$C = \ln\left(\frac{\sqrt{\overline{u}^2-1}+(\overline{u}\cdot w^*-1)\sqrt{\frac{1}{(w^*)^2-1}}}{\overline{u}-w^*}\right).$$

Note that w^* describes the complex conjugated coordinate of a point in D^* domain in w-plane. The electric field is solved for the linear boundaries listed in table 4.4.

The different solutions for the electric field are superposed, forming the 2D channel electric field

Table 4.4: Electric field solutions E for applied linear potential boundaries resulting in constant electric fields E_y between two points on the u-axis $\overline{u}_a$ and $\overline{u}_b$

E – Field	$\vec{E}_y$	$\overline{u}_a$	$\overline{u}_b$
$\vec{E}^{s1}$	$-\dfrac{V_g - V_{fb} - \varphi(0,t_{ch})}{\tilde{t}_{in}}$	u_4	u_5
$\vec{E}^{s2}$	$-\dfrac{V_g - V_{fb} - \varphi(0,0)}{\tilde{t}_{in}}$	u_2	u_3
$\vec{E}^{d1}$	$-\dfrac{V_g - V_{fb} - \varphi(l_{ch},t_{ch})}{\tilde{t}_{in}}$	u_2	u_3
$\vec{E}^{d2}$	$-\dfrac{V_g - V_{fb} - \varphi(l_{ch},0)}{\tilde{t}_{in}}$	u_4	u_5

$$\vec{E} = \vec{E}^{s1} + \vec{E}^{s2} + \vec{E}^{d1} + \vec{E}^{d2}. \tag{4.53}$$

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CHAPTER 5

Tunneling Probability

Based on the calculations for the device electrostatics in chapter 4 and especially the band-structure in section 4.5, this chapter deals with the estimation of the different tunneling probabilities and their pre calculations. A first introduction of the tunnel effect and the different tunneling events is given in section 2.3 and 2.4.

In the beginning of this chapter, the occurring tunneling events within the TFET are investigated in section 5.1, followed by the calculation of a quasi 2D WKB approach to estimate the tunneling probability in section 5.2. The application of this approach is done in section 5.3 for band-to-band tunneling and in section 5.4 for trap-assisted-tunneling.

5.1 Tunneling Events in Tunnel-FETs

There are four different tunneling events occurring in all different states of the TFET. It is important to know that the tunneling events are not necessarily displacing each other by passing through the states instead they are omnipresent. Single tunneling events are only predominant in a specific bias range. Figure 5.1 illustrates the predominant tunneling events for each state and indicates the omnipresence in the resulting current transfer characteristics. In the on-state the band-to-band tunneling at the source/channel interface prevails T_{b2b}^{s}. In the transition from on- to off-state, the trap-assisted-tunneling at the source side increases T_{tat}^{s}, which is then overtaken by the tat at the drain side T_{tat}^{d} in the transition from off- to the ambipolar-state. The band-to-band tunneling at the drain side T_{b2b}^{d} is predominant in the ambipolar-state.

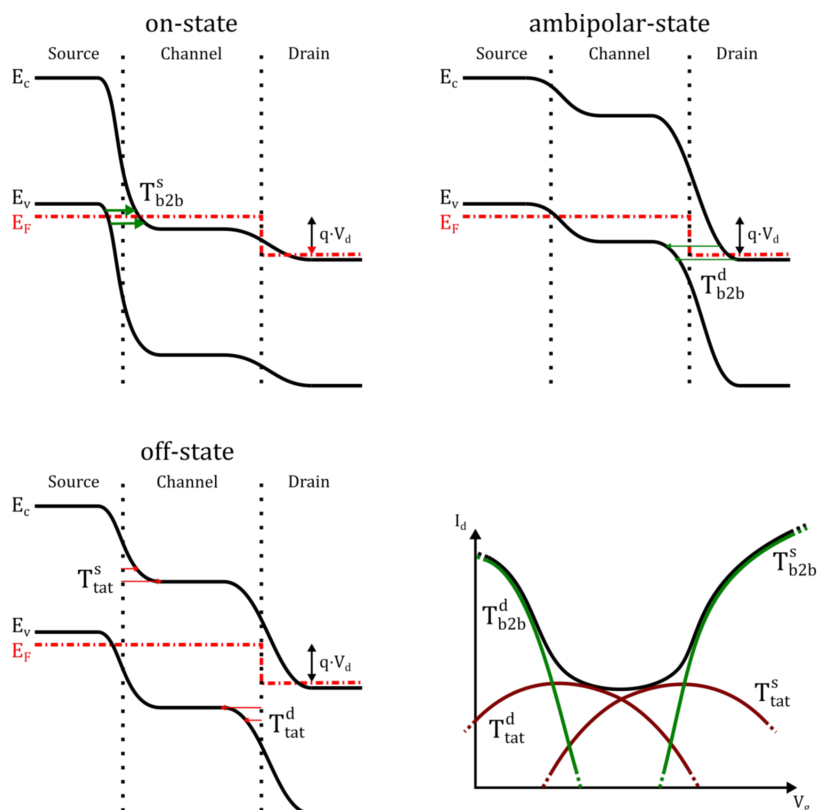

Figure 5.1: Predominant tunneling events in the three states of the TFET. T^s_{b2b} in on-state, $T^{s/d}_{tat}$ in off-state and T^d_{b2b} in ambipolar state. The omnipresence of all events is indicated in the resulting current transfer characteristics.

5.2 Quasi 2D WKB Approach

The WKB approximation is firstly introduced in section 2.3 as a method for estimating a tunneling probability through a rectangular barrier. The more complex tunneling barrier shapes within the TFET are simplified to numerous triangular problems, in order to apply the WKB approximation.

For the calculation of the tunneling probability for all different tunneling events, a general quasi 2D WKB approach is introduced. Since the WKB expression (2.27) is integrated over the barrier, some assumptions have to be made [61].

$$T \approx \exp\left(-2\int_{x_1}^{x_2}\left[\frac{2m}{\hbar^2}(U(x) - E_{car})\right]^{1/2} dx\right) \tag{5.1}$$

The calculations are firstly explained in figure 5.2 for b2b tunneling in the on-state of the device but are also valid for the other tunneling events. By considering a tunneling path from a point in source region a to a point on the same energy level in channel region b, a triangular barrier can be defined with the help of the electric field (potential slope) at point b. Thereby, the electric field is assumed to be constant over the tunneling length l_{tun}

$$U(x) = -q|\overrightarrow{E}(b)| \cdot (x-b) \tag{5.2}$$

which results in the barrier height h_{bar} at position a $U(a) = -q|\overrightarrow{E}(b)| \cdot -l_{tun} = h_{bar}$ and $U(b) = 0$. By using the electric field in the channel region to create the triangular profiles, more realistic tunneling barriers are created. If only carriers are taken into account on the same energy level as a and b, then $E_{car} = 0$ and the tunneling probability is reduced to

$$\begin{aligned} T &\approx \exp\left(-2\int_a^b \left[\frac{2m}{\hbar^2}(-q|\overrightarrow{E}(b)| \cdot (x-b))\right]^{1/2} dx\right) = \exp\left(\frac{4}{3}\frac{\sqrt{2m}}{\hbar \cdot q|\overrightarrow{E}(b)|}(q|\overrightarrow{E}(b)| \cdot (b-x))^{3/2}\Big|_a^b\right) \\ &= \exp\left(\frac{4}{3}\frac{\sqrt{2m}}{\hbar \cdot q|\overrightarrow{E}(b)|}(q|\overrightarrow{E}(b)| \cdot l_{tun})^{3/2}\right) = \exp\left(\frac{4}{3}\frac{\sqrt{2m}}{\hbar \cdot q|\overrightarrow{E}(b)|}(h_{bar})^{3/2}\right), \end{aligned} \tag{5.3}$$

with the carrier dependent effective mass $m = m_{n/p} \cdot m_0$. At this point the tunneling probability for any point in the channel region b can be calculated depending on the electric field at said point $|\overrightarrow{E}(b)|$ and the tunneling distance l_{tun}. These calculations can not only be applied at the source/channel junction to calculate ether b2b- or tat-probabilities but they are also valid at the drain/channel junction to calculate the hole tunneling probabilities. Only different expressions for the tunneling lengths have to be found.

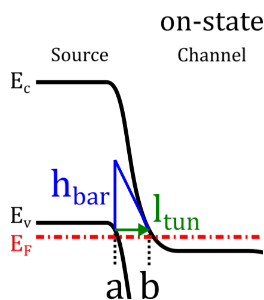

Figure 5.2: Parameters for the quasi 2D WKB approximation.

5.3 Band-to-Band Tunneling Probability

The band-to-band tunneling current is predominant in the on-state at the source/channel interface and in the ambipolar-state at the drain-channel interface. By investigating the band-structure within the channel region, it can be seen that an electron tunneling at the source junction is likely if the conduction band in the channel region overlaps with the valence band in the source region. Figure 5.3 illustrates such an overlap, starting at the position $x \geq x_{int}$.

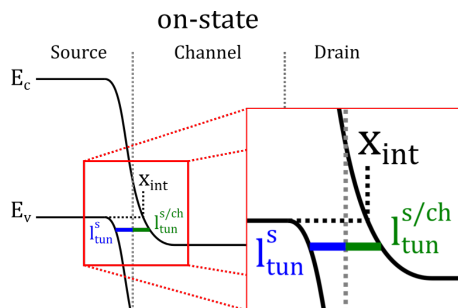

Figure 5.3: B2b tunneling length in on-state at source/channel junction.

5.3.1 Tunneling Length

In the range where b2b tunneling is possible the tunneling distance l_{tun} consists of two parts. One part in the source region l^{s}_{tun} and one part at the source side in the channel region $l^{s/ch}_{tun}$. One part of l_{tun} is already given with the x-coordinate $l^{s/ch}_{tun} = x$, the other part has to be calculated. Therefore, the valence-band energy at the far source end $E^{s}_{v}(y) = E_{v}(-l_{sd},y)$ and at the source/channel junction $E^{js}_{v}(y) = E^{ch}_{v}(0,y)$ from equation (4.48) are needed, as well as the y-depending band bending distance in source region $d_{s}(y)$ from equation (4.25). With those points a parabola for the source valence band is modeled in order to calculate the tunneling distance

$$E^{l_{tun}}_{v}(x,y) = \frac{E^{js}_{v}(y) - E^{s}_{v}}{d_{s}(y)^2} \cdot (x - d_{s}(y))^2 + E^{s}_{v}. \tag{5.4}$$

The tunneling distance in source region l^{s}_{tun} for a specific conduction band energy within the channel region E^{ch}_{c}, which has the same energy level as the valence band in the source region $E^{l_{tun}}_{v} = E^{ch}_{c}$, can be calculated with the reverse function of equation (5.4):

$$l^{s}_{tun} = d_{s} - \sqrt{(E^{ch}_{c} - E^{s}_{v}) \cdot \frac{d^2_{s}}{E^{js}_{v} - E^{s}_{v}}}. \tag{5.5}$$

By adding the missing tunneling distance in the channel $l^{s/ch}_{tun} = x$, the tunneling length for b2b tunneling in the on-state l^{on}_{b2b} is complete:

$$l_{b2b}^{on} = x + d_s - \sqrt{(E_c^{ch} - E_v^s) \cdot \frac{d_s^2}{E_v^{js} - E_v^s}}. \tag{5.6}$$

Figure 5.4 illustrates, that at the drain side, the b2b tunneling length also consists of two parts, one part in the drain region l_{tun}^{d} and one part at the drain end of the channel region $l_{tun}^{d/ch}$. Here, one part is easily calculable as well $l_{tun}^{d/ch} = l_{ch} - x$.

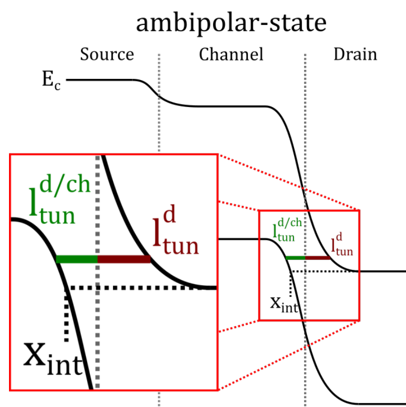

Figure 5.4: B2b tunneling length in ambipolar-state at drain/channel junction.

For the tunneling distance in drain region l_{tun}^{d}, the conduction band energy at the far drain end $E_c^d(y) = E_c(l_{ch}+l_{sd},y)$ and at the drain/channel junction $E_c^{jd}(y) = E_c^{ch}(l_{ch},y)$ from equation (4.48), as well as the band bending distance in drain region $d_d(y)$ from equation (4.26) are needed. With those points a parabola for the conduction band in drain region can be modeled for the tunneling length calculation

$$E_c^{l_{tun}}(x,y) = \frac{E_c^{jd}(y) - E_c^d}{d_d(y)^2} \cdot (x - (l_{ch} + d_d(y)))^2 + E_c^d. \tag{5.7}$$

The tunneling distance in drain region l_{tun}^{d} for a specific valence band energy within the channel region E_v^{ch}, which has the same energy level as the conduction band in the drain region $E_c^{l_{tun}} = E_v^{ch}$, can be calculated with the reverse function of equation (5.7) minus the channel length, since only the distance in drain region is needed

$$l_{tun}^{d} = d_d - \sqrt{(E_v^{ch} - E_c^d) \cdot \frac{d_d^2}{E_c^{jd} - E_c^d}}. \tag{5.8}$$

By adding the missing tunneling distance in the channel $l_{tun}^{d/ch} = l_{ch} - x$, the tunneling length for b2b tunneling in the ambipolar-state l_{b2b}^{amb} is complete:

$$l_{b2b}^{amb} = l_{ch} - x + d_d - \sqrt{(E_v^{ch} - E_c^d) \cdot \frac{d_d^2}{E_c^{jd} - E_c^d}}. \tag{5.9}$$

5.3.2 Transmission Coefficient

With the calculated tunneling lengths l_{b2b}^{on} and l_{b2b}^{amb}, the electric field in the channel region $\vec{E}$ and the general WKB equation (5.3), the band-to-band tunneling probabilities can be calculated

$$T_{b2b}^{s}(x,y) = \exp\left(\frac{4}{3}\frac{\sqrt{2 \cdot m_n \cdot m_0}}{\hbar \cdot q|\vec{E}(x,y)|}(h_{bar}^{s})^{3/2}\right), \tag{5.10}$$

with $h_{bar}^{s} = q|\vec{E}(x,y)| \cdot l_{b2b}^{on}$ and

$$T_{b2b}^{d}(x,y) = \exp\left(\frac{4}{3}\frac{\sqrt{2 \cdot m_p \cdot m_0}}{\hbar \cdot q|\vec{E}(x,y)|}(h_{bar}^{d})^{3/2}\right), \tag{5.11}$$

with $h_{bar}^{d} = q|\vec{E}(x,y)| \cdot l_{b2b}^{amb}$.

5.3.3 Barrier Height

For almost flat bands within the channel region of the TFET, the approximation of a triangular barrier profile using the electric field results in very low barrier heights, and with that, an overestimation of the tunneling probability. Therefore, the barrier height is limited to a minimum percentage value c_{bar} of the source band-gap $h_{bar}^{s} \geq c_{bar} \cdot E_g^s$ in the on-state and at the drain region $h_{bar}^{d} = c_{bar} \cdot E_g^d$ for the ambipolar-state.

5.4 Trap-Assisted-Tunneling Probability

The trap-assisted-tunneling effect with the trap definition is firstly introduced in section 2.4.1. Figure 5.5 illustrates that, different to the band-to-band tunneling, the tat probability has to be calculated for all positions within the channel region.

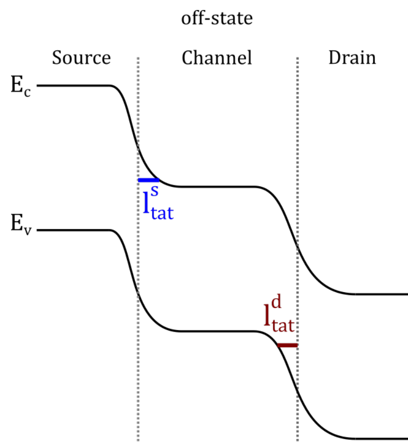

Figure 5.5: Tat tunneling lengths in off-state.

The calculations for the tat probabilities are not that complex in comparison to the band-to-band ones. Traps are considered directly at the channel junctions of the device, so the tat tunneling length at the source-side is easily given with

$$l^{s}_{tat} = x \tag{5.12}$$

and at the drain-side through

$$l^{d}_{tat} = l_{ch} - x. \tag{5.13}$$

Considering the electric field within the channel region $\vec{E}$, the tunneling carrier masses $m_{n/p}$ at source- and drain-side, as well as the tat-lengths $l^{s/d}_{tat}$, the tat probabilities can be calculated:

$$T^{s/d}_{tat}(x,y) = \exp\left(\frac{4}{3}\frac{\sqrt{2 \cdot m_{n/p} \cdot m_0}}{\hbar \cdot q|\vec{E}(x,y)|}(h^{s/d}_{bar})^{3/2}\right), \tag{5.14}$$

with $h^{s/d}_{bar} = q|\vec{E}(x,y)| \cdot l^{s/d}_{tat}$.

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CHAPTER 6

Current Calculation

The last part of the analytical model consists of the device current calculation. The tunneling-based device current forms the centerpiece of the TFET. It enables subthreshold slopes below the 60 $^{mV}/_{dec}$ limitation of the conventional thermionic based MOSFET. Thus, making it an optimal device for low-power applications. The calculation of this current, however, is not at all trivial.

Based on fundamental physics from chapter 2, the electrostatics solution from chapter 4 and the tunneling probabilities from chapter 5, the different current parts can be calculated. In the on-state of the device the b2b-current at the source/channel junction is predominant, whereas in the off-state the tat-current at both channel junctions is superior. In the ambipolar state, the b2b-current at the drain/channel junction succeeds. For each current part a different calculation is valid and explained in this chapter.

6.1 Band-to-Band Tunneling Current

The calculations for the b2b tunneling currents are separated in two parts. The first one is the on-state b2b current at the source/channel junction I_{on}^{b2b} and the second one, the b2b current in ambipolar-state at the drain/channel junction I_{amb}^{b2b}. In the beginning the calculations for the on-state current are explained. Both current calculations are based on Landauer's transmission theory [62], leading to a carrier gradient depending tunneling mechanism. In order to determine the carrier concentration on both sides of the barrier, the Fermi-statistics firstly introduced in section 2.2.2 are needed. Figure 6.1 illustrates the Fermi statistics in source region f_s with source-related Fermi potential [35]

$$f_s^{on}(x,y) = \frac{1}{1 + \exp[(E_c^{ch}(x,y) - E_F^s)/kT]} \tag{6.1}$$

and in channel region with the drain-related Fermi potential f_d

$$f_d^{on}(x,y) = \frac{1}{1 + \exp[(E_c^{ch}(x,y) - E_F^d)/kT]}. \tag{6.2}$$

In equation (6.1), the energy value of the conduction band in the channel region $E_c^{ch}(x,y)$ is used, since it has the same energy level as the valence band in source. With the Fermi-statistics in both regions, a drain bias depending carrier probability gradient is given, which is used for the following current calculation.

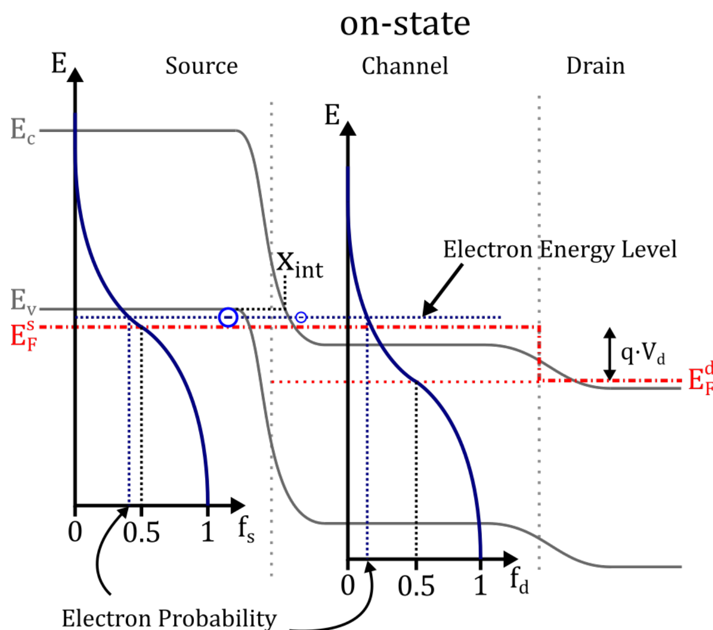

Figure 6.1: b2b current calculation based on Landauer's transmission theory, showing source- and drain-related Fermi-statistics $f_{s/d}$.

The b2b-current in the on-state at the source/channel interface can be calculated for all points within the channel region, where a b2b-tunneling is possible. The starting point of the calculations is the energy overlap of the conduction band in the channel region with the valence band in source region x_{int}, as indicated in figure 6.1. Then follows an integration over all those positions to determine the overall b2b current [62]

$$I_{b2b}^{on} = w \cdot \frac{\mu_{tun}^{n} \cdot N_V \cdot q^2}{k \cdot T} \int_{0}^{t_{ch}} \int_{x_{int}}^{l_{ch}} T_{b2b}^{s} \cdot (f_s^{on} - f_d^{on}) \cdot |\vec{E}|^2 \cdot dxdy \tag{6.3}$$

with the device width w, electron tunneling mobility μ_{tun}^n and the density of states in the valence band N_V.

The second b2b current part occurs at the drain/channel interface, when the valence band in

the channel region overlaps with the conduction band in drain region at position x_{int2}. To determine the carrier density gradient for Landauer's transmission theory, the Fermi statistics for holes in drain region with drain-related Fermi-level f_d^{amb} and for holes in channel region with source-related Fermi-level f_s^{amb} are needed:

$$f_d^{amb}(x,y) = \frac{1}{1 + \exp[(E_F^d - E_v^{ch}(x,y))/kT]}, \tag{6.4}$$

$$f_s^{amb}(x,y) = \frac{1}{1 + \exp[(E_F^s - E_v^{ch}(x,y))/kT]}. \tag{6.5}$$

Then, the b2b-current in the ambipolar-state at the drain/channel interface can be calculated [62]

$$I_{b2b}^{amb} = w \cdot \frac{\mu_{tun}^p \cdot N_c \cdot q^2}{k \cdot T} \int_0^{t_{ch}} \int_0^{x_{int2}} T_{b2b}^d \cdot (f_d^{amb} - f_s^{amb}) \cdot |\vec{E}|^2 \cdot dxdy, \tag{6.6}$$

with the hole tunneling mobility μ_{tun}^p and the density of states in the conduction band N_c.

6.2 Trap-Assisted-Tunneling Current

The most influencing effect regarding subthreshold slope degradation and off-state current limitation is the tat effect, which makes it one of the mayor performance factors and has to be modeled thoroughly. In the off-state of the device only carriers located at midgap traps at the channel junctions are able to tunnel into the channel area, thus only the tat effect determines the off-state current. In doing so, it strongly influences the minimum subthreshold slope depending on the trap density N_T and the carrier emission rates e. The tat effect was firstly introduced in section 2.4.1, where an expression for the trap distribution was given.

Based on equation (2.29), the trap distributions at source- and drain/channel junction $N_T^{s/d}$ can be calculated depending on the energy level within the channel region towards which the carrier should tunnel

$$N_T^s = N_{Tmax}^s \cdot \exp\left(-\frac{E_c^{ch}(x,y) - E_v(0,y)}{n \cdot kT}\right), \tag{6.7}$$

$$N_T^d = N_{Tmax}^d \cdot \exp\left(-\frac{E_c(l_{ch},y) - E_v^{ch}(x,y)}{n \cdot kT}\right). \tag{6.8}$$

Figure 6.2 illustrates the tat based current machanism. Electrons on the valence band at the channel junction emit onto midgap traps at higher energy levels, from which they can tunnel into the channel region.

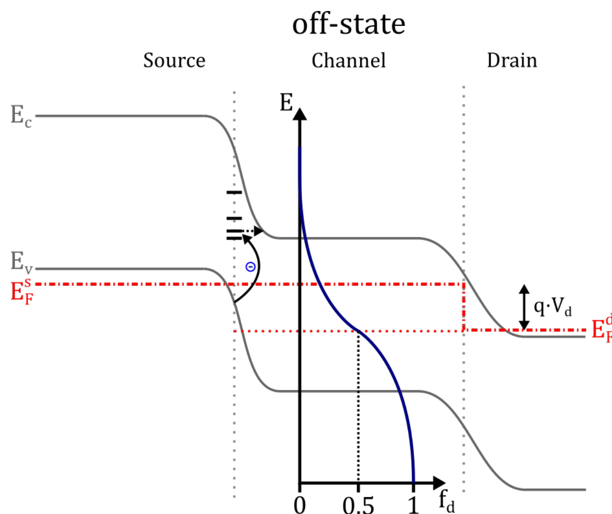

Figure 6.2: Trap-assisted-tunneling current at the source/channel junction. Electrons emit to midgap traps and tunnel into the channel region.

For the current calculation, this means that the density of states and carrier mobility is replaced with the trap concentration and the emission rates

$$\mu_{tun}^{n/p} \cdot N_{V/C} \cdot |\vec{E}| = e_{n/p} \cdot N_T. \tag{6.9}$$

With the tat probability T_{tat} from equation (5.14) follows for the off-state current at source/channel interface:

$$I_{tat}^{on} = w \cdot \frac{e_n \cdot q^2}{k \cdot T} \int_0^{t_{ch}} \int_0^{l_{ch}} N_T^s \cdot T_{tat}^s \cdot (f_s^{on} - f_d^{on}) \cdot |E| \tag{6.10}$$

and at drain/channel interface:

$$I_{tat}^{amb} = w \cdot \frac{e_p \cdot q^2}{k \cdot T} \int_0^{t_{ch}} \int_0^{l_{ch}} N_T^d \cdot T_{tat}^d \cdot (f_d^{amb} - f_s^{amb}) \cdot |E|. \tag{6.11}$$

6.3 Device Current

The overall device current is now put together with the b2b current parts from equation (6.3) and (6.6) and tat current parts from equation (6.10) and (6.11):

$$I = I_{b2b}^{on} + I_{tat}^{on} + I_{tat}^{amb} + I_{b2b}^{amb}. \tag{6.12}$$

At this point the analytical 2D current model for the TFET is complete and can be compared to TCAD Sentaurus simulation data and measurements.

CHAPTER 7

Model Verification and Performance Evaluation

In this chapter, the model is verified by comparing to TCAD Sentaurus simulation data, as well as measurement data. Therefore, a standard device and the simulation setup is specified in section 7.1. Various changes in device geometry were carried out to verify the accurateness of the model in section 7.2. Conclusions about performance improvements are drawn in section 7.3 by optimizing the subthreshold slope and suppressing the current in ambipolar-state. Also the capabilities of hetero-junctions are investigated in section 7.3.2.

7.1 Device Specification and Simulation Setup

Within this section the parameters for the device simulation with TCAD Sentaurus are listed and explained, including the device geometry and materials, doping profiles, band-gap narrowing as well as tat and b2b tunneling models. For the comparison of the model and TCAD, a standard device is defined from which parameter variations are performed in order to see how the physics based analytical model is able to predict such variations. Therefore, it is important to point out that only one initial parameter fitting in the analytical model is done for the standard device. The fitting parameters shown in table 7.2 are the screening length parameter λ_{fit} from equation (2.20), carrier mass m, tunneling mobility μ_{tun}, barrier height limitation factor c_{bar} from section 5.3.3, doping diffusion potential extension shift x_{shift} from equation (4.45), trap distribution constant n from equation (2.29) and the carrier emission rate e from equation (6.10). The large changes in drain doping concentration have to be fitted separately, as well as the hetero-junction devices, therefore only parameters are listed which differ from the standard fitting in table 7.2.

The standard device parameters for the comparison to TCAD simulation data are specified in table 7.1. Investigated is a silicon double-gate n-TFET with a high-κ HfO_2 gate insulator to maximize the gate control over the channel region. The double-gate structure offers the advantage to estimate the current in fin-structures with large fin heights while keeping the

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mathematics "simple". The source region of the device is highly p-doped, the drain region is highly n-doped, while the channel region stays intrinsic. Doping profiles at the channel junctions are implemented to capture the unwanted doping diffusion processes occurring during the device fabrication. Defect states (midgap traps) are defined at the source- and drain/channel junction, which limit the off-state current of the device. To simulate the b2b tunneling current a non-local tunneling model is implemented within the simulation. It considers only energetically constant (horizontal) tunneling directions and is based on the WKB-approximation [37]. For the tat current the Hurks tat model is implemented within the simulations [37]. The channel length is chosen to be 22 nm in order to demonstrate the consideration of short channel effects. A channel thickness of 10 nm is sufficient to neglect quantization effects [63] and still fullfil the l_{ch} >> t_{ch} requirements. For a suppression of the ambipolar current different drain doping concentrations are investigated. The performance enhancing effects of a hetero-junction (hj) TFET are shown on two different devices with the same geometry. The first one is a Ge/Si hj-TFET similar to the device introduced in [64]. The second one is a SiGe/Si hj-TFET similar to the device shown in [65]. For the device specification and the fabrication process of the measured nanowire-TFET refer to [66].

Table 7.1: Standard TCAD simulation setup for model verification.

Parameter	*Value*	*Parameter*	*Value*
l_{ch}	22 nm	N_s	10^{20} cm^{-3}
t_{ch}	10 nm	N_d	10^{20} cm^{-3}
t_{in}	2 nm	N_{Tmax}	10^{12} eV^{-1}cm^{-2}
l_{sd}	20 nm	Device material	Si
σ	1 nm	Oxide material	HfO_2

Table 7.2: Model fitting parameters for the standard device, drain doping variation and hetero-junctions.

Parameter	*Standard*	N_d = 5e19	N_d = 1e19	N_d = 5e18	*Ge/Si*	*SiGe/Si*	*NW*
λ_{fit}^s [-]	1.1						1.2
m_n [-]	0.32				0.27	0.23	0.05
μ_{tun}^n [cm^2/Vs]	4.5				10	10	0.5
c_{bar}^s [-]	0.28						0.2
λ_{fit}^d [-]	1			1.2			0.8
m_p [-]	0.5	0.43	0.26	0.2			0.3
μ_{tun}^p [cm^2/Vs]	38	200	30	0.5			0.5
c_{bar}^d [-]	0.32	0.38	0.38	0.33			0.3
x_{shift} [nm]	-0.4						-0.2
n_s [-]	2						1
e_n [s^{-1}]	5e7				1e7	3e6	2e13
n_d [-]	2						1
e_p [s^{-1}]	7e7	1.5e8	8e8	2e9	2e8	7e6	2e16

7.2 TCAD Verification

In this section a comparison of the physics-based analytical model with TCAD Sentaurus simulation data is performed. Based on the simulation setup introduced in section 7.1, firstly the electrostatic solution is compared, followed by the current characteristics for the standard device. The capabilities of the model are tested by various parameter variations at the end of this section.

7.2.1 Electrostatic Solution

The first results show a comparison of the electrostatic solutions of the TFET model with the simulations. Keep in mind that the fitting is done for an accurate device current, therefore some deviations are to be expected in this part of the results to level approximations in the current calculation.

In figure 7.1 the potential solution is shown along a y-cross-section directly below the gate insulator at $y = 0.05\ nm$. The gate voltage is varied $V_g = -0.25$ to $1\ V$ in steps of $0.25\ V$, while the drain voltage is $V_d = 0.7\ V$. The three different potential solutions are visible in source, channel and drain region. Per TCAD definition, the built-in potential in source region is on the negative intrinsic Fermi-level. The second part of the potential solution shown in figure 7.2

illustrates the results at different y-cross-section positions $y = 0.05, 1.5, 5\ nm$ at $V_g = 0.25\ V$ and $V_d = 0.7\ V$. With an increasing distance to the gate insulator, the electrostatic influence of the gate-electrodes on the channel region is weakening, which results in a flattened potential distribution. Besides small expected deviations, the potential model is able to predict an accurately behaving 2D potential solution not only within the channel region but at every point of the device.

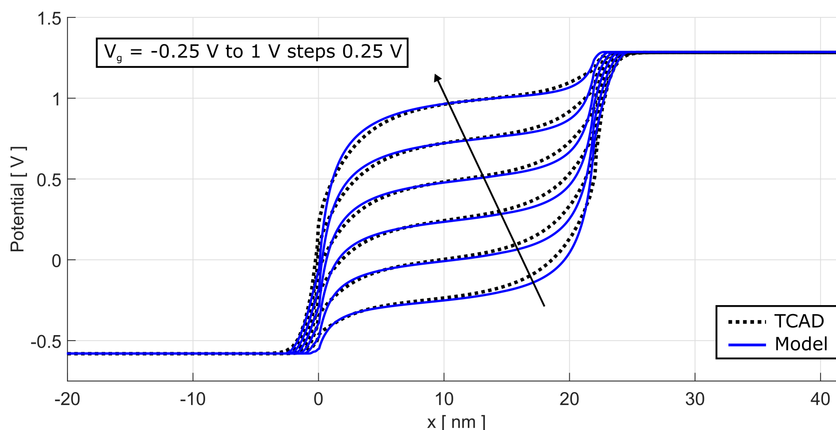

Figure 7.1: Comparison of the potential solution with TCAD simulation data for $V_g = -0.25$ to $1\ V$ in steps of $0.25\ V$ at $y = 0.05\ nm$ and $V_d = 0.7\ V$.

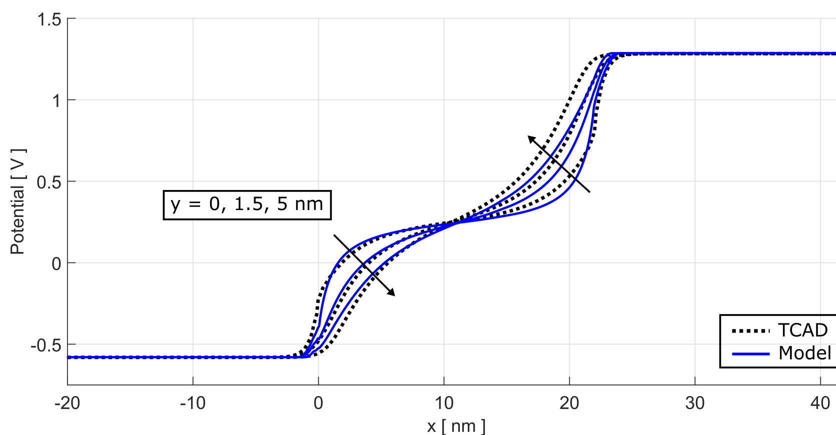

Figure 7.2: Comparison of the potential solution with TCAD simulation data at different y-cross-sections $y = 0.05, 1.5, 5\ nm$ at $V_g = 0.25\ V$ and $V_d = 0.7\ V$.

An exact potential solution forms the basis of the band-structure calculation, which is compared in the next results illustrated in figure 7.3. The band-structure of the standard device is shown for different gate voltages $V_g = -0.25, 0.25, 0.75\ V$ in all three states of the device. Some

deviations at the conduction band at the source/channel interface and the valence band at the drain/channel interface of the device are visible. Although the doping profiles are accounted for within the potential solution of the device, the band-gap narrowing transition at the channel interfaces is still abrupt, thus leading to the visible kinks. However, they are not important in terms of the current calculation, since at these points no tunneling is occurring.

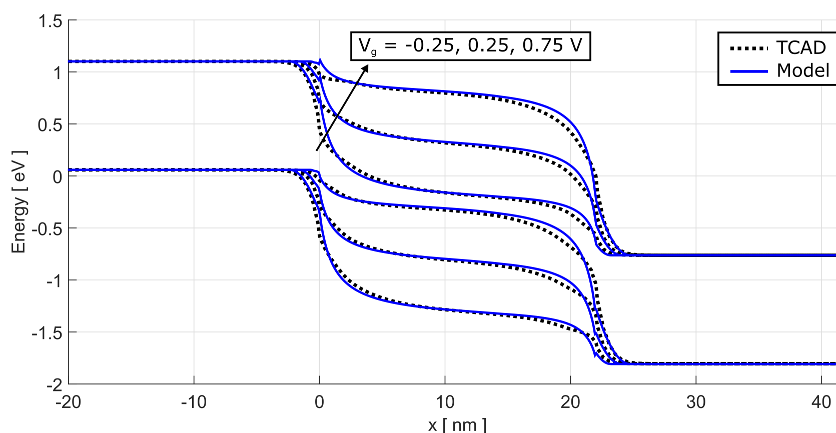

Figure 7.3: Band-structure comparison of the standard device in all three states of the TFET at $V_g = -0.25, 0.25, 0.75\ V$ and $V_d = 0.7\ V$. The aprubt bgn model leads to kinks at the channel junctions.

The last results in this section show a comparison of the electric field solution within the channel region of the device in figure 7.4. Here, the results are shown for all three states of the device as well at $V_g = -0.25, 0.25, 0.75\ V$. Similar to the band-structure plot, the electric field directly at the junctions do not account for the current calculation.

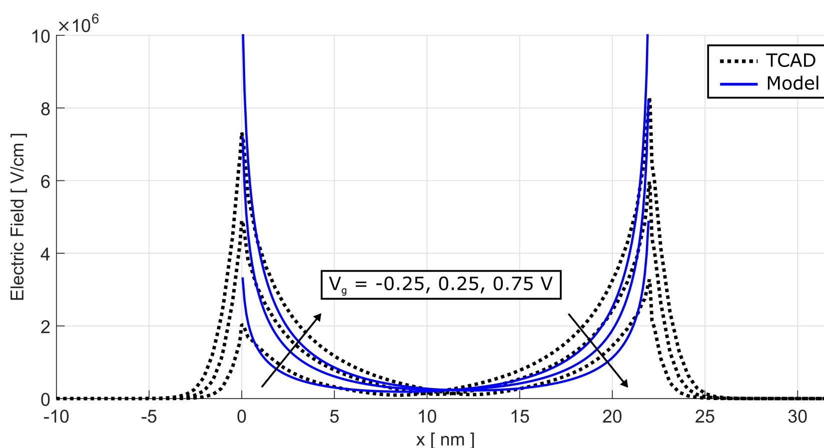

Figure 7.4: Electric field comparison in the channel region of the standard device in all three states of the TFET at $V_g = -0.25, 0.25, 0.75\ V$ and $V_d = 0.7\ V$.

7.2.2 Current Characteristics

Based on the electrostatics solution, the tunneling probability and device current is calculated. It contains a b2b current in the on-state at the source junction, two tat current parts in the off-state and a b2b current in the ambipolar-state at the drain junction. This section shows the transfer- and output-characteristic of the TFET.

The first results in this section show a comparison of the current transfer characteristics of the standard double-gate n-TFET introduced in section 7.1. Figure 7.5 shows the model results in comparison to TCAD Sentaurus simulation data for different drain voltages $V_d = 0.1, 0.3, 0.5, 0.7\ V$.

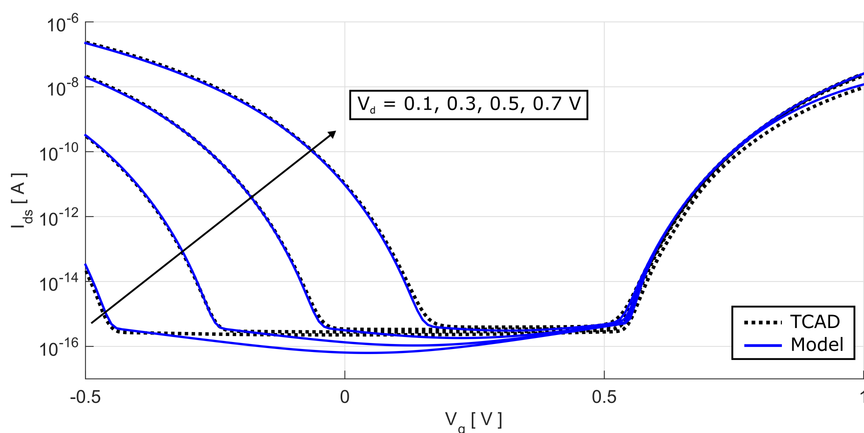

Figure 7.5: Current transfer characteristics of the standard TFET for $V_d = 0.1, 0.3, 0.5, 0.7\ V$.

Evidently, the model captures all necessary drain voltage related dependencies and predicts an accurate current output. Three different aspects can be seen based on the transfer characteristics. The first, most fundamental aspect is the current reduction in the on-state of the device for smaller drain voltages, similar to MOSFET.
The second aspect is tat-based off-state current of the device, typical for the TFET. Here, direct conclusions can be drawn to the present traps at the channel interfaces. The lower the off-state current of the device, the less traps are present.
The third aspect, typical for the TFET, is the drain voltage dependent transition into the ambipolar state of the device. In order to understand this behavior a closer look into the band-structure is necessary. Figure 7.6 shows the band-structure at the drain/channel interface for different drain voltages and a constant gate voltage. The ambipolar-state begins when the valence band in the channel region overlaps with the conduction band in the drain region. For low drain voltages a much lower gate voltage is necessary to achieve such an overlap, whereas for the medium drain voltage the overlap has just happened for this particular gate voltage.

For the highest drain voltage, the device is already deep in the ambipolar-state. In summary, the drain voltage has direct influence on the band-overlap, and with that, the ambipolar-state. This behavior is an important (unwanted) aspect in terms of future circuit design and has to be dealt with carefully. Because of this reason the suppression of the ambipolar-state current is one of the major goals in TFET development.

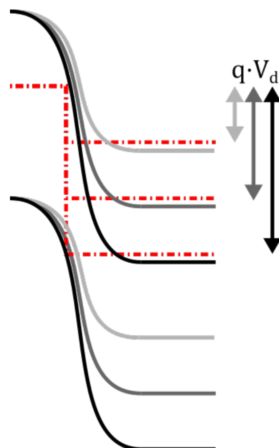

Figure 7.6: Drain voltage dependency on the ambipolar-state of the TFET.

The second results in this section show the current output characteristics of the standard device at different gate voltages $V_g = 0.7, 0.8, 0.9, 0.1\ V$ in figure 7.7. The output current behavior is captured accurately for low and high drain voltages. However, there are some deviations present in the transition which can be traced back to current calculation using Landauer's transmission theory.

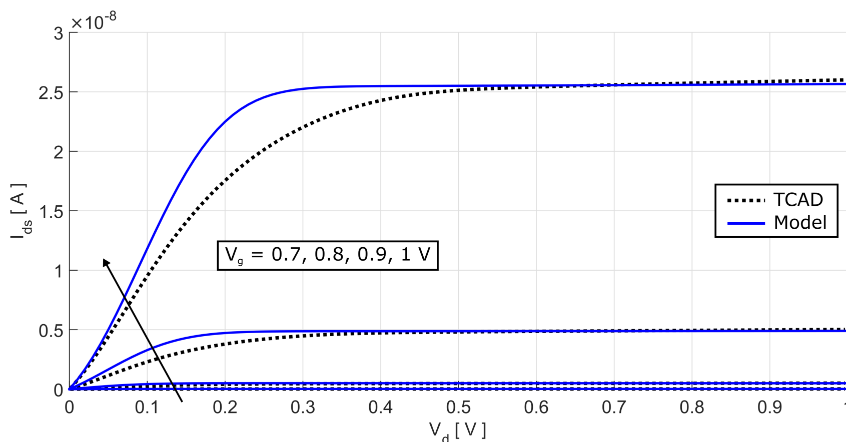

Figure 7.7: Current output characteristics of the standard TFET for $V_g = 0.7, 0.8, 0.9, 0.1\ V$.

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7.2.3 Parameter Variation

In this section the capabilities of the physics-based analytical model are tested by varying diverse parameters and compare the result to TCAD simulation data. Thereby, the model should be able to predict the resulting outcome without additional fitting within a reasonable parameter variation range. The obtained results are discussed in terms of performance enhancement.

The first three results cover important geometric changes of the device structure, beginning with a variation of the channel length in figure 7.8. The results show the impact of an increasing channel length $l_{ch} = 22, 45, 65, 90$ nm on the current transfer characteristic. While for 22 nm short channel effects are present which lead to a increased subthreshold slope and lower on-state current, the simulation data for $45, 65$ and 90 nm show almost no difference. Concluding from this behavior, the TFET shows almost no current dependency from the channel length (despite short channel effects). The reason for that is the "bottle neck" effect of the tunneling mechanism at the source/channel junction, which is the major limiting factor for the device current. The analytical model is able to correctly predict the short-channel based influence on the subthrehold slope in the on-state. The current increase for long-channel devices at higher gate voltages, however, has to be fitted separately.

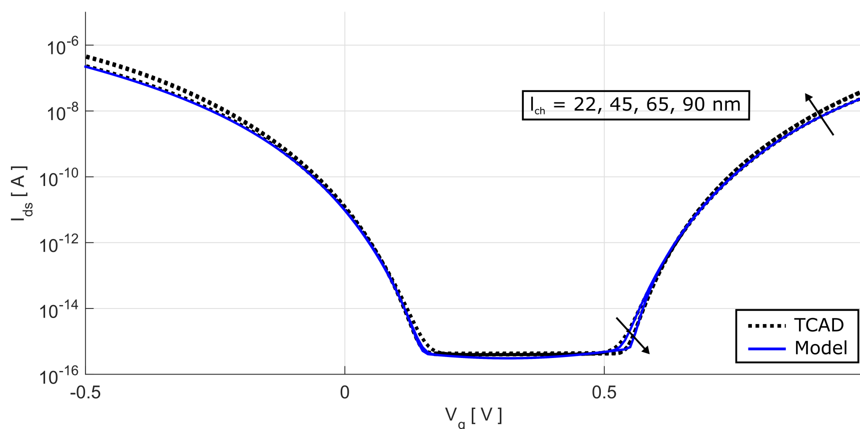

Figure 7.8: Channel length influence on the current transfer characteristic for $l_{ch} = 22, 45, 65, 90$ nm at $V_d = 0.7$ V.

The second comparison in this section shows the variation of the channel thickness. Especially in double-gate devices the channel thickness is a very sensitive parameter. By reducing the distance of both gates to each other, the electrostatic influence of one gate on the not primarily controlled channel region increases dramatically, thus leading to a big performance enhancement. Figure 7.9 shows the change in device current for various channel thicknesses $t_{ch} = 8, 10, 12$ nm. The results show an improved subthreshold slope for thinner device thicknesses, as well as an

increased current. This performance enhancing behavior is captured by the analytical model, although the influence is slightly overestimated. At this point it is important to point out, that this performance enhancing behavior based on a device thickness reduction has a limit. At some point (below 10 nm [63]) quantum effects occur and subbands are being formed, worsening the performance.

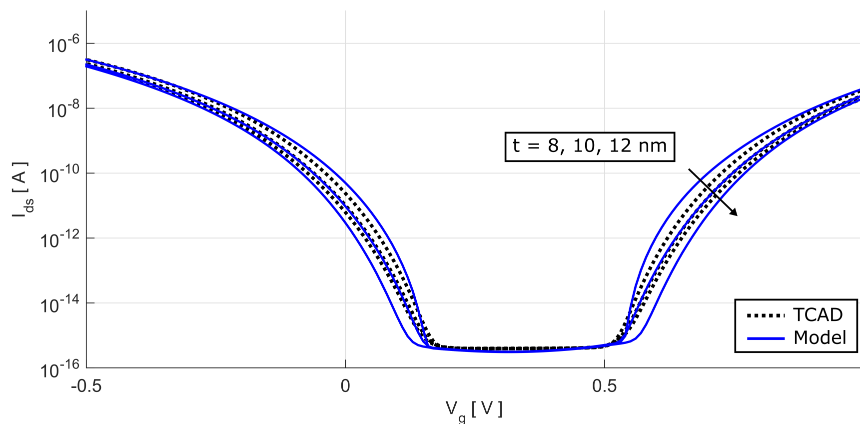

Figure 7.9: Device thickness influence on the current transfer characteristic for t_{ch} = 8, 10, 12 nm at V_d = 0.7 V.

The last geometric variation deals with the influence of the insulator thickness on the device current and is illustrated in figure 7.10 for thicknesses of t_{in} = 1 to 3 nm in 0.5 nm steps. The gate insulator thickness has one of the most sensitive influence on the device current. The thinner the insulator, the bigger the electrostatic influence on the channel region, and with that, the tunneling barrier and device current. Evidently the model is able to accurately predict a wide range of different thicknesses. Not only this shows, that a geometric variation is predicted correctly but a change of the dielectric constant ϵ, based on the used insulator material, can be predicted as well due to equation (4.3).

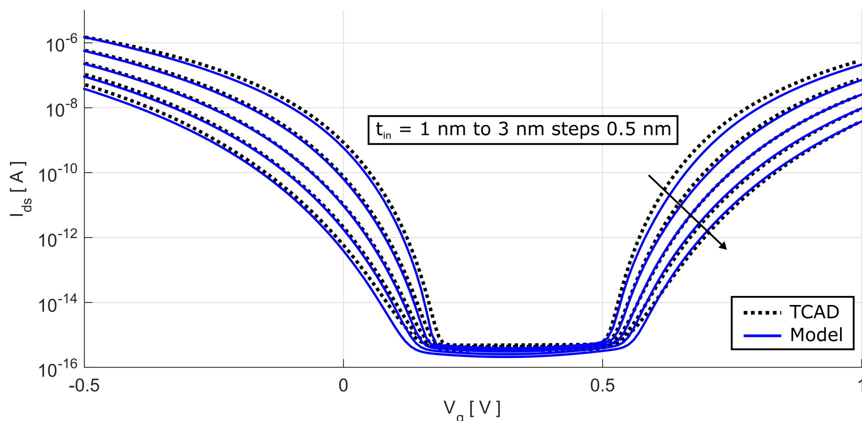

Figure 7.10: Gate insulator thickness influence on the current transfer characteristic for t_{in} = 1 to 3 nm in 0.5 nm steps at V_d = 0.7 V.

At this point the last two significant performance limiting aspects have to be investigated. As mentioned before, the device's off-state current is based on trap-assisted-tunneling events at the source- and drain/channel interface. Hereby, the current level directly correlates with the maximum trap concentration at these junction. The following results in figure 7.11 show the influence of the maximum trap concentration on the off-state current for $N_{Tmax} = 10^{12}, 10^{13}, 10^{14}, 10^{15}, 10^{16}\ eV^{-1}cm^{-2}$. The simulation results show a linear correlation between the trap concentration and the off-state current, which is correctly reproduced by the analytical model. This shows, that a low off-state current can be directly linked with a low trap concentration. Due to an improving subthreshold slope of the b2b-related current at low current levels, the off-state current level limits the lowest achievable subthreshold slope as well. Concluding from this behavior, the trap concentration limits the off-state current and has the highest influence on the minimum subthreshold slope.

The last performance limiting aspect is the quality of the doping profiles at the channel interfaces. The steeper this profile, the steeper the bands in the channel region, and with that, the shorter the tunneling distances. By considering a Gaussian-shaped doping profile at the source/channel interface, the standard deviation σ of this profile is a measure of its quality. The results in figure 7.12 show a comparison of the current transfer characteristics of the model with the simulation data for various standard deviation σ = 0 to 2 nm in 0.5 nm steps. The doping profile based potential extension from section 4.4.3 is able to predict the worsening of the subthreshold slope and on-state current correctly for $\sigma = 0.5, 1\ nm$. For more extended profiles only the reduction in on-state current is captured well. The disproportional increase of off-state current is not captured properly for this regime. Since steep doping profiles are striven for, the model results are sufficient.

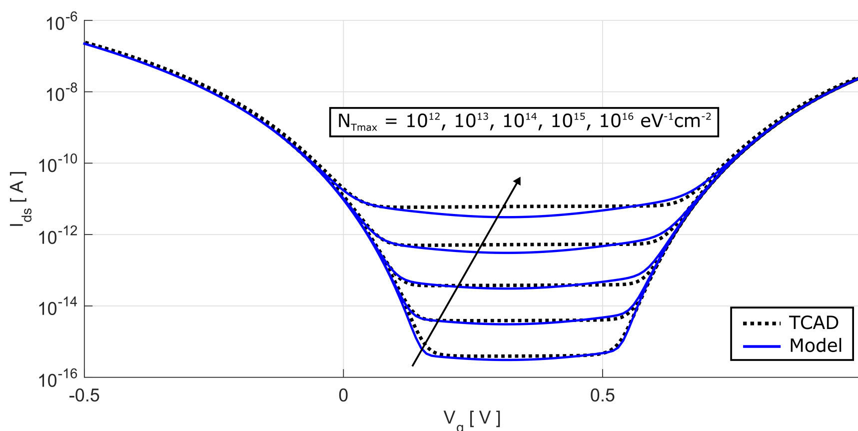

Figure 7.11: Influence of the maximum trap concentration on the TFET's off-state current for $N_{Tmax} = 10^{12}, 10^{13}, 10^{14}, 10^{15}, 10^{16}\ eV^{-1}cm^{-2}$ at $V_d = 0.7\ V$.

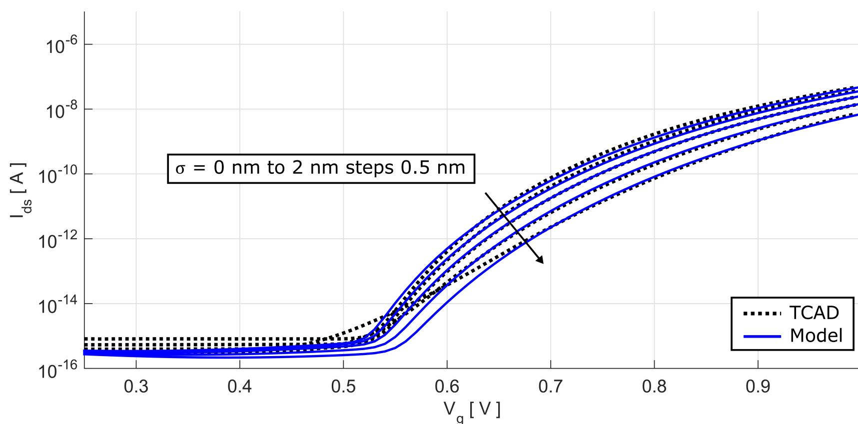

Figure 7.12: Influence of the doping profile quality (standard deviation) at the source/channel junction on the device current for $\sigma = 0$ to $2\ nm$ in $0.5\ nm$ steps and $V_d = 0.7\ V$.

7.3 Device Optimization

This chapter already revealed some performance enhancing methods with the variation of different device geometries, trap concentrations and doping profiles. Within this section other TFET discrepancies are investigated and prospects of their overcoming are given.

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7.3.1 Suppressing Ambipolar Currents

The ambipolar behavior of the TFET occurs because of its asymmetrical doping. It leads to additional complexity in circuit design and should be avoided if possible [67]. There already have been introduced a few methods to suppress this ambipolarity. The simplest way, which can easily be captured with the analytical model, is a reduction of the drain doping concentration. Such a measure has direct influence on the band steepness at the drain/channel junction, which can be equated with an increase of tunneling distance leading to a significant current reduction. Other methods aim for the same effect of a tunneling distance increase e.g. by gate underlaps or low-κ dielectrics at the drain end of the channel region [67].
A high variation of the drain doping can not be captured by the model with the fitting for the standard device, hence all drain doping variations have to be fitted separately as shown in table 7.2. In figure 7.13 the influence of the drain doping concentration on the ambipolar-state current is illustrated for $N_d = 10^{20}, 5 \cdot 10^{19}, 10^{19}, 5 \cdot 10^{18}\ cm^{-3}$. The model shows a good fit with the TCAD simulation data. Evidently, the current in ambipolar-state can be reduced significantly by this measure. However, the drian doping reduction has its limits. By further decreasing the doping concentration, an additional potential barrier is formed at the channel/drain interface. An overcoming of this barrier is only possible by thermionic emission, which limits the subthreshold slope again to 60 $^{mV}/_{dec}$.

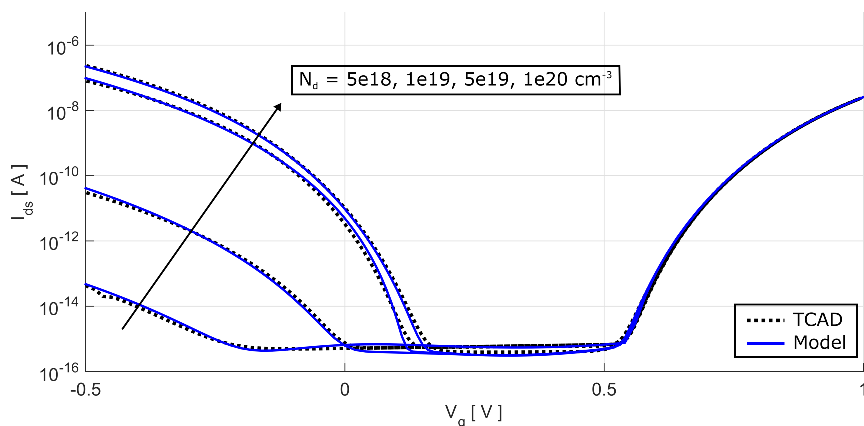

Figure 7.13: Influence of the drain doping concentration on the current in ambipolar-state of the TFET for $N_d = 10^{20}, 5 \cdot 10^{19}, 10^{19}, 5 \cdot 10^{18}\ cm^{-3}$ at $V_d = 0.7\ V$.

7.3.2 Introducing Hetero-Junctions

There are several advantages III/V semiconductors offer compared to standard silicon. Their improved physical parameters such as carrier masses and mobilities directly enhance device performance. If they are used to form hetero-junctions, their smaller band gaps are beneficial for

shorter tunneling distances, which results in increased currents [24]. These upsides have already been recognized and numerous devices with different hetero-junctions have been built. Aim of this thesis is not the application of the model on all different kinds of hetero-junctions but to show that it provides the general possibility to include hetero-junctions in the calculations. In addition to that, the performance enhancing effects of hetero-junctions in TFETs are pointed out and possible downsides are discussed. To give a comparable example, the standard device described in section 7.1 is used with different source materials to generate a hetero-junction at the source/channel interface. The investigated materials are: germanium (Ge), a silicon germanium alloy ($Si_{0.5}Ge_{0.5}$) and the standard Si TFET for comparison. The analytical model has to be fitted individually for each hetero-junction as shown in table 7.2 and the constant material dependent parameters have to be adjusted according to literature [35].
The results in figure 7.14 show the influence of two different hetero-junctions on the current transfer characteristics. The model is able to calculate the current with high accuracy. Compared to the silicon TFET, both hetero-junction devices show an increase in on-state current, due to superior carrier properties. There is an improvement in subthreshold slope observable as well for the SiGe hj device. However, this beneficial effect disappears for the Ge hj entirely and the slope ends up even worse than in the Si TFET. This shows that hetero-junction engineering is quite delicate and has to be carried out thoughtfully. One important thing can be concluded from this comparison and the several fabricated hetero-junctions listed in [26]. There seems to be a trade-off between the maximum on-state current and minimum achievable subthreshold slope. The higher the current, the worse the slope. Nevertheless, an optimum can be found where the positive influence of the hj benefits both, the current and the slope, like for the SiGe hj in figure 7.14.

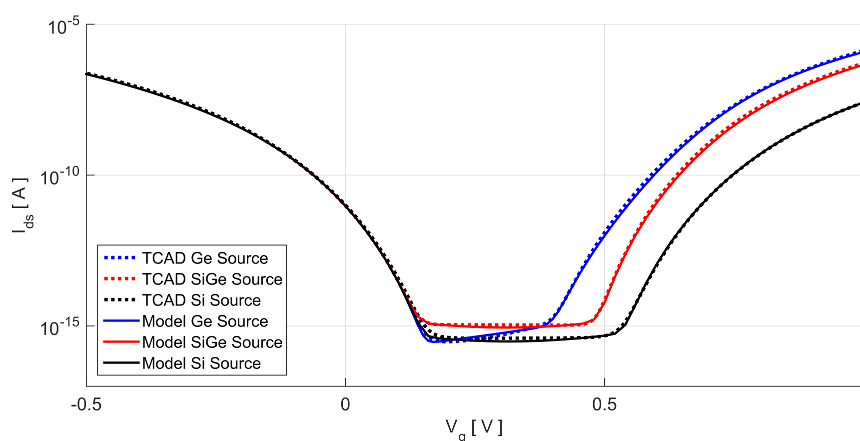

Figure 7.14: Influence of hetero-junctions within the TFET on the on-state current and subthreshold slope with a Ge/Si and $Si_{0.5}Ge_{0.5}$/Si hetero-structure. Silicon device for comparison at $V_d = 0.7\ V$.

7.4 Nanowire n-TFET

Since the model includes all important physical effects that occur in fabricated devices, a comparison to measurement data is possible. The measured device is a nanowire n-TFET introduced in [66]. Due to its geometric parameters it is possible to model the current directly below the gate oxide of the nanowire by using the double-gate Tunnel-FET current with an equivalent width of $w_{dg} \approx \frac{2t_{nw} + w_{nw}}{2}$, hereby w_{nw} and t_{nw} are the width and the thickness of the nanowire, respectively. Figure 7.15 shows the modeled current transfer characteristics for different drain voltages $V_d = 0.1, 0.2, 0.3, 0.4, 0.5\ V$ in comparison to the measurement data. The model fitting is listed in table 7.2.

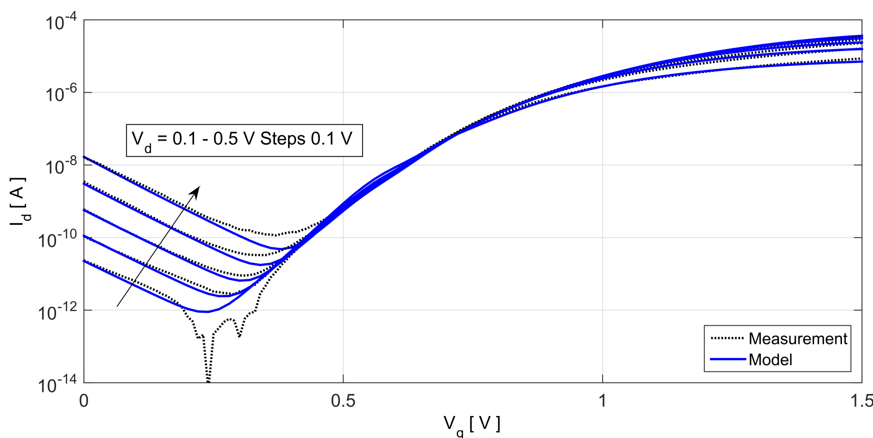

Figure 7.15: Measured current transfer characteristics of a nanowire n-Tunnel-FET for different $V_d = 0.1, 0.2, 0.3, 0.4, 0.5\ V$ in comparison to a single-gate Tunnel-FET model with equivalent device width. Model parameter: $N_{s/d} = 10^{20}\ cm^{-3}$, $N^{s}_{Tmax} = 10^{13}\ eV^{-1}cm^{-2}$, $N^{d}_{Tmax} = 10^{17}\ eV^{-1}cm^{-2}$.

The comparison shows that the model is able to reproduce the measured current transfer characteristics of the nanowire TFET. This shows that all included physical effects are sufficient for a fabricated device prediction.

CHAPTER 8

Random Dopant Fluctuation

The influence of random dopant fluctuations (rdf) on device performance is increasing for the ongoing scaling of nanoscale transistor devices. In the current MOSFET technology this effect mainly affects the threshold voltage V_{th}, which is reduced in terms of the actual distribution of single dopants within the channel region [68]. These dopants are the result of a diffusion process, that occurs during the annealing step in the fabrication of the doped source/drain region. This effect influences the TFETs as well and its effect on device performance has to be investigated.

In this chapter a general explanation of the rdf effect is given in section 8.1, followed by a description of the possible TCAD simulation methods in section 8.2. A general rdf model is introduced in section 8.3, which is later customized for MOSFET devices in section 8.4. In the end an extensive simulation analysis is discussed in section 8.5 for MOSFET and TFET devices. The developed models are compared to TCAD simulation data in section 8.6.

8.1 RDF Basics

In general random dopant fluctuations describe the influence of localized dopants on the device electrostatics and the resulting device current. Or put in simpler words: Not only determines the doping concentration the device characteristics but also the distribution of the discrete doping atoms within the device. These randomly distributed atoms lead to a range of possible current outputs. The dimension of this range, and how it can preferably be described is explained in this section.

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The schematic influences of rdf on the drain current in TFETs are illustrated in figure 8.1. The discretization of dopants leads to different current characteristics. Thereby, the standard deviation of the current can directly be calculated with the current level leading to σ_{I_d}. An equivalent range in gate voltage can also be calculated to cover this current variation, which leads to σ_{V_g}.

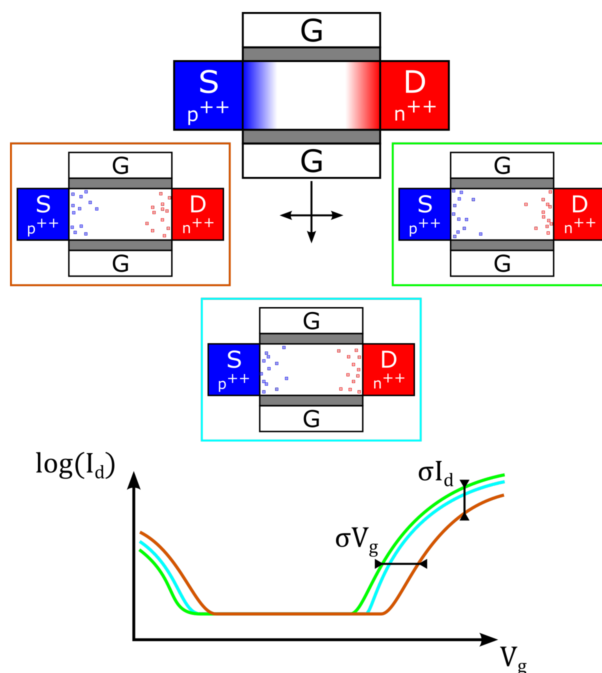

Figure 8.1: Random dopant fluctuation influence on TFET device current, showing standard deviation for gate voltage σ_{V_g} and the standard deviation of the drain current σ_{I_d}.

Figure 8.2 illustrates an example discretization of an n-MOSFET with l_{ch} = 40 nm, t_{ch} = 5 nm, w = 30 nm, $N_{s/d}$ = 10^{20} cm^{-3}, N_{ch} = 10^{18} cm^{-3} and σ = 1 nm. There are 37 dopants diffusing into the channel region from the source- and drain doping (red) and only 3 dopants from the channel doping (blue). This shows how delicate the position of these few dopants can be, regarding the current output.

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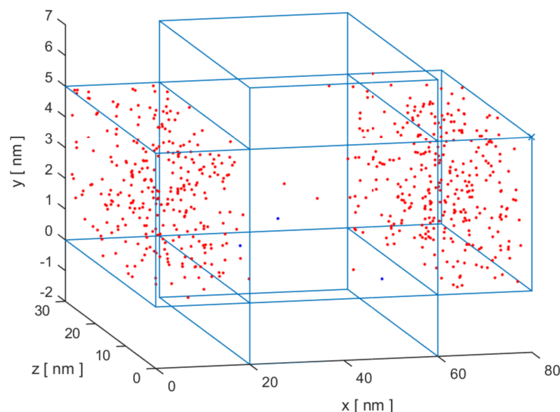

Figure 8.2: Visualized discrete dopants within a MOSFET for l_{ch} = 40 nm, t_{ch} = 5 nm, w = 30 nm, $N_{s/d}$ = 10^{20} cm^{-3}, N_{ch} = 10^{18} cm^{-3} and σ = 1 nm. 37 dopants from the Gaussian doping profiles in the channel region (red) and 3 dopants from the constant channel doping (blue).

8.2 Simulation Methods

There are two elaborate simulations methods available to capture the influence of rdf on the device current. The first one is a small effort noise-based simulation method, called impedance field method (ifm), which is discussed in section 8.2.1. The second method provides a higher accuracy and deeper insight into the rdf effect but also requires a high simulation effort, which is based on randomized profiles and introduced in section 8.2.2.

8.2.1 Impedance Field Method

In this section rdf is simulated in 2D using the impedance field method, which is comparable to noise modeling [69]. For each point of the device rdf is described by the second-order statistical moments of the dopant distribution. These moments are modeled using an analytical function. By using ifm, it is possible to describe the influence of small dopant fluctuations on the applied terminal voltages [70]. Figure 8.3 shows some example simulation results for a DG n-TFET. The plot shows the device current I_d, its standard deviation σ_{I_d}, the relative standard deviation of the device current $rel.\sigma_{I_d} = \sigma_{I_d}/I_d$ and the resulting standard deviation of the gate voltage σ_{V_g}. Due to the constant current in the devices off-state, a small current change leads to a significant gate voltage variation σ_{V_g}.

8.2.2 Randomized Profiles

The theory behind randomized profiles is comparable with the introduction of rdf in section 8.1. In the beginning the analytical doping profiles within the device are discretized using the Sano

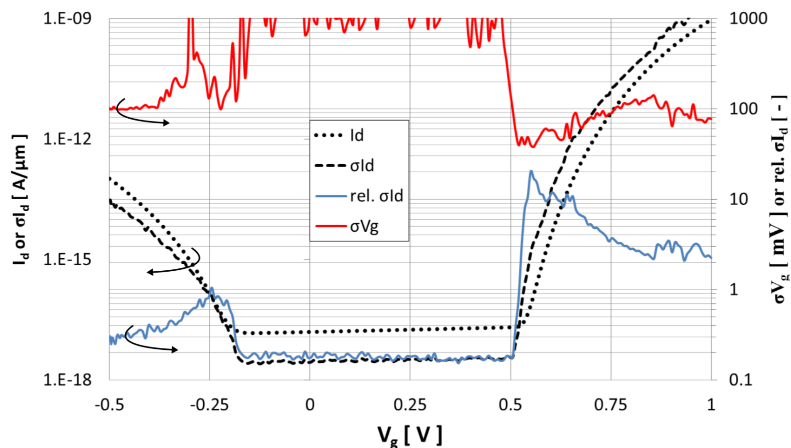

Figure 8.3: 2D TCAD simulation results for a DG n-Tunnel-FET using ifm for N_d = 10^{19} cm^{-3}, σ = 1 nm at V_d = 0.5 V. The results for σ_{V_g} are scaled for w = 30 nm. Geometric parameters listed in table 7.1.

method described in [71]. Thereby a specific number of device samples N is created. Figure 8.4 shows the analytical doping profile and the doping discretization at a randomly chosen cross section of the channel region of a TFET for different standard deviations of the doping profiles σ. The simulation parameters are listed in table 7.1.

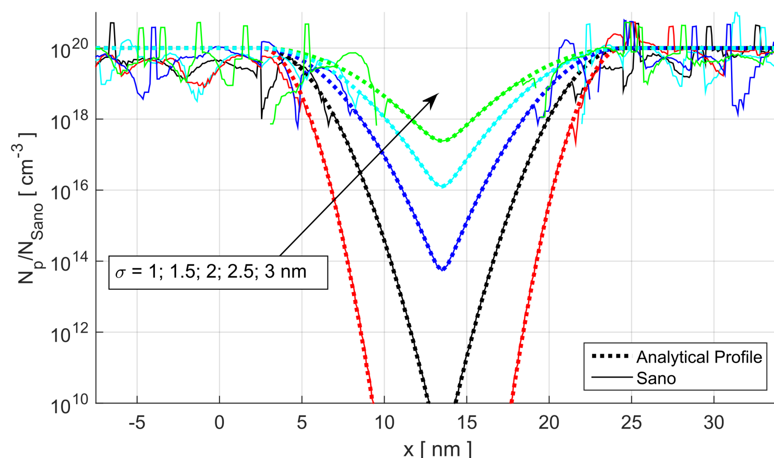

Figure 8.4: Discretization of Gaussian doping profiles using the Sano method.

After creating N devices, they are simulated three-dimensionally with w = 30 nm. After obtaining the current transfer characteristics, the standard deviations for current and gate voltage have to be calculated. Therefore, the average current I_{dAvr} is calculated with

$$I_{dAvr}(V_g) = \frac{1}{N} \sum_{k=1}^{N} I_d^k(V_g) \tag{8.1}$$

and for standard deviation of I_d follows

$$\sigma_{I_d}(V_g) = \frac{1}{N} \sqrt{\sum_{k=1}^{N} \left(I_d^k(V_g) - I_{dAvr}(V_g)\right)^2}. \tag{8.2}$$

The standard deviation of V_g can be calculated using the inverse expressions of I_d: $V_g(I_d)$

$$\sigma_{V_g}(V_g(I_{dAvr})) = \frac{1}{N} \sqrt{\sum_{k=1}^{N} \left(V_g^k(I_{dAvr}) - V_g(I_{dAvr})\right)^2}. \tag{8.3}$$

8.3 General Modeling Approach

The effects of rdf on the drain current can alternatively be described as a result of a randomly distributed gate voltage with a specific variation. In figure 8.1 the schematic connection between rdf and the equivalent standard deviation of the gate voltage is shown. The requirements of a model are to calculate this equivalent gate voltage standard deviation depending on the doping profile at the channel junctions and the channel doping. In the beginning a general model is introduced, which captures the doping influence on the complete channel region of the device. This model is firstly introduced in [72].

The model is developed in three steps. The first step is the calculation of the expected dopant variation within the channel region. Therefore, a mesh grid has to be applied to the device as shown in figure 8.5.

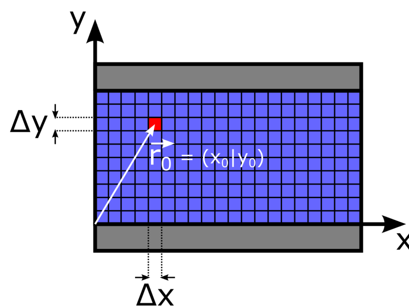

Figure 8.5: Meshing of the channel region, showing a specific cell vector r_0 and the mesh parameters Δ_y, Δ_x.

The expected total number of dopants in the channel region N_{count} can be calculated for every mesh cell. Therefore, the source/drain doping profile N_s/N_d and the channel doping N_{ch} have to be superposed [72]

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$$N_s = \Delta y \int_{\Delta x} N_s \cdot \exp\left(-\frac{x^2}{\sqrt{2\sigma^2}}\right) \cdot dx, \tag{8.4}$$

$$N_d = \Delta y \int_{\Delta x} N_d \cdot \exp\left(-\frac{(x - l_{ch})^2}{\sqrt{2\sigma^2}}\right) \cdot dx, \tag{8.5}$$

$$N_{ch} = N_{ch} \cdot \Delta x \cdot \Delta y, \tag{8.6}$$

$$N_{count} = N_s + N_d + N_{ch}. \tag{8.7}$$

Assuming Poisson distributed dopants, the expected value N_{count} equals the variance of the dopants σ_N^2 [70].

The second step is to capture the influence of randomly distributed dopants in the channel region on the gate charge. Therefore, for every σ_N^2, the associated gate charge variation σ_Q^2 is calculated. Considering a point charge without boundaries, the electric field variance of these charges is given through:

$$|\sigma_{\vec{E}}^2(\vec{r} - \vec{r_0})| = \frac{q \cdot \sigma_N^2}{2\pi\varepsilon|\vec{r} - \vec{r_0}|}. \tag{8.8}$$

The D-field variance is then given through:

$$\sigma_{\vec{D}}^2 = \varepsilon \cdot \sigma_{\vec{E}}^2. \tag{8.9}$$

In order to get the equivalent charge variance σ_Q^2, the D-field variance orthogonal to the gate insulator has to be integrated (see Fig. 8.6)

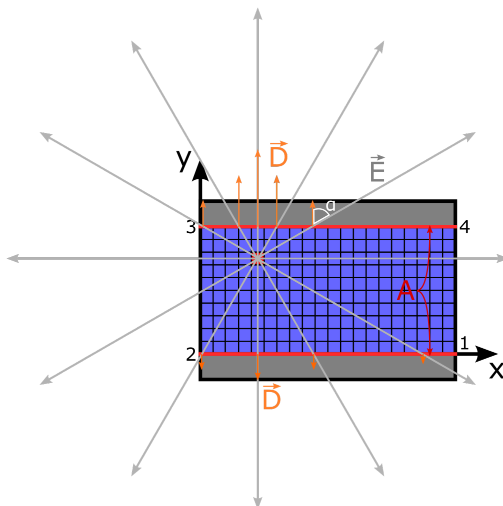

Figure 8.6: Visualization of the considered orthogonal D-field components for the gate charge calculation below the gate oxide and the applied integration borders.

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$$\sigma_Q^2(x_0,y_0) = \int_1^2 |\sigma_{\vec{D}}^2(x_0,y_0)| \cdot \cos(\alpha) \cdot dx + \int_3^4 |\sigma_{\vec{D}}^2(x_0,y_0)| \cdot \cos(\alpha) \cdot dx. \tag{8.10}$$

Considering

$$\cos(\alpha) = \frac{y - y_0}{|\vec{r} - \vec{r_0}|} \tag{8.11}$$

and

$$|\vec{r} - \vec{r_0}| = \sqrt{(x - x_0)^2 + (y - y_0)^2}, \tag{8.12}$$

simplifies equation (8.10) to

$$\begin{aligned}
\sigma_Q^2(x_0,y_0) &= \int_1^2 \frac{q \cdot \sigma_N^2}{2\pi\varepsilon|\vec{r} - \vec{r_0}|} \cdot \frac{y - y_0}{|\vec{r} - \vec{r_0}|} \cdot dx + \\
&\quad \int_3^4 \frac{q \cdot \sigma_N^2}{2\pi\varepsilon|\vec{r} - \vec{r_0}|} \cdot \frac{y - y_0}{|\vec{r} - \vec{r_0}|} \cdot dx \\
&= \frac{q \cdot \sigma_N^2}{2\pi\varepsilon} \int_1^2 \frac{(y - y_0)}{(x - x_0)^2 + (y - y_0)^2} \cdot dx + \\
&\quad \frac{q \cdot \sigma_N^2}{2\pi\varepsilon} \int_3^4 \frac{(y - y_0)}{(x - x_0)^2 + (y - y_0)^2} \cdot dx \\
&= \frac{q \cdot \sigma_N^2}{2\pi\varepsilon} \cdot \left[\arctan\left(\frac{x - x_0}{y - y_0}\right)\right]_1^2 + \\
&\quad \frac{q \cdot \sigma_N^2}{2\pi\varepsilon} \cdot \left[\arctan\left(\frac{x - x_0}{y - y_0}\right)\right]_3^4.
\end{aligned} \tag{8.13}$$

In the third and last step the gate voltage variation $\sigma_{V_g}^2$ can be calculated with the gate charge variation σ_Q^2 and the insulator capacitance C_{in}. Therefore, σ_Q^2 has to be integrated over the whole device:

$$\sigma_{V_g}^2 = \int_0^{t_{ch}} \int_0^{l_{ch}} Q_{fit} \frac{\sigma_Q^2(x,y)}{C_{in}} dx \cdot dy, \tag{8.14}$$

with $C_{in} = \varepsilon_{in}/t_{in} \cdot 2 \cdot l_{ch}$ and a fit factor Q_{fit}, which compensates the assumption of a point charge without boundaries. The standard deviation of the gate voltage is then given through

$$\sigma_{V_g} = \sqrt{\sigma_{V_g}^2}. \tag{8.15}$$

The adaption of this two-dimensional modeling approach on devices with a specific width w can be done by considering [70]

$$\sigma_{V_g}^{3D} = \sigma_{V_g}^{2D} \cdot \sqrt{1cm/w}. \tag{8.16}$$

8.4 RDF-Model Adjustments for MOSFETs

The basic idea of the general model is used to develop a method for an rdf estimation in short-channel double-gate MOSFET devices. For MOSFETs, the current limiting attribute is the potential barrier within the channel region. Therefore, only the influence of randomly distributed dopants within the channel region on the height of the potential barrier at x_m is important. This calculation is inspired by the impedance field method [70], where for each point of the device, RDF is described by the second-order statistical moments of the dopant distribution. In this section all necessary calculation steps are explained to calculate the rdf-based standard deviation of the threshold voltage in MOSFETs.

In the beginning, the influence of a single dopant within the channel region has to be captured by using the solution of Poisson's equation

$$\Delta\Phi = -\frac{\rho}{\epsilon}. \tag{8.17}$$

According to the impedance field method, a variation of doping at a position (x_0,y_0) has influence on the potential. In a small volume dV (or small area for a 2D calculation dA) the doping concentration changes by ∂N, which leads to a charge density change of $\partial\rho$ and results in a changing potential $\partial\Phi$. This relation can be displayed by a superposition of Poisson's equation

$$\Delta(\Phi + \partial\Phi) = \Delta\Phi + \Delta\partial\Phi = -\frac{1}{\epsilon}(\rho + \partial\rho). \tag{8.18}$$

The two solutions can be separated to $\Delta\Phi = -\frac{\rho}{\epsilon}$, which is already solved in the mathematical basics 3.1 of this thesis, and

$$\Delta\partial\Phi = -\frac{\partial\rho}{\epsilon}, \tag{8.19}$$

whereby the boundary conditions along the channel border are zero, since they are already attended to in the potential solution. In order to keep the same surface potential while introducing $\partial\rho$, the flux in the insulator has to change. For the MOSFET only the position of the potential barrier x_m is important because of its current limiting effect. Therefore, the effect of ∂N on the shift of threshold voltage V_{th} is according to the contribution of ∂N to the flux in the insulator at the potential barrier. Figure 8.7 illustrates the flux caused from a doping variation and the position of the potential barrier x_m. For the simulations in this section, the device is operated in linear region at V_d = 50 mV, for which the position of x_m is assumed to

be in the middle of the channel region $x_m = l_{ch}/2$.

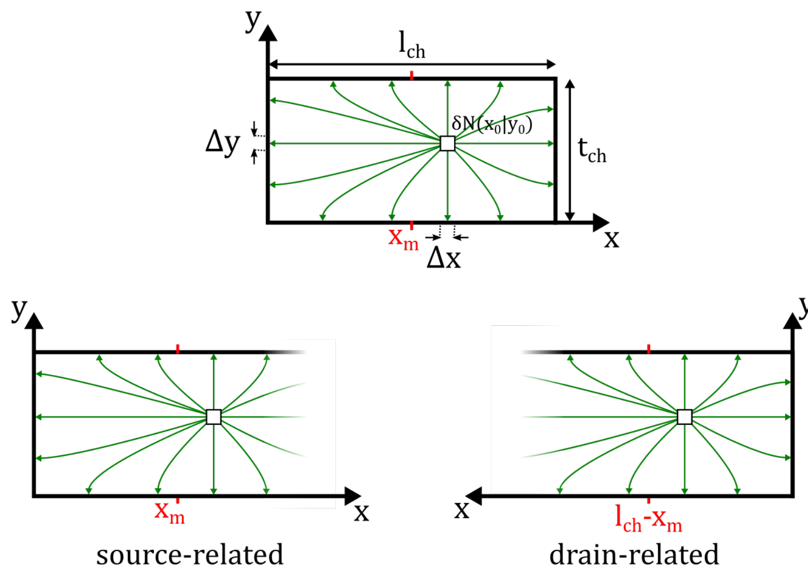

Figure 8.7: Influence of a doping variation ∂N on the potential barrier at x_m. The structure is decomposed in source- and drain-related case.

In order to calculate the flux at x_m, the four-corner structure is decomposed into two two-corner structures: the source- and drain-related case. The source-related structure is used if ∂N is in the left half of the channel region ($x_0 < l_{ch}/2$), otherwise the drain-related structure is used ($x_0 > l_{ch}/2$).

In order to calculate the flux through x_m, the two structures are conformally mapped from z-plane into w-plane using the inverse transformation function $t^{-1}(z)$ from equation (3.25)

$$w = u + jv = t^{-1}(z = x + jy) = \cosh\left(\frac{\pi \cdot z}{t_{ch}}\right). \tag{8.20}$$

Applied on the position of the charge $x_0 + jy_0$ follows

$$w_0 = u_0 + jv_0 = \cosh\left(\pi \frac{x_0 + jy_0}{t_{ch}}\right) \tag{8.21}$$

and for the potential barrier position x_m

$$w_m = u_m = \cosh\left(\pi \frac{x_m}{t_{ch}}\right). \tag{8.22}$$

Figure 8.8 illustrates the mapping of the source-related structure including charge position ($x_0 + jy_0 \rightarrow u_0 + jv_0$) and potential barrier ($x_m \rightarrow u_m$). With the help of a mirror charge at $u_0 - jv_0$ the flux through the mapped potential barrier position u_m can be calculated. The dielectric flux of a line charge is given with

$$D(r) = \frac{q\partial N(x_0,y_0)dA}{2\pi|r|}, \tag{8.23}$$

where $|r| = \sqrt{(u_0 - u_m)^2 + v_0^2}$. Only the D-field parts orthogonal to the u-axis D_u contribute to the flux and can be calculated with the angle α

$$D_u(r) = D(r) \cdot \cos(\alpha). \tag{8.24}$$

By superposing the influence of the ± charge, the vertical flux at u_m can be calculated in w-plane

$$\partial D_m^{(w)} = 2 \cdot \frac{q\partial N(u_0,v_0)dA}{2\pi} \cdot \frac{\cos(\alpha)}{\sqrt{(u_0 - u_m)^2 + v_0^2}} \tag{8.25}$$

and with

$$\cos(\alpha) = \frac{v_0}{\sqrt{(u_0 - u_m)^2 + v_0^2}} \tag{8.26}$$

follows

$$\partial D_m^{(w)} = \frac{q\partial N(u_0,v_0)dA}{\pi} \cdot \frac{v_0}{(u_0 - u_m)^2 + v_0^2}. \tag{8.27}$$

In the next step the solution of the flux in w-plane has to be scaled by $\left|\frac{dz}{dw}\right|$ from equation (3.21) to achieve the solution for z-plane [53]

$$\partial D_m^{(z)} = \partial D_m^{(w)} \cdot \left|\frac{dz}{dw}\right|\Bigg|_{w_m} = \partial D_m^{(w)} \cdot \frac{\pi}{t_{ch}} \cdot \left|\sqrt{u_m^2 - 1}\right| \tag{8.28}$$

with

$$\frac{dz}{dw} = \frac{t_{ch}/\pi}{\sqrt{w-1} \cdot \sqrt{w+1}}. \tag{8.29}$$

For the drain-related case, the same equations apply only for other positions w_0 and w_m

$$w_0 = u_0 + jv_0 = \cosh\left(\pi \frac{l_{ch} - x_0 + jy_0}{t_{ch}}\right), \tag{8.30}$$

$$w_m = u_m = \cosh\left(\pi \frac{l_{ch} - x_m}{t_{ch}}\right). \tag{8.31}$$

With Poisson distributed dopants, the mathematical expectation ∂N equals the variance of said dopants $\sigma^2 \partial N$ [70].The total variance of the flux at x_m can be calculated by integrating over the whole channel region

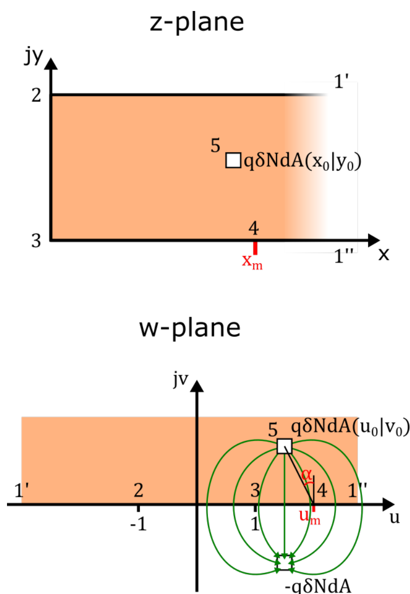

Figure 8.8: Schematic mapping of the source-related structure from z- to w-plane. Flux calculation in u_m using a mirror charge.

$$\sigma_{D_m}^2 = \int_{x_0=0}^{l_{ch}} \int_{y_0=0}^{t_{ch}} \partial D_m^{(z)}(x_0,y_0,x_m)dydx. \tag{8.32}$$

This integral is solved numerically by applying a mesh over the channel region as introduced in section 8.3. Assuming that the variation of the gate voltage equals a variation of the threshold voltage, it can be calculated using the insulator capacitance $C_{in}^{'} = \epsilon_{in}/\tilde{t}_{in}$

$$\sigma_{V_{th}}^2 = \frac{\sigma_{D_m}^2}{C_{in}^{'}}. \tag{8.33}$$

The calculations are only considering a single-gate device so far. For the rdf estimation of double gate devices, the width of a SG-device is doubled $w_{DG} \approx 2 \cdot w_{SG}$ in the scaling process. Additionally the scaling in 3rd dimension is possible using equation (8.16)

$$\sigma_{V_g}^{3D} = \sigma_{V_g}^{fit} \cdot \sigma_{V_g}^{2D} \cdot \beta \cdot \sqrt{\frac{1cm}{2 \cdot w_{SG}}}. \tag{8.34}$$

with the fitting factor $\sigma_{V_g}^{fit}$ and a slope degradation factor $\beta = \frac{S_{avr}}{kT \cdot \log(10)}$. The slope degradation factor takes into account the reduced gate control of the channel region by the gate due to short channel effects. In the following results this parameter has been extracted from the average of TCAD simulations S_{Avr}.

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8.5 Simulation Analysis

In this section a comparative numerical rdf analysis for MOSFETs and TFETs is done in order to demonstrate the influence of this effect for different device types. The aim is to show general dependencies and give recommendations to improve device performance.

To compare MOSFET and TFET in a reasonable way, the device geometries shown in figure 8.9 are kept identical. A silicon DG-n-TFET and a silicon DG-n-MOSFET are under investigation. The TFET device parameters are given in table 7.1. In the MOSFET the only differences are an n-type source doping and a p-type doped channel. To reduce the rdf effects of the channel doping in the MOSFET the doping concentration is kept low at $N_{ch} = 10^{15}\ cm^{-3}$. Gaussian shaped doping profiles are applied at the channel junctions with different standard deviations $\sigma = 1, 1.5, 2, 2.5, 3\ nm$. The doping profile is randomized using the Sano method described in [71] with a cut-off parameter $k_c = 112.336 \cdot 10^6\ cm^{-1}$. This is done for a specific number of samples N.

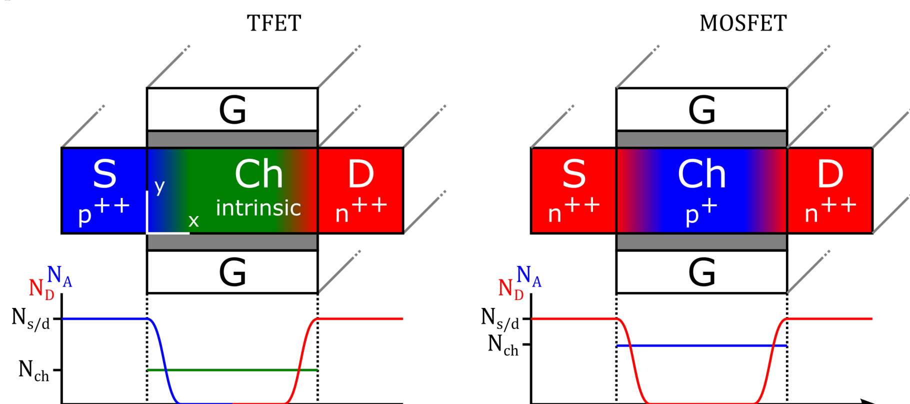

Figure 8.9: Geometries of a DG-n-TFET and a DG-n-MOSFET, showing the doping types and Gaussian doping profiles at the channel junctions.

Firstly the rdf influences on the transfer characteristics in MOSFETs are investigated in section 8.5.1, followed by an analysis for TFETs in section 8.5.2.

8.5.1 RDF in MOSFETs

With the ongoing miniaturization, the rdf effect gains importance even in the conventional MOSFET technology. To further investigate the influence of rdf on the device characteristics a deeper look into the simulations reveals answers. One of the main effects observed is a current shift, which can be expressed as a negative shift in threshold voltage [68]. Figure 8.10 shows $N = 40$ current transfer characteristics simulated with randomized profiles as described in section 8.2.2. The mentioned threshold voltage shift in figure 8.10 is clearly visible but the origin of this behavior can not be determined.

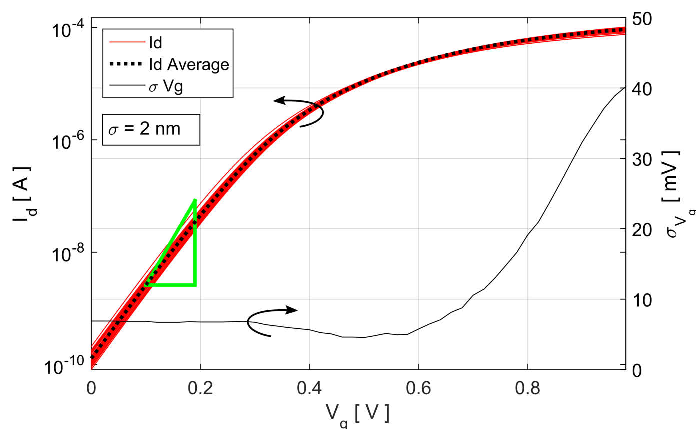

Figure 8.10: Current transfer characteristics of $N = 40$ dg-n-MOSFETs with randomized profiles, showing the calculated average current I_{dAvr} and standard deviation of the gate voltage σ_{V_g} at $V_d = 1\ V$. The green triangle indicates a 60 $^{mV}/_{dec}$ slope.

In order to understand the rdf dependency in the MOSFET, figure 8.11 shows the band structure of the device directly below the gate oxide for randomly chosen $N = 5$ devices.

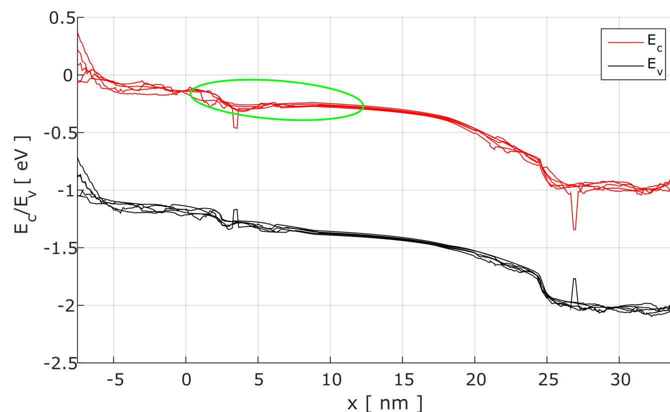

Figure 8.11: Band structure below the gate oxide at a randomly chosen cross-section for $N_{sample} = 5$ MOSFET devices in ON-state with $V_g = 1\ V$, $V_d = 1\ V$ and a standard deviation of the doping profile of $\sigma = 2\ nm$. The green circle shows the area of interest.

Generally, the band structures vary in energy due to the randomized doping level, which leads to a rippling band gap narrowing effect. These variations are also present at the energy barrier in the channel region of the MOSFET. Since the energy barrier is the current limiting parameter for the MOSFET (and its threshold voltage), a variation at the barrier directly leads to a varying current. This connection is the reason for the rdf dependency.

8.5.2 RDF in TFETs

The TFET simulation analysis in this section should give a deeper insight on the variability problems with this new device, since the alternative current transport mechanism shows completely different weaknesses regarding doping discretization and fabrication tolerances. The simulations are done using randomized profiles with the FEM-Simulator TCAD Sentaurus.

Figure 8.12 shows the current transfer characteristics for $N = 20$ samples with $\sigma = 1.5\ nm$. In comparison to the homogeneous doping profile, the threshold voltage of all samples is smaller and the S is worsening.

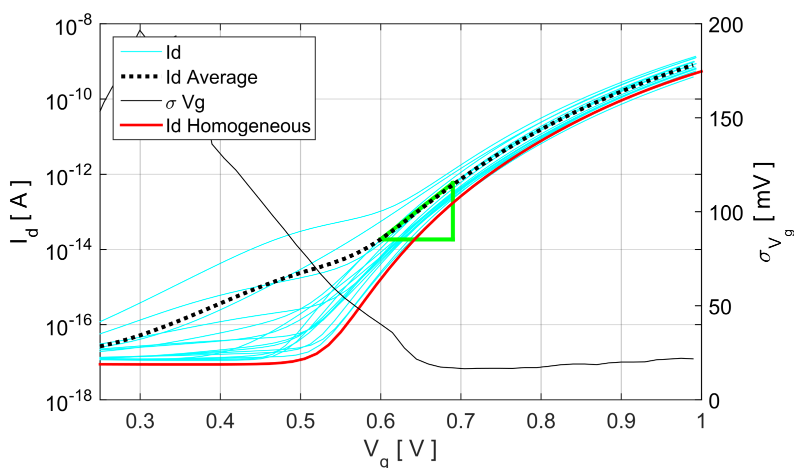

Figure 8.12: TFET drain current I_d for $N = 20$ randomized samples in comparison to a homogeneous doping profile. Standard deviation of the gate Voltage σ_{V_g} on the right. Green triangle $= 60\ {}^{mV}/_{dec}$ slope.

In order to understand these effects, two samples are further analyzed. One with the best subthreshold slope S_{min}, and one with the worst S_{max}. Figure 8.13 shows the current transfer characteristics of these two devices.
A deeper insight on why the current characteristics are so different for the same device parameters, gives the band structure. In figure 8.14 the band structure at the source/channel interface at characteristic gate voltages $V_g = 0.25, 0.5, 0.65, 1\ V$ is shown. The results are extracted at a position directly below the gate oxide where the maximum current of the device is flowing. At $V_g = 0.25\ V$ current flow starts in the S_{max} device, whereas in the S_{min} device this happens for a higher gate bias of $V_g = 0.5\ V$. At $V_g = 0.65\ V$ the current reaches the same level in both devices, and at $V_g = 1\ V$ the current in the S_{min} device is higher.

The results in figure 8.14 show that the threshold voltage of randomized devices is lower due to different distinctive band-gap narrowing effects near the channel junction. This greatly affects

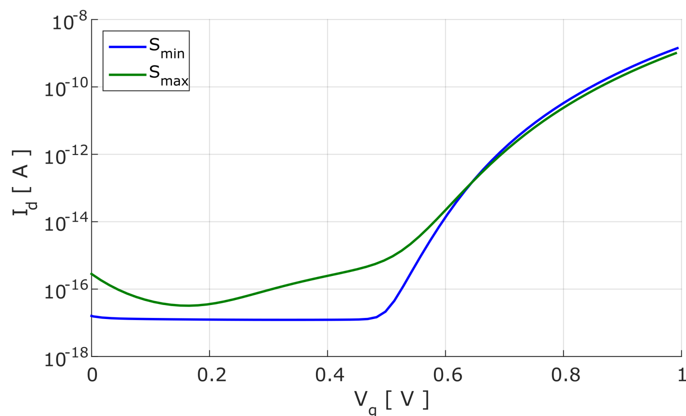

Figure 8.13: Drain current of two devices with S_{min} and S_{max}.

the gate voltage needed to get an overlap of the valence band in the source region with the conduction band in the channel.

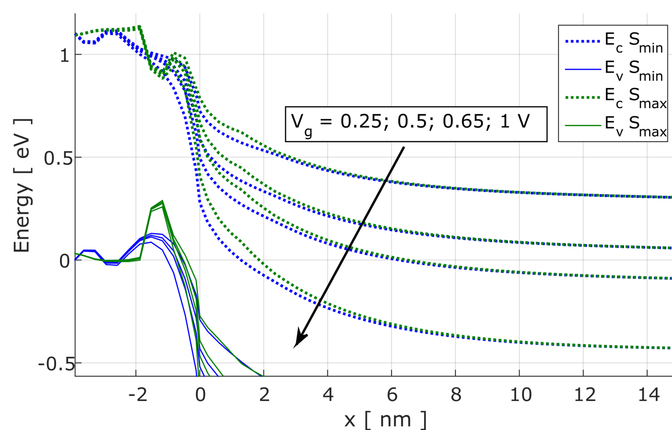

Figure 8.14: Band structure of two TFET devices with S_{min} and S_{max} at maximum current and characteristic gate voltages.

The subthreshold slope is decisively depending on the tunneling distance reduction rate for increasing V_g. For $V_g = 1V$ the tunneling distance of the S_{min} device gets shorter than for the S_{max} device at the same bias. This explains the reduced on-state current of the S_{max} device. Therefore, a discrete dopant located in the channel region near the junction is also negatively affecting the subthreshold slope of the device.

A direct influence of the doping profiles standard deviation on σ_{V_g} is suspected. Meaning that,

the fewer dopants are in the channel region, where charges are tunneling to, the less deviation of the current is to be expected. Figure 8.15 is supporting this suspicion and it shows a decreasing σ_{V_g} for less standard deviation of the doping profile.

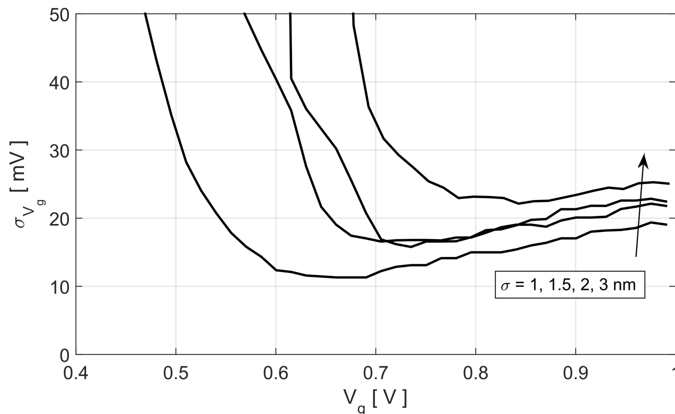

Figure 8.15: Comparison of the gate voltage deviation σ_{V_g} for different doping profile standard deviations $\sigma = 1, 1.5, 2, 3$ nm at $N = 20$ and $V_d = 1$ V.

The results of this simulation analysis provide an alternative explanation and understanding of the commonly known effects of threshold voltage shifting, subthreshold slope degradation and drain current variability in fabricated TFET devices. Due to band-gap narrowing caused by discrete dopants at the channel junctions, the band overlap position is affected, resulting in a threshold voltage shift. Within the channel region, discrete dopants influence the tunneling distance reduction rate, which leads to a subthreshold slope degradation.

After analyzing rdf in MOSFETs and TFETs, fundamental differences have been discovered in the band structure comparison. The MOSFET is less predisposed than the TFET regarding rdf effects. A deeper look into the band structure of both devices shows different dependencies. Due to doping dependent band-gap narrowing at the channel junctions the energy barrier is directly influenced by rdf in the MOSFET, which leads to the current variation. In the TFET, this same energy variation leads to a comparatively higher variation in the tunneling distance, which is decisive for the TFET current. Therefore, rdf has a higher influence on the TFET.

8.6 RDF Model Results

The general model introduced in section 8.3 is applied to estimate the standard deviation of the gate voltage σ_{V_g} in TFET devices. Since the basic model is not gate voltage dependent, in contrast to σ_{V_g} in TFETs, it is fitted for $V_g = 0.9$ V. Device paramters listed in table 7.1. The simulations are done using randomized profiles with $N = 20$ samples for each doping profile. The results show that the basic model is able to correctly predict the gate voltage standard

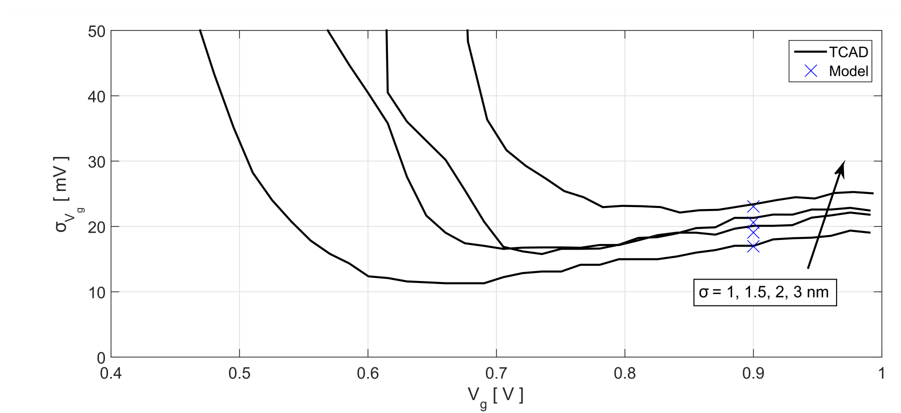

Figure 8.16: Model comparison of the gate voltage deviation σ_{V_g} for different doping profile standard deviations $\sigma = 1, 1.5, 2, 3\ nm$ at $N = 20$, $Q_{fit} = 0.25$ and $V_d = 1\ V$.

deviation for various doping profiles. The focus of this section, however, lays on the MOSFET-adjusted model for which a variety of simulations are carried out.

In the following the MOSFET-adjusted model is compared to TCAD simulation data for various l_{ch}, N_{ch} and σ in order to demonstrate its accuracy. A short channel standard Si n-MOSFET is chosen with the following parameters: $l_{ch} = 10\ nm$, $t_{ch} = 5\ nm$, $t_{in} = 2\ nm$, $N_{s/d} = 10^{20}\ cm^{-3}$, $N_{ch} = 10^{18}\ cm^{-3}$, $\sigma = 1\ nm$. The gate voltage variation is extracted at a constant current level $I_d = 10^{-8}\ A$ and the barrier position is set to be in the channel mid $x_m = \frac{l_{ch}}{2}$ due to the low drain voltage of $V_d = 50\ mV$. Since the shift of the current transfer characteristic can be seen as a shift in threshold voltage stands:

$$\sigma_{V_{th}} \approx \sigma_{V_g}. \tag{8.35}$$

For each TCAD data point $N = 40$ randomized profiles are simulated and analyzed. The first results in figure 8.17 show the deviation of the gate voltage σ_{V_g} for different channel lengths $l_{ch} = 10, 20, 40\ nm$. The model is able to predict the simulation results and shows an increasing rdf influence below $l_{ch} = 20\ nm$. This behavior is further investigated later in this section.

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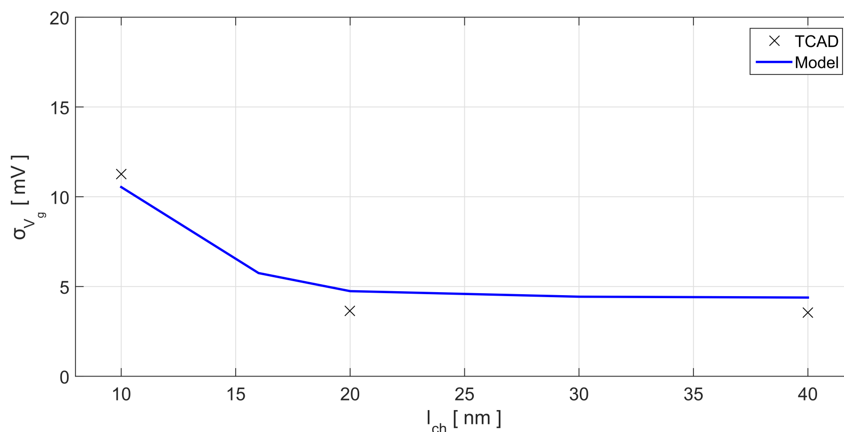

Figure 8.17: Rdf influence on the gate voltage deviation σ_{V_g} for different channel lengths $l_{ch} = 10, 20, 40$ nm at $V_d = 50$ mV.

The deviation of the gate voltage in dependency of the channel doping is shown in figure 8.18. For an increasing channel doping concentration $N_{ch} = 10^{16}, 10^{17}, 10^{18}$ cm^{-3} the rdf influence is rising as well, which results in a higher standard deviation.

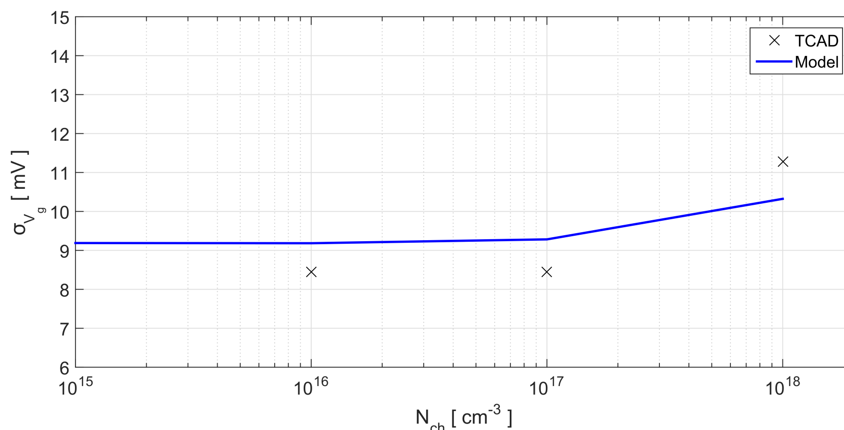

Figure 8.18: Rdf influence on the gate voltage deviation σ_{V_g} for different channel doping concentrations $N_{ch} = 10^{16}, 10^{17}, 10^{18}$ cm^{-3} at $V_d = 50$ mV.

Figure 8.19 shows the results for a varying standard deviation of the doping profile $\sigma = 0.5, 1, 1.5$ nm. The expected σ_{V_g} increase for larger doping profiles is correctly reproduced with the model. For this plot the channel doping is kept low at $N_{ch} = 10^{15}$ cm^{-3} to better capture the influence of the doping profiles.

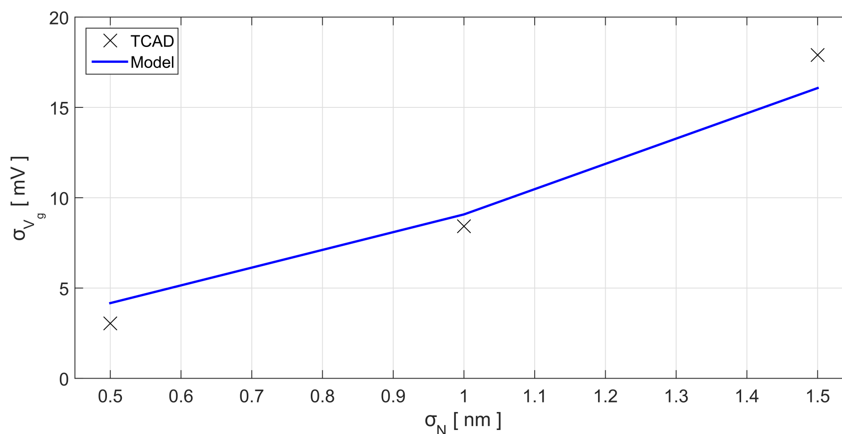

Figure 8.19: Rdf influence on the gate voltage deviation σ_{V_g} for different doping profile deviations $\sigma_N = 0.5, 1, 1.5$ nm at $V_d = 50$ mV.

A deeper insight into this results is given with $\partial D_m^{(z)}$ from equation (8.32). By investigating this parameter, specific regions within the channel area show a higher influence on the potential barrier than others. The first device which is investigated has a small channel length $l_{ch} = 10$ nm, a high channel doping concentration $N_{ch} = 10^{18}$ cm^{-3} and a doping profile standard deviation of $\sigma_N = 1$ nm. The model results in figure 8.20 show the regions with high rdf influence. For this short channel length the doping profiles near the channel junctions have an influence on the potential barrier in the channel mid as well. The maximum of this influence is not located at the maximum doping profile concentration directly at the channel junction nor at the shortest distance to the potential barrier directly at the gate oxide. The optimum region is where still a high doping profile concentration is present but not too far away from the barrier. The decreasing influence near the gate oxide can be explained by the preferential direction of the $\vec{D}$-field lines directly to the gate and not the detour over the potential barrier. The additional high channel doping leads to an increased influence directly below the oxide at the potential barrier position in the channel mid.

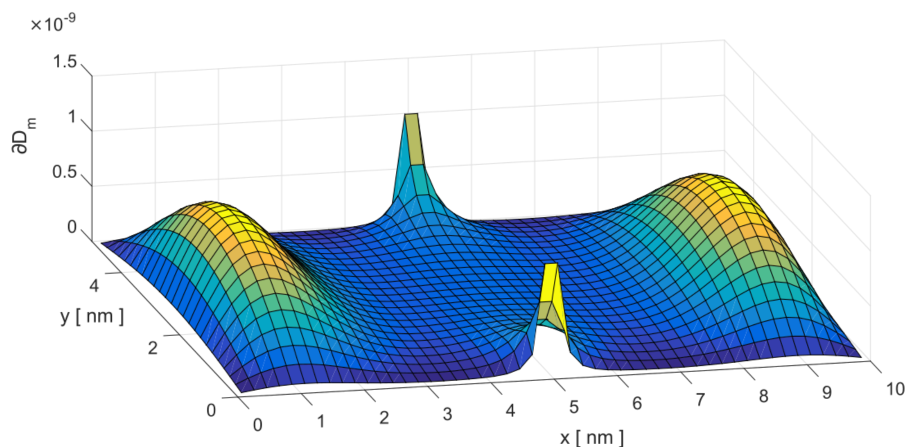

Figure 8.20: Rdf influential channel regions analyzed with $\partial D_m^{(z)}$ for l_{ch} = 10 nm, N_{ch} = 10^{18} cm^{-3} and σ = 1 nm.

In figure 8.21 the channel doping is reduced and with that the influence of that doping disappears. Now only the doping profiles at the channel junctions contribute to the standard deviation of the gate voltage.

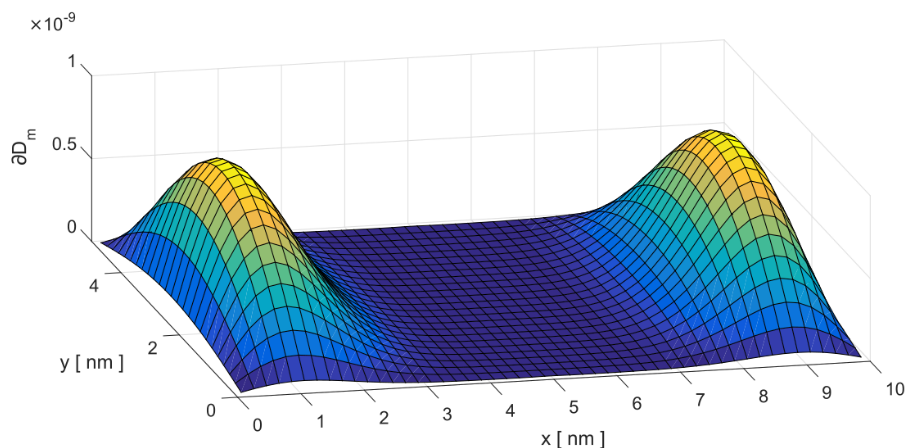

Figure 8.21: Rdf influential channel regions analyzed with $\partial D_m^{(z)}$ for l_{ch} = 10 nm, N_{ch} = 10^{15} cm^{-3} and σ = 1 nm.

In the last results of this section in figure 8.22 the channel length is altered to show, that for long channel devices the doping profiles do not contribute to the standard deviation of the gate voltage. Instead, only the channel doping is relevant. This explains the swift increase of σ_{V_g} for shorter channel lengths.

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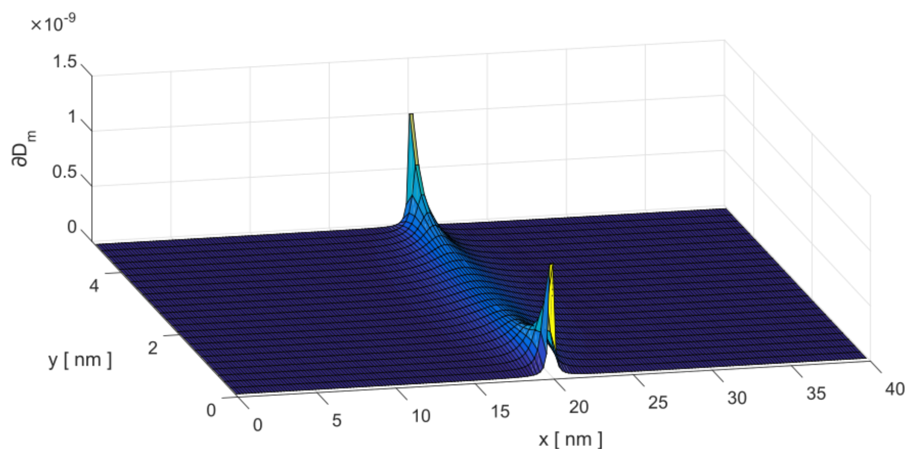

Figure 8.22: Rdf influential channel regions analyzed with $\partial D_m^{(z)}$ for l_{ch} = 40 nm, N_{ch} = 10^{18} cm^{-3} and σ = 1 nm.

The results show that the improved analytical MOSFET rdf model is able to predict the rdf-based gate voltage standard deviation (or threshold voltage variation) in dependency on the channel length, channel doping concentration and standard deviation of the Gaussian doping profiles at the channel junctions. By considering short channel effects, accurate model results are achieved, which allow a deeper insight in rdf-sensitive regions within the channel area.

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CHAPTER 9

Conclusion

This work introduces an analytic tool for a realistic two-dimensional calculation of the double-gate TFET device current in all operating regimes. All important physical effects occurring in these kind of devices are implemented in the model.

The potential is solved for each region of the device. In the channel region parabolic boundaries at the source- and drain-channel junction are taken into account, as well as constant boundaries at the gate electrodes. With the help of structural decomposition and the conformal mapping technique, the calculations lead to a two-dimensional potential solution within the channel region. Adjacent to this solution, parabolic potential extensions in source and drain region are introduced. Gaussian-shaped doping profiles at the channel junctions are considered by implementing a doping profile based potential extension, which completes the two-dimensional device potential solution. The electric field is needed within the channel region of the device, which is obtained with the help of conformal mapping and the single-vertex approach. The potential solution together with the electric field form the basic electrostatic solution of this work.

By considering band-gap narrowing and hetero-structures, the band-structure of the TFET is calculated. It forms the basis for the determination of the band-to-band tunneling distance, occurring at the channel junctions. Combining the electric field solution within the channel region with the determined tunneling distance a quasi two-dimensional WKB approach is introduced, which enables an estimation of the band-to-band tunneling probability individually for each point within the channel region, where band-to-band tunneling is possible. Based on the same wkb approach, an expression for the trap-assisted-tunneling probability is found. Carriers tunnel from mid-gap traps, located at the channel junctions, to the bands in the channel region.

In the last step of the model, the device current is calculated based on Landauer's transmission theory. Therefore, the carrier concentrations are calculated using Fermi statistics for each

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region. An integration over the current density in the channel region leads to the overall device current. This last calculation step completes the analytical two-dimensional double-gate TFET model, including all important physical effects occurring in these devices.

The different important solution steps of the developed model are firstly compared against TCAD Sentaurus simulation data. The dimensions of the simulated device are chosen to be similar to commonly used transistor technology. While considering short-channel effects, the two-dimensional electrostatic solutions are predicted well with the model. Versatile parameter changes are analyzed by comparing the resulting device current with the simulation data. Not only is the model able to predict changes in the devices geometry like channel length, channel thickness or insulator thickness but also changes in the doping profiles standard deviation and trap concentration. With the consideration of hetero-junctions, the model is able to capture even technologically advanced transistors with enhanced performance abilities.

Although the TFET is a promising candidate to be the successor of the current MOSFET technology, some performance challenges still have to be met. One of the major problems is the trade-off between a sufficient on-state current and a steep subthreshold slope, which requires a low off-state current. This work shows, that a combination of doping profiles and mid-gap traps at the channel junctions are the main performance determining effects within the TFET. The device can be optimized by realizing steep doping profiles with a low trap concentration. Further improvement can be achieved by introducing hetero-junction devices with a three-dimensional nanowire geometry.

The vast improvement of general transistor performance the last few years is mainly due to device miniaturization. Recently fabricated devices already reach channel lengths down to 14 nm. In these dimensions discretization effects gain influence on the device performance. In this thesis the random dopant fluctuation influence on the device threshold voltage is investigated and modeled. The general rdf model is able to capture the rdf influence on the gate voltage in TFET devices for a specific operating regime. A for MOSFET devices optimized rdf model is able to predict the rdf-based threshold voltage variation on the potential barrier for various channel lengths, channel doping concentrations and doping profile standard deviations at the channel junctions. By further investigating the rdf dependencies in both devices, the MOSFET current varies less compared to a TFET device. In the MOSFET rdf only has a direct influence on the potential barrier, which limits the device current. In TFETs, however, a variation of the potential near the channel junctions leads to more complex variations in tunneling distance and band-overlap position, and with that, a higher variation in device current. Optimization possibilities are steep doping profiles at the channel junctions, as well as low channel doping concentrations regardless of the device type.

The analytical models introduced in this work, although accurate end efficient, can not be

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implemented in a circuit simulator. In order to utilize the model, compact expressions for the introduced mathematical equations have to be found and implemented into a compact model. This can subsequently be implemented in a circuit simulator for first TFET-based circuit simulations. A first transition of the band-to-band current model into a compact form in Verilog-A was done in [73]. In order to demonstrate the numerical stability of the model, a basic circuit in form of a single stage inverter is simulated using complementary TFET logic, which stays in good agreement with the measurement data.

Since the geometric development aims for new performance enhancing three-dimensional structures like the nanowire, an adaption of this structure for the model is a high priority for future work.

References

[1] G. Busch, “Early history of the physics and chemistry of semiconductors-from doubts to fact in a hundred years,” *European Journal of Physics*, vol. 10, no. 4, p. 254, 1989.

[2] M. Faraday, *On a New Law of Electric Conduction; On Conducting Power Generally*. Royal Society, 1833.

[3] J. Weiss, *Experimentelle Beiträge zur Elektronentheorie aus dem Gebiet der Thermoelektrizität*. J. Weiss, 1910.

[4] A. H. Wilson, “The theory of electronic semi-conductors,” *Proceedings of the Royal Society of London A: Mathematical, Physical and Engineering Sciences*, vol. 133, no. 822, pp. 458–491, 1931.

[5] M. Riordan and L. Hoddeson, “The origins of the pn junction,” *IEEE spectrum*, vol. 34, no. 6, pp. 46–51, 1997.

[6] W. Shockley, “The path to the conception of the junction transistor,” *IEEE Transactions on Electron Devices*, vol. 23, no. 7, pp. 597–620, 1976.

[7] J. S. Kilby, “Invention of the integrated circuit,” *IEEE Transactions on electron devices*, vol. 23, no. 7, pp. 648–654, 1976.

[8] L. Esaki, “Discovery of the tunnel diode,” *IEEE Transactions on Electron Devices*, vol. 23, no. 7, pp. 644–647, 1976.

[9] L. J. Edgar, “Method and apparatus for controlling electric currents,” Jan. 28 1930. US Patent 1,745,175.

[10] L. J. Edgar, “Device for controlling electric current,” Mar. 7 1933. US Patent 1,900,018.

[11] M. M. Atalla, E. Tannenbaum, and E. Scheibner, “Stabilization of silicon surfaces by thermally grown oxides,” *Bell System Technical Journal*, vol. 38, no. 3, pp. 749–783, 1959.

[12] D. Kahng and M. Atalla, “Silicon-silicon dioxide field induced surface devices,” in *IRE Solid-State Device Research Conference*, 1960.

[13] K. Dawon, "Electric field controlled semiconductor device," Aug. 27 1963. US Patent 3,102,230.

[14] S. E. Thompson and S. Parthasarathy, "Moore's law: the future of si microelectronics," *Materials today*, vol. 9, no. 6, pp. 20–25, 2006.

[15] G. Moore, "The future of integrated electronics," *Fairchild Semiconductor internal publication*, vol. 2, 1964.

[16] G. E. Moore, "Progress in digital integrated electronics, digest of the 1975 international electron devices meeting," 1975.

[17] S. Thompson, M. Alavi, M. Hussein, P. Jacob, C. Kenyon, P. Moon, M. Prince, S. Sivakumar, S. Tyagi, and M. Bohr, "130nm logic technology featuring 60nm transistors, low-k dielectrics, and cu interconnects.," *Intel Technology Journal*, vol. 6, no. 2, 2002.

[18] T. Ghani, M. Armstrong, C. Auth, M. Bost, P. Charvat, G. Glass, T. Hoffmann, K. Johnson, C. Kenyon, J. Klaus, B. McIntyre, K. Mistry, A. Murthy, J. Sandford, M. Silberstein, S. Sivakumar, P. Smith, K. Zawadzki, S. Thompson, and M. Bohr, "A 90nm high volume manufacturing logic technology featuring novel 45nm gate length strained silicon cmos transistors," in *IEEE International Electron Devices Meeting 2003*, pp. 11.6.1–11.6.3, Dec 2003.

[19] K. Mistry, C. Allen, C. Auth, B. Beattie, D. Bergstrom, M. Bost, M. Brazier, M. Buehler, A. Cappellani, R. Chau, *et al.*, "A 45nm logic technology with high-k+ metal gate transistors, strained silicon, 9 cu interconnect layers, 193nm dry patterning, and 100% pb-free packaging," in *2007 IEEE International Electron Devices Meeting*, pp. 247–250, IEEE, 2007.

[20] M. Bohr and K. Mistry, "Intel's revolutionary 22 nm transistor technology," *Intel website*, 2011.

[21] S. Natarajan, M. Agostinelli, S. Akbar, M. Bost, A. Bowonder, V. Chikarmane, S. Chouksey, A. Dasgupta, K. Fischer, Q. Fu, *et al.*, "A 14nm logic technology featuring 2 nd-generation finfet, air-gapped interconnects, self-aligned double patterning and a 0.0588 μm^2 sram cell size," in *2014 IEEE International Electron Devices Meeting*, pp. 3–7, IEEE, 2014.

[22] ITRS, *International Technology Roadmap for Semiconductors 2.0 Executive Report*, 2015.

[23] D. J. Frank, R. H. Dennard, E. Nowak, P. M. Solomon, Y. Taur, and H.-S. P. Wong, "Device scaling limits of si mosfets and their application dependencies," *Proceedings of the IEEE*, vol. 89, pp. 259–288, Mar 2001.

[24] A. C. Seabaugh and Q. Zhang, "Low-voltage tunnel transistors for beyond CMOS logic," *Proceedings of the IEEE*, vol. 98, pp. 2095–2110, Dec. 2010.

[25] H. Lu and A. Seabaugh, "Tunnel field-effect transistors: State-of-the-art," *IEEE Journal of the Electron Devices Society*, vol. 2, pp. 44–49, July 2014.

[26] A. Seabaugh, C. Alessandri, M. A. Heidarlou, H. M. Li, L. Liu, H. Lu, S. Fathipour, P. Paletti, P. Pandey, and T. Ytterdal, "Steep slope transistors: Tunnel fets and beyond," in *Proc. 46th European Solid-State Device Research Conf. (ESSDERC)*, pp. 349–351, Sept. 2016.

[27] J. Appenzeller, Y.-M. Lin, J. Knoch, and P. Avouris, "Band-to-band tunneling in carbon nanotube field-effect transistors," *Phys. Rev. Lett.*, vol. 93, p. 196805, Nov 2004.

[28] S. Mookerjea, D. Mohata, R. Krishnan, J. Singh, A. Vallett, A. Ali, T. Mayer, V. Narayanan, D. Schlom, A. Liu, and S. Datta, "Experimental demonstration of 100nm channel length in0.53ga0.47As-based vertical inter-band tunnel field effect transistors (tfets) for ultra low-power logic and SRAM applications," in *Proc. IEEE Int. Electron Devices Meeting (IEDM)*, pp. 1–3, Dec. 2009.

[29] G. Dewey, B. Chu-Kung, J. Boardman, J. M. Fastenau, J. Kavalieros, R. Kotlyar, W. K. Liu, D. Lubyshev, M. Metz, N. Mukherjee, P. Oakey, R. Pillarisetty, M. Radosavljevic, H. W. Then, and R. Chau, "Fabrication, characterization, and physics of iii-v heterojunction tunneling field effect transistors (h-tfet) for steep sub-threshold swing," in *Proc. Int. Electron Devices Meeting*, pp. 33.6.1–33.6.4, Dec. 2011.

[30] L. Knoll, Q. T. Zhao, A. Nichau, S. Trellenkamp, S. Richter, A. Schäfer, D. Esseni, L. Selmi, K. K. Bourdelle, and S. Mantl, "Inverters with strained si nanowire complementary tunnel field-effect transistors," *IEEE Electron Device Letters*, vol. 34, pp. 813–815, June 2013.

[31] D. Sarkar, X. Xie, W. Liu, W. Cao, J. Kang, Y. Gong, S. Kraemer, P. M. Ajayan, and K. Banerjee, "A subthermionic tunnel field-effect transistor with an atomically thin channel," *Nature*, vol. 526, no. 7571, pp. 91–95, 2015.

[32] M. G. Bardon, H. P. Neves, R. Puers, and C. Van Hoof, "Pseudo-two-dimensional model for double-gate tunnel fets considering the junctions depletion regions," *IEEE Transactions on electron Devices*, vol. 57, no. 4, pp. 827–834, 2010.

[33] L. Zhang and M. Chan, "Spice modeling of double-gate tunnel-fets including channel transports," *IEEE Transactions on Electron Devices*, vol. 61, no. 2, pp. 300–307, 2014.

[34] A. Biswas, L. De Michielis, A. Bazigos, and A. M. Ionescu, "Compact modeling of dg-tunnel fet for verilog-a implementation," in *2015 45th European Solid State Device Research Conference (ESSDERC)*, pp. 40–43, IEEE, 2015.

[35] K. K. N. S. M. Sze, *Physics of Semiconductor Devices.* John Wiley & Sons, 2007.

UNIVERSITAT ROVIRA I VIRGILI
Two-Dimensional Analytical Modeling of Tunnel-FETs
Michael Gräf

[36] P. Stolk, H.-J. Gossmann, D. Eaglesham, D. Jacobson, C. Rafferty, G. Gilmer, M. Jaraiz, J. Poate, H. Luftman, and T. Haynes, "Physical mechanisms of transient enhanced dopant diffusion in ion-implanted silicon," *Journal of Applied physics*, vol. 81, no. 9, pp. 6031–6050, 1997.

[37] Synopsys, *TCAD Sentaurus*. Synopsys, Inc., c-2009.06 ed., 2009.

[38] J. Slotboom and H. De Graaff, "Measurements of bandgap narrowing in si bipolar transistors," *Solid-State Electronics*, vol. 19, no. 10, pp. 857–862, 1976.

[39] J. Del Alamo, S. Swirhun, and R. Swanson, "Simultaneous measurement of hole lifetime, hole mobility and bandgap narrowing in heavily doped n-type silicon," in *Electron Devices Meeting, 1985 International*, pp. 290–293, IEEE, 1985.

[40] H. S. Bennett and C. L. Wilson, "Statistical comparisons of data on band-gap narrowing in heavily doped silicon: Electrical and optical measurements," *Journal of applied physics*, vol. 55, no. 10, pp. 3582–3587, 1984.

[41] S. Jain and D. Roulston, "A simple expression for band gap narrowing (bgn) in heavily doped si, ge, gaas and gexsi1- x strained layers," *Solid-State Electronics*, vol. 34, no. 5, pp. 453–465, 1991.

[42] A. Tsormpatzoglou, C. A. Dimitriadis, R. Clerc, Q. Rafhay, G. Pananakakis, and G. Ghibaudo, "Semi-analytical modeling of short-channel effects in si and ge symmetrical double-gate mosfets," *IEEE Transactions on Electron devices*, vol. 54, no. 8, pp. 1943–1952, 2007.

[43] G. Wentzel, "Eine verallgemeinerung der quantenbedingungen für die zwecke der wellenmechanik," *Zeitschrift für Physik*, vol. 38, no. 6-7, pp. 518–529, 1926.

[44] H. A. Kramers, "Wellenmechanik und halbzahlige quantisierung," *Zeitschrift für Physik*, vol. 39, no. 10-11, pp. 828–840, 1926.

[45] L. Brillouin, "Remarques sur la mécanique ondulatoire," *J. Phys. Radium*, vol. 7, no. 12, pp. 353–368, 1926.

[46] A. Vandooren, D. Leonelli, R. Rooyackers, A. Hikavyy, K. Devriendt, M. Demand, R. Loo, G. Groeseneken, and C. Huyghebaert, "Analysis of trap-assisted tunneling in vertical si homo-junction and sige hetero-junction tunnel-fets," *Solid-State Electronics*, 2013.

[47] B. Bhushan, K. Nayak, and V. R. Rao, "Dc compact model for soi tunnel field-effect transistors," *IEEE Transactions on Electron Devices*, vol. 59, no. 10, pp. 2635–2642, 2012.

[48] M. Graef, T. Holtij, F. Hain, A. Kloes, and B. Iniguez, "Two-dimensional modeling of an ultra-thin body single-gate si tunnel-fet," in *Ultimate Integration on Silicon (ULIS), 2014 15th International Conference on*, pp. 101–104, IEEE, 2014.

UNIVERSITAT ROVIRA I VIRGILI
Two-Dimensional Analytical Modeling of Tunnel-FETs
Michael Gräf

[49] T. Krishnamohan, D. Kim, S. Raghunathan, and K. Saraswat, “Double-gate strained-ge heterostructure tunneling fet (tfet) with record high drive currents and« 60mv/dec subthreshold slope,” in *2008 IEEE International Electron Devices Meeting*, pp. 1–3, IEEE, 2008.

[50] D. H. Morris, U. E. Avci, R. Rios, and I. A. Young, “Design of low voltage tunneling-fet logic circuits considering asymmetric conduction characteristics,” *IEEE Journal on Emerging and Selected Topics in Circuits and Systems*, vol. 4, no. 4, pp. 380–388, 2014.

[51] Y. Lee, D. Kim, J. Cai, I. Lauer, L. Chang, S. J. Koester, D. Blaauw, and D. Sylvester, “Low-power circuit analysis and design based on heterojunction tunneling transistors (hetts),” *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 21, no. 9, pp. 1632–1643, 2013.

[52] M. Cotter, H. Liu, S. Datta, and V. Narayanan, “Evaluation of tunnel fet-based flip-flop designs for low power, high performance applications,” in *Quality electronic design (ISQED), 2013 14th international symposium on*, pp. 430–437, IEEE, 2013.

[53] E. Weber, *Electromagnetic fields, Vol.I., Mapping of fields.* John Wiley, New York, 1950.

[54] K. Simonyi, *Theoretische Elektrotechnik.* Deutscher Verlag der Wissenschaften, 1976.

[55] A. Kloes, *Analytische Modellierung mehrdimensionaler Effekte in Submikron-MOSFETs.* PhD thesis, TU Darmstadt, 1996.

[56] M. Schwarz, T. Holtij, A. Kloes, and B. Iñíguez, “Analytical compact modeling framework for the 2d electrostatics in lightly doped double-gate mosfets,” *Solid-State Electronics*, vol. 69, pp. 72–84, 2012.

[57] T. Dutta, Q. Rafhay, G. Pananakakis, and G. Ghibaudo, “Modeling of the impact of source/drain regions on short channel effects in mosfets,” in *Ultimate Integration on Silicon (ULIS), 2013 14th International Conference on*, pp. 69–72, IEEE, 2013.

[58] A. Kloes, M. Weidemann, D. Goebel, and B. T. Bosworth, “Three-dimensional closed-form model for potential barrier in undoped finfets resulting in analytical equations for v_T and subthreshold slope,” *IEEE Transactions on Electron Devices*, vol. 55, pp. 3467–3475, Dec 2008.

[59] A. Gnudi, S. Reggiani, E. Gnani, and G. Baccarani, “Semianalytical model of the subthreshold current in short-channel junctionless symmetric double-gate field-effect transistors,” *IEEE Transactions On Electron Devices*, vol. 60, no. 4, pp. 1342–1348, 2013.

[60] M. Graef, F. Hain, F. Hosenfeld, B. Iniguez, and A. Kloes, “Analytical approach to consider gaussian junction profiles in compact models of tunnel-fets,” in *Ultimate Integration on*

Silicon (EUROSOI-ULIS), Joint International EUROSOI Workshop and International Conference on, pp. 213–216, IEEE, 2015.

[61] A. Gehring, *Simulation of Tunneling in Semiconductor Devices.* PhD thesis, TU Wien, 2003.

[62] E. Gnani, S. Reggiani, A. Gnudi, and G. Baccarani, “Drain-conductance optimization in nanowire tfets,” in *Solid-State Device Research Conference (ESSDERC), 2012 Proceedings of the European*, pp. 105–108, IEEE, 2012.

[63] Y. Omura, S. Horiguchi, M. Tabe, and K. Kishi, “Quantum-Mechanical Effects on the Threshold Voltage of Ultrathin-SOI nMOSFETs,” *IEEE Electron Device Letters*, vol. 14, no. 12, pp. 569–571, 1993.

[64] G. Dewey, B. Chu-Kung, J. Boardman, J. M. Fastenau, J. Kavalieros, R. Kotlyar, W. K. Liu, D. Lubyshev, M. Metz, N. Mukherjee, P. Oakey, R. Pillarisetty, M. Radosavljevic, H. W. Then, and R. Chau, “Fabrication, characterization, and physics of iii-v heterojunction tunneling field effect transistors (h-tfet) for steep sub-threshold swing,” in *2011 International Electron Devices Meeting*, pp. 33.6.1–33.6.4, Dec 2011.

[65] L. Knoll, Q. T. Zhao, A. Nichau, S. Trellenkamp, S. Richter, A. Schäfer, D. Esseni, L. Selmi, K. K. Bourdelle, and S. Mantl, “Inverters with strained si nanowire complementary tunnel field-effect transistors,” *IEEE Electron Device Letters*, vol. 34, pp. 813–815, June 2013.

[66] G. Luong, S. Trellenkamp, Q. Zhao, S. Mantl, and K. Bourdelle, “Strained si nanowire gaa n-tfets for low supply voltages,” in *Ultimate Integration on Silicon (EUROSOI-ULIS), 2015 Joint International EUROSOI Workshop and International Conference on*, pp. 65–68, IEEE, 2015.

[67] Hraziia, A. Vladimirescu, A. Amara, and C. Anghel, “An analysis on the ambipolar current in si double-gate tunnel {FETs},” *Solid-State Electronics*, vol. 70, pp. 67 – 72, 2012. Selected Full-Length Papers from the {EUROSOI} 2011 Conference.

[68] C. Shin, X. Sun, and T.-J. K. Liu, “Study of random-dopant-fluctuation (rdf) effects for the trigate bulk mosfet,” *Electron Devices, IEEE Transactions on*, vol. 56, no. 7, pp. 1538–1542, 2009.

[69] F. Bonani, G. Ghione, M. R. Pinto, and R. K. Smith, “An efficient approach to noise analysis through multidimensional physics-based models,” *Electron Devices, IEEE Transactions on*, vol. 45, no. 1, pp. 261–269, 1998.

[70] A. Wettstein, O. Penzin, E. Lyumkis, and W. Fichtner, “Random dopant fluctuation modelling with the impedance field method,” in *Proceedings of International Conference on Simulation of Semiconductor Devices and Processes*, pp. 91–94, 2003.

UNIVERSITAT ROVIRA I VIRGILI
Two-Dimensional Analytical Modeling of Tunnel-FETs
Michael Gräf

[71] N. Sano, K. Matsuzawa, M. Mukai, and N. Nakayama, "On discrete random dopant modeling in drift-diffusion simulations: physical meaning of atomistic dopants," *Microelectronics Reliability*, vol. 42, no. 2, pp. 189–199, 2002.

[72] M. Graef, F. Hain, F. Hosenfeld, F. Horst, A. Farokhnejad, A. Kloes, and B. Iñíguez, "Comparative numerical analysis and analytical rdf-modeling of mosfets and dg tunnel-fets," in *Mixed Design of Integrated Circuits and Systems, 2016 MIXDES-23rd International Conference*, pp. 47–51, IEEE, 2016.

[73] F. Horst, M. Graef, F. Hosenfeld, A. Farokhnejad, F. Hain, G. V. Luong, Q.-T. Zhao, B. Iñíguez, and A. Kloes, "Implementation of a dc compact model for double-gate tunnel-fet based on 2d calculations and application in circuit simulation," in *Solid-State Device Research Conference (ESSDERC), 2016 46th European*, pp. 456–459, IEEE, 2016.

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