- Departament d'Enginyeria Electrònica -

PhD Thesis

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Wide Bandgap Semiconductors for MEMS and Related Process Technologies

A dissertation submitted to the department of electronic engineering and the committee on graduate studies of Universitat Autònoma de Barcelona in partial fulfilment of the requirements for the degree of doctor of philosophy by:

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MOTIVATION

It is nowadays difficult to imagine the life without transistors. Transistor is a sort of sandwich made up mainly with Silicon, a dielectric (generally the Silicon native oxide, Silicon dioxide) and a metal. None of our common modern electronic devices would exist without it. No affordable computers, phones, entertainment devices and medical equipment would be available and Internet probably would not exist. But this is not all, since several years, another transformation has begun, with MEMS. MEMS is the acronym of micro-electro-mechanical-system and refers to devices that range in size from the sub micrometer level to the millimetre level, and combines electrical and mechanical components. MEMS extend the fabrication techniques developed for the integration circuit industry to add mechanical elements such as beams, membranes and springs to devices.

This technology was limited during many years to in-house manufacturing or automotive products, such as inkjet print-heads or accelerometers in airbag sensors and it has been more recently applied to a raft of consumer devices and mobiles phones. The most famous examples of devices using such a technology are probably the iPhone from Apple and the Wii from Nintendo. The built-in accelerometer in these devices serves to detect motion and changes in orientation. But an explosion of possible applications is now moving to the industrial and medical instrumentation. With all this panel of new applications, the MEMS market is expected to tremendously grow and any company that is in semiconductors now must do MEMS. In past, the real applications started to exploit the transistor by 20 years after its invention. After 20 years of development the MEMS sector is not in a bad position. The main difference between the semiconductor and MEMS industry is that there has not been a platform MEMS technology on which you can base a number of different devices. Moreover, the industry is still learning, working with different laboratories, to establish a standard process for MEMS, to achieve a level of standardization similar to the CMOS technology in the semiconductor industry.

Transistors and MEMS are currently changing our world. Transistor opened the doors to the computation revolution. MEMS is now part of the evolution, lopening the doors to all about sensors, the sensing revolution. It is sure that transistor and MEMS will continue to drive product research and technological advances we can’t yet even begin to imagine. This is particularly true when imagining new devices with emergent technologies such as Wide Bandgap (WBG) materials, such as Silicon carbide (SiC) and III-nitrides (Gallium nitride, GaN, and Aluminum nitride, AlN), or Carbon-based materials, such as nanotubes and graphene. This will lead to transistors faster than the existing one, more resistant for operation in aggressive ambient, and will lead to computer processors hundred of times faster than the silicon-based products. Up to now, the dominant technology for transistors and MEMS remained the Silicon one, for

economical and technical reasons. However, depending on the aimed application, many other materials have superior electrical and mechanical properties relative to Si, such as SiC or GaN. The success of Si electronics is intimately lied to the high quality of insulating layers of silicon dioxide.
But there is now considerable evidence of the need for a semiconductor technology which exceeds the limitations imposed by Si across a wide spectrum of applications. WBG materials, such as SiC and GaN, offer the potential to overcome the harsh environment operation limitation of Si, both for MEMS and transistors devices.

During years, the WBG technology development was limited due to the difficulty in growth and processing of these semiconductors. However, in the past decade, special efforts have been put into the growth and processing aspects of SiC mainly for power devices, and III-nitrides for opto-electronical devices. As a result, the application of such materials both as MEMS or transistors based material has appeared attractive and becomes now clearly realistic.

These materials show no or very low reaction with molecules from the air, thus being a clear advantage respect to Si, for MEMS devices based on surface and small mass loads variation. The high Young's modulus of WBG materials enables them to achieve higher frequencies and quality factors than those obtained with Si resonant devices of identical geometry. The possibility to obtain crystalline or polycrystalline forms also allows to achieve low dissipation layers, thus resulting beneficial in reaching high quality factors.

An important point for WGB MEMS application is the entire compatibility with Si industry. In this sense, it is important to develop a technology fully compatible with the Si one, since Si electronics is still expected to dominate the market for several years. For this, some things are important, the first one being that the process has to be entirely realizable in traditional industrial equipment. This can be easily achieved if the WBG-based device is integrated with Si. In this sense, all the studied WBG resonators presented in this thesis were grown on Si substrate, fully compatible with the traditional Si processes. Moreover, to imagine a possible industrialization of WBG resonators, it is indispensable to dispose of the associated electronics, and thus transistors for eventual circuitry integration, such as the CMOS extensively used at ETSE/CNM [1-7].

Recently, Chung and al. from MIT have reported the first on-wafer integration of Si(100) MOSFETs and AlGaN/GaN HEMTs [8]. This could be an opening way for realizing AlGaN/GaN resonators with Si-integrated circuitry, or why not, with III-nitride circuitry. In fact, III nitrides can also offer piezoelectricity, and in the case of using AlGaN/GaN heterostructures as structural layer, a two-dimensional electron gas (2DEG) is created at the interface, that can be used for actuation/detection.

In such a way, in order to integrate transistor or possible electronic circuitry directly on the structural material of the mechanical part, following the same concept than the successfully Si cantilever integrated with transistors [9], GaN transistors have also attracted our attention. These GaN-based transistors have recently emerged as a possible alternative to the SiC or Si ones. Both GaN metal-oxide-semiconductor and AlGaN/GaN high-electron-mobility transistors (i.e. MOSFETs and HEMTs) could represent a solution for actuation/detection in GaN-based MEMS. Moreover, these devices are also highly interesting for power electronics, and actually the HEMTs ones seem more promising than MOSFETs due to the availability of the 2DEG at the interface.

OUTLINE OF THE THESIS

The attractive physical, electrical and mechanical properties of WBG materials are reviewed in a first part (*Chapter I*). We will see that the high mechanical, thermal, chemical and biochemical stability of the WBG materials enables applications in ambient where Si is limited. Moreover, the high Young modulus of the WBG materials favours their use in high sensitivity applications, such as mass sensors. All these excellent properties render the use of WBG materials very interesting for MEMS fabrication. However, their realization relies on the knowledge of the elastic properties, rupture and fatigue of the thin films materials, such as their internal residual constraint. Since WBG materials are sparse to obtain, compared to Si, it was required to verify the feasibility of such WBG devices.

To achieve this, we have first decided to realize SiC micromechanical devices based on cantilevers and bridges using the SiC/Si heterostructure, using research material from CRHEA (Valbonne, France) and LMI (Lyon, France). Therefore, more details about MEMS and the mechanical behaviour of test structures, which are the base for more complicated devices, are described in *Chapter II*.

Then in the following section, *Chapter III*, a review of the main WBG reported etching techniques is summarized, and we present the first tests performed at CNM. This allowed us to verify the feasibility of SiC and III-nitrides etching with the CNM equipments, but above all to orientate us to establish a first technological process for the realization of beam-based MEMS.

A summary of the realized devices using SiC is then provided in *Chapter IV*, demonstrating the advantages of SiC devices compared with Si. The study begins with the SiC/Si heterostructure as starting material, and follows with the use of SiC on insulated substrate, to avoid electrical leakage problems.

Then in the following parts, III-nitride materials were investigated. In *Chapter V*, AlN on Si was investigated as possible starting material for MEMS fabrication. Electrical measurements motivated us to study this research material as possible dielectric.

Finally, *chapter VI* mainly concerns the first steps realized at CNM into the GaN devices technology, for both MEMS and transistors application. For this, different technological steps such as cleanings, ohmic contacts formation and gate dielectric choice will be studied. The first GaN MOSFETs fabricated at CNM, and AlGaN/GaN HEMTs from CRHEA, will be also presented, compared and measured with temperature.

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1 CHAPTER I

GENERAL PROPERTIES OF WBG MATERIALS FOR MEMS (TRANSISTORS) APPLICATIONS

1.1 Silicon Carbide

The first descriptions of SiC were performed by Berzelius in 1824, in Sweden [1]. In 1891, while Achelson was tenting to find suitable material as abrasive as the diamond, he found a compound of silicon and carbon. The first SiC fabricated device was realized in 1907 and was a light emitting diode, with yellow, green and orange emission [2].

1.1.1 Crystalline structure

SiC crystallizes in more than 100 different structures with particular crystal symmetries, called *polytypes*, but with the same stoichiometry [3]. All the SiC polytypes are constituted of bi-layers Silicon-Carbon, only distinguished by the stacking sequence. The SiC structure is tetraedric, as shown in in figure 1.

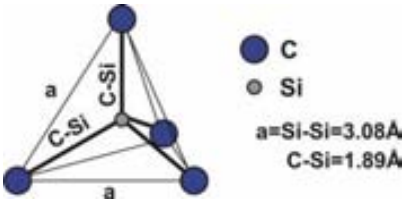

Figure 1. SiC tetraedric structure.

From a compact layer (or plane) A, it exists two possibilities of stacked sequence of the following layers (planes), either in B either or in C (figure 2).

Figure 2. Stacked sequence of layers B or C on an A layer.

The order of the planes stacking determines the types of close-packed structures and their symmetry properties. Then different symmetries, noted AB, ABC, ABCB, ABCACB… are possible and represent the periodicity of the polytype. The three more encountered symmetries are the *cubic* (C), the *hexagonal* (H) and the *rhombohedral* (R). In the figure 3 are represented some stacked sequences of different polytypes, with the corresponding Ramsdell notations (the sequence ABCB is written 4H-SiC). This notation is very useful for some polytypes. Composed by a numeric, the number of bi-layers representing the stacking sequences, followed by a letter defining the structure symmetry, this notation shows immediately its interest for example for the polytype 15R-SiC.
The 3C-SiC is formed by the sequence ABCABC that gives a cubic structure of zinc-blende type, and the 2H-SiC, an hexagonal structure of wurtzite type.
Each polytype presents different properties.

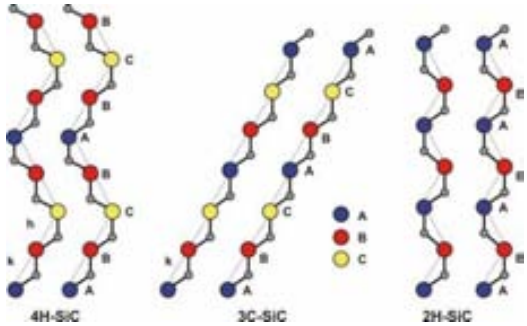

Figure 3. Stacked sequence of three polytypes.

1.1.2 Electrical, thermal and mechanical properties

The wide bandgap (WBG) semiconductors exhibit outstanding electrical, chemical and electrical properties, highly interesting for different applications. SiC, GaN and AlN (or AlGaN) also exhibit high hardness and Young and bulk modulus. WBG crystal quality is of particular relevance, resulting in clear difference properties for single crystalline, polycrystalline or amorphous materials.

Table I-1. General properties of WBG semiconductors with comparison to Si.

Material	**Si**	**3C-SiC**	**4H-SiC**	**6H-SiC**	**2H-GaN**	**2H-AlN**
Structural properties						
Structure	diamond	Zc-blende	wurtzite	wurtzite	wurtzite	wurtzite
Lattice constant (Å)	5.43	4.34	a : 3.07 c : 10.05	a : 3.08 c : 15.12	a : 3.18 c : 5.18	a : 3.11 c : 4.98
Density ($g.cm^{-3}$)	2.33		3.21		6.15	3.23
Density (cm^{-3})	5×10^{22}		9.6×10^{22}		8.9×10^{22}	9.6×10^{22}
Electrical properties at 300K						
Bandgap Eg (eV)	1.12	2.4	3.2	3	3.44	6.28
n_i (cm^{-3})	10^{10}	1.5×10^{-1}	8.2×10^{-9}	2×10^{-6}	1.9×10^{-10}	10^{-31}
Breakdown field ($V.cm^{-1}$)	2.5×10^{5}	2×10^{6}	3×10^{6}	3×10^{6}	3.3×10^{6}	1.5×10^{6}
Electron mobility ($cm^2.V^{-1}.s^{-1}$)	1400	750	800	370	1000	300
Hole mobility ($cm^2.V^{-1}.s^{-1}$)	400	50	115	90	350	15
Electron drift velocity ($cm.s^{-1}$)	1×10^{7}	2.5×10^{7}	2×10^{7}	2×10^{7}	2.5×10^{7}	1.8×10^{7}
Dielectric contant ε_r	11.8		9.7		9.5	8.4
Thermal and mechanical properties at 300K						
Melting Temperature (°C)	1500		3100		2500	2200
Thermal conductivity ($W.cm^{-1}.K^{-1}$)	1.5	5	5	5	1.3	2.85
Hardness ($kg.mm^{-2}$)	1000	3980	2130	2930	350	1100
Thermal dilatation coefficient (K^{-1})	2.6×10^{-6}	3.2×10^{-6}	a : 3.3×10^{-6} c : 3.2×10^{-6}		a : 5.6×10^{-6} c : 3.2×10^{-6}	a : 4.2×10^{-6} c : 5.3×10^{-6}
Young modulus (GPa)	170	350-600	450	300-500	350	300-350

The available information in literature is in many cases sparce and is also in some cases contradictory. This is in part due to measurements on samples of widely varying quality. Table I-1 resumes the main properties of the SiC and III-nitrides used in this work. For SiC, the properties of the most important three polytypes are presented.

The wide bandgap of SiC renders it an ideal candidate for operation at elevated temperatures. Silicon is limited at temperatures around 180ºC while SiC allows operation up to 600ºC. Another advantage of SiC is its excellent thermal conductivity (5 $W.cm^{-1}.K^{-1}$). It is more than 3 times superior to the Si one (1.5 $W.cm^{-1}.K^{-1}$), being similar to the Copper Cu (around 4 $W.cm^{-1}.K^{-1}$), thus allowing a rapid evacuation of the heat produced in operating devices. Moreover, SiC is chemically inert. Only some concentrated acid or basic solutions, such as HF or KOH, at elevated temperatures, can etch away the SiC surface (cf. *Chapter 3*). It is naturally less sensitive to radiations than Si, and possesses hardness 2-4 times superior to the Si one. The high values of the critical field and electron drift velocity allow higher operation frequencies and higher breakdown voltages. Mechanically, SiC possesses good properties, high hardness and Young modulus.

1.1.3 Growth on Si

Traditionally, for devices realization such as MOSFET, self-standing SiC substrates are used. 4H or 6H substrates with different kind of epitaxial layers, with different orientations (11-20, 000-1) are commercially available, CREE currently providing materials of high crystalline quality. The cubic polytype is sparser available as freestanding substrate, and not commercially available. In fact, a variety of different substrates can be used for the growth of 3C-SiC. The most important requirement is the growth temperature that can limit the substrate choice, depending of the desired crystalline quality. For polycrystalline layers, practically no limitations exist in the choice of substrates. Moreover, between the different SiC polytypes, only the cubic type can be grown on silicon substrate, by far the most commercially available. In fact it has been the most used method to produce SiC films for use in MEMS applications. Few exceptions concerned other polytypes for MEMS applications. For this reason, the following explanations will only concern cubic SiC growth on Si (or related) substrate. It is important to note that 3C-SiC on Si is a research material since it is not commercially available. Moreover it has recently gained interest not only for MEMS applications but also for microelectronics applications [4] and several projects concerning 3C MOS and MOSFET studies are currently in course.

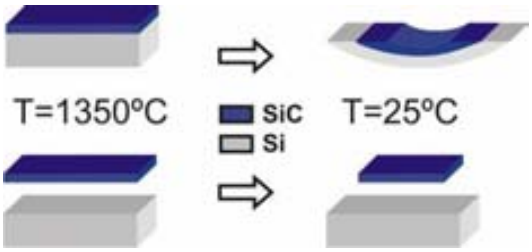

Figure 4. SiC/Si thermal mismatch.

SiC growth from a stoichiometric melt is not feasible due to thermodynamic reasons because it sublimes at T>2800ºC, therefore vapour phase epitaxy is needed for film growth. The chemical vapour deposition (CVD) method is the preferred technique to grow 3C-SiC films on Si substrates. However, due to the significant difference of the thermal expansion coefficients and the 20% misfit between Si and 3C-SiC the defect density in these films is high, and high stress levels and bowing are often observed, as it is illustrated in figure 4. Progress has been achieved recently in defect reduction at the interface by studying the temperature of the growth process, the Si substrate orientation, etc.

Briefly, the CVD system consists of a horizontal hot wall reaction chamber. For samples grown at CRHEA, the typical precursor gases are silane (SiH_4) and propane (C_3H_8) as Si and C sources respectively and hydrogen as carrier gas. The carbonization process, i.e. the Si surface preparation for SiC growth, is carried out at specific temperature reached in few minutes. For carbonization, only hydrogen and propane gases are introduced on the heated substrate. After the carbonization step, the substrate is heated to the required growth temperature, while a mixture of silane, propane and hydrogen are introduced into the reactor. A typical CVD growth process is described in figure 5. Doping can also be performed during the growth. For achieving an n-type region, introduction of phosphorus or nitrogen can be realized, while aluminium is typically used for p-type, but being much more difficult to achieve. It has to be noted that usually the obtained 3C-SiC is always unintentionally n-type doped (due to the nitrogen contamination coming from the used materials), thus also complicating the p-type doping.

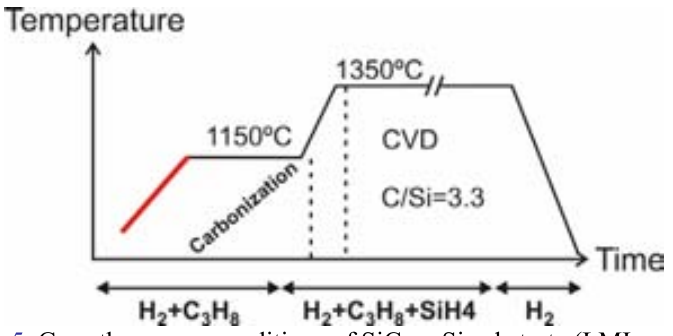

Figure 5. Growth process conditions of SiC on Si substrate (LMI process).

The most common defects in the 3C-SiC layers are stacking faults (SFs), microtwins (MTs) and anti-phase boundaries (APBs).

1.1.4 SiC MEMS

A resume of the main results concerning the reported 3C-SiC MEMS is given in Table I-2. From this table, we can note that the main reported works concerned polycrystalline SiC, easier to obtain and with less resulting stress between the two materials. Other works also considered amorphous SiC. Single crystalline was also reported and some devices fabricated. Moreover, the main commonly actuation principles were employed with SiC (cf. *Chapter 2*).

Most of the reported SiC electrostatic resonators with lateral displacement were comb drive-based structures (Table I-2), operating in vacuum ambient. However, many applications require operation at atmospheric pressure and single cantilever-based structure allows reduced mass, in order to achieve higher sensitivity and quality factor. Other SiC electrostatic structures cantilever or bridge-based were designed for vertical displacement but some of them with full area metal deposition, thus affecting the SiC resonance frequency by added mass. Other devices, in general with submicron thicknesses, also used magnetomotive actuation, requiring a complicated set-up to generate high magnetic field.

From all these reported results, it is clear that electrostatic actuation is actually the best actuation principle for SiC MEMS, thus following the same way that Si MEMS. Actually the best material for Si electrostatic-based MEMS is the SOI-based one.

Table I-2. Main reported results concerning 3C-SiC MEMS.

Materials	Structure*			Dimension (µm) (L×w×t)	*f* (MHz)	*Q*	Environment	E (GPa)	stress (Mpa)	Ref.
polySiC/Si_3N_4/SiO_2/Si	B	E	V	(51-110)×0.9×0.7	1.5-4	490	17K, 6T, UHV	385-512	73-171	[5,6]
polySiC/Si (and polySiC/SiO_2/Si)	CB	E	L	(50-1000)×10×1 for a cantilever	0.02-0.07	590	1mtorr/ambient	710	472	[7]
single SiC/Si	C	E	L	40×(1-2.5)×3.3	1-2.5	100-133	ambient	480	<200	[8] this work
polySiC/polySi/SiO_2/Si	CB	E	L	2 µm thick	0.01-0.028	25-152 (ambient) 57828-107926 (vacc.)	ambient/vacuum	250-427	NR	[9]
NiCr/polySiC/SiO_2/Si (NiCr/polySiC/Si)	BI	E	V	(25-200)×15×3 --- 2 µm thick (NiCr 250 nm)	0.066-1.729	NR	NR	NR	NR	[10]
Pt/single SiC/Si (NiCr/polySiC/SiO_2/Si)	BI	ET	V	200×15×3 (50×34×2) - Pt 500 nm (NiCr 280 nm)	0.117 (0.897)	NR (estimated arround 2000 and 400)	RT, 1mbar	NR	NR	[11]
Au/single SiC/Si	BI (U-type)	PR		(0.6-33)×(0.4-5)×0.1 - 70 nm SiC thick + 30 nm Au	0.052-127	15-400 (500-1000)	ambient/vacuum (0.01torr)	440 (Au 78)	??	[12]
single SiCOI	CB	E	L	2 µm thick	~0.042	10000	15 µtorr	359	NR	[13]
Au/Ti/single SiC/Si	BI	M	V	(30-160)×4×0.2 (Au/Ti 150-250 nm)	0.01-0.38	30-110	ambient, 0.5 T	NR	NR	[14]
Al/SiC	BI	M	V	12×100 nm ×30 nm thick (30-195 nm Al)	10.41	~2000	vacuum	410 (68 for Al) --- assumed	189 (-49 for Al)	[15]
Single SiC/SOI (SiC/SIS)	C	E	L	40×(1-2.5)×3	1.3-2.9	130	air	450	150	[16] this work

***Structure (type, actuation, movement)**
BI: bi-cantilever; CB: comb drive; C: cantilever; B: bridge
E: electrostatic; ET: electro-thermal; PR: piezoresistive; M: magnetomotive
V: vertical; L: lateral
NR: not reported

1.2 III-nitrides

1.2.1 Historical

The first descriptions of GaN were reported by Johnson et al. [17] in 1932. In 1938, Juza et al. [18] also synthesized GaN by passing ammonia over hot gallium. Curiously, the first reported GaN device, was, as for SiC, a LED and was reported in 1971 [19]. Since then, GaN especially attracted researchers to use it for application in optoeletronics. GaN has also been recently considered for power electronics application. AlN was discovered in 1862 by Brieglib et al [20], and was first synthesized in 1877 by Mallet et al. [21]. AlN is an interesting material for application in microelectronics and has recently found use in opto-electronic devices, as dielectric, as substrate and as piezoelectric material and for III-nitrides heterostructures. The first AlN device was recently reported by Taniyasu et al [22] and consisted in a LED emitting in UV.

1.2.2 Crystalline structure

Three crystalline forms of GaN and AlN (and III-nitrides generally, including InN and AlGaN) can be found: wurtzite (hexagonal), Zn-blende and rock-salt (NaCl), the most thermodynamically stable at ambient conditions being the wurtzite one. Like SiC, the structure is tetradric (figure 6).

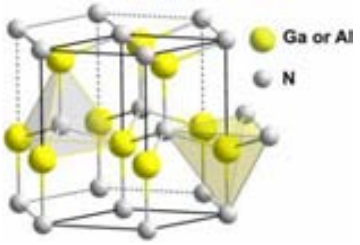

Figure 6. GaN or AlN wurtzite form.

Both zinc-blende and wurtzite structures lack a center of inversion and thus possess a polar axis which determines lattice orientation ([0001 and [111] direction for wurtzite and Zc-blende respectively). As a result the crystals are piezoelectric and properties of the (000-1) and (0001) crystal faces differ significantly.
Consequently, III-nitrides exhibit excellent piezoelectric properties and their use in acoustic devices has been reported with poly or single crystals [24]. Usually, works with piezoelectric materials mainly relied on ceramics such as PbZrTiO (PZT), quartz or polymers, but thin film AlN (and recently ZnO) begin to be considered for several applications requiring electronics integration, biocompatibility, integration to MEMS/NEMS and harsh ambient operation.

1.2.3 Electrical, thermal and mechanical properties

The available information in literature on the physical properties of III-nitrides is in some cases still in progress, and thus still sometimes controversial. This is in part due to measurements on samples of widely varying quality. The main properties of the III-nitrides are detailed in Table I-1.

GaN is a chemically stable compound exhibiting significant hardness. For this reason, it was attractive as protective coatings. It is an excellent candidate for devices operating at high temperature, thanks to its large bandgap. However, during years, despite its good mobilities values, close to the Si ones, no development in GaN technology was made mainly due its high stability impeding any kind of efficient and useful etching for devices fabrication.

AlN also has interesting mechanical and electronic properties. For example, amorphous AlN is highly interesting for Si electronic packaging since it is very hard, has high thermal conductivity, resistance to high temperature and almost all chemical products. Its wide bandgap has also always attracted researchers to test it as an insulating material. AlN maintained its presence as an important semiconductor thanks to it piezoelectric properties, for surface acoustic wave devices. More recently, AlN has regained high interest due to its ability to form alloys with GaN producing AlGaN and allowing the fabrication of AlGaN/GaN devices. Mechanically, AlN is interesting since it has an elevated Young's modulus, and it is very hard.

As mentioned above, the particularity of III-nitrides is the possibility to grow ternary nitride layers ($Al_xGa_{1-x}N$) with tailored properties such as the gap energy. This renders III-nitrides suitable compounds for high temperature and optoelectronic devices, but also using hetero-junctions devices. The spontaneous polarization field is an inherent physical property of wurtzite semiconductors, having a polar-atomic arrangement along the c-axis with ionic chemical bonds. This polarity allows to obtain a two dimensional electron gas (2DEG) at the interface of an AlGaN/GaN heterostructure. The 2DEG formation is the result of the generation of combined polarization fields, the spontaneous polarization in AlGaN and GaN but also to the piezoelectric polarization in AlGaN, leading to the existence of a 2DEG without any doped layers. This is highly interesting, and is the main difference and advantage compared with the other III-V compounds heterostructures like the ones made on AsGa.

1.2.4 Growth on Si

A variety of substrates can also be used for the growth of III-nitrides. Once again, the most important requirement is the growth temperature that can limit the substrate choice, depending of the desired crystalline quality. For polycrystalline layers, practically no limitations exist in the choice of substrates. Silicon substrates are very attractive not only because of their high quality, availability and low cost but also for the possibility of integration of Si-based electronics with wide bandgap semiconductor devices [25]. Both Zc-blende and wurtzite GaN and AlN epilayers have been grown on Si by Vapor phase methods such metal organic chemical vapour deposition (MOCVD or MOVPE) or molecular beam epitaxy (MBE). Usually ammonia is used as nitrogen precursor and the metal precursor species are trimethylgallium (TMG) and trimethylaluminum (TMA); silane can also be used to provide n-type doping with

silicon. TMG and TMA are only used by MOCVD, and for MBE, one uses metallic Al of Ga.

However, due to the significant difference of the thermal expansion coefficients and lattice mismatch between Si and III-nitrides, the defect density in these films is high, and high stress levels and bowing are often observed, leading often to cracks when the film thickness exceeds a critical value (typically 1 µm).

Some attempts of single crystalline GaN growth on Si at CRHEA, by MBE, for MEMS application, resulted in a high tensile residual stress, with a high density of defects and pits.

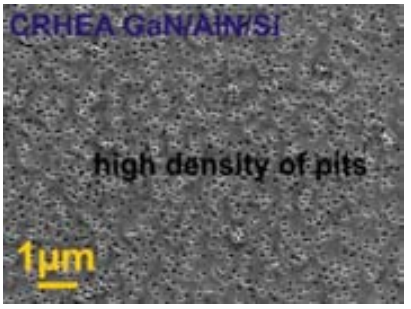

Figure 7. SEM image showing the GaN surface obtained from growth on Si substrate, with only a thin AlN buffer layer.

Studies are in course to grow GaN on a 3C-SiC on Si substrate by means of carbonization, such as in the 3C-SiC growth.

The used technique for reducing stress levels obtained in GaN layers consisted in growing thin AlN layers directly on Si followed by GaN deposition. In order to achieve the wurtzite structure, the (111) orientation is employed.

Usually, a large number of extended defects such as dislocations, stacking faults and twins are observed. Typically, AlN buffer layers, grown at high temperature (900-1100ºC) represent the most commonly scheme to grow GaN on Si. However, in most cases, GaN grown using just a single high-temperature AlN buffer produces cracks during cooling down to room temperature, or high density of pits as observed in the SEM image of figure 7. Then to reduce them, a buffer layer based on alternating various AlN and GaN layers is sometimes used.

Progress has been achieved recently in defect reduction at the interface by studying the temperature of the growth process, the Si substrate orientation, etc [26]. Other methods to reduce stresses in GaN layers have been reported, consisting in growing low-temperature AlN buffer, thus achieving relaxed layers.

1.2.5 III-nitrides MEMS

Compared with SiC, III-nitride MEMS have been less reported. Nevertheless this material offer similar mechanical properties to SiC, but also allows further detection techniques, due to the piezoelectricity, and to 2DEG created at the interface of nitrides heterostructures.

Only recently III nitride materials have regained high interest and many recent work reported interesting results, mainly due to the high piezoelectric coupling efficiency of nitrides, giving them high potential for MEMS fabrication.

A summary of the main works concerning III-nitride MEMS can be seen on Table I-3.

Table I-3. Main reported results concerning III-N MEMS.

Materials	Structure*		Dimension (µm)	*f* (MHz)	*Q*	Environment	E (GPa)	stress (Mpa)	Ref.
Single AlN/Si	B	M	(3.9-5.6)×(0.2)×0.17 (+Au)	82	21000	vacuum	345	NR	[27]
AlN/Si	B	M	(250-2)×(4-0.5)×0.2	0.02-5	NR	v	NR	NR	[28]
GaN/AlN/Si	B,C	--	(50-200)×(2-20)×(??) µm	NR	NR	NR	352	730-890	[29]
Mo/AlN/Mo/Si3N4/Si	B	PZ	350×80×2	NR	NR	NR	NR	300-700	[31]
AlGaN/GaN/AlN/GaN/AlN/Si	C	2DEG	(80-200)×(100)×1.5	NR	NR	NR	250	125	[34]
AlN/Si	C/B	P[a]	(220-10)×(20-10)×0.2	0.03-1	150-1000	air	300	340-1000	[35] this work
AlGaN/GaN/Si (GaN/Si)	various	2DEG	250×250×1 (accelerometer)	NR	NR	NR	NR	698-93	[36]
Mo/AlN/Mo/Si3N4/Si	B	PZ	(300-500)×(60-100)×1.93(0.15Mo+0.8AlN+0.15Mo+0.03Ti+0.8Si_3N_4)	2.23 (highest value)	NR	NR	NR	600	[37]
Mo/spuAlN/Mo/spuAlN/Si	C/B	PZ	(4-6)×0.9×0.32 (0.02AlN+0.1Mo+0.1AlN+0.1Mo)	80	960 (9.1 MHz) - 670 (80 MHz)	5 mtorr	329-345	NR	[38]
AlGaN/GaN/Si	B	2DEG	(10-1000)×(2-10)×0.68	0.2-8.1	100	air	NR	~800	[39]
AlGaN/GaN	B	2DEG	100×5×?	1.05	180	air	NR	NR	[40]

Structure (type, actuation)
C: cantilever; B: bridge
P[a]: piezoelectric (extern); PZ: piezoelectric; M: magnetomotive; 2DEG: 2D electron gas
NR: not reported

The first studies about AlN consisted in fabricating a pure mechanical structure, such as the bridges reported by Cleland [27] from Caltech, to take advantage of the low density and high Young modulus of this material. It was the first time that a mechanical AlN resonator oscillated at a frequency of 80 MHz. However measurements were only possible in vacuum to detect such a resonance. Since then, few works reported pure AlN mechanical resonator. Only a group from TU Ilmenau [28] pursued this topic, in order to demonstrate a possible sensing in air. However, these devices required a thin deposition of a metal layer to use magnetomotive actuation and thus requiring a complicated set-up to generate high magnetic field. GaN also interested the MEMS community with its mechanical properties, and have recently been fabricated using either AlN [29] or Si substrate as sacrificial layers [30].

Another important step was the use of the piezoelectric properties to actuate a bridge of sputtered AlN [31] sandwiched between 2 Mo electrodes and insulated from the substrates by Si_3N_4. The same concept was used with SiC cantilevers [32-33], however, few reports exist about such applications combining SiC and AlN which constitutes a promising heterostructure for WBG MEMS.

Another interesting way, but rarely reported, is the use and integration of a 2DEG in MEMS. This opens new sensing principle for both actuation and detection. During years, this was impeded due to the difficulty of selectively etching either the substrate or a sacrificial layer. However, recent advances in growth of AlGaN/GaN on

Si open the way to easily etch the Si substrate without damaging it (and even SiC recently [cf. *Chapter 3*]). Zimmermann was the first to report an integrated HEMT structure on a mechanical cantilever [34]. Higher sensitivity was observed when the gate is biased with a voltage close to the pinch-off.
Recently, the III nitrides have highly attracted the MEMS community and important progresses have been realized, in part due to the improvement in quality of the grown material. Different structures have been developped, taking advantages of the mechanical and piezoelectric properties, but also of the 2DEG formed at the interface. Recently we have demonstrated that AlN, despite its high stress, is well suited to realize large area MEMS/NEMS by two different processes [35]. The clear advantage of these strained resonators is their improved sensitivity. Lv [36] has also demonstrated that GaN is also well suited for large area GaN devices. Gonzalez [37] used sputtered AlN to fabricate piezoelectric resonator for mass sensing. Karabalin from Caltech [38] also reported an AlN piezoelectrical resonator using sputtered AlN sandwiched between 2 Mo electrodes thus demonstrating the efficiency of sputtered AlN for NEMS. The creation of a 2DEG and thus the integration of HEMTs into resonators was improved recently by Brucker [39] and Faucher [40]. This principle is actually the more promising since it could allow the integration of HEMT and resonators during the fabrication. Actually at CNM, further investigations are in course to realize a suspended HEMT structure.

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2 CHAPTER II

MEMS PRINCIPLE AND OPERATION

2.1 MEMS structures

MEMS cover an elevated number of possible applications, and can thus appear in very different geometries, using different operation principles.
Most miniaturized MEMS to be integrated into small sensors are based on two basic structures: beams (cantilever, bridges...) [1] and membranes [2]. Other more complex structures exist (figure 1) such as comb drives [3], micromotors [4] etc… but will not be considered here.

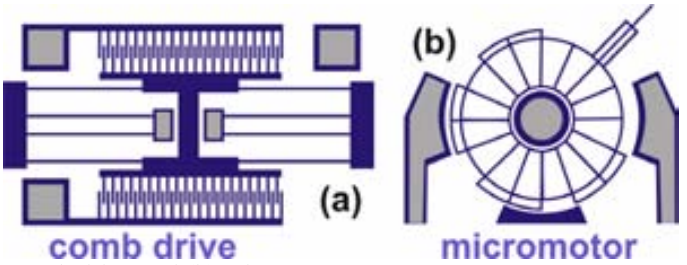

Figure 1. (a) Comb drive and (b) micromotor structure.

Membranes

Membranes are thin self-standing layers and have mainly a square or circular geometry. They are very interesting due to their large area, and thus, their ability to be used as large suspended functional layers. Usually, bulk micromachining from the rear side of the wafer is employed. Therefore for their fabrication it is not required any etch of the functional layer. Some applications are strain sensors, pressure sensors, thin film resonators and micropumps. The read-out of the sensor can be piezoresistive [5], piezoelectric [6], capacitive [7] and more recently by a confined 2DEG (2 Dimensional Electron Gas) in an AlGaN/GaN heterostructure [8] scheme during the deflection of the membrane.

Beam

Beam can have different appearances, singly clamped (cantilever type), coupled (U-type or V-type cantilevers) or doubly clamped (bridge type).
The main application of cantilevers is atomic force microscopy (AFM). Usually AFM cantilevers are fabricated by Si bulk micromachining techniques [9], while integrated cantilevers for sensor applications use surface micromachining [10]. Traditionally, the deflection is detected using optical methods, using the four quadrant photodiode (as the one developed for AFM) or by interferometry. More recently electrical methods such as the capacitive sensing have been intensively used for Si cantilevers. The main applications for cantilever are strain, temperature and chemical sensors. The sensitivity can be improved using resonant operation.
Bridges are usually fabricated by surface micromachining. Their applications are also small sensors, but also RF devices. Such as the cantilevers, resonant mode operation is also often used.

Resonators/Oscillators

The sensors based on membrane or beam can operate in static (DC) or resonant (AC) mode. In the DC mode, the value to measure induces a continued deflection of the mechanical structure. Cantilevers used as biosensors are largely used in such a mode. In the AC mode, the principle consists in an oscillation of the mechanical structure, obtained by an external excitation, thus obtaining a resonant state. The value to measure modifies this resonance. Therefore, resonant sensors are systems oscillating at a certain frequency. These devices are very interesting for high precision sensors such as mass sensing application [11]. In the field of communication circuits, these structures have been widely used in particular as filters and reference oscillators [12, 13]. Cantilevers and beams usually oscillate in the vertical or lateral direction (figure 2). In all these devices, electrical energy is converted into mechanical energy by exciting one resonant mode. The resulting displacement is then converted directly (by one of the integrated detection scheme) or indirectly (for example optically) into an electrical signal. In the next section some of the major possible actuation/sensing mechanisms are introduced.

Figure 2. (a) Vertical and (b) lateral cantilever vibration mode.

2.2 Actuation/detection techniques

The main actuation and detection techniques used in MEMS are summarized in this part. More details can be found in [14].

2.2.1 Actuation techniques

Electrostatic: the resonant state is obtained with a variable electric field applied between the resonator and another structure. This structure can be either the substrate for a vertical vibration, or a parallel electrode for a lateral vibration. Electrostatic actuation is useful for low-power consumption, is well controllable, fast and requires simple structures.
Thermal: a layer of a material with a different thermal expansion coefficient is deposited on the resonator surface. By heating, a stress (compression/tension) in each of the bonded materials is generated thus inducing the movement of the mechanical structure. Displacement is large (the generated forces are greater) but the consumed power is also higher than electrostatic or piezoelectric methods. This technique is easy to implement but the response times are very long.
Magnetomotive: usually a thin layer of a material sensible to external magnetic field is deposited on the resonator surface. However this method requires a heavy set-up under high magnetic fields (1-10 Tesla).
Piezoelectric: deformation is induced by applying an alternative voltage to a piezoelectric material. This piezoelectric layer is usually deposited on the structural material (constituting the resonator).

2.2.2 Sensing/Detection techniques

Capacitive: it is based on the measurement of the capacitance change induced by the deformation of the movable mechanical part (membrane or beam).
Piezoresistive: it is based on the use of resistors, which vary with the strain induced by the deformation.
Inductive: it is based on the generated voltage when a conductor is moved into a magnetic field.
Optical: it is usually based on the use of external methods such as interferometric techniques.

2.3 Why SiC and III-nitride MEMS?

Technology is very mature for Silicon and it is actually the dominant technology for MEMS. Accelerometers, inkjet printer heads, micromirrors for projection were the first commercialized MEMS devices [15-17]. An important variety of sensors, most of them for the automotive industry, have also been developed. Aerospatial industry is also requiring more and more MEMS. However, in many cases, this increasing demand mainly concerns devices operating in harsh environment, at elevated temperatures and/or pressures, or in corrosive ambient. This is the first limitation of the conventional Silicon-based technology. Si requires complicated protection or encapsulation to operate under demanding conditions. Moreover, for biomedical applications, the use of Si is limited since it exhibits low biocompatibility.

According with this, WBG semiconductors offer the possibility to fabricate devices with better reliability and resistance in harsh environment, or operation in ambient where Si cannot be used. In general, WBG materials are less reactive to air molecules when compared with the Si, which is important for sensing at the surface. Moreover, WBG materials have the particularity of having an elevated Young's modulus, which is also an important feature. This allows the achievement of higher frequencies and quality factor in resonant devices, for the same geometrical dimensions.

In addition, new opportunities and concepts arise when using these new materials. SiC presents the highest Young's modulus, AlN the highest piezoelectricity, and can also be used an insulator. GaN is particularly interesting when combined in heterostructure with AlN or AlGaN, thus inducing a 2DEG at the interface. Combining these materials and their respective advantages would allow to create optimized MEMS.

Compared with Si, very few MEMS have been fabricated using SiC or III nitrides. This was mainly due to the WBG material quality which was no enough to envisage fabricating devices. Recently, thanks to the progress realized during the last decades in growth and technology, these materials come back to the MEMS scene. However, further investigations still have to be performed. For example, the etching, which is particularly important for WBG MEMS fabrication, needs optimization, and is still under research. But, another important step is the development of an efficient WBG switch (transistor). Actually the clear advantage of Si is the possible monolithical integration to the existing technologies of electronic devices, such as complementary-metal-oxide-semiconductor (CMOS) circuitry. It appears evident that in a near future, with optimized WBG technology, and with efficient WBG switch (transistor), the first WBG MEMS devices should be commercially available.

2.4 Oscillators

Resonators are systems vibrating when they are submitted to an excitation force. A notable increase of the oscillation amplitude can be noted when approaching to excitation frequencies. When the oscillations are maximal, the frequency is called ***resonance frequency***. Resonance frequencies are characteristics of the stiffness, mass and vibration mode of the structure. But the stiffness of such a structure depends on its geometry, and also of the elastic properties and potentially of the internal constraints of the structural material. Thus, for a structure with fixed geometry and mass, resonance frequency measurements allow to determine the elastic properties, and in some cases, the internal mechanical constraint of the material.

Vibration amplitude at resonance essentially depends on the damping of the surrounded ambient, damping of internal friction in the materials constituting the structure, and energy losses in clamping areas.

To understand the operation of resonant structures such as cantilevers, bridges or more complicated structures (based on these last ones), it is first necessary to modelling in a simple way an oscillating system. Mainly three approaches have been reported in literature. The first one is based on the energy conservation method, also named Rayleigh-Ritz method [18] but was not developed in this work. Finite element methods (FEM) are also reported and consist in meshing the microstructure in a finite number of elements, elements which have a known behaviour for a finite number of parameters. This method is very interesting since it allows finding approximations for the resonance frequencies and their associated modes. It was widely used in this thesis but will be not detailed here. The other reported method is an analytical method (Euler-Bernouilli) and allows to calculate the resonance frequencies resolving the differential equation of the movement satisfying the boundary conditions. This method is well adapted for simple devices.

2.4.1 Driven damped oscillator

The simplest model for such a system is the damped oscillator driven by an externally applied force. Such a system can be modelled by a mass-spring-damper system, i.e., a mass *m* attached to a spring of stiffness *k*, and damper *c* (figure 3).

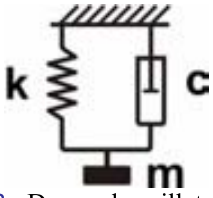

Figure 3. Damped oscillator model.

A viscous damper will be considered, i.e., the damping (friction) force is proportional to the instant velocity with a factor *c* (viscous damping coefficient).

If an external oscillatory force $f = F_0 \cos \omega t$ with amplitude F_0 and pulsation ω is applied to the mass m, the mass movement is:

$$m\frac{d^2x}{dt^2} + c\frac{dx}{dt} + kx = F_0 \cos \omega t \qquad \text{Eq. 2.1}$$

A particular solution of this equation in form of $x_p(t) = X.\cos(\omega t - \phi)$ gives for X and ϕ:

$$X = \frac{\delta_{st}}{\sqrt{(1-(\omega/\omega_n)^2)^2 + (1/Q)(\omega/\omega_n)^2}} \text{ and } \phi = \arctan\left(\frac{(1/Q)(\omega/\omega_n)}{1-(\omega/\omega_n)^2}\right) \quad \text{Eq. 2.2}$$

where δ_{st} is the static deflection generated by the force F_0, ω_n the eigen pulsation of the system, and ***Q* the quality factor**. They are defined by:

$$\delta_{st} = \frac{F_0}{k}\ ,\ \omega_n = \sqrt{\frac{k}{m}} \text{ and } Q = \frac{m\omega_n}{c} \quad \text{Eq. 2.3}$$

where k, m and c are the spring constant, the mass and the viscous damping coefficient, as previously defined.

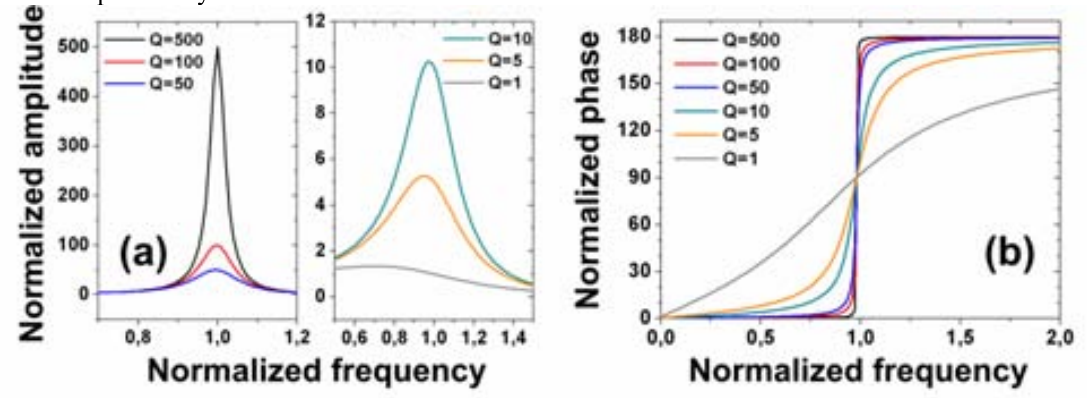

Figure 4. Theoretical variations of (a) the normalized amplitude X/δ_{st} and (b) oscillation phase ϕ as a function of the normalized frequency ω/ω_n for different quality factor Q values.

The normalized amplitude X/δ_{st} and the oscillation phase ϕ are plotted as a function of the normalized pulsation ω/ω_n in the graphs of figure 4 above.

From these results, the vibration amplitude and phase of a forced vibration characteristics are extracted:

- The vibration amplitude X presents a resonance near eigen pulsation ω_n.
- ω_n increases with stifness k and decreases with mass m.
- The higher the quality factor Q of the resonance (low damping), the more intense and narrower the resonance peak.
- The vibration amplitude at eigen pulsation ω_n is $X = Q\delta_{st}$. If $Q > 1/\sqrt{2}$ (≈0,70), the maximum of amplitude is produced at pulsation:

  $\omega_{max} = \omega_n\sqrt{1-1/(2Q^2)}$ Eq. 2.4

  Thus the damping has as effect to shift the resonance to lower frequencies.

  The maximal vibration amplitude is then equal to:

  $X_{max} = Q\delta_{st}/\sqrt{1-1/(4Q^2)}$ Eq. 2.5
- For a very small damping ($Q^2>>1$), $\omega \approx \omega_n$ and $X_{max} = Q\delta_{st}$. Then the resonance quality factor can be determined by the following relation:

$$Q = \frac{\omega_n}{\omega_2 - \omega_1} \qquad \text{Eq. 2.6}$$

where ω_1 and ω_2 are the pulsations at left and right of the maximum such as $X = X_{\max} / \sqrt{2}$.

- The curve X/δ_{st} (ω/ω_n) is dissymmetric with lower amplitudes hereafter the resonance.
- The damping effect is the most important at resonance.
- The response is in retard with excitation before resonance and inversely after. For small damping (elevated Q), the phase varies approximatively 180º around resonances. The response and excitation become then in phase opposition hereafter the resonance.

The quality factor can also be defined equivalently from energetic considerations:

$$Q = \frac{W_0}{\Delta W} \qquad \text{Eq. 2.7}$$

where W_0 is the total energy in the structure, and ΔW the total energy loss by period.

2.4.2 Comparison with real case: non-linearity and several dampings.

An important element to take into account regarding previous calculations, is that we have supposed the force applied at the mass. However, in the case of an external excitation by a piezoelectric disc, the excitation comes from the substrate. It is not needed to re-do all the calculations since the obtained equation has the same form than Eq.2.1, and that the obtained response is thus the same, considering a force with an amplitude A dephased from α.

For high vibration amplitudes, it could be necessary to consider no linear displacement terms in the movement equation.
The equation takes then the form:

$$m.\frac{d^2x}{dt^2} + c\frac{dx}{dt} + f(x) = F_0 \cos \omega t \qquad \text{Eq. 2.8}$$

where $f(x)$ is a non constant function.

Where the linearity is due to restore force, it can be considered that $f(x)$ is of the form $ax \pm bx^3$ (Duffin equation) where the sign + corresponds to a spring of increasing stiffness (hard spring) and the sign – to a spring of decreasing stiffness (soft spring). In this case, a hysterisis near resonance of the vibration amplitude curve as function of the frequency (figure 5) is observed. This phenomenon is easily observed in the case of thin microstructures. It has to be avoided when resonance frequencies have to be determined with precision. Moreover, when the vibrations are no linear, sub-harmonic ($\omega_k = k/\omega$, k integer) and super-harmonic ($\omega_k = k\omega$) vibrations are produced. This different phenomena characteristic of no linear vibrations could be annoying for quantitative analysis of high amplitude vibrations.

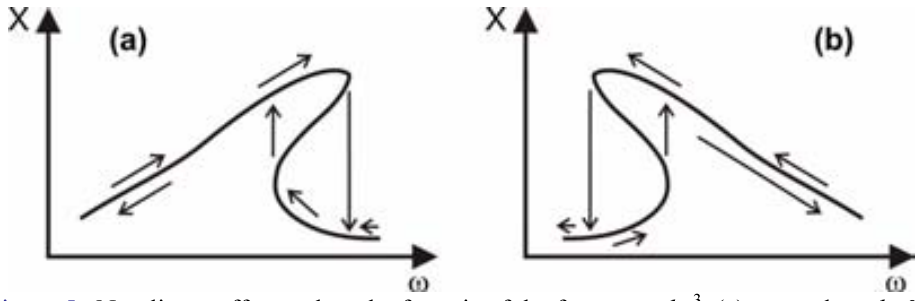

Figure 5. Non linear effects when the force is of the form $ax \pm bx^3$. (a) case where $b>0$ (hard spring), (b) case where $b<0$ (soft spring).

The simple modelling that we have seen is useful for understanding the dynamic behaviour near the resonance in a point of a micromechanical structure such a cantilever, bridge or membrane.

However, to determine the dynamic and exact behaviour of a microstructure, it is necessary to consider the mass and stiffness of the structure for the considered movement. Freedom degrees and thus resonance frequencies and mode are infinites. Each vibration mode has a specific form, resonance frequency and quality factor.

The quality factor of a resonance for a micromechanical structure is determined by the different losses mechanisms producing vibrations damping. As a first approximation, we suppose the global quality coefficient is determined by the superposition of the different damping sources:

$$\frac{1}{Q} = \sum_i \frac{1}{Q_i} \qquad \text{Eq. 2.9}$$

where Q_i corresponds to the i-type damping, and are related to air damping, thermo-elastic damping,etc... More details will be given in *Chapter IV*.

2.5 The cantilever

In this section, the resonance frequencies and modes of a cantilever will be theoretically determined as a function of its dimensions and structural material properties.

The model of driven-damped-oscillator seen in the last section indicates that for quality factors $Q^2>>1$, the resonance frequencies for driven vibration are closer to the eigen frequencies. The measured quality factors being usually superior to 50, the determination of the eigen frequencies is enough for the results analysis.

The different types of vibration of a cantilever are (figure 6):

- Longitudinal vibrations, parallel to the bar axis.
- Flexion (vertical or lateral) vibrations, transverse to the bar axis.
- Torsion vibrations, producing a rotation of each bar section around the bar inertial axe which is immobile.

Only transverse (flexion) vibrations will be considered, and ideal cantilevers [19].

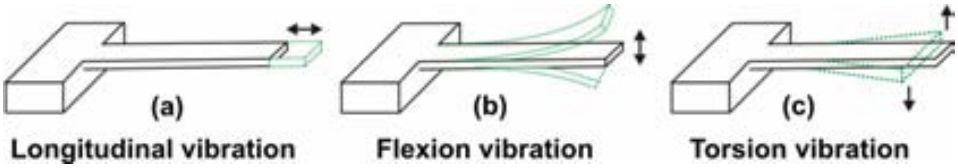

Figure 6. The different types of cantilever vibration mode: (a) longitudinal, (b) flexion and (c) torsion.

2.5.1 The ideal cantilever

A cantilever is considered ideal when:
- it has constant thickness and width along the length,
- it is constituted of a material ideally elastic and homogeneous,
- it is thin (the dimensions of the section of the cantilever are very small compared to its length),
- no axial strain is applied to the cantilever.

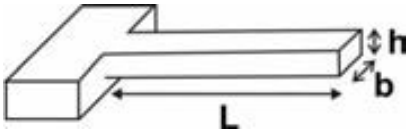

Figure 7. Ideal microcantilever schematic.

Classical formulation

The resonance frequency of order n of an ideal microcantilever (figure 7), L long, b wide and h thick, is given by [19] (cf. *Annex A1* for more details):

$$f_n = \frac{(\lambda_n)^2}{2\pi\sqrt{12}} \frac{h}{L^2} \sqrt{\frac{E}{\rho}} \qquad \text{Eq. 2.10}$$

where the constants λ_n, forming a infinite serie, are solutions of the equation:

$$\cos(\lambda_n).\cosh(\lambda_n) + 1 = 0 \qquad \text{Eq. 2.11}$$

Depending of the cantilever width, Poisson coefficient in Young modulus value has to be taken into account: E then becomes $E/(1-\nu^2)$. Usually the real value of the Young modulus is between these 2 values.

Table II-1 gives the values of constants λ_n and $\lambda_n^2 / 2\pi\sqrt{12}$.

Table II-1. Useful constants for the resonance frequencies and vibration modes calculation of an ideal microcantilever.

n	λ_n	$\lambda_n^2 / 2\pi\sqrt{12}$
1	1.875	0.161
2	4.694	1.012
3	7.854	2.834
4	10.995	5.554
5	14.137	9.182
n>5	$(2n-1)\pi/2$	$(2n-1)^2\pi/(8\sqrt{12})$

In the case of an ideal microcantilever with known dimensions and density, the measurement of one of the resonance frequencies allows to calculate the Young

modulus constituting the material. In practice, the fundamental resonance frequencies of different lengths are measured, and the Young modulus determinated by the shape of the linear curve $1/\sqrt{f}$ as a function of L. Another method, more precise because less dependent on possible technological variations, consists in measuring several resonance frequencies of a same microcantilever.
Figure 8 below give an aspect of the first calculated modes [19].

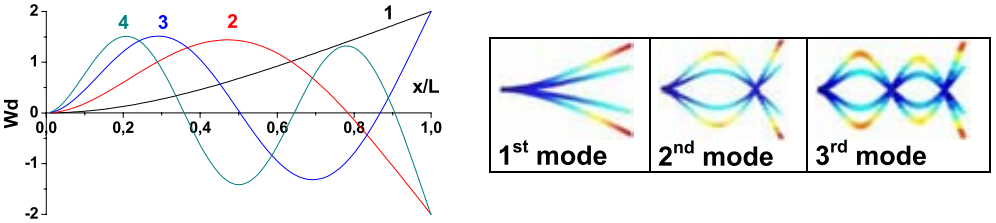

Figure 8. Aspect of the first resonance modes of an ideal microcantilever.

The node position from the clamping is:

- x/L = 0,774 for the second mode
- x/L = 0,500 and 0,868 for the third mode
- x/L = 0,356 - 0,644 and 0,906 for the fourth mode

Let us note that the effective mass of the microcantilever corresponding to the n^{th} mode is equal to:

$$m_n = m_0 . \frac{3}{(\beta_n . L)^4} \qquad \text{Eq. 2.12}$$

where β_n is a constant depending of the microcantilever resonance mode (cf. *Annex A1*).

m_0 is the microcantilever mass, its value is :

$$m_0 = \rho . L . h . b \qquad \text{Eq. 2.13}$$

The elastic constant (stiffness, spring constant…) of the microcantilever is given by the following expression:

$$k = 3\frac{E.I}{L^3} = \frac{E.h.b^3}{4.L^3} \qquad \text{Eq. 2.14}$$

where I is the inertia momentum (cf. Eq. A1.2 in *Annex A1*).

Microcantilever width effect

As already noted, the effective Young modulus varies between the unixial Young modulus E and the second biaxial modulus $E/(1-\nu^2)$. In fact, this depends on the ratio b/L of the section. This variation can reach about 10 %. Therefore it has to be taken into account to obtain precise measurements, especially when the length is small compared to the others dimensions.

2.5.2 Real microcantilevers

Real microcantilevers present several differences with the ideal microcantilevers above considered:

- Generally sub-etching (underetching) near the ancrage is present.

- Vibrations are damped.
- Real microcantilever section is rarely rectangular.
- Thin films constituting the microcantilevers initially present residual internal constraint. The new equilibrium resulting from the microcantilever release produces a microcantilever form change.

It is thus often useful to apply correctives factors taking into account these differences.

Residual constraint effect

Deposited thin films invariably present elevated internal residual constraint. These constraints rely to the restriction of the expansion and contraction of the film imposed by their attachment to the substrate. These constraints can have intrinsic (linked to the growth process) or extrinsic (linked to extern conditions) origin. The intrinsic constraints depend of the film and substrate nature, the elaboration method and post-treatments. External constraints are often thermal constraint due to the difference of thermal coefficients between the film and the substrate.

These constraints are relaxed in released film portions from the substrate. The resulting volume increase or decrease leads to a new mechanical equilibrium state, and thus to global deformation of the device.

If the initial constraint s_0 in the film is homogeneous in depth, when a realized microcantilever is released from the substrate, the constraint is relaxed by a microcantilever elongation (extension) if s_0 is compressive or by a contraction if s_0 is extensive. For the Young modulus determination from resonance frequencies taking into account the length L, the possible effect of the constraint has to be taken into account, even if it is small.

If the constraint is inhomogeneous in depth, the effect is much more significant. The presence of a stress gradient produces a curvature of the microcantilever (cf. figure 14(b)). Usually the stress gradients are elevated in thin films, and curvature is often important. It is obvious that this affects the resonance frequency.

2.6 The microbridge

2.6.1 Ideal microbridge

Classical formulation

Microbridges are microcantilevers clamped at their two extremities (figure 9). The deflexion and its derivative are zero at extremities.

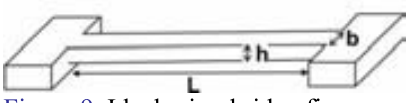

Figure 9. Ideal microbridge figure.

The movement equation describing the free vibrations in flexion of non constrained microbridges is the same than for the microcantilever previously described (Eq. 2.10). Its resolution, with the limit conditions defined above, leads to an similar expression of resonance frequencies obtained for microbridges, but with different λ_n constants.

It can be demonstrated that the λ_n constants for microbridges are solutions of the equation:

$$\cos(\lambda_n).\cosh(\lambda_n)-1=0 \qquad \text{Eq. 2.15}$$

Table II-2 gives the λ_n and $\lambda_n^{\,2}/2\pi\sqrt{12}$ constants values.

Table II-2. Useful constants for the resonance frequencies and vibration modes calculation of an ideal microbridge.

n	λ_n	$\lambda_n^{\,2}/2\pi\sqrt{12}$
1	4.730	1.028
2	7.853	2.8336
3	10.995	5.554
4	14.137	9.182
5	17.278	13.717
n>5	$(2n+1)\pi/2$	$(2n+1)^2\pi/(8\sqrt{12})$

Node position from the clamping is:

- x/L = 0,500 for the second mode
- x/L = 0,359 and 0,641 for the third mode
- x/L = 0,278 - 0,500 and 0,722 for the fourth mode

And the aspect of the first calculated modes can be seen on figure 10:

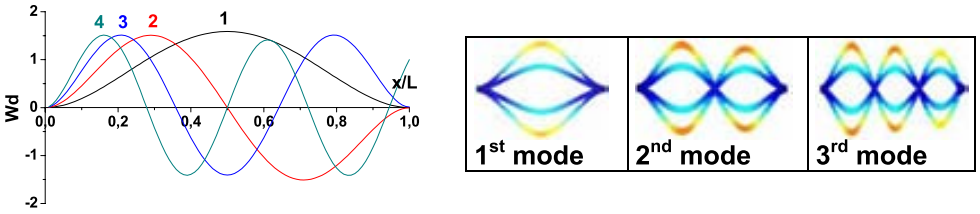

Figure 10. Aspect of the first resonance modes of an ideal microbridge.

Microbridge width effect

The effect of the ratio width/length of microbridges is identical to the microcantilevers one, considering that the effective Young modulus varies between E and $E/(1-\nu^2)$.

2.6.2 Real microbridges

Real microbridges can have the same geometrical imperfections than the reals microcantilevers, i.e. a clamping underetching and a non perfectly rectangular section. The residual constraints have little effect on the cantilever resonance frequencies, but have to be inevitably taken into account in the case of bridges.

Constraints effect

Two cases have to be distinguished, depending on nature of the constraints, tensile or compressive (figure 11).

Figure 11. Effect of the (a) tensile and (b) compressive constraint on microbridge structure.

- **First case :** extensives constraints

The microbridge remains in tension after release because the constraint cannot relaxe due to the clamping at extremities.

- **Second case :** compressives constraints

Below a particular compressive constraint value σ_{cr}, called critical buckling constraint (or critical buckling load), the bridge remains flat. If the constraint exceeds this value, a mechanical instability, the buckling, is produced.

For a rectangular section microbridge, the critical buckling constraint is given by the expression [20]:

$$\sigma_{cr} = -\frac{\pi^2}{3}\frac{E.h^2}{L^2} \qquad \text{Eq. 2.16}$$

The critical level of buckling is lower if the microbridge is longer and thinner.

The n^{th} mode resonance frequency $f_n(\sigma)$ in presence of a constraint is linked to the resonance frequency $f_n(0)$ without constraint by the relation:

$$f_n(\sigma) = f_n(0)\sqrt{1+\gamma_n\frac{\sigma}{|\sigma_{cr}|}} \qquad \text{Eq. 2.17}$$

where γ_n is a constant.

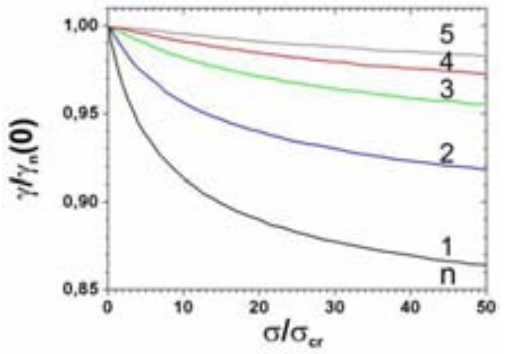

Figure 12. Normalized γ_n coefficients as a function of the normalized constraint for resonance modes 1 to 5 (Adapted from [20]).

Previous works [20] generally consider γ_n coefficients constant. In fact, numerical calculation shows that these coefficients rigorously depend on σ/σ_{cr} [21]. This is illustrated in the figure 12 which represents the normalized γ_n coefficients at their value $\gamma_n(0)$ for $\sigma = 0$ as a function of the normalized constraint σ/σ_{cr} for the 5 first modes. We can note that the coefficients can be considered constant with good precision only for elevated order modes. The γ_n coefficient calculated for the first mode when $\sigma = -|\sigma_{cr}|$ is equal to 1. This is conforming to the fact that the resonance frequency is zero at the buckling threshold.

If the resonance frequencies of several modes can be measured, the Young modulus E and the constraint σ can be determined.

More precise values of the γ_n coefficients are then determined with the curves of figure 12, and the procedure re-iterated. The precision can be increased after several iterations. However the precision obtained is generally enough after the first iteration because of the small dependence of coefficients γ_n with constraint.

2.7 Structural layer

The knowledge of electrical and mechanical properties of a layer is a first step for the conception of microsystems more complex. Therefore, we have realized simple test structures based on cantilever and bridges. Moreover, the mobile structure is often used as sensible element (electrode), thus it is important to have a conductive layer.

The mechanical properties are essential for MEMS realization, and low constraints are necessary to avoid deformations on fabricated structures. For example, in the case of a high compressive stress, or in presence of a stress gradient, bending of the structure can occur during releasing. These mechanical properties entirely depend on layer growth parameters and eventually thermal annealing. An effective control of growth parameters is then necessary to obtain optimized layers for the fabrication of mechanical structures.

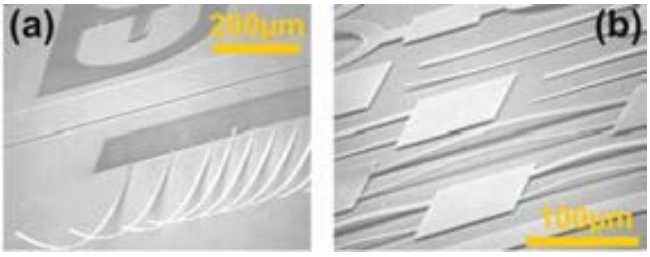

Figure 13. Effect of the (a) axial constraints on poly-Silicon microcantilevers and (b) stress gradient on poly-Silicon microbridges.

Two kinds of stress can deform the released thin devices, the axial stress, that can be tensile or compressive, and the stress gradient. Their effect on poly-Si structures can be seen in figure 13.

2.7.1 The different constraints

The compressive axial stress will bend the structures for a particular critical length (length depending of the stress), while a tensile stress will tense the structures, disminishing their elasticity. In many cases, the stress reduction is crucial for bridge-type structures. The vertical stress gradient is visible on cantilever-type devices, bending them up or down depending of its signus.

The presence of a stress gradient will be thus optically invisible in bridge-type structures, such as the axial stress, compressive or tensile, will be on cantilever-type structures.

2.7.2 Test structures

As already mentioned, the main test structures are cantilevers and bridges.

Axial constraints measurements: bridges and bridges on ring

These structures are the more elemental to measure this kind of constraint. It consists in two sets of structures that are deformed when the layer presents axial constraints. The first set is constituted of a serie of simple bridges (clamped beam at the 2 extremities) of variable length L. The second set is constituted of a serie of bridges inserted on a ring with a diameter L variable.

For a certain stress value, if the stress is compresive, the simple bridges will begin to bend in the z direction for a critical length. The critical stress value of the layer then can be determined from Eq. 2.16.

If, by contrast, the stress is tensile, the simple bridges will be not deformed and the bridges on ring will be flambed to a particular length L_C, and the stress value can only be approached.

A simple and rapid method to evaluate the stress of a layer is possible by determining the first bridge length which induces a curvature of the structure.

Gradient stress measurements: cantilevers

The cantilevers are typical structures for the gradient stress measure. The free extremity will bend towards the substrate or opposite, depending of the gradient signus, negative in the first case, or positive in the second (figure 14).

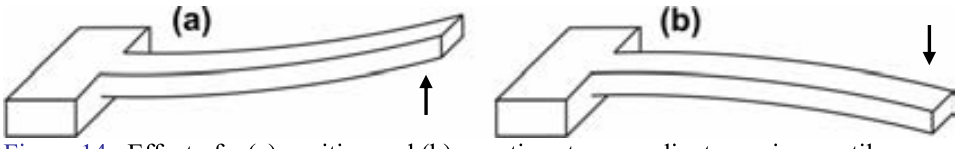

Figure 14. Effect of a (a) positive and (b) negative stress gradient on microcantilevers.

2.8 The electrostatic resonator

The operation principle of micro-resonators with electrostatic actuation has been extensively described by Nguyen [12-13, 22-23]. Different kind of electrostatic resonators can be found in literature, the firsts reported in past being based on vertical vibration mode. Lateral vibration mode resonators were then developed, once technological process optimized, and different electrostatic structures, such as comb-drives, beams and disks investigated. In our work, only beam resonator has been

investigated. Usually, different configurations can be encountered for resonator, as a dipole or quadripole, depending of the ports number (figure 15).

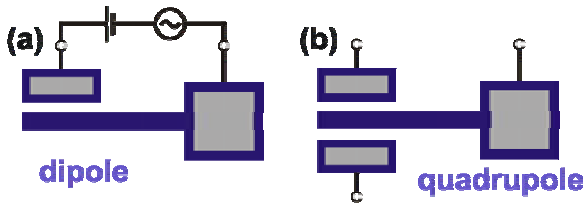

Figure 15. Cantilever resonator configuration (a) dipole, (b) quadrupole.

In our approach, the mechanical cantilever is electrostatically actuated and a capacitive detection scheme converts mechanical oscillations into an electrical signal. To better understand this approach, i.e. how an electric voltage can be transformed into a mechanical force and a mechanic displacement into an electric current, the two cases have to be considered.

2.8.1 Electrical to mechanical signal translation

Let us consider a parallel capacitor (with one mobile electrode) constituted of two plates (electrodes) having an area A and separation d (figure 16). When a voltage V is applied to one of the electrodes, the force generated between the plates by the electric field is:

$$F = \frac{V^2}{2}\varepsilon_0 \frac{A}{(d-x)^2} \qquad \text{Eq. 2.18}$$

where x is the mobile electrode displacement.
Thus, in this case, the force is a non-linear function of both the applied voltage and displacement. To obtain a linear transduction, the signal is superimposed to a continuous voltage.

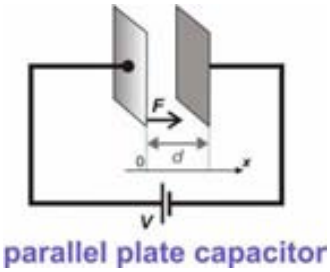

Figure 16. Schematic of a parallel plate capacitor.

Therefore, let us consider now a continuous voltage V_{DC} superimposed to an alternative voltage V_{AC}, with $V_{AC} << V_{DC}$. Neglecting the second order term, we can consider the square voltage applied to the electrode is:

$$E^2 = V_{DC}^2 + 2V_{DC}V_{AC} + V_{AC}^2 \qquad \text{Eq. 2.19}$$

Conserving only the alternative component of this expression, and assuming that the mobile electrode displacement x is small compared to d, we obtain for the low signal sinusoidal mode:

$$f = V_{AC} V_{DC} \varepsilon_0 \frac{A}{d^2}, \qquad \text{Eq. 2.20}$$

where f and V_{AC} are the small signal magnitudes of the force and the input voltage respectively. We consider as input voltage only the sinusoidal component V_{AC} of the voltage applied to the transducer electrode.
For small displacements, the value below defined is the electromechanical coupling coefficient:

$$\delta = \frac{f}{V_{AC}} = V_{DC} \frac{\varepsilon_0 A}{d^2} \qquad \text{Eq. 2.21}$$

Thus the electrostatic transducer generates a mechanical force proportional to the input voltage.

2.8.2 Mechanical to electrical signal translation

Let us now consider that only V_{DC} is applied to the transducer and that the mobile electrode has a displacement of a distance x. The displacement modifies the capacitance of the transducer. Since the applied voltage is maintained constant, a charge variation occurs between the electrodes:

$dQ = V_{DC} dC$

For the low signals regime we obtain:

$$dC = d\left(\frac{\varepsilon_0 A}{(d-x)}\right) = \frac{\varepsilon_0 A}{(d-x)^2} dx \approx \frac{\varepsilon_0 A}{d^2} dx,$$

Thus $dQ = V_{DC} \frac{\varepsilon_0 A}{d^2} dx = \delta dx$

Since $\frac{dQ}{dt} = i$, where i is the current through the capacitance, we obtain the following relation:

$i = \delta \frac{dx}{dt} = \delta v$, where v is the mobile electrode displacement velocity.

2.8.3 Equivalent electrical modelling of a resonator

Apart the mechanical model previously seen, an electrical model can also describe the resonator behaviour. In the previous section, we have described the mechanical resonator behaviour using its mass m, its constant spring k and its damping coefficient c. However, a mechanical oscillator m, k, c is equivalent to an electrical RLC oscillator. The Table II-3 below shows the analogous terms in mechanics and electronics. Therefore a pure mechanical resonator can be described by a single RLC branch. Increasing the resistance R will be similar that increasing the damping c, thus diminishing the quality factor Q and giving magnitude and phase responses similar to those obtained in figure 4. However, in the electrostatic approach, the structure is constituted by the resonator and 2 transducers (input/output). The 2 transducers are polarized at a continuous voltage, applied to the resonator. The input signal is applied to the input electrode, thus the total voltage applied to the input transducer is a superposition of these 2 voltages (figure 17(a)). The input transducer generates on the resonator a force proportional to the input signal. The resonator reacts by oscillations only at frequencies which correspond to the favoured resonance mode. Then the output

transducer, which is also polarized at continuous voltage, detects the oscillation converting them to output current. This output current can then be amplified by an integrated circuit.

Table II-3. Analogous terms of an oscillator system in mechanics and electronics

Mechanical	Electrical
Position x	Charge q
Velocity $\frac{dx}{dt}$	Current $\frac{dq}{dt}$
Mass m	Inductance L
Spring constant k	Elastance $\frac{1}{C}$
Damping c	Resistance R
Driving force F	Voltage E
$f_n = \frac{1}{2\pi}\sqrt{\frac{k}{m}}$	$f_n = \frac{1}{2\pi}\sqrt{\frac{1}{LC}}$
$Q = 2\pi f_n \frac{m}{c}$	$Q = 2\pi f_n \frac{L}{R}$

2.8.4 Equivalent small signal electrical scheme of the resonator

Is is demonstrated that a mechanical resonator with 2 electrostatic transducers is electrically seen as an RLC with the capacitances of the input/output transducers (C_{01} and C_{02}) and a capacitance between the input and output electrodes [19], called coupling capacitance C_C. This is illustrated in figure 17, with a possible measurement set-up and the equivalent electrical circuit.

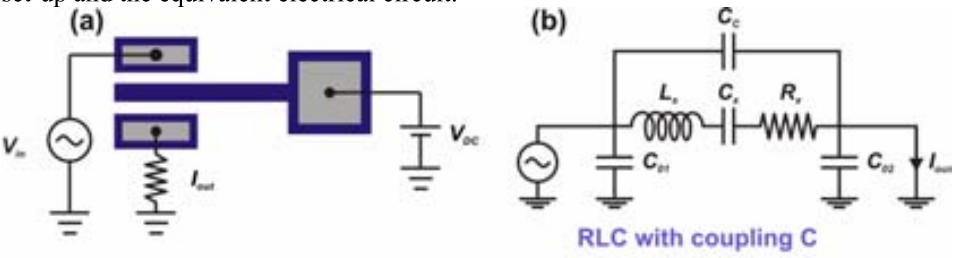

Figure 17. (a) A possible electric and detection measurement scheme for a micro-electromechanical cantilever-based resonator and (b) its equivalent electrical schematic.

Thus the resonator is electrically seen as an RLC with a coupled capacitance. Therefore, the magnitude and phase completely differ from a single RLC branch. In this configuration, the magnitude response exhibits a resonance peak immediately followed by an anti-resonance peak. Figure 18 shows the evolution of the magnitude and phase simulated for a resonator for different capacitance coupling. This latter determines the magnitude and phase of the anti-resonance peak, being respectively more and less pronounced when it is elevated. The characteristic obtained with the value of 1 pF is close to the value without C_C (cf. figure 4).

The motional inductance L_x, capacitance C_x and resistance R_x model respectively the inertia, the elasticity and the energy losses. The equivalences are given by:

$$L_x = \frac{m}{\delta^2},\ C_x = \frac{\delta^2}{k},\ R_x = \frac{c}{\delta^2} \qquad \text{Eq. 2.22}$$

where δ is the electromechanical coupling coefficient, and *m*, *k* and *c* are respectively the mass, stiffness and damping coefficient.

The parallel capacitances at ground C_{01} and C_{02} are the transducers capacitances (the vibrant structure is connected to a fixed bias, thus to the low signal ground). All the parasitic capacitances created by external connection are often particularly disturbing during the resonator operation.
At resonance, L_x and C_x cancel and the branch is thus reduced to the motional resistance R_x. R_x has to be the lowest possible to obtain low-power resonators, usually reached for low k value, large coupling area, small gap or high DC voltage. The most effective way would consist in reducing the gap, but its minimum value is limited by the fabrication process. Therefore, typical R_x values for MEMS are in the MΩ range, which could be problematic for impedance adaptation with the 50 Ω impedance instrument. The capacitance coupling has also to be minimized since it can induce low impedance values at resonance, smaller than R_x, thus giving higher contribution to the motional current. The capacitance coupling can be highly reduced by integration of electronic circuitry with the mechanical resonator.

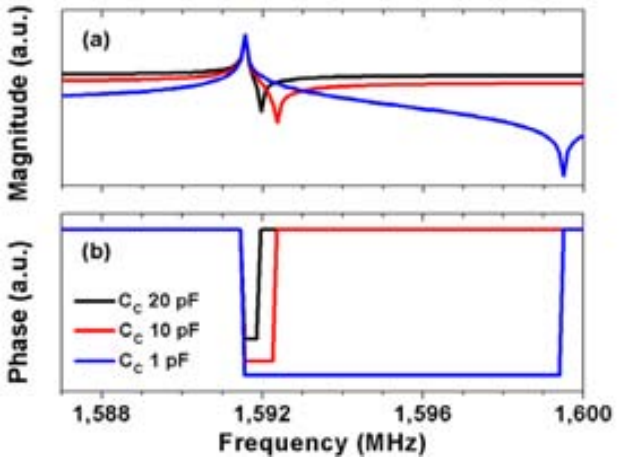

Figure 18. (a) Magnitude and (b) phase electrical simulation of the RLC//C_C electrical resonator model considering C_C different values. R, L and C are chosen to give a resonance frequency around 1.5 MHz.

2.9 Summary

In this chapter, we have summarized the analytical expressions allowing to model the mechanical behaviour of the basic mechanical structures. The working principle of MEMS is presented, giving the main reported actuation/detection techniques and the relevant parameters for the characterization of resonant-based

MEMS. The electrical behaviour of electrostatic based-beam structures is also introduced and analyzed.

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3 CHAPTER III

WBG ETCHING TECHNOLOGY

Because WBG-based semiconductors are thermally and chemically very stable, they are attractive for many applications in harsh conditions such as high temperature and high pressure environment. However, due to their extremely high stability, every step of the fabrication of both MEMS and transistors in these materials is challenging. For example, the resistance of the ohmic contacts mainly depends on the combination of differents metal stacks and it is also very sensitive to the thickness of each layer. Also the lack of a reproducible wet etching technique renders necessary the use of dry etching techniques. However, dry etching is also known to create surface damage and degradation of the electrical properties, especially in the case of transistor fabrication. For both MEMS and transistors applications, etching and ohmic contact formation are two important steps to be optimized. For this reason, the main techniques for the dry etching both on SiC and III-nitrides are reported in this section. A brief state of the art is first given, and then the preliminary etching results are presented.

3.1 SiC etching

3.1.1 Wet etching

The high hardness of SiC makes impossible the chemical etching in water-based solutions and renders difficult to etch in typical acid or base solutions, especially in its single crystal form. Usually chemical etches are not used since they require extremely elevated temperatures thus complicating the finding of adequate mask layers able to resist to such an aggressive ambient. Some attempts of SiC etching has been reported in orthophosphoric acid (H_3PO_4), hydrofluoric acid (HF), sulphuric (H_2SO_4) and nitric acids (HNO_3) combination, but resulting in a very instable etching and only observed for polycrystalline SiC. Some etching methods bypassed the SiC single crystalline etching difficulty by Ar or He implantation in selected areas to render it amorphous and thus easily removable in HF-HNO_3 solution at 45ºC [1].

3.1.2 Photoelectrochemical etching (PEC)

The only effective method for wet chemical etching consisted in using illumination, the *photoelectrochemical (PEC) etching,* which involves an oxidation-reduction reaction. Different solutions have been reported for the n- and p-type doped α-SiC and β-SiC etching, with HF+H_2O+methanol, HF+H_2O+ethanol +UV light, HF + H_2O, etc. Typically, SiC is oxidised by the water oxidant leading to the formation of SiO_2 at the Si surface, followed by the subsequent dissociation in CO and CO_2 [2] (h^+ means the positive charge transfer by a hole):

$$SiC + 2H_2O + 4h^+ \rightarrow SiO + CO\uparrow + 4H^+ \quad (1)$$

$$SiC + 4H_2O + 8h^+ \rightarrow SiO_2 + CO_2\uparrow + 8H^+ \quad (2)$$

Then the HF acid contained in the electrolyte solution removes the formed oxide [2]:

$$SiO_2 + 6HF \rightarrow 2H^+ + SiF_6^{2-} + 2H_2O \quad (3)$$

The reaction can be strongly enhanced by generating additional holes by ultraviolet excitation [3]. Another parameter which allows tuning of the etch rate is the applied voltage. The flatband voltage difference between n- and p-type SiC explains the dopant selective etching demonstrated by different works, thus also leading to selective removal of polytype. Therefore, selective removal of n-SiC from p-SiC can be

performed but the reverse removal can also be done under dark conditions. Furthermore, it has also to be noted that the etch rate on the C-face polarity is higher compared with the Si-face, explained by the higher oxidation rate of the C-face.
This technique leads to a very high etch rate, up to 1-2 µm.min^{-1}, especially under Hg lamp. Some degree of anisotropy could also be obtained with metal masks (Ti or Au/Cr). However a possible shadowing of the ultraviolet light can lead to some etch inhomogeneities. Some of the disadvantages of the technique include fairly rough surface morphologies. This is due to the enhanced etch rates for areas around crystal defects but especially the inability to pattern very small dimension features and poor uniformity of etch rate. For these reasons, and especially because PEC etching is highly defects dependent, the most used techniques for SiC etching are by far the plasma-based ones.

3.1.3 Sputter etching

The sputter etching or ion beam milling is a gas phase process, which can be applied to all materials. Energetic ions are accelerated in the plasma to the substrate surface at high energies (>200 keV). By momentum conservation law, some of this energy is transferred to surface atoms that are then ejected, leading to material removal. The main advantage of this technique is the high anisotropy of the etching process, which enables the fabrication of structures with abrupt side walls. Due to the pure physical nature of the etching process, sputter etching is unselective and etches materials and even masks with similar rates. This requires the use of thick mask layers. The main inconvenient is the high impact of the bombarding ions on the surface, which can create defects and amorphous surface layers. The sputtering etch rate is directly depending of the ion mass, the ion energy, the rf field, the rf frequency, the substrate temperature… and reaches values about 20 nm.min^{-1}. This physical technique is sometimes used with Ar^+ ions to clean and smooth the surface before metallization to improve the properties of Ohmic and/or Schottky contacts.

3.1.4 Plasma-based etching

Currently, plasma-based chemical dry etching is the most used patterning technique for SiC. Reliable, well-controlled patterning can be achieved by a variety of plasma reactor platforms.

Reactive Ion Etching (RIE)

Reactive Ion Etching (RIE) was the first plasma-based technique for SiC etching. A plasma at a radio frequency of 13.56 MHz between two parallel electrodes in a reactive gas is generated (figure 1). The electrons are accelerated and collide with gas molecules thus contributing to sustaining the plasma. The substrate is placed on the power electrode, not grounded, leading to a large negative DC self-bias on the sample which attracts ions from plasma causing damage on the surface. This results in high etch rates and anisotropy. However, highly energetic ions seriously damage the sample surface.

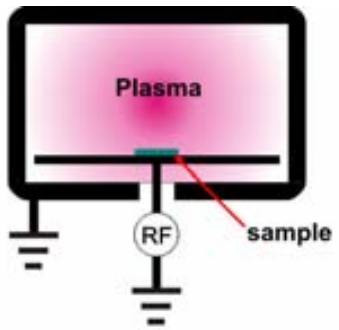

Figure 1. Schematic of a RIE reactor.

High-density plasma: Electron-Cyclotron Resonance (ECR) and Inductive Coupled-Plasma (ICP)

High-density plasma Electron-Cyclotron Resonance (ECR) and Inductive Coupled-Plasma (ICP) etch processes are interesting in yielding smooth, highly anisotropic, etch characteristics.

ECR plasmas are formed at low pressures with low plasma potentials and ion energies due to magnetic confinement of electrons in the source region. Therefore, the surface damage in ECR may be less than with the RIE technique. ECR provides high ion density (10^{11}-10^{12} cm^{-3}) compared with RIE (10^{9} cm^{-3}) without inducing high damage on the sample because the plasma potential is much lower.

ICP plasmas are formed in a dielectric vessel encircled by an inductive coil into which rf power is applied. A strong magnetic field is induced in the center of the chamber, which generates a high-density plasma (~5×10^{11} cm^{-3}) due to the circular region of the electric field that exists concentric to the coil.

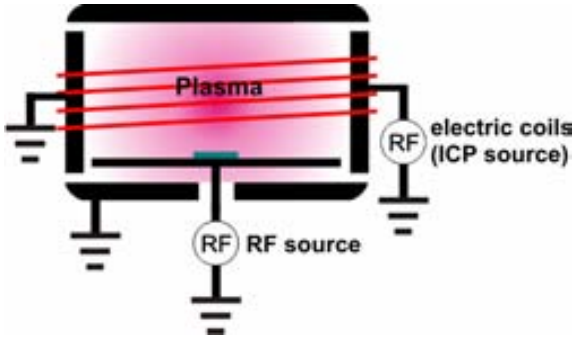

Figure 2. Schematic of a ICP reactor.

Several chemistries were used for SiC etching in ICP/ECR. It has to be noted that the chemistry must be reactive with SiC and the species produced by the chemical reactions must be volatile compounds under the temperature and pressure condition to avoid possible residues on the surface. Fluorine, chlorine and bromine containing plasmas were investigated. A selected number of etch chemistries and the obtained etch rates on different polytypes is presented on Table III-1. It is important to note that the off-orientation affects the etch rate.

Table III-1. Reported etch rates[1] of SiC obtained from different dry etching techniques.

Gas chemistry	Etching technique	Etch rate (nm.min^{-1})			References
		3C(100)	4H(0001)	6H(0001)	
CHF_3/O_2	RIE	20		16	[4]
CHF_3	RIE	40			[5]
CF_4/O_2	RIE	35		32	[4]
SF_6/O_2	RIE	45		45	[4]
NF_3/O_2	RIE	85		58	[4]
NF_3	RIE		150	150	[6]
$CF_4/O_2/N_2$	RIE			220	[7]
$Cl_2/SiCl_4/O_2/N_2$	RIE			160	[8]
$Cl_2/SiCl_4/O_2/Ar$	RIE			190	[8]
SF_6/O_2	ECR	26			[9]
CF_4/O_2	ECR	70		70	[10]
SF_6/Ar	ECR			450	[10]
SF_6/O_2	ECR	250		250	[10]
Cl_2/Ar	ECR			250	[10]
IBr/Ar	ECR			110	[10]
NF_3/O_2 or Ar	ICP			400	[10]
NH_3	ICP		800		[10]
SF_6	ICP			970	[10]
SF_6/O_2	ICP			800	[11]

3.1.5 Discussion

From table I, it could be noted that the higher etch rates are obtained with ECR or ICP techniques with fluorine chemistry. Meanwhile reduced etch rates are obtained with bromine chemistry. This is explained by examining the boiling points for potential etch products in these plasmas, which give an indication of the relative volability. The boiling points of some potential etch products in plasma etching are summarized in Table III-2 and it appears clear that fluorinated products are more volatile than chlorinated counterparts.

Table III-2. Boiling points of etch products in dry etching of SiC.

Etching products	Boiling points (°C)
$SiCl_4$	57.6
CCl_4	76.8
SiF_4	-86
CF_4	-128

The reaction mechanism of SiC in F_x-based chemistry is shown below.

$$Si + xF \rightarrow SiF_x \qquad x \leq 1-4$$

$$C + xF \rightarrow CF_x \qquad x \leq 1-2$$

Different gas were added to investigate the effects on the etch behaviour, including O_2, Ar, H_2 and N_2. Particular attention were given to prevent carbon residues or micromasking effects, and to increase the etch rate without roughness increase.

[1] the reported etch rate refers to the maximum value obtained from referenced work

Oxygen helps to avoid carbon residues (by CO_x formation) and has also often been added to fluorine-based chemistries under RIE conditions to enhance the active fluorine concentration and increase SiC etch rate [4]. Moreover, it prevents the deposition of sulphur compounds on the chamber walls.

By contrast, the addition of H_2 to the gas mixture reduces the etch rate [4] but supports the carbon removal [12] and prevents residue Al formation by forming volatile alane (AlH_3) [13].

Physical sputtering of the substrate surface can be increased by adding nonreactive gases such as argon, or nitrogen. The addition of such gases can reduce the formation of residues in the etched areas by sputtering away etch-resistant materials that would otherwise interfere with the etch process.

No measurable difference in the etch rates between n- and p-type SiC were observed, indicating that Fermi level effects play no role in the etch mechanism under ICP conditions [14]. By contrast with the RIE technique, the etch rate increases when n-type doping increases [15].

It has also to be noted that the dangling bond densities and the corresponding reactivities of the crystal faces are different for a polytype. Each atom on cubic (001) face has two dangling bonds, whereas only one dangling bond exists on a (111) face or similarly to the (0001) face of hexagonal SiC. This is another concept to take into account for possible differences in etch rates.

Concerning the different fluorinated gases available, NF_3, BF_3, CF_4, PF_5 and SF_6, the highest etch rates have been reported with NF_3 and SF_6. This is in good correlation with the average bond energies for the gases, i.e. BF_3 154 kCal/mol, PF_5 126 kCal/mol, SF_6 78.3 kCal/mol and NF_3 66.4 kCal/mol. The lower the bond energy, the more effective is the dissociation in the ICP source to form atomic fluorine neutrals which are the active etchant species. Here, although NF_3 tends to etch SiC at a faster rate, SF_6 is more desirable for use as a feed gas because it is less expensive and safer.

Usually, for a fixed source ICP power, the etch rate increases if the rf chuck power is increased. The rf chuck power allows higher ion energies, thus increasing the Si-C bond breaking efficiency and favouring the etch products formation.

In our SiC etching investigation, the most effective way consisted in using ICP with SF_6/O_2 gases (cf. section 3.1.6). As reported, the addition of O_2 to SF_6 allows to increase the etch rate but also influences the selectivity of the used mask, especially with Al, through its rapid oxidation into Al_2O_3, more sputter resistant. The etch rates initially increases for O_2 percentage lower than 25%, thus increasing selectivity over Al mask. However it is lowered if too much oxygen is added, in part by dilution of the primary gas and by formation of SiO_x on the surface [16].

Different works reported on the effects of various process parameters on the SiC etch rate and selectivity to the mask. Usually, for a fixed platen power, the higher rates are obtained with low pressures, around 3-5 mTorr.
Usually, elevated platen powers give lower selectivity to the mask and elevated pressures (higher than 5mTorr) promote residue formation, whereas lower pressures cause increased trenching at the base of the sidewall.

Concerning the mask choice, photoresist can not be used due to the high ion energies needed to etch SiC. Si, SiO_2 and Si_3N_4 have also been used but the obtained selectivity with SiC was not high enough for using these materials as masks in dry etching processes, but could be interesting as sacrificial layers. For plasma-based processes, metallic masks are required, since they allow higher selectivities, and thus permit to perform deep etching. Al, Ti and Ni (and Cr) are usually used. These metals can also be deposited on Si, oxide or nitride in order to reduce the induced stress (both in the metal and SiC) and for supporting the removal of the mask. A reduced stress could play an important role for low errors during the photolithography step, especially for thin motive devices.

The formation of residues on the etched surface is a significant problem in SiC etching. The highly energetic ions cause significant erosion of the etch mask, and sputtered mask materials that redeposit on the SiC surface can act as micromasks. Sputter erosion of the electrode surface of the walls of the chamber can also cause micromasking.

Trenching is another problem commonly encountered when etching SiC. The flux is often enhanced at the base of the sidewall, which increases the etch rate and produces a trench. The trenches can be reduced by diminishing the ion energies or increasing pressure, at the detriment of lower etch rates.

It should be noticed that most of the reported etching techniques deal with anisotropic etching of SiC. Few works demonstrated the isotropic etching, which could be important for the releasing of structures in SiC substrates. Isotropic etching has been reported with $NF_3/O_2/Ar$ plasma at elevated temperature [17] and more recently only with SF_6 [18, 19]. This is of high interest for MEMS using AlGaN/GaN heterostructure on SiC substrate, thus allowing the release by isotropic etching of SiC.

3.1.6 First attempts of SiC dry etching

As previously stressed, the resonators made with membranes or beams (cantilever or bridge) structures are very useful in the field of high sensing applications such as mass detection for gas sensing devices for example. In all cases, the key process for sensors fabrication is the etching. However, by contrast to Si, and as it has been pointed out in the previous section, SiC cannot be etched chemically and requires dry plasma-based etching techniques. During this study, RIE technique was first investigated and was well suited for etching layers thinner than 1 µm. However, the etched surfaces were highly damaged, with trenching/pitting, micromasking and ridges along the vertical sidewall, as shown in figure 3(a). Micromasking is mainly attributed to etched metal particles from the mask acting as ‘micromask’ redeposits and often resulting in degradation of the etched surfaces. The quartz overplate protecting the cathode has also been reported to act in such a way. During the patterning of the SiC layer, micro-trenches (figure 3(b)) can be created at the foot, or edges, which underlie the metal mask layer. This trenching is more pronounced with narrower features, and could be responsible of the decrease of breakdown voltages in power devices. Etch pits can also be formed. The sidewall usually present ridges that come in part from the mask edge definition during the lithography step. These ridges depend of the used mask material and its pattern definition and will be inevitably present for any etching process. In the case of the Al, the grain size of the metal layer can influence this effect, thus requiring an optimization of the conditions of the Al deposition for SiC etching.

Moreover, for thicker SiC layers, RIE technique is limited and an efficient SiC etching with high aspect ratio is thus required. As previously explained, increasing the plasma density by use of ECR or ICP is a common solution to obtain higher etching rates.
Figure 3(a) shows an example of micromasking leading to the formation of pillars. This problem is common during SiC etching and can be associated with the redeposition of non-etched products and/or sputtered material from the chamber or by slow etching of some defects present in the SiC layer.

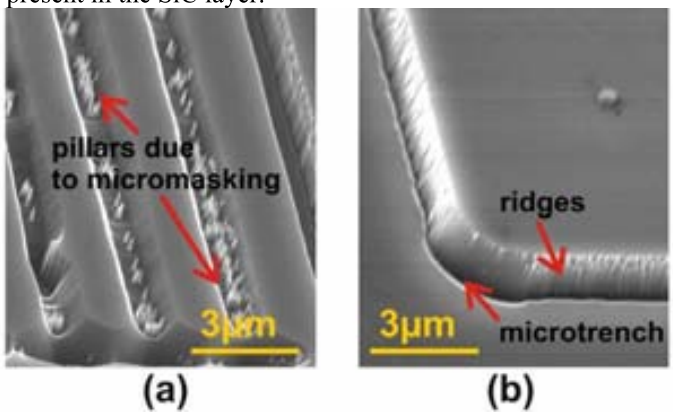

Figure 3. SEM images showing (a) pillars and (b) ridges and microtrenching

First etching tests were performed using RIE but the etching depth was limited. Then, different etching tests using ICP technique were performed on different SiC polytypes by varying different parameters. The main priority was to achieve deep etching profile using adequate mask, with good selectivity, and adjusting the parameters to reduce as much as possible the encountered defects aforementioned.

SEM images in figure 4 show a comparison of the obtained etching profiles from RIE and ICP techniques. In figure 4(b), no trenching, no pits and no micromasking were observed with ICP etching (in this particular case). Moreover, the obtained etching rates varied from 50 to 100 nm/min for RIE and from 300 to 800 nm/min for ICP (Table III-3), in agreement with previous reported works [Table III-1]. ICP seems well adapted for etching at increased rates, but also for reducing the surface defects commonly observed after RIE.

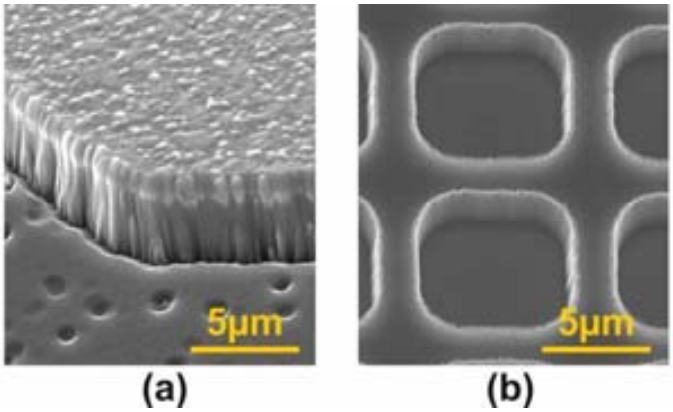

Figure 4. SEM images showing etch profiles obtained from (a) RIE and (b) ICP techniques

However, these defects have to be reduced as much as possible since they are also present using ICP. Thus it requires adjusting the different parameters and choosing a mask that allows deep etching. First etching tests were performed with the most common (and economical) mask, photoresist. However, and by contrast to Si, photoresist cannot be used as etching mask since SiC is etched at similar rate, often resulting in a selectivity lower than 1. For example, to etch 0.7 µm, a photoresist thickness around 4 µm would be necessary. SiO_2 mask was then tested, some details and results of the SiC etching using an oxide mask are detailed in the Table III-4.

Table III-3. Achieved etch rates with RIE and ICP techniques.

Technique	Etch rate (nm/min)
RIE	50-100
ICP	300-800

The sample used here is 4H n-type SiC. The coil power was fixed at 800 W while the platen power and O_2 percentage slightly varied. The selectivity remained constant, around 1.4-1.7. At 75 W platen power and for a flux of SF_6 of 25 sccm, adding around 20% oxygen allows to achieve an optimal etching rate (+20%). Higher O_2 percentage resulted in lower etch rates. Maintaining the platen power at 75 W, the flow of SF_6/O_2 were tested at 40/5 and 40/0. By contrast to the 25 sccm SF_6 flow, the etch rate was higher without O_2. Curiously, similar behaviour was observed at 150 W RF power, slightly higher etch rate was obtained without oxygen.

Table III-4. Details of the used ICP parameters, SiC etching rate and selectivity with SiO_2 mask (using SF_6/O_2 gases). The pressure is 5 mtorr.

N°	Sample name: AH0752-06	P_{coil} (W)	P_{platen} (W)	Flows (sccm)	SiC etch rate (nm/min)	Selectivity
1	Q_3 1st	800	150	25/5	2000	Al
1	Q_3 2nd	800	75	25/5	1700 (1812)	1.41 (1.64)
2	Q_4 1st	800	75	25/10	1310	Al
2	Q_4 2nd	800	75	25/0	1490 (1400)	1.68
3	Q_5	800	75	40/5	1587	1.54
4	Q_6	800	75	40/0	1796	1.46
5	Wafer 4	800	75	25/5	1700	1.41
6	Wafer 5	800	150	25/0	2200	1.5

Despite its low selectivity, SiO_2 mask was mainly investigated because the first etching tests using Al mask resulted in marked microtrenches and ridges along the etched wall. In the images of figure 5, the SiC etched profile using an Al mask can be seen for different RF powers. The 3 samples present the more common etching defects, mainly micromasking and trenching. The obtained etch rates are detailed in Table III-5.

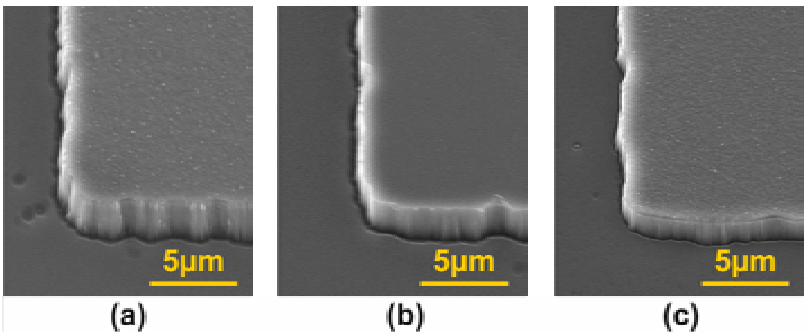

Figure 5. SEM images showing the SiC etched profile with an Al mask for (a) 200, (b) 150 and (c) 75 W.

As it can be seen in figure 5, microtrenching seems to increase with RF power. The profile etched at 75 W clearly showing less microtrench. The etch rate is considerably decreased and thus the selectivity is also degraded when diminishing the RF power.

Table III-5. SiC etching rate and Al selectivity as a function of RF power.

RF power	200	150	75
Al etch rate (Å/min)	590	640	517
SiC etch rate (Å/min)	3000	2800	1850
Selectivity	5	4.4	3.5

It is interesting to note that a good compromise between SiC etching rate, selectivity, and defects, was obtained using the 150W RF power.

Using SiO_2 as mask, we have observed less ridges along the etched SiC and less micromasking effect (figure 6(a)), compared to Al mask. In the same way, the SiO_2 mask presents some ridges (figure 6(b)), probably coming from ICP etch for mask definition. However, charging phenomenom could play a role. Charging has often been reported to occur during high density plasma etching [20]. Okamoto [21] has recently reported that important differences in microtrenching, etch rates and etching profile are observed depending of the conductivity of the SiC surface. He compared the etching of an n-type and semi-insulating (SI) sample: for the SI one, the etch rate was lower, the sidewall slope higher, and the etched bottom rounder and without microtrench, when comparing to the n-type sample. This was attributed to the higher accumulation of electrons along the sidewall of the SI sample. The difference in the electrical conductivity influences the accumulation of a negative charge at the sidewall, explaining the observed difference. The same concept can be transposed using an insulator mask. A SiO_2 mask can also play a role in the formation of sidewall polymers (acting as protectors) enhancing the anisotropy and the microtrenching. As shown in figure 6, the interface presents a highlighted zone, revealing a charge accumulation.

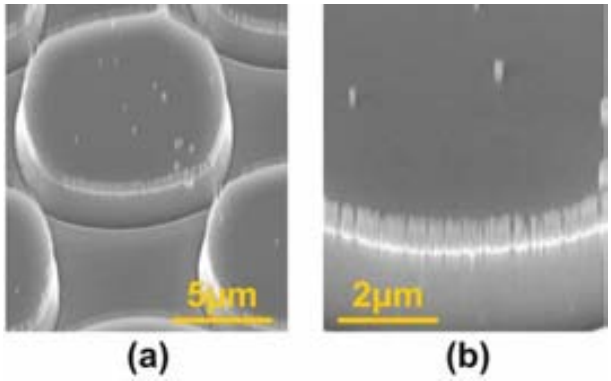

Figure 6. SEM images showing the SiC etched profile with an SiO_2 mask without removing the mask (sample AH0752.06).

We have also remarked that with a SiO_2 mask, the etching shape can be likely rounded (figure 7(a)) or very sharp (figure 7(b)), depending if O_2 is used as reactive gas in the ambient during the ICP etching.

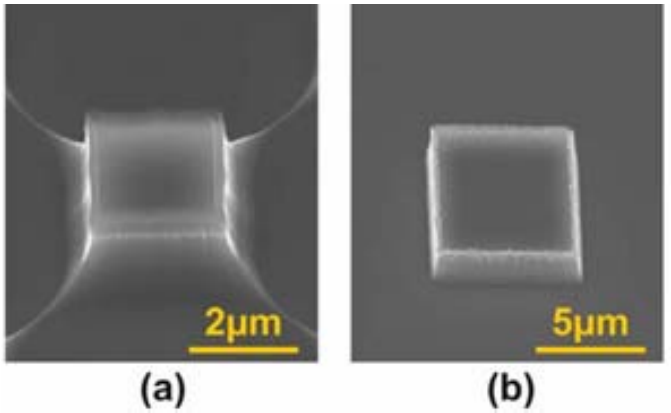

Figure 7. SEM images showing ICP etch profiles obtained with a SiO_2 mask (a) with O_2 and (b) without O_2.

Thus a proposed solution to avoid micromasking, microtrenches and ridges, was to use a bi-layer mask of Al/SiO_2 (with Al on top). Samples 1 and 2 from Table III-4 were processed in 2 etching steps, the first one with the bi-layer, and the second only with SiO_2. Using this last method, the ridges along the SiC wall are considerably reduced, as well as the microtrench, as it can be seen in the figure 8. Table III-6 briefly resumes the process used for 3 different samples. The influence of the platen power can be clearly seen in figure 8(a), with a platen power of 150 W producing more ridges than with 75 W. In figure 8(b), the etching shape is more rounded, due to the 40% O_2. From figure 8(c) it can be seen that the shape is sharper but it seems that a slight lateral etching has affected the surface.

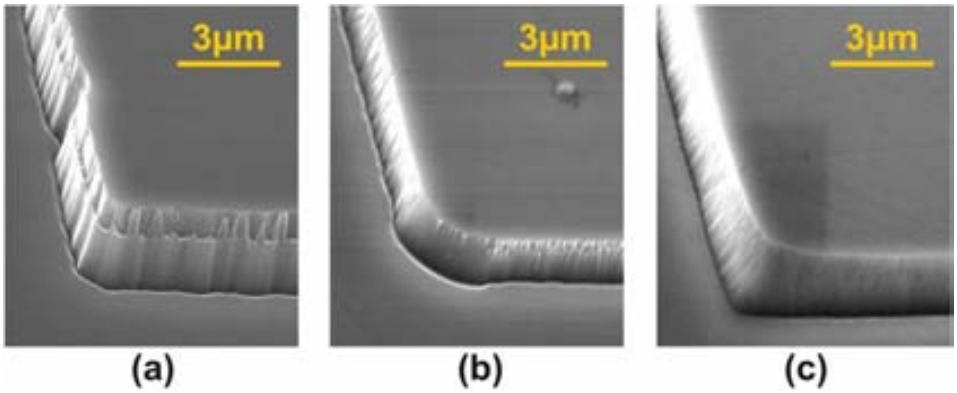

Figure 8. SEM images showing the SiC etched profile with (a) an SiO_2/Al mask, (b) and (c) SiO_2 mask.

Table III-6. Process details of the etching using Al/SiO_2 mask.

Sample	Platen power	1st etch SF_6/O_2	2nd etch SF_6/O_2
Wafer Q_3	150+75	25/5 sccm 6 min	25/5 sccm 10 min
Wafer Q_4	75	25/10 sccm 10 min	25 sccm 5 min
Wafer Q_5	75	40/5 sccm 10 min	-

However, the selectivity is still too low to allow a deep etching and thus other masks have to be investigated. For this reason, only metallic masks were then used in plasma etching for the resonator fabrication process. Usually metals such as Ti, Ni and Cr are used. Among them, Ni is the most commonly used since it presents good selectivity and less micromasking effect than other metals, especially for low O_2 percentage. However, most of the previous works were focused on studying only the etching rate without the aim of realizing a device. In this case, Ni presents interesting properties, especially in term of selectivity. However, with the aim of fabricating a device, it is preferred to use Al, rather than Ni or other metals, since Ni or Ti can be considered as contaminant for some equipment in the cleanroom. Moreover, Al adheres better than Ni (it is often required a bi-layer of Ti/Ni) and is easier to remove than Ni (or bi-layers).
Very few works have reported on SiC etching using an Al mask in an ICP equipment. In this sense, efforts were done to improve and reduce the problems using only an Al mask.

With Al mask, it is required adding oxygen since it helps to improve the selectivity by conversion of the Al surface into Al_2O_3. However, the O_2 percentage is usually below 20% to obtain high etching rate. At higher O_2 percentage, it has been reported that atomic oxygen does not play an efficient role in SiC etching. Moreover, increasing O_2 percentage, the selectivity tends to increase and becomes infinite beyond ~40%, since Al easily oxidizes. The main problem of aluminum is micromasking. However the micromasking is also often due to the cathode. Quartz is often deteriorated during the etching using SF_6/O_2, and with a simple Si wafer introduced on the quartz or using Si wafer pieces, micromasking is avoided. The use of Si in the reactive ambient favours the formation of volatiles species SiF_x and also avoids micromasking due to the cathode. In general, the higher the area of the sample to etch is, the higher the micromasking effect is. Pieces of the etching mask can be redeposited on the surface to etch and thus causing the formation of little peaks. Thus any possible residue on the

mask has to be avoided. For example, Vang [22] has reported that the presence of cut lines induces micromasking, simply by the fact that the delimitation motives can act as walls impeding the evacuation of pieces of the etching mask.

3.2 III-V nitride etching

III nitrides are similar to SiC, presenting elevated hardness and excellent stability in corrosive liquids. Moreover, compared to other III-V compounds, III nitrides etch at much slower rates. III nitrides have strong bond energies compared with other compound semiconductors. The bond energies are 8.92 eV/atom for GaN and 11.52 eV/atom for AlN. These high bond strengths and wide bandgaps make them essentially chemically inert and highly resistant to acids and bases at room temperature.

As for SiC, to initiate and maintain the etching of nitrides, an external energy source is required and can it be delivered via various media:

- Thermal, heating for example in acids/basics solutions
- Photoelectrochemical wet etching, with irradiation of the sample surface with UV radiation
- Dry etching techniques, with energetic ions

This energy is essential in order to obtain adequate etch rates for device fabrication. However, the quality of the etched surfaces is dependent on the energy and the mass of the incident radiation. Energetic ions (>50 eV) cause damage to surfaces. In this sense, it is highly desirable to obtain the lower damage possible, which can be obtained by wet etching, reactive ion etching with low energy ions and plasma etching with incident low energy electrons.

3.2.1 Wet etching

In practice, GaN and AlN can be etched in basic (KOH or NaOH) solutions, the first at temperature above 250 ºC [23], and the second around 60-80 ºC [24]. Acids such H_3PO_4 have also been reported to etch AlN around 80 ºC [25]. Chemical etching reports for GaN are sparse, due to the extreme required temperature. By contrast, AlN has been much more investigated. However, the etch rate strongly depends on the crystalline quality. Nanocrystalline quality AlN is chemically etched at higher etch rates than polycrystalline which is also etched stronger than single crystalline. This could allow the use of sacrificial layer, as reported by Cimalla [26], for fabricating GaN MEMS using AlN as sacrificial layers. The etching is also polarity dependent, with the N-face more prone to be etched away than the metal face [27].

3.2.2 Photoelectrochemical etching

As reported for SiC, using illumination the chemical etches are effectively improved. Following the same concept that the SiC one, the GaN semiconductor surface is oxidised and the resulting oxide subsequently dissolved:

$$2\,GaN + 6h^{+} + 6\,OH^{-} \rightarrow Ga_2O_3 + 3H_2O + N_2 \uparrow$$

$$Ga_2O_3 + 6OH^- \rightarrow 2GaO_3^{3-} + 3H_2O$$

The oxidation process requires holes that can be generated by light with photon energy larger than the band gap.

Tuning the etch rate can be performed by adjusting the doping and choosing adequate light, thus making possible selective etching. A modification of the PEC consisted in irradiating the GaN surface by a 2 keV Ar ion beam, thus charging (by trapped negative charges) the exposed surface areas, which are not attacked during PEC [28]. This demonstrates an elegant form of GaN patterning without masks deposition. PEC can be used for the mesa step of HEMTs fabrication, and gate recess process.

3.2.3 Sputter etching

This technique, described in the last section for SiC, lacks from possible selectivity between materials, due to the physical nature of the process. Moreover, bombarding ions on the nitride surface creates defects, amorphous surface layers and nitrogen losses.

3.2.4 Plasma-based etching

Currently, such as SiC, plasma-based dry etching techniques are the most used methods to pattern the III-nitrides.

Reactive ion etching (RIE)

As for SiC, it was the first dry etching technique applied to III nitrides. In RIE, as already quickly described for SiC, a plasma is generated from a reactive feed gas by applying a radio frequency excitation between two electrodes. Ions are accelerated toward the substrate through a sheath with energy related to the DC self-bias voltage. Etching is typically with biases of a few hundred volts and gas pressures ranging from a few mtorr to a few hundred mtorr.

The III nitrides etch rates attained using RIE with various chemistries rarely surpassed 200 nm/min^{-1} and usually ranged from 15 to ~180 nm/min^{-1}. Very few works reported faster etch rates and were found to depend strongly on the plasma self-bias voltage, and essentially independent of the chamber pressure for pressures lower than 80 mtorr. The higher etch rates were obtained at high plasma DC biases from -300 to -400 V. Anisotropic etch profiles were obtained in all cases but they were overcut which meant that physical mechanisms dominated the etching, even with reputed durable mask such as NiCr metal or SiO_2. In conventional RIE, physical and chemical components of etching cannot be independently controlled. This impacts the shape of etch profiles significantly especially in the case of III-nitrides where high ion energy is required to break the bonds. Moreover, the surfaces etched tended to be highly N deficient, often resulting in damage surface with holes. This tendency is a common observed characteristic of GaN surfaces after plasma or ion beam-based etching.

High-density plasma: Electron-Cyclotron Resonance (ECR) and Inductive Coupled-Plasma (ICP)

As already described for SiC, high density plasma systems use magnetic confinement of electrons in the plasma to generate very high ion densities (>5×10^{11} cm^{-3}). These systems are capable of delivering large ion fluxes at low energies (or biases) and typically operate at pressures ranging from a few mtorr to a few tens of mtorr.
Plasma chemistry has a prominent role in patterning III nitrides. ICP and ECR etching can produce lower damage than RIE while maintaining faster etch rates.
ICP-RIE sources are easier to scale up than ECR sources and are more economical to operate since ICP does not require the electromagnets of waveguiding technology necessary in ECR and the automatic tuning technology is much more advanced for rf-generated plasma than for microwave-generated plasmas.
Whatever the used method, the used chemistry must be as much as possible reactive with GaN and the species produced by the chemical reactions must be volatile compounds under the temperature and pressure condition to avoid possible residues on the surface. Chlorine and fluorine gases were the most investigated. A selected number of etch chemistries and the obtained etch rates on different polytypes is presented on Table III-7.

Table III-7. Reported etch rates[2] of III nitrides obtained from different dry etching techniques.

Gas chemistry	Etching technique	Etch rate (nm.min^{-1}) GaN	AlN	References
SF_6	RIE	16.7		[29]
CHF_3,C_2ClF_5	RIE	45		[30]
$SiCl_4$[W/Ar,SiF_4]	RIE	55		[31]
$SiCl_4$:Ar:SF_6	RIE	56		[32]
BCl_3[W/Ar,W/N2]	RIE	104		[33]
BCl_3	RIE	132		[34]
BCl_3/Ar	ECR	30	17	[35]
Cl_2/H_2/Ar	ECR	200	110	[36]
IBr/Ar	ECR	300	160	[37]
SF_6/N_2	ICP	67		[38]
Cl_2/SF_6	ICP	130	184	[39]
CH_4/H_2/Ar	ICP	140	30	[40]
Cl_2/H_2/Ar	ICP	688		[41]
Cl_2/N_2	ICP	820		[42]
BCl_3/Cl_2	ICP	850		[43]
Cl_2/Ar	ICP	980	670	[44]

3.2.5 Discussion

Etch rates and profiles can be strongly affected by the volatility of the etch products formed. As mentioned earlier, Table III-8 shows the boiling points of possible etch products for III-V compound semiconductors exposed to halogen- and hydrocarbon-based plasmas. It appears that chlorinated products are more volatile than fluorinated counterparts, thus explaining the higher etch rates achieved with chlorine chemistry. The higher etch rates are obtained with ICP techniques. It has been

[2] the reported etch rate refers to the maximum value obtained from referenced work

demonstrated that the etch-products for nitrides etched in Cl-based gases are $GaCl_x$ and $AlCl_x$. However, the etching mechanism is not yet well understood, since here there is also N_2 that affects the etching. Nitrogen tends to escape though the volatile N_2, much more than though NCl_3.

Table III-8. Boiling points of etch products in dry etching of GaN.

Etching products	Boiling points (ºC)
$AlCl_3$	183
AlF_3	> 1200
$GaCl_3$	201
NCl_3	71
GaF_3	> 1000
NF_3	-129
N_2	-196

The reaction mechanism of GaN in Cl_2-based chemistry is shown below.

$$Ga + xCl \rightarrow GaCl_x$$

$$N + xCl \rightarrow NCl_x$$

$$N + N \rightarrow N_2$$

When only Cl_2 is used, the surface morphology is usually rough. The addition of BCl_3 to the plasma chemistry reduces the etch rate due to less available reactive Cl, but the etch rate is smoother and more anisotropic. Moreover, BCl_3 is also used to etch away surface oxide.

Concerning the different chlorinated gases available, Cl_2, BCl_3, $SiCl_4$, C_2ClF_3, the highest etch rates have been reported with combination of Cl_2 and BCl_3. This is in good correlation with the average bond energies for the gases, i.e. BCl_3 110 kCal/mol, $SiCl_4$ 94 kCal/mol and Cl_2 59 kCal/mol. The lower the bond energy, the more effective is the dissociation in the ICP source to form atomic chlorine neutrals which are the active etchant species.

O_2, H_2, N_2 or Ar have been added to halogen-based plasma chemistries to modify the concentration of reactive species in the plasma or initiate the formation of sidewall polymers to enhance the anisotropy. GaN etch rates doesn't really increased as H_2 was added to the Cl_2/Ar and BCl_3/Ar plasma. Small concentration of N_2 (lower to 40%) allows to obtain higher etch rates in BCl_3-based plasma while it resulted in decreased etch rates with Cl_2-based plasma [45]. Ar helped to stabilize the plasma, thus increasing etch rate and anisotropy, especially for BCl_3-based plasma [45].
Other halogen gases, fluorine-based (SF_6, SiF_4 ..) or bromine-based (ICl, IBr) and hydrocarbonated gases, have also been tested with no effective results. However, SF_6 was added in Cl_2/Ar or BCl_3/Ar mixtures giving different results. For Cl_2-based plasma, the etch rates diminished with SF_6 concentration while the opposite trend was observed for BCl_3 where at low concentration of SF_6 (25%) the BCl_3 dissociation was enhanced.

The maximum etch rates were achieved with low pressure, between 2 and 5 mtorr. Usually, at higher pressures, the etch rates decrease due either to higher ion energies, lower plasma densities, redeposition, or polymer formation on the substrate surface.

As for SiC, for a fixed ICP power, increasing the rf-cathode power allows obtaining higher etching rates. By contrast, the ICP source power doesn't affect so much the etch rate, but rather the roughness.

Concerning the mask, different materials have been used, photoresist, SiO_2, Ni, Cr, NiCr, and baked photoresist. The most successfully ones are SiO_2 or the metallic ones, except obviously Al. Moreover, it has also been reported a stacked mask of photoresist and Al.

3.2.6 First attempts of III-nitrides dry etching

The first etching tests were performed on III-nitrides to realize quickly an efficient etch for AlN resonators using epitaxial AlN on Si substrate as starting material. Since the thickness to etch was moderate (<300 nm), no deep etching was necessary. Moreover, here metallic masks (other than Al) were not possible since they are considered as contaminant for the etching equipment at CNM. Therefore, a photoresist mask layer was used. A similar chemistry than the one used for Al etching was applied to AlN. Cl_2, BCl_3 and N_2 gases were introduced at 7, 25 and 40 sccm respectively, with a RF power of 125 W at a pressure of 325 mTorr, in a RIE equipment (Quad Drytek System) [46]. Under these conditions, the etching profile was enough for our desired application, without microtrenching and with well defined sidewalls. Etching rate was around 80 nm/min.

The same concept cannot be transposed directly to GaN. Obtaining epitaxial GaN on Si substrates to realize resonators was much more complicated. Due to high mismatches in thermal expansion and lattice parameter between GaN and Silicon, there is a huge tensile stress in these layers. Thus the resulted single crystalline GaN directly grown on Si substrate usually presents high defects density. A method to reduce both strain in the layer and defects density consists in using a buffer layer alternating AlN and GaN layers before growing the epitaxial structural layer. Our first idea consisted in using only a 40nm thick AlN layer as buffer, since it can be selectively etched and thus GaN structures can be easily released. However, only the AlN layer was not enough to reduce defects density, as it can be seen in figure 7 of *Chapter 1*. Therefore this concept was not possible to realize. The only form to obtain a GaN layer with good crystalline quality was to use a buffer layer constituted of 40 nm AlN, 250 nm GaN and 250 nm AlN. Then the growth of the 1.6 µm thick single crystalline GaN layer is performed and results in a mainly free of defects and strain layer.
Etching 2.14 µm was more difficult, since more than 20 minutes is required using the same process, the same mask and assuming an etch rate similar to the AlN one. Thus ICP with chlorinated gases should be required. However, these gases are not standardly installed since they are highly aggressive for the ICP equipments and not available at CNM.

To have a direct comparison with AlN, the same recipe was used. The GaN etching rate under these conditions was reasonable (90-100 nm/min) and slightly higher than AlN. However, the selectivity was not very good, and the sidewalls not perfectly vertical (figures 9(a) and (b)).

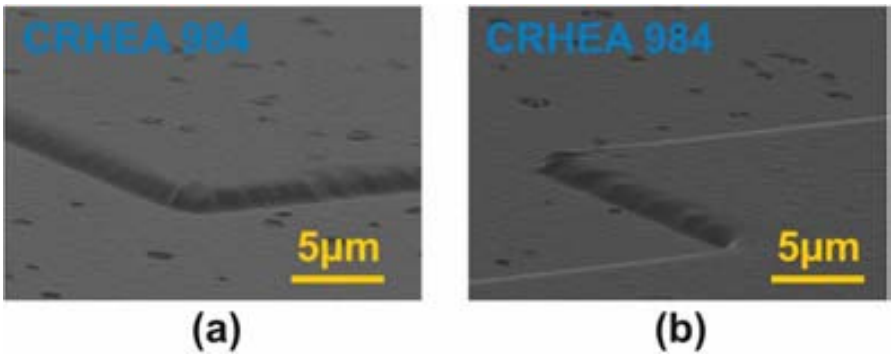

Figure 9. SEM images showing RIE etch profiles obtained with a photoresist mask.

Further investigations concerning GaN etching are actually in process, either using thick photoresist or SiO_2 mask. A SiO_2 mask layer 400-500 nm thick should be probably enough to etch more than 2 µm, but would require around 30 minutes.

The same recipe was applied to an AlGaN layer. This is highly interesting for achieving a complete isolation in HEMT devices, where an etching depth around 150-400 nm in order to fully remove the 2DEG between active regions, is required. A fluorinated etching was also applied to verify eventually the effect on AlGaN surface. A summary of the etching tests and the obtained depth is reported in Table III-9.

Table III-9. AlGaN/GaN etching tests (measured depth) for mesa isolation using $BCl_3/Cl_2/N_2$.

Sample	#1	#2	#3	#4	#5
Process time	**2'40**	**2'40**	**2'40**	**3'**	**3'**
position 1	290 nm	296 nm	330 nm	400 nm	387 nm
position 2	345 nm	371 nm	340 nm	445 nm	448 nm
position 3	340 nm	316 nm	330 nm	445 nm	438 nm
position 4	325 nm	349 nm	340 nm	445 nm	469 nm
position 5	325 nm	354 nm	345 nm	440 nm	444 nm

Two different structures were tested. The average etching rate under these conditions was comprised between 110-160 nm/min using the chlorinated recipe. The first set of samples #1, #2 and #3, which were identical, is etched during 2 min 40, while the second set of samples, #4 and #5 is etched during 3 min. However, since these samples alternate AlGaN and GaN layers, it is difficult to determine an exact etching for each layer. In the first set the etching rate is comprised between 110-140 nm/min while it is comprised between 130-160 nm/min for the second set. However there is an important difference between these 2 sets: in the first the etched GaN thickness is clearly lower than the etched AlGaN thickness while in the second the etched GaN thickness is clearly superior to the etched AlGaN thickness. This seems indicating that the GaN is etched at higher etch rate than AlGaN. Below a brief summary of the obtained etch rate in III-nitrides using the same chlorinated recipe (Table III-10) is presented.

Table III-10. Obtained etch rates using the RIE BCl_3/Cl_2 recipe.

Etch rate ($nm.min^{-1}$)		
GaN	**AlN**	**AlGaN**
100-140	80	110

Etching test with fluorinated etch was also performed using SF_6 chemistry (25 sccm, 150W, 0.07 mbar). With SF_6 in an RIE equipment, the etch rates are usually lower than 10 nm/min (here evaluated around 80 Å/min) and the etched surface often presents pits, probably related to preferential etching where threading dislocations reach the sample surface. This low etching rate could be interesting for recess metal method, and is still under investigation.

3.2.7 Selective etching of III nitrides

As previously seen in the etching test of AlGaN/GaN, since the III nitrides are often used as heterostructures, consisting of alternating AlGaN and GaN layers for example, it could be interesting to obtain etching selectivity between them. In fact, many works have reported etching selectivity with these materials.
The etching selectivity can be performed either using wet (chemical and photoelectrochemical) or dry (ICP mainly) etching.
Taking advantage that AlN is removed in KOH at 85ºC, Mileham et al. reported microdisk laser structures consisting of the GaN/InGaN/AlN stack, after patterning it by $Cl_2/CH_4/H_2/Ar$ dry etching, and then selective etching in KOH solution [47]. Different techniques have been implemented to fabricate GaN resonators etching AlN or InGaN layers used as sacrificial layers. Polycrystalline AlN grown at low-temperature (600ºC) on sapphire substrates by PIMBE or nanocrystalline AlN grown by sputtering at 350ºC have been reported by Zaus [48] and Tonisch [49] respectively. The tendency was to reduce the crystalline quality in order to facilitate the removal of the AlN sacrificial layer. However, GaN structures from [48] presented elevated stresses in structures resulting in bended and buckled cantilevers and bridges. By contrast, structures from [49] were fully relaxed without observed buckling.
Photoelectrochemical etching was also used taking advantage of the different bandgap of III nitrides. Illuminating an III-nitride heterostructure, with a functional material and sacrificial layer with bandgap higher and lower than the photon energy, the required holes for etching are only generated in the sacrificial layer. Thus this allows to selectively etch GaN for example without affecting AlGaN or AlN layers [50].
A PEC etching technology was also developed to fabricate GaN cantilevers [51] based on GaN/InGaN/GaN/sapphire stack. It consisted in first pattern the heterostructure by front-side illumination with high photon energy, and then etching the InGaN sacrificial layer, controlling the light on the backside by a metallic mask, the thick GaN acting as filter and preventing any etching of the GaN top functional layer.
PEC etching can also be dopant selective, as demonstrated by Strittmatter [52] undercutting p-GaN epilayer grown on n-type sacrificial layer.

Lee and al. [53] reported a selectivity of 32:1 between GaN and AlGaN using $Cl_2/O_2/Ar$ (AlGaN with small proportion of Al). Schuette and al. [54] reported a selectivity of 60:1 between GaN and AlGaN using $Cl_2/O_2/N_2$ plasma. Oxigen is here the main factor determining the obtained selectivity. Addition of oxygen slows etch rates of GaN and AlGaN, as it forms stable oxide with Ga (Ga_2O_3) and Al (Al_2O_3), but due to the higher volatility of Ga-containing oxides compared to Al-based oxides, the etching of Ga-containing oxides takes place faster than Al-containing oxides. N_2 acts to dilute the reactive chlorine in the plasma, thus reducing the etch rate, and increasing the O_2 reactivity, enhancing selectivity. Moreover, N_2 is beneficial to obtain smoother surfaces

since N_2-rich conditions favour lower nitrogen loss. Recently, Green and al. [55] reported a $SiCl_4/SF_6$ plasma chemistry giving a selectivity of 14:1 between GaN and AlGaN. Cl2/SF6 is also a good selective etchant of GaN over AlGaN [56]. Both PEC and dry etching techniques are useful for the fabrication of gate recessed in nitride-based HEMTs.

3.3 Summary

Plasma techniques available at CNM have been investigated to etch deeply the SiC and III-nitrides. Different reactors, RIE and ICP have been tried, as well as different parameters and various masks. The work was not rigorously oriented as a full etching study, but rather as development steps directly targetting our applications, based on literatures and on the possibilities offered by the CNM equipments.

The etching of deep features for SiC MEMS structures has appeared feasible, using the combination of ICP with SF_6/O_2 and metal masks or combinations of SiO_2 with metal mask. Addition of O_2 to the plasma chemistry increases the etch selectivity for SiC over Al under some conditions, due to oxidation of the Al. It has been reported in literature that Ni presents a better selectivity than Al and thus allows deeper etches. However, with the aim of fabricating devices, it is better to use Al, since Ni can be problematic and considered contaminant in some plasma equipments. Moreover, Ni often requires Ti to improve the adherence to SiC, and a bi-layer mask is usually more strained (depending to the crystalline quality), thus difficulting the patterning, in particular with thin motives. Thus the retained process for SiC etching was based on the use of ICP reactor with Al mask at flows of SF_6/O_2 at 25/5 sccm, with a pressure around 5 mtorr. ICP and RF power gives satisfactory results for 800 and 150 W values. This configuration allows to achieve etch rates around 300 nm/min. Trenching and micromasking can be clearly improved using bi-layer masks of SiO_2/Al and by using Si wafer or pieces during the etch.

Concerning the III-nitride etching, some limitations, due to the non availability of chlorinated gases in the ICP equipments, have orientated our research with RIE reactor. RIE reactor gives satisfactory results to etch III-nitride layers lower than few micrometers (1-2). Using chlorinated chemistry, $Cl_2/BCl_3/N_2$, at flows of 7, 25 and 40 sccm respectively, with a RF power of 125 W at a pressure of 325 mTorr, and combined with a photoresist mask was the retained process. Different etch rates have been established with this recipe. However, further investigations are in process at CNM, concerning the use of other masks, and the possibility to use chlorinated chemistry in ICP equipment.

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4 CHAPTER IV

SIC RESONATORS

In this chapter we propose to set a technological process for the fabrication of micromechanical structures in SiC using the SiC/Si material. As a first step, back side Silicon etching will be studied with the aim of achieving SiC suspended membranes. Then, based on the etching results obtained in the previous chapter, SiC micromechanical structures will be realized, etching the SiC layer. The different encountered problems are discussed.

4.1 Membranes by Si back side etching

Membrane is the sensing element of many sensors, and particularly pressure sensor, which represents the main part of sensors total market. In Silicon, these devices are based on circular or rectangular diaphragms [1] of some micrometers thick, depending of the sensitivity and pressure to measure. Usually anisotropic etching solutions allow to successfully releasing the desired membrane (figure 1(a)) by using oxide or nitride-based masks.

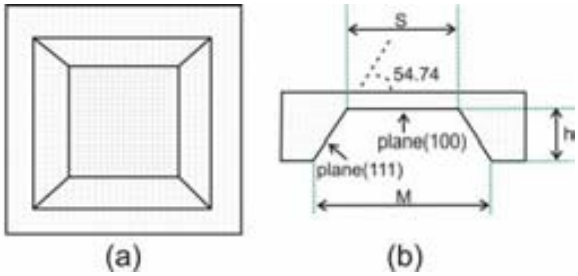


Figure 1. Typical Si micromachined membrane, view (a) etched side and (b) cross section.

Obtaining similar SiC membranes is a little bit more complicated [2]. For such device realization, the well developed Si micromachining technology can be employed. Another possible concept remains on the emerging wafer bonding technology that could allow such devices realization by bonding patterned substrates with WBG structural wafers. Bulk 3C-SiC could also be used but it is obvious that it is easier to etch Si than SiC substrate. In this sense, our study only concerns microstructure fabrication with SiC on Si substrates. Thus a backside wet etching is usually used to release SiC membranes, but dry etching could also be used (with an adequate mask choice). Different wet etchants (KOH, TMAH…) were used, the TMAH giving the best results. The SiC layer is not etched by TMAH excepted in some defects regions, thus acting as etch stop layer.

The first attempts of membranes release from as deposited samples resulted in some problems during the anisotropic etching, principally due to an undesired thin SiC layer formation (tens of nm) on the Si back side during the CVD growth (and Flash Lamp processes). The encountered solution consisted in performing a back side polishing before processing. The membrane fabrication process basically begins by back side SiO_2 deposition (1.5 µm) or eventually by dry or wet oxidation, followed by a photolithography step of the back side, the deposited or formed SiO_2 acting as mask during the wet or dry Si etching. Other successful mask consisted in bi-layers of SiO_2/Si_3N_4 (300/700 nm). The SiC oxidation was not preferred since this step could be critical (SiC thickness reduction, added strain, impact on the SiC crystallinity).

Moreover, other problems were also encountered: (1) the high level of stress near the SiC/Si interface impeding the entire Si etching, (2) the problem of the (111) orientation. The first one was mainly solved by improving the interface of the starting

material. The high anisotropy obtained by using KOH or TMAH results in preferential etching in some orientations, giving different etch rates. Thus, the (100) planes are 100 much more quickly etched than the (111) planes giving structures having the form depicted in figure 1(b). Therefore, to obtain for example a squared SiC membrane with a determined side S, from a Si substrate of thickness h, this effect has to be taken into account during the mask design. The relation is the following:

$$M = S + 2h / \tan(54) \qquad \text{Eq. 4.1}$$

where M and h are respectively the aperture and the depth to etch.

The optical images in figure 2 show the front and back side view of 'non-polished Si back side', with visible remaining Si. With our optimized process, different squared membranes with various dimensions (1 to 4 mm side) were successfully obtained, demonstrating thus the feasibility of membrane-based sensors, such as pressure sensors.

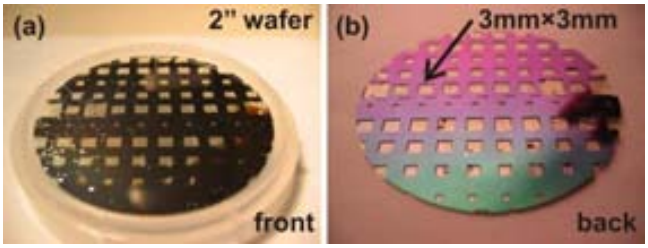


Figure 2. Pictures of bulk micromachined SiC freestanding membranes (a) front and (b) back side view of a 2 inches processed wafer with Si back side not polished (FlaSiC 113).

Several processes with many samples were performed before successfully realizing such membranes. Typical SiC thicknesses for the different samples were between 3-8 µm. It is important to note that the membranes fabrication is highly depending on the material, especially axial residual stresses (cf. *Chapter 2*).

Such a membrane was simulated with Ansys, predicting a resonance frequency around 43.5 kHz considering a Young modulus of 450 GPa, and without taking into account the residual stress. Simulation result can be seen in figure 3.

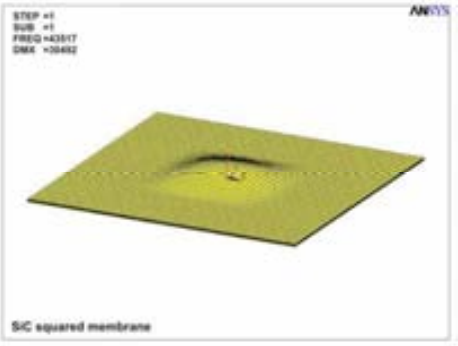


Figure 3. Ansys simulated square SiC membrane – fundamental resonance mode at 43.5 kHz.

4.2 Vertical resonators

The resonators are very useful in the field of high sensing operation. Structures as cantilevers and beams which can oscillate either in vertical or lateral direction are highly interesting, first to evaluate the material properties, i.e. the Young's modulus, the strain but also to determine mechanical parameters as resonant structures, i.e. resonance frequency, quality factors.

To fabricate the first SiC resonators, we have optimized the results obtained from the first attempts of SiC etching combined with the Si well-known etching techniques, dry or wet etching to control underetching and removal of metal mask.

4.2.1 CNM 014 mask: Test structures

This mask has been designed to study the eventual constraints of microstructures. It is a necessary step before realizing more complex devices.

There are different structures for stress measurement: cantilevers to verify the presence of a stress gradient, and bridges, in two different forms, to verify the presence of an axial compressive or tensile stress. The mask has the following aspect:

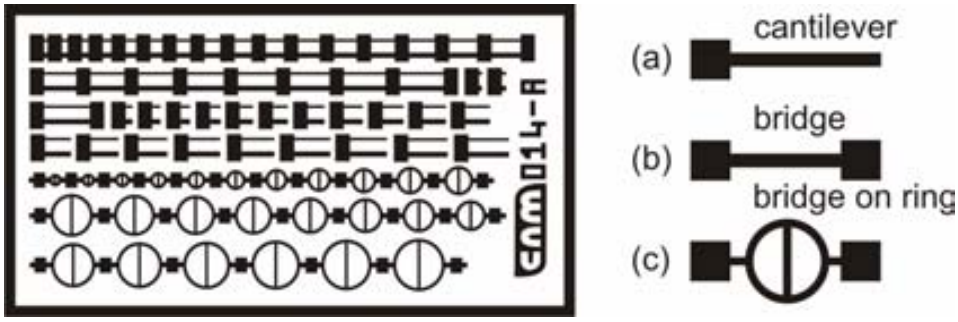


Figure 4. Test structures (cantilever, bridge and bridge on ring) of the mask CNM 014.

The cantilevers, 10 and 20 µm wide, have lengths from 10 to 220 µm, with a 10 µm increment. The bridges, 10 and 20 µm wide, have lengths from 10 to 250 µm, also with a 10 µm increment. The bridges on ring, with only a 10 µm width, have lengths from 30 to 270 µm, with a 10 µm increment. More details can be found in [3].

4.2.2 Resonator fabrication

Main etching process

Figure 5 shows the key process steps for both types of vertical and lateral resonators. The process begins with the deposition of an Aluminum (Al) mask layer on n-type 3C-SiC film [figure 5(a)]. Then, for patterning the resonator geometry, an optical lithography step followed by a dry etching of the Al mask is done [figure 5(b)]. Next, the resonator pattern is defined on the 3C-SiC by dry etching with a SF_6/O_2 plasma in an ICP equipment, the Al layer acting as mask [figure 5(c)]. ICP parameters conditions have been chosen for this optimized process, etch rate of SiC is around ~300 nm/min. Higher etching rates could be obtained with ICP but the lateral over-etch would be

higher, which is not desirable and especially for future low dimension structures. Dry etching selectivity with Al mask is evaluated to be 1/7, which is better than with SiO_2 mask. Finally, the Al mask is stripped and the devices are released by $HF:HNO_3:H_2O$ (7:5:1) isotropic wet etch [figure 5 (d)]. This mixture, chosen to its etch isotropy, by contrast to KOH or TMAH that allows etch anisotropy, provides a non linear Si etch rate (probably to the decrease of solution reactivity), but with an average rate around 200-150 nm/min. No protection of the single SiC layer should be needed since SiC is acid resistant, but can sometimes be required to protect some defects etching mechanism (through Si clusters for example). Using TMAH solution, heating, up to 80ºC, is sometimes required.

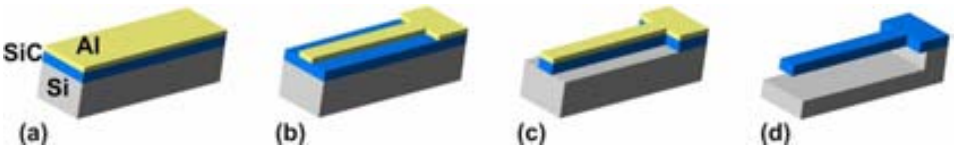


Figure 5. 3C-SiC on Si resonators fabrication process: (a) Deposition of an aluminium mask layer, (b) Optical lithography and Al patterning, (c) ICP dry etching, (d) Isotropic wet etching in $HF:HNO_3$ mixture.

Metallic contacts formation

Metallic contact pads can also be included in the process either before the SiC etch step, or just before the final Si etching. For this, an implantation (Phosphorus+Nitrogen) step [4] not shown here (with subsequent annealing around 1300ºC) has also been tested and could be required depending of the doping of the epitaxial layer (for eventual posterior contacts formation) but could result in stress increase and difficulty to follow with the process, especially after eventual implantation annealing. More details will be given in the next section concerning electrostatic resonators. The choice of metal is particularly important since it has to allow both good ohmic contact characteristics and compatibility with the Si etch process.

4.2.3 The different generations of fabricated resonators

This first resonators run was done with a mask set with various vertical structures of several sizes, cantilevers (width: 10 and 20 µm, length: from 10 to 240 µm), bridges and bridges inserted in ring (width: 10 and 20 µm, length: from 10 to 270 µm), in order to investigate the eventual curvature that the microstructures could show. The curvature of the microstructures indicates the presence of stress or stress gradient inside the layers. In past, many fabricated devices have shown spectacular bending and curvature, indicating the presence of high stress in the layer, as described in the *Chapter 2* and shown in figure 6 [5].

The results in achieving successful structures strongly depend on the starting material. Thus growth has to be performed with this objective, trying to reduce as much as possible stress levels, surface roughness, surface defects, that could be detrimental for micromechanical structures.

Several processes with different starting SiC/Si materials were performed before achieving satisfactory results. Many difficulties were encountered during the different etching and release tests of the structures mainly due to the starting material quality and structure. Another problem relied on the difficulty to control their exact geometry. This

problem was identified to come from the overetching of the Al mask layer either during its definition or during the SiC etching with unoptimized process, and could be very problematic for small dimensions structures. In the first processes, the Al mask was patterned with AlEtch. However, chemical etching is isotropic and thus resulted in some loss of mask dimensions. For this reason we then decided to use dry etching for the mask pattern definition.

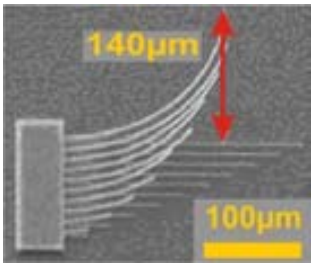


Figure 6. Influence of stress gradients on SiC cantilevers (Courtesy of Christophe Serre, Universitat de Barcelona).

First generation

On the SEM images of figure 7, the first tests of resonator fabrication on different samples can be observed.

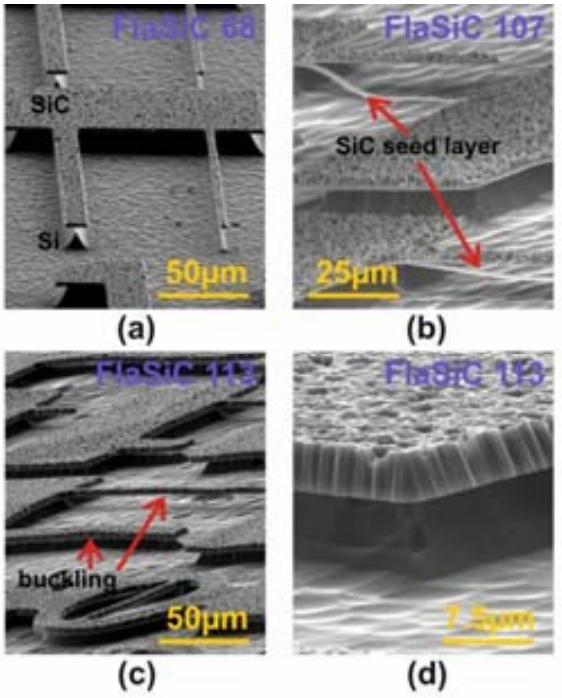


Figure 7. First attempts of SiC resonator fabrication with an Al mask using different processes and samples. (a) View of cantilevers after SiC dry etching, FlaSiC68, (b) Al mask entirely etched resulted in damaged SiC surface, FlaSiC107, (c) Buckling effect on structures, FlaSiC113 and (d) Zoom of figure 7(c), FlaSiC113.

In a first attempt, only the ICP process was applied, and the Si was in part over-etched during this step, demonstrating that only a dry etching step is enough to release small SiC devices, as it can be observed in the figure 7(a). A thin Al mask layer of 1 µm was used for the first attempts, being in some cases problematic as it can be observed in the sample of the figure 7(b). Here, the Al entirely disappeared after the ICP process, thus damaging considerably the SiC layer. Different solutions were tested to avoid the total mask etching: adjusting the ICP parameters to decrease slightly the etching rate and/or the etching time, and using a thicker Al mask layer, up to ~ 1.5 µm. In the sample shown in figures 7(c) and 7(d), the process parameters were slightly adjusted and resulted in a more aggressive etch due to the elevated attained etching rate. It is interesting to note the buckling in the structures in figure 7(c) due to the high lattice mismatch between SiC and Si, resulting in a bowing of the wafer.

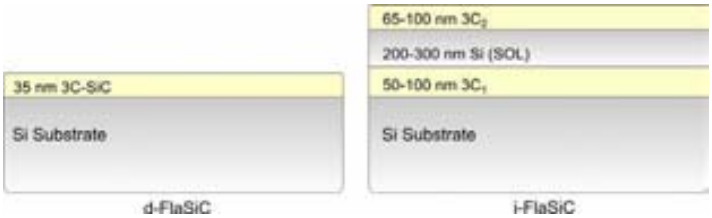


Figure 8. Schematics of the different FlaSiC processes, showing the layers submitted to the irradiation.

In the figure 7(b), a thin layer seems detached from the interface of the structures. This layer is probably a thin SiC layer of bad crystalline quality. Briefly, two FlaSiC processes were basically used, the first one, called FlaSiC (or d-FlaSiC, d for direct), based on the irradiation of the SiC/Si interface, and another one, called i-FlaSiC (i for inverse) based on the irradiation of the Si/SiC_1 interface (where SiC_1 is the seed layer). In the i-FlaSiC process, a thin Si layer (SOL for Silicon Over Layer) is introduced between the SiC seed layer, SiC_1 or $3C_1$ and a cap SiC layer, SiC_2 or $3C_2$. This SOL just serves during the FlaSiC process. The $3C_2$ cap layer and SOL are then etched before the SiC regrowth. More details on both methods can be found in [6]. Therefore, in some cases, it is possible that a thin SOL remains, resulting in a bad crystalline quality of the top 3C layer on top. Therefore the suspended thin layer could be the SOL one.

Second generation

In another attempt of resonator fabrication, other problems were encountered. Figures 9(a) and 9(b) show two different areas of the same sample, respectively at the center and edge of the wafer.

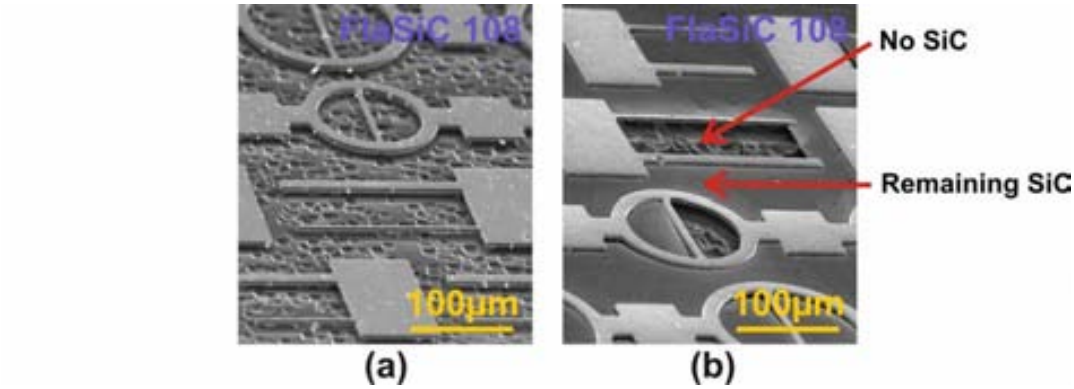


Figure 9. SEM images of some structures located at the (a) center and (b) edge of the wafer. The structures at the center are entirely released, by contrast to those located at the edge of the wafer.

The SiC layer was entirely etched at the center by contrast to the edges, resulting in devices not entirely released at the extremity of the wafer. In figure 9(b), the Si has been probably underetched through defects or through microtrenches, as shown in figure 10(a). The degradation of the Al mask during the dry etching is also visible since part of it still remains in this figure, resulting in clearly visible microridges along the section of the structure. However, this problem is directly related to the Al mask definition through chemical etch, resulting in a slight Al overetching and loss of the real dimensions of the devices (figures 10(a) and 10(b)). Here, by contrast to the first generation, no micromasking was observed, since an anti-µmask ring was used, as well as a support coated with Al.

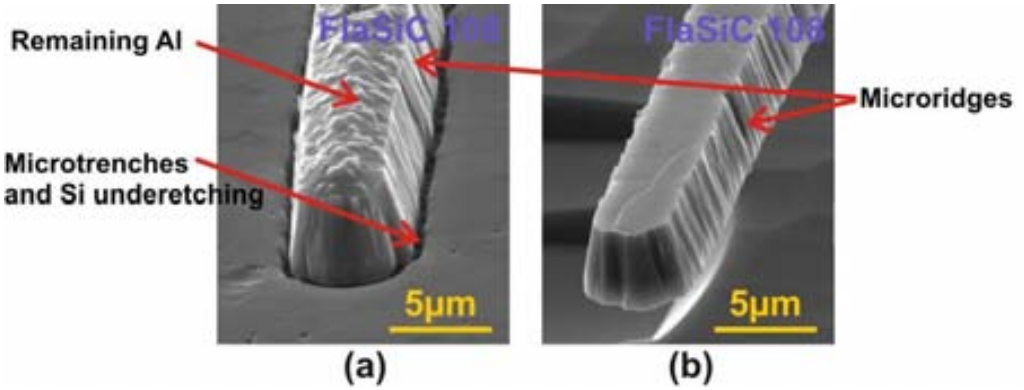


Figure 10. SEM images of a SiC cantilever after Si etching
(a) not totally released due to incomplete SiC etching, with visible microtrench, and underetching of the Silicon below the cantilever (note: Al mask is still present)
(b) perfectly released at the center of the wafer (without Al mask).

Third generation

An Al mask definition by dry etching in a Quad equipment (Quad Drytek System) has clearly improved the aspect of the vertical sidewall, the structures presenting rectangular section very well defined, as shown in figures 11(a)(b)(c) and (d). This was basically obtained by improving the Al etch process but also by improving the starting material as described below.

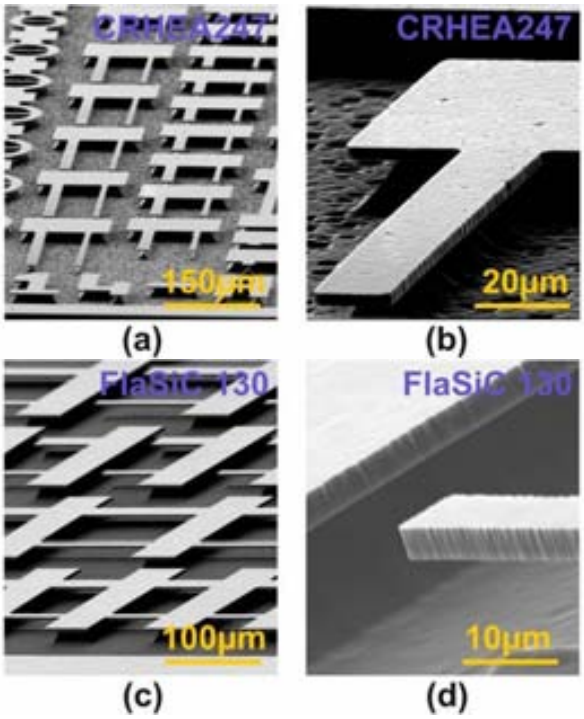


Figure 11. SEM images showing the successful and validated fabrication process with Al dry etching, (a) General view, CRHEA247, (b) Zoom of figure 11(a), CRHEA247 (c) General view, FlaSiC130, (d) Zoom of figure 11(c), FlaSiC130.

The figure 12 shows a summary of the realized progresses both in the process and in surface quality, depending of the CVD growth process used during this work. It is important to note that all the samples called 'FlaSiC' are not always done using the FlaSiC process. In figure 12(a) we can observe a strong roughness of the SiC surface. This is typical of standard CVD deposited layers, which can exhibit surface roughness higher than 500nm. Here the material is also probably polycrystalline. This is not really desirable for device fabrication since it highly affects the quality factor of the structure.

Through a collaboration with LMI, CRHEA and NovaSiC [7], many adjustments were proposed to obtain improved crystalline quality of the 3C-SiC layer on Si, basically by changing the CVD process parameters. One of them was to use a Flash Lamp Annealing process to reduce the defects and strain of the layer. This consists on using a flash light with an intensive pulse after the carbonization step in order to improve the SiC film quality at the interface (for more details see ref. [8]). Another method, the checker-board solution, was used to reduce significantly the wafers bow.

This technique consists on the alternate deposition of compressive and tensile areas (see figure 13), obtained by tuning the substrate temperature when the very first molecules of propane are introduced into the reactor (for more details see ref. [9]).

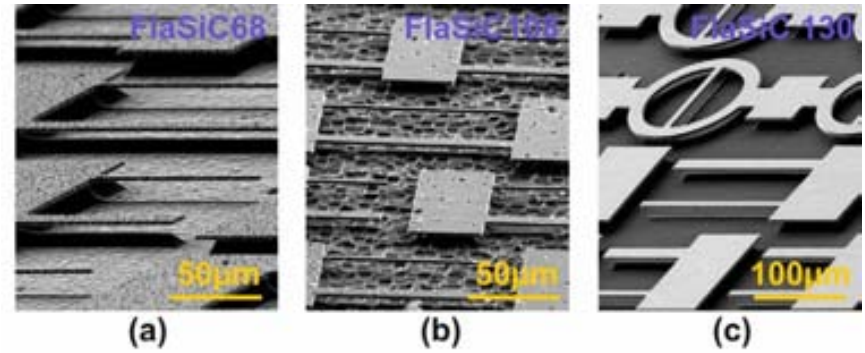


Figure 12. Generations of fabricated vertical resonators, (a) FlaSiC68: Standard 3C, 4.9 µm thick, (b) FlaSiC108: i-FlaSiC, 4.5 µm and (c) FlaSiC130: standard 3C, 4.3 µm.

Basically, depending of the substrate carbonization conditions, the resulting constraint is tensile or compressive but the experimental conditions are so close that it is not possible to use an intermediate temperature compensating these 2 phenomena. Thus a SiO_2 layer is deposited at CNM through a checkerboard mask: the first carbonization can be performed and by removing the SiO_2 mask with HF, then the second one allows to obtain the desired effect. The carbonization order has no really importance, but for a same surface ratio 'compressive/tensile' the obtained layers are always tensile. Thus the obtained wafer is relatively plan, with low bowing and ready for SiC homoepitaxy on this formed checkerboard. However, in this work, there is no sample with the checker board process.

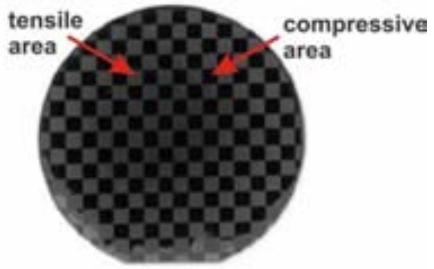


Figure 13. Aspect of checkerboard 35 mm wafer showing tensile (light) and compressive (dark) areas (Courtesy of LMI, Lyon).

Moreover, by a polishing process after CVD SiC deposition, the roughness was efficiently reduced. All these changes on CVD process were optimized to achieve the best quality of SiC layer possible, with poor density of clusters and holes, with low bow, and with moderate strain, resulting on a very promising material for mechanical devices. The quality of the obtained SiC wafers is very good and most of the typical microelectronics processes, such as lithography step, become realizable on these wafers.

The evolution can be clearly seen in figure 12: in the picture (b), we can see the presence of pits in the SiC layer after Si wet etching step. These holes are due to the etching of the clusters of Si included in the SiC layer during growth. In picture (c), the CVD process has been optimized to reduce significantly the presence of Si clusters,

resulting in perfect smooth SiC surface without holes. In addition, the modification of the CVD process has not increased the stress of the layer. So, no appreciable bending of the cantilevers or bridges was detected on any of the fabricated structures, as it is observed in picture (c), indicating that they are almost free of residual stress.

Any of the fabricated structures (cantilever, bridge or bridge inserted in ring) did not present significant curvature even on the long devices. This indicates both a low compressive stress and a low stress gradient.

The optimal ICP parameters for the SiC resonators etching process, are summarized in the Table IV-1 below:

Table IV-1. Main ICP parameters used for SiC dry etching.

Flow gases	SF_6/O_2 25/5 sccm
Pressure	5 mtorr (0.67 Pa)
Coil Power	800 W
Platen Power	150 W
Temperature	18ºC

In conclusion, close collaboration with the research groups working on SiC growth has allowed to establish an optimized SiC/Si technological fabrication process for SiC resonators. SiC micromechanical structures, cantilevers and bridges, very flat, without any apparent curvatures, with well vertical sidewalls and perfect rectangular cross-section, have been successfully fabricated. For this, different improvements, both in growth process, such as FlaSiC technique, polishing, etc... and in fabrication, such as mask choice, mask definition, ICP parameters adjustments… have been required. In the next section, we will treat about mechanical characterization of these fabricated structures. All the samples were sufficiently etched resulting in a high distance from cantilever to substrate, allowing a correct vertical displacement of the devices.

4.2.4 Mechanical characterization

The mechanical properties characterization of the first fabricated SiC vertical mode resonators have been performed using AFM [10] and from the direct observation of the resonant properties such as resonance frequency and quality factor. One method used for actuation is by the use of a piezoelectric (PZT) actuator (shear or horizontal). The devices samples were glued on a piezoelectric (PZT) disk. By applying a sinusoidal voltage coming from a waveform generator, we obtain vibrations of the whole sample. The sample vibration amplitude is lower than PZT disk and is not known precisely, but is sufficient to provide mechanical excitation and to detect the resonance. A CCD camera or an automated interferometric system [11] is used to measure optically the mechanical characteristics(for more details see *Annex A2*).
Using this mechanical method for the vertical structures, the fundamental resonance frequencies for the first and second vibration modes have been measured for different aspect ratios (length/width). The resonance frequency values varied from the different samples due to the different epitaxial SiC layer thicknesses.

Cantilevers

No cantilever presented curvature, indicating low stress gradient in all the samples. Some values comparing the theoretical and measured resonance frequencies for vertical cantilevers and bridges are listed in Tables IV-2 and IV-3 for 2 material

generations (FlaSiC68 and FlaSiC130). The theoretical and measured resonance frequency dependence with cantilever length for first and second mode of sample FlaSiC 130 is also plotted in figure 14.

Table IV-2. Theoretical and experimental resonant frequencies for the first vibration modes of vertical cantilevers with various lengths of sample FlaSiC68 (t 2.5, E 400).

Cantilever length (µm)	width (µm)	220	200	180	160	140	100
Theoretical frequency (kHz)[3]	--	93	113	140	177	231	452
Simulated frequency (kHz)[4]	20	90	109	133	168	218	416
	10	91	110	136	171	222	428
Measured frequency (kHz)[5]	20	89	108	133	166	221	436
	10	90	109	135	169	224	449

The measured resonance frequencies comply quite well with the theoretical frequency relation (Eq. 2.10). However, the resonance frequencies for larger cantilever are always lowers, and this is especially true for a length lower than 150 µm for the 20 µm width cantilever, and for a length lower than 90 µm for the 10 µm width cantilever. It seems that the relation (Eq. 2.10) is well suited for length/width ratio superior to 8.

Table IV-3. Theoretical and experimental resonant frequencies for the first vibration modes of vertical cantilevers with various lengths of sample FlaSiC130 (t 4, E 455).

Cantilever length (µm)	width (µm)	220	200	180	160	140	100
Theoretical frequency (kHz)[6]	--	158	192	237	300	392	768
Simulated frequency (kHz)[7]	20	153	184	226	284	367	698
	10	155	186	229	289	375	719
Measured frequency (kHz)[8]	20	164	197	240	301	376	broken
	10	168	200	244	307	396	749

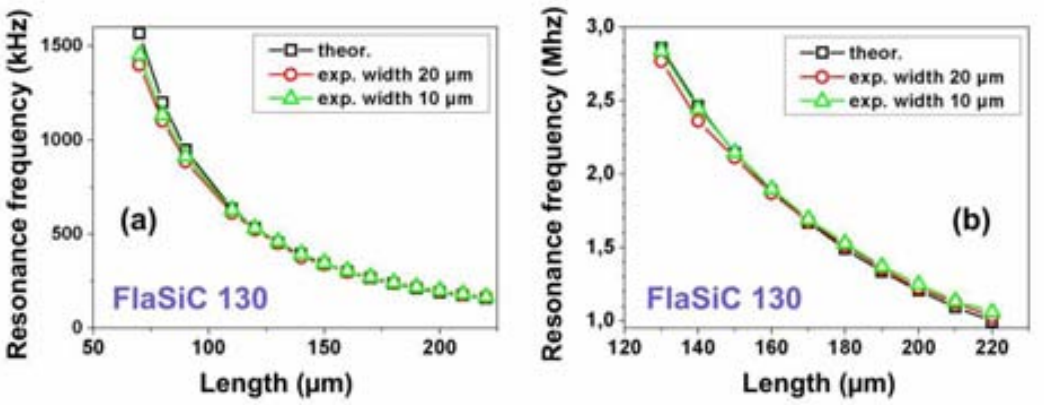


Figure 14. SiC cantilevers resonance frequency for the (a) 1st mode and (b) 2nd mode for different length/width ratio.

[3] From Eq. 2.10
[4] From FEM with Ansys (the first line corresponds to width 20 µm while the second line to 10 µm)
[5] The first line corresponds to width 20 µm while the second line to 10 µm
[6] From Eq. 2.10
[7] From FEM with Ansys (the first line corresponds to width 20 µm while the second line to 10 µm)
[8] The first line corresponds to width 20 µm while the second line to 10 µm

The measured cantilevers fundamental frequencies for the first mode ranged from 80 kHz to 1.5 MHz and from 1 MHz to 2.8 MHz for the second mode.

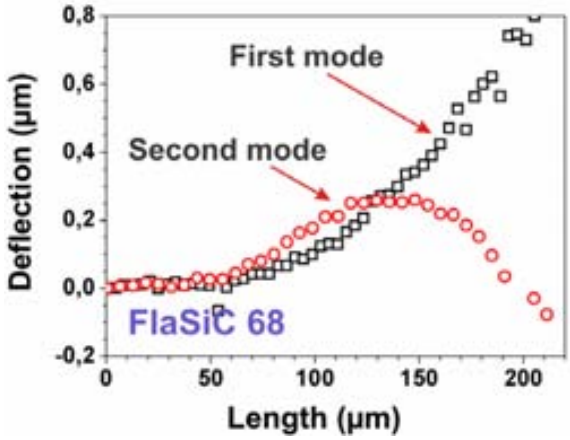


Figure 15. Deflection along the cantilever for the first and second vibration modes of a free beam 220 µm long (FlaSiC68, 1st and 2nd mode at 106.9 and 661 kHz respectively).

The figure 15 shows the deflection of a 220 µm long cantilever for the first and second vibration modes respectively. This measurement was performed using an automated interferometric system that allows recording the amplitude of the deflection along the structure.

Bridges

None of the bridges presented buckling, indicating no compressive stress in the SiC layer. Bridge resonance frequencies have also been measured for different lengths and ranged from 1.2 MHz to 2.8 MHz, as summarized in Tables IV-4 and IV-5 for samples FlaSiC68 and FlaSiC130. The theoretical and measured resonance frequency dependence with bridge length for the first mode is also plotted in figure 16(a) for the sample FlaSiC130.

Table IV-4. Theoretical and experimental resonant frequencies for the first vibration modes of vertical bridges with various lengths of sample FlaSiC68.

Bridge length (µm)	width (µm)	220	200	180	160	140	100
Theoretical frequency (kHz)[1]	--	593	718	886	1122	1465	2873
Simulated frequency (kHz)[2]	20	547	656	799	993	1265	2258
	10	676	702	828	1036	1331	2449
Measured frequency (kHz)[3]	20	903	1015	1173	1358	1641	--
	10						

The measured values varied significantly (20%) from those obtained from equation (Eq 2.10). This was attributed both to the tensile stress influence in bridges but also to the over-etching length influence. As described in *Chapter 2*, the stress could increase the resonance frequencies of bridge structures. But the over-etching has also to be considered in bridge devices, since the two extremities are exposed during the isotropic release. Figure 16(b) shows a theoretical fit taking into account stress and overetching, with used values of 220 MPa and 10 µm respectively. With these introduced corrections, the theoretical values fitted very closely the experimental ones. That is interesting to note is that initially most of the 3C samples from LMI (and CRHEA) were

compressively stressed. Upon bridges resonator release it seems that the stress turns from compression to tension.

Table IV-5. Theoretical and experimental resonant frequencies for the first vibration modes of vertical bridges with various lengths of sample FlaSiC130.

Bridge length (µm)	width (µm)	220	200	180	160	140	100
Theoretical frequency (kHz)[1]	--	1013	1225	1513	1915	2501	4052
Simulated frequency (kHz)[2]	20	920	1099	1337	1657	2105	3719
	10	947	1137	1389	1733	2220	4048
Measured frequency (kHz)[3]	20	1210	1400	1640	1971	2449	--
	10	1242		1700		2504	

No second mode was observed for the bridges since the resonance frequencies theoretically estimated were higher than 3 MHz for the longer structure, which was the maximum detectable frequency.

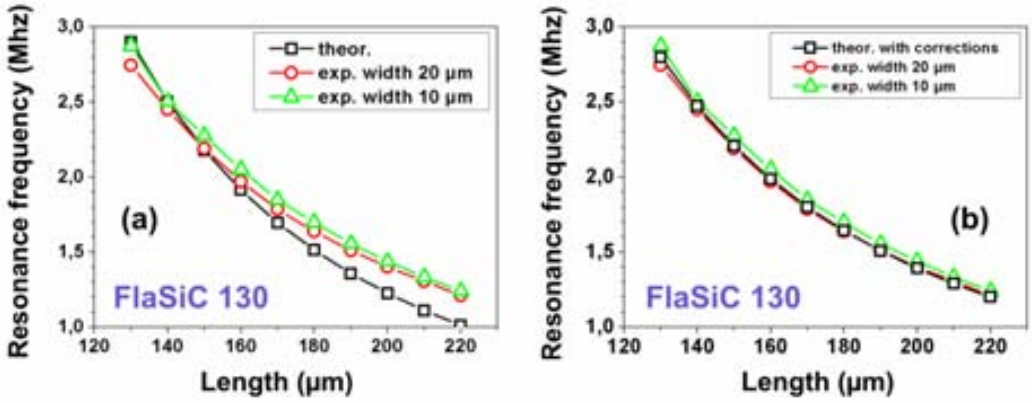


Figure 16. SiC bridges resonance frequency for the 1st mode for different length/width ratio with (a) theoretical frequencies without stress and length correction, (b) theoretical frequencies with stress and length correction.

Young modulus

From all these measurement results, performed in air, a Young modulus in the range of 455 GPa has been evaluated, which is among the highest reported values [12]. The residual tensile stress was determined to be very moderate for the SiC layer, around 200MPa. The figures 17(a) and (b) show the amplitude of the vibration of a 200 µm long cantilever as a function of frequency, for the first and second mode. In this case, the resonance frequency was 195 and 1225 kHz for the first and second mode respectively, and the quality factor was 65 and 490. We can note that the vibration amplitude is not very high, lower than 1 µm for the first mode, and lower than 250 nm for the second mode. It is interesting to note that the first and second modes present similar maximum amplitudes. This is because the voltage applied to the PZT actuator was adjusted to obtain an amplitude vibration comprised between 90 and 120 nm, which is the best range to detect the movement with the measurement set-up.

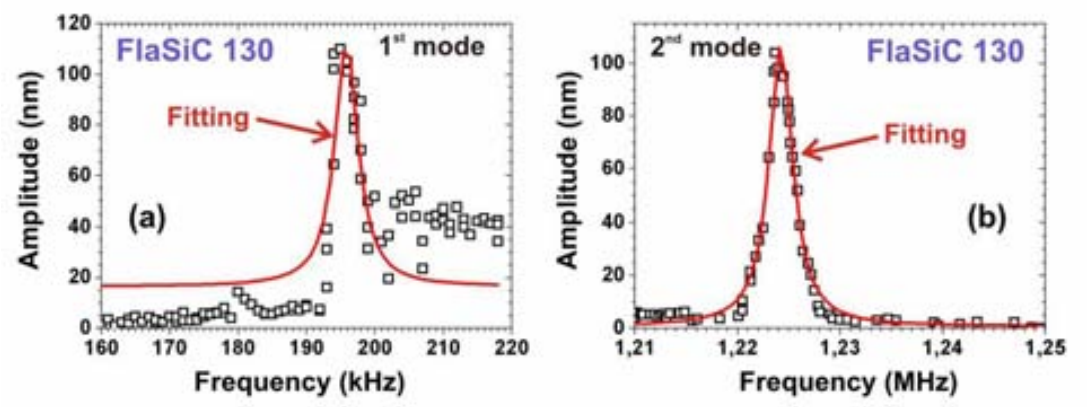


Figure 17. Fundamental resonance peaks for a 200 µm long vertical resonator obtained with the automated interferometric system
(a) mode 1, f_0 = 195.5 kHz, A_{max} = 109 nm, Q = 65
(b) mode 2, f_0 = 1224.25 kHz, A_{max} = 97.5 nm, Q = 490

Quality factor

The quality factor values are always more elevated for higher modes. It is a typical and easy method used by many groups to improve the quality factor of resonators [13]. However, others methods exist to improve the quality factor of the fundamental mode.

We have measured the quality factor of the resonance fundamental mode for different lengths in air ambient. The experimental quality factor-length dependence is shown in figure 18. Q varied from 75 to more than 1000 according to the length. The effective Q is the result of several losses mechanisms, which are related to intrinsic or extrinsic processes. The intrinsic loss is mainly related to internal friction in the structure and the support loss at the anchor of the cantilever, while the external loss is correlated to the radiation damping that depends on the coupling with the surrounding medium. Yang [14] discussed about four mechanical energy losses acting in Si cantilevers, and estimated the Q-factor of a resonator to be:

$$\frac{1}{Q} = \frac{1}{Q_{air}} + \frac{1}{Q_{TED}} + \frac{1}{Q_{clamping}} + \frac{1}{Q_{others}} \qquad \text{Eq. 4.2}$$

where Q_{air} is the air damping Q-factor, Q_{TED} the thermoelastic loss dissipation Q-factor, $Q_{clamping}$ the support loss (anchor or clamping) Q-factor and Q_{others} the related one with other energy losses (bi-layer, surface or volume effects, etc...).

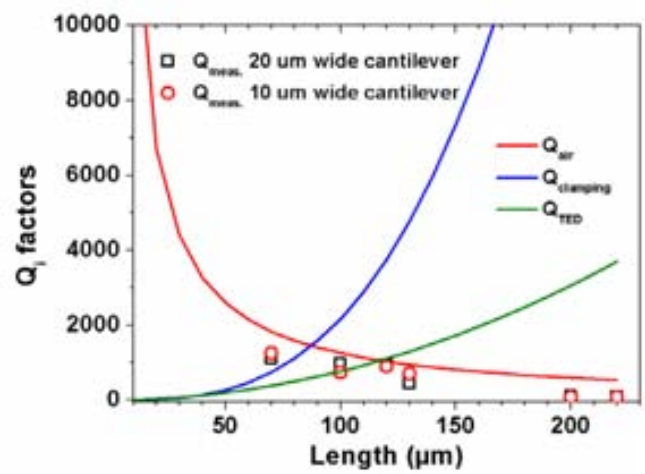


Figure 18. Measured quality factor of the fundamental mode for cantilevers with various length/width ratio and Q_i factors associated to the different energy losses.

The different Q factor corresponding to the above-cited energy losses can be described by the analytical expressions:

- $Q_{air} = \frac{\lambda_n^2 \sqrt{\rho E}}{12\pi\sqrt{3}} \frac{wt^2}{LR(1+R/\delta)\mu}$ Eq. 4.3 with λ_n the vibration mode coefficient defined in *Chapter 2*, R the effective sphere radius, δ the boundary layer thickness, μ the viscosity of the surrounding air.
- $Q_{TED} = \frac{C_p}{\alpha_T^2 ET} \frac{1+(w_0\tau_r)^2}{w_0\tau_r}$ Eq. 4.4 with $\tau_r = \frac{\rho C_p t^2}{\pi^2 k}$ the relaxation time, C_p the specific heat at constant pressure, α_T the coefficient of linear thermal expansion, w_0 the angular resonant frequency and k the material thermal conductivity.
- $Q_{clamping} = \beta\left(\frac{L}{t}\right)^3$ Eq. 4.5 with β a coefficient ranging from 0 to 2.2, depending of the resonant mode.

The calculated Q-factor of SiC cantilevers after considering the different loss mechanisms using (Eq. 4.2) were calculated, as well as the different contributions. In figure 18 it appears clear that the predominant mechanism for energy dissipation is air damping, at least for length lower to 90 μm. The material properties used in calculation are listed in the Table IV-6.

Depending of the design, resonance frequency and quality factor can be optimized. For example, bridges presented higher quality factors, comprised between 500 and 1500. However, 2nd modes were not possible to detect with this set-up for the above explained reasons.

Table IV-6. Material properties used for the quality factor terms.

Parameter	Units	3C-SiC	References
Air damping			
Vibration mode coeff. λ_n	--	1.875	*Chapter 2*
Density ρ	kg/m^3	3200	*Chapter 1*
Young modulus E	GPa	455	This work
Air viscosity μ	Kg/(s.m)	1.83×10^{-5}	[15]
Thermoelastic dissipation			
Specific heat C_p	J/(kg.K)	675	[16]
Thermal expansion coeff. α	K^{-1}	2.77×10^{-6}	[17]
Thermal conductivity K	W/(m.K)	490	[16]
Clamping loss			
Clamping coeff. β	--	1570	This work

We have reported only the results for the last and best sample, FlaSiC 130, but different samples were previously used for resonators fabrication. Some of them were characterized, and mechanical parameters extracted. Below appears a table (table IV-7) with the different Young's modulus from different samples. The main difference between these samples was the growth technique and parameters. We can see that the Young's modulus depend on the material growth conditions. However, FlaSiC 68 and FlaSiC 130 samples were similarly processed. Therefore, the difference in young modulus cannot be only explained from a growth point of view. In fact, the roughness of the surface of the resonators could affect the resonance frequencies, and by the way, the Young modulus determination.

Table IV-7. Young's modulus obtained from different SiC resonators samples.

Sample	Young modulus (GPa)
FlaSiC68	398
FlaSiC107E	--
FlaSiC108E	412
SiC247	395
FlaSiC130	455

Young modulus as a function of temperature

Measurements of Young modulus with temperature have been performed. However, for these structures, requiring a external excitation mechanism, it was not possible to measure at temperature higher than 80ºC since the PZT disk, used for structures mechanical actuation, put on a typical Peltier heater, begins to degrade seriously around 80ºC. The results of the fundamental resonance variation as a function of temperature on a 210/20 µm long/wide vertical bridge resonator are shown in the figure 19 below.

From this measurement, the resonance frequency varies very slightly with temperature up to 80ºC, from 1186.6 to 1189 kHz, so less than 0.5%. In this range, the variation is linear and gives a temperature sensitivity of +40 Hz/ºC (+42 ppm/ºC). Since the density could be considered constant in this range, the temperature shift is mainly due to the Young's modulus variation.

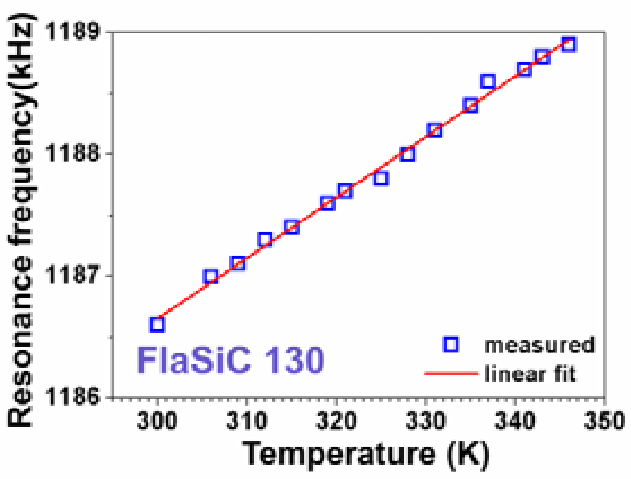


Figure 19. Linear dependence of the resonance frequency with temperature up to 80ºC.

4.2.5 Summary

This first set of SiC resonators based on mask set CNM014 allows us to optimize the technology at CNM simultaneously with the improvements in the CVD growth through the different collaborations, to perform successful integration of SiC microstructures. The SiC mechanical properties have been extracted and superior characteristics, compared to Si equivalent devices, have been demonstrated: the resonance frequencies of these structures have been evaluated to be 60-70% higher than those of equivalent Si device and, the quality factor is also increased by more than 50 %. The Young modulus was evaluated in the range 395-455 GPa. Measurements with temperature were also performed until 80ºC and revealed SiC temperature highly resistant, at least until this temperature, even if its potential is much higher.
In order to take fruitfully profit of these superior characteristics, in a second step we have decided to carry on the optimization of the SiC technological process by the realization of smaller devices, and the integration of electrostatic actuation/detection, which will allow the temperature measurements in a wider range.

4.3 SiC electrostatic lateral resonators

In a second phase and once optimized the CVD deposition process and SiC etching for optimal vertical mode resonator fabrication, a second mask set has been designed with lateral mode resonator exhibiting much smaller features. These structures are specially designed to be excited/measured electrostatically, and some structures have 3, 4 or 5 electrodes to eventually improve the readout signal. This design was motivated by the fact that an intensive work on electrostatic resonators has been done at CNM using Si, and the idea was to apply the same concept to SiC.

4.3.1 CNM SiC 013 mask

The mask design has been realized with CADENCE program. There are 2 mask levels, one for SiC and Si etching, and the other for metallization. The elemental field has a size of 7.5 mm by 5 mm. It is constituted of 6 lines with 6 different structures (figure 20). All these structures are designed to resonate laterally.
The series R, X, Y, Z and the last line correspond to different structures.

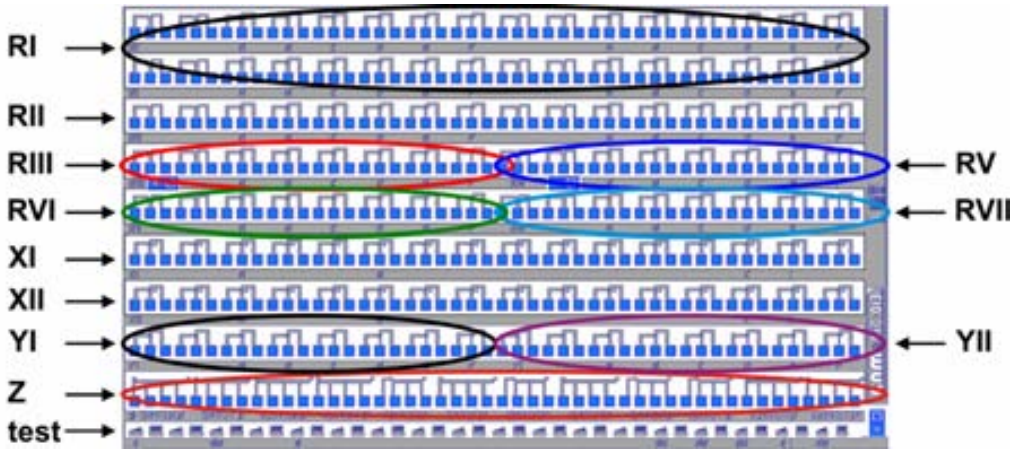


Figure 20. CNM-SiC 013 mask with various lateral electrostatic devices.

The serie R is constituted of different dimensions cantilevers destined to be excited electrostatically. There are 2 models for this serie, as shown in figures 21(a) and (b): one model with an actuation electrode and another model with 2 electrodes.
The serie X is constituted of identical structures to the R serie, with the difference that a triangular electrode is present in front of the cantilever (figure 21(c)). This was to eventually put a drop closer to the cantilever.
The serie Y is very similar to structures of serie R, the difference being here that we have two coupled cantilevers forming a structure called diapason (figure 21(d)). This kind is expected to improve the readout signal.

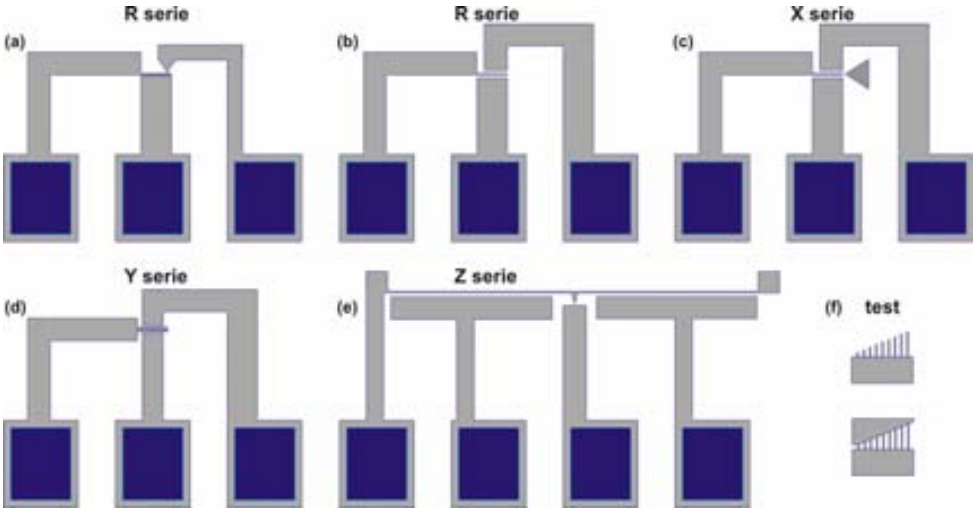


Figure 21. The main tructures of the CNM SiC 013 mask.

The serie Z is a serie that allows measuring the tunneling effect current (figure 21(e)). These structures are constituted of bridges up to 500 µm long for 1 µm width.
Finally the last line is constituted of test structures (figure 21(f)): cantilevers and bridges with different widths and lengths. Other test structures are also present.
All the dimensions of the different structures are detailed in the technical note [18]. Microcantilevers width varies from 2.5 to 1 µm. Below (figure 22) the number of fields on a 50 and 35 mm wafer can be seen. In 35 mm wafers, 14 entire chips are available.

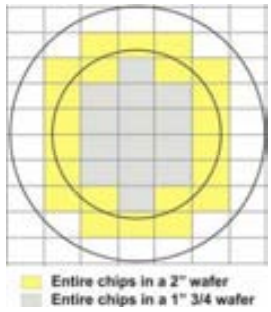


Figure 22. Chips repartition on a 35 mm and 2″ wafers.

4.3.2 Lateral resonator fabrication

The fabrication process is similar to the developed one for vertical resonators. The main differences results in the essential need of using metal masks, due to the etching of some µm thickness with very thin patterns (width). Moreover another level is required for the metallic contact pads and can be also included in the process either before the SiC etch step, or just before the final Si etching.

As described in the *Chapter 2*, an electrostatic resonator is made of electrodes. Most of them designed in the mask are constituted of two parallel electrodes, one for the cantilever excitation, and the other for detection.

Here the movement has to be in plane, lateral, by contrast to the previous vertical structures with out plane movement (vertical). To favour a lateral movement, it is important to fabricate resonators with a thickness larger than the width. Typically, 3C-SiC epi-layers are between 3-5 µm thick, thus lateral dimensions smaller than 3-5 µm width are required.

Moreover, using lateral movement is beneficial to obtain resonance frequencies reliabibility, since the resonance frequency is determined here by the width, and does not depend of possible 3C-SiC layer thickness variations, as it has been observed for vertical resonators.

Etching process

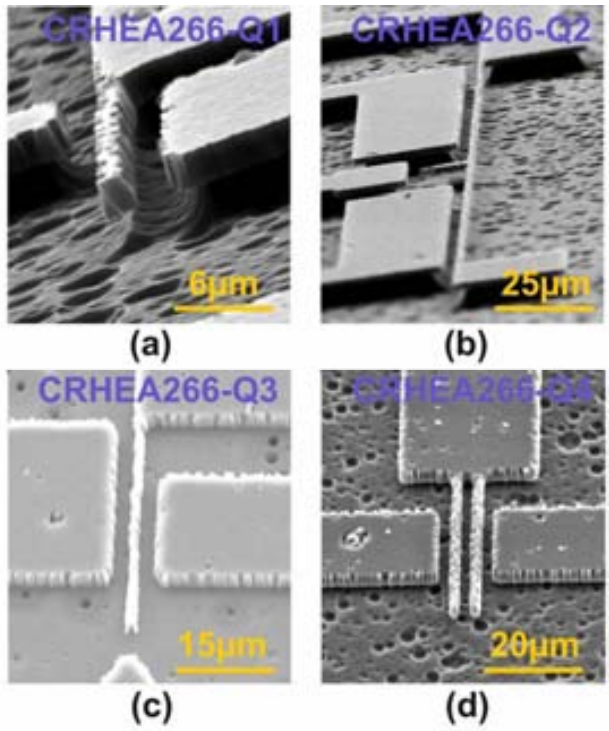


Figure 23. First attempts of releasing thin motives resonators (a) cantilever from sample 266-Q_1, (b) beam from sample 266-Q_2, (c) cantilever from sample 266-Q_3 and (d) diapason structure from sample 266-Q_4.

As previously, the critical step for successful fabrication or resonators is the etching. Different processes were performed before obtaining very well defined devices. We will summarize the evolution and the main encountered problem with these thin motive devices.

Figure 23 shows the results of applying the typical process used in the last section. Structures were correctly released but the main difficulty was in obtaining very well defined thin patterns, as shown in figures 23(a)(b)(c) and (d). The width of the cantilevers is in the range 0.8µm to 2.5µm. Some devices, bridge-based, are successfully fabricated, with spectacular dimensions, 300 or 500 µm long (figure 23(b) or 26(b)), for 1 µm width and in the range 2-5 µm thick. No bending are present indicating that the material is good for mechanical structures. However, the borders of

the structures, fabricated during the first process, are not regulars due to ICP deep etching. At the beginning, it was mainly attributed to the Al mask, defined during the lithography step, and the use of CMOS not-compatible metals as etching mask, such as Ti or Ni, was believed to be a possible solution to obtain a better definition for the thinner devices of this mask. The results of using such an Al mask resulted, after the SiC etching step, in sidewalls not very well defined and was repeatable (figures 24(a)(b) and (c)) for another process but this phenomenon was more marked in some area zones of the sample. Therefore, another run with a back side polishing to reduce possible slight bowing and thus facilitate lithography step was performed. The result is shown in figures 24(d) and 25.

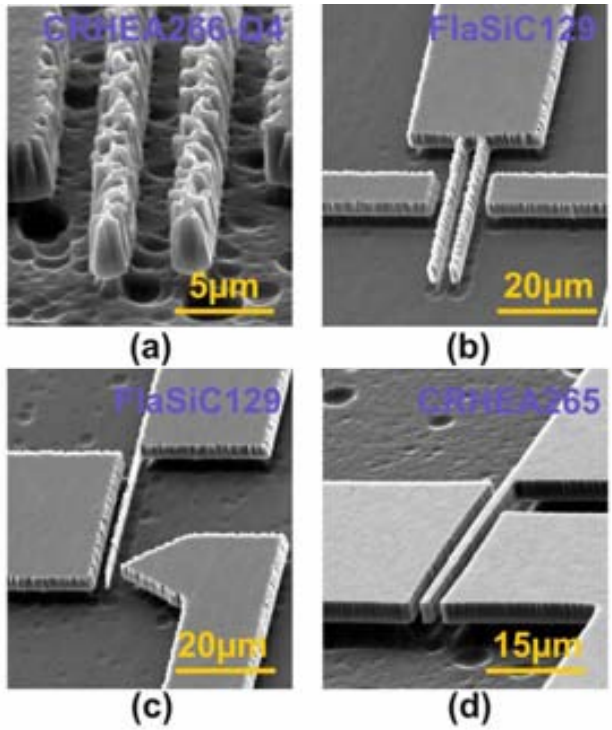


Figure 24. Generations of fabricated vertical resonators: (a) diapason structure from sample CRHEA266-Q_4, (b) diapason structure from sample FlaSiC129, (c) cantilever from sample FlaSiC129 and (d) cantilever from sample CRHEA265.

Polishing the back face, in addition to the front face, associated to a previous reduction of the bowing by an optimized CVD process, allowed to obtain a much higher lithography resolution and successfully obtain well defined devices thinner than 2 µm, as it can be observed in the SEM images of figure 25 for sample CRHEA265 and CRHEA495. Some pits due to some growth defects could remain but do not affect the behaviour of the resonators.

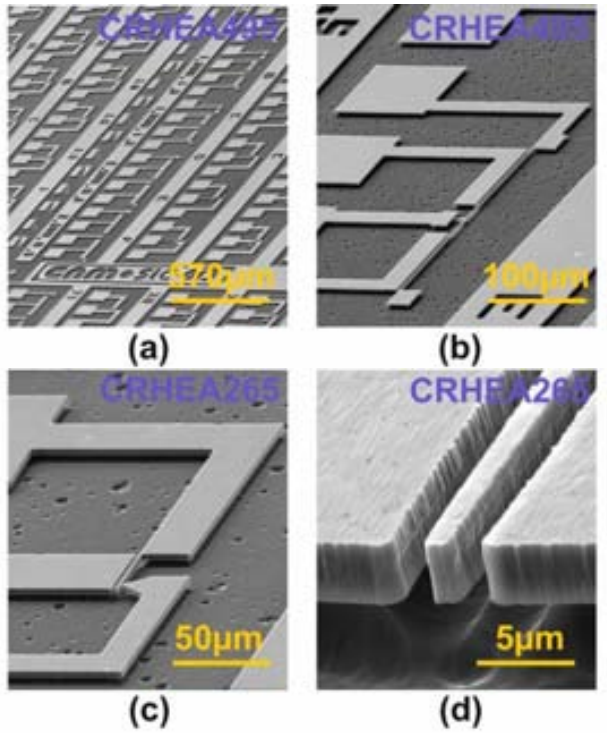


Figure 25. SEM images of electrostatic resonators : (a) general view, (b) bridge 500 µm long and 1 µm width, (c) cantilever 40 µm long and 1 µm width and (d) zoom view.

Contact formation

Then a metallization step was required. For this purpose, typical SiC metal scheme consisting of Ni/Au was used. For electrostatic resonator actuation, one requirement is that the layer has to be n-doped. For biasing, an ohmic contact is preferred but the contact resistivity is not critical. In Si devices biasing is often performed without metallic pads. For 3C-SiC, if the structural layer is not n-type doped during the growth, co-implanted Nitrogen and Phosphorus through an oxide mask could be performed before the resonator fabrication step. Multiple implantation step of Phosphorus, at energies of 25, 45, 83 and 160 keV for a total dose of ~ 3.5×10^{14} cm^{-2} (0.26×10^{14}, 0.36×10^{14}, 0.81×10^{14}, 2.1×10^{14} cm^{-2}) were performed followed by another multiple implantation step of Nitrogen, at energies of 20, 40, 65 and 100 keV for a total dose of ~3.6×10^{14} cm^{-2} (0.47×10^{14}, 0.65×10^{14}, 0.96×10^{14}, 1.5×10^{14} cm^{-2}). This co-implantation scheme was chosen because it successfully brought for 4H and 6H polytype to squared profile and low sheet resistance values [19]. The TRIM (transport-of-ions-in-matter) [20] Monte Carlo simulation predicted a 0.2 µm deep implanted region as shown in figure 26, with a suggested doping peak concentration, at the mean projected range, high enough (~$10^{19}cm^{-3}$) to assure a sufficiently high concentration in the near surface, even with a few activation percentage of dopant species, for ohmic contact formation. However, it has to be noted that TRIM simulation doesn't take into account the crystallinity of the 3C-SiC sample, and thus the possible canalisation effects, by contrast to i2SiC, a software developed at CNM by Erwan Morvan [21]. However, SRIM simulation has been used here only to give us an idea of the implantation depth.

Then, the activation annealing is limited at 1300ºC (Ar, 30 min) since higher temperature used in 4H-SiC (~1600ºC) can not be used here due to the Si substrate.

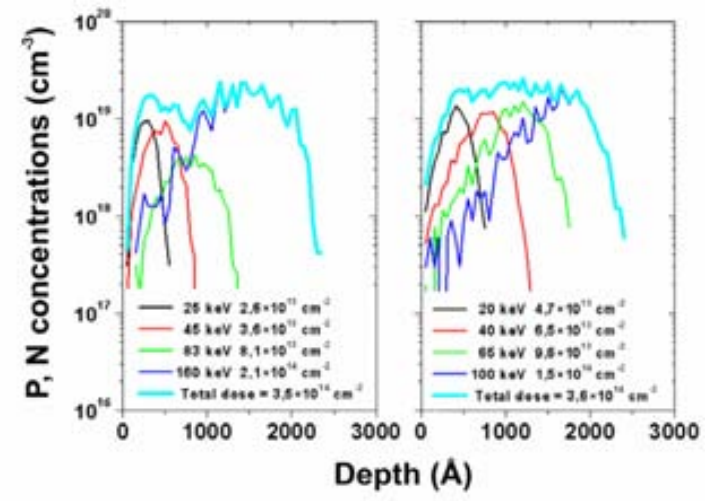


Figure 26. SRIM simulated P^+ and N^+ implantation doping profiles to create the ohmic contacts for MEMS.

Post-implantation anneal is then performed in Ar ambient to activate the implanted dopants. Next, Ni and Au with 100 nm and 50 nm thicknesses were sequentially deposited by sputtering and patterned by lift-off, to form the contact pads pattern. The contacts were then alloyed by RTA (rapid thermal annealing) at 900ºC for 1 min in Ar ambient. TLM structures were specially fabricated in order to evaluate the contact resistivity in 3C-SiC material. Since the wafers were full-area implanted, the lateral isolation was obtained by etching. The gap spacings between the TLM contacts were 5, 10, 20, 40 and 100 µm, respectively. The process was identical to the one used for MEMS. Table IV-8 shows the extracted electrical parameters of the contact formed on a FlaSiC sample and on a N^-/N^+ bulk 4H-SiC sample annealed at 1600ºC for reference. The contact resistivity on the 3C-SiC FlaSiC sample is almost two orders of magnitude higher than for the 4H-SiC. Similarly, the activation rate is one order of magnitude lower. This is due to the lower activation annealing temperature (1300ºC instead of 1600ºC) used for the FLASIC sample.

Table IV-8. Electrical parameters of the contact formed on the 3C FlaSiC sample and 4H-SiC as reference.

Sample	Metal nnealing T (ºC)	Contact resistivity ρ_C ($\Omega.cm^2$)	Doping N_D (cm^{-3})
3C FlaSiC	Before annealing	1×10^{-3}	5×10^{18}
3C FlaSiC	900	9×10^{-4}	2.7×10^{18}
3C FlaSiC	950	9×10^{-4}	1.7×10^{18}
4H-SiC (as ref.)	950	2×10^{-5}	2.1×10^{19}

SEM images of the ohmic contact are shown in figure 27. In some pads, the contacts showed bad adherence but this can be improved.

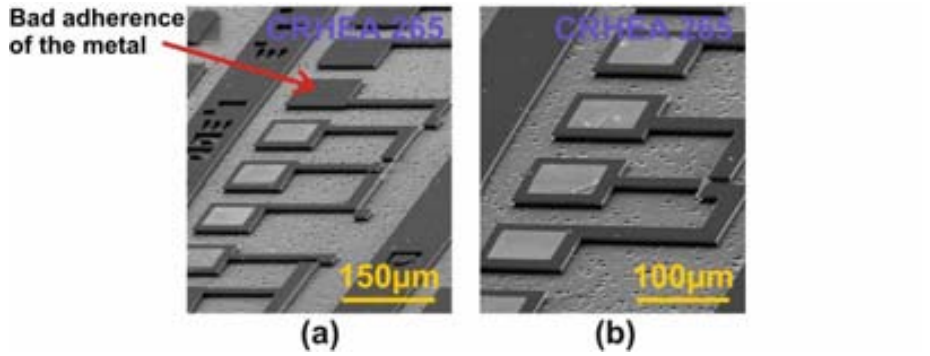


Figure 27. SEM images showing the SiC ohmic contact on top of resonator pads.

4.3.3 Electrical characterization

In order to actuate electrostatically the resonators, a combination of sinusoidal AC voltage and DC voltage have been applied. Thus, we can excite them into lateral vibration, and with an optical microscope coupled to a CCD camera we detect the oscillation amplitude of the cantilever. An illustration of the used set-up for actuation is shown in figure 28.

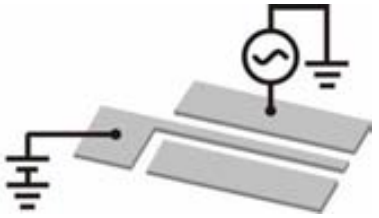


Figure 28. Dynamic excitation: a DC voltage applied to the cantilever and an AC voltage applied to the driver electrode produce cantilever oscillation around the resonance frequency.

In principle, this design allows an all electric actuation/detection. All measurements were performed in ambient atmosphere. The resonance was first optically detected by the cantilever movement through the real time observation around the expected resonance frequency. At the resonance, the cantilever end is blurred. Usually, after some attempts, the resonance is detected: optical images of the cantilever at resonance and out of resonance are shown in figure 30.

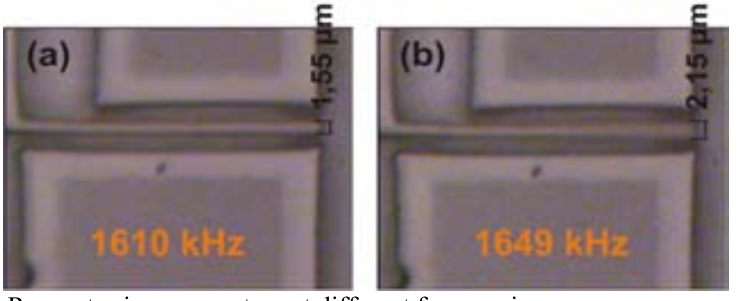


Figure 29. Resonator images capture at different frequencies
(a) 1610 kHz (b) 1649 kHz.

Once the resonance detected, a signal can be expected through the readout electrode. However, it was not possible with our set-up to electrically detect the resonance, the readout current being too low and with elevated noise. The main reason was due to the poor electrical isolation from the substrate, as depicted in the figure 30 showing the current-voltage characteristics through the SiC/Si heterostructure.

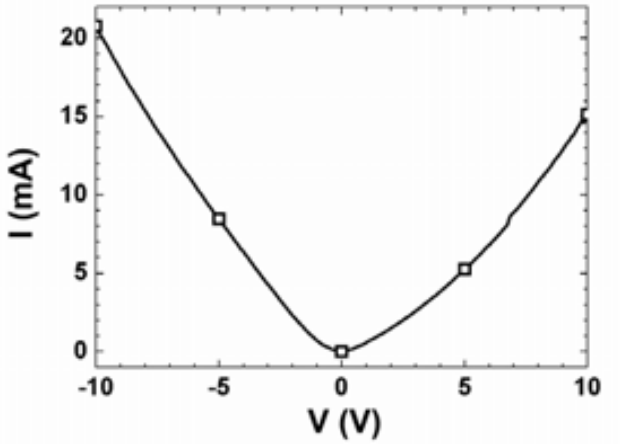


Figure 30. Current-Voltage characteristic of the interface 3C-SiC/Si.

However, it is possible to analyze some characteristics of the resonance without readout electrical signals. One of them consists in performing an analysis on the CCD images, thus becoming possible determining the oscillation amplitude (with an accuracy of 0.5 µm) as a function of frequency. Another one consists on analyzing the photodiode electrical signal based on the reflection of a laser beam on the cantilever, thus giving a current peak at the maximal amplitude. From these two methods, the resonance frequencies were precisely determined.

The vibration amplitudes of a 40 µm long cantilever as a function of frequency are shown in figure 31. In the first case, the resonance frequency was for the first mode 1041.8 kHz, and the quality factor was 133, for an actuation voltage of 90V DC. In the second case, for a wider resonator, the resonance frequency and quality factor were higher, around 1.65 MHz and 148 respectively, for an actuation voltage of 100V DC. Typically the measured resonance frequencies were comprised between 1 and 2.5 MHz for the 40 µm long cantilevers, and quality factors comprised between 100 and 200 for the first resonant mode.

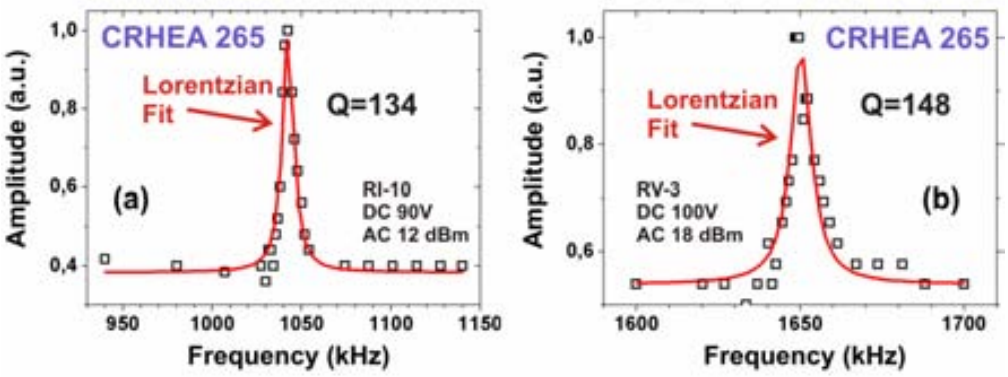


Figure 31. Fundamental resonance peak for (a) a 40 µm long and 1 µm width lateral resonator - mode 1 - f_0 = 1041.8 kHz, Q ~ 134, (b) a 40 µm long and 1.3 µm width lateral resonator - mode 1 - f_0 = 1.65 MHz, Q ~ 148.

Resonances were also observed using the laser detection method for different actuation voltage combinations, as it can be shown on amplitude and phase graphs in figure 32. At high V_{DC}, higher amplitude should be expected, but it was not observed on the reported graphs of figure 32. This could be explained due to the laser beam not perfectly focalized on the cantilever in vibration. Adjusting precisely the beam on the cantilever extremity, the returned amplitude highly increased. The difficulty is mainly due to the laser spot diameter, around 10 µm, which resulted in difficulty on focalizing on thinner devices.

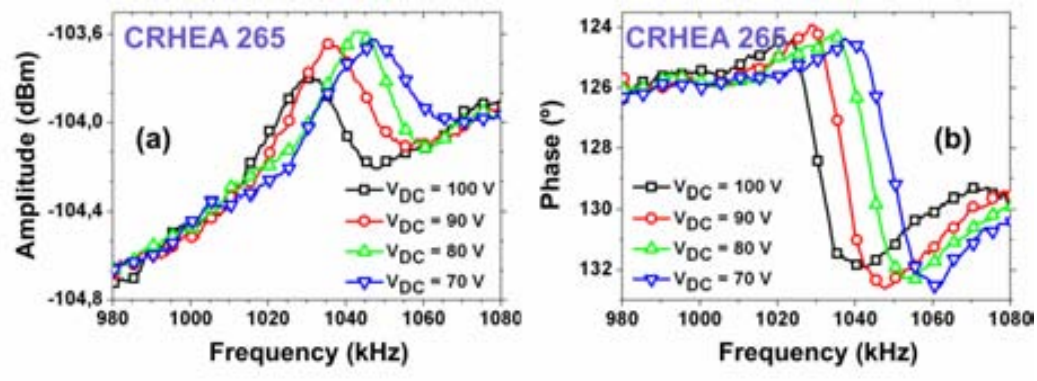


Figure 32. Resonance graphs showing (a) vibration amplitude (b) vibration phase of the free cantilever extremity for several V_{DC} voltages of a 40/1 µm long/width cantilever.

Moreover, the measured amplitude with detection laser method is small and mainly depends on the spot position along the cantilever.

For increasing V_{DC}, it can be effectively verified that the resonance frequencies are lowered. Representing the resonance frequency as a function of V_{DC}^2, we can obtain the natural frequency of the cantilever. The dependence of the resonant frequency with the applied voltages is given by Eq. 4.6 [22]:

$$f_r = f_0 - \frac{2C_0 l^3 f_0}{Ew^3 d^2 e}(V_{DC}^2 + \frac{1}{2}V_{AC}^2) \qquad \text{Eq. 4.6}$$

where E is the Young modulus, f_0 the natural resonance frequency, l the length of the cantilever, w the width, e the thickness, d the gap between the cantilever and the driver, V_{DC} and V_{AC} the applied voltages and C_0 the capacitance:

$$C_0 = \varepsilon_0 . \frac{l.e}{d} \qquad \text{Eq. 4.7}$$

where ε_0 is the vacuum dielectric constant.

Below, in figure 33, we can see the linear variation of the measured resonance frequency values for different V_{DC}/V_{AC} combinations for two of the cantilever structures, R-I-10 (1/40 µm long/width cantilever) and R-II-3 (2/40 µm long/width cantilever), according to the equation Eq. 4.6. In these cases, the extrapolated natural resonance frequencies were 1.065 and 2.5 MHz, approaching the expected resonance frequencies determined by analytical and FEM analysis with Ansys. For example, for the cantilever of the figure 33, a natural resonance frequency of 1065 kHz is evaluated from the resonance frequencies measured for different voltages, close to the 948 kHz predicted by Ansys simulation.
This simulation program was also used to predict pull-in voltages, taking into account the surrounding air effect. In simple terms, the pull-in voltage can be defined as the voltage at which the restoring spring force can no longer balance the attractive electrostatic force [23].

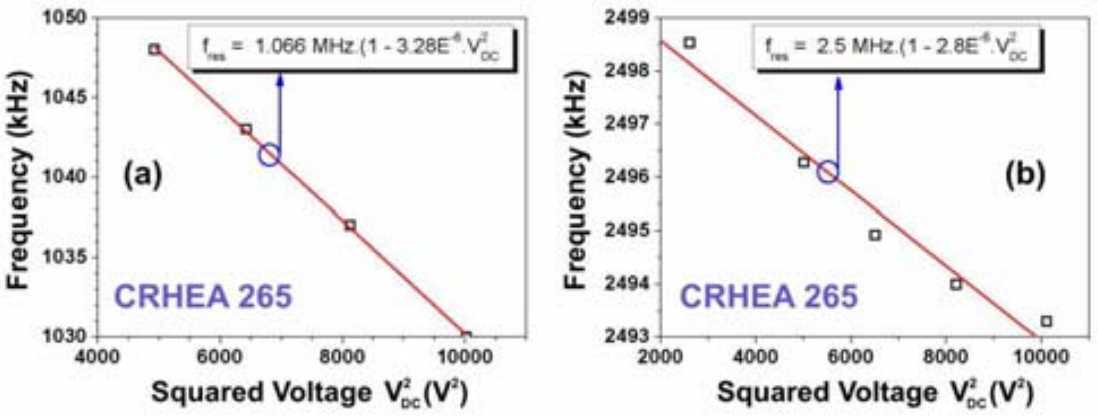


Figure 33. Experimental resonance frequency values as a function of the applied quadratic voltage for (a) R-I-10 (40/1 µm long/width cantilever), (b) R-II-3 structure (40/2.5 µm long/width cantilever).

A mesh of the structural material is shown in figure 34(a). Simulated pull-in voltages were superior to 300 V for most of the structures. For example, for a 40 µm long cantilever, the simulated pull-in voltage was around 300 V, as shown in figure 34(b). This means that DC+AC excitation voltages have not to exceed this value, which is more than three times superior to the one obtained for an equivalent Si device.

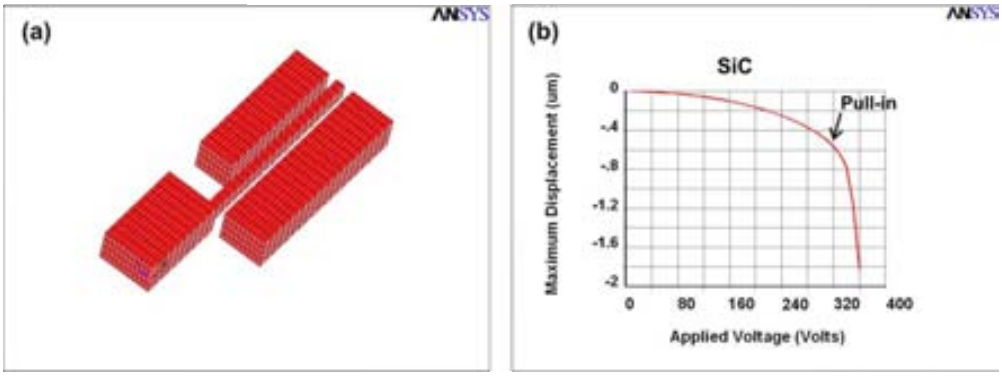


Figure 34. Ansys simulation: (a) Cantilever meshing, (b) Pull-in voltage: a DC voltage is applied to the cantilever (40 µm long, 1.5 wide, 3.3 µm thick).

4.3.4 Other structures

Other structures were measured. In particular, two coupled cantilevers forming a diapason structure, as it can be seen in the figure 35. This kind of structures is interesting and is the base of the comb drive ones. For the structure of the figure 36, with length and width of 40 and 1.5 µm respectively, resonance was expected around 1.81 MHz (for a Young modulus of 450 GPa). Applying different voltage combinations, the resonance was optically observed only for the cantilever closer to the actuation electrode, the vibration of the other cantilever being probably too small to see it. Moreover, such as for the cantilever structures, no electrical current was measured through the readout electrode. For 100 V DC the resonance frequency was 1.85 MHz, and increased to 1.88 MHz for 30 V DC actuation.

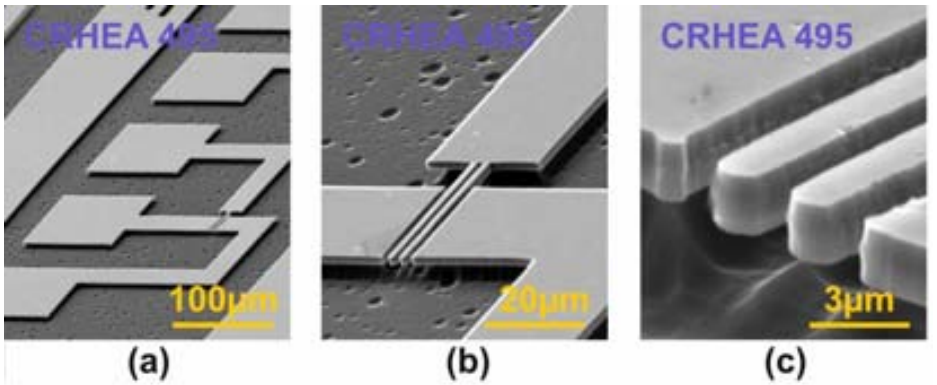


Figure 35. SEM images of a diapason structure, (a) general view of the structure, (b) zoom 1 and (c) zoom 2.

More details can be obtained from figure 36(a) which depicts the characteristic response of the diapason. Increasing the DC voltage, a clear spring-softening effect is verified, and is traduced by a resonance frequency decrease. Figure 38(b) shows the dependence of the resonance frequency with the applied voltage: a fundamental resonance frequency of 1899 kHz is extracted, which is close of the one theoretically expected.

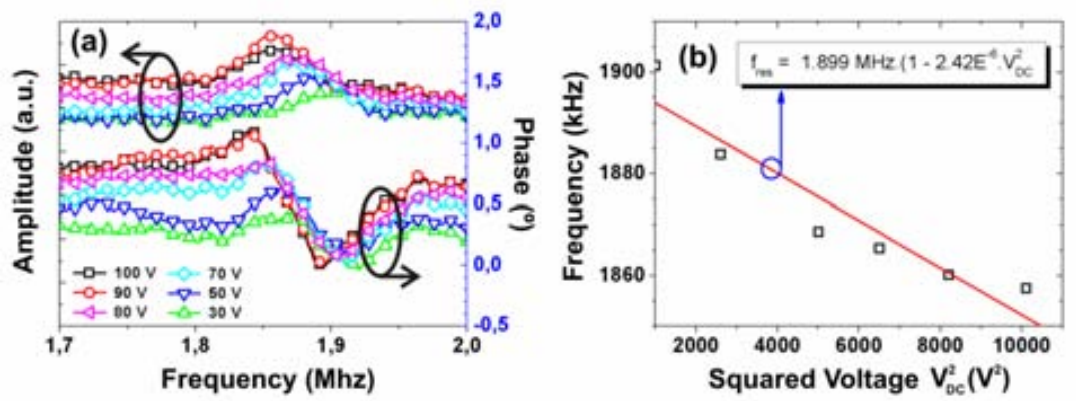


Figure 36. (a) Resonance spectra of diapason in air for several V_{DC} voltages, (b) resonance frequency dependence with V_{DC} of the diapason.

Bridge structures were also fabricated, many of them doing 300 or 500 µm long for 1 µm wide, as it can be seen in figure 37. It is worth to note that they mechanically resist and bridges were successfully released, revealing once more the importance of fabricating MEMS with SiC.

The bridge of figure 37(b) has a length/width of 500/1 µm respectively and is expected to resonate around 46 kHz without taking into account any stress. Resonance was observed but at a frequency around 234 kHz. This is easily explained considering the tensile stress of the cantilever, thus increasing the expected resonance frequency, as seen for the vertical bridges. As previously, no capacitive signal was detected.

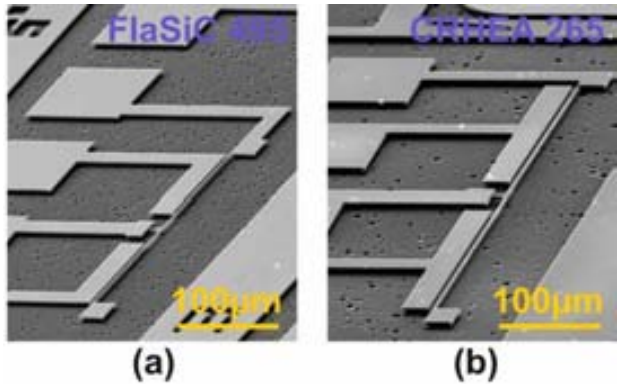


Figure 37. SEM images of electrostatic bridges 1 µm width, (a) 300 µm, (b) 500 µm long.

The spectra were recorded for different voltages combination (figure 38(a)), thus allowing to extract the fundamental resonance frequency of the bridge, 243 kHz. As a consequence, a tensile residual stress around 155 MPa is evaluated.

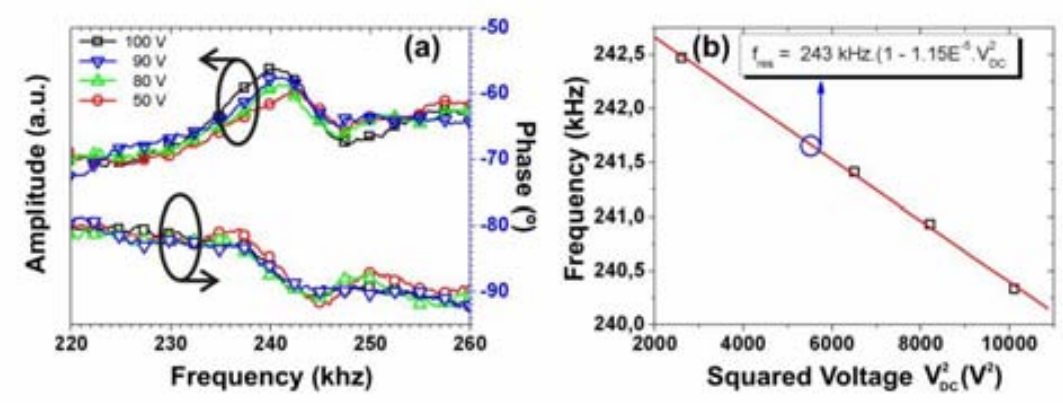


Figure 38. (a) Resonance spectra of bridges in air for several V_{DC} voltages, (b) resonance frequency dependence with V_{DC} of the bridge.

4.3.5 Summary

Using a novel surface micromachining process, with back side polishing, we have obtained suspended devices with thicknesses higher than 1 µm and with vertical sidewalls clearly defined. Thin devices, with width ranging from 0.8 µm to 2.5 µm were successfully fabricated, and some of them with length up to 500 µm. The single crystalline SiC grown on large-area Si used in this work has revealed its outstanding mechanical properties, with low stress, and has demonstrated that it is an appropriated material to realize SiC-based MEMS on a common low-cost platform, using the well controlled Si bulk micromachining techniques. Moreover, the resonator lateral design allows to avoid possible non-uniformity of the resulting SiC layers (due to mismatch with substrate) and thus the possible non uniformity in resonance frequencies of vertical resonators.

Moreover, the experimental results presented here also clearly showed that that higher resonance frequency (by 40 %) and higher quality factor (more than 100%) are achieved with this material, compared to an equivalent Si device. This is particularly interesting for high sensing applications such as mass sensors.

Ohmic contacts were also studied since the electrostatic actuation required the cantilever and electrodes biasing. The reasonable values obtained for contact resistivity was enough for electrostatic actuation. In this sense, the cantilever, constituting the movable plate of microcapacitors, was correctly actuated, revealing that this concept works quite well. However, due to the poor electrical isolation of the SiC layer from the Si bulk and to air-ambient measurements (which results in losses through the bulk and a low quality factor, respectively), it was not possible to detect an electrostatic displacement current. Therefore, resonance frequency detection was only optically performed, through observation of CCD images or using a laser-based set-up.

It appears clear that an all electrical actuation/detection is required and this is possible only considering other substrates or other materials.

Thus, to overcome this problem, next studies will concern the possible use of SiC on Insulator as starting substrate for resonator fabrication, SiCOI (like the SOI material for Silicon), SiC on semi-Insulated Silicon (SIS) and SiC on SOI. These materials are expected to allow electrical signal measurements through the read-out electrode, and thus also beneficial for other electrostatic devices such as micromotors or

comb drive resonators. Other materials, such as III-nitrides, will be also considered in the next chapter. Moreover, means of reducing the gap between electrodes and cantilever will be also discussed, as a possible way of disminishing the high voltages required for actuation. The possibility of performing smaller devices, with thinner patterns, at nanometric scale, will be also studied with e-beam lithography (300 nm expected), since our stepper lithography is limited to 0.5 µm width.

Based on the obtained results in the last section, our work has been first focalized in isolating the SiC layers from the substrate, and then to study possible solutions of reducing the gap between electrodes and resonator.

4.4 SiC/SOI and SiC/SIS electrostatic resonators

In Si technology, Si-On-Insulator (SOI) wafers are the most used substrates. In this case, the buried oxide layer is used as the sacrificial film, and suspended Si structures are easily released in HF-based solution. Fabricating such SiC devices is much more challenging due to the lack of high quality reliable and commercial insulated wafers analogue to the SOI one [24, 25].We have used recent advances [26] in the growth of 3C-SiC on Si to overcome these problems. Growth parameters and methods were optimized in order to obtain a good quality crystalline layer. High quality SiC layers on Semi-Insulating crystalline Si (SiC/SIS) and on SOI substrate (SiC/SOI) have been grown. The feasibility of single crystalline SiC resonators insulated from the substrate and electrically driven is then here demonstrated. Results of electrical characterization for the fabricated SiC electrostatic resonators are also reported revealing the potential of this material for harsh environment electrostatic MEMS.

4.4.1 Materials growth

Several methods of achieving SiC on insulating substrates have been reported, growing directly on an insulator, such as amorphous Si_3N_4 or SiO_2 and also on insulating substrates such as crystalline sapphire, high temperature glass or quartz. The former approach was using polycrystalline SiC since it can be directly deposited on dielectric layers such as SiO_2 [27-31]. However, the poor crystalline quality obtained (which resulted in poor electrical characteristics) motivated the search of single SiC-on-insulator (SiCOI) solutions. To some extend, polycrystalline quality was enough for proper functionality [32], but with the vision of possible circuitry or transistor integration it is interesting the use of single crystal SiC. Moreover, it was reported that single crystal SiC improves the quality factor (lowering internal stress), thus reducing internal losses [33]. Single SiCOI resonators, based either on wafer bonding [34] or/and etch-back techniques [35], were also reported. State of the art is summarized in Table IV-9. It is interesting to note that all the reported lateral SiC resonators were based on comb drives structures for operation in vacuum ambient. A single cantilever allows achieving higher sensitivity due to its lower mass.

Table IV-9. Main results of SiC electrostatic resonators on insulating substrate from literature.

Materials	Structure*		*L*×*w*×*t* (µm)	*f* (MHz)	*E* (GPa)	*σ* (Mpa)	Ref.
polySiC on $Si_3N_4/SiO_2/Si$	B	V	(51-110)×0.9×0.7	1.5-4	385-512	73-171	[28]
polySiC on SiO_2/Si	CB	L	1 µm thick	0.02-0.07	710	472	[29]
polySiC on polySi/SiO_2/Si	CB	L	2 µm thick	0.01-0.028	250-427	NR^+	[30]
NiCr/polySiC on polySi/SiO_2/Si	BI	V	(25-200)×15× 2	0.066-1.729	NR^+	NR^+	[31]
Single SiCOI	CB	L	2 µm thick	~0.042	359	NR^+	[35]
Single SiC on SOI	C	L	40×(1-2.5)×3	1.2-2.9	650	150	This work

*B: Bridge, CB: Comb drive, C: cantilever, BI: Bi-layer cantilever, V and L: vertical and lateral displacement respectively ($^+$NR: not reported).

Two inches (100)-oriented SIS and thin (100)-oriented SOI wafer supplied by SOITEC have been used for 3C-SiC films deposition. For both starting materials, a heteroepitaxial growth of 3C-SiC layers was carried out using an horizontal, low pressure, resistively heated, hot wall CVD system, with a reactor chamber ready to accept the 4-inches wafers by NovaSiC/CRHEA [36]. The SiC/SOI samples used had a size of ~ 20 × 20 mm^2 and the thicknesses of the Si-overlayer (SOL) and the buried thermal oxide layer (BOX) were 200 and 1000 nm, respectively. The deposited 3C-SiC films for SOI were 3 µm thick with a non-intentionally doped (NID) layer (0.5 µm thick) followed by an n-type layer (2.5 µm thick) with a nitrogen doping concentration of ~1×10^{19} cm^{-3}. The main problem of applying the usual 3C-SiC growth process to an SOI substrate with very thin silicon over layer was the degradation of buried oxide at high temperature resulting in the apparition of large cavities in the BOX (figure 39).

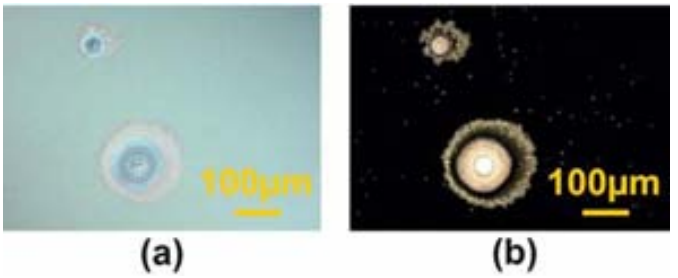


Figure 39. Bright field image (a) of typical defects created in SOL / BOX structure during the ~80min growth of 3.3µm thick 3C-SiC film. Image size is 500x670 µm². The white points on the dark image (b) are the voids created during the carbonization step at 3C-SiC/Si interface.

The created defects come in part from the poor thermal stability of the buried SiO_2 layer at 3C-SiC elaboration conditions, and their density and size were increasing with the growth duration and growth temperature. The first attempt resulted in an important deterioration of the BOX, with high defects density. The growth rate was then 2.4 µm/h. To moderate this undesirable effect, a first remedy consisted in reducing the growth duration by limiting the film thickness of the doped-layer to 0.5 µm. A second solution consisted in increasing the growth rate to 4.1 µm/h. Finally, based on this second solution, the C/Si ratio was adjusted in another sample. Defects density was sufficiently reduced in the most part of the samples area, with respect to the initial one. For SiC/SIS, the deposited 3C-SiC films were 1 µm thick.

The 3C-SiC growth process was performed in two classical steps [37]. During carbonization, propane (C_3H_8) and hydrogen (H_2) flows were opened and ramped up to 1050 ºC. The growth was done at 1350 ºC. The thickness of the deposited layers were determined from Fourier Transform Infra-red Reflectance (FTIR) spectra (not shown) on the 3C-SiC/Si film and by Scanning Electron Microscopy (SEM), as shown in figure 40. The samples were finally Chem-Mechanically Polished (CMP) in order to obtain smoother surfaces.

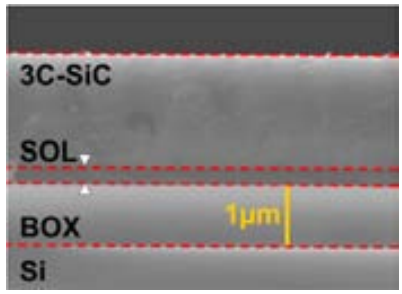


Figure 40. SEM cross-section image of the 3C-SiC grown on SOI substrate.

After polishing, the samples were studied by atomic force microscopy (AFM) and by SEM in order to determine the roughness and the surface morphology. The results demonstrate that the layers grown on SOI substrates are comparable to the layers grown on Si wafers i.e. smooth and free of defects surfaces, with root-mean-square (rms) roughness about 1 nm for 2x2 µm² images. High Resolution X-Ray Diffraction (HRXRD) ω-scan rocking curve of the (002) peak was performed on the full wafer growth (figure 41). The full width at half maximum (FWHM) of the peak is around 0.29 and 0.30º for SOI and Si substrate respectively, at 0 and 90º, showing that the epilayers are of similar high crystalline quality.

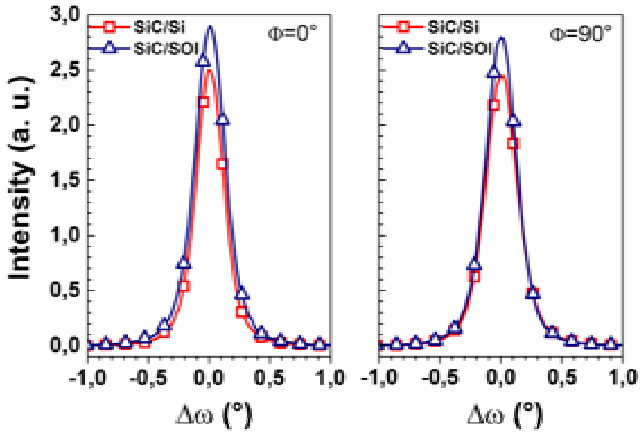


Figure 41. XRD Rocking curve of the (002) peak showing the good crystallinity of the SiC layer grown on SOI substrate, left: at 0º, right: at 90º.

4.4.2 Fabrication

The fabrication process was similar to the one established for SiC/Si electrostatic resonators in the last section. For SiC/SIS, the process is almost identical to the one described in last section. For SiC/SOI, the main difference resides that during the SiC etching, it is possible either to etch up to the BOX, and then using this BOX as sacrificial layer, with the risk of obtaining SiC/Si bi-layers resonators, either to etch up to the Si substrate and to use it as sacrificial layer.
After double side polishing, the fabrication process consisted in patterning the SiC layer through an Al mask layer using a SF_6/O_2 plasma in an ICP equipment. As it has been seen in the previous section, probably most part of the SiC microstructures were already released only with the dry etching. Controlling precisely only the SiC etching is difficult since the SiC thickness in these small samples is not uniform, and it could be much more appropriate etching up to the Si. Finally, the Al mask is stripped and the devices are released by HF-based solution etching isotropically the Si substrate.
Various microstructures were fabricated on monocrystalline 3C-SiC layers grown on SIS and SOI substrates, most of them consisting of lateral cantilevers with different aspect ratio (figure 42).

Again, our study was focused on electrostatically driven and capacitively read-out two port structure with in plane resonance. Therefore the resonator possesses two electrodes, as displayed in figure 42. The input signal is applied to the excitation electrode, the resonator being connected to a dc voltage, and the motional current generated by the resonator movement is sensed through the read-out electrode. This configuration allows a reduction of the parasitic feedthrough current when compared to a one-port structure, whereas the use of lateral vibration modes makes the resonance frequency of the structure independent of material thickness, which would be not entirely uniform on SiC/SOI samples.

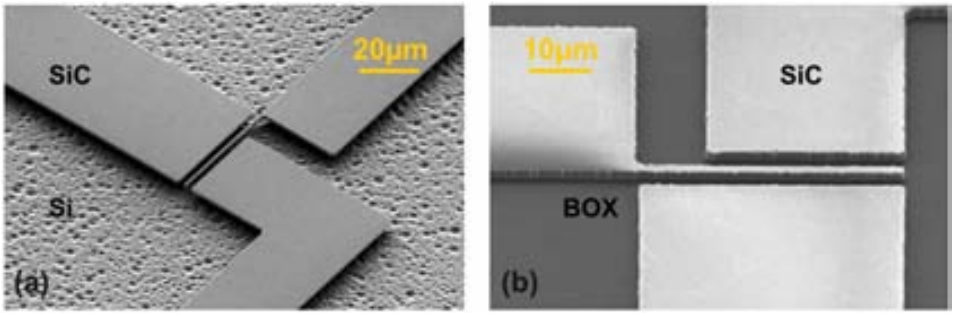
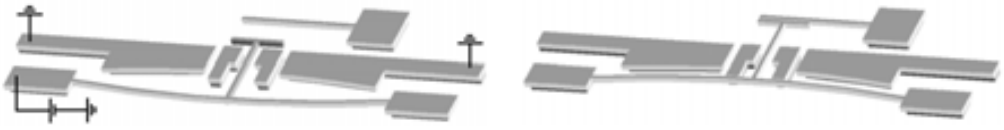


Figure 42. SEM image of (a) SiC/SIS and (b) SiC/SOI electrostatic cantilever 40 µm long, 1 µm width.

However these lateral electrostatic devices suffer from a limitation imposed by the optical lithography used in this work, which restricts the gap obtained between the resonator and electrodes. This results in rather high voltages to actuate them. In addition, these high gaps induce high motional impedance. The motional impedance value plays a role in the input-output impedance adaptation and determines the insertion loss and the output signal level. This impedance should be as low as possible. Most of the used methods for reducing the gap consisted in the use of new technological processes such as e-beam lithography, or by the use of solid gap dielectric, complicating

seriously the process, the remove of subproducts and often resulting in stiction problems, and were only feasible for small dimensions resonator. Moreover these approaches require complex and expensive technologies, hardly compatible with industrial environment. The concept presented here appears as realizable with most lithography process, since electrode and resonators are fabricated in the same structural layer. Moreover it is especially recommended for WBG MEMS realization where complicated processes such as e-beam lithography are difficult to implement. An innovative approach to reduce the gap value of (thick) structural layer limited by optical lithography methods is presented by the use of transducer bistable electrodes. This is achieved by employing motor electrodes that allow the transducer electrodes to position at its second stable position. A bistable mechanism consists in a device that tends to remain in one of two stable equilibre positions. These mechanisms have been used in numerous applications including switches, relays, sensors, etc, but never to effectively reduce the gap post fabrication.

To reduce effectively the electrode-to-resonator gap, we propose to use an electrostatic motor that moves the transducer electrodes close to the resonator. In figure 43, a schematic representation of one of the transducer electrodes with motor is shown. The as fabricated device is shown in figure 43(a). The transducer electrode is fixed to a bistable beam. The motor electrodes are placed laterally and when biased regarding the transducer electrode, a mechanical force acts on the bistable structure. If the force is high enough, and the bistable structure properly designed, it snaps from one stable position to another, as shown in figure 43(b). The geometry of the device is designed in such a way that this displacement approaches the signal electrode to the resonator, and so the signal electrode-to-resonator gap reduces. Moreover, to avoid mechanical and electrical contact due to a possible too elevated mechanical force, stoppers are put near the final position of the bistable beam. The final electrode-to-resonator gap is defined by the difference between the initial electrode-to-resonator gap and the distance between the two stable positions at the beam center: $d_{final} = d_{initial} - d_{stable}$.



(a) **(b)**

Figure 43. Concept of the bistable mobile electrodes
(a) the bistable mobile electrode in its first stable position, after fabrication,
(b) the bistable mobile electrode in its second stable position, after applying a DC voltage.

Particular attention has to be dedicated to the design of the curved beam since bistability is not guaranteed and depends of various design parameters, the type of arch, material properties (residual stress) and type of loads (step, punctual, uniform).

This kind of bistable design for electrodes is particularly relevant since it allows reducing the gap after the fabrication of the devices in standard equipements.

In this sense, another mask, CNM-SiC023 was designed with different structures, most of them based on the cantilever-based structures of the mask CNM-SiC013. Many of them included different electrode designs (figure 44) to reduce the gap post fabrication but will be not detailed here. Many structures were damaged, and many stoppers entirely released.

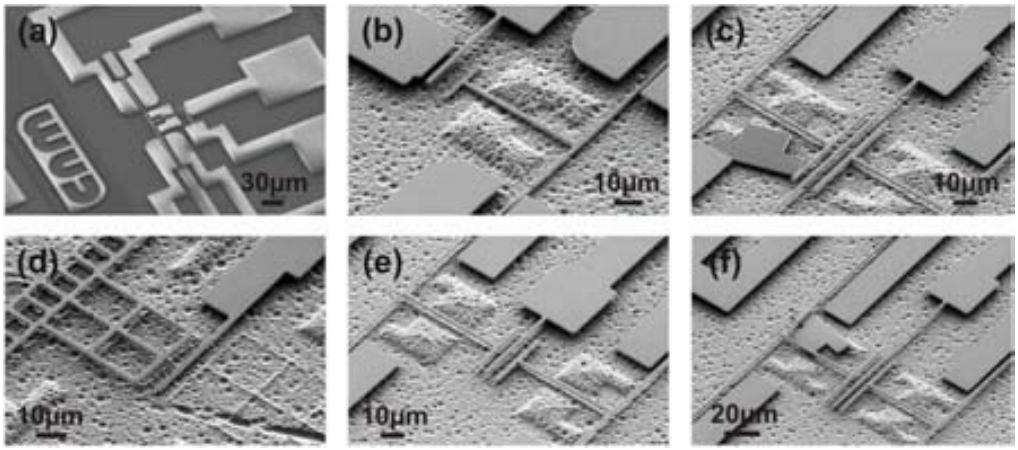


Figure 44. SEM images of some structures of the mask CNM-SiC023. (a) cantilever with bistable electrodes (b) zoom of figure(a) (c) bridge with mobile electrodes (d) cantilever with spring electrode, (e) and (f) cantilever with mobile electrodes.

4.4.3 Material characterization

Raman spectroscopy

Micro-Raman measurements were performed to evaluate the axial stress. The spectra were recorded in backscattering geometry with a Jobin-Yvon T-64000 Raman spectrometer attached to an Olympus microscope and equipped with a liquid-nitrogen-cooled CCD detector. The experiments were performed at room temperature using the 5145 Å line of Ar-ion laser as the excitation source, along the growth c-axis in z(yy)-z orientation, i.e., light incident in the z direction, polarized in the y direction, Raman light measured in z direction, polarised in the y direction. The focused laser spot on the sample was about 1 µm in diameter and the excitation power was around 0.17 mW to avoid the heating on measured structures. The residual stress is thus determined from the Transversal Optical (TO) phonon frequency shift, by the following relation [38]:

$$\Delta\omega_{TO}\,(cm^{-1}) = k\sigma\,(GPa) \qquad \text{Eq. 4.7}$$

Where $\Delta\omega_{TO}$ is the shift in the phonon energy, with respect to bulk unstrained phonon peak at 795.9 cm^{-1} (zero stress energy) and k = 2.5 the Raman stress factor determined by the Young's modulus, the Poisson's ratio (ν=0.25) and the strain coefficient [38].

The Raman spectra recorded on bridges for the SiC/SIS and SiC/SOI are reported in figure 45. Measurements were performed at anchored position, and at released position. From the spectra, the redshifted phonon peak clearly showed the presence of a tensile stress component in the SiC layers, as expected due to thermal expansion and lattice mismatch. For SiC/SiS, the T.O. phonon energy peak appears at 794.8 cm^{-1} at anchored position and at 795.1 cm^{-1} at released position. This indicates first that the stress between the two materials is about 390 MPa, and when released, the structure still possesses a component of tensile stress around 300 MPa. For SiC/SOI, the T.O. mode appears at 794.4 cm^{-1} at anchored position and at 795.5 cm^{-1} at released position, corresponding to biaxial stress level around 590 MPa before release and 150

MPa after release. The lower value obtained from SOI substrate after structure release is in good agreements with the fact that the SOI structure helps to relax the strain from the SiC epitaxial films [24]. However, before release, the SOI substrate does not seem to act as stress relaxation.

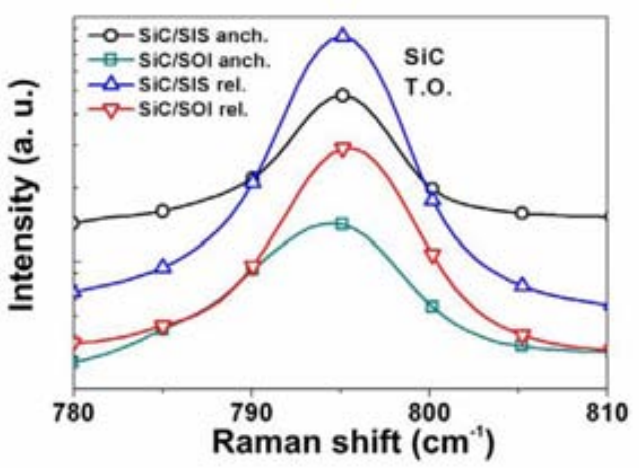


Figure 45. Raman spectra of the SiC obtained from SiC/SOI and SiC/SIS at anchored and released position.

EDX analysis

Since the samples were polished after the SiC growth, the resulting SiC was not uniform, and in some areas, the SiC was etched up to the oxide, and in other areas, up to Si subtrate. This can be seen in the optical images of figure 46: in (a), (b) and (c) the oxide layer is clearly distinguished while in (d), (e) and (f) the BOX was entirely etched probably during the dry etching. In 46(a), some typical defects above described and obtained in SiC/SOI can also be observed.

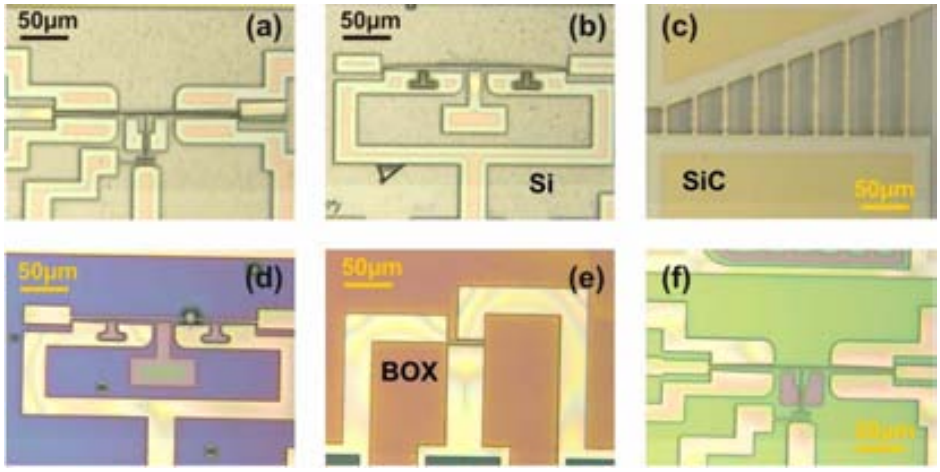


Figure 46. Optical images of some SiC/SOI structures etched up to:
(a), (b), (c) the oxide (BOX)
(d), (e), (f) the Si substrate

What is important here, is that in both cases, either SOL or Si substrate, depending of the etching depth during the SiC etching, is exposed during the Si etching in TMAH solutions, thus allowing a correct releasing of the SiC structures. However, in the case of etching up to the substrate, it has often been observed double suspended structures, the up ones being SiC and the down ones being SiO_2 (BOX) structures, as it can be observed in the SEM images of figure 47. In many devices, the BOX structure, probably due to its high stress level, presents a high curvature that often induces the buckling of the SiC structure, and sometimes its breakdown.

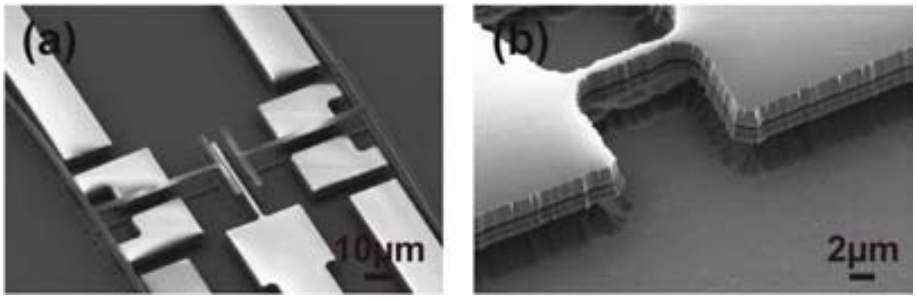


Figure 47. SEM images showing the double suspended layer. In (a) the top SiC layer electrodes have been broken by the stressed BOX layer. In (b) the two layers, SiC and BOX, are clearly visibles.

EDX analysis was also performed on the sample surface of the SiC/SOI sample after the microstructures fabrication to detect exactly in some devices the composition. As expected, Si, O and C were detected in the surface (figure 48(a)). Figure 48(b) displays the SEM micrograph and X-ray maps obtained for Si, O and C. The different X-ray maps revealed an important quantity of O (light areas) around the cantilevers (the zone in dark in SEM micrograph). Si and C were mainly detected at the cantilevers. This clearly indicate that the SiC was only etched up to the oxide, as in the case of figures 46(a)(b)(c).

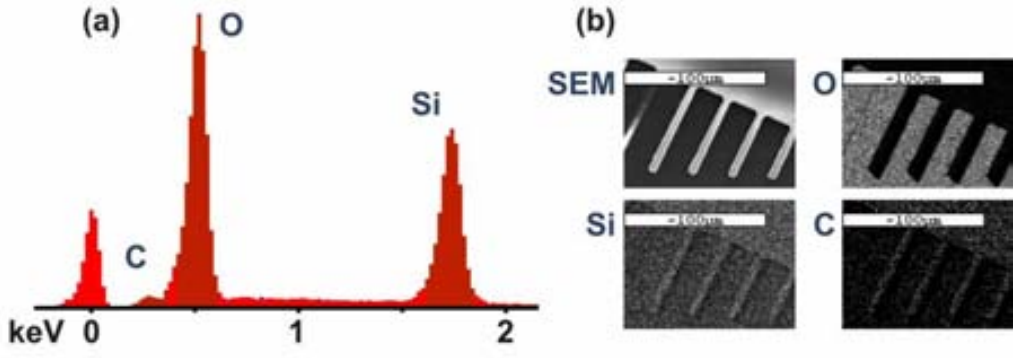


Figure 48. (a) Standard EDX spectrum, (b) SEM micrograph and distribution of O, Si and C.

4.4.4 Electrical characterization

Electrical characterization of the fabricated devices has been performed in air using an S_{21} measurement by means of a network analyzer (Agilent 5100) for the SiC/SOI and SiC/SiS samples. More details on the measurement set-up can be found in *Annex A2*. The experimental resonance was first optically detected by a camera focusing on the cantilever during the frequency swept, as it can be seen in figures 49 and 50 for SiC/SIS and SiC/SOI resonators respectively. Relatively low voltages of few tens of volts were required to actuate electrostatically the cantilever, for both materials, demonstrating that our device concept is suitable as electrostatic SiC MEMS. For example, for a 40/1.5 µm long/width SiC cantilever on SIS, a DC voltage of 30 V and an AC voltage lower than 10V were enough to detect optically the resonant condition.

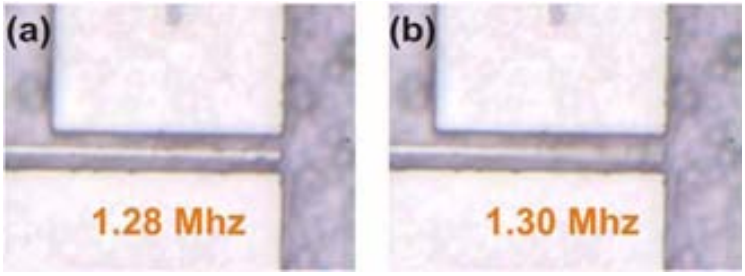


Figure 49. SiC/SIS resonators images capture at different frequencies
(a) 1.28 MHz (b) 1.30 MHz.

Moreover, it was possible to obtain an electrical signal through the read-out electrode, in air ambient, but only for the SiC/SOI sample. Figure 51(a) shows the resonator frequency response (magnitude and phase) for different biasing voltages and an applied input power of 18 dBm for a resonator 40 µm long and 1.5 µm width. Clear resonance and anti-resonance magnitude peaks are obtained without using any amplification circuitry.

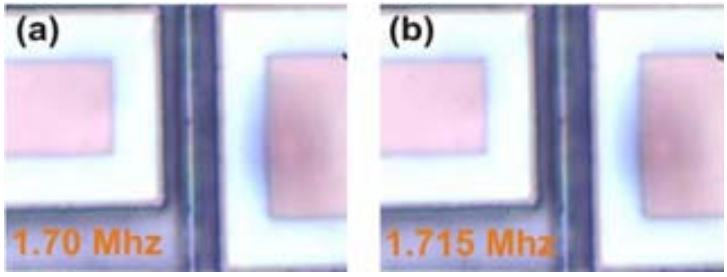


Figure 50. SiC/SOI resonators images capture at different frequencies
(a) 1.70 MHz (b) 1.715 MHz.

The variation of the resonance frequency with the applied DC voltage was analyzed and shown in figure 51(b). The bias linear dependence with frequency allows extracting the natural resonance frequency of the cantilever and the frequency tuning, 1.93 MHz and 1.51 ppm/V^2 in this case. The extracted Young's modulus, around 520 GPa, allows achieving 2/3 higher resonance frequency than an equivalent Si device.

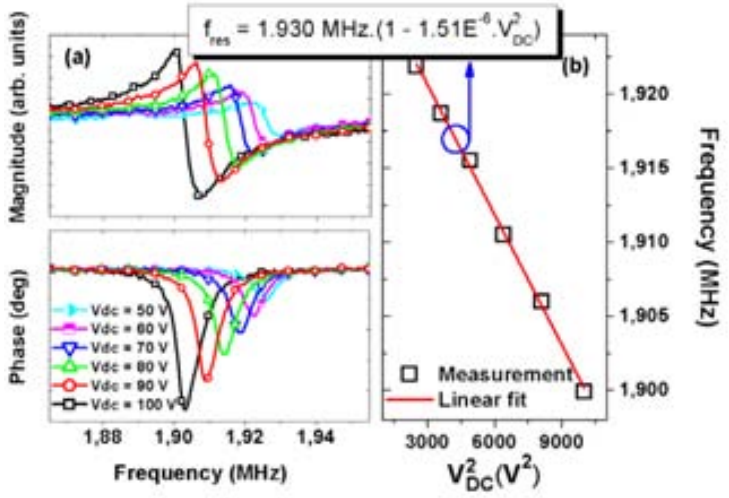


Figure 51. Capacitive electrical response for a 40 µm long and 1.5 µm wide SiC on SOI resonator measured in air for different applied DC voltages. (a) Magnitude and phase. (b) Resonance frequency vs. V_{DC}^2.

For the SiC/SIS sample, the Young's modulus has been evaluated to be around 410 GPa from resonance frequency optical measurements.
Due to its insulating properties, the devices from the SiC/SOI sample are electrically driven and sensed, exhibiting negligible substrate losses and a reduced actuation voltage, compared to those required in the previous section. The obtained results clearly favour the SiC/SOI material compared to the SiC/SIS one for SiC electrostatic MEMS able to operate in harsh environment.

4.4.5 Temperature measurements

Temperature measurements of the electrical response were then performed to verify the stability of the resonance of the SiC cantilever. Figure 52 shows the obtained response as a function of the temperature for an applied DC voltage of 90 V. The magnitude and phase signals (figure 52(a)) are slightly degraded when increasing temperature, especially above 150 ºC. The resonance frequency drops from 1.7189 MHz at 25 ºC to 1.7135 MHz at 200 ºC (figure 52(b)). In this range, the variation is linear and gives a temperature sensitivity of -30.5 Hz/ºC (-17.9 ppm/ºC). The resonance frequency depends of the Young's modulus, which is known to vary with temperature [30]. However the temperature coefficient was positive for vertical resonators (cf. p. 75). We are currently investigating the origin of this difference.

Moreover, the linear coefficient of thermal expansion is also expected to induce different stresses with increasing temperature, especially if the device is constituted from different layers.

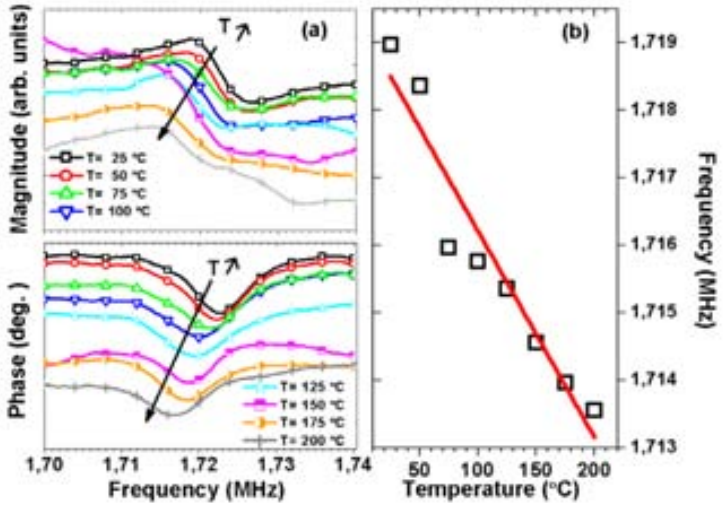


Figure 52. Temperature dependence of the capacitive electrical response for a 40 µm long and 1.3 µm wide SiC on SOI resonator measured in air for an applied DC voltage of 90V. (a) Magnitude and phase. (b) Resonance frequency vs. temperature.

To compare SiC with Si material, similar electrostatic devices resonating at similar frequencies were investigated, first at ambient temperature and then increasing up to 200 ºC. The figure 53 shows the obtained electrical response as a function of the applied DC voltage for a Si (SOI) and SiC (SiCSOI) resonator. The Si resonator was 2 µm wide while the SiC one was 1.3 µm wide. Their responses are similar, the SiC device being slightly less sensible to the applied DC voltage (0.88 ppm/V^2 for the SiC while it is 1.12 ppm/V^2 for the Si). These electrostatic resonators were also measured as a function of temperature, the magnitude and phase being reported in the figure 54, for an applied DC voltage of 90 V.

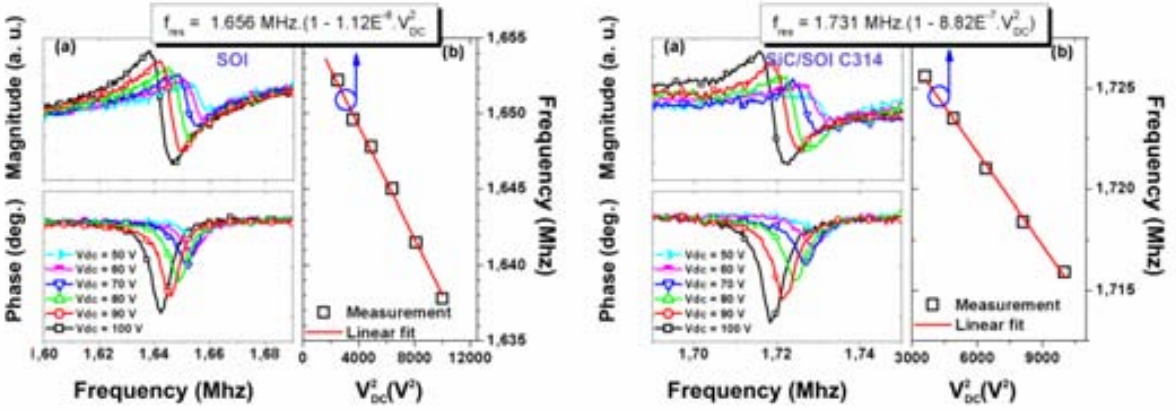


Figure 53. Capacitive electrical response for Si (left) and SiC (right) devices resonating at similar frequency. The Si resonator 2 µm wide and the SiC 1.3 µm wide. Their length is 40 µm. (a) Magnitude and phase. (b) Resonance frequency vs. V_{DC}^2.

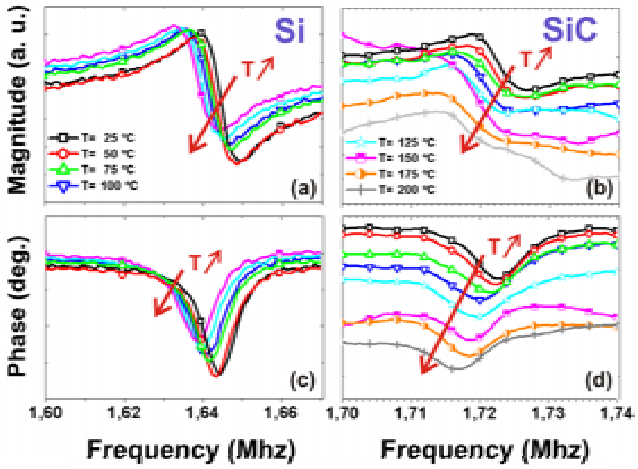


Figure 54. Temperature dependence of the capacitive electrical response for a Si and SiC resonator measured in air for an applied DC voltage of 90V. (a) Magnitude and (c) phase for the Si device, (b) Magnitude and (d) phase for the SiC device.

In both cases, the signal was degraded with temperature, the magnitude and phase being reduced increasing temperature. The figure 55 shows the normalized resonance frequency shift with temperature for the SiC and Si. The temperature sensitivity for the Si device is -60 Hz/ºC giving a temperature coefficient of -33.5 ppm/ºC, which is about twice higher than the values obtained for a SiC device.

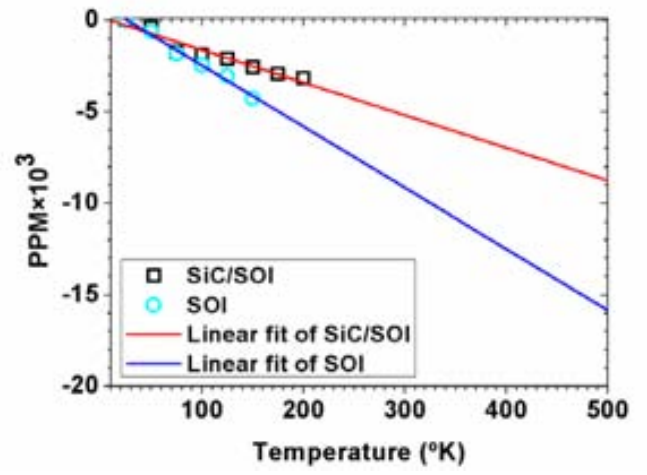


Figure 55. Temperature coefficient for SiC and Si.

4.4.6 Summary

In conclusion, we have optimized the 3C-SiC monocrystalline growth process on SOI and SIS substrates. The samples were polished in order to obtain SiC smooth surfaces of around 1 nm rms. Freestanding electrostatic SiC microstructures were then fabricated and electrically tested. The results obtained showed that isolation of the bulk is critical to avoid leakage current and in reducing considerably the required voltage to

actuate them. Using this new material scheme, it becomes possible to obtain an electrical signal from a system based on a capacitive structure. Thus it becomes possible to imagine identical SiC devices than the Si ones portable developed at CNM with (CMOS) integrated circuitry. Either SiC or Si circuitry could be integrated in these materials. SiC circuitry has been recently demonstrated with 3C-SiC JFET and 3C-SiC MOSFETs are regained high interest and are currently under investigations. A possible route for the achievement of electrically driven portable MEMS operating in harsh environment, such as temperatures over 200ºC, is here demonstrated.

4.5 Conclusions

In a fist part, we have verified the feasibility of 3C-SiC membranes. To attain this objective, using 3C-SiC on Si as starting material, it was required to develop and optimize an etching process for the Si bulk substrate. Different problems were encountered, i.e. the high level of stress near the SiC/Si interface impeding the Si etching, the problem of the (111) orientation etc. Optimizing both the starting material and our etching process, squared membranes up to 4 mm side were successfully fabricated, opening the door to the world of sensors able to operate in harsh environment.

Then vertical SiC test structures fabrication was investigated. It was required to optimize both the starting material and the SiC etching technology to successfully pattern the SiC devices. Different improvements in the growth of the SiC layer were performed with the emphasis of SiC MEMS fabrication. Large cantilever and bridges-based structures allowed extracting the mechanical properties of the SiC layer, which were highly interesting and superior than Si for MEMS applications. The Young modulus was evaluated between 395-455 GPa and the estimated stress low. Resonance frequencies and quality factors of the SiC devices were higher than equivalent Si ones (around 60%).

To take advantage of the superior mechanical characteristics of SiC, we have then decided to realize smaller devices by integrating lateral electrostatic actuation/detection, and using the same starting material, SiC on Si. Using the same process and optimizing some steps, suspended devices with thicknesses higher than 1 μm, with width comprised between 0.8-2.5 μm and length up to 500 μm were successfully fabricated. Ohmic contacts were also formed with reasonable values for the contact resistivities, enough for electrostatic actuation. In this sense, the cantilever was correctly actuated but due to both poor electrical isolation of the SiC layer from the Si bulk and air-ambient measurements, it was very difficult to detect an electrostatic displacement current, and the resonance frequency was only optically detected.

Finally, to render possible a full electrical actuation/detection, other substrate material has been considered. SiC on semi-Insulated Silicon (SIS) and SiC on SOI were studied as possible materials for SiC electrostatic MEMS fabrication. Concepts to reduce the gap post fabrication have also been introduced and are currently investigation. The 3C-SiC monocrystalline growth process has been optimized on SIS and SOI substrate. SiC crystal quality has been corroborated by means of XRD, AFM, SEM and Raman. The results show that isolation of the bulk is critical to avoid leakage current and in reducing considerably the required voltage to actuate the SiC resonators. Full electrical resonance frequency measurements were also performed in the temperature range of 25-200 ºC, demonstrating the good stability of the SiC devices at these temperatures.

4.6 References

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5 CHAPTER V

NITRIDE RESONATORS

In this part, the III-nitrides, which represent an interesting alternative to the SiC material, were investigated. III-nitrides are particularly interesting since they have high mechanical properties, high Young's moduli, high chemical resistance, and moreover present piezoelectric properties which can substitute functional ceramics. Moreover, these materials can be made insulating, semiconducting, conducting, piezoelectric, and even confine electrons when used in heterostructures, depending of the doping, design, thickness, stress, etc… We have used recent advances in the growth of epitaxial AlN on Si to investigate this material, and its possible applications. This single crystalline material being interesting, preliminary measurements were performed to evaluate the piezoelectric properties. This material revealed an insulating behaviour that motivated us to investigate in this sense, and compare it with sputtered material. Therefore AlN was studied as an insulator, and the effect of its oxidation is evaluated. Then the realization of mechanical structures to demonstrate the feasibility of such structures based on this material is investigated and discussed.

5.1 Introduction

Due to its very good (5pm/V) piezoelectric properties, Aluminum Nitride (AlN) has been basically used for surface or bulk acoustic wave devices [1-2], taking benefit of the piezoelectric effect. Up to now, sputtered AlN was the most used for this kind of devices, but it is known that sputtered materials are of poor crystalline quality compared to epitaxial material [3]. Nevertheless, AlN has very interesting mechanical properties, and particularly a high Young modulus, a required and essential parameter for mechanical devices realization. To date, very few AlN-based devices have been fabricated using this feature [4-5]. Furthermore AlN is a wide bandgap material (E_g ~ 6.2 eV at 300 K), and is thus very resistant in aggressive environments, such as elevated temperatures, high pressures or corrosive liquids. Compared to other piezoelectric materials, such as ceramics (quartz, PZT…) which alter Silicon (Si) devices by contamination (with Zn or Pb ions), AlN has the advantage that it can be grown on Silicon. This compatibility with semiconductor technology is of particular importance to integrate this piezoelectric film with electronic devices. Moreover, AlN is biocompatible [6] and will have probably an important role to play in the field of chemical or biological MEMS and sensors. Some mechanical devices have been already fabricated with others materials, including Si [7], GaAs [8], SiC [9], GaN [10] and ZnO [11] but in most cases, the actuation and/or detection, based on electrostatic, optical or magnetomotive techniques, was difficult to implement and suffer from low output signals. All these aspects, and particularly the piezoelectricity which provides the possibility of integrated piezoelectric actuation and/or detection, coupled with high mechanical parameters, make AlN a suitable candidate for high sensitivity MEMS realization. Recently, Si and GaAs doped mechanical systems have been developed [12-13], thus allowing the integration of multitude of junctions directly onto the mechanical part. Such devices, extended to AlN material, the best compromise in terms of high mechanical and piezoelectric properties, could be a solution to the problematic actuation/detection of nano(micro)mechanical motion.
In such a way, Karabalin [14] from Caltech have recently reported an AlN piezoelectrical resonator using sputtered AlN sandwiched between two Mo electrodes thus demonstrating the efficiency of sputtered AlN for NEMS. Another solution, on

which we are working with CRHEA, could be to fabricate a piezoelectrical epitaxial AlN resonator sandwiched between two GaN (highly doped) electrodes.

In this chapter, the growth of the material is first described. As preliminary steps to determine the piezoelectric properties of this epitaxial AlN, Capacitance-Voltage (C-V) and Current-Voltage (I-V) measurements were performed, and indicated that this AlN has relatively good insulator behaviour. Therefore, further investigation was realized to verify this capability, comparing with sputtered AlN, and oxidizing for an eventual use in WBG passivation. We report on the characteristics of metal-insulator-semiconductor (MIS) capacitors with aluminium nitride (AlN) as the insulator material. AlN has been grown on (111) Si by means of Molecular Beam Epitaxy (MBE) and DC magnetron sputtering (SPU). AlN layers have been characterized before and after dry thermal oxidation in O_2. By analyzing changes in morphology and electrical properties, different oxidation mechanisms were identified, due to the crystalline quality difference of the AlN samples. In both cases, oxidation at 1000ºC was beneficial for the electrical characteristics of the MIS structures, presumably due to passivation of atom vacancies. Although AlN was only partially oxidized, the flatband voltage was reduced and the density of interface traps improved. Poole-Frankel conduction mechanism was identified for the SPU sample, and followed a hopping conduction one after oxidation.

After this preliminary step concerning the material characterization, two different methods are presented to fabricate freestanding single-crystalline AlN structures on Si(111) platform. In the two cases, the AlN layers were grown on Si(111) substrates by molecular beam epitaxy (MBE). The first method used is based on the etching of the AlN and Si materials while the second one is only based on Si etching, thus avoiding the use of undesirable based-chlorine gases. The two different fabrication processes are described, as well as mechanical properties of the released structures, i.e. Young modulus and residual stress, from wafer curvature, cantilever/bridge bending, resonance tests and micro-Raman scattering. Finally, other methods currently investigated at CNM for III-nitrides MEMS will be presented.

5.2 Material growth

Prior to the growth, a surface preparation was done in order to remove the native oxide and to produce a hydrogen passivated surface. AlN layers are grown in a Riber Compact-21 MBE system on 2 inches (111) Silicon wafers. Ammonia, used as N-precursor, is introduced through a thermal cracker cell heated at 300°C. The growth temperature is 900°C [15]. In the two methods, a 250 nm AlN thick layer is grown on the Si (111) substrate, with a growth rate of 0.1 µm/h. Thanks to the Reflection High-Energy Electron Diffraction (RHEED) real-time monitoring (figure 1), the growth parameters are adjusted in order to get both a smooth surface and a pure single crystalline wurtzite phase. Due to high mismatches in thermal expansion and lattice parameter between AlN and Silicon [16, 31-33], there is a huge tensile stress in these layers. With ammonia-MBE, Al-polarity films are obtained, achieving the best material quality, in contrast to the non-controlled polarity of sputtered films [17].

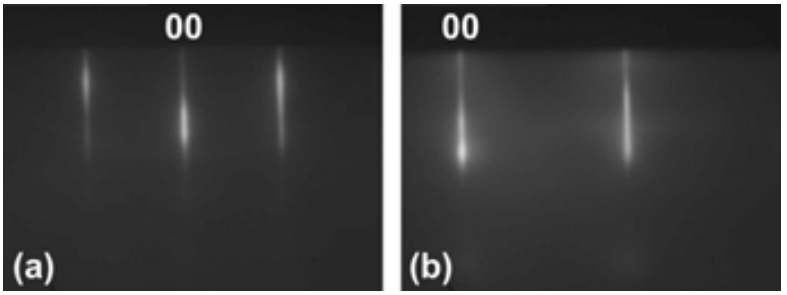

Figure 1. RHEED patterns along the (a) <1-210> and (b) <10-10> azimuths of a 250 nm AlN film shown the good surface quality of the layer.

The growth was completely similar for the two approaches. The RHEED patterns were streaky and thin (figure 1), suggesting a smooth surface and a good crystalline quality. After the two different growths, the samples are studied by atomic force microscopy (AFM) and by scanning electron microscopy (SEM) in order to determine the roughness and the surface morphology. The results demonstrate that layers grown on patterned substrates are as good as layers grown on full planar wafers, i.e. smooth and free of surface defects, with root-mean-square roughness about 5 Å for 2x2 μm² images. High Resolution X-Ray Diffraction (HRXRD) ω-scan rocking curve of the (002) peak was performed on the full wafer growth (figure 2).

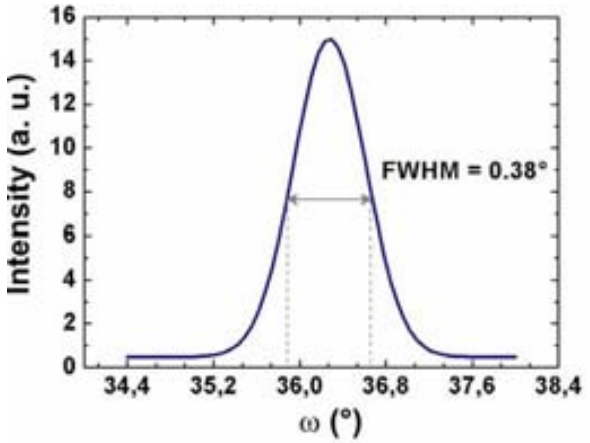

Figure 2. XRD Rocking curve of the (002) peak showing the good crystallinity of a 250 nm thick AlN layer.

The full width at half maximum (FWHM) of the peak is 0.38º showing that the epilayer is of very high crystalline quality (for comparison, sputtered AlN FWHM is superior to 1º [18]).

5.3 AlN material study through oxidation

As previously seen, the properties of AlN render it interesting for many applications and it has been successfully used as platform for smart deep UV solid-state light sources [18], resonators [19] and acoustic wave devices [20]. Moreover, undoped AlN is characterized by remarkably low electrical conductivity. It has a great potential for applications in metal-insulator-semiconductor (MIS) devices [21-25], especially due to its high breakdown field strength of more than 3.3 MV/cm. In addition, AlN is particularly suitable for III-V semiconductor MIS structures, where no thermal SiO_2 oxide can be grown. It has been well reported that AlN oxidation leads to oxides similar to alumina Al_2O_3 [26-30]. The study of AlN oxidation, and related AlGaN materials, is of great interest and may be employed to produce electrically insulating layers in GaN-based devices.
However, it is still a long way to exploit all the material potential advantages since technology is yet not mature enough. Here, we report on a comparison of the electrical interfacial properties of AlN layers 110 nm thick grown on Si by Molecular Beam Epitaxy (MBE) and DC magnetron sputtering. Thermal oxidation of these layers has been carried out on these AlN layers in an attempt of improving their electrical properties.

5.3.1 Samples preparation

MBE AlN layers (MBE) were grown in a Riber Compact-21 MBE system on 2 in. (111) n-type silicon wafers, as described in the previous section.

Sputtered aluminum nitride (SPU) was deposited (110 nm thick) in an Alcatel 610 DC magnetron sputtering equipment on n-type Si substrate at room temperature (Gas mixture of 50% N_2 and 50% Ar). AlN MBE (MBE ox) and SPU (SPU ox) thermal oxidation was carried out in a dedicated furnace in dry oxygen at 1000^{o}C for 1 hour.
Both processes, MBE at high temperature and SPU at room temperature, are commonly used techniques in clean room semiconductor technology. In general, the MBE growth of AlN films at high temperature (T>800ºC) results in layers with better crystalline quality. However, when deposited on Si, the resulting MBE AlN layers are more strained than SPU AlN, thus altering somehow the interface properties. Moreover, the high temperature can also promote the species inter-diffusion, thus being detrimental for the interface quality.

5.3.2 Structure and morphology

Surface morphology was examined using Optical Microscope (OM), Scanning Electron Microscope (SEM) and Atomic Force Microscope (AFM). A Focused Ion Beam (FIB) has been used to investigate the AlN layer structural composition and the AlN/Si interface. MBE AlN samples were further examined by a SIMS depth profiling technique. The crystal structure of thin films was determined by x-ray diffraction (XRD). The analyses of sample structure and composition have been done by x-ray diffraction (Rigaku-200B diffractometer) at room temperature. Capacitance and conductance measurements have been carried out using an Hg mercury probe Model 802B-200 with a computerized HP 4192 A Impedance Analyzer. This feature mitigates

the problem of the back contact resistance, which is the main source of series resistance in MOS capacitors. Furthermore, this method allows skipping any metallization step resulting in a bare surface suitable for subsequent process. Current vs voltage characteristics have been measured using a Keithley 251 IV SMU system.

The samples were first investigated with OM. Delimited colored zones regularly disseminated were observed for SPU ox suggesting regions of different oxide thickness. The oxide color was much more uniform for the MBE ox. This is related to a higher crystal quality, more uniform morphology and stress of the epitaxial AlN compared to the sputtered one (see XRD section below). It can be suggested [17] that sputtered AlN is composed by a mixing of both Al and N-polarity, while epitaxial AlN is unipolar. This polarity can also influence the oxidation rate, since the N-face oxidizes faster than the Al-face.

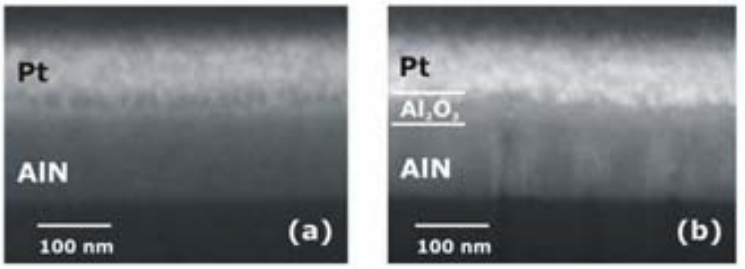

Figure 3. SEM (cross section) of AlN layers (a) grown epitaxially on Si and (b) oxidized.

Cross-section SEM micrographs of MBE AlN sample before and after oxidation are shown in figure 3. A thin Platinum (Pt) layer was deposited to improve microscopy imaging. It has been widely reported the formation of thin (2-3 nm thick) native oxide growth (Al_2O_3) on the AlN surface. A stacked structure was revealed from figure 3(b), confirming the oxide formation (35 nm thick), after oxidation at 1000ºC for 1 h. This thermally grown layer exhibits good uniformity with a basically abrupt interface with the remaining AlN. Nevertheless, the AlN micro-structure was modified to some extend with extended defects and dislocations becoming evident. This is probably due to both, oxygen incorporation into the AlN layer and Silicon diffusion into the AlN, ie. diffusion of Al and O atoms into the Si substrate, amorphous SiO_x interfacial layer and passivation of N vacancies and other defects created during growth could take place [30,34,35]. Previous works [34] have reported oxidation rates significantly higher. This oxidation rate depends on the crystalline quality of the AlN to be oxidized: A layer by layer mechanism on optimized crystalline AlN material may only thermally grow few nanometers of oxide as seen in figure 3. This concords with the limitation of the oxidation through the initially formed oxide surface (Deal-Grove linear rate) thus acting as protecting layer. It is worth to mention that 1000^{o}C have been often seen like a kind of transition temperature to higher oxidation rates. We have observed that in our furnace, the temperature can vary by around 50ºC depending on the sample position. This could also be an explanation, since oxidation at 950ºC gives oxidation rate values significantly smaller. One additional reason could be that the Al-polarity of the MBE sample can influence the oxidation rate, since Al-face oxidizes slower than N-face.

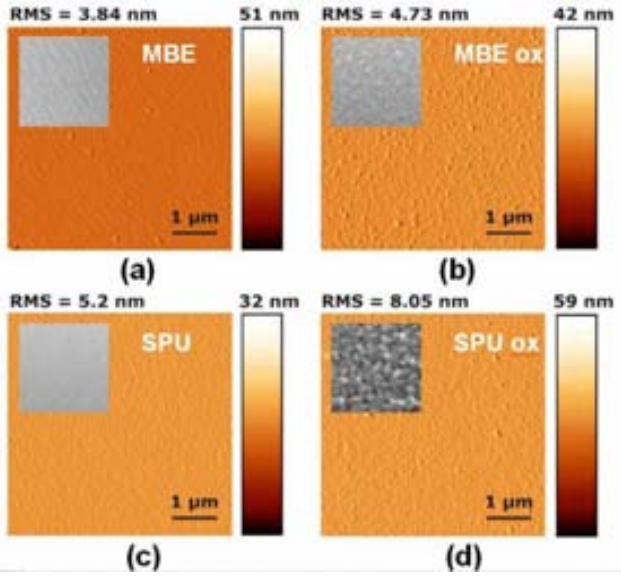

Figure 4. AFM (Inset: SEM) images of 5 µm × 5 µm areas for the (a) as grown (MBE) and (b) oxidized AlN (MBE Ox), and for the (c) as deposited (SPU) and (d) oxidized AlN (SPU Ox).

Thermal annealing also results in morphological changes as revealed from AFM experiments (figure 4). For the MBE samples the surface topology is clearly different before and after oxidation though the roughness rms value is similar 4-5 nm. Before oxidation, MBE AlN presented large terraces due to step bunching formation, becoming more granular or bubble-like after oxidation. For the SPU AlN samples, the rms roughness is significantly increased, from 5.2 nm before oxidation, to more than 8 nm after oxidation. As for MBE ox, the morphology is more granular-like than before oxidation. The SEM images (inset figure 4) reveal that the MBE ox sample presents smaller pore density when compared to the SPU ox sample. This higher density of interstices of SPU ox suggests that the oxidation mechanism is more three-dimensional-based. SPU AlN exhibits a more spongy morphology with amorphous-like material clustering helping to provide a way for an easier oxidation through improved diffusion. On the other hand, a typical epitaxial layer by layer oxidation mechanism is expected for MBE AlN because thermal oxidation of epitaxial AlN is rather slow, as stressed above.

Crystalline microstructure was investigated by means of X-ray diffraction. The analyses of sample structure and composition were carried out both in the θ–2θ Bragg Brentano geometry using a Rigaku diffractometer which has a focused monochromatic Cu Ka1 rotated source with radiation λ = 1.54Å , and using a Bruker AXS GADDS. The XRD peaks for all the samples are shown in figure 5. The MBE AlN exhibited only one peak corresponding to the wurtzite phase in (002) orientation, which was slightly shifted upon oxidation. No other peaks were observed after oxidation. Polycrystalline AlN presents main peaks at 33.24º, 36.12º and 37.94º, corresponding respectively to the (100), (002) and (101) orientations. The XRD pattern of SPU films do not show any definite crystalline phase, suggesting that they are mostly amorphous (also the surface of as-grown SPU AlN seems to be amorphous with no grains visible). After oxidation, the peaks completely vanished and no other additional peaks were observed. However,

since the atomic form factor of the gamma alumina is very small compared with that of AlN, it can be difficult to detect any weak Bragg peak, with our X-Ray diffraction set-up. Although there is no XRD peak after oxidation of SPU sample, the formed aluminum-oxide might not be amorphous.

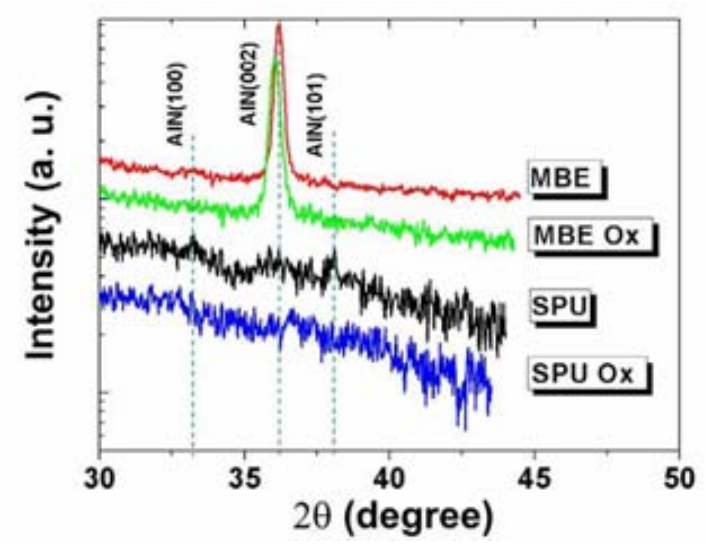

Figure 5. X-Ray diffraction intensity vs scattering angle (2θ) of as grown and oxidized films.

5.3.3 Electrical Characterization

The typical high frequency capacitance-voltage C-V characteristics for the AlN and oxidized AlN samples are presented in figure 6. The frequency of the C-V measurements was 100 kHz to minimize the series resistance effect. The contact area was 4.5×10^{-3} cm^2. From figure 6 it can be seen that MBE samples have switched the doping type behavior to p-type because of the surface preparation and the MBE growth. This behavior was not expected and SIMS measurements were then performed (figure 7). It can be inferred that Al atoms have been incorporated in the Si surface while Si atoms have diffused towards the AlN layer. The extracted acceptor concentration value was 5×10^{17} cm^{-3}.

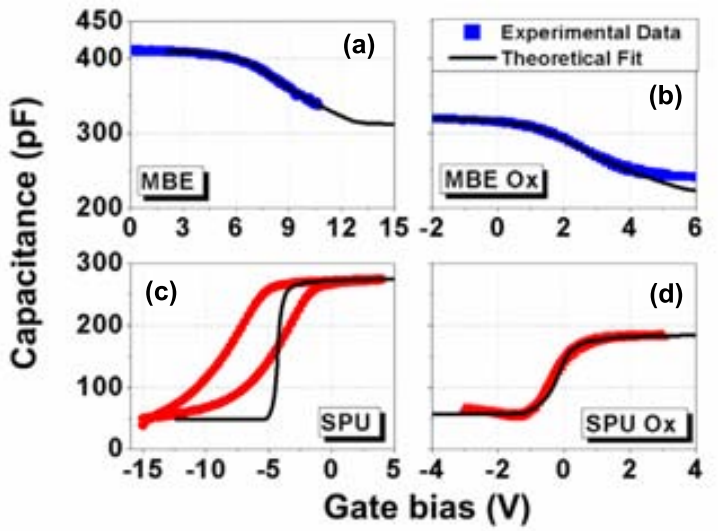

Figure 6. Capacitance-voltage characteristics of MIS capacitors for the (a) as grown (MBE) and (b) oxidized AlN (MBE Ox), and for the (c) as deposited (SPU) and (d) oxidized AlN (SPU Ox).

The dielectric constant was determined from the value of the capacitance, with the capacitor biased in strong accumulation mode at 100 kHz. The high-*k* dielectric property of the insulator is given by a dielectric constant for mono-crystalline AlN reported in the range of 8-10.4 [23]. The dielectric constant experimentally determined for the MBE AlN was of ε_r=10.2 (MBE) and ε_r=8.7 (MBE ox). The dielectric constant experimentally determined for the SPU AlN was of ε_r=7.5 (SPU) and ε_r=5.0 (SPU ox). Kang et al. [34] reported that crystalline aluminium silicate ($Al_xSiO_{2-\delta}$) and amorphous (a-SiO_2) interfacial layers are formed by diffusion of Si atoms into the resultant Al_2O_3 film, during thermal oxidation of AlN/Si. This would explain the fact of a reduced dielectric constant after oxidation. Sputtered insulator layers (and hence, amorphous or with few degree of crystallinity due to poly or nano-crystals) usually exhibit lower dielectric constant than crystalline materials from epitaxial growth or with induced crystallization [36]. Our results seem to confirm this trend.

MBE shows a positive flat-band voltage shift while SPU shows a negative shift. In both cases, this shift is an indication of trapped charges in the bulk AlN and/or in the AlN/Si interface. For both, MBE and SPU, this shift is reduced after oxidation. SPU samples also exhibit a marked hysteresis behavior that accounts for a larger slow interface traps density.

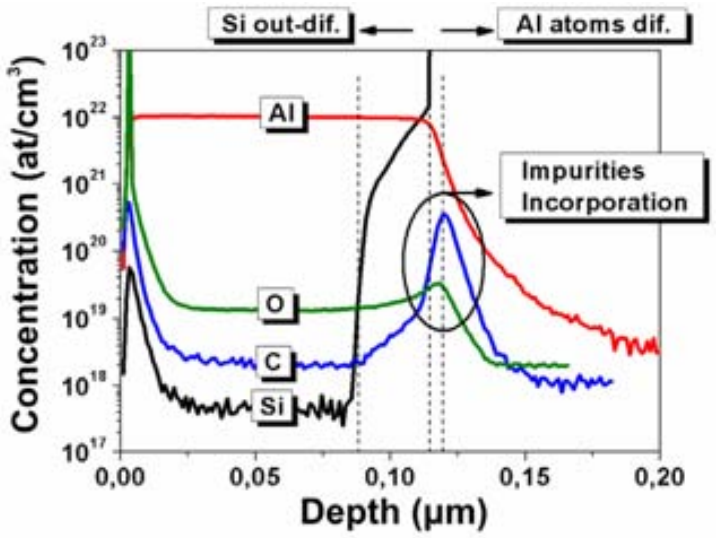

Figure 7. SIMS depth profile of the MBE sample.

An estimation of the interfacial trap density has been determined (figure 8) from the C–V deviation from ideal characteristics, by means of the Terman method [37]. The interface state density (D_{it}) spectra within the bandgap close to the valence band and conduction band, for the AlN capacitors implemented on p-type and n-type Si substrates, respectively, is presented. An interface state density of $2.5\text{x}10^{11}$ $cm^{-2}eV^{-1}$ has been extracted at $E_T–E_V = 0.25$ eV for the MBE sample, similar to $1.8\text{x}10^{11}$ $cm^{-2}eV^{-1}$ extracted at $E_c–E_T = 0.25$ eV for the MBE ox sample. As mentioned above, it can be inferred that a thin amorphous SiO_x layer will almost certainly contribute to an increase in some way of the density of interface states and would explain the analogous interface properties before and after oxidation.

The D_{it} profile close to the conduction band for the SPU sample is also presented in figure 8(b). A large interface state density of $7.3\text{x}10^{12}$ $cm^{-2}eV^{-1}$ has been extracted at $E_c–E_T = 0.25$ eV before oxidation. This may be attributed to a large number of dislocations, roughness and lattice mismatches at the AlN/Si interface presumably related to the low temperature growth. The D_{it} value significantly drops to a value of $5.0\text{x}10^{11}$ $cm^{-2}eV^{-1}$ after oxidation, which is comparable to the MBE sample, due to the high temperature annealing which might improve the interfacial properties together with and amorphous SiO_x interfacial layer formation.

I-V measurements have been carried out on the MIS structures (gate biased in accumulation i.e., n-type gate bias positive and p-type negative) as shown in figure 9(a). MBE with higher crystalline quality results in lower leakage current compared to SPU films. MBE ox and SPU ox exhibited a reduced leakage current when compared with MBE and SPU, respectively. This is attributed to a coupled effect of oxygen atoms in the AlN layers: the formation of amorphous SiO_x interfacial layer and passivation of N vacancies and other defects created during growth. Transport in thermally grown SiO_2 (and hence, in a insulator with a reduced defect density) at low gate voltage is fitted by a process known as hopping conduction or phonon assisted tunnelling [38]. In such systems, electrons are trapped in spatially localised states.

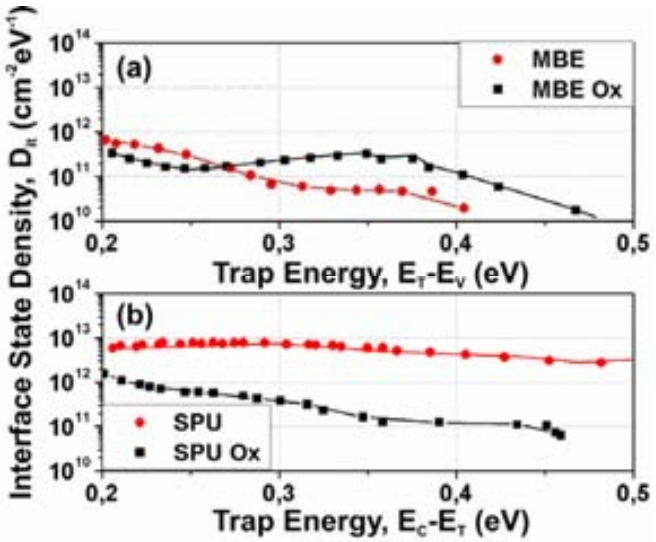

Figure 8. Interface state density for (a) MBE and oxidized MBE AlN (b) SPU and oxidized SPU AlN.

To conduct, electrons need to hop from state to state and this mechanism yields an ohmic characteristic (linear with the electric field) exponentially dependent on temperature. The situation can be different for the dielectrics based on AlN, where trap assisted mechanisms may play an active role. With a theoretical energy threshold of 3.2 eV [39], the Schottky emission phenomena, in which only electrons with sufficient energy to surmount the surface potential barrier (barrier height ϕ_t) are able to escape the condensed phase, should be negligible. However, because of the N vacancies and other defects incorporated during the AlN layer growth, the barrier height felt by the electron may be distorted. The leakage current induced by the vacancies, calculated by considering a model based on a continuous band diagram or integrating the local leakage current densities at the interface [40], follows a Schottky emission model. On the other hand, the insulator-bulk defect-related Poole-Frenkel emission is due to field-enhanced thermal excitation of trapped electrons into the conduction band [38]. For trap states with Coulomb potentials, the expression is virtually identical to that of the Schottky emission. The expressions for hopping conduction Schottky emission and Poole-Frenkel mechanism are [38]:

$$J_{HO} = C_1 E \exp\left(-\frac{q\phi_a}{kT}\right) \qquad \text{Eq. 5.1}$$

$$J_{SE} = A^* T^2 \exp\left(-\frac{q\phi_t}{kT}\right)\exp\left(\frac{E^{1/2}}{kT}\sqrt{\frac{q^3}{4\pi\varepsilon_0 K_T}}\right) \qquad \text{Eq. 5.2}$$

$$J_{PF} = C_2 E \exp\left(-\frac{q\phi_t}{kT}\right)\exp\left(\frac{E^{1/2}}{rkT}\sqrt{\frac{q^3}{\pi\varepsilon_0 K_T}}\right) \qquad \text{Eq. 5.3}$$

where A^* is the effective Richardson constant, C_1 and C_2 are constants, q is the electronic charge, k denotes the Boltzman constant, T is the temperature, ε_0 denotes the permittivity of free space, K_T is the high frequency dielectric constant, square of the

refractive index (n) and E denotes the electric field. In Eq. (1), ϕ_a is the activation energy of electrons. A coefficient r is introduced in Eq. (3) to take into account the influence of the trapping or acceptor centers ($1<r<2$) [41]. The Schottky emission and Poole-Frenkel mechanisms present the same characteristics in a $ln(J/E)$ *vs* $E^{1/2}$ plot due to the same voltage dependence on the current density, (the linear dependence of Poole-Frenkel expression is negligible when compared with the exponential dependence). Hence, the way to distinguish both current mechanisms is by determining the slope of the $ln(J/E)$ *vs* $E^{1/2}$ plot and considering as well, if it is compatible with the high frequency dielectric constant value optically determined or previously reported [39]. Simulations have been performed with the set of equations described above to fit the experimental I-V traces. A theoretical model accounting for a double hopping/Schotkky emission conduction mechanism has been used [42]. At the lower electric fields (< 1 MV/cm), hopping mechanism seems to establish the carrier transport properties of the MBE and SPU AlN layers. The current at higher gate bias seems to be described by the Schottky emission theory (MBE and SPU) and then, Poole-Frenkel relation at the AlN insulator bulk (SPU), as it can be derived from the figure 9(b).

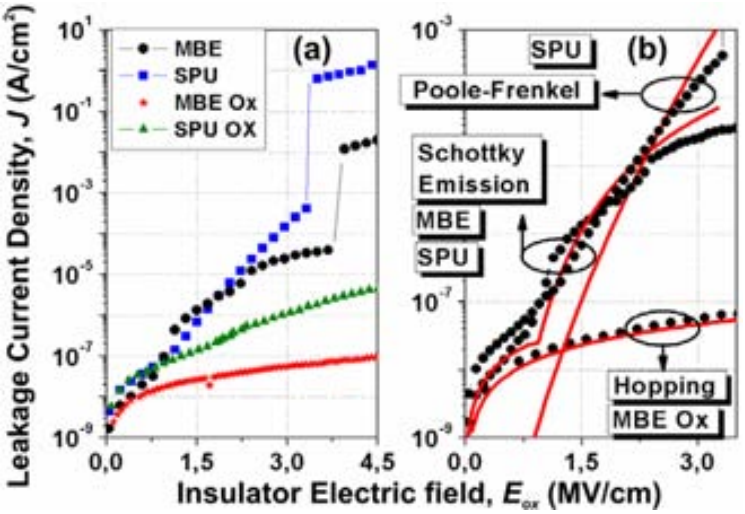

Figure 9. (a) Current-voltage characteristics of MIS capacitors for the as grown (MBE) oxidized AlN (MBE Ox) and for the as deposited (SPU) oxidized AlN (SPU Ox). (b) Conduction mechanism for the different layers.

These results clearly indicate that defect-related conduction mechanisms such as Poole-Frenkel are more relevant in sputtered AlN layers when compared to MBE AlN. SEM measurements revealed a more columnar structure after MBE AlN oxidation suggesting a higher number of extended defects on the AlN bulk. However, this was not correlated with a higher leakage current or premature breakdown. On the contrary, oxidation appears to have a beneficial effect resulting in a presumably passivation of nitrogen or other atoms vacancies of the AlN films as mentioned above. After the dry oxidation, MBE and SPU AlN follow a hopping conduction mechanism up to the dielectric breakdown for electric fields of more than 6.5 MV/cm. This dielectric breakdown value should be increased if adequate passivation schemes are applied to the test MIS structure.

5.4 Resonators fabrication

The first technique used, named full-area-growth (FAG) approach, is based on traditional methods, on patterning and etching the structural material. A photoresist mask layer is deposited and patterned during the lithography step. Next, the pattern is transferred to the AlN film using $Cl_2/Bl_3/N_2$-based anisotropic reactive ion etching (RIE) using a Quad Drytek System. Cl_2, BCl_3 and N_2 gases are introduced at 7, 25 and 40 sccm respectively, with a RF power of 125 W at a pressure of 325 mTorr. The AlN etching rate under these conditions was reasonable (80 nm/min) and allowed to obtain well-defined vertical sidewalls, without trenching or micromasking effects. Finally, the underlying Si layer is etched by fluor-based isotropic solutions, such as $HF:HNO_3:H_2O$ or $NH_4F:HNO_3:H_2O$, releasing thus the suspended structures. No protection of the AlN layer was needed since high quality AlN is resistant and only some defects could be etched. Different optical images can be seen at different steps of the process in the figure 10. It is interesting to note that in some areas, the Si is undesirably etched though punctual defects (figure 10(d)), while in other areas undesired Si etching seems following particular directions (figure 10(e)), leading to AlN separation, and thus structures breakdown. We are still investigating this phenomenon, and trying to find a solution to avoid this separation. Theses images also show that the patterns are well replicated without any dimensions loss.

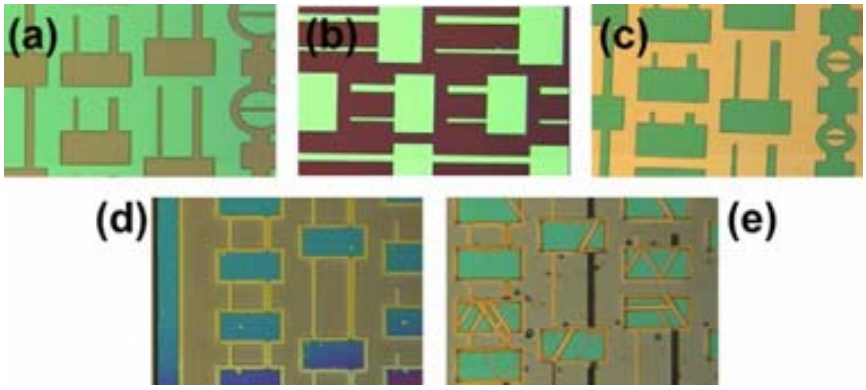

Figure 10. Optical images of the AlN etching process during the FAG approach (a) with photoresist mask (b) part of the AlN etched by RIE (c) AlN totally etched and (d),(e) Si chemically etched in different areas views.

To date, AlN was always etched for the fabrication of cantilevers using chlorine based-plasmas [4-5]. Only Yang and al. [43] reported GaN cantilevers fabrication without etching the structural material. Using this principle technology for AlN, we have obtained the same AlN suspended structures without etching the structural material. This concept, named selective-area-growth (SAG) approach, is based on AlN growth on a Silicon patterned substrate. Thus the same microstructures can be realized with common silicon micromachining equipments. The process begins first by the anisotropic patterning of Si substrate using optical lithography and inductively coupled plasma deep reactive ion etching (ICP-RIE) in an Alcatel A601 equipment.

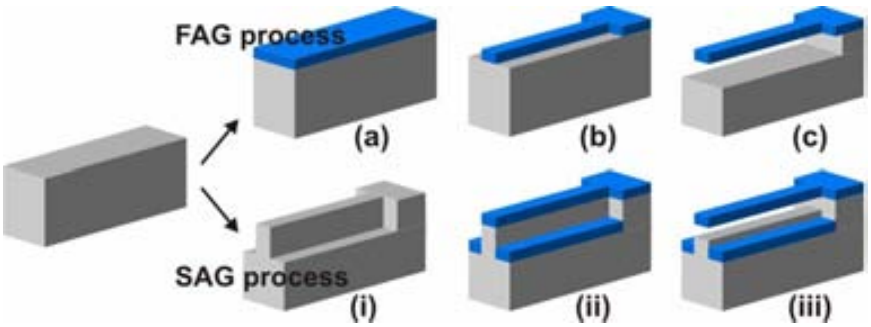

Figure 11. Schematic showing the two different used processes, FAG (Full Area Growth) and SAG (Selective Area Growth). (a) AlN growth, (b) AlN dry etching, (c) Si wet etching. (i) Si dry etching, (ii) AlN growth, (iii) Si wet etching.

A plasma of SF_6 and C_4F_8 was used at a pressure of 2.1 Torr, with respective flows of 150 and 100 sccm, with a 1500W ICP power and a DC bias of 120V. Then AlN is grown on patterned substrate in similar conditions than those grown on full wafer. Only a wet etch is then done to release the microstructures. Although a thin AlN deposit can be observed on the sidewalls of the silicon vertical facets, this is of poor quality and can be easily etched away. A detailed scheme of the two used processes is shown in figure 11. Moreover, the epitaxial layers replicate quite well the initial substrate patterning [17], and as confirmed by the SEM images in figure 12. It is interesting to note here the presence of AlN grains and their size. In fact, during this first SAG process no particular cleaning was performed before the growth and the resulting AlN was polycrystalline (also confirmed by RHEED).

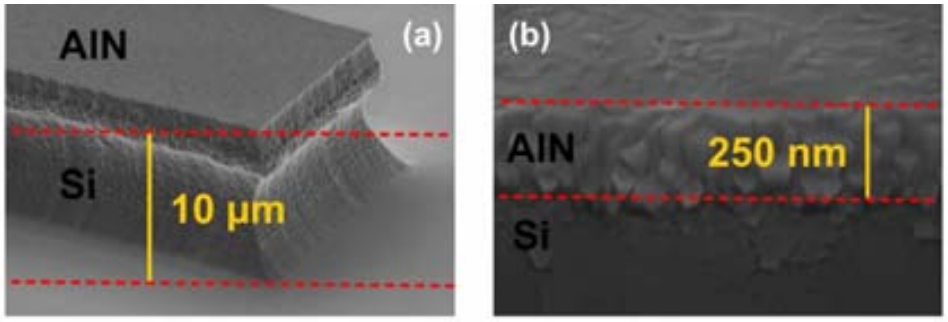

Figure 12. SEM images of the SAG showing (a) the etched Si depth (b) the polycrystalline AlN thickness and grains size.

As it has been previously indicated, in some areas of the wafer, the epitaxial AlN layer presents cracks, especially after the Si chemical etch. We are currently investigating this phenomenon, which induces physical separation of AlN zones after release (figure 13). Different causes are suspected, (1) the thickness of the epitaxial layer is close to a critical thickness responsible of cracks, (2) the different steps induce a high constraint to the wafer, or (3) the Si under the AlN is highly compressed and its breakdown is favoured during the chemical etching. The AlN separation seems to appear just few minutes after the dipping. In any cases, many devices were entirely intact.

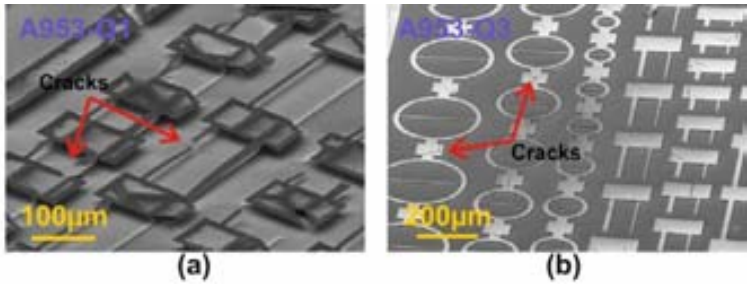

Figure 13. SEM images of typical cracks observed after the chemical etching for releasing the structures (a) A953-Q1, (b) A953-Q3, after few minutes.

Examples of the fabricated devices by the two different methods are shown the figure 14. To demonstrate the high quality of the material obtained on patterned substrate, we compare the results obtained on microstructures bending and resonance frequencies between the two different growths.

Various microstructures with different geometries (from 10 to 200 µm long and 10 or 20 µm wide) were fabricated. Low bending (<2µm) was observed for cantilever structures length shorter than 80 µm, for the two processes, revealing low stress gradient level. This is preferable to avoid high deformation and even structure breaks.

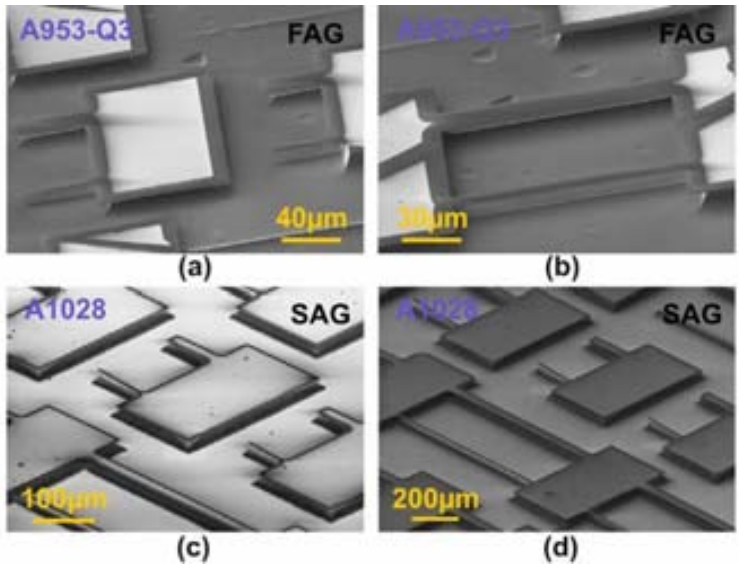

Figure 14. SEM images of 50 µm long cantilever structures fabricated by (a) and (b) full-area-growth, cantilever and bridge. (c) and (d) Selective-area-growth approach, cantilever and bridge. In (c) and (d) the wider structures are not released.

5.4.1 Mechanical characterization

We have measured the cantilever fundamental resonance frequencies of both approaches. For a resonator, the resonance frequency is determined by Young modulus and structure's geometry according to the relation Eq. 2.10. Many techniques used for actuation of suspended devices rely on magnetomotive excitation and require a metallization layer [4,5-7,8], thus shifting the resonance frequencies by added mass and reducing the sensitivity. We have used piezoelectric excitation with a PZT actuator in order to not alter the resonance frequencies. Various devices of the two different processes with different length/width ratios have been measured and optically detected by an interferometric system [20].

From resonance frequencies measurements, shown in figure 15 and reported in Table V-1, we have evaluated average Young moduli of 286±5.5 and 272±11 GPa for SAG and FAG approaches respectively, in good agreement with the reported values [16].

Table V-1. Measured resonance frequencies and determined Young's moduli of various cantilevers fabricated by FAG/SAG approach. In the last line are included the average values of the Young's moduli.

	SAG approach (AlN 240 nm thick)		**FAG approach (AlN 260 nm thick)**	
Length (µm)	f_{res} [kHz] measured	E [GPa]	f_{res} [kHz] measured	E [GPa]
50	147	292	153	270
40	225	280	234	258
30	404	285	435	283
-	-	**286**	-	**271**

Cantilever resonance frequencies were clearly identified, while for the bridges, nothing was observed. We explained this due to the high tensile axial stress expected in the AlN film (estimated between 0.5 and 1.5 GPa [44]), which affects considerably the expected bridges resonance frequencies by increasing the stiffness. The stress is a very important parameter that could be problematic for the expected designed device functionality, especially when it induces defects or bending. However, the tensile strain could be advantageous, and could significantly increase the resonance frequencies and quality factors of bridges [45,46]. For example, for a 250 µm long bridge, a fundamental resonance frequency f_1 of 37 kHz is expected, but under tensile axial stress, this value could increase considerably according to [47]:

$$f_1(\sigma) = f_1\sqrt{1+\frac{\sigma L^2}{3.4Eh^2}} \qquad \text{Eq. 5.4}$$

thus reaching a value comprised between 0.87-1.3 MHz [for an estimated stress range between 0.5-1.5 GPa], more difficult to actuate with our set-up. Tuning the residual stress through adjusting growth conditions could be a very interesting technique for obtaining high resonance frequencies values. Quality factors between 150-200 were obtained, slightly superior than those obtained from equivalent SiC devices [48].

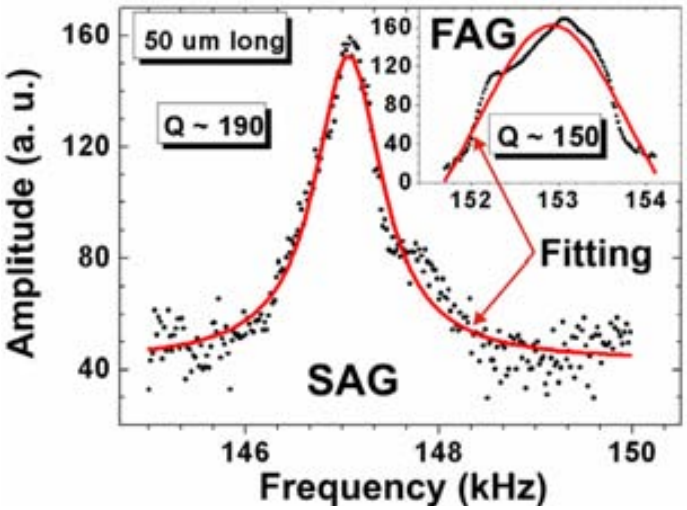

Figure 15. Measured resonance frequency of a 50 µm long AlN cantilever fabricated with SAG approach. Inset: measured resonance frequency of an equivalent AlN device fabricated with FAG approach.

To evaluate the axial stress, a Raman analysis [49], identical to the one used for SiC devices in the previous chapter, was performed. The residual stress is then determined from the E_2^2 phonon frequency, by the relation Eq. (4.7) previously defined, the Raman stress factor being $k = 6.3\ cm^{-1}\,GPa^{-1}$ [44] and the bulk phonon peak at 657.4±0.2 cm^{-1} (zero stress energy).

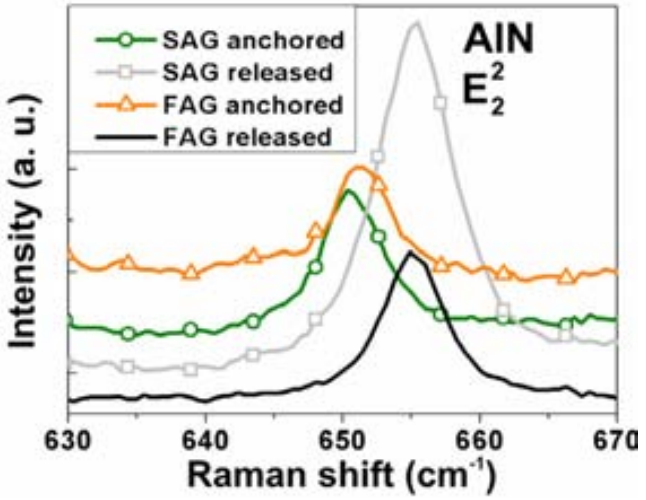

Figure 16. Raman spectra of the AlN obtained from FAG and SAG approach at anchored and released position.

The Raman spectra recorded on bridges for the FAG and SAG approaches are reported in figure 16. We have measured basically on 2 sites, the first one at anchored position (so with Si below), and the other one, at released position (without Si below). From the spectra, the redshifted phonon peak clearly showed the presence of a tensile stress component in such materials, as expected due to thermal expansion mismatch.

From the FAG structures, the phonon energy peak appears at 651.4 cm^{-1} at anchored position and at 655.2 cm^{-1} at released position. This indicates first that the stress between the two materials is about 1 GPa, but also that the released structures still possess a component of tensile stress ~ 340 MPa. These results, higher than those obtained from sputtered material, matches with these obtained from wafer curvature measurements [3]. From the AlN SAG structures, the phonon peak appears at 651 cm^{-1} at anchored position and at 655.4 cm^{-1} at released position, corresponding to similar stress level obtained from the first approach. This value is surprising, due to the fact that a lower stress could be expected due to the edge relaxation, but this effect is probably negligible due to the large size of the devices. First attempt for SAG approach gave AlN devices with polycrystalline quality, in part from surface contamination due to the mask layer. From these devices, stress values of ~520 MPa and ~240 MPa at anchored/released position have been found, showing clearly that the better the crystalline quality the higher the strain. Moreover, a slight dimensions loss was observed during the Si etching of this polycrystalline layer, but without the typical undesired Si etched lines observed for the single crystalline AlN.

5.4.2 Resonators using AlGaN/GaN heterostructure

III-nitrides MEMS employing the AlGaN/GaN heterostructure are interesting due to the 2DEG at the interface that could be used for actuation and/or detection. Moreover the piezoelectricity of the AlGaN layer can also be used. As described in the *Chapter 2*, different actuation/sensing mechanisms can be used in MEMS. The magneto-motive one is probably the easiest to implement but require both a metallic layer and the use of an external magnet. The electrostatic principle, as used in the last chapter, is probably the most reported, especially for Si MEMS, but often requires an electronic signal amplification to increase the signal-to-noise ratio. AlGaN/GaN material offers the possibility to fully integrate the sensor and eventual associated electronics circuitry in the same fabrication process.

The operating principle is similar to a single piezoelectrical driven beam-based resonator [50], using a single piezoelectric layer (usually PZT), sandwiched between metallic layers, and with two separated electrodes on each clamping side, forming the excitation and readout electrodes. When a voltage is unilaterally applied to the beam, the piezoelectric layer is vertically (i.e. in the direction of the applied voltage) deformed, being slowly compressed or stretched. Therefore, in the opposite side, the beam is also deformed, and this deflection can be detected to the inverse piezoelectric effect. To favour the fundamental resonant mode, and obtain maximum excitation and readout signals, the electrodes have to be situated close to the ¼ and ¾ of the beam length [50]. Moreover, DeVoe [50] reported that piezoelectric devices provide higher output signals than electrostatic ones.

Recently two works concerning AlGaN/GaN resonators have been reported [51, 52]. We are currently investigating and designing new structures with the aim of fabricating nitride resonators, such as the one reported in figure 17.

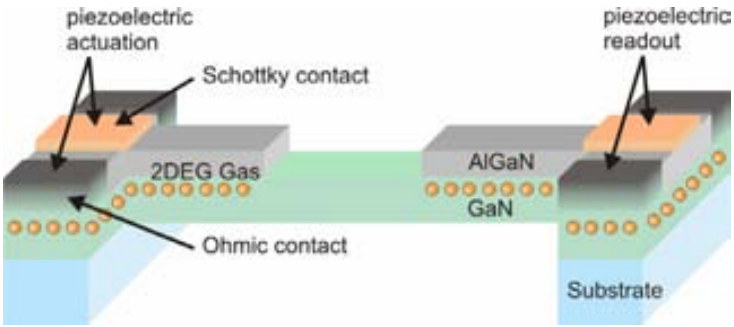

Figure 17. A possible bridge-based MEMS structure based on an AlGaN/GaN heterostructure and taking advantage of the 2DEG for both actuation and detection.

5.4.3 Summary

In conclusion, in this chapter, the insulator properties of the epitaxial AlN has been first investigated, by thermally oxidizing (1000 ºC) AlN in O_2. AlN has been grown by both, DC magnetron sputtering (SPU) and Molecular Beam Epitaxy (MBE), and their physical and electrical characteristics were compared. XRD measurements have revealed the amorphous (or weakly polycrystalline) nature of sputtered AlN when compared to the wurtzite phase (002) orientation epitaxial MBE material. The textured polycrystalline AlN resulted in rougher surface as well as a higher oxidation rate. MIS capacitors were fabricated and characterized. MBE AlN exhibited a higher dielectric constant value of 10.2 when compared to 7.5 for SPU AlN. After oxidation, these dielectric constants further reduced, probably due to the amorphous aluminum silicate and amorphous SiO_x interfacial layers are formed by diffusion of Si atoms into the resultant Al_2O_3 film. The density of interface traps (D_{it}) has been extracted for all the samples. MBE samples showed much lower D_{it} (2×10^{11} $cm^{-2}.eV^{-1}$) rather than SPU (7×10^{12} $cm^{-2}.eV^{-1}$). After thermal oxidation, the D_{it} on SPU sample was significantly reduced, while on MBE sample remained almost the same. Hopping, Schottky Emission and Poole-Frankel conduction mechanisms have been identified after I-V stress and modelling. Poole-Frenkel insulator trap assisted current is more relevant for SPU sample, suggesting a larger number of N vacancies and other defects created during the AlN growth. The insulator strength of the layer greatly improves after oxidation where hopping phenomenon is the major conduction mechanism for low to medium dielectric fields.

Then we report two methods for the fabrication of suspended devices from AlN on Si(111) substrates. Releasing AlN structures from Si(111) usually requires dry ICP etch process using chlorine-based plasmas. A technique has been successfully demonstrated for fabricate AlN MEMS without direct etching of the structural material, and only using the well controlled Si etching techniques. We have also determined the mechanical parameters of AlN from resonance frequencies measurements and micro-Raman scattering, and the results obtained were similar for both growth approaches. Moreover, we have reported that a high tensile stress is advantageous to increase resonance frequency and quality factor, especially for devices operating in air. We believe that this method will be very useful to fabricate highly sensitive AlN-based piezoelectric MEMS and sensors. The next step will be the fabrication of FBAR from epitaxial AlN directly on Si substrate to obtain thinner high tensile films and thus higher resonance frequency and quality factor than those obtained from sputtered AlN [53, 54].

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6 CHAPTER VI

NITRIDE TRANSISTORS

The work described in the previous chapters mainly concerned the realization of WBG MEMS to explore first the properties of such materials, and then propose solutions to the fabrication of more complex structures. For this, it has been necessary to establish the technology to realize the micromachining of SiC and AlN layers on Si. This has required a great deal of technological innovations such as, fast and well-controlled etching process of the epitaxial layer and the substrate, electric contact definition, sometimes with implantation. In addition to this study, it could be interesting to consider the WBG transistor fabrication, since up to now no reliable process has been still established. The success of the Si MEMS relies on its full technology that allows easy integration of electronic devices, such as CMOS. In this sense, one of the first steps towards circuitry development is to establish a reliable technology for WBG transistors. Thus, apart from MEMS, other solid state devices such as metal-oxide-semiconductor field-effect transistor (MOSFET) and high electron mobility transistor (HEMT) will be considered to complete on-chip integration. Compared to the advanced silicon or even SiC process technology, GaN is still in its early stage, particularly for resonator and MOSFET technology. Since our group is specialized on SiC transistors, with several PhD thesis realized on the SiC/SiO_2 interface and SiC MOSFETs fabrication [1-5], this work explore GaN transistors study.

Therefore, in this section, the main technological steps for GaN transistor fabrication have been studied. The first part will briefly concern the surface cleaning/preparation, which is particularly important for III-nitrides. Then ohmic contacts formation will be investigated on Si-implanted p-type GaN and n-type AlGaN/GaN. A third part will concern the study of different dielectrics on GaN, especially SiO_2. Finally, the last part will concern the results of the electrical measurements of the first fabricated GaN MOSFETs at CNM and HEMTs from CRHEA (France), as function of the temperature.

6.1 Cleanings

The GaN surface exposed to air is rapidly contaminated with oxygen and carbon, which can be problematic for interfaces realization. Thus an efficient cleaning is a crucial requirement before realizing any interface, either with metals or dielectrics.

Different conventional methods exist to remove any metallic and organic contaminants from the surface. However, these methods always leave a thin oxide layer on the surface, of thickness similar to the native oxide. Some techniques have been reported to give satisfactory results and will be here reported. Common problems on surface stoichiometry, the effects of wet chemistry and the relative cleanliness of n-type and p-type GaN surfaces are also discussed.

As received, GaN usually shows amounts of oxygen and carbon on the surface, which increases after exposure to photoresist. Process steps such as photolithography or etching induce carbon contamination and chemical residues on the surface. GaN surface forms a thin GaO_x when exposed to air, which can increase the contact resistance of ohmic contacts, especially if combined with the presence of any organic residues. This undesired layer can also be detrimental for dielectric interfaces, increasing the density of interfaces states. After solvent cleaning, hydroxide species (OH^-) are often present on GaN surfaces. The carbon contamination on the GaN surface comes from the C-O and C-H bonding. The C and O contamination cannot be easily removed, either at temperature higher than the decomposition one (around 800-850 ºC).

Efficient methods to remove a thin oxide are the same methods than the ones used during epitaxy, the 'growers recipes'. Usually, they use plasma or thermal treatments that are satisfactory in reducing these contaminants, however they are less feasible with typical metal or dielectric deposition equipment. The use of an O_2 plasma or a reducing environment such as H, at high temperature (usually near the temperature growth) are efficient methods. HCl or HF are efficient to remove any native oxide from the surface but not to eliminate contaminants (especially carbon and chlorine). The UV/ozone treatment is also useful in greatly decreasing the hydrocarbons. A typical surface cleaning may include an organic solvent treatment, acid etch and rinsing in deionized water but the results can be improved with a UV/O_3 oxidation after the acid dipping. The use of dry etching techniques before forming interfaces, such as dielectric/GaN interface, are also been reported as a way to reduce the surface defects [6].

King and al reported an interesting review on III-nitrides cleaning [7]. From this work, many researchers working on GaN have applied the standard 1:1 $HCl:H_2O$ etch (1 min, rinse with DI water, blow dry N_2) followed by a 1:99 $HF:H_2O$ etch (1 min, rinse with DI water, blow dry N_2) for surfaces cleaning. However, few works reported more information about the cleaning effects and modification of the GaN surface [8, 9]. In this sense, it has been demonstrated recently that different behaviour are obtained depending of the cleaning sequence order. Reversing the conventional order of the HCl-HF etch, Losego [10] discovered a nearly complete cessation of oxide growth. Ga-polar surfaces receiving a final treatment with concentrated HCl, resisted to MgO growth by MBE (under conditions of low Mg flux and high substrate temperatures). It has been shown that an HCl treatment left a Cl contamination of approximately one monolayer, thus decreasing notably the deposition rate of MgO. This curious phenomenom has been successfully used to selectively pattern epitaxial oxide structures that could be used as mask for plasma etching or dopant implantation for example.

In his work, Losego also showed that the interface quality can be in part determined by the cleaning procedure. He has observed that the leakage current through a GaN/CaO/MgO structure is dominated by Frenkel-Poole defect-assisted tunneling if the GaN is exposed to the HCl/HF etch. Through evaluating several other wet chemistries, he showed that a treatment consisting of a 1:1 $HCl:H_2O$ etch followed by a buffered HF etch (1:6 $HF:NH_4F$) led to a reduction in leakage current with a concomitant change in the leakage mechanism, from Frenkel-Poole to field emission by the Fowler-Nordheim mechanism. This change in the mechanism implies an improvement in the interface quality of the CaO/GaN structure, presumably brought about by some change in the GaN surface by the modified etching procedure.

Moreover, it is important to note that GaN and AlN react differently to the different treatment, the oxygen reduction being lower for AlN compared to GaN, probably due to the larger bond strength of the Al-O bond relative to Ga-O. This is very important to take into account for the ohmic contact formation to AlGaN/GaN. The polar face has also to be taken into account since different results have recently been reported on these faces.

Concerning the stoichiometry, it is generally verified that GaN surfaces are Ga-rich, however this behaviour is not well understood and nowadays still unexplained. Common methods to address Ga-rich surfaces are annealing under nitrogen or ammonia (N_2 or NH_3) atmospheres. Usually any sputtering method performed either at room

temperature or at elevated temperature affects the GaN surface, inducing an increase of the Ga content. This was explained by a slight surface oxidation during sputtering. It was reported in the literature that annealing in N_2 or NH_3 atmosphere helps to achieve a stoichiometry near to unity. However recently Craft [11] performed such experiments on n- and p-type GaN and noted no effect on n-type but effectively observed a decrease in the Ga:N ratio of p-type as a function of temperature.

As received, n- and p-type materials already present differences. It has been reported that the p-type GaN surface has around 1 nm of Ga_2O_3, by contrast to the case of n-type and undoped sample, in which submonolayer quantities of oxide and hydroxide contamination were found. It is believed that this additional surface oxidation of p-type GaN surfaces is due to the dopant activation anneal necessary in the processing of Mg-doped GaN films. Additionally, King suggested [7] that the p-type GaN surface may be more prone to oxidation than n-type GaN, as the valence band lies at a higher energy, in close alignment with the energy of OH- ions in aqueous solution.

Summarizing, the removal of the native oxide and contaminants is of particular importance for III-nitrides, to achieve a clean surface to realize high quality interfaces. However, nowadays, several groups are still searching solutions to obtain contaminants free and clean surface.

6.2 III-N ohmic contacts formation

We have studied the ohmic contact formation on n-implanted GaN and non-doped AlGaN. The formation of an ohmic contact in these layers is particularly interesting for MOSFET and HEMT fabrication. To maximize the efficiency of the ohmic contacts, the contact resistance needs to be the lowest possible and thus process has to be optimized. However, between these materials, the involved mechanism for the ohmic contact formation is different.

In general, making low resistance ohmic contact is difficult for WBG materials, especially for p-type. For most devices, ohmic contacts with resistances lower than 10^{-5} $\Omega.cm^2$ are desired. Usually Ti is the key metal in metallization scheme of nitride devices and Ti-based contacts with contact resistances of 10^{-6}-10^{-5} $\Omega.cm^2$ have been demonstrated on both n-type GaN and AlGaN. In GaN, these contacts are found to take advantages of the formation of a thin interfacial TiN layer, which exhibits metallic conductivity, and possess a low work function (~ 3.74 eV).

As for the current conduction mechanism in these ohmic contacts, the large metal-semiconductor barriers diminish the possibility of thermionic emission-governed ohmic contacts to GaN. The alternative mechanism is some form of tunnelling that may take place if GaN is so heavily doped as to cause a very thin depletion region. Tunneling is possible if, due to annealing (typically between 700-900 ºC for tens of seconds), Al and Ti within undergo substantial interaction with each other and GaN. Different works showed that Ti receives N from GaN, forming a metallic layer, while the lack of N on GaN provides the desired benefit of increased electron concentration though N vacancy formation. Aluminum passivates the surface and also possibly reacts with Ti to form $TiAl_x$ stabilizing thus the contact. In some cases, a based bi-layer metal

scheme is also used as cap on top on the Ti/Al to prevent diffusion and oxidation of Ti/Al during the annealing.

To date, most technological studies have been reported either on the Si implantation to GaN [12] or on the ohmic contact formation on as grown n-type GaN [13]. Few works have reported the ohmic contact formation to Si-implanted GaN.

As seen in the previous section, the surface treatment of GaN prior to the metal deposition could have a strong effect on the final performance of the contacts. It must be also considered prior metal deposition.

Both in implanted p-GaN and in AlGaN, achieving pure Ohmic contacts is much more challenging than in n-GaN. In this work, we will describe the results obtained on the first ohmic contacts formation to GaN at CNM, which is useful for both transistor and resonator application.

6.2.1 Contacts to Si-implanted GaN

The transport properties of Si-implanted GaN are much worse than those obtained from epitaxially grown n-GaN films with a comparable carrier concentration. This is generally attributed to the high impurity incorporation (i.e., Mg and Si) and the unrecoverable ion-implanted damage. In addition, due to its refractory nature, implant activation of GaN dopants is much more difficult than in others semiconductors, requiring annealing temperatures above 1500ºC for a complete activation [14]. Post implantation anneals generally used in the fabrication of GaN-based devices are performed at growth temperature (~1000-1200ºC). This temperature is enough efficient to partially activate the Si implants and recover the crystal induced-damage. Nevertheless, even annealing at these significantly reduced temperature, causes severe degradation and loss of N from the surface if it is not protected [15]. This results in a rough surface, which is detrimental for the electrical performances of solid-state devices, especially for field-effect devices as MOSFETs. To reduce these undesirable effects, cap layers such as SiO_2 [15], AlN [16] or Si_3N_4 [17] have been used, even though they are often difficult to remove after annealing.

There are few data available on the correlation of these protection techniques and the electrical performances of final devices. In this sense, we have studied the influence of a protection cap (graphite and SiO_2) during post-implantation anneal on the ohmic contacts properties to Si implated GaN. Ohmic contacts have been fabricated on protected (PR) and unprotected (UP) surface with a Ti/Al bilayer as described in the following section.

Experimental

The starting material was a p-type GaN epilayer grown on a c-plane sapphire substrate, supplied by TDI Inc. The p-epilayer was 6 µm thick, Mg doped (N_a = 1.9×10^{17} cm^{-3}). A high resistivity Zn compensated buffer layer was also grown between the sapphire substrate and the p-layer. A Si^+ implantation at 160 keV and with a dose of 3.0×10^{15} cm^{-2} was performed. The TRIM (transport-of-ions-in-matter) [18] Monte Carlo simulation predicted a 0.2 µm deep implanted region as shown in figure 1, with a suggested doping peak concentration, at the mean projected range, high enough

(~10^{20}cm^{-3}) to assure a sufficiently high concentration in the near surface, even with a few activation percentage of dopant species. Post-implantation anneal with or without protection are then performed in N_2 ambient to activate the implanted Si. The annealing processes consisted in two-step method, first in a low temperature, T=1000ºC, for one minute and then at 1150ºC for a short time as tens of seconds. This combination of implantation and annealing was choosen since it gave the best results. Next, Ti and Al with 35 nm and 115 nm thicknesses were sequentially deposited by sputtering and patterned by lift-off, to form TLM (Transmission Line Method) pattern. This test structure is a standard rectangular structure on ion-implanted material. The lateral isolation is obtained by the n-wells created during Si-implantation in the p-type epitaxial GaN. The gap spacings between the TLM contacts were 5, 10, 20, 40 and 100 μm, respectively. The contacts were then alloyed by RTA (rapid thermal annealing) at 700ºC in Ar ambient.

Characterization

Surface morphology was examined using SEM and the surface roughness of the annealed implanted GaN and ohmic contacts evaluated by an AFM. Additionally, XRD was used to identify any crystalline compounds present at the metal-semiconductor interface formed during the metal annealing. Current-voltage (I-V) measurements on the TLM were carried out at room temperature.

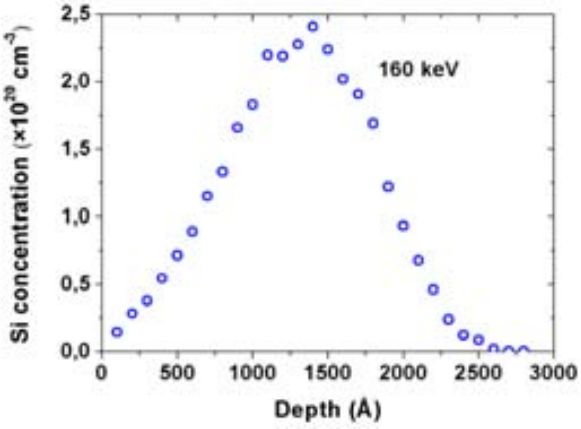


Figure 1. Implantation Profile of Si into the GaN layer simulated by SRIM.

As mentioned before, high temperature post-implantation annealing leads to significant GaN surface dissociation, together with a severe degradation of the surface. The morphological effect of implanting and annealing can be seen in the AFM images shown in figure 2. The roughness value for the received material was very low, less than 1 nm rms. After implantation, the surface was not so much degraded, with a rms roughness value around 1.5 nm (figure 2(a)). By contrast, during the post-implantation annealing with or without protection, roughness increases substantially. The unprotected sample resulted in a RMS roughness around 37 nm, as shown in figure 2(b), with a high density of pits due to nitrogen loss. Graphite based caps was successfully used for SiC [19] and similar results were expected on GaN. However, as shown in figure 2(c), the GaN surface was seriously damaged. The graphite (baked photoresist) reacted with the implanted GaN at elevated temperature and was impossible to remove, even after various O_2 plasma etching processes, leading to a RMS roughness of 126 nm. The best

results were obtained with a SiO_2 cap layer (figure 2(d)), with a very low pit density. In this case, the post-implantation anneal have not resulted in such surface roughness increase, exhibiting a RMS value of 13 nm. However this no-negligible variation compared with the non annealed surface (1.5 nm) could be explained by the different thermal coefficients of expansion between GaN and SiO_2 thus generating stress in the GaN layer, and resulting in increased roughness.

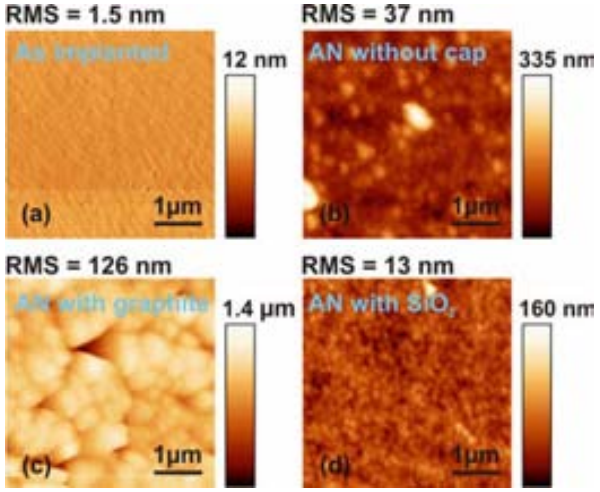


Figure 2. AFM images of the Si-implanted GaN (a) as implanted (b) annealed without cap (c) annealed with graphite cap (d) annealed with SiO_2 cap.

After removing the SiO_2 cap from PR sample, a 150 nm Ti/Al bilayer (35/115 nm) was deposited both on protected and unprotected samples and annealed at 700 ^oC. SEM images of the annealed Ti/Al on Si-implanted GaN and annealed without or with cap, are shown in figure 3.

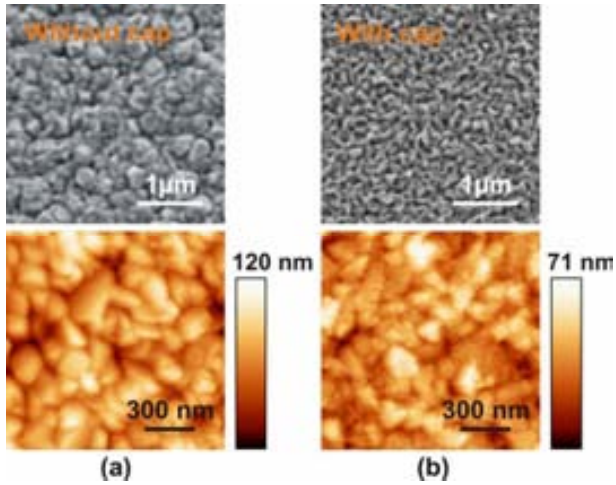


Figure 3. SEM and AFM images of the metal bi-layer alloyed at 700ºC for the Si-implanted GaN annealed (a) without cap (b) with cap layer.

Again, the metal contact of the sample annealed with protection showed smoother surface morphology than the one annealed without the SiO_2 cap. Ti/Al

contacts are usually very rough, in GaN as well as in other semiconductors such SiC [20, 21]. This roughness mainly depends on the annealed temperature and is usually attributed to excess of Al and/or to its tendency to ball-up/oxidize for temperatures higher than 600ºC. On the other hand, Al and Ti react themselves forming different Al-Ti alloys. SEM images have not revealed appreciable Al spreading, hence concluding that the Al-Ti alloy stick together. However the granular structure on the unprotected sample is clearly more visible than in protected sample, showing a clear correlation between the rms roughness value of the annealed Ti/Al contacts and the initial presence of pits from the GaN surface.

Specific contact resistance was extracted by measuring the resistance vs. distance between the four-point transmission line method (TLM) patterns, shown in the inset of figure 4. After metal alloying at 700ºC in Ar ambient for 90s, all the measured I-V characteristics showed that contacts become ohmic. Linear plots were obtained for both the implanted GaN without and with SiO_2 cap. The average values of the sheet resistances of the implanted GaN for both the unprotected and protected samples, were 119 and 428 Ω/□. These values correspond to resistivity (ρ) of 2.38×10^{-3} and 8.56×10^{-3} Ω.cm. The lower values of the sheet resistance for the unprotected sample when compared with the protected one are consistent with the higher N vacancies expected in the unprotected one, thus resulting in higher concentration of donors. The good fitting of the resistance variation between the pads vs. their distance, shown in figure 4 for the protected sample, indicate the good contact quality. However, we have observed a slightly higher dispersion on the extracted R_{sh} value for the protected sample. The exact reason for this is not completely understood but we believe that is related with the different thermal coefficients of expansion of GaN and SiO_2 cap layer resulting in stresses and thus roughness increase after post-implantation annealing.

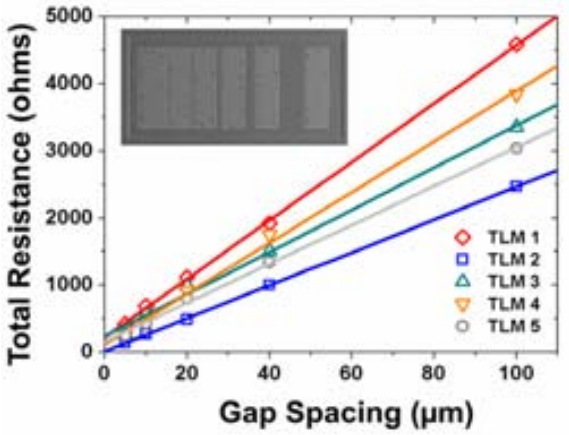


Figure 4. Total resistance as function of the gap spacing for different TLM structures. Inset: SEM image of the TLM structure used to evaluate the ρ_c.

The specific contact resistivity extracted from these measurements revealed a clear dependence on the fact of having a protection cap or not. For one side, protected sample has shown a reduced contact resistance in the range from 1.1 to 2.8×10^{-5} $\Omega.cm^2$. This contact resistance value extracted was very uniform as shown in figure 5. The uniformity of the value seems to correlate well with the uniform surface of the Al-Ti alloy after the contact anneal.

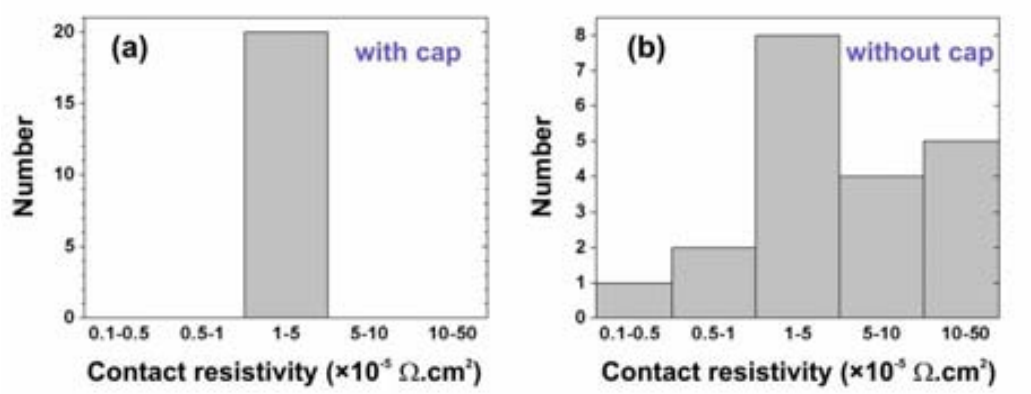


Figure 5. Statistical repartition of the ρ_c for the Si-implanted GaN annealed (a) with cap (b) without cap layer.

However, a reduced roughness of the Ti/Al contacts does not guaranty a good electrical contact at all. We suggest that the key point here is the modification of the interfacial properties between deposited metal and GaN surface. These reactions are much more uniform for PR sample due to its smoother surface. A TiN formation layer is likely more easily formed on this kind of surface [22].

In contrast, unprotected sample exhibited much more dispersion on the contact resistance extracted. In fact, we measured ρ_c comprised between 4×10^{-4} and 4.2×10^{-6} $\Omega.cm^2$, with some devices displaying lower contact resistance than the average from protected sample. It is worth mentioning that some of the as-deposited (before the 700 ^oC RTA contact anneal) unprotected contacts exhibited ohmic-like behaviour and contact resistivities in the range of $\sim 1 \times 10^{-4}$ $\Omega.cm^2$.

These results imply that the surface barrier potential was lowered after implantation, thus allowing relatively easy passage of electrons and ohmic-like behaviour for some of the non-alloyed Ti/Al contact. We explained these results as a consequence of the damage due to Si implantation. It has been demonstrated that induced damage in nitride materials may take various forms, leading to changes in their electrical properties [23]. Previous works reported that surface treatments, and in particular plasma-based etching, can significantly improve the quality of ohmic contacts to n-type GaN [24,25]. Si implantation, as well as plasma etching, produces Nitrogen vacancies on the surface, which is desirable for the improvement of contact resistance. However, the implantation also causes crystalline defects, which can degrade the film quality and the contact resistance. During post-implantation annealing, part of the crystal damage is recovered. Thus, contact improvement could be obtained only when the treatment is well controlled and does not cause more damage that the produced benefits. For this reason, only etching or cleaning techniques, which induced-crystal damage is easier to control than the implantation ones, have been used to improve the contact resistance with much more reproducibility.

To verify this, a reported successfully Ti/Al metal scheme was chosen due to its low work function [25-28]. Ti helps to improve the adhesion and reacts easily with N forming a TiN interface often even only after deposition [22]. The formation of TiN at the metal/GaN interface results in the generation of N vacancies, and, is often used to improve the ohmic contact resistivity by the creation of an heavily doped GaN surface. Moreover Ti/Al ratio of 1/3 is commonly reported, to promote the formation of Al_3Ti

alloy during annealing, also known to improve the thermal stability due to its higher resistance to oxidation than either Al or Ti [28].

The crystal structure of thin films was determined by x-ray diffraction (XRD) measurements. The analyses of sample structure and composition were carried out both in the θ–2θ Bragg Brentano geometry using a Rigaku diffractometer which has a focused monochromatic Cu Kα1 rotated source with radiation λ= 1.54 Å, and using a Bruker AXS GADDS. This system is equipped with a 2D X-ray detector and allows the examination of a wide range of reciprocal space. XRD measurements confirmed the presence of Al_3Ti for unprotected and protected samples. However, no evidence of the formation of TiN-rich interface was detected. From figure 6, we can infer that for unprotected sample, a weak peak of the Al_3Ti phase appears together with remaining peaks of Al and Ti. This indicates that the thermodynamic reaction of species involved seems to be more difficult on the rougher surface. For the rougher surface, the Ti thin layer has a poor coverage, especially in the vicinity of the GaN pits. This results in Al areas without Ti below. During alloying, this Al alone melts and balls-up, as showed in figure 3(a), resulting in a granular surface, which is more prone to oxidation. Moreover, part of this Al is probably oxidized, as observed essentially at the edges of the samples. In contrast, for PR, the Al_3Ti peak is slightly stronger and only a small remaining peak of Al is observed. These results suggest that Al_3Ti alloy formation also depends of the GaN surface morphology.

The formation of TiN at the interface is reported to reduce effectively the barrier height [28]. The mechanism is that the formation of TiN creates N vacancies in the GaN surface during the contact anneal that act as donors, enhance the doping level at the interface, then reducing the contact resistance. Since we have not detected TiN, we believe that our measurement may be not sensitive enough to detect the formation of a thin TiN layer at the interface. First, according to the literature the interface TiN layer should be 4-6 nm thick [28], as revealed by TEM analysis and likely of not very good crystalline quality. In addition, the θ–2θ reported TiN (111) reflection [ICDD-PDF #65-0565] is expected at 36.7º. In this angular region there is a strong background tail associated to the ion implanted damaged top layer of the GaN, which could hinder the observation of any weak spike from any thin layer on top of the implanted GaN.

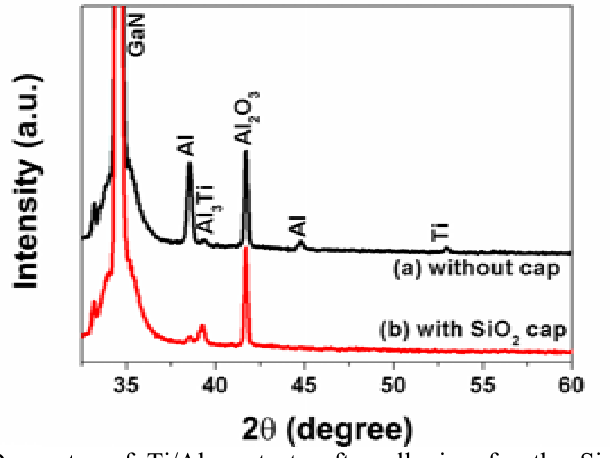


Figure 6. XRD spectra of Ti/Al contacts after alloying for the Si-implanted GaN annealed (a) without cap (b) with cap layer.

A correlation between the electrical performance of the contact and the compounds formed at the interface after the different surface treatments has been found. Nitrogen vacancies randomly created on the unprotected GaN after post-implantation annealing should explain the dispersion on the extracted ρ_c when compared with the absolutely uniform value extracted for the sample protected with the SiO_2 cap. Moreover, during metal annealing, we argue that a smoother surface before metals deposition is beneficial to improve the alloy formation.

Summary

The effect of post-implantation annealing caps on the contact resistance of Ti/Al ohmic contact to Si-implanted GaN has been investigated. P-type GaN has been implanted using a Si ion dose of 3.0×10^{15} cm^{-2}, resulting in a simulated n-type well Gaussian profile of 0.2 μm depth, with a doping peak of 10^{20} cm^{-3}. After implantation, a protective cap (SiO_2 and graphite) has been used in some of the samples to avoid the nitrogen evaporation from the surface. The post-implantation N_2 annealing temperature was 1150 ºC. Graphite has been found to be unpractical since this cap reacts with the GaN surface, resulting in a non-removable intermixing layer. Samples with a SiO_2 protective cap have revealed a much smoother surface with a RMS comparable to the starting material, with a RMS value of 13 nm. After depositing the metal stack Ti (35nm)/Al (115 nm), contact annealing (700 ºC for 90s in Ar) was performed to improve the metal-semiconductor adhesion and reduce the contact resistance. We have found that protection during post-implantation annealing is very important to obtain a good uniformity on the contact performance. During this process, the formation of Al_3Ti alloy has been observed by XRD. No TiN formation has been observed with our equipment. However, the fact of having much more dispersion, as well as lower contact resistance for some of the samples (in the range of $4x10^{-6}$ Ωcm^2) for the unprotected samples, makes us to suggest that the contact resistance mechanism is related with the formation of N vacancies on the GaN surface during both the post-implantation and contact annealing .

6.2.2 Contacts on AlGaN

In general, making low resistance ohmic contact is difficult for WBG materials, especially for p-type. For most devices, ohmic contacts with resistances lower than 10^{-5} $\Omega.cm^2$ are desired. Usually Ti is the key metal in metallization scheme of nitride devices and Ti-based contacts with contact resistances of 10^{-7}-10^{-5} $\Omega.cm^2$ have been demonstrated on n-type GaN. In GaN, these contacts are found to take advantages of the formation of a thin interfacial TiN layer, which exhibits metallic conductivity, and possess a low work function (~ 3.74 eV). However, achieving low contact resistance on AlGaN is more difficult, due to the Schottky barrier height of many metals on AlGaN being larger than 1 eV. The best specific contact resistivity on AlGaN is usually several orders of magnitude higher than on GaN. Until now, the same metallic scheme Ti/Al-based was transferred to AlGaN for achieving ohmicity. However the formation mechanism is not as easy as in GaN and until now some doubts subsist concerning about the exact involved mechanism. It is believed that TiN formation during annealing leads to a reduction of the barrier height and thus allowing carrier transport from the Schottky-Mott theory. N-vacancies in the GaN layer have been also reported to create a large band bending and thus allowing carrier transport through tunnelling mechanism.

Moreover, the cleanings have different effects on the AlGaN compared to the GaN surface. Therefore it is still a challenge to develop reliable and low ohmic contact resistivity on AlGaN and try to understand the involved mechanism in Ohmic contact formation.

In this section, we investigate the annealing effects on electrical characteristics and surface morphology of the contact. The samples were submitted to different annealing steps.

Experimental

The AlGaN/GaN heterostructure was grown by QinetiQ in an MOCVD system. The sample structure consisted of 28 nm of undoped $Al_{0.28}Ga_{0.72}N$ on 1.2 µm of GaN, grown on an (0001) c-plane oriented sapphire substrate. The nominal carrier concentration varied from 8.0×10^{12} to 9.9×10^{12} cm^{-2}, and the sheet resistance from 641 to 717 Ω/sq.

A Ti/Al/Ti/Pt metallic scheme was used for ohmic contact formation with thicknesses of 20/80/20/50 nm respectively and was sequentially deposited by sputtering and patterned by lift-off, to form rectangular TLM (Transmission Line Method) pattern. No mesa isolation was performed by etching. The gap spacings between the TLM contacts were 20, 15, 10, 5 and 2 µm respectively. The first sample was annealed in an halogen lamp RTP furnace while another one in a conventional furnace, under flowing argon gas environment at temperature around 860ºC for 1 minute. The specific contact resistivities and sheet resistance, ρ_c and R_{sheet}, were determined from the plot of the measured resistances against the spacings between the pads.

Characterization

Figure 7(a) shows the I-V characteristics of sample 1 after a first annealing in a halogen lamp RTP furnace at 870ºC for 1 min in Ar ambient. The obtained contacts remained rectifying. As comparison, figure 1(b) shows another sample with the same metal scheme after a first annealing in a RTP furnace at 860ºC for 1 min in Ar ambient. The difference obtained from these measurements is not well understood, but could be easily explained by the fact that depending of the sample position in the furnace, the temperature can vary by around 50ºC. However, at 800ºC in a conventional furnace it is usually observed truly-ohmic behaviour in Ti/Al based-scheme contacts. The only difference between the two processes is the UV radiation heating from tungsten lamps to heat the sample that provides a more uniform heating and cooling at the surface and thus reducing possible gradients that could induce defects of failure such as dislocations. It has to be noted that UV radiation is often used in GaN etching due to induced photochemical effects. Here it seems that induced defects during annealing in a classical furnace could probably help to obtain easily ohmicity in AlGaN contacts.

The specific contact resistivity extracted from these measurements was very uniform, comprised between 1.2 and 3.3 x 10^{-3} Ω.cm^2. This value is similar to those reported in literature, however it could be improved by adjusting better the Al/Ti/metal barrier/Pt (here Ti) ratios.

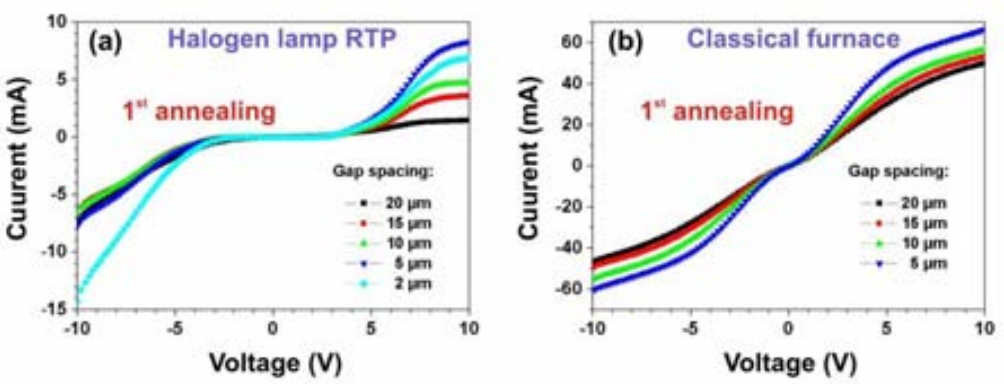


Figure 7. I-V characteristics of (a) sample 1 annealed in a halogen lamp RTP, (b) sample 2 annealed in a classical RTP furnace.

To understand the mechanism of ohmic contact formation, x-ray diffraction (XRD) measurements were performed. The crystal structure of thin films was determined by x-ray diffraction (XRD) measurements. The analyses of sample structure and composition were carried out both in the θ–2θ Bragg Brentano geometry using a Rigaku diffractometer which has a focused monochromatic Cu Kα1 rotated source with radiation λ= 1.54 Å, and using a Bruker AXS GADDS. Figure 8 shows the XRD spectra of the reference sample (without metal), the sample with the as-deposited metal film on AlGaN, and the samples 1 and 2 annealed in a halogen lamp RTP and classical RTP furnace, giving respectively rectifying and quasi-ohmic contacts.

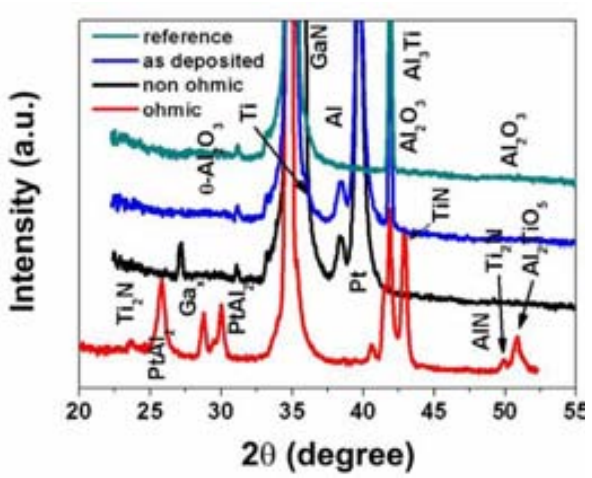


Figure 8. XRD spectra of reference sample, as deposited, non ohmic and quasi-ohmic contacts for the Ti/Al/Ti/Pt scheme.

In the reference sample, it can be seen both the GaN and/or AlGaN peaks and the Al_2O_3 peak. This later peak can be due either to the substrate or to a possible native oxide in the AlGaN surface. In the as deposited sample, different peaks corresponding to Al and Pt metals can be seen. In the non-ohmic sample, annealed in a halogen lamp RTP, the same peaks corresponding to the metals are still present, but curiously the Al_2O_3 peak has disappeared. This is actually not well understood but UV exposure in N_2

atmosphere could probably help to remove or deteriorate a possible native oxide. That is important here is that no alloy was created during the annealing, thus explaining the results obtained in the electrical measurements. By contrast, in the ohmic sample, annealed in a classical furnace, many new peaks have appeared. TiN, AlN, Ti_2N and $PtAl_2$ phases have been detected. It is also interesting to note that the peaks corresponding to Al and Pt have disappeared, clearly indicating that they have been consumed in alloying reactions. The Al_2O_3 peak is still present but has probably been degraded as it can be seen in the much more strong tail. Curiously, the GaN peak is much thinner, indicating that the closer AlGaN peak has probably been deteriorated.

These different results indicate that performing annealing in a typical furnace with nitrogen ambient is much proper than in a RTP with radiation scheme. The ohmic contact formation, which requires diffusion-based processes between metals, seems to be easily achieved in a conventional furnace than in a radiation-based one.

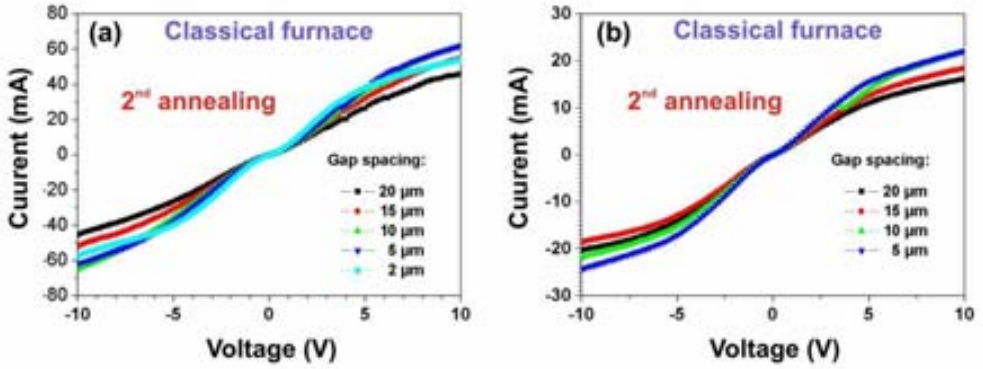


Figure 9. I-V characteristics of (a) sample 1 and (b) sample 2 after a 2nd annealing in a classical RTP furnace.

A second annealing step in the conventional furnace has been performed for the two samples. Electrical measurements have been realized to see possible improvements. Figures 9(a) and (b) show the I-V characteristics of sample 1 and 2 after a second annealing in a RTP furnace at 870ºC for 1 min in Ar ambient. The level current attained for the sample 1 after this annealing is similar and slightly superior to the one achieved in sample 2 after the 1st annealing. As expected from this observation, the specific contact resistivities extracted from these measurements were slightly lower than those obtained after the 1st annealing of sample 2, comprised between 9.8×10^{-4} and 2.3×10^{-3} $\Omega.cm^2$. Curiously, for sample 2, a second annealing resulted in lower current level and a lower saturation current, as it can be seen in figure 9(b). This degradation clearly indicates a reduction of the carrier injection efficiency. In this case, ρ_c was comprised between 1.8 to 8.7×10^{-3} $\Omega.cm^2$.

Surface morphology and surface roughness of the annealed AlGaN and metallic contacts were examined using optical (OM), atomic force (AFM) and scanning electronic microscopy (SEM). Optical images in figure 10 show the contact edges of as deposited and annealed samples. It seems that annealing in a halogen lamp RTP furnace is not beneficial to obtain well defined edges.

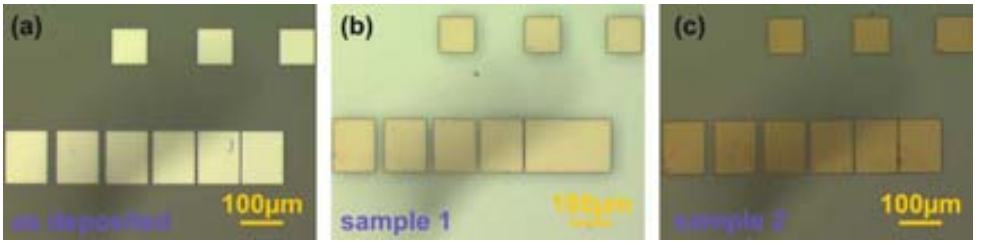


Figure 10. Optical images showing the line edge definition of (a) as deposited, (b) sample 1 after annealings (c) sample 2 after annealings.

However, the acuity in achieving well defined and sharp edges is of particular importance for obtaining small geometry devices. As deposited (figure 11(a)), the metallic interface is sharp and there is little intermixing. After annealing, it can be seen in figures 11(b) and (c) that some metals have dripped on the AlGaN surface. Sample 1, which was irradiated, seems presenting lower acuity that could be problematic for thin gap, as observed in the optical image. However, in both cases, the lateral flow remained lower than 1 µm, which is a good result. Probably the high melting temperature of Pt has helped to minimize this spatial flow. However, in future work, special attention will be given to this topic in order to reduce it as much as possible.

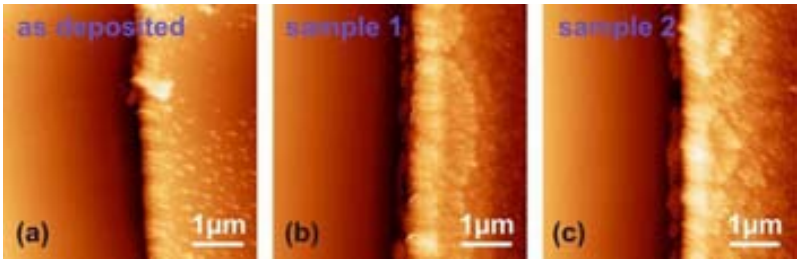


Figure 11. Metallic contact edges of (a) as deposited, (b) sample 1 after annealings and (c) sample 2 after annealings.

The GaN (AlGaN) surface seems not affected but since sputtering, photoresist or the chemical photoresist etchant during the lift-off may slightly modify the GaN surface, AFM measurements were performed and can be seen in figure 12. No significant variation was observed after the different steps, the RMS roughness of GaN surface remaining between 1 to 1.2 nm. Only a slight modification of the surface morphology after lift off can be observed on figure 12(b) but was recovered after annealing (figure 12(c)) and identical to the initial surface (figure 12(a)).
Usually Ti/Al-based contacts are very rough in III-nitrides. This roughness mainly depends on the annealed temperature and is usually attributed to excess of Al and/or to its tendency to ball-up/oxidize for temperatures higher than 600ºC. Here, the Ti/Pt scheme used on top of this Ti/Al helps avoiding possible Al oxidation and thus to improve the reaction of Ti and Al.

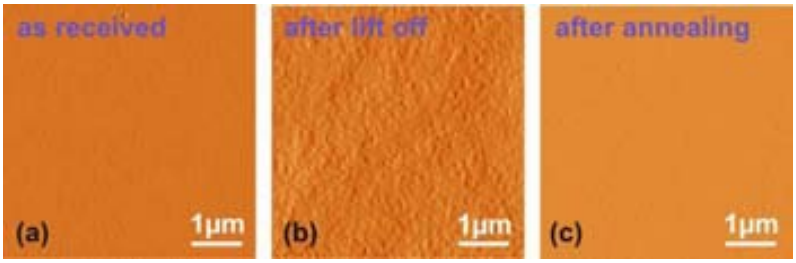


Figure 12. GaN (AlGaN) surface roughness (a) initial sample, (b) sputtered sample and (c) annealed sample.

The surface morphology of the Ti/Al/Ti/Pt metallic scheme was also investigated before and after annealing using AFM and SEM. AFM images of the surface are shown in figure 13. The obtained morphology before (figure 13(a)) and after (figures 13(b) and (c)) the annealing treatments clearly shows difference, the non annealed sample showing pits while the two annealed samples show a more granular surface, probably to melts and balls up. The RMS value before annealing was 4.9 nm and was 5.7 and 6.7 for process 1 and process 2. The peak to peak value was 59.5 for the as deposited sample, indicating that probably Ti is exposed in some areas to the top surface. After annealing, no significant difference was observed between the 2 processes, giving a peak to peak value of 49.6 and 42.9 nm for process 1 and 2 respectively.

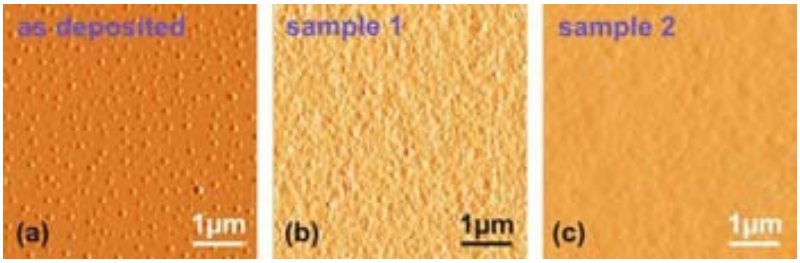
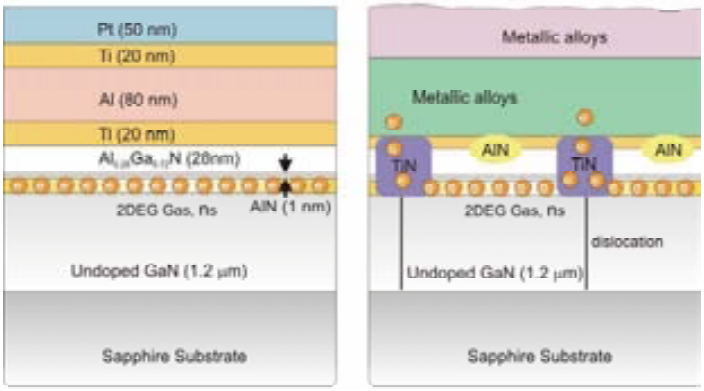


Figure 13. Metallic surface roughness (a) as deposited, (b) sample 1 after annealings and (c) sample 2 after annealings.

The obtained results on the electrical characteristics have motivated us to understand the ohmic contact formation mechanism. It has been recently reported by Wang [29] that TiN islands penetrating through the AlGaN layer are preferentially formed along threading dislocations during metal annealing. Thus TiN helps establishing direct electrical link between the 2DEG and the metal contact. This mechanism is consistent with the electrical results obtained after the different annealings. It could be advanced that annealing in a RTP furnace favours induced-defects formation and especially dislocations formation at GaN/substrate interface. These dislocations originate from the GaN/buffer interface because of substrate/epilayer lattice mismatch and terminate at the AlGaN surface. These dislocations are fast diffusion channels for Ti, and thus favour the TiN islands formation. A schematic of the involved mechanism for the ohmic contact formation is shown in figure 14.



(a) (b)

Figure 14. Schematic of the reaction mechanisms between the metals and semiconductor after annealing and giving the ohmic contact mainly due to TiN formation along dislocations.

These TiN islands could severely degrade the 2DEG if their density is too high thus compromising its electron density. It has appeared that performing a second annealing resulted in degradation of the contact resistivity of the sample 2 while sample 1 shown an ohmic contact similar to the one obtained after the first annealing of the sample 1.

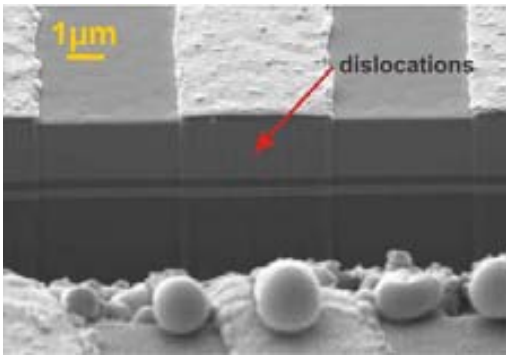


Figure 15. SEM image showing the dislocations below the alloyed contacts.

Figure 15 shows a SEM cross-section of areas with metals forming ohmic contacts. It is clearly observed that dislocations are disseminated along the nitride bulk on the areas where metal is present, confirming the above discussed mechanism.

Summary

The formation of ohmic contacts in AlGaN is not still well understood and appears to be a complex process depending of many factors. Here the effect of metal annealing of the Ti/Al/Ti/Pt contact in different furnaces was investigated. A clear correlation has been found between the electrical results and annealings in different furnace. An annealing step at 860ºC for 1 min was chosen based on literature results and reported as the optimum annealing temperature. Two different annealings were performed in different furnaces for the same temperature and time. Annealing in an RTP

furnace based on a tungsten lamp radiation resulted in rectifying contacts while annealing in a conventional furnace has given truly ohmic contacts. Specific contact resistivity around 10^{-3} $\Omega.cm^2$ was achieved. This value is elevated enough but similar to others reported in literature. It could be improved by adjusting better the Al/Ti/metal barrier/Pt (here Ti) ratios and controlling precisely the TiN formation. This different behaviour can be explained by the difference in defects formation between the 2 used furnaces. In an RTP with radiation, the substrate is heated by radiation from a tungsten source, and a small change in the radiation affects temperature distribution in the substrate. Further, a desired annealing temperature may not be carefully maintained. Temperature fluctuations may occur more severely than in a furnace without radiation scheme. Moreover, possible defects are expected to be mainly formed at the radiated surface. Another possible explanation could be the amorphisation of the substrate, thus resulting in lower defects formation. In the case of a conventional furnace, defects are more easily formed thus explaining the quasi-ohmicity obtained after annealing. It has been recently demonstrated that TiN formation mainly depends of dislocation formation.
Summarizing for the ohmic contact formation in AlGaN/GaN layer, different reactions have to be favoured:
1) $TiAl_x$ alloy that allows stabilizing the contact and prevent the contact structure from balling-up
2) A barrier layer on top of the Ti/Al, to prevent diffusion, minimize lateral flow and possible oxidation of the Al. This usually requires the use of a high melting metal such as Mo, Pt or Au.
3) Favour reasonably the dislocations formation to promote TiN formation by an adequate annealing (temperature, time) and set-up (furnace choice).

6.3 SiO_2 on GaN

Silicon (Si)-based metal-oxide-semiconductor (MOS) devices possess high quality insulating layers of silicon dioxide (SiO_2) grown directly on Si using wet or thermal processes. This high quality oxide and interface play a crucial role in achieving high performance devices, preventing thus efficiently leakage current. Many semiconductor materials with superior electrical properties relative to Si, such as gallium nitride (GaN), do not currently form good semiconductor/insulator interfaces being detrimental for their use on high-frequency or high-power applications.

The ideal insulator for GaN-based devices should exhibit a good chemical and thermal stability because GaN is expected to extend the silicon high temperature operation range. For this reason it should have no mobile oxide traps, low interfacial trap density and a dielectric constant higher than GaN to avoid premature breakdown at low electric fields. A large band offset of conduction and valence bands to provide good confinement of carriers is also a requirement.

Due, to its very well established technology, large band offsets and low leakage current, SiO_2 still remains the general insulator of choice for successful GaN MOSFETs. Other crystalline insulators such as MgO [30], Sc_2O_3 [31] or Gd_2O_3 [32] have recently been investigated since they present ordered interfacial structure resulting in lower interfacial trap density but they also could induce high strain levels favouring thus the defects diffusion at the interface. Although its evident potential applicability, for example in a power switch device, there is much less information available of the

characteristics of the MOS interface on GaN when it is compared with Si or SiC which has been massively investigated.

6.3.1 Experimental details

The MOS structures were fabricated on p- and n-type (0001) 2H-GaN epilayers grown on c-plane sapphire substrates, supplied by TDI Inc. The p-epilayer was 6 µm thick, Mg doped (N_a = 1.9×10^{17} cm^{-3}) while the n-epilayer was 5 µm thick, unintentionally doped (N_d = 2×10^{16} cm^{-3}). A high resistivity Zn compensated buffer layer was grown between the sapphire substrate and the GaN layers. Samples were submitted sequentially to solvent degrease (acetone, isopropanol) and using SiO Etch. Finally, a chemical RCA based cleaning process was performed. A 100 nm thick (t_{ox}) amorphous SiO_2 layer was then deposited by PECVD using either TEOS or silane as source material, both on n- and p-type substrate. Temperature deposition was 380ºC and 400ºC for the silane and TEOS-based process respectively. Table VI-1 summarizes the main parameters used in both processes. Lateral n- and p-type MOS capacitors were fabricated to determine the density of interface traps within the bandgap close to the conduction and valence band, respectively.

Table VI-1. Summary of the silane- and TEOS-based SiO_2 deposition parameters.

Process	Thick. [nm]	Temp.	Pressure	Time (dep. Step)	Flow Rates (sccm)	Others
Silane-based	100	380 ºC	1 Torr	2 min.	20 SiH_4 1000 N_2O 800 N_2	RF power: 250W
TEOS-based	100	400 ºC	9 Torr	17 sec.	1000 O_2 500 TEOS	RF power: 395W

The area of the gate electrode was 0.45 mm^2. Capacitance-voltage (C-V) and conductance-voltage (G-V) measurements were performed in dark using a Keithley K82 system. Quasistatic (C-V) characteristics were probed using the linear ramp voltage sweeping technique in which the charge current is measured instead of the capacitance. The quasi-static capacitance is then calculated from the low frequency current ($C=I/(dV/dt)$) in which a sweep rate of $dV/dt=0.7$ V/s was used. High frequency C-V characteristics were also measured at 10, 100 and 1000 kHz using different signal amplitudes and time stresses. After as deposited (AD) electrical characterization, an annealing (AN) was performed at 800 ºC for 2 min in N_2 ambient as an attempt to improve the electrical characteristics. Surface morphology was examined using optical microscope, scanning electron microscope (SEM) and atomic force microscope (AFM). Secondary-ion mass spectrometry (SIMS) was also used to analyze the depth distribution of chemical elements after the SiO_2 annealing.

6.3.2 Physical and electrical characteristics

Quasi-static C-V curves

Figure 16 shows a typical quasistatic C-V curve for as-deposited (AD) MOS capacitors with silane and TEOS-based SiO_2 on *n*- and *p*-type GaN. The negative flat-band shift observed suggests that fixed positive oxide charges are present in the SiO_2 bulk or at the GaN/SiO_2 interface, being slightly higher for the silane-based SiO_2.

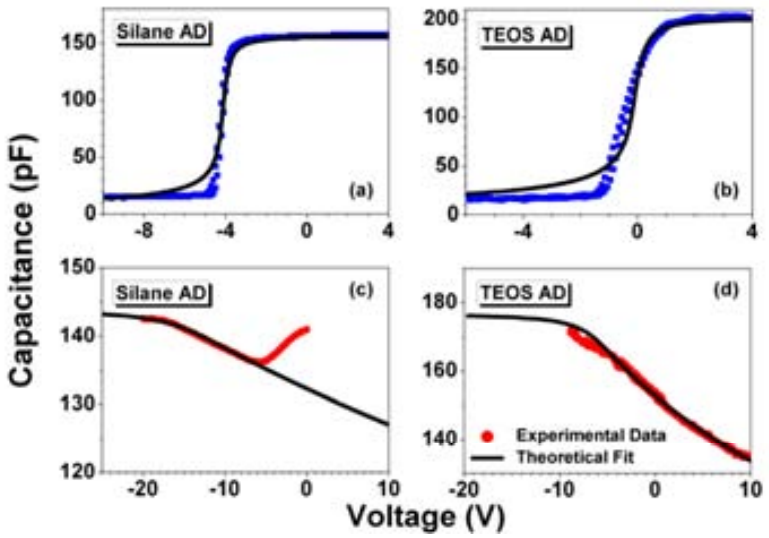


Figure 16. Quasi-static capacitance-voltage characteristics for the as-deposited (a) Silane-based SiO_2 on n-type GaN and (b) TEOS-based SiO_2 on n-type GaN and for the (c) Silane-based SiO_2 on p-type GaN and (d) TEOS-based SiO_2 on p-type GaN.

It was routinely observed a lower accumulation capacitance value (C_{ox}) obtained on the silane-based SiO_2 on n- and p-type capacitors. Profilometer measurements confirmed the homogeneity of our process with a deposited thickness of 100 nm for both, TEOS and Silane. We suggest that this C_{ox} difference would come from a higher dielectric constant value (around 4.9) for AD TEOS–based SiO_2 as previously reported for Si capacitors [33].

After annealing (AN) for 2 minutes in a N_2 ambient at 800 ºC, both *n*-type TEOS AN and silane AN still show negative flat-band voltage shift. For the silane AN, this shift is small but for TEOS AN flat-band capacitance is clearly shifted towards negative values. The C_{ox} value for TEOS AN is now analogous to the silane AN (figure 17). Again, it would be an indication of a change of the dielectric constant which would be also associated with a densification of the TEOS SiO_2 film. Da Silva *et al.* [34] reported the presence of –OH contamination in the oxide layer and they suggested that the increased dielectric constant was due to dielectric polarization of OH molecules in the film. It is well known that SiO_2 deposited from TEOS at low temperature results in silanol (Si-OH) incorporation due to the large size of the TEOS molecule. On the contrary, silane chemistry only requires the elimination of small hydrogen molecule. It is reasonable to suggest then that after annealing the contamination coming from the C-H and O-H is reduced, thus decreasing the dielectric constant value.

Moreover, it is also well known that Mg-doped GaN grown by MOCVD inherently contains a huge amount of hydrogen (H) atoms which passivates Mg acceptors. During the PECVD deposition, H incorporation is also possible, since SiO_2 films use source gases that have hydrogen related bonds, and thus H migration into GaN can occur. It was theoretically predicted that H can be as a deep donor in p-type GaN, and enhances the diffusion of defects [35]. For this reason, an annealing is usually performed in nitrogen ambient to remove this undesired H both in GaN and dielectric layers. However, the concentration of H impurities still remains elevated in p-type nitrides after conventional annealing [35].

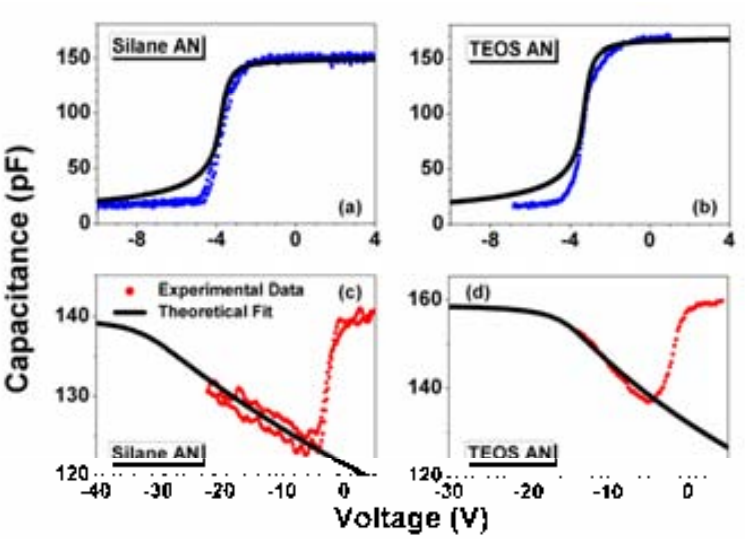


Figure 17. Quasi-static capacitance-voltage characteristics for the annealed (2 min at 800ºC in N_2) (a) Silane-based SiO_2 on n-type GaN and (b) TEOS-based SiO_2 on n-type GaN and for the (c) Silane-based SiO_2 on p-type GaN and (d) TEOS-based SiO_2 on p-type GaN.

Silane-based SiO_2 on *p*-type samples shows a rather uncommon characteristic for a wide band gap MOS capacitor. It is well known that GaN or SiC MOS structures generally not show surface inversion at room temperature, because the generation rate of the minority carriers is extremely low (n_i is around $10^{-10}cm^{-3}$), thus resulting in the deep depletion feature in the CV characteristic. Nevertheless, an inversion characteristic seems to take place, as it can be inferred in the quasi-static curve figure 16(c). This inversion characteristic seems ever more evident after the N_2 annealing. Huang *et al.* [36] and Nakano *et al.* [37] already reported a surface inversion in a *p*-type GaN capacitor, without the presence of minority carriers source. Nakano *et al.* [37] attributed this behaviour to dislocations, acting as recombination centers and thus helping to the formation of a surface inversion layer at the interface. They also attributed the decrease of the inversion capacitance with frequency to incomplete ionization of Mg dopants, which can follow the voltage modulation when the C-V frequency is decreased.

High frequency C-V curves and interface state density

The high frequency (higher than 10 kHz) C-V curves of the as deposited and annealed samples are shown in figures 18 and 19 for the n- and p-type capacitors respectively. Although it is not reported here, the accumulation capacitance presents a much more important decrease at frequencies higher than 10 kHz, especially at 100 kHz, compared to the Quasi-Static C-V value. This situation reminds a typical series resistance effect commonly observed in MOS structure [38].

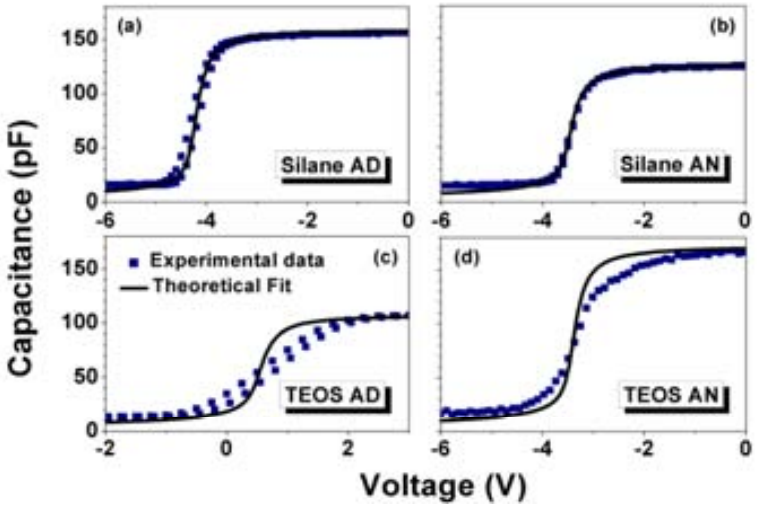


Figure 18. High frequency capacitance-voltage characteristics of MIS capacitors for the n-type GaN/SiO_2 capacitors with (a) as deposited silane-based SiO_2, (b) annealed silane-based SiO_2, (c) as deposited TEOS-based SiO_2, (d) annealed TEOS-based SiO_2.

An estimation of the interfacial trap density has been determined from the C-V deviation from ideal characteristics (figures 18 and 19), by means of the Terman method [39] and the conductance losses. The interface state density (D_{it}) spectra within the bandgap close to the valence band and conduction band, for the silane- and TEOS-based SiO_2 capacitors implemented on n- and p-type GaN substrates, respectively, is presented in figures 20 and 21.

Fon *n*-type GaN (close to the conduction band), an interface state density of 1.1×10^{11} $cm^{-2}.eV^{-1}$ and 6×10^{11} $cm^{-2}.eV^{-1}$ has been extracted at $E_c–E_T = 0.2$ eV for silane AD and TEOS AD, respectively. After annealing, the interface trap density of *n*-type silane AN is reduced to 6.1×10^{10} $cm^{-2}.eV^{-1}$, clearly indicating an improvement of the interface characteristics after the thermal treatment. On the contrary, the TEOS AN D_{it} is increased to 9.2×10^{11} $cm^{-2}.eV^{-1}$, revealing a deterioration of the interface. This trend is corroborated with the conductance-voltage measurements. It was observed lower conductance losses for silane AN SiO_2, while theses losses are increased for TEOS AN. For *p*-type GaN (close to the valence band), an interface state density of 1.1×10^{11} $cm^{-2}.eV^{-1}$ and 1×10^{12} $cm^{-2}.eV^{-1}$ has been extracted at $E_T–E_V = 0.2$ eV for silane AD and TEOS AD, respectively. After annealing, the D_{it} is slightly increased to 4.2×10^{11} $cm^{-2}.eV^{-1}$ for silane AN, while for the TEOS AN, D_{it} was reduced to 2.9×10^{11} $cm^{-2}.eV^{-1}$, revealing an improvement of the interface.

Summarizing, the deposited silane-based SiO_2 presents the best interfacial properties in term of low D_{it}, with a symmetric interface state density, which is slightly higher close to the valence band. The TEOS-based SiO_2 interface state density is markedly asymmetric. D_{it} is lower near the conduction band in the TEOS AD but lower near the valence band in the silane AD. Such an asymmetric interface state density, with higher values near the valence band is in agreement with Huang [36].

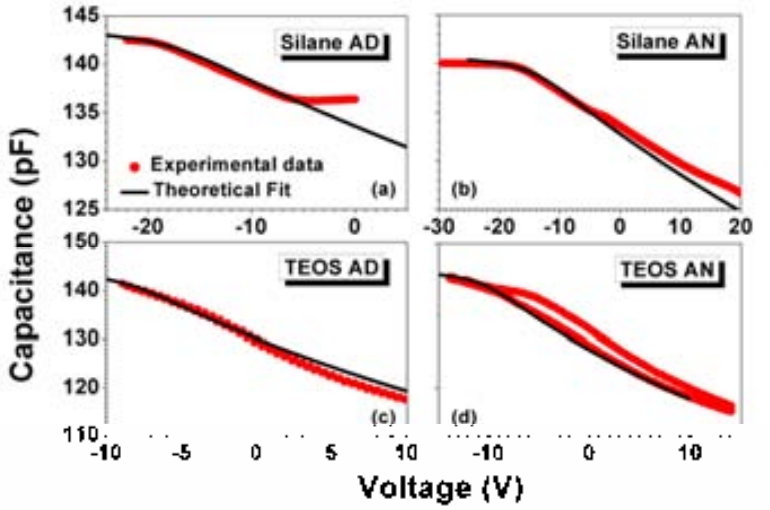


Figure 19. High frequency capacitance-voltage characteristics of MIS capacitors for the p-type GaN/SiO_2 capacitors with (a) as deposited silane-based SiO_2, (b) annealed silane-based SiO_2, (c) as deposited TEOS-based SiO_2, (d) annealed TEOS-based SiO_2.

We suggest that this difference between conduction and valence band may be due to the difference in starting material quality between *n*- and *p*-type. The p-type usually presents larger number of dislocations, higher surface roughness due to the required annealing thermal budget required to activate the Mg dopants during or after the growth. Moreover, it has been reported [40] that any plasma deposition method induces inevitably a thin amorphous GaO_x layer, which almost certainly contributes to an increase somehow of the density of interface states.

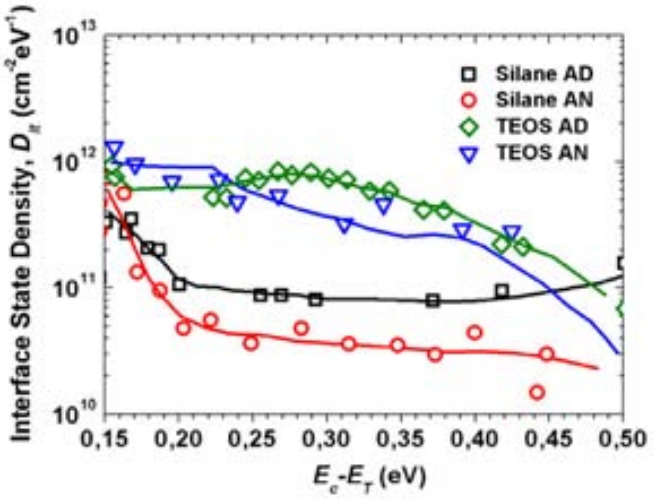


Figure 20. Interface state density for the n-type GaN/SiO_2 capacitors for the as deposited and annealed Silane- and TEOS-based SiO_2.

The interfacial traps in the upper half of the band gap are believed to be acceptor like in nature and these states are responsible for the scattering of free carriers in *n*-channel devices. For an *n*-channel MOSFET only the upper band gap acceptor states must be

considered since the lower band gap donor states are neutral when the inversion channel is formed. For this reason *n*-type capacitor characteristics have attracted more attention. A rough comparison with previously reported D_{it} values could be done. Nevertheless it should be considered that the D_{it} value depends on the extraction method and in the experimental set-up. Bae [40] reported a value for the D_{it} around (2-9)×10^{11} $cm^{-2}.eV^{-1}$ using a Ga_2O_3/SiO_2 dielectric scheme. Lin [41] reported a value of 5.9×10^{10} $cm^{-2}.eV^{-1}$ (at 0.4 eV from the conduction band) for an annealed sample using a $GaO_xN_y/$ SiO_2 stacked dielectric strategy. Huang [36] has reported the lowest value, around 3.8×10^{10} $cm^{-2}.eV^{-1}$ (at 0.2 eV from the conduction band) for an annealed TEOS-based SiO_2. Therefore, values reported here are comparable to the state of the art, especially for the annealed silane-based SiO_2.

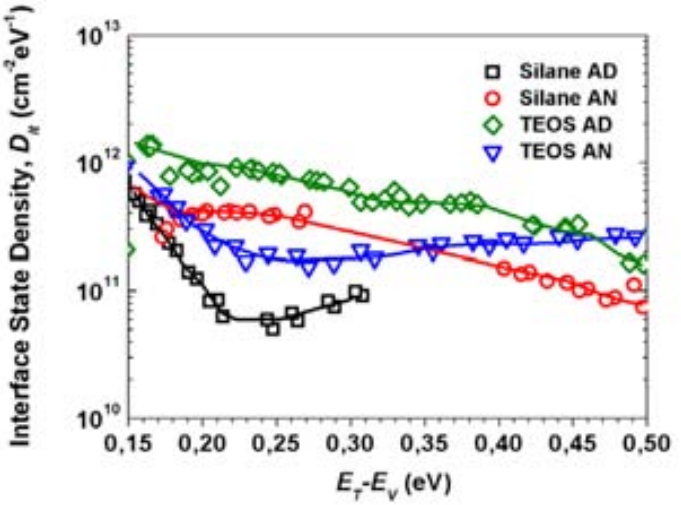


Figure 21. Interface state density for the p-type GaN/SiO_2 capacitors for the as deposited and annealed Silane- and TEOS-based SiO_2.

AFM

It was observed that for both silane and TEOS the surface morphology becomes rougher after annealing. Figure 22 shows AFM scans of the *n*-type and *p*-type SiO_2/GaN after anneal. For the *n*-type samples, the surface morphology of the SiO_2 silane AN and TEOS AN are similar. They present a relatively low mean roughness (rms) of 2.9 and 2.6 nm, respectively. These values are higher than before annealing where the rms was 0.74 nm and 0.86 nm, for Silane AD and TEOS AD, respectively. For the *p*-type GaN samples the surface morphology is significantly rougher than for *n*-type. Before annealing it was extracted a rms of 1.35 nm and 1.68 nm for Silane AD and TEOS AD. After annealing, it was measured a rms of 3.7 and 18 nm for Silane AD and TEOS AD, respectively. As it can be seen in figure 22 (d), many island-like aggregations up to 1 μm diameter and 200 nm thick can be observed on the surface of the TEOS-based SiO_2 AN. These islands remained after many cleaning processes including an O_2 plasma.

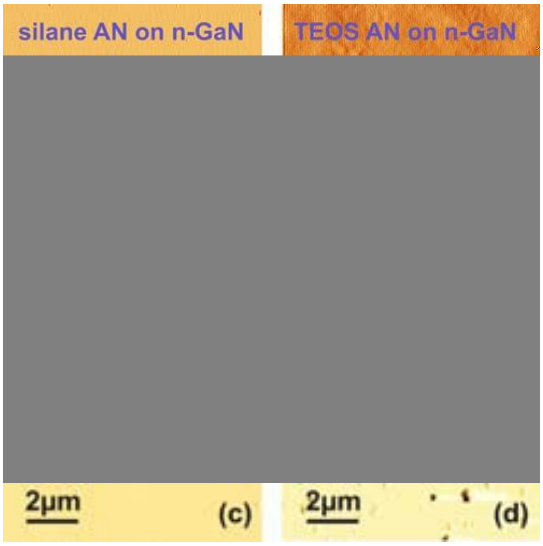


Figure 22. AFM images of the SiO_2 (a) silane-based on n-GaN, (b) TEOS-based on n-GaN, (c) silane-based on p-GaN, (d) TEOS-based on p-GaN.

Nakano *et al.* [42] reported similar islands in the early stage of thermal oxidation of GaN:Mg. and were found to be composed of Ga and O. They also found a high density of microholes in the GaN surface related to dislocations formed during the annealing. Lin et al. [43] also reported some droplets in the oxidized *n*-type GaN surface at 800°C suggesting a possible atom out-diffusion mechanism.

XRD

After annealing, an x-ray diffraction (XRD) measurement was performed to determine any crystalline change. The analyses of the sample structure and composition were carried out both in the θ–2θ Bragg Brentano geometry using a Rigaku diffractometer which has a focused monochromatic Cu Kα1 rotated source with radiation λ= 1.54 Å and using a Bruker AXS GADDS. The XRD patterns of the annealed SiO_2 films on both n- and p-type (figure 23) do not show any definite crystallite phase, suggesting that they remained mostly amorphous. Moreover the annealed samples showed a background tail of the GaN peak, probably associated to a slight degradation of the GaN surface during the high temperature treatment, which could hinder the observation of a Ga_2O_3 or Ga peak.

Since no change in the crystalline phase of the material is observed, it can be suggested that the observed electrical changes after annealing are related to a modification of the interface (as seen in the different morphology and increased roughness) and the removal/apparition of defects either in the oxide or in the semiconductor.

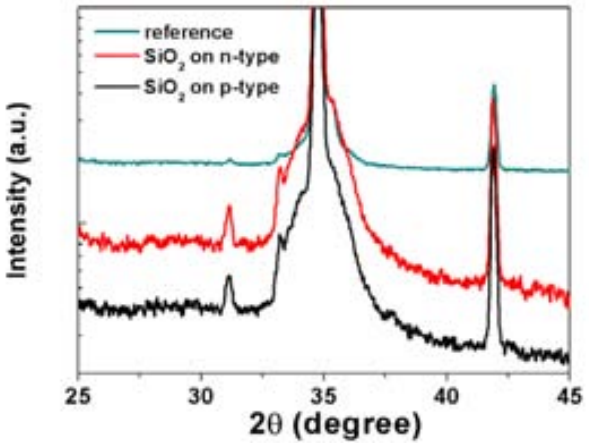


Figure 23. XRD spectra of the SiO_2 dielectric on n- and p-type GaN after annealing at 800 ºC in N_2 ambient during 2 min.

SIMS

This *p*-type TEOS AN sample was further analyzed. A time-of-flight secondary ion mass spectroscopy (TOF-SIMS) analysis has been performed to detect plausible species interdiffusion mechanisms between the TEOS-based SiO_2 and the *p*-type GaN after annealing (figure 24). TOF-SIMS (IONTOF IV instrument) depth profiling was carried out using Bi as high energy primary ion source (25 keV), combined with low energy sputter guns at 2 keV (Cs^+, O^{2-}) with angle of incidence 45° with respect to the surface normal. The sputtering ion beam is scanned over a 300 × 300 μm^2 area, while the primary beam is within an area of 50 × 50 μm^2 in the centre of the sputtered crater. Cesium ions were first used to sputter etch the surface while measuring the depth profile (figure 24(a)). A bare *p*-type GaN sample was also used as reference sample, to provide a clear comparison of the different involved mechanisms that could occur.

Different information can be extracted from this measurement. There is a clear evidence of an unexpected aluminium signal at the SiO_2/GaN interface extending towards the GaN layer. The wafer provider (TDI Inc.) corroborated that Al tails can be detected in SIMS depth profile scans for some of their commercial samples and linked this phenomenon with a kick-off mechanism of diffusion via point defects. It may be due to TMAl in the reaction chamber during the growth, but no details concerning the growth were provided. Another explanation could be that Al atoms can diffuse during the post SiO_2 deposition from the Al_2O_3 substrate into the GaN layer and segregate into dislocations [44, 45]. It also becomes evident a peak of GaO_x at the interface revealing the presence of Ga extending towards the SiO_2, as shown by the tail spreading into the oxide layer. This could be explained by the out-diffusion of the Ga from GaN into the SiO_2 layer.

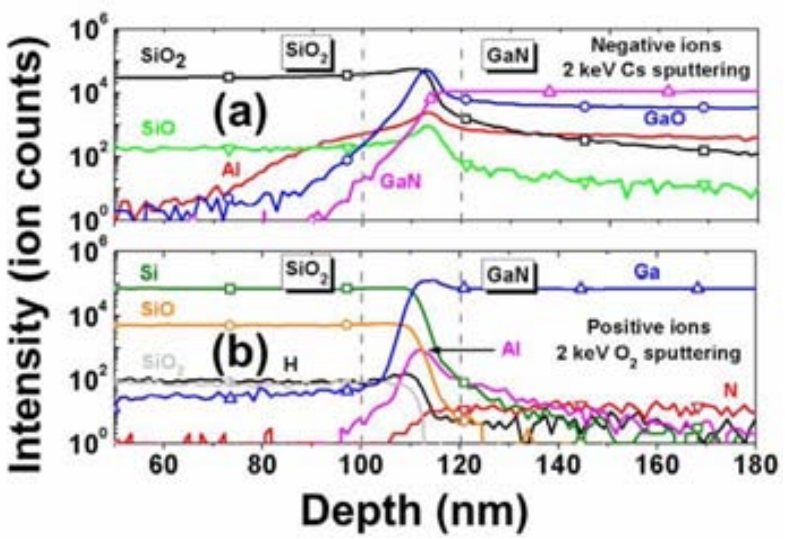


Figure 24. Quantitative TOF-SIMS depth distribution profiles of the aluminium, gallium, nitrogen, silicon, hydrogen, SiO and SiO_2 elements using (a) Cs^+ and (b) O^{2-} clusters for the TEOS-based SiO_2 deposited on GaN and annealed at 800 ºC in N_2 ambient during 2 min.

When oxygen ions are used as sputter medium for the measurements (figure 24(b)), Ga is detected in the whole SiO_2 layer from the top down to the SiO_2/p-GaN interface. This seems indicating that diffusion of Ga has occurred, even if no clear diffusion tail was observed. We suggest that, apart of the potential out-diffusion of Ga during high temperature treatments, Ga could be present in the SiO_2 as GaO_x from the GaN/SiO_2 interface oxidation [41]. It was suggested that Ga begins to out-diffuse during the SiO_2 deposition due to the presence of oxygen in the deposition chamber. In this sense, Lin *et al.* [41] already reported Ga diffusion into SiO_2. The diffusion rate of Ga in SiO_2 would be about 100 times faster than Si in GaN. The faint peak of Ga observed at our interface seems to effectively confirm a Ga diffusion process. Analogously, it has been reported out diffusion of Ga during the NiO_x deposition for contact realization on *p*-GaN. In this case, the oxygen assists diffusion of Ga from GaN and thus creating Ga vacancies below the contact and lowering the Fermi level [46]. Al is also detected at the interface, probably bonded with oxygen. Hydrogen is also observed. A light tail of silicon into the GaN layer seems also indicating a possible diffusion, which probably occurs during the annealing. Nevertheless, it should be mentioned that due the relatively high roughness obtained on the TEOS AN sample, the SIMS non-abrupt interface may be magnified and the diffusion processes overestimated.

6.3.3 Discussion

Compared to other Semiconductor/SiO_2 interfaces, the GaN/SiO_2 interface has not been extensively investigated and few works are available. The physics of the III-nitride/dielectric interface is rather complicated, since the III-nitrides surface is much more altered than expected with air ambient and/or products exposure during the different technological processing steps. Their varying polarity, lattice mismatch with most dielectrics, initial defects density (mainly depending on the type of material, and

Al concentration) and the high temperature treatment required for device fabrication also add difficulties to reliably reproduce and thus establish a reference process.

It may be considered that GaN technology is still in its infancy. Nowadays, commercial GaN wafers usually present an overall high density of threading dislocations, which can affect seriously the device behaviour. The effects of such imperfections are still not well understood. The interaction of dislocations with impurities, and in particular, silicon or oxygen, may create defects states in the band gap, acting as traps for carriers. As a general rule, any thermal process in an ambient containing oxygen and/or hydrogen requires particular attention since it could affect seriously the GaN surface, favouring the defects formation/diffusion. This would be especially relevant in the case of *p*-type GaN, since these species (Si and O impurities, and Mg dopants) migrate rapidly into the GaN. The plausible cause of this accelerated migration is related with the presence of dislocations. Compensation is possible with oxygen atoms if they were both present in a high enough concentration and electrically active. The hydrogen can also strongly influence the activation of *p*-GaN, even when unintentionally present. In particular for GaN on sapphire, species from the Al_2O_3 substrate may diffuse within the disordered interfacial region, creating donors responsible for the formation of an impurity band [47]. It has been reported that the amount of oxygen during the growth process can also induce an impurity band about 78 meV below the conduction band [48]. Moreover, the incorporation of oxygen into *p*-GaN is also possible after a SiO_2 thin layer on top was annealed [49]. Moreover, Al diffusion from the Al_2O_3 substrate has also been definitively observed during the GaN growth [44, 45] and could explain the result obtained in the Al peak at the interface in the SIMS measurement.

In addition to the possible diffusion mechanism occurring in the GaN/sapphire wafer, the TEOS and the silane process are inherently different. The TEOS-based deposited SiO_2 films are more prone to silanol (Si-OH) incorporation due to the large size of the TEOS molecule. Therefore, a complete restructuring is required to form dense SiO_2, and eliminate the –OH groups, which can be complicated if the absorbed molecule is under the surface, covered by subsequent deposition. By contrast, in the silane-based SiO_2, it is only required the elimination of the small hydrogen molecule.

Table VI-2 summarizes the electrical and physical properties obtained for the different SiO_2 capacitors. Comparing the interfacial properties of silane and TEOS-based SiO_2, it could be derived that the TEOS-based are more sensible to the annealing processes. N atoms can be also introduced into the bulk oxide during the deposition of the silane-based SiO_2, which uses N_2O and N_2 gases, explaining the higher negative flatband shift obtained compared to the TEOS-based SiO_2. It can also be argued that during the N_2 annealing, N can be incorporated into SiO_2, with the result that Si-N bond or Si-O-N bond are formed in SiO_2, and could explain the shift towards negative values of the TEOS-based SiO_2 C-V curve after the annealing. Moreover, the N from N_2 can react with the Si near the SiO_2/GaN interface to form Si oxynitride, which can block the nitrogen out diffusion from the GaN substrate more effectively than SiO_2. In fact, we suggest that nitrogen from the GaN surface is probably incorporated into the oxide, thus creating an SiO_xN_y layer at the interface, and this nitrogen lowering in the GaN near surface renders the gallium able to diffuse through the SiO_2 and up to its surface, at least for the TEOS-based SiO_2 on *p*-type GaN.

Table VI-2. Summary of the physical and electrical characteristics of the GaN SiO_2 capacitors.

Sample	ε_r	Q_{eff} [cm^{-2}]	D_{it} [$cm^{-2}eV^{-1}$]	*rms* [nm]
n-type				
Silane AD	3.9	9.7×10^{11}	1.1×10^{11}	0.74
Silane AN	3.9	8.9×10^{11}	6.1×10^{10}	2.9
TEOS AD	4.9	3.2×10^{11}	6×10^{11}	0.86
TEOS AN	4.9	7.9×10^{11}	9.2×10^{11}	2.6
p-type				
Silane AD	3.9	1.7×10^{12}	1.1×10^{11}	1.35
Silane AN	3.9	1.6×10^{12}	4.2×10^{11}	3.7
TEOS AD	3.9	--	1×10^{12}	1.68
TEOS AN	3.9	1.2×10^{12}	2.9×10^{11}	18

Lin [17] also reported the formation of SiGaON glass at the interface or in the dielectric layer. Moreover, SIMS clearly indicates species interdiffusion both into the oxide and the GaN layer, and an interfacial region around 15 nm can be distinguished. AFM measurements revealed the formation of islands that increased significantly the surface roughness both at the GaN surface and SiO_2 surface (or GaN/SiO_2 interface) of the TEOS-based SiO_2/p-GaN capacitors. These islands are either Ga metallic or Ga oxide or oxynitride, and could introduce additional interface states. However, the Ga-related interface states are probably not the only responsible of the anomalous capacitance behaviour observed after annealing at 800 °C. We believe that the incorporated hydrogen during the SiO_2 deposition, which are known to passivate the Mg acceptors and acting as donors, reduce the total number of acceptors. This could also explain the reduction of the accumulation capacitance and the presence of an inversion layer in the p-type capacitors.

The abnormal *n*-type conductivity behavior in the *p*-type GaN samples in the low frequency regime (quasi-static) (figures 16 and 17) indicates a decrease of minority carrier's response time. This fact could be attributed to the diffusion of Si or O atoms (from O precursor during deposition or from SiO_2 during annealing) into the Mg-doped GaN layer. Thus an undesired GaN region with Si or O impurities could introduce a reduced response time for the minority carriers to an applied gate voltage. The minority carrier generation can be explained by deep level impurities introduced during the SiO_2 deposition. This explanation correlates well with the fact that no inversion was observed in the TEOS AD SiO_2 capacitor (figure 16), since in this case the silicon atoms were already oxidized and could not diffuse into GaN. However, after thermal treatment, the inversion is observed, indicating a possible Si or O diffusion as it can be derived from the the Si tail into the GaN layer from the SIMS (figure 24).

Another explanation for the observed inversion in the QS CV curve, more speculative, could be related to the presence of local AlGaN or AlN, which could be a source of electrons when the capacitor begins to deplete, thus creating locally 2DEG areas.

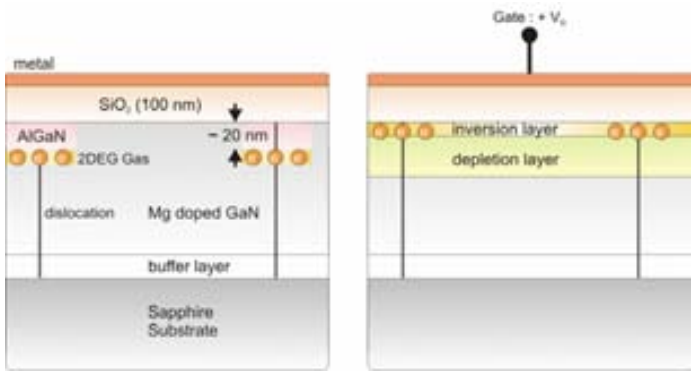


Figure 25. Possible mechanism explaining the observed inversion in the p-type MOS capacitors.

However, no 2DEG formation is expected in the NID AlGaN/p-GaN heterostructure. Nevertheless, during the SiO_2 deposition, Si or O can be easily incorporated through these areas (through the dislocations), thus creating a possible n-GaN or compensated GaN region, which thus satisfy and can result in a 2DEG formation at the interface. When a positive voltage is applied to the gate, a depleted region is created. However, in some areas, some AlGaN/GaN heterostructures can also be present, thus being a possible local source of electrons. Therefore these electrons are available to create a thin inversion layer. In figure 25, a schematic helps to understand the possible involved mechanism explaining the observed inversion.
Therefore, using an undoped AlGaN layer in top of the p-GaN layer could be a strategy to dispose of electrons for an n-channel GaN MOSFET.

6.3.4 Summary

In this section we have studied the properties of the SiO_2/GaN interface using different PECVD SiO_2 oxides with silane and TEOS as precursors. *n*- and *p*-type GaN on sapphire capacitors were fabricated and physically/electrically characterized. An annealing was performed at 800ºC for 2 min in N_2 ambient as an attempt to improve the electrical characteristics. Before and after annealing, C-V, G-V, I-V, SEM, AFM and TOF-SIMS measurements were performed. Globally, the *p*-type samples presented higher interface state density and rougher surfaces. The surface roughness also increases after annealing. The interfacial trap density for the different SiO_2/GaN interface has been determined. Silane samples exhibit lower D_{it} that TEOS samples. For *n*-type, annealed SiO_2 from silane has been found the sample with the lowest D_{it}. The annealing on the SiO_2 from silane samples seems to be no so effective for the *p*-type with the D_{it} actually increasing. Some peculiar droplets were also observed on the surfaces of the *p*-type samples. These droplets could be related with atoms diffusing out of the oxide in the form of Ga clusters, or local Ga_xO_y oxide becoming more evident after the high temperature annealing. The implication of different diffusion mechanisms is then discussed.

6.4 Transistors

Nitride transistors are expected to conquer part of the power management ICs market in the next years. Silicon power devices are rapidly approaching maturity, the performance improvement during the last 30 years being around two orders of magnitude, and the cost of possible enhancement prohibitive. WBG materials offer the possibility to surpass Si mainly in power conversion performance. SiC FETs emerged on the scene in the past ten years to address these issues but suffer from significant costs of the material. Moreover, SiC based technology lack from highly scalable substrate size, material supply and fabrication manufacturing platform. Likewise, GaN FETs have also been in development in the last ten years, especially in Japan by several industrial companies (Toshiba, Fuji Electric, Matsushita Electric, Oki, Hitachi). International Rectifier has also recently been interested in this material and important advances have been recently announced. Drastic reductions in energy consumption in end applications are expected, covering markets such as computing, communications, consumer appliances, lighting and automotive. Applications in high-end servers, and portable electronics products, such as notebooks, mobile handsets and smart phones, will probably first drive the demand. To further reduce the fabrication cost of parts using this material, important advances are currently being made in growing GaN layers on silicon and/or using bonding wafer techniques.

However, it is not clear which FET device will drive the GaN market, the battle being opened between the MOSFET and HEMT. In this part, we will discuss about the fabrication and electrical characterization of such devices, and will compare them for high temperature applications.

6.4.1 GaN MOSFETs

The MOS-based device is expected to be the base structure for GaN power switching applications. In silicon, the main developed high voltage (>300V) devices for this objective are the MOS-bipolar based structures [50]: the IGBT (Insulated Gate Bipolar Transistor) and the IBT (Insulated Base Transistor). However these devices are nowadays not possible to realize using GaN materials since highly doped P+ substrates are scarce and too resistive, and P+ implantation difficult to achieve with good activation. Moreover, the use of MOSFETs will allow the use of complementary devices, thus producing less power consumption and simpler circuit design. The main challenge for this technology is probably identifying a suitable gate dielectric, as it has been reported in the last section. However, despite many advances on GaN MIS-HEMTs, few GaN MOSFETs studies have been reported, especially in inversion-type device and with normally off characteristics. The main results on normally off GaN MISFETs are summarized in TableVI-3. It can be seen than all the results are recent, and the higher mobilities were achieved using SiO_2 as dielectric gate. Our first results are promising, and we expect to reach higher mobilities values, optimizing the different steps, in particular the dielectric gate processing. Currently we are the only group in Europe working on such devices, and having successfully fabricated them.

TableVI-3. Peak field effect mobility for lateral and vertical 2H-GaN MOSFETs found in the literature.

Polytype	μ_{FE} (cm^2/Vs)	Gate dielectric	Year	Ref.
Lateral n-Channel MOSFET on 2H-GaN				
undoped GaN on sapphire	45	SiO_2 LPCVD	2005	[51]
p-GaN on sapphire	< 0.1	MgO MBE 100 C 80 nm	2006	[52]
p-GaN on sapphire	167	SiO_2 100 nm	2006	[53]
p-GaN on sapphire	10	Al_2O_3 ALD	2008	[54]
p-GaN on sapphire	20	SiO_2 PECVD TEOS	2009	This work
p-GaN on sapphire	70-90	HfO_2 PLD	2010	[55]
Vertical n-Channel MOSFET on 2H-GaN				
$n^+/p/n^-/n^+$ GaN on sapphire	131	Si_xN_y/SiO_2 (1/100 nm) ECR-PAD	2008	[56]

Experimental details

Enhancement-mode GaN MOSFETs and capacitors have been fabricated on a p-type (0001) 2H-GaN epilayer grown on a c-plane sapphire substrate, supplied by TDI Inc, and identical to the one used for p-type capacitors. After solvent clean steps, a Si^+ implantation at 160 keV with a dose of 3.0×10^{15} cm^{-2} was performed to define source and drain regions [57]. The activation annealing process of the Si-implanted GaN was carried out with a 60 nm thick SiO_2 cap protection layer, deposited by Plasma-Enhanced Chemical Vapor Deposition (PECVD). The post-implantation annealing consisted of a two-step method, first at 1000ºC, for one minute, and then at 1150ºC for a tens of seconds. After removing the protection cap layer using SiO Etch, a chemical RCA based cleaning process was performed. A 100 nm thick (t_{ox}) SiO_2 layer was then deposited by PECVD as a gate oxide and annealed at 750ºC for 9 min in Ar ambient. Titanium and Aluminum were then deposited by sputtering and patterned by lift-off. The source and drain contacts were annealed at 700ºC for 90s in Ar ambient. The contact resistance of the source and drain electrodes was determined [57] to be lower than 10^{-5} Ω.cm^2. MOSFET characterization was performed with a set of Keithley units. Similarly to the MOS capacitors, the surface morphology was meticulously examined using SEM and AFM and the different observations discussed.

Electrical characteristics

Figure 26(a) shows the drain current-voltage characteristics of the lateral GaN MOSFET with a channel length (L) of 2 µm and a channel width (W) of 150 µm at room temperature, for different gate voltages. The output current is around 1 mA for a gate voltage of 22 V. The drain current (I_D) as a function of gate voltage (V_G) was also measured, at constant drain voltage (V_D) of 0.5 V. From these characteristics, the threshold voltage V_{th} was estimated by extrapolating the linear region down the voltage axis, to be about 2.5V. The direct drain-source characteristics were measured in the temperature range of 25-200ºC.

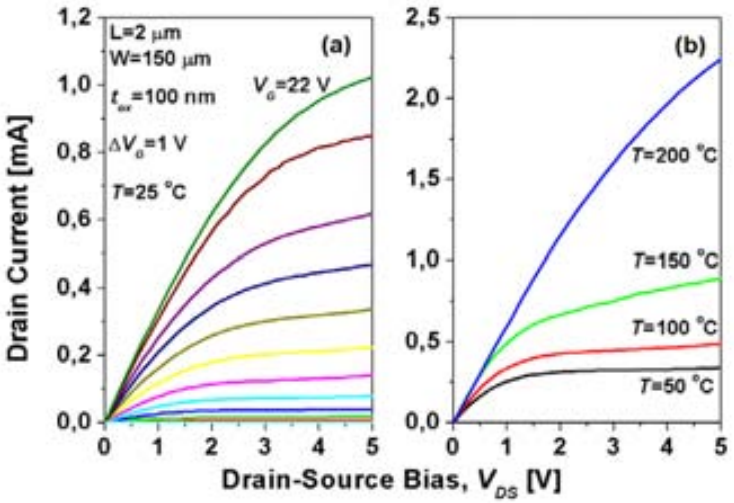


Figure 26. Drain current *vs* drain voltage, (a) varying gate voltage, (b) varying temperature.

Figure 26(b) shows the drain characteristics at different temperatures for a gate voltage of 14 V. The current increased significantly with temperature, in contrast with others reported results [58, 59] where high stability operation up to 200ºC was observed. The field-effect mobilities of the fabricated MOSFETs have been evaluated from the derivation of the transconductance curve using:

$$\mu_{FE} = \frac{L}{WC_{ox}V_D}\left(\frac{\partial I_D}{\partial V_G}\right) = \mu_{inv}\left[1+\frac{Q_{inv}}{\mu_{inv}}\frac{d\mu_{inv}}{dQ_{inv}}\right]\times\left[1+\frac{dQ_{trap}}{dQ_{inv}}\right]^{-1} \qquad \text{Eq. 6.1}$$

where C_{ox} is the insulator capacitance per unit area. For MOSFETs with a large density charge trapped at interface states (Q_{trap}), the values of field-effect mobility μ_{FE} will not correspond to the true inversion mobility μ_{inv} due to the presence of additional interface charge. Quantitatively, this correction introduces small difference in the computation of μ_{FE} from μ_{inv} [60], where Q_{trap} and Q_{inv} are the trapped and the inversion charge per unit area respectively. Figure 27 shows the field-effect mobility evolution with temperature. As it can be seen from figure 27(a), the field-effect mobility increases with V_G up to certain gate bias which depends on the temperature. The mobility increases more than three times (figure 27 (b)) for operation at 200 ºC compared to room temperature, for an effective insulator field of 0.5 MV/cm. The insulator field is defined by $E_{ox} = V_G / t_{ox}$, where t_{ox} is the oxide thickness. Since the bulk mobility decreases when temperature increases (see next section), other mechanisms have to be responsible of this behaviour.

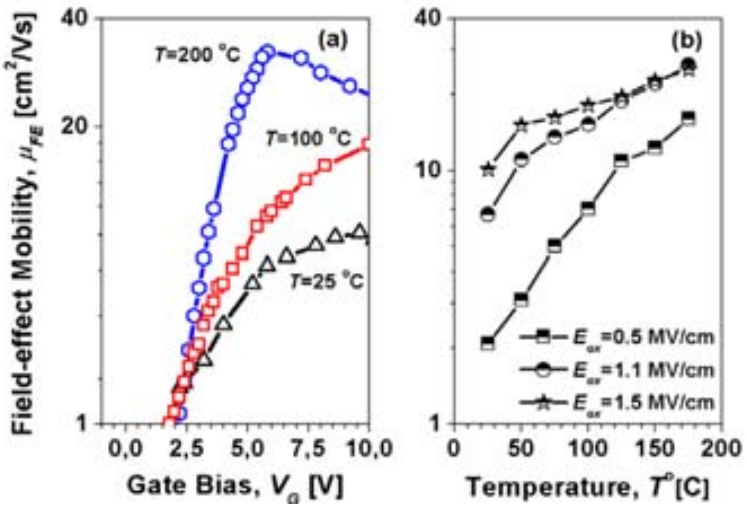


Figure 27. (a) Temperature influence of the experimental Field-Effect mobility vs gate voltage. (b) Field-Effect mobility vs temperature (for different insulator electric fields).

Physical characteristics

SEM images of the fabricated GaN transistor were performed to see the morphology of the different layers. It could be seen in figure 28 that the active area seems 'etched' but this is mainly due to the field oxide around the active area. To understand better these SEM images, a cross section of the fabricated MOSFET can be seen in the figure 29.

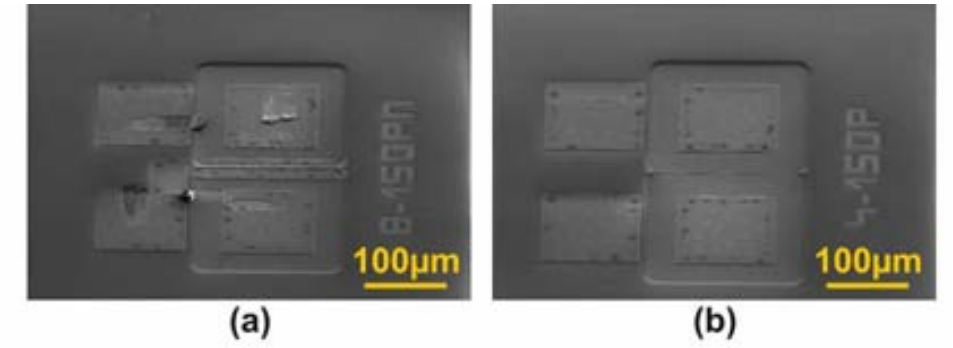


Figure 28. SEM images of a GaN MOSFET (a) with gate (b) without gate.

It appears obvious from this schematic that the observed SEM images are consistent with the observed morphology. In the SEM image of figure 30, more details on this active area and on the ohmic contact can be distinguished.

Figure 29. Cross section of the fabricated GaN MOSFET.

It should be also noted that the gate oxide between the two implanted area present a 'triangle shape' (figures 28(b) and 30(a)) thus suspecting a slight etching of the implanted GaN areas, especially marked in the small channel length devices. White drops were also observed on the SiO_2 gate oxide, and circular black areas observed below metals. To situate precisely the mechanism responsible of the undesired etch, different tests were performed:

(1) annealing on a single implanted sample (implanted only in opened areas and then annealing with an SiO_2 cap layer covering both implanted and protected areas), with opened and protected areas with SiO_2,

(2) annealing on a reference sample with opened and protected areas with SiO_2.

It was suspected that the damaged implanted-GaN was more prone to chemical solutions, such as the photoresist developer after ion implantation, or the SiOEtch used to remove the SiO_2 cap layer. Therefore these solutions were also investigated to verify if they can affect the GaN surface.

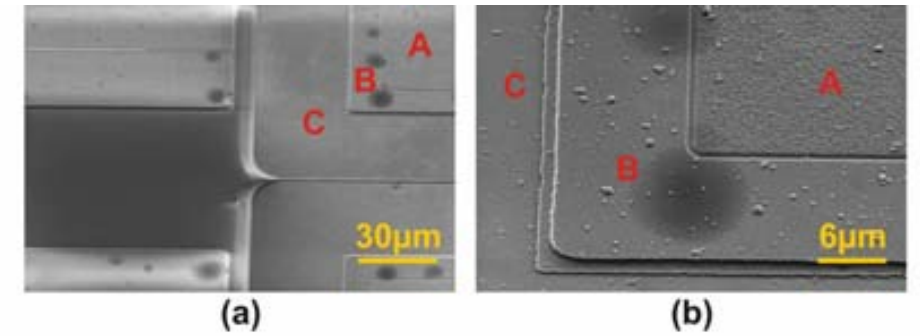


Figure 30. SEM images of the (a) active area, (b) ohmic contacts. The marked zones A, B and C correspond to Ti/Al on implanted GaN, Ti/Al on gate oxide on implanted GaN and gate oxide on implanted GaN respectively.

Optical images of the Si implanted sample can be seen in figure 31. From these images, we can note a presence of pits concentrated on the implanted and SiO_2 capped areas, especially at the edges and in some of them following lines in particular directions. These pits must be associated with dislocations terminating at the surface.

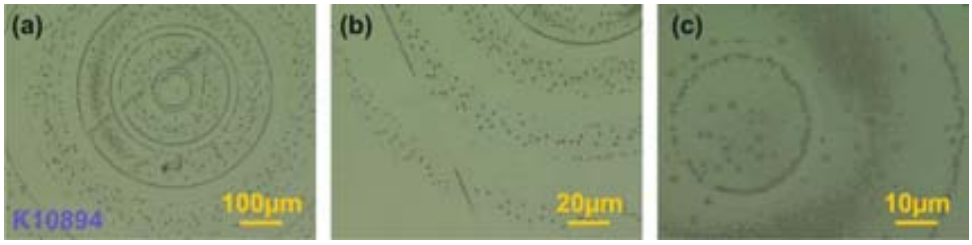


Figure 31. Optical images of sample K10894 with implanted and protected areas. The SiO_2 cap 100 nm thick was then deposited on the entire sample for the annealing step. (a) X5, (b) X20 and (c) X50 magnification.

In the AFM images of figure 32, these different areas are clearly distinguished. Black pits are present in the implanted area while in the protected GaN, white peaks are present. In the implanted areas, circular pits, up to 4 µm diameter and 100-150 nm deep, are present after annealing, indicating probably some material loss. To have another approach, SEM images (figure 33) were also performed, sustaining the morphology observed in the AFM images.

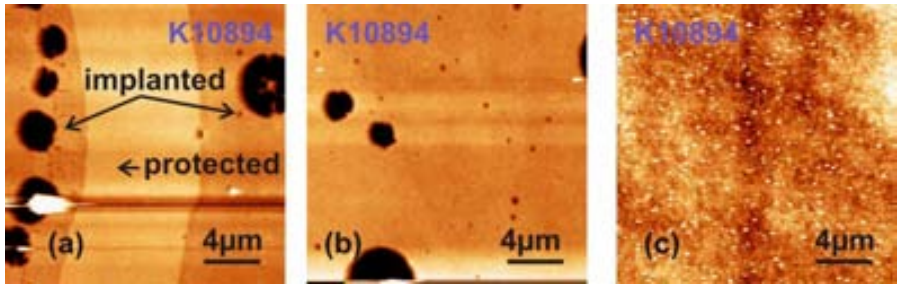


Figure 32. AFM images of the GaN surface after annealing in (a) the two zones (b) implanted zone and (c) protected GaN zone.

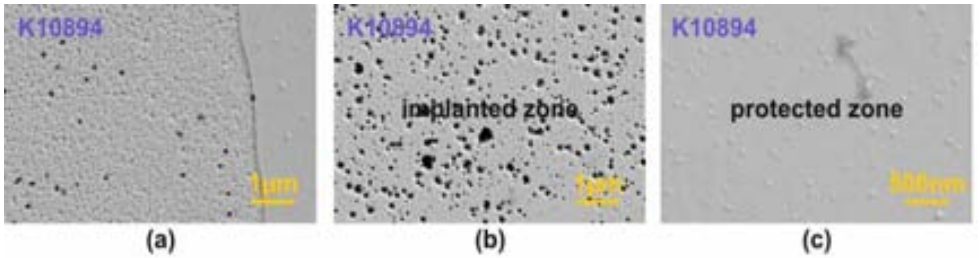


Figure 33. SEM images of the GaN surface after annealing in (a) the two zones (b) implanted zone and (c) capped GaN zone.

RMS roughness was estimated to be around 20 nm, similar to the values obtained in figure 2(b), but many pits (100-200 nm diameter) were observed and in some areas seem to segregate forming pits up to 2-4 µm diameter and 150 nm deep. The rougher surface (compared with the initial one) can be explained by the evaporation of the implanted GaN surface during the annealing with the SiO_2 cap, probably due to species diffusion favoured by the damaged material near surface and the generated stress at the interface with the cap. Between the protected and unprotected areas, there is a measured step of 15 nm.

That is interesting to see here for the MOS structure is the aspect of the (protected) GaN surface annealed with the SiO_2 cap layer: white residues up to 1 µm width and 50-100 nm thick (typically the thickness of the SiO_2 cap) are disseminated along the surface, revealing that the GaN/SiO_2 interface in the MOS structure probably presents the same roughness and residues.

Similarly, optical images of the reference sample are shown in figure 34. It can be seen that the capped area presents a clear contrast with the unprotected area (figure 35, 36), revealing that some material loss can effectively occur during the annealing. By contrast to the implanted sample, in the reference sample, the pits density in the opened areas is more elevated than in the protected implanted areas (figure 36(b)), but the pits have similar in diameter but much more deep, up to 500 nm, resulting in mean roughness around 35 nm.

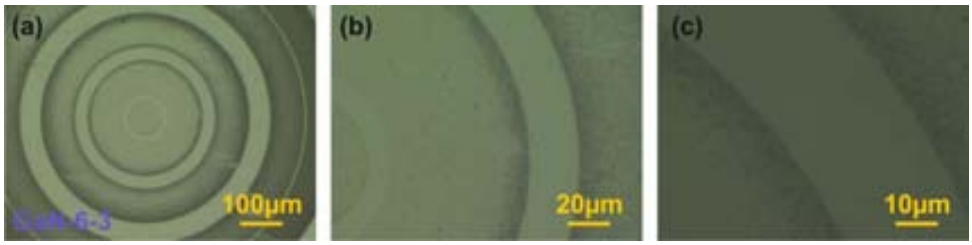


Figure 34. Optical images of the reference sample GaN-6-3 with exposed and protected (with SiO_2 cap) areas during the annealing step. (a) X5, (b) X20 and (c) X50 magnification.

The same white residues are observed in the areas protected with SiO_2. In both cases, a similar step between the uncapped and capped areas during the annealing around 15 nm is observed.

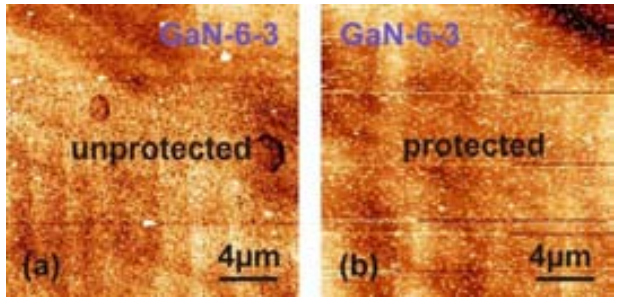


Figure 35. AFM images of the GaN surface in (a) uncapped GaN zone and (b) capped GaN zone.

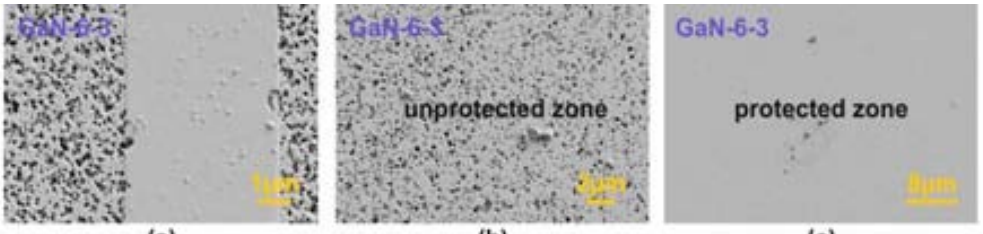


Figure 36. SEM images of the GaN surface after annealing in (a) the two zones (b) unprotected zone and (c) capped GaN zone.

Therefore, from these observations, different conclusions can be carried out:

(1) The implantation itself has little effect on the p-GaN surface,
(2) The developer has no effect on the GaN surface, implanted GaN surface and implanted/annealed GaN surface,
(3) Annealing on unprotected areas affects the surface: high density of holes are formed,
(4) Annealing on implanted GaN surfaces (which are protected with SiO_2) affects the surface: holes are formed and can segregate into large area holes,

Annealing in areas capped with SiO_2 does not increase so much the GaN roughness but result in the apparition of white microdrops in the GaN surface.

The use of SiOEtch, which can also be responsible of the undesired etching, is currently being investigated. It is also interesting to note that in figure 37, circular black areas are present in the metal contacts. This seems clearly reflected in the metal contacts with SiO_2 below but also on the metal on Si-implanted GaN, which has been annealed with a SiO_2 cap. Further investigations are also in course to understand this phenomenon but it is believed that localized reactions and formation of metal-silicides are probably occurring.

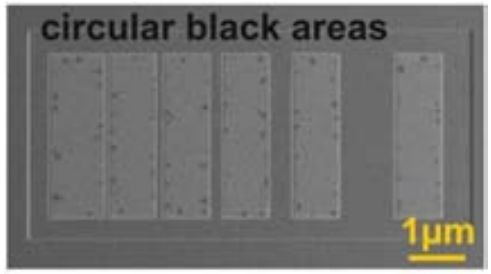


Figure 37. SEM image showing the observed circular black areas on a TLM structure.

6.4.2 Description of the mobility model

In this part, a physics-based model on the inversion charge and charge trapped in interface states characteristics has been used to investigate the temperature dependence of the inversion MOS channel mobility. The field-effect mobility increase with temperature is due to an increase of the inversion charge and a reduction of the trapped charge, for a given voltage gate. Then, for larger gate bias and/or higher temperatures, surface roughness effects become relevant. The good fitting of the model with the

experimental data, leads to consider that the high density of charged acceptor interface traps together with a large interface roughness, modulates the channel mobility due to scattering of free carriers in the inversion layer. A closed form expression for the experimental inversion MOS channel mobility is proposed.

Inversion Channel Mobility Model

The bulk carrier mobility (μ_B) for any semiconductor is a function of the temperature and doping concentration. The bulk mobility can be described by the well-known empirical derived formulation of Caughey-Thomas:

$$\mu_B(N_A,T) = \mu_0 + \frac{\mu_{\max}(T) - \mu_0}{1 + (N_A / C_r)^{\alpha 1}} \qquad \text{Eq. 6.2}$$

$$\text{with } \mu_{\max}(T) = \mu_{\max}\left(\frac{T}{300}\right)^{-\gamma} \qquad \text{Eq. 6.3}$$

where N_A is the acceptor impurity concentration (in the case of a p-type semiconductor) and μ_0, $\mu_{\max}$, C_r, $\alpha 1$ and γ are fitting parameters [61]. The mobility of carriers in the inversion channel of a MOSFET device is always a part of the carrier mobility in the semiconductor bulk. This is due to a collection of surface effects in the semiconductor/insulator interface. Lombardi [62] proposed a physics-based model where carrier mobility is described by the sum of several mobility contributions following the Matthiessen's Rule:

$$\mu_{inv} = \left[\frac{1}{\mu_B} + \frac{1}{\mu_{AC}} + \frac{1}{\mu_{SR}} + \frac{1}{\mu_C}\right]^{-1} \qquad \text{Eq. 6.4}$$

The widely accepted model consisting of the first three terms of (4) provides a good description of channel mobility for Silicon MOSFETs. There, μ_{AC} is the carrier mobility limited by the acoustic phonons scattering and μ_{SR} is the carrier mobility limited by surface roughness scattering.

Surface Acoustic Phonons

The surface acoustic phonons mobility coming from the quantized mode of vibration occurring in the crystal lattice is given by [62]:

$$\mu_{AC}(E_\perp,T) = \frac{B}{E_\perp} + \frac{CN_A^{\alpha 2}}{TE_\perp^{1/3}} \qquad \text{Eq. 6.5}$$

where B and C are two fitting parameters, that allow adjusting the degree of mobility reduction due to the electric field normal to the current flow and temperature, respectively. The dependency of μ_{AC} on the impurity concentration is given by $\alpha 2$.

Surface Roughness

Matsumoto [63] reported a very simple and popular approximation for the surface roughness mobility:

$$\mu_{SR}(E_{\perp}) = \frac{\delta}{E_{\perp}^{2}} \qquad \text{Eq. 6.6}$$

where $E_{\perp}$ is the perpendicular electric field, and δ is a fitting parameter. Based on detailed numerical calculations of the surface roughness-limited mobility it has been demonstrated [64] that the exponential of the perpendicular electric field ($\alpha 3$) and δ are not independent of the surface quality and temperature. A more general formulation of the surface-roughness, linking the mobility value with the interface quality is given by:

$$\mu_{SR}(E_{\perp},T) = \frac{A(\Delta\Lambda)^{-2}}{(E_{\perp}/E_{o})^{\alpha 3}}\left(1-\frac{T}{T_{o}}\right) \qquad \text{Eq. 6.7}$$

where Δ is the root mean square (rms) surface roughness of the asperities, Λ is the correlation length. A, T_0 and E_0 are fitting parameters depending of the doping and the semiconductor material.

Interface Traps Coulomb Scattering

The classical Lombardi model ($\mu_{inv}^{-1} = \mu_{B}^{-1} + \mu_{SR}^{-1} + \mu_{AC}^{-1}$) is successfully used for modelling the channel properties of MOSFETs with a properly passivated insulator/semiconductor interface. There, the oxide and interfacial traps are negligible. These traps, when charged, are responsible for the disturbing Coulomb scattering of free carriers in the inversion layer. In [65], a mobility model has been proposed for describing the mobility degradation observed in MOSFET devices including Coulomb scattering effects at interface traps. This model assumes a fixed charge distribution of ionized traps on the interface treating the random spatial fluctuations of charge density as a quantum mechanics perturbation. The free carrier screening effect introduces the dependence on the inversion trap. An additional term is then included to account for the Coulomb scattering at interface traps μ_C :

$$\mu_{C}(E_{\perp},T) = NT^{\alpha 4}\frac{(Q_{inv}(E_{\perp},T))^{\beta}}{Q_{trap}(E_{\perp},T)} \qquad \text{Eq. 6.8}$$

where N is proportionality constant, $\alpha 4$ is a temperature coefficient and β is an empirical coefficient.

In order to compute the field-effect mobility model (Eq. 6.4) it is necessary to determine $E_{\perp}$ along with the trapped and inversion charges for each gate voltage at a given temperature and this will be described in the next sections.

GaN/SiO_2 MOS Interface properties, Q_{trap}

Figure 38 shows the high-frequency C-V curve for a MOS capacitor with deposited SiO_2 on p-type GaN. The significant flatband shift, suggests that fixed positive oxide charges are present in the deposited SiO_2 bulk or at the GaN/SiO_2 interface. From the C-V and conductance characteristics, it is possible to determine the interface state density (D_{it}). In this case, D_{it} has been extracted by means of Terman method [39].

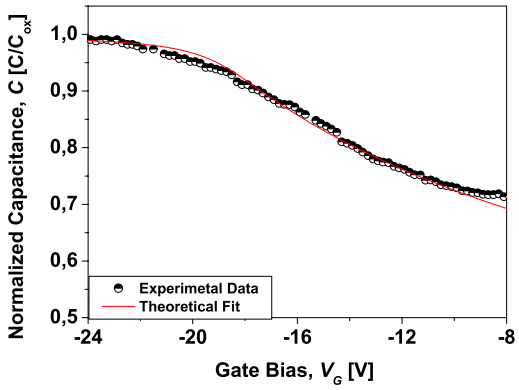


Figure 38. Normalized Capacitance-Voltage at 100 kHz.

This method is based on the quantification of the interface traps-induced distortion on the experimental C-V when compared to a theoretical C-V curve (displayed in figure 39 for $N_A=1.9\times10^{17}$ cm^{-3}). Solid points in figure 39 are the experimentally derived interface trap density within the bandgap. An interface state density close the valence band of 1.3×10^{12} $cm^{-2}eV^{-1}$ has been extracted at $E_T - E_V = 0.25$ eV. Inversion carrier mobility will depend on the amount of charge trapped at these interface traps. For a continuous energy distribution of interface states, the trapped charge in the interface states may be approximated by [38]:

$$Q_{trap}(E_F) = \int_{E_i}^{E_F} D_{it}(E)dE \qquad \text{Eq. 6.9}$$

where E_F is the surface Fermi level and E_i is the intrinsic level. As it can be seen from figure 39, the experimental D_{it} values increase significantly toward the valence band edge.

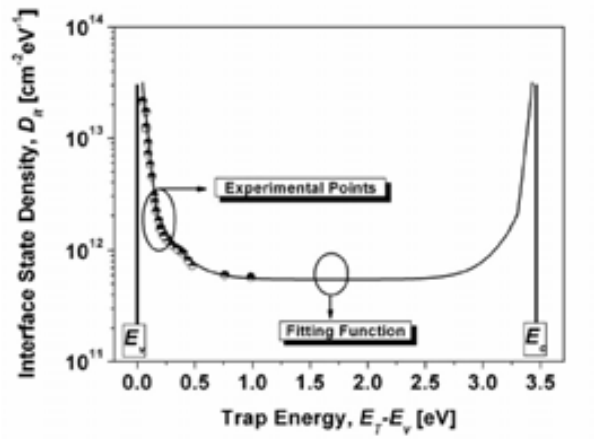


Figure 39. Interface state density *vs* Fermi energy. Experimental data from p-type GaN capacitors with deposited SiO_2.

For fitting that D_{it} distribution versus the trap energy E_T, we have used the following analytical function:

$$D_{it}(E_T) = \begin{cases} a_1 + a_2 e^{(E_V - E_T/\xi_1)}, & E_T - E_V > E_0 \\ b_1 + b_2 e^{(E_V - E_T/\xi_2)}, & E_T - E_V < E_0 \end{cases} \qquad \text{Eq. 6.10}$$

where a_1, a_2, b_1, b_2, ξ_1 and ξ_2 are parameters fitting the experimental interfacial trap spectra within the bandgap. E_V is the valence band energy. $E_0 = E_T - E_V = 0.15\,eV$ is an energy level chosen for describing the rapid increase of interface state density when approaching the valence band at the GaN/SiO_2 interface. The values of the fitting parameters are listed in Table VI-4.

Table VI-4. Interface traps simulation parameters values.

Parameter	Units	2H-GaN	References
D_{it} profile fitting parameters			
a_1	$cm^{-2}eV^{-1}$	5.1×10^{11}	This work
a_2	$cm^{-2}eV^{-1}$	4×10^{12}	This work
b_1	$cm^{-2}eV^{-1}$	3.45×10^{10}	This work
b_2	$cm^{-2}eV^{-1}$	8.55×10^{13}	This work
ξ_1	eV	0.160	This work
ξ_2	eV	0.040	This work
$E_0 - E_i$	eV	0.69	This work
Bandgap vs T			
E_{G0}	eV	3.47	[66]
α_G	eV/K	7.7×10^{-4}	[66]
β_G	K	600	[66]

GaN charge sheet computation, V_G, $E_\perp$ and Q_{inv}

A charge sheet model [60] of the Metal-Oxide-Semiconductor system was used for calculating the dependence of the inversion-layer charge density on Fermi energy E_F and gate voltage V_G, thus serving as a starting point for the description of current transport in MOS transistors. The model simplifies the calculation of inversion charge assuming that the inversion layer is a charge sheet of infinitesimal thickness. The charge sheet model equations are also used to compute the average effective field in the inversion layer $E_\perp$ required to calculate μ_{AC} and μ_{SR}. The solution for Q_{inv}, for an arbitrary value of V_G, is rather unwieldy. To compute the inversion channel mobility versus gate voltage it is simpler in practice to calculate values of Q_{inv}, Q_{trap}, $E_\perp$ and V_G for any arbitrary value of the Fermi potential, u_S. The inversion charge can be simplified by the difference between the total space charge Q_{sc} and the charge within the depletion layer Q_{dep}. Analogously, the effective field at the interface could be determined with $E_\perp = \varepsilon_s^{-1}\left(Q_{inv}/2 + Q_{dep}\right)$, where ε_s is the semiconductor dielectric constant. All the equations and variables used in the calculation of the inversion charge are detailed elsewhere [66]. The parameters used in the computation were N_A=2×10^{17}

cm^{-3}, $E_A - E_V$=0.2eV, $E_C - E_D$=0.1eV, $m_{d,e}$=0.2 m_0 (m_0 is the electron mass), $m_{d,h}$=1.5 m_0, ε_s=9.5, ε_{ox}=3.9 and t_{ox}=100nm.

Discussion

The experimental and simulated field-effect mobility of the fabricated MOSFET is presented in figure 40, at 25 ºC and 180 ºC. The computed values for μ_B, μ_{SR}, μ_{AC} and μ_C are depicted in this figure using the parameters detailed in Table VI-5. In a semiconductor bulk, the two main carrier scattering mechanisms limiting the mean free path of carriers (at low electric fields) are ionized impurity and lattice scattering [62]. The effect of both mechanisms, increase with temperature and hence, μ_B diminishes with temperature. Analogously, the mobility due to surface acoustical phonon scattering (μ_{AC}) diminishes with temperature. The three most important phonon-scattering processes [67] are deformation potential acoustic, piezoelectric acoustic and polar optical. It is usually assumed that acoustic phonons can propagate freely in all three dimensions, though electrons are confined to a thin inversion layer near the interface. There, the relaxation time depends on piezoelectric and lattice properties.

Hence, we could assume that neither μ_{AC} nor μ_B depend on the insulator/semiconductor interface properties. They depend on semiconductor material properties ($\mu_{mat}^{-1} \equiv \mu_B^{-1} + \mu_{AC}^{-1}$). Using parameters reported in the literature (due to the lack of data for 2H-GaN we have considered μ_{AC} values from 4H-SiC) [61, 68, 69], both μ_B and μ_{AC} were computed to be above 150 cm^2/Vs up to 300 ^oC. This mobility value was significantly higher than the experimental field effect mobility for our MOSFETs and the computed values of μ_{SR} and μ_C, thus their effect is considerably feeble following Eq. 6-4. At room temperature, it is clear that for our MOSFET, Coulomb scattering at charged interface traps dominates, and the mobility increases as a function of the gate voltage. This is due, as previously pointed out, to a density of traps at the SiO_2/GaN interface relatively high μ_C increases with temperature. Our modelling suggests that this improvement is due to two coupled effects, regardless of the linear temperature dependence for μ_C. When the temperature increases, for a given gate bias, the trapped charge is reduced due to screening of interface states by bandgap narrowing. On the other hand, a significant increase of inversion charge (a higher number of free carriers reduces the Coulomb scattering effect at interface traps) is a decisive factor for collecting more electrons in the drain of the device (figure 40(b)).

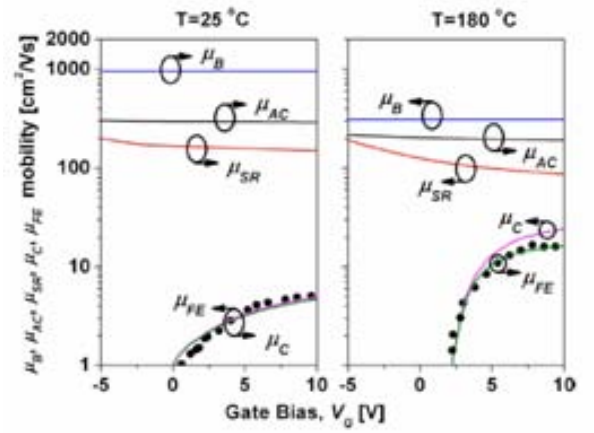


Figure 40. Simulated (solid lines) μ_B, μ_{AC}, μ_{SR}, μ_C and μ_{FE} and experimental μ_{FE} (symbols) *vs* gate bias for 25 and 180 ºC.

However, for temperatures higher than 150 °C and/or sufficiently high insulator electric field (i.e., effective field in the inversion layer), the field-effect mobility can not be entirely fitted by the Coulomb scattering term. This is due to the fact that surface-roughness is gradually becoming more and more relevant. Therefore, the mobility model simplifies to:

$$\mu_{inv} \approx \left[\frac{1}{\mu_{SR}} + \frac{1}{\mu_C}\right]^{-1} = \left[\frac{\Delta^2}{A'}\frac{E_\perp^{\alpha 3}}{(T-T_o)} + \frac{1}{NT^{\alpha 4}}\frac{Q_{trap}}{Q_{inv}^{\beta}}\right]^{-1} \qquad \text{Eq. 6.11}$$

This is a closed form expression for the experimental channel mobility for a MOSFET suffering interface collisions and scattering events. It explicitly depends on the interface quality main parameters: Δ, the surface rms roughness and Q_{trap}, the charge trapped in the interface states. A' (where $A' = AE_o^{\alpha 3}\Lambda^{-2}T_o^{-1}$), T_o and N are fitting parameters. $\alpha 4$ and β are empirical constants for describing the screening of the scattering charges by the mobile charges in the inversion layer and experimentally determined to be $\alpha 4 = \beta \approx 1$. Q_{inv} and $E_\perp$ are related to V_G by means of a charge sheet model. The exponential of the perpendicular electric field has been experimentally determined to be $\alpha 3$=2.3. High temperature post-implantation annealing leads to significant GaN surface dissociation, together with a severe degradation of the surface. Although a protective SiO_2 cap layer has been used, a significantly pit density has been observed [57]. The rms surface roughness of the GaN surface before the gate oxide deposition, measured using an Atomic Force Microscope (AFM), was 130 Å. A' is determined to be 1570 $cm^{4-\alpha 3}V^{\alpha 3-1}/sK$ from this value. Therefore, it is clear that for our fabricated MOSFET, interface trap charge along with surface roughness play a major role. In a GaN MOSFET device with a *perfect* insulator/semiconductor (i.e., (i) Δ=0 and (ii) $D_{it} < 10^{10} cm^{-2}$ and hence $Q_{trap}/Q_{inv} \to 0$) the field-effect mobility would tend to μ_{mat}. Improved GaN surface preparation and post-implantation annealing at high temperature are critical fabrication steps to achieve a good and smooth MOS interface.

Table VI-5. Model parameter values for the four terms, μ_B, μ_{SR}, μ_{AC} and μ_C.

Parameter	Units	2H-GaN	References
Low field channel mobility			
μ_0	cm^2/Vs	100	[61,68,69]
C_r	cm^{-3}	3×10^{17}	[61, 68,69]
$\alpha 1$		0.7	[61, 68,69]
μ_{max}	cm^2/Vs	1600	[61, 68,69]
γ		3.0	[61, 68,69]
Acoustic-phonon scattering			
B	cm/s	1.0×10^6	[61, 69]
C	$K\cdot cm/s(V/cm)^{-2/3}$	3.23×10^6	[61, 69]
$\alpha 2$		0.0284	[61, 69]
Surface roughness scattering			
A'	$cm^{4-\alpha 3}V^{\alpha 3-1}/sK$	1570	This work
$\alpha 3$		2.3	This work
T_0	K	700	This work
Coulomb scattering			
$\alpha 4$		1	[65]
β		1	[65]
N	$cm^2/VsK^{\alpha 4}$	0.2336	This work

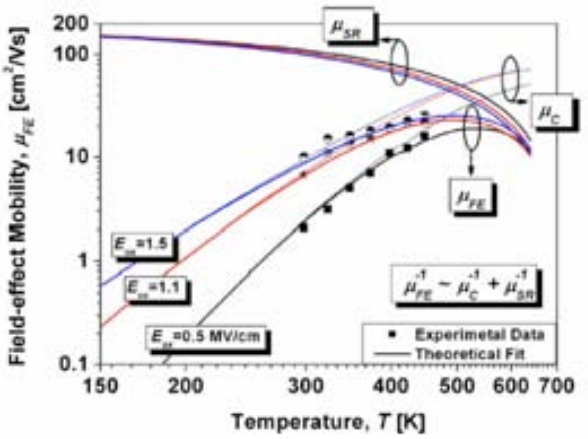


Figure 41. Simulated (solid lines) and experimental field-effect mobility (symbols) as a function of temperature. We have good agreement between the computational results and experimental mobility measurements.

Summary

In this section, we have reported the fabrication of GaN MOSFETs. The devices were electrically characterized with temperature and field-effect mobilities around the state of the art values have been obtained. Different observations using mainly SEM and AFM have shown that uncontrolled GaN surface modifications have occurred during the GaN MOSFET fabrication, revealing that this material is particularly sensible to the different involved steps. A compact channel mobility model has also been used to study the on-state and temperature dependence of the device suffering interface collisions and

scattering events. Interface trap density and surface roughness have been investigated and their dependence on the channel mobility has been reported. In our case, at low temperatures and/or insulator electric fields the channel mobility was well explained by Coulomb scattering at interface traps, taking into account their screening effect. When increasing the temperature and/or insulator electric field the surface roughness becomes relevant. We have good agreement between the computational results and experimental mobility measurements.

6.4.3 AlGaN/GaN HEMTs

III-nitrides heterostructures are also interesting for other transistor devices, taking advantage of a large confined two-dimensional Electron Gas (2DEG). This allows the realization of devices offering sticking electron mobilities (> 1500 cm^2/Vs), the High Electron Mobility Transistors (HEMTs). The main inconvenient of conventional HEMTs is that they are normally-on, and many groups are actively working to make them normally-off. Different techniques such as recess gate [70], fluoride based plasma treatments [71] or combining MOS with recessed gate HEMT have been proposed for this objective. However, the major limitations are due to DC/RF drain current dispersion and elevated gate-leakage currents. Different techniques have been used to withdraw these problems, one of them consisting in AlGaN-surface passivation, with dielectric layers such as SiO_2, SiN, AlN or depositing Si atoms [72-74], reducing efficiently the 2DEG sheet resistance and suppress the drain current collapse, but frequently at the detriment of a gate leakage increase.

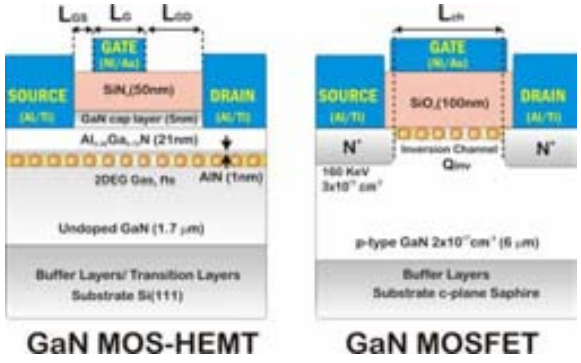


Figure 42. Cross section of the fabricated GaN MOS-HEMT and MOSFET.

Another concept, often combined with the first one cited (the surface passivation), involves a MIS structure (insulator under the gate) to reduce the gate leakage current. This could also be a solution to sustain higher voltage swings. Figure 42 present a MISHEMT device and compare it with the MOSFET.

In this part, we present the temperature measurements of HEMT and MISHEMT fabricated at CRHEA. This work was done using similar conditions to the measurements of our MOSFETs, in order to make a comparison.

Experimental details

AlGaN/GaN insulated gate HEMTs (MIS-HEMTs) have been fabricated on commercial Si(111). After a MBE growth at 920 °C of a 40 nm-thick AlN nucleation layer, a stress mitigating stack previously optimized to obtain a crack-free GaN layer up to 2–3 µm on Si(111) was deposited. This stack was basically formed by 250 nm of GaN and 250 nm of AlN. Then, a 1.7 µm GaN layer was grown at 800 °C, followed by the active layers. The active layer of the HEMT consists in a 1 nm AlN spacer to reduce alloy scattering and to enhance the electron mobility, and a 21 nm undoped AlGaN barrier with 0.3–0.31 Al mole fraction. Finally, the structure was covered with an additional 5 nm GaN cap layer. MIS-HEMT devices were processed as follows: First, a thin SiN passivation layer was deposited using the procedure described in [75]. Then, the device isolation was achieved by means of a 150 nm deep mesa etch realized by Cl_2/Ar reactive ion etching. Source/Drain ohmic contacts were formed by a Ti/Al/Ni/Au stack annealed for 30 s at 750 °C by rapid thermal annealing. The gate contact was made with a Ni/Au bi-layer. A reduced source/drain contact resistance of 9×10^{-6} Ω.cm^2 was extracted from the TLM measurements.

Electrical characteristics

HEMTs with 150-µm gate transistor with different drain-to-source spacing and channel length were fabricated. Measurements were performed on AlGaN/GaN HEMT and MIS-HEMT devices with a channel length of 11 µm and drain-to-source spacing of 20 µm. Both devices demonstrated good pinch-off characteristics. The maximum drain current density at Vgs=0 V is 230 mA/mm for the reference PTC166 and reaches 375 mA/mm for the sample SiN467. Figure 43 shows the typical DC I-V characteristics of these samples. Threshold voltages V_t of -4 and -10 V were extracted at 25ºC. Off-state source-drain leakage currents of 2 and 10 µA were measured at V_{gs} = -10V and V_{ds} = 6V. When compared with the reference HEMT, the passivated HEMT exhibits a higher drain current, especially at high electric fields. The higher drain current of the MIS-HEMT correlates with a more negative threshold voltage V_{th} and a higher sheet carrier density N_s [75]. This effect is usually observed on the output characteristics whatever the gate length. The shift of V_{th} is mainly due to the increasing distance between the gate and the 2DEG and can be determined by the following relation:

$$V_{th(MIS-HEMT)} = \frac{n_{s(MIS-HEMT)}}{n_{s(HEMT)}}\frac{C_{HEMT}}{C_{MIS-HEMT}}V_{th(HEMT)} \simeq \left(1+\frac{d_{ox}}{d_r}\frac{\varepsilon_B}{\varepsilon_{ox}}\right)V_{th(HEMT)} = 2.5\times V_{th(HEMT)} \quad \text{Eq. 6.12}$$

where d_r and d_{ox} are the AlGaN and dielectric barrier thicknesses (21 and 45 nm), ε_B and ε_{ox} the layer permittivities of AlGaN and SiN (8.8 and 7.4).

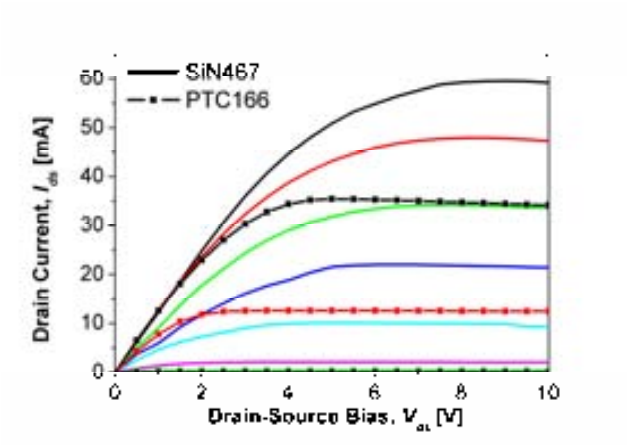


Figure 43. Output characteristics of 10 µm × 150 µm gate devices realized on the reference HEMT PTC166 and the MIS-HEMT SiN467 (V_{gs} is varied from 0 V to -10 V).

The DC I_{ds}-V_{ds} characteristics of these transistors are shown in figure 44 for different temperatures.

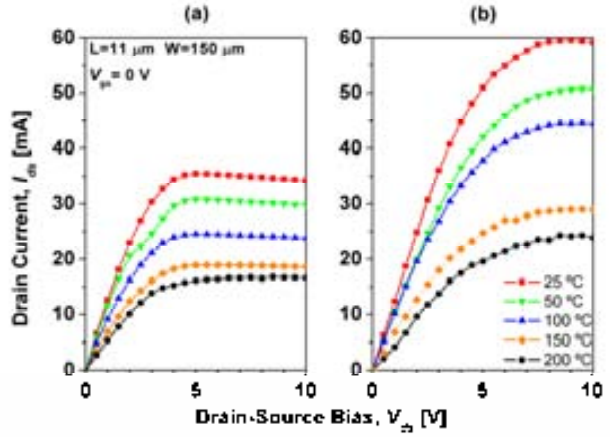


Figure 44. Drain current I_{ds} at V_{gs} = 0V in 11 µm × 150 µm gate devices varying temperature for the (a) HEMT and (b) MIS-HEMT.

As can be inferred from this figure, the drain current was significantly reduced with temperature, down to I_{ds} = 100 and 160 mA/mm at 200 °C for the HEMT and MIS-HEMT. A pinch-off voltage of −4 and −10 V was extracted at 25 °C for the HEMT and MIS-HEMT respectively. It was reduced with T up to a value of -6.5 V at 200 °C for the MIS-HEMT while it remains similar for the HEMT (figure 45). The transfer characteristics shown in figure 44 were measured at V_{ds} = 6 V. The maximum transconductance was evaluated in the range of 80 and 44 mS/mm at 25 °C and 45 and 24 mS/mm at 200 °C for the HEMT and MIS-HEMT respectively.

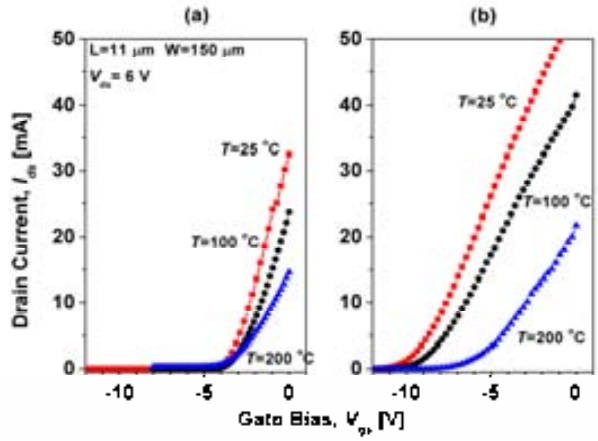


Figure 45. Drain current Ids at Vds = 6V in 11 μm × 150 μm gate devices varying temperature for the (a) HEMT and (b) MIS-HEMT.

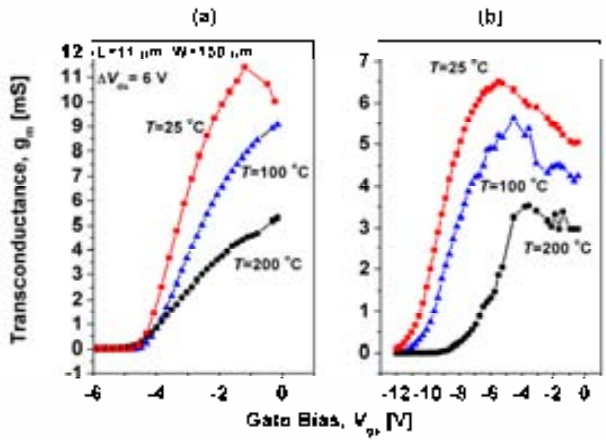


Figure 46. Experimental transconductances g_m for different temperatures for the (a) HEMT and (b) MIS-HEMT

6.4.4 MOSFET vs HEMT for high temperature applications

In this part, based on the temperature measurements obtained previously, we will compare the characteristics at high temperature of different GaN transistor devices, MOSFETs and MIS-HEMTs. The MOSFET and MIS-HEMT devices studied here have similar active areas, i.e., source-to-drain spacing. However, it is clear that the MIS-HEMT devices are capable of handling a higher level of current. To evaluate such current properties, specific on-resistance (R_{on}) has been estimated with the power device equation [76, 77]:

$$\frac{1}{R_{on}} = \frac{\partial I_{ds}}{\partial V_{ds}} \times \frac{1}{WL_a} \qquad \text{Eq. 6.13}$$

$$R_{on}(HEMT) = \frac{L_{ds}^2}{q\mu_n n_s}$$
$$R_{on}(MOSFET) = \frac{L_{ch}^2}{\mu_n C_{ox}(V_{gs} - V_{th})} \qquad \text{Eq. 6.14}$$

Where W is the channel width and L_a is generally the active area for power devices, i.e. the area where there is carrier flow within the device. Here, L_a has been defined for HEMTs as the source-to-drain spacing (L_{ds}=20 μm). L_a can be defined also as source-to-drain spacing (20 μm) for MOSFETs, although the channel length region (L_{ch}=2 μm) is by far the main contribution to the on-resistance. However, to be more precise, the effect of the contact resistance should be added.

For MOSFETs, the transconductance current (g_m) increases with temperature, while for HEMTs is reduced. Their specific on-resistance (R_{on}) follows the same trend as pointed out for g_m. Specific contact resistivity (ρ_c) to implanted Si N^+ GaN also diminishes with T, whereas for AlGaN/GaN ρ_c remains practically constant.

The MOSFET's field effect mobility increases with T being a trade-off between surface roughness and interface traps Coulomb scattering. Analogously, the HEMT's g_m decrease with T is attributed to a significant reduction of the 2DEG gas carrier mobility due to polar optical phonon scattering.

The MOSFET principle of operation in GaN is not substantially different from one transistor defined on Silicon which is well known: depending on the gate bias, one can create a depletion region containing immobile negatively charged acceptor ions. A further increase in the gate voltage eventually causes electrons to appear at the interface creating a low-resistance channel where charge can flow from drain to source. The main but crucial difference is the lack of a high quality native thermal oxide which results in a poor interface. It appears to be a problem common with other wide band gap dielectrics and/or other insulator stacks other than thermally grown SiO_2. Therefore, text book theory for GaN MOSFETs should not be straightforward applied without taking into account surface scattering effects and Coulomb interface trapping in particular. As already seen in the previous section, the mobility can be described by Eq. 6.4, the Coulomb scattering at interface traps described by Eq. 6.8.

The physics behind the HEMT transistor is notably different. It has been suggested [78] that surface AlGaN donor-like traps are the source of the electrons in the 2DEG channel, being these electrons driven into the channel by the strong polarization fields. Effectively, the positively charged donors in the AlGaN produce an electric field which creates a potential well in the GaN, confining electrons to a narrow strip at the interface, and leading to a quantization of the energy-band structure into sub-bands. This two-dimensional electron-gas density is a function of AlGaN doping level, its passivation scheme or the presence or not of an spacer layer [79], but it is typically in the range 5×10^{12}-10^{13} cm^{-3}.

The main scattering mechanisms in a 2DEG channel are well reported [79-83]. The 2DEG mobility is modelled analytically as the sum of several contributions including acoustic deformation-potential, piezoelectric, polar optic phonon, allow disorder, interface roughness, dislocation and remote modulation doping scattering. Therefore, the total relaxation time could be calculated as the sum of the relaxation times due to

each scattering process following again the Matthiessen's Rule. At temperatures above 80 K, the validity of this relation becomes questionable due to the relaxation-time approximation made for inelastic optical phonon scattering. However, the polar optical phonon scattering (μ_{po}) is the dominant scattering mechanism for 2D electrons in a wide temperature range since the impurity scattering is minimized, due to spatial separation of electrons and ionized impurities, being especially true for temperatures above 300 K. Therefore equation Eq. 6.13 describes this mobility for a 2DEG using the conventional relaxation-time approximation for the case when the optical-phonon energy is greater than the thermal energy [80]:

$$\mu_{2D,po} = \frac{(\varepsilon_{s,\infty}^{-1} - \varepsilon_s^{-1})^{-1} k_0 \hbar^2}{2\pi q \omega_0 m^{*2} G(k_0)} \left(e^{\frac{\hbar\omega_0}{k_B T}} - 1 \right) \left(1 + m^* k_B T \left(\frac{1 - e^{-\frac{\pi\hbar^2 n_s}{m^* k_B T}}}{\pi\hbar^2 n_s} \right) \right) \qquad \text{Eq. 6.15}$$

Where $\varepsilon_{s,\infty}$ is the permittivity of the semiconductor at high frequencies and $\hbar\omega_0$ is the energy of the polar optical phonon, The wave vector of the polar optical phonon is computed by $k_0 = \sqrt{2m^*\omega_0/\hbar}$. In this case, the form factor $G(k_0)$ depends on the channel geometry and in the in the narrow channel near the heterointerface can be calculated as

$$G(k_0) = \frac{b\left(8b^2 + 9k_0 b + 3k_0^2\right)}{8(k_0 + b)^3} \qquad \text{Eq. 6.16}$$

With the variational parameter, b being

$$b = \left(\frac{33\pi m^* q^2 n_s}{2k_0 \hbar^2} \right)^{1/3} \qquad \text{Eq. 6.17}$$

As for the case of MOSFETs, it has been proposed [82] simpler empirical relationships for the polar-optical mobility:

$$\mu_{2D,po} \simeq \frac{C}{n_s^{\delta 1} T^{\gamma 1}} + \frac{D}{n_s^{\delta 2} T^{\gamma 2}} \simeq \frac{C}{n_s^{\delta 2} T^{\gamma 2}} \qquad \text{Eq. 6.18}$$

Equation Eq. 6.18 may be considered as an interpolation between the temperature dependence near 77 K ($\delta 1, \gamma 1$) and the temperature dependence near 300 K ($\delta 2, \gamma 2$). At elevated temperatures, Eq. 6.18 simplifies then to the last term.

The GaN-based transistor temperature dependence (R_{on}, saturation current, transconductance…) is determined by the electron mobility. Simple semi-empirical comprehensible Eq. 6.4 and Eq. 6.18 have also been proposed for describing the actual electron transistor mobility on the MOS inversion and 2DEG channel at elevated temperatures, respectively.

In the case of MOSFET transistors, electron mobility depends on Coulomb scattering at interface traps. It has been observed that for our GaN MOSFET electron

channel mobility (and transconductance) increases with T, i.e. GaN MOSFETs exhibit a positive temperature coefficient, $T \sim T^{2.2}$. This behaviour is due to two coupled effects, regardless of the linear temperature dependence for μ_c. When the temperature increases, for a given gate bias, the trapped charge (Q_{trap}) is slightly reduced due to screening of interface states by bandgap narrowing. On the other hand, a significant increase of inversion charge (Q_{inv}) - a higher number of free carriers reduces the Coulomb scattering effect at interface traps- is a decisive factor for collecting more electrons in the drain of the device (figure 47(a)).

In contrast, HEMT transistors exhibit negative temperature coefficient, $T \sim T^{-1.8}$. In the case of HEMTs material lattice vibrations due to polar-optical phonons on the non-intentionally doped GaN layer are the mobility limitation factor at elevated temperatures. This polar-optical phonon mobility depends on temperature (mainly because phonons follows the Bose-Einstein distribution function of occupancy) and 2DEG sheet charge density. However, as depicted in figure 47(a), the sheet carrier density of electrons in the 2DEG is almost constant up to 500 K.

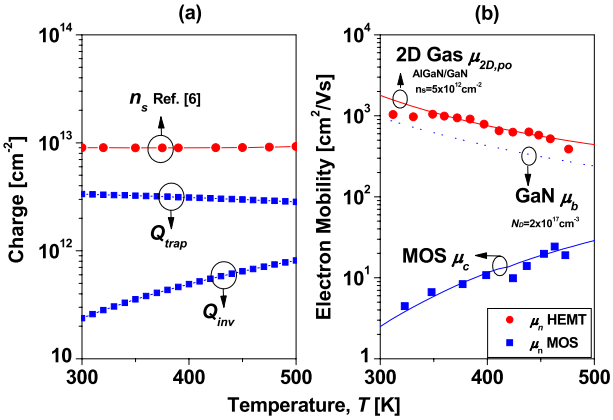


Figure 47. (a) HEMT sheet carrier density (n_s), MOS inversion charge and interface traps charge (b) Experimental (symbols) vs modelled (solid lines) electron mobility vs temperature.

Figure 47(b) shows the experimental electron mobility, as a function of the temperature, for MOSFET and HEMT transistors as evaluated from the on-resistance equation Eq. 6.13. Theoretical computed mobilities as extracted from Eq. 6.4 and Eq. 6.18 are also presented (solid lines). The good fit obtained would suggest that our approach seems appropriate.

From figure 47(b) it becomes evident the higher electron mobility values ($\times$ 10-100) achieved in our 2DEG AlGaN/GaN channels when compared to our inversion MOS deposited SiO_2/GaN channels. The reason for such a huge mobility difference is that, in the MOSFET transistor, conduction electrons occupy the same space region than ionized impurities and hence, channel mobility is limited theoretically by bulk carrier mobility (μ_b). Besides, MOSFET mobility is in practice a fraction (via Matthiessen's Rule) of this bulk mobility due to scattering effects at the insulator/semiconductor interface, mainly Coulomb scattering at interface traps, that is dramatically relevant in GaN based MOSFETs. In HEMT transistors optical phonon limited mobility (bulk or

2DEG) is already higher than the bulk mobility for GaN under the same transverse electric field. This difference in the peak mobility value is more relevant at room temperature since at elevated temperatures the 2DEG mobility drops following the classical phonon dependence. Therefore, 2DEG high mobility based channels appears to be more adequate for the new highly efficient power switch based on GaN (especially if it is not required elevate temperatures of operation) though open issues, as the normally-on behavior, gate leakage current and device reliability, remain.

6.4.5 Summary

The DC characteristics of signal GaN-based MOSFETs and HEMTs transistors at elevated temperatures are compared in this section. The transconductance of MOSFETs increases with temperature while g_m decreases with T for HEMTs. The specific on-resistance of the MOSFET is much larger than the on-resistance for the HEMT which is depending on the mobility of the electrons in their respective channels. The channel mobility for MOS inversion and 2DEG channels are extracted from the on-resistance. Physically-based models are used to fit the experimental transistor mobility. MOSFET mobility is in practice a fraction (via Matthiessen's Rule) of the GaN bulk mobility due to scattering effects at the insulator/semiconductor interface, mainly Coulomb scattering at interface traps. In HEMT transistors optical phonon limited mobility, which is the main limiting mechanism, is already higher than the bulk mobility for GaN and for this reason 2DEG channels are able to handle much more current density for a given drain bias, making GaN based HEMT structures highly interesting as the basis for an advanced power semiconductor switch.

6.5 Summary

In this part, the main steps for the fabrication of a GaN transistor device have been investigated. Surface cleanings, ohmic contact formation to Si-implanted GaN or AlGaN and SiO_2 deposition were preliminary steps to develop a GaN technology at CNM. Therefore, the first 2H-GaN MOSFETs have been successfully fabricated at CNM using TEOS-based SiO_2 and have shown promising results, especially for high temperature operation. Few groups in Europe have reported the fabrication of a GaN MOSFET, and research is currently intense to realize a GaN transistor device that could substitute the Si one to surpass its limitation as well in high frequency that in power or high temperature applications. However, the obtained mobilities were low compared to those reported for the AlGaN/GaN HEMT devices. Especial interest has been then focalized in this kind of devices, to take profit of the elevated 2DEG gas carrier mobility present in these heterostructures. For this reason, the last part introduces the concept of HEMT devices and the electrical characteristics measured with temperature. A PhD thesis has also recently began at CNM concerning the fabrication of a GaN HEMT device to produce a normally-off power GaN switch 600-1200V/5A. This confirms the choice and strategy of the CNM to pursue with the GaN technology and optimize the different processes.

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CONCLUSIONS

The main work of this thesis consisted in improving the WBG technology for resonator and transistor applications. In this sense, summarizing in few lines the most important achievements of this work, it could be said that:

1. SiC lateral electrostatic resonators insulated from the substrate have been developed using single crystalline material, allowing thus in the future an eventual electronics integration. To achieve this goal, different steps were required: finding the material (not commercially available), set up a suitable technological process and improving the material for the desired application, working closely with material growth research groups. The Young modulus of the different used SiC layers was evaluated between 395-530 GPa. Innovative devices, with thicknesses higher than 1 μm, with width comprised between 0.8-2.5 μm and length up to 500 μm were successfully fabricated using SiC on Si as starting material. Ohmic contacts were also developed on the SiC layer, and reasonable contact resistivities values were achieved. Comparison with equivalent Si devices revealed that SiC is mechanically better, showing higher resonance frequencies and quality factors. However due to poor electrical isolation with the substrate, it was difficult to sense electrically the resonator. For this reason, pursuing our collaboration with CRHEA and LMI, different SiC research materials insulated from the substrate, SiC on semi-Insulated Silicon (SIS) and SiC on SOI, were considered as possible materials for SiC electrostatic resonators fabrication. Concepts to reduce the gap post fabrication were also investigated using bistable and spring structures, and are still under investigation. The SiC crystal quality has been corroborated by means of XRD, AFM, SEM and Raman. The results shown that isolation of the bulk was critical to avoid leakage current and in reducing considerably the required voltage to actuate the SiC resonators. Full electrical resonance frequency measurements were also performed in the temperature range of 25-200 ºC, demonstrating the good stability of the SiC devices at these temperatures.

2. III-nitrides, and especially AlN, have been then considered as an alternative material to SiC for resonator fabrication. Pursuing our collaboration with CRHEA, single crystalline AlN grown by MBE has been obtained, and investigated for MEMS applications. As part of material characterization, the insulator properties of the epitaxial AlN were first investigated, by thermally oxidizing (1000 ºC) AlN in O_2, and directly compared with sputtered AlN. It has appeared that epitaxial AlN is a rather good dielectric: an interface state density of 2.5×10^{11} $cm^{-2}.eV^{-1}$ has been extracted from C-V measurements, and was slightly improved to 1.8×10^{11} $cm^{-2}.eV^{-1}$ after oxidation. From I-V measurements, the as deposited AlN followed a hopping conduction

mechanism for low electric fields while at higher biases, the current was described by a Schottky emission theory. These results motivated us to study this material and its oxidation as possible insulator for GaN. Investigation is currently in course.
Two methods for the fabrication of suspended devices from AlN on Si substrates have been then investigated in this thesis. The first one was based on etching the AlN layer using dry chlorine-based plasma, while the second one only relied on Si etching techniques. The mechanical parameters of AlN have been determined from resonance frequency measurements, giving values of Young moduli comprised between 286 and 272 GPa. Moreover, the high tensile stress of the AlN layer allows abruptly increasing the resonance frequency of bridge-based resonators, thus increasing the sensitivity. Further investigation of III-nitrides resonator fabrication is currently in course using the AlGaN/GaN heterostructure, and taking advantage of the 2DEG created at the interface.

3. In a third part, the III-nitride technology was investigated through the realization of a GaN MOSFET device, compatible with the MEMS fabrication. The different involved steps for GaN transistor or MEMS fabrication were studied: the surface cleaning, the formation of ohmic contacts both on implanted p-type GaN (for MOSFET) and AlGaN (for HEMT), and the dielectric gate deposition using SiO_2… the etching step being reported in Chapter 4. From these different parts, it has appeared that the physics of the III-nitride/metal or III-nitride/dielectric interface is rather complicated, since the III-nitrides surface is much more altered than expected with air ambient and/or products exposure during the different technological processing steps. Their varying polarity, lattice mismatch with most dielectrics, metal alloying for ohmic contact formation, initial defects density (mainly depending on the type of material, and Al concentration) and the high temperature treatment required for device fabrication also add difficulties to reliably reproduce and thus establish a reference process. Contact resistivity (ρ_C) in the range of $(1\text{-}5)\times10^{-5}$ $\Omega.cm^2$ was obtained for Si-implanted p-type GaN contacts using the Ti/Al metallic scheme, and around 10^{-3} $\Omega.cm^2$ for contacts using the Ti/Al/Ti/Pt scheme in an AlGaN/GaN heterostructure. In both cases, the mechanism responsible for the contact ohmicity is different but is believed to be related to TiN formation.
Concerning the dielectric study on GaN, our investigation was focused on plasma deposited SiO_2 using different precursors. Electrical and physical characterizations demonstrated that different diffusion mechanisms probably occurred during the dielectric deposition and annealing. An interface state density of 6×10^{10} cm^{-2} has been obtained for the silane-based SiO_2.
GaN MOSFETs fabricated at CNM, and GaN HEMTs fabricated at CRHEA, have also been characterized at elevated temperatures and are compared in a final part. The transconductance of MOSFETs increased with temperature while it decreased for HEMTs. In MOSFET devices, the mobility is a fraction of the bulk mobility, due to scattering effects at the semiconductor/dielectric interface, mainly Coulomb scattering, while in HEMT devices, the limiting for mobility factor is the optical phonon mobility, which is higher than the GaN bulk mobility.

SUGGESTIONS FOR FUTURE WORK

Several suggestions for future work are here announced, some of them being currently investigated by our group.

1. Concerning the SiC MEMS, the fabrication process is now optimized. Various structures are currently being investigated to reduce the gap between the resonator and input electrode. A PhD thesis currently in course is investigating 3C-SiC insulators and thus possible 3C-SiC MOSFET fabrication. Another PhD thesis has recently began at CNM with the objective of SiC circuitry integration. Another PhD thesis, concerning the thermal mechanical stress in SiC devices has also began. All these future works will probably open the doors to a possible SiC circuitry integration for SiC MEMS and a better understanding of the thermal stresses during the MEMS operation.

2. About the AlN, this material is highly interesting for MEMS application. We are currently investigating the piezoelectric properties of epitaxial AlN. Moreover, the study of the mechanical stresses in AlN layer is particularly interesting since it is also used in buffer layers for AlGaN/GaN heterostructures. AlGaN/GaN is being currently investigated as a possible starting material for AlGaN/GaN MEMS fabrication, taking advantage of both the 2DEG created at the interface, and the piezoelectrical properties of III-nitride layers. Moreover, the interesting insulating properties of AlN have attracted us to investigate it as a possible dielectric for GaN MIS structures, and are currently under study.

3. Concerning the GaN part, further investigation is required to understand the effects of the different process steps to its surface and interface with metals and dielectrics. We are currently investigating different dielectrics for GaN MIS structures (epitaxial and sputtered AlN, Al_2O_3 and HfO_2), in order to reduce the scattering effects and achieve higher mobility in GaN MOSFETs. Parallel to this work, a PhD thesis has began concerning the AlGaN/GaN HEMTs fabrication for power switching application, thus confirming the CNM strategy to bet on this technology.

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ANNEX 1: TRANSVERSE VIBRATIONS OF AN IDEAL BEAM

In this section, the natural free vibration modes for beams, like the cantilever shown in figure 1, are derived. These equations will be solved for the cantilever, and will be similar for the bridge.

Case of the microcantilever:

Most relevant dimensions of the beam are shown in the figure 1.

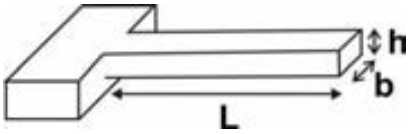

Figure 1. Schematic of an ideal beam with the important dimensions: thickness *h*, width *b* and length *L*.

The free resonance modes are given by the Euler-Bernouilli equation and can be written [1]:

$$EI\frac{\partial^4 w(x,t)}{\partial x^4}+\rho A\frac{\partial^2 w(x,t)}{\partial t^2}=0 \qquad \text{Eq. A1.1}$$

where the variable *w(x,t)* is the dynamic deflection of the beam as a function of the position along the beam axis *x* and time *t*; *E* the Young modulus, and *I* the moment of inertia.
p is the mass density of the beam material
A is the cross sectional area of the beam

The first term describes the restoring force due to the stiffness of the beam in flexion EI, while the second the inertia lied at the mass by length unit.
For a cantilever having a rectangular section with a width *b* and thickness *h*, $A=bh$, and the area moment of inertia is:

$$I=\int_A z^2 dA=\frac{bh^3}{12} \qquad \text{Eq. A1.2}$$

Writing *w* as the product of space *W* and time *T* functions, we have:

$EIT\frac{\partial^4 W}{\partial x^4}+\rho AW\frac{\partial^2 T}{\partial t^2}=0$ giving, dividing by WT:

$\frac{EI}{W}\frac{\partial^4 W}{\partial x^4}=-\frac{\rho A}{T}\frac{\partial^2 T}{\partial t^2}$, functions depending only on the position (left term) and time (right term), therefore two functions equal to a constant $\rho A\omega^2$.

There is therefore a time harmonic dependence $T=e^{iwt}$ and the equation Eq. A1.1 becomes:

$$\frac{\partial^4 W}{\partial x^4} - \frac{\rho A \omega^2}{EI} W = 0 \qquad \text{Eq. A1.3}$$

We can find W in the form of a sum of complex exponential functions $W = \sum_{i=0}^{3} a_i e^{\beta_i x}$ and by grouping the conjugated terms of this sum we can write:

$$W(x) = C_1(\cos(\beta x) + \cosh(\beta x)) + C_2(\cos(\beta x) - \cosh(\beta x)) + C_3(\sin(\beta x) + \sinh(\beta x)) + C_4(\sin(\beta x) - \sinh(\beta x)) \qquad \text{Eq. A1.4}$$

The boundary conditions at $x = 0$ (bending moment $\frac{\partial^2 w}{\partial x^2}$ and shear force $\frac{\partial}{\partial x}\left(EI\frac{\partial^2 w}{\partial x^2}\right)$ equal to 0) and at $x = L$ (deflection w and derivative $\frac{\partial w}{\partial x}$ equal to 0) allow to calculate the constants C_1, C_2, C_3 and C_4, and we obtain

$$\cos(\beta_n L).\cosh(\beta_n L) + 1 = 0 \qquad \text{Eq. A1.5}$$

where $\beta^4 = \frac{\rho A w^2}{EI}$

Therefore, for a cantilever, the angular frequencies of the resonance are given by the expression:

$$\omega = \beta^2 = \sqrt{\frac{EI}{\rho A}} = \frac{(\beta L)^2}{L^2}\sqrt{\frac{EI}{\rho A}} \qquad \text{Eq. A1.6}$$

And in the case of cantilever with a rectangular section:

$$\omega_n = \frac{(\beta_n L)^2}{\sqrt{12}}\frac{h}{L^2}\sqrt{\frac{E}{\rho}} \qquad \text{Eq. A1.7}$$

Writing $\lambda_n = \beta_n L$ and $\omega_n = 2\pi f_n$, the resonance frequencies are given by:

$$f_n = \frac{(\lambda_n)^2}{2\pi}\frac{1}{L^2}\sqrt{\frac{EI}{\rho A}} = \frac{(\lambda_n)^2}{2\pi\sqrt{12}}\frac{h}{L^2}\sqrt{\frac{E}{\rho}} \qquad \text{Eq. A1.8}$$

The values for the constants λ_n, $\lambda_n^2/2\pi$, $\lambda_n^2/2\pi\sqrt{12}$ are given in the table below for the first modes.

Table A1-1. Constants values for the determination of the resonance frequencies for the first vibration modes of ideal cantilevers.

n	λ_n	$\lambda_n^2/2\pi$	$\lambda_n^2/2\pi\sqrt{12}$
1	1.875	0.559	0.161
2	4.694	3.506	1.012
3	7.854	9.819	2.834
4	10.995	19.242	5.554
5	14.137	31.088	9.182
n>5	$(2n-1)\pi/2$	$(2n-1)^2\pi/8$	$(2n-1)^2\pi/(8\sqrt{12})$

Case of the microbridge:

It can be demostrated that the boundary conditions in the case of a bridge study lead to:

$$cos(\beta_n L).cosh(\beta_n L) - 1 = 0 \qquad \text{Eq. A1.9}$$

Table A1-2. Constants values for the determination of the resonance frequencies for the first vibration modes of ideal microbridges.

n	λ_n	$\lambda_n^2 / 2\pi$	$\lambda_n^2 / 2\pi\sqrt{12}$
1	4.730	3.560	1.028
2	7.853	9.815	2.8336
3	10.995	19.242	5.554
4	14.137	31.808	9.182
5	17.278	47.516	13.717
n>5	$(2n+1)\pi / 2$	$(2n+1)^2\pi/8$	$(2n+1)^2\pi/(8\sqrt{12})$

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ANNEX 2: MEASUREMENT TECHNIQUES

In this section the basic measurement techniques are explained. These techniques are based on the working principles presented in *Chapter 2*.

Different methods were tested during this thesis. The first one consisted in determining the Young modulus of the film with a beam bending technique using an atomic force microscope (AFM) [1]. However, our first samples presented high roughness and the results from this method were difficult to interpret.
Therefore, the following methods consisted in using the mechanical resonance of the structures to determinate the mechanical properties of the layer and structures.

Mechanical (piezoelectric) excitation and optical detection

The working principle is simple: it consists on the use of a piezoelectric (PZT) actuator (shear or horizontal mode). The devices samples were glued on this PZT disk. By applying a sinusoidal voltage coming from a waveform generator to the PZT electrodes, we obtain vibrations of the whole sample. The sample vibration amplitude is lower than the PZT disk and is not know precisely, and mainly depends on the support nature and sample fixation. Single PZT disks from speakers are often useful to obtain vibration, but more efficient actuators can also be used depending on the resonance mode to actuate. We have used a glass plate as support, and the actuator is directly glued on it. To fix the sample, we have typically used a silver paint conductive solution directly on the actuator. A CCD camera coupled to an optical microscope or an automated automatic interferometric system [2] is used to measure optically the mechanical characteristics. With this set-up, we can actuate microstructures up to a frequency of some MHz, typically 2-3 MHz.

Figure 1. Zoomsurf 3D system from Fogale Nanotech. The sample is directly fixed on the PZT actuator which is glued on a glass plate.

One of the equipment we have used is the Zoomsurf 3D (figure 1) from Fogale Nanotech [3] which is an advanced white light interferometer system profiler. This system is basically constituted of a microscope with an interferometric objective, a waveform generator and a CCD camera connected to dedicated software performing all the calculation and control. The interferometric objectives are constituted of a classical objective and miniature interferometer. The sample acting as a mirror, the interferogram recorded by the camera is the result of the interferences between the reflected beam on the reference mirror and sample. In static mode, the interferometric signal is constituted

of fringes with period $\lambda/2$ where λ is the source effective mean wavelength. The vibrations produce a contrast reduction of the interference fringes (figure 2). By performing a quantitative analysis of the interference pattern contrast in static and dynamic mode, vibration mode shapes or vibration spectra can be measured. For vibration amplitudes lower than 120 nm, this analysis is fully automated.

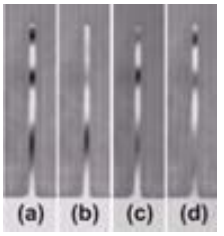

Figure 2. Static and dynamic averaged interferograms on a vibrating cantilever microbeam, (a) static, (b) 1st vibration mode, (c) 2nd vibration mode, (d) 3rd vibration mode.

Electrostatic excitation and optical or electrical detection

Figure 3 shows the main parts of the measurement set-up. An optical microscope equipped with a CCD camera connected to a computer allows recording the vibration. For direct on chip measurement, we have used a manual probe table Süss MicroTech PA 200 and RF probes. A network analyzer Agilent E5100A and a Keithley DC voltage source are used for the S21 measurements.

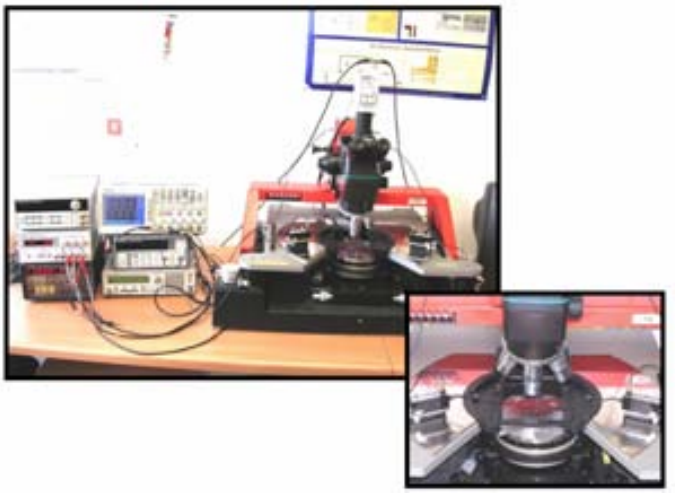

Figure 3. Set-up used for the electrical measurement of electrostatic microbeams.

S21 measurement involves the use of a network analyzer and a DC source to bias the mechanical resonator, as shown in the figure 4. The output of the network analyzer is connected to the excitation electrode and the input is connected to the read-out electrode, whereas the DC voltage source is directly connected to the resonator.
An interesting feature of the network analyzer is the calibration of the background signal. The parasitic signal originating from parasitic capacitances can be so high that the resonance peak is masked. The first step of the calibration procedure consists in

measuring the background signal by normally polarizing the resonator with VAC=0 and VDC=0 so that the resonator is not excited, thus measuring only the current produced by its parasitic and static capacitances. In real time, this background signal is subtracted to the newly recorded signal containing the resonance peak, thus highlighting it.

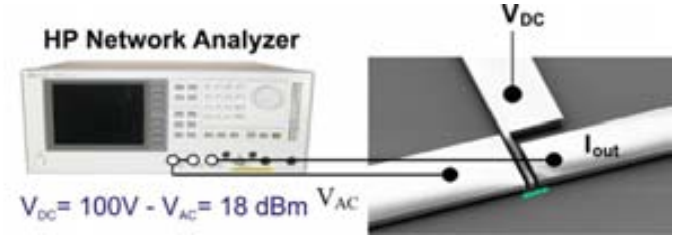

Figure 4. Direct S21 measurement connection.

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