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Modular multilevel converters for power system applications

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Doctoral Thesis

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MODULAR MULTILEVEL CONVERTERS
for power system applications

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Cover photo: Converter station hall of a HVdc transmission link between France and Spain, HVDC Plus IGBT converter modules for 1000 MW.

Não há nenhum caminho tranquilizador à nossa espera.
Se o queremos, teremos de construí-lo com as nossas mãos.

There is no easy path waiting for us.
If desired, we should build it with our own hands.

José Saramago

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pela compreensão, companheirismo, carinho e suporte manifestados durante esta agradável e inesquecível aventura.

Abstract

This thesis discusses the operation of the grid-tied modular multilevel converters (MMC) applied to dc power transmission, particularly in the medium and high-voltage applications. First, it is presented the evolution of the power converters used on the high-voltage dc transmission field (HVdc) with special focus on the modular multilevel-based power converters.

Then, due to the intrinsic nature of the converter, besides the control requirements for its dc and ac buses interactions, its energy storage should be carefully managed in order to achieve a safe and knowledgeable operation of this power converter. Hence, its control requirements are presented and mathematically supported. Moreover, the progressive design and validation of its control loops are addressed in this thesis by means of the converter simulation over a broad range of operating conditions.

One key-point factor of the MMC performance is the strategy followed to modulate the voltages generated on its arms. In this vision, different modulation techniques were combined with peculiar zero sequence signals in order to analyze their impact on the voltages across the converter arms and its intrinsic performance. This study was also complemented by different procedures followed to balance the energy storage of its capacitors. A transversal research question of this voltage source converter topology is its efficiency. Then, besides the analysis of the ac power flow impact on the power losses produced by its semiconductors, a mathematical expression is deduced and proposed that can describe the power losses produced semiconductors, over a broad range of the MMC's of operating conditions.

Finally, the possible degrees of freedom of an half-bridge-based MMC

are explored whenever it is operating in the static synchronous compensation (STATCOM) mode. Depending on the converter operation aspect requiring optimization, the voltage across its dc poles can be adjusted to achieve an improved performance of the MMC.

Resumen

La presente tesis trata del funcionamiento de los convertidores modulares de multinivel (MMC) usados en la transmisión de corriente continua, en particular en las aplicaciones de media y alta tensión. En primer lugar, se presenta la evolución de los convertidores de potencia utilizados en el campo de transmisión de corriente continua de alta tensión (HVdc) con especial atención a los convertidores de potencia basados en varios niveles.

Debido a la naturaleza intrínseca del convertidor, además de los requisitos de control para sus interacciones de los buses DC y AC, su almacenamiento de energÃa debe ser manejado cuidadosamente para lograr un funcionamiento seguro de este convertidor. Por lo tanto, sus requisitos de control son presentados y apoyados matemáticamente. Además, el diseño progresivo y la validación de sus bucles de control se abordan en esta tesis mediante la simulación del convertidor en una amplia gama de condiciones de funcionamiento.

Un factor clave del rendimiento del MMC es la estrategia seguida para imponer los voltajes generados en sus ramas. Por esta razón se combinaron diferentes técnicas de modulación con señales de secuencia cero para las ramas del convertidor y se estudió el rendimiento de este equipo. Este estudio también se complementó con diferentes procedimientos seguidos para equilibrar el almacenamiento de energía de sus condensadores. Una cuestión de investigación transversal de esta topología de convertidor de tensión es su eficiencia. Luego, además de la análisis del tránsito de potencia AC sobre las pérdidas de producidas por sus semiconductores, se deduce y se propone una expresión matemática que puede describir las pérdidas de potencia producidas por semiconductores, sobre una amplia gama de condiciones de fun-

cionamiento de la MMC. Por fin, se exploran los posibles grados de libertad de un MMC con submódulos basados en medio puente cuando está operando en el modo de compensación estática (STATCOM). Dependiendo de la operación del convertidor y la variable que se requiera para ser optimizada, se puede ajustar la tensión entre sus polos DC para lograr un desempeño superior del convertidor.

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Chapter 1

Introduction

1.1 Context

A DC grid based on multi-terminal voltage-source converter is a newly emerging technology, which is particularly suitable for the connection of offshore wind farms. Multi-terminal DC grids will be the key technology for the proposed European offshore SuperGrid.

At the moment, there is a lack of operational experience and of skilled engineers in DC grids in Europe. The Seventh Framework Programme of the European Union has provided funding to MEDOW to operate as a Marie Curie Initial Training Network. The network aims not only to address technical challenges but also to train and develop promising early-career researchers so as to form a pool of expertise in the field and to develop researchers with technical and transferable skills, private sector experience and an established network of contacts. This will give them the opportunity to undertake successful research careers with impact in a field in which is shaped by industry demand. It will also help to address the current and future skills shortage in power and energy engineering.

The network's research covers four broad areas: connection of offshore wind power to DC grids (work package 1); investigation of volt-

age source converters for DC grids (work package 2); relaying protection (work package 3); and interactive AC/DC grids (work package 4). MEDOW researchers are studying DC power flow, DC relaying protection, steady state operation, dynamic stability, fault-ride through capability, and the impacts of DC grids on ac grid operation. Systematic comparison of DC grid topologies, stability control strategies for offshore wind power transmission and onshore AC grid interconnection are been accomplished in various simulation platforms and experimental test rigs. The project's anticipated achievements will contribute to integrating offshore wind power into the onshore AC grids of European countries and to the European SuperGrid.

The MEDOW consortium consists of five universities and five industrial organizations. The combination of academic and private sector partners not only contributes to the individual researchers' training and development but also serves to foster greater ties between industry and academia in this important development area.

1.2 Objectives and scope of the thesis

The framework of the thesis it is focused on the investigation of voltage source converters for dc grids, particularly on the modular multilevel converter (MMC) performance, which is inserted into MEDOW's work package 2. Several operating aspects of the MMC are investigated in different chapters of the thesis in accordance with the structure pointed out in the Figure 1.1.

The analysis performed on the MMC for power system applications field responds to the following objectives:

- **Analysis the different voltage source converter (VSC) topologies introduced in the literature over the years to be applied on the high-voltage dc transmission field (HVdc).** A detailed description of the evolution of the VSC-HVdc topologies is given. Starting from the two-level VSC to the MMC solution, the current state-of-the-art, this study shows the

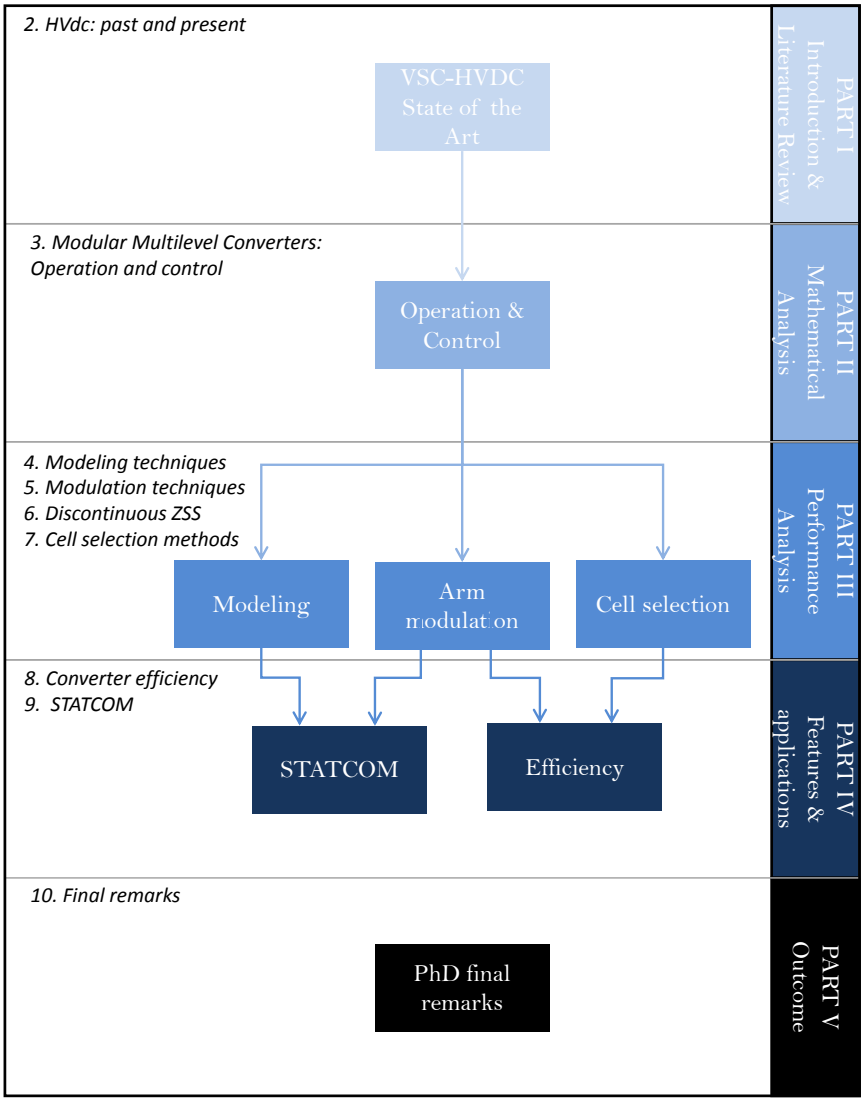


Figure 1.1: Thesis outline.

trend towards the half-bridge-based MMC systems. This objective is identified on the thesis structure as the "Part I: Introduction and literature review".

- **Design of the control loops for the three-phase-based modular multilevel converters.** Due to the converter complexity, first it is emphasized the electric variables that should be controlled in order to reach a safe and knowledgeable operation of this power equipment are emphasized. Then, in accordance with the control requirements of the MMC, the control methodology is described and mathematically supported. The control approach is then validated during the balanced and unbalanced grid voltage conditions. This goal comprises the Part 2 of thesis, namely the "Operation and control of the MMC".

- **Analysis of the time performance and accuracy of the MMC models.** The literature reveals that the complexity of the MMC models can be categorized in several groups from the most to the least accurate. This work analyses two common models and, in addition, two converter mathematical models and their features are proposed. The validation of those models is accomplished in simulation, by means of steady-state and ac fault behavior analysis. This task is included in the Part 3 of the thesis, specifically, the "Performance analysis of the converter".

- **Analysis of different modulation techniques applied to the medium voltage-MMC-based arm voltage orchestration.** A detailed description of several arm voltage modulations is presented. The study is based on the aggregation between several modulation schemes with different zero sequence signals injection, and the corresponding impact on the steady-state performance of the converter. The assessment consisted of analyzing its harmonic content, capacitor's voltage ripple and its global efficiency. This task is situated in the Part 3 of the thesis, specifically, the "Performance analysis of the converter".

- **Impact analysis of the different strategies followed to rotate the inserted capacitors on the converter performance.** The methodology used to balance the energy balance among the capacitors placed in the same stack greatly affects the converter performance. Therefore, several cell selection techniques present in the literature are studied. Moreover, a strategy is also proposed and validated that can further reduce the semiconductor's power losses and ergo increase the converter efficiency. This task is situated in Part 3 of the thesis, specifically, the "Performance analysis of the converter".

- **Mathematical model of the MMC-HVdc-based semiconductor's power losses.** The aim of this work is to propose a mathematical model that can describe the power losses produced by the MMC semiconductors over a broad range of steady-state operating conditions. Thus, a polynomial-based expression that reaches the estimation of the switches' power losses is concluded, and its parameters are adjusted in accordance with the power quadrant that the MMC is operating. This goal comprises Part IV of thesis, namely the "Features & applications".

- **Analysis of HVdc-design-based half-bridge MMC on the STATCOM operation.** In case of a strongly interconnected ac and dc network, the dc transmission grids are expected to be re-structured over the time in order to maximize the global power transmission efficiency. Therefore, it is expected that some MMC-terminals may get isolated from the dc grids and, hence, the voltage across their dc poles' becomes adaptable. This work investigates the degrees of freedom of the converter dc poles voltage in terms of the converter control and on its operation performance. Then, superior converter performance is achievable whenever its dc voltage value is adjusted. This objective is identified in the thesis structure as the "Part IV: Features & applications".

1.3 Thesis related work and activities

In this section, an overview of the chronological activities developed during the PhD thesis is outlined.

In October 2013, the author moved from Porto (POR) to Barcelona (ESP) to start his doctoral studies in the context of the MEDOW project. The author was hosted at the company designated as *Control Intel·ligent de l'energia* (short name CINERGIA). In addition, the PhD degree is being completed at the *Escuela Técnica Superior de Ingeniería Industrial de Barcelona* (ETSEIB) part of the Polytechnic university of Catalonia (UPC), in accordance with the MEDOW project agreement.

Since the start of the doctoral studies in Barcelona, the author followed his work-plan to different countries to undertake collaborative work with the various partners of the project. In particular with the Porto University (Portugal), Cardiff University (Wales-UK), KU Leuven (Belgium) and State Grid (China). From May to September 2014, the author received specific training at the Faculty of Engineering of Porto University, relating to the study of the power losses generated by the semiconductors. The study was complemented with the coaching in electro-magnetic transient Synopsis/ Saber software. The tasks developed by the author were related to the impact of the semiconductors model on the modular multilevel converter efficiency carried out in the Synopsis/ Saber software. From May to July 2015, the author was enrolled at Cardiff University to collaborate with local researchers. During this period, the author performed a comparative analysis between the frequency support provided by the conventional two-level converters and the modular multilevel converter. In May 2016 the author visited the China Electric Power Research Institute (CEPRI- State Grid) in order to finish a collaborative project between UPC and CEPRI related to simplified MMC models to reduce the simulation lengths.

In parallel to the training and research activities, the author was also assigned with the supervision of a dissertation carried out by a MSc student. The MSc dissertation focused on laboratory implementation of a full-bridge-based MMC cell.

Chapter 2

HVdc: past and present

The acceptance of high-voltage direct current (HVdc) technology in power grids is rapidly growing. Since the first HVdc link was commissioned in the 1950s, several projects and technologies have been developed and have embraced on this field, namely line-commutated converter (LCC) technologies (Classic HVdc) and the more recent self-commutated semiconductor based technologies (voltage source converter VSC).

Due to the intrinsic features of the LCC and VSC technologies, the former have grown in the HVdc field, either in voltage and power ratings. As a result, converter stations have become more efficient along the way. LCC technology is by far the most mature solution for transporting power over large distances. However, due to the recent developments in multi-terminal dc grids and the introduction of the modular and multilevel converter, VSC-based technologies also play an important role on the field.

2.1 HVdc evolution

Electric conversion from ac to the dc field started in the late 19^{th} century. By 1880 Thomas Edison was trying to improve incandescent light bulb filaments so as to have more durable materials and longer lifetimes. However, in one of his experiments where he was trying to understand the reason for the uneven blackening of bulbs in his incandescent lamps, he added a metallic foil to the bulb (darkest near the positive terminal of the filament) and connected it to the positive pole

of a voltage source (see Figure 2.1). With his action, Edison surprisingly discovered the flow of an electric current on the added foil. The existence of this electrical current exceptionally when the metallic base was connected to the positive pole of the battery, was classified as the first attempt of an unidirectional current flow converter: namely an ac to dc converter [1].

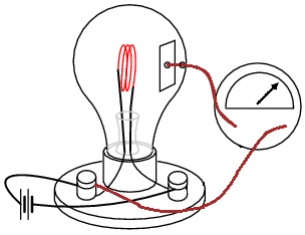


Figure 2.1: Circuit demonstrating the Edison effect.

This effect was further studied and explored by several physicians such as Owen Willans Richardson (1900) and Peter Cooper-Hewitt who added mercury gas into the bulb and improved the light bulb developed by Edison in 1901 [2]. This development started the roadmap of the mercury-arc-based rectifiers. However, the technology breakthrough was not smooth and several power electronic devices were developed afterwards. In 1957, silicon-based power electronic devices were introduced, namely the thyristor [2, 3]. The development of the insulated-gate bipolar transistor (IGBT) in the late 1980s also started the voltage sourced converter trend in the field of HVdc [4].

The next sections present the major breakthroughs in the HVdc field due to the evolution of conversion methods settled by mercury arc valves, thyristors (HVdc classic) and IGBT-based (VSC-HVdc) power converters.

2.1.1 The Mercury-arc valve HVdc System

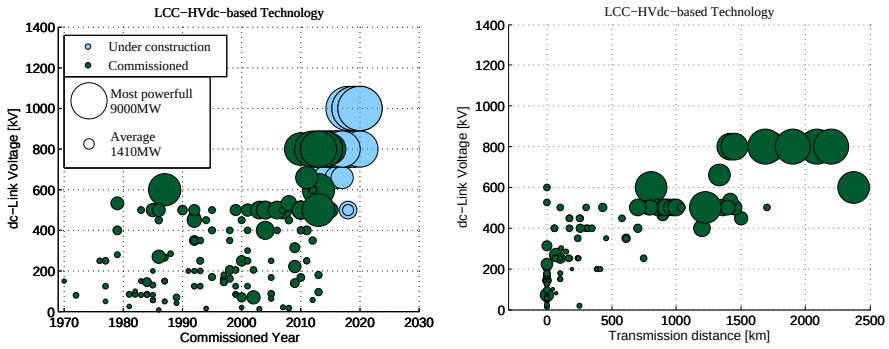
The development of mercury-arc valves started opening new horizons, such as power transmission in dc. Due to its construction limitations,

several challenges arose in experimental projects that motivated ongoing development of the technology until the first commercial HVdc link was commissioned in Germany, named the Elbe-Project [3, 5, 6] in 1941. As mercury-arc valves were maturing, namely the development of the power and voltage rating of the devices, the power converters were capable of transmitting more power. This fact was progressively developed and it reached its golden years in the 1960s with the highest rated power and transmission line voltage project achieved in the *Pacific DC Intertie* HVdc link with 1.62 GW and ±400 kV respectively [7]. However, the development of the semiconductor-based switches changed the paradigm of the HVdc.

2.1.2 HVdc classic

The introduction of silicon-based devices changed the paradigm of power transmission. Low on-state voltage, short-duration pulse in gating circuitry, better temperature characteristics (silicon temperature up to 175^oC) and higher power controllability of thyristor devices rather than the mercury-arc valves all marked a new era in the HVdc [6].

As the technology matured and most of the challenges were overcome, thyristors were examined in operation in the real Gotland HVdc link in 1967. By that time the converter was operating with mercury-arc valves, and one of valves of the inverter station (50 kV/220 A) was replaced by two parallel stacks of thyristors. The success and the experience acquired with this attempt, led to changing all the mercury-arc valves in the Gotland HVdc link to thyristors in 1970. This upgrade led to an increase of transmitting capacity from 20 MW to 30 MW and started the era of the thyristor-based HVdc links (or line commutated converters-LCC), as illustrated in Figure 2.2 [6, 8]. In subsequent years new LCC-HVdc projects came about and the replacement of mercury-arc valves technology took place. The major technology leap happened with the *Itaipu* project in 1985, which significantly increased the voltage rating and power transmission capability of the converter stations and for more than two decades held the record for the highest power transmission capability link (6.3 GW) and direct voltage (± 600 kV) [9].



(a) (b)

Figure 2.2: Overview of the worlwide LCC-HVdc projects: (a) commissioned year and (b) transmission length.

In 2010 another technology breakthrough was reported, namely the availability of converter terminals with dc voltage ratings higher than ±600 kV. Since then, several HVdc links have been created in India and China with the direct voltage of ± 800 kV and rated capacity of 8 GW [9–11]. In 2013 the Rio Madeira HVdc link (Brazil) was commissioned, which is the actual holder of the dc transmission line length record of 2400 km. Although these numbers are already quite impressive, they will be further improved in coming years with the introduction of a new LCC generation with direct voltage of ±1100 kV, which allow to step up the power ratings up to 10 GW and, thus, it can viably extend the transmission line lengths up to 3000 km [9]. The evolution of the LCC-HVdc-based links, especially on the recent years, clearly shows that the solution is mature and very interesting for bulky power transmission over really large distances, due to its efficiency and robustness [12]. Currently, there are more than 100 LCC-HVdc projects in operation from the 100 MW to 10 GW range [5].

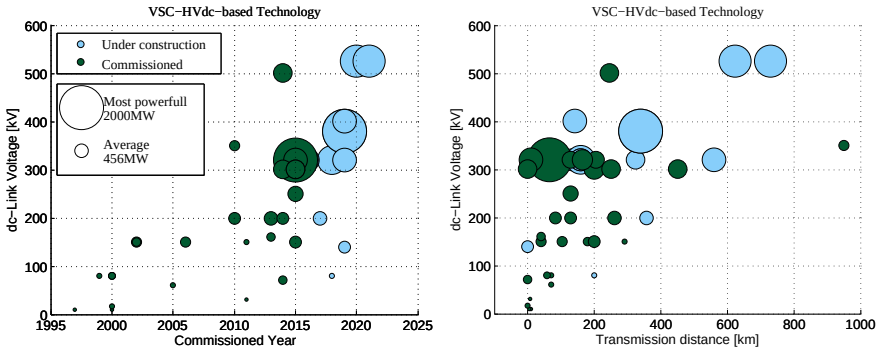
2.1.3 VSC-HVdc

With the development of power semiconductor components, new devices with interesting features were introduced, such as insulated gate bipolar transistors (IGBT). These self-commutating switch devices have

the possibility of being opened or closed directly, enabling an increase in switching frequency in respect to the line commutated converters. By means of a proper switching scheme, the VSCs synthesize a stepped-voltage waveform at their ac bus and they modulate the necessary fundamental voltage waveform at the output terminals appropriately. Depending on the topology chosen for the VSC, a converter station can be achieved with few voltage levels with a high switching frequency or a multilevel based solution with reduced switching frequency. Either ways, the harmonic content of the currents managed by the VSCs can be more easily filtered when compared to the LCC-based terminals. As a result, the VSC require fewer ac filters either in number or in size [13, 14]. The motivation to reduce the substation footprint is particularly important when it comes to the discussing the offshore substations linked to the wind farms through HVdc lines.

The fact that the IGBTs are characterized by their non-grid dependency to operate permits the independent control of active and reactive power flow between the converter terminals and the ac network. Adding the fact that these semiconductors require low power demand in their gating circuitry to operate a new highway on the HVdc field has been opened dedicated to the VSCs [13, 15].

The introduction of VSCs on the dc power transmission field took place in 1997 with a two-level converter (2L-VSC), at this time a small scaled demonstration project capable to transmit 3 MW along the 10 km between Hällsjön and Grängesberg (Sweden) in a ± 10 kV line [16, 17]. This demonstration project initiated the VSC-HVdc road-map until the present time as illustrated in Figure 2.3. After verifying the power transmission with the VSC concept, the first commercial VSC-HVdc link was materialized in Gotland (Sweden) in 1999. The consequent years were remarkable, and new VSC structures were adopted to the power transmission field, new modulation techniques were developed and the semiconductor devices were improved, either in voltage ratting and efficiency (see Figure 2.4). The second VSC-HVdc generation started with a three-level VSC with the neutral point clamped (3L-NPC) structure, and was used in the Eagle Pass (USA) project [18–20].



(a) (b)

Figure 2.3: Overview of the worldwide VSC-HVdc projects: (a) commissioned year and (b) transmission length.

The introduction of an additional voltage step on the VSCs by the 3L-NPC, besides reducing the load stress, allowed the converter switching frequency to be reduced, which became slightly more efficient than the previous VSC generation. However, the voltage balancing challenge of the dc capacitors and the uneven loss distribution between the semiconductor devices were some factors that led to the later downgrade from three-level-based VSC to the 2L-VSC. Nonetheless, this generation was characterized by an improved modulation strategy applied to the semiconductor devices [21–23]. Later on, a new multilevel converter structure was tested and reached a new higher level of efficiency achieved by VSC-HVdc solutions, the modular multilevel converter (MMC). At this stage, which is the so-called fourth MMC generation, the converter losses equals 1 %, the minimum so far achieved by the VSCs [24]. It was first commercialized in 2010 in the *Transbay Cable* project and, since then, the number of MMC-HVdc-based projects commissioned is increasing worldwide [25–32]. Due the clear improvements shown by the MMC generation, more than ten projects have been recently proposed and/or are currently in the construction stage [32, 33], which clearly shows its importance to the HVdc field.

In the following sections the performance of the aforementioned VSC-HVdc generations is briefly presented [34, 35].

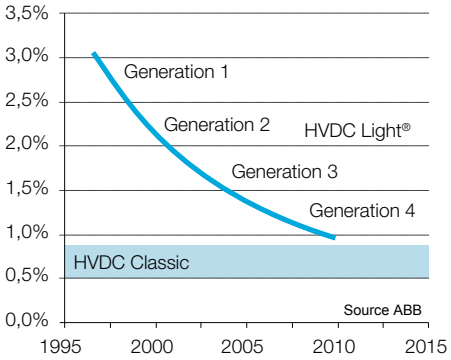


Figure 2.4: Power losses evolution of the VSC-HVdc terminals [12].

Two level converters

The first VSC attempt on the HVdc field was based on the two-level converter (2L-VSC) displayed in Figure 2.5. Each leg of the converter

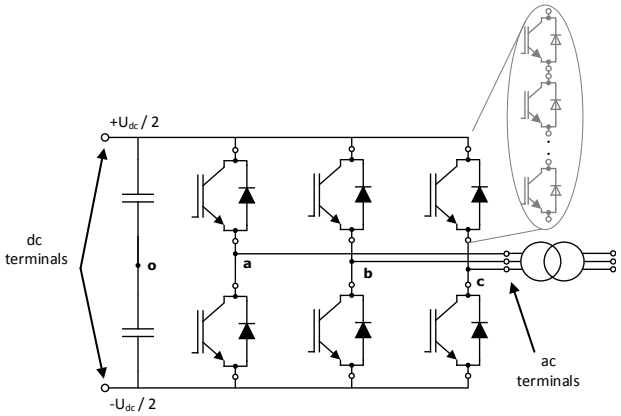


Figure 2.5: Three-phase circuit of the two-level VSC.

is composed of two stacks of IGBTs, respectively protected by its anti-parallel diode. The stacks are thereafter linked in parallel to a set of charged capacitors placed at the converter's dc terminals. The mid-point of each leg can be connected to the to the positive $(+U_{dc}/2)$ or negative $(-U_{dc}/2)$ pole of the dc-bus by either closing the upper or lower stack respectively. Since there are only two voltage values admissible at the midpoint of the leg (in respect to "o"), it accordingly

defines the name of the converter scheme. The states of the switches are progressively swapped with a high frequency approach[1], and therefore a stepped voltage waveform is created in v_{jo} ($j \in \{a, b \text{ or } c\}$). The pulse width modulation strategy applied to the switches allows the voltage modulation in amplitude and phase angle in v_{jo}, as shown in Figure 2.6. The stepped voltage at the ac bus of the converter is decoupled from the ac grid by means of an inductance (modeled as the leakage inductance of the transformer), which is also responsible for filtering the current that flows in its ac bus, thus reducing its harmonic content. With a suitable control strategy, the states of the switches are consequently managed in order to synthesize the required ac voltage at v_{jo} and therefore the active/ reactive power flow between the converter and the network.

Later, in the third VSC generation, some improvements were made in the voltage modulation of the 2L-VSCs [12, 22]. An optimal pulse width modulation (OPWM) strategy was implemented and it successfully reduced the average switching frequency of the 2L-VSC to 1150 Hz. This advance characterized the third VSC-generation, which was more efficient than the previously discussed 2L-VSC (first VSC-HVdc generation) and the three-level-based VSC (second VSC-HVdc generation), which will be presented in the next section.

[1]The Swedish demonstration project *Hellsjon* was based on a 2L-VSC, whose switching frequency was designed for 2 kHz [36].

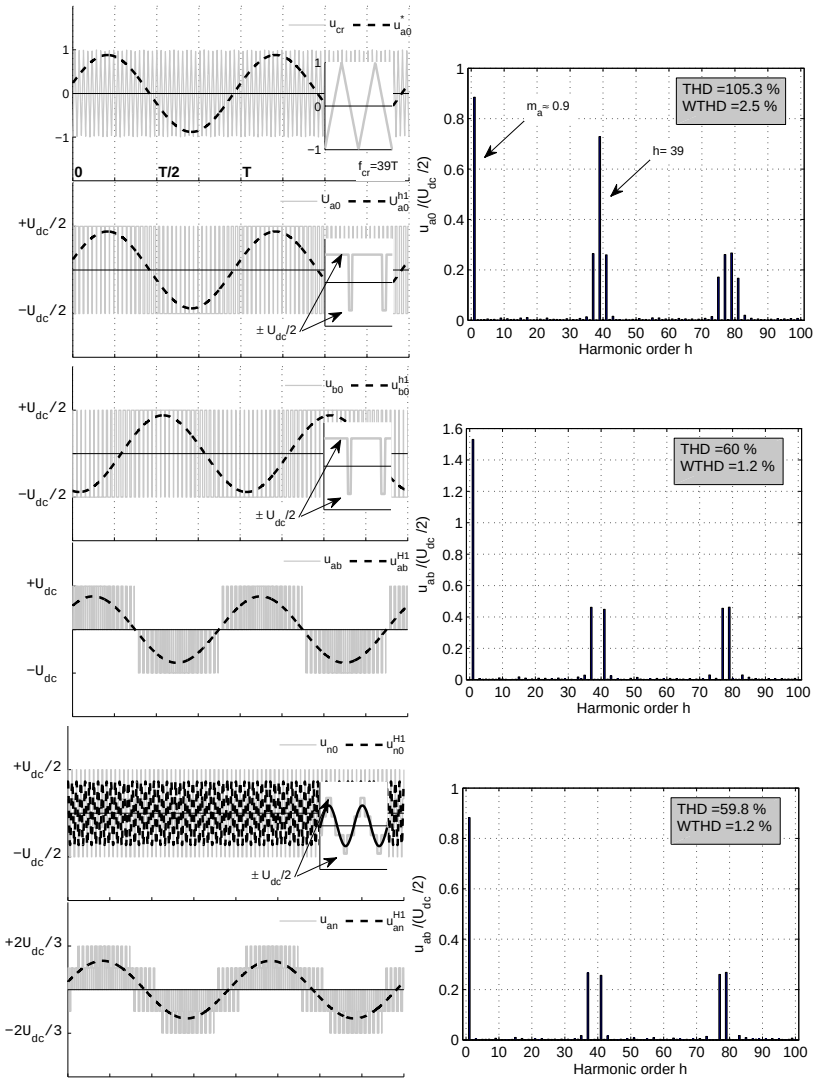


Figure 2.6: Operation of the 2L-VSC in the linear region[2].

[2]Simulation accomplished with the asymmetrical regular sampled PWM [37].

Three level converters

The second VSC-HVdc generation is composed of the three-level neutral point clamped (3L-NPC) VSC, which is illustrated in Figure 2.7. Although the number of semiconductor devices were increased, the addi-

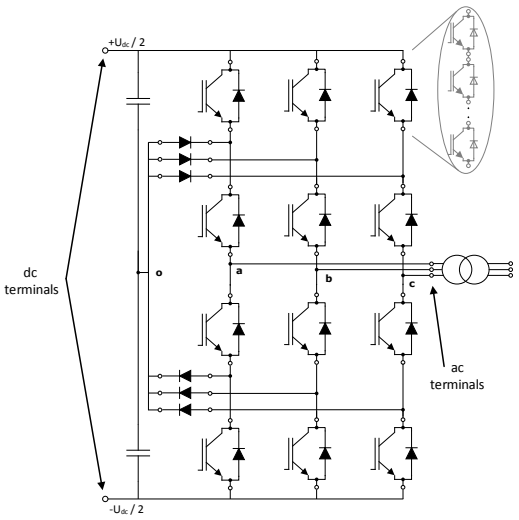


Figure 2.7: Three-phase circuit of the 3L-NPC VSC.

tional voltage step present in u_{j0} ($j \in \{a, b \text{ or } c\}$) permits the reduction of the switching frequency to 1.5 kHz [19,38]. Hence, it globally reduces the losses produced in comparison to the first VSC generation [12]. The 3L-NPC structure has a major drawback which is the uneven loss distribution among the semiconductor devices [39, 40]. During the state that the point o is connected to the point j, this is inevitably done through the upper or lower clamping diodes in case of positive or negative current flow respectively. Depending on the power factor, those devices can hit the thermal limits and therefore restrict the maximum power flow on the converter. Some records are found that reveal that the clamping diodes were replaced by IGBTs switches (active NPC), which have two redundant states more than the NPC in its standard version. The choice of the most suitable redundant state, among the four available, is accomplished in such a way that reduces the junction temperature deviation among the clamping devices [41]. This fact ex-

tends the limits of the NPC converter, however, the normalized total losses generated by the ANPC is nearly equal to the ones quantified by the NPC [41].

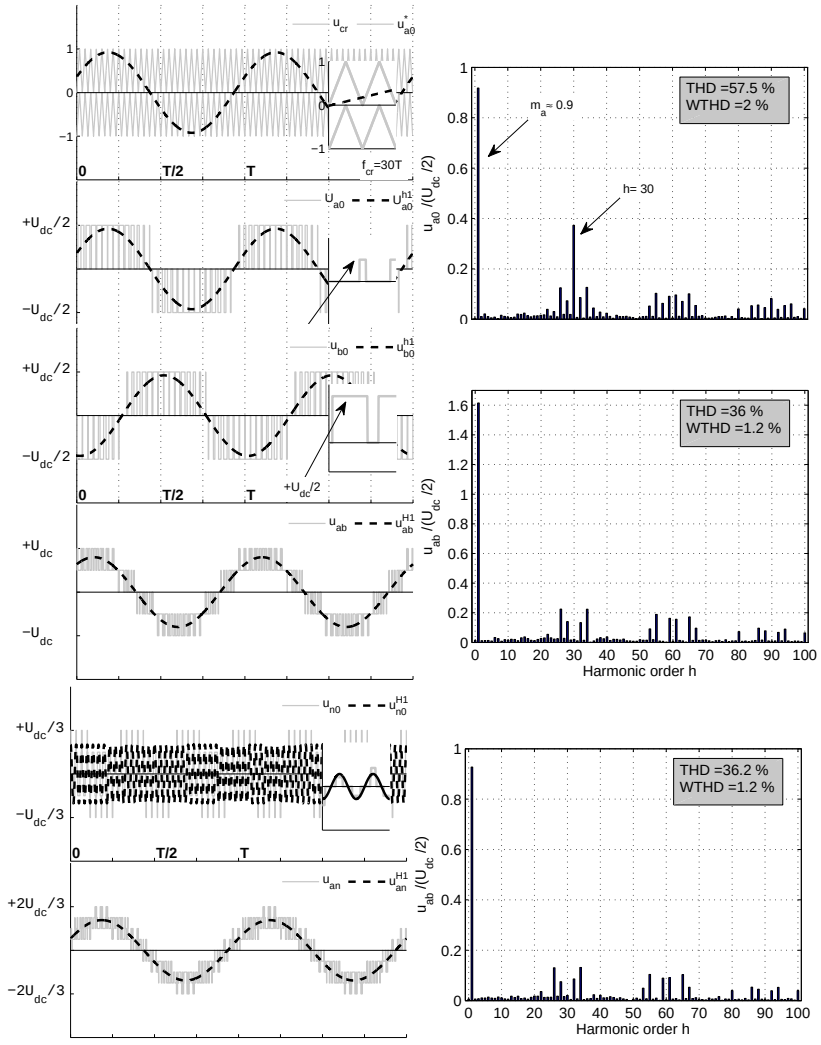


Figure 2.8: Operation of the 3L-NPC in the linear region[3].

[3]Simulation accomplished with the asymmetrical regular sampled phase disposition PWM scheme [37].

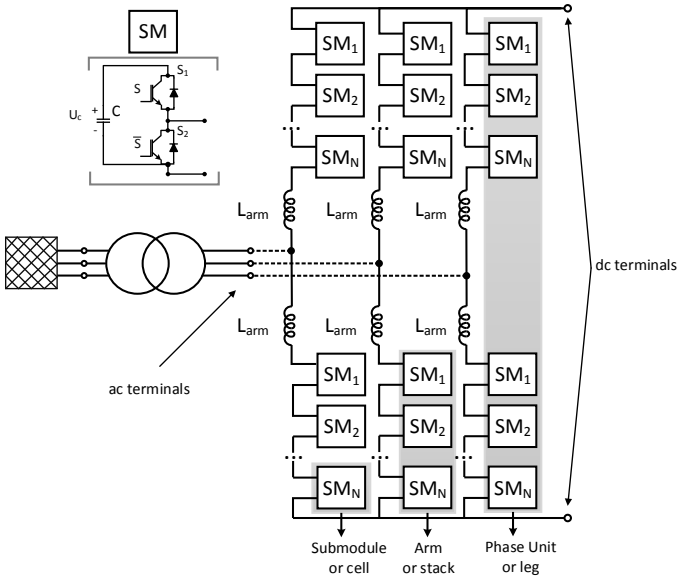


Figure 2.9: Three-phase circuit of the modular multilevel converter.

Modular and multilevel converters

Currently, the fourth VSC-HVdc generation is the modular multilevel-based converter (MMC) structure, introduced in 2001 on the HVdc field [42, 43], and commercialized in 2010 in the Trans Bay project [25, 44]. The sketch of the MMC structure is illustrated in Figure 2.9. The converter is composed of the series connection of small-scaled power converters designated as submodules (SM) or cells. In opposition to the previous versions of VSC-HVdc projects, in which the semiconductors were aggregated in series, on the original-version of the MMC hundreds of series-connected choppers were used. The series connection of the submodules are typically designated as stacks or the arms of the converter.

The operating principle of this converter structure is the variation of the series-connected number of low-voltage-rated capacitors over the time in each arm, by means of IGBT-based switches present on the SMs. As the number of inserted capacitors increases, more voltage steps are available at the stack's voltage and accordingly at the converter

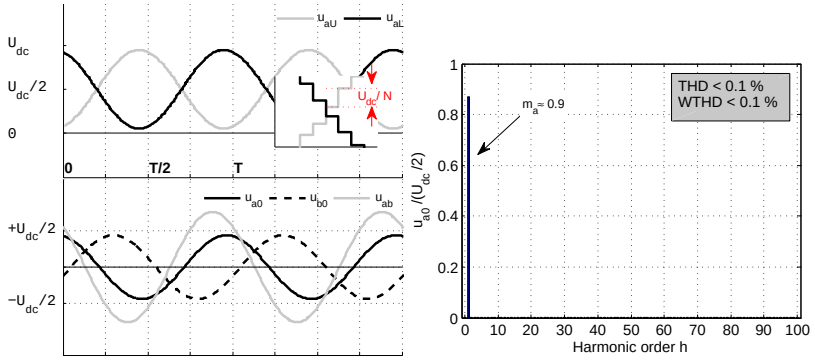


Figure 2.10: Operation of the 400 level-based MMC in the linear region[4]

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[4]The arm voltages were modulated according to the nearest level control (NLC) [45], combined with the cell selection procedure presented in [43].

output. The main achievement of this converter structure is that it overcomes the challenge of simultaneously firing the series connection of semiconductor switches, the bottleneck of the previous VSC-HVdc solutions. Moreover, the capacitors and the semiconductor switches of the cells are then designed to withstand only few kV (less than 2 kV), a common voltage rating value in the market. For this reason the structure does not employ capacitors in the dc-link and the voltage between the dc poles is managed accordingly with the inserted number of SM's capacitors on each converter leg. In this view, its modular nature permits a flexible design to suit the particular characteristics of each HVdc project. Once a SM design is achieved, the adaptation between MMC-HVdc-based projects is done by adjusting the suitable number of SMs assembled in each stack.

Furthermore, due to the fact that each capacitor is responsible for a particular voltage step on the converter arms, a MMC composed of hundreds of SMs generate relatively low harmonic content on its ac voltage, as shown in Figure 2.10. This is particularly important because this VSC requires fewer ac filters than the previous VSC-HVdc solutions [20, 43]. Furthermore, due to its exceptional output voltage, its average switching frequency is noticeably small, more specifically, each IGBT

commutates between 4 and 8 times (100 to 200 Hz), being responsible for generating up to 1 % of total losses [25].

Due to their interesting properties and the clear improvement shown by the MMC generation, several MMC-HVdc-based projects have been proposed and/or are under construction to reinforce local grids, connecting offshore wind farms and interconnecting different grids, as illustrated in Table 2.1. The data shown clearly emphasizes the MMC importance on the HVdc field because it comprises 31 out of the 43 VSC-HVdc projects presented in Figure 2.3. Due to its clear relevance to the topic, the operation of the MMC was studied in the present text and the basic operation of the MMC is described in the following section.

Table 2.1: MMC-HVdc worldwide projects.

Company	Project	Power (MW)	DC link (kV)	Length (km)	Commissioning year	Application
Siemens	TransBay (USA)	400	± 200	94	2010	Grid reinforcement
	INELFE (ESP/FRA)	2000	± 320	65	2014	Grid reinforcement
	SylWin1 (DEU)	864	± 320	205	2014	Offshore connection
	HelWin1 (DEU)	576	± 250	130	2014	Offshore connection
	BorWin2 (DEU)	800	± 300	200	2014	Offshore connection
	Helwin2 (DEU)	690	± 320	130	2015	Offshore connection
	ElecLink (GBR/ FRA)	1000	± 320	70	2019	Interconnecting grids
	BorWin3 (DEU)	900	± 320	160	2019	Offshore connection
	NEMO (GBR/ BEL)	1000	± 400	140	2019	Interconnecting grids
	COBRA (DEU/ DNK)	700	± 320	355	2019	Grid reinforcement
	Ultranet (DEU)	2x1000	± 380	800	2020	Grid reinforcement
ABB	DolWin1 (DEU)	800	± 320	165	2014	Offshore connection
	Mackinac (USA)	200	± 71	B2B	2014	Grid reinforcement
	Skagerrak 4 (DEU/NOR)	715	± 500	244	2014	Interconnecting grids
	NordBalt (SWE/LTU)	700	± 300	450	2015	Interconnecting grids
	DolWin2 (DEU)	900	± 320	135	2016	Offshore connection
	Maritime Link (CAN)	500	± 200	170	2017	Grid reinforcement
	Caithness Moray (GBR)	1200	± 320	160	2018	Grid reinforcement
	Johan Sverdrup (NOR)	100	± 80	200	2018	Offshore oilfield
	Krigers-Flak (DEU-SWE-DNK)	410	± 140	B2B	2019	Offshore connection
	NordLink (DEU/NOR)	1400	± 525	623	2020	Interconnecting grids
	NSN (GBR/NOR)	1400	± 525	730	2021	Interconnecting grids
Alstom/GE	Tres Amigas (USA)	2250	± 300	B2B	2014	Interconnecting grids
	SouthWest (SWE)	1440	± 300	200	2015	Interconnecting grids
	DolWin 3 (DEU)	900	± 320	162	2017	Offshore connection
	Atlantic Wind (USA)	3000	± 320	Planning	2019	Offshore connection
C-EPRI	Shanghai Nanhui (CHN)	18	± 30	8	2011	Demonstration Project
	Nan'ao (CHN)	200	± 160	4 terminals	2013 (3T)	Grid reinforcement
	Zhoushan (CHN)	1000	± 200	5 terminals	2014	Grid reinforcement
	Xiamen, Fujian province	1000	± 320	10.7	2015	Demonstration Project
	Dalian (CHN)	1000	± 320	47.6	Postponed	Grid reinforcement

2.2 Modular Multilevel Converter

2.2.1 Original structure - Siemens AG version

The original scheme of the three-phase circuit of the MMC structure is shown in Figure 2.11 [46]. Each phase unit is composed of two stacks

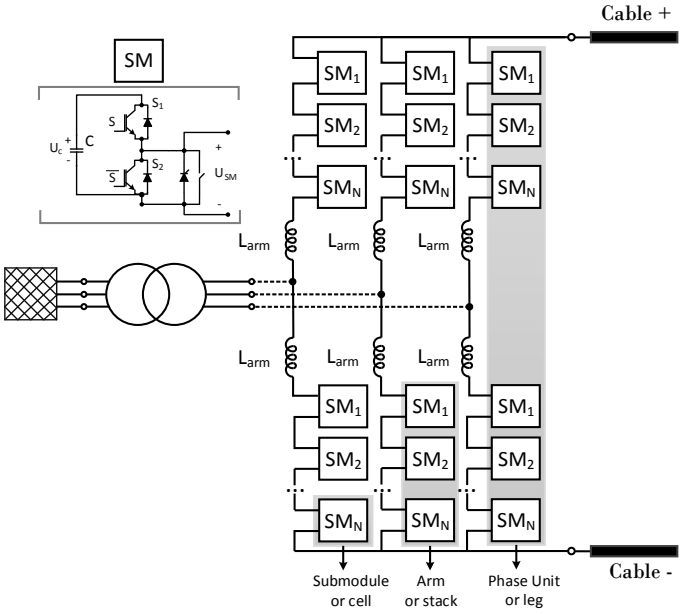
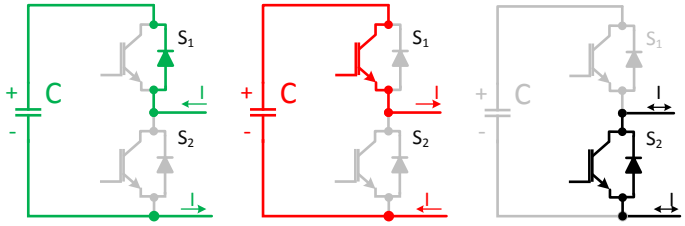


Figure 2.11: Modular multilevel converter version of Siemens AG.

of N small-scaled power converters, with half-bridge (HB) topology. The chopper switches S_1 and S_2 are controlled to either connect or bypass the charged capacitor C to/from the terminals of the cell. The firing pulses of the switches are then managed by the logical signal S. Logically, both switches cannot be simultaneously closed, otherwise a short-circuit of the capacitor would occur. If the control signal S carries the logical value *high*, the switch S_1 becomes closed (S_2 open), which directly connects the capacitor to the SM terminals. Then, its stored energy varies according to the correspondent arm current flow. On the other hand, if S takes the logical value *low*, the lower switch S_2 is closed (S_1 open), which short-circuits the SM and the capacitor is

(a) (b)

Figure 2.12: Submodule realization of the MMC by Siemens Ag: (a) layout and (b) the stacks realization at the INELFE project.



(a) (b) (c)

Figure 2.13: States of an HB cell: the capacitor is (a) charging, (b) discharging or (c) removed from the SM output.

removed from the correspondent stack current flow. The realization of the Siemens HB-cell is shown in Figure 2.12 [47]. The states of the HB cell are illustrated in Figure 2.13. The duty cycle of the logical signal S combined with the stack current has a tremendous impact on the stored energy of the SM capacitors.

A suitable control strategy is compulsory to guarantee the stable operation of the converter. Since the HB-cell only admits two non-negative values at its terminals, namely zero or its capacitor voltage, the voltage generated at each stack can vary from zero to the voltage sum of all the stack capacitors. Therefore, the SM states of each leg are controlled in such a way that synthesizes an ac voltage at the correspondent converter bus, as well as, the necessary dc voltage at the corresponding dc bus.

Additionally, due to the parallel connection of the converter legs, the voltage of the inserted capacitors in each phase unit must be controlled otherwise inrush currents may flow to/from the dc bus or to/from the remaining legs of the converter. However, thanks to the arm inductors, the voltage sum of the inserted capacitors in each leg is then decoupled. Moreover, those inductors permit the electric current flow between legs to be controlled, as well as, the rise rate limitation of the arm currents in a short-circuit event on the dc-side of the MMC [48].

Due to the series connection of the HB submodules (HBSM), if a fault occurs on the dc-side of the converter, the anti-parallel diodes will become forward biased and power will flow from the ac to the dc sides of the converter. As a consequence of the fault identification, the control signals of the semiconductors S_{jki} are set to the logical value *low* which removes the IGBTs and the capacitors from the fault current path. Moreover, in order to protect the submodules, a thyrisitor device is activated which accordingly pulls out the remaining on-state semiconductors of the SM. Therefore, until the fault is cleared either by a dc circuit breaker (DCCB) or by an ac breaker, the thyristors are kept closed and the equivalent circuit of the converter is a diode-bridge rectifier.

On the other hand, if a malfunction is detected in one of the SMs, to ensure the continuous operation of the converter, and considering that the converter was designed with redundant cells, the SMs are also equipped with an electromechanical breaker which mechanically bypasses the corresponding cell from the current path if a malfunction is detected. Consequently, a redundant SM will replace the deteriorated module and the converter can operate without any interruption [46].

2.2.2 Cascaded two level (CTL) structure - ABB AB version

The manufacturer ABB decided to develop the cascaded two level (CTL) version of the MMC due to its long experience in developing VSC-HVdc converters based on series-connected and simultaneous switching IGBTs. In opposition to the single-switch-based HBSM

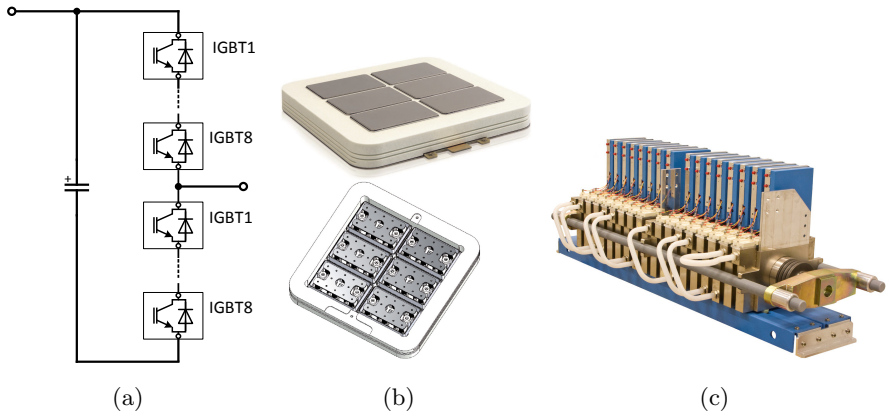


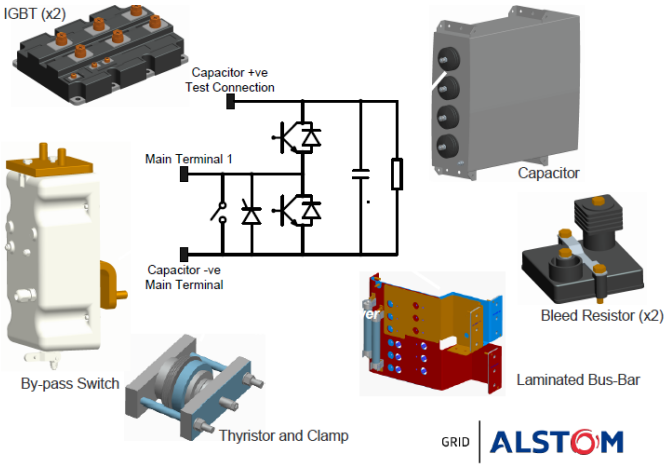
Figure 2.14: SM realization of the CTL converter by ABB AB: (a) layout, (b) IGBT module (press-pack) and (c) construction.

chopper proposed by Siemens AG, on the CTL converter the chopper switches comprise eight Press-Pack switches, as emphasized in Figure 2.14. Particularly to the IGBT modules, ABB uses the press-pack (StakPak) modules, which are optimized devices to be electrically connected in series. Moreover, if one IGBT device has a failure, due to its construction, it enters a short-circuit failure mode (SCFM), a critical feature in series-connection applications. Moreover, as can be seen in Figure 2.14(b), the StakPak IGBT module is composed of multiple parallel chips[5], which are in practice also multiple IGBTs connected in parallel in order to reach high current-rated devices. Figure 2.14(c) also illustrates the creation of a CTL-based chopper with eight IGBT press-pack modules. Moreover, the nominal voltage of this SM solution is 17.6 kV [49]. Therefore, for the same dc-link voltage terminal, the CTL converter has a much lower number of HBSMs when compared to the Siemens AG MMC-based version.

[5]In case of Figure 2.14(b), six IGBTs are connected in parallel. In the portfolio of ABB can be identified StackPak packages with 3 and 4 parallel connected IGBTs.

2.2.3 Modular Multilevel structure - Alstom Grid version

The Alstom Grid is also a worldwide player in providing HVdc solutions. Furthermore, Alstom Grid has developed its own half-bridge-based MMC solution as shown in Figure 2.16. It is worth mentioning that the SM switches are based on HiPak modules of IGBTs and the SM main components depicted in the figure are similar to the original version of the MMC [50]. As can be observed in Figure 2.15(b), approximately half of the SM volume belongs to the capacitor. Moreover, to be at the vanguard of technology, Alstom Grid also developed a Medium voltage/power demonstration project at its Stafford headquarters (GBR), as illustrated in Figure 2.16 [51].



(a)

(b) (c)

Figure 2.15: SM creation of the MMC by Alstom Grid: (a) main components; (b) frontal and (c) rear panel of the submodule.

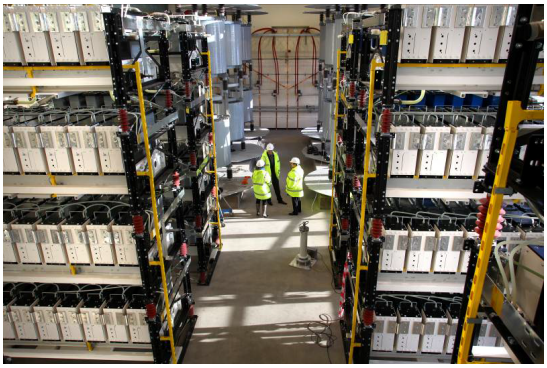


Figure 2.16: MMC demonstration project in Alstom Grid facilities.

Alstom Grid also proposed a hybrid MMC-based solution designated as alternate arm converter (AAC). It follows the overall structure of the original version of the MMC, but based on the series-connected full-bridge SMs (FBSM) in series with a direct switch [52]. Furthermore, the operation of this converter diverges from the original MMC, and so was not investigated in this text.

2.2.4 Basic Operation of the MMC

The MMC can operate as a bridge between ac and dc grids, and besides the intrinsic requirements of that feature, it should have additional control algorithms to balance the overall energy storage deviation between the SM's capacitors, and between its arms and legs. Therefore, it reveals an increased control complexity compared to previous VSC-HVdc generations due to its decentralized way of storing energy. The fundamental stages of MMC control are briefly explained in this section.

As mentioned, a suitable number of capacitors should be inserted into each phase unit to impose the voltage across the dc poles of the converter. In opposition, the number of inserted capacitors in each arm should be variable, in order to synthesize the proper ac voltage at the ac converter bus. Figure 2.17 briefly illustrates the converter operation with four HBSMs assembled in each converter arm (N=4).

The picture describes how the selection of the cell states affects the

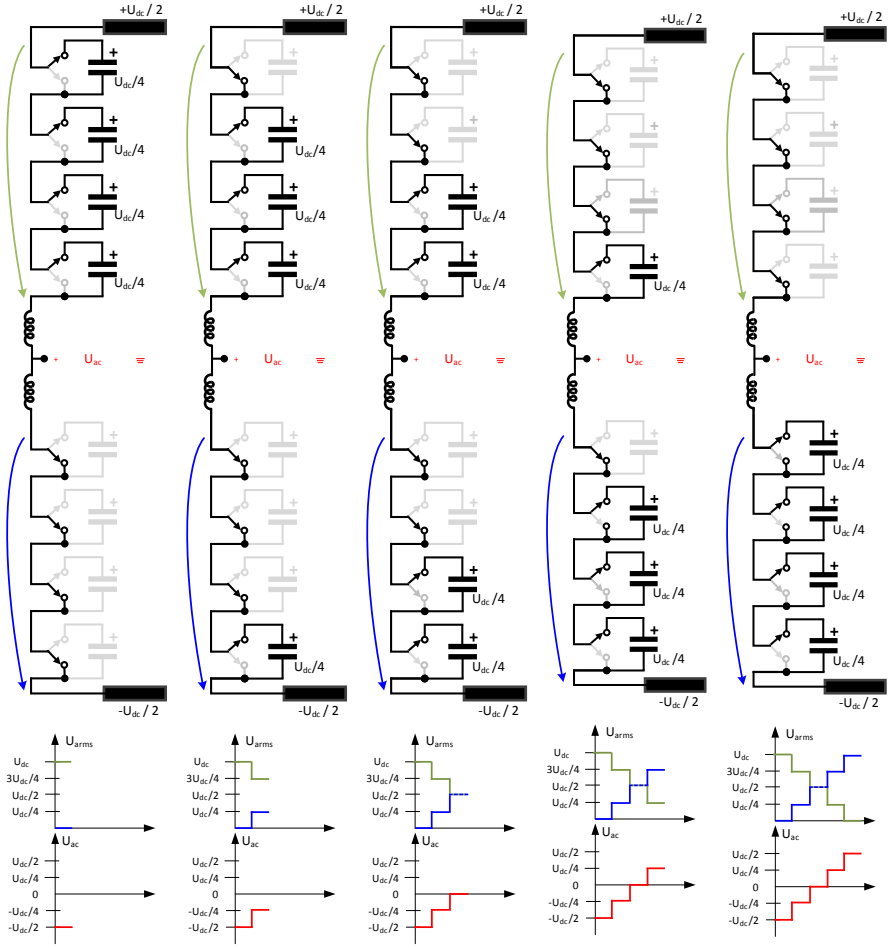


Figure 2.17: Basic operation of the MMC with four cells per arm.

voltages across the converter arms and on its ac bus. Considering that the voltage across each particular capacitor is fixed and equal to $(U_{dc}/4)$, four capacitors are required to be inserted in each leg of the converter. Then the voltage at U_{ac} is managed by varying the ratio of the inserted capacitors between the upper and lower arms. To accomplish this goal a convenient control strategy is compulsory for the MMC.

Whenever the converter operates in inverter mode, as presented in

Figure 2.18, the upcoming current from the positive dc terminal (blue) is obliged to spread over the converter legs, which consequently converge into the negative dc pole. Taking into account that several capacitors are inserted into its legs, the portion of the dc current flow will globally charge the capacitors of the converter. Eventually the converter control will reflect the energy surplus and will regulate the ac power injection to maintain the total energy storage at the nominal conditions. Due to the large current fluctuation on the converter arms and in their equivalent capacitance, it causes an asymmetric charging trend among the stacks which should be compensated by the converter controllers to be properly operated. Therefore, at steady state operation, the incoming power from the dc bus should be re-directed to the main ac grid in order to maintain the energy storage on the converter equal to its nominal conditions. Thus, to compensate the alleged energy storage deviations between the converter arms/ legs, internal currents should be controllably imposed to circulate on the converter legs to overcome this defect, and accordingly cancel the deviations referred to.

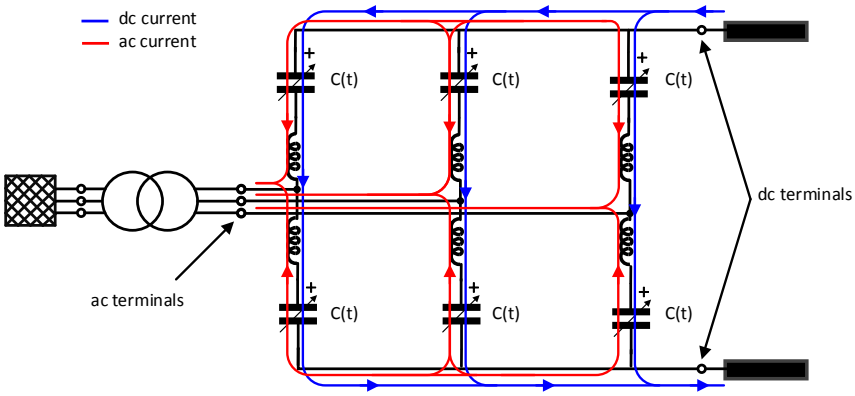


Figure 2.18: Power flow on a grid-tied MMC.

Overall control diagram

Besides the ac/dc interactions control, as in the previous VSC-HVdc versions, when it comes to the MMC control, additional control loops should be considered. This is justifiable with the need for its internal energy storage dynamics control to guarantee an uniform energy distribution storage between the converter legs, stacks and cells. Hence, the overall control scheme of the modular multilevel converter is summarized in Figure 2.19. According to the figure, three main levels of

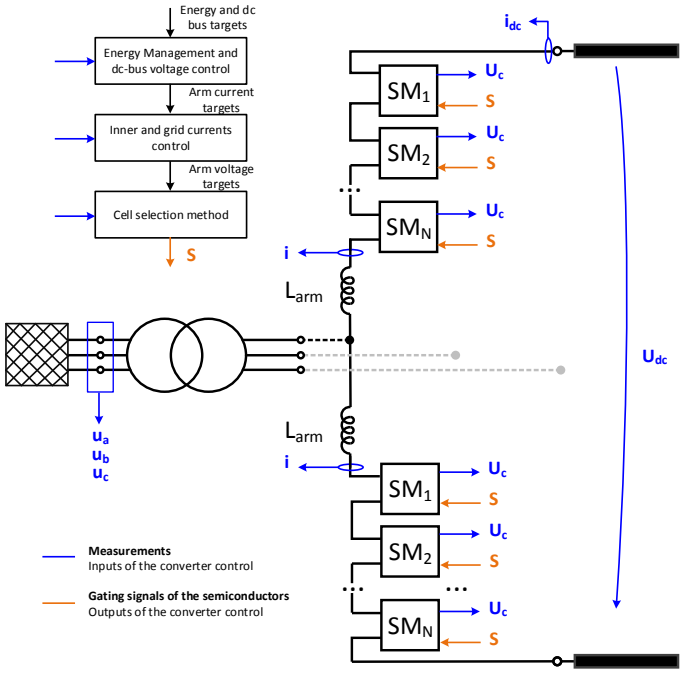


Figure 2.19: Overall control diagram of the MMC.

control are identified:

1. The energy management and dc link control: which, according to the individual capacitors voltage measurements $U_{c_{jki}}$, as well as dc-bus voltage U_{dc} knowledge, the inner and grid current targets are settled to establish the dc voltage set-point and eliminate any energy storage deviation between the stacks and legs.

2. The inner and grid current control: correlates the set-point created by the energy management higher hierarchical level i^*_{jk} and the required stack voltage voltage output u^*_{jk}.

3. Selective control of the submodules: determines the capacitors that should be inserted on the converter stacks, not only to meet the target u^*_{jk}, but also to guarantee restricted energy distribution among the stack cells. This stage computes all the gating signals S to be applied on the MMC switches.

The inherent details of the converter control are explained in depth in the next chapter.

2.3 Other MMC topologies

According to the VSC-HVdc state-of-the-art, it should be emphasized that HBSM-based MMCs are so far the only SM structure being applied to the field. However, other interesting SM solutions have emerged that might also be interesting for certain converter operating conditions.

Section 2.3.1 presents some SM structures that can be used to replace the HBSM to overcome technological limitations or to achieve a higher operating performance of the converter during its normal operation.

Furthermore, Section 2.3.2 shows SM schemes that can be utilized on the MMC with the inherent feature of blocking the dc faults. This feature might possibly be a vital feature for multi-terminal dc grids, and therefore could eliminate the power feeding of the defect until it becomes isolated.

2.3.1 Submodules with improved operating performance

Double submodule (2013)

The double submodule (DSM) structure was proposed in 2013 and is composed of two capacitors and several semiconductor switches as illustrated in Figure 2.20 [53,54]. The main idea of this topology, despite

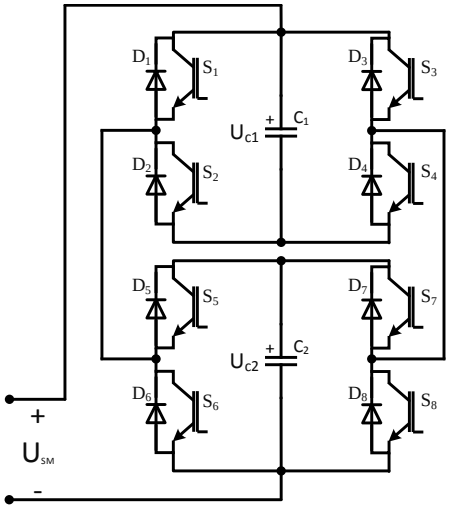


Figure 2.20: Double submodule structure.

having the capability to connect either in series or parallel its capacitors, is that the arm current is theoretically spread in half and pursues two different paths. Hence, either the switches can be rated to half of the nominal current and so, these SMs can be composed of cheaper semiconductors when compared to the HBSM. Or, on the other hand, if state-of-the-art semiconductors are embraced, this structure can double the power rating of the converter.

Figures 2.21 and 2.22 illustrate the voltage levels that can be generated at the output of this SM structure, particularly, zero, U_c or $2U_c$. However, in order to synthesize the U_c several options may exist, such as connecting one of the capacitors to the sub-module terminals (either $C1$ or C_2) or connecting both capacitors in parallel to the SM output. Furthermore, regardless of the voltage generated at DSM output, there are always two paths available for the arm current.

The parallel connection of the capacitors achieves better energy balancing from the capacitors, because doing so intrinsically balances the energy distribution between them [53, 54]. Moreover, this structure can reduce the voltage ripple of the capacitors when compared to the HFSM scheme.

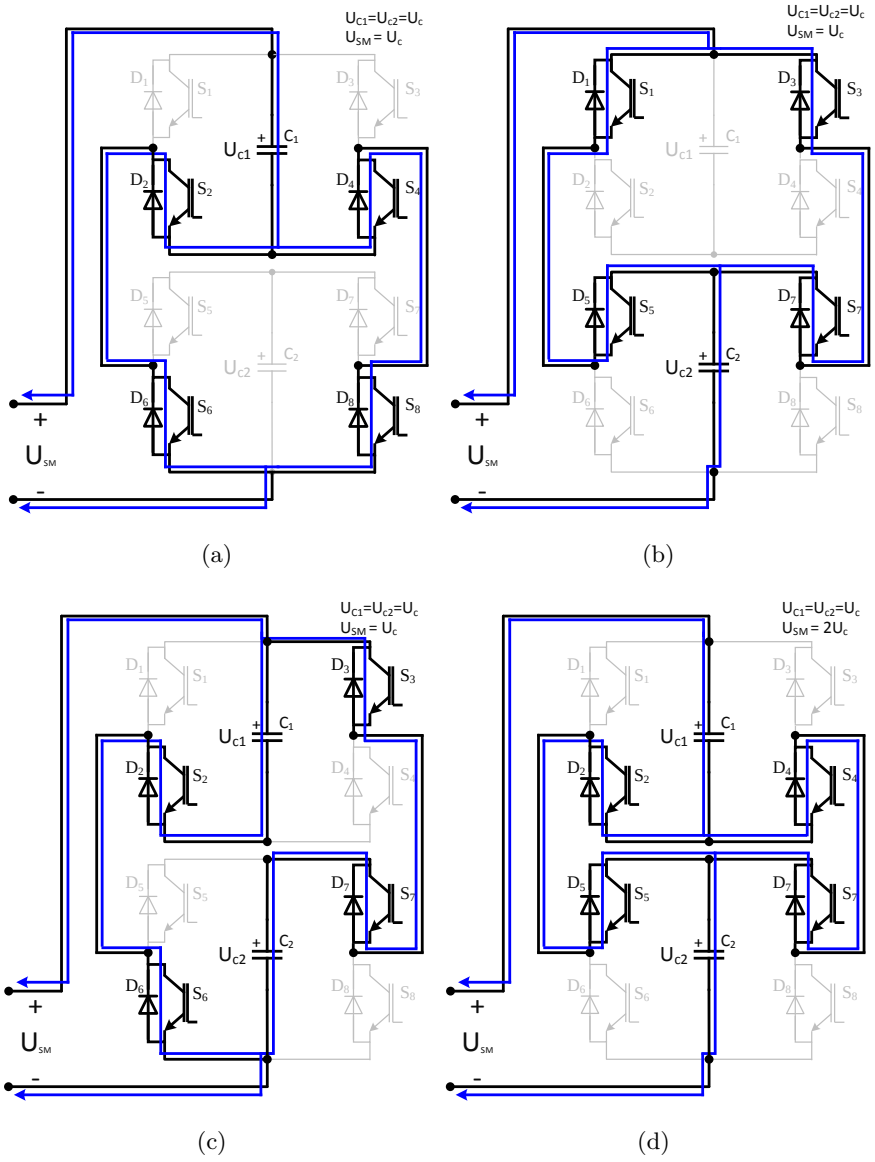


Figure 2.21: Non-zero voltage levels generated in the DSM.

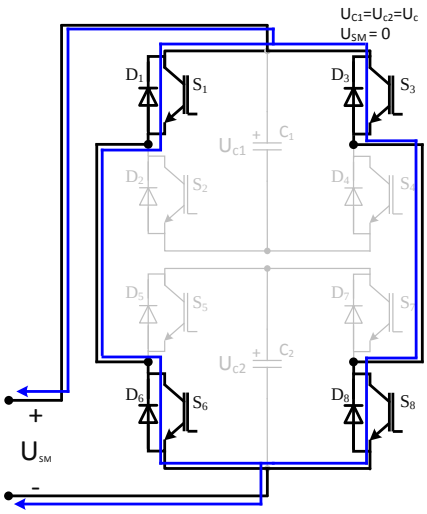


Figure 2.22: Bypass state of the DSM.

Soft-switching submodule (2014)

In 2014 the soft-switching submodule (SSSM) was introduced. As the name implies, it permits soft-switching commutations on the correspondent SM, which becomes more efficient. The structure of the SSSM is depicted in Figure 2.23. The core of its structure is the same as the HBSM, but an auxiliary resonant commutated pole (ARCP) was introduced in order to deviate the current from the main semiconductor switches whenever they commute (lossless switching events) [55]. The transition between the bypassed to inserted mode (or vice-versa) is done in eight steps, being a complex sequence. The increased complexity of this structure is the price to pay for the 45% reduction of the losses generated by the HBSM [55].

Other multilevel SM structures

Other multilevel converter structures have been proposed for use on the submodules of the modular multilevel converter, such as the flying capacitor (FC) and the neutral point clamped converter (NPC) [56]. There are two main goals that the proponents wanted to achieve by

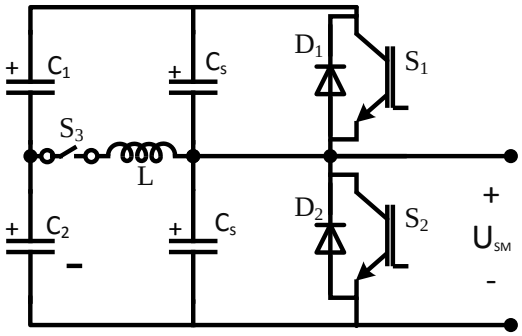


Figure 2.23: Soft-switching submodule structure.

using the FC or NPC schemes in the MMC submodules. First, it is the acceptance of those SM structures that can overcome legal problems related to patents [56]. Secondly, in the view of the manufacturers that provide those structures in compact version packages, it might be advantageous to use those multi-level converter schemes to reduce the overall size of the MMC [56].

The usage of such multilevel converter topologies increases the complexity of the MMC and the intrinsic voltage balancing of the capacitors may not be possible in some operating conditions [54, 56].

2.3.2 Submodules with dc fault blocking capability

One of the most discussed topics related to the HVdc field is the feasibility of building high-voltage dc grids and how they should operate [57, 58]. In this matter, several challenges are raised on the converter stations in order to upgrade from point-to-point connections to multi-terminal dc grids.

Regarding the point-to-point schemes, as illustrated in Figure 2.24, in the case of a fault event occurrence on the dc transmission line, both ac grids will feed the short-circuit. This fact occurs due to the subjugation of the dc voltage in respect to the ac lines, which causes the converter diodes to be forward biased. This condition lasts until a breaker is opened, either on the ac or dc side of the converter. However, since there

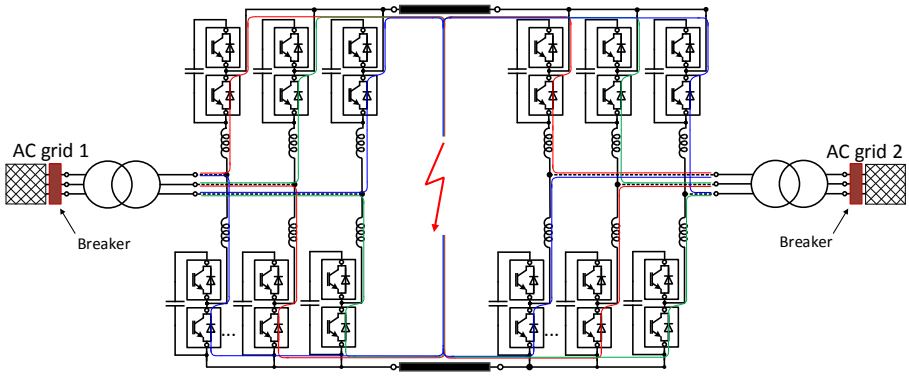


Figure 2.24: Point-to-point MMC-HVdc-based transmission scheme.

is a great deal of experience in manufacturing ac breakers, and it being easier to breach an ac current than a dc one, the ac breaker solution is being successfully applied to point-to-point HVdc transmission schemes.

Nonetheless, when multi-terminal dc schemes are brought into discussion, if a fault event occurs on one of the dc transmission lines, as shown in Figure 2.25, all the ac grids and the correspondent converter terminals will be affected by the defect. In this view, if the ac breaker prevailed as an option, all the terminals would be disconnected from their main ac grids, shutting down the whole dc grid until the faulty cable is repaired. Therefore, in order to add value to the multi-terminal dc schemes and enhance their continuous operation, it is imperative to break the dc faults from the dc side. In that case, breakers should be applied to both sides of the dc transmission lines, then being able to directly isolate the faulty line and ensuring that the dc network can continue to operate without this faulty path.

In recent years several submodules schemes have been proposed to be applied to MMC, allowing the converter to be able to block the feeding of the defect from the correspondent ac grids. Although the dc breakers continue to be needed to isolate the fault, the converters may help block it. Furthermore, an overview of the previously proposed submodule structures was performed and is discussed in the next section.

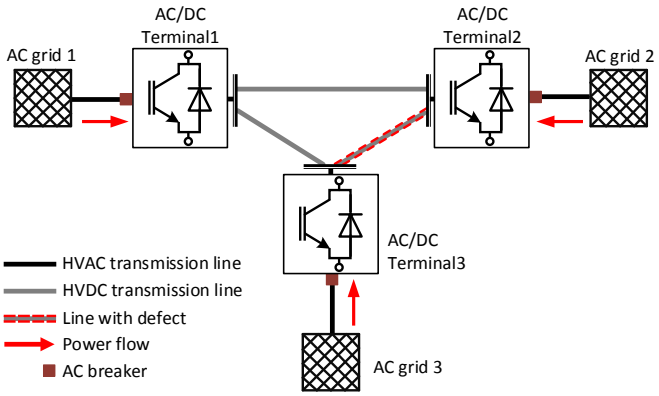


Figure 2.25: Three-terminal dc grid operating with a short circuit in one HVdc line.

Operating principle

As briefly described in the previous sections, during the normal operation of the MMC, the correspondent SMs should be able to create zero or a positive voltage steps at their output to synthesize the required arm voltages. However, if a short circuit occurs on a dc transmission line and the fault needs blocking, proper design of the submodules must be adopted to impose a positive or negative voltage level at their output. In addition, this task should be automatically ensured by means of diodes, which block the power flow from the ac to dc sides of the converter. The idea behind the converter's dc fault blocking capability is described in Figure 2.26.

Once the fault is detected by the converter control, all the gating signals for the IGBTs become blocked, the diodes being the semiconductor devices that drive the arm currents until the fault is nullified. Thereafter, depending on the voltage between lines at the ac side terminals, the proper polarities of the capacitors are connected to the SM's terminals, and if the voltage sum of the inserted capacitors exceeds the line-to-line voltage of the converter, the diodes become reverse biased, and consequently block the current flow.

Several submodule schemes with dc fault blocking capability were

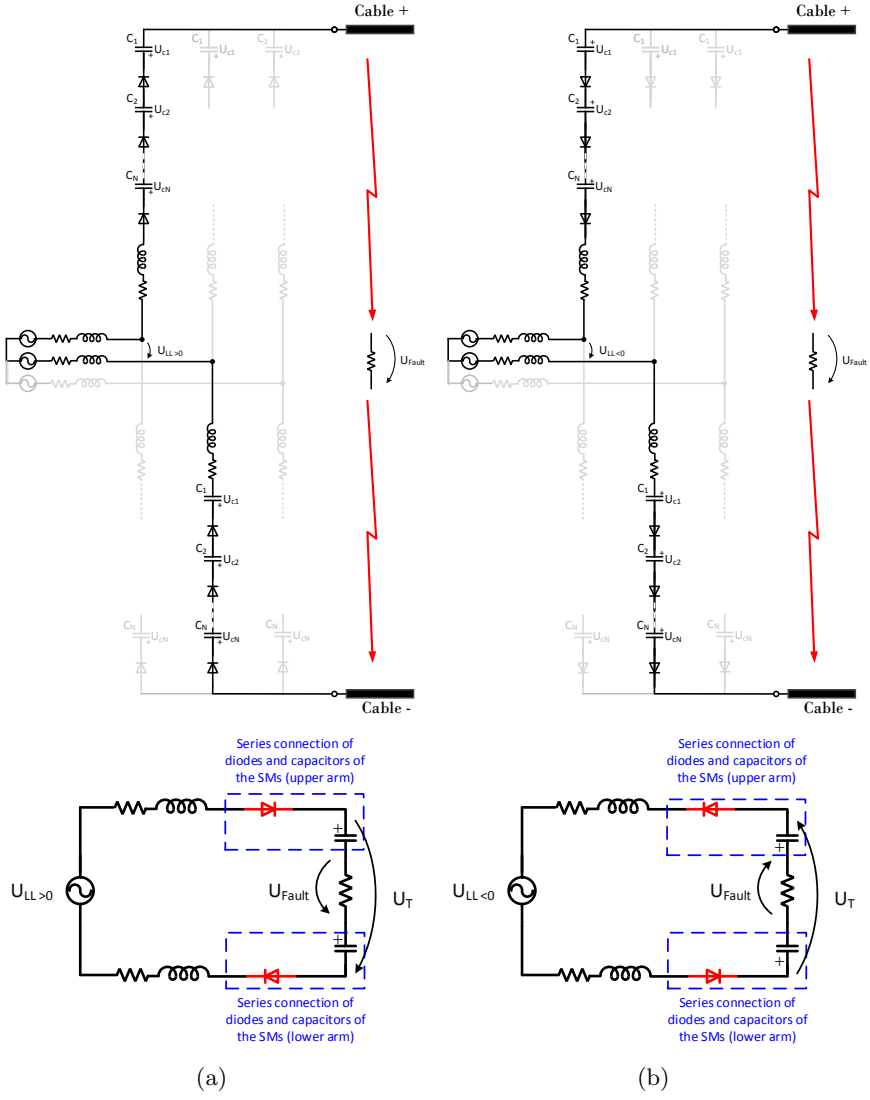


Figure 2.26: Operating principle of the MMC-based topology with dc fault blocking capability: whenever the arm current at the fault instant is (a) positive or (b) negative.

proposed in the literature. The particular features of each SM are explained in the next sections.

Full-bridge submodule (2010)

The full-bridge (FB) scheme is a very familiar topology which was presented as a viable SM solution in 2010 [59]. The full-bridge submodule (FBSM) is composed of four semiconductor switches and a capacitor device as illustrated in Figure 2.27.

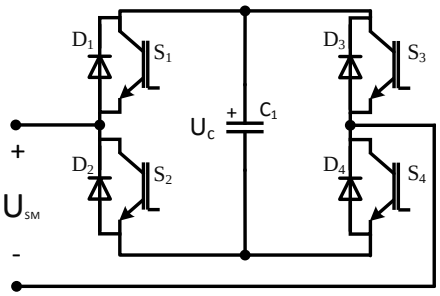


Figure 2.27: Full-bridge submodule structure.

The most evident fact regarding this structure is that uses twice the number of the semiconductor switches compared to the HBSM. Ergo, it generates much greater power losses [60], leading to a less efficient converter design. The FBSMs can generate three voltage levels at their output, particularly zero and $\pm U_c$, as illustrated in Figure 2.28. Regardless of the arm current flow, whenever the switches (S_1/D_1) and (S_4/D_4) are closed, the SM capacitor is inserted on the converter arm with a positive polarity. On the other hand, whenever the switches (S_2/D_2) and (S_3/D_3) are closed instead, the SM inserts the capacitor on the series-chain but with a negative polarity. Although negative polarity is not a requirement to operate the MMC under normal conditions, it can be used in order to reduce the voltage ripple of the capacitors of the cells or to extend the arm's voltage range [61]. Furthermore, two redundant states are available on the FBSM to bypass its capacitor.

Once a fault is recognized and the IGBTs are commanded to open, depending on the arm current direction, the proper diodes will be forced

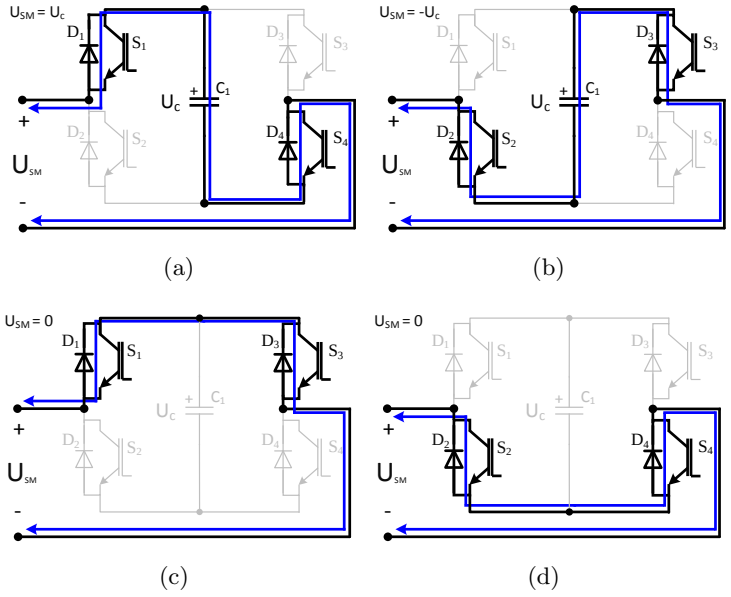


Figure 2.28: States of the FBSM in normal mode: the capacitor is inserted with (a) positive or (b) negative polarity; in (c) and (d) the capacitor is removed from the series-chain.

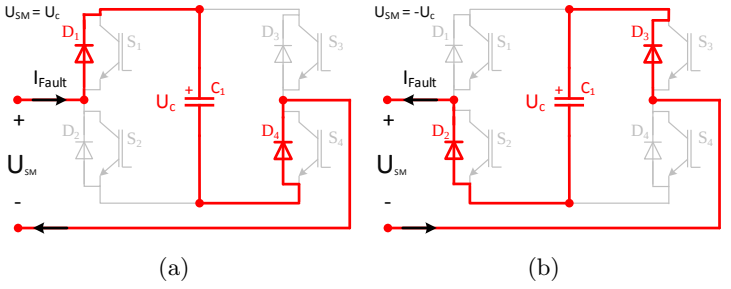


Figure 2.29: States of the FBSM in fault mode: the capacitor is inserted with (a) positive or (b) negative polarity.

to close, as summarized in Figure 2.29. Hence, if the corresponding fault current is positive, as illustrated in Figure 2.29(a), the diodes D_1 and D_4 will conduct the arm current, connecting the capacitor to the SM's output (with positive polarity). During this transient, the voltage sum of the capacitors should be higher than the ac grid amplitude[6], which applies a negative voltage to the arm inductor and the corresponding arm current reduces, until it decreases to zero and the diodes become blocked. On the other hand, if at the fault instant the correspondent arm current is negative, as illustrated in Figure 2.29(b), D_2 and D_3 will conduct the fault current until it reaches zero and the diodes become blocked.

Since the FBSM adopts twice more semiconductors than the HBSM, hybrid converter designs with both schemes are being proposed. This is due to the fact that enhances the MMC with dc fault blocking capability with lower losses than the MMC equipped only with FBSM [60]. The combination between the HFSMs with the SM schemes presented in the next sections are being also proposed for the same reasons [60].

Clamped double-submodule (2010)

The Clamped double-submodule (CDSM) was introduced in 2010 and it is composed of two equivalent half-bridge-based submodules with an additional IGBT with the corresponding anti-parallel diode (S_5/D_5) and two additional diodes (D_6 and $D7$), as illustrated in Figure 2.30 [59].

During the normal operation, the switch S_5 is permanently closed. Moreover, the states of the switch pairs (S_1/S_2) and (S_3/S_4) are independently managed as if they were two independent HBSMs connected in series. As presented in Figure 2.31, three voltage levels are expected at the CDSM's terminals: zero, U_c or $2U_c$. Both capacitors are bypassed by closing the switches S_2 and S_3, and the electrical current flows on the corresponding IGBTs or diodes accordingly to its direction.

[6]This is a design criteria of the converter terminal project.

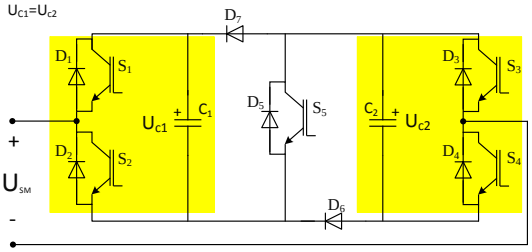


Figure 2.30: Clamped double-submodule

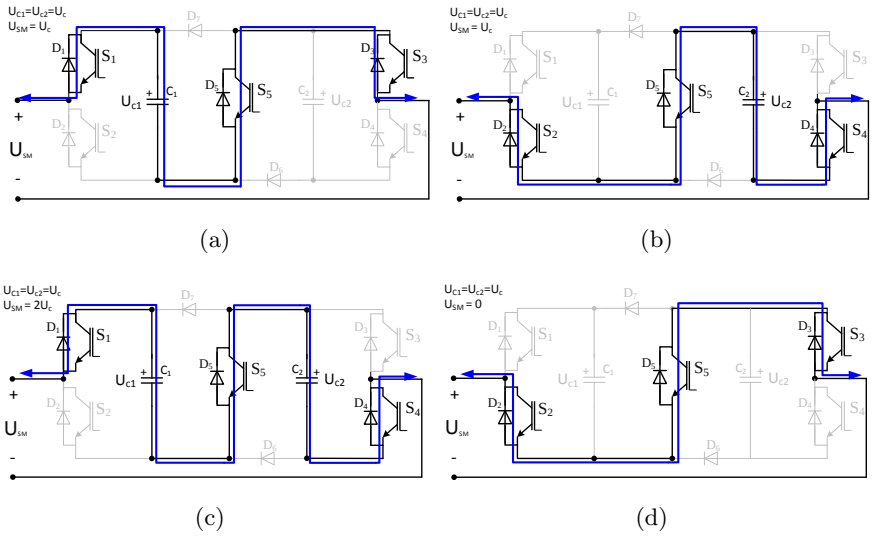


Figure 2.31: States of the CDSM in normal mode: (a) C_1, (a) C_2 or (c) both capacitors are inserted in the series stack; (d) both capacitors are bypassed from the series-chain.

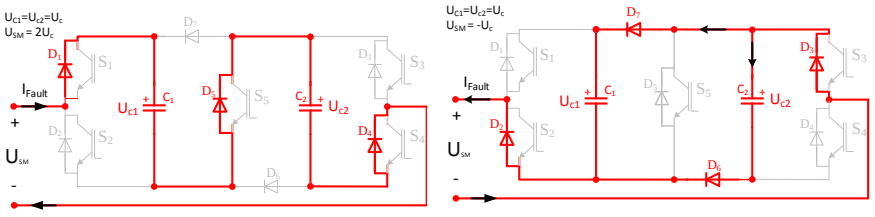


Figure 2.32: Operation of the CDSM in fault mode: with the arm current being (a) positive or (b) negative.

Once a fault is recognized and the IGBTs are ordered to open, as illustrated in Figure 2.32, the diodes of the CDSM are the active elements on the dc fault blocking feature. Based on the arm current direction, the diodes of the cell will automatically connect the capacitors with positive or negative polarity in its output. Hence, if the corresponding arm current is positive, as illustrated in Figure 2.32(a), the diodes D_1, D_4 and D_5 will conduct the arm current, connecting also both capacitors in series to the SM's output (with positive polarity). On the other hand, if at the fault instant the corresponding arm current is negative, as illustrated in Figure 2.32(b), D_2, D_3, D_6 and D_7 will be forward biased and conduct the fault current, which last until it reaches zero and the diodes become reverse biased. However, during this negative current scenario, special attention must be paid because the capacitors are connected in parallel. Therefore, the SM can only generate the $-U_c$ voltage step. As a deduction, a suitable number of CDSM should be assembled on the converter stacks in order to safely block the flow of the dc fault currents.

Clamped single-submodule (2013)

The clamped single-submodule (CSSM) is very similar to the HBSM but with a dc fault blocking capability. As illustrated in Figure 2.33, the CSSM structure is based on a HB cell with access to the middle point of its dc bus and with an additional pair of switches (S_3/D_3 and

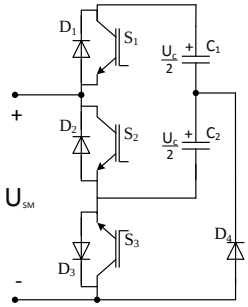


Figure 2.33: Clamped single-submodule.

S_4). Both capacitors are symmetrically charged. Furthermore, one of the switches is bidirectional in current (S_3/D_3). In contrast, a single diode (D_4) should be present to ensure dc fault blocking capability to the converter [62].

During the normal operation of the converter, the switch (S_3/D_3) is permanently closed. Moreover, the states of the switches (S_1/D_1) and (S_2/D_2) are managed to either insert or bypass both capacitors like the HBSM. Then, the CCSM scheme introduces one switch more to the current path, when compared to the HBSM.

In the event of a dc fault (see Figure 2.34(b)), if the arm current is positive, after opening of all the IGBTs, the diodes D_1 and D_3 will be forced to close and therefore connect the series of the capacitors to the SM's terminals, as illustrated in Figure 2.34(a). On the other hand, if at the fault moment the arm current is negative, as Figure 2.34(b) shows, D_2 and D_4 will be forced to drive the corresponding arm current and therefore insert the lower capacitor with $U_c/2$ in the series string. As a result, and similarly to what occurs in the CDSM, whenever connecting a negative voltage at the SM terminals is required, only half of the cells voltage sum available is attainable. Thus, the number of SMs assembled in each stack should be carefully designed in such a way that the converter can safely block the faulty current, regardless of its direction.

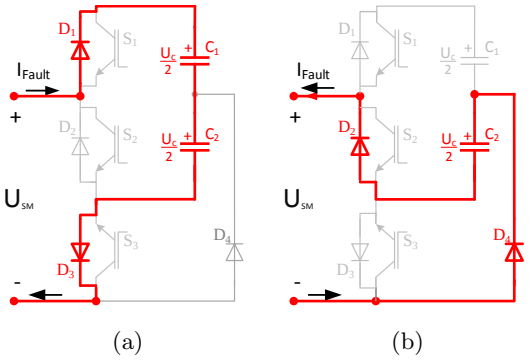


Figure 2.34: Operation of the CSSM in fault mode: (a) the arm current is positive or (b) negative.

Cross-connected submodule (2013)

The cross connected submodule (CCSM) is essentially composed of two half-bridge submodules which are linked by means of two additional switches (S_5/D_5 and S_6/D_6) as depicted in Figure 2.35 [63]. In opposition to the CDSM structure, the states of the half-bridges switches of the cross-connected-based submodule are not independently managed. Hence, the control signals of the six switches are determined accordingly to the required voltage that should be present at the SM's output. Moreover, the CCSM can generate four non-zero voltage levels and the zero voltage at its output, as illustrated in the Figures 2.36 and 2.37 respectively.

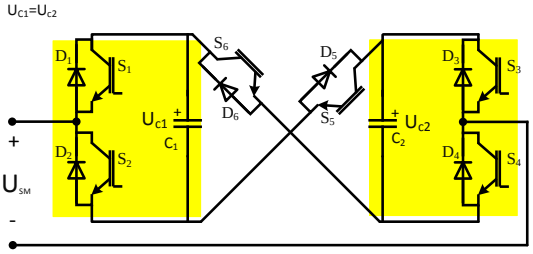
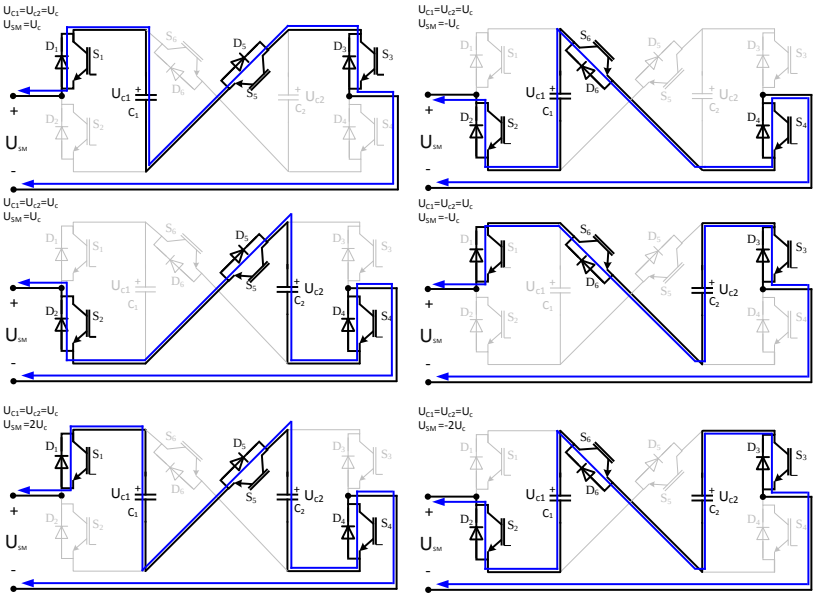
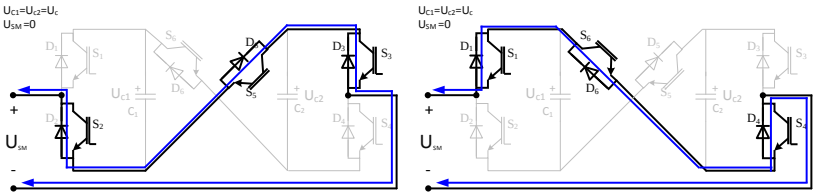


Figure 2.35: Cross connected-submodule



(a) (b)

Figure 2.36: Operation of the CCSM in normal mode: the capacitors are linked to the output with (a) positive or (b) negative polarity.

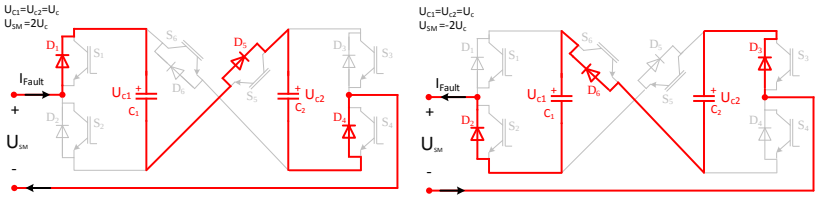


(a) (b)

Figure 2.37: Redundant states of the CCSM to bypass the capacitors.

As both figures present, whenever the switch (S_5/D_5) is closed, the non-negative voltage values (zero, U_c or $2U_c$) are expected at the SM's output. In contrast, if the switch (S_6/D_6) is closed instead, the non-positive voltage values (zero, $-U_c$ or $-2U_c$) are obtained at the SM's terminals. Therefore, this cross-connected submodule can generate five voltage levels at the converter output.

Regarding the CCSM operation during fault mode, as shown in Figure 2.38, $+2U_c$ or $-2U_c$ can be generated depending on the arm current flow direction. Then, in opposition to the CSSM and the CDSM designs, this structure generates symmetrical voltages on both current directions. As with the MMC-CDSM-based design, inserting two capacitors in the series-chain requires three switches. Hence, one switch less/more than the FB/HB submodule designs.



(a) (b)

Figure 2.38: The CCSM states during the dc fault scenario.

During normal converter operation, if the negative values are not intended to be used, the IGBT S_6 can be removed, and the diode D_6 becomes responsible for connecting this branch in a dc fault event [60]. In this way, the five-level CCSM (5L-CCSM) is changed to a three-voltage level CCSM (3L-CCSM), as it can only synthesize three voltage levels during the normal converter operation, namely the zero, U_c and $2U_c$. Moreover, the operation of the 3L-CCSM during the fault mode is the same as on the 5L-CCSM.

Semi-full-bridge submodule (2015)

The semi full-bridge submodule (SFB) is considered to be an extension of the CDSM, due to the replacement of the individual diodes by

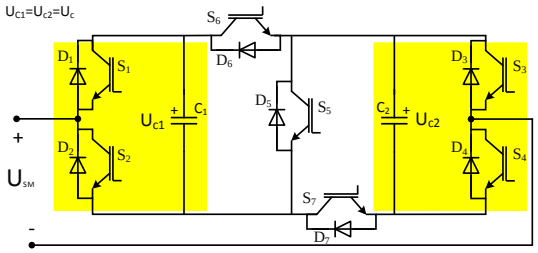
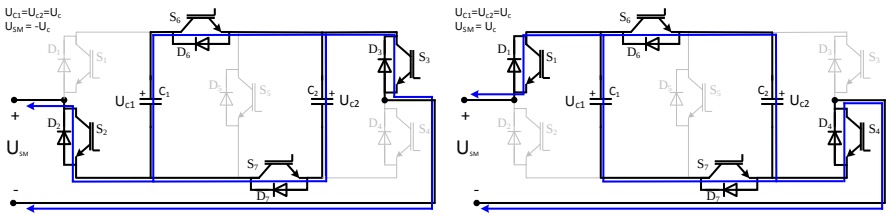


Figure 2.39: Semi-full-bridge submodule structure.

active switches as Figure 2.39 illustrates [64]. This structure can bypass or insert both capacitors to the converter arms either connected in series or parallel. In its proposal, the goal of the switches D_6/S_6 and D_7/S_7 is to connect both capacitors in parallel. In consequence, if at a given time both switches are closed (with D_5/S_5 open) and, by considering that they are exactly equal, as shown in Figure 2.40, they conduct half of the arm current. Consequently, the switches have half of the current rating when compared to the remaining switches. On the other hand, with switches S_6 and S_7 open the states of the cell are the same as the CDSM.



(a) (b)

Figure 2.40: Extension of the CDSM granted by the SFB in normal mode: the capacitors are linked to the SM output in parallel with (a) positive or (b) negative polarity.

Hence, with the referred extension, this structure can generate zero, U_c, $2U_c$ and $-U_c$ during the normal operation. Similarly to the CDSM, during the fault mode, the SFB ensures the asymmetrical voltages of

$2U_c$ and $-U_c$ at the cell output whenever the fault current is positive or negative respectively. Once again, proper design of the number of SFBSMs should be followed to ensure the converter's dc fault blocking capability.

Unipolar-voltage full-bridge submodule (2015)

The unipolar-voltage full bridge SM (UFBSM) is a simplification of the FBSM as illustrated in Figure 2.20 [60]. Considering that negative voltages are not used during the normal converter operation, the active switch S_3 of the FBSM is not required. In this view, the zero and U_c are still available on the normal converter operation. Moreover, whenever a dc fault occurs and the IGBTs are opened, the dc fault blocking capability of the UFBSM performs the same as the FBSM.

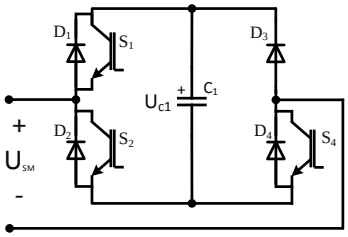


Figure 2.41: Double submodule structure.

2.4 Conclusions

The HVdc field is rapidly evolving and several options are available in the market with distinct features. On one hand, the LCC is the only solution that merges the robustness and efficiency to transmit power over thousands of kilometers. It is a very mature solution and continues to evolve, either in power rating or transmission length. The introduction of the VSC on the HVdc field was done in the late nineties (a relatively recent option). Four converter generations were put into operation and, step-by-step, the technological challenges were being overcome.

Currently, the fourth VSC-HVdc generation is composed of modular

multilevel converter based solutions. This option was proposed at the beginning of the present century but was validated on a HVdc project only a few years ago. This power converter structure is, in turn, composed of hundreds of low-power rated converters. Its features such as modulatity, power quality and the ac grid support provided classify the MMC as a breakthrough in the VSC-HVdc field, with a high potential for evolution.

In its original version, the MMC was composed of choppers and up to now has been the solution adopted by manufacturers. In recent years, other submodules were proposed in academia with particular features, namely to increase the converter efficiency, to double the power rating of the converter and to block dc faults (critical feature in dc grids). Depending on the importance is given to the variable needing optimizing, the proper submodule design should be selected.

In this work priority is given to submodules that maximize the efficiency of the converter without a substantial increase in its complexity. In this vision, the half-bridge-based submodules were used to study the behavior of the modular multilevel converter and afterwards used in the thesis.

Chapter 3

Modular Multilevel Converter Operation and Control

As introduced in the previous chapter, VSC-HVdc is evolving fast and the current state-of-the-art clearly shows the trend of the modular multilevel generation (MMC) in the dc transmission field. Additionally, due to its modular structure, it is expected to be present in a broad range of applications, at least, from medium to high voltage profiles.

The operational and control details of the MMC scheme are analyzed in this chapter. The theoretical analysis is then complemented with several time domain simulations performed in the Matlab/ Simulink environment. The numerical simulation permits the control strategies used to manage the internal dynamics to be validated as well as the interactions between the dc and ac sides of the converter.

The chapter is structured as follows: first, the converter operation is explored, which is complemented by the corresponding mathematical support. Afterwards, the procedure adopted to generate the required voltages across the converter stacks is presented. Subsequently, in accordance with the numeral analysis of the converter, its control scheme is deduced and designed, which is finally validated in the simulation environment referred to.

3.1 Mathematical Analysis

Perceiving the correct behavior of the converter plays a very important role in reaching a fully controlled, stable and robust MMC-VSC

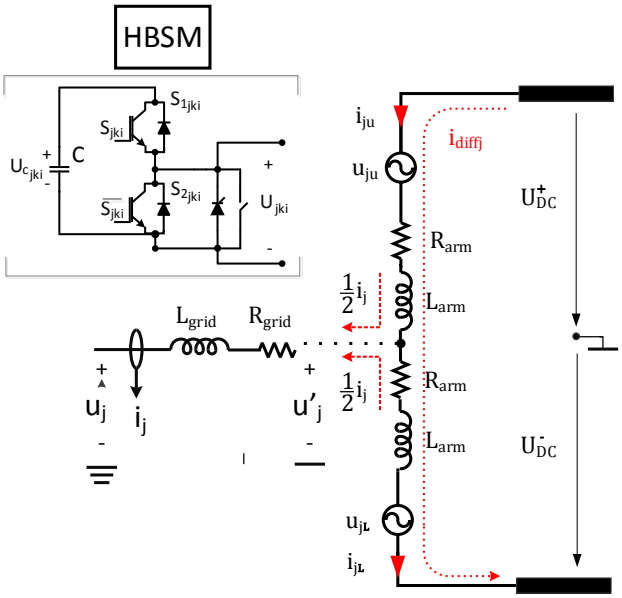


Figure 3.1: Single line diagram of the MMC equivalent circuit.

system. Figure 3.1 shows a single phase electrical equivalent circuit of a MMC. To facilitate the analysis of the converter, which has N HBSMs in each arm, the following subscripts were attached to the electrical variables:

- j addressing the converter leg ($j \in \{a, b \; or \; c\}$),
- k the arm position (k $\in \{U(pper) \; or \; L(ower)\}$) and
- i the submodule location in the corresponding arm (i $\in [1; N]$)

The MMC's DC link is modeled as two DC voltage sources (U_{DC}^{+} and U_{DC}^{-}). The point of common coupling (PCC) is modeled by an AC source (u_j) with the series impedance (R_{grid}/L_{grid}), which define the short circuit ratio (SCR) at the PCC. The MMC's arms are equipped with an inductance L_{arm} with a parasitic resistance R_{arm} that represents the coil losses.

The HBSMs are composed of a capacitance C_{jki} with the $U_{c_{jki}}$ voltage and two bidirectional power switches, $S_{1_{jki}}$ and $S_{2_{jki}}$. The switches S_1

and S_2 are driven in a complementary manner by the control signal S_{jki}. The SMs admit two operating states: either its capacitor is *inserted* in the series chain, when the switch $S_{1_{jki}}$ is closed (S_{jki} equals one); or the SMs are *bypassed*, with $S_{1_{jki}}$ opened (S_{jki} equals zero). The variation of the SMs operating mode with the S_{jki} signal accordingly impacts on their output voltage U_{jki}, as:

$$U_{jki}(t) = \begin{cases} U_{c_{jki}}(t), & \text{if } S_{jki}(t) = 1 \\ 0, & \text{if } S_{jki}(t) = 0 \end{cases} \Rightarrow U_{jki}(t) = S_{jki}(t)U_{c_{jki}}(t) \quad (3.1)$$

The management of the SM states also affects the synthesized voltage across the jk arm u_{jk} as (3.2) and also modifies the equivalent capacitor across the arms C_{jk}^{arm} (3.3). If considered that all the HBSMs are exactly equal, and so are their capacitors (3.4), the equivalent arm capacitance (3.3) is further simplified to (3.5).

$$u_{jk}(t) = \sum_{i=1}^{N} U_{jki}(t) = \sum_{i=1}^{N} S_{jki}(t)U_{c_{jki}}(t) \quad (3.2)$$

$$C_{jk}^{arm}(t) = \left[\sum_{i=1}^{N} \frac{1}{C_{jki}} S_{jki}\right]^{-1} \quad (3.3)$$

$$C_{jk1} \simeq C_{jk2} \simeq \ldots \simeq C_{jkN} = C \quad (3.4)$$

$$C_{jk}^{arm}(t) = C\left[\sum_{i=1}^{N} S_{jki}(t)\right]^{-1} \quad (3.5)$$

With proper management of the SM states, the voltage across the stacks can vary from zero (if all the capacitors are bypassed) to the maximum voltage available U_{jk}^{Σ} which leans on the number of energized submodules and their particular voltages (3.6). In order to investigate the converter operation, from now on, all the capacitors are considered balanced and share the same voltage value $U_{c_{jk1}}$. Hence, the maximum voltage vector applied on the MMC arms is given by (3.7)

$$U_{jk}^{\Sigma}(t) = \sum_{i=1}^{N} U_{c_{jki}}(t) \quad (3.6)$$

$$U_{jk}^{\Sigma}(t) = NU_{jk1}(t) \tag{3.7}$$

Adopting the grid and the differential current directions, respectively modeled as i_j and i_{diff_j} in the previous figure, leads to the arm currents i_{jk} (3.8). The grid current component models the current flow between the converter and its ac grid. In turn, the differential current component models the current flow in the converter legs. The grid and differential current components can contain multiple harmonic frequencies, which are also embedded in i_j and i_{diff_j} [65].

$$\begin{cases} i_{jU}(t) = i_{diff_j}(t) + \dfrac{i_j(t)}{2} \\ i_{jL}(t) = i_{diff_j}(t) - \dfrac{i_j(t)}{2} \end{cases} \tag{3.8}$$

The Kirchhoff voltage law (KVL) was applied to the jk arms and respective dynamics of the converter are described as:

$$\begin{cases} U_{DC}^{+}(t) - u_{jU}(t) - R_{arm}i_{jU}(t) - L_{arm}\dfrac{\mathrm{d}i_{jU}(t)}{\mathrm{d}t} - u'_j(t) = 0 \\ -U_{DC}^{-}(t) + u_{jL}(t) + R_{arm}i_{jL}(t) + L_{arm}\dfrac{\mathrm{d}i_{jL}(t)}{\mathrm{d}t} - u'_j(t) = 0 \end{cases} \tag{3.9}$$

By subtracting and adding the equations (3.9), it leads to MMC internal voltage drop u_{diff_j} and the equivalent emf model generated by the converter e_j, respectively given in (3.10) and (3.11).

$$\begin{aligned} U_{DC}^{+}(t) + U_{DC}^{-}(t) - (u_{jU}(t) + u_{jL}(t)) &= 2R_{arm}i_{diff}(t) + 2L_{arm}\frac{\mathrm{d}i_{diff}(t)}{\mathrm{d}t} \\ \underbrace{U_{DC}(t) - (u_{jU}(t) + u_{jL}(t))}_{\substack{\text{Voltage across the series} \\ \text{connected arm impedances} \\ u_{diff_j}(t)}} &= 2\left(R_{arm}i_{diff}(t) + L_{arm}\frac{\mathrm{d}i_{diff}(t)}{\mathrm{d}t}\right) \end{aligned} \tag{3.10}$$

where the dc poles $U_{DC}^{\pm}$ were considered balanced and equal to 0.5 U_{DC}.

$$\underbrace{\frac{u_{jL}(t) - u_{jU}(t)}{2}}_{\substack{\text{Equivalent emf} \\ \text{voltage generated} \\ \text{by the converter} \\ e_j}} = u'_j(t) + \frac{R_{arm}}{2}i_j(t) + \frac{L_{arm}}{2}\frac{\mathrm{d}i_j(t)}{\mathrm{d}t} \tag{3.11}$$

where u'_j is the voltage at the mid-point of the converter arms in respect to mid-point of the dc bus (3.12), as previously illustrated in the Figure 3.1.

$$u'_j(t) = u_j(t) + R_{grid} i_j(t) + L_{grid} \frac{\mathrm{d}i_j(t)}{dt} \tag{3.12}$$

The dynamics between the converter and its ac grid attached u_j are obtained by replacing the mid-point voltage model (3.12) in (3.11), respectively given as:

$$e_j(t) = u_j(t) + R_{eq} i_j(t) + L_{eq} \frac{\mathrm{d}i_j(t)}{\mathrm{d}t} \tag{3.13}$$

where R_{eq} is the equivalent resistance between the converter emf and u_j (3.14). Similarly, L_{eq} is the equivalent inductance between the converter emf and u_j (3.15).

$$R_{eq} = R_{grid} + \frac{R_{arm}}{2} \tag{3.14}$$

$$L_{eq} = L_{grid} + \frac{L_{arm}}{2} \tag{3.15}$$

Taking a look at the *emf* dynamics of the MMC (3.11) and at the inner voltage drop dynamics (3.10), shows that the common voltage values applied on the arms within the same phase unit are consequently canceled at e_j. In contrast, these common voltage values are added together to synthesize the inner differential voltage u_{diff_j} (3.10). Hence, both common and differential voltage components present at the converter arms can be assumed to be decoupled. This fact means that those voltage components can be used to independently control the inner (inner current control) and external (ac grid current control) dynamics of the converter.

Put shortly, two voltage components e_j and u_{diff_j} are expected on the converter arms within the same phase unit. The first component should be present at the upper and lower arms with complementary signs whereas the second component should be introduced as a common variable to both arms. In this vision, the common voltage values of u_{diff_j} only impact the inner dynamics of the converter, by contrast, the anti-phase e_j elements should be responsible for managing the dynamics between the converter and the electrical ac grid. Hence, two functional

diagrams of the converter operation can be presented, such as the inner dynamics representation of the converter, shown in Figure 3.2, and the interactions between the converter and its ac grid, depicted in Figure 3.3.

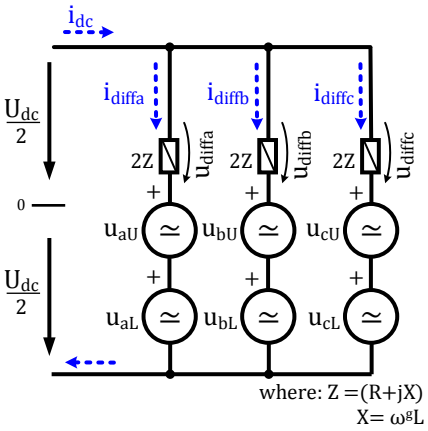


Figure 3.2: Representation of the converter inner dynamics.

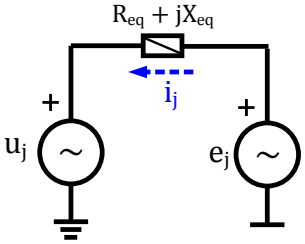


Figure 3.3: Single phase representation of the converter ac dynamics as a representation of a two-node HVac network.

Regarding the inner dynamics representation of the MMC, a dc current i_{dc} is presented that approaches the dc terminals of the converter from the dc transmission line and is spread over the three phase units of the converter. However, the quota of the dc current that flows in each phase unit depends on u_{diff_j}. With proper management of the voltage drop in the phase unit's impedance, the allocation of the dc current among the three phase units is achieved and, as will be explained later, it may be useful for various purposes.

In terms of the interactions of the converter with the ac grid, as a grid-tied VSC, it can be represented by two voltage sources. Therefore, by managing the magnitude and phase angle of e_j, the active and reactive power flow between both sources is handled.

Solving the equation system composed of (3.10) and (3.11) in respect to the arm voltages u_{jU} and u_{jL}, it is reasonable to fragment the arm voltages according to the individual components e_j and u_{diff_j}, as emphasized in (3.16) [66].

$$\begin{cases} u_{jU}(t) = \dfrac{U_{DC}(t)}{2} - \dfrac{u_{diff_j}(t)}{2} - e_j(t) \\ u_{jL}(t) = \dfrac{U_{DC}(t)}{2} - \dfrac{u_{diff_j}(t)}{2} + e_j(t) \end{cases} \tag{3.16}$$

If the fragmentation depicted in the previous expression is accepted, by imposing a particular voltage in the upper and lower arms, and affecting the equation system with the measurement of $U_{dc}(t)$, it is intrinsically imposing the e_j and u_{diff_j} values generated by the converter. Hence, in order to manage the converter variables, a reverse engineering procedure is embraced, and a control scheme is adopted that outputs the proper e_j and u_{diff_j} targets (e_j^* and $u_{diff_j}^*$) to accordingly define the arm voltage targets u_{jk}^* as (3.16).

Later on, the arm capacitors are sorted out and inserted in such a a way that approximate as much as possible the real u_{jk} and target u_{jk}^* values. As the number of the arm capacitors increases on the stacks, the higher the number of the voltage steps available becomes, which reduces the discrepancy between u_{jk}^* and u_{jk} (see Figure 3.4). To deduce the converter control scheme it was assumed that the MMC has a considerably large number of SMs and so, the discrepancy between the u_{jk}^* and u_{jk} was negligible (3.17). Hence, it can be affirmed that e_j and u_{diff_j} are roughly equal to their targets (3.18).

$$u_{jk}^* \approx u_{jk} \tag{3.17}$$

$$\begin{gathered} u_{diff_j}^* \approx u_{diff_j} \\ e_j^* \approx e_j \end{gathered} \tag{3.18}$$

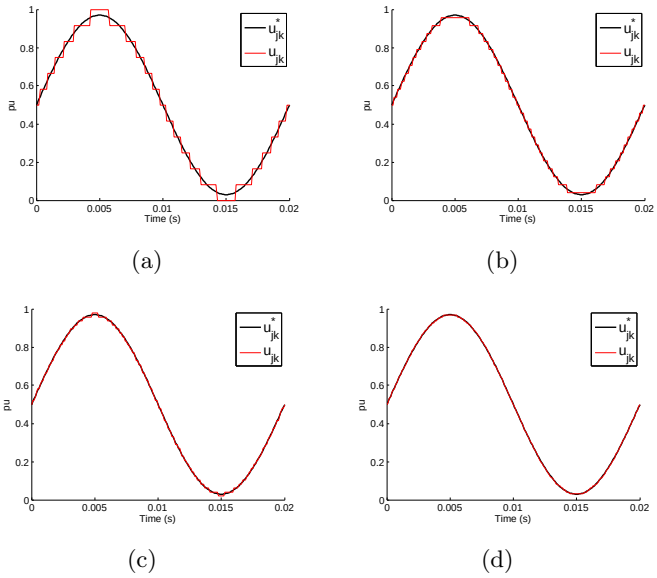


Figure 3.4: Number of submodules impact on the MMC's voltage waveform quality: (a) N=12, (b) N=24, (c) N=48 and (d) N=96.

3.2 Energy dynamics and general circuit analysis

3.2.1 Energy dynamics

In consideration of equal voltage distribution among the N cells that are placed in the same arm, its energy storage W_{jk}^{Σ} is:

$$W_{jk}^{\Sigma} = N \underbrace{\frac{1}{2} C \left(\frac{U_{jk}^{\Sigma}}{N} \right)^2}_{\substack{\text{Energy storage} \\ \text{of one single} \\ \text{capacitor}}} = \frac{1}{2} \frac{C}{N} \left(U_{jk}^{\Sigma} \right)^2 \tag{3.19}$$

Due to the fact that the arm current directly flows on the arm capacitors, it directly affects their energy storage. Hence, by definition, the variation of the energy storage over the time is dependent on the power that is flowing, as shown in (3.20) and (3.21).

$$\frac{dW_{jU}^{\Sigma}}{dt} = P_{jU} = i_{jU} u_{jU} \tag{3.20}$$

$$\frac{dW_{jL}^{\Sigma}}{dt} = P_{jL} = i_{jL}u_{jL} \tag{3.21}$$

Therefore, according to the arm currents (3.8) and voltages (3.16), the corresponding arm energy storage fluctuation is given by (3.22) and (3.23).

$$\frac{dW_{jU}^{\Sigma}}{dt} = i_{jU}u_{jU} = \left(\frac{i_j}{2} + i_{diff_j}\right)\left(\frac{U_{dc}}{2} - e_j - \frac{u_{diff_j}}{2}\right) \tag{3.22}$$

$$\frac{dW_{jL}^{\Sigma}}{dt} = i_{jL}u_{jL} = \left(-\frac{i_j}{2} + i_{diff_j}\right)\left(\frac{U_{dc}}{2} + e_j - \frac{u_{diff_j}}{2}\right) \tag{3.23}$$

Moreover, the total energy storage of each particular phase unit W_j^{Σ} is given by the sum of the individual storages of each arm (3.24). The energy difference between the arms within the same phase unit is given by (3.25).

$$W_j^{\Sigma} = W_{jU}^{\Sigma} + W_{jL}^{\Sigma} \tag{3.24}$$

$$W_j^{\Delta} = W_{jU}^{\Sigma} - W_{jL}^{\Sigma} \tag{3.25}$$

By adding (3.22) and (3.23) yields to the total energy variation in respect to the operating conditions of the converter as:

$$\frac{dW_j^{\Sigma}}{dt} = i_{diff_j}\left(U_{dc} - u_{diff_j}\right) - e_j i_j \tag{3.26}$$

Three components are identified in the energy storage dynamics of the converter legs [66]:

- $i_{diff_j}U_{dc}$- The dc component of i_{diff_j}, due to its positive sign, is (a portion of the total dc current that reaches the converter terminals i_{dc}) the component that brings power from the dc transmission line respectively[1]. The product between the differential current (dc component) by the dc bus voltage describes the total input power of the corresponding phase unit j, which is responsible for boosting its energy storage.

[1] At steady-state conditions with $W_a^{\Sigma} = W_b^{\Sigma} = W_c^{\Sigma}$, the incoming power from the dc line is equally distributed among the three-phase units. Hence, the dc component of i_{diff_j} will be equal to $i_{dc}/3$.

- $e_j i_j$ - The product between these two components models the power that is delivered to the ac grid. According to the negative sign, the power delivered to the ac grid comes from the energy stored at the MMC capacitors. Hence, by balancing the power injected into the ac grid as a function of the power received from the dc bus, the global energy storage is managed on the corresponding leg of the converter.

- $i_{diff_j} u_{diff_j}$ - models the losses caused by the differential current.

On the other hand, subtracting (3.22) and (3.23) yields the energy variation between the arms within the same phase unit, in respect to the operating conditions of the converter:

$$\frac{dW_j^{\Delta}}{dt} = \underbrace{-2e_j i_{diff_j}}_{\textcircled{1}} + \left(\frac{U_{dc}}{2} - \frac{u_{diff_j}}{2}\right) i_j \tag{3.27}$$

The harmonic frequencies present in u_{diff_j} and i_{diff_j} should be reinforced and should be the same (3.10). Furthermore, as long as there is no dc component in the converter's *emf* voltage e_j and on the grid currents i_j, the dc component present in u_{diff_j} and i_{diff_j} used to manage the energy balance between the converter legs does not affect the energy deviation between the arms of the converter. Hence, the previous equation emphasizes that the dc components of u_{diff_j} and i_{diff_j} do not impact the energy balance of the converter arms.

Therefore, an ac current component should be imposed to flow between the phases of the converter (i_{diff_j}). Thus, by imposing an ac component in u_{diff_j} with the same nature as e_j, the component $\textcircled{1}$ will be different from zero, and hence, the resultant ac current component of i_{diff_j} can be used to manage the energy deviation between arms.

As a conclusion, the differential current of the converter, namely its dc and ac components, play a tremendous role in its stability. Proper management of their harmonic frequencies addresses the energy balancing across the converter phase units and arms.

3.2.2 General circuit analysis

The fact that the power that is delivered to the ac grid flows across the arm capacitors results in the fluctuation of their energy storage. To analyze the fluctuation of the energy storage of the capacitors, let's consider that the converter is operating at steady-state condition, with a symmetric energy distribution among the six arms (no ac component is present in u_{diff_j}/i_{diff_j}). Furthermore, let's focus only on the phase unit a, operating with the electrical variables defined as:

$$\begin{aligned} e_a &= \hat{e}_a \cos(\omega t + \phi) \\ i_a &= \hat{i}_{ga} \cos(\omega t + \theta) \\ u_{diff_a} &= \hat{u}_{diff_a} \\ i_{diff_a} &= \frac{I_{dc}}{3} \end{aligned} \tag{3.28}$$

where, $(\hat{e}_a,\, \phi)$, $(\hat{i}_{ga},\, \theta)$ are the amplitudes and the phase angles respectively, of the *emf* of the converter (e_a) and the grid current (i_a). ω is the angular frequency of the electrical grid. $\hat{u}_{diff_a}$ is the voltage drop across the series connected inductors of the phase unit.

By replacing the variables defined in the previous equation on (3.22) and (3.23), the energy storage fluctuation of the stack capacitors is described as:

$$\begin{aligned} \frac{dW_{jU}^{\Sigma}(t)}{dt} = & \frac{U_{dc}\hat{i}_{ga}}{4}\cos(\omega t + \theta) && \text{(1)} \\ & - \frac{\hat{i}_{ga}\hat{e}_a}{4}\left[\cos(\theta - \phi) + \cos(2\omega t + \phi + \theta)\right] && \text{(2)} \\ & - \frac{\hat{i}_{ga}\hat{u}_{diff_a}}{4}\cos(\omega t + \theta) && \text{(3)} \\ & + \frac{I_{dc}U_{dc}}{6} && \text{(4)} \\ & - \frac{I_{dc}\hat{e}_a}{3}\cos(\omega t + \phi) && \text{(5)} \\ & - \frac{I_{dc}\hat{u}_{diff_a}}{6} && \text{(6)} \end{aligned} \tag{3.29}$$

$$\begin{aligned}
\frac{dW_{jL}^{\Sigma}(t)}{dt} = & -\frac{U_{dc}\hat{i}_{ga}}{4}\cos(\omega t+\theta) && \textcircled{1}\\
& -\frac{\hat{i}_{ga}\hat{e}_a}{4}\left[\cos(\theta-\phi)+\cos(2\omega t+\phi+\theta)\right] && \textcircled{2}\\
& +\frac{\hat{i}_{ga}\hat{u}_{diff_a}}{4}\cos(\omega t+\theta) && \textcircled{3}\\
& +\frac{I_{dc}U_{dc}}{6} && \textcircled{4}\\
& +\frac{I_{dc}\hat{e}_a}{3}\cos(\omega t+\phi) && \textcircled{5}\\
& -\frac{I_{dc}\hat{u}_{diff_a}}{6} && \textcircled{6}
\end{aligned} \tag{3.30}$$

From the analysis of (3.29) and (3.30), we can conclude that at steady-state operation, the dW_{jk}^{Σ}/dt has the following structure[2]:

$$\frac{dW_{jk}^{\Sigma}(t)}{dt} = k_0 + k_{\omega}\cos(\omega t+\xi_{\omega}) + k_{2\omega}\cos(2\omega t+\xi_{2\omega}) \tag{3.31}$$

where k_0 represents the power imbalance between the dc and ac sides of the converter. (k_{ω}, ξ_{ω}) and ($k_{2\omega}$, $\xi_{2\omega}$) are the amplitude and the phase angles of the first and second harmonic frequencies present in W_{jk}^{Σ}, respectively.

It should be emphasized that in order to maintain the mean energy storage constant over a fundamental grid cycle, the mean value of the previous equation should be zero. Furthermore, as a consequence of the power that flows on the converter arms, the energy stored on the corresponding capacitors varies as described in the previous equation.

Regarding the energy storage dynamics of converter leg (3.24), it is obtained by adding the expressions (3.29) and (3.30). The sum of both equations will cancel out the odd-based elements of the expressions (①, ③ and ⑤). Thus, the result of the energy storage dynamics of the leg

[2]If a detailed analysis on the harmonic content of the SM capacitors U_{jk}^{Σ} is performed and accordingly in W_{jk}^{Σ}, the third and fourth harmonics should be also represented. However, only the dc, the fundamental and the double-line harmonic elements were considered due to their considerably large amplitude when compared to the third and fourth ones [67].

j will have the form:

$$\frac{dW_j^{\Sigma}}{dt} = \frac{d\left(W_{jU}^{\Sigma}(t) + W_{jL}^{\Sigma}(t)\right)}{dt} = k_0^{'} + k_{2\omega}^{'}\cos\left(2\omega t + \xi_{2\omega}^{'}\right) \tag{3.32}$$

where $k_0^{'}$ is the difference between the incoming/leaving power flow on the corresponding phase unit j. ($k_{2\omega}^{'}$,$\xi^{'}$) characterizes the amplitude and phase angle of the second harmonic frequency [3].

To maintain the mean energy storage value constant, the mean value of the previous equation must necessarily be zero.

In contrast, the dynamics of the energy deviation between the upper and lower arms is obtained by differentiating the expressions (3.29) and (3.30). This fact annuls the (②, ④ and ⑥) elements of the referred equations and immediately results in the following form:

$$\frac{dW_j^{\Delta}}{dt} = \frac{d\left(W_{jU}^{\Sigma}(t) - W_{jL}^{\Sigma}(t)\right)}{dt} = k_0^{''} + k_{\omega}^{'}\cos\left(\omega t + \xi_{\omega}^{'}\right) \tag{3.33}$$

where $k_0^{''}$ models the energy imbalance between the upper and lower arms. ($k_{\omega}^{'}$, $\xi_{\omega}^{'}$) characterizes the amplitude and phase angle of the fundamental harmonic frequency [4].

This means that the energy difference between the upper and lower arms, under balanced conditions, fluctuates with a period defined by ω. Logically, it should be also mentioned that the harmonic frequency that characterizes the energy fluctuation in W_{jk}^{Σ}, W_j^{Σ} and W_j^{Δ} are also spotted on the capacitors voltage sum U_{jk}^{Σ}, $\left(U_{jU}^{\Sigma} + U_{jL}^{\Sigma}\right)$ and $\left(U_{jU}^{\Sigma} - U_{jL}^{\Sigma}\right)$ respectively.

[3] A fourth harmonic element, despite having an amplitude much smaller when compared to $k_{2\omega}^{'}$, could be included in this expression [67].

[4] A third harmonic element, despite having an amplitude much smaller when compared to $k_{\omega}^{'}$, could be included in this expression [67].

3.3 Arm modulation index

3.3.1 Introduction

Once the voltage targets for the arms are settled, their voltage requires modulation. To do so, the those targets are first normalized. Consequently, according to the normalized value, the most appropriate capacitors, either in number or voltage, are selected to be inserted on the converter arms.

In the literature two independent alternatives to normalize the arm voltage targets can mainly be found, being responsible for leading to different operation performances of the converter. Either the direct modulation approach [66] or the dc-bus-voltage-based modulation can be used [48, 68, 69]. The characteristics of both schemes are shown in the next sub-sections.

3.3.2 Direct Modulation

Once the arm voltage target u^*_{jk} is determined by (3.16), in the presence of the direct modulation the arm modulation index set-point m^*_{jk} is normalized according to the maximum voltage magnitude U^{Σ}_{jk} that can be synthesized on the corresponding arm. The normalization is ergo accomplished as:

$$m^*_{jk}(t) = \frac{u^*_{jk}(t)}{U^{\Sigma}_{jk}(t)} \tag{3.34}$$

where m^*_{jk} varies from 0 to 1, according to $0 \leq u^*_{jk} \leq U^{\Sigma}_{jk}$.

Then, the arm modulation index set-point is used by the selective control of the SMs to determine the value of the control signals S_{jki} to properly insert the desired capacitors with $U_{c_{jki}}$ (3.35). As the number of series-connected SMs increases, the arm voltage value is approximated to its reference ($u^*_{jk} \approx u_{jk}$). Hence, the real arm modulation

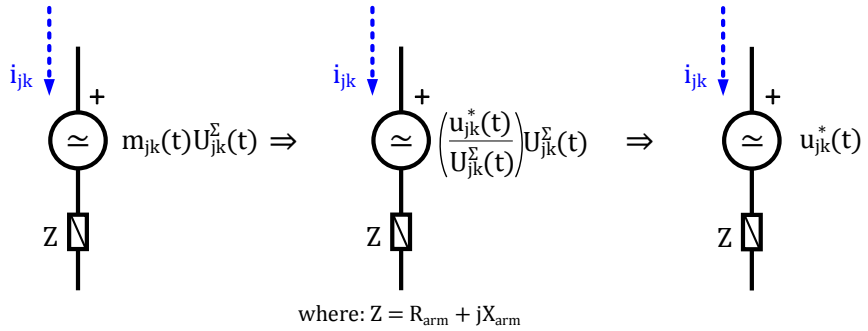


Figure 3.5: Arm voltages conception based on the direct modulation.

index m_{jk} is roughly equal its reference m^*_{jk} (3.36).

$$m_{jk}(t) = \frac{\sum_{i=1}^{N} S_{jki}(t) U_{c_{jki}}(t)}{\sum_{i=1}^{N} U_{c_{jki}}(t)} \tag{3.35}$$

$$m^*_{jk}(t) \approx m_{jk}(t) \Rightarrow u^*_{jk}(t) \approx \sum_{i=1}^{N} S_{jki}(t) U_{c_{jki}}(t) \tag{3.36}$$

Agreeing with what has been previously said, using direct modulation on a converter with a large number of SMs on the arms shows that its operation can be modeled as illustrated in Figure 3.5. As the left figure shows, if the real arm modulation index m_{jk} is replaced by its set-point defined as (3.34), as previously mentioned they are roughly equal (3.36), then the numerator and denominator shown in the middle figure get canceled. Thus, from the perspective of converter control, the direct modulation scheme directly imposes the corresponding voltage set-point across the converter stacks.

Furthermore, if the arm voltage targets are directly established across the converter arms, the *emf* and u_{diff_j} become explicitly imposed.

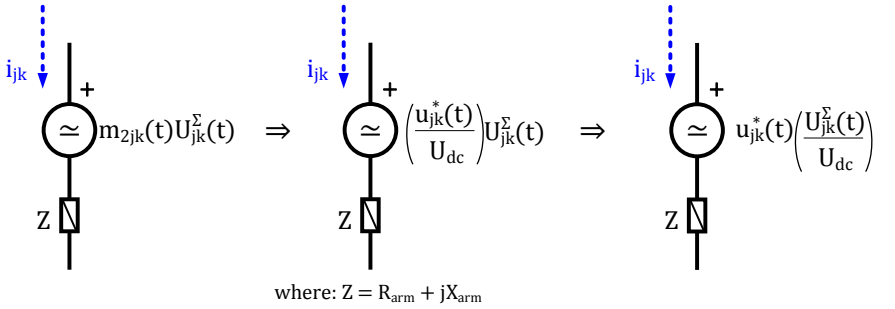


Figure 3.6: Arm voltages conception based on the dc-link modulation.

3.3.3 dc-voltage-based modulation

In this methodology, instead of normalizing the arm voltages according to the maximum voltage amplitude of the arms U^{Σ}_{jk}, the normalization is complete according to the dc bus voltage U_{dc}, as shown in $m_{2_{jk}}$ (3.37) [48, 65, 68–70]:

$$m^{*}_{2_{jk}}(t) = \frac{u^{*}_{jk}(t)}{U_{dc}(t)} \tag{3.37}$$

Hence, the voltage of the capacitors is not taken into account at the instant that $m^{*}_{2_{jk}}$ is determined. Consequently, whenever the arm voltages are modulated with the dc-link-based method, the voltages across the arms are given by:

$$u_{jk}(t) = m_{2_{jk}}(t)U^{\Sigma}_{jk}(t) \quad \overset{(3.37)}{\Rightarrow} \quad u_{jk}(t) = u^{*}_{jk}(t)\frac{U^{\Sigma}_{jk}(t)}{U_{dc}(t)} \tag{3.38}$$

In contrast to the direct modulation, on the dc-link-based modulation, the arm voltage targets are affected by the harmonic content of U^{Σ}_{jk}. Hence, the voltage oscillations present at U^{Σ}_{jk} affect the arm voltages, as the previous equation and Figure 3.6 demonstrate.

The usage of this modulation strategy introduces a common voltage harmonic element on the upper and lower arms of the converter $u_{2\omega_j}$ (see Figure 3.7), which is characterized by the double-frequency of its ac lines 2ω and with a negative sequence of phases (3.39) [65, 70]. Consequently this modulation excites a flow of a differential current with 2ω on the phase units of the converter. Moreover, the presence of a second

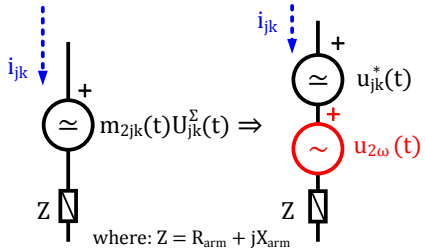


Figure 3.7: Consequences of the dc-link-based voltage modulation.

harmonic in u_{diff_j} and on the differential current flow i_{diff_j} increases the harmonic content in U_{jk}^{Σ} [65, 70].

$$\begin{cases} u_{2\omega_a} = \hat{u}_{2\omega_a} \cos\left(2\omega t + \xi\right) \\ u_{2\omega_b} = \hat{u}_{2\omega_b} \cos\left(2\omega t + \xi + \dfrac{2\pi}{3}\right) \\ u_{2\omega_c} = \hat{u}_{2\omega_c} \cos\left(2\omega t + \xi - \dfrac{2\pi}{3}\right) \end{cases} \tag{3.39}$$

Then, additional control loops should be considered to inject a second voltage harmonic into the converter arms modulation to eliminate the perturbation engaged by the dc-link-based modulation strategy. The feed-forward open-loop approach introduced in [70], the closed-loop circulating current suppression controller (CCSC) [69] or the closed-loop-based proportional-resonant controllers [71] are control schemes proposed in the literature to remove the second-harmonic order voltage from the arms. Since direct modulation intrinsically eliminates the flow of this harmonic current without including additional control loops, it has been the modulation used in all the studies performed in this work.

3.4 Cell selection algorithm

After the voltage targets for the MMC arms are defined (3.16), and normalized with the direct modulation approach (3.34), this stage has the role of selecting the proper capacitors to be inserted and accordingly defines the firing pulses of the semiconductors. Moreover, besides

its intrinsic goal of synthesizing the arm voltages, it also balances the energy deviation across the capacitors assembled in the same stack of cells.

This stage is typically referred in the literature to 'sort and select' algorithm. As the name describes, it combines two independent stages: the sort of the capacitors by voltage and the selection of a target number of capacitors to be inserted (N_{jk}^{*}). According to the positive or negative current flow on the arms, the capacitor voltages are sorted either in ascending or descending order. Thus, if the arm current is positive, the first N_{jk}^{*} most discharged capacitors are inserted in series to be charged, whereas the remaining are bypassed. On the other hand, whenever the arm current is negative, the first N_{jk}^{*} most charged capacitors are inserted on the arm current path, which discharge them. The frequent repetition of this procedure balances the energy storage of the capacitors assembled at the same stack.

Further details will be discussed in Chapter 7.

3.5 Control structure of the MMC

3.5.1 Introduction

In accordance with what has already been said, the inner dynamics of the MMC and its interactions with its ac network should be controlled in order to ensure safe converter operation. In order to accomplish this goal, the main assignment consists of analyzing the degrees of freedom allowed by the converter. Hence, numerous electrical variables should be considered in the converter control scheme, such as:

- W_T - the total energy that is stored in the converter;
- W_j^{δ} - the absolute energy storage deviation on the converter legs;
- W_j^{Δ} - the energy storage deviation between the upper and lower arms of the phase unit j;
- U_{dc} or P- the voltage across the dc poles of the converter or the power that is injected towards the dc bus;

- i_j^{+-} - the electrical currents of the three-phase system ($^{+-}$ positive and negative components respectively[5]). The flow of the grid currents on the converter is illustrated in Figure 3.8.

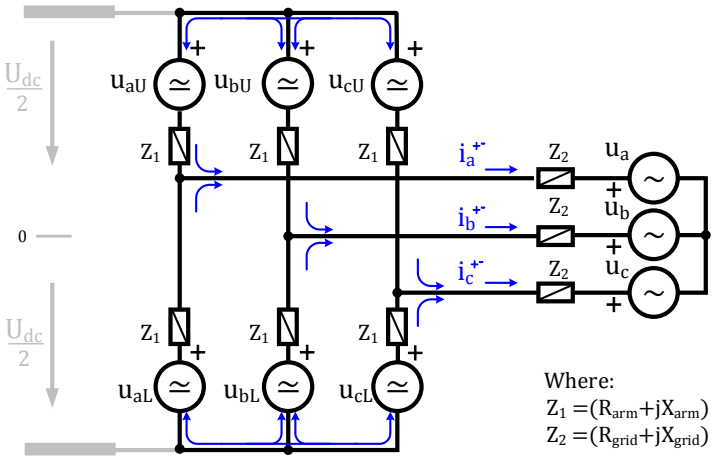


Figure 3.8: Grid currents path on the converter.

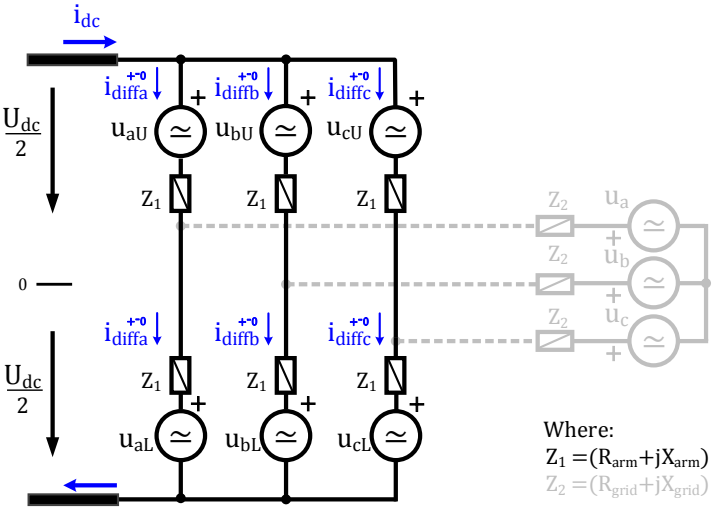


Figure 3.9: Differential currents path on the converter.

[5]The absence of connection between the middle point of the dc bus with the ac ground prevents the flow of an homopolar current. Therefore, the homopolar current controllers of the ac current have been omitted.

- $i_{diff_j}^{+-0}$ - the internal currents of the converter ($^{+-o}$ positive, negative and homopolar components respectively). The flow of the differential currents in the converter phase units is illustrated in Figure 3.9.

Conceptually, with the voltage measurement of the individual capacitors $U_{c_{jki}}$ and the knowledge of their capacitance C, how much energy is being stored on the converter arms (W_{jk}^{Σ}) (3.19) becomes noticeable. Consequently, the energy storage in each phase unit W_j^{Σ} (3.40), as well as, the existing deviations among converter legs W_{jj}^{Δ} are simply determined as (3.41).

$$W_j^{\Sigma} = W_{jU}^{\Sigma} + W_{jL}^{\Sigma} \tag{3.40}$$

$$\begin{cases} W_{ab}^{\Delta} = W_a^{\Sigma} - W_b^{\Sigma} \\ W_{bc}^{\Delta} = W_b^{\Sigma} - W_c^{\Sigma} \\ W_{ca}^{\Delta} = W_c^{\Sigma} - W_a^{\Sigma} \end{cases} \tag{3.41}$$

The energy deviation that exists between the upper and lower arms of the converter W_j^{Δ} is also obtainable as:

$$W_j^{\Delta} = W_{jU}^{\Sigma} - W_{jL}^{\Sigma} \rightarrow \begin{cases} W_a^{\Delta} = W_{aU}^{\Sigma} - W_{aL}^{\Sigma} \\ W_b^{\Delta} = W_{bU}^{\Sigma} - W_{bL}^{\Sigma} \\ W_c^{\Delta} = W_{cU}^{\Sigma} - W_{cL}^{\Sigma} \end{cases} \tag{3.42}$$

Finally, the total energy stored in the converter is given by:

$$W_T = \sum_{j \in \{a,b,c\}} W_j^{\Sigma} \tag{3.43}$$

To ensure that the converter operates with the defined pole-to-pole voltage of the dc bus U_{dc}^{*} or it injects the proper power P^{*} into the dc bus, the energy storage deviation between phase units $W_{jj}^{\Delta *}$ and arms $W_j^{\Delta^*}$, the flow of a suitable target is imposed for the inner currents $i_{diff_j}^{+-0^*}$. On the other hand, according to the targets defined for the total energy storage and the reactive power flow at the point of common coupling, a proper grid current target will be also enforced.

Along with the previous and focusing in a point-to-point dc-transmission connection, the two converters rely on different operating mode principles as identified in Figure 3.10. The MMC1, in this example, behaves

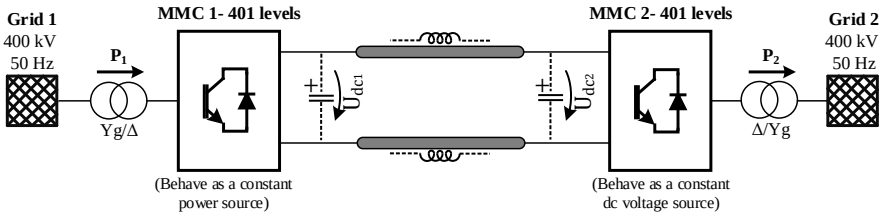


Figure 3.10: Overall control scheme of a point-to-point dc transmission link.

like a constant power source. Then, in addition to its inner energy storage control, this converter is responsible for injecting a constant power value into the dc transmission 1. On the other hand, the MMC2 is responsible for managing the power injection into the grid 2, modeled as P_2, as a function of the dc voltage U_{dc2}. Therefore, the MMC2 behaves as a dc voltage source.

From the perspective of converter control, the two operating modes are illustrated in Figure 3.11. From the measurement of the individual capacitor values, the energy amount being stored in the converter is calculated, as well as the energy deviations that may exist between its arms and legs. Then, two decoupled control loops are identified: the inner dynamics (illustrated in orange) and the interactions between the dc and ac sides of the converter (illustrated in green). In terms of ac/dc dynamics, both schemes are similar, the grid current control stage is responsible for managing the converter's emf, either in magnitude and phase angle, to accordingly handle the flow of currents between the converter and its corresponding ac grid. In respect to the inner dynamics, the control scheme determines the value of u_{diff}^{+-} to fulfill a symmetric energy distribution between the six stacks of the converter. The difference between the global control schemes shown relies on the methodology embraced to control the homopolar component of the differential currents. Then, the converter in the rectifier mode, particularly the MMC1, the i_{diff}^{0} is controlled in such a way that the converter operates as a power source which injects constant power into the dc transmission line (Figure 3.11(a)). In contrast, at the other extreme of the intercon-

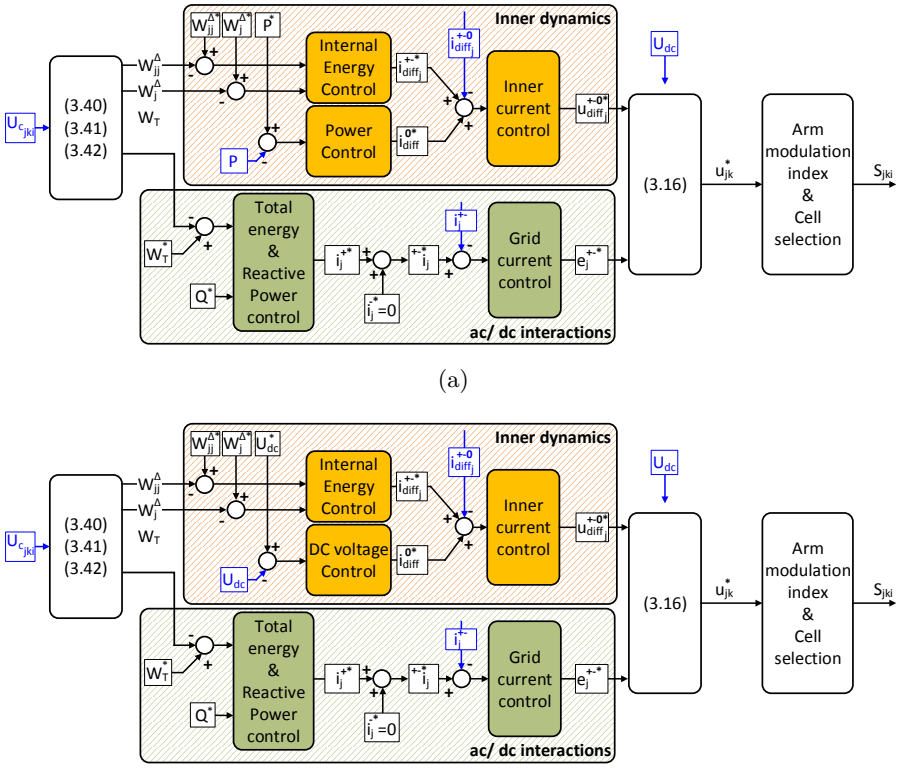


Figure 3.11: Overall control scheme of the MMC for the: (a) power source operation mode and (b) dc voltage source.

nection, the MMC2 operates in inverter mode and the i^0_{diff} is controlled in such a way that the converter operates as a dc-voltage source, which manages the injected power of the grid 2 as a function of the dc voltage value (Figure 3.11(b)).

Due to the similarities between the control schemes mentioned, the converter control design performed in this thesis is focused on the dc-voltage-based control, which is shown in Figure 3.11(b). The details of each block represented in the referred figure will be discussed in subsequent sections.

3.5.2 Grid-side current control

Introduction to vector control

The representation of grid-side currents as time-varying sinusoidal terms makes them hard to operate. In order to achieve satisfactory control performance and small-steady-state errors [72], the sinusoidal-based signals were transposed to the so-called Park domain. This transformation is characterized by an orthogonal reference frame, typically referred as *dq* frame, which rotates synchronously with the phase *a* of the electrical grid, as illustrated in Figure 3.12. Thus, the sinusoidal-based terms described on the stationary *abc* reference frame are then represented by constant values in the Park domain.

The Park transformation matrix is defined as:

$$T(\theta) = \frac{\sqrt{2}}{3}\begin{bmatrix} \cos(\theta) & \cos\left(\theta - \frac{2\pi}{3}\right) & \cos\left(\theta + \frac{2\pi}{3}\right) \\ \sin(\theta) & \sin\left(\theta - \frac{2\pi}{3}\right) & \sin\left(\theta + \frac{2\pi}{3}\right) \end{bmatrix} \tag{3.44}$$

and its inverse is:

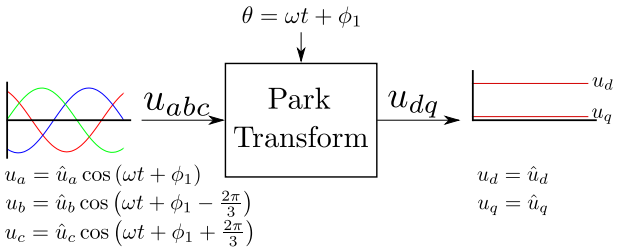
$$T^{-1}(\theta) = \sqrt{2}\begin{bmatrix} \cos(\theta) & \sin(\theta) \\ \cos\left(\theta - \frac{2\pi}{3}\right) & \sin\left(\theta - \frac{2\pi}{3}\right) \\ \cos\left(\theta + \frac{2\pi}{3}\right) & \sin\left(\theta + \frac{2\pi}{3}\right) \end{bmatrix} \tag{3.45}$$

Thus, if the Park transformation matrix $T(\theta)$ is applied to a balanced three-phase vector x_{abc}, their sinusoidal-based values are projected to the *dq* reference frame as their root mean square (*rms*) values.

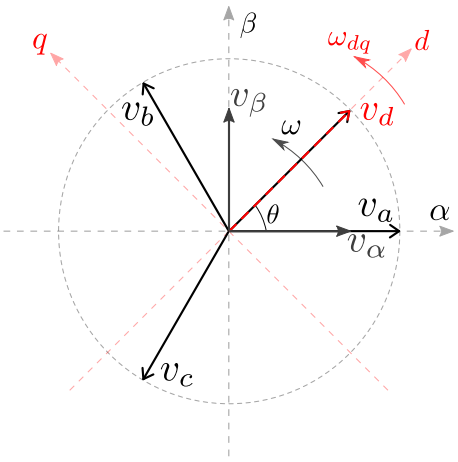
$$x_{dq} = T(\theta)x_{abc} \tag{3.46}$$

The success of the Park transform greatly depends on an accurate measuring or estimation of the phase angle of the stationary three-phase reference frame. To obtain this information, the phase-locked-loops (PLLs) are common methods adopted to achieve this goal [72–74]. A simplified schematic diagram of a PLL is shown in Figure 3.13.

In the first stage of the PLL, the voltage measurements of the three-phase grid voltages u_{abc} (3.47) are transposed to the Park domain u_{dq}



(a) Translation of the stacionary *abc* to *dq* reference frames.



(b) Combined vector representation of the three-phase (*abc*), two-phase ($\alpha\beta$) and synchornous (*dq*) reference frames.

Figure 3.12: Representation of the three-phase variables in the Park domain.

using an initial estimation. Consequently, the PLL adjusts the rotational speed of the synchronous reference frame ω' in such a way that tracks the phase angle of the line voltage "*a*".

$$u_{abc} = \sqrt{2}U \begin{bmatrix} \cos(\omega t + \phi) \\ \cos\left(\omega t + \phi - \frac{2\pi}{3}\right) \\ \cos\left(\omega t + \phi + \frac{2\pi}{3}\right) \end{bmatrix} \tag{3.47}$$

where U, ω and ϕ are the *rms* value, angular frequency and phase angle of the grid voltages respectively.

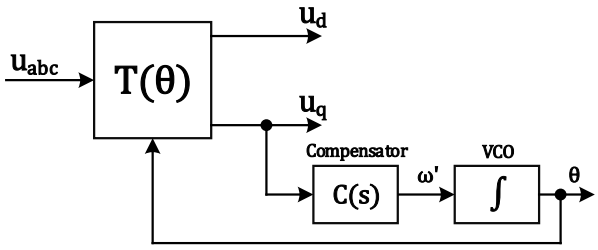


Figure 3.13: Simplified schematic diagram of a PLL.

The PLL reaches steady-state operation whenever the quadrature component of the grid voltage u_q equals zero. Under these circumstances, the rotational reference defined by the PLL is synchronous to $\omega t + \phi$ and hence the PLL is locked to the angle of the phase voltage "a" (3.48).

$$\begin{aligned} \theta &= \omega t + \phi \\ u_d &= U \\ u_q &= 0 \end{aligned} \tag{3.48}$$

Several PLL strategies have been introduced in the literature, however, since it was not the focus of this thesis, the decoupled double synchronous reference frame PLL (DDSRF-PLL) was adopted due to its satisfactory results [75, 76]. As the name suggests, the DDSRF-PLL uses two decoupled synchronous reference frames which are able to accurately estimate the angle of the grid voltage "a", even during asymmetric voltage conditions. Additionally, this PLL scheme also provides the following data:

- u_d^{PLL+} and u_q^{PLL+}: the *rms* values of the positive sequence vector of the grid voltage transposed to the dq reference frame.
- u_d^{PLL-} and u_q^{PLL-}: are the *rms* values of the negative sequence vector of the grid voltage referred on the Park domain. These variables get non-zero values whenever the grid voltages are not balanced.

The methodology used to control the grid currents is vulnerable to the operating conditions of the electrical grid. Hence, two operating scenarios were considered for the converter, namely its operation whenever connected to an electrical grid with symmetric or asymmetric voltages. Both schemes are depicted in the subsequent sections.

Grid current control- Symmetric three-phase system

Next we shall define the grid-tied MMC model (3.13) referred to in the Park domain (3.49).

$$\begin{bmatrix} e_d \\ e_q \end{bmatrix} = R_{eq} \begin{bmatrix} i_d \\ i_q \end{bmatrix} + L_{eq} \begin{bmatrix} \frac{di_d}{dt} \\ \frac{di_q}{dt} \end{bmatrix} + \begin{bmatrix} u_d \\ u_q \end{bmatrix} + \omega L_{eq} \begin{bmatrix} -i_q \\ i_d \end{bmatrix} \tag{3.49}$$

where:

$$\begin{cases} e_{dq}(t) = T(\omega t + \phi) e_{abc}(t) \\ u_{dq}(t) = T(\omega t + \phi) u_{abc}(t) \\ i_{dq}(t) = T(\omega t + \phi) i_{abc}(t) \end{cases}$$

Moreover, in the Park domain, the instantaneous real- and reactive-power components that flow into the electrical grid are defined as (3.50). However, as the equations suggest, if the quadrature component of the grid is zero, which occurs at the steady state operation of the PLL, the real- and reactive-power components become proportional to i_d and i_q, respectively.

$$\begin{cases} P = 3\left(u_d i_d + u_q i_q\right) \\ Q = 3\left(-u_d i_q + u_q i_d\right) \end{cases} \tag{3.50}$$

Applying the Laplace transform ($\mathcal{L}$ operator) to (3.49), the grid currents transfer functions can be obtained as (3.51), which are depicted in Figure 3.14.

$$\begin{aligned} I_d(s) &= \frac{E_d(s) - U_d(s) + \omega L_{eq} I_q(s)}{sL_{eq} + R_{eq}} \\ I_q(s) &= \frac{E_q(s) - U_q(s) - \omega L_{eq} I_d(s)}{sL_{eq} + R_{eq}} \end{aligned} \tag{3.51}$$

where:

$$I_d(s) = \mathcal{L}[i_d(t)]$$
$$I_q(s) = \mathcal{L}[i_q(t)]$$
$$E_d(s) = \mathcal{L}[e_d(t)]$$
$$E_q(s) = \mathcal{L}[e_q(t)]$$
$$U_d(s) = \mathcal{L}[u_d(t)]$$
$$U_q(s) = \mathcal{L}[u_q(t)]$$

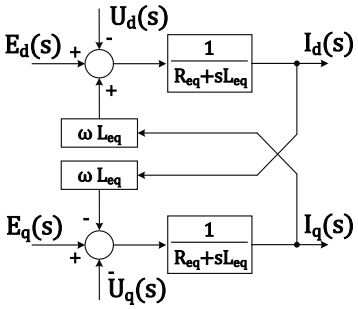


Figure 3.14: Transfer function of the grid currents in the Park domain.

From the grid current transfer function it is clear that there is a coupling between the two orthogonal axes due to the L_{eq} being a common element of the two axes. Therefore, it is relevant to eliminate the dependency between the direct and quadrature current components. Based on the transfer functions presented, the current control scheme shown in Figure 3.15 was adopted.

The presence of the feed-forward voltages U_d' and U_q' in the control scheme, which are paradoxical to $U_d^{''}$ and $U_q^{''}$, removes the association between the direct and quadrature axis. Therefore, both axes can be treated as independent, as shown in Figure 3.16.

Moreover, if it is assumed that the phase locked loop is capable of extracting the details from the grid voltages ($U_d^{\text{PLL}+} = U_d$ and $U_q^{\text{PLL}+} = U_q$) perfectly, the fact of feed-forwarding U_{dq}^{PLL+} in the current control scheme removes the grid voltage dynamics from current control. This

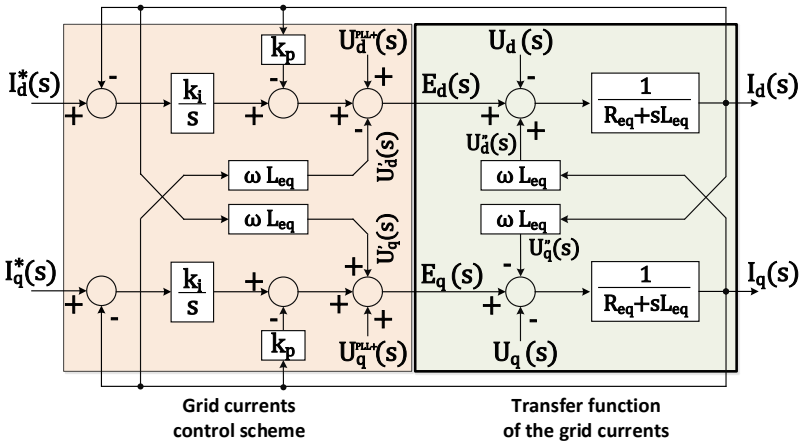


Figure 3.15: Grid current control scheme in the Park domain.

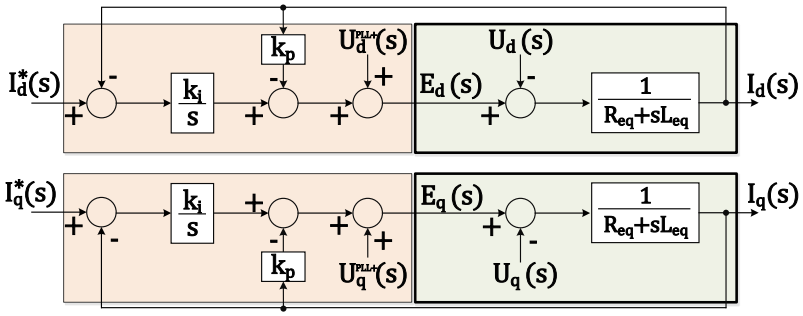


Figure 3.16: Grid current control scheme - decoupled *dq* axis operation.

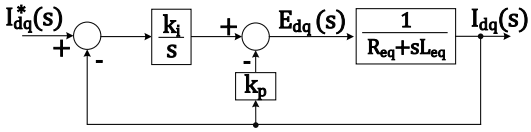


Figure 3.17: Simplified grid current control scheme on the *dq* frame.

simplifies the control scheme to the one presented in Figure 3.17. As a result, the grid current control closed loop transfer function becomes:

$$\frac{I_{dq}(s)}{I^*_{dq}(s)} = \frac{\dfrac{k_i}{L_{eq}}}{s^2 + \left(\dfrac{k_p + R_{eq}}{L_{eq}}\right) s + \dfrac{k_i}{L_{eq}}} \tag{3.52}$$

where the k_p and k_i are the constants of direct i_d and quadrature i_q current controllers, which were designed to ensure the required second order closed-loop response (see Appendix B).

The grid-side currents should be handled quickly to ensure safe operation of all the converter devices. Hence, this control loop was designed to perform with a time constant with ten times higher than the sampling period, which according to the system parameters presented in Appendix A, leads to a settling time ≈ 5 ms. Also, it was designed to have an overshoot lower than 5 % during the transient response. Then, the ΔE_{dq} value computed by the controller is given by:

$$\begin{aligned} \Delta E^*_{dq}(s) &= \frac{k_i}{s}\left[I^*_{dq}(s) - I_{dq}(s)\right] - k_p I_{dq}(s) \\ &= \frac{1.13e+05}{s}\left[I^*_{dq}(s) - I_{dq}(s)\right] - 126.91 I_{dq}(s) \end{aligned} \tag{3.53}$$

Considering the sampling rate of 10 kHz, the controller was discretized by using the Tustin bilinear transformation, resulting in:

$$\Delta e^*_{dq}(z) = 5.65\frac{z+1}{z-1}\left[i^*_{dq}(z) - i_{dq}(z)\right] - 126.91\ i_{dq}(z) \tag{3.54}$$

Consequently, the resulting system response was verified in accordance with the parameters depicted in the previous equation. The evolution of the actual and reference values for the direct and quadrature currents is illustrated in Figure 3.18. As the figure shows, the real value of i_{dq} has a second order evolution with $\approx$5ms of settling time. Hence, it is conclusive that the controller is operating as has been sized.

Considering all the assumptions made, and reinforcing the fact that the grid voltages are balanced, the global grid control scheme adopted is presented in Figure 3.19. In the next section the methodology used in scenarios in which the converter is connected to an unbalanced three-phase network is explained.

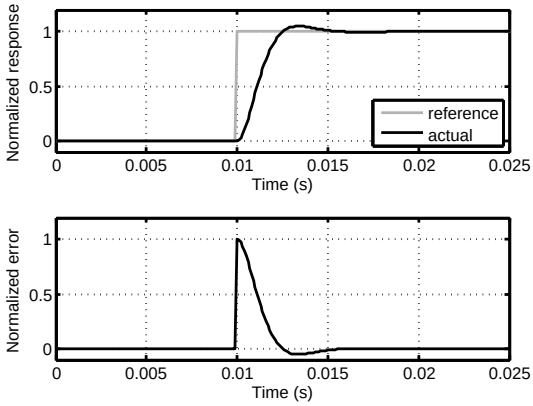


Figure 3.18: Grid current evolution experiment for a step reference change.

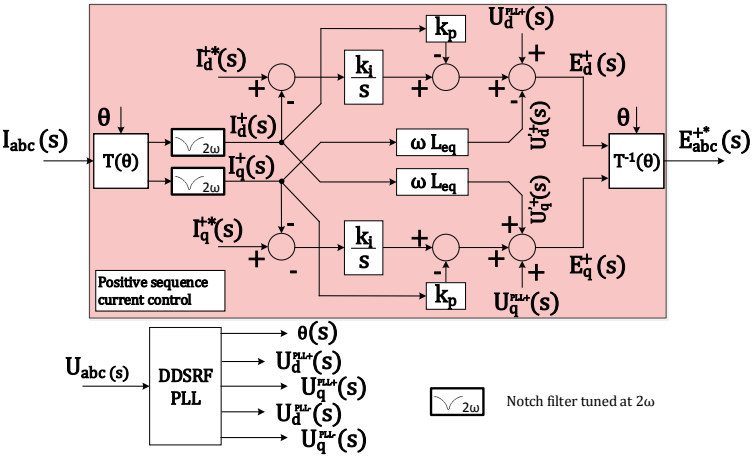


Figure 3.19: Simplified grid currents control scheme referred on the *dq* frame.

Grid current control- Asymmetric three-phase system

In this section a more general operation condition is considered where the grid voltages are no longer balanced and the voltages seen by the converter can be divided into two balanced three-phase systems, namely positive u_{abc}^{+} and negative u_{abc}^{-} sequence of voltages (3.55). In order to deduct the grid current control scheme it is assumed at this stage that

the positive and negative sequences are decoupled and thus independently controlled.

$$u_{abc}(t) = \sqrt{2}u^{+}\begin{bmatrix}\cos(\omega t+\phi^{+})\\ \cos\left(\omega t+\phi^{+}-\frac{2\pi}{3}\right)\\ \cos\left(\omega t+\phi^{+}+\frac{2\pi}{3}\right)\end{bmatrix}+\sqrt{2}u^{-}\begin{bmatrix}\cos(\omega t+\phi^{-})\\ \cos\left(\omega t+\phi^{-}+\frac{2\pi}{3}\right)\\ \cos\left(\omega t+\phi^{-}-\frac{2\pi}{3}\right)\end{bmatrix} \tag{3.55}$$

where:

u^{+} and u^{-}	are the *rms* voltages of each particular phase of the positive and negative sequences,
ϕ^{+} and ϕ^{-}	are the angles of the ac grid phase "a" for the positive and negative sequences.

Hence, applying the Park transform to the positive sequence u^{+}_{abc} with $\theta = (\omega t + \phi^{+})$, the positive reference frame u^{+}_{dq} is obtained as:

$$u^{+}_{dq}(t) = T(\omega t+\phi^{+})u^{+}_{abc}(t) \tag{3.56}$$

Repeating the procedure for the negative sequence component u^{-}_{abc} with $\theta = (-\omega t - \phi^{-})$, the negative reference frame u^{-}_{dq} is obtained as:

$$u^{-}_{dq}(t) = T(-\omega t-\phi^{-})u^{-}_{abc}(t) \tag{3.57}$$

$$\begin{cases} e^{+}_{d}(t) = u^{+}_{d}(t) + R_{eq}i^{+}_{d}(t) + L_{eq}\frac{\mathrm{d}i^{+}_{d}(t)}{\mathrm{d}t} - \omega L_{eq}i^{+}_{q}(t)\\ e^{+}_{q}(t) = u^{+}_{q}(t) + R_{eq}i^{+}_{q}(t) + L_{eq}\frac{\mathrm{d}i^{+}_{q}(t)}{\mathrm{d}t} + \omega L_{eq}i^{+}_{d}(t)\\ e^{-}_{d}(t) = u^{-}_{d}(t) + R_{eq}i^{-}_{d}(t) + L_{eq}\frac{\mathrm{d}i^{-}_{d}(t)}{\mathrm{d}t} - \omega L_{eq}i^{-}_{q}(t)\\ e^{-}_{q}(t) = u^{-}_{q}(t) + R_{eq}i^{-}_{q}(t) + L_{eq}\frac{\mathrm{d}i^{-}_{q}(t)}{\mathrm{d}t} + \omega L_{eq}i^{-}_{d}(t)\end{cases} \tag{3.58}$$

where:

$$\begin{cases} e^{+}_{dq}(t) = T(\omega t+\phi^{+})e^{+}_{abc}(t)\\ u^{+}_{dq}(t) = T(\omega t+\phi^{+})u^{+}_{abc}(t)\\ i^{+}_{dq}(t) = T(\omega t+\phi^{+})i^{+}_{abc}(t)\end{cases} \qquad \begin{cases} e^{-}_{dq}(t) = T(-\omega t-\phi^{-})e^{-}_{abc}(t)\\ u^{-}_{dq}(t) = T(-\omega t-\phi^{-})u^{-}_{abc}(t)\\ i^{-}_{dq}(t) = T(-\omega t-\phi^{-})i^{-}_{abc}(t)\end{cases}$$

By applying the Laplace transform to (3.58), the grid current model referred in the positive and negative dq frames is obtained in (3.59)

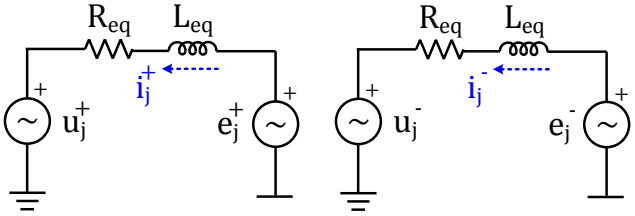


Figure 3.20: Equivalent ac dynamics circuit for the unbalanced case.

and accordingly illustrated in Figure 3.21. The grid current models referred in the positive and negative sequence are conceptually equal to the model already presented in the previous section (see Figure 3.14). Hence, the methodology presented to extract the control scheme as well as its dynamics should be replicated to the positive and negative sequence scenarios.

$$\begin{aligned} I_d^+(s) &= \frac{E_d^+(s) - U_d^+(s) + \omega L_{eq} I_q^+(s)}{sL_{eq} + R_{eq}} \\ I_q^+(s) &= \frac{E_q^+(s) - U_q^+(s) - \omega L_{eq} I_d^+(s)}{sL_{eq} + R_{eq}} \\ I_d^-(s) &= \frac{E_d^-(s) - U_d^-(s) + \omega L_{eq} I_q^-(s)}{sL_{eq} + R_{eq}} \\ I_q^-(s) &= \frac{E_q^-(s) - U_q^-(s) - \omega L_{eq} I_d^-(s)}{sL_{eq} + R_{eq}} \end{aligned} \tag{3.59}$$

As previously described with the balanced operation of the ac grid, the closed-loop response of the ac grid current control is described as:

$$\frac{I_{dq}^{+-}(s)}{I_{dq}^{+-*}(s)} = \frac{\dfrac{k_i}{L_{eq}}}{s^2 + \left(\dfrac{k_p + R_{eq}}{L_{eq}}\right) s + \dfrac{k_i}{L_{eq}}} \tag{3.60}$$

where the k_p and k_i are the constants of direct i_d and quadrature i_q current controllers, which were designed to ensure the required second order closed-loop response (see Appendix B).

In practice, the control of the grid currents is summarized in Figure 3.22. During the balanced voltage conditions of the network, the

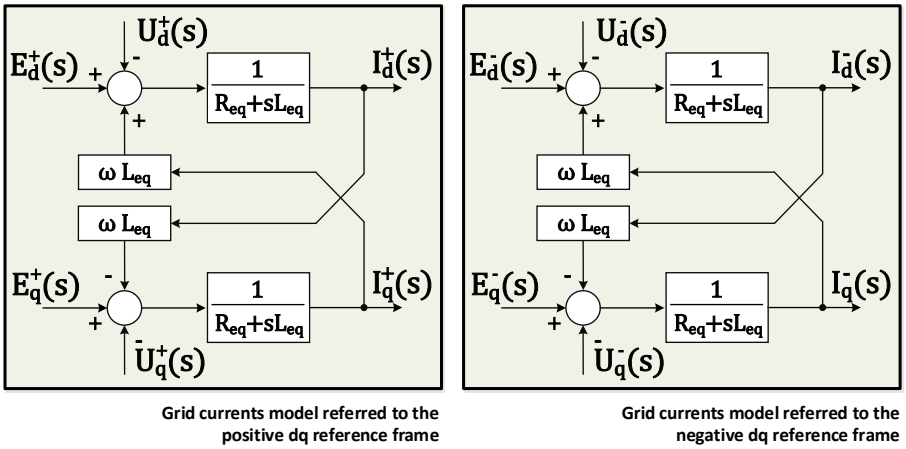


Figure 3.21: Grid current model transposed in the positive and negative dq reference frame.

negative sequence vectors of the grid voltage is zero and, therefore, a negative sequence component of the grid currents does not exist. Thus, once the Park transform is applied to $I_{abc}(s)$, the extracted $I_{dq}^{+-}(s)$ values have constant values. In contrast, if the converter is handling unbalanced ac currents, whenever they are measured and transformed into the positive and negative rotational frames, the positive and negative sequences interact with each other and a current ripple at twice the grid frequency 2ω is generated in $I_{dq}^{+}(s)$ and $I_{dq}^{-}(s)$ [77]. To remove those oscillations notch filters were added after the Park transformation matrix (see Appendix A).

In accordance with Figure 3.22, the interfaces of the overall current control structure are subdivided in inputs (I) and outputs (O), as:

- (I) The grid current targets for the positive (i_{dq}^{+*}) sequence. The direct and quadrature current components address the real and reactive power flow injection into the ac grid (3.50), respectively;
- (I) The grid current targets for the negative (i_{dq}^{-*}) sequence. These current components were set to zero in order to guarantee a balanced three-phase current injection into the ac grid even during

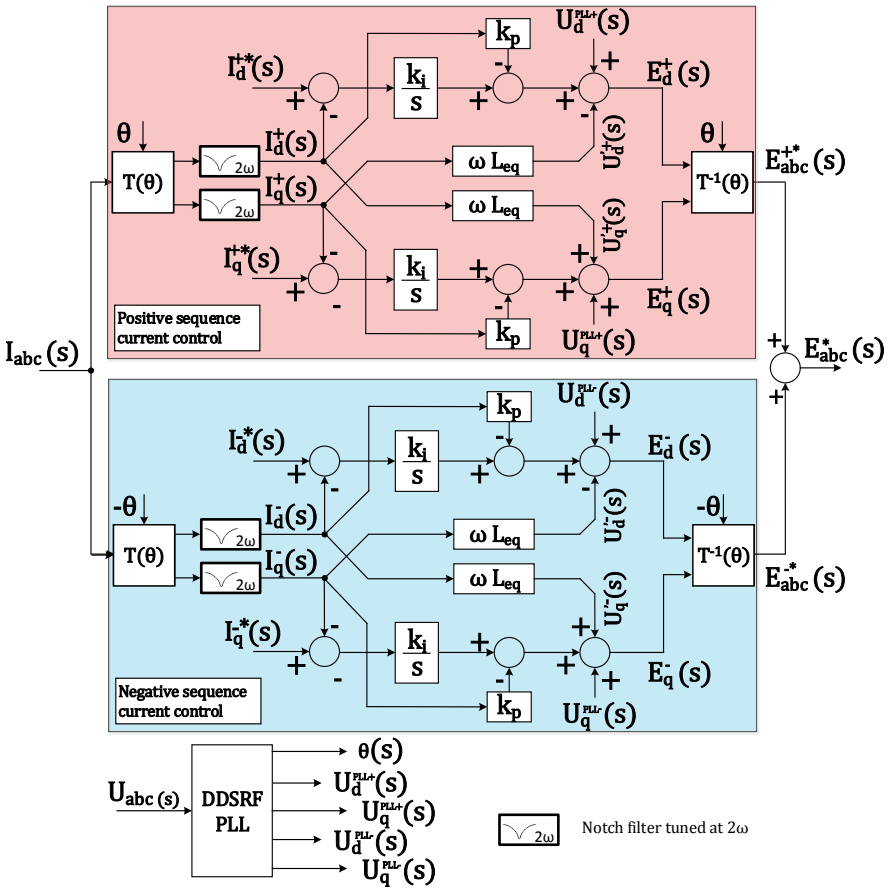


Figure 3.22: Overall scheme of grid current control under unbalanced grid conditions.

the unbalanced grid voltage conditions;

- (I) The measures of the grid currents i_{abc};
- (I) The data determined by the DDSRF-PLL, specifically: the angle of the grid voltage θ and the grid voltages transposed in the positive and negative dq reference frames (u_{dq}^{PLL+} and u_{dq}^{PLL-}) ;
- (O) The voltage targets for the *emf* of the converter e_{abc}^{*}.

3.5.3 Total energy storage control

As pointed out in section (3.2.1), the power that comes to each phase unit from the dc transmission link P_{in}, respectively defined as $i_{dc}U_{dc}$, globally charges its capacitors. On the other hand, each leg of the converter is responsible for sending the power P_{out} to the ac grid, accordingly defined by $e_j i_j$, reducing its energy storage amount. Therefore, if the power losses are neglected, the global energy storage dynamics are described as:

$$\frac{dW_T}{dt} = P_{in} - P_{out} \tag{3.61}$$

Acknowledging that the dc input power is not locally controlled, the real power that is injected into the ac grid is managed in order to address the desired value for converter energy storage. Based on the previous equation, the control diagram for the global energy storage presented in Figure 3.23 was defined. As the figure illustrates, depending on the

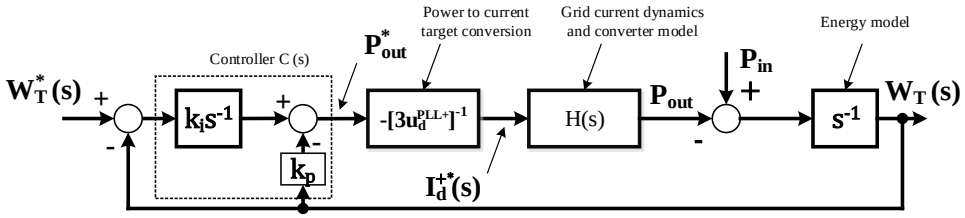


Figure 3.23: Block diagram of the total energy storage control.

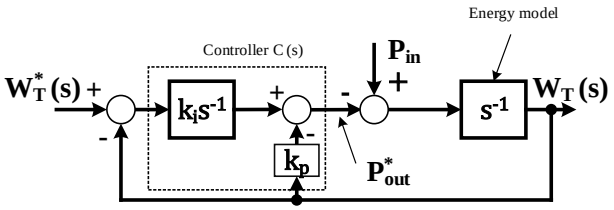


Figure 3.24: Simplified block diagram of the total energy storage control.

real and target values for the energy storage, the controller $C(s)$ define a set-point for the active power flow injection into the network. According to the existing linearity between the real-power flow component and the direct current component i_d (3.50) (whenever the $u_q^{PLL+} = 0$), the

target for the active current injection i_d^{+*} into the ac grid is defined. Consequently, the inner cascaded grid current control loop imposes the flow of the referred-to current target, and the inherent power flow target. Assuming that the controller $C(s)$ is designed with much lower dynamics than the grid current control loop, the grid current dynamics can be neglected from the energy control stage. In this view, the block diagram can be simplified to the one presented in Figure 3.24. Focusing on the simplified block diagram of the energy storage control loop, its dynamics are described as:

$$\frac{W_T(s)}{W_T^*(s)} = \frac{k_i}{s^2 + k_p s + k_i} \tag{3.62}$$

The k_p and k_i parameters of controller $C(s)$ define the behavior of the system dynamics. As the equation suggests, the proportional and integral part of the controller can be designed to impose a second-order system response (see Appendix B). Moreover, to avoid eventual disturbances between the cascaded control loops (energy storage and grid power injection), the dynamics of W_T were established to be much slower than its inner loop. Therefore, the settling time of this control loop was settled to 100 ms[6], with a maximum overshoot allowed of 5%. Hence, in accordance with Appendix B, the output power target $P_{out}^*(s)$ computed by $C(s)$ is given by:

$$\begin{aligned} P_{Tout}^*(s) &= \frac{k_i}{s}\left[W_T^*(s) - W_T(s)\right] - k_p W_T(s) \\ &= \frac{3766.7}{s}\left[W_T^*(s) - W_T(s)\right] - 84.71 W_T(s) \end{aligned} \tag{3.63}$$

The bilinear transformation (Tustin) was embraced to discretize the previous transfer function for a sampling frequency of 10 kHz:

$$P_{Tout}^*(z) = \overbrace{0.1883}^{k_i}\frac{z+1}{z-1}\left[W_T^*(z) - W_T(z)\right] - \overbrace{84.71}^{k_p} W_T(z) \tag{3.64}$$

To validate the performance of this controller, a simulation of the system response to a change in the reference $W_T^*(z)$ is performed. The

[6]The settling time of the grid currents was set to 5ms, 20 times faster that the energy control loop.

progress of the $W_T(z)$ compared to its target is shown in Figure 3.25. The system exhibit a damped response close to the specified second order system. In practice, as illustrated in Figure 3.26, from the discrete

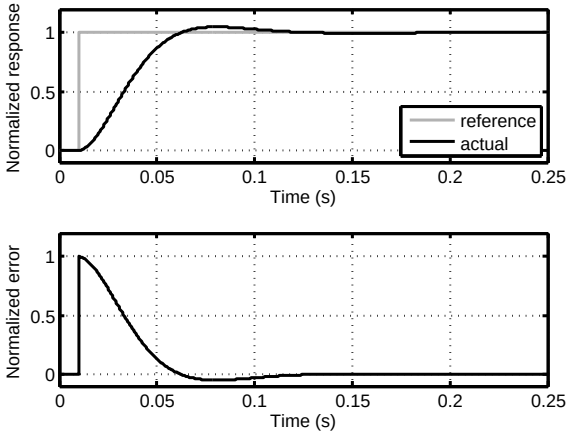


Figure 3.25: Energy storage evolution for the step reference change.

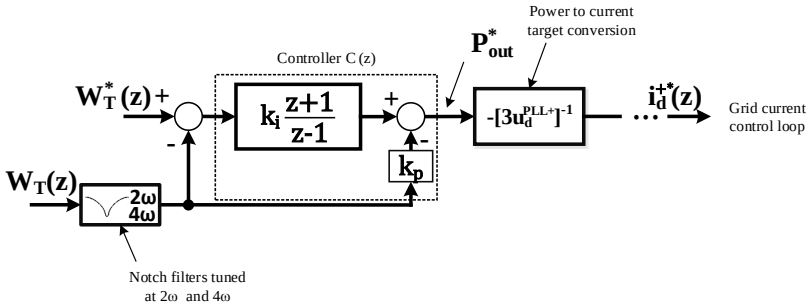


Figure 3.26: Block diagram of the total energy control scheme adopted.

measurements of the individual voltages of the SM capacitors and their capacitance, the total energy storage of the converter is determined as (3.6), (3.19), (3.40) and (3.43). As explained in Section 3.2.2, the energy storage W_T has considerable harmonic content at 2ω and 4ω, which characteristics depend on the operating conditions of the converter. If not removed from the measurement, the 2ω will be amplified by the controller and afterwards injected into i_d^{+*}, which is not desirable. Hence, a notch filter tuned to the corresponding frequencies was considered to remove these parasitic harmonic elements (see Appendix C).

In accordance with Figure 3.26, the interfaces of this control structure are subdivided in inputs (I) and outputs (O), as:

- (I) Total energy storage target for the MMC W_T^*;
- (I) The 6N voltage measurements of the capacitors of the MMC $U_{c_{jki}}$ (to quantify W_T);
- (I) Magnitude of the positive sequence of the network voltage u_d^{PLL+} (to make the active power to the active current target conversion);
- (O) Direct current component of the positive sequence target i_d^{+*}.

By combining the total energy storage and the grid current control schemes, the overall control scheme for the MMC's external dynamics is depicted in Figure 3.27. Two cascaded loops can be identified: an inner loop that manages the converter *emf* target e_j^* as a function of the grid current targets. In addition, the total energy storage and the reactive power flow targets define the grid current targets for the positive sequence.

The control of the inner dynamics of the converter will be addressed in the following sections.

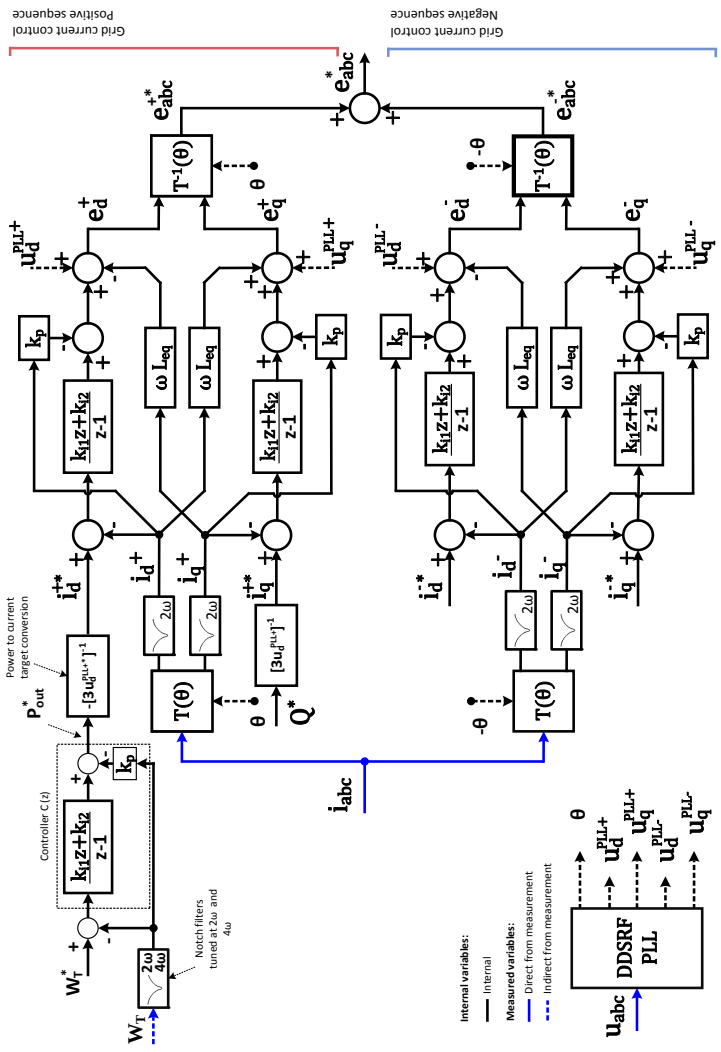
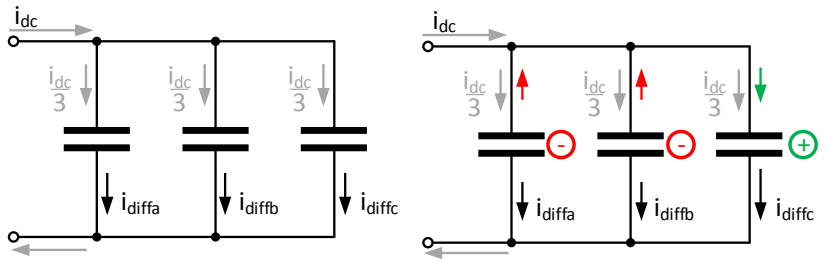


Figure 3.27: Overall control diagram of MMC dc/ac interactions.



(a) (b)

Figure 3.28: Distribution of the differential dc current components over the converter legs: for the (a) balanced and (b) unbalanced energy storage operation.

3.5.4 Differential current control

The differential currents that flow between the converter legs can be divided into several harmonic elements. Each particular harmonic is used to address a particular goal, such as energy balancing control, between the upper and lower arms (vertical balancing) and/or between the converter legs (horizontal balancing). Hence, as introduced in Section 3.2.1, two main current harmonic frequencies are expected to flow between the converter phase units (i_{diff_j}):

- dc component (0ω) - its purpose is to manage the energy storage of each phase unit. In practice, two dc current components may coexist in the converter, as illustrated in Figure 3.28. The dc current component coming from the HVdc transmission line is subdivided into the converter legs. When the network is balanced and the converter operates at steady state conditions, the dc current is equally spread by its three legs (Figure 3.28(a)). On the other hand, for instance, if for some reason, it is required to increase the energy storage of the phase unit c over the others, an additional dc current is temporary imposed to flow between the converter legs (Figure 3.28(b)), which unbalances the dc current over the converter legs.

- ac component (ω) - the scope of the ω current component is the energy balancing over the upper and lower arms of the converter. This current flows between the converter legs, affecting neither the dc nor ac currents that flow into the converter.

- ac component (2ω) - an additional harmonic frequency with 2ω may circulate internally on the converter. Either as a consequence of the arm modulation technique used or as a repercussion of the control scheme adopted. This harmonic order component can be used to achieve some goals as the reduction of the voltage fluctuation on the capacitors or the reduction of the peak current of the arms, with the drawback of generating higher losses [78]. In this thesis, priority was given to converter efficiency, and hence this harmonic frequency was intrinsically removed due to the use of the direct modulation (see Section 3.3.1).

By applying the Laplace transform to the differential currents model referred to the stationary frame *abc* (3.10), the transfer function model $G(s)$ is obtained as:

$$G(s) = \frac{I_{diff_j}(s)}{U_{diff_j}(s)} = \frac{b}{s+a} \tag{3.65}$$

where:

$$\begin{aligned} U_{diff_j}(s) &= \mathcal{L}[u_{diff_j}(t)] \\ I_{diff_j}(s) &= \mathcal{L}[i_{diff_j}(t)] \\ a &= \frac{R_{arm}}{L_{arm}} \\ b &= \frac{1}{2L_{arm}} \end{aligned}$$

According to the specifications of the inner currents, due to the energy storage asymmetries between the converter legs the inner current controllers should be able to manage asymmetric dc and ac current components. Therefore, two independent controllers ($C_1(s)$ and $C_2(s)$) were selected to individually control the 0ω and ω harmonic frequencies of I_{diff_j} as Figure 3.29 illustrates. Depending on the error (ϵ) between

the measured and target values for the differential current, the corresponding controllers determine the set-point for the differential voltage drop $U_{diff_j}^{+-0*}(s)$. Assuming that the converter is composed of a large number of SMs and thus the real voltage drop on the series connected impedances is identical to its reference (3.66), the inner current control loop can be simplified to the one presented in Figure 3.30.

$$U_{diff_j}^{+-0*}(s) \approx U_{diff_j}^{+-0}(s) \tag{3.66}$$

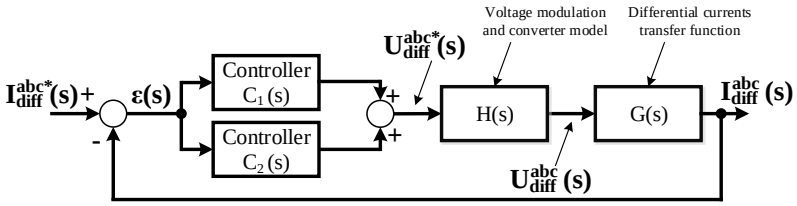


Figure 3.29: Block diagram of the inner currents control.

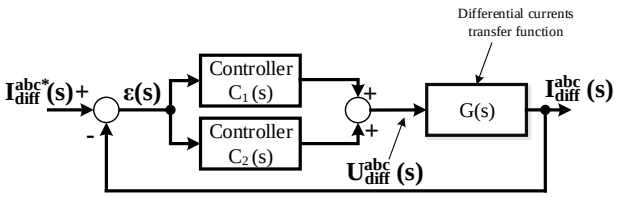


Figure 3.30: Simplified block diagram of the inner currents control.

Assuming that both controllers do not disturb each other's performance, the design of $C_1(s)$ and $C_2(s)$ was independently addressed according to the control of the dc and ac components of the inner currents respectively.

Design of the controller C_1

The control of the dc component of the inner currents is ensured by the controller C_1 and its design was based on the internal model principle (IMP). Moreover, the closed-loop system dynamics were intended to behave as a first-order system to step changes in $I_{diff}^{abc[dc]*}(s)$[7]. Hence,

[7] $I_{diff}^{abc[dc]*}(s)$ is the dc component of $I_{diff}^{abc*}(s)$, which is presented in Figure 3.30.

according to the IMP, the controller $C_1(s)$ should be composed by two parts:

$$C_1(s) = \frac{P(s)}{\Gamma_r(s)} \tag{3.67}$$

First, the nature of the controller denominator $\Gamma_r(s)$ should have the same nature as the reference signal that is requiring tracking. Therefore, the if the inner current targets vary as a step, then the controller $C_1(s)$ admits a pole at frequency zero in order to track step-based references:

$$\Gamma_r(s) = s \tag{3.68}$$

The consequent step in the design of $C_1(s)$ is the delineation of the time response of the closed-loop system, which can be addressed by the internal mode control principle on the consequent design of the controller numerator $P(s)$ (see appendix B). In turn, the numerator $P(s)$ should be composed of two parts. First, as a first order response of the system to a step change at its input $I_{diff}^{abc[dc]*}(s)$ was demanded, the low-frequency pole of the process $G(s)$ should be eliminated from the open-loop transfer function $L(s)$ (3.69).

$$L(s) = \frac{I_{diff}^{abc[dc]}(s)}{\epsilon(s)} = C_1(s)G(s) \tag{3.69}$$

where:

$\epsilon(s)$	is error between the reference and actual value of $I_{diff}^{abc[dc]}(s)$,
$C_1(s)$	is the transfer function of the controller in the Laplace domain,
$G(s)$	is the transfer function of the differential currents in the Laplace domain (it was defined in (3.65))

Hence, the inverse transfer function model of $G(s)$ was included in the controller numerator. Secondly, the time constant τ of the closed-loop system dynamics should be also included in $C_1(s)$. Thus, the final form of the controller is:

$$C_1(s) = \frac{P(s)}{\Gamma_r(s)} = \frac{1}{\tau}\frac{G^{-1}(s)}{\Gamma_r(s)} = \frac{1}{\tau s}\left(\frac{s+a}{b}\right) \tag{3.70}$$

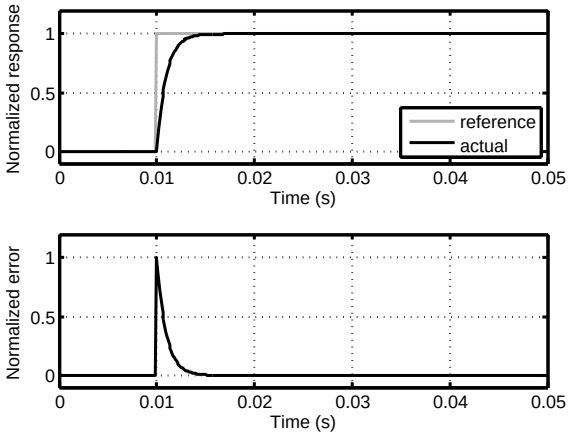


Figure 3.31: Inner current evolution for a step reference change.

The differential currents of the converter should be rapidly controlled to ensure safe operation on all its devices, in particular, its semiconductors. Hence, for this control loop, it was designed to perform with a time constant ten times higher than the sampling frequency which, according to the system parameters presented in Appendix A, leads to τ= 1 ms. Then, the controller transfer function was obtained:

$$C_1(s) = \frac{100s + 200}{s} \tag{3.71}$$

This transfer function was then transformed to z using the Tustin bilinear transformation for a sampling frequency of 10 kHz:

$$C_1(z) = \frac{100z - 99.99}{z - 1} \tag{3.72}$$

To validate the performance of this controller, a simulation of the system response to a step change at its input was performed. The progress of the $i_{diff_j}(t)$ was compared with its target shown in Figure 3.31. The system displays an exponential evolution that matches with the specified requirements.

In the next section the procedure used to design the controller C_2 to accordingly manage the ac component of $i^*_{diff_j}(s)$ is explained.

Design of the controller C_2

Regarding the design of the controller C_2, responsible for managing the ac component of $i_{diff_j}(t)$, the methodology followed was also based on the internal model principle (IMP). According to the IMP, in order to achieve an accurate command tracking, the controller should condense the representation of the reference nature [79]. Therefore, the controller is characterized by two parts. First, as mentioned, the controller should have the representation of the input reference nature at $\Gamma_r(s)$. Secondly, it should include a polynomial $P(s)$ which guarantees the required closed loop response. Then its structure should be:

$$C_2(s) = \frac{P(s)}{\Gamma_r(s)} \tag{3.73}$$

Thus, the controller to be able to track an sinusoidal curve with ω frequency (3.74), $\Gamma_r(s)$ should admit the resonant-based form of the reference $r(t)$ ($R(s)$ in the Laplace domain), specifically, a double complex pole tuned to $\pm\omega$ [79]. Moreover, to avoid stability problems associated with an infinite gain of the controller at frequency ω, the non-ideal form of a resonant controller was adopted in $\Gamma_r(s)$ (3.75), resulting in the controller form (3.76) [79].

$$r(t) = \alpha \sin(\omega t) \overset{\mathcal{L}}{\Rightarrow} R(S) = \frac{\alpha\omega}{s^2 + \omega^2} \tag{3.74}$$

$$\Gamma(s) = s^2 + \omega_c s + \omega^2 \tag{3.75}$$

$$C_2(s) = \frac{P(s)}{s^2 + \omega_c s + \omega^2} \tag{3.76}$$

The consequent design step of $C_2(s)$ is the calculation of the polynomial roots of $P(s)$ to address the closed loop system response. Next, lets decompose the plant $G(s)$ (3.65) into the polynomials $G_1(s)$ and $G_2(s)$ as:

$$G(s) = \frac{G_1(s)}{G_2(s)} = \frac{b}{s+a} \quad \Leftrightarrow G_1(s) = b, \quad G_2(s) = s + a \tag{3.77}$$

Considering the controller form (3.76) and the divided plant (3.77), in accordance with the system presented in Figure 3.30, the closed-loop

system response $T(s)$ is characterized by (3.78). The corresponding polynomial characteristic $P_{cl}(s)$ is given by (3.79).

$$T(s) = \frac{G_1(s)P(s)}{G_1(s)P(s) + G_2(s)\Gamma(s)} \tag{3.78}$$

$$P_{cl}(s) = \underbrace{G_1(s)P(s)}_{①} + \underbrace{G_2(s)\Gamma_r(s)}_{②} \tag{3.79}$$

where:

① $\quad G_1(s)P(s) = bP(s)$

② $\quad \Gamma_r(s)G_2(s) = s^3 + s^2\left(a + \omega_c\right) + s\left(\omega^2 + a\omega_c\right) + a\omega^2$

According to the polynomial characteristic of the closed loop system it is divided into the part ① which is linear to $P(s)$, and ② which is changeless and is characterized by a third order polynomial, which has its origin in the product of $\Gamma_r(s)$ (3.75) and $G_2(s)$ (3.77). Therefore, in order for it to be possible to reshape the characteristic equation $P_{cl}(s)$ and accordingly manage the dynamics of the closed loop system, the polynomial $P(s)$ should comprehend a second order polynomial with three coefficients (3.80). Thus resulting the final form of the controller $C_2(s)$ as (3.81), and the closed-loop polynomial characteristic as (3.82).

$$P(s) = p_2 s^2 + p_1 s + p_0 \tag{3.80}$$

where p_0, p_1 and p_2, are the coefficients of the polynomial $P(s)$.

$$C_2(s) = \frac{p_2 s^2 + p_1 s + p_0}{s^2 + \omega_c s + \omega^2} \tag{3.81}$$

$$P_{cl} = s^3 + s^2\left(a + \omega_c + p_2 b\right) + s\left(a\omega_c + \omega^2 + p_1 b\right) + \left(a\omega^2 + p_0 b\right) \tag{3.82}$$

The dynamics of the closed-loop scheme are determined by the previous third order expression, characterized by three roots. Let's admit a generic third order polynomial characteristic where two of its roots dominate the closed-loop dynamics as a second order system, but the third pole ϵ was settled well above the desired natural frequency (see appendix B). Then, the final equation characteristic is $P'_{cl}(s)$:

$$\begin{aligned} P'_{cl}(s) &= (s + \epsilon)\left(s^2 + 2\zeta\omega_0 s + \omega_0^2\right) \\ &= s^3 + s^2\left(2\zeta\omega_0 + \epsilon\right) + s\left(2\zeta\omega_0\epsilon + \omega_0^2\right) + \left(\epsilon\omega_0^2\right) \end{aligned} \tag{3.83}$$

Comparing the real (3.82) and the considered (3.83) characteristic equations, the proper coefficients of the $P(s)$, and accordingly the numerator of $C_2(s)$ is obtained as:

$$\begin{aligned} a + \omega_c + p_2 b &= 2\zeta\omega_0 + \epsilon & \Leftrightarrow p_2 &= \frac{2\zeta\omega_0 + \epsilon - a - \omega_c}{b} \\ a\omega_c + \omega^2 + p_1 b &= 2\zeta\omega_0\epsilon + \omega_0^2 & \Leftrightarrow p_1 &= \frac{2\zeta\omega_0\epsilon + \omega_0^2 - \omega^2 - a\omega_c}{b} \\ \omega^2 + p_0 b &= \epsilon\omega_0^2 & \Leftrightarrow p_0 &= \frac{\epsilon\omega_0^2 - \omega^2}{b} \end{aligned} \tag{3.84}$$

For the ac inner current dynamics, the settling time of the closed-loop dynamics was chosen to be 5 ms and the maximum overshoot of 5 %, which directly leads to the natural frequency response ω_0 as 1.23 krad/s and the damping factor ζ =0.69. The third root ϵ was settled at $10\omega_0$. The resulting controller is:

$$C_2(s) = \frac{1397s^2 + 2.22e06s + 1.849e09}{s^2 + s + 9.87e04} \tag{3.85}$$

The transfer function of the controller is then discretized by using the Tustin bilinear transformation for a sampling frequency of 10 kHz:

$$C_2(z) = \frac{1512z^2 - 2783z + 1290}{z^2 - 1.999z + 0.999} \tag{3.86}$$

To validate the performance of this controller, a simulation of the system response (Figure 3.30- only with C_2) to a change in the reference $i^*_{diff_j}(z)$ is performed. The progress of the $i_{diff_j}(z)$ compared to its target is shown in Figure 3.32. The system exhibits a damped response close to the specified second order system.

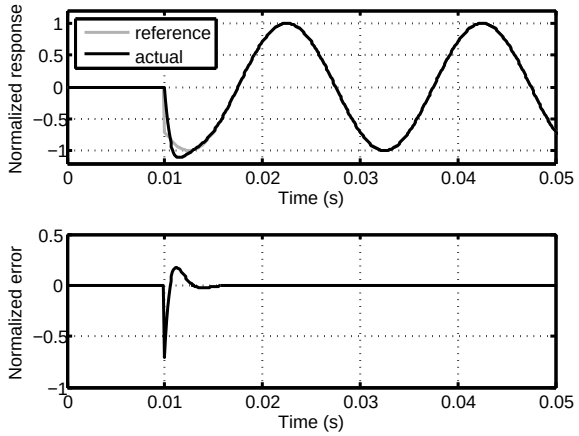


Figure 3.32: Inner current evolution for the sinusoidal reference change.

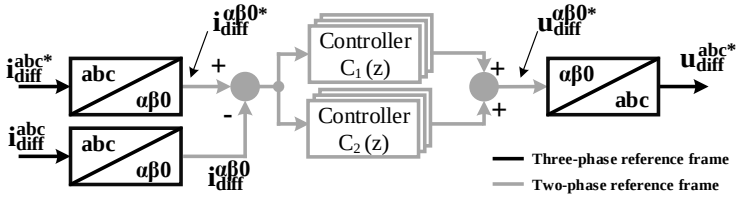


Figure 3.33: MMC's control diagram of the inner differential currents.

In practice, as depicted in Figure 3.33, the inner currents were controlled in the stationary Clarke domain (also named $\alpha\beta o$ reference frame) (3.87). The real and target values of the inner currents referred on the three-phase reference frame (i_{diff}^{abc}) were transposed to the Clarke domain ($i_{diff}^{\alpha\beta 0}$) by applying the corresponding transformation matrix C (3.88). Then, the deviation between the measured and target values of the $i_{diff}^{\alpha\beta 0}$ is handled by the controllers $C_1(z)$ and $C_2(z)$, which produce the inner voltage drop target $u_{diff}^{\alpha\beta o*}$. Afterwards, the inner voltage drop is translated to the stationary three-phase domain, by means of the inverse Clarke transformation (3.89).

$$x_{\alpha\beta 0}(t) = Cx_{abc}(t) \tag{3.87}$$

$$C = \begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & \frac{\sqrt{3}}{2} \\ \frac{1}{3} & \frac{1}{3} & \frac{1}{3} \end{bmatrix} \tag{3.88}$$

$$x_{abc}(t) = C^{-1} x_{\alpha\beta 0}(t) \tag{3.89}$$

Thus, the interfaces of the inner current control diagram are classified into inputs (I) and outputs (O), as:

- (I) The inner current targets: i_{diff}^{abc*},
- (I) The differential currents measurements: i_{diff}^{abc},
- (O) The inner voltage drop target u_{diff}^{abc*};

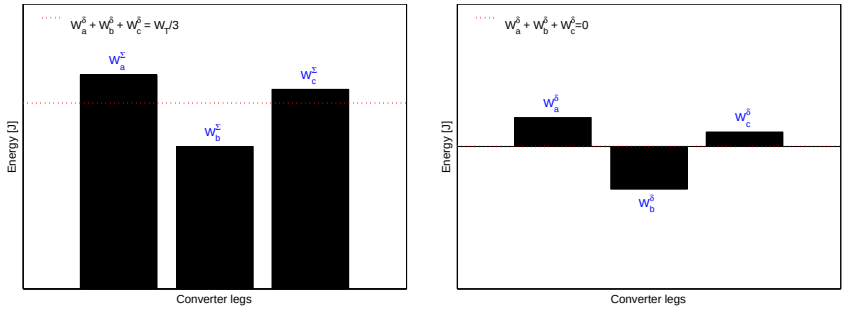
3.5.5 Internal energy storage control

Finally, the last control stage deals with the internal energy storage balancing of the converter. Depending on the energy storage targets defined for the individual arms or legs of the converter, this stage imposes a concrete power flow on the converter legs, in order to consummate the related targets.

Therefore, as introduced in sections 3.2.1 and 3.5.1, on the MMC applications two types of energy storage deviations are perceptible:

- Energy deviation between phase units $W_{jj}^{\Delta}(t)$ - which is defined as the energy storage difference between the phase units of the converter and it can be managed by a proper control of the dc current component of $i_{diff_j}(t)$ (3.26).
- Energy deviation between stacks $W_{j}^{\Delta}(t)$- which is defined as the energy storage divergence between the upper and lower stacks of the converter and it is controlled by injecting a sinusoidal current component into $i_{diff_j}(t)$ (3.27).

The internal energy storage control is addressed in the following sections.



(a) (b)

Figure 3.34: Normalization of the leg's energy storage in respect to the average.

Energy deviation between converter legs

At this stage, managing the absolute energy deviation between the converter legs is required. Hence, the first step followed was to relate the energy storage difference between the converter legs ($W_j^{\Sigma} \rightarrow W_{jj}^{\Delta}$) as:

$$\begin{bmatrix} W_{ab}^{\Delta} \\ W_{bc}^{\Delta} \\ W_{ca}^{\Delta} \end{bmatrix} = \underbrace{\begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix}}_{M_1} \begin{bmatrix} W_a^{\Sigma} \\ W_b^{\Sigma} \\ W_c^{\Sigma} \end{bmatrix} \tag{3.90}$$

where W_{ab}^{Δ}, W_{bc}^{Δ} and W_{ca}^{Δ} are the energy storage deviations between the phase units [a,b], [b,c] and [c,a], respectively. M_1 is the matrix which relates the energy storage deviation between the converter legs.

Logically, once W_{jj}^{Δ} is determined, the energy storage knowledge of the corresponding phase unit j is lost. Then, if the result W_{jj}^{Δ} is then affected by M_1^T, the energy storage deviation is obtained normalized in respect to the mean energy storage of the legs W_j^{δ}, as emphasized in Figure 3.34.

As a consequence of the relative energy values being transformed to normalized quantities ($W_{jj}^{\Sigma} \rightarrow W_j^{\delta}$) (3.91), the energy divergence between legs can be managed in an absolute manner. This is particularly interesting due to the fact that this loop can still manage the energy di-

vergence between the converter legs without impacting the total energy storage control loop.

$$\begin{bmatrix} W_a^\delta \\ W_b^\delta \\ W_c^\delta \end{bmatrix} = k \underbrace{\begin{bmatrix} 1 & -1 & 0 \\ 0 & 1 & -1 \\ -1 & 0 & 1 \end{bmatrix}^T}_{M_1} \begin{bmatrix} W_{ab}^\Delta \\ W_{bc}^\Delta \\ W_{ca}^\Delta \end{bmatrix} \tag{3.91}$$

where W_j^δ is the absolute energy deviation from W_j^Σ. k is a constant gain that maintains the energy magnitude drift unchanged from W_j^Σ to W_j^δ.

Taking into consideration the nature of W_j^Σ (3.32), let's consider the three-legs of the converter are balanced and their energy storage is defined as (3.92). Where $\bar{W}_j^\Sigma$ is the mean energy stored in the leg j, $W_{2\omega}^{rms}$ and ζ' are the *rms* and phase angle values of the second harmonic present in W_j^Σ respectively.

$$W_{abc}^\Sigma = \bar{W} + \sqrt{2} W_{2\omega}^{rms} \begin{bmatrix} \cos(2\omega t + \zeta') \\ \cos\left(2\omega t + \zeta' + \frac{2\pi}{3}\right) \\ \cos\left(2\omega t + \zeta' - \frac{2\pi}{3}\right) \end{bmatrix} \tag{3.92}$$

By applying (3.90) into the defined values for W_j^Σ, the relative energy storage deviation between the converter legs results as:

$$\begin{bmatrix} W_{ab}^\Delta \\ W_{bc}^\Delta \\ W_{ca}^\Delta \end{bmatrix} = k\sqrt{2} W_{2\omega}^{rms} \begin{bmatrix} \cos(2\omega t + \zeta') - \cos\left(2\omega t + \zeta' + \frac{2\pi}{3}\right) \\ \cos\left(2\omega t + \zeta' + \frac{2\pi}{3}\right) - \cos\left(2\omega t + \zeta' - \frac{2\pi}{3}\right) \\ \cos\left(2\omega t + \zeta' - \frac{2\pi}{3}\right) - \cos(2\omega t + \zeta') \end{bmatrix} \tag{3.93}$$

Since the three-legs of the converter were keeping the same energy amount, the average value of the previous expression over a period (π/ω) is zero. Afterwards, if $M1^T$ is applied to the previous equation, the absolute energy deviation W_j^δ is achieved as:

$$\begin{bmatrix} W_a^\Delta \\ W_b^\Delta \\ W_c^\Delta \end{bmatrix} = 3k\sqrt{2} W_{2\omega}^{rms} k \begin{bmatrix} \cos(2\omega t + \zeta') \\ \cos\left(2\omega t + \zeta' + \frac{2\pi}{3}\right) \\ \cos\left(2\omega t + \zeta' - \frac{2\pi}{3}\right) \end{bmatrix} \tag{3.94}$$

Comparing the absolute energy deviation W_j^{δ} to the absolute energy storage W_j^{Σ}, it is understood that k should be equal to 1/3 in order to have the same energy discrepancy in the W_j^{δ} and W_j^{Σ}. Finally, in order to quantify the absolute energy deviation between the converter phase units, should be considered the transformation matrix $M^{\Sigma 2\delta}$, given by:

$$\begin{bmatrix} W_a^{\delta} \\ W_b^{\delta} \\ W_c^{\delta} \end{bmatrix} = \frac{1}{3} M_1 M_1^T \begin{bmatrix} W_a^{\Sigma} \\ W_b^{\Sigma} \\ W_c^{\Sigma} \end{bmatrix}$$
$$\begin{bmatrix} W_a^{\delta} \\ W_b^{\delta} \\ W_c^{\delta} \end{bmatrix} = \underbrace{\frac{1}{3} \begin{bmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \\ -1 & -1 & 2 \end{bmatrix}}_{M^{\Sigma 2\delta}} \begin{bmatrix} W_a^{\Sigma} \\ W_b^{\Sigma} \\ W_c^{\Sigma} \end{bmatrix} \tag{3.95}$$

Depending on the absolute energy deviation target for the converter legs $W_{abc}^{\delta *}$, a controller $C(s)$ is responsible for settling a proper dc power to flow within the converter phase units to address the referred target. Hence, in accordance with the goals already mentioned for this control loop, its simplified control diagram is shown in Figure 3.35. The controller $C(s)$ imposes a finite value for the dc power flow P_{diff}^{abc*}, which is addressed by the inner current control loop $H(s)$.

As this control loop is designed to manage the energy storage deviation between the converter legs, as a requirement, the homopolar component of $W_{abc}^{\delta *}$ should be zero:

$$W_a^{\delta *} + W_b^{\delta *} + W_c^{\delta *} = 0 \tag{3.96}$$

Then, for some reason, if the particular energy amount γ needs to be sent to the phase unit "c" from "a" and "b", the corresponding targets can be for instance:

$$\begin{aligned} W_a^{\delta *} &= -0.5\gamma \\ W_b^{\delta *} &= -0.5\gamma \\ W_c^{\delta *} &= +\gamma \end{aligned} \tag{3.97}$$

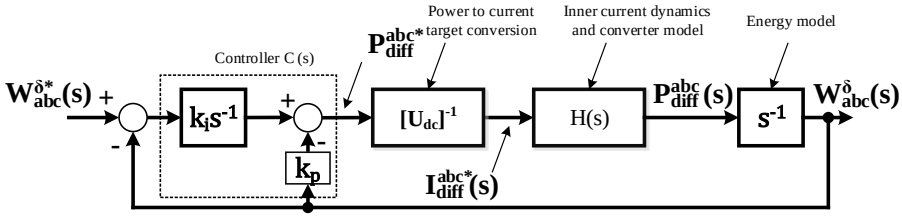


Figure 3.35: Block diagram of the leg's energy deviation control.

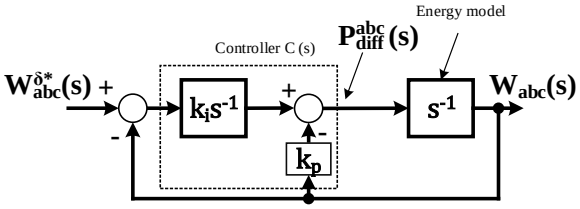


Figure 3.36: Simplified block diagram of leg's energy deviation control.

If $C(s)$ is designed to respond with one decade less time than the control loop $H(s)$, the current control loop dynamics can be neglected from the delineation of $C(s)$. Then, a simplified control loop is accomplishable, as shown in Figure 3.36, and it is characterized by:

$$\frac{W^{\delta}_{abc}(s)}{W^{\delta*}_{abc}(s)} = \frac{k_i}{s^2 + k_p s + k_i} \tag{3.98}$$

As the previous equation suggests, the controller $C(s)$ is designed in such a way that the system dynamics are expressed as a second-order system. The closed-loop system was confined to have a 200 ms of settling time with a maximum overshoot of 5 % (see Appendix B). Thus, resulting in the system:

$$\begin{aligned} P^{abc}_{diff}(s) &= \frac{k_i}{s}\left[W^{\Delta*}_{abc}(s) - W^{\Delta}_{abc}(s)\right] - k_p W^{\Delta}_{abc}(s) \\ &= \frac{941.66}{s}\left[W^{\Delta*}_{abc}(s) - W^{\Delta}_{abc}(s)\right] - 42.35 W^{\Delta}_{abc}(s) \end{aligned} \tag{3.99}$$

The previous transfer function was then discretized by using the

Tustin bilinear transformation with a sampling frequency of 10 kHz:

$$P^{*}_{Tout}(z) = \overbrace{0.04708}^{k_i}\frac{z+1}{z-1}\left[W^{\Delta *}_{abc}(z) - W^{\Delta}_{abc}(z)\right] - \overbrace{941.66}^{k_p}W^{\Delta}_{abc}(z) \tag{3.100}$$

To validate the performance of this controller, it was discretized and simulated the control scheme of Figure 3.36. The performance of the controller $C(z)$ (3.100) on the $W^{\delta}_{abc}(z)$ management is shown in Figure 3.37. The progress of the $W^{\delta}_{abc}(z)$ system exhibits a damped response with an overshoot of 5% and a settling time ≈200ms, matching with the design criteria.

In practice, the absolute energy deviation control was implemented as shown in Figure 3.38. From the individual measurements of the SM capacitors and after quantifying the energy stored in each leg of the converter, the absolute energy deviation is determined according to (3.95)[8]. Then, depending on the real and target values for $W^{\delta}_{abc}(z)$, the dc component target for the converter inner currents, and the inherent power flow, are defined.

According to Figure 3.38, in order to manage the energy deviation between the converter legs, the corresponding inputs (I) and outputs (O) of the control scheme are:

- (I) The absolute energy deviation target ($W^{\delta *}_{abc}$).
- (I) The quantification of the absolute energy deviation between the converter legs (W^{δ}_{abc}).
- (O) The dc inner current target $i^{*}_{diff_j}$;

Energy deviation between converter arms

As the name suggests, this section deals with the energy balancing between the upper and the lower arms of the converter. Similarly to

[8] As mentioned, the W^{Σ}_{j}, besides its dc value is also characterized by a relevant 2^{nd} and 4^{th} harmonics. In order to eliminate those ac components from the measurements two notch filters, respectively tuned at 2ω and 4ω were considered (see Appendix C).

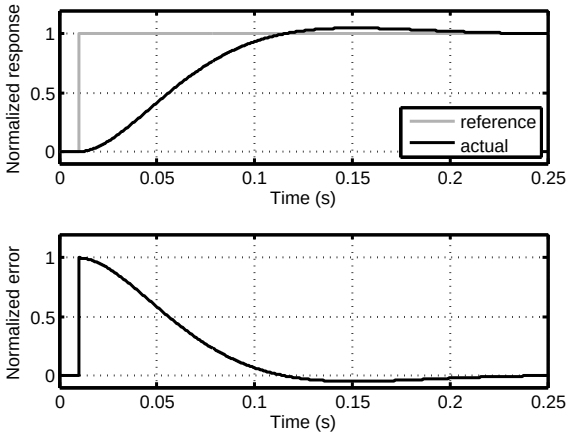


Figure 3.37: Leg's energy deviation evolution for a step reference change.

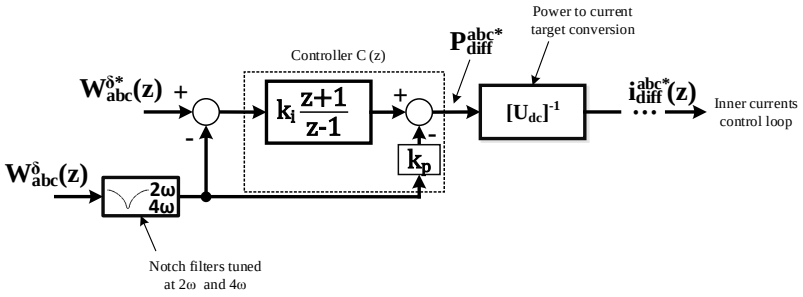


Figure 3.38: Block diagram of leg's energy deviation control adopted.

what was described in the previous section, depending on the real and target values settled for the energy storage difference between the arms W^{Δ}_{jk}, the proper power flow is imposed to flow between the converter legs, but, with an ac nature. Thus, at this stage a similar control structure to the previous section was adopted, but the controller $C(z)$ is used to manage the amplitude of the ac power flow $\hat{P}^{abc*}_{diff}$, as exhibited in Figure 3.39[9]. After defining the appropriate magnitude of the ac

[9] As mentioned, W^{Δ}_{jk} is characterized by a relevant dc value and the (ω, 3ω) harmonics. In order to eliminate those ac components from the measurements two notch

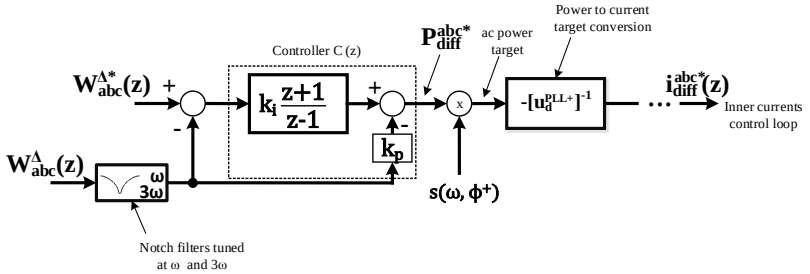


Figure 3.39: Block diagram of arm's energy deviation control adopted.

power flow $\hat{P}^{abc*}_{diff}$, it is then multiplied by an unitary-based signal "s" which has the same frequency ω and phase angle ϕ^+ of the converter *emf* (e^+_{abc}) (3.101).

$$s(\omega, \phi^+) = \begin{bmatrix} \cos(\omega t + \phi^+) \\ \cos\left(\omega t + \phi^+ - \frac{2\pi}{3}\right) \\ \cos\left(\omega t + \phi^+ + \frac{2\pi}{3}\right) \end{bmatrix} \tag{3.101}$$

The energy deviation between the converter arms has the same model as the one shown in the previous section. Therefore, the controller delineated in the previous section was also used to manage the ac power flow magnitude $\hat{P}^{abc*}_{diff}$, required to handle the energy deviation between the converter arms.

According to the figure 3.39, in order to manage the energy deviation between the converter arms, the corresponding inputs (I) and outputs (O) of the control scheme are:

- (I) The energy deviation target ($W^{\Delta*}_{abc}$).
- (I) The energy divergence quantification (W^{Δ}_{abc}).
- (I) The phase angle and frequency of the converter *emf* (ϕ and ω).
- (O) The ac target for the inner current flow $i^*_{diff_j}$;

filters, respectively tuned at ω and 3ω were taken into account (see Appendix C).

3.5.6 Voltage across the MMC's dc terminals

In the HVdc field, the dc transmission cables are characterized by having a small capacitance value between their conductor core and the metallic/ shield layers [22, 80]. Adding to the fact that there is a high-voltage drop between those layers, a non-negligible energy amount stored on the cables is foreseen and therefore they are commonly modeled as a capacitor with value C_{cable} as illustrated in 3.40(a) [80]. The positive and negative cable poles are directly connected to the respective dc poles of the converter and therefore, the converter has the additional goal of controlling the pole-to-pole dc voltage.

In order to design the pole-to-pole dc voltage control loop for the MMC electrical circuit of the displayed in Figure 3.40(b), symmetrical energy distribution between the converter legs is assumed (3.102).

$$\begin{cases} C_a(t) = C_b(t) = C_c(t) = C_j(t) \\ U_a^{\Sigma} = U_b^{\Sigma} = U_c^{\Sigma} = U_j^{\Sigma} \end{cases} \tag{3.102}$$

Thereafter, if an equal voltage drop ΔU is imposed on the converter legs $U_j^{\Sigma} + \Delta U$, it uniformly affects the differential voltage u_{diff_j}. Thus, it has no impact on the inner energy deviation, but on the power amount that is absorbed from the dc bus. Therefore, by proper management of the homopolar voltage component of u_{diff}, the energy storage of the dc transmission line W_{dc} is controlled as:

$$\frac{dW_{dc}}{dt} = P_{rec} - P_{in} \tag{3.103}$$

where P_{in} is the power coming from the HVdc transmission bus and P_{rec} is the power amount being injected into the HVdc line by the remaining rectifier.

Depending on the real and target energy storage values for the converter's dc link W_{dc} (3.104), a controller $C(s)$ is responsible for settling a proper homopolar dc power to flow on the converter phase units. Hence, in accordance with the goals already mentioned, the dc voltage control loop is depicted in Figure 3.41.

$$W_{dc} = \frac{1}{2} C_{cable} U_{dc}^2 \tag{3.104}$$

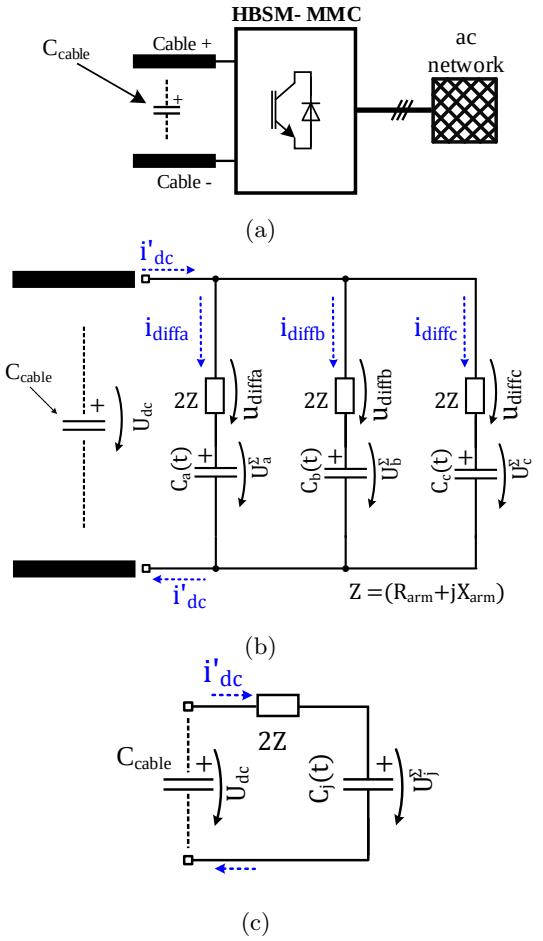


Figure 3.40: MMC equivalent circuit for the pole-to-pole dc voltage control.

The controller $C(s)$ determines the homopolar power flow target P^{0*}_{diff}, which is later converted to the homopolar target of the differential current i^{0*}_{diff}. The inner current target is consequently managed by the differential current loop $H(s)$. In the case of the controller dynamics are settled to have a response time with, at least, one decade more time than the one achieved by the differential current dynamics, the converter model can be neglected from the delineation of $C(s)$, as shown in Figure 3.42. The closed control loop dynamics are modeled

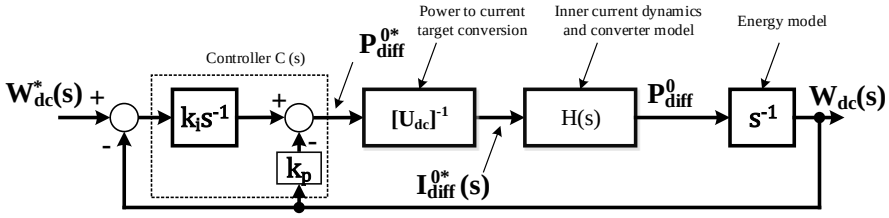


Figure 3.41: Block diagram of the dc-bus energy storage control.

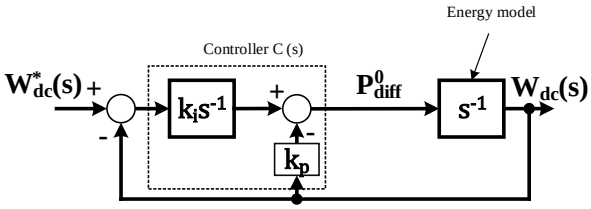


Figure 3.42: Simplified block diagram of the dc-bus energy storage control.

as:

$$\frac{W_{dc}(s)}{W^{*}_{dc}(s)} = \frac{k_i}{s^2 + k_p s + k_i} \tag{3.105}$$

As the previous equation suggest, the controller $C(s)$ is designed in such a way that the system dynamics is expressed as a second-order system. The closed-loop system was confined to have a 50 ms of settling time with a maximum overshoot of 5 % (see Appendix B). Thus, resulting the system:

$$\begin{aligned} P^{0}_{diff}(s) &= \frac{k_i}{s}\left[W^{*}_{dc}(s) - W_{dc}(s)\right] - k_p W_{dc}(s) \\ &= 10^3 \frac{15}{s}\left[W^{*}_{dc}(s) - W_{dc}(s)\right] - 169.4 W_{dc}(s) \end{aligned} \tag{3.106}$$

The previous transfer function was discretized by the Tustin bilinear transformation for a sampling frequency of 10 kHz:

$$P^{0*}_{diff}(z) = \overbrace{0.7533}^{k_i} \frac{z+1}{z-1}\left[W^{*}_{dc}(z) - W_{dc}(z)\right] - \overbrace{169.4}^{k_p} W_{dc}(z) \tag{3.107}$$

To validate the performance of this controller, it was discretized and simulated the control scheme of Figure 3.42. The performance of the

controller $C(z)$ (3.107) on the $W_{dc}(z)$ management is shown in Figure 3.43. The progress of the system exhibits a damped response with an overshoot of 5% and a settling time ≈50 ms, matching with the design criteria.

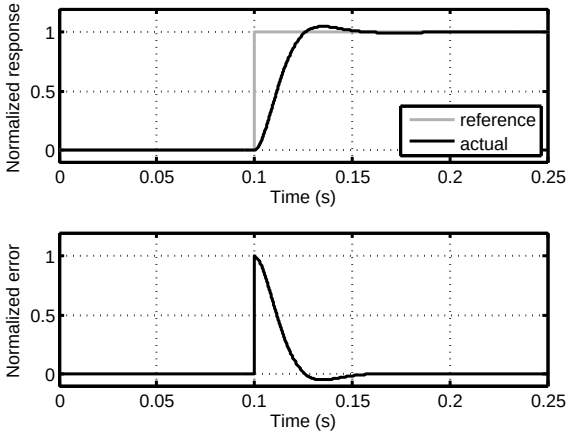


Figure 3.43: Leg's energy deviation evolution for a step reference change.

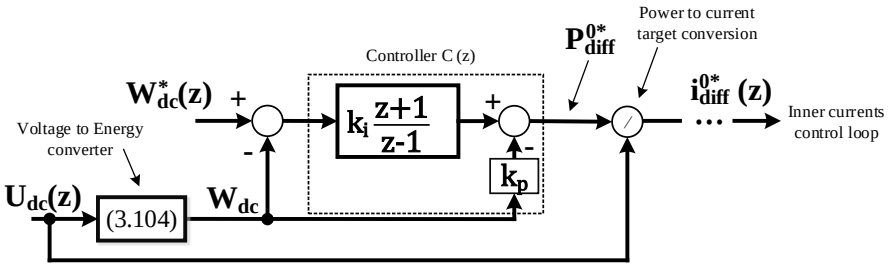


Figure 3.44: Block diagram of dc-bus energy storage control adopted.

In practice, the dc-bus energy storage control was implemented as shown in Figure 3.44. From the dc-bus voltage measurement and the C_{cable} estimation, the corresponding energy storage is determined. Then, depending on the real and target values for $W_{dc}(z)$ the controller $C(z)$ determines the homopolar differential power flow target P^{0*}_{diff}, later

translated to the differential current target i_{diff}^{0*} , which feeds the inner current control scheme.

According to Figure 3.38, in order to manage the pole-to-pole dc voltage the corresponding inputs (I) and outputs (O) of the control scheme are:

- (I) The energy storage target (W_{dc}^{*}).
- (I) The pole-to-pole dc-bus voltage (U_{dc}).
- (O) The homopolar inner current target i_{diff}^{0*};

Taking into account all the individual control loops that were presented earlier, the overall control scheme for the MMC's inner dynamics is depicted in Figure 3.45. It can be identified two cascaded loops. An inner loop characterized by the differential current control loop, that manages the differential voltage drop target $u_{diff_j}^{*}$ as a function of the differential current target referred on the Clarke domain $i_{diff_{\alpha\beta 0}}^{*}$. Then several external control loops can be observable, particularly the energy deviation control between the MMC's legs and arms, as well as, the energy storage on its dc-bus. Each energy control scheme directly impacts on the nature of the differentail current target $i_{diff_j}^{*}$.

The voltage targets defined for the MMC arms, respectively, e_j^{*} (see Figure 3.27) and $u_{diff_j}^{*}$ (see Figure 3.45) are used in combination with the dc-bus voltage measurement U_{dc} and the arms total voltage sum U_{jk}^{Σ} to modulate the arm voltages as (3.16) and (3.34).

On the next section, the MMC operating in a broad range of scenarios is examined, which allowed the validation of the elaborated control schemes presented.

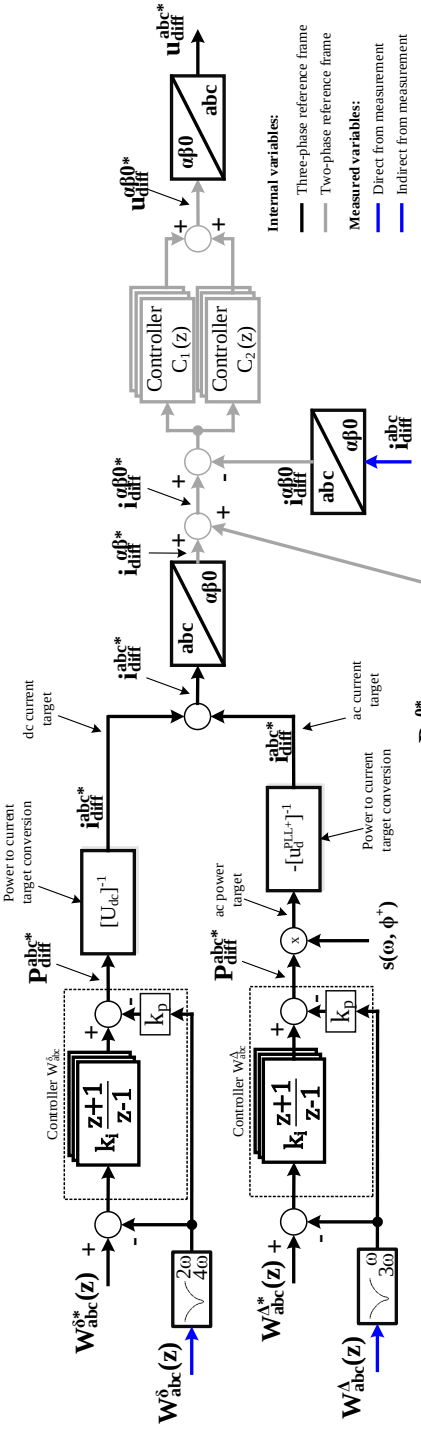


Figure 3.45: Overall control diagram of the MMC inner dynamics.

3.6 Validation of the control scheme

In order to validate the control strategy deduced in the previous section, the Thévenin-equivalent MMC model [81] and the classical cell selection method [43] were combined into the Matlab/ Simulink to analyze the converter control performance in different operating scenarios. The parameters adopted for the converter were inspired in the current MMC-HVdc-based interconnector between Spain and France, which is designated as *INELFE* and it is introduced in the Appendix A. Essentially it is composed of two independent point-to-point transmission links rated to 1 GW. One of the transmission links is presented in Figure 3.46. In this experiment, the converter 1 is responsible for absorbing from the *Grid 1* a certain amount of power P and its consequently injection into the dc transmission line. Furthermore, the converter 2, which is the focus of this study, it manages the interactions between its dc and the *Grid 2* depending on the reactive power flow and energy storage targets.

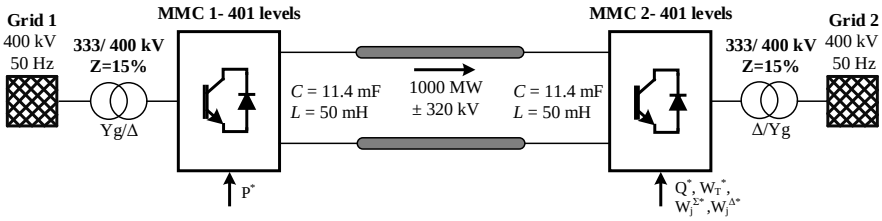


Figure 3.46: INELFE MMC-HVdc-based interconnector scheme.

The verification of the controllers was done in several stages. The first step was to study the MMC operation at the nominal and steady-state conditions, which is discussed in section 3.6.1. Latterly, it was investigated the converter behavior during several types of transients. The performance of the MMC2 whenever the power transmission is changed in presented in section 3.6.2. The management of the energy storage deviation between the converter arms and legs is respectively presented in section 3.6.3 and section 3.6.4.

3.6.1 Steady-state operation

For the steady-state operation, it was considered the converter was running with the nominal conditions. Hence, in order to maintain the energy storage equal to its nominal conditions its target $W_T^{\Sigma*}$ was established in 35 MJ. Also, no energy storage deviation between the converter arms and legs are allowed ($W_j^{\Sigma^*}$ and $W_j^{\Delta^*}$). The MMC1 was injecting 1 GW to the dc transmission link and the MMC2 besides controlling its energy storage targets, it also provides 300 Mvar to Grid 2.

The measured and target values for the arm voltages are illustrated in Figure 3.47. As can be seen, the disparity between the referred variables is diminished. Hence, the assumption initially made in (3.17) have a residual error, which can be negligible without a severe impact on deductions made. Moreover, the fact that the voltage actual and target values for the arm voltages are similar, it demonstrates that the cell selection algorithm is accomplishing its goal.

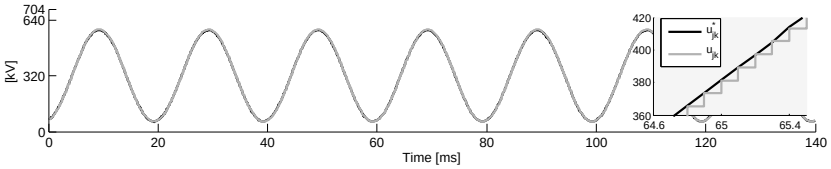
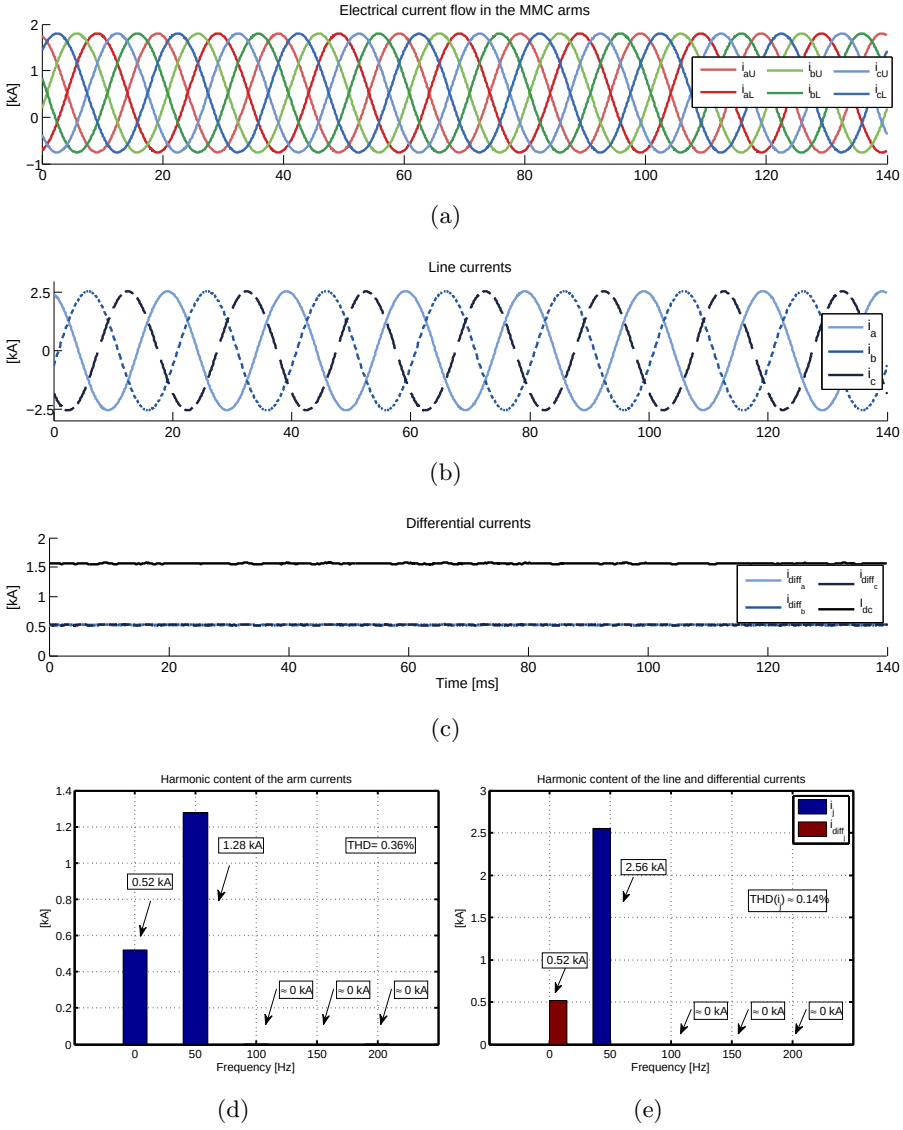


Figure 3.47: Deviation between the target and real arm voltage profiles.

In Figure 3.48 the characteristics of the electrical currents that flow on the MMC are illustrated. The most evident fact is the quality of the ac current waveforms, which incorporate very few harmonic frequencies (THD $\approx 0.36\%$). As depicted, at steady-state operation, the arm currents comprises two harmonic current frequencies. One relates the line currents (1.28 kA ac) and the second relates the inner current flow (0.52 kA dc). Regarding the differential currents (Figure 3.48(c)), they result from an equal distribution of the dc transmission line current by the three legs of the converter (3x0.52 kA). The results also show that there is no ac differential current component flowing between the converter legs and, therefore, there is a symmetrical energy distribution among the six stacks of the SMs. On the other hand, the line currents are characterized by a THD approximately equal to 0.14%, due to the

lower harmonic content generated by the MMC. In addition, the results also show that the converter arms drive half of the line currents.

Regarding the voltage sum of the capacitors and their energy stored, they are depicted in Figure 3.49. The voltage sum of the capacitor voltage clusters is balanced and centered at 704 kV. Therefore, with a 10% more voltage than the dc-bus. Since the voltage sum across the N capacitors is higher than the dc voltage, not all the stack capacitors are inserted to synthesize the required dc voltage, meaning that some SMs are redundant and they increase the converter reliability in the event of a SM malfunction or during energy unbalance transients. Regarding the mean value of the energy storage, as presented in Figure 3.49(b), each leg stores $\approx$ 11.7 MJ, precisely one third of the nominal energy storage conditions (35 MJ). In respect to the energy deviation between the upper and lower arms, as shown in Figure 3.49(c), it is centered at 0 MJ, which demonstrates that the upper and lower stacks store the same energy amount $\approx$ 5.8 MJ.



(a)

(b)

(c)

(d)

(e)

Figure 3.48: Electrical current profile during the steady-state operation.

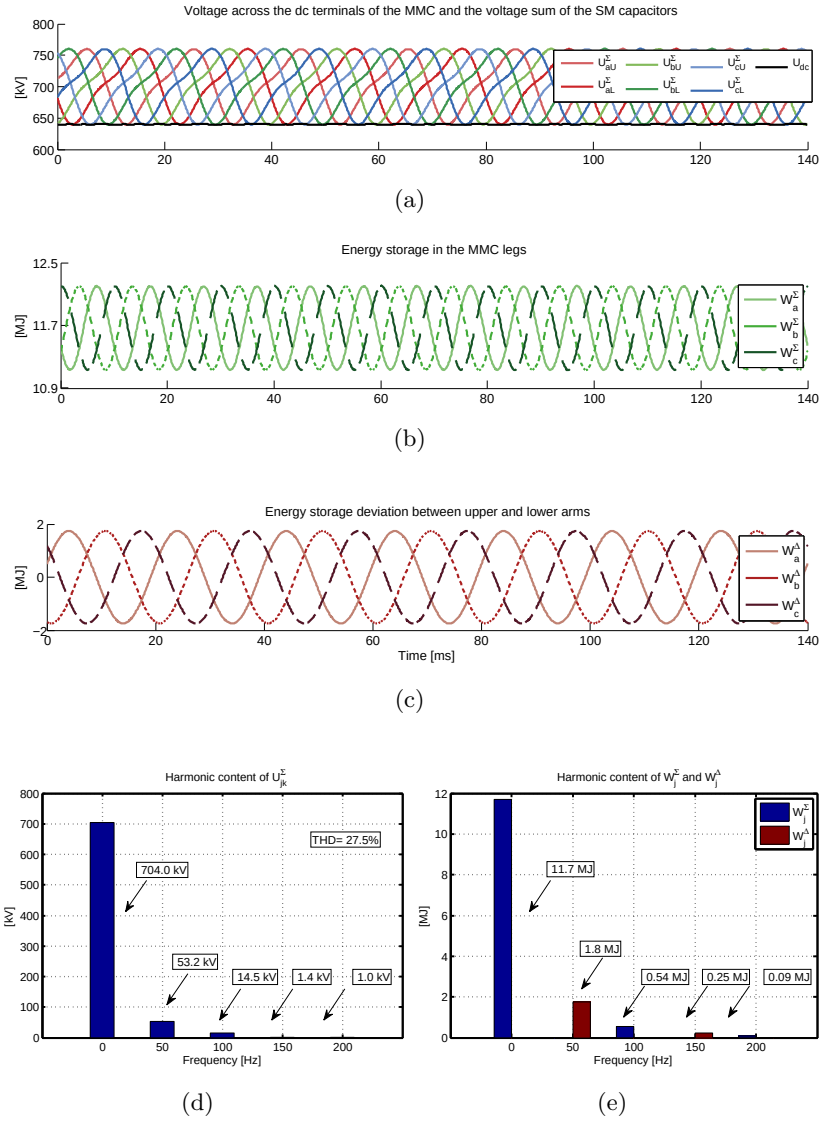


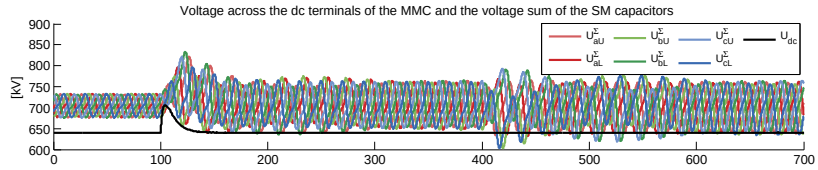
Figure 3.49: Energy storage profile during the steady-state operation.

From Figure 3.49(d), it can be seen that the harmonic spectrum of the capacitors voltage sum is composed of several components. Besides the dc voltage value, the most pertinent harmonics are the fundamental 50 Hz and its 2nd, 3rd and 4th multiples. As previously analyzed, the fact of those harmonic amplitudes are equal among the six stacks of the converter, there is an anti-phase disposition in some frequencies between the upper and lower stacks. This fact is corroborated by analyzing Figure 3.49(d) and Figure 3.49. The dc, 2nd and 4th harmonic frequencies are common elements of U_{jU}^{Σ} and U_{jL}^{Σ}, they are added together in W_j^{Σ} and they become canceled in W_j^{Δ} (see (3.6), (3.24) and (3.25)). In contrast, the fundamental and third harmonic frequencies are in phase opposition in respect to U_{jU}^{Σ} and U_{jL}^{Σ} values. Moreover, it can be also observed that the fundamental and the second voltage harmonic frequencies are the most relevant in W_j^{Δ} and W_j^{Σ}[10], respectively.

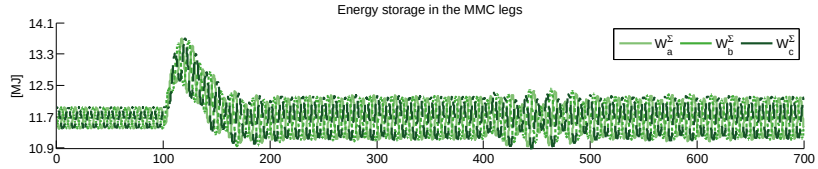
3.6.2 AC/DC interactions

This section analyses the performance of the MMC2, whenever there is a step change in the dc power transmission. The experiment starts at t=0 ms with the MMC operating at steady state, with the nominal energy storage conditions. The MMC2 is receiving 500 MW from the HVdc transmission link, which is after injected into the Grid 2 with unity power factor. Later on, at t= 100 ms, the power flow in the transmission link is increased to 1 GW. Suddenly, at t= 400 ms, the MMC2 starts to provide 300 Mvar with capacitive power factor into the Grid 2. The most relevant variables of MMC2 were recorded and illustrated in Figure 3.50.

[10]The dc value was not considered.



(a)



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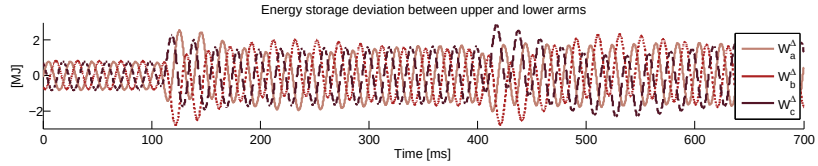

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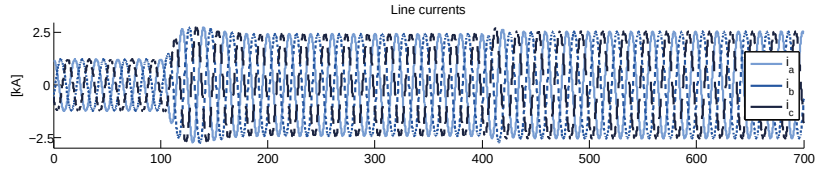
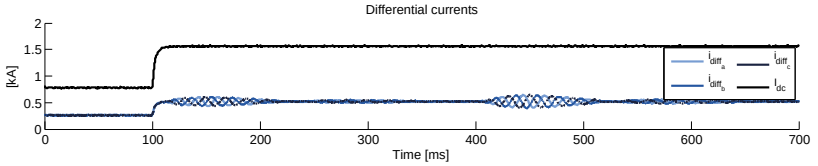


(d)



(e)

Figure 3.50: MMC performance during dynamic power flow conditions.

At the beginning of the experiment, the mean voltage sum of the capacitors is 704 kV and in accordance with the energy conditions and the differential current nature, the internally stored energy is symmetrically distributed among the six stacks of the converter. However, due to the sudden increase of the power transmission at t = 100 ms, it causes a power imbalance between the dc and the ac sides of the converter, which globally charge the capacitors. Consequently, the converter control increases the active power flow injection into the network 2 to bring back its energy storage back to the nominal conditions. In addition, the homopolar component of the differential currents is increased to restore the dc link voltage.

At the step change instant, the inserted ratio of capacitors on the upper/lower arms is different, which unequally charges the arms. Hence, as is observable in Figure 3.50(e), the inner current controllers impose the required ac current component to flow between the converter legs to overcome the referred perturbation. Once the differential currents become equal without any evidence of an ac components, the MMC2 is once again operating in the steady state mode.

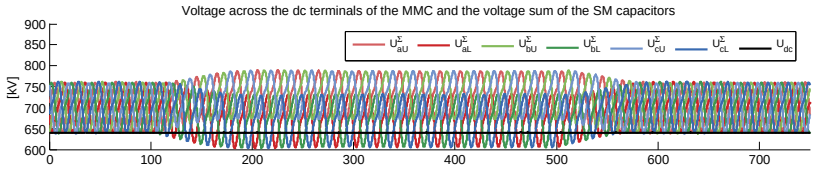
As mentioned, at t=400 ms, the reactive power set-point Q^* was step changed in the MMC2 from zero to 300 Mvar (cap.). As a result, the fact of changing the power flow conditions in the converter (hence the line current magnitude and phase angle) directly impacts the harmonic content of the capacitor voltage sum. Moreover, a small energy deviation occurs between the upper and lower stacks, which has its origin on the asymmetry between the insertion index between the upper/lower stacks at the instant of the grid current change, as was materialized in the previous transient. Again, the energy deviation control loop imposed the circulation of a sinusoidal current between the converter legs to overcome the disturbance referred to.

3.6.3 Energy deviation among arms

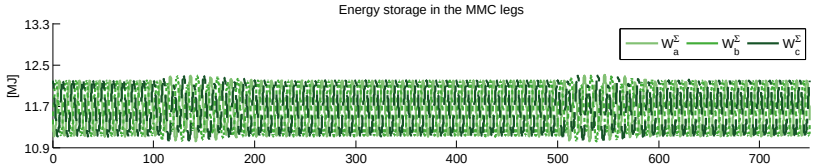
This section was considered to validate control algorithm used to manage the energy storage deviation between the converter arms. To perform this task, at t=0 s, the converter was running with the nominal power and energy storage conditions. Afterwards at t= 100 ms, the converter was forced to store more energy on the upper arms than on the lower ones. Hence, the energy deviation $W_j^{\Delta *}$ was varied from zero (upper/lower arms balanced) to 1 MJ (upper arms store 1 MJ more than the lower ones). Later on, at t= 500 ms, the set-point $W_j^{\Delta *}$ was brought back to zero, forcing the arms to be balanced again. The converter behavior is presented in Figure 3.51.

As can be seen in Figure 3.51(a), at t= 100 ms, the U_{jU}^{Σ} voltages start to deviate from the U_{jL}^{Σ}, whereas, the mean energy storage in each leg of the converter is maintained at its nominal condition of 11.7 MJ (see Figure 3.51(b)). Figure 3.51(c) illustrate that $\approx$ 200 ms after the target was varied, the upper arms become permanently 1 MJ more charged than the lower. At the contrary, when the set-point $W_j^{\Delta *}$ is varied from 1 MJ to zero, at t= 500 ms, the converter again reaches its steady-state operation with similar performance. In this vision, the energy deviation controller is responding as it was designed for.

The fact of unbalancing the energy storage of the upper/lower stacks, as can be observed in Figure 3.51(d), does not impact on the ac side of the converter. This matter only impacts the internal dynamics of the converter, as illustrated in Figure 3.51(e). As mentioned, the arm's energy storage control is performed by imposing a suitable ac power flow between the converter legs to either impose or remove any energy deviation between them.



(a)



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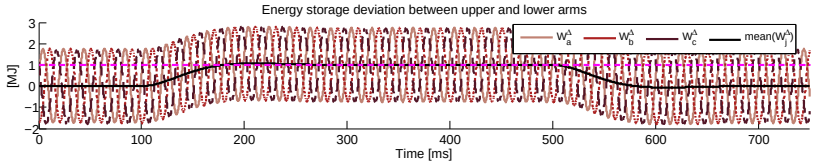

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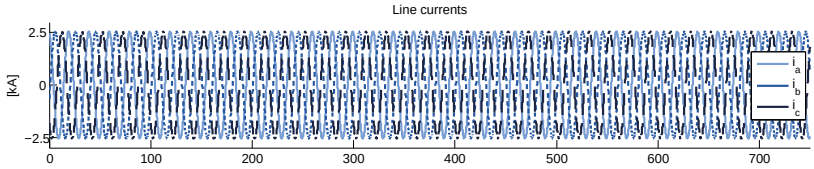

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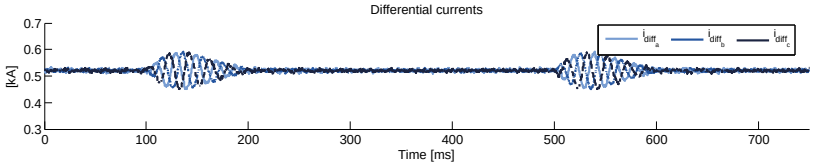


(e)

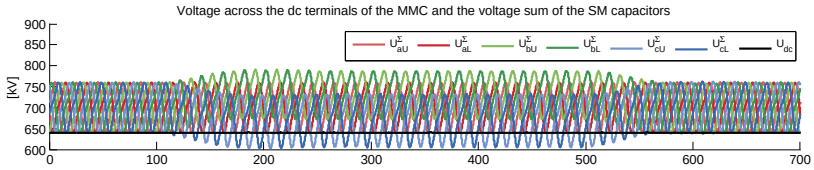
Figure 3.51: MMC operation with imbalance energy distribution (arms).

3.6.4 Energy deviation between phase units

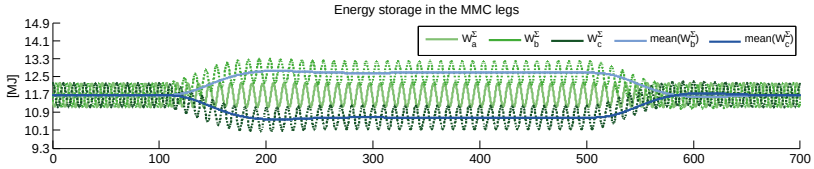
In this section the performance of the MMC2 is tested, whenever imbalancing the energy distribution between the converter legs is required. The experiment starts at t=0 ms with the MMC operating at steady state, with the nominal energy storage conditions. The MMC2 is receiving 1 GW from the HVdc transmission link and it is injecting 300 Mvar (cap.) into the Grid 2. Suddenly, at t= 100 ms, sending 1 MJ from the leg c is required to store on the leg b of the converter. Later on, at t= 500 ms, equally balancing the energy between the three legs of the converter is required. The converter performance is presented in Figure 3.52.

As can be seen in Figure 3.52(a), from the 200 ms to 500 ms, the voltage sum of the capacitors from the upper and lower arms of the phase unit "b" clearly have higher voltage than the remaining arms. Whereas, in the same time window, the arms from the phase unit "c" distinctly have less voltage, and the arms from the phase unit "b" present no changes. Focusing on the dynamics of the energy storage of the phase unit "b" and "c", either to imbalance or balance the energy distribution, as depicted in Figure 3.52(b), both present a second-order evolution with a settling time around 200 ms, which matches with the design criteria performed. The fact of moving the energy from one leg to the other does not perturb the ac power flow condition.

Furthermore, as already mentioned, to manage the total energy storage of each particular phase unit, the flow of a dc current flow is imposed on the the differential currents, as can be validated in Figure 3.52(e). To charge the phase unit "b" over the phase unit "c" (keeping "a" constant), at t=100 ms, the dc component of the differential current flow is increased/ decreased in the phase units "b" and "c" respectively. Moreover, the sum of the differential currents flow in the converter legs, particularly before and after the 100 ms, are changeless, which does not perturb the homopolar component of the differential currents and, accordingly, the total energy storage of the converter.



(a)



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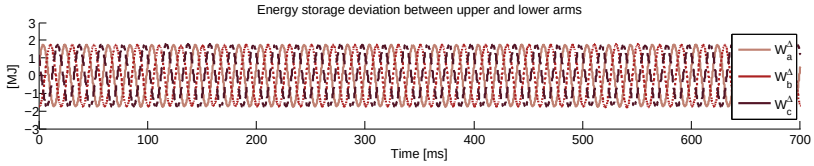

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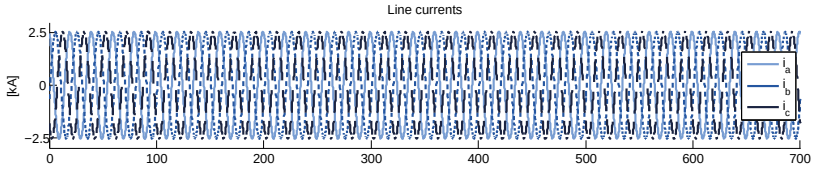

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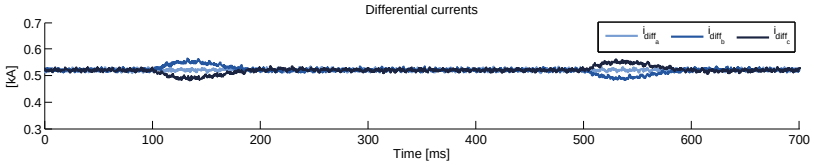


(e)

Figure 3.52: MMC operation with imbalance energy distribution (legs).

3.7 Conclusions

The modular multilevel converter (MMC) apparently has a straightforward structure, but in order to be safely operated, it requires a complex control structure. The chapter analyzes the operation of a grid-tied MMC and, additionally, it is sustained by the relevant mathematical support.

In accordance with the mathematical analysis of the converter operation, the electrical variables that are required to be controlled were investigated. Furthermore, this chapter presents the methodology followed to deduce the control scheme used in the thesis, as well as, the procedure used to design all the corresponding compensators embraced.

Finally, after explaining the converter operation and deducing the corresponding control structure, it was validated in the Matlab/Simulink environment. To perform this task, the system parameters of the state-of the-art VSC-HVdc-based interconnector between France and Spain (INELFE project) were embraced. Thus, by reproducing several operating scenarios for the converter, it is demonstrated that the designed control scheme performs in accordance with the requirements settled.

Chapter 4

Modeling techniques

4.1 Introduction

The introduction of the modular multilevel converters (MMC) supposes a revolution from the electrical point of view because it is composed of a large number of semiconductor switches. the fact of a HVdc-based converter is characterized by hundreds of electrical nodes, its simulation leads to long simulation periods. Hence, to make the MMC study more affordable, simplified models have been proposed. Depending on the converter analysis that is intended to be carried out, different types of models can be selected.

This chapter starts by describing classification of the MMC models, in respect to their accuracy and inherent computational efforts, introduced by IEEE. The MMC models goes from type 1 (most accurate) to type 6 (least accurate). In terms of the focus of this thesis, as will be emphasized later, the type 3 and 4 models are the most relevant to be studied. Thus, two literature-based models were studied and compared with two proposed models. The assessment of the simulated models was done in terms of their accuracy and the related simulation lengths retrieved.

4.2 IEEE models classification

Due to the relevant number of MMC models present in the literature, the IEEE Working Group on Modeling and Analysis of Systems Transients Using Digital Programs [32, 82] proposed a generic classification

of the corresponding models sorted by their level of detail. The classification goes from type one (more accurate) to six (less accurate) and they can be used in different kind of converter studies. For example, according to the modeling raking, the details of the converter models goes from the mathematical modeling of the semiconductors (very detailed analysis) to the representation of the electrical variables as phasors.

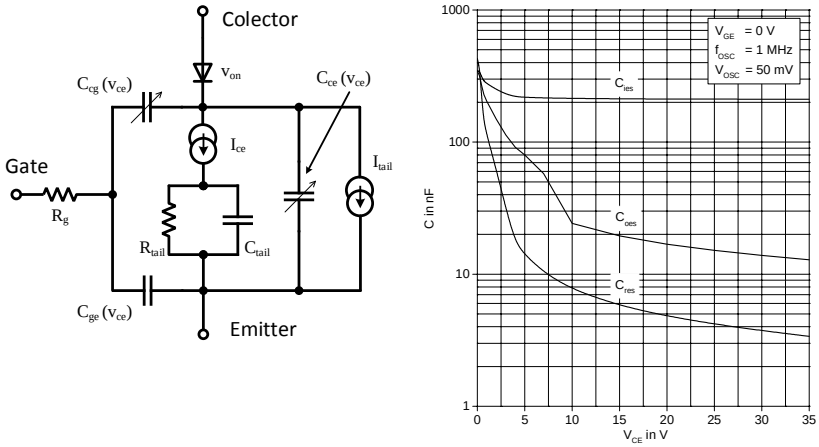
The next sections will clarify the intrinsic level of detail that characterizes each type of model.

4.2.1 Type 1

On the MMC type 1 models, the power structure of the converter is meticulously duplicated into the simulation environment and its semiconductors are characterized by differential equations or equivalent circuits. Moreover, the semiconductor parameters vary in accordance with their operating conditions, such as temperature, opening and closing times of the switches, energy dissipated, etc. Logically, this category of models provide very accurate results due to fact that they mathematically describe the physical events of its elements. As a consequence of its high-level accuracy, it requires very small time-steps (in the nanoseconds range), which attains large computational efforts and very long simulation times [83, 84].

The type 1 models, due to their high level of description, are used for very particular studies, typically, on the semiconductor level. Figure 4.1 shows an equivalent circuit of an IGBT, which can be used on the type 1-based MMC models [85]. It is a behavioral model which can accurately describe the static and dynamical characteristics, non-linear capacitance between power terminals, hard turn-off tail currents of the referred semiconductor devices. Hence, the results of a type 1 model can be a good compromise with the laboratory-based implementations [86]. Due to their high accuracy, they are particularly interesting to manufacturers that provide custom power electronics based solutions because they permit to reduce the number of iterations of the corresponding prototypes. However, from the power system studies perspective, due to

its large computational effort and detail, this group of models is not plausible [82].



(a) IGBT equivalent circuit.

(b) Typical capacitances C_x vs. collector emiter voltages v_{ce} [87].

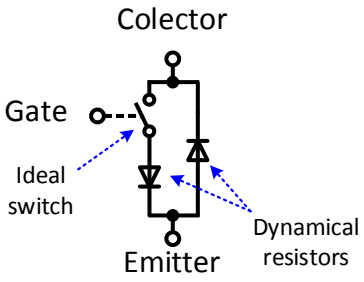
Figure 4.1: Type 1-based IGBT behavior model.

4.2.2 Type 2

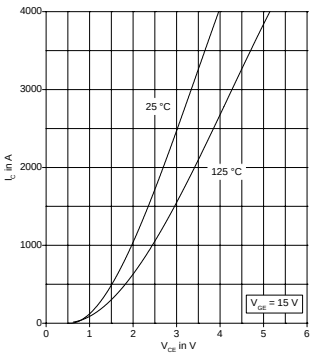
Type 2 model is a simplification of the type 1, and so relatively less accurate. In opposition to the type 1, in the type 2 model, the IGBTs are modeled as ideal switches in series with one non-linear resistor and in parallel with another non-linear resistor, as pointed out in Figure 4.2. These resistors are used to describe the non-linear on-state resistors of the semiconductors [32, 82].

The on-state resistors are represented by the *V-I* curve of the correspondent switches. Hence, the voltage drop that occurs on the IGBT or diode terminals depend on the driven current respectively done by the IGBTs or diodes. Moreover, since the switching events of the semiconductors are not described, this model is not suitable for converter studies that embrace the analysis of the IGBT behavior during the switching transients.

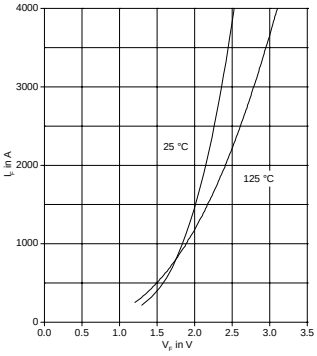
The fact of this model embraces less computational data than the previous one, it is relatively faster to simulate. The decrease of the



(a) IGBT model



(b) V-I curve of the IGBT (D1 model) [87].



(c) V-I curve of the diode (D2 model) [87].

Figure 4.2: Type 2-based IGBT behavior model.

computational time, in this case, comes with the cost of losing accuracy.

4.2.3 Type 3

In opposition to the type 2, on the type-3-based model, the resistors across the power terminals of the diodes and IGBTs can have only two discrete values, an on-based resistor r_{on} in the order of mΩ (if the switch is closed) or an off-based resistor in the order of MΩ (if the switch is open). Therefore, the value of the resistor does not depend on the magnitude of the driven current, but the correspondent cell state and the sign of the correspondent arm current [32, 82]. Hence, whenever the SM is inserted, the resistance value across its switches depends on the arm current direction. Hence, if the arm current is positive, the current flows on the IGBT, whereas, if the arm current is negative it flows on

Table 4.1: Resistance values across the semiconductors as a function of the cell state and the arm current direction.

Cell state	Arm current sign	Resistance value R_1	Resistance value R_2
Inserted	Positive	$r_{i_{on}}$	$r_{_{off}}$
	Negative	$r_{d_{on}}$	$r_{_{off}}$
Bypassed	Positive	$r_{_{off}}$	$r_{i_{on}}$
	Negative	$r_{_{off}}$	$r_{d_{on}}$

where R_1 and R_2 are the resistors across the upper and lower switches of the cells, respectively; ($r_{i_{on}}$, $r_{d_{on}}$) pair is the on-state resistance values of the IGBTs and diodes respectively; $r_{_{off}}$ is the off-state resistor value applicable to the open-circuit-branch of the SM.

the diode. The resistor values for the switches are exposed in the Table 4.1.

This model, when compared to the type 2, curtails simulation duration due to the simplification of the resistor values from non-linear functions to two-static values. It should be emphasized that the number of electrical nodes from the type 1 to 3 models is kept unchanged and the representation of the semiconductor switches is being simplified.

4.2.4 Type 4

The type 4 model is based on a simplification of the type 3 model. In this case, the semiconductors are also based on two-state resistor values, but, the SMs models are then replaced by a Thévenin equivalent circuit, as displayed in Figure 4.3 [32, 81, 82, 88, 89].

In order to deduct the Thévenin equivalent circuit of a SM, let's consider that the voltage across the capacitor C is represented by an trapezoidal integration method, such as:

$$U_{c_{jki}}(t) = R_{c_{jki}} I_{cjk}(t) + U_{ceq_{jki}}(t - \Delta t) \tag{4.1}$$

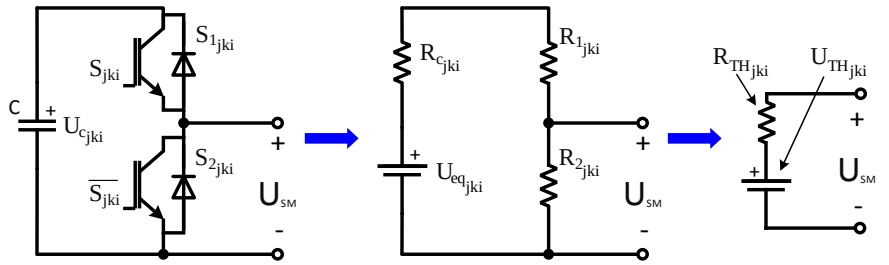


Figure 4.3: Progress of the type 4-based MMC model.

where:

$$R_{c_{jki}} = \frac{\Delta t}{2C}$$
$$U_{ceq_{jki}}(t-\Delta t) = \frac{\Delta t}{2C} I_{c_{jki}}(t-\Delta t) + U_{c_{jki}}(t-\Delta t)$$

Voy Consequently, after replacing the $S_{1_{jki}}$ and $S_{2_{jki}}$ switches with their respective equivalent on-state resistors $R_{1_{jki}}$ and $R_{2_{jki}}$, according to Figure 4.3(b), the Thévenin equivalent circuit of the jki SM is obtained as:

$$R_{TH_{jki}} = R_{2_{jki}} \left(1 - \frac{R_{2_{jki}}}{R_{1_{jki}} + R_{2_{jki}} + R_{c_{jki}}}\right) \tag{4.2}$$

$$U_{TH_{jki}}(t-\Delta t) = \frac{R_{2_{jki}}}{R_{1_{jki}} + R_{2_{jki}} + R_{c_{jki}}} U_{ceq_{jki}}(t-\Delta t) \tag{4.3}$$

where ($U_{TH_{jki}}$, $R_{TH_{jki}}$) pair is the equivalent Thévenin voltage and resistance of the jki SM, respectively (see Figure 4.3(c)).

The output voltage of each SM U_{jki} is then given by (4.4). Since the SMs are connected in series, by adding the series connected ($U_{TH_{jki}}$, $R_{TH_{jki}}$) values, leads to the arm equivalent voltage u_{jk} (4.5) .

$$U_{jki}(t) = U_{TH_{jki}}(t-\Delta t) + i_{jk}(t) R_{TH_{jki}}(t) \tag{4.4}$$

$$u_{jk}(t) = \underbrace{\sum_{i=0}^{N} U_{TH_{jki}}(t-\Delta t)}_{U_{TH_{jk}}(t-\Delta t)} + i_{jk}(t) \underbrace{\sum_{i=0}^{N} R_{TH_{jki}}(t)}_{R_{TH_{jk}}(t)} \tag{4.5}$$

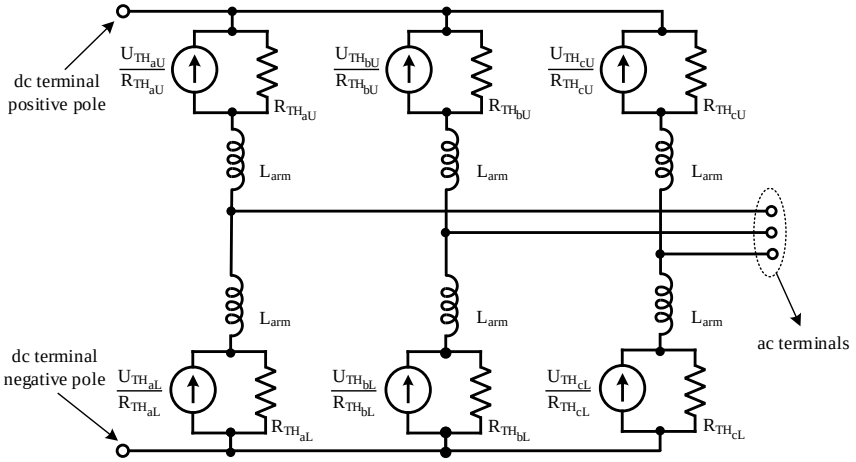


Figure 4.4: Type 4-based MMC model.

where ($U_{TH_{jk}}$, $R_{TH_{jk}}$) pair is the equivalent Thévenin voltage and resistance of the jk arm, respectively.

Finally, if each arm can be represented by a variable resistor $R_{TH_{jk}}$ in series with a voltage source $U_{TH_{jk}}$ (Thévenin equivalent) or in parallel with a current source $I_{TH_{jk}}(U_{TH_{jk}}/R_{TH_{jk}}$ Norton equivalent), the number of electrical nodes of the converter is fixed, not depending on the number of SMs. The type-4 MMC model is presented in Figure 4.4. As the figure emphasizes, the N SMs that composes the converter arm are replaced by an equivalent Norton circuit. Therefore, regardless of the number of SMs that composes each stack, the number of electrical nodes is kept equal to eleven.

The fact of using a converter model with a changeless number of nodes is particularly interesting on the converter models that are characterized by hundreds of SMs. The correspondent time consumption is reduced in comparison to the previously presented models [81, 88, 90, 91].

The type 4 model, besides being used to study the internal behavior of the converter and the interactions with its ac and dc buses, it is also popular to analyze the energy balancing algorithms of the capacitors within the same stack and to validate the average models of the MMC (type 5-based), which are introduced in the next section.

4.2.5 Type 5 and Type 6

The average MMC models are referred to the type-5 and the SMs of the arms are replaced by controlled sources, average functions or mathematical representations of the converter. The fact of removing the dynamics of the switching events (only the average is represented), the time-steps can be increased, which significantly reduces the simulation length, whenever compared to the previous models.

Essentially the converter operation is divided into its ac and dc representation. Regarding the ac representation of the MMC, from the converter control the *emf* of the converter e^*_{abc} (4.6) is settled and, depending on the modulation technique adopted (in (4.7) the nearest level modulation is considered), the voltages across the arms are imposed as (4.8), as illustrated in Figure 4.5(a) [82, 92, 93].

$$m_{abc}(t) = 2\frac{e^*_{abc}(t)}{U_{dc}(t)} \tag{4.6}$$

where m_{abc} represents the modulating indexes for the converter *emf* and U_{dc} is the voltage across the dc link[1].

$$m'_{abc}(t) = \text{round}\left(N m_{abc}(t)\right)\frac{1}{N} \tag{4.7}$$

$$\begin{cases} u_{jU}(t) = \dfrac{U_{dc}(t)}{2}\left(1 - m'_{abc}(t)\right) \\ u_{jL}(t) = \dfrac{U_{dc}(t)}{2}\left(1 + m'_{abc}(t)\right) \end{cases} \tag{4.8}$$

If the Kirchhoff voltage law is applied to the electric circuit of Figure 4.5(a), it is concluded that the interactions between the converter and its ac grid are managed by means of the ac source e_{abc} (4.9) as depicted in Figure 4.5(b).

$$e_{abc}(t) = m'_{abc}(t)\frac{U_{dc}(t)}{2} \tag{4.9}$$

[1]The voltage across the capacitor C_{eq}, which models the total energy storage of the converter in its dc representation.

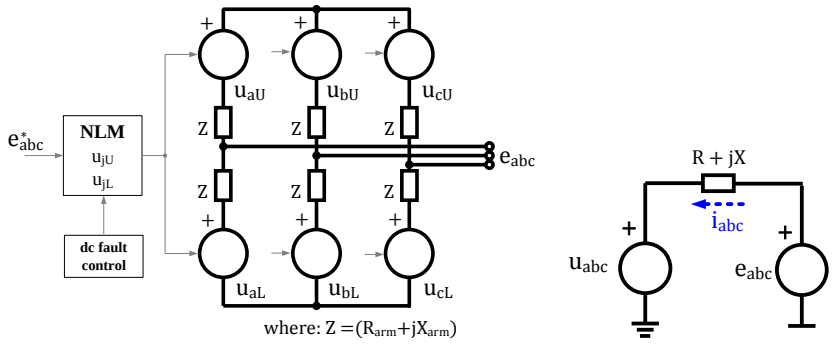


Figure 4.5: ac representation of the MMC type-5-based models.

Hence, by controlling the modulation signals either in magnitude and phase angle, either in balanced or for imbalanced grid conditions, the emf of the converter, the interactions with the ac grid are managed.

Regarding the dc representation of the MMC, it is represented by one capacitor C_{eq} that models the total energy storage of the MMC W_T. The capacitor has the dc-link voltage U_{dc} across its terminals and it models the energy storage of the 6N capacitors C with voltage U_c (4.10).

$$W_T = 6N\left[\frac{1}{2}CU_c^2\right] = \frac{1}{2}C_{eq}U_{dc}^2 \overset{NU_c=U_{dc}}{\Rightarrow} C_{eq} = 6\frac{C_{SM}}{N} \tag{4.10}$$

Similarly to what happens on the two-level-based VSCs, the voltage across the model capacitor C_{eq} is managed in accordance with the the power that flows on its terminals. Hence:

$$P_{ac} = P_{dc} + P_{loss} \tag{4.11}$$

$$\sum_{j=a,b,c} v_j i_j = U_{dc}I_{dc} + P_{loss} \tag{4.12}$$

Replacing (4.9) into the previous equation divided by U_{dc} leads to:

$$\underbrace{\frac{1}{2}\sum_{j=a,b,c} m'_j i_j}_{i_c} = I_{dc} + \underbrace{\frac{P_{loss}}{U_{dc}}}_{i_{loss}} \tag{4.13}$$

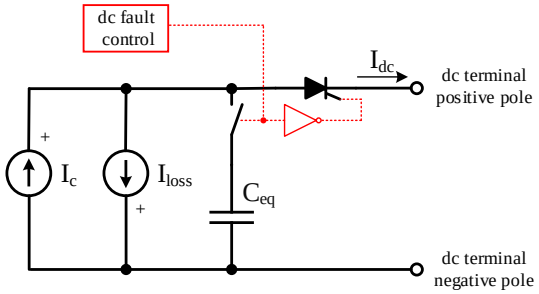


Figure 4.6: dc representation of the type 5-based MMC model.

where i_c models the current that goes into the ac side of the converter and i_{loss} models the current losses of the converter (4.14). The resistor R models the power losses of the converter, which is typically designed so that the MMC model dissipates 1% of the nominal power [32, 93].

$$i_{loss} = \frac{P_{loss}}{V_{dc}} = R\frac{i_c^2}{V_{dc}} \tag{4.14}$$

Finally, the dc representation of the type 5-based model is illustrated in Figure 4.6. During the non-dc-fault conditions, the capacitor C_{eq} is linked to the dc terminals of the converter. Then the current imbalance between $(I_c - I_{loss})$ and I_{dc} consequently charges or discharges the referred capacitor. During the fault conditions, since the gating signals of the IGBTs become blocked and the SM thyristors are ordered to close, the capacitors become bypassed. Then on the type 5 model a switch in series with C_{eq} is added in order to remove this device from the model, whenever a dc fault occurs [32].

The type 5 model is capable of modeling the interactions between the converter and the electrical grid as well as the interactions with the dc grid. However, the inner dynamics of the converter, particularly, its inner currents and its internal energy balancing, is not possible to model. Due to the very simplistic way to model this VSC, the type 5 model greatly reduces the simulation time, when compared to the type 1 to 4 models.

The type 6 models, according to their classification, concern the phasor models of the MMC. Due to their nature, they are commonly used

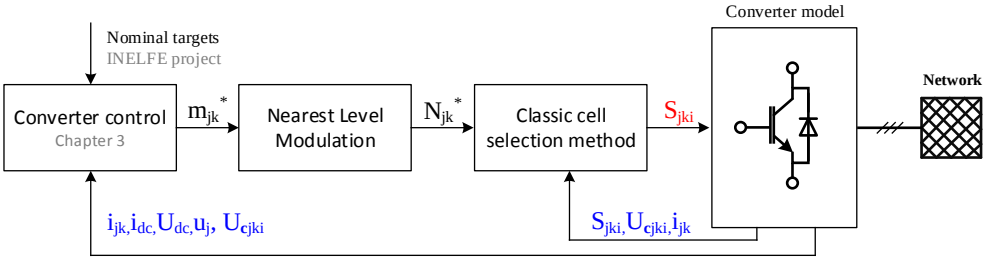
to study medium-term (time frame 400ms to 10s) and long-term (10s to several min) power systems transients [32]. This type of models was not considered in the scope of this thesis.

4.3 MMC modeling techniques analyzed

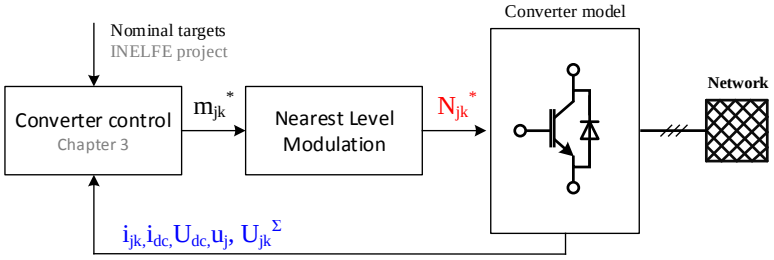
In the present thesis four MMC models characterized by different levels of accuracy were analyzed. The purpose of this analysis was in fact to verify how much time can be saved as the MMC model is being simplified. As mentioned, the type-1 and -2 models are very detailed and suitable for studies which require real-time analysis of the semiconductor behavior, which was not the scope of this thesis. In contrast, the type 5 and 6 models are not capable to describe the inner energy dynamics of the converter, which were not suitable for the thesis scope also. Therefore, the type-3 and -4 based models were the ones considered to be analyzed in this thesis, specifically in Section 4.3.1 and Section 4.3.2 respectively. On the other hand, if certain considerations are made, the DEM model can be further reduced and a new MMC model is deduced. The simplified DEM (SDEM) is discussed in Section 4.3.3. Finally, a new MMC model, named as simplified dynamic model (SDM) is deduced and is presented in Section 4.3.4. Along with the SDEM, and according to the IEEE model's accuracy ranking, the SDM is an average model of the MMC but it permits the modeling of the internal energy balancing dynamics of the converter.

For fair comparison of such methods, the control scheme presented in the previous chapter was adopted, which determines the arm modulation index m_{jk} (3.34) that should be applied to each arm, as a dependence on the operational and targets values of the converter. Afterwards, the nearest level modulation (NLM) [45] was adopted to determine the number of capacitors that should be inserted in the stack jk, respectively modeled as N^*_{jk}, in order to guarantee the modulation index target. Consequently, the so called classic cell selection approach [43], was selected to balance the energy distribution between the capacitors within the same stack as illustrated in Figure 4.7(a). On the other hand,

the SDEM and SDM do not model the individual voltage values of the capacitors, but their voltage sum. Therefore, the procedure to select the cells is no longer required for these models, which has a simpler block diagram like the one described in Figure 4.7(b). Hence, by reason of removing the need to use the ranking-based cell selection methods it boosts simulation performance.



(a)



(b)

Figure 4.7: Block diagram of the Matlab/ Simulink environment for the: (a) TDM and DEM; and (b) SDEM and SDM models.

4.3.1 Traditional detailed model

As introduced in the previous section, the traditional detailed model of the MMC-HVdc is characterized by hundreds of electrical nodes. Then, the mathematical model of the converter will be characterized by large matrices, which require suitably large computational efforts. In addition, as previously explained, each semiconductor is replaced by a resistor, whose value depends on the operation state (open or

closed). However, in the Matlab/ Simulink environment, the semiconductor switches were replaced by ideal resistors with either 0 Ω (if the device is closed) or ∞ (if the device is open).

The performance of the TDM is discussed in Section 4.4.

4.3.2 Data equivalent model

The second model analyzed is designated as the data equivalent model (DEM), and is based on the Thévenin equivalent model of the SMs, hence categorized as a type 4 [81]. As discussed in the previous section, in this model category, the number of electrical nodes does not depend on the number of SMs that are assembled on the converter stacks. Therefore, the converter stacks were replaced by their Thévenin equivalent circuit, which vary as a function on the gating signals of the cells S_{jki}.

In order to achieve the Thévenin equivalent of the converter stacks, as a type 4-based model, it was necessary to define the resistors values that model the semiconductors ($R_{1_{jki}}$ and $R_{2_{jki}}$) in accordance with the SM states S_{jki}. In this model, the on-and and off-state resistors for the IGBTs and diodes were considered equal to 1 mΩ ($r_{i_{on}} = r_{d_{on}} = r_{on}$) or 100 kΩ ($r_{off}$).

The performance of the DEM is discussed in Section 4.4.

4.3.3 Simplified data equivalent model

The simplified data equivalent model (SDEM) is a simplification of the DEM and it is valid if very particular considerations are made. From the converter control perspective, particularly its inner energy management loops, they do not need the individual voltages of the capacitors, but their total voltage sum (each arm). Furthermore, if a cell selection algorithm is adopted that retrieves a high switching frequency of the cells, it imposes an approximately equal voltage distribution between the capacitors (4.15) [43, 94].

$$U_{ceq_{jk1}} \approx U_{ceq_{jk2}} \approx U_{ceq_{jkN}} \approx U_{ceq_{jk}} \Rightarrow U_{ceq_{jk}} = \frac{U_{jk}^{\Sigma}}{N} \tag{4.15}$$

Under these circumstances, it is pointless to save the voltages of 6N capacitors, and progressively sort them at each time frame. Therefore, on the SDEM it is considered that there is a symmetrical energy distribution between the capacitors within the same stack, and so, only the voltage value of one generic capacitor per stack $U_{ceq_{jk}}$ is recorded, whereas the others are considered to be equal. Adding the fact that it was considered that the semiconductor resistors $R_{1_{jki}}$ and $R_{2_{jki}}$, admit either zero (device closed) or ∞ (device open) values, it consequently affects the equivalent Thévenin equivalent circuit of each SM as (4.16) and (4.17).

$$\text{SM inserted} \Rightarrow \begin{cases} R_{TH_{jk}}(t) = R_c \\ U_{TH_{jk}}(t - \Delta t) = U_{ceq_{jk}}(t - \Delta t) \end{cases} \tag{4.16}$$

$$\text{SM bypassed} \Rightarrow \begin{cases} R_{TH_{jk}}(t) = 0 \\ U_{TH_{jk}}(t - \Delta t) = 0 \end{cases} \tag{4.17}$$

where:

$$R_c = \frac{\Delta t}{2C}$$

Consequently, since the bypassed SMs present no voltage drop, the arm voltages only depend on the number of the inserted SMs N_{jk} and their correspondent Thévenin equivalent circuit becomes:

$$U_{jk}(t) = \left(R_c(t) i_{jk}(t) + U_{ceq_{jk}}(t - \Delta t)\right) N_{jk}(t) \tag{4.18}$$

$$= \underbrace{R_c(t) N_{jk}(t)}_{R_{TH_{jk}}} i_{jk}(t) + \underbrace{U_{ceq_{jk}}(t - \Delta t) N_{jk}(t)}_{U_{TH_{jk}}} \tag{4.19}$$

Due to the nature of the converter, N_{jk} SMs will be inserted and charging, whereas the remaining $(N - N_{jk})$ cells will be bypassed and keeping their voltage equal to $U_{ceq_{jk}}(t - \Delta t)$. Then, the voltage sum of

the capacitors $U_{jk}^{\Sigma}(t)$ is given by:

$$U_{jk}^{\Sigma}(t) = \underbrace{\left(R_c i_{jk}(t) + U_{ceq_{jk}}(t-\Delta t)\right) N_{jk}(t)}_{\text{Inserted SMs}} + \\ + \underbrace{U_{ceq_{jk}}(t-\Delta t)(t)\left(N - N_{jk}(t)\right)}_{\text{Bypassed SMs}}$$

$$U_{jk}^{\Sigma}(t) = U_{ceq_{jk}}(t-\Delta t)N + \left(R_c i_{jk}(t)\right) N_{jk}(t) \tag{4.20}$$

Therefore, in order to guarantee a symmetrical energy distribution between the cells of the same stack, the current voltage $U_{ceq_{jk}}(t)$ is accordingly obtained as:

$$U_{ceq_{jk}}(t) = \frac{U_{jk}^{\Sigma}(t)}{N} \\ = U_{ceq_{jk}}(t-\Delta t) + R_{c_{jk}} i_{jk}(t)\frac{N_{jk}(t)}{N} \tag{4.21}$$

Hence, by adopting (4.19), (4.20) and (4.21), a MMC model is obtained that does not provide individual access to the capacitor's voltages due to the fact that they are considered equal.

As mentioned, the SDEM saves computational time when compared to the DEM because it does not required to sort all the cells between time-steps and it only records the voltage value of one generic capacitor $U_{ceq_{jk}}(t-\Delta t)$, in opposition to the N capacitors recorded in DEM $U_{ceq_{jki}}(t-\Delta t)$.

The performance of the SDEM is presented in Section 4.4.

4.3.4 Simplified dynamic model

The simplified dynamics model is an average-based model of the MMC, but it is capable of describing the inner dynamics of the converter. Section 4.2.5) introduced an average model of the MMC, which energy storage is modeled by a single capacitor C_{eq} that is connected to the dc terminals of the converter (see Figure 4.6). Since the total energy storage of the MMC is concentrated in a single capacitor, it does not model the energy storage deviation between the converter legs and arms as well as the inner currents of the converter.

However, if six capacitors were adopted to model the energy storage in each converter arm, it is possible to model the energy storage deviation between them.

Therefore, as presented in (3.5), due to the variation of the number of inserted capacitors over the time to synthesize the required arm voltages, the equivalent arm capacitance is accordingly affected. However, if the number of SMs available on the converter is sufficiently large (4.22), it can be assumed that the arm capacitance can be approximated to (4.23).

$$C\left[\sum_{i=1}^{N} S_{_{jki}}(t)\right]^{-1} \approx \frac{C}{Nm_{jk}(t)} \tag{4.22}$$

$$C_{jk}^{arm}(t) = \frac{C}{Nm_{jk}(t)} \tag{4.23}$$

If (4.23) is verified, an expression is achieved that defines the arm voltage dynamics as a function of the arm modulation index and the correspondent current flow as:

$$\frac{C}{Nm_{jk}(t)}\frac{du_{jk}(t)}{dt} = i_{jk}(t) \tag{4.24}$$

However, if both equation sides are multiplied by the arm modulation index m_{jk}, the dynamics of the voltage sum of the capacitors assembled in the same stack U_{jk}^{Σ} is obtained as:

$$\frac{C}{N}\frac{dU_{jk}^{\Sigma}(t)}{dt} = m_{jk}(t)i_{jk}(t) \tag{4.25}$$

where C/N is a capacitor with voltage U_{jk}^{Σ} that models the energy storage in each stack on the SDM.

If the arm currents i_{jk} are divided as (3.8), the voltage dynamics of the capacitor (C/N) is obtained as:

$$\begin{cases} \dfrac{C}{N}\dfrac{du_{jU}^{\Sigma}(t)}{dt} = m_{jU}(t)\left(i_{diff_{j}(t)} + \dfrac{i_j(t)}{2}\right) \\ \dfrac{C}{N}\dfrac{du_{jL}^{\Sigma}(t)}{dt} = m_{jL}(t)\left(i_{diff_{j}(t)} - \dfrac{i_j(t)}{2}\right) \end{cases} \tag{4.26}$$

Gathering the information of (3.10), (3.11), (3.35) and (4.26) results in the MMC model as displayed in Figure 4.8. Where $U_{j\Sigma}$ and e_j are respectively given by (4.27) and (4.28).

$$\begin{aligned} U_{j\Sigma}(t) &= u_{jU}(t) + u_{jL}(t) \\ &= m_{jU}(t)U_{jU}^{\Sigma}(t) + m_{jL}(t)U_{jL}^{\Sigma}(t) \end{aligned} \tag{4.27}$$

$$\begin{aligned} e_j(t) &= \frac{u_{jL}(t) - u_{jU}(t)}{2} \\ &= \frac{m_{jL}(t)U_{jL}^{\Sigma}(t) - m_{jU}(t)U_{jU}^{\Sigma}(t)}{2} \end{aligned} \tag{4.28}$$

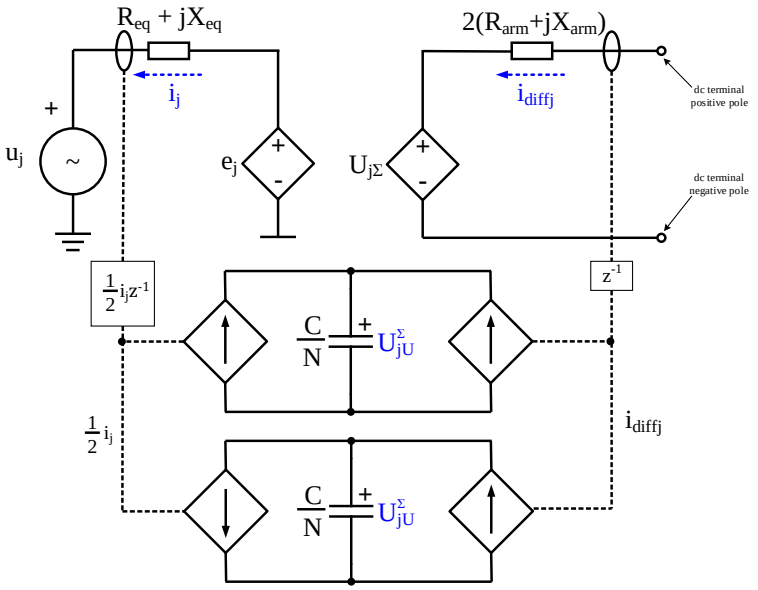


Figure 4.8: Single-line diagram of the SDM configuration.

Depending on the required modulation indexes for each particular stack m_{jk}, the voltage sum of the arms (4.27) and the converter *emf* e_j (4.28) values are imposed. Furthermore, depending on the $i_j(t - \Delta t)$ and $i_{diff_j}(t - \Delta t)$, the voltage across the (C/N) capacitor is managed. If the sampling frequency is sufficiently large, the delay propagated to the voltage U_{jk}^{Σ}, due to the measured values of the currents, become negligible.

Table 4.2: Capacitances considered for the 40- and 400-cell based MMC.

Number of cells N	**Voltage across cell's capacitor** $U_{c_{jki}}$	**Energy storage 35 MJ**
40	17.6 kV	C_{jki}=942 μF
400	1.76 kV	C_{jki}=9.42 mF

The performance of the SDM is presented in the next section.

4.4 Comparison of the MMC models

The MMC models, particularly the TDM, DEM, SDEM and SDM, were examined in the Matlab/ Simulink with the parameters of the INELFE project, which are given in the Appendix A. As emphasized, the control scheme of the previous chapter was duplicated to handle each MMC model. The classic cell selection method was also taken into account in the TDM and DEM models [43].

As previously introduced, the type 3 MMC models are characterized by a large number of electrical nodes, being computationally heavy. Then, to facilitate the analysis of this model, the MMC model analysis was divided in two parts. Initially, the four models referred were composed of a converter-based on 40 cells in each arm (similarly to a cascaded two level converter [49]). In the second stage, due to the large computational effort retrieved by the TDM, the analysis of a 400-cell-based MMC was composed only of the DEM, SDEM and SDM. Either on the 40 or 400 cells-based MMC, the capacitors of both converters were designed to store 35 MJ (see Appendix A), which resulted the values defined in the Table 4.2.

Finally, the four MMC models are compared in terms of their accuracy and time performance in Section 4.4.1 and Section 4.4.2 respectively.

4.4.1 Accuracy

To examine the behavior of such models, they were experimented in different operating conditions, particularly for the steady-state and during the line-to-ground ac fault intervals. Therefore, the accuracy of the MMC models was quantified by determining the normalized mean absolute error (NMAE) factor between the signals retrieved by the DEM, SDEM and SDM in respect to the TDM's signals.

The NMAE is determined in two stages. First, it was computed the mean absolute percentage error (MAE):

$$\mathrm{MAE} = \frac{1}{N_s}\sum_{\kappa=1}^{N_s}|x_{e_\kappa} - x_{r_\kappa}| \tag{4.29}$$

where N_s is the length of the signal x; the pair (x_{e_κ},x_{r_κ}) is the estimated and exact values[2] of the analyzed signal respectively.

Then, the MAE factor was later normalized (NMAE) in respect to the signal x_r. The normalization of MAE was performed according to the variables' nature and it was done either regarding the range or the mean value of x_r on the correspondent interval analyzed. With the variables that exhibits zero crossings, such as the grid currents, it would lead to immeasurable normalizations. Hence, it was defined that on the signals that zero crossings exist, the normalization was accomplished in respect to the mean value of x_r (4.30), or the range of x_r otherwise (4.31).

$$\mathrm{NMAE}(\%) = 100\frac{\mathrm{MAE}}{|\mathrm{mean}\,(x_r)\,|} \tag{4.30}$$

$$\mathrm{NMAE}(\%) = 100\frac{\mathrm{MAE}}{\max\,(|x_r|) - \min\,(|x_r|)} \tag{4.31}$$

Steady-state operation

In this section the accuracy of the DEM, SDEM and SDM models for the nominal conditions of the MMC (see Appendix A) is analyzed

[2]It is reinforced that the signals provided by the TDM were considered as exact values to compute the NMAE of the DEM, SDEM and SDM models.

and quantified. The 40-cell-based converter models were implemented in Matlab/Simulink environment and a stead-state interval where the converter was injecting 1 GW and 300 Mvar values into its ac network was selected. Thus, the results are illustrated in Figure 4.12.

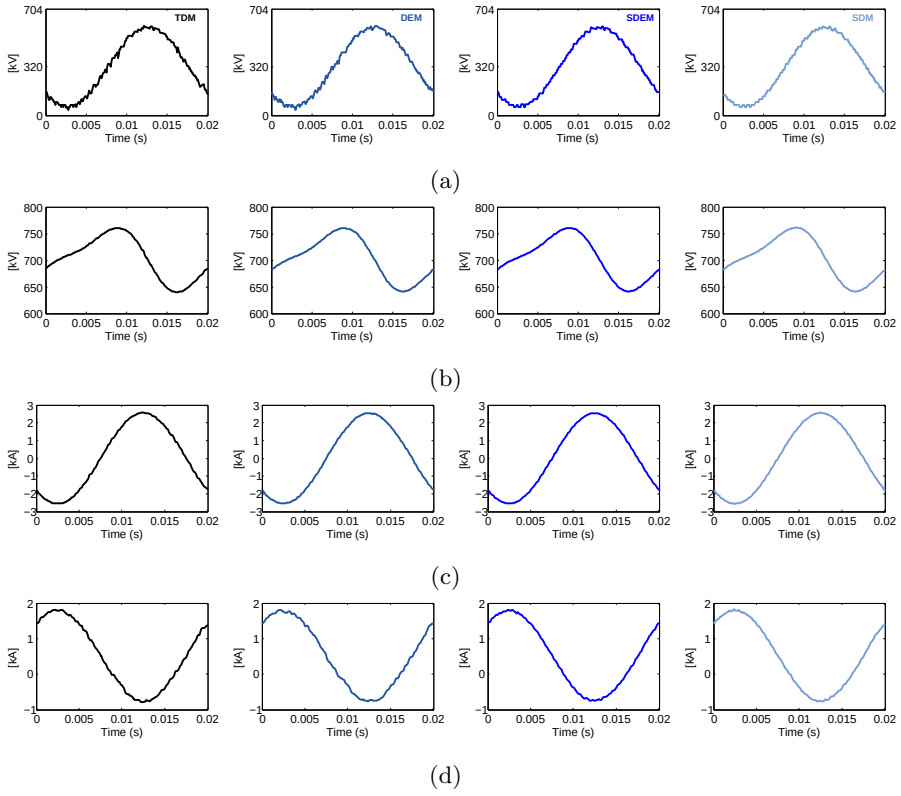


Figure 4.9: Steady-state operation of the MMC's models (N=40): (a) voltage across the arm cL; (b) voltage sum of the capacitors in cL, (c) phase c grid current. (d) cL arm current.

The most evident fact of the figure is that there is a great similarity between the four models. As illustrated, the fact of having large voltage steps on the cell's capacitors, precisely to 17.6 kV, the correspondent arm voltages have spiky waveforms (see Figure 4.9(a)). The voltage sum of the stack capacitors and the ac current signals retrieved by the four models are also identical. Small differences can be spotted in the converter arm currents signals. The similarities between the

Table 4.3: NMAE of the DEM, SDEM and SDM at steady-state operation.

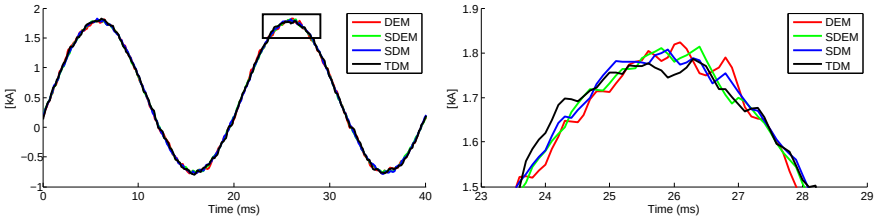
Signal	**MMC models**		
	DEM	SDEM	SDM
u_{cL}	2.49 %	2.15 %	2.33 %
u_{cL}^{Σ}	0.22 %	0.19 %	0.32 %
i_c	0.35 %	0.38 %	0.32 %
i_{cL}	0.97 %	0.91 %	0.88 %

DEM, SDEM and SDM steady-state signals can be corroborated by the NMAE, shown in the Table 4.3.

As a consequence of the large voltage steps and different switching instants retrieved by the MMC models, the voltages generated across the converter stacks are slightly different. This fact contributes to the relatively large NMAE factors > 2.1 % retrieved by the DEM, SDEM and SDM in comparison with the TDM. Another consequence of the large arm voltage steps is the fact of being more complex to control the converter inner currents, and subsequently the arm currents. This issue leads to different arm voltage mutation instants for the referred MMC models and therefore, it is expected that the arm voltages and the currents retrieve slightly more deviations to the TDM than the remaining signals.

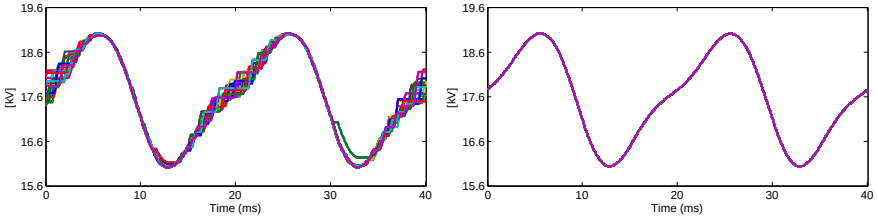
Furthermore, the deviations presented in the previous table suggests that, besides the arm voltages, the arm currents are the signals that most deviate from the TDM. Figure 4.10 clarifies the impact of those NMAE factors on this time-domain signal. The graphic presented in Figure 4.10(b) was amplified approximately ≈ 8 times in order to be identified the deviations between the arm current signals retrieved by the four models. Therefore it is sought to illustrate that the ≈ 0.9 % of NMAE that exists on the arm current signals retrieved by the DEM, SDEM and SDM is reduced.

Additionally, Figure 4.11 presents the divergences between the original and the simplification of the DEM. As already mentioned, the DEM uses a cell selection method that amends the inserted capacitors when-



(a) (b)

Figure 4.10: Ac current in the line c: (a) steady-state and (b) zoomed.



(a) DEM (b) SDEM

Figure 4.11: Individual voltages of the capacitors in the arm aU.

ever the N_{jk} value is changed [43]. This fact can be observable at the integer multiples of 20±2 ms instants. During these intervals, considerable inequalities are visible on the capacitor voltages because the N_{jk} signal is rarely changed in comparison with other intervals (see Figure 4.11(a)). In opposition, in the simplified version of the DEM, it is considered that all the capacitors are perfectly balanced and no energy storage differences occurs between them (see Figure 4.11(b)). Logically, the individual voltage differences between the DEM and SDEM models depends on the cell selection method selected. Instead of being considered the classic sorting method, if the tolerance-band-based cell selection methods were used [95], the individual voltage differences between both models would be much higher. However, at steady-state, the voltage sum of the N capacitors in each arm are approximately the same, because the total energy storage is managed towards the same target.

Consequently, the signals retrieved by the 400-cell-based MMC models are analyzed. However, due to the large computational efforts re-

Table 4.4: NMAE of the DEM, SDEM and SDM at ac fault operation.

Signal	MMC models		
	DEM	SDEM	SDM
u_{cL}	2.85 %	2.34 %	2.33 %
u_{cL}^{Σ}	0.24 %	0.20 %	0.25 %
i_c	0.35 %	0.38 %	0.36 %
i_{cL}	1.00 %	0.93 %	0.91 %

quired to simulate the TDM, it was not considered. The signals retrieved by the DEM, SDEM and SDM models are depicted in Figure 4.12. As the voltage steps are reduced, the high-order harmonic content of the arm voltage waveforms is approximately undetected and, consequently, the signals retrieved by the three MMC models are pragmatically identical. Since the TDM was not implemented for the 400-cell-based condition, the accuracy quantification of these three models is inconceivable. However, due to the closeness characteristics between these three models, a good affinity to the TDM is also expected.

AC line-to-ground fault

The accuracy of the referred models during the line-to-ground ac faults is analyzed in this section. At the beginning of the experiment the 40-cell-based converter was operating at stead-state and injecting 2/3 of its rated power into the ac grid. Suddenly, at t= 0.1 s, the ac line c is short circuited to ground and, later returned to its nominal conditions at t=0.2 s. The relevant waveforms produced by the 40- and 400-cell-based models are illustrated in Figure 4.13 and Figure 4.14 respectively. In terms of the NMAE, it was determined for the interval [0, 0.6] s for the 40-cell MMC models, and it is presented in the Table 4.4.

During the ac fault transient, although the results retrieved by the four models are again very similar and identically describe the same dynamic trends, the NMAE factors are marginally higher. The deviations between the referred models presented in the table also confirm that the models are very adjacent, exhibiting relatively low discrepancies.

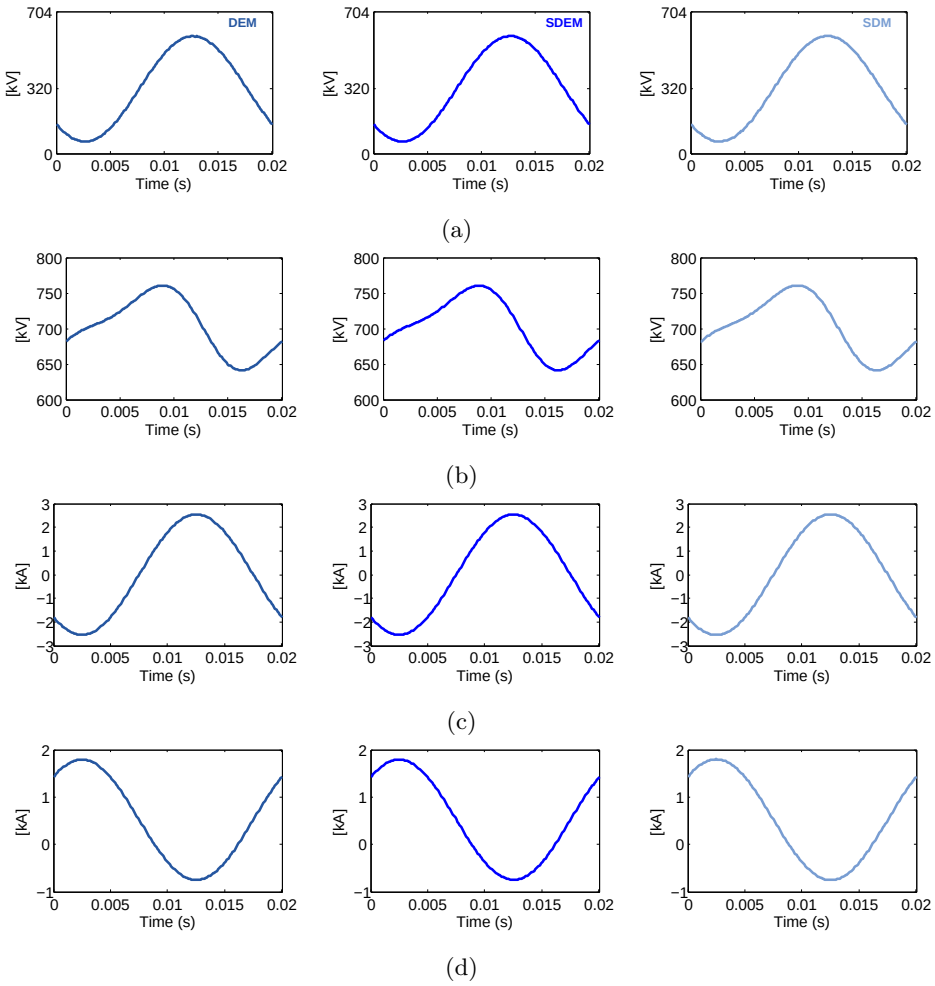


Figure 4.12: Steady-state operation of the MMC's models (N=400): (a) voltage across the arm cL; (b) voltage sum of the capacitors in cL, (c) phase c grid current. (d) cL arm current.

4.4.2 Time performance

A four second simulation was performed for the 40- and 400-cell-based MMC models, with the exception of the TDM for 400 cells. Both simulations were done in the Matlab/ Simulink numerical tool and resolved with the *ODE45* solver with a maximum time-step of 100 μs. The simulations were conducted on a 3.4 GHz i7-4770 Intel core CPU with 16 GB of RAM. The simulation lengths for each particular model

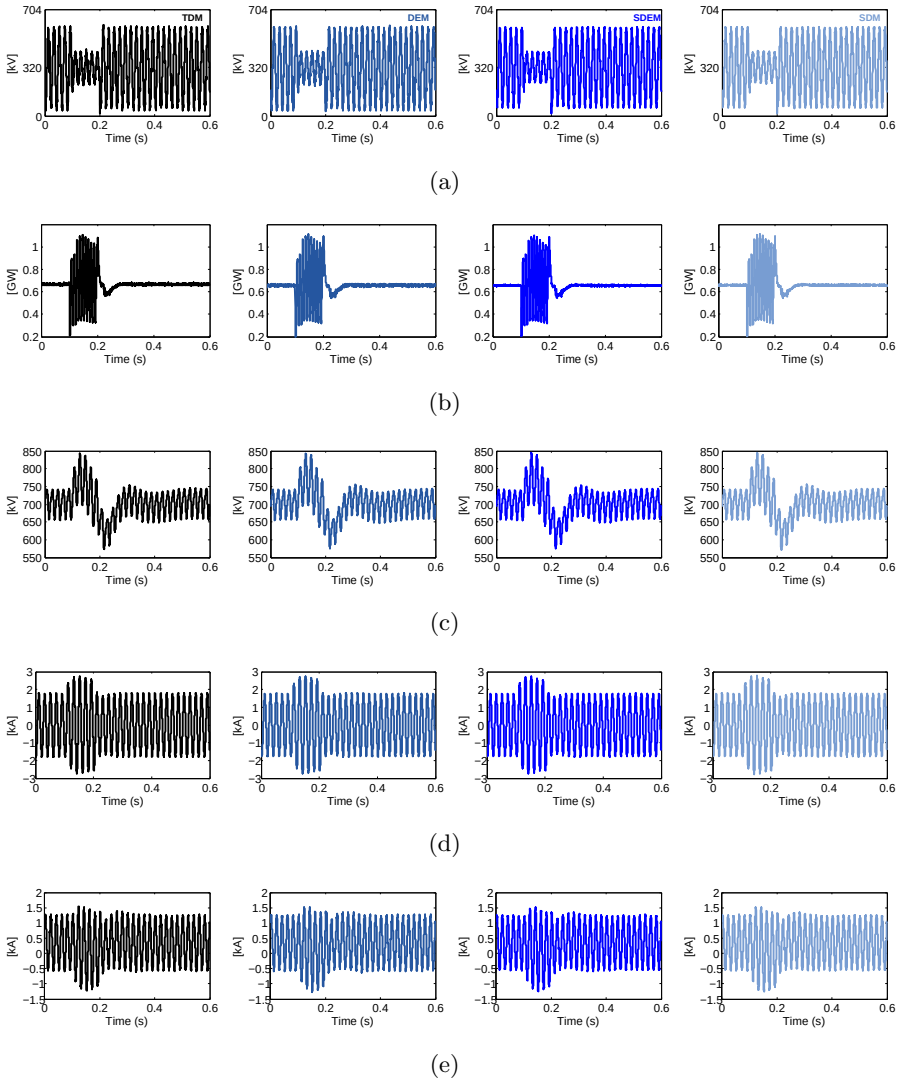


Figure 4.13: Line-to-ground fault on the phase c applied at [0.1,0.2] s (N=40): (a) voltage across the arm cL; (b) power injection into the ac grid; (c) voltage sum of the capacitors in cL; (d) grid current on the line c; (e) cL arm current.

are presented in the Table 4.5 and related in Figure 4.15.

The TDM is by far the modeling technique that requires more time

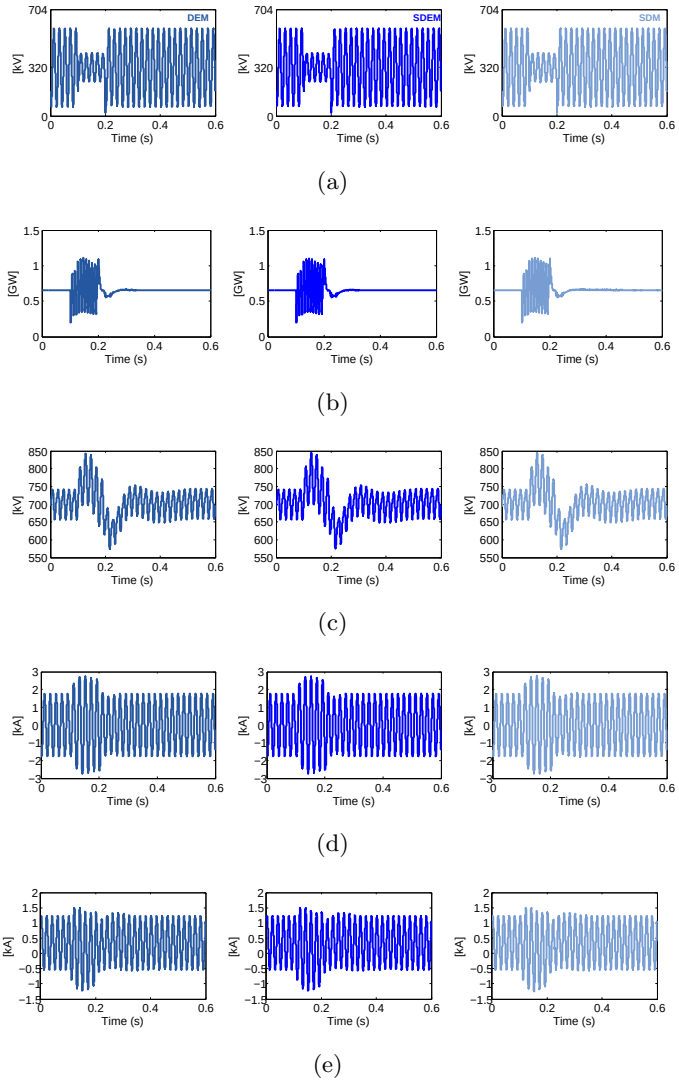


Figure 4.14: Line-to-ground fault on the phase c applied at [0.1,0.2] s (N=400): (a) voltage across the arm cL; (b) power injection into the ac grid; (c) voltage sum of the capacitors in cL; (d) grid current on the line c; (e) cL arm current.

to simulate the behavior of the MMC, even in the reduced 40-cell-based structure. As the number of cells increases, the simulation lengths prop-

agated in the TDM trends to evolve extremely fast [90] being impracticable to study the behavior of the 400-cell-based MMC with the TDM in an ordinary computer. Hence, the use of simplified versions of this model is motivated. The DEM is capable of ideally reducing the simulation length of the MMC by at least one decade. It required 24 seconds to simulate a 40-cell-based converter, which is a reasonable value considering the complexity of the MMC. However, depending on the focus of the converter studies, the MMC models can be further simplified to the SDEM or SDM modeling techniques. These two models do not grant access to the individual voltages of the capacitors, which are not suitable for studies that require their use, such as for analyzing in real-time the switching losses of the converter. The SDEM and SDM retrieve close results and both can further reduce the simulation lengths propagated by the DEM, regardless of the number of cells that are employed on the converter.

The number of SMs available in the converter model demonstrate having a relatively high impact on the DEM. Although the number of electrical nodes is the same, the fact of considering more SMs in the simulation means the simulation length is increased due to the sorting state of the cell's selective control procedure. The SDEM and SDM perform similarly and they are undoubtedly capable of reducing the computational efforts retrieved by the TDM and DEM models.

As the number of cells available on the converter increases in accordance with the results, it seems that the SDM is the modeling technique that most reduces the simulation length of the MMC (up to 89 % for N=400 when compared to DEM).

4.5 Conclusions

In this chapter different modeling techniques for the modular multilevel converter were analyzed. Due to the converter complexity, a standardization of the MMC models is available in the literature, which consists of six types of converter models. Therefore, from the type one (most accurate) to the six (least accurate) several models are available in

Table 4.5: Simulation lengths of the MMC modeling techniques.

Parameters	MMC models (N=40)			
	TDM	DEM	SDEM	SDM
Time (s)	2670	24	12	13
Reduction ratio to TDM (%)	-	99.1	99.6	99.5
Parameters	**MMC models (N=400)**			
	TDM	DEM	SDEM	SDM
Time (s)	-	123	16	14
Reduction ratio to DEM (%)	-	-	87.0	88.6

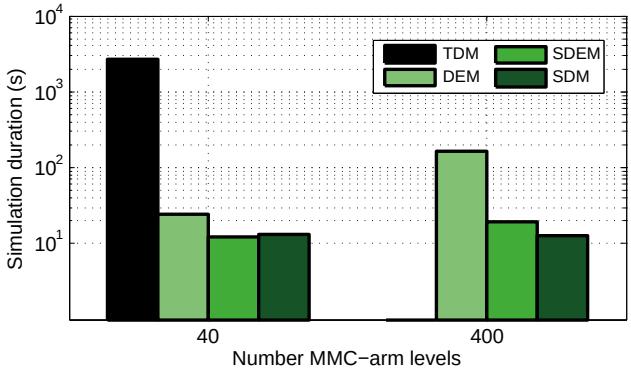


Figure 4.15: Simulation lengths retrieved by the converter models analyzed.

the literature. This chapter describes two literature-based models: the traditional detailed model (TDM) and the detailed equivalent model (DEM), respectively categorized as type three and type four. Additionally, two distinct MMC models are proposed: the simplified data equivalent model (SDEM) and the simplified dynamic model (SDM).

Finally, the accuracy of the DEM, SDEM and SDM models was analyzed in comparison with the 40-cell based MMC's TDM. The results accomplished by the DEM, SDEM and SDM show diminished deviations to the TDM either for the steady-state and for the ac line-to-ground fault intervals. The arm voltages and currents were the signals analyzed that retrieved larger deviations between models. This is sup-

ported with the fact that the large voltage steps on the converter arms contribute to different mutations of the arm voltages on each particular model. However, the success of the DEM, SDEM and SDM models are expected to increase with the number of cells available on the converter stacks.

On the other hand, the four MMC models were analyzed regarding their intrinsic computational efforts. As the models are becoming more simpler, the simulation lengths are being curtailed without severely compromising their overall accuracy.

Particularly in the SDEM and SDM models proposed, they are capable of reducing up to 89 % of the simulation time lengths required in the Thévenin-based model. The time improvement comes with the cost that the SDEM and SDM models can not individually describe the voltages of the submodules capacitors. Therefore, they are slightly restrictive in the converter studies.

Chapter 5

Modulation techniques for Medium Voltage MMC

5.1 Introduction

The modular multilevel converter (MMC) is a reasonably young inverter technology with a promising future in medium voltage DC (MVdc) systems, such as large wind turbines in the DC collection grids, large PV integration, large marine current and wave energy integration [96–99]. The modularity, the redundancy and the high quality voltage waveforms makes the MMC a viable solution for dc transmission applications [94,100–102]. However, the management of the arm voltage waveforms and accordingly at the converter output, evokes several concerns on its performance.

Over time, several modulation techniques have been proposed to compile the required ac voltage at the output of the multilevel-based voltage source converters [45,102–108]. Most of the proposals were carrier-based PWM (CB-PWM) and depending on the carrier's nature, different pulse patterns are applied to the converter's switches. Hence, different output voltage profiles can be conceived at the VSC's, influencing then their performance.

This chapter presents a review of the CB-PWM techniques proposed for the previous multilevel VSC generations. Then, the relating strategies were considered to shape the voltage generated on the MMC's arms in combination with an additional capacitor's energy balancing algorithm. Additionally, the performance of the presented modulation

strategies was complemented with the impact analysis of the zero sequence signals (ZSS) injection into the MMC arms modulation. A medium voltage-based MMC model with 15 MW/ 28 submodules is embraced to analyze the impact of several arm voltage modulation strategies on the converter performance, namely, on its efficiency, capacitors ripple and the quality of its waveforms.

This chapter is organized as follows: Section 5.2 presents and discusses several modulation strategies and zero sequence signals proposed in the literature that can be used to improve the operation of the inverters. The methodology followed to assess the performance of the MMC is discussed in Section 5.3. The impact of the modulation strategies on the converter performance is then argued in Section 5.4. The final remarks are presented in Section 5.5.

5.2 Multilevel modulation techniques

Several modulation strategies have been introduced to drive multilevel converters, namely for the Neutral Point Clamped (NPC) [109], Flying Capacitor (FC) [110] and Cascaded H-Bridge (CHB) [111–115] and more recently the modular multilevel converter [42, 43].

The first three VSC structures require proper PWM-controlled strategies in order to balance the energy storage of their dc-bus capacitors, without the use of additional hardware [116, 117]. Once the control scheme of these converters determines the require voltage target for their output u_j^*, it is normalized in accordance with the maximum voltage amplitude synthesizable at the VSC's output, particularly, the dc-bus voltage U_{dc} as:

$$m_j = u_j^*/U_{dc} \tag{5.1}$$

The correspondent modulation index m_j^* of a M-level converter is then compared with (M-1) carriers, resulting then in 2(M-1) logical signals to drive the correspondent switches of each converter leg. The intrinsic features of each CB-PWM techniques and their redundant voltage vectors are responsible for balancing the dc capacitors voltages [114].

In terms of the MMC, the energy is no longer stored on its dc side bus but instead in the capacitors placed inside the submodules. Due to the converter nature, the grid currents flow directly on the SM's capacitors and this situation establishes a great voltage ripple variation. As a result, the energy stored in the capacitors tends to diverge over the time, which forces the need to balance the voltage along all the capacitors of the converter for proper operation [53, 118]. This goal is addressed by selecting the proper redundant voltage vectors on the MMC arms, but this stage is done by means of a selective control of the cells.

So, if in the NPC, FC and CHB solutions, the CB-PWM techniques were used to shape their output voltages and to balance the energy storage of their capacitors regarding the MMC, in this study, this is done in two stages. First, the CB-PWM schemes are considered to modulate the arm voltages. In the second stage, the cell selection methods are required to ensure controlled energy distribution between the capacitors within the same stack [53, 119]. The flexibility allowed by sorting and selecting the MMC capacitor's to be inserted, besides the knowledge of their individual voltages, also permits a decision on which capacitors are inserted in the chain depending on the SM's semiconductors temperatures [120].

The classification of the modulation strategies treated in this work are depicted in Figure 5.1. The modulation methods are then classified as carrier-based PWM (CB-PWM), nearest level modulation (NLM) and selective harmonic elimination (SHE) methods and they are presented in the sections 5.2.1, 5.2.2 and 5.2.3 respectively. Moreover, the presence of zero sequence signals injection into the converter modulation are also discussed in 5.2.4.

5.2.1 Carrier-based PWM

In a carrier-based PWM applied to a M level inverter, (M-1) carriers are used with particular technicalities as their frequency, amplitude, phase and dc offset. Combining different specifications on those signals entails different modulation strategies, which denote a different behavior of the converter. On the first modulation stage, (M-1) carriers are

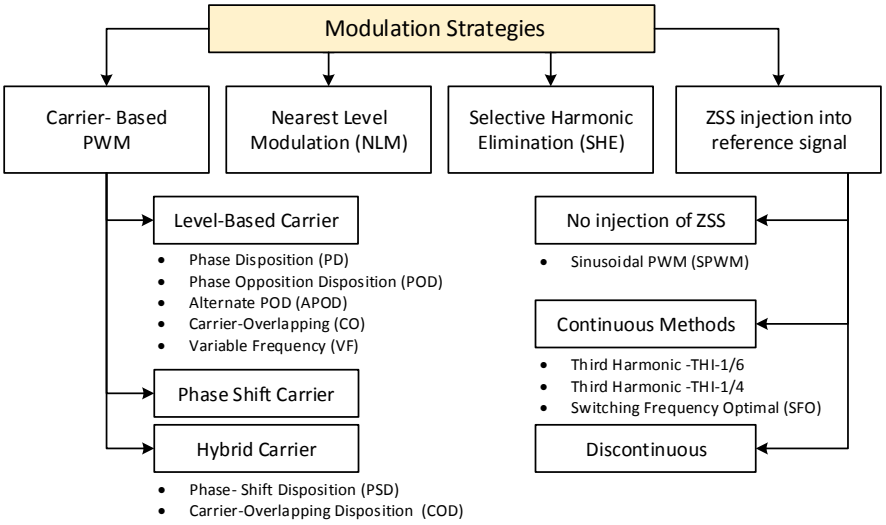


Figure 5.1: Classification of the modulation strategies.

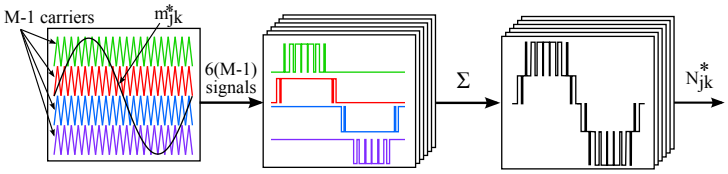


Figure 5.2: CB-PWM techniques applied in MMC applications.

compared to the MMC arms modulation indexes m_{jk} (3.34), resulting 6(M-1) modulation patterns. To be compatible with the 'sort and select' algorithm, the six groups of (M-1) firing pulses are added and the target number of inserted capacitors N^*_{jk} (one per arm) is created, as Figure 5.2 illustrates [69].

In this work, the CB-PWM techniques are classified into: level-shifted PWM (LS-PWM), phase shift-carriers PWM-based (PSC-PWM) and hybrid PWM (H-PWM). The LS-PWM is characterized by placing (M-1) carriers in adjacent vertical bands. The PSC-PWM is characterized by having (M-1) carriers with the same amplitude and frequency however, shifted in phase angles. Lastly, the hybrid PWM (H-PWM) merges some characteristics of the LS-PWM and PSC-PWM strategies. The

individual details are presented in the next sections.

Level-Shifted PWM

The LS-PWM strategies were mainly proposed to be applied on the multilevel NPC and FC converters [121, 122]. The LS-PWM are not a suitable option for CHB converters since they produce an unequal power distribution among the H-Bridge-cells which pollutes the harmonic spectrum of the grid current[1] [122]. The individual LS-PWM techniques are briefly described in the following sections.

Phase Disposition (PD), Alternate Phase Opposition Disposition (APOD) and Phase Opposition Disposition (POD): the carriers have the same amplitude and frequency, but placed in different levels (offsets) [108]. The carriers on the PD method have the same phase angle, as presented in Figure 5.3(a). In POD, the carriers above the zero line voltage reference are in phase opposition to those below, as shown in Figure 5.3(b). In the APOD method, all the carriers are alternatively in phase opposition, as presented in Figure 5.3(c).

The analytical and experimental comparison of the voltage harmonic spectrum generated by a three-phase/ five-level NPC (5L-NPC) inverter driven by APOD, POD and PD modulation methods was performed in [108, 123]. It was demonstrated that the PD has superior harmonic performance, as long as the carrier frequency is an odd triple multiple of the fundamental frequency, due to the fact that it concentrates significant harmonic energy at the carrier's frequency and it is canceled on the VSC's line to line voltage. Furthermore, if a third harmonic is injected into the output voltage modulation, the PD continues to retrieve better results than the APOD and POD methods in the same conditions [124, 125].

The APOD, POD and PD strategies were also applied to a five-arm-level MMC without any energy balance strategy [126]. In those conditions, a substantial amount of harmonics on the arm voltages and

[1] This fact is also extended to the MMC, by the reason of the MMC also being a cascaded-connected-based cell converter.

currents was generated due to the fact of the non-controlled and unequal voltage across the capacitors. These CB-PWM techniques, under the refereed conditions, are not suitable for MMC applications [126]. An intermediate mapping between the PD modulation and the firing pulses of the MMC's switches was investigated in [127].

Carrier Overlapping (CO): the carriers share the same frequency and phase, despite the amplitude and offset are designed to overlap the adjacent bands as shown in Figure 5.3(d) [106]. The overlapping distance between the adjacent carriers is half the value of their amplitude.

This method was compared to the phase disposition methods for a 3-level NPC (3L-NPC) converter [106, 128]. For modulation indexes lower than 0.7, the CO retrieves far less harmonic distortion on the line voltages than the PD methods because the reference intercepts more times the carriers due to the overlapping. On high modulation indexes (m_j >0.8), the harmonics distortion of such methods are similar.

The authors did not find any publications of this strategy applied on the MMC.

Variable Frequency (VF): it is an evolution of the PD method and it was created to equalize the power loss distribution along the NPC levels [104, 106]. Whenever the NPC phases are modulated by the phase disposition method, the switches placed on the top/bottom layers commute more often than the ones placed on the intermediate levels. To adjust the transition asymmetry, a carrier with higher frequency was implanted on the intermediate levels as Figure 5.3(e) illustrates.

In opposition, in terms of the MMC, as the arm current reaches its peak values the voltage of the capacitors trend to drift, which motivates the need for rotating the inserted capacitors more often. Hence, higher frequencies on the top levels were considered to change more often the active SM reference N_{jk}^{*} as shown in Figure 5.3(f) [129]. The reference [129] studied the variable-frequency strategy to be applied on the MMC, but with a crescent carrier frequency as the level increases. However, in the case of having unequal and unrelated carrier frequencies in each

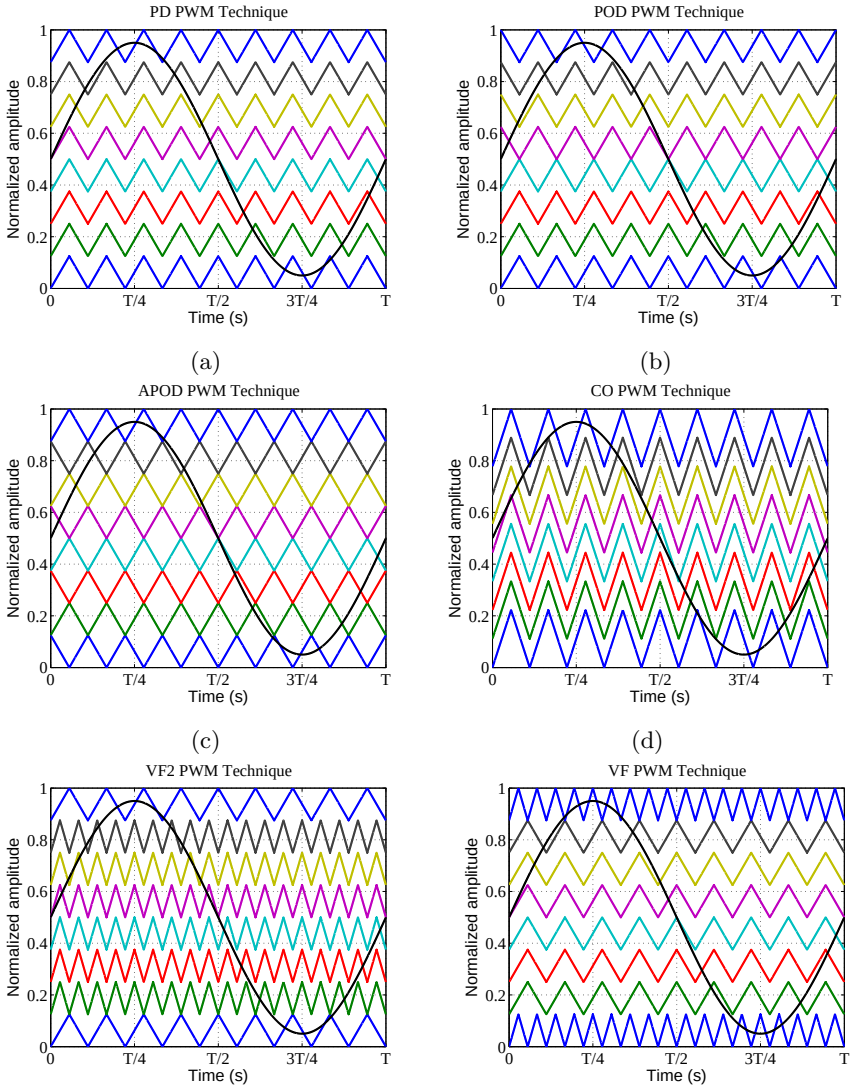


Figure 5.3: Level-Shifted PWM strategies:(a) Phase Disposition, (b) Phase Opposition Disposition, (c) Alternate Phase Opposition Disposition, (d) Carrier Overlapping and (e) Variable Frequency - original and (f) Variable Frequency - MMC-based approach.

particular level, the harmonic spectrum is increased on the converter's line voltages. Hence, to avoid this issue, only two frequencies were considered, specifically for the intermediate and top layers.

Phase-Shift Carrier PWM

The phase shifting technique was the first multi-carrier-based PWM strategy presented in the literature. It was used to interleave n two-level converters that were connected in parallel [103]. All the carriers have the same amplitude, frequency and offset, but phase-shifted by $(2\pi/n)$ as shown in Figure 5.4. This method reduced the voltage ripple on the dc-link capacitors and eliminated certain groups of grid current harmonics [103].

The PSC overcame the asymmetric power distribution among the floating capacitors on the CHB and FC converters [121, 122, 130]. A M-level inverter driven by the PSC-PWM with carrier frequency f_c, significant harmonic content will be seen in the converter line-neutral voltages around $(M-1)f_c$ [125, 130]. Adjusting the frequency of the carriers in the PSC-PWM method, the correspondent voltage harmonic spectrum becomes equal to the APOD method [94, 123, 131].

This modulation mechanism can be used in MMC applications, however with limited bounds because it is not sensitive to the capacitor voltages drifts [95]. The reference [69, 132, 133] adapts the PSC-PWM to operate associated with an additional ranking and selection of cells approach.

Hybrid Carrier PWM

The denomination of hybrid-carrier is due to the fact that uses multiple CB-PWM techniques. According their features, can only be applied to converters with odd number of levels.

Phase-Shift Disposition (PSD): it is a combination of the PSC and PD modulation methods [105, 107, 125]. It is used to drive a M-level inverter and it consists of placing two groups of (M-1)/2 carriers waves

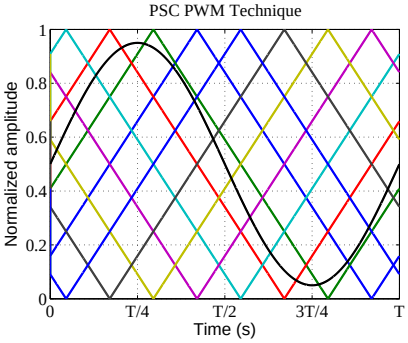


Figure 5.4: Phase-shift carrier PWM strategy.

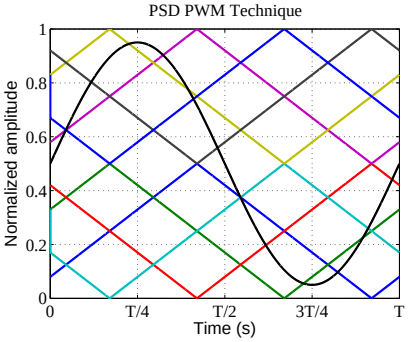


Figure 5.5: Phase-shift disposition carrier PWM strategy.

with the PSC disposition in two adjacent bands in anti-phase as illustrated in Figure 5.5. This modulation method is characterized by placing significant harmonic content on the phase voltage around $f_c(M-1)/2$ [125]. Which can be adjusted, as well as the PSC, to retrieve similar results as the APOD method [123].

The efficiency of the PSD was analyzed for a 5L-NPC and compared to the previously presented CB-PWM techniques in [107]. The study reveals that, whenever the converter is operating with higher modulation indexes than 0.7, the PSD retrieves fewer switching losses than PD, POD, APOD, CO, PSC and COD, as long as the same carrier frequency is considered on all the correspondent methods [107].

The authors did not find any publications of this PWM strategy applied to the MMC.

Carrier Overlapping Disposition (COD): it is a combination of the the CO strategy with the LS-PWM strategies. In a M-level inverter, two groups of (M-1)/2 overlapped carriers are placed in two contiguous bands as Figure 5.6 shows. The combination of different phase angles for the adjacent carriers formulates different modulations schemes, as the CO-PD, CO-POD and CO-APOD which are formerly introduced in the next sections [134].

The authors did not find any publications of this COD modulation strategy applied to the MMC.

Carrier Overlapping- Phase Disposition (CO-PD): In this strategy the (M-1) carriers share the same phase as Figure 5.6(a) shows. This modulation technique was compared to PD, APOD, POD, PSC, CO and PSD for a 5L-NPC over the linear and over-modulation ranges [107]. The CO-PD retrieves similar results as the CO, being slightly more efficient for particular low modulation indexes.

Carrier Overlapping- Phase Opposition Disposition (CO-POD): this strategy imposes that the carriers placed on the upper and lower bands have their phase angle rotated by 180 degrees as shown in Figure 5.6(b).

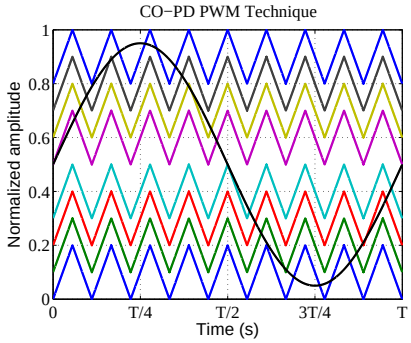
Carrier Overlap.- Alternate Phase Opposition Disposition (CO-APOD): this method settles that two consecutive carriers are placed in antiphase as Figure 5.6(c) clarifies. The CO-APOD was proposed to be applied in a 5L-NPC, labeled as SPD in [105].

5.2.2 Nearest level modulation (NLM)

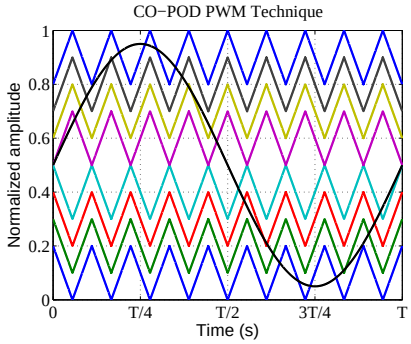
The NLM is a non-carrier method and suitable for MMC-HVdc-based applications [49]. In contrast to the CB-PWM methods, where the individual pulse patterns are added to create the N^*_{jk} target, on the NLM this set-point is obtained directly from the arm modulation index m^*_{jk} as:

$$N^*_{jk} = \text{round}\left(N m^*_{jk}\right) \tag{5.2}$$

where N is the number of SMs available on the MMC stacks.



(a)



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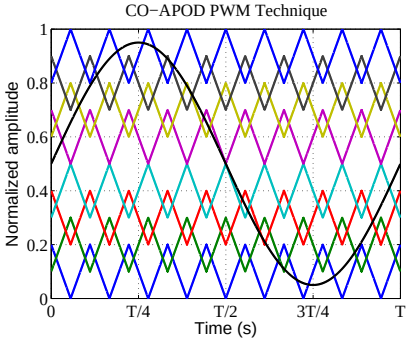


(c)

Figure 5.6: Carrier overlapping disposition strategies: (a) carrier overlapping with Phase disposition, (b) carrier overlapping with phase opposition disposition and (c) carrier overlapping with alternate phase opposition disposition.

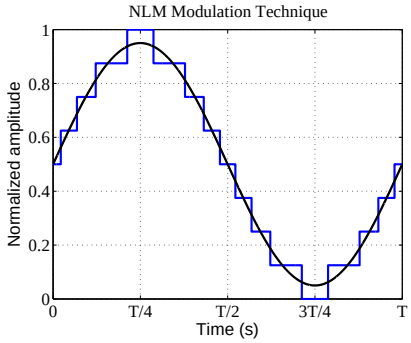


Figure 5.7: Nearest Level Modulation.

In this strategy, the modulator (Nm^*_{jk}) is discretized by rounding it to the closest integer number of SMs attainable, as shown in Figure 5.7. The greater number of levels is, the more accurate the output waveform becomes.

The NLM was proposed to drive a 4 asymmetric-CHB cells (81 level converter) in conjunction to the DTC scheme applied to an induction machine [45]. When compared to a PWM-based modulation, as the number of voltage levels is higher, the NLM shows a clear reduction of the number of switching events [45, 121].

The NLM was first applied in MMC applications in 2010 [135], and since then, has been widely used to drive this converter structure in HVdc applications [49, 95, 101, 136].

5.2.3 Selective harmonic elimination (SHE)

The SHE is also called programmed harmonic elimination method. This modulation method consists of an optimization technique that, in accordance with the desired objective function, provides the firing pulses that should be applied on the semiconductors [23, 137, 138]. It can be applied either in real-time or in an offline mode, and is commonly adopted on power converters to minimize the switching losses, torque pulsations and elimination of particular low-order harmonics [139, 140].

On multilevel converters composed of an high number of voltage steps,

they can synthesize low-harmonic content-based voltage waveforms and, therefore, this modulation strategy becomes unsuitable [95, 101, 119]. The author could not find the SHE for MMC applications with more than 20 levels. Therefore, due to the relatively high number of levels of the MMC-based case study, this method was not considered in this study.

5.2.4 Zero sequence signals (ZSS)

Zero sequence signals (ZSS) are triple order harmonics that can be added to the modulation signals of the three-phase-based power converters. Injecting an odd-multiple of the third harmonic signals (H_3,H_9, H_{15},...) into the modulation of the three-phase system, these harmonics will be canceled on the line-to-line output voltages. The ZSS are used to address some goals such as harmonic spectrum reduction of the ac grid currents, increase the converter efficiency and to increase the linear range of the converter's modulation indexes [94, 128, 141–148].

If no ZSS is considered, it is designated in this work as sinusoidal PWM (SPWM). Otherwise, depending if they are derivable in the time domain, as illustrated in Figure 5.1, the ZSS signals are classified in this work as continuous or discontinuous.

Third Harmonic (THI)

The third harmonic-based ZSS (THI-ZSS) is a continuous common mode signal that is injected into the voltage modulation of the VSCs, mainly used to maximize the usage of its dc-bus. The THI-ZSS and is illustrated in Figure 5.8(a). On two level inverters the amplitude of the THI-ZSS influences the performance of the converters differently. If a third harmonic ZSS with (1/6) of the converter's *emf* magnitude is considered, the linear range of the VSC is extended by ≈15.5 % in comparison with the SPWM, which is the maximum achievable on the VSCs [141, 143]. Therefore is the typically the ZSS solution adopted [49, 94, 141, 143]. On the other hand, the injection of a third harmonic common mode signal with (1/4) of the converter's output voltage target

into its modulation, it minimizes the harmonic spectrum on the output voltages [141].

Switching frequency optimal (SFO)

This technique is also called naturally sampled space vector modulation (SVM) [104, 128, 149]. This ZSS technique is commonly used in ac drives applications [142] and it is illustrated in Figure 5.8(b). The ZSS-SFO curve is identical with a triangular curve, but in reality it is achieved by means of trigonometric functions (5.3).

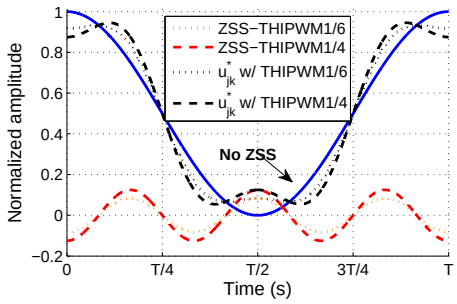
$$\lim_{x \to 0} \frac{sin(x)}{x} = 1 \tag{5.3}$$

The amplitude of the triangular waveform is equal to (1/4) of the output voltage magnitude desired for the converter and, conjointly with the THI (1/6), the linear range of the VSC's voltage modulation is extended by 15 % in comparison with the SPWM [150, 151].

Several combinations between the CB-PWM techniques with the SFO-ZSS were studied [106, 128, 152]. Particulatly on a GTO-tyristor inverter, the aggregation of the APOD, PD and CO methods with the SFO-ZSS reduces the distortion factor of the grid currents, when compared to the CB-PWM techniques on their own [152]. Moreover, the SFO can slightly reduce the THD in the line-neutral voltages for particular modulation indexes when combined with PD or CO [106, 128].

Discontinuous ZSS (D-ZSS)

On the discontinuous ZSS-based modulations an offset is added to the modulation index target in such a way that voltage generated at the VSC's output it is clamped to a voltage level. In the literature it is shown that its possible to clamp the converter voltages over 30, 60, and 120 degrees intervals [142, 143, 153], and during those intervals the switching events are avoided [154]. Figure 5.8(c) shows an equivalent VSC's voltage reference when it is clamped on its top over 60 degrees. This particular case is commonly referred in the literature as the flat top D-ZSS. In this work, the MMC arm voltages were clamped over



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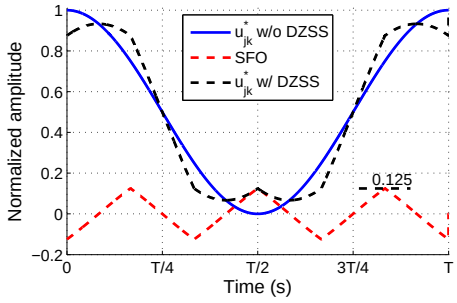

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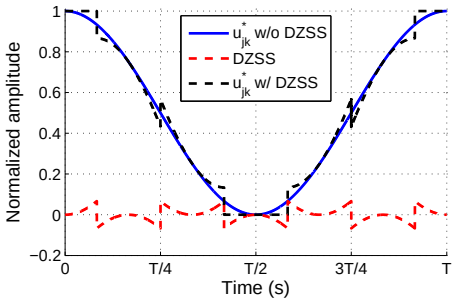


(c)

Figure 5.8: The ZSS injected on the MMC's arm voltage modulation: (a) a third harmonic, (b) switching frequency optimal (SFO) and a discontinuous-ZSS.

the 60 degrees intervals, particularly when the arm currents reach their positive and negative uppermost values.

The impact of the combination between the modulation techniques and the ZSS presented on the modular multilevel converter performance was also analyzed and presented in Section 5.4.

5.3 Methodology followed to assess the converter performance

The impact of the presented modulation techniques and the corresponding aggregation with the ZSS, were analyzed in terms of the semiconductor's power losses, harmonic distortion factors of the grid currents and arm voltages, and finally, the voltage ripple of the SM capacitors. This study was based on the point-to-point dc transmission scheme of Figure 5.9. The converter 1 and 2 are characterized by the parameters shown in the Table 5.1. The MMC1 was controlled to inject 15 MW into the dc bus, whereas the MMC2 was designed to maintain the dc pole-to-pole voltage at its nominal conditions. The modulation strategies presented have been implemented on the MMC2, whose performance is being studied in this chapter.

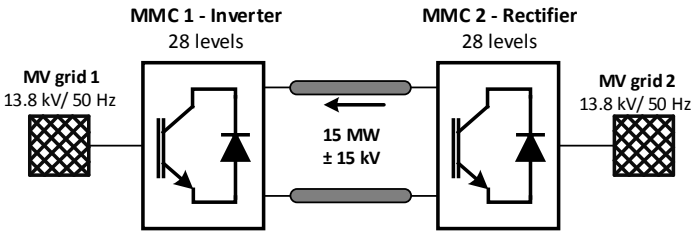


Figure 5.9: MMC-MVdc transmission system analyzed.

The methodology used to model the MMC2 and to describe its semiconductors power losses is presented in Section 5.3.1. The procedure to used to rotate the inserted capacitors is explained in Section 5.3.2. The semiconductor's power losses and the harmonic content retrieved by the CB-PWM techniques greatly depend on the frequency that is adopted

for the correspondent carriers. Therefore Section 5.3.3 presents the reasoning adopted in the carrier's frequency design.

Table 5.1: Circuit Parameters used for simulation

Parameters	Notation	Value
Number of submodules/arm	N	28
Rated active power	P	15 MW
Power factor	cosϕ	1
Line voltage	U_{LL}	13.8 kV
Grid frequency	f_{grid}	50 Hz
dc-bus voltage	U_{dc}	$\pm$ 15 kV
Cell capacitance (35 kJ/MW)	C	4.5 mF
Nominal submodule voltage	$\bar{U}_{c_{jki}}$	1200 V
Arm inductance	L_{arm}	20 mH
Grid Inductance	L_{grid}	5 mH
Parasitic resistance of the inductors	R	0.1 Ω

5.3.1 Converter modeling and semiconductor losses estimation

Several MMC models with different levels of detail have been presented in the previous chapter. In order to study the modular multilevel converter efficiency, the DEM was implemented but characterized by ideal switches (zero or ∞ Ω). Then, the semiconductor's power losses were estimated according to methodology presented in [155]. As the author described, to estimate the power losses generated by the switches, besides the knowledge of its features (voltage drop and energy loss vs. driven current), the operating characteristics should be recorded during the on-state mode (guided current) and during the switching events (SM capacitor voltage and guided current). Hence, it was necessary to record the referred electrical signals for the 6N submodules, and, in addition, the firing pulses S_{jki} were also recorded to acknowledge the states of each particular switch.

In terms of the semiconductor device used, in accordance with the operating conditions presented in the Table 5.1. The nominal voltage of the capacitors and the electrical current flow on the stacks of the

converter, the ABB device 5SNA 1500E250300 seems to be a possible option [156]. The details of this semiconductor device and the methodology followed to estimate the power losses produced in this application are further detailed in the next sections.

On-state losses

The conducting losses of the semiconductors are affected by several phenomenons such as: the device's junction temperature (T_j), the voltage drop at the devices terminals (IGBTs: $U_{CE_{sat}}$/ diodes U_F), the operating currents (IGBTs: i_{CE} / diodes i_F) and, in case of IGBTs, the driver circuitry voltage (U_g). The average on-state losses of a single SM IGBT ($P_{T1}^{con}/P_{T2}^{con}$) and the diodes ($P_{D1}^{con}/P_{D2}^{con}$) over a grid period ($[t_s, T_s]$) are given by (5.4) and (5.5) respectively [155].

$$P_{T\lambda}^{con} = \frac{1}{T_{ss}} \int_{t_s}^{t_s+T_{ss}} i_{CE}(t)\ U_{CE}^{[U_g,T_j]}\left(i_{CE}(t)\right) dt \tag{5.4}$$

where λ, in this context addresses the upper ($\lambda = 1$) or the lower upper ($\lambda = 2$) switch of the HBSM.

$$P_{D\lambda}^{con} = \frac{1}{T_{ss}} \int_{t_s}^{t_s+T_{ss}} i_F(t)\ U_F^{[T_j]}\left(i_F(t)\right) dt \tag{5.5}$$

Particularizing (5.4) and (5.5) to the specific IGBTs and diodes of the jki SM, as well as, the operating state S_{jki} of the SM[2], it respectively leads to:

$$P_{T\lambda_{jki}}^{con} = \frac{1}{T_{ss}} \int_{t_s}^{t_s+T_{ss}} i_{jk}(t)\ U_{CE}^{[U_g,T_j]}\left(i_{jk}(t)\right) S_{T\lambda jki}(t) dt \tag{5.6}$$

$$P_{D\lambda_{jki}}^{con} = \frac{1}{T_{ss}} \int_{t_s}^{t_s+T_{ss}} i_{jk}(t)\ U_F^{[T_j]}\left(i_{jk}(t)\right) S_{D\lambda jki}(t) dt \tag{5.7}$$

[2]From the SM state S_{jki} and the arm current direction, it is deduced whether the upper or lower switches, namely the diodes or the IGBTs, are the devices that are conducting. Then, a correlation between the SM state and the state of the correspondent semiconductor should be made $S_{T\lambda jki}/S_{D\lambda jki}$. The $S_{T\lambda jki} = 1/S_{T\lambda jki} = 0$ means that the IGBT $T\lambda$ is closed/open. The $S_{D\lambda jki} = 1/S_{D\lambda jki} = 0$ means that the diode $D\lambda$ is closed/open.

By applying the previous equations through all the γjki switches, the total on-state power dissipated on the semiconductors P_{cond} as:

$$P_{cond} = \sum_{\lambda jki} (P^{con}_{T_{\lambda jki}} + P^{con}_{D_{\lambda jki}}) \tag{5.8}$$

The oscillation of the junction temperature over the different operating conditions, as the voltage amplitude variation on the gating circuitry were not considered ($T_j \approx 125$ ^{o}C/ U_g= 15 V). The non-linear relation between IGBT's saturation voltage and the diode's forward voltage with the corresponding flowing currents were fitted from the manufacturer component data (5.9), and they are illustrated in Figure 5.10.

$$U(i) = a + b\ i^c \Rightarrow \begin{cases} U_{CE_{sat}}(i_{CE}) = 0.654 + 0.007889(i_{CE})^{0.7483} \\ U_F(i_F) = 0.4715 + 0.03069(i_F)^{0.5314} \end{cases} (V) \tag{5.9}$$

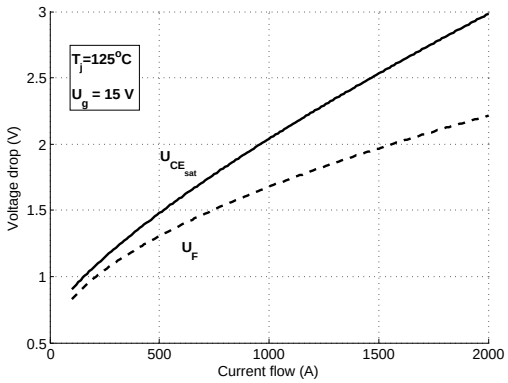


Figure 5.10: Estimated V-I characteristics of the semiconductor used.

Switching losses

The required time that a semiconductors need to commute has a nonlinear relation with the electrical current that is flowing on the correspondent instant. Therefore, due to the non-zero time interval of a switching event, some energy is dissipated. For the presented IGBT device, the switching energy loss was obtained from the component's

data-sheet and described as a cubic relation in respect to the switched current as (5.10), and illustrated in Figure 5.11.

$$E(i) = a + b\ i + c\ i^2 + d\ i^3 \Rightarrow \begin{cases} E_{on}^{U_{CE}=1250V}(i_{CE}) = (4.988\text{e-}11)i_{CE}^3 \\ \qquad\qquad + (3.697\text{e-}8)i_{CE}^2 \\ \qquad\qquad + (7.264\text{e-}4)i_{CE} \\ \qquad\qquad + 0.0868 \\ E_{off}^{U_{CE}=1250V}(i_{CE}) = (1.371\text{e-}10)i_{CE}^3 \\ \qquad\qquad - (6.740\text{e-}7)i_{CE}^2 \\ \qquad\qquad + (2.038\text{e-}3)i_{CE} \\ \qquad\qquad + 0.21 \\ E_{rec}^{U_F=1250V}(i_F) = (5.29\text{e-}11)i_F^3 \\ \qquad\qquad - (4.016\text{e-}7)i_F^2 \\ \qquad\qquad + (1.109\text{e-}3)i_F \\ \qquad\qquad + 0.1229 \end{cases} \tag{5.10}$$

where (i_{CE}, i_F) pair is the collector-emitter current of the IGBT and diode at the moment of the commutation. ($E_{on}^{1250\text{V}}$, $E_{off}^{1250\text{V}}$) pair is the energy dissipated on the turn-on and turn-off event of a IGBT which has a capacitor with 1250V across its terminals. $E_{rec}^{1250\text{V}}$ is the energy dissipated on a turn-off event of a diode which has 1250 V across its terminals.

Afterwards, the energy estimation loss (5.10) was linearly adjusted to the switched voltage value present at the device's terminals during the switching event as (5.11) [155].

$$\begin{aligned} P_{on_{T\lambda jki}} &= \frac{1}{T_{SS}} \sum_{\beta} \left(\frac{U_{c_{jki}}(t_\beta)}{U_{CE}^{REF}} \right) E_{on_T}^{[T_j]} \left(i_{jk}(t_\beta) \right) \\ P_{off_{T\lambda jki}} &= \frac{1}{T_{SS}} \sum_{\gamma} \left(\frac{U_{c_{jki}}(t_\gamma)}{U_{CE}^{REF}} \right) E_{off_T}^{[T_j]} \left(i_{jk}(t_\gamma) \right) \\ P_{rec_{D\lambda jki}} &= \frac{1}{T_{SS}} \sum_{\kappa} \left(\frac{U_{c_{jki}}(t_\kappa)}{U_{F}^{REF}} \right) E_{rec_D}^{[T_j]} \left(i_{jk}(t_\kappa) \right) \end{aligned} \tag{5.11}$$

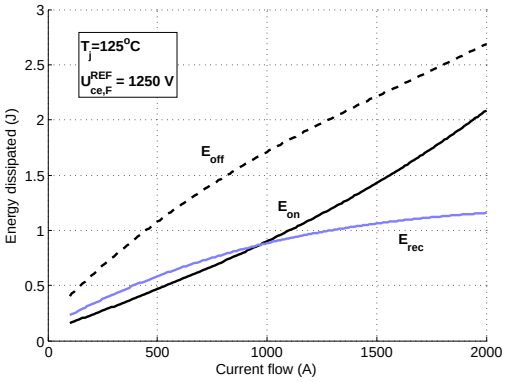


Figure 5.11: Estimated energy lost characteristics of the semiconductor.

where the $i_{CE}(t_\beta)$/ $i_{CE}(t_\gamma)$ are the switched currents and $U_{CE}(t_\beta)$/ $U_{CE}(t_\gamma)$ are the voltages at the IGBT terminals at the β/ γ triggering/ blocking events.

By applying the previous equations through all the jki switches, the total power dissipated on the commutation of the semiconductors P_{sw} is given by:

$$P_{sw} = \sum_{jki} (P_{onT_{jki}} + P_{offT_{jki}} + P_{recD_{jki}}) \tag{5.12}$$

5.3.2 Cell selection strategy

The consequent step of determining the target N^*_{jk} is the generation of the individual firing signals for the converter switches, in such a way that balances the energy storage of the individual capacitors. The schematic of the 'sort & select' algorithm is illustrated in Figure 5.12. The sorting algorithm (1) ranks the converter capacitors by their voltage $U_{c_{jki}}$. Then, depending on the arm current flow direction i_{jk}, it is selected in (2) the first or the last N^*_{jk} capacitors of the ranked list. As long as the target N^*_{jk} is not changed, the capacitors that are inserted on the stacks are not rotated.

As mentioned, this is accomplished by generating a firing pulse with a value 1 or 0 in $S_{jki}(t)$, to respectively insert or bypass the capacitor placed in the jki position. The cell selection algorithm embraced is

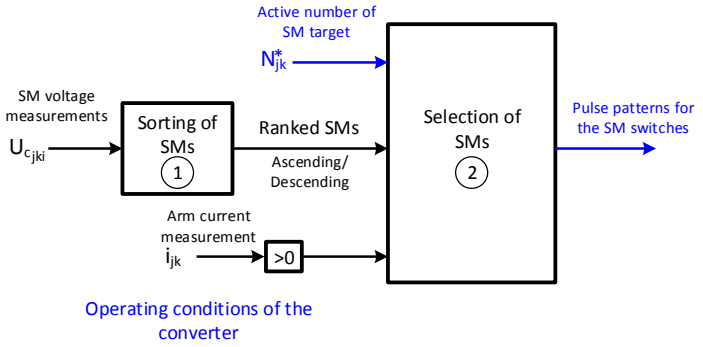


Figure 5.12: Overall scheme of the classic selection method.

named as the classic cell selection method [43] and further details are provided in the Chapter 7.

5.3.3 Carriers frequency in the CB-PWM methods

In order to achieve a fair comparison between all the modulation strategies presented, a set of operating conditions was considered on the frequency design of the carriers used.

As mentioned, each particular carrier-based method introduces a significant harmonic content centered on a specific harmonic frequency of the MMC's line-neutral voltages spectrum. This frequency is designated in this work as the carrier central frequency f_{cc}. The intrinsic nature of the carrier's disposition endorses a particular harmonic spectrum of the arm voltages. Then, in order to achieve a fair harmonic distortion comparison between all the modulation techniques, the central frequency should be the same for all the CB-PWM methods.

To reach an equivalent total harmonic distortion over the three *emf* voltages of the converter, the central frequency of the carriers should be equal to an odd multiple of three of the fundamental grid frequency (5.13) [141].

$$f_{cc} = 3(2n-1)f_{grid} \qquad n{=}1{,}2\ ...\infty \tag{5.13}$$

In accordance with what has been mentioned, the central frequencies selected for the carriers were the lowest three-values of n in (5.13),

Table 5.2: Selected values for the carriers frequencies.

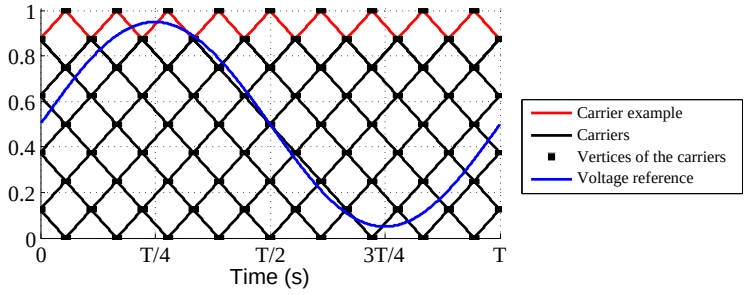
CB-PWM method		f_{cc} [Hz]		
		150	450	750
APOD, POD, PD, CO CO-PD, CO-POD, CO-APOD	f_{c1}	150	450	750
VF	f_{c1}/f_{c2}	150/ $3f_{c1}$	450/ $3f_{c1}$	750/ $3f_{c1}$
PSC	f_{c1}	$\frac{150}{N}$	$\frac{450}{N}$	$\frac{750}{N}$
PSD	f_{c1}	$2\frac{150}{N}$	$2\frac{450}{N}$	$2\frac{750}{N}$

namely 150 Hz, 450 Hz and 750 Hz. The individual frequency of each particular CB-PWM carrier is shown in the Table 5.2.

On the LS-PWM techniques, the frequency of the individual carriers is equal to the central frequency, because those techniques add significant harmonic content in the arm voltages, particularly around the carrier's frequency. On the VF technique, the carrier levels that cross the top and bottom part of the arm voltage targets have three times the frequency of the inner layers due to symmetry issues over the three-phase system, as has already been pointed out. Finally, as the phase-shift-based strategies add their harmonic content as a dependence on the number of cells and the individual carrier's frequency, the last factor was designed in such a way that the harmonic content injected in the converter arm voltages would be centered around the LS-PWM techniques.

If the carriers are designed in accordance with the Table 5.2, in terms of the APOD, PSC and PSD techniques, they will look as depicted in Figure 5.13. The figure illustrates an example of the disposition of the APOD, PSC and PSD carriers for a 8-cell-based MMC. Focusing on the disposition of the APOD carriers, their frequency is 9 times higher than the voltage reference (450 Hz if T= 20 ms). On the other hand, the carriers of the PSC and PSD methods were designed to have 56.25 Hz and 112.5 Hz respectively, as depicted in Figure 5.13(b) and Figure 5.13(c). Thus, if the resultant disposition of the carriers for the APOD, PSC and PSD methods are investigated, the arm voltage targets will

cross a particular carrier precisely at the same instant across the APOD, PSC and PSD methods. As a result, the set-points for the number of inserted capacitors N_j^* retrieved by the APOD, PSC and PSD methods will be the same. Therefore, the results obtained for the APOD, PSC and PSD techniques match together.



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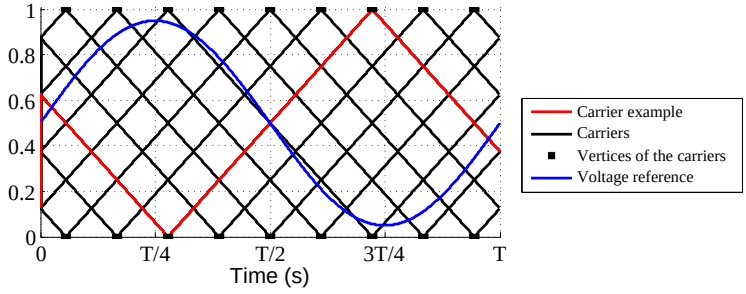

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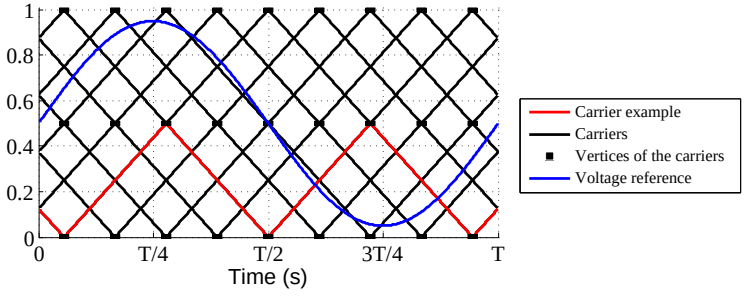


(c)

Figure 5.13: Similarity between the disposition of the carriers for the: (a) APOD,(b) PSC and (c) PSD methods.

5.4 Impact of the modulation techniques on the MMC-MVDC performance

The CB-PWM and NLM methods in conjunction with each particular ZSS strategy were used to modulate the arm voltages of the MMC in the Matlab/ Simulink environment. Then, the total harmonic distortion generated by each modulation technique is presented in the subsection 5.4.1. On the other hand, the generated losses by the converter are shown in the subsection 5.4.2. Finally, the voltage ripple of the capacitors is shown in Section 5.4.3.

5.4.1 Power quality

To inspect the impact of the CB-based techniques on the THD generated on the arm voltages, they were first implemented for the central frequency of 150 Hz, 450 Hz and 750 Hz without the presence of the ZSS. In addition, they were also compared with the NLM. The results are shown in Figure 5.14.

As illustrated in the figure, the NLM is kept equal for the three f_{cc} scenarios, since it is not a frequency dependent technique. In addition, it is the technique that minimizes the THD of the arm voltages (whenever no ZSS is considered). Furthermore, as the central frequency increases, the THD of the voltage becomes higher, independently of the CB-PWM employed. Particularly, the CO-POD is the technique that is most affected with the increase of f_{cc}, its THD is 8.6 %, 11.5 % and 14.2 % for the f_{cc} respectively equal to 150 Hz, 450 Hz and 750 Hz. This occurs because the harmonics generated around the central frequency become more dominant as the frequency of the carriers are incremented, as Figure 5.15 suggests.

If the zero sequence signals are considered on the MMC arm's voltage modulation, more harmonic frequencies are included, which then magnifies the THD factor of the arm voltages, as depicted in Figure 5.16. In the no-ZSS-based scenario, the arm voltages present less harmonic content and, logically, the lowest THD factor is retrieved regardless of the frequency considered for the modulation techniques. By including

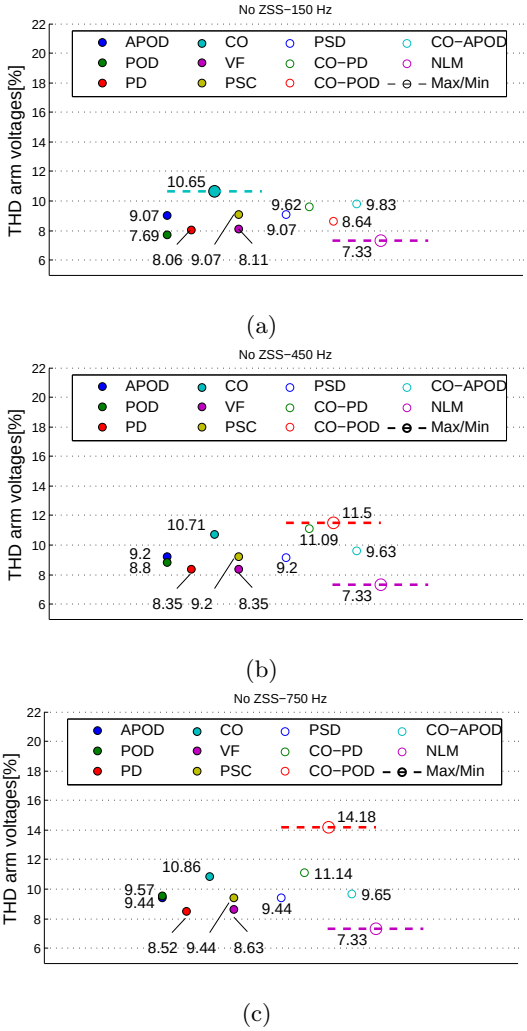


Figure 5.14: Modulation techniques impact on the arms voltages THD: (a) f_{cc}= 150 Hz, (b) f_{cc}= 450 Hz and (c) f_{cc}= 750 Hz.

a third harmonic with (1/6) of the *emf*'s magnitude of the converter into its modulation, it is the second-lowest THD-based solution. In contrast, if it included a third-harmonic with (1/4) of the converter's magnitude, it originates higher THD factors than for the (1/6) condition and slightly higher than the THD factors retrieved by the SFO. As the discontinuous-ZSS is composed of several third-order-based harmonics, it severely impacts on the arm voltages THD factors.

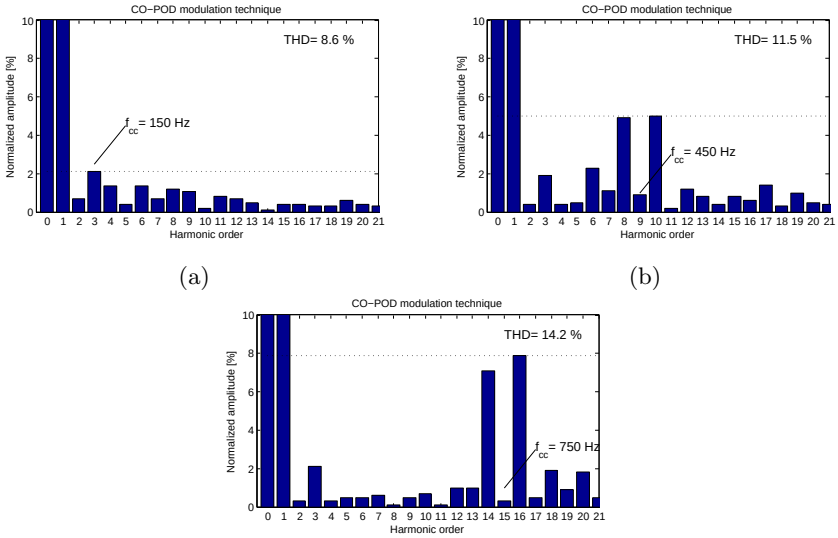
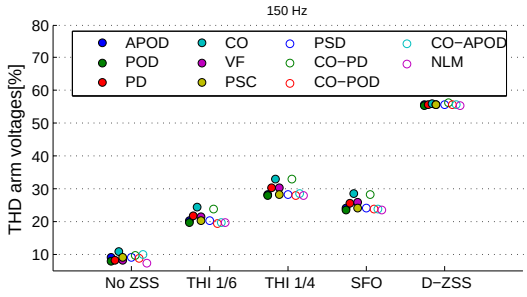


Figure 5.15: Carrier's frequency impact on the arm's voltage spectrum: (a) f_{cc}= 150 Hz, (b) f_{cc}= 450 Hz and (c) f_{cc}= 750 Hz.

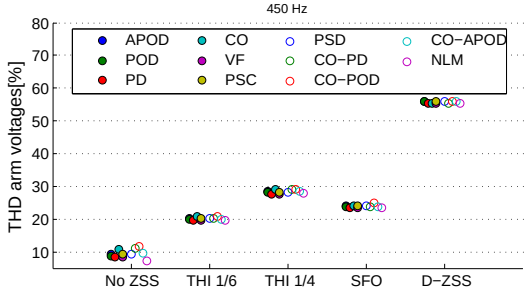
In terms of the total harmonic distortion (THD) of the grid currents, the results retrieved by the combination of the modulation techniques are displayed in Figure 5.17.

First, the MMC operation emphasizes a notably low harmonic distortion of its grid current waveforms, which is an accurate indicator of the power quality of its waveforms. The presented arm voltage modulations retrieve the remarkable values for THD between 0.71 % and 2.55 %. The POD-based techniques are the modulation solutions that more harmonics inject into the grid line currents (apart from the carrier's frequency). In opposition, the NLM is the technique that most reduces the grid line THD. Furthermore, the remaining strategies retrieve alike results in terms of the current THD. In terms of the zero sequence signals, their impact on the grid-line currents' THD is also indistinguishable, as they got canceled at the line-to-line voltage converter's output.

For the frequency dependent modulation techniques, the minimum THD factors for the ac currents are obtained for the lowest central frequency examined, namely for f_{cc}=150 Hz.



(a)



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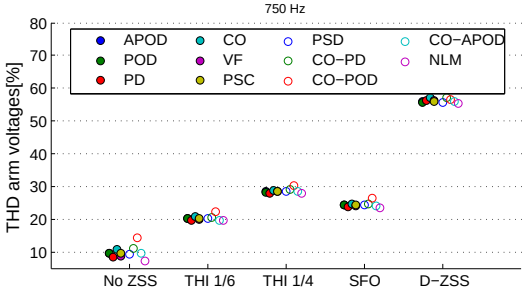
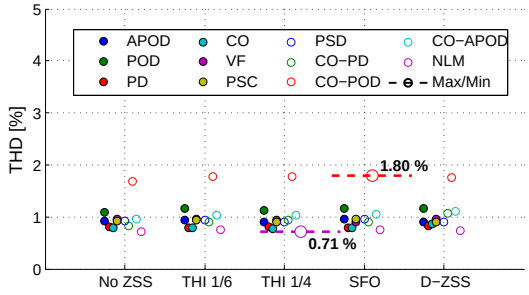
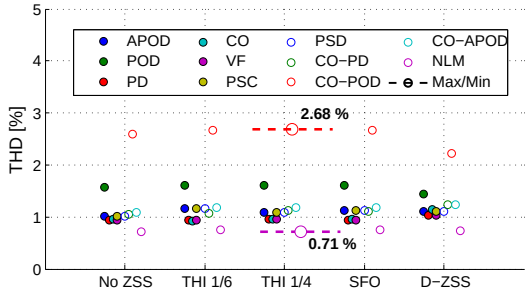


(c)

Figure 5.16: Impact of the ZSS on the arm's voltage THD: (a) f_{cc}= 150 Hz, (b) f_{cc}= 450 Hz and (c) f_{cc}= 750 Hz.



(a)



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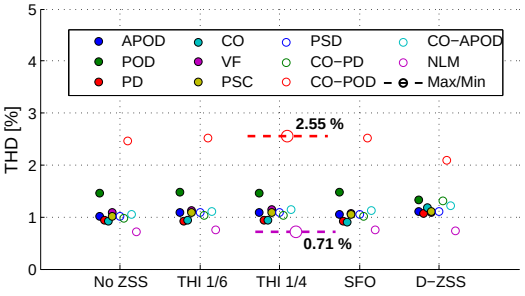


(c)

Figure 5.17: Modulation methods impact on the total harmonic distortion of the MMC's line currents for: (a) f_{cc}= 150 Hz, (b) f_{cc}= 450 Hz and (c) f_{cc}= 750 Hz.

5.4.2 Converter efficiency

This section presents the average power losses produced by the MMC semiconductors. Once the results were extracted from the Matlab/ Simulink model, the methodology presented in Section 5.3.1 was followed to estimate the power losses. As mentioned, the power losses were categorized as conducting P_{cond}, for the intervals that the semiconductors were closed and hence guiding the arm currents, or as switching losses P_{sw}, for the events that the semiconductors changed their state. For each combination between the modulation techniques, carrier's central frequency (if applied) and the ZSSs presented, the conducting and switching power losses generated were quantified, which are depicted in Figure 5.18 and Figure 5.19 respectively.

As the converter nature requires the arm current to be continuously flowing, there is always one semiconductor per submodule that is closed and carrying the arm current. Then, according to the converter model (Table 5.1), there are always 28 semiconductors (IGBTs and/ or diodes) conducting on the converter stacks. The fact that the converter is operating with the same power flow conditions in all the modulation techniques presented, the number of inserted capacitors in each leg is roughly equal. Thus, all the modulation techniques intrinsically enforce that the number and the nature of the closed switches are approximately the same. For this reason it is reinforced that regardless of the strategy adopted to modulate the arm voltages, the average conducting losses of the MMC are identical. Therefore, under those conditions, as the vertical bar graph of Figure 5.18 illustrates, the conducting power losses are approximately equal for the three f_{cc} scenarios studied, and their variance is practically nonexistent.

In terms of the semiconductor's power losses during the commutation events, as revealed in Figure 5.19, they are attached to the modulation strategy used. In the interest of the carrier's central frequency, as it increases, the target for inserting the number of cells N^*_{jk} is more often varied. Therefore, according to the classic cell selection method used, if N^*_{jk} has more pulses, the MMC cells are more often rotated. This issue directly increases the semiconductor's switching frequency and, as a

result, they will dissipate more power. Moreover, the fact of increasing the f_{cc} factor, as the vertical bar graph of Figure 5.19 presents, the switching losses variance becomes more expanded.

Another important aspect for this study is the performance of the discontinuous zero sequence signal that is injected into the arms voltage modulation. Independently of the methodology followed to synthesize the arm voltages, if a discontinuous zero sequence signal is used to bypass the capacitors on the most stressful intervals of the semiconductors, according to the selective control of the cells adopted, it certainly reduces the power losses (switching). For the modulation scenarios studied, the aggregation between the NLM modulation with the DZSS minimizes the switching power losses and the aggregation makes the usage of the CB-PWM techniques pointless from the converter efficiency perspective.

If the continuous-based ZSS are used instead, the converter performance should be evaluated individually to the modulation strategy considered. This happens because it is not a straightforward correlation between the continuous-based ZSS features with the disposition and frequency of the carriers. However, the APOD/ PSC/ PSD tend to be the CB-based techniques that most reduces the switching losses (f_{cc}=150 Hz). As the increase of the f_{cc} factor leads to a further increase of the power dissipation on the CB-based scenarios, on the f_{cc}= 450 Hz and f_{cc}= 750 Hz circumstances, all the CB techniques exceed the power dissipation retrieved by the NLM. In contrast, due to the nature of the carrier-overlapping-based techniques, for the same f_{cc} factor as the other CB-PWM solutions, the modulation indexes m_{jk} intercepts the carriers more times, which imposes more pulses in N^*_{jk}. Therefore, the CO-based techniques tend to compute higher switching events and power losses as the central frequency factor is enlarged.

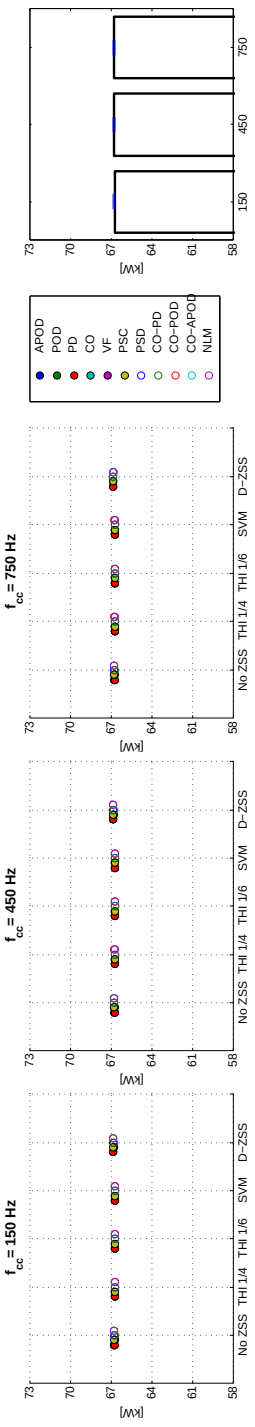


Figure 5.18: Summary of semiconductor's conducting losses retrieved by the presented modulation techniques.

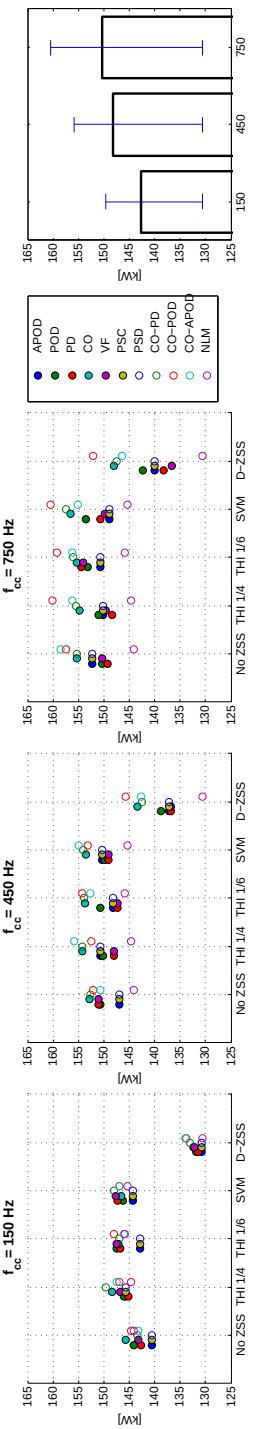


Figure 5.19: Summary of semiconductor's switching losses retrieved by the presented modulation techniques.

From an efficiency point of view, it is more advantageous to use either the APOD/ PSC/ PSD (f_{cc}=150 Hz without ZSS) or the NLM (with the DZSS) due to their reduced generation of the power losses. In fact, even for the DZSS injection scenario, both solutions are very close. Hence, the decision to move forward to either solutions may depend on the intrinsic hardware implementation difficulty that each one requires. Finally, the total power losses produced can vary from 167 kW (67 kW + 130 kW) to 207 kW (67 kW + 140 kW), depending if the NLM with the DZSS is adopted or the referred CB-based techniques without the ZSS, respectively. Either ways, the power losses of the semiconductor's is roughly equal to 1 % of the MMC rated value, which corroborates the previous analysis done in the MMC's efficiency analysis [68, 157].

The power losses produced by the MMC is greatly dependent on the cell selection method adopted. Due to the high rotation of the cells imposed by the classic cell selection method embraced, the commutation losses can be further reduced by implementing another strategy. However, since the focus of this chapter is to analyze impact of the arm voltage modulation schemes on the converter performance, this fact is considered to be out of the scope.

5.4.3 Capacitor's voltage ripple

The combination between the modulation techniques with the ZSS incites further changes on the MMC performance, namely in the capacitor's voltage ripple. The mean voltage ripple is characterized by the range of (U_{jk}^{Σ}/N) and was normalized in respect to the SPWM. The impact of the presented modulation strategies on the mean voltage ripple of the MMC's capacitors are shown in the Figures 5.20 and 5.21 respectively.

Again, the nature of the ZSS entails relevant consequences for converter performance. Regardless of the modulation itself, if the THI (1/4) is injected on the MMC arms voltage modulation, the capacitor's ripple is minimized among the selected ZSSs analyzed. This occurs because the *emf* voltage component of the arms is practically aligned with the line currents. Then, as the THI (1/4) is the technique that most

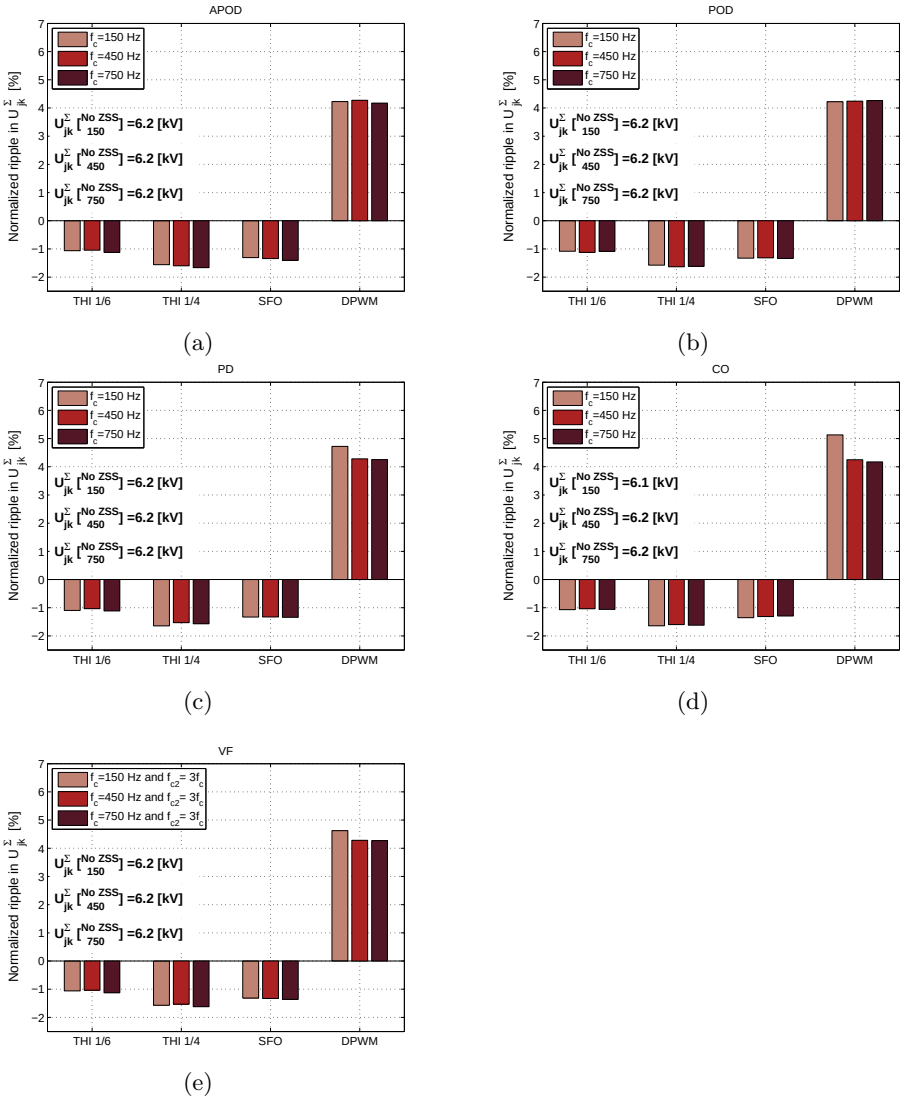


Figure 5.20: Impact of the LS modulation strategies on the capacitor's voltage ripple: (a) APOD/ PSC/PSD, (b) POD, (c) PD, (d) CO and (e) VF

reduces the amplitude of the arm voltages when the current reaches its peak, it intrinsically reduces the voltage amplitude across the converter stacks. This fact leads to a reduction of the number of capacitors that

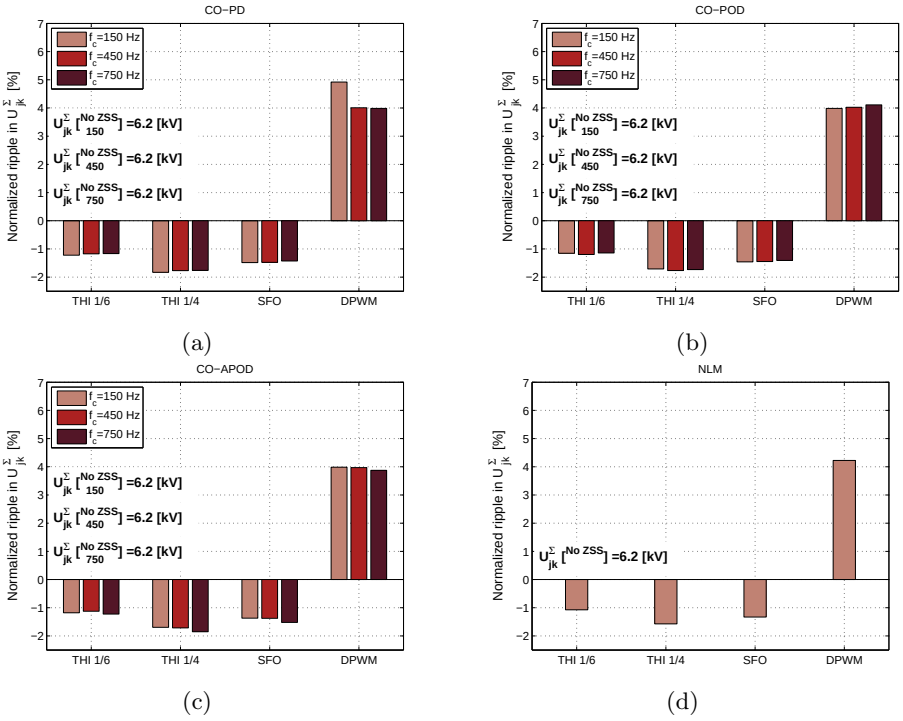


Figure 5.21: Impact of the CO-hybrid and NLM modulation strategies on the capacitor's voltage ripple: (a) CO-PD, (b) CO-POD, (c) CO-APOD, (d) NLM.

are inserted during the peak current instant, which contributes to the minimization of the capacitor's voltage ripple.

On the other hand, as the DZSS forces the capacitors to go longer without being rotated in comparison with the other ZSS techniques. Under these circumstances, the voltage ripple across the capacitors is increased to higher values than the ones obtained without the presence of any ZSS.

The most evident fact is that the inclusion of the third harmonic or the SFO into the voltage modulation, it has an higher impact on the capacitors mean voltage ripple than the predisposition of the carriers and their central frequency f_{cc}. For those ZSS techniques, the impact of

the disposition of the carriers on the capacitor's voltage ripple is below 0.3 %, which corroborates their light impact on this factor.

The fact of the carrier-overlapping-based techniques inflicting more pulses on N_{jk}^{*} than the other CB techniques, inherently contributes to a higher rotation of the converter capacitors. Thus, the CO-based schemes contributes to the capacitor's average voltage ripple reduction. Finally, the minimum voltage ripples achieved for the converter capacitors were:

- -1.83 %: for CO-PD with THI 1/4 f_{cc}= 150 Hz;
- -1.77 %: for CO-PD with THI 1/4 for f_{cc}= 450 Hz;
- -1.85 %: for CO-APOD with THI 1/4 for f_{cc}= 750 Hz;

For the reasons already pointed out, the aggregation between the CO-based techniques and the injection of the third harmonic (THI 1/4) component into the arms voltage modulation leads to the minimization of the capacitors' voltage ripple.

5.5 Conclusions

The modular multilevel converter (MMC) has very interesting features for medium voltage applications, and one important concern about this converter is the modulation strategy that should be embraced. This chapter presents a review and a validation of the modulation strategies that can be used to modulate the voltages across the converter's arms.

The alliance between the zero sequence signals and the presented modulation strategies can be used to achieve several goals such as better power quality, higher efficiency or the reduction of the capacitor's voltage ripple.

The fact of adding common based signals to the converter's output voltages directly increases the total harmonic distortion of the arm voltages of the converter. However, due to the relatively high number of submodules available on the converter model, the distortion factors of

its line currents are diminished. The aggregations between the presented carrier-based strategies and zero sequence signals could not further reduce the total harmonic distortion factor retrieved by the nearest level modulation strategy, which was responsible for a factor of 0.71 %.

Regarding the efficiency of the converter, the modulation schemes for the MMC does not impact the on-state losses of the semiconductors, but on the power losses computed by the commutation of the switches. Depending on the frequency that is selected for the carriers and the existence of a continuous or discontinuous ZSS, the alternate phase opposition disposition (APOD) or the nearest level modulation strategies are the solutions that most reduces the semiconductor's power losses. Whenever the converter is operating at the nominal conditions, in the case of being modulated by those strategies, its semiconductors generate roughly 1 % of power loss.

In terms of the voltage ripple of the capacitors, in the case of modulating the arm voltages with carrier-overlapping-based techniques, a higher rotation of the capacitors is imposed which reduces their voltage ripple. Additionally, the presence of the third harmonic with (1/4) of the *emf*'s magnitude into the voltage modulation guarantees a higher reduction of the voltage ripple.

Finally, it is concluded that the selection of the modulation strategy embraced greatly depends on the factor that needs to be minimized. Generally, the nearest level modulation is responsible for generating low harmonic content on the grid currents as well as, it generates less power losses that the remaining techniques. On the other hand, regarding the ZSS, the third harmonic with (1/4) reduces the voltage ripple of the capacitors, the third harmonic with (1/6) conjointly with the SFO maximizes the linear range of the modulation and, finally, the discontinuous-ZSS reduces the switching events and the corresponding losses of the semiconductors.

Chapter 6

Adaptive D-ZSS for MMC applications

The modular multilevel converter (MMC) is being adopted by the HVdc industry due to its interesting features, such as its efficiency, which is greatly affected by the modulation strategy adopted. From the perspective of converter voltage modulation, there are two main options that notably impact the MMC's efficiency, namely the strategy used to rotate the inserted capacitors and the aggregation of the zero sequence signals (ZSS).

As depicted in the previous chapter, the presence of the discontinuous zero-sequence signals (D-ZSS) in the arm's voltage modulation improves the MMC's efficiency. So, this chapter formally proposes a technique to inject a D-ZSS into the MMC's voltage modulation in order to avoid/ eliminate the semiconductor's switching events on the time intervals where their load is maximum. According to the converter output voltage magnitude and phase angle, the ZSS injection into the arms voltage modulation will be adjusted in such a way that clamps the MMC arm voltages over 60 degrees. By doing this on the referred 60 degrees intervals, the semiconductor's switching events are reduced which retrieves less switching losses. The steady-state and dynamic performance of the proposed method were supported by simulation.

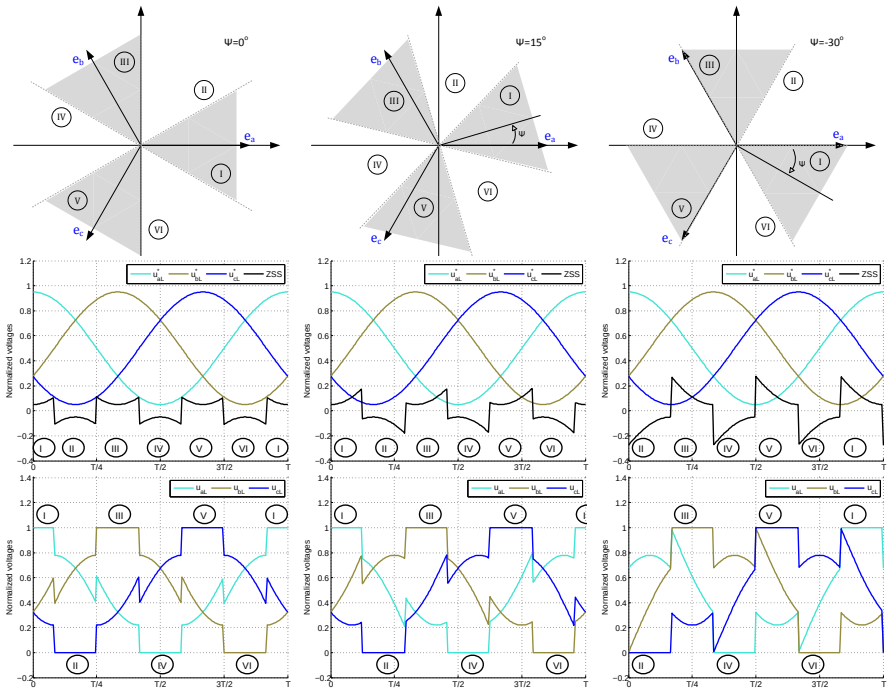
6.1 The D-ZSS applied on the MMC

A zero sequence signal (ZSS) is a triple-order-harmonics-based signal that is added to each output voltage reference on the three-phase voltage source converters. Depending on the nature of the ZSS selected a superior performance of the VSCs is obtained [143, 158]. Particularly, the discontinuous-based ZSS (D-ZSS) are employed in VSCs, in order to clamp their line-neutral voltages to a particular level. By implementing this feature on the time intervals where the semiconductors drive large currents, thereby retrieving large switching losses, it allows the reduction or elimination of the switching occurrences when the semiconductor's load is high. With the adoption of the D-ZSS, when compared to the non-ZSS-based scenario, the number of switching events can be potentially higher but they occur on instants with a relatively low load, which allegedly leads to a more efficient operation of the converter.

The voltage clamping on the three-phase VSCs is done in periodic time intervals, such as $(\pi/6)$, $(\pi/3)$ and $(2\pi/3)$ radians [158] [151]. To achieve that goal, the fundamental (2π) period is respectively subdivided into 12, 6 and 3 intervals and, in each particular section, a particular arm of the converter is clamped. This work focuses on the $(\pi/3)$ clamping periods, which are illustrated in Figure 6.1. In this scenario, as mentioned, the fundamental period is subdivided into sextants, which are numbered from I to VI. In the odd sextants (I, III and V, which are colored in gray) the *emf* of the converter phases e_j are clamped to an upper bound. On the other hand, in the even sextants (II, IV and VI, which are colored in white), the *emf* voltages are correspondingly clamped to a lower voltage bound. In each particular sextant, the arm voltages are suitably clamped to subsequently address the clamping intervals of the e_j intervals.

Moreover, the rotation of the defined sextants, by means of ψ, clamps the converter voltages over different phase angles. This reshapes the arm voltages, which became flat at different intervals. Contextualizing to the MMC and depending on the selective control of the cells embraced, this feature can avoid the rotation of the SMs in the re-

ferred clamping intervals, reducing the amount of energy lost considerably. The application of the D-ZSS have intrinsic technical limits on the MMC, which are explored in the next section.



(a) $\psi = 0$ rad. (b) $\psi = 15$ rad. (c) $\psi = -30$ rad.

Figure 6.1: Impact of the D-ZSS on the normalized upper arms voltages of the modular multilevel converter.

6.1.1 Technical limits and context

The action of imposing a flat voltage on the converter arms is not a straightforward task, as in the case of the two-level converters. Focusing on the MMC with two arms on each phase unit, whenever the arm k is clamped to zero, all the correspondent capacitors are removed from the arm current flow over a sixty-degree interval. Hence, in order to impose the required dc voltage at the correspondent phase unit's terminals, the appropriate number of capacitors should be inserted on the

remaining arm. Hence, if in one hand all the capacitors are removed from the arm current flow, on the remaining arm, most of the capacitors become inserted, during the aforementioned sixty degrees interval. This fact, have a strong impact on the capacitor's voltage ripple amplitude. Due to the clamping interval, on the most stressed arm, the capacitor's eventually become more time inserted, which leads to an higher voltage ripple amplitude.

In order to verify the impact of the D-ZSS on the converter efficiency, a cell selection algorithm whose performance do not rely on the ripple amplitude of the capacitor's voltage was selected, namely the classic cell selection method (see Chapter 6).

Another important fact is the modulation of the converter arms (3.34). Whenever a D-ZSS is added to the arm voltage references, even if the arm voltage becomes flat on the correspondent interval, the number of inserted capacitors should be changed due to the charge/discharge of the inserted capacitors which are subject to the flowing current, as shown in Figure 6.2(a). As illustrated, around $t = T/2$, the arm voltage reference is maintained flat at ≈ 0.9 pu, and due to the discharge of the inserted capacitors U_{jk}^{Σ}, the arm modulation index is increased up to one, inserting all the capacitor in the stack. Therefore, in the eventual need to clamp the arm voltages to a higher level this could not be possible, because the correspondent phase unit can not ensure U_{dc} at the correspondent terminals. Then, the feasibility of this method varies with the converter design. Specifically, the average value of the voltage sum of the capacitors may take the following values:

- $U_{jk}^{\Sigma} = U_{dc} \rightarrow$ In this scenario, the maximum clamping voltage is less than one. Due to discharge of the capacitors during the clamping interval, the modulation index increases and it can saturate the converter ($m_{jk} = 1$), as shown in Figure 6.2(a). As illustrated, according to the aforementioned operating conditions and design, whenever the arm voltages are clamped to 0.9 pu, at the end of the clamping interval, the arm insertion index is already one. If an higher clamping voltage value is intended, the modula-

tion index will be saturated, which will cause voltage oscillations in the dc bus.

- $U_{jk}^{\Sigma} > U_{dc} \rightarrow$ In this case, not all the cells are used to synthesize the required dc voltage, however they are rotated over the time to guarantee symmetrical energy distribution among the cells. As U_{jk}^{Σ} increases beyond U_{dc}, more cells become redundant and the arm voltages can be clamped to higher voltage values, as Figure 6.2(b) illustrates. The fact of $U_{jk}^{\Sigma}/U_{dc} \approx 1.1$, reduces the arm modulation index peak, which allows the arm voltage to be clamped to an higher value ($u_{jk} = U_{dc}$), without saturating m_{jk}.

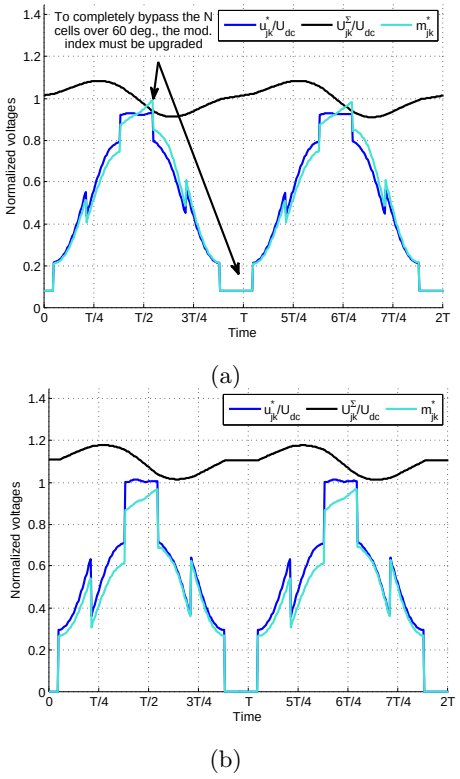
With the aim of achieving a modular converter design that can clamp the arm voltages up to 1 pu, only the second scenario was explored in this work, particularly in Section 6.2.

6.1.2 Formulation of the ZSS

In terms of the formulation of the ZSS, this is accomplished in real time depending on the phase angle of the converter *rms*. Depending on the disposition of the sextants, as previously emphasized in Figure 6.1, it is directly known what is the arm voltage that should be clamped. Therefore, the first definition of the D-ZSS is the clamping intervals, which vary with the sextants disposition ψ (defined in Figure 6.1). Consequently, the second concern is the maximum voltage that can be imposed on the converter arms to ergo clamp them. To address this goal, a proper value is computed for the zero sequence signal ZSS(t) and it is consequently added to the stack voltage targets (3.16). As a result, the voltage targets for the MMC arms become:

$$\begin{cases} u_{jU}^{*}(t) = \dfrac{U_{dc}(t)}{2} - \left[e_j^{*}(t) + \mathrm{ZSS}(t)\right] - \dfrac{u_{diff_j}^{*}(t)}{2} \\ u_{jL}^{*}(t) = \dfrac{U_{dc}(t)}{2} + \left[e_j^{*}(t) + \mathrm{ZSS}(t)\right] - \dfrac{u_{diff_j}^{*}(t)}{2} \end{cases} \tag{6.1}$$

Considering that the cell's insertion indexes are not saturated, as the upper/ lower arm voltages are affected with the ZSS in anti-phase, from the dc-side perspective, the D-ZSS does not impact the dc-side



(a)

(b)

Figure 6.2: D-ZSS impact: (a) on a dc-bus coupled-based MMC ($U_{jk}^{\Sigma} = U_{dc}$) or (b) on a dc-bus decoupled-based MMC ($U_{jk}^{\Sigma} \neq U_{dc}$).

voltage control dynamics. This occurs due to the fact that, from the dc perspective, it is still synthesized ($U_{dc}(t) - u^*_{diff_j}(t)$) (3.10), which is obtained from the sum of both equations in (6.1). However, the ZSS(t) does impact on the voltages that are synthesized across the MMC stacks.

Therefore, according to (6.1) and the arguments already presented, in any moment, the voltage sum of the upper and lower arm target should not exceed (6.2), otherwise, the internal voltage drop target $u^*_{diff_j}$ is no longer achievable, which may lead to an uncontrolled scenario of the converter inner currents.

$$u^*_{jU}(t) + u^*_{jL}(t) = U_{dc}(t) - u^*_{diff_j}(t) \tag{6.2}$$

Focusing on the first sextant, since the *emf* of the leg "a" of the MMC should be clamped to the highest voltage level, the proposed

ZSS(t) that can be included in the arm voltage targets is given by (6.3) which accordingly defines the final arm voltage targets in the first sextant (6.4).

$$\mathrm{ZSS}(t) = \frac{U_{dc}(t)}{2} - \frac{u^*_{diff_a}(t)}{2} - e_a(t) \tag{6.3}$$

$$\begin{cases} u_{aU} = 0 \\ u_{aL} = U_{dc}(t) - u_{diff_a} \\ u_{bU} = -e_b - \dfrac{u^*_{diff_b}(t)}{2} + e_a + \dfrac{u^*_{diff_a}(t)}{2} \\ u_{bL} = U_{dc}(t) + e_b - \dfrac{u^*_{diff_b}(t)}{2} - e_a - \dfrac{u^*_{diff_a}(t)}{2} \\ u_{cU} = -e_c - \dfrac{u^*_{diff_c}(t)}{2} + e_a + \dfrac{u^*_{diff_a}(t)}{2} \\ u_{cL} = U_{dc}(t) + e_c - \dfrac{u^*_{diff_c}(t)}{2} - e_a - \dfrac{u^*_{diff_a}(t)}{2} \end{cases} \tag{6.4}$$

In this scenario, the arm voltage target in u_{aU} is zero, which means that no capacitors need to be inserted during the sextant. Under these circumstances, as there is no energy variation of the capacitors in the aU stack, there is no need to rotate the correspondent capacitors. As a result, no switching events will occur on the correspondent arm during the referred-to sextant. In addition, the synthesized *emf* of the phase "a" will be clamped to (6.5), as pretended.

$$e_a = \frac{U_{dc}(t) - u_{diff_a}(t)}{2} \tag{6.5}$$

Furthermore, in respect to (6.3), if the first component ($U_{dc}/2$) is affected by a voltage level factor k ($k \leq 1$), it is possible to clamp the arm voltages to relatively lower values. This is particularly important in those MMC designs that can have technical limitations, as argued in the previous section. Hence, the generic definition of the ZSS(t) on the sextant I becomes equal to (6.6), which accordingly leads to the arm voltage targets (6.7).

$$\mathrm{ZSS}(t) = k\frac{U_{dc}(t)}{2} - \frac{u^*_{diff_a}(t)}{2} - e_a(t) \tag{6.6}$$

$$\begin{cases} u_{aU} = \dfrac{U_{dc}(t)}{2}(1-k) \\ u_{aL} = \dfrac{U_{dc}(t)}{2}(1+k) - u_{diff_a} \\ u_{bU} = \dfrac{U_{dc}(t)}{2}(1-k) - e_b - \dfrac{u^*_{diff_b}(t)}{2} + e_a + \dfrac{u^*_{diff_a}(t)}{2} \\ u_{bL} = \dfrac{U_{dc}(t)}{2}(1+k) + e_b - \dfrac{u^*_{diff_b}(t)}{2} - e_a - \dfrac{u^*_{diff_a}(t)}{2} \\ u_{cU} = \dfrac{U_{dc}(t)}{2}(1-k) - e_c - \dfrac{u^*_{diff_c}(t)}{2} + e_a + \dfrac{u^*_{diff_a}(t)}{2} \\ u_{cL} = \dfrac{U_{dc}(t)}{2}(1+k) + e_c - \dfrac{u^*_{diff_c}(t)}{2} - e_a - \dfrac{u^*_{diff_a}(t)}{2} \end{cases} \tag{6.7}$$

The same reasoning can be employed in deducing the converter arm references on the remaining sextants, which results in the generic ZSS(t) form presented in the Table 6.1.

Sextant		Clamp Interval			ZSS(t)	
I	$e_a \uparrow$	0	$\leq \theta_c <$	$\pi/6+\psi$	$\left(k\frac{U_{dc}(t)}{2} - \frac{u^*_{diff_a}(t)}{2}\right)$	$-e_a(t)$
II	$e_c \downarrow$	$\pi/6+\psi$	$\leq \theta_c <$	$3\pi/6+\psi$	$-\left(k\frac{U_{dc}(t)}{2} - \frac{u^*_{diff_c}(t)}{2}\right)$	$-e_c(t)$
III	$e_b \uparrow$	$3\pi/6+\psi$	$\leq \theta_c <$	$5\pi/6+\psi$	$\left(k\frac{U_{dc}(t)}{2} - \frac{u^*_{diff_b}(t)}{2}\right)$	$-e_b(t)$
IV	$e_a \downarrow$	$5\pi/6+\psi$	$\leq \theta_c <$	$7\pi/6+\psi$	$-\left(k\frac{U_{dc}(t)}{2} - \frac{u^*_{diff_a}(t)}{2}\right)$	$-e_a(t)$
V	$e_c \uparrow$	$7\pi/6+\psi$	$\leq \theta_c <$	$9\pi/6+\psi$	$\left(k\frac{U_{dc}(t)}{2} - \frac{u^*_{diff_c}(t)}{2}\right)$	$-e_c(t)$
VI	$e_b \downarrow$	$9\pi/6+\psi$	$\leq \theta_c <$	$11\pi/6+\psi$	$-\left(k\frac{U_{dc}(t)}{2} - \frac{u^*_{diff_b}(t)}{2}\right)$	$-e_b(t)$
I	$e_a \uparrow$	$11\pi/6+\psi$	$\leq \theta_c <$	2π	$\left(k\frac{U_{dc}(t)}{2} - \frac{u^*_{diff_a}(t)}{2}\right)$	$-e_a(t)$

Table 6.1: Formulation of the D-ZSS.

where θ_c ($0 \leq \theta_c \leq 2\pi$) is the phase angle of the converter ac voltage e_j. ψ is the phase shift of the ZSS in respect to the converter phase.

6.2 Validation of the ZSS scheme

The impact of the discontinuous-based zero sequence signal (D-ZSS) on the HVdc-based modular multilevel converter performance is analyzed in this section. To carry out this task, the parameters of the INELFE HVdc transmission scheme were considered (see Appendix A).

As mentioned, the injection of the D-ZSS into the converter modulation can avoid semiconductor switching events at particular intervals, namely, those which the commutations dissipate higher losses. As introduced in the previous section, there are two degrees of freedom when it comes to the D-ZSS on the MMC, namely the clamping voltage (k) and the phase of the ZSS (ψ). The clamping factor k addresses the clamping voltage on the converter arms. On the other hand, the second parameter, namely the ZSS's phase angle, addresses the corresponding time interval to the referred clamping voltage.

In this context, the case study is analyzed in steady-state and its dynamic operation. On the steady-state operation, discussed in Section 6.2.1, the impact of the clamping voltage on the converter performance is analyzed while ψ is managed to clamp the arm voltages on the intervals whose arm currents are maximum. Thereafter, the impact of the power factor change on the D-ZSS's phase angle ψ and the resulting converter performance is presented in the dynamic operation Section 6.2.2.

6.2.1 Steady-state operation

The D-ZSS and its impact on the converter steady-state performance is addressed in this section. As discussed earlier, due to its multilevel characteristics of the MMC, there is the degree of freedom on what voltage should be elected to clamp arm voltages, which accordingly leads to different benefits.

The steady-state assessment was based on the a fundamental cycle operation of the converter at its nominal power conditions. The effect of several clamping voltage factors k, on the most relevant variables of the MMC is displayed in the Figures 6.3, 6.4 and 6.5, correspondingly for k=0.85, k=0.925 and k=1.

The results correspond to one fundamental grid cycle. Particularly, at t=10 ms, the phase angle of the converter *emf* was located on the first sextant[1]. From Figures 6.3(a), 6.4(a) and 6.5(a) it is deduced

[1]The arm voltages u_{aU}/u_{aL} are respectively clamped to a low/high voltage level,

that, on the first sextant, the clamping factor increase directly leads an higher/lower insertion of capacitors in series on the aL/aU arms. Regarding the aU arm, the reduction of the number of inserted capacitors is also responsible for the reduction of their voltage variation $dU_{aU}^{\Sigma}(t)/dt$ (see Figures 6.3(b), 6.4(b) and 6.5(b)). On the k=1 scenario, during the sixty-degree interval, all the aU capacitors become bypassed and therefore, the remaining aL withstands the dc voltage in the corresponding interval.

Regardless of the k factor selected, as displayed in the Figures 6.3(c), 6.4(c) and 6.5(c), it can be detected that the flat tops of e_a are aligned with the grid current peaks, as it was intended. In addition, as previously argued, one of the arms within the same phase unit is necessarily clamped to a low voltage level based on the factor k. Under these circumstances, due to the low target number of inserted capacitors, the D-ZSS demands fewer switching events in comparison to the sinusoidal-based modulation. At the limit that (k=1), all the capacitors become bypassed which inflicts a flat bottom voltage on the suitable arm (equal to zero). Moreover, no switching events occur during the corresponding 60-degree interval.

Regarding converter power quality, the action of increasing the clamping factor accordingly leads to the increase of the triple-based harmonics magnitude present on the arms voltages. Thus, as emphasized in Figures 6.3(d),6.4(d) and 6.5(d), regardless of the k factor selected, the triple order harmonics present on the converter *emf* become canceled due its three-phase symmetry.

The methodology proposed in [155] to estimate the semiconductor's losses was adopted. Moreover, the semiconductor's power losses and the average voltage ripple of the MMC capacitors were quantified and presented in Table 6.2. First, it should be emphasized that, in comparison to the sinusoidal voltage modulation, the appliance of the D-ZSS reduces the total power losses of the semiconductors with the cost of an higher control complexity and a slight increase in voltage ripple on

and consequently the *emf* of the phase "a" of the converter is clamped to an upper bound.

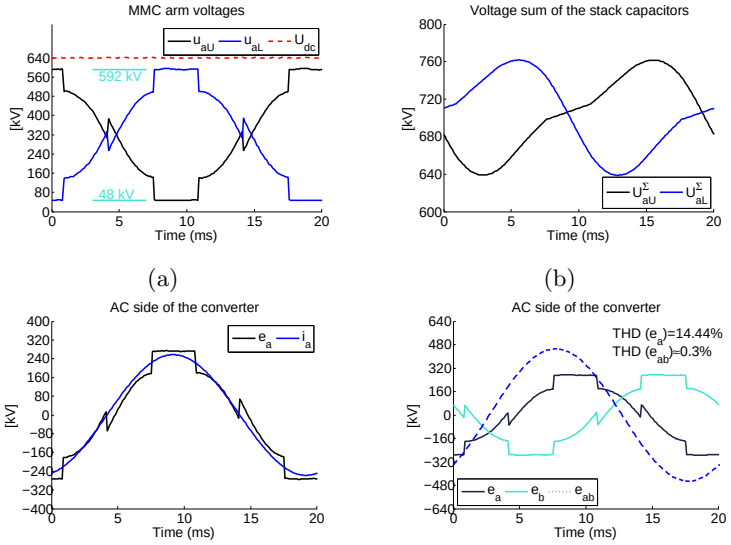


Figure 6.3: D-ZSS impact on the MMC static behavior ($k = 0.85$).

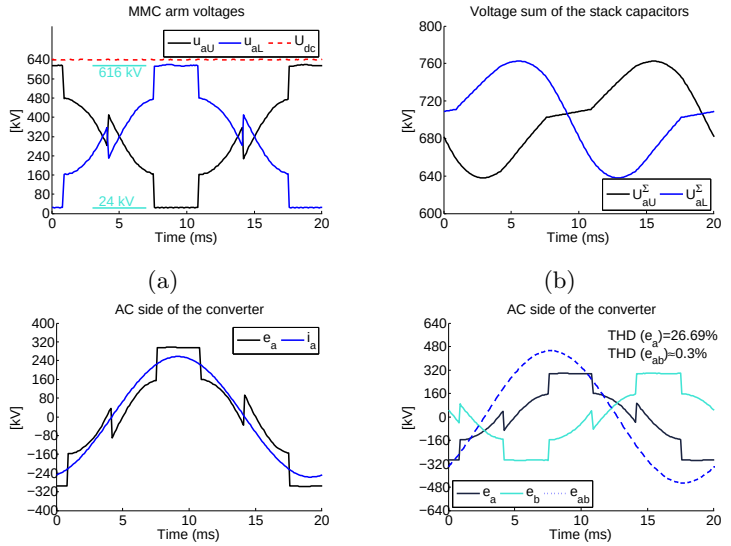


Figure 6.4: D-ZSS impact on the MMC static behavior ($k = 0.925$).

the capacitors. With the increase of the clamping factor, this technique reduces the switching events and the corresponding losses. At the limit

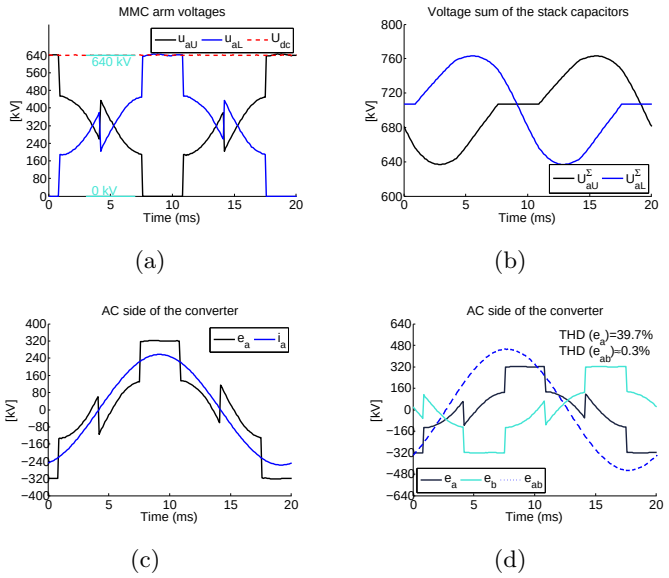


Figure 6.5: D-ZSS impact on the MMC static behavior ($k = 1.0$).

that all the capacitors are removed from the arm current path ($k = 1$), the D-ZSS provides 6.6% of total loss reduction in comparison with the sinusoidal-based modulation.

Table 6.2: Impact of the D-ZSS on MMC operation performance.

Parameters analyzed	Sinusoidal modulation	D-ZSS modulation Clamping factor k		
		0.85	0.925	1.0
Switching losses [MW]	18.95	17.71	17.59	17.31
Conduction losses [MW]	5.44	5.45	5.45	5.46
Total losses [MW]	24.39	23.16	23.05	22.77
Losses reduction [%]	-	5.0	5.5	6.6
Average peak voltage of the capacitors [V]	1912	1917	1918	1921

6.2.2 Power step-change operation

To validate the dynamics of the presented D-ZSS technique, a step-change was conceived on the reactive power flow target. Then, the converter controllers accordingly adapted the phase angle of the converter *emf* and grid currents. This action, in accordance to what was previously mentioned, demands that the D-ZSS dynamically adapt ψ to

accomplish the alignment between the arm voltages and currents. The dynamic evolution of the phase angle ψ is illustrated in Figure 6.6.

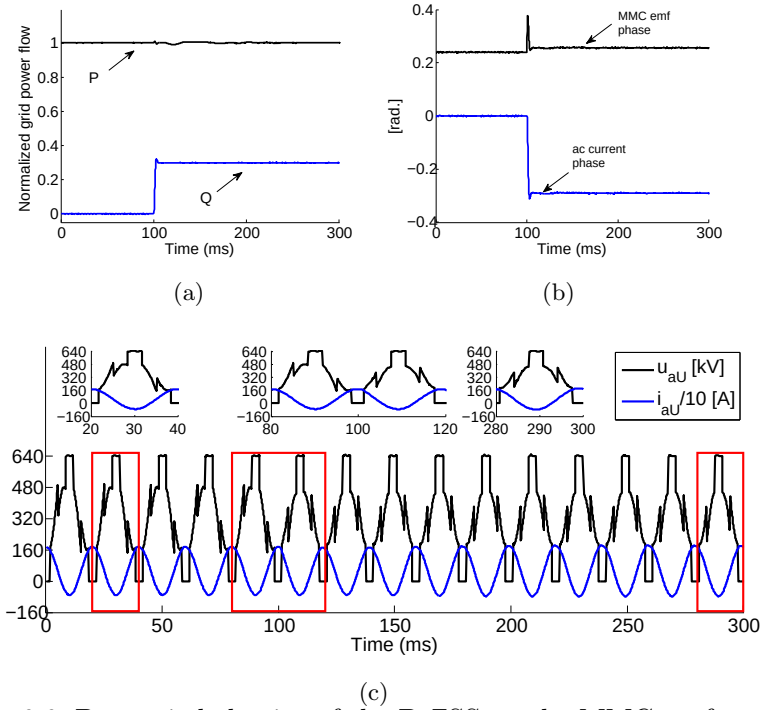


Figure 6.6: Dynamic behavior of the D-ZSS on the MMC performance.

The experiment starts with the converter injecting the nominal active power into the ac grid (see Figure 6.6(a)). At t=100 ms, the nominal step-change of 300 Mvar (cap.) is settled. The performance of this method can be analyzed by the complementary observation of the phase of the converter ac variables in Figure 6.6(b) and the arm voltages shape in Figure 6.6(c). At the beginning of the experiment the arm voltage had the shape shown in small axis on the top-left of Figure 6.6(c), with a clear alignment with the grid current. Afterwords, at the instant t=100 ms, in the presence of the reactive power flow change, the converter's emf accordingly changes its phase angle and amplitude to guarantee the required power flow. Hence, due to the phase relation between the emf and the grid current, the phase of the ZSS ψ was accordingly upgraded in order to slightly move the clamping interval, in order to be re-aligned

to the new operating conditions. The impact of this transition is clearly observed on the small axis on the top-center of Figure 6.6(c). The harmonic content of the arm voltage on the fundamental cycle [80 100]ms clearly changes to a different one at [100 120]ms, due to the arm voltage reshaping to reach an alignment with the driven current. As can be seen, the transition is very fast and, accordingly to the previous section, ensures an higher efficiency of the converter.

6.3 Conclusions

The feasibility of using discontinuous-based zero sequence signals (D-ZSS) to clamp the MMC's arm voltages, either in amplitude and interval are discussed in this work.

This technique is being used by two level converters to eliminate the switching events during the intervals with a high level of stress on the semiconductors. However, when it comes to multilevel inverters there is the degree of freedom of the clamping voltage that should be selected. The formulation of the ZSS as well as the technical limitations of the method on what concerns the converter design is discussed.

The presented method is analyzed for steady-state and dynamic conditions of the converter. Regarding the steady-state operation, the D-ZSS increases the global efficiency of the converter in respect to the sinusoidal arm modulation. As the clamping voltage is increased, fewer switching events occurred, and at the limit in which all the capacitors are removed from the current path, the D-ZSS reaches reduces the semiconductor's power losses. Several clamping factors were considered for this study and the removal of all the arm capacitors from the current flow (maximum clamping factor), is the operating condition that most reduces the total losses of the semiconductors. The maximum reduction achieved was equal to 6.6% of the total losses. Moreover, in respect to the dynamic behavior of the method, even with high power flow transients, the presented method can be rapidly adjusted to reach the alignment between the flat top voltages of the arms and the corresponding currents.

Chapter 7

Cell selection methods for Modular Multilevel Converters

Over the last decades, Europe become aware of the need to decarbonize the power system and the European countries are increasing the installed power of renewable energy sources (RES). Particularly, in the North Sea offshore wind power is being developed fast. In view of this, high voltage dc transmission (HVdc) is playing an important role to overcome technical challenges. One of the current foundations that make the VSC-HVdc attractive is the usage of the modular multilevel converter (MMC)-based solutions. However, as the number of power converters and their rated power increases, special attention is being paid to their efficiency.

The number of submodules used on the MMC can reach several hundreds of units, and the management of their states is a complex task. Several selective procedures have been proposed in the literature to manage the submodules states and they lead to different performances of the converter [43,69,95,159,160]. Each particular method has its own advantages, they can either minimize the voltage ripple on the HBSM capacitors, the switching frequency of the semiconductors, the power losses produced and, lastly, can be implemented with different levels of complexity. This work compares the performance of the some cell selection methods proposed in the literature. In addition, two selective methods to manage the HBSM states are proposed.

This work is organized as follows: Section 7.1 introduces the methodology adopted to synthesize the voltages across the converter arms. In

Section 7.2 the cell selection methods analyzed are presented. Finally, the simulation results of the strategies studied are illustrated in Section 7.3. The final comments are summarized in Section 7.4.

7.1 MMC's operating principle: insight of the cell selection method

In order to study the impact of different cell selection methods on the performance of a HVdc-based MMC, the global control diagram of the converter shown in Figure 7.1 was considered. The control structure scheme and the arm voltage modulation (direct modulation) adopted were discussed in Chapter 3. Then, in terms of the cell selection method stage, as shown in Figure 7.1 it was sub-divided in two stages. The first sub-stage deals with the methodology embraced to compute the target number of inserted capacitors N^*_{jk}, which was previously discussed in Chapter 5. The second stage deals with the gating signals calculation of the IGBTs, which is explored in this chapter, particularly in Section 7.2.

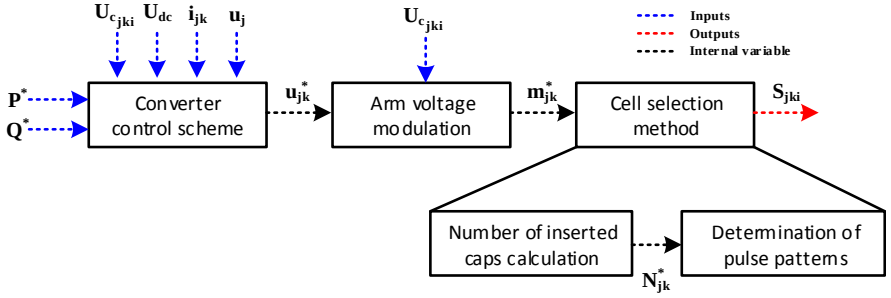


Figure 7.1: Overall control diagram of the MMC.

The nearest level modulation [45], as discussed along the previous chapters of the thesis, it is an effective method used to compute the active number of cells N^*_{jk} as:

$$N^*_{jk} = \text{round}\left(Nm^*_{jk}\right) \tag{7.1}$$

However, at the moment that the target number of inserted capacitors is computed, in the NLM strategy, the capacitor voltages on the

arm jk are treated as equal, then having an equal energy distribution. In the previous chapters that the NLM was used (sub-stage 1 in Figure 7.1), the classic cell selection method for the second sub-stage was considered [43]. Thus, since it imposes a high rotation of the capacitors in such a way that all the capacitors assembled in the same stack store approximately the same energy (see Figure 4.11), the NLM reveals to be a straightforward and competent procedure. However, the NLM entails some problems whenever the selective stage of the capacitors allow an asymmetric energy storage distribution among the capacitors assembled in the same stack.

In order to explain the bottleneck of the rounding function of the NLM, lets consider the voltage distribution of the 400 capacitors presented in Figure 7.2[1]. The 400 cell voltages are inside the band defined by 1.6 kV ±10 % and they are balanced in accordance with the CTBsort approach. As the figure illustrates, from time t=1.3773 s to t=1.3774 s, 61 SMs reach the maximum limit (1.6 kV+10 %) and they are replaced by the 60 SMs with the lowest voltages with ≈ 1.4 kV. Since (7.1) do not consider the individual voltages of the capacitors, the correspondent stack suffers a variation of ≈ 23 kV, as illustrated in Figure 7.3(a). Therefore, under these circumstances, the real arm modulation index imposed by the CTBsort method does not satisfy the modulation index target m^*_{jk}. However, the converter control corrects this deviation as if it was a perturbation, as shown in Figure 7.3(b).

The voltage gap originated by the NLM can be understood as a perturbation from the MMC control perspective and it should be corrected. To address this goal the standard NLM approach depicted in Figure 7.4 was evolved to the procedure shown in Figure 7.5. If at the instant that N^*_{jk} is determined, the ranking list L of the cell selection method is known, the target number of inserted capacitors N^*_{jk} can be iteratively amended. To do so, it is determined an initial estimation number of capacitors to be inserted N_{jk} by the standard form of the NLM (1). Afterwards, at the adjust stage (2) (see Figure 7.5), the first N'_{jk} capac-

[1] These results were retrieved by the CTBsort cell selection method proposed in [95], which is later discussed in Section 7.2.3

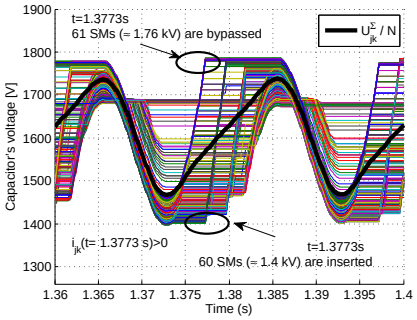
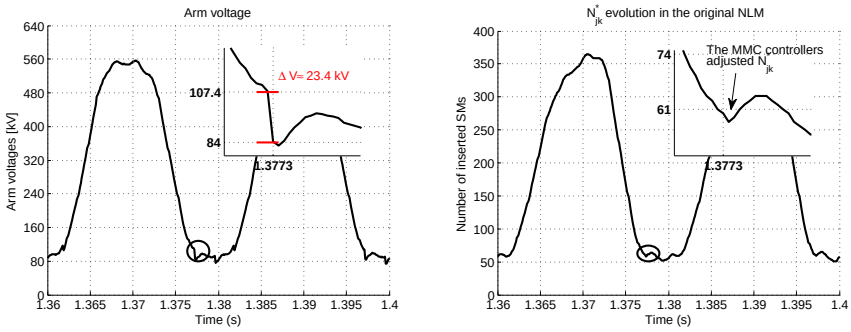


Figure 7.2: A tolerance band-based cell selection method.



(a) (b)

Figure 7.3: The NLM performance applied to a MMC with unequal voltage balance of the SMs: (a) arm voltages and (b) inserted capacitors.

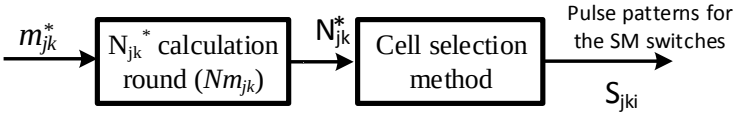


Figure 7.4: Original version of the NLM.

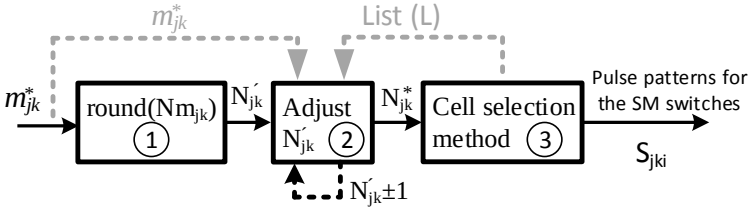
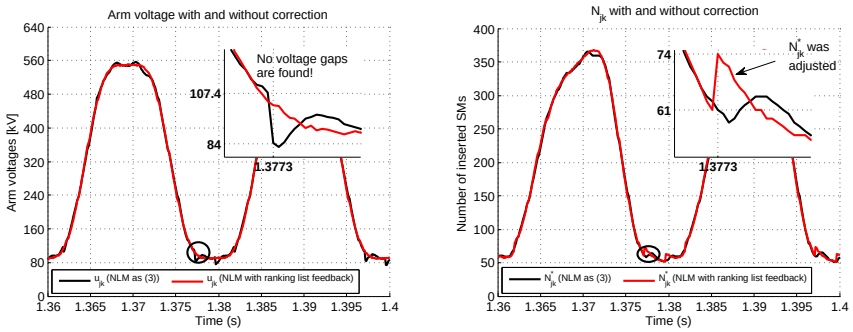


Figure 7.5: Block diagram of the iterative-based NLM.



(a) (b)

Figure 7.6: Iterative-based NLM impact on the converter arms modulation: (a) arm voltages and (b) number of inserted capacitors.

itors of the known list are added and the resultant modulation index (7.2) is compared to the modulation index target (input of the stage ①). Consequently, if the arm modulation index target is higher/lower than the retrieved by the first N'_{jk} capacitors of the list, N'_{jk} is incremented/decremented by one capacitor. This procedure is repeated until the target number of inserted capacitors is found that most approximate the arm voltage target and real values. The final value of N'_{jk} will became the final target number of cells inserted N^*_{jk}, which feeds the cell selection method stage ③. Other methods have been proposed to adjust N'_{jk} in order to minimize the perturbation imposed by the cell selection method on the converter control [161, 162].

$$m'_{jk} = \frac{\sum_{ii=1}^{N'_{jk}} U_{c_{jkL(ii)}}}{U^{\Sigma}_{jk}} \tag{7.2}$$

where ii is the index that crosses the sorting list L. $U_{c_{jkL(1)}}$ is the voltage of the first capacitor in the list.

The impact of adjusting the target number of inserted capacitors as an iterative-based NLM is illustrated by means of red curves in Figures 7.6(a) and 7.6(b). If the sorting list is considered at the time that N^*_{jk} is determined, once the SMs need to be rotated (the capacitor

hit the tolerance band) and in order to avoid a voltage gap on the arms (see Figure 7.6(a)), the inserted number of SM's target will be iterativelly upgraded. Thus, due to the adjustment of N^*_{jk}, it will have a discontinuity. As a result, the arm voltages and the consequent arm modulation indexes will not suffer any perturbation created by the cell selection method. Therefore, the usage of this iterative NLM-based method improves the performance of the converter control, whenever it is adopted an asymmetric energy distribution strategy for the stack SMs.

Several procedures to insert N^*_{jk} cells and the correspondent effects on the converter performance are discussed in the next section.

7.2 Cell selection methods for the MMC

7.2.1 Classical approach

The classical approach refers the methodology proposed in conjunction with the MMC in [43] to manage the states of the submodules. The capacitors of the SMs are progressively measured and the ranking list (L) is updated with the sampling frequency rate. Then, the N^*_{jk} most discharged/ charged capacitors are inserted when the arm current is positive/negative, energizing/de-energizing them, while the remaining ones are bypassed and their voltage remains unchanged. By repeating this procedure with the sampling frequency rate, the inserted capacitors will be regularly rotated. The average number of switching events are reduced if the active SMs are swapped only if the set-point N^*_{jk} changes its value [43].

7.2.2 Reduced switching frequency sorting method

The reduced switching frequency (RSF) cell selection algorithm was presented in [69]. In this strategy, the voltage of the capacitors are continuously measured and the sorting list is updated consonant the sampling frequency. The fact that differs from the previous method is the methodology for selecting the active cells. The reference number

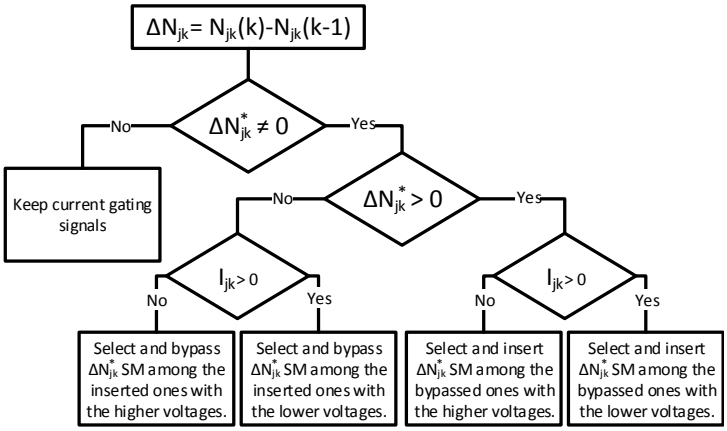


Figure 7.7: Overview of the RSF cell selection method.

of active cells determined at the instant k ($N^*_{jk}(k)$) is compared with the one calculated on the previous control cycle $k-1$ ($N^*_{jk}(k-1)$). The variation of the active number of SMs ($\Delta N^*_{jk}(k)$) (7.3) imposes the number of SMs that are changed between two consecutive time steps accordingly to Figure 7.7.

$$\Delta N^*_{jk}(k) = N^*_{jk}(k) - N^*_{jk}(k-1) \tag{7.3}$$

7.2.3 Fixed tolerance band and sorting method

The fixed tolerance band and sorting method (CTBsort) is characterized by progressively inserting the first N^*_{jk} capacitors of the sorting list. Although, the ranking list is only updated when an active SM hits the tolerance band limits defined by $V_{\max}/V_{\min}$ as pointed in Figure 7.8 [95]. As long as the voltage of an inserted capacitor is outside the tolerance band defined by $V_{\max}/V_{\min}$, the ranking list is continuously updated, which rotates more often the inserted capacitors.

The CTBsort is very interesting, besides limiting the voltage of the capacitors, it does not need to sort all the capacitors at each time step, which facilitates its implementation when compared to the previous methodologies presented.

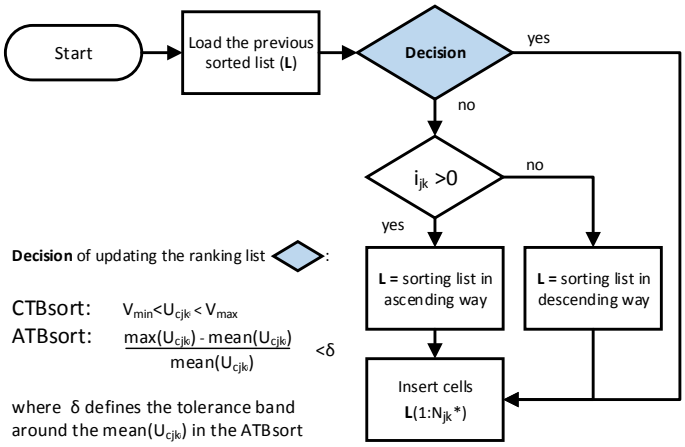


Figure 7.8: Overview of the CTBsort and ATBsort methods.

7.2.4 Tolerance band around the average voltage

The tolerance band around the average voltage sorting method (ATBsort) is similar to the CTBsort [95]. Likewise with the CTBsort, the sorting list in this method is amended whenever the voltage of one cell reaches the boundary imposed. In this strategy, the boundary is defined according to the capacitors voltage span in respect to the average voltage of the stack capacitors as illustrated in Figure 7.8. Since the decision of updating the ranking list is based on the deviation between the individual voltages of the capacitors and their mean voltage, it limits the voltage divergence between the capacitors within the same stack.

7.2.5 Hybrid modulation - fixed tolerance band

The hybrid fixed tolerance band sorting method (*HCTBsort*) is composed of the aggregation of the classic and RSF cell selection methods with the benefit of considering the voltage limitation of the capacitors. The capacitor voltages are continuously measured and ranked at each time interval. As long as, the capacitor voltages do not reach the imposed limit, the states S_{jki} computed by the RSF are applied to the converter switches, due to the fact that only allows the change of ΔN^*_{jk} cells. However, if at least one capacitor hits the boundary, the gating

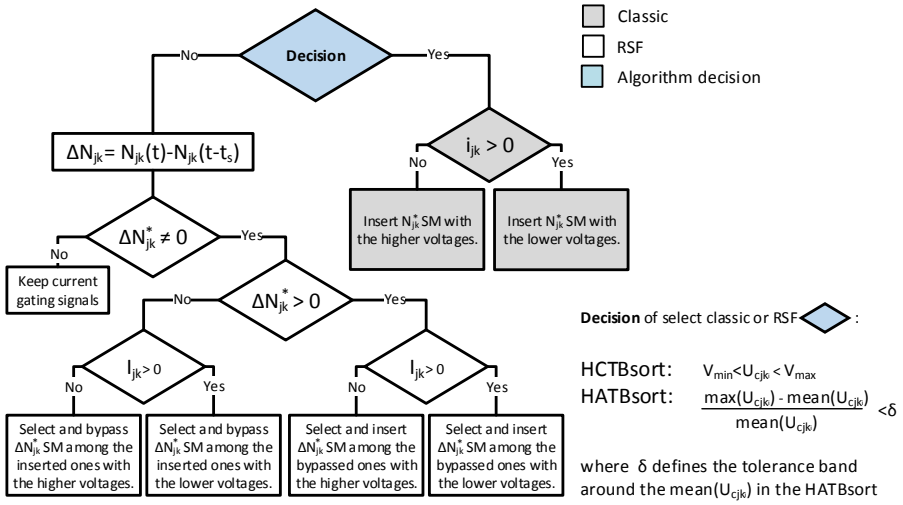


Figure 7.9: Overview of the HCTBsort and HATBsort methods.

signals calculated by the classic are applied instead, which automatically rotates the SMs that have their voltage limits violated. The HCTBsort scheme is shown in Figure 7.9.

7.2.6 Hybrid modulation - Tol. band around the average voltage

The hybrid modulation - tolerance band around the average voltage sorting method (HATBsort) is similar to the HCTBsort, being distinct on the algorithm decision stage. While the HCTBsort decides between the classic and the RSF methods according to the fixed voltage range limit $V_{\max}/V_{\min}$, the HATBsort varies between those methods by the relative voltage deviation of each capacitor to the average voltage of the cells. Hence, it has the same algorithm decision as the ATBsort.

7.3 Comparison of the cell selection methods

To evaluate the steady-state performance of the cell selection methods shown, the MMC's model was characterized by the parameters pre-

sented in Table 7.1. The methodologies presented to select the capacitors that are inserted on the converter stacks were equally applied to the six stacks and the correspondent performance was evaluated. However, due to the similarity of the results across the six stacks, only the results of the arm *aU* are depicted. To facilitate the analysis of those methods, the voltage generated and the correspondent current flow of the correspondent stack are presented in Figure 7.10.

Table 7.1: Circuit parameters used in simulation.

Parameters	Notation	Value
Number of submodules/arm	N	400
Rated active power	P	1.0 GW
Rated reactive power	Q	300 Mvar
Line voltage	U_{LL}	333 kV
dc-bus voltage	U_{dc}	± 320 kV
Cell capacitance (35 kJ/MW)	C	11.4 mF
Nominal submodule voltage	U_{nom}	1.6 kV
Arm inductance	L_{arm}	50 mH
Grid Inductance	L_{grid}	50 mH
Parasitic resistance of the inductors	R	0.1 Ω
Sampling frequency	f_s	10 kHz
IGBT device model	ABB 5SNA2000K450300	

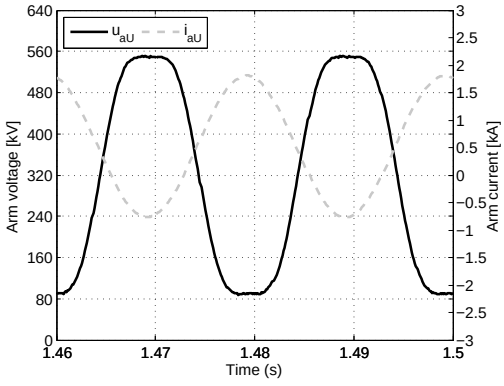


Figure 7.10: Nominal conditions of the arm *aU* voltage and current.

7.3.1 Individual analysis of the cell selection methods

As mentioned, the individual voltages of the capacitors greatly depend on the cell selection method adopted for the MMC. Therefore, in those methods that a tolerance band for the capacitor's voltages is embraced, their uppermost voltages are intrinsically defined. Therefore, to achieve a fair comparison between the methods, for those strategies, the limits of the tolerance bands were defined in such a way that the peak voltage across the capacitors will be equal. Thus, the peak voltage of the capacitors was defined to exceed by 10% their nominal voltage U_{nom}. In the following sections the results of each specific method are analyzed.

Classical modulation

The individual cell voltages of the MMC's stack respectively produced by the classic cell selection method are presented in Figure 7.11(a). Due to the fact that all the SMs were rotated every time that $\Delta N^*_{jk} \neq 0$, the capacitors become undoubtedly well balanced. In this case, since the voltage across each capacitor is approximately equal, the NLM (7.1) could be used without a significant degradation of the converter operation. As Figure 7.10 confirms, around the instant t=1.48s, the arm voltage is considerable flat and on this interval the N^*_{jk} is maintained slightly constant. Therefore, the fact of the number of inserted capacitors target is not frequently modified means that the capacitor's voltages slightly diverge around the referred instant.

The ripple magnitude of the capacitors at the nominal operating conditions is 8.1%, however, it comes with the cost of having a high switching frequency as emphasized in Figure 7.11(b). As the sorting list and the gating signals are frequently updated, the SM's switching frequency greatly depends on the number of SM available and the sampling frequency.

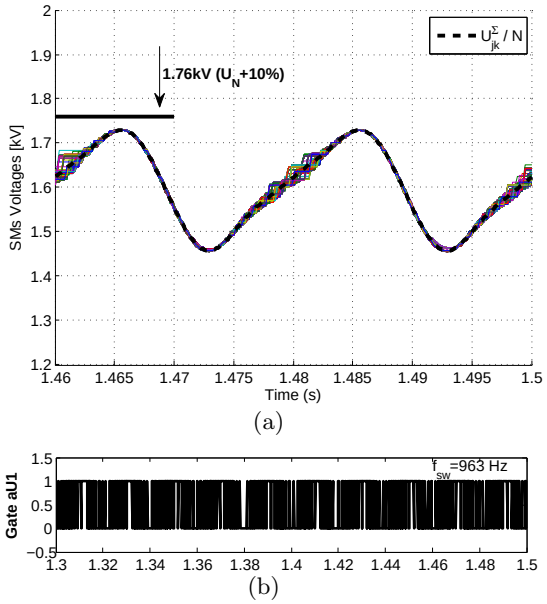


Figure 7.11: Performance of the classic sorting method: (a) capacitor voltages and (b) states of a particular cell.

Reduced switching frequency

The individual voltages motivated by the RSF method are illustrated in the Figure 7.12(a). Until t=0.4 s the classic modulation was calculating the gating signals of the IGBTs, being then swapped to the RSF. Due to the fact that the RSF is used with the NLM, where the N^*_{jk} is invariably increasing or decreasing (see Figure 7.6(b)), the SMs are obliged to be inserted over large periods, which greatly charges or discharges the corresponding cells. Hence, once the cells are inserted, will remain changeless for a long time period as shown in Figure 7.12(b), retrieving very low switching frequencies. Then, the inserted SMs greatly deviate from the ones that are bypassed and, since there is no limit imposed on the SM voltages, this strategy is incompatible with the presented nearest level modulation.

In the original proposal of the RSF in [69], the set-point for the active number of SMs N^*_{jk} was determined in a PWM-based procedure, and the ΔN^*_{jk} was progressively positive and negative, allowing the most

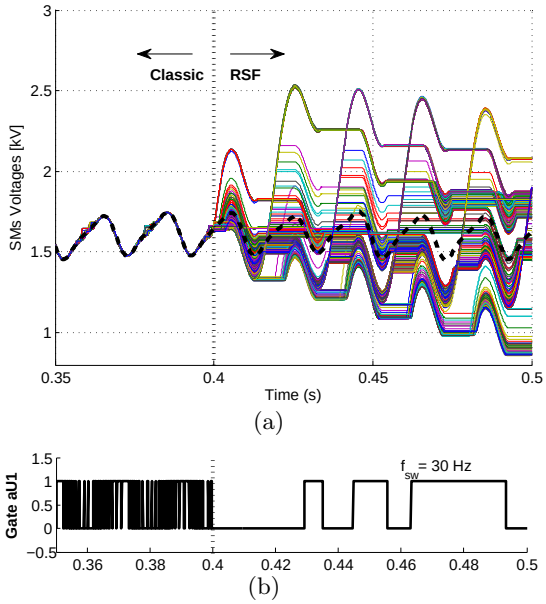


Figure 7.12: Performance of the RSF method: (a) capacitor voltages and (b) states of a particular cell.

charged and discharged cells to rotate. Then, in accordance with the results obtained, the aggregation between the RSF method with the NLM is concluded that is incompatible.

Fixed tolerance band sorting method

The performance of the CTBsort method with a tolerance band of $\pm 10\%$ of U_{nom} is illustrated in Figure 7.13. Due to the harmonic content on the SMs voltages, the uppermost and lowest peaks of the SMs average voltage are not symmetrically around U_{nom}. Hence, if a symmetrical band is adopted for the capacitors voltage limits, eventually, depending on the converter operating conditions, by the time that $\bar{U}_{c_{jki}}$ reaches one of its peaks, the capacitors will be subject of a higher rotation.

Particularly, on the operating conditions mentioned, at the instant t=1.4708 s, some of the inserted capacitors hit the lower limit and are then replaced. After some control cycles, at t=1.4714 s, few active SMs also reach the lower band limit and, no "violated" capacitors are

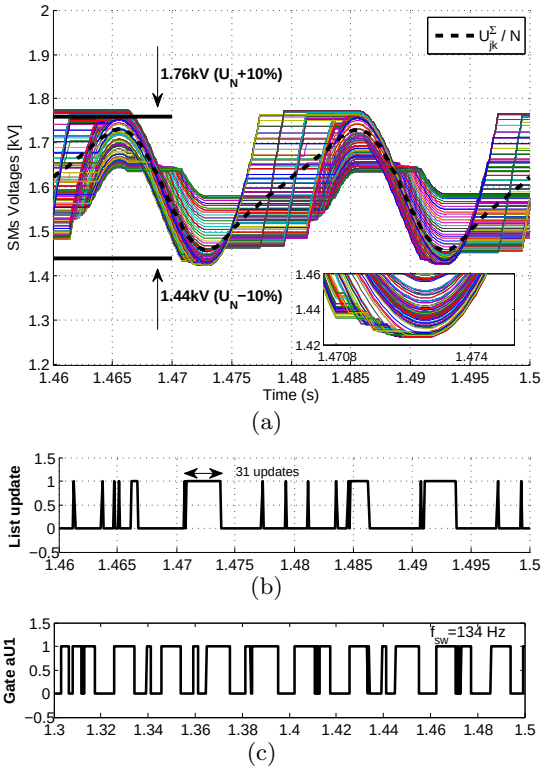


Figure 7.13: Performance of the CTBsort method: (a) capacitor voltages, (b) time instants when the ranking list was updated and (c) states of a particular cell.

available. Under these circumstances the sorting list is continuously updated, which will rotate the violated capacitors at each time step until this violation is vanished (t= 1.4737s), as emphasized in Figure 7.13(b) and Figure 7.13(c).

Moreover, when compared to the previous algorithms, the sorting list of the CTBsort method is updated fewer times, which contributes to a considerable small switching events in Figure 7.13(c). Furthermore, this method also takes advantage of the technical limits of the capacitor voltages since they are widely distributed within the tolerance band, in contrast to the classic method, which are very concentrated.

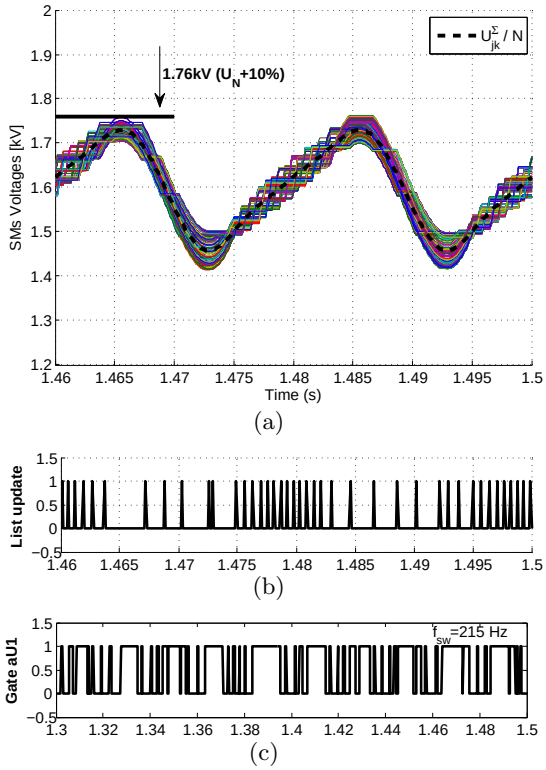


Figure 7.14: Performance of the ATBsort method: (a) capacitor voltages, (b) time instants when the ranking list was updated and (c) states of a particular cell.

Tolerance band around the average voltage

As previously argued, the sorting list is updated whenever a capacitor voltage deviates more than the allowed range defined in respect to its mean voltage (U_{jk}^{Σ}/N), as illustrated in Figure 7.14. Considering that the power flow conditions contributes to a voltage ripple of 8.1% in U_{jk}^{Σ}/N (value obtained with the classic sorting), a 1.9% voltage range was considered around $\bar{U}_{\mathrm{c}_{jki}}$, to fulfill the upper bound mentioned of 10%. For the reason that the admissible band around $\bar{U}_{\mathrm{c}_{jki}}$ is short, the capacitor voltages are satisfactorily together.

Although the voltage peak of the capacitors was set to 10% for the CTBsort and ATBsort, the number of rotations in the last approach

is much higher. So, it does not explore the capacitor voltage limits like the CTBsort. Since the tolerance band is relatively low, on the instants that the arm current reaches its maximum peak (for instance at t≈1.48 s), there is a higher concentration of list update "flags" in Figure 7.14(b), when compared to the minimum current peak instant (for instance at t≈1.49 s).

This method inflicts the switching events of Figure 7.14(c) to the SM *aU1*. According to what has been argued, obviously, this method has a higher switching frequency than the CTBsort.

Hybrid modulation - fixed tolerance band

For the presented conditions, the individual voltages of the capacitors when guided by the HCTBsort method are presented in Figure 7.15. The capacitor voltages are very similar to the ones led by the CTBsort method. However, by either imposing gating signals S_{jki} calculated by the classic or the RSF methods in consequence to the capacitor ripple voltage, not only the SM voltages are below the 10% band, but as as shown in Figure 7.15(b), it also reduces the SMs average switching frequency of the semiconductors due to the progressive update of the sorting list.

In opposition to CTBsort, this method is more arduous to be implemented because, besides computing the gating signals of two sorting algorithms at each time step, it continuously updates the sorting list which requires substantial computational effort. At nominal conditions, it retrieves slightly fewer switching events than on the CTBsort method.

Hybrid modulation - Tol. band around the average voltage

The individual voltages of the capacitor when guided by the HATBsort method are presented in Figure 7.16. This method provides similar results to the ATBsort, albeit with a slightly reduction on the average switching frequency of the SMs. This fact occurs because, by adopting a method that continuously updates the sorting list as well as in the HCTBsort method, unnecessary switching events are avoided. This al-

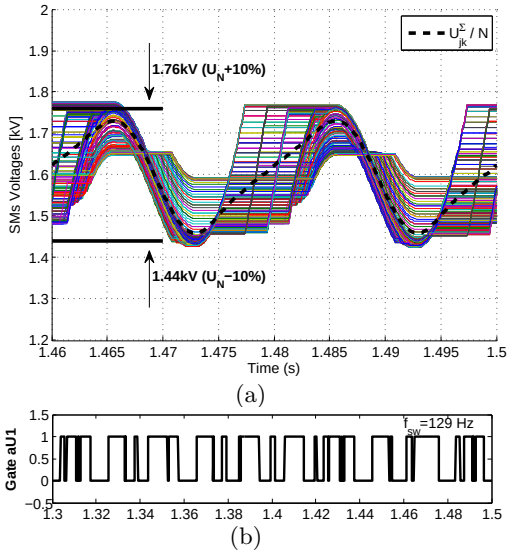


Figure 7.15: Performance of the HCTBsort method: (a) capacitor voltages and (b) states of a particular cell.

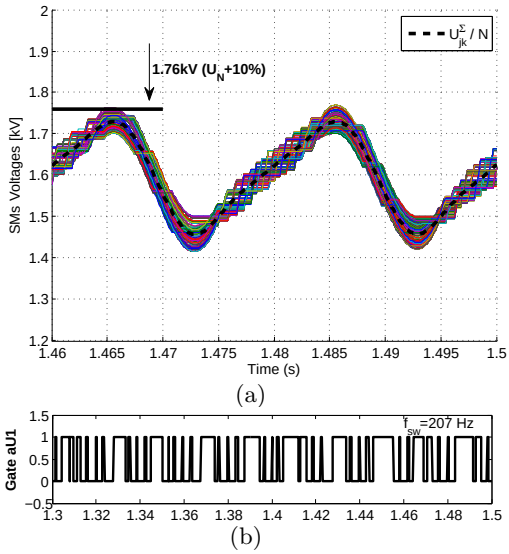


Figure 7.16: Performance of the HATBsort method: (a) capacitor voltages and (b) states of a particular cell.

Table 7.2: Performance of the cell selection methods at nominal conditions.

Method	Classic	RSF	CTBsort	ATBsort	HCTBsort	HATBsort
Switching frequency	963 Hz	30 Hz	134 Hz	215 Hz	129 Hz	207 Hz
Switching losses	14.1 MW	not appl.	1.74 MW	4.25 MW	1.69 MW	4.21 MW
Capacitor voltage ripple	8.1%	>10%	10%	10%	10%	10%
Exploitation of permissible limits of capacitors	Low	not appl.	High	Medium	High	Medium
Hardware implementation	High	High	Medium	Medium	High	High

gorithm has the disadvantage, as does the HCTBsort, of continuously updating the sorting list which is challenging to implement whenever it comes to a HVdc-based project with hundreds of SMs stacked.

7.3.2 Comparison of the cell selection methods performance at nominal conditions

For each method, the power dissipated on the switching events was computed [155]. The results achieved are summarized in the Table 7.2.

The classic approach is the one that most reduces the voltage ripple of the capacitors due to its imposed intrinsic high switching frequency. On the other hand, the HCTBsort is the one that most reduces the switching events of the SMs and is also the most efficient. Regarding the Hybrid-ATBsort, it slightly increases the efficiency of the ATBsort method.

As previously discussed, the aggregation between the RSF and the NLM is not compatible since it leads to very low switching events. As a result, the RSF leads to the dispersion of the capacitor voltages to critical values.

The methods that progressively sort the capacitors voltages, namely the classic, RSF and the hybrid, were considered to be more difficult to implement in real HVdc applications than the ones that update the sorting list few times over the grid cycle (CTBsort and ATBsort). Despite being complex to implement, the HCTBsort is expected to reduce the power dissipated of the commutations in comparison with the CTBsort.

Finally, the election of the most suitable cell selection method depends on the parameter needing optimization. In this vision, it is a

trade-off between the voltage limits of the capacitors, hardware implementation complexity and switching frequency that directly influences the converter efficiency.

7.3.3 Comparison of the cell selection methods performance for different reactive power flow scenarios

In this section the presented cell selection methods were analyzed for different power flow conditions. The reactive power flow was varied from 0 to 300 Mvar, despite the fact of the active power flow was maintained at its nominal conditions. The modification of the reactive power flow establishes a different harmonic magnitude and content on $\bar{U}_{c_{jki}}$, which varies the peak voltage of the capacitor's ripple and the average switching frequency, as shown in Figure 7.17 for the classic sorting method. As expected, the classic cell selection method continues to compute a large number of switching instants. Moreover, the capacitor's ripple magnitude at each reactive power condition was used to adjust the tolerance band of the HATBsort and ATBsort methods. The remaining cell selection methods were then analyzed and the correspondent results are displayed in Figure 7.18. It can be seen that the hybrid methods can slightly reduce the switching frequency of the SMs when it comes to the CTBsort and ATBsort methods respectively. The switching frequency reduction established with the HATBsort in comparison to the ATBsort is residual. In opposition, as depicted in Figure 7.19, the Hybrid-CTBsort method can reduce the switching losses up to 14% when it comes to the CTBsort method.

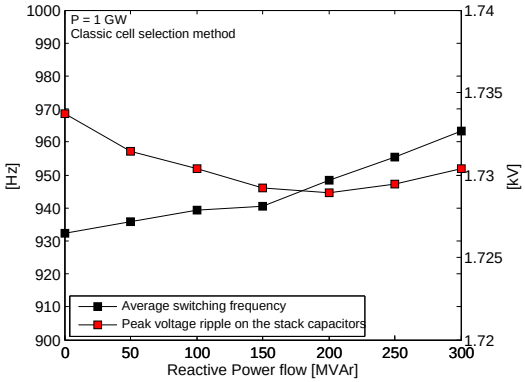


Figure 7.17: Reactive power flow impact on the MMC's switching frequency (classic sorting).

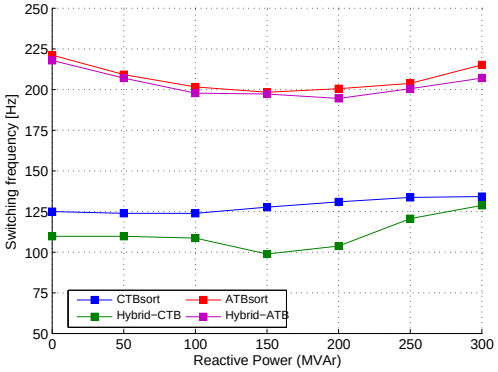


Figure 7.18: Average switching frequency of the SMs vs. the reactive power flow for the presented cell selection methods.

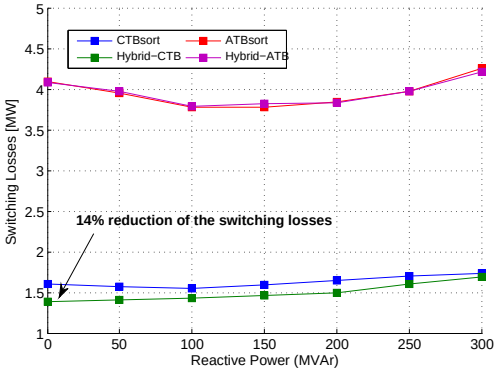


Figure 7.19: Reactive power flow impact on the MMC's switching losses.

7.4 Conclusions

The modular multilevel converter efficiency is strongly affected by the methodology adopted to select the capacitors to be inserted in the converter stacks. Several methods are present in the literature, and each one has specific features and advantages. However, the procedure adopted to select one particular method depends on the parameter that is required to be optimized, such as the voltage ripple magnitude, the average switching frequency, converter efficiency and hardware implementation complexity.

At nominal conditions, the denominated classic approach minimizes the voltage ripple of the capacitors to 8.1% with the cost of a substantial switching frequency ($\approx$ 960 Hz) and high power losses ($\approx$ 14 MW). On the other hand, at nominal conditions, if the magnitude of the capacitor's voltage ripple equal to 10% is imposed, the Hybrid-CTBsort is the one that most curtails the switching events and losses. It is responsible for the average switching frequency for the SMs of 129 Hz and the inherent switching losses of 1.69 MW. Nonetheless, this last approach results from a combination of two cell selection methods and at each time step continuously sorts the voltages of the capacitors which is expected to be difficult to implement on a HVdc-based converter with hundreds of SMs. Finally, the CTBsort ranks the voltages of the capacitors only a few times per grid cycle, which facilitates its hardware implementation but generates more switching events and losses than the Hybrid-CTBsort method.

Several reactive power flow scenarios were taken into account in to study the performance of the presented methods. Moreover, the Hybrid-CTBsort and Hybrid-ATBsort obliges less switching occurrences than the CTBsort and ATBsort respectively. Furthermore, the HCTBsort method can reduce up to 14% of the switching losses produced by the CTBsort method.

Chapter 8

Analysis of the power dissipated by the semiconductors

Over the past years, an increase in worldwide energy demand and the expansion of the transmission networks has been witnessed, putting the security of energy supply to consumers at risk. These premises are some of many foundations that are driving the research in a broad range of electrical engineering fields, namely in the energy generation and transmission sectors. Taking those factors into account, high-voltage dc (HVdc) transmission is being pointed as one possible key-point breakthrough.

A transversal research topic to the current VSC-HVdc solution is to identify its efficiency. As introduced in Chapter 2, there are several SM schemes that can be applied to the MMC which have different characteristics regarding their efficiency. There are qualitative and quantitative assessments that characterize the efficiency of each SM structure [24,44]. The emphasis goes to the half-bridge SM structure, which is the most efficient and straightforward solution [60]. For that reason, it is the submodule structure that is mostly selected to investigate the losses generated by the MMC [68, 157, 163]. References [157, 163] estimate the converter power losses at its nominal power flow conditions. Furthermore, in [163] the converter efficiency whenever the capacitors are rotated by means of different strategies is also assessed. On the other hand, the MMC efficiency is also analyzed for different power factors in [68]. The author studies the impact of the power factor on the converter losses, particularly with unity- or zero-power factor conditions.

Consequently, the converter only exchanges either active or reactive power with its ac grid. Thus, according to the work already done on the converter efficiency, there is a lack of information on values beyond the nominal. Adding the fact that the multi-terminal onshore and offshore dc grids schemes are a reality for power transmission [57, 58, 164–166], the overall efficiency of the those grids has a relevant impact from the converter insight, whose efficiency varies according to its load. Besides the analysis of the ac power flow impact on the converter efficiency, the goal of this work is to provide a methodology that can be followed to deduce a mathematical model that can describe the semiconductor power losses of a grid-tied MMC. As a result, the mathematical model deduced in this chapter can be directly adopted in optimal power flow (OPF) studies.

Two expressions are deduced describing the converter efficiency behavior under different operation modes. The first model describes MMC efficiency when it operates within its active power limits with unity power factor and, in addition, the converter efficiency is also adjustable in accordance with the average switching frequency selected for the converter. The second part focuses on the converter efficiency when it exchanges active and reactive power with the electrical grid, but in a fixed switching frequency-based scenario.

To perform the tasks referred to, the methodology presented in Section 5.3.1 was embraced to analyze the efficiency of the HVdc-based design. Therefore, since it was considered a more suitable semiconductor model to complete this study, its features are presented in Section 8.1. Then, the ac grid power injection impact on the on-state losses of the MMC semiconductors is analyzed in Section 8.2. Consequently, the mathematical model of the semiconductor's power losses is deduced in Section 8.3. The final remarks of the chapter are summarized in Section 8.4.

8.1 Semiconductors features

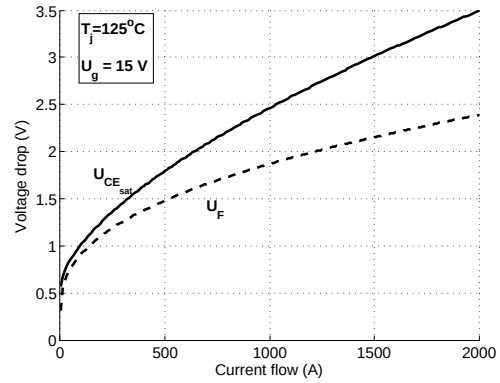
Several methods to estimate the semiconductors power losses have been proposed in the literature [155, 167–170]. The methodology followed in the thesis was proposed by the MMC's manufacturer Siemens AG [155] and it has been widely used since then [68, 69, 160, 171]. As explained in Section 5.3.1, the referred method estimates the semiconductor power losses as a consequence of the simulation results in which the semiconductors are modeled as ideal switches [155].

The quantification of the losses generated is dependent on the semiconductor device adopted. Hence, by admitting the INELFE system parameters presented in the Appendix A, the nominal voltage of the capacitors would be 1.76 kV, which fluctuate $\approx \pm 10\%$ at nominal power conditions. Adding the fact that the MMC arms can operate with less than the 400 cells[1], it was considered that the MMC would be sufficiently robust if composed of 4.5 kV blocking voltage-based IGBTs. Therefore, the state of the art semiconductor model ABB-5SNA2000K450300 (4.5 kV /2 kA device) seems to be a viable option to quantify the losses generated by the MMC case study [87]. The methodology presented in Section 5.3.1 is complemented with the semiconductor module parameters described in Section 8.1.1 and Section 8.1.2.

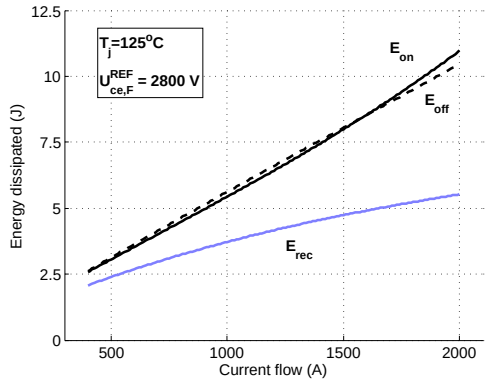
8.1.1 On-state features

The methodology followed to estimate the on-state losses of the converter was explained in Section 5.3.1. However, concerning the features of the semiconductor module used, the non-linear relation between voltage drop of semiconductor devices and their guided current, were fitted from the device's catalog. Then, the saturation voltage of the IGBT $U_{ce_{sat}}(i_{_{CE}})$ and the forward voltage drop of its anti-parallel

[1] If a failure occurs in a particular cell and, is consequently bypassed by the mechanical switch, the energy that it stores is divided by the remaining cells of the correspondent stack [172]. In this vision, the cells should be able to operate with voltage values slightly higher than the nominal.



(a)



(b)

Figure 8.1: ABB-5SNA2000K450300 semiconductor model features: (a) on-state voltage drop and (b) energy dissipated in a switching event.

diode $U_F(i_{_F})$, are represented in (8.1), and illustrated in Figure 8.1(a).

$$U(i) = a + b\ i^c \Rightarrow \begin{cases} U_{ce_{sat}}(i_{CE}) = 0.568 + 0.02497\,(i_{CE})^{\,0.6267} \\ U_F(i_{_F}) = 0.313 + 0.08916\,(i_{_F})^{\,0.414} \end{cases} \quad (V) \tag{8.1}$$

8.1.2 Switching features

The strategy followed to estimate the semiconductor's power losses during the commutation events was replicated from the one presented in Section 5.3.1. The energy lost during a commutation event of the 4.5 kV semiconductor was represented by the nonlinear relation with the electrical current as (8.2), and illustrated in Figure 8.1(b).

$$E(i) = a + b\ i + c\ i^2 + d\ i^3 \Rightarrow \begin{cases} E_{on}^{U_{CE}=2.8kV}(i_{_{CE}}) = (3.527\text{e-}10)i_{CE}^3 \\ \qquad\qquad\qquad\qquad - (7.152\text{e-}7)i_{CE}^2 \\ \qquad\qquad\qquad\qquad + (5.216\text{e-}3)i_{CE} \\ \qquad\qquad\qquad\qquad + 0.5816 \\ E_{off}^{U_{CE}=2.8kV}(i_{_{CE}}) = (7.237\text{e-}11)i_{CE}^3 \\ \qquad\qquad\qquad\qquad - (3.473\text{e-}7)i_{CE}^2 \\ \qquad\qquad\qquad\qquad + (5.383\text{e-}3)i_{CE} \\ \qquad\qquad\qquad\qquad + 0.5118 \\ E_{rec}^{U_F=2.8kV}(i_{_F}) = (1.231\text{e-}10)i_F^3 \\ \qquad\qquad\qquad\qquad - (1.008\text{e-}6)i_F^2 \\ \qquad\qquad\qquad\qquad + (3.965\text{e-}3)i_F \\ \qquad\qquad\qquad\qquad + 0.6427 \end{cases} \tag{8.2}$$

where (i_{CE}, i_F) pair is the collector-emitter current of the IGBT and diode at the moment of the commutation. ($E_{on}^{2.8\text{kV}}$, $E_{off}^{2.8\text{kV}}$) pair is the energy dissipated on the turn-on and -off event of an IGBT which have 2.8 kV across its terminals. $E_{rec}^{2.8\text{kV}}$ is the energy dissipated on a turn-off event of a diode which have 2.8 kV across its terminals.

As proposed in [155], the energy lost during the commutation event is linearly adjusted from the device's reference data in respect to the real voltage across the semiconductors terminals at the switching instant.

8.2 Impact of the power factor on the on-state semiconductors

As the active and reactive power flows at the PCC varies in respect to the *emf* of the MMC, the correspondent arm voltages and the semiconductors that are active and transporting the arm current are respectively influenced. Focusing on the operation of one half-bridge cell, the combination between its state S_{jki} and the electrical current flow i_{jk} defines which semiconductor device is active. Whenever a capacitor is inserted in the arm current path (S_{jki}= 1), it will be charged (current flow in the $S_{1_{jki}}$-diode) or discharged (current flow in the $S_{1_{jki}}$-IGBT) according to the positive or negative direction of the arm current. On the other hand, whenever the SM capacitor is bypassed, the electrical current with the positive (negative) direction flows on the IGBT (diode). Therefore, in accordance with the semiconductor's gating signals, the number of active (N_{jk}^{on}) and bypassed (N_{jk}^{off}) cells is obtained as (8.3) and (8.4) respectively.

$$N_{jk}^{on}(t) = \sum_{i=1}^{N} S_{jki} \tag{8.3}$$

$$N_{jk}^{off}(t) = \left(N - N_{jk}^{on}(t)\right) \tag{8.4}$$

Once identified the number of on-state semiconductor devices, identifying which is the semiconductor conducting the arm current is required, namely the IGBT or diode placed on the upper or lower switch of the HBSM. To do so, it is necessary to observe the arm current direction and, thus, the logical variable $sign^{+}$ (8.5) and $sign^{-}$ (8.6) is also defined according to the correspondent current flow direction on the jk arm.

$$sign_{i_{jk}}^{+}(t) = \begin{cases} 1 & i_{jk} > 0 \\ 0 & i_{jk} \leq 0 \end{cases} \tag{8.5}$$

$$sign_{i_{jk}}^{-}(t) = \overline{sign_{i_{jk}}^{+}}(t) = \begin{cases} 1 & i_{jk} < 0 \\ 0 & i_{jk} \geq 0 \end{cases} \tag{8.6}$$

Once defined the number of active cells and the correspondent arm current direction, the expression with the number of on-state diodes (N_{jk}^{D}) and on-state IGBTs (N_{jk}^{I}) are directly obtained as (8.7) and (8.8) respectively.

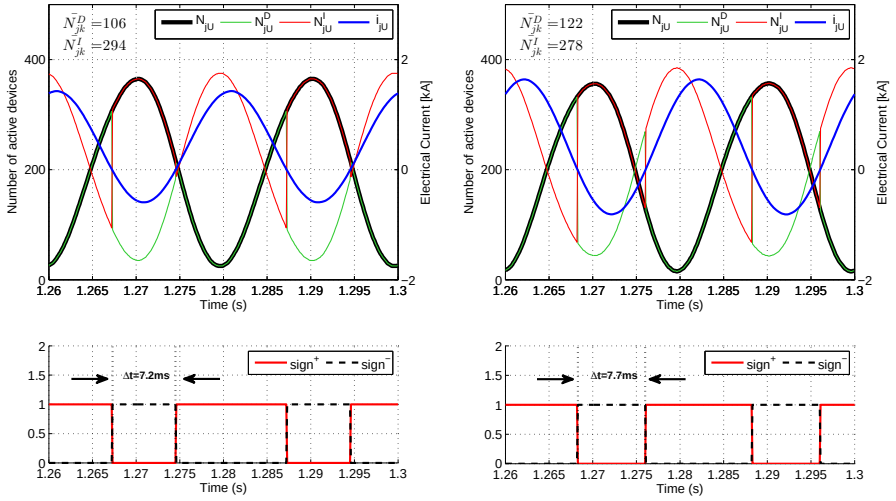
$$N_{jk}^{D}(t) = N_{jk}^{on}(t) sign_{i_{jk}}^{+}(t) + N_{jk}^{off}(t) \overline{sign_{i_{jk}}^{+}}(t) \tag{8.7}$$

$$N_{jk}^{I}(t) = N_{jk}^{off}(t) sign_{i_{jk}}^{+}(t) + N_{jk}^{on} \overline{sign_{i_{jk}}^{+}}(t) \tag{8.8}$$

Considering a MMC tied to a very strong grid, as a result of a small adjustment of the converter *emf* e_j leads to a considerable transformation in the electrical current (magnitude and phase). Thus, the arm modulation index, the arm current flow and consequently the number of conducting semiconductors are accordingly affected, as shown in Figure 8.2. An almost negligible change in the magnitude and phase on the arm modulation index significantly changes the reactive power flow on the PCC. As can be seen, the 400 Mvar increase shifts the $sign^{+}$ signal and increases its duty cycle[2] due to the ac current magnitude increase. After specifying the corresponding number of IGBTs and diodes that are inserted, accordingly coded in red and green, it is evident that their ratio varies over time. However, the total number of inserted devices is always equal to 400, i.e. the number of SMs available in each converter arm. As depicted, the average number of inserted diodes and IGBTs varies in the two presented scenarios. In the scenario presented in Figure 8.2(a), the average number of inserted diodes and IGBTs was respectively 106 and 294 units. In contrast, when the reactive power injection was increased (see Figure 8.2(b)), the average number of inserted diodes and IGBTs was respectively affected and changed to 122 and 278 units.

Therefore, the active and reactive power flow between the converter and its ac grid affects the ratio of diodes/IGBTs that are conducting and, hence, it influences the converter efficiency. The methodology adopted for determining the on-state losses of the IGBTs and diodes

[2]Ratio between the time width of the logical level *high* and the period of the signal.



(a) (b)

Figure 8.2: Impact of the power flow conditions on the on-state semiconductor devices for P=800 MW and: (a) Q= 200 Mvar (ind.) or (b) Q= 600 Mvar (ind.).

was already introduced in Section 5.3.1 [155]. The parameters used for the MMC were according to the INELFE project, which are presented in Appendix A.

First, the converter was examined for the four quadrants of operation, namely for the inverter and rectifier modes, as well as for the leading and lagging power factor conditions. The on-state losses produced in the diodes (P^D_{cond}) and IGBTs (P^T_{cond}) for the four quadrants and at the selected ac power flow conditions are presented in Figure 8.3.

The most evident fact is that the MMC generates fewer losses on the rectifier operating mode. This occurs because in the rectifier mode (power quadrants 2 and 3), the arm currents flow mainly on the diodes, which present smaller on-state voltage drops than the IGBTs. During the inverter operation mode (power quadrants 1 and 4), the most stressed devices are the IGBTs and therefore, on these power conditions, more losses are expected.

In the results depicted, the ratio between the active and reactive

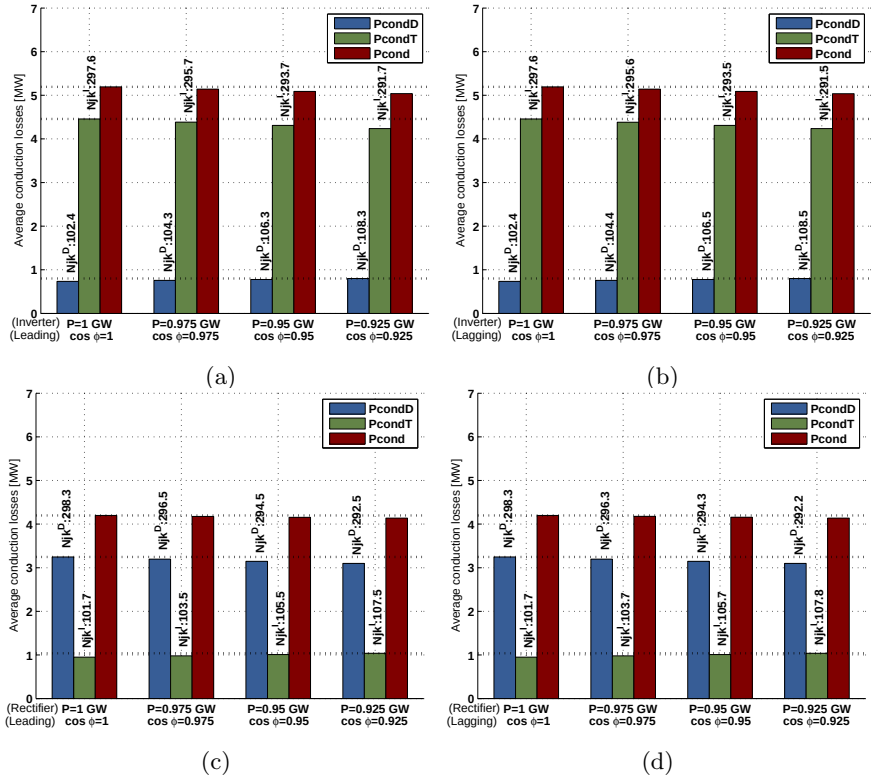


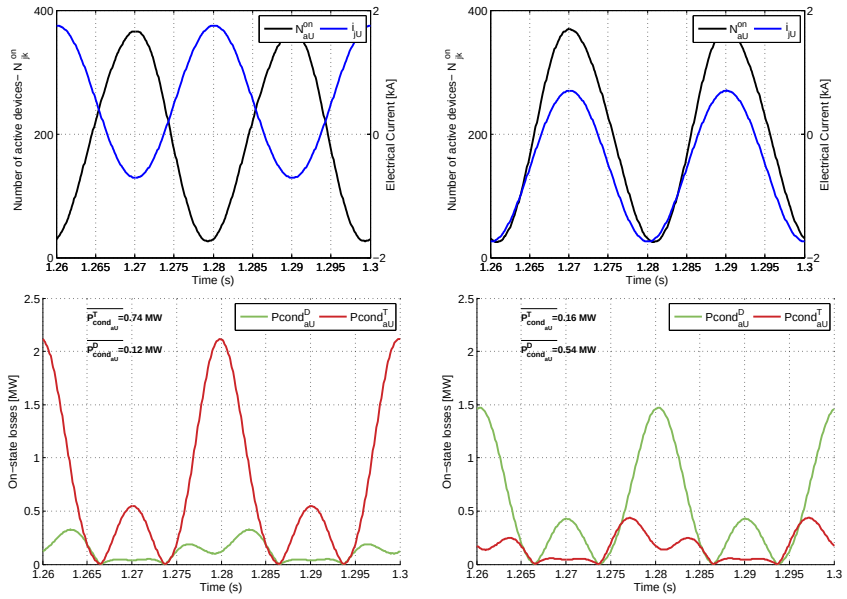
Figure 8.3: Average on-state losses of the MMC's semiconductors in: (a) inverter mode/ power factor (leading), (b) inverter mode/ power factor (lagging), (c) rectifier mode/ power factor (leading) and (d) rectifier mode/ power factor (lagging).

power flow injection is being decreased, whereas the apparent power is constant. The reduction of the active power flow between the converter and its ac grid accordingly reduces the ac and dc currents that flow on the converter arms. Therefore, it accordingly reduces the overall conducting losses that are being generated. Thus, regardless of which power quadrant that the MMC is operating, the reduction of the power flow injection into the ac grid leads to lower conducting losses on the semiconductors.

Focusing on the inverter (rectifier) mode of operation, as the active power is being increased, the average number of on-state IGBTs (diodes)

is also being increased over the number of inserted diodes (IGBTs). On the other hand, if the nature of the power factors is analyzed, in terms of the on-state losses, the lagging power factors retrieve residual less power losses than the leading ones, since the number of inserted devices N_{jk}^{on} is marginally lower.

Specifically, by analyzing the cell's insertion index in one converter arm and the correspondent arm current flow it can be further deduced what is the semiconductor's nature that is more stressed inside the half-bridge cells. Let's focus on the stack aU operation in power quadrants 1 and 2, which is presented in Figure 8.4.



(a) (b)

Figure 8.4: On-state losses of the arm aU whenever the converter is: (a) delivering or (b) absorbing 1 GW from the grid ($\cos\phi$=1).

In accordance with the results, regardless of the power flow direction to the electrical grid, the instant that more power is being dissipated on the MMC semiconductors occurs when the arm current reaches its peak value. Therefore, in the presented scenarios, the arm current reaches its

absolute peak value at approximately the same instant that the cell's insertion indexes reach they minimum value. This means that during the instant that most of the cells are bypassed, they are crossed by the absolute peak current (instants 1.26 s, 1.28 s and 1.3 s of Figure 8.4). Thus, the absolute peak current flows mainly on the lower switches of the half-bridge cells. Therefore, as presented on the lower part of Figure 8.4, whenever the converter is operating at steady-state and in the inverter or rectifier modes, the switch $S_{2_{jki}}$ (lower switch of the HBSM) is the most stressed device and it is contributing to the power dissipation peak of the correspondent arm ($\approx$ 2.1 MW/ $\approx$ 1.5 MW during the inverter/ rectifier mode respectively).

On the other hand, if the second arm current peak (instants 1.27 s and 1.29 s in Figure 8.4) is taken into account, regardless of the power flow direction, the second power dissipation peak is mainly generated on the upper switches of the HBSM. The second highest power loss peak is several times lower than the first, which demonstrates that there is a great power loss asymmetry over the SM's upper/lower switches. This fact can be relevant for the MMC's manufacturers because it can be technically and economically more attractive the use of two different semiconductor types for the lower and upper switches of the converter.

8.3 Semiconductors power losses model for HVdc applications

Since the MMC is composed of individual elements connected in series, the number of active cells N_{jk} in a given instant depends on the reference created by the converter control method N^*_{jk}. Thus, it can be said that the number of devices in series at a particular time does not depend on cell selection method, as long as the adopted method is capable of inserting the required number of SMs in the chain (8.9). So, if at each particular operating point (8.9) is verified, the number of semiconductors in the on-state mode will remain equal for any strategy adopted to select the cells, quantifying then the same on-state losses.

$$N^*_{jk}(t) = N_{jk}(t) \tag{8.9}$$

Several selective control algorithms of the cells have been proposed in the literature with different characteristics [43, 95, 160, 173]. The reference [163] presents and experimentally validates the selection strategy named CTBsort which balances the energy of the stack cells and maintains the correspondent voltages below the imposed limits. Due to its promising performance, the CTBsort cell selection method was adopted for this study. In this method, as introduced in Section 7.2.3, as long as the capacitor voltages $U_{c_{jki}}$ remain inside the voltage range defined by V_{max} and V_{min} (8.10), the sorted list L of capacitor voltages is not updated [163].

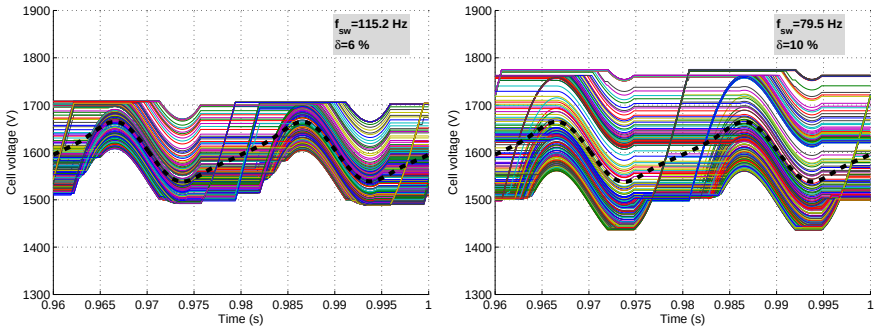
$$\begin{cases} V_{max} = (1+\delta)U_{nom} \\ V_{min} = (1-\delta)U_{nom} \end{cases} \tag{8.10}$$

where δ is a constant that defines the voltage band around the capacitor's nominal voltage U_{nom}.

Once at least one cell hits the voltage limits defined by V_{max} and V_{min}, the ranking list of the correspondent stack is updated in the ascending/descending order in case that the arm current is positive/negative. As a consequence, once the capacitors that have their voltage limits violated[3], they will be forced to swap [163]. As the voltage range defined by δ becomes smaller, more often the capacitor voltages reach their limits and, as a result, the cells are more often replaced. So, it is concluded that the voltage range defined by δ directly impacts the MMC switching frequency.

From the variation of the capacitor voltage limits δ and the corresponding power conditions of the MMC, two mathematical models representative of the semiconductor losses were deduced. The first model is capable of predicting the semiconductor's model as a function of the active power flow and the switching frequency of the converter (unity power factor). Consequently, the second model is characterized by estimating the semiconductor's power losses whenever the converter is exchanging active and reactive power with the electrical grid, but with a fixed switching frequency. On the MMC-HVdc-based applications,

[3]The voltage limits V_{max} and V_{min} are defined in accordance with δ (8.10).



(a) (b)

Figure 8.5: CTBsort tolerance band impact on the average switching frequency of the cells for: (a) 6% and (b) 10%.

typically the average switching frequency varies around 150 Hz due to semiconductor limits and practical limitations [44, 49, 69, 174]. Therefore, as will be reinforced later, the capacitor voltage limits were varied by means of δ, in order to achieve this fixed commutation ratio. Depending on the MMC operating conditions, the proper losses model should be selected.

The procedure used to deduce a generic expression that can represent the converter losses was structured in three distinct stages. The first stage is characterized by simulating and recording the outcome data, considering the converter operation with ideal switches inside the cells. This stage is further explained in Section 8.3.1. Consequently, the acknowledged data was used to calculate the semiconductors generated losses in offline mode. The methodology adopted to estimate the semiconductor's power losses was presented in Chapter 5 and it was complemented with the details of the semiconductor device in Section 8.1. Finally, the inference of the first and second mathematical models are respectively accomplished in Section 8.3.2 and Section 8.3.3.

8.3.1 Data extraction

The point-to-point HVdc transmission line of the INELFE project [47, 93], illustrated in Figure 8.6, was embraced in this work to as-

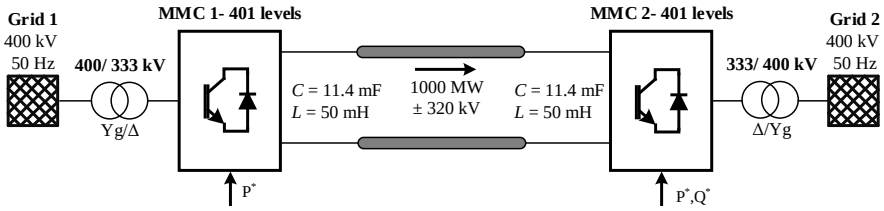


Figure 8.6: MMC-HVdc transmission system scenario for efficiency analysis.

sess the MMC efficiency. The two HVdc-link terminals have the same characteristics presented in the Table 8.1, however, they are differently controlled. The MMC-1 terminal was controlled as a current source which injects/absorbs into/from the dc transmission line a constant power, according to the pre-defined reference P^*_{MMC-1}. In its turn, the MMC 2 manages the active power flow at PCC to guarantee the voltage at the dc transmission line equal to its nominal value, as well as, the nominal energy storage on the converter stacks. Moreover, MMC-2 is able to control the reactive power that flows between the converter and the network 2, as a consequence of the desired set-point Q^*_{MMC-2}. By handling the active and reactive power flow references in both HVdc terminals with the control scheme presented in the Chapter 3, the efficiency of the MMC-2 was analyzed in two independent situations. First, the set point Q^*_{MMC-2} was left equal to zero, whereas P^*_{MMC-1} and δ were being changed, as will be discussed in section 8.4.1.a. On the next case study, explained in section 8.4.1.b, the voltage limits of the sorting algorithm were varied in order to find, for each combination of P^*_{MMC-1} and Q^*_{MMC-2}, the average switching frequency of 150 Hz, as previously mentioned.

Table 8.1: Circuit Parameters used in simulation

Parameters	Notation	Value
Number of submodules/arm	N	400
Rated apparent power	S	1.0 GVA
Line voltage	U_{LL}	333 kV
dc-bus voltage	U_{dc}	± 320 kV
Cell capacitance (35 kJ/MVA)	C	11.4 mF
Nominal submodule voltage	U_{nom}	1.6 kV
Rated submodule voltage	U_{SM}^{R}	4.5 kV
Arm inductance	L_{arm}	50 mH
Grid Inductance	L_{grid}	50 mH
Parasitic resistance of the inductors	R	0.1 Ω
Sampling frequency	f_s	10 kHz
Converter model [32, 81, 82, 175, 176]	Data equivalent model (Type 4)	
Arm voltage modulation	Nearest level Modulation [177]	
Zero sequence signal	Third harmonic injection	
Cell selection method	CTBsort [95]	
IGBT device model	ABB 5SNA2000K450300	

(a) Unity power factor condition

In order to obtain the converter's efficiency whenever it operates with unity power factor ($Q^*_{MMC-2} = 0$ Mvar) and also below its limits ($S \leq 1$ pu), the active power flow reference on the MMC-1 terminal P^*_{MMC-1} was varied from 0.1 to 1 pu. Then, for each particular steady-state scenario ($P^*_{MMC-1} = P^*_{MMC-2}$), the voltage limits of the capacitor voltages δ were varied from 5% to 15%. For the same active power flow condition, the fact of varying the tolerance band voltage of the capacitors subsequently changes the average switching frequency of the semiconductors.

The procedure adopted to extract the simulation data for the unity power factor condition is illustrated in the Figure 8.7 and the Algorithm 1. For each particular combination of (P^*_{MMC-1}, $Q^*_{MMC-2} = 0$, δ), the data resultant from the simulation was recorded in an individual file to be processed later.

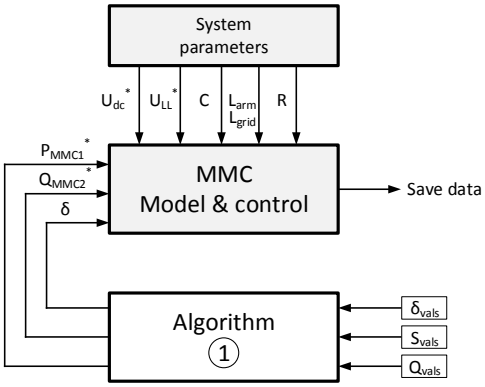


Figure 8.7: Methodology adopted on the data extraction (the unity power factor study).

Algorithm 1: MMC-2 operation
$S \leq 1$, $\cos\phi$ =1, $5\% \leq \delta \leq 15\%$

```
procedure GET FILES 1
    Snom ← 1.0 GVA
    Unom ← 1.6 kV
    Svals ← [1 : −0.1 : 0.1] pu
    Qvals ← 0 pu
    δvals ← [0.15 : −0.005 : 0.05] pu
    for i=1:length(Svals) do
        for j=1:length(δvals) do
            Simulate MMC-HVDC transmission with:
            P*_MMC−1 ← sqrt((Svals(i)Snom)^2 − Qvals
            Q*_MMC−2 ← Qvals
            vmax ← (1 + δvals(j)) Unom
            vmin ← (1 − δvals(j)) Unom
            Create file and save results
        end for
    end for
end procedure
```

(b) Fixed switching frequency condition

Due to the non-linear behavior between the power flow conditions, capacitor's voltage ripple and the average switching frequency, it was decided to study the converter efficiency over several combinations of (P_{MMC-1}, Q_{MMC-2}) $(S \leq 1)$, but with fixed switching frequency. To accomplish this task, the algorithm illustrated in Figure 8.8 was implemented, which is detailed in the Algorithm 2. As the algorithm shows, per each combination of active and reactive power flow conditions, namely (P_{MMC-1}, Q_{MMC-2}) over the four power quadrants defined in Figure 8.9, the SM's voltage range of the MMC2 was incremented until it was found the value of δ that retrieved $149 \leq f_{sw} \leq 151$ Hz. Once the suitable value of f_{sw} was found, a new data file was created with the simulation data, to be later processed.

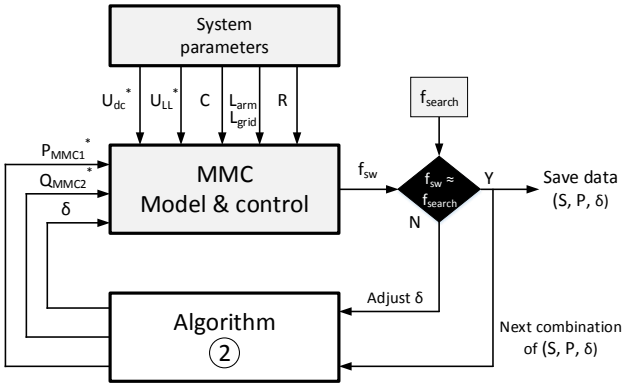


Figure 8.8: Methodology adopted on the data extraction (fixed switching frequency study).

Algorithm 2: MMC-2 operation
$S \leq 1$, cos$\phi \leq 1$, $fsw \approx 150$ Hz

procedure GET FILES 2
  $Snom \leftarrow 1$ GVA
  $Unom \leftarrow 1.6$ kV
  $f_{search} \leftarrow 150$ Hz
  $Svals \leftarrow [1 : -0.1 : 0.1]$ pu
  $Pvals \leftarrow [1 : -0.1 : 0.1]$ pu
  $\delta vals \leftarrow [0.001 : 0.001 : 0.2]$ pu
  for `i=1:length(`$Svals$`)` **do**
    for `j=1:length(`$Pvals$`)` **do**
      $S^* \leftarrow Svals(i)Snom$
      $P^*_{MMC-1} \leftarrow Pvals(j)S^*$
      $Q^*_{MMC-2} \leftarrow \sqrt{(S^*)^2 - \left(P^*_{MMC-1}\right)^2}$
      for `k=1:length(`$\delta vals$`)` **do**
        `Simulate MMC-HVDC with:`
        $(P^*_{MMC-1}, Q^*_{MMC-2})$
        $vmax \leftarrow (1 + \delta vals(k))\, Unom$
        $vmin \leftarrow (1 - \delta vals(k))\, Unom$
        `Analysis` *Post* `simulation (k):`
        $fsw \leftarrow$ `Calculate avg.`f_{sw}
        if $fsw(k) \in [f_{search} \pm 1])$ **then**
          `Save` $\delta vals(k)$
          `Save simulated data in new file`
          `Proceed to next` j
        end if
      end for
      if NOT(find$(fsw(k) \in [f_{search} \pm 1])$ **then**
        `Save` $\delta vals(k)$ `w/ closest` $fsw(k)$
      end if
    end for
  end for
end procedure

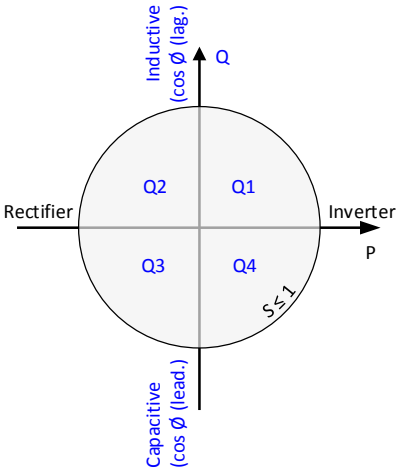


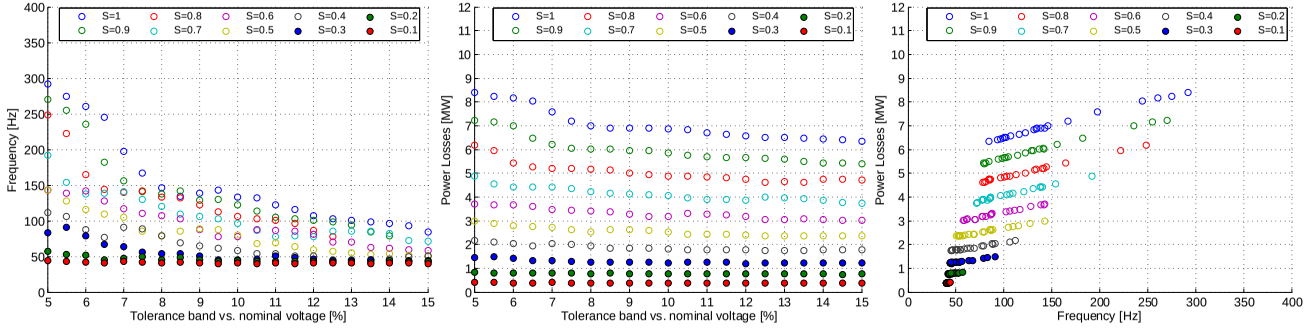
Figure 8.9: Power quadrants (P,Q) definition.

The proposed methodology to deduct an expression that defines the efficiency of the converter is addressed in Section 8.3.2 for the unity power factor operation and in Section 8.3.3 for the fixed switching frequency operation.

8.3.2 Semiconductors power losses model- Unity power factor

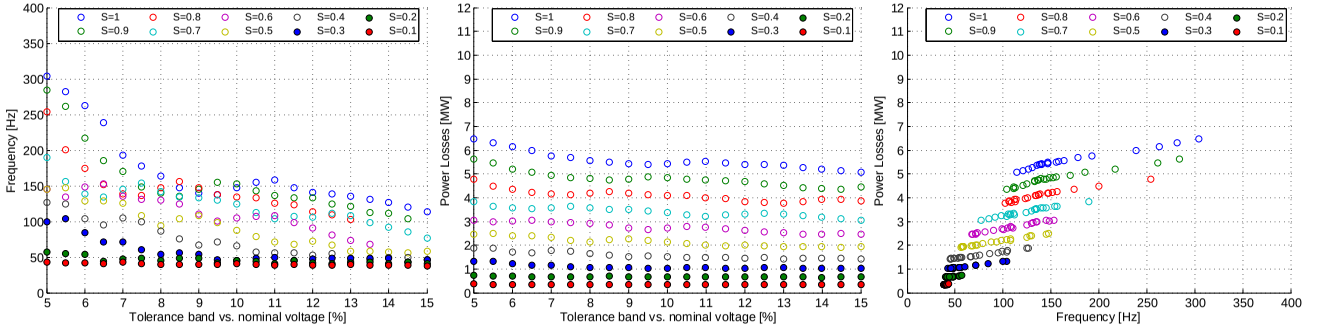
After executing the Algorithm 1 and computing the semiconductors generated losses from the recorded data, the inference of the losses model P_{loss} is initiated. The power loss outcome data in respect to the active power flow P_{flow} (unity power factor), tolerance band δ of the CTBsort and the average switching frequency f_{sw} are illustrated in Figure 8.10 and 8.11 for the inverter and rectifier operation modes, respectively.

First, it should be emphasized that, at the steady-state and nominal operation of the MMC, the SMs are globally characterized by their reduced switching frequency, roughly below the 300 Hz rate. As the arm power flow is varied, the capacitor's energy storage is highly affected which leads to different switching frequency conditions.



(a) (b) (c)

Figure 8.10: Semiconductors power losses with the MMC operating at unity power factor (inverter mode): (a) SM average switching frequency, (b) total losses - P_{loss} and (c) P_{loss} vs. average switching frequency.



(a) (b) (c)

Figure 8.11: Semiconductors power losses with the MMC operating at unity power factor (rectifier mode): (a) SM average switching frequency, (b) total losses - P_{loss} and (c) P_{loss} vs. average switching frequency.

Especially for short tolerance bands, the replacement of the capacitors is triggered more often. Thus, from the converter efficiency perspective, as illustrated in Figures 8.10(b) and 8.11(b), regardless of the power flow direction, the worst operating scenario is materialized whenever the converter is running with the shortest capacitor's voltage limits. The usage of a tolerance band interval from 5% to 15% retrieves the SM's switching frequencies roughly between 100 Hz to 300 Hz (nominal conditions), which was considered to be realistic.

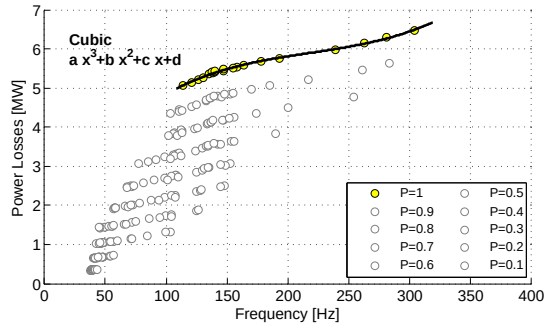
The combination between the SMs average switching frequency f_{sw} of Figure 8.10(a)/ 8.11(a) and the semiconductor's losses P_{loss} of Figure 8.10(b)/ 8.11(b) eliminates the dependency of the capacitor's voltage limits, as illustrated in Figure 8.10(c)/ 8.11(c). Taking this procedure into account, it is a relevant practice to extract a generic expression capable of defining the converter efficiency without the intrinsic details of the cell selection method. Re-drawing the rectifier mode results of Figure 8.11(c) in the given Figure 8.12, and by means of the yellow circles a relation is emphasized between the semiconductor power losses vs. the average switching frequency (yellow circles for P= 1 pu) in Figure 8.12(a), as well as, the semiconductor power losses vs. active power flow (yellow circles for f_{sw}= 100 Hz) in Figure 8.12(b). These two individual relations were used to deduce the mathematical model $P_{loss}(f_{sw},\ P_{flow})$ that estimates the semiconductor power losses for a suitable range of (f_{sw}, P_{flow}) values.

Whenever the MMC is absorbing 1 GW from its ac grid, the semiconductor's power losses can be defined as a cubic function of the switching frequency within the interval presented (8.11).

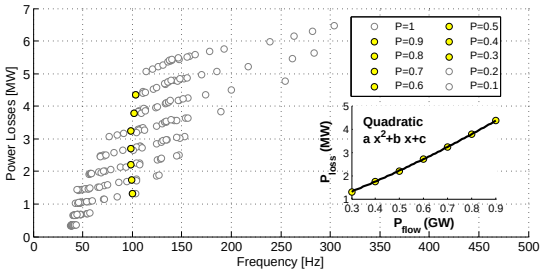
$$P_{loss}(f_{sw}) = y_3 f_{sw}^3 + y_2 f_{sw}^2 + y_1 f_{sw} + y_0 \tag{8.11}$$

where y_x are the coefficients of the polynomial that define $P_{loss}(f_{sw})$.

However, as the power being transferred is changed, the y_x coefficients are changed. Hence, the so called y_x coefficients should not be constants, but functions that vary in accordance with the power flow. Therefore, as Figure 8.12(b) illustrates, there are several combinations of the ac



(a)



(b)

Figure 8.12: Illustration of the relation: (a) P_{loss} vs. f_{sw} (P= 1 pu) and (b) P_{loss} vs. P_{flow} (f_{sw}= 100 Hz).

power flow P and δ that motivate the average switching frequency of 100 Hz. Then, if the $f_{sw} \approx 100$ Hz yellow circles are considered, the semiconductor's power losses can be resembled as a quadratic function of the power flow (8.12).

$$P_{loss}(P) = z_2 P^2 + z_1 f_{sw} + z_0 \tag{8.12}$$

where z_x are the coefficients of the polynomial that define the $P_{loss}(P)$.

In this vision, if the cubic and the quadratic relations are assumed to be the most accurate and representative of the semiconductor's power losses, the (8.11) and (8.12) combined can model the semiconductor's power losses as a function of the switching frequency f_{sw} and its steady-state power flow P, in accordance with the mathematical model $P_{loss}(f_{sw}, P)$

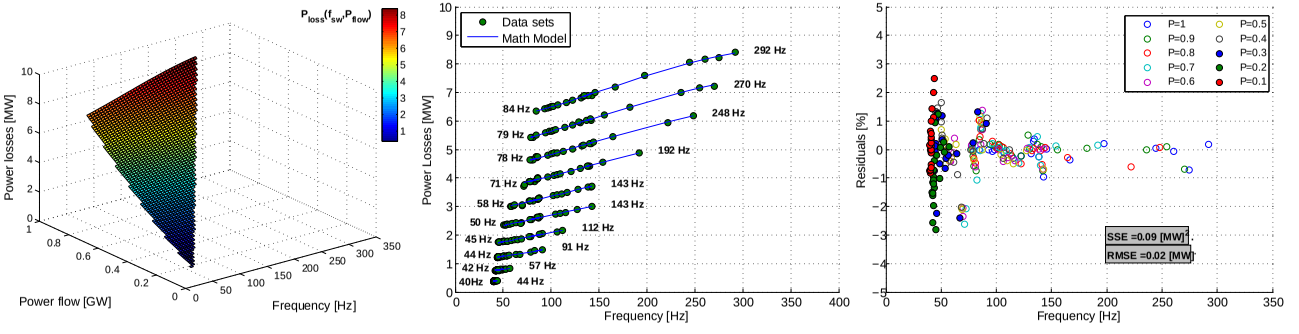
defined as:

$$\begin{aligned} P_{loss}(f_{sw}, P) = &\left(a_1 P^2 + a_2 P + a_3\right) f_{sw}^3 \\ &+ \left(b_1 P^2 + b_2 P + b_3\right) f_{sw}^2 \\ &+ \left(c_1 P^2 + c_2 P + c_3\right) f_{sw} \\ &+ \left(d_1 P^2 + d_2 P + d_3\right) \end{aligned} \tag{8.13}$$

where $(a_\gamma, b_\gamma, c_\gamma d_\gamma)$ $(\gamma \in \{1, 2, 3\})$ are the constants that define the model $P_{loss}(f_{sw}, P_{flow})$. f_{sw} and P are accordingly defined in Hz and pu.

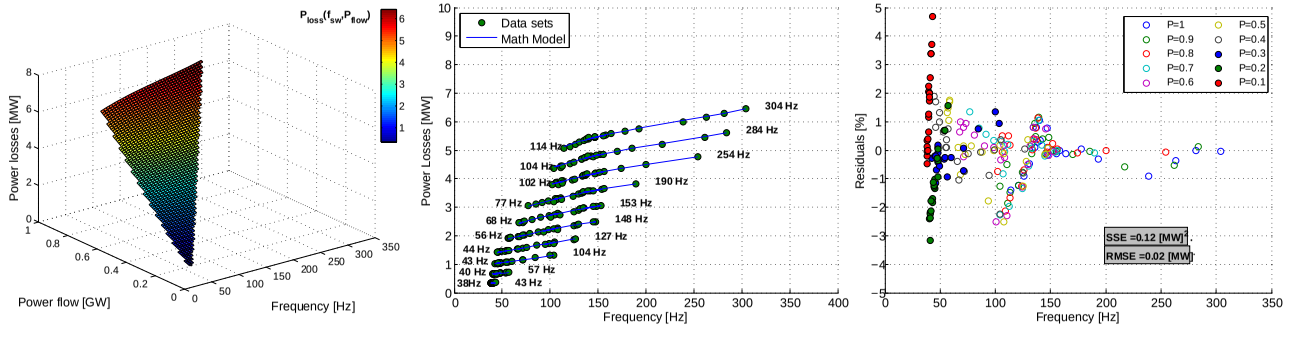
The Levenberg-Marquardt optimization algorithm was used to determine the values of the coefficients $(a_\gamma, b_\gamma, c_\gamma d_\gamma)$ that minimize the least absolute deviations (LAD)(8.14) between the $P_{loss}(f_{sw}, P_{flow})$ model (8.13) and the inverter and rectifier results data of the Figures 8.10(c) and 8.11(c), respectively [178]. The parameters found are presented in the Table 8.2. Moreover, the matching models for the inverter and rectifier modes are illustrated in Figure 8.13 and 8.14 respectively.

$$LAD = \sum_{i=1}^{N_{samples}} \left| P_{loss}^i - data^i \right| \tag{8.14}$$



(a) (b) (c)

Figure 8.13: Semiconductor's power losses model (unity power factor in inverter mode): (a) mathematical model, (b) simulation data vs. model proposed and (c) the corresponding residuals.



(a) (b) (c)

Figure 8.14: Semiconductor's power losses model (unity power factor in rectifier mode): (a) mathematical model, (b) simulation data vs. model proposed and (c) the corresponding residuals.

Parameters		Inverter Mode [pu]	Rectifier Mode [pu]
$P_{loss}(f_{sw}, P_{flow})$ model	a_1	−1.681e−11	−2.386e−10
	a_2	−2.000e−10	6.915e−10
	a_3	1.071e−10	−3.056e−10
	b_1	7.150e−8	4.869e−8
	b_2	−6.982e−10	−2.538e−7
	b_3	−1.880e−8	1.050e−7
	c_1	−1.988e−5	1.734e−6
	c_2	2.107e−5	3.547e−4
	c_3	1.957e−6	−8.944e−7
	d_1	3.714e−3	8.379e−4
	d_2	2.045e−3	1.902e−3
(S_{base}=1 GVA)	d_3	6.798e−6	2.476e−4

Table 8.2: Semiconductors power losses model coefficients for the unity power factor operation of the converter.

As illustrated, the resultant model $P_{loss}(f_{sw}, P_{flow})$ has good accuracy for the optimized parameters. For sake of clarity and according to the proposed model, if the converter is injecting 1 GW into its the ac grid (inverter mode) and the capacitors are being rotated with a 200 Hz cadence (see Figure 8.13(b)), in respect to the base value depicted in the Table (S_{base}= 1 GVA), the power loss estimation is given by:

$$\begin{cases} f_{sw} = 200Hz \\ P_{flow}^{pu} = \dfrac{P_{flow}}{S_{base}} = 1\ pu \end{cases} \Rightarrow \begin{cases} P_{loss}(f_{sw}, P_{flow}) = \left(a_1(1)^2 + a_2(1) + a_3\right) 200^3 \\ \qquad\qquad + \left(b_1(1)^2 + b_2(1) + b_3\right) 200^2 \\ \qquad\qquad + \left(c_1(1)^2 + c_2(1) + c_3\right) 200 \\ \qquad\qquad + \left(d_1(1)^2 + d_2(1) + d_3\right) \\ \qquad\qquad = 0.0076\ pu \end{cases} \tag{8.15}$$

In this view, in the presented operating conditions, the proposed model estimates that the MMC semiconductor's are dissipating 7.6 MW/ 0.0076 pu of power losses, which is corroborated in Figure 8.13(b).

As presented in the previous figures, the model is capable of defining the total power lost by the converter, whenever the switching frequency is maintained on the limits presented in Figure 8.13(b) (inverter mode) and 8.14(b) (rectifier mode). Regardless of the power flow direction, whenever the converter is operating close to its nominal power conditions, the mathematical model presented is capable of estimating the power losses with an error below ±1%. However, as the power flow becomes smaller, the residuals between the data simulated and the model proposed slightly increases to ≈ 3% (at P=0.1 pu) and to ≈ 5% (at P=0.1 pu) for the inverter and rectifier modes respectively. Focusing on the estimation that is characterized by the highest relative error, particularly 5 %, for the $P_{loss}(f_{sw} = 40 \text{ Hz}, P_{flow} = 0.1 \text{ pu})$, the converter is dissipating ≈ 450 kW. Under these circumstances, the relative error that defines the model leads to the residual deviation of ≈ 23 kW, which is considered to be negligible.

8.3.3 Semiconductors power losses model- four power quadrants

The procedure to deduce a mathematical model that can describe the MMC's power losses over the four power quadrants is similar to the one presented in the previous section. Once the Algorithm 2 is executed, the δ values that motivate the average switching frequency of 150 Hz for the selected active and reactive power (P, Q) combinations are obtained. Then, the power losses dissipated on the semiconductors over the four (P, Q) quadrants were computed and they are respectively presented in Figure 8.15. The left-sided graphs show the average switching frequency (≈ 150 Hz) and the capacitor's voltage range for each apparent power flow conditions (S in GVA represented in different colors). Regarding the switching frequency vs. the capacitor's voltage limits graphs, as the apparent power flow is reduced, the correspondent capacitor's voltage ranges are becoming more concentrated around a particular δ point. On the second axis, the power losses as a function of the apparent S and active power P flow are presented. For the same apparent power, the fact that the active power is modified, it means that the reactive

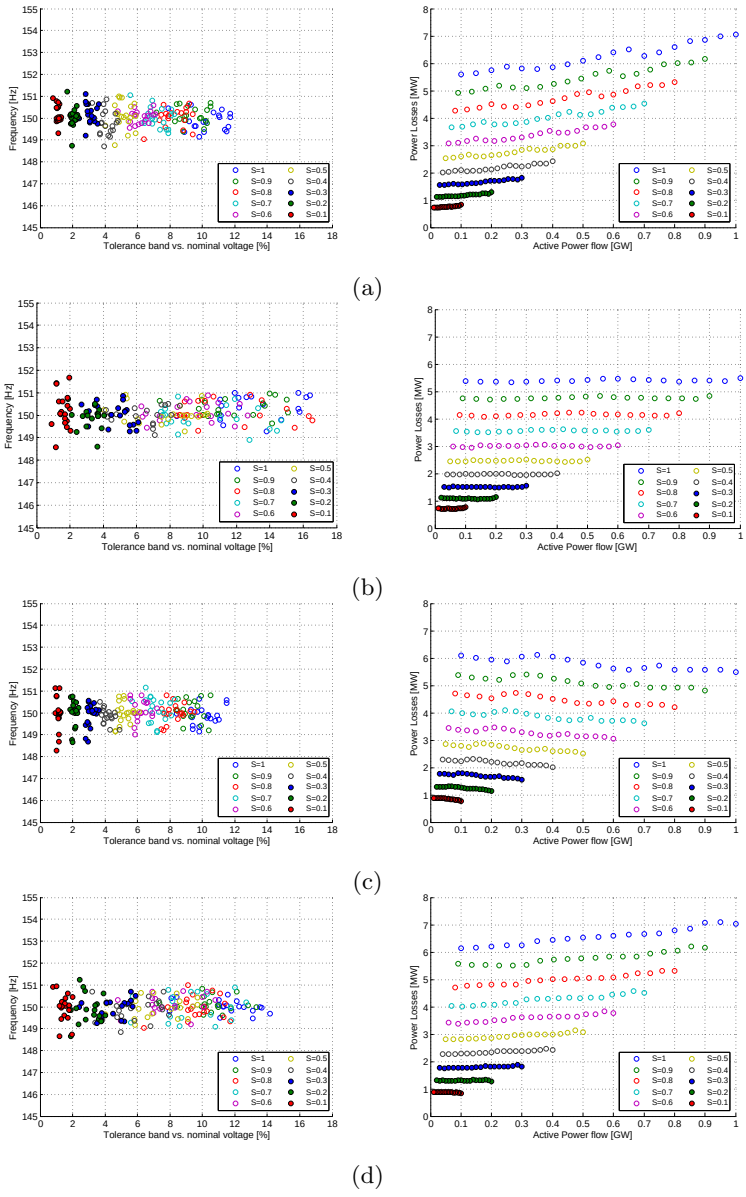


Figure 8.15: Power losses generated by the MMC's semiconductors over the four power quadrants: (a) quadrant 1- Q1, (b) quadrant 2- Q2, (c) quadrant 3- Q3 and (d) quadrant 4- Q4.

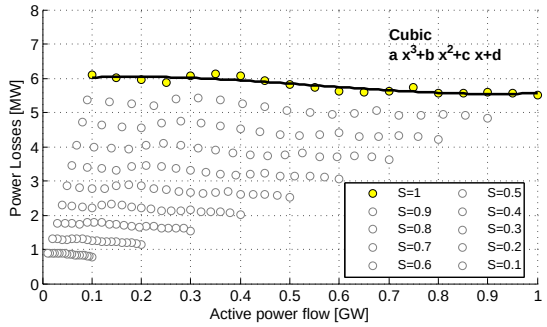
power is being appropriately adjusted. As previously argued, as the active power is reduced, the stress of the semiconductors is scaled down which dissipates less power over the time.

As discussed in Section 8.2, the converter is more efficient on the rectifier (quadrants 2 and 3) than the inverter mode (quadrants 1 and 4). This occurs due to the fact that, on the correspondent 2 and 3 quadrants, the average number of conducting diodes over a grid period is larger than the IGBTs, and the non-controllable devices have a lower on-state voltage, which generate less power losses.

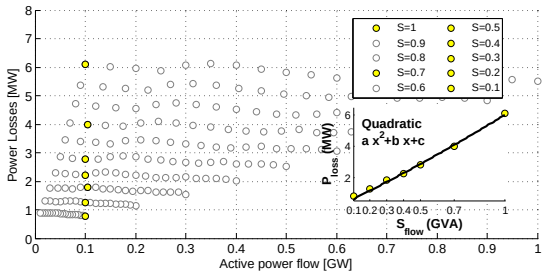
The methodology mentioned in Section 8.3.2 used to deduce either the generic expression, as well as, its parameters to describe the losses model P_{loss} in respect to the combination ($S_{flow}, P_{flow}, f_{sw} \approx 150$ Hz) was again employed. The power losses retrieved by the MMC on the power quadrant 2 that is illustrated in Figure 8.15(b) were reconsidered in Figure 8.16. Then, it was emphasized by means of the yellow circles the relation between the semiconductor power losses vs. active power flow (yellow circles for S_{flow}= 1 GVA) in Figure 8.16(a), as well as, the semiconductor power losses vs. apparent power flow (yellow circles for P_{flow}= 0.1 GW) in Figure 8.16(b). These two individual relations were used to deduce the mathematical model $P_{loss}(S_{flow},\ P_{flow})$ over the four power quadrants of operation. Further, as Figure 8.16(a) illustrates, for the constant value of S_{flow} presented, the losses retrieved by the $\{P, Q\}$ ratio is efficiently modeled as a cubic expression. In opposition, as shown in Figure 8.16(b), for the same active power flow of 0.1 GW, the semiconductor power losses vs. the apparent power flow $P_{loss}(S_{flow})$ is competently modeled as a quadratic expression. Thereby, the $P_{loss}(S_{flow}, P_{flow})$ outcome is depicted as:

$$\begin{aligned} P_{loss}(S_{flow}, P_{flow}) = &\left(a_1 S_{flow}^2 + a_2 S_{flow} + a_3\right) P_{flow}^3 \\ &+ \left(b_1 S_{flow}^2 + b_2 S_{flow} + b_3\right) P_{flow}^2 \\ &+ \left(c_1 S_{flow}^2 + c_2 S_{flow} + c_3\right) P_{flow} \\ &+ \left(d_1 S_{flow}^2 + d_2 S_{flow} + d_3\right) \end{aligned} \tag{8.16}$$

Consequently, the Levenberg-Marquardt optimization algorithm was again used to determine the values of the coefficients ($a_\gamma, b_\gamma, c_\gamma d_\gamma$) which



(a)



(b)

Figure 8.16: Impact of ac power flow conditions on the overall semiconductors power losses: (a) P_{loss} vs. P_{flow} and (b) P_{loss} vs. S_{flow}.

best characterizes the MMC efficiency over the four power quadrants [178]. According to the model formulation, the independent variables P and S have intrinsic limits which validates the conferred model, such as:

- S must be within the $[0.1, ..., 1]$ GVA;
- The P must be inward the interval defined $P \leq S$ and $P \geq 0.1S$.

The deduced model is presented in Table 8.3[4]. The model's accuracy

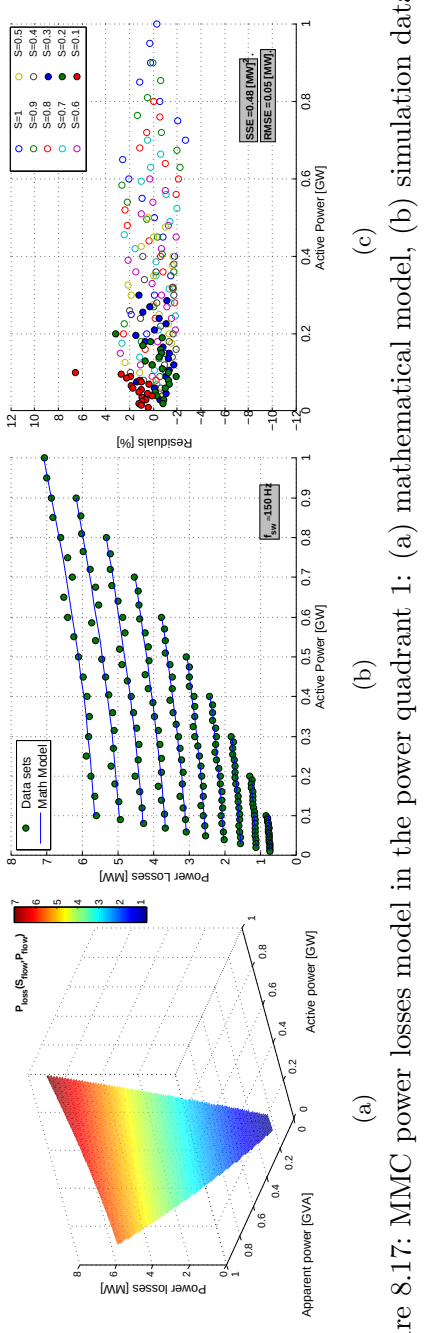
[4]The $P_{loss}(S, P)$ model addresses the power losses in [MW] as a function of the combination of (S in [GVA],P in [GW]). In order to normalize the corresponding model ($P_{loss}(S, P)$ in %) its coefficients should be multiplied by 0.1 (100%/1000MW).

for each particular power quadrant is presented from Figure 8.17 to Figure 8.20, from the first to fourth quadrant respectively.

		Power quadrants (see Figure 8.9)			
		Q1	Q2	Q3	Q4
Parameters		[pu]	[pu]	[pu]	[pu]
$P_{loss}(S_{flow}, P_{flow})$ model	a_1	1.536e−3	−6.333e−4	2.850e−3	−1.054e−3
	a_2	−5.259e−4	4.161e−4	−10.530e−3	5.022e−3
	a_3	−1.333e−3	−1.159e−4	10.200e−3	−2.899e−3
	b_1	−2.607e−3	1.515e−3	3.839e−3	−8.540e−7
	b_2	2.969e−3	−3.668e−4	−3.053e−3	−3.867e−3
	b_3	1.064e−3	−8.592e−4	−4.971e−3	2.478e−3
	c_1	−7.282e−5	−2.123e−3	−2.658e−3	−7.591e−4
	c_2	−5.397e−5	2.551e−3	4.874e−3	2.899e−3
	c_3	4.923e−4	−3.571e−4	−9.094e−4	−7.508e−4
	d_1	1.889e−3	1.752e−3	1.686e−3	2.007e−3
	d_2	3.346e−3	3.210e−3	3.738e−3	3.501e−3
(S_{base}= 1 GVA)	d_3	3.644e−4	3.828e−4	5.000e−4	5.251e−4

Table 8.3: Semiconductors power losses model coefficients for the fixed switching frequency operation of the converter.

The semiconductors power losses model was deduced, for a fixed switching frequency of 150 Hz, over the four power quadrants and they are respectively illustrated in the Figures 8.17(a), 8.18(a), 8.19(a) and 8.20(a). It is worth reinforcing that the model's coefficients $(a_\gamma, b_\gamma, c_\gamma d_\gamma)$ were optimized for the previously mentioned domain defined as $(0.1 \leq S \leq 1)$ GVA and $(0.1S \leq P \leq S)$ GW. Therefore, depending on the power quadrant that the converter is operating, the combination between the apparent and active power flows can lead to power losses of roughly around 1 MW (shaded in dark blue) to 7 MW (shaded in dark red). Thus, if the model is normalized in respect to its nominal conditions, for the same inputs, the correspondent power losses vary from 0.1% to 0.7%, which corroborates the efficiency reduction computed by this VSC-HVdc solution when compared to the previous VSC generations.

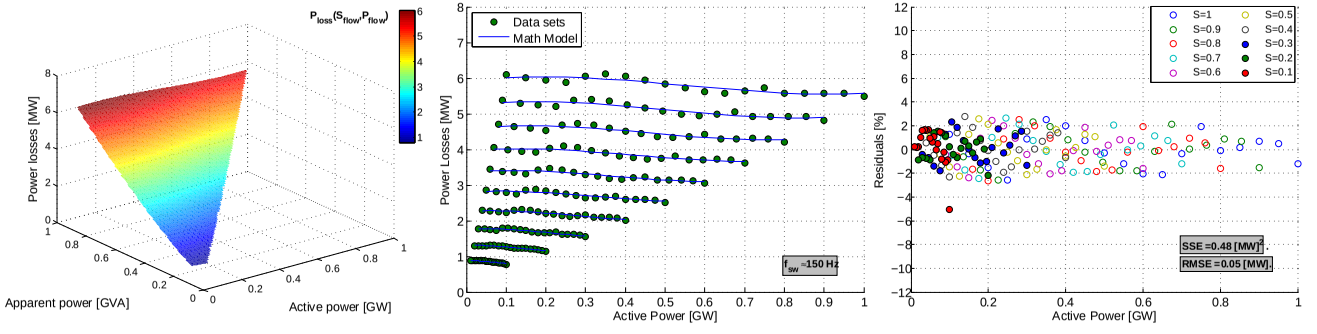


(a) (b) (c)

Figure 8.17: MMC power losses model in the power quadrant 1: (a) mathematical model, (b) simulation data vs. model proposed and (c) the correspondent residuals.

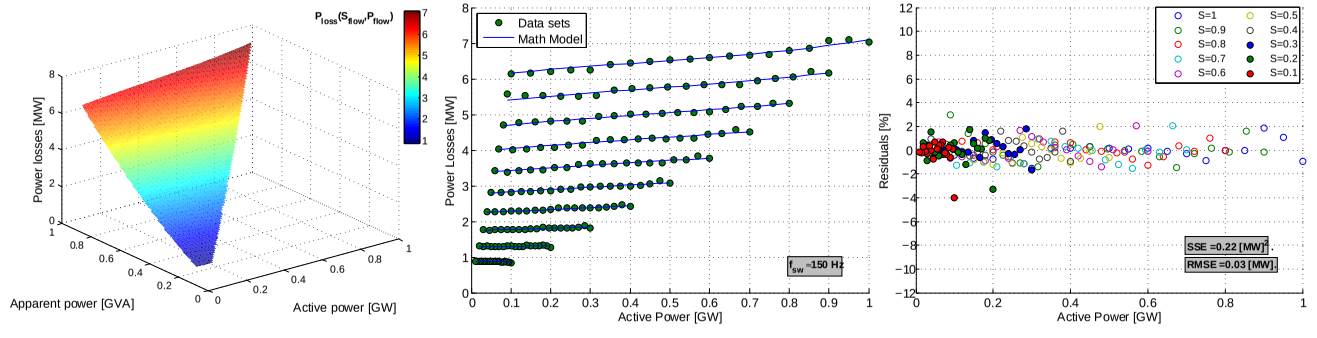
(a) (b) (c)

Figure 8.18: MMC power losses model in the power quadrant 2: (a) mathematical model, (b) simulation data vs. model proposed and (c) the correspondent residuals.



(a) (b) (c)

Figure 8.19: MMC power losses model in the power quadrant 3: (a) mathematical model, (b) simulation data vs. model proposed and (c) the correspondent residuals.



(a) (b) (c)

Figure 8.20: MMC power losses model in the power quadrant 4: (a) mathematical model, (b) simulation data vs. model proposed and (c) the correspondent residuals.

Figures 8.17(b), 8.18(b), 8.19(b) and 8.20(b) compare the discrete data points retrieved by the MMC's simulation and the model proposed. As depicted, the mathematical expression presented is capable of sharply describing the semiconductor's power losses over the four power quadrants. For sake of clarity and according to the proposed model, if the converter is operating as a rectifier and exchanging 0.5 GW/ 0.33 Gvar (inductive) from its ac grid, the converter is accordingly operating on the second power quadrant (see Figure 8.9). Then, the group of constants of the power quadrant 2 should be embraced to estimate the power losses generated by the MMC's semiconductors:

$$\begin{cases} P_{flow}^{pu} = \dfrac{P_{flow}}{S_{base}} = 0.5 \text{ pu} \\ S_{flow}^{pu} = \dfrac{S_{flow}}{S_{base}} = \dfrac{\sqrt{P_{flow}^2 + Q_{flow}^2}}{S_{base}} = 0.6 \text{ pu} \end{cases} \Rightarrow$$

$$\Rightarrow \begin{cases} P_{loss}(S_{flow}^{pu}, P_{flow}^{pu}) = \left(a_1 0.6^2 + a_2 0.6 + a_3 \right) 0.5^3 \\ \qquad\qquad + \left(b_1 0.6^2 + b_2 0.6 + b_3 \right) 0.5^2 \\ \qquad\qquad + \left(c_1 0.6^2 + c_2 0.6 + c_3 \right) 0.5 \\ \qquad\qquad + \left(d_1 0.6^2 + d_2 0.6 + d_3 \right) \\ \qquad\qquad = 0.003 \text{ pu} \end{cases} \tag{8.17}$$

In this view, for the presented operating conditions, the mathematical model estimates that the MMC semiconductors are dissipating 3 MW/0.003 pu of power losses, which is confirmed in Figure 8.18(b).

The accuracy of the proposed model can be validated in accordance to the individual residuals between the real and estimated points, which are presented in the Figures 8.17(c), 8.18(c), 8.19(c) and 8.20(c). Regardless of the power quadrant, whenever the apparent power is higher than 0.3 GVA, the mathematical expression can estimate the power losses of the converter with a relative error up to 3%, which meticulously represents the efficiency of the converter. In the scenarios where the apparent power is not higher than 0.3 GVA, the power loss model presents an almost negligible offset to the real data set points, which increases the relative errors in this area. This occurs because for $S \leq 0.3$

GVA the data sets are more concentrated, particularly for S=0.1 GVA, which is more difficult to reach a better closeness at these points without compromising the model's accuracy at higher power flow operation of the converter. Taking into account the scenario in which the model carries the highest residual, particularly ≈ 8.2 %, that occurs for the converter operation in the rectifier mode with S=0.1 GVA and P=0.1 GW (quadrant 2), the semiconductor's power losses is roughly 0.76 MW, whereas the model estimate 0.7 MW. Hence, the 8.2 % refers to a deviation of only 60 kW. Although the deviation is relatively high, since it refers to very low power flow scenarios, under these circumstances the relative error that characterizes the converter operation is considered to be negligible.

8.4 Conclusions

In the present day, multi-terminal HVdc grids are a viable solution to transport energy to remote and/ or distant areas. The operation of such grids and their efficiency depends, among other things, on the converter power loss knowledge. Therefore, to be able to optimize the power flows in multi-terminal dc networks, it is necessary to recognize its efficiency for different points of operation.

In terms of the on-state losses of the MMC, this was explored under different operating conditions. In accordance with the results, there is an highly asymmetric power loss distribution over the MMC's cells semiconductors. The lower switch of the half-bridge-based submodule (HFSM) is responsible for generating several times more losses than the upper switch. Therefore, a slightly improvement in the voltage drop of the HBSM's lower switch can have a great impact on the converter global efficient.

The power losses generated by the modular multilevel converter is strongly dependent on the cell selection strategy adopted. Therefore, by electing a state of the art MMC selective control of the cells and accordingly a modern estimation method to quantify the semiconductors losses, the converter efficiency was modeled according to two operat-

ing scenarios. The active power exchange with the electrical grid, over a considerable switching frequencies range was taken into account as the first scenario. A polynomial-based expression, whose parameters were optimized according to the Levenberg-Marquardt method, was proposed to describe the converter losses generation P_{loss} when it operates between 0.1 to 1 GW (unity power factor) P_{flow}, and accordingly to the switching frequency selected f_{sw}, resulting in the $P_{loss}(f_{sw}, P_{flow})$ model. Moreover, at the second stage, several combinations of (P, Q) were considered, nonetheless, maintaining the average switching frequency of the converter cells fixed to the 150 Hz value, which accordingly to the literature is the typical switching frequency of the SMs in real applications. Then, a second polynomial-based expression was described and proposed to outline the converter efficiency over the power quadrants defined by the direction of (P, Q). The resultant models, as presented, can accurately match the converter losses with the maximum absolute error $\leq 3\%$, which is an exceptional estimator of the power losses produced by the modular multilevel converter.

Chapter 9

MMC-HVdc in STATCOM mode

The challenges of adopting multi-terminal HVdc schemes are being advanced due to the HVdc technology development [179, 180]. Thankfully to the introduction of the modular multilevel converter (MMC) in the HVdc field, among other reasons, the multi-terminal dc schemes are no longer an illusion, but a reality [27]. With this achievement, the creation of an European dc super grid composed of interconnected smaller dc grids, with different configurations is expected in a long-term [15, 57, 181, 182].

In case of a strongly interconnected ac and dc network, the dc transmission grids are expected to be re-structured over time in order to maximize power transmission efficiency [164, 183]. In this vision, in some grid configurations, it is eventually more efficient to transmit power in ac than dc. Therefore, some of the existing HVdc-based MMCs could be sectioned and consequently isolated from the dc grid. Hence, by endowing those MMC-based dc grid converters with the static synchronous compensation (STATCOM) operating mode, they become more valuable whenever they get split from the correspondent dc grid.

Several STATCOM structures have been proposed in the literature for medium voltage [184, 185] and high voltage applications with different voltage source converter structures. A MMC with cluster of bridge-cells connected in star or delta can be found in [130, 186–190]. Moreover, the MMC in STATCOM mode can be found in the literature with a chopper cells-based structure for a three and four phase-based schemes [184,191,192]. Hence, dedicated MMC designs to operate in STATCOM mode are found in the literature.

This work studies the degrees of freedom of a MMC that was designed for high voltage dc transmission applications, and, whenever it is sectioned from its dc grid and it is equipped with the STATCOM mode. Once the converter becomes split from a dc grid, its dc voltage target become flexible, and can be altered to guarantee a better performance of the converter. In the converter control perspective, several options are available to modify its dc voltage value, such as the modification of the individual voltages of the capacitors and/or the mean voltage generated on the converter arms. The converter performance in terms of switching frequency, capacitor voltage ripple and number of voltage steps in its output is analyzed and presented.

9.1 HVdc-based MMC in the STATCOM operation mode

As mentioned, in a futuristic vision, large and interconnected ac and dc grids should have a flexible arrangement in order to optimize the power transfer from generation until consumption. According to ac and dc grid planning, some of the VSC can be isolated for the dc grid by opening the dc breakers. Those HVdc-based MMCs can be used to provide ac grid support, as managing the reactive power flow with the ac network.

According to the MMC nature, if it needs to be isolated from its dc grid by means of mechanical breakers, as pointed out in Figure 9.1, there is no specific requirement for the voltage across the dc terminals of the converter, as long as the converter can still synthesize the necessary e_j voltage in order to control the active and reactive power flow at the point of common coupling (PCC).

Considering the STATCOM operation mode, the converter can enhance an alternative performance by adjusting the voltage across the dc terminals. Figure 9.2 emphasizes the fact that the mean voltage across the converter arms can be modified, which intrinsically varies the voltage across its dc terminals. As discussed in Chapter 3, whenever the converter is connected to a dc grid, the converter control handles the

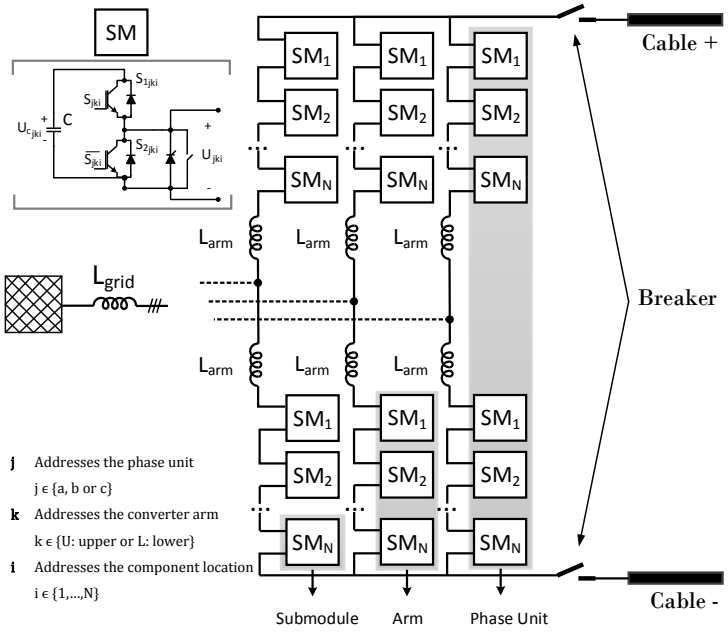
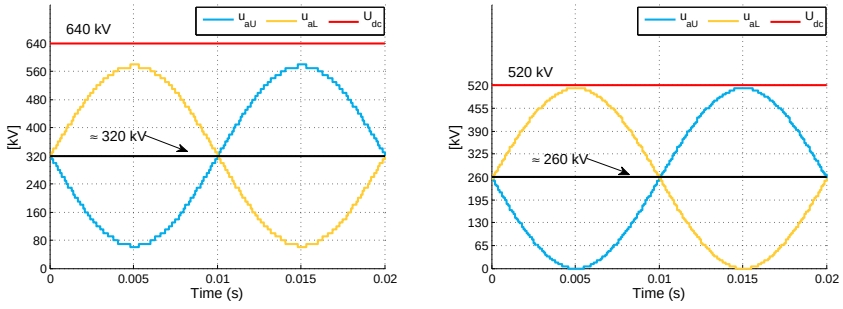


Figure 9.1: Structure of a three-phase MMC.



(a) MMC in HVdc interconnected mode. (b) MMC in isolated mode (STATCOM).

Figure 9.2: HVdc-based MMC operating in interconnected or isolated from the dc grid.

dc bus voltage by means of the homopolar current component of the differential current. But, in contrast, when it becomes split from the dc

grid, no homopolar current will flow. Thus, the internal state control of the converter is then updated to the one illustrated in Figure 9.3, whereas, the control scheme of the converter interactions with the ac grid are the remained unchanged.

The voltage variation at the dc bus of the converter can be accomplished in different ways, leading to different performances of the converter. Combining (3.10) and (3.34), and rewriting them to (9.1), it can be deducible that the MMC's dc-bus voltage can be directly handled by a proper management of the common values of the $m_{jU}U_{jU}^{\Sigma}$ and $m_{jL}U_{jL}^{\Sigma}$ components, when it operates in the isolated mode. Moreover, the fact of varying the common values of the $m_{jU}U_{jU}^{\Sigma}$ and $m_{jL}U_{jL}^{\Sigma}$ components, it does not affect the interactions between the converter and its ac grid, as they are canceled at the converter's *emf* e_j.

$$U_{DC} = u_{diff_j} + \left(\underbrace{m_{jU}U_{jU}^{\Sigma}}_{u_{jU}} + \underbrace{m_{jL}U_{jL}^{\Sigma}}_{u_{jL}} \right) \tag{9.1}$$

The fact of the MMC being isolated from its dc grid means the dc-bus voltage becomes dependent on the total voltage sum of the stack's SMs U_{jk}^{Σ}. Hence, the direct modulation should be conjointly upgraded. Therefore, the U_{dc} measurement in (3.16) is then replaced by a quarter of $(U_{jU}^{\Sigma} + U_{jL}^{\Sigma})$ [1] (9.2).

$$\begin{aligned} m_{jk}^{*} &= \frac{\frac{1}{2}\frac{U_{jU}^{\Sigma} + U_{jL}^{\Sigma}}{2} - \frac{u_{diff_j}^{*}}{2} \pm e_j^{*}}{U_{jk}^{\Sigma}} \\ &= \frac{1}{2} + \frac{\pm e_j - \frac{u_{diff_j}}{2}}{U_{jk}^{\Sigma}} \end{aligned} \tag{9.2}$$

[1] In (9.2) it is considered that $U_{jU}^{\Sigma} = U_{jkL}^{\Sigma} = U_{jk}^{\Sigma}$.

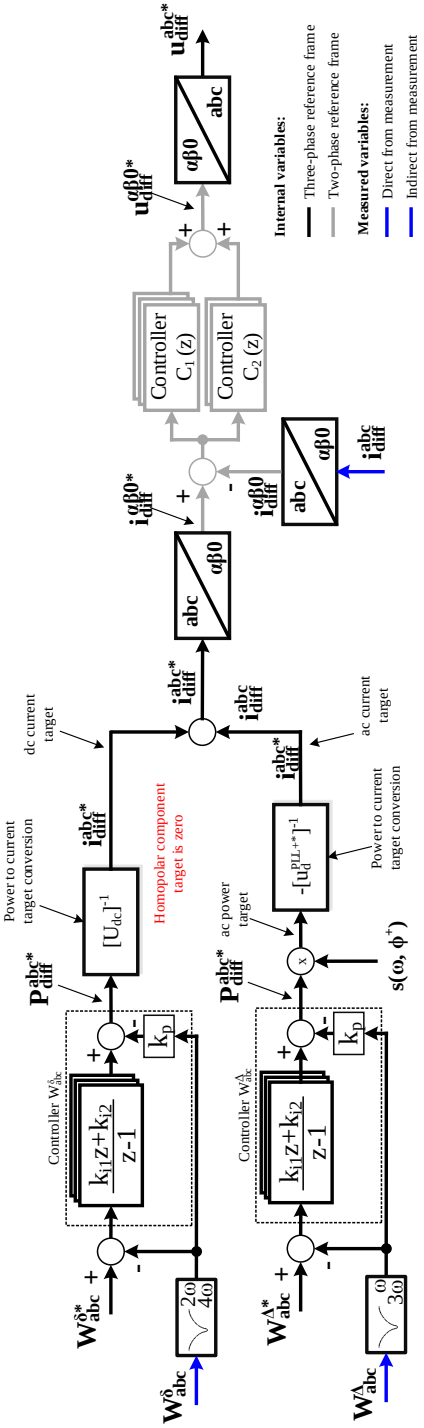


Figure 9.3: Overall control diagram of the MMC in STATCOM mode.

Hence, in accordance with what was emphasized and with (9.1), once the converter gets isolated from the dc grid, several scenarios are available to synthesize the converter's dc-bus voltage. They are enumerated as:

1. The pole to pole voltage at the dc bus can be imposed to be equal to the interconnected mode (no changes in the converter performance). Then, the stack modulation index m_{jk} and its stored energy is remained equal to the interconnected mode.

2. The dc bus voltage is reduced by means of decreasing the average value of m_{jk}. This is done by adding a variable k into the arms voltage modulation and according to its value ($0 \leq k \leq 1$), the mean value of m_{jk} is varied (9.3).

$$\begin{aligned} m_{jk}(t) &= \frac{k(t)\left(\frac{U_{jU}^{\Sigma}+U_{jL}^{\Sigma}}{4}\right) \pm e_j(t) - \frac{u_{diff_j(t)}}{2}}{U_{jk}^{\Sigma}(t)} \quad \text{where } k(t) \leq 1 \\ &= k(t)\frac{1}{2} + \frac{\pm e_j(t) - \frac{u_{diff_j(t)}}{2}}{U_{jk}^{\Sigma}(t)} \end{aligned} \tag{9.3}$$

   If it is imposed that k equals 1, the mean value of the arm modulation remains equal to (1/2), which become equal to the already presented scenario 1. The minimum value of k depend on the grid voltage peak.

3. The dc voltage is increased[2] or decreased accordingly to the U_{jk}^{Σ} value. If the converter absorbs or injects the required or the energy surplus from or to the ac grid, it directly impacts on the U_{jk}^{Σ} value. At this stage it is considered that the value of k is equal to 1, and therefore the modulation index is centered in (1/2).

[2] In the scenario that U_{jk}^{Σ} increases, the energy stored in each submodule is also increased. Hence, its uppermost value is defined accordingly to the most critical voltage-dependent device in the SM, i.e., sensors, capacitors, semiconductors, etc. In this study, it was considered that the voltage sum U_{jk}^{Σ} could be increased by 5% above the nominal conditions.

Table 9.1: Circuit parameters of the MMC.

Parameters	Notation	Value
Number of submodules/arm	N	400
Rated active power	P	1.0 GW
Rated reactive power	Q	300 Mvar
Line voltage	U_{LL}	333 kV
dc-bus voltage	U_{dc}	± 320 kV
Cell capacitance (35 kJ/MW)	C	11.4 mF
Nominal submodule voltage	U_{nom}	1.6 kV
Arm inductance	L_{arm}	50 mH
Grid Inductance	L_{grid}	50 mH
Parasitic resistance of the inductors	R	0.1 Ω
Sampling frequency	f_s	10 kHz
Cell selection method	HATB	Band 3%
IGBT device model	ABB 5SNA2000K450300	

4. The dc voltage is increased[2] or decreased by a simultaneous management of either in the $k(t)$ (9.3) and U_{jk}^{Σ} values.

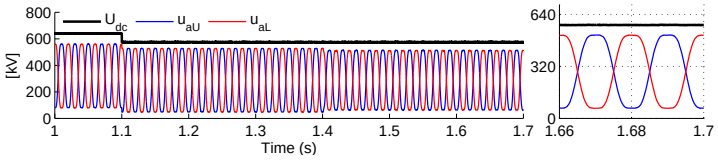
It was considered that the value of $k(t)$ is equal for the six stacks and MMC energy is equally distributed among the six stacks. Moreover, it was also assumed that the three-phase system of the network is balanced. Each particular condition enumerated has a particular impact on the converter operating performance, which is analyzed in the next section.

9.2 Case study

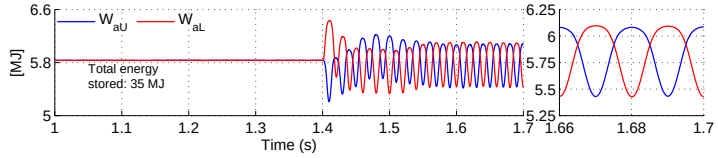
The aforementioned four operating scenarios of the HVdc-based MMC in STATCOM mode are validated in this section. The MMC model adopted was based on the parameters presented in the Table 9.1. As the table shows, the HVdc converter is designed to store 35 MJ in all its capacitors and it also manages up to 1 GW/ 300 Mvar in its ac bus. Moreover, at nominal conditions the SMs states can be managed to synthesize voltages up to 640 kV in each stack of SMs, which is also the nominal pole-to-pole voltage at the dc side of the converter. Particularly, in the islanded mode, the possible options for the pole-to-pole voltages at the dc side of the converter are listed bellow:

1. The voltage at the dc bus can be either controlled to be equal to

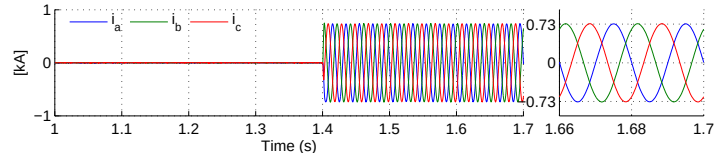
640kV, or to be reduced, as shown in Figure 9.4. Until t=1.1 s, the converter is controlled in order to impose the voltage across its dc terminals equal to the nominal conditions. Later on, the dc voltage was reduced to 576 kV by changing the k factor from 1 to 0.9. This event adjusted the average voltage of the converter arms without affecting its energy storage, internal currents and the ac grid interactions.



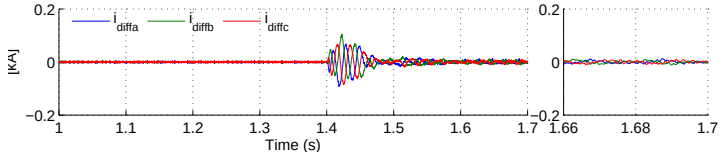
(a) MMC voltages in the upper and lower arms (phase unit a).



(b) Energy storage at the upper and lower arms (phase unit a).



(c) Three-phase currents at PCC.



(d) Differential currents flow on the converter legs.

Figure 9.4: HVdc-based MMC in the STATCOM mode with reduced dc voltage (k is reduced from 1 to 0.9).

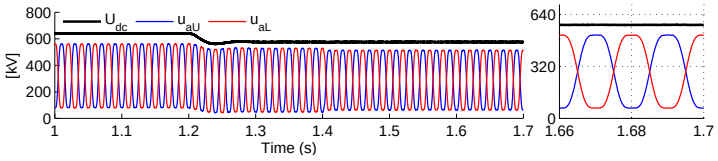
2. The dc voltage can be changed by enhancing the converter with additional energy (if possible) which will boost the voltage across each SM and correspondingly the maximum voltage vector mag-

nitude applicable to each stack U_{jk}^{Σ} >640 kV. In opposition, the MMC capacitors can be slightly discharged, hence, reducing the magnitude of the vector U_{jk}^{Σ} to values lower than 640 kV. Figure 9.5 shows the dynamics of the converter whenever the energy storage target is reduced from 35 MJ to 28 MJ and the arm maximum voltage vector is then reduced from 640 kV to 576 kV (whereas k is equal to 1). Until t=1.2 s, the converter is operating with its nominal conditions and afterwards, its energy surplus is injected into the ac grid. During this transient ($\approx$ 100 ms), internal currents are flowing on the converter to guarantee symmetrical energy distribution among the six stacks of the converter until the steady-state is achieved.

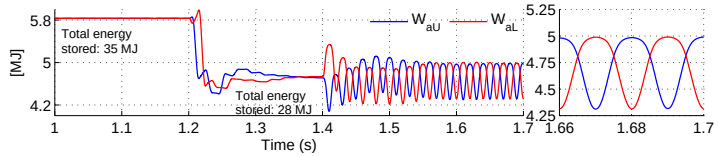
3. Finally, the remaining solution is to settle the dc voltage on the dc-side of the converter by acting simultaneously on the energy storage (varying U_{jk}^{Σ}) and on the k factor as illustrated in Figure 9.6. Until t=1.1 s the converter was operating with nominal conditions and at that instant k was changed from 1 to 0.9 (affecting the average arm voltage). Later on, at t=1.2 s, the vector magnitude U_{jk}^{Σ} was respectively reduced to 90% of their nominal conditions.

Several combinations of the average voltage imposed across the stacks u_{jk} and the energy storage of the converter (function of U_{jk}^{Σ}, can lead to the same voltage across the dc terminals of the converter (9.1). However, each particular aggregation leads to very peculiar results, which are consequently analyzed. The converter performance assessment was done by varying k from 1 to 0.8 and the amplitude of U_{jk}^{Σ} from 1.05 to 0.85 pu. The parameters analyzed were the capacitor voltage sum ripple (ripple in U_{jk}^{Σ}), the number of arms voltage levels and the average switching frequency of the SMs. Thus, the results are summarized in the Table 9.2.

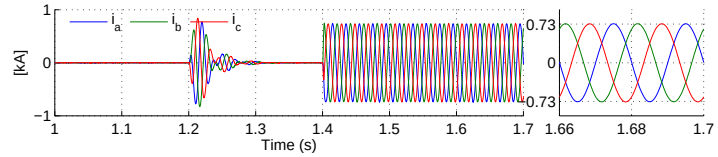
It should be emphasized that during the STATCOM operation, no active power is flowing on a permanent basis (only to compensate the losses). Moreover, the converter can handle up to the nominal 300



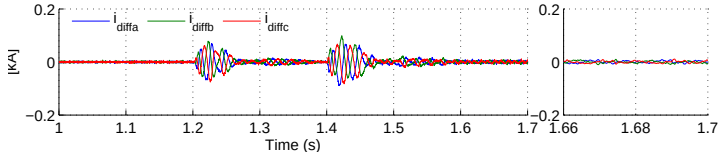
(a) MMC voltages in the upper and lower arms (phase unit a).



(b) Energy storage at the upper and lower arms (phase unit a).



(c) Three-phase currents at PCC.

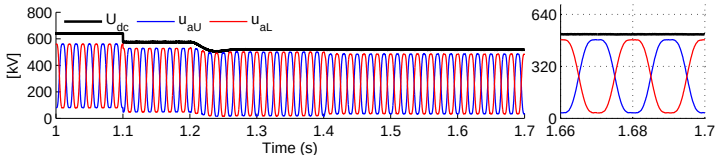


(d) Differential currents flow on the converter legs.

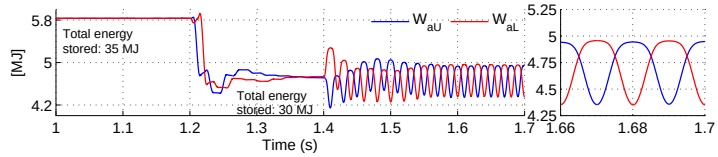
Figure 9.5: HVdc-based MMC in the STATCOM mode with reduced energy condition (U_{jk}^{Σ} downgraded to 576kV).

Mvar of reactive power flow with the network. Moreover, the converter stores 35 MJ which is subdivided equally in all its submodules and imposes approximately 640kV between its dc poles. In this scenario, its performance is characterized by generating 297 voltage steps at the arms and the SMs were being rotated at a rate of approximately 69 Hz. Then, by varying either the k factor or the energy that is stored on the converter, those values are changed, which indicate that the converter was moved towards a distinct operating point.

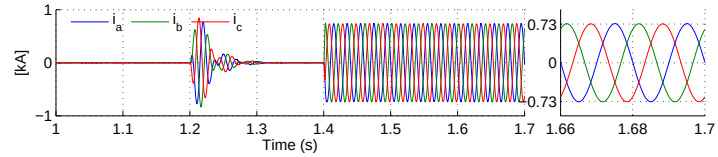
The reduction of the k factor, besides reducing the average voltage of the converter arms, directly impacts the average number of active SMs



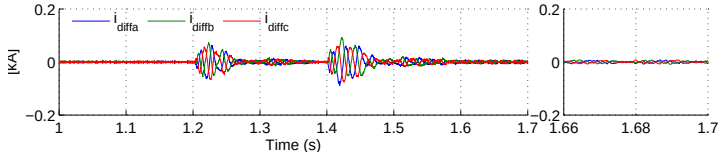
(a) MMC voltages in the upper and lower arms (phase unit a).



(b) Energy storage at the upper and lower arms (phase unit a).



(c) Three-phase currents at PCC.



(d) Differential currents flow on the converter legs.

Figure 9.6: MMC-HVdc-based STATCOM in non-nominal conditions (U_{jk}^{Σ} downgraded to 576kV and and k reduced to 0.9 respectively).

in each particular stack. The reduction of the mean voltage synthesized on the converter arms is accomplished by the linear reduction of the average number of capacitors inserted in each arm. As Figure 9.4 shows, in order to synthesize a 640 kV across the dc terminals of the converter, the mean voltage of the arms were put around 320 kV (N/2 inserted capacitors). Affecting k with the value of 0.9, linearly reduces the average number of active capacitors to (0.9N/2), and the dc voltage to 576 kV (0.9 pu). In practice, with the reduction of the average number of active SMs, fewer capacitors will be needed to synthesize the same ac voltage

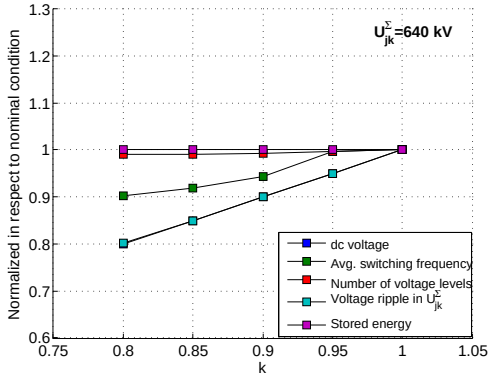
Table 9.2: MMC performance under the presented operating scenarios.

Udc factor	Notation	$U_{jk}^{\Sigma}=544$kV $W_{jk}^{\Sigma}=25$MJ	$U_{jk}^{\Sigma}=576$kV $W_{jk}^{\Sigma}=28$MJ	$U_{jk}^{\Sigma}=608$kV $W_{jk}^{\Sigma}=32$MJ	$U_{jk}^{\Sigma}=640$kV $W_{jk}^{\Sigma}=35$MJ	$U_{jk}^{\Sigma}=672$kV $W_{jk}^{\Sigma}=39$MJ
1.00	Dc-bus voltage (kV)	543	575	607	639	671
	Switching frequency (Hz)	75	72	71	69	67
	Number of levels	351	331	313	297	283
	Ripple in U_{jk}^{Σ} (kV)	41.1	41.1	41.1	41.1	41.1
0.95	Dc-bus voltage (kV)	516	546	577	607	638
	Switching frequency (Hz)	75	72	70	69	67
	Number of levels	349	329	312	296	282
	Ripple in U_{jk}^{Σ} (kV)	39.1	39.1	39.1	39.1	39.1
0.90	Dc-bus voltage (kV))	489	518	546	575	604
	Switching frequency (Hz)	75	73	70	69	64
	Number of levels	348	328	311	295	281
	Ripple in U_{jk}^{Σ} (kV)	37.0	37.0	37.0	37.0	37.0
0.85	Dc-bus voltage (kV)	461	489	516	543	570
	Switching frequency (Hz)	74	72	71	64	62
	Number of levels	346	326	309	294	280
	Ripple in U_{jk}^{Σ} (kV)	34.9	34.9	34.9	34.9	34.9
0.80	Dc-bus voltage (kV)	441	460	485	511	537
	Switching frequency (Hz)	68	70	64	61	61
	Number of levels	341	326	309	294	280
	Ripple in U_{jk}^{Σ} (kV)	34.5	32.9	32.9	32.9	32.9

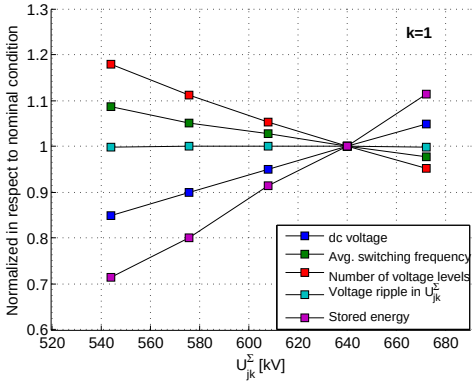
waveform. Under these circumstances, a smaller number of capacitor rotations is acquired because less capacitors hit their imposed limits. The reduction of the rotating events of the cells also translates into the decrease of the converter's switching frequency. Moreover, if there are less capacitors used over a fundamental grid cycle, it also translates in the reduction of their voltage ripple.

The variation of the converter's energy storage directly influences the pole-to-pole voltage of the converter, as emphasized in the gray-scale row of the Table 9.2. As the converter stores less energy, which accordingly affects U_{jk}^{Σ}, the modulation index of its arms should increase in order to synthesize the same e_j voltage (9.3). This fact correspondingly leads to a higher number of voltage steps present on the arm voltages, which properly ensures a higher switching frequency of the cells.

The impact of the k factor, as well as, the amplitude of stack voltage U_{jk}^{Σ} were normalized in respect of the converter nominal conditions and they are illustrated in Figure 9.7. Observing the impact of both factors, although some values generate the same dc voltage, it is clear that the converter performance is affected in different ways. It is evident that the reduction of the mean voltage of the arms has a significant impact on the



(a)



(b)

Figure 9.7: Impact of the (a) k and (b) U_{jk}^{Σ} values on the STATCOM performance.

switching frequency and voltage ripple reduction. By contrast, reducing the energy storage of the converter, significantly increases the number of voltage levels produced in each stack, which directly increases the power quality of the converter, with the cost of increasing the switching frequency of the converter. On the other hand, if the converter can safely withstand higher voltage amplitudes than U_{jk}^{Σ}=640 kV in the respective arms, it is also an interesting option. Besides enabling a higher energy storage, this action also reduces the average switching frequency of the converter due to the capacitor's voltage increase.

Under the circumstances, in one way, the k factor can be used to increase the converter efficiency, as well as the reduction of the voltage ripple of the capacitors. On the other hand, the energy storage of the converter can be handled in such a way that increases the number of voltage levels on the arms, which outlines the power quality increase of the converter. However this option compromises the average switching frequency of the converter. Depending on the performance goal, the combination between both options are also valid.

9.3 Conclusions

In a futuristic vision, a deeply interconnected ac and dc network is expected which would be re-structured over the time in order to maximize the power transmission efficiency. In some grid configurations, grid-tied inverters can eventually become isolated from the dc grid by means of breakers and enhancing those converters with the STATCOM functionality increases their value and its operation should be studied.

Once the HVdc-based MMC gets isolated from the dc grid, the pole-to-pole voltage at the dc side can be settled to increase its performance when compared to its nominal operating conditions. Specifically, the increase of the converter efficiency, power quality or energy storage were aspects analyzed in this work.

Essentially, it is demonstrated that the dc voltage across the converter terminals can be settled by either varying the energy storage of the converter, by varying the mean voltage that is generated on the converter arms, or by handling both. The reduction of the mean voltage of the arms, and accordingly on its dc-bus voltage side, has a significant impact on the switching frequency and voltage ripple reduction. On the other hand, the number of voltage steps generated on the converter arms can be enlarged by reducing its energy storage, improving then its power quality. Hence, depending on the performance needed for the STATCOM-MMC, the suitable solution should be selected.

Chapter 10

Conclusions

Several studies for improving the operation of the modular multilevel converters (MMC) have been presented in this thesis. This chapter details the main findings throughout the thesis and it includes directions for future work.

10.1 Contributions

The contributions are detailed per chapter.

- In **Chapter 3** the methodology used to control the converter is presented. In addition, the control scheme is complemented with a step-by-step procedure to design all the controllers embraced. Moreover, it is pointed out that it is feasible to internally move energy between the converter stacks.
- In **Chapter 4** the need to achieve faster models to obtain fast and accurate results for power system studies is discussed. Consequently, two modeling techniques are proposed that significantly reduce the simulation time lengths without severely compromising their accuracy. The time span reduction of the proposed models comes with the cost of not representing the individual voltages of the capacitors. However, from the power system operation perspective, the knowledge of the individual voltages across the capacitors is not relevant.
- In **Chapter 5** the feasibility of aggregating several modulation techniques with the zero sequence signals (ZSS) to synthesize the

voltage across the converter arms is studied. This study reveals that the presence of the ZSS on the arm voltage modulation has an higher impact on the converter performance than the methodology followed to modulate the converter voltage. Then, it is verified that the nature of the ZSS influences the converter behavior differently. Therefore, depending on the ZSS nature selected, different parameters of the MMC can be improved, namely the converter efficiency, voltage ripple across the capacitors and/or the total harmonic distortion factors of its ac variables.

- **Chapter 6** is dedicated to the MMC performance when the voltages across its arms admit a discontinuous ZSS (D-ZSS). A methodology is proposed to reduce or even eliminate the need of introducing capacitors on the arm current path whenever the load stress of the semiconductors reaches its uppermost value. The proposed D-ZSS enables the reduction or elimination of switching events on the MMC arms over a 60 degrees intervals. By aligning this switch-less intervals with the instants that the arm current reaches its maximum point a considerable power loss amount is reduced.

- In **Chapter 7** two hybrid selective strategies are proposed to rotate the inserted capacitors on the MMC stacks (HCTBsort and HATBsort). Those algorithms were compared to other schemes already presented in the literature. Then, the HCTBsort is characterized by the global reduction of the semiconductor's power losses and the large exploitation of the capacitor's limits. On the HATBsort, depending on the strategy that is compared with, it can also increase the converter efficiency.

- In **Chapter 8** the power dissipated on the semiconductors of the MMC is analyzed. It is demonstrated that there is a great asymmetric losses distribution between the upper and lower switches of the half-bridge cell. Furthermore, a polynomial-based expression is proposed that can describe the power losses produced by the semiconductors as a function of the operating conditions of the converter. The proposed model can be used in optimal power

flow (OPF) studies and it estimates the semiconductors power losses with high accuracy.

- In **Chapter 9** the degrees of freedom of the HVdc-based MMC that is endorsed with the STATCOM mode of operation is analyzed. Once a MMC is demanded to be isolated from its dc grid, by adjusting the voltage across its dc terminals, an improved exploitation of the converter is attained. Particularly, the dc voltage management can lead to a more efficient operation of the converter, as well as the capacitor voltage ripple reduction, which might contribute to a longer life-time of its devices.

10.2 Future work

The modular multilevel converter is one of the most promising technologies for HVdc transmission. It is a relatively new technology and there is still much research to do in many different parts in this field. The work developed on this thesis, has raised several research lines for future work. Given this, the future research lines are described by chapter:

- Chapter 3
  - Replacement of the notch filters by the inverse model of the converter to improve the dynamic behavior of the control strategy.
  - Test the control design on an MMC experimental platform.
- Chapter 4
  - Include the type 1 and 2 models on the accuracy analysis of the models presented;
  - Ratify the accuracy of the modeling techniques analyzed with a small-scale laboratory implementation of the converter.

- Chapter 5 and 6
  - Analyze the impact of aggregating the presented arm voltage modulation techniques with other selective control techniques on the converter performance.
  - Expand the analysis performed by including other arm voltage modulation strategies.
- Chapter 7
  - Include and analyze the impact of the dead-time applied to the switches of the half-bridge-based submodules on the average switching frequency of the converter.
  - Include a communication delay between the voltage sampling of the capacitors placed at the submodules and the control structure.
- Chapter 8
  - Analyze the impact of having different converter parameters, such as the ac and dc bus voltages, on the mathematical model proposed.
  - Perform the economical-technical comparison of building the half-bridge submodules of with equal or different semiconductor features in the upper and lower switches.
- Chapter 9
  - Investigate the minimum dc-voltage value that can be synthesized on the MMC in STATCOM mode during an ac fault event.

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Appendices

Appendix A

INELFE Interconnector

The first HVdc interconnection between Spain and France was commissioned in 2015 and was entitled *INterconnexion ELectrique France Espagne* (INELFE). This interconnector allowed the reinforcement of the Iberia peninsula's power system. This project permits to dispatch the excess of renewable energy generated in Portugal and Spain towards other European countries. With this achievement, the Iberia peninsula power system become more reliable and the security of supply to consumers was increased.

The interconnector is composed of two identical and independent HVdc transmission circuits that link the *Santa Llogaia* (Spain) and *Baixas* (France) substations as displayed in Figure A.1. These redundant power circuits are managed by the corresponding transmission system operators (TSOs) involved, specifically the REE (*Red Eléctrica de España*) and RTE (*Réseau de transport d' Electricité*).

The innovation of this project concerns power rating and nature of the converter stations which are based on the state of the art solution of the VSC-HVdc technology, the modular multilevel converter (MMC). Each link can transmit up to 1 GW in any direction, which yields to an overall transmission capability of 2 GW between the two countries. In addition, each converter station can manage up to 300 Mvar of reactive power at the corresponding ac grid bus. Since, this MMC-HVdc-based link holds the dc power transmission rating record, the parameters of the INELFE terminals were used for studying the details of the MMC in this thesis. The converter details are presented in Table A.1.

Table A.1: Circuit Parameters used in simulation

Parameters	Notation	Value
Number of submodules/arm	N	400
Rated active power	P	1.0 GW
Rated reactive power	Q	300 Mvar
Line voltage	U_{LL}	333 kV
dc-bus voltage	U_{dc}	± 320 kV
Cell capacitance (35 kJ/MW)	C	9.4 mF
Nominal submodule voltage	U_{SM}^{N}	1.76 kV
Rated submodule voltage	U_{SM}^{R}	4.5 kV
Arm inductance	L_{arm}	50 mH
Grid Inductance	L_{grid}	50 mH
Parasitic resistance of the inductors	R	0.1 Ω
Sampling frequency	f_s	10 kHz
IGBT device model	ABB 5SNA2000K450300	

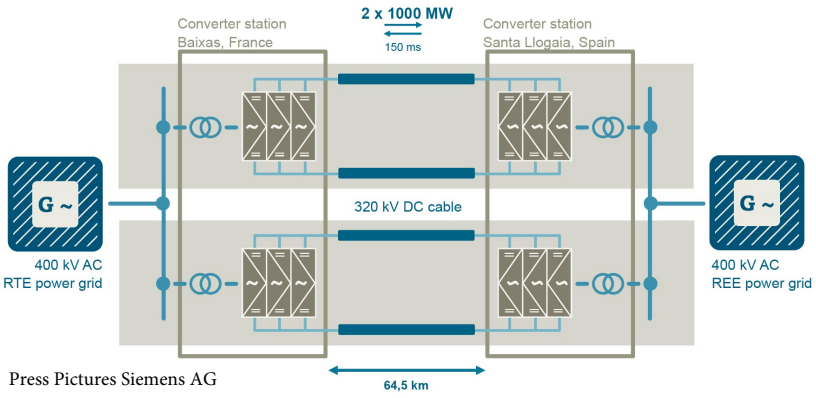
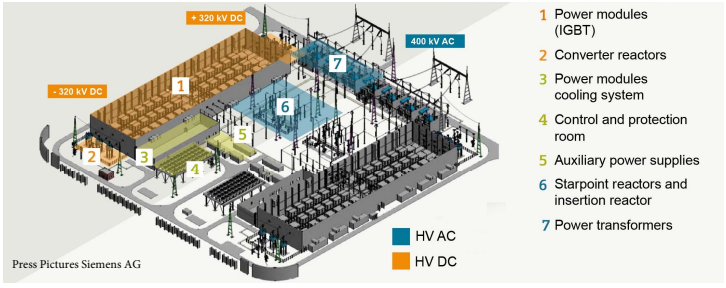


Figure A.1: Global scheme of the INELFE interconnector.

(a)



(b)

Figure A.2: Santa Llogaia substation of the INELFE interconnector: (a) panorama view and (b) layout diagram.

Appendix B

Controllers design

Once a mathematical model is discovered that describes the behavior of a process, the design of the corresponding the control scheme becomes feasible. This appendix presents the methodology followed to design a controller $C(s)$ in such a way that the corresponding system's transfer function $T(s)$ has a first or second order response, whenever it is excited by a step function. A classical feedback-based control scheme is depicted in Figure B.1.

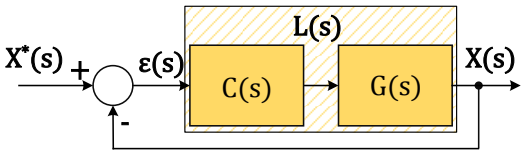


Figure B.1: Classical closed-loop control system defined in Laplace domain.

where:

$X^*(s)$	is the target value of the variable $X(s)$,
$\epsilon(s)$	is the error between target and actual values of $X(s)$.
$C(s)$	is the controller's transfer function,
$G(s)$	is the transfer function of the process requiring control,
$L(s)$	is the open-loop transfer function ($\epsilon(s)$ to $X(s)$).

The closed-loop transfer function of a system is typically defined as:

$$T(s) = \frac{L(s)}{1 + L(s)} \tag{B.1}$$

The classification of the system's transfer function $T(s)$ in this thesis was based in first and second order. As the name suggests, this classification concerns the response behavior of the system, which will be detailed in the following sections.

B.1 First order systems

In order to achieve a first-order-based closed-loop system response, $T(s)$ should be defined as (B.2). Under these circumstances the open-loop transfer function $L^*(s)$ should be consequently defined as (B.3), which is emphasized in Figure B.2.

$$T(s) = \frac{X(s)}{X^*(s)} = \frac{1}{\tau s + 1} \tag{B.2}$$

$$L^*(s) = \frac{1}{\tau s} \tag{B.3}$$

where τ is the time constant of the system response.

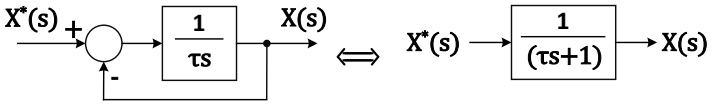


Figure B.2: Block diagram of a generic first order response system.

The first-order systems are mathematically described as exponential functions in time domain (B.4). Whenever a transfer function with the form (B.2) is deduced, the only element requiring to be designed is the corresponding time constant τ. The time constant value influences the behavior of the system response as illustrated in Figure B.3. As the time constant becomes smaller the system responds faster to a step-based excitation. By defining a steady-state band of $\pm 2\%$ around the final value of the transient response $x^*(t)$, the relation between the closed-loop system time constant and the correspondent settling time T_s is deduced in (B.5).

$$\frac{X(s)}{X^*(s)} = \frac{1}{\tau s + 1} \rightarrow X(s) = \frac{1}{\tau s + 1}\frac{1}{s} \xrightarrow{\mathcal{L}^{-1}} x(t) = 1 - e^{(-t/\tau)} \tag{B.4}$$

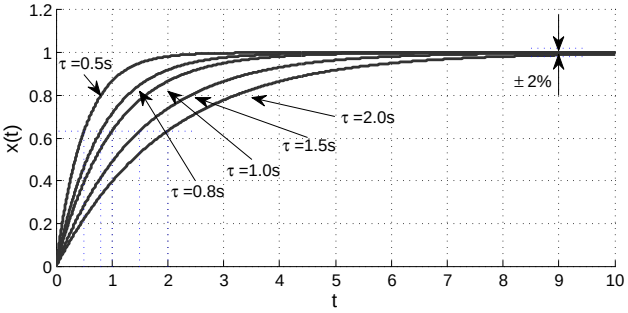


Figure B.3: Impact of the time constant on the system behavior.

where $\mathcal{L}^{-1}$ is the inverse Laplace operator.

$$\begin{aligned} x(t) &= 1 - e^{(-t/\tau)} \\ x(T_s) &= 1 - 0.02 \quad \Rightarrow \quad T_s = -\tau ln(0.02)) \\ &\approx 3.91\tau \end{aligned} \tag{B.5}$$

Thus, as the previous equation suggests, according to the desired settling time T_s for a closed-loop system, the value of τ is directly given by $T_s/3.91$ s. As a consequence, it can be determined the constants of the controllers in such a way that the open loop transfer function is given by $(1/\tau s)$.

Next, lets assume that the process $G(s)$ is required to be controlled with the controller $C(s)$, as defined in (B.6) and presented in Figure B.4.

$$G(s) = \frac{b}{s+a} \qquad C(s) = k_p + \frac{k_i}{s} \tag{B.6}$$

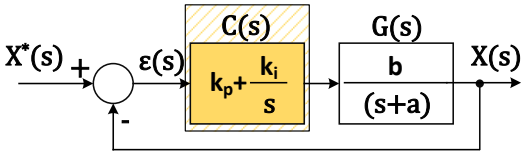


Figure B.4: Block diagram of a typical control scheme used in the thesis.

According to what was previously argued, in order to obtain a first order response on the presented closed-loop system, the open-loop trans-

fer function $X(s)/\epsilon(s)$ should be equal to (B.3). Under these circumstances, the constants of $C(s)$ should be designed as:

$$\frac{X(s)}{\epsilon(s)} = C(s)G(s) = L^*(s)$$

$$\left(k_p + \frac{k_i}{s}\right)\left(\frac{b}{s+a}\right) = \frac{1}{\tau s} \rightarrow \begin{cases} k_p = \dfrac{1}{\tau b} \\ \\ k_i = \dfrac{a}{\tau b} \end{cases} \tag{B.7}$$

B.2 Behavior of second order control systems

To reach a second-order closed-loop-based transfer function $T(s)$ (B.8), the required open-loop transfer function $L^*(s)$ should be accordingly defined as (B.9) (see Figure B.5).

$$T(s) = \frac{X(s)}{X^*(s)} = \frac{\omega_0^2}{s^2 + (2\zeta\omega_0)\, s + \omega_0^2} \tag{B.8}$$

$$L(s) = \frac{\omega_0^2}{s^2 + (2\zeta\omega_0)\, s} \tag{B.9}$$

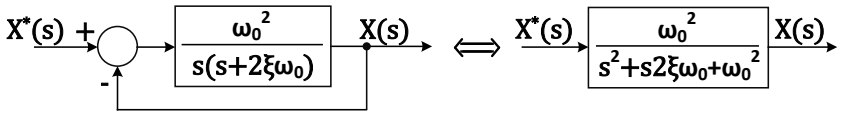


Figure B.5: Block diagram of a second order system.

The dynamic behavior of a second order system can be described according to the damping ratio ζ and the natural frequency response ω_0 parameters. The second-order response of $T(s)$ to a step change in $X^*(s)$ is classified according to ζ as:

- $\zeta = 0$, the system response is designated as *undamped*. As the name suggests, the system starts to perpetually oscillate whenever the $X^*(s)$ value is modified.

- $0 < \zeta < 1$, the system response is designated as *under-damped* and the transient response trends to $X^*(s)$ with an oscillatory behavior.

- $\zeta = 1$, the system response is critically-damped.

- $\zeta > 1$, it is obtained an over-damped system response.

Figure B.6 shows the family of $x(t)$ signals in response to the unit step change $x^*(t)$, for a selection of ζ values ($\omega_0 = 5$rad/s).

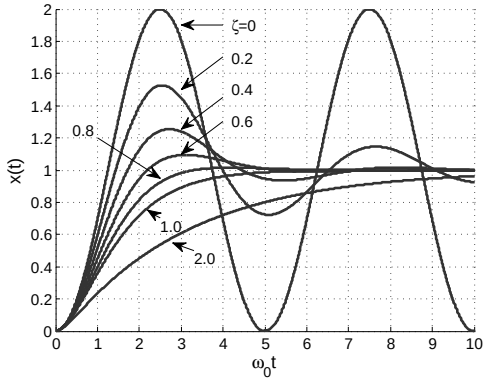


Figure B.6: Impact of the damping ratio to the step response.

As the damping ratio increases the system responses become more damped. Furthermore, as shown in the figure, for the under-damped system response with ζ varying from 0.6 to 0.8 rapidly approaches the steady-state condition.

Several combinations of ζ and ω_0 lead to different responses and should be designed in accordance with specific requirements as: rising time (t_r), peak time of the first overshoot (t_p), settling time (T_s) and overshoot (OS in %) (see Figure B.7). The second-order-based control loops used in this work were designed to have a under-damped behavior, whose design factors treated were the maximum overshoot allowed in the system's response and the corresponding settling time.

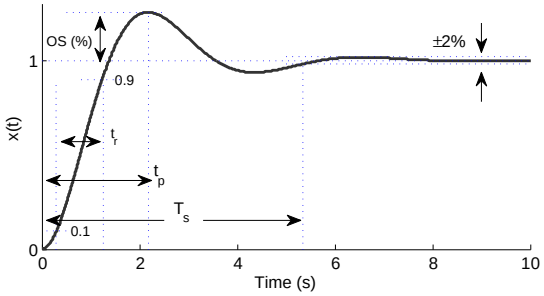


Figure B.7: System response $x(t)$ to a normalized step change at $x^*(t)$.

Taking into consideration that the closed-loop response $x(t)$ reach the steady-state operation whenever inside the $(x^*(t) \pm 2\%)$ band, the values of ζ and ω_0 are respectively given by (B.10) and (B.11) [193].

$$\zeta = -\frac{\ln\left(OS/100\right)}{\sqrt{\pi^2 + \ln^2\left(OS/100\right)}} \tag{B.10}$$

$$\omega_0 = -\frac{\ln\left(0.02\sqrt{1-\zeta^2}\right)}{\zeta T_s} \tag{B.11}$$

Over the thesis some block diagrams were presented in which the process requiring to be controlled is characterized by a first-order model $G(s)$ (B.6) and the corresponding output was managed as the generic scheme illustrated in Figure B.8.

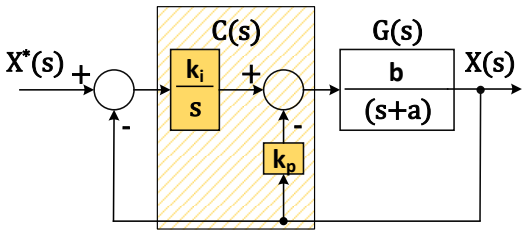


Figure B.8: Block diagram of a generic second order response system.

The behavior of the closed loop system presented in the previous figure is characterized by a classical second-order approach (B.12).

$$\frac{X(s)}{X^*(s)} = \frac{k_i b}{s^2 + s\,(bk_p + a) + k_i b} \tag{B.12}$$

To meet the design criteria, specifically the system's damping ratio (B.10) and natural frequency response (B.11), the constants k_p and k_i assigned to the controllers (B.12) should be accordingly defined as:

$$\begin{aligned} \frac{X(s)}{X^*(s)} = \frac{k_i b}{s^2 + s\,(bk_p + a) + k_i b} = \frac{\omega_0^2}{s^2 + 2\zeta\omega_0 + \omega_0^2} \Rightarrow \\ \Rightarrow \begin{cases} k_i b = \omega_0^2 \\ bk_p + a = 2\zeta\omega_0 \end{cases} \end{aligned} \tag{B.13}$$

Appendix C

Notch filter design

The generic transfer function $H(s)$ of a band-reject or notch filter in the Laplace domain is given by (C.1) [194].

$$H(s) = H_0 \frac{s^2 + \omega_z^2}{s^2 + \frac{\omega_n}{Q} s + \omega_n^2} \tag{C.1}$$

where H_0 is the gain of the filter at ω=0 rad/s. The ω_z and ω_n are the so called zero and notch frequencies and Q is the quality factor of the filter.

Depending on the relation between the zero ω_z and notch ω_n frequencies, different filter designs may be obtained. The three cases are enumerated below and presented in the Figure C.1.

- $\omega_z > \omega_n$: a low-pass notch filter is attained. It is characterized by amplify the low frequencies and filter the zero frequency;
- $\omega_z = \omega_n$: a standard notch filter is obtained. It present an unitary gain at low and high frequencies and its main function is to reduce/eliminate the notch frequency from the spectrum;
- $\omega_z < \omega_n$: a high-pass-based notch filter is accomplished. In this scenario, the low frequencies are cut down whereas at the high frequencies the filter presents an unitary gain.

In the thesis, the standard notch filter was considered to reduce/eliminate some harmonic frequencies from the measurement of particular variables to improve the MMC control. In accordance with the transfer function

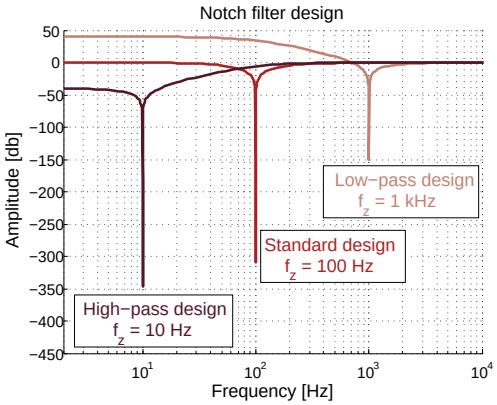
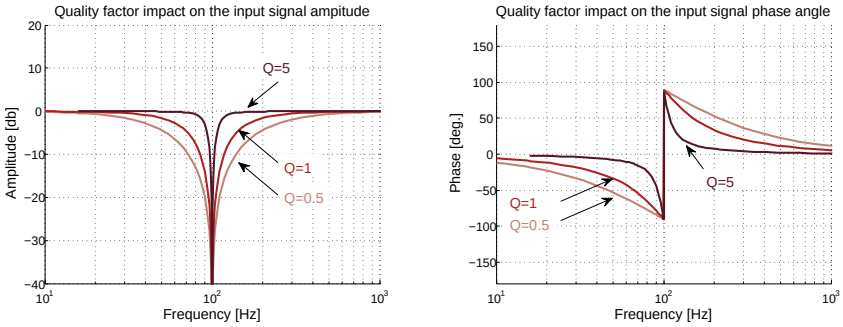


Figure C.1: Notch filter design types.

of the notch filter, besides the design of the notch frequency ($\omega_z = \omega_n$), it was also designed the quality factor of the filter. The quality factor influences the performance of the filter, as illustrated in the Figure C.2.



(a) (b)

Figure C.2: Quality factor Q impact on the filter's input signal: (a) magnitude and (b) phase angle.

As illustrated, as the quality factor of the filter is increased, the band-rejection of the filter becomes narrower and the phase angles of its input signals become less perturbed. As a result of the narrower rejection band and the phase angle change, the quality factor is being also acting on the transient response of the filter. Whenever a input signal of the

filter $x(t)$ suffers a step-change, the dynamic behavior of the output response of the filter $y(t)$ is affected by Q, as exhibited in the Figure C.3.

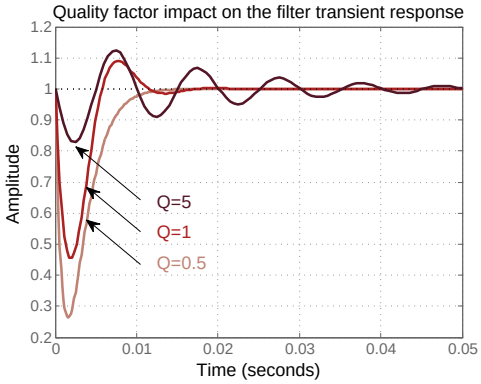


Figure C.3: Quality factor impact on the notch filter transient response.

As presented in the previous figure, for a quality factor of 0.5, the notch filter presents a damped response. In contrast, as the Q factor is increased, more oscillating becomes its response.

The quality factors comprehended between 0.5 to 0.7 were considered to have a good compromise between the filtering and dynamic behavior features, which were the acceptable values used in the thesis.

Appendix D

Publications

This section presents the publications related to the specific topics of this thesis the author has contributed to.

Journal papers

Submitted - Included in the thesis

J1 Abel Ferreira, Oriol Gomis-Bellmunt, "Modular Multilevel Converter losses model for HVdc applications", accepted for publication in Elsevier Electrical Power System Research, Jan., 2017.

J2 Abel Ferreira, Carlos Collados, Oriol Gomis-Bellmunt, "Modulation Techniques applied to Medium Voltage Modular Multilevel Converters for Renewable Energy Integration", submitted to Elsevier Renewable and Sustainable Energy Reviews, Jan., 2016.

J3 Abel Ferreira, Oriol Gomis-Bellmunt, "HVDC-based modular multilevel converter in STATCOM mode", submitted to IEEE Transactions on Power Delivery, Jan., 2017.

Conference papers

Published - Included in the thesis

C1 Abel Ferreira, Oriol Gomis-Bellmunt, Miquel Teixidó, "Modular multilevel converter modeling and controllers design", *European Conf. on Power Electronics and Applications (EPE'14-ECCE Europe)*, Lappeenranta (FIN), 2014.

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