Nanomechanical structures are defined using EBL. The complete process consists of EBL, metal deposition, lift off, RIE and wet etching. A variety of resonating structures are fabricated on different substrates. Discrete devices serve to establish the EBL design and exposure conditions, metal deposition and etching processes parameters. Combination with UV lithography facilitates the electrical characterization of device performance. A procedure for precise aligment is established. EBL is used to define nanomechanical structures monolithically integrated into CMOS circuitry. CMOS enhances the resonator signal for high sensitivity applications. A complementary approach using FIB direct machining is also presented. Both methods are adapted to keep the integrity of the CMOS circuitry.

4 Fabrication of nanomechanical devices

4.1 Introduction to nanomechanics

Mechanics as a discipline deals with the response of structures to applied forces. The working principle is easily visualised in terms of energy. The whole process can be treated in terms of the accumulation of applied force in the form of potential energy. Ideally, this energy is converted to movement. The motion of the mechanical element is determined by the structure shape, mass, dimensions, material and external forces. For clamped elements, there are two main displacement modes, dynamic (vibration) or quasi static (deflection).

Vibration consists of oscillation about an equilibrium point. In the resonance state, the amplitude of vibration is maximized at a certain frequency. The efficiency of the energy conversion is measured in terms of the quality factor, Q, that quantifies the amount of dissipated energy. Indeed, real structures are subject to frictional forces.

Deflection is the response of the mechanical structure to loading forces. It causes structure deformation from the equilibrium point and, in the eleastic regime, it returns to the origin if no force is applied. An excess in the applied force may cause the break or permanent deformation of the movable element, since plastic range is reached.

Mechanical devices are used in combination with a transducer, to constitute the mechanical system. Transduction is the conversion of the movement measurement to another signal type, typically electrical or optical. It includes both the movement excitation (actuation) and the sensing operation (detection). Electromechanical systems are formed by mechanical elements coupled to electronics circuits using an electromechanical transducer, this is, conversion of electrical energy into mechanical energy (motion or displacement), or viceversa. The miniaturization of mechanical elements and their combination with microelectronics evolved in the

microelectromechanical systems (MEMS). MEMS comprise a great number of daily used applications (1).

The feasibility of higher resolution in lithography and fabrication methods allows to reduce the mechanical structures down to the nanoscale range (2). As an alternative method, bottom up approaches can be introduced to fabricate this kind of systems. Hence, nanoelectromechanical systems (NEMS) are feasible. The interest of NEMS is not only seen as the natural evolution of MEMS miniaturization, but also may support the research in nanoscience. For mesoscopic or nanoscale devices, surface effects begin to be significant for the device performance and models based on macroscopic mechanics may not be valid anymore. This, far from being a limitation, can be exploded for a great number of applications, ranging from higher resolution sensing to fundamental science (3).

The ideal type of NEMS would be those where monitored phenomena exhibit large and measurable changes for small displacements of the nanomechanical structure. In consequence, higher frecuencies and weak applied forces generate faster and low power devices, in addition to provide spatially localized response. The possibility to precisely tailor their geometry allows to determine the motion direction.

However, the complete control over the NEMS technology encounters three main challenges. The magnitude of the displacement signals usually is directly proportional to the structure dimensions, the mechanisms that involve can differ from the controllable or understandable processes and system fabrication is often difficult to be absolutely reproducible or controllable. In practice, dissipation and noise play a central role in the NEMS characterization and improvement and the development of valid applications.

One of the typical nanomechanical device is the doubly clamped beam. As an example, the description of the mechanical model is included and it serves to illustrate the resonating structure performance and specifications that are crucial. Also, the dissipation and noise sources are presented, specially, in relation to the transduction system. Hence, this general overview ought to support the relation of results presented in this chapter. The results discussion is focused only in the fabrication process and, specifically, based on EBL as the patterning technique.

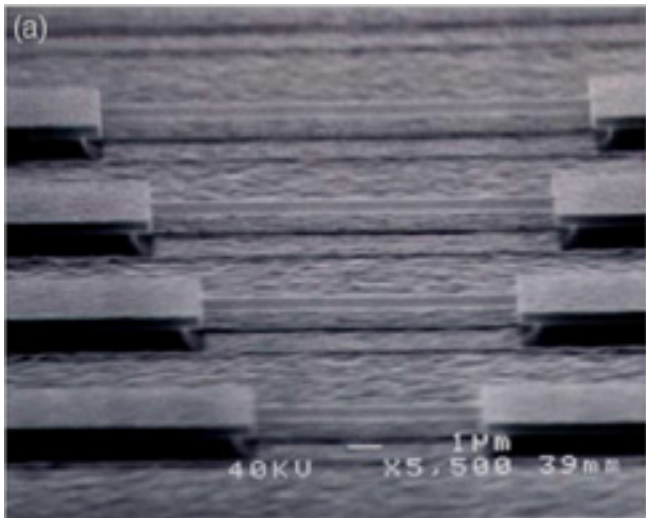

Figure 4.1 Example of doubly clamped beams. Done in the same structuring material and equivalent width (w) and thickness (t), the difference in lenght (l) implies different natural resonance frequency for each structure ($\omega_0 \alpha\ 1/l^2$), from reference (3).

The beam motion can be described as a 1D (out of plane) harmonic oscillator, which displacement, x(t), is expressed by,

$$\frac{d^2x(t)}{dt^2}+\frac{\omega_0}{Q}\frac{dx(t)}{dt}+\omega_0{}^2x(t)=\frac{f(t)}{m_{eff}} \tag{4.1}$$

where, f(t) is the steering force, m_{eff} is the effective mass, ω_0 is the resonance frequency and Q the quality factor. In first approximation and in the vicinity of a mode resonance frequency, they are given as,

$$\begin{aligned} m_{eff} &= 0.735\cdot l\cdot t\cdot w\cdot \rho, \\ \omega_0 &= 2\pi\cdot(1.05)\sqrt{\frac{E}{\rho}}\frac{t}{l^2} \\ k_{eff} &= 32E\cdot t^3\frac{w}{l^3} \end{aligned} \tag{4.2}$$

where, l, t, w are the dimensions, E is the Young's modulus, ρ is the mass density of the beam and k_{eff} is the stiffness (4). The motion of the element is determined by the dimensions and materials that constitute it and it is restricted by the intrinsic energy dissipation and non idealities.

Applying the same development to the simplest mechanical structure, the motion characteristics for one side clamped beam (cantilever) are expressed as,

$$\begin{aligned} \omega_0 &= 2\pi(0.17)\sqrt{\frac{E}{\rho}}\frac{t}{l^2} \\ k_{eff} &= \frac{2}{3}Et^3\frac{w}{l^3} \end{aligned} \tag{4.3}$$

Scaling down the dimensions of the mechanical element leads to important consequences on their operation. In special, resonance frequency is inversely proportional to the size or mass sensitivity scales with the fourth power of length, what is interesting for high frequency applications or in terms of mass sensing resolution, respectively (Figure 4.2).

magnitude	scaling factor
lenght, L	K
area, A	K^2
volume, V	K^3
mass, m	K^3
stiffness, k	K
resonance frequency, f_0	K^{-1}
mass sensitivity, S	K^4

Figure 4.2 Magnitudes expressed in terms of the scaling factor.

The measurement of the motion is possible through the transducer, this is, the actuactor and the sensor. The transduction system is characterised in terms of sensitivity

or resolution: the capability to apply or to detect sufficiently small forces or displacements, respectively. The detection is characterised by the noise level and displacement responsitivity. The influence of the excitation method on the motion (backaction) is also critical, together with the coupling circuit, for the system resolution. The fabrication of the transduction and mechanical element on-chip often represents an improvement for the system performance.

There are two main techniques for the actuation, magnetomotive or electrostatic (capacitive) methods, while detection may be done by magnetomotive, optical, capacitive displacement and piezoresistive or piezoelectric detection and electron tunneling. Description of each one them is included in (1) and detailed description of each noise and dissipation sources can be consulted in (5).

4.2 Fabrication process

One of the key issues of NEMS is the fabrication of the nanomechanical device. In general, this is accomplished with the combination of MEMS micromachining with nanolithographic techniques. Nanopatterning provides the starting point for achievement of controlled submicronic features that are subsequently transferred to the substrate layers. Hence, the 3D movable structure is defined and ready to be connected to the transductor element, which is intended to carry out the actuation and sensing operations.

The general scheme for the fabrication of nanomechanical structures is illustrated in Figure 4.3 (6). EBL is the most commonly used technique for nanolithography in this kind of configurations. The process starts with the resist deposition by spin coating, electron beam exposure and resist development. After this, metal deposition and resist lift off defines the mask for the dry etching that transfers the pattern to the structural layer. The end of the process is the release of the structure by wet underetching of the sacrificial layer.

The use of EBL for patterning represents many advantages that provide an ideal lithographic platform for the NEMS fabrication. Its high resolution is capable of defining features down to the nanoscale if needed. More important, the pattern design flexibility may be very convenient for prototyping, since in these devices design optimization is often essential. In addition, the possibility to precisely align with other lithographic levels in a flexible and compatible way may be also very useful, as it is shown in the following sections. However, direct writing EBL may be limited for a rather low throughput, consequence of the serial addressing of the beam.

The rest of fabrication steps may be also challenging and they ought to be considered for the design of the pattern and also for the complete processing flow. Dry etching is characterised by its anisotropy. However, deep etchings require a robust mask capable of resisting the entire process and a good control over the etching profile, in terms of both directionality and scalloping. More generally, the undercut may be a problem for some configurations and limitations are encountered for etching narrow trenches, small features, etc. For the release of the structure, the main difficulties affect the design of the structure, together with the thickness of the sacrificial layer and etching time. Feature lateral size determines the configuration, but may be reasonable in terms of time and space, for example to avoid clamping structure collapse. In addition to this, drying after wet etching often causes the released structures to stick to the substrate. Some of these aspects and their experimental solution are described more in detail in the next section.

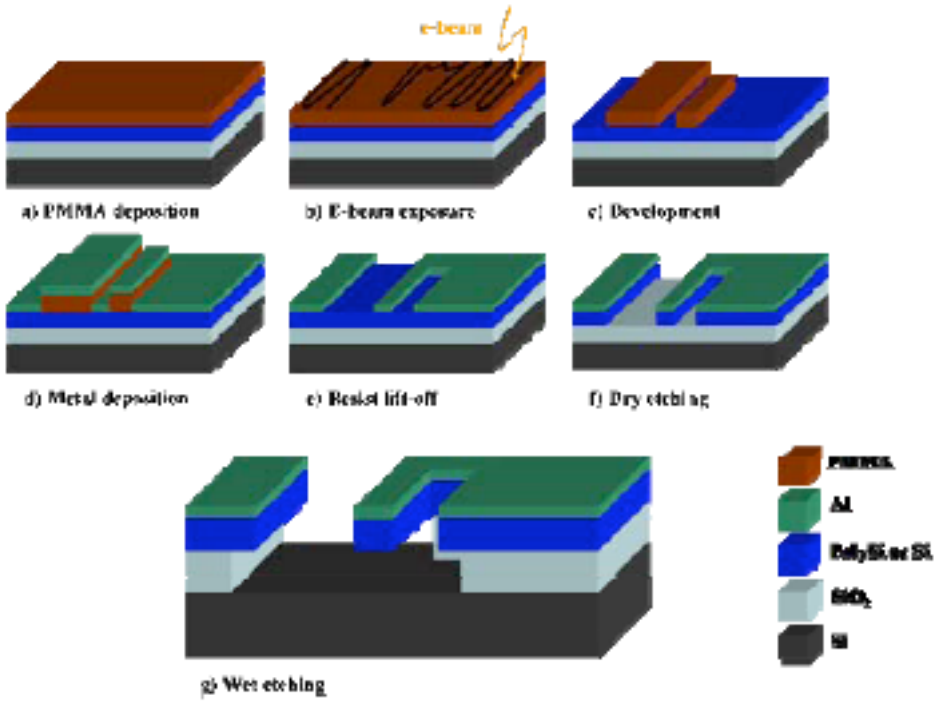

Figure 4.3 Scheme of the whole processing flow for the fabrication of free standing nanomechanical structures. It is based on EBL and metal lift-off, RIE and wet etching.

4.3 Fabrication of discrete nanomechanical devices

In this case, Silicon on Insulator (SOI) substrates are the base material for fabricating the nanomechanical structures. Two different SOI thicknesses are used, 0.6 and 1.5 µm, on 1 µm of SiO_2. The SOI layer is highly n-doped by diffusion of phosphor at high temperature (surface doping: $N_d = 10^{18}$ at·cm^{-3}). Then doping impurities are thermally activated under O_2 and N_2 atmosphere. Therefore, it is not necessary to evaporate a metal for the contacts in the device characterization, after the release of the structures.

Design of nanomechanical structures

A variety of design structures are tested. Cantilevers, quad beams and paddles for lateral, vertical or torsional motion, respectively. In order to optimize their performance, also different pad configurations and device sizes are tested (Figure 4.4). The study of all these parameters and the electrical characterization of the devices has been performed by Julien Arcamone and it is compiled in his thesis (7).

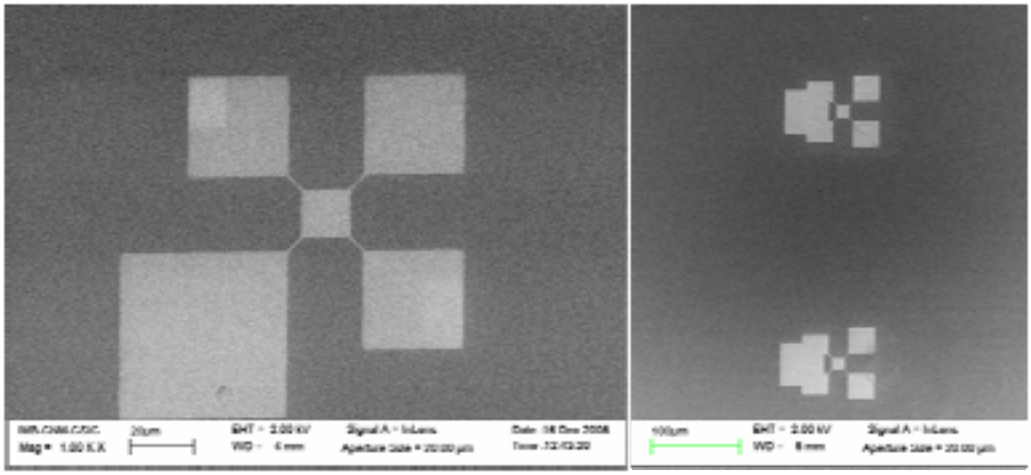

Figure 4.4 Examples of different configurations for quad-beam structures.
EBL pattern flexibility facilitates the optimization of the design.
Several different clampling structures are tested.

Patterning of the structure by EBL

The patterning is based on EBL on a PMMA layer of ~100 nm at 10 keV beam energy and with a WF size of 100 x 100 μm^2. The design feature sizes are not difficult to obtain since they are typically of a few hundred nanometers, but precise definition of the structures in terms of symmetry, edge definition, etc is crucial. A thin layer of Al (24 nm) is deposited and lift off of the resist is performed on warm acetone with ultrasonic assistance and rinse in IPA and water. As can be seen in Figure 4.5, left, resulting structures show a good performance of the EBL in terms of resolution. However, some inaccuracies are also encountered. For example, for the double cantilever configurations, slight differences in the trench and cantilever width appear, even if the design is completely equivalent (Figure 4.5, center). In the case of quad beam structure, incorrecteness of anchor contact with the clampling areas and central plate may make worse the device performance (Figure 4.5, right). These defects are compensated by adjusting the pattern design, the cantilever widths and gap respect to the area, or exposing first the critical parts and enlarging the beams to ensure the proper contact.

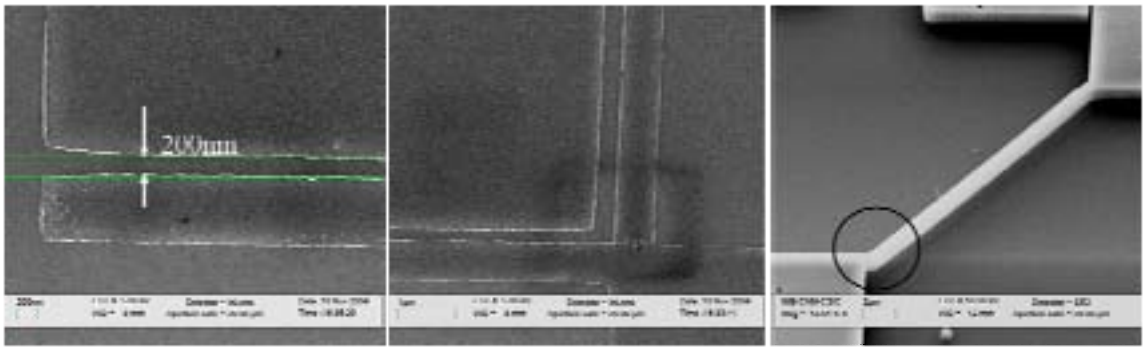

Figure 4.5 Results of EBL in terms terms of accuracy and resolution. In the left, narrow trenches (200 nm) are obtained after metal deposition and lift off. However, uncertainties in the design reliability may cause defects when transferred to the structural layer. In the center, equivalent gap between driver and cantilever in the design is not experimentally obtained without correction (center) and anchoring placement is also ensured (right).

Transference of the pattern to the structural layer by RIE

The next step of the process is the RIE for transferring the metal pattern to the Si layer. The dry etching has been optimised to precisely tune the profile and to achieve a reliable transference of Al pattern. The main difficulties are due to the Si thickness and controlling the width of the trenches. RIE is performed on Alcatel A601E and it is based on a nanoscale plasma etching recipe: alternating cycles of C_4F_6 and SF_6 at room temperature (8). The results in Figure 4.6 show the accuracy of the etching process and the appropiate choice of Al for suitable selectivity and the mask resistance of the thin metal layer.

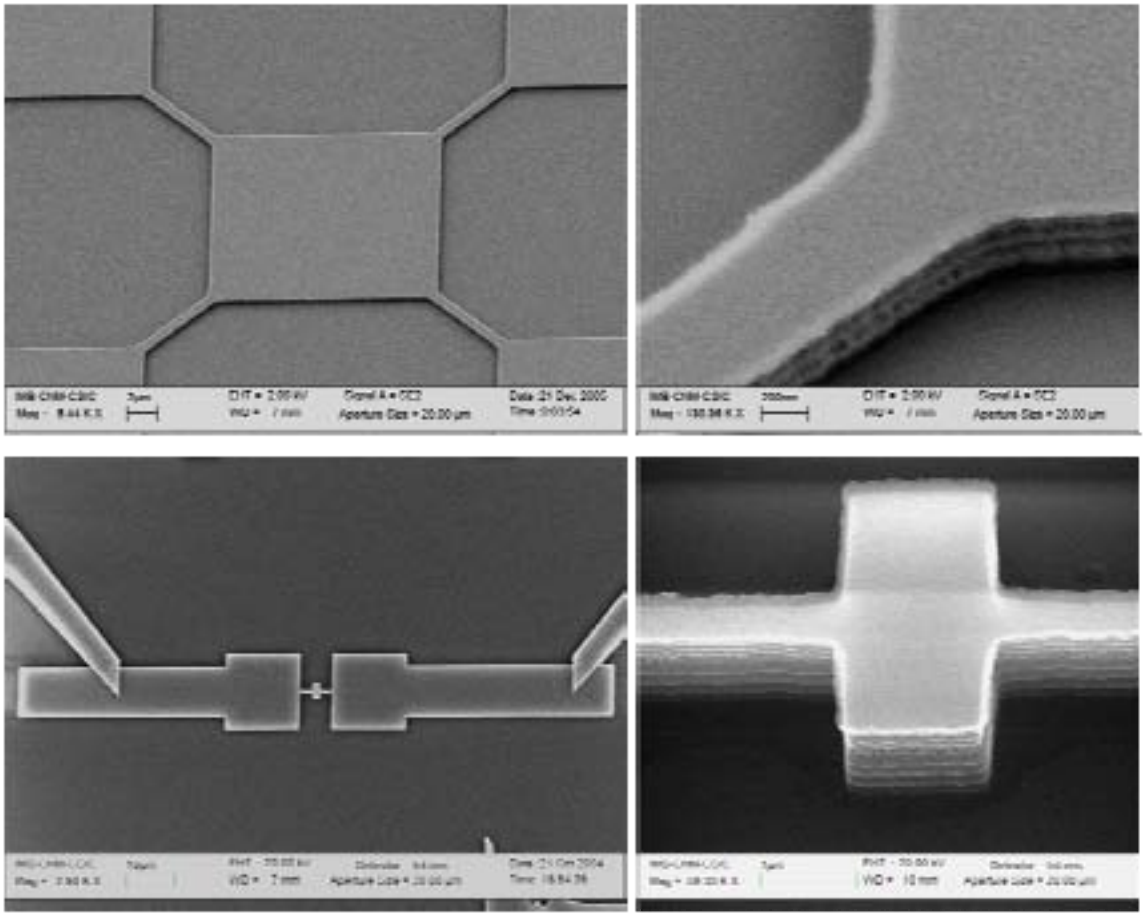

Figure 4.6 Results of optimized RIE process, on quad-beam (top) and paddle (bottom) structures. Both thin (0.6 μm) and thick (1.5 μm) Si layer are controllably etched for vertical profiles and low undercut.

Release of the structure by wet etching

The structure fabrication ends with the release of the movable part. For this, a commercial buffered HF solution, SiOetch (9) is used. The time duration of the immersion determines the etched lateral size and depth. Hence, for the releasing of large central plates long etching times are needed. In addition, certain tendency for the structures to collapse or to stick to the substrate is encountered. This is due to the

surface tension forces that are present during the solvent evaporation (Figure 4.7). The release efficiency is improved with the use of critical point drying (CPD).

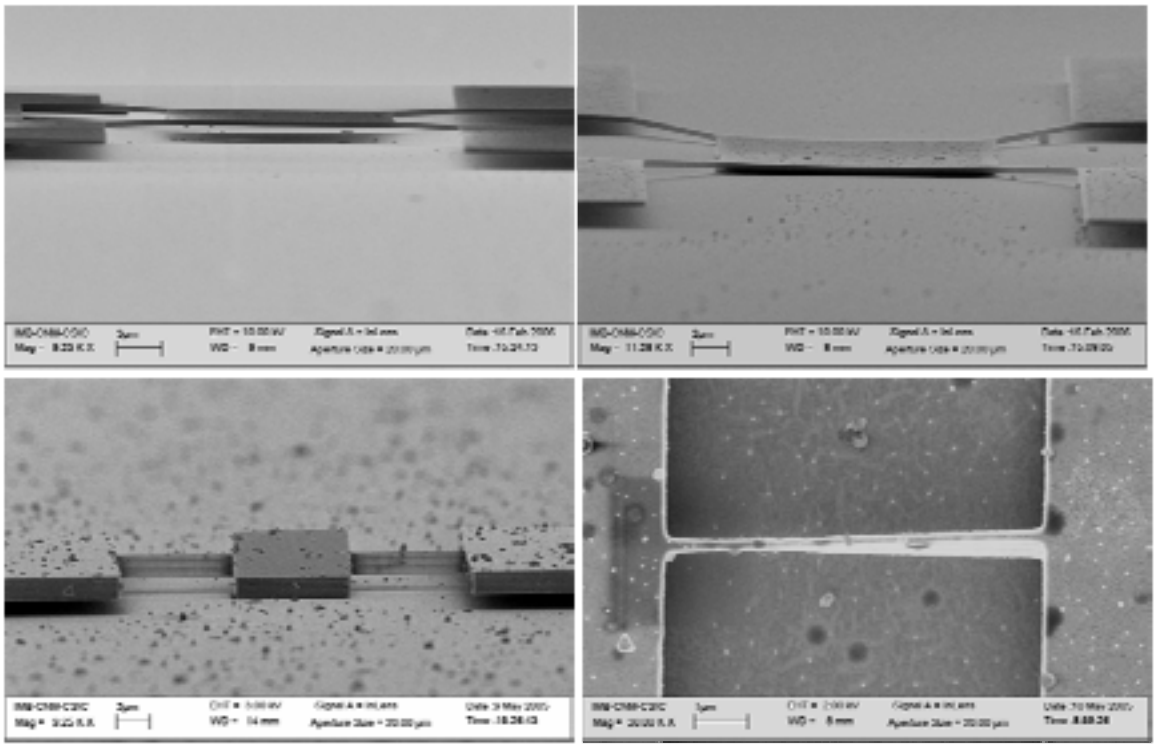

Figure 4.7 SEM images of some examples of results obtained after the release of the nanomechanical structures. The central plate of the quad beam structure is suspended in the top left image. The tendency to stick (quad beam structure, top right) or to collapse (paddle structure, bottom) reduces the fabrication yield.

Combination of EBL with photolithography

Once the fabrication processing flow is established and the optimization of structure design is done, the combination of EBL with photolithography is convenient to facilitate external electrical contacts. First, pads, contact lines and aligment marks are defined by photolithography and metal deposition and lift off. Then, the patterning of the nanomechanical structure has to be defined by, for example, EBL to achieve submicronic features. The characteristics of EBL not only contribute in terms of resolution. It also allow to adapt the positioning and dimensions calibration with the existing structure, in addition to the high flexibility in the pattern design.

Dedicated marks are used to align the EBL with the existing structure that configures the contact pads. Due to the mask design, WF size for EBL is changed to 200 x 200 μm^2. The main difficulty relies on the materials that constitute the marks. RIE is performed in a CMOS compatible equipment, which implies that SEM high contrast materials (e.g. Au) can not be used to define the alignment marks. Due to this, the contrast for the WF alignment is very low and a high number of lines is needed during the scan for the mark recognition (Figure 4.8, left). Aligment procedure starts with the definition of a first reference system (origin and X axis). This allows to blindly move the stage to the relative positions where EBL is to be done. There, mark recognition is performed to finely match position and dimensions of photolithography and EBL (Figure 4.8, right).

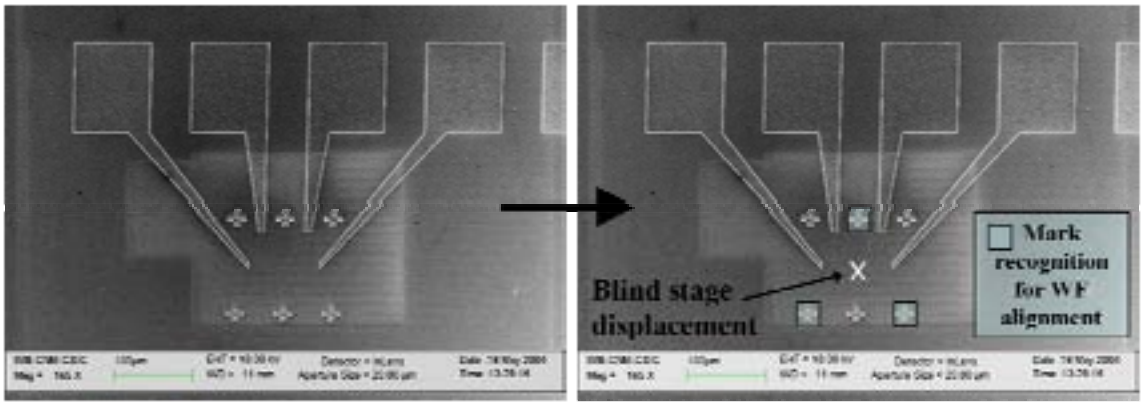

Figure 4.8 In the left, SEM image of the prestructure defined by photolithography and metal lift off. Low contrast with the Al marks is observed. In the right, scheme of the procedure for the EBL alignment.

Combination of EBL with photolithography at wafer scale level

A similar approach is used for fabricating quasi-static nanomechanical structures. In the framework of BioFinger (10), polySi cantilevers are fabricated at wafer scale level with integrated piezoresistance for detection of the vertical deflection. This work has been developed by Guillermo Villanueva and the design and the fabrication details are compiled in his thesis (11). In this case, EBL is used to define cantilevers with submicronic arms width, not reachable by photolithography. The final goal of the project is the direct detection of molecular interactions, which can be obtained because of the increase of sensitivity due to the reduced dimensions.

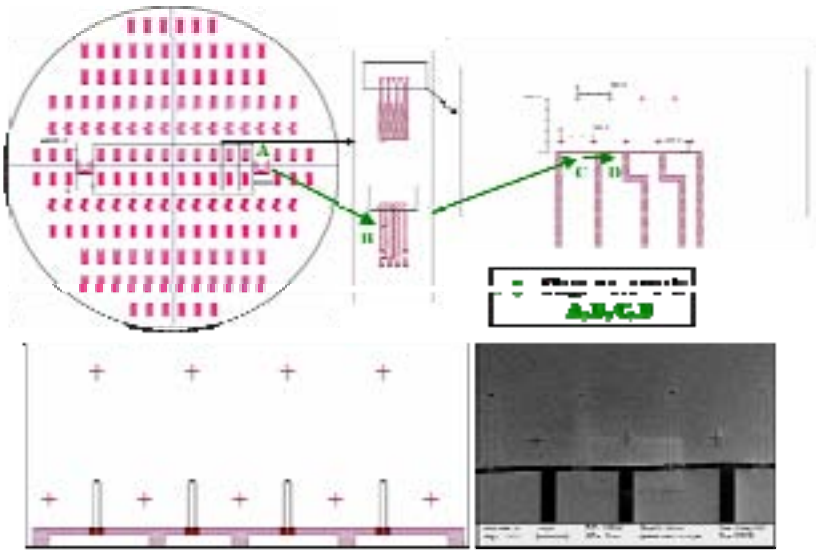

Figure 4.9 Detailed description of the structure and the aligment procedure from the wafer scale level (top, left) to each individual position for EBL realization (bottom left). From A to D, letters represent the stage displacements (from photolithography alignment marks (A), to the reference point for each array (B), to the first array position (C) and to the rest of array positions (D)). SEM image is an example of an array of four identical cantilevers (250 nm in lenght), correctly defined and placed, after lift off step.

The same alignment strategy than in the previous case is used. Thanks to the silicon nitride marks (200 nm thick) that provide higher contrast than aluminum marks, the aligment procedure is easier. Working with wafers implies longer displacements and, hence, the definition of the stage references should be more accurate. First, the photolithography alignments marks are used to establish the origin and to correct the wafer rotation (A). An intermediate point (B) is used to approach to the EBL positions (C and D), where mark recognition is performed for the fine WF alignment (WF size is 800 x 800 μm^2). In total, there are 20 arrays with four positions in each array to be individually addressed and aligned. The important aspect for this system is the correct definition of four identical cantilevers and their precise placement for each array. As can be seen in the SEM image in Figure 4.10, the alignment procedure and the exposure process, at 10 keV, are valid. A thin Al metal layer (32 nm) is used as the mask for the subsequent process steps.

The challenge of this technology relies on the fragility of the structures during the etching and release of the structures. In particular, the transfer to the structural layers is done by RIE on a three layer system (two polysilicon layers, 400 and 200 nm, separated by a thin SiO_2 film, 30 nm). The simulataneous release of all the chips, which contain the cantilever arrays, is realized on the whole wafer from the back side. In Figure 4.10, some final results are shown, where the precision of the feature shape and alignment for the EBL process are observed.

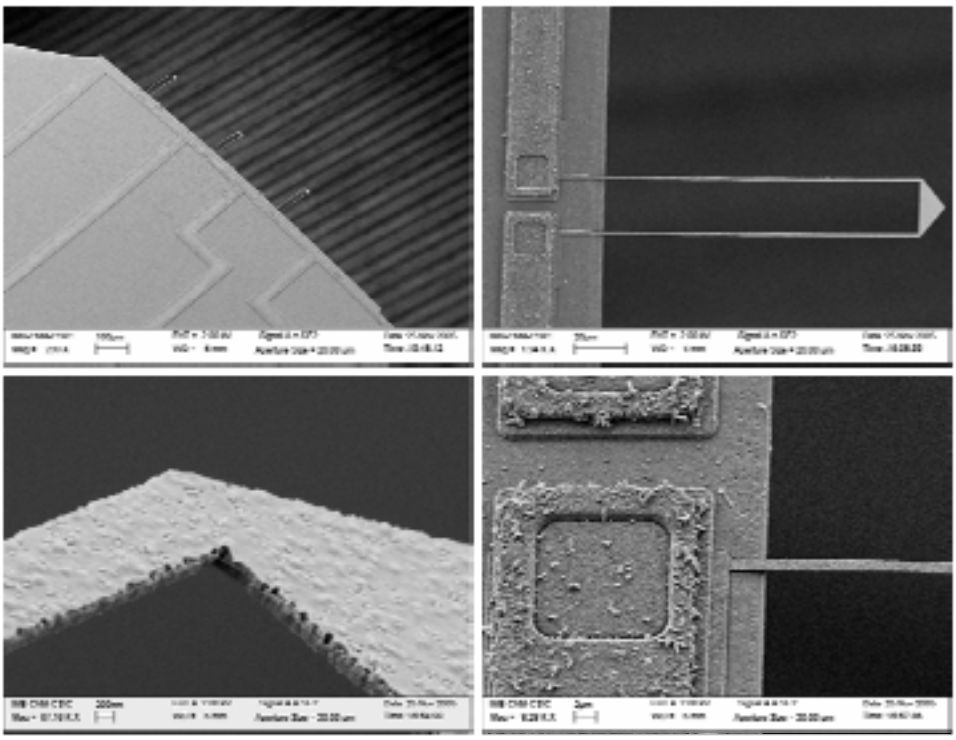

Figure 4.10 SEM images of some results of fabricated nanocantilevers.
The fragility of the structures may cause their break (in the top left image,
a cantilever is missing after release of the structures and manipulation).
Patterning accuracy and precise alignment is also observed in the left side images.

In addition, the performance of the nanomechanical structures has been tested and it proved the piezoresistance of the cantilever. The measurement system is based on the change of the electrical response when applying a bending force with the tip of an

AFM. Simultaneous acquisition of the electrical signal in the deflected cantilever and an identical one allows to establish the dependence of voltage with the deflection, as can be seen in Figure 4.11.

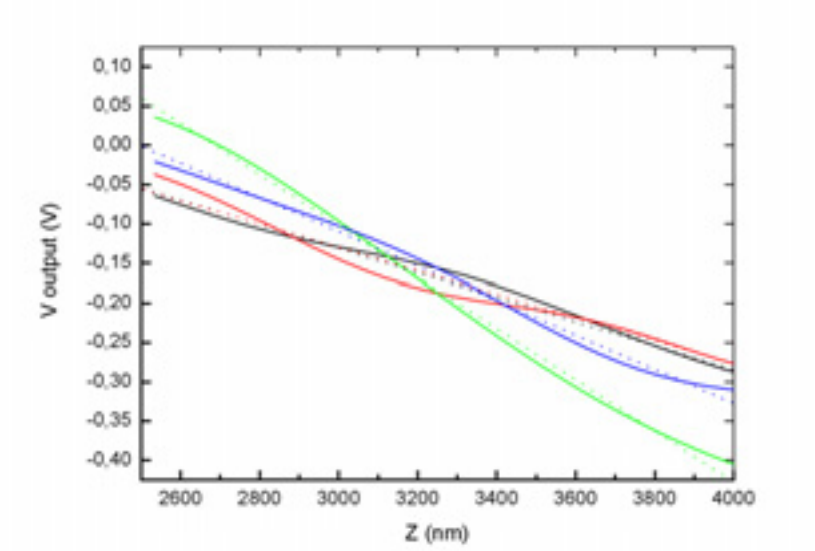

Figure 4.11 Electrical response to the AFM-induced cantilever bending. Cantilevers are 150 µm long and leg width is 500 nm. The force is applied at 15 µm for the anchoring point. Dotted lines correspond to linear fits.

More results of lithography combined fabrication

In the case of the resonating structures defined at chip level, good results are also obtained, as can be seen in Figure 4.12. Both in terms of pattern definition and alignment, the three types of structures (single and double cantilevers, paddles and quad beams) are precisely defined.

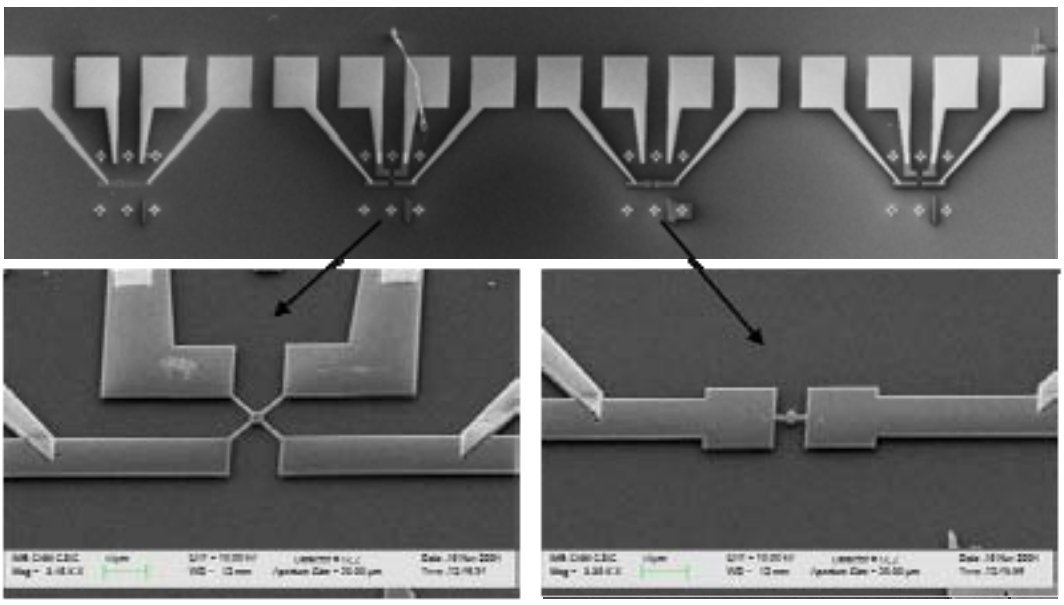

Figure 4.12 SEM images of some results obtained working at chip level. EBL alignment and pattern resolution can be again observed for the different configurations.

The RIE process is good and the release of the structure appears as the main difficulty. In addition to the CPD, AFM can often be used to gently separate the movable part from the driver if sticked (Figure 4.13). Also the long etching times make optically defined pads lines to collapse (Figure 4.13, arrow), which is solved with shorter etching times thanks to the inclusion of small apertures in the central plate (Figure 4.13, bottom right). The performance characteritzation of these devices has been tested by capacitive detection and the results are found in (8).

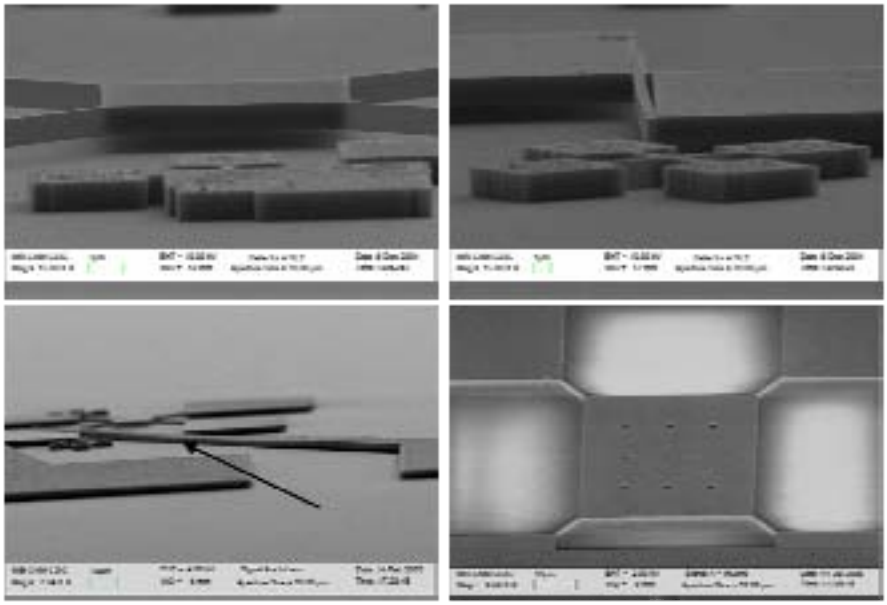

Figure 4.13 Detailed results of the fabrication process (SEM images). The good RIE profile is shown for quad beam and double cantilever structure (top images). The lateral bending of the cantilevers to the driver may be solved by AFM based methods. Long etching times may cause structural defects (the arrow in the bottom left image indicates the collapse of a photolithography defined line). The inclusion of small apertures in the central plate may help to solve this aspect (bottom right).

4.4 Fabrication of CMOS-integrated nanomechanical devices

Technologically, it is possible to fabricate resonating structures that reach natural resonance frecuencies in the GHz range and high quality factors. However, their characterization and their use as high performance sensors is often masked by the noise of the intrinsic signal and limitations in signal transduction (5).

In order to optimise the device performance, the integration of the nanomechanical resonators into a CMOS circuit is proposed. Thus, devices are both actuated and sensed electrically (capacitive read-out). The direct connection with the circuit not only makes the system more portable, but is expected to reduce the parasitic capacitances. This allows to register the oscillation of, for example, very small cantilevers.

Monolithic integration of nanomechanical structures into CMOS by EBL

The complete fabrication process consists of the combination of CNM CMOS circuit technology with the definition of the nanomechanical structure as a post process based on EBL. Definition of the cantilever with dimensions well below 1 μm requires

the use of advanced UV lithography (like Deep UV lithography) or other nanolithography techniques. Advanced UV lithography, although it is very robust and presents a high throughput, it has the drawbacks of un-assumable cost for prototyping and difficulties when patterning non planar surfaces. The use of advanced UV lithography has sense if the cantilever is defined during the fabrication of the CMOS circuit, which is feasible (12) but it limits the flexibility in the design (as for example, the selection of suitable materials).

On the other hand, electron beam lithography presents the advantages of assumable cost, high resolution and it is adapted to pattern surface with some topography. In this case, the definition of the cantilever after being completed the fabrication of the CMOS circuits give additional flexibility to the design either for the selection of materials and processing at chip level. Details of the fabrication of integrated cantilevers on CMOS as a post-process module can be found in (13, 14). A dedicated area, the integration area, is used for the monolithical integration of the resonator. The layers that constitute the CMOS circuit are used to define the structure. Hence, one of the polySi layers acts as the structural layer, whereas the field oxide layer is used as a sacrificial layer for the release of the structure.

After the CMOS circuit fabrication, openings in the pasivation layer are done in the integration areas and the wafers are diced. A PMMA layer is spin coated on the chip for the EBL step. A thin layer of Al (32 nm) is deposited after development and the resist lift off is done. RIE is used to transfer the Al pattern to the polySi layer and the structures are release by wet etching. In order to protect the circuits during the SiO_2 etching, a negative photoresist mask, patterned by UVL is employed (Figure 4.14).

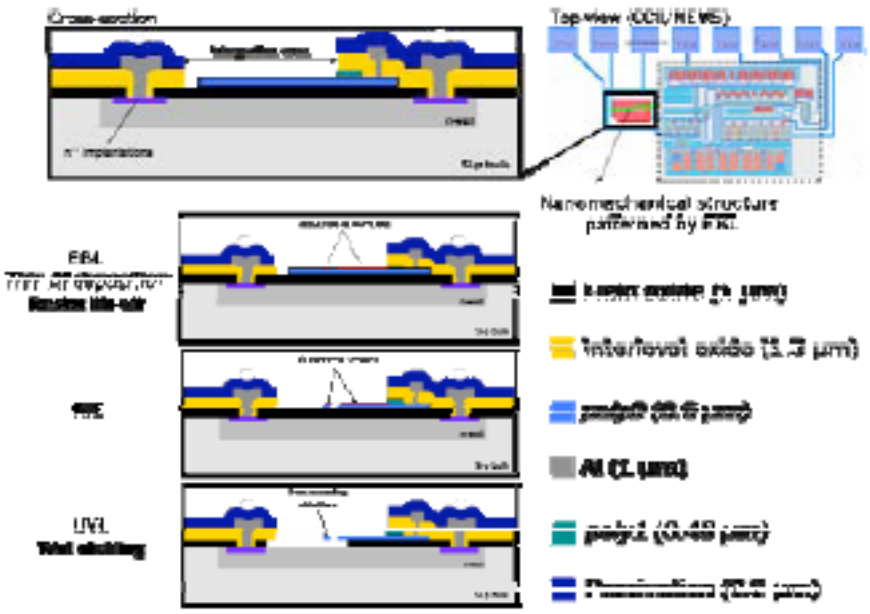

Figure 4.13 Scheme of the main steps for the fabrication of nanomechanical devices into the CMOS circuit by means of EBL.

Issues of EBL on CMOS circuits

The use of EBL to define nanostructures on CMOS circuits encounters three main issues that should be considered: aligment, beam energy and topography. Originally, the design of the chip was oriented to use nanostencil lithography at wafer scale level to define the resonating structures (15). In consequence, there are not dedicated marks that can be used to blindly address the EBL exposure. The previous experience in aligment is used to establish a specific procedure that enables the correct placement of the structures. Starting from the GDS file of the CMOS design, compatible with the Raith software, the coordinates of each integration area are determined. There are 23 positions prepared to be exposed (Figure 4.15). In addition to this, several reference points separated from the circuits are established ($x_{\#}$, in Figure 4.15). These reference marks are chosen among the structures that are defined within the chip. In particular, selected points are not part of the circuits that connect each integration area, but they are close enough to reduce long stage displacements. Additionally, it is convenient that the integration areas to be patterned are placed within the zone delimitated by the three mark sites that have been chosen.

The alignment procedure differs from the previous cases in the importance of the definition of the reference system for the stage movement. First, the corner of the chip is used to define the origin and the rotation of the sample. Then, three reference points are used to precisely establish the UV reference system that determines the stage displacements. As an example, x_1, x_2 and x_3 are used for paterning integration areas from A to I. Stage is blindly displaced to the coordinate of each integration area and exposure is directly executed (WF calibration is previously performed in the chess calibration sample, see chapter 2).

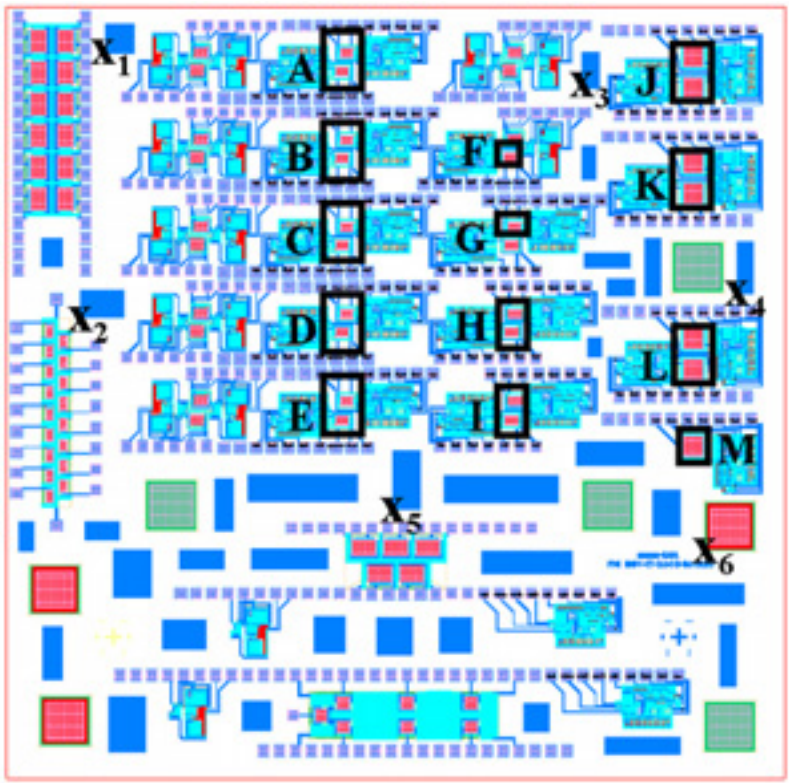

Figure 4.15 Design of the whole chip area. The integration areas are marked in black with letters (A-M), 23 EBL positions, and examples of reference points correspond to $x_{\#}$.

Concerning the beam energy, it is reported that energetic electron beams induce damage in the CMOS circuits (see chapter 6)). Due to this, the possibility to use lower energies to define the structures with no effect on the circuit performance is tested. For 3 keV beam energy on PMMA, the electron range is about 300 nm. As can be seen in Figure 4.16, the simulations of electron trajectories on 100 nm of PMMA on Si show a larger charge confinement in the resist layer for 3 keV beam energy, while for 10 keV a significant fraction of the incoming electrons are stopped along the Si layer.

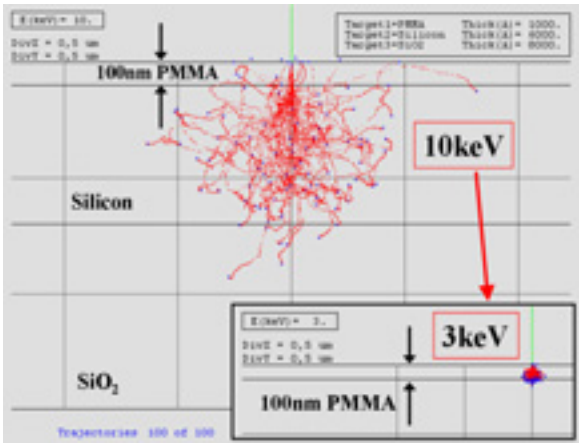

Figure 4.16 Electron trajectories simulation at 10 and 3 keV beam energies in 100 nm of PMMA upon Si layer. The charge confinement at low energy is clearly seen.

The clearing dose and designs are tested to determine the exposure parameters that may allow a good pattern definition. In Figure 4.17, examples of these trials after final optimisation are included. Control over the cantilever width and good edge definition is feasible for this kind of structures at low beam energy (3 keV).

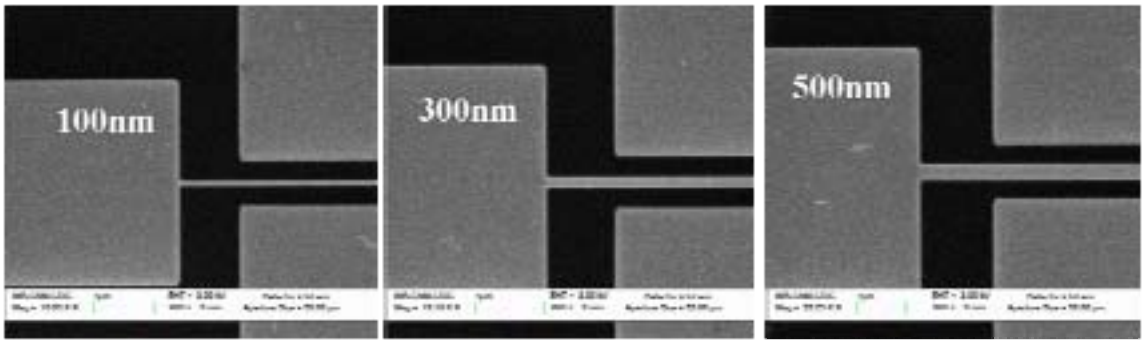

Figure 4.17 SEM images of the set up of EBL patterning at low beam energies (3 keV), after development. Clearing doses are determined and control over the dimensions (cantilever widths are indicated in white) and good edge definition is obtained.

As mentioned, the passivation layer is removed from the surface integration areas in order to permit the post processing for the fabrication of the nanomechanical structure. Due to this, the topography of the chip represents a limitation over the resist deposition control. The standard spin speed (1500 rpm) for depositing the thin layer is used. However, it is possible that thicker or thinner layers are formed for the same spin conditions, if delivered resist is trapped or does not penetrate the hollow area. An excess of resist, added to the limited electron penetration range, may cause that resist is not

completely developed in the edges of the integration areas. As a result, lift off evidences for the disconnection of the structures to the circuit and lowers the fabrication yield (Figure 4.18, right). In addition, the use of a thin layer of Al does not ensure a complete coverage of the steeped profile, which is needed for masking the subsequent dry etching. For this reason, the use of conformal sputtering for the metal deposition is advantageous.

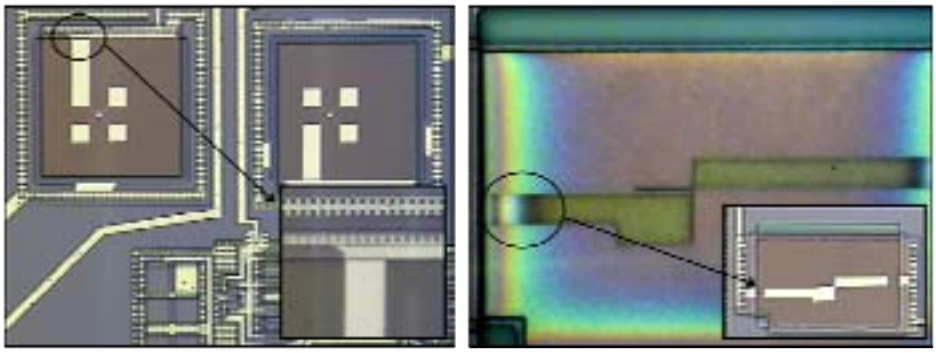

Figure 4.18 Optical images for some results after the development (right) and after the lift off process (left and insets). Good edge contact can be obtained (left), but no control over the resist deposition and low beam energy may limit the possibility to fully expose the resist, mainly in the contact to the circuit (inset of right side image).

A possible solution is the addition of Al contacts by UV lithography previous to the EBL step (Figure 4.19). This strategy is been tested in the framework of project NANOMASS (16), where also nanomechanical structures are integrated into CMOS circuits (17). Even if it is possible to achieve good contact definition (Figure 4.18, left and Figure 4.20, bottom left), the predefined Al contacts ensure the correct definition of the resonator-circuit connection and increases the tolerance in the alignment, more important for small integration areas or complex configurations (Figure 4.19). Hence, the efficiency of the fabrication process is increased.

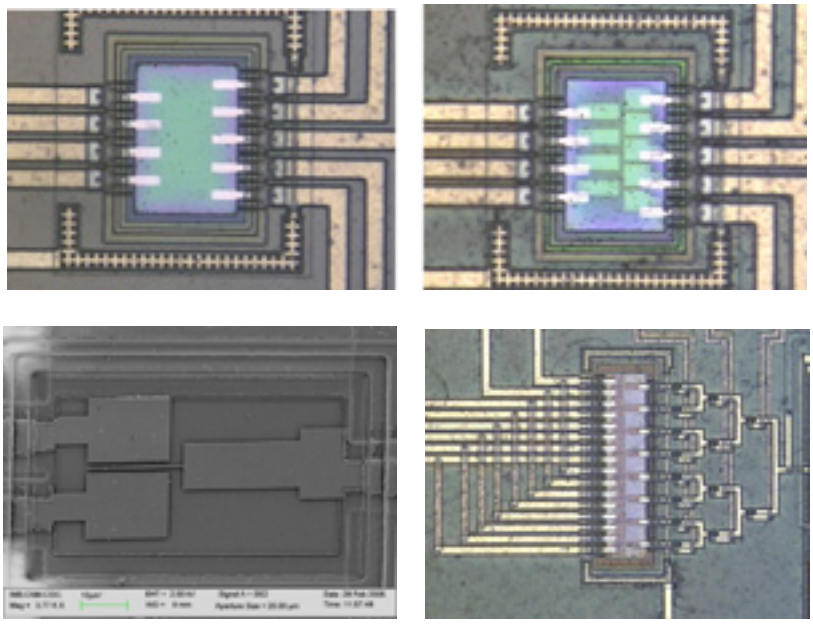

Figure 4.19 Optical images of the integration area with Al precontacts defined by photolithography (top). Even if it is possible to successfully define the contacts only by EBL (bottom left SEM image)

the Al contacts facilitate the patterning, specially for small integration areas and complex designs.

Results of integrated nanomechanical devices

During the release of the structure in wet etching, the rest of the circuit is masked for protecting. Photolithography leaves open only a portion of the integration area, in order to remove the SiO_2 almost only underneath the nanomechanical structure. The alignment tolerances for EBL are larger than Nanomass chips (Figure 4.19), thanks to bigger integration areas and to the design of the circuits contacts (Figure 4.20). However, this additional photolithography, after the EBL-based nanofabrication, limits the freedom degree for the placement of the nanomechanical structure within the integration area.

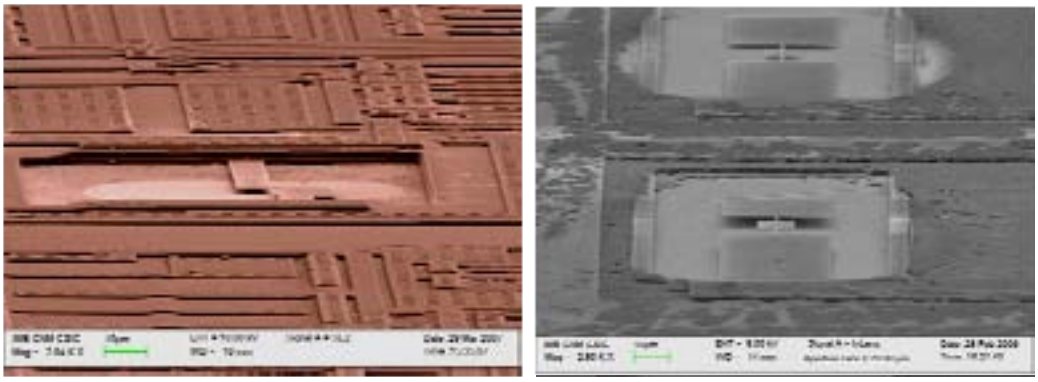

Figure 4.20 SEM images of cantilever (left) and paddle structures (right) after the release of the structures. The epoxy resist mask used for the circuit protection during wet etching is also observed.

Some results of device fabrication are shown in Figure 4.20 and 4.21. Device performances are electrically characterized and used for mass sensing applications. The good functional performance of the system is demonstrated in (8) and (18).

In conclusion, a reliable technology process is established for the realisation of NEMS. Concerning to nanofabrication, EBL is capable of fullfilling the requirements of the process: good pattern definition, precise alignment and compatibility with CMOS circuitry. Also, the difficulties in pattern transfer and release of the structure are solved or adjusted.

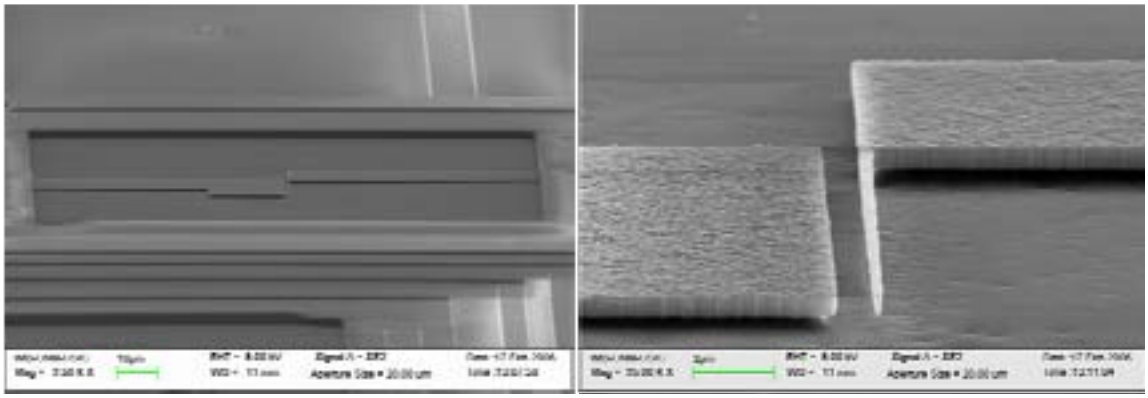

Figure 4.21 SEM images of the final result of a cantilever based device monolithically integrated into the CMOS circuit.

4.5 Focused Ion Beam fabrication combined with Electron Beam Lithography

An alternative method for the fabrication of nanomechanical structures on CMOS chips is proposed. Based on the technology presented above, the fabrication of the cantilevers for lateral motion and capacitive read-out is performed with the machining capabilities of FIB. The focused beam of ions can be used to remove or to deposit material (19). In this case, instead of using RIE, the critical definition of the cantilever width and trench is undertaken by direct structuring with the Ga^+ ions.

Fabrication process by direct FIB machining

This methodology allows to fabricate discrete devices with nanomechanical structure specificacions of higher resolution, this is, narrow cantilevers or small gaps. This is due to the slower etching rate, as compared to RIE, and in situ control of the results. The fabrication processing flow is outlined in Figure 4.22. EBL lithography is used to define the pre-structure that will constitute the cantilever and driver after the FIB milling (obviously, this step could be also accomplished by photolithography, but a dedicated mask would be needed and pattern flexibility for prototyping is then cancelled). Pattern transfer is done again by metal deposition and lift-off and RIE for the etching of the Si layer. Then, FIB is used to directly define the separation of cantilever and driver by cutting the whole Si thickness. Finally, wet etching is used for the nanomechanical structure release.

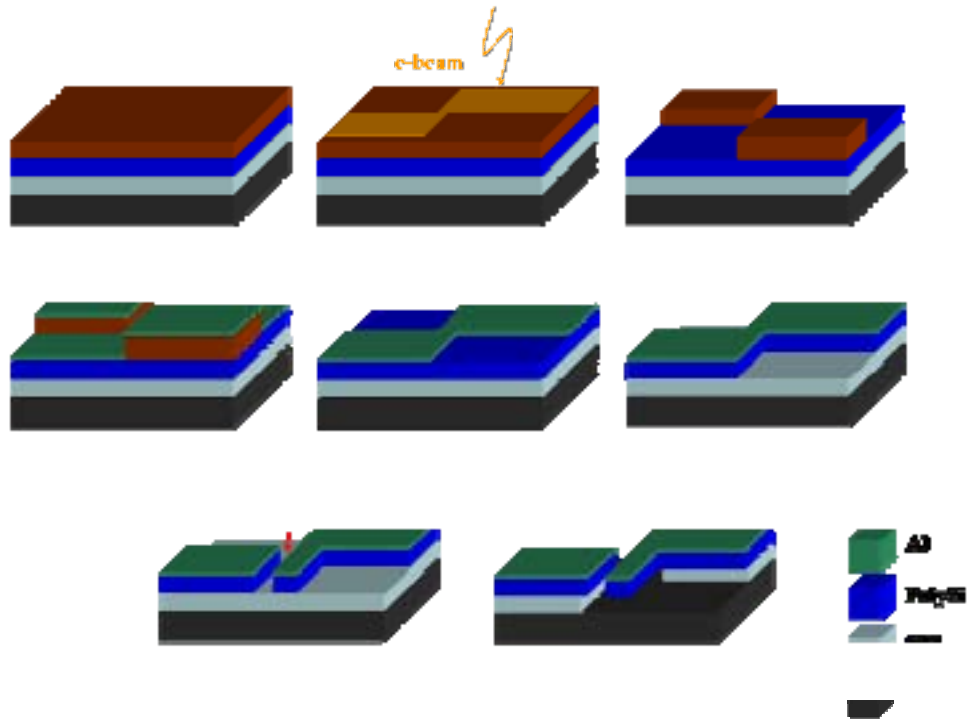

Figure 4.22 Scheme of the fabrication process of nanomechanical structures combining EBL and FIB machining.

Establishment of the FIB procedure

Experimentally, the feasibility of the FIB based process is tested. The FIB equipment is a Crossbeam 1560 XB from Carl Zeiss. Among its most relevant characteristics, it is equiped with a Ga^+ ions column and a field emission SEM, that enables the on-line monitoring of ion beam process.

The fabrication is performed in the same CMOS chips that have been used in section 4.4. These CMOS circuits are designed to actuate the cantilever by electrostatic excitation and to detect the movement by capacitive detection, as described in (20).

First, the beam alignment point is determined in order to make FIB and electron beam coincidental. SEM assesses the movement of the stage to the integration area that is to be machined, but it is reduced as much as possible. Fast FIB imaging at low current (10 pA) is used to define the pattern design on the pre-structure. The beam current during the milling is shifted to medium-low level (100 pA), which means that slow material removal is performed and better milling control is expected. The cutting conditions have been tested previously in analogous structures. As can be seen in Figure 4.23, the possibility to use this strategy to define the structure is confirmed. The release of the structure is analogous to the previous cases and consists of the elimination of SiO_2 underneath the cantilever by means of wet etching.

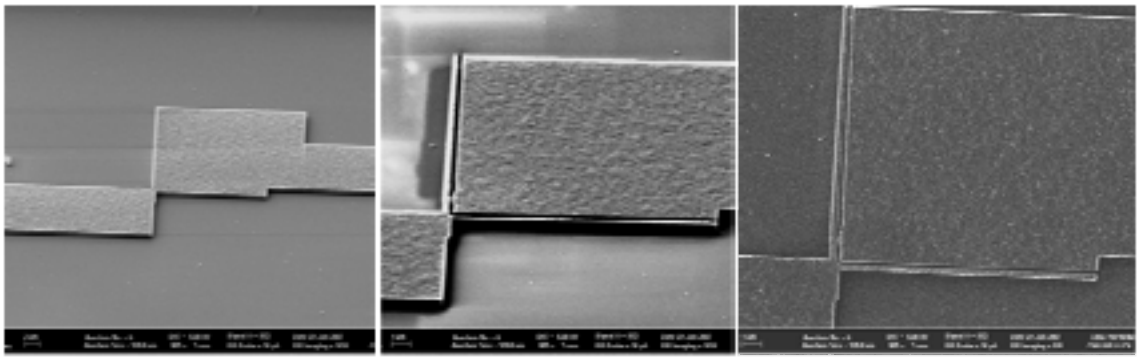

Figure 4.23 SEM images of the pre-structure defined by EBL, metal deposition and RIE (left) and after the cantilever definition by FIB milling (center, tilted image, and right, top view)

Results of FIB based fabrication

The effect of the energetic ion beam (30 keV) on the system is also studied to evaluate a possible damage in the circuits or the characteristics of the integration area (19). For this, different options are tested in different integration areas: SEM imaging, cutting with or without SEM on-line imaging and different cutting configurations. The circuits are then measured and no major modification is observed in their performance.

One of the limitations of the process is the depth determination of the cutting. Milling rate may be slightly variable and strongly dependent on beam current, material, design dimensions, etc. As a result, the achievement of complete milling of the Si layer is not univoquely defined and both over or underetching may occur. However, even with an excess of milling, the CMOS circuit is not modified. In figure 4.23, it is shown the electrical characterization of the resonance spectra of a cantilever fabricated by FIB.

Electrostatic actuation and capacitive readout by the integrated circuit (IC) are used for detecting the oscillations of polysilicon resonators in the MHz range. The resonator is electrostatically driven by a DC+AC voltage. Its readout electrode, electrically connected to the IC input, collects a capacitive current whose, one part is specifically generated by the variation of electrode-resonator capacitance due to the mechanical motion itself. With the aim of reading out this current, a dedicated interfacing CMOS circuit (21) was designed based on a second generation current conveyor (CCII). Basically, the CMOS circuit ensures a constant input voltage biasing, while it amplifies the input current and converts it to an output voltage signal according to the load resistor. We have not found any difference in their performance between before and after FIB processing, as it can be observed in figure 4.23. More details about the circuit can be consulted in (7). Another aspect that difficults the control over the FIB machining relies on the beam drift. In consequence, the patterned result may not correspond with the designed structure.

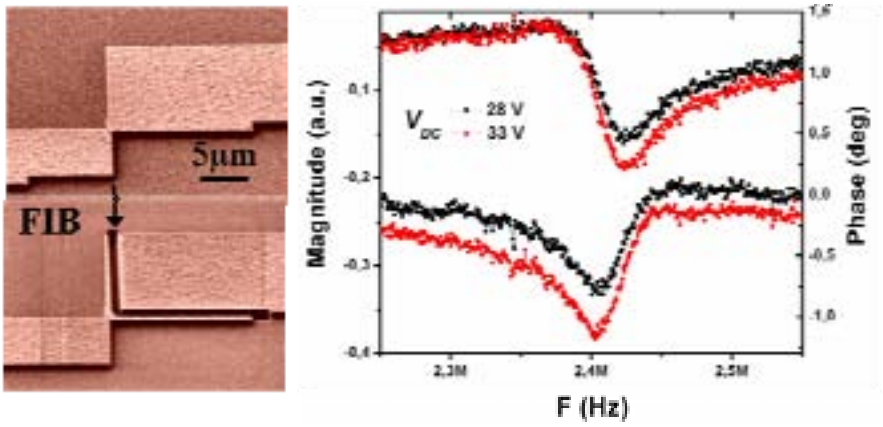

Figure 4.24 In the left, SEM images of the prestructure (top) and after FIB machining (bottom). In the right, the characterization of the released structure performance shows the compatibility and consistency of the processing flow.

In summary, the fabrication of nanomechanical devices by EBL has been described and the complete technology is established and optimized. First, discrete devices are fabricated, which allowed to determine the specific process conditions. Combination of EBL with photolithography facilitates the electrical characterization of nanomechanical device in operation. The main achievement consists of the monolithic integration of nanoresonators into CMOS circuits, which enhances the signal of the nanomechanical element response. Alternative method of fabrication based on FIB is also demonstrated.

References

(1) K. L. Ekinci
Electromechanical transducers at the nanoscale: Actuation and sensing of motion in nanoelectromechanical systems (NEMS)
Small **1** (8-9), 786-797 (2005)

(2) A. Husain, J. Hone, H. W. C. Postma, X. M. H. Huang, T. Drake, M. Barbic, A. Scherer, and M. L. Roukes
Nanowire-based very-high-frequency electromechanical resonator
Applied Physics Letters **83** (6), 1240-1242 (2003)

(3) K. L. Ekinci and M. L. Roukes
Nanoelectromechanical systems
Review of Scientific Instruments **76** (6) (2005)

(4) A.N. Cleland
Foundations of Nanomechanics
Springer-Verlag **ISBN 3-540-43661-8** (2003)

(5) A. N. Cleland and M. L. Roukes
Noise processes in nanomechanical resonators
Journal of Applied Physics **92** (5), 2758-2769 (2002)

(6) H. G. Craighead
Nanoelectromechanical systems
Science **290** (5496), 1532-1535 (2000)

(7) J. Arcamone
Integration of nanomechanical sensors on CMOS by nanopatterning methods
PhD Dissertation, July 2007, Universitat Autònoma de Barcelona

(8) J. Arcamone, G. Rius, G. Abadal, J. Teva, N. Barniol, and F. Perez-Murano
Micro/nanomechanical resonators for distributed mass sensing with capacitive detection
Microelectronic Engineering **83** (4-9), 1216-1220 (2006)

(9) SioetchH 06/01 VLSISelectipur
worldaccount.basf.com/wa/EU~en_GB/Catalog/Chemicals/pi/BASF/PRD/30268479

(10) BioFinger
Diagnosis tool based on measurement of molecular interactions
IST-2001-34544

(11) G. Villanueva
Development of cantilevers for biomolecular measurements

PhD Dissertation, December 2006, Universitat Autònoma de Barcelona

(12) J. Verd, A. Uranga, G. Abadal, J. Teva, F. Torres, F. Perez-Murano, J. Fraxedas, J. Esteve, and N. Barniol
Monolithic mass sensor fabricated using a conventional technology with attogram resolution in air conditions
Applied Physics Letters **91** (1) (2007)

(13) J. Verd, G. Abadal, J. Teva, M. V. Gaudo, A. Uranga, X. Borrise, F. Campabadal, J. Esteve, E. F. Costa, F. Perez-Murano, Z. J. Davis, E. Forsen, A. Boisen, and N. Barniol
Design, fabrication, and characterization of a submicroelectromechanical resonator with monolithically integrated CMOS readout circuit
Journal of Microelectromechanical Systems **14** (3), 508-519 (2005)

(14) M. Villarroya, E. Figueras, J. Montserrat, J. Verd, J. Teva, G. Abadal, F. P. Murano, J. Esteve, and N. Barniol
A platform for monolithic CMOS-MEMS integration on SOI wafers
Journal of Micromechanics and Microengineering **16** (10), 2203-2210 (2006)

(15) NaPa
Emerging nanopatterning methods
NPM4-CT-2003-500120

(16) NANOMASS
Smart NEMS system for high sensitivity mass detection
IST-2001-33068

(17) S. Ghatnekar-Nilsson, E. Forsen, G. Abadal, J. Verd, F. Campabadal, F. Perez-Murano, J. Esteve, N. Barniol, A. Boisen, and L. Montelius
Resonators with integrated CMOS circuitry for mass sensing applications, fabricated by electron beam lithography
Nanotechnology **16** (1), 98-102 (2005)

(18) J. Arcamone, E. Dujardin, G. Rius, F. Perez-Murano, and T Ondarçuhu
Evaporation of femtoliter sessile droplets monitored with nanomechanical mass sensors
Journal of Physical Chemistry B **on line** (2007)

(19) C. Lehrer, L. Frey, S. Petersen, and H. Ryssel
Limitations of focused ion beam nanomachining
Journal of Vacuum Science & Technology B **19** (6), 2533-2538 (2001)

(20) J. Arcamone, G. Rius, J. Llobet, X. Borrisé, and F. Pérez-Murano
Mass measurements based on nanomechanical devices: differential measurements
submitted to IOP Journal of Physics: Conference Series (2007)

(21) J. Arcamone, B. Misischi, F. Serra-Graells, M. A. F. van den Boogaart, J. Brugger, F. Torres, G. Abadal, N. Barniol, and F. Perez-Murano

A compact and low-power CMOS circuit for fully integrated NEMS resonators
IEEE Transactions on Circuits and Systems Ii-Express Briefs **54** (5), 377-381 (2007)

Carbon nanotubes are used as active elements of electronic devices. After a brief introduction to CNTs, fabrication of devices based on EBL is discussed. FETs are accomplished by contacting single tubes that have been either deposited or grown on oxidised substrates. For on chip-synthesized CNTs, four different approaches are tested in order to optimize device fabrication by the deposition control of the growth catalyst. Postprocessing approach to adapt CNTFETs for sensing applications is developed. A methodology to selectively control CNT placement and orientation is proposed using zeolites.

5 Fabrication of Carbon Nanotube based devices by EBL

5.1 Introduction to carbon nanotubes

The continuos development of microelectronics has been based on the miniaturization of metal oxide semiconductor field-effect transistor (MOSFET). Along last decades, the advances of integrated silicon technologies allowed device scalability, which results in improved speed and power consumption. Hence, better device performance and increased density is achieved. Obviously, industrial interest continues to pursue this progress, but this strategy will at some point reach both physical and technological limitations. Indeed, a new approach is needed and it can be undertaken by two ways: creation of a completely new concept for the devices or introduction of new materials that overcome current limitations in the existing configurations. For the moment, this second solution seems easier to implement and benefits from the discovering of unique and promising materials (1, 2).

Carbon nanotubes (CNT) are considered one of the most suitable building blocks that could lead the evolution for the next generation of devices. Accidentaly, in 1991 S. Ijima observed their synthesis by discharges in carbon electrodes (3). Their appearance was preceded of fullerene discovering, a stable large closed-cage carbon cluster that can be considered nearly 0D (4). CNTs are seen as quasi 1D structures due to their large aspect ratio. Carbon atoms are arranged in long lengths and small diameters that result in interesting physical properties. CNT structure can be described as rolled graphene sheets with half a fullerene in each final edge. This forms a cylinder of few nanometers in diameter that can reach several microns in length. Aside from the interest of studing this structure from a fundamental point of view, their additional outstanding properties make them ideal for many applications (5). As a matter of fact, CNTs exhibit unique electronic, structural and molecular behaviour in terms of electrical conductivity, mechanical strength, chemical reactivity and optical activity (6).

Their use covers a diverse range of interesting potential applications: energy storage, molecular electronics, probes and sensors, composite materials or templates. For example, in molecular electronics they can be used for fabrication of field emitting devices or transistors. As a prerequisite, their properties have to be controllable to allow engineered molecular devices. In composite materials, the high strength, flexibility and low weight make them ideal to reinforce material matrices.
Morphologically, they can be classified in different ways. A single graphene sheet forms what is called a single-wall carbon nanotube (SWCNT), whereas multi-wall carbon nanotube (MWCNT) is a collection of concentric SWCNT of increasing diameter. Specially SWCNTs tend to form bundles, due to their intrinsic electronic configuration (Figure 5.1) that induce intertube attractive Van der Waals forces (7).

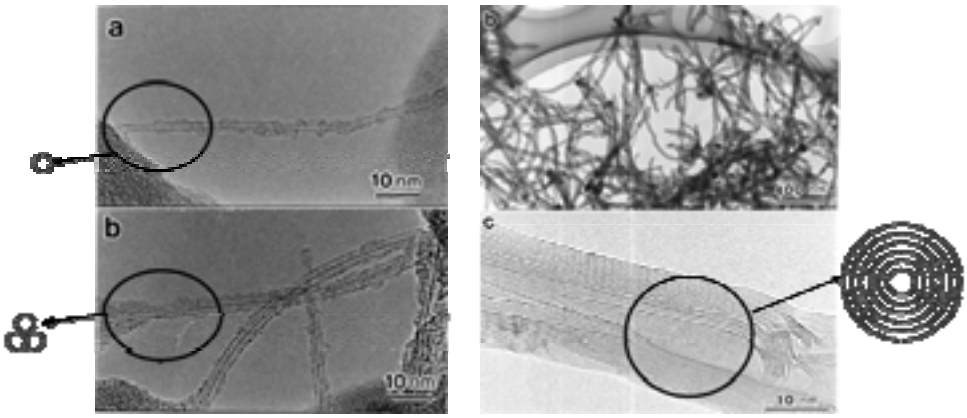

Figure 5.1 TEM images for different CNTs structures. (Left) a. Single wall CNT; b. Bundle of SWCNTs. (Right) b. Multi wall CNTs; c. Concentric structure of MWCNTs (8).

Considering in detail the structure and atomic configuration, their special properties can be modelled. Seen as a graphene sheet wrapped in a certain direction, SWCNT can be described by discrete numbers that determine a chiral vector. The excellent mechanic properties of stiffness and strength are quantified by elastic modulus and tensile strength and they can be deduced from the formation of covalent sp^2 bonds between individual carbon atoms (9).

Their electronic properties can be modeled directly from their morphology (10, 11, 12). Chiral vector is perpendicular to the axis of the CNT and relates equivalent atom sites in the tube by means of the unit vectors in real space of the graphene sheet, a hegaxonal lattice (Figure 5.2, left). The electronic properties strongly depend on the exact arrangement of carbon atoms. Extrapolation from the band structure of graphene in 2D to CNTs in 1D can distinguish metallic tubes from semiconducting ones in terms of chiral indices, m and n. When m = n, tubes are metallic and called armchair tubes . If n-m = 3i (where i is an integer $\neq 0$), tubes are small gap semiconductors (semi-metallic), the zig-zag tubes. The rest of combinations are semiconducting tubes, called chiral and distinguished by the chiral angle ($0<\phi<30^{\circ}$) (Figure 5.2, right). Tight binding description of the electronic structure predicts E_{gap} in terms of carbon-carbon distance and CNT diameter.

Experimentally, the exact determination of tube diameter together with their conduction could allow to deduce atomic arrangement and compare it with direct imaging results. But it is difficult to perform these three characterizations at the same time. TEM sample preparation is not compatible with device fabrication for electrical characterization of an individual CNT, so only indirect techniques such as Raman can

contribute to compare results with theoretical model. Other advanced characterization techniques are been established, such as AFM-based methods (13).

This description does not include defects in the structure that cause deviations from the ideal model. Among others, bends, torsions, formation of junctions or impurities affect their characteristics. Great efforts in simulations are done to predict their contributions (14).

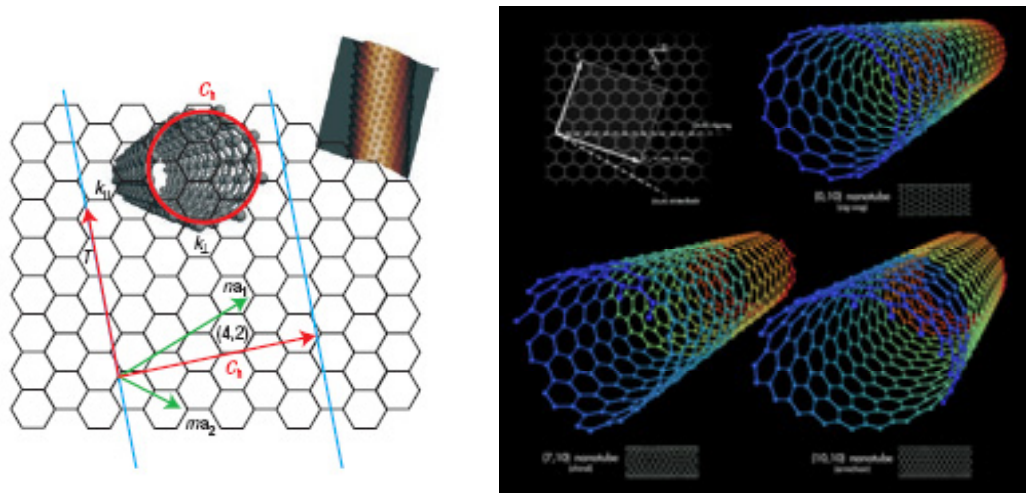

Figure 5.2 (Left) CNT shown as rolled graphene sheet of determined chiral vector. (Right) Types of SWCNTs in function of the atomic configuration: zig zag (top), chiral (bottom left) and armchair (bottom right) CNTs. Chirality determines electronic transport (2).

As mentioned, one of the crucial aspects for the development of applications is based on the possibility to control CNT properties. Growth mechanism is still controversial and it seems difficult to believe that chirality could ever be tuned. Control over synthesis parameters, like pressure, temperature, gases ratios or catalyst particle diameters, seems reasonable. In the growth, carbon atoms are extracted from gases, graphite, etc, when certain external energy is supplied and they tend to form tubular structures.

The synthesis is performed mainly by means of four techniques: arch discharge (15), laser ablation (16), CVD (4) and flame synthesis. Arch discharge consists of two carbon rods placed in an enclosure filled with inert gas. The application of a direct current creates a high temperature discharge between the two electrodes and CNTs are formed. It is easy to implement and results in a large quantity of material, but often contain more impurities than with other techniques. Laser ablation is similar to arch discharge. It is realized in an oven at high temperature by ablation of the graphite target with laser beam. In this case, a smaller quantity of tubes is created, but they are cleaner. The third possibility, CVD uses gaseous carbon sources (methane, acetilene, etc) that are decomposed by the external energy and catalyst particles act as ‘nucleation’ centers. It will be further presented in the next section. Some authors consider that the tubes have poorer quality and larger diameter that other techniques, but the advantage is that it seems easier to scale up and the control over several parameters could allow its use for device fabrication. Flame synthesis is more unusual and relies on the application of a flame to metal catalyst islands that form an aerosol. Its interaction with the carbon atoms from hydrocarbon fuels creates CNTs. No general characteristics for these tubes are reported.

5.2 Fabrication of CNTFETs

From the technological point of view, the fabrication of devices based on CNTs is challenging. Their integration to develop specific functions encounters two main limitations: the control of intrinsic properties of the tubes and the compatibilization of the different processes during device fabrication. Ideally, the control on diameter, length or quantity, the choice of semiconducting vs metallic conduction or the ability to locate them in selected places and either vertical or horizontally is desired.

The first electrical measurements performed on individual CNTs are reported in 1998 for CNTFETs (17,18). The devices were fabricated with a simple approach based on photolithography for the definition of noble metal contacts on an oxidized substrate with highly doped silicon underneath. CNTs were placed by chance on the contacts from a solution (Figure 5.3, left).

The performance of those early devices was far from making CNTFETs competitive to MOSFETs. They behaved as p-type transistors with modulation of drain current from gate voltage. But their characteristics showed low current and transconductance, high parasitic resistance and subthreshold slope and no current saturation.

Patterning contacts on top of the CNTs improves significantly device performance, because metal-CNT contact is not due to weak van der Waals forces anymore (Figure 5.3, center). Other efforts to optimize the electrical properties are done by thermal annealing or choice of metal to adjust metal Fermi level with CNT band edge. It is also desirable to control their conduction. On air, they behave as p-type transitors (hole conduction), but doping may convert them to n-type (electron conduction) (19). Even sometimes they show ambipolar transport (20). This reinforces the necessity of a homogeneus controllable synthesis, in terms of diameter, length, chirality, etc.

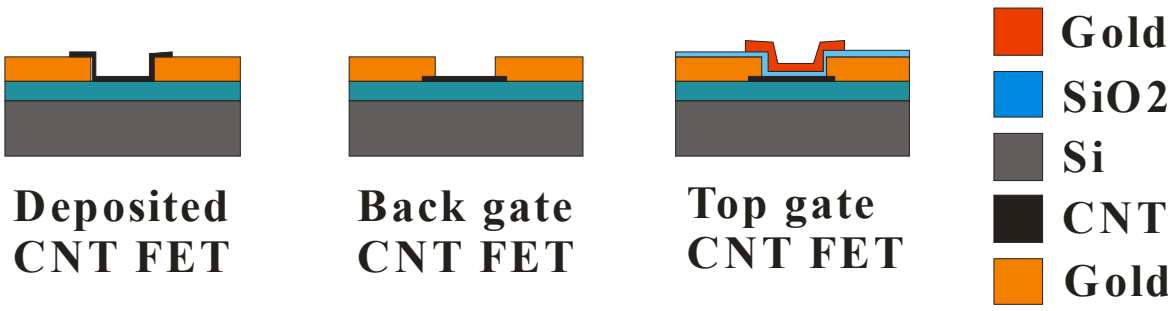

Figure 5.3 Different configurations of CNTFETs. (Left) FET based on deposited tubes on the contacts. (Center) FET based on CNTs underneath the metal contacts. (Right) FET based on CNTs underneath the metal contacts and top gate modulation.

Other approaches implement devices by means of other configurations. In particular, the placement of the gate may allow many different options. The results above correspond to the back-gate configuration, but also top-gate transistors, where modulation is driven from a contact upon a gate oxide on the CNT (Figure 5.3, right), or placement of a proximity third electrode, that lead to single electron transistor devices, are possible.

During the development of this PhD thesis, the technology to fabricate CNTFET has been established at IMB-CNM-CSIC. A general process flow is established for the fabrication of discrete devices based on EBL. A first approach is based on deposition of CNTs and contact definition. In the second part, the introduction of CVD for CNT synthesis allows a better integration and process is optimized by selective deposition of catalytic particles.

Results in this chapter are restricted to back-gate configuration. A good performance for the devices will be presented. Technological issues and different processing flows for device fabrication are discussed along the subsections 5.2.1 and 5.2.2, whereas electrical characterization of contacted CNTs will be studied in 5.3. The common part of the device fabrication process is schematized in Figure 5.4

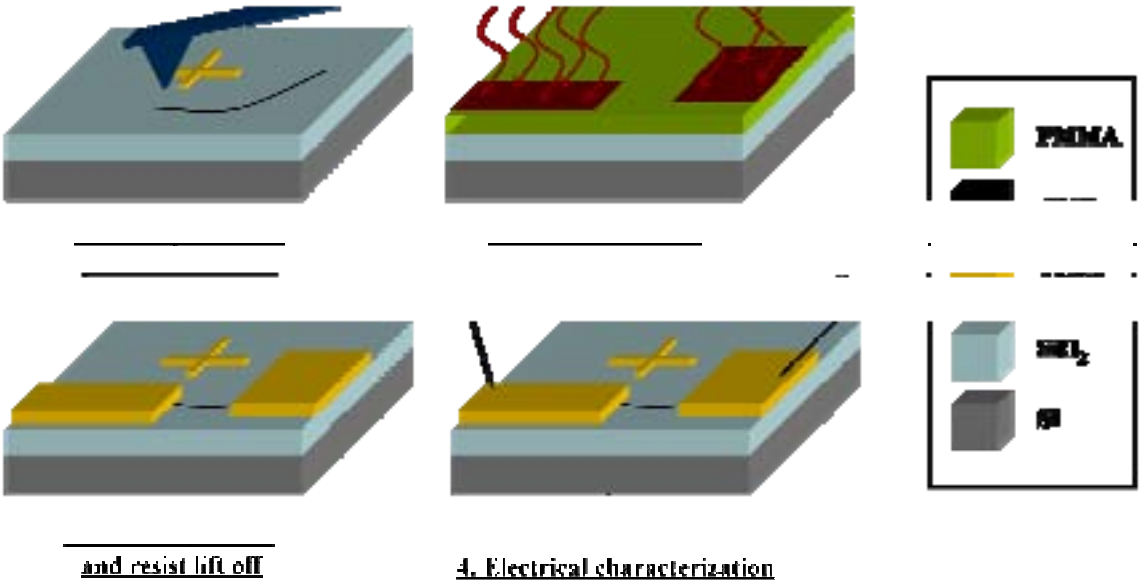

Figure 5.4 Common processing steps for the fabrication of CNT based devices.

5.2.1 Contacting deposited CNTs

The first FET based on a CNT fabricated at the IMB-CNM was presented in the Nanospain workshop in 2006 and, probably, it was the first time that such devices were fabricated by a spanish laboratory (July 2006).

As mentioned, back gate configuration is chosen to implement CNT based devices. A commercial silicon wafer is processed in the Clean Room of the CNM. Implantation is performed to highly dope silicon substrate and thermal oxidation is used to grow a high quality SiO_2 layer of controlled thickness, 200 nm. After cutting the wafer in dices of 1.5 x 1.5 cm^2, the fabrication process for the devices consists of two levels of lithography and pattern transfer by metal deposition and resist lift off, to define drain and source contacts.

Figure 5.5 Fabrication process for contacting individual SWCNTs. It is based on two levels of EBL and AFM inspection for the determination of CNT coordinates.

First, reference marks are fabricated. For this, a chip is covered with 120 nm of PMMA by spining and patterned by EBL. Marks design consists of two sets of marks, one for the determination of CNT coordinates and the other for the aligment of the second level of lithography. This mark design is defined along the chip in many determined positions (typically 70-100) automatically. A thin layer ~30 nm of gold (with an thinner adhesion layer of chromium underneath) is deposited by thermal evaporation and lift off of the resist is realized in warm acetone, sonication, rinsing in IPA and drying in N_2 (Figure 5.5). The choice of thickness and material has to ensure that mark recognition in the second level of lithography will be possible.

The single-walled CNTs have been synthesized by laser ablation and they are presented as powder material. For the deposition, a little amount of CNT material in powder is dissolved in 1,2 dichloroethane and sonicated for 15 minutes in order to disgregate CNTs. Some drops are deposited covering the whole area and the chip is spun at 1000 rpm during one minute to evacuate the excess of solvent. It is important to perform this manipulation with clean laboratory equipment and inside controlled facilities to avoid contamination and impurities in the surface and CNT, respectively. (Figure 5.6, left)

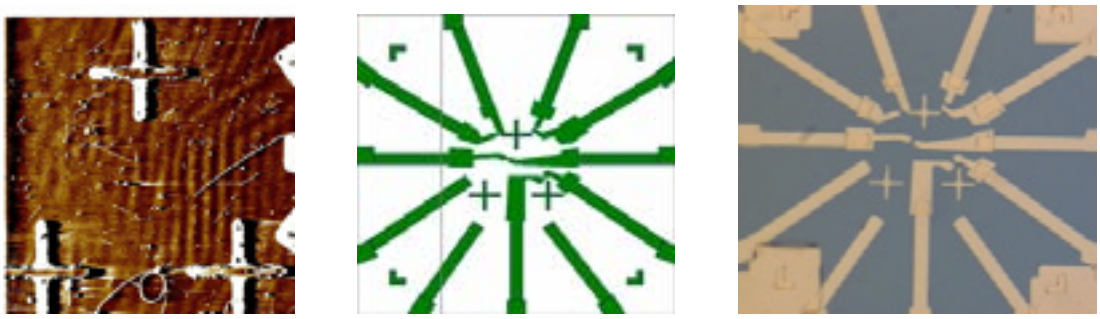

Figure 5.6 (Left) Deposition of CNTs on prepatterned substrate and AFM based CNT coordinates determination relative to the marks. Image scan size is 30 µm. (Center) Design of the second level of EBL for contacting CNTs. (Right) Result of metal deposition and resist lift off. Four CNTs are contacted in this sample position.

The determination of precise coordinates of the CNTs with respect to the reference marks allows to design the pattern for contacting selected tubes. The inspection is performed with an AFM equiped with a close loop scanner, in order to

improve calibration accuracy. Again, it is important to have a clean surface and smooth edge metal marks in order to facilitate inspection: SWCNTs are 1 nm in diameter, whereas metal layer is 30 times thicker. Often, amplitude signal recording in the AFM imaging provides a more suitable contrast than topography, since it reflects rather the change in surface topography than the topography itself. Isolated, long, straight and small diameter tubes are chosen to be contacted.

The definition of drain-source contacts is again based on EBL patterning of PMMA layer. The pattern design is realized manually placing the coordinates of the two end points of each tube in the original design of the reference marks. Then, it consists of adding the contacts with the shape adapted to the tube form and contact separation length that is desired (Figure 5.6, center). The alignment procedure is similar to the one described in previous sections (Chapters 2, 4) . First, a reference system is defined with a chip corner (origin) and chip side (axis) and the stage is driven blindly to the positions where EBL will be performed. Mark recognition consists of opening small windows to adjust the write field references for the beam scan control of deflection in the hardware of lithography. In this case, a double layer of 495k MW + 950k MW PMMA, in total ~250 nm, is used to facilitate the lift off process without sonication to avoid creation of structural defects in the CNT. The metal deposition again consists of evaporation of a layer of 3-5 nm Cr and 25 nm Au (Figure 5.6, right)

After contact fabrication, the edges of the selected tubes are trapped by the metal, obviously if aligment is correct. But also it is important to remark that some rests for the CNT deposition are eliminated and, more importantly, non contacted tubes still remain on the surface. This enables to iterate contacting steps in the same chip if needed.

In addition to contacting deposited SWCNTs, a similar approach has been applied to perform electrical characterization of MWCNT grown at CNM by CVD. The recipe to synthesise MWCNTs provides a great number of vertically oriented tubes. From one side, it is interesting to characterise the nature of these MWCNTs individually since they will be used collectively for sensing, but also the fabrication of discrete devices may take advantage of this massive CNT production that has been established at CNM.

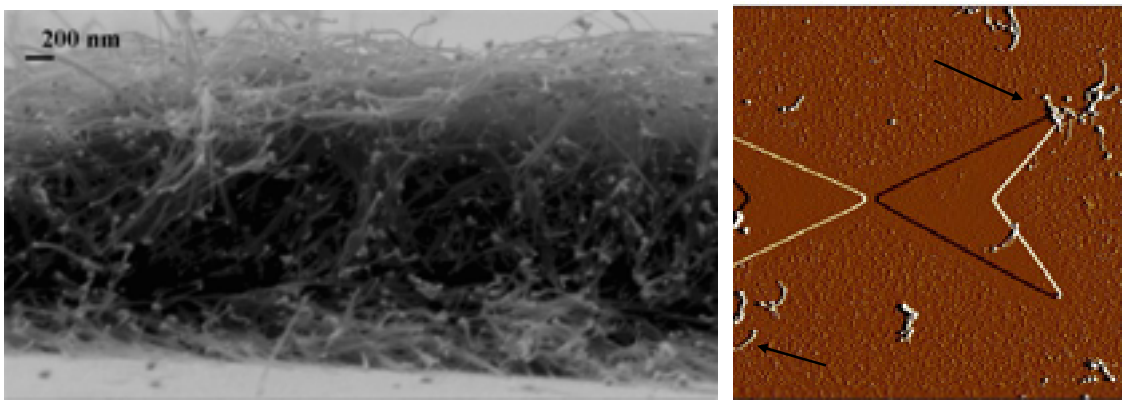

Figure 5.7 (Left) Massive CVD-grown MWCNTs used for individual contacting. Typical tube diameter is 20 nm. (Right) CNTs are dissolved on IPA and deposited in a prepatterned subtrate. AFM Amplitude signal scale is 0.3 V and scan size is 20 µm.

The fabrication process is analogous to the precedent case and only the set up of the solution of CNTs to be deposited differs. A great number of ~1.5 μm length grass-like CNTs are grown in a SiO_2 layer using Pt as catalyst (Figure 5.7, left). The whole chip is immersed in IPA and sonicated for 1 minute. The dark colour of the chip where CNTs were synthesized changed to a clear one indicating that CNTs were certainly detached from the substrate. Some drops are deposited in silicon oxide substrate where previously some reference and alignment marks have been defined by EBL. AFM inspection is performed to determine tube coordinates, but non uniformity and aggregation of CNTs appears. (Figure 5.7, right). For further experiments, more sonication of the solution helps to disgregate them and to increase the potential number of tubes to be contacted.

The fabrication of contacts for electrical characterization is the same that has been described above. It would be convenient to have longer CNTs in order to have more tolerance with coordinates determination of the MWCNTs and, hence, to facilitate metal contac fabrication (Figure 5.8). The electrical characteristics are included in the next section 5.3.

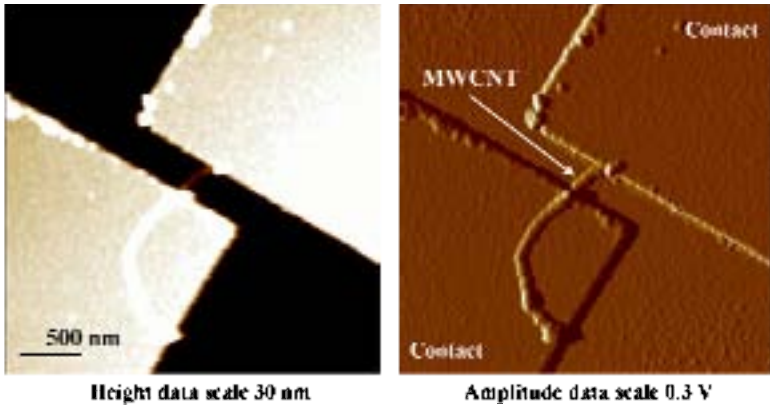

Figure 5.8 Example of a deposited MWCNT that has been contacted.

5.2.2 Contacting CVD grown CNTs

The challenge to integrate CNTs in the conventional fabrication processes for the production of great number of devices is not completely solved yet. One of the main limitations comes from the synthesis of CNTs, which is not directly compatible with most of current technologies. In particular, the temperature of synthesis for the CNTs is typically above 700ºC. This fact can cause the alteration of previous processes characteristics or damage of structures defined before the synthesis. From the existing synthesis techniques, only CVD seems suitable to be combined with silicon based microfabrication.

The fabrication of discrete devices follows the back-gate conguration and only four minor alternatives of process flow are presented (Figure 5.9). Even if the results will not be analized until the next section in terms of device performance, some aspects can be remarked and their extrapolation to the integration of CNTs with conventional technologies may be useful.

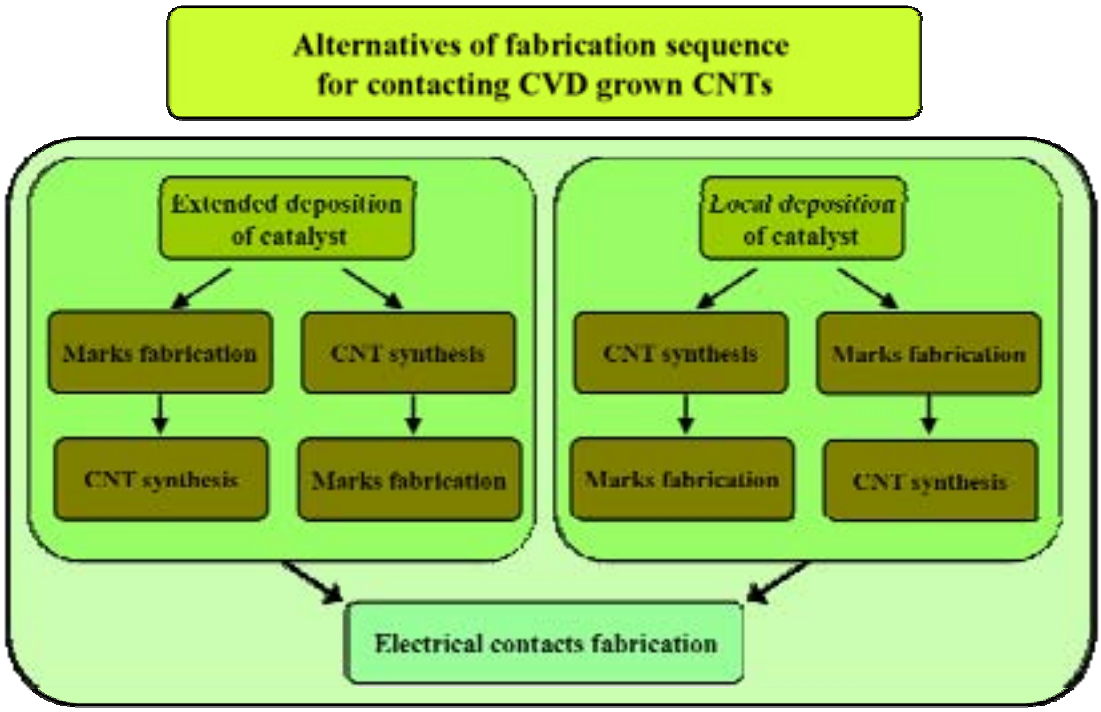

Figure 5.9 Four strategies are used to optimize the fabrication of CNTFETs.
Extended deposition of catalyst before or after the alignment marks definition.
Local deposition of catalyst before the marks fabrication or under the very same marks.

The first fabrication process comes directly from the technology used in the precedent section 5.2.1. Alignment and reference marks are defined along SiO_2 layer by EBL in many determined positions and transferred by metal deposition and resist lift off.

Next, the deposition of the catalyst material is realized. Metal catalyst is spread all over the chip from a solution. The solution concentration can be controlled, which was not the case for the solution used in previous section for depositing CNTs. Clean catalyst compound (for example, ferric nitrate nonahidrated) is weighted, solved in a determined quantity of proper solvent and sonicated for a certain time. Sample is covered with some drops of solution. The precipitation of the catalyst on the sample substrate can be done by two methods, in function of catalyst used. Whether the solution is drop delivered, left to rest on the chip and then rinsed or dissolution is poured while sample is spun at low spin speed. The results of the deposition are not fully controllable neither uniform. Process varies with many parameters: wettability, topography, roughness, catalyst, concentration, spin speed, etc in almost a non controllable way. Then, CVD is used for the tubes synthesis. Again, AFM inspection allows to determine the results of the growth and particularly, the exact coordinates of CNTs. Indeed, this imaging step is very time consuming due to the long time that it takes the acquisition of each high resolution image and sometimes also due to the low number of existing CNTs. As mentioned it is desirable that only one or two tubes lie near each inspected reference mark (Figure 5.10).

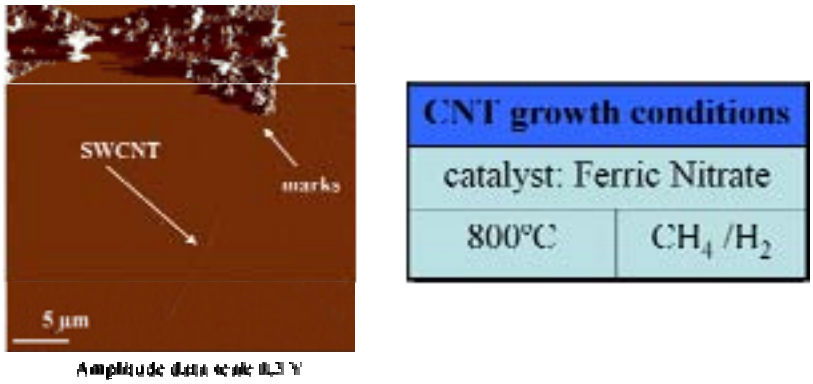

Figure 5.10 Example of the result of CVD after the aligment mark fabrication.
(Left) Thermal process degrades the mark. SWCNT is 7µm long.
(Right) Growth conditions are almost common for all the cases.

Once this is done, the fabrication process is equivalent to the previous case. In particular, EBL is performed at 10 keV beam energy, tipically with a dose of ~120 µC/cm^2 and developed in MIBK and IPA. Evaporation of Cr + Au thin layer is used for the metal contact definition. The results for the different catalyst materials, oxide thicknesses or synthesis processes are presented within device performance discussion (5.3).

However, the integrity of the metal marks can be ruined in the CVD process due to the high temperatures and reaction with the gaseous species. In consequence, AFM imaging for tubes coordinates determination can be more difficult, due to metal disgregation (Figure 5.10, left). and also EBL alignment may be afected

The second possibility interchanges the order of synthesis and mark fabrication steps and relies on the experience of contacting deposited CNTs. Once on the surface, CNTs are not easily detached from it. Thanks to this, it is possible to first realize CNT synthesis and then fabricate reference marks for the determination of tube coordinates. As can be seen in Figure 5.11, left, certainly tubes are not removed in the resist development, neither in the lift off of the resist after metal deposition for the pattern transfer of the marks (Figure 5.11, center). On the other hand, incrementing the number of catalyst particles deposition improves tube growth yield, but may interfere in device performance (Figure 5.11, right).

Figure 5.11 AFM images of the fabrication of CNTFETs using the second approach for extended catalyst deposition. (Left) CNT coordinates determination. (Center) Top view of one SWCNT contacted. (Right) 3D image of another contacted CNT. Spikes are due to the catalyst.

In the introduction, the convenience to control the placement of the CNTs has been highlighted specially for achieving batch production of CNT-based devices. It is necessary to realize devices, wherever it is desired, and also to increase the fabrication throughput. A third strategy is proposed for improving this issue.

In this case, the selective deposition of catalyst material aims to restrict the formation of nanotubes to the places surrounding the specific places where particles are deposited. Once deposited or in contact with the substrate surface, metal catalyst particles are strongly bonded to it and it is difficult to remove them.

Taking advantage of this behaviour, selective deposition is realized through a resist mask patterned by EBL. For this, prior to the synthesis, the sample is spun with a single 950k MW PMMA layer at 1500 rpm and patterned with a variety of design configurations (areas down to 1 μm^2) on specific positions of the chip. PMMA is compatible with catalyst solution and can stand wetting process. Resist stripping is performed in acetone. Figure 5.12, demonstrates that selective metal catalyst deposition is been achieved. Subsequent CVD results in spacially constrained CNTs in a clean surface (Figure 5.12, right). The optimal design to selectively place catalyst could not be determined mainly due to the non reproducibility of synthesis results, caused by solution deposition, resist stripping and growth process uncertainties. However, sometimes the wet elimination of PMMA also dissolves metal particles and results in re-deposition of the catalyst material out of the patterned areas (Figure 5.12, left). Optimization of resist stripping with plasma etching might be convenient to minimize re-deposition of the metal particles.

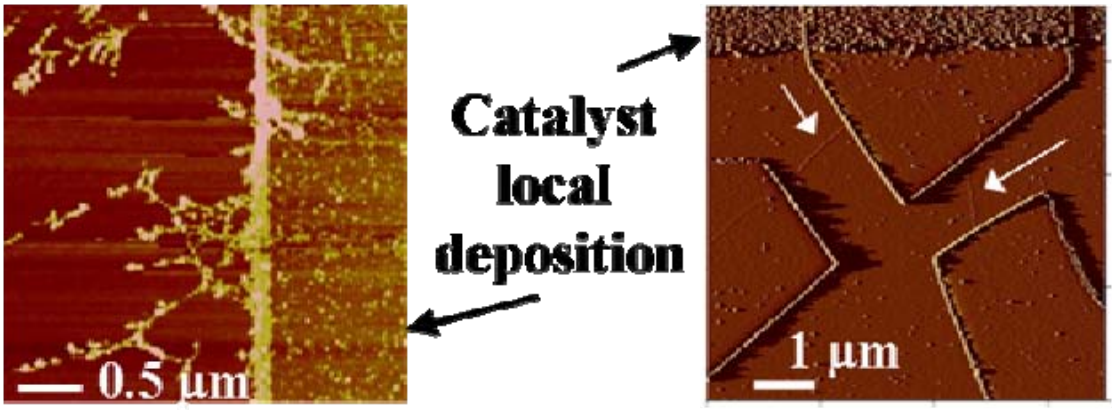

Figure 5.12 (Left) AFM image shows a detail of selective catalyst deposition after PMMA stripping. Some rests are redeposited out of the patterned area. (Right) Two CNTs (white arrows) grown from selective catalyst deposition are contacted. In the upper part of the image the local deposition can be seen together with the cleanness of the rest of the surface.

The fabrication process follows with the definition of marks. It is performed by a second EBL aligned with selective catalyst deposition, metal deposition and lift off. Then, AFM inspection and fabrication of drain and source contacts, as described before. An example of the final result of CNT device fabrication is shown in Figure 5.12, right.

The fourth process sequence is a variation of the previous approach, but reduces its complexity to two lithography levels. In this case, the patterning of PMMA is used for reference and alignment marks definition together with selective deposition of the catalyst. After EBL and development, catalyst metal particles are deposited underneath the Cr + Au thin layer used for fabrication of the marks. Figure 5.13, left and center, shows that the strategy is valid for the CNT growth.

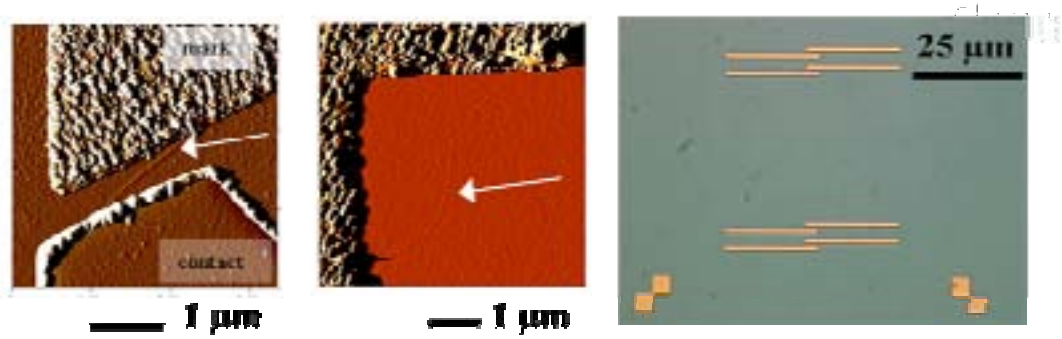

Figure 5.13 Results of local catalyst deposition under the alignment mark sites. (Left) Contacted CNT using the mark as contact interface.(Center) Example of a SWCNT grown with this technique. (Right) Optimization of marks shape and configuration may lead to precontacted CNTs.

In addition, contact using metal mark interface after CVD is possible, as realized in Figure 5.13 (more details in section 5.3). AFM inspection corroborates that SWCNTs are obtained (Figure 5.13 center). Actually, this method is used for fabrication of many devices (Figure 5.27). An optimal design could tailor pre-contacted CNTs, as intented in Figure 5.13, right and make device fabrication easier or open to new catalyst materials or possibilities. As an example, ferrocene (catalyst) has been immobilised with a thin metal layer and subsequent CVD growth shows that it is possible to synthesize massive number or individual CNTs in selected places, Figure 5.14.

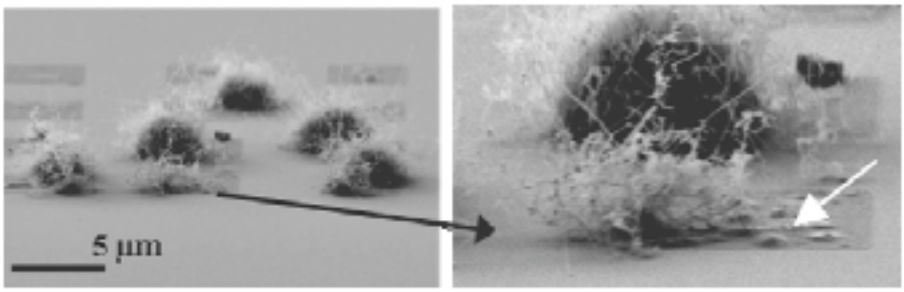

Figure 5.14 SEM images of potential application of this approach where catalyst is deposited below the thin metal layer (white arrow). Ferrocene has been used as the catalyst for the CNT synthesis.

5.3 Electrical characterization

The introduction of CNTs as part of electronic devices represents an evolutionary approach from existing silicon based technologies (common configuration). After more than four decades of improvement of electronic systems by the scaling down of transistors, the end of this development comes closer. Even if technologies continue to improve device dimensions with enhanced fabrication processes, Si-based nanoscale devices will account from loss of bulk properties of their constituent solids (materials). In consequence, leakage current, energy quantization, velocity saturation, drain and source series resistance, etc may disable further evolution.

The use of single molecules is suposed to be capable of overcoming this barrier by maintaining the operating principle of MOSFETs. Molecular based transistors should perform in signal amplification regime in order to allow separate signal treatment in logical operation chains. Moreover, noise is reduced by decreasing thermal fluctuations and environmental disturbances.

MOSFET is the most important device in the semiconductor industry. It is based on a configuration that consists of three terminals (a fourth terminal, substrate, is typically used, but it does not participate actively in device performance). Two electrodes (drain and source contacts) connect the two heavily doped areas and they are separated by the non doped Si channel. The third electrode acts as the gate and is isolated from the rest by a thin insulator layer (typically, SiO_2) (Figure 5. 15).

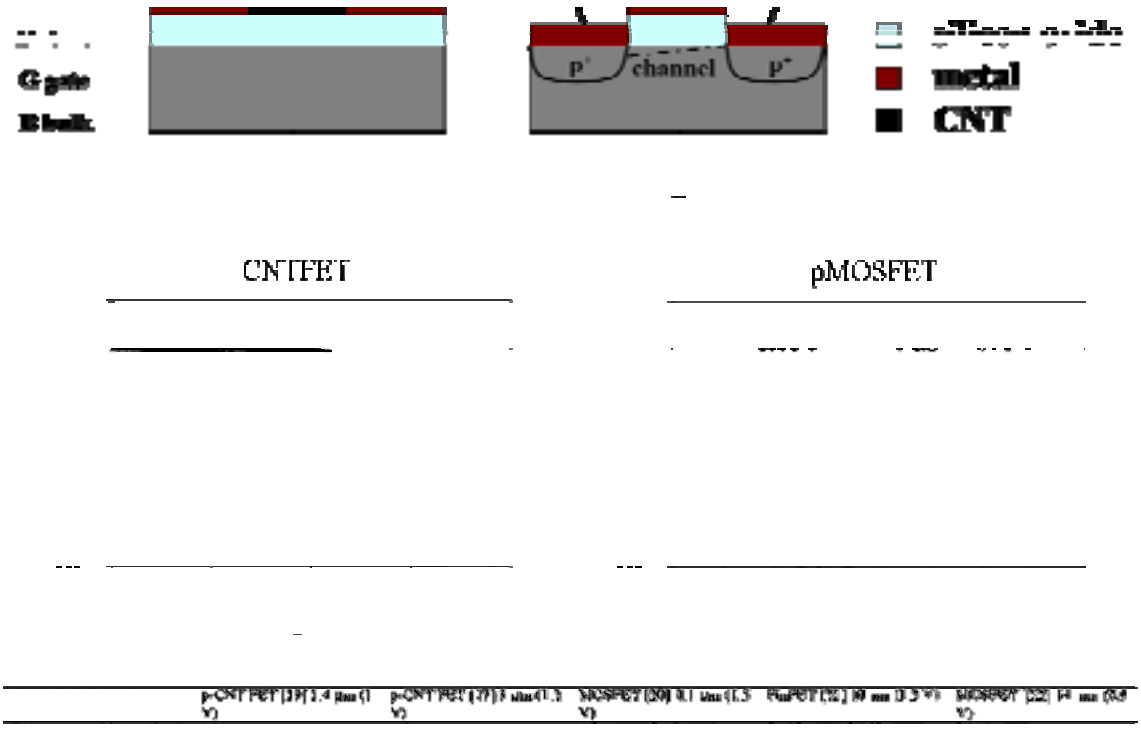

Figure 5.15 Comparison of FET configurations using the CNT as the device channel (top left) or with the conventional MOSFET structure (top right). In pMOSFETs, Si substrate is n type doped and proper device polarization induces the creation of the channel that starts device conduction.
(Center) Comparison of electrical characteristics for two devices fabricated at the CNM. CNTFET (1 μm lenght channel) performance is nearly comparable to MOSFET (3x3 μm^2), whereas device dimensions are significantly smaller for CNT-based device.
(Bottom) Comparison table of experimental CNTFETs and MOSFETs from (21).

The working principle relies on the modification of channel resistivity by means of external electric fields. For the nMOSFET in Figure 5.15, the presence of positive charge on the gate (Vg) does not cause n-type channel conduction until a certain threshold voltage is applied between source and gate contacts. Hence, switching mechanism is based on channel resistance modulation.

For molecular based transistors, single molecules are proposed to play the role of channel conduction. As presented above, CNT structure (diameter and chirality) determines whether their intrinsic electronic transport is metallic or semiconducting. Theoretical studies based on local-density-functional and tight-binding calculations predict their electronic distribution (5). Semiconducting tubes are expected to be characterized by an energy gap,

$$E_{gap} = 2\gamma_0 \, a_{c\text{-}c} / d,$$

where $a_{c\text{-}c} = 0.142$ nm is carbon-carbon distance, γ_0 is C-C tight binding overlap energy and d is the tube diameter.

Besides this, their quasi 1D structure reduces phase space for scattering, so ballistic transport is predicted for ideal SWCNTs due to their perfect symmetry and periodicity. Equivalent effective mass for electrons and holes leads to both negative and positive charge carrier mobility. Therefore, CNTs may stand out in electronic devices due to metallic and semiconducting transport for interconnections and transistors, respectively, high mobilities for high speed device applications, 1D confinement for decreasing channel length, ambipolar conduction controled by V_{gate} for CMOS-like technology (logic circuits), etc (22, 23, 19).

Defects in their atomic structure are seen as scattering centers that interfere in the ideal charge transport. Chemical doping induces diffuse transport and impurities cause resistivity increase in SWCNTs. MWCNTs show also scattering effects and diffussive electron motion, with a characteristic localization of few nanometers and high tube-tube variability in conduction. What is more, semiconducting tubes are more difficult to analise due to interband scattering, but they are usually described in terms of classical physical laws of diffusivity, conduction in terms of effective mobility (24).

A model to explain the operation mechanism and to determine the expressions, which quantifies the FET conduction as a function of device properties, is detailed in the PhD thesis of Sami Rosenblatt from Cornell University (‘Pushing the limits of Carbon Nanotube Transistors’, January 2006). As mentioned, FET is a variable conductor, where the amount of carriers at the interface of the semiconductor is a function of the voltage applied to the gate (Vg). For the CNTFETs, the characteristics can be obtained analogous to the derivation of 3D FET, considering diffusive transport confined to 1D material. The steeped transistor operation is consequence of the application of band structure properties of the CNT. For the CNT relative to the gate contact, the configuration is equivalent to a MOS capacitor. The voltage applied to the gate modulates the position of CNT Fermi level from valence band to conduction band. Hence, the contact resistances between CNT and metal contacts determine the final operation of the device.

The device performance parameters that characterise a FET are common for both configurations, Si or CNT based FETs.

- On current (Ion) determines the amount of charge that is transmitted,
- On-off current ratio (Ion-off) quantifies the difference in conduction between on and off device state,

- Threshold voltage (Vth) determines the gate potential necessary to switch on the transistor effect,
- Transconductance (G) (or similarly, subthreshold slope) accounts for the dependence of current on gate voltage.

These parameters are the ones that are used in present section to evaluate the performance of actual fabricated CNT based devices.

First FET based on a CNT is reported by Tans et al (17) even when the switching mechanism was not well understood. As a matter of fact, to directly export MOSFET configuration does not imply that device performance works equivalently. It is generally accepted that, CNTFET switching occurs by modulation of the contact resistance, that is, the existence of Schottky barriers (SB) in the metal-CNT junctions controls device performance (25, 26). Charges in the channel are blocked by the SBs, but the application of a determined electric field decreases them to allow thermally assisted tunneling and, in consequence, device becomes conductive. With this assumption and together with their 1D transport confinement, CNTs could provide the ideal platform for increasing device density. However, some disadvantages are found from this working mechanism. Indeed, the charge transfer in the CNT-electrode contact is crucial and work function difference or interface quality can dramatically determine device characteristics. Anyhow, excellent properties for CNTFETs are experimentally reported in comparison with MOSFETs, in particular, high conductivity and stability, large current on/off ratios, high values for maximum current density, etc (27, 28).

5.3.1 Electrical measurements set up.

Once devices are fabricated, the electrical measurements are performed to determine their performance and, hence, CNT transport typology. Standard commercial equipment is used: a probe station from Karl Suss PA200 (Figure 5.16, left) for the electrical contacting, and a semiconductor parameter analizer, HP4155 (Figure 5.16, right), to control applied signals and data recording. Measurements are taken in the laboratory of electrical characterization at CNM under normal ambient conditions. This causes an inherent variability in the experimental conditions (temperature, relative humidity, etc), but also simulates real conditions for the operation of the devices, that finally are intended to be used for applications in non restricted environment (on air, in liquid, etc).

Figure 5.16 Equipment used for the electrical characterization on ambient conditions. (Left) Karl Suss probe station. (Right) HP4155 semiconductor analizer.

The sample is placed in the vacuum chuck and stage is motorized to place devices under the optical microscope that assists probe contacting. The contact pads of the CNT device are connected with tungsten probes of 7 μm in radius. Probe header is manually adjusted in X, Y and Z by means of micrometer screws. The conductive probe headers are connected by coaxial wires from the shielding covered probe station to the channels of the semiconductor analizer. Channels are assigned in the analizer interface for the different variables that will control drain, source and gate signals (V_d, V_s – ground- and V_g).

As all the devices are based on back-gate configuration, gate is managed through the probe station chuck, so correct grounding might be ensured. Initial measurements served to establish the biasing conditions and protection limits that are convenient not to damage devices by excessive current, peaks, etc. Initially often both I_{ds}/V_{ds} and I_{ds}/V_{gs} are registered. Since the interest is to use CNT as an active part of devices, the main attention is later centered in I_{ds}/V_{gs} curves, that enables to discriminate CNTFETs from contacted metallic tubes.

The aim of studying the effect of electron beam exposure on devices described in chapter 6 and in particular for CNTFETs, requires systematic electrical measurements to enable comparison in the analysis of the results. This leads to establish a common methodology for the data acquisition, in order to keep invariable electrical measurement conditions. For iterative measurements on a same device, it is specially required to maintain always same channel assignment (probe header wire) for each device contact pad. The biasing control is always driven with the same sequence. V_{gs} slope is supplied in constant direction from positive to negative values (typically, V_{gs} = (5, -5)V) and measurement time is defined by the option short integral time in the analizer. Drain-source potential is established for the acquisition of six curves, ranging from 10 mV to 260 mV in steps of 50 mV. In addition, time evolution control for some devices is necessary to discard device intrinsic variability.

5.3.2 Results for semiconducting and metallic contacted CNTs

Most of the work that is going to be presented has been made in the framework of two collaborative projects. Crenatun (29) is devoted to optimize and control unidirectional growth of CNTs and Sensonat (30) aims to develop specific sensing applications based on CNTs. Both projects are based on collaborative work with other universities, UPV, URV and UAB that also have CVD capabilities for the CNT synthesis, and ICMAB, involved in advanced caracterization of the CNTs.

In the previous section, a general processing flow for back-gate transistors with deposited and CVD sinthesized CNTs is shown. The electrical results cover the different devices fabricated with CNTs synthesized by CVD in the CNM, URV or UAB. In addition, the devices that are manufactured from deposited tubes, which served to implement the first devices and determine measurement methodology, are presented. The discussion is focused on the fabrication and device performance, hence, the variability concerning to catalyst, gases, temperature, etc that is using each partner only will be mentioned if rellevant.

Metallic CNTs

An example of metallic behaviour of a deposited CNT device is shown in Figure 5.17. Contacted tube, with a diameter of 0.7 nm and a distance between contacts of 0.8 μm from AFM measurement, shows no depence with Vgs (Figure 5.17, center) which determines its metallic nature (Figure 5.17, center and right). Main parameters are I_{on} = 1.3 μA for V_{ds} = 0.26 V, i.e. R_{on} = 0.2 MΩ.

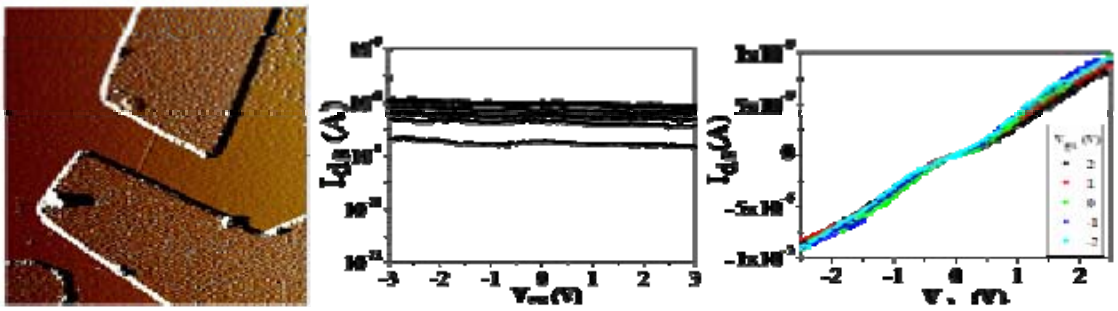

Figure 5.17 Example of a metallic contacted CNT and its electrical characteristics. (Left) AFM image after contact fabrication, image scan size is 5 μm. (Center) Ids/Vgs, Vds ranges from 10 to 260 mV. (Right) Ids/Vds, Vgs range is (-2, 2) V.

Another metallic behaviour with the same type of SWCNTs and fabrication process even reaches current saturation. It is described in (31) that small diameter SWCNTs can carry up to 25 μA at high bias. Electrical characterists in Figure 5.18 shows that saturation current is reached, but, current level is higher than expected. This may indicate that the contacting is not a done on a single tube, but a bundle, which is in agreement with AFM measured height of the tube (about 6-8 nm).

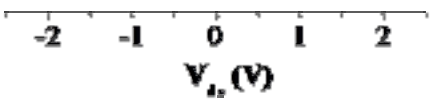

Figure 5.18 Example of another metallic CNT. The high current level indicates that a few number of individual CNTs are simultaneously contacted.

Similar results are achieved with the CNTs synthesized by Iñigo Martin from CNM (32). A great amount of the manufactured devices are based on CNTs synthesized by (RT)CVD. The synthesis equipment is a Jipelec Jetstar 100ST with working temperature range (300-1200)ºC up to 30ºC/s. Injection gases available are N_2, Ar, H_2,

CH_4, N_2O and SiH_4. The catalyst particle is ferric nitrate nonahidrated for all the devices shown here. As can be seen in Figure 5.19, the device characteristics is equivalent to the one above, which may indicate that metallic tubes are not so sensitive to the different fabrication parameters as semiconducting tubes indeed are, in terms of device performance.

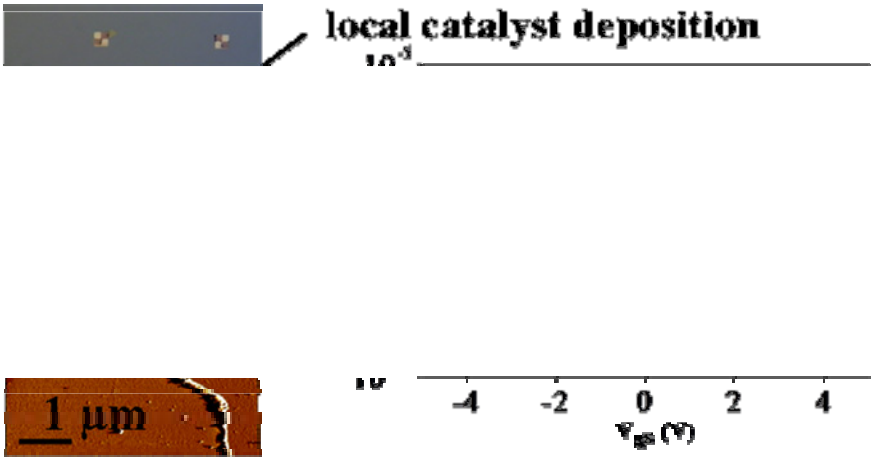

Figure 5.19 Example of a metallic CVD grown CNT using the local deposition of catalyst.

However, it does not mean that device fabrication is not a key parameter for using CNTs as interconnections. As an example, in Figure 5.20, the first device based on the approach of placing catalyst particles under the reference marks is presented. The ridged mark, resulting from the synthesis process (triangular shape), is used as the contacting material for one side of the tube. The metal degradation due to the CVD process seems to be reflected on its performance with a low current level, two orders of magnitude less than previous examples, and a higher resistance of ~17 MΩ.

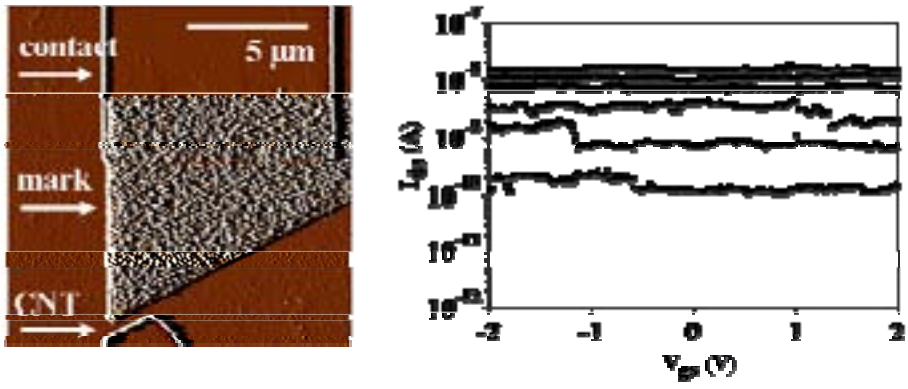

Figure 5.20 Using the strategy of locally depositing catalyst under the marks not only allows to synthesize CNT and contact them, but also the marks can be used as the metal contact interface (left).

Concerning to MWCNTs, they are dissolved from the growth template (Figure 5.7, left) and dispersed on the SiO_2 substrate (Figure 5.21, left). Contacting individual MWCNT has been possible, but a significant variability in the device characteristics is registered. The first electrically measured device has a current of 0.2 µA for V_{ds} = 260 mV (1.3 MΩ), which does not seem so promising as desired for their use in sensor devices (Figure 5.21, right). As mentioned, they have short length, ~1.5 µm, and large

diameter, ~20 nm, which difficults the fabrication in terms of aligment and lift off. Perhaps a thicker metal layer should be convenient to ensure a good and complete contact-CNT interface.

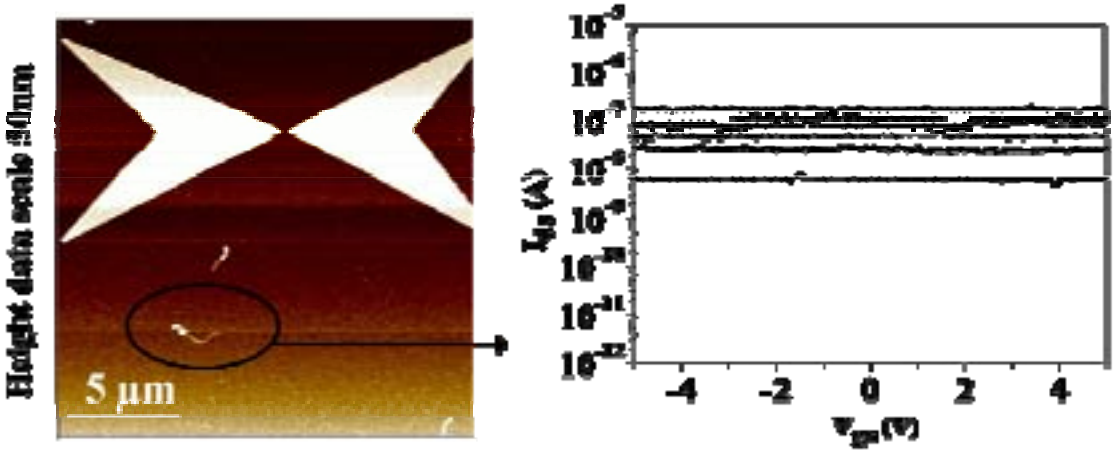

Figure 5.21 (Left) AFM inspection to determine CNT coordinates. These tubes are 1.5 µm in lenght. (Right) Electrical characteristic of the contacted MWCNT.

The second sample with MWCNTs is processed at the same time, but it shows repeatedly higher current levels which may indicate that electrical characteristics are typically more similar to the one in Figure 5.22. In this case, AFM image is taken and it seems that even, probably, the current level is enhanced by means of the catalyst Pt particles that lead the MWCNT growth. Therefore, particle may be more intimately bound to the CNT than the thin metal layer does and it improves device conduction.

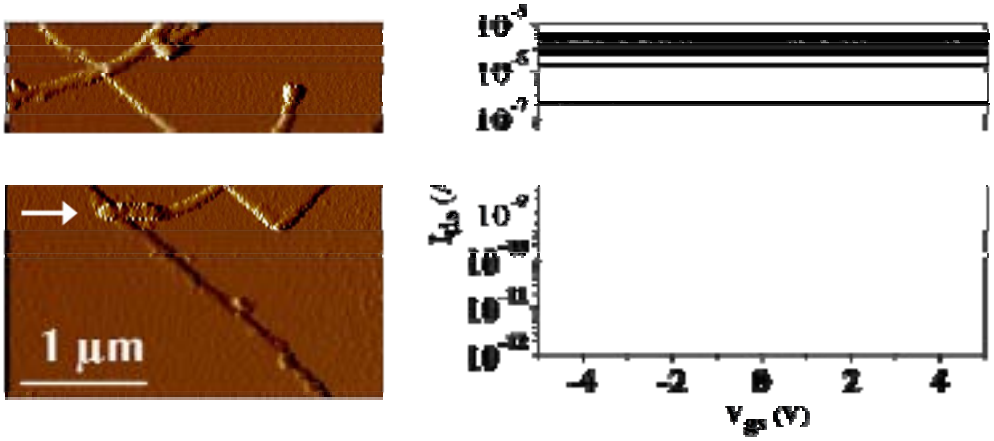

Figure 5.22 Another MWCNT is contacted and measured. Intimate contact with the Pt catalyst enhances the contact with the CNT and, hence, higher conduction is achieved.

Semiconducting CNTs: CNFETs

Concerning to semiconduting CNTs, a general behaviour for the devices is difficult to be established. FETs are typically described in terms of the on current, threshold voltage, transconductance, subthreshold slope, etc. CNT based FETs are complicated to compare due to the intrinsic variability of the CNTs, with respect to diameter, chirality, etc. In addition, they can show time scale inestabilities, hysteresys

and sensitivity to environmetal conditions and processing that strongly affect their performance. Therefore, a general overview of performance characteristics is shown for different devices.

Deposited CNTs synthesized by laser ablation are contacted and characterised electrically, resulting in the curves of the following examples. In Figure 5.23, right, the first CNTFET fabricated at CNM is shown. The CNT of 1nm in diameter is contacted by metal contacts and acts as the FET channel, which is 1μm in length. The resulting on resistance is about 1 MΩ, whereas threshold voltage is 2V and subthreshold slope 0.4 nA/V (Figure 5. 23, left).

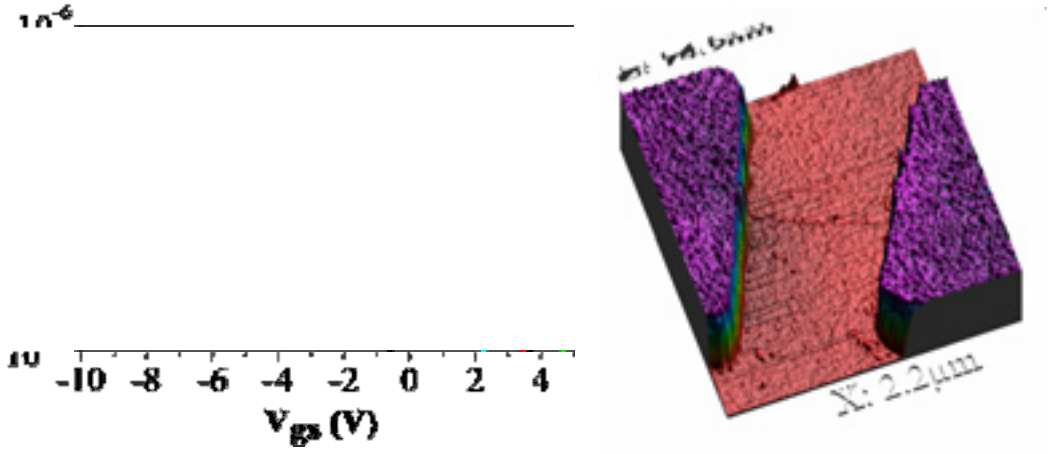

Figure 5.23 (Left) Electrical caracteristic of a CNTFET and (Right) AFM image of this deposited semiconducting CNT and metal contacts.

One of the inconvenients of using deposited CNTs from laser ablated synthesis comes from the impurities that powder material contains and it is reinforced for the resulting random inhomogeneus distribution. As can be seen in Figure 5.24, left, the AFM inspection for the determination of CNTs coordinates can be strongly difficult and even when tubes are successfully contacted (Figure 5.24, center) their electrical characteristics may be altered (Figure 5.24, right)

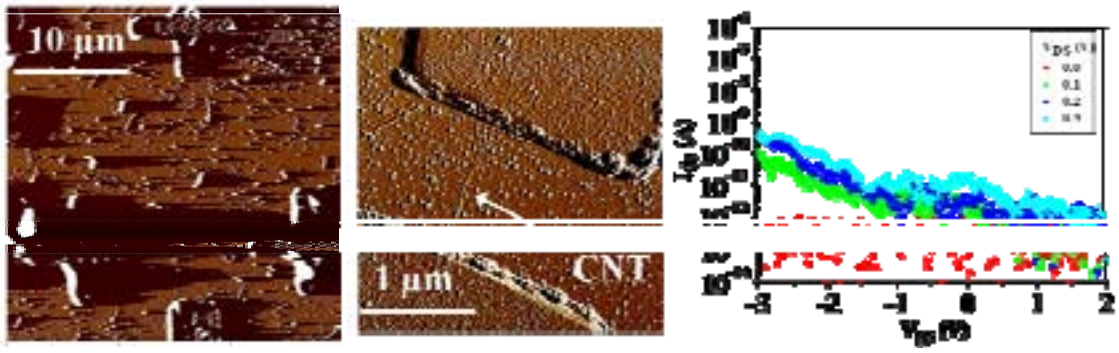

Figure 5.24 (Left) CNT deposition often results in excess of rests that difficult AFM imaging and CNT contact. Even if it is possible to individually contact the CNTs (Center), the electrical characteristics account for a bad result (Right).

As mentioned, some of the CNTFETs tend to operate with hysteresis, while others do not. In Figure 5.25, left, both ramps for increasing and decreasing V_{gs} are

plotted. This device has no hysteresis performance, but certainly it is not outstanding, due to its high threshold voltage and relatively low current and subthreshold slope. In addition, a control of its characteristics in consecutive days corroborates a slight variability of this device, that can not be easily attributed to a single specific cause (Figure 5.25, right).

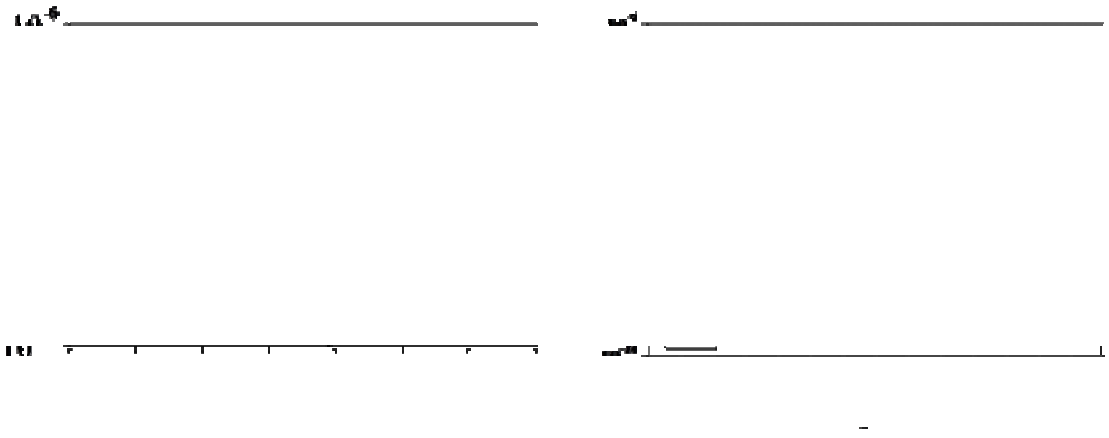

Figure 5.25 (Left) Example of a CNTFET that does not present hysteresis, acquired signal corresponds both to the increasing and decreasing variation of Vgs. (Right) Same device identically measured in several consecutive days. A slight performance variability is registered.

The use of CVD grown CNTs is not only convenient in terms of easier integration with wafer scale fabrication, but also appears to result in higher device performance. In Figure 5.26, two examples of CNTFETs manufactured with the third approach (local deposition of catalyst particles) is shown. In both cases, ambipolar conduction arises for the first time, which was not the case for deposited CNTs, and occurs repeatedly with CVD synthesized CNTs. It corroborates the theoretical background that predicts such phenomena (33). Although they have similar switching response, the quantitative values are again considerably different. While on current levels are in the same magnitude order, off current differs in two orders and also threshold voltage is shifted 1 V. However, in terms of device performance, they have good quality.

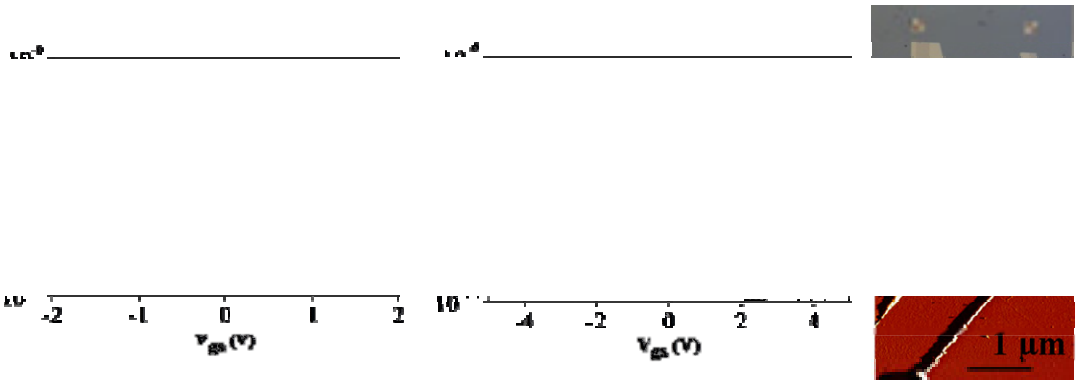

Figure 5.26 Two examples CNTFETs using CVD grown tubes. Both devices show outstanding characteristics: $I_{on} > 4x10^{-7}$ A, V_{th} = (1, 2) V and R_{on}= (0.65, 0.4) MΩ.

For the processing flow based on the placement of catalyst material under reference marks, further experiments demonstrate the validity of the methodology (Figure 5. 27 left). As can be seen in Figure 5.27, center, device performance is really good in terms of gain, but it presents a strong hysteresis behaviour (Figure 5.27, right). Nonetheless, it does not mean that this phenomena is exclusively found for this kind of devices.

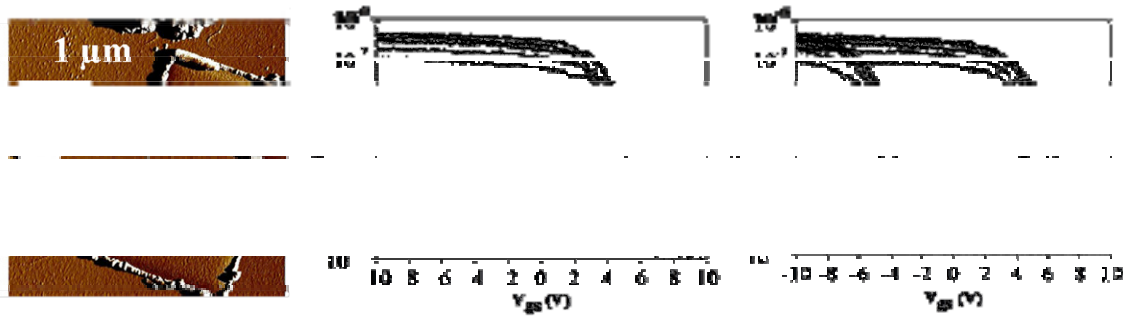

Figure 5.27 In other cases CNTFETs do present hysteresis behaviour (Right). However, the characteristics show a high gain (Center). AFM image (left) corresponds to this device.

With the simplest approach of growing CNTs from the catalyst delivered on the whole sample, the results often resemble those of deposited laser ablated CNTs, where interferences from impurities or other tubes (Figure 5.28, left) lead to a worse device response (Figure 5.28, right).

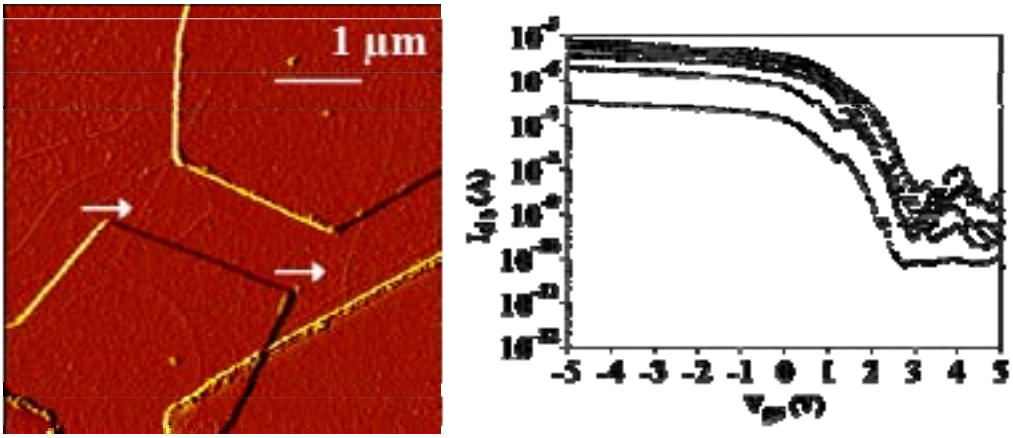

Figure 5.28 An excessive number of CNTs can difficult the individual contact of CNTs and, in consequence, cause worse electrical characteristics.

However, good results can be also achieved with this same fabrication strategy. As an example, the devices using CNTs sinthesized at URV are presented in Figure 5.28. Same catalyst particles (ferric nitrate) are used to grow the tubes on a conventional oven for CVD process. Exceptionally, the SiO_2 layer thickness of device in Figure 5.29, top left, is 500 nm, whereas all the other devices have a common insulator layer of 200 nm. In addition to their good individual performance, it is also noteworthy that the three have very similar behaviour (Figure 5.29). From on current level (>10^{-6} A) to threshold

voltage (constant ~ 4 V) they are quantitavely comparable, even if configuration properties are different (oxide thickness, separate growth and metal deposition, etc).

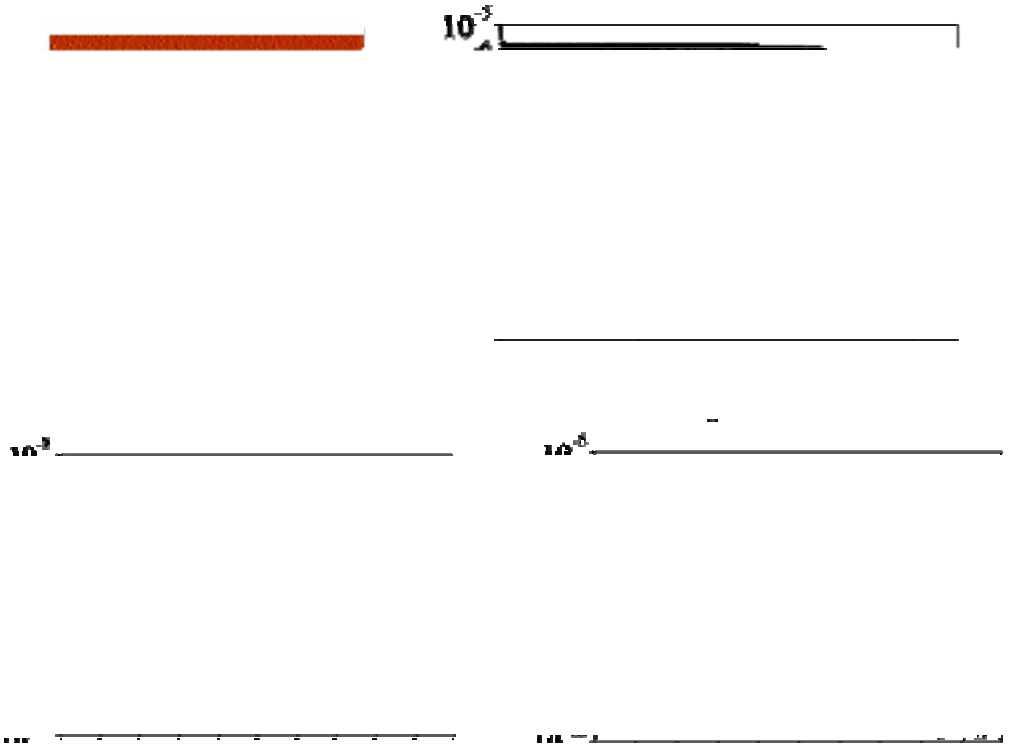

Figure 5.29 Examples of three CNTFETs fabricated with a SiO_2 thickness of 500 nm (top) and 200 nm (bottom). The insulator thickness does not hinder high performance of the device.

Last series of exemplary devices, correspond to the ones sinthesized by the UAB group. In Figure 5.30 two very different curves are presented, although their manufacturing is equivalent. The catalyst is ferric nitrate embedded in a solution with aluminum oxide, molybdenum methoxiethoxide and ethanol, which is demonstrated to have a large CNT growth rate (Figure 5.30, left). The excess of tubes together with rests from the catalyst precursor may contribute to degrade switching mechanism and, in consequence, the convenience of selectively depositing the catalyst is reinforced. As in previous case, similar threshold voltage is found, but, in this case, the rest of device parameters are not comparable (Figure 5.30, center and right).

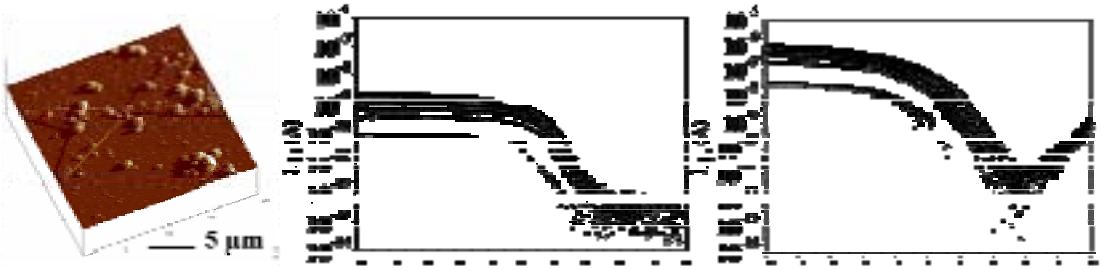

Figure 5.30 The necessity of local deposition with aluminum oxide embedded catalyst is clear. (Left) AFM image shows the excess of rests present on the sample surface after the CVD process. It certainly affects the electrical characteristics (Center and right).

In Figure 5. 31, again raw ferric nitrate is non selectively spread upon sample surface to synthesise CNTs with UAB furnace. The device characteristics presents a high on current, but also an inconvenient high off current level. It can be explained from the AFM image (Figure 5.31, right), where it seems that not only a single tube is contacted. As a matter of fact, accidentally it became a compound device.

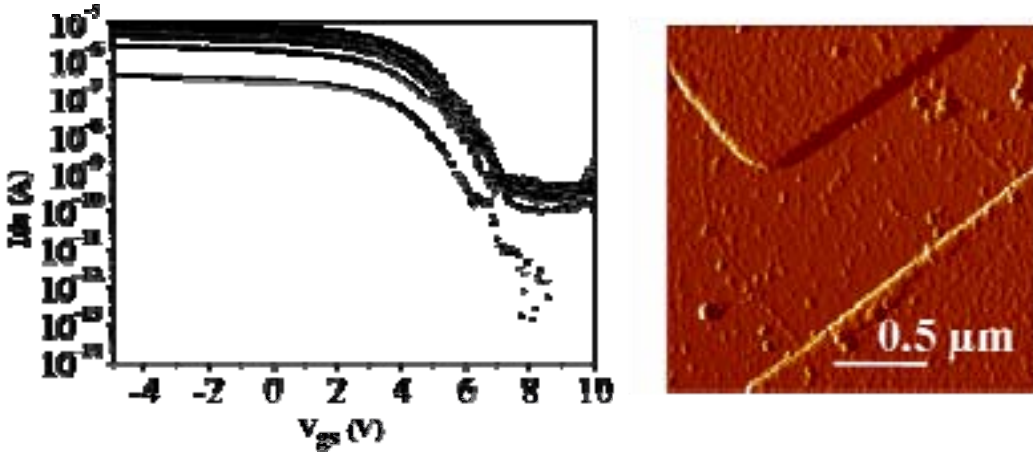

Figure 5.31 (Left) Electrical characteristic shows high off current,which can be caused by the contact of two CNTs (Right)

Double CNT contacts

Double contacts are also being intentionally designed. Their operation may be very interesting to be analized, since future applications of CNTs as building blocks of circuits will be required. Different configurations are possible, where two tubes are contacted in such a way that they share a metal contact (Figure 5.32) or even when a same long CNT is contacted twice. The later could be very convenient to compare conduction between contacts, but, also, to support e-beam exposure experiments that are presented in chapter 6.

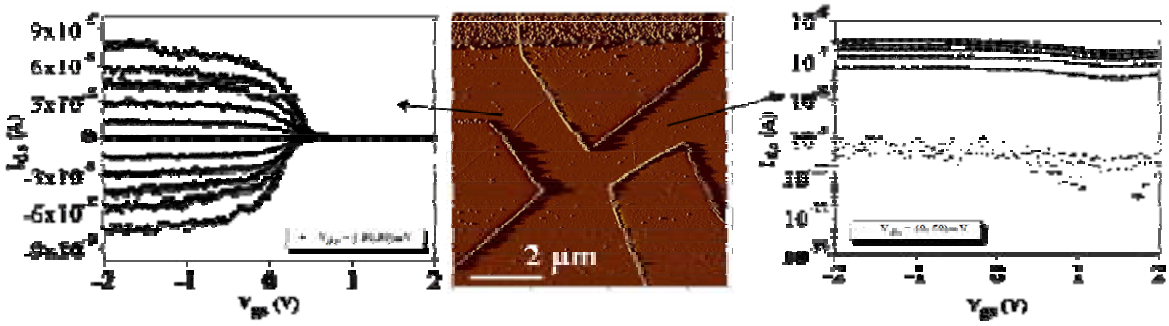

Figure 5.32 Intentionally contacting two or more tubes is the approach to fabricate logic circuits. The left side contacted tube is semiconducting, whereas the one in the right side is metallic.

As an example of such systems, the characteristics of separate contact pairs are shown in Figure 5.33, top, and the response for the compound device (Figure 5.33, bottom left) is presented in Figure 5.33, bottom right. Upper and intermediate contact shows metallic response, whereas intermediate and bottom contact behaves as a CNTFET. As a result, semiconducting tube dominates global system response. Metallic

contribution can be seen as a resistance in series that just lowers total on current level from the on current of CNTFET.

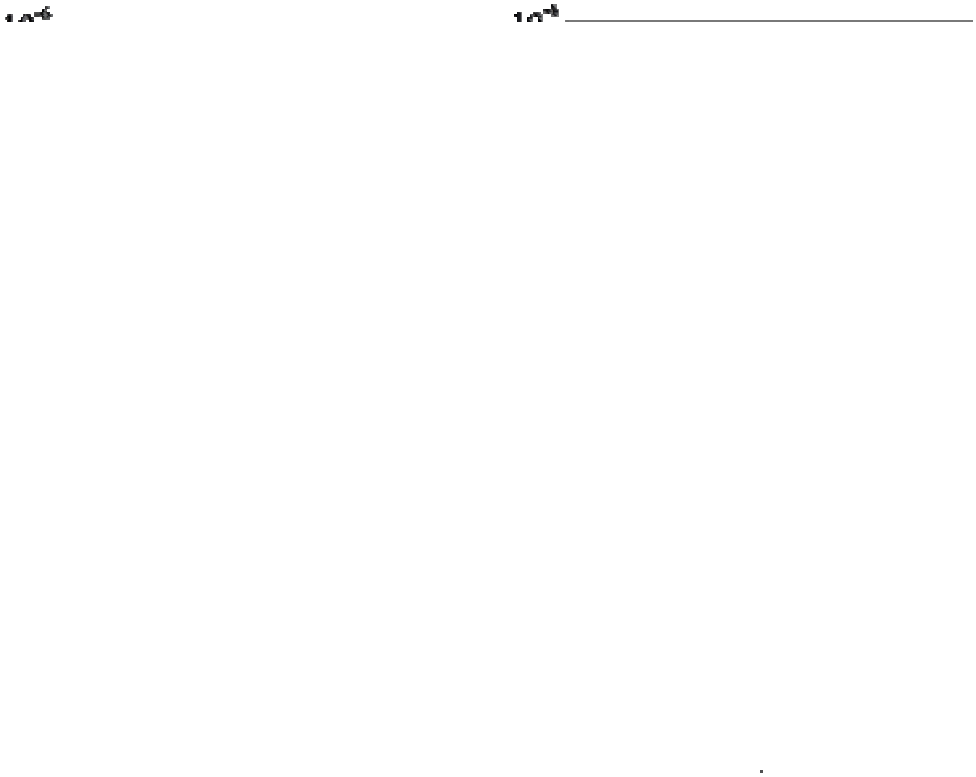

Figure 5.33 Example of double contact of CNTs. (Top) Electrical characterisitics of device formed by contacts 1-2 (left) and 2-3 (right). (Bottom) Optical image of the whole configuration and its global electrical characteristic (contacts 1-3). Semiconducting CNT determines the device performance.

Finally, two examples of a single long CNT with double contact are shown. In Figure 5.34, a curved semiconducting tube is electrically measured and its performance presents high value both on and off current levels. Perhaps, the second tube that can be seen in the left side of the long CNT also contributes to the conduction, but distortion of ideal conduction for curved CNTs is also theoretically predicted.

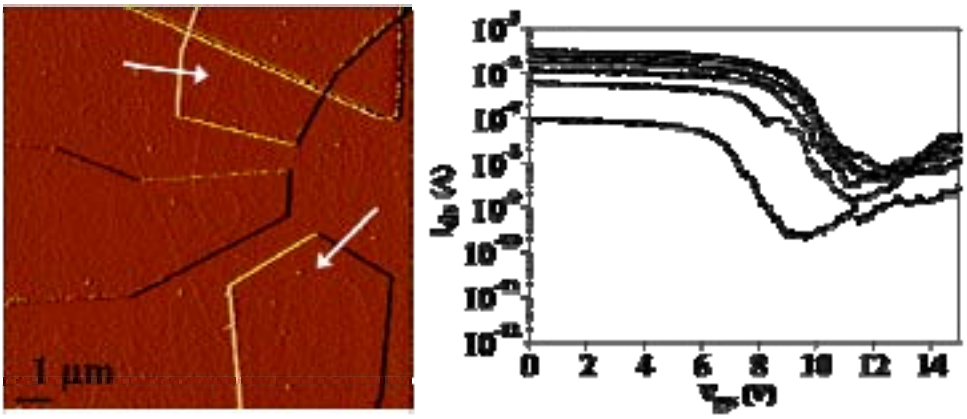

Figure 5.34 Electrical characteristic of the CNTFET placing measurement probes where white arrows indicate.

The contacting of a metallic long tube is also very interesting. In this case, signal from a first contact pair is absolutely equivalent to the one of the second pair. In consequence, it seems that the CNT-metal interface is equivalent for both and that current does not significantly change with small tube lenght variations (Figure 5.35).

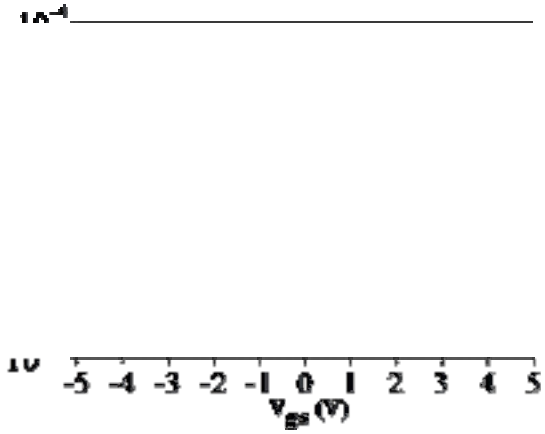

Figure 5.35 Long metallic tube shows no dependence on CNT-metal contact nor channel lenght.

5.3.3 Device performance overview

A systematic analysis from the obtained device characteristics is obviously not possible, due to the reduced number of samples and the diversity of their individual characteristics. However, a global overview of the results can help to establish a flavour of what is expected from the devices and what would be convenient to improve or control in the fabrication process.

Regarding the most immediate device properties from electrical characteristics, a certain general behaviour can be established. For example, on current for metallic and semiconducting tubes is plotted in Figure 5.36. It can be seen that for metallic devices Ion is typically ranged from 10^{-5} to 10^{-7} A, whereas semiconducting devices do not surpass 10^{-5} A and have a considerable higher dispersity in their values. This confirms expected behaviour of semiconducting tubes, since their transport is much more sensitive to all the surronding conditions, from synthesis to electrical characterization and including all the different fabrication processes.

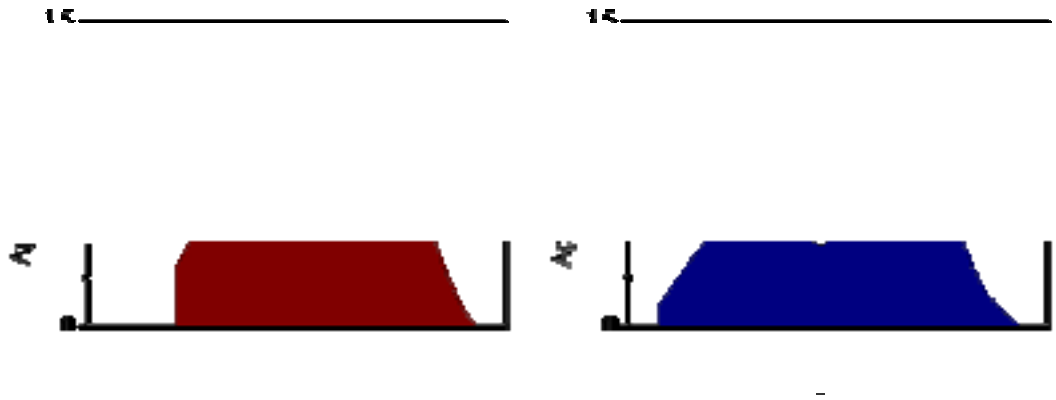

Figure 5.36 Summary of the Ion levels for metallic (left) and semiconducting (right) CNT based devices. Semiconducting tubes have slightly lower Ion and more variability.

The same is observed on the analysis of on-off current ratio and threshold voltage. On-off current ratio is very important for circuits since it determines the feasibility of the desired system operation as a sequence of chained devices. As can be seen in Figure 5.37, right, their values tend to be comprised between 4 and 5 orders of magnitude for the switching mechanism, which is not as sparse as threshold voltage values are. The capability of charge conduction is theoretically different and constraint for both types of tubes, so probably the cause of its variability is mainly related with the different fabrication steps. Figure 5.37, left, compiles resulting threshold voltage for all fabricated CNTFETs. They range from zero up to 10 V with a high dispersion and it can be understood from the strong dependence of this parameter on both tube atomic configuration and characteristics of the fabrication processing flow.

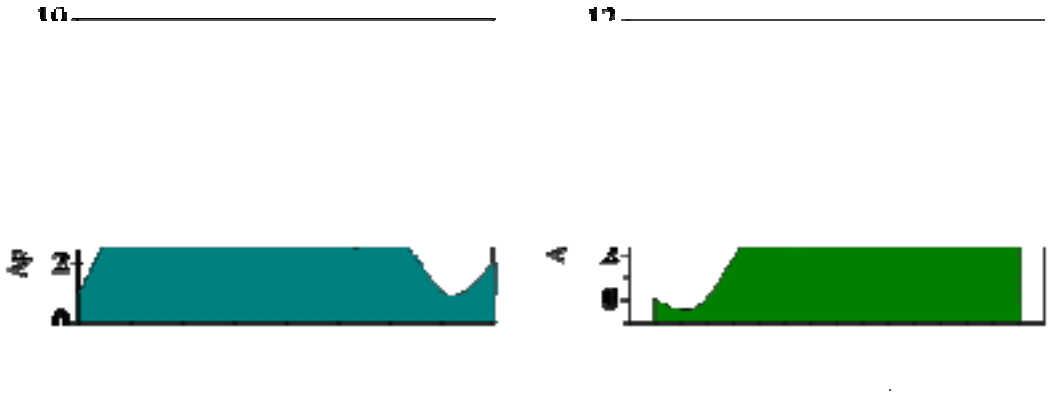

Figure 5.37 Analysis of CNTFETs fabricated. (Right) Ion-off ratio is typically 5 orders of magnitude. (Left) Threshold voltage presents variability, in general, about 3.5V.

From this results it seems clear that precise control and minimization of processing parameters is needed, together with uniform and repetitive tube synthesis. As mentioned, the later is even more difficult to acomplish, so the main effort would be centered to design and fabrication for the real achievement of CNT use as part of devices. However, it is noteworthing that their demonstrated good performance and potential and promising properties are comparable or individually exceed those of conventional MOSFETs.

5.4 Sensors based on CNTFETs

The outstanding properties of CNTs are well known for comprising electronic, structural and molecular characteristics. Due to this, a wide range of high performance devices and structures is potentially proposed for many different applications.

The remarkable chemical reactivity (34) of CNTs relies on their curvature. Specially for SWCNTs, backbone structural atoms constitue also the surface atoms and, hence, pi-orbital mismatch is found. As a result, increased reactivity is expected for smaller tube diameters and covalent chemical modification is demonstrated. Together with the possibility to be functionalised, they exhibit good thermal and chemical stability that make them ideal for sensing applications (35). Another important property comes from their electronic characteristics. The good performance of CNTs as components of devices is supported by their conductivity dependence with environmental conditions, which enables them for direct detection (19, 20) with high

sensitivity. Due to their nanometric size, high spatial resolution, specificity and minimum analyte quantity are spected to be implementable for sensing. Their mechanical properties of strength and flexibility allow their use and manipulation to integrate them in robust electrodes. Biocompatibility represents an important reason for the effort needed to introduce them as part of sensor devices and it is the subject of intense studies.

In consequence, post device fabrication is often needed. In the following sections, several approaches are tested on single CNT devices and preliminar results are presented.

5.4.1 CNT protection, passivation

As mentioned, CNTs are very sensitive to ambience conditions. In consequence it has to be taken into account when used for device fabrication. As part of circuits, they may be protected to avoid environmental interference or, contrarily, it can be exploited to alter their conduction characteristics (20). For sensing, constrained/confined sensing area may be desirable or, even, needed for unequivoquely quantify the analite. The use of two different polymers has been studied for both protection and isolation of CNTs and device (36).

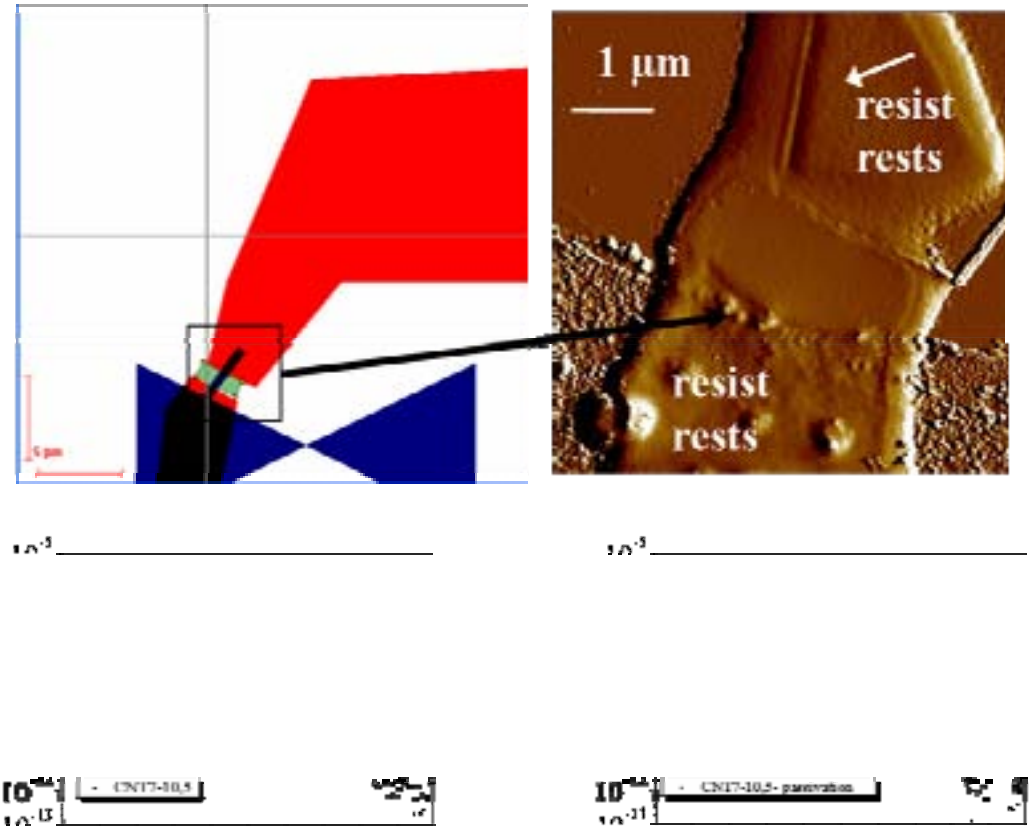

Figure 5.38 Example of a CNTFET protected with mr-EBL 6000.1. (Top) Green area is designed to cover the CNT channel. Result of EBL shows good alignment, but resist residuals are observed on metallic surfaces. (Bottom). Electrical curve before (left) and after (right) resist protection. Electrical characteristic does not change significantly.

First, the epoxy based resist (mr-EBL 6000.1) described in Chapter 3 is used. This negative resist can be used for coverage of the channel of a CNTFET by precisely aligned EBL. Exposure is realized at 3 keV incoming beam energy using the alignment marks defined for drain-source contact fabrication. The reason for choosing this beam energy comes from the analysis of electron beam effect on devices described in Chapter 6 to avoid electron beam induced damage. In Figure 5.38, top, the design of CNT covering area (green) and the result of lithography are shown, together with the electrical characteristics before and after resist passivation, Figure 5.38, bottom (left and right, respectively). It can be seen that aligment is precisely placed, but some rests of the resist are also found in the surrounding area. It has been already observed (Chapter 3) a certain affinity of this polymer to stick to the Au layer. More importantly, electrical characteristics are almost unafected, so good performance is expected for this resist as a passivation layer and the EBL process methodology is valid.

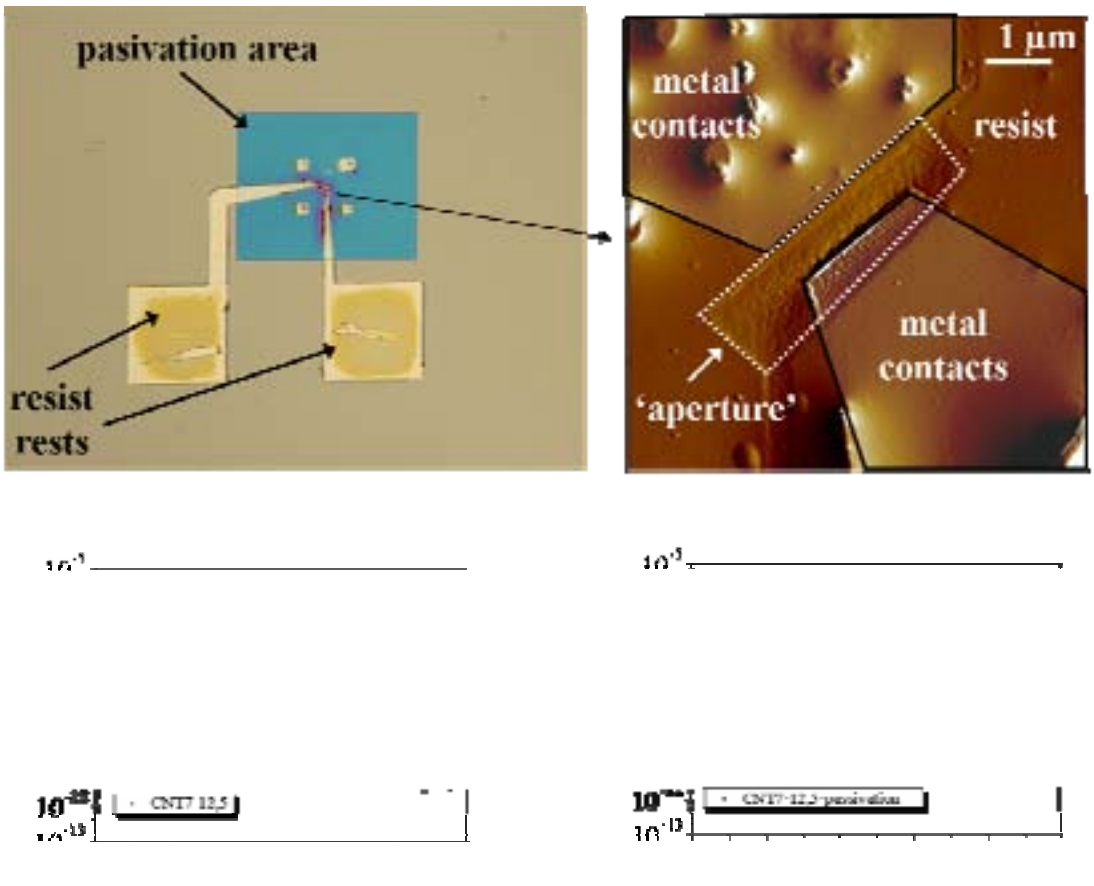

Figure 5.39 Example of device passivation with negative resist to protect metal contacts and to leave CNT channel on air. (Top) AFM image (right) shows that either dose is excessive or development is not complete. Some resist residuals in non exposed metal areas appear again (left). Electrical characteristic is almost invariable (bottom).

Same method and exposure conditions are used to test this resist as a protection layer, for example, in liquid measurements. In this case, design might consist of a big area that leaves the FET channel (CNT) and contact pads on air, for sensing and electrical recording, respectively. The results are shown on Figure 5.39. Again, some rests are found in non desired locations, whereas good alignment has only partially been

achieved. In this case, exposure is not trivial due to the large area coverage and required aligment precision. Alignment precision requires exposure of CNT area with a small WF (typically, SEM magnification 1500x for 100 x 100 μm^2), but large area coverage is done with bigger ones (250x for 800 x 800 μm^2). The high sensitivity of this resist helps to reduce exposure time importantly, but two aligned steps of exposure will be needed. A precisely aligned exposure with small WF size and a second one for patterning the rest of the area to be covered with a larger WF. Rests may be attributed to an accidentaly incomplete development process or perhaps even a certain affinity of this resist to stick to gold. On the other hand, electrical measurements show no effect on device characteristics. It confirms that this material and the used exposure conditions might be a possible choice for establishing a passivation method.

The alternative method is using a positive resist to be patterned by EBL. PMMA is reported to show a good performance as an ambience insulating material and also offers the possibility to be used as a barrier for selective and specific sensing (20).

A single layer of 950kMW PMMA is used for the passivation test and it is patterned by EBL at 3 keV to open areas in the FET channel and contact pads. High precision and pattern resolution is achieved as it is expected for this conventional resist (Figure 5.40). Electrical measurements are not shown because this device already failed before the passivation experiment.

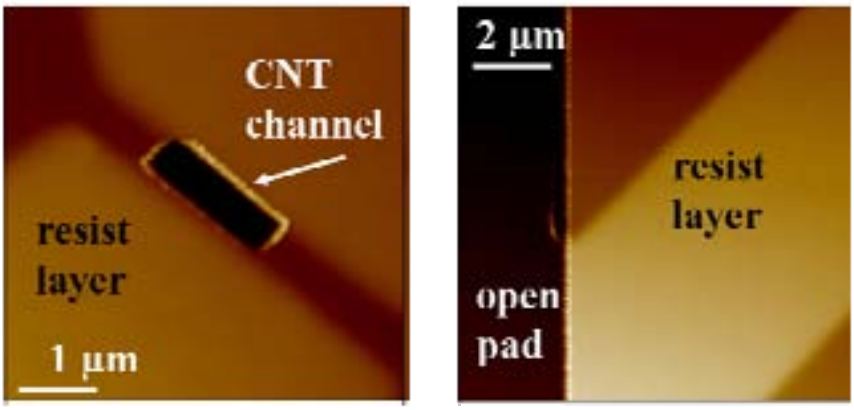

Figure 5.40 Passivated device with PMMA. EBL conditions and aligment are correct.

In conclusion, the two resists seem suitable for the passivation and optimal conditions are nearly established. Feasibility might be checked if further specific limitations arise. For example, negative epoxy based resists are suposed to possess more robust, stable and higher etch resistance properties that might be useful in some cases.

5.4.2 Liquid measurements

First measurements in liquid with CNTFETs are undertaken based on the previous process flow. PMMA is used as mask to drop liquid only on the CNT. Hence, electrical characteristics might not be affected by liquid contact of drain and source metals.

The openings are defined as in previous case and several different designs are tested for achieving precise placement, good resolution and finally, CNT wetting, in few

devices. Again, EBL technique shows a good performance and achieves desired results (Figure 5.41).

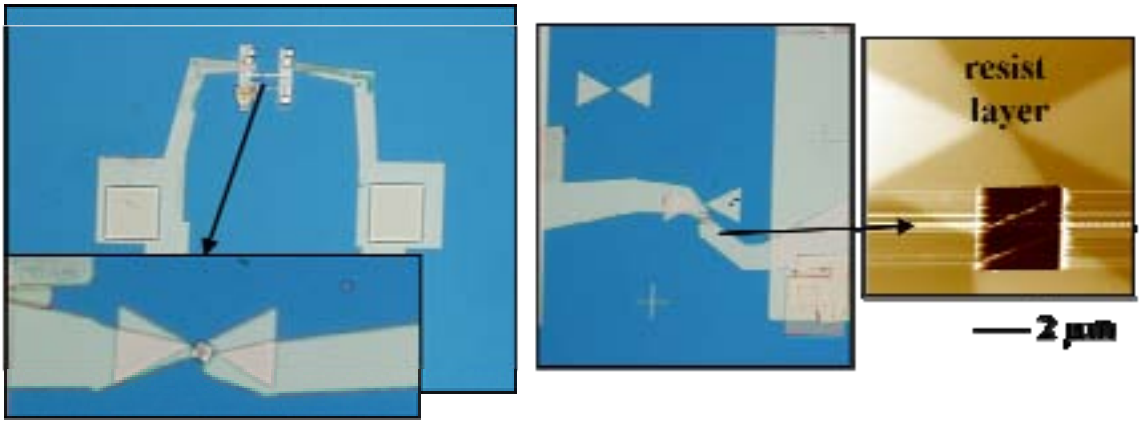

Figure 5.41 Different designs are tested on a 100 nm PMMA layer to prepare devices for liquid measurements. (Left) Optical image of passivated device. Apertures are patterned at CNT channel and contact pads.

On the other hand, sometimes electrical characteristics of the devices after passivation are affected when the openings are patterned and developed. For example, for the device in Figure 5.42 threshold voltage diminishes aproximately 1V and I_{off} seems slightly higher, whereas $I_{on\text{-}off}$ ratio and transconductance are almost constant. This change does not seem very important considering the results in 5.3, since some devices already showed little variations with time spontaneously.

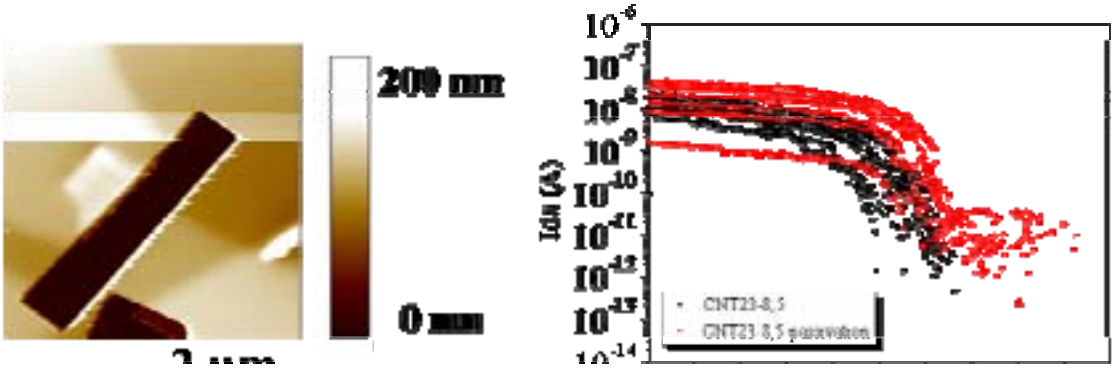

Figure 5.42 In order to avoid metal contact wetting, openings are precisely adjusted to the channel width (left). (Right) Electrical characteristics of the CNTFET before (black curves) and after (red curves) passivation.

Other measured devices present a more dramatic effect on their characteristics, as can be seen in Figure 5.43, when openings in the channel are realized. Semiconducting tube device (Figure 5.43, left), increases I_{off} in three orders of magnitude and I_{on} diminishes in about one order, resulting in nearly the loss of transistor effect behaviour. Concerning to the contacted metallic tube (Figure 5.43, right), the

current decrease exceeds four orders of magnitude. The reason of such change is not clear and may be attributed to the combination of many causes. Perhaps, some contamination from the surface that was not clean at all (Figure 5.11, right), imprecisions in the alignment or other effects are responsible of it. A deeper study of this behaviour will be needed prior to systematic liquid measurements..

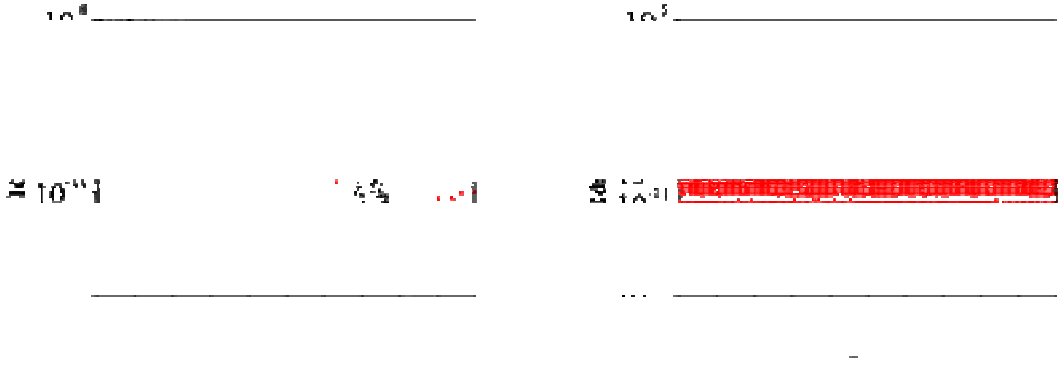

Figure 5.43 After passivation, some devices show a significant change in electrical performance. Black curves correspond to measurements before PMMA passivation and red curves after EBL processing.

The first trial measurements in liquid have been performed in collaboration with Mª José Esplandiu from the Chemical Sensors group of the UAB. Another selectively passivated device is wetted in the simplest solution, raw deionized water. The device characteristics are taken before liquid delivery (Figure 5.44, right, black curves). Water drop is manually placed in the opening of the CNTFET and optical microscope image is taken which corroborates its correct placement (Figure 5.44, left). First electrical characteristics show a shift of threshold voltage of +3 V, enhanced subthreshold slope, slight increase of on current and noise signal suppresion (Figure 5.44, right, red curves). One minute later, a second device characteristics is taken and a change is again seen. In situ optical microscope inspection revealed that water drop was no longer on the CNT area. The current remains almost constant while all the other observed parameters change. Noise signal increases to the original level, threshold voltage shifts again until ~ 6 V, subthreshold slope is similar to the pre-liquid delivery one and ambipolar behaviour appears.

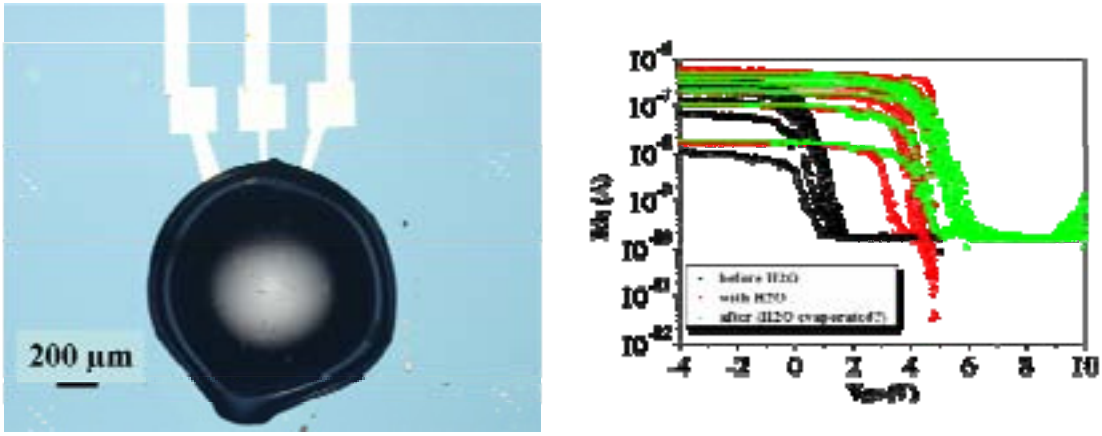

Figure 5.44 Test of depositing deionised H_2O on a passivated CNFET. Water drop induces Vth shift to a higher value and cancels Ioff (red curves). After second measurement is acquired (green curves), optical inspection showed that drop has gone. Ioff has recovered the original level.

It seems that water might induce the first change in device performance, whereas the second behaviour could be attributed to the remaining humidity when water drop is evaporated or slithered down the surface. More importanly, the effect on the CNTFET performance is different from the following case when saline solution is used. Therefore, selectivity of the device to different solutions and validity of the system configuration for liquid measurements seems to be confirmed.

PMMA passivated device in Figure 5.42 is used to deliver saline solution on CNT opening (Figure 5.45, left) and electrical characteristics are immediately registered. In Figure 5.45, center, device performance evolution is shown from the electrical characteristics of the original device –black-, with manually deposited drop of solution –red- and after one and two N_2 sprays –green and blue-. An AFM image of the channel of CNTFET after liquid measurements is shown in Figure 5.45, right. Even if CNT is absolutely covered with crystals from the solution, electrically it continues to work.

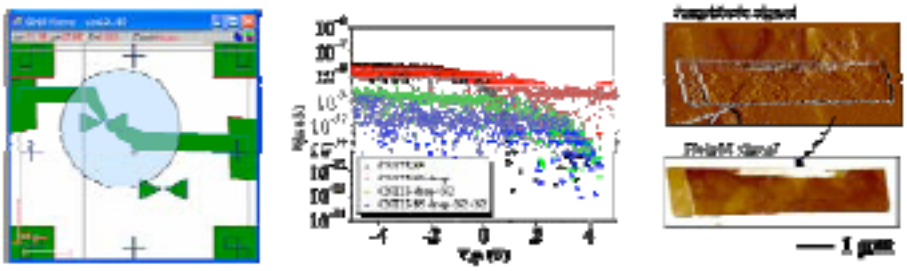

Figure 5.45 First CNTFET measurement in liquid. (Left) A drop of saline solution is placed on the passivated devices of Figure 5.42. (Center) Electrical characteristics of the experiment (black = reference; red = drop delivery; green = first N_2 drying; blue = second N_2 drying). (Right) Crystal salts are found on CNTFET opening after the experiment. Amplitude and height data scale are 0.3 V and 150 nm, respectively.

These results are not specially important to evaluate sensing performance of the device, but they allow to determine solved issues and technological challenges for further experiments in liquid. In particular, PMMA is able to passivate device, since it performs adequately as a hidrofobic barrier for the solution. Even though drop deposition has been achieved, an easier way of controlling liquid delivery is needed and the effect of the solution on device performance should be systematically studied.

5.4.3 Set up for CNT based measurement systems

Previous sections 5.4.1 and 5.4.2 have presented several methods to enable applications and studies of CNT based devices. The establishment of the different approaches is intended to support their combination and, in consequence, to make possible all the specific systems that can be desirable.

Some examples of proposed systems for sensing applications or other configurations for specialised research are here presented which can be implemented in the near future.

The use of selective etching of CNT channel by means of a PMMA mask can encounter many purposes to be applied. As an example, a systematic study of the effect of SiO_2 thickness on CNTFET is proposed. Device performance as a function of oxide layer can be determined by subsequent depth controlled etchings in the same single device. This strategy may avoid variability between tubes, tunnel current contributions from contact pads in ultrathin oxide layers, etc. Similarly, taking advantage of it, the fabrication of NEMS based on CNTs could be improved. Thanks to the EBL resolution on PMMA, etching for the release of CNTs could be performed only in the channel. It may avoid short circuits due to contact metal collapse on substrate and even control of released CNT length is possible, which may make nanodevice fabrication easier or even 'tunnable' resonators feasible.

Moreover, same method can be applied to a great number of possibilities. Besides specific environmental sensing, selective doping of CNTs for device performance studies or development of discrete logic circuits are available this way.

For liquid measurements, the evolution of presented measurement system is already designed. Passivated devices with selective aperture of channel and contact pads will be combined with wire bonding and PCB integration for the realization of real experiments in liquid. After CNT devices are fabricated and sample is protected with PMMA and patterned for the openings, wire bonding will be realized to connect devices to the PCB. Taking advantage of measurement configuration developed by the biomedical applications group at the CNM, wires will be manually protected with PDMS paste. The liquid container will be finally sticked on top of it to allow solution delivery (Figure 5.46)

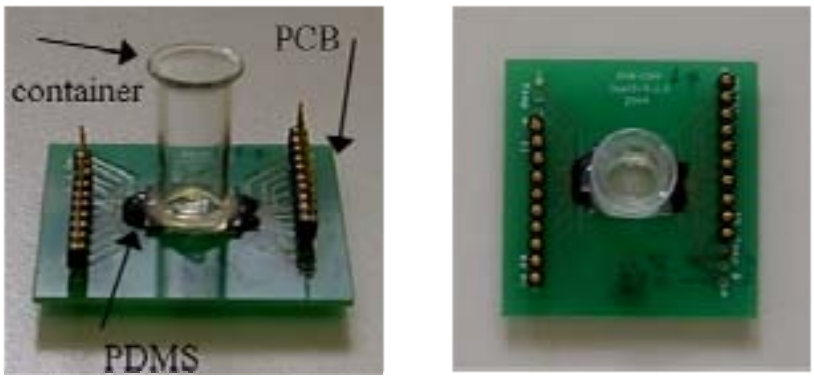

Figure 5.46 Set up proposed to realize real tests in liquid. After passivation, devices are wire bonded to a PCB. Wires are protected with PDMS and liquid container is fixed to the PCB.

Slightly simpler configurations are needed for other especific experiments to be realized on CNT based devices. In particular, the effect of C_{60}^- bombardment of CNTFETs requires a vaccum compatible system with simultaneous recording of device electrical characteristics. Previous work on wire bonding on PCBs and the use of external device polarization enables it. Adjustment of connections to the C_{60}^- source tool is under development. Eventually, very long tubes with many contacts could be selectively bombarded by means of selective protection protection with PMMA (See section 6.3.5).

In relation with this, the continuation of the studies of electron beam effect on CNTs that are compiled in chapter 6 may be refined with in situ electrical measurements by means of the FIB tool and combined with advanced AFM based characterization,

current and force detection. Finally, as another example, resist protection also could be used to determine electron range in the resist as a function of beam energy from the change of device performance.

The systems presented are just a general overview of the amount of possibilities that technological development could validate. Even though fabricated systems are very far from massive batch production, all the advances will contribute to extend the integration CNTs on microsystems.

5.5 Local and oriented growth of CNTs for fabrication of devices

Many times along this section, it has been highlighted the interest to integrate CNTs as nanodevice components and the limitation resulting from their wilful growth. Even if some enhanced improvements are achieved, device development continues to be only partially successful. Engineering smart strategies are proposed to optimize CNT use. The aim of this section is focused to achieve control over the location and growth direction in the synthesis of CNTs by means of fabrication based strategies.

Crenatun project works in the controlability of one-direction CNT growth. This issue is undertaken with the combination of advanced/tuned catalyst materials and adapted technology processes. In particular, for the growth of horizontal and XY spacially aligned tubes, the use of catalyst embedded on ceramic materials together with two fabrication approaches is proposed.

Zeolites (37) are porous materials that can be artificially synthesized from silica and alumina to form structures rather controllably (Figure 5.47, left). The porous molecular structure is characteristic for each different zeolite type and, more importantly for this case, other materials, such as metals, can be rather easily incorporated. The maximum size of the species that enter the pore is controlled by the diameter of the channels.

Using zeolite material to hold catalyst particles for the CNT growth has been demonstrated and replicated with CVD at the CNM (Figure 5.47, left). Not only control over the size of the particles is ensured, also CNT growth directions are restricted to the zeolite channel directions (Figure 5.47, right).

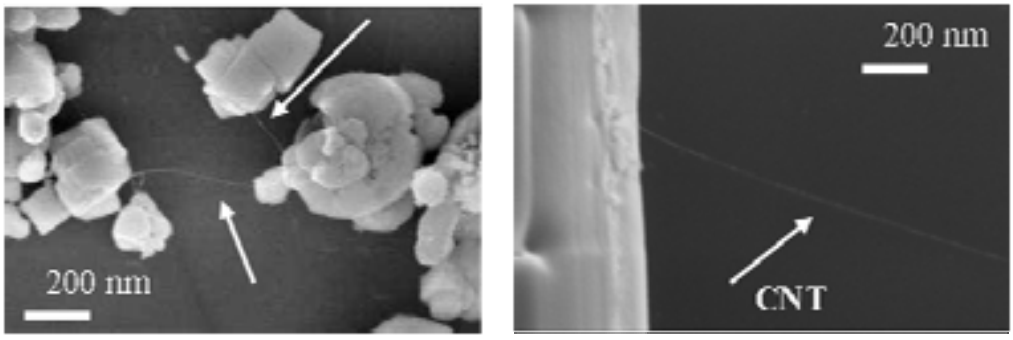

Figure 5.47 (Left) General view of zeolites used to synthesize CNTs.
(Right) Some CNTs grow in radial direction.

Directional growth of CNTs complemented with placement of the zeolites in selected places may contribute to incorporate CNTs in the fabrication of devices. The

control over zeolites positioning and compatibility with the rest of processing flow of device fabrication is realized through micro/nanofabrication processes. This is an example of combination of top-down and bottom –up technologies. Zeolites are doped with the catalyst particles that will act as CNT growth precursor, whereas engineered structures or masks place zeolites in the desired positions. In this section, first results for two different approaches are presented. The realization of devices may be undertaken in the near future.

The zeolites used are provided by the ITQ (Instituto de Tecnología Química) group from the Universidad of Valencia. Zeolites are dimensionally controlled and typically about 1 μm in diameter and 5 μm in lenght (Figure 5.48, left), which determines the dimensions of the masks that are next presented. Moreover, standard deposition of zeolites from solution shows a non uniform distribution and certain tendency to form aggregates (Figure 5.48, right).

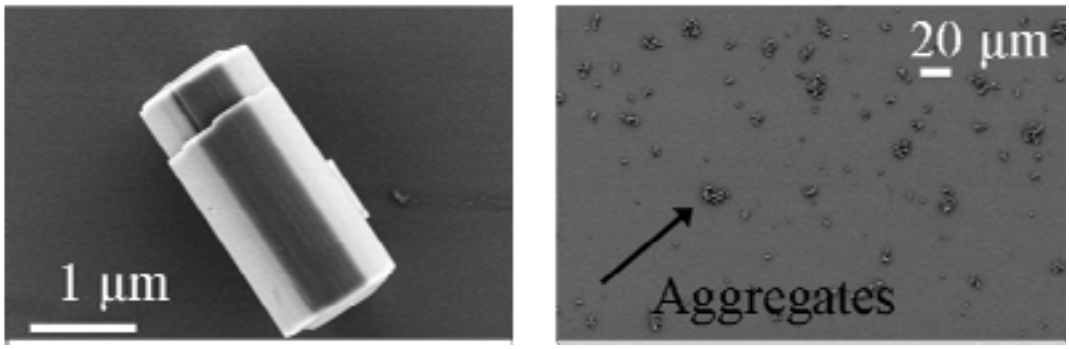

Figure 5.48 (Left) SEM image of typical dimensions of the zeolites used for selective positioning. (Right) Zeolites tend to form aggregates.

5.5.1 Negative resist

The first alternative to place zeolites in determined sites of a chip is based on the use of a negative resist and pattern transfer to the substrate. In particular, ~120 nm of mr-EBL 6000.1 (see chapter 3) is exposed by EBL. This pattern is used as a mask for the Si substrate etching. RIE has been chosen for its anisotropy, but eventually wet etching could be also adapted. The mask design is shaped to induce zeolites to rest in a certain direction and mainly in the coordinates where structures are patterned (Figure 5.49, right). Here, a kind of bottleneck structure is proposed in order to induce zeolites the tendency to rest confined in the central part of the structure. Zeolites placement together with addressing zeolite direction and CNT growth restricted to their channels may optimize contacting them for CNT use on applications. Etching depth can be controlled to be adjusted to the zeolite diameter and the solution deposition method (Figure 5.49, left), but first the etching selectivity should be checked.

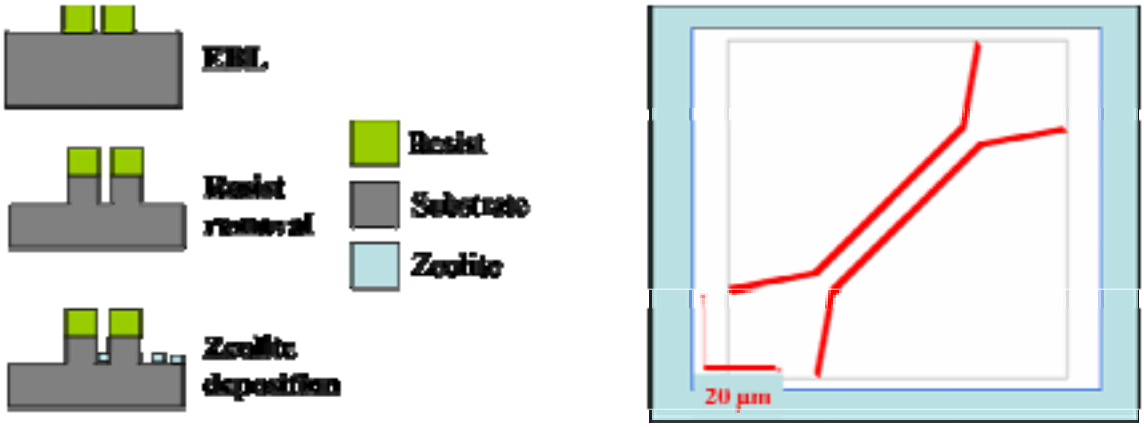

Figure 5.49 First approach proposed to selectively locate zeolites.
(Left) Fabrication process is based on a negative resist patterned by EBL and transferred by RIE.
(Right) Design of the structure (red) to induce zeolites to be placed in the trench.

For this first approach, the exposure parameters are determined. Specially exact dose and separation between the 'arms' of the structure to avoid proximity effect in the center (Figure 5.50, left) are adjusted, due to the high resist sensitivity (see chapter 3). The RIE of Si in SF_6 for 30 " and 1 min is realized in two different samples. Resulting etching depth is about 150 nm (Figure 5.50, center and right). Regarding etching profile, it is clear that resist thickness could not stand during all the etching process and, hence, it started to engrave part of the originally resist protected area (Figure 5.50, center). Indeed, this polymer does not resist longer RIE processes, therefore with this technique, some limitations in the fabrication process arise yet before zeolites deposition test.

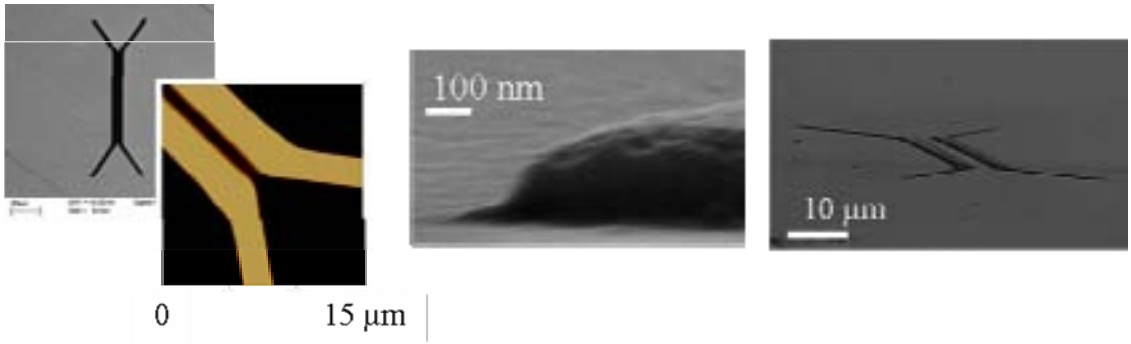

Figure 5.50 (Left) SEM and AFM images of the EBL result on mr-EBL 6000.1. (Center) Result of RIE. Trenches are less than 200 nm in depth. (Right) General tilted SEM image of the final structure.

5.5.2 Positive resist

The alternative process is based on the use of a EBL positive resist to act directly as a mask for the zeolite solution deposition. Prior to the subsequent CNT synthesis, stripping of the resist is needed and no effect on the selectively deposited zeolites is a must (Figure 5.51, left).

The sample is covered with a thick layer of MMA-MAA by spinning. This resist is usually used for technological processes based on pattern transfer by metal deposition and lift off of the resist. Underneath a higher resolution layer of resist, it provides

favourable profile (undercut), due to its high sensitivity and size of chain scission elements (see chapter 3).

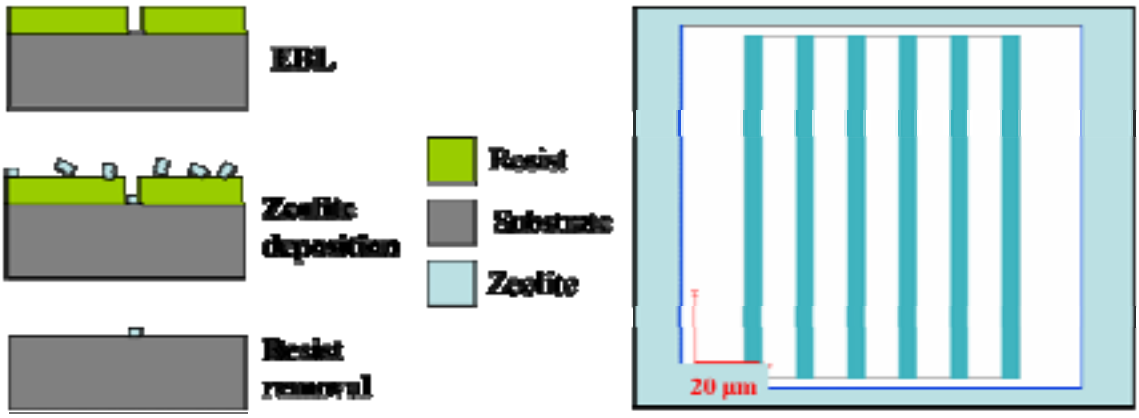

Figure 5.51 Second approach prposed to selectively locate zeolites. Positive resist is pattrened by EBL, zeolites are deposited and resist is eliminated. Design consists of long trenches of 5 µm in width.

The choice of copolymer to be directly patterned is very convenient for many reasons. Among the advantages for this specific application, the following aspects are remarkable. Required resolution does not represent a challenge in terms of lithography, since feature size might be in the few micrometer range. Besides this, typical copolymer deposition results in thickness layers ranging from 300 to 700 nm and clearing dose is low. Both properties are very adequate in this case, because it fits better with zeolites diameter and reduces exposure time, respectively.

A simple structure is designed, in particular, the pattern consists of an array of 100 µm long and 5 µm width of trenches (Figure 5.51, right). Samples are exposed by EBL automatically all along the sample and they are developed in PMMA standard developer (MIBK: IPA) (Figure 5.52). Structures are patterned about 500 times using automatized EBL mode (see chapter 2).

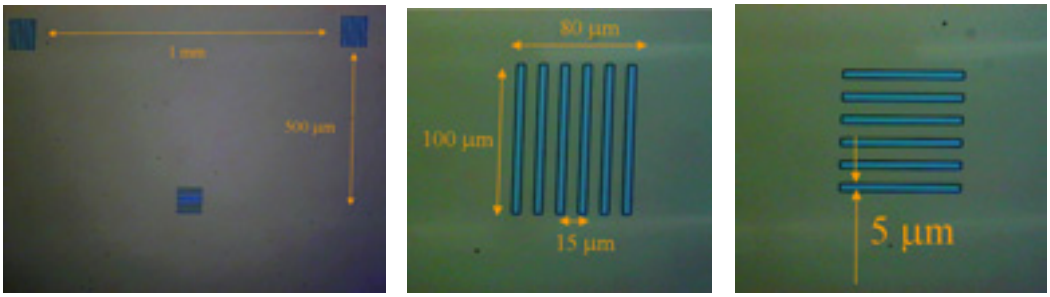

Figure 5.52 Optical images of the results of EBL in the copolymer layer. Resist thickness is 650 nm.

5.5.3 Zeolites deposition

Once first templates are prepared, their compatibility with zeolites solution and deposition method is evaluated.

Zeolites-L are provided as powder material. A dissolution is prepared with 20 mg of solid material and 40 ml of ethanol. Sonication is used to make solution more uniform. Liquid delivering is tested by three different methods: spinning, inmersion or drop covering, in non patterned substrates. For spinning, the whole sample is covered with liquid and turned at 500 rpm, inmersion consists of the introduction of the substrate in the dissolution and N_2 drying, and drop delivering refers to surface covering followed either by N_2 or on air drying. The results show that both spinning (500 rpm) and drop delivering turn out well to place zeolites on the substrate, whereas immersion does not, at least for this solution concentration.

Deposition tests are realized on both types of templates. First, the ones fabricated by patterning of a negative resist and RIE are used. Spinning leads to low number of zeolites on the surface, but, indeed, a certain tendency to be placed on desired locations is seen (Figure 5.53, top). Trying to increment their number in the patterned structures by drop deposition, certainly increases the density on the whole sample, but also aggregation arises (Figure 5.53, bottom). In consequence, for optimal results an initial higher concentration of zeolites dissolution should be convenient, in combination with spinning delivering on templates with a deeper profile.

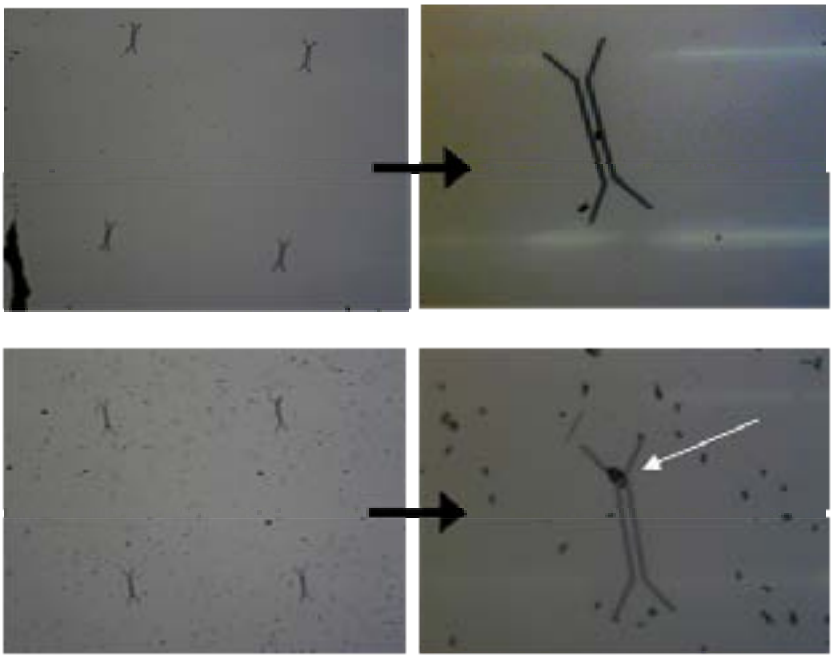

Figure 5.53 Deposition test of zeolites on the sample of negative resist and RIE. (Top) After one drop of zeolites solution deposition. Few zeolites are deposited. (Bottom) Addition of zeolites causes aggregates.

Similarly, solution deposition is performed on the samples of the second fabrication method, positive resist patterning. Ab initio, the weakness of this approach relies on the stripping of the resist since there was no experience on it for this specific case. It is essential than selectively placed zeolites inside the trenches remain there when resist layer is removed, in order to enable the CNT growth based on them.

First, spin delivery is tested on patterned copolymer. Same solution and spin speed are used and it results in a higher concentration of deposited zeolites, both on trenches and polymer surface. This may be due to the higher depth of the trenches (650 nm for copolymer vs 150 nm for previous approach), but also to a better affinity of zeolites with the resist, compared to silicon in the case above (Figure 5.54).

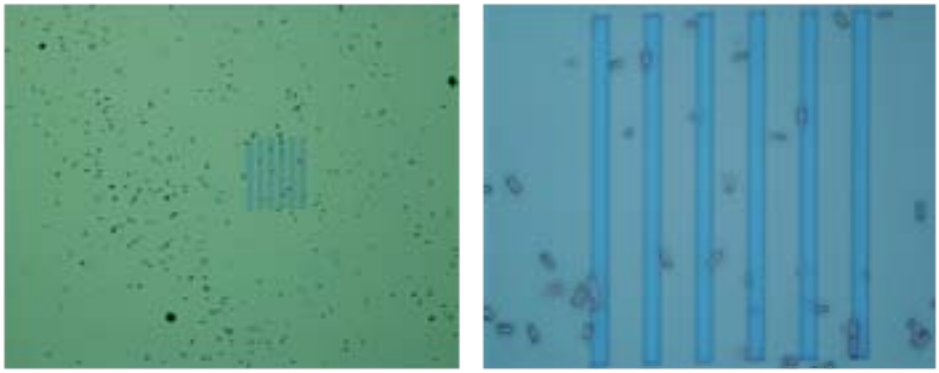

Figure 5.54 Deposition test of zeolites on the sample based on positive resist.

Again, the addition by drop delivering increases number of deposited zeolites and leads to the formation of aggregates (Figure 5.55). Therefore, it does not seem the more suitable way to increase concentration. Further templates may, for example, refine design dimensions (narrower and shorter trenches).

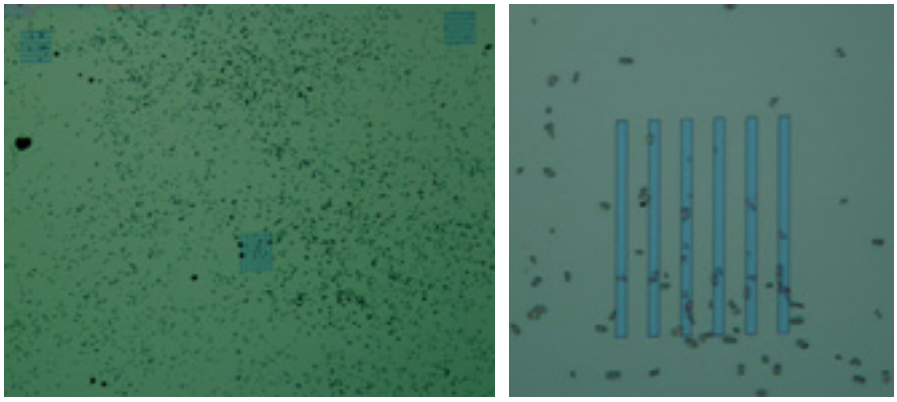

Figure 5.55 Iteration of zeolites deposition causes increase of zeolites deposited on desired locations.

The number of zeolites can be adjusted if the elimination of zeolites is feasible, keeping resist integrity. Immersion in IPA does not dissolve zeolites, but sonication in combination with IPA achieves a completely clean surface, with no effect over MMA-MAA layer (Figure 5.56). This result allows to precisely adjust the deposition by iteration, if needed.

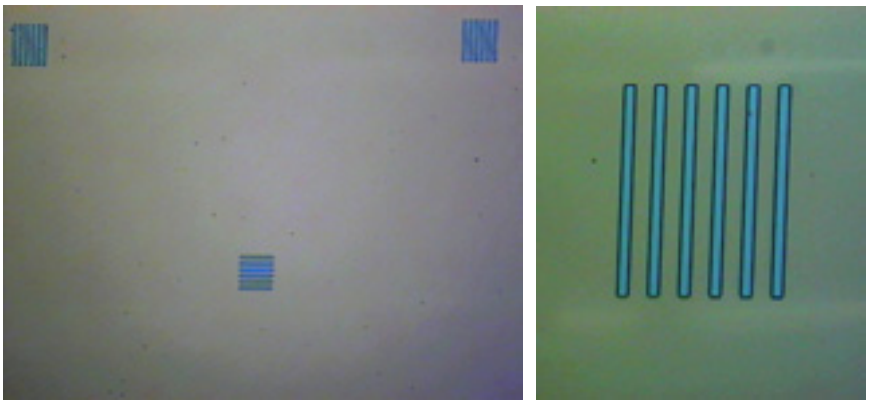

Figure 5.56 Zeolites removal is performed using IPA immersion and US bath. Resist is intact and zeolites deposition can be adjusted.

Final step is the mask elimination, without disturbing the zeolites deposited on the substrate and inside the trenches. In order to make optical inspection easier after resist stripping, a huge amount of zeolites are delivered (Figure 5.57, left). Co-polymer elimination in acetone resulted in re-deposition of some zeolites along the sample, but certainly, selectively placed zeolites remained absolutely intact (Figure 5.57, center and right), as defined by the original array of trenches.

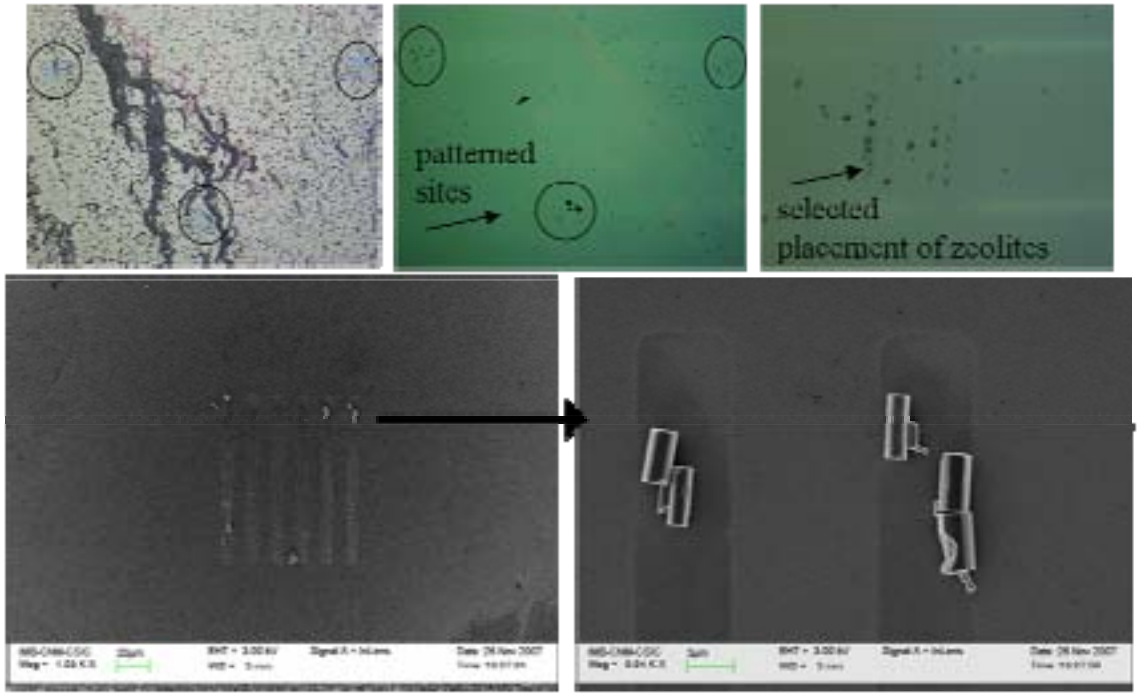

Figure 5.57 (Top) Elimination of copolymer is done in acetone. A big amount of zeolites are deposited (left). After stripping, patterned sites can be recognised (center). Zeolites placement is achieved (right). (Bottom) SEM images of another test for selective deposition of zeolites.

These exploratory works correspond to a first approach and, thus, have not been optimized in terms of fabrication, for the pattern design or resist thickness, neither for the etching nor the dissolution concentration. Both methods show promising results, specially the one based on positive resist for its simplicity. Efectively, positive resist patterning results a simpler method. It is a single fabrication step plus zeolites deposition, where resist patterning and post exposure processing (development, no etching and resist stripping) are easier. Next step should be the verification of synthesis of CNTs, in terms of growth and throughput, in combination with the local and oriented zeolite placement. However, it corroborates that engineering materials and technology strategies may support the introduction of CNT as building blocks of devices.

References

(1) P. Avouris
Carbon nanotube electronics and optoelectronics
Mrs Bulletin **29** (6), 403-410 (2004)

(2) P. Avouris, Z. H. Chen, and V. Perebeinos
Carbon-based electronics
Nature Nanotechnology **2** (10), 605-615 (2007)

(3) S. Iijima
Helical Microtubules of Graphitic Carbon
Nature **354** (6348), 56-58 (1991)

(4) M. Endo, K. Takeuchi, S. Igarashi, K. Kobori, M. Shiraishi, and H. W. Kroto
The Production and Structure of Pyrolytic Carbon Nanotubes (Pcnts)
Journal of Physics and Chemistry of Solids **54** (12), 1841-1848 (1993)

(5) Z. Chen
Nanotubes for Nanoelectronics
Encyclopedia of Nanoscience and Nanotechnology **X** (ISBN 1 58883 001 2), p. 1-24 (2004)

(6) Eindhoven University of Technology
The wondrous world of Carbon Nanotubes: a review of current carbon nanotube technologies
(2003)

(7) M. Dresselhaus, G. Dresselhaus, and P. Avouris
Carbon Nanotubes
Springer Verlag Editors (2001)

(8) Mukul Kumar and Yoshinori Ando
Single-wall and multi-wall carbon nanotubes from camphor--a botanical hydrocarbon
Diamond and Related Materials **12** (10-11), 1845-1850 (2003)

(9) M. F. Yu, O. Lourie, M. J. Dyer, K. Moloni, T. F. Kelly, and R. S. Ruoff
Strength and breaking mechanism of multiwalled carbon nanotubes under tensile load
Science **287** (5453), 637-640 (2000)

(10) J. C. Charlier, X. Blase, and S. Roche
Electronic and transport properties of nanotubes
Reviews of Modern Physics **79** (2), 677-732 (2007)

(11) G. Pennington and N. Goldsman
Semiclassical transport and phonon scattering of electrons in semiconducting carbon nanotubes
Physical Review B **68** (4) (2003)

(12) B. Shan and K. J. Cho
First principles study of work functions of single wall carbon nanotubes
Physical Review Letters **94** (23) (2005)

(13) J. Fraxedas, G. Rius, F. Perez-Murano, and A. Verdaguer
Determining radial breathing mode frequencies of single-walled carbon nanotubes with an atomic force microscope
EuroPhys. Lett. **78** (1) (2007)

(14) B. Shan, G. W. Lakatos, S. Peng, and K. J. Cho
First-principles study of band-gap change in deformed nanotubes
Applied Physics Letters **87** (17) (2005)

(15) T. W. Ebbesen and P. M. Ajayan
Large-Scale Synthesis of Carbon Nanotubes
Nature **358** (6383), 220-222 (1992)

(16) S. H. Jung, M. R. Kim, S. H. Jeong, S. U. Kim, O. J. Lee, K. H. Lee, J. H. Suh, and C. K. Park
High-yield synthesis of multi-walled carbon nanotubes by arc discharge in liquid nitrogen
Applied Physics a-Materials Science & Processing **76** (2), 285-286 (2003)

(17) S. J. Tans, A. R. M. Verschueren, and C. Dekker
Room-temperature transistor based on a single carbon nanotube
Nature **393** (6680), 49-52 (1998)

(18) R. Martel, T. Schmidt, H. R. Shea, T. Hertel, and P. Avouris
Single- and multi-wall carbon nanotube field-effect transistors
Applied Physics Letters **73** (17), 2447-2449 (1998)

(19) R. Martel, V. Derycke, J. Appenzeller, P. H. S. Wong, and P. Avouris
Carbon nanotube field-effect transistors and logic devices
Abstracts of Papers of the American Chemical Society **222**, U184-U185 (2001)

(20) V. Derycke, R. Martel, J. Appenzeller, and P. Avouris
Controlling doping and carrier injection in carbon nanotube transistors
Applied Physics Letters **80** (15), 2773-2775 (2002)

(21) W. Hoenlein, F. Kreupl, G.S. Duesberg, A.P. Graham, M. Liebau, R. Seidel, and E. Unger
Carbon nanotubes for microelectronics: status and future prospects
Materials Science and Engineering: C **23** (6-8), 663-669 (2003)

(22) A. Bachtold, P. Hadley, T. Nakanishi, and C. Dekker
Logic circuits with carbon nanotube transistors
Science **294** (5545), 1317-1320 (2001)

(23) J. Appenzeller, R. Martel, V. Derycke, M. Radosavjevic, S. Wind, D. Neumayer, and P. Avouris
Carbon nanotubes as potential building blocks for future nanoelectronics
Microelectronic Engineering **64** (1-4), 391-397 (2002)

(24) P. Avouris, R. Martel, V. Derycke, and J. Appenzeller
Carbon nanotube transistors and logic circuits
Physica B-Condensed Matter **323** (1-4), 6-14 (2002)

(25) S. Heinze, J. Tersoff, R. Martel, V. Derycke, J. Appenzeller, and P. Avouris
Carbon nanotubes as Schottky barrier transistors
Physical Review Letters **89** (10) (2002)

(26) Z. H. Chen, J. Appenzeller, J. Knoch, Y. M. Lin, and P. Avouris
The role of metal-nanotube contact in the performance of carbon nanotube field-effect transistors
Nano Letters **5** (7), 1497-1502 (2005)

(27) T. Durkop, B. M. Kim, and M. S. Fuhrer
Properties and applications of high-mobility semiconducting nanotubes
Journal of Physics-Condensed Matter **16** (18), R553-R580 (2004)

(28) T. Durkop, S. A. Getty, E. Cobas, and M. S. Fuhrer
Extraordinary mobility in semiconducting carbon nanotubes
Nano Letters **4** (1), 35-39 (2004)

(29) Crenatun
Crecimiento de Nanotubos de Carbono Unidireccional
INTRAM-FRON 2005-50F0151

(30) Sensonat
Tecnología para sistema sensores y electrodos basados en nanotubos de carbono
NAN2004-09306-C05-01

(31) J. Y. Park, S. Rosenblatt, Y. Yaish, V. Sazonova, H. Ustunel, S. Braig, T. A. Arias, P. W. Brouwer, and P. L. McEuen
Electron-phonon scattering in metallic single-walled carbon nanotubes
Nano Letters **4** (3), 517-520 (2004)

(32) I. Martin
Crecimiento de Nanotubos de Carbono mediante RTCVD con Nanopartículas Férricas
Treball de recerca, Universitat Autònoma de Barcelona (2007)

(33) R. Martel, V. Derycke, C. Lavoie, J. Appenzeller, K. K. Chan, J. Tersoff, and P. Avouris
Ambipolar electrical transport in semiconducting single-wall carbon nanotubes
Physical Review Letters **87** (25) (2001)

(34) S. Niyogi, M. A. Hamon, H. Hu, B. Zhao, P. Bhowmik, R. Sen, M. E. Itkis, and R. C. Haddon
Chemistry of single-walled carbon nanotubes
Accounts of Chemical Research **35** (12), 1105-1113 (2002)

(35) C. Staii and A. T. Johnson
DNA-decorated carbon nanotubes for chemical sensing
Nano Letters **5** (9), 1774-1778 (2005)

(36) J. Zhang, A. Boyd, A. Tselev, M. Paranjape, and P. Barbara
Mechanism of NO_2 detection in carbon nanotube field effect transistor chemical sensors
Applied Physics Letters **88** (12) (2006)

(37) C. Baerlocher, W.M. Meier, and D.H. Olson
Atlas of Zeolite Framework Type
Elsevier, 5th edition (2001)

The effect of charged particle irradiation is analized on different substrates. CMOS transistors are exposed to electron and ion beams at different incident energies and resulting damage is monitored on line. Motion of NEMS is induced by low energy electron beam delivery and modeling allows to establish a new method of NEMS actuation and detection. Damage of CNTFETs caused by electron beam irradiation is intensively studied in terms of electron beam energy, dose, etc. Dedicated AFM-based characterization complements these results to completely understand the electron beam induced effect on the CNT-based devices.

6 Study of the effect of charged particle irradiation on electronic nanodevices

Radiation effects refer to the consequences of energy in wave form or moving particles on matter and comprises neutral or charged species interactions. The mechanisms that they induce may vary from direct production of phenomena, reactions or scattering (excitation, ionization or atomic/ionic displacement), i.e. thermal, kinetic or quantum interactions (1). A great number of different charged particles are employed in a wide range of fields. Among others, electrons, protons or heavier atomic ions are used for many applications that range from fundamental studies to electronic goods or medical diagnosis and that exploit the effects of their interactions with other elements.

In the case of electrons, precisely because of its ionizing nature they can be used to overcome the imaging limitations of light and to reconstruct surface topography down to the nanometer scale. These are the foundations of SEM. However, there are additional electron beam induced effects. It is reported that electron beam irradiation induce surface or bulk processes, as diverse as surface oxidation, gas adsorption, dissociation, atomic/ionic migration, evaporation, contaminant or species desorption, adsorbate dissociation, etc (2).

As a matter of fact, EBL takes profit of the effect of electron exposure to intentionally modify the properties of resists by the selective degradation of their molecular bonds and it represents a useful tool for high resolution patterning. Other established methods, such as Electron Beam Induced Current (EBIC) (3) and Electron Beam Induced Deposition (EBID) (4), are also constructively used.

Contrarily, some of the effects may alter the characteristics of materials or devices unwisely (5, 6). In the following sections, some specific devices are analized in order to evaluate the use of SEM and EBL for both characterization and nanofabrication. Together with it, the findings or dedicated characterization that this study provides may result as much interesting as the central goal itself.

6.1 Effect of Electron Beam on CMOS integrated circuits and devices

The microelectronics industry is mainly based on CMOS circuits. The evaluation of device parameters, for example, under real applications, or their combination with other devices is of major interest for the improvement of their performance or for the development of new systems. The failure of devices evolved in an increased interest to study the causes of circuit damage or degradation. In addition, the aim to achieve the continuos downward scaling of devices for higher density, speed and resolution and low power consumption required the introduction of advanced fabrication methods, such as RIE or EBL, that should be compatible with the device operation.

Ionizing radiation is considered one of the causes of circuit and device alterations or damage. It may be encountered during electronic device use in real situations, such as radiation detection, but also may be present under X ray or electron beam imaging or processing methods, such as e-beam evaporation or EBL.

Mainly, the incidence of radiation is considered to break atomic bonds on Si and SiO_2 layers when a certain amount of energy is deposited on the solid. For SiO_2, the band gap is about 9 eV and it is considered that about the double (~18 eV) is enough to induce electron-hole pair creation (triple for semiconducting materials (7)). In consequence, a change in the charge and energy distribution of the MOS structure may occur. The generally accepted mechanism induced by ionizing radiation is schematized in Figure 6.1, for the case of electron exposure.

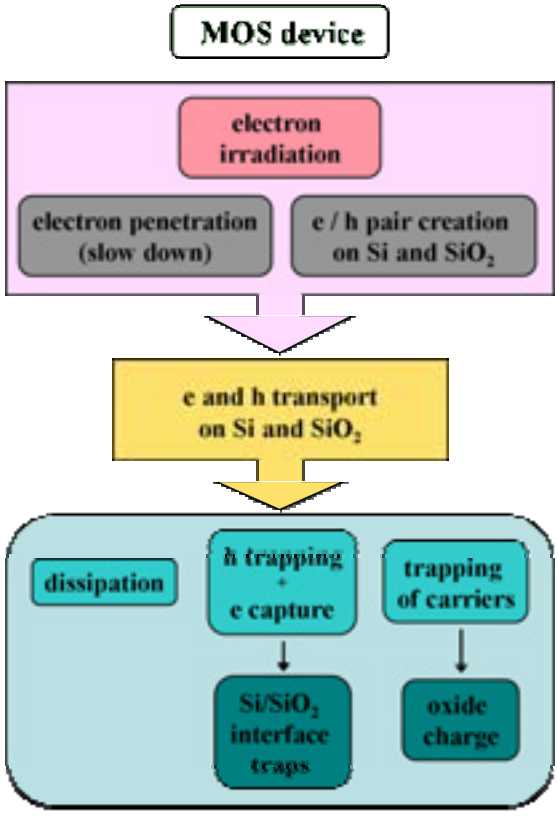

Figure 6.1 Scheme of the effect of electron beam irradiation on MOS devices (Adapted from (1)).

The effect of electron beam irradiation of MOS structures at energies of a few keV is described from the penetration of electron in the solid matrix and the interactions experienced by the charges. Incident electrons loose their energy as a result of elastic and inelastic collisions. They are slown down changing the incoming direction (trajectory) or creating electron–hole pairs, until they are completely stopped (see chapter 2 or 3 for a complementary description). The amount of created pairs is directly proportional to the absorbed energy and, hence, beam energy and dose determine the damage. A certain portion of the electron-hole pairs are almost immediately recombined, the rest suffer transport processes along metal, Si or SiO_2 layers. Electrons have high mobility, even into the SiO_2 matrix, whereas the effective mobility of holes is much lower. In consequence, most electrons move to the contacts (dissipation), whereas some holes remain trapped and cause a net positive charge in the SiO_2 layer. Another portion of the created holes move towards the Si/SiO_2 interface, where they can capture electrons. As a result, charged interface traps are created (Figure 6.2). In addition, the generation of electron–hole pairs may broke some chemical bonds that might act as electrically active defects and some SiO_2 impurities may be released. Interface traps and oxide charging are considered the major cause of damage or effect on device performance, in particular, concerning to SiO_2 contribution.

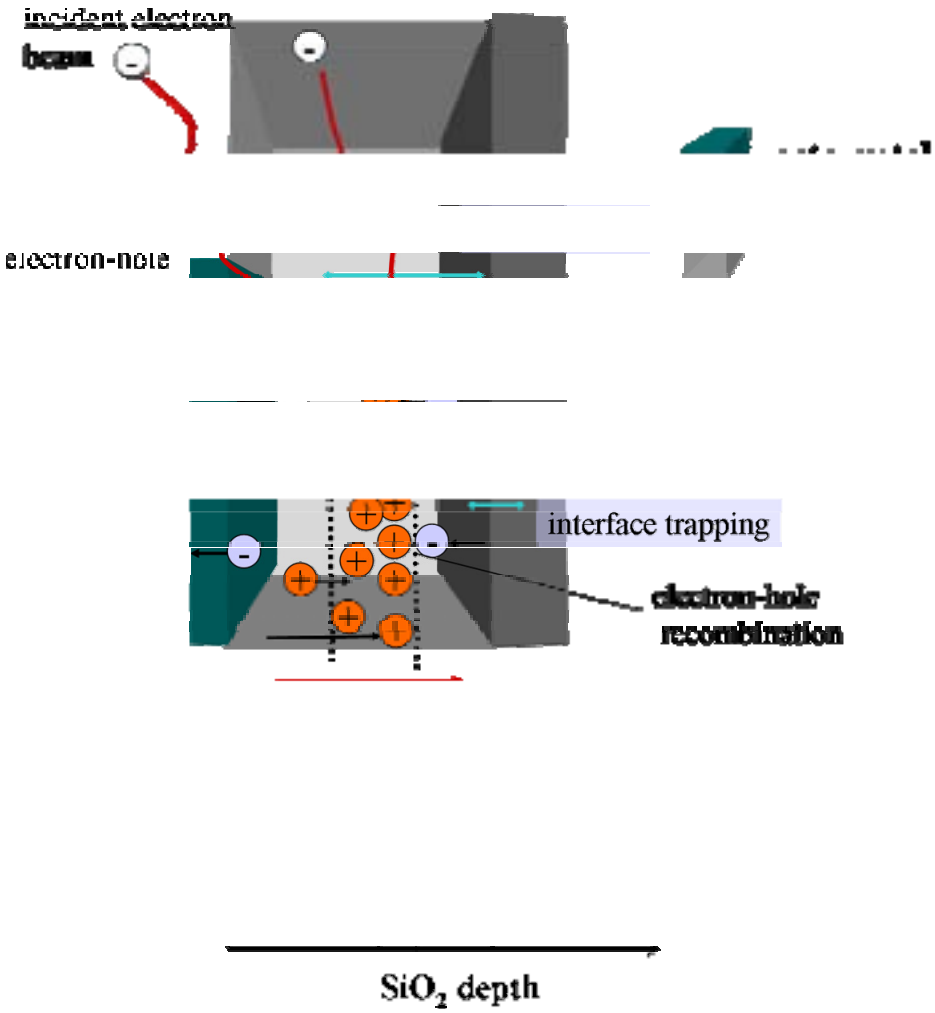

Figure 6.2 Mechanisms induced by electron beam exposure and representation of resulting charge distribution on MOS structures (Adapted from (8)).

The results of several studies of radiation effects on MOS devices and circuits are compiled in (1) and contribute to establish the fundamental mechanisms of the interactions and their effect on device performance, together with a better understanding of MOS structures and defect implications.

The performance of MOSFETs, the workhorse of semiconducting industry, can be explained considering a capacitor as a simpler configuration to describe the mechanism of operation of the MOS structure. A qualitative description in terms of energy band diagrams and the derivation of MOS C-V curves is described in (1). For the ideal case, some assumptions are considered (no leakage current, uniform doping, etc) and allow to determine the device performance as a function of the structure characteristics. Applying more realistic conditions to this description, the effect of non idealities is balanced. The difference in metal-semiconductor workfunction, immobile charges or mobile ions in the oxide or interface traps should be considered. Focusing on charges, both mobile and immobile particles in the SiO_2 layer cause a shift in the flatband voltage, whereas the interface traps modify the surface potentials and arise as an increase of capacitance. Applying this description to the devices, electron mobility in the channel, i.e. conduction, threshold voltage and transconductance may be altered.

The introduction of the ionizing radiation mechanism into this qualitative description allows to predict the changes in the device and circuit performance. In MOSFETs, the created net charge induces an additional electric field through the oxide layer and interface traps act as scattering centers and affect the carrier mobility. In consequence, on current decreases, threshold voltage is shifted and transconductance is lowered.

6.1.1 Damage during fabrication of CMOS-NEMS

Experimental evidences of the electron beam induced damage on electronic devices are found in the literature (2,9). In summary, all of them report a damage of the structure characteristics and, thus, degradation of the device or circuit performance. For MOSFETs, decrease in gain and shift of threshold voltage is translated to IC performance with slower response, higher leakage currents or even cease of operation.

The research undertaken in the frame of Nanomass II project (IST-2001-33068) included the monolithic integration of NEMS in CMOS circuits (10). The evaluation of EBL compatibility for the fabrication of the nanomechanical structures has been done in collaboration with Lund University (in Sweden) and Dra. Francesca Campabadal (from CNM-CSIC) and it is reported in (11).

Two different electron beam exposure approaches are tested. First, the effect of SEM imaging on the circuits is established (at CNM) and, second, the fabrication process based on EBL is experienced (by Lund University). All experiments are done at varying beam energies and doses on the same nMOS transistors. In particular, the chips are similar to the ones that are used in Chapter 4 for the integration of nanomechanical structures in CMOS and equivalent to the ones referenced in Figure 4.18. Specifically, an nMOS transistor is located in close proximity to an integration area (Figure 6.3, left). The gate of the transistor is directly connected to the integration area, as it is the case in the usual configuration of CMOS-NEMS.

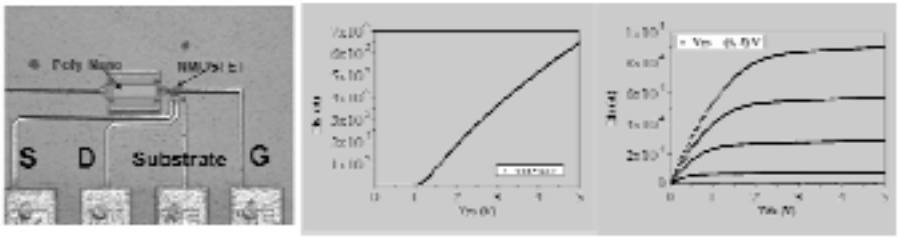

Figure 6.3 (Left) Optical image of the device used for the exposure tests.
(Center and right) Example of the electrical characteristics of one MOSFET.

In the first case, SEM imaging is performed directly on the whole integration area at 10 keV beam energy and, in the other, higher beam energy (30 keV) is used to expose a rectangular area of 10 x 40 μm^2 in the integration area. For both cases, a shift of threshold voltage to negative values and change in the transconductance appear. The decrease of the on current is higher for 30 keV beam energy. This behaviour is in agreement with the mechanism described in the previous section. Interface traps and oxide charging cause the change of circuit characteristics. Assessing the experimental conditions and configuration with Monte Carlo simulations of electron trajectories the effect can be more precisely inferred. As shown in Figure 6.4 top, the electron penetration range and its effect at 10 keV is limited close to the first Si/SiO_2 interface, whereas for 30 keV beam energy, electrons travel several microns within the structure, not only in depth, but also laterally. In consequence, higher damage at higher energies may be attributed to the electron beam effect on the two Si/SiO_2 interfaces, the oxide charging and even its effect on the closer transistor (Figure 6.4, bottom).

In the second exposure test, the cantilever fabrication process is analogous to the one described on Chapter 4 for the monolithical integration of resonating structures on CMOS circuits. In that case, circuits are measured before the EBL step and after the exposure, metal deposition and resist lift off. Beam energies ranging from 4 to 35 keV are tested. The results indicate that, again, high energies (>15 keV) cause an important degradation of the circuit performance and confirmed the previous assumptions. However, the effect is transitory and device performance recovering is registered at room temperature after a long period of time (a few months).

As a matter of fact, electron beam damage is not uniquely due to the beam energy and amount of dose, but it is the result of the relative values of the process variables, that is, beam energy, electron dose and structure configuration, in terms of materials, thickness, etc.

Results described above corroborate the necessity to adjust process parameters for NEMS fabrication in order to ensure prevention of the electron beam damage of MOS circuits. The demonstration of the compatibility of low beam energy (3 keV) for EBL is reported in (12) and an equivalent approach is also presented in (13). As mentioned, the electron penetration depth of electrons using 3 keV is almost limited to the resist layer and just a little portion of polysilicon layer. In addition, the lowest the beam energy, the lowest the clearing dose (e.g. for 950k MW PMMA is ~100 $\mu C/cm^2$ at 10 keV vs ~30 $\mu C/cm^2$ at 3 keV, see chapter 3). Hence, electrons are far from expected to reach Si/SiO_2 interface and exposure doses are indirect and relatively low. In addition, the oxide layer is etched for the release of the structure in a portion of the integration area, which implies than even part of the damage causes are eliminated during wet etching.

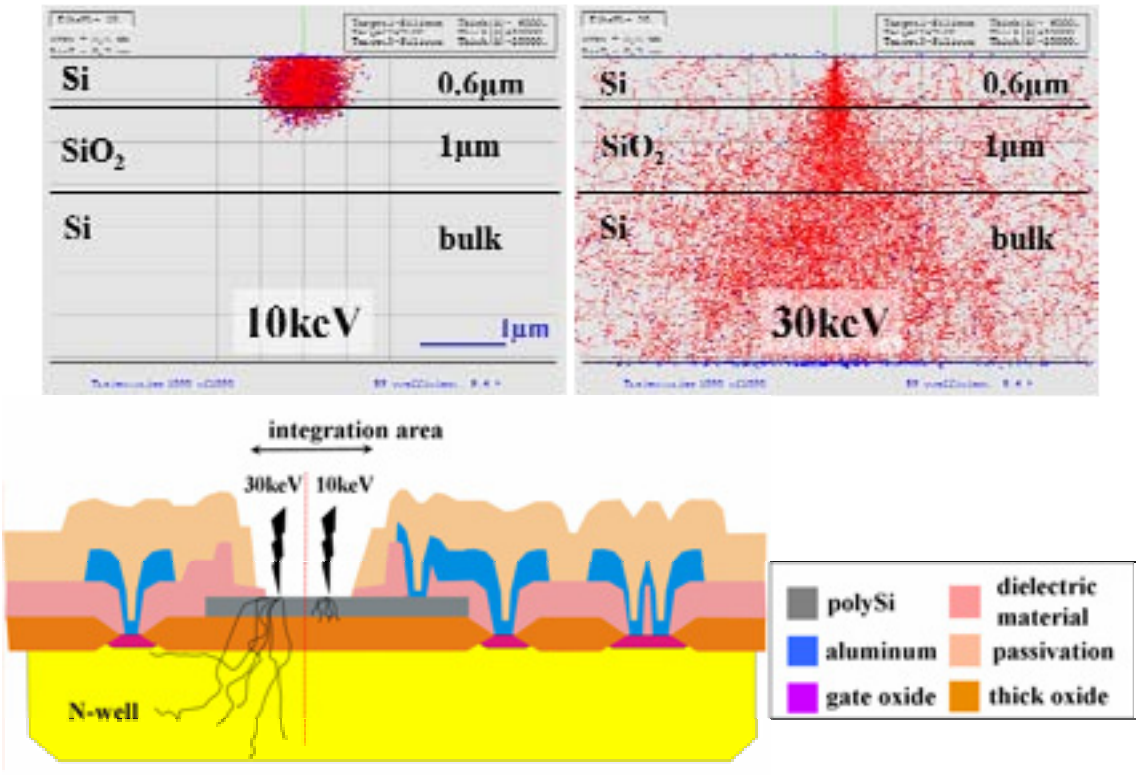

Figure 6.4 (Top) Electron trajectories simulations for 10 and 30 keV beam energy on the MOS structure with layer thicknesses analogous to the real integration area. (Bottom) representation of electron range on the MOS circuit configuration at both beam energies. Electrons may even reach the transistors at 30 keV.

In section 4.5, an alternative fabrication method based on FIB milling is presented. The implications are important in terms of fundamental information about the interaction of charged particles on solids, but specially for testing the applicability of FIB as a fabrication tool. No significant damage is induced in the present case (Figure 4.22). Even if Ga^+ beam is driven at 30 kV acceleration voltage, ions do not penetrate deep in the solid (in this case, Si). Even though it is accepted that implantation or doping occurs during ion exposure (14), the results indicate that a certain minimal dose is needed to alter significantly the structure performance. In addition, the SEM assisstance, at low beam energy and fast scan rate, is in consequence proved to be compatible with this FIB-based fabrication process.

Specially oriented exposure tests have been realized to corroborate the experiments described above and to study the fabrication compatibility in terms of exposure conditions. In particular, irradiation tests are performed at both 3 and 30 keV electron beam energy and 30 keV ion beam energy. The procedure is based on the on-line monitoring of the effect, on the MOS transistors (in Figure 6.3 and 6.4 (bottom)) during the incidence of charged particle beams (i.e. simultaneously to exposure).

In order to do it, samples are processed using FIB (as mentioned in Chapter 4, dual beam - Ga^+ ions and electrons) and in situ connection of the devices with the micropositioning probes placed inside the FIB chamber. The electrical performance of the devices is determined with the semiconductor analizer HP4155 (Figure 5.16, right). Two kind of curves are acquired: Ids/t, for obtaining the change of device conduction simultaneous to the exposure, and Ids/Vds, to establish more accurately the effect on device characteristics (transconductance, threshold voltage, etc). For the Ids as a

function of time, the polarization conditions are common for all the measurements: Vd = Vg = 5 V. Basically, two positions are irradiated: the integration area (i.e. equivalent to the fabrication of integrated nanomechanical structures) and the (passivated) transistor (i.e. imaging). For electron exposure the smallest aperture (7.5 µm) is used, which implies 8 and 22 pA for 3 and 30 keV, respectively, as measured using a Faraday cup. For ions, several apertures are tested, which determine beam currents from 1 to 200 pA.

The results of electron beam exposure clearly show that the main damage is produced when the transistor is directly irradiated (Figure 6.5) and that high electron beam energies (30 keV) (Figure 6.5, right) cause more important effect than low beam energies (3 keV). In any case, the induced effect has certain transitory nature and spontaneously is partially recovered.

Figure 6.5 Change of Ids during electron beam exposure. The main damage is induced if transistor is directly exposed to the 30 keV electron beam.

In the case of ion beam irradiation, the effect on the device is observed exposing an area (20 x 35 µm^2) covering the transistor. Exposure time is 2.8 s. The results for 1 pA ion beam are shown in Figure 6.6. A change of Ids is obtained when exposing the transistor, in the same order of the change registered for 3 keV electron beam, but opposite sign. The main aspect, as compared to electrons, is that, in this case, fast recovering is not observed. Exposure on the integration area leads to insignificant alteration of transistor performance. A SEM image at 3 keV after transistor irradiations not only accounts for the exposure that has been realized (darker area), but again accounts for the same effect (current increase) that it has been previously described in Figure 6.5, left.

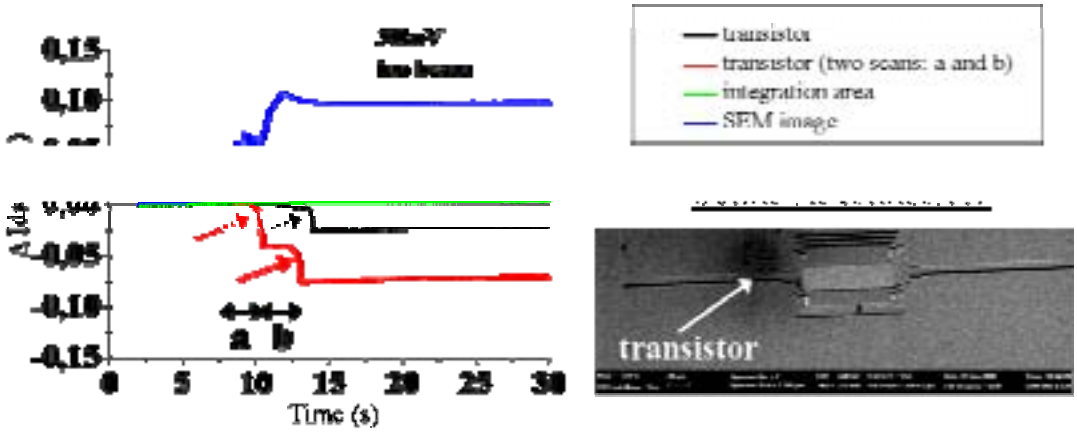

Figure 6.6 Change of Ids for the different irradiation test using Ga^+ beam. Ion beam does not cause effect when the integration area is exposed, whereas transistor irradiation does. Subsequent SEM imaging compensates the ion beam induced effect.

Some additional ion beam exposure tests have been realized on the integration area in order to evaluate the contribution of ion beam current. Higher apertures, up to 200 pA, are used on different scan time and area conditions. The results indicate a strong dependence on the exposure shape and dose, which can be correlated with either milling or implantation caused by Ga ions on the Si layer.

The interpretation of the results obtained for electrons are in agreement with the experiments and discussion reported in (11). The penetration depth at high beam energies is correlated with a higher effect on MOS transistor performance and the damage can be attributed to the oxide charge and Si/SiO_2 interface electron-hole pairs.

In the case of ion beam exposure, at low doses, on the transistor, the effect is significantly lower than for electrons due to the short penetration depth in the passivation layer. However, for higher doses, irreversible damage might be expected if the protection layer is removed due to milling. Further experiments will be realized soonly.

Regarding to device performance, the degradation of its characteristics is clear, as presented in Figure 6.7. Alteration of the threshold voltage and decrease of transconductance is registered. Even, current saturation is not clear if it does occur after exposure. The main effect is obtained when the transistor is discretely exposed with electrons (spot) twice (jump from red to green curve, Figure 6.7, left) and lower damage is obtained for ion beam exposure at low doses (green curve, Figure 6.7, right).

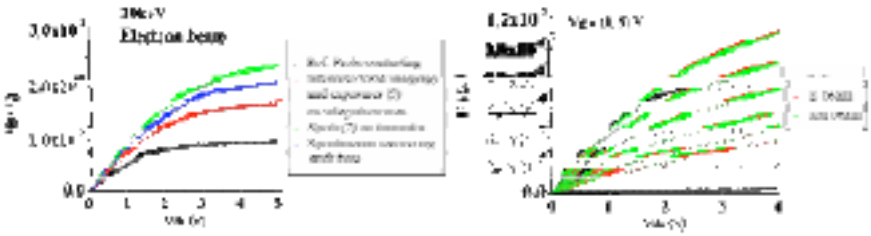

Figure 6.7 (Left) Different electron beam exposures have been realized between the different curves. The higher effect is obtained for direct transistor irradiation. All curves correspond to Vg = 5 V.
(Right) From the reference curve (black), the degradation of transistor characteristics is clear. More significant for electron beam exposure (red) than for ion beam irradiation (green).

In conclusion, the results determine the safer exposure conditions that might be used when the fabrication process on MOS devices is executed by means of charged particle beams. For electrons, low beam energy and far enough from the transistor position is required. For ion beam, correct dose must be determined and it has to be executed away from the circuit area. In addition, the experimental results define the changes of device performance that can be expected after beam based lithography or SEM imaging.

6.1.2 Electron Beam induced motion of NEMS

SEM is a powerful imaging tool that provides high spatial resolution information about devices and systems. It is based on the re-ejected electrons produced by the specific interaction of incident electrons with the solid substrate. Hence, information about material, topography, dimensions, etc can be obtained. However, it is obvious that sample integrity is not always guaranteed, even at very low beam energy. The ionizing nature of electrons can cause modifications and alteration of their performance. But, here, a particular favorable application of electron beam is presented.

During micro and nanofabrication, SEM is often used to monitor the evolution of the sequential fabrication processes. The consequences of SEM imaging on nanomechanical structures monolithically integrated into CMOS circuits appear as a novel application of electron beam scanning. The description of the experimental conditions, variables, mechanism of operation and process modelling enables to establish the basis of a new and complete NEMS, including the three system elements: transducer, actuator and sensor.

The nanomechanical element consists of a resonating cantilever with an electrode located very close, for electrostatic actuation and capacitive read-out, as described in (13). It is placed in a dedicated area of a CMOS circuitry and it has been fabricated as a post-CMOS process based on EBL (see chapter 4 for the details of fabrication). The aim of the imaging session is to determine precisely the dimensions of the nanomechanical structure, in order to relate them with the system performance characteristics (resonance frequency, Q, ...).

Experimental conditions

SEM imaging is performed at 3 keV beam energy with a 20 μm diameter aperture size. The sample is mounted in a standard Al sample holder by means of a carbon conductive sticker on a stub. A general view of the integration area is shown in Figure 6.8, where the nanomechanical element, driver and connecting paths to the CMOS circuit can be observed. In particular, the resonating structure is connected to the IC, i.e. in contact with sample substrate, whereas driver is floating. Motion actuation is, tipically, performed applying external bias through contact pad (white circle).

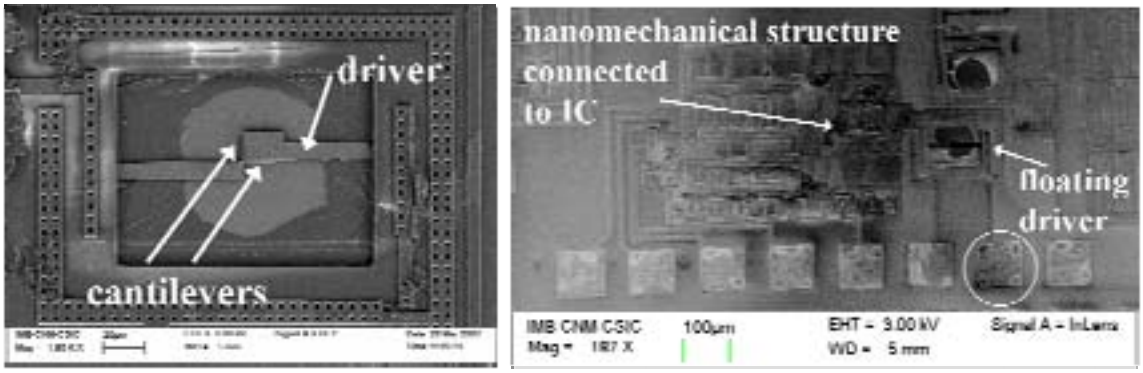

Figure 6.8 SEM images of the general view of an integration area with the integrated nanomechanical element (right) and the whole system (left). Double cantilever system is directly connected to the CMOS circuit. Driver is isolated from the sample substrate. Actuation is performed externally (white circle).

Determination of the electron beam induced movement

Fast scan imaging is used to quickly locate the movable element and then high resolution images (this is slow scan images or higher scan time) at high magnification are performed, in order to determine exactly the cantilever width and separation to the driver. As can be observed in the left side of Figure 6.9, the cause of cantilever deflection phenomena has to be related with the electron beam delivery and charge, since no other movement induction is applied. The same behaviour is observed in another integration area (Figure 6.9, right). The image at lower magnification and fast scan speed causes no effect on the cantilever, whereas slow scan in a reduced portion, again nearby the final point of the cantilever, produces the lateral collapse of the cantilever to the driver. In consequence, the cantilever displacement is not directly related with the image magnification.

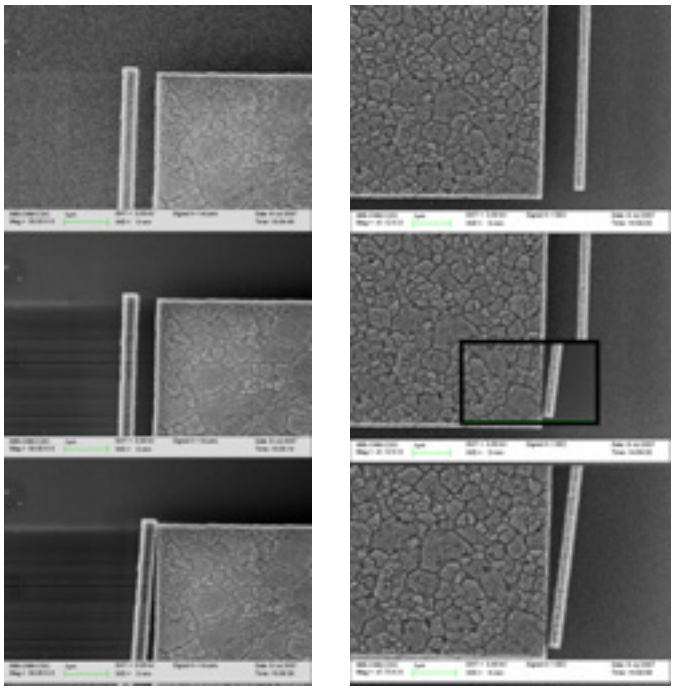

Figure 6.9 Cantilever deflection is induced by SEM image.
(Left) Increase of image scan time results in cantilever displacement.
(Right) Reduced SEM image at higher scan time again causes cantilever deflection.

The determination of the variables of the process is tested next. The system of two cantilevers with different separation to the driver enables to determine configuration conditions for the electron beam induced effect. Reduced imaging in the more separated element (horizontal cantilever) reveals the displacement of the second cantilever (vertical) when a general image is immediately acquired. This fact not only indicates the importance of the separation to the driver, but also accounts for the deslocalization of the interaction (Figure 6.10). Hence, it makes sense to attribute the phenomena to charge effects in the driver area.

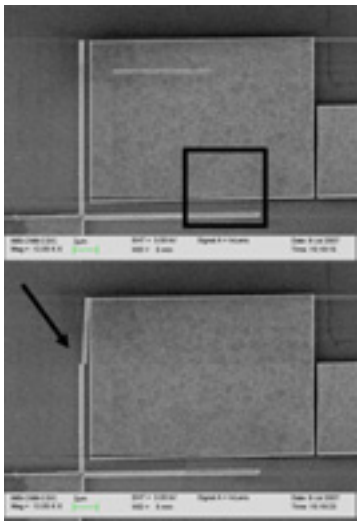

Figure 6.10 Reduced SEM image in the horizontal cantilever appears to be the induction factor of vertical cantilever deflection. Image scan has been stopped where the arrow is pointing.

However, the exceptional characteristic of the process is that cantilever movement induced by electron beam is not restricted to permanent displacement. As a matter of fact, some of them do not remain sticked to the driver, but return to the original position. More importanly, they show periodic movement that directly relates with higher scan time (slower image).

In the Figure 6.11, an example of this dependence is presented. The same cantilever is imaged under different scan speeds for three different exposed areas of the driver. For a constant scanning area, the higher the scan time, more times is repeated the cantilever motion along the image. At the same scan speed, a bigger imaging area results in faster periodic motion.

Figure 6.11 The black lines indicate the limits of the scanned area.
Images arranged in rows correspond to the three different exposure areas,
whereas they are presented in columns for the equivalent scan speeds.

However, it is not simply related with the total amount of charge received by the driver in each cycle and appears modulated by the rate of each line scan. Doubling both the scan area and the image time do not lead to the same periodic movement if the additional portion of the image is out of the driver. The evidence of this fact can be deduced from the right side image of Figure 6.12. The defect in the driver (hole) causes that longer exposure is needed to accomplish the cantilever displacement. The discharge rate per line scan is faster than charging rate. In addition, it is not a constant speed movement, otherwise, acceleration can be observed in the upper displacements, that have wider amplitude.

Up to now, the signal of the secondary electron detector is shown in the figures (see chapter 2). However, monitoring the Inlens detector signal corroborates the charged nature of the electron beam based phenomena. The induction of cantilever movement is directly related with the signal contrast. As it is observed on insulators, when charging occurs, signal of Inlens detector significantly increases. This is, sample accumulated charges partially screen electron incidence and higher angle-scattered electrons are collected (Figure 6.12, left and center). In addition, it is confirmed that electron beam induced motion is independent of scan direction nor sense.

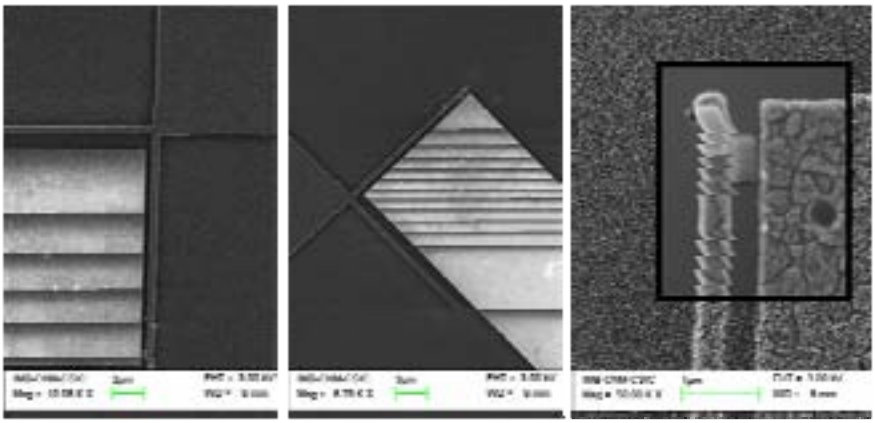

Figure 6.12 (Left and center) Charging effect can be monitored using Inlens detector. Scan direction nor sense are not determinant to induce the cantilever movement. (Right) The hole causes that line scan discharge compensates input charge.

Mechanism of electron beam induced motion

The interpretation of the cause and mechanism for cantilever motion can be determined considering the whole system. Electronic charge incident on the driver during SEM imaging is partially accumulated. This is due to the fact that the rate of constant electron delivery is higher than the charge dissipation rate from the driver. In addition, electron penetration of electrons on Si at 3 keV beam energy does not exceed 10 nm in depth. In consequence, an attractive electrostatic force is exerted on the cantilever causing its displacement. A certain amount of charge, i.e. determined electrostatic potential, is needed to displace cantilever to the maximum amplitude permitted by the configuration, the separation to the driver. When the cantilever touches the driver, electrons find a fast path to flow and driver discharge is instantaneous.

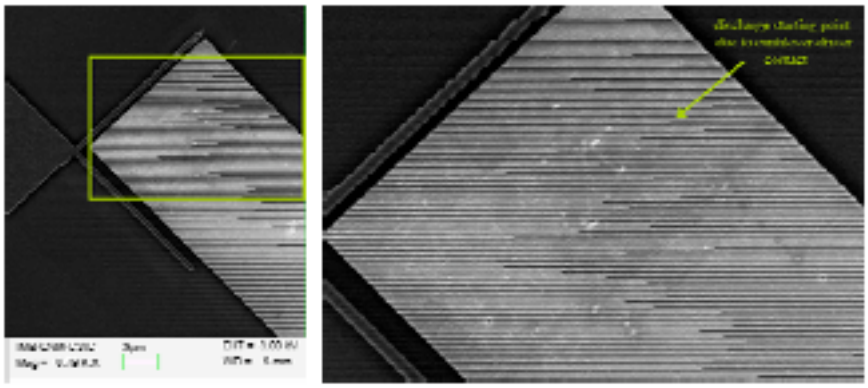

Figure 6.13 SEM image of the cantilever motion induced by the electron beam.
The arrow in the magnified portion of the image (right) remarks the discharge point.

A simple dynamical model based on this process is described. The mechanics of the movable element, the cantilever, is determined by the structuring material and its dimensions and it is expressed by the elastic constant, k (15),

$$k = \frac{E}{4}\frac{\omega^3}{l^3}t(Nm^{-1}) \tag{6.1}$$

where E is the Young modulus and ω, l and t are the width, length and thickness of the cantilever, respectively. The response of the cantilever to the application of a voltage through the close driver is described in (16, 17). For a certain voltage, called the snap-in voltage (Vsi), the cantilever deflection is so large that collapses to the driver. It is expressed by,

$$V_{si} = \sqrt{0.22\frac{E}{\varepsilon_0}\frac{\omega^3 s^3}{l^4}}(V) \tag{6.2}$$

where s is the distance between driver and cantilever and ε_0 is the permittivity in vacuum.

Considering the charging process of the driver to behave as the addition of charges in a conductive rectangular plate, the potential caused by each accumulated electron can be approximated as,

$$V_{e-} = \sqrt{\frac{8}{27}\frac{k}{\varepsilon_0}\frac{s^3}{A}}(V) \tag{6.3}$$

where A is the driver area.

The number of electrons and, hence, the maximum charge that is stored in the driver before cantilever collapses is theoretically determined. The dynamics of the charging process is the balance of constant electron beam delivery and spontaneous

discharge process, considering the discharge process characterized by a time constant, $\tau=RC$. Incident charge can be determined from the dimensions of the exposure area in the SEM image, the image scan time and the beam current (measured with the Faraday cup). This value is modulated by a certain factor (<1) that accounts for the portion of the electron beam delivery that is effectively delivered on the driver area, the ratio of incident electrons that contribute to the potential. Matching the experimental results (exp) for the cantilever collapse and this model (th) is shown in Figure 6.14.

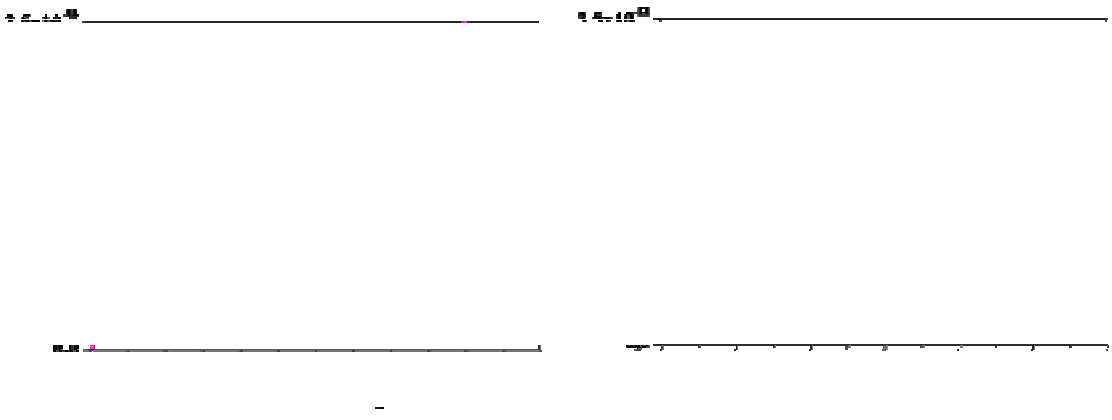

Figure 6.14 Plots of both experimental and modelled results for the electron beam induced motion of cantilevers. (Left) Charge as a function of number of line scans for different values of the time constant τ. (Right) Charge as a function of the number of line scans for different values of the effective exposure area.

The model predictions are in agreement with the experimental results, both qualitatively and quantitatively, refered to the number of image scan lines that are necessary to induce the motion. If time constant value is very low (fast dissipation rate), it may be possible that snap-in charge is not reachable. That is what occured in the example shown in Figure 6.9 and 6.10, where until accumulation does not exceed discharge per line, cantilever is immobile. On the contrary, for a system with lower dissipation rate, the charge evolution tends to linearity. Concerning to the efficiency factor, the higher the ratio of electrons that are absorbed in the driver, the less scan lines are needed to reach the snap-in potential. As shown in Figure 6.11, adjusting scan area to be a minimum time out of the driver, the increase of driver scan area implies that less scan lines are needed to move the cantilever.

The potential applications of this robust system comprise both fundamental and technological studies. The limit of validity of the theoretical assumptions in nanomechanical elements can be evaluated with the choice of system configuration (cantilever structure, driver dimensions, etc). Technologically, the performance of this configuraton may be compared with other conventional techniques for motion excitation and read-out. The simplicity of operation of this system is remarkable. The actuation method is, at the same time, the sensing method and signal transduction is direct. On-line excitation and monitoring enables to adapt in situ the experimental conditions for the best operation. Hence, beam current can be increased or decreased, image area and portion on the driver can be adjusted, efficiency may be improved with beam energy, etc and, in consequence, it is possible to select the motion period (Figure 6.15). In terms of energy, only one source is necessary, this is the SEM supply, and dissipation energy and noise, typical from electric transduction, are avoided.

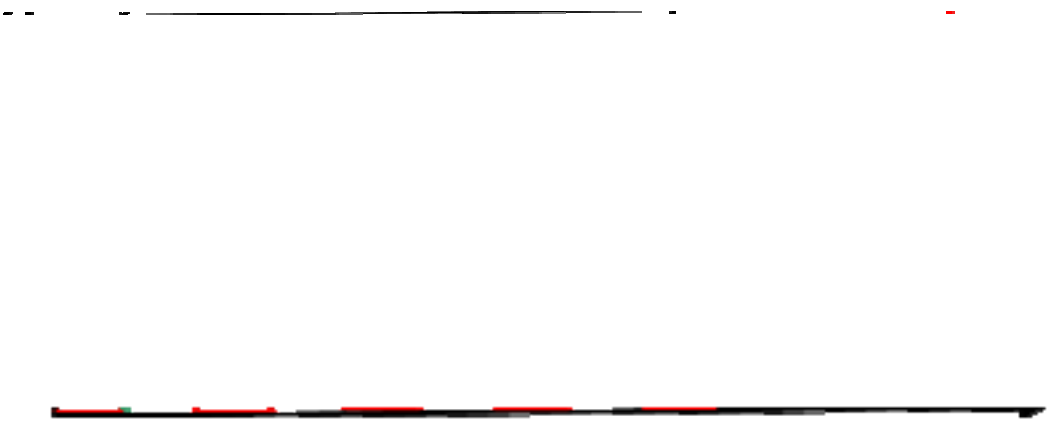

Figure 6.15 Model for the mechanism that induces cantilever motion.
Predicting motion charge (Qsi) from the nanomechanical element and separation to the driver, electron beam delivery can be adjusted to induce the desired displacement by beam current, line scan structure (time and position) and driver/circuit area. Efficiency may be improved selecting beam energy.

6.2 Atomic Force Microscopy based characterization techniques

Scanning probe microscopy (SPM) comprises a wide range of high resolution characterization techniques. Among others, TappingMode™ (also denominated Amplitude Modulation, dynamic mode AFM) atomic force microscopy (AFM) is the most popular scanning method for imaging, thanks to the improved control of the tip-sample interaction. The problems associated with conventional contact mode scanning in terms of sample damage (friction, adhesion, etc) or image distortion (e.g. due to electrostatic forces) are minimized.

In dynamic AFM, the tip is scanned across the sample surface combining punctual contact for high resolution and lift to avoid damage and distortion. The cantilever is excited at or near its natural resonance frequency. During scanning, the free resonance amplitude is reduced due to energy losses in tip-sample contact. The surface reconstruction consists of the compensation of height variations caused by sample topography by means of the feedback loop. The controlling electronics keeps constant the oscillation amplitude adjusting the tip-sample distance (18).

Electrical Force Microcopy (EFM) and Kelvin Probe Force Microscopy (KPFM) are two of the AFM-based techniques based on this scanning method. In this case, long-range Coulomb forces are used to monitor the electrical properties of the sample, whether on the surface or just beneath. The interaction with the AFM conductive tip causes changes in the oscillation amplitude and phase (Figure 6.16, left). Using the so called LiftMode the contribution of topography is compensated. LiftMode consists of two passes across each scan line. In the first pass, the height profile is recorded and, in the second, these data are used to lift the tip above the surface with an adjustable constant separation, lift height (Figure 6.16, right). Hence, phase changes are univoquely attributed to the electrical field interaction between tip and sample (19).

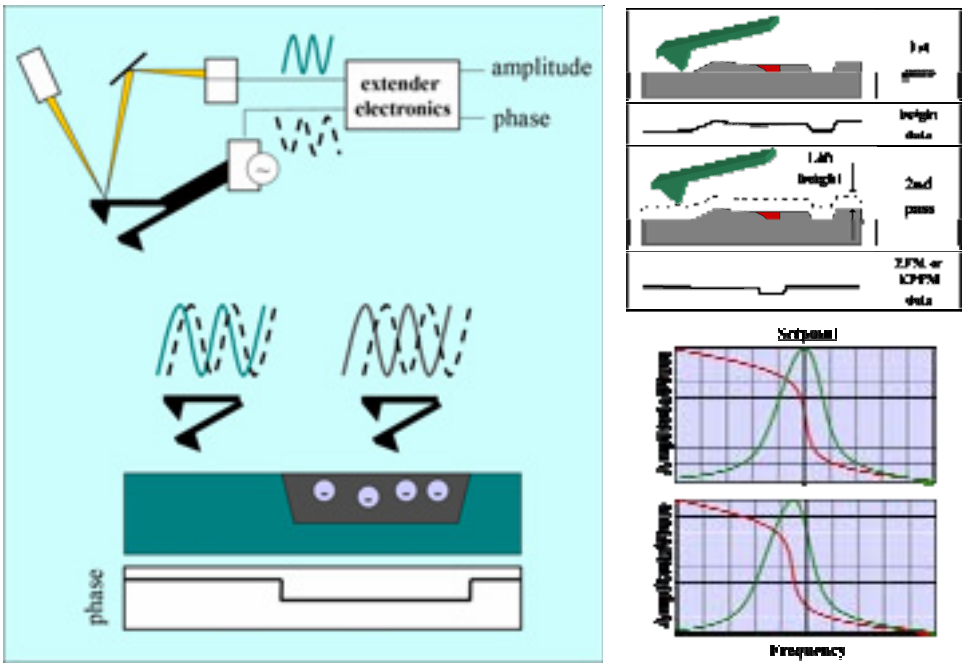

Figure 6.16 Operation of AFM during EFM and KPFM. (Left) Principle of Phase imaging. (Right) Representation of LiftMode and Resonance Shift.

All the measurements that will be related in the following sections (6.2.1 and 6.2.2) are performed in a commercial microscope placed at the Nanofabrication laboratory at CNM. The relative humidity is limited approximately between 30 and 60 %, which implies that AFM based measurements are susceptible to its variability. The AFM is composed of Nanoscope IV controller and Dimension 3100 from Veeco. The head has closed loop XY scanner with a maximum scanner range of 80 microns. The sample can be contacted externally either with micropositioners or by the chuck. Both EFM and KPFM measurements are directly implemented by the Nanoscope IV software and controller. The current measurements from the tip can be measured using the TUNA module, which allows to detect current from 100 fA to 10 nA.

6.2.1 Electrical Force Microscopy

Phase imaging (20), this is phase detection in Tapping Mode AFM, surpasses topographical determination to resolve surface material composition, friction, etc, but also informs about electrical and magnetic properties of the sample.

EFM accounts for the gradient of electric field between the tip and the sample and, thus, it is very convenient to obtain information about the induced effect of electron beam exposure on different configurations with high spatial resolution.

Three different detection modes can be derived from the resonance frequency shift in Figure 6.16, right, amplitude detection, phase detection or frequency modulation. The data acquisition is schematized in Figure 6.17. Phase detection is preferred, since it is the most sensitive. In general, the built-in electric field gradient provides enough contrast to be recorded, but also it can be induced by applying a voltage directly to the tip from the microscope electronics.

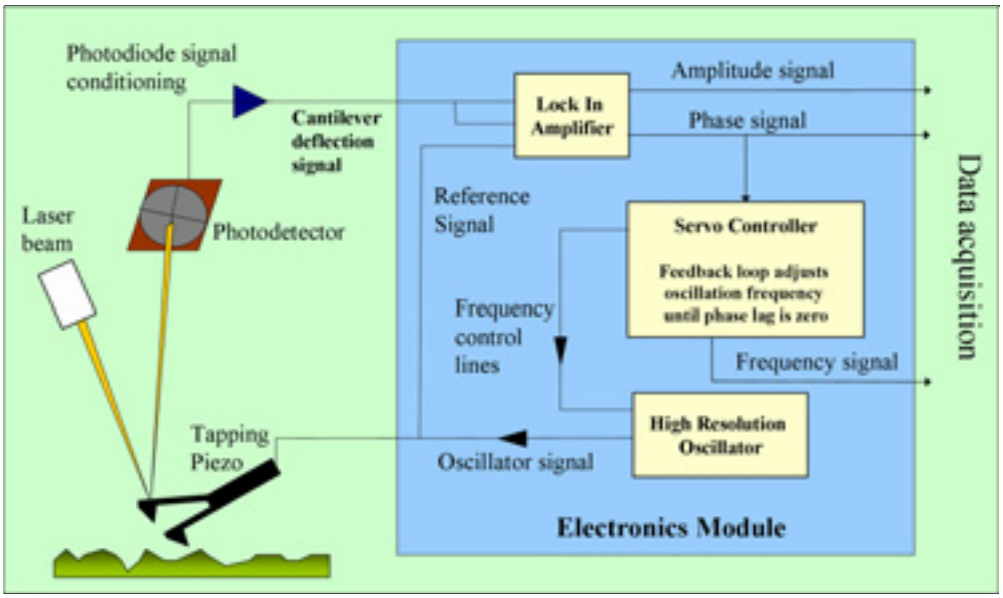

Figure 6.17. Scheme of the microscope operation
for the different detection techniques during EFM, from (19).

Electron beam irradiations of different surfaces at varying energies and exposure doses are characterized by EFM. In particular, typical examples of nanofabrication conditions are tested: substrates such as Si, SiO_2 or Au, beam energies of 3 and 10 keV and doses ranging from 100 (PMMA clearing dose) to 33.000 μC/cm^2. Conductive commercial Si tips covered with Pt are used.

Slightly doped Si samples, with native oxide, are directly exposed to the electron beam on selected sample coordinates. The results of phase detection are presented in Figure 6.18. The effect of the exposure shows a high contrast for electron doses higher than 10.000 μC/cm^2. At low energy, the squared shape of the feature is mantained, whereas for 10 keV pattern is distorted as a result of electron penetration depth and higher scattering angles. Even if the tip shows a strong changeability that difficults the data acquisition, the possibility to use phase detection to monitor charge effect on the surface as a function of dose and energy is demonstrated. As reported in (21), electron beam irradiation at a few eV on Si induces modification of the charges of the Si surface. In particular, the change of wettability properties after electron beam exposure can be used for selective functionalization. As an example, for SiO_2 it is attributed to the modification of surface free energy (22).

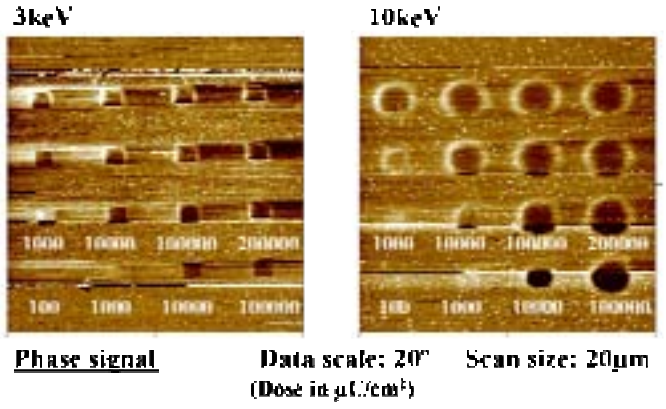

Figure 6.18 Phase imaging of an electron beam exposure test on a Si substrate
at 3 (left) and 10 keV (right). Doses range from 100 to 330.000 μC/cm^2.

In order to establish the EFM imaging procedure, different scanning conditions are tested. In particular, different lift heights, amplitude setpoint and tip bias are registered in a same image to compare their influence in the image contrast of the electrical field gradient. A long rectangle of 25 x 3 μm is irradiated at 3 keV on a layer of 200 nm thick SiO_2 on Si. As can be seen in Figure 6.19, for all these cases, phase signal is lower in the exposed area, but the constrast is enhanced with optimized choice of amplitude setpoint. The results reinforce the idea that a strong sensitivity of EFM signal with tip, scanning and surface conditions exists and corroborate the charge spatial confinement at low electron beam energies.

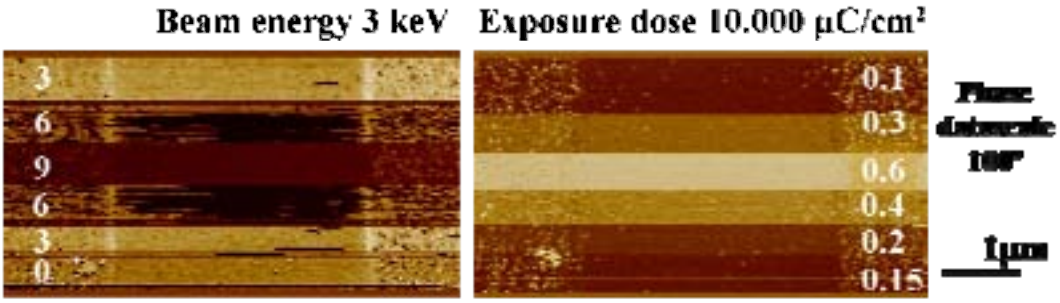

Figure 6.19 EFM images of an electron beam exposure at 3 keV on 200 nm of SiO_2.
Signal contrast changes with the variation of image scanning parameters, lift height (left) and amplitude setpoint (right). No external voltage is applied between tip and sample.

However, data acquired after equivalent exposure conditions on similar samples show that phase reversal may occur when changing lift height or if tip bias is applied. It is not possible nor easy to attribute the exact cause or to quantify electron beam effect in terms of charge signal or imaging parameters contribution. An example of such behaviour is shown in Figure 6.20. Same material configuration (200 nm of silicon oxide on Si) for different samples have been used to be exposed with the same beam energy. For one sample, the exposed areas with lift height 0 and 5 nm appear as depressions (Figure 6.20, left and center), whereas for 10 nm lift height as protusions. In another sample, using lift height of 10 nm, exposure also is registered as protusions. In both cases, signal contrast is lower if lift is applied, whereas the shape of the charge d area is absolutely equivalent to the case without applied lift.

Figure 6.20 EFM images resulting from electron beam exposures of 200 nm of SiO_2 at 3 keV.
Left and center images correspond to the same exposure with different lift height.
On the right, change of lift height and different sample presents inverse signal contrast.

Studying the time evolution of the signal, the dissipation of the electron beam exposure is observed. The results above are all obtained the same day that irradiation has been realized. As an example, an area just after exposure or 22 days later is included in Figure 6.21. Only a few remaining charges can be detected, corresponding to the higher exposure doses at 10 keV. For the same exposure doses and sample at 3 keV exposure effect completely disappears. The simultaneous acquisition of topographical image (during first scan pass) allows to verify the correct positioning of the image, when electron beam induced field disappears. In fact, electric field decrease can be monitored in a smaller time scale. Lower electric field gradient is yet detected along the same exposure day and subsequent days. The discharge phenomena is in agreement with precedent results (11).

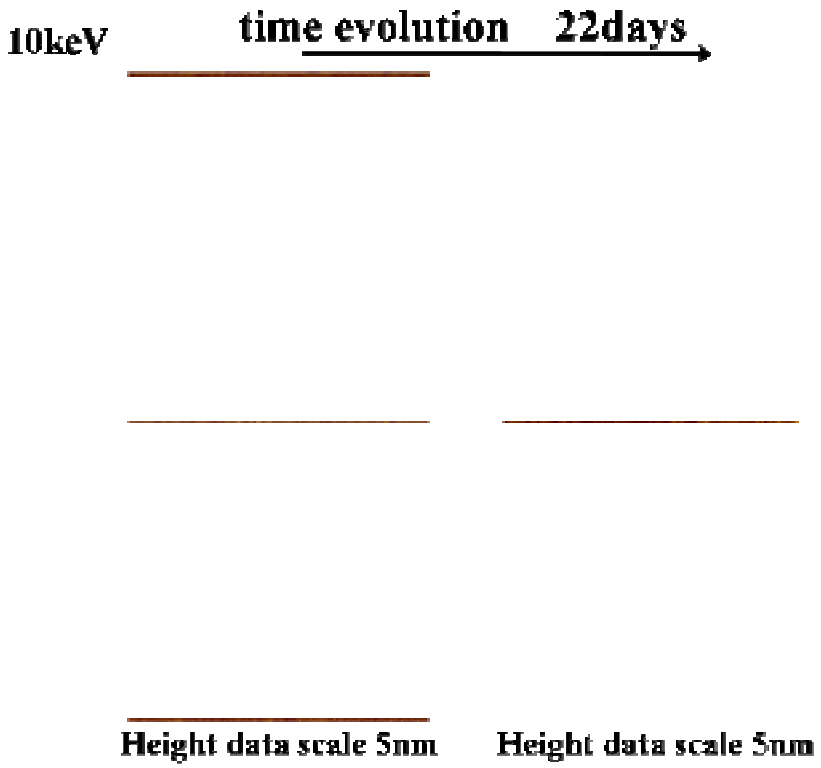

Figure 6.21 EFM images resulting from electron beam exposures of 200 nm of SiO_2 at 10 keV. The charge spread due to beam energy and scattering is clear, in the left. The extinction of EFM contrast indicates that electron beam induced charge is dissipated after some days. Topographical images corroborate the image positioning.

Paying attention to the topographical changes on patterned areas, some additional remarks can be done. The protusions are not always created after electron beam exposure (Figure 6.25, right). As a matter of fact, it seems more related with the sample, surface condition and perhaps its "processing history". As can be seen in Figure 6.22, beam energy is not the main cause and even dose has little contribution. More importantly, EFM measurements are not significantly affected for the low height of electron beam induced protusions (Figure 6.21).

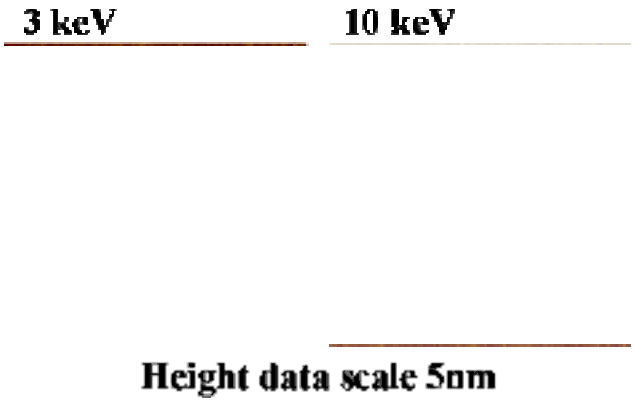

Figure 6.22 Topographical images of electron beam exposures on 200 nm of SiO_2 at two different beam energies show similar low height effect for both and almost constant signal with exposure dose.

The evaluation of charge distribution after exposure on the oxidised surfaces can be related with the mechanisms described in section 6.1. While for 3 keV charge confinement and homogeneous phase signal is obtained, the interpretation at 10 keV involves a deeper analysis. For low doses (100-1.000 μC/cm^2), the square shape of the charged area corresponds to the design. Increasing dose to 10.000 μC/cm^2 appears an additional ringed contribution of inverse sign surrounding the exposed area. Extended version is encountered for doses even higher (100.000 μC/cm^2) with twice the halo contribution (Figure 6.23).

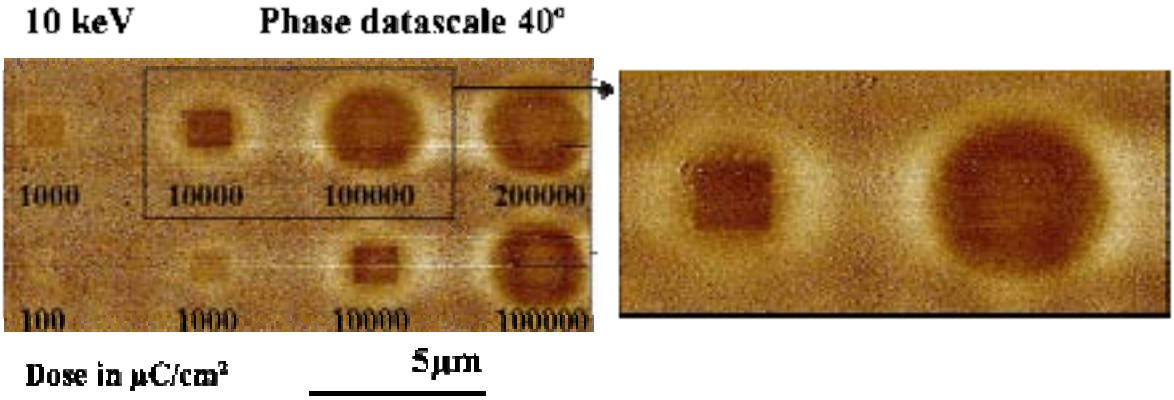

Figure 6.23 Phase imaging of electron beam exposures on 200 nm of SiO_2 at 10 keV. Significant changes are registered as a function of delivered dose.

This phenomena can be explained from the creation of charges within the oxide layer and can be illustrated with the assessment of electron trajectories simulation (see Chapter 3). In Figure 6.24, the simulation results for electron stopping positions at 3 and 10 keV in a 200 nm thick SiO_2 are represented, for different amounts of delivered electrons (i.e. exposure doses). This is not directly equivalent to the real results, but helps to visualise the range and weight of electron beam induced processes and can be complemented with the scheme described in Figure 6.2.

For 10 keV beam energy, the charge is accumulated just under the exposure area. As the electron-pair creation energy is about tens of eV, the stopping point is close to the last electron-solid interactions, in addition to the energy dissipated along the electron trajectory, that also contributes to the pair creation. Increasing the number of

electrons, the number of charges and their depth distribution increases, but also a significant amount is radially spread. Further dose increase magnifies this behaviour and also trapping in the Si/SiO_2 interface gets rellevant. Compared to 3 keV behaviour, the simulations already depict the charge spatial confinement. Low variation of phase signal is recorded with increasing dose and it can be attributed univoquely to the electric field created by oxide charging, since electrons at this incident energy do not reach the Si/SiO_2 interface and the technique intrinsic limitation to detect signal in depth.

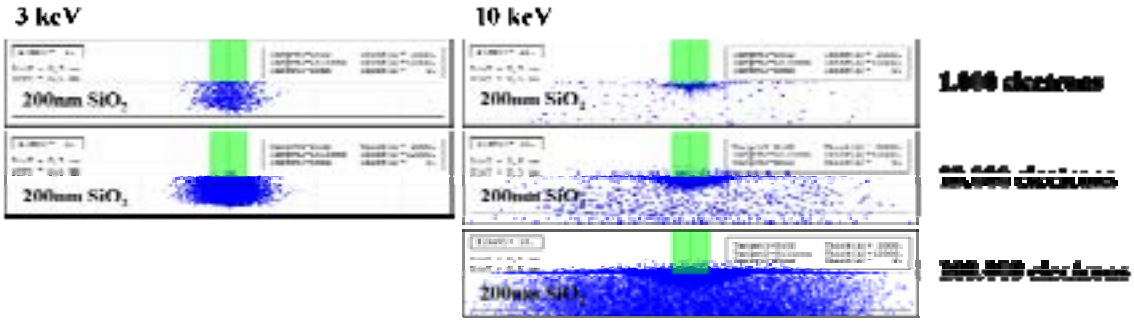

Figure 6.24 Monte Carlo simulation of electron beam exposures on 200 nm of SiO_2 at 3 and 10 keV for different electron doses. Representation of electron stopping positions in planar projection for the cylindrical symmetry process. At 3 keV, all the beam energy is dissipated through the SiO_2 layer.

On metallic surfaces (triangle shape in Figure 6.25, left), the electron exposure is uniformly distributed and no electric field distributions can be detected. Again, the shape of the electron beam induced effect for 10 keV on SiO_2 layer for a dose of 18.000 $\mu C/cm^2$ is coincident with other results (Figure 6.17, center), even if topography changes (Figure 6.25, right).

However, summarizing the results, they only inform about the existence of a electric field gradient, but not about the sign of the charge. Spatial and exposure dose resolution is obtained. Due to the low or null topography changes, direct phase imaging (without lift) can be used to avoid the loss of resolution, signal variability and low throughput inherent of EFM method (LiftMode), without significant contribution in the phase detection that alter the interpretation of the results.

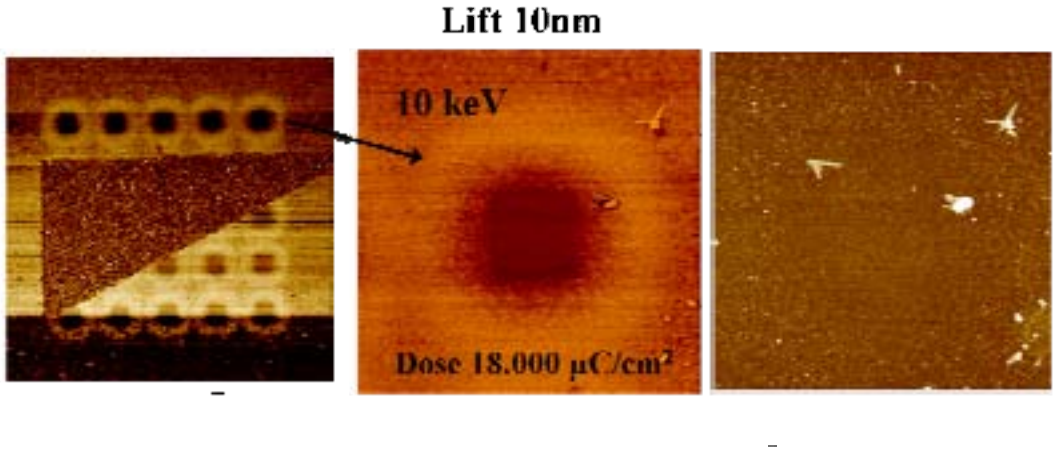

Figure 6.25 EFM images of exposure test on 200 nm of SiO_2 and thin layer of Au (triangle) at 10 keV. Doses range from 10.000 to 18.000 $\mu C/cm^2$. In this sample, topographical induced effect is insignificant (right). No charging effect is registered in the metal surface.

6.2.2 Kelvin Probe Force Microscopy

KPFM (also called Surface Potential Imaging) is able to reconstruct the electrostatic potential map of the sample surface. During the LiftMode scan, the tip and the cantilever experience a certain force where sample surface potential differs from the tip potential. The KPFM is based on nullifying this force by the application of voltage to the tip (Figure 6.26). AC electrical signal applied to the tip during the lift scan induces a periodic Coulomb force which contributes to drive the cantilever in its resonance motion. Then, feedback electronics adjusts DC voltage of the tip to compensate the potential induced by the sample. At this point, the periodic Coulomb force has a frequency that is twice the natural resonance frequency of the cantilever. The compensation DC potential signal is registered in the microscope to configure the KPFM image (i.e. surface potential mapping of the sample) (Figure 6.26).

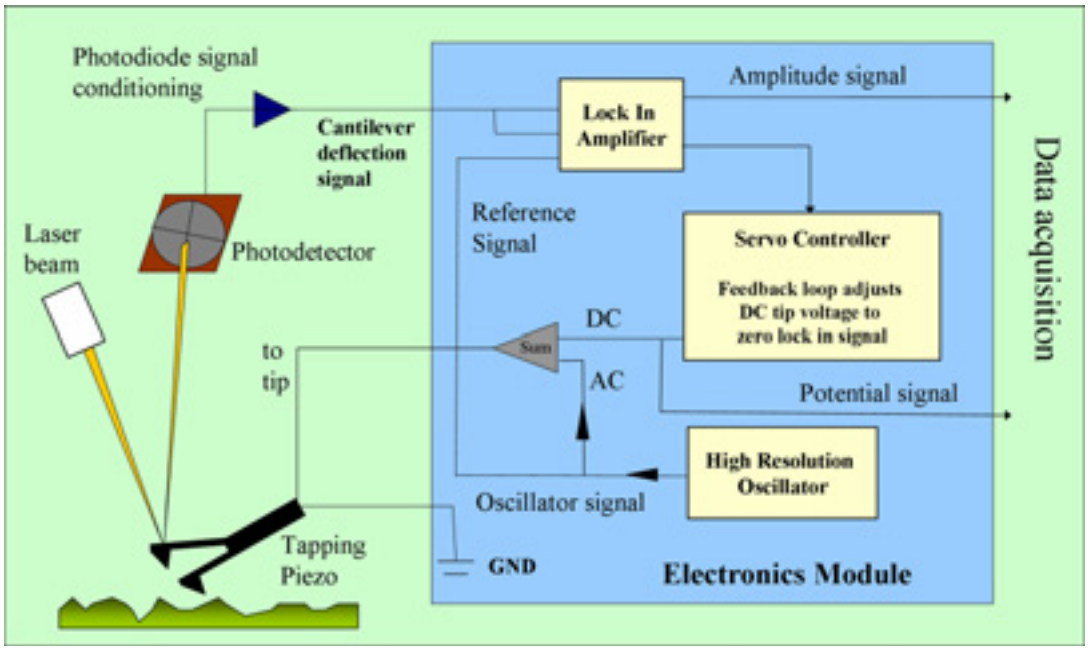

Figure 6.26. Scheme of the microscope operation during KPFM, from (19).

The principle of KPFM is more easily explained from the mathematical expressions that describe the system interactions during each scanned point. During LiftMode pass, the cantilever is excited electrostatically. Therefore, the potential on the tip is,

$$V_{tip} = V_{dc} + V_{ac} \sin \omega t \tag{6.4}$$

In the presence of a potential on the surface (ϕ), the force that is applied to the tip would be,

$$F_{cap} = \frac{1}{2}\left(V_{tip} - \phi(x)\right)^2 \left(\frac{dC}{dz}\right) \tag{6.5}$$

(i.e. the tip force has components at ω and 2ω). Using lock-in amplifier, only the oscilation at ω is detected.

$$F_{cap}(\omega) = \frac{dC}{dz}\left(V_{dc} - \phi(x)\right)V_{ac}\sin\omega t \qquad (6.6)$$

Then, the feedback loop acts on V_{dc} to compensate surface potential value and, in consequence, the force is null, $F_{cap}(\omega) = 0$. The V_{dc} is the acquired signal that enables to reconstruct surface potential.

The aim to establish this characterization technique is to complement EFM measurements in order to determine more accurately the nature, effect and mechanisms involved in the electron beam exposure. Thus, deeper comprehension of experimental results on devices could be assessed.

Again, commercial AFM conductive tips are used to characterise exposure processes similar to the EFM. As an example, the results of the exposure in the oxidised samples at 10 keV beam energy are shown in Figure 6.27. Surface potential imaging confirms all the EFM statements in terms of beam energy and dose. At low doses the effect of the exposure is restricted to the patterned area, whereas increasing delivered dose leads to the charge radial spread within the surface. In addition, it has a high spatial resolution both quantifying the potential and revealing the difference between direct or indirect induced effect. At high electron doses, e.g. 100.000 μC/cm^2, saturation is reached in the exposure area and the halo of charge appears as punctual detected signal, which is related with the discrete nature of incident electrons. Comparison between the results of KPFM and EFM can be established. In terms of resolution, what appeared as a continuos gradient of electric field in EFM measurements, is detected in KPFM as discrete signal and it is consistent with the simulations (Figure 6.27). Besides this, additional punctual features arise, which can be attributed to the effect of exposure in preexisting defects of the oxide layer. However, it is difficult to estimate further explanations from the data, as could be the sign of the charge or the depth range of detection.

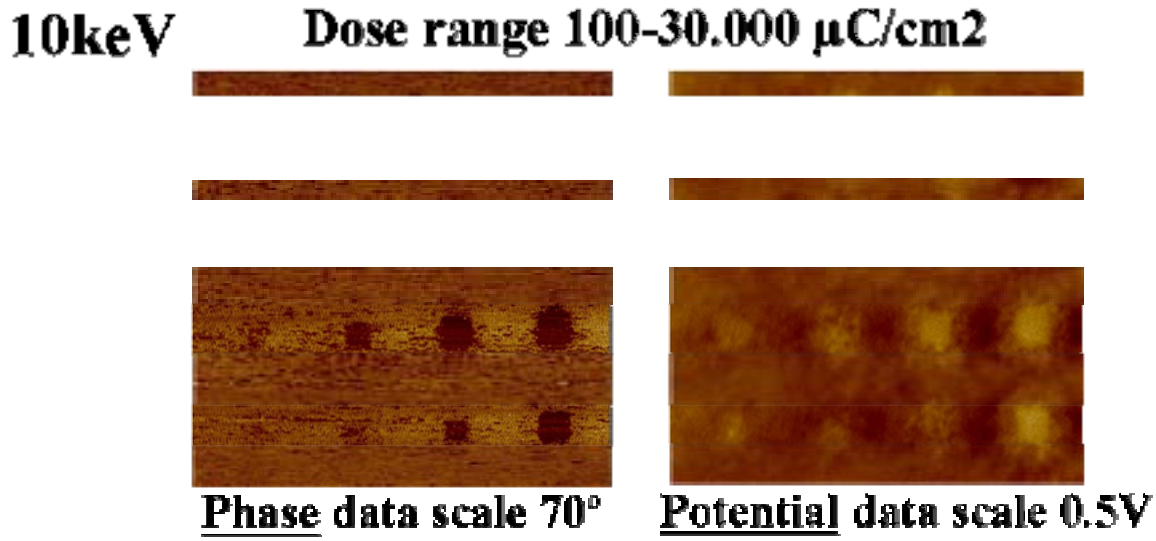

Figure 6.27 EFM and KPFM images of an electron beam exposure on 200 nm of SiO_2 at 10 keV. Doses range from 100 to 30.000 μC/cm^2 and lift height is 10 nm.

The change of surface potential as a function of beam energy is also notorious. Charge confinement and uniformity is confirmed for the low voltage electron irradiation

(3 keV), whereas at 10 keV the electron effect is also distributed surrounding the exposed area (Figure 6.28). Again, it is difficult to univoquely interprete the results. At 3 keV is reasonable to think that lower potential is only attributed to the positive charge created in the oxide layer. However, for 10 keV, the balance of created oxide charge, interface traps and contribution of the electron dose that reaches Si underneath difficults an exact determination and a dedicated study should be done.

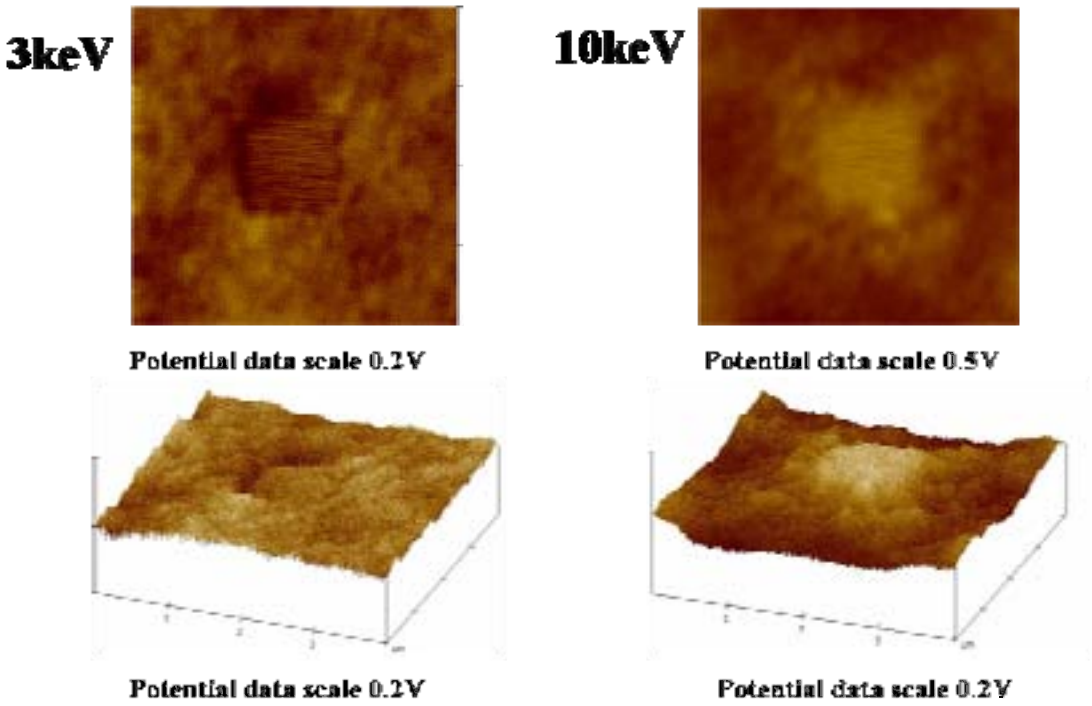

Figure 6.28 KPFM zoomed images of exposure beam exposures at 3 and 10 keV for exposure dose 10.000 μC/cm^2. Lift height is 10 nm. Charge confinement is seen for 3 keV, whereas backscattering effect is present for 10 keV. Signal contrast is reversed.

The time evolution monitoring is also determined for the KPFM measurements. Coincidental with EFM images (Figure 6.21), the effect of electron beam exposure spontaneously dissapears after some days (correct positioning is again assisted by topographic reference) (Figure 6.29). As can be seen in the left side image, the relative potential of the exposed areas is not easily related with the electron beam effect and the creation of charges of determined sign, since equivalent exposures show slight variations. In addition, perhaps the deffects on oxide layer are the cause of singularities that appear in the surface potential image just after electron beam exposure. This reinforces the imaging capability of the KPFM technique.

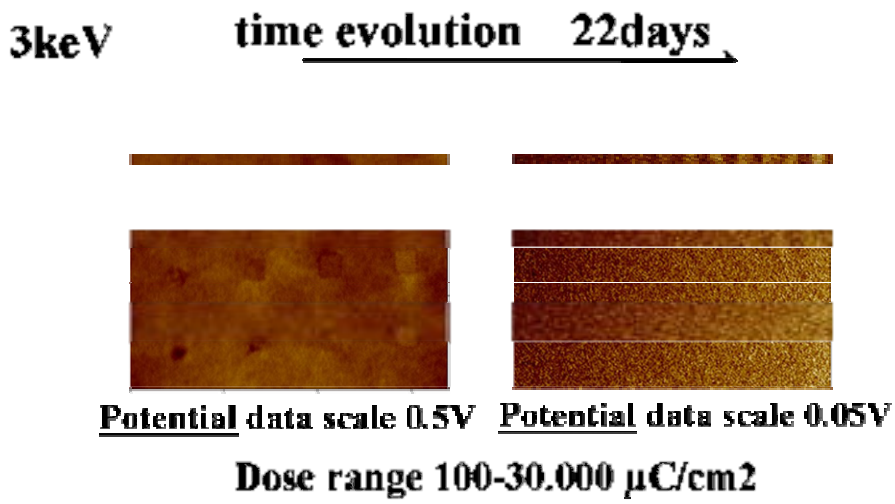

Figure 6.29 KPFM images of electron beam irradiation at 3 keV on 200 nm of SiO_2. (Left) Image taken just after exposure and (right) 22 days after. Dissipation of induced charge is clearly seen, topographic signal is used to guarantee correct positioning.

6.3 Electron Beam exposure on CNTFETs

The outstanding properties of CNTs make them the ideal platform for the next generation of electronic devices and, also, for the fundamental study of electronic transport and mechanical characteristics. The difficulties to integrate them massively as part of devices or systems cause that patterning techniques, as it is direct writing EBL, are preferred to define discrete devices. In addition, high resolution measurement systems and specially adapted characterization techniques are needed to determine their operation.

In the previous sections and chapters, a variety of electron beam induced effects on different configurations, devices and systems are presented. Now, it seems interesting to evaluate the effect of electron beam on CNTs, used during the device fabrication (Chapter 4), in order to discard any induced alteration, for example during fabrication.

This is reinforced with results found in the literature. It is reported the degradation of CNTFET performance at high electron beam energies, due to the induction of defects in the carbon structure (23), or the change in Raman spectra of electron beam irradiated CNTs (24). Many of them are working either with MWCNTs (25), high number of tubes or, very high energies and ionic beams (26). The use of low electron beam energies to expose SWCNTs in FET configuration is presented next.

6.3.1 Electrical characterization

The first irradiation experiments are amde on back gated CNTFETs with deposited CNTs (see section 5.2.1 for the details of device fabrication). The electron beam induced effect is monitored by the acquisition of the electrical response from the devices. Before the exposure, the electrical characteristics are always registered (named as Ref. in the figures). The electrical measurements are systematically done, as

described in chapter 5. In particular, in order to avoid eventual ambiguities caused by hysteresis (Vg from +5 V to -5 V).

The exposure methodology is based on the design of the irradiated area as a separate layer in the GDSII design file that has been used to fabricate the device (Figure 6.30, center). Thus, the irradiation is controlled by means of the lithography program, using the blind alignment via the fabrication reference marks and the determination of delivered dose with the exposure parameters. This strategy avoids using extra dose due to SEM positioning or uncertainties in delivered charge.

The first experiment is performed on the whole transistor area (7 x 6 μm^2) at a beam energy of 10 keV (fabrication beam energy) and a dose of 10.000 $\mu C/cm^2$ (Figure 6.30, left, white rectangle). The electrical characteristics after the exposure reveal a decrease of the on current, degradation of the transconductance and displacement of the threshold voltage. However, this is a transient effect and the CNTFET recovers after several days (Figure 6.30, right). Due to this, series of exposures under different conditions on the same device could be performed to study and compare the effect of beam energy and dose dependence. If not mentioned, dose per unit area is kept constant for all the experiments (10.000 $\mu C/cm^2$), i.e. total delivered charge depends on the size of the designed area.

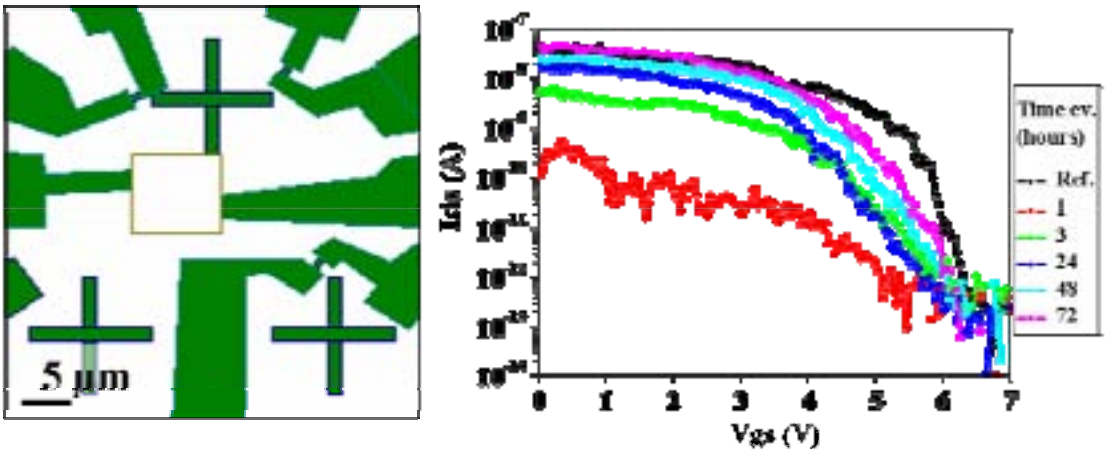

Figure 6.30 (Left) Design of the exposure area for the irradiation of the whole FET. (Right) Time evolution of the electrical characteristics for the exposure of the whole FET at 10 keV. Dose is 10.000 $\mu C/cm^2$.

Additional tests at 10 keV are performed to determine in which part of the CNTFET structure the exposure causes a major effect. The trials include a line of 0.5 µm in width perpendicular to the CNT channel, the metallic part of the drain contact or two punctual exposures in the CNT-metal contact interface (200 x 100 nm^2). The electrical characteristics and their time evolution are presented in Figure 6.31. The results are not absolutely conclusive since delivered dose is not equivalent, but more importantly due to the large interaction volume in the substrate (SiO_2 and Si) at this beam energy (10 keV). However, the general tendency is that the amount of delivered charge increases the device degradation effect and the main alteration is registered when the exposure is placed on the CNT.

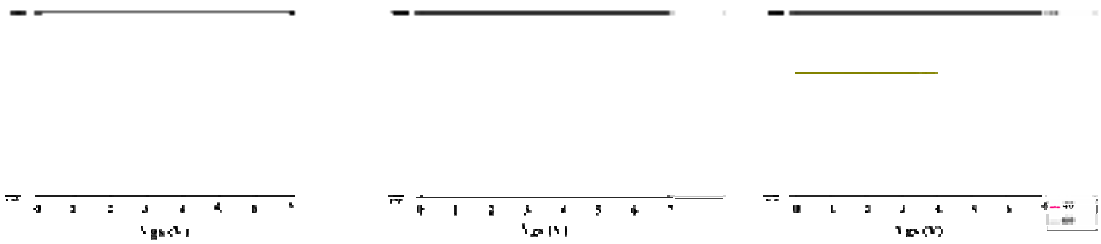

Figure 6.31 Evaluation of the exposure on the different parts of the device at 10 keV. The strongest effect is registered when the CNT is directly irradiated.

Based on the Monte Carlo simulations of electron trajectories (see details in Chapter 3), it is found that an incident 3 keV beam energy is enough to confine the electron penetration range on the metal layer or the SiO_2 below 100 nm. In consequence, the rest of the experiments are operated at this beam energy to ensure that the delivery of dose is nearly limited only to the desired locations.

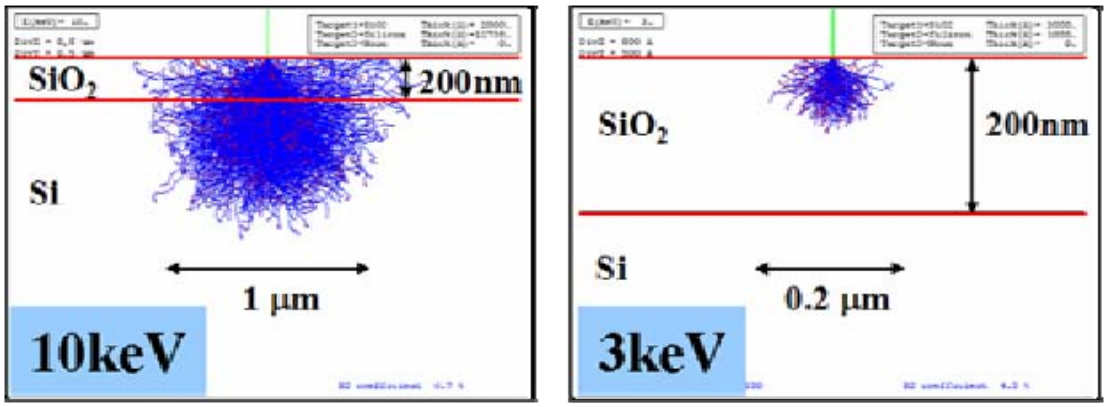

Figure 6.32 Planar projection of the electron trajectories using Monte Carlo simulations. For the present experimental configuration, 200 nm of SiO_2 on Si (right) and thin Au layer (35 nm, not shown), an electron beam of 3 keV is stopped at about 100 nm in depth on SiO_2.

Previous trials on different parts of the CNTFET structure are repeated and the results demonstrate the avoidance of crossed contributions due to the charge scattering. For the contact metal exposure, no effect on device performance is observed, whereas CNT line exposure reveals the most significant damage: equivalent to the irradiation of the whole FET area. The punctual exposure at the metal-CNT interface shows a displacement of the threshold voltage to negative values and decrease in transconductance, whereas punctual exposure in the CNT channel center, with the same charge, appears as a decrease in the on current (Figure 6.33). However, these punctual exposures are more susceptible to the alignment precision and it is not convenient to infer deeper explanations from these results.

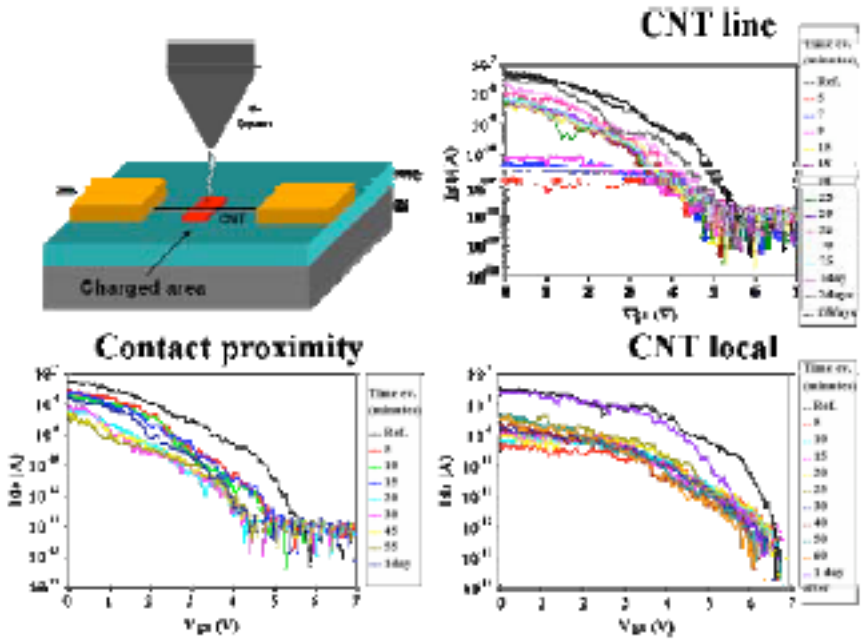

Figure 6.33 Schematic drawing of the local exposure experiments by electron beam on the CNT devices and experimental results for the determination of the device portion that is more sensitive to the electron exposure. At 3 keV, charge is locally absorbed both laterally and in depth.

The results above are derived from the exposure of CNTs sinthesized by laser ablation, this is, using deposited tubes for contacting. CVD grown CNTs are also used to test the effect of extended and local irradiation (see section 5.2.2 for the details of device fabrication). Analogous behaviour is found. Again, the degradation of the transistor operation in terms of on current, transconductance and change in threshold voltage is obtained (Figure 6.34). The total charge delivery is about 10 times larger for the left side case (whole FET) than for the one in the right side (line), which has a drastic effect on the electrical characteristics of the device, but recovering after several days occurs.

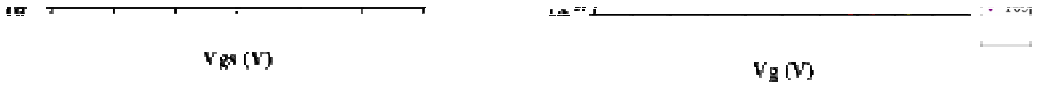

Figure 6.34 Effect of 3 keV exposure on a CVD grown CNTFET. All curves correspond to V_{ds}=260 mV.
(Left) Irradiation on the whole transistor area causes higher device degradation.
(Right) Line exposure causes lower effect, as it delivers less dose.

Analysing the time evolution of different exposures, the threshold voltage shift is higher and takes slightly longer to completely recover for 10 keV as compared to the same exposure at 3 keV (Figure 6.35).

Figure 6.35 Time evolution of the on current after different exposures. Higher beam energy and increased amount of charge induce larger damage and slower device recovering.

6.3.2 Electrical Force Microscopy and Kelvin Probe Force Microscopy on exposed CNTFET devices

As presented in previous section 6.2, EFM allows to monitor how the surface is charged or modified after local electron beam exposure. Expressed in terms of the gradient of electric field in the surface, the effect induced by the electron irradiation in CNTFETs in the electrical characteristics can be complemented with EFM. Images provide information about charge trapping extension and evolution with time. In addition, these measurements verify the lateral resolution and positioning accuracy of the electron beam exposure (Figure 6.36).

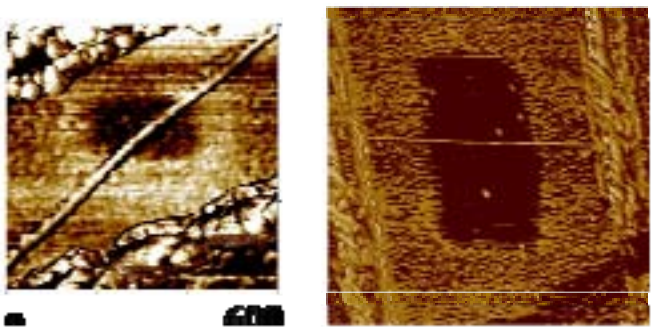

Figure 6.36 Two examples of EFM imaged in contacted CNTs after electron beam exposure. The beam energy is 3 keV and the exposure dose is 10.000 μC/cm^2.
Charge confinement and precise EBL alignment are clearly seen. Metal contacts are not polarised.

Two examples of electron beam exposures at 3 keV on contacted CNTs are shown in Figure 6.36, for local and line exposure (left and right, respectively). Relating the effect of increasing beam energy on the induced damage, EFM is consistent with the electrical characterization results in previous section. Exposure at 10 keV offers more signal contrast and remains longer, the same behaviour observed in the device operation. This is possibly caused by some additional effects with respect to 3 keV beam energy exposure.

The creation of trapped charge in the SiO_2 is observed, but no significant effect on the CNT is registered. However, device electrical characteristics indicate that the main contribution of electron damage occurs in the CNT itself, rather than in the contacts. It has to be taken into account that EFM image is not acquired immediately after exposure and that contacts of the devices are on air (i.e. not biased) while imaged.

To better understand the effect of the local exposure, KPFM is used. This AFM-based technique provides surface potential description of the device under exposure. The CNT is biased by only one electrode (Drain) and the gate (Figure 6.37). A commercial Si tip coated with Pt is used. Gate bias is applied via the AFM chuck. Images are taken before and after e-beam irradiation at variable polarizations of gate and metal contact.

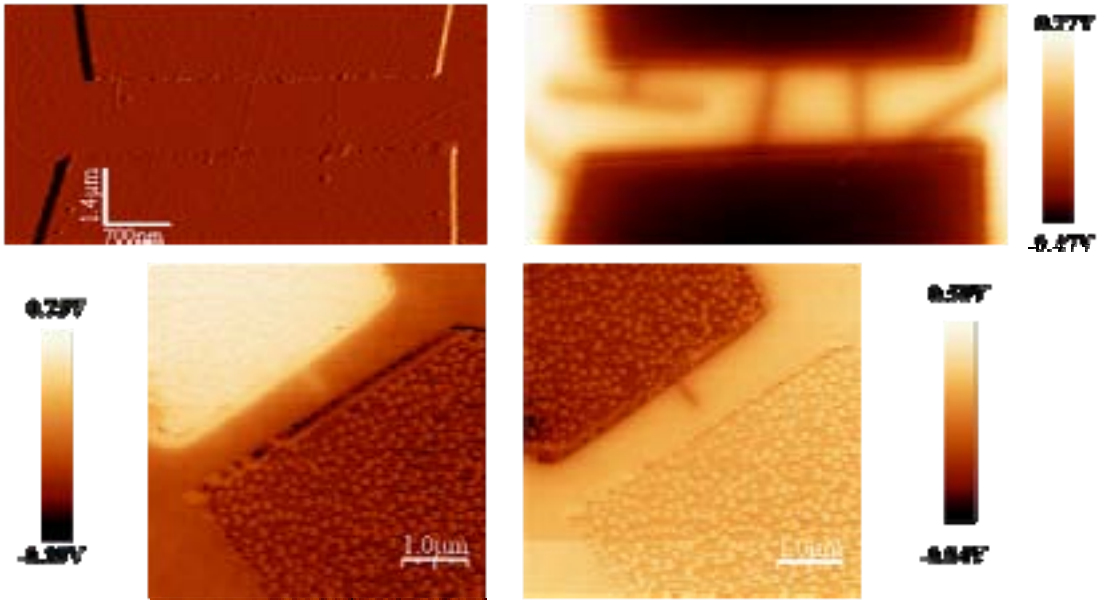

Figure 6.37 Examples of KPFM images of positive or negative biased CNTFETs. This technique allows to visualize actually contacted CNTs (top) or even to determine the exact point where the CNT transport ceases (bottom).

Figure 6.38 shows a KPFM image of a CNT FET after exposing the channel. The electron beam exposed area appears with a lower potential (Figure 6.39). The profile extracted from this image reveals that the decrease of the surface potential is of the order of 0.2V. However, in this configuration, the effect of the electrodes separated by a short gap of ~ 1 μm reduces surface potential contrast due to the signal contribution from the metal electrodes. The force experienced not only at the tip, but in all the cantilever is stronger due to biased metal contacts (27). In consequence, signal constrast is lower, as compared with bare oxidised surface (see images in section 6.2.2).

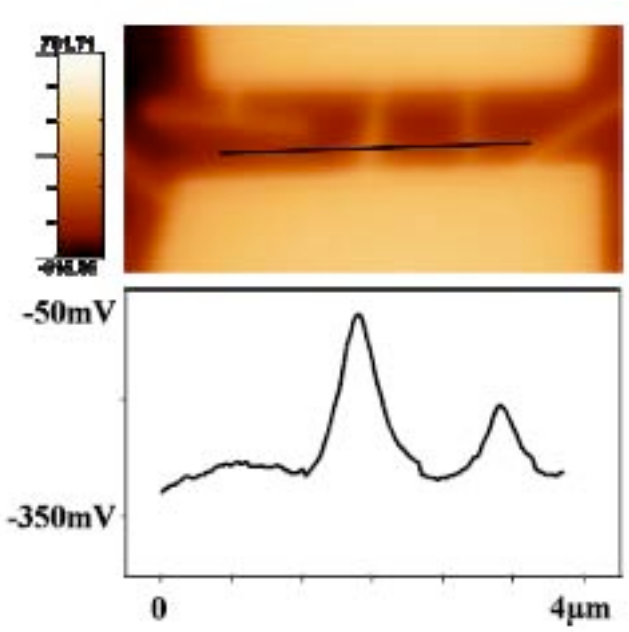

Figure 6.38 KPFM image after performing an electron beam exposure of 10.000 µC/cm^2 on the CNT placed in the FET channel, V_d=2 V, and its representative profile.

To achieve a better understanding we have realized irradiations using one-side contacted CNTs (Figure 6.39). In addition, the exposure dose is increased to 100.000 µC/cm^2 in order to enhance signal contrast. The charging of the oxide layer is again clearly seen as a confined region of decreased potential. The most relevant feature arises from the unexpected potential increase measured on the CNT, exactly where it is exposed (see profiles in Figure 6.39). This behaviour is found systematically.

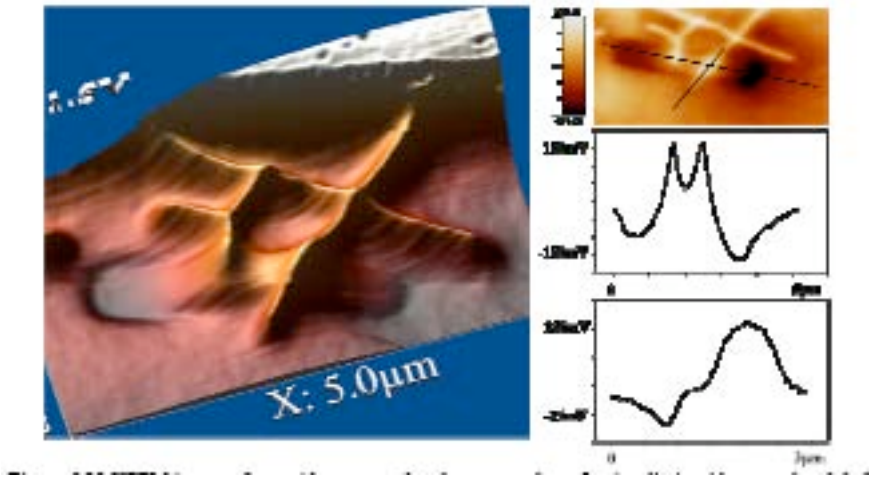

Figure 6.39 KPFM image of one-side contacted carbon nanotubes after irradiation (depressed and darker area). Nanotubes are biased at +2 V. Right, potential profiles to observe the potential spatial distribution across the irradiation area (up) and along the CNT (down). Exposure dose is 100.000 µC/cm^2.

The effect is enhanced when the voltage difference between nanotube and substrate is larger. As it is shown in Figure 6.40, the change of imaged potential on the different areas is determined taking the non exposed oxide as the reference potential. Irradiated SiO_2 shifts to negative values, whereas exposed CNT area presents a certain tendency to behave as the metal electrode. This behaviour indicates that the effect of the charge in the oxide below the CNT may change the local electrical properties of the nanotube itself.

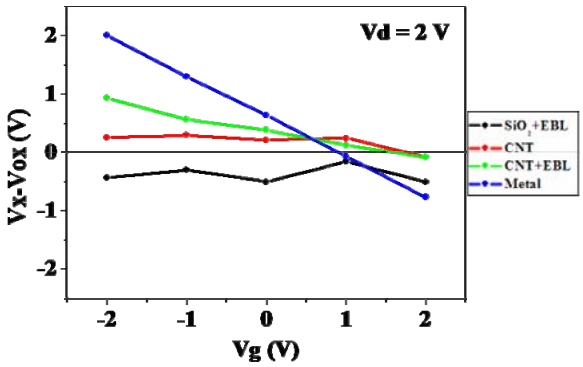

Figure 6.40 Surface potential values obtained in the electrode, CNT, exposed area of the CNT and exposed oxide area. Non-exposed oxide is used as the potential reference, for different biasing conditions on Vgate and Vdrain.

6.3.3 Electrostatic simulations

In order to explain this behaviour, 3D finite elements simulations (28) of the device including electronic charging and the presence of a polarized AFM tip are developed in collaboration with the group of Dr. David Jiménez from the department of Enginyeria Electrònica at the Escola Tècnica Superior d'Enginyeria-UAB. This methodology enables to compare the modelled electrostatic potential of the device with the registered surface potential obtained by KPFM. An overview of the simulation flow is showed in Figure 6.41. Model includes biased contact and gate, locally delivered charge and polarized AFM tip.

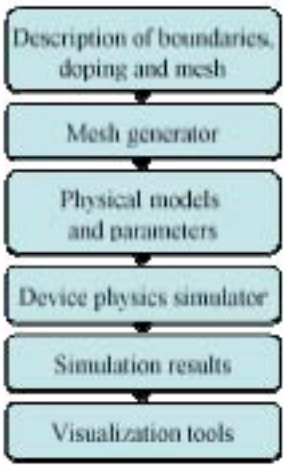

Figure 6.41 Processing flow for the ISE TCAD simulations.

An example of the results of the simulated electric field are presented in Figure 6.42. On the left, it is represented the potential distribution of the whole system for an undoped or slightly doped silicon layer of (1x0.5x0.5) μm^3 dimensions, a 0.25 μm thick SiO_2 layer, a gold electrode, a thin copper cylinder playing the role of the CNT of 1.5 nm in diameter and a semi spherical platinum electrode simulating a 30 nm radius AFM tip. The effect of the local exposure is simulated by a confined charged region in the oxide surface of 10^{16} electrons. On the right side, it can be seen the results of an extracted profile of the surface potential as a function of the position at the oxide surface, perpendicular to the nanotube and at a distance of few microns from the electrode.

There is much information that can be extracted from the simulations. For example, the decrease of the potential on the surface due to the delivered electronic charge is clearly reproduced. The most remarkable effect is that the AFM tip potential produces a large depression of the surface potential below the tip. In this sense, interpretation of the KPFM becomes extremely complex: KPFM is operated in close loop, so that the tip potential is set to a value that minimizes the electrostatic energy. In the present configurations, we have an extremely inhomogeneous surface where the nanotube is located (the nanotube is almost a potential singularity), and the tip potential determines the potential of the oxide surface. Under these conditions, the effect shown in figure 6.38 can be understood as the competing effects of electrical charge in the oxide, tip potential and CNT potential, which induces a rather complex an unexpected electrical field distribution. Among other implications, it confirms the model already depicted from the electrical characteristics (section 6.3.1). The changes of conductance characteristics of the CNT after electron beam irradiation are caused by the electron beam-induced electrical field distribution.

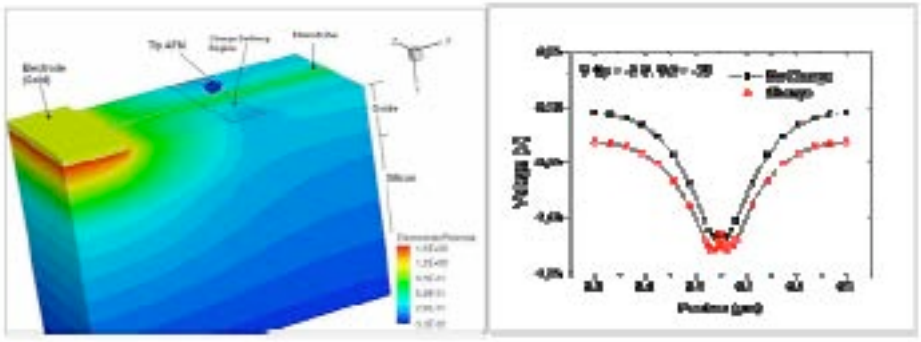

Figure 6.42 (Left) Simulated electrostatic potential map of a simplified system formed by a thin Cu cylinder contacted with a Au electrode, and a semi spherical Pt electrode. (Right) Surface potential along z-axis below the tip and perpendicular to the CNT, showing the effects of the trapped charge in the oxide.

6.3.4 Comparison to MOS results and theoretical analysis

The effect induced by electron radiation on MOS devices is explained from the modification of the charge distribution in their structural layers. As presented in section 6.1, the creation of positive charges in the insulator and the Si/SiO_2 interface trapped

charge are determinant for the device performance. Applied to the MOSFETs, induced oxide charge modifies the relative energy levels and interface traps difficult the channel conduction acting as scattering centers. In consequence, MOSFET suffers a shift in the threshold voltage and decrease in transconductance and on current, respectively. The experiments reported in 6.1.1 corroborate these assumptions for more complex systems.

The comparison of MOSFET and CNTFET is unavoidable. Their structures are configured by the same materials, except for the conduction channel, and the device operation is based on different mechanisms. However, they can experience similar degradation under electron beam exposure (Figure 6.43).

In the case of CNTFETs, Si/SiO_2 interface traps cannot directly affect the channel conduction (CNT) since they are not in close contact. The elucidation of the electron beam induced perturbation can be solved with the fundamental analysis of the unique structure of the CNT. Theoretical calculations of the effect of external electric fields on CNT conduction can be consulted in (29, 30). Theoretical development of the effect of transverse electric fields on CNTs predict both electrical characteristics and KPFM results.

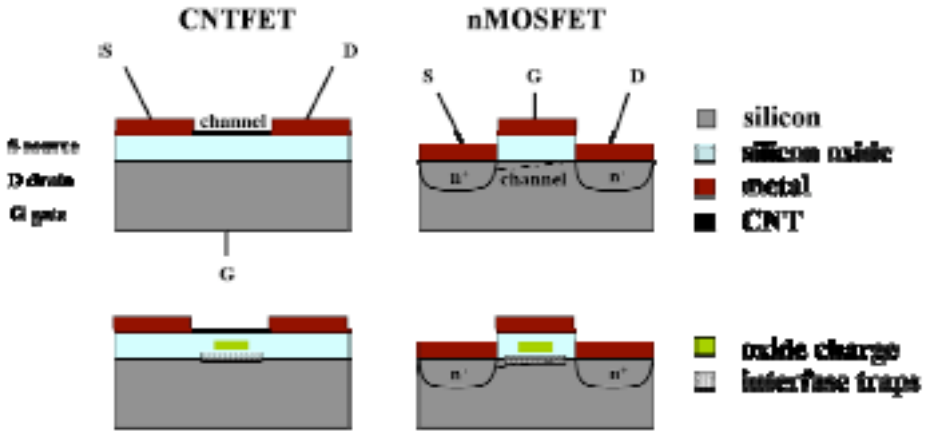

Figure 6.43 Comparative scheme of a CNTFET and a nMOSFET structure.
The mechanism induced by the electron beam irradiation causes oxide charge and interface traps, that affect the FET performance characteristics.

The existence of strong electric field inhomogeneties or anisotropic potentials breaks the symmetry of the CNT. In consequence, the band structure is altered widening the gap in the density of states near the Fermi level. The exposure-induced oxide charge defines the local electric field that establishes a barrier that reflects electrons. As CNT has 1D conduction, this singularity creates backscattering in the transmission channel and perturbs FET conduction. In addition, an extended and homogeneous perpendicular electric field is considered to induce tube transition from semiconductor to metallic behaviour (31). This explains the local unexpected rise of KPFM signal since, in addition to the intrinsic singularity of the CNT, the effect of applied field for surface potential measurements (27) is reinforced with the local potential induced by the electron beam exposure. This justification not only matches with the results presented above, but also are in agreement with (31).

Some similarities can be encountered with the work of Zdrojek et al (32,33), where comparable results are established by charge injection on CNTs and immediate

EFM characterization. Polarized CNTs appear with a change of signal contrast restricted to the "active" area of the nanotube (Figure 6.44, top). In addition, discharging process is also monitored as a function of time and at specific locations of the CNT lenght (Figure 6.44, top right), and the effect on the acquired signal of potentials applied to the tip is presented.

Compared to the results presented in previous sections, the local irradiation of contacted tubes appears as spatially limited charge area and increased signal in KPFM (white arrows, Figure 6.44, bottom left). Discharge through the insulating layer is possible, but, in this case the obtained results have to be attributed to positive charge since time scale is different (lasting time for imaging is now longer than electron dissipation time on the oxide layer) (Figure 6.44, bottom). Besides this, signal contrast is inverse, what additionally agrees with the degradation of device characteristics due to the presence of locally induced electric fields.

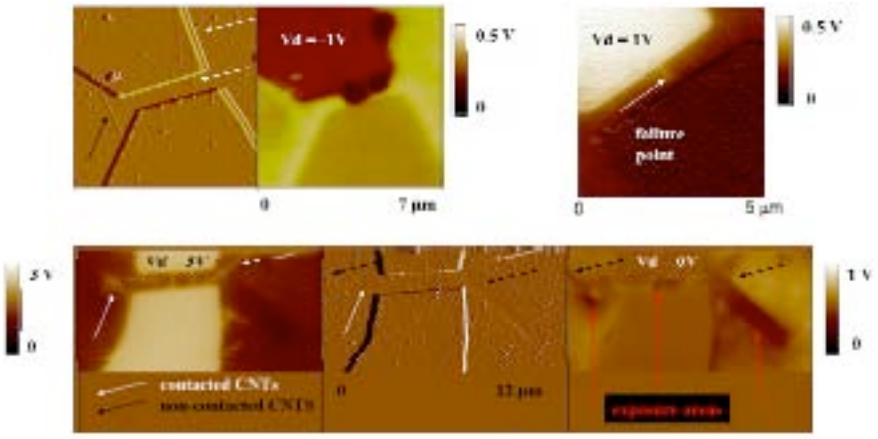

Figure 6.44 Examples of KPFM images on devices. Vd is the metal contact polarization. (Top) Contacted tubes account for the charge conduction when biased. In particular, on the right side, a device that does not operate anymore shows the stopping point of CNT conduction, marked by the white arrow. (Bottom) Electron irradiation implies an increase of signal due to additional charge/electric field on contacted CNTs. Non contacted tubes are polarized by trapped positive charge. Central image corresponds to amplitude signal.

6.3.5 Design of ion beam induced experiments on CNTFETs

The results shown in precent sections highlight the necessity to take into account the consequences of the use of SEM and EBL. Results are aimed to contribute to understand experimental observations or to motivate theoretical studies to explain the electronic transport of CNTs. Many other experiments and measurement systems may be interesting. AFM-based current measurements could evaluate the local change of charge transport characteristics due to electron beam or electron beam effect on FETs.

Future work is oriented to evaluate the effect of other charged particles in the CNT based devices. In particular, the interaction of carbon related materials will be studied by the bombardment of CNTFETs with an ion source of C_{60}^- (fullerene), in collaboration with Pr. Eli Kolodney from Technion University.

The design of the experiment is oriented to electrically characterize on line the effect of local C_{60}^- exposure on CNTFETs (Figure 6.45). In order to do it, several issues may be considered.

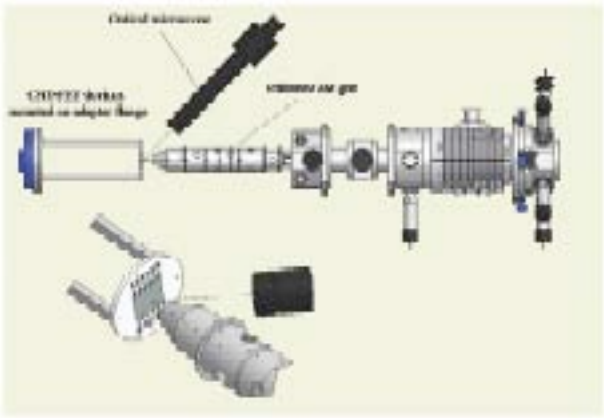

Figure 6.45 The experimental set-up for the CNTFET exposure experiment.
The C_{60}^- bombardment is at normal incidence for maximum effect. Performance of the nano-device is measured on line as a function of exposure conditions (impact energy, current density, total dose).

The C_{60}^- ion source has not beam direct writing capabilities, therefore selective exposure may be implemented by masking. For this a CNT compatible material is used. Taking advantage of the passivation tests of CNTFETs with PMMA (chapter 5), the integrity of the resist under C_{60}^- has also been tested. As a result, CNTFET samples are covered with a standard layer (~100 nm) of 950k MW PMMA. Selective openings are defined with EBL at low beam energy (3 keV) (Figure 5.42, left).

Electrical measurements require dedicated connexions. CNTFETs sample is sticked and wire bonded to a PCB (Figure 6.46, center and right). The design of the PCB matches with the microscopical size of the devices, in order to reduce wire length. The electrical connections between the PCB board and the exterior of the chamber are realized with dedicated cables and flanges. Vacuum–side UHV compatible multipin (25) electrical feedthroughs are used. The cable assemblies are with PEEK connectors and Kapton insulated ribbon cables. These connections serve to polarize and transfer the signal to an standard semiconductor analizer for the on line device performance monitoring.

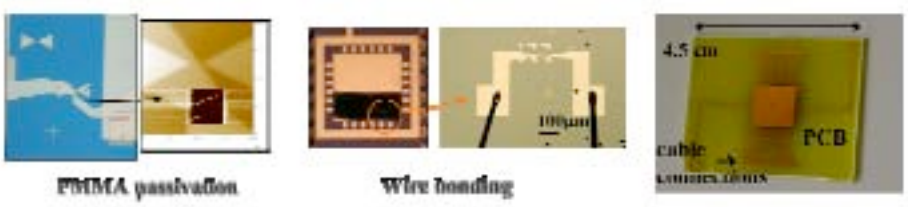

Figure 6.46 Detailed images of the set-up for the selective exposure of CNTFETs to C_{60} ions.
(Left) Opening in a PMMA layer. (Center) CNTFET connected to the PCB by wire bonding.
(Right) PCB designed to connect cables to the flange.

Several mechanisms are already predicted that may occur for the different beam energies in which the ion source can be operated or as a function of dose (Figure 6.47). In consequence, AFM will be used to assess the characterization of morphological changes or charging effects with the experience of previous experiments. In particular, it is possible that bombardment causes changes in the properties and structure of the insulator, affects the CNT structure or even modifies the device configuration. For example, those effects may change the performance mechanism of the CNTFET, the transport properties of the CNT, etc or induce repairing or damage in the CNT structure.

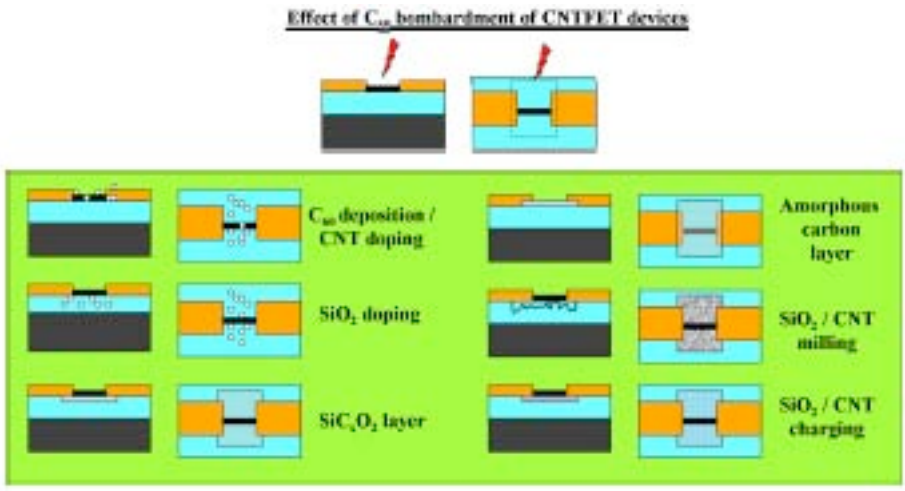

Figure 6.47 Possible mechanisms induced by C_{60} ion bombardment on CNTFET structure. Experimental variables are beam energy and exposure dose.

Summarizing the contents of this chapter, the evaluation of the effect of electron beam on devices is described. First, the damage of CMOS circuits by both electron and ion beams is determined for different exposure conditions. A novel concept of NEMS using electron beam induced motion is also presented. An exhaustive study of the electron irradiation of CNTFETs comprises the second part of the section. Advanced AFM-based characterization and FE simulations assist the results of FET electrical characteristics to better understand the mechanism that causes electron beam exposure. The results help to establish the compatibility of electron beam-based fabrication and imaging, but also provide more fundamental information about the induced processes and the role and operation of the different device elements.

References

(1) T.P. Ma and P.V. Dressendorfer
Ionizing radiation effects in MOS devices and circuits
Ed. John Wiley & Sons, ISBN 047184893X (1989)

(2) L. L. Kazmerski, N. A. Burnham, A. B. Swartzlander, A. J. Nelson, and S. E. Asher
Electron-Beam Effects in the Analysis of Compound Semiconductors and Devices
Journal of Vacuum Science & Technology a-Vacuum Surfaces and Films **5** (5), 2814-2818 (1987)

(3) E. K. Hieke and J. Tihanyi
Electron-Beam Induced Current in Biased Mos-Transistors
Solid-State Electronics **22** (2), 221-& (1979)

(4) M. Fischer, H. D. Wanzenboeck, J. Gottsbachner, S. Muller, W. Brezna, M. Schramboeck, and E. Bertagnolli
Direct-write deposition with a focused electron beam
Microelectronic Engineering **83** (4-9), 784-787 (2006)

(5) M. Isaacson
Electron-Beam Induced Damage of Organic-Solids - Implications for Analytical Electron-Microscopy
Ultramicroscopy **4** (2), 193-199 (1979)

(6) T. Bret, N. Utke, P. Hoffmann, M. Abourida, and P. Doppelt
Electron range effects in focused electron beam induced deposition of 3D nanostructures
Microelectronic Engineering **83** (4-9), 1482-1486 (2006)

(7) R. C. Alig and S. Bloom
Electron-Hole-Pair Creation Energies in Semiconductors
Physical Review Letters **35** (22), 1522 (1975)

(8) A. Holmes-Siedle and L. Adams
Handbook of radiation effects
Oxford university Press (2nd Edition), ISBN

(9) B. Das, S. Subramaniam, and M. R. Melloch
Effects of Electron-Beam-Induced Damage on Leakage Currents in Back-Gated Gaas/Algaas Devices
Semiconductor Science and Technology **8** (7), 1347-1351 (1993)

(10) Z. J. Davis, G. Abadal, B. Helbo, O. Hansen, F. Campabadal, F. Perez-Murano, J. Esteve, E. Figueras, J. Verd, N. Barniol, and A. Boisen
Monolithic integration of mass sensing nano-cantilevers with CMOS circuitry

Sensors and Actuators a-Physical **105** (3), 311-319 (2003)

(11) F. Campabadal, S. Ghatnekar-Nilsson, G. Rius, C. Fleta, J.M. Rafí, E. Figueras, and J. Esteve
CMOS degradation effects due to electron beam lithography in smart NEMS fabrication
Proceedings of SPIE **5836**, 667-674 (2005)

(12) S. Ghatnekar-Nilsson, E. Forsen, G. Abadal, J. Verd, F. Campabadal, F. Perez-Murano, J. Esteve, N. Barniol, A. Boisen, and L. Montelius
Resonators with integrated CMOS circuitry for mass sensing applications, fabricated by electron beam lithography
Nanotechnology **16** (1), 98-102 (2005)

(13) J. Arcamone, G. Rius, G. Abadal, J. Teva, N. Barniol, and F. Perez-Murano
Micro/nanomechanical resonators for distributed mass sensing with capacitive detection
Microelectronic Engineering **83** (4-9), 1216-1220 (2006)

(14) L. A. Gianuzzi and F.A. Stevie
Introduction to Focused Ion Beams
Ed. Springer ISBN 0387231161 (2004)

(15) S. Timoshenko and J Goodier
Theory of Elasticity
NY, Mc Graw Hill (1970)

(16) G. Abadal, Z. J. Davis, B. Helbo, X. Borrise, R. Ruiz, A. Boisen, F. Campabadal, J. Esteve, E. Figueras, F. Perez-Murano, and N. Barniol
Electromechanical model of a resonating nano-cantilever-based sensor for high-resolution and high-sensitivity mass detection
Nanotechnology **12** (2), 100-104 (2001)

(17) N. Tas, T. Sonnenberg, H. Jansen, R. Legtenberg, and M. Elwenspoek
Stiction in surface micromachining
Journal of Micromechanics and Microengineering **6** (4), 385-397 (1996)

(18) C.B. Prater, P.G. Maivald, K.J. Kjoller, and M. G. Heaton
TappingMode Imaging: Applications and Technology, Application Note AN04
Available from www.veeco.com, Digital Instruments Veeco Metrology Group (2004)

(19) F.M. Serry, K. Kjoller, J.T. Thornton, R.J. Tench, and D. Cook
Electric Force Microscopy, Surface Potential and Surface Electric Modification with th Atomic Force Microscope, Application Note AN27
Available from www.veeco.com, Digital Instruments Veeco Metrology Group (2004)

(20) K.L Babcock and C.B. Prater

Phase Imaging: beyond topography, Application Note AN11
Available from www.veeco.com, Digital Instruments Veeco Metrology Group (2004)

(21) B. Y. Han, K. Nakayama, and J. H. Weaver
Electron- and photon-stimulated modification of GaAs(110), Si(100), and Si(111)
Physical Review B **60** (19), 13846-13853 (1999)

(22) D. Aronov and G. Rosenman
Surface energy modification by electron beam
Surface Science **601** (21), 5042-5049 (2007)

(23) B. W. Smith and D. E. Luzzi
Electron irradiation effects in single wall carbon nanotubes
Journal of Applied Physics **90** (7), 3509-3515 (2001)

(24) S. Suzuki, K. Kanzaki, Y. Homma, and S. Y. Fukuba
Low-acceleration-voltage electron irradiation damage in single-walled carbon nanotubes
Japanese Journal of Applied Physics Part 2-Letters & Express Letters **43** (8B), L1118-L1120 (2004)

(25) F. Banhart, J. X. Li, and A. V. Krasheninnikov
Carbon nanotubes under electron irradiation: Stability of the tubes and their action as pipes for atom transport
Physical Review B **71** (24) (2005)

(26) A. V. Krasheninnikov and K. Nordlund
Irradiation effects in carbon nanotubes
Nuclear Instruments & Methods in Physics Research Section B-Beam Interactions with Materials and Atoms **216**, 355-366 (2004)

(27) H. O. Jacobs, P. Leuchtmann, O. J. Homan, and A. Stemmer
Resolution and contrast in Kelvin probe force microscopy
Journal of Applied Physics **84** (3), 1168-1173 (1998)

(28) **Dessis: Comprehensive Semiconductor Device Simulator.**
Integrated Systems Engineering AG, Switzerland [Online]. Available: http://www.ise.com

(29) Yong-Hyun Kim and K. J. Chang
Subband mixing rules in circumferentially perturbed carbon nanotubes: Effects of transverse electric fields
Physical Review B **64** (15), 153404 (2001)

(30) S. V. Rotkin and K. Hess
Possibility of a metallic field-effect transistor
Applied Physics Letters **84** (16), 3139-3141 (2004)

(31) A. Vijayaraghavan, K. Kanzaki, S. Suzuki, Y. Kobayashi, H. Inokawa, Y. Ono, S. Kar, and P. M. Ajayan
Metal-semiconductor transition in single-walled carbon nanotubes induced by low-energy electron irradiation
Nano Letters **5** (8), 1575-1579 (2005)

(32) M. Zdrojek, T. Melin, C. Boyaval, D. Stievenard, B. Jouault, M. Wozniak, A. Huczko, W. Gebicki, and L. Adamowicz
Charging and emission effects of multiwalled carbon nanotubes probed by electric force microscopy
Applied Physics Letters **86** (21) (2005)

(33) M. Zdrojek, T. Melin, H. Diesinger, D. Stievenard, W. Gebicki, and L. Adamowicz
Charging and discharging processes of carbon nanotubes probed by electrostatic force microscopy
Journal of Applied Physics **100** (11) (2006)

7 Conclusions

"I would like to describe a field, in which little has been done, but in which an enormous amount can be done in principle. This field is not quite the same as the others in that it will not tell us much of fundamental physics but is more like solid-state physics in the sense that it might tell us much of great interest about the strange phenomena that occur in complex situations. Furthermore, a point that is most important is that it would have an enormous number of technical applications."

'There is plenty of room at the bottom', Richard P. Feynman.

These premonitory words were pronounced more than 40 years ago, when it seemed far from reachable. Nowadays the concept has become not only feasible, but the source of fruitful research.

Nanoscience studies new materials, structures and devices and manipulates them at the atomic, molecular and macromolecular scale. Nanotechnology is the ability to manipulate these materials, to design and fabricate the structures, devices and systems and to characterise their performance.

This thesis has little tackled with both fields for specific cases and aspects. Based on a common tool, the focused electron beam, the following subjects have been addressed:

- Establishment of EBL technique performance
- Fabrication of NEMS
- Fabrication of CNT based devices
- Evaluation of electron beam effect on devices and systems

The main results that have been achieved are next summarized and embrace the backbone information that has been exposed within chapters 3, 4, 5 and 6.

Chapter 3 compiles the results of electron beam exposure of different resist materials. It contains practical information about the use of EBL as a patterning method and about resist processing.

The response to electron beam exposure of PMMA has been studied in terms of beam energy, dose, MW and layer thickness. The results have been compared to predictions based on electron trajectory simulations and they are in agreement with the performance tendencies reported in the literature. Copolymer resist has also been studied and starting values for exposure parameters are determined.

Irradiation tests have been done on a new epoxy based resist, that has result in a new commercial negative resist available for EBL. First, the exposure parameters and results on thick layers of a SU-8 like resist, mr-L 5005, are presented. Comparison to electron trajectories simulations shows proper correlation as a function of beam energy, dose and forward and backward scattering. The resolution limitations indicate that EBL at (relatively) low beam energies serves to define submicron features or 3D structures, mainly, in combination with photolithography.

Thin layers of a new resist, mr-EBL 6000.1, are studied to determine the performance characteristics of this new polymer. Results have assessed the optimization of the resist formulation in terms of PAG containance and have established the general exposure parameters and the characteristics of features patterned at different conditions (beam energy, substrate, feature dimension vs dose, roughness, resolution, feature density, etc). The etching resistance in this material has been evaluated. In particular, it has been demonstrated that the processes for wet etching of SiO_2 and dry etching of Si can be used for fabrication of nanostructures.

The correction of proximity effect has been achieved for both PMMA and mr-EBL 6000.1. The complete correction methodology has been established. First, the proximit effect correction parameters have been experimentally determined using doughnut-like structures and they have been used to modulate the exposure dose distribution. The strategy of correction using commercial software NanoPECS has been presented. It has been checked using specific designs to determine the final adjustment of exposure parameters. Now, the methodology is available to be used in other examples.

Chapter 4 shows the results of fabrication of nanomechanical structures based on electron beam lithography.

A wide diversity of designs of mechanical devices have been defined by EBL, transferred by RIE and released by wet SiO_2 etching. Discrete nanomechanical resonators have been patterned on SOI substrates to determine the etching process parameters. Mix and match with photolithography-defined structures is performed at both chip and wafer scale level. The proper connection of resonators and piezoresistive cantilevers to contact pads has enabled the measurement of electrical sensing of resonator oscillation by capacitive detection and cantilever deflection by piezoresistivity. The most relevant important result corresponds to the monolithical integration of nanoresonators on CMOS circuits. In this case, a specific alignment procedure is established and the use of low beam energy is settled to avoid damage of the circuitry. An alternative fabrication process based on FIB machining has been tested for the integration of nanomechanical devices on CMOS demonstrating the compatibility of FIB post-processing of CMOS chips.

Chapter 5 contains the fabrication process development and electrical characterization of electronic devices based on CNTs.

CNTs have been individualy contacted on oxidised substrates by means of dedicated EBL patterning. Both deposited and on chip CVD grown CNTs have been used. In the case of CVD synthesis, four different approaches have been tested in order to control the CNT placement. The results show that the fabrication strategies using selective deposition of catalyst are the more suitable options.

Electrical characterization is realized to determine the transport characteristics of each contacted CNT and allowed to obtain the first CNTFETs fully fabricated in Spain. The general overview of the device characteristics on nearly a hundred of devices indicates that their performance is usually excellent, although certain degree of variability is registered. The first experiments to prepare CNT based devices for sensing applications are realized. In particular, protection and passivation with PMMA and mr-EBL 6000.1 have been tested. PMMA has been demonstrated to be valid to define selective aperture on CNT channel and as passivation layer. In addition, a process for the selective and oriented placement of zeolites has been defined, which is intended to be used to synthesize CNT with spatial and directional control.

Chapter 6 embraces four studies of the electron beam induced effects on various configurations, devices or systems.

The damage processes generated on NEMS integrated in CMOS circuits have been evaluated first. The damage induced by electron irradiation on MOS transistors is presented and it is correlated with the system configuration (materials, dimensions and layer thicknesses) and beam energy, and contrasted with the results reported in the literature for similar cases. Exposure test with electrons and Ga ions and on line monitoring of transistor current complement previous results. It allowed to determine the proper EBL based fabrication conditions that have been successfully used, as explained in chapter 4.

The induced motion of cantilever structures by SEM imaging is studied in detail. Not only the operation mechanism has been comprehended, but also a model that correctly quantifies the relation of incoming charge and electrostatic force is given. This might represent the starting point of the development of a new kind of NEMS, in terms of both actuation and detection.

The mechanisms and phenomena caused by electron beam exposure of bare substrates (mainly, oxidised surfaces) under different conditions have been studied by AFM based advanced characterization . In particular, EFM and KPFM are applied to determine the electron beam induced changes of substrate electrical field as a function of beam energy, dose and time. Both techniques are proved to enable high spatial resolution and sensitivity.

Finally, an exhaustive study of the effect of electron beam irradiation of CNT based devices is presented. The evidence of the degradation of CNTFET operation under electron beam exposure has been intensively characterized. Electrical degradation of the CNTFET is analized under differents conditions of beam energy, dose and charge delivery position and its time evolution is registered. Local exposure on the contacted CNT (transistor channel), at low beam energy, 3 keV, gives rise to the most important device characteristics variation. EFM has enabled to corroborate the irradiation correct positioning and the existence of built-in electric field in the silicon oxide substrate. KPFM characterization has provided unique information to dilucidate the mechanism of device degradation. Unexpected results account for the crytical nature of the

characterization in such complex electrical field configurations. Electrostatic simulation of the whole system during KPFM have been used to predict and understand the observed phenomena. Discussion of the mechanism caused by electron beam is compared to similar experiments on MOS devices and it is attributed to the oxide charging and consequential modification of CNT electronic configuration.

In summary, this thesis has provided new knowledge about the fundamentals and applications of electron beam lithography in the areas of nanofabrication, nanoelectronics and nanomechanics. This work is expected to be extended by additional nanofabrication developments, such as CNT based sensors, and specific studies of irradiation of devices with charged particles, such as C_{60} ions on CNT devices or MOS circuits.

Glossary

AFM	Atomic Force Microscope
CCD	Charge Coupled Device
CMOS	Complementary Metal Oxide Semiconductor
CNM	Centro Nacional de Microelectrónica
CNT	Carbon NanoTube
CSIC	Consejo Superior de Investigaciones Científicas
CVD	Chemical Vapor Deposition
DAC	Digital to Analogic Conversion
DNA	DesoxyriboNucleic Acid
DUV	Deep UV
EB	Electron Beam
EBL	Electron Beam Lithography
EFM	Electrical Force Microscopy
EUV	Extreme UltraViolet
FET	Field Effect Transistor
FIB	Focused Ion Beam
IBM	International Business Machines
IC	Integrated Circuit
ICN	Institut Català de Nanotecnologia
IMB	Institut de Microelectrònica de Barcelona
IPA	Isopropanol / Isopropilic Alcohol
ITQ	Instituto de Tecnología Química
KPFM	Kelvin Probe Force Microscopy
MAA	MethAcrylic Acid
MBE	Molecular Beam Epitaxy
MEMS	MicroElectroMechanical System
MIBK	Methyl Iso Butil Ketona
MMA	Methyl MethAcrylate
MOSFET	Metal Oxide Semiconductor FET
MW	Molecular Weight
NanoPECS	Nano Proximity Effect Correction Software
NEMS	NanoElectroMechanical System
NGL	Next Generation Lithography
NPGS	Nanometer Pattern Generation System
PAG	Photo Acid Generator
PC	Photonic Crystal
PDMS	PolyDiMethylSiloxane
PE	Proximity Effect
PEB	Post Exposure Bake
PEC	Proximity Effect Correction

PGMEA	Polyethilene Glycol Methyl Ether Acetate
PMMA	Poly Methyl MethAcrylate
QD	Quantum Dot
RTCVD	Rapid Thermal CVD
SB	Schottky Barier
SEM	Scanning Electron Microscope
SET	Single Electron Transistor
SNOM	Scanning Near-field Optical Microscope
SOI	Silicon On Insulator
SPL	Scanning Probe Lithography // Single Pixel Lines
SPM	Scanning Probe Microscope
STM	Scanning Tunneling Microscope
UAB	Universitat Autònoma de Barcelona
UHV	Ultra High Vacuum
UPV	Universitat Politècnica de Valencia
URV	Universitat Rovira i Virgili
UV	Ultra Violet
VLSI	Very Large Scale Integration
WA	Working Area
WD	Working Distance
WF	Write Field

Scientific CV

Publications

(1) G. Rius, A. Verdaguer, F.A. Chaves, I. Martin, P. Godignon, E. Lora-Tamayo, D. Jimenez, and F. Perez-Murano
Characterization at the nanometer scale of local electron beam irradiation of CNT based devices
Microelectronic Engineering (2008) doi:10.1016/j.mee.2007.12.014

(2) I. Martin, G. Rius, P. Atienzar, L. Teruel, N. Mestres, F. Pérez-Murano, H. Garcia, P. Godignon, A. Corma, and E. Lora-Tamayo
CVD oriented growth of carbon nanotubes using AlPO4-5 and L type zeolites
Microelectronic Engineering (Accepted)

(3) J. Arcamone, E. Dujardin, G. Rius, F. Perez-Murano, and T Ondarçuhu
Evaporation of femtoliter sessile droplets monitored with nanomechanical mass sensors
Journal Physics Chemistry B **111** (45), 13020 -13027 (2007)

(4) J. Fraxedas, G. Rius, F. Perez-Murano, and A. Verdaguer
Determining radial breathing mode frequencies of single-walled carbon nanotubes with an atomic force microscope
EuroPhysics Lett. **78** (1), 16001 (2007)

(5) C. Martin, G. Rius, A. Llobera, A. Voigt, G. Gruetzner, and F. Perez-Murano
Electron beam lithography at 10 keV using an epoxy based high resolution negative resist
Microelectronic Engineering **84** (5-8), 1096-1099 (2007)

(6) G. Rius, I. Martin, P. Godignon, A. Bachtold, J. Bausells, E. Lora-Tamayo, and F. Perez-Murano
Response of carbon nanotube transistors to electron beam exposure
Microelectronic Engineering **84** (5-8), 1596-1600 (2007)

(7) J. Arcamone, G. Rius, G. Abadal, J. Teva, N. Barniol, and F. Perez-Murano
Micro/nanomechanical resonators for distributed mass sensing with capacitive detection
Microelectronic Engineering **83** (4-9), 1216-1220 (2006)

(8) G. Gomila, I. Casuso, A. Errachid, O. Ruiz, E. Pajot, J. Minic, T. Gorojankina, M. A. Persuy, J. Aioun, R. Salesse, J. Bausells, G. Villanueva, G. Rius, Y. Hou, N. Jaffrezic, C. Pennetta, E. Alfinito, V. Akimov, L. Reggiani, G. Ferrari, L. Fumagalli, M. Sampietro, and J. Samitier
Advances in the production, immobilization, and electrical characterization of olfactory receptors for olfactory nanobiosensor development
Sensors and Actuators B-Chemical **116** (1-2), 66-71 (2006)

(9) F. Campabadal, S. Ghatnekar-Nilsson, G. Rius, C. Fleta, J.M. Rafí, E. Figueras, and J. Esteve
CMOS degradation effects due to electron beam lithography in smart NEMS fabrication
Proceedings of SPIE **5836**, 667-674 (2005)

(10) C. Martin, G. Rius, X. Borrise, and F. Perez-Murano
Nanolithography on thin layers of PMMA using atomic force microscopy
Nanotechnology **16** (8), 1016-1022 (2005)

(11) G. Villanueva, J. Montserrat, F. Perez-Murano, G. Rius, and J. Bausells
Submicron piezoresistive cantilevers in a CMOS-compatible technology for intermolecular force detection
Microelectronic Engineering **73-74**, 480-486 (2004)

Articles in preparation

(1) Performance characterization of a new epoxy based electron beam negative resist

(2) Proximity effect correction of electron beam lithography

(3) Local and oriented growth of CNTs based on zeolites for fabrication of devices

(4) Novel concept for actuating NEMS devices

(5) Effect of local electron and ion beam exposure on CMOS substrates

Contributions at scientific conferences

• Contributions at international conferences

(1) G. Villanueva, J. Montserrat, F.Pérez Murano, G. Rius, J. Bausells
Submicron piezoresistive cantilevers for intermolecular force detection in a CMOS-compatible technology
Micro and nanoengineering, MNE'03, Cambridge, UK, September 2003. Poster

(2) S. Sadewasser, G. Abadal, L. Fonseca, G. Rius, N. Barniol, J. Esteve
Development of an on-chip tunneling device
Micro and nanoengineering, MNE'04. Rotterdam, the Netherlands, September 2004. Poster

(3) F.Pérez-Murano, F. Campabadal, E. Figueras, C. Martín, G. Rius, J. Esteve
NANOMASS: Mass sensor based on resonating nanocantilevers integrated in CMOS circuits
1st Workshop on Nanomechanical Sensors. Madrid, Spain, November 15th and 16th, 2004. Invited talk

(4) G Gomila et al
Artificial nose integrating olfactory receptors and NEMS
ISOEN Conference, Barcelona, Spain, April 2005. Invited talk

(5) F. Campabadal, S. G. Nilsson, G. Rius, E. Figueras, J. Esteve
CMOS degradation effects due to electron beam lithography in smart NEMS fabrication
SPIE Symposium on Microtechnologies for the New Millennium 2005, Sevilla, Spain, May 2005. Poster

(6) C. Martín, G. Rius, X. Borrisé, F. Pérez-Murano
Direct nanopatterning on thin layers of PMMA using AFM
Micro and nanoengineering, MNE'05, Viena, Austria, September 2005

(7) J. Arcamone, G. Rius, G. Abadal, J. Teva, N. Barniol, F. Pérez-Murano
Mechanical resonator for distributed mass sensing and capacitive detection
Micro and nanoengineering, MNE'05, Viena, Austria, September 2005

(8) J. Arcamone, G. Rius, F. Pérez-Murano,
Micro/nano mechanical resonators for distributed mass sensing with Capacitive detection
International Workshop on Nanomechanical Sensors, Copenhagen, Denmark, May 7-10, 2006

(9) G. Villanueva, G. Rius, J. Montserrat, F. Pérez-Murano, J. Bausells
Piezoresistive cantilevers for intermolecular force detection

International Workshop on Nanomechanical Sensors, Copenhagen, Denmark, May 7-10, 2006

(10) G. Rius, J. Arcamone, X. Borrisé, C. Martín, J. Bausells, F. Pérez-Murano.
Fabrication of nanomechanical systems (INVITED TALK)
International Conference on Modern Materials & Technologies (CIMTEC 2006) Acireale, Sicilia, Italy, June 2006

(11) C. Martin, G. Rius, A. Llobera, A. Voigt, G. Gruetzner , F. Pérez-Murano.
A high resolution negative resist for nanopatterning by electron beam lithography
International Conference on Nanoscience and Technology ICN&T 2006. Basel, Switzerland, July 30th – August 4th, 2006

(12) C. Martin, G. Rius, A. Llobera, A. Voigt, G. Gruetzner, F.Pérez-Murano
Electron beam lithography at 10 keV using an epoxy based high resolution negative resist
32nd International Conference on Micro and Nano Engineering (MNE'06), 17-20 September 2006, Barcelona, Spain. 2006. Poster

(13) G. Rius, I. Martín, P. Godignon, A Bachtold, J. Bausells, E. Lora-Tamayo, F.Pérez-Murano,
Response of carbon nanotube transistors to electron beam exposure
32nd International Conference on Micro and Nano Engineering (MNE'06), 17-20 September 2006, Barcelona, Spain. 2006. Poster

(14) J. Arcamone, G. Rius, J. Llobet, X. Borrise, F. Pérez-Murano
Mass measurements based on nanomechanical devices: differential measurements
International Conference on Nano Science and Technology (ICN+T 2007). Stockholm, Sweden. 2007. Oral presentation.

(15) G. Rius, I. Martín, P. Godignon, A. Bachtold, J. Bausells, E. Lora-Tamayo, F. Pérez-Murano
Rapid thermal CVD growth of carbon nanotube transistors and its response to electron beam exposure
Spring Meeting of the European Material Research Society (E-MRS). Strasbourg, France. 2007. Poster

(16) G. Rius, A. Verdaguer, F.A. Chaves, I. Martin, P. Godignon, E. Lora-Tamayo, D. Jimenez, and F. Perez-Murano
Characterization at the nanometer scale of local electron beam irradiation of CNT based devices
Micro and Nano Engineering (MNE'07), 23-26 September, 2007. Copenhagen, Denmark. Poster.

(17) I. Martin, G. Rius, P. Atienzar, L. Teruel, N. Mestres, F. Pérez-Murano, H. Garcia, P. Godignon, A. Corma, and E. Lora-Tamayo
CVD oriented growth of carbon nanotubes using AlPO4-5 and L type zeolites

Micro and Nano Engineering (MNE'07), 23-26 September, 2007. Copenhagen, Denmark. Poster.

(18) X. Borrise, G. Rius, J.Arcamone, J.Llobet, F.Perez-Murano
Focused ion beam fabrication and functionalization of CMOS integrated silicon nanocantilevers
Micro and Nano Engineering (MNE'07), 23-26 September, 2007. Copenhagen, Denmark. Poster.

(19) J. Arcamone, T. Ondarçuhu, E. Dujardin, G. Rius and F. Pérez-Murano
Monitoring the evaporation of femtoliter droplets with CMOS integrated nanomechanicals sensors
2007 IEEE Sensors conference. Atlanta, USA. Oral presentation.

(20) J. Arcamone, T. Ondarçuhu, E. Dujardin, G. Rius and F. Pérez-Murano
Monitoring the evaporation of femtoliter droplets with CMOS integrated nanomechanicals sensors
2007 MNC, Kyoto, Japan. November 2007. Oral presentation.

• Contributions at national conferences

(21) J. Bausells, G. Rius, J. Montserrat, M. Duch, G. Villanueva, F. Pérez -Murano
Development of a silicon nanocantilever technology with electron beam lithography
4ª Conferencia de Dispositivos Electrónicos (CDE 2003), Calella de la Costa (Barcelona), 12-14 de febrero de 2003.

(22) J. Bausells, F. Pérez-Murano, J. Esteve, J.A. Plaza, J. Montserrat, G. Villanueva, G. Rius
Fabrication of micro/nano electromechanical devices in silicon
1st Nanospain Workshop. San Sebastian, 10-12 de Marzo de 2004

(23) S. Sadewasser, G. Abadal, L. Fonseca, G. Rius, N. Barniol, J. Esteve
Desarrollo de un dispositivo de efecto túnel integrado
IV Congreso Español de Fuerzas Atómicas y Efecto Túnel. Vic, Septiembre 2004.

(24) F. Campabadal, S. Ghatnekar-Nilsson, G .Rius, E. Figueras, J. Esteve
Nanocantilevers with integrated CMOS: Effects of electron beam lithography on NMOS transistors
Spanish Conference on Electron Devices, Tarragona, Febrero 2005

(25) G. Rius, M.Villarroya, J. Verd, J. Teva, G. Abadal, E. Figueras, J. Esteve, N. Barniol, F. Pérez-Murano
Patterning of nanometer-scale cantilevers integrated in CMOS circuit by e-beam lithography
2nd Nanospain Workshop. Barcelona, 14-17 de Marzo de **2005**

(26) G. Rius, G. Villanueva, X. Borrisé, A. Errachid, J. Bausells, F. Pérez-Murano
Fabrication of electrodes with controllable sub-20 nm gap spacing
2nd Nanospain Workshop. Barcelona, 14-17 de Marzo de **2005**

(27) J. Arcamone, G. Rius, X. Borrisé, F. Pérez-Murano
Combination of e-beam and UV lithography for the prototyping of nano-mechanical devices
2nd Nanospain Workshop. Barcelona, 14-17 de Marzo de **2005**

(28) G. Rius, S. Blanqué, X. Borrisé, A. Bachtold, F. Pérez- Murano
Contacting single carbon nanotubes by e-beam lithography.
3rd Nanospain Workshop. Pamplona, 20-23 de Marzo de **2006**

(29) G. Villanueva, G. Rius, J. Montserrat, F. Pérez-Murano, J. Bausells
Piezoresistive cantilevers for molecular force detection
3rd Nanospain Workshop. Pamplona, 20-23 de Marzo de **2006**

(30) C. Martin, G. Rius, A. Llobera, A. Voigt, G. Gruetzner, F. Pérez-Murano
Electron beam lithography at 10 KeV using an epoxy-based high resolution negative resist
Jornadas de Nanofabricacion. Barcelona, Noviembre de 2006. Poster

(31) I. Martin, G. Rius, N. Mestres, F. Perez-Murano, E. Lora-Tamayo, P. Godignon
Local growth of carbon nanotubes by thermal Chemical Vapour Deposition from iron based precursor nanoparticles
Jornadas de Nanofabricación. Barcelona, Noviembre de 2006. Poster

(32) G. Villanueva, G. Rius, J. Montserrat, F. Pérez-Murano, J. Bausells
Piezoresistive cantilevers for molecular force detection
Jornadas de Nanofabricación. Barcelona, Noviembre de 2006. Poster