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Novel materials and processes for gate dielectrics on Silicon carbide

A dissertation submitted to the department of physics and the committee on graduate studies of Universitat Autònoma de Barcelona in partial fulfilment of the requirements for the degree of doctor of philosophy by:

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CERTIFICA

El treball que duu per títol "*Novel materials and processes for gate dielectrics on Silicon carbide*", presentat per Amador Pérez Tomás que constitueix el treball de Tesis del programa de Tercer Cicle de Ciències de Materials, ha estat realitzat sota la direcció de Philippe Godignon, Científic Titular del CSIC.

Bellaterra, Juny de 2005

Dr. Philippe Godignon

Tutor: Prof. Jordi Pascual i Gainza

A Sílvia, Amador i Núria.

(…) οὐ σέ γ᾽ ἔπειτα ἔολπα τελευτήσειν, ἃ μενοινᾷς.
παῦροι γάρ τοι παῖδες ὁμοῖοι πατρὶ πέλονται,
οἱ πλέονες κακίους, παῦροι δέ τε πατρὸς ἀρείους.
ἀλλ᾽ ἐπεὶ οὐδ᾽ ὄπιθεν κακὸς ἔσσεαι οὐδ᾽ ἀνοήμων,
οὐδέ σε πάγχυ γε μῆτις Ὀδυσσῆος προλέλοιπεν, (…)

Ὁμήρου

Ὀδύσσεια
Ραψῳδία β´, 275 – 280

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Bellaterra, Catalunya, *June* 2005

Contents

VI. Alternative high-*k* gate dielectrics

VII. Field-effect mobility model with high traps density in the interface

VIII.   Conclusions and future work

Notation

Symbol	Description
A	Effective Richardson constant
A_{DG}	Deal-Grove linear rate constant
A_{gate}	Gate Area
B	Fitting parameter for the acoustic-phonon scattering (1)
b'	Direct tunneling constant
B_{DG}	Deal-Grove parabolic rate constant
C	Capacitance
$C1$	Fitting parameter for the acoustic-phonon scattering (2)
C_{fb}	Flat band capacitance
C_{HF}	High Frequency capacitance
C_I	Insulator capacitance
C_{it}	Interface traps capacitance
C_{LF}	Low Frequency capacitance
C_m	Measured capacitance
c_n	Interface trap electron capture probability
c_p	Interface trap hole capture probability
C_s	Semiconductor capacitance
D	Fitting parameter for the surface roughness scattering (1)
D_{it}	Interface states/traps density
$\bar{E}, E$	Electric Field
E_B	Activation energy for Deal-Grove parabolic rate
$E_{B/A}$	Activation energy for Deal-Grove linear rate
E_{bd}	Electric breakdown field
E_{cr}	Semiconductor critical electric field
E_C	Conduction band energy

E_F	Fermi energy
E_g	Energy of band gap
E_i	Intrinsic level energy
E_{ins}	Electrical field within the insulator
E_T	Interface trap energy
E_V	Valence band energy
E_{YI}	Perpendicular electric field at the interface (insulator)
E_{YS}	Perpendicular electric field at the interface (semiconductor)
$E_\perp$	Effective perpendicular electric field at the interface
$f(\omega)$	Frequency
$f_p(\omega_p)$	Frequency corresponding to the peak value of $\langle G_P \rangle / \omega$
f_i	IT occupancy factor for the ith energy level
G_m	Measured admittance
g_m	Transconductance
G_P	Equivalent MIS parallel conductance
h	Planck constant
I_{DS}	Drain-source current
I_{DSsat}	Drain-source current at the saturation
J	Current density per unit area
k	Boltzman constant
K_T	High frequency dielectric constant
l	Interval between two sites in hopping conduction
L	Channel length
L_D	Intrinsic Debye length
$L_{Dp(n)}$	Debye length for holes (electrons)
$m*$	Effective mass
M_x	x molecular weight, x: Ta$_2$O$_5$, SiO$_2$, Ta$_2$Si, O-Ta$_2$Si
n	Electron concentration
N	Fitting parameter for the IT Coulombic scattering (1)
$n*$	Density of free electrons in the insulator
N_A	Acceptor impurity concentration
N_D	Donor impurity concentration
n_i	Intrinsic carrier concentration
N_{it}	Total number of traps
n_{op}	Optical refractive index value
N_{REF}	Bulk mobility parameter (3)
p	Hole concentration
q	Electron charge
Q_f	Insulator fixed charges
Q_G	Charge on the MIS-C gate
Q_I	Effective insulator charge

Q_{inv}	Inversion charge per unit area
Q_m	Insulator mobile ionic charges
Q_{ot}	Insulator trapped charges
Q_{trap}	IT trapped charge per unit area
r	Poole-Frenkel compensation term
R_{on}	On-resistance
S	Subthreshold slope
T	Temperature
t_{eq}	SiO$_2$ equivalent thickness
t_{ins}	Insulator thickness
t_{ox}	Oxide thickness
t_x	x thickness, x: Ta$_2$O$_5$, SiO$_2$, Ta$_2$Si, O-Ta$_2$Si
t	Time
U	Normalized electrostatic potential
U_F	Normalized Fermi potential
U_s	Normalized electrostatic potential at the semiconductor surface
V	Electrostatic potential
V_G'	Ideal MIS-C gate bias
V_{bd}	Electric breakdown voltage
V_{DS}	Drain-source voltage
V_{DSsat}	Drain-source voltage at the saturation
V_{fb}	Flat band voltage
V_G	MIS-C gate bias
V_{GS}	Gate-source voltage
V_S	Source voltage
v_{sat}	Saturation electron drift velocity
V_T'	Ideal MIS threshold voltage
$\overline{v_{th}}$	Average thermal velocity of the electron gas
V_{th}	MOSFET threshold voltage
W	Channel width
α	Coulomb scattering temperature coefficient
$\alpha 1$	Fitting parameter for the acoustic-phonon scattering (3)
β	Coulomb scattering inversion charge coefficient
Δn	Additional inversion carrier concentration
Γ	Mean hopping frequency
$\gamma 1$	Fitting parameter for the surface roughness scattering (2)
ε_0	Permittivity of free space
ε_I	Insulator permittivity
ε_i	Insulator dynamic permittivity
ε_r	Effective dielectric constant / dielectric permittivity

ε_s	Semiconductor permittivity
ε_x	x dielectric permittivity, x: Ta$_2$O$_5$, SiO$_2$, Ta$_2$Si, O-Ta$_2$Si
θ	XRD glancing angle / (2θ) diffraction angle
λ	Wavelength
$\lambda 1$	Bulk mobility parameter (4)
μ_{AC}	Acoustic-phonon scattering mobility
μ_B	Bulk mobility
μ_C	(Interface traps) Coulombic scattering mobility
μ_{EFF}	Effective mobility
μ_{FE}	Field effect mobility
μ_{inv}	Inversion mobility
μ_{max}	Bulk mobility parameter (1)
μ_{min}	Bulk mobility parameter (2)
μ_n	Electron mobility of the semiconductor
μ_p	Hole mobility of the semiconductor
μ_{scl}	Space-charge-limited mobility
μ_{SR}	Surface roughness scattering mobility
ϕ	Surface potential
ϕ_a	Activation energy of electrons
ϕ_B	Fermi potential
ϕ_i	Activation energy of ions
Φ_m	Metal work function
Φ_{ms}	Metal-semiconductor work function difference
ϕ_s	Surface potential at the semiconductor surface
ϕ_t	Barrier height
ψ	Band bending
ψ_s	Band bending at the semiconductor surface
ρ	Charge density
ρ_I	Insulator mobile ionic charges distribution
ρ_s	Surface charge density
ρ_x	x density, x: Ta$_2$O$_5$, SiO$_2$, Ta$_2$Si, O-Ta$_2$Si
χ_S	Semiconductor electron affinity
σ_{it}	Capture cross section of the interface states
σ_s	Standard deviation of the band bending
σ_T	Thermal conductivity
τ	Deal-Grove time constant
τ_n	Interface trap time constant for electrons
τ_p	Interface trap time constant for holes

List of Acronyms

ACCUFET	Accumulation Channel MOSFET
AFM	Atomic Force Microscopy
APCVD	Atmospheric Pressure Chemical Vapor Deposition
BFM	Baliga' Figure of Merit
CCD	Charged Couple Device
CMOS	Complementary Metal-Oxide-Semiconductor
CNM	Centre Nacional de Microeletrònica
CRT	Cathode Ray Tube
C-V	Capacitance – Voltage
CVD	Chemical Vapor Deposition
DMOS	Double-diffused Metal-Oxide-Semiconductor
EDX or EDS	Energy Dispersive X-Ray Spectroscopy
EEPROM	Electrically Erasable and Programmable Read Only Memory
ESR	Electron Spin Resonance
HT	High Temperature
HTCVD	High Temperature Chemical Vapor Deposition
HVEM	High Voltage Electron Microscopy
IBT	Insulated Base Transistor
IC	Integrated Circuit
IGBT	Insulated Gate Bipolar Transistor
IT	Interface Traps
I-V	Current – Voltage
JFM	Johnson' Figure of Merit
JVD	Jet Vapor Deposition
KFM	Keyes' Figure of Merit
LCVD	Laser-induced Chemical Vapor Deposition
LDMOS	Lateral Double-diffused MOSFET
LPCVD	Low Pressure Chemical Vapor Deposition
LTO	Low Temperature Oxide
LT-SiO$_2$	Low Temperature Thermally Grown (O$_2$) SiO$_2$
MEMS	Micro-Electro-Mechanical Systems
MIS	Metal-Insulator-Semiconductor
MIS-C	Metal-Insulator-Semiconductor Capacitor
MOS	Metal-Oxide-Semiconductor

MOS-C	Metal-Oxide-Semiconductor Capacitor
MOSFET	Metal-Oxide-Semiconductor Field Effect Transistor
N_2O-Ta_2Si	Oxidized (N_2O) Ta_2Si
NSG	Non-doped Silicate Glass
O-Ta_2Si	Oxidized (O_2) Ta_2Si
O-$TaSi_2$	Oxidized (O_2) $TaSi_2$
PCVD	Photo-induced Chemical Vapor Deposition
PECVD	Plasma Enhanced Chemical Vapor Deposition
PVT	Physical Vapor Transport or Sublimation
Q-V	Charge – Voltage
RAF	Repeated a-Face Growth Process
RBS	Rutherford Backscattering Spectrometry
RCA	Radio Corporation of America
RF	Radio-Frequency
RMS	Roughness Mean Square
RTA	Rapid Thermal Annealing
RTCVD	Rapid Thermal Chemical Vapor Deposition
SAXS	Small Angle X-ray Scattering
SEM	Scanning Electron Microscopy
SIMS	Secondary Ion Mass Spectrometry
SPM	Scanning Probe Microscopy
TEM	Transmission Electron Microscopy
TEOS	Tetra-ethoxy-silane
TFT	Thin-Films Transistor
TLM	Transmission Line Model
ToF	Time of Flight
ToF-SIMS	Time of Flight Secondary Ion Mass Spectrometry
T-SiO_2	Thermally Grown (O_2) SiO_2
UHT-CVD	Ultra-High Vacuum Chemical Vapor Deposition
UV	Ultra-Violet
VDMOS	Vertical Double-diffused MOSFET
VLSI	Very Large Scale Integration
XPS	X-ray Photoelectron Spectroscopy
XRD	X-Ray Diffraction
XTEM	X-ray Transmission Electron Microscopy

Chapter I

Introduction

Perhaps you have never think on it, but Silicon devices have changed our life for ever. When we look back in our recent evolution, only a few technological advances have been so decisive. The first big changes in people's lives and ideas began to occur only about 10,000 years ago. The Neolithic Revolution changed the way humans daily lived their nomadic lives creating a consistent food source, new materials, and new tasks. 5,000 years ago, the rise of the writing in the Middle East civilizations allows the efficient transmission of knowledge from one generation to the next. Science and philosophy spring from this simple achievement. Another simple advance will provoke the next revolution, the printing press. The process was developed independently in China and Europe. Before the invention of printing, multiple copies of a manuscript had to be made by hand, a laborious task that could take many years. Printing made it possible to produce more copies in a few weeks than formerly could have been produced in a lifetime by hand. Invented by Gutenberg in 1450, the printing press made the mass publication and circulation of ideas and literature possible. Since then, the technological and scientific achievements have been countless. In the last decades of the last century arises the small but with great impact last breakthrough, the transistor. The transistor is on the basis of the last great change: the global digital revolution.

1.1. Motivation

As hundreds of thousands of interconnected tiny polyps make up a colossal coral colony, transistors are the base of computers and innumerable electronic devices. Computers are connected in a global network around the world. The information available is now almost infinite and immediate, the sources are innumerable and plural. Nothing will be the same, this is our revolution. There are nothing more abundant than transistors fabricated for men on earth. The most of these transistors are made of Silicon, and are metal-oxide-semiconductor (MOSFET) devices, that is a sort of sandwich made up with Silicon, Silicon dioxide (SiO_2, generally know as *gate dielectric or gate oxide*) and a metal. The great success of the digital technology seems to indicate

1

that Silicon is the most suitable material for this issue. However, Silicon is a mediocre material for electronic applications. There are a number of potential semiconductors that improve the performances of Silicon. Hence, where lies the success of Silicon as the material of the digital revolution?. There are two main technological and one economic reasons for the overwhelming Silicon predominance:

    i)   The capability to grow large area wafers with controlled doping properties and very low residual defect density.

    ii)   Its insulator native oxide: SiO_2.

    iii)   Its abundance and low cost.

Silicon is an ordinary semiconductor, but SiO_2 is one of the best insulators that are known[1]. It can be argued that the key element enabling the scaling of the Silicon based metal-oxide-semiconductor is the material properties associated with the dielectric employed. The use of amorphous, thermally grown SiO_2 offers several key advantages in microelectronic processing including a stable (thermodynamically and electrically), high quality Si-SiO_2 interface as well as superior electric isolation properties.

There is now considerable evidence of the need for a semiconductor technology which exceeds the limitations imposed by silicon across a wide spectrum of industrial applications. Examples range from in-engine sensors and controls for automotive and aerospace sectors to electronic system for power transmission and distribution. Wide bandgap semiconductor, such as Silicon carbide (SiC), Gallium nitride (GaN) and diamond, offer the potential to overcome both the temperature and voltage blocking limitations of Si. They are expected to play critical roles in applications for well logging, aerospace, automotive and other industrial sectors[2]. The gradual emergence of wide bandgap semiconductor technology in these areas not only will greatly improve device and system performances, but will also reduce maintenance costs due to improved reliability.

On the other hand, SiC is proving to be the most attractive candidate, offering significant potential advantages at both high temperature and high voltage levels whilst benefiting from tractable materials technology. Moreover, SiC is the only that can be thermally oxidized to form a high quality native oxide (SiO_2), which enables the fabrication of MOS based devices. Although SiC offers substantial advantages over Si, it is still immature as a semiconductor material. Recently, new breakthroughs in the fields of material growth and of technological processes have been proposed[3], which will boost the development of SiC microelectronic devices and its industrial production. Concretely, production of high quality material on large area wafers (4") is now possible. However, single crystal wafers of SiC have only been commercially available since around 1990 and a number of critical material and processing issues are still under active investigation. These investigation fields include activation of ion implanted impurities, formation of thermally stable contacts, reliable and controllable etching techniques, and specially high quality dielectric films suitable for MOS devices[4]. To this last exiting challenge, improve the poor quality of the interface of insulator layers grown on SiC substrates, are focused the main efforts carried out in the framework of this thesis.

1.2. Outline of the thesis

The attractive physical and electrical properties of Silicon carbide are reviewed in *Chapter II*. This chapter also surveys recent progress towards the realization of commercial SiC wafers with regard to performance limiting areas, where most technological maturation is required. The main current and potential applications of SiC devices are enumerated, introducing one of the primordial problems still unsolved: the poor quality of the interface between the SiC surface and the gate oxide on SiC devices.

Metal-insulator-semiconductor (MIS) capacitors (with or without metallization) are a structure widely used to characterize and distinguish a suitable gate oxide on a semiconductor. The physical and electrical characterization methods of MIS structures used throughout this thesis are described in *Chapter III*. Physical methods are generally aimed at the composition or structural analysis of the insulator. Electrical methods are mainly used to extract the dielectric properties of the insulator or to determine the quality of the insulator/semiconductor interface.

Chapter IV reviews the thermal oxidation of SiC to form gate oxide. In this thesis, thermal oxidation are performed in O_2 (dry or wet) or diluted N_2O under different conditions. Metal-oxide-semiconductor field effect transistors (MOSFETs) are fabricated with thermally grown oxides as gate insulator. A SiC MOSFET performances state-of-the-art is detailed in this chapter.

Thermal oxidation produces oxides with low interfacial quality, presumably due to problems related with Carbon liberation. One possible solution is the use of deposited oxides as gate dielectric. *Chapter V* is focused to the study of deposited oxides (based on SiO_2) to form gate dielectrics using different precursors (SiH_4, TEOS, Si) and procedures. Promising results are obtained for the PECVD TEOS oxides.

Alternative insulators to SiO_2 are studied in *Chapter VI*. The innovative Tantalum silicide (Ta_2Si) oxidation is a simple way to produce a high-*k* dielectric on SiC ($\varepsilon_r \sim 20$). High-*k* dielectrics for gate dielectric fabrication present several key advantages respect to Silicon dioxide, but their development is still immature even on Silicon substrates. One of the first well behaved high-*k* SiC MOSFET available on the literature has been developed in this thesis using the oxidized Ta_2Si layers. Stacked structures made up with SiO_2 and oxidized Ta_2Si, and the oxidation of the common silicide ($TaSi_2$) have also been characterized as gate oxides.

Chapter VII is a theoretical foray into the MOSFET electrical response when a high density of interface traps is present. Our starting point is the semi-empirical well established Lombardi model taking into account interface trap scattering. From this model (with adequate modifications) along with 2D simulations, the experimental field-effect mobility of SiC MOSFETs can be reproduced. The Coulomb scattering on interface traps is also used to explain the commonly reported dependence of the field effect mobility on doping and temperature, and other unreported effects such as the anomalous mobility enhancement of Ta_2Si transistors in strong inversion.

The conclusions of this thesis are finally drawn in *Chapter VIII* and recommendations for future work are suggested.

References

[1]   D. A. Muller, T. Sorsch, S. Moccio, F. H. Baumann, K. Evans-Lutterodt, and G. Timp, *Nature,* **399**, 758, (1999).

[2]   NASA Silicon Carbide Electronics, http://www.grc.nasa.gov/www/SiC/index.html

[3]   D. Nakamura, I. Gunjishima, S. Yamaguchi, T. Ito, A. Okamoto, H. Kondo, S. Onda, and K. Takatori, *Nature,* **430**, 1009, (2004).

[4]   V. V. Afanas'ev, F. Ciobanu, S. Dimitrijev, G. Pensl, and A. Stesmans , *Mater. Sci. Forum* **483-485**, pp. 569, (2005).

Chapter II

Why Silicon carbide?

Silicon Carbide (SiC) is a wide band gap semiconductor with specific electrical properties such as a high breakdown electric field, a high thermal conductivity and a high inertness. Recently, new breakthroughs in the fields of material growth and of technological processes have been proposed, which will boost the development of SiC microelectronic devices and its industrial production. Concretely, production of high quality material on large area wafers is now possible, allowing the fabrication of reliable high temperature, high frequency or high current power electronic devices, improving the already optimised Silicon based structures. SiC devices possess a very wide range of industrial applications, such as spacecraft, aircraft, automobile, communication or energy distribution, among others. Therefore, SiC devices are expected to play a fundamental role, in normal life and in the cutting edge investigations, for high current/voltage management or harsh environments in the 21st century. An additional advantage of SiC is that among compound semiconductors, only SiC can be thermally oxidized to grow insulating, high quality SiO_2 layers. These insulating layers are of paramount importance in nearly all the SiC applications described below. However, the poor quality of the interface between the insulator and the semiconductor, is nowadays a great obstacle for this sort of devices.

2.1. Physical and electrical properties of SiC

Silicon carbide is the only stable binary compound of silicon and carbon existing in a solid phase. It crystallizes in three Bravais lattices[1]:

- Close packed cubic (zincblende structure)
- Hexagonal (wurtzite structure)
- Rhombohedral

The ion (12%) – covalent (78%) bonding of Silicon ($1s^2 2s^2 2p^2 3s^2 3p^2$) and carbon ($1s^2 2s^2 2p^2$) atoms is tetrahedral with a binding energy of 5 eV [2]. In real space, each Bravais lattice corresponds to two interpenetrating sublattices of silicon and carbon atoms. The material exhibits the phenomenon of poytypism, which refers to one-dimensional polymorphism, i.e. the existence of geometrically different stacking of the basic structural elements: the {111} Si-C bilayers of cubic structure or the equivalent {0001} layers of the hexagonal modification[3]. In the zincblende structure, there are three alternating layer pairs of silicon and carbon, which are obtained by slicing the fcc structure perpendicular to its (111) axis. This is the only pure cubic SiC polytype, also known as β-SiC. Two alternating layers can be distinguished in the wurtzite structure, which represents the only pure hexagonal SiC polytype. All other polytypes are combination of these basic structures. Many other stacking arrangements can thus occur, yielding a wide range of ordered, long period, stacked hexagonal or orthorombrohedral structures, which are collectively known as α-SiC. The stacking sequence of the close-packed planes of covalently bonded Si-C elements[3] can be described by the Ramsdell notation, according to their positions in the lattice, as it is shown in Fig. 2.1.
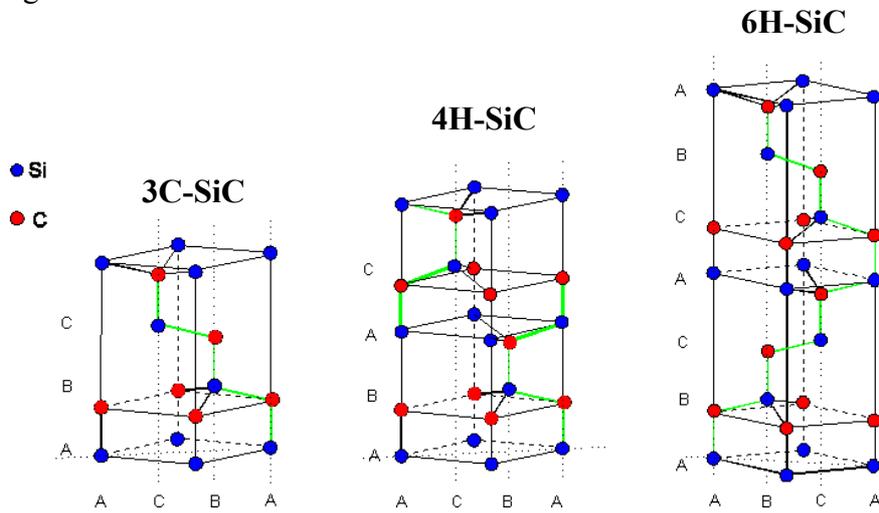
Fig. 2.1. Stacking sequences of 3C-SiC, 4H-SiC and 6H-SiC.

The basic forms are indicated by 3C, 2H and R where the number gives the layer pairs of the succession period and C, H, and R, refer to cubic, hexagonal, and rhombohedral form. The reason for the occurrence of polytypism in SiC may be the small energy difference of about 2.4 meV per atom between the cubic and the hexagonal stacking[1].

SiC shows excellent mechanical and electronic properties which can, however, vary significantly between different SiC modifications, due to different arrangements of the silicon and carbon atoms in the unit cell between the SiC polytypes. Relevant material properties of Si and diamond and of the 3C, 6H, and 4H polytype of SiC are shown in Table II.1. The various forms of SiC have the largest indirect energy gaps found in common semiconductor materials, ranging from 2.2 eV for 3C-SiC to 3.33 eV for 2H-SiC at room temperature. This indicates its potential for use in heterostructure electronic devices and high energy wavelength emission (e.g. blue light) and reception (e.g. UV light)[1]. Due to its wide bandgap a remarkable small intrinsic carrier concentration, n_i, of about 10^{-1} cm^{-3} for 3C-SiC and 10^{-10} cm^{-3} for 2H-SiC is found. For proper device operation, it should be negligible compared to the doping concentration. Electronic

devices based on SiC are predicted to operate at temperatures up to 900 °C ($n_i \sim 10^{15}$ cm^{-3}) without suffering from intrinsic conduction effects[1]. Due to the exponential temperature dependence of failures rates, the reliability of those devices operating at lower temperatures will moreover be orders of magnitude higher that than obtained from Si devices.

Material	E_g (eV) @300K	μ_n (cm²/V.s)	μ_p (cm²/V.s)	v_{sat} (cm/s)	E_{cr} (V/cm)	σ_T (W/cm)	ε_r
Si	1.12(i)	1 450	450	10^7	3×10^5	1.3	11.7
GaAs	1.4(d)	8 500	400	$2 \times e10^7$	4×10^5	0.54	12.9
3C - SiC	2.3(i)	900	90^a	2.5×10^7	2×10^6	5	9.6
6H - SiC	2.9(i)	415	90	2×10^7	2.5×10^6	5	9.7
4H - SiC	3.2(i)	950	115	2×10^7	3×10^6	5	10
GaN	3.39(d)	1000	350	2×10^7	5×10^6	1.3	8.9
Diamond	5.6(i)	2200	1800	3×10^7	5.6×10^7	20	5.7

Table II.1. Electrical parameters of the main microelectronics semiconductors. (i) indirect gap, (d) direct gap. From Ref. [1], [2].^{a}Rough estimate.

The free carrier mobility in SiC is lower that in Si or diamond which is attributed to the partial polar bonding of the Si and C atoms. The free carrier mobility is also related to the SiC polytype. 6H-SiC has, for example, the lowest electron mobility of the three SiC modifications compared in Table II.1, due to the built-in potential, 6H-SiC has an additional long period of the potential field of 15.12 Å, indicating the existence of small minibands whose band discontinuities control the scattering and transport properties. For 3C-SiC the width of the mini-Brillouin zones is sufficiently large (the period of the stacking arrangement is about 4.4 Å), and the transport properties are not greatly influenced by the miniband structure[5]. Electron mobility and hole mobility are critically important device parameters, affecting the microwave performance, transconductance, output gain and on-resistance of MOSFETs[6]. Although carrier mobility in SiC is relatively low at low electric fields, in high power high frequency applications, it is compensated by the high saturation electron drift velocity (v_{sat}) and high critical electric field (E_{cr}).

Figures of Merit	Si	3C-SiC	6H-SiC	4H-SiC	Diamond
$JFM = \left(E_{cr} v_{sat} / \pi \right)^2$	1	900	900	1640	11664
$BFM = \varepsilon_r \mu_n E_{cr}^3$	1	140	920	1840	84.4
$KFM = \sigma_T \sqrt{v_{sat} / \varepsilon_r}$	1	5.8	5.1	5.9	32.1

Table II.2. Normalized figures of merit for Si, diamond and the most important SiC polytypes. From Ref. [7].

The expected theoretical performance of a semiconductor material for this application can be expressed by Johnson's figure of merit (JFM), which considers the high frequency and high power capability of transistors[7]. The normalized values of

Johnson's figure of merit of the common SiC polytypes are shown in Table II.2. in comparison to Si and diamond. As can be inferred, the values are significantly higher for SiC and diamond, indicating the high potential of those materials. One of the most advantageous property of SiC is its high breakdown electric field, allowing this material to withstand a voltage gradient up to 10 times higher than Si without undergoing avalanche breakdown. This permits much higher doping and thinner drift region layers in vertical SiC power device structures for a given blocking voltage, resulting in considerably lower specific on-resistances[7]. An indication of the performances of high voltage unipolar devices in SiC can be deduced from Baliga's figure of merit (BFM) shown in Table II.2. The high thermal conductivity of SiC also indicates the potential for high device packing density for integrated circuits[7], as the limit on the device size is set by the maximum permissible thermal resistance of the semiconductor material. Keyes' figure of merit (KFM), which takes into account the thermal limit of the high frequency device performance imposed by the semiconductor is given in Table II.2. Collectively, the outstanding material properties of all common polytypes allow SiC devices to offer tremendous benefits over other available semiconductor devices in optical, high temperature, high frequency, high power, and radiation hard applications, as we will detail further on[8].

2.2. SiC material growth

The availability of high purity and defect free on large area wafers is of vital importance for the industrial development. The feasibility to produce low cost, high volume large area Si wafers has been one of the main reasons for its success and domination in the microelectronic applications. Currently SiC has not reached yet the performances of Si in terms of material quality but recent breakthrough should be a step forward allowing the fully industrialization of SiC devices and systems. Today, the main polytype of SiC produced is the 4H polytype due to its superior carrier mobility and critical electric field. The main techniques currently used to grow SiC are based on vapor phase growth techniques, such as sublimation (PVT) and Chemical Vapor Deposition (CVD), for both bulk SiC and epilayers.

(a)   (b)
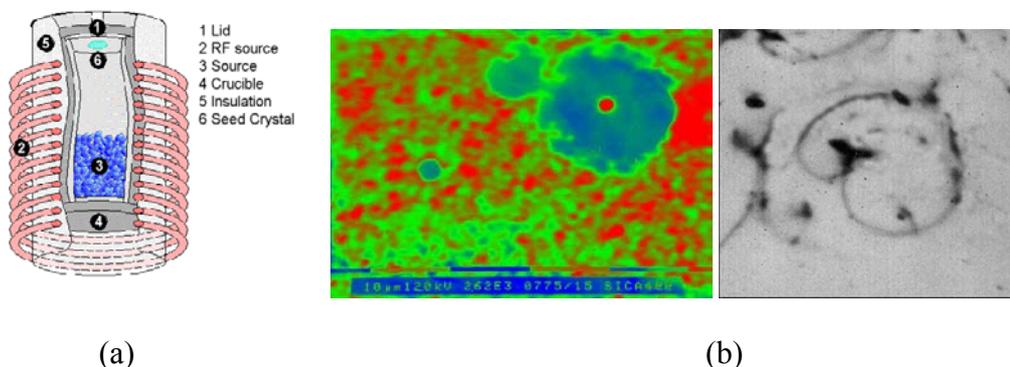
Fig. 2.2. (a) http://www.ifm.liu.se/matephys/, Schematic drawing of the modified Lely setup. (b) http://www.df.unibo.it/semiconductors/image_gallery.htm, Scanning electron microscopy image of typical micropipes (left side) and dislocations (right side).

Concerning bulk growth, the Lely modified technique[9] based on the sublimation of SiC at temperatures higher than 2000 ºC (Fig. 2.2 (a)), is used nowadays by the main SiC substrate providers from USA (CREE: www.cree.com), Japan (Sixon: www.sixon.com) and Europe (SiCrystal: www.sicrystal.com).

The growth rate is in the range of few mm/hour. Currently the standard commercially available wafer size is 3 inches. It is widely considered by the device manufacturers that 4 inches is the minimum wafer diameter to manufacture industrially viable devices. Up to date, 4 inches wafers have been demonstrated with high quality and low defects density. Micropipes (μp) are the main device killer defects in the SiC substrates, and the micropipe density is the main parameter limiting the size of the microelectronic devices (Fig. 2.2(b)). Micropipe densities lower than 5 μp/cm^2 on 3 inches commercial wafers have been obtained. Micropipes densities lower than 1 μp/cm^2 have been demonstrated and are expected in the market very soon. Other defects however are also present in the SiC crystal such a dislocations (500-1000 cm^{-2}) and stacking faults, which are particularly prejudicial for bipolar device fabrication (Fig. 2.2(b)). Then, other approaches can be used for SiC bulk growth. In the case of semi-insulating substrates used especially for RF devices, wafers grown by means of a high temperature CVD (HTCVD) process[10] have shown better characteristics than the Lely modified wafers since the purity of the starting material is higher, resulting in a lower residual doping. The HTCVD technique can also be used for N$^+$ or P$^+$ substrate growth but it has not provided superior characteristics than the conventional method. Recently CVD has been also used by Hoya[11] to grow 3C bulk material.
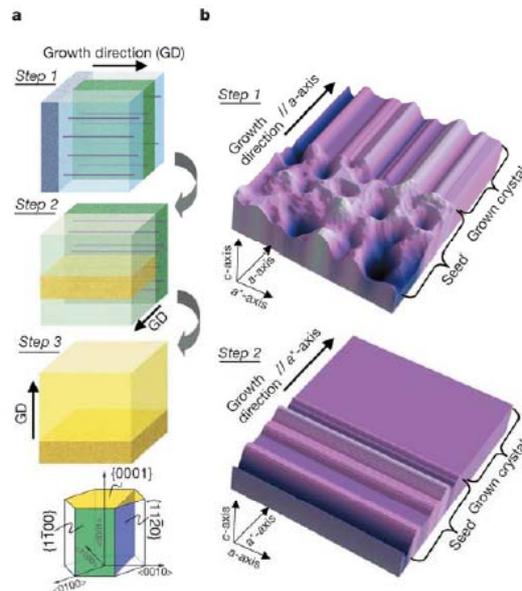
Fig. 2.3. Schematic illustrations of 'repeated a-face' (RAF) growth process. (1): first a-face growth. (2): second a-face growth perpendicular to first a-face growth. (3): c-face growth with offset angle of several degrees. From Ref. [12].

Nevertheless, the main breakthrough in bulk growth was proposed in 2004 by Toyota/Denso[12]. This process, known as *Repeated a-face growth process (RAF),* allows obtaining micropipe free 4H-SiC substrates with a very low density of dislocations. The concept is based on the sequential growth of the substrate along 3 different orientations. It was shown that SiC growth along the a-face reduces significantly the micropipe

density. However, for device fabrication, a c-face grown material provides better electrical results. Consequently, this new process combines both aspects, a first growing perpendicular to the a-face axis and then to the c-face axis, as depicted in Fig. 2.3 [12]. The last growth step is performed on the standard c-face taking profit of the defect free material obtained from the two previous steps. The commercial availability of this novel material at a reasonable cost should definitively boost the SiC devices production. The main remaining question is the industrialization of this process for mass production.

In addition to the continuous improvement of wafer diameter and defect density, several challenges remain in the SiC bulk growth technology. The first one is the absence of highly doped low defects P^+ substrates. These substrates are necessary for several applications such as power IGBTs (Insulated Gate Bipolar Transistors) or IBTs (Insulated Base Transistors)[13]. The second one is the impossibility up to now to obtain low doped N^- substrate, which also have a lot of applications in the fields of power devices and radiation detectors. Another need is the availability of Silicon Carbide on Insulator. Several tentatives have been done to growth by CVD 3C-SiC on Si and SiO_2/Si substrates. The high lattice mismatching between SiC and Si results in highly defective SiC layers. The best solution proposed up to now seems to be the SMARTCUT® technique patented by SOITEC (www.soitec.com). This technology allow to bond 3C or 4H SiC thin layers on different type of substrates such as SiO_2/Si (SiCOI) or even on metallized Si substrates. Moreover, the resulting cost of this technique is lower than the bulk growth of 4H-SiC. The availability of SiCOI wafers is highly desirable for application of MEMS and of high temperature integrated circuits.

Concerning epilayer growth, CVD is the more stable, reliable and extended technique today. The main limitation of CVD is its low growth rate, a few μm per hours, resulting in a high cost of thick (>10 μm) epilayer production. Since many application for power electronics require 3 KV-20 KV voltage rated devices, epilayers with thickness range from 30 μm to 200 μm are needed as starting material. The cost of CVD epi growth results very high in this case. This is why other techniques, such as sublimation are also studied to increases the growth rate of SiC epilayers. Growth rates of 100 μm/hours can be achieved. Sublimation epitaxy also allow a reduction of defect density of the starting substrate. However, the main disadvantage is that this technique is intrinsically more susceptible to chemical contamination than CVD, leading to higher residual doping and compensation phenomena.

2.3. SiC Technology and applications

SiC, as a new semiconductor, the first drawback to overcome towards to its development is the capability to grow large area wafers with controlled doping properties and very low residual defect density. As stated before, by the end of the 70s, a first step has been done towards reaching this objective by means of the development of the modified Lely method, which allows growing boules of SiC larger than 1 inch diameter. This achievement waked up the interest of the microelectronic research community, and technological and device activities on this semiconductor started again. Since then, SiC has demonstrated its great potential as base material for high-power, high-temperature and high-frequency devices over the past recent years. The physical background of this potential lies on its superior material properties (Table II.1). The physical and electronic properties of SiC make it the foremost semiconductor material

for short wavelength optoelectronics, high temperature, radiation resistance, and high-power/high-frequency electronic devices[14,15].

Among others properties its wide bandgap allows the operation of SiC electronic devices at extremely high temperatures without suffering from intrinsic conduction effects. For example, radiation hard high temperature silicon carbide electronics will play a key role in future missions to the hostile environments near the sun and on the surfaces of the inner planets. Long-term operation of probes within Venus's scorching 450 ºC atmosphere will require the use of uncooled silicon carbide electronics. For spacecraft operating near the Sun, silicon carbide electronics would enable significant reductions in spacecraft shielding and heat dissipation hardware, so that more scientific instruments could be included on each vehicle. These achievements could be, of course, eventually used in the conventional (Fig. 2.4) aircraft or automobile industry[8].

SiC can withstand a voltage gradient (or electric field) over eight times greater than Si or GaAs without undergoing avalanche breakdown. This high breakdown electric field enables the fabrication of very high-voltage, high-power devices such as diodes, power transistors, power thyristors and surge suppressors, as well as high power microwave devices. Additionally, it allows the devices to be placed very close together, providing high device packaging density for integrated circuits. SiC is an excellent thermal conductor (SiC possess high thermal conductivity). Heat will flow more readily through SiC than other semiconductor materials. In fact, at room temperature, SiC has a higher thermal conductivity than any metal.
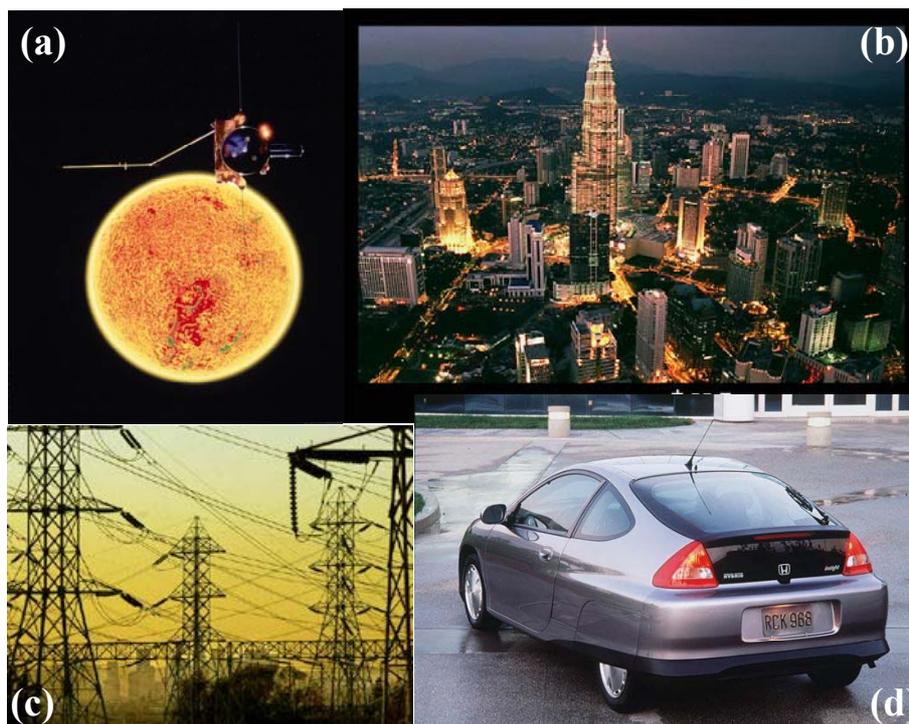
Fig. 2.4. (a) Spacecraft with high temperature, radiation hard SiC electronics will enable challenging missions in both the inner and the outer solar system. (b) SiC is highly suitable for energy saving in public power distribution. (c) The high voltage power lines that currently destroy the beauty of the land killing the birds of prey can be buried under ground. (d) SiC sensors and control on an automobile (electric or hybrid) engine will result in cleaner burning, more fuel efficient cars.

This property enables SiC devices to operate at extremely high power levels and still dissipate the large amounts of excess of heat generated. The high-saturated electron drift velocity explain why SiC devices can operate at high frequencies (RF and microwave) because of the high saturated electron drift velocity of SiC. Power semiconductor devices are a critical element of "smart" power electronics technology. Today, utilities generate on average 20% more electricity than is consumed at any given time. This excess power reserve is needed to ensure that electric service is reliably immune to everyday load changes and component failures that cause electrical glitches throughout the power grid. The incorporation of solid-state "smart" power electronics into the power grid should significantly reduce the power reserve margin necessary for reliable operation, because these semiconductor circuits can detect and instantaneously compensate for local glitches. It has been estimated that a mere 5% reduction in power reserve margin would eliminate the need for $50 billion worth of new power plants within the next 25 years. This same smart power technology would also enable as much as 50% larger power capacities to be carried over existing power lines. Presently, these devices are all implemented in conventional silicon-based semiconductor technology. In short, SiC power devices could standoff higher voltages and respond faster using devices with lower parasitic resistances and physically sizes much smaller than silicon power devices. Faster switching speed not only increases power system conversion efficiency, but it also enables the use of smaller transformers and capacitors to greatly shrink the overall size and weight of the system. Furthermore, the high temperature capability of SiC greatly reduces cooling requirements that are also a substantial portion of the total size and cost of a power conversion and distribution system. SiC devices are therefore expected to drastically improve the distribution and efficient usage of electric power in the 21st century (Fig. 2.4).

	SiC vs Si advantage	Application
Electrical properties	High Electric Field	Power Devices
	Wide Band Gap	HT Electronics & Sensors
		UV & Radiation Detectors
	High carrier saturation velocity	High Frequency (RF devices)
Mechanical Properties	Young Modulus	Mechanical Sensors
	Hardness	Surface Coating
Chemical Properties	Inertness	Chemical Sensors (gas, HT,...)
	Biocompability	Bio-sensors
Thermal Properties	High thermal conductivity	Power Devices

Table II.3. Main SiC advantages and related applications fields.

As well as the paramount importance challenges described below, many types of devices and applications can be covered nowadays by SiC with superior performances than Si. Apart from power devices, which is the main application field of SiC, biomedical sensors (Fig 2.5(a))[16], UV and radiation detectors (Fig 2.5(b))[17,18], MEMS

micro and nano-resonators (Fig 2.5(c)), magnetic and temperature Hall sensors (Fig 2.5(d))[19] and gas sensors[20] are other applications in which SiC can play a major role to improve their current performances. Table II. 3 summarizes the main SiC advantages and the identified application fields where it can be applied.

(a) (b)

(c) (d)
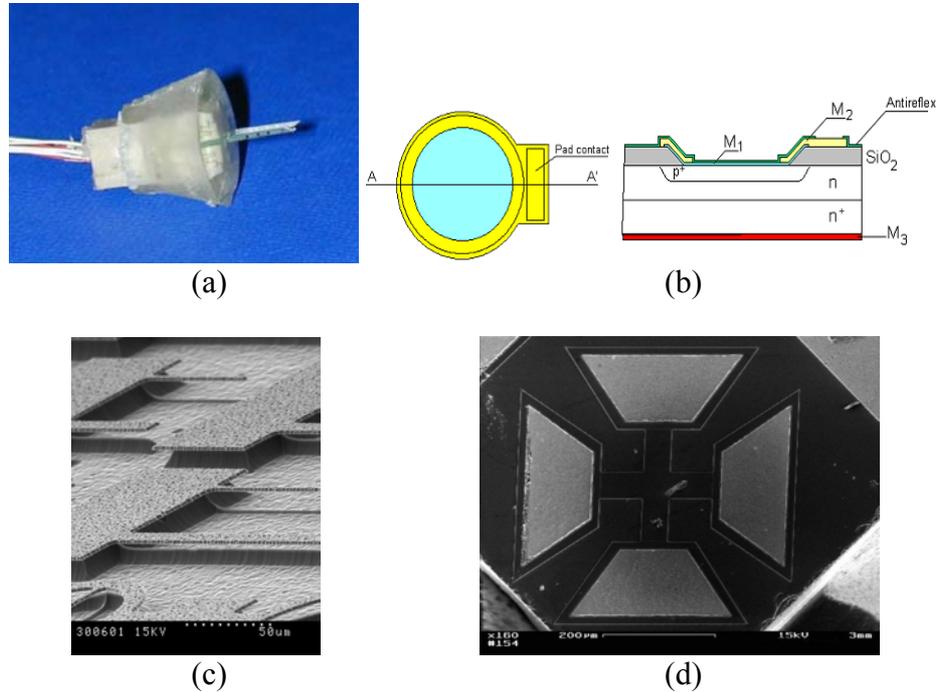
Fig. 2.5. Pictures of SiC devices for different applications. (a) biomedical impedence sensor needle, (b) UV bipolar detector, (c) Micromachined resonator, and (d) Temperature Hall effect sensor. All of them fabricated at the CNM.

2.4. Yes, but … The SiO$_2$/SiC interface problem

SiC is the only compound semiconductor that can be thermally oxidized, as Silicon, to grow insulating, high quality SiO$_2$ layers. These insulating layers are crucial in nearly all the electrical applications described in the last section. However, the high density of imperfections encountered at the SiC/oxide interface represents a major obstacle in the development of functional SiC devices[21,23] (mainly metal-oxide-semiconductor devices). Properties of defects encountered at the oxidized surfaces of Silicon carbide (SiC) suggest their origin to be different from the dangling-bond-type defects (P$_b$-centers) commonly observed in oxidized silicon. After nearly a decade of intensive research efforts in the field of SiC oxidation it remains unclear what factor(s) make the interface between thermal oxides and SiC so dramatically different from the *classic* and highly successful SiO$_2$/Si interface. In this respect, one may notice, for instance that the Si-face [(0001) surface plane] of hexagonal SiC polytypes is structurally isomorphic with the (111)Si surface. It must be stressed that on (111)Si, gate oxides present poorer performances than on the standard (100)Si surface.

However, oxidation of these two surfaces, even after hydrogen passivation treatments, results in interface with densities of electrically active centers different by at least two orders of magnitude, i.e., in the range of 10^{10} cm^{-2} in Si/SiO$_2$ [24] and 10^{12} cm^{-2}

in SiC/SiO$_2$ [25]. The major question, still unanswered, is whether this high density of structural imperfections (leading to the high interface trap denisity, D$_{it}$) is an intrinsic property of the oxidized SiC or not? As yet, there exists no consensus regarding this subject. On the one side, the theoretical results suggest that the topology and geometry of SiC surfaces is not suitable for abrupt interfaces[26,27]. This would make suboxide bonds inevitable, leading to a graded SiC-oxide transition with poor insulating properties. On the other hand, the experimental results reveal a clear trend of gradual improvement of the electrical properties of the SiC/SiO$_2$ interface as better (alternative) procedures are employed for SiC epitaxial layer growth, pre-oxidation surface preparation, oxidation parameters, and post-oxidation treatment[22,23].
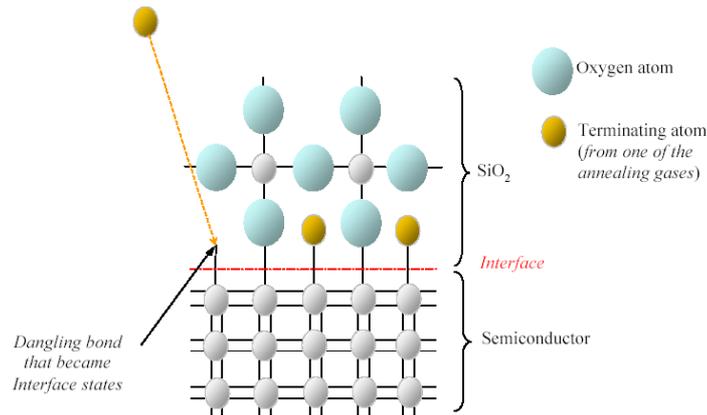
Fig. 2.6. Thermal oxidation of a semiconductor (SiC or Si) showing the formation of dangling bonds at the interface.

Both the donor- and acceptor-type interface states exhibit a wide energy distribution. Such spread is untypical for the Si dangling bond type defects corresponding to three-fold coordinated Si atoms at the (111) plane routinely encountered at the (111)Si/SiO$_2$ interface[28]. The latter exhibit an amphoteric electrical behavior with (-/0) and (0/+) transition D$_{it}$ peaks with a width at half height of 0.2-0.3 eV. Another specific feature of P$_b$-centers is their interaction with hydrogen which results in the formation of electrically inactive Si$_3$≡Si-H entities[29]. This effect, known as passivation is widely used in the Si-MOS technology to attain interfaces with low D$_{it}$. Unfortunately, passivation of the SiC/SiO$_2$ interfaces is observed to occur only after damaging the region by irradiation or charge injection. Basically, this annealing restores the D$_{it}$ observed after oxide growth which is still much higher than in the Si/SiO$_2$ structures[30]. Thus, the effects responsible for this high D$_{it}$ appear to be resistant to hydrogen passivation. These features together with the fact that the process-induced variations of the SiC/SiO$_2$ interface donors and acceptors density may occur in opposite directions, indicate that one cannot ascribe these defect to the class of simple Si dangling bonds centers common for Si/SiO$_2$ interfaces (Fig 2.6). Thus, one must look to alternative atomic models of SiC/SiO$_2$ interface states.

In a search for possible sources of imperfections in SiC/SiO$_2$ entities, it was noticed that a higher D$_{it}$ is systematically encountered on the faces of SiC with a higher density of carbon atoms[25]. In line with this observation it was found that the application of specific anti-carbon surface cleaning steps (UV-ozone exposure) may effectuate a significant reduction in the SiC/SiO$_2$ D$_{it}$[31]. Therefore, excess carbon atoms were suggested to contribute significantly to the SiC/SiO$_2$ interface state density. According

to the "carbon-cluster" model[25] the D_{it} distribution, within the band gap of the semiconductor, can be explained by a combination of the contributions of π-bonded clusters of different size (Fig. 2.7(a)). In a-C:H the highest occupied states correspond to the π-bonds of sp^2-hybridized carbon atoms arranged in clusters of different size. The size of a π-bonded carbon cluster determines both the position of the upper filled electron states and the π-π* splitting which corresponds to the optical bandgap width[32]. Therefore, assuming formation of carbon clusters of different size during oxidation of SiC, they would account for a quasi-continuum D_{it} spectrum. Since the carbon cluster model was proposed, numerous experimental results appeared in the literature which demonstrate the clustering of elemental carbon at the oxidized SiC surfaces and its relationship to the interface states density: The excess carbon at the 6H-SiC/SiO$_2$ interfaces was detected using angle resolved X-ray photoelectron spectroscopy and correlated with D_{it}[33]; Atomic-force microscopy revealed the presence of C-related particles after removing thermal oxide from SiC[34]; Transmission electron microscopy/energy loss spectroscopy also observed carbon-enriched regions at the SiC/SiO$_2$ interfaces[35,36]. Finally, electron spin resonance spectroscopy (ESR) gives most straightforward evidence for paramagnetics centers related to dangling bonds of C atoms in a surrounding similar to that encountered in amorphous carbon[37].
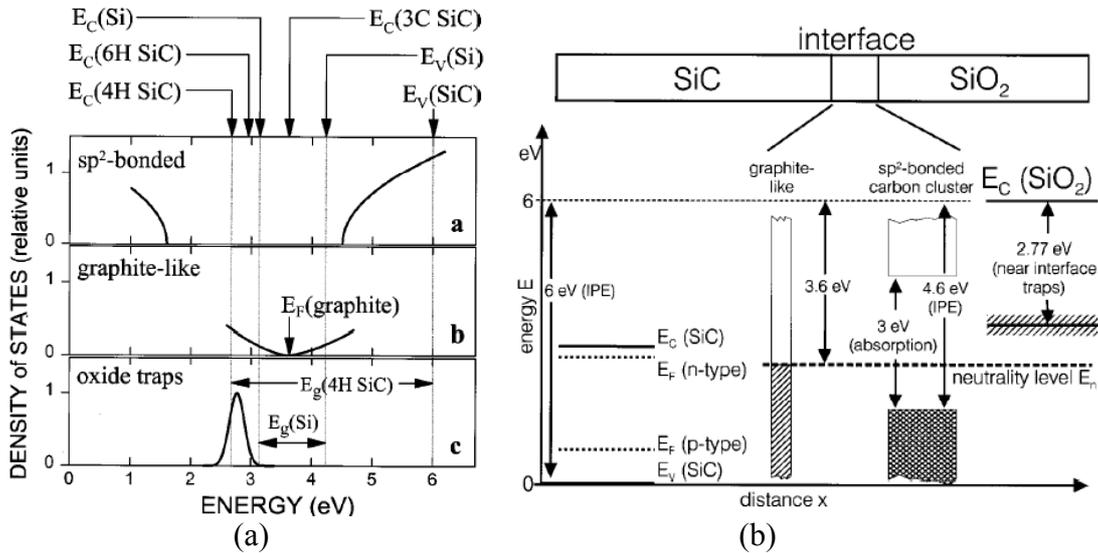
Fig. 2.7. (a) The schematic energy distribution of interface states originating from a) wide energy gap carbon clusters, b) graphite-like carbon clusters and c) near-interfacial oxide defects. (b) The "Carbon Cluster Model" for interface states at SiC/SiO$_2$ MOS structures. The interface states are governed by wide energy gap sp^2-bonded carbon clusters and graphite-like carbon clusters. Near-interface oxide traps are marked at 2.77 eV below the conduction band edge of SiO$_2$. From Ref. [25].

However feasible the carbon cluster model, there is a portion of the SiC/SiO$_2$ spectrum which cannot be immediately ascribed to the presence of carbon clusters[25]: Close to the conduction band of 4H-SiC, D_{it} exceeds 10^{13} cm^{-2}eV^{-1} (according to Hall effect measurement it approaches[38] 10^{14} cm^{-2}eV^{-1}), which is much higher than observed for the donor states of carbon clusters across the SiC bandgap (Fig. 2.7(b)). As a possible explanation, the contribution of intrinsic SiO$_2$ defects, also observed at the Si/SiO$_2$ interface[39], was proposed[25]. This suggestion is corroborated by the observation of an uncorrelated variation in D_{it} in the lower part of the 4H-SiC bandgap and near its

conduction band edge, which points to a different atomic origin of imperfections responsible for these two contributions to D_{it}[25]. Comparative investigations performed both on SiC/SiO$_2$ and Si/SiO$_2$ interfaces suggest that these oxide defects are acceptors characterized by an energy level at ~2.8 eV below the conduction band of SiO$_2$, i.e., close to the conduction band edge of 4H-SiC[39]. Another explanation for the high D_{it} near the conduction band of 4H-SiC may entail in a local polytypic transition form 4H-SiC to the more narrow-gap 3C-SiC polytype[40]. However, the bandgap width of the SiC at the interface with thermal SiO$_2$ keeps corresponding to the initial SiC polytypes[25,41]. Furthermore, no measurable decrease is observed of the 4H-SiC volume fraction at its interface with SiO$_2$ when the oxidation temperature increases from 1000 to 1300 ºC[42]. Therefore, the oxide trap model provides a much better account for the observed properties of SiC/SiO$_2$ interface traps than the 4H → 3C-SiC polytype transition.

2.5. Conclusions

Silicon Carbide (SiC) is a wide band gap semiconductor with specific electrical properties such as a high breakdown electric field, a high thermal conductivity and a high inertness. The material exhibits the phenomenon of poytypism (the existence of geometrically different stacking of the basic structural elements), the most common sequences are 3C, 6H and 4H-SiC. The physical and electronic properties of SiC make it the foremost semiconductor material for short wavelength optoelectronics, high temperature, radiation resistance, and high-power/high-frequency electronic devices. SiC devices possess a very wide range of industrial applications, such as spacecraft, aircraft, automobile, communication or energy distribution, among others.

Impressive progress in SiC processing technology has been carried out in the last decade. Recently, new breakthroughs in the fields of material growth and of technological processes have been reported, which will boost the development of SiC microelectronic devices and its industrial production. The process known as *Repeated a-face* growth, allows obtaining micropipe free SiC substrates with a very low density of dislocations. Nowadays, 4 inches wafers (the minimum wafer diameter to manufacture industrially viable devices) have been demonstrated with high quality and low defects density.

Several technological vital issues still must be overcome to produce commercially SiC based electronics. In particular, insulators capable of reliable high temperature operation with high breakdown field strength and low interface state densities require further investigation. SiC is the only compound semiconductor that can be thermally oxidized, as Silicon, to grow insulating, high quality SiO$_2$ layers. However, the high density of imperfections encountered at the SiC/oxide interface represents a major obstacle in the development of many functional SiC devices.

Properties of defects encountered at the oxidized surfaces of SiC suggest their origin to be different from the dangling-bond-type defects commonly observed in the oxidized Silicon. Excess Carbon atoms were suggested to contribute significantly to the unacceptable high SiC/SiO$_2$ interface state density (D_{it}). However , there is a portion of the SiC/SiO$_2$ spectrum which cannot be immediately ascribed to the presence of carbon clusters: Close to the conduction band of 4H-SiC, D_{it} exceeds 10^{13} cm^{-2}eV^{-1}, which is much higher than the measured value for the donor states of carbon clusters across the SiC bandgap. As a possible explanation, the contribution of intrinsic SiO$_2$ defects was proposed, also observed at the Si/SiO$_2$ interface.

References

[1] Y. Goldberg, M. E. Levinshtein, S. L. Rumyantsev, *Properties of Advanced Semiconductor Materials GaN, AlN, SiC, BN, SiC, SiGe*. John Wiley & Sons, Inc., New York, (2001).

[2] G. L. Harriss (Editor), *Properties of Silicon Carbide*, EMIS Datareviews Series No. 13, Institution of Electrical Engineers, London, U.K., (1995).

[3] R. C. Marshall, Jr, and C. E. Ryan (Editors), *Silicon Carbide*, University of South Carolina, Columbia, SC, USA, (1974).

[4] H. Matsunami, *Physica B* **185**, 65, (1993).

[5] P. A. Ivanov, and V. E. Chelnokov, *Semicond. Sci. Technol.* **7**, 863, (1992).

[6] Y. P. Tsividis, *Operation and modeling of the MOS transistor*, McGraw-Hill in Electrical Engineering, (1987).

[7] B. J. Baliga, *IEEE Electron Device Lett.* **10**, 455, (1989).

[8] NASA Silicon Carbide Electronics, http://www.grc.nasa.gov/www/SiC/index.html

[9] Y. M. Tairov, and V. F. Tsvetkov, *J. Cryst. Growth*, **43**, 209, (1978).

[10] A. Ellison, B. Magnusson, N. T. Son, L. Storasta, and E. Janzén, *Mater. Sci. Forum,* **433-436**, 33 (2003).

[11] H. Nagasawa, K. Yagi, T. Kawahara, and N. Hatta, *Mater. Sci. Forum,* **433-436**, 3 (2003).

[12] D. Nakamura, I. Gunjishima, S. Yamaguchi, T. Ito, A. Okamoto, H. Kondo, S. Onda, and K. Takatori, *Nature,* **430**, 1009, (2004).

[13] P. Godignon, J. Fernández, D. Flores, S. Hidalgo, J. Rebollo, J. Millán, and J. P. Chante, *Solid State Electron.,* **39**, 1777 (1996).

[14] CREE SiC Substrates and Epitaxy, http://www.cree.com/products/sic_index.asp

[15] A. R. Powell, and L. B. Rowland, *Proceedings of the IEEE* **90**, 942, (2002).

[16] J. Pascual, F. Valvo, P. Godignon, J. Aguiló, J. Millán, J. Camassel and N. Mestres, *Mater. Sci. Forum,* **457-460**, 1483, (2004).

[17] G. Brezeanu, P. Godignon, E. Dimitrova, C. Raynaud, D. Planson, A. Mihaila, F. Udrea, J. Millán, G. Amaratunga, and C. Boianceanu, *Mater. Sci. Forum* **457-460**, 1495, (2004).

[18] G. Bertuccio, S. Binetti, S. Caccia, R. Casiraghi, A. Castaldini, A. Cavallini, C. Lanzieri, *Mater. Sci. Forum* **483-485**, 1015, (2005).

[19] J.L. Robert, S. Contreras, J. Camassel, J. Pernot, S. Juillaguet, L. DiCioccio, T. Billon, *Mater. Sci. Forum* **389-393**, 1435, (2002).

[20] A. Baranzahi, *High Temperature Solid State Gas Sensors Based on Silicon Carbide*, PhD Thesis dissertation, Department of Physics and Measurements Technology, Linköping University, Sweden, 1996.

[21] M. R. Melloch, and J.A. Cooper, Jr., *MRS Bull.*, **22**, 42, (1997).

[22] H. Matsunami, *Mater. Sci. Forum,* **389-393**, 3, (2002).

[23] J.A. Cooper, Jr., *Mater. Sci. Forum,* **389-393**, 15, (2002).

[24] See, e.g., Y. C. Cheng, *Progr. Surf. Sci.,* **8**, 181, (1977).

[25] V. V. Afanas'ev, M. Bassler, G. Pensl, and M. Schulz, , *Phys. Stat. Sol. (a)* **162**, 321-337, (1997).

[26] M. Di Ventra, and S. T. Pantelides, *Phys. Rev. Lett.,* **83**, 1624, (1999).

[27] R. Buczko, S. J. Pennycook, and S. T. Pantelides, , *Phys. Rev. Lett.,* **84**, 943, (2000).

[28] E. H. Poindexter, *Semicond. Sci. Technol.,* **4**, 961, (1989).

[29] A. L. Stesmans, *Defects in SiO₂ related dielectrics: Science and Technology*, NATO ASI Series II (2), Kluwer, Dordrecht, (2000).

[30] J. Campi, Y. Shi, Y. Luo, F. Yan, and J. H. Zhao, *IEEE Trans. Electron Devices,* **46**, 511 (1999).

[31] V. V. Afanas'ev, A. Stesmans, M. Bassler, G. Pensl, M. J. Schulz, and C. I. Harris, *Appl. Phys. Lett.* **68**, 2141, (1996).

[32] J. Robertson, *Adv. Phys.,* **35**, 317, (1984).

[33] V. K. Vathuya, D. N. Wang, and M. H. White, *Appl. Phys. Lett.,* **73**, 2161 (1998).

[34] V. V. Afanas'ev, A. Stesmans, and C. I. Harris, *Mater. Sci. Forum* **264-268**, 857, (1998).

[35] K. C. Chang, T. Nuhfer, L. M. Porter, and Q. Wahab, *Appl. Phys. Lett.,* **77**, 2186, (2000).

[36] K. C. Chang, L. M. Porter, J. Bentley, C.Y. Lu, and J. Cooper, Jr., *J. Appl. Phys.* **95**, 8252, (2004).

[37] V. V. Afanas'ev, A. Stesmans, and M. O. Adersson, *Phys. Rev. B,* **54**, 10820, (1996).

[38] N. S. Saks, S. S. Mani, and A. K. Agarwal, *Appl. Phys. Lett.,* **76**, 2250, (2000).

[39] V. V. Afanas'ev, and A. Stesmans, *Phys. Rev. Lett.,* **78**, 2437, (1997).

[40] R. S. Okojie, M. Xhang, P. Pirouz, S. Tumakha, G. Jessen, and L. J. Brillson, *Appl. Phys. Lett.* **79**, 3056, (2001).

[41] V. V. Afanas'ev, F. Ciobanu, S. Dimitrijev, G. Pensl, and A. Stesmans, *J. Phys. Condens. Matter,* **16**, S1839, (2004).

[42] V. V. Afanas'ev, and A. Stesmans, *Mater. Sci Eng. B.,* **102**, 308, (2003).

Chapter III

Characterization methods of metal-insulator-semiconductor structures

The study of the properties of insulators as gate oxide on a semiconductor is mainly performed on stacked structures composed of an oxide sandwiched between a metal and a semiconductor, the metal-insulator-semiconductor (MIS) structure. The characterization of the bulk insulator and interfacial properties are usually performed with a combination of several physical and electrical characterization methods. In this chapter, we will make a brief description of the various characterization tools used during this thesis. This chapter does not aim at detail the theoretical aspects of each method, but only to stress the principle, the implementation and the principal information which one can obtain. In the first section, the physical characterization methods will be presented. The physical characterization methods are addressed to establish the composition, the thickness or the morphology of the insulator layers. In the next section, the electrical characterization methods will be detailed (measurements of capacity and current). The electrical methods are used to evaluate the insulator properties, as well as the quality of the insulator/semiconductor interface, among others.

3.1. Physical characterization methods

The physical characterization carried out during this thesis has been performed through collaboration with different laboratories. *AFM* and *XRD* experiments have been performed in the Institut de Ciència de Materials de Barcelona. *SEM* and *EDX* measurements have been carried out in the Serveis de Microscopia Electrònica (UAB). *SIMS* measurements were made for PROBION and the INSA of Lyon in France. *TEM* and *EDX* measurements have been investigated in a collaboration with the Department of Physics of the Aristotele University of Thessaloniki (Greece) and the Centre de Recherche sur l'Hétéroépitaxie et ses Applications of Antipolis (France).

3.1.1. AFM: Atomic Force Microscope

- Description of Technique

Atomic Force Microscopy[1,2] (AFM) is a form of scanning probe microscopy (SPM) where a small probe is scanned across the sample to obtain information about the sample's surface. The information gathered from the probe's interaction with the surface can be as simple as physical topography or as diverse as measurements of the material's physical, magnetic, or chemical properties. These data are collected as the probe is scanned in a raster pattern across the sample to form a map of the measured property relative to the X-Y position. Thus, the AFM microscopic image shows the variation in the measured property, e.g., height or magnetic domains, over the area imaged.
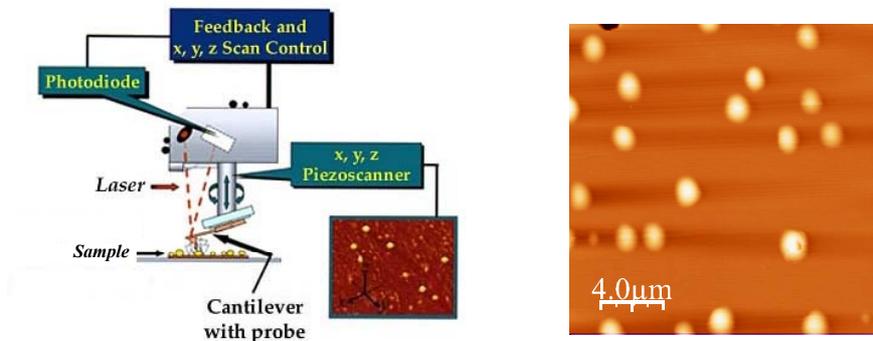
Fig. 3.1. The AFM instrument configuration, and the surface profile of an oxidized Ta_2Si layer on SiC.

The AFM probe has a very sharp tip, often less than 100 Å diameter, at the end of a small cantilever beam. The probe is attached to a piezoelectric scanner tube, which scans the probe across a selected area of the sample surface. Interatomic forces between the probe tip and the sample surface cause the cantilever to deflect as the sample's surface topography (or other properties) changes. A laser light reflected from the back of the cantilever measures the deflection of the cantilever. This information is fed back to a computer, which generates a map of topography and/or other properties of interest. Areas as large as about 100 μm square to less than 100 nm square can be imaged.

- Analytical Information

Contact Mode AFM - The AFM probe is scanned at a constant force between the probe and the sample surface to obtain a 3D topographical map. When the probe cantilever is deflected by topographical changes, the scanner adjusts the probe position to restore the original cantilever deflection. The scanner position information is used to create a topographical image. Lateral resolution of <1 nm and height resolution of <1 Å can be obtained.

Intermittent Contact (Tapping Mode) AFM - In this mode, the probe cantilever is oscillated at or near its resonant frequency. The oscillating probe tip is then scanned at a height where it barely touches or "taps" the sample surface. The system monitors the probe position and vibrational amplitude to obtain topographical and other property

information. Accurate topographical information can be obtained even for very fragile surfaces. Optimum resolution is about 50 Å lateral and <1 Å height. Images for phase detection mode, magnetic domains, and local electric fields are also obtained in this mode.

Lateral Force Microscopy – This mode measures the lateral deflection of the probe cantilever as the tip is scanned across the sample in contact mode. Changes in lateral deflection represent relative frictional forces between the probe tip and the sample surface.

Phase Detection Microscopy - With the system operating in Tapping mode, the cantilever oscillation is damped by interaction with the sample surface. The phase lag between the drive signal and actual cantilever oscillation is monitored. Changes in the phase lag indicate variations in the surface properties, such as viscoelasticity or mechanical properties. A phase image, typically collected simultaneously with a topographical image, maps the local changes in material's physical or mechanical properties.

Magnetic Force Microscopy - This mode images local variations in the magnetic forces at the sample's surface. The probe tip is coated with a thin film of ferromagnetic material that will react to the magnetic domains on the sample surface. The magnetic forces between the tip and the sample are measured by monitoring cantilever deflection while the probe is scanned at a constant height above the surface. A map of the forces shows the sample's natural or applied magnetic domain structure.

Image Analysis - Since the images are collected in digital format, a wide variety of image manipulations are available for AFM data. Quantitative topographical information, such as lateral spacing, step height, and surface roughness are readily obtained. Images can be presented as two-dimensional or three-dimensional representations in hard copy or as digital image files for electronic transfer and publication.

Nanoindentation - A specialized probe tip is forced into the sample surface to obtain a measure of the material's mechanical properties in regions as small as a few nanometers.

- Typical Applications

• 3-dimensional topography of IC device
• Roughness measurements for chemical mechanical polishing
• Analysis of microscopic phase distribution in polymers
• Mechanical and physical property measurements for thin films
• Imaging magnetic domains on digital storage media
• Imaging of submicron phases in metals
• Defect imaging in IC failure analysis
• Microscopic imaging of fragile biological samples
• Metrology for compact disk stampers

- Use in this thesis

AFM has been routinely used for the surface topography analysis of the dielectrics grown or deposited on SiC. The main analytical parameter extracted is the surface roughness, accounted by the roughness mean square value (RMS).

3.1.2. EDX: Energy Dispersive X-Ray Analysis

- Description of Technique

Energy Dispersive X-Ray Spectroscopy[1,3,4] (EDX or EDS) is a chemical microanalysis technique used usually in conjunction with scanning electron microscopy (SEM) or transmission electron microscopy (TEM). The EDX technique detects x-rays emitted from the sample during bombardment by an electron beam to characterize the elemental composition of the analyzed volume. Features or phases as small as 1 µm or less can be analyzed.

When the sample is bombarded by the SEM's electron beam, electrons are ejected from the atoms comprising the sample's surface. The resulting electron vacancies are filled by electrons from a higher state, and an x-ray is emitted to balance the energy difference between the two electrons' states. The x-ray energy is characteristic of the element from which it was emitted.
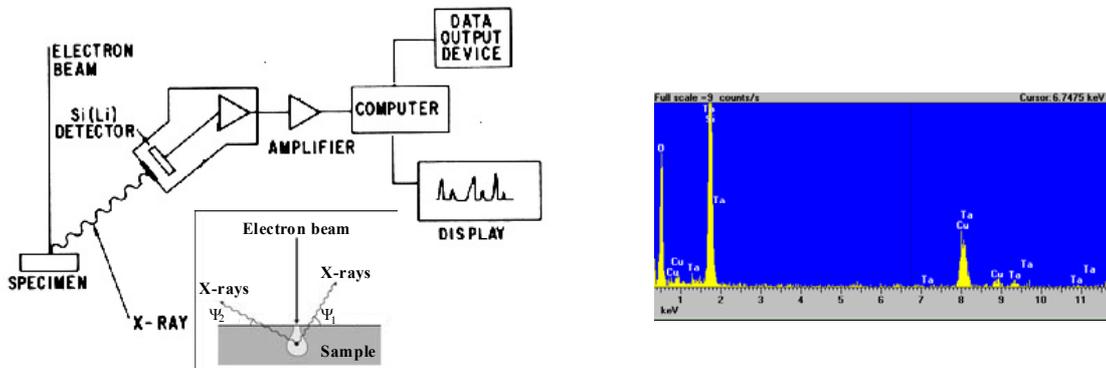
Fig. 3.2. Schematic presentation of a EDX System and the EDX graph of an oxidized Ta_2Si layer on SiC.

The EDX x-ray detector measures the relative abundance of emitted x-rays versus their energy. The detector is typically a lithium-drifted silicon, solid-state device. When an incident x-ray strikes the detector, it creates a charge pulse that is proportional to the energy of the x-ray. The charge pulse is converted to a voltage pulse (which remains proportional to the x-ray energy) by a charge-sensitive preamplifier. The signal is then sent to a multichannel analyzer where the pulses are sorted by voltage. The energy, as determined from the voltage measurement, for each incident x-ray is sent to a computer for display and further data evaluation. The spectrum of x-ray energy versus counts is evaluated to determine the elemental composition of the sampled volume.

- Analytical Information

Qualitative Analysis - The sample x-ray energy values from the EDX spectrum are compared with known characteristic x-ray energy values to determine the presence of an element in the sample. Elements with atomic numbers ranging from that of beryllium to uranium can be detected. The minimum detection limits vary from approximately 0.1 to a few atom percent, depending on the element and the sample matrix.

Quantitative Analysis – Quantitative results can be obtained from the relative x-ray counts at the characteristic energy levels for the sample constituents. Semi-quantitative results are readily available without standards by using mathematical corrections based on the analysis parameters and the sample composition. The accuracy of standardless analysis depends on the sample composition. Greater accuracy is obtained using known standards with similar structure and composition to that of the unknown sample.

Elemental Mapping - Characteristic x-ray intensity is measured relative to lateral position on the sample. Variations in x-ray intensity at any characteristic energy value indicate the relative concentration for the applicable element across the surface. One or more maps are recorded simultaneously using image brightness intensity as a function of the local relative concentration of the element(s) present. About 1 μm lateral resolution is possible.

Line Profile Analysis - The SEM electron beam is scanned along a preselected line across the sample while x-rays are detected for discrete positions along the line. Analysis of the x-ray energy spectrum at each position provides plots of the relative elemental concentration for each element versus position along the line.

- Typical Applications

  • Foreign material analysis
  • Corrosion evaluation
  • Coating composition analysis
  • Rapid material alloy identification
  • Small component material analysis
  • Phase identification and distribution

- Use in this thesis

Energy dispersive x-ray spectroscopy has been used in the investigation of the composition of the oxidized Ta_2Si layer on Si and on SiC substrates (*Chapter VI*). EDX measurements have been carried out along with SEM in the analysis of Tanalum pentoxide peaks located on the surface or using TEM in the cross-sectional investigation.

3.1.3. RBS: Rutherford Backscattering Spectrometry

- Description of Technique

Rutherford Backscattering[5-7] (RBS) is based on collisions between atomic nuclei and derives its name from Lord Ernest Rutherford, who in 1911 was the first to present the concept of atoms having nuclei. It involves measuring the number and energy of ions in a beam which backscatter after colliding with atoms in the near-surface region of a sample at which the beam has been targeted. With this information, it is possible to determine atomic mass and elemental concentrations versus depth below the surface. RBS is ideally suited for determining the concentration of trace elements heavier than the major constituents of the substrate. Its sensitivity for light masses, and for the makeup of samples well below the surface, is poor.

When a sample is bombarded with a beam of high energy particles, the vast majority of particles are implanted into the material and do not escape. This is because the diameter of an atomic nucleus is on the order of 10^{-15} m while the spacing between nuclei is on the order of 2×10^{-10} m. A small fraction of the incident particles do undergo a direct collision with a nucleus of one of the atoms in the upper few micrometers of the sample. This "collision" does not actually involve direct contact between the projectile ion and target atom. Energy exchange occurs because of Coulombic forces between nuclei in close proximity to each other. However, the interaction can be modeled accurately as an elastic collision using classical physics.
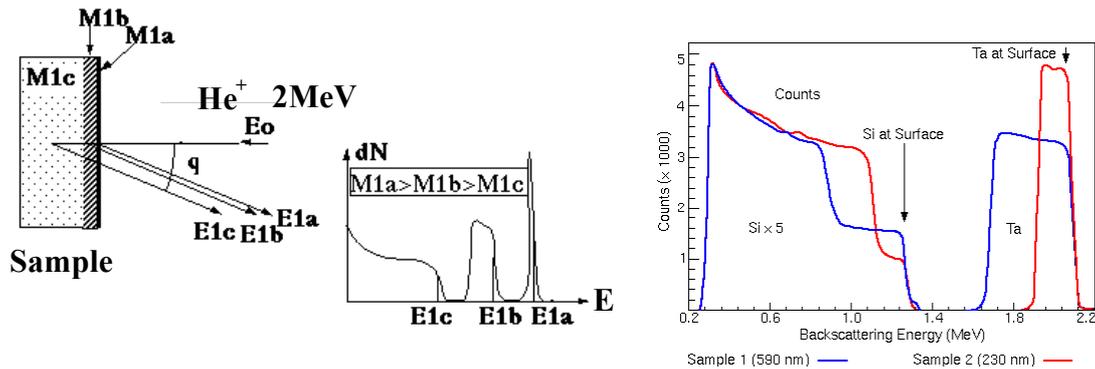
Fig. 3.3. Schematic representation of the RBS principle and the backscattering energy graph of a deposited TaSi$_2$ layer on Si.

The energy measured for a particle backscattering at a given angle depends upon two processes. Particles lose energy while they pass through the sample, both before and after a collision. The amount of energy lost is dependent on that material's stopping power. A particle will also lose energy as the result of the collision itself. The collisional lost depends on the masses of the projectile the target atoms. The ratio of the energy of the projectile before and after collision is called the kinematic factor.

The number of backscattering events that occur from a given element in a sample depends upon two factors: the concentration of the element and the effective size of its nucleus. The probability that a material will cause a collision is called its scattering cross section.

- Analytical Information

Rutherford Backscattering Spectrometry (RBS) is used to bombard a sample with very high energy helium ions, and measure the yield and energy of backscattered helium. RBS is an energy spectrometry of MeV He$^+$ ions, elastically scattered by nuclei of the analytical sample, providing quantitative elemental depth profiling of multi-component surface layers to a depth of 1 μm or more.

Typically RBS is used not only to determine thin film thickness and composition as a function of depth, but also to determine lattice disorder and location of lattice impurities. In addition, RBS provides concentration as well as depth distribution of hydrogen in thin films.

- Typical Applications

Typical RBS applications include:

• Absolute thickness of films, coatings and surface layers (in atoms/cm^2)
• Surface/interface contaminant detection (oxide layers, adsorbates, etc)
• Interdiffusion kinetics of thin films (metals, silicides, etc)
• Elemental composition of complex materials (phase identification, alloy films, oxides, ceramics, glassy carbon, etc)
• Quantitative dopant profiles in semiconductors
• Process control monitoring - composition, contaminants
• Catalytic surface dynamics

▪ Use in this thesis

RBS has been used in the Ta$_2$Si deposition study (*Chapter VI*). Rutherford backscattering spectrometry measurement on deposited Ta$_2$Si films on top SiC give a composition very close to stoichiometry.

3.1.4. SEM: Scanning Electron Microscope

▪ Description of Technique

Scanning electron microscopy[1,8-10] (SEM) is a method for high-resolution imaging of surfaces. The SEM uses electrons for imaging, much as a light microscope uses visible light. The advantages of SEM over light microscopy include much higher magnification (>100,000X) and greater depth of field up to 100 times that of light microscopy. Qualitative and quantitative chemical analysis information is also obtained using an energy dispersive x-ray spectrometer (EDS) with the SEM.
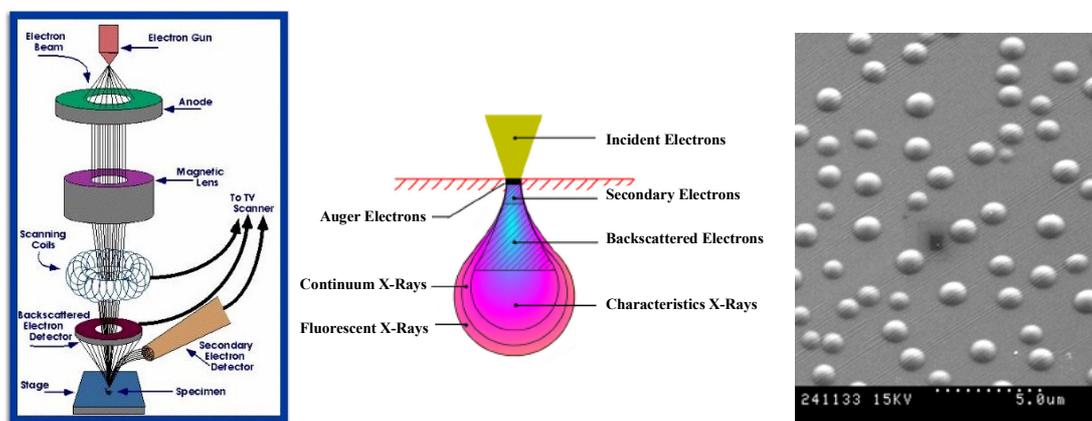
Fig. 3.4. Schematic cross-section of the SEM apparatus, the electron beam interaction diagram and a SEM image of an oxidized Ta$_2$Si layer on SiC.

The SEM generates a beam of incident electrons in an electron column above the sample chamber. The electrons are produced by a thermal emission source, such as a heated tungsten filament, or by a field emission cathode. The energy of the incident electrons can be as low as 100 eV or as high as 30 keV depending on the evaluation objectives. The electrons are focused into a small beam by a series of electromagnetic lenses in the SEM column. Scanning coils near the end of the column direct and position the focused beam onto the sample surface. The electron beam is scanned in a raster pattern over the surface for imaging. The beam can also be focused at a single

point or scanned along a line for x-ray analysis. The beam can be focused to a final probe diameter as small as about 10 Å.

The incident electrons cause electrons to be emitted from the sample due to elastic and inelastic scattering events within the sample's surface and near-surface material. High-energy electrons that are ejected by an elastic collision of an incident electron, typically with a sample atom's nucleus, are referred to as backscattered electrons. The energy of backscattered electrons will be comparable to that of the incident electrons. Emitted lower-energy electrons resulting from inelastic scattering are called secondary electrons. Secondary electrons can be formed by collisions with the nucleus where substantial energy loss occurs or by the ejection of loosely bound electrons from the sample atoms. The energy of secondary electrons is typically 50 eV or less.

To create a SEM image, the incident electron beam is scanned in a raster pattern across the sample's surface. The emitted electrons are detected for each position in the scanned area by an electron detector. The intensity of the emitted electron signal is displayed as brightness on a cathode ray tube (CRT). By synchronizing the CRT scan to that of the scan of the incident electron beam, the CRT display represents the morphology of the sample surface area scanned by the beam. Magnification of the CRT image is the ratio of the image display size to the sample area scanned by the electron beam.

Two electron detector types are predominantly used for SEM imaging. Scintillator type detectors (Everhart-Thornley) are used for secondary electron imaging. This detector is charged with a positive voltage to attract electrons to the detector for improved signal to noise ratio. Detectors for backscattered electrons can be scintillator types or a solid-state detector.

The SEM column and sample chamber are at a moderate vacuum to allow the electrons to travel freely from the electron beam source to the sample and then to the detectors. High-resolution imaging is done with the chamber at higher vacuum, typically from 10^{-5} to 10^{-7} Torr. Imaging of nonconductive, volatile, and vacuum-sensitive samples can be performed at higher pressures.

- Analytical Information

Secondary Electron Imaging - This mode provides high-resolution imaging of fine surface morphology. Inelastic electron scattering caused by the interaction between the sample's electrons and the incident electrons results in the emission of low-energy electrons from near the sample's surface. The topography of surface features influences the number of electrons that reach the secondary electron detector from any point on the scanned surface. This local variation in electron intensity creates the image contrast that reveals the surface morphology. The secondary electron image resolution for an ideal sample is about 3.5 nm for a tungsten-filament electron source SEM or 1.5 nm for field emission SEM.

Backscatter Electron Imaging - This mode provides image contrast as a function of elemental composition, as well as, surface topography. Backscattered electrons are produced by the elastic interactions between the sample and the incident electron beam. These high-energy electrons can escape from much deeper than secondary electrons, so surface topography is not as accurately resolved as for secondary electron imaging. The production efficiency for backscattered electrons is proportional to the sample material's mean atomic number, which results in image contrast as a function of composition, i.e., higher atomic number material appears brighter than low atomic number material in a

backscattered electron image. The optimum resolution for backscattered electron imaging is about 5.5 nm.

Variable Pressure SEM - Traditionally, SEM has required an electrically-conductive sample or continuous conductive surface film to allow incident electrons to be conducted away from the sample surface to ground. If electrons accumulate on a nonconductive surface, the charge buildup causes a divergence of the electron beam and degrades the SEM image. In variable-pressure SEM, some air is allowed into the sample chamber, and the interaction between the electron beam and the air molecules creates a cloud of positive ions around the electron beam. These ions will neutralize the negative charge from electrons collecting on the surface of a nonconductive material. SEM imaging can be performed on a nonconductive sample when the chamber pressure is maintained at a level where most of the electrons reach the sample surface, but there are enough gas molecules to ionize and neutralize charging. Variable pressure SEM is also valuable for examination of samples that are not compatible with high vacuum.

▪ Typical Applications

• Microscopic feature measurement
• Fracture characterization
• Microstructure studies
• Thin coating evaluations
• Surface contamination examination
• IC failure analysis

▪ Use in this thesis

SEM images (Secondary Electron Imaging) has been used as a complement of AFM images in the topography evaluation of insulators on SiC, specially in samples composed of oxidized Ta_2Si (*Chapter VI*). EDX measurements have been performed in these samples using the TEM facilities.

3.1.5. SIMS: Secondary Ion Mass Spectroscopy

▪ Description of Technique

Time of Flight Secondary Ion Mass Spectrometry[1,11-13] (ToF-SIMS) is an analytical technique used to obtain elemental and molecular chemical data about surfaces (static SIMS), and detect parts per billion concentrations of impurities in semiconductors and metals (dynamic SIMS). All elements, including hydrogen, are detectable by SIMS. In ToF-SIMS analysis, the sample is placed in an ultrahigh vacuum environment where primary ions bombard the sample and sputter atoms, molecules, and molecular fragments from the sample surface. The mass of the ejected particles (i.e., secondary ions) are analyzed via time-of-flight mass spectrometry. In the ToF analyzer, ejected ions are accelerated into the analyzer with a common energy, but at different velocities depending on the particle mass. Due to the differences in these velocities, smaller ions move through the analyzer faster than the larger ions. The mass of the secondary ions are determined by their travel time through the analyzer. SIMS is a surface-sensitive analysis method, since only the secondary ions generated in the outermost 10 to 20 Å

region of a sample surface can overcome the surface binding energy and escape the sample surface for detection and analysis.
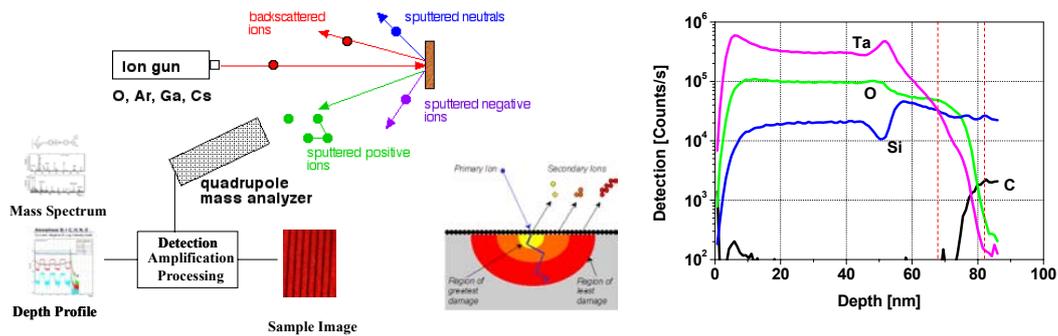
Fig. 3.5. The SIMS instrument configuration (showing the damage on the sample surface), and a depth profile of an oxidized Ta$_2$Si layer on SiC.

▪ Analytical Information

Mass Spectrum - SIMS analysis identifies the elemental and ion composition of the uppermost 10 to 20 Å of the analyzed surface from positive and negative mass spectra. The high resolution of the ToF analyzer can distinguish species whose masses differ by only a few millimass units.

Depth Profile - During SIMS analysis, the sample surface is slowly sputtered away. Continuous analysis obtains composition information as a function of depth. Depth resolution of a few angstroms is possible. High-sensitivity mass spectra can be recorded or reconstructed at any depth of the profile.

Secondary Ion Mapping - A SIMS map measures the lateral distribution of elements and molecules on the sample's surface. To obtain a SIMS map, a highly focused primary ion beam is scanned in a raster pattern across the sample surface, and the secondary ions are analyzed at specific points on a grid pattern over the selected surface area. Image brightness at each point is a function of the relative concentration of the mapped element or molecule. Lateral resolution is less than 0.1 μm for elements and about 0.5 μm for large molecules.

▪ Typical Applications

• Identifying lubricants on magnetic hard discs
• Measuring dopant distributions in semiconductors
• Profiling thickness of insulating films on glass
• Mapping elemental and molecular patterned surfaces
• Identifying compounds in thin organic films
• Determining the extent of crosslinking in polymers

▪ Use in this thesis

Depth profile SIMS analysis have been used for the composition determination, the thickness and dielectric constant evaluation of different gate oxides throughout the thesis. SiC substrate impurity concentration has also been extracted with this technique.

3.1.6. TEM: Transmission Electron Microscopy

- Description of Technique

Transmission electron microscopy[10,14,15] (TEM) is an imaging technique whereby a beam of electrons is focused onto a specimen causing an enlarged version to appear on a fluorescent screen or layer of photographic film (see electron microscope), or can be detected by a CCD camera. In the past, light microscopes have been used mostly for imaging due to their relative ease of use. However, the maximum resolution that one can image is determined by the wavelength of the photons that are being used to probe the sample; nothing smaller than the wavelength being used can be resolved.
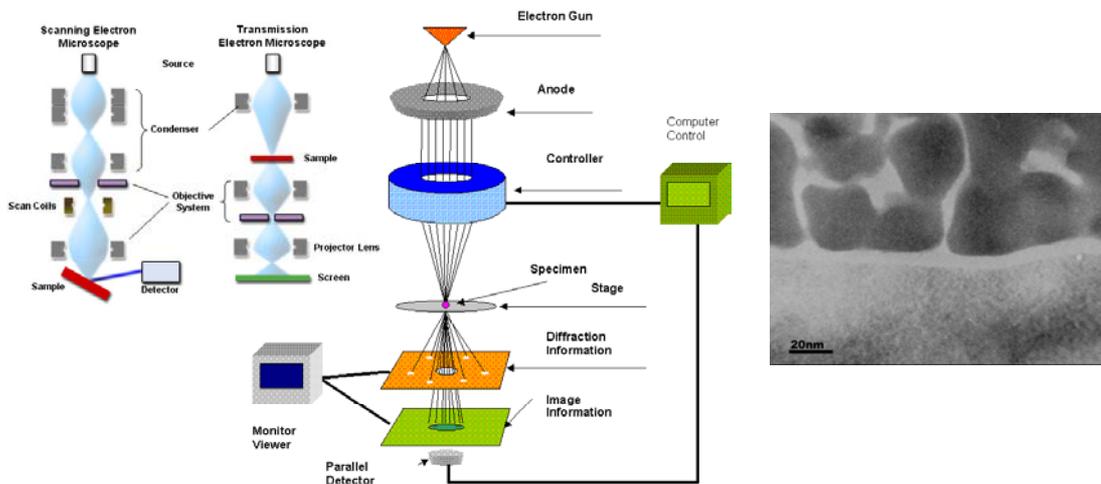
Fig. 3.6. Schematic cross-section of the TEM apparatus comparing its configuration with the SEM, and a cross-sectional TEM image of an oxidized Ta_2Si layer on SiC.

Visible light has wavelengths of 400-700 nanometers; larger than many objects of interest. Ultraviolet could be used, but soon runs into problems of absorption. Even shorter wavelengths, such as x-rays, exhibit a lack of interaction: both in focusing (nothing interacts strongly enough to act as a lens) and actually interacting with the sample. Like all matter, electrons have both wave and particle properties, and their wave-like properties mean that a beam of electrons can in some circumstances be made to behave like a beam of radiation. The wavelength is dependent on their energy, and so can be tuned by adjustment of accelerating fields, and can be much smaller than that of light, yet they can still interact with the sample due to their electrical charge. Electrons are generated by a process known as thermionic discharge in the same manner as the at the cathode in a cathode ray tube, or by field emission; they are then accelerated by an electric field and focused by electrical and magnetic fields on to the sample. The electrons can be focused onto the sample providing a resolution far better than is possible with light microscopes, and with improved depth of vision. Details of a sample can be enhanced in light microscopy by the use of stains; similarly with electron microscopy, compounds of heavy metals such as lead or uranium can be used to selectively deposit heavy atoms in the sample and enhance structural detail, the dense electron clouds of the heavy atoms interacting strongly with the electron beam. The electrons can be detected using a photographic film, or fluorescent screen among other technologies. An additional class of these instruments is the electron cryomicroscope,

which includes a specimen stage capable of maintaining the specimen at liquid nitrogen or liquid helium temperatures. This allows imaging specimens prepared in vitreous ice, the preferred preparation technique for imaging individual molecules or macromolecular assemblies. In analytical TEMs the elemental composition of the specimen can be determined by analyzing its x-ray spectrum or the energy-loss spectrum of the transmitted electrons.

- Analytical Information

In a conventional transmission electron microscope, a thin specimen is irradiated with an electron beam of uniform current density. Electrons are emitted from the electron gun and illuminate the specimen through a two or three stage condenser lens system. Objective lens provides the formation of either image or diffraction pattern of the specimen. The electron intensity distribution behind the specimen is magnified with a three or four stage lens system and viewed on a fluorescent screen. The image can be recorded by direct exposure of a photographic emulsion or an image plate or digitally by a CCD camera. The acceleration voltage of up to date routine instruments is 120 to 200 kV. Medium-voltage instruments work at 200-500 kV to provide a better transmission and resolution, and in high voltage electron microscopy (HVEM) the acceleration voltage is in the range 500 kV to 3 MV. Acceleration voltage determines the velocity, wavelength and hence the resolution (ability to distinguish the neighboring microstructural features) of the microscope.

Diffraction - Electrons of 0.072 Å wavelength at 100 kV excitation transmitted through about 0.1 μm thin foil specimen are diffracted according to Bragg's law, $n\lambda = 2d\,Sin\theta$, forming a diffraction pattern on the display screen of the microscope. Although the real diffraction phenomena is due to complex interactions of charged electrons with the periodic potential field of the lattice, Bragg's Law or Laue Conditions are sufficient approximations for usual practical applications. A diffraction pattern is, in the simplest sense, a Fourier transform of the periodic crystal lattice, giving us information on the periodicities in the lattice, and hence the atomic positions.

Imaging - The image of the specimen in conventional microscopy, on the other hand, is formed selectively allowing only the transmitted beam (Bright Field Imaging) or one of the diffracted beams (Dark Field Imaging) down to the microscope column by means of an aperture. The origin of the image contrast is the variation of intensities of transmitted and diffracted beams due to the differences in diffraction conditions depending on the microstructural features on the electron path.

- Typical Applications

The TEM is used heavily in both material science/metallurgy and the biological sciences. In both cases the specimens must be very thin and able to withstand the high vacuum present inside the instrument. Typical biological applications include tomographic reconstructions of small cells or thin sections of larger cells and 3-D reconstructions of individual molecules via Single Particle Reconstruction. In material science/metallurgy the specimens tend to be naturally resistant to vacuum, but must be prepared as a thin foil, or etched so some portion of the specimen is thin enough for the beam to penetrate.

The contrast in a TEM image is not like the contrast in a light microscope image. A crystalline material interacts with the electron beam mostly by diffraction rather than absorption. If the planes of atoms in a crystal are aligned at certain angles to the electron beam, the beam is transmitted strongly; while at other angles, the beam is diffracted, sending electrons in another direction. In the TEM, the specimen holder allows the user to rotate the specimen to any angle in order to establish the desired diffraction conditions; while an aperture placed below the specimen allows the user to select electrons diffracted in a particular direction. The resulting image shows diffraction contrast, which highlights faults in the crystal structure very clearly. This is very important in materials science. Faults in crystals affect both the mechanical and the electronic properties of materials, so understanding how they behave gives a powerful insight. In the most powerful diffraction contrast TEM instruments, it is possible to produce a diffraction pattern image which is directly analogous to the planes of atoms in the crystal.

- Use in this thesis

Transmission electron microscopy has been used in the cross section analysis of gate insulators (*Chapter VI*). Relevant information has been derived using this technique, as it will be stressed in the next chapters.

3.1.7. XRD: X-Ray Diffraction Analysis

- Description of Technique

There are several techniques of XRD (X-Ray Diffraction)[16-20] which use x-rays as source radiation and as carrier of sample information. X-rays are electromagnetic radiation with typical photon energies in the range of 100 eV - 100 keV. For diffraction applications, only short wavelength x-rays (hard x-rays) in the range of a few angstroms to 0.1 angstrom (1 keV - 120 keV) are used. Because the wavelength of x-rays is comparable to the size of atoms, they are ideally suited for probing the structural arrangement of atoms and molecules in a wide range of materials. The energetic x-rays can penetrate deep into the materials and provide information about the bulk structure. X-rays primarily interact with electrons in atoms. When x-ray photons collide with electrons, some photons from the incident beam will be deflected away from the direction where they original travel, much like billiard balls bouncing off one anther. If the wavelength of these scattered x-rays did not change (meaning that x-ray photons did not lose any energy), the process is called elastic scattering (Thompson Scattering) in that only momentum has been transferred in the scattering process. These are the x-rays that we measure in diffraction experiments, as the scattered x-rays carry information about the electron distribution in materials. On the other hand, in the inelastic scattering process (Compton Scattering), x-rays transfer some of their energy to the electrons and the scattered x-rays will have different wavelength than the incident x-rays. Diffracted waves from different atoms can interfere with each other and the resultant intensity distribution is strongly modulated by this interaction. If the atoms are arranged in a periodic fashion, as in crystals, the diffracted waves will consist of sharp interference maxima (peaks) with the same symmetry as in the distribution of atoms. Measuring the diffraction pattern therefore allows us to deduce the distribution of atoms in a material.
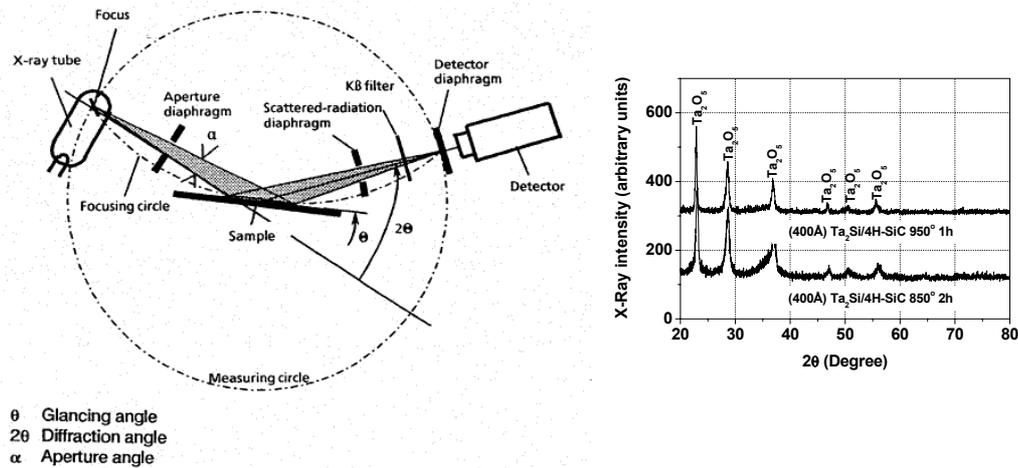
Fig. 3.7. Schematic representation of x-Ray diffraction apparatus used in conventional mode, and a XRD theta-2theta scan of Ta_2Si films oxidized on SiC.

- Analytical Information

Powder Diffraction - Powder XRD (X-ray Diffraction) is perhaps the most widely used x-ray diffraction technique for characterizing materials. As the name suggests, the sample is usually in a powdery form, consisting of fine grains of single crystalline material to be studied. The technique is used also widely for studying particles in liquid suspensions or polycrystalline solids (bulk or thin film materials). The term "powder" really means that the crytalline domains are randomly oriented in the sample. Therefore when the 2-D diffraction pattern is recorded, it shows concentric rings of scattering peaks corresponding to the various d spacings in the crystal lattice. The positions and the intensities of the peaks are used for identifying the underlying structure (or phase) of the material.

Thin Film Diffraction - Generally speaking thin film diffraction refers not to a specific technique but rather a collection of XRD techniques used to characterize thin film samples grown on substrates. These materials have important technological applications in microelectronic and optoelectronic devices, where high quality epitaxial films are critical for device performance. Thin film diffraction methods are used as important process development and control tools, as hard x-rays can penetrate through the epitaxial layers and measure the properties of both the film and the substrate.

Basic XRD measurements made on thin film samples include:

- Precise lattice constants measurements derived from $2\theta - \theta$ scans, which provide information about lattice mismatch between the film and the substrate and therefore is indicative of strain and stress
- Rocking curve measurements made by doing a q scan at a fixed 2θ angle, the width of which is inversely proportionally to the dislocation density in the film and is therefore used as a gauge of the quality of the film.
- Superlattice measurements in multilayered heteroepitaxial structures, which manifest as satellite peaks surrounding the main diffraction peak from the film. Film thickness and quality can be deduced from the data.

- Glancing incidence x-ray reflectivity measurements, which can determine the thickness, roughness, and density of the film. This technique does not require crystalline film and works even with amorphous materials.

Texture Measurement - Texture measurements are used to determine the orientation distribution of crystalline grains in a polycrystalline sample. A material is termed textured if the grains are aligned in a preferred orientation along certain lattice planes. One can view the textured state of a material (typically in the form of thin films) as an intermediate state in between a completely randomly oriented polycrystalline powder and a completely oriented single crystal.

Residual Stress Measurement - Structural and residual stress in materials can be determined from precision lattice constants measurements. For polycrystalline samples high resolution powder diffraction measurements generally will provide adequate accuracy for stress evaluation. For textured (oriented) and single crystalline materials, 4-circle diffractometry is needed in which the sample is rotated so that measurements on multiple diffraction peaks can be carried out.

Small Angle X-ray Scattering (SAXS) - SAXS measurements typically are concerned with scattering angles $< 1^o$. As dictated by Bragg's Law, the diffraction information about structures with large d-spacings lies in the region. Therefore the SAXS technique is commonly used for probing large length scale structures such as high molecular weight polymers, biological macromolecules (proteins, nucleic acids, etc.), and self-assembled superstructures.

X-ray Crystallography - X-ray crystallography is a standard technique for solving crystal structures. Its basic theory was developed soon after x-rays were first discovered more than a century ago. However, over the years it has gone through continual development in data collection instrumentation and data reduction methods. In recent years, the advent of synchrotron radiation sources, area detector based data collection instruments, and high speed computers has dramatically enhanced the efficiency of crystallographic structural determination. Today x-ray crystallography is widely used in materials and biological research. Structures of very large biological machinery (e.g. protein and DNA complexes, virus particles) have been solved using this method. In x-ray crystallography, integrated intensities of the diffraction peaks are used to reconstruct the electron density map within the unit cell in the crystal. To achieve high accuracy in the reconstruction, which is done by Fourier transforming the diffraction intensities with appropriate phase assignment, a high degree of completeness as well as redundancy in diffraction data is necessary, meaning that all possible reflections are measured multiple times to reduce systematic and statistical error.

▪ Typical Applications

Thin film analysis XRD is the most versatile diffraction technique available to characterize layers and films. It allows one to analyze all the same parameters as reflectometry while adding the following advanced capabilities: preferred orientation, composition, defect levels, topography, residual stresses, pole figures, reciprocal space maps. Additionally, determination of material properties: thickness, roughness, density, curvature, lateral correlation, among others.

▪ Use in this thesis

XRD has been found to be very useful in the determination of crystalline phases of oxidized Ta₂Si insulator (*Chapter VI*). Grazing incidence has been routinely used in the insulator thickness determination for (thermally grown or deposited) SiO_2 or alternative insulators on SiC.

3.2. Electrical characterization methods

Using the MIS capacitor for measuring electrical properties of the MIS system, the following properties can be obtained[21]:

1. Surface band bending and depletion layer width in the semiconductor as a function of the gate bias.
2. Voltage and field at avalanche breakdown in the semiconductor.
3. Doping profile in the semiconductor.
4. Interface trap level density as a function of energy in the bandgap.
5. Interface trap capture probability for both electrons and holes as a function of energy in the bandgap.
6. Lifetime in the bulk semiconductor.
7. Surface recombination velocity.
8. Insulator thickness.
9. Insulator breakdown field.
10. Charge configurations in the insulator such as insulator fixed charge and the charge at the interface between one insulator and another insulator deposited on top of it.
11. Nonuniformities in the insulator charge distribution and nonuniformities of surface potential caused by the discrete nature of charge in the insulator.
12. Work function differences between semiconductor and gate.
13. Ionic drift and polarization effects in insulator.
14. Diffusion of water into insulator.
15. Band-to-Band tunneling in the semiconductor and tunneling into insulator.
16. Quantum effects in the inversion layer at low temperatures (surface quantization).
17. Results of thermally activated chemical reactions and electrochemical reactions in Insulator.
18. Conductivity type of semiconductor.
19. Dielectric constant of semiconductor.
20. Dielectric constant of the insulator.
21. Properties of electron and hole traps in insulator.

The MIS capacitor has also been used in determining ways of controlling insulator fixed charge and interface trap level densities, effects of light on interface traps and surface charges, and in studying the effects of ionizing and radiation on insulator. Internal photoemission measurements using the MIS capacitor have yielded information about the barrier height between the conduction bands of semiconductor and insulator and about trapping centers distributed in the insulator layer. The goal of studying the MIS system is to improve the performance and the stability of devices such as the MOSFET used in integrated circuits. The MIS capacitor is simpler to use for these studies that the actual devices used in integrated circuits. The MIS capacitor is useful in

such studies because any change in processing that improves the electrical properties of the MIS capacitor makes the same improvement on the actual device. Thus the simplicity and the versatility of the MIS capacitor can be exploited with confidence for optimizing integrated circuit processing.

3.2.1. Electrostatic MIS theory and C-V behavior

The cross-section view of an ideal MIS capacitor is shown in Fig. 3.8(a). The corresponding energy band diagram without gate bias polarization[22] is depicted in Fig. 3.8(b). The ledge at the top of the vertical line, known as the vacuum level, denotes the minimum energy an electron must posses to completely free itself from the material. The energy difference between the vacuum level and the Fermi energy in a metal is known as the metal workfunction, Φ_m. In the semiconductor, the height of the surface barrier (relative to the conduction band E_C) is specified in terms of the electron affinity, χ_S. The forbidden band of a semiconductor is represented by E_C and E_V, the conduction and valence energy, respectively. Ideally, no charge should be present in the insulating layer of MIS capacitors. It should be neither induced during the processing cycle nor originate as a result of degradation during operation of the complete device. At the same time, leakage current must be negligible under normal operation conditions and a long time to breakdown must be guaranteed under stress conditions.

(a)   (b)
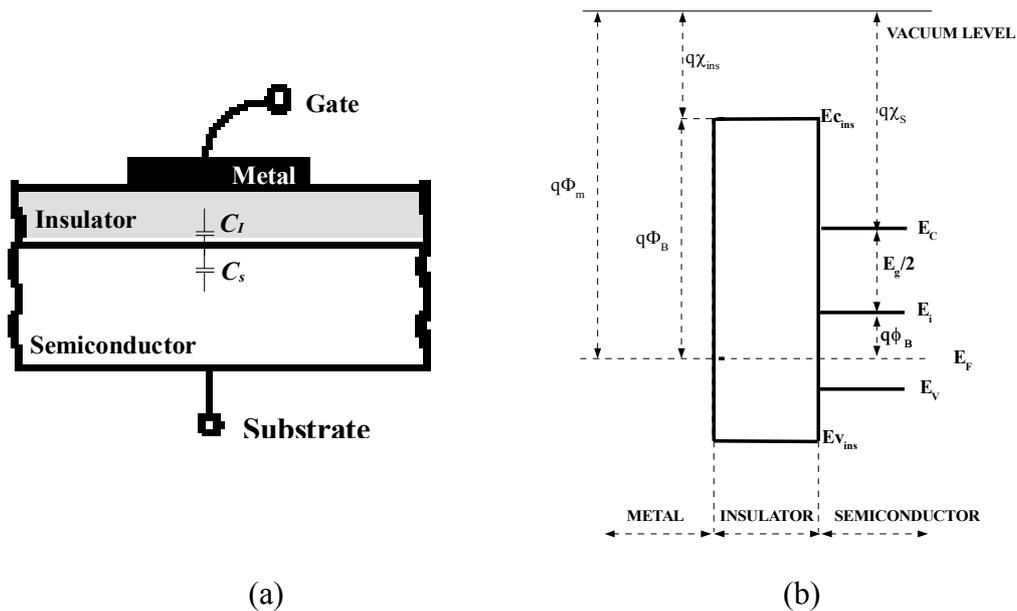
Fig. 3.8. (a) Ideal MIS capacitor and (b) its energy band diagram under equilibrium conditions.

Expressions for the charge density, electric field, and potential as a function of position inside the semiconductor are obtained by solving Poisson's equation. In solving Poisson's equation one could work with the standard system parameters and variables such as the semiconductor doping (N_A, N_D) and the electrostatic potential V. However, is more convenient to deal in terms of normalized parameters. It is therefore customary to introduce the following quantities[21,22]:

- $q\phi(x) \equiv E_F - E_i(x)$ (3.1) Surface potential.

- $\psi(x) \equiv \phi(x) - \phi_B$ (3.2) Band bending.

- $U_F \equiv \dfrac{1}{kT}\phi_B = -\ln\dfrac{N_D}{n_i}$ (3.3) Normalized Fermi potential substrate n-type.

- $U_F \equiv \dfrac{q}{kT}\phi_B = \ln\dfrac{N_A}{n_i}$ (3.4) Normalized Fermi potential substrate p-type.

- $U(x) \equiv \dfrac{1}{kT}\left[E_i(bulk) - E_i(x)\right] = \dfrac{q}{kT}\psi(x)$ (3.5) Normalized electrostatic potential.

Since the MIS capacitor is assumed to be a one-dimensional structure, Poisson's equation simplifies to,

$$\frac{dE}{dx} = \frac{\rho}{\varepsilon_s \varepsilon_0} = \frac{q}{\varepsilon_s \varepsilon_0}\left(p - n + N_D - N_A\right) \qquad (3.6)$$

Solving the differential equation and applying the boundary conditions[22]:

$$E = -\frac{kT}{q}\frac{dU}{dx} = \hat{U}_s \frac{kT}{q}\frac{F(U, U_F)}{L_D} \qquad (3.7)$$

(a)   (b)
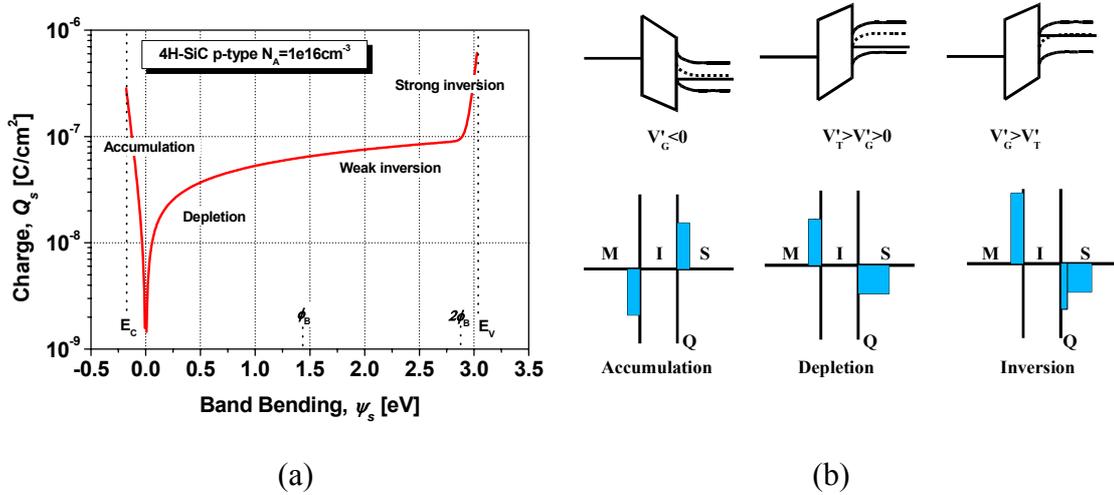
Fig. 3.9. (a) Plot of the total charge per unit area at the surface of the semiconductor, as a function of the band bending ψ_s. (b) Energy band diagrams for a p-type semiconductor for accumulation, depletion and inversion.

where

$$F(U, U_F) \equiv \left[e^{U_F}\left(e^{-U} + U - 1\right) + e^{-U_F}\left(e^{U} - U - 1\right)\right]^{1/2} \qquad (3.8)$$

$$\hat{U}_s \equiv \begin{cases} +1 & U_s > 0 \\ -1 & U_s < 0 \end{cases} \qquad (3.9) \qquad\qquad L_D = \left[\frac{\varepsilon_s \varepsilon_0 kT}{2q^2 n_i}\right]^{1/2} \qquad (3.10)$$

The "s" subscript means functions evaluated at the surface ($x=0$), and L_D is the intrinsic Debye length. k is the Boltzman constant, T is the temperature, ε_s is the semiconductor dielectric constant, q is the electronic charge, ε_0 the permittivity of free space, and n_i is the semiconductor intrinsic carrier concentration. When a bias voltage is applied to the ideal MIS capacitor, three different charge conditions are achieved at the semiconductor surface: accumulation, depletion and inversion, as inferred from Fig. 3.9.

Gate voltage relationship

We begin by noting that V_G' in the ideal structure is dropped partly across the insulator and partly across the semiconductor.

$$V_G' = \Delta V_{semi} + \Delta V_{ins} \quad (3.11)$$

Applying the Gauss's theorem and considering no carriers or charge centers in the insulator can be obtained the following relation[22]:

$$V_G' = \frac{kT}{q}\left[U_s + \hat{U}_s \frac{t'_{ins}}{L_D} F(U_s, U_F)\right] \quad (3.12) \qquad t'_{ins} \equiv \frac{\varepsilon_s t_{ins}}{\varepsilon_I} \quad (3.13)$$

where t_{ins} is the insulator thickness, and ε_I is the insulator dielectric constant.

Capacitance-Voltage Characteristics

Let us consider an ideal MIS capacitor with a low frequency ac signal applied to the gate of the device. When the ac gate voltage, v_g', is added to the dc gate voltage, V_G', the charge on the MIS-C gate is of course modified to $Q_G + q_g$, where Q_G and q_g are the dc gate charge per unit area and ac gate charge per unit area, respectively. Provided the device can follow the ac change in gate potential quasi-statically, the assumed case at low operational frequencies, one can state $Q_G(V_G') + q_g$ equals $Q_G(V_G' + v_g')$ or $q_g = Q_G(V_G' + v_g') - Q_G(V_G') = \Delta Q_G$.

Since quite generally: $C = A_{gate} \dfrac{q_g}{v_g}$

where A_{gate} denotes the gate area. In the low frequency limit, for the ideal structure:

$$C = A_{gate}\frac{q_g}{v_g'} = A_{gate}\frac{\Delta Q_G}{\Delta V_G'} \rightarrow A_{gate}\frac{dQ_G}{dV_G'} = -A_{gate}\frac{dQ_S}{dV_G'} = -A_{gate}\frac{dQ_S}{dU_s}\frac{dU_s}{dV_G'} \quad (3.14)$$

Thus, performing the required differentiations and reorganizing the results, it is concluded[22]:

$$C = \left[\frac{1}{C_I} + \frac{1}{C_s}\right]^{-1} = \frac{C_I}{1 + \dfrac{W_{eff}}{t'_{ins}}} \quad (3.15)$$

$$W_{eff} = \hat{U}_s L_D \left[\frac{2F(U_s, U_F)}{e^{U_F}(1 - e^{-U_S}) + \dfrac{e^{-U_F}(e^{U_S} - 1)}{1 + \Delta}}\right] \quad (3.16) \qquad C_I = \frac{\varepsilon_0 \varepsilon_I A_{gate}}{t_{ins}} \quad (3.17)$$

where for p-type devices:

$$\Delta \equiv dU \begin{cases} 0 & LOW - FREQ \\[2mm] 0 & Accumulation \\[2mm] \dfrac{(e^{U_S} - U_s - 1)/F(U_s, U_F)}{\displaystyle\int_0^{U_S} \dfrac{e^{U_F}(1 - e^{-U})(e^U - U - 1)}{2F^3(U, U_F)} dU} & Depletion / Inversion \quad HI - FREQ \end{cases} \quad (3.18)$$

For n-type devices:

Compute the V_G' as in the p-type case, changing the sign in the calculation of W_{eff}.

$$W_{eff}(U_s, U_F) = W_{eff}(-U_s, -U_F) \qquad (3.19)$$

At $U_s = 0$ the expression for W_{eff} becomes indeterminate and must be replaced by :

$$W_{eff} = \frac{\sqrt{2} L_D}{\left[e^{U_F} + e^{-U_F}\right]^{1/2}} \qquad (3.20)$$

C cannot be expressed explicitly as a function of V_G' in the exact charge formulation. Both variables, however, have been related to U_s and it is possible to compute numerically the capacitance expected from the structure for a given applied gate voltage. The usual and most efficient computational procedure is to calculate C and the corresponding V_G' for a set of assumed U_s values. Assuming $E_C - E_i \approx E_i - E_V \approx E_g / 2$ it can be easily demonstrated that if E_F is confined to band gap energies between E_V and E_C (no degeneration conditions):

$$U_F - (E_G / 2kT) \leq U_S \leq U_F + (E_G / 2kT) \quad (3.21)$$

Deep depletion

After the onset of weak inversion, the C-V characteristics of the MIS capacitor depend on measurement conditions (Fig. 3.10). A rapid change in gate voltage with insufficient time for minority charge generation will force the semiconductor surface into deep depletion. Increasing gate bias to enhance minority carrier generation results in an increase of the depletion layer width until a nonthermal process like avalanche, can lead to destructive breakdown of the MIS structure. The large bandgap of SiC, results in extremely low thermal generation of minority carriers at room temperature. No inversion layer at the SiC/SiO$_2$ interface can, therefore, be formed and only deep depletion C-V characteristics will be measured. If, however, additional minority carriers are created at the SiC/SiO$_2$ interface by elevated temperature (300 $^{\circ}$C) or by UV illumination, an inversion layer will build up during the voltage sweep. The limiting case as far as deep depletion is concerned occurs when the semiconductor is totally devoid of minority carriers-totally deep depleted. Except for a wide depletion width, the total deep depletion condition shown in the figure is precisely the same as a simple depletion condition. Consequently, by analogy and based on the delta-depletion formulation[22], the limiting-case capacitance exhibited by the structure under deep depletion conditions should be

$$ C = \frac{C_I}{\sqrt{1 + \dfrac{V_G'}{\dfrac{q}{2}\dfrac{\varepsilon_s t_{ins}^2}{\varepsilon_I^2 \varepsilon_0}\left(N_A - N_D\right)}}} \qquad (3.22) \qquad\qquad V_G' > V_T' \;\; \text{p-type} \qquad V_G' < V_T' \;\; \text{n-type} $$

where V_T' is the threshold voltage[22]. This equation is in excellent agreement with experimental observations and is essentially identical to the result obtained from an exact charge analysis.
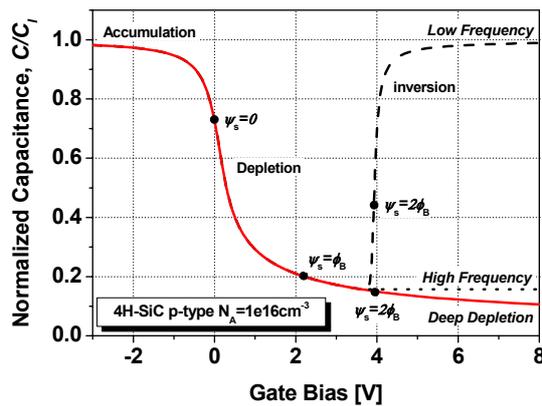
Fig. 3.10. C-V curves of an ideal p-type 4H-SiC MIS capacitor with (i) low frequency C-V curve, (ii) high frequency C-V curve with inversion, and (iii) high frequency C-V with deep depletion.

Parameter extraction from C-V measurements

Insulator Thickness.

With the C-MIS biased in strong accumulation:

$$C \approx C_I = \frac{\varepsilon_0 \varepsilon_I A_{gate}}{t_{ins}} \qquad (3.23)$$

Doping Level.

With the C-MIS biased in depletion:

$$N_{A,D} = \frac{2}{A_{gate} q \varepsilon_0 \varepsilon_s} \left[\frac{d}{dV} \left(\frac{1}{C^2(V)} \right) \right]^{-1} \quad (3.24)$$

Flatband capacitance.

$$C(\psi_s = 0) = C_{fb} = \frac{\varepsilon_0 \varepsilon_I A_{gate}}{t_{ins} + \frac{\varepsilon_I}{\varepsilon_s} \sqrt{\frac{\varepsilon_s \varepsilon_0 kT}{N_{A(D)} q^2}}} = \frac{\varepsilon_0 \varepsilon_I A_{gate}}{t_{ins} + \frac{\varepsilon_I}{\varepsilon_s} L_{Dp(n)}} \qquad (3.25)$$

Determination of semiconductor bandgap energy

An indirect method to obtain the semiconductor band bending as a function of the gate bias, uses comparison of a theoretical high frequency C-ψ_s curve with a measured high frequency C-V curve. Hence, from the C-V curve it is possible to interpolate the values of C_m (capacitance measured value) at a determined gate voltage into the theoretical high frequency C-ψ_s curve and thus, obtain the experimental value of ψ_s and then, from $\psi_s(C_m) \rightarrow \psi_s(V_G)$. However, there are two ways to directly measuring semiconductor band bending as a function of the gate bias[21]:

Q-V method.

$$\psi_s = \psi_s(0) + V_G \left(1 + \frac{C_w}{C_I} \right) - V_i \left(\frac{C_i}{C_I} \right) \qquad (3.26)$$

Low Frequency C-V method.

$$\psi_s(V_G) - \psi_s(V_{fb}) = \int_{V_{fb}}^{V_G} \left[1 - \frac{C_{LF}}{C_I} \right] dV \quad (3.27)$$

In the Low Frequency method (or its variance known as Berglund method[21]) the $\psi_s(V_G)$ can be obtained from an experimental low frequency C-V curve alone ($C_{LF}(V_G)$). V_{fb} is the flatband voltage. Q-V method is not considered in this thesis. It

will be explained how interface trap level density, D_{it}, can be determined as a function of the gate bias using capacitance or conductance methods. Furthermore, it will be shown how D_{it} and the interface trap time constants τ_p or τ_n can be found as function of gate bias using the conductance methods. To complete the interface trap analysis, the position of the Fermi level with respect to the majority carrier band edge at the semiconductor surface must be determined as a function of gate bias:

$$\frac{E_C - E_T}{q} = \frac{E_g}{2q} + \psi_s - \phi_B \qquad E_C - E_T = \frac{E_g}{2} - kTU_s + kTU_F \qquad \text{n-type (3.28)}$$

$$\frac{E_T - E_V}{q} = \frac{E_g}{2q} + \psi_s - \phi_B \qquad E_T - E_V = \frac{E_g}{2} + kTU_s - kTU_F \qquad \text{p-type (3.29)}$$

3.2.2. Interface and insulator charge

3.2.2.1. Flat-band Voltage: Insulator Charge

Interface and insulator charge are structural, chemical or impurity related defects in the insulator which can significantly affect the physical and electrical properties of field effect devices, in particular stability and reliability. The density of those defects depends on process condition. Effective control of defect centers in MIS structures is, therefore, essential for device operation. The charge centers associated with the MIS system are classified according to their electrical properties as interface trapped charge, fixed charge, mobile ionic charge, and oxide trapped charge (Fig. 3.11(a)).

(a)   (b)
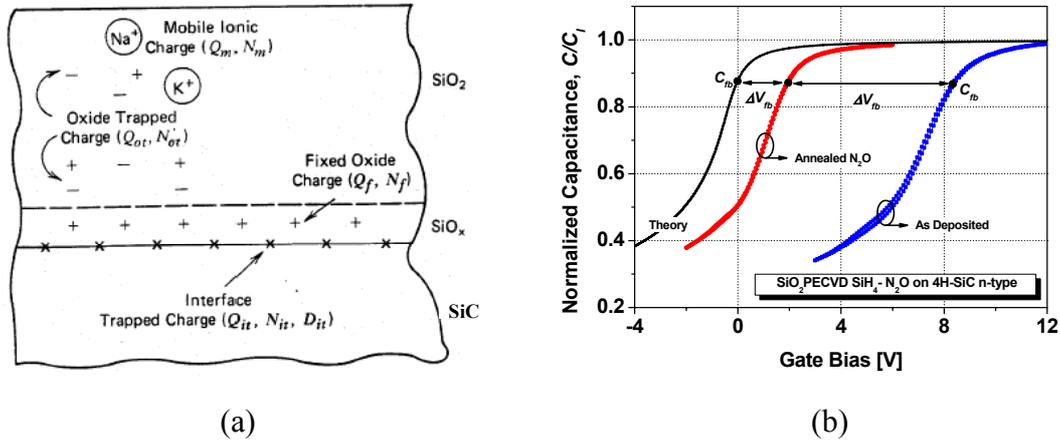
Fig. 3.11. (a) Pictorial description of the charge center associated with the MIS system. (b) The effect of annealing in reducing the insulator charge of deposited SiO_2 on SiC and hence, the flatband voltage shift.

The fixed charge centers Q_f, are located within a thin layer near the semiconductor/insulator interface. Fixed charges cannot transfer charge across the interface, but they can act on band bending of the semiconductor through their electric field. This results in a shift of the band bending of the semiconductor through their electric field (Fig. 3.11(b)). This results in a shift of the C-V curve toward negative

voltages for positive fixed charges and toward positive voltages for negative fixed charge.

$$\Delta V_G = \left(V_G - V_G'\right)\big|_{U_S} = -\frac{Q_f}{C_I} \quad (3.30)$$

Mobile ionic charges Q_m, can be related to sodium and potassium ions which are distributed randomly throughout the insulator bulk, with an ionic charge distribution $\rho_I(x)$. At room temperature, Q_m is detected as a fixed charge. At higher temperatures under an applied electric field, however, the charges become mobile and can be cycled back and forth between the metal/insulator and the insulator/semiconductor interface and the resulting ionic current can be detected.

$$\Delta V_G = \left(V_G - V_G'\right)\big|_{U_S} = -\frac{1}{\varepsilon_0 \varepsilon_I} \int_0^{t_{ins}} x \rho_I(x) dx = -\frac{Q_m' \gamma_m}{C_I} \quad (3.31)$$

$$\gamma_m \equiv \int_0^{t_{ins}} x \rho_I(x) dx / t_{ins} \int_0^{t_{ins}} \rho_I(x) dx \quad (3.32)$$

Insulator trapped charges, Q_{ot}, are associated with defects created either by impurities, radiation damage or hot charge carriers. Generally neutral, they become charged when charge carriers are captured by these traps, causing a voltage shift or a hysteresis of C-V curve.

An additional contribution results form the freeze-out of interface states. No clear distinction between these insulator charges and uncharged interface states is possible from electrical measurements carrier out at room temperature and so it will be inferred from the effective insulator charge Q_I calculated from the flat band voltage shift.

$$\Delta V_{fb} = \Delta V_f + \Delta V_m + \Delta V_{ot} = \frac{Q_I}{C_I} \quad (3.33)$$

$$Q_I = Q_f + Q_m + Q_{ot} \quad (3.34)$$

The metal-semiconductor work function difference, Φ_{ms}, also significantly affects the flat band voltage shift, and must therefore be taken into account[23]:

$$\Phi_{ms} = \Phi_m - \left(\chi_S + \frac{E_g}{2} + \phi_B\right) \quad (3.35)$$

Therefore, the actual insulator charge, Q_I, can be determined using:

$$Q_I = C_I\left(\Phi_{ms} - \Delta V_{fb}\right) \quad (3.36)$$

3.2.2.2. Interface traps

Judged in terms of their wide-ranging and degrading effect on the operational behavior of MIS devices, insulator-semiconductor interfacial traps must be considered the most important nonideality encountered in MIS structures. A common manifestation of a nonnegligible interfacial trap concentration within a MOS-C is the distorted or spread out of the nature of the C-V characteristics (Fig. 3.12(a)). Electrically, interfacial traps (also referred as surface states or interface states) are allowed energy states in which electrons are localized in the vicinity of a material's surface. The interface states can and normally do introduce energy levels distributed throughout the forbidden gap. Interfacial levels can also occur at energies greater E_C or less than E_V, but such levels are usually obscured by the much larger density of conduction or valence band states. In thermal equilibrium (Silicon), all interface traps levels above the Fermi level are positively charged, whereas all interface trap levels below the Fermi level are negatively charged. By moving the Fermi level, interface traps can interact with the semiconductor conduction or valence band by capturing and emitting charge resulting in a change of their occupancy (Fig. 3.12(b)).

(a)   (b)
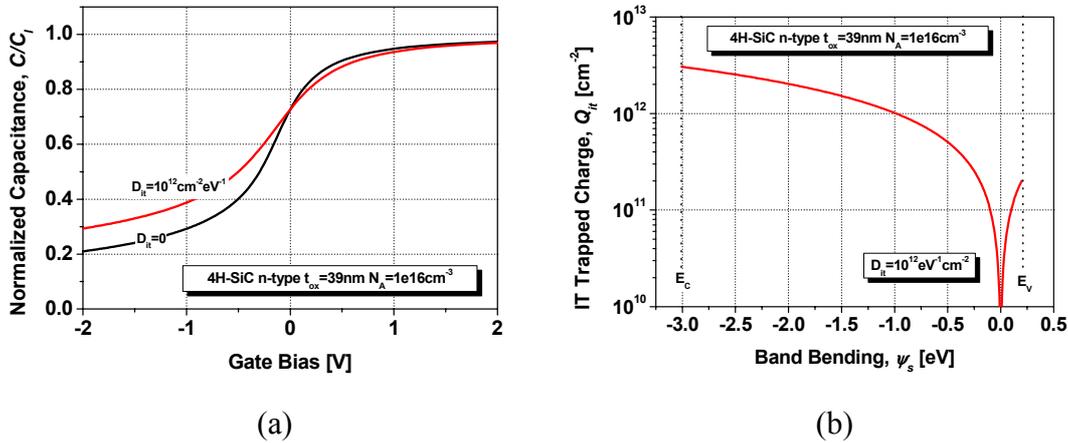
Fig. 3.12. (a) A theoretical high frequency C-V curve with interface trap "stretch out" compared to a theoretical C-V curve, with no interface traps[21]. $D_{it}=10^{12}$ cm^{-2}eV^{-1}. (b) Interface trapped charge vs band bending for an homogeneous IT distribution

Extraction of interface trap properties from the conductance

In the conductance method[21], interface trap levels are detected through the loss resulting from changes in their occupancy produced by small variations of gate voltage. A small ac voltage applied to the gate of a MIS capacitor alternately moves the band edges toward or away from the Fermi level. Majority carriers are captured or emitted, changing occupancy of interface trap levels in a small energy interval a few kT/q wide centered about the Fermi level. This capture and emission of majority carriers causes an energy loss observed at all frequencies except the very lowest (to which interface traps immediately respond) and the very highest (to which no interface trap response occurs). At any given frequency of ac gate voltage, the loss depends both on the speed of response of interface traps, determined by their capture probability, and on the interface trap level density near the Fermi level at the semiconductor surface. Knowing the loss at all frequencies and biases form experiment, we can find capture probability and interface trap level density for energy levels within the semiconductor bandgap.

The conductance technique is based on the measurement of the equivalent MIS parallel conductance $\langle G_P \rangle$. $\langle G_P \rangle$ represents the loss mechanism due to interface trap capture and emission of carriers, as a function of gate voltage and frequency.

$$\frac{\langle G_P \rangle}{\omega} = \frac{\omega C_I^2 G_m}{G_m^2 + \omega^2 (C_I - C_m)^2} \quad (3.37)$$

Assuming a simplified equivalent circuit of a MIS capacitor with a continuous distribution of interface traps within the semiconductor bandgap and with band bending fluctuations at the semiconductor/insulator interface, the equivalent MIS parallel conductance can be described as:

$$\frac{\langle G_P \rangle}{\omega} = \frac{q A_{gate}}{2} \int_{-\infty}^{\infty} \frac{D_{it}}{\omega \tau_p} \ln(1 + \omega^2 \tau_p^2) P(U_s) dU_s \quad (3.38)$$

A random spatial distribution of discrete interface charges results in a spatial distribution of band bending over the semiconductor-insulator interfacial plane. The probability than the band bending is U_s, is [The most common distribution characterized by only its mean and variance is the Gaussian. Moreover, when a large number of independent events (charges) contribute to U_s, a Gaussian distribution results from the law of large numbers]:

$$P(U_s) = \left(2\pi\sigma_s^2\right)^{-1/2} \exp\left[\frac{\left(U_s - \langle U_s \rangle^2\right)^2}{2\sigma_s^2}\right] \quad (3.39)$$

where σ_s is the standard deviation of the band bending. The measured characteristics time constants now corresponds approximately to mean band bending and is given by: $\tau_n = \frac{1}{c_n N_D} \exp(-\langle U_s \rangle)$ for electrons $\tau_p = \frac{1}{c_p N_A} \exp(\langle U_s \rangle)$ for holes. c_n and c_p are the electron and hole capture probabilities, respectively. Defining $\xi \equiv \omega \tau_p \cong \omega (c_p N_A)^{-1} \exp(\langle U_s \rangle)$ and $\eta \equiv U_s - \langle U_s \rangle$:

$$\frac{\langle G_P \rangle}{\omega} = \frac{q A_{gate} D_{it} \left(2\pi\sigma_s^2\right)^{-1/2}}{2\xi} \int_{-\infty}^{\infty} \exp\left(-\frac{\eta^2}{2\sigma_s^2}\right) \exp(-\eta) \ln(1 + \xi^2 \exp 2\eta) d\eta \quad (3.40)$$

The standard deviation of band bending, σ_s, is a measure of the width of $\langle G_P \rangle / \omega$ versus log frequency. The procedure to determine σ_s is to measure the amplitude of change of this curve either between the points f_p and f_p / n or between f_p and $n \times f_p$ (Fig. 3.13(a) and (b)),where f_p is the frequency corresponding to the peak value of $\langle G_P \rangle / \omega$:

$$\frac{\left(\langle G_P \rangle / \omega\right)_{f_p/n}}{\left(\langle G_P \rangle / \omega\right)_{f_p}} = n \frac{\int\limits_{-\infty}^{\infty} exp\left(-\frac{\eta^2}{2\sigma_s^2}\right) exp(-\eta) ln\left(1 + \xi_p^2 \, exp(2\eta)/n^2\right) d\eta}{\int\limits_{-\infty}^{\infty} exp\left(-\frac{\eta^2}{2\sigma_s^2}\right) exp(-\eta) ln\left(1 + \xi_p^2 \, exp \, 2\eta\right) d\eta} \qquad (3.41)$$

or

$$\frac{\left(\langle G_P \rangle / \omega\right)_{nf_p}}{\left(\langle G_P \rangle / \omega\right)_{f_p}} = \frac{1}{n} \frac{\int\limits_{-\infty}^{\infty} exp\left(-\frac{\eta^2}{2\sigma_s^2}\right) exp(-\eta) ln\left(1 + n^2 \xi_p^2 \, exp \, 2\eta\right) d\eta}{\int\limits_{-\infty}^{\infty} exp\left(-\frac{\eta^2}{2\sigma_s^2}\right) exp(-\eta) ln\left(1 + \xi_p^2 \, exp \, 2\eta\right) d\eta} \qquad (3.42)$$

where $\xi_p \equiv \omega_p \tau_p \cong \omega_p \left(c_p N_A\right)^{-1} exp\left(\langle v_s \rangle\right)$.

(a)   (b)

Fig. 3.13. (a) A typical $\langle G_P \rangle / \omega$ versus log frequency curve obtained experimentally for 4H-SiC with thermal oxide, where f_p is the frequency corresponding to the peak value. The points $5 \times f_p$ and $f_p / 5$ defined the width of the curve on the low and high frequency. (b) Computed plot of $\left[\langle G_P \rangle / \omega\right]/\left[\langle G_P \rangle / \omega\right]_{fp}$ versus standard deviation of band bending . This curve is used to get σ_s from the with of a $\langle G_P \rangle / \omega$ versus log frequency curve.

To calculate D_{it} it must evaluate $\xi = \xi_p$ and obtain the peak value $\left(\langle G_P \rangle / \omega\right)_{f_p}$

$$\left(\frac{\langle G_P \rangle}{\omega}\right)_{f_p} = \frac{q A_{gate} \, D_{it} \left(2\pi\sigma_s^2\right)^{-1/2}}{2\xi_p} \int\limits_{-\infty}^{\infty} exp\left(-\frac{\eta^2}{2\sigma_s^2}\right) exp(-\eta) ln\left(1 + \xi_p^2 \, exp \, 2\eta\right) d\eta \qquad (3.43)$$

Solving for D_{it}, and defining $f_D(\sigma_s)$ computed in Fig. 3.14(a):

45

$$D_{it} = \left(\frac{\langle G_P \rangle}{\omega} \right)_{f_p} f_D(\sigma_s) \qquad (3.44)$$

$$f_D(\sigma_s) \equiv \left[\frac{q A_{gate} \left(2\pi\sigma_s^2 \right)^{-1/2}}{2\xi_p} \int_{-\infty}^{\infty} \exp\left(-\frac{\eta^2}{2\sigma_s^2} \right) \exp(-\eta) \ln\left(1 + \xi_p^2 \exp 2\eta \right) d\eta \right]^{-1} \quad (3.45)$$

To determine τ_p, the condition $\dfrac{d}{d\xi}\left(\left(\dfrac{\langle G_P \rangle}{\omega} \right)_{f_p} \right) = 0$ is used:

$$\int_{-\infty}^{\infty} \exp\left(-\frac{\eta^2}{2\sigma_s^2} \right) \exp(-\eta) \left[\frac{2\xi_p^2 \exp 2\eta}{1 + \xi_p^2 \exp 2\eta} - \ln\left(1 + \xi_p^2 \exp 2\eta \right) \right] d\eta = 0 \quad (3.46)$$

Solving numerically yields ξ_p as a function of σ_s (Fig. 3.14(b)). Then, from the relation $\xi_p = \omega_p \tau_p$ the interface trap level time constant can be extracted. In summary, we need only two points on a $\langle G_P \rangle / \omega$ versos log frequency curve to determine D_{it} and τ_p namely $\left[\langle G_P \rangle / \omega \right]_{fp}$ and $\left[\langle G_P \rangle / \omega \right]_{nfp}$. Because it is not possible in advance to know these two frequencies, it is not possible to measure the admittance at only these two points; a complete admittance versus frequency curve must be measured at fixed bias.

(a)

(b)
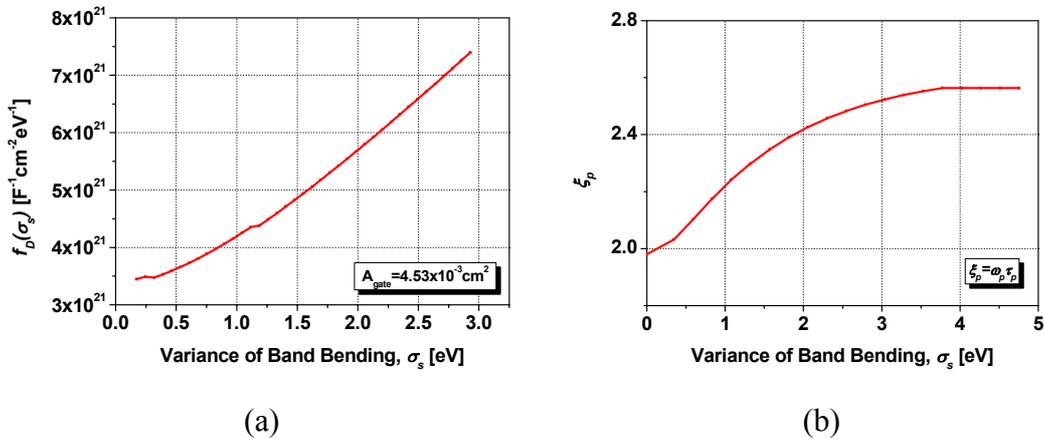
Fig. 3.14. (a) Computed plot of the universal function $f_D(\sigma_s)$ defined in (3.45) versus σ_s, used to calculated D_{it}. (b) Computed plot of ξ_p as a function of σ_s, used to calculate interface trap response time.

The standard deviation of band bending σ_s is a measure of the width of the experimental $\left[\langle G_P \rangle / \omega \right] / \left[\langle G_P \rangle / \omega \right]_{fp}$ vs the logarithm of the frequency. If those curves are narrow, band bending fluctuations can be neglected $\sigma_s \approx 0$ and the previous equations can be simplified.

$$\frac{\langle G_P \rangle}{\omega} = \frac{qA_{gate}D_{it}}{2\omega\tau_p} ln\left(1 + \omega^2\tau_p^2\right) \qquad (3.47)$$

This Equation shows a maximum of $\dfrac{\langle G_P \rangle}{\omega} = \dfrac{qA_{gate}}{2.5}D_{it}$ at $\omega_p = \dfrac{1.98}{\tau_p}$

Surface state density, D_{it}, is determined from the peaks of the experimental $\langle G_P \rangle / \omega$ vs $log\,\omega$ plots. Interface trap levels with time constant τ_p, respond completely to the applied ac signal for a given band bending. Hence, interface trap level density can be calculated:

$$D_{it} = \frac{2.5}{qA_{gate}}\left(\frac{\langle G_P \rangle}{\omega}\right)_{f_p} \qquad (3.48)$$

And interface time constant can be determined:

$$\tau_p = \frac{1.98}{\omega_p} = \frac{1}{c_p N_A}\exp(U_s) = \frac{1}{\sigma_{it}\overline{v_{th}}N_A}\exp\left(\frac{q\psi_s}{kT}\right) \quad (3.49)$$

Where σ_{it} is the capture cross section of the interface states and $\overline{v_{th}}$ the average thermal velocity of the electron gas.

Extraction of interface trap properties from the capacitance

There are three approaches to extract the interface trap level density as a function of the gate bias from the capacitive component of the measured admittance[21]:

(1) Comparison of the measured high frequency capacitance with theoretical capacitance with no interface traps. *Terman Method*.
(2) Comparison of a measured low frequency capacitance with a theoretical capacitance with no interface traps. *Low Frequency Method*.
(3) Comparison of a measured high frequency capacitance with a measured low frequency capacitance. *Hi-Low Frequency Method*.

Capacitance measurements reveal interface traps by way of stretch out of the C-V curves along the gate bias axis and the contribution of interface traps to the capacitance.

High Frequency Capacitance Method. (Terman Method)

The Terman method provides a rapid evaluation of the semiconductor-insulator interface. It is based on the extraction of the experimental surface potential ψ_s versus gate voltage curve V_G, by comparing the experimental C_m vs V_G curve with the theoretical C vs V_G plot. The resulting ψ_s vs V_G relation is a stretched out version of

the theoretical curve which contains all the relevant information to determine interface trap density:

$$D_{it}(\psi_s) = \frac{1}{qA_{gate}} \left(C_I \left[\left(\frac{d\psi_s}{dV_G} \right)^{-1} - 1 \right] - C_s(\psi_s) \right) \qquad (3.50)$$

The exact doping concentration of the semiconductor must be known, however to calculate the $C_s(\psi_s)$ relation.

Low Frequency Capacitance Method

Again, a C-V curve is measured at a constant frequency but now at a frequency so low that interface trap response is immediate. Because interface traps immediately respond to the ac gate voltage, they will contribute an additional capacitance C_{it} to the measured low frequency C-V curve.

$$D_{it}(\psi_s) = \frac{1}{qA_{gate}} \left(\left[\frac{1}{C_{LF}} - \frac{1}{C_I} \right]^{-1} - C_s(\psi_s) \right) \qquad (3.51)$$

Just as with the high frequency capacitance method, a theoretical calculation $C_s(\psi_s)$ is necessary.

Combined High-Low Frequency Capacitance Method

Combine high and low frequency C-V curves to obtain a measured C_s is possible. The step eliminates the need for a theoretical computation of C_s and for measurement of the doping profile of the device.

$$D_{it}(\psi_s) = \frac{1}{qA_{gate}} \left(\left[\frac{C_{LF}C_I}{C_I - C_{LF}} \right] - \left[\frac{C_{HF}C_I}{C_I - C_{HF}} \right] \right) \qquad (3.52)$$

Because of its advantages, the conductance method is used when a complete characterization of interfacial properties is desired or when sensitivity and accuracy are paramount. However, in many applications only interface trap level density is of interest and the sensitivity and accuracy of the conductance methods is not needed. The three capacitance methods are equivalent. If the substrate characteristics are unknown or with nonuniformities, the most suitable method is the combined high-low frequency capacitance method. In addition, this method allows obtaining interfacial characteristics without additional theoretical calculation. However, this last method can not be applied with dielectrics with moderate leakage current and is particularly susceptible to underestimating the trap density, if UV light is not used to empty all the deep-lying traps during measurement. Low frequency capacitance method suffers the same constrains than the combined High-Low frequency method.

3.2.3. I-V measurements

The most important parameters available from I-V measurements include, the identification of conduction mechanism in the insulator, the leakage current characteristics or the electrical breakdown phenomena investigation, which correspond to disintegration of the dielectric under high applied voltage. Electrical conduction in ideal insulators of MIS capacitors is assumed to be zero, but in real dielectrics a leakage current is observed when the electric field or temperature is sufficiently high. Electrical conduction in MIS devices is voltage and temperature dependent and may be caused by different carrier transport mechanisms[23]. The conduction mechanism are listed in Table III.1. In Table III.1, the parameters are: A, effective Richardson constant; E, electric field; t_{ins}, insulator thickness; m^*, effective mass; Γ, mean hopping frequency between two sites separated by an interval l; μ_{scl}, mobility; ϕ_a, activation energy of electrons, b', positive constant independent of V and T; K_T is the high frequency dielectric constant, square of the refractive index (n_{op}); ϕ_t is the barrier height; ε_i, insulator dynamic permittivity; V, applied voltage; h, Planck constant; n^*, density of free electrons in the insulator; and ϕ_i, activation energy of ions.

Process	Expression	
Schottky emission	$J = AT^2 \exp\left(-\dfrac{q\phi_t}{kT}\right)\exp\left(\dfrac{E^{1/2}}{kT}\sqrt{\dfrac{q^3}{4\pi\varepsilon_0 K_T}}\right)$	(3.53)
Poole-Frenkel emission	$J \approx E \exp\left(-\dfrac{q\phi_t}{kT}\right)\exp\left(\dfrac{E^{1/2}}{kT}\sqrt{\dfrac{q^3}{\pi\varepsilon_0 K_T}}\right)$	(3.54)
Direct Tunneling	$J \approx sh\left(\dfrac{b't_{ins}^2 E}{4\phi_t^{1/2}}\right)$	(3.55)
Fowler-Nordheim tunneling	$J \approx E^2 \exp\left(-\dfrac{8\pi\sqrt{2m^* q\phi_t^3}}{3hE}\right)$	(3.56)
Space-Charge-Limited	$J \approx \dfrac{8\varepsilon_i \mu_{scl} V^2}{9t_{ins}^3}$	(3.57)
Ohmic	$J = \dfrac{q^2}{kT}l^2\Gamma n^* E$	(3.58)
Hopping	$J \approx E \exp\left(-\dfrac{q\phi_a}{kT}\right)$	(3.59)
Ionic Conduction	$J \approx \dfrac{E}{T}\exp\left(-\dfrac{q\phi_i}{kT}\right)$	(3.60)

Table III.1. Conduction mechanisms in insulating films, from Sze[23].

Depending on the insulator, one of the charge transport processes may dominate in a certain temperature and voltage range. Illustrating this, Fig. 3.14 shows the I-V characteristic of 40 nm of Ta₂Si oxidized at 750 ºC during 2 h on a 4H-SiC substrate.

From 15 V of gate bias, Poole-Frenkel conduction mechanism considering the Ta_2O_5 optical constant ($n_{op} = 2.06$) can be invoked.
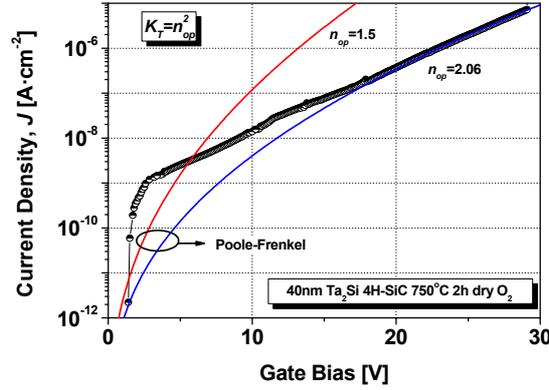
Fig. 3.14. An illustrative I-V curve obtained on MIS capacitors. The insulator is made up 40 nm deposited Ta_2Si and oxidized at 750 ºC during 2 h in O_2. Poole-Frenkel leakage mechanism is identified at high gate voltages.

The electrical field within the insulator can be computed by (t_{ins} is the insulator thickness):

$$E_{ins} = \frac{V_{gate}}{t_{ins}} \quad (3.61)$$

The current density per unit area is (A_{gate} is the capacitor area):

$$J\left[A{\cdot}cm^{-2}\right] = \frac{I_{gate}}{A_{gate}} \quad (3.62)$$

The average electric breakdown field E_{bd} can be extracted also from the I-V characteristics, when a critical current is reached.

3.3. Conclusions

The principal investigations carried out in this thesis are related with the characterization of thin insulators on SiC substrates. This thin insulator is generally used to create the gate of field-effect transistors (MOSFETs), and is known as *gate oxide.* The study of the properties of insulators as gate oxide on a semiconductor is mainly performed in a stacked structures composed of an oxide sandwiched between a metal and a semiconductor known as the metal-insulator-semiconductor (MIS) structure. The goal of studying the MIS system is to improve the performance of devices such as the MOSFET.

There are several physical methods to characterize the insulator layer in MIS capacitors. They are based in different physic principles such as the x-ray diffraction in the crystal lattice, the energetic binding energy of the atoms or the material resistance to a ion beam. The physical characterization methods employed in our layers and the

fundamentals of the technique have been briefly described in this chapter: Atomic Force Microscope (AFM), Energy Dispersive X-Ray analysis (EDX), Rutherford Backscattering Spectrometry (RBS), Scanning Electron Microscope (SEM), Secondary Ion Mass Spectroscopy (SIMS), Transmission Electron Microscopy (TEM) and X-Ray Diffraction Analysis (XRD) are introduced. AFM and SEM are used to obtain topographic information. TEM investigates the cross-section of thin layers. XRD, EDX, RBS and SIMS are employed to determine the composition, structure and/or thickness of the insulator layers.

The electrical measurements on MIS capacitors allow obtaining primordial information about the semiconductor or insulator dielectric properties, from both C-V and I-V measurements. The MIS capacitor has also been utilized in determining insulator fixed charge and interface traps densities. The insulator charge within the insulator provokes a shift in the flat-band voltage of the C-V curve. A common manifestation of a nonnegligible interfacial trap concentration within an MIS capacitor is the distorted or spread out of the nature of the C-V characteristics. Electrically, interfacial states are allowed energy states in which electrons are localized in the vicinity of a material's surface. In this thesis, to determine D_{it}, capacitance methods (Terman, Hi-low and Low frequency) and the conductance method are used, and described in this chapter.

References

[1]   The Handbook of Analytical Methods for Materials of the Materials Evaluation and Engineering, Inc. (MEE), http://www.mee-inc.com/ham.html

[2]   R. Wiesendanger, *Scanning Probe Microscopy and Spectroscopy: Methods and Applications*, Cambridge University Press, Cambridge U.K., (1994).

[3]   J. I. Goldstein, D. E. Newbury, P. Echlin, D. C. Joy, C. Fiori, and E. Lifshin, *Scanning Electron Microscopy and X-ray Microanalysis*, Plenum Press, (1981).

[4]   L. C. Feldman, and J. W. Mayer, *Fundamentals of surface and thin film analysis*, North-Holland, (1986).

[5]   Charles Evans and Associates RBS Tutorial, http://www.eaglabs.com/cai/rbstheo/cairtheo.htm

[6]   J.F. Ziegler, J.P. Biersack, and U. Littmark, *The stopping and range of ions in solids*, Pergamon, New York, (1985).

[7]   McIntyre, Leavitt, and Weller, *Handbook of Modern Ion Beam Materials Analysis; Chapter 4: Backscattering Spectrometry*, Materials Research Society, Pittsburg, (1995).

[8]   S. L. Flegler, J. W. Heckman, Jr., and K. L. Klomparens, *Scanning and Transmission Electron Microscopy: An Introduction*, Oxford University Press, (1993).

[9]   J. I. Goldstein, D. E. Newbury, P. Echlin, D. C. Joy, C. Fiori, and E. Lifshin, *Scanning Electron Microscopy and X-Ray Microanalysis: A Text for Biologists, Materials Scientists, and Geologists*, Plenum Press, (1984).

[10]   D. Chescoe and P. J. Goodhew, *Operation of Transmission and Scanning Electron Microscopes*, Oxford University Press, (1990).

[11]   Charles Evans and Associates SIMS Tutorial, http://www.cea.com/cai/simstheo/caistheo.htm

[12]   National Institute of Standards SIMS, http://www-sims.nist.gov/

[13]   A. Benninghoven, F. G. Rüdenauer, and H. W. Werner, *Secondary Ion Mass Spectrometry: Basic Concepts, Instrumental Aspects, Applications, and Trends*, Wiley, New York, (1987).

[14]   D.B. William,s and C.B. Carter, *Transmission Electron Microscopy*, Plenum Press, (1996).

[15]   Transmission Electron Microscopy (TEM)- Storyboard: P. Goodhew, University of Liverpool Based on Textbook: Transmission Electron Microscopy - Basics by D.B.Williams and C.B.Carter, http://www.matter.org.uk/tem/

[16]   Introduction to X-ray Diffraction, The Materials Research Laboratory (MRL) at the University of California, Santa Barbara, http://www.mrl.ucsb.edu/mrl/centralfacilities/xray/xray-basics/Xray-basics.html

[17]   J. Als-Nielsen, and D. McMorrow, *Elements of Modern X-ray Physics*, Wiley, New York, (2001).

[18]   B. E. Warren, *X-ray Diffraction*, General Publishing Company, (1969).

[19]   B.D. Cullity, *Elements of X-ray Diffraction*, 2nd Edition, Addison-Wesley, (1978).

[20]   D. K. Bowen and B. K. Tanner , *High Resolution X-ray Diffractometry and Topography*, Taylor & Francis, Ltd., (1998).

[21]   E. H. Nicollian and J. R. Brews, *MOS Physics and Technology*, Wiley, New York (1982).

III. CHARACTERIZATION METHODS OF MIS STRUCTURES

[22] R. F. Pierret, *Field effect devices. Modular series on solid state devices, v. 4*, Addison-Wesley, Reading, USA, (1983).

[23] S. M. Sze, *Physics of Semiconductor Devices*, Wiley, New York, (1969).

Chapter IV

Thermal oxidation of SiC

S ilicon carbide reacts chemically with oxygen to form a native oxide insulator which has the same chemical properties as thermal SiO_2 on Si. Oxides layers are needed for several applications, including the fabrication of MOS structures and MOSFET transistors which is the first step towards integration. Additionally, they are also necessary for field oxide and passivation layers used in most of microelectronic devices. Thermal oxides are also used as a material for masking operations during device fabrication, but in this case interface properties are not critical. The oxidation rate and the oxide properties depend on several factors such as, the SiC polytype, the terminal face of the substrate being oxidized, the doping concentration or the crystallographic orientation[1]. In any case, the density of interface traps close to the semiconductor conduction band edge is at least one order of magnitude higher for SiC than Si[2]. The interface state density is sensitive to variations in processing and efforts to reduce the trap density are described in this chapter.

4.1. Thermal oxidation in O_2

In a manner similar to Si, SiC forms a SiO_2 layer at the surface when exposed to O_2 (dry oxidation) or H_2O (wet oxidation) at high temperature. Thermal wet and dry oxidation of 3C, 4H and 6H-SiC has been extensively studied at temperatures ranging from 900 ºC to 1250 ºC [1]. SiC offers a high resistance to thermal oxidation which requires temperatures higher than 1000 ºC to be practical. Under the same growth conditions, the thermal oxidation of SiC is slower than the oxidation of Si [3]. Under usual conditions (flow of O_2 and/or H_2O between 800 ºC and 1200 ºC), several hours are needed to obtain an oxide layer. During dry oxidation, the principal chemical reactions are[4]:

$$SiC + \frac{3}{2}O_2 \Leftrightarrow SiO_2 + CO \quad (4.1)$$

$$SiC + O_2 \Leftrightarrow SiO_2 + C \qquad (4.2)$$
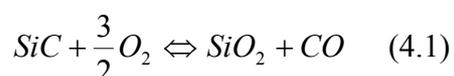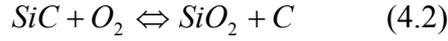
The amount of carbon left in the oxide will also be determined by the reactions

$$SiC + 2CO \Leftrightarrow 3C + SiO_2 \qquad (4.3)$$

$$2C + O_2 \Leftrightarrow 2CO \qquad (4.4)$$

It is generally believed that most of the carbon is removed from the oxide as $CO_{(g)}$ or $CO_{2(g)}$. Auger electron spectroscopy and the refractive index, as determined by ellipsometry, among other characterization techniques, show that the oxide is close to stoichiometric SiO_2 [5,6]. The oxidation kinetics of SiC is described by the same kinetics rules as oxidation of Si [6], as defined by Deal and Grove[7]. In the beginning, the oxidation growth regime is linear, that is the oxidation is limited by reactions at the SiO_2/SiC interface. Then, once an oxide layer is formed, the oxidizing species have to cross through this oxide layer. During this diffusion-controlled phase, the oxidation becomes slower and the growth regime is parabolic. This growth can be written as[7],

$$t_{ox}^{\ 2} + A_{DG} t_{ox} = B_{DG}(t + \tau) \qquad (4.5)$$

where t_{ox} is the oxide thickness, and t is the oxidation time. When a thermal oxide of thickness, t_{ox}, is formed, $0.45\, t_{ox}$ of thickness of SiC is consumed. The time constant, τ, takes into account the thickness of the initial oxide layer. Constant B_{DG} is proportional to the diffusion coefficient and is called the parabolic rate. These two constants are thermally activated[7] as $\exp(-E_{B/A}/kT)$ and $\exp(-E_B/kT)$ for the linear and parabolic rate respectively. $E_{B/A}$ and E_B can be found in the literature[1] for the different SiC polytypes.

4.1.1. Dry O₂ oxidation. The standard thermal oxidation.

Different oxidation processes have been employed during this thesis: wet and dry CNM oxidation processes for SiC including a re-oxidation at low temperature. After the cleaning procedure, SiC wafers are immediately transferred to a resistance heated quartz wall furnace tube with pyrogenic steam generation capability for wet or dry thermal oxidation. During oxidation, wafers are placed vertically on a quartz boat, located on a SiC cantilever. The total gas flow is kept at about 6 slm. The purity of the gases is in the 99.995-99.9995% range.

In the CNM oxidation process, developed[8] for high quality SiC oxides, samples are loaded in oxygen at 800 ºC with a 10 min push and the temperature is raised to the oxidation temperature with a ramp of 5 ºC/min. Oxidation is carried out at 1000-1175 ºC in pure oxygen. The oxidation is followed by a 60 min in-situ argon anneal at the oxidation temperature. This argon anneal is assumed to be important for the out-diffusion of remaining carbon in the grown oxide, thus favoring the stoichiometry of the SiO_2 layer[8].

After the anneal, the temperature is ramped down at 5 ºC/min in argon to 950 ºC and a reoxidation in dry or wet O_2 ambient is carried out for 180 min, because it has been found to significantly lower interface and insulator defect density[9]. The re-

oxidation anneal results in almost no further oxidation of the SiC substrate. It is speculated[9] that, low temperature reoxidation completes the oxidation of any possible carbon compounds and encourage stoichiometry at the SiC/SiO$_2$ interface. The temperature is then gradually reduced at 5 ºC/min to 800 ºC and the wafers are withdrawn from the furnace under Ar flow with a 10 min pull. Fig. 4.1. exhibits the thermal oxidation process with post-oxidation anneal and low temperature wet reoxidation. This process will be referred as the *(CNM) standard thermal oxidation*. The oxides grown with this process will be used as reference (on 4H-SiC and 6H-SiC) in the next chapters. Previous experiments[8] have shown that dry oxidation, at 1150 ºC, gives better results than wet oxidation in terms of thickness, leakage current, oxide charges and oxide reliability.
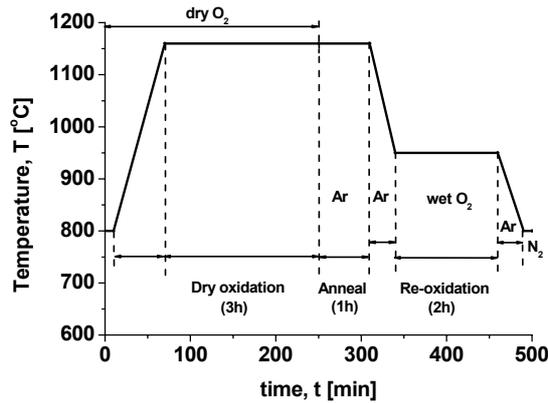
Fig. 4.1. The CNM standard thermal oxidation to grown ~40 nm of SiO$_2$ on 4H-SiC and on 6H-SiC.

High frequency C-V measurements of MOS structures are commonly used to characterize the quality of semiconductor/interfaces[10]. The flatband voltage shift indicates thereby the presence of a fixed insulator charge Q_I, whereas a high density of interface trapped charge Q_{trap}, due to the trapping of carriers in interface states described by D$_{it}$, is responsible for broad slope variations or distortions of the CV curve. The wide bandgap of SiC has to be taken into account for adopting a characterization methodology for SiC MOS capacitors. The majority of interface states at the SiC/SiO$_2$ interface are energetically away from the band edges, leading to extremely large emission times at room temperature[11]. Low frequency capacitance is measured using the quasi-static method, by using a slow sweep rate. As stated in *Chapter III*, by combining the high and low frequency curves, the interface states density spectrum D$_{it}$, can be calculated. Terman's method using only the high frequency curve can also be used. The conductance method is also a tool to calculate D$_{it}$ spectra and the capture cross-section, although measurements take longer.

4H-SiC Thermal oxidation

When making SiC power devices, the 4H-SiC polytype is preferred to 6H-SiC since the bulk electron mobility is higher and more isotropic in 4H-SiC [12]. For this reason, the major work of this thesis is focused on oxides on 4H-SiC substrates in the Si-face with (0001) crystallographic orientation, that is the main commercial available substrate. The 4H-SiC (11-20) orientation has also been used, yielding exiting results, as

will be illustrated in the next chapter. 6H-SiC substrates have also been eventually used to compare the electrical properties of MOS gated devices in both polytypes.

Fig. 4.2 shows the high (100 kHz) and low frequency curves for MOS capacitors with standard thermal oxide on (a) n-type and (b) on p-type 4H-SiC substrates. Theoretical curves are derived from Ref. 10, as stated in *Chapter III*, and flatband corrected. A large deviation from the ideal traces is observed in both substrates, specially for p-type substrate. Flatband, and thus insulator fixed charges, is also higher for p-type substrates.

(a)   (b)
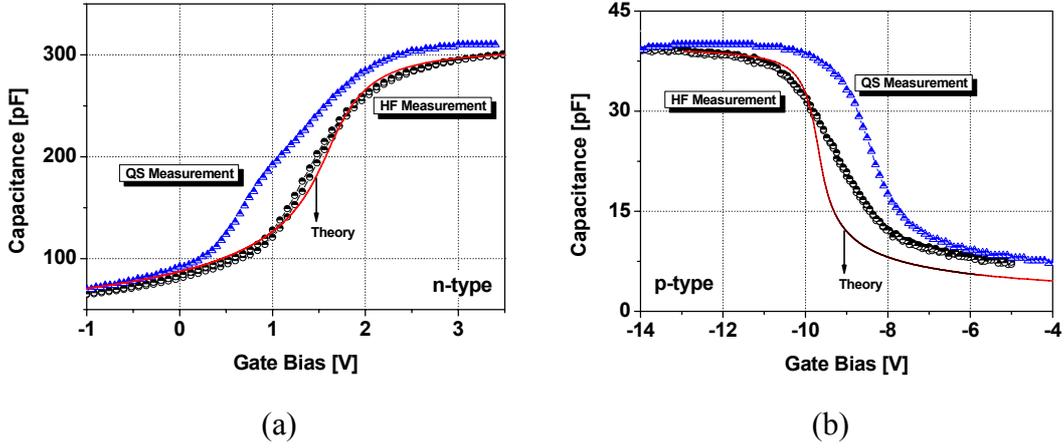
Fig. 4.2. High frequency (100kHz) and quasitatic C-V on (a) n-type and (b) p-type 4H-SiC (0001) Si capacitors with 40 nm thick oxides.

(a)   (b)
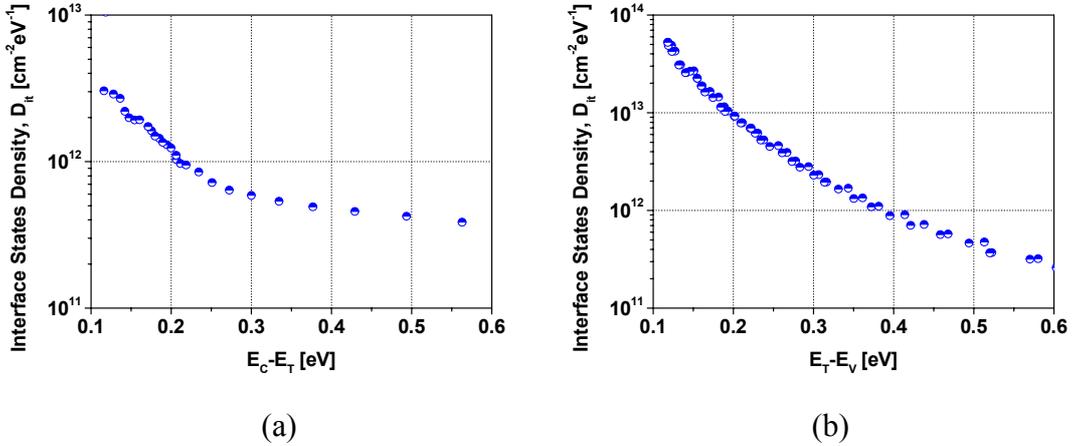
Fig. 4.3. Interface states density, D_{it}, as a function of energy for 4H-SiC for (a) close the conduction band (n-type), and (b) close the valence band (p-type).

The interface traps density within the band-gap close to the conduction and valence band is presented in Fig. 4.3. MOS capacitors on n-type 4H-SiC are used to extract D_{it} close to the conduction band (Fig. 4.3(a)). Analogously, MOS capacitors on p-type substrate are used to investigate the traps close the valence band (Fig. 4.3(b)). Our experimental results aim at a significant increase of interface traps when approaching to the conduction band. D_{it} of 1×10^{12} eV^{-1}cm^{-2} at $E_C - E_T = 0.2$ eV has been obtained for thermally grown oxides on n-type substrate. Significant higher interface traps density is achieved for thermally grown oxides on p-type substrates, 1×10^{13} eV^{-1}cm^{-2} at $E_T - E_V = 0.2$ eV. Interface states density very close (<0.1 eV) the

conduction or valence band is difficult to detect with simple electrical measurement, and must be considered as an approximation[10].

6H-SiC Thermal oxidation

For comparison purposes, MOS capacitors with thermally grown oxides have been fabricated on (0001)Si n-type 6H-SiC substrates. The grown kinetics has been found to be similar to the 4H-SiC polytype. However, slightly higher oxidation rate in the 6H-SiC polytype seems to be inferred. It is generally assumed that the density of interface traps close to the semiconductor conduction band edge is at least an order of magnitude higher for 4H-SiC than 6H-SiC polytype[13,14]. Our experimental results clearly agree with this assumption. High frequency (100 kHz) and quasistatic C-V characteristics of MOS on 6H-SiC are shown on Fig. 4.4(a). The distortion of the high frequency C-V curve is significantly lower (compared with the 4H-SiC C-V), and the differences between high and low frequency measurements is also markedly reduced. An interface trap density of 1×10^{11} eV^{-1}cm^{-2} at $E_C - E_T$ =0.2 eV has been obtained for thermally grown oxides on 6H-SiC n-type substrate, as it can be derived from Fig. 4.4(b).

(a) (b)
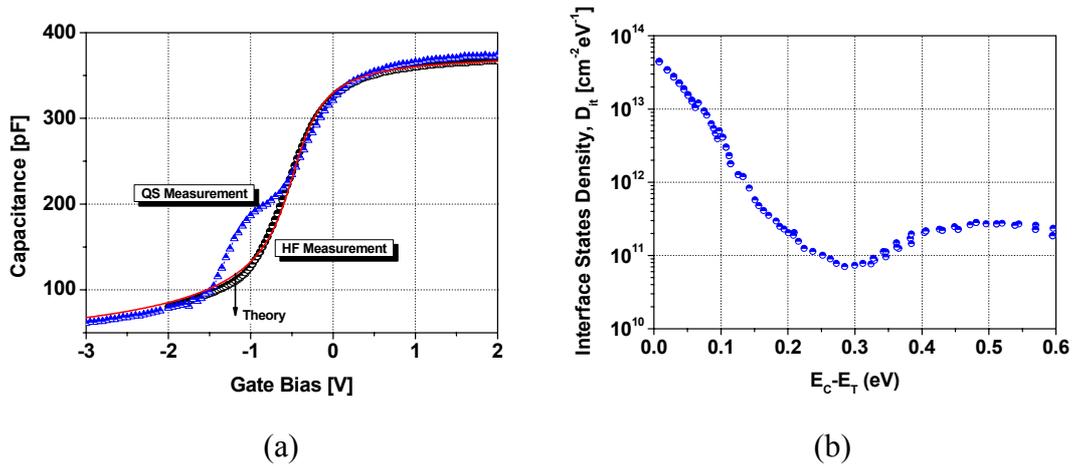
Fig. 4.4. (a) High frequency (100kHz) and quasitatic C-V, and (b) D$_{it}$, as a function of energy for, 6H-SiC on n-type (0001) Si capacitors with 40 nm thick oxide.

The interface traps within the bandgap for the 4H-SiC and the 6H-SiC polytypes are presented in Fig. 4.5. E_C and E_V indicate the conduction and valence band, respectively. As it has been stressed before, it is difficult to define the actual interface traps density very close (<0.1 eV) to the semiconductor bandgap edges with electrical methods or even with physical measurements. However, some trends are well established: D$_{it}$ is higher for the 4H-SiC polytype and for p-type rather than n-type. Schörner *et al.*[13], suggested that the interface traps generated during thermal oxidation are confined to a small energy range and pinned at approximately 2.9 eV above the valence band edge. Hence, for polytypes with bandgaps around or smaller than 2.9 eV, such as 6H-SiC [3.02 eV], 15R-SiC [2.98 eV] or 3C-SiC [2.38 eV], these interface traps will become resonant with the allowed states in the conduction band, thus diminishing their negative influence on the SiO$_2$/SiC interface quality. Afanas'ev *et al.*[15], explain the considerable asymmetry in the defect density between the upper and lower part of the

SiC bandgap, caused by an additional high density of donor-type defects with energy levels close to the valence band.
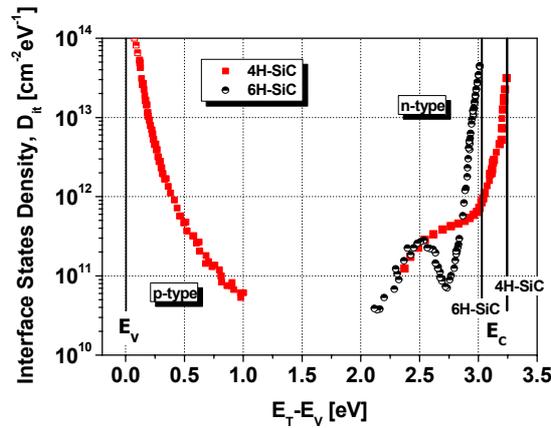
Fig. 4.5. Interface state density within the bandgap for 6H (circles) and 4H (squares) SiC/SiO$_2$ structures with standard thermal oxidation. The bandgap energy is 3.02 eV and 3.26 eV, respectively

3C-SiC Thermal oxidation

Nowadays, the most promising SiC polytype is 3C-SiC, where record high mobilities[16] of 229 cm^2/Vs have been achieved, as it will be detailed in the last section. This correlated with the low density of interface traps found near the 3C-SiC conduction band-edge. The reason the 3C-SiC MOSFET has not achieved supremacy is due to the low quality of the 3C-SiC single crystalline material. Preliminary dry thermal oxidation of 3C-SiC substrates has also been performed in this thesis. 3C-SiC substrates used in this thesis are not commercial substrates, but represent the best state of the art of 3C-SiC on Si Material.

(a)   (b)
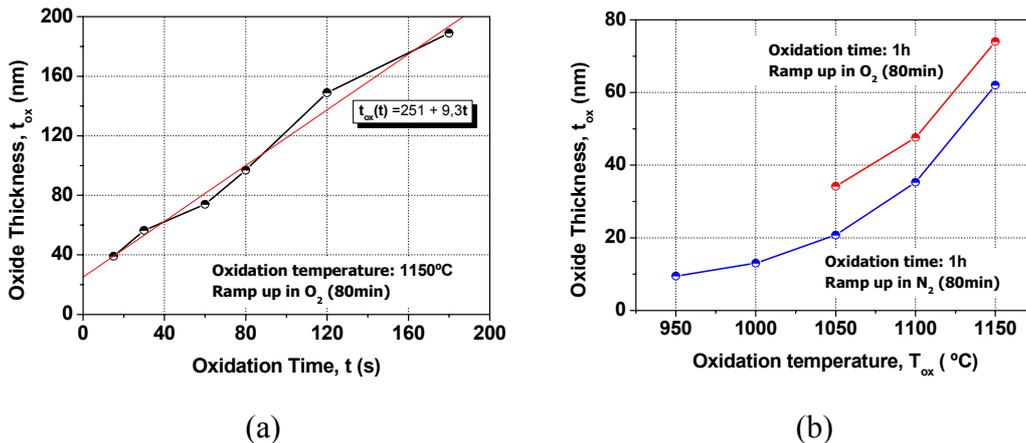
Fig. 4.6. Oxide thickness in thermal dry oxidation on 3C-SiC substrate as a function of (a) time at 1150 ºC, and (b) Temperature during 1 h.

As inferred from Fig. 4.6(a), the oxide growth rate on 3C-SiC substrate is higher (approximately six times) when compared with 4H-SiC or 6H-SiC polytypes. At 1160 ºC, an oxidation time of 20 min is needed to achieve 40 nm of thermal SiO$_2$, whereas to reach the same thermal oxide thickness on hexagonal phases [(0001)Si-face] requires at

least 3 hours. The oxidation temperature is the other relevant parameter according with Deal and Grove[7] formulation (Fig. 4.6(b)).

However, the 3C-SiC substrates used in this preliminary research present very high non-uniformities and roughness. The thermally grown oxide on 3C-SiC substrates presents roughness of more than ten times (Fig. 4.7) the one obtained for the oxides thermally grown on the 4H-SiC or 6H-SiC polytype. The applicability of such substrates is only demonstrated as material for nanocantilevers. The MOS capacitors fabricated on the 3C-substrates have presented very high oxide traps yielding flatband voltages of more than –30 V for 40 nm thick oxides. Fig. 4.8 presents a high frequency C-V curve for a dry thermal oxidation carried out at 950 ºC during 1 h.
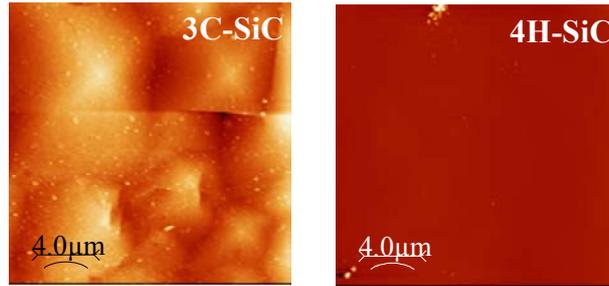
Fig. 4.7. AFM images of thermal oxidized SiC surfaces on the 3C-SiC/Si and commercial 4H-SiC substrates. A columnar growth is detected for the 3C-SiC sample
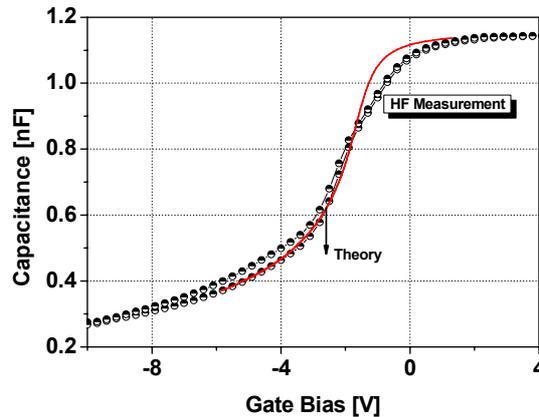
Fig. 4.8. C-V characteristic measure at 100 kHz in n-type 3C-SiC capacitors grown on non-commercial substrate.

The oxide thickness is around 10nm. High interfacial traps density have been obtained for these capacitors with 1×10^{13} eV^{-1}cm^{-2} at $E_C - E_T$ =0.2 eV. Due to the significant oxide contamination, the insulator formed during thermal oxidation of these 3C-SiC substrates, also presents poor insulator strength with a high leakage current (1 mA) at very low gate voltages (1 V).

4.1.2. Other oxidation conditions.

Wet oxidation can be carried out on the SiC samples following the standard oxidation process, replacing pure oxygen with a wet O$_2$ ambient (H$_2$/O$_2$/C$_2$Cl$_2$O$_2$: 3/4.5/0.15 slm). Several studies[17-19], on different SiC polytypes, have reported than wet

thermal oxides have lower oxide charge and interface state densities than dry ones. However, other studies[20,21] have reported higher D_{it} but lower oxide fixed charge for wet oxides, and that the electrical properties depend on the oxidation ambient and temperature[20]. Although it is not the scope of this thesis, some wet thermal oxides have been analyzed on 4H-SiC substrates. In particular, short time wet oxidation of 4H-SiC substrates have been studied. Fig. 4.9 shows (a) the high frequency C-V and (b) the D_{it} profile near the conduction bandgap for the MOS capacitors.

(a)   (b)
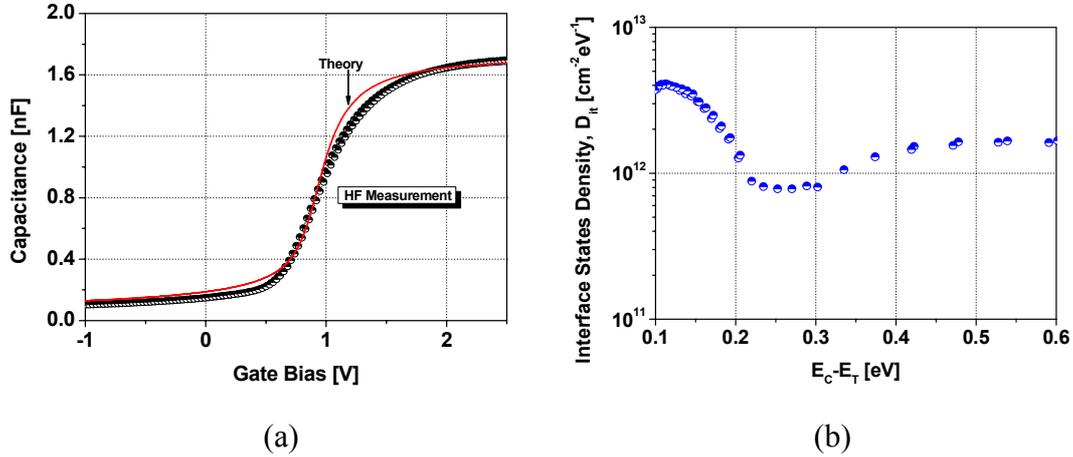
Fig. 4.9. (a) High frequency (100 kHz) C-V, and (b) D_{it} as a function of energy, for 4H-SiC on n-type (0001) Si capacitors (wet thermal oxidation) with 10 nm thick oxide.

No significant improvements have been achieved when compared with standard dry thermal oxidation. A D_{it} of 1×10^{12} eV^{-1}cm^{-2} at $E_C - E_T$ =0.2 eV has been obtained for thermally grown wet oxides on 4H-SiC (0001)Si n-type substrates.

Another relevant issue is the oxidation temperature. It has been reported that, oxides grown at 1000 ºC display less charges than oxides grown at higher temperatures[20]. When increasing oxidation temperatures, the oxide charge and interface defect densities also increase[9,22].

Apart from wet oxidation or oxidation temperature, impurities can alter both the SiC oxidation rate and the quality of the SiC/SiO$_2$ interface. The density of interface traps close to the conduction band-edge can be reduced and transistors made using contaminated oxides have high field-effect mobility[23-25]. In the patent of Alok *et al.*[26], metallic impurities were introduced by placing a piece of sintered alumina (Al$_2$O$_3$) containing iron impurities in the oxidation chamber. Ölafson *et al.*[27], introduce impurities into the oxide during oxidation, performing oxidation in an environment where both, the furnace tube and the boat carrying the sample are made of alumina. At the time of this writing, metallic contaminated gate oxide is the best gate fabrication process reported, achieving record high mobility in 4H-SiC (0001)Si substrates as it will be shown later on. The use of metallic impurities incorporation on the gate oxide must be an important issue for the future works related with this thesis.

4.1.3.   Post oxidation treatments.

Interface traps at the silicon/oxide interface can be passivated by annealing in hydrogen at 450 ºC so many hoped for an equivalent solution for the SiC/oxide interface. Lipkin *et al.*[9], showed that annealing the oxide in pyrogenic steam at temperatures below the oxidation temperature of SiC reduces the density of deep

interface states and thus also reduced the apparent fixed oxide charge. This post-oxidation annealing step is referred to as a reoxidation step. It is thought that reoxidation reduces the amount of carbon at the interface, thus reducing the number of deep interface states. This, however, does not improve the transconductance of 6H-SiC n-channel MOSFETs. However, by optimizing the water content during the reoxidation anneal, Kosugui et al.[28], showed that the filed-effect mobility for 4H-SiC MOSFETs could reach 47 cm^2/Vs.

Analogously, post-annealing in hydrogen at 800ºC improves the interface and the MOSFET mobility is raised[29-32]. Other post-oxidation treatments, such as Ar or He [33,34] annealings, have been reported to reduce interface state density and oxide charges. For these reason, our standard thermal oxidation process (Fig. 4.1) includes, a post-oxidation annealing and a low temperature re-oxidation. The oxidation process, the annealing process, and the reoxidation conditions have been extensively studied and optimized in our furnace. Nevertheless, high interface traps density still remains near bandgap edges, especially in the thermally grown SiO$_2$ on the 4H-SiC polytype. The simple thermal oxidation seems to direct our efforts to a cul-de-sac. Hence, it is justified, even necessary, the search of novel materials and processes for gate dielectrics on Silicon carbide, that is the scope of this thesis.

4.2. NO or N$_2$O nitridation

4.2.1.   Nitridation versus oxidation

The theory of NO nitridation in SiO$_2$/Si is that NO diffuses through the oxide and reacts with the interface, leaving nitrogen and promoting new oxide growth; however, the exact reaction mechanism is unknown[35]. At the same time as the interfacial reaction, oxygen atoms at the surface of the oxide are exchanged with oxygen atoms in the gas phase. Nitric oxide discomposes at high temperatures by the reaction[36,37]:

$$2NO \rightarrow N_2 + O_2 \qquad (4.6)$$
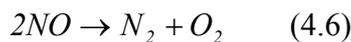
At these temperatures, N$_2$ is inert, but O$_2$ removes the nitrogen incorporated at the SiO$_2$/SiC interface and increases the oxide thickness. To understand and optimize nitridation process using NO, careful attention must be given to the composition of the gas ambient during an anneal. Excess silicon and carbon could be intrinsic components of the transition layer between SiC and SiO$_2$, and their complete removal from the interface may not be possible[38]. It is also know that silicon suboxide bonds exits at both the Si/SiO$_2$ and SiC/SiO$_2$ interfaces[39,40], and the density of these defects is estimated to be ~10^{15} cm^{-2} in silicon. These suboxides defect states evidently do not lie within the band gap of silicon, as shown by the low D$_{it}$ values achievable in Si/SiO$_2$, but these states may be within the band gap of SiC. Instead, the passivation of these defects with additives like nitrogen might be used to change the energy of these states in the band gap and reduce their detrimental effects. Nitridation using NO provides an effective technique for reducing D$_{it}$ in SiO$_2$/4H-SiC near the conduction band and increasing the channel mobility[41,42]. The interfacial properties of SiO$_2$/SiC, such as excess carbon, are clearly responsible for many features observed in NO nitridation. A comparison of SiO$_2$/SiC with the well-studied SiO$_2$/Si system is instructive in understanding how the

interface affects nitridation. A comparison of NO nitridation in SiO_2/Si and SiO_2/SiC shows similar initial behavior, although the amount of incorporated nitrogen and new oxide growth is ~10 time greater at the SiO_2/Si interface. The nitridation of SiO_2/SiC by NO proceeds by two processes[35]: (1) NO reacts with silicon and carbon at the interface to incorporate nitrogen; (2) O_2 produced by the thermal decomposition of NO oxidizes the substrate and removes nitrogen from the interface. The Nitrogen removal from the SiO_2/SiC interface is due to a fundamental property of SiC, such as the excess carbon at the interface. However, nitrogen removal is observed in the oxidation of Si using N_2O.

4.2.2.   Oxides grown or annealed in NO

The double mechanism of NO at the SiC interface requires the optimization of the conditions of nitridation process. Significant improvement on the MOS devices performances has been achieved with NO based treatments. Annealing or growing the oxide in nitric oxide (NO) reduces the interface state density near the conduction band in 4H-SiC by a factor of ten[43-45] and it improves the n-channel mobility significantly (35-70 cm^2/Vs) [42,46,47]. The NO anneal also affects interface states in the lower half of the band-gap[45]. The nitridation of $SiO_2/4H$-SiC in NO significantly reduces the interface trap near the conduction band; however, the effect saturates at ~2.5×10^{14} cm^{-2} of nitrogen, leaving a trap density that is still higher than silicon[48]. Trap passivation depends only on the nitrogen content and is independent of the annealing conditions.

4.2.3.   Oxides grown or annealed in N_2O

Nitrous oxide (N_2O) is by far preferred processing environment due to its availability and the high toxicity of pure NO. Identical chemical structures at the SiC-SiO_2 interface for gate oxides grown in either NO and N_2O ambient were found by x-ray photoelectron spectroscopy (XPS) analysis[49]. This is because N_2O can dissociate into NO, O_2 and N_2 at temperatures higher than 1000 ^{o}C. It is found that at high temperature N_2O decomposes according to the following two reactions:

$$N_2O \rightarrow N_2 + O_2 \qquad (4.7)$$

$$N_2O + O \rightarrow 2NO \qquad (4.8)$$
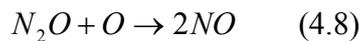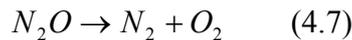
Most of the N_2O decomposes according to reaction (4.7) and only a very small amount of N_2O reacts according to reaction (4.8) [50]. NO is responsible for the beneficial effects, thus N_2O nitridation process optimization has been necessary to avoid (or at least minimize) any adverse effects related to the presence of oxygen during annealing or growth in N_2O. The initial results on gate oxides grown in 100% N_2O on SiC[41,50] were not encouraging as D_{it} and the near-interface trap density were increased. Several authors[44,45,51] have performed electrical and physical characterization of gate oxides on 4H-SiC grown in diluted N_2O. It has been suggested that the rates of carbon accumulation (due to oxidation) and carbon removal (due to nitridation) are closer in diluted N_2O, which results in the observed improvements. Analogously, Lipkin *et al.*[52], performed thermal dry and wet oxidation under several conditions and subsequent N_2O anneals improved drastically the channel mobility, especially in wet thermal oxides (25 cm^2/Vs). Nevertheless, other works[53-55] have not reported significant improvement using N_2O anneals in similar conditions.

Thermal oxides grown directly in Ar diluted N_2O have been fabricated and electrically characterized. Metal-oxide-semiconductor capacitors were fabricated on Si-faced, n-type 4H-SiC wafers with 5-μm-thick P-type epilayers with a doping level of $2.18 \cdot 10^{16}$ cm^{-3}, oriented 8° off the (0001) direction that were purchased from CREE Inc. Thermal oxides (10-20 nm thick) were prepared by three different processes: (1) growth in 10% of N_2O diluted in N_2 at 1300 °C during 90 min, (2) growth in 25% of N_2O diluted in Ar at 1300 °C during 90 min and (3) growth in 15% of N_2O diluted in Ar at 1300 °C during 90 min. The capacitors were characterized at room temperature using capacitance-voltage (C-V) measurements. The flat-band voltage, the oxide charge, the hysteresis behavior and the thickness of gate oxides grown in N_2O have been extracted using C-V measurements as it is shown in Fig. 4.10(a). Interface states density (D_{it}) analysis has been realized using both Terman method and conductance method near the conduction band. As it can be inferred from Fig. 4.10(b), the interface state density for nitridated oxides are similar in the depletion bias.
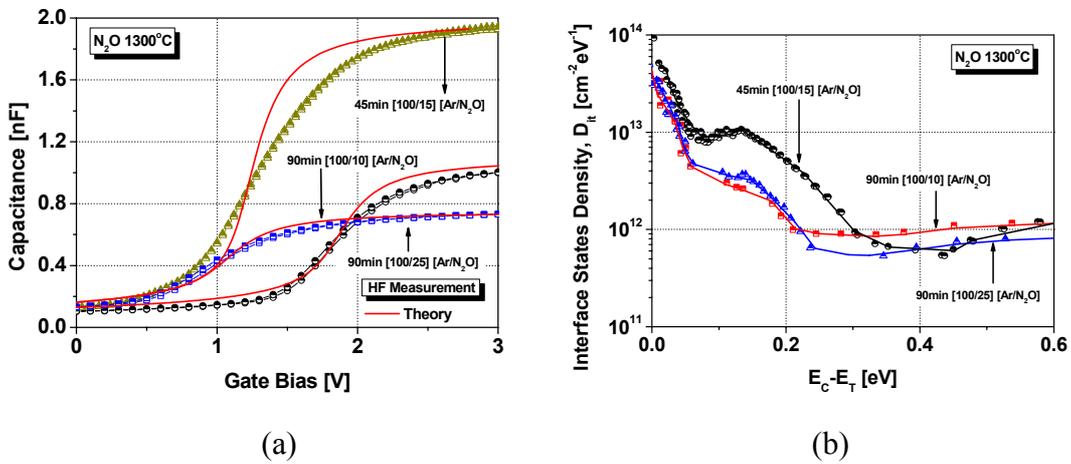
Fig. 4.10. (a) High-Frequency C-V curves for N_2O grown MOS structures. (b) Effect of N_2O nitridation ambient on D_{it} for 4H-SiC MOS capacitors.

The oxide thickness depends on both oxidation time and N_2O diluted concentration. The lower interface states density and oxide charges have been obtained with the process (2) (growth in 25% of N_2O diluted in Ar at 1300 °C during 90 min). Process (3) results in the thinner oxide, and the associated oxide charge and D_{it} is significantly higher when compared with the other two processes. These results suggest that a minimum thickness/oxidation time must be considered in order to achieve adequate electrical characteristics. The high interface traps density, for the gate oxides grown in diluted N_2O in Ar ambient, indicate that further efforts must be carried out as the D_{it} is not substantially reduced, when compared with the standard thermal oxidation.

The activation energy for dry oxidation of 4H-SiC is about 1 eV[56]. This low $E_{A/B}$ value was explained in terms of reduced solubility of the oxidants in the SiO_2 layer caused by an intermediate $SiC_{4-x}O_2$ layer or outdiffusing species. Quite significantly, Jamet *et al.*[44], found that the activation energy for oxidation in both NO and N_2O gases is much higher, on the order of 3 eV. According to an N_2O-growth model developed for silicon[57], the creation of Si≡N bonds at the interface reduces concentration growth sites, which is the reason for reduced oxidation rate in NO and N_2O when compared to the rate of dry oxidation (Fig. 4.11). Analogously, the growth rates in either NO or N_2O are limited by the concentration of growth sites at the SiC surface, and not by the solubility of the oxidizing species in the complex silicon oxycarbon layer (this layer is

almost eliminated in the nitridated oxides). This explains why $E_{A/B}$ for oxide growth in NO and N_2O are so different from $E_{A/B}$ for the dry oxidation, and so close to the energy of 3 eV needed to remove silicon from SiC, thus creating new growth sites.
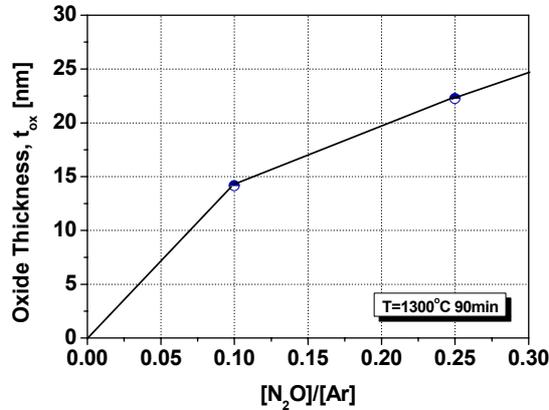
Fig. 4.11. Oxide thickness of 4H-SiC substrates oxidized in diluted N_2O as a function of the N_2O/Ar ratio at 1300 ºC during 90 min.

4.3. MOSFET fabrication

The metal-oxide-semiconductor field-effect transistor (MOSFET) is the building block of VLSI circuits in microprocessors and dynamic memories[58]. Because the current in a MOSFET is transported predominantly by carriers of one polarity only (e.g. electrons in an n-channel device), the MOSFET is usually referred to as a unipolar or majority-carrier device. The basic structure of a MOSFET is shown in Fig. 4.12.
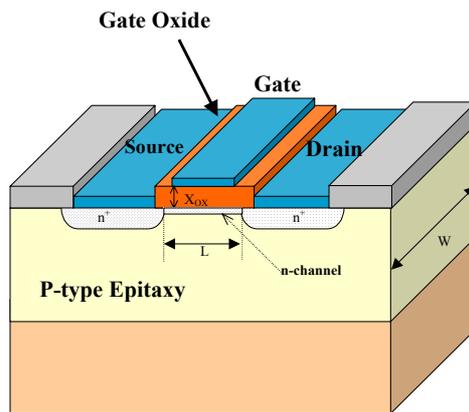
Fig. 4.12. Three-dimensional view of basic (n-channel) MOSFET device structure.

It is a four-terminal device with the terminals designated as *gate(G)*, *source(S)*, *drain(D)* and *substrate* or *body(B)*. An n-channel MOSFET, consists of a p-type SiC (or Silicon, GaAs,…) substrate into which two N^+ regions, the source and the drain, are formed (e.g. ion implantation). The gate electrode is usually made of metal or heavily dopped polysilicon and is separated by a thin insulator film, the *gate oxide*. The gate oxide is usually formed by thermal oxidation of SiC[59]. In VLSI circuits, a MOSFET is

surrounded by a thick oxide called the field oxide to isolate it from the adjacent devices. The surface region under the gate oxide between the source and the channel is called the channel region and is critical for current conduction in a MOSFET. The basic operation of a MOSFET device can be easily understood from the MOS capacitor discussed in *Chapter III*. When there is no voltage applied to the gate or when the gate voltage is zero, the p-type SiC surface is either in accumulation or depletion and there is not current flow between the source and drain. The MOSFET device acts like two back-to-back p-n junction diodes with only low-level leakage current present. When a sufficiently large positive voltage is applied to the gate, the SiC surface is inverted to n-type, which forms a conducting channel between the N^+ source and drain. If there is a voltage difference between them, an electron current will flow from the source to the drain. A MOSFET device therefore operates like a switch ideally suited for digital circuits. Since the gate electrode is electrically isolated from the substrate, there is no dc gate current, and the channel is capacitively coupled to the gate via the electric field in the oxide (hence the name field-effect transistor).

One of the key assumptions in any 1-D MOSFET model is the gradual channel approximation, which assumes that the variations of the electric field in the y-direction (along the channel) is much less than the corresponding variations in the x-direction (perpendicular to the channel). This allow us to reduce Poisson's equation to the 1-D form (x-component only). A charge-sheet approximation is introduced to obtain analytical expressions for the source-drain current in the linear and saturation regions (the surface channel vanishes at the drain end of the channel when saturation occurs). It assumes that all the inversion charge is located at the Silicon carbide surface like a sheet of charge and that there is no potential drop or band bending across the inversion layer.

For V_{GS} larger than V_{th}, a positive drain to source voltage V_{DS} causes a stream of electrons to flow out of the source and be swept into the drain. The source to drain current I_{DS} depends to first approximation on the mobility μ_{inv} of the charges in the channel, the drain to source voltage V_{DS} and the length of the channel[58]:

$$I_{DS} = \mu_{inv} C_I \frac{W}{L} (V_{GS} - V_{th}) V_{DS} \qquad (4.9)$$

The equation shows that the drain current varies linearly with V_{DS} for low drain bias. If V_{DS} is increased so that $V_{DS} \approx (V_{GS} - V_{th})$, the drain current I_{DS} saturates, because the drain voltage V_{DS} affects the channel bias near the drain and reduces the surface charge. The maximum of the drain current I_{DS} for a given V_{GS} is[58]:

$$I_{DSsat} = \frac{\mu_{inv} C_I}{2} \frac{W}{L} (V_{GS} - V_{th})^2 \qquad (4.10)$$

Occurs at the saturation voltage V_{DSsat}:

$$V_{DSsat} = (V_{GS} - V_{th}) + V_S \qquad (4.11)$$

where V_S is the source voltage.

4.3.1. The CNM SiC MOSFETs with thermally grown gate oxide

In this section, a brief description of the SiC prototype MOSFET layouts are given. n-channel enhancement mode MOSFETs in SiC substrates using a minimum of photolithographic steps have been fabricated during this work. The objective is to further evaluate the high quality gate oxides, characterized with MOS capacitors. The starting material is a p-type SiC wafer where an epitaxial layer has been grown with a doping level in the 1×10^{16} cm^{-3} to 1×10^{17} cm^{-3} range. The n-channel enhancement mode MOSFET structures can also be fabricated over a p-implanted region for CMOS and power applications. The p-type wells are created by an Aluminum or Boron multiple energy implant (energies ranging 25-320 keV) and posterior RTA (Rapid Thermal Annealing) at 1650 ^{o}C. The mask layout has been designed using the CADENCE environment. An alignment error of 1 μm and a minimum feature size of 4 μm have been assumed. The complete layout is shown in Fig. 4.13.
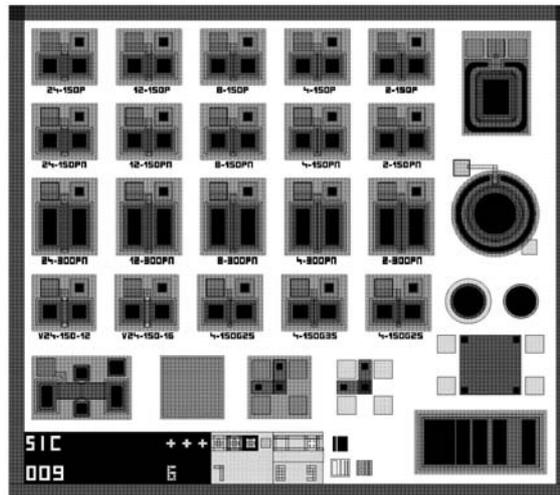
Fig. 4.13. Schematic diagram of the mask layout for SiC MOSFETs.

The electrical activation of dopants of SiC in the post implantation annealing step requires temperatures between 1400 ºC to 1700 ºC, which is too high for oxide, passivation, or metal layers. Therefore, the implantation annealing steps must be carried out at the beginning of the fabrication process. The masks set consists of 7 levels as follows[8]:

a) Plasma etch of registration/alignment marks. This step must be first, because the high temperature anneal does not permit the use of conventional reference patterns, required for the alignment of the following masks. However, this also permits changing the mask sequence for the manufacture of different processes.
b) P-well implant mask.
c) N^{+} implant mask for the definition of source and drain of MOSFET devices.
d) Gate active region definition.
e) Contact opening.
f) Contact metallization pattern.
g) Gate metallization pattern.

The main purpose of the lateral MOSFETs is to measure the mobility of carriers in the channel and the specific on-resistance. Therefore, they are designed with two common width W (300 and 150 μm) and different channel lengths L (2, 4, 8, 12, 24 μm). However the effective channel length, determined by the distance between source and drain (Fig. 4.12), depends on the lateral impurity dispersion, created by channeling effects during implantation and by diffusion during the high temperature anneal. Simulations have been carried out with a Montecarlo simulator developed at CNM[60] to optimize the implantation conditions and to minimize the effect of lateral channeling. It has been shown that lateral diffusion of the implanted nitrogen is negligible for annealing temperatures lower than 1700 ºC. The effective channel length is, therefore, supposed to be equal to the channel length designed in the mask layout. Apart from conventional MOSFET devices, other test structures are included in the layout, such as, enveloped geometry MOSFET, VMOS, combined TLM-Kelvin structures and Hall structures. Only MOS capacitors and MOSFET devices are studied in this thesis. MOS capacitors structures fabricated over the substrate and the p-well region are used to measure the oxide thickness, the effective oxide charge and the interface states density. The area of MOS capacitors is 400 μm x 400 μm.

During this thesis, MOS field-effect transistors with dry CNM gate oxide have been fabricated on both 6H-SiC and 4H-SiC substrates (Fig. 4.14). The performances of MOS transistors is determined in large part by the mobility of electron in the inversion layer. Therefore, special emphasis is focused on the characterization of the inversion channel field effect mobility μ_{FE}. The field effect mobility has been extracted for each transistor from the transconductance curves:

$$\mu_{FE} \equiv g_m \frac{L}{WC_I V_{DS}} \quad (4.12)$$

where $g_m = \frac{\partial I_{DS}}{\partial V_{GS}}$ is the transconductance and V_{DS} is the drain to source voltage.

(a)   (b)
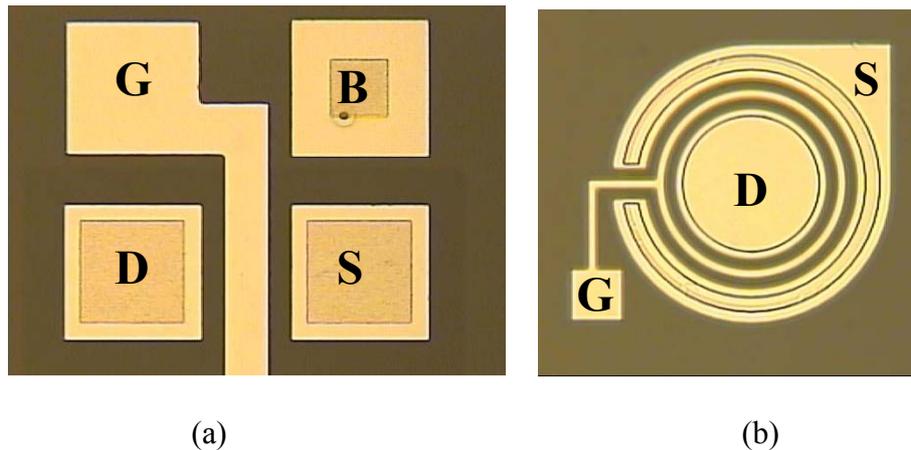
Fig. 4.14. Optical micrograph of one of the fabricated 4H-SiC MOSFET (a) test MOSFET with W =150 μm, (b) circular geometry MOSFET with W =1 mm.

The gate oxide of the 6H-SiC enhancement mode MOSFET devices is grown using the dry CNM standard oxidation process with the post-oxidation annealing and subsequent low temperature re-oxidation. The gate oxide thickness determined by C-V

measurements was 38 nm. The forward I-V characteristics are plotted in Fig. 4.15(a), for an epitaxial transistors with L =4 μm and W =150 μm.

(a)   (b)
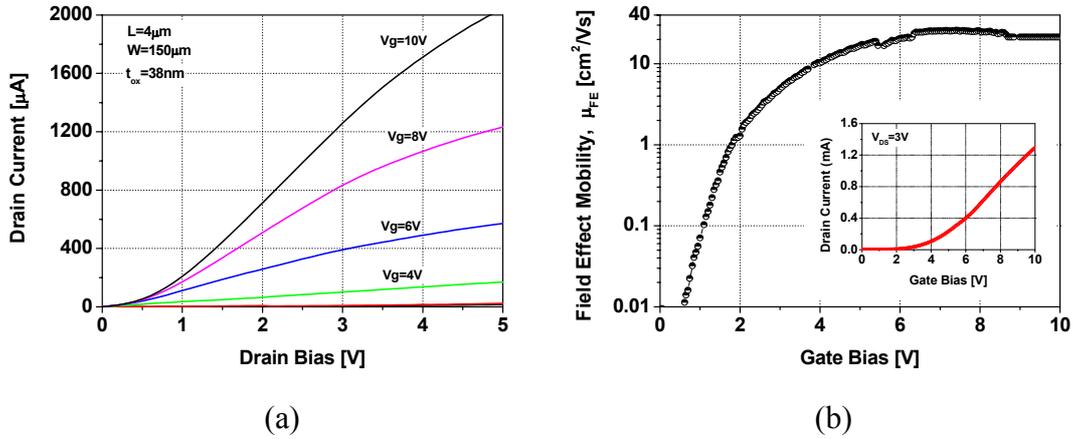
Fig. 4.15. (a) Forward I-V characteristics for standard dry oxidized gate oxide 6H-SiC epitaxial MOSFET. (b) Field effect mobility vs gate bias and transconductance curve.

Rectifying effect has been detected for lower drain voltages, although that the MOSFET is normally off with adequate subthreshold, direct and saturation characteristics. Threshold voltages of around V_{th} ~2.5 V have been routinely obtained for these devices. The value of field effect channel mobility has been extracted from transfer characteristics, measured at room temperature. For the MOSFETs fabricated on an epitaxial region, a peak mobility up to 26 cm^2/Vs has been measured, as it is shown in Fig. 4.15(b). This mobility value can be considered independent on the channel length/width ratio. However, slightly lower mobilities have been extracted for MOSFET devices on a p-implanted and annealed region.

Analogously, MOS field-effect transistors with dry CNM standard gate oxide have been fabricated on 4H-SiC substrates. The fabrication process is identical to the carried out for the 6H-SiC devices. The gate oxide thermally grown is again approximately 38 nm. The forward I-V characteristics are plotted in Fig. 4.16(a), for an epitaxial transistors with L =4 μm and W =150 μm.

(a)   (b)
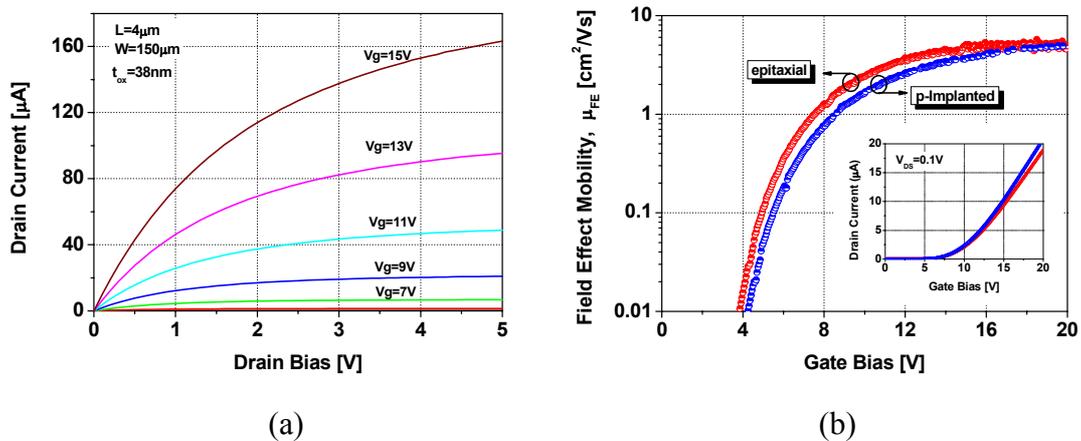
Fig. 4.16. (a) Forward I-V characteristics for standard dry oxidized gate oxide 4H-SiC epitaxial MOSFET. (b) Field effect mobility vs gate bias and transconductance curve.

Rectifying effect has been erased for lower drain voltages with an adequate post-deposition contact annealing. As occurs with the 6H-SiC devices, the MOSFET is normally off with adequate subthreshold, direct and saturation characteristics. Nevertheless, significant differences arises in the channel conduction properties. Threshold voltages is notably shifted to around $V_{th} \sim 6$ V. The value of field effect channel mobility has been extracted from transfer characteristics, measured at room temperature. For the MOSFETs fabricated on an epitaxial region, a lower (when compared with 6H-SiC devices) field-effect peak mobility of 5 cm^2/Vs has been extracted, as it is shown in Fig. 4.16(b). Other trends have been reproduced for 4H-SiC devices, i.e., the slightly lower mobilities extracted for MOSFET devices on a p-implanted and annealed region (Fig. 4.16(b)) or the lack of dependence on the channel length/width ratio (Fig. 4.17).

(a)   (b)
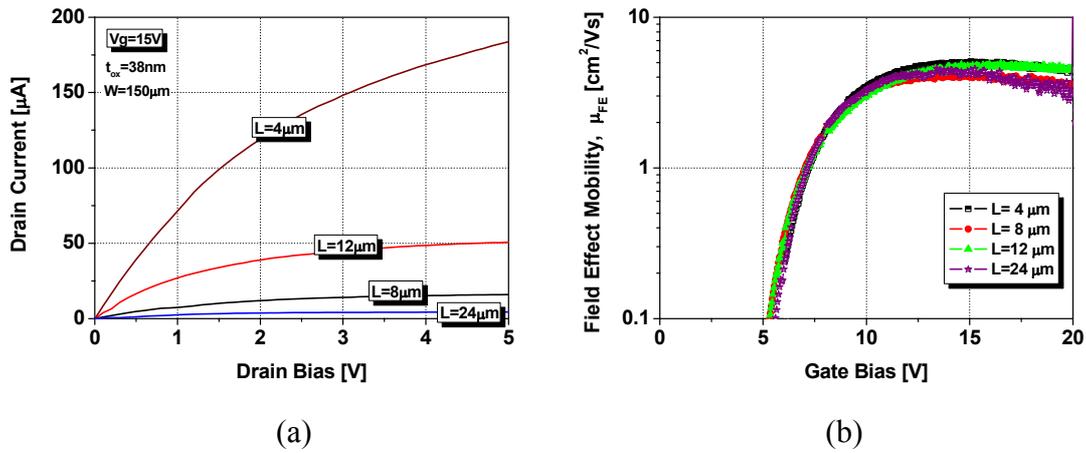
Fig. 4.17. (a) Forward I-V characteristics for standard dry oxidized gate oxide 4H-SiC epitaxial MOSFET for different channel lengths with a fixed gate bias. (b) Field effect mobility vs gate bias is almost independent of the channel length.

The MOS capacitor interface traps analysis indicates that the density of interface traps close to the semiconductor conduction band edge is at least an order of magnitude higher for 4H-SiC than in 6H-SiC. In 6H-SiC the oxide states coincide mostly with the states in the conduction band and they are only filled when the MOS structure is in strong accumulation. This is reflected in the fact that 6H-SiC n-channel MOSFETs have higher channel mobility that the ones made on 4H-SiC substrates, as it can be inferred from Fig. 4.18(a). This may come as a surprise, since the electron bulk mobility is higher in 4H-SiC than in 6H-SiC. It must be stressed that the oxide traps are also observed at the SiO$_2$/Si interface. In this case, however, they are well within the conduction band of silicon and therefore do not interfere with the operation of the silicon n-channel MOSFET. As well as the polytype, the epilayer substrate quality seems to play a fundamental role in the SiC MOSFET performances. 4H-SiC transistors were made on 8° off-axis Si face P$^+$ substrates with a 10 μm thick p-type chemical vapor deposition (CVD) commercial epilayer from CREE Inc. A second series of transistors were made using 8° off-axis Si face n$^+$ CREE substrates with a 72 μm thick p-type epilayer grown by sublimation, or physical vapor transport (PVT), at Linköping University. The main features of this technique have been reported[24] to be a high growth rate and improvement of the structural quality with thickness. Thus very thick layers are possible to grow with better structural quality compared to the substrate, and excellent surface morphology. In our case, as it can be inferred form Fig. 4.18(b), the field-effect

mobility is improved from 5 cm^2/Vs in the commercial CVD epilayers to 10 cm^2/Vs for the PVT grown epilayers from Linköping. Sveinbjörnsson *et al.*[24] attributed the high peak mobility to good surface morphology of the PVT grown epilayers resulting in less surface scattering and lower density of interface states, as compared to the reference CVD epilayers.

(a)   (b)
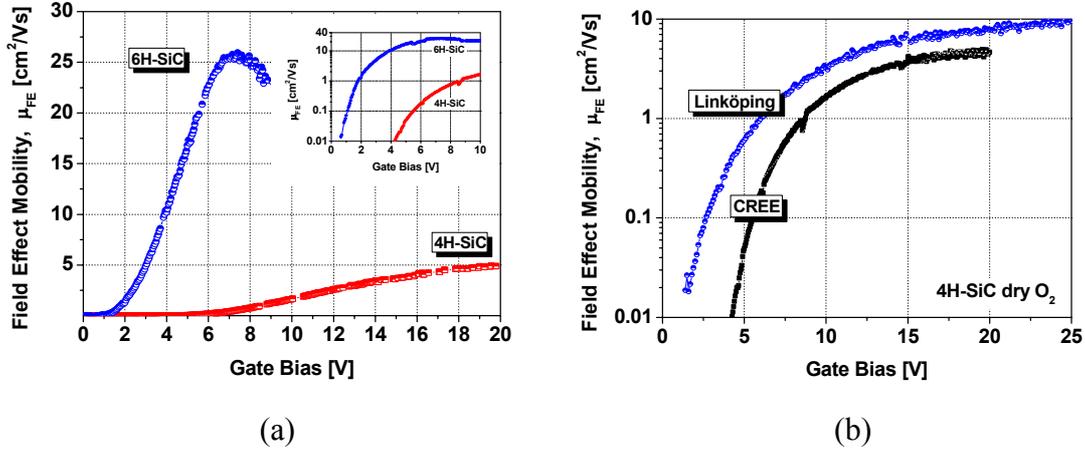
Fig. 4.18. Comparison of the field effect electron channel mobility for transistors made with standard dry oxidation (a) on 4H-SiC and 6H-SiC commercial substrates, (b) on 4H-SiC commercial CVD (CREE) and PVT substrates (Linköping).

One batch of n-channel MOSFETs with a standard gate thermal oxide followed by N$_2$O 1 h 1300 $^\circ$C annealing have been investigated and compared with the standard thermal oxide 4H-SiC reference MOSFETs. The forward I-V curves of one fabricated n-channel MOSFET are presented in Fig. 4.19(a).

(a)   (b)
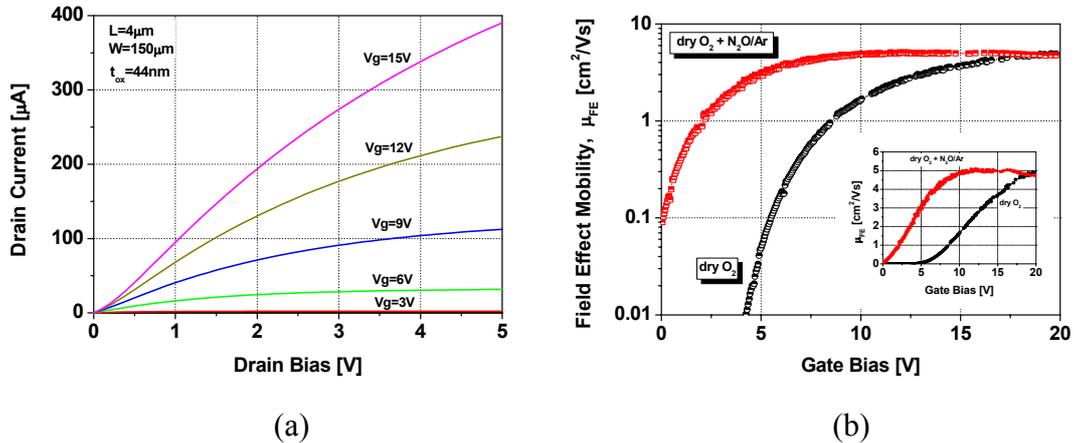
Fig. 4.19. (a) Forward I-V characteristics for standard dry oxidized and N$_2$O annealed gate oxide 4H-SiC MOSFET. (b) Comparison of the field effect electron channel mobility in transistors made using dry oxide and dry oxide annealed in N$_2$O.

As it can be derived from Fig. 4.19(b), where effective channel mobility is plotted versus gate voltage, the effective surface channel mobility of the 4H-SiC MOSFETs is almost the same using a dry thermal gate oxide with (~5 cm^2/Vs) or without (~4.5 cm^2/Vs) 1300 $^\circ$C N$_2$O anneal. However, there are significant differences in the MOSFET threshold voltages. For the dry O$_2$ + N$_2$O/Ar sample we obtained V_{th} ~1

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V while for the dry O_2 we obtained V_{th} ~6 V. The threshold voltage reduction along with the slightly improvement on the MOSFET mobility suggest that N_2O annealing would be effective diminishing only oxide charges and near interface traps. However, the interface traps have not been efficiently passivated with this treatments.

4.3.2.   The SiC MOSFETs state-of-the-art

In the previous sections, MOS capacitors have been used to establish the interface traps spectra within the bandgap for thermal oxidized gate oxides on 6H-SiC and 4H-SiC (0001)Si-face commercial substrates. It has also been listed some success additional/alternative treatments for the 6H- and 4H-SiC/oxide interface.

Face	μ_{FE} (cm²/Vs)	Gate dielectric	Year	Ref.
Lateral n-channel MOSFET on 4H-SiC				
Si	208	O_2 Contaminated Oxides (Al_2O_3) – on SGE [a]	2005	[24]
Si	160	LTO + wet ox 1100ºC + reox 950 ºC [b]	1998	[68]
Si	150	N_2O grown – Contaminated Oxides (Al_2O_3)	2004	[23]
Si	73	Contaminated Oxides (Al_2O_3) [c]	2000	[64]
Si	50-70	Cree nitridated Oxide [d]	2004	[46]
Si	48	Thermal oxide partially grown in NO	2002	[47]
Si	47	Dry ox 1200ºC + reox 950ºC	2002	[28]
Si	45	***Dry Ox 1050ºC + SiO₂-TEOS***	2005	*V*
Si	45	***Oxidized Ta₂Si gate oxide***	2005	*VI*
Si	37	Wet ox + NO anneal	2001	[42]
Si	30	Dry Ox + NO anneal	2001	[42]
Si	25	Wet ox + N_2O anneal	2002	[52]
Si	10	***CNM Dry ox on Linköping substrates***	2005	*IV*
Si	5-10	Dry ox 1200ºC	2002	[28]
Si	5-6	Wet ox	2000	[65]
Si	5	***CNM Dry ox on CREE substrates***	2005	*IV*
Si	5	Dry ox	2001	[42]
Si	5	Wet ox	2001	[42]
C	111	Wet ox + H_2 anneal 800ºC	2004	[32]
C	98	Wet reox	2004	[32]
C	16.8	Dry ox	2004	[32]
$(11\bar{2}0)$	216	***Dry Ox 1050ºC + SiO₂-TEOS***	2005	*V*
$(11\bar{2}0)$	110	Wet ox 1150ºC + H_2 anneal 800ºC	2002	[31]
$(11\bar{2}0)$	82-96	Wet ox	2000	[65]
$(11\bar{2}0)$	32	Wet ox 1150ºC	2002	[31]
$(03\bar{3}8)$	10	Wet ox	2002	[67]

Table IV.1. Peak field effect mobility for lateral planar inversion mode 4H-SiC MOSFETs found in the literature. [a]SGE: Sublimation grown epitaxy, [b]No reproduced, [c]Presumibly contaminated oxides[27], [d]Low substrate impurity concentration.

However, today the trap density is quite high (>10^{11} eV^{-1}cm^{-2}) regardless which processing technique is used. Analogously, MOSFET devices have been fabricated on

6H-SiC and 4H-SiC substrates, to evaluate the actual parameter that limits the SiC technology: the inversion channel mobility. 26 cm²/Vs and 5 cm²/Vs for the dry thermal gate oxides have been obtained on 6H-SiC and 4H-SiC, respectively. Some questions then arise, such as if the CNM dry thermal gate oxide is especially highly defective attending the extremely low values for the inversion channel mobility. Table IV.1 summarizes some of the recent published results on the peak field-effect mobility in lateral 4H-SiC MOSFETs, and can be considered as an state-of-the-art of the MOSFET mobilities (from Óllafson[27]). The low mobility value for dry thermal oxidized gate oxides at the CNM coincides with the commonly reported. Thus, there is nothing especially wrong in our oxides. The major breakthrough on 4H-SiC devices is the use of contaminated oxide with record high mobility of 208 cm²/Vs [24]. To date, only one group has reported such high mobility level. In recent years, nitridation has attracted the attention of many research groups. However, as it can be inferred from Table IV.1, the peak field-effect mobility value achieved with treatments based on Nitrogen incorporation has just reach 70 cm²/Vs (with low doped substrates)[46], and normally are in the range 30-50 cm²/Vs [28,42]. N_2O based treatments achieve even lower field effect mobilities, 25 cm²/Vs [52]. The relevance of our results becomes obvious looking at this table. Two of the treatments proposed further on in this thesis are presented. Deposited oxides based on SiO_2-TEOS (*Chapter V*) and an alternative high-*k* insulator (oxidized Ta_2Si, *Chapter VI*) are the more interesting innovative processes attending 4H-SiC MOSFET performances. Both processes have produced MOSFETs that enhances the field-effect mobility with thermally oxidized gate oxide and are even better than the common reported MOSFET devices with nitridation. In particular, the mobility peak achieved (216 cm²/Vs) for (11-20) 4H-SiC MOSFETs with SiO_2-TEOS improves all the previous results for this orientation. Moreover, oxide metallic contamination or nitrogen incorporation can be eventually implemented in these novel processes in order to increase further the MOSFET channel conduction.

One alternative device design to the inversion mode MOSFET is the buried channel MOSFET. Here, the channel region is ion implanted, making the channel n-type up to a certain depth. Usually, this will make the threshold voltage negative resulting in a normally-on device, which is considered a disadvantage by the circuit designer. However, by carefully choosing the depth and dose of ion implant it is possible to obtain a normally-off device. Such devices have been demonstrated with a peak field-effect mobility of above 202 cm²/Vs with a threshold voltage of 1.3 V [61]. Table IV.2 summarizes some of the recent published results on the peak field-effect mobility in buried channel 4H-SiC MOSFETs.

Face	μ_{FE} (cm²/Vs)	Gate dielectric	Year	Ref.
Buried Channel MOSFET on 4H-SiC				
Si	202	Dry ox + Deposited Oxide	2002	[61]
Si	140	Dry ox 1200ºC + reox 950ºC	2001	[63]
$(11\bar{2}0)$	216	Wet ox 1150ºC + H_2 anneal 800ºC	2002	[66]

Table IV.2. Peak field effect mobility for buried channel 4H-SiC MOSFETs found in the literature.

A disadvantage of the buried channel MOSFET is that for higher gate voltage the field effect mobility drops rapidly. SiC MOSFETs with buried channel show the

strong effect of the interface on the electrical characteristics, if the channel is located adjacent to the interface when compared with a conventional MOSFET. Hence, with this alternative design the field-effect mobility is increased but the interface problem still remains.

As stated before, the 4H-SiC polytype is considered the best candidate to the future SiC MOS device. Other polytypes are constantly being considered, and these include 6H-SiC, 3C-SiC and 15R-SiC. Table IV.3 presents some of the recent published results on the peak field-effect mobility in lateral 6H-SiC MOSFETs. As inferred from the table, the CNM dry thermal oxidation is again in the sate-of-the-art. The optimization of the 6H-SiC/SiO$_2$ interface is out of the scope of this thesis.

Face	μ_{FE} (cm^2/Vs)	Gate dielectric	Year	Ref.
		Lateral n-channel MOSFET on 6H-SiC		
Si	130	Contaminated Oxides (Al$_2$O$_3$)	2005	[25]
Si	110	LTO + wet ox 1100ºC + reox 950ºC[a]	1998	[68]
Si	72	ONO	1999	[9,69]
Si	40-50	Wet ox 1025ºC + reox 950ºC	1999	[9,69]
Si	45	Wet ox	2000	[65]
Si	43	N$_2$O grown oxide	2005	[25]
Si	25	***CNM Dry ox on CREE substrates***	2005	*IV*
Si	24	Thermal oxide 1100ºC	1999	[13]
(11$\bar{2}$0)	36-116	Wet ox 1150ºC	2000	[65]

Table IV.3. Peak field effect mobility for lateral planar inversion mode 6H-SiC MOSFETs found in the literature. [a]No reproduced.

Face	μ_{FE} (cm^2/Vs)	Gate dielectric	Year	Ref.
		Lateral n-channel MOSFET on 3C-SiC		
3C	229	Wet 1100ºC + reox	2003	[16]
3C	165	Wet 1150ºC + reox	2002	[70]
		Lateral n-channel MOSFET on 15R-SiC		
15R	50	Wet ox	1996	[9,69]
15R	47	Dry ox	1996	[9,69]
15R	33	Thermal oxide 1100ºC	2000	[65]

Table IV.4. Peak field effect mobility for lateral planar inversion mode 3C- and 15R-SiC MOSFETs found in the literature.

Table IV.4 presents some of the recent published results on the peak field-effect mobility in lateral 3C-SiC and 15R-SiC MOSFETs. Currently the most promising polytype is 3C-SiC, where record high n-channel mobilities of 229 cm^2/Vs have been achieved[16]. This correlated with the low density of interface traps found near the conduction band edge. The reason the 3C-SiC MOSFET has not achieved supremacy is due to the low quality of the 3C-SiC single crystalline material. Again, the extensive study of the 3C-SiC/oxide interface is not considered in this thesis, but it would be an exciting challenge for further investigations.

4.4. Conclusions

In a manner similar to Si, SiC forms a SiO_2 layer at the surface when exposed to O_2 (dry oxidation) or H_2O (wet oxidation) at high temperature. Oxide layers are needed for several applications, including the fabrication of MOS structures and MOSFET transistors which is the first step towards integration. It is generally believed that most of the carbon is removed from the oxide as $CO_{(g)}$ or $CO_{2(g)}$. SiC offers a high resistance to thermal oxidation which requires temperatures higher than 1000 ºC to be practical. The oxidation kinetics of SiC is described by the same kinetics rules as the oxidation of Si, defined by Deal and Grove.

In the *(CNM) standard thermal oxidation*, developed for high quality SiC oxides oxidation is carried out at 1000-1175 ºC in pure oxygen (180 min) with in-situ argon anneal (60 min) at the oxidation temperature. After the anneal, the temperature is ramped down (5 ºC/min) in argon to 950 ºC and a reoxidation in dry or wet O_2 ambient is carried out for 180 min.

MOS capacitors have been fabricated to establish the insulator charge and the interface traps spectra within the bandgap for thermal oxidized gate oxides. Moderate insulator charge and high interface traps density is achieved for thermally grown oxides on (0001) 4H-SiC substrates. Experimental results aim at a significant increase of interface traps when approaching to the conduction band with D_{it} of 1×10^{12} $eV^{-1}cm^{-2}$ ($E_C - E_T$ =0.2 eV) on n-type substrates, and 1×10^{13} $eV^{-1}cm^{-2}$ ($E_T - E_V$ =0.2 eV) on p-type substrates. No significant improvements have been achieved when compared a wet standard thermal oxidation with standard dry thermal oxidation. Better interface characteristics have been obtained for thermally grown oxides on (0001) 6H-SiC n-type substrate with D_{it} of 1×10^{11} $eV^{-1}cm^{-2}$ ($E_C - E_T$ =0.2 eV). Dry thermal oxidation on no commercial (however one of the best available) n-type 3C-SiC substrates has been also performed. Very high roughness, high current leakage, high insulator traps and high interfacial traps density have been obtained for these capacitors with D_{it} of 1×10^{13} $eV^{-1}cm^{-2}$ ($E_C - E_T$ =0.2 eV).

It has been reported for several groups that *nitridation* (thermal oxidation in NO or N_2O ambient) provides an effective technique for reducing D_{it} in SiO_2/4H-SiC near the conduction band. However, experimental results for gate oxides grown or annealed on (0001) 4H-SiC in diluted N_2O in Ar ambient, indicate that further efforts must be carried out as the D_{it} is not substantially reduced, when compared with the standard thermal oxidation.

Analogously, MOSFET devices have been fabricated on 6H-SiC and 4H-SiC substrates, to evaluate the actual parameter that limits the SiC technology: the inversion channel mobility. 26 cm^2/Vs and 5 cm^2/Vs for the dry thermal gate oxides have been obtained on 6H-SiC and 4H-SiC, respectively. The low mobility value for dry thermal oxidized gate oxides at the CNM coincides with the commonly reported literature values. Thus, there is nothing especially wrong in our oxides.

Additional/alternative treatments for the 6H- and 4H-SiC/oxide interface listed in the literature have revealed some discreet success. However, today the trap density is quite high (>10^{11} $eV^{-1}cm^{-2}$) regardless which processing technique is used. The major breakthrough on (0001) 4H-SiC devices it the use of contaminated oxide with record high mobility of 208 cm^2/Vs. To date, only one group has reported such high mobility level. In recent years, nitridation has attracted the attention of many research groups. However, the peak field-effect mobility value achieved with treatments based on

Nitrogen incorporation has just reach 70 cm^2/Vs (with low doped substrates), and normally are in the range 30-50 cm^2/Vs. N$_2$O based treatments achieve even lower field effect mobilities, 25 cm^2/Vs. The main reason why the (0001) Si face is preferred, is that the epitaxial growth techniques are more developed. However, studies on other crystal faces have shown that is possible to achieve high mobility on other faces. The (11-20) face has demonstrated promising results (up to 110 cm^2/Vs) and on the C-face mobility values above 111 cm^2/Vs have been demonstrated. Currently the most promising polytype is 3C-SiC, where record high n-channel mobilities of 229 cm^2/Vs have been achieved. This correlated with the low density of interface traps found near the conduction band edge. The reason the 3C-SiC MOSFET has not achieved supremacy is due to the low quality of the 3C-SiC single crystalline material.

References

[1]   C. Raynaud, *J. Non-Cryst. Solids*, **280**, 1, (2001).

[2]   V. V. Afanas'ev, F. Ciobanu, S. Dimitrijev, G. Pensl, and A. Stesmans, *Mater. Sci. Forum* **483-485**, 563, (2005).

[3]   E. G. Stein Von Kamienski, F. Portheine, J. Stein, A. Gölz, and H. Kurtz, *J. Appl. Phys.* **79**, 2529, (1996).

[4]   C. I. Harris, and V. V. Afanas'ev, *Microelectron. Engineering,*, **36**,167, (1997).

[5]   L. Muehloff, M. J. Bozack, W. J. Choyke, and J. T. Yates, *J. Appl. Phys.* **60**, 2558, (1986).

[6]   C. D. Fung, and J. J. Kopanski, *Appl. Phys. Lett.* **45**, 757, (1984).

[7]   B. E. Deal, and A. S. Grove, *J. Appl. Phys.* **36**, 3770, (1965).

[8]   S. Berberich, *SiC Processing Technology for Fabricating MOSFET Devices and Micromachined Condenser Microphones*. Thesis dissertation. CNM, Spain and Technishe Universität of Darmstadt, Germany, (2004).

[9]   L. A. Lipkin, and J. W. Palmour, *J. Electr. Mater.*, **25**, 909, (1996).

[10]   E. H. Nicollian, and J. R. Brews, *MOS Physics and Technology*, Wiley, New York, (1982).

[11]   P. Friedrichs, E. P. Burte, and R. Schörner, *J. Appl. Phys.* **79**, 7814, (1996).

[12]   G. L. Harris, *Properties of Silicon Carbide*, INSPEC, London, (1995).

[13]   R. Shörner, P. Friedrichs, D. Peters, and D. Stephani, *IEEE Electron Device Lett.* **20**, 241, (1999).

[14]   N. Saks, S. S. Mani, and A. K. Agarwall, *Appl. Phys. Lett.* **76**, 2250, (2000).

[15]   V. V. Afanas'ev, M. Bassler, G. Pensl, and M. Schulz, *Phys. Stat. Sol.(a)* **162**, 321, (1997).

[16]   K. K. Lee, Y. Ishida, T. Ohshima, K. Kojima, Y. Tanaka, T. Takahashi, H. Okumura, K. Arai, and T. Kamiya, *IEEE Electron Device Lett.* **24**, 466, (2003).

[17]   S. M. Tang, W. B. Berry, R. Kwor, M. V.Zeller, and L. G. Matus, *J. Electrochemical Soc.* **137**, 221, (1990).

[18]   T. Ouisse, N. Bécourt, C. Jaussaud, and F. Templier, *J. Appl. Phys.* **75**, 6304, (1994).

[19]   J. A. Cooper, *Phys. Stat. Sol.(a)* **162**, 305, (1997).

[20]   S. Zaima, K. Onoda, Y. Koide, and Y. Yasuda, *J. Appl. Phys.* **68**, 6304, (1990).

[21]   H. Yano, F. Katafuchi, T. Kimoto, and H. Matsunami, *IEEE Trans. Elect. Dev.* **46**, 504, (1999).

[22]   L. A. Lipkin, D. B. Slater Jr, and J. W. Palmour, *Mater. Sci. Forum* **264-268**, 853, (1998).

[23]   G. I. Gudjonsson, H. Ö. Ólafsson, and E. Ö. Sveinbjörnsson, *Mater. Sci. Forum*, **457-460**, 1425, (2004).

[24]   E.Ö.Sveinbjörnsson, H. Ö. Ólafsson, G. Gudjónsson, F.Allerstam, P.-Å. Nilsson, M. Syväjärvi, R. Yakimova, C. Hallin, T. Rödle, and R. Jos, *Mater. Sci. Forum* **483-485**, 841, (2005).

[25]   F. Allerstam, G. Gudjónsson, H. Ö. Ólafsson, E. Ö. Sveinbjörnsson. T. Rödle, and R. Jos, *Mater. Sci. Forum* **483-485**, 837, (2005).

[26]   D. Alok, E. Arnold, R. Egloff, and S. Mukherjee, United States Patent and Trademark Office 6,559,068 (2003).

27   H. Ö. Ólafsson, *Detection and removal of traps at the SiO₂/SiC interface*. Thesis dissertation. Chalmers University of Technology, Sweden, (2004).

28   R. Kosugi, M. Okamoti, S. Suzuki, J. Senzaki, S. Harada, K. Fukuda, and K. Aral, *Mater. Sci. Forum* **389-393**, 1049, (2002).

29   E. S. von Kamienski, A. Gölz, and H. Kurz, *Mater. Sci. Eng. B*, **29**, 131, (1995).

30   K. Fukuda, S. Suzuki, T. Tanaka, and K. Arai, *Appl. Phys. Lett*. **76**, 1585, (2000).

31   J. Senzaki, K. Kojima, S. Harada, R. Kosugi, S. Suzuki, T. Suzuki, and K. Fukuda, *IEEE Electron Device Lett.* **23**, 13, (2002).

32   K. Fukuda, M. Kato, K. Kojima, and J. Senzaki, *Appl. Phys. Lett*. **84**, 2088, (2004).

33   N. N. Singh, and A. Rys, *J. Appl. Phys.* **73**, 1279, (1993).

34   A. Rys, N. N. Singh, and M. Cameron, *J. Electrochemical Soc.* **142**, 1318, (1995).

35   K. McDonald, L. C. Feldman, R. A. Weller, G. Y. Chung, C. C. Tin, and J. R. Williams, *J. Appl. Phys.* **93**, 2257, (2003).

36   R. J. Wu, and C. T. Yeh, *Int. J. Chen. Kinet.*, **28**, 89, (1996).

37   N. M. Laurendeau, *Combust. Sci. Technol.*, **11**, 89, (1975).

38   B. Hornetz, H-J. Michel, and Halbritter, *J. Mater. Res.*, **9**, 3088, (1994).

39   K. C. Chang, N. T. Nuhfer, L. M. Porter, and Q. A. Wahab, *Appl. Phys. Lett*. **77**, 2186, (2000).

40   G. G. Jernigan, R. E. Stahlbush, M. K. Das, J. A. Cooper, Jr., and L. A. Lipkin, *Appl. Phys. Lett*. **74**, 1448, (1999).

41   H.-F. Li, S. Dimitrejev, H. B. Harrison, and D. Sweatman, *Appl. Phys. Lett*. **70**, 2028, (1997).

42   G. Y. Chung, C. C. Tin, J. R. Williams, K. McDonald, R. K. Chanana, R. A. Weller, S. T. Pantelides, L. C. Feldman, O. W. Holland, M. K. Das, *IEEE Electron Device Lett.* **22**, 176, (2001).

43   G. Y. Chung, C. C. Tin, J. R. Williams, K. McDonald, M. Di Ventra, S. T. Pantelides, L. C. Feldman, R. A. Weller, *Appl. Phys. Lett*. **76**, 1713, (2000).

44   P. Jamet, S. Dimitrijev, and P. Tanner, *J. Appl. Phys*. **90**, 5058, (2001).

45   V. V. Afanas'ev, A. Stesmans, F. Ciobanu, G. Pensl, K. Y. Cheong, and S. Dimitijev, *Appl. Phys. Lett*. **86**, 568, (2003).

46   M. K. Das, *Mater. Sci. Forum* **457-460**, 1275-1279, (2004).

47   R. Schörner, P. Friedrichs, D. Peters, D. Stephani, S. Dimitrijev, and P. Jamet, *Appl. Phys. Lett*. **80**, 4253, (2002).

48   K. McDonald, R. A. Weller, S. T. Pantelides, L. C. Feldman, G. Y. Chung, C. C. Tin, and J. R. Williams, *J. Appl. Phys*. **93**, 2719, (2003).

49   P. Jamet, and S. Dimitrijev, *Appl. Phys. Lett.,* **79**, 323, (2001).

50   R. C. De Meo, T. K. Wang, T. P. Chow, D. M. Brown, and L. G. Matus, *J. Electrochem. Soc.*, **141**, 150, (1994).

51   K. Y. Cheong, S. Dimitrijev, J. Han, and H. B. Harrison, *J. Appl. Phys.*, **93**, 5682, (2003).

52   L. A. Lipkin, M. K. Das, and J. W. Palmour, , *Mater. Sci. Forum* **389-393**, 985, (2002).

53   S. Chakraborty, P. T. Lai, J. P. Xu, C. L. Chan, and Y. C. Cheng, *Solid State Electron.*, **45**, 471, (2001).

54   J. P. Xu, P. T. Lai, and C. L. Chan, *Solid State Electron.*, **47**, 1397, (2003).

55 W. Wang, T. P. Chow, R. J. Gutman, T. Issacs-Smith, J. Williams, K. A. Jones, A. Lelis, W. Tripton, S. Scozzie and A. Argarwal, *Mater. Sci. Forum* **457-460**, pp. 1309, (2004).

56 A. Gölz, G. Horstmann, E. Stein von Kamienski, and H. Kurz, *Proccedings of the International Conference on SiC and Related Materials*, Kyoto, Japan, 18-21 September 1995. *IOP conference Series* **142**, pp. 725, (1996).

57 S. Dimitrijev, and H. B. Harrison, *J. Appl. Phys.*, **80**, pp. 2467, (1996).

58 Y. Taur, T. H. Ning, *Fundamentals of Modern VLSI Devices*, Cambridge University Press, UK, (1998).

59 J. Shenoy. *Basic MOS Studies for Silicon Carbide Power Devices*. Ph. D. Thesis, Purdue University, (1996).

60 E. Morvan, P. Godignon, J. Montserrat, J. Fernández, D. Flores, J. Millán, and J. P. Chante. *Mat. Sci. and Eng. B* **42**, pp. 218, (1997).

61 S. Keneko, H. Tanaka, Y. Shimoda, N. Kiritani, S. Tanimoto, M. Yamanaka and M. Hoshi, *Mater. Sci. Forum* **389-393**, pp. 1073-1076, (2002).

62 S. Sridevan and B. J. Baliga, *IEEE Electron Device Lett.* **19**, pp. 228-230, (1998).

63 S. Harada, S. Suzuki, J. Senzaki, R. Kosugi, K. Adachi, K. Fukuda, and K. Arai, *IEEE Electron Device Lett.* **22**, pp. 272, (2001).

64 D. Alok, E. Arnold, and R. Egloff, *Mater. Sci. Forum* **338-342**, pp. 1077-1080, (2000).

65 H. Yano, T. Kimoto, H. Matsunami, M. Bassler, and G. Pensl, *Mater. Sci. Forum*, **338-342**, pp. 1109, (2000).

66 J. Senzaki, K. Fukuda, K. Kojima, S. Harada, R. Kosugi, S. Suzuki, and K. Arai, *Mater. Sci. Forum*, **389-393**, pp. 1061, (2002).

67 T. Hirado, H. Yano, T. Kimoto, H. Matsunami, and H. Shiomi, *Mater. Sci. Forum*, **389-393**, pp. 1065, (2002).

68 S. Sridevan, and B. J. Baliga, *Mater. Sci. Forum*, **264-268**, pp. 997, (1998).

69 L. A. Lipkin, and J. W. Palmour, *IEEE Trans. Elect. Dev.* **46**, pp. 525, (1999).

70 J. Wan, M. A. Capano, M. R. Melloch, and J. A. C. Jr., *IEEE Electron Device Lett.* **23**, pp. 482, (2002).

Chapter V

Deposited a-SiO$_x$ as gate dielectric

The high density of defects encountered at the SiC/SiO$_2$ interface represents a major obstacle in the successful fabrication of MOS electronic devices. The origin of these defects has been invoked to be the formation of Silicon oxycarbide or Carbon clusters at or near the interface[1] during the oxidation. Hence, the use of alternative techniques, such as the SiO$_2$ deposition, in SiC MOS gated devices is currently under exhaustive investigation. The deposition of high quality insulator layers allows avoiding the problems related with the Carbon liberation during the thermal oxidation. Moreover, all these techniques avoid the anisotropy of oxidation rate experienced during thermal oxidation. Deposited oxides have been used as gate material on SiC devices during the last years, but not widely. The deposition method (based on Chemical Vapor Deposition, CVD) and conditions varies strongly depending the author, and includes PECVD[2,3] (Plasma enhanced CVD), LTO[4-7] (Low Temperature Oxides), JVD[8,9] (Jet Vapor Deposition), RTCVD[10] (Rapid Thermal CVD) or LPCVD[11-16] (Low Pressure CVD). In this chapter, deposited oxides with different techniques have been used for the gate fabrication of MOS and MOSFET devices. The actual stoichiometry of the deposited silica is very difficult to determine. However, the scope of this chapter is the electrical performances and its feasibility for MOSFET fabrication. Therefore, although the academic notation for deposited silicon dioxide would be (amorphous) *a-SiO$_x$*, the term *SiO$_2$* will be used to refer the deposited insulator in this chapter.

5.1. a-SiO$_x$ layers from PECVD with SiH$_4$ and N$_2$O as precursors

CVD is the formation of a film on a surface from a volatile precursor (vapor or gas), as a consequence of one or more chemical reactions which change the state of the precursor[18]. Many different films can be deposited: elements and compounds, crystalline, polycrystalline and amorphous. Most films can be deposited from several different precursor systems. Plasma discharge can be used to help things along, or the substrate and/or the gas can be heated or cooled. By varying the experimental condition

such as the substrate temperature, composition of the reaction gas mixture, total pressure and gas flows, materials with different properties can be grown. Each film has an optimal set of characteristics techniques. Nevertheless, in every case, CVD processes must:

- Provide a volatile precursor containing the constituents of the film
- Transport that precursor to the deposition surface
- Encourage or avoid reaction in the gas phase.
- Encourage surface reactions that form the film
- And do it rapidly, reproducibly, and uniformly for industrial applications.

The deposition process can be activated by temperature (CVD), laser (LCVD), photo induced (PCVD) or plasma (PECVD). A plasma is a partially ionized gas. Plasma-enhanced chemical vapor deposition is a powerful tool for many film deposition processes that cannot be achieved with temperature control alone or low temperature conditions. Fig. 5.1 shows the schematic of a PECVD equipment. The gas pressure inside the deposition chamber has also a great influence on the kinetic of the process. Hence, the CVD deposition processes can be classified taking into account the pressure in the deposition chamber as ultra-high-vacuum (UHT-CVD), low pressure (LPCVD) or atmospheric pressure CVD (APCVD).
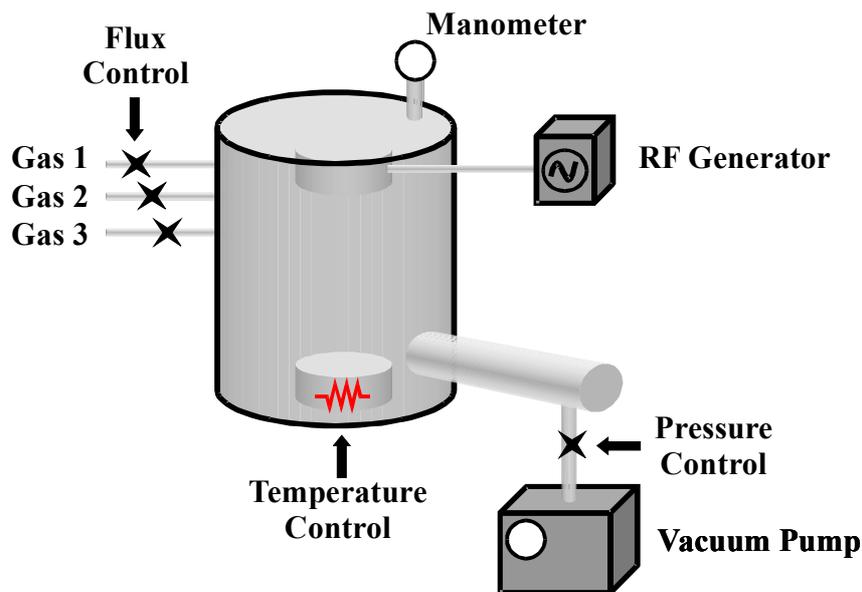
Fig. 5.1. Schematic of a (rf-) PECVD equipment.

One of the most common Silicon volatile precursor for a-SiO$_2$ CVD deposition is Silane (SiH$_4$). Silane (more properly monosilane), is a gas at room temperature and is moderately toxic, but explosion hazards are usually more severe. The basic overall reaction for the deposition of silicon dioxide from Silane in a thermal process[17] requires the removal of the hydrogen atoms and addition of two oxygen atoms (Fig. 5.2). When oxygen is present is excess, water is the main byproduct (APCVD), whereas in low-oxygen conditions, hydrogen will be produced (LPCVD). Because the heat of formation of Silane is small and that of silicon dioxide is large, this process is very exothermic. In general, many radicals (such as the biradical SiH$_2$) are produced and branching chains

are certainly possible. At the surface, these various reactive compounds tend to stick readily, giving high roughness and mediocre conformality. Once they are in place on the surface, additional "condensation" reactions must occur to remove the excess hydrogen and form the bridge bonds of the oxide film, with water or hydrogen being produced. Hence, in moderately oxidizing conditions Si-H will be present in the film. When copious oxygen is present during growth the films contains Si-OH. Excessive H in the films can lead to various problems. For example, oxides containing large amount of Si-OH are more hygroscopic, and readily absorb water molecules from the air. The water can migrate through the deposited materials to the gate oxide yielding reducing reliability and creating hot electron phenomena.
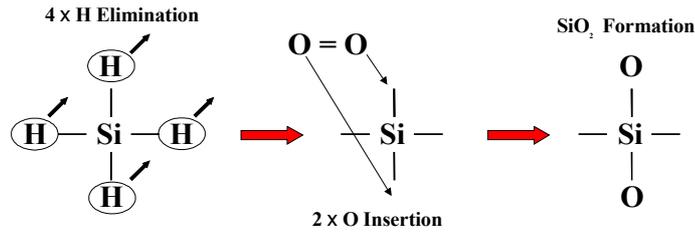
Fig. 5.2. The basic overall reaction for the deposition of silicon dioxide from Silane in a thermal process

N$_2$O is employed in PECVD reactors as an oxidant instead of O$_2$ since pure Oxygen is typically found to be too reactive and can produce lost of powder[19]. The films properties are fairly similar to those obtained using thermal CVD from Silane; conformality is generally poor to mediocre. However, the addition of the plasma enhances rather easy control of film stoichiometry, ranging from amorphous silicon to nearly pure silicon dioxide, by varying the gas mixture and flows.

5.1.1. The CNM PECVD with SiH$_4$ and N$_2$O as precursors - Experimental Details

N-type 4H-SiC 8°-off Si face substrates with 10 μm thick epilayers were used in this study. The net donor concentration ranging form 8.5×10^{15}-3×10^{16} cm^{-3}. Prior to deposition the sample were cleaned by RCA method. Then the samples were loaded into a plasma enhanced chemical vapor deposition (PECVD) apparatus to form SiO$_2$ films. Films with 100-110 nm thickness were obtained with deposition time of 5 min with the parameters listed in Table V.1.

Process	Thick. [nm]	Temp.	Pressure	Time	Flow Rates	Others
rf- PECVD	100	350 ºC	3 Torr	5 min	100% Ar 10% O$_2$/H$_2$ 10% SiH$_4$/Ar (1%)	RF power: 50 W

Table V.1. Summary of the PECVD SiO$_2$ deposition parameters.

To enhance the global performance of the films further, thermal post-deposition annealing have been performed on the samples. Deposited oxides often have strained bonds and reduced density. At temperatures of around 650 ºC to 700 ºC, local structural readjustments become possible. Oxides annealed at temperatures above 700 ºC for a

few minutes are normally found to be "densified", with reduced hydrogen content, removal of H$_2$O and improved stability in subsequent annealings. However, very high temperatures indeed are necessary to completely remove moisture and erase all memory of the deposited structure. Hence, isolated Si-OH will survive anneals at over 1000 ºC, presumably because there's nowhere for the hydrogen to go, as it needs to find another hydrogen to be removed as H$_2$ or even H$_2$O. Therefore, the electrical characteristics of the layers as deposited and after a short time (5 min) post-deposition annealing in N$_2$O at high temperature (1050-1150 ºC) have been analyzed. The samples are loaded in N$_2$O at 750 ºC and the temperature is raised to the post-deposition annealing temperature.

5.1.2. MOS Physical and Electrical characteristics

C-V measurements have been performed on the MOS structures fabricated using a mercury probe. Fig.5.3(a) shows the high frequency (20 kHz) C-V characteristics measured for one sample before and after the post deposition annealings. As it can be inferred from the figure, the as deposited sample presents higher flat band voltage (an indication of oxide traps) and higher stretch in the CV traces (an indication of high interface traps density). Precise fitting of the theoretical with experimental traces for high frequency C-V curves has been successfully obtained, especially for the annealed sample. A small hysteresis behaviour, evidencing the low formation rate of slow traps in the interface, has been detected in both the as deposited and annealed samples, but is also higher in the first one. By varying the deposition conditions, different oxide thicknesses have been obtained as derived from Fig. 5.3(b). However, independently of the thickness of the deposited SiO$_2$ layer, the same trends are observed for the annealed samples: the reduction of flat-band voltage, stretch and hysteresis.

(a)   (b)
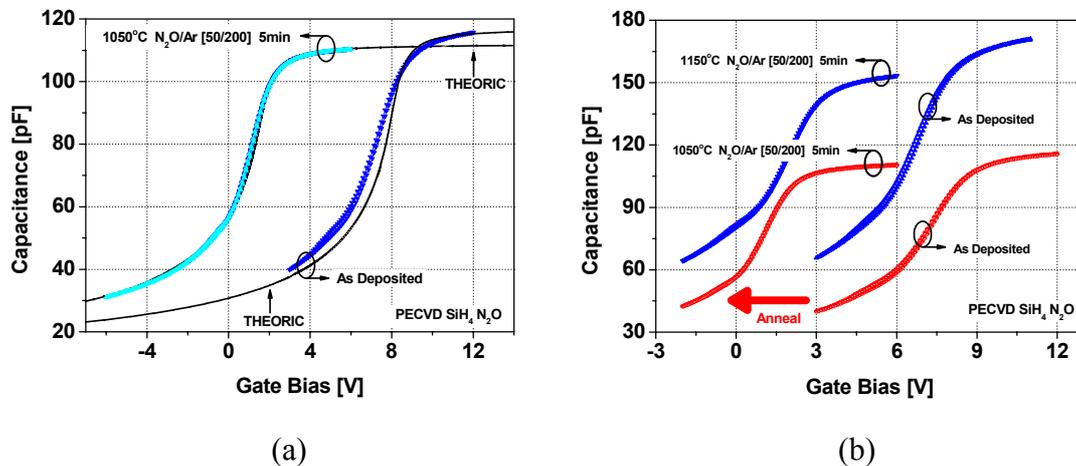
Fig. 5. 3. (a) Theoretical and experimental C-V curves for MOS capacitors fabricated from PECVD deposited oxide. (b) C-V of the MOS capacitors under different post deposition annealing conditions.

The interface trap density (D$_{it}$) has been extracted for the samples, corroborating a reduction of the interfacial traps density when the annealing processes are performed. Interface states density analysis have been realized using both Terman and conductance method[20] near the conduction band. Fig 5.4. shows the interface states density for the as deposited and annealed samples. Similar D$_{it}$ profiles(4-5$\times10^{11}$ eV^{-1}cm^{-2} at $E_C - E_T$ =0.2

eV) has been obtained for the samples annealed at two different temperatures. Higher D$_{it}$ is obtained for the as deposited sample (1×10^{12} eV^{-1}cm^{-2} at $E_C - E_T$ =0.2 eV).
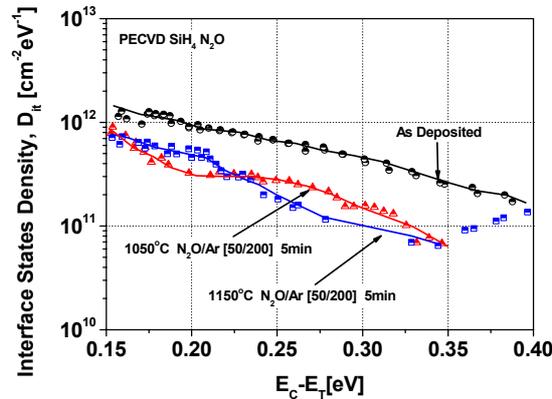
Fig. 5.4. The effect of annealing on the interface states density for 4H-SiC MOS capacitors.
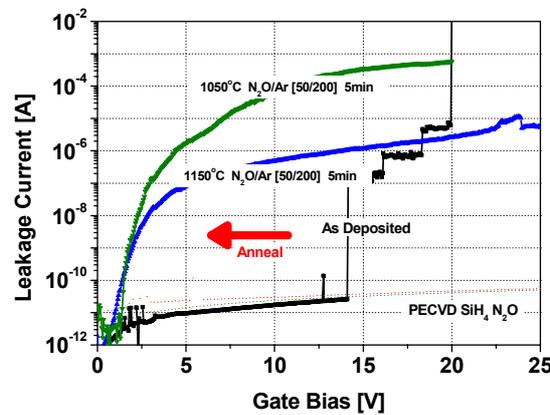
Fig. 5.5. Leakage current for 4H-SiC n-type capacitors as deposited and with different post deposition annealing conditions.
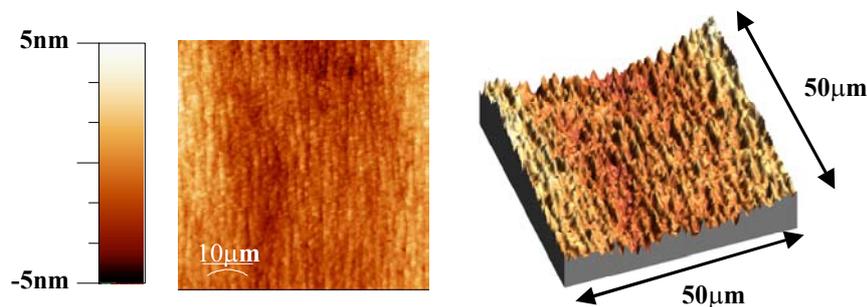
Fig. 5.6. Surface topology of deposited SiO$_2$ PECVD layer and annealed in N$_2$O at 1050ºC during 5min.

In spite of the relatively good results for the interfacial characteristics, very poor results have been obtained concerning the leakage current behavior. I-V measurements have been carried out in the MOS structures in the accumulation range. As it can be inferred from Fig. 5.5, the annealing in N$_2$O provokes a significant degradation of the

dielectric strength at the lower gate bias. The carrier transport mechanism through the insulator presents significant differences between the as deposited and the N$_2$O annealed samples. The current leakage after annealing seems to be leaded by impurities of the film as described by the Poole-Frenkel effect[21]. Leakage current measurements show that the dielectric properties of these films before and after thermal treatments must be improved.

The surface topology of one annealed sample is show in Fig. 5.6. Very high roughness has been inferred presumably due to the rapid reaction in the gas phase yielding the growth of large nuclei. These nuclei are incorporated into the film roughening the insulator surface.

5.2. a-SiO$_x$ layers from TEOS as source material

The use of deposited SiO$_2$ oxides with TEOS (Tetra-ethoxy-silane) as source material on SiC has not been widely studied. Indeed, only a few works can be found in the literature[22,23]. The use of TEOS as source material in the oxide deposition processes has overcame the traditionally used techniques in the SiO$_2$ deposition in the Si CMOS technology due to its superior characteristics. Among the enhanced properties of the TEOS technique it must be stressed the SiO$_2$ layer fluency on the substrate that allows obtaining smooth and regular surfaces. In fact, the main difference between TEOS and Silane is that in TEOS, the Silicon atom is already oxidized and thus, the conversion of TEOS to Silicon dioxide is essentially a rearrangement rather than an oxidation reaction. This section is focused on the study of the electrical characteristics of TEOS plasma enhanced CVD deposited oxides on 4H-SiC substrates for SiC gated devices, and the effect of post deposition annealing in different ambients. The characteristics of 4H-SiC MOSFETs fabricated using these layers are presented, to our knowledge, for the first time.

5.2.1. The CNM PECVD with TEOS as source material - Experimental Details

TEOS is a liquid at room temperature, with a vapor pressure of about 1.5Torr. TEOS slowly hydrolizes into silicon dioxide and ethanol when in contact with ambient moisture, but its flammability and toxicity are similar to that of an alcohol. To produce the vapor for use in processing, one may use a bubbler or a liquid injection system. In both cases, temperatures above room temperature are usually used to increase the TEOS partial pressure; thus it becomes necessary to heat the gas lines to prevent condensation therein. The key to understanding the difference between TEOS and silane is that in TEOS the silicon atom is already oxidized, with much reduced changes in free entalphy and free energy[18].

The basic overall reaction for the deposition of silicon dioxide requires the removal of two oxygen atoms (Fig. 5.7). While gas phase reactions can occur, particularly at the high end of the temperature range, deposition is probably the result of TEOS surface reactions. TEOS chemisorbs onto silanol groups (Si-OH) at the surface as well as strained surface bonds. TEOS will not absorb onto the resulting alkaly-covered surface, so deposition is probably limited by removal of the surface alkaly groups. These groups can undergo elimination reactions with neighboring molecules to form Si-O-Si bridges. This process takes place in an inert atmosphere: TEOS can be its own oxygen source,

and SiO$_2$ can be deposited from TEOS in nitrogen. However, addition of oxygen increases the deposition rate, presumably through providing an alternative path for removal of the ethyl group from the surface.

(a)   (b)
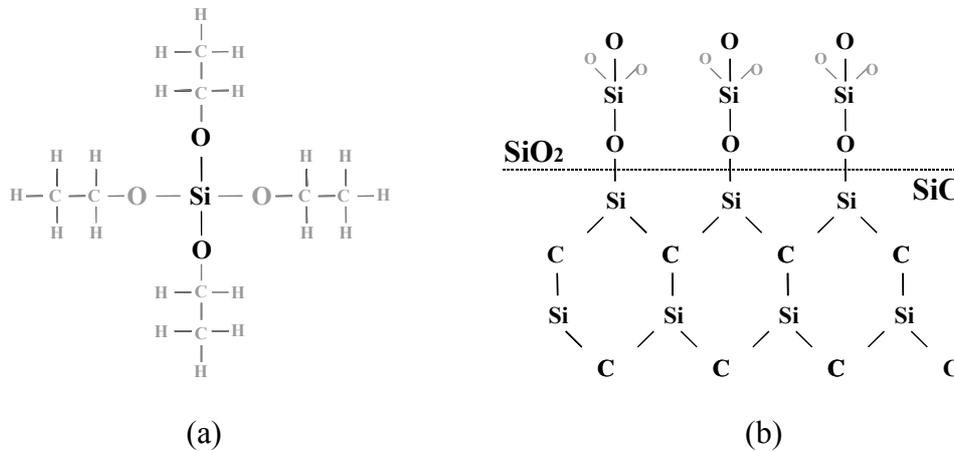
Fig. 5.7. (a) TEOS (Tetra-ethoxy-silane) is the deposited SiO$_2$ source material. (b) Structural model of the SiC(0001)/SiO$_2$ interface, where the basic overall reaction for the SiO$_2$ deposition requires the removal of two oxygen atoms.

As we discussed previously, TEOS is a relatively inexpensive, safe source for silicon dioxide. However, deposition using oxygen or inert ambients requires temperatures in excess of 600 ºC. To achieve lower temperature deposition, a first solution is to add a more aggressive oxidant. The use of ozone as this oxidant has been widely explored and found commercial applications[24]. Combining TEOS with ozone, in an attempt to preserve the excellent step coverage of TEOS/oxygen LPCVD at lower temperatures, was successful but, results in significant problems with film stress, moisture absorption, and low stability not observed by most other techniques.

Another approach to achieving deposition from TEOS at lower temperatures is to add plasma excitation. Plasma-enhanced deposition of oxides from TEOS (PETEOS) was first reported in the late 60's[17]. Extensive commercial development was performed in the 80's. Modern commercial processes employ parallel-plate showerhead reactors with RF plasma excitation, typically operating at pressures of 1 to 10 Torr, with gas flows of a few slpm including a few tens to hundreds of sccm of TEOS. Bubblers or liquid injection is employed to deliver the TEOS, as in thermal CVD.

With plasma excitation, high deposition rates are obtained at temperatures of 300-450 ºC from TEOS/oxygen. In single-wafer reactor rates of 5000-10000 A/min can be achieved, using pressures around 6-10 Torr and very small electrode gaps (< 6 nm). The problems encountered in thermal TEOS/ozone deposition (water absorption, silanol, stress, cracking) are also present in plasma-deposited films, but the presence of the plasma allows improved flexibility in dealing with them. Increasing RF power and increasing pressure while decreasing electrode gap, and increasing the oxygen/TEOS ratio, all help produce films which are "dry" and stable in air. Increasing the pressure with corresponding decreases in the gap has the nice property of increased rate without degraded stability. However, increasing the amount of oxygen decreases the deposition rate, so the final process is a trade-off of stability with throughput. Conformality is greatly superior to that obtained from plasma or thermal silane/oxygen deposition, but inferior to thermal TEOS. Relatively little gas phase reaction gives smooth films.

In this sense, to achieve higher interface quality, as an alternative technique to thermal oxidation, we deposited amorphous SiO$_2$ layers (100 nm) at a low temperature of 380-430 ºC by plasma enhanced CVD technique using TEOS as a source material on 8º off axis (0001) 4H-SiC substrates. The summary of the PECVD SiO$_2$-TEOS deposition parameters is listed in Table V.2.

Process	Thick. [nm]	Temp.	Pressure	Time	Flow Rates	Others
rf- PECVD	100	380ºC to 430ºC	3 Torr	X min	50% TEOS 50% O$_2$	RF power: 50W

Table V.2. Summary of the PECVD SiO$_2$-TEOS deposition parameters.

To improve the interface quality further, different post deposition annealings have been performed in oxidizing (O$_2$ and diluted N$_2$O) or inert (N$_2$ and Ar) ambients. The Additionally, prior to the SiO$_2$-TEOS deposition, some samples have been thermally oxidized in dry O$_2$ and diluted N$_2$O, at the low temperature (for SiC) of 1050 ºC (1 h) and 1200 ºC (20 min) respectively. These oxidation processes produce an interfacial insulator with thickness of ~10 nm (O$_2$) and ~20 nm (N$_2$O), presumably with less dangling bonds and better interfacial characteristics when compared with a standard dry oxidation carried out at higher temperatures and larger times. After the low temperature oxidation, 100 nm of SiO$_2$-TEOS has been deposited. Post deposition annealing in Ar, N$_2$ and O$_2$ has also been performed in some of these samples. The summary of the post TEOS deposition annealings and prior TEOS deposition oxidation processes is presented in Table V.3.

Name	Process	Temperature	Time
Prior SiO$_2$ - TEOS deposition Interface oxidation			
O$_2$	O$_2$ oxidation	1050 ºC	1 h
	N$_2$O:Ar [1/1] oxidation	1200 ºC	20 min
Post SiO$_2$ - TEOS deposition annealing			
O$_2$	O$_2$ annealing	1050 ºC	1 h
Ar	Ar annealing	1000 ºC	1 h
N$_2$	N$_2$ annealing	950 ºC	1 h
RTA N$_2$O	N$_2$O:Ar [2/1] RTA	950 ºC	5 min

Table V.3. Summary of the prior SiO$_2$ - TEOS deposition interfacial oxidation and post deposition annealing processes performed on 4H-SiC MOS structures.

5.2.2. MOS Physical and Electrical characteristics

C-V measurements have been performed on the fabricated MOS structures using a mercury probe. Fig. 5.8 shows the high frequency (10 kHz) C-V characteristics measured for the samples after the different post deposition annealings. As it can be inferred from the figure, the as deposited sample is not well-behaved and thus, post deposition treatments must be carried out. The flat band voltage shift (an indication of oxide traps) is reduced performing subsequent annealings. The N$_2$ annealing seems to be more effective in reducing the flat band shift and the hysteresis of the capacitance-

voltage characteristics. An appreciable hysteresis behaviour, evidencing the presence of slow traps in the dielectric, has also been obtained if the sample is only annealed in N$_2$O. However, the lower oxide traps density is achieved with the combination of the two annealing processes.
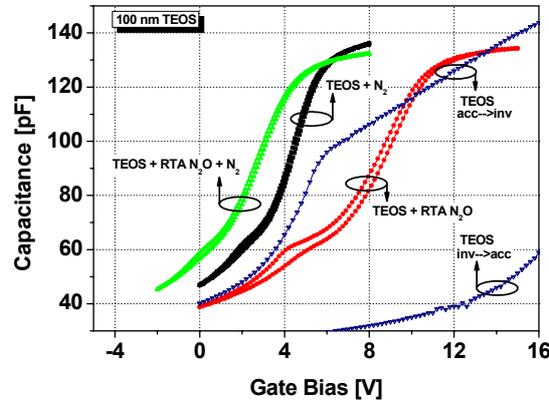
Fig. 5.8. High-frequency capacitance-voltage (C-V) characteristics for the MOS capacitors under different post deposition annealing conditions.
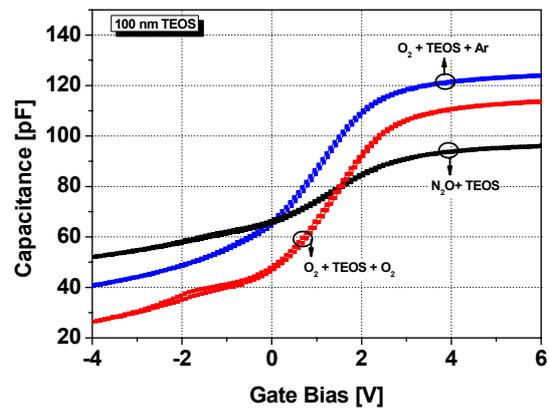
Fig. 5.9. High-frequency capacitance-voltage (C-V) characteristics for the MOS capacitors with different prior deposition oxidation processes and post deposition annealing ambients.

Analogously, the samples oxidized prior to TEOS deposition show lower flat band shift and hysteresis when compared with the direct deposited TEOS samples. As it can be inferred from Fig. 5.9, similar flat band voltage shift is obtained for the samples oxidized in O$_2$ or N$_2$O. However, the oxide thickness significantly increase (lower capacitance) when the samples are oxidized prior to deposition, especially for the N$_2$O oxidation, due to the additional SiO$_2$ from the SiC surface oxidation.

The interface trap density has been extracted for the samples, pointing out a marked dependence of the interfacial characteristics on the oxidation and annealing processes. Interface states density analysis has been performed using both Terman method and conductance method[20] near the conduction band. Fig 5.10 shows the interface states density for the annealed and the prior deposition oxidised TEOS samples . The lower D$_{it}$ (5×10^{11} eV^{-1}cm^{-2} at $E_C - E_T$ =0.2 eV) has been obtained for the N$_2$O grown sample N$_2$O/SiO$_2$-TEOS. Slightly higher interface traps density is achieved for the sample oxidized in O$_2$ and annealed in Ar (8×10^{11} eV^{-1}cm^{-2} at $E_C - E_T$ =0.2 eV).

However, the interface seems to degrade if the post TEOS deposition annealing process is performed in an oxidation ambient (O$_2$). A poorer D$_{it}$ profile (1×10^{12} eV^{-1}cm^{-2} at $E_C - E_T$ =0.2 eV) has been obtained for the N$_2$ annealed sample. The higher D$_{it}$ is obtained for the N$_2$O annealed sample (3×10^{12} eV^{-1}cm^{-2} at $E_C - E_T$ =0.2 eV).
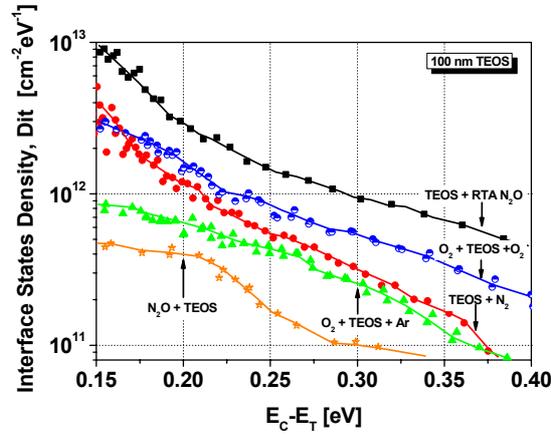
Fig. 5.10. Effect of annealing ambients and interfacial oxidation on the interface states density for 4H-SiC MOS capacitors.
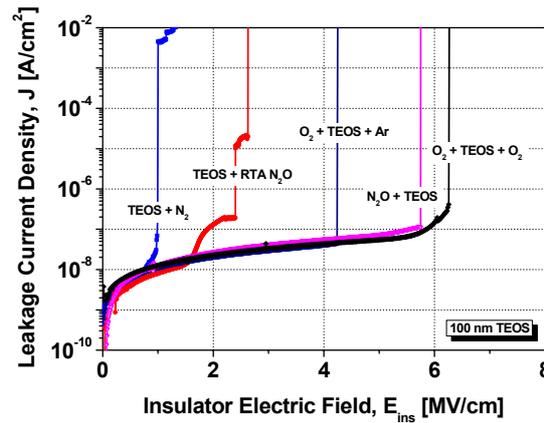
Fig. 5.11. Leakage current for 4H-SiC n-type capacitors with different prior SiO$_2$ - TEOS deposition interfacial oxidation processes and post deposition annealing conditions.

I-V measurements have also been carried out in the MOS structures biased in accumulation. As it can be inferred from Fig. 5.11, the annealing in O$_2$ and N$_2$O is more effective in reducing the leakage current than the Ar or N$_2$ treatment. Again, the best performances have been obtained with the previously oxidized samples. The oxidation of a thin layer after the deposition has been found to be very effective in reducing the current leakage. The O$_2$ and N$_2$O annealings have probably oxidized a thin layer of the surface, and thus the leakage current is also diminished. Leakage current measurements show that the dielectric properties of these films after thermal treatments should be improved.

The refractive index at optical frequencies, often used for oxide characterization, can vary for many reason and is very sensitive to the process parameters. Nevertheless, dielectric constant at DC to microwave frequencies or infrared absorption are much

better ways to characterize SiO$_2$. The insulator thickness has also been obtained physically in order to verify that considering the dielectric constant of SiO$_2$ of 3.9 is actually a good approach. In particular, SIMS depth profile analysis have been carried out in our samples as shown in Fig. 5.12. The thickness of the stacked structure made up of the thin interfacial low temperature thermal SiO$_2$ and the deposited SiO$_2$-TEOS has been found to be ~110 nm from both, the SIMS and C-V measurement, considering the dielectric constant for SiO$_2$ ε_r=3.9.
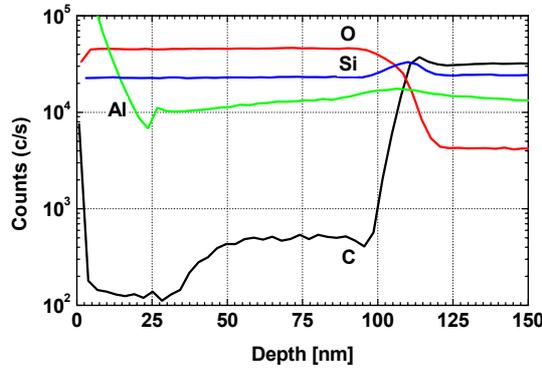
Fig. 5.12. SIMS depth profile of 10 nm dry oxide (1050 ºC, 1 h) and (100 nm) SiO$_2$-TEOS annealed in Ar (1000 ºC, 1 h).

(a)   **(b)**   **(c)**
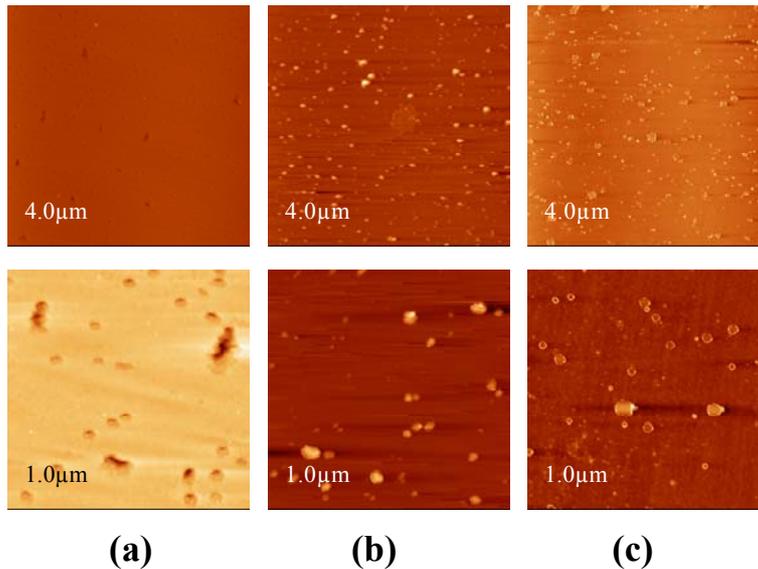
Fig. 5.13. AFM images of SiO$_2$-TEOS deposited film (a) on interfacial thin SiO$_2$ (10 nm), (b) on 4H-SiC and annealed in O$_2$ (1050 ºC, 1 h), (c) on 4H-SiC and annealed in N$_2$O (1150 ºC, 5 min),

The surface roughness of the deposited SiO$_2$ from TEOS as source material has been evaluated by atomic force microscopy working in non contact tapping mode. We have found a marked difference between the roughness of the samples with deposited oxide on thin interfacial SiO$_2$ or directly on 4H-SiC. The formation of nuclei seems to be more regular on a previously oxidized SiC surface. As inferred from Fig. 5.13 the rough mean square is drastically reduced in the stacked structure Fig. 5.13(a), RMS=1 nm ,when compared with the SiO$_2$ MOS with deposited oxides directly on 4H-SiC and

annealed Fig. 5.13(b), (c). RMS ranging 6-12 nm has been determined for the Fig. 5.13(b) and (c) samples annealed on O$_2$ (1050 ºC, 1 h) and N$_2$O (1150 ºC, 5 min), respectively.

5.2.3. 4H-SiC SiO$_2$-TEOS MOSFETs fabrication

In the previous section, the main electrical properties of the SiO$_2$-TEOS gate oxides have been extracted. The best interface characteristics, lower flat-band voltage shift and lower leakage current have been achieved when the SiC substrate has been thermally oxidized at relatively low temperature and during short time prior to SiO$_2$-TEOS deposition. The oxide charge in the SiO$_2$-TEOS oxide has also been reduced with an inert (Ar or N$_2$) post-deposition annealing. Hence, the MOSFET gate fabrication is based in these two processes. Hence, the MOSFET gate fabrication is based in these two processes. MOSFETs have been fabricated with two different TEOS deposition processes and on two SiC crystal orientation. We used two N$^+$ 4H-SiC substrates epitaxied with a P-type layer doped at 5×10^{16} cm^{-3} on the 8º off Si (0001) face from CREE, and one N$^+$ 4H-SiC (11-20) substrate (CREE) with a P-type layer doped at 2×10^{17} cm^{-3} grown at LMI Lyon. The gate insulator was grown by dry oxidation during 1 h at 1050 ºC. Afterwards, SiO$_2$-TEOS was deposited and annealed in Ar during 1 h at 950 ºC. The resulting dielectric final thickness was calculated to be around 100 nm in all substrates. The gate area was defined etching selectively the source and drain regions. Evaporated Aluminium and Nickel were used to form the MOS gate and the source/drain contacts, respectively.

(a)   (b)
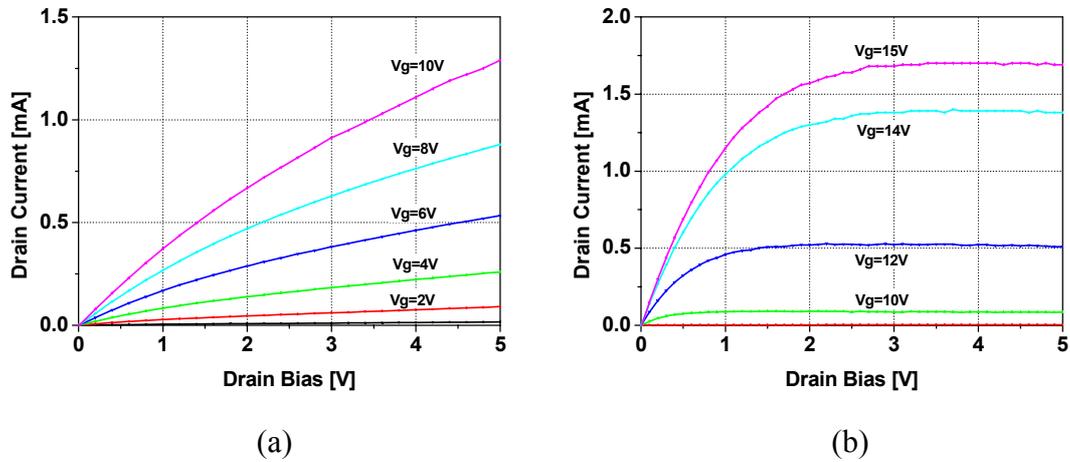
Fig. 5.14. Forward I-V characteristics of TEOS SiO$_2$/Thermal SiO$_2$ (a) 4H-SiC (0001) MOSFET, and (b) 4H-SiC (11-20) MOSFET, (L =4 μm, W =150 μm) measured at room temperature.

The MOSFET forward I-V characteristics are presented in Fig. 5.14(a) for the MOSFET implemented in the (0001) face and in Fig. 5.14(b) for the MOSFET implemented in the (11-20) face, where L =4 μm, W =150 μm, t_{ox} =110 nm and t_{ox} =70 nm, respectively. The gate insulator thickness on the (11-20) face has been found to be lower than the predicted, measured from capacitors adjacent to the MOSFET. The drain characteristics presents several relevant differences depending on the substrate orientation. The saturation voltage in (0001) 4H-SiC devices is higher than in the (11-20) ones. The origin of this discrepancy can be explained considering a higher threshold

voltage and a higher field-effect mobility for the devices fabricated on the (11-20) face, as it will be shown later on.

The inversion channel field-effect mobility has been extracted from the MOSFET fabricated with the stacked thermal SiO$_2$ and deposited SiO$_2$-TEOS. The field-effect mobility has been evaluated from the derivate of the transconductance curves (Fig. 5.15(a)).

(a)   (b)
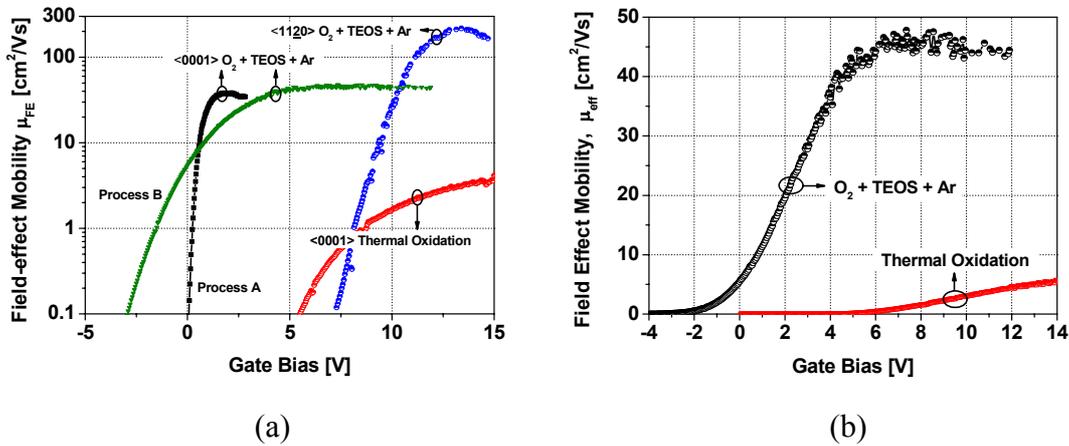
Fig. 5.15. (a) Comparison of the field effect electron channel mobility in transistors made using standard dry oxidation and low temperature dry oxide plus SiO$_2$-TEOS. (b) The mobility of (0001) 4H-SiC of the standard thermal oxidation is improved up to nine times.

The higher peak mobility, up to the record value of 216 cm^2/Vs, is achieved for MOSFET fabricated in the (11-20) face. This is a very high field-effect mobility value for 4H-SiC devices, the higher reported to our knowledge. The devices fabricated in the (0001) face also present high mobility, when compared with a thermal oxidation but significantly lower when compared with the (11-20) face. In this last situation peak mobility values ranging 38-45 cm^2/Vs have been obtained depending on the TEOS deposition process on the previously oxidized gate thermal oxide (Fig. 5.15(b)). This (high) field effect mobility is not routinely obtained for 4H-SiC (0001) Si face devices with only dry oxidation processes. Indeed, only few process (based on nitridation, contaminated oxides or alternative high-k dielectrics) have been reported to be effective to achieve that field-effect mobility level[25-27]. In 1998, Sridevan *et al.*[4], reported mobility on (0001) Si-face 4H-SiC MOSFETs as high as 165 cm^2/Vs, using low temperature deposited oxides (LTO) in the gate process fabrication. However, this result, reporting the first lateral 4H-SiC MOSFET, has not been reproduced in the literature during the last years, and has lost credibility progressively. Ólafsson[28] has speculated that this high mobility could proceed from the oxide contamination.

At this point, one fundamental question arises, why we obtain these extremely high mobility values. One significant difference is obtained when the electrical characteristics of the MOSFETs are compared with low mobility value devices (i.e. standard thermal oxidation). The gate current leakage is higher in the devices with higher mobilities in the (0001) and in the (11-20) faces. Hence, we are tempted to assume that there is a relation between gate leakage current and the field-effect mobility improvement. However, this is not true for all the set of studied MOSFETs. In some of the samples (on the (0001) face), a significant reduction of interface traps has been detected. This becomes obvious considering two set of MOSFET fabricated on the

(0001) face. MOSFET fabricated on the (0001) face present marked differences depending on the fabrication process (process named A or process named B). The gate definition differences between the fabrication of run A and B resides in different TEOS deposition conditions (deposition temperature and TEOS/O$_2$ ratio). As it can be inferred from Fig. 5.16(a), for samples fabricated using the process A the gate leakage current seems to be negligible, and the improvement on the field effect mobility is related with and effective reduction of interface traps.

(a)   (b)
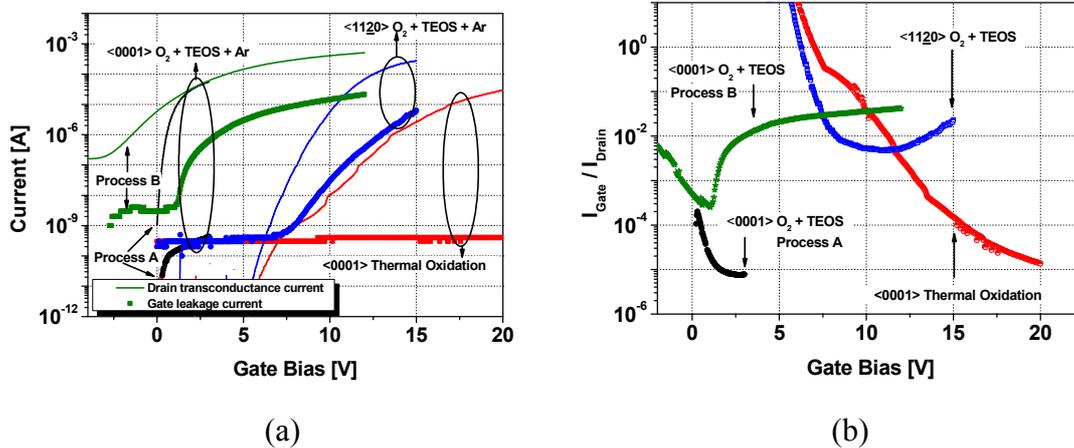
Fig. 5.16. (a) Leakage current (gate current) and transconductance (drain current) measurements and (b) I$_{Gate}$/I$_{Drain}$ (to source) measured in a transconductance curve for transistors TEOS transistors.

(a)   (b)
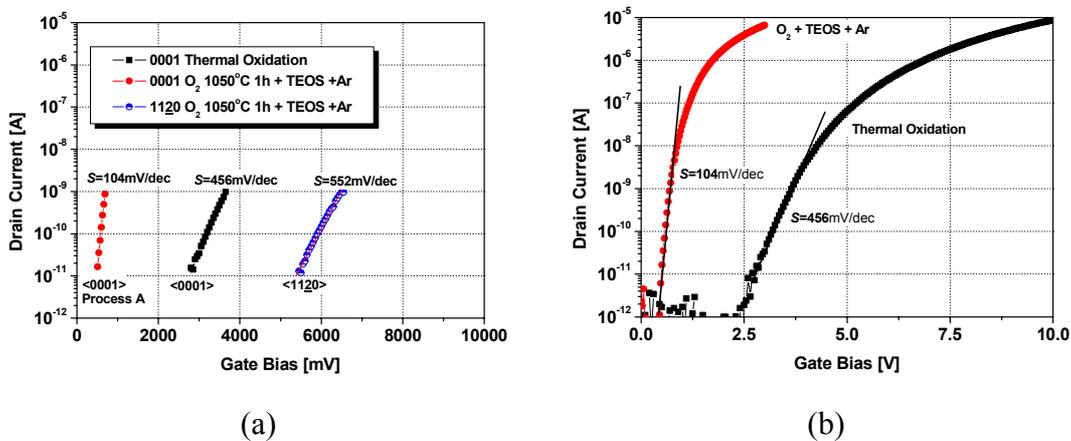
Fig. 5.17. (a) Comparison of the sub-threshold characteristics in transistors made using standard dry oxidation and low thermal dry oxide plus SiO$_2$-TEOS. (b) *S* is markedly reduced in the low leakage TEOS process on (0001) 4H-SiC.

However, for samples fabricated using the process B the improvement mechanism seems to be different, and presumably related mainly with the gate leakage current. A corroboration of this statement was found when the sub-threshold slope *S* was analyzed. MOSFET fabricated with process named A actually reduce their sub-threshold swing, when compared with a standard thermal gate oxide, from 456 mV/dec to 104 mV/dec. These last results are a clear indication of the reduction of interface traps that can affect the drift of carriers in the inversion layer[29]. However, the values for *S* obtained in MOSFETs fabricated with process named B are degraded when compared to MOSFETs fabricated with thermal oxide. The MOSFET implemented in the (11-20)

face follows the same behavior as the (0001) MOSFET with gate oxide fabrication process named B (Fig. 5.17). In these two last samples, the mobility obtained is higher, but the gate leakage and the sub-threshold slope are also higher. The relation between the gate (to source) current and the drain (to source) current measured in transconductance, is presented in Fig. 5.16(b). As it can be inferred from the figure, once the inversion channel is formed, when the gate voltage increases over the threshold voltage, the gate current is only 100 – 50 times lower than the drain current. (0001) MOSFET with process A does not follow this behavior, since the mobility improvement seems to be related with effective interface trap passivation. Table V.4 summarizes the main electrical variables of the fabricated devices.

4H-SiC Face	Process	μ_{FE} [cm^2/Vs]	V_{th} [V]	S [mV/dec]
0001	*Standard Thermal oxidation*	5	5	456
	O$_2$ + TEOS (Process A)	38	0.5	104
	O$_2$ + TEOS (Process B)	45	-2.5	> 500
11<u>2</u>0	*O$_2$ + TEOS* (Process B)	216	8	552

Table V.4. Summary of the electrical characteristics for the 4H-SiC MOSFET. *Standard Thermal Oxidation* 1150 ºC 3 h, *TEOS:* O$_2$ 1050 ºC 1 h + SiO$_2$ TEOS + Ar 950 ºC 1 h.

Although the origin of the very relevant field-effect mobility improvement is not completely understood, it seems that it is not the reduction of interface traps passivation (as it should be desirable), at least in the more relevant case, the MOSFET on the (11-20) face. However, enhanced interface properties have been obtained with low temperature oxidation and deposited SiO$_2$ from TEOS as source material as it can be inferred from the characteristics of MOSFET fabricated with process named A. Considering the impressive results of this work as one decisive step toward one possible solution to the low mobility in 4H-SiC devices seems to be a thorny subject. If the enhancement is related with the gate leakage current could lead a reduced reliability and reproducibility. Indeed, it is mandatory to investigate what is the real origin of the mobility improvement or if it is an apparent improvement few controllable. The authors speculate that our mobility improvement could be related with the use of contaminated gate oxides that recently have been reported to give very high mobility values[7,25]. In our case, the contaminants (or anything else that improves the mobility) are presumably introduced during the TEOS SiO$_2$ deposition.

VDMOS power devices

As stressed in *Chapter II*, the physical and electronic properties of SiC make it the foremost semiconductor material for high temperature, radiation resistance, and high-power/high-voltage electronic devices. The relatively high mobility values achieved with TEOS oxides can allow developing competitive MOS gated power devices with our SiC technology. In this sense, a structure which does overcome many of the voltage and on-resistance limitations of conventional MOS transistors is the double-diffused or DMOS technology. DMOS structures began to appear in literature in the early 1970s, and it was this structure which made possible the revolution in discrete power MOS devices in Silicon. DMOS result in transistors with both, a short channel length and the ability to withstand high drain-to-source voltages because of the

separation of the active of channel region of the device from the region of the device that sustains the drain-to-source voltage. The two types of MOS power transistors which have found widespread commercial acceptance in discrete form are the LDMOS (Lateral DMOS) and VDMOS (Vertical DMOS) devices. Of these two, the VDMOS is by far the more common (although the LDMOS device has some advantages in specific applications, primarily lower-voltage situations). The structure of one typical VDMOS transistors is shown in Fig. 5.18.
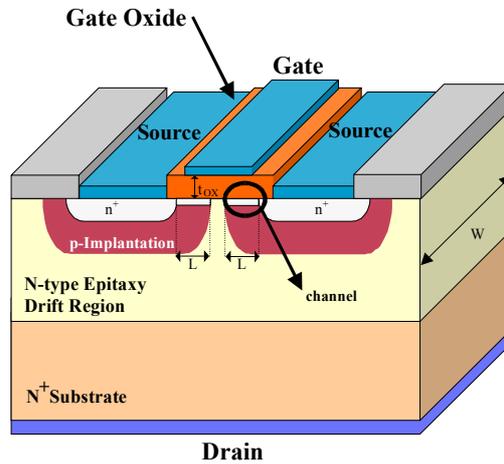
Fig. 5.18. Three-dimensional view of basic (n-channel) VDMOS device structure.

The carriers flow from the source through the channel at the surface of the body region (p-implantation) to the lightly doped drift region under the influence of voltages on the gate and drain. However, when the electrons reach the lightly doped epitaxy drift region below the gate, they flow away from the surface of the Silicon carbide toward the more heavily doped drain region.
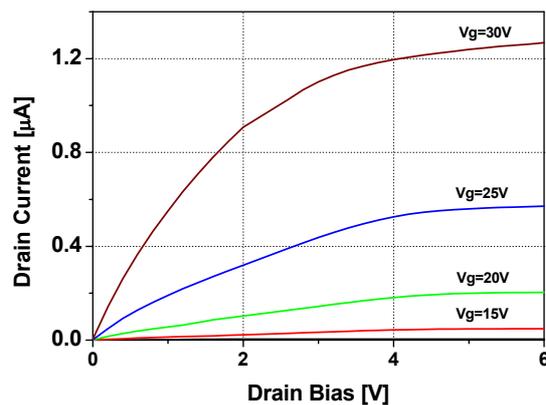
(a)   (b)

Fig. 5.19. (a) Photography of the fabricated VDMOS. (b) Forward I-V characteristics with TEOS gate oxide for the 4H-SiC p-implanted VDMOS.

As demonstrator of MOS gated power device, VDMOS power transistors with different geometrical parameters are also included in the mask set described in *Chapter IV* (Fig. 5.19(a)). The channel is formed between the N$^+$ implant edge and the p-

implantation pitch edge and is determined by photolithography and not by a double diffusion, because impurities do not diffuse in SiC at the annealing temperatures used (1700 ºC). The gate fabrication process is based in the low thermal dry oxide plus SiO$_2$-TEOS. Fig. 5.19(b) shows the I-V characteristic of a VDMOS with L =24 μm and W =150 μm.

5.3. a-SiO$_x$ layers from RTCVD Si layer oxidized in diluted N$_2$O

Nitrous oxide (N$_2$O) can be used as an alternative gas for nitridation, and it would be a preferred gas to NO for use in semiconductor industry because of its non-toxic property[30]. Identical chemical structures at the SiC-SiO$_2$ interface for gate oxides grown in either NO and N$_2$O ambient were found by x-ray photoelectron spectroscopy (XPS) analysis[31]. This is because N$_2$O can dissociate into NO, O$_2$ and N$_2$ at temperatures higher than 1000ºC. A nitridation model, that qualitatively accounts for the observed beneficial effects in N$_2$O and NO grown/annealed oxides on SiC, states for a double beneficial effect[32]: (1) strong Si≡N bonds are created at the SiO$_2$-SiC interface, as in the case of SiO$_2$-Si, (2) carbon compounds inherent processing defects occurring during SiC oxidation- are removed from the SiO$_2$-SiC interface. Analogously, the work of Afanas'ev $et\ al.$[33] indicates that nitridation improves the 4H-SiC/SiO$_2$ interfaces by two, not directly coupled, mechanisms: First, there is a reduction of the fast interface state density by the removal of π-bonded carbon either physically or through chemical passivation. Second, the major mechanism of the interface improvement by nitridation in NO is related to the removal of very slow interface states and likely related to defects in the near-interface oxide layer. Further optimization of the N$_2$O oxidation process may not only concern refining the nitrogen incorporation procedures, but also the oxide growth itself. In this sense, we propose and report for the first time[34] the N$_2$O oxidation of thin Si layers deposited on 4H-SiC by means of Rapid Thermal Chemical Vapor Deposition (RTCVD). With this procedure, it is possible to combine the known beneficial effects in nitride oxides with the growth of a stable free carbon SiO$_2$ layer from the deposited Si layer. In addition, this technique could allow obtaining SiO$_2$ thicker layers adequate for passivation purposes, when compared with direct SiC N$_2$O oxidation. Few works reports on innovative silicon oxidation on SiC. Tan et al.[35], proposed the dry thermal oxidation of a polycrystalline silicon layer CVD deposited on 6H-SiC at 580 ºC. Analogously, Kaneko et al.[36], report on 4H-SiC ACCUFET with stacked gate oxide that comprises a thin thermal oxide and non-doped silicate glass (NSG) deposited over it.

5.3.1. The CNM Si RTCVD oxidized in diluted N$_2$O - Experimental Details

The chemical vapor deposition of Si on SiO$_2$ has been largely used in the semiconductor industry with a vast variety of applications. Hence, polycrystalline silicon films have been used for the fabrication of thin-films transistors (TFTs)[37], metal-oxide-semiconductor gates[38], and electrically erasable and programmable read only memories (EEPROMs)[39], among other devices, while amorphous and porous amorphous silicon have interesting properties that make this material suitable for

optoelectronics applications[40]. Rapid thermal chemical vapor deposition has also been shown to be an alternative method of producing high quality oxides on silicon[41].

Our reactor is an RTCVD system with air-cooled tungsten lamps that allows temperature transitions on the surface of the wafers as fast as 50 ºC/s, maintaining the walls of the deposition chamber at much lower temperatures. In such a way, the deposition processes are initiated and terminated by temperature switching, thus minimizing the thermal budget. The system is equipped with a turbomolecular pump able to give an ultimate vacuum of 10^{-6} mbar before the initiation of the depositions. This gives the clean growth environment essential to obtain good quality structures. The RTCVD deposition temperatures have been considered within the interval 950 – 1050 ºC. Diluted SiH_4 in Ar [10/100] has been used as source gas.

Process	Thick. [nm]	Temp.	Pressure	Time	Flow Rates	Others
RTCVD	10 - 25	950 - 1050ºC	1 Atm	10 min	100 sccm Ar 10 sccm (10%) SiH_4/Ar	5 Rapid Cicles

Table V.5. Summary of the Si RTCVD deposition parameters.

Thermal oxides (10-25 nm thick) were prepared in a N_2O diluted in Ar (50%) ambient at 1300 ºC during 15 min. Metal-oxide-semiconductor capacitors were fabricated on Si-faced, n-type 4H-SiC wafers with 5-μm-thick epilayers with a doping level of 2.18×10^{16} cm^{-3}, oriented 8º off the (0001) direction that were purchased from CREE Research Inc.

5.3.2. MOS Physical and Electrical characteristics

C-V measurements have been performed on the fabricated capacitances. As it can be derived from the Fig. 5.20, for RTCVD Si deposited and N_2O oxidized layers, the high frequency capacitance voltage characteristics (C-V) shows little pronounced hysteresis and reduced flatband voltage. To be practical as gate oxide, the thickness of these deposited and nitridated Si layers will be increased, either in the deposition/nitridation process or depositing SiO_2 after the layer formation.
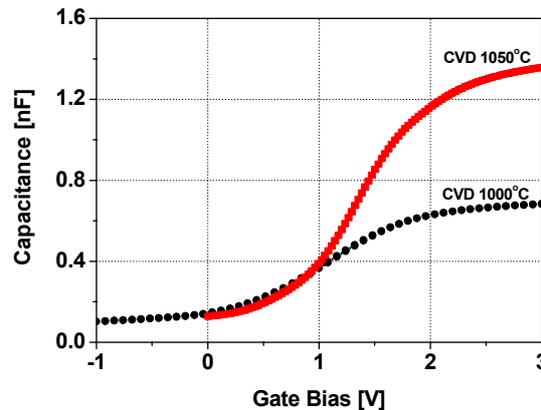
Fig. 5.20. High frequency C-V of RTCVD Si deposited on SiC oxidized in N_2O samples.

The N$_2$O oxidation conditions have been chosen based on the previously reported beneficial effects when 4H-SiC substrates are considered[30-33]. A high oxidation temperature (1300 ºC) improves the oxide quality reducing both interfacial and oxide charges. The oxidation in a N$_2$O ambient of the Si RTCVD layer is performed in a relatively short time in order to minimize the SiO$_2$ growth from the 4H-SiC substrate. Nevertheless, the controlled oxidation of only the Si layer is a difficult issue in practice. Hence, some oxidation of the silicon carbide substrate can occur, especially at the temperature considered. Lower temperatures, such as 950 ºC, could be used to avoid SiC oxidation, but at these temperatures the N$_2$O oxidation process has a very low efficiency.

Thermally N$_2$O grown oxides directly on 4H-SiC have been also studied in order to evaluate the influence of nitridation conditions in the electrical characteristics of the insulator. Thermal oxides (10-20 nm thick) were prepared by three different processes: (A) growth in 10% of N$_2$O diluted in Ar at 1300 ^{o}C during 90 min, (B) growth in 25% of N$_2$O diluted in Ar at 1300 ^{o}C during 90 min and (C) growth in 15% of N$_2$O diluted in Ar at 1300 ^{o}C during 45 min. The flat-band voltage, the oxide charge, the hysteresis behavior and the thickness of gate oxides grown in N$_2$O have been extracted using C-V measurements shown in Fig. 5.21.
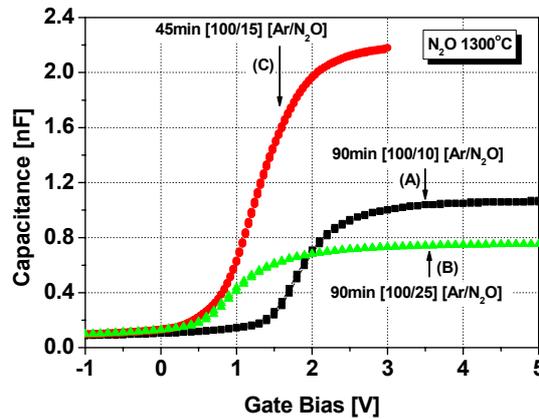
Fig. 5.21. High frequency C-V curves for thermally N$_2$O grown MOS capacitors at 1300 ºC for different oxidation conditions.

The oxide thickness depends on both oxidation time and N$_2$O diluted concentration. The lower interface states density and oxide charges have been obtained with the process (B). Process (C) results in the thinner oxide, and the associated oxide charge and D$_{it}$ is significantly higher when compared with the other two processes. These results suggest that a minimum thickness/oxidation /nitridation time must be considered in order to achieve adequate electrical characteristics. Interface states density analysis have been realized by means of the conductance method on both N$_2$O grown oxides and N$_2$O oxidized RTCVD Si layers, as well as on an standard dry thermal oxide (1160 ºC – 3 h) used as reference. Fig. 5.22 displays the D$_{it}$ profiling versus trap energy within the band gap, representing a significant reduction of D$_{it}$ of both N$_2$O oxidized RTCVD Si process types, when compared with standard dry thermal oxides. When compared with the best N$_2$O grown oxide [oxidation condition (B)], D$_{it}$ is reduced especially for interface traps lying in the $E_C - E_T$ =0.3-0.6 eV range.
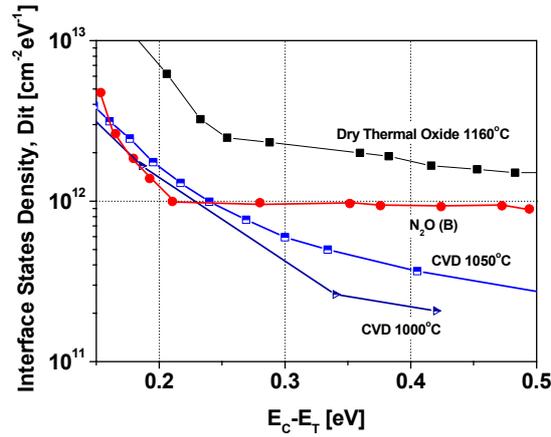
Fig. 5.22. D$_{it}$ profile of RTCVD Si deposited on 4H-SiC (0001) and nitridated samples near the conduction band.

The standard deviation of the surface potential[42] of N$_2$O oxidized RTCVD Si samples has been reduced from ~3 kT (standard thermal oxide) to more silicon-like values of ~0.8 kT implying a more homogeneous charge distribution at the interface, approaching to a SiC/SiO$_2$ interface with a distributed trap levels with no band-bending fluctuations (Fig. 5.23). Thus, higher mobility in 4H-SiC MOSFET devices could be expected using these RTCVD Si layers oxidized in N$_2$O ambient.
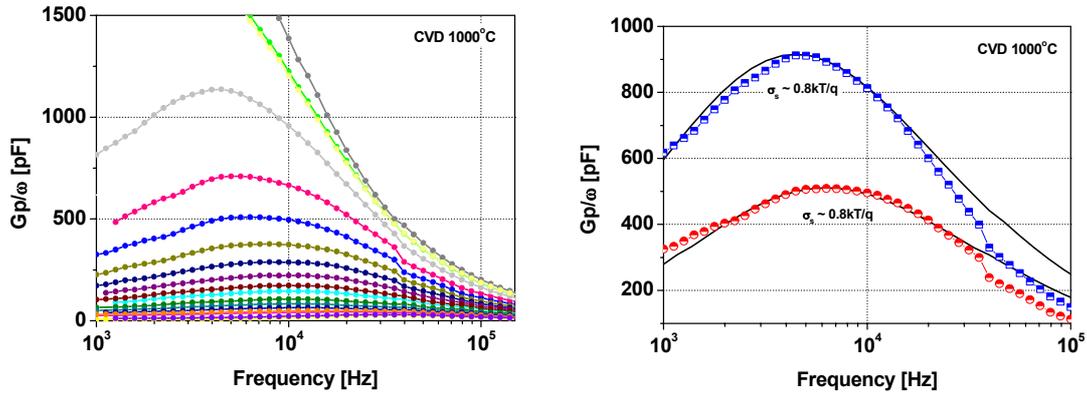
Fig. 5.23. Equivalent G$_p$/ω versus log ω plots in conductance method. Theoretical fits have been derived using the Nicollian - Goetzberger model Ref. 42.

The surface topology of the nitridated RTCVD Si layer has been evaluated by atomic force microscopy (AFM) working in the non contact tapping mode. An average height of the surface (RMS) of ~1 nm has been extracted for the samples. The investigated area was 3.5×3.5 μm^2 as shown in the Fig. 5.24. No implantation processes have been performed on SiC samples, prior to RTCVD Si layer deposition and oxidation. Previously to deposition, SiC surface roughness presents typical values ranging 0.8-1 nm. When performed on implanted layers, the roughness is expected to be higher due to the surface degradation caused by the activation annealing carried out at high temperature (typically 1600 ºC).
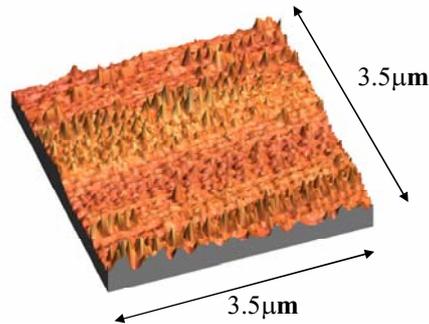
Fig. 5.24. Surface topology of RTCVD (1000 ºC) Si deposited and N$_2$O oxidized layers.

5.4. Conclusions

The deposition of high quality insulator layer allows avoiding the problems related with Carbon liberation during the thermal oxidation that presumably strongly degrade the quality of the interface. Moreover, all these techniques avoid the anisotropy of oxidation rate experienced during thermal oxidation. Chemical Vapor Deposition (CVD) is the formation of a film on a surface from a volatile precursor (vapor or gas), as a consequence of one or more chemical reactions which change the state of the precursor. The deposition process can be activated by temperature (CVD), laser (LCVD), photo induced (PCVD) or plasma (PECVD). Plasma-enhanced chemical vapor deposition is a powerful tool for many film deposition processes that cannot be achieved with temperature control alone.

PECVD SiO$_2$ has been deposited on 4H-SiC substrates with SiH$_4$ and N$_2$O as precursors. The most common Silicon volatile precursor for SiO$_2$ CVD deposition is Silane (SH$_4$). The basic overall reaction for the deposition of silicon dioxide from Silane in a thermal process requires the removal of the hydrogen atoms and addition of two oxygen atoms. N$_2$O is employed in PECDV reactors as an oxidant instead of O$_2$ since pure Oxygen is typically found to be too reactive. To enhance the global performance of the films further, thermal post-deposition annealing have been performed on the samples. In spite of the relatively good results for the interfacial characteristics (4-5×10^{11} eV^{-1}cm^{-2} at $E_C - E_T$ =0.2 eV), very poor results have been obtained for the leakage current behavior. The post-deposition annealing in N$_2$O provokes a significant degradation of the dielectric strength (< 1 MV/cm). The current leakage after annealing seems to be leaded by impurities in the film as the Poole-Frenkel effect.

The use of TEOS as source material in the oxide deposition process has overcame the traditionally used techniques in the SiO$_2$ deposition in the Si CMOS technology. Among the enhanced properties of the TEOS technique it must be stressed the SiO$_2$ layer fluency on the substrate that allows obtaining smooth and regular surfaces. The main difference between TEOS and Silane is that in TEOS the silicon atom is already oxidized and thus, the conversion of TEOS to Silicon dioxide is essentially a rearrangement rather than an oxidation reaction. The innovative SiO$_2$ deposition has been carried out with a plasma enhanced CVD TEOS deposition process on 4H-SiC substrates. Ar, O$_2$, N$_2$ and N$_2$O annealing processes have been performed after the deposition to enhance the electrical properties of deposited oxides. The flat-band voltage and the interface trap density have been reduced after these thermal treatments. Stacked structures based on thermally grown oxides (in O$_2$ and N$_2$O) at low temperature along with SiO$_2$-TEOS deposited oxide have also been fabricated. The

stacked structure improves, in terms of leakage current and interface properties, the directly deposited and annealed oxides.

4H-SiC MOSFETs have been fabricated using these stacked oxides subsequently annealed in Ar. On (0001) face samples, peak mobility values ranging 38-45 cm^2/Vs have been obtained depending on the SiO$_2$-TEOS deposition process parameters. This high field effect mobility is not routinely obtained for 4H-SiC (0001) Si face MOSFETs with only thermal oxidation processes as gate dielectric. Indeed, only few processes (based on nitridation or contaminated oxides) have been reported to be effective to achieve that field-effect mobility level on 4H-SiC. In addition, higher peak mobility, up to a record value of 216 cm^2/Vs, is achieved for MOSFET fabricated in the (11-20) face, compared with (0001) face for a given TEOS gate oxide. This mobility value is also higher than previous values obtained on (11-20) face using thermal oxides. Taking into account the threshold voltage and the sub-threshold slope (S), we can see that we have three ways to increase the mobility. First, by using (11-20) face material as already proposed. Second, by reducing the interface traps density as done with some TEOS process. And third, in the most favorable conditions obtained with other TEOS deposition process, the mobility improvement seems to be related with the current leakage more than (or together with) an interface traps reduction of the gate insulator. This last statement agrees with the high value of S measured in the high mobility devices or with the presence of oxide charges that provokes a shift of the threshold voltage.

Finally, as innovative gate oxide definition process, we propose the N$_2$O oxidation of thin Si layers deposited on 4H-SiC by means of Rapid Thermal Chemical Vapor Deposition (RTCVD). With this procedure, it is possible to combine the known beneficial effects in nitridated oxides with the growth of a stable free carbon SiO$_2$ layer from the deposited Si layer. In addition, this technique could allow obtaining SiO$_2$ thicker layers adequate for passivation purposes, when compared with direct SiC N$_2$O oxidation. D$_{it}$ is reduced (when compared with a N$_2$O oxidation) for interface traps lying in the $E_C - E_T$=0.3-0.6 eV range and a reduced band bending fluctuation (implying a more homogeneous charge distribution at the interface, approaching to a Si/SiO$_2$ interface) have been obtained for N$_2$O RTCVD Si layers. AFM measurements have revealed an adequate smooth surface topology for the fabrication of MOS gated devices.

References

[1] V. V. Afanas'ev, M. Bassler, G. Pensl, and M. Schulz, , *Phys. Stat. Sol. (a)* **162**, 321, (1997).

[2] H. Yano, T. Hatayama, Y. Uraoka and T. Fuyuki, *Mater. Sci. Forum* **483-485**, 685, (2005).

[3] A. Gölz, S. Grof, R. Janssen, E. Stein von Kamienski, H. Kurz, *Diamond Relat. Mater.*, **6**, 1420, (1997).

[4] S. Sridevan and B. J. Baliga, *IEEE Electron Device Lett.* **19**, 228, (1998).

[5] D. Alok, E. Arnold, and R. Egloff, *Mater. Sci. Forum* **338-342**, 1077, (2000).

[6] S. Sridevan, and B. J. Baliga, *Mater. Sci. Forum* **264-268**, 997, (1998).

[7] D. Alok, E. Arnold, R. Egloff, and S. Mukherjee, United States Patent and Trademark Office 6,559,068 (2003).

[8] X. W. Wang, J. Luo, and T-P. Ma, *IEEE Trans. Electron Devices* **47**, 458, (2000).

[9] X. W. Wang, Y. Takahashi, T. P. Ma, C. J. Cui, T. Tamagawa, B. Halpern, and J. J. Schmitt, *Mater. Sci. Forum* **264-268**, 865, (1998).

[10] S. Sridevan, V. Misra, P. K. McLarty, B. J. Baliga, J. J. Wortman, *IEEE Electron Device Lett.* **16**, 524, (1995).

[11] C. J. Scozzie and J. M. McGarrity, *Proceedings of the High Temperature Electronics Conference*, Albuquerque (NM) USA, June 14 to 18, 23, (1998).

[12] L. A. Lipkin, and J. W. Palmour, *IEEE Trans. Electron Devices* **46**, 525, (1999).

[13] L. A. Lipkin, D. B. Slater,Jr., and J.W. Palmour, *Mater. Sci. Forum* **264-268**, 853, (1998).

[14] T. Billon, E. Bano, L. Di Cioccio, T. Ouisse, P. Lassagne and C. Jaussaud, *Microelectronic Engineering*, **28**, 193, (1995).

[15] M. K. Das, *Mater. Sci. Forum* **457-460**, 1275, (2004).

[16] W. Cho, R. Kosugi, J. Senzaki, K. Fukuda, K. Arai, and S. Suzuki, *Appl. Phys. Lett.* **77**, 2054, (2000).

[17] D. M. Dobkin, and M. K. Zuraw, *Principles of Chemical Vapor Deposition: What's Going on Inside the Reactor?*, Kluwer Academic Publishers, (2003).

[18] D. M. Dobkin, *Chemical Vapor Tutorial*, http://www.enigmatic-consulting.com/

[19] M. Ceiler, B. Kohl, and S. Bidstrup, *J. Electrochemical Soc.* **142**, 2067, (1995).

[20] E. H. Nicollian and J. R. Brews, *MOS Physics and Technology*, Wiley, New York (1982).

[21] S. M. Sze, *Physics of Semiconductor Devices*, Wiley, New York, (1969).

[22] K. Kamimura, D. Kobayashi, S. Okada, T. Mizuguchi, E. Ryu, R. Hayashibe, F. Nagaune and Y. Onuma, *Appl. Surf. Sci.* **184**, 346, (2001).

[23] K. Ramanujam, H. Furuichi, K. Taguchi, S. Yukumoto and S. Nishino, *Mater. Sci. Forum* **483-485**, 677, (2005).

[24] K. Fujino, Y. Nishimoto, N. Tokumasu, and K. Maeda, *J. Electrochemical Soc.* **137**, 2883, (1990).

[25] E.Ö.Sveinbjörnsson, H. Ö. Ólafsson, G. Gudjónsson, F.Allerstam, P.-Å. Nilsson, M. Syväjärvi, R. Yakimova, C. Hallin, T. Rödle, R. Jos, *Mater. Sci. Forum* **483-485**, 841, (2005).

[26] M. K. Das, *Mater. Sci. Forum* vol. **457-460**, 1275, (2004).

[27] A. Pérez-Tomás, P. Godignon, N. Mestres, J. Montserrat, and J. Millán,, *Mater. Sci. Forum* vol. **483-485**, 713, (2005).

[28] H. Ö. Ólafsson, *Detection and removal of traps at the SiO$_2$/SiC interface*. Thesis dissertation. Chalmers University of Technology, Sweden, (2004).

[29] E. Arnold, D. Alok, *IEEE Trans. Elect. Dev.* **48**, 1870, (2001).

[30] L. A. Lipkin, M. K. Das and J. W. Palmour, *Mater. Sci. Forum* **389-393**, 985, (2002).

[31] P. Jamet and S. Dimitrijev, *Appl. Phys. Lett.* **79**, 323, (2001).

[32] K. Y. Cheong, S. Dimitrijev, J. Han, and H. B. Harrison, *J. Appl. Phys.* **93**, 5682, (2003).

[33] V. V. Afanas'ev, A. Stesmans, F. Ciobanu, G. Pensl, K. Y. Cheong and S. Dimitrijev, *Appl. Phys. Lett.* **82**, 323, (2003).

[34] A. Pérez-Tomás, D. Tournier, P. Godignon, N. Mestres, and J. Millán, *Mater. Sci. Forum*, **483-485**, 673, (2005).

[35] J. Tan, M. K. Das, J. A. Cooper, Jr, and M. R. Melloch, *Appl. Phys. Lett.* **70**, 2280, (1997).

[36] S. Kaneko, H. Tanaka, Y. Shimoda, N. Kiritani, S. Tanimoto, M. Yamanaka and M. Hoshi, *Mater. Sci. Forum* **389-393**, 1073, (2002).

[37] T. Noma, T. Yonehara, and H. Kumoni. *Appl. Phys. Lett.* **59**, 653, (1991).

[38] E. Ibok, and S. Garg, *J. Electrochemical Soc.* **140**, 2927, (1993).

[39] C. Cobianu, O. Popa, and D. Dascalu, *IEEE Electrón Dev. Lett.*, **14**, 213, (1993).

[40] H.V. Nguyen. Y. Lu, S. Kim, M. Wakagi, and R. W. Collins, *Phys. Rev. Lett.* **74**, 3880, (1995).

[41] X. L. Xu, R. T. Kuehn, J. J. Wortman, and M. C. Özturk, *Appl. Phys. Lett.* **60**, 3063, (1992).

[42] E. H. Nicollian and A. Goetzberger, *Bell Syst. Tech. J.* **46**, 1055, (1967).

Chapter VI

Alternative high-*k* gate dielectrics

Silicon carbide is a promising material for power electronics because of its wide band gap and high breakdown field, saturation drift velocity and thermal conductivity. Additionally, the material is attractive because, like Si, its native oxide is SiO_2. The use of amorphous, thermally grown SiO_2 as a gate dielectric offers several key advantages in CMOS processing, including a thermodynamic and electrical stable interface, as well as superior electrical isolation properties. However, oxides grown on SiC with high interface-state density and a large amount of fixed charges, especially for the SiO_2 /p-SiC structure, have been reported[1,2]. The development of commercial SiC metal–oxide–semiconductor field effect transistors (MOSFETs) has been impeded by the low effective carrier mobility in the MOS channel that is directly linked to interface defects that either trap or scatter carriers[3]. The use of alternative dielectrics as gate material, with a higher dielectric constant can be considered as a valuable alternative in order to enhance the channel conduction in MOSFETS and reduce the oxide degradation due to current injection[4]. Additionally, one approach to improving the insulator reliability of MIS devices is to utilize a dielectric material with a higher dielectric constant than SiO_2. Gauss' law ($\nabla \varepsilon_r \varepsilon_0 \vec{E} = 0$) requires the product of the relative dielectric constant and the normal field of two materials to be constant at their interface ($\varepsilon_{r1}\vec{E}_1 = \varepsilon_{r2}\vec{E}_2$). SiC has a higher dielectric constant than SiO_2. Therefore, a material with a dielectric constant higher than that of SiC will have a lower electric field than the adjacent SiC, reducing its dielectric stress.

6.1. Ta$_2$Si thermal oxidation, a simple route to a high-*k* gate dielectric on SiC

Nowadays, extensive research and development efforts to grow high-*k* dielectrics on semiconductors are underway. Applications include extending the limits of transistor gate capacitance beyond that of ultra-thin silicon dioxide[5], and to improve passivation

layers and gate dielectric reliability in wide band gap semiconductor devices. In this sense, we propose the use of deposited and oxidized Tantalum silicide (Ta_2Si) films on 4H-SiC substrates as dielectric in metal-insulator-semiconductor structures. Tantalum silicide is oxidized to form Ta_2O_5 and SiO_2, with a high effective dielectric constant, due to its unique oxidation properties[6]. The feasibility of this insulator on SiC (and on Si) has been firstly proposed in the framework of this thesis[7].

In this section, the main structural and electrical properties of deposited and thermal oxidized (dry O_2) Ta_2Si layers on 4H-SiC and Si are examined. The oxidized layers present correct film topology, enhanced interface properties, relatively low leakage current and are fully compatible with the SiC CMOS processes and thus, these layers can be successfully used as high-*k* dielectric in SiC MOS gated devices as we demonstrate in this chapter.

6.1.1. Experimental Details

Ta_2Si films ranging 15-60 nm thickness have been deposited by direct sputtering on n-type 4H-SiC (and 6H-SiC) substrates after a cleaning procedure based on three H_2O_2 containing etch solutions ($H_2SO_4:H_2O_2$, $HCl:H_2O_2$, $NH_3:H_2O_2$). The substrates have not been heated during the Ta_2Si deposition. X-ray diffraction analysis showed no specific peaks of Ta, Si or Ta_2Si, indicating that the as-deposited films were amorphous. Following the deposition the samples have been oxidized in dry environment at atmospheric pressure during 120 min at 750 ^{o}C and 850 ^{o}C, 90 min at 950 ^{o}C and 60 min at 1050 ^{o}C. For the sake of comparison, Ta_2Si films ranging 15-50 nm have been deposited and oxidized at 850 ^{o}C, 950 ^{o}C and 1050 ^{o}C on n-type and p-type Si substrates, in the same furnace under the same conditions. For electrical characterization of the dielectric layers, MIS (Metal-Insulator-Semiconductor) capacitors have been fabricated on SiC and Si substrates.

6.1.2. Physical Characterization

As stated before, after deposition of the Ta_2Si layers, X-ray diffraction analysis showed no specific peaks of Ta, Si or Ta_2Si, indicating that the as-deposited films were amorphous to the crystallinity level detectable. Rutherford Backscattering Spectrometry (RBS) measurements on deposited Ta_2Si films on top of 4H-SiC give a composition very close to stoichiometry within the experimental error.
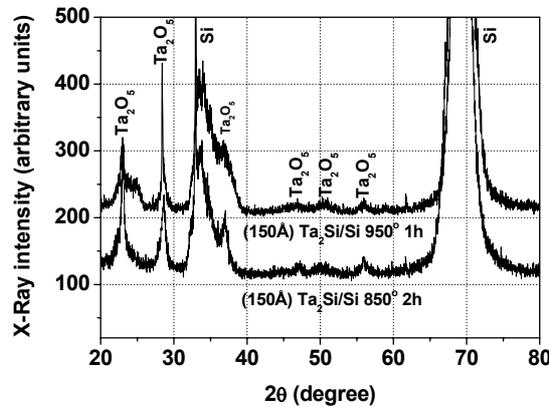
Fig. 6.1. XRD theta-2theta scan of Ta_2Si films deposited and oxidized on p-type Silicon at 850 ^{o}C (2 h) and 950 ^{o}C(1 h).

Using X-ray diffraction analysis, after oxidation Ta_2O_5 peaks are clearly evidenced implying an hexagonal [8-11] δ-Ta_2O_5 (ε_r=25-57) phase on p-Si (Fig. 6.1) and n-type 4H-SiC (Fig. 6.2) substrates. The Ta_2O_5 crystalline structure coincides with the most common reported configuration after direct tantalum pentoxide deposition by sputtering or by LPCVD and subsequent annealing [12,13]. At 750ºC, the diffraction of the incipient crystalline δ-Ta_2O_5 layers is too weak, and only the 4H-SiC substrate peaks are observed. No peaks corresponding to Ta, Si or Ta_2Si have been observed.
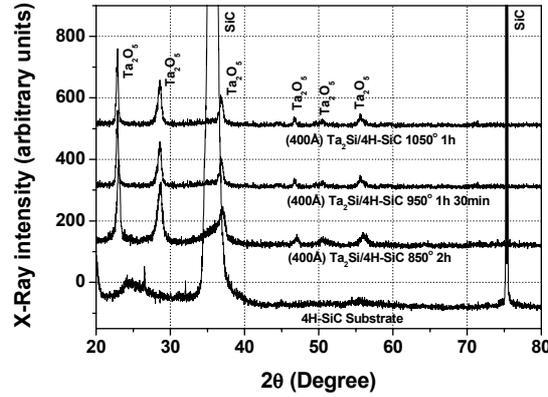
Fig. 6.2. XRD theta-2theta scans of 40 nm Ta_2Si films deposited on n-type 4H-SiC and oxidized under different conditions.

This fact is due to the unique oxidation properties of Ta_2Si. No other silicides are formed, as it occurs when the common Tantalum disilicide ($TaSi_2$) thermal oxidation on silicon is performed (instead of the rare silicide here considered, Ta_2Si). During the oxidation of Ta_2Si, only the formation of SiO_2 and Ta_2O_5 is predicted, as it is shown by ternary phase diagrams[6], using thermodynamic considerations in thin-films reactions (Fig. 6.3). This fact agrees with the study of Cros et al.[14] carried out at room temperature on Si. Other previous works[14,15] (always using Si as semiconductor substrate) have pointed out that when oxidation (1000 ºC) of deposited Tantalum disilicide ($TaSi_2$) on silicon is performed, Ta is poorly oxidized due to its diffusion through the underneath silicon and SiO_2 is mainly formed.
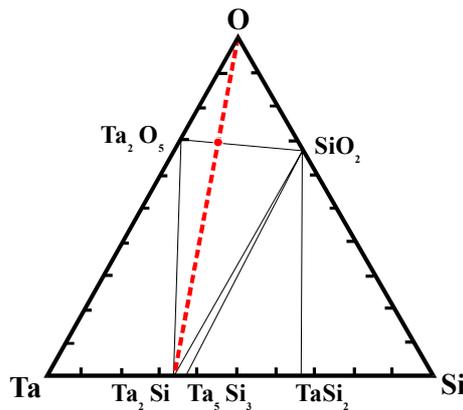
Fig. 6.3. Ternary representations of Tantalum silicide oxidation on inert substrates[6]. SiO_2 and Ta_2O_5, but not Ta, $TaSi_2$ or Si, are possible products of Ta_2Si.

Nevertheless, when $TaSi_2$ oxidation takes place on an inert substrate, such as a SiO_2 layer, both SiO_2 and Ta_2O_5 species are achieved. In the same way, when Tantalum

silicide (Ta$_2$Si) is considered instead of Tantalum disilicide (TaSi$_2$), both Ta$_2$O$_5$ and SiO$_2$ are formed directly on the semiconductor as we also evidence in this work. As shown in Fig. 6.3, any phase having a tie line which intersects the line drawn between oxygen and the Tantalum silicide is a possible oxidation product.

The oxide nature strongly depends on oxidation temperature when Ta$_2$Si is deposited on a Si substrate. At the range of oxidation temperatures considered, both Ta$_2$Si and bulk Si oxidation occur. Thus, the nature of the insulator grown during thermal oxidation of Ta$_2$Si on Silicon can be explained assuming that the process is controlled by the competition between diffusion of oxygen in the oxide and diffusion of silicon in the Ta$_2$Si layer [15].

Cross-section TEM (XTEM) observations on thermal oxidized Ta$_2$Si layers on 4H-SiC substrates reveal the presence of two different layers as clearly evidenced in Fig. 6.4.
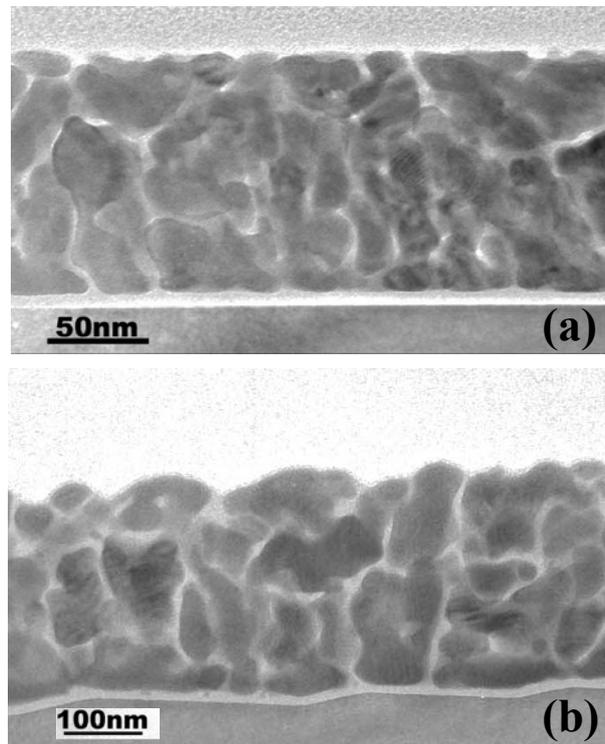
Fig. 6.4. Cross-sectional TEM images of two Ta$_2$Si films deposited and oxidized on 4H-SiC: (a) 40 nm Ta$_2$Si 1050 ^{o}C 1 h, (b) 60 nm Ta$_2$Si 850 ^{o}C 2 h. The δ-Ta$_2$O$_5$ grains with SiO$_x$ channels and the interfacial layer are evidenced.

The bulk insulator consists of polycrystalline Ta$_2$O$_5$ rich grains separated with amorphous SiO$_x$ (presumably SiO$_2$) channels. The width of these channels is larger close to the upper surface. Steps are also evident on the SiC surface for the 850 ºC oxidized sample. The steps are due to the 8º substrate miss cut. An interfacial layer composed of amorphous SiO$_x$ is also formed. The composition of the amorphous channels and the interfacial layer seems to be identical and Ta is not detected in the layer close to the substrate as we will show further on. The oxidation or annealing temperature increase results in a significant narrowing and densification of the amorphous SiO$_x$ channels. Analogously, the interfacial layer becomes thicker when increasing the oxidation temperature. The bulk insulator thicknesses are 195 nm and

130nm with an interfacial layer thicknesses of 4 nm and 9 nm for the samples of Fig. 6.4(a) and Fig. 6.4(b), respectively. The comparison of the cross-sectional TEM (XTEM) observations on 4H-SiC and Si samples confirms the existence of two different layers. One, A labeled in Fig. 6.5, consisting of grains of polycrystalline Ta_2O_5 separated by amorphous SiO_x channels. The B region is the interfacial dielectric (SiO_x) layer. Although the applied thermal treatment was the same for Si and SiC samples; on Si substrates, the SiO_x channels in the A region are very narrow and dense. The interfacial layer is also thicker, due to the higher oxidation rate of Si compared with SiC. On 4H-SiC substrates, the oxidation temperature increase results in a significant narrowing and densification of amorphous SiO_x channels. The interfacial layer becomes thicker when increasing the oxidation temperature, as it has been inferred from TEM measurements. Ta_2Si oxidation at 950 °C or at lower temperatures practically has no effect on the SiC surface, avoiding possible problems related with carbon SiC surface liberation. At the range of 950-1050 °C, the formation of an ultra-thin SiO_x interfacial layer (few nanometers) due to SiC surface oxidation may result from oxygen diffusion across Ta_2O_5 and SiO_x layers.
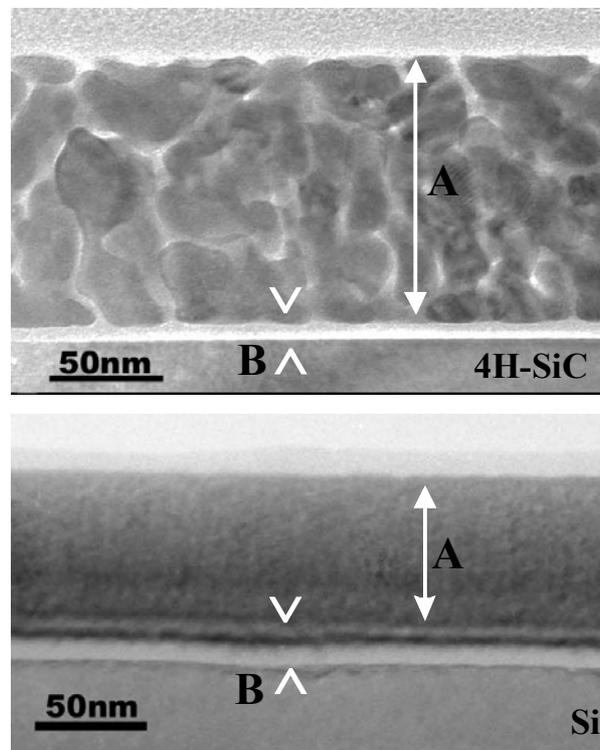
Fig. 6.5. Cross-sectional TEM images of deposited Ta_2Si films on 4H-SiC and on Si, and oxidized at 1050 °C and 850 °C, respectively.

Fig. 6.6. presents the detail of the interfacial layer of both a 60 nm deposited Ta_2Si and oxidized at 850 °C during 2 h on both Si and SiC substrates. Some structural properties in the interfacial layer can also be stressed when the Tantalum silicide oxidation occurs on a Si substrate. In this case, the interfacial layer seems to be formed with a double SiO_x structure with a crystalline δ-Ta_2O_5 rich layer between them. The SiO_x layer close to the interface could be formed from the Si surface oxidation. The upper SiO_x interfacial layer is created from the Tantalum silicide oxidation process since the SiO_x tends to accumulate at the semiconductor interface or for thermodynamic instabilities in the semiconductor surface. In this sense, the thin (~2 nm) Ta_2O_5 rich

layer origin can be explained considering the competition of the Si substrate and Ta_2Si oxidation with different oxidation rates.
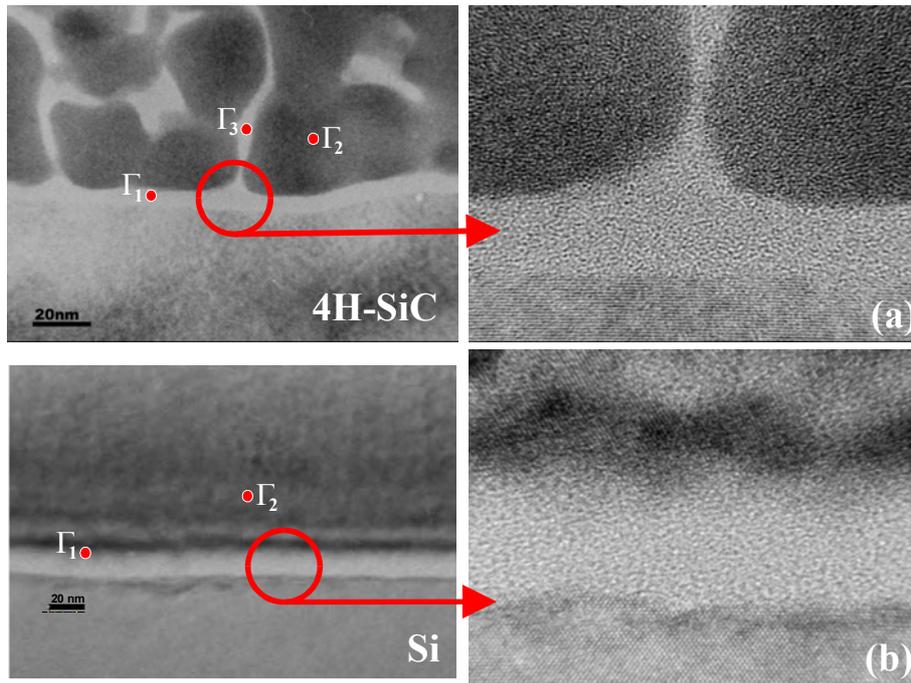
Fig. 6.6. Detailed interfacial TEM images of deposited Ta_2Si films on 4H-SiC (a) and on Si (b), and oxidized at 850 ºC.

(a)　　　　　　　　　　　　**(b)**
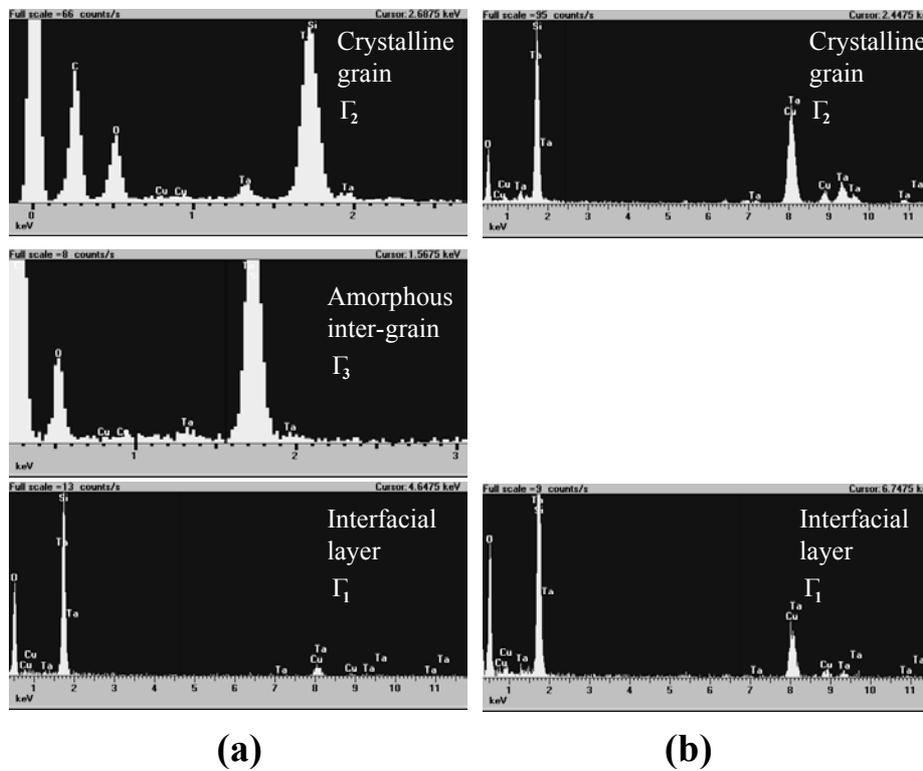
Fig. 6.7. EDX spectra of deposited Ta_2Si films and oxidized at 850 ºC (2 h), (a) on 4H-SiC and (b) on Si,

EDX (Energy Dispersive X-ray) analysis have corroborated that Ta is not present in the interfacial layer. Composition measurements have been performed in three different regions of the insulator, the interfacial layer (Γ_1), the crystalline grain (Γ_2) and the amorphous inter-grain regions (Γ_3). Fig. 6.7 shows the different species detected in EDX measurements. Although the Ta and Si peaks superposition, it is clear that Ta is not detected in neither the interface layer nor the amorphous inter-grains. SIMS depth profile measurements have corroborated a SiO_x accumulation and a Tantalum concentration decrease near the SiC surface, suggesting a SiO_x/SiC based interface (Fig. 6.8 and Fig. 6.9).
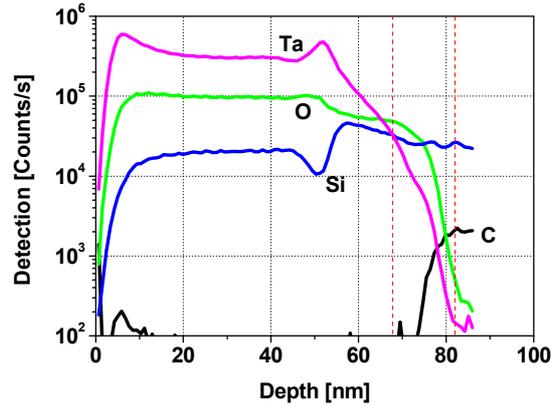
Fig. 6.8. SIMS depth profile of oxidized Ta_2Si (15 nm) films on 4H-SiC.
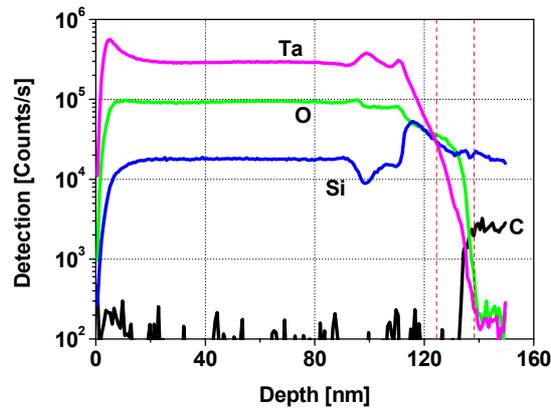
Fig. 6.9. SIMS depth profile of oxidized Ta_2Si (40 nm) films on 4H-SiC.

The surface topography has been investigated by AFM (Atomic Force Microscope) and SEM (Scanning Electron Microscope) measurements. Microscopy measurements, in 4H-SiC samples, shows that the dielectric layer roughness decreases when the oxidation temperature is increased due to Ta_2O_5 grains coalescence along with inter-grains channels SiO_x densification as it is shown in Fig. 6.10 and Fig. 6.11. AFM images before deposition show smooth surfaces with typical RMS values below 1nm. At the lower oxidation temperature, 750 ºC, the δ-Ta_2O_5-rich layers form islands or facets probably caused by its high adatom diffusibity. Thus, the film roughness increases dramatically upon the structural transition from amorphous to crystalline films in the oxidation process. The most common thin film growth kinetic theories[16] agree with considering temperature as a beneficial factor on the diffusion effect due to higher surface diffusibity. Hence, if the surface diffusion dominates the growing process, the

columnar structure is diminished and the layer tends to coalesce becoming a complete layer and erasing the initial surface configuration. The formation of islands becomes more effective at 850 ºC, competing with Tantalum pentoxide diffusion through the surface. The insulator layer presents a considerable roughness (RMS=28 nm). The island coalescence increases at 950 ºC, providing a more regular surface but with numerous craters (RMS=15 nm). Finally, at 1050 ºC one achieves the smoothest surface with RMS=2.9 nm.
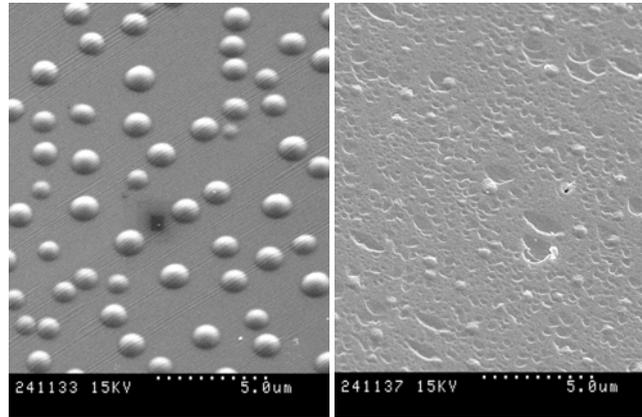
Fig. 6.10. SEM images of 400 Å deposited Ta_2Si on 4H-SiC and oxidized at 750 ºC during 120 min (left) and at 950 ºC during 90 min (right).

(a)   **(b)**   **(c)**   **(d)**
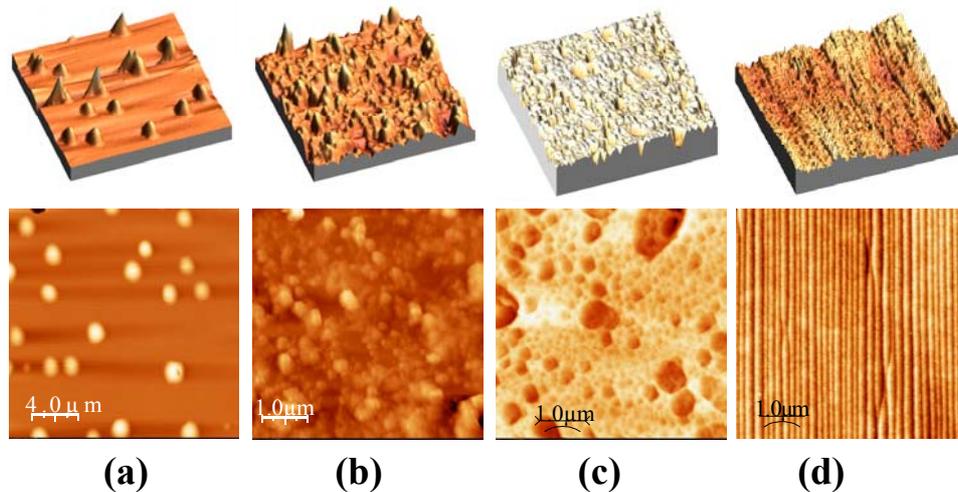
Fig. 6.11. AFM images of Ta_2Si films deposited and oxidized on 4H-SiC.(a) 750 ºC 2 h, (b) 850 ºC 2 h, (c) 950 ºC 90 m, (d) 1050 ºC 1 h.

At the oxidation temperatures range, in the Si samples, both Ta_2Si and bulk Si oxidations occur. Thus, the structural properties of the insulator grown during thermal oxidation of Ta_2Si on Silicon can be explained assuming that the process is controlled by the competition between the diffusion of oxygen in the oxide and the diffusion of silicon in the Ta_2Si layers. The narrowing and densification of channels also influence the layer surface characteristics, as shown in Fig. 6.12. On Si substrates, a smooth surface is obtained independently of the oxidation temperature (RMS<1 nm).

(a)   **(b)**   **(c)**
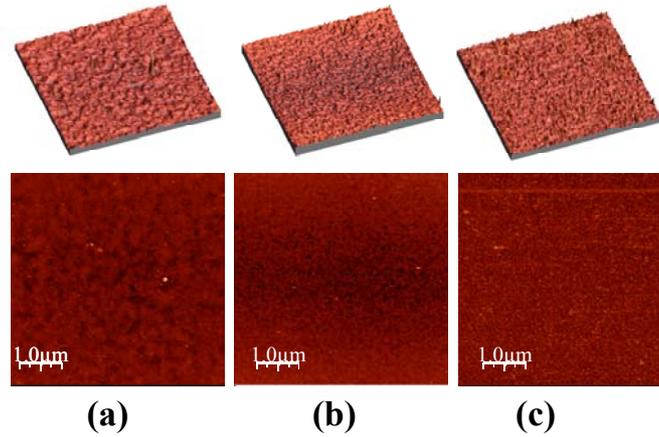
Fig. 6.12. Surface topology of Ta$_2$Si films oxidized on Si at, (a) 850 ºC 2 h, (b) 950 ºC 90 min, (c) 1050 ºC 1 h.

6.1.3. Insulating Properties

It is expected that defect states play an important role in the leakage current characteristics of oxidized Ta$_2$Si films as it occurs in pure Ta$_2$O$_5$ films. The origin of these defects, in Ta$_2$O$_5$ capacitors on Si, has been suggested[17] to be O vacancies (insufficiently oxidized Ta), and Si/O vacancy complexes (insufficiently oxidized Si), that can cause current in Ta$_2$O$_5$ films. Fleming *et al.*[18] suggested that the defects present in the dielectric layer form a defect band that spans the width of the film, and conduction occurs via this defect band. Phenomenologically, several processes have been invoked to explain conduction in Ta$_2$O$_5$ thin films, including Schottky emission[19,20], Poole-Frenkel [9,21] effect, or Fowler-Nordheim[22] tunneling process.

TEM measurements evidence the stacked structure of the oxidized Ta$_2$Si oxidized films. The interfacial SiO$_x$ layer modifies the electrical response of the high-*k* dielectric layers made up of δ-Ta$_2$O$_5$ and SiO$_x$. Experimentally, most high-*k* materials, in particular pure Ta$_2$O$_5$, result in the formation of a thin interfacial layer at the Si interface[23-25], which can influence the band offset to Si. The appearance of this (almost) inevitable mixed layer, which generally consists of SiO$_2$ and sub-oxides of Si and Ta, is an attribute of both the deposition method and the thermal-oxidation processes. The growth of this layer is favored by the active oxidizing ambient. Its presence is also a result of the oxidation of Si, and the thermodynamic instability of metal oxides in direct contact with Si, unlike what happens during the SiO$_2$ formation. This layer controls the leakage current and may have a great impact on the carriers transport through the capacitor. In our case, the interfacial layer has been found to be free of Ta or other species and seems to be amorphous SiO$_2$-like (SiO$_x$), especially in SiC capacitors.

In Fig. 6.13 the I-V characteristics of MIS capacitors (Al/Oxidized Ta$_2$Si/n-type 4H-SiC) are shown, where the electric field across the insulator, E_{ins}, is $E_{ins} = V / t_{ins}$ (*V* the applied gate voltage and t_{ins} the insulator thickness). The Schottky emission and Poole-Frenkel mechanism present the same characteristics in a *ln(J/E) vs* $E^{1/2}$ plot due to the same voltage dependence on the current density, (the linear dependence of Poole-Frenkel expression is negligible when compared with the exponential dependence). Hence, the way to distinguish both current mechanisms is by determining the slope of

the *ln(J/E) vs E$^{1/2}$* plot (Inset Fig. 6.13) and considering as well, if it is compatible with the high frequency dielectric constant value optically determined or previously reported. In the inset of Fig. 6.13, E_2 indicates the electric field in the A region (Fig. 6.5), E_1 is the electric field at the interfacial layer (B region), and d_1 and d_2 are the B and A region thicknesses, respectively.
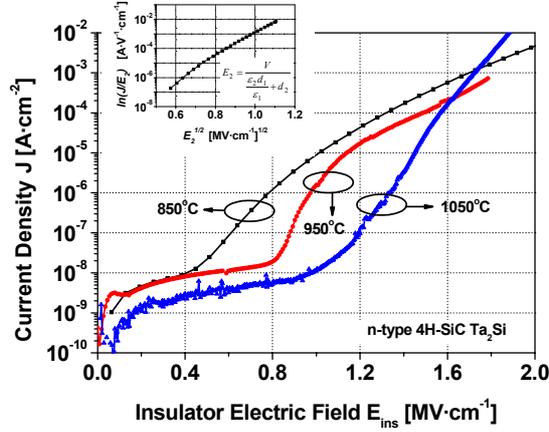
Fig. 6.13. Leakage current in Al/Oxidized Ta$_2$Si/4H-SiC n-type capacitors with different oxidation temperatures. In the inset: Poole-Frenkel plot for 60 nm Ta$_2$Si oxidized at 850 ^{o}C on 4H-SiC substrate. A linear region can be identified indicating a Poole-Frenkel effect conduction mechanism.

When the top electrode is sufficiently positively biased (on n-type MIS structures), electrons injected from the substrate tunnel through the oxide layer to the impurity levels of δ-Ta$_2$O$_5$ before crossing δ-Ta$_2$O$_5$ layer via a one or more defects bands that span the width of the film. As it can be suggested from Fig .6.13, the initial stages of the conduction (at low gate voltages) are sustained by the interfacial SiO$_x$ layer. The samples oxidized at the higher temperature are less leaky due to the thicker (and denser) interfacial layer. Regardless of the oxidation temperature, the current at relatively high gate bias seems to be described with a Poole-Frenkel (or Schottky emission) relation at the insulator bulk (A region), as it can be suggested from the inset of Fig 6.13. In order to quantify the leakage current, a theoretical model accounting for a double hopping and tunnel/Poole-Frenkel conduction mechanism is proposed. The expressions for hopping conduction and Poole-Frenkel mechanism are[26]:

$$J_{HO} = A_1 E \exp\left(-\frac{q\phi_a}{kT}\right) \tag{6.1}$$

$$J_{PF} = A_2 E \exp\left(-\frac{q\phi_t}{kT}\right) \exp\left(\frac{E^{1/2}}{rkT}\sqrt{\frac{q^3}{\pi\varepsilon_0 K_T}}\right) \tag{6.2}$$

where A_1 and A_2 are constants, q is the electronic charge, k denotes the Boltzman constant, T is the temperature, ε_0 denotes the permittivity of free space, K_T is the high frequency dielectric constant, square of the refractive index (n) and E denotes the electric field. Eq. (6.1) corresponds to the electronic hopping conduction process and is attributed to jump of thermally excited electrons from one isolated state to another. The

expression (6.2) describes the Poole-Frenkel effect. This mechanism is based on the emission of trapped electrons towards the dielectric conduction band (barrier height ϕ_t). A coefficient r is introduced in Eq. (6.2) to take into account the influence of the trapping or acceptor centers ($1<r<2$)[27].

Assuming a dielectric constant of $\varepsilon_1=3.9$ for the interfacial layer films and $\varepsilon_2\sim55$ for δ-Ta$_2$O$_5$ layers[9,10], the interfacial layer electric field (B region) is substantially higher than the A region electric field. Such a field is high enough to cause Fowler-Nordheim or direct tunneling injection into the bulk insulator layer when interfacial layer breaks down. Due to the thinness of the SiO$_2$ interfacial layer, electrons are injected from the substrate and tunnel to the impurity levels in Ta$_2$O$_5$ through the SiO$_2$ layer, or are trapped at the Ta$_2$O$_5$ interface, even if a relatively low voltage is applied across the whole capacitor. At low voltages we consider that the conduction mechanism is managed by an electronic hopping conduction process. When $E_1 > 8$ MV/cm, we assume that the interfacial SiO$_x$ layer breaks down and the conduction is led by other of the common current mechanisms in the Ta$_2$O$_5$ films. As it is clearly evidenced in Fig. 6.14, considering the common values reported[9,10,28] for the crystalline δ-Ta$_2$O$_5$ optical refractive index value ($n_{op}\sim2.2$), the good agreement between the experimental data and the theoretical values for Poole-Frenkel mechanism discards Schottky emission, hopping or field emission as possible conduction mechanisms. Schottky emission and Fowler-Nordheim expressions can be found elsewhere[26,29].

Thus, considering the agreement between the proposed model and the experimental data, it can be suggested that the conduction mechanism is due to a hopping mechanism prior to the break down of the interfacial layer and the injection of carriers to the bulk insulator is described by Poole-Frenkel effect. Other conduction mechanisms can be discarded as it can be inferred from Fig. 6.14. From the slope of Poole-Frenkel plots along with the proposed model, the refractive index for the bulk insulator (region A) has been determined ($n_{op}=2.4$ for 60 nm Ta$_2$Si oxidized at 850 ºC on 4H-SiC substrate).
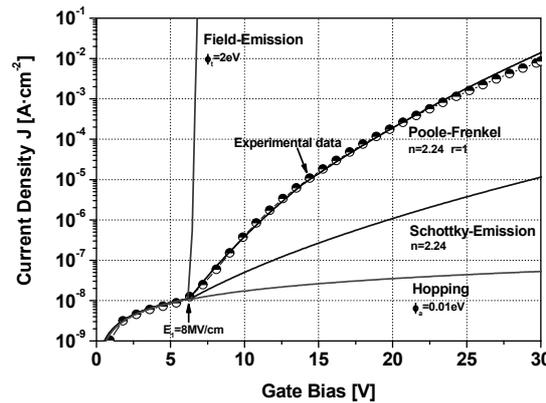
Fig. 6.14. Theoretical (solid lines) and experimental (symbols) leakage current traces from oxidized 60 nm Ta$_2$Si 850 ºC on 4H-SiC substrate.

It is generally assumed that polycrystalline gate dielectrics may be problematic because grain boundaries act as high-leakage paths[4]. If pure Ta$_2$O$_5$ layers are thermally stressed above 600–700 ºC, the deposited layers will become poly-crystalline. However, as previously stated, during deposition of most metal oxides on Si, an interfacial region of SiO$_x$ (Si-Ta-O in the case of Ta$_2$O$_5$ deposited on Si) can be formed. High-temperature

annealing crystallizes the Ta_2O_5 film and converts the composite interfacial oxide to a more stoichiometric SiO_2 layer. Thus, the interfacial layers can reduce the leakage current at low or intermediate electric fields (<1-2 MV/cm). However, the leakage current at high electric fields becomes higher in almost all reported studies. This behavior can be qualitatively explained considering the previously proposed electrical model. If the leakage current is modulated by the conduction mechanism in the interfacial region the injection of carriers into the bulk dielectric will be significantly higher when the interfacial layer breaks down, when compared with a "net" trap assisted Poole-Frenkel effect in the insulator bulk. Hence, the general assumption associating crystallinity with leakage current is not directly applicable in all cases since the interfacial layer modifies the current-voltage response of the dielectric, and this layer becomes almost inevitable in the annealing process, especially in oxidant ambients such as O_2 or N_2O. Additionally, an adequate band offset, to prevent tunneling processes, is a more demanding requirement in a wide band gap semiconductor like SiC than in Si [30,31]. Therefore, the interfacial layer intrinsically obtained oxidiziding Ta_2Si directly on SiC is effective in reducing the current leakage compared to other pure high-*k* insulators on SiC such as MgO [32] or HfO_2 [33].

The high-*k* Ta_2O_5-based Ta_2Si oxidized layer presents significantly structural differences when deposited and oxidized on 4H-SiC and on Si substrates due to the Si substrate diffusion influence or to the 4H-SiC inertness, respectively. Fig. 6.15(a) shows the current-voltage traces for a n-type 40 nm Ta_2Si oxidized at 1050 ºC on 4H-SiC and Si substrates. The Poole-Frenkel characteristic has been observed for both semiconductor substrates at sufficiently high electric fields. The leakage current is reduced on Si capacitors. In both substrates (SiC and Si), analogous insulating properties have been extracted for the minimum insulator thickness considered (40-50 nm) and Poole-Frenkel conduction mechanism can be invoked in these capacitors.

(a)   (b)
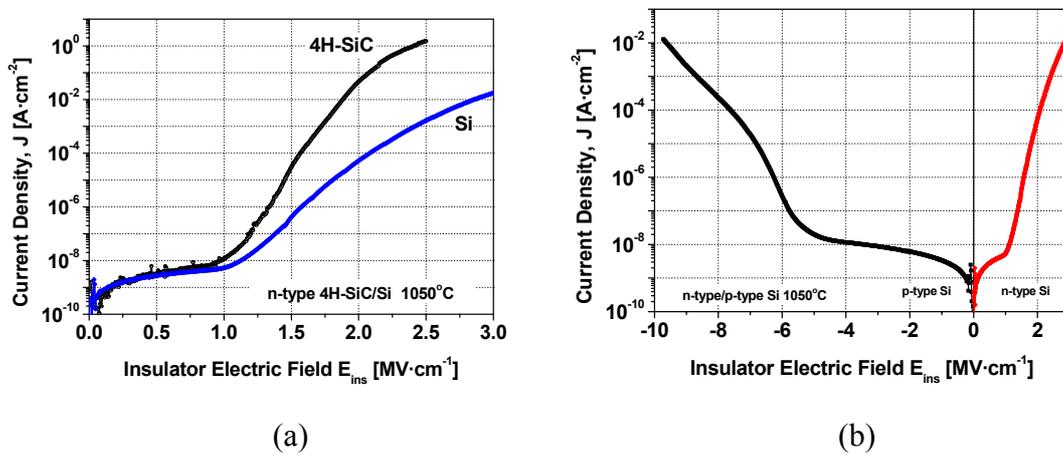
Fig. 6.15. (a) Leakage current of Al/Oxidized Ta_2Si/4H-SiC or Si n-type capacitors. (b) Leakage current of Al/Oxidized Ta_2Si/Si for n-type and p-type capacitors oxidized at 1050ºC.

Considering that the leakage current conduction occurs via a defect band that spans the with of the film, the metal work function difference between the electrodes and the insulator layer can affect the symmetry of the conduction with gate bias polarity[18,34]. This asymmetry detected in thermal oxidized Ta_2Si layers has been verified on Si capacitors (Fig. 6.15(b)). n-type and p-type Si capacitors have been used in order to avoid the undesirable depletion layer effect. An enhanced insulator breakdown

strength (in terms of the restriction of the current flow in MIS capacitor by the depletion layer), is experimented on negatively biased n-type (positively biased p-type) capacitors. The leakage current asymmetry can be qualitatively explained in terms of a higher thermal barrier for electron conduction (via the defect band) since the Fermi level of the top Al electrode is located substantially below the defect band. When a forward bias is applied, a steady state current is detected. Since the Fermi level is pinned at the defect band, little activation energy is needed to excite an electron into the defect band. These electrons must pass through the interfacial layer via a tunnel mechanism. A schematic energy band diagram is presented in Fig. 6.16. The same assessments are valid for SiC substrates since the alignment of bands are expected to be similar, especially for the conduction band.
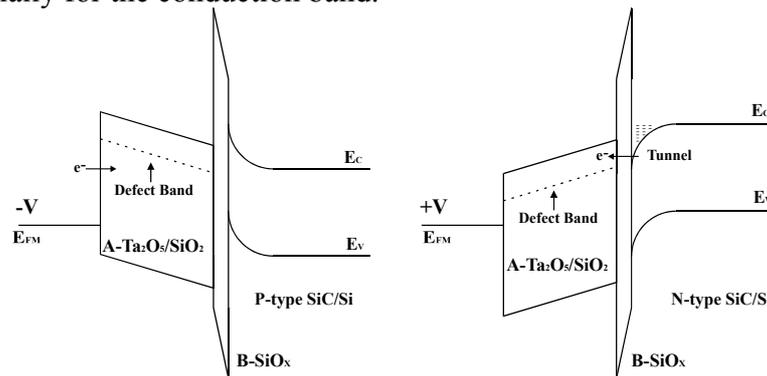
Fig. 6.16. Schematic energy diagrams of the defect band in the MIS structure showing the double conduction mechanism.

In summary, Poole-Frenkel mechanism is detected at sufficiently high bias under all oxidation conditions for both SiC and Si substrates. The oxidation temperature increase provokes a reduction of the leakage current at low gate electric fields. Leakage current shows an asymmetric behavior with the gate bias polarity (gate +V or –V) yielding a leakage current density as low as 10^{-8} Acm^{-2} at 1 MVcm^{-1} and 4.5 MVcm^{-1}, respectively. Different post-deposition treatments have been proposed in order to reduce the leakage current in Ta_2O_5 capacitors on Si, which can be eventually applied to oxidized Ta_2Si structures. Among these process, the most common involve furnace annealing[8,35,36], in N_2, O_2, O_3 or N_2O, rapid thermal annealing (RTA)[8,36-38] also in N_2O or O_2, or doping the Ta_2O_5 films with either Carbon[34] or Zirconium[20].

6.1.4. Capacitance Properties

The high-*k* dielectric constant of the Ta_2Si oxidized layers has been extracted by means of capacitance-voltage measurements. High-frequency and quasistatic measurements[39] have been carried out on our samples. High Frequency C-V measurements have been carried out in all the samples in order to obtain the MIS interface electrical characteristics (see Fig. 6.17). The capacitance measured in strong accumulation (C_I) combined with SIMS or TEM depth profile measurements supply the effective dielectric constant. C-V high frequency curves have been obtained from MIS capacitors with Al or Hg (mercury probe) as gate metal. The mercury probe avoids permanent metal surface contamination and allows diminishing the roughness topography influence upon the measurements.
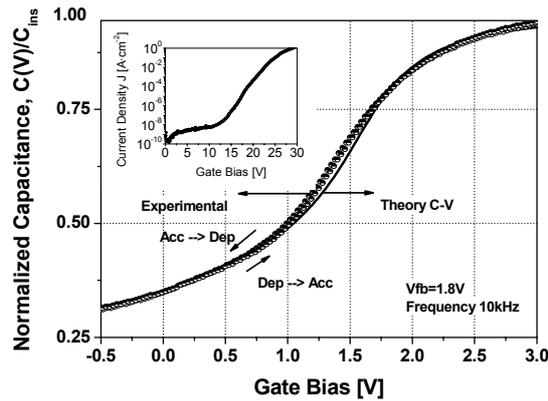
Fig. 6.17. Typical high frequency (100 kHz) C-V plot of 40 nm Ta_2Si deposited and oxidized at 1050 ^oC 1 h. Theoretical plots are simulated using equations found in *Chapter III* and flat-band corrected. I-V measurement is presented in the inset.

Fig. 6.18(a) shows typical C-V curves recorded at 100 kHz for 1050 °C 40 nm 1 h oxidized Ta_2Si on 4H-SiC and on Si substrates. On 4H-SiC substrates, an effective dielectric constant of $\varepsilon_r \sim 20$ has been achieved for the Ta_2Si deposited and oxidized insulating films derived from C-V measurements. The oxidized Ta_2Si layers thickness has been extracted using XTEM, SIMS, X-Ray reflectometry methods, and profilometer analysis etching selectively the Ta_2Si deposited layer before the thermal oxidation. The capacitance value obtained for oxidized Ta_2Si MIS structures on 4H-SiC substrate is only weakly dependent on the oxidation temperature ranging from 850 ^oC to 1050 ^oC. The flat-band value diminishes by increasing the oxidation temperature and with no appreciable hysteresis behavior[40]. The dielectric constant is only slightly dependent of the oxidation temperature although the thickness increase of the interfacial layer. This last result suggests a competition between the interfacial layer thickness increase (and densification) and the recrystallization of the δ-Ta_2O_5 grains that would cause an increment of their dielectric constant.

(a) (b)
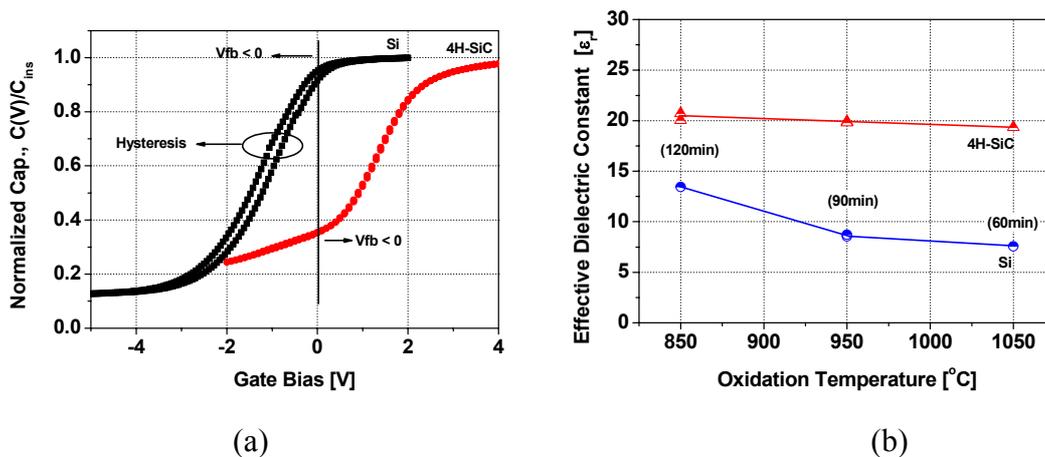
Fig. 6.18. (a) High-frequency C-V characteristics for the MIS capacitors composed by 40 nm Ta_2Si oxidized at 1050 °C 1 h on 4H-SiC and Si substrates. (b) Effective dielectric constant extracted from MIS capacitors biased in strong accumulation.

The C-V measurements obtained for oxidized Ta$_2$Si MIS structures on Si have revealed a clear dependence on the oxidation temperature. This is an indication of the coexistence of Si substrate and Ta$_2$Si diffusion and oxidation processes along with the oxidation of the Si surface (Fig. 6.19). Appreciable hysteresis behavior, evidencing the presence of slow traps in the dielectric, has been routinely obtained. The different oxide nature for Ta$_2$Si oxidized layers along with the different metal-semiconductor workfunction on SiC or Si substrates would be the reason of the flat band voltage discrepancy derived in C-V curves. The effective dielectric constant derived from oxidized Ta$_2$Si/Si capacitors ($\varepsilon_r \sim 10$-7) is significantly lower than on SiC. In addition, the dielectric constant of the MIS structure is reduced when the oxidation temperature is increased as it can be inferred from Fig. 6.18(b).
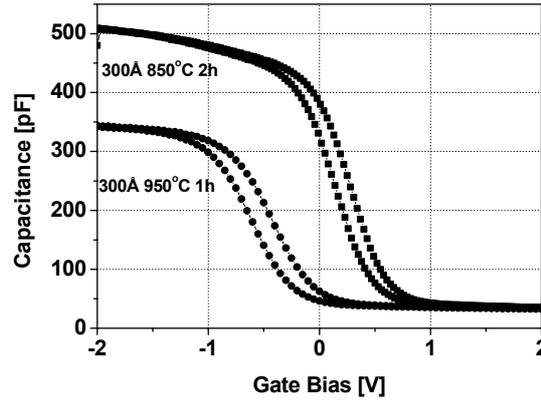
Fig. 6.19. C-V high frequency characteristics of MIS structures composed by Ta$_2$Si films deposited and oxidized on p-type Silicon at 850 ^{o}C (2 h) and 950 ^{o}C(1 h).

The most simple physical (academic) model compatible with the experimental data derived for 4H-SiC MIS structures is based in a stacked insulator composed of an amorphous SiO$_2$ layer and a Ta$_2$O$_5$ polycrystalline layer on the top of this SiO$_2$. However, as it occurs with Si substrates, the formation of an ultra-thin interfacial layer of SiO$_2$ on account of SiC surface oxidation may result from oxygen diffusion across Ta$_2$O$_5$ and SiO$_2$. In 4H-SiC, for all the oxidation temperatures considered, the influence of this thin SiO$_2$ interfacial layer in the insulator capacitance can be neglected due the presence of a much thicker SiO$_2$ layer formed from the Ta$_2$Si oxidation. Thus, if this model is considered, the stoichiometric reaction could be described with

$$Ta_2Si + \frac{7}{2}O_2 \rightarrow Ta_2O_5 + SiO_2 \quad (6.3)$$
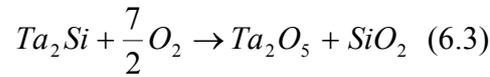
With the Ta$_2$Si oxidation time used, the Ta$_2$O$_5$ crystallization seems to be an ineludible characteristic, because the large oxidation time needed for the complete oxidation of the deposited layer at temperatures lower than 750 ºC make it unfeasible. In this ideal modeling the capacitance experimentally inferred consists of the series combination of two capacitors composed by Ta$_2$O$_5$ ($\varepsilon_{Ta_2O_5}, t_{Ta_2O_5}$) and SiO$_2$ ($\varepsilon_{SiO_2}, t_{SiO_2}$). The thickness of each of these layers can be evaluated using the oxidation equilibrium relation (6.3), the molecular weight ($M_{Ta_2Si}, M_{SiO_2}, M_{Ta_2O_5}$) and the density of the species oxidized or generated in the process ($\rho_{Ta_2Si}, \rho_{SiO_2}, \rho_{Ta_2O_5}$). Analogously, the relative thickness relation between the two oxidation products can be analogously

evaluated[41]. The effective dielectric constant of the insulator derived from the Ta_2Si oxidation can be evaluated from the relative thickness of both layers, SiO_2 and Ta_2O_5 and their dielectric constants.

	Structure	Density [g·cm^{-3}]	Molecular Weigh [g·mol^{-1}]	Volume [cm^{3}mol^{-1}]	Dielectric Constant
Ta_2Si	*Amorphous*	14.0[a]	389.98	27.8	
SiO_2	*Amorphous*	2.2[b]	60.08	27.3	3.9[b]
Ta_2O_5	*Amorphous*	5-6[c]	441.89	80.3	25-26[c]
Ta_2O_5	*δ-orthorhombic*	4-9[d]	441.89	53.9	56-58[d]

Table VI.1. Structural parameters of the species involved in the thermal Ta_2Si oxidation. [a]Ref. 42, [b]Ref. 41, [c,d]Ref. 8-12, 43, 44.

In Table VI.1 these parameters are listed with the dielectric constant value. As it occurs with the thermal oxidation of silicon, a volume expansion takes place during Ta_2Si oxidation. This expansion arises due to the oxygen incorporation to the insulator layer and can be calculated from the density and the molecular weight of the species involved in the oxidation (6.4).

$$\frac{t_{ins}}{t_{Ta_2Si}} = \frac{M_{SiO_2}/\rho_{SiO_2} + M_{Ta_2O_5}/\rho_{Ta_2O_5}}{M_{Ta_2Si}/\rho_{Ta_2Si}} \approx 2.9 \quad (6.4)$$

Therefore, the relationship between the deposited Ta_2Si layer thickness and the oxidized Ta_2Si layer is determined to be around three times thicker the oxidized layer versus the deposited Ta_2Si thickness. This thickness ratio coincides with the thickness ratio experimentally inferred for the SiC MIS structures analyzed. In this sense, the relative thickness relation between the two oxidation products can be analogously evaluated:

$$\frac{t_{Ta_2O_5}}{t_{SiO_2}} = \frac{M_{Ta_2O_5}/\rho_{Ta_2O_5}}{M_{SiO_2}/\rho_{SiO_2}} \approx 2 \quad (6.5)$$

The insulator product of the Ta_2Si oxidation effective dielectric constant can be computed from equations (6.3) and (6.5) as it is shown in equation (6.6)

$$\varepsilon_r = \frac{t_{ins}\varepsilon_{Ta_2O_5}\varepsilon_{SiO_2}}{\varepsilon_{Ta_2O_5}t_{SiO_2} + \varepsilon_{SiO_2}t_{Ta_2O_5}} = \left(1 + \left(\frac{M_{Ta_2O_5}/\rho_{Ta_2O_5}}{M_{SiO_2}/\rho_{SiO_2}}\right)\right)\frac{\varepsilon_{SiO_2}\varepsilon_{Ta_2O_5}}{\left[\varepsilon_{Ta_2O_5} + \varepsilon_{SiO_2}\cdot\left(\frac{M_{Ta_2O_5}/\rho_{Ta_2O_5}}{M_{SiO_2}/\rho_{SiO_2}}\right)\right]} \quad (6.6)$$

In general, the density of a thin Ta_2O_5 film depends on its thickness, the annealing temperature, the crystallization state or the deposition method[12,43]. In Fig. 6.20 the dielectric constant of the insulator stack model is plotted versus the Ta_2O_5 density in the range commonly reported. The dielectric constant values experimentally obtained for insulators grown on n-type 4H-SiC substrates for different oxidation temperatures and deposited thickness of Ta_2Si (~20) is higher than the predicted with the model. As it can be derived from Fig. 6.20, the way to achieve this high value is reducing the Ta_2O_5 density (lower than the densities commonly reported) or increasing

the dielectric constant of the Ta_2O_5 layer (higher than the dielectric constants commonly reported). The origin of this discrepancy could proceed for several sources. (1) The stoichiometric relationship is not exactly as suggested in (6.3) due to diffusion processes or thermodynamic instabilities of the species involved. (2) The density values of Ta_2O_5, especially in its crystalline structure, have not been widely reported. (3) The same could occur with the dielectric constant of the δ-Ta_2O_5 phase. Nevertheless, as stated before, Ta_2O_5 seems to be unstable in contact with silicon and forms an interfacial SiO_x layer. This interfacial layer reduces dramatically the dielectric constant of MIS structures on Si capacitors. Chaneliere *et al.*[9] have suggested electric permittivity values as high as 84 if *really pure* δ-Ta_2O_5 capacitors are considered. This is consistent with the lower dielectric constant observed in Si capacitors where the Si diffusion creates an additional SiO_2 layer that reduces noticeably the insulator dielectric constant.
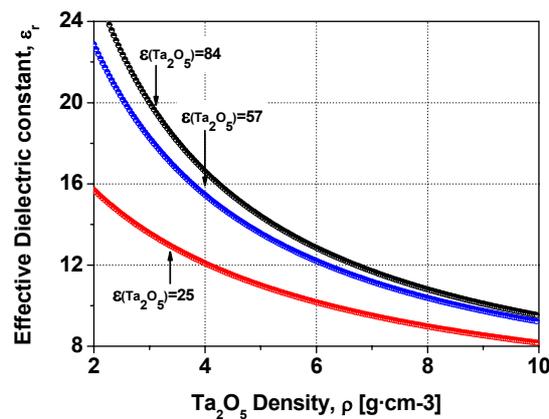
Fig. 6.20. Effective dielectric constant versus Ta_2O_5 density computed with the stack SiO_2-Ta_2O_5 model.

Fig. 6.21 shows a typical quasistatic measurement on 40 nm Ta_2Si oxidized at 850 ºC 4H-SiC capacitor. Theoretical plots are simulated using equations found *Chapter III*. Quasistatic C-V curves are also used to correct doping calculations for the presence of traps, measuring band bending, and for calculating interface traps densities[45].
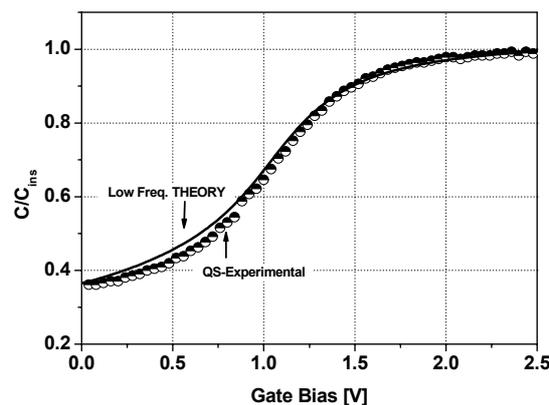
Fig. 6.21. Quasistatic capacitance-voltage characteristic of a MIS capacitor on 4H-SiC (40 nm Ta_2Si oxidized at 850 ºC). Theoretical plots are simulated using equations found in *Chapter III* and flat-band corrected.

The presence of a high quality insulating interfacial layer allows quasistatic measurements, implying a relatively low leakage current when compared with

displacement current in all 4H-SiC samples. However, the quasistatic measurement on Si substrates produces a marked distortion as shown in Fig. 6.22. It should be noted that the quasistatic characteristics obtained by the ramp voltage or the charge-voltage method have not been widely successfully investigated for Ta_2O_5 capacitors on Si. It has been pointed out that the high current leakage is at the origin of the distortion on the quasistatic traces obtained by several authors[9,46]. Nevertheless, the leakage current characteristics for oxidized Ta_2Si/Si samples are slightly better when compared with oxidized $Ta_2Si/4H$-SiC under identical conditions, as stated before. Hence, we would be tempted to assume that the distortion origin in quasistatic traces is not only in the leakage current, at least in oxidized Ta_2Si/Si capacitors.
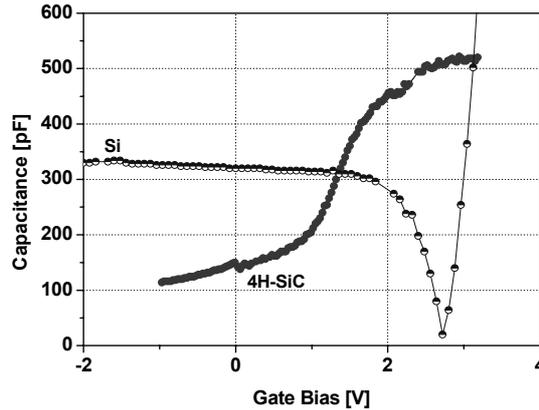
Fig. 6.22. Quasistatic capacitance-voltage characteristic of MIS capacitors on 4H-SiC and Si (40 nm Ta_2Si oxidized at 1050 °C 1 h).

The relative low temperature for a complete Ta_2Si layer oxidation is one of the most attractive features of this new insulator on SiC, since this semiconductor offers a high resistance to thermal oxidation requiring temperatures higher than 1000 °C to be practical. As explained in previous chapters, when SiO_2 is thermally grown, the residual carbon of the interface forms interfacial carbon clusters or supplies dangling bonds[47,48]. These oxidation defects greatly reduce the quality of the SiC/SiO_2 interface. Thus, Ta_2Si oxidation at 950 °C or at lower temperatures practically has no effect on the SiC surface, avoiding possible problems related with carbon liberation at the SiC surface. However, the formation of an ultra-thin SiO_2 interfacial layer (few nanometers) due to SiC surface oxidation, results from oxygen diffusion across Ta_2O_5 and SiO_x layers, as it occurs on Si substrates. It results in the stacked structure SiC/SiO_2 (interfacial)/ SiO_x and Ta_2O_5 (Ta_2Si oxidation).

Experimental results from Ta_2Si thermal oxidation at 850 °C and 950 °C suggest that the poor quality of the interface is mainly due to structural mismatch between the SiC surface and the SiO_x layer created from the Ta_2Si oxidation, since the SiO_2 interfacial layer is extremely thin. Subsequent annealing of these capacitors in inert ambient, strongly improves their electrical reliability as well as their interfacial properties, reducing both flat-band voltage and interface states density (D_{it}). Thus, after the oxidation process, the samples oxidized at 850 °C have been annealed in N_2 during 1h at 950 °C and subsequently at 1050 °C under the same conditions or directly annealed at 1050 °C in N_2 during 1h. The samples oxidized at 950 °C have been annealed at 1050 °C during 1h in N_2. D_{it} has been extracted from all the samples using the conductance method[41]. The traps density spectra has been determined within the band-gap as it is shown in Fig. 6.23, where $E_C - E_T$ is the conduction band energy

minus trap energy. The lowest interface states density has been achieved on samples oxidized at 850ºC and annealed in N_2 at 950 ºC and subsequently at 1050 ºC, resulting 8.5×10^{11} cm^{-2}eV^{-1} at $E_C - E_T$ =0.2 eV. An interface state density of 1.7×10^{12} cm^{-2}eV^{-1} has been extracted at $E_C - E_T$ =0.2 eV on samples oxidized at 850 ºC and directly N_2 annealed at 1050 ºC. Basically, the same D_{it} profile is obtained from samples oxidized at 950 ºC and annealed at 1050 ºC. Thus, the inert atmosphere annealing produces both SiO_2 (interfacial or Ta_2Si oxidized) layer restructuring along with an increase of amorphous SiO_2 in the interface[23,24], improving the SiC/SiO_2 interface characteristics. An oxidation temperature of 1050 ºC or higher is enough to slightly oxidize the SiC surface, and the interfacial properties might be similar to those of a thermal oxidation carried out at such temperature. At 1050 ºC the thermal stress is significantly lower when compared to standard dry thermal oxidation at 1160 ºC. In this case, interfacial oxide films are grown at a slower rate, thus reducing disorder and dangling bonds. This fact, along with the smooth and regular surface obtained, produces an excellent capacitance properties reproducibility. 400 Å Ta_2Si oxidized at 1050 ºC samples show current densities in the range of 10^{-8} A·cm^{-2} up to 15V (the I-V plot for a typical capacitor is shown in the inset of Fig. 6.17). An interface state density of 1.5×10^{12} cm^{-2}eV^{-1} has been determined at $E_C - E_T$ =0.2 eV on these capacitors (see Fig. 6.23).
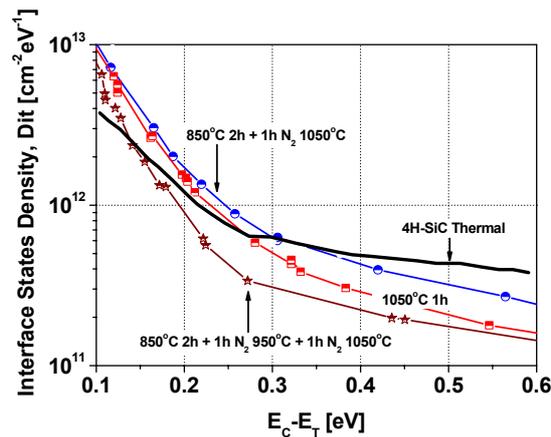
Fig. 6.23. Interface state density spectra as a function of the conduction band energy minus trap energy ($E_C - E_T$) of Ta_2Si films on 4H-SiC oxidized under different conditions.

The structural and insulating trends aimed in the study of the oxidized Ta_2Si on 4H-SiC are also valid for the 6H-SiC polytype, since this last polytype presents the same resistance to thermal oxidation. The main differences could appear in the interfacial properties due to the narrower band-gap of the 6H-SiC polytype (3.02 eV) when compared with the 4H-SiC polytype (3.26 eV). The narrower band-gap of the 6H-SiC polytype is traduced in a lower density of interface states below the conduction band edge and thus, a higher mobility when a thermal oxidation is considered in the gate insulator formation process[49]. The high frequency (100 kHz) C-V characteristics of thermal oxidized Ta_2Si on 6H-SiC substrates are shown in Fig. 6.24. As it can be inferred from the figure, the flat-band voltage is reduced increasing the oxidation temperature and low hysteresis behavior has been extracted under all the oxidation conditions. Nevertheless, the C-V distortion produced by the fast interface traps (the C-V stretch) is noticeably higher when the oxidation temperature of deposited Ta_2Si is

increased. The lowest distortion (an indication of low interface traps) is obtained for the 6H-SiC standard thermal oxidation. Hence, the achievement of low density of interface states is a more demanding issue in the 6H-SiC polytype, when compared with the 4H-SiC polytype, due to the narrower band-gap of this polytype. The interface traps density spectra within the band-gap is presented in Fig. 6.25. The D_{it} spectra has been determined using both conductance and Terman method[41]. The lower D_{it} is obtained for the thermal oxide resulting 2×10^{11} cm^{-2}eV^{-1} at $E_C - E_T$ =0.2 eV. An interface state density of 6×10^{11} cm^{-2}eV^{-1} and 9×10^{11} cm^{-2}eV^{-1} has been obtained at $E_C - E_T$ =0.2 eV for 40 nm deposited Ta$_2$Si and oxidized at 950 ºC (90 min) and 1050 ºC (1 h), respectively.
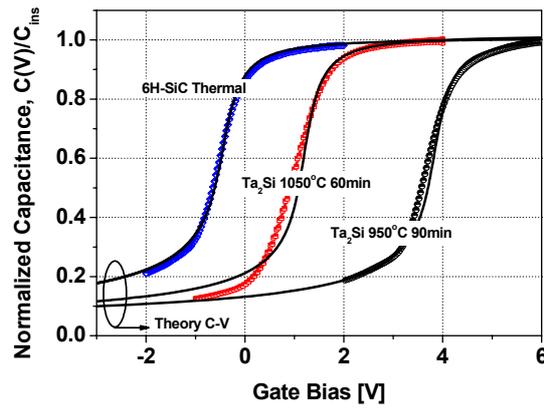
Fig. 6.24. High frequency CV characteristics of the oxidized Ta$_2$Si films on 6H-SiC.
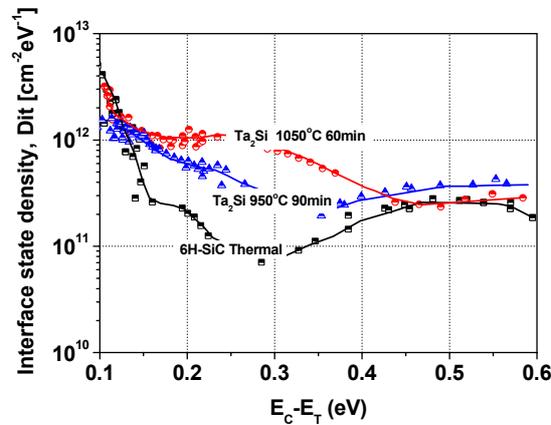
Fig. 6.25. Interface state density spectra of oxidized Ta$_2$Si films on 6H-SiC.

6.1.5. 4H-SiC Ta$_2$Si MOSFETs fabrication

In the previous sections, the main physical and electrical properties of dry oxidized Ta$_2$Si layers, directly on SiC or Si substrates, have been presented and compared. Under such Ta$_2$Si oxidation conditions, the SiC substrate seems to be more adequate for device fabrication since the better definition of the interfacial layer and the higher dielectric constant. An extensive study of Ta$_2$Si silicide oxidation dynamics in dry O$_2$ or other ambients is a very attractive study due the lack of results in the literature[14,50], at least for SiC substrates. Preliminary results aim at considering the oxidation time used in this study to be too long, especially on Si substrates.

In order to demonstrate the feasibility of this insulator as gate material and to verify the compatibility with standard SiC MOSFET fabrication materials and processes, 4H-SiC MOSFETs have been implemented. The schematic of the fabrication process is presented in Fig. 6.26, evidencing the simplicity of the gate MOSFET definition and its compatibility with an existing 4H-SiC MOSFET technology.

Deposition Ta₂Si

(sputtering, 25°C 1atm) ~50nm Ta₂Si

N⁺   N⁺

4H-SiC Substrate

Selective etching Ta₂Si

N⁺   N⁺

4H-SiC Substrate

Ta₂Si oxidation

(1050°C 1h dry O₂)

~150nm O-Ta₂Si

N⁺   N⁺
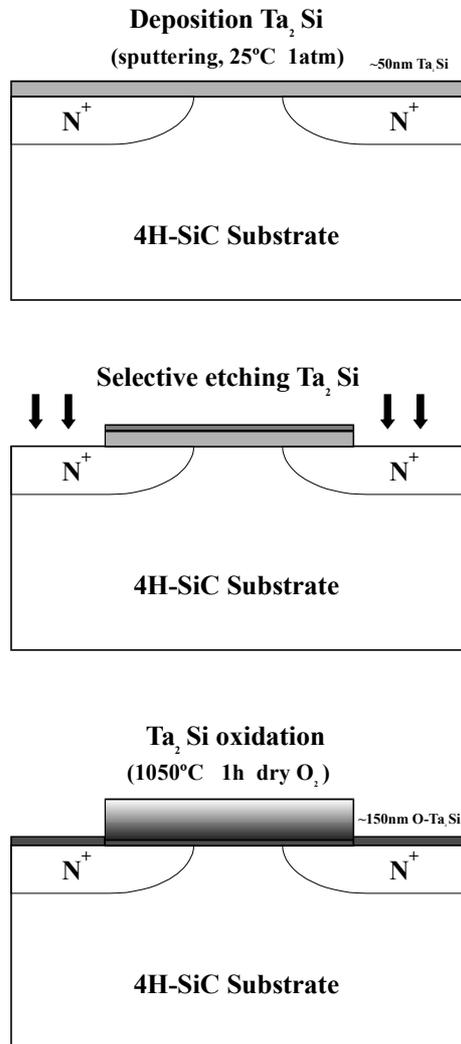
4H-SiC Substrate

Fig. 6.26. Schematic of the 4H-SiC O-Ta$_2$Si MOSFET fabrication process.

4H-SiC N⁻ MOSFETs have been fabricated using a N⁺-type 4H-SiC substrate epitaxied with a P-type layer, with a doping level in the $5 \cdot 10^{16}$ cm⁻³ range, on the 8° off Si (0001) face. The n-channel inversion channel MOSFETS structures have also been fabricated on a p-implanted region for CMOS and power applications. The p-type wells are created by a Boron multiple energy implant (energies ranging 25-320 keV) and posterior RTA (Rapid Thermal Annealing) at 1650 °C. Ta$_2$O$_5$ is highly resistive to many chemicals depending upon its preparation technique and can in fact be employed as a protective coating material against corrosion[12,13]. Therefore, the gate of the transistors has been defined prior to oxidation, etching selectively the Ta$_2$Si deposited layer. All the gate fabrication steeps have been performed in a clean room using dedicated

equipment, in a process fully compatible with standard 4H-SiC MOSFET fabrication. The gate insulator has been grown by dry oxidation of 50 nm deposited Ta_2Si during 1h at 1050 ^oC. The resulting dielectric thickness has been determined to be 150 nm. Evaporated Aluminum and Nickel have been used to form the MOS gate and the source/drain contacts. The dark layer covering the source and drain region after the Ta_2Si oxidation is the residual oxidation of the SiC surface. Subsequently, this thin layer of oxide is removed with an adequate etching (protecting the oxidized Ta_2Si gate) for the contact opening. This is the most simple way to define the gate of the MOSFETs and avoids the introduction of additional masks.
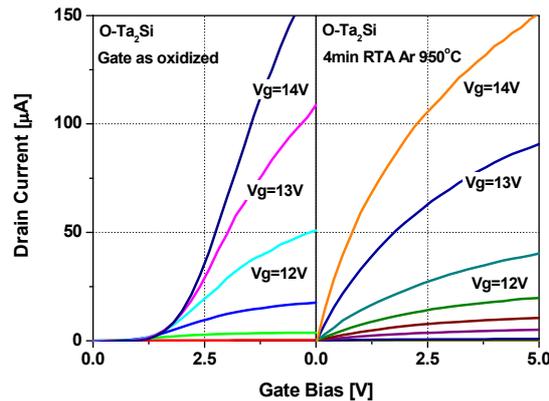
Fig. 6.27. Effect of contact RTA process on drain current characteristics.

After gate and drain/source metal deposition, a contact RTA process must be performed, in order to obtain an ohmic contact on these regions. As it can be inferred from Fig. 6.27, the drain current characteristics are significantly improved carrying out a 4 min RTA in Ar at 950 ºC. Thus, after correcting rectifying effects, the MOSFET is normally off with adequate subthreshold, direct and saturation characteristics. The forward I-V characteristics are plotted in Fig. 6.28, for p-implanted and epitaxial transistors.

(a)   (b)
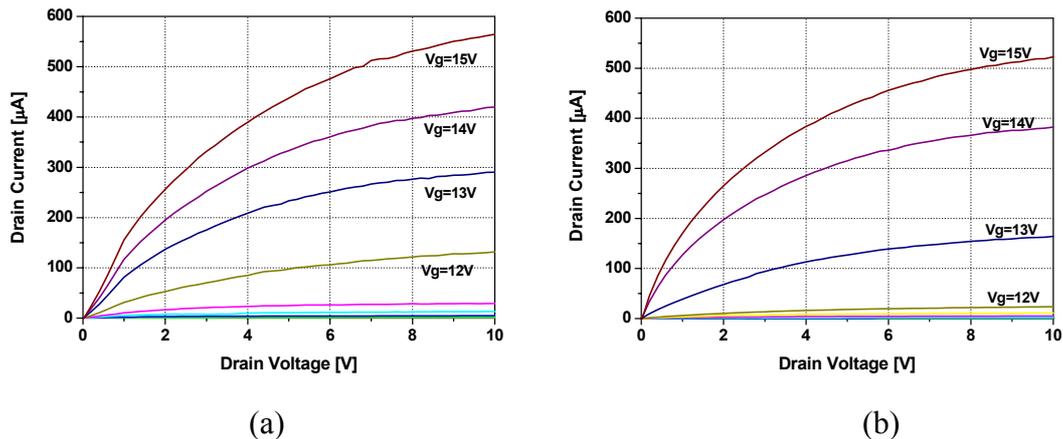
Fig. 6.28. Forward I-V characteristics of oxidized Ta_2Si MOSFET (L =4 μm, W =150 μm) at room temperature (a)on epitaxial layer, (b) on p-implanted layer.

For the MOSFETs fabricated on a p-implanted and annealed region, a peak field effect mobility up to 45 cm^2/Vs has been extracted, as it is shown in Fig. 6.29. The peak mobility is significantly increased for oxidized Ta_2Si MOSFETs when compared with

standard dry thermal oxidized SiO_2 4H-SiC MOSFETs (see *Chapter IV*) and is higher for p-implanted devices. Inversion channel mobility has been found slightly dependent on channel length and presents adequate reproducibility.
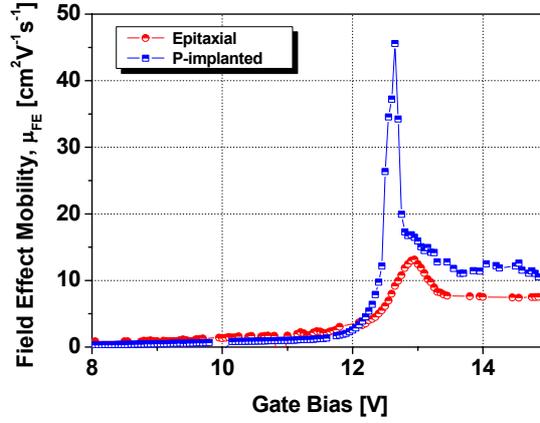
Fig. 6.29. Field effect electron channel mobility in transistors fabricated with oxidized Ta_2Si as gate insulator.

The leakage current limit of 10^{-1} Acm^{-2} is reached at 15 V (Fig. 6.30). This leakage current should be reduced with an adequate passivation and with the use of other gate metals as Ti or TiN instead of Al [51]. The gate leakage current density has been found to be independent of the gate length and the implantation below the O-Ta_2Si gate.
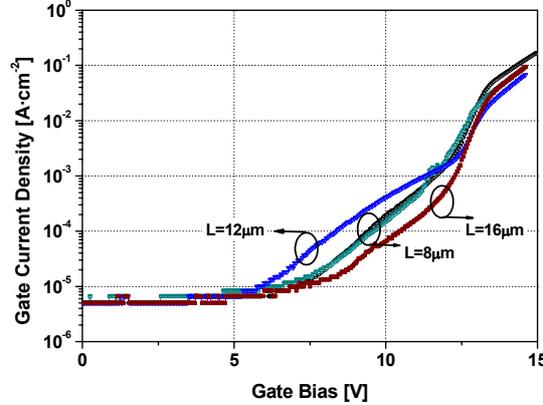
Fig. 6.30. Gate current density for oxidized Ta_2Si for different gate lengths.

One of the main advantages of using a high-*k* dielectric, instead of SiO_2 as gate material, is the increase of drain current in terms of on-resistance[52] (R_{on}) reduction.

$$R_{on} \equiv \frac{\partial V_G}{\partial I_D} = \frac{1}{g_m} = \frac{L}{W\mu_{FE}C_I V_{DS}} \qquad (6.8)$$

where, μ_{FE} is the channel effective mobility, L and W are the channel length and width respectively, C_I the capacitance and V_{DS} the drain bias. As well as efforts in channel mobility improvement, the use of alternative high-*k* materials as gate dielectric,

also reduces the on-state resistance in terms of C_I increase, taking into account the equivalent thickness of oxidized Ta_2Si layers. Fig. 6.31 compares the measured drain current versus gate voltage characteristics of a long channel (L=4 μm) n-channel MOSFET with 40 nm of thermally grown SiO_2 (named T-SiO_2) with the oxidized Ta_2Si MOSFET (named O-Ta_2Si). The 150 nm O-Ta_2Si gate insulator with permittivity of 20 results in t_{eq}=31 nm of equivalent SiO_2, where equivalent thickness (t_{eq}) is calculated from[4]:

$$t_{eq} = \frac{\varepsilon_{T-SiO_2}}{\varepsilon_{O-Ta_2Si}} t_{O-Ta_2Si} \quad (6.9)$$

as clearly illustrated on Fig. 6.31, at 15 V of gate bias, the on-resistance of the device is reduced from 86 mΩcm^2 (t_{ox}=40 nm T-SiO_2) to 29 mΩcm^2 (t_{eq}=31 nm O-Ta_2Si) at 0.2 V drain bias.
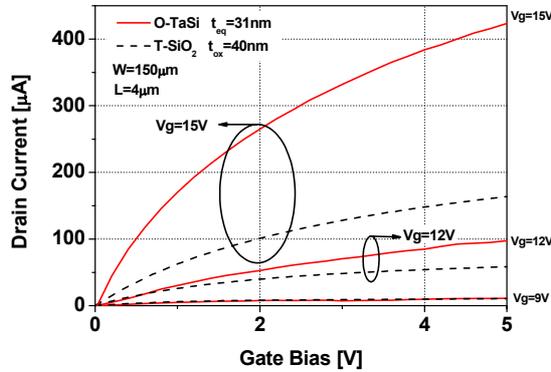
Fig. 6.31. Comparison of drain current characteristics of a p-implanted oxidized Ta_2Si (O-Ta_2Si) MOSFET, and a standard T-SiO_2 MOSFET.
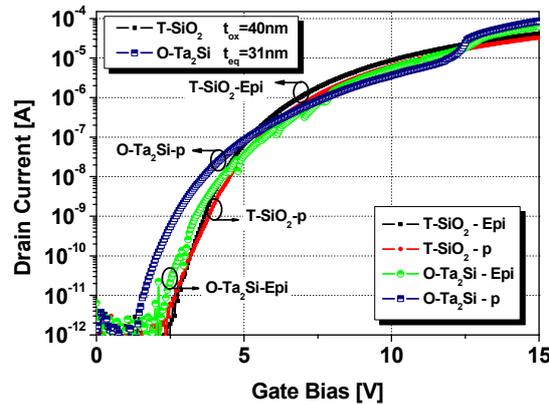
Fig. 6.32. Comparison of transfer characteristics of oxidized Ta_2Si and T-SiO_2 MOSFET on an implanted and no implanted p region.

From the measured drain current versus gate voltage for O-Ta_2Si and T-SiO_2 MOSFETs, fabricated on implanted region or directly on the epitaxy, the subthreshold slope, S, could be determined (Fig. 6.32). Subthreshold technique is also used in threshold voltage extraction. From the $\log I_{DS}$ versus V_{GS} plot the voltage threshold is the point depart from linearity. The values of effective mobility, specific on-resistance

and threshold voltage for the fabricated O-Ta$_2$Si MOSFETs are listed in Table VI.2, and compared with a standard T-SiO$_2$ devices with gate O$_2$ dry oxidized (1160 ºC 3 h).

The field effect electron channel mobility of MOSFET has been also extracted from the experimental transconductance g_m, as it is shown in Fig. 6.33. As stated before, the peak mobility is significantly increased for O-Ta$_2$Si MOSFETs when compared with standard dry T-SiO$_2$ 4H-SiC MOSFETs. The field effect mobility increase for O-Ta$_2$Si devices, takes place for relatively high electric fields, and we would tempted to assume that electrical conduction improvements result primarily from current injection trough the interfacial SiO$_2$-like interfacial layer. Analogously, on-resistance has been clearly reduced using O-Ta$_2$Si gate based devices. Slightly higher R_{on} has been routinely obtained on p-implanted T-SiO$_2$ MOSFETs. This characteristic has not been reproduced for the O-Ta$_2$Si MOSFETS and in general, p-implanted devices present higher reliability. The threshold voltage is maintained in the range 1.5-3 V for the most of the devices analyzed, for both O-Ta$_2$Si and T-SiO$_2$ MOSFET devices.

Sample	*Vth* [V]	R_{on} @ **14V** [mΩ.cm^2]	μ_{FE} (peak) [cm^2/Vs]
P-implanted (O-Ta$_2$Si)	1.9	29.0	45
Epitaxial (O-Ta$_2$Si)	2.3	42.8	19
P-implanted (T-SiO$_2$)	2.5	86.1	5
Epitaxial (T-SiO$_2$)	2.4	84.2	6

Table VI.2. Summary of extracted parameters from forward and transconductance curves.
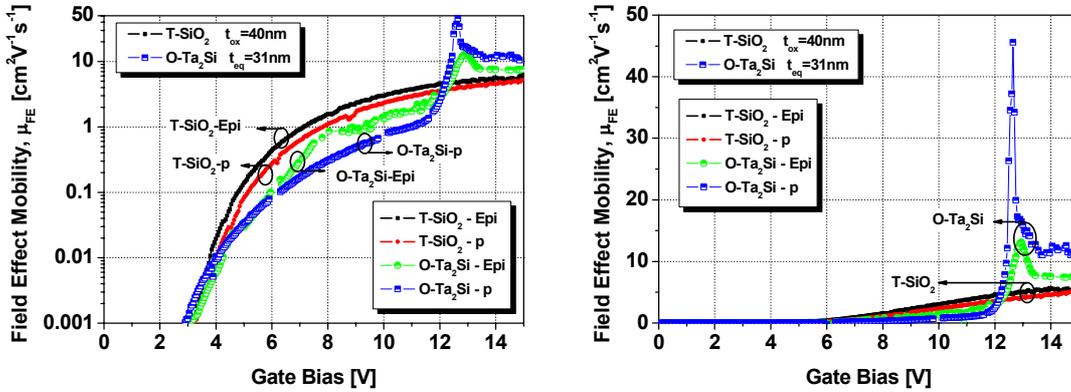
Fig. 6.33. Comparison of field effect electron channel mobility of oxidized Ta$_2$Si and T-SiO$_2$ MOSFET on and implanted and no implanted p region. The μ_{FE} logarithmic scale reveals similar values of the subthreshold slope for all cases.

As expected, the leakage current is higher for O-Ta$_2$Si MOSFETs than for T-SiO$_2$ MOSFETs due to the presence of Poole-Frenkel conduction mechanism in the gate of the high-*k* dielectric. The increase of the peak mobility seems to be related with this leakage current, since the subthreshold slope (an indication of interface trap that degrade the channel conduction) is almost the same for the two gate process fabrication. This last result agrees with the assumption of a SiO$_x$ interfacial layer, during the Ta$_2$Si oxidation, yielding similar interface properties when compared with thermal oxidation.

The anomalous high mobility peak obtained in these O-Ta$_2$Si devices will be analyzed in detail in the last chapter of this thesis.
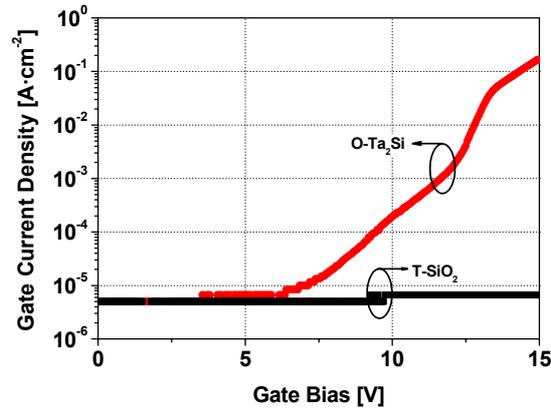
Fig. 6.34. Gate current density for oxidized Ta$_2$Si and T-SiO$_2$ 4H-SiC MOSFET.

6.2. Stacked structures based on SiO$_2$/O-Ta$_2$Si

6.2.1. O-Ta$_2$Si on standard thermal SiO$_2$ (T-SiO$_2$)

The physical and electrical characteristics of Ta$_2$Si layers oxidized directly on SiC an on Si have been reported in the previous section. MOSFETs devices have also been fabricated using the dielectric layer produced by the oxidation of Ta$_2$Si layer, demonstrating one of the first well behaved SiC MOSFET with alternative high-k in the gate definition, that can be found in the literature[53]. In order to improve the electrical characteristics of the Ta$_2$Si oxidized layers, especially the leakage current, an interesting solution could be the construction of staked dielectrics with a SiO$_2$ layer in the semiconductor-insulator interface. In this sense, MIS staked structures have been fabricated composed of Ta$_2$Si oxidized layers in dry O$_2$ a on standard thermal oxidized 4H-SiC (T-SiO$_2$) n-type substrate (see *Chapter IV*) yielding a SiO$_2$ layer of approximately 40 nm. Fig. 6.35(a) shows the high frequency C-V measurements of T-SiO$_2$ and a typical T-SiO$_2$/O-Ta$_2$Si capacitor. O-Ta$_2$Si layers have been implemented with 50 nm of deposited Ta$_2$Si and oxidized at 950 $^{\circ}$C during 90 min in dry O$_2$. The dielectric constant experimentally inferred for T-SiO$_2$/O-Ta$_2$Si capacitors has been determined to be ε_r=10.8. Fig. 6.35(b) shows the computed mapping of stacked dielectric constant, versus the Ta$_2$Si deposited thickness, considering a SiO$_2$ thickness of 40 nm with a dielectric constant of 3.9. As we have experimentally demonstrated in the previous section, O-Ta$_2$Si layers on an inert substrate, such as SiC at temperatures below 1000 $^{\circ}$C, present high-k dielectric constant of ~20. Therefore, as it can be argued that a SiO$_2$ layer is even less reactive substrate than the SiC surface and the influence of the substrate can be neglected, an effective dielectric constant of 20 has been used for O-Ta$_2$Si layer on T-SiO$_2$. It must be stressed that the relationship used between the deposited (Ta$_2$Si) and oxidized (O-Ta$_2$Si) thickness layer is that the O-Ta$_2$Si layer is three times thicker than the Ta$_2$Si deposited layer, as it has also been well established in the previous section. The stacked dielectric constant has been determined considering the two capacitance layers in series and is computed with the expression (6.7):

$$\varepsilon_r = (t_{O-Ta_2O_5} + t_{SiO_2}) \frac{\varepsilon_{O-Ta_2O_5} \varepsilon_{SiO_2}}{\varepsilon_{O-Ta_2O_5} t_{SiO_2} + \varepsilon_{SiO_2} t_{O-Ta_2O_5}} \qquad (6.7)$$

A very good agreement between the computed ε_r values and the experimental ε_r values has been extracted as it can be inferred from Fig. 6.35(b).

(a)   (b)
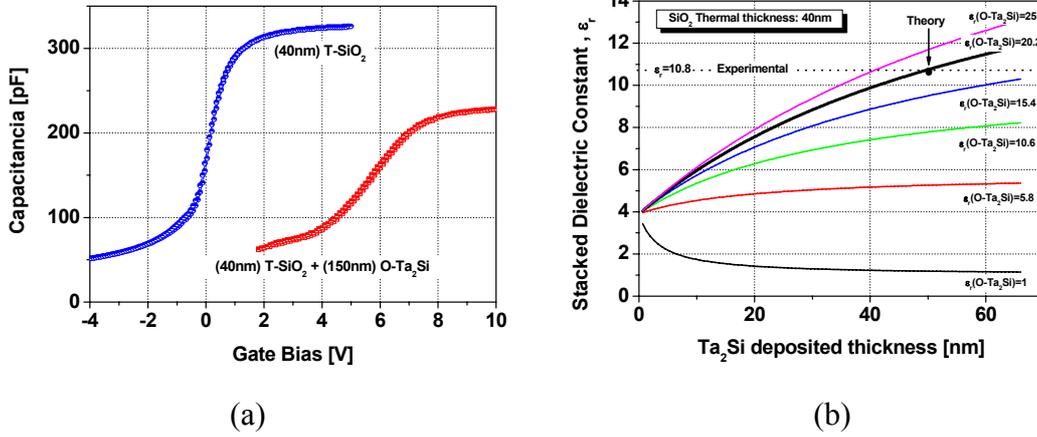
Fig. 6.35. (a) C-V high frequency characteristics of MIS structures of standard thermal oxidized 4H-SiC(T-SiO$_2$) and 50 nm of Ta$_2$Si oxidized at 950 ^{o}C (90 min). (b) Effective dielectric constant extracted from MIS capacitors biased in strong accumulation compared with the stacked computed values.
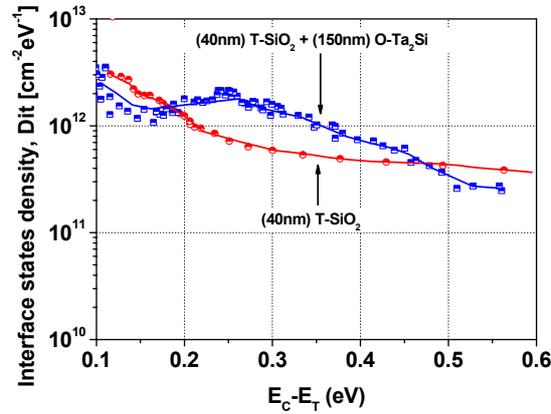
Fig. 6.36. Interface state density spectra of oxidized Ta$_2$Si films on the standard oxidized 4H-SiC.

Nevertheless, the interfacial characteristics of T-SiO$_2$/O-Ta$_2$Si capacitors are expected to be similar to those of T-SiO$_2$ capacitors. T-SiO$_2$ layers on SiC (especially in the 4H-SiC polytype) presents high density of interface states that is traduced in a reduced field effect mobility in 4H-SiC MOSFET devices (~5 cm^2/Vs). The interface states density spectra within the band gap close the conduction band is presented in Fig. 6.36 for T-SiO$_2$ and T-SiO$_2$/O-Ta$_2$Si capacitors. As it can be derived from the figure, similar D$_{it}$ profile have been obtained for both samples with ~1×10^{12} cm^{-2}eV^{-1} at $E_C - E_T$ =0.2 eV.

Poole-Frenkel phenomenon has been invoked as the conduction mechanism of pure O-Ta$_2$Si layer on SiC and Si substrates. This trap assisted conduction mechanism

provokes high leakage current densities at relative low dielectric fields (~1 MV/cm). However, the dielectric constant is also at least four times higher that for the conventional SiO_2. I-V characteristics have been measured in the stacked capacitors (T-SiO_2/O-Ta_2Si) with a breakdown voltage around ~45 V as it can be derived from Fig. 6.37.
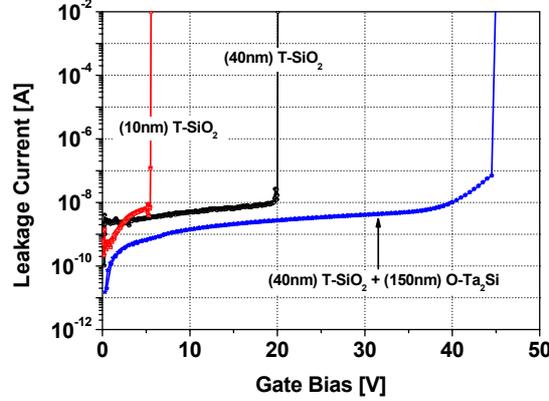
Fig. 6.37. Leakage current of stacked T-SiO_2/O-Ta_2Si on n-type 4H-SiC capacitors.

A factor of merit is introduced[30] in order to compare the leakage characteristics of the different oxidation processes. This factor of merit is determined from the definition of the capacitance and the dielectric breakdown field. The breakdown point criteria was established considering a current density of 10^{-4} A·cm^{-2} across the MIS terminals.

$$\frac{C \cdot V_{bd}}{\varepsilon_0} = \varepsilon_r E_{bd} \qquad (6.8)$$

where C is the MIS capacitance per unit area extracted from C-V measurements biased in the strong accumulation range, ε_r is the dielectric constant, ε_0 denotes the permittivity of free space, V_{bd} is the breakdown voltage and E_{bd} is the dielectric breakdown field. Assuming that the (commonly established) dielectric breakdown field is 10 MV/cm[41] for the thermally oxidized SiO_2 layers and its dielectric constant is 3.9, for a T-SiO_2 capacitor a typical value close to $\varepsilon_r E_{bd}$ ~39 MV/cm would be obtained. Hence, if this value is taken as reference we can define the thermal SiO_2 breakdown ratio (T-SiO_2 ratio) as a measure of the dielectric strength of the layers when compared with thermally grown SiO_2, taking into account the high-*k* benefits. I-V measurements with the mercury probe performed on (40 nm) T-SiO_2 structures have resulted in a breakdown voltage of only 20 V as it can be inferred from Fig. 6.37. This produces a experimental T-SiO_2 ratio of 50% when compared with the theoretical measurements. For pure O-Ta_2Si capacitors oxidized at 950 ºC during 90 min ~49% of theoretical T-SiO_2 has been extracted. The stacked insulator composed of 40nm SiO_2 thermal oxide and 50 nm deposited Ta_2Si oxidized at 950 ºC (90 min) slightly improves this merit ratio up to ~65% of the theoretical T-SiO_2. Therefore, the stacked MIS structure presents enhanced insulator properties when compared with pure O-Ta_2Si or even with experimental T-SiO_2.

The surface roughness of the oxidized Ta_2Si layer has been evaluated by atomic force microscopy working in the non contact tapping mode. The average height of the surface (RMS) has been extracted for samples dry oxidized during 1 h at 950 ºC in both

T-SiO$_2$ and 4H-SiC samples. The investigate area was 5×5 μm^2 as shown in figure 6.38. The RMS on 4H-SiC substrates (10 nm) is higher than on T-SiO$_2$ substrates (3 nm). The lower RMS observed on T-SiO$_2$ substrates would be attributed to the more regular surface previous oxidation.

(a)   **(b)**
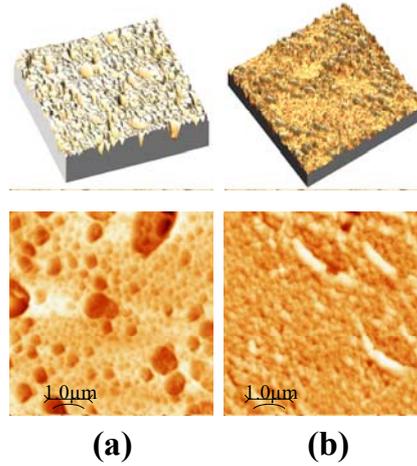
Fig. 6.38. AFM images of Ta$_2$Si films (50 nm) deposited and oxidized (950 ^{o}C 90 min) on (a) 4H-SiC, (b) standard thermal oxidation on 4H-SiC (T-SiO$_2$).

Hence the initial configuration would affect the subsequent grown of the insulator layer. No implantation processes have been performed on SiC samples, prior to the SiC surface oxidation and subsequent Ta$_2$Si deposition. SiC surface roughness presents typical values ranging 0.8-1 nm. If implanted SiC samples are considered, a typical RMS of 4 nm would be obtained for Al or N implanted and annealed samples.

6.2.2. O-Ta$_2$Si on low temperature thermally grown SiO$_2$ (LT-SiO$_2$)

We have demonstrated that the 4H-SiC MOSFET field effect mobility of devices with SiO$_x$ deposited using TEOS as source material in the gate fabrication process, has been substantially improved with an interfacial low temperature oxidation (prior to the SiO$_x$ deposition)[54]. Analogously, the nitridation (NO or N$_2$O) of the interface was demonstrated to be an effective process to improve SiC MOS interface properties. In this case, a thin oxide was preferable to reduce the interface state density because a high amount of nitrogen was able to reach the interface by radical nitridation[55]. Seems clear that a low temperature oxidation, presumably reduces the disorder and dangling bonds in the interface and makes it more accessible to posterior annealing treatments. Therefore, this procedure has been tested with an 4H-SiC interfacial low temperature[a] thermal oxidation (LT-SiO$_2$) performed at 1050 ºC during 1h prior to the deposition and subsequent oxidation of Ta$_2$Si.

4H-SiC stacked LT-SiO$_2$/O-Ta$_2$Si n-channel MOSFETs on the 8° off Si (0001) face have been implemented. The n-channel inversion channel MOSFETS structures have also been fabricated on a p-implanted region for CMOS and power applications. The p-type wells are created by a Boron multiple energy implant (energies ranging 25-320 keV) and posterior RTA (Rapid Thermal Annealing) at 1650 ^{o}C. In order to define the gate insulator, a low temperature thermal oxidation (1050 ºC 1 h) has been carried

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[a] LT-SiO$_2$:Low temperature when compared with standard oxidation (1150 ºC 3 h)

out in the gate region, that composes the closest layer to SiC (the interfacial LT-SiO$_2$ layer). Subsequently, the upper gate insulator has been grown by dry oxidation of 24 nm deposited Ta$_2$Si during 20 min at 950 $^{\circ}$C. The resulting dielectric thickness has been determined to be 85 nm. Evaporated Aluminum and Nickel have been used to form the MOS gate and the source/drain contacts.

(a)   (b)
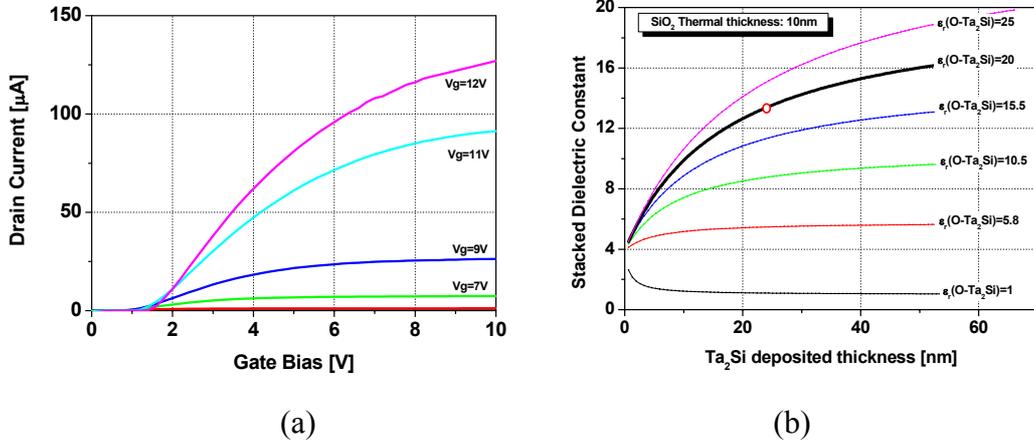
Fig. 6.39. (a) Forward I-V characteristics of LT-SiO$_2$/O-Ta$_2$Si MOSFET on epitaxial layer with L =4 μm, W =150 μm. (b) Computed effective dielectric constant for stacked structure with low temperature thermal oxidation and O-Ta$_2$Si.

The stacked 4H-SiC MOSFET forward drain current is presented in Fig. 6.39(a). Rectifying contact effect can be observed since no posterior contact definition annealing has been performed. A dielectric constant of 13.4 has been computed for the gate insulator using the equation (6.7). The mapping of the dielectric constant versus the Ta$_2$Si deposited thickness is presented in Fig. 6.39(b). The higher the Ta$_2$Si deposited thickness the higher the stacked dielectric constant will be, considering a constant value for the interfacial LT-SiO$_2$ thickness (10 nm).
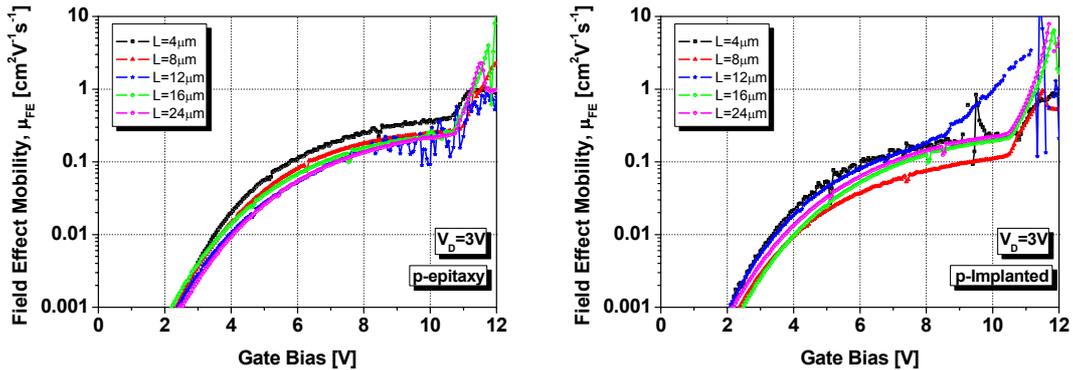
Fig. 6.40. Field effect electron channel mobility in transistors with O-Ta$_2$Si and low temperature T-SiO$_2$ as gate insulator MOSFET on and implanted and no implanted p region.

The MOSFET field effect electron channel mobility has been extracted from the experimentally derived transconductance, as it is shown in Fig. 6.40, for devices implemented on a p-type epitaxy and on p-implanted region. The extracted μ_{FE} is significantly lower when compared with a conventional thermal T-SiO$_2$ 4H-SiC

MOSFET, maintaining its value lower than 1 cm^2/Vs, up to the anomalous mobility improvement for the higher gate bias. This anomalous mobility improvement seems to be of the same origin that those obtained for pure O-Ta$_2$Si MOSFET and is related with the gate leakage current injection of carrier, as it will be analyzed in the last chapter of this thesis.
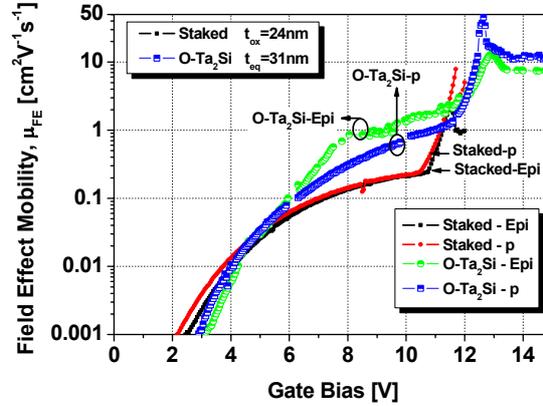
Fig. 6.41. Comparison of field effect electron channel mobility of O-Ta$_2$Si and low temperature T-SiO$_2$/O-Ta$_2$Si as gate insulator MOSFET on and implanted and no implanted p region.

Indeed, the significantly low mobility, even when compared with pure O-Ta$_2$Si devices (see Fig. 6.41) , remains as an open issue. The interfacial characteristics of this stacked structure would be similar to the T-SiO$_2$. Physical measurements are currently under investigation in order to explain the origin of this noticeable mobility reduction. From Fig. 6.41 the anomalous mobility enhancement in strong inversion becomes obvious for both, the O-Ta$_2$Si and the LT-SiO$_2$/O-Ta$_2$Si devices.

6.3. Ta$_2$Si oxidized in N$_2$O

Reduction of interface-trap density on MOS structures, increased channel mobility and oxide reliability in 4H-SiC MOSFET devices, have been obtained considering thermally grown oxides[56] or annealed[57] in NO and N$_2$O ambients. Nitrous oxide (N$_2$O) is by far preferred processing environment due to its availability and the high toxicity of pure NO. The enhancements produced by the nitridation treatments seems to be directly linked with the nitrogen incorporation in the interface removing carbon interface concentration or carbon clusters[58] or passivating intrinsic defects extending from the interface into the oxide layer[59]. In the other hand, in the previous sections it has been demonstrated the potential of oxidized Ta$_2$Si layer as high-*k* dielectric for SiC MOSFET devices. Nevertheless, as it can be derived from the experimental results, the interface trap density in these last devices must be further improved. Hence, the combination of N$_2$O treatments at the interface along with the oxidation of deposited Ta$_2$Si, that requires lower temperatures in the thermal oxidation, must be considered an attractive procedure. In this sense, we propose the N$_2$O oxidation of deposited Ta$_2$Si layer in order to combine the nitrogen incorporation at the interface as well as the high-*k* advantages of the O-Ta$_2$Si layers. Additionally, N$_2$O post

deposition thermal treatments on pure Ta_2O_5 capacitors have shown a reduction of the current leakage with an increment of the insulator reliability[36,37].

On Si substrate

Si substrates have been used in a preliminary study. On p-type Si substrates with a doping level of $N_A=1\times10^{16}$ cm^{-3}, Ta_2Si (24-30 nm) has been deposited by sputtering and oxidized in (diluted) N_2O at 950 ºC during 5 min (N_2O-Ta_2Si). Very short times have been used evidencing the rapid oxidation of the Ta_2Si layer, at least in a N_2O ambient. X-ray diffraction analysis have not shown crystalline phases in the N_2O-Ta_2Si layers as it can be inferred from Fig. 6.42(a), where the N_2O-Ta_2Si sample is compared with an O-Ta_2Si sample oxidized at the same temperature (950 ºC) during 60 min.
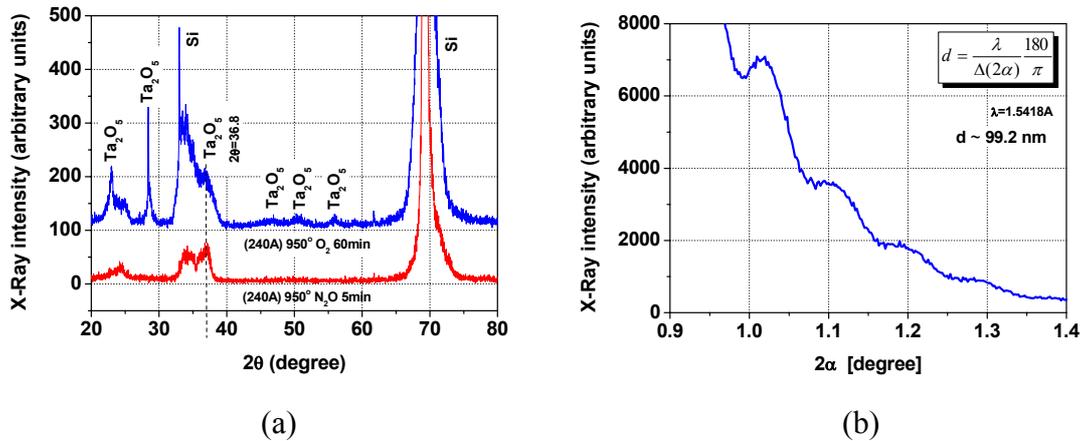
Fig. 6.42. (a) XRD theta-2theta scans of Ta_2Si films deposited on p-type Silicon and oxidized at 950 ºC in O_2 (1h) and N_2O (5 min). (b) X-Ray glancing incidence for the N_2O-Ta_2Si layer indicating an estimated thickness of 99 nm.

The only peak that seems to be susceptible to be detectable from δ-Ta_2O_5 layers is from the (101) reflection[60] with 2θ=36.8º, but there are not definitive arguments to assure this. Hence, the N_2O-Ta_2Si layer oxidized at 950 ºC in N_2O during 5 min seems to be amorphous to the crystallinity level detectable. More experiments must be performed in order to determine if the amorphous structure is due to the oxidizing ambient, N_2O instead of O_2, or is due to the significantly shorter oxidation times. X-ray glancing incidence measurements have been used in order to determine the oxidized layer thickness as it is shown in Fig. 6.42(b).

From capacitance measurements the dielectric constant value can be extracted. A dielectric constant value of ε_r=8.4 has been determined for the N_2O-Ta_2Si (950 ºC 5 min N_2O) capacitor, a value slightly lower than the determined for O-Ta_2Si (950 ºC 1 h O_2) capacitors (ε_r=8.6). High frequency C-V measurement have also shown the drastic reduction of the hysteresis behavior routinely obtained when O-Ta_2Si oxidation is performed on Si at higher oxidation times as it can be inferred from Fig 6.43. Higher flat-band shift (to negative gate voltages) is obtained for the N_2O-Ta_2Si samples (and indication of higher oxide charge).
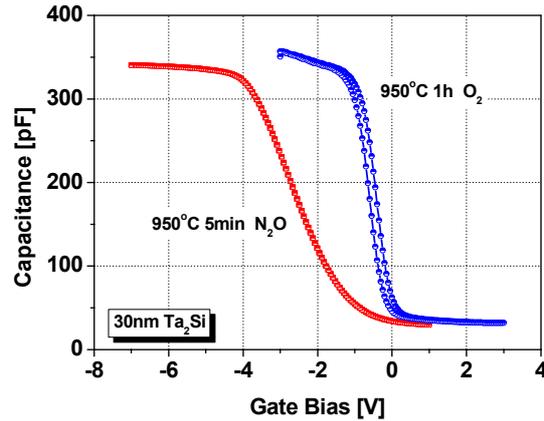
Fig. 6.43. High-frequency (100 kHz) capacitance-voltage characteristics for the MIS capacitors composed of 30 nm Ta_2Si oxidized on p-type Silicon at 950 ^{o}C in O_2 (1 h) and N_2O (5 min).
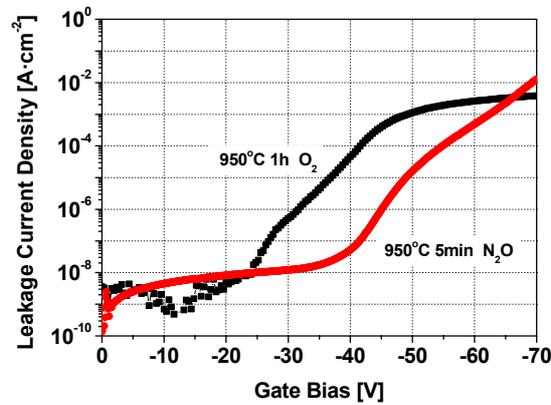
Fig. 6.44. Leakage current of p-type Si capacitors with 30 nm Ta_2Si oxidized on p-type Silicon at 950^oC in O_2 (1 h) and N_2O (5 min).

The leakage current density is diminished for the N_2O-Ta_2Si capacitors when compared with the O-Ta_2Si MIS structures, as it can be derived from Fig. 6.44. The dielectric strength is also higher for N_2O-Ta_2Si capacitors. The breakdown criteria, that determines the critical electric field, is established when the leakage current density reaches 10^{-4} A/cm^2. The dielectric breakdown field for the N_2O-Ta_2Si p-type Si capacitors is E_{bd}=5.1 MV/cm that is higher that the obtained for O-Ta_2Si (E_{bd}=4.5 MV/cm). Compared with the factor of merit (Eq. (6.8)) from thermal SiO_2 theoretical breakdown ratio (T- SiO_2 ratio), superior insulator properties are obtained compared to those obtained with the p-type capacitor thermally oxidized on Si. T- SiO_2 ratio of ~109.8% and ~98.2% have been achieved for N_2O-Ta_2Si (950 ºC 5 min N_2O) and O-Ta_2Si (950 ºC 1 h O_2) p-type Si capacitors, respectively.

On 4H-SiC substrate

Ta_2Si films of 40 nm thickness have been deposited by direct sputtering on n-type 4H-SiC substrates (N_D=1×10^{16} cm^{-3} purchased from Sterling inc.) after a cleaning procedure based on three H_2O_2 containing etch solutions (H_2SO_4:H_2O_2, HCl:H_2O_2, NH_3:H_2O_2). The substrates have not been heated during the Ta_2Si deposition. Following

the deposition the samples have been oxidized in a N_2O ambient diluted in Ar [50/50] during 5 min at 1100 ºC.

X-ray diffraction analysis has been carried out on Ta_2Si oxidized in N_2O layers. Unlike the N_2O oxidized layers on Si substrates, Ta_2O_5 crystalline peaks are clearly evidenced in a theta-2theta scans on n-type 4H-SiC substrates, after the very short time N_2O oxidation. Significant differences in the XRD spectra between samples, where the Ta_2Si silicide (40 nm) was oxidized at temperatures ranging 850 – 1050 ºC and the N_2O oxidized layers at 1100 ºC (Fig. 6.45(a)), have not been detected. Glancing incidence x-ray reflectivity measurements were used to determine the oxidized layer thickness, as illustrated in Fig. 6.45(b). As it can be inferred from the figure, the reflectivity peaks are very well defined. Presumably, this is due to the short oxidation time that defines an abrupt interface between the insulator and the SiC surface. After the N_2O oxidation of 40 nm of Ta_2Si, the insulator thickness obtained is 130 nm. Therefore, the relationship between the oxidized and the deposited thickness, as it occurs when Ta_2Si is oxidized in O_2 ambient, is around 3 times thicker.

(a)   (b)
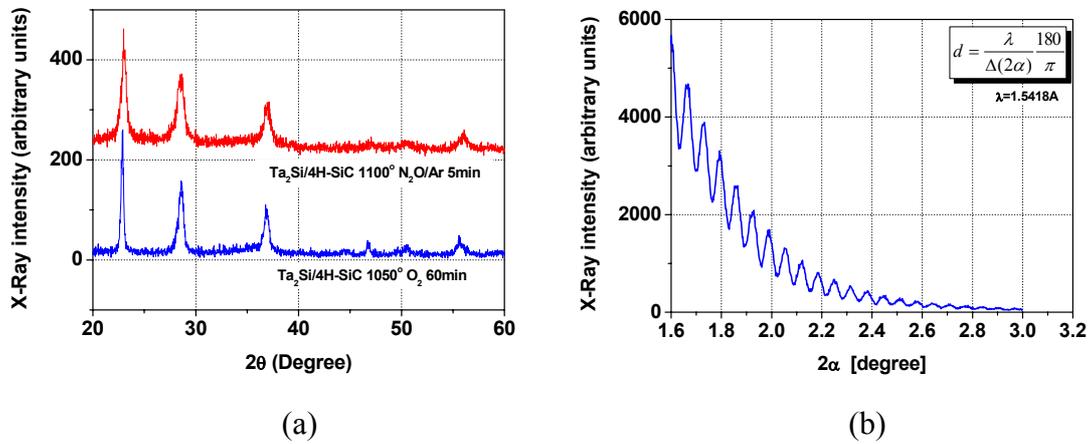
Fig. 6.45. (a) XRD theta-2theta scan of Ta_2Si films deposited on 4H-SiC and oxidized at 1050 ºC in O_2 (1h) and at 1150 ºC N_2O (5 min). (b) X-Ray glancing incidence for the N_2O-Ta_2Si/SiC layer indicating an estimated thickness of 130 nm.

Fig 6.46(a) shows the capacitance-voltage measurement for capacitors made up with 40 nm N_2O-Ta_2Si oxidized at 1100 ºC. Oxidation times of 5 min, at 1100 ºC, in N_2O seems to be enough to completely oxidize this layer, since depletion and deep depletion regions are observed. The capacitance value measured in strong accumulation, along with the thickness determined from XRD glancing incidence, allows determining the effective dielectric constant value. A dielectric constant value of ε_r ~20 (19.5) has been determined for the N_2O-Ta_2Si capacitor. This value is basically the same obtained for O-Ta_2Si layers (oxidized at temperatures higher than 850 ºC). High frequency C-V measurements have also been carried out in our samples in order to determine its insulator charge and the interfacial properties. C-V measurement have shown a marked hysteresis behavior routinely observed when N_2O-Ta_2Si oxidation is performed on SiC, as it can be inferred from Fig 6.46(a). Higher flat-band shift (to positive gate voltages) is obtained for the N_2O-Ta_2Si samples when compared with the O-Ta_2Si samples, oxidized at larger times indicating higher content of insulator charge.

The interface states density spectra within the band gap close the conduction band is presented in Fig. 6.46(b), for O-Ta_2Si and N_2O-$TaSi_2$ capacitors on n-type 4H-

SiC substrates. As it can be derived from the figure, a significantly higher D_{it} profile has been obtained for the N_2O-$TaSi_2$ sample with $\sim 6 \times 10^{12}$ cm^{-2}eV^{-1} at $E_C - E_T = 0.2$ eV.

(a)   (b)
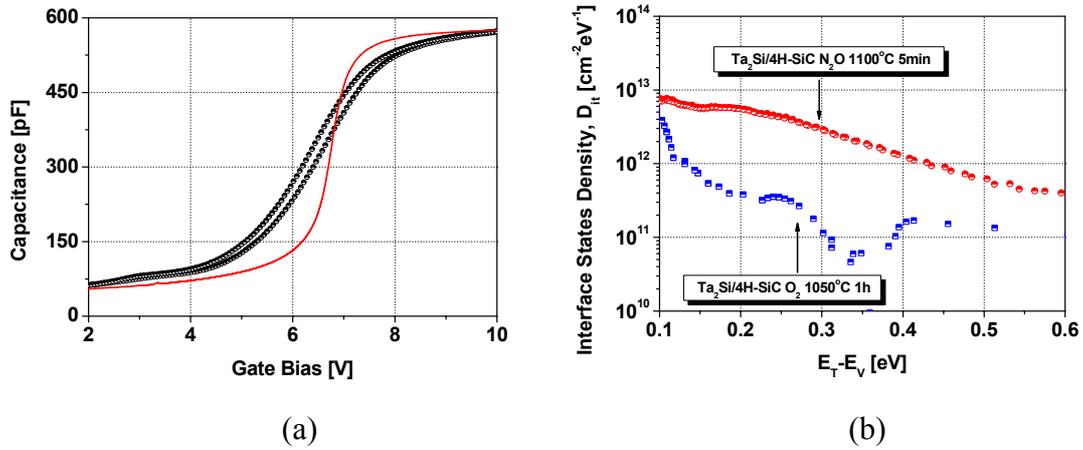
Fig. 6.46. (a) High frequency experimental and theoretical traces of the N_2O-$TaSi_2$ films (1100 ºC 5 min) on 4H-SiC. (b) Interface state density spectra of oxidized Ta_2Si/4H-SiC under O_2 (1100 ºC 1 h) and N_2O (1100 ºC 5 min) oxidation conditions.

I-V measurements have been performed on N_2O-Ta_2Si capacitors to determine the leakage current characteristics (Fig. 6.47). For relative low gate voltages (lower than 15 V), the leakage current depends on the previous stress conditions. Hence, higher leakage current values are obtained when subsequent measurements are performed on the same N_2O-Ta_2Si capacitors. However, once stressed the I-V characteristics follow a repetitive trace as illustrated in Fig. 6.47(b).

(a)   (b)
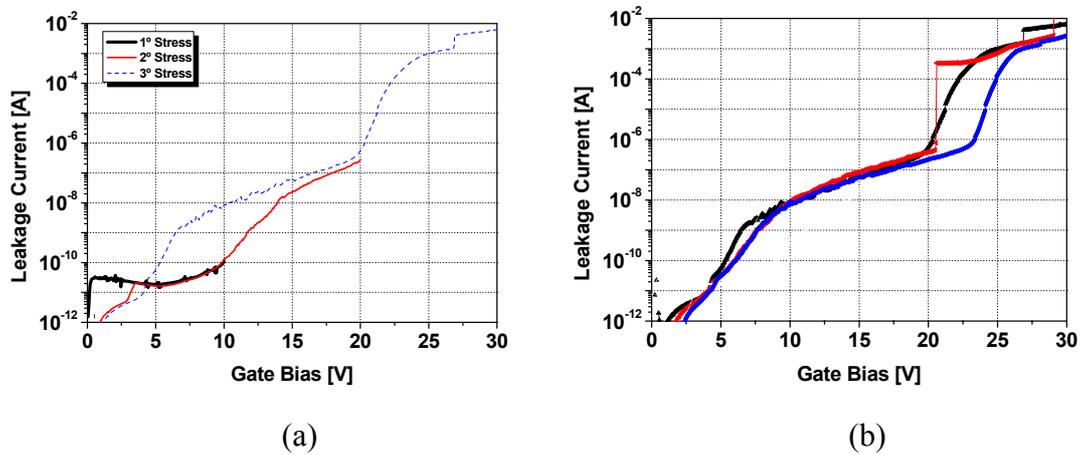
Fig. 6.47. Leakage current vs gate bias field for N_2O-Ta_2Si/SiC (a) with hysteresis behavior, (b) and with repetitive I-V characteristic.

The formation of a SiO_x rich interfacial layer between the insulator and the semiconductor strongly influences the current-voltage characteristics of oxidized Ta_2Si layers. However, the oxidation at a relative short times and the sharp glancing incidence peaks suggest a very thin (or/and few dense) interfacial layer. On p-type Si substrates, a reduction of the leakage current in the samples oxidized in N_2O ambient has been extracted. However as inferred from Fig. 6.48, in n-type SiC substrates, the I-V behavior is quite different. Although the trap assisted conduction Poole-Frenkel

mechanism can be observed in the N_2O-Ta_2Si layers, the absence (or the lack of influence) of the interfacial layer allows the trap assisted mechanism even at the lower electric fields. A similar situation is detected for O-Ta_2Si layers oxidized at 750 ºC (Fig. 6.48). However, the leakage current density is orders of magnitude lower in this last case than for N_2O-Ta_2Si capacitors. In both cases, the formation of a dense interfacial layer must be ruled out. The difference seems to lie in the higher degree of crystallinity of the N_2O-Ta_2Si sample. The higher the amount of crystalline phase, the higher the dielectric constant but at the same time, increasing the current leakage (more inter-grain leaking conduction through grain boundaries).

(a)   (b)
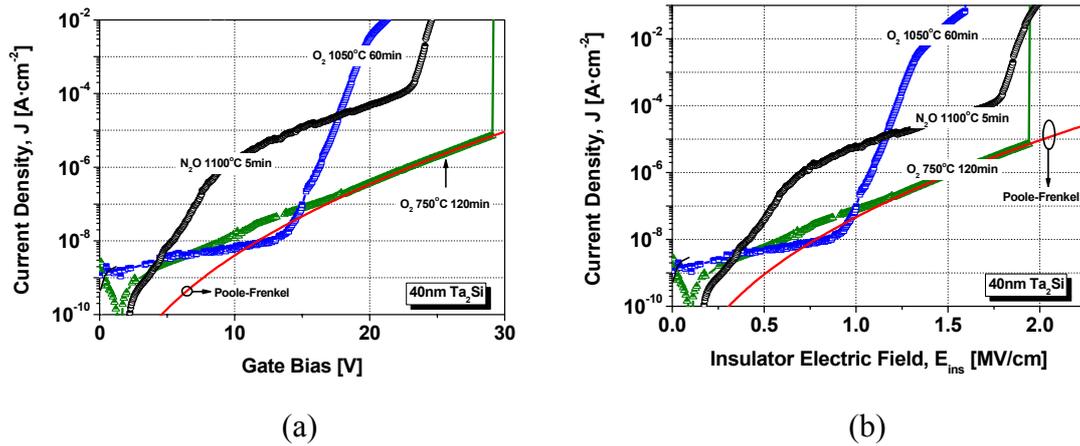
Fig. 6.48. Leakage current vs (a) gate bias and (b) insulator electric field for, O-Ta_2Si/SiC (750 ºC 120 min /1050 ºC 60 min) and N_2O-Ta_2Si/SiC (1100 ºC 5 min).

6.4. $TaSi_2$ thermal oxidation, the oxidation of the common Tantalum silicide to form dielectric layers on SiC

In this section, the most common used in microelectronic processing of Tantalum silicides ($TaSi_2$ − Tantalum disilicide), has been dry thermally oxidized on 4H-SiC substrates. As stated before, Tantalum silicide (Ta_2Si) presents several advantages when compared with $TaSi_2$ when oxidized, to form an insulator. It has been reported[6,15] that when $TaSi_2$ is oxidized on Silicon, other undesirable oxidation species (as well as Ta_2O_5 and SiO_2) are achieved. This additional compounds should provoke a degradation of the insulator properties and reproducibility problems of the oxidized insulator layer. Furthermore, as the Silicon/Tantalum ratio of $TaSi_2$ is higher than in Ta_2Si silicide, the dielectric constant must be lower for the oxidized $TaSi_2$ layers. In contrast to this, the major content of SiO_2 from the oxidation of $TaSi_2$ may favor an increase of the dielectric strength of the oxidized layer.

In this experiment, $TaSi_2$ films of 40 nm thickness have been deposited by direct sputtering on n-type 4H-SiC substrates after a cleaning procedure based on three H_2O_2 containing etch solutions (H_2SO_4:H_2O_2, HCl:H_2O_2, NH_3:H_2O_2). The substrates have not been heated during the Ta_2Si deposition. Following the deposition, the samples have been oxidized in dry environment at atmospheric pressure during 60 min at 1050 ºC. After this first process we found that the samples were not completely oxidized. Thus, thermal oxidation during 60 min more at the same temperature has been performed.

When X-ray diffraction analysis on Ta_2Si/SiC samples dry oxidized are carried out (section 6.1), Ta_2O_5 peaks are clearly evidenced on n-type 4H-SiC substrates. Significant differences in the XRD spectra have not been detected, when the Ta_2Si silicide (40 nm) was oxidized at temperatures ranging 850 – 1050 ºC. When $TaSi_2$ silicide was deposited on 4H-SiC and oxidized during 60 min, no crystalline peaks were observed. 120 min is enough to completely oxidize the silicide layer (40 nm of $TaSi_2$) on 4H-SiC, and Ta_2O_5 peaks also arise in the XRD spectra (Fig. 6.49).
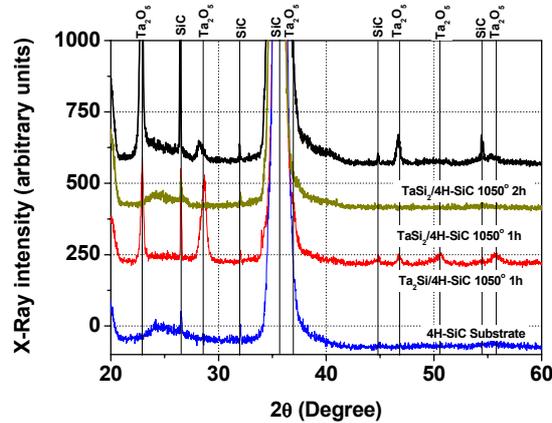
Fig. 6.49. XRD theta-2theta scan of Ta_2Si (1 h) and $TaSi_2$ (1 h, 2 h) films deposited and oxidized on n-type 4H-SiC at 1050 ºC.

However, some structural differences are detected when the XRD spectra of the oxidized Ta_2Si (O-Ta_2Si) or $TaSi_2$ (O-$TaSi_2$) at 1050 ºC during 1 h or 2 h, respectively, are compared. Crystalline tantalum pentoxide presents principally two phases: an orthorhombic phase and a hexagonal phase. The orthorhombic structure can be divided into two forms, with a reversible transition occurring at about 1360 ºC: a high-temperature form and a low-temperature form which is called β-Ta_2O_5 [12]. The lattice parameters for orthorhombic Ta_2O_5 are a=6.198 Å, b=40.290 Å and c=3.88 Å. The orthogonal unit cell of this compound contains 11 formula units. The structure was solved in projection from the Patterson functions. The ideal structure for β-Ta_2O_5 can be generated from a chain of 8 edge-sharing pentagons. The plane group of the (001) projection of this ideal structure is *pgm*, and the ideal unit cell contains 22 Ta atoms and 58 O atoms. The real structure contains on the average three distortion planes per unit cell, so that one has a reduction in the coordination number of some metal atoms: the real unit cell of β-Ta_2O_5 contains 22 Ta atoms and 55 O atoms.

For the hexagonal phase, the lattice parameters are a=3.62 Å and c=3.87 Å. Fukumoto and Miwa[61] used first-principles calculations to predict the crystal structure or hexagonal δ-Ta_2O_5 since it is still unknown. Three crystal structures were chosen for evaluation, after referring to the XRD data: *P6/mmm*, *P6m2* and *P63/mmc*. Their results show that the predicted structure has the space group of P6/mm with two formula units in the unit cell (a=7.191 Å and c=3.831 Å; a is assumed to be twice as large as the measured value due to the extinction rule), and that the coordination number of O atoms to Ta atoms is 8 for one Ta atom and 6 for the other three atoms. Fig 6.50(a) shows the expected position[60] of peaks in a theta-2thetha scan in a XRD spectra and the relative intensity for both, the crystalline δ-Ta_2O_5 and the crystalline β-Ta_2O_5 phases. The position of these peaks (to the most important we have arbitrary referred as $β_x$ or $δ_x$ in the table) are listed in Table VI.3. As it can be inferred from Fig. 6.50(a), it is difficult

to distinguish between the two known phases of Ta_2O_5 since the strongest peaks are very close.

(a)

(b)
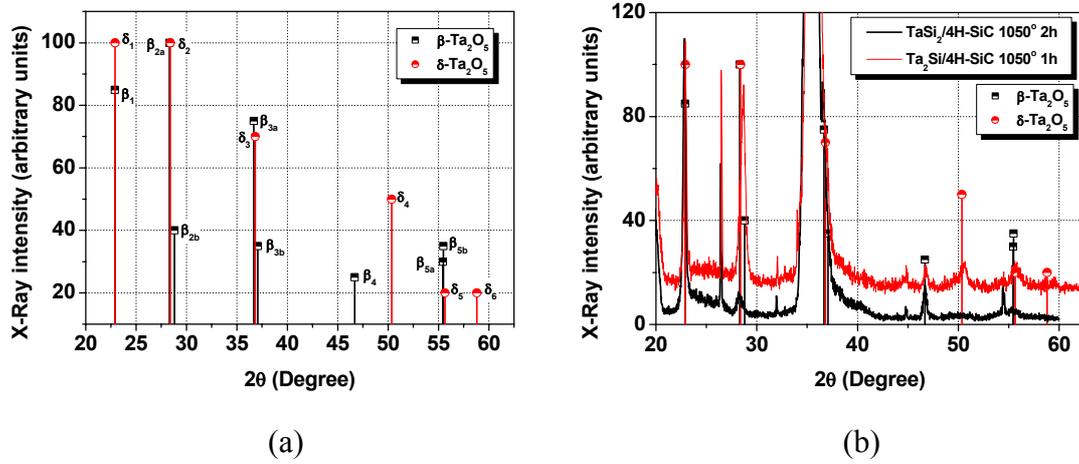
Fig. 6.50. (a) Tabulated position and intensity of the crystalline phases of Ta_2O_5. (b) The normalized measured X-Ray intensity and the tabulated position of the Ta_2O_5 peaks.

(a)

(b)
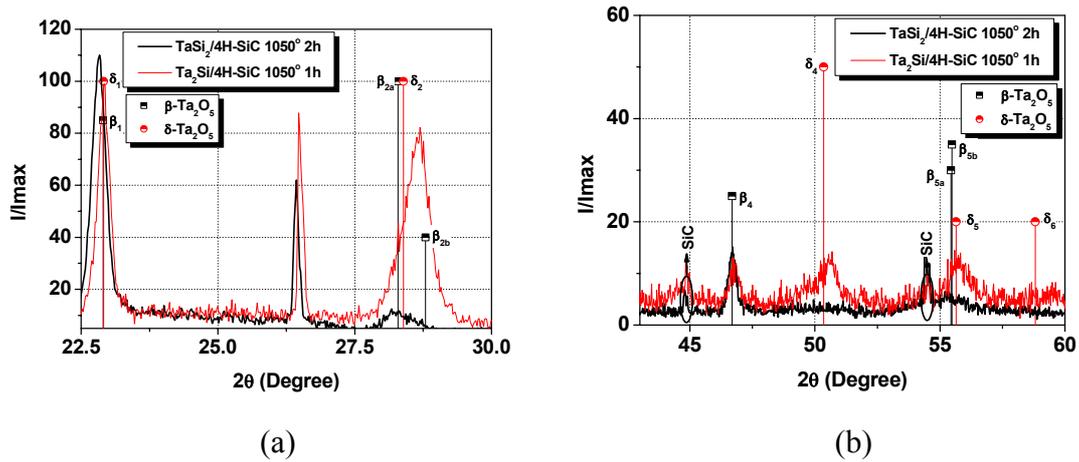
Fig. 6.51. Detail of the normalized (to I_{max}) theta-2theta scan of Ta_2Si and $TaSi_2$ films oxidized on n-type SiC for, (a) The two strongest peaks and, (b) the high 2theta peaks.

Lattice	2θ	Intensity	Name	Lattice	2θ	Intensity	Name
	22.902	85	β_1		22.909	100	δ_1
	28.291	100	β_{2a}		28.391	100	δ_2
β-Ta_2O_5 Orthorombic	28.795	40	β_{2b}	δ-Ta_2O_5 Hexagonal			
	36.666	75	β_{3a}		36.813	70	δ_3
	37.073	35	β_{3b}				
a = 6.19 Å b = 40.29 Å c = 3.88 Å	46.687	25	β_4	a = 3.62 Å c = 3.87 Å	50.351	50	δ_4
	55.441	30	β_{5a}		55.649	20	δ_5
	55.477	35	β_{5b}				
					58.816	20	δ_6

Table VI.3. Diffraction patterns for crystalline Ta_2O_5 from Ref. 60.

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Fig. 6.51(a) and Fig. 6.51(b) present the detailed normalized (respect the higher Ta_2O_5 intensity) XRD spectra for the two strongest peaks and for the higher 2θ values. An accurate analysis of the experimental XRD data aims at considering different crystal structure between the O-Ta_2Si and the O-$TaSi_2$ samples. When 40 nm of Ta_2Si is oxidized at 1050 ºC during 1 h, the main peaks seems to correspond to the δ-Ta_2O_5 with presumably a no-negligible presence of the β-Ta_2O_5 phase. Analogously, when 40 nm of $TaSi_2$ is oxidized at 1050 ºC during 2 h, only the peaks corresponding to the β-Ta_2O_5 phase seem to be present. Some important differences, for solid-state device applications, have been reported with Ta_2O_5 layers constructed with the two crystalline phases[9]. In general, δ-Ta_2O_5 layers have been found to be of higher dielectric constant than amorphous or β-Ta_2O_5 layers[8,9,12].

Glancing incidence x-ray reflectivity measurements were used to determine the oxidized layer thickness. This technique does not require crystalline film and thus, the no completely oxidized and presumably amorphous (or poor crystalline) 40 nm $TaSi_2$ oxidized during 1 h at 1050 ºC can be studied. Fig. 6.52(a) shows the XRD glancing traces for the two $TaSi_2$ oxidized samples. 50 nm has been obtained for O-$TaSi_2$ (1 h) and no peaks have been obtained for the oxidized during 2 h. As it can be inferred from Fig 6.1(b), the volume increase of O-Ta_2Si vs Ta_2Si is higher (3 times thicker) than O-$TaSi_2$ vs $TaSi_2$, that practically maintains a relationship of 1:1.
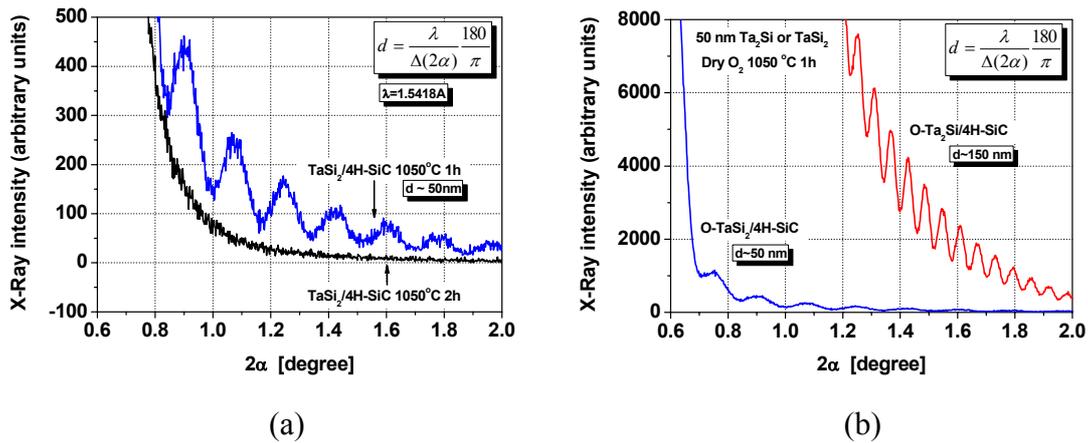
Fig. 6.52. Glancing incidence x-ray reflectivity measurements for, (a) O-Ta_2Si layers and, (b) for O-Ta_2Si and O-$TaSi_2$ oxidized under the same conditions.

High frequency C-V measurements have been carried out in our samples in order to determine its dielectric constant and the interfacial properties. Fig 6.53(a) shows the capacitance-voltage measurements for capacitors made up with 40 nm of O-Ta_2Si or O-$TaSi_2$ oxidized at 1050 ºC, with the same area. The deposited $TaSi_2$ layer and oxidized during 1 h has not been completely oxidized (no depletion-inversion), since 2 h are necessary to completely oxidize this layer. The capacitance value, along with the thickness determined from XRD glancing incidence, allows determining the effective dielectric constant, ε_r. Fig 6.53(b) presents the evolution of the dielectric constant as a function of the oxidation temperature (850-1050 ºC) for O-Ta_2Si and the comparison with the O-$TaSi_2$ at 1050 ºC. There is a strong difference between the O-Ta_2Si dielectric constant, $\varepsilon_r \sim 20$, and the one extracted for O-$TaSi_2$, $\varepsilon_r \sim 2.5$. Therefore,

while O-Ta$_2$Si layers can be considered high-*k* dielectric layers, the O-TaSi$_2$ layers have low dielectric constant values, even lower than the SiO$_2$ ($\varepsilon_r \sim 3.9$).

(a)   (b)
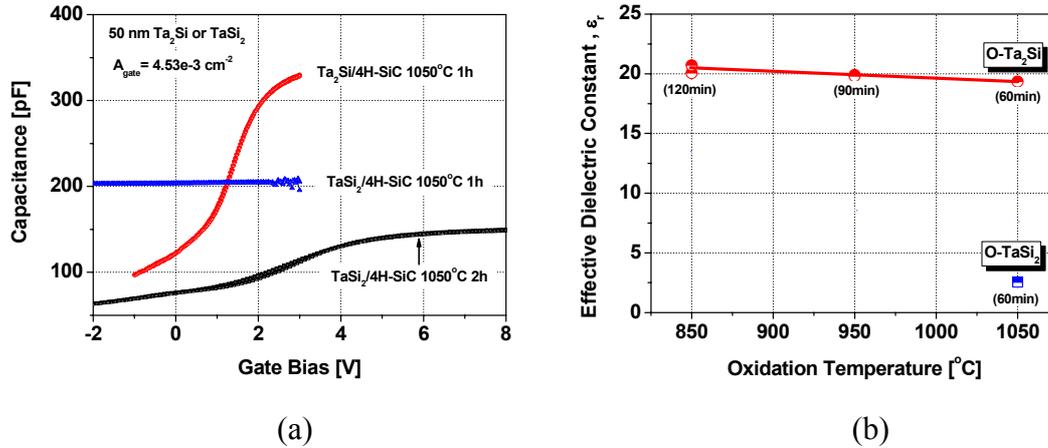
Fig. 6.53. (a) High frequency (100 kHz) C-V measurements for the O-Ta$_2$Si and O-TaSi$_2$ capacitors. (b) Effective dielectric constant extracted from MIS capacitors biased in strong accumulation.

What it comes at a surprise is that the oxidized TaSi$_2$ layers could be used as insulator, since the thermodynamic theory of its oxidation predicts metallic impurities or additional silicides in the layer[15]. However, the flat-band shift and the hysteresis (an indication of charges in the oxide) are relatively low in the O-TaSi$_2$ capacitors (Fig. 6.55). The interface states density spectra within the band gap close the conduction band is presented in Fig. 6.55(b) for O-Ta$_2$Si and O-TaSi$_2$ capacitors. As it can be derived from the figure, higher D$_{it}$ profile have been obtained for the O-TaSi$_2$ sample with $\sim 3 \times 10^{12}$ cm^{-2}eV^{-1} at $E_C - E_T = 0.2$ eV.

(a)   (b)
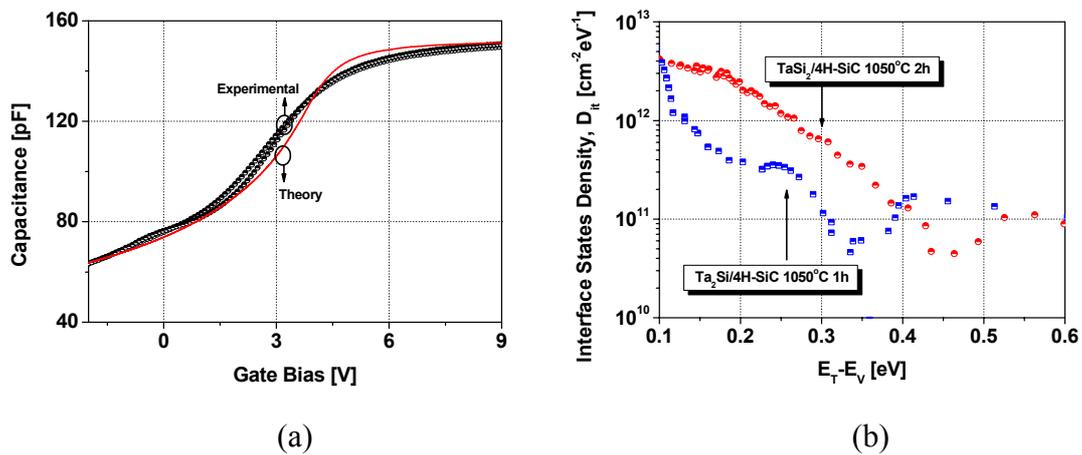
Fig. 6.55. (a) High frequency experimental and theoretical traces of the O-TaSi$_2$ films (O$_2$ 1050 ºC 120 min) on 4H-SiC. (b) Interface state density spectra of oxidized Ta$_2$Si and TaSi$_2$ films under similar oxidation conditions.

Poole-Frenkel phenomena have been invoked as the conduction mechanism of pure O-Ta$_2$Si layer on SiC and Si substrates (Section 6.1.3). This trap assisted conduction mechanism provokes high leakage current densities at relative low dielectric

fields (~1 MV/cm). However, its dielectric constant is also at least four times higher than the one of conventional SiO_2.

(a)   (b)
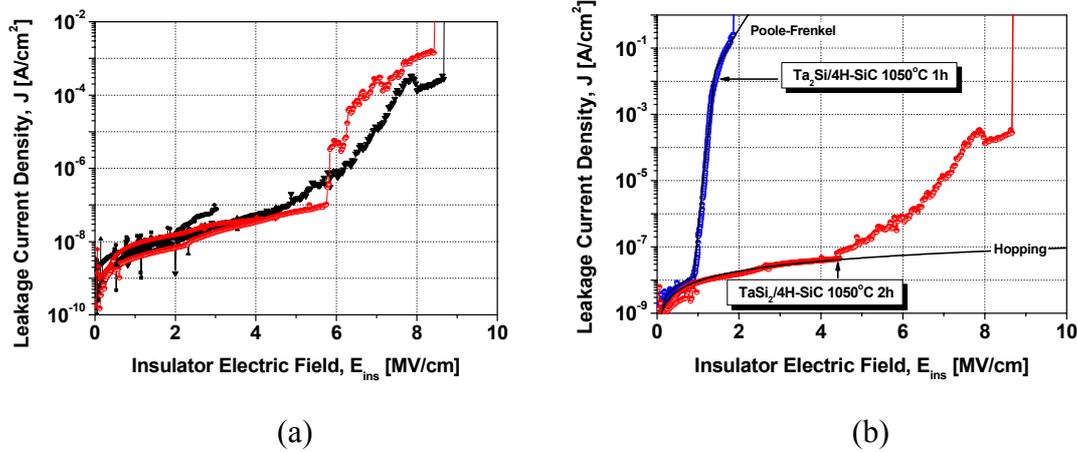
Fig. 6.56. (a) Leakage current vs insulator electric field for, (a) O-Ta_2Si (O_2 1050 ºC 120 min) and, (b) Ta_2Si and $TaSi_2$ films under similar oxidation conditions.

I-V characteristics have been measured in the O-$TaSi_2$ with a breakdown insulator electric field of ~ 6 MV/cm as it can be derived from Fig. 6.56(a). Hopping (as it occurs with thermal SiO_2) has been identified for the lower electric field. No Poole-Frenkel or other common mechanisms have been identified as the leakage current mechanism of the oxidized $TaSi_2$ layers from the 4-6 MV/cm region. As shown in Fig. 6.56(b), when compared with O-Ta_2Si layers, O-$TaSi_2$ dielectric strength is strongly increased from 1 MV/cm to 6 MV/cm. Table VI.4 resumes the main parameters extracted for both oxidized silicides.

Tantalum Silicide	Oxidation rate (O_2)	$TaSi_x$/O-Tasi$_x$ ratio	Crystalline Phases	ε_r	D_{it}	E_{bd}	Current mechanism
	(40nm) 1050^oC	*(40nm)* 1050^oC			$eV^{-1} cm^{-2}$ $E_T =0.2eV$	*MV/cm*	
O-Ta_2Si	5 min [a]	1:3	δ-Ta_2O_5 β-Ta_2O_5 [b]	20	8×10^{11}	1	Hopping / Poole-Frenkel
O-$TaSi_2$	120 min	1:1	β-Ta_2O_5	2.5	3×10^{12}	6	Hopping

Table VI.4. Comparison of the main parameters for the O-Ta_2Si and O-$TaSi_2$ layers oxidized at 1050 ºC. [a]Preliminary result. [b]δ-Ta_2O_5 is the strongest detected phase.

6.5. Conclusions

Nowadays, extensive research and development efforts to grow high-*k* dielectrics on semiconductors are underway. Applications include extending the limits of transistor gate capacitance beyond that of ultra-thin silicon dioxide, and to improve passivation layers, interface quality and gate dielectric reliability in wide band gap semiconductor devices.

In this sense, we have shown for the first time that the Ta_2Si silicide can be oxidized to form Ta_2O_5 and SiO_2 on SiC and Si substrates, taking advantage of its unique properties. Deposited Ta_2Si has been thermally oxidized at temperatures ranging 850 – 1050 ºC to produce a mixture of amorphous SiO_2 and polycrystalline δ-Ta_2O_5. TEM measurements evidence a SiO_x interfacial layer in both 4H-SiC and Si MIS capacitors. The distribution of Ta_2O_5 and SiO_2 in the bulk insulator is in channel-like SiO_2 regions between the δ-Ta_2O_5 grains. For 4H-SiC substrates, an increase of the oxidation temperature produces a densification of the SiO_2 channels, diminishing the surface roughness along with an increase of the interfacial layer thickness. On Si substrates, under the same oxidation conditions, the SiO_2 channels are much narrower and the interfacial layer thicker. The surface of the oxidized layers on Si is very smooth for all oxidation temperatures studied.

The current leakage in oxidized Ta_2Si (O-Ta_2Si) layers has been fitted with a double conduction mechanism. At low electric fields, the current is governed by the interfacial layer that sustains the gate voltage with a hopping-like conduction mechanism. When the electrical field at the interfacial layer increases up to a critical value, direct carriers tunneling into the bulk insulator occurs. These electrons are modulated by a Poole-Frenkel conduction mechanism. Asymmetric conduction behavior (gate +V or -V) has been observed for these layers, with a leakage current density as low as 10^{-8} Acm^{-2} at 1 $MVcm^{-1}$ and 4.5 $MVcm^{-1}$, respectively.

The dielectric constant obtained for 4H-SiC (and 6H-SiC) MIS is $\varepsilon_r \sim 20$ independently of the insulator thickness or the oxidation temperature. The dielectric constant obtained on Si MIS capacitors decreases with oxidation temperature and has been found to be in the 7-10 range. Interfacial traps density of this new high-k dielectric on 4H-SiC have been extracted. Annealing in N_2 the dielectric layers improves the interface characteristics (up to 8×10^{11} $cm^{-2}eV^{-1}$ at $E_C - E_T$ =0.2 eV) for samples oxidized at 850 ºC and 950 ºC, where 4H-SiC substrate oxidation is negligible. The achievement of low density of interface states is a more demanding issue in the 6H-SiC polytype than for the 4H-SiC polytype.

In order to demonstrate the feasibility of this insulator as gate material and to verify its compatibility with standard SiC MOSFET fabrication materials and processing, n-channel MOSFETs have been fabricated on p-type 4H-SiC (0001)Si face. The gate insulator has been grown by dry oxidation of 50 nm deposited Ta_2Si during 1h at 1050 ºC. For the MOSFETs fabricated on a p-implanted and annealed region, a peak mobility of 45 cm^2/Vs has been extracted with and an on-resistance of 27 mΩ·cm^2. These MOSFET performances improve the commonly reported characteristics for standard SiO_2 (O_2 oxidation) gated 4H-SiC MOSFETs, demonstrating the feasibility of this insulator and reporting one of the first well behaved MOSFET on SiC with high-*k* gate dielectric. The field effect mobility increase for O-Ta_2Si devices, takes place for relatively high electric fields, and we would be tempted to assume that electrical conduction improvements (referred as *anomalous mobility enhancement*) primarily result from current injection trough the interfacial SiO_2-like interfacial layer.

In order to improve the dielectric characteristics of the oxidized Ta_2Si layers, an interesting solution is the implementation of staked dielectrics with a thermally grown SiO_2 layer (T-SiO_2) in the semiconductor-insulator interface. Nevertheless, the interfacial characteristics of T-SiO_2/O-Ta_2Si capacitors are similar to those of T-SiO_2 capacitors. The stacked MIS structure presents enhanced leakage current properties when compared with pure O-Ta_2Si or even with experimental standard thermal oxidation. MOSFETs have been fabricated on 4H-SiC interfacial with low temperature thermal oxidation performed at 1050 ºC during 1 h prior to the deposition and

subsequent oxidation of Ta$_2$Si. The extracted field-effect is significantly lower when compared with a conventional thermal 4H-SiC MOSFET, maintaining its value lower than 1 cm^2/Vs, up to the anomalous mobility improvement for the higher gate bias.

In the search of better gate insulator performances, we propose the N$_2$O oxidation of deposited Ta$_2$Si layer to combine the nitrogen incorporation at the interface as well as the high-*k* advantages of the O-Ta$_2$Si layers. Additionally, N$_2$O post deposition thermal treatments on pure Ta$_2$O$_5$ capacitors have shown a reduction of the current leakage with an increment of the insulator reliability. Ta$_2$Si layers have been deposited and oxidized in (diluted) N$_2$O at 950 ºC during 5 min (N$_2$O-Ta$_2$Si) on p-type Si and n-type 4H-SiC. Very short times have been used evidencing the rapid oxidation of the Ta$_2$Si layer, at least in a N$_2$O ambient. XRD analysis have not shown crystalline phases on Si substrates. Ta$_2$O$_5$ crystalline peaks are clearly evidenced on n-type 4H-SiC substrates. No significant differences in the XRD spectra of O-Ta$_2$Si (850 – 1050 ºC) and N$_2$O-Ta$_2$Si (1100 ºC) on 4H-SiC, have been detected. Dielectric constants values of ε_r=19.5 and ε_r=8.4 have been determined for N$_2$O-Ta$_2$Si capacitors on 4H-SiC and Si respectively. Significantly higher D$_{it}$ profiles have been obtained for the N$_2$O-TaSi$_2$/4H-SiC samples with (6×10^{12} cm^{-2}eV^{-1} at $E_C - E_T$=0.2 eV). On Si capacitors, the leakage current density is diminished for the N$_2$O-Ta$_2$Si capacitors when compared with the O-Ta$_2$Si MIS structures. On 4H-SiC substrates, although the trap assisted conduction Poole-Frenkel mechanism can be observed in the N$_2$O-Ta$_2$Si layers, the absence (or the lack of influence) of interfacial layer allows the trap assisted mechanism even at the lower electric fields, similarly to O-Ta$_2$Si layers oxidized at 750 ºC. However, the current leakage density is orders of magnitude lower in this last case than for N$_2$O-Ta$_2$Si capacitors. The difference seems to lie in the higher degree of crystallinity of the N$_2$O-Ta$_2$Si sample.

The most common of Tantalum silicides, TaSi$_2$, has been dry thermally oxidized on 4H-SiC substrates. At least 120 min are needed to completely oxidize the TaSi$_2$ layer (40 nm 1050 ºC) on 4H-SiC, and Ta$_2$O$_5$ peaks arise in the XRD spectra. For O-Ta$_2$Si (1050 ºC 1 h), the main peaks seems to correspond to the δ-Ta$_2$O$_5$ with presumably a non-negligible presence of the β-Ta$_2$O$_5$ phase. For O-TaSi$_2$ (1050 ºC 2 h), only the peaks corresponding to the β-Ta$_2$O$_5$ phase seem to be present. In general, δ-Ta$_2$O$_5$ layers have a higher dielectric constant than amorphous or β-Ta$_2$O$_5$ layers. What it comes at a "surprise" is that the oxidized TaSi$_2$ layers could be used as insulator, since the thermodynamic theory of its oxidation predicts metallic impurities or additional silicides in the layer. However, the flat-band shift and the hysteresis (an indication of charges in the oxide) are relatively low in the O-TaSi$_2$ capacitors. However, while O-Ta$_2$Si layers can be considered high-*k* dielectric layers, the O-TaSi$_2$ layers have low dielectric constant (ε_r~2.5), even lower than SiO$_2$. Poor D$_{it}$ profiles have been obtained for the O-TaSi$_2$ sample with 3×10^{12} cm^{-2}eV^{-1} at $E_C - E_T$=0.2 eV. When compared with O-Ta$_2$Si layers, O-TaSi$_2$ dielectric strength is strongly increased from 1 MV/cm to 6 MV/cm. No Poole-Frenkel or other common mechanisms have been identified as the leakage current mechanism.

References

1   M. K. Das, *Mater. Sci. Forum,* **457-460**, 1275, (2004).

2   S. Dhar, Y. W. Song, L. C. Feldman, T. Isaacs-Smith, C. C. Tin, J. R. Williams, G. Chung, T. Nishimura, D. Starodub, T. Gustafsson and E. Garfunkel, *Appl. Phys. Lett.,* **84**, 1498, (2004).

3   E. Arnold and D. Alok, *IEEE Trans. Elect. Dev.*, **48**, 1870, (2001).

4   G. D. Wilk, R. M. Wallace and J. M. Anthony, *J. Appl. Phys.,* **89**, 5243, (2001).

5   I. C. Kizilyalli, R. Y. S. Huang and P. K. Roy, *IEEE Electron Device Lett.,* **19**, 423, (1998).

6   R. Beyers, *J. Appl. Phys.,* **56**, 147, (1984).

7   A. Pérez, D. Tournier, J. Montserrat, N. Mestres, F. Sandiumenge and J. Millán, *Mater. Sci. Forum,* **457-460**, 845, (2004).

8   B.K. Moon, C. Isobe and J. Aoyama, *J. Appl. Phys.,* **85**, 1731, (1999).

9   C. Chaneliere, S. Four, J. L. Autran, R. A. B. Devine and N. P. Sandler, *J. Appl. Phys.,* **83**, 4823, (1998).

10   P. C. Joshi and M. W. Cole, *J. Appl. Phys.,* **86**, 871, (1999).

11   E. Atanassova, D. Spassov, A. Paskeleva, J. Koprinarova, M. Georgieva, *Microelectronics Journal* **33**, 907, (2002)

12   C. Chaneliere, J. L. Autran, R. A. B. Devine and B. Balland, *Mater. Sci. Eng. R.,* **22**, 269, (1998).

13   S. Seki, T. Unagami and B. Tsujiyama, *J. Electrochem. Soc.,* **182**, 2505, (1983).

14   A. Cros, and K. N. Tu, J. Appl. Phys. 60, 3323, (1986)

15   K. C. Saraswat, R. S. Nowicki, and J. F. Moulder, Appl. Phys. Lett. 41, 1127, (1982)

16   M. Kardar, G. Paris, Y. C. Zhang. *Phys. Rev. Lett*. 56, 889, (1998)

17   W. S. Lau, L. L. Leong, Taejoon Han and Nathan P. Sandler, *Appl. Phys. Lett.,* **83**, 2835, (2003).

18   R. M. Fleming, D. V. Lang, C. D. W. Jones, M. L. Steigerwald, D. W. Murphy, G. B. Alers, Y.-H. Wong, R. B. van Dover, J. R. Kwo and A. M. Sergent, *J. Appl. Phys.,* **88**, 850, (2000).

19   S. Ezhilvalavan and Tseung-Yuen Tseng, *J. Appl. Phys.,* **89**, 4797, (1998).

20   J-Y. Tewg, Y. Kuo, J. Lu and B. W. Schueler, *J. Electrochem. Soc.,* **151**, 1731, (2004).

21   E. Atanassova and A. Paskaleva, *J. Mat. Sci.,* **14**, 671, (2003).

22   S. Zaima, T. Furuta, Y. Koide, Y. Yasuda and M. Ida, *J. Electrochem. Soc.,* **137**, 2867, (1990).

23   R. A. B. Devine, *Appl. Phys. Lett.*, **68**, 1924, (1996).

24   G. B. Alers, D. J. Werder, Y. Chabal, H. C. Lu, E. P. Gusev, E. Garfunkel, T. Gustafsson and R. S. Urdahl, *Appl. Phys. Lett.,* **73**, 1517, (1998).

25   Y-S. Lai, K-J. Chen and J. S. Chen, *J. Appl. Phys.,* **91**, 6428, (2002).

26   S. M. Sze, *Physics of Semiconductor Devices*, Wiley, New York, (1969).

27   J. R. Yeargan and H. L. Taylor, *J. Appl. Phys.,* **39**, 5600, (1968).

28   N. V. Nguyen, C. A. Richter, Y. J. Cho, G. B. Alers and L. A. Stirling, *Appl. Phys. Lett.,* **77**, 3012, (2000).

29   D. Frohman-Bentchkowsky and M. Lenzlinger, *J. Appl. Phys.,* **40**, 3307, (1969).

30   L. A. Lipkin and J. W. Palmour, *IEEE Trans. Electron Devices,* **46**, 525, (1999).

[31] K. Y. Gao, T. Seyller, L. Ley, F. Ciobanu, G. Pensl, A. Tadich, J. D. Riley and R. G. C. Leckey, *Appl. Phys. Lett.,* **83**, 1830, (2003).

[32] C. Bondoux, P. Prené, P. Belleville, F. Guillet and R. Jérisian, *Mater. Sci. Forum,* **457-460**, 1373, (2004).

[33] V. V. Afanas'ev, S. A. Campbell, K. Y. Cheong, F. Ciobanu, S. Dimitrijev, G. Pensl, A. Stesmans and L. Zhong, *Mater. Sci. Forum,* **457-460**, 1361, (2004).

[34] K. Chu, J. P. Chang, M. L. Steigerwald, R. M. Fleming, R. L. Opila, D. V. Lang, R. B. Van Dover and C. D. W. Jones, *J. Appl. Phys.,* **91**, 308, (2002).

[35] C. Chaneliere, S. Four, J. L. Autran and R. A. B. Devine, *Microelectron. Reliab.,* **39**, 261 (1999).

[36] S. C. Sun and T. F. Chen, *IEEE Trans. Electron Devices*, **44**, 1027, (1997).

[37] W. S. Lau, L. Zhong, Allen Lee, C. H. See, Taejoon Han, N. P. Sandler and T. C. Chong, *Appl. Phys. Lett.,* **71**, 500, (1997).

[38] G. S. Oehrlein, F. M. d'Heurle and A. Reisman, *J. Appl. Phys.,* **55**, 3715, (1984).

[39] M. Khun, *Solid-State Electron.,* **13**, 873, (1969).

[40] A. Pérez-Tomás, P. Godignon, N. Mestres, D. Tournier, J. Montserrat and J. Millán, *Mat. Res. Soc. Symp. Proc.,* **815**, J3.2.1, (2004).

[41] E. H. Nicollian and J. R. Brews, *MOS Physics and Technology*, Wiley, New York (1982).

[42] Center for X-Ray optics, Berkeley lab., http://www.cxro.lbl.gov/

[43] T-W. Huang, H-Y. Lee, Y-W. Hsieh, and C-H. Lee, *J. Crystal Growth* 237-239, 492, (2002).

[44] International Advanced Materials, http://www.iamaterials.com

[45] J. R. LaRoche, J. Kim, J. W. Johnson, B. Luo, B. S. Kang, R. Mehandru, Y. Irokawa, S. J. Pearton, G. Chung and F. Ren, *Electrochem. and Solid-State Lett.* **7**, G21, (2004).

[46] G. S. Oehrlein, *Thin Solid Films,* **156**, 207, (1988).

[47] C. Radtke, I. J. R. Baumvol, B. C. Ferrera, and F. C. Stedile, *Appl. Phys. Lett.,* **85**, 1, (2004).

[48] V. V. Afanas'ev, A. Stesmans, and C. J. Harris, *Mater. Sci. Forum* 389-393, 961, (2002)

[49] R. Schorner, P. Friedrichs, D. Peters, and D. Stephani, *IEEE Electron Device Lett.* 20, 241, (1999)

[50] R. Gómez-San Román, R. Pérez-Casero, J. Perrière, J. P. Enard and J. M. Martínez-Duart, *J. Vac. Sci. Technol. A,* **13**, 54, (1995).

[51] Q. Lu, D. Park, A. Kalnitsky, C. Chang, C-C. Cheng, S. P. Tay, T-J. King, C. Hu, *IEEE Electron Device Lett.* 19, 341, (1999)

[52] Y. P. Tsividis, *Operation and modeling of the MOS transistor*, McGraw-Hill in Electrical Engineering, (1987).

[53] A. Pérez-Tomás, P. Godignon, J. Montserrat, J. Millán, N. Mestres, P. Vennegues and J. Stoemenos, *J. Electrochem. Soc.*, **152**, G259, (2005).

[54] A. Pérez-Tomás, P. Godignon, N. Mestres, D. Tournier and J. Millán, *Proccedings of CDE 05*, Febrary 2 - 4, 2005, Tarragona, Spain.

[55] H. Yano, Y. Furumoto, T. Niwa, T. Hatayama, Y. Uraoka, and T. Fuyuki, *Mater. Sci. Forum,* **457-460**, 1333, (2004).

[56] P. Jamet, S. Dimitrijev, and P. Tanner, *J. Appl. Phys*, **90**, 5058, (2001).

[57] L. A. Lipkin, M. K. Das, and J. W. Palmour, *Mater. Sci. Forum* **389-393**, 985, (2002).

[58]   K.-C. Chang, L. M. Porter, J. Bentley, C.-Y. Lu, and J. Cooper, Jr., *J. Appl. Phys.* **95**, 8252, (2004).

[59]   Eckhard Pippel, Jörg Woltersdorf, Halldor Ö. Ólafsson, and Einar Ö. Sveinbjörnsson, *J. Appl. Phys.* **97**, 034302, (2005).

[60]   ASTM X-ray Powder Data Card, No. 18-1304

[61]   A. Fukumoto, and K. Miwa. *Phys. Rev. B* **55**, 11155 (1997)

Chapter VII

Field-effect mobility model with high traps density in the interface

Besides its favourable physical properties, high performant MOSFET's fabrication in SiC remains an open issue due to its low channel mobility values. The effect of charge trapping and the scattering at interface states have been invoked as the main reasons for mobility reduction in SiC thermal oxidized MOS gated devices[1-5]. In this chapter, we propose a compact mobility model based on the well established Lombardi model[6], taking into account interface trap scattering. Using 2D electrical simulations and the proposed model, the experimental field effect mobility of 4H-SiC devices has been fitted with a good agreement. The Coulomb scattering on interface traps is also used to explain the commonly reported dependence of the field effect mobility on the substrate impurity concentration and temperature. On the other hand, anomalous high inversion channel mobilities have been experimentally extracted in 4H-SiC MOSFETs fabricated with oxidized Ta$_2$Si high-k dielectric as gate insulator in the strong inversion regime, as was shown in *Chapter VI*. This phenomenon has also been observed for MOSFET devices using thermal SiO$_2$. However, the measured interface states density has not been particularly reduced in these devices. This anomalous mobility enhancement has been explained in terms of effective inversion charge increase due to a carrier injection through the gate. The additional inversion channel charge has been evaluated with the mobility model considering the interface trapping and scattering of electrons.

7.1. Interface traps Coulomb scattering modeling on the effective channel mobility in 4H-SiC MOSFET devices

The channel conduction modeling on thermally oxidized Silicon carbide metal-oxide-semiconductor field effect devices must be performed taking into account the effect of the high density of traps encountered at its semiconductor/oxide interface[1,5].

These traps are originated during the oxidation of the SiC surface and their effect is the Coulomb scattering and trapping of free carriers when the inversion layer is formed. This effect is specially harmful in the case of 4H-SiC MOSFET devices, due to the rapid increase of interface state density when approaching to the conduction band. One of the keys of the success of the Si based MOS technology is the excellent interfacial characteristics between the silicon and its native thermal oxide. In the Si/SiO$_2$ interface, the oxide and interfacial traps can be effectively erased with adequate post-oxidation annealing processes and the traps Coulomb scattering can be generally neglected. Hence, the traditional mobility model for Si devices, such as the usually incorporated in commercial 2-D simulators, does not account for the effect of a large density of interfacial states on the channel conduction. In this section, a mobility expression, based on the Lombardi mobility model, has been developed including this scattering effect. The mobility degradation due to the number and distribution of the interface traps within the band-gap has been analyzed. The interfacial traps scattering effect qualitatively explains the commonly reported dramatic reduction on the channel mobility, the temperature and substrate doping behavior.

7.1.1. Lombardi mobility model with traps coulomb scattering

The Lombardi mobility model describes the degradation observed in MOSFET devices taking into account acoustic-phonon scattering (μ_{AC}), surface roughness scattering (μ_{SR}) and the effect of Coulombic scattering (μ_C) can also be added. As stated before, the effect of Coulombic scattering (mainly due to oxide fixed charge and surface states charge) is known to dominate the surface electron mobility especially at low temperature and in weakly inverted surfaces in SiC devices. Hence, the inversion carrier mobility can be approximated by the sum of four terms, where μ_B represents the bulk mobility factor (see appendix Ref. 6):

$$\mu_{inv} = \left[\frac{1}{\mu_B} + \frac{1}{\mu_{AC}} + \frac{1}{\mu_{SR}} + \frac{1}{\mu_C} \right]^{-1} \quad (7.1)$$

The Coulomb mobility term can be described by the expression (7.2) at a point z far from the interface, accounting a fixed charge distribution and the effect of carrier screening:

$$\mu_C(z) \propto \frac{1}{Q_{trap}} T^\alpha \left(\int_0^z n(z)dz \right)^\beta = \frac{1}{Q_{trap}} T^\alpha Q_{inv}{}^\beta \quad (7.2)$$

where Q_{inv} is the inversion charge per unit area, Q_{trap} is the trapped charge per unit area, T is the temperature, and α is a temperature coefficient that will be analyzed latter on. The expressions for Q_{inv} and Q_{trap} have been derived from the literature. The inversion-layer carrier density per unit area is given by[7]:

$$Q_{inv} = \int_0^{\phi_S} \frac{n(\phi)}{E_{YS}(\phi)} d\phi \quad (7.3)$$

where E_{YS} is the perpendicular electric field, ϕ_s is the Fermi potential, and n is the free-carrier density, all of them at the interface. For a continuous energy distribution of interface states (D$_{it}$), the trapped charge interface state charge[8] may be approximated by:

$$Q_{trap} = \int_{E_i}^{E_F} D_{it}(E)\,dE \qquad (7.4)$$

Thus, the Coulomb mobility term can be written as:

$$\mu_C = N \frac{1}{Q_{trap}} T^\alpha Q_{inv}{}^\beta = N T^\alpha \frac{\left[\int_0^{\phi_S} \dfrac{n(\phi)}{E_{YS}(\phi)} d\phi\right]^\beta}{\int_{E_i}^{E_F} D_{it}(E)\,dE} \qquad (7.5)$$

Considering all the above degradation factors, the total inversion mobility can be rewritten as[6]:

$$\mu_{inv} = \left[\frac{1}{\mu_B} + \frac{1}{\mu_{AC}} + \frac{1}{\mu_{SR}} + \frac{1}{\mu_C}\right]^{-1} =$$

$$= \left[\frac{1}{\mu_B(N_A)} + \frac{1}{\dfrac{B}{E_\perp} + \dfrac{C1 N_A^{\alpha 1}}{T\sqrt[3]{E_\perp}}} + \frac{E_\perp^{\gamma 1}}{D} + \frac{1}{N T^\alpha} \frac{\int_{E_i}^{E_F} D_{it}(E)\,dE}{\left[\int_0^{\phi_S} \dfrac{n(\phi)}{E_{YS}(\phi)} d\phi\right]^\beta}\right]^{-1} \qquad (7.6)$$

The bulk mobility (low field channel mobility) is described by the expression[9]:

$$\mu_B(N_A) = \mu_{min} + \frac{\mu_{max} - \mu_{min}}{1 + (N_A / N_{REF})^{\lambda 1}} \qquad (7.7)$$

The common values reported for μ_{max}, μ_{min}, N_{REF} and $\lambda 1$ along with the bulk parameters of 4H-SiC have been discussed elsewhere[10-12]. The set of fitting parameters for the acoustic-phonon scattering are B, $C1$ and $\alpha 1$. D and $\gamma 1$ are parameters used to describe the surface scattering term. In order to compute the Coulomb scattering term, a proportionality constant N has been introduced. The Coulomb scattering term has been experimentally described as a function of the inversion charge per unit area Q_{inv}^β. β has been reported in the range $0.5 - 1$ [1,6,13]. Our experimental results show the most accurate mobility fit for $\beta \approx 1$. The default value ($\alpha =1$) proposed by Lombardi *et al.*[6] has been used for the temperature dependence of μ_C. The D$_{it}$ profile has been experimentally extracted by means of Terman, conductance and Hi-Low method[8,14] on 4H-SiC samples. The experimental D$_{it}$ has been fitted using analytical functions, taking into account the rapid increase of D$_{it}$ close the conduction and valence band edges. The interface density spectra in the upper region of the band gap is described by:

$$D_{it} = \Delta \times \begin{cases} \xi_1 + \xi_2 \exp\left(\dfrac{E - E_C}{\chi}\right) & E < E_0 \\ \\ \theta_1 + \theta_2 \exp\left(\dfrac{E - E_C}{\lambda}\right) & E > E_0 \end{cases} \qquad (7.8)$$

where Δ, ξ_1, ξ_2, θ_1, θ_2, χ and λ are parameters that fit the experimental interfacial traps spectra within the bandgap. E_0 is an energy level for describing the rapid increase of interface state density when approaching to the conduction band in SiC/SiO$_2$ interfaces. E_C is the conduction band energy.

7.1.2. 4H-SiC MOSFETs 2-D simulations

The perpendicular electrical field at the SiC surface E_{YS}, the inversion layer concentration n and the Fermi potential ϕ_s are needed to compute the model. The charge-sheet model[7,15] and other analytic solutions restrict the discussion to systems in equilibrium. Such systems include MOS capacitors and MOSFETs with small applied drain bias. The electrical properties are calculated from deep subthreshold to heavy inversion. Poisson equation can be expressed as:

$$\frac{dE}{dx} = \frac{q}{\varepsilon_s}\left[N_D^+ - N_A^- + p - n\right] \quad (7.9)$$

Using 2D-Simulation packages with trapping effect, such as MEDICI[16], the Poisson equation can be modified to include the density of electrons that are trapped at the interface states or the oxide charge effects:

$$\frac{dE}{dx} = \frac{q}{\varepsilon_s}\left[N_D^+ - N_A^- + p - n - \sum_i N_{it} f_i\right] - \rho_s \quad (7.10)$$

N_{it} is the total number of traps (cm^{-3}eV^{-1}) for the *ith* energy level and f_i is the occupancy factor. N_{it} is also a function of energy and position. In MEDICI simulator N_{it} is positive for electron traps and negative for hole traps. In SiC MOS devices, the interfacial traps in the upper half of the band gap are believed to be acceptor-like in nature. The charge states close to the two band edges are usually almost equal in magnitude and opposite in their charging character; that is, states near the conduction and valence band are believed to be acceptor-like and donor-like in nature[17-19], respectively. Mobility MEDICI simulations taking into account a donor distribution in the lower half of the bandgap have supplied similar results to those considering only the acceptor states of the upper band gap. Thus, for simplicity, the interfacial D$_{it}$ has been restricted to the upper band gap acceptor states. ρ_s is a surface charge density that may be present due to fixed charge in insulator materials. Additionally, the use of 2D simulators allows taking into account a large number of other known effects as carrier to carrier scattering, impact ionization or recombination. The effective perpendicular electric field at the interface is computed using the relation[16]:

$$E_\perp = \zeta_1 E_{YS} + \zeta_2 \times \left[\left(\frac{\varepsilon_I}{\varepsilon_s} \right) E_{YI} + \frac{q Q_I}{\varepsilon_s} - E_{YS} \right] \quad (7.11)$$

where ζ_1 and ζ_2 are constant factors, ε_s and ε_I are the permittivity of the semiconductor and the insulator respectively, Q_I is the insulator charge, E_{YS} and E_{YI} are the perpendicular electric fields at the interface in the semiconductor and the in the dielectric, respectively. Test structures have been implemented in MEDICI with a channel length of 4 μm. The structural parameters, such as epitaxy doping level, drain and source diffusion length and width, or oxide capacitance, were determined from the fabricated devices (*Chapter IV*).

Once ϕ_S, $E_{YS}(\phi)$, $E_\perp(\phi)$ and $n(\phi)$ have been determined at the semiconductor surface for each gate bias, the Lombardi model with interface traps scattering can be evaluated. The values for the three "conventional" (μ_B, μ_{SR} and μ_{AC}) terms of Lombardi model are listed in Table VII.1.

Parameter	Units	4H-SiC	References
Acoustic-phonon scattering			
B	cm/s	1.0×10^6	[6],[12],[16]
$C1$	K·cm/s·	1.74×10^5	[12]
	(V/cm)$^{-2/3}$	3.23×10^6	[6],[16]
$\alpha 1$		0.0284	[16]
Surface roughness scattering			
D	cm^2/Vs·	5.82×10^{14}	[12], [16]
	(V/cm)$^{\gamma 1}$		
$\gamma 1$		2.0	[16]
Low field channel mobility			
μ_{min}	cm^2/V·s	40	[9], [12]
N_{REF}	cm^{-3}	2×10^{17}	[9], [12]
$\lambda 1$		0.76	[9], [12]
μ_{max}	cm^2/V·s	950	[9], [12]

Table VII.1. Lombardi model MEDICI parameters values for the three first terms, μ_B, μ_{SR} and μ_{AC}.

The value of these parameters are extracted from the literature and especially from the work of Linewih *et al.*[12], that attempt to fit the field mobility of 4H-SiC devices with N$_2$O grown gate oxides using the conventional Lombardi model. For the computation of the Coulomb scattering term (μ_C), the interface traps profile within the bandgap as a function of the Fermi potential (or energy), is required. The D$_{it}$ profile has been experimentally extracted by means of Terman, conductance and Hi-Low method on 4H-SiC samples. The experimental D$_{it}$ has been fitted with the equation (7.8) taking into account the rapid increase of D$_{it}$ close the conduction and valence band edges. Fig. 7.1 shows the experimental interface trap spectra within the bandgap extracted from an standard thermal oxidized 4H-SiC (0001) Si face sample (T-SiO$_2$). The theoretical lines are computed using Δ as parameter. Δ is used to simulate the influence of different

traps density. Varying Δ roughly emulates the reduction/increase of interface states, helping to understand qualitatively their influence on the electrical MOSFET characteristics. E_i is the intrinsic Fermi level. From experimental traces, ξ_1, ξ_2, θ_1, θ_2, χ and λ and E_0 have been determined with Δ=1.
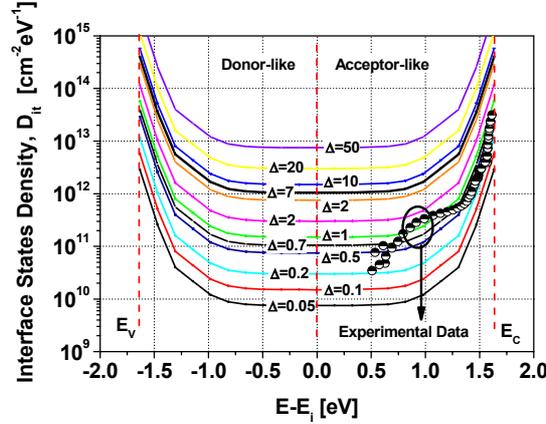
Fig. 7.1. Interface states spectra with Δ as parameter. Solid points are experimental points for thermal SiO$_2$ on n-type 4H-SiC capacitors.

In our standard dry O$_2$ oxidation carried out at 1160 ºC during 3 h, an interface states density of 1×10^{12} cm^{-2}eV^{-1} at $E_C - E_T$=0.2 eV has been extracted. α and β parameters of the μ_C term have been derived from the literature and adapted to our experimental results, and N was fitted with Δ=1 and T=300 K. The value of the parameters involved in the definition of the interface traps Coulomb scattering term are listed in Table VII.2.

Parameter	Units	4H-SiC	References
Traps Coulomb scattering fitting parameters			
α		1	[6]
β		1	[1], [14]
N	cm^2/VsK$^\alpha$	0.0128	
D$_{it}$ profile fitting parameters			
ξ_1	cm^{-2}eV^{-1}	4.24×10^{11}	
ξ_2	cm^{-2}eV^{-1}	2.01×10^{13}	
θ_1	cm^{-2}eV^{-1}	1.92×10^{12}	
θ_2	cm^{-2}eV^{-1}	8.59×10^{13}	
χ	eV	0.062	
λ	eV	0.022	
$E_0 - E_i$	eV	1.47	

Table VII.2. Interface traps simulation parameters values.

7.1.3. The inversion and the field effect mobility in MOSFETS with a large density of interface states.

In a long-channel MOSFET, at low drain voltage V_{DS} and for a given gate voltage, the drain current is[1]

$$I_{DS} = \frac{W}{L} q \mu_{inv} |Q_{inv}| V_{DS} = \frac{W}{L} \sigma V_{DS} \quad (7.12)$$

where W and L are the gate width and length, Q_{inv} is the inversion charge, μ_{inv} is the average mobility of the carriers in the inversion layer, and

$$\sigma = q \mu_{inv} |Q_{inv}| \quad (7.13)$$

is the sheet conductance of the inversion layer. A common procedure for obtaining the mobility from the transfer characteristic of the MOSFET is to relate the inversion charge to the gate voltage V_{GS}

$$Q_{inv} = -\frac{C_I}{q}(V_{GS} - V_{th}) \quad (7.14)$$

where V_{th} is the threshold voltage and C_I is the insulator capacitance per unit area.

From (7.12) and (7.14), two different expressions for mobility are defined[1]: the effective mobility μ_{EFF}

$$\mu_{EFF} = \frac{L}{WC_I(V_{GS} - V_{th})}\left(\frac{dI_{DS}}{dV_{DS}}\right) \quad (7.15)$$

and the field-effect mobility μ_{FE}

$$\mu_{FE} = \frac{L}{WC_I V_{DS}}\left(\frac{dI_{DS}}{dV_{GS}}\right) = \frac{1}{C_I}\frac{d\sigma}{dV_{GS}} \quad (7.16)$$

In the absence of carrier trapping in interface states, and in the case where the mobility is independent of the drain voltage and the gate voltage, (7.15) and (7.16) yield the same values for the mobility. In silicon MOSFETs the effects of interface states can generally be ignored, but the carrier mobility does change with the gate voltage. If the slope dI_{DS}/dV_{GS} of a typical "S"-shaped transfer characteristic curve is taken at the steepest part of the $I_D - V_G$ characteristic, and V_{th} is taken as the intercept of the straight line representing that slope, the mobility values calculated from (7.15) and (7.16) will be equal and representative of the carrier mobility μ_{inv}.

In SiC MOSFET with a large density of interface states, the values of μ_{EFF} and μ_{FE}, determined from (7.15) and (7.16) at the point of steepest slop of the $I_D - V_G$ characteristics, will be equal, but will not correspond to the true mobility μ_{inv}. The

intercept in the $I_D - V_G$ curve now depends on the trapped charge density and can no longer be used as an estimate of the threshold voltage. Equation (7.15), therefore, cannot be easily applied, but the field-effect mobility given by (7.16) can be estimated as described further on.

The calculation of the immobile interface charge, which includes the oxide fixed charge Q_f and the charge Q_{trap} trapped in interface states, requires only the knowledge of Q_{inv} as a function of V_{GS}. A change δV_{GS} in gate voltage results in a change δQ_{trap} in the charge trapped in interface states and a change δQ_{inv} in the inversion charge[1], as the surface Fermi level E_F moves away from the intrinsic level E_i, towards the conduction band edge E_C

$$\delta V_{GS} = -\frac{q}{C_{ins}}\left(\delta Q_{trap} + \delta Q_{inv}\right) \quad (7.17)$$

Combining (7.13), (7.16) and (7.17) we obtain:

$$\mu_{FE} = \mu_{inv}\frac{\left[1 + \dfrac{Q_{inv}}{\mu_{inv}}\dfrac{d\mu_{inv}}{dQ_{inv}}\right]}{1 + \dfrac{dQ_{trap}}{dQ_{inv}}} \quad (7.18)$$

The expression in square brackets accounts for the variation of carrier mobility with gate voltage. Kang *et al.*[4] reported that this term equals unity if μ_{FE} is computed at the point of the steepest slope of $I_{DS} - V_{GS}$ characteristic. In our case, we use the inversion mobility expression proposed by Lombardi *et al.*[6] with the Coulomb scattering term (7.6). At room temperature, it is generally assumed that the dominant degradation mechanism in SiC MOSFET, especially with thermal gate oxides, is the Coulomb scattering term. Thus equation (7.6) can be reasonably simplified to

$$\mu_{inv} \approx \mu_C = NT^\alpha \frac{Q_{inv}^\beta}{Q_{trap}} \quad (7.19)$$

Considering this last assumption, the expression in square brackets in (7.18) equals $(1+\beta)$ at the point of the steepest slope and when the semiconductor surface gets degenerated, as we will show further on. On the other hand, the trapped charge Q_{trap} also is function of the Fermi level position. If the gate bias is sufficiently high, in strong inversion mode, the semiconductor becomes degenerate and the Fermi level reaches the conduction band. Thus, the charge trap Q_{trap} reaches its maximum value, remaining constant for higher gate biases. In this situation Q_{trap} is not a function of the gate voltage and thus,

$$\delta V_{GS} = -\frac{q}{C_I}\left(\delta Q_{inv}\right) \quad (7.20)$$

Then combining (7.19) and (720) the mobilities relationship can be rewritten as

i) $E_F < E_C$

$$\mu_{FE} = \mu_{inv} \frac{\left[1 + \dfrac{Q_{inv}}{\mu_{inv}} \dfrac{d\mu_{inv}}{dQ_{inv}}\right]}{1 + \dfrac{dQ_{trap}}{dQ_{inv}}} = \mu_{inv} \frac{\left[1 + \beta - \dfrac{Q_{inv}}{Q_{trap}} \dfrac{dQ_{trap}}{dQ_{inv}}\right]}{1 + \dfrac{dQ_{trap}}{dQ_{inv}}} \qquad (7.21)$$

ii) $E_F > E_C$

$$\mu_{FE} = \mu_{inv}\left[1 + \frac{Q_{inv}}{\mu_{inv}} \frac{d\mu_{inv}}{dQ_{inv}}\right] = \mu_{inv}\left[1 + \beta\right] \qquad (7.22)$$

The field-effect mobility in the strong inversion range is proportional to the inversion mobility of the layer, with a $(1 + \beta)$ coefficient when the Coulomb scattering term from equation (7.19) is considered. Fig. 7.2(a) shows the simulated inversion and trapped charge that are in the basis of the computation of the inversion channel mobility, μ_{inv}. Note that Q_{trap} is a constant value when the Fermi level reaches the conduction band energy.

(a)

(b)
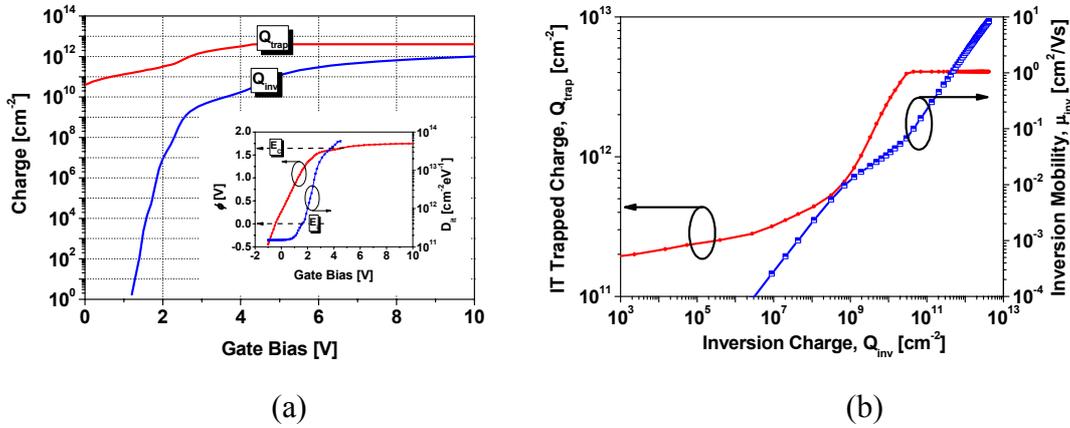
Fig. 7.2. (a) The inversion and the trapped charge computed from simulation results. The inset shows ϕ vs the gate voltage calculated for the main energy levels of the upper band gap. (b) Q_{trap} and μ_{inv} as function of the inversion charge to compute μ_{FE}.

To calculate the field-effect mobility, the μ_{inv} and Q_{trap} derivatives respect to Q_{inv} must be performed, once the inversion channel mobility is computed. Fig. 7.2(b) presents Q_{trap} and μ_{inv} as function of the inversion charge. Considering equation (7.19) and interface coulomb scattering as the main term in the inversion conduction modulation, only dQ_{trap} / dQ_{inv} derivative must be calculated, as inferred in (7.21). Field-effect mobility can then be computed as shown in Fig. 7.3(a). Some relevant trends can be aimed from this calculation. When the SiC surface gets degenerated (gate voltage higher than 4.5 V with our parametrization) the inversion and the field-effect

mobility are proportional. At the steepest slope region, in the weak inversion condition, the field-effect mobility can be approximated with

$$\mu_{FE} \approx (1+\beta)\frac{dQ_{inv}}{dQ_{trap}}\mu_{inv} \qquad (7.23)$$

since $dQ_{trap}/dQ_{inv} >> 1$, as illustrated in Fig. 7.3(b).
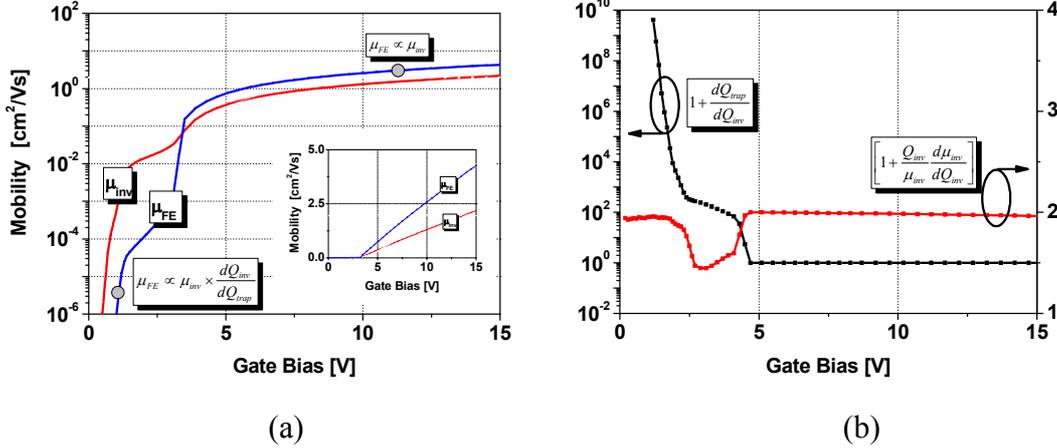
Fig. 7.3. (a) A comparison of the inversion and the field-effect mobility in linear and logarithmic scale, (b) The numerator and denominator of equation (7.18).

Therefore, the field-effect mobility at the lower gate voltages is strongly influenced by traps, yielding a field-effect mobility orders of magnitude lower than the inversion mobility, for the same gate bias. Nevertheless for higher gate voltages, inversion mobility and field-effect mobility are equivalent, independently of the traps present at the SiC/oxide interface. The variation of the carrier mobility with gate voltage (numerator of equation (7.18)) produces small changes in the evaluation of the field-effect mobility (25% maximum), before the SiC surface gets degenerated, as shown in Fig. 7.3(b).

Summarizing, interface traps from SiC surface oxidation will affect the experimental field-effect mobility in two different ways:

i)   The transport of carriers in the MOS interface is perturbed by the presence of charged interfacial traps that act as scattering terms in the inversion channel. This degradation effect is accounted by the Coulomb scattering in interface trap term in the inversion channel mobility, μ_{inv} (7.19).

ii) In a SiC MOSFET with a large density of interface states, μ_{FE} will not correspond to the true mobility μ_{inv}, due to the additional voltage required at the MOSFET gate to charge the interface traps, apart of the well known variation of the inversion carrier mobility also with gate voltage. These differences can be evaluated analytically with (7.18) and are specially relevant for the lower gate bias.

7.1.4. The charging and the scattering of electrons in interface traps

The effect of only charge trapping on interface traps in the channel mobility is analyzed with a set of simulations performed using the standard Lombardi mobility model without taking into account the trap Coulombic scattering. 2-D simulations with MEDICI program have been carried out in order to obtain a realistic electrical field at the surface E_{YS}, the inversion layer concentration n, and the Fermi potential ϕ_s as a function of the gate bias, as it is illustrated in Fig. 7.4 for E_{YS} regarding different traps spectra densities. The charge trapping modifies the electrical response at the interface as shown in the figure for the electric field.
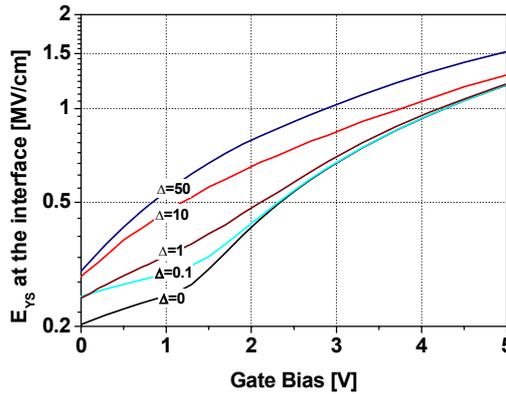
Fig. 7.4. Simulated electric field at the interface for SiO$_2$/4H-SiC MOSFET for different values of traps spectra density (Δ).

(a)	(b)
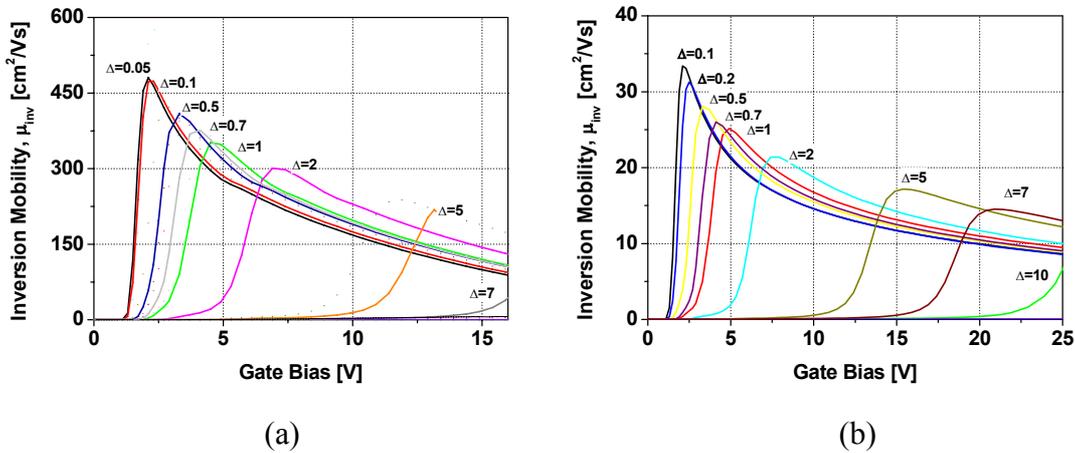
Fig. 7.5. Simulated mobility curves with Lombardi model without taking into account the scattering term. (a) default Si parameters (MEDICI), (b) Linewih *et al.* (Ref. 12) parameters for μ_{SR} and μ_{AC} terms.

The field effect peak mobility reduction under these conditions is mainly due to the stretch of the electric field induced by free carriers trapping. The threshold voltage is then influenced for such trapped charge, but the reduction on mobility is not due to the traps. The mobility peak reduction can be explained in terms of the other degradation terms following an universal behavior as function of gate bias once the channel is formed. Fig. 7.5 shows the simulated field effect mobility curves with different values for the parameters of conventional Lombardi scattering terms and taking into account

different profiles of interface states that trap electrons of the inversion layer (Δ). With the default Si values for the Lombardi model, a peak mobility as high as 500 cm^2/Vs is achieved for the lower interface traps densities.

Commonly, the acoustical-phonon scattering term plays a fundamental role in the peak inversion mobility reduction without considering the Coulomb scattering in interface traps, as evidenced in Fig. 7.6(a). The surface roughness scattering is negligible. In particular, according to the work of Linewih *et al.*[12] the experimental mobility curves were fitted primordially with the $C1$ coefficient of μ_{AC} as can be inferred from Fig. 7.6(b).

(a)   (b)
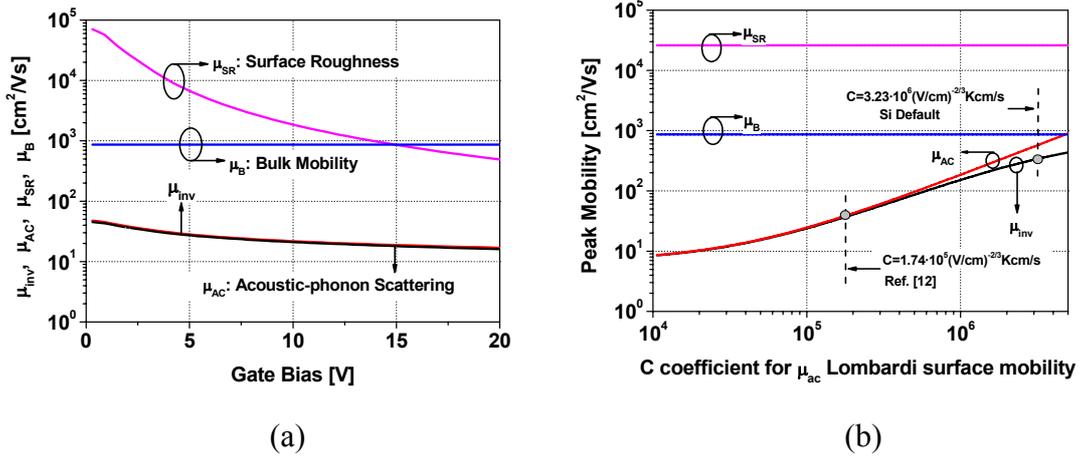
Fig. 7.6. (a) The value of the different Lombardi terms from Linewih *et al.* (Ref. 12) and Δ=0.1. (b) The influence of the $C1$ coefficient in the peak mobility reduction.

Nevertheless, it is not possible to reproduce the poor effective mobility obtained for 4H-SiC standard thermal oxidized MOSFETs without considering the Coulombic scattering term. The effect of Coulomb scattering in interface traps is so high (at room temperature) in a standard thermal oxidized 4H-SiC MOSFET that the field effect mobility can be described primarily using the μ_C term. Fig. 7.7 shows the effective channel inversion mobility for a thermal oxidized 4H-SiC MOSFET on the (0001) Si face (40 nm T-SiO$_2$) with channel length of L=4 μm and channel width of W=150 μm.
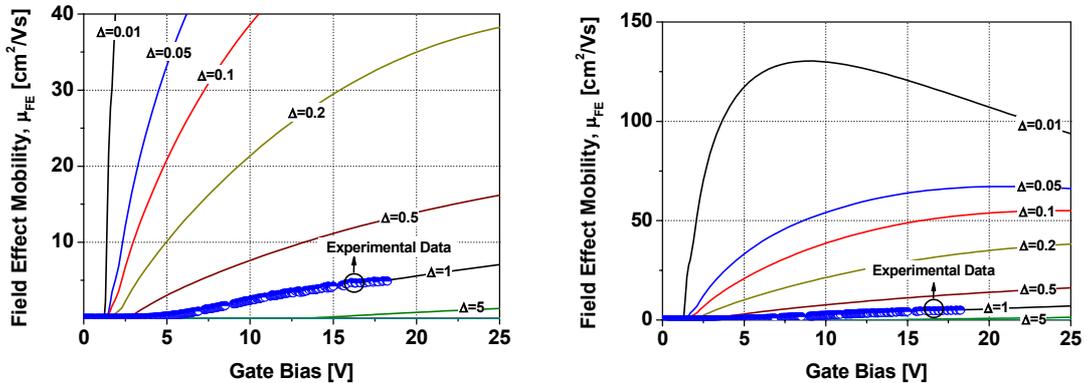
Fig. 7.7. Effective mobility versus gate voltage for an standard oxidized 4H-SiC thermal MOSFET. Solid line obtained from the proposed mobility model.

The solid lines correspond to the proposed model results obtained for Δ=0.01-10 according to equation (7.8). The parameters for the computation of the conventional Lombardi terms (Table VII.1) are derived from the work of Linewih *et al.*[12], except for the $C1$ parameter on μ_{AC} where it has been used the silicon default value (3.23×10^6 K·cm·s^{-1}(V/cm)$^{-2/3}$). N is maintained constant in all the simulations, and the parameter Δ is used to account for different D$_{it}$ profiles.

Recently, a reduction of interface-trap density (up to $\sim 10^{11}$ cm^{-2}eV^{-1} at $E_C - E_T$ =0.2 eV), increasing channel mobility ($\sim$48-120 cm^{2}V^{-1}s^{-1}) and a reliability has been obtained on thermally grown oxides in NO and N$_2$O ambients[20-22]. In some of these nitridated MOSFET subthreshold properties similar to Si devices have been reported[22] and thus, both Coulombic trap scattering and carrier trapping terms seems that can be neglected. Similar results have been obtained for MOSFETs fabricated on the (11$\bar{2}$0) faces instead of conventional (0001) Si faces[23]. However, simulation results have depicted that the Coulomb scattering in interface traps (standard thermal oxidation gate oxide) is so high that the other degradation factors can be neglected, at room temperature. Therefore, μ_C is the main mobility degradation term. The field effect mobility improvement reducing the interface traps density (reducing Δ) has also been verified with the proposed model.

7.1.5. The profile of interface traps dependence

In this section, the influence of close conduction band or deep (closer to intrinsic Fermi level) states on the field effect mobility will be analyzed. Different profiles of the interface traps density within the band-gap have been reported. Apart from the measurement method, this is due to the different oxidation processes or post-oxidation treatments. Several works have reported a decrease of the interface states density when approaching to the conduction band edge, specially with nitridation processes based on NO and N$_2$O [21,24-26], deposited oxides[27] or contaminated oxides[28,29]. In contrast, others work report on the decrease of D$_{it}$ specially in the shallow traps which energies are closer to the intrinsic Fermi level[30].

In order to account for this D$_{it}$ heterogeneous behavior, three different fitting functions have been used. Model named A in Fig. 7.8 (Eq.(7.24)), is the fitting function with a double exponential that takes into account the rapid increment of traps when approaching to the conduction band-gap. ξ_1, ξ_2, θ_1, θ_2, χ, λ and E_0 are fitting constants (see Table VII.2). This model has been used in the previous section. Model named B (Eq. (7.25)), is a simplification of the previous expressions that also considers the D$_{it}$ increase close to the band-gap edge. Model named C (Eq. (7.26)), is an idealization of the D$_{it}$ profile considering a constant value within the band-gap.

$$(A) \quad D_{it} = \begin{cases} \xi_1 + \xi_2 \exp\left(\dfrac{E_T - E_C}{\chi}\right) & E_T < E_0 \\ \\ \theta_1 + \theta_2 \exp\left(\dfrac{E_T - E_C}{\lambda}\right) & E_T > E_0 \end{cases} \qquad (7.24)$$

$$(B) \quad D_{it} = \xi_1 + \xi_2 \exp\left(\frac{E_T - E_C}{\chi}\right) \tag{7.25}$$

$$(C) \quad D_{it} = \xi_1 \tag{7.26}$$
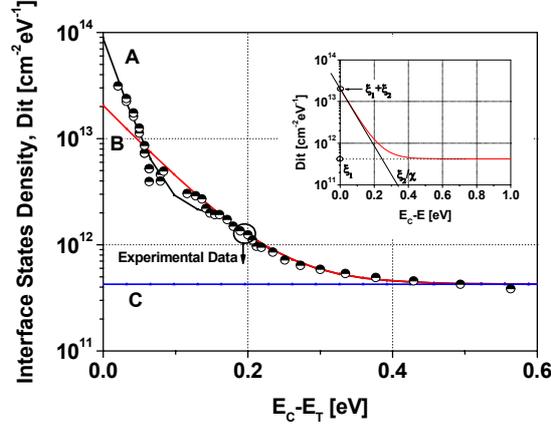
Fig. 7.8. The D$_{it}$ experimental profile with the three proposed fitting functions. In the inset: The schematic profile of an arbitrary interface traps profile near the conduction band edge.

This three fitting functions have been chosen to quantify if the interface traps close the conduction band are really in the origin of the field effect mobility degradation, or on the contrary are the states lying close to the mid-gap. Therefore, model name C is an idealization of a MOS interface without the rapid increase of interface states close to the conduction band, conventionally reported in SiC/SiO$_2$ interfaces. As shown in the previous section, the experimental field effect mobility for a thermal oxidized (gate oxide) 4H-SiC MOSFET transistor using a standard oxidation process is well reproduced in weak inversion and strong inversion range, as it can be inferred from the inset of Fig. 7.9, using model A.
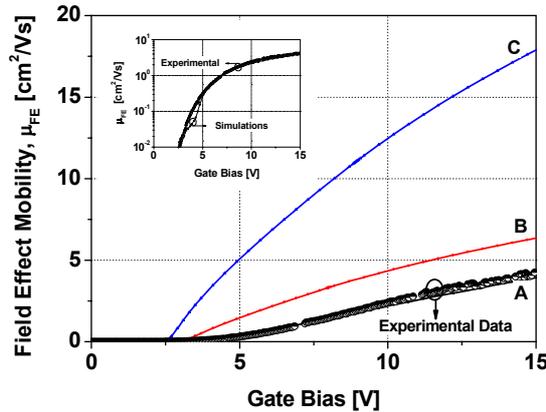
Fig. 7.9. Measured field effect mobility (μ_{FE}) versus gate bias. The calculated gate bias dependence according to the proposed D$_{it}$ profiles (A, B and C) are also shown. In the inset: The fit of the experimental mobility using function A in μ_C calculation.

The traps Coulomb scattering numerical computation using the 2-D simulations results allows determining the inversion and the trapped charge as a function of the gate bias. As it can be derived from Fig. 7.10, the inversion charge in the strong inversion range, for the interface trap density experimentally determined (A) or lower (B, C), is almost independent of the charge trapping. In contrast, the charge trapping is strongly dependent on the D$_{it}$ profile within the band-gap, specially in the strong inversion range. Both, the D$_{it}$ shape and value affects the trapped charge in interfacial states. The dramatically effect on the mobility reduction observed in 4H-SiC devices is explained and quantified considering this simplified model. A reduction of the high density of traps near the conduction band is traduced in an increment of the field effect mobility and a shift of the threshold voltage (Fig. 7.8 and Fig. 7.9).
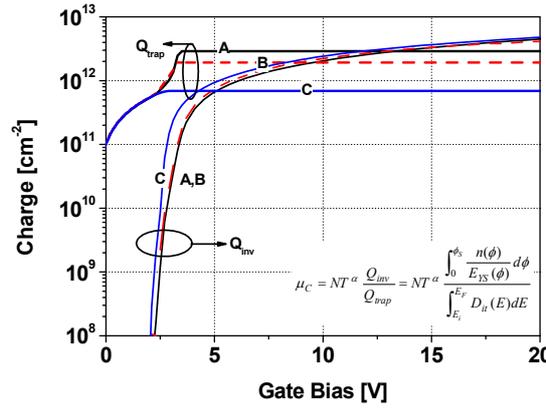
Fig. 7.10. The inversion charge and the trapped charge computed from the simulation results for the three considered interfacial traps profile functions.

The inset of Fig. 7.8 shows a typical spectrum of the interface traps in the upper half of the band-gap. This profile can be schematically described with three magnitudes that can be experimentally derived, the mid gap interface trap density, ξ_1, $\xi_1 + \xi_2$ that represents the interface trap density when the Fermi level reaches the conduction band and the slope of the rapid increment toward the conduction band edge, ξ_2 / χ. This slope has been determined developing in Taylor series the expression named B (or A) when it approaches to the conduction band edge.

$$D_{it} \approx \left(\xi_1 + \xi_2\right) + \frac{\xi_2}{\chi}\left(E_T - E_C\right) \quad E_T - E_C \to 0 \qquad (7.27)$$

The trapped charge is determined integrating D$_{it}$. In the strong inversion range (in our case for gate voltages higher than ~5 V) and taking into account that the Fermi level is above the conduction band edge (E_C), the trapped charge can be considered as a constant value:

$$Q_{trap} = \xi_1\left(E_C - E_i\right) + \xi_2 \chi \qquad (7.28)$$

where E_i is the intrinsic Fermi energy. In such conditions, a set of simulations have been carried out in order to analyze the effect of the mid gap density of states along with the increase towards the band edge. The main interest of this approach lies in that from a simple MOS capacitor electrical measurements, it is possible to estimate the

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field effect mobility for MOSFET with high density of interface states in the interface. MOS fabrication is much simpler and cost-effective than the MOSFET fabrication, especially in SiC substrates. Indeed, there are few groups in Europe that actually fabricate SiC MOSFET devices. Therefore, this computational solution allows estimate the MOSFET mobility performances (the really interesting parameter for engineers and the industry) from the MOS capacitor, that is simply an indicator of the quality of the MOS interface. Fig. 7.11 presents the results obtained taking into account a fixed value of χ (varying this magnitude does not through significant qualitatively differences). The rapid increase of D$_{it}$ when approaching the conduction band edge is accounted with the parameter Γ, that is $\xi_2 = \Gamma \cdot \xi_1$.
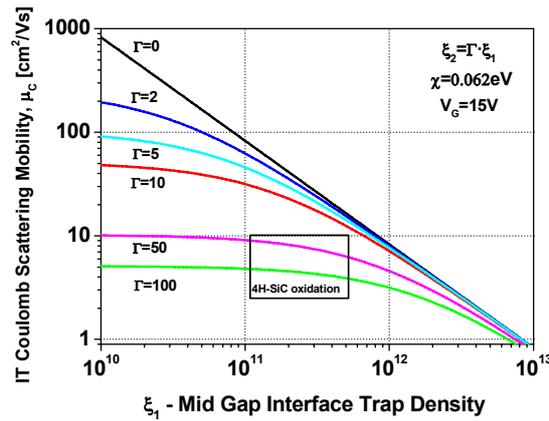
Fig. 7.11. Computed interface traps (IT) Coulomb scattering mobility versus mid gap interface trap density map in strong inversion.

The higher Coulomb scattering mobility is obtained when the interface traps near the conduction band are small when compared with the mid gap interface trap density (Γ small). Analogously, the lower the mid gap interface trap density, the higher μ_C will be. It must also be stressed that the enhancement of the channel mobility is not only linked to the removal of the interface traps near the conduction band, but the reduction of interface traps within the band-gap as well. For example, in our standard thermal oxidation, the removal of near conduction band interface traps, that is, model named C, yield a mobility improvement of *only* a factor ~3 (Fig. 7.9). Hence, the improvement is significant, but the reduction of the mid gap interface trap density is mandatory, since the problem of Coulomb scattering still remains, and the channel mobility is still very far from the value predicted from bulk mobility (950 cm^2/Vs).

Summarizing, with this model is possible to perform a map of the traps Coulomb scattering mobility (or field effect mobility if all Lombardi terms are taken into account) as a function of the mid gap interface trap density, in the upper half of the band-gap, and taking into account the rapid increase of D$_{it}$ when approaching to the conduction bad. The square named 4H-SiC oxidation in Fig. 7.11 represents the experimental (and commonly reported) D$_{it}$ and mobilities values of 4H-SiC MOSFET devices with standard dry oxidized gate.

7.1.6. Substrate impurity concentration dependence

The 4H-SiC MOSFET field effect mobility dependence on the substrate impurity concentration (N_A) has been studied in several works[31,32]. This is an important issue since the low mobility obtained in SiC devices implies a large on-resistance. In order to reduce the on-resistance, the channel length reduction could be an attractive solution. However, when the channel length is reduced the substrate impurity concentration must be increased in order to avoid short channel effects.

We have applied our model to study the field effect mobility properties of 4H-SiC MOSFETs devices as function of the substrate impurity concentration. Simulations have been performed varying the 4H-SiC MOSFET impurity concentration in the range 5×10^{15}-1×10^{18} cm^{-3}, and considering the model named A for D$_{it}$ as the best fit to the experimental mobility characteristics with $N_A = 1 \times 10^{16}$ cm^{-3} and $T = 300$ K.
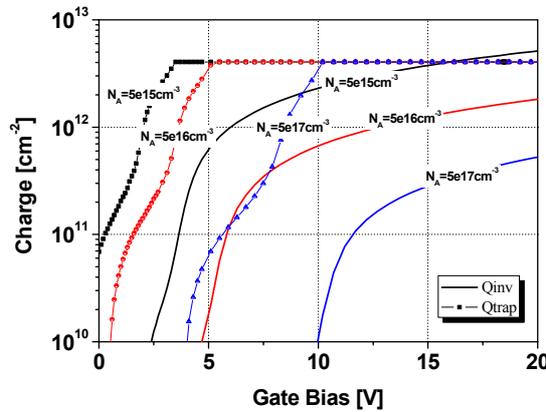
Fig. 7.12. The inversion charge and the trapped charge versus the gate bias computed from the simulation results for different substrate impurity concentration.

Fig. 7.12 shows the inversion charge and the charge trapped simulated for different values of the substrate impurity concentration. The threshold voltage is shifted to higher gate voltages as N_A is increased, as it can be inferred for the trapped charge and the inversion charge behavior. In spite of the voltage shift, the trapped charge in interface states remains unchanged. However, the inversion charge is reduced as the substrate impurity concentration is increased. This last effect could be attributed to the electric field increase at the interface when the substrate doping is increased[33] (see Eq. (7.3)). Hence, taking into account the interfacial traps Coulomb scattering it is possible explain a field effect mobility reduction with the N_A increase without considering an additional degradation on the interfacial properties.

The computed field effect mobility is showed in Fig. 7.13. Again, if model A is considered for the D$_{it}$ profile, the effect of the interface traps Coulomb scattering is so high that dominates the transconductance behavior of the device and then, the approximation $\mu_{FE} \sim \mu_C$ seems to be reasonable. The inclusion of all Lombardi mobility degradation terms does not through significant differences in the μ_{FE} computation. The higher the impurity concentration of the substrate, the lower the field effect mobility will be. The MOSFET threshold voltage also increases when the impurity substrate concentration increases as it can be also derived from the inset of Fig. 7.13. The mobility variation as a function of substrate impurity concentration is shown in Fig.

7.14. The abrupt decrease for the mobility at 10 V of gate bias is due to the threshold voltage shift.
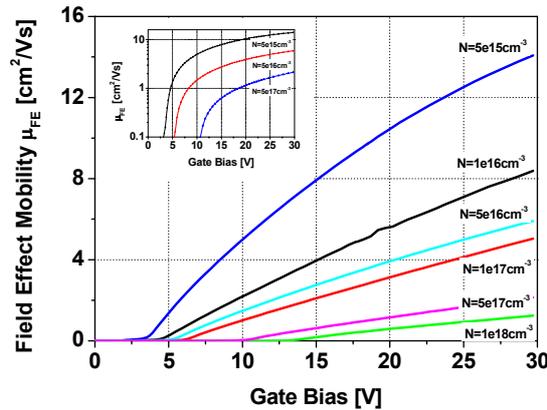
Fig. 7.13. The computed field effect mobility versus the gate bias for different substrate impurity concentration values. In the inset: the logarithmic scale shows the variation on threshold voltage.
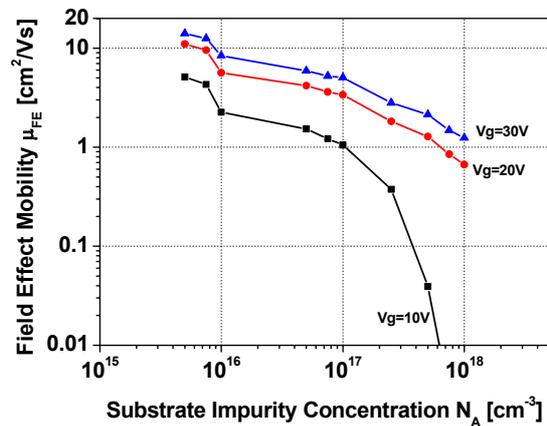
Fig. 7.14. The computed field effect mobility versus the substrate impurity concentration for three gate bias in inversion regime.

The field effect peak mobility degradation with increasing N_A is a well known effect in Si devices and it is incorporated in the mobility models, such as the Lombardi model with an impurity scattering term[16]. When the substrate doping level increases, the probability of scattering in the additional impurities centers increases as well. This mechanism, generally becomes relevant for high doping levels of the substrate. However, when the interface trap density is as high as in thermal 4H-SiC oxidation, the mobility is (almost) totally modulated by the Coulomb scattering (at room temperature). In this case, the mobility degradation is not due to an additional scattering in the impurity charge but to the reduction in the inversion charge. Therefore, the Coulomb scattering of charged interface traps seems to produce the undesirable effect of reducing the field mobility when the substrate impurity concentration is increased.

7.1.7. Temperature dependence

Sah *et al.*[34] have shown that, assuming a fixed charge distribution of ionized traps on the interface, neglecting the free carrier screening effects and treating the random spatial fluctuations of charge density as a perturbation, yields a linear temperature dependence with the scattering of ionized electron trapped in interface states. Apart of this, both Q_{trap} and Q_{inv} are temperature dependent. Thus, the temperature dependence of the Coulomb scattering by ionized interface traps will be a complex temperature function,

$$\mu_C = NT^\alpha \frac{Q_{inv}}{Q_{trap}} = NT^\alpha f(T) \quad (7.29)$$

experimentally, some works on the literature have reported an exponential temperature dependence[23],

$$\mu_{FE} = \zeta T^\gamma \quad (7.30)$$

assuming that the interface traps Coulomb scattering is the main degradation factor (at least at room temperature) and performing some algebraic operation the following expression can be derived for the temperature coefficient (α).

$$\alpha = \gamma + \frac{\ln\left[\dfrac{\zeta}{Nf(T)}\right]}{\ln T} \quad (7.31)$$

2D simulations have been performed varying the temperature in order to study its dependence. Function name A has been used to describe the interface traps profile and a substrate impurity concentration of $N_A = 1 \times 10^{16}$ cm^{-3} has been considered. Yano *et al.*[23] reported a value of $\gamma = 2.6$ ($\zeta \sim 2 \times 10^{-6}$ cm^2/V·s·K$^\gamma$) that has been used to estimate the temperature coefficient, α. Fig. 7.15 shows the values derived for α considering different temperatures.
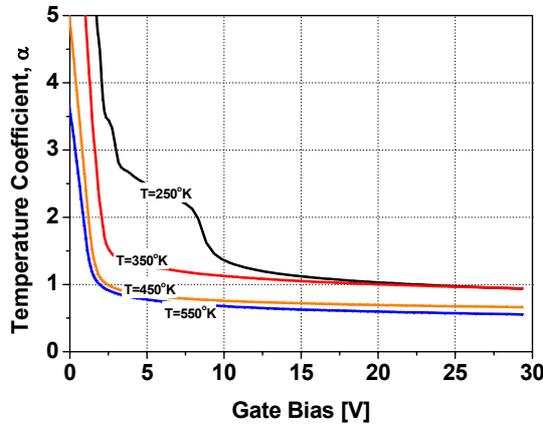
Fig. 7.15. Temperature coefficient (α) as a function of the gate bias simulated for different temperatures.

In the strong inversion region, α seems to be in the range 0.5-1. At room temperature it is reasonable to consider $\alpha \sim 1$. As a simplification, $\alpha \sim 1$ will be used in the mobility temperature dependence estimation further on.

The inversion charge and the trapped charge are presented in Fig. 7.16 for different temperatures. The inversion charge is increased when the temperature augments, since the free electron concentration is increased (and the intrinsic concentration as well). In the same way, the trapped charge in interface states is significantly reduced when the temperature is increased. This last situation is due to the Fermi level shift towards the intrinsic Fermi level along with an additional band-gap narrowing when the temperature is increased. For the same reason, the threshold voltage is also reduced when the temperature is increased. The combination of the inversion charge increase and trapped charge reduction, produces a dramatic reduction of the traps Coulomb scattering effect and a drastic increase of the Coulomb mobility when the temperature is increased, as it is shown in Fig.7.17.
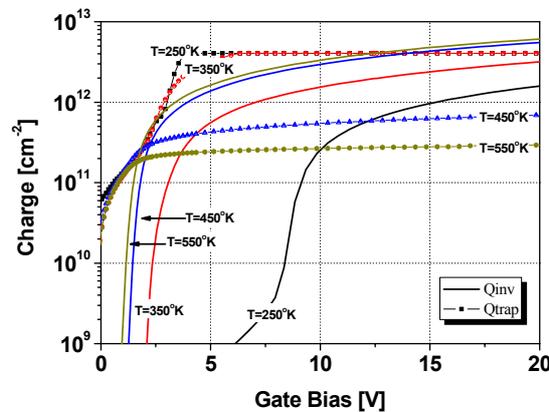
Fig. 7.16. The inversion charge and the trapped charge computed from the simulation results for different temperatures.
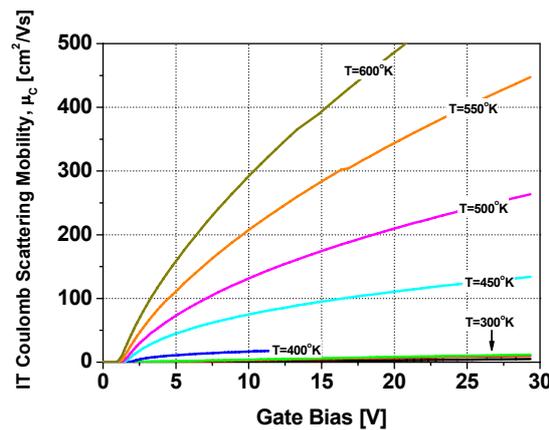
Fig. 7.17. The interface traps (IT) Coulomb scattering mobility versus the gate bias simulated for different temperatures.

However, some of the other mobility degradation mechanisms detected on MOS gated devices on Si or SiC are also sensitive to a temperature variation. In particular, the acoustical phonon scattering mobility term presents a $\sim T^{-3}$ temperature dependence[6]. Hence, the scattering due to acoustical phonon increases when the temperature is increased. For this reason, the mobility observed in thermally oxidized 4H-SiC

MOSFETs must be a trade-off of these two effects. Fig.7.18 shows the computed field effect mobility taking into account all the Lombardi terms (μ_B, μ_{SR}, μ_{AC} and μ_C) varying the temperature. The parameters for the computation of the three first terms are derived from the work of Linewih *et al.*[12] except for the $C1$ parameter where it has been used the silicon default value (3.23×10^6 K·cm·s^{-1}(V/cm)$^{-2/3}$). Corroborating that, when the interface traps are reduced drastically, using some NO and N$_2$O treatments or other SiC crystal orientation the field effect mobility seems to tend to a decrease with the increase of the temperature[23,35,36].
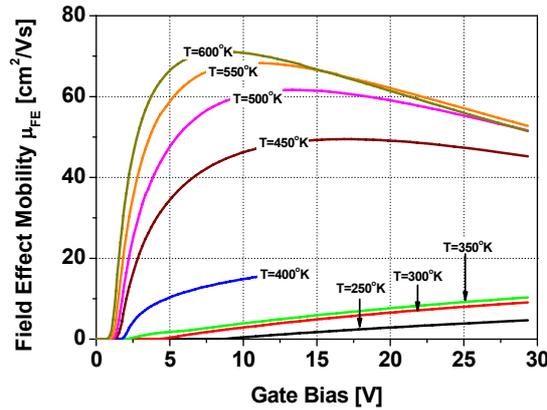
Fig. 7.18. The simulated field effect mobility versus the gate bias for different temperature values.

The mobility behavior of a 4H-SiC device with temperature is directly related with the interface traps density. The proposed model agrees with the temperature behavior commonly reported. If the density of traps is sufficiently high to consider the traps Coulomb scattering term the dominant effect (such as in an standard O$_2$ (0001) Si-face 4H-SiC oxidation), we will obtain a positive behavior with the temperature. On the contrary, if D$_{it}$ is efficiently reduced a negative behavior with the temperature (Si-like behavior) will be obtained.

7.2. Anomalous mobility enhancement on 4H-SiC MOSFETS due to gate leakage inversion carriers injection

It has been presented a mobility expression based on the Lombardi mobility model that accounts for interface trap scattering and can be implemented in 2D electrical simulators. The weak and strong inversion characteristics of conventional 4H-SiC MOSFETs can be well fitted using this model. Anomalous high mobilities have been extracted in 4H-SiC MOSFETs with thermal SiO$_2$ (T-SiO$_2$) (~100 cm^{2}V^{-1}s^{-1}) or oxidized Ta$_2$Si high-*k* dielectric (O-Ta$_2$Si) (~50 cm^{2}V^{-1}s^{-1}) as gate insulators in the strong inversion regime. The interface states density (D$_{it}$) has not been particularly reduced in neither T-SiO$_2$ nor O-Ta$_2$Si MOSFETs. This anomalous mobility enhancement is explained in terms of the Coulomb scattering reduction and quantified using the proposed model. The increase of free carriers in the inversion layer induced by the gate leakage diminishes the effect of the interface trap Coulomb scattering.

7.2.1. Anomalous mobility enhancement

When acoustic-phonon or surface scattering are the dominant mobility degradation factors, the device presents a silicon-like subthreshold characteristics with a peak mobility close to the threshold voltage and then, the effective mobility reduces when increasing the gate voltage (Fig. 7.5). On the contrary, when the dominant degradation factor is assigned to a Coulombic scattering process, the mobility does not diminishes increasing the gate voltage, at least not in a such pronounced way (Fig. 7.7). In this last situation, the mobility becomes higher increasing the gate bias since the inversion charge (n) increases. If the gate bias is sufficiently high, in strong inversion mode, the semiconductor becomes degenerate and the Fermi level reaches the conduction band. Thus, the charge trap Q_{trap} reaches its maximum value, remaining constant for higher gate biases. Hence, if no other scattering effects occur, the mobility increases up to the gate breakdown.

The anomalous mobility increase seems to arise in these last situations if an additional inversion charge appears. The paradigm of this effect has been routinely observed on 4H-SiC MOSFETs fabricated with oxidized Ta$_2$Si as gate material[37], as explained in *Chapter VI*. The gate of O-Ta$_2$Si/4H-SiC MOSFETs is composed of a stacked structure[38] that consists of a SiO$_2$-like interfacial layer and amorphous SiO$_2$ (a-SiO$_2$) combined with crystalline Ta$_2$O$_5$ (δ-Ta$_2$O$_5$) high-*k* mixture with a global dielectric constant of ε_r ~20. The interfacial layer forms a carrier barrier at relatively low gate voltages and the leakage current is negligible. When the thin interfacial layer breaks down, the electrons (positive gate bias) are injected to the upper layer, and experiment Poole-Frenkel conduction mechanism across the crystalline δ-Ta$_2$O$_5$ layers. In that situation, more electrons are required from the source of the device to compensate the increasing leakage current. Considering that the Fermi level of the semiconductor is above the conduction band, Q_{trap} is a constant value. The inversion charge at the interface is thus increased and the mobility drastically rises. The schematic of this situation is presented in Fig. 7.19.
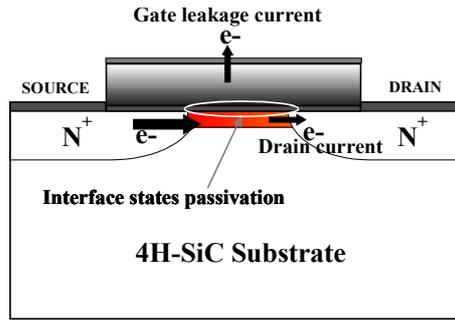
Fig. 7.19. Schematic of the anomalous mobility increase due to *controlled* gate leakage current.

Fig. 7.20 shows the mobility versus gate voltage characteristic of an O-Ta$_2$Si/4H-SiC MOSFET. The leakage current density is presented in the inset. The drain current of the O-Ta$_2$Si/4H-SiC MOSFET is shown in Fig. 7.21.
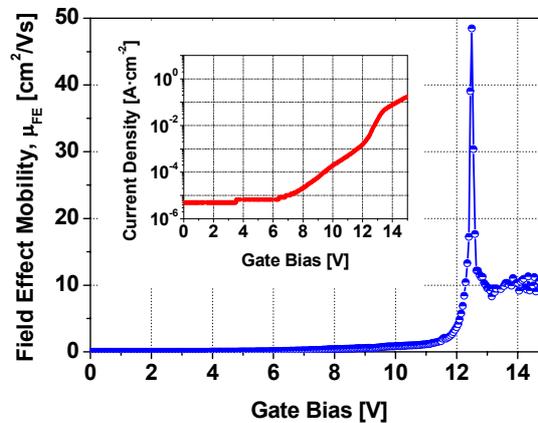
Fig. 7.20. Anomalous improved effective mobility versus gate voltage for an oxidized Ta$_2$Si/4H-SiC MOSFET. The gate leakage current density is presented in the inset.
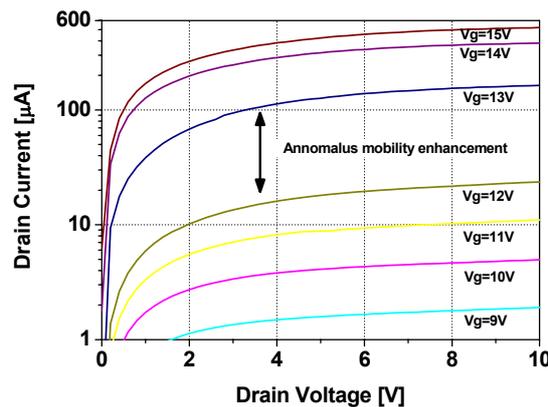
Fig. 7.21. Drain characteristics of an O-Ta$_2$Si/4H-SiC MOSFET experimenting the anomalous mobility increase. Correct subtreshold, inversion and saturation characteristics are obtained in the 8-15V gate bias range.

The device is normally off with a threshold voltage of ~4 V. These devices exhibit adequate subthreshold, saturation and drive characteristics up to the leakage current limit of 10^{-1} Acm^{-2}, that is reached at a gate bias of 15 V. A mobility peak of 50

cm^{2}V^{-1}s^{-1} has been measured on these devices. Once the gate leakage current density reaches the current limit, the device no longer behaves correctly. The anomalous mobility increase is closely related with the leakage current, and also with the gate breakdown mechanism. The observed interfacial SiO$_2$ tunnel combined with δ-Ta$_2$O$_5$ Poole-Frenkel mechanisms seems to be a sufficiently low abrupt transition in gate breakdown to obtain an effective "passivation" of the interface traps. Nevertheless, this effect has also been observed on thermal oxidized 4H-SiC structures with a breakdown leakage current sufficiently smooth. Fig. 7.22 shows the mobility versus gate voltage of an T-SiO$_2$/4H-SiC MOSFET. In this case the peak mobility reaches 100 cm^{2}V^{-1}s^{-1}.
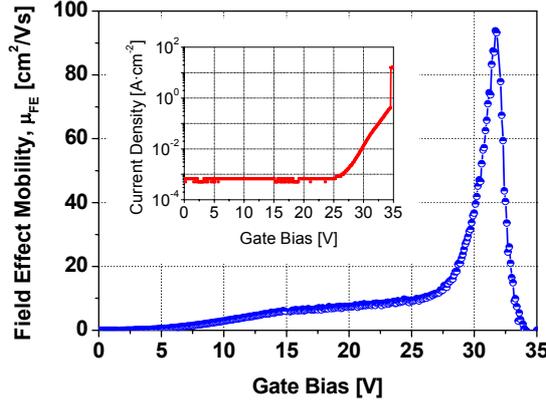
Fig. 7.22. Anomalous improved effective mobility versus gate voltage for an standard oxidized 4H-SiC thermal MOSFET (T-SiO$_2$/4H-SiC). The gate current leakage density is presented in the inset.

The additional free carrier concentration in the inversion layer contributing to the effective reduction of trap scattering can be evaluated using the Coulomb scattering term proposed in the mobility model.

$$\mu_{FE} \approx \mu_C = NT^\alpha \frac{\int_0^{\phi_S} \frac{n_{TOTAL}(\phi)}{E_{YS}(\phi)} d\phi}{\int_{E_i}^{E_F} D_{it}(E) dE} \quad (7.32)$$

We assume that the semiconductor gets degenerated and the other potential degradation effects are irrelevant small when compared with the Coulombic scattering. In such conditions, the additional amount of free carriers can be expressed by:

$$n_{TOTAL}(\phi) = n(\phi) + \Delta n(\phi) \quad (7.33)$$

performing some algebraic operations and deriving respect the Fermi potential the following expression can be obtained:

$$\Delta n(\phi) = E_{YS}(\phi) \frac{\int_{E_i}^{E_F} D_{it}(E) dE}{NT^\alpha} \frac{\partial \mu_{FE}}{\partial \phi} - n(\phi) \quad (7.34)$$

The additional inversion carrier concentration can be evaluated with equation (7.34). The experimental inferred effective mobility is expressed as a function of the

calculated Fermi potential for a given gate bias, in order to compute the additional amount of inversion charge. When the additional inversion carrier concentration is small, the model reproduces the measured field effect mobility, and thus $\Delta n / n \sim 0$. This is the situation of a conventional MOSFET with no leakage gate. Fig. 7.23 shows the modeled and measured field effect mobility for the T-SiO$_2$ and O-Ta$_2$Si/4H-SiC MOSFETs.
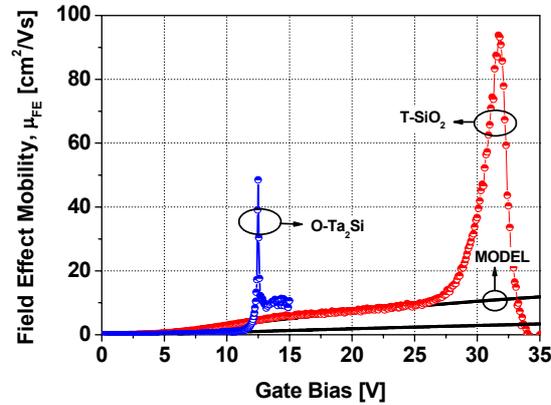
Fig. 7.23. The field effect mobility measured and modeled for the T-SiO$_2$ and O-Ta$_2$Si/4H-SiC MOSFETs. The anomalous mobility enhancement is achieved at strong inversion range.

Fig. 7.24 shows the additional inversion charge supplied by the controlled gate leakage current ($\Delta n / n$) as a function of the gate bias experimentally derived for O-Ta$_2$Si/4H-SiC and T-SiO$_2$/4H-SiC MOSFETs. Once the anomalous mobility increase is detected on the gate of the device, the amount of free carriers on the inversion layer progressively increases (between 10^1-10^2 times the inversion layer concentration), up to the gate breakdown.
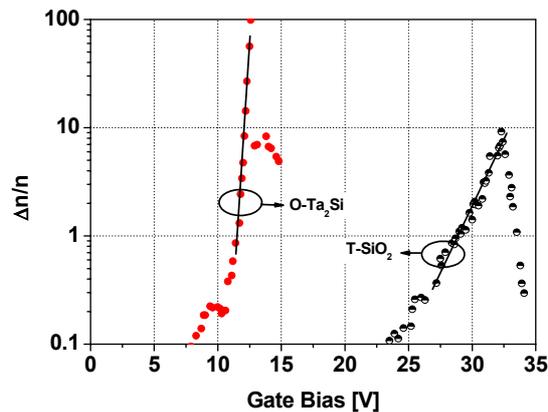
Fig. 7.24. The extracted additional inversion carrier concentration derived from the analytical expression proposed (Eq. (15)) for T-SiO$_2$ and O-Ta$_2$Si/4H-SiC MOSFETs.

In a similar way, the improvement of the drain to source current when the anomalous mobility improvement is present (showed in Fig. 7.21), can be evaluated with a combination of the inversion charge increase along with a reduction of the interfacial traps Coulomb scattering (also due to the inversion charge increase). The drain to source current with the additional inversion charge can be computed combining (7.12), (7.19) and (7.33)

$$I_{DS} = \frac{W}{L} q \mu_{inv} |Q_{inv}| V_{DS} \approx \frac{W}{L} q \frac{NT^{\alpha}}{Q_{trap}} V_{DS} \left[\int_0^{\phi_s} \frac{n(\phi)}{E_{YS}(\phi)} \left(1 + \frac{\Delta n(\phi)}{n(\phi)} \right) d\phi \right]^2 \qquad (7.35)$$

where the same assumptions (high interfacial trap scattering and strong inversion gate condition) contemplated for the definition of equation (7.34) have been considered.

Summarizing, the anomalous mobility increase arises when the following combination of factors occur:
(1) High density of interface traps to allow an appreciable Coulomb scattering of trapped charges, (2) The rest of mobility degradation contributions must be sufficiently small in order to not limit the anomalous potential increase on the mobility, (3) The gate leakage/gate current breakdown must be sufficiently smooth for an effective increase of the inversion layer charge. Due to its high density of defects, almost all oxidation procedures and dielectrics on 4H-SiC accomplish requirement (1). Requirement (3) is also compatible with most of the high-*k* dielectrics, including oxidized Ta$_2$Si. Condition (2) seems to be more difficult to predict because the mobility degradation mechanisms and their link with technological processes are not completely understood.

7.3. Conclusions

One of the keys of the success of the Si based MOS technology is the excellent interfacial characteristics between the silicon and its native thermal oxide. In the Si/SiO$_2$ interface, the oxide and interfacial traps can be effectively erased with adequate post-oxidation annealing processes and the traps Coulomb scattering can be generally neglected. Hence, the traditional mobility model for Si devices, such as the usually incorporated in commercial 2-D simulators, does not account for the effect of a large density of interfacial states on the channel conduction. The high density of interface states plays a fundamental role in the poor field effect mobility values extracted on SiC MOSFETs. In this chapter, a mobility expression, based on the Lombardi mobility model, has been developed including this scattering effect.

A compact model, based on the well established semi-empirical Lombardi mobility model, has been proposed to fit 4H-SiC MOS gated field effect on-state characteristics. The model takes into account acoustic-phonon scattering, surface roughness scattering and interface traps Coulomb scattering. The interface traps Coulomb scattering term is computed taking into account the inversion charge and the trapped charge. This model can be combined with 1D, 2D simulation packages. Using 2D MEDICI$^{®}$ simulations and the proposed model, the experimental mobility of 4H-SiC devices has been fitted with a good agreement. Simulations have been performed in order to study the influence of the interface traps density profile, the substrate impurity concentration and the temperature. The D$_{it}$ rapid increase towards the conduction band and the mid-gap interface states density have been considered in order to evaluate the mobility degradation. The increase of the substrate impurity concentration implies a reduction in the inversion charge and thus, a reduction in the interface traps Coulomb scattering mobility. The threshold voltage is also shifted. The temperature affects both the inversion charge and the trapped charge. The interface traps Coulomb scattering is reduced when the temperature is increased. However, other degradation factors such as

the acoustic phonon scattering are magnified when the temperature is increased. The total mobility when the temperature is increased results in a trade-off between these two effects. Hence, the proposed model not only fits accurately the experimental mobility but reproduces the behavior commonly reported for thermally grown gate oxides 4H-SiC MOSFETs for D$_{it}$ profile, substrate impurity concentration and temperature.

The Coulomb scattering term has been used to explain an anomalous mobility enhancement observed under strong inversion conditions in 4H-SiC MOSFETS fabricated employing thermal SiO$_2$ (T-SiO$_2$) and oxidized Ta$_2$Si (O-Ta$_2$Si) high-k dielectric as gate material. High peak mobilities up to 50 cm^2/Vs and 100 cm^2/Vs have been obtained for O-Ta$_2$Si/4H-SiC and T-SiO$_2$/4H-SiC MOSFETs, respectively. The interface states density has not been particularly reduced in neither T-SiO$_2$ nor O-Ta$_2$Si MOSFETs. This anomalous mobility enhancement has been explained in terms of effective inversion charge increase due to a carrier injection through the gate. This increase of inversion charge provokes the reduction of the mobility scattering effects. An analytical expression is proposed to evaluate the additional free carrier increase. This effect is routinely observed due the Poole-Frenkel mechanism through the gate of the device on O-Ta$_2$Si/4H-SiC MOSFETs. In T-SiO$_2$/4H-SiC MOSFETs, the observation of this effect seems to be strongly related with the fabrication process. The correct behavior of the device is not lost during the anomalous mobility enhancement until to the gate current limit density is reached.

References

[1] E. Arnold, and D. Alok, *IEEE Trans. Elect. Dev.* **48**, 1870, (2001).

[2] S. Harada, R. Kosugi, J. Senzaki, W-J. Cho, K. Fukuda, and K. Arai, *J. Appl. Phys.* **91**, 1568, (2002).

[3] S. K. Powell, N. Goldsman, J. M. McGarrity, J. Bernstein, C. J. Scozzie, and A. Lelis, *J. Appl. Phys,* **92**, 4053, (2002).

[4] J. S. Kang, D. K. Schroder, and A. R. Alvarez, *Solid-State Electron.* **32**, 679, (1989).

[5] R. Schörner, P. Friedrichs, D. Peters, and D. Stephani, *IEEE Electron Device Lett.* **20**, 241, (1999).

[6] C. Lombardi, S. Manzini, A. Saporto, and M. Vanzi, *IEEE Trans. on Computer-Aided Design* **7**, 1164, (1998).

[7] E. Arnold, *IEEE Trans. Elect. Dev.* **46**, 497, (1999).

[8] E. H. Nicollian, and J. R. Brews, *MOS Physics and Technology*, Wiley, New York, (1982).

[9] D. M. Caughey, and R. E. Thomas, *Proc. IEEE*, **52**, 2192, (1967).

[10] M. Roschke, and F. Schwierz, *IEEE Trans. Elect. Dev.* **48**, 1442, (2001).

[11] M. Ruff, H. Mitlehner, and R. Helbig, *IEEE Trans. Elect. Dev.* **41**, 1040, (1994).

[12] H. Linewih, S. Dimitrijev, and K. Y. Cheong, *Microelectron. Reliab.,* **43**, 405, (2003).

[13] A. Hartstein, T. H. Ning, and A. B. Fowler, *Surface Sci.,* **58**, 178, (1982).

[14] J. R. LaRoche, J. Kim, J. W. Johnson, B. Luo, B. S. Kang, R. Mehandru, Y. Irokawa, S. J. Pearton, G. Chung, and F. Ren, *Electrochem. and Solid-State Lett.* **7**, G21, (2004).

[15] A. Kumar, N. Kaushik, S. Haldar, M. Gupta, and R. S. Gupta, *Microelectron. Engineering,* **65**, 416, (2003).

[16] Technology Modeling Associates, Inc., *TMA, MEDICI User's Manual* 2002, Ver. 2.2

[17] V. V. Afanas'ev, M. Bassler, G. Pensl, and M. Schulz, *Phys. Stat. Sol.(a)* **162**, 321, (1997).

[18] N. S. Saks, S. S. Mani, and A. K. Agarwal, *Mater. Sci. Forum* **338-342**, 1113, (2000).

[19] C. Raynaud, *J. Appl. Phys* **88**, 424, (2000).

[20] G. Gudjónsson, H. Ö. Ólafsson, and E. Ö. Sveinbjörsson, *Mater. Sci. Forum* **457-460**, 1425, (2004).

[21] M. K. Das, *Mater. Sci. Forum* **457-460**, 1275, (2004).

[22] R. Schörner, P. Friedrichs, D. Peters, D. Stephani, S. Dimitrijev, and P. Jamet, *Appl. Phys. Lett.* **80**, 4253, (2002).

[23] H. Yano, T. Hirao, T. Kimoto, and H. Matsunami, *Appl. Phys. Lett.,* **78**, 374, (2001).

[24] K. -C. Chang, L. M. Porter, J. Bentley, C. -Y. Lu, and J. Cooper, Jr., *J. Appl. Phys.* **95**, 8252 (2004).

[25] K. Y. Cheong, S. Dimitrijev, J. Han, and B. Harrison, *J. Appl. Phys.* **93**, 5682 (2003).

[26] V. V. Afanas'ev, A. Stesmans, F. Ciobanu, G. Pensl, K. Y. Cheong, and S. Dimitrijev, *Appl. Phys. Lett.,* **82**, 568, (2003).

[27] G. Y. Chung, J. R. Williams, T. Isaacs-Smith, F. Ren, K. McDonald, and L. C. Feldman, *Appl. Phys. Lett.,* **81**, 4266, (2002).

[28] E.Ö.Sveinbjörnsson, H. Ö. Ólafsson, G. Gudjónsson, F.Allerstam, P.-Å. Nilsson, M. Syväjärvi, R. Yakimova, C. Hallin, T. Rödle, and R. Jos, *Mater. Sci. Forum* **483-485**, 841, (2005).

[29] D.Alok, E. Arnold, R. Egloff, and S. Mukherjee: US Patent No. 6,559,068 (2003).

[30]   A. Pérez-Tomás, D. Tournier, P. Godignon, N. Mestres, J. Millán, *Mater. Sci. Forum* **483-485**, 673, (2005).

[31]   G. Gudjónsson, H.Ö. Ólafsson, F. Allerstam, P.-Å. Nilsson, E.Ö. Sveinbjörnsson, T. Rödle, and R. Jos, *Mater. Sci. Forum* **483-485**, 833, (2005).

[32]   T. Hatakeyama, T. Watanabe, J. Senzaki, M. Kato, K. Fukuda, T. Shinohe, and K. Arai, Mater. *Sci. Forum* **483-485**, 829, (2005).

[33]   S. C. Sun and J. D. Plummer, *IEEE J. Solid-State Circuits*, **SC-15**, 562 (1980).

[34]   C. T. Sah, T. H. Ning, and L. L. Tschopp, *Surface. Sci.* **32**, 561, (1972).

[35]   G. Y. Chung, J. R. Williams, C. C. Tin, K. McDonald, D. Farmer, R. K. Chanana, S. T. Pantalides, O. W. Holland, and L. C. Feldman, *Appl. Surf. Sci.* **184**, 399, (2001).

[36]   D. M. Brown, M. Ghezzo, J. Kretchmer, E. Downey, J. Pimbley, and J. Palmour, *IEEE Trans. Elect. Dev.* **41**, 618 (1994).

[37]   A. Pérez-Tomás, P. Godignon, N. Mestres, J. Montserrat, and J. Millán, *Mater. Sci. Forum* **483-485**, 713, (2005).

[38]   A. Pérez-Tomás, P. Godignon, J. Montserrat, J. Millán, N. Mestres, P. Vennegues and J. Stoemenos, *Electrochem. and Solid-State Lett.* **7**, F89, (2004).

Chapter VIII

Conclusions and future work

In this chapter, the general conclusion of this thesis are presented. The main work of this thesis is related with the detection and the efforts in reducing the amount of traps, including the proposition of several innovative gate oxide process fabrication. However although difficult to compare, today the trap density is quite high ($>10^{11}$ eV^{-1}cm^{-2}) regardless which processing technique is used, including the ones developed in this work. The fabrication of MOSFET devices with these layers is the unequivocal test for these thin insulators. Some praiseworthy results have been achieved, especially for deposited gate oxides. The mobility model with Coulomb scattering in interface traps proposed in *Chapter VII* along with simulation results reproduces the low field-effect mobility and provides an explanation for the anomalous mobility improvement, suggesting other disturbing questions. Finally, recommendations for future work are suggested.

8.1. General conclusions

In this thesis some novel materials and processes to form gate dielectrics on Silicon carbide have been introduced. To date, the poor quality of the interface, when a SiC surface is thermally oxidized, has impeded the promising success curse of SiC metal-oxide-semiconductor field effect transistors, MOSFETs. The main efforts of this thesis have been directed to the detection and reduction of interface traps in the oxide/SiC interface. To achieve this demanding objective, two different ways have been contemplated. In one way, investigations have been carried out to improve the thermal oxidation or even to improve the formation of the interface with alternative techniques as nitridation or deposited oxides. On the other hand, the classical insulator made up with SiO_2 has been replaced by other innovative dielectrics. In both ways, we have gone round some pioneering paths with some exiting results, sometimes.

The magnitude that accounts for the number of traps at the interface is the interface states density, D_{it}. D_{it} can be measured from both, electrical and physical

methods. Only electrical measurements are performed in this thesis. D_{it} is difficult to compare from one author to another since it is the result of an indirect measurement, and due to the variety of methods or the strong influence of experimental setups and subsequent analysis procedure. However, although the direct comparison with the literature is a horny subject, our thermal oxidation can be used as the baseline of interfacial quality determination. Table VIII.1 presents the values for D_{it} obtained for all the procedures used in this thesis for the gate oxide definition with a comparison with the commonly reported values of literature.

	Oxidation Process	D_{it} $[cm^{-2}eV^{-1}]$	Polytype (doping)	Improve T-SiO$_2$	Literature
Thermal Oxidation	*CNM Standard*	1×10^{12}	4H-SiC (n)		State-of-the-art
	CNM Standard	1×10^{13}	4H-SiC (p)		State-of-the-art
	CNM Standard	$2\text{-}3 \times 10^{11}$	6H-SiC (n)		State-of-the-art
	O$_2$ Oxidation	1×10^{13}	3C-SiC (n)		Not improved
Nitridation	*N$_2$O/Ar 10%*	1×10^{12}	4H-SiC (n)	X	Not improved
	N$_2$O/Ar 25%	1×10^{12}	4H-SiC (n)	X	Not improved
Deposited Oxides	*PECVD SiH$_4$ N$_2$O*	$4\text{-}5 \times 10^{11}$	4H-SiC (n)	√	State-of-the-art
	TEOS + N$_2$O	3×10^{12}	4H-SiC (n)	X	New process
	TEOS + N$_2$	1×10^{12}	4H-SiC (n)	X	New process
	O$_2$ + TEOS + Ar	8×10^{11}	4H-SiC (n)	√	New process
	O$_2$ + TEOS + O$_2$	1×10^{12}	4H-SiC (n)	X	New process
	N$_2$O + TEOS	5×10^{11}	4H-SiC (n)	√	New process
	RTCVD Si N$_2$O	1×10^{12}	4H-SiC (n)	√	New process
Alternative Dielectrics	*O-Ta$_2$Si (850 ℃ 2 h)*	8×10^{11}	4H-SiC (n)	√	New process
	O-Ta$_2$Si (950 ℃ 1.5 h)	1×10^{12}	4H-SiC (n)	X	New process
	O-Ta$_2$Si (1050 ℃ 1 h)	8×10^{11}	4H-SiC (n)	√	New process
	O-Ta$_2$Si (950 ℃ 1.5 h)	8×10^{11}	6H-SiC (n)	X	New process
	O-Ta$_2$Si (1050℃ 1 h)	1×10^{12}	6H-SiC (n)	X	New process
	T-SiO$_2$/O-Ta$_2$Si	1×10^{12}	4H-SiC (n)	X	New process
	N$_2$O-Ta$_2$Si	6×10^{12}	4H-SiC (n)	X	New process
	O-TaSi$_2$ (1050℃ 1 h)	3×10^{12}	4H-SiC (n)	X	New process

Table VIII.1. Interface states density of the most relevant gate processes developed throughout this thesis. The column *Improve T-SiO$_2$* indicates if the proposed process actually improves our thermal oxide. *T-SiO$_2$*: Thermally grown SiO$_2$ (dry O$_2$).

We have found that among all the process tested in this thesis there are four different gate oxide fabrication processes that improve the standard thermal oxidation on 4H-SiC substrates. The SiO$_2$ deposition from PECVD with SiH$_4$ and N$_2$O has already been reported, with promising results, as gate insulator for SiC devices. However, other relevant issues must be faced up with this dielectric, such as the very high leakage current or the incorporation of oxygen into the layer from the atmosphere. As stressed in *Chapter V*, to date, only two works report about TEOS oxide on SiC. Neither of them, has been deposited using low temperature PECVD technique, and their insulator performances are much more discrete. The RTCVD deposition and subsequent N$_2$O oxidation of a thin Si layer on a SiC substrate is a technique firstly proposed by us in the prestigious conference ECSCRM 2004 (Bologna). However, the main breakthrough in gate process fabrication, of this thesis is the use of the *rare* Tantalum silicide, Ta$_2$Si, to form high-*k* insulator on semiconductors. Although intensive work with silicides has been performed in the last two decades, since they are common

material in microelectronic processing, surprisingly, Ta_2Si has gone unnoticed as potential material to form gate insulators. We have demonstrated that the thermal oxidation of Ta_2Si is a simple way to achieve a high-k dielectric on SiC (and on Si). All the work related with this material (XRD, TEM, C-V, I-V, AFM …) has never been published by other groups. The oxidation that we performed of the common silicide, $TaSi_2$, on SiC also shed new results to the scientific community.

MOS capacitor fabrication is much simpler and cost-effective than the MOSFET fabrication, especially in SiC substrates. For this reason, there are few groups in Europe that actually fabricate SiC MOSFET devices. However, the main objective of the optimization (carried out on MOS capacitors) of thin layers on SiC is the fabrication of high performant SiC MOSFETs, i.e. increase the field effect inversion channel mobility. Some of the thin insulator layers, whose interfacial traps densities have been collected in Table VIII.1, have been utilized to form the gate oxide of SiC MOSFET (generally on the 4H-SiC polytype) throughout this thesis. A summary of the MOSFET channel conduction is presented in Table VIII.2.

	Oxidation Process	SiC Substrate	Mobility [cm²/Vs]	Improve T-SiO₂	Literature
Thermal Oxidation	*CNM Standard*	<0001> 4H	5		State-of-the-art
	CNM Standard	<0001> 4H[a]	10	√ (×2)	Improved
	CNM Standard	<0001> 6H	25		State-of-the-art
Nitridation	*N₂O/Ar 10% Anneal*	<0001> 4H	5	X	No improved
Deposited Oxides	*O₂ + TEOS + Ar*	<0001> 4H	35-45	√ (×9)	Improved
	O₂ + TEOS + Ar	<11-20>4H[b]	216	√ (×44)	Record
Alternative Dielectrics	*O-Ta₂Si (1050 ℃ 1 h)*	<0001> 4H	45	√ (×9)	Improved[c]
	T-SiO₂/O-Ta₂Si	<0001> 4H	5	X	No Improved[c]

Table VIII.2. Measured field-effect inversion channel mobility of n-channel MOSFET with the most relevant gate process developed throughout this thesis. All devices has been implanted on CREE substrates except: [a]Linköping Epitaxy (0001) 4H-SiC and [b]LMI Lyon (11-20) 4H-SiC. [c]anomalous mobility enhancement

With thermal oxides the mobility values achieved are in the unacceptable low level of the state-of-the-art for both the 4H-SiC and 6H-SiC polytypes. N_2O post-oxidation anneal has not result in improving the 4H-SiC field-effect mobility. If low doped 4H-SiC Linköping epitaxies are used instead of the CREE commercial substrates the mobility values rises up to 10 cm²/Vs.

Very high field-effect mobilities have been extracted for planar inversion 4H-SiC MOSFETs with deposited SiO_2-TEOS gate oxides. Mobilities of around 216 cm²/Vs have been extracted for (11-20) 4H-SiC MOSFETs with gate definition using thermal oxidation at 1050 ℃ during 1 h and a subsequent deposition of SiO_2 with TEOS as source material. MOSFET devices have also been fabricated on the (0001) Si face. In this case, depending on the SiO_2 deposition conditions, the mobility improvement (up to 38-45 cm²/Vs) is also remarkable, when compared with a dry thermal oxidized gate oxide (5 cm²/Vs). Indeed, only few processes (based on nitridation or contaminated oxides) have been reported to be effective to achieve that field-effect mobility level on (0001) Si-face 4H-SiC. In the most favorable conditions, the mobility improvement seems to be related with the current leakage more than (or along with) an interface traps reduction of the gate insulator interface. This last statement agrees with the high value

of the sub-threshold slope measured in the high mobility devices or with the presence of oxide charges that provokes a shift of the threshold voltage.

Considering the results aimed in this thesis, the combination of a thin thermal oxide (O_2, N_2O) with a deposited dielectric (TEOS, high-k) seems to be the best solution to achieve performant gate structures. It is generally accepted that a minimum mobility, that thermally grown oxides on 4H-SiC does not achieve, is necessary to fabricate competitive power MOSFETs and VDMOS. We reach this goal in this thesis, and our best results and solutions are already used for the integration of industrial oriented VDMOS.

Surprisingly, high field-effect mobility peak (~50 cm^2/Vs) has been extracted in 4H-SiC (0001) Si face MOSFETs with oxidized Ta_2Si (O-Ta_2Si) high-k dielectric (ε_r ~20) as gate insulator, in the strong inversion regime. As stated from table VIII.1, the interface states density (D_{it}) has not been particularly reduced in O-Ta_2Si capacitors. This anomalous mobility enhancement is explained in terms of the *Coulomb scattering* reduction and quantified using a physical model based on the Lombardi mobility model. The anomalous mobility increase is closely related with the leakage current, and also with the gate breakdown mechanism. The observed interfacial SiO_2 tunnel combined with δ-Ta_2O_5 Poole-Frenkel mechanisms at the O-Ta_2Si gate seems to be a sufficiently low abrupt transition in gate breakdown to obtain an effective *passivation* of the interface traps. Therefore, the increase of free carriers in the inversion layer induced by the gate leakage diminishes the effect of the interface trap Coulomb scattering. Anomalous high mobilities have also been extracted in 4H-SiC MOSFETs with thermal SiO_2 (~100 cm^2/Vs).

Although high mobility devices have been achieved in this thesis, some disturbing issues still remain. Reducing to the minimum the interface trap density is possible to stay far from their predicted bulk mobility value. The search of better mobility performances for SiC MOSFETs seems to be related not only with the enhancement of the interface quality, but also the SiC substrate itself. In fact, it is possible that other mobility degradation factors (as the so-called *acoustical phonon scattering*) strongly influence the inversion carrier flow. Therefore, our results seem to indicate that carriers scattering in interface traps is only a part of the problem.

8.2. Suggestions for future work

The efficient optimization of a simple thermal oxidation is the most desirable solution for fabricating SiC gate oxides, from the engineering point of view. A lot of efforts have been aimed to this issue in the last decade for many research groups. However although difficult to compare, today the trap density is quite high (>10^{11} cm^{-2}eV^{-1}) regardless which processing technique is used, including the ones developed in this thesis. To date, only few success histories seem to approach to the expected solution, and are based in modification of thermal oxidation, especially nitridation or contaminated oxides. Therefore, more work must be carried out in order to approach, as far as possible, the quality of the SiC/SiO_2 (or SiC/oxide) interface to the quality of the nearly ideal Si/SiO_2 interface (<10^{10} cm^{-2}eV^{-1}).

Apart from the poor interface quality, in general, the dielectric properties (leakage current) of the processes tested in this work must be increased. Deposited oxides must be further densified and its stoichiometry should be studied, especially PECVD with

SiH$_4$ and N$_2$O as precursors, whose interfacial properties are promising. Analogously, more work in reducing the insulator bulk defects, which allow carrier conduction via Poole-Frenkel conduction mechanism, of the oxidized Ta$_2$Si layers is required. The asymmetry observed when the gate is biased with positive or negative bias should be further analyzed, as well as the band alignment with the insulator-semiconductor structure.

A lot of work in physical characterization the oxidation of Ta$_2$Si (and TaSi$_2$) layers on Silicon carbide could be performed. A systematic study of the influence of time, ambient, oxidants (i.e. N$_2$O, ozone, NO, …) and temperature on dielectric properties and the possible applications are brand new investigation fields. The oxidation in presence of other dopant species, such as Zr or Hf is another completely immaculate road. Basically, all the investigations related with Ta$_2$Si should be of interest for the scientific community since they remain uninvestigated.

Although the initial expectations of N$_2$O and NO thermal oxides have been progressively growing cold, N$_2$O nitridation or anneal have not significantly reduced D$_{it}$, or increased the field-effect mobility with neither thermal oxidation nor Ta$_2$Si oxidation. Future work must be directed to improve these poor results, taking into account that NO is really the best reported solution for nitridation.

TEOS oxides have resulted in an impressive field effect mobility improvement. The exact nature of this very important mobility enhancement must be further analyzed. The experimental results aim at two related issues for the channel conduction improvement, the SiO$_2$-TEOS deposition process as the critical step and an important leakage current through the gate. Considering the impressive results of this thesis as one decisive step toward one possible solution to the low mobility in 4H-SiC devices seems to be a thorny subject. If the enhancement is related with the gate leakage current could lead a reduced reliability and reproducibility. Indeed, it is mandatory to investigate what is the real origin of the mobility improvement or if it is an apparent improvement few controllable. We speculate that our mobility improvement could be related with the use of contaminated gate oxides that recently have been reported to give very high mobility values. In our case, the contaminants (or anything else that improves the mobility) are presumably introduced during the TEOS SiO$_2$ deposition.

In a similar way, the anomalous mobility enhancement at the gate of oxidized Ta$_2$Si devices on 4H-SiC biased in strong inversion, should be further investigated. Although it seems to be from different nature than the TEOS one, this improvement is also closely related with the leakage current, providing an additional source of inversion charge in the conduction channel. The author speculates that this mobility improvement can be linked with other field-effect enhancement techniques such as the buried-channel MOSFETs. Again the actual applicability, reliability and reproducibility of this effect should be better clarified.

The mobility model proposed in *Chapter VII* can be extensively used in the simulation of inversion channel field-effect devices with high interest in power electronics. Simulation of the on-state characteristics of power lateral MOSFET, IGBT, IBT or VDMOS with high traps density in the interface are susceptible of being studied in combination with commercial 2D simulators. Additionally the mobility model can be eventually enhanced with more rigorous physics or semi-empirical investigations.

VIII. CONCLUSIONS AND FUTURE WORK

Among the investigations beyond the scope of this thesis it can be included a large number of issues, such as the influence of high-k dielectric on the field-effect conduction and in the interface traps Coulomb scattering, the influence of temperature on the dopant activation or the influence on both the energetic and the physical position of traps within the interface, among others.

Publication List of the Author

Publications in International Journals

[1] A. Pérez-Tomás, X. Jordà, P. Godignon , J.L. Gálvez, M. Vellvehí, and J. Millán "IGBT gate driver IC with full-bridge output stage using a modified standard CMOS process", *Microelectronics Journal*, vol. 35 (8), pp. 659-666, 2004.

[2] A. Pérez-Tomás, X. Jordà, and P. Godignon , "Optimization of a very cost-effective high voltage p-channel transistor implemented in a standard twin-tub CMOS technology", *Microelectronic Engineering*, vol. 77, pp. 158-167, 2005.

[3] A. Pérez, D. Tournier, J. Montserrat, N. Mestres, F. Sandiumenge, and J. Millán, "Electrical Characterization of Deposited and Oxidized Ta_2Si as Dielectric Film for SiC Metal-Insulator-Semiconductor Structures", *Mater. Sci. Forum* vol. 457-460, pp. 845-849, 2004.

[4] A. Pérez-Tomás, P. Godignon, N. Mestres, D. Tournier, J. Montserrat, and J. Millán "4H-SiC MIS structures using oxidized Ta_2Si as high-*k* dielectric", *Mat. Rec. Soc. Symp. Proc.* 815, J3.2.1, 2004.

[5] A. Pérez-Tomás, P. Godignon, J. Montserrat, J. Millán, N. Mestres, P. Vennegues and J. Stoemenos "Ta_2Si thermal oxidation, a simple route to a high-*k* gate dielectric on 4H-SiC", *Electrochem. and Solid-State Lett.* vol. 7, pp. F89-F92, 2004.

[6] A. Pérez-Tomás, P. Godignon, N. Mestres, J. Montserrat, and J. Millán, "4H-SiC MOSFETs using thermal oxidized Ta_2Si films as high-k gate dielectric", *Mater. Sci. Forum* vol. 483-485, pp. 713-716, 2005.

[7] A. Pérez-Tomás, D. Tournier, P. Godignon, N. Mestres, J. Millán, "4H-SiC MOS structures fabricated from RTCVD Si layers oxidized in diluted N_2O", *Mater. Sci. Forum*, vol. 483-485, pp. 673-676, 2005.

[8] A. Pérez-Tomás, P. Godignon, J. Montserrat, J. Millán, N. Mestres, P. Vennegues and J. Stoemenos "Characterization of High-k Ta_2Si Oxidized Films on 4H-SiC and Si Substrates as Gate Insulator", *Journal of The Electrochemical Society*, vol. 152, pp. G259-G256, 2005.

[9] A. Pérez-Tomás, P. Godignon, D. Tournier, N. Mestres, and J. Millán, "Effect of oxidation and annealing in Ar diluted N_2O ambient on gate insulator in 4H-SiC", To be published in the *Romanian Journal of Information Science and Technology*

[10] R. Pérez, D. Tournier, A. Pérez-Tomás, P. Godignon, N. Mestres, and J. Millán, "Planar edge termination design and technology consideration for 1.7kV 4H-SiC PiN diodes", Accepted for publication in *IEEE Transactions on Electron Devices*

[11] A. Pérez-Tomás, P. Godignon, N. Mestres, R. Pérez, J. Millán, "A study of the influence of the annealing processes and interfaces on 4H-SiC MOS structures with deposited SiO_2 TEOS as gate insulator ", Submitted for publication in *Thin Solid Films*

[12] A. Pérez-Tomás, M. Vellvehí, N. Mestres, J. Millán, P. Vennegues, and J. Stoemenos, "A theoretical study on the anomalous field-effect mobility peak of O-Ta_2Si/4H-SiC high-k MOSFETs measured in strong inversion", Submitted for publication in *Mater. Sci. Forum*

[13] A. Pérez-Tomás, C. Blanc, P. Godignon, N. Mestres, V. Soulière, and J. Camassel, "PECVD deposited TEOS for field-effect mobility improvement in 4H-SiC MOSFETs on the (0001) and (11-20) faces", Submitted for publication in *Mater. Sci. Forum*

Publications in International Conferences

[1] X. Jordà, P. Godignon, M. Vellvehí, A. Pérez, N. Schofield and B. Taylor. "IGBT-gate *driver* circuit optimised for electric vehicle traction", *Proceedings of SAAEI-Alcalá de Henares. Spain,* 2002.

[2] A. Pérez, P. Godignon, X. Jordà, M. Vellvehí, and J. Millán "P- and N-channel MOSFETs for power integrated circuits using a modified standard CMOS process", *Proceedings of CDE Calella. Spain*, 2003.

[3] A. Pérez, X. Jordà, P. Godignon, M. Vellvehí, J. Rebollo and J. Millán "Complementary high voltage MOSFETs using a modified standard CMOS process", *Proceedings of IEEE-CAS Sinaia Romania*, 2003.

[4] A. Pérez, X. Jordà, P. Godignon, M. Vellvehí, J. L. Gálvez and J. Millán "An IGBT gate driver integrated circuit with full-bridge output stage and short circuit protections", *Proceedings of IEEE-CAS Sinaia Romania*, 2003.

[5] A. Pérez-Tomás, X. Jordá, P. Godignon, M. Vellvehí, and J. Millán, "Optimization of a high voltage p-channel transistor fabricated using a standard CMOS process", *Proceedings of DCIS, Bordeaux, France*, 2004.

[6] A. Pérez-Tomás, X. Jordà, P. Godignon, J. L. Gálvez and J. Millán, "Integrated IGBT gate driver with single floating voltage supply and short-circuit protections", *Proceedings of SAAEI-EPF, Toulose, France*, 2004.

[7] A. Pérez, D. Tournier, J. Montserrat, N. Mestres, F. Sandiumenge, and J. Millán, "Electrical Characterization of Deposited and Oxidized Ta_2Si as Dielectric Film for SiC Metal-Insulator-Semiconductor Structures", *Proceedings of ICSCRM 03*, October 5-10, 2003, Lyon, France.

[8] A. Pérez-Tomás, P. Godignon, N. Mestres, D. Tournier, J. Montserrat, and J. Millán "4H-SiC MIS structures using oxidized Ta_2Si as high-*k* dielectric", *Proceedings of MRS spring Meeting 04*, April 12 - 16, 2004, San Francisco, CA, USA.

[9] A. Pérez-Tomás, P. Godignon, N. Mestres, J. Montserrat, and J. Millán, "4H-SiC MOSFETs using thermal oxidized Ta_2Si films as high-*k* gate dielectric", *Proceedings of ECSCRM 04*, August 31- September 4, 2004, Bologna, Italy.

[10] A. Pérez-Tomás, D. Tournier, P. Godignon, N. Mestres, J. Millán, "4H-SiC MOS structures fabricated from RTCVD Si layers oxidized in diluted N_2O", *Proceedings of ECSCRM 04*, August 31- September 4, 2004, Bologna, Italy.

[11]   A. Pérez-Tomás, P. Godignon, D. Tournier, N. Mestres, and J. Millán, "Gate Oxides on 4H-SiC Substrates Grown or Annealed in N_2O/Ar Mixture", *Proceedings of CAS 04*, October 2 - 4, 2004, Sinaia, Romania.

[12]   A. Pérez-Tomás, P. Godignon, N. Mestres, D. Tournier and J. Millán, "A study of the influence of N_2O and N_2 annealing processes on 4H-SiC MOS structures with deposited TEOS SiO_2 as gate oxide", *Proceedings of CDE 05*, Febrary 2 - 4, 2004, Tarragona, Spain.

[13]   X. Jordà , D. Tournier , M. Vellvehi, A. Pérez, R. Pérez , P. Godignon, and J. Millán, "Comparative Evaluation of High Current SiC Schottky Diodes and Si PN Junction Diodes", *Proceedings of CDE 05*, Febrary 2 - 4, 2004, Tarragona, Spain.

[14]   D. Tournier, A. Perez-Tomás, P. Godignon, José Millán, H. Mank and D. Turover, D. Hinchley, "Impact of fine surface Chemical-Mechanical Polishing on the fabrication yield of 1.2kV SiC-Schottky Barrier Diodes", *Proceedings of ISPSD 2005*, May 22 - 26, 2004, Santa Barbara, CA, USA.

[15]   J. Millán, A. Pérez-Tomás, and X. Jordà, "A Cost-effective high-voltage p-channel MOSFET implemented in a standard twin-tub CMOS technology: Integrated IGBT Gate Driver", *Proceedings of ISIE 2005*, June 20 - 23, 2005, Dubrovnik, Croatia.

[16]   A. Pérez-Tomás, M. Vellvehí, N. Mestres, J. Millán, P. Vennegues, and J. Stoemenos, "A theoretical study on the anomalous field-effect mobility peak of O-Ta_2Si/4H-SiC high-k MOSFETs measured in strong inversion", *Proceedings of ICSCRM 05*, September 18-23, 2005, Pittsburgh, PA, USA.

[17]   A. Pérez-Tomás, C. Blanc, P. Godignon, N. Mestres, V. Soulière, and J. Camassel, "PECVD deposited TEOS for field-effect mobility improvement in 4H-SiC MOSFETs on the (0001) and (11-20) faces", *Proceedings of ICSCRM 05*, September 18-23, 2005, Pittsburgh, PA, USA.

[18]   A. Pérez-Tomás, P. Godignon, N. Mestres, J. Montserrat, and J. Millán, "A study of the thermal oxidation of $TaSi_2$ and Ta_2Si silicides to form dielectric layers for MIS structures on 4H-SiC", *Proceedings of CAS 05*, October 3 - 5, 2005, Sinaia, Romania.