RTCVD synthesis of carbon nanotubes and their wafer scale integration into FET and sensor processes

Thesis presented to apply for the degree of Doctor in Electronic Engineering
at the Universitat Autònoma de Barcelona

by,

Iñigo Martín Fernández

Instituto de Microelectrónica de Barcelona
Centro Nacional de Microelectrónica
IMB-CNM (CSIC)

Philippe Godignon

(Advisor)

Research Professor

Instituto de Microelectrónica de Barcelona
Centro Nacional de Microelectrónica
IMB-CNM (CSIC)

David Jiménez Jiménez

(University tutor)

Associate Professor

Universitat Autònoma de Barcelona
UAB

cnm Centro Nacional de Microelectronica IMB CSIC UAB Universitat Autònoma de Barcelona

SECTION 3: WAFER SCALE INTEGRATION OF SINGLE SWCNTs INTO CNT-FETs

SWCNTs are one-dimensional structures that, depending on their structure, may present a semiconducting characteristic. Therefore, transistors based on semiconducting SWCNTs may benefit from their morphology and from their other exceptional electronic characteristics.

Prototypes of devices based on CNT-FETs or CNT-FET like structures with outstanding characteristics have been demonstrated in the fields of nanoelectronics, sensors and NEMS but well established processes for the wafer scale fabrication have not been developed because SWCNT synthesis is not yet controlled.

This section addresses two goals. The first goal is the development of a process for the wafer scale fabrication of a large amount of back gated CNT-FETs and the development of other processes that may contribute to the optimization of the original design. The second goal is the development of a testing procedure to enable statistical analyses on the fabrication of the devices and on their electric characteristics.

The section is divided in three chapters. The first chapter overviews the transport mechanism on a CNT-FET, its fabrication and its potential applications. The second chapter describes the fabrication of a CNT-FET monitor chip on 4 inch wafers and validates a testing procedure, which is based on the labelling of the electric characteristic of each structure, for statistical analyses on the devices. This testing procedure identified more than 10,000 structures on a 4 inch wafer as functional transistors. The last chapter is devoted to the upgrade of the previously presented process for the fabrication of sensors for bio-electrochemical detection based on passivated CNT-FETs.

Index of Section 3

6 The carbon nanotube field effect transistor ... 109
6.1 Electrical transport on carbon nanotubes ... 110
6.1.1 Electronic structure of SWCNTs ... 110
6.1.2 Transport on a CNT-FET ... 111
6.2 Evolution of the CNT-FET structure ... 112
6.3 Other applications based on CNT-FETs ... 114
Challenges ... 115
7 Wafer scale fabricated CNT-FET structures ... 117
7.1 The monitor chip design ... 118
7.1.1 The test structures ... 118
7.1.2 The carbon nanotube transistors ... 119
7.1.3 Conclusions on the design of the monitor chip ... 120
7.2 Monitor chip fabrication ... 121
7.2.1 Substrate preparation ... 121
7.2.2 Selective synthesis of the SWCNTs ... 122
7.2.3 Electrode patterning ... 123
7.2.4 Technological process optimization ... 124
7.2.5 Results on the wafer scale fabrication ... 126
7.2.6 Conclusions on the wafer fabrication ... 128
7.3 CNT-FET characterization ... 128
7.3.1 The electric characterization procedure ... 128
7.3.2 Statistical analyses on the fabrication and on the performance of the CNT-FETs ... 131
7.3.3 Conclusions on the characterization ... 139
Chapter conclusions ... 140
8 Wafer scale fabrication of a CNT-FET platform for (bio-)electrochemical sensing ... 141
8.1 Design of the CNT-FET based sensing platform ... 141
8.2 Technological process ... 143
8.2.1 Fabrication of the CNT-FET ... 144
8.2.2 Conclusions on the fabrication ... 149
8.3 Electrical characterization ... 150
8.3.1 Overall fabrication yield vs. previous monitor chip fabrication yield ... 150
8.3.2 Statistical analyses on the device identification ... 151
8.3.3 Influence of the design parameters on the fabrication yield ... 152
8.3.4 Conclusions on the electric characterization ... 153
8.4 Electrochemical sensing with the passivated CNT-FET sensors ... 154
8.4.1 Bio-sensing analyses based on passivated CNT-FETs ... 154
8.4.2 Environmental analysis based on passivated CNT-FETs ... 155
Chapter conclusions ... 156
Outlook ... 157
References ... 158

6
The carbon nanotube field effect transistor

The transistor is the fundamental building block of modern electronic devices, and its presence is ubiquitous in modern electronic systems. A FET (Figure 6.1-a) is an electronic device that is composed of a channel, two contacts (source and drain), and a gate that controls the current through the channel. Its actuation is achieved by generating an inversion region (the channel) by applying a voltage to the gate, allowing the flux of electrons across it. These transistors are the basis of today's electronics. There is a great interest in shrinking down the size of this component since a higher integration density can result in the fabrication of more powerful and faster systems on a chip. The transistor scaling is described by the International Technology Roadmap for Semiconductors [1].

A picture of a top gated single CNT-FET is shown in Figure 6.1-b. Its structure is similar to a FET. The channel is a semiconducting SWNT, which is contacted by two metals and actuated, in this case, by a top gate. Although the structure is similar to the MOSFET, the operation of the device is different. When a voltage is applied to the gate of a CNT-FET, it is not an inversion channel that appears along the nanotube but the CNT-metal barriers what are modified.

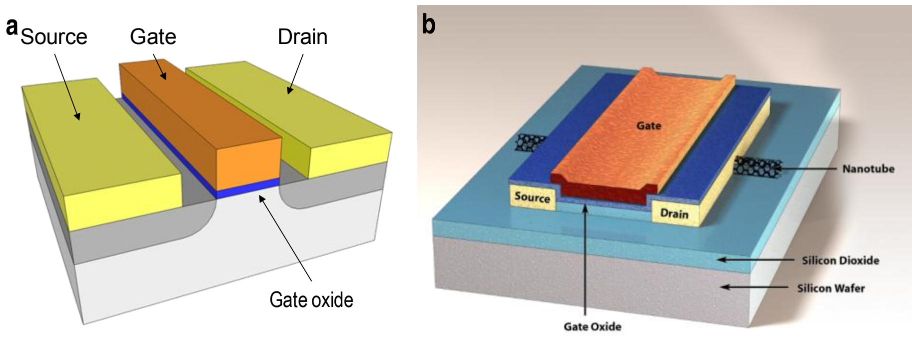


Figure 6.1: Pictures of (a) a MOSFET and (b) a single SWCNT CNT-FET.

The CNT-FET is a device of great interest in the field of nanoelectronics since it presents several advantages with respect to a silicon FET, most of which are related to their structure. First, the fact that a SWCNT is 1D results in a decrease of the phase scattering and so, on an increase of the on-state current. Additionally, its cylindrical structure minimises the scattering due to dandling bonds and allows the utilization of a wider range of gate insulators. This way, the gate actuation may be improved. Furthermore, the "short channel effects" can also be improved because of the strong electron confinement due to the small diameter of the SWCNTs (1-2 nm). Regarding the development of a process technology, the semiconducting SWCNTs are appropriate for the fabrication of a complementary metal oxide semiconductor (CMOS) technology since, according to band structure, electrons and holes present the same effective mass. Besides, and unlike silicon, semiconducting SWCNTs are a direct-gap material, therefore, this could favour the integration of optoelectronics. The ultimate goal would be to integrate metallic and semiconducting CNTs on a same circuit to fabricate a totally CNT-based electronic system.

This chapter describes the operation and the fabrication of CNT-FETs, possible applications different from nanoelectronics and, finally, the technological challenges that are to be overcome for the development of a reliable fabrication process.

6.1 Electrical transport on carbon nanotubes

Electrical transport along a CNT is 1D and the transport characteristics depend on its structure. This way, MWCNTs normally behave as metallic whereas SWCNTs may behave as metallic or semiconducting depending on their structure. The next sections overview the electronic structure and the electrical switching on the SWCNTs.

6.1.1 Electronic structure of SWCNTs

The electronic structure of SWCNTs is normally explained in terms of the band structure of graphene since a SWCNT is normally explained as a folded graphene layer (Chapter 1). Because of the folding of the SWCNT, the energy states of graphene get quatizated and, thus, the energy states of a SWCNT can be considered as a cut of the allowed energy states of graphene (Figure 6.2). When these cuts pass through a K point (Fermi point) of the Brillouin zone, the SWCNT becomes metallic. Otherwise, the tube is semiconducting.

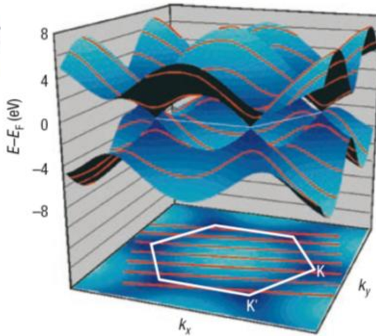


Figure 6.2: The band structure (top) and Brillouin zone (bottom) of graphene. The quatization due to the circunferential structure of the CNT leads to the formation of the discrete energy sub-bands that are depicted by the red lines. Figures extracted from [2].

As explained in Chapter 1, the electronic characteristics of a SWCNT depend on its structure. This way, “armchair” SWCNTs (*m*=*n*, *n* and *m* being the indexes of the SWCNT) are always metallic, SWCNTs where *n*-*m*=3*i* (*i* being an integer) are nearly metallic with a small, curvature-induced gap and, the others (*n*-*m*≠3 *i*) are semiconducting. In the case of the semiconducting SWCNTs, the energy gap (E_g) is around 0.5 eV and depends on the diameter of the SWCNT according to the following expression:

$$E_g = 2\gamma_0 a_{C-C}/d \qquad (6.1)$$

where γ_0 is the is the C–C tight-binding overlap energy (~2.5 eV), a_{c-c} is the nearest neighbour C-C distance (1.42 Å) and d is the diameter of the SWCNT [3]. According to eq. (6.1), the smaller the diameter of a semiconducting SWCNT, the larger its energy gap is.

Theoretical calculations have determined that, for a random distribution of SWCNTs, 1/3 and 2/3 of them will be metallic and semiconducting, respectively.

6.1.2 Transport on a CNT-FET

The existence of two metal-CNT contacts results in two Schottky barriers that govern the transport on the CNT-FET. If the work function of the metal forming the CNT-metal contact is high (such as for palladium), hole and electron transport will be enhanced and inhibited, respectively. On the other hand, if the work function of the metal is low (such as for aluminium), transport will be favoured for the electrons and inhibited for the holes. It is also typical to obtain an ambipolar transport characteristic where hole and electron transport occur for negative and positive gate voltages, respectively (Figure 6.3). Ambipolar transport can be inhibited, by choosing an specific contact metal, by double-gate approaches to control the Schottky barriers [4] or by doping selective areas of the CNT-FET so that atoms or molecules are chemically absorbed on the SWCNT by a charge transfer mechanism [5].

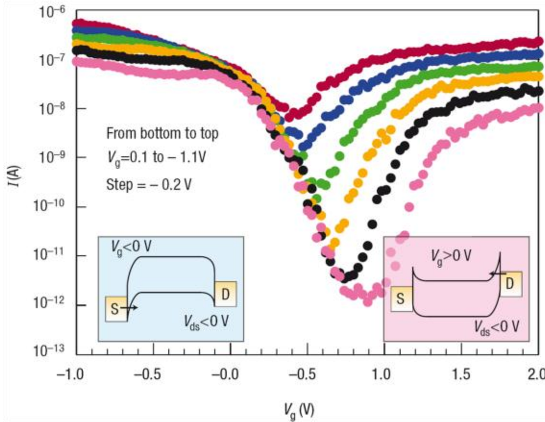


Figure 6.3: Ambipolar transfer characteristics (current versus gate voltage) of a CNT-FET: V_{DS} from –0.1 V to –1.1 V. Left inset: schematic of the band structure of a Schottky barrier semiconducting CNT in a FET under negative gate bias. Holes are injected from the source (S). Right inset: under positive gate bias electrons are injected from the drain (D). Extracted from [2].

The ON-current of a CNT-FET is typically around µA and ratios between the ON and OFF currents in the range of 10^5 and 10^7 can be obtained for unipolar CNT-FETs. Another parameter of importance is the inverse-subthreshold slope, S, that quantifies the efficiency with which the gate switches the channel. Figure 6.4 shows the electrical characteristic of a CNT-FET with optimised CNT-metal contacts, which is actuated by a top gate through a high-k dielectric. I_{ON}≈ 1 µA, I_{ON}/I_{OFF}≈ 10^5 and S≈ 80 mV/dec (close to 60 mV/dec, which is the theoretical optimum). Optimised CNT-metal contacts and gate actuation favour unipolar transport and achieving control over the Schottky barriers at the CNT-metal contacts [4].

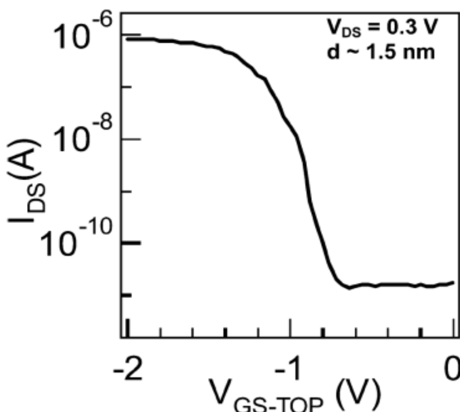


Figure 6.4: Transfer characteristic of a CNT-FET with optimised CNT-palladium contacts and a high-k dielectric (HfO_2).Extracted from [4].

6.2 Evolution of the CNT-FET structure

The transistor effect on CNTs was first reported in 1998 [6, 7] after SWCNTs were deposited on chips where metal contacts had previously been patterned (Figure 6.5-a). Since then, significant progress has been attained on the optimization of the CNT-FET structure [5, 8-12] but, in most of the cases, this was achieved by a dedicated pattern that contacted previously located CNTs [13]. This way, the first logic circuits based on various SWCNTs [14] and on single SWCNT CNT-FETs [15] were first reported in 2001. Research led, in 2006, to the first IC, a 5 ring oscillator, to be fabricated on a single SWCNT [16] (Figure 6.5-b).

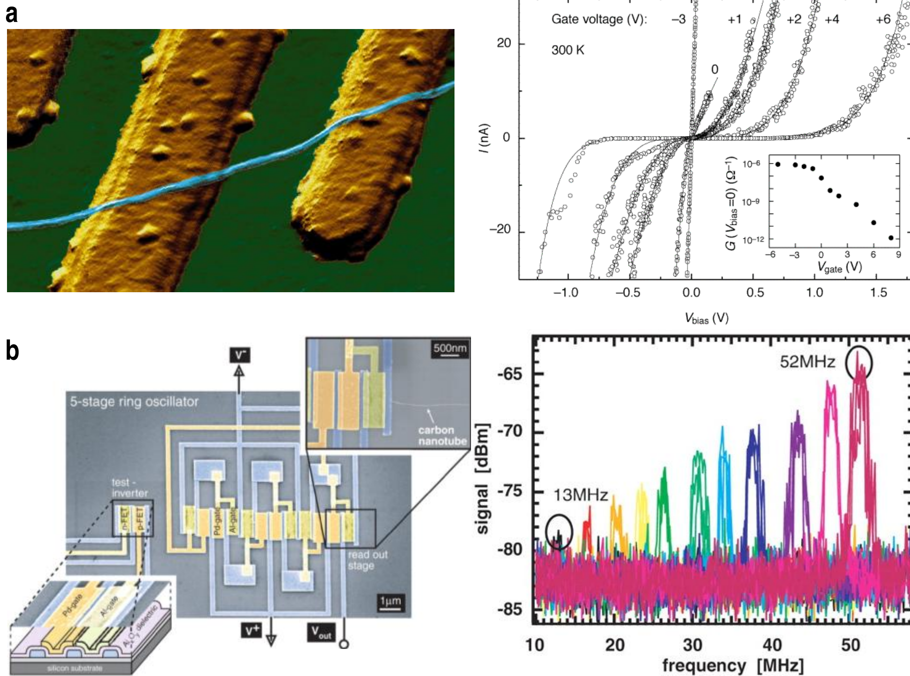


Figure 6.5: Advances on CNT-FET fabrication. (a) AFM image of a SWCNT deposited on metal electrodes and electric characteristic from the first works on the semiconducting characteristic of the CNT-FETs [7]. (b) SEM image of the first IC (a 5 ring oscillator) fabricated on a single SWCNT and its voltage-dependent frequency spectra [16].

However, even if substantial advances have been attained on the improvement of the CNT-FET transport characteristics, not such advance has been yet reached on the standardization of a process for the wafer scale fabrication of CNT-FETs. On the one side, dedicated processes are time consuming and they are not compatible with a standardised fabrication process. On the other side, the processes based on conventional fabrication steps that have been proposed up to date have not succeeded in a massive fabrication of CNT-FETs and in high fabrication yields [12, 17-20].

For example, Tseng addressed the integration of CNT-FETs by optimising the local deposition of the CNT catalyst material, the metal deposition by a double PMMA/photoresist layer and by designing a “u” shaped electrode so that the chances to contact a SWCNT were maximised [12, 17] (Figure 6.6-a). Even if the processes were conventional, presumably because of the CVD synthesis process, the fabrication was performed at chip level. The reported low fabrication yield on functional transistors,

around 1% [17], seems to be significantly improved in reference [12], most probably because of the SWCNT synthesis optimization.

The other fabrication approach that has been proposed for the wafer level fabrication of CNT-FETs is based on dielectrophoresis, which aims a local deposition of CNTs from a solution between two metal electrodes where an electric field is generated for the CNTs to align [21] (Figure 6.6-b). By using this procedure, Vijayaraghavan [19] and Akinwande [20] achieved high yields on the fabrication of high densities of CNT-FETs on a chip and the monolithic integration of CMOS and CNT-FETs, respectively. Two are the main advantages of this procedure. The first is that CNTs are not synthesised but deposited. Therefore, the samples do not have to be subjected to high temperatures that may degrade any device on the sample. The second advantage is that the CNTs may be deposited on any location of the sample and in any orientation. Additionally, as CNTs may be pre-ordered according to their structure, if a certain structure CNTs are preselected to prepare the solution, for example, by differentiation [22], only that in structure CNTs will be deposited. On the other hand, the chance of dielectrophoresis for VLSI is low, due to the fact that the application of a local electric field requires pre-patterned metal electrodes and a procedure to apply the voltage between a large array of electrodes.

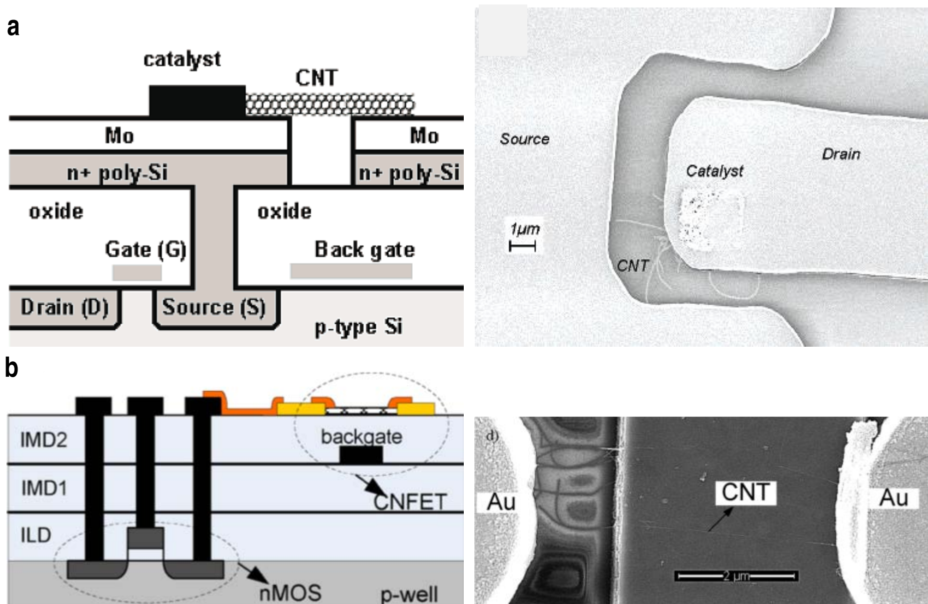


Figure 6.6: CNT-FET integration onto CMOS technologies. (a) Integration based on the selective synthesis of the SWCNTs [17]. (b) Integration based on the selective deposition of the SWCNTs from a solution [20].

As CNT integration into single CNT devices is still not solved, new approaches based on the fabrication of CNT-FETs with channels formed by arrays of CNTs have come to prominence. In these cases, the arrays of SWCNTs may be formed by CNTs that have been grown parallel on a quartz substrate [23, 24], or by arrays of CNTs that grow in any direction after a non selective deposition of the catalyst material [25]. These technological approaches are very promising as wafer scale fabricated circuits have already been demonstrated (Figure 6.7) [24, 26]. However, this fabrication strategy does not solve the challenges related to the fabrication of single CNT devices.

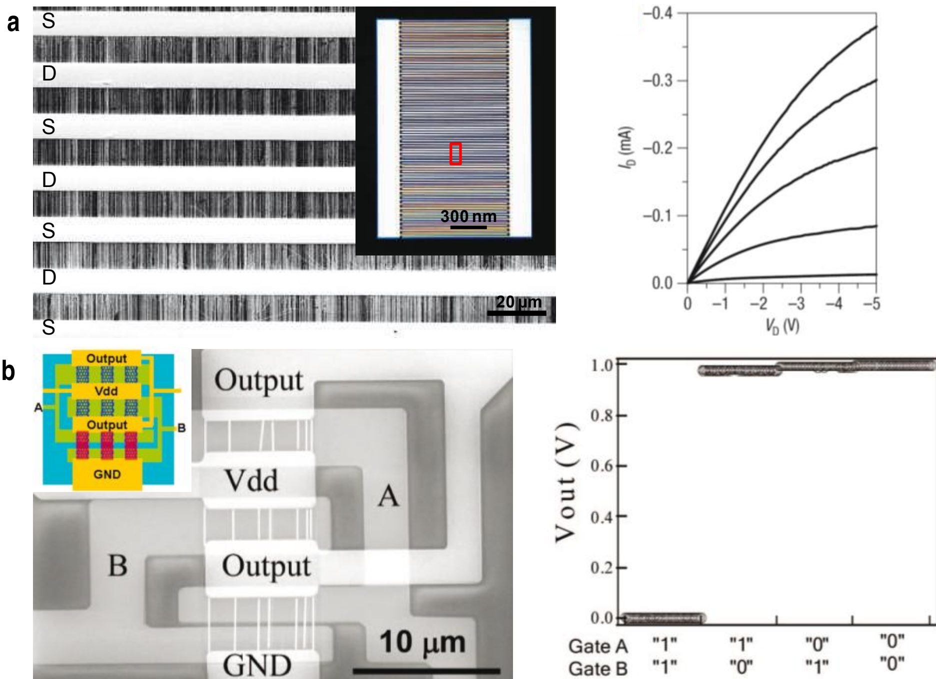


Figure 6.7: Use of arrays of aligned SWCNTs for the fabrication of CNT-FETs and CNT-FET based circuits. (a) Optical (inset), SEM images and transfer curve of a transistor that uses interdigitated source and drain electrodes. The box in the optical image inset delineates the region shown in the SEM image. The gate voltage varies from –5 V to 5 V (top to bottom) [24]. (b) Schematic (inset), SEM image and output characteristic of a NAND circuit [26].

6.3 Other applications based on CNT-FETs

CNT-FETs with channels formed either of one CNT or of an array of CNTs, and CNT-FET-like structures with clamped by the metal electrodes single CNTs are of big interest in fields such as nanoelectronics, sensing or NEMS to exploit the outstanding properties of the CNTs.

As explained in section 6.1, semiconducting SWCNT are, unlike silicon, direct band gap materials which band gap depends on their diameter and are, additionally, very selective to the wavelength [27]. Therefore, semiconducting SWCNTs are very attractive for developing applications in the frame of optics and photonics [28-31].

The fact that significant conductance change is produced with the molecular gating of a CNT-FET makes these devices very attractive for sensing. In addition, the fact that functionalization of the CNTs is possible by different approaches, enables the fabrication of sensors that are selective to a certain analyte. CNT-FETs have been demonstrated for chemical sensing [32-35] and for label free (bio)electrochemical detection [36-40]. These sensors have been shown to be, in some cases, the most sensitive devices. For example, the biochemical sensor developed in [40] was demonstrated to be the most sensitive device for the detection of Bisphenol A in water to date.

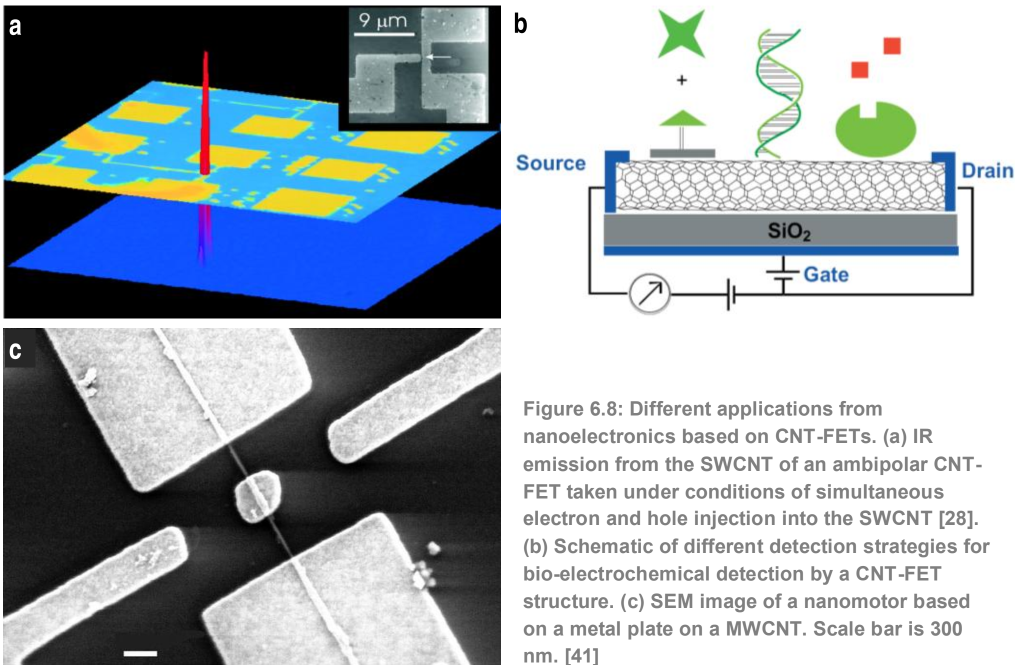


Figure 6.8: Different applications from nanoelectronics based on CNT-FETs. (a) IR emission from the SWCNT of an ambipolar CNT-FET taken under conditions of simultaneous electron and hole injection into the SWCNT [28]. (b) Schematic of different detection strategies for bio-electrochemical detection by a CNT-FET structure. (c) SEM image of a nanomotor based on a metal plate on a MWCNT. Scale bar is 300 nm. [41]

The processes used for the fabrication of CNT-FETs may also be used for the fabrication of CNT based NEMS. These devices have not only been exploited as oscillators but also for applications such as sensing [42-44], for mechanical signal processing [45] or for the fabrication of devices such as nanomotors [41, 46].

Challenges

There is no doubt about the potential of CNTs for the fabrication of performing transistors and as a building block for the fabrication of other devices such as NEMS or sensors. However, the difficulties to standardize the synthesis of the CNTs and the fabrication of CNT based devices at wafer level are hindering the development of CNT based systems.

Whether SWCNTs will be used in the following IC technologies will be elucidated in the next years [47]. At the time being, the development of a standard process for the fabrication of ICs based on single SWCNTs seems not feasible. On the other hand, the reported advances on the fabrication of circuits based on arrays of SWCNT have demonstrated that this technology is promising in a near future. Besides, the development of technologies based on single CNTs or on arrays of CNTs is very promising for applications in the frame of opto-nanoelectronics, sensing and NEMS where the design and fabrication rules may be not so demanding.

7
Wafer scale fabricated CNT-FET structures

As explained in the previous chapter, although the fabrication of different circuits, sensors and NEMS, based on CNT-FET have been demonstrated, the development of conventional technological processes for single SWCNT CNT-FET systems still needs to be attained. This technology should overcome the challenges related to the control of the SWCNT structure and orientation at wafer level and should also address the fabrication of the CNT-FETs at wafer level and by means of conventional microelectronic techniques.

In this chapter previously reported technologies for the batch fabrication of CNT-FETs [12, 17] are considered to develop a similar technology for the batch and massive fabrication of CNT-FET based devices. The objectives of the presented technology are:

- To develop a technological process to achieve the fabrication of a large number of functional CNT-FETs at wafer level and to improve previously reported yields.
- To develop an automatic testing procedure to test every individual device on the wafer in a reasonable time and to perform statistical analyses on the technology as well as on the electric characteristics of the CNT-FETs.

At the present stage, the technology does not aim to overcome the challenges related to the control over the SWCNT diameter and their growth direction. This could be addressed in future technology upgrades.

In order to accomplish these goals, a monitor chip containing almost 6,000 back-gated CNT-FET structures (Figure 7.1) and test patterns was designed, and four inch wafers hosting tens of chips were fabricated by means of conventional microelectronic steps.

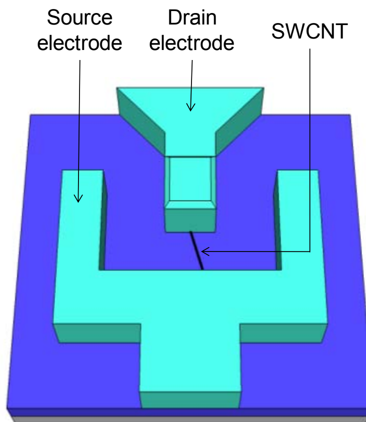


Figure 7.1: Schematic of the back-gate actuated CNT-FET which design, fabrication and characterization are described in this chapter.

Apart from the process, an automatic identification procedure was also developed. The measured data was used to analyse the CNT-FET design parameters' influence on the fabrication yield and on the device performances.

The chapter has been divided in three sections: the monitor chip design, the wafer fabrication and the CNT-FET characterization. In the first section, the different CNT-FET designs, the CNT-FET arrangement and the test structures are described. The second section describes the process flow and shows the results on the fabrication of the chips on 4 inch wafers. The third section addresses the automatic characterization procedure and summarizes the results on the statistical analyses on the CNT-FET fabrication and on their electric characteristics.

7.1 The monitor chip design

The monitor chip is a vehicle to evaluate the CNT-FET technological process. The chip can be divided in two regions (Figure 7.2). The upper region is composed of different testing structures to evaluate the process steps. The lower region is, in turn, divided into 16 zones, each one corresponding to a different CNT-FET geometry. Patterns to perform and evaluate alignment among the three lithographic levels are distributed on the chip edges. In addition to these marks, other motifs for local alignment around the CNT-FETs were also included so that they can be used in further experiments. The size of the monitor chip is 15 x 15 mm^2.

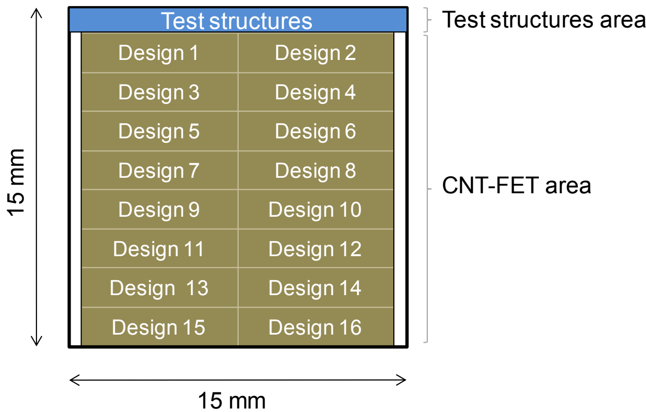


Figure 7.2: Distribution of the test structures and the 16 CNT-FET zones on the monitor chip.

7.1.1 The test structures

The test structures are located at the upper region of the monitor chip and aim at evaluating CNT synthesis and metal patterning (Figure 7.3). The CNT synthesis patterning aims at evaluating catalyst particle deposition and CNT synthesis. The patterning consists of square shaped motifs of different dimensions. The metal structures are L-shaped patterns with different widths and spacing. These structures reveal the minimum width of a metal stripe and the minimum gap between two metal stripes.

Figure 7.3: Schematic of the test structures for the evaluation of the metal patterning. These test structures are 2 µm wide and their spacing is 1, 3, 5 or 7 µm.

7.1.2 The carbon nanotube transistors

The CNT-FET region contains the back-gated CNT-FET structures (Figure 7.4). The SWCNTs that form the channel of the CNT-FET are grown from a catalyst area that is located below the drain electrode. As no strategy is adopted for the oriented growth of the SWCNTs, the growth direction is random. In order to maximise the chances for a SWCNT to be contacted by the source electrode, it was designed U-shape in a similar way to [12, 17]. Besides, the back-gate actuation of the SWCNT is achieved through a metal electrode that contacts the bulk material.

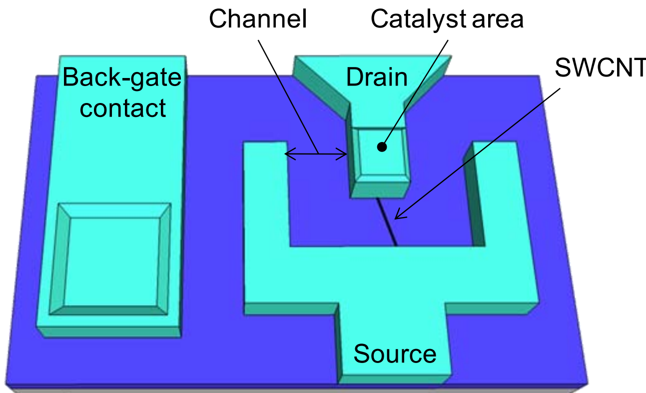


Figure 7.4: Schematic of the designed CNT-FET structure showing the main design parameters.

Each of the 16 zones forming the CNT-FET area correspond to one of the 16 *catalyst area* and *channel* design combinations. *Catalyst area* refers to the area were the catalyst particles are deposited. The catalyst areas are square shaped and of different size: 1 x 1, 2 x 2, 4 x 4 or 5 x 5 µm^2. *Channel* defines the gap between the two metal electrodes. From now on, *channel* will be assumed to be the channel length though it should be taken into account that the CNTs might grow neither perpendicular to the edges of the metal contacts nor straight. The channel length can be 1, 3, 5 or 7 µm. Table 7.1 summarizes the *catalyst area* and the *channel* values for each of the 16 designs.

Each of the 16 zones is sorted in 30 modules which are, in turn, arranged in a 10 row x 3 column matrix (Figure 7.5). Every module is formed of 16 pads. The pads are 100 x 100 µm^2 and the pitch is 150 µm. The distance between two consecutive CNT-FET rows is 180 µm. 12 of the pads on a

Table 7.1: *Catalyst area* and *channel* values for each of the 16 CNT-FET designs on the monitor chip.

Design	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Cat. Area (µm^2)	1 x 1				2 x 2				4 x 4				5 x 5			
Channel (µm)	1	3	5	7	1	3	5	7	1	3	5	7	1	3	5	7

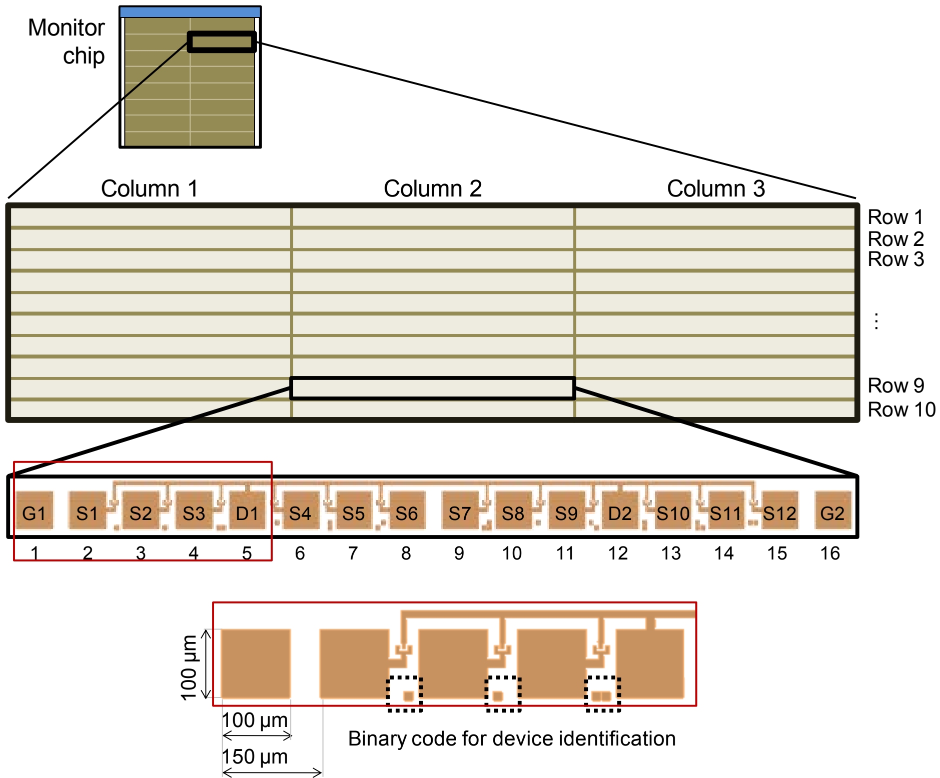


Figure 7.5: CNT-FET distribution on each of the 16 CNT-FET zones. Each zone is arranged in 3 rows x 10 columns modules, each of them being composed of 16 pads. The lower figure shows detail of some of the CNT-FET structures and binary code for device identification on a module.

module are individually related to CNT-FET structures (S1-S12), two pads are common electrodes (D1, D2), and the other two correspond to bulk contacts (G1, G2). A binary code below each CNT-FET structure allows identifying a device among the rest of the structures on the module.

The monitor chip contains a total of 5,760 CNT-FET structures*. Hence, the device density is 2,560 CNT-FET structures/cm^2. Every device on the monitor chip is fully identified by checking its design (1-16), its row number (1 - 10), its module column number (1-3) and its binary code (1-12).

7.1.3 Conclusions on the design of the monitor chip

A monitor chip containing 5,760 CNT-FET structures has been designed to study the fabrication of CNT-FET structures by conventional process technology and their electric characteristics. Thus, neither E-beam lithography nor AFM inspection will be needed, as it is usual, in the fabrication of the CNT-FETs. 16 different CNT-FET designs, which combine 4 different catalyst areas and 4 different channel lengths, have been included in the chip. Therefore, these parameters can be optimised. Besides, the pads of the CNT-FETs have been designed so that the devices can be tested in an automatic probe station.

* 5,760 CNT-FET/monitor chip = 12 CNT-FET/module x 30 module/CNT-FET design x 16 CNT-FET design/ monitor chip

7.2 Monitor chip fabrication

The process, which is made of 15 individual CMOS compatible microfabrication steps, can be divided in three main sections: substrate preparation, selective synthesis of the SWCNTs and electrode patterning. Dislike conventional fabrication of CNT-FET, photolithography is the only patterning technique used in the fabrication of the structures. Three photolithographic levels are needed to complete the fabrication.

7.2.1 Substrate preparation

The starting point material is a 4 inch, 500 µm thick and highly n-doped silicon wafer (Figure 7.7-a). First, the wafers are implanted with phosphorous to optimise the gate actuation of the CNT-FET (Figure 7.7-b). Second, a 100 nm thick silicon oxide layer is thermally grown in dry oxygen atmosphere at 1,100 ºC (Figure 7.7-c).

After these first steps, the first photolithographic level, CNT283-OXID (Figure 7.6), is patterned (Figure 7.7-d). This level allows patterning the windows to connect the bulk material and the metal

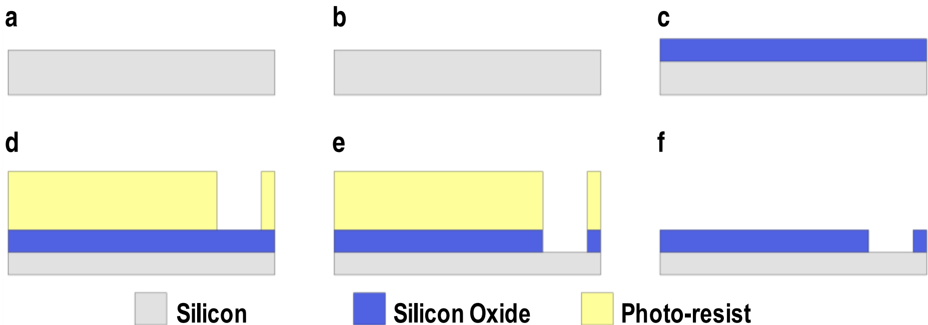


Figure 7.7: Technological steps constituting the substrate preparation. (a) Bulk Si material. (b) Phosphorous implantation on device side. (c) Thermal oxidation. (d) Photolithography. (e) RIE of silicon oxide. (f) Removal of the photoresist by oxygen plasma.

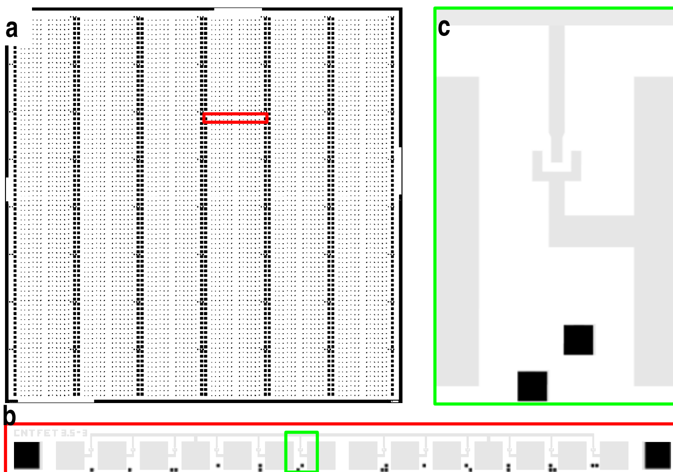


Figure 7.6: Schematic of the CNM283-OXID mask level. (a) Monitor chip level, (b) module level, (c) transistor level. A shadow (light gray) of the metal layer has been included in (b) and (c) for a better understanding of the mask.

electrodes to form the back-gate contact. The alignment motifs and some of the test structures are also included. The etching of the silicon oxide is done by RIE (Figure 7.7-e). The last process of this section consists in removing the photoresist by oxygen plasma (Figure 7.7-f).

7.2.2 Selective synthesis of the SWCNTs

The selective synthesis of the CNTs is accomplished by the selective deposition of the CNT catalyst material. As the catalyst solution is based on a solvent that dissolves photoresist, a strategy based on a PMMA/photoresist double layer was optimized to achieve the selective deposition of the catalyst.

Different strategies were studied to get the pattern transferred to the PMMA layer. These experiments are explained in detail in the next section. Best results were attained with the strategy based on 35K PMMA deposition in combination with oxygen plasma etching.

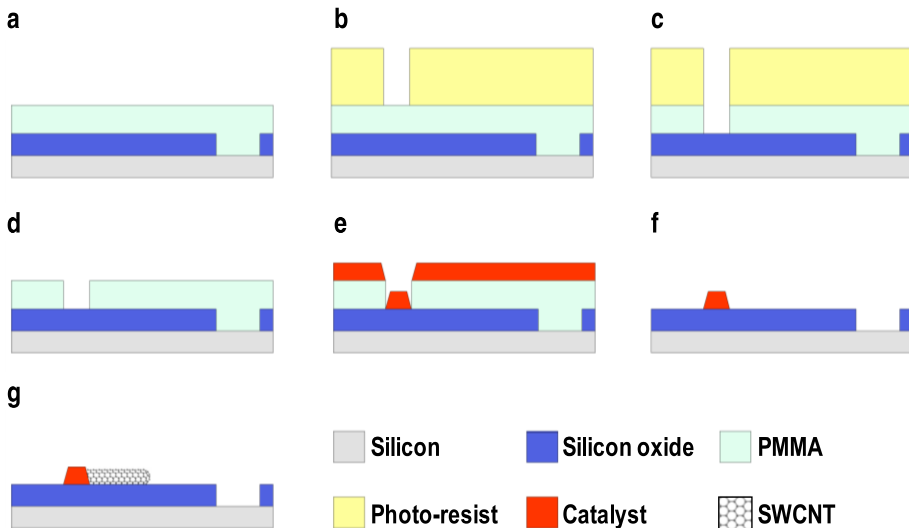


Figure 7.8: Technological steps constituting the selective synthesis of SWCNTs. (a) PMMA coating. (b) Photolithography. (c) Oxygen plasma etching of the PMMA. (d) Photoresist removal. (e) Catalyst material deposition. (f) Catalyst material lift-off. (g) CVD synthesis of SWCNTs.

An initial PMMA layer is deposited by spin coating (Figure 7.8-a). Then, the photolithographic 2nd mask level, CNM283-CNT (Figure 7.9), defines the areas on which the catalyst is to be deposited (Figure 7.8-b). It is important to remark that the dehumidification step that is normally performed for the photoresist for a good adherence would result useless in this case because photoresist is deposited on the PMMA layer. In addition, dehydration was demonstrated to be harmful to achieve an acceptable lift-off of the catalyst material because of PMMA hardening (strategy 2 in next section). Then, the PMMA is patterned by RIE (Figure 7.8-c). The PMMA etching recipe was optimized to control the PMMA etching rate and to achieve a good uniformity across the wafer. The wafers were then immersed in isopropyl alcohol to remove the photoresist, but not the PMMA layer, and rinsed with de-ionised water (Figure 7.8-d).

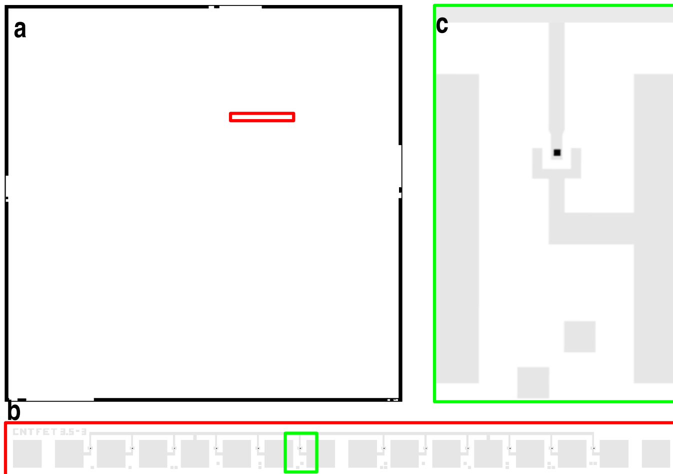


Figure 7.9: Schematic of the CNM283-CNT mask level. (a) Monitor chip level, (b) module level, (c) transistor level. A shadow (light gray) of the metal layer has been included in (b) and (c) for a better understanding of the mask.

The catalyst material is deposited by spin coating (Figure 7.8-e). Iron based particles (iron nitrate and Fe/Mo/Al_2O_3) are used as CNT catalyst (Sections 4.1 and 4.2.4). Optical imaging of the test structures determines if more than one coating is needed to fill the catalyst areas. The lift-off of the catalyst layer is performed in acetone (Figure 7.8-f).

Finally, the SWCNTs are synthesized in the RTCVD system (for a description of the RTCVD system, refer to section 2.1.1) (Figure 7.8-g). A recipe to synthesis a low density of SWCNTs, activation: 800ºC, 400 $sccm_{H2}$, growth: 800ºC; 1200 $sccm_{CH4}$, 400 $sccm_{H2}$, 6 min (section 4.1), should be used in this case. Metallic and semiconducting SWCNTs are randomly expected.

7.2.3 Electrode patterning

The third main issue of the process is the electrode patterning. First, the third photolithographic mask, CNM283-METAL2 (Figure 7.11) is used to pattern the contact metals, tracks and pads (Figure 7.10-a). A 10 nm Ti and 100 nm Pt bi-layer is deposited afterwards by sputtering (Figure 7.10-b). Sputter-etching has to be avoided to prevent the ions etching the SWCNTs on the metal areas. Finally, the metal lift-off is performed in acetone similarly as for the catalyst material lift-off (Figure 7.10-c). Soft ultrasonication may be applied in this case to improve the lift-off results.

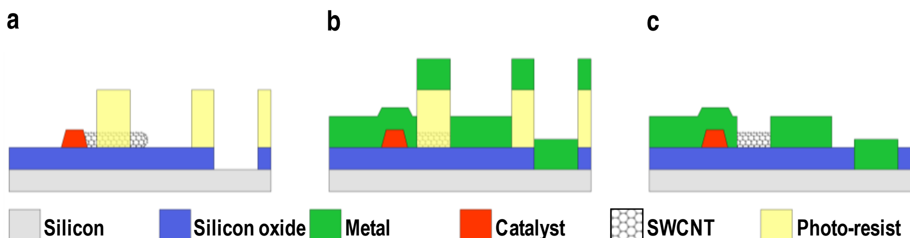


Figure 7.10: The process steps constituting the electrode patterning section: (a) photolithography; (b) metal deposition; (c) metal lift-off.

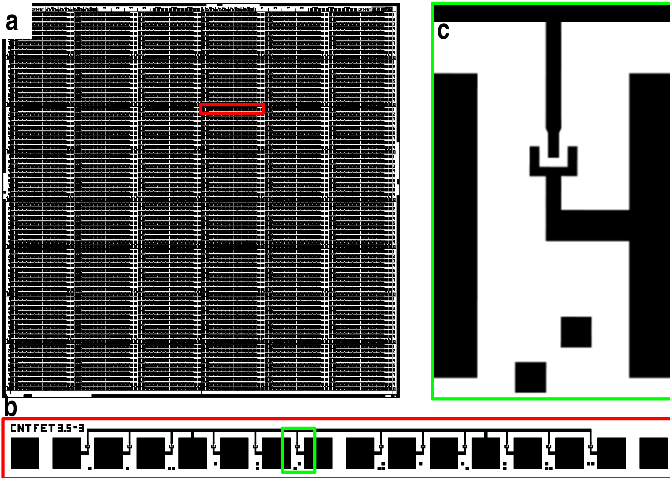


Figure 7.11: Schematic of the CNM283-METAL level. (a) Monitor chip level, (b) module level, (c) transistor level.

7.2.4 Technological process optimization

As explained in the previous section, the technological process development focused, apart from on CNT synthesis optimization, which is discussed in Chapter 4, on the selective deposition of the catalyst material on the wafer.

Three different strategies were analysed to transfer the second photolithographic level for CNT catalyst deposition (Table 7.2). All of them are focused on a PMMA/photoresist bilayer because of the photoresist being utilised in standard CMOS technology and because of the non solubility of PMMA in isopropyl alcohol and methanol, the solvents that are used for catalyst solution preparation (sections 4.1.1 and 4.2.4).

Two different PMMA resists were studied: the 950K PMMA, which is usually utilised in E-beam lithography, and the 35K PMMA, which is used for Nanoimpint lithography. The difference between them lies on the length of the polymer strands, which are shorter in the 35K PMMA.

Table 7.2: Summary of the three studied strategies to pattern a double PMMA/photoresist layer.

	PMMA		Photoresist		PMMA etching	Photoresist removal
	Ref.	thickness	Ref.	thickness		
Strategy 1	950K	100 nm	6512	1.2 μm	Chlorobenzene	IPA
Strategy 2	950K	100 nm	6512	1.2 μm	RIE	IPA
Strategy 3	35K	300 nm	6512	1.2 μm	RIE	IPA

A) Strategy 1

The first strategy involves the use of chlorobenzene (C_6H_5Cl) to etch the 100 nm thick layer of the 950K PMMA since it is very selective to photoresist. The performed experiments, however, did not succeed in attaining standard etching conditions for a uniform etching of the PMMA layer. Figure 7.12 shows the optical images of two test samples that evidence over-etching and under-etching.

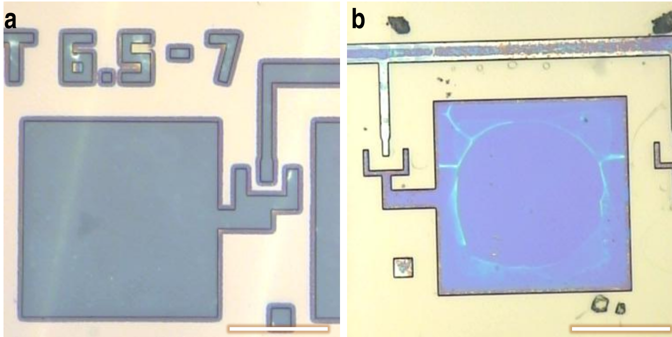


Figure 7.12: Optical images of sample tests for chlorobenzene etching of PMMA. Images show an under-etching of the PMMA layer below the photoresist layer. Scale bars are 10 µm.

Additionally, the etch-stop and the residue removal was demonstrated to be critical because the chlorobenzene solvents (chloroform ethanol, ethyl ether, benzene) are not compatible with the photoresist and because its solubility in water is very poor (around 0.4 g/l). Remaining residues can be observed on both samples in Figure 7.12.

B) Strategy 2

The second strategy consisted in replacing chlorobenzene by oxygen plasma to etch the 100 nm thick 950K PMMA layer.

The etching rates for the photoresist and the PMMA were determined to be similar. As the deposited photoresist layer is more than ten times thicker than the PMMA layer, complete etching (or even over etching) of the PMMA layer did not yield the total removal of the photoresist layer.

This strategy resulted in a good PMMA layer patterning but not in a good lift-off because of PMMA hardening during the photoresist baking step. This baking produces the hardening of the PMMA that results in its deficient removal by acetone and/or plasma oxygen (Figure 7.13).

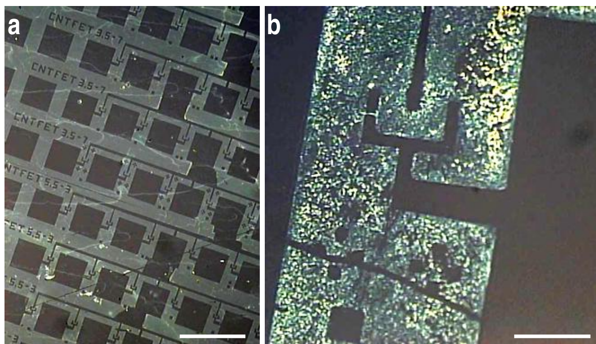


Figure 7.13: PMMA residual layer after PMMA removal with acetone and oxygen plasma. Residues come from the hardening of the PMMA layer. Scale bars are 200 µm and 20 µm, respectively.

C) Strategy 3

The third strategy consisted in replacing the standard PMMA (950K PMMA) by another PMMA composed of shorter polymer strands (35K PMMA).

In this case, a good patterning of the PMMA was achieved (Figure 7.14-a,b) and, even after its hardening, the PMMA layer could be easily removed by acetone Figure 7.14-c.

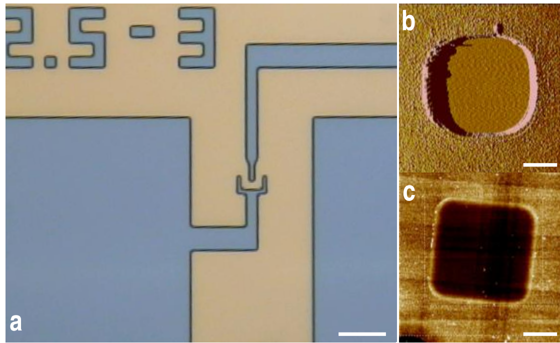


Figure 7.14: Optical and AFM images PMMA/photoresist of test sample. (a) Optical image after PMMA etching. (b-c) Amplitude and topographic AFM images of two different catalyst areas after photoresist removal and after PMMA removal with acetone, respectively. Scale bars are 20 µm, 1 µm and 2 µm in a-c, respectively. Z scale are 50 mV and 5 nm in b and c, respectively.

The optical image in Figure 7.14-a corresponds to a sample after the plasma etching of the PMMA layer. The image shows no residue and a correct definition of the geometries. The AFM image of a catalyst area in Figure 7.14-b shows the adequate removal of the photoresist layer with isopropyl alcohol. The darker colour of the catalyst area in the AFM image in Figure 7.14-c corresponds to a 2 nm etching of the silicon oxide layer. This is due to the over-etching of the PMMA layer to assure the complete removal of PMMA across the wafer.

The attained results were considered acceptable and so, as described in the previous section, this was the retained strategy for the patterning of the PMMA/photoresist bi-layer.

7.2.5 Results on the wafer scale fabrication

The wafers were fabricated as described in the previous sections. The catalyst material and the SWCNT processes were varied on different wafers so that their influence could be analysed. Regarding the catalyst material, apart from the Fe/Mo/Al_2O_3 catalyst composite, the iron nitrate particles were deposited on some wafers. Regarding the SWCNT synthesis, CVD processes to grow low density or high density of SWCNTs were utilised in all cases.

Figure 7.15 shows representative optical images of one of the processed wafers (RUN4672-Obl.1).

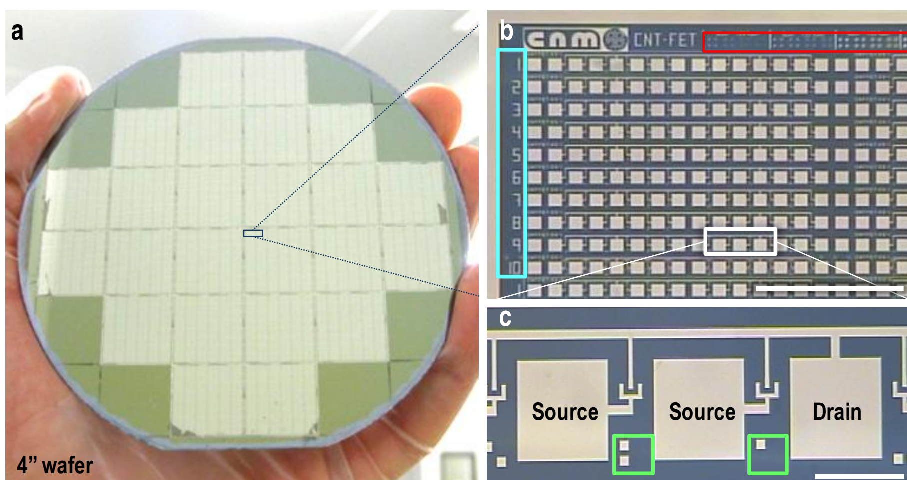


Figure 7.15: Optical images of the fabricated devices. (a) 4 inch wafer hosting 24 monitor chips. (b) Top left corner of a monitor chip. (c) Detail of two devices. Scale bars are 1 mm and 100 µm in b and c, respectively.

Each wafer contains 24 monitor chips (Figure 7.15-a) with almost 140,000 devices in total†. Figure 7.15-b is a zoom of the top left corner of CHIP16. The test structures region on the top of the image is visible as well as the reference numbers for the row identification on the left side. Figure 7.15-c shows two devices in detail corresponding to a 5 x 5 μm^2 *catalyst area* and 5 µm *channel,* and the binary code to identify the device position in the module. The common drain contact for each source contact is also observed.

The fabrication of all CNT-FET designs was successfully achieved except for the 1 µm *channel*, since the 1 µm metal gap was several times miss-patterned after the lift-off process, because of the non optimised parameters of the *electrode patterning* step. However, at this stage the concern was not the yield optimization (yield is analysed in section 7.3.2) but to achieving the CNT-FET fabrication. The metal patterning problems (section 7.2.5) were solved, afterwards, by increasing the photoresist thickness.

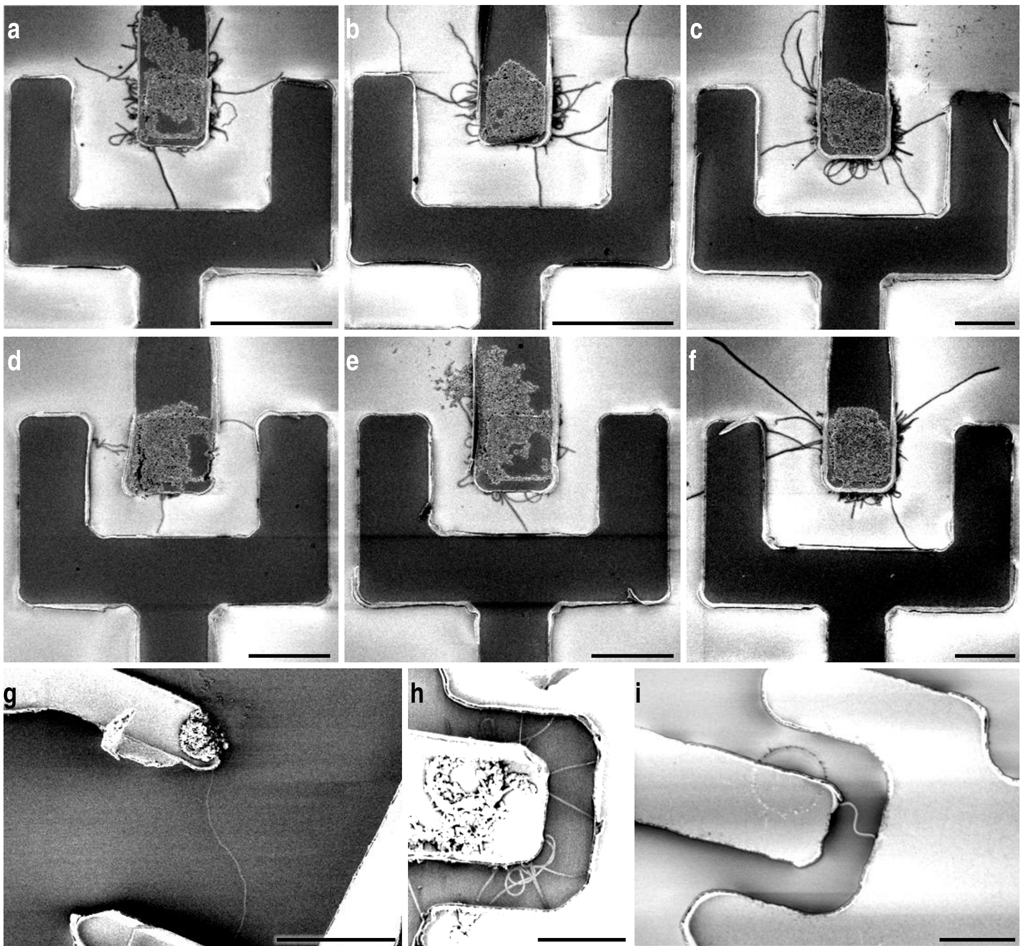


Figure 7.16: SEM images showing that the fabrication of the CNT-FETs was achieved for every design.

† $5{,}760\ \frac{CNT-FET}{MONITOR\ CHIP}\ x\ 24\ \frac{MONITOR\ CHIP}{WAFER} = 138{,}240\ \frac{CNT-FET}{WAFER}$

The SWCNTs synthesis was achieved on 4 inch wafers. The growth density was estimated to be 0.45 SWCNT/μm^2 for the Fe/Mo/Al_2O_3 based catalyst solution, when using CVD process to grow low density of SWCNTs. SEM, AFM and Raman characterization determined, as discussed in section 4.2.4, that synthesised CNTs were SW and that they were typically between 1 and 10 μm long. It has to be noted that for a certain structure it can be found to have no SWCNT, a single SWCNT (Figure 7.16-a,e,g,i) or more than one SWCNTs (Figure 7.16-b, c, d, f, h).

It has to be noted that SWCNTs in the pictures appear to be more than 2 nm in diameter because the discharged silicon oxide around the SWCNTs provides a big contrast with respect to the rest of the surface. Besides, the SEM pictures of the CNT-FET show a metal border around them that was formed because of the conformal deposition linked to the sputtering process. These borders could have been avoided with stronger ultrasonication in the lift-off process. However, it was decided to avoid them to minimise any catalyst material removal that could destroy the metal electrodes and cause damage to the SWCNTs.

7.2.6 Conclusions on the wafer fabrication

These sections have addressed the fabrication of the monitor chip at wafer scale. 24 chips have been included on each 4 inch wafer. Therefore, each processed wafer contains 138,240 CNT-FET structures. The fabrication of the 16 designs on a monitor chip has been achieved, though the wafers' inspection suggests that the yield of the 1 μm channel devices is very low. Besides, the SWCNT synthesis has been achieved at 4 inch wafer level. The CNT-FETs may be formed of one, few or no SWCNTs.

7.3 CNT-FET characterization

Once thousands of CNT-FET structures have been fabricated, a procedure for their testing is required in order to extract individual and statistical information concerning the fabrication yield and their electric characteristics.

The subsequent sections discuss the validation of a procedure to identify the CNT-FET characteristics that enables statistical analyses on the fabrication process and on the performance of the devices. As the complete characterization of all devices on a wafer becomes unaffordable, due to the high density of devices, a procedure based on the automatic and fast testing of the structures had to be developed. The results reported in this section are based on the characterization of wafer RUN4672-Obl.1, which is taken as reference.

7.3.1 The electric characterization procedure

The electric characteristics of a CNT-FET depend on the type (metallic or semiconducting) and on the number of SWCNTs forming its channel. As presented in the previous section, fabricated CNT-FETs may be composed of one or several SWCNTs.

A) Electric characteristics of the CNT-FET devices

Concerning a single-contacted SWCNT CNT-FET, as it has been described in Chapter 6, the SWCNT may behave as semiconducting or metallic depending on its chirality. The electric characteristics in Figure 7.17-a are the typical characteristics of a fabricated CNT-FET, which the SWCNT behaves as metallic. In this case, the drain-source current (I_{DS}) is independent of the gate-source voltage (V_{GS}). Figure 7.17-b is the typical I_{DS}-V_{GS} characteristic for a fabricated CNT-FET with a single semiconducting SWCNT. In this case, I_{ON} (the maximum I_{DS} when V_{DS}= 0.3V for V_{GS} in the range

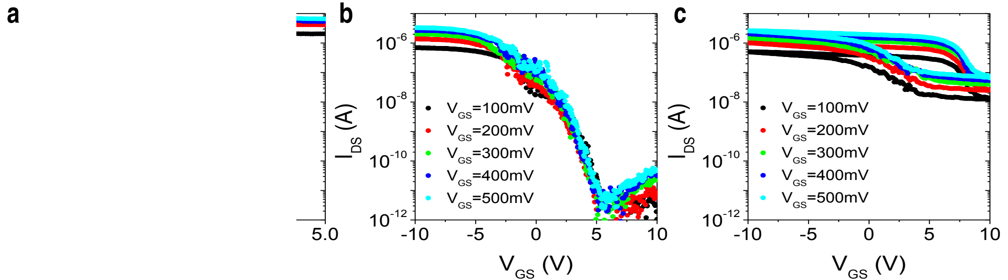


Figure 7.17: Typical I_{DS} - V_{GS} characteristics of the fabricated CNT-FET devices for (a) a device formed of a single metallic SWCNT, (b) a structure formed of a single semiconducting SWCNT, and (c) a structure formed of a combination of metallic and semiconducting SWCNTs.

comprised between -10 and 10V) is in the range of µA and I_{OFF} (the minimum I_{DS} when V_{DS}=0.3V for V_{GS} in the range comprised between -10 and 10V) in the range of pA. In the case of a multi-contacted SWCNT CNT-FET structure, its electrical characteristic is a combination of the characteristics of the CNTs forming the device. An example is shown in Figure 7.17-c. In this case, the fabricated CNT-FET was composed of a metallic and a semiconducting SWCNT.

B) CNT-FET characteristic identification

The device characterization was performed on an automatic probe station (for a detailed description of the setup, refer to section 2.2.2). However, even by an automatic system, the complete measurement of all the devices on a wafer is time consuming. Thus, a two step procedure was developed to evaluate the CNT-FET structures.

The first step of the procedure is the device identification. This step consists in measuring I_{DS} on each individual device at a fixed V_{DS} (300 mV) at three different V_{GS} (-5, 0, and 5 V)[‡]. This step is performed automatically on the wafer. Then, the ratios between the sets of three I_{DS} values (current trios) are computationally analysed in order to identify the device characteristic. The devices can be classified as *open-circuit*, *short-circuit*, *functional transistor* or *metallic and multi-contacted*. The test of all devices on a monitor chip takes approximately 4 hours (~2.5 s/device). The I_{DS}-V_{GS} characteristics in Figure 7.18-a and the current trios in Figure 7.18-b illustrate the procedure. The noise level is different in both figures because of the used different testing parameters.

- ***Open-circuit***: This characteristic is related to devices without any element between the metal electrodes. It can also be related to very unusually ruined devices because of a metal removal (scratches or deficient metal deposition). Their I_{DS}-V_{GS} characteristics are at noise level (devices 2 and 6 in Figure 7.18-b). In this case, the current trio is also below the noise level. The noise levels for the automatic identification and for the complete I_{DS}-V_{GS} characterization were estimated to be 700 pA and 20 pA, respectively.
- ***Short-circuit***: This characteristic is found on devices where a metal layer short-circuits the source and the drain electrodes due to metal lift-off defects. Additionally, short circuited characteristics are also assigned to devices number S7 to S12 on row 1, from column 3 of even numbered designs (check designs description in section 7.1). In this case, both the I_{DS}-

[‡] The program for the automatic probe system to perform the automatic measurements at wafer level was developed by Mr. Marc Sansa.

V_{GS} characteristic and the current trio are above the saturation current level. The saturation current of the devices was estimated to be 12 μA.

- ***Functional transistor***: This characteristic is related to devices where the channel is formed by one or several SWCNTs having, in global, a semiconducting characteristic. A device is identified as functional transistor if $I_{ON}/I_{OFF} \geq 100$, where $I_{ON}=I_{DS}(V_{GS} = -5\ V)$ and $I_{OFF}=\min[I_{DS}(V_{GS} = 0\ V), I_{DS}(V_{GS} = 5\ V]$. The **dark blue** characteristic in Figure 7.18-a, and the device 5 in Figure 7.18-b correspond to *functional transistor* devices. The calculated I_{ON}/I_{OFF} ratio may be lower than the real one (it might be 1000 times lower), which is obtained when performing the whole I_{DS}-V_{GS} characterization, as only three currents are evaluated.

- ***Metallic and multi-contacted***: This characteristic is related to devices in which the channel is formed by a single metallic SWCNT or by several SWCNTs showing, in global, a non *functional transistor* characteristic. In this case, the I_{DS} is between the noise and the saturation levels and $I_{ON}/I_{OFF}<100$. The **light blue** (single metallic SWCNT) and the **red** (multi-contacted SWCNTs) characteristics in Figure 7.18-a, and current trio of devices 1 and 4 in Figure 7.18-b correspond to *metallic and multi-contacted* devices.

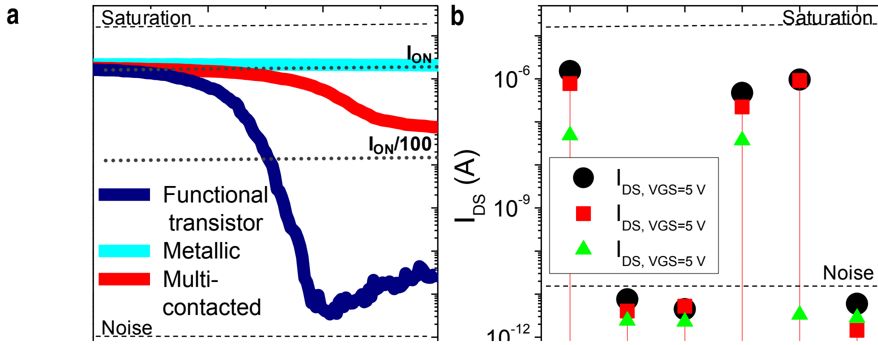


Figure 7.18: I-V chracteristics explaining the automatic device identification procedure. (a) Typical I_{DS}-V_{GS} characteristic of CNT-FETs showing a *metallic and multi-contacted* (light blue and red curves, respectively) and functional transistor (dark blue) characteristics. (b) I_{DS} trios of six devices obtained from the automatic testing. The comparison of the three I_{DS} values of each device is used to identify their electric characteristics.

C) Detailed characterization

The second step is the detailed characterization of the devices identified as functional transistors. The characterization consists in measuring I_{DS}-V_{GS} (V_{GS} ranging from -10 to 10 V), at different fixed V_{DS} values (100, 200, 300, 400, and 500 mV).

D) The Current mapping

The most direct approach to get information on device labelling is the *current mapping*, which consists in plotting the current trios of either an individual chip or all chips on a wafer, according to the different designs. Figure 7.19 is the *current mapping* of the devices on one of the central monitor chips on the wafer (CHIP16 on wafer with reference RUN4672-Obl.1). Each current trio corresponds to one

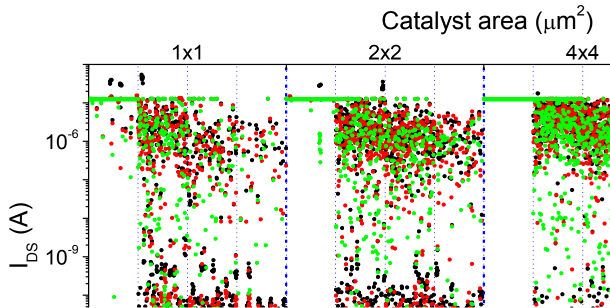


Figure 7.19: ***Current mapping*** **of the devices on one chip. The graph is sorted according to the 16 different designs.**

specific device on the chip. The horizontal axis of the figure is sorted in correspondence with the 16 different designs on the monitor chip. The top horizontal axis sorts the devices according to the 4 different *catalyst area* values, whereas the lower horizontal axis sorts each of the *catalyst area* sections according to the 4 different *channel* values.

The mapping provides with an indication on the global result on the sample. For example, Figure 7.19 shows that the fabrication yield of the 1 µm *channel* devices was very low, since most of the current trios corresponding to these devices are over the saturation level. This evidences non-optimised metal patterning parameters for small *channel* designs. On the other side, for the 7 µm *channel* the current trios are more likely to be at the noise level. This behaviour is expected since the probability of a SWCNT to be contacted decreases with the increase of the channel length.

The *current mapping* by itself is not useful to infer statistical conclusions. On the other hand, the current magnitudes in combination with device identification are suitable for statistics on device process fabrication and on their performance.

7.3.2 Statistical analyses on the fabrication and on the performance of the CNT-FETs

Statistical analyses on the fabricated devices can be performed in different ways. For example, CNT-FETs with a specific I-V characteristic may be pre-selected out of thousands of devices to be used in a certain experiment. This section, however, does not focus on the statistical analyses based on the pre-selection of devices but on demonstrating that the three-current-characterization procedure yields to statistics on the fabrication process and on the performance of the fabricated CNT-FETs.

A) Statistical analyses on device identification

Statistics on device identification are the most straightforward way to evaluate the fabrication process. Table 7.3 shows the results from the device identification comparing the current trios for every structure on each monitor chip across the wafer.

The results on the structure identification for the whole wafer are plotted on the pie graph in Figure 7.20. The most relevant result is that more than 10,000 *functional transistors* were found on the same 4 inch wafer. The fabrication yield is 7%, much higher than that reported by Tseng in reference [17] where 1% yield was attained over 2,048 CNT-FETs. Additionally, the fact that another 33,000 structures were identified as *metallic and multi-contacted* is also noticeable.

The fact that almost half of the structures (46.51%) were identified as open circuit indicates either that the CNT growth density was too low, or that the channels of the CNT-FET structures were too large. This may be clarified when analysing the influence of the fabrication process and the CNT-FET design parameters in the next sections.

The high ratio of labelled as *short-circuit* devices (22.38%) evidences problems on the fabrication of the CNT-FET structures. In particular, it evidences a problem to pattern the electrodes for the small channel (1 μm) structures, which has already been mentioned (section 7.2.5). The improvement of

Table 7.3: Summary of the results on the device identification after the comparison of the current trios for the wafer with reference RUN4672-Obl.1.

	Open circuit		Short circuit		Metallic + multi-contacted		Operative transistors	
	total	%	total	%	Total	%	total	%
CHIP1	3991	69.29	790	13.72	800	13.89	179	3.11
CHIP2	3336	57.92	742	12.88	1291	22.41	391	6.79
CHIP3	3439	59.70	520	9.03	1422	24.69	379	6.58
CHIP4	3274	56.84	1338	23.23	811	14.08	337	5.85
CHIP5	2718	47.19	1138	19.76	1406	24.41	498	8.65
CHIP6	3004	52.15	662	11.49	1652	28.68	442	7.67
CHIP7	2996	52.01	1321	22.93	1178	20.45	265	4.60
CHIP8	2638	45.80	1820	31.60	919	15.95	383	6.65
CHIP9	2083	36.16	2610	45.31	845	14.67	222	3.85
CHIP10	1985	34.46	1877	32.59	1448	25.14	450	7.81
CHIP11	3162	54.90	857	14.88	1310	22.74	431	7.48
CHIP12	2370	41.15	1184	20.56	1817	31.55	389	6.75
CHIP13	2750	47.90	1401	24.32	1349	23.42	260	4.51
CHIP14	2958	51.61	1408	24.44	958	16.63	436	7.57
CHIP15	1645	28.70	2310	40.10	1251	21.72	554	9.62
CHIP16	2024	35.14	1532	26.60	1632	28.33	572	9.93
CHIP17	3093	53.70	646	11.22	1573	27.31	448	7.78
CHIP18	1909	33.14	1245	21.61	2058	35.73	548	9.51
CHIP19	2942	51.08	1181	20.50	1242	21.56	395	6.86
CHIP20	2601	71.63	1526	26.49	1142	19.83	491	8.52
CHIP21	2758	47.88	975	16.93	1501	26.06	526	9.13
CHIP22	2521	43.77	1085	18.84	1618	28.09	536	9.31
CHIP23	2093	36.34	1513	26.27	1635	28.39	519	9.01
CHIP24	2008	34.86	1253	21.75	1968	34.17	531	9.22
TOTAL	**64298**	**46.51**	**30934**	**22.38**	**32826**	**23.75**	**10182**	**7.37**

the technological parameters should lead to the decrease of this ratio.

Finally, the yield of the identified as *metallic and multi-contacted* structures is slightly higher than 23.5%. Theoretically, if no strategy is applied to achieve the synthesis of a particular SWCNT type, the ratio between metallic and semiconducting SWCNT should be 1:2 [48]. According to the pie graph the ratio between "metallic" (*metallic and multi-contacted*) and "semiconducting" (*functional transistors*) devices is 3:1, far from the theoretical expectation. However, it has to be taken into account that the "metallic" devices group is not only composed of devices with a single metallic SWCNT, but also of devices formed of more than one SWCNT, which leads to I_{ON}/I_{OFF} <100. Furthermore, devices formed of a single semiconducting SWCNT with shifted I-V characteristics may also been identified as *metallic and multi-contacted*. Therefore, the ratio between metallic and semiconducting SWCNTs cannot be directly calculated by comparing this ratio.

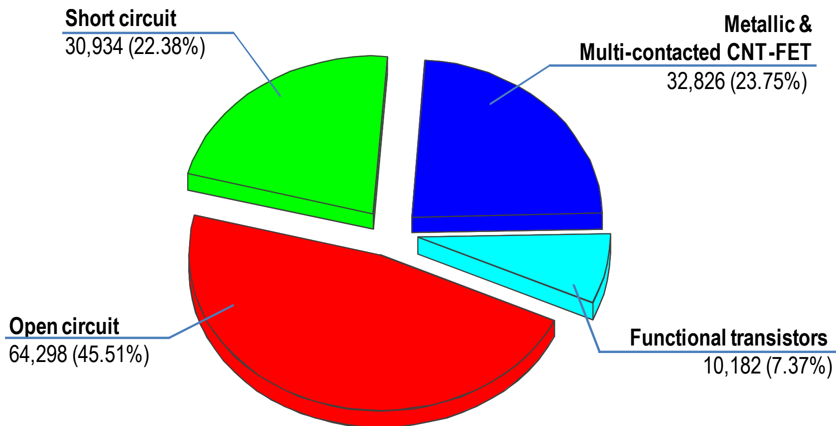


Figure 7.20: Pie graph on the device identification for all the structures on a 4 inch wafer (138,240 CNT-FET structures).

B) Fabrication yield across the wafer

If the statistics on the device identification are reordered according to the location of the CNT-FET structures across the wafer, information on the influence of the fabrication yield as a function of the location of the devices may be obtained.

In this sense, Figure 7.21 shows the percentage of functional transistors per monitor chip as a function of the location of the chip on the wafer (data extracted from Table 7.3). The graph shows that the percentage of functional transistors increases in the south-east direction.

A closer look is taken to three chips in the north-south direction (CHIP1, CHIP15 and CHIP23 in Figure 7.21) in Figure 7.22. The comparison of the bar graphs shows that the percentage of structures identified as *functional transistors* plus the *metallic* structures increases from north to south. Additionally, the bars also show that the percentage of *open circuit* devices is higher for CHIP1 than for CHIP23. These two facts evidence the deposition of higher concentrations of catalyst particles in the south-east areas of the wafer. Although the deposit was performed by spin coating, the evidence of this gradient suggests that this step will need further optimization in order to achieve a homogeneous deposit of the catalyst material on the wafer.

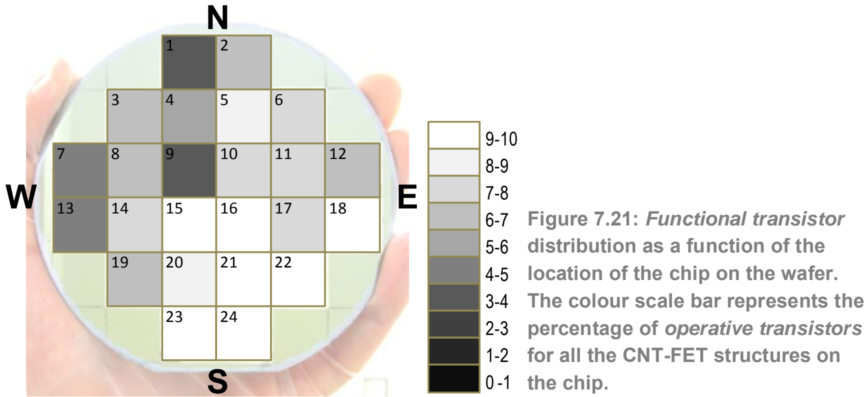


Figure 7.21: *Functional transistor* distribution as a function of the location of the chip on the wafer. The colour scale bar represents the percentage of *operative transistors* for all the CNT-FET structures on the chip.

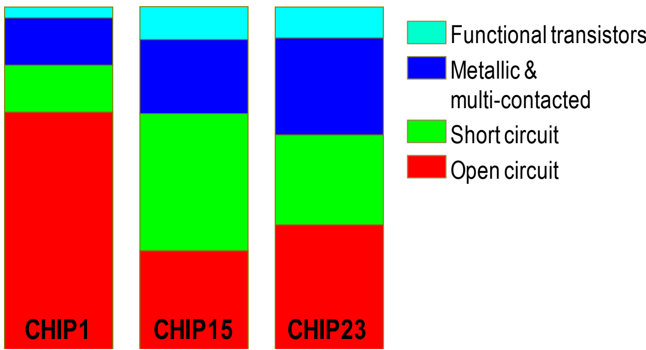


Figure 7.22: Bar graphs showing the distribution of devices for three different chips in the north-south (N-S) direction in Figure 7.21.

Besides the conclusions on the CNT catalyst material deposition, the bar graphs also evidences a higher defect density due to short-circuits on chips at the centre of the wafer. This problem is related to the photolithographic step.

C) Influence of the design parameters on the fabrication yield

The device identification can be used to analyse the influence of the CNT-FET design parameters on the fabrication yield. Thus, the bar graphs in Figure 7.23 shows the labelled as *operative transistors* according to the different CNT-FET designs. The graph is arranged as in the case of the *current mapping* (Figure 7.19). The top horizontal axis is arranged according to the four different *catalyst areas* and the lower horizontal axis divides each section according to the four different *channels*. Regarding the vertical axis, the maximum amount of structures that could be identified as functional transistors is 8,640 (yield of 100%). As previously described, the CNT-FET area on the monitor chip is divided in 16 zones, each of them corresponding to an individual CNT-FET design and each of them being composed of 360 CNT-FET structures (section 7.1). Besides, the 4 inch wafer contains 24 monitor chips (section 7.2.5). Then,

$$360\ ^{\text{same design CNT-FET}}/_{\text{chip}} \times 24\ ^{\text{chips}}/_{\text{wafer}} = 8{,}640\ ^{\text{Same design CNT-FET}}/_{\text{wafer}} \qquad (7.1)$$

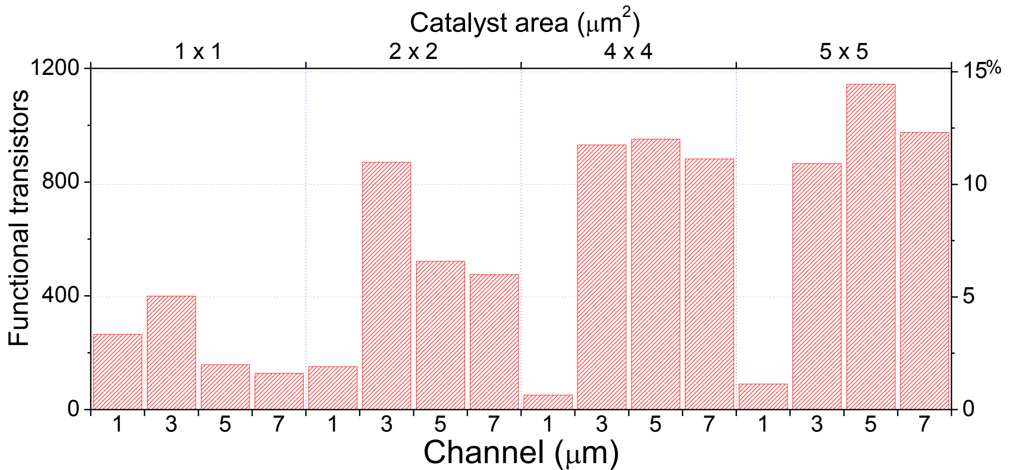


Figure 7.23: Distribution of the functional transistors across the wafer with reference RUN4672-Obl.1 according to the design parameters.

The bar graph shows that the larger the *catalyst area*, the higher the yield on *functional transistors*. The highest yield (almost 15% at wafer level) was attained for the 5 x 5 μm^2 *catalyst area* and 5 μm *channel*. The fact that the yield for the 1 μm *channel* designs is very low is in accordance with previous discussions (sections 7.2.5 and above sections).

The above presented yields at wafer level are not the same as for each monitor chip. This is because of the influence of the location of the chip on the fabrication yield (as discussed in the previous section). In this sense, Figure 7.24 shows the distribution of the functional transistors for CHIP16, which is located at the centre of the wafer. The bar graph is arranged as in Figure 7.23 but, in this case, the maximum number of devices that can be labelled as *operative transistors* is 360.

For this chip in particular, the optimal design was the 4 x 4 μm^2 *catalyst area* and the 5 μm *channel*.

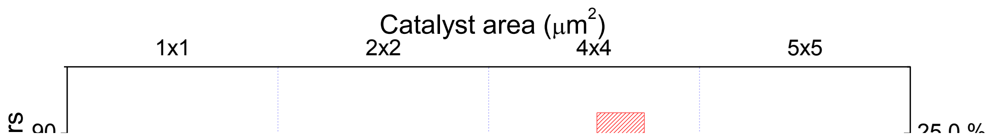


Figure 7.24: Distribution of the *functional transistors* on CHIP16 from the wafer with reference RUN4672-Obl.1 according to the design parameters.

The yield for this design was higher than 25%. Yields close to and higher than 20% were reached on this and other chips for designs where the *catalyst areas* and *channel* were 4 x 4 μm^2 or 5 x 5 μm^2 and 3, 5 or 7 μm, respectively.

The graphs in Figure 7.25 rearrange the data from Figure 7.23 to analyse the influence of the CNT-FET design parameters on the fabrication yield of the *functional transistors*. The fabrication yield for the *operative devices* (*functional transistors* + *metallic and multi-contacted)* has been also included in these graphs.

As it has already been pointed out, regarding the influence of the *catalyst area* (Figure 7.25-a), the yield on functional transistors increases as the catalyst area becomes larger, although the maximum seems to be for the 5 x 5 μm^2 or slightly larger areas. This suggests that the synthesized SWCNT density is low. Therefore, if the synthesis yield was improved or if larger *catalyst areas* were implemented; higher fabrication yield of *functional transistors* could be expected. Regarding the fabrication yield of *operative* devices, the larger the *catalyst area,* the more SWCNTs will be synthesised and, thus, larger number of *operative devices* would be obtained.

Regarding the influence of the *channel*, Figure 7.25-b shows that, once the 1 μm *channel* is rejected (because of the defective fabrication), the smaller the *channel*, the higher the fabrication yield of the *functional transistors*. This conclusion is in agreement with the fact that the SWCNT density on the wafer is low. Figure 7.25-b shows also that the decrease of *operative devices* with the channel length increase is more intense than for the *functional transistors*. This is due to the fact that *multi-contacted* devices are less possible for longer channel lengths.

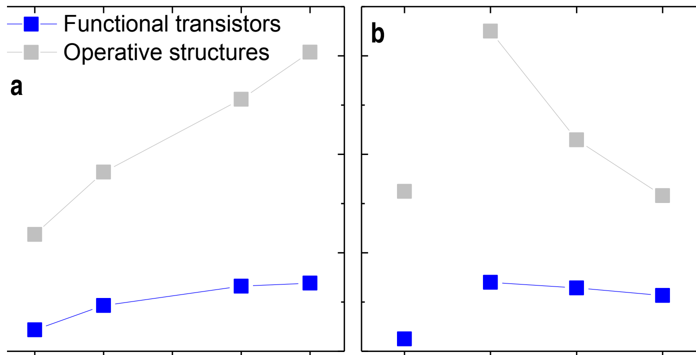


Figure 7.25: *Functional transistor* yield depending on the *catalyst area* (a) and on the *channel* (b). The yield for the *operative devices* (*functional transistors* plus *metallic and multi-contacted*) has been also plotted.

D) Statistical analyses on the performance of the CNT-FET

In the previous section it has been proved that automatic identification procedure can provide statistical information on the device fabrication yield, on the fabrication processes and on the influence of the design parameters. In addition to those statistics, the automatic current trio characterization can be used to perform statistical analyses on the electric characteristics of the devices. Thus, to show the capability of the method, the dependence of the current on the CNT-FETs with the length of the SWCNT was analysed. This study was performed separately on the CNT-FET

that had been identified as *operative transistors* and on those that had been identified as *metallic and multi-contacted*.

I_{DS1}, the drain-to-source current when V_{GS}=-5 V and V_{DS}=0.3 V, was the parameter to be used to carry out these analyses. Although the length of the SWCNTs differs from that of the channel since SWCNT seldom grow straight and perpendicular to the electrodes, the length of the SWCNTs was assumed to be that of the channel because length differences were significantly smaller than the difference between different values of *channel* parameter.

The currents of the devices identified as *functional transistors* and as *metallic and multi-contacted* were grouped according to the *channel* parameter (1, 3, 5 and 7 µm). Then, the histograms of those currents were calculated and normalised to the number of devices for the mean current value. The calculated histograms are compiled in Figure 7.26. The legend of each histogram includes the value

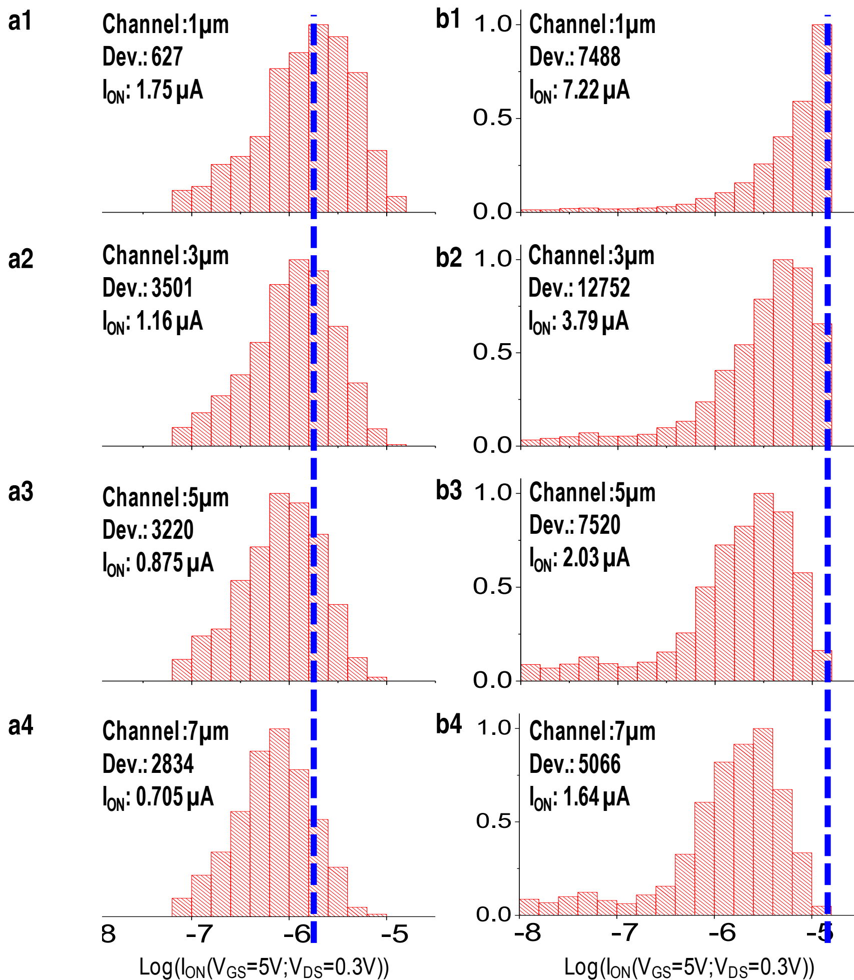


Figure 7.26: Histograms on I_{DS}(V_{GS}=-5V,V_{DS}=0.3V) values for the devices identified as *operative transistors* (a1-a4) and *metallic and multi-contacted* (b1-b4) according to the channel lengths values.

a **b**

Figure 7.27: (a) Dependence of the current with the length of the SWCNT (data extracted from Figure 7.26) and (b) calculated evolution of the resistance for the *functional transistors* and *metallic and multi-contacted.*

of the channel length, the total number of CNT-FET structures to be identified that case and the mean value of the current. Figure 7.26-a1 to Figure 7.26-a4 and Figure 7.26-b1 to Figure 7.26-b4 are the corresponding histograms for the 1, 3, 5 and 7 µm *channel* CNT-FETs that had been identified as *functional transistors* and as *metallic and multi-contacted,* respectively. A vertical line has been drawn at the mean value of the current for the 1 µm channel in both cases to visualise the evolution of the mean current.

Figure 7.27 plots the dependence of the current on the length of the SWCNTs for the *functional transistors* and the *metallic and multi-contacted* CNT-FET structures. Figure 7.27-a shows the evolution of the mean values of the current according to the histograms in Figure 7.26, and Figure 7.27-b plots the calculated resistance values[§]. Two major conclusions can be extracted from Figure 7.27.

First, from Figure 7.27-a it is obvious that the current of the *metallic and multi-contacted* devices is higher than that of *functional transistors* for a given channel length. This is related, on the one side, to the saturation current for a metallic SWCNT, which is higher than for a semiconducting one because of differences in the band structure at the CNT-metal contact [48]. On the other side and as the main reason in this case, the current of the *metallic and multi-contacted* devices is higher than that of *functional transistors,* because they involve the multi-contacted CNT devices where higher currents may flow.

Second, it is evident that the current shifts to lower values as the length of the channel increases. From the graph on the resistance (Figure 7.27-b) one can infer that there exists a linear relationship between the resistance and the channel length. Therefore, it becomes evident that the resistance shift can be related to inelastic scattering due to the structural defects on the SWCNT. This relationship is totally linear in the case of the *functional transistors* (R^2=0.99955 over the data from 10,000 structures), whereas it is not so accurate for the *metallic and multi-contacted* devices (R^2=0.97455). The reason is that the amount of multi-contacted structures is, at the same time, dependent on the channel length as it was discussed in section 7.3.2.

[§] $R = V_{DS} \cdot (I_{DS})^{-1} \xrightarrow{V_{DS} = 300\ mV} R = 300\ mV \cdot (I_{DS})^{-1}$

According to the linear fits, the resistances per length unit are 42.62 and 24.64 kΩ/μm and the contact resistances 128.66 and 14.30 kΩ for the *functional transistors* and for the *metallic and multi contacted* devices, respectively. The difference in the resistance per length unit accounts for, as previously discussed, the devices being formed by more than one SWCNT, whereas the difference on the contact resistance is also due to the band distribution for the CNT-metal contact.

Previous studies on the dependence of the current with the length of the SWCNT based on different characterization techniques have been previously reported [49]. However, this is the first time that these analyses have been performed over 43,000 devices that had been fabricated on a same wafer, in a same process and that had been automatically tested.

7.3.3 Conclusions on the characterization

An automatic procedure for the testing of all the devices across the wafer (138,240 CNT-FET structures) has been discussed. This procedure allows the identification of the electric characteristic of every device on the wafer and eases statistical analyses on the CNT-FETs fabrication and on their electric characteristics.

The most relevant result is the identification of more than 10,000 devices as *functional transistors* (7% of the total structures). Regarding the fabrication statistics, the testing procedure has been demonstrated for analyses on the fabrication yield at wafer level and across the wafer, and for analyses on the yield as a function of the CNT-FET design parameters. The CNT-FET fabrication yield could even be improved in a second fabrication by taking into account these results.

Apart from the statistics on the fabrication, the procedure has been demonstrated for the statistical analyses on the electric characteristics of the CNT-FETs. In this sense, the analyses on the dependence of the drain-source current on the length of the SWCNTs determined that the current is proportional to the amount of defects on the SWCNTs for SWCNT lengths in the 1 to 7 μm range. This analysis was performed over more than 43,000 CNT-FETs.

Chapter conclusions

This chapter has dealt with the development of a technology for the batch and massive fabrication and testing of CNT-FET structures. In order to demonstrate the process technology, a monitor chip has been designed and fabricated to perform statistical analyses on the CNT-FET structures. In particular:

- The technology for the massive and batch fabrication of CNT-FET structures has been presented and demonstrated at 4 inch wafer level. 138,240 CNT-FET structures were included in the wafer. Only conventional microelectronic processes are required to complete the fabrication process being photolithography the only patterning technique to be used in the process.
- A simple and fast labelling procedure based on automatic measurements and on a three-current-characterization has been developed and demonstrated for device identification and for statistical analyses.
- The test procedure has been demonstrated for the analysis of the yield across the wafer. 10,182 CNT-FETs on the same 4 inch wafer were identified as functional transistors. Moreover, another 33,000 structures were identified as devices formed of a single metallic SWCNT or of multi-contacted SWCNTs.
- The procedure has been proved for the analysis of the yield as a function of the CNT-FET location on the wafer. In particular, the dependence of the catalyst location as a function of the position of the chip on the wafer has been determined.
- The procedure has been proved for the yield analysis as a function of the CNT-FET design by analysing the influence of the CNT-FET parameters on the process fabrication of functional transistors.
- The procedure has been proved for the analysis of the device performance as a function of CNT-FET design. In particular, the dependence of the current through the devices on the length of the SWCNT has been evaluated.

The first upgrades of the technology and the development of new CNT-FET based devices for sensing and for new analyses of the electrical performances of SWCNTs are presented in the next chapter.

8
Wafer scale fabrication of a CNT-FET platform for (bio-)electrochemical sensing

Once the viability of the technology to fabricate CNT-FET structures at wafer level was demonstrated, the fabrication of new CNT-FET based devices was considered. In particular, this chapter overviews the wafer scale fabrication of passivated CNT-FETs for bio-electrochemical sensing.

As described in the introductory chapter, CNT-FET based sensors have been demonstrated to be very sensitive for electrochemical sensing. Their higher sensibility facilitates the charge transfer from an analyte and, at a certain threshold voltage, the conductivity along the SWCNT can be dramatically enhanced or decreased. However, the lack of a technological process for the batch fabrication of a large number of devices has hindered the use of passivated CNT-FETs on a wide range of applications.

This chapter focuses on the design of CNT-FET based sensors, on their fabrication, and on the evaluation of the impact of the geometrical parameters on the behaviour of the CNT-FET devices.

Figure 8.1 is a schematic of a bio-electrochemical CNT-FET sensor. The CNT-FET structure is formed of a SWCNT that is contacted by two metal electrodes and is actuated by a back-gate. The sensor also includes a liquid polarization electrode that is devoted to electrochemical experiments. The sensor is fully passivated except on the channel region of the CNT-FET, on the electrochemical electrode and on the connection pads.

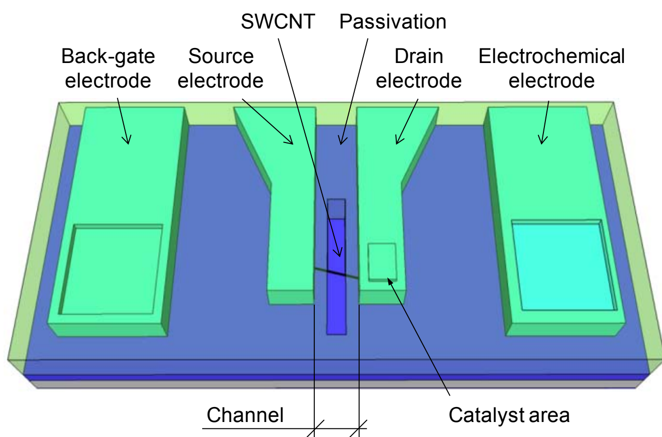


Figure 8.1: Schematic of a passivated CNT-FET sensor and its main elements.

8.1 Design of the CNT-FET based sensing platform

The CNT-FET sensing platform is shown in Figure 8.2. The schematic in Figure 8.2-a represents the full platform whereas the schematic in Figure 8.2-b shows one of the four quadrants the platform is

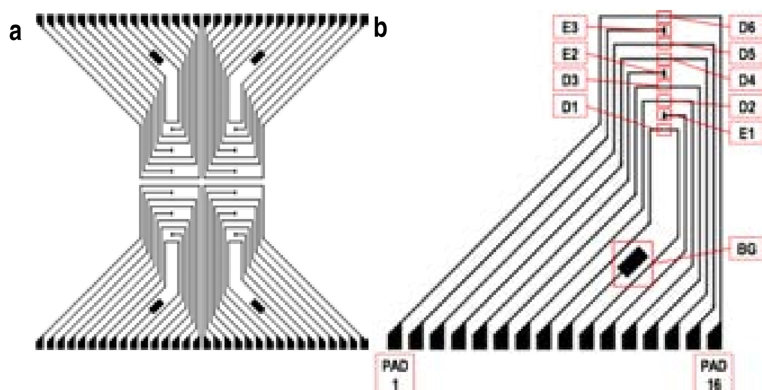


Figure 8.2. (a) Schematic of the CNT-FET platform. (b) Schematic of one of the four quadrants forming the platform. The four quadrants are symmetrically the same. Labels are related to Table 8.1.

formed of. The four quadrants on a chip are symmetrically the same. The platform design aims at concentrating the maximum number of CNT-FET structures at the centre of the chip, far from the connection pads, for a 3 mm in diameter interface chamber to be installed when performing the electrochemical experiments.

The elements on a quadrant are the 6 CNT-FET structures, a back-gate electrode and 3 liquid polarization electrodes, which correspond to labels D1 to D6, to labels E1 to E3 and to label BG in Figure 8.2-b, respectively. Each quadrant is related to a 16 pad matrix that is adequate to be used in the automatic testing of the devices (section 2.2.2). The size of these pads is 100 x 100 μm^2 and the pitch is 150 µm. Table 8.1 summarises the different elements on a quadrant and their corresponding pads. Regarding the pad labelling, it has to be remarked that the pads on each quadrant are always labelled from left to right being PAD1 is the pad at the left edge and PAD16 the pad at the right edge.

Eight different CNT-FET structures were designed combining 3 different parameters (channel length, electrode shape and number of catalyst areas). Schematics of the different configurations are shown

	Element	**PADs**
BG	Back-gate	P9
D1	CNT-FET_1	P8-P10
D2	CNT-FET_2	P7-P12
D3	CNT-FET_3	P6-P13
D4	CNT-FET_4	P4-P14
D5	CNT-FET_5	P3-P15
D6	CNT-FET_6	P1-P16
E1	Top electrode 1	P11
E2	Top electrode 2	P5
E3	Top electrode 3	P2

Table 8.1: Elements forming a quadrant and their connections. The table is related to the labels on Figure 8.2.

Figure 8.3: Schematic of the three design parameters of a CNT-FET structure: (a) channel length, (b) electrode shape, (c) number of catalyst areas.

in Figure 8.3-a to Figure 8.3-c. The channel length, the electrode shape and the number of catalyst areas may be 1.5 or 3 µm, L-shaped or T-shaped, and 1 or 2, respectively.

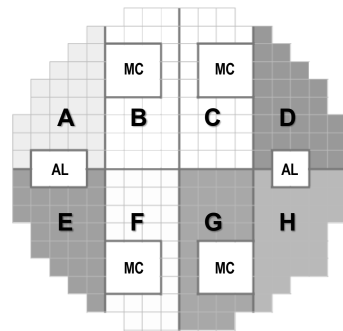
Table 8.2 shows the configuration of the eight different designs, which are labelled A to H. All the CNT-FETs on a chip are identical in design. The table also shows the amount of chips of each design per a 4 inch wafer. The drawing in Table 8.2 shows the chip and designs' distribution across the wafer. Apart from the areas labelled A to H, which correspond to de CNT-FET sensor chips, 6 additional areas are observed on the picture.

The MC labelled areas identify 4 monitor chips. These monitor chips are identical to those described in chapter 7. They serve as a testing vehicle to evaluate the fabrication of the sensors. The AL labelled areas are the areas containing the alignment marks and the test structures.

A 4 inch wafer is composed, in total, of 234 chips that are related to 5,616 CNT-FET structures[*]. Apart from those structures, the 4 included monitor chips lead to a total of 23,040 CNT-FET structures[†].

Table 8.2: Summary of the design of the 8 different designs on the wafer and the designs' distribution across the wafer.

Design	Gap (µm)	Electrode shape	Number of cat. areas	Number of chips
A	1.5	line	1	26
B	1.5	line	2	26
C	1.5	T	1	26
D	1.5	T	2	27
E	3	line	1	26
F	3	line	2	26
G	3	T	1	26
H	3	T	2	27



8.2 Technological process

The fabrication of the CNT-FET platform is divided into two main steps: the fabrication of the CNT-FET structures and their passivation process.

[*] $5{,}616 = 6\,\frac{CNT-FET}{quadrant}\;x\;4\,\frac{quadrant}{chip}\;x\;234\,\frac{chip}{wafer}$

[†] $23{,}040 = 5{,}760\,\frac{CNT-FET}{monitor\ \ chip}\;x\;4\,\frac{chip}{wafer}$

8.2.1 Fabrication of the CNT-FET

The fabrication process of the CNT-FET structures is based on that of the monitor chips (section 7.2). Thus, the process only includes conventional microelectronic processes and, therefore, photolithography is the only patterning technique to be used. The fabrication of the chips is performed at 4 inch wafer level.

Because of the similarities of the process to fabricate the sensors and the process to fabricate the monitor chips, a detailed description is only given for the process steps that were upgraded in relation with the former process. For a detailed description of neglected individual steps, refer to section 7.2.

The fabrication of the chips can be divided in three main phases: the substrate preparation, the selective synthesis of the SWCNTs, and the metal electrode deposition and patterning. Schematics of the fabrication of a CNT-FET sensor are shown in Figure 8.4.

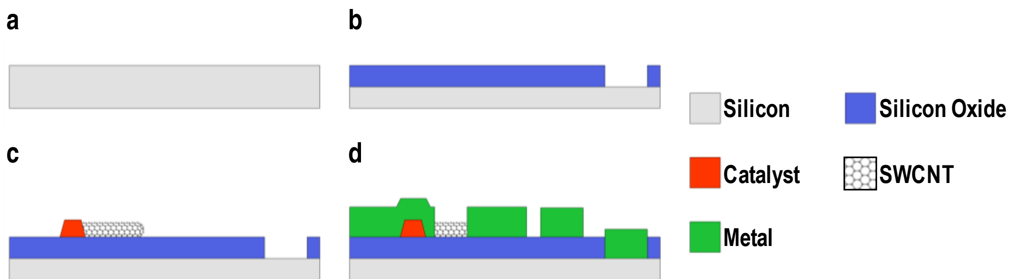


Figure 8.4: Schematic of the main steps of the technological process for the fabrication of the CNT-FET structures: (a) silicon substrate, (b) substrate preparation, (c) selective synthesis of SWCNTs and (d) metal electrode deposition and patterning.

The starting material is a highly p-doped 4 inch silicon wafer (Figure 8.4-a). The substrate preparation begins with a further doping on the device face of the wafer to improve the back gate actuation. Then, the wafers are thermally oxidised to grow a 100 nm thick silicon oxide layer. Finally, the first photolithographic step, mask level CNM392-OXID (Figure 8.5-a), and a RIE are performed to pattern the windows that will further be used to contact the bulk material to the electrodes related to the back gate actuation (Figure 8.4-b).

The selective synthesis of the SWCNTs involves the selective deposition of the CNT catalyst material and SWCNT synthesis itself. The process starts by depositing a 35K PMMA layer by spin coating. Then, the second photolithographic step is used to define the catalyst areas (mask level CNM392-CNT (Figure 8.5-b)). Third, the PMMA is patterned by oxygen plasma. Then, the photoresist is removed with isopropyl alcohol. Once the PMMA has been patterned and the photoresist removed, the catalyst material (Fe/Mo/Al_2O_3, section 4.2.4) is spin coated and patterned by lift-off. The SWCNT synthesis is performed in the RTCVD system by a recipe that provides a low density of SWCNTs (Figure 8.4-c).

The metal electrodes patterning step was optimised with respect to the previous fabrication of CNT-FET structures to avoid the miss-patterning of the metal for small channel lengths. The improvement consisted in using a thicker photoresist layer than the standard one, 2 µm instead of 1.2 µm. By increasing the resist thickness, it is more difficult for the lateral deposition to hinder the lift-off and thus, better metal definitions can be expected. The mask level CNM348-METAL (Figure 8.5-c) is used to pattern the metal electrodes, the stripes, the pads and the new alignment marks to be used in the

further lithographic steps. The remaining steps and parameters for the metal electrodes patterning are those reported in section 7.2. After the lithography is performed, a titanium/platinum (10/100 nm) bi-layer is deposited by sputtering and then patterned by lift-off (Figure 8.4-d).

A) CNT-FET passivation procedure

A passivation procedure was optimised to achieve the fabrication of passivated CNT-FETs. The major difficulty of this process was related with the accurate alignment of the pattern with respect to the already fabricated structures. For this reason, due to its alignment and writing precision, E-beam lithography was the selected lithographic technique. In order to keep the process scalable to wafer

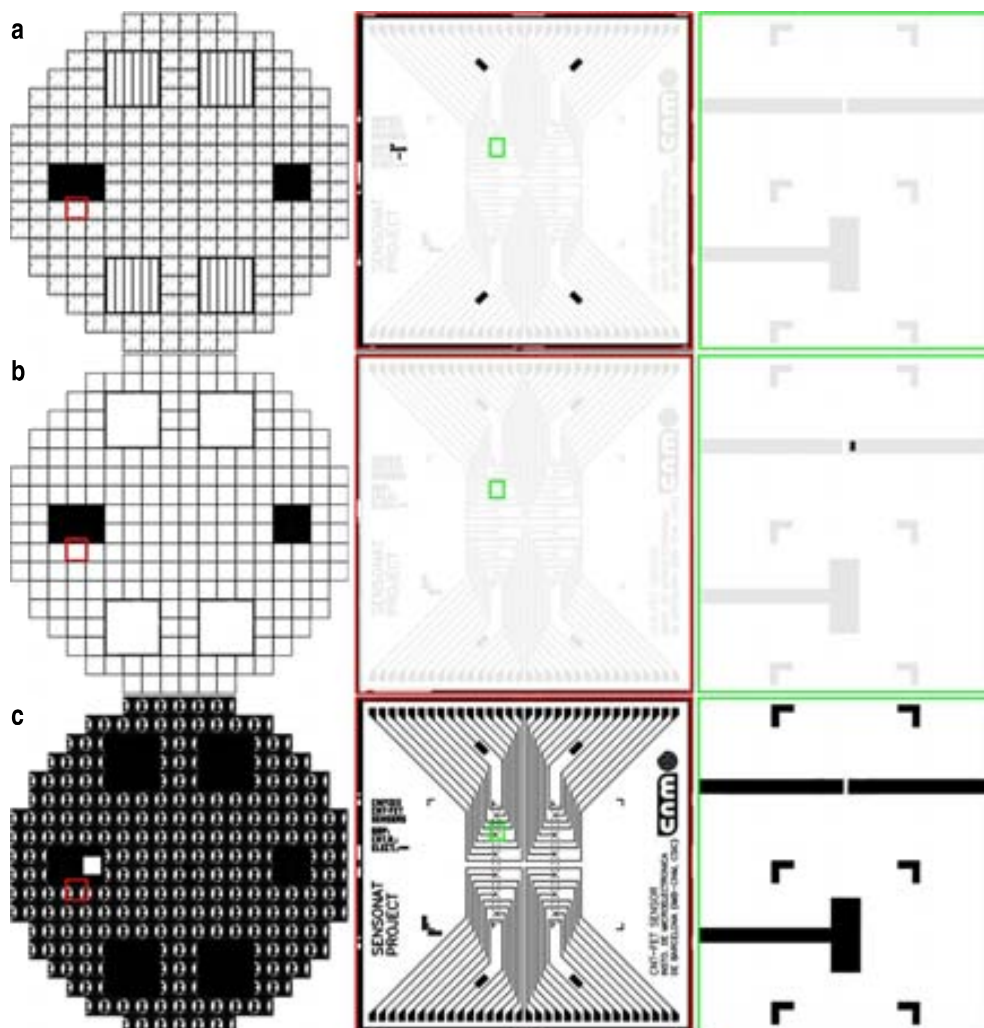


Figure 8.5: Schematic of the mask levels used in the fabrication of the CNT-FET structures: (a) mask level CNM392-OXID, (b) mask level CNM392-CNT and (c) mask level CNM-392-METAL. The light gray backgrounds at the chip and detail schematics in a and b are included for a correct undestanding of the mask levels. These backgrounds are not part of the mask levels.

level, a Raith150-Two E-beam system that allows a semi-automatic[‡] alignment on wafers up to 8 inch was used. The E-beam conditions (5 kV) were set based on the previous results on E-beam exposure of CNT-FET devices [50] so that the electron exposure did not cause any permanent damage on the devices.[§]

Even if the described processes are scalable at wafer level, they were optimised at chip level for the fabrication process to be faster and the samples to be easier to manipulate. This way, the wafer was diced into 1 x 1 cm^2 chips by means of an automatic dicing saw so that, each chip was formed of a 2 x 2 array of CNT-FET chip platforms. Before its dicing, the wafer was protected by coating its surface with a PMMA layer to prevent it from any dust or water getting in contact with the devices. After dicing the wafer, the protective layer was removed with acetone and then rinsed in isopropyl alcohol.

The main steps of the passivation procedure are the PMMA coating, the E-beam lithography and the removal of the PMMA from the pads. A schematic of the main steps is shown in Figure 8.6.

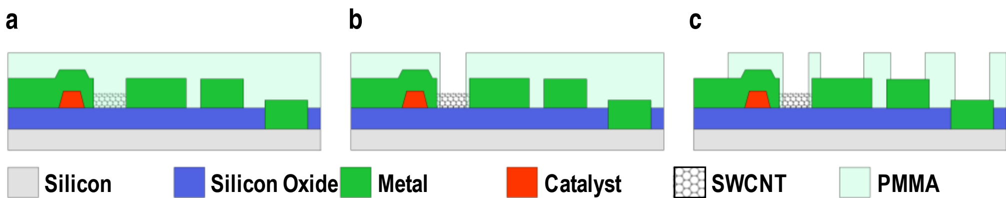


Figure 8.6: Schematic of the main steps for the fabrication of passivated CNT-FET structures. (a) CNT-FET structure. (b) CNT-FET structure after PMMA deposition. (c) CNT-FET structure after E-beam lithography and PMMA development.

The procedure starts by coating the chips with a double 100 nm thick 950K PMMA layer, the resist that is usually employed in E-beam lithography. A double layer has to be deposited to assure the coverage of the structures that are thicker than 100 nm. Figure 8.6-a is the schematic of a CNT-FET after the PMMA coverage.

The second step consists of the E-beam lithography to pattern the passivation layer on the channels of the CNT-FETs and on the liquid polarization electrodes (Figure 8.6-b). These openings are 50 µm × 500 nm. The E-beam alignment procedure requires different marks to define the field where the E-beam writing takes place. The smaller the field, the more accurate the alignment and the writing result. Two different set of marks were used for the field alignment: a set of 3 marks for the alignment at chip level (Figure 8.7-a) and sets of 4 marks around each CNT-FET structure to define the local fields (Figure 8.7-b). The chip alignment marks are only required for the first alignment. Once the first field has been defined, E-beam may be automatically performed at chip level and, subsequently, at wafer level. After the structures have been exposed, the PMMA layer is developed in a methyl isobutyl ketone (MIBK) solution.

The final step of the passivation procedure is the removal of the PMMA layer from the pads. At the present stage, the PMMA was removed with a swab soaked in acetone (Figure 8.6-c). In further fabrications, a strategy based on a double PMMA/photoresist layer and posterior oxygen plasma could be adopted. This way, after the PMMA patterning by E-beam, a new photolithographic step

[‡] Semi-automatic alignment refers to a manual alignment of the first field and an automatic alignment of the following fields.

[§] Lithography was optimized by Dr. Xavier Borrisé together with the author.

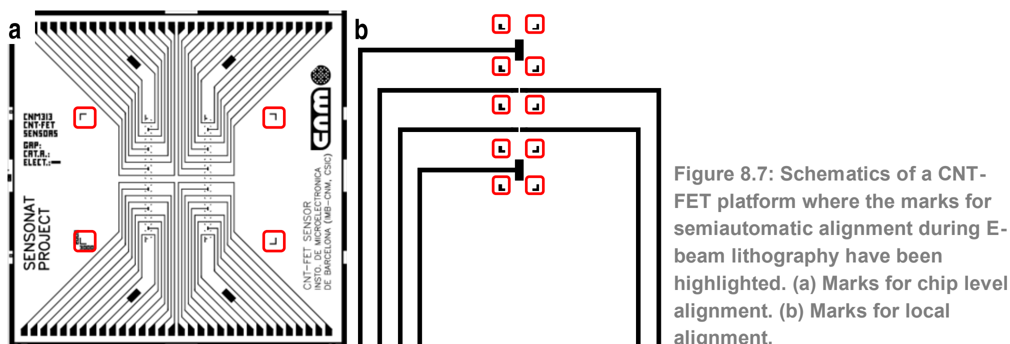


Figure 8.7: Schematics of a CNT-FET platform where the marks for semiautomatic alignment during E-beam lithography have been highlighted. (a) Marks for chip level alignment. (b) Marks for local alignment.

would be performed to pattern the pad areas and then, by oxygen plasma, the PMMA would be etched from the pads. Photoresist would finally be removed with isopropyl alcohol.

B) CNT-FET platform fabrication

The photograph in Figure 8.8 demonstrates the fabrication of the CNT-FET chip platforms on a 4 inch wafer. As described in section 8.1, each wafer contains 234 CNT-FET chips and 4 monitor chips. No problems were encountered in the fabrication except for the 6 chips at the lowest portion of the wafer because of misalignment of the first photolithographic level with respect to the wafer.

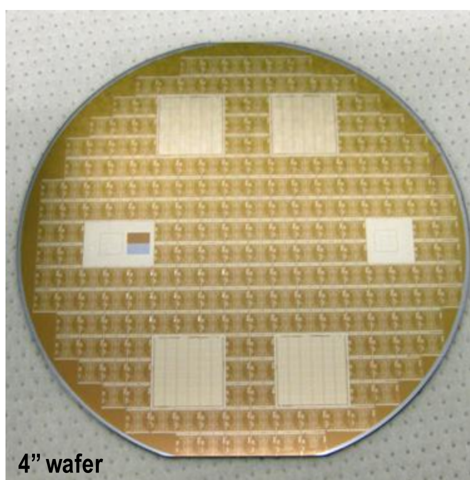


Figure 8.8: Photograph of a 4 inch wafer hosting 234 CNT-FET platforms, and 4 CNT-FET monitor chips.

Figure 8.9-a is an optical image of a CNT-FET sensor chip after the dicing. In this case, the 24 CNT-FETs that are hosted in the chip present a channel length of 1.5 μm, L-shaped electrodes and 2 catalyst areas. The design parameters for this and every chip are indicated at their left side. Figure 8.9-b shows the area of one of the quadrants where the CNT-FET structures and the top electrodes are located. The local alignment marks around each structure are also observed.

Figure 8.10 shows the results from the semi-automatic alignment procedure. The SEM image in Figure 8.10-a shows the two E-beam exposures on an alignment mark for the local field alignment. Figure 8.10-b is the profile that the E-beam system calculates out of the exposures on the alignment marks and uses to perform the local alignment. These profiles are used to adjust the horizontal, the vertical and the angular deviation of the field.

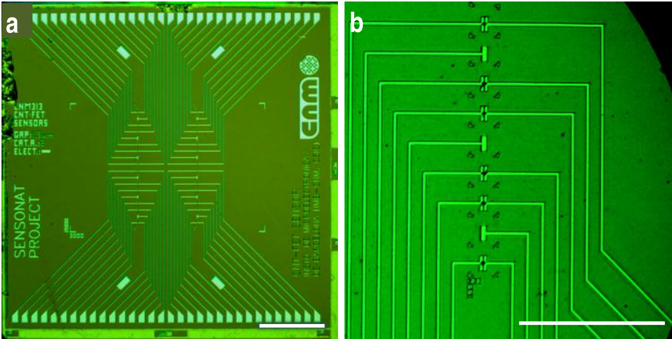


Figure 8.9: Photographs of (a) a CNT-FET platform after dicing and (b) the CNT-FET structures and the top electrodes forming one of the four quadrants of the platform. Scale bars are 1 mm.

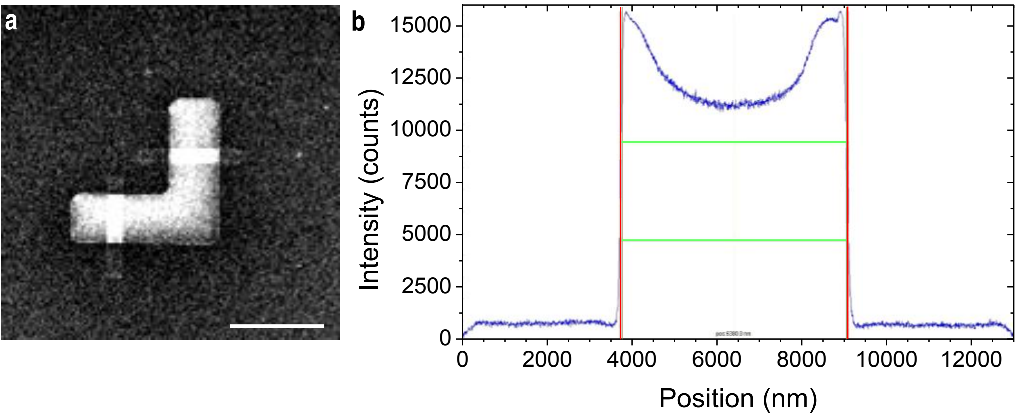


Figure 8.10: (a) SEM image of a local alignment mark where two E-beam exposures had been performed for the field alignment. Scale bar is 10 µm. (b) The profile that the E-beam system calculates out of the exposures on the alignment marks and used to perform the local alignment.

The evaluation of the semi-automatic E-beam lithography demonstrated that the alignment of the patterns was successful except for some cases in which the local alignment marks had been miss-patterned. Figure 8.11-a is a topographic AFM image of an opening. Figure 8.11-b shows the measured profile along the white line on the AFM image. The gap between the metal electrodes forming the structure was measured to be 3 µm and the patterned opening 500 nm. The thickness of the PMMA passivation layer on the channel of the structure was 160 nm.

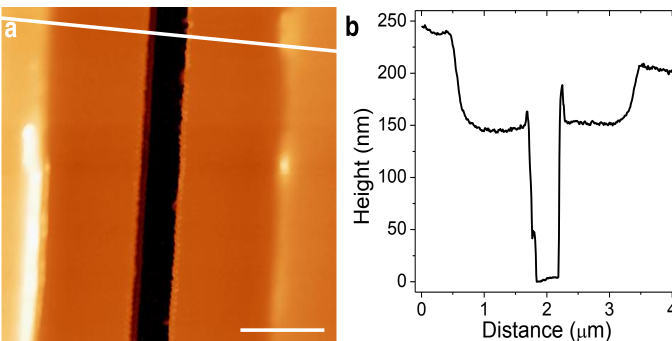


Figure 8.11: (a) Topographic AFM image of an opening that had been patterned by E-beam. (b) Profile along the white line (a). Scale bar is 1 µm. Z amplitude is 250 nm.

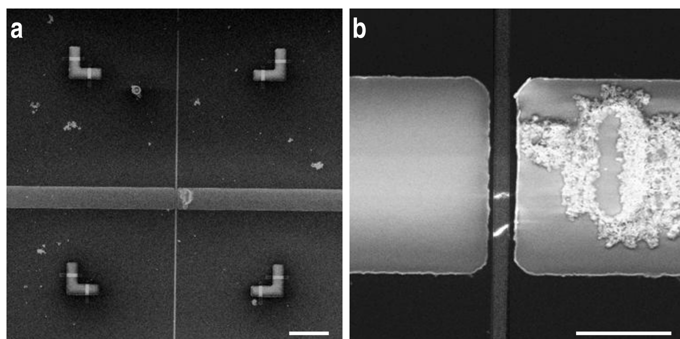


Figure 8.12: SEM images of a CNT-FET structure after the PMMA passivation. The channel length is 1.43 µm and the opening is 800 nm wide.

Figure 8.12 depicts SEM images of a passivated CNT-FET structure. Figure 8.12-a shows the CNT-FET structure and its corresponding local alignment marks, which had been exposed to an E-beam during the process. Figure 8.12-b shows a detail of the device in Figure 8.12-a. The image shows the two metal electrodes, the catalyst particles (below the right side electrode), the two SWCNTs forming the channel and the opening, which had been successfully patterned between the electrodes. According to the images, the channel length for this device is 1.43 µm and the width of the trench is 800 nm.

The optical image in Figure 8.13 shows a sensor chip platform after the automatic E-beam lithography and the removal of the PMMA layer from the pads. The PMMA removal from the pads is mandatory to achieve a good contact between the probe and the pad. The chip in Figure 8.13 is ready to be used for (bio-)electrochemical sensing.

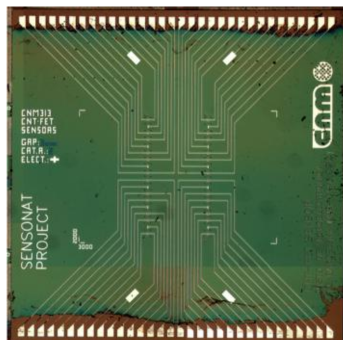


Figure 8.13. Photograph of a sensors chip platform after the CNT-FET structures have been passivated and the PMMA layer has been removed from the pads. The chip is 5 x 5 mm^2.

8.2.2 Conclusions on the fabrication

The fabrication of passivated CNT-FET structures has been proved at 4 inch wafer scale. A wafer contains 238 chips that host 5,616 CNT-FET sensors in total. Conventional process steps have only been used in the fabrication except for the E-beam lithography that is needed, due to the accuracy requests, to open the passivation layer. However, this step has also been optimised so that it can be performed semi-automatically at wafer level.

Regarding the fabrication of the CNT-FET structures, the process has successfully been upgraded (with respect to that proposed in the previous chapter) to overcome the problems related to the metal patterning of short channel CNT-FETs.

Regarding the passivation procedure, even though at this stage the PMMA layer on the pads was removed manually, a procedure for its removal by conventional fabrication processes has been proposed.

8.3 Electrical characterization

Figure 8.14 shows the electrical characteristics of a CNT-FET with semiconducting SWCNT forming its channel. Typically, the I_{ON} and the I_{OFF} current ranges are in the order of µA and pA, respectively. However, the evaluation of the devices did not focus on the analysis of the complete I-V characteristics of the CNT-FET devices but on the identification of their electric characteristic to evaluate the fabrication yields. This analysis was performed, as described in section 7.3.1, by comparing a current trio for each CNT-FET structure. Two major features were evaluated. First, the fabrication yield was compared to that of the monitor chips in the previous chapter. Second, the fabrication yield of the new CNT-FET designs was analysed at wafer level and according to the different designs on the wafer. These analyses were performed before the dicing of the wafer.

Figure 8.14: Typical I_{DS}-V_{GS} characteristics of a CNT-FET with a single semiconductor SWCNT (*functional transistor*).

8.3.1 Overall fabrication yield vs. previous monitor chip fabrication yield

Table 8.3 summarises the results on the identification of the CNT-FET structures for the 24 monitor chips on the wafer with reference RUN4672-Obl.1 (extracted from section 7.3.2), the "previous process yield" column, and the results obtained for one of the monitor chips from the fabricated wafer, *"Upgraded process"* yield. Two major conclusions may be inferred:

First, the percentage of devices identified as *short-circuits* decreased considerably with respect to the

	Previous process yield (%)	Upgraded process yield (%)
Open-circuit	45.51	75.75
Short-circuit	22.38	1.63
Metallic & multi-contacted	23.75	18.87
Functional transistor	7.37	3.75

Table 8.3: Comparison between the previous fabrication yield and yield of the upgraded fabrication monitor chips.

previous results. This evidences that the optimization of the photolithography step leads to a better metal patterning and, thus, that the process optimization woked out.

Second, the table shows that the yield of *functional transistors* is lower than the previously obtained average yield. However, according to Figure 3.21; i.e., the impact of the transistors' location across the wafer on the yield of *functional transistors,* it also evidences the existence of regions where an even lower yield had been obtained.

8.3.2 Statistical analyses on the device identification

Table 8.4 compiles the results obtained from the identification of the CNT-FET sensing structures on a 4 inch wafer. The number of measured chips does not match with that on Table 8.2 because, as discussed in section 8.2.1, there were some chips from designs F and G that did not work.

Figure 8.15 plots the results on the device identification for each CNT-FET structure on the wafer (data extracted from last line on Table 8.4). The pie graph shows that almost 9% of the structures on the CNT-FET chips were labelled as *functional transistor*. This yield improves the yield attained for the fabrication of *functional transistors* on the wafers hosting the monitor chips (section 7.3.2). Regarding the amount of *operative devices* (*functional transistors* plus *metallic and multi-contacted*), 30% of the total devices on the wafer were identified as *operative*. This yield is similar to that obtained in the fabrication of the monitor chips in the previous chapter. Finally, the pie graph also evidences that the metal patterning was successful as the percentage of devices identified as *short circuit* was only 0.57%.

Table 8.4: Summary of the device identification procedure of each CNT-platform. Results are ordered according to the different CNT-FET designs.

	Measured platforms	Measured CNT-FET	Open circuit		Short circuit		Metallic & multi-contacted		Functional transistor	
			Total	%	Total	%	Total	%	Total	%
A [1.5,I,1]	26	624	490	78.53	0	0.00	78	12.50	56	8.94
B [1.5,I,2]	26	624	314	50.32	0	0.00	218	34.94	92	14.74
C [1.5,T,1]	26	624	370	59.30	0	0.00	177	28.37	77	12.34
D [1.5,T,2]	27	648	242	37.35	9	1.39	313	48.30	84	12.96
E [3,I,1]	26	624	614	98.40	1	0.16	4	0.64	5	0.80
F [3,I,2]	23	552	526	95.29	1	0.18	14	2.54	11	1.99
G [3,T,1]	23	552	513	92.94	0	0.00	26	4.71	13	2.36
H [3,T,2]	27	648	379	58.49	17	2.62	151	23.30	101	15.59
TOTAL	**204**	**4896**	**3448**	**70.42**	**28**	**0.57**	**981**	**20.04**	**439**	**8.97**

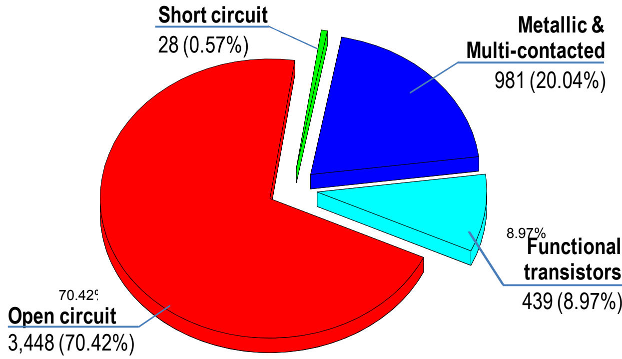


Figure 8.15. Pie graph showing the distribution of the different electric characteristics of the CNT-FETs on the platforms.

8.3.3 Influence of the design parameters on the fabrication yield

The bar graph in Figure 8.16 shows the percentage of *operative devices* for the 8 different designs on the wafer (A-H). The design with the highest yield of *functional transistors* (more than 15%) is design H (2 catalyst areas, T-shape electrodes and 3 µm channel). Yields close to or higher than 10% were also attained on the designs where the channel length was 1.5 µm (designs A-D). The maximum yield of *metallic and multi-contacted* devices was 48.30% for design D.

The comparison of the yields for the different design parameters is depicted in Figure 8.17. Regarding the channel length, it is evident that higher yields were obtained for 1.5 µm channel lengths. The data in Figure 8.17 is in accordance with the data from the monitor chips and indicates that the CNT synthesis process led to SWCNTs that were, typically, shorter than 5 µm (5 µm is the length of the longest channel (3 µm) plus the distance between the catalyst area and the border of the electrode (2 µm)). Concerning the shape of the electrodes, the yields for T-shaped electrode CNT-FETs were higher than those of L-shaped electrode devices (C vs. A; D vs. B; G vs. E and H vs. E). Regarding the number of catalyst areas, yields for the design involving two catalyst areas were found to be higher.

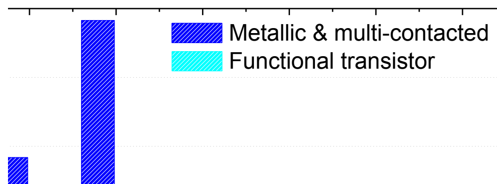


Figure 8.16: Distribution of the *functional transistors* and the *metallic and multi-contacted* devices according to the different CNT-FET designs.

Figure 8.17: Distribution of the *functional transistors* and the *metallic and multi-contacted* devices according to the CNT-FET design parameters.

A) Influence of the E-beam exposure on the I-V characteristics of the CNT-FETs

The influence of E-beam irradiation on the CNT-FETs during the passivation step was analysed for process optimization reasons. This analysis consisted of the comparison of the I_{DS}-V_{GS} characteristics of pre-selected devices before and after their irradiation.

Figure 8.18 plots the electric characteristics of a functional transistor **before** and **after** the E-beam lithography had been performed. The graph shows that the electric characteristic of the CNT-FETs shifts because the silicon dioxide under the SWCNTs traps electrons coming from the irradiation. However, this is a transient effect that disappeared after some days. The obtained results are in accordance with those obtained from the experiments on the influence on an E-beam exposure of SWCNTs on CNT-FET structures [50].

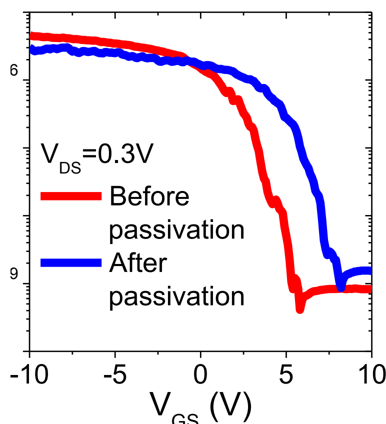


Figure 8.18: I_{DS} vs. V_{GS} characteristics of a CNT-FET before and after E-beam exposure.

8.3.4 Conclusions on the electric characterization

The characterization of the CNT-FETs was based on the automatic identification of the devices. This identification was performed at wafer level before the CNT-FET passivation procedure. The analysis has given evidence of the fabrication yield improvement since, in comparison to the fabrication of the

monitor chips in the previous chapter, fewer structures were identified as *short circuit* and the yield of *functional transistors* has become higher. Moreover, the yield for *functional transistors* could have been higher since unexpected short growth of the SWCNTs decreased the yield for the CNT-FET designs with 3 μm channel length. Besides, the influence of the E-beam has been checked to confirm it did not cause permanent damage to the devices.

8.4 Electrochemical sensing with the passivated CNT-FET sensors

The electric characteristics of the SWCNTs provide the CNT-FET devices with very attractive possibilities for the label free bio-electrochemical recognition in which no additional modification of the analyte is needed. Therefore, different groups have been interested in the use of the fabricated CNT-FET platforms. In particular, the platforms are being employed in bio-recognition and in environmental detection experiments.

8.4.1 Bio-sensing analyses based on passivated CNT-FETs

The group of Sensors and Biosensors of the *Universitat Autònoma de Barcelona* (UAB) is specialised on the study of new materials for electrochemical transduction and on the development on sensors based on those materials [51-54]. Now, they are employing the CNT-FET platforms for the bio-detection of proteins. They aim at developing novel strategies for the functionalization of the SWCNTs by aptamers as a route to improve the recognition that can be performed by a functionalization with antibodies.

Aptamers, which are artificial specific oligonucleotides, can bind to the proteins with high selectivity and with an affinity for their targets comparable or even higher than their monoclonal antibody counterparts. Regarding the sensing FET technology, the aptamers may contribute to the detection since, opposite to what happens with the antibodies, their length may be shorter than the Debye length and so, the binding event between the aptamers and the target proteins can occur within the electrical double layer. Thus, changes in the charge distribution close to the CNT may be detected more easily. Figure 8.19 shows a schematic of the main steps of the functionalization of the SWCNTs and a preliminary calibration curve for the detection of thrombin. Passivated CNT-FETs appear to be highly sensitive to very low analyte concentrations.

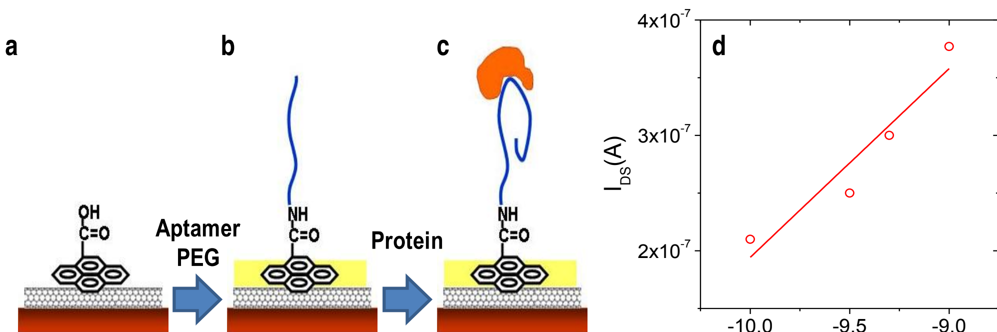


Figure 8.19: (a-c) Schematic of the SWCNT functionalization and the protein detection: (a) immobilization of the pyrene-COOH linkers to the SWCNTs and the blocking agent (PEG); (b) covalent attachment of the NH_2-aptamer via an amide bond formation; (c) protein detection. (d) Calibration curve of the drain current against thrombin concentration for the detection of thrombin (V_{GS}= 1 V; V_{DS}= 0.3 V). The figures are courtesy of Mercè Pacios.

8.4.2 Environmental analysis based on passivated CNT-FETs

The *Quimiometría y Cualimetría* group at URV is involved in the functionalization of SWCNTs by biological receptors to detect molecules that have an important role in the biochemistry of the human beings and to detect pathogen agents like some bacteria [40, 55, 56].

Recently, the group has developed a fast and selective CNT-FET biosensor based on arrays of SWCNTs for the detection of Biphenol A (BPA), an organic compound that is used in the synthesis of several important plastics and plastic additives. Since it is suspected of being hazardous to humans, the use of BPA in consumer products is regulated [40]. The evaluation of their biosensor demonstrated a sensibility of $2.19 \cdot 10^{-7}$ M, which is below the US-EPA reference dose for humans (50 $\mu g \cdot kg^{-1} \cdot day^{-1}$) and also below the concentrations reported by previous methods in the literature [57-59].

The group is currently using the passivated CNT-FET chips to exploit the ultimate performance of a single SWCNT CNT-FET sensor and to investigate if the detection limits can be further improved.

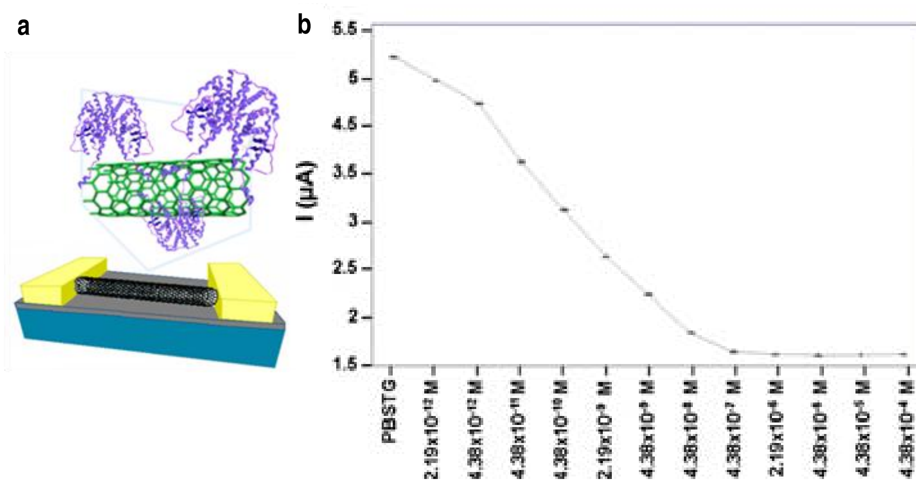


Figure 8.20: (a) Schematic of the CNT-FET sensor after its functionalization with estrogens. (b) Behaviour of the I_{DS} vs. the BPA concentration. The gate voltage was set to -5 V. Figures extracted from [40].

Chapter conclusions

This chapter has dealt with the development of a CNT-FET platform to be used for electrochemical sensing. Developed tasks have comprised the design and the fabrication of the CNT-FET platform and the testing of the CNT-FET structures.

Regarding the design of the chip platform:

- A chip containing 24 back-gate actuated CNT-FET structures and 12 liquid polarization electrodes has been designed for electrochemical sensing. 8 different CNT-FETs have been designed in order to analyse the impact on the optimal yield of 3 key parameters: the channel length, the channel shape and the number of catalyst areas.

Regarding the fabrication of the chip platforms:

- Fabrication of the structures has been proved at 4 inch wafer scale. A 4 inch wafer hosts 238 chips that include, in total, 5,616 CNT-FET structures.
- The fabrication process of the CNT-FETs has been upgraded with respect to the process presented in the previous chapter to overcome the problems related to the patterning of the metal electrode on short channel CNT-FETs.
- A procedure based on PMMA coating and a posterior E-beam lithography has been optimised for the passivation of the SWCNTs forming the channels of the CNT-FETs. The E-beam lithography has been optimised in order to get a semi-automatic wafer level scalable process.

Regarding the test of the chip platforms:

- The automatic identification procedure of the CNT-FET structures showed a yield of *functional transistors* of 9%. This yield improves that of the previous chapter, which was 7%. The improvement of yield of *short circuits* (1.6% against 22.4%) proves that the metal patterning step upgrade was successful.
- The evaluation of the CNT-FET design parameters has determined their influence on the device fabrication yield. In addition, this analysis has also revealed an unexpected short growth of the SWCNTs.
- The influence of the E-beam irradiation on the SWCNTs has proved to be transient as the electric characteristics of the CNT-FET are recovered after some days.

In conclusion, this chapter reports an upgrade of the fabrication of CNT-FET structures at wafer level. In this case, the objective was the fabrication of CNT-FET based devices for electrochemical sensing and thus, a semi-automatic lithography procedure has been developed to passivate the CNT-FETs. The procedure could be eventually used for the deposition/removal of layers on/from the CNT-FETs for the fabrication of either a new contact on the SWCNTs, top gate actuated CNT-FETs or SWCNT based NEMS.

Outlook

This section reports a technological process and related upgrades for the wafer scale integration of SWCNTs into CNT-FET based devices and a procedure for their automatic testing and identification. It has to be highlighted that only conventional microelectronic steps are used in the fabrication of the structures, except for the passivation procedure, which is performed by E-beam lithography, due to precision requests. This process was optimised in order to be automatically scaled to wafer level.

In particular, the section has focused on the development of a monitor chip to evaluate the synthesis of SWCNTs and the fabrication of CNT-FETs, and on the development of a platform for electrochemical sensing based on passivated CNT-FET structures. The technological processes have resulted in the fabrication of more than 10,000 CNT-FETs on a 4 inch wafer. The fabrication yield of *functional transistors* has reached 25% for the optimal CNT-FET designs. These results highly improve those reported in the recent literature. Apart from the monitor chip and the CNT-FET based sensors, the developed technology has also been used for the fabrication of other SWCNT based devices, which have not been described in these chapters because the experiments have not been concluded yet.

Even if the results on the fabrication of devices based on the CNT-FET fabrication technological process have been very promising, the process and the testing procedure may be further improved.

Regarding SWCNT synthesis, the control on their structure and growth orientation (the two major challenges on SWCNT integration to fabricate CNT-FET structures) has not been faced yet. Although it was expected that the use of zeolite crystals, as SWCNT support, would lead to overcome these problems, difficulties to control SWCNT growth from these particles has hindered their use until now. Besides, future efforts should also be oriented towards the optimization of the SWCNT-metal contact to reduce the contact resistance and to gain control over the electric characteristic of the CNT-FETs. With respect to the testing procedure, it could be upgraded for a more complete characterization of the structures and to optimise the fabrication yields by applying a current to burn out the *metallic* SWCNTs.

In conclusion, this technological process is a step forward to the VLSI of CNTs. The developed technological process is of interest for the wafer scale, batch and massive fabrication of CNT-FET based nanoelectronics, sensors and NEMS. Furthermore, it has been proved that the developed technological process may be used for the integration of CNTs into other systems different from a FET.

References

1. International Technology Roadmap for Semiconductors, http://www.itrs.net/
2. P. Avouris, Z.H. Chen, and V. Perebeinos, Carbon-based electronics, Nature Nanotechnology, 2007. **2**(10): p. 605-615.
3. J.W.G. Wildoer, L.C. Venema, A.G. Rinzler, R.E. Smalley, and C. Dekker, Electronic structure of atomically resolved carbon nanotubes, Nature, 1998. **391**(6662): p. 59-62.
4. A. Javey, J. Guo, D.B. Farmer, Q. Wang, D. Wang, R.G. Gordon, M. Lundstrom, and H. Dai, Carbon nanotube field-effect transistors with integrated ohmic contacts and high-k gate dielectrics, Nano Letters, 2004. **4**(3): p. 447-450.
5. M. Shim, A. Javey, N.W.S. Kam, and H. Dai, Polymer functionalization for air-stable n-type carbon nanotube field-effect transistors [9], Journal of the American Chemical Society, 2001. **123**(46): p. 11512-11513.
6. R. Martel, T. Schmidt, H.R. Shea, T. Hertel, and P. Avouris, Single- and multi-wall carbon nanotube field-effect transistors, Applied Physics Letters, 1998. **73**(17): p. 2447-2449.
7. S.J. Tans, A.R.M. Verschueren, and C. Dekker, Room-temperature transistor based on a single carbon nanotube, Nature, 1998. **393**(6680): p. 49-52.
8. P.C. Collins, M.S. Arnold, and P. Avouris, Engineering carbon nanotubes and nanotube circuits using electrical breakdown, Science, 2001. **292**(5517): p. 706-709.
9. A. Javey, H. Kim, M. Brink, Q. Wang, A. Ural, J. Guo, P. McIntyre, P. McEuen, M. Lundstrom, and H.J. Dai, High-kappa dielectrics for advanced carbon-nanotube transistors and logic gates, Nature Materials, 2002. **1**(4): p. 241-246.
10. A. Javey, J. Guo, Q. Wang, M. Lundstrom, and H.J. Dai, Ballistic carbon nanotube field-effect transistors, Nature, 2003. **424**(6949): p. 654-657.
11. Z.H. Chen, J. Appenzeller, J. Knoch, Y.M. Lin, and P. Avouris, The role of metal-nanotube contact in the performance of carbon nanotube field-effect transistors, Nano Letters, 2005. **5**(7): p. 1497-1502.
12. Y.C. Tseng, K. Phoa, D. Carlton, and J. Bokor, Effect of diameter variation in a large set of carbon nanotube transistors, Nano Letters, 2006. **6**(7): p. 1364-1368.
13. H.T. Soh, C.F. Quate, A.F. Morpurgo, C.M. Marcus, J. Kong, and D. Hongjie, Integrated nanotube circuits: Controlled growth and ohmic contacting of single-walled carbon nanotubes, Applied Physics Letters, 1999. **75**(5): p. 627-629.
14. A. Bachtold, P. Hadley, T. Nakanishi, and C. Dekker, Logic circuits with carbon nanotube transistors, Science, 2001. **294**(5545): p. 1317-1320.
15. V. Derycke, R. Martel, J. Appenzeller, and P. Avouris, Carbon Nanotube Inter- and Intramolecular Logic Gates, Nano Letters, 2001. **1**(9): p. 453-456.

16. Z.H. Chen, J. Appenzeller, Y.M. Lin, J. Sippel-Oakley, A.G. Rinzler, J.Y. Tang, S.J. Wind, P.M. Solomon, and P. Avouris, An integrated logic circuit assembled on a single carbon nanotube, Science, 2006. **311**(5768): p. 1735-1735.

17. Y.C. Tseng, P.Q. Xuan, A. Javey, R. Malloy, Q. Wang, J. Bokor, and H.J. Dai, Monolithic integration of carbon nanotube devices with silicon MOS technology, Nano Letters, 2004. **4**(1): p. 123-127.

18. H. Lin, Y.W. Park, and S. Tiwari, A compact single-walled carbon nanotube transistor integrated with a silicon MOSFET using a single common gate, in Materials Research Society Symposium Proceedings. 2006. p. 101-105.

19. A. Vijayaraghavan, S. Blatt, D. Weissenberger, M. Oron-Carl, F. Hennrich, D. Gerthsen, H. Hahn, and R. Krupke, Ultra-Large-Scale Directed Assembly of Single-Walled Carbon Nanotube Devices, Nano Letters, 2007. **7**(6): p. 1556-1560.

20. D. Akinwande, S. Yasuda, B. Paul, S. Fujita, G. Close, and H.S. Philip Wong, Monolithic integration of CMOS VLSI and carbon nanotubes for hybrid nanotechnology applications, IEEE Transactions on Nanotechnology, 2008. **7**(5): p. 636-639.

21. R. Krupke, F. Hennrich, H.B. Weber, M.M. Kappes, and H.v. Löhneysen, Simultaneous Deposition of Metallic Bundles of Single-walled Carbon Nanotubes Using Ac-dielectrophoresis, Nano Letters, 2003. **3**(8): p. 1019-1023.

22. M.S. Arnold, A.A. Green, J.F. Hulvat, S.I. Stupp, and M.C. Hersam, Sorting carbon nanotubes by electronic structure using density differentiation, Nature Nanotechnology, 2006. **1**(1): p. 60-65.

23. K. Ryu, A. Badmaev, C. Wang, A. Lin, N. Patil, L. Gomez, A. Kumar, S. Mitra, H.S.P. Wong, and C. Zhou, CMOS-Analogous Wafer-Scale Nanotube-on-Insulator Approach for Submicrometer Devices and Integrated Circuits Using Aligned Nanotubes, Nano Letters, 2008. **9**(1): p. 189-197.

24. S.J. Kang, C. Kocabas, T. Ozel, M. Shim, N. Pimparkar, M.A. Alam, S.V. Rotkin, and J.A. Rogers, High-performance electronics using dense, perfectly aligned arrays of single-walled carbon nanotubes, Nature Nanotechnology, 2007. **2**(4): p. 230-236.

25. E.S. Snow, J.P. Novak, P.M. Campbell, and D. Park, Random networks of carbon nanotubes as an electronic material, Applied Physics Letters, 2003. **82**(13): p. 2145-2147.

26. K. Ryu, A. Badmaev, C. Wang, A. Lin, N. Patil, L. Gomez, A. Kumar, S. Mitra, H.S.P. Wong, and C. Zhou, CMOS-Analogous Wafer-Scale Nanotube-on-Insulator Approach for Submicrometer Devices and Integrated Circuits Using Aligned Nanotubes, Nano Letters, 2009. **9**(1): p. 189-197.

27. P. Avouris, M. Freitag, and V. Perebeinos, Carbon-nanotube photonics and optoelectronics, Nature Photonics, 2008. **2**(6): p. 341-350.

28. J.A. Misewich, R. Martel, P. Avouris, J.C. Tsang, S. Heinze, and J. Tersoff, Electrically Induced Optical Emission from a Carbon Nanotube FET, Science, 2003. **300**(5620): p. 783-786.

29. M. Freitag, Y. Martin, J.A. Misewich, R. Martel, and P. Avouris, Photoconductivity of Single Carbon Nanotubes, Nano Letters, 2003. **3**(8): p. 1067-1071.

30. J. Chen, V. Perebeinos, M. Freitag, J. Tsang, Q. Fu, J. Liu, and P. Avouris, Bright Infrared Emission from Electrically Induced Excitons in Carbon Nanotubes, Science, 2005. **310**(5751): p. 1171-1174.

31. E. Adam, C.M. Aguirre, L. Marty, B.C. St-Antoine, F. Meunier, P. Desjardins, D. Ménard, and R. Martel, Electroluminescence from Single-Wall Carbon Nanotube Network Transistors, Nano Letters, 2008. **8**(8): p. 2351-2355.

32. J.P. Novak, E.S. Snow, E.J. Houser, D. Park, J.L. Stepnowski, and R.A. McGill, Nerve agent detection using networks of single-walled carbon nanotubes, Applied Physics Letters, 2003. **83**(19): p. 4026-4028.

33. E.S. Snow, F.K. Perkins, E.J. Houser, S.C. Badescu, and T.L. Reinecke, Chemical detection with a single-walled carbon nanotube capacitor, Science, 2005. **307**(5717): p. 1942-1945.

34. A. Star, V. Joshi, S. Skarupo, D. Thomas, and J.C.P. Gabriel, Gas sensor array based on metal-decorated carbon nanotubes, Journal of Physical Chemistry B, 2006. **110**(42): p. 21014-21020.

35. D.R. Kauffman and A. Star, Carbon nanotube gas and vapor sensors, Angewandte Chemie - International Edition, 2008. **47**(35): p. 6550-6570.

36. A. Star, E. Tu, J. Niemann, J.C.P. Gabriel, C.S. Joiner, and C. Valcke, Label-free detection of DNA hybridization using carbon nanotube network field-effect transistors, Proceedings of the National Academy of Sciences of the United States of America, 2006. **103**(4): p. 921-926.

37. X. Tang, S. Bansaruntip, N. Nakayama, E. Yenilmez, Y.-l. Chang, and Q. Wang, Carbon Nanotube DNA Sensor and Sensing Mechanism, Nano Letters, 2006. **6**(8): p. 1632-1636.

38. B.L. Allen, P.D. Kichambare, and A. Star, Carbon nanotube field-effect-transistor-based biosensors, Advanced Materials, 2007. **19**(11): p. 1439-1451.

39. M.T. Martínez, Y.C. Tseng, N. Ormategui, I. Loinaz, R. Eritja, and J. Bokor, Label-free DNA biosensors based on functionalized carbon nanotube field effect transistors, Nano Letters, 2009. **9**(2): p. 530-536.

40. Z.C. Sanchez-Acevedo, J. Riu, and F.X. Rius, Fast picomolar selective detection of bisphenol A in water using a carbon nanotube field effect transistor functionalized with estrogen receptor-Î±, Biosensors and Bioelectronics, 2009. **24**(9): p. 2842-2846.

41. A.M. Fennimore, T.D. Yuzvinsky, W.-Q. Han, M.S. Fuhrer, J. Cumings, and A. Zettl, Rotational actuators based on carbon nanotubes, Nature, 2003. **424**(6947): p. 408-410.

42. C. Hierold, A. Jungen, C. Stampfer, and T. Helbling, Nano electromechanical sensors based on carbon nanotubes, Sensors and Actuators, A: Physical, 2007. **136**(1): p. 51-61.

43. K. Jensen, K. Kim, and A. Zettl, An atomic-resolution nanomechanical mass sensor, Nature Nanotechnology, 2008. **3**(9): p. 533-537.

44. B. Lassagne, D. Garcia-Sanchez, A. Aguasca, and A. Bachtold, Ultrasensitive mass sensing with a nanotube electromechanical resonator, Nano Letters, 2008. **8**(11): p. 3735-3738.

45. B. Lassagne, Y. Tarakanov, J. Kinaret, G.S. David, and A. Bachtold, Coupling mechanics to charge transport in carbon nanotube mechanical resonators, Science, 2009. **325**(5944): p. 1107-1110.

46. A. Barreiro, R. Rurali, E.R. Hernandez, J. Moser, T. Pichler, L. Forro, and A. Bachtold, Subnanometer Motion of Cargoes Driven by Thermal Gradients Along Carbon Nanotubes, Science, 2008. **320**(5877): p. 775-778.

47. International Technology Roadmap for Semiconductors, http://www.itrs.net/.

48. A. Jorio, G. Dresselhaus, and M.S. Dresselhaus, Carbon Nanotubes: Advanced Topics in the Synthesis, Structure, Properties and Applications. 2008, New York: Springer.

49. P.J. de Pablo, C. Gómez-Navarro, J. Colchero, P.A. Serena, J. Gómez-Herrero, and A.M. Baró, Nonlinear Resistance versus Length in Single-Walled Carbon Nanotubes, Physical Review Letters, 2002. **88**(3): p. 036804.

50. G. Rius, I. Martin, P. Godignon, A. Bachtold, J. Bausells, E. Lora-Tamayo, and F. Perez-Murano, Response of carbon nanotube transistors to electron beam exposure, Microelectronic Engineering, 2007. **84**(5-8): p. 1596-1600.

51. B. Pérez, M. Pumera, M. Del Valle, A. Merkoçi, and S. Alegret, Glucose biosensor based on carbon nanotube epoxy composites, Journal of Nanoscience and Nanotechnology, 2005. **5**(10): p. 1694-1698.

52. M.J. Esplandiu, M. Pacios, E. Bellido, and M. Del Valle, Carbon nanotubes and electrochemistry, Zeitschrift fur Physikalische Chemie, 2007. **221**(9-10): p. 1161-1173.

53. M. Pacios, M. del Valle, J. Bartroli, and M.J. Esplandiu, Electrochemical behavior of rigid carbon nanotube composite electrodes, Journal of Electroanalytical Chemistry, 2008. **619-620**(1-2): p. 117-124.

54. A. Bonanni, M.J. Esplandiu, and M. del Valle, Impedimetric genosensors employing COOH-modified carbon nanotube screen-printed electrodes, Biosensors and Bioelectronics, 2009. **24**(9): p. 2885-2891.

55. R.A. Villamizar, A. Maroto, F.X. Rius, I. Inza, and M.J. Figueras, Fast detection of Salmonella Infantis with carbon nanotube field effect transistors, Biosensors and Bioelectronics, 2008. **24**(2): p. 279-283.

56. G.A. Zelada-Guillen, J. Riu, A. Düzgün, and F.X. Rius, Immediate detection of living bacteria at ultralow concentrations using a carbon nanotube based potentiometrie aptasensor, Angewandte Chemie - International Edition, 2009. **48**(40): p. 7334-7337.

57. D.E. Walsh, P. Dockery, and C.M. Doolan, Estrogen receptor independent rapid non-genomic effects of environmental estrogens on $[Ca^{2+}]_i$ in human breast cancer cells, Molecular and Cellular Endocrinology, 2005. **230**(1-2): p. 23-30.

58. A. Zsarnovszky, H.H. Le, H.-S. Wang, and S.M. Belcher, Ontogeny of Rapid Estrogen-Mediated Extracellular Signal-Regulated Kinase Signaling in the Rat Cerebellar Cortex: Potent Nongenomic Agonist and Endocrine Disrupting Activity of the Xenoestrogen Bisphenol A, Endocrinology, 2005. **146**(12): p. 5388-5396.

59. A.L. Wozniak, N.N. Bulayeva, and C.S. Watson, Xenoestrogens at Picomolar to Nanomolar Concentrations Trigger Membrane Estrogen Receptor$-\alpha$ Mediated Ca^{2+} Fluxes and Prolactin Release in GH3/B6 Pituitary Tumor Cells, Environ Health Perspect, 2005. **113**(4).

SECTION 4:
WAFER SCALE INTEGRATION OF DENSE ARRAYS OF CNTs INTO ELECTRODES

This section addresses the wafer scale integration of dense arrays of CNTs into the metallic electrodes of the Impedance Needles and the Multi-Electrode-Arrays (MEAs) from the Bio-Applications Group (*Grupo de Aplicaciones Biomédicas*, GAB) at CNM, which are aimed at in-vitro or in-vivo bio-impedance measurements, respectively.

Even if the bio-sensing devices from GAB have been demonstrated to be sensitive enough for the applications for which they are aimed at, the fact that the last steps of the fabrication need to be performed manually and at chip level hinders the device fabrication yield. In this sense, the development of a process to improve the electrode-electrolyte interface based on standard microelectronic steps is of great interest. Regarding the device fabrication, the process should be wafer scalable to achieve a high reproducibility and a high throughput. Furthermore, as the electrodes are intended for bio-applications, the materials involved in their fabrication should be bio-compatible. Regarding the electrochemical response of the electrodes, the process should result in the improvement of the life time and the stability of the electrodes and should also reduce the parasitic resistance of the electrode-electrolyte interface.

The section is divided in two main chapters. The first chapter is devoted to overview the key factors related to the fabrication of electrodes, bio-electrochemical sensing and the benefits from the CNT integration. The second section is devoted to the upgrade of the process for the fabrication of multi-electrode devices previously demonstrated by GAB. This upgrade addresses the design of the process for the integration of the CNTs, the fabrication of the electrodes and their characterization.

Index of Section 4

9 Introduction to bio-electrochemical applications based on electrode devices 167

9.1 Key points of the (bio-)electrochemical sensing based on electrodes 167

9.2 Carbon nanotube based electrodes 168

9.2.1 CNTs as a material for electrochemical sensing 168

9.2.2 Modification of electrodes based on CNT 168

9.2.3 Fabrication of CNT modified electrodes 170

Challenges 170

10 Carbon nanotube modified electrodes for bio-impedance applications 171

10.1 The bio-sensing devices from GAB 171

10.1.1 Electrode fabrication 173

10.1.2 Improvement of the electrode impedance 173

10.1.3 Electrode performance 175

10.2 Integration of carbon nanotubes into metallic electrodes 176

10.2.1 Technological process for the integration of the CNTs 176

10.2.2 Results of the fabrication 178

10.2.3 Conclusions on the fabrication 180

10.3 Characterization of the carbon nanotube-modified electrodes 180

10.3.1 Mechanical stability of the CNT layer 180

10.3.2 Electrical continuity 185

10.3.3 Electrochemical characteristic of the electrodes 186

10.3.4 Conclusions on the electrode characterization 190

10.4 The MWCNT modified electrodes vs. the previous electrodes from GAB 190

10.4.1 Fabrication yield comparison 190

10.4.2 Electrochemical characteristic comparison 192

10.4.3 Conclusions on the performance of the MWCNT modified electrodes 193

10.5 Other experiments based on the MWCNT modified electrodes 193

10.5.1 Bio-compatibility of the MWCNT modified electrodes 194

10.5.2 CNTs functionalization for label free electrochemical bio-detection 194

10.5.3 Study on the emergent activity in cortical networks 195

Chapter conclusions 197

Outlook 199

References 200

9
Introduction to bio-electrochemical applications based on electrode devices

As discussed previously (Sections 1.2 and 6.3), CNTs present very attractive electrical, chemical and mechanical properties for the development of chemical sensors, in general, and for electrochemical detection, in particular.

This chapter briefly overviews the main principles on the fabrication of electrodes for bio-electrochemical sensing and introduces the benefits CNTs may confer to these devices.

9.1 Key points of the (bio-)electrochemical sensing based on electrodes

The key issues on a (bio-)electrochemical device are those related to the interface between the sensing element and the analyte, that is, those related to the electrode (Figure 9.1). Therefore, the right choices of the electrode morphology, of its material and, in the case of bio-sensors, of its surface functionalization, are the key to the successful performance of any bio-electrochemical device.

The morphology of the electrode and the distribution of the electrode array is one of the first key factors that have to be taken into account. The bigger the surface of the electrode, the more sensitive it will result. However, the bigger the electrode, the lower it will be its spatial resolution. Therefore, strategies to improve its effective area so that the sensitivity is improved without affecting the spatial resolution are usually performed [1], for example, the electrochemical deposition of a metal coating [2-4]. Regarding the electrode distribution, there are 3 main electrode configurations, the interdigitated electrode configuration, the isolated electrodes configuration and the multi-electrode-array (MEAs) configuration. In the case of the MEAs, the array may be formed of isolated electrodes or of an array of electrode connected to one sole metal pad.

Besides the electrodes' morphology and their configuration, the selection of the material the electrodes or the top surface are made of is critical as it must fulfil other requests such as to be stable at the conditions the measurements take place, for example in liquid or if inserted into tissue, and it

Figure 9.1: Schematic of an electrode and its corresponding stripe. The electrode has been drawn rougher to exemplify the importance of its surface.

must be compatible with the device fabrication process. Additionally, depending on the application, other concerns must be taken into consideration. In the case of bio-sensors, for example, the capacity of that material to be functionalised must also be taken into account [5]. Furthermore, if the device is to get in touch with a living tissue, for example, in the cases of cellular stimulation and/or recording or the insertion of the electrodes into a living tissue [6], it will be necessary to avoid any bio-toxicity by using only bio-compatible materials in the fabrication of the devices. Materials such as gold, platinum, iridium, titanium, titanium nitride or carbon are often used in the fabrication of electrodes.

9.2 Carbon nanotube based electrodes

Different allotropes of carbon such as graphite, glassy carbon and carbon black are materials that have been frequently use in bio-electrochemistry for the past years in applications such as energy storage in batteries and supercapacitors, for metal production and as catalyst supports due to their electrochemical properties [7-9]. These materials provide, in general, good electrical conductivity, high thermal and mechanical stability, a wide operable potential window with slow oxidation kinetics and, in many cases, electrocatalytical activity [10].

9.2.1 CNTs as a material for electrochemical sensing

Since CNTs came to prominence [11] their use has been boosted in an unprecedented way for electrochemical and electroanalytical applications [12-15]. Such interest on CNTs is related to their size and their structure, which result in a high active area, and to their electro-catalytic anisotropy (of the tip with respect to the walls and vice versa). Moreover, the fact that different electrode morphologies can be fabricated and the fact that CNTs can be functionalised by different strategies [5] favours the fabrication of targeted CNT based sensors.

However, as in the applications in the previous section (Chapters 1 and 3), the not totally controlled synthesis of the CNTs hinders not only the standardization of the fabrication processes, but also the CNT modification procedures and the electrochemical characteristics of the devices since it has been demonstrated that they strongly depend on the structure of the CNTs [16]. This way, for example, bamboo like CNTs are much more electroactive than perfect in structure and big in diameter MWCNTs.

In the same sense, the structure of the CNTs is relevant for their bio-compatibility, which is still unresolved [17-23]. On the one side, it has been demonstrated that, sometimes, when CNTs are inserted into the body, they may act as asbestos fibres [21]. On the other side, CNTs have been demonstrated as a bio-compatible material, for example, for the fabrication of implants [17, 18] and to enhance the recording of the signal form neurons [20, 22]. Furthermore, other studies involving cell culture on CNTs did not find any non-compatibility of the CNTs and the cells [19].

9.2.2 Modification of electrodes based on CNT

Besides the CNT structure, the procedure to integrate the CNTs strongly affects the characteristic of the electrodes since it will determine its roughness and the alignment of the CNTs and their edges. The two most extended routes to integrate the CNTs are a direct deposition of the CNTs either from a solution [24] (Figure 9.2-a), by a CNT-polymer paste [16, 25] (Figure 9.2-b) or screen printing, and in the selective synthesised of the CNTs on the electrodes [19, 26, 27] (Figure 9.2-c,d). In the first case, deposited CNTs will typically lay parallel to the surface. In the second case, after the optimization of the CNT synthesis conditions, vertical alignment of the CNTs is achievable. As shown in Figure 9.2-d, this process may result in the fabrication of single CNT electrodes [26]. There exists a third case were

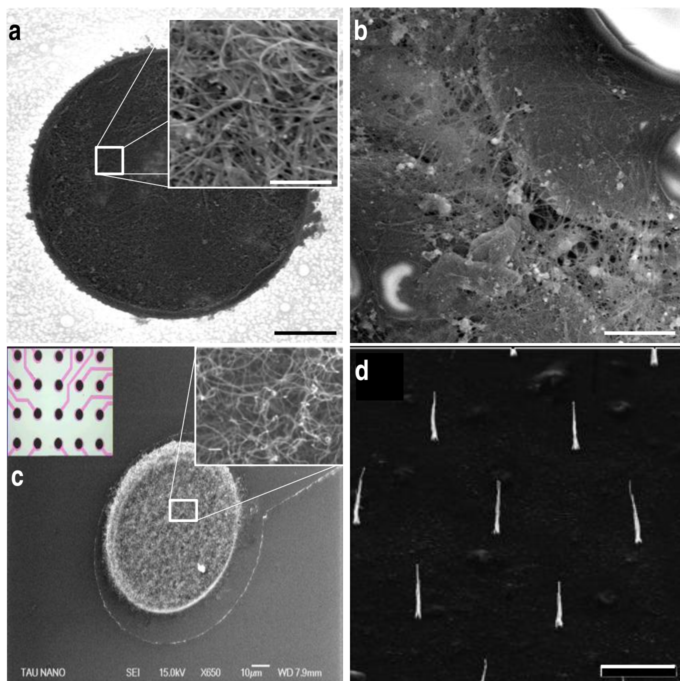


Figure 9.2: Examples of different electrodes where the CNT modification consisted of (a) manually deposited SWCNTs; (b) a CNT-polyestirene composite; (c-d) selectively synthesised on the electrodes arrays and single MWCNTs, respectively. Scalebars are 500 μm, and 5 μm in a, 1 μm in b, 10 μm and 100 nm in c and 5 μm in d. (a-b) courtesy of Dr. G. Gabriel. (c-d) and extracted from [19] and [26], respectively.

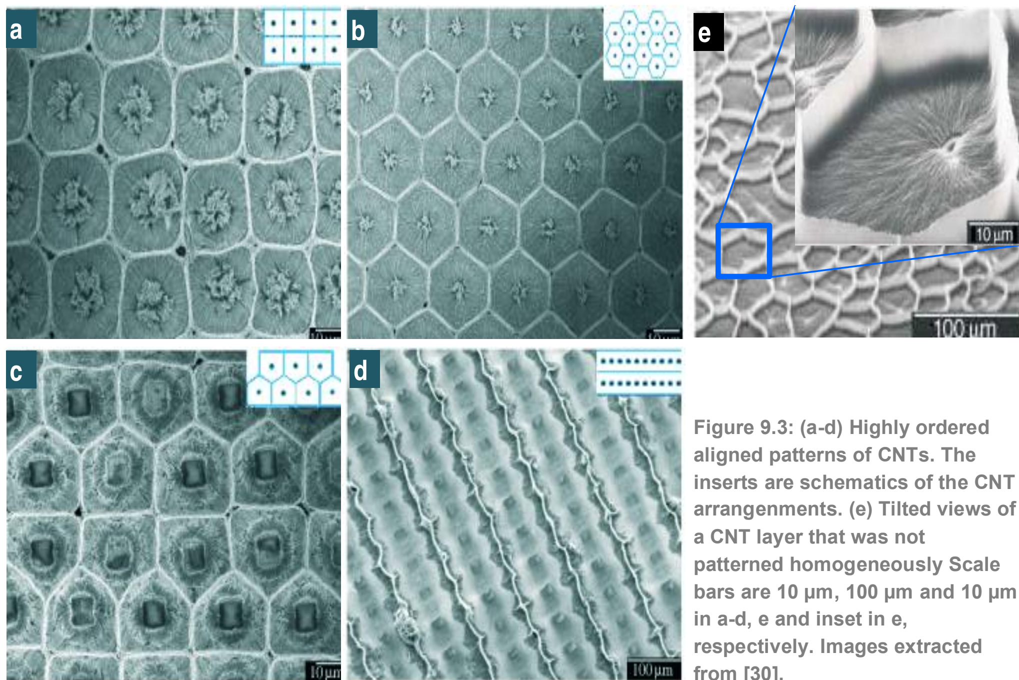


Figure 9.3: (a-d) Highly ordered aligned patterns of CNTs. The inserts are schematics of the CNT arrangements. (e) Tilted views of a CNT layer that was not patterned homogeneously Scale bars are 10 μm, 100 μm and 10 μm in a-d, e and inset in e, respectively. Images extracted from [30].

vertically aligned arrays of MWCNTS are synthesised and then detached from the original substrate and transferred to the electrode [28, 29].

Regarding the characteristics of the electrodes, those based on deposited CNTs should be, in principle, more robust that the electrodes modified by CVD synthesised CNTs since the CNTs are anchored at more than one point to the substrate. On the other hand, the electrodes based on synthesised CNTs should be more sensitive since the CNT packaging is expected to be lower and thus, the electrode will benefit of a higher roughness resulting in a higher active area. In these cases it should also be taken into account that the vertical alignment of the CNT layer may be lost if the measurements are done in liquid [27, 30]. As example, Figure 9.3 shows SEM images on the self-assembly of three-dimensional micropatterns of aligned CNT films [30].

9.2.3 Fabrication of CNT modified electrodes

As stated above, the CNT integration will be normally achieved based on either the direct deposition of CNTs on the electrode or on the selective synthesis of the CNTs on the electrode.

In the first case, the CNTs can be deposited on any size electrodes as long as there is no restriction due to the deposition process itself. For example, Gabriel reported that her method to deposit SWCNTs on metal electrodes resulted in a non uniform deposition on electrodes which diameter was bigger than 100 µm [31].

In the second case, on the contrary, more parameters need to be taken into consideration since the device fabrication must be made compatible with the synthesis of the CNTs and vice-versa. The main goals of the integration of the CNTs are to inhibit the diffusion of the catalyst material into the electrode, to guarantee a good contact between the electrode and the CNTs and to avoid any damage to the electrodes. To inhibit the diffusion of the catalyst two approaches may be considered: the use of a metal to form the electrode and a catalyst material that will not react among them (such as titanium nitride and nickel [19]) and the use of a diffusion barrier to inhibit the diffusion(typically metals or silicides [32] and even thin silicon oxide layers [33]). Regarding the damage to the electrodes the CVD synthesis conditions must be optimised so that the metal stripes and the passivation withstand the thermal budget.

Challenges

CNTs present very attractive properties for the development of sensors based on CNT-electrodes, which are already being demonstrated, coming from their size, their aspect ratio and their structure. However, there still exist technological challenges for the integration to be overcome. At this point, the main challenge is, possibly, attaining control over the synthesis of the CNTs, that is, attaining control over the diameter, number of layers and graphitization/defect, since the electrochemical properties of the CNTs highly depend on these parameters.

10 Carbon nanotube modified electrodes for bio-impedance applications

This chapter deals with the wafer scale integration of dense arrays of CNTs into the metallic electrodes of two different devices for bio-impedance applications, an Impedance Needle and a MEA, which had been developed by the Biomedical Applications Group of CNM. The wafer scale integration of the CNTs is expected to improve the fabrication yield and the mechanical and electrochemical characteristics of the electrodes.

As the electrodes are aimed at bio-applications, only bio-compatible materials should be used in their fabrication. Thus, in order to avoid the use of any non-biocompatible material, CNTs are grown by using platinum as the catalyst material instead of the usually utilized conventional material (iron, nickel and cobalt). The presented CNT integration process is based on the CNT synthesis optimization reported in Chapter 5.

This chapter is divided in 5 blocks. The first one is devoted to describe the fabrication and the characteristics of the devices from GAB. The second block deals with the fabrication of the CNT modified devices. Then, the third block addresses the mechanical, electrical and electrochemical characterization of the CNT modified electrodes. The fourth block compares the here developed electrodes with those previously developed by GAB. Finally, the fifth block presents other experiments by other research groups by the CNT modified electrodes.

10.1 The bio-sensing devices from GAB

Since 1997 GAB has developed devices to be used in bio-medical applications. Their main work has been oriented towards the developed of Impedance Needles and a Multi-Electrode Arrays (MEAs) [6, 24, 31, 34, 35] (Figure 10.1).

The Impedance Needles (Figure 10.1-a) are 4-point bio-impedance sensors that are intended to be minimal invasive when inserted in the tissue. The first Impedance Needle prototypes were patented (CSIC ES9901923) and they are now in clinical development [6]. Impedance Needles are formed by 4 300 x 300 μm^2 platinum electrodes and a temperature sensor. The whole device is passivated by a double silicon oxide/silicon nitride layer except for the electrodes and the connection pads. The size of an Impedance Needle is 15 mm x 0.7 mm.

MEAs (Figure 10.1-b) are aimed at serving for the monitorization and stimulation of tissues. MEAs are formed by 16 platinum electrodes, which can be round or square shaped. The diameter/side of the electrodes may be 10, 20, 30, 40 or 300 µm. MEAs include 2 reference electrodes and 2 temperature sensors. As for the Impedance Needles, the whole device is passivated by a double silicon oxide/silicon nitride layer except for the electrodes. The size of a MEA is 15 x 15 mm^2.

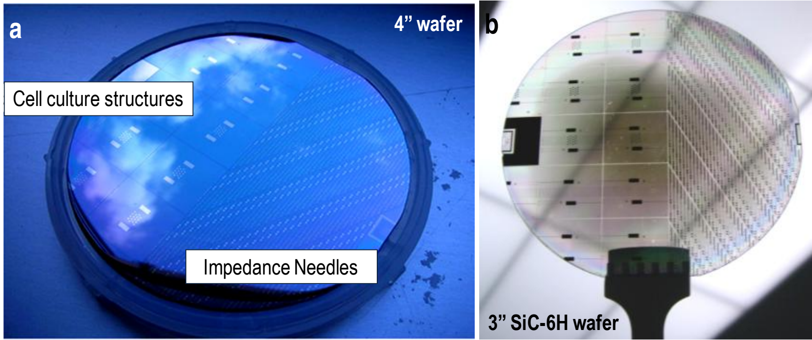


Figure 10.1: Photographs of (a) a 4 inch silicon wafer and (b) a 3 inch silicon carbide wafer where Impedace Needles and MEAs had been simultaneously fabricated.

The fabrication of the devices, which is normally performed on 4 inch silicon wafers [6, 31], has also been demonstrated on silicon carbide (3 inch wafer) [34], Pyrex (3 inch wafer) and SU-8 substrates [35]. Silicon carbide is better substrate than silicon for impedance measurements because of its higher resistivity [36]. In addition, its transparency to light is also of interest in cell culture applications. However, device fabrication on silicon carbide is more complicated and expensive. Pyrex is a much cheaper material than silicon carbide and presents also good characteristics in terms of resistivity and transparency. Its disadvantage is that it does not stand high temperatures and, thus, it is difficult to make it compatible with some of the fabrication process steps. SU-8 is a bio-compatible polymer. This material was used for the fabrication of Impedance Needles because, due to its flexibility, it may be less harmful when inserted into the tissue. Figure 10.1-a and Figure 10.1-b show a 4 inch silicon wafer and a 3” silicon carbide wafer where Impedance needles and MEAs had been fabricated, respectively.

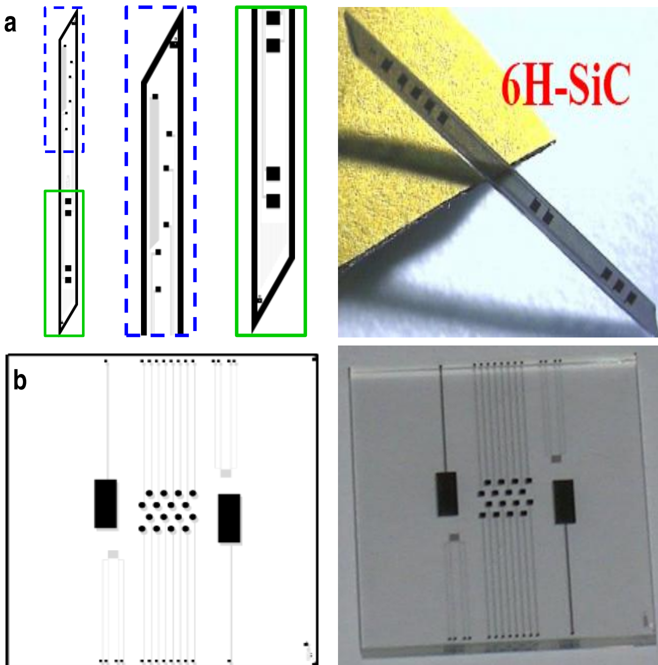


Figure 10.2: Schematics and photographs of (a) an Impedance Needle and (b) a MEA.

10.1.1 Electrode fabrication

The Impedance Needles and the MEAs can be simultaneously fabricated by a technological process analogous to the one described in [6] that only involves conventional process steps. The schematics of the main steps of the fabrication scheme are shown in Figure 10.3.

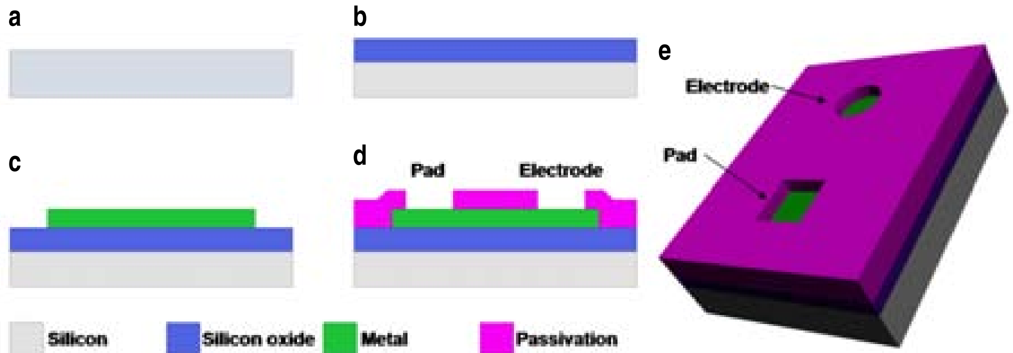


Figure 10.3: Main steps of the fabrication scheme: (a) silicon wafer; (b) thermal oxidation; (c) metal electrode patterning; (d) electrode passivation.

The starting point are 4 inch p-type silicon wafers (resistivity 4–40 Ω·cm) (Figure 10.3-a). First, the wafers are thermally oxidized to grow a 1.5 μm silicon oxide layer (Figure 10.3-b). The first photolithographic step (mask level CNM251-METAL, Figure 10.4-a), is used to pattern the metal electrodes. These electrodes are formed by sputtering of a titanium/platinum bi-layer (30/150 nm), which is then patterned by means of a lift-off process (Figure 10.3-c). Afterwards, the devices are passivated by a silicon oxide/silicon nitride layer (300/700 nm) that is deposited by PECVD. The second lithography (mask level CNM251-WINDOWS, Figure 10.4-b) is then used to pattern the contact windows for both electrodes and bonding paths, which are patterned by RIE. The final step is the resist removal by oxygen plasma (Figure 10.3-d,e). Once the devices have been fabricated, they are diced with a dicing saw system.

10.1.2 Improvement of the electrode impedance

As described in the previous chapter, the way to improve the parasitic impedance of an electrode-electrolyte interface without losing spatial resolution is to increase its active area. Among the different strategies, researchers from GAB have evaluated two electrode modification approaches.

A) Surface modification by electrode platinization

Figure 10.5-a shows the electrode of an Impedance Needle that had been fabricated on a silicon wafer after a layer of black platinum had been selectively deposited on it by electroplating [6, 34, 35]. The image evidences that the platinum deposition was homogeneous on most of the surface of the electrode. Figure 10.5-b shows detail of the increase of the roughness of the surface of the electrode due to the black platinum layer deposition. The disadvantage of this electrode modification procedure is that, since it is a manual process, it is time consuming and attained coverage is not fully reproducible between different electrodes or between different chips even if it is uniform at electrode level.

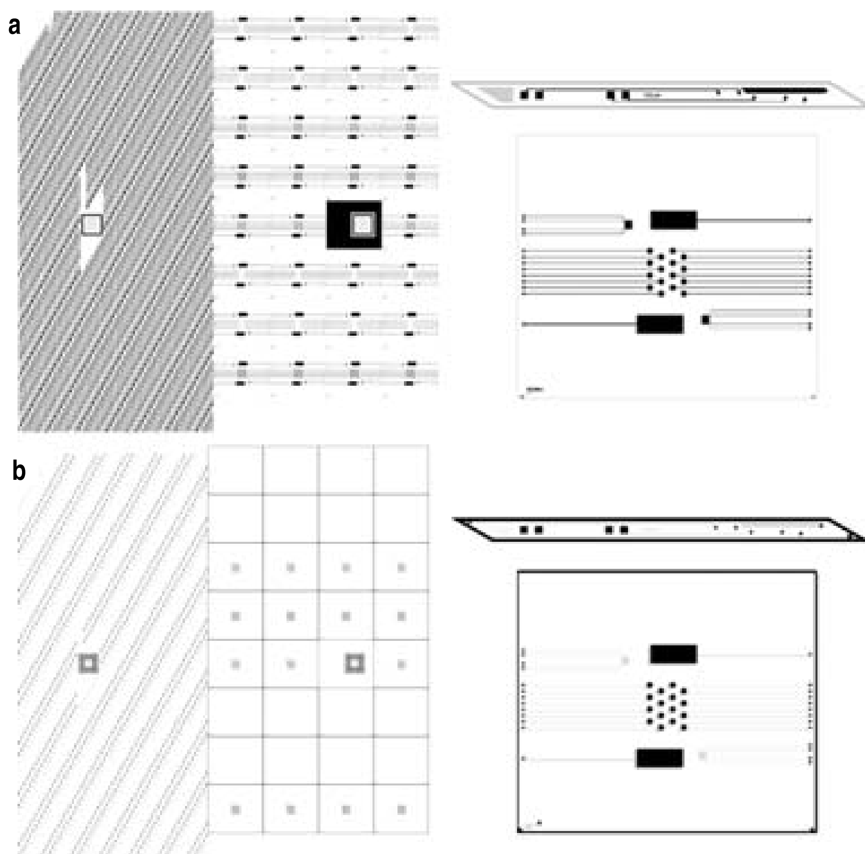


Figure 10.4: Schematic of the two mask levels that are used in the fabrication of the Impedance Needlesand and MEAs. (a) Mask level CNM251-METAL. (b) Mask level CNM251-WINDOWS. Detailed schematics of each maslk level (right) show detail of the mask for an Impedance Needle (top) and a MEA (bottom). Light gray schematics of the devices have been included in this detailed schematics for a better understanding of the masks.

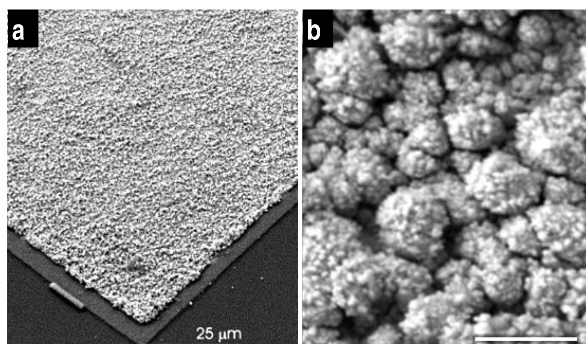


Figure 10.5: (a) SEM images of a platinum electrode after an electrodeposition of black platinum and (b) detail of part of its surface [34]. Scale bars are 25 µm and 5 µm, respectively.

The impedance characteristics of platinized electrodes fabricated on a Si wafer are discussed after Figure 10.7.

B) Surface modification by SWCNT deposition

Modification of the electrodes with CNTs was analysed aiming at an improvement of their mechanical and electrical properties together with their chemical stability [37].

The procedure to deposit SWCNTs on the electrodes is manual and consisted in the selective deposition of SWCNTs from a solution by a shadow mask [24, 31]. This procedure is versatile since it is easy to perform and it can be repeated as many times as required until the electrode to be perfectly covered (Figure 10.6-a). In addition, the procedure may also be used to deposit any structure CNT. However, it was determined to be valid only for electrodes smaller than 100 µm since the coverage was not uniform, most probably, because of SWCNT removal from the electrodes during the wiping step (Figure 10.6-b). In addition, the images of the electrodes after the SWCNT deposition showed that the SWCNTs were not only confined at the electrodes, most probably because of some SWCNTs moving to the surrounding areas of the electrodes during the surface washing.

The impedance characteristics of the SWCNT modified electrodes are discussed in the next section after Figure 10.7.

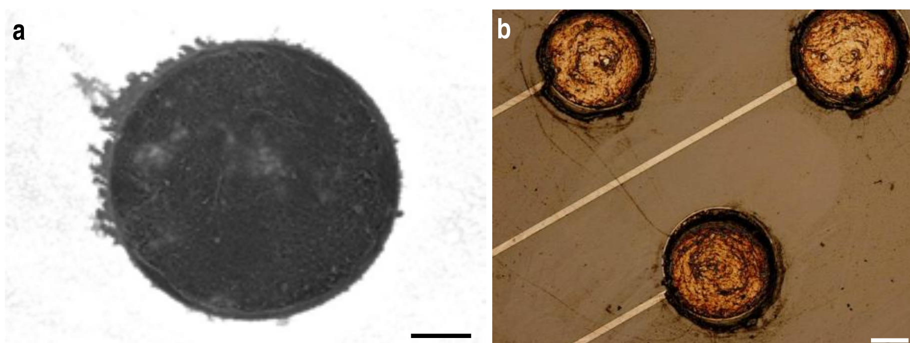


Figure 10.6: Images of electrodes that had been modified by deposited SWCNTs. (a) SEM image of a 20 µm in diameter electrode. (b) Optical image of three 300 µm in diameter electrodes [24]. Scale bars are 100 µm and 5 µm, respectively.

10.1.3 Electrode performance

The impedance characteristics of the bare platinum electrodes compared to the black platinum and SWCNT modified electrodes are shown in Figure 10.7. Figure 10.7-a depicts the impedance of 40 µm in diameter electrodes, whereas Figure 10.7-b depicts that of 300 µm in diameter electrodes.

The impedance characteristics evidence a clear improvement of the impedance for the modified with black platinum or SWCNTs electrodes and thus, that the active area of the electrodes was significantly improved [31]. The comparison of the impedance improvements demonstrated that SWCNT deposition was, for both electrode diameters, the most efficient modification procedure. In the case of the 40 µm electrodes, SWCNT modification was demonstrated to be much better performing than the black platinum modification. In the case of the 300 µm electrodes, however, the impedance characteristics of the SWCNT modified electrodes with respect to the black platinum ones were found to be similar, most probably, due to a non efficient deposition of the SWCNTs for the big diameter electrodes (Figure 10.6-b).

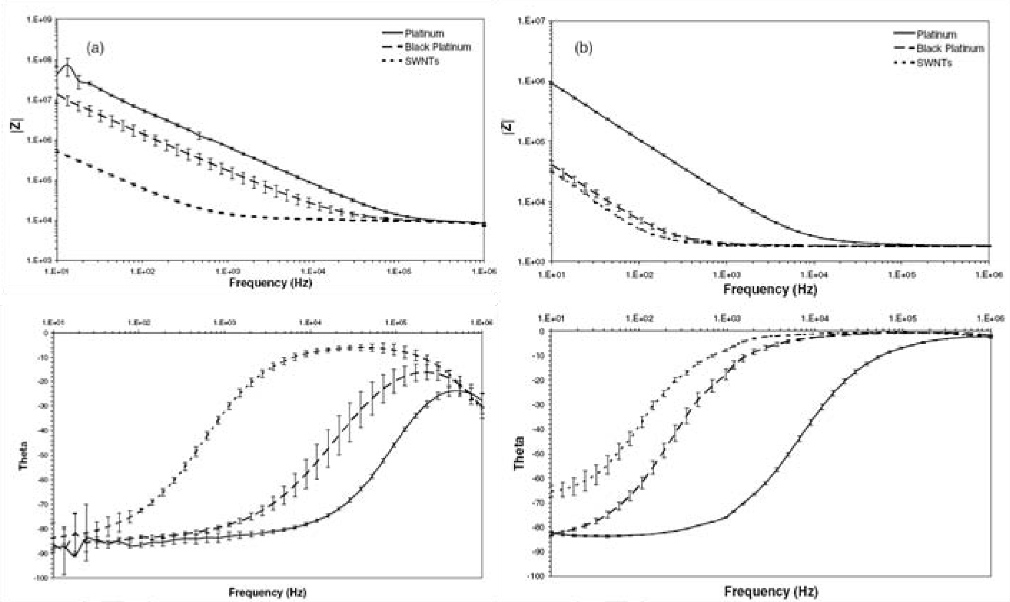


Figure 10.7: Impedance characterization of bare platinum electrodes and electrodes that had been modified with black platinum or SWCNTs for 40 µm and 300 µm in diameter electrodes fabricated on silicon substrates [31].

These electrodes were also evaluated for recording and stimulation of tissue. Experiments were positive but revealed that the electrodes degraded progressively because of the frailty of the black platinum and to detaching of the deposited SWCNTs. Furthermore, problems we encountered to achieve a good contact between the tissue and the electrodes.

10.2 Integration of carbon nanotubes into metallic electrodes

This section addresses the fabrication of CNT modified Impedance Needles and MEAs on 4 inch silicon and 3 inch silicon carbide wafers. Presented CNT integration process was conceived as a further fabrication step to be included after the base electrodes had been fabricated (section 10.1.1). As in that case, the process was designed so that only standard microelectronic techniques were employed.

Regarding the CNT synthesis, as the application requested the use of bio-compatible materials, platinum was used as the catalyst material. As this material has seldom been used as CNT catalyst, a big effort was required for the optimization of the CNT synthesis (Chapter 5).

10.2.1 Technological process for the integration of the CNTs

The CNT integration process, which is composed of 4 main steps (Figure 10.8), is similar to that used in the optimization of dense arrays of MWCNTs from platinum thin layers (section 5.2)

The starting point are the passivated platinum electrodes, which are fabricated at 4 inch wafer scale as described in section 10.1.1. The CNT integration steps start with the deposition of a 15 nm thick silicon oxide layer by means of PECVD similarly to [33] (Figure 10.8-a). As it was discussed in section 5.2.2, this silicon oxide layer improves CNT synthesis by inhibiting diffusion of the catalyst to the

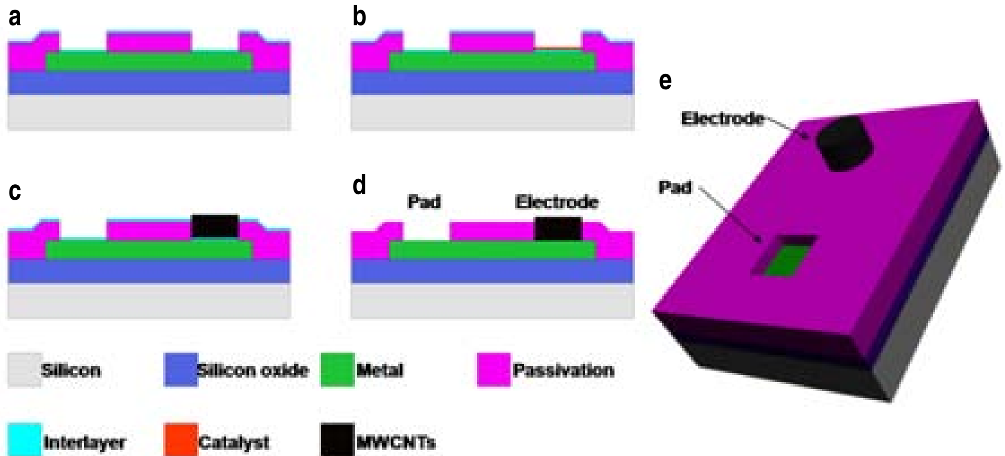


Figure 10.8: Process scheme to integrate the CVD synthesized CNTs on the electrodes: (a) base electrode; (b) silicon oxide deposition by PECVD; (c) local deposition of the catalyst material; (d) CVD synthesis of CNTs; (e) silicon oxide removal by wet etching.

metal electrode and by increasing the roughness of the electrode so that smaller and closer catalyst particles form [38].

The second step of is the selective deposition of the catalyst material. This step comprises a photolithographic step (mask level CNM251-CNT (Figure 10.9)), the catalyst layer deposition and its patterning by means of a lift-off process (Figure 10.8-b). 4 nm thick sputtered platinum layers were usually deposited as catalyst layers but other platinum thicknesses between 1 and 3 nm were also tested. These layers were deposited by evaporation*.

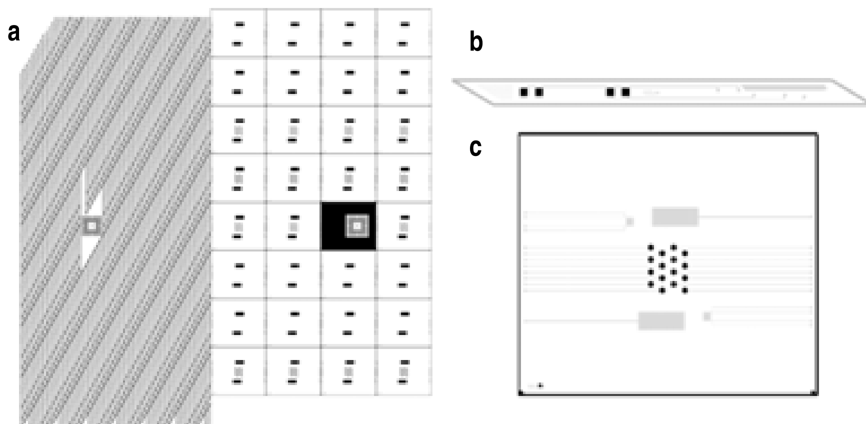


Figure 10.9: Pictures of the mask level used for the selective deposition of the CNT catalyst material, CNM251-CNT. (a) The whole mask level. (b-c) Schematics of the mask level for an Impedance Needle and a MEA, respectively. Light gray motifs (not related to this level) have been included in b and c for a better understanding of the mask level.

* Evaporation of the platinum layers was performed at the *Laboratori de Capes Primes* of UAB

The third step of CNT integration is the synthesis of the MWCNT array (Figure 10.8-c). The RTCVD process parameters are adjustable according to the results on CNT synthesis optimization reported in section 5.2. The most standard CVD process is divided in a catalyst activation step (800ºC; hydrogen) and a CNT growth step, which is, in turn, composed of two stages (stage1: 800ºC; methane/hydrogen // stage2: 800ºC; methane).

The final fabrication step is the removal of the PECVD deposited silicon oxide layer by wet etching to optimise the contact between the electrode and the MWCNTs and to assure a correct wire-bonding at the connection pads (Figure 10.8-d,e). This etching should not affect to the adhesion of the CNTs to the metallic electrodes since most of them are expected to be in contact with it [33].

10.2.2 Results of the fabrication

Images on the fabrication of the MWCNT modified electrodes are shown in Figure 10.10 to Figure 10.12. Figure 10.10 depicts a 4 inch silicon wafer and a 3 inch silicon carbide wafer where MEAs (top) and Impedance Needles (bottom) had been fabricated. Optical images in Figure 10.11 show the electrode areas of some Impedance Needles and a MEA fabricated on a silicon wafer. The darker areas in these images are the electrodes where the CNTs had been selectively synthesized. Their darkness and their homogeneous colour are evidence of the CNT layers being very dense. Besides, sample inspection showed that the silicon oxide/silicon nitride passivation on the platinum stripes sometimes cracked locally because of the thermal budget during the CNT synthesis process. These defects in the passivation were neglected in the electrochemical experiments.

SEM images in Figure 10.12 show the aspect of the synthesized on the electrode MWCNT layers when the catalyst layer was 4 nm (Figure 10.12-a,b) and 1 nm (Figure 10.12-c,d). Figure 10.12-a and Figure 10.12-c comparison evidences that the obtained CNT density when using the thinner thickness of the catalyst layer (1 nm) is much higher than in the other case. This, which was discussed in section 5.2.4, is due to the catalyst layer dewetting into smaller, more uniform and more densely distributed catalyst islands for the CNTs to grow from.

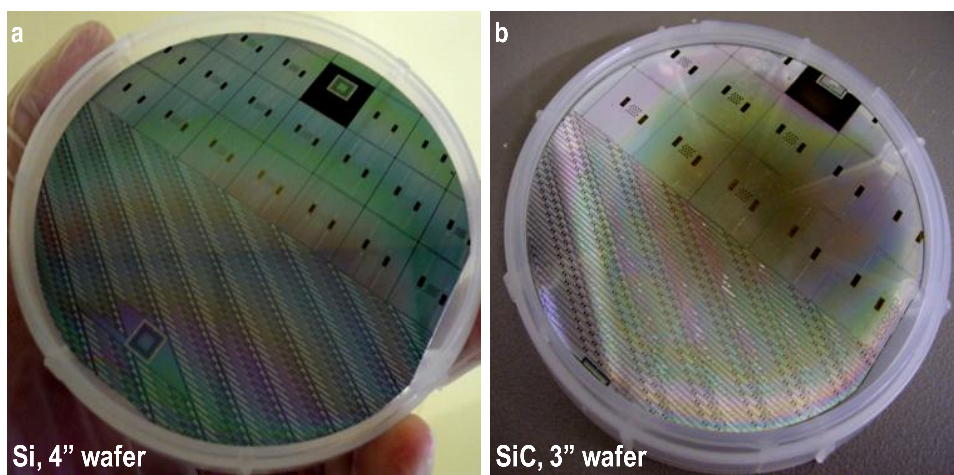


Figure 10.10: Photographs of (a) a 4 inch silicon wafer and (b) a 3 inch silicon carbide wafer where dense arrays of CNTs had been selectively integrated into the electrodes (the darkest areas on the photographs).

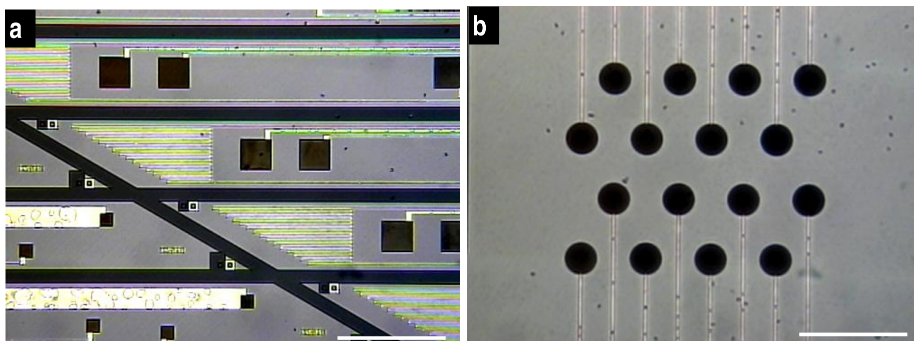


Figure 10.11: Optical images on the selective synthesis of CNTs on the metal electrodes of (a) Impedance Needles and (b) MEAs. Scale bars are 1 µm.

In both cases the CNT arrays aligned vertically because of the CNT density. When the catalyst layer is 4 nm thick, CNTs align vertically due to the formation of a top CNT crust [39] whereas, when it is 1 nm thick, CNTs align vertically because the very high density of CNTs inhibits their growth in any other direction. Synthesized CNTs were evaluated as MW, their diameters ranging between 10 and 20 nm, their length was measured to be ~1 µm and their graphitization level was checked to be high. Refer to sections 5.2.3 and 5.2.4 for a full discussion about the characteristics of these CNT arrays.

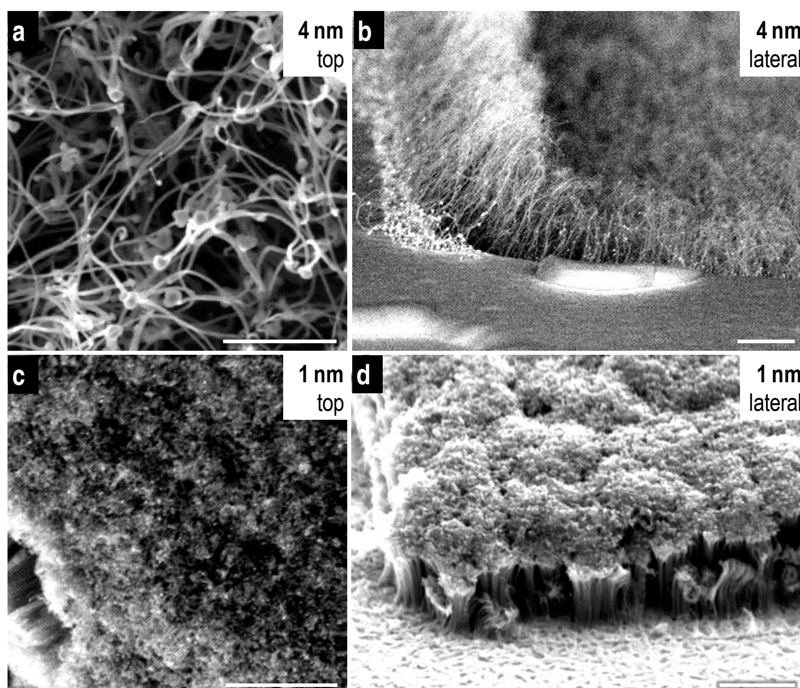


Figure 10.12: SEM images of the MWCNTs that were synthesized on the platinum electrodes. (a-b) top and tilted view images of the MWCNTs that were synthesized out of a 4 nm thick platinum layer. (c-d) top and tilted view images of the MWCNTs that were synthesized out of a 1 nm thick platinum layer. Scale bars are 500 nm and 1 µm in (a-c) and (b-d), respectively.

Henceforth, electrodes where the MWCNTs layer was synthesized out of a 4 nm thick platinum layer will be named electrodes *type-A* and electrodes where CNTs were synthesized out of a 1 nm thick platinum layer will be named electrodes *type-B*. Depending on the experimental setup one or both types of electrodes will be used.

10.2.3 Conclusions on the fabrication

These sections have presented and demonstrated a process for the integration of CNTs into metallic electrodes by an electrode-CNT catalyst barrier and the selective synthesis of the CNTs. Every process step involved in the process is conventional and, as it has been demonstrated, the fabrication of the electrodes can be performed at wafer scale. The characterization of the synthesised MWCNTs has shown that the CNT arrays are dense and, thus, they tend to align vertically, and that their morphology depends on the thickness of the platinum layer that is used as CNT catalyst.

10.3 Characterization of the carbon nanotube-modified electrodes

This section, which is divided in three blocks, presents the results on the characterization of the fabricated in the previous section Impedance Needles and MEAs.

Since the CNT-modified electrodes are aimed at being used in liquid environments and at being inserted into the tissue, the first block of the section addresses their mechanical stability. The second block describes an experiment on the electric continuity of the CNT-electrode interface. Finally, the third block presents the electrochemical measurements on the impedance and the cyclic voltamperometry of the electrodes that will serve, afterwards, to evaluate the active area of the electrodes.

10.3.1 Mechanical stability of the CNT layer

Since the fabricated electrodes are aimed at performing measurements in liquid and/or at being inserted into tissue, it was important to test their mechanical stability. This way, different tests were performed to check the stability of the CNT array in liquid, its stability when inserting the electrodes into tissue and its stability when scratching the surface.

A) CNT layer stability in liquid

It is well known that the alignment of a CNT layer may be altered when introduced in a liquid environment [27, 30]. Since CNT alignment affects the active area of the electrodes and therefore, the electrochemical characteristic of the devices, it was relevant to perform some experiments to evaluate the electrodes in liquid environment.

The experiments consisted in comparing the morphology of the MWCNT arrays before and after the silicon oxide interlayer etching. It has to be noted that the etching was performed as if it was a standard wet etching process, without taking care to avoid any damage of the CNT array. The samples were immersed in the hydrofluoric acid based solution, rinsed in deionised water and dried with a nitrogen gun.

SEM images in Figure 10.13 show the MWCNT layer before and after the etching for the electrodes *type-A* (Figure 10.13-a,b) and the electrodes *type-B* (Figure 10.13-c,d). The images give evidence of the importance of the MWCNT density to preserve the vertical alignment of the CNT layer.

In the case of the electrodes *type-A*, where the MWCNTs had aligned vertically because of the formation of a top CNT crust, the CNT array collapsed because of the gap between the MWCNTs and because they were not thick enough to stand the capillarity forces.

In the case of the electrodes *type-B*, where the MWCNTs had aligned vertically because of the CNT packaging, the MWCNTs stood with a vertical alignment since they could not fold. However, SEM observation of the CNT arrays shows that, because of the capillarity forces, CNTs will collapse ones against each other and so, trenches on the CNT array will appear (Figure 10.13-d). Optimization of the packing of the CNT array would lead to the control over its morphology when performing the wet etching to remove the silicon oxide interlayer and during an experiment in liquid environment.

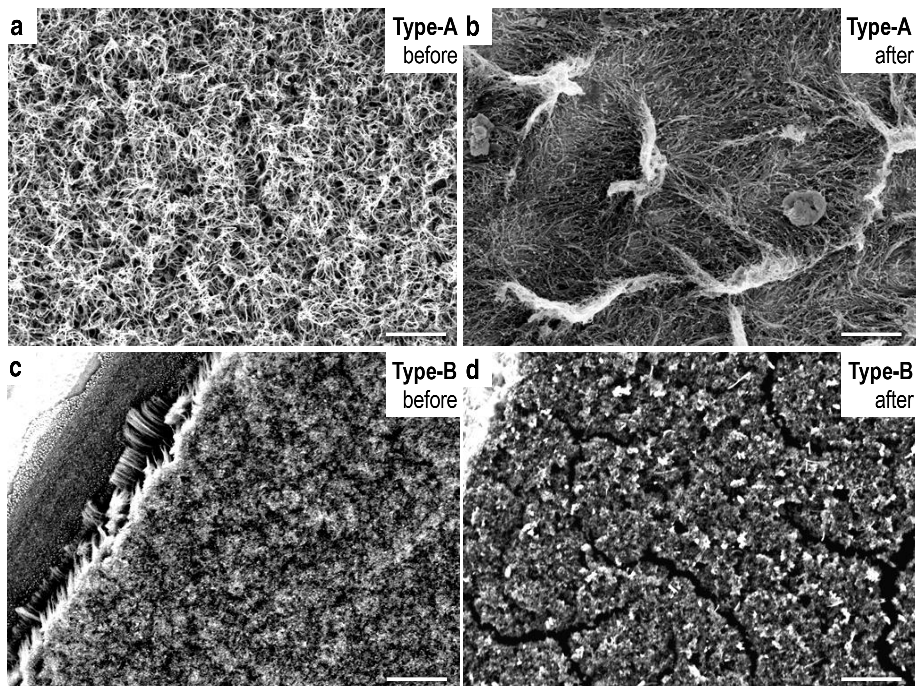


Figure 10.13: SEM images on the influence of the wetting of the CNT layer depending on its morphology (a-b) for an electrode type-A (4 nm thick catalyst layer) and (c-d) an electrode type-B (1 nm thick catalyst layer). Scale bars are 1 µm.

B) CNT layer stability when scratching

The stability of the CNT layer when scratched was analysed to evaluate the durability of the CNT-modified electrodes. The experiments consisted in scratching the surface of the electrodes and checking how the MWCNT array had been modified. As in the previous case, the experiments were performed on electrodes *type-A* and on electrodes *type-B*. Moreover, the *s*cratches were performed on samples where the silicon oxide interlayer had and had not been removed to evaluate the role of silicon oxide interlayer before and after the wet etching.

The first experiments consisted in scratching CNT arrays with a sponge. When using this material the CNT arrays were removed from every sample. For this reason, scratching on posterior experiments was done locally with a probe.

Figure 10.14 shows scratches on the CNT array of an electrode *type-A* before the wet etching (Figure 10.14-a) and for an electrode *type-B* before (Figure 10.14-b) and after (Figure 10.14-c) the wet etching. The SEM images in Figure 10.14-a,b demonstrate how only MWCNTs in the way of the scratch were removed from the electrode surface when the scratch was performed on the samples where the silicon oxide had not been removed. Similar was observed when the scratch was performed on electrodes *type-A* where the silicon etching had been performed. However, when the scratch was performed on electrodes type-B after the wet etching blocks of MWCNTs were removed as depicted in Figure 10.14-c.

In the case of the electrodes *type-A*, the results before and after the etching are analogous because, due to the space between the MWCNTs, when the electrodes are immersed in the acidic solution, the MWCNTs lay down on the substrate and so, they do not lose the contact with it. In the case of the electrodes *type-B*, on the other hand, as the MWCNTs are perpendicular to the surface and it is only their tips that are in contact with the substrate, when etching the silicon oxide interlayer some of the tips may detach. Additionally, the interaction forces between the MWCNTs are much stronger than in the previous case (due to the denser packaging) and, thus, when scratching the CNT array, detached MWCNTs drag other MWCNTs.

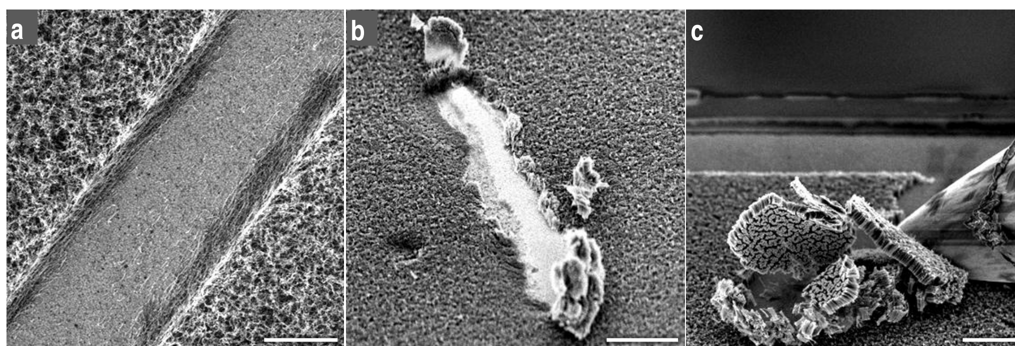


Figure 10.14: SEM images of scratches on different in density MWCNT layers. (a-b) Scratches on electrode type-A and type-B, respectively, before the silicon oxide interlayer removal. (c) Scratch on an electrode type-B after the silicon oxide interlayer removal. Scale bars are 5 µm.

C) CNT layer stability when inserting the electrodes into tissue

The adherence of the CNTs to the electrode was checked because the Impedance Needles are aimed for insertion into tissue. Impedance Needles where electrodes *type-A* had been fabricated were used in this experiment.

The experiment consisted in inserting different Impedance Needles into a chicken liver (Figure 10.15). Optical and SEM images of the Impedance Needles were acquired prior the insertions and after them, before and after washing the electrodes with a bleach based solution and de-ionized water.

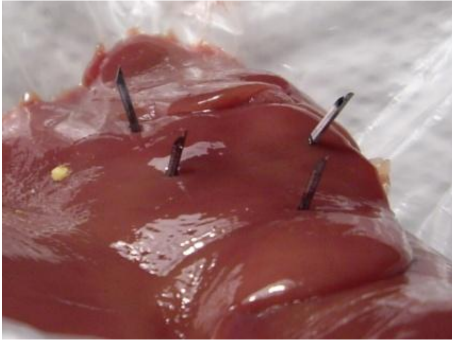


Figure 10.15: Photograph on the experiment to check the adherence of the MWCNT layer when the Impedance Needles were inserted into tissue.

The optical images in Figure 10.16 refer to three of the Impedance Needles that were used in the experiment. The Impedance Needle in Figure 10.16-a was used as the reference device. Impedance Needles in Figure 10.16-b,c were inserted into the liver one time and five times, respectively. Figure 10.16 evidences that the more insertions of the Impedance Needles, the more cellular residues on the device. Impedance Needles did not break because of their insertion into the tissue. Marked areas on the Impedance Needles refer to the electrodes that are shown in detail in Figure 10.17.

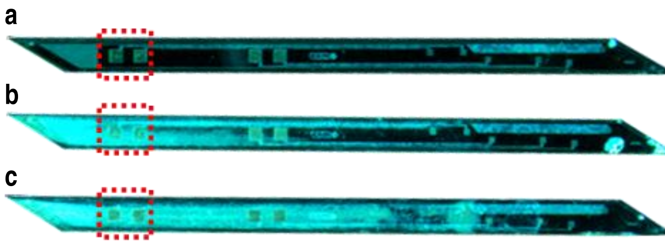


Figure 10.16: Optical images of three of the Impedance Needles that were used in the experiments on the insertion into tissue. (a-c) Reference, one time inserted and five times inserted Impedance Needles, respectively.

Figure 10.17 depicts detail of part of the electrodes of the reference device (Figure 10.17-a) and of the inserted devices before (Figure 10.17-b1,c1) and after (Figure 10.17-b2,c2) the cleaning process. Images in Figure 10.17-b2,c2 show that the bleach based cleaning process was effective since no cellular trace is observed on the needles after the washing. The optical images reveal that the electrodes remained dark coloured after the insertion and after the cleaning process and, thus, that the MWCNT array was still very dense after the insertion and washing. No scratches on the MWCNT layer related to the insertion of the devices could be observed.

The SEM images in Figure 10.18 show part of the MWCNT array on an electrode after it had been inserted into the tissue and after it had been washed. The SEM in Figure 10.18-b, which is a higher in magnification SEM image of part of the CNT layer in Figure 10.18-a, evidences that the MWCNTs remained on the electrodes. The images give also evidence of the loss of the vertical alignment of the CNT array. This loss of verticality was predictable based on the experiment on the stability of the CNT array when it is immersed in liquid. The loss of the vertical alignment should not imply a loss of the electrical response when performing measurements on the stimulation and/or recording from a tissue since the CNT layer squashes because of the contact of the CNTs and the tissue and because of the Velcro characteristic of the CNTs [20, 22].

It has to be noted that the fact that the CNT layer stood the insertion into dead tissue is indicative of it standing the insertion into a living tissue as the cellular membrane becomes stiffer when it is dead due to the loss of water.

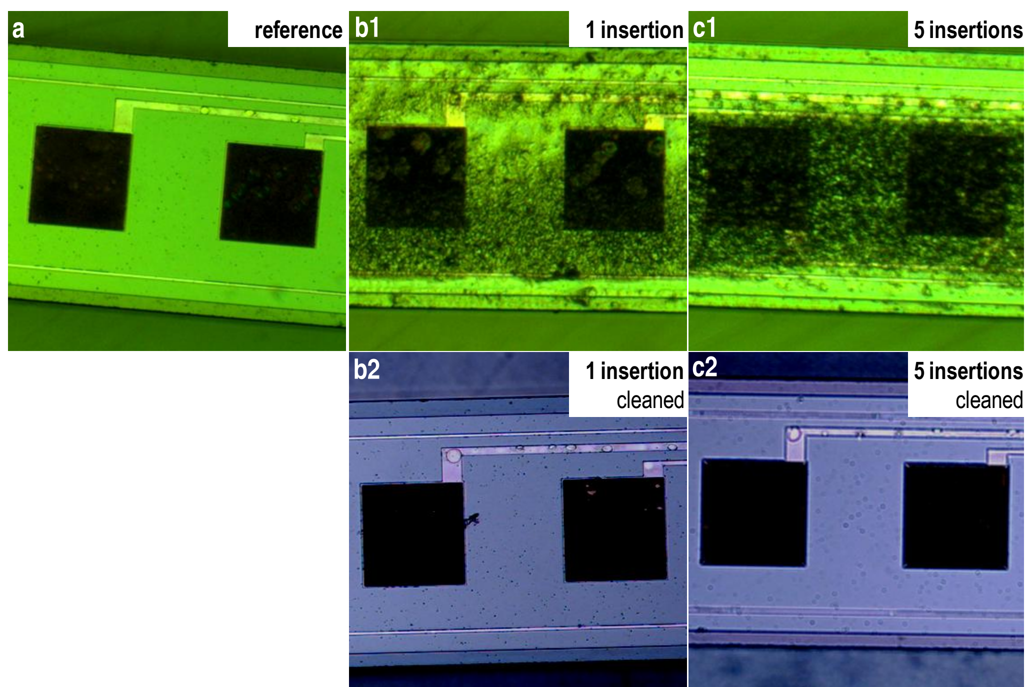


Figure 10.17: Optical images of the electrodes of the Impedance Needles that were used in the experiments on the insertion into tissue. (a) Electrodes from the reference Impedance Needle. (b1, b2) Electrodes from the Impedance Needle that was inserted one time after insertion and after needle washing, respectively. (c1, c2) Electrodes from the Impedance Needle that was inserted five times after insertion and after device washing, respectively.

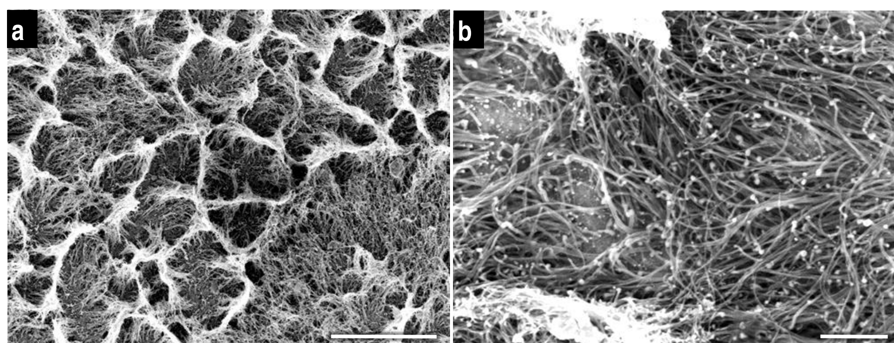


Figure 10.18: SEM images on the aspect of the CNT modified electrodes on an Impedance Needle after the device had been inserted into the tissue and washed with a bleach based solution. Scale bars are 5 µm and 500 nm.

10.3.2 Electrical continuity

Two probe electrical measurements were performed to check the continuity between the electrode and the CNT layer and to analyse its resistance on electrodes *type-B*. Electrodes *type-A* were not used in this experiment because of the difficulties to achieve a good contact on the CNT layer.

Based on the fact that the MWCNT layer could be very easily scratched, this experiment was performed inside the monitored chamber of a SEM with probing capabilities to avoid any damage on the MWCNT layer[†]. Although the electrodes had a contact pad, since the SEM field was not large enough to visualise the electrode and the pad simultaneously, a contact window had to be opened on the platinum stripe, close to the electrode, by an argon milling of the passivation layer. In order to prevent the MWCNT layer from being scratched and to achieve a good contact on the different materials, the probe positioning was monitored by SEM and, additionally, a voltage was applied between the probes to monitor the current.

SEM images in Figure 10.19 show probe positioning (Figure 10.19-a) and the hollow that had been left on the CNT array after performing the contact (Figure 10.19-b,c). Depending on the probe positioning, a bigger hollow was observed. The cases where the hollow seemed to go through the CNT layer were neglected.

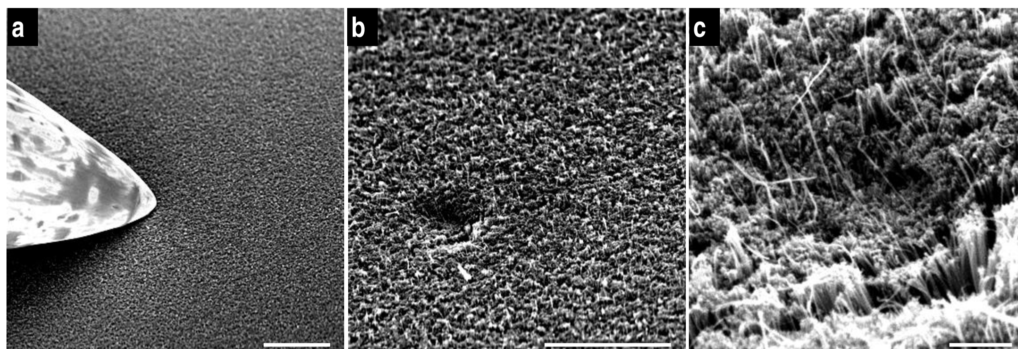


Figure 10.19: SEM images on the SEM monitorization of the probe contact on an electrode type-B. (a) SEM image of the probe contacting the MWCNT array. (b-c) SEM images of the hollow that was formed when the probe contacted the MWCNT array. Scale bars are 10 μm, 5 μm and 500 nm, respectively.

The current monitoring consisted in applying 50 mV between the probes and measuring the current (Figure 10.20). When the contact had not been achieved, the current was measured to be at noise level, whereas, when the probe was put in contact with the CNT array, it increased up to the mA range.

It has to be noted that even if contacts were monitored by SEM and by measuring the current, reaching the contacts on the CNT layer was difficult. Moreover, achievement of good contacts could not be certified as the interaction of the CNTs and the probe were unknown. As an example, the current characteristic in Figure 10.20 shows how the current level increased 20% when the probe was slightly lowered after the contact had been attained.

[†] The FIB system was operated by the FIB engineer at CNM's clean room.

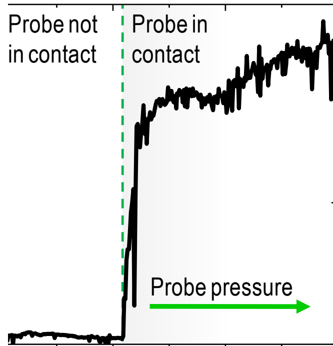


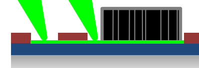
Figure 10.20: Example of the current monitorization during the probe contact on MWCNT array. The other probe had been placed on the wire. 50 mV had been applied between the probes.

Current-voltage curves in Figure 10.21 show the electrical characteristic of an electrode. In this case, the silicon oxide interlayer had been removed prior to the electrical measurements. The curves in the graph correspond to the **electrode-wire path**, to the CNT **layer-electrode path** and to the CNT layer-**electrode-wire path**.

The graph shows that the resistance of the electrode-pad path was around ten times lower than that for the others and that the current levels for the paths where the CNT array was involved were similar. This evidences that the decrease of the current was related to the non-optimised contact between the CNTs and the metallic electrode, which has already been demonstrated by the experiments on the scratching of the CNT array (section 10.3.1).

a

b Elec.-pad



c CNT-elec.

d CNT-pad

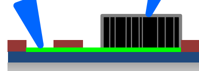


Figure 10.21. I-V characteristics of the MWCNT-modified electrodes. Green, red and blue characteristics in (a) are related to measurement setups in b, c and d, respectively.

10.3.3 Electrochemical characteristic of the electrodes

The electrochemical characteristic of the electrodes *type-A* was evaluated by impedance spectroscopy and cyclic voltamperometry. For the MEAs to be easy to manipulate, fabricated devices were diced and then encapsulated on PCBs (Figure 10.22). Encapsulation consisted of the gluing the MEAs to previously fabricated PCBs, of the wire-bonding of the chips and, finally, of the protection of

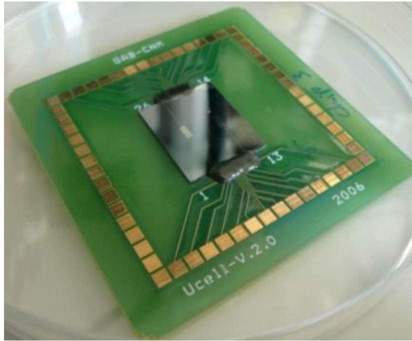


Figure 10.22 MEA that had been encapsulated for electrochemical measurements.

the wires with an epoxy based resist[‡]. Before the measurements took place, a ring lid was glued to the PCB so that the solution was confined to it during the experiments.

A) Electrochemical impedance measurements

The impedance measurements were conducted by using a commercial impedance analysis system, a commercial platinum electrode and physiological saline solution. The measurements were conducted

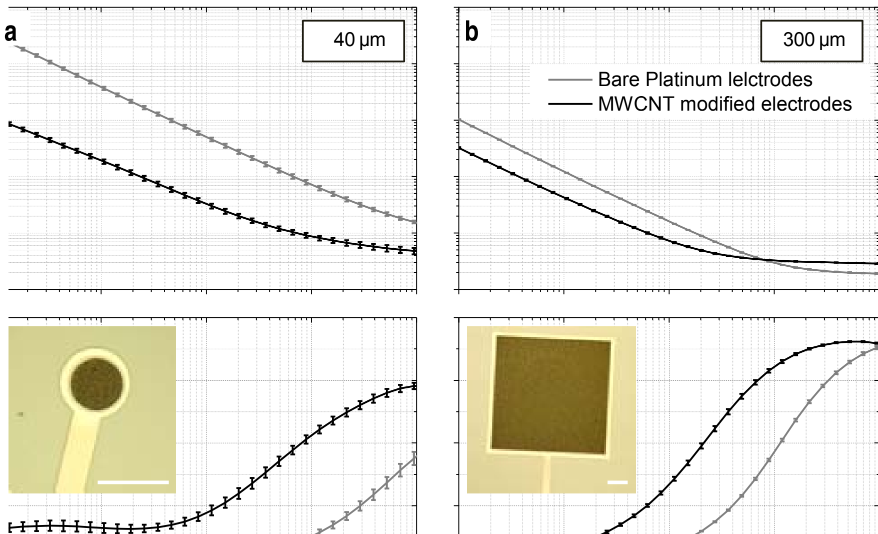


Figure 10.23: Impedance characteristics of the MWCNT modified MEAs compared to the original platinum electrodes for (a) round shaped 40 µm and (b) square shaped 300 µm. Optical images on the phase diagrams are representative images of the electrodes. Scale bars are 50 µm. Impedance characteristics of the bare platinum electrodes courtesy of Dr. Gemma Gabriel.

‡ These steps were performed by Mr. Alberto Moreno and Ms. María Sanchez at the Device Packaging Laboratory at CNM.

between 10 Hz and 100 kHz. Refer to section 2.2.2 for a more in detail explanation of the experiment.

Figure 10.23 shows the impedance characteristics of two different MWCNT modified electrodes against their equivalent platinum electrodes: round shaped 40 µm electrodes (Figure 10.23-a) and square shaped 300 µm electrodes (Figure 10.23-b).

In order to analyse the impedance characteristics, the electrode–electrolyte interface behaviour was approximated by the parallel combination of the charge transfer resistance (R_{CT}) and a constant phase element (C_{PE}—nonfaradaic pseudocapacitance), which represents the doublelayer interface capacitance impedance, in series with the spreading resistance (R_s—solution resistance) (Figure 10.24). C_{PE} is expressed by

$$Z_{CPE}(\Omega) = Q(j\Omega)^{-n} \quad (10.1)$$

where Q is a constant affecting the magnitude of the impedance, and n is a constant [$1 \geq n \geq 0$] that affects both the magnitude and the impedance and represents the inhomogeneities on the surface electrode. When n is equal to 1, C_{PE} describes an ideal capacitor whereas, when n equal to 0, C_{PE} describes an ideal resistor. [40]

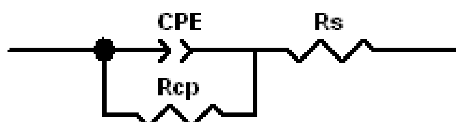


Figure 10.24: Schematic of the equivalent electrode-electrolite interphase behaviour.

Regarding the 40 µm electrodes, according to the calculations after Figure 10.23-a, n switches from values around 0.8 for the bare platinum electrodes to values close to 0.7 for the MWCNT modified electrodes, indicating an increase of the roughness of the electrode. Q was calculated to be around $5 \cdot 10^{-8}$ and around $7.2 \cdot 10^{-10}$ for the MWCNT modified electrodes and for the bare platinum electrodes, respectively. Regarding R_{CT}, even if the values could not be calculated because of insufficient data at low frequencies, it is evident how the modulus of the impedance of the modified with MWCNT electrodes diminishes with respect to that of the bare platinum electrodes in almost 2 orders of magnitude for the lowest frequencies.

Regarding the 300 µm electrodes, Figure 10.23-b shows how the impedance of the electrodes is improved, again, with respect to that of the bare platinum electrodes. This time, however, the improvement of the impedance is not as significant as it would be expected from the results on the 40 µm electrodes. Furthermore, the phase characteristics of the electrode do not evidence any improvement on the electrode roughness. In this case it is also surprising how the R_s is higher for the MWCNT modifies electrodes than for the bare platinum electrodes. The obtained characteristic could indicate the presence of amorphous carbon around the CNTs inhibiting the electron exchange.

B) Cyclic voltammetry measurements

The MWCNT electrodes were evaluated by cyclic voltammetry to quantify their capacitance similarly to [19]. The experiments were conducted in saline solution similarly to the impedance experiments. A silver electrode and a platinum electrode were used as reference and counter, respectively. Refer to section 2.2.2 for a detailed description of the experimental setup.

Figure 10.25 depicts the voltammograms for the electrodes that were analysed in the previous experiment. Figure 10.25-a1 and Figure 10.25-b1 show the obtained voltammograms for the scan speeds ranging from 25 mV/s to 2000 mV/s for the round shaped 40 µm electrodes and the square shaped 300 µm electrodes, respectively. Figure 10.25-a2 and Figure 10.25-b2 represent the current

a1

b1

a2

b2

Figure 10.25 Cyclic voltammetry analysis of the CNT-modified electrodes. (a) Voltammograms at different scan rates between 25 mV/s and 2000 mV/s. (b) Evolution of the current measured for V=0.3 V.

evolution (current measured for V= 0.3V) from the voltammograms in Figure 10.25-a1 and Figure 10.25-b1, respectively.

As no redox couple had been included to the solution for the experiments, observed current evolution, can be considered as the current due to the capacitance of the electrode. The insets in Figure 10.25-a2 and Figure 10.25-b2 show detail of the current evolution for scan speeds up to 200 mV/s. Faster than 200 mV/s scan rates were not considered for the capacitance calculations of the electrodes because at those scan speeds the electrode saturated.

Table 10.1 is a summary of the results calculated from the voltammograms. The capacitances were calculated to be 45.1 nF and 79.4 nF for the 40 μm and the 300 μm electrodes, respectively. Even if

	C (nF)	A (μm2)	$C/_A \; \left(\mu F/_{cm^2}\right)$
40 μm electrodes	45.1	(Φ = 36 μm) 1,018	4,331
300 μm electrodes	79.4	(Φ = 296 μm) 87,616	91

Table 10.1: Summary of the calculation on the capacitance of the MWCNT modified electrodes after the clyclic voltametries.

the capacitance for the bigger electrode is higher, it is remarkable how the capacitance per area is, however, almost 25 times higher for the smaller electrode (4.331 μF/cm^2 against 91 μF/cm^2) similarly to discussed in the previous section for the impedance measurements.

Obtained values of the capacitance per unit area for the 40 μm electrode are higher than the DC specific capacitance of commercial titanium nitride micro-electrodes (2.5 mF·cm^{-2}) but lower than that attained in [19], most probably because of a loose of effective active area on the MWCNT layer due to the measurements being performed in liquid.

10.3.4 Conclusions on the electrode characterization

The previous sections have evaluated the mechanical, the electrical and the electrochemical characteristics of the MWCNT modified electrodes.

Good mechanical adherence has been observed for the CNTs on electrodes type-A. The not so good adherence on electrodes type-B appears to be caused by the very high packaging and to the removal of the interlayer the CNT layer looses part of the adherence. The electrodes *type-A* lose their vertical alignment but because of that, they remain in contact (attached) to the metallic electrode and they stand insertion into tissue. The fact that they can stand this insertion is indicative of the electrodes standing insertion into living tissue.

Electrical continuity exists between the top of the CNT layer and the electrode on both types of electrodes. The fact that the resistance is high on electrodes type-B may be due to some contact loose when removing the interlayer.

The MWCNT modification of the electrodes has been demonstrated to improve the impedance of the platinum electrodes. However, the improvement has been found to be more significant in the case of the smaller electrodes, maybe because of an amorphous carbon deposition on the walls of the CNTs.

10.4 The MWCNT modified electrodes vs. the previous electrodes from GAB

This section compares the fabrication and the characteristics of the above evaluated *type-A* electrodes with those previously developed by GAB: the bare platinum electrodes, the black platinum modified electrodes and electrodes where SWCNTs had been deposited (section 10.1) [31].

10.4.1 Fabrication yield comparison

Figure 10.26 shows images of the four different types of electrodes: a 40 μm platinum electrode (Figure 10.26-a), a 40 μm black platinum modified electrode (Figure 10.26-b), a 300 μm modified with SWCNT electrode (Figure 10.26-c) and a CVD 300 μm electrode that has been modified with selectively synthesised MWCNTs (Figure 10.26-d).

As described previously (section 10.1.1), the platinum electrodes are fabricated at 4 inch wafer scale by conventional processes. Therefore, the fabrication yield of the base electrodes is high. On the other hand, the fabrication yield of the black platinum and SWCNT modified electrodes is low since the processes are performed manually and electrode by electrode (section 10.1.2). Furthermore, these modifications result in non homogeneous electrodes. Figure 10.26-b evidences the difficulties to perfectly control the deposition rate so that the black platinum is only deposited on the electrode area. Regarding the SWCNT modification of the electrodes (Figure 10.26-c), as it is discussed in [31], the process is uniform up to 100 μm electrodes since it results in a non-uniform coverage of bigger electrodes. Moreover, as the selective deposition is performed by a shadow mask a good alignment of the CNT area with respect to the electrodes is difficult to be achieved.

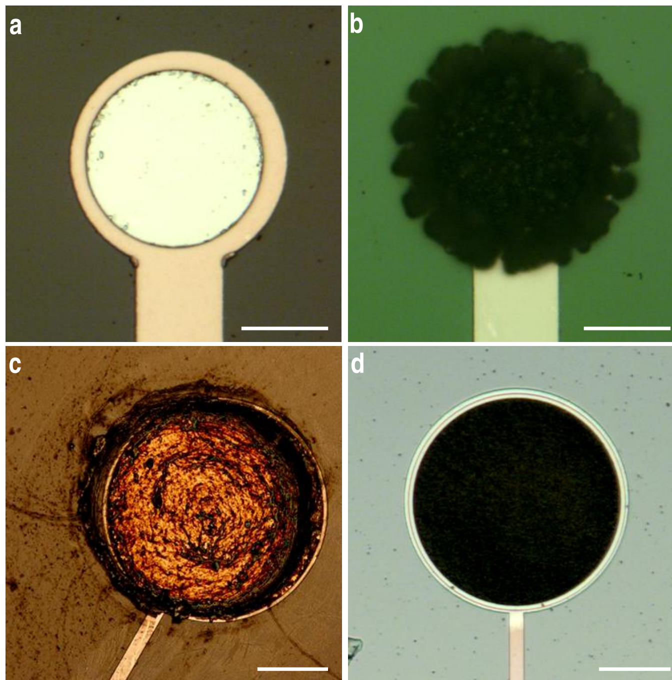


Figure 10.26: Images of the different types of electrodes: (a) bare platinum electrode; (b) modified with black platinum electrode; (c) modified with deposited SWCNTs electrode; (d) modified with synthesized MWCNTs electrode. Scale bars are 20 µm in (a-b) and 100 µm in (c-d).

Besides, the fabrication yield of the electrodes that are modified by the selective synthesis of MWCNTs is high (Figure 10.26-d) since the devices are fabricated at wafer level and by conventional process steps. Therefore, the fabrication of these devices results in a homogeneous coverage of the electrodes. The growth of this CNT array will never overflow the sensing area (as in the cases of the black platinum and the SWCNT deposition) since CNTs only grow where the catalyst material has previously been deposited. Additionally, the electrodes can be made as big or as small as desired and, as shown in section 10.1.2, the morphology of the CNT array can be tuned by optimising the CNT catalyst deposition and the CVD synthesis conditions.

Regarding the mechanical stability of the electrodes, experiments by GAB had concluded that the black platinum and SWCNT modified electrodes were not very stable since the black platinum layer is frail and the SWCNTs detach from the electrode. Presented in this chapter results for the mechanical characteristics of the electrodes *type-A* have demonstrated that the CNTs do not detach from the electrodes and, thus, that their stability is good.

Table 10.2: Comparison of the fabrication and stability of the different types of electrodes.

	Platinum	Black platinum	Deposited SWCNT	Synthesized MWCNT
Fabrication	Batch	Batch + post-processing	Batch + post-processing	Batch
Sample size	4” wafer level	Chip	Chip	4” wafer
Fabrication yield	High	Low	Low	High
Electrode size	Any	Any	Not uniform if $\Phi \geq 100$ µm	Any
Elec. stability	High	Low	Low	High

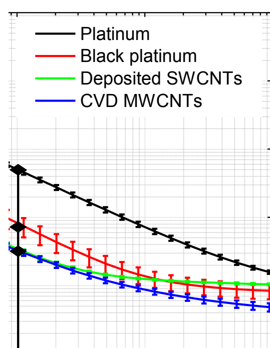
Table 10.2 summarizes a comparison on the fabrication of the different types of electrodes.

10.4.2 Electrochemical characteristic comparison

The electrochemical characteristics of the electrodes *type-A* was compared to that of the previously developed by GAB electrodes: bare platinum electrodes, black platinum modified electrodes and deposited SWCNT modified electrodes (section 10.1).

With respect to the impedance characterization of the electrodes (Figure 10.27), the main issues to be highlighted are the following. First, the n parameter for the MWCNT-modified electrodes was found to be the lowest. This indicated that the surface roughness was maximum in those electrodes. Second, the calculations of the values of Q indicate that it was also maximum for the MWCNT-modified electrodes. Finally, the fact that Rs was minimum in the MWCNT-modification case is also noticeable since the MWCNTs had not been pretreated to remove any amorphous carbon on their walls nor to generate carboxylic groups to enhance the electron exchange electrochemical reaction as it had been done in the case of the deposited SWCNTs.

Figure 10.28 is a comparison of the voltammograms of the 4 different types of electrodes (scan rate is 200 mV/s). The voltammograms comparison confirms that the capacitance of the MWCNT modified electrodes is the biggest since the characteristic of the MWCNT modified electrode is the one showing the highest charge accumulation.



	Q	n
Bare platinum	$7.2\cdot10^{-8}$	0.91
Black platinum	$4.16\cdot10^{-9}$	0.93
Deposited SWCNT	$1.03\cdot10^{-8}$	0.94
Synthesised MWCNTs	$5.1\cdot10^{-8}$	0.72

Figure 10.27: Comparative of the impedance characteristics of the different types of the analysed 40 µm electrodes and summary of the equivalent lectrode-electrolyte interphase parameters.
Impedance characteristics of the bare platinum electrode, the black platinum and the deposited SWCNT electrodes courtesy of Dr. Gemma Gabriel.

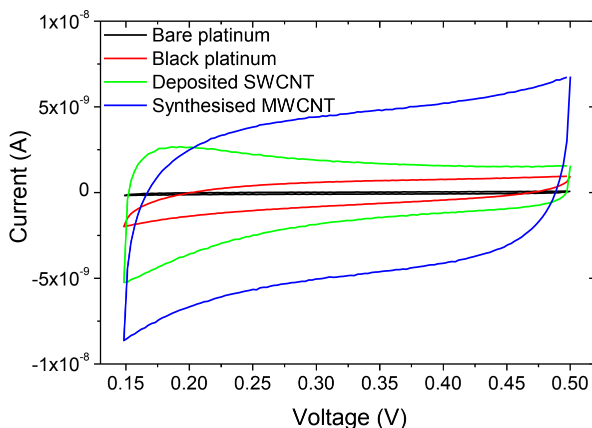


Figure 10.28: Comparison of the voltamogrammes for the different 40 µm in diameter electrodes. Scan rate 200 mV/s.

The capacitance of the different electrodes was calculated as in 10.3.3 by doing different measurements at different scan rates. Table 10.3 summarises the calculated capacitances for each of the electrodes. The table shows that the capacitance for the MWCNT-modified electrodes significantly improves that of the previous developed electrodes.

	C (nF)	A (µm2)	$^{C}/_{A}$ $(^{\mu F}/_{cm^2})$
Bare Platinum	0.6	(Φ = 40 µm) 1,257	48
Black platinum	6.3	(Φ = 55 µm) 2,376	265
Deposited SWCNTs	19	(Φ = 40 µm) 1,257	1,512
Synthesized MWCNTs	45.1	(Φ = 36 µm) 1,018	4,431

Table 10.3: Comparison of the capacitances of the previously developed MEAs and the optimised MWCNT-modified electrodes.

10.4.3 Conclusions on the performance of the MWCNT modified electrodes

In terms of the device fabrication, the yield of the here developed electrodes is higher than that of the black platinum or that of the deposited SWCNT based electrodes because the process is based on conventional fabrication steps that are homogeneous and reproducible at wafer level.

Regarding their electrochemical characteristics, the experiments have shown that the increase of the roughness of the MWCNT modified electrodes results in an improvement of the capacitance. Besides, it has to be taken into account that presented results could further be improved by optimising the CNT array either by optimising other CNT structures and/or other CNT array morphologies, or by optimising during-growth and/or post-growth purification steps to minimise the amorphous carbon on the walls and to generate free edges to favour the electron exchange.

10.5 Other experiments based on the MWCNT modified electrodes

The MWCNT modified electrodes have been/are being utilised in experiments on bio-electrochemical detection and in experiments on recording of the electrical signal from neurons. The subsequent sections overview these experiments.

10.5.1 Bio-compatibility of the MWCNT modified electrodes

MEAs were utilised by the *Unidad de Neuroprótesis y Rehabilitación Visual* of the *Instituto de Bioingeniería* of *Universidad Miguel Hernández* (UMH) for a preliminary check of the bio-compatibility of the CNTs on the electrodes since, as described in the previous chapter (section 9.2), it is a controversial issue.

The experimental setup consisted in a 3 day cell culture of neurons from the hippocampus rats on the MEAs. The observation of the electrodes after that period (Figure 10.29) determined that the cell culture was viable and that the neurons tent to grow on top of the electrodes where the CNTs had selectively been synthesised. Thus, the experiment suggested that the CNT modified electrodes were bio-compatible for this experimental setup.

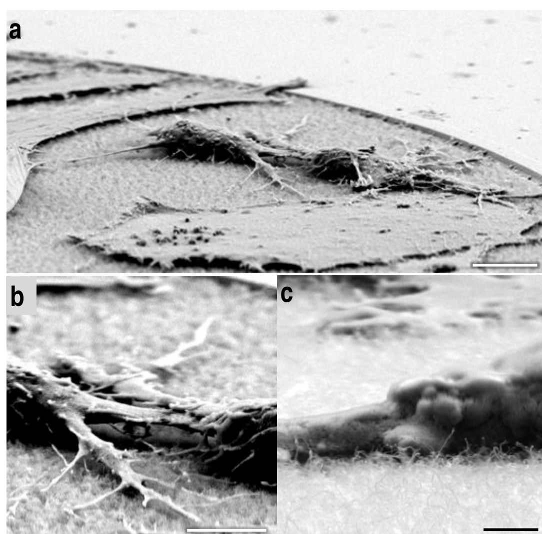


Figure 10.29: SEM images of the cell culture experiments on the CNT modified electrodes. (a) Image of neurons on the electrode. (b-c) Detail of the neurons in a. Scale bars are 10, 5 and 1 µm in a, b and c, respectively.

10.5.2 CNTs functionalization for label free electrochemical bio-detection

Researchers from the group of Sensors and Biosensors of UAB are developing CNT functionalization protocols for the bio-detection based on DNA hybridization or on the use of aptamers in a similar way to described in section 8.4.1.

In the case of the procedures based on the DNA hybridization, different protocols for the DNA attachment to the CNTs and the detection of the DNA hybridization have been developed. Regarding the DNA attachment procedures, protocols based on the physical absorption or on the single-point covalent attachment (which is more flexible since it enhances the DNA hybridization) are being developed. Regarding the detection procedures, the direct (irreversible) oxidation of certain bases of the DNA or the reversible oxidation and reduction of redox indicators that are included to the solution are being investigated.

For example, Figure 10.30-a shows a schematic of a single point attachment functionalization of the CNTs where the DNA hybridization is detected by electrostatic accumulation of a cationic redox marker. Figure 10.30-b presents the peak-to-peak potential separation (ΔE_p) in the cyclic voltammogram at different stages of the electrode functionalization process, for different hybridizations (complementary (polyC) and not complementary (PolyT) DNA strands) and for different

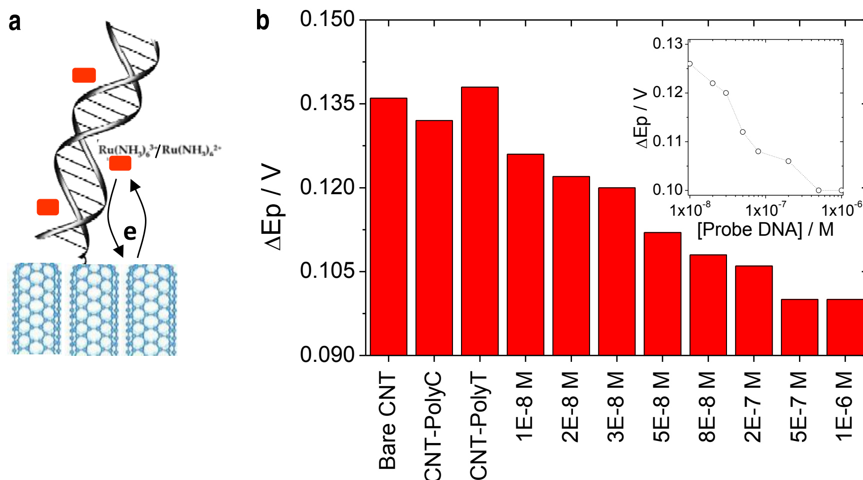


Figure 10.30: (a) Schematic of the detection of the DNA hybridization by a cationic redox marker. (b) Comparison of the ΔE_p of the electrode before and after the functionalization and for different complementary strands concentrations. The inset shows the ΔE_p variation according to the complementary strand concentration. Figures courtesy of Dr. M.J. Esplandiu.

concentrations of the complementary DNA strand. The graph shows how the electron transfer kinetics are enhanced because of the accumulation of the cationic markers at the interface when the hybridization occurs. The inset shows the sensitivity of the detection.

10.5.3 Study on the emergent activity in cortical networks

GAB works together with the group of Prof. M.V. Sanchez-Vives at the *Institut d'Investigacions Biomèdiques August Pi i Sunyer* (IDIBAPS) in the understanding of the operation of the cerebral cortex by the analysis of the electrical response of neurons. In this frame, different in electrode structure MEAs (bare platinum, black platinum modified electrodes, deposited SWCNT modified electrodes, and CVD grown MWCNTs modified electrodes) are being utilized to record the spontaneous rhythmic activity generated by ferret cortical slices [41] before and after blockade of inhibition.

Figure 10.31 includes two photographs of the experiment setup. Figure 10.31-a is a photograph of the general view of the MEA, the plate where it was assembled and the rest of the accessories for perfusion and measurement. Figure 10.31-b shows detail of the cortex slide on the MEA, of the ring lid, of the perfusion inlet and outlet and of a tungsten wire electrode that was also used in the experiments. The recordings were obtained at physiological temperatures and under conditions close to an interface chamber [42].

Figure 10.32 shows the spontaneous activity that was recorded from the tissue when using electrodes from a CVD grown MWCNT modified MEA (E1-E7) and a tungsten wire that was inserted into the tissue (EW). Figure 10.32-a shows that the same signal was recorded by the tungsten electrode and the electrodes on the MEA. Moreover, the signal on the electrodes presented a lower signal-to-noise ratio that allowed registering higher signal levels. Figure 10.32-b depicts an epileptic discharge that was recorded by the tungsten electrode and by the MWCNT modified electrodes. The only electrode that appeared not to be in contact with the tissue was electrode E3.

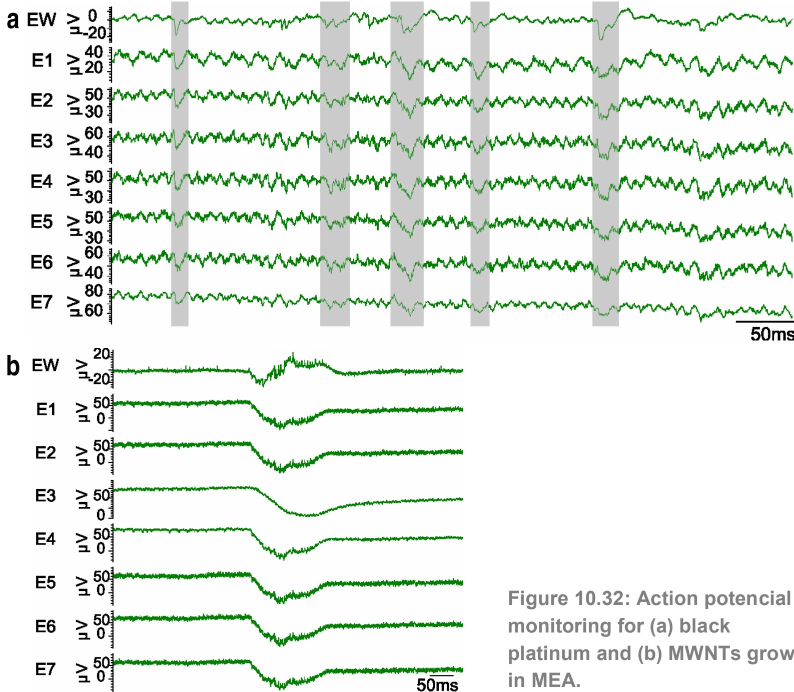


Figure 10.32: Action potencial monitoring for (a) black platinum and (b) MWNTs grown, in MEA.

It has to be highlighted that the obtained results were the most positive among the experiments with the different types of MEAs as no activity was recorded in the other cases (bare platinum, black platinum, deposited SWCNTs). Therefore, it may be concluded that the CVD grown MWCNT modification of the electrodes enhanced the interaction between the tissue and the electrode as previously demonstrated [20, 22]. This signal enhancement is attributed to mechanical and electrochemical effects. On the one side, the MWCNT modification enhances a better contact of the tissue and the electrode due to the increase of the roughness of the surface of the electrode (section 10.3.1) and to the Velcro effect of the CNT layer on the neurons. On the other side, the found increased capacitance for these electrodes (section10.3.3) increases the charge transfer and improves the signal registering enabling the measurement of higher signals.

More work is in progress. Now, efforts are being oriented to the optimization of the measurement setup and to the optimization of the MEA design for the tissue to live for longer periods of time (see Annex 2).

Chapter conclusions

A technological process for the wafer scale fabrication of CNT integrated electrodes for bio-electrochemical sensing applications has been demonstrated at 4 inch wafer level.

Regarding the fabrication of the electrode:

- A strategy based on the use of a silicon oxide layer for the inhibition of the CNT catalyst diffusion to the metal electrode and to enhance the synthesis of dense arrays of CNTs has been demonstrated at wafer level.
- The wafer scale integration of very dense vertically aligned MWCNTs has been demonstrated at wafer level on silicon (4 inch) and silicon carbide (3 inch) substrates. Additionally, the CNT synthesis process has been optimised so that a bio-compatible material is used to synthesise the CNTs so that only bio-compatible materials are utilised in the fabrication.
- Optimised CNT synthesis parameters have led to the fabrication of two different in morphology vertically aligned CNT layer electrodes.

Regarding the characterization of the MWCNT-modified electrodes:

- The mechanical characterization of the MWCNT-modified electrodes has demonstrated that their stability depends on the morphology of the CNT layer and on the interlayer between the metal electrode and the CNTs.
- The electrical characterization has demonstrated electrical continuity between the electrode and the top of the CNT array. However, it has also evidenced that the interlayer between the electrode and the CNTs has to be optimised to minimise the loose of contact between the electrode and the CNTs when certain morphology CNT arrays are synthesised.
- The electrochemical characterization of the electrodes *type-A* has revealed an improvement of the impedance of the electrodes due to the increase of the roughness of the surface of the electrode.

Regarding the comparison of the MWCNT-modified electrodes with the previously developed electrodes:

- The fabrication yield of the MWCNT-modified electrodes is higher than for the other modified electrodes since the fabrication processes is only composed of conventional fabrication steps. Moreover, the process results in electrodes that are more homogeneous, since the processes are uniform at wafer level, and enables the fabrication of any size electrodes.
- The electrochemical characteristics of the 40 µm MWCNT-modified electrodes improve those of the previously developed electrodes, mainly, because of the high increase of the active area.

In conclusion, the developed technological process is a step forward to the fabrication of electrodes for bio-electrochemical applications since their fabrication and their characteristics improve those of the previous electrodes. The fabricated devices are now being used in research works on bio-electrochemical detection and on the recording of the activity of the cortex tissue.

Outlook

This section has evaluated the wafer scale integration of dense vertically aligned arrays of CNTs on the metal electrodes of previously demonstrated electrodes for bio-sensing applications.

The proposed CNT integration process has been demonstrated to be successful. On the one hand, the fabrication yield of these electrodes compared to that of the previous electrodes is higher since the processes steps are conventional and they are performed at wafer level. On the other hand, fabricated electrodes exhibit mechanical, electrical and electrochemical characteristics that improve those of the previous devices.

However, even if the results have been positive, there are still aspects of the fabrication that may be improved to increase the fabrication yield and/or their mechanical, electrical and bio-electrochemical characteristics. Regarding the CNT integration process, it would be desirable to optimise the CNT-electrode interlayer so that it would be conductive. This way, its removal would not be necessary and the mechanical adherence of the CNTs to the electrode would not be damaged. Besides, it would be desirable to optimise the CNT synthesis conditions so that different in structure CNTs (i.e. SWCNTs and bamboo like MWCNTs) could also be integrated.

The fabricated devices have been demonstrated to be valuable for bio-electrochemical experiments and to study the activity from a tissue. It is worth remembering, at this point, that the use of the MWCNT-modified electrodes has enabled, for the first time by our experimental setup, the recording of the signal from a cortex slide. In this sense, improvement of the design of the MEA to enable the respiration of the deposited on the electrodes tissue would highly improve the experimental setup and enable a data acquisition for longer time periods.

References

1. L.A. Geddes 1972 Electrodes and the Measurement of Bioelectric Events (New York: Wiley)
2. C.A. Marrese, Preparation of strongly adherent platinum black coatings, Analytical Chemistry, 1987. **59**(1): p. 217-218.
3. S.J. Paik, Y. Park, and D.I. Cho, Roughened polysilicon for low impedance microelectrodes in neural probes, Journal of Micromechanics and Microengineering, 2003. **13**(3): p. 373-379.
4. P.D. Van Der Wal, M. Dadras, M. Koudelka-Hep, and N.F. Rooij, Modification of the surface roughness of platinum thin film electrodes by alloy formation with aluminium, 206th Meeting of Electrochemical Society, 2004.
5. A. Hirsch, Functionalization of single-walled carbon nanotubes, Angewandte Chemie - International Edition, 2002. **41**(11): p. 1853-1859.
6. A. Ivorra, R. Gomez, N. Noguera, R. Villa, A. Sola, L. Palacios, G. Hotter, and J. Aguilo, Minimally invasive silicon probe for electrical impedance measurements in small animals, Biosensors & Bioelectronics, 2003. **19**(4): p. 391-399.
7. P.L. Walker and L.R. Rarovic, *Chemistry and Physics of carbon*, New York.
8. K. Kinishita, *Carbon Electrochemical and Physicochemical properties*. 1988, New York: John Wiley & Sons.
9. C.A. Leon y leon and L.R. Radovic, *In Chemistry and Physics of Carbon*, ed. P.A. Thrower. Vol. 24. 1994, New York: Dekker.
10. R.L. McCreery, Advanced carbon electrode materials for molecular electrochemistry, Chemical Reviews, 2008. **108**(7): p. 2646-2687.
11. S. Iijima, Helical Microtubules of Graphitic Carbon, Nature, 1991. **354**(6348): p. 56-58.
12. R.H. Baughman, A.A. Zakhidov, and W.A. de Heer, Carbon nanotubes - the route toward applications, Science, 2002. **297**(5582): p. 787-792.
13. E. Bekyarova, Y. Ni, E.B. Malarkey, V. Montana, J.L. McWilliams, R.C. Haddon, and V. Parpura, Applications of carbon nanotubes in biotechnology and biomedicine, J. Biomedical Nanotechnology, 2005. **1**(1): p. 3-17.
14. Y. Yun, Z. Dong, V. Shanov, W.R. Heineman, H.B. Halsall, A. Bhattacharya, L. Conforti, R.K. Narayan, W.S. Ball, and M.J. Schulz, Nanotube electrodes and biosensors, Nano Today, 2007. **2**(6): p. 30-37.
15. J.J. Gooding, Nanostructuring electrodes with carbon nanotubes: A review on electrochemistry and applications for sensing, Electrochimica Acta, 2005. **50**(15): p. 3049-3060.
16. M. Pacios, M. del Valle, J. Bartroli, and M.J. Esplandiu, Electrochemical behavior of rigid carbon nanotube composite electrodes, Journal of Electroanalytical Chemistry, 2008. **619-620**(1-2): p. 117-124.

17. V.M. Tiainen, Amorphous carbon as a bio-mechanical coating-mechanical properties and biological applications, Diamond and Related Materials, 2001. **10**(2): p. 153-160.

18. S. Garibaldi, C. Brunelli, V. Bavastrello, G. Ghigliotti, and C. Nicolini, Carbon nanotube biocompatibility with cardiac muscle cells, Nanotechnology, 2006. **17**(2): p. 391-397.

19. T. Gabay, M. Ben-David, I. Kalifa, R. Sorkin, Z.R. Abrams, E. Ben-Jacob, and Y. Hanein, Electro-chemical and biological properties of carbon nanotube based multi-electrode arrays, Nanotechnology, 2007. **18**(3).

20. E.W. Keefer, B.R. Botterman, M.I. Romero, A.F. Rossi, and G.W. Gross, Carbon nanotube coating improves neuronal recordings, Nature Nanotechnology, 2008. **3**(7): p. 434-439.

21. C.A. Poland, R. Duffin, I. Kinloch, A. Maynard, W.A.H. Wallace, A. Seaton, V. Stone, S. Brown, W. MacNee, and K. Donaldson, Carbon nanotubes introduced into the abdominal cavity of mice show asbestos-like pathogenicity in a pilot study, Nature Nanotechnology, 2008. **3**(7): p. 423-428.

22. G. Cellot, E. Cilia, S. Cipollone, V. Rancic, A. Sucapane, S. Giordani, L. Gambazzi, H. Markram, M. Grandolfo, D. Scaini, F. Gelain, L. Casalis, M. Prato, M. Giugliano, and L. Ballerini, Carbon nanotubes might improve neuronal performance by favouring electrical shortcuts, Nature Nanotechnology, 2009. **4**(2): p. 126-133.

23. S.Y. Hong, G. Tobias, K.T. Al-Jamal, B. Ballesteros, H. Ali-Boucetta, S. Lozano-Perez, P.D. Nellist, R.B. Sim, C. Finucane, S.J. Mather, M.L.H. Green, K. Kostarelos, and B.G. Davis, Filled and glycosylated carbon nanotubes for in vivo radioemitter localization and imaging, Nature Materials, 2010. **9**(6): p. 485-490.

24. G. Gabriel, R. Gómez, M. Bongard, N. Benito, E. Fernández, and R. Villa, Easily made single-walled carbon nanotube surface microelectrodes for neuronal applications, Biosensors and Bioelectronics, 2009. **24**(7): p. 1942-1948.

25. E. Mendoza, J. Orozco, C. Jime?nez-Jorquera, A.B. Gonza?lez-Guerrero, A. Calle, L.M. Lechuga, and C. Ferna?ndez-Sa?nchez, Scalable fabrication of immunosensors based on carbon nanotube polymer composites, Nanotechnology, 2008. **19**(7).

26. J. Li, H.T. Ng, A. Cassell, W. Fan, H. Chen, Q. Ye, J. Koehne, J. Han, and M. Meyyappan, Carbon nanotube nanoelectrode array for ultrasensitive DNA detection, Nano Letters, 2003. **3**(5): p. 597-602.

27. T.D.B. Nguyen-Vu, H. Chen, A.M. Cassell, R.J. Andrews, M. Meyyappan, and J. Li, Vertically aligned carbon nanofiber architecture as a multifunctional 3-D neural electrical interface, IEEE Transactions on Biomedical Engineering, 2007. **54**(6): p. 1121-1128.

28. K. Hata, D.N. Futaba, K. Mizuno, T. Namai, M. Yumura, and S. Iijima, Water-assisted highly efficient synthesis of impurity-free single-waited carbon nanotubes, Science, 2004. **306**(5700): p. 1362-1364.

29. Z.F. Liu, Z.Y. Shen, T. Zhu, S.F. Hou, L.Z. Ying, Z.J. Shi, and Z.N. Gu, Organizing single-walled carbon nanotubes on gold using a wet chemical self-assembling technique, Langmuir, 2000. **16**(8): p. 3569-3573.

30. H. Liu, S. Li, J. Zhai, H. Li, Q. Zheng, L. Jiang, and D. Zhu, Self-assembly of large-scale micropatterns on aligned carbon nanotube films, Angewandte Chemie - International Edition, 2004. **43**(9): p. 1146-1149.

31. G. Gabriel, R. Gómez-Martínez, and R. Villa, Single-walled carbon nanotubes deposited on surface electrodes to improve interface impedance, Physiological Measurement, 2008. **29**(6): p. S203-S212.

32. S. Wolf, Silicon Processing for the VLSI Era, Vol. 2: Process Integration. 1990: Lattice Press.

33. F. Javier del Campo, J. Garcia-Cespedes, F. Xavier Munoz, and E. Bertran, Vertically aligned carbon nanotube based electrodes: Fabrication, characterisation and prospects, Electrochemistry Communications, 2008. **10**(9): p. 1242-1245.

34. G. Gabriel, I. Erill, J. Caro, R. Gómez, D. Riera, R. Villa, and P. Godignon, Manufacturing and full characterization of silicon carbide-based multi-sensor micro-probes for biomedical applications, Microelectronics Journal, 2007. **38**(3): p. 406-415.

35. M. Tijero, G. Gabriel, J. Caro, A. Altuna, R. Hernández, R. Villa, J. Berganzo, F.J. Blanco, R. Salido, and L.J. Fernández, SU-8 microprobe with microelectrodes for monitoring electrical impedance in living tissues, Biosensors and Bioelectronics, 2009. **24**(8): p. 2410-2416.

36. A.J. Rosenbloom, D.M. Sipe, Y. Shishkin, Y. Ke, R.P. Devaty, and W.J. Choyke, Nanoporous SiC: A candidate semi-permeable material for biomedical applications, Biomedical Microdevices, 2004. **6**(4): p. 261-267.

37. A. Jorio, G. Dresselhaus, and M.S. Dresselhaus, Carbon Nanotubes: Advanced Topics in the Synthesis, Structure, Properties and Applications. 2008, New York: Springer.

38. A.C. Dupuis, The catalyst in the CCVD of carbon nanotubes-a review, Progress in Materials Science, 2005. **50**(8): p. 929-961.

39. L. Zhang, Z.R. Li, Y.Q. Tan, G. Lolli, N. Sakulchaicharoen, F.G. Requejo, B.S. Mun, and D.E. Resasco, Influence of a top crust of entangled nanotubes on the structure of vertically aligned forests of single-walled carbon nanotubes, Chemistry of Materials, 2006. **18**(23): p. 5624-5629.

40. X. Muñoz-Berbel, N. Godino, O. Laczka, E. Baldrich, F.X. Muñoz, and F.J. del Campo, Impedance-Based Biosensors for Pathogen Detection, in Principle of Bacterial Detection: Biosensor, Recognition Receptors and Microsystems, Mohammed Zourob, Sauna Elwary, Anthony P. F Turner Editor. 2008, Springer.

41. M.V. Sanchez-Vives and D.A. McCormick, Cellular and network mechanisms of rhythmic recurrent activity in neocortex, Nature Neuroscience, 2000. **3**(10): p. 1027-1034.

42. R. Reig, M. Mattia, A. Compte, C. Belmonte, and M.V. Sanchez-Vives, Temperature Modulation of Slow and Fast Cortical Rhythms, J Neurophysiology, 2010. **103**(3): p. 1253-1261.

General conclusions

This thesis has dealt with the optimization of the CNT synthesis by RTCVD and with the wafer scale integration of CNTs into FET and sensing applications. Despite the inherent problematic of the technological process developments, most the initially foreseen goals have been fulfilled.

The use of the RTCVD technique has been validated for the synthesis of SW and for MWCNTs, Synthesis of CNTs by conventional (mainly iron and nickel) and by nonconventional (platinum) catalyst materials has been optimised. Besides, it is remarkable how the CNT synthesis processes have been standardized at 4 inch wafer scale for either low density of SWCNTs or for dense, vertically aligned arrays of MWCNTs.

Iron has been the catalyst material used **to establish the influence of the RTCVD process parameters** on the CNT synthesis. In addition, it has also been utilized for the synthesis of SWCNTs in the CNT-FET applications. Besides, the results on the **synthesis of SWCNTs from catalyst particles inside the pores of zeolite L crystals** are to be highlighted as a promising strategy to overcome the challenges on the control over the structure of the SWCNTs and on the control over their orientation.

When using **nickel silicide**, positive results have been attained on the growth of MWCNTs and on the control of their density. Even if SWCNT synthesis has not been achieved, presented tasks constitute a step forward to the synthesis of SWCNTs since they confirm the strategies for the integration of thinner CNTS (SWCNTs).

Platinum has been proved to be as active as iron for CNT synthesis, since platinum deposition and RTCVD optimization have led to the synthesis of either **isolated SWCNTs** or **vertically aligned arrays of MWCNTs**. These results are relevant as platinum is a material that has seldom been used in CNT synthesis and because, due to its properties, it could be utilized in the fabrication of bio-compatible devices or in devices for catalysis applications. Furthermore, it has been demonstrated that, under certain CVD conditions, it is possible to synthesize **a MWCNT-graphene composite material** that could be used for the fabrication of novel devices and structures.

Regarding the wafer scale integration of the CNTs, two main processes have been optimised. On the one side, SWCNTs have been integrated into the fabrication of CNT-FETs. On the other side, high densities of CNTs have been integrated into metallic electrodes that had previously been demonstrated.

Regarding the **wafer scale integration of CNTs into single SWCNT CNT-FET devices**, first, **a monitor chip has been designed and fabricated to test the synthesis of the SWCNTs, the fabrication of the CNT-FETs and their electrical performance**. Additionally, a test procedure based on an automatic probe measurement and a three-current-characterization has been developed to enable the identification of the electric characteristics of each device. This procedure has identified **more than 10,000 CNT-FET as functional transistors on a 4 inch wafer, which is, most probably, the largest fabrication of CNT-FETs on a wafer reported to date.**

Then, the technology has been upgraded for the fabrication of **CNT-FET based sensors for bio-electrochemical sensing by optimizing a procedure** to passivate the CNT-FETs. Even if this procedure is based on E-Beam lithography, a semiautomatic alignment process has been optimized for the process to be scalable to wafer level. The developed procedure may also be used for the fabrication of optimized CNT-FETs, for the fabrication of other CNT-based sensors or for the fabrication of CNT-based NEMS.

Regarding the **wafer scale integration of CNTs into metallic electrodes**, a process for the synthesis of arrays of high density of vertically aligned MWCNTs on platinum electrodes has been demonstrated. The MWCNT modified electrodes show positive mechanical, electrical and electrochemical properties. **The comparison of these electrodes with previously reported ones** (bare platinum electrodes, black platinum modified electrodes and manually deposited SWCNTs) evidences that **the fabrication yield is highly improved** for the MWCNT modified electrodes. Regarding their electrochemical characteristics, the MWCNT modified electrodes show **improved electrochemical characteristics due to the increase of the roughness** of their surface. The capacitance of these electrodes results in an improved signal to noise ratio on the measurements and, thus, has enabled the recording of the activity from cortical slices.

In conclusion, the results that are presented in this thesis are **a step forward to the VLSI of CNTs**. The developed processes are of interest in the field of **nanoelectronics**, in the field of **bio-electrochemical sensing**, for the fabrication of **optoelectronic devices** and for the fabrication **NEMS**.

Perspective

Even if the main objectives have been accomplished, efforts may still be the dedicated to optimise some of the fabrication steps and the testing procedures to reach a higher fabrication yield.

Regarding the CNT-FETs, different issues may be addressed to improve their fabrication and their testing. The integration of zeolite L crystals to grow constricted in diameter and oriented SWCNT is, perhaps, the most challenging upgrade of the process but, at the same time, it could result in overcoming the main challenges that hinder the integration of SWCNTs. An easy to implement optimization of the process would be the improvement of the CNT-metal contact. Besides, the optimization of the device identification procedure could be addressed so that devices were more accurately labelled and so that the complete characterization of the functional transistors would be made automatically. Furthermore, the testing procedure could be programmed to improve the performance of the CNT-FETs by burning out the metallic SWCNTs.

Regarding the fabrication of the CNT modified electrodes, they could be further be optimized to achieve more robust electrodes and to improve their electrical and bio-electrochemical characteristics. A possible upgrade would consist in optimizing an electrode-to-CNT interlayer so that this layer would not need to be removed. Another improvement that should be addressed is the optimization of the CNT synthesis in order to grow other structure CNTs (i.e. SWCNTs and bamboo like CNTs). Moreover, efforts should also be dedicated to the optimization of purification strategies. Strategies based on hydrogen, thermal or plasma treatments, which are already being studied, would be the most compatible with the wafer scale fabrication of the electrodes.

ANNEXES

Annex 1: List of publications

Peer reviewed articles:

1 **I. Martin-Fernandez**, X. Borrise, P. Godignon, E. Lora-Tamayo, F. Perez-Murano, “Batch wafer scale fabrication of passivated carbon nanotube transistors for electrochemical sensing applications”, Journal of Vacuum Science and Technology B **28** (2010), C6P1-C6P5.

2 **I. Martin-Fernandez**, M. Sansa, M.J. Esplandiu, E. Lora-Tamayo, F. Perez-Murano, P. Godignon, “Massive manufacture and characterization of single-walled carbon nanotube field effect transistors”, Microelectronic Engineering **87** (2010), 1554-1556.

3 **I Martin-Fernandez**, G. Gabriel, G. Rius, R. Villa, F. Perez-Murano, E. Lora-Tamayo, P. Godignon, “Vertically aligned multi-walled carbon nanotube growth on platinum electrodes for bio-impedance applications”, Microelectronic Engineering **86** (2009), 806–808.

4 G. Rius, G., A. Verdaguer, F.A. Chaves, **I. Martín,** P. Godignon, E. Lora-Tamayo, D. Jiménez, F. Pérez-Murano, "Characterization at the nanometer scale of local electron beam irradiation of CNT based devices", Microelectronic Engineering **85** (2008), 1413-1416.

5 **I. Martin**, G. Rius, P. Atienzar, L. Teruel, N. Mestres, F. Perez-Murano, H. Garcia, P. Godignon, A. Corma, E. Lora-Tamayo, “CVD oriented growth of carbon nanotubes using AlPO4-5 and L type zeolites”, Microelectronic Engineering **85** (2008), 1202–1205.

6 G. Rius, **I. Martín,** P. Godignon, A. Bachtold, J. Bausells, E. Lora-Tamayo, F. Pérez-Murano, “Response of carbon nanotube transistors to electron beam exposure” Microelectronic Engineering **84** (2007) 1596–1600.

Conference proceedings:

7 P. Godignon, **I. Martin**, G. Gabriel, R. Gomez, M. Placidi and R. Villa, “New generation of SiC based biodevices implemented on 4” wafers”, Materials Science Forum Vols. 645-648 (2010), 1097-1100.

8 **I. Martin-Fernandez**, M. Sansa, E. Lora-Tamayo, F. Perez-Murano, P. Godignon, “A test vehicle and a two step procedure to evaluate a massive number of single-walled carbon nanotube field effect transistors”, Proceedings of the 2010 IEEE International Conference on Microelectronic Test Structures (2010), 48-51.

9 **I. Martin**, G. Rius, G. Gabriel, M.J. Esplandiu, N. Mestres, F. Perez-Murano, E. Lora-Tamayo, P. Godignon, “Local growth of carbon nanotubes by thermal chemical vapor deposition from iron based precursor nanoparticles”, Proceedings of the 2007 Spanish Conference on Electron Devices (2007), 329-332.

In preparation:

- Single-walled carbon nanotube based microsensors for nerve agent simulants detection , M.C. Horrillo, J. Martí, D. Matatagui, J.P.Santos, I. Sayago, J. Gutiérrez, **I. Martín-Fernández**, P. Ivanov, I. Grácia, C. Cané (submitted to Sensors and Actuators).
- Biocompatible MWNTs-based MEAs for the study emergent activity in the cortical network.
- RTCVD synthesis of a CNT-graphene composite.
- RTCVD synthesis optimization of CNTs by various platinum based catalyst materials.

Annex 2: Other CNT-based devices

This annex introduces other devices based on CNTs that have not been included in the main part of the document because they are still under development or because their fabrication process required no further development with respect to the devices that are included in the main sections.

A) Selective synthesis of SWCNTs to analyse the response of carbon nanotube transistors to electron beam exposure

Selectively synthesised SWCNTs were used in the analysis of the response of CNT-FETs to e-beam exposure by Dr. Gemma Rius [1, 2]. The experiments consisted in evaluating the I-V characteristics of CNT-FETs (electrically and by AFM based techniques, in particular, by EFM and by KPFM) after selective areas of the devices had been irradiated (Fig. 1-a,b). These studies concluded that the alteration of the I-V characteristics was transient and mainly due to electron trapping in the silicon oxide layer. Therefore, these alterations could be controlled (Fig. 1-c).

These experiments resulted in the establishment of the conditions for using electron and ion beam-induced-deposition of metal to define contacts to SWCNTs so that CNT-FETs with good electrical performance can be obtained [3].

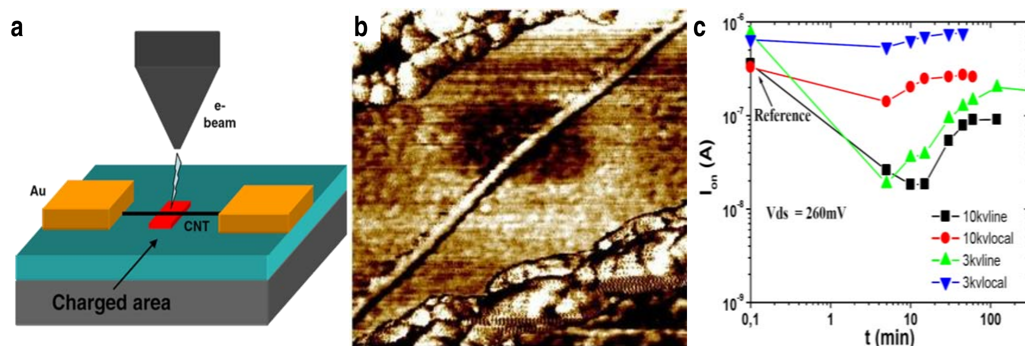


Fig. 1: (a) Schematic of the e-beam irradiation of the CNT-FET. (b) Phase AFM image of the channel of a CNT-FET after the local irradiation of the SWCNT (X,Y: 600 nm). (c) Time evolution of the on-current on the CNT-FETs for different e-beam exposures. (a) and (b-c) extracted from [2] and [1], respectively.

B) Novel structure for the measurement of the contact resistance on nanoscaled materials

A novel structure based on the classic Kelvin structure, “nanoKelvin”, (Fig. 2-a) is being explored for the measurement of the contact resistance between a metal and a nanoscaled structure [4]. This work is being performed in collaboration with Dr. Joaquín Santander and Dr. Xavier Borrisé.

The CNT-FET sensor chip platform (chapter 8) has been used as the starting point for fabrication of the “nanoKelvin” structures. The fabrication process is an upgrade of the passivation procedure and aims at patterning a stripe along the channel of the CNT-FETs to connect two consecutive liquid

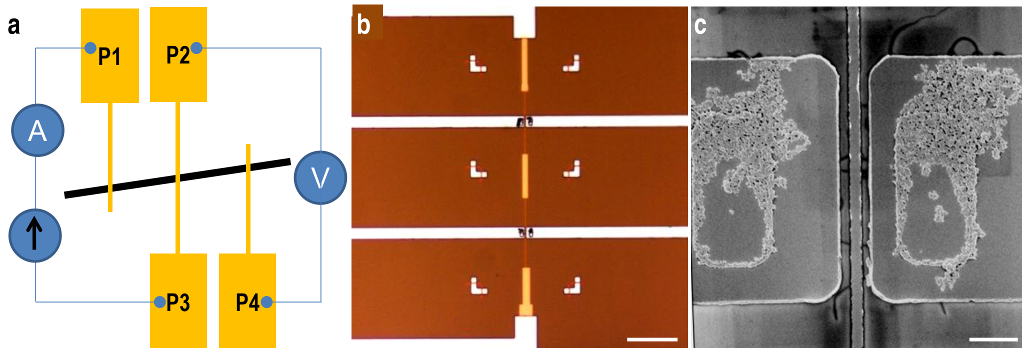


Fig. 2: (a) Schematic of the "nanoKelvin" structure and (b) optical and (c) SEM images of a fabricated structure. The optical image shows a stripe connecting two liquid polarization electrodes, top and bottom, along the channels of 2 CNT-FETs. The SEM image is a detail of the stripe along the channel of a CNT-FET. Scale bars are 50 μm in (b) and 2 μm in (c).

polarization electrodes (Fig. 2-b). A detail of a stripe along the channel of a CNT-FET is shown in Fig. 2-c.

C) Microwave characterization of arrays of SWCNTs coplanar structures

Collaboration with the AntennaLab Group at the *Universtat Politècnica de Catalunya* (UPC) has been established to evaluate the properties of arrays of SWCNTs on coplanar configurations under microwave conditions [5]. The developed tasks include the fabrication of the structures similar to that depicted in Fig. 3-a by a process analogous to that employed for the fabrication of CNT-FETs on very resistive wafers to minimise any parasitic effect on the devices. Fig. 3-b,c show part of the devices on a wafer and detail of a device where 4 SWCNTs are found between the two metal electrodes.

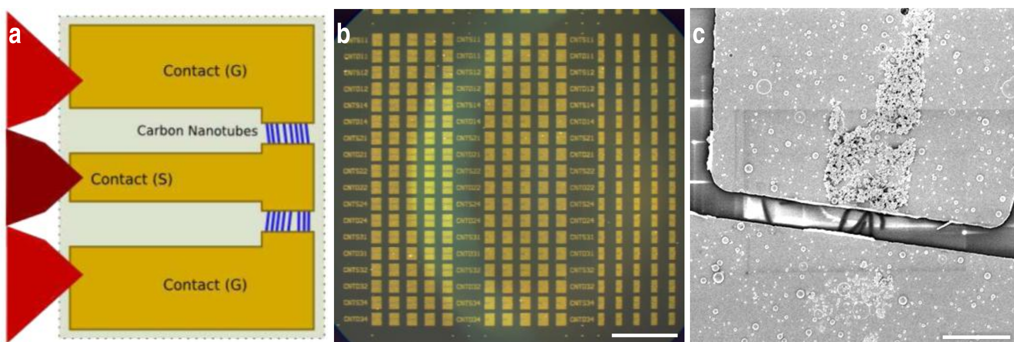


Fig. 3: (a) Schematic of the coplanar structures. (b) Optical image of some of the structures on a wafer. (c) SEM image of a structure. In this case, 4 SWCNTs were found between the two metal electrodes. Scale bars are 1 mm in b and 5 μm in c.

D) Integration of SWCNTs into microsensors for gas sensing applications

SWCNTs have been integrated into microsensors for gas detection that had been previously developed by the Gas Sensors group at CNM (Fig. 4-a) [6]. The integration of the SWCNTs consisted

in the selective synthesis of a very dense layer of SWCNTs between the electrodes of the sensors to form their transducing layer and in making compatible the synthesis of the SWCNTs with the previous and posterior device fabrication steps. Fig. 4-b,c are optical images of a gas sensor chip, which is composed of four individual sensors, and of the detail of the SWCNT layer on the membrane of the sensor, respectively. The selective synthesis was achieved by a selective deposition of the Fe/Mo/Al_2O_3 catalyst material by means of the PMMA/photoresist approach (Fig. 4-b).

Fabricated sensors are currently being used by the Gas Sensors group from the *Instituto de Física Aplicada* (IFA, CSIC) for the detection of low concentrations of stimulants of Chemical Warfare Agents such as Sarin, Soman or Distilled Mustard.

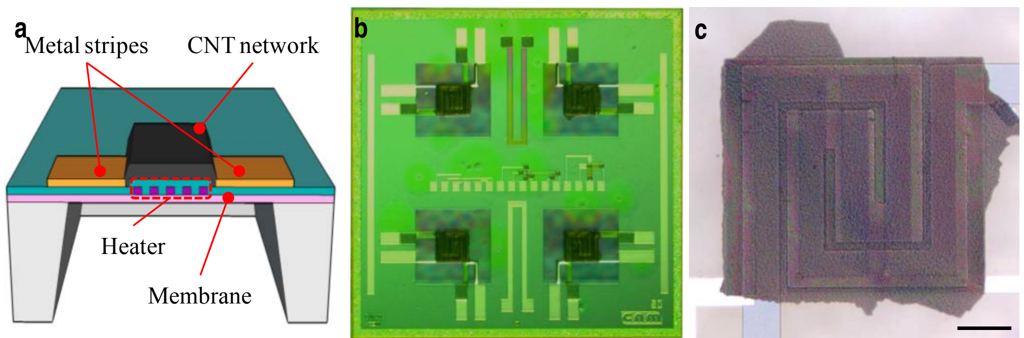


Fig. 4: (a) Schematic of the microsensor. (b) Optical image of chip containing 4 microsensors. The chip is 5 x 5 mm^2. (c) Optical image of the SWCNT layer that was synthesised on the electrodes of the sensor. Scale bars are 100 µm in c.

E) Fabrication of optimized CNT-modified MEAs

A new technological process has been developed by GAB to improve the yield of the tissue stimulation and/or recording experiments when utilising the MEAs. The optimization consists in fabricating the electrodes on top of a perforated membrane to enable double perfusion and, thus, to improve the oxygen and nutrients supply to the tissue during the experiments to inhibit its premature death. Fig. 5-a shows a schematic of a perforated MEA.

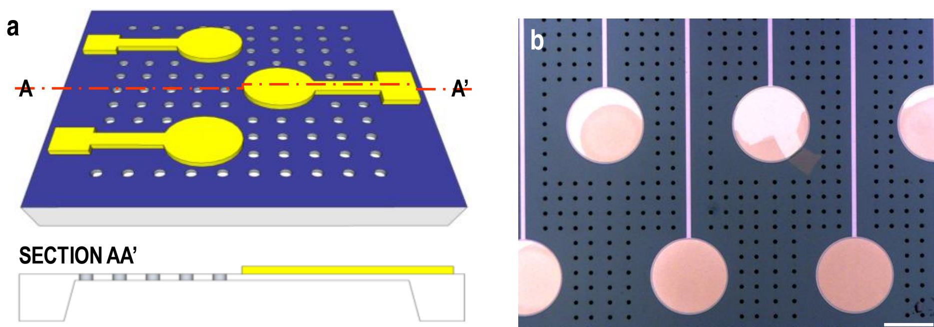


Fig. 5: (a) Schematic of the new design of the perfored MEA device. (b) Optical image of a defective catalyst patterning on the electrodes of the MEA. Scale bar is 200 µm.

At this point, a CNT integration process is also being desing and the first wafers are being fabricated. However, the fabrication of the devices in not yet concluded since problems related to the patterning of the catalyst layers have been encountered. Fig. 5-b shows how the catalyst layer detached from the electrodes during the before the CNT synthesis step.

References

1. Rius, G., I. Martin, P. Godignon, A. Bachtold, J. Bausells, E. Lora-Tamayo, and F. Perez-Murano, Response of carbon nanotube transistors to electron beam exposure, Microelectronic Engineering, 2007. **84**(5-8): p. 1596-1600.
2. Rius, G., A. Verdaguer, F.A. Chaves, I. Martin, P. Godignon, E. Lora-Tamayo, D. Jimenez, and F. Perez-Murano, Characterization at the nanometer scale of local electron beam irradiation of CNT based devices, Microelectronic Engineering, 2008. **85**(5-6): p. 1413-1416.
3. Rius, G., J. Llobet, M.J. Esplandiu, L. Solé, X. Borrisé, and F. Pérez-Murano, Using electron and ion beams on carbon nanotube-based devices. Effects and considerations for nanofabrication, Microelectronic Engineering, 2009. **86**(4-6): p. 892-894.
4. Lan, C., P. Srisungsitthisunti, P.B. Amama, T.S. Fisher, X. Xu, and R.G. Reifenberger, Measurement of metal/carbon nanotube contact resistance by adjusting contact length using laser ablation, Nanotechnology, 2008. **19**(12): p. 125703.
5. Rutherglen, C., D. Jain, and P. Burke, Nanotube electronics for radiofrequency applications, Nature Nanotechnology, 2009. **4**(12): p. 811-819.
6. Ivanov, P., E. Llobet, F. Blanco, A. Vergara, X. Vilanova, I. Gracia, C. Cané, and X. Correig, On the effects of the materials and the noble metal additives to NO_2 detection, Sensors and Actuators B: Chemical, 2006. **118**(1-2): p. 311-317.