8.1.2. POLYSILICON AND NITRIDE PROCESSES

The polysilicon layers that conformed the resistor grids used in active PCR-chips were deposited, whenever possible, using standard CMOS deposition techniques. Even so, since they were key steps in the development of active PCR-chips, they are detailed here together with doping and pre-metallization processes.

Standard polysilicon deposition

The standard polysilicon deposition process consisted in the deposition of 4800 Å of polysilicon by low-pressure chemical-vapor deposition (LPCVD). Deposition was accomplished by exposing the wafers to a 40 standard liter minute (slm) silane gas (SiH_4) flow at 105 mTorr and 630 ºC for 1:07 h, at a rate of about 70 Å/min. The tolerance margin was of 6% and the resulting layer thickness was checked with a Nanospec spectrophotometer (*Nanometrics*).

Standard polysilicon doping

Polysilicon layer doping with phosphorous impurities was carried out in a ASM furnace at atmospheric pressure, by exposing the wafers to an N_2-flow-vaporized $POCL_3$ gaseous mixture. The vaporized $POCL_3$ reacted with the polysilicon surface, creating a composite P_2O_5-SiO_2 layer that was then diffused in an O_2 atmosphere at 950 ºC for 20 min. The process resulted in the formation a 70 nm dual polysilicon-PSG layer (55:45 / diffused:grown). The PSG parasitic oxide layer was then removed by immersing the wafers in a 5% HF solution for 10 min. The polysilicon thus doped presented a nominal 15.8 Ω/□ resistance.

Pre-metallization process

To ensure efficient electrical contacts between previously doped polysilicon layers and the 1 μm-thick aluminum layer deposited afterwards for contact pad formation, a pre-metallization step was carried out to remove any parasitical oxides that might have grown on the polysilicon surface during intermediate processes. Parasitic oxide removal was again conducted by immersion of the wafers in 5% HF solution for 5 min.

Nitride deposition processes

Silicon nitride (Si_3N_4) was used as a base layer for polysilicon deposition, since it is an efficient heat-dissipater that has been described to yield homogenous and defined thermal transfers from thin-film heaters to the underlying silicon wafer ([Ciureanu1992], [Lin2000b]). Typical 1800 Å silicon nitride layers were deposited by LPCVD under a mixed SiH_2Cl_2:NH_3 (30:200 slm) flow at 150 mTorr and 800 °C for 45 min. The tolerance margin was of 8% and the resulting layer thickness was checked with a Nanospec spectrophotometer (*Nanometrics*).

8.1.3. OXIDATION PROCESSES

Thermal oxidation processes

Thermal oxidation processes were important aspects of DNA-chips processing, since they produced the insulating layer that would electrically isolate electrophoresis chips and the PCR-friendly passivation layer for PCR-chips (see p.114). Wet thermal oxidation was conventionally used to grow the thick passivation layers required in electrophoresis chips, whilst dry thermal oxidation was the preferred method for producing highly pure passivation substrates in PCR-chips.

Dry thermal oxidation

To create passivation layers for PCR-chips, 380 or 500 Å oxide layers (tolerance ±40 Å) were grown by dry thermal oxidation in ASM quartz-tube furnaces at 1100 °C. Oxidation was carried out by exposing the wafers to a 6.0 standard liter minute (slm) rate of O_2 for 6 h, then to a chlorine enriched (4%HCl equivalent) O_2:DCE mixture (6.0:0.24 slm) for at least 2 h and ending in a pure O_2 ambient (6.0 slm) for 10 h. Oxidation results were checked on a Nanospec epsilometer (*Nanometrics*).

Oxide Chemical Vapor Deposition (CVD)

Deposited non-doped oxide layers were also routinely used in both electrophoresis and PCR-chip processes, where they served basically as masking and protection layers. Typically, oxides were deposited by showerhead (Pyrox) Atmospheric Pressure Vapor Deposition (APVD) in a reactor at 400 °C under a SiH_4, O_2 gas mixture. Optionally, Plasma-

Enhanced Chemical Vapor Deposition (PECVD) was also used to deposit silicon oxide and silicon nitride layers for wafer protection. PECVD depositions were carried out at 380 ºC.

8.1.4. RESIST DEPOSITION AND FILM-TO-MASK TRANSFER

Standard resist deposition

Standard (single-side) photolithographic processes were carried out with HIPR-6512 negative photo-resist (*Arch Chemicals*) on an automated Karl-Suss aligner. The protocol for resist deposition, insulation, development and baking was the following:

- Wafer des-humectation at 200 ºC for 30 min in stove.
- Spinner deposition and evaporation of HMDS primer for further des-humectation.
- Deposition of HIPR-6512 negative photo-resist at 4000 rpm for 25 s.
- Soft-bake at 100 ºC for 20 min in stove.
- Insulation for 8-10 s under 7 mW 360-400 nm UV light.
- Post-exposure bake (PEB) at 110 ºC for 20 min.
- Development by immersion in HPRD-428 developer solution (*Arch Chemicals*) for 15 min and rinsing with de-ionized water.
- Hard-bake at 115 ºC for 20 min in stove.

Thick-layer positive resists

Thick-layer positive resists were used to avoid membrane breakage in the final stages of integrated active PCR-chips process (see p.240), where pressure differentials during access hole RIE-etch perforation could break the fragile wafer structure. Positive resist was used in this instance to avoid the formation of hard-to-remove resist layers under exposition to ambient light. The maP1275 (*Micro-all-resist*) resist was deposited in a manual spinner with custom vacuum pincers at the wafer margins following the protocol described below:

- Initial spinner deposition and dissemination of maP1275 positive photo-resist at 900 rpm for 20 s (low acceleration ramp).
- Further deposition at 900 rpm for 40 s.
- Soft-bake in a hotplate at 75 ºC for 30 min.

- Hard-bake in exhaust oven at 100 °C for 1 h.

With these parameters, 8 μm-thick resist layers were deposited, effectively protecting the wafer from breakage and clamping damage during the RIE-etch process. The use of below-100 °C baking allowed then an easy removal of the photo-resist layer from the wafer surface with developer and organic solvents, prior to undergoing anodic bonding (see p.294).

Film-to-mask transfer

The transfer of patterned DIN-A5 high-resolution (3200 dpi) films to glass masks was a key feature in the global technological process of the work here described, since it allowed the use of cheap masks for designing big (mm size) motifs and, thus, far more design trials than the use of standard microelectronic masks would have allowed (see p.124). For conducting the transfer process, blank SLW 5090-15C-AR-S1400 masks (*Hoya Corp.*) were bought. These masks are composed of a triple (Cr, anti-reflection Cr_xO_y and negative photo-resist) layer over a 2 mm-thick ultra-pure glass wafer (see Figure 157).

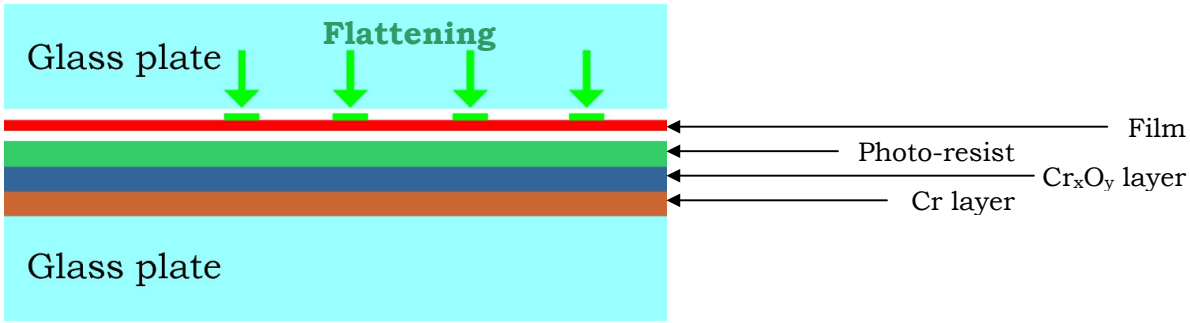

Figure 157 - Film flattening and alignment onto the glass plate prior to insulation for pattern transfer.

To initiate the transfer process, the high-resolution film was cut to plate dimensions (127x127 mm^2), manually aligned onto the plate surface and flattened and hold tight with another chrome-stripped glass plate (see Figure 157). The mask was then insulated through the patterned film for 15 s under 360-400 nm 7 mW UV light to transfer the pattern onto the resist layer and then developed for 25 s in 100% (v/v) HPRD428 (Arch Chemicals) developer solution. The extended insulation and developing times ensured that the poorer transparency of films did not produce *granulose* clear regions. Evidently, due to shade-effects, the over-insulation

had a tradeoff in the minimal resolution limit, but this tradeoff was estimated to be in the whereabouts of 2-3 μm and, thus, it was not considered a critical parameter in the current designs.

Resist-deposition processes were customized and carried out by *Zenon Navarro*, to whom I feel much indebted for his dedication and counsel.

8.1.5. DOUBLE-SIDE ALIGNMENT

Due to the technological reasons already discussed (see p.120), photolithographic alignment and processing of double-side wafers is a key issue in the development of PCR-chips. Double-side alignment was carried out in a Karl-Suss aligner.

Resist spinner deposition and baking

Prior to alignment, the non-exposed side of the wafer was protected by deposition of a mechanical protection HIPR-6512 negative resist (*Arch Chemicals*) with the following spinner protocol: primer deposition and primer evaporation hold, plus resist deposition and spinner pulses: 900 rpm for 2 s and 3000 rpm for 40 s. The protection resist was then soft-backed at 115 ºC for 15 min. After cleansing of the exposed wafer side, HPIR-6512 resist was deposited by spinner (using the above parameters) and soft-baked (100 ºC for 30 min) in a stove.

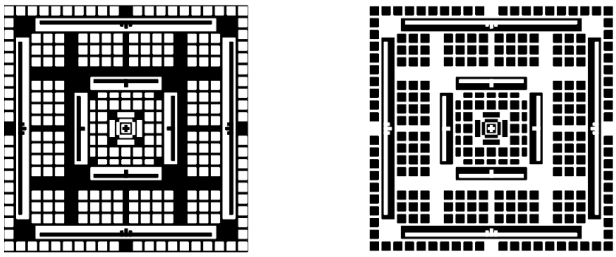

Figure 158 - Dark- and clear-field alignment motifs for double-side alignment following **[Navarro1993]**. Motifs are 6.2 mm^2 and located at 4.57 cm from each other on the wafer surface.

Alignment, insulation, development and hard-bake

Double-side contact alignment was carried out by visual micro-inspection of special double-side alignment patterns ([Navarro1993], see Figure 158). After alignment, the exposed side of wafer was insulated from 6 to 10 s with UV

light and the wafer underwent a post-exposure stove bake (110 ºC for 10 min). Resist patterned motifs were then developed by immersion for 45 s in a HPRD-428 (*Arch Chemicals*) developer solution, and thoroughly rinsed for 15 min under running de-ionized water. In order to withstand the ensuing technological processes and evaporate any remaining traces of developer, the deposited resist was finally hard-baked in a stove (110 ºC for 10 min).

8.1.6. DEEP WET SILICON ETCHING

The deep wet silicon etching procedures utilized in this work correspond to deep silicon TMAH attacks that were conducted at CNM-IMB Microsystems class-10,000 clean-room lab by, or under supervision of, Dr. Marta Duch. The attacks were conducted in a temperature-controlled chemical workbench, wearing hard latex gloves and a facial protector.

Basic TMAH etching procedures

Wafer preparation

Basic TMAH attacks were conducted by simple immersion of the wafers in a hot TMAH solution. The wafers had been typically passivated with a 1 µm-thick wet (or 500 Å-thick dry) thermal-oxide layer (see *Materials and Methods*, p.287), followed by the deposition of a 1800 Å Si_3N_4 layer (see Figure 159). An etching window was opened at these layers by dry etching of the silicon nitride layer following a photolithographic process and using the etched nitride layer as a mask for wet chemical etching of the oxide layer in a HF bath. The resulting composite nitride-oxide mask allowed silicon TMAH attacks up to 500 µm (and over), since TMAH presents strong selectivity towards SiO_2 and Si_3N_4: 64 µm/h - Si, 124 Å/h - termal Si_3N_4 and 17 Å/h - thermal SiO_2 ([Ristic1994], [Merlos1993], [Duch1996]).

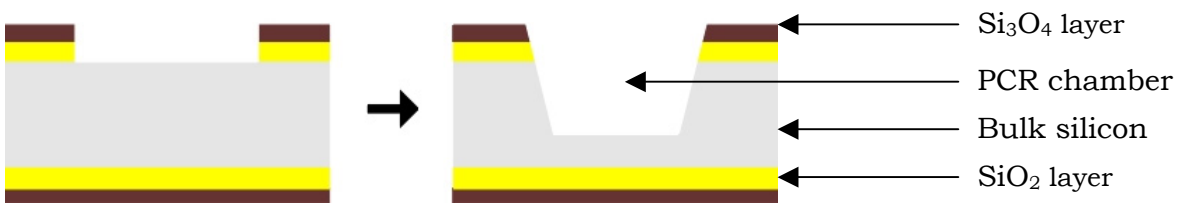

Figure 159 - General outline of the patterned SiO_2 and Si_3N_4 mask layers and the subsequent deep-silicon TMAH attack for etching a PCR chamber.

To conduct a TMAH attack (or to restart an interrupted attack if more than 6 hours had elapsed), wafers were dipped in a 10% HF solution for 10-30 s to remove the layer of parasitic silicon dioxide that invariably forms on a room-temperature air-exposed silicon wafer, a layer that strongly hinders initial TMAH action, leading to much longer etch times. The complete removal of the oxide layer was ascertained by depositing a drop of de-ionized water on top of the wafer surface and noting its hydrophobic behavior.

TMAH attack

Prior to wafer insertion, the 25% (v/v) solution of TMAH in de-ionized water was prepared, poured into the attack chamber and left to heat up to 80 ºC under constant water-flux refrigeration and thermostat control. Afterwards, wafers mounted on a standard multi-wafer methacrilate rack were inserted in the TMAH solution and the attack chamber was closed during the attack.

Etch rates were estimated to be in the whereabouts of 15-25 μm/h for P-type silicon, and the achieved etch depths were evaluated on a fastest-rate case basis in a Nanospec epsilometer (*Nanometrics*). After reaching the desired depth, wafers were extracted from the TMAH solution, thoroughly rinsed with de-ionized water and either dried with an N_2 flow or left to dry (in case of perforation) in a oven at 200 ºC mounted on a glass multi-wafer rack.

Double-side deep silicon etching

Simultaneous double-side etching

To open holes in a chamber like structure, the most time-efficient (and reagent efficient) approach is to expose both sides to attack simultaneously by inserting double-side window-patterned wafers into a TMAH solution until perforation of the wafer was achieved. This method was applied to PCR-chip wafers at the initial stages of this work, following the methodology above described. However, wafers etched by simultaneous double-side etching presented marked frailty due to lateral wafer attack by TMAH (see p.123) and were discarded for PCR-chip processing.

Single-side protected etching

To overcome frailty problems, a process typically used for protecting circuitry under TMAH attacks was used. The method consisted in the mounting of the wafer in a custom-made methacrilate tool (see Figure 160a). The methacrilate tool, with its corresponding toric joints, sandwiched the wafer, exposing only one side to the TMAH solution, while the protected side (see Figure 160b) was internally exposed to a N_2 flow to prevent TMAH intrusion (and etch) after perforation of the wafer. After the attack, the wafer was cleansed as described above, and the methacrilate tool and its joints were also thoroughly rinsed with de-ionized water and left to dry at air temperature to prevent decay. Although this technique prevented multi-wafer etching and doubled attack times for double-side processing, it yielded a secure, reliable and reproducible method for the back opening of holes in micro-machined PCR chambers.

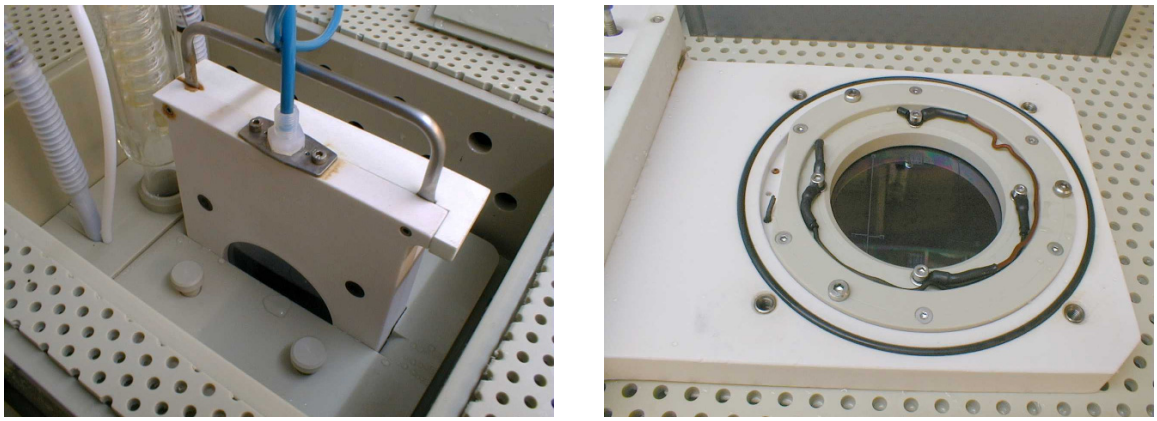

Figure 160 - Single-side TMAH etch. (a) Mounted wafer is introduced in the attack chamber (the blue tube provides N_2 flow) and (b) protected, internally exposed, side of the wafer.

8.2. HOUSING AND PACKAGING

8.2.1. ANODIC BONDING

Anodic bonding (also known as field-assisted glass-metal sealing, [Wallis1969]) is a procedure that permits the bonding of silicon and glass wafers below the softening point of glass. The physical basis for the method relies on the mobility of glass Na^+ ions, which are attracted to the cathode on the opposite glass surface (see Figure 161). After some minutes, this

kinetic process leaves the bonding glass surface with a rough negative charge that pulls both bonding surfaces (silicon and glass) into contact.

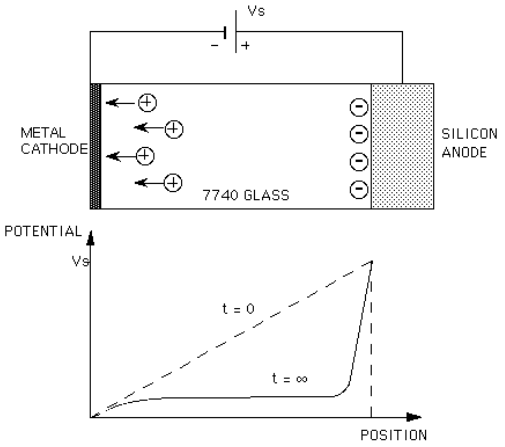

Figure 161 - Kinetic displacement of Na^+ ions under the applied electric field.

The bonding then usually begins at the electrode point of contact by formation of Si-O-Si bonds between the two surfaces [Kanda1990] yielding a strong, irreversible bond that expands across the confronting surfaces. The usual experimental setup of anodic bonding can be seen in Figure 162.

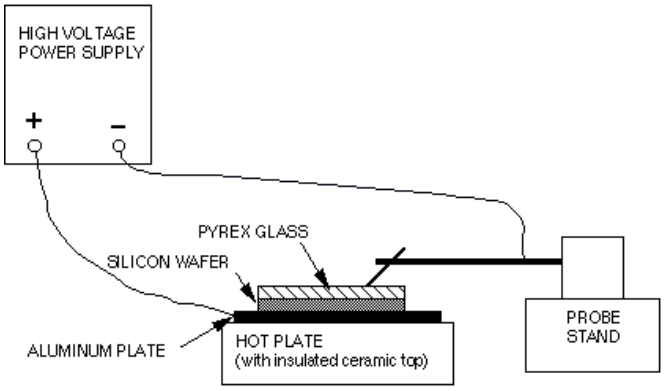

Figure 162 - General setup for the anodic bonding process.

PCR-chips anodic bonding

Conventional anodic bonding requires very smooth (less than 0.1 μm roughness) ultra-pure glass and silicon surfaces. Both P and N type native silicon wafers can be used, while the usual glass wafers are Pyrex 7740 or similar, since they present an adequate thermal expansion coefficient that closely matches that of silicon, thus preventing thermal disruption of the

bond or wafer breakage [Wallis1969]. Typical temperatures range between 200 and 300 ºC, with applied voltages of 100-800 V.

In the case of PCR-chips, a passivation SiO_2 layer was required to overcome inhibition problems (see p.116). Although bonding of surface passivated silicon wafers had been reported in the literature [Kanda1990], it implied the use of higher temperatures and voltages, and a specific variation of the standard anodic bonding setup at CNM-IMB was required to acknowledge the special requisites SiO_2-passivated wafer bonding.

Setup

Anodic bonding was carried out on a FAB150S bonding machine (*Plasmos*) at atmospheric pressure. Ultra-pure #7740 (*Pyrex*) or SD-2 (*Hoya*) glass wafers were used, and both silicon and glass wafers were previously rinsed in a N_2 flux to ward off impurities. The bonding parameters were as follows:

- Heat ramp (40 ºC/min) from room temperature to 400 ºC.
- Temperature stabilization hold (5 min) to avoid thermal disruption.
- Voltage ramp (0-1 kV).
- Voltage/temperature hold (60 min).
- Heat ramp (-40 ºC/min) from 400 ºC to room temperature.

Using this procedure, efficient bonding was reported with bare silicon wafers and passivated silicon wafers with up to 4800 Å silicon oxide layers or a combination of thick oxide and polysilicon layers (see p.117).

Anodic bonding procedures were optimized and carried out by (or under the supervision of) Jose A. Plaza and Mª Cruz Acero.

8.2.2. ULTRASONIC DRILLING

Ultrasonic drilling was assayed as a possible technology for opening access ports in the glass wafers that were to seal the PCR silicon chambers (see p.119). Ultrasonic drilling was assayed in two different manners. Initially, ultrasonic drilling experiments were carried out on glass wafers prior to anodic bonding (see *Materials and Methods*, p.293). Later, drilling was assayed on glass wafers that had already been anodically bonded to silicon micro-machined wafers.

Basics of ultrasonic drilling

Ultrasonic drilling is a wafer perforation technique based on the acoustic transmission of ultrasonic motions (around 20 kHz) from a vibrating drill end to a solution that contains an abrasive agent. The grinding produced by the high-speed motion of the abrasive particles machines a replica of the drill end motif onto the surface substrate.

Methodology

All the ultrasonic drilling experiments here depicted were conducted at the UB Serveis Cientifico-Tècnics[9] with the assistance of their technical staff. Glass wafers were drilled using a 601 ultrasonic drill (*Gatan*), with a drill end that provided 3 mm diameter holes after 3 to 5 minutes drilling.

Non-bonded glass wafer drilling

Drilling of non-bonded glass wafers was carried out without conducting previous alignment procedures, nor drill-stop techniques, apart from a rough estimation (3-5 minutes) of the drilling time. After drilling, the wafers were carried back to CNM-IMB clean-room facilities, where they were methodically rinsed from 1 to 5 minutes with de-ionized water flow. After rinsing, they were dried with N_2 flow and immersed in a 10%HF solution for 10 minutes, in order to minimize the surface in-homogeneities introduced by the drilling technique near hole edges [Diepold1996]. Wafers were subsequently rinsed thoroughly with de-ionized water and dried again under N_2 flow. After drying, silicon anodic bonding assays were carried out with the drilled glass wafers, but none of the yielded consistent bonds (see p.119).

Bonded glass wafer drilling

To overcome this problem, glass wafer drilling was assayed on already anodically bonded glass wafers. To do this, an initial estimation of the drilling time for this wafer was carried out in a non-critical area of the wafer in order to determine drill-stop procedures to prevent silicon-wafer perforation. Afterwards, the drill end was manually positioned on top of a PCR (or electrophoresis) reservoir and drilling was executed. Although some

[9] Universitat de Barcelona (UB), Barcelona, Spain.

of the attempts at drilling glass wafers in this way were quite successful, there were serious impediments for yielding reproducible results:

- Even if independently calculated for each wafer, drill-stop estimates were, at their best, rough, since abrasive concentration and distribution (which varies at each drill location) play an important role in determining the drilling rate. Thus, on many occasions, the underlying silicon wafer reservoir was inadvertently perforated, yielding unusable devices (see Figure 51, p.120).

- Even when drill-stops were conducted successfully, abrasive and glass debris irreversibly filled and got stuck at PCR chambers and electrophoresis channels, thus also rendering the devices unusable (see also Figure 51, p.120).

8.2.3. MECHANICAL DEVICES

As already stated, the development of mechanical devices for pressure driven chip cleansing and insertion and extraction of solvents was one of the key issues in the development of PCR-chip systems, since it circumvented many of the numerous problems that μ-TAS systems commonly face in their interface with the macroscopic world. Large-pressure washing (see p.317) with different reagents in electrophoresis and PCR-chips was achieved by coupling chip access ports to Ø4 mm tubing and to syringe, vacuum or peristaltic pumps through mechanical devices (see p.128), and micro-liter reagent dispensing and removal was accomplished with specially developed pipette-envelope-shape mechanical outfits (see p.145).

Materials

Mechanical devices were manufactured either from methacrilate or Teflon 10 mm-thick slabs (*Electrocome*), which were then cut and leveled to the desired thickness for each device. Allen Ø4 mm steel screws were used for clamping of the device and 1.02 mm-thick $Ø_i$1.27 mm NBR toric joints (*Epidor*) were used to provide airtight connections.

Methodology

The common process for the production of both methacrilate and Teflon based devices starts with the abrading and outline of the device upper and lower slabs. This process was simultaneously done in a 5 μm precision XYZ Powermill (*Kondia*). After abrading and cutting the slab to the appropriate dimensions (typically 90x50 mm^2 and 10 mm [upper slab] and 5 mm [lower slab] thickness), the standard chip outline (40x10 mm^2) was then engraved 0.5 mm deep by grinding with the mill machine onto the base slab surface, in order to ease chip repositioning at each use. Thereafter, Allen screw Ø4 mm matching holes were produced at the desired locations of both slabs with either a A-35 (*Ibarma*) or a 601 Ara-Mon (*Sades*) adjustable-tilt driller and a screw-negative Ø4 mm drill bit. The same drills were then used to open Ø4 mm alignment holes on both slabs and access holes on the upper slabs. The latter could either be screw-negative Ø3 mm holes for the insertion of Ø4 mm tube interfaces or conical-shape holes for pipette insertion; in both cases, the lower opening had a Ø3.31 mm, 1 mm-deep indent drilled for toric joint placement. Conical-shape holes were created with a custom-ground drill bit, following the conicity angle (0.261º) reported by the pipette tip manufacturer (*ART*). Finally, directional motifs for upper and lower slab positioning were rubbed with a L1/225 lathe (*Pinacho*) and Ø4 mm steel alignment sticks were cut with an automated saw (*Uniz*), polished with a T650 rectifier (*Kair*) and hammered into their respective holes.

Designs

Many methacrilate device designs were assayed for different chips and conditions, but, among them, only three were finally used in PCR-chip applications.

Methacrilate washing device

A device able to deliver high pressures to chips through airtight connections was a prerequisite for electrophoresis chips (in order to insert and remove viscous gel substances from thin capillaries) and a very welcome tool for chip reuse in PCR systems (see p.128). Although there exist some alternatives (like direct chip-tube gluing), after some studies (see p. 127) methacrilate devices were deemed the best option to implement high-pressure air/liquid delivery. Methacrilate devices offered very tight

connections via clamped toric joints and they were easily reusable and could be cleansed independently of the chips. Even though many washing methacrilate devices were developed, the main washing methacrilate design used in the work here described was the PCR-chip washing device shown in Figure 163.

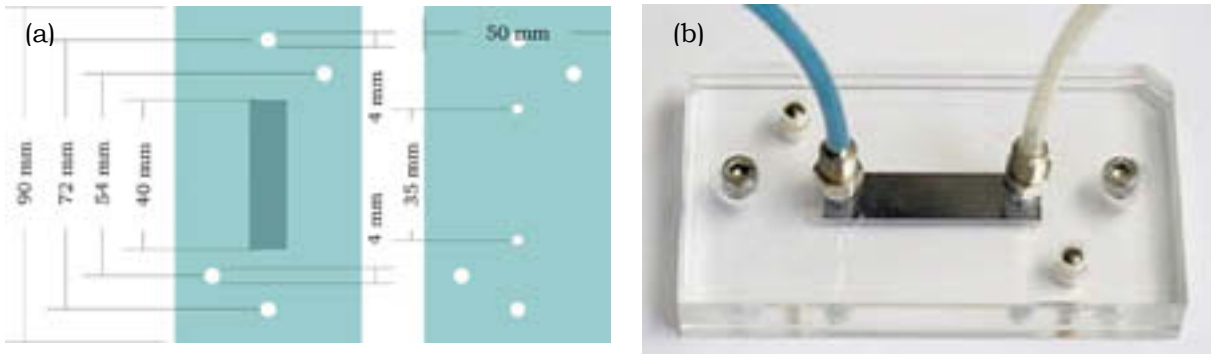

Figure 163 - Lower and upper slab designs (a) and assembled injection system (b) for standard washing methacrilate device.

Methacrilate insertion/extraction device

Insertion and extraction of reagents could be carried out with the above-described devices, but at the cost of using large amounts of reagent and risking tube-wall sticking during extraction. Therefore, special customized methacrilate devices were manufactured with ad-hoc conical holes that matched the shape of standard pipette tips. In this way, small positive and negative pressures could be applied using a micropipette and the desired reagent quantities.

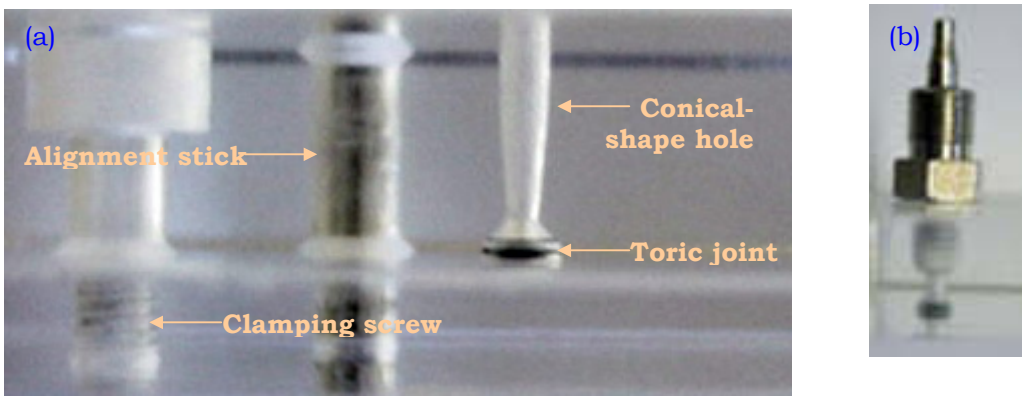

Figure 164 - Pipette-shape access aperture and clamping and alignment holes for reagent deliver devices (a) and Ø4 mm tube connection access holes for washing devices (b).

With the finished devices, highly successful and reproducible insertion and extraction of reagents were demonstrated for both serpentine-like and rhomboidal shape PCR-chips (see p.145). Conicity values for 20-P pipette tips were gently provided by the pipette tip manufacturer (*ART*) and a standard Ø2.5 mm drill tip was manually ground to replicate the 0.261° conicity angle. After drilling the pipette envelope holes on the upper 10 mm-thick slab, the upper cross-sectional area presented a 2 mm diameter, while the lower reported a 1 mm diameter. The outline of the pipette-shape access hole is shown in Figure 164.

Teflon active PCR-chip holder

The simultaneous allocation of electrical contacts and effective sealing mechanisms in active PCR-chips posed a considerable problem, since both kind of elements had to access the same chip face at very close positions. Moreover, both elements (and specially sealing mechanisms) required some form of clamping to ensure effective operation. To fulfill these requirements, an existing heat-resistant Teflon chip-holder device that had previously been developed for chip operation with small (30 mm^2) Peltier cells (see p.182) was retrofitted to accommodate electrical-access holes and pedestal clamps for custom developed copper electric-contact bars. A wide opening was also drilled at one of the device ends to allow Pt100 sensor introduction for monitoring purposes. The overall design of the device can bee seen in Figure 165.

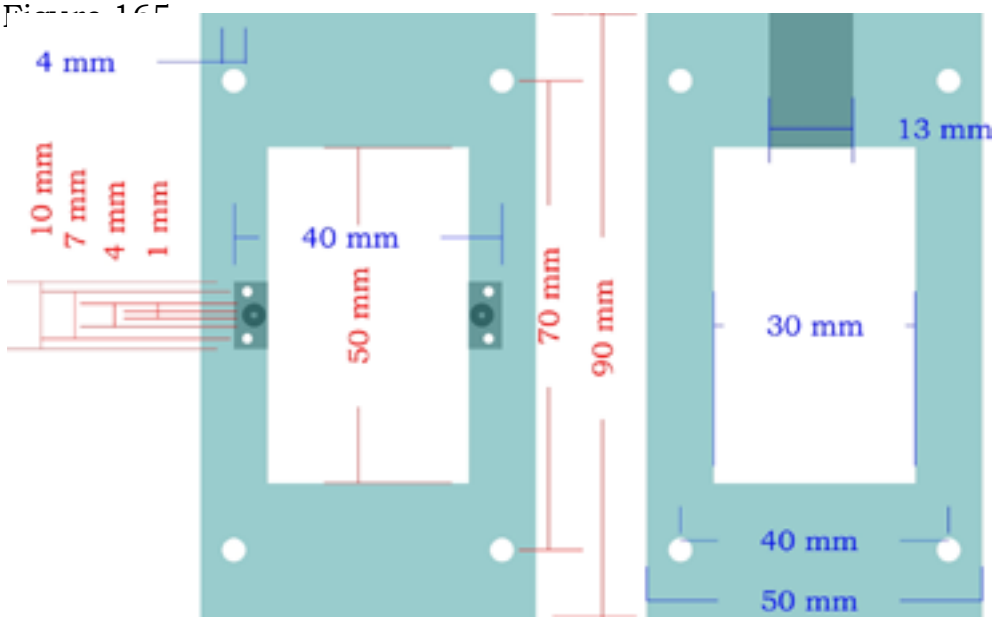

Figure 165 - Schematic design of the retrofitted active PCR-chip holders: inferior (left) and upper (right) Teflon slabs. Dark green represents ground surfaces.