PART IV - MATERIALS AND METHODS

8. TECHNOLOGICAL MATERIALS AND METHODS

8.1. SILICON TECHNOLOGY

8.1.1. COMPLETE TECHNOLOGICAL PROCESSES

The following is a comprehensive report of the technological processes and mask sets involved in the fabrication of both passive and active PCR-chips.

Passive PCR-chips complete technological process

The basic technological process for passive PCR-chips can be approximately divided into four separate sub-processes. Firstly (steps 1-3 in Figure 153), the wafer is prepared for the ensuing deep silicon etches by means of silicon oxide and nitride passivation steps. Secondly (steps 4-8), double-side photolithographic processes define the regions where the silicon etch is to take place (reservoir and access holes), and these motifs are transferred to the underlying passivation layers through wet chemical etching. Finally (steps 9-12), silicon is micro-machined by deep TMAH etching in a two-step procedure, and the completed wafer is passivated again with dry silicon oxide for PCR-compatibility.

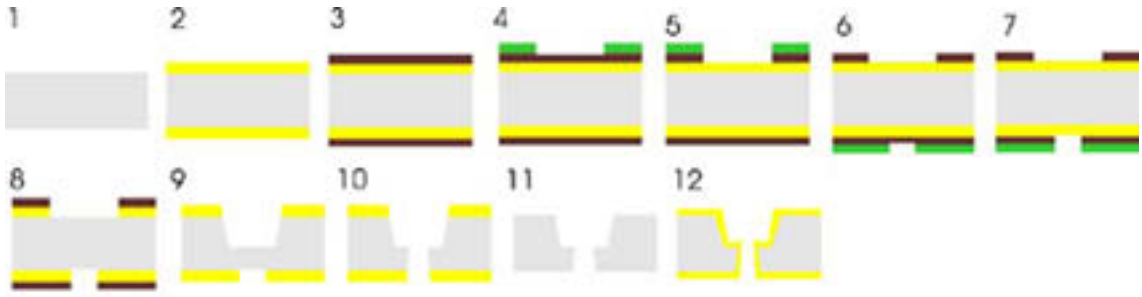

Figure 153 - Complete technological process for the production of passive PCR-chips.

The detailed process file is as follows:

1) BEGIN - Process start
   a) MARC-PXA - selection and backside nicking of p-type 4-400 Ω 300 μm-thick double-side polished wafers
   b) NETG-SIM - Standard wafer cleansing

2) OHC-XXX - Non-standard dry thermal oxidation. Layer thickness: 2 μm.
   a) NETG-SIM - Cautionary wafer cleansing prior to the following nitride deposition

3) DNITAAA - Standard 1800 Å silicon nitride deposition (both sides)

4) FOTO-FCD - Standard two-sided wafer photolithographic process on the front side. Mask: HOYAPCRXC0.

5) NIT-QUAD - Standard silicon nitride RIE-etch in QUAD machine (*Drytek*). Front side. Etch-depth: 1800 Å. Underlying substrates: dry thermal oxide (2 μm).
   a) DEC-RESI - Photo-resist stripping.

6) FOTO-FKD. Standard two-sided wafer photolithographic process on the back side. Mask: HOTAPCRXD0.

7) NIT-QUAD - Standard silicon nitride RIE-etch in QUAD. Back side. Etch-depth: 1800 Å. Underlying substrates: dry thermal oxide (2 μm).
   a) DEC-RESI - Photo-resist stripping.

8) QGOXNXXX - Non-standard oxide wet etch with nitride mask. Etch-thickness: 2 μm. Both sides.
   a) QDNITXXX - Variable thickness wet nitride stripping. Etch thickness: 1800 Å. Underlying substrates: dry thermal oxide (2 μm) / p-type silicon.

9) GHUM-ESP - Deep silicon TMAH etch on the front side. Etch thickness: 175 μm. Back side protected with PVC ring. Mask layers: silicon nitride (1800 Å) onto thermal silicon oxide (1 μm).

10) GHUM-ESP - Deep silicon TMAH etch on the back side. Etch thickness: ~125 μm (until wafer perforation). Front side protected with PVC ring. Mask layers: silicon nitride (1800 Å) onto thermal silicon oxide (1 μm).

11) GHUM-ESP - Equivalent to QDOXTXXX. Variable thickness wet oxide stripping to remove the residual oxide. Etch thickness: 2 μm. Underlying substrates: p-type silicon. Micro-machined wafers: careful handling.
   a) GHUM-ESP - Equivalent to NETG-SIM. Cautionary wafer cleansing prior to the ensuing dry thermal oxidation. Micro-machined wafers: careful handling.

12) OXINAAA - Standard initial CMOS thermal dry oxidation. Layer thickness: 380 Å. Both sides.

13) ESPECIAL - Anodic bonding process at 400 ºC/1 kV with 0.5 mm-thick glass wafers.

14) END - Formal process ending.

Mask set

The complete mask set for rhomboidal passive PCR-chips includes two different dark-field masks (front-side reservoirs and back-side holes) with double-side alignment motifs, as shown in Figure 154:

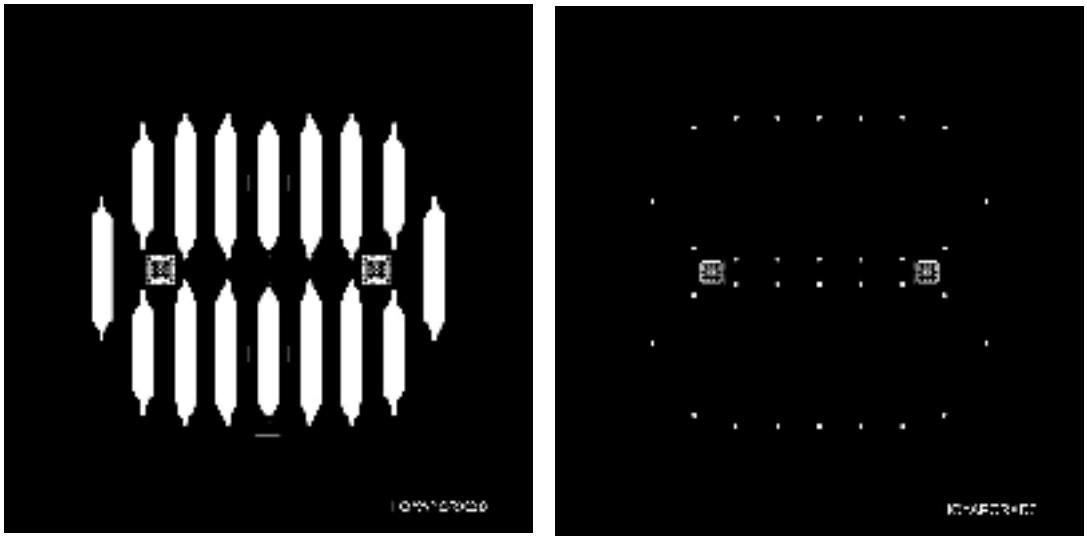

Figure 154 - Complete mask set for rhomboidal passive PCR-chips.

Active PCR-chips complete technological process

As expected, the complete technological process for active PCR-chips (and its respective mask set) is far more complex than that of passive PCR-chips. Also, as in the previous case, the process can be seen to divide into five separate stages. In stage one (steps 1-2 in Figure 155), the wafer is readied for process with the deposition of the main different layers to be used later. Afterwards (steps 3-5), an initial process at the back side defines and passivates the polysilicon resistors. Thereafter (steps 6-10), the process switches back to the front side, where it delineates, etches and passivates the PCR reservoirs. At stage four (steps 11-18), the process swings again to the back side, creating electrical-contact openings and depositing and patterning aluminum contact pads. Finally (steps 19-20), a final deep silicon RIE-etch opens the access holes and the completed wafer gets bonded to a glass counterpart.

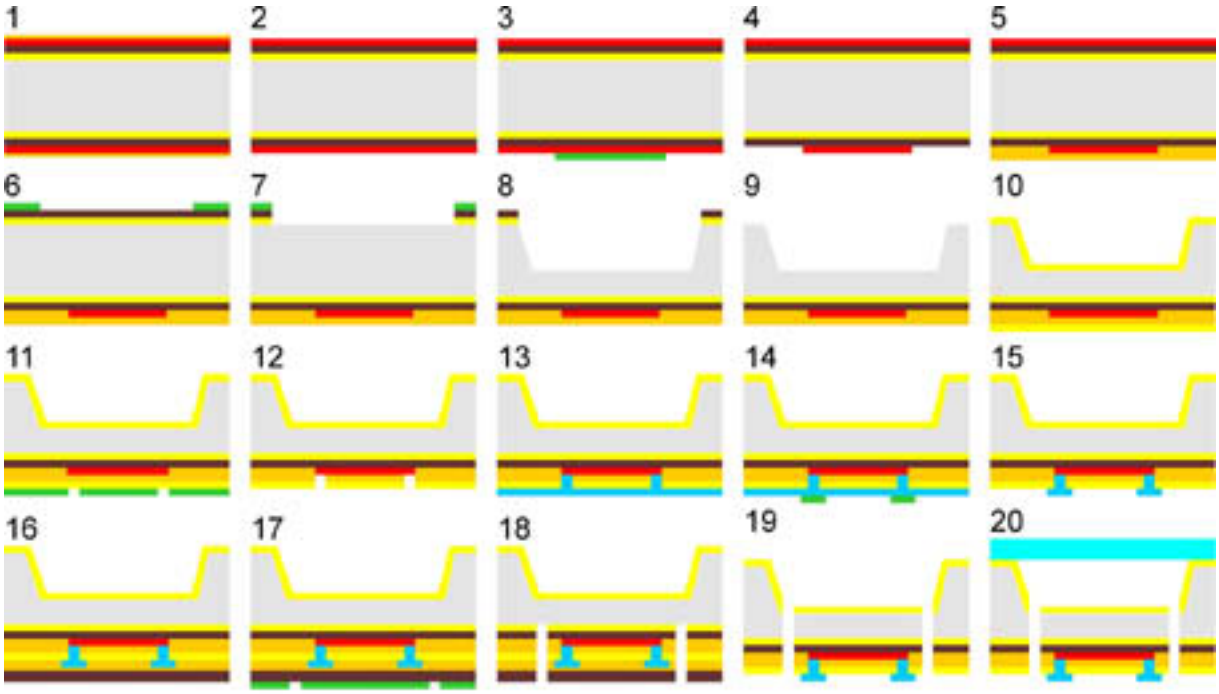

Figure 155 - Complete technological process for active PCR-chips.

The detailed process file for the active PCR-chips process is sketched below:

1) BEGIN - Process start
   a) MARC-PXA - selection and backside nicking of p-type 4-400 Ω 300 μm-thick double-side polished wafers
   b) NETG-GEN - Standard complete wafer cleansing
   c) OSC-500 - Non-standard dry thermal oxidation to mitigate nitride-silicon mechanical stresses. Layer thickness: 500 Å. Both sides.
   d) NETG-SIM - Cautionary wafer cleansing prior to the following nitride deposition
   e) DNITAAA - Standard 1800 Å silicon nitride deposition. Both sides.
   f) MES-NANO - Nanospec (*Nanometrics*) measure of the deposited nitride layer. Back side.
   g) NETG-SIM - Standard simple wafer cleansing prior to polysilicon deposition.
   h) DPOLAAA - Standard 4800 Å polysilicon deposition. Both sides.
   i) OPOC4800 - Standard polysilicon doping with phosphor impurities (O_2+$POCL_3$). Both sides.

2) QDPSGC25 - Standard wet stripping of the parasitic oxide layer (PSG).

3) FOTO-ESP - Equivalent to FOTO-FCD. Standard two-sided wafer photolithographic process on the front side. Repeated insulation to remove mask imperfections. First development: on track. Second development: manual. Polysilicon resistor grid definition. Back side. Mask: HINT-PCRPOL.

4) PQ1P1C25 - Standard polysilicon RIE-etch in QUAD. Etch depth: 4800 Å. Back side.
   a) DEC-RESI - Photo-resist stripping.
   b) MES-NANO - Silicon nitride layer thickness verification. Back side.
   c) NETG-SIM - Simple wafer cleansing prior to oxide deposition.

5) DPYRXXX - Variable-thickness Pyrox oxide deposition to passivate polysilicon resistors. Back side. Layer thickness: 5500 Å.
   a) PQ1P1C25 - Standard polysilicon stripping to define front-side nitride reservoir windows. Front side.

6) FOTO-ESP - Equivalent to FOTO-FKD. Standard two-sided wafer photolithographic process on the back side. Repeated insulation to remove mask imperfections. Definition of PCR reservoirs. Front side. Mask: HINT-PCRPISC.

7) NIT-QUAD - Standard silicon nitride RIE-etch in QUAD. Front side. Etch-depth: 1800 Å. Underlying substrates: dry thermal oxide (500 Å).
   a) QUAD-ESP - Equivalent to OXI-QUAD. Standard silicon oxide RIE-etch in QUAD. Front side. Etch depth: 500 Å. Underlying substrates: p-type silicon.
   b) DEC-RESI - Photo-resist stripping.

8) GHUM-ESP - Deep silicon TMAH etch on the front side. Etch thickness: 175 μm. Back side protected with PVC ring. Mask layers: silicon nitride (1800 Å) onto thermal silicon oxide (500 Å).

9) NIT-QUAD - Standard silicon nitride RIE-etch in QUAD. Residual nitride stripping. Front side. Etch-depth: 1800 Å. Underlying substrates: dry thermal oxide (500 Å).
   a) QUAD-ESP - Equivalent to OXI-QUAD. Standard silicon oxide RIE-etch in QUAD. Residual oxide stripping. Front side. Etch depth: 500 Å. Underlying substrates: p-type silicon.
   b) GHUM-ESP - Equivalent to NETG-SIM. Simple wafer cleansing prior to oxidation. Micro-machined wafers: careful handling.

10) OSC-500 - Non-standard dry thermal oxidation. Final PCR-friendly oxide layer on front side. Layer thickness: 500 Å. Both sides.

11) FOTO-ESP - Equivalent to FOTO-FCD. Standard two-sided wafer photolithographic process on the back side. Repeated insulation to remove mask imperfections. First development: on track. Second development: manual. Definition of electrical access holes. Back side. Mask: HINT-PCRVIA.

12) QUAD-ESP - Equivalent to OXI-QUAD. Standard silicon oxide RIE-etch in QUAD. Back side. Etch depth: ~5500 Å. Underlying substrates: polysilicon (4800 Å).
    a) DEC-RESI - Photo-resist stripping.
    b) QPRMEC25 - Standard parasitic oxide layer removal prior to metallization.

13) MZ550ING - Standard aluminum (AlSiCu) deposition to contact polysilicon. Layer thickness: 1 μm. Back side.

14) FOTO-ESP - Equivalent to FOTO-SAR. Two-sided wafer photolithographic process on the back side. Non-refracting photo-resist to avoid notching. Repeated insulation to remove mask imperfections. First development: on track. Second development: manual. Definition of electrical pads. Back side. Mask: HINT-PCRPAD.

15) QGACSXXX - Variable thickness aluminum wet chemical etch. Etch thickness: 1 μm. Back side.
    a) DEC-RESI - Photo-resist stripping.
    b) GHUM-ESP - Equivalent to NETG-SIM. Simple wafer cleansing prior to passivation. Micro-machined wafers: careful handling.

16) DOXNTAAA - Standard CMOS passivation: silicon oxide (4000 Å) + silicon nitride (11000 Å), to be used as the masking window for deep silicon etch.

17) FOTO-ESP - Equivalent to FOTO-SAR. Two-sided wafer photolithographic process on the back side. 2 μm-thick non-refracting photo-resist to avoid notching. Repeated insulation to remove mask imperfections. First development: on track. Second development: manual. Extended hardbake at 200 °C. Definition of reagent access holes. Back side. Mask: HINT-PCRAGJ.

18) OXNT-RIE - Standard passivation RIE etch. Etch depths: 7000+11000 Å. Back side.
    a) GIR-ESP - Silicon oxide RIE etch in GIR. Nominal etch depth: 5500 Å. Expected etch depth: 5000 Å. Underlying substrates: silicon nitride (1800 Å). Back side.
    b) GIR-ESP - Silicon nitride RIE etch in GIR. Etch depth: ~1800 Å; refer to step 4b. Back side.
    c) GIR-ESP - Silicon oxide RIE etch in GIR. Etch depth: 500 Å. Expected depth etch: 5000 Å. Underlying substrates: silicon nitride (1800 Å). Back side.
    d) DEC-RESI - Photo-resist stripping.

19) FOTO-ESP - 8 μm positive photoresist deposition and extended 200 ºC hardbake to withstand pressure drop during wafer perforation. Front side.
   a) A601-D - Deep silicon (+silicon oxide) etch in 601 RIE machine (*Alcatel*). Back side. Etch depth: 125 μm (silicon) + 500 Å (oxide).

20) ESPECIAL - Anodic bonding process at 400 ºC/1 kV with 0.5 mm-thick glass wafers.

21) END - Formal process ending.

Mask set

The complete mask set for active PCR-chips contained four dark-field masks (reservoirs, electrical and reagent holes) and two clear-field masks (polysilicon resistors and aluminum pads/tracks), as it can be seen here below:

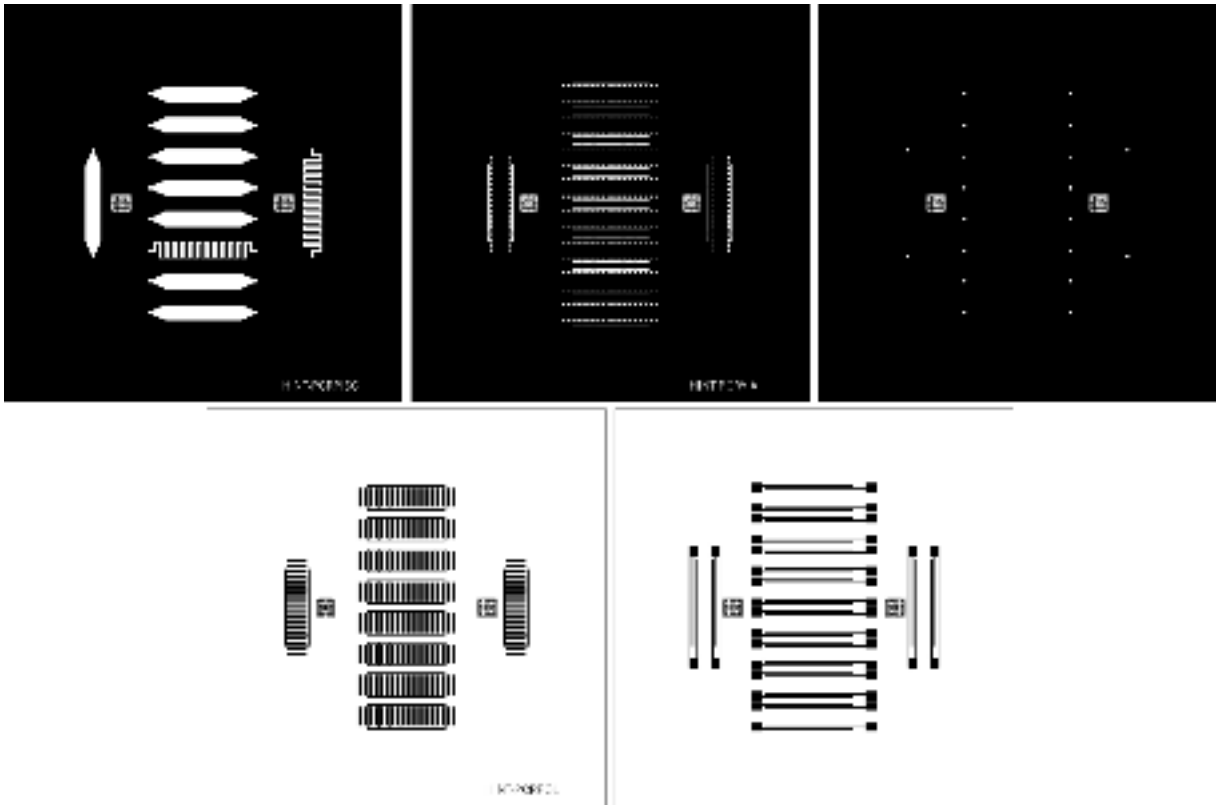

Figure 156 - Complete mask-set for the active PCR-chip process.