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Inkjet Printed Microelectronic Devices and Circuits

Ph.D. Thesis Dissertation
(Microelectronics and Electronics System Department)

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I certify that I have read this dissertation and that, in my opinion, it is fully adequate in scope and quality as a dissertation for the degree of Doctor of Philosophy.

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ABSTRACT

In the last years there has been a growing interest in the realization of low-cost, flexible and large area electronic systems such as item-level RFID tags, flexible displays or smart labels, among others. Printed Electronics has emerged as one of the most promising alternative manufacturing technologies due to its lithography- and vacuum-free processing. Related to this, organic and inorganic solution processed materials advanced rapidly improving the performance of printed devices. However, the fabrication of organic transistors, key element to build circuits for acquisition and processing, suffers from the poor resolution and layer-to-layer registration of current printing techniques such as inkjet and gravure printing. To compensate that, transistors implemented in those technologies have large channel lengths and large gate to source/drain overlaps. These large dimensions limit the performance of the printed transistors, despite the improvements in materials.

This thesis focuses on circumventing the printing resolution challenges using compensation techniques and new layout geometries while keeping an all-inkjet purely printing process. The dissertation deals with the development of microelectronic passive and active devices implemented using low-cost inkjet printing machinery. I focussed my effort in the design, manufacturing & characterization (electrical and morphological) points of view in order to allow the fabrication of organic integrated circuits.

Several thousands of resistors, capacitors and transistors were fabricated, all of them fully inkjet-printed. All devices were morphologically and electrically characterized. A high number of experiments were developed to ensure efficient manufacturing and report on parameter variation, thus obtaining statistically significant data. Process variations present in transistor fabrication lead to a certain variability on the resulting transistor parameters that need to be taken in account. Scalability, variability and yield were analysed by using different strategies.

Fabricated inverters show a clear inversion behaviour demonstrating the state of the inkjet fabrication process to integrate printed devices in circuits. This is a first step in the way to fabricate all-inkjet complex circuits.

The amount of samples manufactured by the fully inkjet printing approach can be considered an outstanding achievement and contributes to a better knowledge of the behaviour and failure origins of organic and printed devices.

RESUM

En els darrers anys ha anat creixent l'interès per la fabricació de sistemes de baix cost, flexibles i sobre gran àrea com, per exemple, les etiquetes RFID per a identificació de productes, les pantalles flexibles o les etiquetes intel·ligents entre d'altres. La tecnologia d'impressió electrònica (Printed Electronics) s'ha posicionat com una de les tecnologies alternatives de fabricació més prometedores pel fet de no utilitzar tècniques fotolitogràfiques i de buit. Alhora, la millora en materials orgànics i inorgànics ha provocat un increment en les prestacions dels dispositius impresos. Tot i això, la fabricació de transistors orgànics, element clau per a construir circuits electrònics d'adquisició o processament, es veu afectada per la poca resolució i registre entre capes de les tecnologies d'impressió actuals com inkjet o gravat. Per compensar-ho, els transistors implementats utilitzant aquestes tecnologies tenen llargades de canal molt grans i grans solapaments entre porta i font/drenador. Aquestes grans dimensions limiten les prestacions dels transistors impresos, tot i les millores obtingudes en els materials.

Aquesta tesi està enfocada en contrarestar els problemes provocats per la poca resolució en impressió utilitzant tècniques de compensació i noves geometries de dispositius mantenint el procés completament inkjet. Aquest treball s'enfoca en el desenvolupament de dispositius microelectrònics passius i actius implementats amb maquinària inkjet de baix cost. He enfocat el meu esforç en el disseny, la fabricació i la caracterització (elèctrica i morfològica) amb l'objectiu de fer possible la fabricació de circuits integrats orgànics.

En el marc de la tesi, s'han fabricat varis milers de transistors, capacitats i resistències exclusivament amb tecnologia inkjet. Tots els dispositius s'han caracteritzat tant elèctrica com morfològicament. S'ha dut a terme un gran número d'experiments per assegurar una fabricació eficient, estudiar la variabilitat dels paràmetres i obtenir dades estadísticament significatives. La variació en els processos de fabricació de transistors porta a una important variabilitat en els paràmetres dels dispositius impresos fins ara poc estudiada. Escalabilitat, variabilitat i rendiment s'han analitzat utilitzant diferents estratègies.

S'han obtingut circuits digitals amb un comportament adient, demostrant l'estat actual de la tecnologia inkjet per a integrar dispositius impresos en circuits. Aquest és un primer pas en el camí per fabricar circuits més complexes amb tecnologia d'impressió inkjet.

La quantitat de mostres fabricades amb tecnologia inkjet es pot considerar com un assoliment important i contribueix a millorar el coneixement del comportament i els orígens de fallades dels dispositius orgànics i impresos.

Nothing in Nature is random...

A thing appears random only through the incompleteness of our knowledge.

Spinoza (1632 - 1677)

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CONTENTS

LIST OF ACRONYMS

AC	Alternating Current
AFM	Atomic Force Microscope
AMEPD	Active Matrix Electrophoretic Display
AMOLED	Active Matrix Organic Light-Emitting Diode
AMTFT	Active Matrix Thin Film Transistor
a-Si	Amorphous Silicon
BG-BC	Bottom Gate – Bottom Contact
BG-TC	Bottom Gate - Top Contact
BioFET	Bio-Field Effect Transistor
B&W	Black&White (monochrome)
CAD	Computer Aided Design
CLK	Clock
CMOS	Complementary Metal-Oxide-Semiconductor
CPD	Counter Printing Direction
CSL	Current-Source Load
C-PVP	Crosslinked Poly(4-vinylphenol)
C–V	capacitance–voltage
D	Drain electrode
DC	Direct Current
DL	Diode Load
DMP	Dimatix Material Printer
DOD	Drop-On-Demand
DS	Drop Spacing
EL	Electro Luminescent
EPD	Electrophoretic Display
EU	European Union
FET	Field-Effect Transistor
FIB	Focus Ion Beam
FlexNet	Network of Excellence for the Exploitation of Flexible, Organic and Large Area Electronics
FOLAE	Flexible, Organic and Large Area Electronics
G	Gate electrode
HF	High Frequency
HOMO	Highest Occupied Molecular Orbital
IC	Integrated Circuit
ITO	Indium Tin Oxide
KGO	Known Good OTFT
LCD	Liquid Crystal Display
LUMO	Lowest Unoccupied Molecular Orbital
MEMS	Micro-Electromechanical Systems
MIM	Metal-Insulator-Metal

MIS	Metal-Insulator-Semiconductor
MISFET	Metal-Insulator-Semiconductor Field-Effect Transistor
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor
MTR	Multiple Trapping and Release
nMOS	n-type Metal Oxide Semiconductor
NP	Nano Particles
OE	Organic Electronics
OE-A	Organic Electronics Association
OFET	Organic Field Effect Transistor
OLED	Organic Light-Emitting Diode
OPC	Optical Proximity effect Correction
OPV	Organic Photovoltaics
OSC	Organic Semiconductor
OTFT	Organic Thin Film Transistor
PCB	Printed Circuit Board
PD	Printing Direction
PEDOT:PSS	Poly(3,4-ethylenedioxythiophene) poly(styrenesulfonate)
PEN	Polyethylene Naphthalate
PET	Polyethylene Terephthalate
PFTP	Pentafluorothiophenol
PMMA	polymethyl-methacrylate
pMOS	p-type Metal Oxide Semiconductor
PSC	Pattern Shape Correction
PTFE	Polytetrafluoroethylene
PVA	Polyvinylalcohol
PVP	Poly(4-vinylphenol)
PZT	Piezoelectric Transducer
P3HT	Poly (3-hexyl thiophene)
RC	Resistance-Capacitance
RES	Rapid Electrical Sintering
RET	Resolution Enhancement Techniques
RF	Radio Frequency
RFID	Radio Frequency Identification
RL	Resistor Load
R2R	Roll-to-Roll
S	Source electrode
SAM	Self-Assembled Monolayer
SEM	Scanning Electron Microscope
SiO_2	Silicon Dioxide
S2S	Sheet-to-Sheet
TDK4PE	Technology & Design Kit for Printed Electronics
TFT	Thin-Film Transistor
TG-BC	Top Gate - Bottom Contact

TG-TC	Top Gate - Top Contact
TIPS	6,13-Bis(triisopropylsilylethynyl)
UPC	Universal Product Code
VOFET	Vertical Organic Field-Effect Transistor
VRH	Variable Range Hopping
VTC	Voltage Transfer Curve
WID	Within- or Intra-die
WORM	Write-Once-Read-Many

LIST OF SYMBOLS

Symbol	Description	Units
C	Capacitance	F
C_i	Capacitance per unit area of the insulator	F/cm^2
$C_{insulator}$	Insulator Capacitor	F
C_p	Parallel Capacitance	F
CTE	Coefficient of Thermal Expansion	K^{-1}
d	Thickness	m
E_G	Band-gap Energy	eV
GND	Ground	V
I_{DS}	Drain-Source Current	A
I_G	Gate Current	A
I_{leak}	Leakage Current	A
I_{OFF}	Off-current (drain)	A
I_{ON}	On-current (drain)	A
I_{ON}/I_{OFF}	On/Off Drain Current ratio	-
IP_s	Semiconductor Ionization Potential	eV
L	Channel Length	µm
R	Resistance	ohm
R	Bending radius	mm
R_B	Bit resistance	ohm
R_c	Contact Resistance (Resistors)	ohm/µm^2
R_c	Contact Resistance (OTFTs)	ohm/cm
R_p	Parallel Resistance	ohm
RVC	Resistor Voltage Coefficient	ppm/V
$R_□$	Sheet Resistance	ohm/□
S	Spreading (ink fluid)	-
S	Strain (bending)	%
S	Subthreshold Slope (OTFTs)	V/dec
T	Relaxation Time	sec
T_f	Falling Time	sec

$\mathbf{T_r}$	Rise Time	sec
$\mathbf{T_{pHL}}$	Falling Propagation Delay	sec
$\mathbf{T_{pLH}}$	Rising Propagation Delay	sec
$\mathbf{V_{DD}}$	Supply Voltage	V
$\mathbf{V_{DS}}$	Drain-Source Voltage	V
$\mathbf{V_G}$	Gate Voltage	V
$\mathbf{V_{GS}}$	Gate-Source Voltage	V
$\mathbf{V_{IH}}$	Input High Voltage	V
$\mathbf{V_{IL}}$	Input Low Voltage	V
$\mathbf{V_{in}}$	Input Voltage	V
$\mathbf{V_{OH}}$	Output High Voltage	V
$\mathbf{V_{OL}}$	Output Low Voltage	V
$\mathbf{V_{out}}$	Output Voltage	V
VNMH	High-state Noise Margin Voltage	V
VNML	Low-state Noise Margin Voltage	V
$\mathbf{V_{SS}}$	Source Supply Voltage	V
$\mathbf{V_T}$	Threshold Voltage	V
W	Channel Width	μm
$\mathbf{\Delta V_T}$	Threshold Voltage shift	V
$\mathbf{\varepsilon_r}$	Relative Permittivity of the material	F/m
$\mathbf{\varepsilon_o}$	Vacuum Permittivity ($8.85 \cdot 10^{-12}$ F/m)	F/m
$\mathbf{\gamma}$	Gamma Parameter	-
$\mathbf{\gamma_{SO}}$	Substrate Surface Energy	N/m
$\mathbf{\gamma}$	Ink Surface Tension	N/m
$\mathbf{\gamma_{SL}}$	Solid-liquid Interaction	N/m
$\mathbf{\theta_E}$	Equilibrium Contact Angle	degree
$\mathbf{\mu}$, $\mathbf{\mu_{FE}}$	Mobility	$cm^2/V \cdot s$
$\mathbf{\Phi_M}$	Electrode Work Function	eV
$\mathbf{\varphi_B}$	Hole Injection Barrier	eV

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1. INTRODUCTION

Electronics has changed our day-by-day life. This have been made possible by the great advances in microelectronics technology, in which miniaturized integrated circuits (ICs) consisting of billions of transistors enable the integration of computation, wireless communication, positioning systems and other features into a small device. For instance, the news and weather forecast, local maps and driving directions, commerce and other services are available by using a pocket-size mobile smartphone.

In parallel, traditional applications printed on paper are being replaced by electronics. The best examples are the barcode on consumer goods replaced by Radio Frequency Identification (RFID) tags, and traditional books replaced by a portable e-book [1].

The deployment of item-level RFID tags will significantly improve inventory control for retailers, as well as speed up the checkout process for customers in a commerce [2]. But in order to break into the current market, an item-level RFID tag needs to cost in the range of one cent USD to become cheaper than a barcode printed on the item label. This goal is extremely challenging because traditionally the cost of electronic devices is reduced by increasing the IC density on a silicon wafer. However, the cost of silicon per area remains high. Although a hybrid process is used combining a printed antenna and bonding of a very low-area silicon chip, the overall cost remains high due to a non-scalable bonding cost [2].

In a different example, a lightweight e-book with a large, thin, and flexible display can replace an entire collection of heavy books to deliver an interactive and comfortable reading experience. In order to massively replace traditional books an e-book needs to cost less than a typical textbook [3]. Currently, the Active Matrix Thin Film Transistor (AMTFT) array used for the display backplane is fabricated with conventional lithographical and vacuum processing, introducing high-cost processing. Furthermore, conventional processing temperatures are too high for plastic substrates required for realizing flexible displays. So, the display remains the major cost bottleneck.

So, a new technology for low-cost and large area applications is required to cover the cost and technological gaps associated with conventional microelectronic processing techniques. Large Area, Printed and Organic Electronics are becoming the most promising candidate to lead the next electronic revolution at low cost.

1.1. Printed Electronics

Printing techniques become an essential part of graphic arts for some centuries. Nevertheless, in the last years new concepts appeared under different names: "plastic electronics", "organic electronics", "printed electronics", "flexible electronics", "large area electronics"… to reflect new domains in electronic technology related to new materials, new devices, new functionalities and new production techniques announcing a revolution in microelectronic industry currently focused in silicon and lithographic techniques. Printing techniques are utilized to deposit functional materials on flexible substrates in order to build functional systems using electronic devices such as resistors, capacitors and transistors [4][5].

Conventionally, the fabrication of ICs involves a series of thin film deposition steps using vacuum processing, along with a series of lithography processes that include spin-coating photoresist, exposure, development, etching and photoresist stripping in order to transfer the desired pattern into a thin film. This patterning method requires several layers of masks and processes and also has a large waste of materials, increasing the processing cost. On the contrary, Printed Electronics utilizes printing techniques such as inkjet, gravure, and offset printing to additively deposit materials where they are required.

Over the past two decades Organic Electronics (OE) has dedicated a lot of efforts for substituting the inorganic semiconductors (silicon, gallium arsenide, etc.), silicon dioxide insulator and the metals such as aluminium and cooper. The efforts have been focused to improve the electrical properties and their stability. In contrast to conventional semiconductors, such as silicon, which are expensive to process, organic semiconductors can be fabricated with low cost techniques. The low thermal budget and the high degree of mechanical flexibility open new opportunities to produce soft, lightweight, environmentally friendly and flexible thin films for electronics applications over a small (sheet-to-sheet manufacturing) or large areas (roll-to-roll manufacturing).

Furthermore, Printed Electronics may begin to exploit high-throughput and mature printing technologies used in Printing Industry such as offset, flexography, inkjet… Roll-to-roll processes have demonstrated to print circuits as fast as some meters per minute, a speed capable of competing with parallel vacuum deposition processes [5]. Also, web-fed printing can use flexible substrates such as plastic or paper, which cost much less than silicon wafers or glass. Nevertheless, a lot of research is in process to improve printing techniques for the microelectronics requirements.

New materials research has become a key challenge for many companies in applied chemical and materials engineering. Several universities and large companies such as Henkel, BASF,

DuPont and Merck among others are developing new materials such as conductive, insulator or semiconductor for new production processes. However, low temperature processing becomes necessary as typical plastic substrates undergo a glass transition around 150-200°C, and the subsequent deformation may destroy the printed devices [6]. Fortunately, the development of inks has been successful in recent years, enabling low-temperature annealing or sintering of the semiconductor and metal nanoparticles, respectively [7][8].

1.1.1. Technology benefits

As Printed Electronics includes the creation of micro- or opto-electronic circuitry using printing methods, there are a number of technology benefits to be considered [9]:

1. **It is a ready route to flexible components.** Examples of these include flexible displays for mobile devices and smart textiles.
2. **It allows complete system integration.** Printing could be capable of the assembly of devices using multiple technologies (logic, memory, battery, displays, etc…).
3. **Process integration.** It allows electronics to be readily integrated as a part of other printed media by printing them on the same press. This gives access to products such as item-level RFID tags and smart packaging.
4. **Printing can be much faster than traditional wafer fabrication.** One estimate puts this speed difference as 4 orders of magnitude per device. This is the key to low cost production and is the facilitator of disposable electronics.
5. **Large surface electronics.** It allows printing electronics on large surfaces not constrained by wafer size, closer to display technologies.
6. **Environmentally friendly.** Organic materials uses more efficient printing processes in terms of lower power consumption and selective deposition processes improving the environmental impact of electronic industry.
7. **Bio-compatibility.** Using organic materials in biomedical implants can improve acceptance of these systems in contact with human body.
8. **Printing has a lower capital investment cost than other fabrication means.** It is estimated that a Printed Electronics plant will cost $30 million, just a fraction of a $3 billion conventional silicon fabrication plant [9].

1.1.2. Current challenges and trends

The current challenges to be considered can be summarized in the following points:

1. **Print quality:** Conventional printing is usually based around macroscopic measures (colour, visual sharpness, etc…) while Printed Electronics will bring in a whole new set such as dot morphology, line continuity, metrics for microscopic defects and layer registration.
2. **Printing substrates:** Substrates for Printed Electronics will probably continue to be dominated by plastics and glass with good dimensional and thermal stability [6]. For smart packaging and other applications paper is potentially useful and essential [9].
3. **Printing methods:** Every traditional analog printing technology (screen printing, flexography, gravure …) has been or is currently being used for creating electronic circuitry. Conventional printing systems such as flexographic, offset and gravure are best suited to mass production and this will likely continue in Printed Electronics. Screen printing also has a place and some early commercial electronics printing activity such as RF antennas or electroluminescent displays. At same time, there is a lot of interest in digital printing, which can be defined as using a digital file as the input to a printing mechanism avoiding use of masks or pre-patterned structures. The technical attributes of inkjet make it best suited to mass customization, small batch size and simple circuitry. Inkjet appears set to become an enabling technology for on demand production in Printed Electronics due to electronic design flexibility and rapid design testing. The choice in printing technologies will be determined by parameters such as run length, feature size and variable data requirements. Although patterning processes are being scaled to smaller dimensions; resolution, registration, uniformity and characterization of the manufacturing processes are still key challenges. Printed technology is planned to be used in room conditions (class 10.000 or lower) as close as possible to normal printing industry conditions.
4. **Ink properties:** In the last years a strong research improving organic semiconductor materials has been done as a strategic key in order to develop more complex systems. Currently, n-type semiconductors are approaching their mobility and stability to p-type ones allowing the use of complementary logic and pushing printed digital systems introduction. Additionally, dielectric and conductive inks have attracted a lot of attention in order to develop active devices or efficient RF antennas, for example.

Aspects at the bottom of Figure 1.1 are currently a key challenge for technology development, due to the fact that the link between materials and printing processes is crucial for the success of technology. Ink physical and chemical properties need to match perfectly with printing specifications. A customized ink is not useful for two different printing technologies.

Layer registration in different printing layers is a key challenge as it affects directly over device performance and system through design rules and device repeatability and stability.

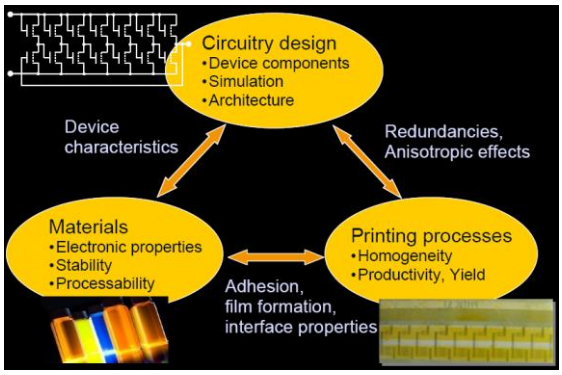


Figure 1.1. The Printed Electronics equation[1].

Design methodology depends directly of the technology evolution. Although circuit design will have the heritage of the silicon technology knowledge, the adaptation to the technology limitations, material evolution and printing processes will be required.

1.1.3. Summary

In sum, with advantages such as the ones previously listed, Printed Electronics has become a suitable technology for realizing low-cost and large area applications such as smart packaging, low cost item-level RFID tags, rollable displays and lighting, flexible solar cells, disposable diagnostic devices or games, printed batteries and so on...

A new business paradigm for Printed Electronics appears complementary to conventional silicon based fabrication. Its low performance and low integration density are its principal handicaps but lower production costs allow highly customized runs and small batch sizes facilitating disposable electronics.

However, Printed Electronics will not substitute traditional silicon microelectronics. Conventional printing technologies do not allow nanometric resolutions, so its potential is comparable to the one developed at beginning of the microelectronics industry. In the future, Printed Electronics will coexist with silicon, taking part only where it is better and beneficial. Link among them will use hybridization using low temperature processes.

[1] Source: BASF Gmbh.

1.2. Applications

New devices and applications has been developed into the fields of Organic Photovoltaics (OPVs), Flexible Displays (OLED and EPD), Lighting (including both OLED and electroluminescent products), Electronics and Components (including RFID, memories, batteries and other components) and Integrated Smart Systems (including smart objects, sensors and smart textiles). Figure 1.2 shows the roadmap for organic and printed electronic applications published bi-yearly by the Organic Electronics Association (OE-A).

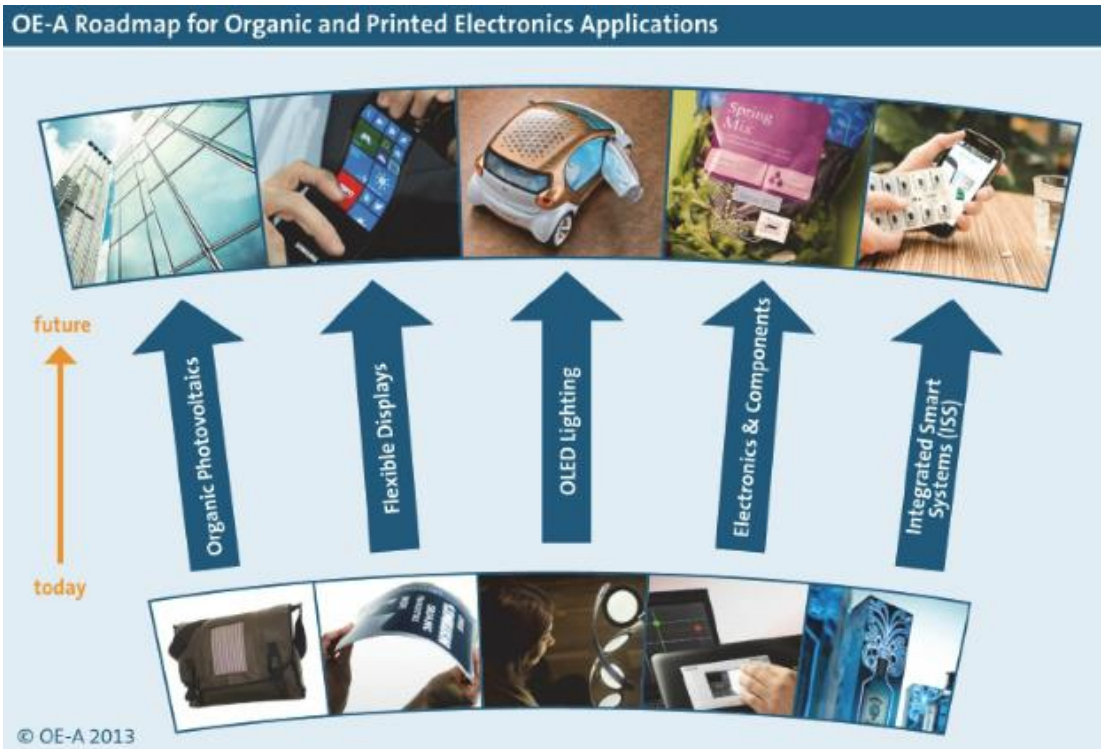


Figure 1.2. Roadmap for Organic and Printed Electronics Applications [10].

As this thesis is focused on electronics devices such as resistors, capacitors and thin film transistors, the examples of applications presented will be related to the use of these devices.

1.2.1. RFID tags and smart objects

The item-level RFID system is expected to replace the UPC barcode on individual consumer and industrial goods to improve automation of inventory control. Furthermore, item-level RFID tags can potentially be integrated with a sensor and a display to provide product information such as expiration date.

Most economic analysis suggests that the cost of each tag needs to be less than one cent USD to be used massively and become economically viable, since the individual tagged product

typically has a price floor in the range of few cents to few tens of cents USD [11]. This goal is extremely challenging.

The carrier frequency of the RFID system is allowed in the following four communication bands: 2.4 GHz, 900 MHz, 13.56 MHz and 135 kHz. For short distance applications, 13.56 MHz is the ideal frequency for item-level RFID applications because near-field inductive coupling can be used and more power can be supplied to the tags [12]. An RFID tag with 13.56 MHz carrier frequency have a small size (around two centimetres per side), and will work well in metal- and water-contaminated environments.

As illustrated in Figure 1.3, the RFID system is comprised of two main components to provide wireless communication: a tag/transponder and a reader/interrogator. The reader initializes the communication by providing a clock signal and power to the tag. Once the tag circuitry is powered up, the data inside the tag is sent back to the reader through a modulation scheme.

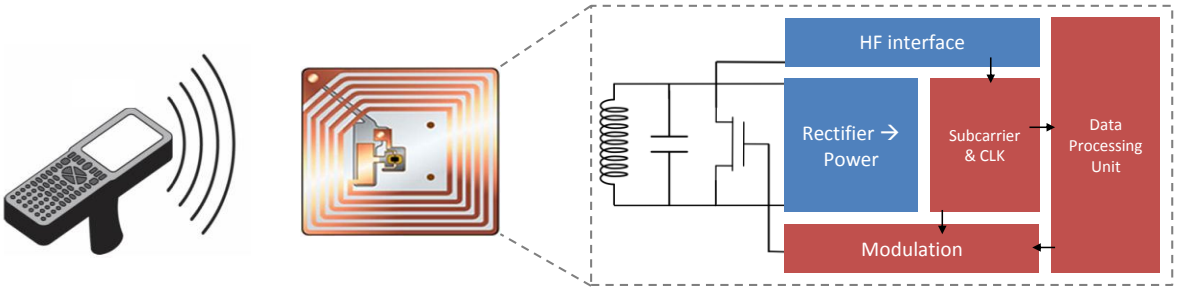


Figure 1.3. A basic RFID system comprising a reader and a passive tag.

In item-level passive RFID tags, the inductor and capacitor on the tag resonates at 13.56 MHz and a rectifier circuit converts the resonant RF signal into a DC power source to supply the circuit. Additionally, the circuitry inside the tag (shift registers, memory arrays, coding and modulation circuits) requires a clock to operate.

In the case of synchronous RFID tags, a high frequency (HF) interface divides down the 13.56 MHz signal to provide the clock for internal circuitry (typically in the range of kHz) and the sub-carrier for the back-modulation circuit. Unfortunately, the switching speed of the transistors produced by printing techniques is about two or three orders of magnitude slower than the required clock frequencies.

Asynchronous RFID is an alternative approach. A low-speed local clock is generated by an internal circuit (up to few kHz), which is feasible for printed transistors. However, the local clock frequency is prone to deviate over time and from tag to tag, due to material stability and the printing-process variations respectively. This difficult the data readout requiring a new RFID protocol to properly communicate with the asynchronous tag.

It is currently unclear whether synchronous or asynchronous tags will be used for item-level printed RFID tags. In either case, the performance and stability of the printed transistors will require a breakthrough in order to meet these requirements.

1.2.2. Sensors

Sensors have been a major topic of scientific and technological development separate to the evolution of the Organic and Printed Electronics industry. Indeed, many of the characteristic features of Organic and Printed Electronics have already been used in the development of sensors, from simple physical sensors (temperature or pressure), through chemical sensors and to very complex and sophisticated biosensors with additional biological components [10].

In the last decade, the attention to OTFTs increased significantly in the field of biosensing applications. The main difference is the replacement of the gate by introducing an electrolyte and a reference electrode [13]. Besides, by functionalizing OTFT with biological materials, a BioFET can be obtained as shown in Figure 1.4a [14]. The main advantage of OTFT based biosensor is the possibility to get an all-integrated, portable and low cost system, compatible with the "single-use sensor" concept. Currently, devices are fabricated by photolithography processes that require expensive masks and clean room facilities. To overcome these drawbacks printed-based OTFT for biosensing applications have been developed recently as shown Figure 1.4b. Among examples of transducers fabricated with these new technologies is the development of electrochemical biosensor based on gold electrodes by inkjet printing for detection of a cancer biomarker [15], glucose detection [16] and other applications [17].

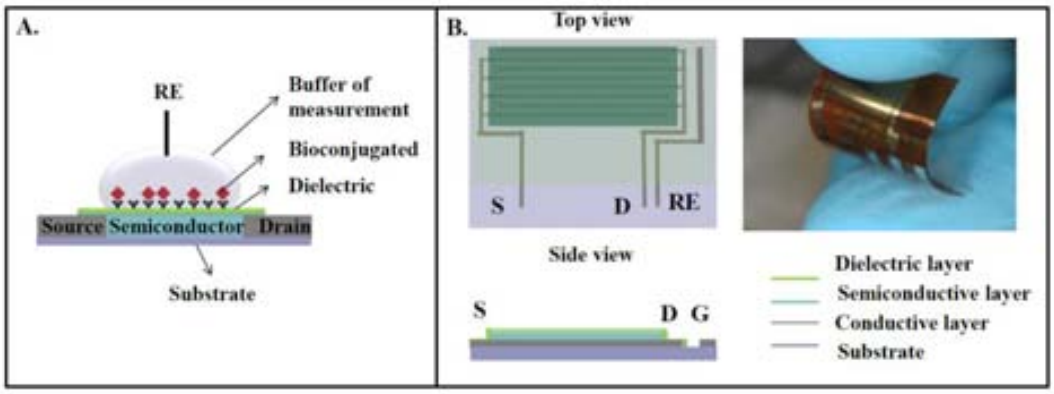


Figure 1.4. a) Scheme of BioFET components; b) top and side views representing each layer of the BioFET; and c) picture of the flexible printed device [17].

The other major obstacle for the implementation of sensors within organic electronics is the ability of organic electronic systems to supply analog electrical input and read analogue electrical output. Electrochemical transducers will require measurement of at least an

output signal and also the application of an input signal, such a signal may have noise of only fractions of a microvolt. This noise level becomes more significant as one tries to detect smaller physical, chemical or biological changes, which correspond to smaller changes in current. However, analog circuits using OTFTs suffer significantly from issues of drift and noise and this seriously inhibits their application to acquisition sensor circuits.

1.2.3. Displays

Display technologies has advanced rapidly and become an essential component of electronic systems. Major display technologies used for portable electronic devices are liquid crystal display (LCD), organic light emitting diodes (OLED), and electrophoretic displays (EPD). These technologies have in common the use of an Active Matrix array of Thin Film Transistors (AMTFT), acting as a backplane to control each pixel individually [18].

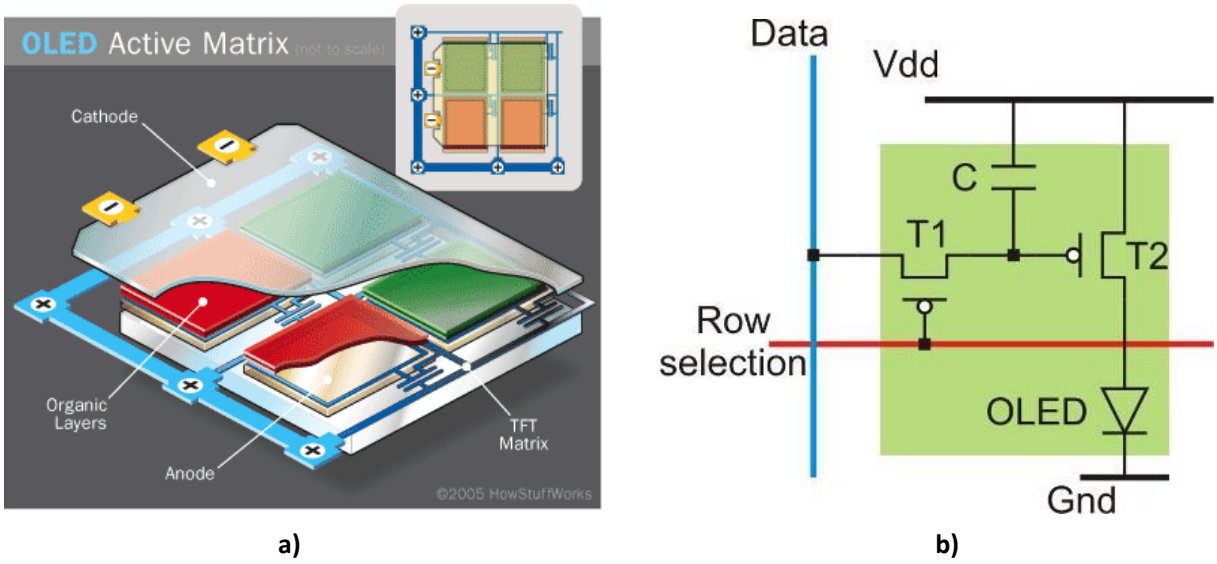


Figure 1.5. a) In an active-matrix OLED, cathode, organic EL and anode layers are stacked above a low-temperature polysilicon substrate layer that contains a thin-film transistor (TFT circuitry)[2]; and b) the schematic layout of a 2T1C pixel driver for AMOLED backplanes [19].

OLED is a self-emitting technology showing an advantage of higher contrast, wider viewing angle and faster response time. Figure 1.5a shows the basic architecture of an AMOLED pixel, comprising an AMTFT array and an OLED device. The OLED typically consists of an electron transport layer, an organic emitter layer, and a hole injection layer. The emitting layer of the OLED is controlled by using a TFT as shown in Figure 1.5b. T1 and the storage capacitor controls the voltage stored that is then applied to the gate of T2 as a gate controlled current source in order to control the OLED emitting current.

[2] Source: How Stuff Works - www.howstuffworks.com

Therefore, the brightness of the OLED is directly proportional to the current through T2 thus, the operational stability, variability and On/Off current ratio of TFTs is critical.

Another type of display technology is the electrophoretic displays (EPD) utilizing the reflective daylight to mimic the appearance of ordinary printed paper. EPDs can be read under direct sunlight and requires no power to maintain the display content, making it the most promising technology for e-book and other low-power applications. Currently, we can find in the market B&W and colour EPD displays. Figure 1.6a shows the cross-sectional structure of a B&W EPD, which is composed of millions of microcapsules sandwiched between two parallel electrodes. Each microcapsule contains white (positively charged) and black (negatively charged) pigment particles suspended in a clear liquid. Applying a negative electric field results in an appearance of a white pixel. And conversely, applying a positive electric field results in a black pixel. Monochrome and colour AMEPD are a promising technology to realize low-cost and flexible displays.

The simple operation of EPD results in a pixel with only one TFT as illustrated in Figure 1.6b. EPDs are voltage-driven and don't suffer extremely on the low stability of OTFTs. This is the reason why EPDs have been the first application to integrate OTFTs for its Active Matrix circuitry.

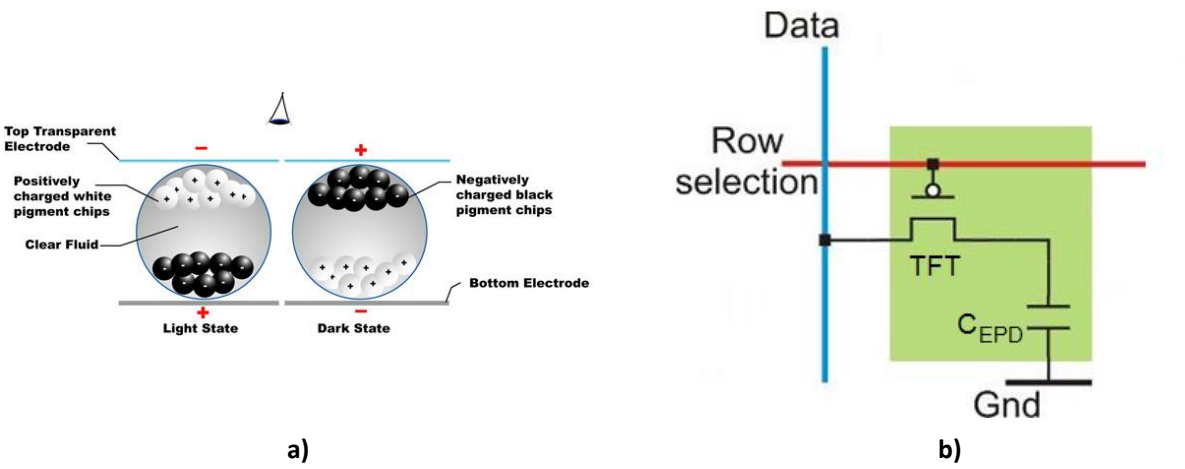


Figure 1.6. a) Electrophoretic display[3]; and b) Schematic diagram of an AMEPD pixel.

Nevertheless, for high resolution displays, manufacturing an Active Matrix array remains challenging due to the poor resolution achievable by printing-only process [20]. As a result, printing is currently more feasible for realizing low-cost and low resolution displays (e.g. AMEPDs). Therefore, a flexible or rollable display has become a market niche for this technology. The technologies implemented in the flexible display will most likely be

[3] Source : Pervasive Displays, Inc - www.pervasivedisplays.com

AMOLED and AMEPD using a cheap plastic substrates, which allows the incorporation of roll-to-roll and high throughput processing to further reduce the manufacturing cost.

Unlike the printed RFID application, which requires high-speed printed transistors, displays only require an operation speed of few KHz. Consequently, the speed-limiting gate-to-source/drain overlap is not a problem by the poor registration capability of printing techniques. However, the parasitic capacitances can disturb the voltage stored via capacitive-coupling from the scan line. This problem can limit the employment of printed Active Matrixes in displays of higher colour depth [21]. As a result, printed transistors with minimum parasitic capacitance are required. An approach to reduce overlap capacitance will be discussed in Chapter 6.

1.3. Printing techniques

A wide range of large area deposition and patterning techniques can be used for organic electronics as a variety of techniques have been used in the printing industry: screen printing, offset printing, flexography, gravure, inkjet printing, etc…

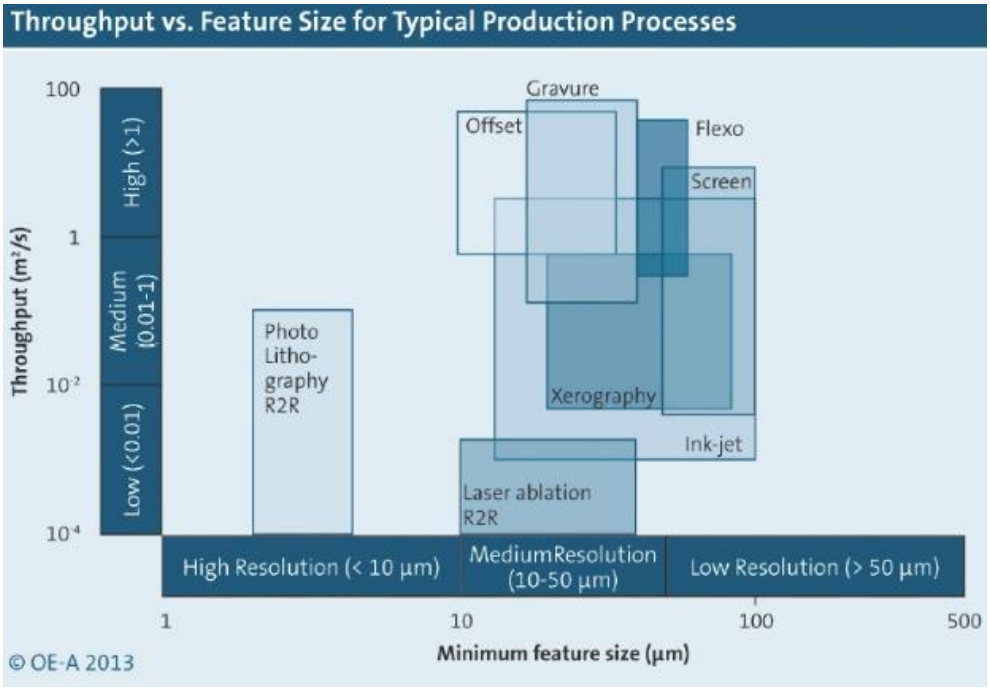


Figure 1.7. Resolution and throughput for a variety of processes [10].

The small feature that can be printed ranges from 20 µm to 100 µm depending on the process, and the film thickness can range from 100 nm to tens of µm. Each method has its individual constrains, and in general, processes with high resolution have smaller throughput as shown in Figure 1.7.

Screen printing has been employed for several years in the application of printed circuit boards, in which a thicker and lower resolution film is not a constraint. However, among the various printing techniques, gravure and inkjet printing are the most attractive systems due to their relatively high printing resolution and ink compatibility [10].

Figure 1.8a shows a schema of a typical gravure system, consisting of an engraved cylinder with a pre-defined pattern (various size wells) on the surface. The ink is coated on the cylinder as it turned through a reservoir and the excess ink on the cylinder surface is wiped off by the doctor blade. The ink filled inside the cylinder wells is then transferred when it turns and contacts the substrate. As a result, the pre-defined pattern is transferred on the substrate in a high-throughput fashion [22]. Therefore, the gravure system is attractive for

industrial high speed manufacturing but too expensive for research purposes. Several examples of devices and circuits using gravure printing are found in the literature [23][24].

Unlike gravure printing, inkjet printing is purely non-contact printing. As illustrated in Figure 1.8b, inkjet printing uses thermal or piezoelectric actuation to jet ink from a reservoir in order to deposit the droplet on the substrate. A pattern is then generated by either moving the substrate or inkjet nozzle to enable drop-on-demand printing [22]. The flexibility of the inkjet-printing system allows a change on-the-fly of the pattern. This non-contact and additive printing feature is well suited e.g. for sensor applications, in which different delicate sensing materials are printed without interfering with others. Moreover, the inkjet system has been utilized in the OLED display industry to deposit polymer materials separately [25].

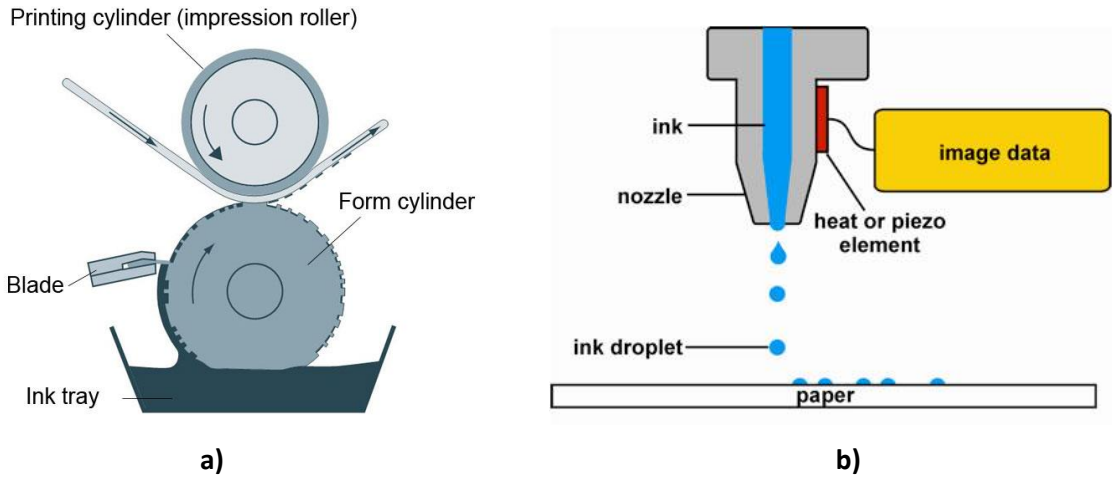


Figure 1.8. a) Principle of gravure printing[4]; and b) Inkjet printing system[5].

The serial printing characteristic of the inkjet system limits the throughput of the deposition. To overcome this disadvantage, industrial inkjet printheads utilizes hundreds to thousands of nozzles to realize throughput enhancement by using parallelization [22].

The feasibility of inkjet printing to realize low-cost Printed Electronics is currently unclear. Nevertheless, the flexibility of the inkjet system is still best suitable for a research purpose. Therefore, as inkjet is the selected printing technology in this thesis work, more details will be discussed in Chapter 2.

[4] Source: Siemens Gmbh.
[5] Source: Image Permanence Institute, Rochester Institute of Technology.

1.4. State of the art on the development of organic inkjet-printed devices and circuits

Over the past two decades the organic electronics community has dedicated a lot of efforts for substituting the inorganic semiconductors (silicon, gallium arsenide, etc.), insulators (silicon dioxide) and metals (such as aluminium and cooper) for alternative organic materials. Basically, the efforts have been focused to improve the electrical properties such as mobility, conductivity, dielectric strength, environmental stability and so on [26]. In contrast to conventional materials such as silicon which are brittle and expensive to process, organic materials can be fabricated with low cost techniques but materials and production processes are still immature [27][28].

In the field of applied materials a lot of research has been published about physical and chemical properties of the functional materials and devices, basically transistors, in order to investigate organic semiconductor materials and devices performance [29]. Although that, most major part of this research has been done using vapour or lithographic deposition techniques since it is a more stable process, better suited to analyse materials performance at very well controlled thickness and morphology. Unfortunately, the obtained performances are far from Printed Electronics concept and difficult to transfer and compare.

An important report about inkjet printing processes and applications was published by Jabbour et al. on 2010 [30] and by Schubert et al. on 2013 [31]. On these progress reports, particular applications such as OTFTs, OLEDs and sensors together with alternative deposition techniques were reviewed as an example of the state of the art on inkjet printing technology developments. Especially active has been the group of Prof. Subramanian from University of California at Berkeley. Some their publications are basic references for this thesis work, e.g. [4][11][32][33] and many others.

Some literature exists in the field of passive devices using inkjet printing techniques. However, resistors and capacitors have not attracted too much attention up to the moment as their advances are related to the progress in material development for OTFTs. Anyway, some recent works using inkjet-printing can be found in capacitors [34][35][36] and resistors [37][38][39][40]. Additional research has been done in inkjet printed devices for specific applications (antennas, conductive lines…). Many papers can be found dealing with coils and antennas by inkjet-printing [41][42][43][44].

Transistors are the basic component for electric switch elements or integrated circuits. It can be used as single component to amplify a current or combined with other transistor as an integrated circuit or logics. Use of OTFTs has been demonstrated in low-end applications not

requiring high mobility or switching speeds, such as item-level RFID tags [5][45] and Active Matrixes for displays [18][46].

For printed transistors, solution-processable materials have advanced rapidly to enhance the performance of printed devices [28][47][48] and to obtain suitable n-type organic semiconductors [13][49]. Maximizing mobility is necessary to achieve high speed transistors. Given this need, there has been significant amount of research demonstrating high-mobility printable materials [50][51]. However, these materials were mostly demonstrated using test structures consisting of a thermally grown oxide and evaporated gold electrodes with modified surfaces. It is currently unclear whether the high performance characteristics can be transferred to a fully printed structure.

Specifically, in the case of OTFTs, the poor printing resolution of state-of-the-art printing techniques has required to the use of large channel length and large gate-to-source/drain overlap to compensate the miss-alignment resulting from the poor layer-to-layer registration capability. Generally, inkjet printing offers a resolution ≥ 20 μm [10], limiting the smallest channel length that can be achieved. This has implications on the circuit design limiting the switching speeds to 1–100 Hz [52]. These large dimensions have prevented printed transistors from gaining commensurate speed improvement via advanced materials.

As a result, to reach scaling, new topologies and geometries of the printed transistors are pursued to enhance their performance in terms of higher operation speed, in a way similar to silicon technology,. Some efforts focused on reducing the channel length in order to overcome the switching speed limitation. Sirringhaus et al. [53] successfully demonstrated the use of a hybrid approach to create channel lengths from the micrometer to sub-100nm range using lithographically patterned hydrophobic banks to contain the spread of inkjet printed source–drain (S/D) electrodes. Similarly, Tseng et al. [3][54][55] fabricated devices and circuit blocks using a novel, fully inkjet-printed transistor process that self-aligns source/drain electrodes to gates, resulting in improved overlap capacitance achieving a minimum overlap of 0.78 μm between the gate the source/drain (S/D), contrasted to the >10 μm typically obtained in conventional inkjet-printed transistors. Other works can be found fabricating self-aligned transistors [52][56] or vertical transistors (VOFET) [57].

Inkjet-printed OTFTs prepared with small molecule semiconductors typically exhibit significant device-to-device performance variations [58]. New approaches to reduce device-to-device variation are required. Madec et al. [59] increased reproducibility of inkjet-printed TIPS-pentacene FET devices using a blend ink composed of TIPS-pentacene and an insulating polymer. They observed that the stable ejection of the blend ink decreased the device-to-device variations [28].

In the area of printed organic circuits, there are some important achievements. As an example for the setup of small molecule based semiconductors, Imec and TNO presented in 2011 an 8-bit organic microprocessor on plastic substrate [60][61]. The organic microprocessor works in a dual-gate configuration, using 4000 p-type pentacene transistors. The design comprises a microprocessor on a substrate and a hard-coded instruction set on a separate foil containing a hard-coded program. The program is capable of operating at frequencies up to 6 Hz, at an operational voltage of 10 V. This important goal was achieved by means of non-printing technologies. On February 2014 the same group presented a new version by using hybrid oxide-organic complementary thin-film technology. The n-type transistors are based on a solution-processed n-type metal-oxide semiconductor, and the p-type transistors use an organic semiconductor. As compared to previous work utilizing unipolar logic gates, the higher mobility n-type semiconductor and the use of complementary logic allow for a >50x speed improvement [62]. Other examples includes item-level RFID tags [5][45][63][64], Active Matrixes for displays [18][46][65][66] and analog circuits [67][68].

Some examples of circuits fabricated by gravure printing can be found in the literature including half- and full-adders on plastic foils [23][69][70].

Unfortunately, there are not similar achievements in printed circuits by using inkjet-printing technologies. Basically inverters have been demonstrated using self-aligned technologies [54] in some cases exhibiting frequencies as high as 1.6 MHz [52].

Summarizing, mobility, conductivity, relative permittivity and strength, switching speed, driving current, supply voltage, lifetime (shelf, operation, temperature, humidity, mechanical stress), processability, printing resolution and thickness of active and insulating layers (thinner and stable without pinholes) among others, are technology parameters that need to be improved through the development of better materials, inks and printing processes. So, there is still a long way to go before the maturity of the Printed Electronics technology.

Therefore, this thesis will focus on the analysis and improvement of OTFTs from different viewpoints as well as the statistical analysis of devices in order to study scalability and variability in all-inkjet printed transistors and passive devices.

1.5. Objective of this thesis

The main objective of this thesis work deals with the development of microelectronic passive and active devices by using organic and inorganic inks and circumventing the printing resolution challenges using compensation techniques and new layout geometries while keeping a low-cost all-inkjet purely printing process and centring the effort in the design, manufacturing & characterization (both electrical and morphological) point of view in order to fabricate organic integrated circuits.

The main objective of this thesis can be specified as follows:

1. **Baseline inkjet printing process & material characterization.** The various roles of active materials lead to different constraints on technology; thus the **d**ifferent conductive, dielectric and semiconductive inks need to be characterized in order to assess the morphology and electrical properties of the materials, interfaces and basic structures to optimize electronic devices.
2. **Development of passive devices.** The development of passive devices is the way to characterize multilayer structures that will allow improving the fabrication process and obtaining reliable materials for the manufacturing of OTFTs.
3. **Development of Organic Thin Film Transistors and simple circuits.** The development of a suitable and simple manufacturing process for all-inkjet printed transistors along with their physical and electrical characterization. The introduction of different strategies and approaches in order to improve OTFTs. The fabrication and characterization of simple circuits as inverters as a demonstration of the technology.
4. **Static and dynamic characterization over time as well as statistical analysis on scalability and variability of devices**. There is no literature in such analysis related to all-inkjet printed OTFTs. This thesis will contribute to the State-of-the-Art on this topic.
5. **An adaptive backend strategy for low-yield OTFT digital circuits** is needed as a solution to overcome one of the main drawbacks of inkjet printed devices, the low yield and variability due to printing effects.

Inkjet printing technology has been used in this work since it is very well suited for research, is a mask-less technology oriented to rapid prototyping for production, uses an additive process over any kind of substrates and it has a low material consumption.

1.6. Thesis organization

This thesis is organized in the following manner. Chapter 2 will introduce the inkjet printing system as well as inkjet fundamentals. Basics of electronic inks, wetting behaviour on surfaces and transistor operations will be reviewed. Baseline inkjet printing process required for a printed transistor will be discussed. Chapter 3 will introduce and discuss about the development of passive devices by using inkjet printing technologies. Different approaches and materials will be studied. Chapter 4, 5 and 6 are related to Organic Thin Film Transistors. Chapter 4 will introduce a complete manufacturing process for all-inkjet printed transistors developed in the framework of this work. Various printing parameters associated with the printed features will be discussed. Chapter 5 will introduce the characterization of such OTFTs manufactured in previous chapter. Static and dynamic characterization over time will be presented as well as the statistical analysis on scalability and variability of devices. Chapter 6 will deal with different approaches studied in order to improve the OTFTs manufactured and characterized. Different design and manufacturing strategies are taken in consideration and some interesting results are presented. Finally, Chapter 7 will introduce and discuss the basics of organic circuits. The static and dynamic analysis of a single stage inverter is reported. An adaptive backend strategy for low-yield OTFT digital circuits will be proposed as a solution to overcome the drawbacks of inkjet printed devices. Chapter 8 will conclude the thesis and outline the potential future work. An annex is included providing references, additional data and the layouts designed and used for this thesis work.

This work has been developed within the framework of two FP7 European projects: FlexNet (contract number 247745) and TDK4PE (contract number 287682). Some material characterizations showed in the following chapters have been performed by my colleagues in both EU projects. Specifically, some of the AFM images and surface characterization (roughness, etc…) of substrate and materials were performed by ENEA and/or TUC as it is marked in figures or text.

The main part of the electrical and morphological characterization was done in our group together with my colleagues at UAB. The electrical characterization of large quantities of devices was done at IMB-CNM by using their unique semi-automatic characterization facilities.

2. INKJET DEPOSITION OF FUNCTIONAL MATERIALS

Inkjet printing is a challenging and attractive technique due to its additive and contact-less processing that will lead to a new paradigm in digital fabrication through the construction of electronic devices and circuits drop by drop. In the last decade, its use has increase and today, inkjet printing is leading the large format printing both in high quality colour and black & white printing.

Moreover, the inherent flexibility of inkjet printing technology has significantly reduced the research time required from idea to proof-of-concept demonstration in a laboratory setting. Therefore, there has been an increasing research developing processes and devices using all-inkjet printing technologies [71][72][4] and hybrid approaches [30]. Advances in ink formulation have made printable materials such as metallic inks commercially available, thus allowing the printing of more sophisticated structures.

In Printed Electronics, the intrinsic characteristics of functional materials lead to different constraints on device technology. Different works [73][74] demonstrated the need for improving the pattern control of inkjet-printed lines and areas. By characterizing and optimizing the conditions or parameters that lead to different printed morphologies, electronic devices can be improved. Consequently, it is necessary to understand the baseline process of single printed layers, as well as multi-layer integration by inkjet printing. Therefore, in this chapter, we will first introduce the inkjet printing technology as well as some basics about the fundamentals of printable inks and ink-surface interactions.

Designing and fabricating devices and circuits requires a wide knowledge of process aspects and a complex interaction among concepts, tools and processes coming from different science and engineering disciplines. Process and design engineers already faced up to this problem several years ago at the earliest stages of silicon microelectronics technology, and the design rules concept contributed removing this interaction gap. For design rules generation we need a concise description of process characteristics. This is done through technology characterization of geometries and morphologies of printed patterns.

Additionally, a methodology for the optimization and characterization of the morphology of the printed lines and areas will be proposed to obtain the physical resolution limits of the manufacturing process.

Summarizing, a baseline inkjet printing processes required to initiate the fabrication of printed devices and circuits will be proposed and used in the following chapters.

2.1. Inkjet technology

During past years, an increasing interest in direct-write fabrication methods has emerged oriented to develop low cost and large area organic electronic systems. For this reason, inkjet printing techniques are attracting more attention as a potential manufacturing tool. Inkjet has a number of attributes for its evaluation and subsequent development: direct micropattern printing from a computer-loaded bitmap file, very low materials (ink) waste, and high-speed parallel nozzle printing.

The true promise of organic micro- and opto-electronics lies in the potential to produce all-polymer integrated circuits without the need to employ complex microlithography. Depositing patterns directly on a substrate with small liquid droplets generated by Drop-On-Demand (DOD) inkjet systems offering a low cost, non-contact, low temperature, flexible, and data driven patterning approach.

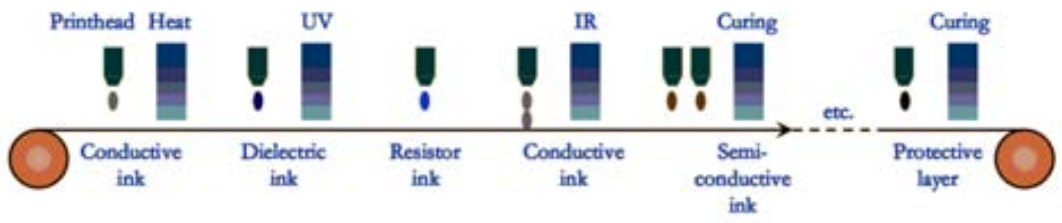


Figure 2.1. Inkjet printing electronics process[6].

Micro-fabrication of electronic and mechanical structures is typically a time-consuming and expensive process because of the complicated optical lithography system. Fabricating process patterns using small ink droplets generated from a DOD inkjet system could be an attractive alternative approach [75], as shown in Figure 2.2.

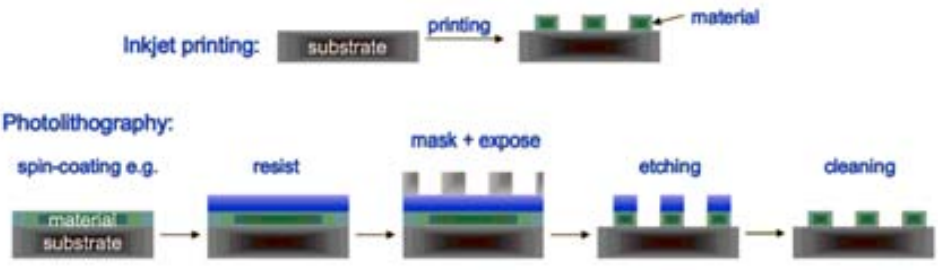


Figure 2.2. Inkjet versus photolithography process[6].

[6] Source: VTT Finland.

In a DOD inkjet printer, a printhead with an array of nozzles ejects material droplets under computer control. The ejected drop falls under action of gravity and air resistance taking a ballistic trajectory from the nozzle until it impacts on the substrate placed in a two dimensional platform (XY), spreads under momentum acquired on the way, and the surface tension aids flowing along the surface [76]. The drop then dries due to solvent evaporation [77]. The neighbour deposited droplets will overlap with each other forming patterns that could be used either as an active device layer or as a mask for subsequent process steps [78].

Maskless lithography using the DOD inkjet printing method has other advantages:

- The pattern quality is no longer limited by the depth of focus of the optics. Since droplets can travel relatively long distances without significant trajectory change, patterning on non-planar surfaces, small objects or even 3D structures becomes feasible.
- As low temperature process, micro-fabrication could also be performed on non-traditional substrates such as paper or plastics, which is especially attractive for building low cost circuits for flat panel displays, identification tags and other disposable electronic devices.
- Inkjet printing manufacturing could handle a wide range of materials; solution based materials like metals, organic semiconductors, polymers and exposure (or etching) sensitive materials could be used.
- As a data driven process, inkjet printing could directly transfer CAD designs into device patterns, which allow design customization.

2.1.1. Drop-on-demand technologies

There are different techniques to generate droplets but mainly can be summarized in thermal-bubble jets and piezoelectric jets [79]. A thermal-bubble jet nozzle consists of an ink reservoir and a small resistive heater as sketched in Figure 2.3.

A pulse of current is injected on the resistive heater to vaporize the ink around, forming a bubble and creating a pressure force to push out the ink in form of a droplet. The heater then cools down, resulting in a vacuum thus refilling the ink reservoir for a new ejection.

The resistive heater elements are typically made from poly-silicon fabricated using conventional silicon and MEMS (micro-electromechanical systems) processing. As a result, this type of nozzle is cheaper to manufacture, as no special materials are required such as piezoelectric crystals. Due to the low fabrication cost, the printheads can be disposed when the nozzles are clogged or cartridges end. Therefore, majority of the consumer inkjet printers commercially available utilize thermal-bubble technology. Another advantage of the thermal-

bubble jet is that it is not affected by the trapped air within the chamber, as the jetting does not rely on the mechanical compression of the ink.

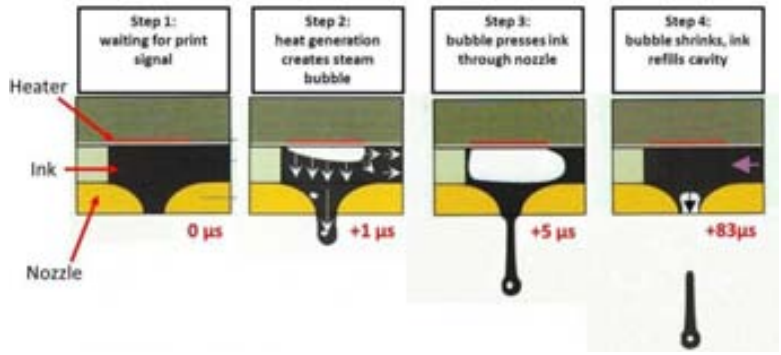


Figure 2.3. Schematic diagram of a thermal-bubble type inkjet nozzle[7].

But thermal-bubble jet has several disadvantages. The nozzles typically suffer from a short lifespan due to residue build-up on the resistive heater, and also, special ink is required to resist rapid thermal change. For the aforementioned reasons, thermal-bubble jet technology is not suitable for functional materials, where the inks used are not compatible with heat stress, e.g. metal nanoparticles can be sintered inside the chamber due to the heat, resulting in the deposition of metal layers on the resistive heater elements thus causing the malfunction of the nozzle.

The most popular technique used in Printed Electronics is the piezoelectric system, as shown in Figure 2.4 [80]. Piezoelectric nozzle does not apply thermal load to the organic inks compared with thermal-bubble inkjet technique. A voltage pulse is applied to the piezoelectric plate to cause a deflection, creating an acoustic wave that propagates inside the chamber and ejects the droplet. Due to the fast actuation of the piezoelectric plate (in the range of µs), the piezoelectric type can jet faster than the thermal-bubble type typically limited by the extra time required in the cooling step.

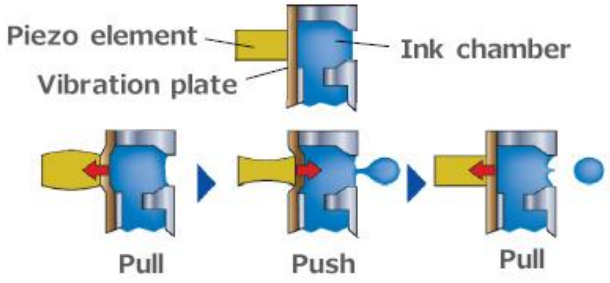


Figure 2.4. DOD inkjet piezoelectric nozzle ejection process[8].

[7] Source: Interactive Coding Equipment, Inc - http://www.interactivecoding.co.uk

The inkjet printing resolution is basically limited by the minimum drop volume ejected by the nozzle system. Currently, inkjet printheads are delivering liquid droplets with a volume starting at 1 pL, which creates spots >15 µm in diameter on the substrate, depending on the liquid contact angle and the substrate surface conditions.

Typically, the serial printing characteristic of the inkjet system limits the throughput of the deposition. To overcome this disadvantage, industrial inkjet printheads utilizes hundreds to thousands of nozzles to realize throughput enhancement via parallelization [22]. Figure 2.5 shows commercial DOD industrial multinozzle printheads from Fujifilm Dimatix Inc, USA.

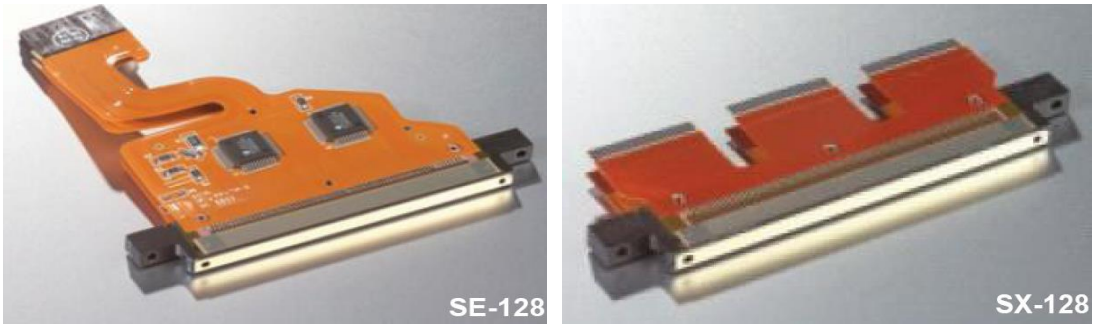


Figure 2.5. DOD inkjet printheads[9].

Recently, a new technology called super-fine inkjet developed by the Nanotechnology Research Institute of AIST[10] allows the ejection of super-fine droplets much smaller than the conventional droplets ejected by a conventional inkjet printer: less than 10% the size and less than 0.1% of the volume of conventional droplets.

2.1.1.1. Jetting waveform

The jetting in the piezoelectric nozzle is controlled by a waveform applied to the piezoelectric transducer (PZT). As illustrated in Figure 2.6, the droplet formation is driven by a waveform that can be divided into four segments. Each segment has three properties: duration, level and slew rate. The applied voltage relates directly to the volume of the pumping chamber, and the slew rate how fast is that operation. Changing duration, slew-rate or level values has a strong influence on drop formation.

More in detail, as shown in Figure 2.6, the start (or Standby) phase brings the PZT to a relaxed position with the chamber at its maximum volume. Immediately, in the first phase, a decreased voltage is applied to retract the PZT drawing fluid into the pumping chamber and

[8] Source: Seiko Epson Corp.
[9] Source: Fujifilm Dimatix, Inc.
[10] National Institute of Advanced Industrial Science and Technology (AIST).

followed by a settling time. In this phase the fluid is pulled into the chamber through the inlet and two in-phase acoustic waves are created in both ends of the chamber travelling in opposite directions (yellow arrows). The end of the first phase need to be aligned with the beginning of the phase 2 to expand the PZT precisely when the two waves meet at the center of the pumping chamber to push out a droplet with its maximum energy [81]. During the third phase, the PZT retracts slightly breaking the droplet from the chamber. The correct slope between phase three and four can provide a damping effect to prevent air from being sucked back into the chamber. Finally at phase four, the voltage returns back to the standby state.

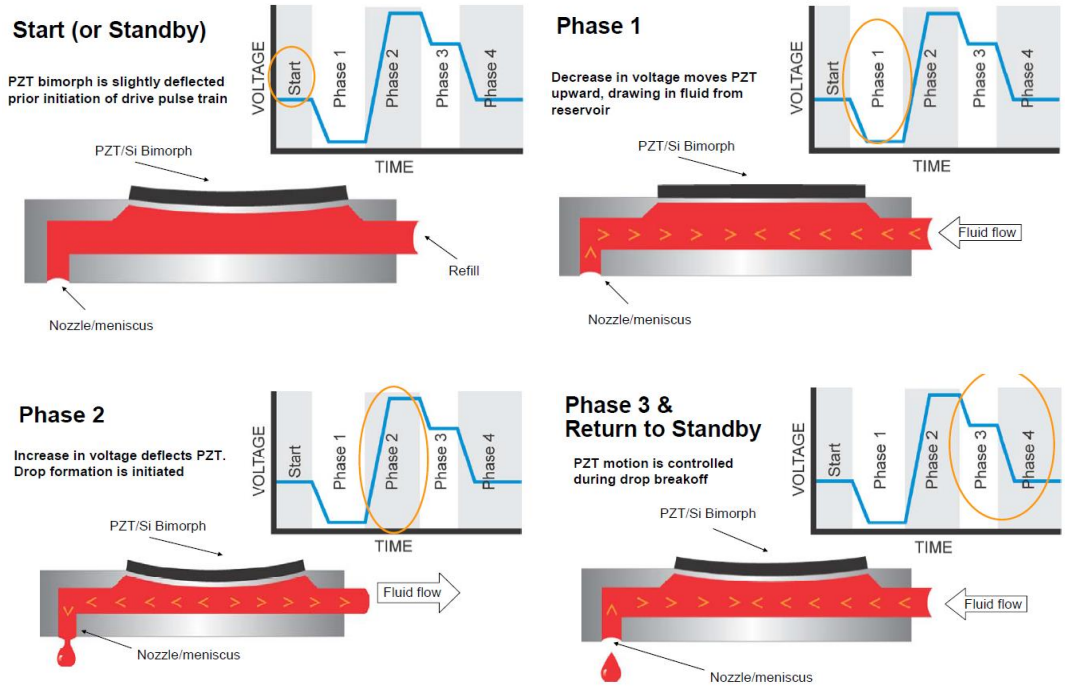


Figure 2.6. Diagram of a piezoelectric chamber showing the 4 phases of the jetting waveform and the corresponding PZT deflection [82].

The voltage applied to the PZT modifies the drop velocity and size. If the voltage is not enough, the drop is not created, as opposite if voltage is higher than the suited one (Figure 2.7a and Figure 2.7d), then the formation of the drop is accompanied by satellite drops (Figure 2.7b and Figure 2.7e). If voltage continues being increased the ejection is a random fluid spray (Figure 2.7c). The drop velocity is a function of the firing voltage, ink viscosity and surface tension. In the DMP system, a drop velocity of 6-10 m/s is desired; therefore, an ink with a viscosity of 10-12 cP and surface tension of 28-33 dyn/cm is recommended to obtain stable jetting [82].

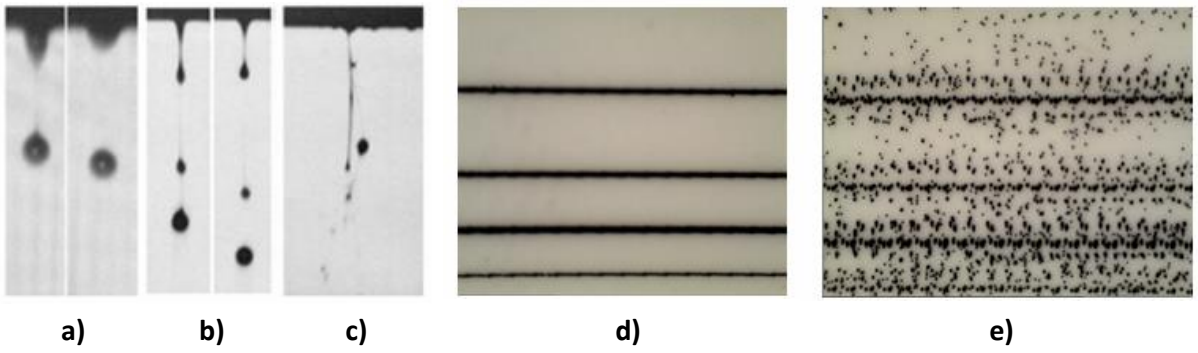


Figure 2.7. a) Correct jetting drops; b) drops with satellites; c) random spray jetting; d) optimum jetting printed line; and e) satellites effects on a printed line[11].

Drop velocity is an important parameter typically used to evaluate droplet jetting. The jetting waveform is typically optimized such that efficient jetting is achieved by obtaining the desired drop velocity using a minimum voltage. Higher drop velocity is desired, as the jetting accuracy can be improved by a reduced time-of-flight of the drop [83]. In addition, the drop velocity needs to be stabilized, as variations in drop velocity can result in variations in drop position. Moreover, in a multinozzle system, drop velocities between nozzles need to be matched in order to prevent variations in drop positions [31]. Therefore, the drop velocity is typically monitored before and during the printing to ensure a reliable printing process.

2.1.2. Inkjet printing for electronic applications

Printing electronic devices is more challenging than printing media. The former requires optimized jetting as well as good film qualities (i.e. good electrical properties and smooth surfaces), while the latter requires mainly a precise colour mixture and drop positioning. E.g. drop misalignments in Printed Electronics can rely in a non-working device while in printing media, an image with the colours misaligned could be sufficient for the human eye to interpret the content.

As shown in Figure 2.8, an inkjet system can be considered to consist of 3 key elements. In order for the system to work each must be compatible with the other two. For example, the ink must wet the media but not run off before drying. Similarly the ink must be compatible with the whole delivery system in the printer, from cartridge to nozzle.

For example, from the perspective of the printhead manufacturer, these issues refer compatibility of the printing fluid and the inkjet head. Similar perspectives correspond to fluid manufacturers [9].

[11] Source: Fujifilm Dimatix.

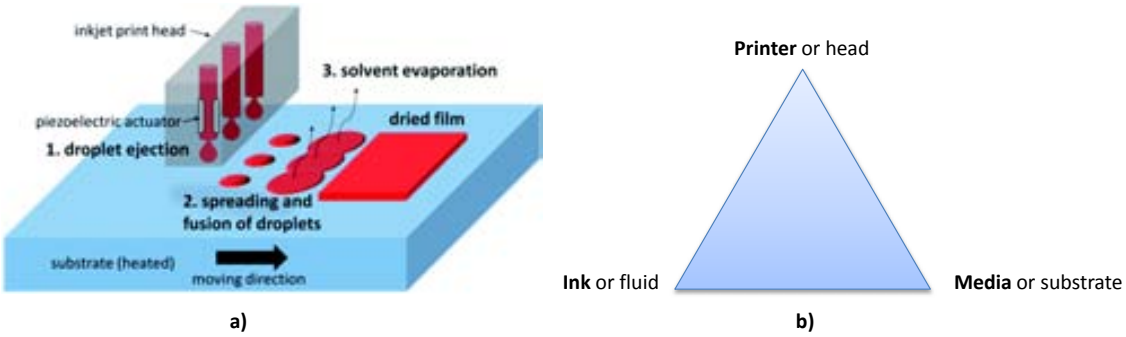


Figure 2.8. a) Inkjet printing process [84]; and b) the printing "system" [9].

Therefore, for inkjetting functional materials, the engineering of ink and ink-surface interaction are crucial in achieving an optimized thin film. Thus, the following sections will introduce electronic inks and discuss the wetting characteristic of inks on surfaces.

2.1.2.1. Electronic inks

Among the various printed electronic devices, active components such as transistors require the biggest quantity of layers. In order to inkjet-print a transistor, at least three categories of inks/materials are needed: conductor, insulator and semiconductor inks. There are organic and inorganic types of conductor, semiconductor and dielectric inks.

The most commonly used inorganic conductor ink is a nanoparticle-based where nano-crystals (5-100 nm) of metallic particles are encapsulated using an organic encapsulant/dispersant. The nanoparticles can then be dispersed in common organic solvents for inkjetting. After printing on a substrate, a heating/sintering step is used to firstly evaporate the solvent, followed by the disassociation of the encapsulant/dispersant, and finally to melt the metallic nanoparticles resulting in a metal thin film. The process [85][86] is depicted in Figure 2.9. Sintered gold nanoparticle has been demonstrated with a conductivity as high as $3 \cdot 10^7$ S/m (70% of bulk gold conductivity) [4]. Therefore, nanoparticle-based inks are promising candidates for producing electrodes and interconnections for printed devices.

The required temperature for the sintering of the nanoparticles is determined by the size of the particles and the encapsulant/dispersant. The melting point of metal nanoparticles is significantly reduced (relative to the bulk melting point) due to a high surface-to-volume ratio. E.g. butane-thiol encapsulated gold nanoparticles with 1.5 nm size have been demonstrated to sinter at a temperature as low as 120 °C [8]. With the advantages of high conductivity and low sintering temperature, silver nanoparticle inks are used exclusively in this thesis for printing interconnections and device electrodes.

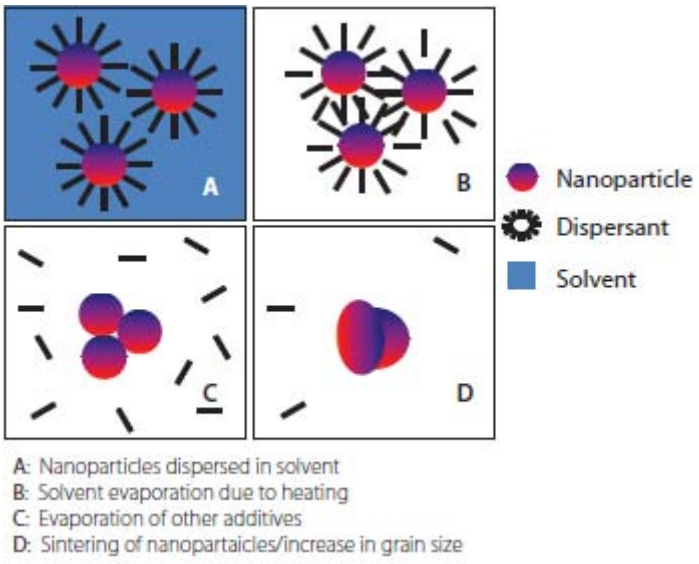


Figure 2.9. Schematic of a sintering process of nanoparticle inks: A) before heating; B) solvent evaporates and start degradation by heat; C) sintering start; and D) sintering finish [86].

For the insulator ink, organic dielectric materials are more widespread than their inorganic counterparts. The most commonly used polymer dielectric is Poly(4-vinylphenol) (PVP) that can be dissolved in alcohol based solvents for inkjetting. Several crosslinking agents are typically used to chemically crosslink the PVP into an electrical insulator. PVP has been used as a standard dielectric in studying organic transistors for years [87] and it will be used on this thesis work as well.

Similarly, semiconductor inks typically consist of an organic semiconductor dissolved in one or more organic solvents.

The advantage of inkjetting a polymer comparing to a nanoparticle ink is that the viscosity can be adjusted directly by changing the polymer concentration in the solvent.

2.1.2.2. Wetting of inks on surfaces

The wetting characteristics of inkjetted deposited drops on surfaces are crucial for controlling the formation of lines and thin films. Basically, the drop has two wetting regimes: partial wetting and total wetting as illustrated in Figure 2.10 [88]. A spreading parameter S is defined as the difference between substrate surface energy γ_{SO} and the sum of ink surface tension γ and solid-liquid interaction γ_{SL}.

When S is negative, the drop forms a spherical cap on the substrate with an equilibrium contact angle θ_E. This behaviour is favourable in printing fine lines for electrode applications. As it will be discussed in Section 2.2, the thickness and linewidth can be controlled with varying drop spacing, platen temperature and number of layers. When S is positive, the

liquid spreads completely thus minimizing its surface energy. This is desirable for printing thin layers of insulators and semiconductors [88]. However, the resulting thin layer typically exhibits a coffee ring stain due to an enhanced evaporation, which will be discussed later.

To change the wetting characteristics, substrate surface treatments are typically used to change the contact angle, as illustrated in Figure 2.10. To improve the wetting, a higher γ_{SO} surface or equivalently a more hydrophilic surface is preferred. On the contrary, a lower γ_{SO} surface or a more hydrophobic surface can be used to reduce the size of a pinned drop, in achieving smaller printed lines. However, when θ_E is larger than 90°, the drop become unstable and can dewet the surface.

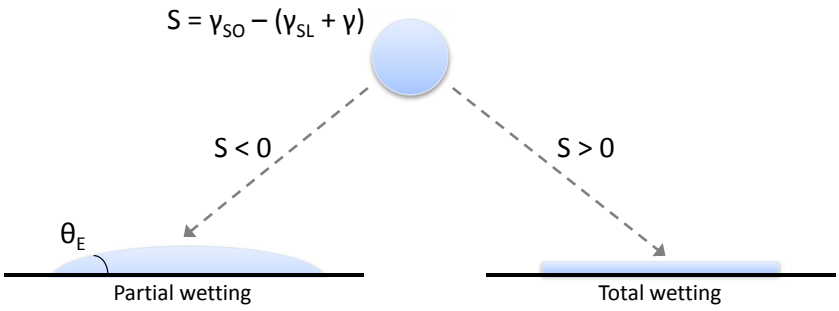


Figure 2.10. Wetting regimes and equilibrium contact angle.

Therefore, for a surface consisting of both hydrophobic and hydrophilic regions, e.g. a hydrophobic PVP with hydrophilic silver source & drain electrodes surface, optimization of surface treatment is required to obtain uniform wetting of inks on such mix of different surfaces. This is the case, in the Thin Film Transistor (TFT) stack used in this thesis work, when printing organic semiconductor on top of the dielectric layer containing source & drain electrodes in. To optimize surface printability rendering the surface more hydrophilic and avoiding dewetting, an oxygen plasma treatment will be used in this thesis work, as it will be discussed in Section 4.4.

2.1.2.3. Coffee ring effect

The coffee ring effect was first explained by Deegan et al. [89]. A coffee ring stain can easily be obtained when the inkjetted drop completely wets the surface leading to an excess of solute at the edges, as shown in Figure 2.11a. This is due to higher evaporation at the outer edges of the deposited drop, causing an outward convective flow to replenish the lost solvent thus resulting in the accumulation of solute at the edges. The coffee ring stain is detrimental for a homogeneous film formation, as relatively thicker walls can appear at the outer edges.

The coffee ring effect can be reduced using several methods: e.g. changing the substrate temperature has been demonstrated to eliminate the coffee ring [78]. In such case, the difference of temperature in the substrate can delay the evaporation in the outer edges much more than in the center of the deposited drop, resulting in a reduced outward flow and hence reduction of coffee ring formation.

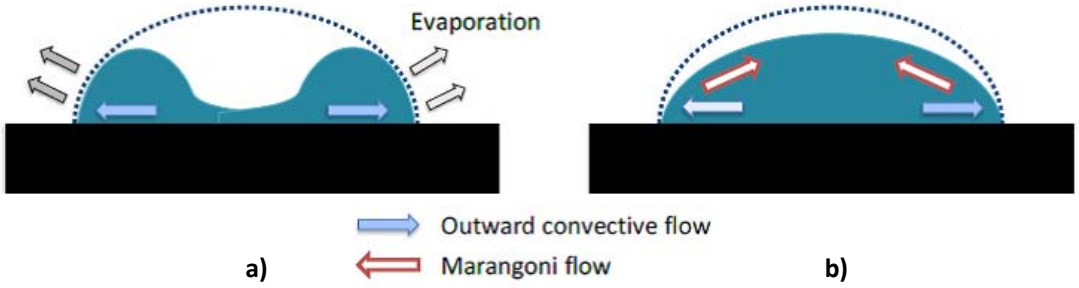


Figure 2.11. The process of drop drying after deposition with inkjet printing: a) coffee ring formation; b) coffee ring suppressed by Marangoni flow [77].

Another method is based in the incorporation of a co-solvent system with a higher boiling point and a lower surface tension to suppress coffee ring [90]. Figure 2.11b illustrates the principle. Due to higher evaporation at the outer edges, the solvent composition at the outer edges becomes mainly the solvent with high boiling point. As a result, the solvent at the edges has a lower surface tension than in the center, resulting in a surface tension gradient, then a surface-tension driven Marangoni flow occurs to carry the solute inward to the center [91]. This Marangoni flow can thus compensate the outward convective flow, eliminating the coffee ring effect. Thus, the mixture of solvents is a key in order to obtain uniform thin layers.

2.1.2.4. Inkjet pattern control parameters

Inkjet printed patterns are composed of discrete pixels due to the digital printing using drop ejection. In inkjet process, it is possible to control distance between ejected drops that creates an overlapped discrete spots of deposited fluid. As shown in Figure 2.12, the difference between idealized pixel and real spot is important in terms of shape matching for parameter extraction process. So, the resolution of printed patterns basically depends on the drop size once is deposited in the substrate and the percentage of drop overlapping.

Drop overlap is determined by drop size and drop spacing. The latter can be controlled in first term by the printer. The drop overlap percentage depends on drop size, and drop size is subjected to ejected drop volume and substrate-ink interaction.

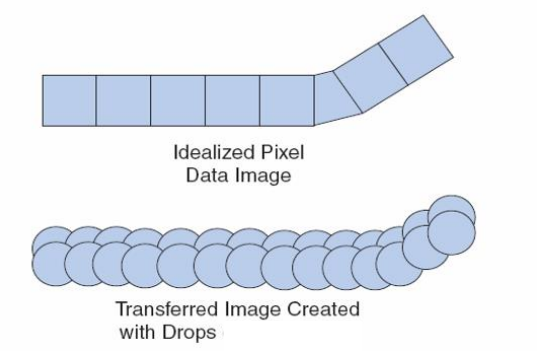


Figure 2.12. Discrete image formation in digital system.

Other important problems, often encountered during printing, are listed in the following paragraphs.

Misdirected nozzles refer to drops that are traveling off axis from left to right, or front to back. Figure 2.13a and Figure 2.13b illustrates a jet ejection off axis in the drop watcher and the effect on printed pattern. The primary causes of misdirected nozzles are contamination on the nozzle plate or air inside the nozzle orifice that are forcing the drop to eject at an angle.

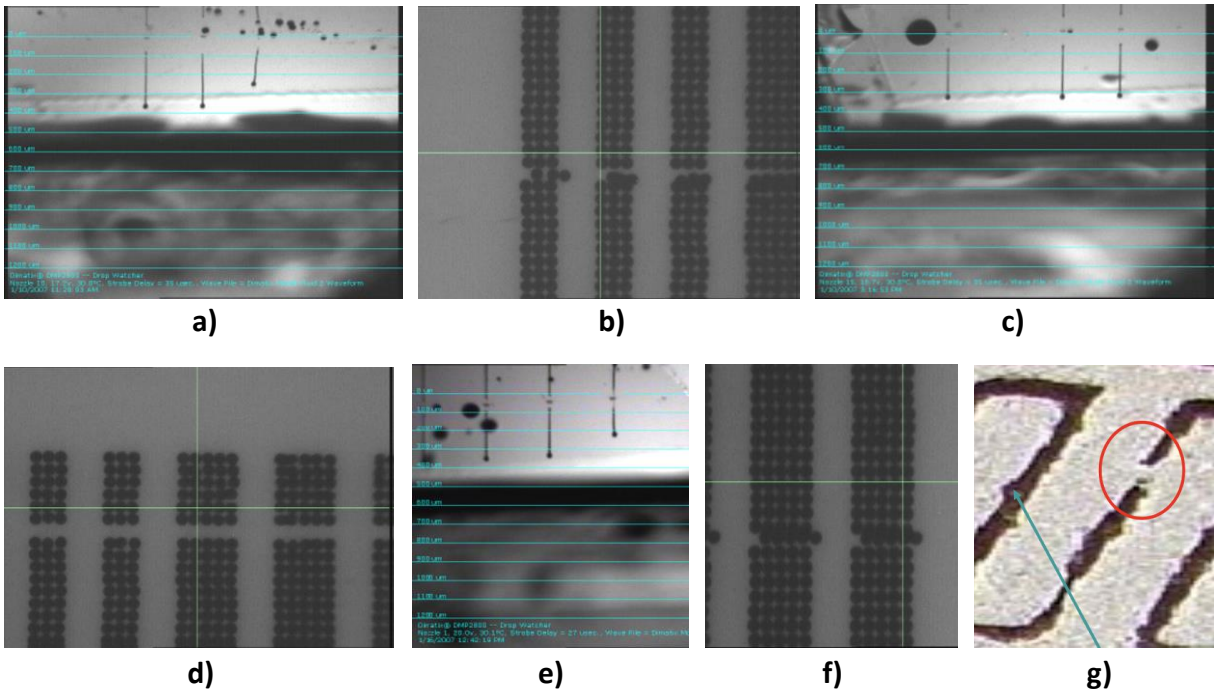


Figure 2.13. a) Misdirected drops and b) effect on printed pattern; c) non-jetting nozzles and d) effect on printed pattern; e) non-matched velocities; f) and g) effect on printed pattern[12].

[12] Source: Fujifilm Dimatix, Inc.

Non-jetting nozzles are nozzles that do not eject a drop under any condition and are adjacent to nozzles that are jetting properly. The reason can be for air entrapment in the pumping chamber or nozzle orifice is clogged. Figure 2.13c and Figure 2.13d shows a non-jetting nozzle in the drop watcher and its effect in the substrate.

Non-Matched Velocities. For a proper parallel ejection it is absolutely essential to adjust the drop velocities for all used nozzles. This has a direct impact on image quality and overall line fidelity. Figure 2.13e shows drop ejection with non-matched velocities. Figure 2.13f and Figure 2.13g shows the effect when the drop velocities are mismatched resulting in deposited drops not correctly aligned with the rest of ejected drops.

2.1.3. Inkjet printer

The inkjet printer used in this thesis is a piezoelectric jet system from Fujifilm Dimatix Inc. The system was used for all the printing in this thesis work, due to its smaller drop volume and hence smaller achievable linewidth. The details of the printer can be found in [82].

2.1.3.1. Dimatix Material Printer

The Dimatix DMP-2831 series is a low-cost commercial research inkjet printer. It is a self-contained system with an A4-size substrate platen, a cartridge holder module, a drop watcher system, a fiducial camera for alignment, etc... as shown in Figure 2.14a and Figure 2.14b. The stage motor has a 5 µm resolution and repeatability of ±25 µm. This resolution and mechanical accuracy is not enough to achieve consistent alignment in printing highly-scaled devices, as it will be analyzed in Section 2.4.2.

The substrate platen can be heated up to 60 °C. The use of substrate heating can be used to slightly enhance the drop drying in order to improve the film formation. But the substrate heating can unintentionally raise the nozzle temperature and degrade the jetting.

General purpose printheads are equipped with nozzles delivering a drop volume of 10 pL. Additionally, printheads with 1 pL nozzles are also available from Fujifilm Dimatix but were not used in this work due to the high evaporation rate at the meniscus, causing frequent clogging of the nozzles thus difficulting the printing operation.

The desired printing pattern can be generated importing a bitmap pattern file. However, the pattern can only be printed in a raster manner, i.e. one horizontal row at a time, even when printing a vertical line. This restricts the printing of single pixel lines used in interdigitated printed devices such as TFTs to be horizontal, as the printing of vertical lines show rough edges as it will be studied in the following section.

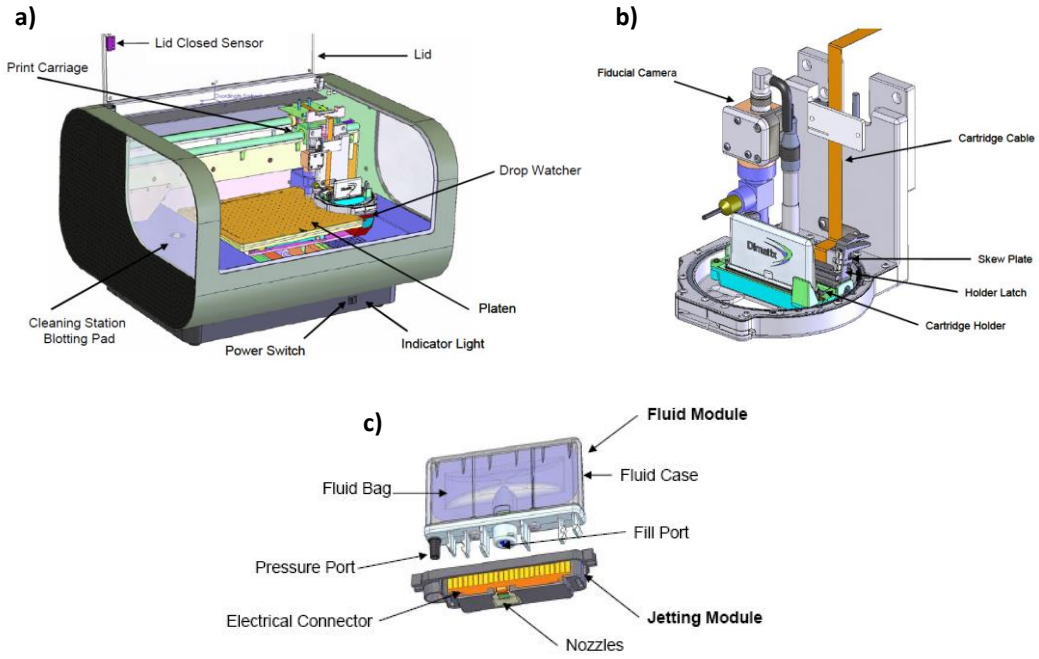


Figure 2.14. a) Dimatix material printer; b) printer cartridge assembly; and c) printhead and cartridge [82]-

The built-in software provides a fast alignment function (both XY alignment and theta calibration). Standard nozzle cleaning routines including spit, purge and blot of the nozzles can be user defined, allowing for an efficient cleaning procedure.

For this thesis work, the drop-on-demand inkjet printing was undertaken in a clean room (class 10.000) laboratory environment comprising a filtered ambient and humidity controlled.

2.2. Printed features characterization and extraction

In Printed Electronics, the intrinsic characteristics of functional materials lead to different constraints on device technology. Different works [73][74] demonstrated the need for improving the pattern control of inkjet-printed lines and areas. By characterizing the conditions or parameters that lead to different printed morphologies, electronic devices can be improved in terms of electrical performance.

2.2.1. Inkjet printing considerations

Some representative effects of inkjet-printed features are reviewed in Figure 2.15 as an example of printing behaviour. The discrete drop nature of inkjet-printed shapes can create scalloping line behaviours as shown in Figure 2.15a. Besides, the balance between drop size, drop spacing and ink-substrate interaction can create a bulging effect [78] as shown in Figure 2.15b.

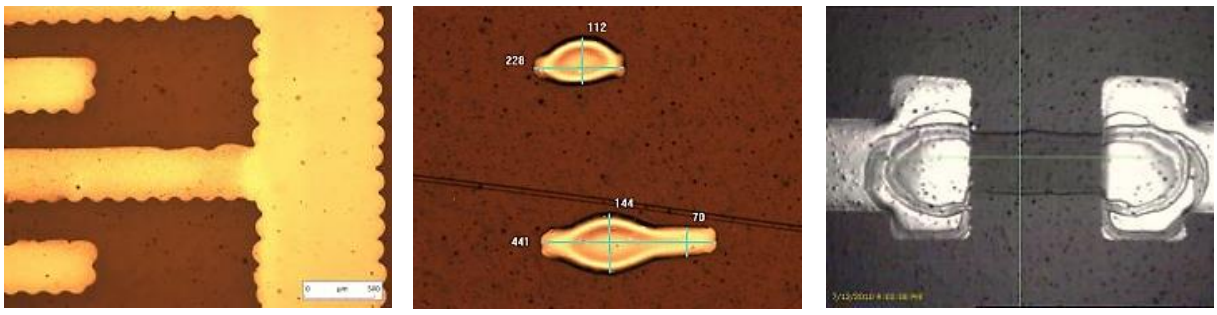


Figure 2.15. Different printing behaviors.

Printing layer-by-layer directly affects the device performance because the prior functional material deposited modifies the expected morphologies of the subsequent layers [92] as shown in Figure 2.15c.

Let us to consider the printing of a complex device such as an Organic Thin Film Transistor (OTFT) as shown in Figure 2.16. OTFTs are excellent candidates for its low-cost of fabrication and large area production, because they allow the construction of blocks such as logic gates and more complex circuits. OTFTs have been fabricated with various device geometries but, basically, these consist of (1) narrow lines as drain-source electrodes (Figure 2.16f); and (2) areas as gate, insulator and organic semiconductor layers (Figure 2.16d, Figure 2.16e and Figure 2.16g). The printed morphology of the lines and areas are one of the key factors to improve electrical characteristics of the OTFTs. In fact, printing parameters can be tuned in order to realize optimal morphologies even though the intrinsic constraints of

the materials. To explain the relation between the electrical characteristics of an OTFT with the device geometry is necessary to take into consideration all parameters that affect the transfer characteristic in the saturation regime:

$$I_{DS_{sat}} = \frac{1}{2}\mu_{FE} C_i \left(\frac{W}{L}\right)(V_{GS} - V_T)^2 \qquad Eq.\ 2.1$$

Variations of the channel length (L) due to scalloping of the lines (Figure 2.15a) or channel width (W) as a result of the non-desired geometry produces a modification of the transfer curve characteristic and thus introduce variability among OTFT devices [93] and finally to logic gates. Besides of lines and areas, the layer thickness plays an important role both in the gate capacitance (C_i) and the gate leakage current for instance.

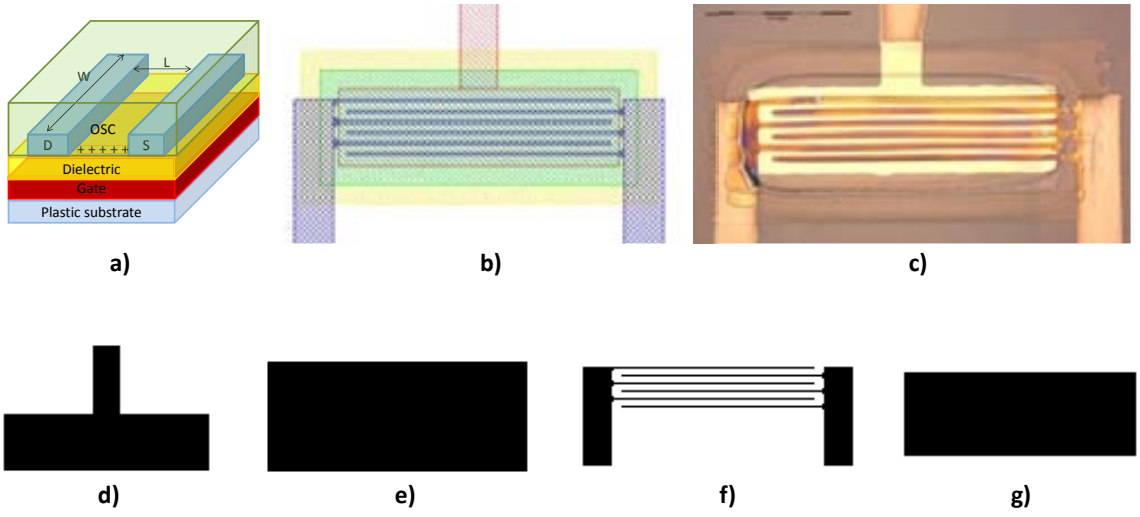


Figure 2.16. a) OTFT Structure; b) OTFT layout design; c) image of an all-inkjet printed OTFT; d) gate contact layer pattern; e) insulator layer pattern; f) Source/drain layer pattern; and g) semiconductor layer pattern.

In this section we propose the technology optimization and characterization methodology for the design rules extraction related to OTFTs but this can be used to other devices (e.g. passive devices, antennas, sensors…). This approach aims to achieve a good matching between the designed and inkjet-printed geometric relations as shown Figure 2.16b and Figure 2.16c respectively. Moreover, an interesting alternative is proposed to reduce the layer thickness by means of tuning the drop lattice.

2.2.2. Technology Characterization Methodology

For design rules generation we need a concise description of process characteristics. This is done through technology characterization of geometries and morphologies of printed patterns. The quantitative relation between designed patterns and printed dimensions are

the key factor, as discrete inkjet printing resolution and inkjet spot-based patterning restricts pattern generation.

We have developed a methodology to optimize the morphology of the printed lines and areas. Different parameters and characterization structures need to be considered in order to find out the optimal printing feature, prevent line instabilities and to obtain the design rules related to the physical resolution limits of the manufacturing process.

In the field of printed technology is important to control the fidelity of the patterning feature to reproduce exactly the circuit layout. By defining the optimal patterning we can find out about the design rules such as minimum width, spacing, notch and so on up to get the minimum feature size manufacturable by the technology.

Previously to the patterning optimization is paramount the characterization and subsequent drop optimization in order to avoid instabilities of deposition, curing and so on. Once, the single drop deposition is optimal the next step is to control the behavior of inkjet-printed lines and areas in order to determinate the final shape (first methodology step). Although some printing parameters are controllable, ink physical properties cause a non-homogeneity distribution of the deposited material. This nature of the inkjet technology leads to the compensation techniques (second methodology step) to sort out the ink coalescence to transfer properly the pattern. After applying the mentioned material characterization and compensation techniques, the printed pattern is totally optimized in terms of morphology and variability. Finally, the design rules (third methodology step) of a particular ink can be extracted by means of pattern test structures. The paramount goal is to print smooth, narrow and straight lines as possible. For the case of areas, the main issue to take into account is the smooth edges. Different pattern test structures are required to obtain the minimum feature size such as width, spacing, notch and corners. The main goal of these structures is to take technology at their limit mitigating unwanted phenomena into the printed features.

2.2.3. Material characterization

Some works reporting one-dimensional [73][94] and two-dimensional [95] models for printed lines dimensions can be found in the literature. In this work, we will focus on its extraction for defined shapes by using an empirical method through test patterns printing and characterization. This is a costly method but, useful for the generation of controlled pattern libraries for target applications.

As inkjet-printing technology is spot-based patterning system, the basic element is the deposited drop.

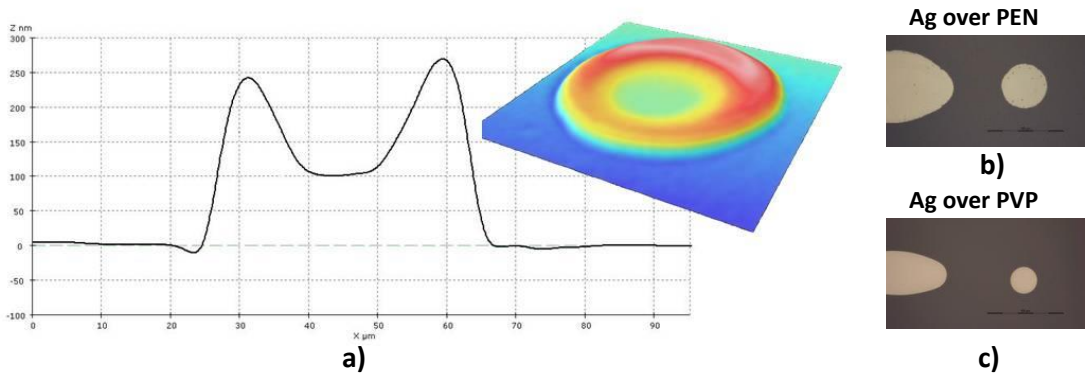


Figure 2.17. a) 3D and sectional image of a drop with coffee ring; b) silver line and dot over PEN substrate; and c) silver line and dot over PVP insulator layer. Images are on the same scale (Note: Measure = 100 µm).

Therefore, a first approach to printed pattern dimensions can be done using the following equation [96] where n is the number of deposited dots, DS is the drop spacing and D is the spot diameter.

$$Width = (n-1) \cdot DS + D \qquad Eq.\ 2.2$$

However, Equation 2.2 can only be considered as a first approach to estimate dimensions for printed patterns before physical characterization because it does not consider the overflow occurred when the ink density increases locally or coalescence occurs. The nature of printed lines is complex and differences arise due to a number of process factors (e.g. ink-substrate interaction, drop spacing, jetting frequency…).

An example of the ink-substrate interaction is shown in Figure 2.17b and Figure 2.17c, the silver line and drop morphology differ depending on the layers beneath it. To exemplify it, take into account an OTFT bottom gate bottom contact structure, the gate and drain-source electrodes will be patterned different onto the substrate or the insulator layer.

It is known in the literature that one can tune the relative distribution of material across the printed line by controlling the substrate temperature and drop-on-demand delay [78]. Our work will extend the research by means of tuning the drop lattice [97].

Furthermore, some works [98][99][100] report the ejection parameters such as viscosity, ink concentration, surface tension, and waveform of piezoelectric printhead and so on to obtain a good bead expelling without satellites or tails. We assume an optimized drop ejection since our work is focused on drop deposition instead of the drop ejection.

The independent variables considered were:

- **Drop spacing:** defined as the distance between two consecutively printed drops and is scaled by the wetting diameter of the drop on the substrate

- **Jetting Frequency:** is inversely proportional to the delay period of the consecutive expelled beads. Clogs or misdirected drops limit the lower jetting frequency.
- **Drop lattice:** Modifying the pixel lattice in pattern design one can adjust geometrically the amount of ink deposited per unit area.
- **Platen temperature:** Substrate temperature is related to solvent evaporation rate, which subsequently affects ink spreading and coffee ring effect.

Different combinations of parameters were used in order to optimize the material deposition.

2.2.4. Experimental for material deposition optimization

This is the first step of the methodology proposed. In this phase of the methodology, a conductive ink was selected for the material characterization and optimization for the critical impact of the drain and source electrodes to the OTFT performance, and its printing complexity in contrast to the organic semiconductor and insulator films.

The conductive ink used was a 20 wt% silver nanoparticle content (Sunchemical Suntronic EMD5603); and poly(-4-vinylphenol) (PVP) with poly(melamine-co-formaldehyde) methylated (crosslinker) was used as insulator. The characterization structures were printed on a flexible DIN-A4 size PEN substrate (DuPont Teijin Teonex® Q65FA). Using our setup, the measured average diameter of the silver ink drop was found to be 52 μm on top of PEN substrate, and 34 μm on top of insulator layer as shown in Figure 2.17b and c. Because of the drain and source are printed onto insulator, the layer beneath the electrodes used for their characterization is the c-PVP.

A first experiment was performed to optimize the printed lines behaviour. The independent variables used in this experiment are drop space and jetting frequency. The substrate is heated at intermediate temperature (40 ºC) and drop space varies from 5 to 40 μm center-to-center. Higher drop spaces were discarded for our silver nanoparticle ink, making no sense to use drop space bigger than the drop diameter.

A few principal behaviours emerge when examining printed silver patterns across a variety of drop spaces and delay periods. A name for these behaviours was introduced by Soltman et al. [78] as isolated drops, scalloped line, uniform line, bulging line, and stacked coins. Figure 2.18a to Figure 2.18d shows these four basic morphologies.

At low drop spacing (DS), an overflowing irregular bead forms and, isolated drops land at large DS. Finally, the minimum drop-on-demand delay is about 1 ms (1 kHz) on our printer. Delays from 100 μs to 1 ms are appended; longer delays become problematic because the ink has sufficient time to form a film skin at the nozzle. Once printed, the resulting patterns are

measured and quantified with a mechanical stylus profilometer and by means of confocal and interferometric microscopy techniques (Sensofar PLu neox).

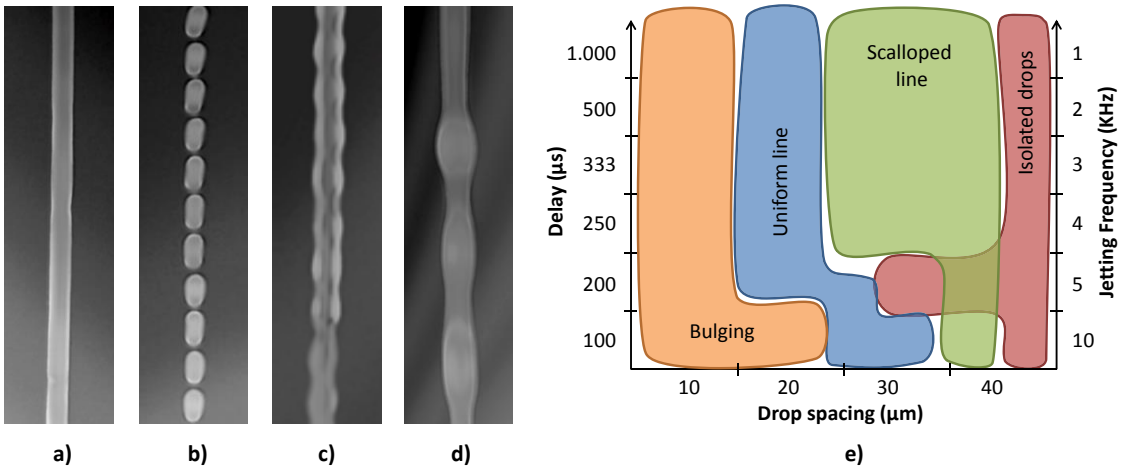


Figure 2.18. Examples of principal printed line behaviors: a) uniform line; b) isolated drops; c) scalloped; d) bulging; and e) typical printed line behavior at intermediate temperature with DS increasing from left to right.

Figure 2.18e schematically shows where each of these behaviours arises on specific drop space and delay at an intermediate temperature. A smooth, narrow and uniform line is achieved for drop spaces no upper than ratio drop diameter or lower than half of ratio drop diameter. For the cases of equal drop space than drop diameter, the line edges are ridged following the boundary of the drop giving a scalloped profile. If the drop space is even higher, isolated drops appears since there is not overlapping among the drops regardless of the delay. For the case of large overlapping i.e. less than half of drop diameter, bulges along the lines arise due to the excess of ink volume per unit of printed area. At a given DS, the line behavior is not strongly affected by delays longer than 250 µs. For shorter delays, uniform line is obtained varying the drop space from 20 µm to 30 µm.

By using those parameter values to obtain uniform lines (drop space of 20 µm and delay of 200 µs) a second experiment was performed focusing on an alternative group of parameters to optimize the homogeneity and cross section. The independent variables used in this experiment were the substrate temperature, drop lattice, and printing orientation. As design degree of freedom, patterns were printed both in printing direction (PD) and counter printing direction (CPD).

The different drop lattice patterns change the percentage of droplets for a given line. This will generate different physical structures that will be characterized in order to improve of film homogeneity.

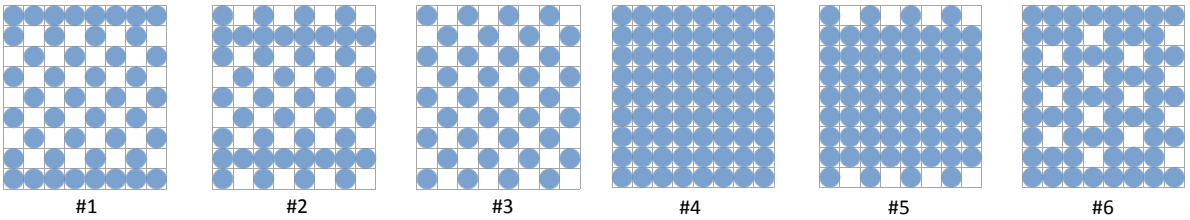


Figure 2.19. Different drop lattice evaluated. Images represent a portion of a horizontal line.

The pattern characterization structures are divided into a set of lines with different pixel lattices as detailed in Figure 2.19. Pattern structures are printed using substrate temperatures ranging from 20 ºC up to 60 ºC and changing the printing direction. Dot density is directly related with the material usage and of course with the corresponding physical properties of the films printed for the given lines.

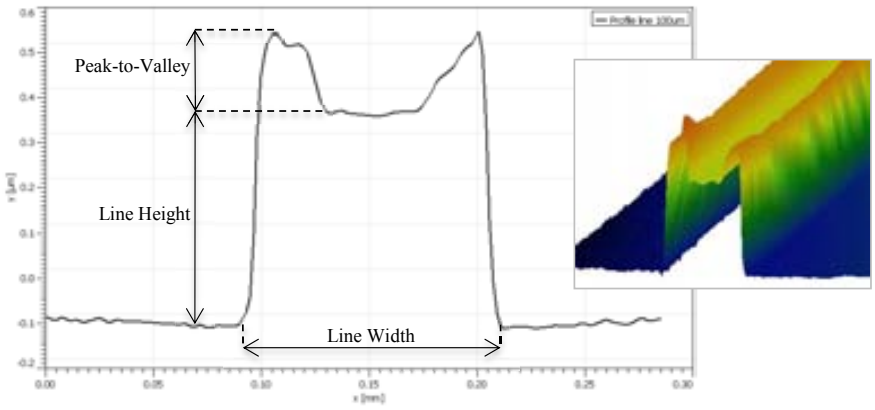


Figure 2.20. 3D and sectional image of a drop and bead parameters defined.

The device characterization methodology defines some qualitative analyses labelled as (1) line width, (2) line height, (3) peak-to-valley coffee ring verse height ratio and (4) line uniformity as is shown in Figure 2.20. Even though the line uniformity was assessed by means of drop space and delay, different drop lattices can produce non-homogeneity layers, in terms of profile, due to the variations of the pixels density and then, the amount of deposited ink per unit area. This is important not only for the intrinsic layer properties but also for the formation of other layers above this one.

The purpose of the printing experiments was to measure the named parameters for different drop lattices, substrate temperatures and printing directions taking cross-sections near the ends and several at the center for each line. Our strategy is based on comparing and seeking the optimal parameters of each cross-section that leads to a squared profile.

Figure 2.21a shows the dependency of line width for each pattern according to the substrate temperature and printing orientation. Taking into account example lines, the expected width

of the printed line was 200 µm as calculated by using Equation 2.2. As depicted in Figure 2.21b, similar to line width, as increase in height is shown owing to merging of the beads deposited. Consequently, the height is maximized for the 100% solid line pattern (4) in both printing orientations at 60 ºC.

The patterns (4) and (5) fit fairly to the desired width. Obviously an increase in line width is observed when the pattern becomes denser, resulting more material deposited per unit area. However, the wider line appears for pattern (6) instead (4). In the same way, the lines printed along the printing direction present larger widths than CPD one due to different printing delays. Nevertheless, pattern (4) shows a closer width in both printing orientations at 40 ºC.

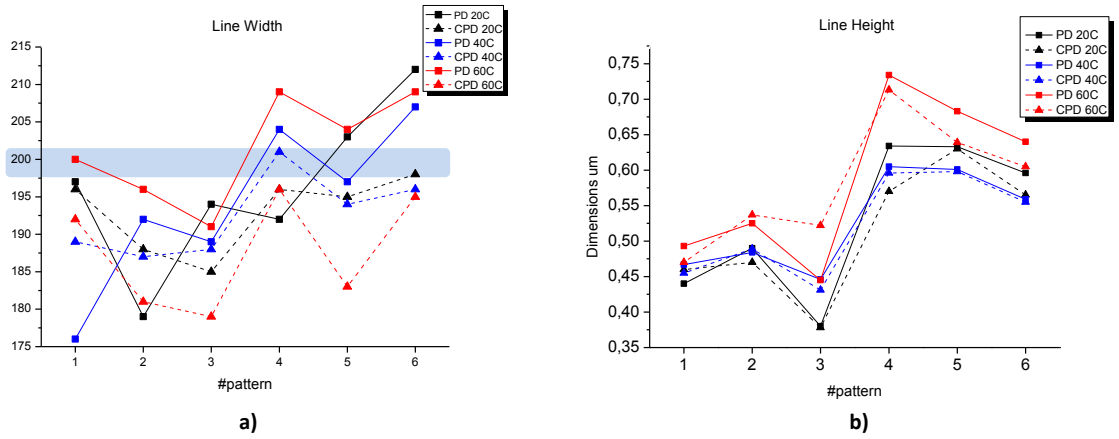


Figure 2.21. Measured a) line width, and b) line height.

Concerning the Soltman et al. work [78], the coffee ring at the feature's edge occur more strongly in a circular drop than in a straight line because of the greater ratio of edge length to center area in the drop. These effect leads to the characterization both drops and lines.

The morphology of the coffee ring on the patterns, i.e. the ratio peak-to-valley versus height, is assessed considering temperature substrate and printing orientation as shown in Figure 2.22. The zero values (illustrated as blue boxes) mean shapes close to a square profile (without coffee ring). Positive values mean a convex profile and negative means concave profile in the line, as shown in left and right inset figures respectively.

Strikingly as the substrate temperature increases, the coffee ring effect is not enhanced. Besides, the coffee ring arises in dense patterns such as (4) and (5) occurring exclusively to CPD lines. Therefore there exists a strong dependence on the printing orientation. The printing direction patterns (4) and (5) at 40 ºC have square profiles close to the desired ones.

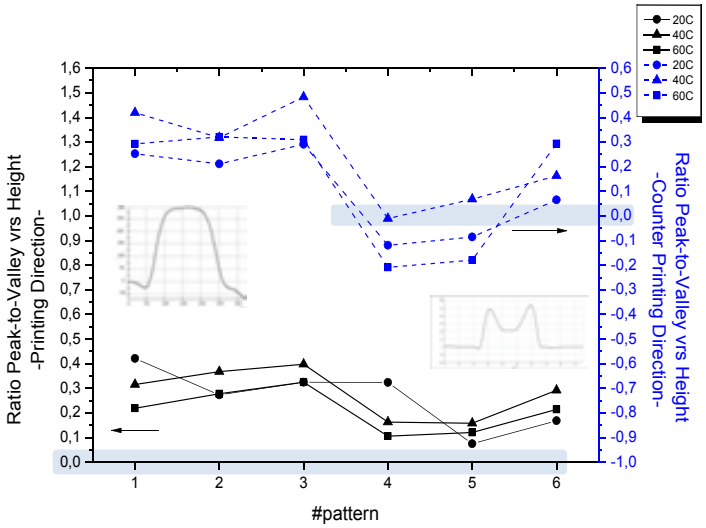


Figure 2.22. Measured ratio peak-to-valley *vs* height

The line uniformity related to the different drop lattices was investigated by means of ridge width [74], Figure 2.23a. The ridge width of scalloped pattern is defined as variation distance of individual rounded contact lines [78].

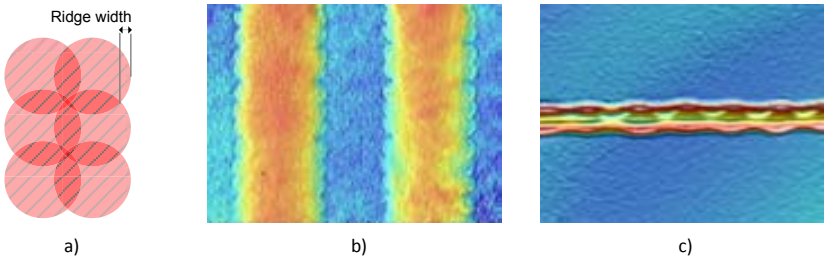


Figure 2.23. Ridge width effect of scalloped lines.

Table 2.1 shows the ridge width depending on the pattern, printing orientation and substrate temperature. Data listed is an average of all performed measurements. The value 0 means straight line without ridge (marked grey).

The experimental results show that the influence of the scalloped phenomenon is stronger for CPD lines than PD lines. As the temperature substrate increase, the instability is slightly enhanced for patterns (2) and (3), which have 50% solid outer line. No ridge occurs for patterns (1) and (6), formed at 40 ºC. Taking a glance of the results, at 40 ºC, the ridge effect is rather light.

Finally, considering (1) line width, (2) line height, (3) ratio peak-to-valley vs. height and (4) line uniformity for different patterns and substrate temperatures, one can conclude that the best printing condition for the silver nanoparticle ink printed on PEN substrate is the

pattern (4) at 40ºC in PD orientation with drop space of 20 μm and jetting frequency of 5 kHz.

Table 2.1. Ridge width (μm) measurement

# pattern	20ºC		40ºC		60ºC	
	CPD	PD	CPD	PD	CPD	PD
1	2.5	0.0	0.0	0.0	2.9	0.0
2	7.6	5.9	9.2	1.5	11.0	7.4
3	8.0	7.1	12.1	4.1	11.2	7.2
4	0.0	5.9	0.0	2.9	2.8	0.0
5	4.0	5.0	0.0	4.3	8.6	5.2
6	2.0	2.0	0.0	0.0	3.3	0.0

2.2.5. Compensation techniques for improving printed structures

For inkjet printed technology, the deposited pattern is deteriorated markedly due to ink coalescence leading to the need of using compensation techniques as is shown in Figure 2.24a. Coalescence of separately deposited drops can occur on some substrates. Drops can move or combine into larger drops creating an ink accumulation that can degrade the pattern fidelity [101][102]. The compensation techniques consist on modifying the pattern shape, e.g. pixels density to redistribute locally ink the density of in order to reduce the ink accumulation/lack at some places of the structure, transferring properly the desired pattern. As a consequence of the usage of compensation techniques, the device mismatches are much less affected by the process variability, increasing yield thus allowing a more aggressive scaling down. This is the second methodology step. An example of the concept is shown in Figure 2.24b.

Figure 2.24. a) Deteriorated printed pattern; and b) Application of a compensation technique.

The Pattern Shape Correction (PSC) is a compensation technique [103] based on Resolution Enhancement Techniques (RETs), especially on Optical Proximity effect Correction (OPC) from photolithography process in silicon technology.

An outstanding improvement of the width notch was obtained by applying compensation techniques which are based on incorporating either additive or subtractive PSC serif-type features to produce the desired shape as is shown in Figure 2.25b.

Although compensations can be applied to all pattern dots, the efforts are being focused on the junction of perpendicular lines as critical points.

By eliminating pixels at the inner and upper left corners as shown in Figure 2.25c, a further resolution and optimizing minimum notch rule is achieved as is shown in Figure 2.25d.

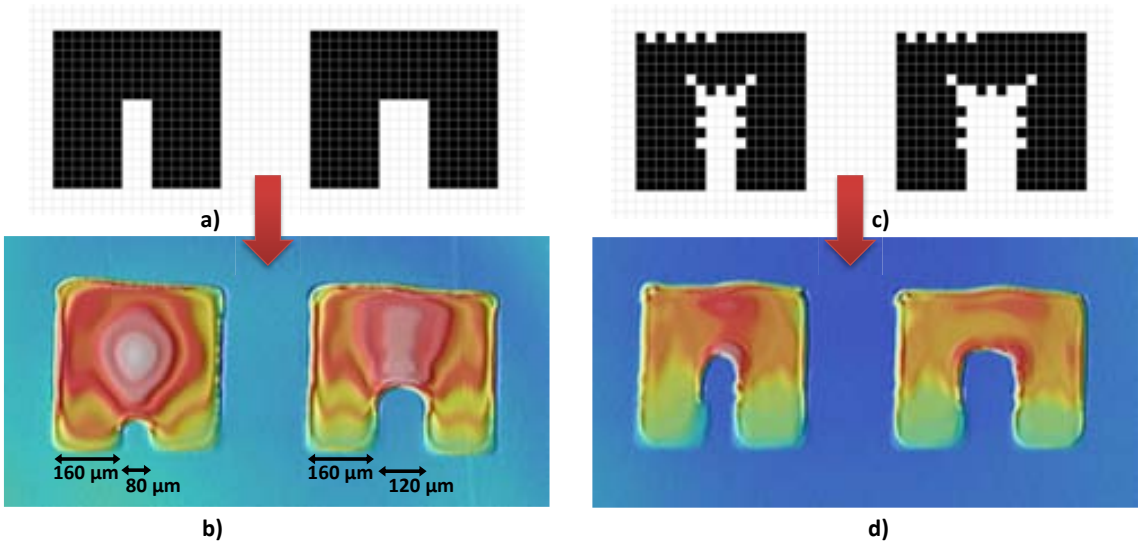


Figure 2.25. a) Non-compensated notch pattern; b) 3D image of the deposited non-compensated pattern; c) PSC Compensated notch pattern; and d) 3D image for PSC compensated notch rule.

Figure 2.26 shows additional examples of subtractive PSC serif-type features evaluated to improve minimum notch rule matching. Compensation feature shown in Figure 2.25c was found the best for our printer/ink/substrate set.

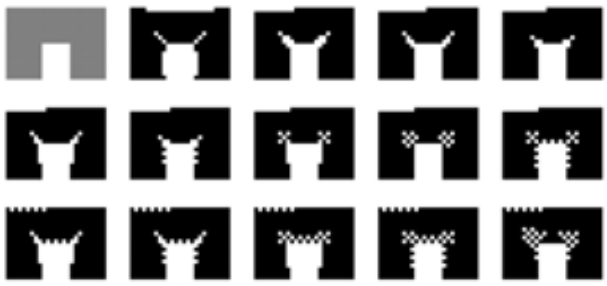


Figure 2.26. Different compensation strategies evaluated by taking out pixels locally.

2.3. Geometric design rule extraction

Although Geometric design rules can comprise a very large set of restrictions, they take into account two considerations: (1) reproducible geometrical patterns by a specific process and (2) the interaction among different layers.

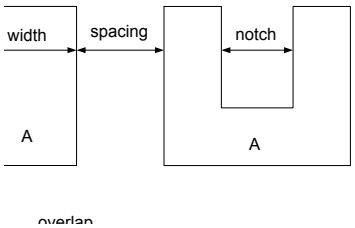


Figure 2.27. Definition of Basic Geometric Design Rules

In the Printed Electronics field is important to control the feature fidelity of the patterning to reproduce exactly the circuit layout that corresponds to electrical circuit parameters. By defining the optimal patterning, we can find out the design rules such as minimum width, spacing, notch and so on up to get the minimum feature size manufacturable allowed by the technology as shown in Figure 2.27.

2.3.1. Design Rules Characterization Structure

By carefully characterizing and understanding the conditions that lead to different printed line morphologies by means of pattern test structures, we will be able to find out the design rules of a particular ink. In this third methodology step, we introduce a set of pattern test structure useful for obtaining the physical limits resolution of the manufacturing process.

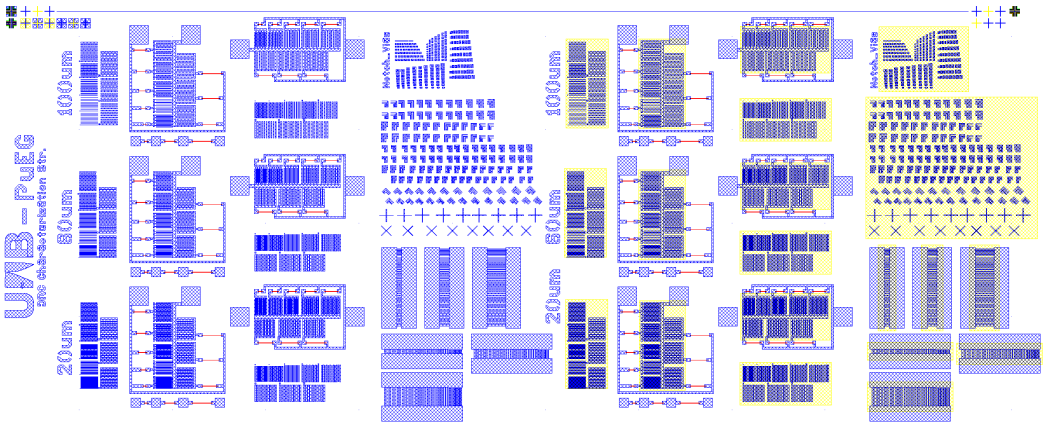


Figure 2.28. Layout of the test structure to characterize the conductive ink on substrate and on insulator. Note: yellow areas corresponds to insulator layers underneath.

As discussed before, the ink-substrate interaction affects the final line/area morphology. For this reason, and continuing with OTFT implementation, silver characterization structures need to be printed in both PEN substrate (since the gate is the first layer printed) and on top of the insulator layer (source and drain are bottom contacts). Left structure of Figure 2.28 includes the characterization structures directly printed onto the substrate; and right structure of Figure 2.28 on top of insulator layer previously deposited. The design is also shown in Annex C.1. As we can observe in Figure 2.17b and c, the morphology of lines strongly varies depending on the previous layer.

By means of the different pattern test structures included in the design of Figure 2.28, one can extract and characterize, by using optical and electrical instrumentation, the minimum design rules for any given material and technology. These characterization structures are discussed in the following sections.

2.3.1.1. Minimum width rule

The structure consists of a set of lines which line width progressively increases, whereas the spacing among them remains constant as shown in Figure 2.29a. The width of the first line is set to 40 µm and increase up to 600 µm. Moreover, spacing between lines needs to be enough to avoid merging.

By means of this pattern, one can obtain the value for the minimum width rule such that the line is sufficiently straight, smooth and without stacked coins, scalloped or bulging behaviours, as shown in Figure 2.29b. This rule gives us, for example, the minimum width such the drain and source electrodes have to be printed to ensure a good morphology onto insulator.

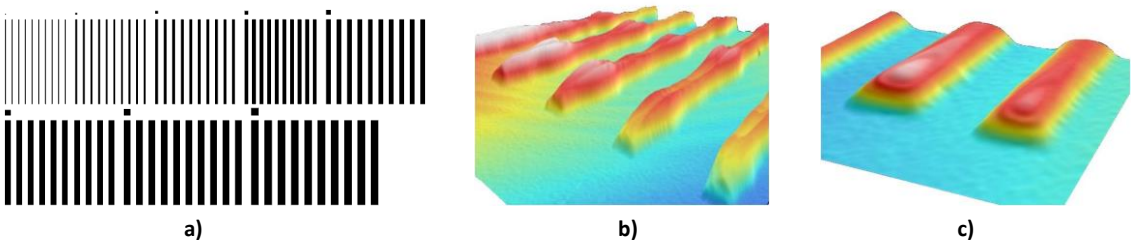


Figure 2.29. a) Characterization pattern for minimum width rule extraction; b) Non-homogeneous line behavior; and c) homogeneous line behavior.

2.3.1.2. Minimum spacing rule

The structure consists of a set of lines which the space width among them progressively increases, whereas its width remains constant.

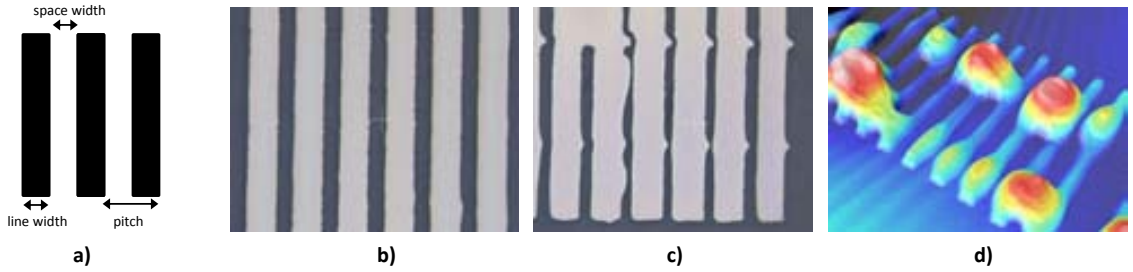


Figure 2.30. a) Diagram of a line and space pattern; b) Correct spacing; c) printer misalignment; and d) electrical shorts, minimum spacing violated.

This experiment needs to be repeated with additional sets of lines with different line widths, since minimum spacing depends also of the overflow caused by line width.

By means of this pattern, one can obtain the minimum spacing rule such that every possible line width is sufficiently separated avoiding merging with neighbour lines. Figure 2.30c shows a displacement error that might lead to short circuit as shown in Figure 2.30d. This rule gives us, for example, the minimum spacing such the drain and source electrodes of an OTFT have to be printed on top of the insulator for obtaining the best channel length (L) for any given finger width.

2.3.1.3. Minimum notch rule

The concept of minimum notch rule concerns to the structure of U-shaped open loop, shown in Figure 2.31 left. The structure consists on a set of U-shaped open loop which line width and notch progressively increase, Figure 2.31 left. As the notch spacing is not enough, ink coalescence will occur on top of the U-shaped (Figure 2.31 right), modifying the width of the upper track and consequently the length and section of the U-track.

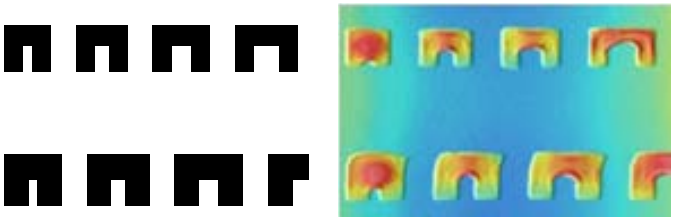


Figure 2.31. Left: Test pattern and; right: 3D image for minimum notch rule extraction.

The goal of this rule is to extract the minimum notch to avoid merging at the inner corners of bended lines. This is a typical rule used in e.g. snake resistors to reduce the area used by the resistive track.

2.3.1.4. Corner structures rule

Integrated circuits require the patterning of corners. Convex corners occur at the junction of lines for instance. Furthermore, an abrupt change of direction of a line has resolution limits owing to corner rounding among others non-desired effects [104].

The proposal of this pattern is to assess the convex corners by means of the common corner structure as shown in Figure 2.32a, increasing the spacing among them whereas the width lines are remained. Experimental results of this test structure will give us how the actual contour varies at the printed edge depending on orientation, e.g. Figure 2.32c and Figure 2.32d.

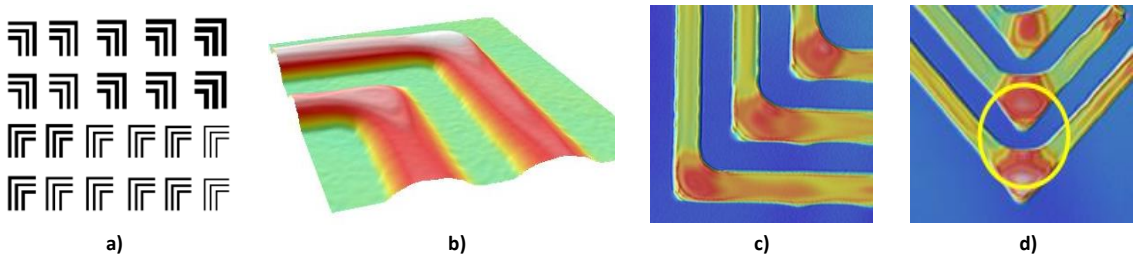


Figure 2.32. a) Test pattern; b) 3D image of corner patterns; c) corner pattern; and d) corner pattern rotated 45º.

By means of this test structure one can find out the optimal line width and spacing such that the ink was confined in right angle line junction without merging, Figure 2.32c and Figure 2.32d respectively. This rule will be used to assure that conductive tracks running in parallel will not be short-circuited when an orientation change occurs.

2.3.1.5. Junctions rule

Microelectronic circuits also require the patterning of junctions. Junctions occur when one line is connected to another perpendicular or to a bigger pattern (e.g. a connection pad). Furthermore, an abrupt change on the morphology can create strangled lines with sections different than expected. Figure 2.33a left shows the characterization structure and Figure 2.33c shows the compensation technique used to improve the junction of source and drain fingers to their pads. The test structure consists of a set of T-shaped lines which line width

progressively increases. The amount of ink entrained for T-shaped depends on the ratio of the line width; for higher ratios, more ink is entrained.

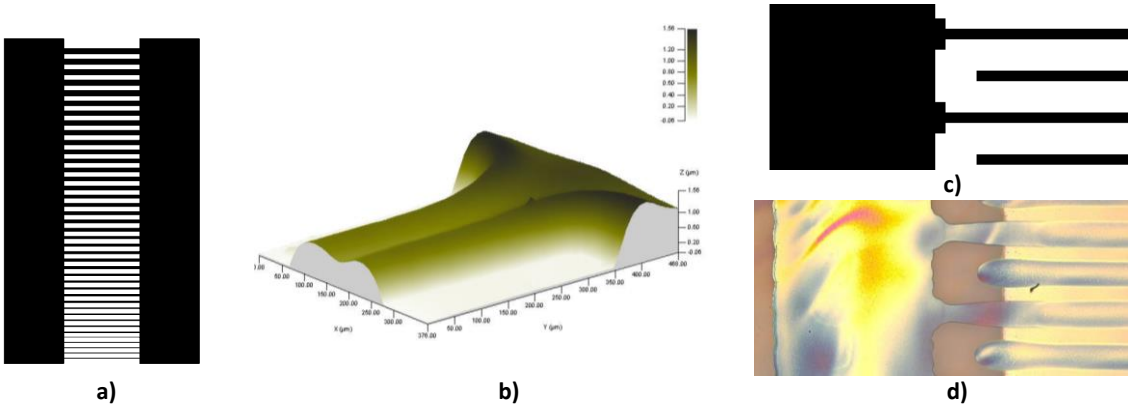


Figure 2.33. a) Test pattern for junction characterization; b) 3D image of junction; c) layout of Source and Drain electrodes with additive PSC serif-type feature to improve junction; and d) image of printed layout with strangled lines although the compensation applied.

2.3.2. Automation of Design Rule Extraction

The characterization of pattern structures to extract Design Rules is a tedious work due to the large quantity of structures to be characterized. Optical, confocal, interferometry or mechanical profilometry techniques are powerful tools but slow in use.

Alternatively, we can use structures that can be characterized by electrical measurements instead of optical metrology techniques. Figure 2.34 shows an interdigitated array of electrodes with a constant spacing among them and which finger width progressively increases. It will allow the characterization of the minimum spacing rule for any given line width. If we repeat the structures varying the line spacing, we will obtain the minimum spacing rule for every line width allowed in our technology.

The characterization structure is formed by an interdigitated array of electrodes where finger width increases. When fingers are not sufficiently separated to avoid merging with neighbour lines a short-circuit current will flow. To identify the set of fingers (related to finger width) not sufficiently separated, a circuit using scaled resistor was used to detect the short-circuit position through current measurement. With only two-point current measurement a large quantity of fingers sets can be analysed though the decomposition of the value of the fixed resistors related to each group of interdigitated array of fingers.

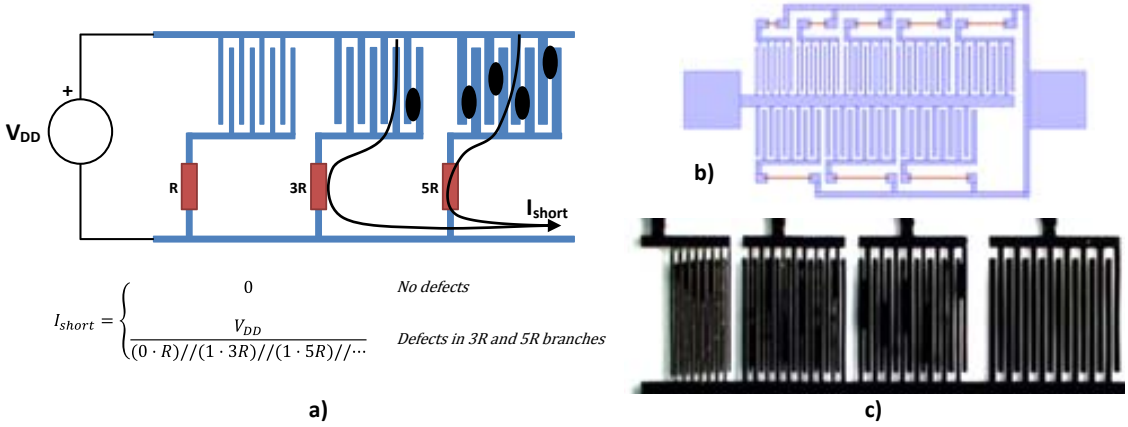


Figure 2.34. a) Electrical circuit of characterization pattern; b) layout of characterization pattern; and c) printed characterization structure over c-PVP with shorts in smaller spacings.

In the characterization structure shown in Figure 2.34, we have characterized groups of interdigitated arrays of electrodes (every one containing at least 10 fingers) with widths ranging from 40 µm to 200 µm, and spacings of 20, 60 and 100 µm directly printed on PEN and on top of insulator layer. Different structures were included to characterize lines printed in the printing direction and in counter printing direction. The electrical characterization of these structures gave us a preliminary minimum spacing rule as summarized in the following table.

Table 2.2. Example of spacing rule.

Line spacing	**20µm**		**60µm**		**100µm**	
Maximum line width allowed [µm]	**PD**	**CPD**	**PD**	**CPD**	**PD**	**CPD**
Ag on substrate	*no*	*no*	100	80	*all*	*all*
Ag on insulator	40	*no*	180	140	*all*	*all*

Measurements were corroborated visually by means of optical microscopy and other techniques.

2.4. Test mask for pattern and overlay parameters in inkjet printing

The simplest way to evaluate a process step is to create a test mask which directly measures the process parameters. Testing on both the horizontal and vertical axes (and on diagonals if it will be used) can identify directional process bias which needs to be addressed.

There are a large variety of test and alignment marks used in the literature [105]. In this work, the designed alignment and test marks are shown in Figure 2.35. The marks should be large enough for the inkjet equipment, and the gap between the box in square and cross in squares should be on the order of the minimum printing spacing defined by design rules.

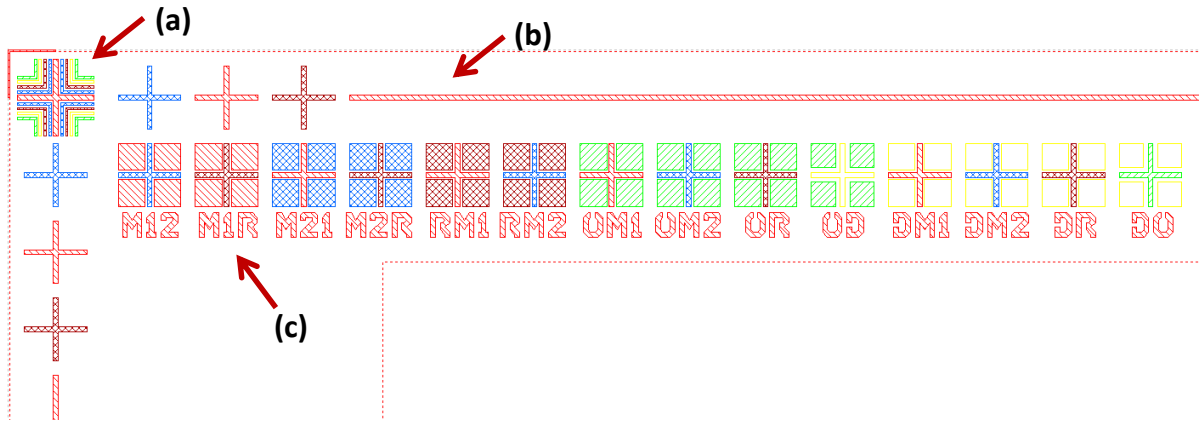


Figure 2.35. Test and alignment mask designed.

The four layers shown in Figure 2.35 are the metal1 (labelled as M1), metal2 (labelled as M2), dielectric (labelled as D), semiconductor (labelled as O) and resistive (labelled as R).

It is generally preferable to print all of the alignment marks on the first layer and then align all of the other layers to this first layer. This prevents additive errors from accumulating in the device stack. In some cases some layers maybe difficult to be observed (e.g. if dielectric, semiconductor or another transparent or semi-transparent layer is being patterned). The base pattern is printed with the metal1 layer and subsequent layers aligned to the base pattern.

Annex C.2 shows the designed base layout used in the experiments done in the current work.

2.4.1. Alignment marks for inkjet printing

Some marks are required for inkjet printing. E.g. mark labelled (a) in the layout of Figure 2.35 is used to align each layer deposited consecutively. The fiducial alignment system of the inkjet printer requires a clear and simple alignment mark. The gap between different layers needs to be accurately designed based on the design rules extracted previously.

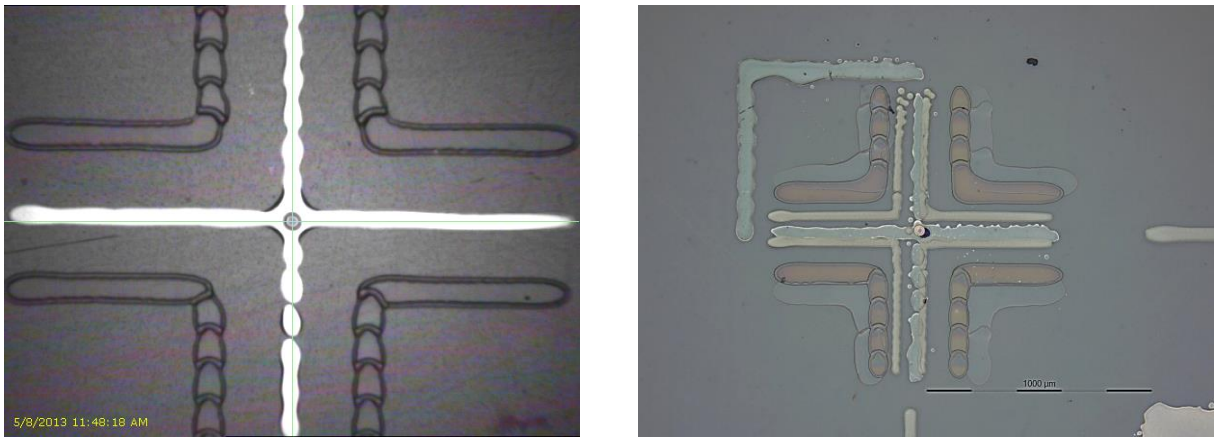


Figure 2.36. Alignment marks a) between metal1 and dielectric and b) between all the layers: metal1, dielectric, metal 2 and OSC.

Figure 2.36a shows an alignment mark as it can be observed in the fiducial camera of the DMP2831 inkjet printer. The white layer is metal1 composed by silver after curing. The dark (semi-transparent layer) is c-PVP dielectric after deposition. Figure 2.36b shows the alignment mark after four layers deposited (metal1, metal2, dielectric and semiconductor). The point in the middle of both crosses is the alignment point used as reference by the alignment software.

Additionally, the angular offset error produced when a substrate is removed from the platen and placed again need to be compensated. To compensate this offset, single crosses are placed at left and right sides of the printed layout. These crosses, labelled (b) in Figure 2.35, are connected by a solid line. The fiducial camera starts with the left cross of the pattern (metal1) and then moves to the right cross following the solid lines to help cross location.

2.4.2. Test mask for pattern and overlay parameters

The crosses and squares labelled (c) in Figure 2.35 are used to directly measure the process parameters. Marks should be large enough for the inkjet printing equipment, and the gap between the box in square and cross in squares should be in the order of the minimum spacing allowable between two consecutive layers. If the two layers are perfectly aligned then same separation in all directions will be kept. By measuring the relative offset of multiple structures with a known distance will help us to improve device alignment and to obtain proper design rules.

Figure 2.37 shows some images by optical microscopy of test masks involving different layers in the stack.

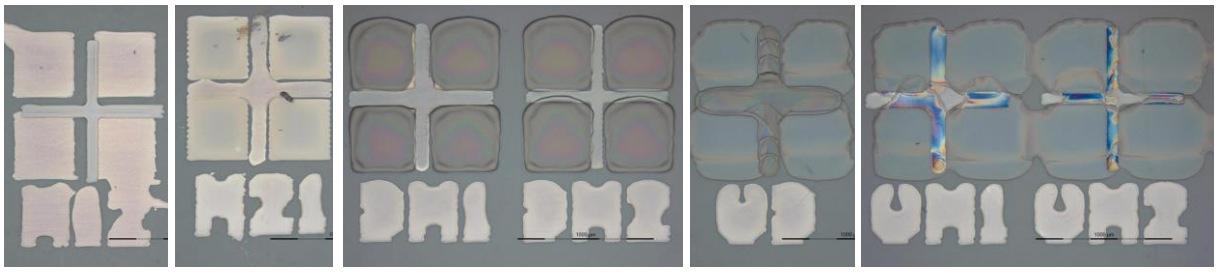


Figure 2.37. Test masks involving different layers: a) and b) metal1 to metal2; c) dielectric to metal1 and metal2; d) dielectric to OSC and e) OSC to metal1 and metal2 (Note: Bar scale = 1 mm).

Misalignment of some materials is difficult to measure due to ink coalescence and spread. E.g. dielectric and OSC inks deposition is not well patterned as shown in Figure 2.37c, Figure 2.37d and Figure 2.37e. Misalignment between metal1, metal2 and dielectric is more critical and it must be measured using the test masks printed in layout designs. By using these test masks, we can extract the misalignment between metal1 and metal2, as shown in Table 2.3. The misalignments were measured in 20 foils printed with similar conditions during several months.

Table 2.3. Misalignment in both directions between metal layers

Misalignment measured	Top left corner [µm]	Bottom right corner [µm]	Deviation between corners [µm]
Metal1 to metal2 vertical	20.16 ± 19.34	34.40 ± 20.08	33.85 ± 24.19
Metal1 to metal2 horizontal	17.04 ± 14.84	38.75 ± 25.80	41.67 ± 46.44

Results shows that the misalignment between metal1 and metal2 layers (corresponding to the first and third layers printed) in the top left corner can be up to 40 µm in both directions. This misalignment is mainly due to the intrinsic alignment error of the printer as reported in the printer specifications (±25 µm). The misalignment in the bottom right corner is larger than in the top left corner of the same foils. This means that an additional misalignment is generated by the deviation between both corners. As shown in the right column of the Table 2.3, this deviation is due to the substrate stretch after two curing processes (metal1 and dielectric). Thermal stress results in a shrink of the substrate and therefore the related additional misalignment. Nevertheless, printer software has the capability to compensate the thermal stretch after proper characterization.

Misalignments between different layers need to be properly taken in account in the definition of design rules.

2.5. Summary and conclusions

We have discussed the extraction and characterization of geometric design rules and the application of compensation techniques for inkjet manufacturing of reliable and precise designs based on the knowledge inherited from the well-developed silicon microelectronics technology.

Our work is focused on the enhancement of the OTFT structure[13] from a morphological point of view to improve device performance, process reproducibility, and increasing yield thus allowing a more aggressive scaling down and higher integration density. As above discussed, line morphology is key factor. Our contribution is a clear methodology to characterize the materials individually onto different substrates/layers to obtain optimal morphologies, for example, to source and drain electrodes.

A part from the inkjet printing parameters widely used as temperature, jetting frequency or DS, we have used the modification of the drop lattice as a novel parameter. Before the extraction of the technology design rules, a methodology to apply compensation techniques has been proposed. A set of compensation structures has been provided to obtain minimum dimensions and improve shapes such as junctions and corners markedly deteriorated due to ink coalescence. Finally, we have introduced an automated solution for the extraction of design rule with electrical measurements and we proposed test masks for alignment characterization.

[13] **BG-BC:** Bottom gate bottom - contact architecture.

3. DEVELOPMENT OF ELEMENTARY DEVICES

Whereas the focus of previous chapters was set on inkjet printing technology specification and process characterization, the main emphasis of the current chapter is on the fabrication of elementary devices for sheet-fed process.

The printability of ink formulations for conductors, resistive and dielectrics is investigated. We characterized the deposited layers concerning functional and morphological properties. Also, the compatibility of selected materials for its use in resistors and capacitors is investigated. The printed films and devices are characterized concerning relevant parameters. Emphasis is on device characterization to analyse its stability, scalability and variability in order to obtain suitable devices for market applications.

Resistors and capacitors using different techniques and materials are fabricated and characterized as well as RC filter circuits to demonstrate its feasibility and maturity. From a processing viewpoint, the procedures described here are attractive because it does not require high temperatures, low pressures, and masks, therefore providing a very low-cost approach to fabricate passive electrical components and simple circuits useful for the electronic industry: embedded passive filters in PCBs or for future use in wearable electronics among other examples. E.g. Future wearable electronic circuits require flexible devices which can be printed at a sufficiently low temperature (<150 °C) to avoid damage to the fabric substrate.

In the literature, there have been a number of approaches to passive devices fabrication using inkjet printing. Some approaches use additional fabrication methods other than inkjet printing, are based on rigid substrates or require high temperature processing which is too high for most substrates. All the devices presented here are fully inkjet.

3.1. Conductive lines

Conductive lines are an important part of electronic circuits as they interconnect devices and systems. Indeed the electrodes of devices are usually made by conductive materials.

Currently, different organic and inorganic materials are suitable to be used as conductors [106]. Nevertheless, the low conductivity of organic materials (~10^2 S/cm) is still far from the requirements for e.g. interconnecting circuits. Thus, in this thesis work, organic conductors will be used as resistive layers and inorganic/metallic nanomaterials as conductive layers.

Inorganic/metallic inks are composed of a combination of nanomaterials, solvents and binders in a given proportion. Solvents start evaporation when ink is jetted and contacts substrate. Inorganic particles deposited have a thin layer of binders (an encapsulant product) helping melting during low-temperature curing process. Low curing temperatures do not create a strong inter-metallic melt, thus binders acts as a conductive adhesive creating a particle melting with a strong union [107] as it is shown in Figure 3.1a.

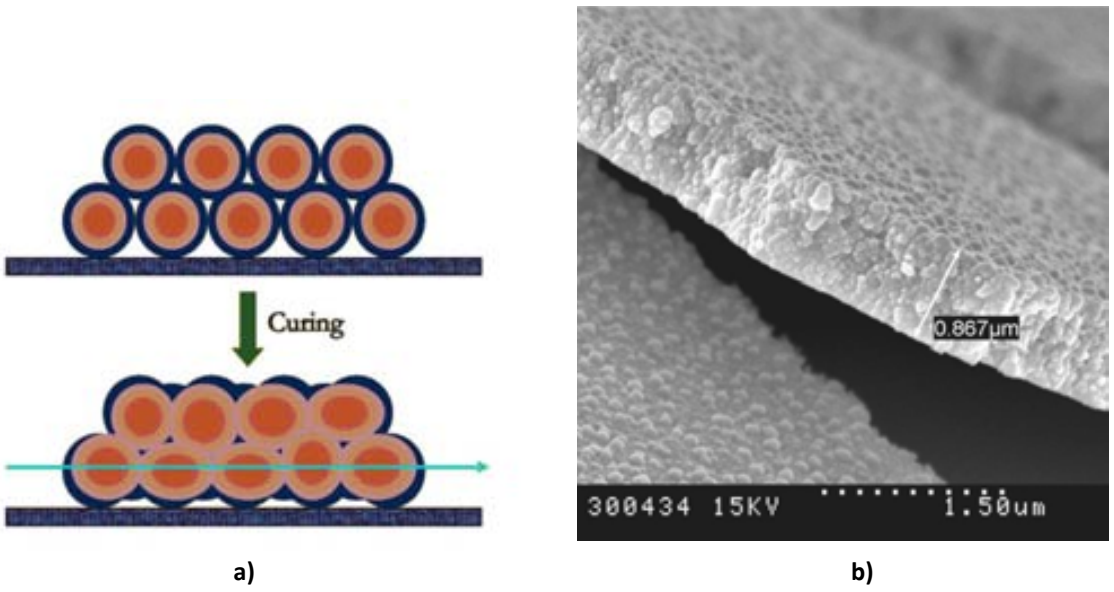


Figure 3.1. a) Ink curing process[14]; and b) SEM image of a thin film using silver nanoparticle ink.

The ink used as a metallic conductor is Sunchemical's Silver ink EMD5603 (commercially known as Suntronic Jettable Silver)[15]. This ink is a silver nanoparticle solution for inkjet printing systems having a 20% of weight of silver particles and a volume resistivity between 5-30 μΩ·cm after curing at 150-300°C, as reported in the manufacturer datasheet. Its surface tension makes it perfect to print using inkjet technique over paper, polymer, glass and other flexible and rigid substrates.

[14] Source: VTT Finland.
[15] This ink has been discontinued by Sunchemical after October 2013.

Silver nanoparticle ink is pre-filtered with a nylon 0.45 µm filter to avoid nozzle obstruction due to silver particles sedimentation, as recommended by Sunchemical. Cartridge works at room temperature and several nozzles with 20-28V activation voltages and 20 µm drop spacing were used for the inkjet printing.

Figure 3.1b shows SEM images[16] of silver nanoparticle ink deposited on polyester based (PET) substrate 150 µm thick. Printed line was cut in order to broken silver surface and measure line thickness. Image shows the silver nanoparticles annealed and film thickness.

The objective of this section is to study the electrical characteristics of a metallic conductive ink as a function of printing, curing processes and substrates in order to use it in later devices as resistors, capacitors and transistors.

3.1.1. Morphological characterization

Figure 3.2a and Figure 3.2b shows the optical image and the cross-section of a printed line of silver nanoparticle ink on paper (*pe:smart paper* from Felix Schoeller) respectively. In Figure 3.2b it can be observed the high roughness of the paper substrate compared to the low roughness of the PEN substrate shown in Figure 3.3b. Nevertheless, printing on paper results in very homogeneous printed patterns thanks to the good absorption of ink on paper.

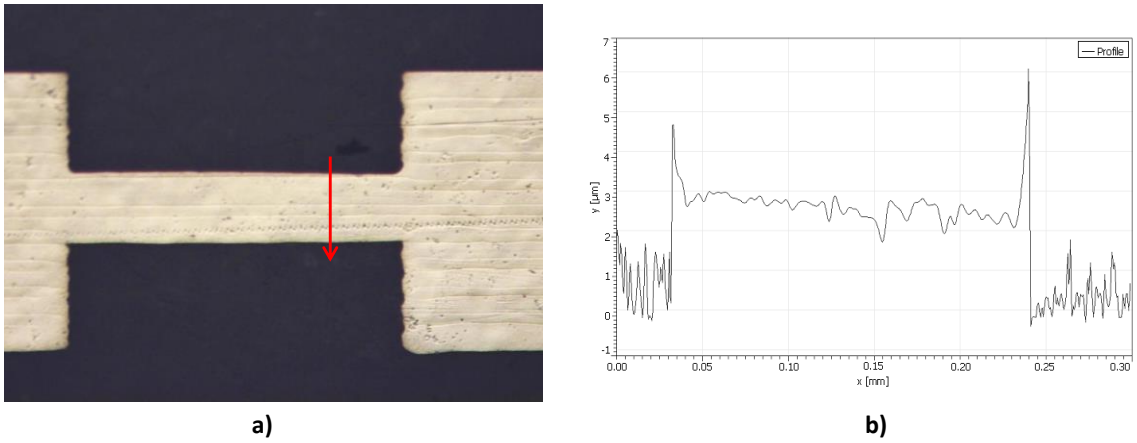


Figure 3.2. a) Optical image; and b) cross-section of a printed line of Ag nanoparticles on paper obtained by confocal. The average thickness of the silver line was 275 nm.

Figure 3.3 shows the optical image and the cross-section profile of a printed line of silver nanoparticle ink on DuPont Teijin Q65FA PEN substrate. Although PEN substrate is significantly more homogeneous compared with paper, the evaporation process is totally

[16] Scanning Electron Microscope from the Servei de Microscòpia at UAB.

different because of PEN is not absorbing the solvents of the ink, thus, the cross-section profile is totally different.

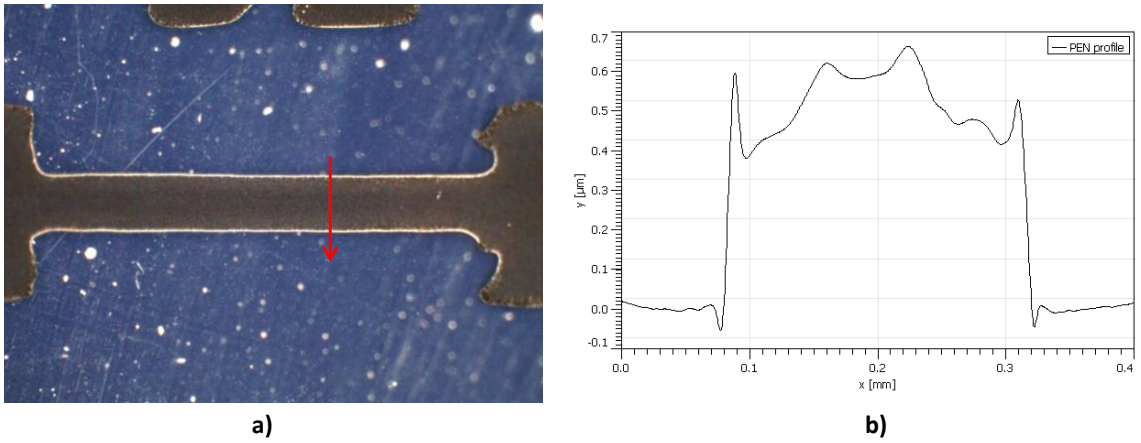


Figure 3.3. a) Optical picture; and b) cross-section of a printed line of Ag nanoparticles on PEN substrate obtained by confocal. The average thickness of the silver line was 450 nm.

The AFM analysis of the silver layer printed on a PEN foil shows the typical nanostructure of this material.

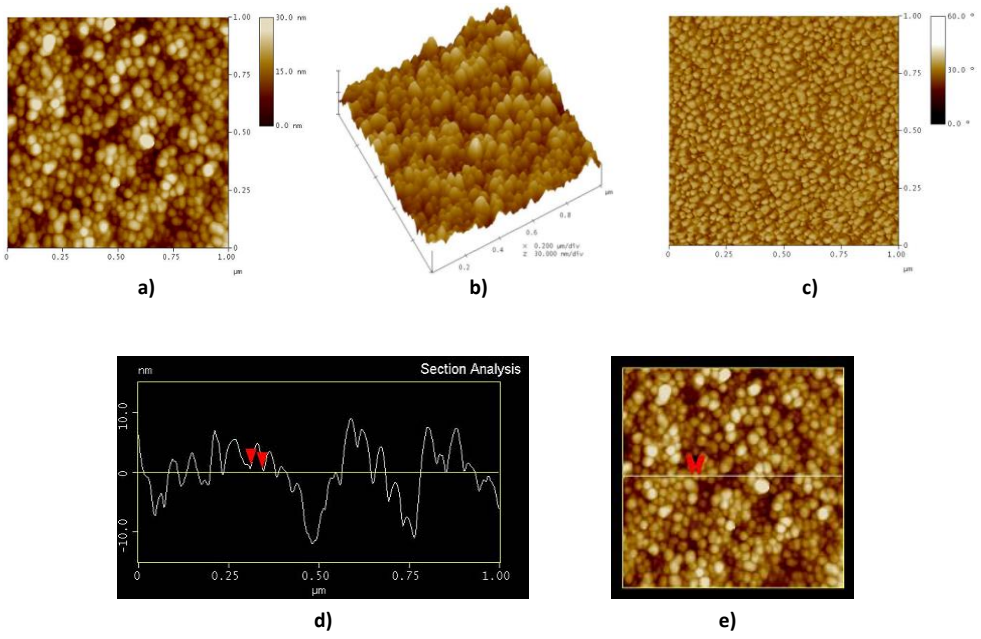


Figure 3.4. AFM images of silver bottom contact printed on Teonex PEN substrate: a) 2D-height; b) 3D-height; c) 2D-phase; d) and e) section analysis[17].

[17] Source: ENEA: Italian National Agency for New Technologies, Energy and Sustainable Economic Development.

Nanoparticles are uniformly distributed in the investigated area as it is possible to observe in both AFM height and phase images (Figure 3.4). The section analysis is used as a tool to further estimate the average dimension of the nanoparticles of around 20-35 nm. The root-mean-square roughness was evaluated equal to 5.2 nm.

3.1.2. Resistivity measurements

Different experiments were performed in order to study the effect of the printing and curing parameters on the final conductivity of the printed lines. Van der Pauw measurements were used to extract the given conductivity.

3.1.2.1. Van Der Pauw Resistivity Measurements

In typical resistivity measurements, four-point probe method leads to a rectangular sample along a straight line (Figure 3.5a). A current is biased from contact A to contact B, and the voltage is measured across contacts C and D, which must be far away from the current contacts in order to obtain a uniform and parallel current flow between C and D. The resistivity of the sample can be derived from the voltage drop across contacts C and D, the applied current, and the geometry of the sample.

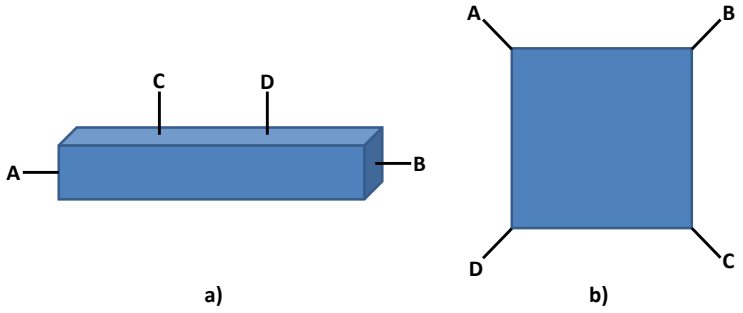


Figure 3.5. a) Conventional resistivity measurement; and b) typical van der Pauw measurement.

Frequently the inkjet printed patterns does not have a geometry that is favourable for the measurement of resistivity, leading to an unknown current distribution. Moreover, it is often difficult to determine accurately the geometry of the sample, limiting the accuracy of the calculated resistivity. In such a case the technique of van der Pauw is used to determine the resistivity of the sample [108]. A common geometry for such a measurement has four electrical contacts at the four corners of a roughly square sample, as shown in Figure 3.5b. However, the van der Pauw technique is applicable for an arbitrary shaped sample as long as the thickness of the sample is known and is uniform, the contact areas are small, and the

contacts are all on the perimeter of the sample. Thus, van der Pauw measurements require contacting the surface at the corners of the film which often causes wrong measurements since the position of the contacts is not precisely located. For this reason, in this work we will use an alternative structure named cloverleaf. This structure uses the same measurement process defined by van der Pauw but the contact position is not as demanding. Although the cloverleaf design will have the lowest error due to its smaller effective contact size, the fabrication is more difficult than a square or rectangle.

Figure 3.6 shows the cloverleaf structure printed on top of PEN and paper substrate, respectively.

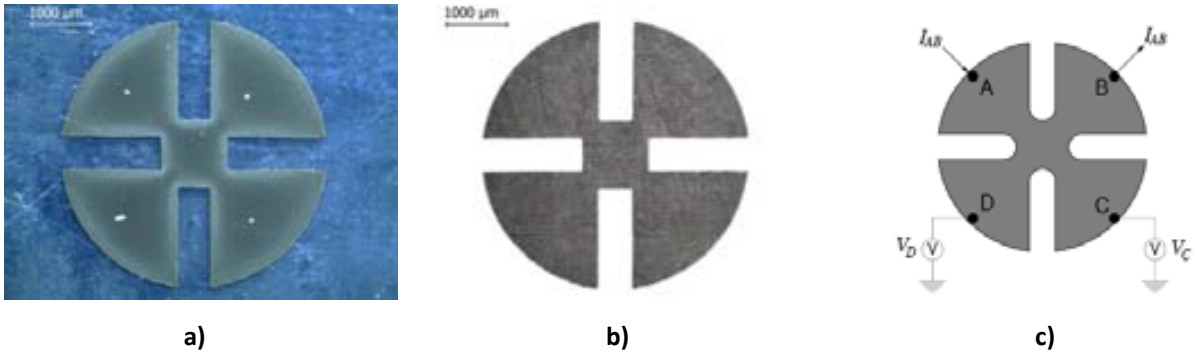


Figure 3.6. Cloverleaf structure printed by inkjet: a) on PEN substrate, b) on paper substrate, c) cloverleaf characterization setup.

3.1.2.2. Resistivity as a function of fabrication process parameters

This preliminary study reports the characterization of silver metal films and lines printed onto plastic and paper substrates by inkjet printing technology. The morphological characterization of inkjet printed films by SEM indicates that a sintering treatment at 250ºC, much lower than the bulk silver melting temperature (962 ºC), for 30 min fully sinterizes the silver metal nanoparticles, as already demonstrated in several publications [109][110].

In the first experiment, a range of curing times (15, 30 and 60 min) and temperatures (80, 100, 120, 140, 160, 180, 200, 250 and 300ºC) were used in order to measure sheet resistance of silver films on a PEN substrate. The results obtained are shown in Figure 3.7.

The curing temperature of 300ºC was not supported by the PEN substrate and thus discarded for further experiments. A temperature of 250ºC also stretched significantly the substrate and thus it is not recommended. The conditions of 30 minutes at 180 or 200ºC are the highest temperatures supported by PEN without any deformation.

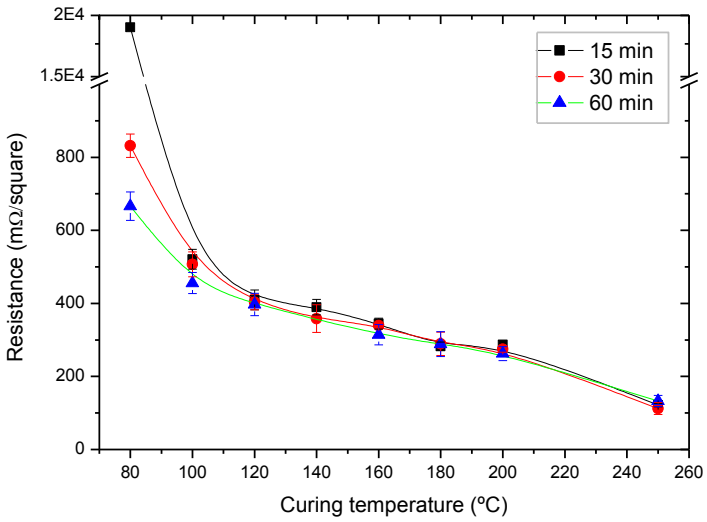


Figure 3.7. Sheet resistance of inkjet silver-based thin films on a PEN substrate as a function of temperature and curing time.

For a curing temperature of 80ºC during 15 min, the sheet resistance reaches up to 18.9 ohm/square. For temperatures higher than 120ºC, we can notice that the curing time does not affect the resistivity of the layer, and then the sheet resistance is basically lowered by the temperature increase.

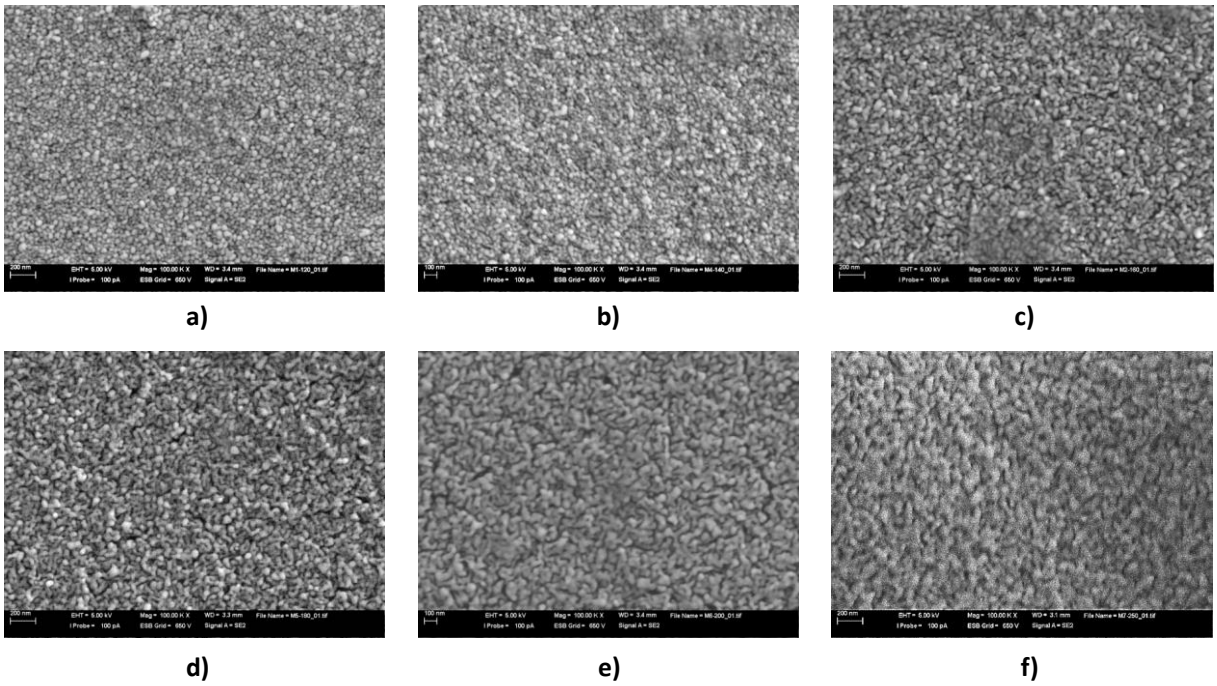


Figure 3.8. SEM plan view of: a) 120ºC, b) 140ºC, c) 160ºC, d) 180ºC, e) 200ºC and f) 250ºC for 30 min annealed samples.

Figure 3.8 shows the SEM images of six samples sintered at 120, 140, 160, 180, 200 and 250ºC for 30 min. It shows clearly the aggregation of the nanoparticles as the curing temperature increase.

As expected, the film resistivity decreases with curing temperature. In particular, at 250ºC the resistivity value, which almost reached a plateau, is about six times higher than the value of bulk Ag, i.e. $4.6 \cdot 10^{-6}\ \Omega \cdot$cm, and has a little dependence on annealing time.

The sheet resistance of the inkjet printed silver nanoparticle film on PEN and paper substrates as a function of curing time for a fixed curing temperature is shown in Figure 3.9. Conductive structures were printed with a drop spacing of 20 µm and sintered at 130ºC with a curing time between 5 and 60 minutes. In PEN substrate, the resistivity decreases exponentially with curing time, and based on the results shown in Figure 3.9a, after 30 min of curing the resistivity decrease is not significant. Additional curing time just reduces the resistivity in a 6%.

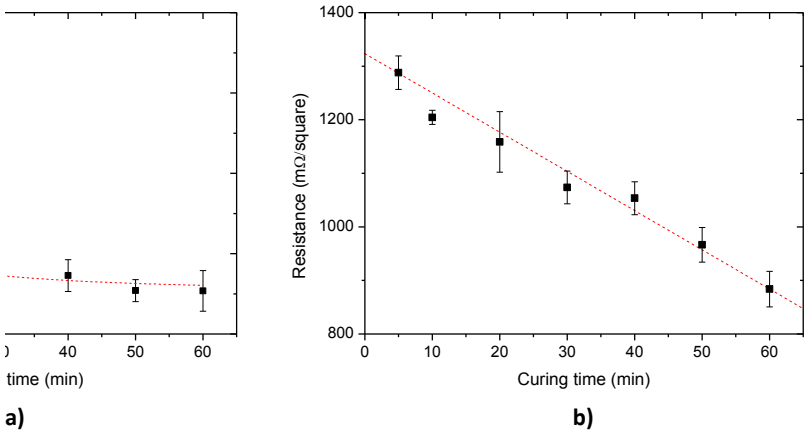


Figure 3.9. Sheet resistance of the inkjet printed silver nanoparticle film as a function of curing time: a) on PEN substrate; and b) on paper.

Although, a curing temperature higher than 120ºC does not increase significantly the conductance, a range of temperatures between 160°C and 200°C gives good values in terms of suitable conductivity. A lower melting point is a key factor as increases number of suitable substrates for printing. A low temperature is desired for paper, polyester (PET) and PEN substrates (that are the cheapest substrate materials considered).

In paper substrates, resistivity of the printed silver layer is between two and three times higher than in PEN substrate, as shown in Figure 3.9b. Main difference between these two substrates is due to their tendency in curing. For paper based substrates the sheet resistance decreases linearly with the curing temperature instead of exponentially as for PEN

substrate. The nature of this effect is elusive but it could be related with the migration of the material through the cellulose of the paper.

Figure 3.10 shows the SEM images of four samples sintered at 130ºC during 5, 10, 30 and 60 min. Unlike Figure 3.8, images do not show clearly the aggregation of the nanoparticles as the curing time increase. So, we can conclude that boundaries disappearance is mainly dependent on the temperature instead of curing time.

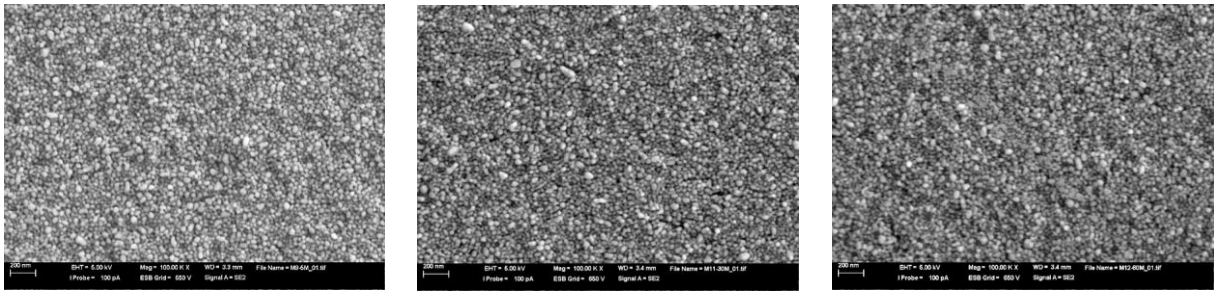


Figure 3.10. SEM plan view of 130ºC for: a) 5 min, b) 30 min, and c) 60 min annealed samples.

In order to extract silver ink conductivity as a function of linewidth, an array of lines was printed and measured. Lines were printed both horizontally (X direction) and vertically (Y direction) to avoid (or measure) direction-dependent printing effects. Lines were printed on a PET substrate with a single nozzle (20 µm drop spacing) and cured at 200°C during 30min. Line thickness was measured using a Nanofocus 3D confocal microscope with an average thickness measured of 280 nm, as shown in Figure 3.11.

Figure 3.12a shows the sheet resistance of the silver films as a function of the number of printed layers. Between one and four layers were printed with a drop spacing of 20 µm and sintered at 130ºC during 30 minutes.

The resistivity decreases linearly but not proportional to the number of layers. First additional layer reduces the layer resistivity in a 14.5% only. A reduction of 33.3% and 54.9% was achieved for three and four layers respectively. In the figure, both sheet resistance and film thickness are depicted showing a linear decrease (or increase) respectively, as expected.

The sheet resistance and the conductivity of the inkjet-printed silver nanoparticle line on PEN substrate as a function of its linewidth are shown in Figure 3.12b.

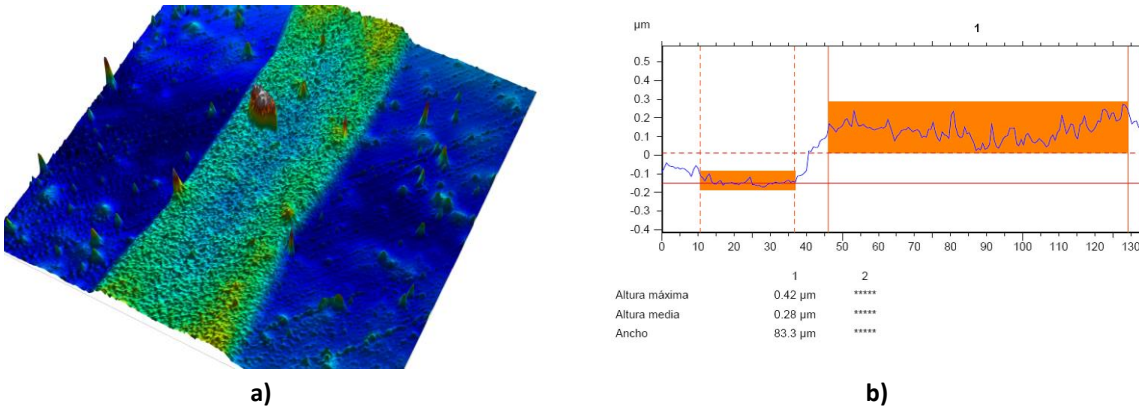


Figure 3.11. 3D confocal microscope measurements.

Conductivity starts to stabilize for widths larger than 125 µm. Narrower widths presents lower conductivities in a linear decrease.

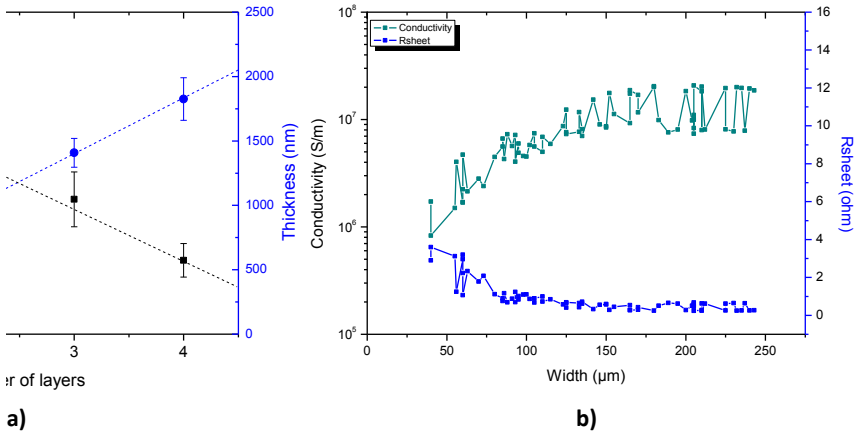


Figure 3.12. a) Resistivity and thickness of the inkjet printed silver nanoparticle film on PEN as a function of the number of printed layers; and b) Conductivity and $R_{\square}$ measured in a one-layer inkjet printed lines as a function of linewidth.

The average value measured for sheet resistance is 54 mΩ/□. Measured conductivity of 10^7 S/m is a good result as bulk silver theoretical conductivity is $6.3 \cdot 10^7$ (6.3 times higher than inkjet-printed lines). Nevertheless, $R_{\square}$ measured for narrower lines (~3-4 Ω/□) can be interesting in order to develop precise resistors using conductive inks although its repeatability cannot be sufficient to assure fixed tolerance as required in some applications (even for the case of parallel matched structures).

Finally, Figure 3.13 shows SEM images of narrower lines scanned and measured to illustrate the effects occurred during printing. Narrower lines are more sensitive to drop misalignments and ink coalescence, making not fully stable in terms of morphology as it

seems to be in a macroscopic level. The drop misalignments reduce as width increases, and a large number of drops form line shape producing differences of width around 20%.

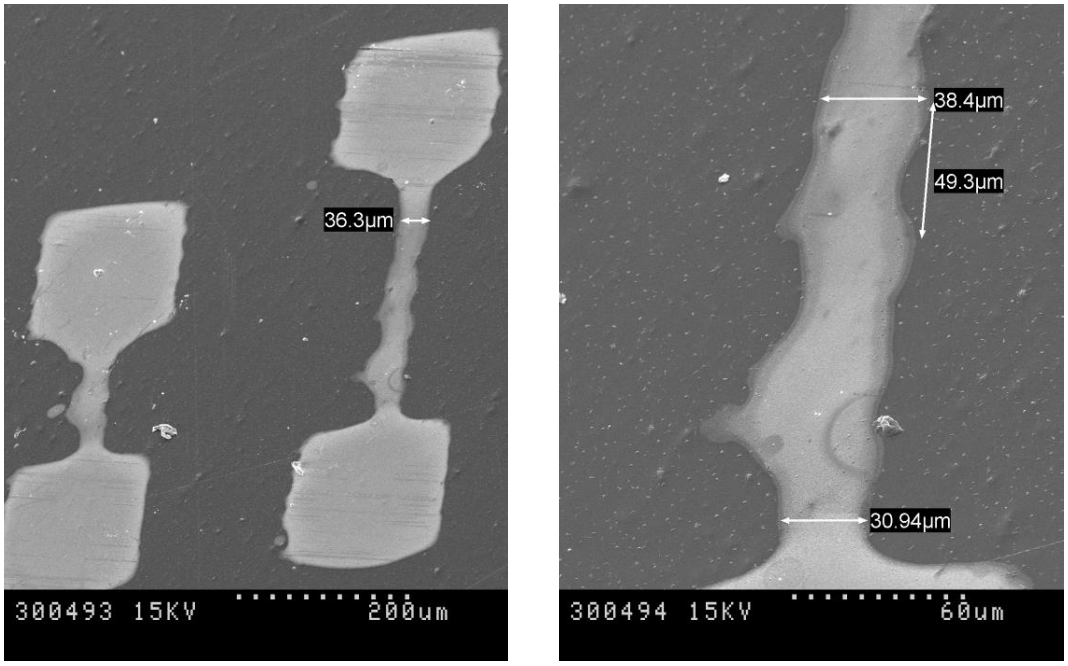


Figure 3.13. SEM images of silver nanoparticle ink printed structures.

3.2. Resistors

The most elementary of all devices is the resistor. It consists of a bar of resistive material that produces a voltage across its terminals by resisting the flow of charge through itself. It is a simple device and plays a critical role in many electronic systems. Usually, it contains a strip of homogeneous material with two conducting pads at their ends as shown in Figure 3.14.

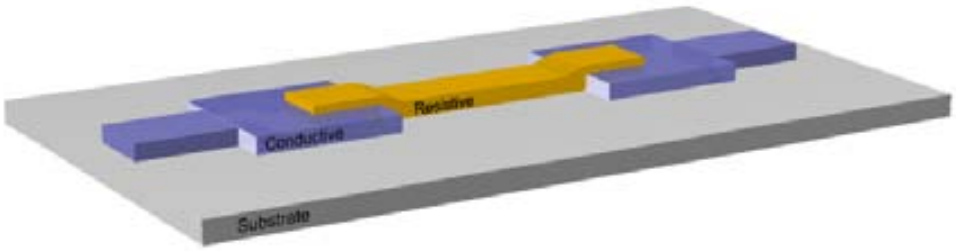


Figure 3.14. Typical deposited/printed resistor structure and geometry.

In this work, different resistor structures have been printed and tested in order to analyse their response and external effects [111]. In this experiment, a silver nanoparticle ink from Sunchemical has been used as contact pads, and different organic and inorganic inks as resistive materials.

3.2.1. Resistor characterization

The resistance indicates how well the device opposes to the electronic current flow and is a function of the resistivity of the material, and the geometrical parameters of the device: length, width and thickness, as shown in Equation 3.1.

$$R = \rho \cdot \frac{L}{S} = \rho \cdot \frac{L}{T \cdot W} = \frac{\rho}{T} \cdot \frac{L}{W} \qquad \textit{Eq. 3.1}$$

where R is the resistance of the linear resistor, ρ the resistivity of the bulk material, L the length, S the section, T the thickness and W the width of the resistive strip.

Last equation can be also converted to:

$$\left(\frac{\rho}{T}\right) \rightarrow sheet\ resistance\ \left(^{\Omega}/_{\square}\right) \rightarrow R_{\square} \qquad \textit{Eq. 3.2}$$

$$\left(\frac{L}{W}\right) \rightarrow \#\ of\ squares\ (\#_{\square}) \qquad \textit{Eq. 3.3}$$

$$R = R_{\square} \cdot \#_{\square} \qquad \textit{Eq. 3.4}$$

Nevertheless, to extract a correct sheet resistance we need to take in account the contact resistance which appears in the interface between the metallic pad and the resistive material. This contact resistance is proportional to the contact area between both materials and it can be calculated as shown in Equation 3.5.

$$R_c = \frac{\phi_c}{W_c \cdot L_c} + \rho_{conductive}\frac{L_c}{T \cdot W_c} + \rho_{resistive}\frac{L_c}{T \cdot W_c} \qquad \textit{Eq. 3.5}$$

Where ϕ_c is the gap between energy levels of both materials, and ρ is the resistivity of the conductive material (silver ink in our case) and resistive material. Nevertheless, in this work, the value of the contact resistance has been extracted experimentally.

Finally, the resistance of a two-terminal device as shown in Figure 3.14 can be calculated by the following equation:

$$R_{total} = R + 2 \cdot R_c \qquad \textit{Eq. 3.6}$$

Higher resistances can be achieved by using high-resistivity materials, increasing the length or using smaller cross-sections. All these factors will allow designing resistor devices with different structures, geometries and materials.

3.2.2. Inorganic resistors

In the previous section we concluded that low sintering conditions (reduced curing time and temperature) results in higher resistance per square values. Figure 3.7 reveals that a silver film cured during 15 min at 80ºC have a sheet resistance of 18.9 ohm/□. In conventional silicon processes, polysilicon is used as resistive material having values starting at 200-300 ohm/square up to some Kohm/□. Reducing the curing time and temperature of the silver strips we can reach values in the same range.

3.2.2.1. Fabrication process

Initially, resistor structures were printed using 10pL printheads and a drop spacing of 20 µm. Substrate used is a PEN film (DuPont Teijin Teonex Q65FA) pre-cleaned with ethanol.

As shown in Figure 3.15, the materials stack is:

- First, one layer of silver nanoparticle ink (Suntronic EMD5603 SunChemical Corp.) used for the contact pads was deposited using a platen temperature of 40°C and sintered at 130°C during 30 min.

- Second, an additional layer of silver ink as resistive layer deposited and sintered using different curing strategies.

Figure 3.15. Linear resistor structure and geometry.

The layout used is shown in Annex C.3. A reduced example of the patterns used is shown in the following figure:

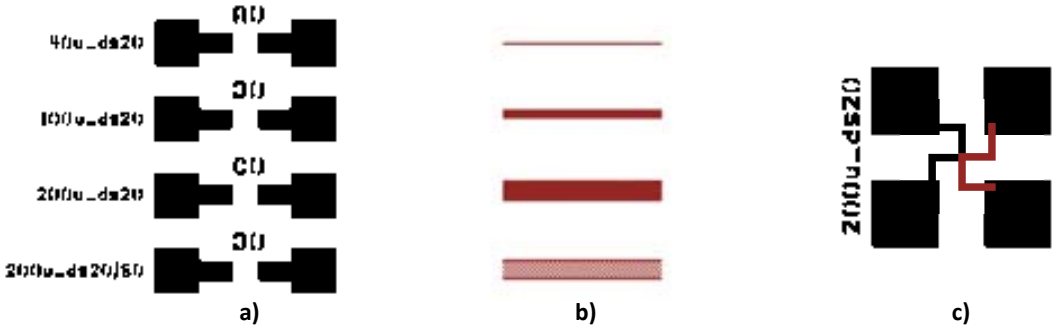


Figure 3.16. a) Metal1 layer; b) resistive material layer; and c) greek-cross structures. Note: layers are not in scale.

Figure 3.16a shows the contact pads, and Figure 3.16b shows the patterns of the resistors which were printed using a fixed length but different widths: 40, 100 and 200 µm. A fourth resistive strip using a 50% pattern and solid edges was also printed.

Figure 3.17a shows an image of printed resistor before curing second layer. The white/brilliant pads were printed and cured using normal settings: 130ºC during 30min. The resistive strip (dark colour) is not yet cured. Picture was taken using the fiducial camera embedded in the printer.

Moreover, greek crosses were added to the general layout in order to extract contact resistance, as shown in Figure 3.17b to Figure 3.17d.

Due to the misalignment problems, shown in Figure 3.17b, inherent to the desktop printer used in this work, the contact resistance was difficult to obtain because the extraction of the exact contact area was difficult. So, an alternative Greek cross was used as shown in Figure 3.17c and Figure 3.17d. This solution solves the misalignment problem thus allowing a right extraction of the contact resistance and allows a correct extraction of contact resistance.

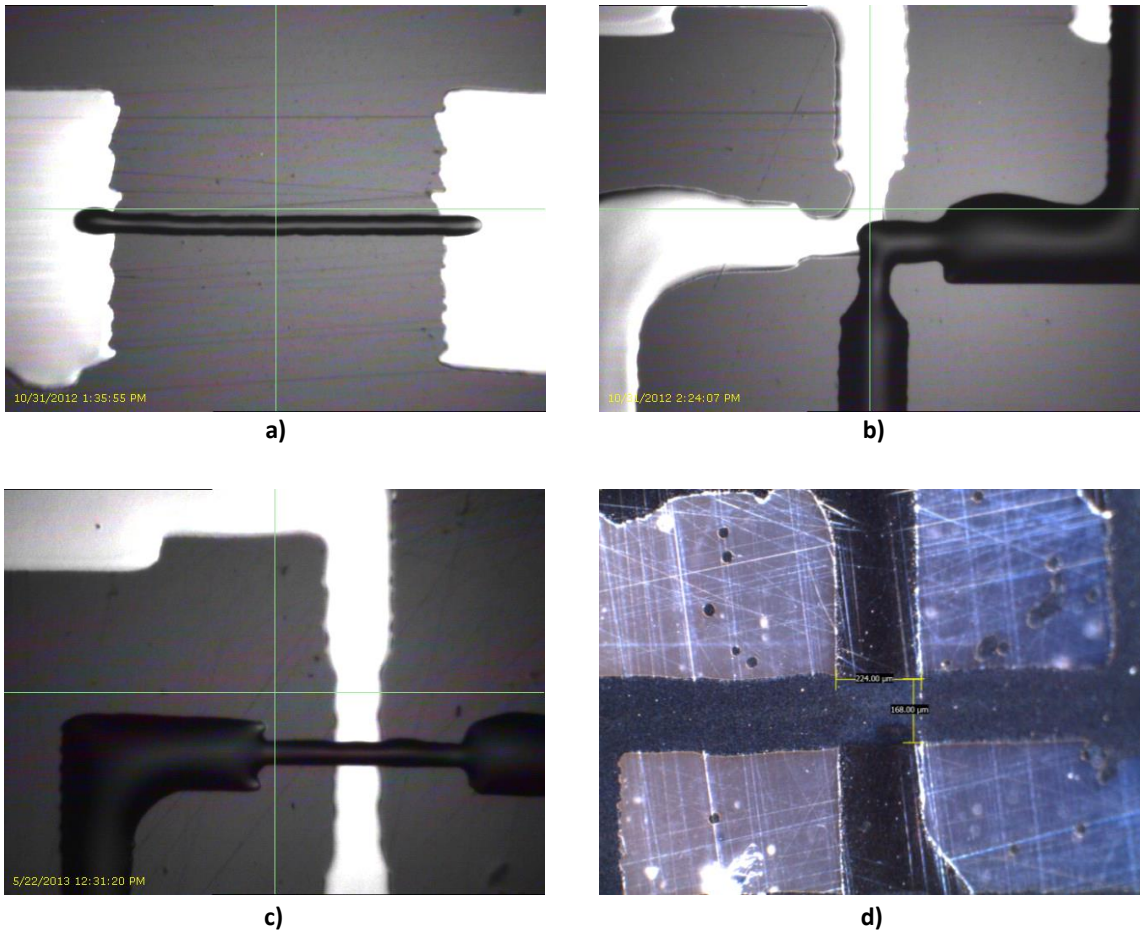


Figure 3.17. a) and b) Examples of resistors printed where the second layer is not yet cured; c) greek cross structure to extract contact resistance; and d) improved greek cross structure to overcome misalignment problems.

Figure 3.18 shows a resistor fabricated with both layers already sintered. We can observe the color difference between both layers (in fact they are made by using the same ink) due to the different curing conditions.

As we can observe in Figure 3.18d, the section of the resistive track is homogeneous without any remarkable coffee ring stain. This results in a more uniform profile that can be due to the low sintering temperature and time, without the need to apply any platen temperature or specific drop space during printing as demonstrated in Chapter 2.

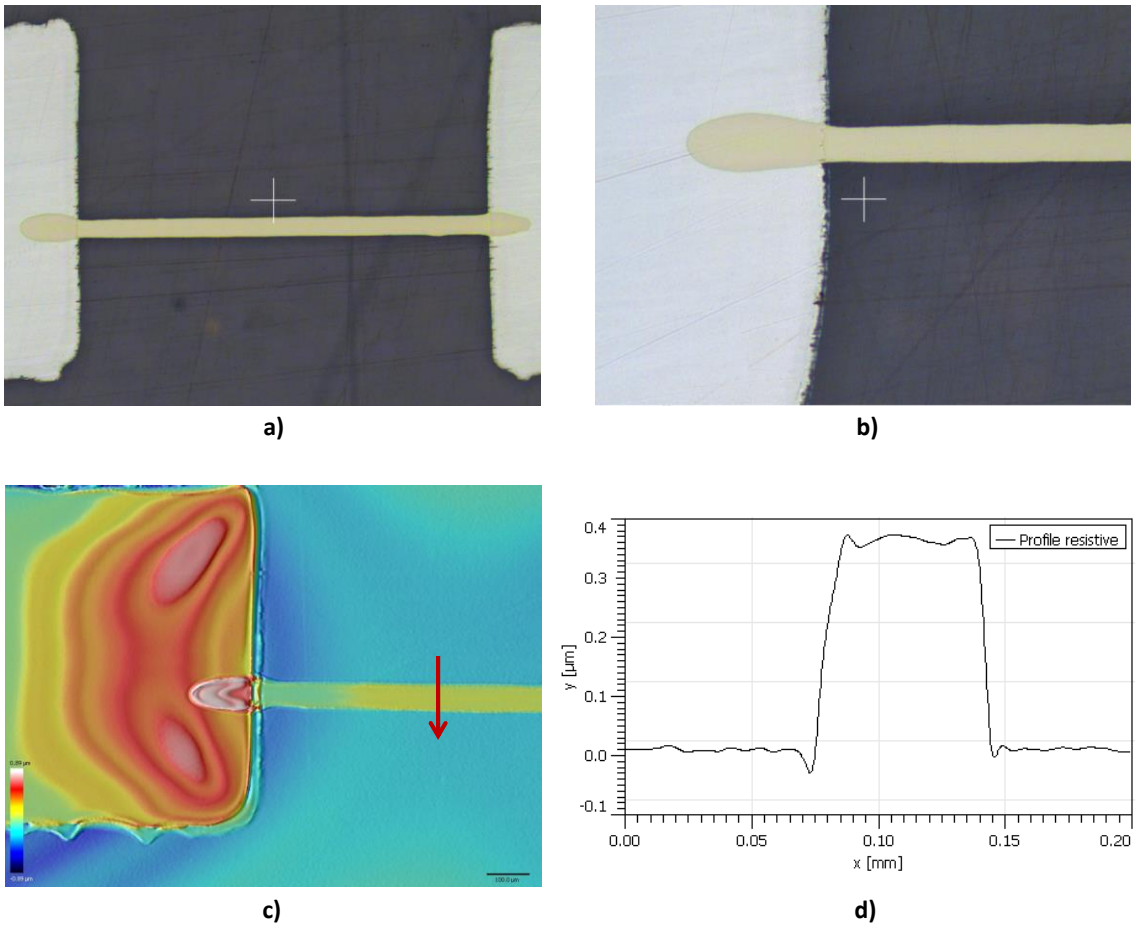


Figure 3.18. Resistors fabricated (measured resistive strip width is 65 µm): a) sintered resistor; b) contact resistance area of the resistor; c) confocal image of the resistor; and d) profile of the resistive track.

The contact interface between both layers was analyzed by FIB cut at Fraunhofer ENAS[18] facilities. Figure 3.19a shows the section of the interface between conductive (deposited underneath) and resistive (deposited on top) layers. The sandwich junction between both layers with different curing processes can be easily observed. Figure 3.19b shows the section of the resistive strip with a thickness of 245 nm. The underneath layer shows less boundaries between the particles due to the higher temperature and sintering time. The section of both layers is similar because we used the same ink and drop spacing. The black region on the bottom part is the PEN substrate used.

[18] Fraunhofer ENAS, Chemnitz (Germany).

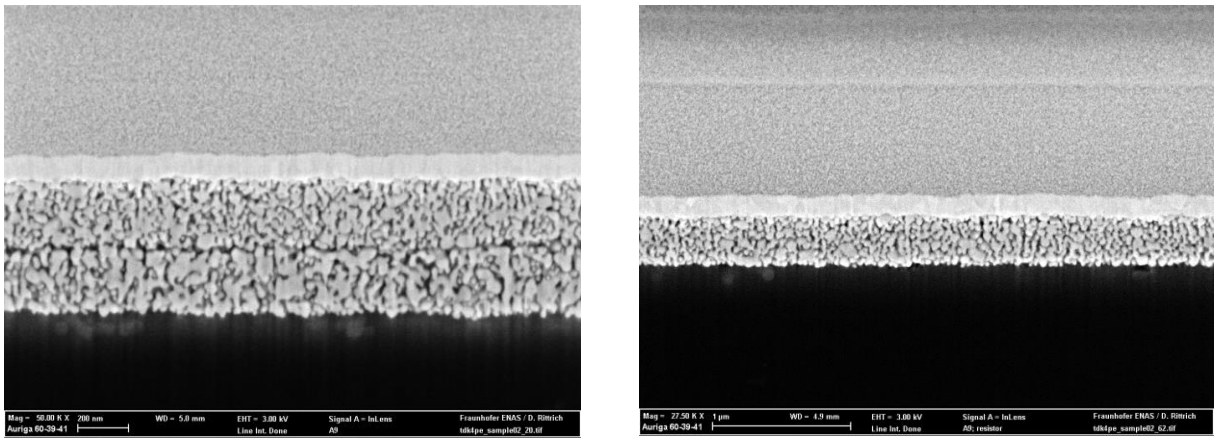


Figure 3.19. FIB section of a resistor: a) section of the interface between conductive and resistive layers; and b) section of the resistive strip[19].

Additionally, the resistive strip surface was analyzed my means of SEM[20] as shown in Figure 3.20.

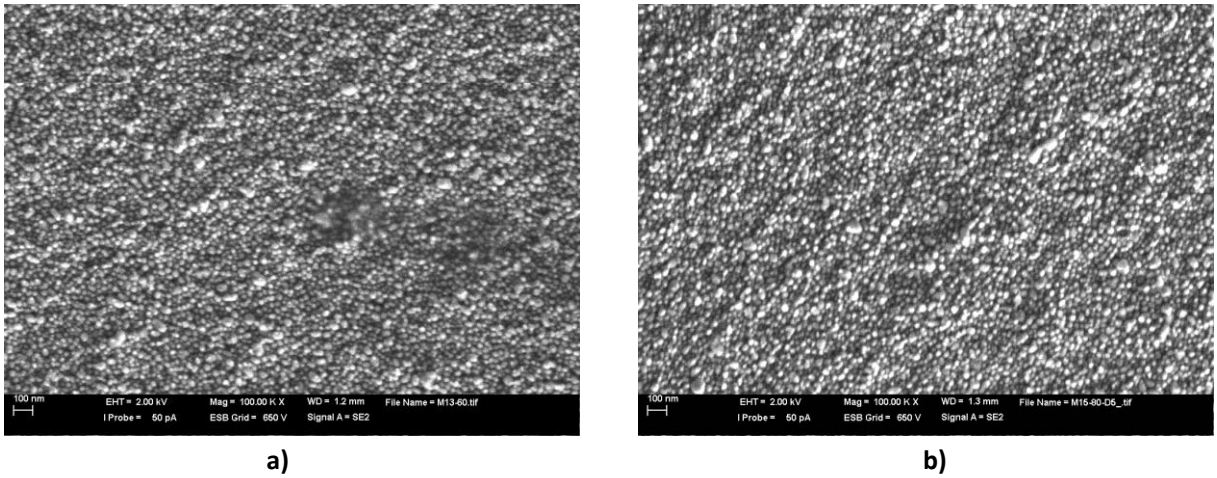


Figure 3.20. SEM images using 100kX augmentation of silver lines: a) cured at 60ºC during 2.5 minutes; b) cured at 80ºC during 10 minutes.

It cannot be observed that the agglomeration of nanoparticle between resistive strips cured at 60ºC during 2.5 min and cured at 80ºC during 10min are slightly different. However, significant electrical differences will be demonstrated in the following section.

[19]Measurements done at TUC.

[20] Servei de Microscopia de la UAB, ZEISS Merlin FE-SEM equipment.

3.2.2.2. Resistivity characterization as a function of the curing time and temperature

Different experiments were performed in order to characterize the resistivity as function of curing time and temperature to obtain a post-processing set-up suitable to make resistors with a high sheet resistance in the range of interest. Initially, the post-processing set-up range and resistive track dimensions were chosen based on the conductive lines characterizations done in the previous section and knowledge.

A big range of curing times (2.5, 3.15, 4, 5, 6.5, 7.5 and 10 min) and temperatures (60, 70 and 80 ºC) were used to have a rough characterization of the sheet resistance versus curing time and temperature. Selected values were lowered compared to those used in Figure 3.7.

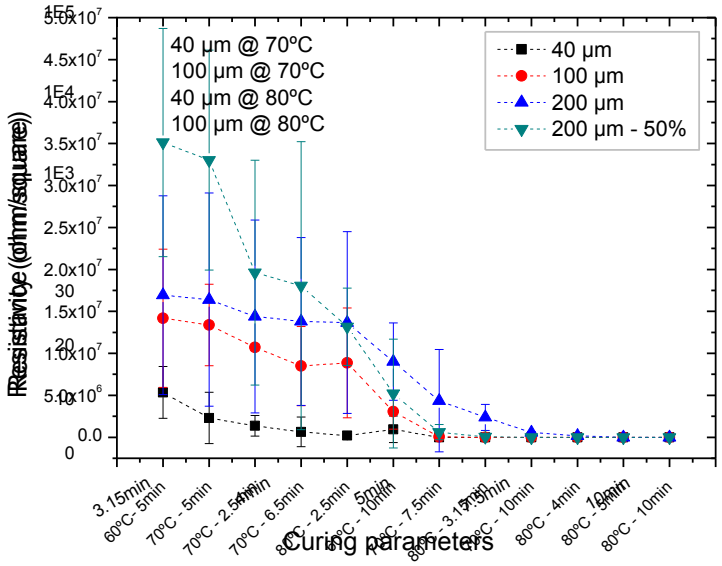


Figure 3.21. Sheet resistance of resistors with different linewidth, patterns, curing times and temperatures.

Figure 3.21 shows the sheet resistance of the characterized samples. The obtained behavior is opposite to the one expected based upon Equation 3.1. An increase in linewidth (W) resistive strip should decrease resistance, but results of 40, 100 and 200 µm resistive strips are opposite to this principle. This is because wider resistors have a higher ink density (bigger quantity of silver nanoparticle ink per area) thus requiring longer curing times. 40 µm resistors are sintered faster than 200 µm ones, thus, reducing faster its resistivity compared with the wider ones.

Resistors using a 50% filling pattern instead of a solid one (100% filled pattern) show the right behavior. A 50% pattern reduces to the half the density of material thus reducing the section and increasing the resistance by 2 as expected. This behavior is shown only for reduced sintering times and temperatures.

So, we can conclude that the scaling of resistors by its section is not linear as expected, thus we need to focus in fixed size comparing results only with the devices having the same dimensions.

The rest of measurements were dismissed because although some of the structures were correctly cured (the finest ones) the wider ones not. The edge between a curing structure and a non-cured one can let to variations from some hundreds of ohm to several Mohm. It is important to assure that any structure could be cured properly showing sheet resistance values in the expected range (tens to hundreds of ohms) regardless the width. To refine these values, an additional experiment was designed with a selected range of curing times and temperatures to obtain a more precise characterization of the resistivity versus curing time and temperature. Selected values were chosen from the results shown in Figure 3.21. A reduced set of device dimensions showing the resistivity were used in this experiment.

Moreover, electrical test vehicles used to characterize the contact resistance were added using the different resistive track widths. The contact resistance was measured by using the Greek cross test structure with a four-terminal measurement.

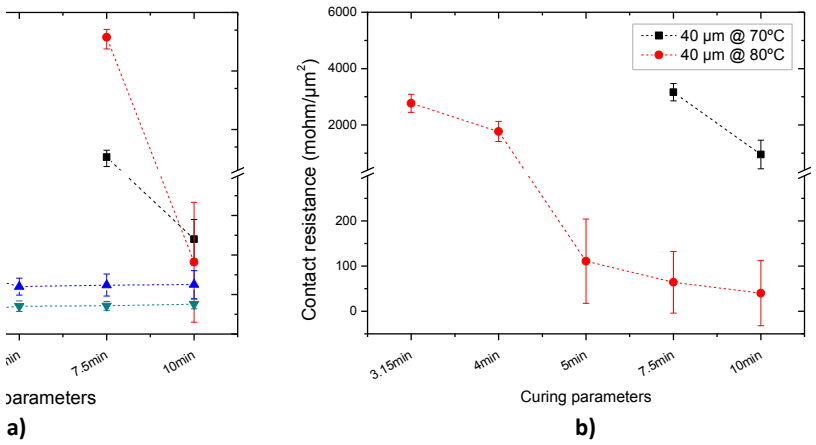


Figure 3.22. a) Sheet resistance; and b) contact resistance of resistors with different linewidth, curing times and temperatures.

From the Figure 3.22a, one can conclude that a curing temperature of 80ºC is the best choice. Lower values results in higher sheet resistances but also higher contact resistances. E.g. 40 µm lines cured at 70 ºC during 7.5 min shows a resistance of 336.44 ohm/□ and a contact resistance of 3.16 ohm/µm² resulting in an excessive $R_{contact}$ of 15 kohm. Same linewidth cured at 80 ºC during 10min shows a resistance of 24.01 ohm/□ and a contact resistance of 4.12 mohm/µm² resulting in a $R_{contact}$ of 19.78 ohm. Measured resistive strip width is 65 µm as shown in Figure 3.18d.

A curing temperature of 80ºC and a curing time of 10 minutes were selected in order to assure a successful curing process and a sheet and contact resistance in the expected range.

3.2.3. Inorganic resistor reliability, scalability and variability

In this experiment, the sheet resistance and resistivity were measured on different sized line resistors. Next figures will show the sheet resistance as a function of the thickness and the width to length ratio (W/L) of different resistor patterns depicted in Figure 3.16. The obtained data show a slight dependence of the resistivity on the size of resistors used in the measurements. These differences can be attributed to the thickness variation typically observed in thin films obtained by printing techniques. The obtained resistivity range of $5 \cdot 10^{-6}$ to 7×10^{-6} Ω·cm can be considered in good agreement with the literature data, when compared to the value obtained by Kim et al. [112] of $3 \cdot 10^{-6}$ Ω·cm for silver patterns (one of the lowest values to our knowledge, but obtained applying a pressure of 5MPa during the sintering process at 250°C, to facilitate the particles coalescence).

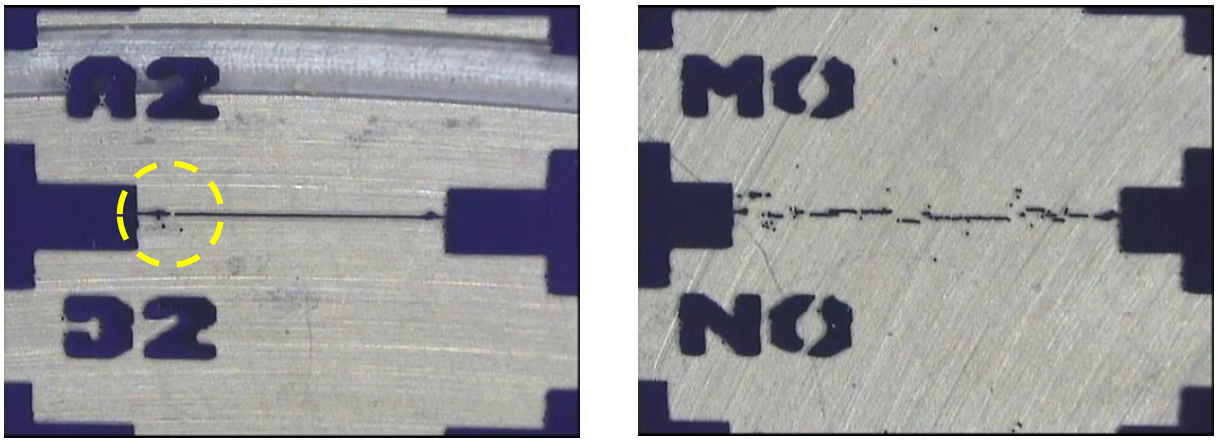
3.2.4. Large-scale fabrication of linear resistors

Based on the obtained results, a new experiment was designed in order to analyse the reliability and variability of these resistors.

In the initial experiment, resistive tracks were printed with a width of 40, 100 and 200 µm (both 50% and 100% solid) obtaining a $R_{\square}$ ranging from 3.35 Ω/□ (T=80 ºC, t=10 min and 200 µm width) to 54.18 Ω/□ (T=80 ºC, t=5 min and 200 µm width).

The new experiment contains devices with resistive tracks widths of 40, 60 and 80 µm, and lengths ranging from 1 mm to 6 mm. Resistors were printed both along and across printing directions. It means “horizontal” and “vertical” resistors. The design is shown in Annex C.4. In total, designs contain 442 resistors in a horizontal geometry and 396 in vertical. The resulting data of the characterization was processed and analysed and is shown in the following figures.

The resistances fabricated using resistive tracks of 40 µm were not successfully printed. Only 60 and 80 µm resistive tracks gave us useful resistors. The reasons come from various effects although the main effects observed are due to the nature of the printed line: a 40 µm resistive track is a line of just 1 drop width and strongly dependent on undesired printing effects. One missing drop or misaligned drop will cause an open circuit as shown in Figure 3.23.



a) b)

Figure 3.23. Undesired printing effects in 40 µm width lines.

As can be seen in Figure 3.24a, similar values of sheet resistance can be observed between the resistors fabricated with different lengths and widths of 60 and 80 µm. As expected, resistors of 80 µm are less resistive due to the bigger section of the track. Standard deviation does not reveal large differences between both approaches. A reasonable yield was obtained in these devices, with a minimum of a 70% and coming close to 100% in some cases, as shown in Figure 3.24b. This indicates a very stable printing process. There is not a clear correlation between yield and length or width of resistors. Differences are depending on the position occupied within the printed sheets, as inkjet printer uses to fail in specific regions of the printed sheet (until printer printhead is cleaned unclogging nozzles).

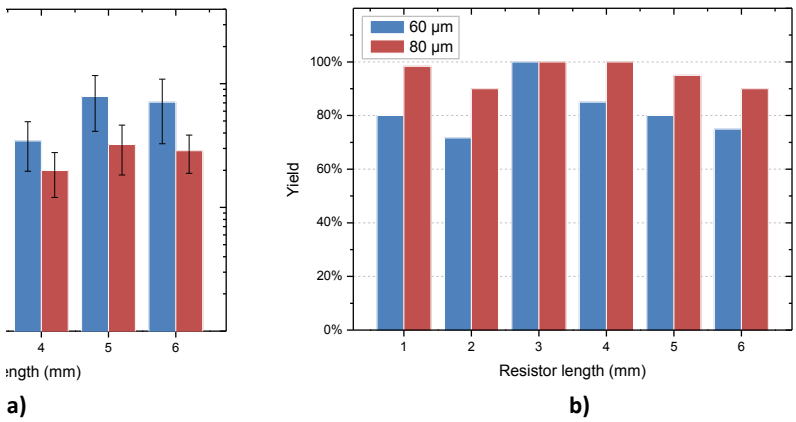


Figure 3.24. Linear horizontal resistors: a) $R_{\square}$ and b) yield, as a function of resistor width and length.

The data obtained from the 409 working resistors give us an average sheet resistance of 45.05 Ω/□ with a standard deviation of 23.56 Ω/□ for 60 µm width resistors. For 80 µm width

resistors, the average sheet resistance obtained is 24.42 Ω/□ with a standard deviation of 14.83 Ω/□. Still, variability is quite high.

The distribution of values is clearly following a Weibull distribution instead of a normal distribution as expected.

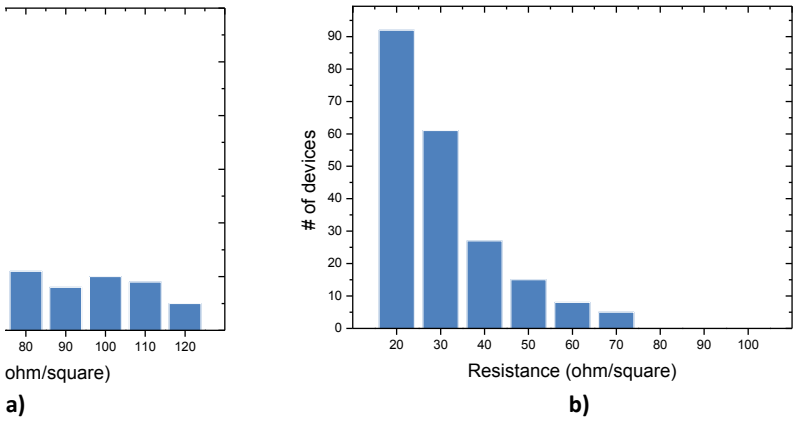


Figure 3.25. Histogram of: a) 60 µm width resistors; b) 80µm width resistors.

Vertical resistors are more sensitive to printing effects. Moreover, due to these printing effects and inhomogeneities observed in the printed resistive tracks, the average sheet resistance is quite higher than that obtained in horizontal resistors, as shown in Figure 3.26a.

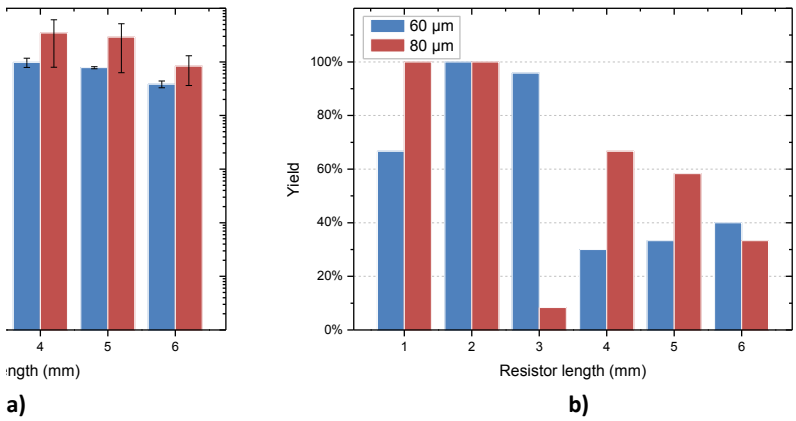


Figure 3.26. Linear vertical resistors: a) $R_{□}$ and b) yield, as a function of resistor width and length.

Differences up to two orders of magnitude in square resistance can be observed at same time than yield decreases significantly. The best yield is obtained for the shorter resistors (since the probability of defects due to printing effects is smaller) and decreases for larger resistors, as depicted in Figure 3.26b. There is a specific situation for 80 µm resistors with 3 mm length were 92% of devices failed due to clogged nozzles.

Therefore, vertical resistors are not recommended as they are strongly dependent of inkjet printing effects.

3.2.5. Large-scale fabrication of snake resistors

Based on the results of linear resistors, a new experiment was designed containing snake resistors with resistive tracks widths (W) of 40 and 60 µm, a fixed length of vertical bars (L) of 820 µm and the number of meanders (Z) ranging from 3 up to 15. The design is shown in Figure 3.27.

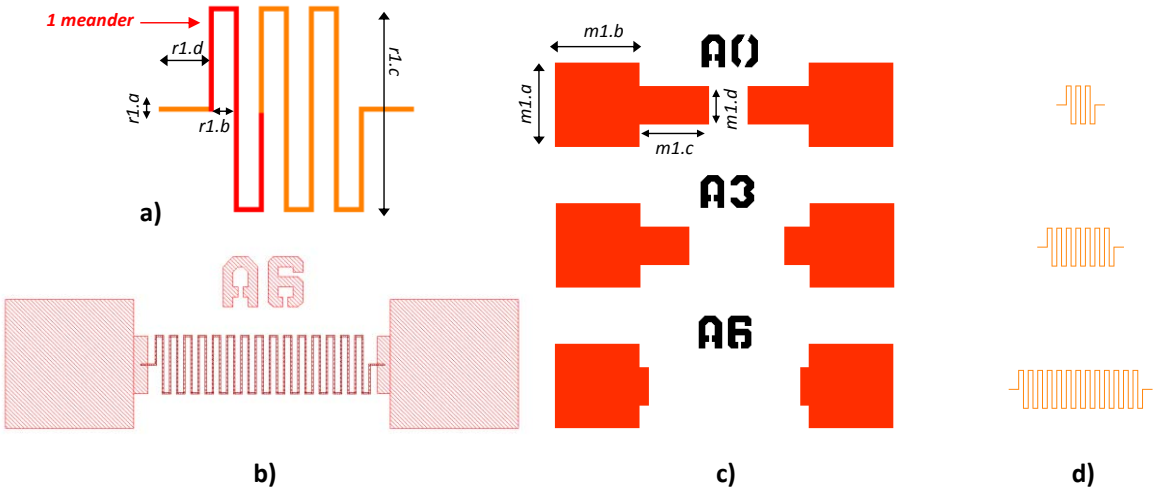


Figure 3.27. a) Schema of a snake resistive strip (red line corresponds to a meander); b) complete layout of a snake resistor; c) contact layer layout; and d) resistance layer layout.

1326 devices were fabricated. From those, only 680 devices were successfully printed and used for characterization. In this fabrication, 40 and 60 µm resistive tracks gave us useful snake resistors. The design is shown in Annex C.5

The snake resistors show of course higher resistances than linear resistors. Next figure shows the average resistance per meander as a function of the number of meanders in resistors. As expected, the resistance increases with the number of meanders.

The resistances were printed vertically resulting in horizontal strips of meanders. This assured larger strips printed in printing direction and only short strips (corners) in counter direction.

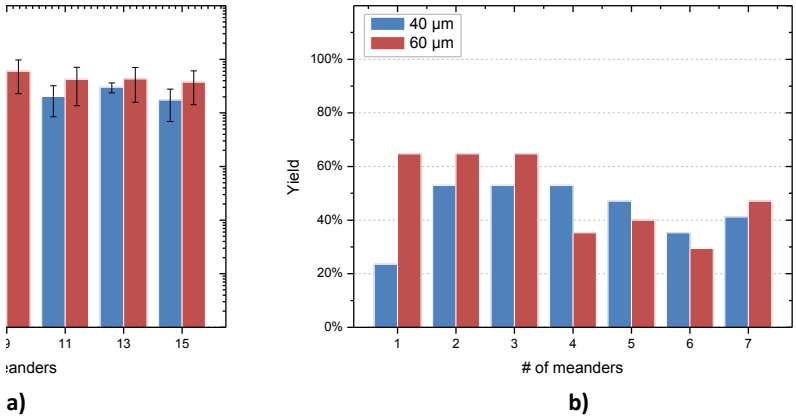


Figure 3.28. Snake horizontal resistors: a) resistance per meander; and b) yield as a function of the number of meanders.

As it can be seen, no big differences can be observed between the resistors fabricated with widths of 40 and 60 µm in terms of resistance per meander. In general, resistors of 40 µm are less resistive due to the smaller section of the track that reduces ink coalescence. Standard deviation does not reveal large differences between both approaches.

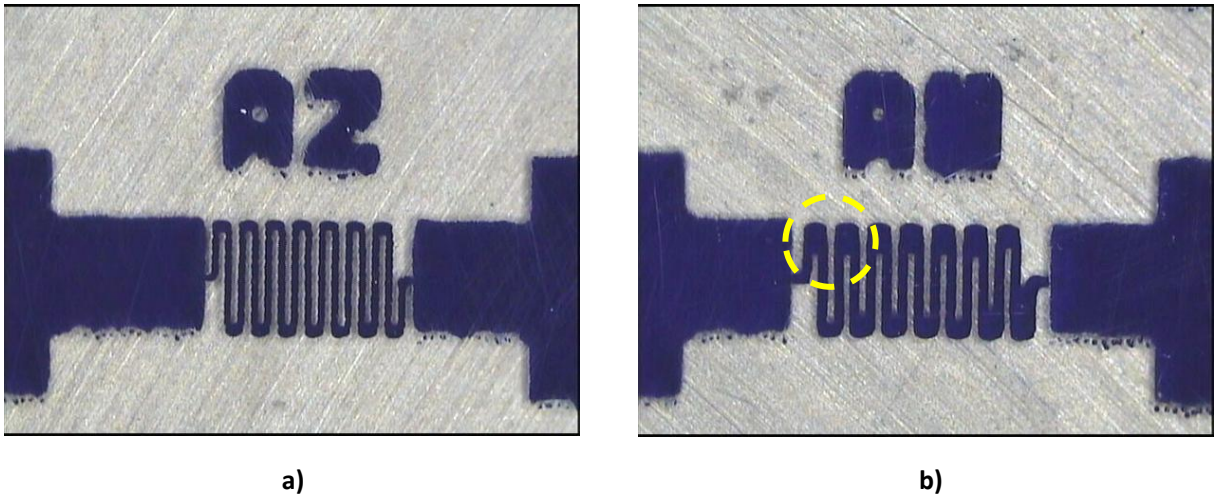


Figure 3.29. Images of snake resistors: a) 40 µm; and b) 60 µm width.

Figure 3.29 shows some representative effects observed in snake resistors. As can be seen, 40 µm lines (Figure 3.29a) keep better the expected line morphology. For 60 µm (Figure 3.29b), the lines are too wide so that the ink coalescence modifies the printed pattern in the corners thus shortening the effective length of resistive tracks and modifying the expected sheet resistance, obtaining a higher value of resistance.

The yield obtained in these devices is comparable low, with an average of only 47% and never higher than 65%. It seems that wider resistors have a bit higher yield, but main differences

arise on the position occupied within the printed sheets. Printing the snake resistive track is more challenging than a simple line as in the linear resistors.

The data obtained from the working snake resistors give us an average resistance of 14.7 KΩ/meander with a standard deviation of 8.37 KΩ/□ for 40 µm width resistors.

3.2.6. Inorganic resistor-based WORM memories

Metallic nanoparticle inks are used for Printed Electronics, but to reach acceptable conductivity the structures need to be sintered, usually using a furnace [113]. In this section, sintering by direct resistive heating is introduced. This method has also been demonstrated in the literature [114][115][116]. In this Joule heating method, a voltage is applied to the printed partially-sintered structure, and the current heats the structure locally between the electrodes.

The technology of changing the electrical properties of conductive lines made by metallic nanoparticles is known as RES (Rapid Electrical Sintering) [117] in the literature.

Figure 3.30 also shows current and resistance curves of a device scanning from 0 V to 10 V. Scanning towards +10 V, the current density has a peak around 8 V. As the section of a 40 µm linewidth partially-sintered track is $21.1 \cdot 10^3$ µm², the change in the resistance starts for a current density of 307 ± 22 nA/µm². This corresponds at current value of 6.3 mA.

The device current is about 2 orders of magnitude higher when the voltage is swept back and for the following appends. Thus, the device conductivity cannot be recovered, indicating a permanent change. There is no recovery observed after 12 months storage.

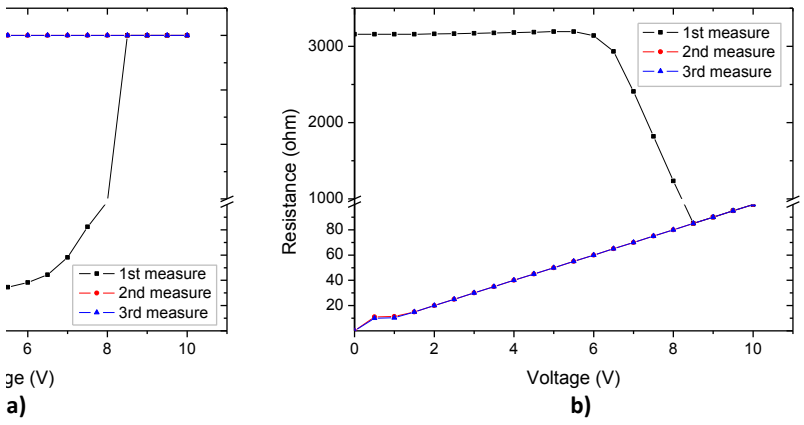


Figure 3.30. a) Current and b) resistance of curves at different measurements. 1st measurement (fresh), 2nd and 3rd measurements after RES effect occurred.

Figure 3.31a shows the electrical sintering process for a single sample. The resistance is constant while the current density does not reach the level of auto-sintering.

An interesting effect can be observed in the Figure 3.31b where the electrical sintering process is interrupted at certain moment (after 1st measurement). The following measurements required of different current densities to start changing the resistance of the partially-conductive track. In the second measurement, the resistance starts lowering and need a higher current density to start electrical sintering process again. This new current density is the value where the first measurement ends. But after partial sintering, the change in the resistance is the same than if the current were applied in a single process.

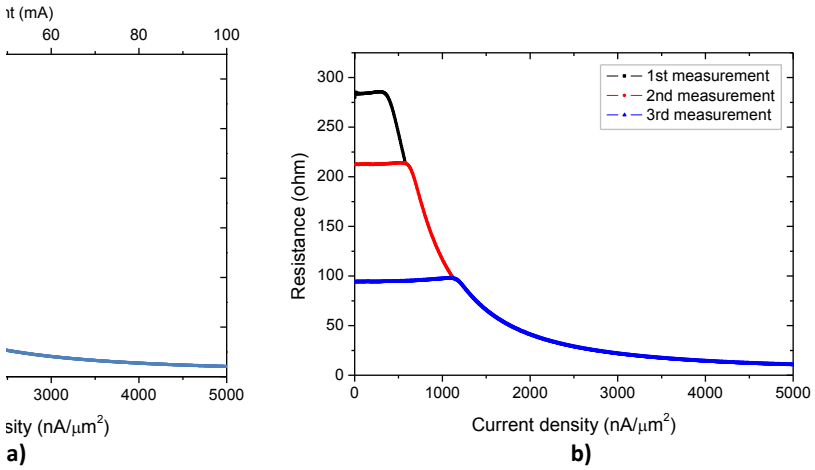


Figure 3.31. Resistance change during an electrical sintering process: a) in a single measurement, b) in consecutive measurements.

Applying a bias current equivalent of 300 nA/μm² (the edge of the change), it can be observed just a slight reduction of a 0.12% ± 0.045% after 30 minutes of continuous bias stress. So, the resistance is quite stable if the level of auto-sintering is not reached.

The rapid electrical sintering (RES) method has been demonstrated in the literature [117][118][119] to enable a fully-printed programmable Write-Once-Read-Many (WORM) memory with low operating power [120]. This property can be used for the fabrication of inkjet printed programmable WORM memories [121]. A memory bit can be arranged as a conducting track pattern consisting of a partially-sintered line between two electrodes.

The memory bits can be switched from an initial, high-resistance state to a low-resistance state using rapid electrical sintering, representing two binary states. RES is realized by applying a voltage over the partially-sintered nanoparticle track. The applied voltage generates power dissipation in the printed bit thus enabling rapid sintering of the nanoparticles.

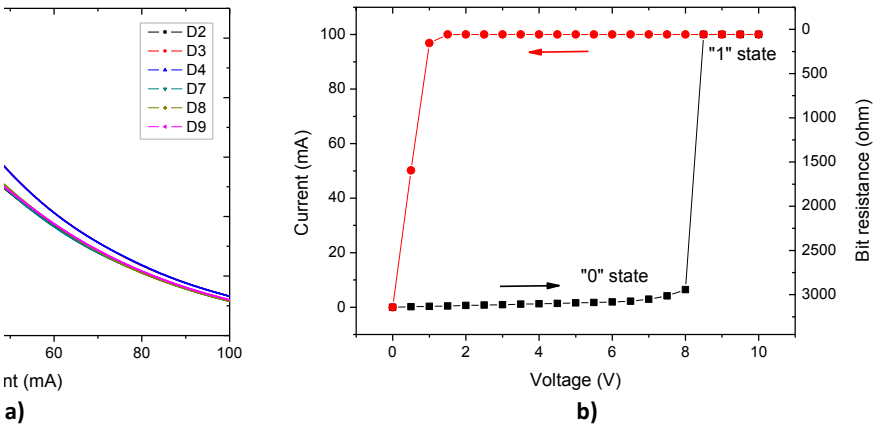


Figure 3.32. a) Resistance change due to electrical sintering process in different devices; b) measured bit resistance (R_B) and applied voltage during bit state switching. The transition from the high-resistance state "0" to the low-resistance state "1" via RES can be observed.

Also, the reproducibility of the process is important. Figure 3.32a depicts the change in resistance measured in several resistors of 200 µm width. Resistors present slight resistance variations in the low-sintered "0" state. These resistance variations can be considered negligible for the highly-sintered "1" state. The curves are very similar, indicating that the current is determined largely by the properties of the partially-sintered silver layer and its interfaces.

As shown in Figure 3.32b, a switching voltage V_{bias} of 8 V is required for the transition from state "0" to state "1" for a typical printed bit of 3 KΩ. Here, the memory can be programmed by coupling a voltage across selected bits in order to switch the bit from state "0" to state "1".

Its long-term stability is also important. The small resistance drift observed demonstrates that it could support 18.000 memory accesses (100 ms access time).

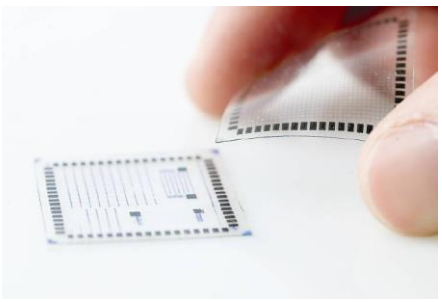


Figure 3.33. Printed WORM memory[21].

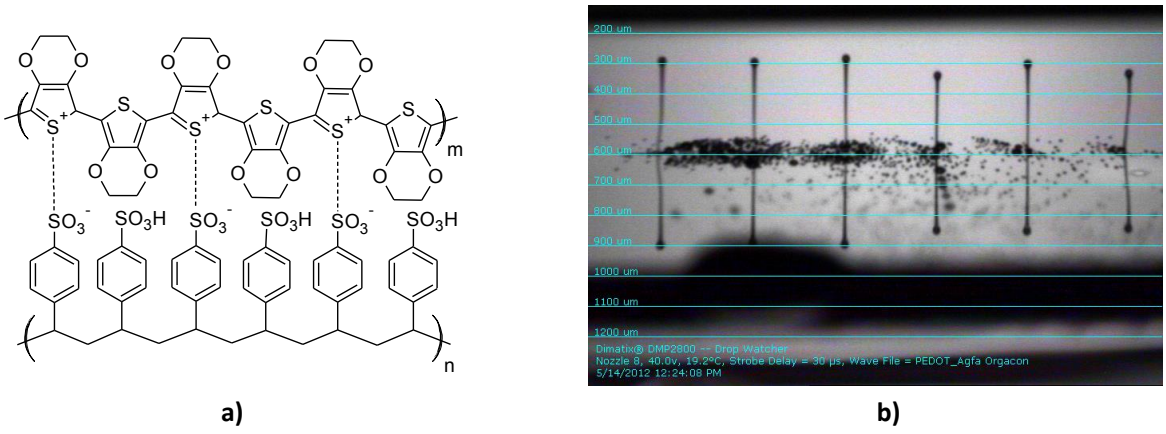
This WORM fabrication and read-out approach offers potential for low-cost memory applications as well as e.g. resistance-change sensors, as shown in Figure 3.33. Other interesting approaches required of more complex materials and/or processes [122].

[21] Source: Thin Film Electronics.

3.2.7. Organic resistors

Organic conductive materials can be used as resistive materials due to its low conductivity compared with inorganic metallic materials. Conductive polymers are organic polymers that conduct electricity in the same manner than semiconductors conducts. The biggest advantage of conductive polymers is their processability. Conductive polymers can combine the mechanical properties (flexibility, toughness, malleability, elasticity, etc.) of plastics (as they are polymers) with relative electrical conductivities. Their properties can be fine-tuned using the methods of organic synthesis. Nevertheless, conductivities are still low and they can be considered in the range useful resistive tracks.

Poly(3,4-ethylenedioxythiophene) poly(styrenesulfonate) (widely known as PEDOT:PSS) is a mixture of two polymers: one conducting positive charges and the other negative ones, as depicted in Figure 3.34a. It is often used as a transparent conductive contact in touch screens, OLEDs and electronic paper as a replacement of ITO layers.



a) b)

Figure 3.34. a) PEDOT:PSS molecular structure; and b) PEDOT:PSS drop ejection.

PEDOT:PSS is a yellow liquid ink containing the polymer conducting mixture, organic solvents and polymeric binders specially prepared for inkjet printing techniques. The ink used is produced by Heraeus GmbH company (its commercial name is Clevios P Jet HC) and have an announced conductivity between $3 \cdot 10^3$ and $9 \cdot 10^3$ S/m (4 orders of magnitude lower than silver ink). In this work, PEDOT:PSS have been used as resistive ink and silver as conductive ink in device electrodes. The ink provided by Heraeus shows a good and stable ejection, as shown in Figure 3.34b.

3.2.7.1. Fabrication process

The resistor structures were printed using 10pL print heads and a drop spacing of 20 µm. Two different substrates were used: Polymide (Kapton) film (DuPont USA) with a thickness

of 100 µm and PEN film (DuPont Teijin Teonex Q65FA). Before any printing step, both films were cleaned using ethanol and dried with nitrogen.

As shown in Figure 3.35, printing the organic resistors required three types of materials: inorganic conductive, organic conductive and insulator ink. A layer of silver nanoparticle ink (Suntronic EMD5603 from SunChemical Corp.) is used for the contact pads. It is deposited using a platen temperature of 40ºC and sintered at 130°C during 30 min. Two or three layers of high conductivity PEDOT:PSS (Heraeus Clevios P Jet HC) are printed with different widths of 200, 300 and 400 µm to evaluate resistance, film thickness and regularity. Finally, a layer of insulator ink have to be deposited onto the PEDOT:PSS to protect the polymer of moisture which could screen the electrical results.

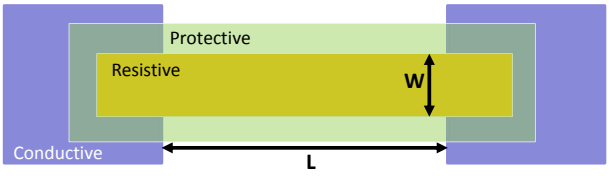


Figure 3.35. Linear resistor structure and geometry.

Initially, the right deposition procedure was investigated. Figure 3.36a shows a resistor where the un-sintered silver pads have been deposited on top of the PEDOT:PSS layer. Silver diffuses on PEDOT:PSS, as shown in figures. If resistive track is shorter it can short-circuit the device, as shown in Figure 3.36b. So, conductive pads are required to be printed first.

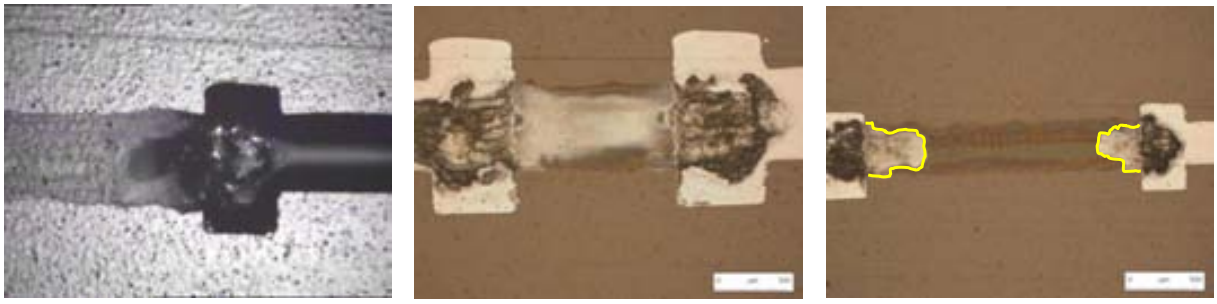


Figure 3.36. Resistances printed depositing PEDOT:PSS as the first layer.

The surface energy of Kapton is 52 mN/m and the contact angle of the used PEDOT:PSS on Kapton is measured at 6.3°. These conditions allow for an interesting wettability of PEDOT:PSS on Kapton film which is very important to get reproducible and defect-free printed structures.

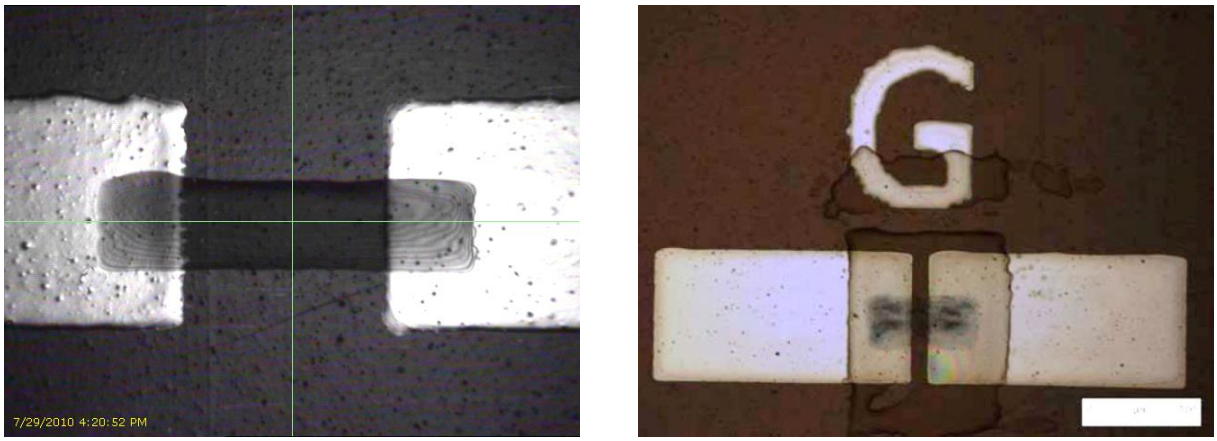


Figure 3.37. PEDOT:PSS printed on Kapton: a) unprotected resistance and b) resistor with a barrier layer.

Figure 3.37a shows a printed resistor before curing the PEDOT:PSS on Kapton. As shown in the figure, the uniformity of the PEDOT:PSS layer can be considered as very good. But Kapton is not the intended substrate to be used in this work since its high roughness is not suitable for the fabrication of OTFTs, and following experiments use PEN substrate.

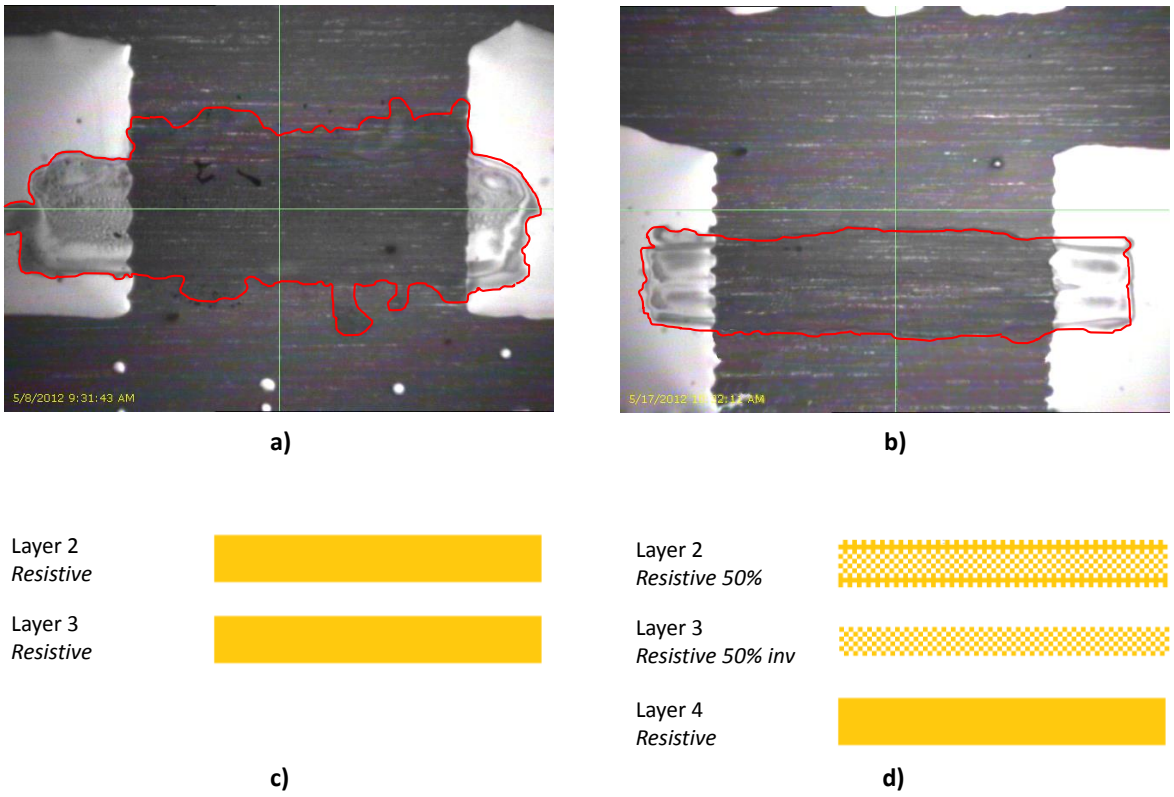


Figure 3.38. PEDOT:PSS printed on PEN: a) without any modified pattern; b) after the application different patterns to improve line homogeneity; c) unmodified pattern; and d) best pattern applied to improve line homogeneity.

The surface energy of PEN is 32 mN/m and the contact angle of the used PEDOT:PSS on PEN is measured at 3.5°. These conditions are more complicated than the previous ones as the wettability of the PEDOT:PSS on PEN film will be more complex to get reproducible and defect-free printed structures. Figure 3.38a shows two printed layers of PEDOT:PSS printed directly on PEN using the pattern shown in Figure 3.38c.

To improve line homogeneity on PEN, different patterns were evaluated. The best result was obtained when the layer of PEDOT:PSS was printed first using a drop lattice of a 50% filling with 100% solid internal line, followed for the inverse pattern of the first one, and finally a last layer using a 100% solid line, as shown in Figure 3.38d. A more homogeneous line was obtained by using the improved pattern as shown in Figure 3.38b. All the layers were printed using a substrate temperature of 60ºC and cured at 130°C during 10 min. An alignment process was performed in order to assure layer accuracy (due to sample move for curing processes and cartridge change).

The resistive layer tends to absorb water from environment because the PEDOT:PSS is hygroscopic. This fact represents a degradation of resistors, as its impedance will change over the time as a function of time and ambient conditions.

Thus, in order to avoid degradation due moisture, an insulator layer of crosslinked PVP (Poly 4-vinylphenol) is added as a barrier layer to protect the device against moisture degradation. Figure 3.37b shows a resistor (dark track between metal electrodes) with the barrier layer of c-PVP printed on top.

3.2.7.2. Characterization of preliminary organic resistors

Initially, a set of 460 resistors printed on PEN substrate changing the width, thickness and printing orientation was fabricated and characterized to extract resistance and tolerance. The layout used for the experiment is shown in Annex C.3.

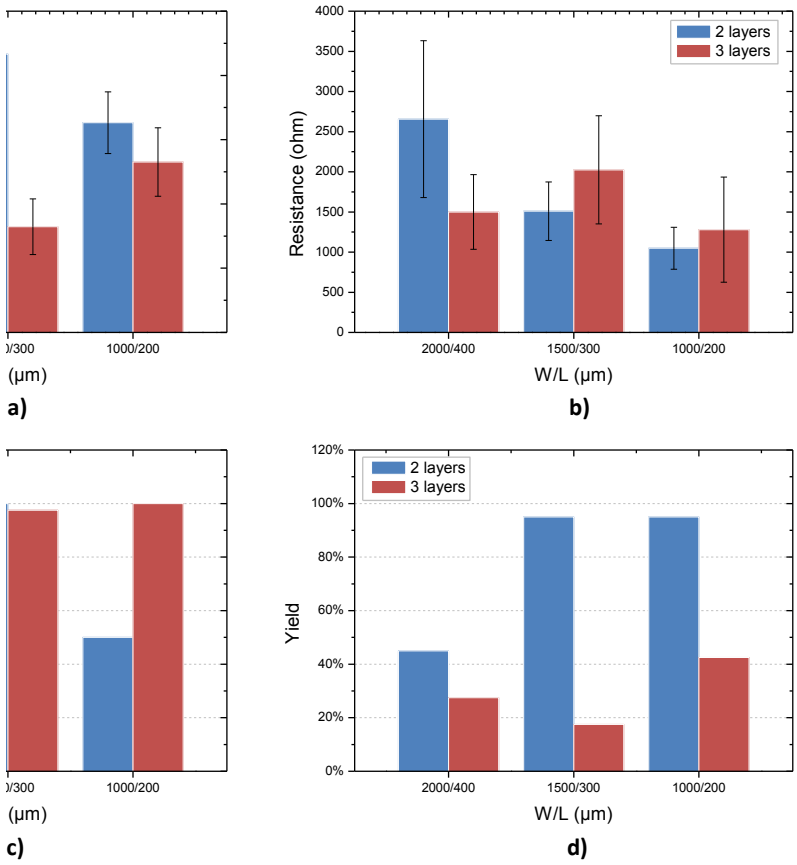


Figure 3.39. a) Mean electrical resistance for horizontal resistors; b) mean electrical resistance for vertical resistors; c) yield for horizontal resistors; and d) yield for vertical resistors. The X axis shows the resistive track dimensions marked as width and length (W/L).

According to the results summarized in Figure 3.39, the best design is printing direction printed with 300 µm width and 2 layers of PEDOT:PSS. The sheet resistance obtained was 340 Ω/□ ± 20%. This is a remarkable result to take into account. The resistor voltage coefficient (RVC) for this design will be less than 1518 ppm/V (estimated in a 1V to 10V range with a confidence of 96% for a set of 40 samples).

As already demonstrated in previous section, yield and variability parameters are better in horizontal (or printing) direction than in vertical (across printing) direction. The reason is because the deposition of materials in printing direction is more regular than across printing direction due to the misalignments produced in printer's carriage.

The results summarized in Figure 3.39 shows 3 different size resistors but all of them having a quantity of squares (# = W/L) of five. So, we should expect obtaining similar resistances in all of them. The differences are caused for the different spread of the ink in the substrate as a function of the number of layers and the width of the deposited layer. Nevertheless, the results are similar and differences can be attributed to the deviation of measures and printing effects.

Measured resistivity takes into account contact resistance according to the Equation 3.6, showing a contact resistance of 0.16 ± 0.02 mohm/µm². An order of magnitude lower than the obtained in inorganic resistors presented in previous section.

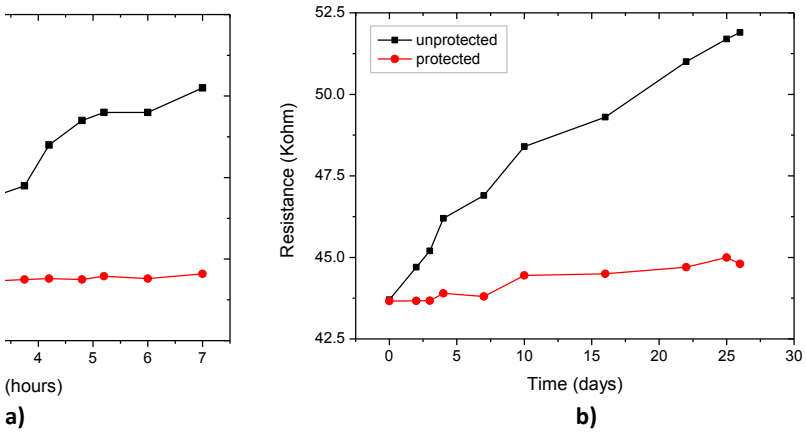


Figure 3.40. Resistance variation in room monitored conditions vs time

Different tests under room conditions were performed to analyze stability of values measured over time, as shown in Figure 3.40.

Results show an increase of resistance in devices over the time. This result was already expected, since one of the key problems in organic polymeric films is that they are affected by oxygen and moisture. Inks are formed by organic molecules with low bonding forces (van der Waals bonds) and water and oxygen molecules are easily absorbed and trapped in the polymer network, thus producing the resistance increase observed in Figure 3.40. Resistors protected with a c-PVP layer present much better behavior than those unprotected.

Based on the previous experimental results a new experiment was set-up by using a snake configuration for proof of concept purposes. A new layout was designed containing 24 snake resistors with an expected value of 100 kΩ.

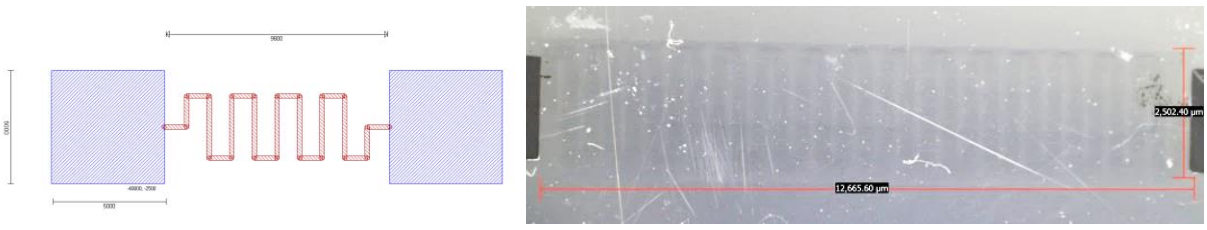


Figure 3.41. Left: Generic resistor layout; Right: the inkjet printed resistor used.

The average measured value was 100,6 kΩ ± 4%. The variability of these devices is reduced and allows using them in organic circuits, e.g. digital/analog converters using resistor networks as R/2R or weighted DACs.

3.2.7.3. Morphological optimization of PEDOT:PSS resistors

The problem of the spread of ink due to a low contact angle has been faced up by different approaches in the literature.

L. Cui et al in [123] demonstrated a simple and novel method for avoiding the coffee ring structure has been demonstrated based on hydrophobic silicon pillar arrays during single-drop evaporation by. In a different approach, H. Kang et al [95], studied the optimization of the geometry of inkjet-printed polymer films demonstrating how drop spacing and ink concentration affect the thickness and morphology of a printed film. These approaches to improve the morphology of the PEDOT:PSS printed lines can be of great significance for extensive applications of material deposition.

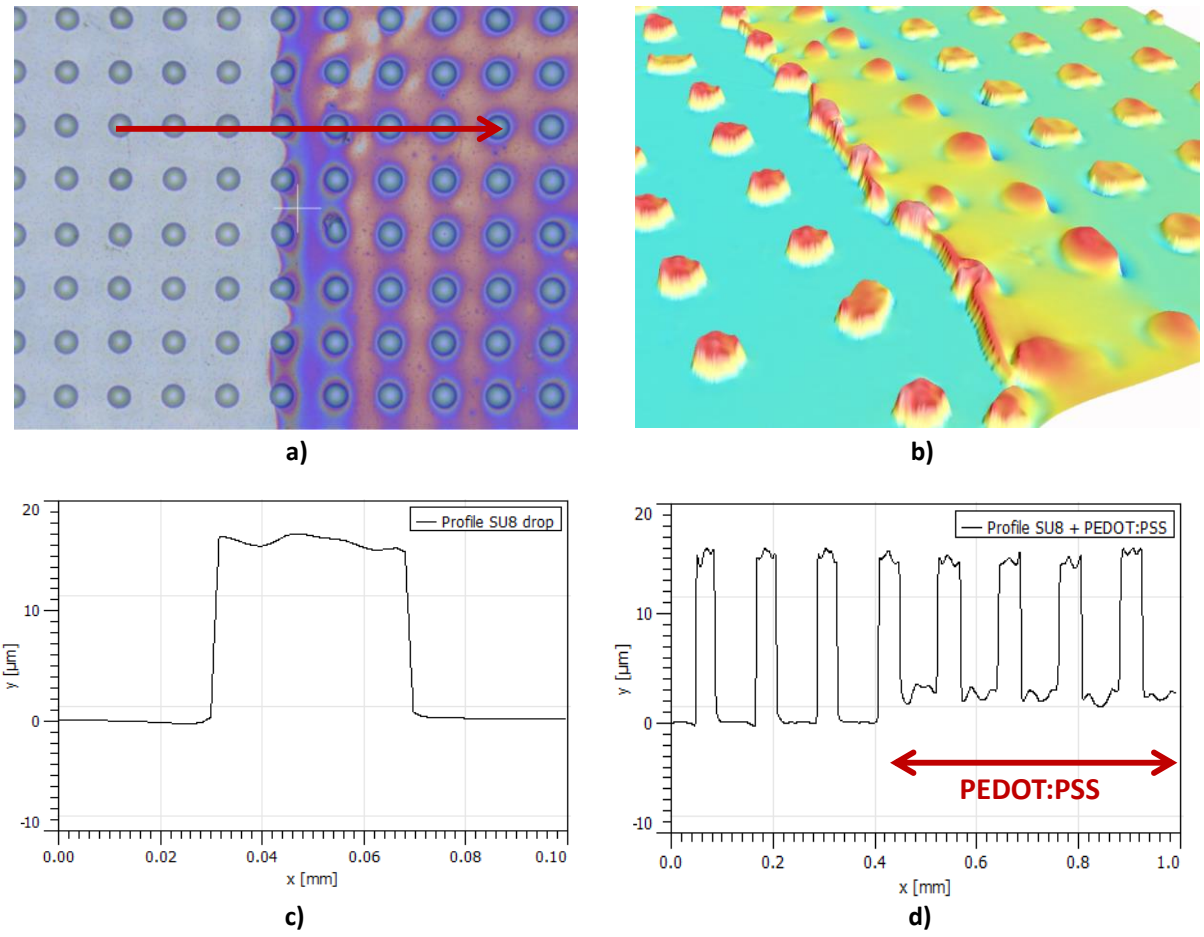


Figure 3.42. a) Optical image of the SU8 drops and PEDOT:PSS (right side); b) confocal image of the same area; c) cross section profile of a SU8 drop/pillar; and d) cross-section profile of a the red arrow in a) showing the SU8 drops and the PEDOT:PSS area.

Starting from these approaches, we proposed an experiment by using SU8 pillars (single drops) deposited in a lattice, as shown in Figure 3.42a, Figure 3.42b and Figure 3.42c. EPR164 is a SU8 experimental ink developed by Microchem USA for inkjet printing. The ink

is developed for inkjet printing by using Dimatix printheads although it is not yet totally optimized for printing.

As shown in Figure 3.42b and Figure 3.42d, SU8 pillars are confining the PEDOT:PSS and avoiding its excessive spread on the PEN substrate due to its low contact angle on it.

Based on that, we worked in two different approaches. First approach, is playing with the PEDOT:PSS pattern in order to improve its deposition. The *reference* layout printed is the same used in the previous section. It is composed of a silver ink layer to print both contact electrodes. PEDOT:PSS is printed in two consecutive layers of solid pattern. The layout of this design was already shown in Figure 3.38c and Figure 3.38a shows a printed resistor. As previously demonstrated, the PEDOT:PSS ink spreads onto the PEN substrate giving a non-homogeneous lines resulting in non-homogeneous devices with a large variability in resistance.

Figure 3.38d shows the layout of a different approach (named approach #2). Here, the first layer of resistive material is printed using a pattern with a 50% solid reinforced with a wall at the edge of the resistive strip. The printing of the second layer, the inverse of the first 50% pattern, is delayed to evaporate the solvent of the first layer avoiding increase of ink coalescence. Third layer is printed on top of the other ones. Finally, the amount of ink corresponds to two layers and we expect to have similar resistance values than with the previous approach. Figure 3.38b shows the improvement obtained using this approach applying different drop lattices.

In a different approach, we used inkjet SU8 ink to create an anchor or wall to the PEDOT:PSS ink to reduce its spread, as already shown in Figure 3.42. Figure 3.43 shows three additional approaches to improve PEDOT:PSS wetting. The first two approaches (Figure 3.43a and Figure 3.43b corresponding to approaches numbered #3 and #4) use SU8 pillars for anchoring PEDOT:PSS avoiding its excessive spread on the surface of PEN substrate. Figure 3.43c shows a different approach (numbered approach #5) where a wall of SU8 is deposited to enclose PEDOT:PSS on the boundaries defined.

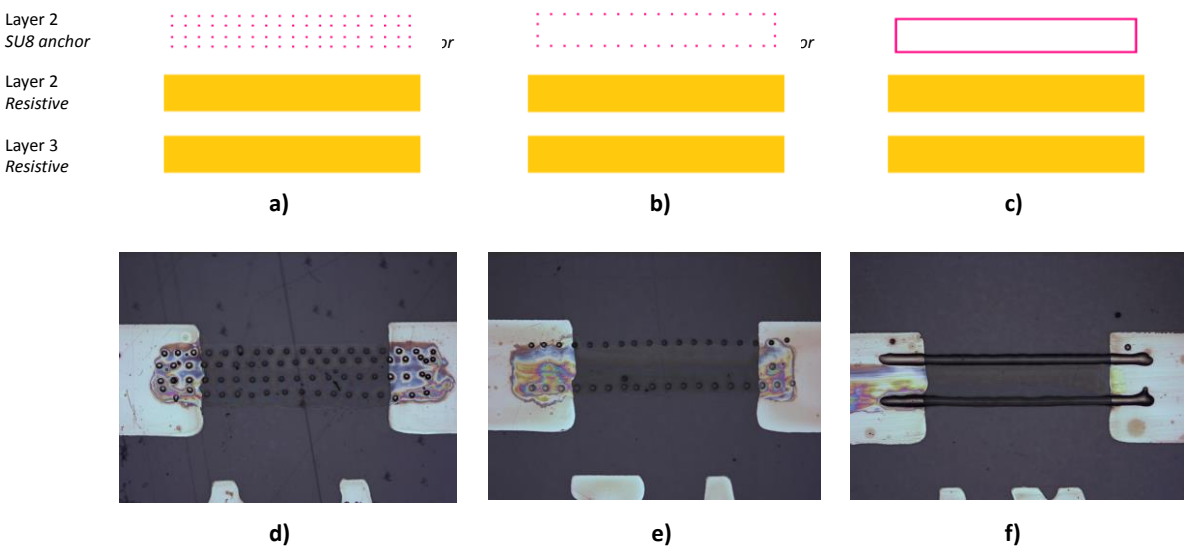


Figure 3.43. Layout and visible image of the different approaches playing with the printed patters: a) and d) approach #3, b) and e) approach #4, and finally c) and f) approach #5.

Based on the five approaches proposed, the electrical characterization of a large number of resistors (100 of each design) was done. Figure 3.44 shows the variability of the resistance versus the different approaches used. We can see that we can reduce the variability in the measurements of the sheet resistance by improving line homogeneity.

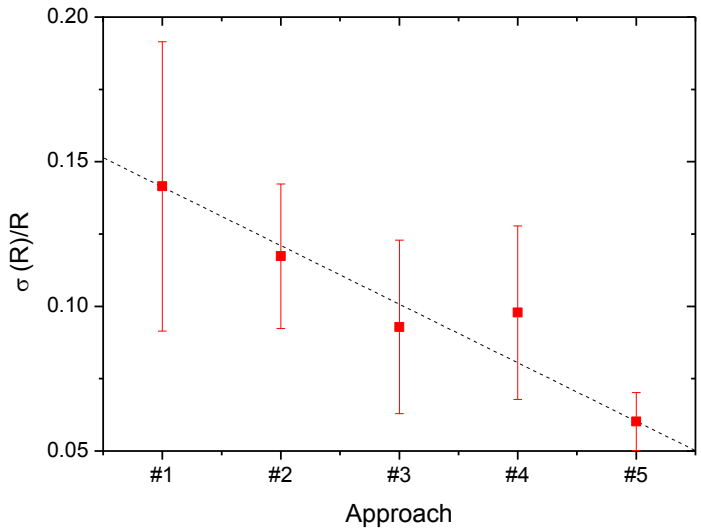


Figure 3.44. Ratio between standard deviation versus the average of square resistance as a function of the different approaches used. The dots are the obtained measurements; the dashed line is the corresponding fit. The error bars corresponds at the variance between resistors with different widths (200, 300 and 400 μm).

Approach #1 has a larger deviation versus the average of sheet resistance. Also, deviation between resistors with different widths is larger than by using the other approaches. Based on these results, we can conclude that the approach #5, corresponding to the layout shown in

Figure 3.43c layout shows the lowest variability. This demonstrates that confining the ink spread by using a SU8 wall is the best approach.

Using PEDOT:PSS as a resistive track is a good option although it implies the use of two additional materials (PEDOT:PSS and c-PVP). Nevertheless, in the following sections we will use c-PVP also for the fabrication of capacitors and OTFTs, so, this additional material will not represent any additional printing step.

3.3. Capacitors

A capacitor is a device that stores electrical charge. In one of its simplest forms, it contains two conducting metal plates separated by an insulator or dielectric material. When a voltage is applied, electric field shifts negative charges to one electrode and positive charges to the other one. This reconfiguration of electrical charge continues until the electric potential equals the applied voltage. Then the charge remains or "is stored" in the dielectric layer even after the voltage source is removed. Capacitance measures how well the charge is stored. Two types of monolithic capacitors can be printed: metal-insulator-metal (MIM) and interdigitated capacitors, but only MIM capacitors have been implemented in this thesis work as they were more interesting due to its multilayer structure and the work to improve them is directly related to the fabrication of OTFTs in the next chapter.

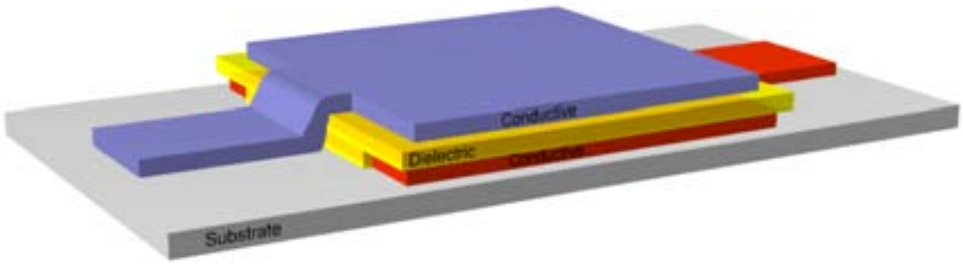


Figure 3.45.Scheme of parallel plate (MIM) capacitor structure

3.3.1. Metal-Insulator-Metal (MIM) fabrication

In the literature, we can find different approaches to fabricate capacitors using inkjet printing have been implemented. Some of them use additional fabrication methods different than inkjet printing [124]. Others reported capacitors are based on non-flexible substrates [36][34] or require high temperature processing (>250 °C) [34] which is too high for most flexible substrates.

In this section, different experiments and fabrications were performed with small quantities of capacitors to evaluate morphological effects and characterize them electrically in deep.

3.3.1.1. Dielectric material selected

In this work, we used a insulator solution called c-PVP which was made of poly(4-vinyl phenol) (PVP) as dielectric and poly(melamine-co-formaldehyde) methylated (PMFM) as crosslinker in propylene glycol monomethyl ether acetate (PGMEA) as solvent shown in Figure 3.46. Several formulations can be found in the literature [125][53][126][54]. UAB and

ENEA developed a new recipe for its formulation that we used in this work. In the literature, spin-coated c-PVP shows decent dielectric strength (up to 1.5 MV/cm) and relative permittivity between 3.9 and 4.3 depending on crosslinker ratio [127].

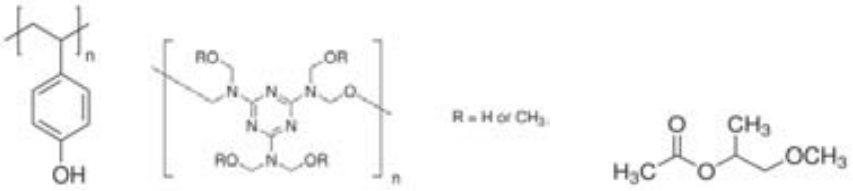


Figure 3.46. Molecular structure of PVP (left), crosslinker PMFM (right) and PGMEA solvent used for the preparation of the c-PVP solution.

Curing procedure consists in drying the sample at temperatures between 120 ºC and 200 ºC. Thicknesses of the inkjet printed layers obtained use to be in the range from 400 nm up to 1.2 µm depending on drop spacing used. The film shows the coffee ring effect with internal area rather planar.

3.3.1.2. Fabrication process

Initial structures were printed using silver nanoparticle ink as electrodes over a PEN (125 µm) substrate. The aforementioned crosslinked PVP (c-PVP) was used as dielectric.

The capacitor structures were printed using DMC-1161 printheads with 21 µm opening nozzle (10 pL) with a firing frequency of 10 KHz and a substrate holder temperature of 40°C.

Figure 3.47 depicts the layer stack of the capacitor device. Figure 3.48a shows the layout drawn using Clewin[22] EDA software for the all-inkjet printed capacitor. The first inkjet printed layer is the conductive silver bottom electrode, represented in red. The second inkjet printed layer is the dielectric film, represented in yellow. Finally the conductive silver top electrode is printed on top of the dielectric layer, represented in blue.

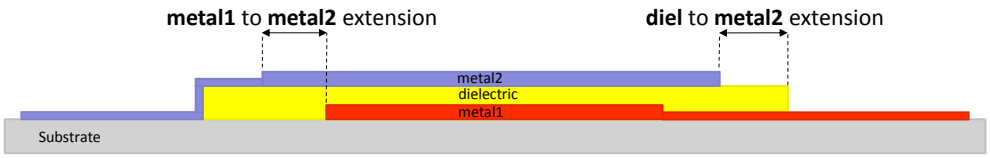


Figure 3.47. Layer stack of a parallel plate capacitor. This image shows also the name of design rules for a capacitor.

Alignment marks on the pattern layout were added to ensure the both parallel plate capacitor electrodes are precisely aligned although we used pyramid geometry to avoid

[22] Clewin layout software from Wieweb Software Inc

misalignment problems. To achieve a high quality capacitor all three layers need low surface roughness and good uniformity. It is important to eliminate pinholes and avoid missing or poorly printed lines in the dielectric layer between the silver electrodes in the capacitor structure. Therefore a large dielectric pattern is printed before to ensure the ink is firing consistently before reaching the active dielectric layer. This avoids the problem, common with inkjet printing, that the first few drops of each line can be unreliably printed.

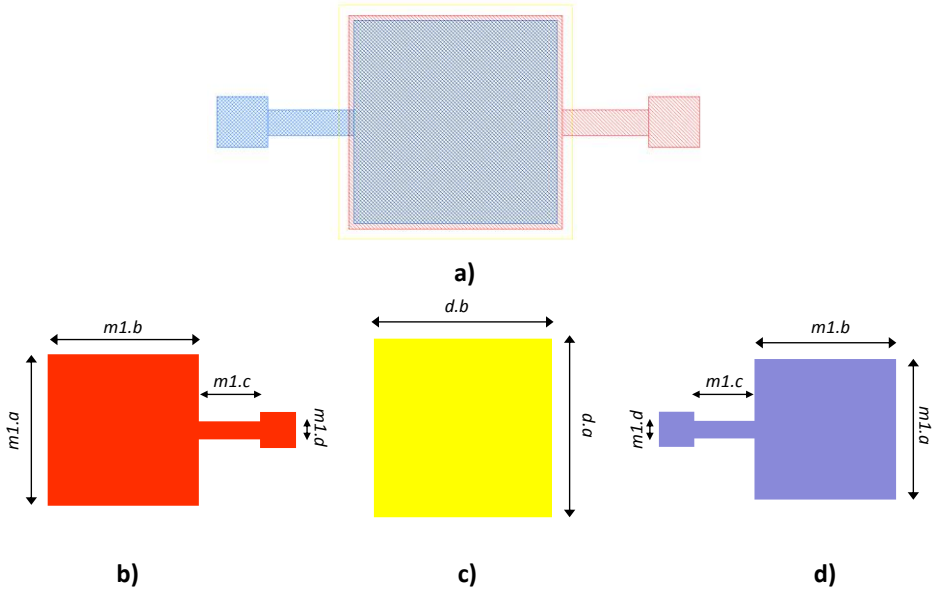


Figure 3.48. a) Layout of the printed capacitor; b) metal1 (bottom contact) layer pattern; c) diel1 (dielectric) layer pattern; and d) metal2 (top contact) layer pattern. Contact pads are 1x1 mm.

The first conductive electrode was inkjet printed on the PEN film with 20 µm drop spacing and a plate temperature of 40°C. The conductive ink used is the silver nanoparticle dispersion EMD5603 from SunChemical Inc. The PEN surface was pre-cleaned with ethanol and dried by a N_2 flux to remove remaining dust particles. This is enough to avoid the requirement to pre-treat the PEN as the wettability of the conductive silver ink is good. Once the bottom silver conductor is printed, it is cured at 130 °C for 30 minutes in a convection oven. 130 °C was chosen because it provides a suitable compromise between sufficient conductivity and future compatibility with fabrication. Next, the c-PVP dielectric was printed. Initially, we used the same drop spacing as for the bottom silver conductor at 20 °C. Dielectric was then sintered in a convection oven at 200°C for 20m. Finally the top silver electrode was printed under the same conditions as the metal1 layer and cured as before.

An optical image of an inkjet printed capacitor and a SEM image of a printed capacitor is shown in Figure 3.49a and Figure 3.49b respectively.

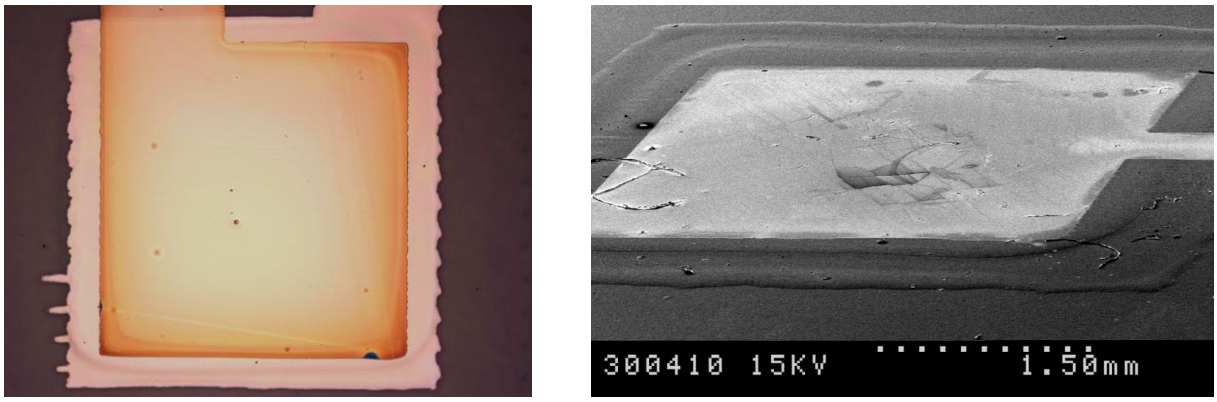


Figure 3.49. a) Capacitor fabricated using c-PVP dielectric; and b) SEM image of an inkjet printed MIM capacitor.

Figure 3.49b shows transparent insulator layer in the bottom with a strong coffee ring effect. Bottom metallic contact is not visible except in left side of image where contact line shape can be observed under insulator film. Top metallic contact is printed over insulator layer after curing.

3.3.1.3. Morphological characterization

Figure 3.50 shows a SEM cross sectional image and a focus ion beam (FIB) cut through the MIM structure of an inkjet printed capacitor.

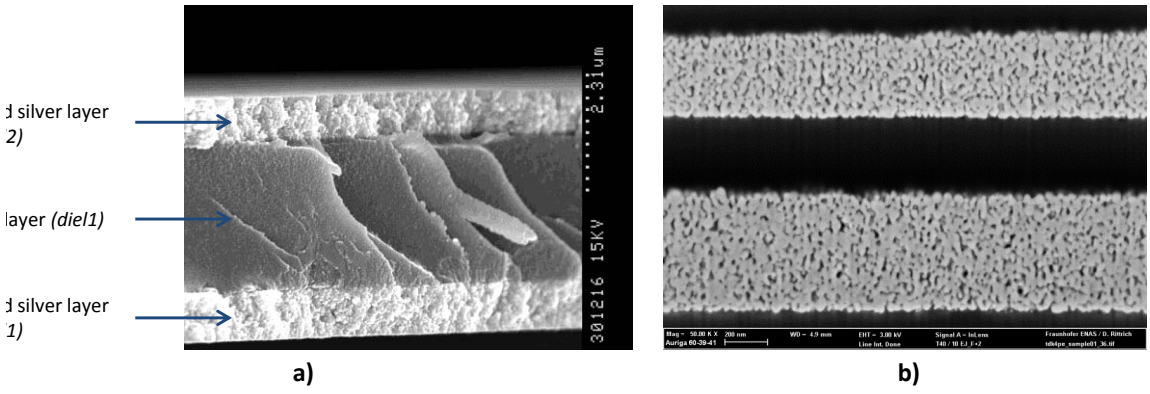


Figure 3.50. a) SEM cross sectional image; and b) FIB cut of the inkjet printed capacitor.

Figure 3.51 shows different images of the printed layers deposited by the inkjet printer. Figure 3.51a show the dielectric layer deposited on top of *metal1*. To assure film homogeneity is mandatory to avoid using the area of *diel1* where the coffee ring stain is present. Figure 3.51b shows the *metal2* (top contact electrode) deposited on top of the previously cured *metal1* and *diel1* layers.

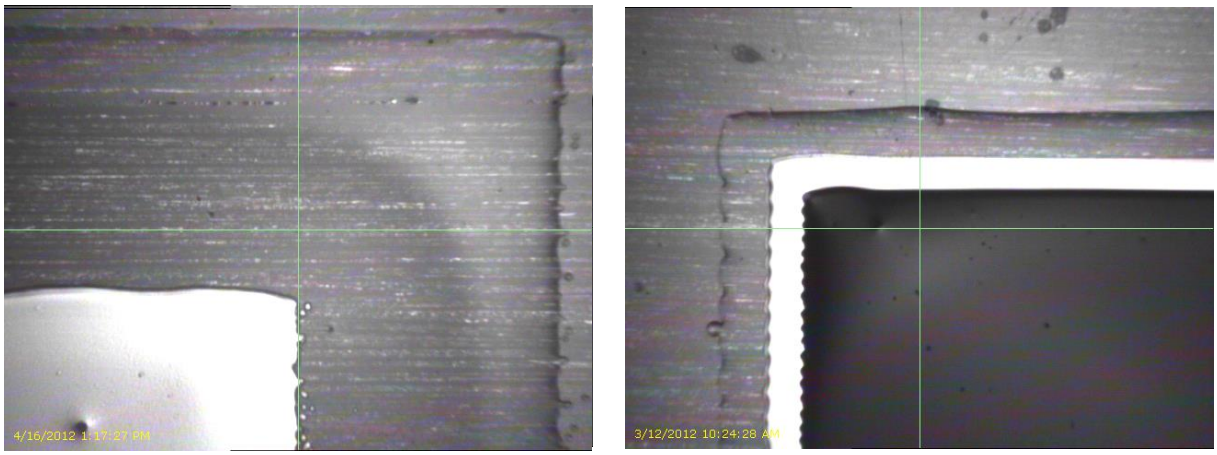


Figure 3.51. Consecutive printed layers to fabricate a capacitor. Images were taken using the fiducial camera of the inkjet printer.

Figure 3.52 shows the coffee ring of a c-PVP layer deposited and its corresponding cross-section profile. As it can be seen in Figure 3.52b the coffee ring height is up to several times higher than the average film thickness in the center. In the following chapter, dielectric morphology will be studied in depth as it is more crucial in the fabrication of OTFTs.

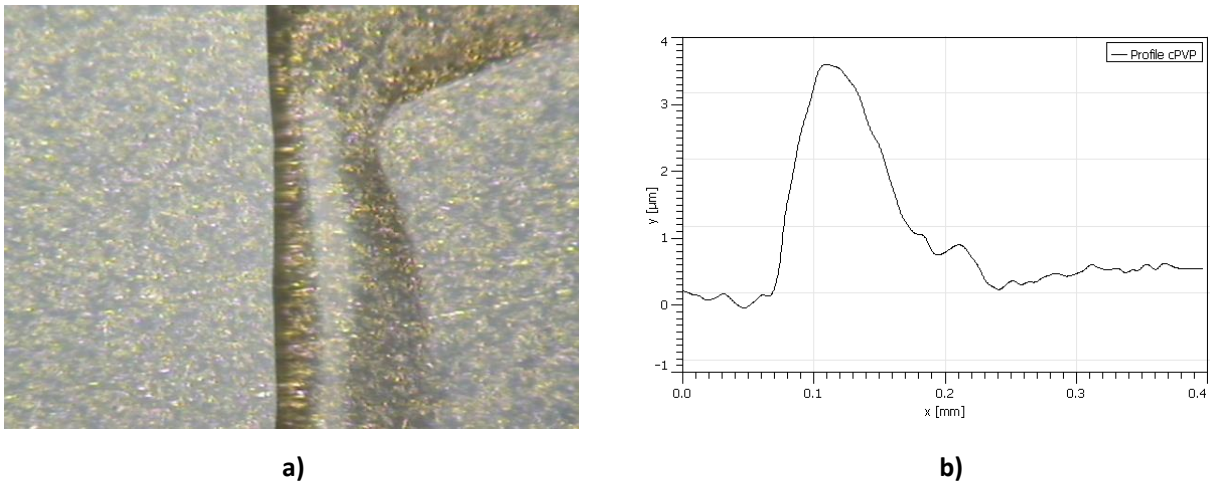


Figure 3.52. a) Microscope image of the c-PVP at the edge; and b) profilometry of a c-PVP layer showing the coffee ring effect at the edge.

In printing, both film thickness and composition may vary due to print process parameters and ink formulation, reducing the uniformity of printed dielectric layer. This is critical in the case of capacitors, where the involved layers but specially the dielectric one must be uniform, defect- and pinhole-free and capable of separating charge at the desired bias without breakdown and with minimal loss. Different printing effects invalidate some of the fabricated

capacitors as non-working devices. The reasons are diverse and an accurate morphological inspection was done to detect them. Basically, the main effects observed are due to:

- Shortcuts: a current path between top and bottom electrodes giving us a low parallel resistance. This effect can be caused by:
- A missing dielectric line as can be shown in Figure 3.53a.
- A dust particle deposited in the first metallic layer modifying the deposited behaviour of the subsequent layers as can be shown in Figure 3.53b.
- Layer misalignment between consecutive deposited layers, as can be shown in Figure 3.53c.
- Open circuits in connection tracks due to missed printed lines of metallic inks. Figure 3.53c (red circle) show this effect observed.

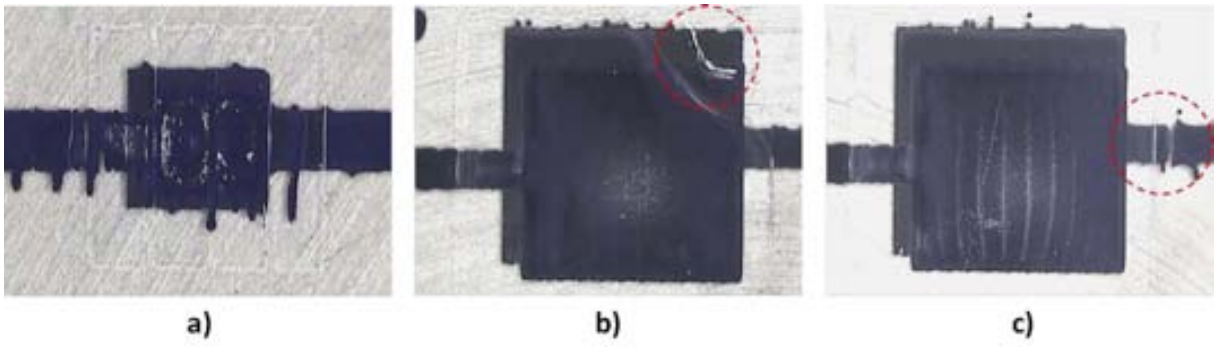


Figure 3.53. Examples of printing effects invalidating devices: a) missing dielectric lines; b) presence of dust; and c) layer misalignment and open circuit (red circle).

Uniformity of the dielectric film is crucial because thin areas of the film will have a bigger chance of dielectric breakdown. Defects, such as cracks or pinholes, provide potential paths that can act as conduits for charge. This may either be in the form of surface conductivity due to moisture, migration of electrode atoms or may be filled by conductor printed over the dielectric material, causing a short circuit. Cracks can appear due to shrink of the dielectric layer during curing or drying, or mechanical damage due to external forces. Pinholes are columns of open space though the thickness of the film. They can be formed due to a bubble of entrapped gas that breaks after the film is set or cured.

3.3.2. Electrical characterization

The capacitance of the devices was measured using an Agilent E4980A LCR measurement system. Parallel Capacitance (C_p) and Parallel Resistance (R_p) across a frequency range from 1 kHz to 1 MHz were measured.

The theoretical capacitance value can be calculated using the following equation.

$$C = \frac{\varepsilon_r \cdot \varepsilon_o \cdot A}{d} \qquad \textit{Eq. 3.1}$$

Where C is the value of the capacitance, ε_r is the relative permittivity of the dielectric material, ε_o is the vacuum permittivity, A is the effective capacitive area of the two parallel plates, and d is the distance between the two parallel plates, which is also the thickness of the dielectric layer.

A capacitor with 3 layers of c-PVP and with an effective area of 16 mm² based on a designed *metal1_to_metal2_extension* of 4 mm was characterized in frequency. The measured thickness of the c-PVP dielectric layer was 1.35 µm. The reported relative permittivity of c-PVP is 4.1-4.3 depending on cross-linker ratio [127]. Therefore, the theoretical capacitance value can be calculated to be 415 pF using Equation 3.1.

The variation of the parallel capacitance and the parallel resistance across the frequency range from 1 KHz to 1 MHz is shown in Figure 3.54.

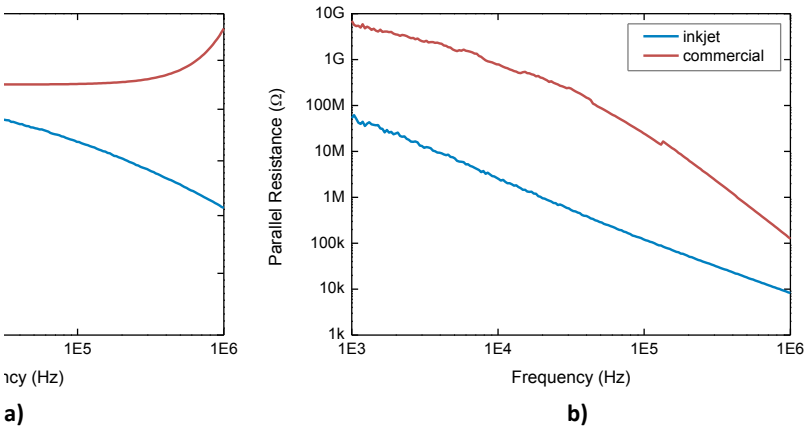


Figure 3.54. a) Capacitance as a function of frequency, b) parallel resistance as a function of frequency for the inkjet printed capacitor and a commercial 390 pF capacitor.

The measured value of the capacitance is 385,9 pF at 1 kHz, 381 pF at 10 kHz, 367.2 pF at 100 kHz and 342.7 pF at 1 MHz. However, for the inkjet printed capacitor, the capacitance begins to drop slightly after 1.3 kHz. The capacitance value of the inkjet printed capacitor reaches 342.7 pF at 1 MHz, a reduction of around 11.2%. But this value can be caused by an artefact because the low resistance at these frequencies can dominate the measurement. The measured value of the parallel resistance is 53.03 MΩ at 1 kHz, 2.5 MΩ at 10 kHz, 116.4 kΩ at 100 kHz and 8.24 kΩ at 1 MHz. The parallel resistance of the inkjet printed capacitor decreases as expected.

Figure 3.54 also shows a comparison with a commercial ceramic multilayer layer 390pF ceramic capacitor supplied by KEMET (Type C-series). The results show that up to 100 KHz there is no reduction in capacitance for the commercial capacitor because self-resonant frequency is around 320 MHz. Also, the reduction in capacitance of the inkjet capacitor is not significant.

An ideal capacitor has infinite parallel resistance. In practice, capacitors have imperfections which create parallel and series resistances. A finite parallel resistance occurs as a result of the small conductivity of the dielectric. Therefore, a small leakage current flows between the two electrodes. Ultimately, the capacitor will be discharged by the parallel resistance with a discharge time controlled by its value. Figure 3.54b shows the change in parallel resistance as a function of frequency. The initial resistance values are different for each device; however the parallel resistances of the commercial capacitor decrease faster. This results shows that the inkjet printed dielectric has a higher leakage current compared to a commercial capacitor. This higher leakage current could be because the inkjet printed layer may be less uniform compared to the ceramic capacitor.

We can conclude that a parallel plate flexible capacitor can be entirely fabricated using inkjet printing using low temperature processes (200 ºC for 12 minutes) on flexible substrates.

The key electrical parameters of the inkjet printed capacitor can be considered acceptable compared with the commercial ceramic multilayer layer capacitors of similar value (390 pF). However, the results show that the dielectric loss, leakage current and plate resistances are slightly higher in the inkjet printed capacitor. It is likely these differences could be improved with more uniformly printed layers or the addition of further printed layers to reduce the occurrences of pinholes in the printed layers.

3.3.3. Capacitor measurements over time

For proper integration in future electronic circuits, the electrical properties of the devices need to be stable over a long period of time. The high sensitivity of most organic materials to ambient conditions or environmental influences, such as oxygen, humidity, and temperature, creates a huge limitation on the performance and stability of devices. In the case of capacitors, device degradation is commonly manifested as a decrease of its parallel resistance, thus, losing its insulating properties.

The purpose of this section is to perform a stability analysis over the time in an inkjet-printed capacitor, being exposed to ambient air and light. Devices fabricated were tested over seven weeks. During that time, the devices were stored in typical ambient conditions, i.e. normal indoor light, temperature about 18-26ºC and relative humidity of 30-45%.

Temperature and humidity were recorded continuously. Figure 3.55a depicts the average temperature and humidity over the period.

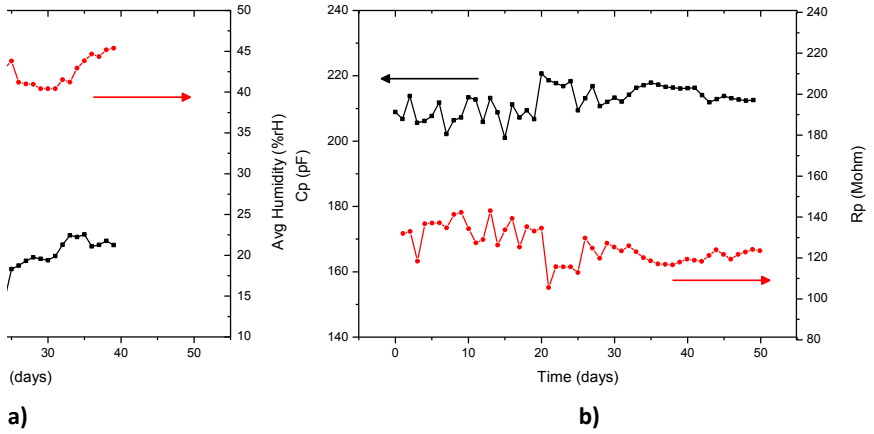


Figure 3.55. a) Average temperature and humidity during the period of measurement; and b) parallel capacitance and parallel resistance measured during 7 weeks.

From the graph, the change in humidity and temperature occurred from day 20th to 30th are easily observed as a change both in capacitance and parallel resistance revealing the sensitivity of c-PVP dielectric to environmental changes, especially to humidity.

Nevertheless, from Figure 3.55b shows good stability on both parameters although some slight changes due to moisture trapping.

3.3.4. c-PVP Dielectric layer optimization

In this section, the main goal is to reduce the leakage current on c-PVP dielectric using different approaches consisting of mix of (i) curing techniques, (ii) the use of drop lattices, (iii) different number of layers and (iv) drop spacing.

Two different approaches were followed. First one is related to process: the procedure of the curing and the use of soaking the sample with the same solvent of the dielectric after the curing of the two printed layers.

The second approach is related to printing conditions: playing with different drop spacings, drop lattices and dielectric area.

For these experiments the focus was to avoid increasing the number of printed layers to do not increase the thickness of the dielectric. Thus, to play with more than one layer we will use an approach already used in chapter 1 when different drop lattices were used for conductive lines. Thus, the approach is based on the idea that each layer of the c-PVP dielectric is deposited with a reduction of 50% of the drop density (checkerboard-like).

Moreover, the second layer is shifted an entire drop spacing value, producing a continuous layer with the superposition of the previous one.

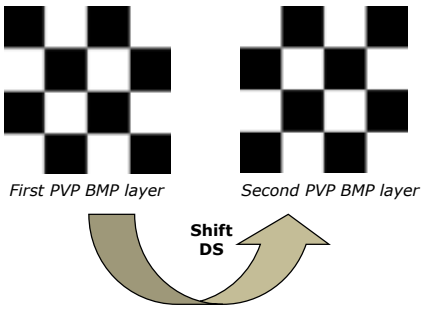


Figure 3.56. Bitmap for first layer of cPVP and bitmap for second layer of cPVP. Second bitmap was shifted an entire drop spacing to produce a continuous layer.

3.3.4.1. Dielectric improvement through curing process optimization

Two techniques have been evaluated on a first experiment. The first one is the curing procedure. Two different curing procedures are proposed. One is based on intermediate curing and, the other one is based on final curing. For intermediate curing, the temperature must be lower than the temperature of polymerization (150-200 ºC) to avoid the hydrophobic effects of c-PVP when a new layer of dielectric is printed on top of it. Curing at 100ºC to evaporate solvents does not activate the hydrophobicity of c-PVP.

The second technique is to soak the sample with the same dielectric solvent (ethanol) to later perform an additional curing. The soaking procedure is applied in order to remove the likely pinholes of the dielectric. Structures without soaking process were also fabricated in order to compare the effect of this procedure.

The diagram on Figure 3.57 shows the different procedures proposed.

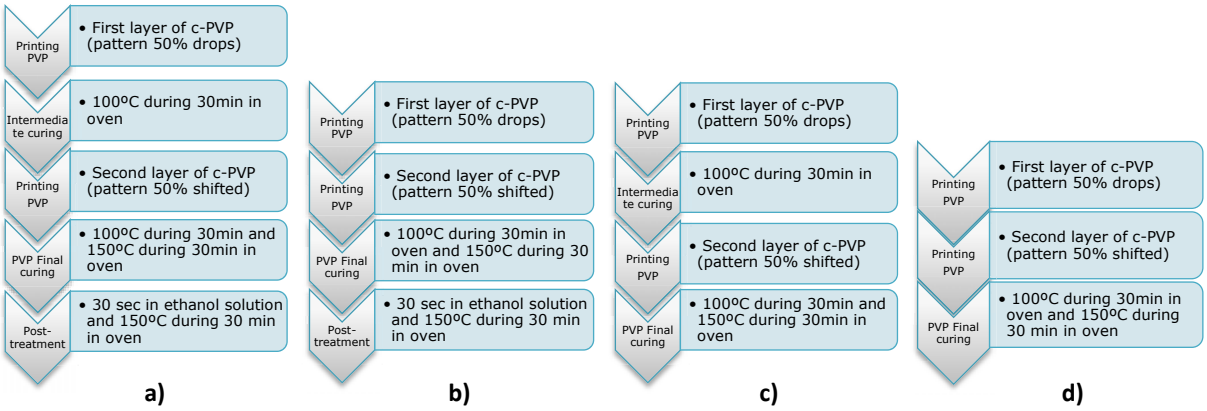


Figure 3.57. C-PVP and curing process for samples: a) with soaking process and intermediate curing; b) with soaking process and without intermediate curing; c) without soaking process and intermediate curing; and d) without soaking process and intermediate curing.

The addition of new steps is not optimal from a point of view of a simple process. Figure 3.57a shows the process descriptions with intermediate curing and soaking.

Following this curing process and for this first experiment, the design in Annex C.6 was used. The design contains a group of individual capacitors with increasing areas: 2.25 mm^2 (for small capacitors) and 9 mm^2 (for medium capacitors).

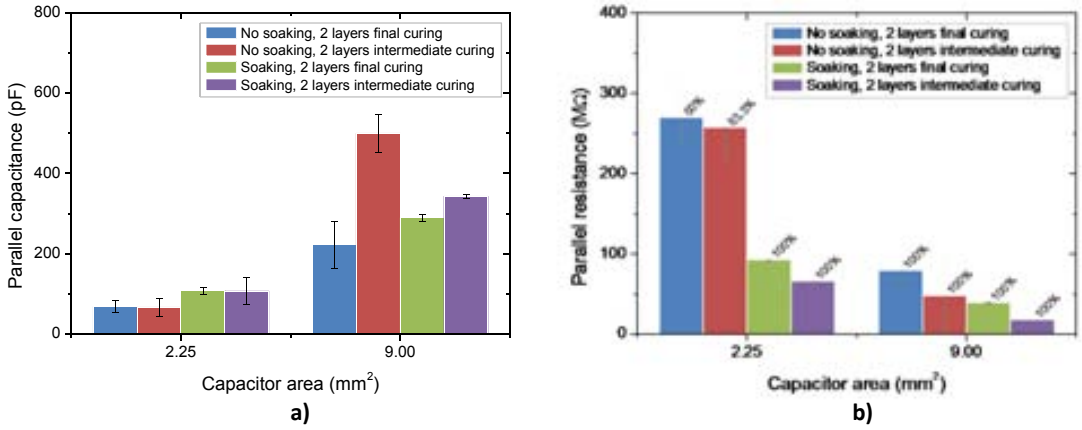


Figure 3.58. a) Parallel capacitance and b) parallel resistance as a function of the capacitor area and depending on (i) soaking process (ii) no soaking process, (iii) intermediate curing and (iv) final curing.

Figure 3.58 shows the parallel resistance measured for the different processes applied. As it can be observed, soaking dramatically reduces the parallel resistance thus increasing leakage current. Moreover, the intermediate curing does not improves the dielectric resistivity, so, this time-consuming intermediate process can be discarded too. Thus, a printed layer without soaking and intermediate curing is the best option.

From the graph we can observe an additional effect such as the parallel resistance appears as a function of the dielectric area. This effect will be studied more in detail in the following experiments.

3.3.4.2. Dielectric improvement by changing the printing conditions

Based on the previous results a new design was prepared with capacitors having the same sizes than the OTFTs that will be fabricated in the next chapter. The objective is to improve the OTFT dielectric area in parallel of the capacitor devices.

The dimensions used are shown in Table 3.1 and corresponds to the transistors labelled T40/10E3, T40/20E3, T40/30E3, T40/30E3sl and T40/40E3 fabricated in Chapter 4. The dimensions of metal1 are omitted but they are 80 µm larger in all directions than those from metal2.

Table 3.1. Parallel plate dimensions of fabricated capacitors

Capacitor active area [µm]	Dielectric layout pattern [µm]	Metal2 layout pattern [µm]
0.89 mm²	$d.b$ = 2680; $d.a$ = 1140	$m2.b$ = 2120; $m2.a$ = 420
1.74 mm²	$d.b$ = 2680; $d.a$ = 1540	$m2.b$ = 2120; $m2.a$ = 820
2.59 mm²	$d.b$ = 2680; $d.a$ = 1940	$m2.b$ = 2120; $m2.a$ = 1220
2.71 mm²	$d.b$ = 1680; $d.a$ = 3140	$m2.b$ = 1120; $m2.a$ = 2420
3.41 mm²	$d.b$ = 2680; $d.a$ = 2340	$m2.b$ = 2120; $m2.a$ = 1620

In order to reduce the dielectric thickness to increase the capacitance per area unit, the c-PVP drop spacing was modified. Additionally, for a drop spacing of 20 µm two different designs were used: one with one layer and a second one with two layers each one using a lattice of 50% and shifting the pixels.

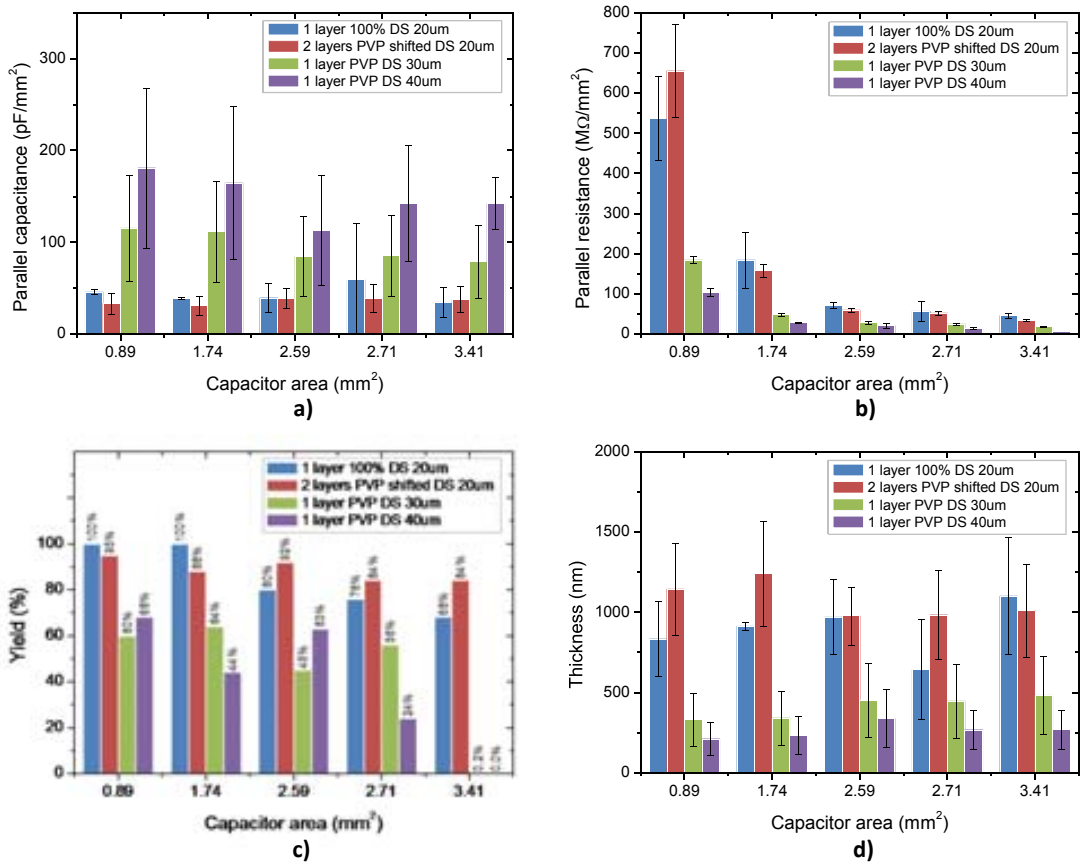


Figure 3.59. a) Parallel capacitance; b) parallel capacitance; c) yield and d) thickness of c-PVP as a function of the capacitor area and depending on (i) number of c-PVP layers, (ii) DS of the c-PVP (iii) drop lattice of the c-PVP.

Figure 3.59a shows the analysis of capacitance per area versus OTFT dielectric areas defined in Table 3.1. In the figure it can be observed a slight reduction of capacitance with the increase of capacitor area. Although the use of drop spacings of 30 or 40 μm could seem the best option, Figure 3.59b shows that the increase of drop space also reduces the parallel resistance, thus increasing tha leakage current in the MIM structure.

The reduction of yield is still more significant, as shown in Figure 3.59c. Using drop spacing of 30 and 40 μm results in lower yields, especially for large areas. Using 20 μm drop space produces yield higher than 70-80%.

Figure 3.59d shows the thickness measured for the different printing approaches considered. It is not possible to observe any thickness increase for large capacitor areas due to the large deviation in measuring thickness . An additional experiment with different capacitor structures is required.

3.3.5. Analysis of the dielectric thickness versus area

A new experiment was planned to assess the effect of the area on the dielectric thickness. All the capacitors in the design of the Annex C.7, have the same parallel plate area and we played with two different design parameters, as depicted in Figure 3.47:

- The extension between metal layers (*metal1* to *metal2* extension) decreasing from top to bottom. Rows labelled with letters have the same dielectric area.
- The dielectric area (*diel1* to *metal2* extension) decreasing from left to right. Columns labelled with numbers have the same dielectric area.

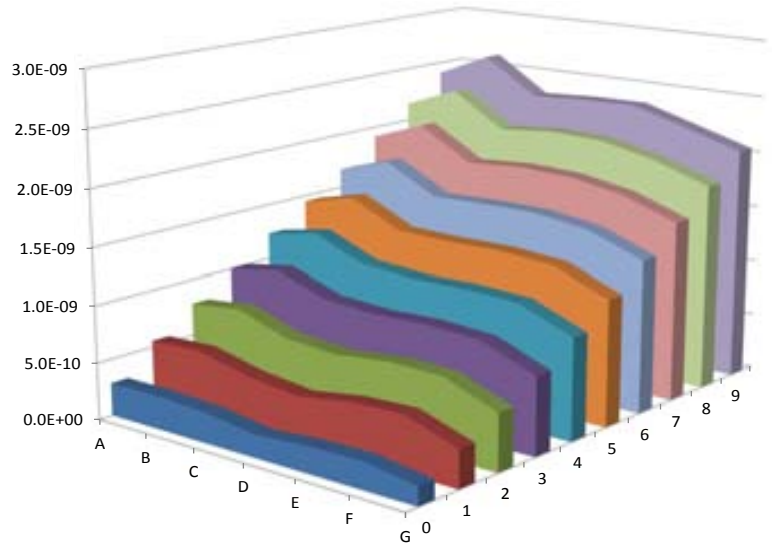


Figure 3.60. Capacitance as a function of the dielectric area and parallel plate overlap. From 0 to 9 the dielectric area is reduced, and from A to G the parallel plate overlap is reduced.

Figure 3.60 shows clearly a reduction of the capacitance with the increase of the dielectric area deposited meaning that large dielectric areas have lower capacitances than small areas. This implies that we can control the dielectric thickness by controlling the pattern of the dielectric layer. This effect is due to the fact that the change in the dielectric area implies a change of the equilibrium between coffee ring effects and Marangoni flow. For bigger areas the distance to the edges is larger and coffee ring effect is affecting less, thus, more material is kept in the center of the pattern.

It can also be observed in Figure 3.60, that the reduction in overlapping area (from A to G) implies a slight reduction of the capacitance due to the reduction of fringing effects.

3.3.6. Reliability study of c-PVP MIM capacitors

In order to study the reliability of the capacitors developed, a new design with a large quantity of devices was printed in order to obtain quantitative data for the statistical analysis and also, to study the scalability of the devices. The layout is shown in Annex C.8.

All the capacitors have some fixed parameters as shown in Table 3.2 based on the dimensions defined in Figure 3.48. Pads used are 1800 x 1800 µm.

Table 3.2: Fixed parameters of fabricated capacitors using layer stack depicted in Figure 3.47.

Digital pattern [µm]
m1.a = 1000
m1.c = 2300 up to 4300
m1.d = 620
d.a = 4000
m2.a = 1320
m2.c = 2500 up to 4500
m2.d = 620

The design contains 140 capacitors with 5 different sizes having effective areas of 3, 4, 5, 6 and 7 mm^2. 113 capacitors were working properly resulting in an average yield of 80%. Non-working devices were mainly related to printing problems not to materials.

As shown in Table 3.3, the height of *metal1*, *diel1* and *metal2* is constant, and only the pattern width is enlarged.

Table 3.3. Parallel plate dimensions of fabricated capacitors

Capacitor active area [µm]	Digital pattern [µm]
3 mm²	*m1.b* = 3000; *d.b* = 3160; *m2.b* = 5000
4 mm²	*m1.b* = 4000; *d.b* = 4160; *m2.b* = 6000
5 mm²	*m1.b* = 5000; *d.b* = 5160; *m2.b* = 7000
6 mm²	*m1.b* = 6000; *d.b* = 6160; *m2.b* = 8000
7 mm²	*m1.b* = 7000; *d.b* = 7160; *m2.b* = 9000

The characterization of those devices was performed by using a LCR meter (Agilent E4980A) at 1 KHz. Following graphs shows the average of Cp-Rp measurements per capacitor active area.

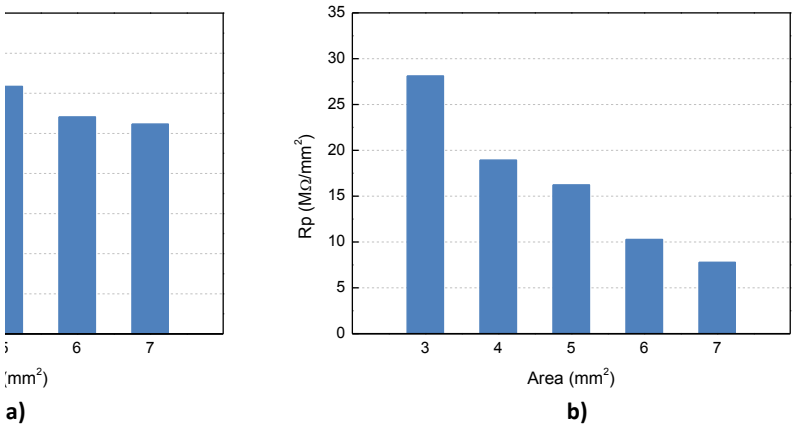


Figure 3.61. a) Parallel capacitance and b) parallel resistance of 113 working capacitors as a function of the capacitor active area.

The average parallel capacitance per area obtained is 59.9 pF/mm² at 1 KHz, with a reduction of around 18,4% if area is duplicated (comparing capacitors of 3 and 6 mm²). The average parallel resistance per area obtained is 16.3 MΩ/mm² at 1 KHz, with a reduction of around 63,3% if area is duplicated (comparing capacitors of 3 and 6 mm²). The decrease of the resistance can be attributed to the presence of pinholes, not only for the thickness reduction.

The analysis of Cp or Rp per (active) area for the complete set of capacitors produces the histograms shown in Figure 3.62. Graphs reveals that the dispersion is lower in capacitance (±50% variation) from the average value (Figure 3.62a) than in resistance (up to 350% variation as shown in Figure 3.62b).

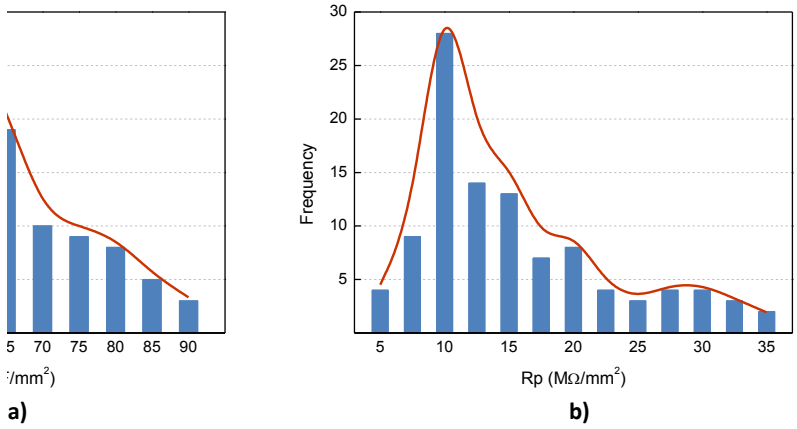


Figure 3.62. Histogram of: a) parallel capacitance and b) parallel resistance.

3.4. Circuits using passive devices

The all-inkjet organic capacitor and resistor developed in the previous sections have been applied to RC filter circuits as a proof of concept of the technology.

3.4.1. RC circuit

Figure 3.63 shows the design of an RC circuit in which the resistor was made of PEDOT:PSS and the capacitor of c-PVP as the ones fabricated and characterized before. Conductive glue (epoxy) was used to connect capacitor and resistor devices and to connect the RC circuit to a function generator and an oscilloscope. Figure 3.63 shows the RC filter circuit schematic and the testing set-up.

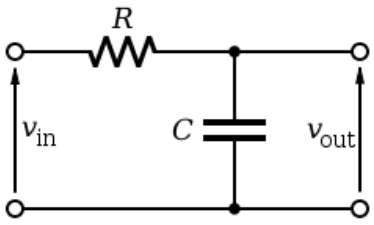


Figure 3.63. RC circuit schematic.

For the RC filter, the resistance is 25 KΩ and the capacitance is 27.75 pF leading a RC time constant of 0.675 μs. For the low-pass filter configuration, it is expected that the amplitude of the output voltage decreases when frequency increases and the amplitude of the input signal is kept constant.

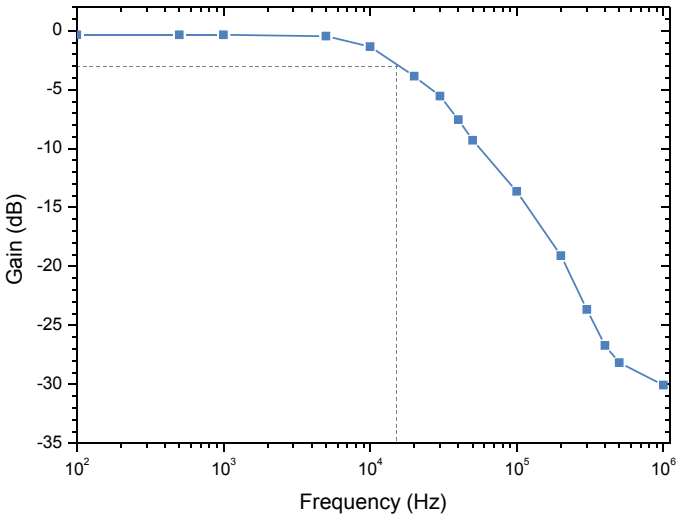


Figure 3.64. Experimental result of the gain vs. log (frequency) for the all-inkjet low-pass filter.

Figure 3.64 shows the experimental results of the low-pass output frequency characteristics with a cut-off frequency of 14 KHz.

In addition, when the input signal is a square wave the transient characteristic of the output signal is an integral curve. Figure 3.65 shows the experimental results of the low-pass filter transient response. The signal input is a square wave at a 10 KHz frequency and amplitude of 15V peak-to-peak.

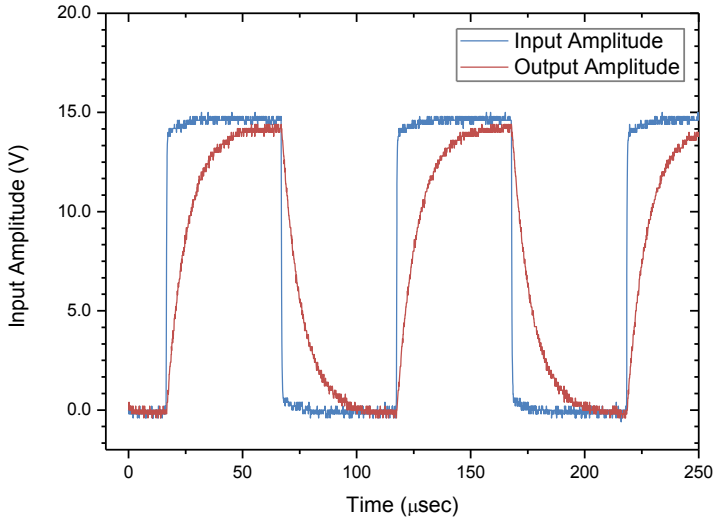


Figure 3.65. Experiment result of transient characteristic for the all-polymer low-pass filter at 10 KHz.

Experimental results are in agreement with what we expect and prove that the RC filter is fully functional. The all-inkjet organic capacitor and resistor demonstrated here can further find its application to the low-cost all-organic circuit industry [36][128].

3.5. Summary and conclusions

We have reported about the manufacturing of different passive electronic devices using S2S inkjet printing. In all cases reported here, the devices were fully inkjet-printed. The focus was set on conductive lines, resistors and capacitors. We have developed manufacturing process operations for inkjet printing and post-treatment methods based on the materials evaluated. Layers and their geometries were designed and characterized. For the geometries, printing tolerances were taken into account related to the employed printing system.

Conductive lines were characterized as a first step towards the fabrication of more complex devices. Conductive lines made of silver nanoparticle ink are widely used in all the devices developed on this thesis work, so its characterization and optimization was mandatory in order to improve all the devices considered.

A high amount of linear resistors was fabricated and all the devices were characterized. Two different strategies were taken in account. First one, by using semi-sintered silver nanoparticle ink gave us good results and became a promising and simple manufacturing process as it only uses a single material. A low curing temperature and reduced curing times assures a sheet and contact resistance in the expected range.

But resistors made by semi-sintered metallic inks have the drawback that its electrical properties can also change by direct resistive heating, thus limiting the density of current flowing through the device. If current exceeds the limit, a non-reversible change occurs in the resistance. So, the rapid electrical sintering (RES) method has been demonstrated for the fabrication of inkjet printed programmable Write-Once-Read-Many (WORM) memories.

Organic resistors made by using PEDOT:PSS were also developed. Different fabrication strategies to improve line homogeneity and reduced variability were taken in account. Since one of the key problems in organic polymeric films is their affectation by oxygen and moisture, resistors protected with a c-PVP layer present much better behavior.

Finally, MIM capacitors have been implemented as a first step towards the fabrication of OTFTs in the next chapter. C-PVP was used as a dielectric and several experiments were performed in order to optimize its deposition to obtain suitable electric devices in terms of dielectric strength, yield, variability and reliability. Nevertheless, the results in this work show that the c-PVP ink still has several disadvantages. Although electrical characteristics are satisfying, film formation is very complex due to the strong coffee-ring effect.

As a summary, resistors and capacitors using different techniques and materials have been fabricated and characterized as well as RC filter circuits to demonstrate its feasibility and maturity.

4. FABRICATION OF INKJET-PRINTED ORGANIC THIN FILM TRANSISTORS

The development of robust processes for manufacturing Organic Thin Film Transistors (OTFTs) circuits is a challenge due to the sensitivity of organic electronic materials, material compatibility limitations and printing technologies restrictions. The device layout, architecture, and material selection have a strong influence on the choice of processing techniques and the fabrication procedure. In this work, we have been focusing our effort on inkjet printing of OTFTs. Several examples of all-inkjet printed OTFTs can be found in literature [129][39][53][30][28][71]. This chapter explores various aspects of OTFT fabrication, concretely the design, fabrication and material characterization of OTFTs in sheet-fed configuration (S2S) by using inkjet printing technologies.

Although the OTFT device structures appear relatively straightforward, its implementation and fabrication is difficult. One of the major challenges when developing a fabrication process for OTFTs is to address the sensitivity to the ambient conditions of the functional organic layers and the compatibility between various material layers involved in building the device to ensure minimum chemical interaction and process-induced material degradation.

Although device materials and structures may be identical in design, device performances can differ significantly according to the processing method. Charge carriers move through the semiconducting layer near the dielectric layer. Therefore the semiconductor–dielectric interface characteristics and the molecular ordering of the semiconductor must be optimized to achieve a high performance [28][130]. Dielectrics must be uniformly deposited to reduce the gate leakage current. Source/drain electrodes should be sufficiently conductive and have an appropriate work function for the effective injection of charge carriers. Meeting these requirements would produce functional transistors and facilitate the design of OTFT circuits manufactured by printing processes. The mere application of a printing method to OTFT fabrication does not necessarily imply the successful preparation of properly functioning devices.

As OTFT printing has become significant in industry, transistors became popular among researchers working on inorganic and organic electronic devices. Several review articles covering printing methodologies are available [30][131][29][132].

As in previous chapters, many inks with different functional properties of conductors, semiconductors and dielectrics were evaluated, and finally a set of materials was selected for the fabrication of the devices. The device structures and geometries were defined taking into account the printing tolerances related to the employed printing systems.

In addition to the fabrication and electrical characterization of the OTFTs, some test vehicles were designed and characterized to evaluate electrical and physical parameters. The test vehicles were used to allow the determination of technology parameters by means of electrical and morphological characterizations.

This chapter presents an overview of OTFT technology. Fundamental properties of organic semiconductors are reviewed in the following section as the key material for building the device. Moreover, the basic operation and characteristics of the OTFT is discussed. Materials used, structures designed and physical characterization of OTFTs are also described in this chapter.

4.1. Introduction

Due to the invention of the transistor around the middle of the last century, inorganic semiconductors based on Si or Ge took the role of dominant materials in electronics. At the beginning of the 21th century the omnipresence of inorganic semiconductor electronics is absolute.

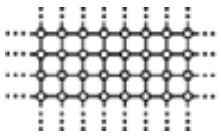
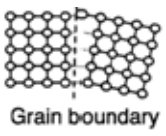
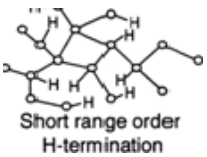
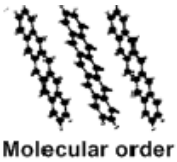
Until to 40 years ago, organic compounds and polymeric materials (also known as plastics) were regarded as inactive substrates and insulating materials.

Since the 1990s, conducting polymers have been attracted the focus of a big technological and scientific effort for FOLAE (Flexible, Organic and Large Area Electronics) device application due to the promise of their low cost and easy processing. Since the 1970s, the synthesis and controlled doping of conjugated polymers established an important step with the discovery of electrical charge carrier transport in polymers which was honoured with the Nobel Prize in Chemistry in 2000. Depending on their behaviour, polymers can behave as semiconductors (referred to as "organic semiconductors"), or they can be highly doped to behave as conductors [133]. Transistors based on organic semiconductors as the active layer to control current flow are commonly referred to as Organic Thin Film Transistors (OTFTs), or sometimes Organic Field Effect Transistors (OFETs). One example of the successful of the conducting polymer is the Organic Light-emitting devices (OLEDs) that suffer a rapid market growth that let to its recent integration in commercial products.

Regarding the nature of the organic materials, OTFTs cannot compete with silicon-based transistors in terms of switching speed or integration density but provide prospects of considerably reducing fabrication costs, allowing large-area manufacturing (i.e. direct application of electronic structures onto large substrates), or implementing mechanically flexible integrated circuits.

Table 4.1 summarizes different kinds of crystal structures and their carrier mobility.

Table 4.1. Different kinds of crystal structure and theirs carrier mobility.

	Crystalline Si	**Poly-crystalline Si**	**Amorphous Si**	**Organic Semiconductor**
Crystal structure				
Carrier Mobility	400 $cm^2/V \cdot s$	50~100 $cm^2/V \cdot s$	0.5~1 $cm^2/V \cdot s$	10^{-3}~1 $cm^2/V \cdot s$

All these advantages can generate applications based upon OTFTs where fabrication costs or flexibility are more important concerns than e.g. switching speed of the transistors. One example is the implementation of extremely low-cost radio-frequency identification (RFID) tags. Fabrication costs below one cent would boost application of RFID devices e.g. in shopping.

The performance of organic semiconductors has improved to the point where they are being considered to replace amorphous silicon in thin film transistors (TFTs) for active matrix display backplanes [134][135]. Semiconductor polymers offer the opportunity for low cost manufacturing of display backplanes because they can be deposited from solution at room temperature. OTFTs with mobility of about 1 $cm^2/V \cdot s$ have been widely studied [134][136] and materials with mobility ~0.5 $cm^2/V \cdot s$ by inkjet printing have been reported, approaching the mobility of a-Si [137]. The On-Off current ratio in the polymers can exceed 10^7, which meets the requirements for display backplanes, and the Threshold voltage is also suitable, although it is usually larger than in a-Si. However, long term stability of OTFTs has not been demonstrated yet. Stability to both atmospheric chemical exposure and electrical stress are of concern [138].

Prior to the discussion of the fabrication of all-inkjet printed transistors, it is necessary to review the basics of OTFTs. Therefore, in the following section, carrier transport and contact barriers in these devices are discussed at first, then various structures of OTFTs will be reviewed. Finally, basic operations of OTFTs will also be introduced.

4.2. OTFT Operation and characteristics

In organic electronics, the term of MOSFET (Metal-Oxide-Semiconductor FET) is erroneous because of the gate dielectric insulator is not an oxide. The MOSFET structure was initially developed for amorphous silicon transistors [139].

Generally speaking, the OTFT MISFET (Metal-Insulator-Semiconductor FET) is composed of three electrodes (gate, source and drain). The Source (S) and Drain (D) electrodes directly contact the semiconductor, whereas the Gate (G) electrode is separated from semiconductor by a dielectric layer. The gate turns the device On and Off with an applied voltage, and thus controls the current flow (I_{DS}) in the semiconductor between the source and drain electrodes.

Without any applied gate voltage (V_G), the intrinsic conductivity of most OSC materials is low. When a source-drain voltage (V_{DS}) is applied between two electrodes, the device is in the Off state and a negligible current can flow through the semiconductor thin film. When a positive (n-type) or negative (p-type) voltage is applied to the gate (V_G), a potential gradient appears in the capacitor structure, and the amount of charge is accumulated at the dielectric-semiconductor interface. Those charges are mostly mobile and lead to the formation of a conducting channel between source and drain electrodes in response to the applied V_{DS} with a conductance directly related to V_G. Then, the transistor is in its On state.

A basic scheme is shown in Figure 4.1 where V_G and V_{DS} are the applied gate and source-drain voltages, respectively.

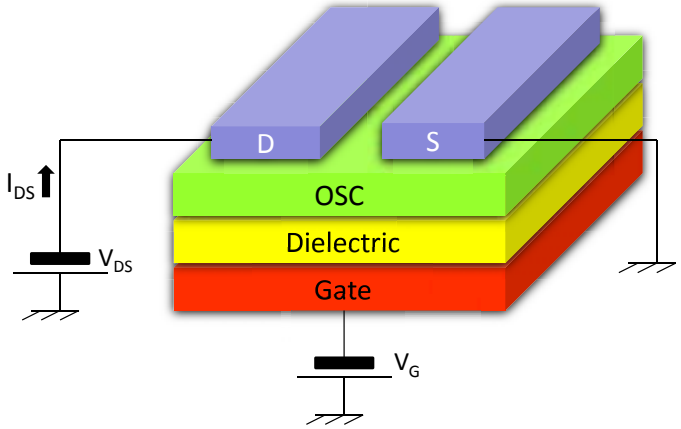


Figure 4.1. Schematic view of a bottom-gate thin film transistor.

Therefore the controlled current takes place in the organic semiconductor. There exist both p-type and n-type semiconductors, and also ambipolar semiconductors showing both behaviours. Nevertheless, the most common organic semiconductor used is p-type due to its higher performance and ambient stability, and they are still improving its performance. For these reasons, along this thesis, a p-type semiconductor is considered.

The TFT structure is well adapted to low conductivity materials, and is currently used in amorphous and polycrystalline silicon transistors [47]. There are a number of functional and structural differences between OFETs and the conventional metal-oxide-semiconductor field-effect-transistor (MOSFET) used in crystalline silicon Integrated Circuits (ICs). First, there is no depletion region in OTFTs to isolate the device from the substrate. Low Off-currents (I_{OFF}) in OTFTs are only guaranteed by the low conductivity of the semiconductor due to the inexistence of a blocking p-n junction near the contacts to prevent the current from flowing between source and drain when the channel is not formed. As a result, the Off-current (I_{OFF}) in OTFTs is relatively high compared to MOSFETs [140].

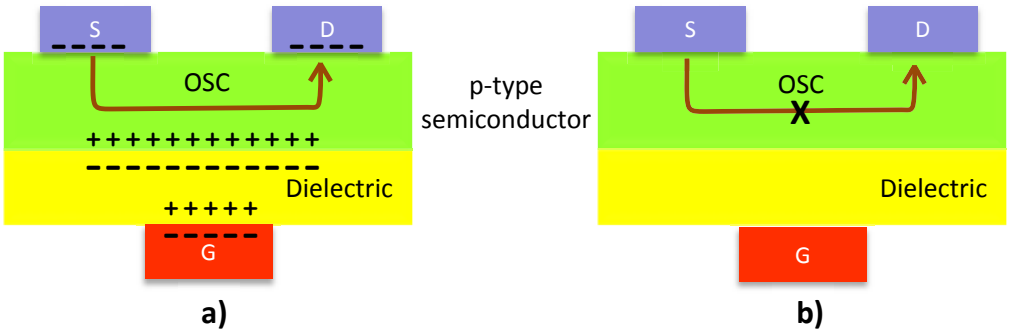


Figure 4.2. Simplified illustration of the operation of a TFT with p-type semiconductor; a) ON state ($V_G < 0$); b) OFF state ($V_G = 0$).

A second important difference is that the Organic FETs (OFETs) operates in the *accumulation regime* while MOSFET operates in the *inversion regime*. The OTFT gate-dielectric-semiconductor structure operates like a capacitor. Ideally, the application of a gate voltage induces an equal charge of opposite polarity in the semiconductor near the dielectric/semiconductor interface, as shown in Figure 4.2a. This charge forms a conducting channel of the same polarity as the majority charge carrier injected into the semiconductor come from source to the drain by applying a bias to the drain electrode. Thus, the conductance of the channel is proportional to the gate voltage and the transistor is said to be in ON state.

When an OTFT is in the Off state (Figure 4.2b) the gate voltage does not create a conduction channel in the semiconductor/dielectric interface which implies, ideally, no current can flow between the source and drain electrodes, even with an applied V_{DS} bias [133].

Figure 4.3 shows typical electrical characteristics of a p-type OTFT. At low drain voltages, the current increases linearly with drain voltage, according to the Ohm's law. When the drain voltage approaches the gate voltage, the voltage drop at the drain contact falls to zero, and the conducting channel is pinched off. This corresponds to the so-called *saturation*

regime, and the current, ideally, becomes independent of the drain voltage. The operating mode of the organic-thin film transistor produces output and transfer current-voltage characteristics as shown in Figure 4.3a and Figure 4.3b, respectively.

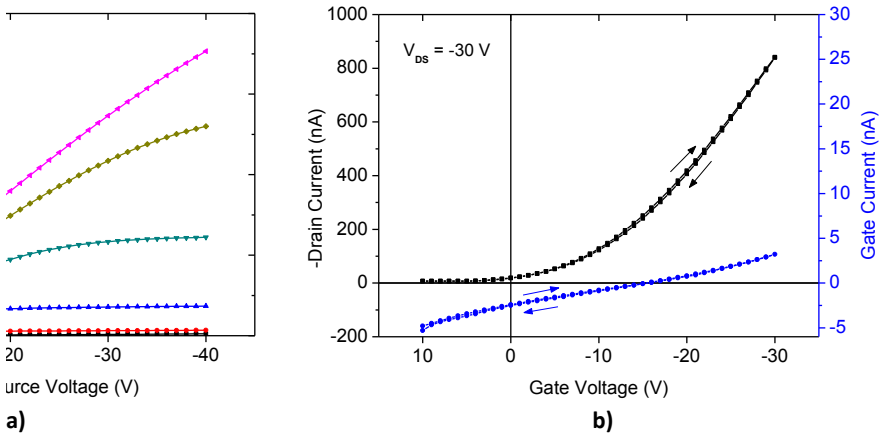


Figure 4.3. Typical electrical characteristics of a p-type OTFT: a) transfer curve (I_{DS}-V_{GS}) showing linear and saturation regime; b) output curves (I_{DS}, I_{GS}) versus gate voltages.

The highest occupied molecular orbital (HOMO) consists of bonding states of the π-orbitals with filled electrons, and is analogous to the valence band in silicon. The lowest unoccupied molecular orbital (LUMO) consists of empty higher energy anti-bonding (π^*) orbitals, and is analogous to the conduction band. The energy difference between the HOMO and LUMO defines the band-gap energy (E_G) [133]. E_G depends on the chemical structure of the repeating unit, and generally decreases if the chain length increases. The E_G of conjugated polymers is typically in the range of 1-4eV. Due to the disordered nature of organic materials, conduction mainly takes place via phonon-assisted hopping and polaron-assisted tunnelling between localized states; this is in contrast to crystalline semiconductors (e.g. silicon) where conduction occurs in energy bands through delocalized states.

The operating principle of FETs based on p-type organic semiconductors can be demonstrated by the simplified energy level diagram of Figure 4.4.

If there is no gate voltage applied (Figure 4.4a), the organic semiconductor, which is intrinsically undoped, will not show any current. The current between source and drain electrodes will be relatively small owing to the high resistance of the organic semiconductors and large distance between source and drain contacts [141]. When a negative gate voltage is applied (Figure 4.4b), if the Fermi level of the source/drain metal is close to the highest occupied molecular orbital HOMO level of the organic semiconductor, then positive charges can be extracted by the electrodes through the application of a voltage, V_{DS}, between the source and drain.

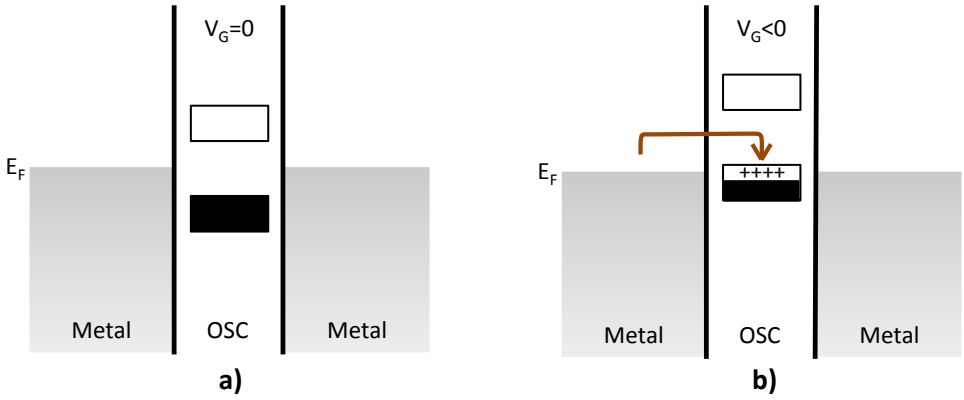


Figure 4.4. A diagram view of energy level of p-type FET: a) no gate voltage applied and b) with gate voltage applied.

Despite the fundamental differences, the characteristic equations of the inorganic MOSFET transistors can be applied, as a first approximation, also to an organic MISFET, that is

$$_{DS_{lin}} \quad _{FE}C_i \left(\frac{W}{L}\right)\left(V_{GS} - V_T - \frac{V_{DS}}{2}\right)V_{DS} \qquad \textit{Eq. 4.1}$$

in the linear zone, where $V_{DS} < (V_{GS} - V_T)$ and

$$_{DS_{sat}} \quad - \quad _{FE}C_i \left(\frac{W}{L}\right)(V_{GS} - V_T)^2 \qquad \textit{Eq. 4.2}$$

in the saturation zone, where $V_{DS} \geq (V_{GS} - V_T)$.

The parameter L is the channel length of the transistor from source to drain in the direction of the current flow, W is the channel width of the transistor, C_i is the capacitance per unit area of the insulating layer, and μ_{FE} is the field effect mobility of the semiconductor layer (hereinafter referred to as just). V_T is the Threshold voltage, V_{GS} the gate-source bias, and V_{DS} is the drain-source bias. The Threshold voltage (V_T) is the V_G corresponding to the opening of the conduction channel.

The operation and performance of the OTFTs are generally governed by two key mechanisms: (i) charge transport in the semiconductor layer and (ii) charge injection and extraction at the source/drain contacts. Field-effect mobility (μ_{FE}) is often used to characterize the efficiency of the charge transport in the device, and contact resistance (R_C) provides a measure of charge injection efficiency in an OTFT.

The mobility is also directly related to the switching time of the device. The slope of the $I_{DS}^{1/2}$ versus V_G is related to the mobility for the saturation region due to the square law relation. For the case of the lineal region, the slope I_{DS} versus V_G is related to the mobility. Another important parameter is the On/Off drain current ratio, which is the ratio between the current in the accumulation mode and the current in the depletion mode.

Note that the mobility is commonly used as a figure of merit for reporting OTFT performance. However, the accurate extraction and modelling of the mobility remains controversial due to different reasons, and as a result, it does not give a precise representation of OTFT performance [133].

4.2.1. Introduction to Organic Semiconductors

Organic semiconductors are the most important materials for the functional layer of organic transistors. The operation and performance of OTFTs basically depends on the characteristics of the active semiconductor layer. In particular, the mobility of the device is related to the efficiency of charge transport through the semiconductor channel.

The definition of what is exactly an organic material is not strict, but generally is defined as those materials that contain carbon [142]. Then organic semiconductors are molecules consisting of a repetition of carbon based compounds with low molecular weight with a specific electrical activity. Depending on the number of repetition units, organic semiconductors belong to one of two categories: oligomers or polymers. An oligomer is a compound with a number of repetitions usually less than 10 to 15 (short chain). Most oligomers cannot be deposited from solution because they are not very soluble in common solvents [143] and usually, they are deposited by vacuum deposition and other conventional technologies. Semiconducting oligomers show superior electrical performance (e.g. switching speed, mobility…) when compared to semiconducting polymers. A popular semiconducting oligomer is pentacene, shown in Figure 4.5a. On the other hand, a polymer is a compound with a higher number of repetition units (long chain). More precisely, a polymer can be defined as a compound where adding a new repetition unit will not alter its chemical and electrical behaviour [133]. In order to make polymers soluble in a variety of solvents and provide a continuous film with properties, side chains are chemically attached to the polymer chain to allow deposition e.g. by printing methods. A popular p-type organic polymeric semiconductor is called polymer poly(3-hexylthiophene) (P3HT) as shown in Figure 4.5b.

The semiconducting materials used in this work are polymeric compounds.

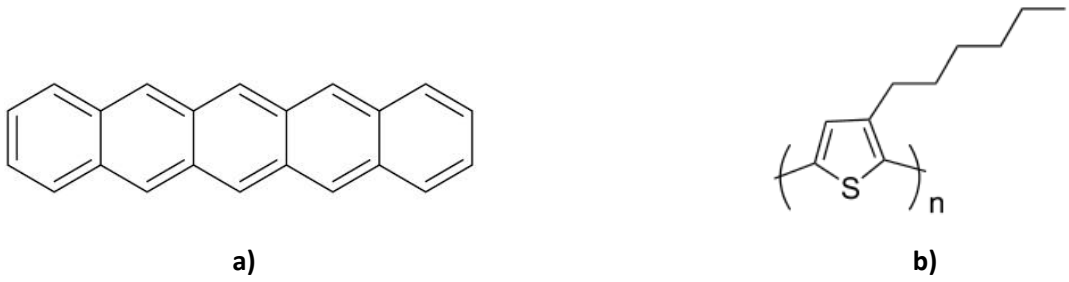


Figure 4.5. a) Pentacene chemical structure as an example of oligomers; b) P3HT structure, one of the most popular organic polymeric semiconductors.

Most conductive polymers in their neutral state are wide-band-gap semiconductors with very low conductivities. Doping is required to increase electrical conductivity, and oxidation and reduction reactions are used to obtain p-type (electron removal) or n-type (electron addition), respectively [133]. These doping processes generate mobile charge carriers, which move in an electric field, giving rise to electrical conductivity. In most cases, conductive polymers are doped by oxidative reactions; thus, p-type conductive polymer materials are more common, with hole as the majority transport carriers.

Highly conjugated organic materials can work as semiconductors because of their strong π-orbital overlap. When an electron is added or a hole is injected, the resultant charge becomes delocalized across the conjugated system. This injected charge acts as a carrier for current conducting through the molecule and through the organic semiconductor thin film.

4.2.2. Charge transport mechanism in organic semiconductors

The free-electron approximation considered in crystalline materials is not applicable for organic semiconductors because the carriers are not as delocalized as in crystalline ones.

One of the most important discussions still active is the nature of the conduction of charge in organic semiconductors. There are two main theories regarding the conduction mechanism.

One is based in the idea that conduction consists of hopping between localized states. This idea centred on the molecular aspects find many followers around chemists and conduction is considered a perturbation to the system. On the other side, the solid-state-physicists approach treats the materials like a normal semiconducting material and using the concept of conduction and valence bands to describe the electronic states of the material. The molecular properties are then treated as a perturbation [142].

Thereby, a variety of mechanisms such as Variable Range Hopping (VRH) and Multiple Trapping and Release (MTR) among others are also used to model the charge transport in

non-crystalline materials. In this section we will focus on the hopping transport since it is more common for organic semiconductors.

4.2.2.1. Hopping transport in organic semiconductors

In well-ordered inorganics, such as single-crystal Si, the delocalization of electrons over equivalent sites leads to a band-type mode of transport, with charge carriers moving through a continuum of energy levels in the solid. Band transport is not applicable to disordered organic semiconductors, where carrier transport takes place by hopping between localized states and carriers are scattered at every step [142]. Figure 4.6 shows this concept of conduction in inorganic and organic semiconducting materials.

Alternative trap states are generated by structural defects as HOMO/LUMO levels may vary from molecule to molecule. The exact energy position of the HOMO/LUMO level is not determined by the chemical structure of the molecule itself but also by the electronic polarisation of its surrounding. Structural imperfections will lead to a fluctuating surrounding (and in the case of polymers to a fluctuating conjugation length).

In inorganic semiconductors the band gap (energy between conduction and valence bands), is rather small, in the order of 1 eV, while in organic semiconductors this band gap is much larger up to 2-3 eV. However, this large band gap justifies the existence of deep levels, causing the electronics processes to be slower. If a midgap trap in silicon can have a relaxation time in the order of microseconds, in the organic materials can be in the order of tens of kiloseconds (also measured in hours) [142]. This makes organic materials notably slow.

Gate voltage dependent mobility is often observed in organic semiconductors. This is caused by the fact that, as the gate voltage increases, injected charge-carriers tend to fill the traps and transport improves. This behaviour is described by the multiple trapping and release (MTR) model.

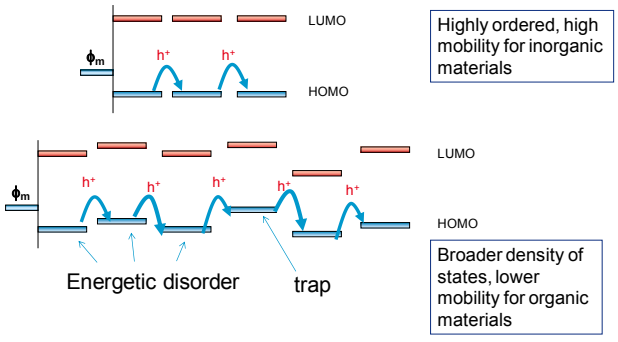


Figure 4.6. Energetic states for organic and inorganic material.

The nature of bonding in organic semiconductors is fundamentally different from the inorganic materials. Organic molecular crystals are van der Waals bonded solids with weaker interaction potential (molecule-molecule and molecule-substrate) as compared to covalent bonded semiconductors like Si or AsGa. This difference implies mechanical and thermodynamic properties like reduced hardness, lower melting point and much weaker delocalization of electronic wave functions among neighbouring molecules. Polymers are slightly different as the morphology of polymer chains can lead to improve mechanical properties. Response to strain is generally different what produces that more "disorder" can be observed in those systems.

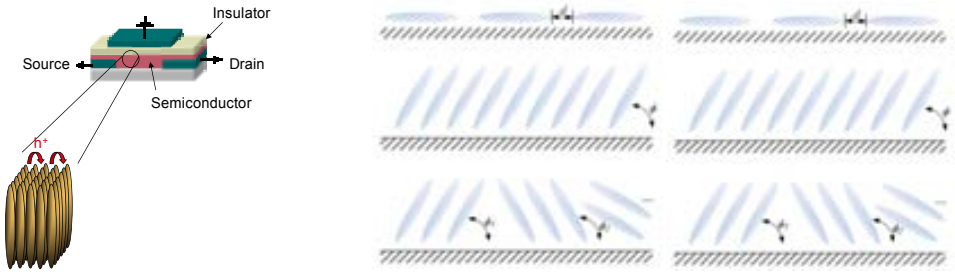


Figure 4.7. a) Hopping transport in organic semiconductors; b) possible molecule orientations and disorder.

The alignment of the polymer chains relative to the electrodes and the OSC-dielectric interface plane of an OTFT is also important, as shown in Figure 4.7b. The disorder in the film together with polymer defects stops or reduces the conductivity, since the charge carrier transport mechanism in organic semiconductors is hopping transport for polymers films.

4.2.3. Functional Interfaces

In recent years, it was assumed that the electrical response is not only determined neither by the quality of the chemical structure or the purity of the organic semiconductor material. The identification of the role of the interfaces in determining devices performances was a key discovery that promoted many fundamental studies on the interface physical properties and characteristics [141].

4.2.3.1. Metal-Organic Semiconductor interface

Metal-semiconductor contacts are an obvious component of any semiconductor device. One of the most important factors affecting the electrical properties of a device is the charge injection that in OTFT happens at the organic semiconductor-metal interface. Depending on the difference between work functions the problem is treated as a (1) Mott-Schottky barrier (rectifying contact) since there is a large mismatch between the Fermi energy of the metal

and semiconductor thus leading to poor charge injection or as a (2) ohmic contact. A proper choice of materials should provide a low resistance ohmic contact to have a good carrier injection [142].

4.2.3.2. Dielectric-Semiconductor interface

The crucial process of charge accumulation and transport takes place very close (few nm) to the interface between the gate dielectric and the semiconductor. Therefore, the interface and the dielectric properties have a crucial influence on the device characteristics.

Ideal gate dielectric has to have high breakdown voltage and should be thermally stable, easily processable and compatible with the other processing steps. Beyond these basic features, the choice of the dielectric species in OTFTs involves many other effects which can influence the carrier transport and mobility with respect to inorganic materials. First, the dielectric can affect the morphology and/or the molecular organization of the organic semiconductor thin film. The surface roughness of the solution processed organic dielectric is a key concern as a non-uniform dielectric/semiconductor interface will generate a higher density of interface traps that are detrimental for charge transport as shown in Figure 4.8.

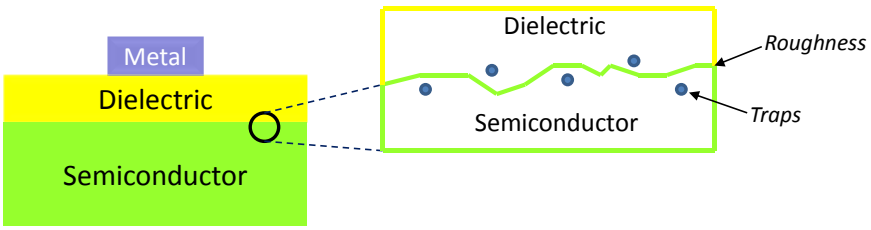


Figure 4.8. Roughness and traps in the interface dielectric-semiconductor.

Surface energy for organic materials is usually weaker than for inorganic ones due to the fact that materials are closed-shell molecules and also because of the van-der-Waals bonding. As a consequence, there are no dangling bonds at the organic surface.

In the same way, a charge carrier excess in an organic molecule leads usually to a molecular deformation and can generate temporal or permanent structural defects.

4.2.4. Desirable OTFT Characteristics

Summarizing, the desirable characteristics of a high-performance OTFT typically include high field-effect mobility, a high On/Off drain current ratio, low leakage current, minimal Threshold voltage shift, sharp subthreshold slope, and low contact resistance. These desirable characteristics are summarized in Table 4.2.

Table 4.2. General requirements for a good OTFT [144]

Requirement	Description
High field-effect mobility (μ_{FE})	Determined by quality, crystallinity, ordering, and microstructure of the semiconductor layer. Requires a low defect density in the semiconductor layer and the interfaces. Mobility influences the switching speed of transistors.
High On/Off drain current ratio (I_{ON}/I_{OFF})	Depends on the quality of the semiconductor and gate dielectric layers. Requires minimum leakage during Off-state and maximum current during conduction (On-state).
Low Threshold voltage (V_T) and minimum Threshold voltage shift (ΔV_T)	Low V_T allows circuits operate at low supply voltages. V_T depends of the interface states of the dielectric film and gate capacitance. Minimal ΔV_T is also critical for stability reasons. ΔV_T depends on interfacial stresses and on the creation of intrinsic defects in the semiconductor layer under a gate bias.
Small subthreshold slope (S)	Small value of subthreshold slope is required for faster switching of the OTFT. Basically, it requires a low density of deep gap states localized at or near the semiconductor-dielectric interface.
Low leakage current (I_{leak})	When a OTFT is off, I_{leak} needs to be small. It is determined by the quality of the gate dielectric.
Low contact resistance (R_C)	Depends on the charge injection efficiency at the semiconductor/contact interface. High R_C limits current driving in the channel and switching speed.

4.3. Fabrication of all-Inkjet Printed Organic Thin Film Transistors

Prior to the discussion of the inkjet processes, it is necessary to review the basics of OTFTs fabrication. Therefore, in this section, most common OTFTs structures will be discussed at first. Selected materials will be analysed to choose the proper layer stack for the all-inkjet devices. The final recipe is summarized in Annex E.

Based on this procedure, an initial recipe will be obtained and used in the following section to manufacture all-inkjet printed transistors.

4.3.1. OTFT Structures

Due to the fact that OTFTs are based on a multilayer stack structure we can find different structures used in the literature varying the relative placement of the gate, source/drain electrodes and the semiconductor layer. Their properties are affected both by the characteristics of the layers and the interface between them.

Depending on the position of the electrodes with respect to the semiconductor and dielectric layer, there are four common device structures: **bottom gate - bottom contact (BG-BC)** (Figure 4.9a), **bottom gate - top contact (BG-TC)** (Figure 4.9b), **top gate - bottom contact (TG-BC)** (Figure 4.9c) and, **top gate - top contact (TG-TC)** (Figure 4.9d) [141].

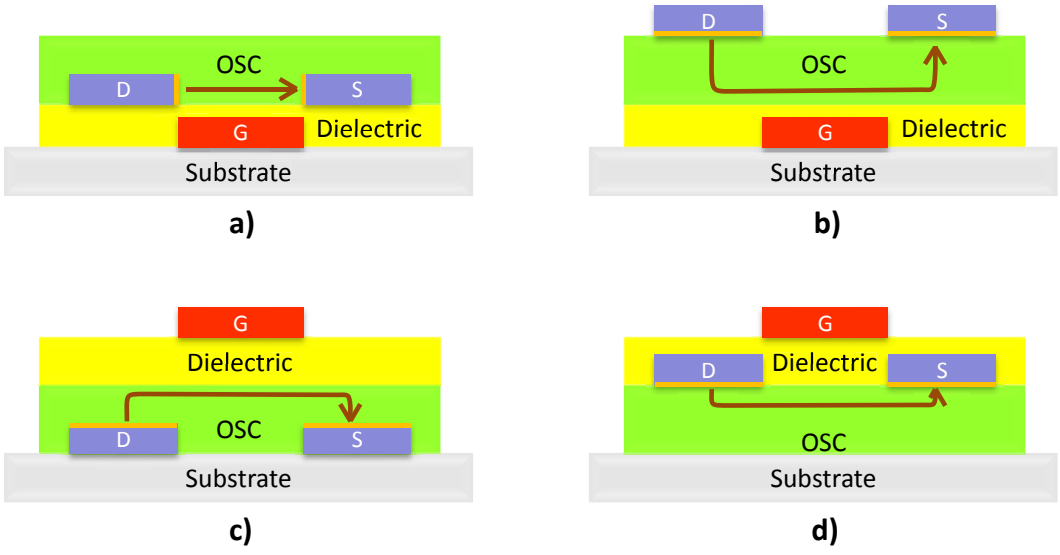


Figure 4.9. Schematic cross-sections of common OTFT structures: a) bottom-gate and bottom-contact; b) bottom-gate and top-contact; (c) top-gate and bottom-contact; and d) top-gate and top-contact.

Every structure has its advantages and disadvantages. For inkjet printed process, the solvent compatibility between layers is critical as the deposited layers can be re-dissolved by subsequent printing if non-orthogonal solvents are used. Moreover, the need of a

homogeneous and flat insulator-semiconductor requires homogeneous underneath layers in terms of morphology.

It is necessary to take into account that when small molecules land on the substrate, they arrange themselves to seat their electron clouds in the region with the highest polarizability. When the molecules are deposited on a metal (especially if its surface is not oxidized), the electron cloud is in its lowest potential energy configuration facing flat into the metal layer. This makes small molecules lie down on the (insulating) substrate at the source and drain contacts, in a different configuration than the one observed in the channel [145] as shown in Figure 4.10.

Figure 4.10. A schematic illustration of the molecular packing in: a) top and b) bottom contact OTFT devices.

This pattern growth leads to a reduction of the device performance in bottom contact configurations due to both a larger series resistance and degraded performance in the section of the channel.

Nevertheless, the most commonly used structure is the **BG-BC** type. This structure is favourable for printing processes, as the semiconductor is printed at last (assuming no encapsulation) avoiding solvent attack by other processing steps and possible doping. This structure is widely used to test the static performance of semiconductor materials using a patterned gate electrode, and an interdigitated S/D contacts resulting in a significant overlap capacitance. One major disadvantage of this structure is the large contact resistance due to the very small effective contact area for charge injection into the channel (orange lines marked in S/D electrodes of Figure 4.9a [146].

Moreover, this configuration has the disadvantage that the organic semiconductor is deposited on two different materials simultaneously: the gate dielectric and the source/drain contacts, so that the morphology of the organic thin film can be disrupted by the non-uniformity of the prior profile and to the wetting/dewetting processes due to different surface tensions as shown in Figure 4.10b.

The second structure is the **BG-TC** structure. The structure is different from the previous one because the S/D electrodes are printed after the semiconductor layer. This structure can reduce the contact resistance between the S/D and the semiconductor, as a larger effective contact area is formed. Furthermore, typical organic semiconductors have a hydrophobic

surface, which can cause the S/D electrodes to dewet, resulting in the loss of line integrity, what is a critical aspect for printing narrow source and drain patterns. Mobility and Threshold voltage of OTFTs can exhibit thickness dependence.

TG-BC and **TG-TC** structures are shown in Figure 4.9c and Figure 4.9d. These structures are the most challenging in terms of process integration, as the semiconductor layer is deposited underneath. In this case, the selection of materials and solvents is crucial. The subsequent deposition of the dielectric material can either damage or unintentionally dope the underlying organic semiconductor compromising the I_{ON}/I_{OFF} ratio. In addition, the subsequent curing steps can potentially degrade the semiconductor material. On the other hand, a fundamental advantage of this structure is represented by the low contact resistance due to the large effective area for injecting charge into the semiconductor channel, which corresponds to the gate/drain and gate source overlap areas. However, this structure offers inherent encapsulation of organic semiconductors, which are typically sensitive to oxygen and moisture.

To conclude, the aforementioned **bottom-gate and bottom-contact (BG-BC)** structure seems to be the most attractive in terms of the "semiconductor-last" processes. Furthermore, it offers a greater flexibility in the choice of materials and fabrication techniques. With this structure, optimizing the transistor performance by modifying or altering semiconductor materials require less experimentation to ensure minimum process-induced disruption at the organic semiconductor layer. The required compatibility between materials will be tested in the following section.

4.3.2. OTFT Device Material Selection and Compatibility

As illustrated in the cross-sectional structure of OTFTs in Figure 4.9a, the functional device layers are the semiconductor, the gate dielectric, and the electrodes. Since these layers are actively involved in the operation of OTFTs, the choice of materials and their compatibility influence device performance. Figure 4.11 shows the key interactions mechanisms between various device layers.

In this section, three basic materials were selected and analysed for the fabrication of all-inkjet transistors. Other materials were also tested or used in additional process steps but their analysis will introduced later.

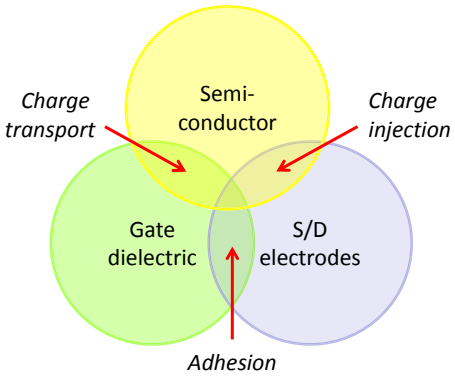


Figure 4.11. Interactions between the three key device layers in an OTFT [133].

4.3.2.1. Organic Semiconductor

The organic semiconductor (OSC) is the core foundation of the OTFT as it governs the charge transport of the transistor.

In this work, an organic polymeric semiconductor from Flexink Inc (FS0027) was chosen since it was commercially available. Work function of FS0027 is 5.5eV.

The implementation of functional and high performance OTFTs is hindered by a number of challenges. First, many commercial semiconductors are very sensitive to air and moisture; thus, the lifetime and stability of the resulting OTFTs is not the appropriate (especially as our processing and characterization is done in ambient conditions). Secondly, the purity of the commercial-grade organic materials is questionable (despite the theoretical 99.9% purity). Impurities are manifested as defects in the organic semiconductor films, which can cause undesirable leakages and traps with a significant reduction of the OTFT performance. Thirdly, the quality of materials tends to vary from batch to batch, affecting device data and analysis uniformity and yield.

As a result, fabricated OTFTs normally display high leakage and Off-currents, low yield and large variability. These issues are a well-known problem among researchers although it is not clearly reported or intentionally hidden in the literature.

A large number of factors can affect the qualities and properties of the organic semiconductor layer, including solvent selection, deposition conditions and surface properties. Different solvents produce films with different degrees of molecular ordering, uniformity and continuity [140] as shown in Figure 4.10. Variations of two orders of magnitude in mobility depending on the choice of solvent have been reported in the literature [133]. The choice of solvent, the concentration of the polymer solution and the deposition parameters must be optimized to yield good quality films.

The organic semiconductor should be confined in the active channel region to isolate each transistor from neighbor devices improving its On/Off current ratio, crosstalk and non-gated current-carrying pathways reducing the Off-current in the device. Inkjet printing allows this selective deposition in which deposition and patterning occurs simultaneously in one single step.

4.3.2.2. Gate Dielectric

The gate dielectric is one of the most critical materials for organic transistor performance as it establishes the field-effect operation in OTFTs.

A general specification for the gate dielectric of OTFTs is summarized as follows: dielectric material has to withstand electric fields of 2 $MV \cdot cm^{-1}$ without breakdown, must have good insulating properties and low charge trapping rate at lower electric field and it should form a high quality interface with the semiconductor layer [147]. In addition, the dielectric film should have low trapping density at the surface, low surface roughness, low impurity concentration and has to be compatible with organic semiconductors.

Examples of organic gate dielectrics for OTFTs include Poly(4-vinylphenol) (PVP), polyvinylalcohol (PVA), polymethyl-methacrylate (PMMA), and polyimide [148][149][150][151]. Organic dielectric materials are less matured than inorganic ones and a research effort is required to enhance material quality, dielectric strength, electrical integrity and other important properties.

Three possible mechanisms have been reported as responsible for the electrical instability of the OTFT [152][153]:

- charge injection from the gate electrode into the organic dielectric layer.
- polarization effect of the polymeric dielectric layer.
- trapped charges at the interface between polymeric dielectric and organic semiconductor layers.

Among them, the effects of the polarization and trapped charges are directly related to the physic-chemical properties and surface morphologies of the polymer dielectrics.

A high-performing transistor should provide a high On-current at low voltages. For an OFET this sets a requirement to the capacitance (C_i) of the dielectric insulator:

$$C_i = \frac{\varepsilon_r \varepsilon_o}{d} \qquad \textit{Eq. 4.3}$$

where C_i is the effective capacitance per unit area, ε_r is the relative permittivity of the insulator, ε_o is the vacuum permittivity and d is the insulator thickness. According to Equation 4.3, there are basically two ways to increase C_i: (1) by decreasing the insulator thickness, or (2) by increasing the relative permittivity [154]. To reach low-voltage operation with OTFTs is challenging while maintaining robustness, stability and flexibility of the structure. Furthermore, nanoscale polymeric films increase the leakage current due to the tunneling effect.

Although successful demonstrations of OTFTs with organic gate dielectrics were demonstrated, most of these devices exhibit a lower I_{ON}/I_{OFF} ratio and high leakage currents than inorganic ones. In order to improve its performance, dielectric composites are being developed. They are compounded by inorganic nanoparticles spatially distributed along the organic polymer. Then, organic dielectric can be mixed with high-k or Si NPs to improve the electrical permittivity.

For the dielectric layer, a crosslinked PVP (c-PVP) polymer material has been used in this work. C-PVP is also a well-known polymeric dielectric. In particular, by cross-linking the PVP the insulating properties are excellent, as reported in literature [150][52][155][156].

4.3.2.3. Electrodes/Contacts

The gate and source/drain electrodes (also known as contacts) for OTFTs can be implemented using metals or organic conductors. The specifications for selecting the gate electrode are very relaxed and include compatibility with device layers and low surface roughness in the case of bottom-gate structures.

In contrast, the choice of materials for source/drain contacts is more stringent because the energetic matching between contact and semiconductor is mandatory to assure an efficient charge injection in OTFTs. Ohmic contact requires that the work function of the metal matches the HOMO level of the organic semiconductor in the case of a p-type OTFTs, and the LUMO one in the case of n-type OTFTs. This implies a high work function metal for p-type OTFTs and a low work function metal for n-type OTFTs.

The interface between the source/drain contact and organic semiconductor requires low contact resistance, which is a function of both parasitic resistance and the energy barrier at the contact/semiconductor interface [1]. Low energy barriers need matching the electrode work function (Φ_M) with the semiconductor ionization potential (IP_s). Figure 4.12 shows the energy scheme at the contact/semiconductor interface. For p-type OTFTs, conductor materials should be selected to minimize the hole injection barrier ($\varphi_B = IP_s - \Phi_M$) thus allowing high charge injection efficiency at the contacts.

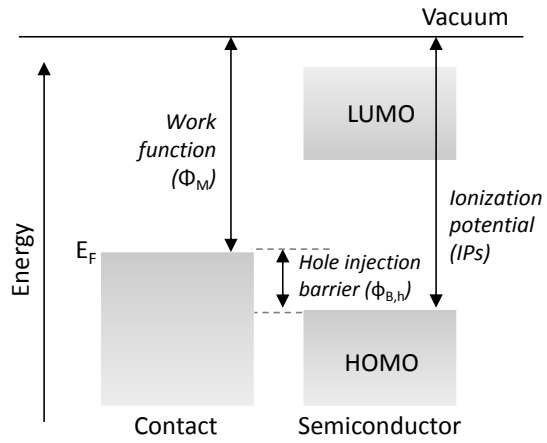


Figure 4.12. Energy band diagram at the contact/semiconductor interface [133].

Since the organic semiconductor used in this work (FS0027 from Flexink Inc) has a work function of 5.5eV, the best metal choice to match with is gold (Au) that has a work function of 5.1eV. Due to the high cost of the AuNP (Au nanoparticles) inks, a silver nanoparticle (Ag) ink was chosen even being aware of some reported problems due to the formation of surface oxide and electrochemical interactions with most organic materials. Silver has a work function of 4.26 eV that can be increased by some additional 0.7 eV when the silver is exposed to oxygen environment [157].

Conductive polymers such as poly(3,4-ethylenedioxythiophene) doped with polystyrene sulfonic acid (also known as PEDOT:PSS) have been used as electrodes in OTFTs. PEDOT:PSS has a workfunction of 5.2 eV matching the requirements of our organic semiconductor material. But, as already reported, the inkjet patterning of PEDOT:PSS is not uniform, therefore complicating its use in a interdigitated transistor structure.

The silver nanoparticle ink EMD5603 from Sunchemical Ink (UK) was selected for gate, drain and source electrodes. This ink has been deeply analysed in previous chapters.

4.3.2.4. Substrate

Substrates reported in the literature include rigid substrates (such as silicon wafers), glass substrates, a variety of flexible substrates such as polymide (commercially known as Kapton® from DuPont), poly(ethylene terephthalate) (PET), poly(ethylene naphthalate) (PEN), aluminium or stainless steel foil, paper, or even corrugated cardboard.

The choice of substrates affects the OTFT performance. Planarity and surface smoothness are particularly critical concerning the OTFT performance because they affect the quality of the overlying thin film device layers. Large substrate surface roughness will cause a greater

density of trap states in the gate dielectric and at the semiconductor/dielectric interface for bottom-gate OTFTs. Klauk et al. [158] reported that pentacene OTFT with a PVP gate dielectric on a PEN substrate have a slightly higher subthreshold swing and Threshold voltage than OTFTs on a glass substrate due to the larger roughness of the PEN substrate compared to glass (15Å for PEN versus 8Å for glass in their study). Moreover, Subramanian et al. [4] demonstrated the increase of the breakdown voltage for capacitors on planarizated PEN substrates when a primer coating layer was deposited onto it in order to flatten its surface.

Since flexibility is an important issue in organic electronics, the OTFTs in this work were printed on a 125 μm flexible PEN substrate (DuPont Teijin Teonex® Q65FA) having a planarized coating side with a roughness of 0.41 nm and a high thermal, chemical and mechanical stability. PEN has a moderate coefficient of thermal expansion (CTE) as shown in Annex D.

4.3.3. OTFT Device Material and Compatibility

Initially, a study of the compatibility between layers was done to choose the suitable layer stack. All the involved layers in the OTFT fabrication were alternatively printed on top of each other's to obtain the best stack for the selected materials.

In Figure 4.13 and Figure 4.14, the small square at right represents the bottom layer and the big square at left the top layer deposited by inkjet printing.

As shown in Figure 4.13a and Figure 4.13b, the compatibility between c-PVP dielectric and silver is good. Both can be printed successfully in top of each other without any significant loss of homogeneity. When the dielectric is printed on top of the silver layer, ink coalescence creates a small area increase (marked with a yellow line in Figure 4.13a) due to the different surface tension of the silver layer. This stack represents the interaction between the gate electrode and the dielectric gate leading to Bottom Gate architecture regarding this stack.

In the case of the OSC layer, the film is not totally homogeneous when printed directly on PEN as it can be observed in Figure 4.13c and Figure 4.13d (marked with a yellow line). Even that OSC was applied after a pre-treatment of the substrate with oxygen plasma (detailed later) to increase the wettability,

Nevertheless, dielectric has a good printability on top of the OSC layer as shown in Figure 4.13c and silver shows some dewetting in the substrate OSC layer transitions that can be observed in Figure 4.13d. Figure 4.13c shows that silver does not present a good printability for the interface dielectric/semiconductor what lead to discard Top Gate architectures, and

therefore the final architecture should be **BG-BC**. Regarding this conclusion, interactions between OSC-Silver and OSC-Dielectric have to be considered.

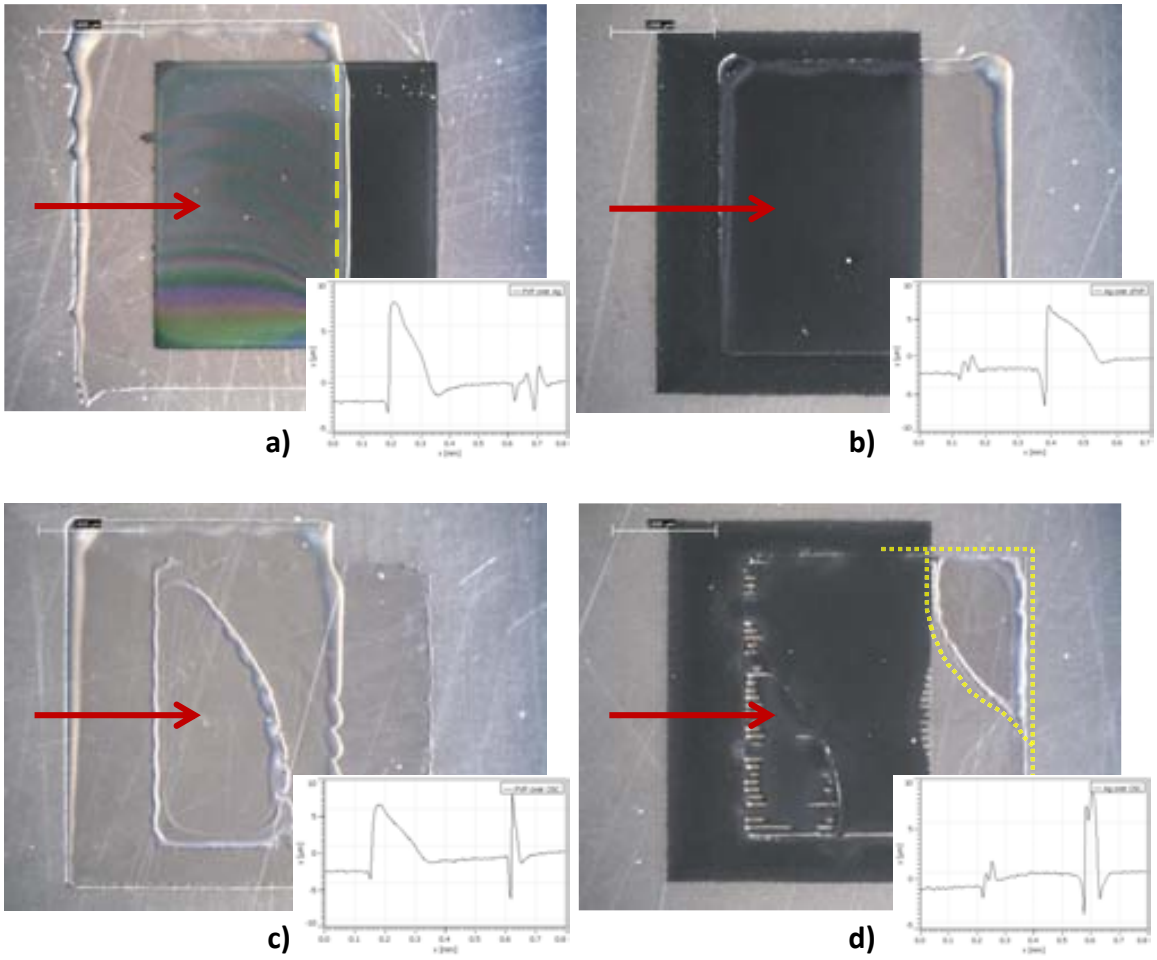


Figure 4.13. a) C-PVP dielectric printed on top of a silver layer; b) silver layer over c-PVP dielectric; c) c-PVP dielectric over OSC layer; and d) silver layer over OSC. (Note: measure = 1mm)

Figure 4.14a and Figure 4.14c shows OSC layer dewetting on top of silver and dielectric layers respectively when no oxygen plasma is applied. Figure 4.14a and Figure 4.14b represents the scenario of the drain and source electrodes interfacing the organic semiconductor. For Figure 4.14c and Figure 4.14d, the stack represents the dielectric/semiconductor interface.

The plasma pre-treatment improves the OSC printability and the layer homogeneity at the top of both silver and dielectric layers as it can be observed in Figure 4.14b and Figure 4.14d respectively. Particularly, OSC film homogeneity on top of the dielectric layer is highly remarkable after plasma pre-treatment. OSC deposited on top of a silver layer shows an important ink accumulation at the center.

These results justify clearly the use of the **bottom gate-bottom contact** structure **using oxygen plasma** in this work.

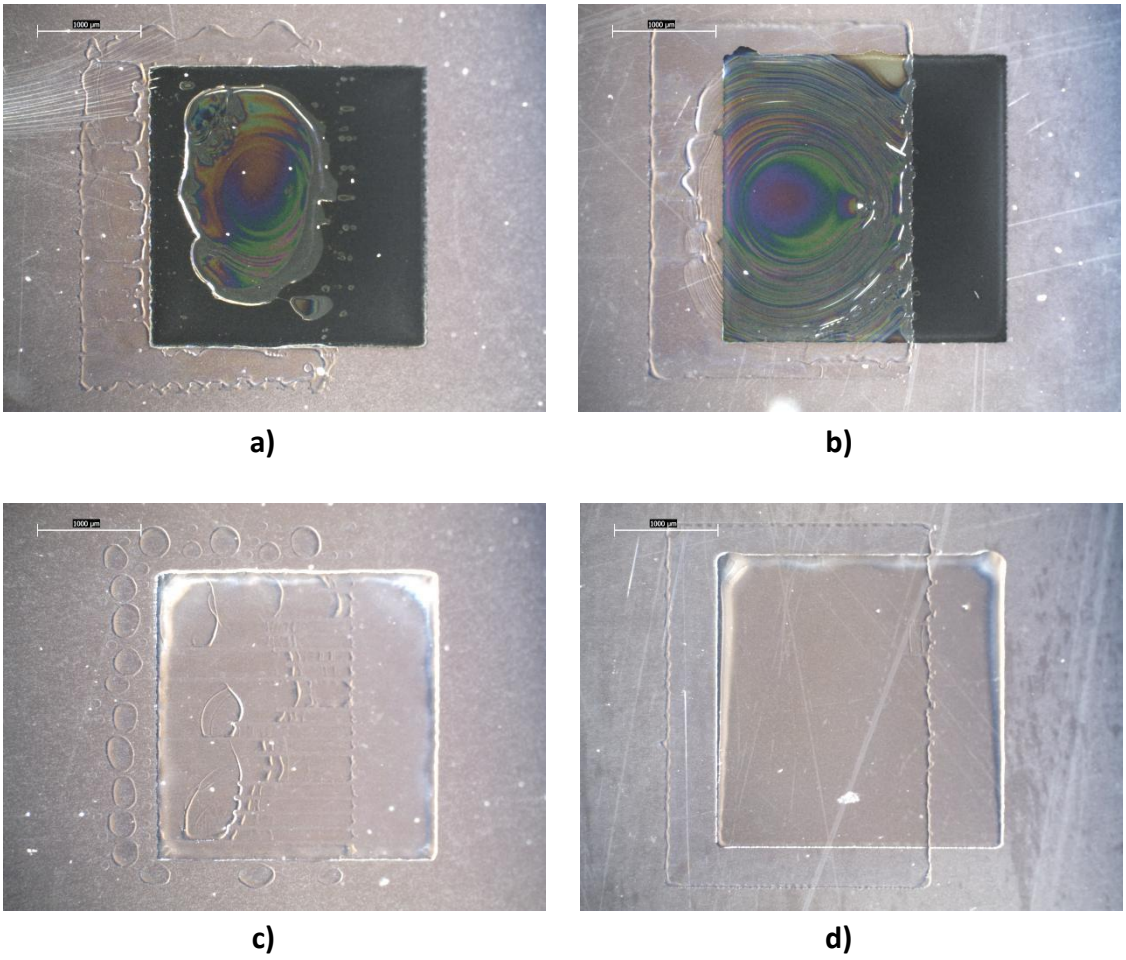


Figure 4.14. a) OSC printed on top of a silver layer without oxygen plasma; b) OSC printed on top of a silver layer using oxygen plasma; c) OSC printed on top of a dielectric layer without oxygen plasma; and d) OSC printed on top of a dielectric layer using oxygen plasma. (Note: measure = 1mm)

4.4. Manufacturing Process Description of all-inkjet Printed OTFTs

In this section, the complete procedure to fabricate all-inkjet printed OTFTs will be deeply explained. Starting from selected materials, the transistor will be built layer by layer and completely characterized in order to fix the recipe. Further device improvements were achieved by means of layout design without changing any material. Those will be detailed in Chapter 6 and will be used in basic circuits in Chapter 7.

The **BG-BC** stack assures the required quality thanks to the compatibility between all the involved materials.

4.4.1. Step-by-step process description

Figure 4.15 shows the applied manufacturing process for **BG-BC** OTFTs based on solvent-based functional materials and the layer stack used. The main technology used to fabricate these devices is inkjet printing.

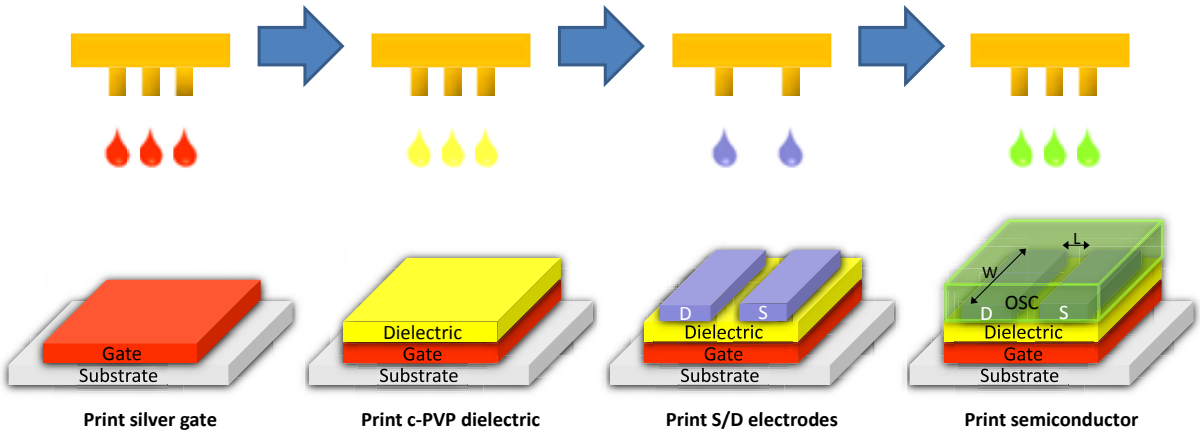


Figure 4.15. Manufacturing process for BG-BC OTFT by inkjet.

First printing step consists in depositing the gate on the substrate and sintered in a convection oven. In the second step, the dielectric is printed on top of the gate electrode and again cured in the convection oven to evaporate the solvents and polymerize the dielectric. Following, the silver source-drain electrodes are printed on top of the dielectric and sintered in the convection oven. Later, oxygen plasma is applied to improve printability and finally, the OSC was deposited and cured on a heating plate. Following sections detail the deposition and characterization of each functional layer.

Figure 4.16 presents a drawing of the 3D view of the layer stack used in this work to fabricate OTFTs.

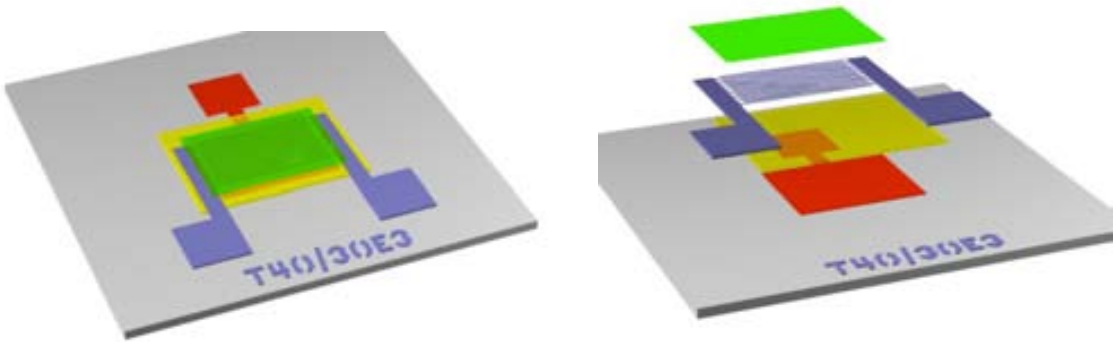


Figure 4.16. 3D view of the OTFT design fabricated.

Every layer of the fully inkjet-printed OTFTs has been morphologically and functionally characterized. Left to right printing direction has always been used. It is worth to mention that to achieve high resolution and low channel width without bulging effect [94], drain and source electrodes have to printed parallel to the printing direction. Figure 4.17 shows images of the manufacturing process for OTFTs with the step-by-step deposition of materials.

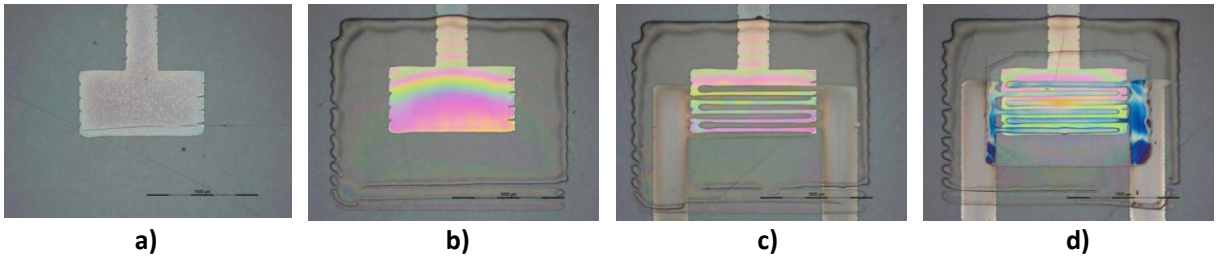


Figure 4.17. Manufacturing process for OTFTs with solvent-based dielectric material (from left to right): a) deposition of the silver gate electrode; b) deposition of the gate dielectric; c) deposition of the drain and source electrodes; and d) deposition of the OSC previously treated by oxygen plasma.

4.4.2. OTFT layout design and related design and compensation rules

One of the first considerations when drawing transistors is the need to set up design and compensation rules. These will be determined by the process engineers according to the selected trade-off between yield and performance and will be required by any circuit designer working at layout level.

Figure 4.18 shows the layout of an OTFT and its layer by layer decomposition. Each layer has its own dimensions related to functional requirements and restricted by the minimum feasible feature dimensions related to the design rules. There are three main parameters when building OTFTs: (1) the precision in the alignment of overlapping layers, (2) the narrowest gap and (3) the minimum line width at which any layer can be reliably printed [105].

The extraction of the complete set of design rules requires specific test structures that are out of the scope of this work. Several layout design and compensation rules were already detailed in previous chapters. Nevertheless, new design rules related to the OTFTs have been obtained out of the experiments in the process development.

Low OSC mobility and the large channel length (>15-20 µm) related to inkjet printing restrictions let to the need of large W/L ratio what allows achieving sufficient drain current through the channel. As already used in inorganic electronics, drawing OTFTs with finger-type (interdigitated) source/drain electrodes allows an optimal balance between large W/L and minimum device area.

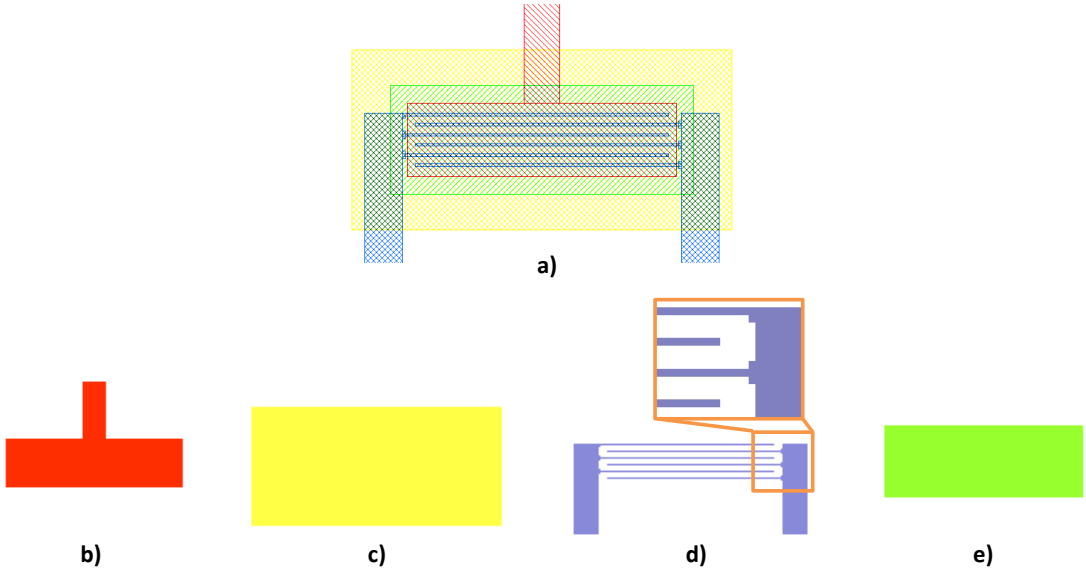


Figure 4.18. a) Layout of an OTFT; b) cross section of the layer stack; c) gate layer pattern; d) dielectric layer pattern; e) D/S layer pattern and f) OSC layer pattern.

The basic guidelines concerning design rules are:

- The metal gate layer should extend beyond the source/drain electrodes. This avoids having uncontrolled reduction of the channel due to interlayer misalignment.
- The metal gate layer area should be large enough to maximize its thickness homogeneity against the coffee ring effect.
- Metal S/D spacing is responsible for the channel length that will be minimal for many transistors to obtain the largest possible current per unit area[23].
- Metal width has to assure the formation of straight and uniform metallic lines, especially for the S/D fingers.

[23] That will be a critical parameter to qualify the process as is in inorganic technologies.

- The dielectric layer should extend far beyond the source/drain electrodes to maximize the thickness homogeneity against the coffee ring effect.
- The border of the OSC should be far enough from the S/D drain electrodes to avoid uncontrolled reduction of the channel width due to interlayer misalignment.
- Minimizing OSC area (up to the surface of the gate electrode) minimizes source/drain overlap capacitance.
- The OSC layer area should be large enough to minimize its homogeneity against the coffee ring effect in order to reduce the parallel S/D resistance.
- Additional, all transistors (independently of their dimensions) should have the bond pads in the same location to simplify its testing by using probe stations.

The basic geometric relations for the design rules are drawn in Figure 4.19.

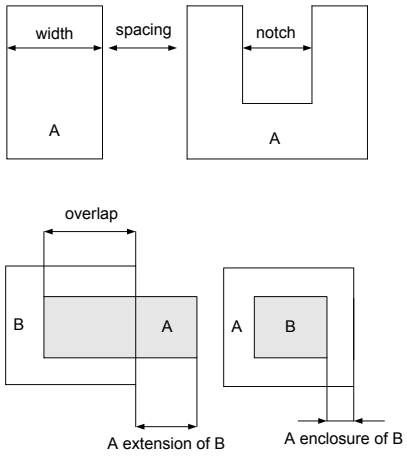


Figure 4.19. Geometric relations.

Figure 4.20 shows the minimum set of design rules used on this thesis work. Value, definition and notation for every rule are described in Table 4.3.

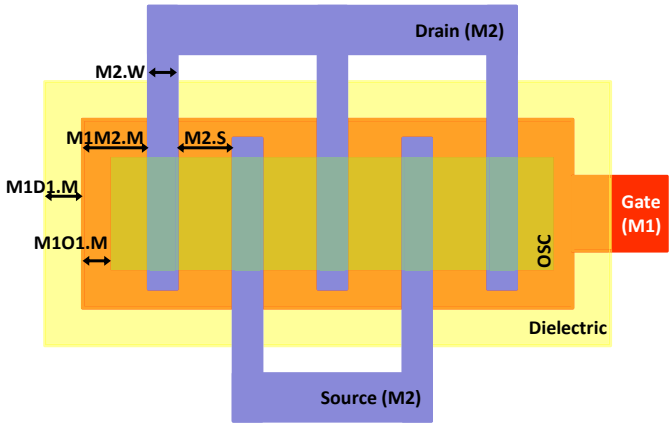


Figure 4.20. The suggested design rules for an interdigitated OTFT.

Design rules are applied on drawing layers that need to be defined previously. For our technological process MET1 refers to the metallic layer used as gate electrode, DIEL1 refer to the gate dielectric, MET2 is the metallic layer used for drain and source electrodes and finally ORG1 represents the OSC layer.

Table 4.3. Suggested OTFT layout design rules

Rule	Description	Value [µm]
M2.W	Minimum width of MET2 source and drain fingers.	40 µm
M2.S	Minimum spacing of MET2 source and drain fingers (channel length).	60 µm
M1M2.M	Minimum margin of MET1 (gate layer) to MET2 (source and drain fingers).	80 µm
M1D1.M	Minimum margin from DIEL1 to MET1.	400 µm
M1O1.M	Minimum margin from MET1 to ORG1.	140 µm

4.4.3. Gate electrode

The fabrication of both metallic layers (MET 1 and MET 2) uses SunTronic EMD5603 (SunChemical). This ink does not require any additional treatment on the surface or the previous layer (substrate for MET1 and dielectric for MET2) to eliminate the coffee ring in order to obtain smooth and continuous lines [94].

At first, the substrate was cleaned using an impregnated wipe with ethanol and dried with a nitrogen flux in order to remove remaining particles from the substrate.

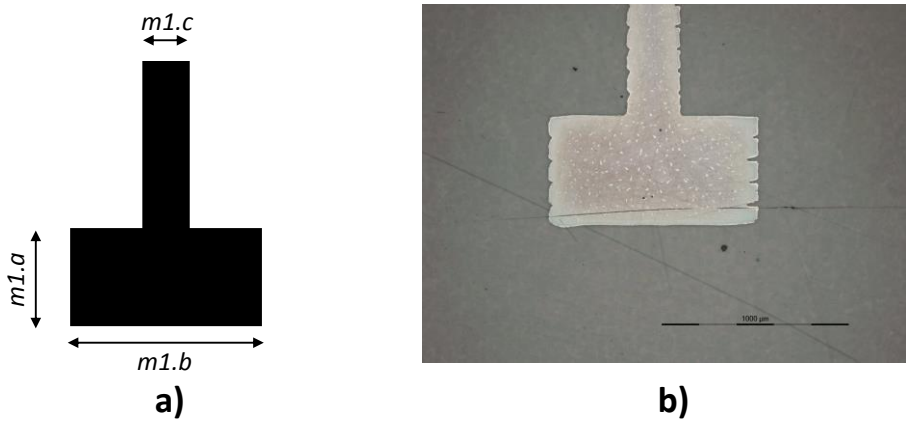


Figure 4.21. a) Layout pattern of gate electrode and contact pad; and b) Printed pattern of gate.

As already mentioned and shown in Figure 4.21, the gate electrode is designed to completely overlap the interdigitated source/drain (S/D) electrodes. This configuration increases overlap capacitance, reducing the speed of the device. However, it also reduces the risk of un-gated channel regions resulting from printing misalignment.

The gate electrode is deposited on the foil using the pattern shown in Figure 4.21a. The gate pattern is printed with a drop spacing of 20 µm, a plate temperature of 40ºC.

The silver gate electrodes printed on PEN foils were electrically characterized using the Van der Pauw four-probe measurement system. The average value obtained for the sheet resistance is 1.52 ± 0.03 Ω/square and for the conductivity 2.54E+06 ± 0.05E+06 S/m. We can improve the conductivity by changing the curing procedure (higher temperatures and longer exposure time on the convection oven) but this is not required for the electrical function of the gate electrode.

An optical microscope was used to determine the printed dimension of the gate layer according the parameters defined in Figure 4.21a. Table 4.4 summarizes the dimensions of the drawn layout and the ones obtained out of the printed samples.

Table 4.4: Comparison of dimensions of layout pattern and printed pattern of the gate layer.

Layout pattern [µm]	Printed Pattern [µm]	Difference
m1.a= 600	619.13 ± 24.93	6.32%
m1.b= 1140	1107.17 ± 18.17	-3%
m1.c= 300	279.47 ± 17.27	-0.2%

The vertical dimension *m1.a* is slightly increased while the horizontal one is even less slightly reduced. This is due to the fact that ink coalescence is more pronounced in horizontal lines (printing direction) than in vertical ones. Consecutive drops tend to move left where the accumulation of ink is bigger, reducing the final pattern size in the horizontal direction.

Gate layer thickness and roughness was determined by optical profilometry. An average height of 280 ± 35 nm was determined by scanning the complete electrode area. To avoid wrong measurement data due to the flexible, bending PEN substrate only 150 µm cross section length was measured as shown in Figure 4.22a.

In the Figure 4.21b, some marks in the gate surface can be observed. These marks where analysed by optical interferometry. The 3D surface scan and the profile are shown in Figure 4.22b and Figure 4.22c revealing small holes as deep as the gate layer thickness. These holes can be either pinholes in the silver layer or measurement artifacts and its origin remains elusive.

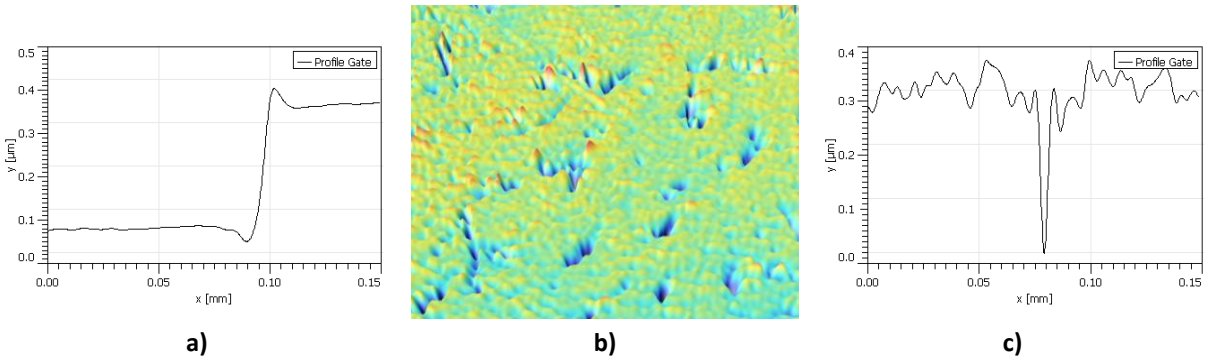


Figure 4.22. a) Profile of the gate cross section; b) 3D surface scan of the gate layer; c) Profile of the gate surface.

Small coffee-ring effect is visible as usual for this ink composition. However, the coffee-ring effect as well as the layer roughness are in a reasonable range for inkjet-printed TFTs and will barely affect the performance. The maximum average peaks detected for the scanned patterns are about 45 ± 5 nm.

Despite of these results, some higher peaks were measured in the bottom left corner of the gate electrode. This irregular concentration of ink was verified in several samples and can potentially cause short-cuts between the gate and the S/D layers as the height measured is larger than the dielectric thickness (1.42 ± 0.32 µm). Figure 4.23 shows this effect measured by confocal microscopy. To avoid that, gate pattern corners should be deposited away from the S/D vertical contacts and fingers. This reinforces the similar argument required by the design rule concerning printing misalignments among these layers (M1M2.M design rule).

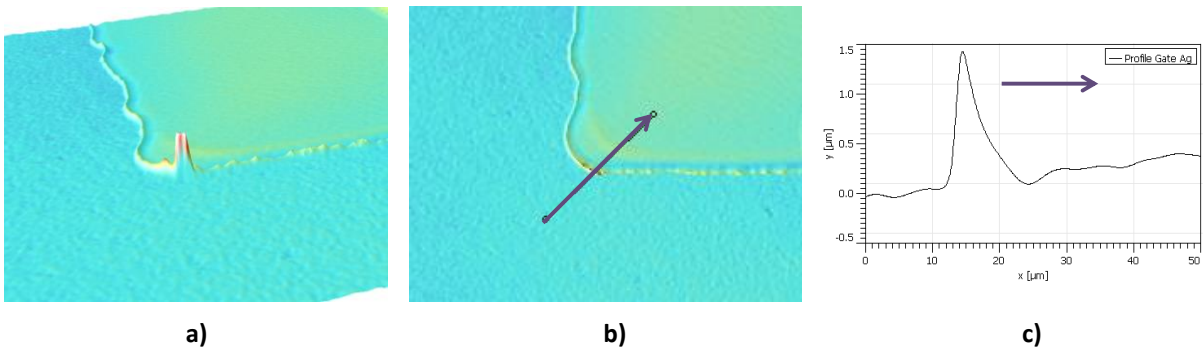


Figure 4.23. a) Gate peak at bottom left corner; b); and c) profile of the peak cross section.

Figure 4.24a and Figure 4.24b shows the optical profilometry of an inkjet-printed gate layer in a large scan area (250 µm x 250 µm) produced using the silver ink filtered with a 0.45 µm PTFE filter as usual. In the figures, one can observe a maximum peak height of 750nm with a surface roughness of 14.5 nm. Figure 4.24c and Figure 4.24d shows similar measurement

performed in an inkjet printed layer previously filtered with a 0.2 µm PTFE filter where the maximum peak height is 350 nm and the substrates roughness is 11.2 nm[24].

The fine filtration reduces the diameter of the silver nanoparticles aggregated that are ejected by the inkjet printhead, resulting in a reduction of the maximum peaks observed in the surface of the silver layer. The reduction of these peaks in the gate layer implies a reduction of the risk of short circuit between both metallic layers, thus improving device yield. This additional filtering step is an alternative way to solve some of the problems observed in Figure 4.23 thus relaxing the M1M2.M (Table 4.3) design rule.

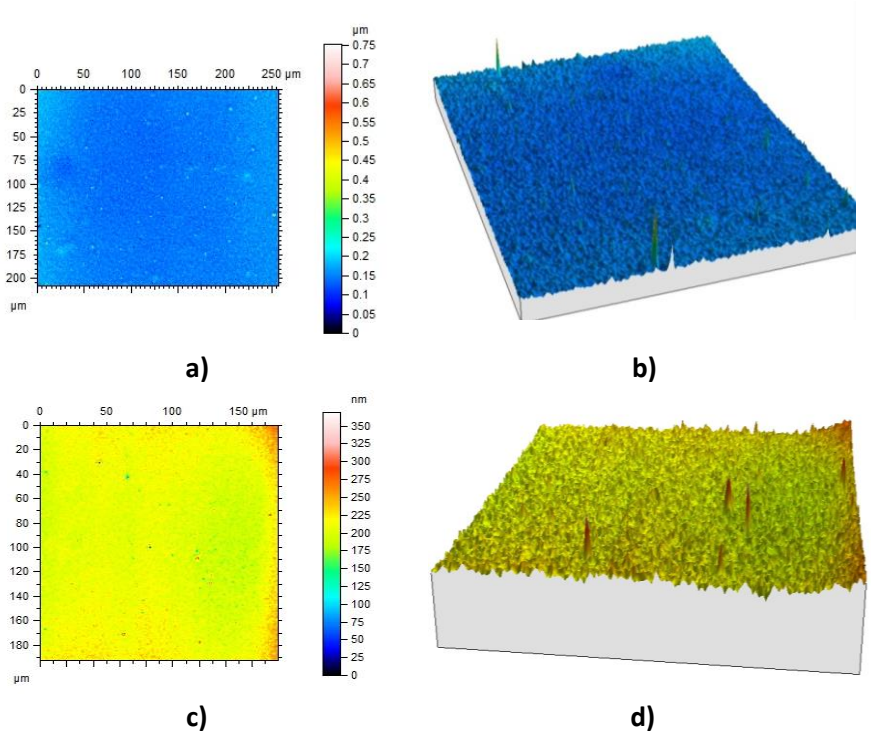


Figure 4.24. Silver ink analysis by optical profilometry: a) and b) 2D and 3D of a silver ink with 0.45 µm PTFE filter; c) and d) 2D and 3D of a silver ink with 0.2 µm PTFE filter[24].

4.4.4. Solvent-based dielectrics

A solvent-based dielectric was selected to obtain thinner layers because the major part of the ink is a volatile solvent which will not be part of the deposited film. This is a key factor to obtain a device with the thinnest dielectric to obtain the best possible OTFT performance. However, solvent based dielectrics have several disadvantages in terms of printing reliability: coffee ring stain, layers with pinholes, material compatibility (compatibility with layers printed before and compatibility with solvent and printhead), environmental issues (harmful solvents) and large curing processes to remove the solvent from the deposited layer.

[24] Measurements performed by ENEA (Naples, Italy) in the framework of the TDK4PE project.

Most of those disadvantages are related to the evaporation process (Marangoni flow). The evaporation process should be very homogeneous, otherwise inhomogeneous evaporation will result in inhomogeneous layer morphology and thus to the risk of reduced printing reliability.

The choice of c-PVP as dielectric material in OTFT structures arises from its good insulating performance and relatively low-temperature condition for thermal curing that makes it compatible with the rest of materials and curing processes required.

The c-PVP ink was formulated using the similar recipe used in the capacitors fabricated in Chapter 3. The ink was prepared by using commercial precursor materials from Sigma Aldrich (USA), starting from a solution of PVP dissolved in PGMEA (propylene glycol monomethyl ether acetate). Then, the crosslinker (poly(melamine-co-formaldehyde) methylated) was added. The final concentration (8.3 wt% for PVP and 1.7 wt% for crosslinker) was suitably optimized in the framework of TDK4PE project in order to assure a stable ejection of the drops by cartridges of Dimatix Materials Printer DMP2831. The post-printing treatment was a thermal curing performed in convection oven at 200 °C for 20 min. The ink was filtered prior printing with a mesh size of 0.2 μm (PTFE filter). After filtering, the ink was introduced in the printhead.

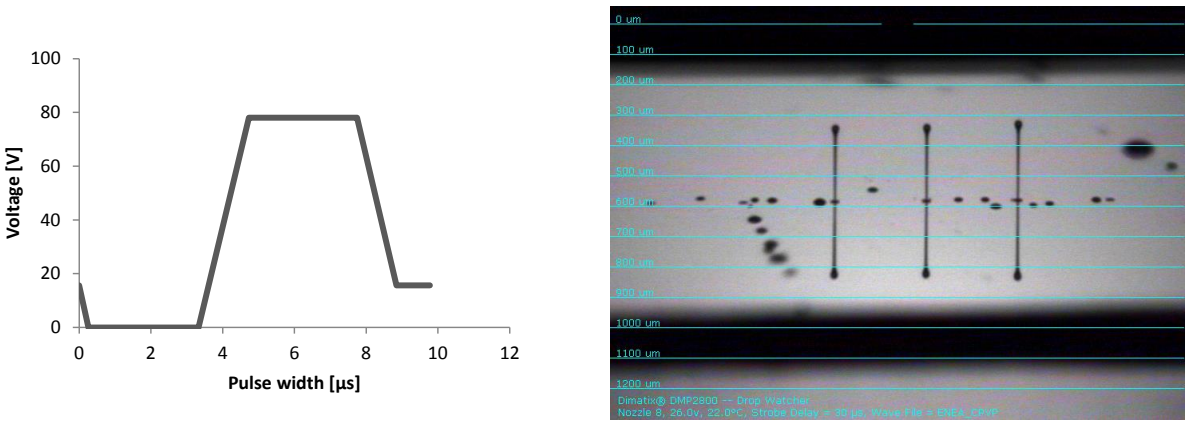


Figure 4.25. a) Waveform for c-PVP ink using 10pL printheads on DMP2831; b) drop watcher picture of ejected c-PVP drops.

A waveform for the c-PVP ink was developed for the 10 pL Dimatix printhead, starting from the waveform of the Dimatix Model Fluid 2 profile. Only small changes were required for stable drop ejection of c-PVP indicating similar physical ink properties. Figure 4.25a shows the developed waveform that was fixed for all the c-PVP layers printed. Only slight changes of voltage were done to optimize the drop ejection in each printing session.

According to this procedure, first printing tests were done onto the Teonex PEN foil depositing single droplets. A drop diameter of about 65 µm was determined with the given printing parameters. A dielectric film with low roughness was obtained by adjusting the inkjet printing parameters (voltage, frequency and shape waveform). A drop space of 20 µm was found in Chapter 3 to provide very smooth lines with sharp edges and reliable film formation without short circuits.

Printing the dielectric layer was supported without any solvent pre-treatment to avoid damaging or scratching the gate electrode. The dielectric layer was printed on top of the gate layer trying to fully cover the entire area of the gate as much homogeneous as possible. But, as shown in Figure 4.26b, the layer exhibits a very prominent coffee-ring effect. Due to this, the layout pattern of c-PVP was designed to achieve that only the inner part (not affected the coffee-ring) would be considered for building the transistor. As already mentioned, the design rule M1D1.M (Table 4.3) for transistors takes into account that the ring is outside of the transistor device.

Figure 4.26 shows the layout pattern for the dielectric layer which are perfectly aligned with the gate patterns already printed.

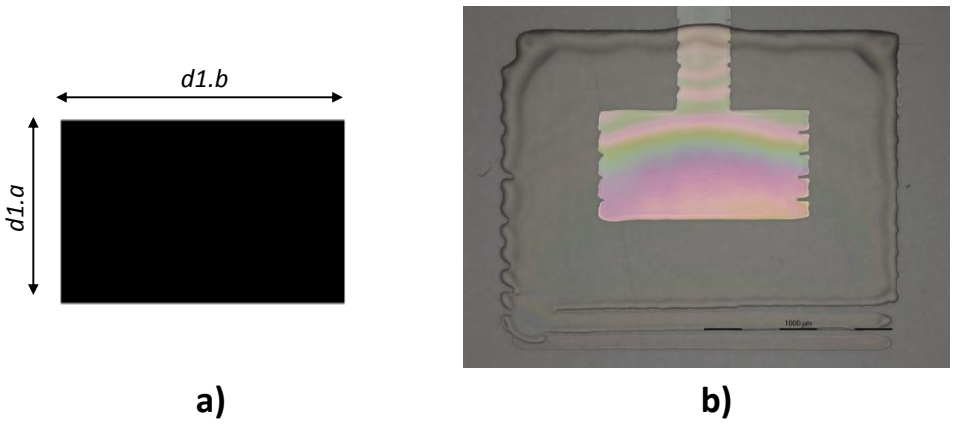


Figure 4.26. a) Layout pattern for the dielectric layer; and b) printed pattern of the dielectric layer with the coffee ring stain clearly visible.

Table 4.5 summarizes the dimensions of the layout pattern and the measured from the printed samples and shows also the deviation obtained due to wetting and dewetting processes.

Table 4.5: Comparison of dimensions of layout pattern and printed pattern of the dielectric layer.

Layout pattern [µm]	Printed Pattern [µm]	Deviation
d1.a= 1440	1510.10 ± 26.60	5.97%
d1.b= 2000	2046.32 ± 43.38	2.26%

In general, c-PVP printing is very stable because the ink does not contain particles and also because drying the solvent is very slow. However, from time to time nozzles were clogged during printing despite good drop ejection (verified using the drop watcher system), causing missing printed lines and resulting in shortcuts between gate and source/drain layers.

Figure 4.27 shows an inkjet printed dielectric layer with missing lines due to a selective obstruction of printhead nozzles, resulting in a non-uniform deposited layer.

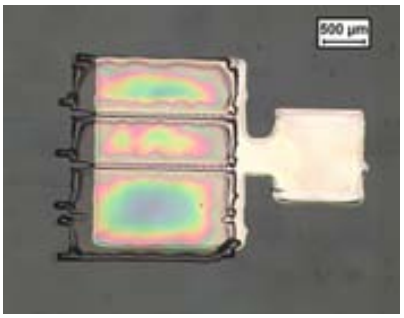


Figure 4.27. Inkjet-printed PVP dielectric on silver with a drop space of 20 µm[25].

4.4.4.1. C-PVP morphological characterization

Figure 4.28 shows the characteristic profile of a c-PVP layer. A big bulge at the edge of the dielectric pattern is visible indicating a strong coffee-ring effect due to the mix of solvents.

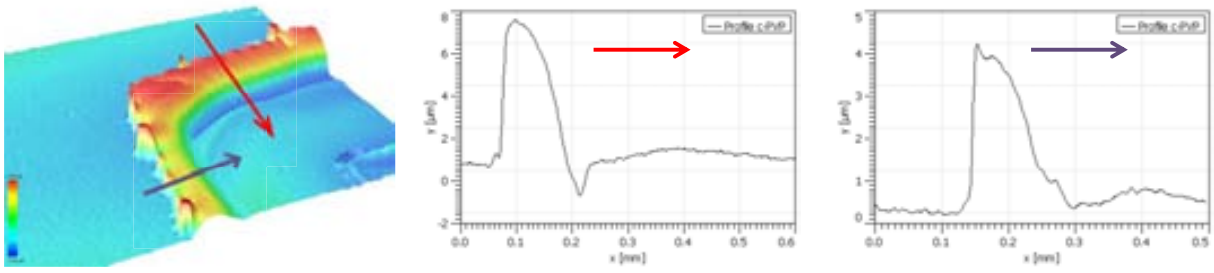


Figure 4.28. a) Confocal image of the c-PVP edge; b) and c) characteristic cross-section profile of c-PVP by optical profilometer.

[25] Source: TUC.

The measurement of the dielectric c-PVP was performed by optical profilometry and shows a layer thickness of 740 nm using a measurement length of about 500 µm. When the measurement length increases, the layer thickness decreases to 370 nm. In particular, the internal region of the c-PVP area is almost flat with average thickness of 400 nm.

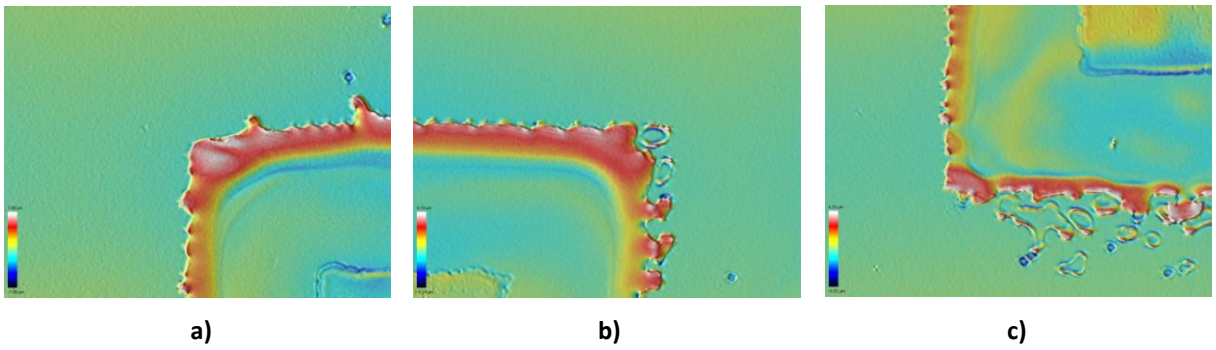


Figure 4.29. Coffee ring stain at different sides of a square patterned c-PVP layer: a) and b) top corners; c) bottom corner.

The coffee ring stain is not homogeneous in all the c-PVP layer sides. As it can be observed in Figure 4.28, the upper wall has an average thickness of 8.1 µm and an average width of 580 µm. But vertical walls have an average thickness of 4.9 µm with an average width of 450 µm. As already demonstrated in Chapter 2, the ink coalescence causes a displacement of the ink to the top left part of the printed pattern. Purple arrow in Figure 4.28a shows the printing direction. Figure 4.29 shows the coffee ring stain caused at different sides of a square patterned c-PVP layer.

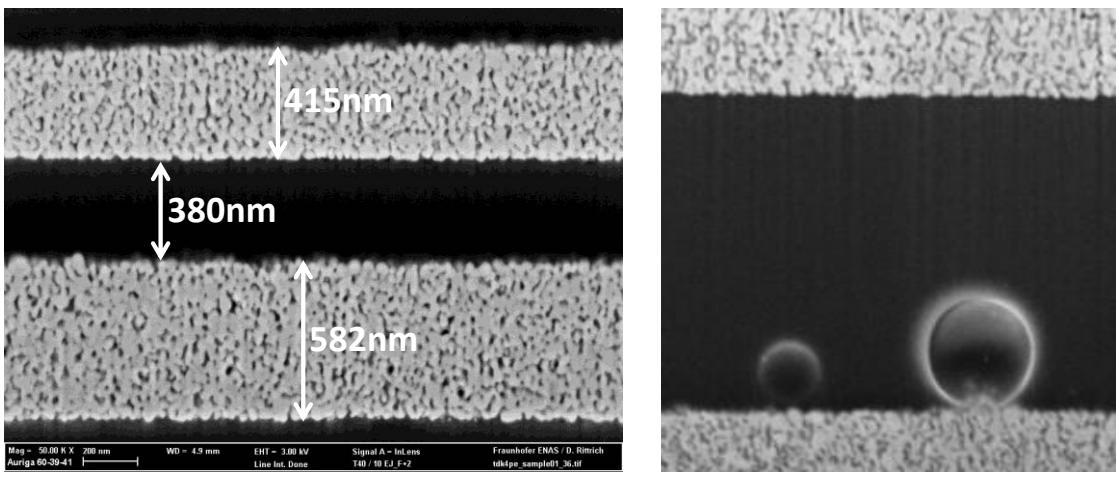


Figure 4.30. Left: cross-sectional FIB image of a fully inket-printed OTFT with the dielectric c-PVP; Right: entrapped air in the dielectric layer[26].

[26] Measurements done at TUC.

Focus-Ion-Beam (FIB) images show similar results than those obtained by confocal profilometry. As indicated in Figure 4.30, the layer thickness of the c-PVP is 380 nm between gate and source/drain fingers. Also, in Figure 4.30b, some bubbles in the c-PVP layer can be observed which might come from entrapped air due to poor degassing.

The AFM analysis of c-PVP layer was performed in an internal area of the printed surface, far from the edges and, hence, in correspondence of the flat region (the active area of the device). AFM images of c-PVP layer are reported in Figure 4.31.

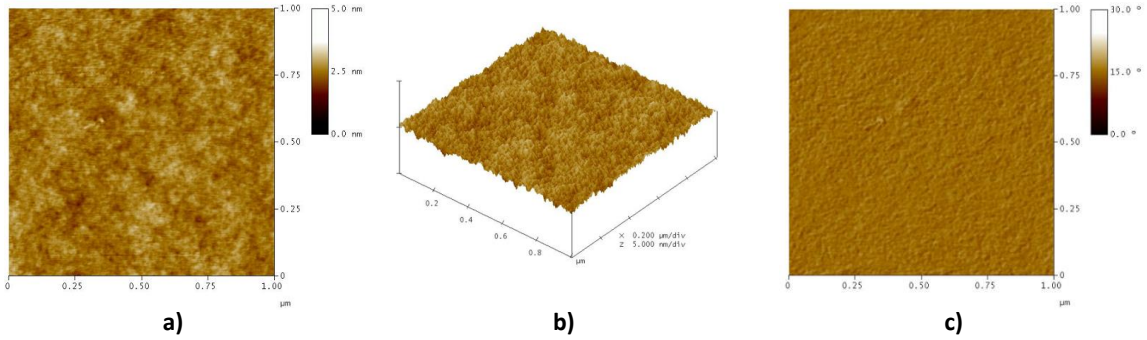


Figure 4.31. AFM images of c-PVP layer printed on top of Ag bottom gate: a) 2D-height; b) 3D-height; and c) 2D-phase[27].

The investigated dielectric layer can be considered as very smooth with a root-mean-square roughness of about 0.20 nm.

4.4.5. Source & drain electrodes

Printing source and drain (S/D) for BG-BC transistor was done with a layout pattern having the dimensions described in the Figure 4.32. These dimensions were extracted from the experiments performed in Chapter 2 and named as design rules M2.S and M2.W (Table 4.3).

[27] Source: ENEA.

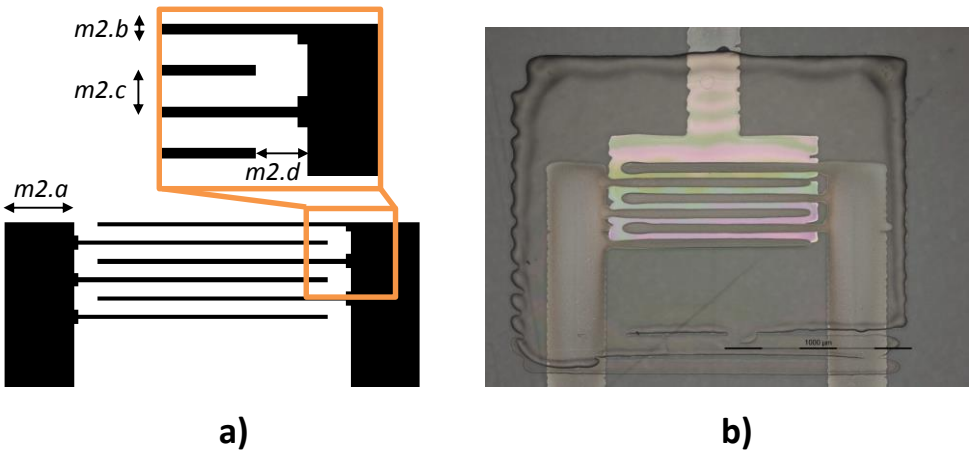


Figure 4.32. a) Layout pattern for the S/D layer; and b) Printed pattern of the S/D layer on top of the dielectric and gate layers.

Before printing the source/drain electrodes any chemical pre-treatment was applied to the dielectric layer. Along with this, printer's plate was heated at 60° C to control the spread of the deposited droplets and to get partially sintered when the droplets fall onto the dielectric. The entire print for this third layer was done with a drop spacing of 20 µm.

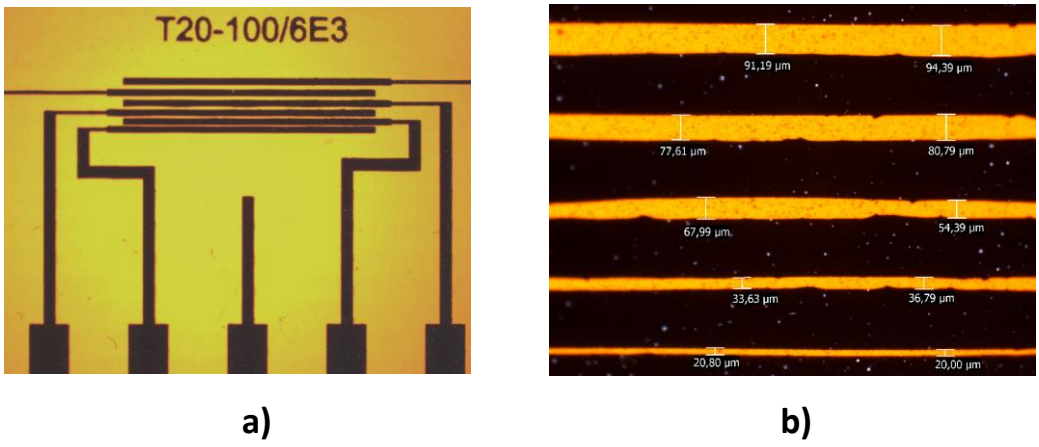


Figure 4.33. a) Test vehicle for a minimum channel length extraction; and b) Minimum distances in interdigitated fingers.

Different experiments were performed to extract the minimum S/D finger separation, as shown in Figure 4.33. Following, the dimensions of the printed source and drain electrodes were investigated using optical microscopy. Table 4.6 gives a summary of all values obtained.

Table 4.6: Comparison of dimensions of layout pattern and printed pattern of the S/D electrodes.

Layout pattern [µm]	Printed Pattern [µm]	Deviation from layout
m2.a = 300	304.83 ± 4.70	1.58%
m2.b = 40	52.70 ± 4.32	24.10%
m2.c = 40	26.78 ± 3.46	- 49.34%
m2.d = 100	90.06 ± 4.10	- 11.04%

As *m2.b* value denotes, the spread of the ink deposited on top of the dielectric surface is higher than on top of PEN substrate. The different surface tensions of PEN substrate and dielectric film cause these different line widths (already introduced in Chapter 2). The decrease of the separation between drain and source electrodes (namely *m2.c*) is mainly due to the higher spreading of the silver layer onto the dielectric surface. Moreover, the horizontal distance between the drain and source electrodes (namely *m2.d*) is also decreased to the bulge effect at the end of the printed line.

The average channel length of 26.78 µm may be too large to obtain sufficient drain current at a lower voltages to reach faster switching speeds. However the device yield of inkjet printing process is compromised by a decreasing channel length due to the fluctuation in the flight direction of the inkjetted droplets [129]. In addition, inhomogeneous wettability of a substrate surface leads to irregularities in printed patterns and short circuit formation between source and drain electrodes.

4.4.5.1. Source/drain layer morphological characterization

In this section the layer morphology of the inkjet-printed silver finger electrodes will be analyzed.

Figure 4.34 shows a characteristic profile of source and drain electrodes printed on crosslinked PVP and characterized by optical profilometry. The electrodes show a clearly visible coffee-ring effect with peaks ranging from 20 to 200 nm. They have an average height of about 450 – 500 nm and a finger width of about 40 µm. The channel width was measured to be about 30 µm.

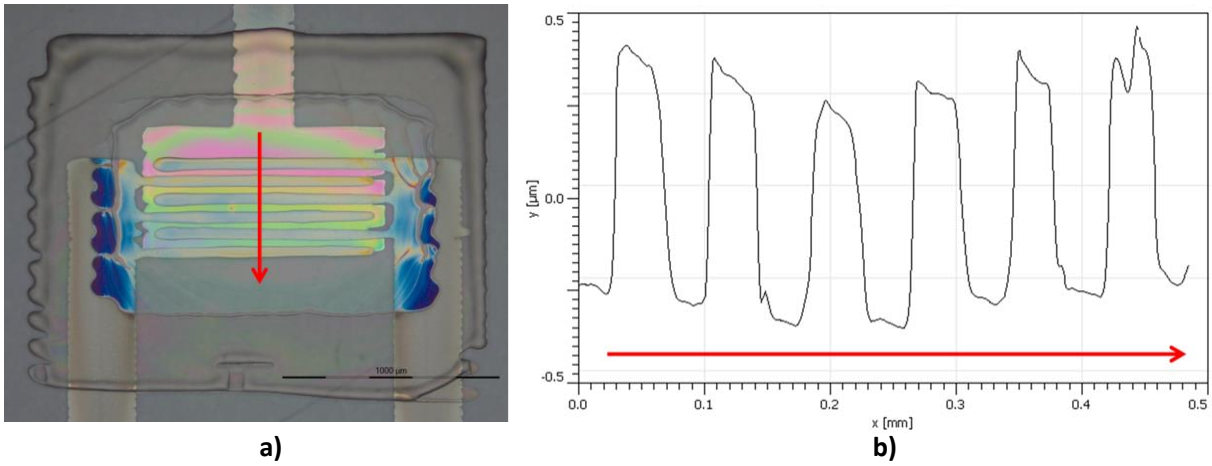


Figure 4.34. a) All-inkjet printed transistor; b) Profile of drain & source interdigitated electrodes. Red arrow shows the direction of measurement.

The FIB images were made by ion beam cutting across the source-drain patterns to shown a cross-section of a single silver electrode, either source or drain. Several features appear in the dielectric such as air bubbles that can be also observed in Figure 4.35.

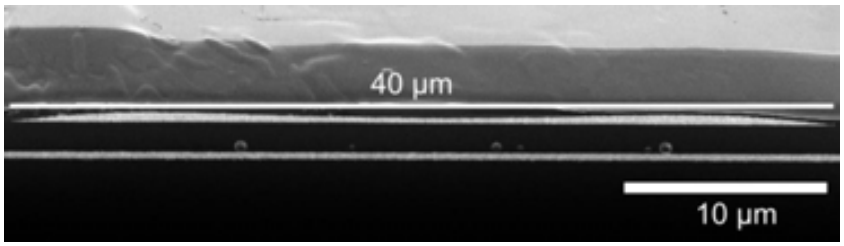


Figure 4.35. SEM cross-sectional image of a fully inkjet-printed OTFT with c-PVP dielectric, the focus is set on the source/drain electrode and its morphology[28].

In order to investigate the surface morphology of the source/drain layer, AFM analysis was performed. The measurements were carried out in tapping mode configuration with a scan size of 1 x 1 μm^2 for all the investigated samples.

The silver layer printed on top of c-PVP is different than the silver bottom layer as the ink is filtered only with a 0.45 µm PTFE filter. Figure 4.36 shows in 2D- and 3D-height images of the silver surface. In this case the root-mean-square roughness was estimated equal to 4.7 nm.

The difference between the root-mean-square roughness values obtained for silver in gate and source/drain layers is attributed to the different understack layers. Indeed, in the former case silver is printed directly on PEN foil having a theoretical surface roughness (0.41 nm)

[28] Measurements done at TUC.

slightly higher than the roughness of c-PVP layer (0.2 nm), which is the understack in the case of source/drain electrodes.

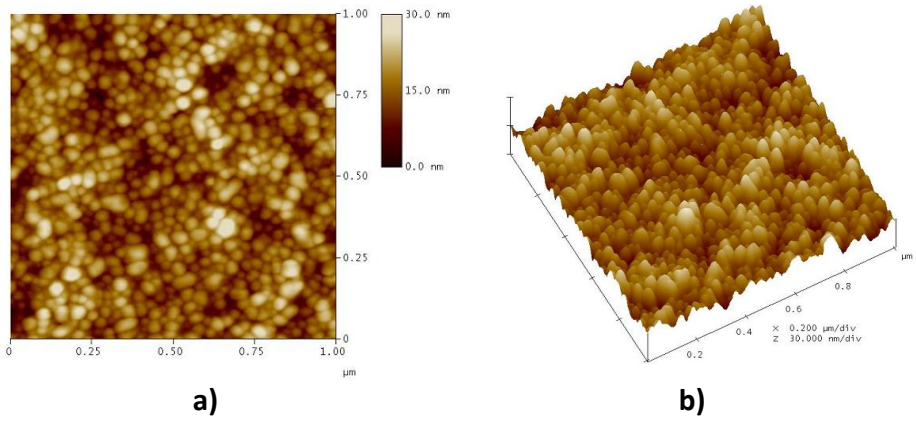


Figure 4.36. AFM images of silver layer printed on top of c-PVP: a) 2D-height; and b) 3D-height[29].

4.4.5.2. Compensation strategies for source/drain improvement

Following on from the results outlined in Section 2.2.5, the electrodes and channel widths have been optimized as shown in Figure 4.34b. The image shows that the electrode profile is regular, without a pronounced coffee ring effect and with sufficient separation in order to obtain a high yield.

Ink coalescence and wet/dewetting processes create different effects resulting in short and open circuits in source & drain electrodes. In order to avoid these undesired effects, we applied the compensation techniques consisting in extracting or adding additional drops to electrodes and junctions, thereby improving the morphology of drain & source electrodes and increasing the yield of the fabricated devices.

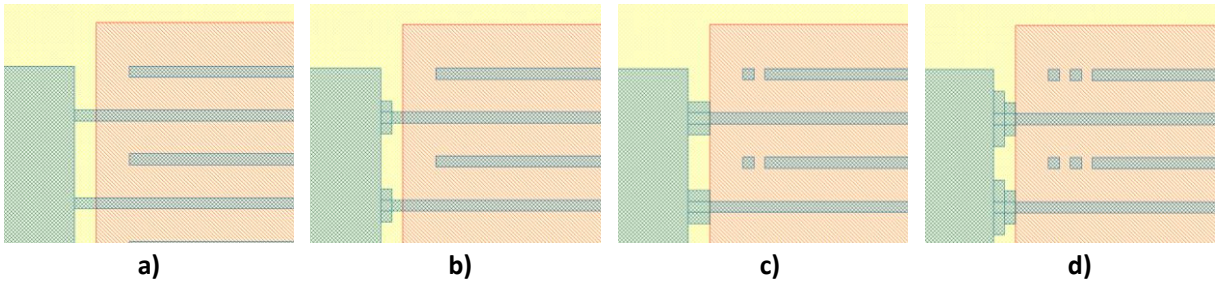


Figure 4.37. Different compensation strategies for S/D improvement.

Figure 4.37 shows the applied methodology for the deposition of the drain and source electrodes on an all-inkjet printed OTFT. Different approaches were taken in account in

[29] Source: ENEA.

order to evaluate the resulting printed patterns to choose the most suitable. This approach was proposed to avoid the match effect at the end of the drain/source electrodes producing short-circuits among them.

Figure 4.38 shows the different printed patterns obtained with and without the application of compensation strategies. Figure 4.38b and c shows different effects that occurred to non-compensated electrodes and junctions such as a bulging effect at the end of the electrodes creating short circuits between drain and source electrodes (Figure 4.38c) and strangled junctions producing open circuits (Figure 4.38b).

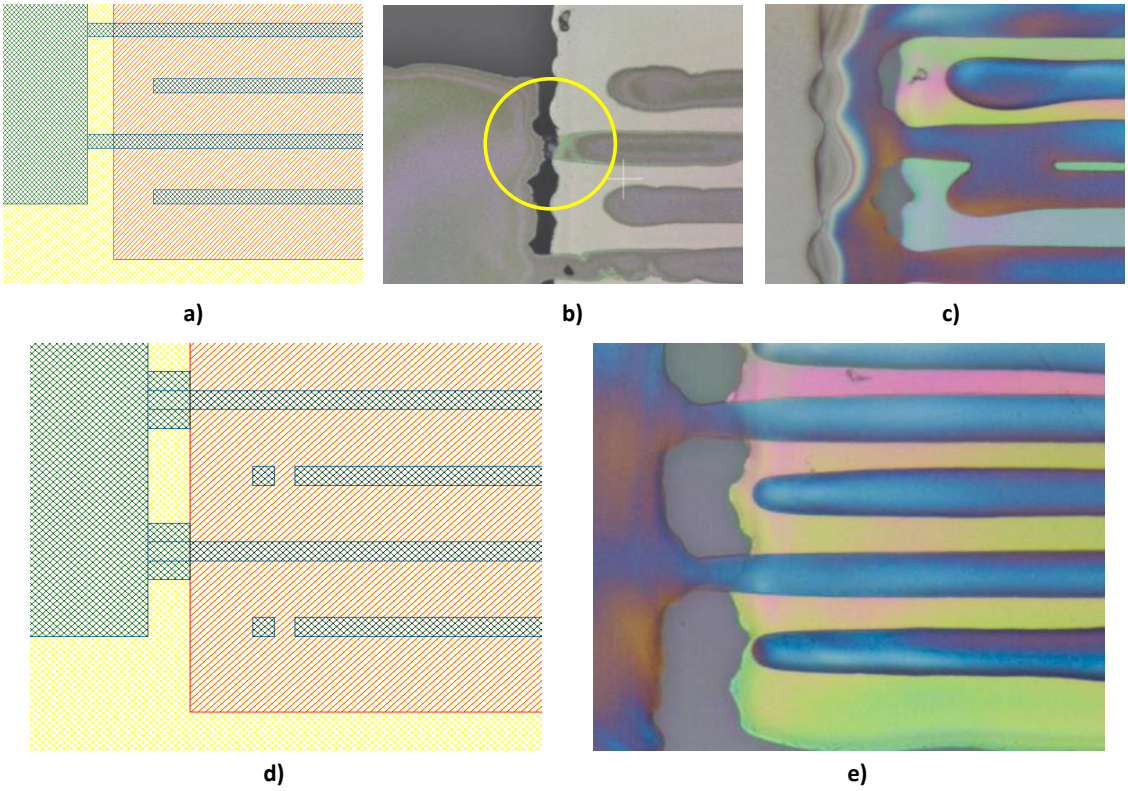


Figure 4.38. a) Layout of source & drain electrodes without compensations; b) and c) different effects occurred to non-compensated electrodes and junctions; d) compensated layout; and e) compensated electrodes.

4.4.6. Organic Semiconductor

Organic semiconducting materials are excellent candidates to be employed as hole transporting layers in thin film transistors. There are several essential requirements for a hole transporting layer material. The formulation must have an appropriate shelf life and stable viscosity, without aggregation, gelation or degradation.

There are several essential properties that the deposited thin film must fulfil. Electrochemical stability is essential in both the storage and operation state, in particular,

resistance to oxidation from ambient air and moisture is required. The film does not have to require additional alignment or passivation layers, or extensive thermal treatments. All thermal treatments must be compatible with the processing temperature limits of the device stack, including the substrate. The electrical performance of the semiconductor must satisfy the requirements of the application when deposited at high throughput.

And finally, the solvent used must be suitable for the environmental legislation of the end-user, and be appropriate for the deposition technique employed, in our case inkjet printing, including optimization of the rheology, evaporation rate, surface tension, flammability etc.

The semiconductor materials used in this chapter were provided by Flexink Inc (UK) in a solvent tetrahydronaphthalene (Tetralin) based formulation. FS0027 is an organic semiconductor formulation containing a polymer semiconductor dissolved in Tetralin solvent at 4 wt %. The formulation is easily deposited and fabricated, requiring only solvent removal and no extended annealing conditions. The data provided by Flexink using partially printed devices show that thin films are amorphous with isotropic mobilities of up to 5 x 10^{-3} $cm^2/V \cdot sec$ and I_{ON}/I_{OFF} ratios up to 10^3. This polymer is completely air stable and can be described as easy to use. FS0027 can be employed in both top and bottom gate transistor architectures, with a range of common organic dielectrics. Deposition can be carried out by spin coating and inkjet printing. All processing and fabrication can be performed in ambient atmosphere. The thin film is stable under ambient conditions. The solution degrades under prolonged exposure to visible and UV light. So, the OSC formulation should be stored at room temperature or lower, in the absence of light.

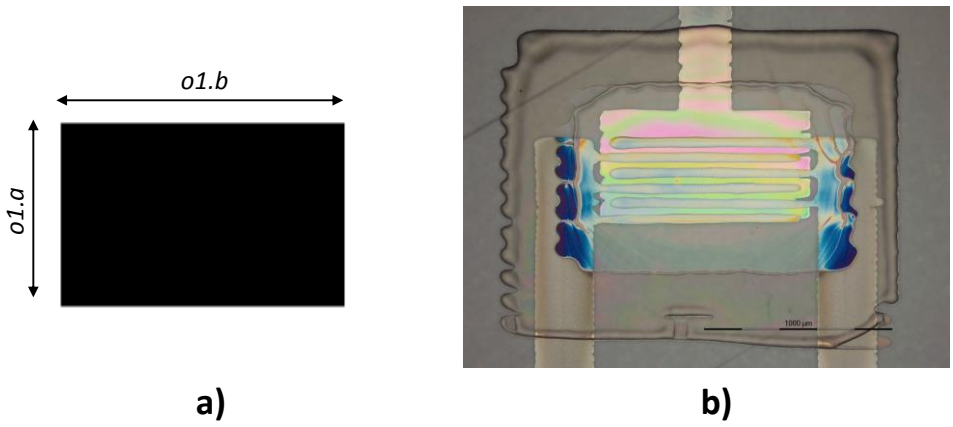


Figure 4.39. a) Layout pattern for the OSC layer; and b) printed pattern of the OSC layer on top of the dielectric and S/D layers.

The OSC was deposited on top of the source/drain and dielectric layers. Oxygen plasma treatment was applied in order to improve the deposition of the FS0027. Thanks to this step,

the OSC forms an almost uniform layer. If the oxygen plasma is not applied the OSC layer behaves as "hydrophobic" on the c-PVP layer and it suffers a huge crystallization as well.

Printing of the OSC was achieved with the layout pattern shown in Figure 4.39a. The printing of the organic semiconductor was done with different drop spacing values for the printed OTFTs. A suitable drop spacing to print on top of the c-PVP and source/drain layers was 25 µm. Printer's plate was heated at 35°C to control the spread of the deposited droplets in order to obtain an uniform layer of the OSC because the droplets are partially sintered when fall onto the dielectric and S/D layer. Once the printing is accomplished, wet layers are cured at 120°C for 15 min on a hotplate or 1 hour on a convection oven.

The resistance between the S/D terminals was measured before and after printing the OSC layer to extract its electrical behaviour. Following values were obtained for resistance before, 1270 ± 340 MOhm (two probe measurement), and after, 340 ± 60 MOhm, depositing the OSC on top of the source/drain interdigitated electrodes.

The drawn and printed patters obtained by optical analysis are listed in Table 4.7.

Table 4.7: Comparison of dimensions of layout pattern and printed pattern of the OSC layer.

Layout pattern [µm]	Printed Pattern [µm]	Deviation
o1.a= 860	1021.86 ± 30.58	15.84%
o1.b= 1400	1489.11 ± 35.94	5.98%

The waveform used for printing the OSC FS0027 ink is shown in Figure 4.40.

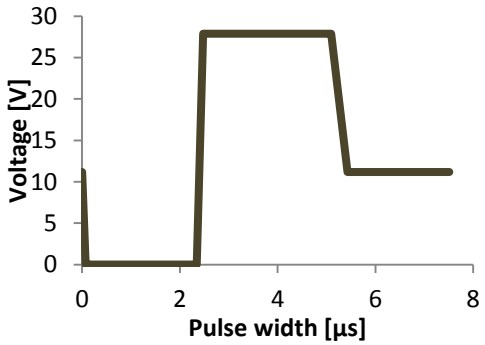


Figure 4.40. Waveform for FS0027 ink using 10 pL printheads on DMP2831[30].

A process using oxygen plasma was required in order to improve OSC printability. Figure 4.41 shows different results obtained by printing the OSC on the source/drain electrodes.

[30] Source: TUC.

Due to the different surface energy of silver and c-PVP, no continuous layer formation is obtained. Most of the materials agglomerated in the middle of the printed layer, as shown in Figure 4.41a. OSC forms isolated big drops mainly glued to silver electrode fingers because the silver layer attracts more FS0027 in comparison to the c-PVP.

Further investigations were carried out to improve the layer formation of the OSC after printing applying O_2 plasma. The application of this treatment doesn't affect the c-PVP layer as already demonstrated by UPat[31] in the framework of the FlexNet EU project. In Figure 4.41b a plasma treatment has been applied. Although the layer uniformity is improved, and some active channels are formed (OSC connects the major part of source/drain fingers) a non-complete homogeneous layer can be observed and OSC is basically covering silver layer regions but not the whole active area (Figure 4.41c). Finally, with a proper application of the oxygen plasma pre-treatment, a perfect deposition is obtained as shown in Figure 4.41d.

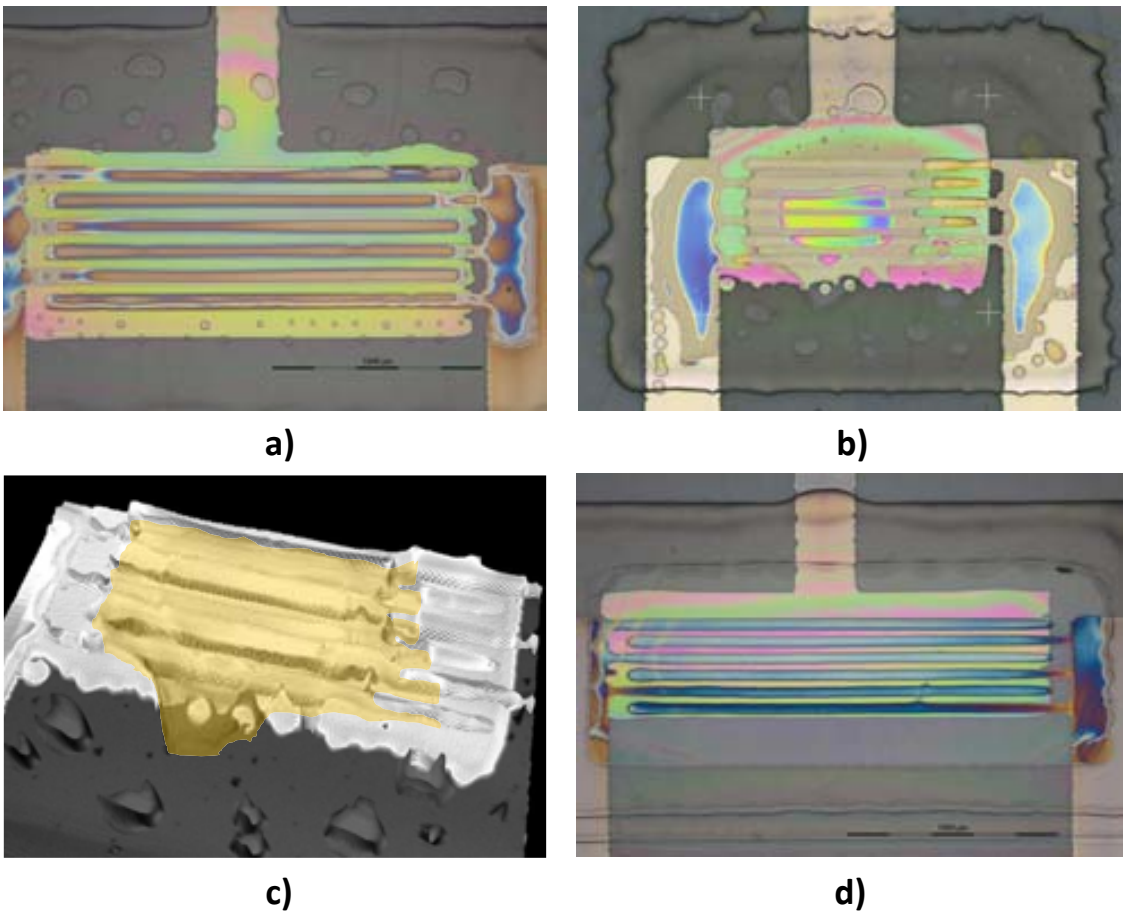
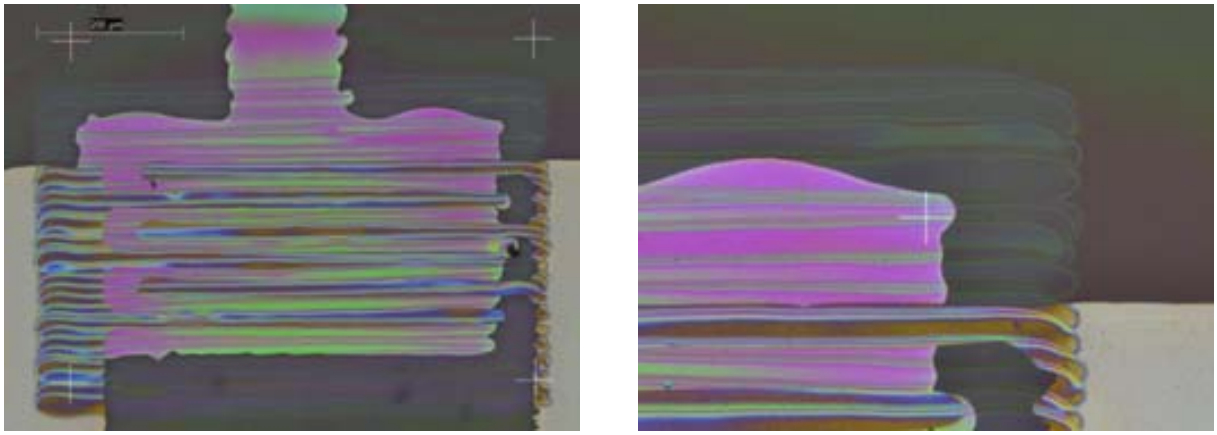


Figure 4.41. Example of plasma applied.

[31] UPat: University of Patras (Greece). Experiments done in the framework of the FlexNet EU project.

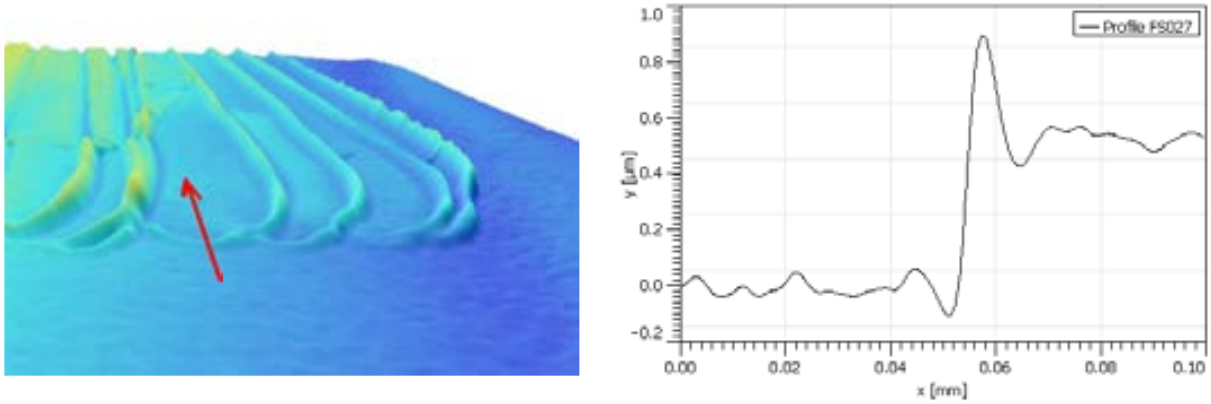
Alternatively, the deposition of a Self-Assembled Monolayer (SAM) was studied in order to improve the OSC printability over c-PVP and S/D layers to avoid the use of O_2 plasma pre-treatment. Interface modifications methods, such as SAM treatments of the dielectric surface prior to semiconductor deposition, are often used to induce ordering of the polymer film and can improve device mobility.



a) b)

Figure 4.42. OSC deposited after PFTP pre-treatment.

The PFTP treatment was performed to enhance further the deposition of the OSC avoiding the accumulation in the center. This treatment is applied by deeping the sample for 7 min in PFTP. Air and a N_2 flow are used to dry the sample. OSC (FS027) printed on understack PFTP treated.



a) b)

Figure 4.43. a) Optical confocal 3D image of a deposited OSC layer after PFTP pre-treatment; and b) cross-section profile of the OSC layer.

OSC printed lines had an average width of 50µm with a strong coffee ring stain, as it can be observed in Figure 4.42 and in Figure 4.43. Again, a drop spacing of 25 µm was used in order to reduce the OSC thickness assuring the layer uniformity with a minimum coverage of a 50%.

The thickness of the FS0027 layer obtained had an average thickness of 582,5 nm ± 29,5 nm. The coffee ring peak had an average of 2.7µm ± 0,34 µm in the horizontal walls, and 1µm ± 0,3 µm in the vertical ones.

Nevertheless, the application of such PFTP pre-process was discarded and O_2 plasma was the definitive pre-treatment process used as more homogeneous layers were obtained.

4.4.6.1. OSC FS0027 layer morphological characterization

The surface morphology of the OSC FS0027 printed on top of the OTFT stack was analyzed in the channel region. It is very flat along all channel area with a smooth surface characterized by a root-mean-square roughness of 0.26 nm as shown in Figure 4.44.

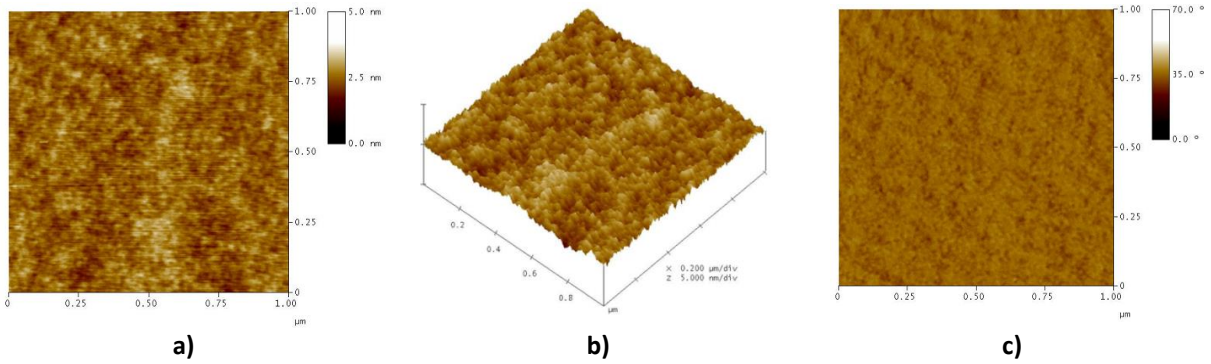


Figure 4.44. AFM images of FS0027 printed on top of Ag Bottom Gate/c-PVP/interdigitated Ag Top S/D stack: a) 2D-height; b) 3D-height; and c) 2D-phase[32].

[32] Source: ENEA.

4.5. Summary and conclusions

This chapter details the fabrication process developed to obtain organic transistors. The fundamental properties of organic semiconductors and the basic operation of OTFT were reviewed. The device architecture and materials selection considered for OTFT fabrication in this research were described.

A complete manufacturing process operation for inkjet printing including curing procedures has been developed based on the evaluated. Lab scale DMP2831 inkjet printing equipment from Fujifilm Dimatix was used as manufacturing system.

Layer geometries were designed and assembled as multilayer stacks to build-up OTFTs successfully. For the geometries, printing tolerances were taken into account related to the printing system to ensure efficient manufacturing. The manufactured layers were characterized according to the morphological and functional properties of the individual layer.

Based on the previous investigations, following materials were fixed for all devices:

- Silver ink from SunChemical as conductor
- c-PVP as dielectric
- FS0027 as semiconductor

The results in this chapter and following ones show that the c-PVP ink formulation presents several disadvantages. It is a "home-made" ink formulation. The solvent used has good properties for stable drop ejection using inkjet printing. Its electrical characteristics are satisfactory but it shows a complex film formation due to the strong coffee-ring effect. On the other hand, that effect seems also to support the development of thin layers while an area overhead is required. We could see a strong dependency of the layer thickness on the area dimensions.

Several hundreds of fully inkjet-printed OTFTs, as the one shown in Figure 4.45, were manufactured using the current recipe developed in this chapter. All devices were characterized. The analysis of the huge amount of data will be presented in the following chapters. Yields up to 78% for a fixed design were obtained.

The resulting OTFTs based on this fabrication procedure will be characterized in the following sections to demonstrate its electrical performance. Several improvement steps will be also applied, both in materials and in device geometries, to improve the results obtained in this initial process developed in order to reach higher performances and improve stability.

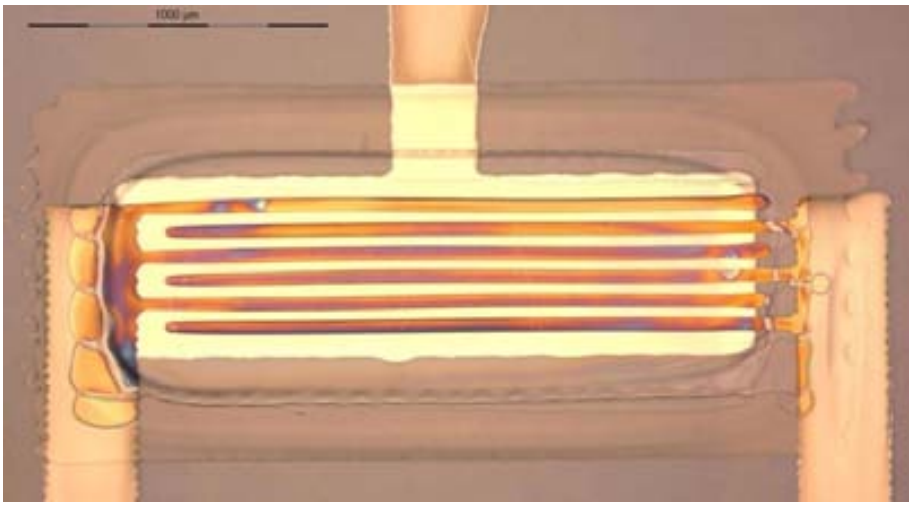


Figure 4.45. All-inkjet printed OTFT.

In conclusion, the development of a suitable fabrication process obtained after large number of experiments, material evaluations and characterizations is an outstanding result. Printing strategies and post-treatment methods have been further optimized (as will be detailed in the following chapters).

The amount of samples manufactured and analysed can also be considered as outstanding achievement.

5. CHARACTERIZATION OF INKJET-PRINTED ORGANIC THIN FILM TRANSISTORS

The present chapter is focused on the characterization of the Organic Thin Film Transistors (OTFTs) fabricated by using inkjet printing technology using the recipe developed in the previous chapter in sheet-fed configuration (S2S). Several hundreds of devices were fabricated using the device structures and geometries defined in the previous chapter. These take into account the printing tolerances related to the printing system used.

In addition to the characterization of the OTFTs, some other electrical and physical structures such as capacitors, were also characterized to obtain complementary information namely about electrical active traps. These structures are named here "test vehicles".

This chapter is organized as follows; it starts by introducing the methodology for OTFT parameter extraction. Next, the electrical characteristics and the operational stability are presented and discussed. The OTFT performance confirms that the optimized printing recipe discussed in the previous chapter is mature and can produce reliable and reasonable high performance OTFTs. Finally, the variability on OTFT parameters and yield was studied and analysed. This study required the fabrication and characterization of a large number of OTFTs (several hundred). This is considered as one of the major achievements of this work.

5.1. Introduction to OTFT electrical characterization

5.1.1. OTFT Parameter Extraction

The current-voltage relations in Equations 4.1 and 4.2 provide a simple approach to OTFT characteristics, and are used as basis for characterizing and comparing a variety of OTFT devices. Figure 5.1b, highlights some of the device parameters that need to be evaluated: effective field-effect mobility, μ ($cm^2/V \cdot s$), On/Off current ratio, Threshold voltage, V_T (V), and contact resistance and R_C (Ω) among others. Field-effect mobility parameter is the drift velocity of the charge carrier flowing through the semiconductor from source to drain when an electric field is applied. This parameter strongly affects the operation speed of the transistor and has a fundamental importance when fast logic circuits are required. In addition, μ is used as a figure of merit for evaluating the performance of semiconductor materials. A high mobility, as well as high On/Off current ratio are desirable qualities for OTFTs. Finally, the subthreshold behaviour also assessed through the inverse of subthreshold slope, S, ($V\ dec^{-1}$).

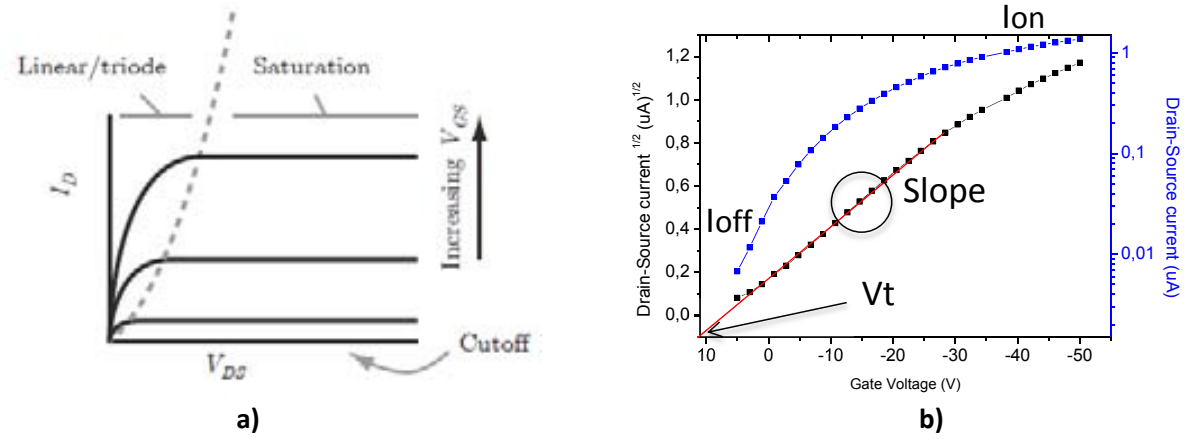


Figure 5.1. Extraction of OTFT device from electrical characteristics: a) gm - V_{GS} plot for extracting mobility and V_T, and b) I_D - V_{GS} plot for deducing I_{ON}/I_{OFF} and Subthreshold slope.

OTFTs are basically characterized by its output characteristics, $I_{DS}(V_{DS})$, and transfer curves, $I_{DS}(V_G)$, shown in Figure 5.1. In the output curve, the drain-to-source voltage (V_{DS}) is swept at different gate voltage (V_G) steps. Thus, the accumulated charges in the active channel modulate the drain-current (I_{DS}). The output-curve can be divided into two regions (Figure 5.1a, namely the linear ($V_{DS} < V_G$) and the saturated region ($V_{DS} > V_G$). The linear region is situated between the Threshold voltage (V_T) and the pinch-off point, in which I_{DS} increases linearly. In this region, the active channel is formed at V_T, and the current is not limited by the charge concentration, that is, the current has an ohmic behavior.

To extract the parameters from the transfer characteristic, the drain current is plotted versus the gate voltage in lineal and semi logarithmic plot for the saturation regime (V_{DS}=-30V), as shown in Figure 5.1b and for the linear regime (V_{DS}=-2V).

5.1.2. IEEE standard P1620™-2004

The IEEE Standard for Test Methods for the Characterization of Organic Transistors and Materials (namely P1620™-2004) describes the methodology for characterizing organic electronic devices, including measurement techniques, methods of reporting data, and the testing conditions during the characterization [159].

The purpose of this standard is to provide a method for systematically characterizing organic transistors, ring oscillators and other subsystems. Moreover, these standards are intended to maximize reproducibility of published results by providing a framework for testing organic devices, whose unique properties cause measurement issues not typically encountered with inorganic devices. This standard stresses disclosure of the procedures used to measure data and extract parameters so that data quality may be easily assessed. This standard also sets guidelines for reporting data, so that information is clear and consistent throughout the research community and industry.

The standard methods for characterizing organic transistors can be found at IEEE Printed and Organic Electronics Working Group webpage[33]. The procedures proposed were taken in account in the characterization processes developed in the current work.

[33] IEEE Standard for Test Methods for the Characterization of Organic Transistors and Materials - http://grouper.ieee.org/groups/1620/

5.2. Preliminary Organic Semiconductor Characterization

In the framework of the TDK4PE EU FP7 project, the consortium partner ENEA[34] manufactured inkjet printed bottom-gate bottom-contact OTFTs on silicon substrates. The objective was to evaluate the electrical properties of the organic semiconductor FS0027 and asses its performance in OTFTs.

The substrate consisted of a 500 µm thick highly doped Silicon (Si++) layer, thin (200 nm) SiO_2 dielectric layer and interdigitated gold source–drain electrodes fabricated by conventional techniques. The semiconductor ink FS0027 was deposited by inkjet printing, as shown in Figure 5.2.

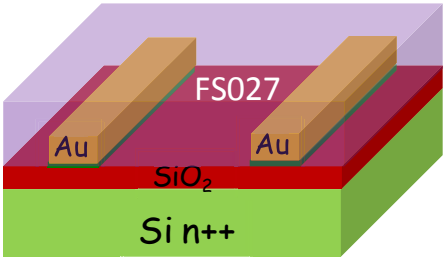


Figure 5.2. Scheme of OTFT BG-BC fabricated by ENEA in order to get information about the printed FS0027 semiconductor performance[33].

The active channels of the manufactured transistors have two possible lengths: L = 20 µm (Type I - FET1 & FET2) and L = 40 µm (Type II - FET3 & FET4), as shown in Figure 5.3a. For all devices the ratio between width (W) and length (L) of the active channels was fixed at 550. Taking into account the size of the interdigitated electrodes, the overall area printed was about 0.56 mm² for Type I devices and 1.65 mm² for Type II devices. Figure 5.3b shows the optical micrographs of the device FET4 inkjet printed with FS027 semiconductor.

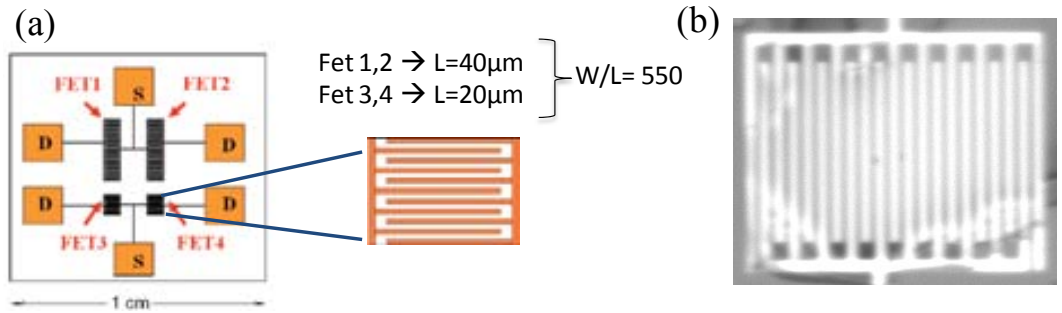


Figure 5.3. a) Schematic view of the devices (Type I devices, FET3,4 with L=20µm; Type II devices, FET 1,2 with L=40µm); and b) optical micrographs of FET4 with FS027 deposited[33].

[34] ENEA: National agency for new technologies, Energy and sustainable economic development (Portici Research Center - Italy).

ENEA performed the electrical measurements at room temperature and in air for FS0027 semiconductor. Figure 5.4 shows the transfer and output curves of one typical OTFTs.

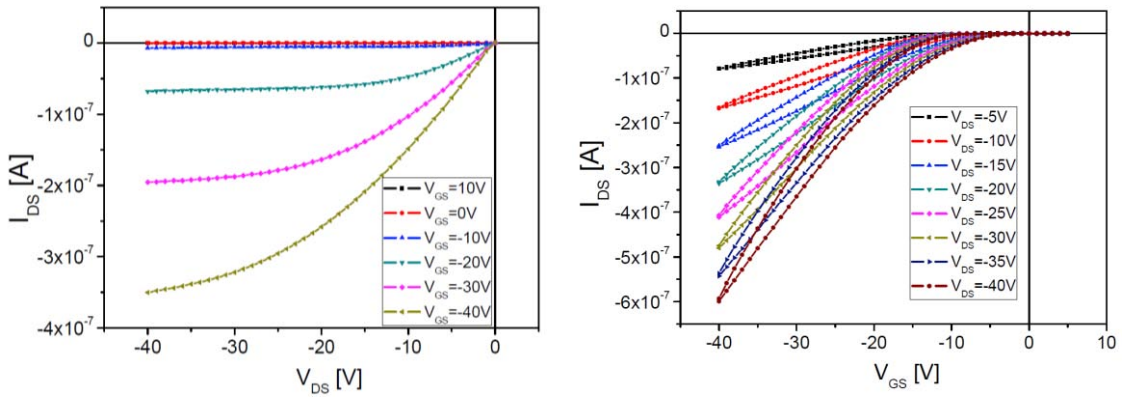


Figure 5.4. Left: Output curves; Right: Transfer curves for FET4 device[35].

For all the samples, the OTFT parameters were extracted and summarized in Table 5.1. FET3 sample showed the higher mobility ($2.5 \cdot 10^{-4}$ $cm^2/V \cdot s$). The V_T value increases probably for memory effect induced by the light illumination.

Table 5.1. Working parameters for all devices[34].

Sample	Mobility [$cm^2/V \cdot s$]	V_T[V]	I_{ON}/I_{OFF}
FET4	$1,5 \cdot 10^{-4}$	-13	10^3
FET3	$2,5 \cdot 10^{-4}$	-7,3	10^3
FET2	$0,8 \cdot 10^{-4}$	-6,1	10^3
FET1	$1,8 \cdot 10^{-4}$	-7,5	10^3

The goal of these preliminary experiments was to extract the mobility and Threshold voltage for FS0027 semiconductor using a well-known set of materials, and to use these results as a benchmark to compare with the all printed devices developed in the framework of this work.

For FET1 device, also dynamic gate-bias stress measurements were carried out. In Figure 5.5 left, I_{DS} vs. time is shown by changing gate bias from V_G = - 40 V to V_G= - 30 V. Also, in Figure 5.5 right, static gate-bias stress analysis is reported by measuring the transfer curve at different times while the gate bias (V_G= -40 V) is continuously applied.

[35] Source: ENEA.

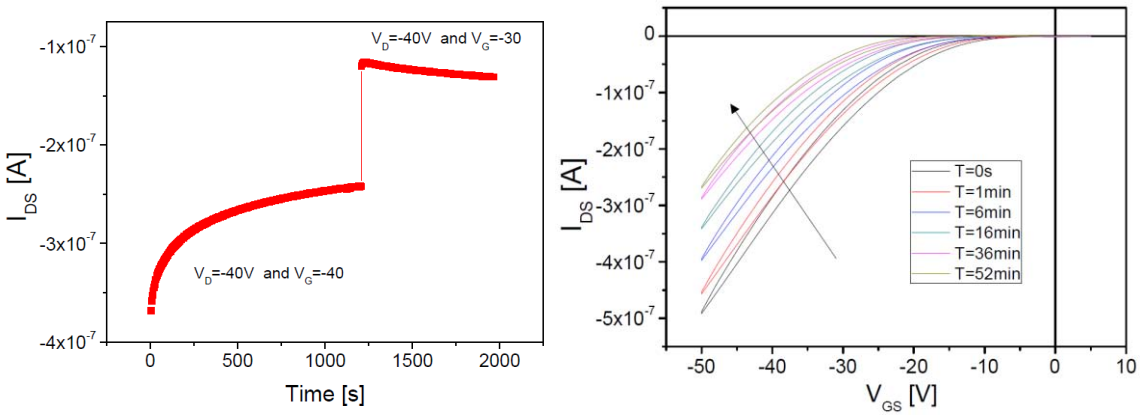


Figure 5.5. Left: Dynamic bias stress for FET1 device. Right: Static bias stress for FET1 device[36].

Static gate-bias stress causes a shift on V_T. Apparently, the field effect mobility also decreases with time under static stress as shown in Figure 5.6. However, this decrease is small and may be an artefact caused by a wrong estimation of the slope of the curved transfer curve. A trap filling mechanism at the dielectric surface causes gate-bias stress and this process should not cause changes in the mobility.

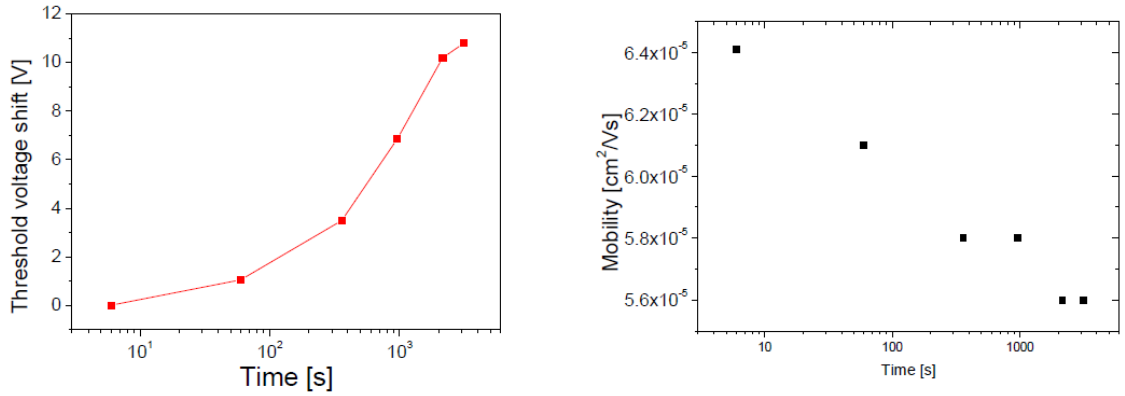


Figure 5.6. Left: V_T shift Right: Mobility vs time for FET1 by static bias stress[35].

The mobility remains almost constant while V_T follows the exponential law (in accordance with the literature of Weibull distribution) [152]:

$$\Delta V_T = V_0 \left\{ 1 - exp\left[-\left(\frac{t}{\tau}\right)^{\beta} \right] \right\} \qquad Eq.\ 5.1$$

where ß=0.56±0.06 and $\tau = 2.1 \cdot 10^4$ sec.

[36] Source: ENEA.

5.2.1. MIS structures as a precursor of OTFT

The Metal-Insulator-Semiconductor (MIS) capacitor structure consists of a dielectric/semiconductor interface sandwiched between two metal electrodes The MIS can be seen as a precursor to the Field-Effect transistor (FET) as the basic difference between them is that a transistor has two electrodes (source and drain) connected in-plane in the semiconductor. The MIS is a valuable device for studying and characterizing the electrical behaviour of transistors [142].

The capacitance–voltage (C–V) measurement is a powerful and commonly used method of determining the gate oxide thickness, substrate doping concentration, Threshold voltage, and flat-band voltage in MIS structures. The C–V curve is based on small signal impedance measurements and usually measured with a C–V meter (Figure 5.7a), which applies a DC bias voltage (V_G), and a small sinusoidal signal (1 kHz–10 MHz) to the MIS capacitor and measures the capacitive current with an AC ammeter.

C-V measurements provide information about the establishment of an accumulation layer and the corresponding Threshold voltage (V_T). Thus, measurements of capacitance as function of the voltage provide information about undesirable electronic states (traps) present at the dielectric/semiconductor interface and inspect for diffusion of ionic species within the dielectric layer.

In the followings sections, all charge induced by the gate in an OTFT was assumed to be free charge. In particular, organic materials, or amorphous materials in general, have a large density of traps. This means that not all charge induced by the gate will contribute to current. The effective mobility can become temperature and/or bias dependent, a phenomenon often observed. Although the immediate effect of a trap is similar to doping, there are differences between charge states of the traps and dopant levels. Both are derived from band, but whereas a dopant becomes neutral when capturing the charge from the band, a trap becomes charged when a charge is captured.

Electronic trap states in organic semiconductors severely affect the performance of such devices. For organic thin-film transistors TFTs or MIS structures, for example, key device parameters such as the effective charge mobility, the Threshold voltage, as well as the operational and environmental stability are considerably influenced by trap states at the interface between the gate dielectric and the semiconductor.

Trapping effects cause hysteresis in the C-V curves, the direction of the hysteresis loop indicates whether the trapped charges are injected from the semiconductor or move in the insulator toward the interface. Clockwise loop indicates electronic charge mechanism, and anticlockwise indicate a movement of mobile ions in the dielectric as shown in Figure 5.7b.

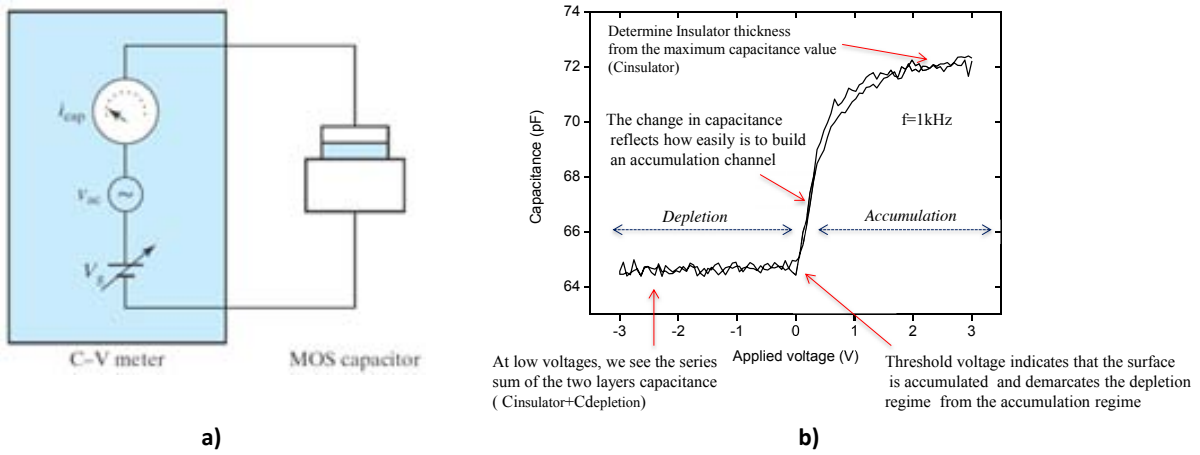


Figure 5.7. a) Setup for the C-V measurement; b) the MIS C-V characteristic curve. We can see two regimes: depletion and accumulation (typical for organic semiconductors)

The capacitance of the MIS structure depends on the voltage (bias) applied on the gate. The dependence is shown in Figure 5.7b showing two regimes of operation separated by two voltages. In contrast with inorganic materials such as silicon, in organic semiconductors there is only one type of carriers: holes or electrons thereby, the inversion regime is not produced and observed in C-V measurements. The regimes are described by what is happening to the semiconductor surface. These are (1) accumulation in which carriers of the same type as the body accumulates at the surface and the MIS capacitor is just a simple capacitor with capacitance $C_{insulator}$; (2) depletion in which the surface is devoid of any carriers leaving only a space charge or depletion layer and the MIS capacitor consists of two capacitors in series: the insulator capacitor ($C_{insulator}$) and the depletion-layer capacitor (C_{dep}).

The voltage that demarcates the depletion from the accumulation regime is the Threshold voltage (V_T).

5.2.1.1. Fabrication of MIS structures

As mentioned before, the MIS structure is a precursor to the FET. In order to validate the selected combination of materials, MIS structures were fabricated and characterized electrically to find out the best receipt of material in order to obtain the highest electrical performance.

Fabrication was done using different deposition techniques to speed up the process and for a better control of material deposition and thicknesses. The experiment was focused to analyse the electrical performance issue rather than the deposition of functional materials already done in previous chapter.

The fabrication procedure followed a similar stack than those used in the OTFTs.

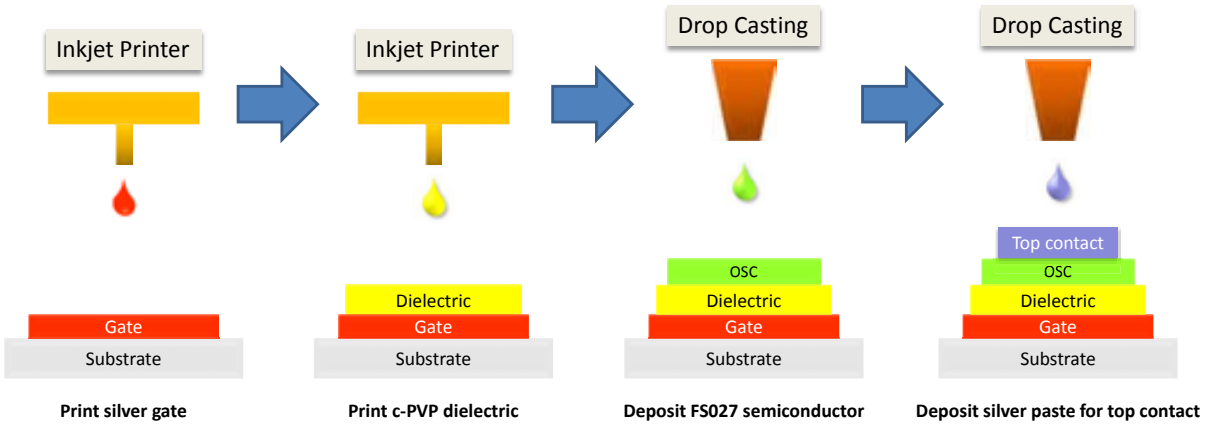


Figure 5.8. Flow of the fabrication process for MIS structure using c-PVP as dielectric and FS0027 as semiconductor.

For the bottom contact, Sunchemical EMD5603 silver nanoparticle ink is deposited using the Dimatix DMP2831 inkjet printer. A drop spacing of 20µm and a substrate holder temperature of 40ºC was used as in previous chapter. The ink was cured at 130ºC for 30 minutes in a convection oven. One layer of silver ink was deposited and its thickness was 500nm.

Following, the dielectric c-PVP was deposited by inkjet. Different number of layers of dielectric was printed with the following printing conditions: drop spacing of 20 µm, cartridge temperature set to 28ºC and a substrate holder temperature of 40ºC. Post-printing procedure for inkjet consists on baking the sample at 200ºC for 20 minutes on convection oven. The thickness obtained for one layer was 300nm by inkjet deposition. As demonstrated before, layer morphology is very planar and uniform, although presents an important "coffee ring" effect at the edges.

The last but not the least step is the deposition of semiconductor by drop casting. This technique was used to avoid the time-consuming step of the printer. Moreover, since the device is a stack of materials, no accuracy of semiconducting placement is required. The layer thickness is around 100-300nm (these values can range because of the non-accurate manual deposition). Post-printing procedure consists on baking the sample at 120ºC for 15 minutes in oven.

A drop of silver adhesive paint (ELECTROLUBE SCP03B) was deposited by drop casting and used as a top contact. Silver adhesive paint cures in open air and don't create additional thermal stress to the underneath layers.

5.2.1.2. Characterization of MIS structures

The electrical characterization of MIM structures provides valuable information about the quality of the dielectric/semiconductor interface established between the semiconductor FS0027 and c-PVP dielectric.

Capacitors where characterized by using small signal impedance techniques, mainly, C-V in a specified frequency. Measurements were done in vacuum, under dark conditions and at room temperature. Figure 5.9 shows the C-V measured at 1 kHz for c-PVP/FS0027 stack.

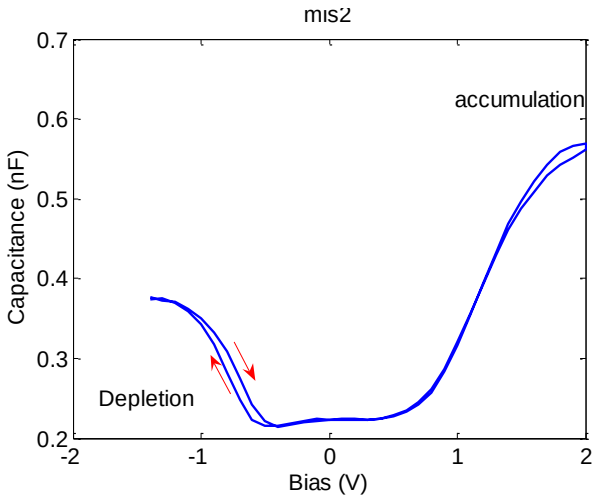


Figure 5.9. Capacitance-Voltage (C-V) measured at 1 kHz de accumulation is clearly visible under positive bias on the top silver electrode. However, the capacitance also rises in depletion. The MIS capacitor is a top gate c-PVP (as dielectric) and as semiconductor was used Flexink FS0027 (drop-casted).

The electrical characterization of the MIS capacitor reveals that although both materials are fully printed a dielectric/semiconductor interface is still formed. C-V measurements shown that under accumulation (positive bias on the top silver electrode) the capacitance rises and reaches a constant value corresponding to the capacitance of the insulator layer as expected (see Figure 5.9). This in agreement with the build-up of an accumulation layer at the dielectric/semiconductor interface

The rise in capacitance begins at 0.5 V. The C-V characteristics have then a Threshold voltage (V_T) of 0.5 volts. This can be interpreted as a sign that slightly trapping occurs at the dielectric/semiconductor interface. As the direction of the hysteresis loop is clockwise, the charged traps are injected from the semiconductor toward the interface.

C-V characteristics of the MIS capacitors often shows some additional features caused by the presence of relatively fast responding interface states and deviations from the standard behaviour attributed to a DC leakage, for instance in Figure 5.9, can be observed an unusual rise in capacitance under weak depletion. This phenomenon is still elusive.

5.3. Electrical characterization of all-inkjet fabricated OTFTs

In the previous chapter, a complete procedure for the fabrication of all-inkjet printed OTFTs was developed using c-PVP as dielectric and FS0027 as OSC. In this section, the transistors manufactured were characterized and reviewed deeply to show the characteristics and best performance of the baseline technology developed.

5.3.1. Electrical Characterization of the OTFTs fabricated

The OTFTs were characterized by a Semiconductor Analyser Agilent B1500A with 4 High Resolution Sources and a Suss EP6 manual Probe Station. The set-up configuration is shown in Figure 5.10. The measurements were done in air and at room temperature.

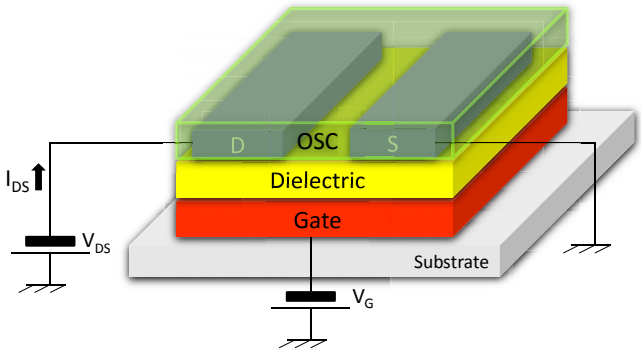


Figure 5.10. Set-up for the I-V measurements of printed OTFTs.

Two OTFT foils were designed and fabricated with different device geometries and W/L ratios. The designs are shown in Annex C.9 and Annex C.10. Among other device geometries (used in next chapter), in this chapter the transistors were fabricated following the Table 5.2.

Table 5.2. OTFT geometries and W/L ratios of fabricated OTFTs.

OTFT reference	L [µm]	finger length [µm]	# of fingers	W [µm]	W/L ratio
T40/5E3	40	1000	6	5E3	125
T40/10E3sl	40	1000	11	10E3	250
T40/10E3sl2	40	500	21	10E3	250
T40/10E3	40	2000	6	10E3	250
T40/20E3	40	2000	11	20E3	500
T40/30E3	40	2000	16	30E3	750
T40/40E3	40	2000	21	40E3	1000

Among all the fabricated transistors, the best results were obtained for the device geometries of (i) large-finger and (ii) short-finger design both with W/L ratio of 250 and similar areas of dielectric and OSC, Figure 5.11 and Figure 5.14 show the layout of these OTFTs. The main difference resides in the transistor geometry. The first one has a horizontal device geometry having large fingers (2000 µm) and the second one has a vertical device geometry having short fingers (500 µm) and named *slim* (*sl* in the OTFT reference).

In the next chapter, we will study these transistors presented due to its best performances in comparison with the other device geometries and sizes.

5.3.1.1. Large-fingers OTFT

Figure 5.11a shows the layout of the OTFT named *T40/10E3* (reference C3 in the layout) with a W/L ratio of 250 and 6 large fingers of 2000 µm length each one. Figure 5.11c, Figure 5.11d, Figure 5.11e and Figure 5.11f shows the extracted layers with its physical dimensions. Finally Figure 5.11b shows an image from conventional microscope.

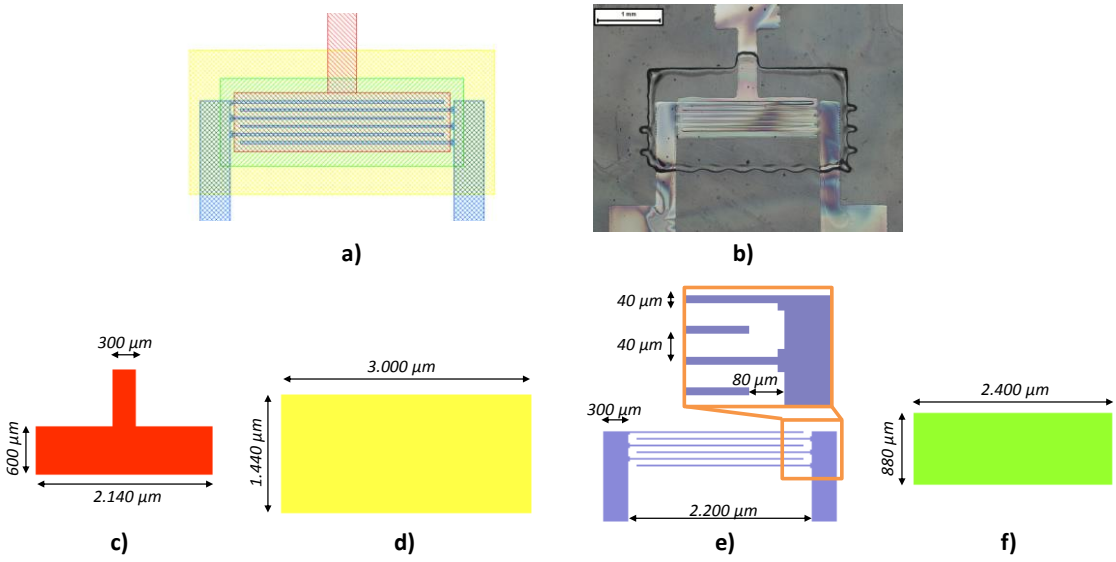


Figure 5.11. a) Layout of the large-fingers OTFT with a W/L ratio of 250; b) image of the OTFT from conventional microscopy; c) dimensions of the gate layout; d) dimensions of the dielectric layout; e) dimensions of the drain and source layout and f) dimensions of the semiconductor layout.

The channel length (L) was designed to be 40 µm. But, as previously studied, due to ink coalescence and the dielectric surface tension, the final dimensions obtained were in the range of 14.1 to 24.6 µm with an average of 19.1 ± 3.4 µm as shown in Figure 5.12b. This will be the effective channel length value used to extract OTFT electrical parameters.

Larger fingers show more homogeneous lines and provoking a reduction a 17% the deviation of the average finger width.

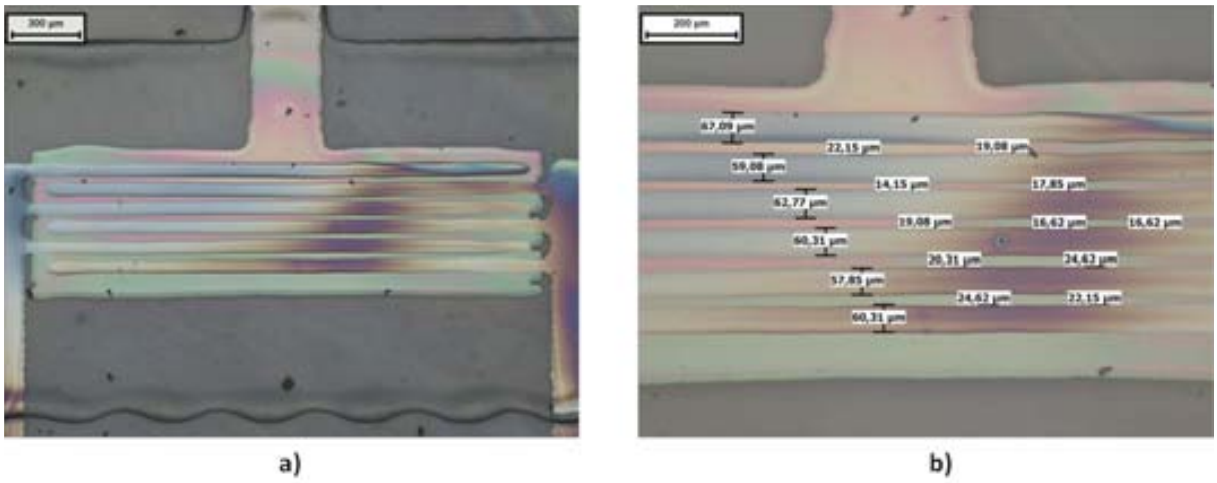


Figure 5.12. Drain and source interdigitated electrodes of the large-fingers OTFT. The measurements of L were performed by optical microscope.

The output and transfer curves exhibit the typical characteristic of an OTFT MISFET, as shown in Figure 5.13.

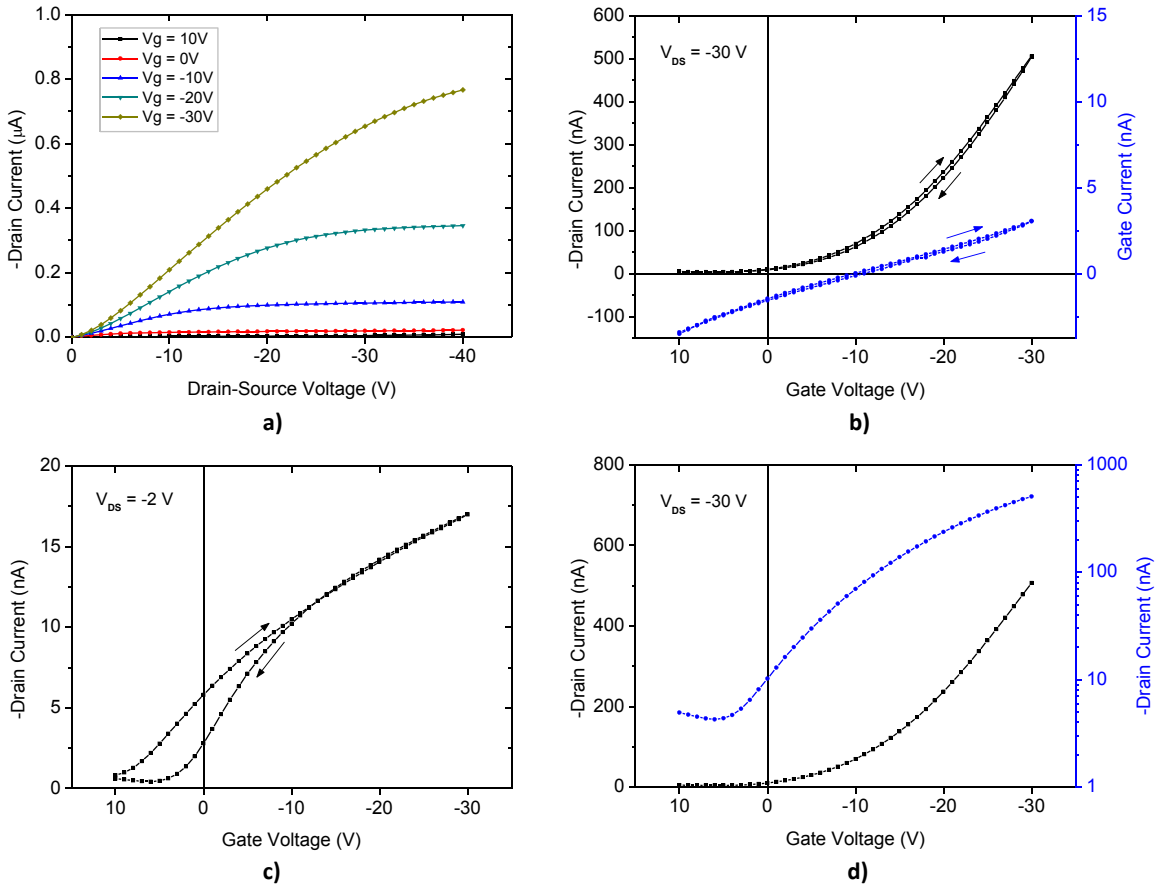


Figure 5.13. Drain-source current and gate current for Transfer and Output curves for OTFTs with V_{GS} ranging from +10 to -30V: a) Output curve with V_{DS} ranging from 0 to -40V; b) Transfer curve and Leakage current with V_{DS} = -30V; c) Transfer curve in linear region with V_{DS} = -2V; and d) Transfer curve in linear and semilog with V_{DS} = -30V.

5.3.1.2. Short-fingers OTFT

Figure 5.14a shows the layout of the OTFT named *T40/10E3sl2* (reference C6 in the layout) with a W/L ratio of 250 and 21 short fingers of 500 µm length each one. Figure 5.14c, Figure 5.14d, Figure 5.14e and Figure 5.14f shows the extracted layers with its physical dimensions. Finally, Figure 5.14b shows an image from conventional microscope.

Basically the design has a similar area than the large-fingers one. Moreover, semiconductor and dielectric areas have similar sizes although printing horizontal and vertical device geometries generates different deposited pattern behaviors.

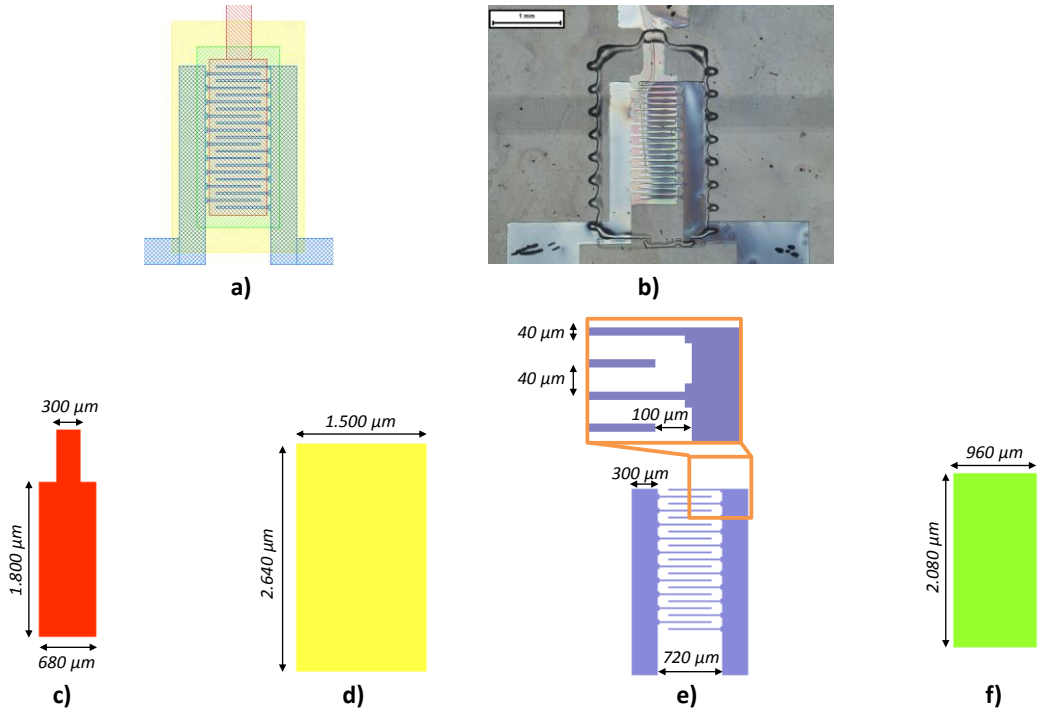


Figure 5.14. a) Layout of the short-fingers OTFT with a W/L ratio of 250; b) image of the OTFT from conventional microscopy; c) dimensions of the gate layout; d) dimensions of the dielectric layout; e) dimensions of the drain and source layout and f) dimensions of the semiconductor layout.

As in previous design, the channel length (L) was designed to be 40 µm. But due to ink coalescence and the dielectric surface tension, the final dimensions obtained were in the range of 11.3 to 37.5 µm with an average of 22.6 ± 8.5 µm as shown in Figure 5.15a.

The results reveal that the L parameter is less homogeneous in terms of morphology than the large-fingers device geometry due to different printing effects as bulging at the end of the finger lines. This effect can help to obtain shorter channel lengths but, as shown in Figure 5.15b, it can easily produces shortcuts between source and drain electrodes thus reducing final yield of devices and circuits.

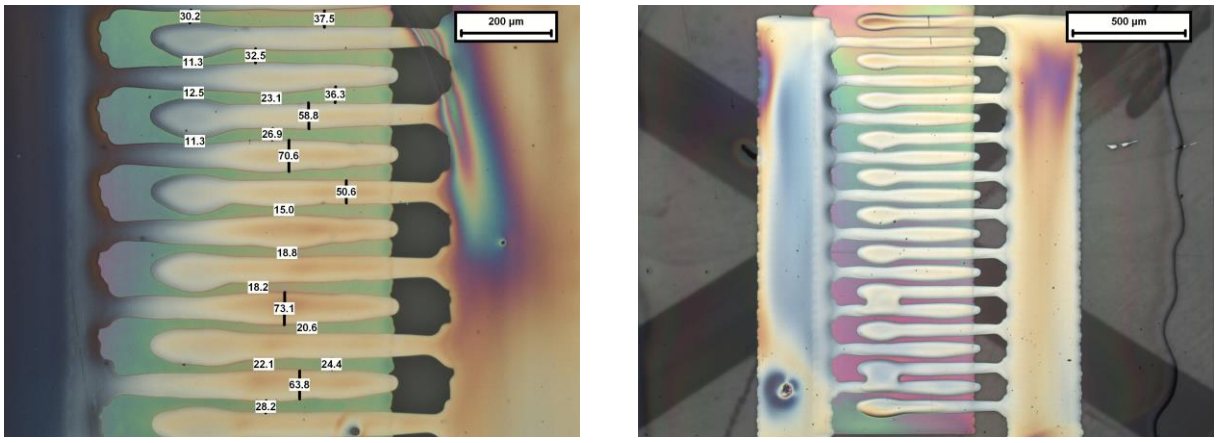


Figure 5.15. a) Drain and source interdigitated electrodes of the printed OTFT. The measurements of W and L were performed by optical microscope. b) Shortcuts between source and drain electrodes due to bulging at the end of the finger lines.

The output and transfer curves exhibit the typical characteristic, as shown in Figure 5.16.

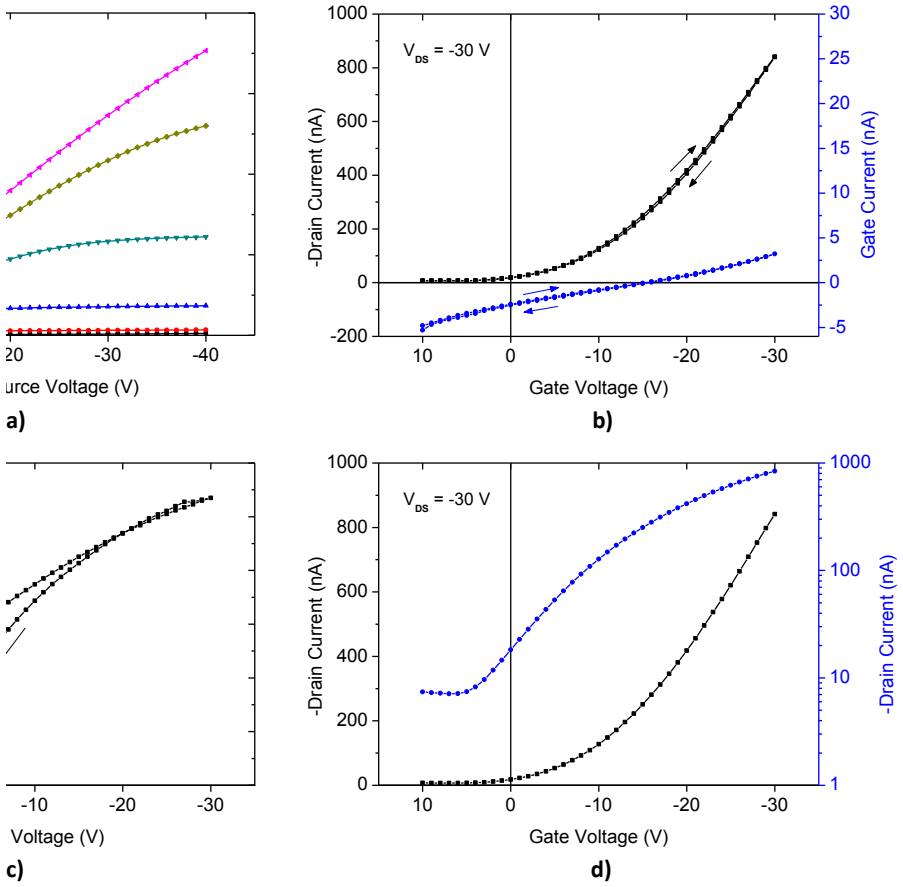


Figure 5.16. Drain-source current and gate current for Transfer and Output curves for short-fingers OTFTs with V_{GS} ranging from +10 to -30V: a) Output curve with V_{GS} ranging from +10 to -40V and V_{DS} ranging from 0 to -40V; b) Transfer curve and Leakage current with V_{DS} = -30V; c) Transfer curve in linear region with V_{DS} = -2V; and d) Transfer curve in linear and semilog with V_{DS} = -30V.

5.3.2. OTFT ideality

The mismatch between OTFTs is caused mostly by variations in the apparent Threshold voltage as estimated from the saturation transfer curves (see Figure 5.13b and Figure 5.16b). The variations on the Threshold voltage and in the Off-current are not intrinsic. This is because the device is susceptible to gate-bias stress which causes a decrease in the Off-current and an increase the Threshold voltage under continuous operation. Basically, when OTFTs are being operated their electrical characteristics change with time [160]. The problem is due to the fact that the threshold gate voltage gradually shifts to the gate bias voltage that is applied. This phenomenon is called the "bias-stress effect".

Silver contacts limit the carrier injection for I_{DS} current above 1 μA. For this reason I-V curves were measured for gate voltages below -30 V. Although, the devices suffer from gate-bias stress, they recover relatively fast their original performance when left under rest (unbiased). The kinetics of this process remains elusive.

Ideally, the Threshold voltage is extracted by fitting a straight line in a transfer curve in the saturation region and extrapolating to I_{DS} =0. However, extracting the Threshold voltage in this way is not easy since it depends on the point of the curve used; both mobility and V_T depend on V_G thus depending on the bias point considered.

The correct procedure for extracting the Threshold voltage is first linearizing the curves by taking the *nth* root of the current. The Threshold voltage can then be found by extrapolation as before. Figure 5.17 shows such linearized curves for short- and large-fingers OTFTs.

This procedure assumes that the transistor current is described by the following equations:

$$DS_{lin} \quad FE C_i \left(\frac{W}{L}\right)\left(V_{GS} - V_T - \frac{V_{DS}}{2}\right)^{1+\gamma} V_{DS} \qquad \textit{Eq. 5.2}$$

in the linear zone, where $V_{DS} < (V_{GS} - V_T)$ and

$$DS_{sat} \quad - \quad FE C_i \left(\frac{W}{L}\right)(V_{GS} - V_T)^{2+\gamma} \qquad \textit{Eq. 5.3}$$

in the saturation zone, where $V_{DS} \geq (V_{GS} - V_T)$.

To study how real devices deviates from ideal ones, the GAMMA (γ, highlighted in red) parameter and the Threshold voltage (V_T) are used. V_T and γ are parameters (figures of

merit) indicating the deviation from the ideal OTFT behavior. An ideal (trap-free) OTFT should have γ=0 and a V_T= 0V.

The γ parameter is related with the number of immobile charge density. Therefore, is most determined by the fabrication procedures. It does not depend on gate bias-stress. Contamination from environment may change it with time.

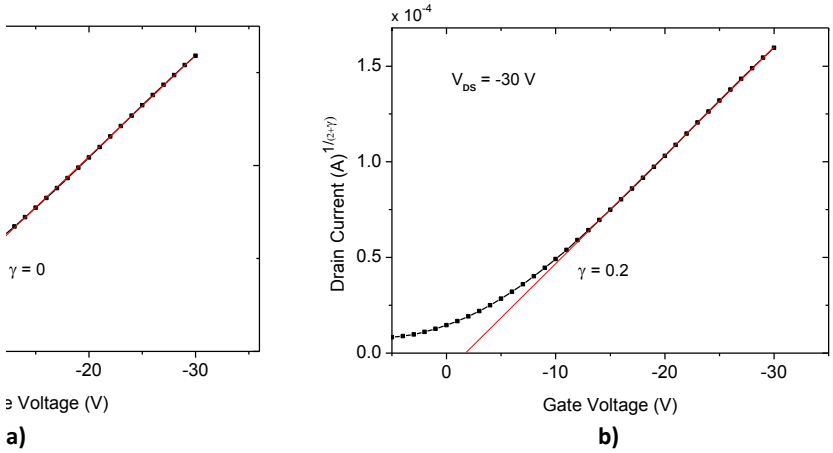


Figure 5.17. Fit to the transfer curves for all the OTFTs measured in the saturation region V_{DS}= -30 V: a) large-fingers OTFT; and b) short-fingers OTFT.

A Threshold voltage between -0.9 (Figure 5.17a) and -1.4V (Figure 5.17b) was found for the transistors evaluated in previous subsections. Both values can be considered close to 0V as expected in an organic semiconductor. Measurements show that both OTFT geometries are closer to an ideal OTFT.

5.3.3. Static bias stress

Static gate-bias stress measurements over the time were carried out. A common way to study the operational instability in OTFTs is to electrically stress them by applying a constant voltage to the gate electrode for a prolonged period of time. To follow changes induced by the stress, the gate-bias is temporally interrupted at short time intervals and the transfer curve is measured to extract the corresponding change in V_T.

The Threshold voltage shift under prolonged operation is caused by carrier trapping in pre-existing or stress-generated deep localized states in the semiconductor, in the gate dielectric, or at the active interface. Once trapped, they no longer contribute to the current, but are still part of the electrostatic charge on the gate dielectric induced by the gate voltage, such that a higher applied gate voltage is needed to achieve the same mobile-carrier concentration and current. The release of the trapped charge over several hours could also be tracked, and it

was found that exposure to above band-gap light accelerated the detrapping process significantly [152][161].

Figure 5.18a shows the transfer curves of an OTFT with W/L ratio of 125 for different stress times with a V_{DS} = -30V. Contrary to our expectations, the main effect of the applied gate bias is a shift of the transfer curves to more positive gate voltages.

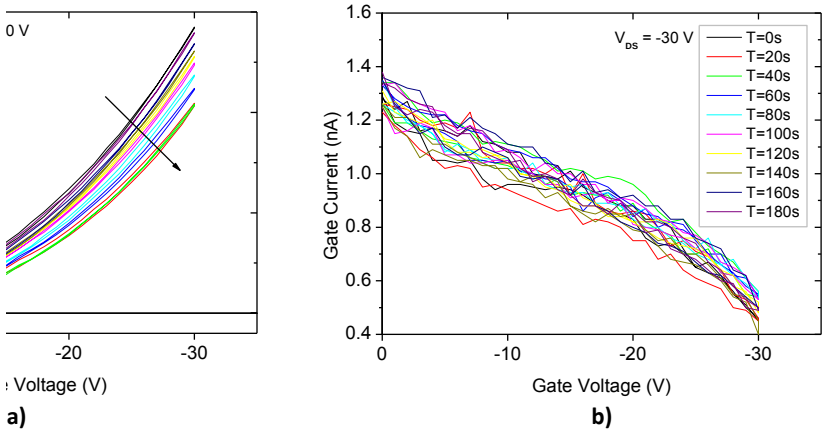


Figure 5.18. Static bias stress for an OTFT with a W/L ratio of 125: a) drain current, b) gate current.

In both device polarities, the current decreases down to 20% with source-drain voltage V_{DS} held at a constant -30V bias for 3 minutes. This behavior was observed for a large number of devices characterized. Interesting, similar phenomena has been also reported for oxide based TFTs [162][163].

The gate current does not show any significant change during the operation, as shown in Figure 5.18b. This reveals that the increase in current is not coming from gate leakage if not for an improvement in the OSC-dielectric interface performance due to its exposition to room conditions.

5.3.4. All-inkjet OTFTs preliminary electrical characterization results

The C-V measurements in MIS structures reveal that it is easy to establish an accumulation layer under bias conditions. Therefore, the interface c-PVP/FS0027 presents good electrical performance. Figure 5.13 and Figure 5.16 shows a typical current-voltage characteristic for both OTFT configurations.

Figure 5.13c and Figure 5.16c show transfer curves in the linear region (V_{DS} = -2V) over an extended gate voltage range (+10 to -30V). Curves are not perfect neither straight lines as they are showing an important hysteresis effects for low gate voltages. This suggests the presence of traps in the dielectric/semiconductor interface with negligible series contact

resistances. Transfer curves in the saturation region are not following a perfect square root behavior (Figure 5.13d and Figure 5.16d). In general, the presence of traps leads to the observation of transfer curves following power-law behaviour with the applied gate voltage.

In contrast to the typical output characteristic, the saturation of the current for high drain-source voltage is not clearly observed for high gate voltages.

As shown in Figure 5.13b and Figure 5.16b the dielectric c-PVP is not as good insulator as the SiO_2 used as reference by ENEA in Section 5.2. Despite of the low leakage current observed, the gate current is just two magnitudes less than drain-source current. A high leakage current through the gate dielectric can degrade the organic semiconductor material at the interface, as reported in literature by de Boer et al. [164].

The so-called gate capacitance corresponds to the parallel gate-drain and gate-source capacitances. Table 5.3 shows the vertical (parallel) capacitance and resistance for the parallel-plate capacitor formed between gate and drain-source electrodes in the OTFTs of the previous sections. Both measurements were done with a LCR meter at 1 KHz.

Table 5.3. Cp-Rp gate capacitance and thickness.

Parameters	**Value** ***Large fingers***	**Value** ***Short fingers***
Parallel capacitance, Cp [pF]	72.82 ± 3.9	73.81 ± 2.38
Capacitance density, Cp [nF/cm²]	9.91 ± 0.53	10.56 ± 0.34
Parallel resistance, Rp [MΩ]	165.7 ± 31.27	214.97 ± 41.94
Relative permittivity of c-PVP	4.3	4.3
Dielectric thickness (extracted) [nm]	384 ± 21.2	360 ± 11.6

The dielectric thickness was extracted based on the relative permittivity of c-PVP and the parallel gate-drain and gate-source capacitances measured and by means of confocal microscopy. Both OTFTs have similar dielectric areas showing similar dielectric thicknesses. These values are in the range reported previously (380 nm) in Figure 4.30 by means of a FIB cut.

The Cp-Rp measurement shows a uniform dielectric layer thickness and Cp standard deviation is between 3.23 and 5.35%. In opposite, Rp has a larger deviation between 18.87 and 19.51%. This reveals that the electrical isolation of the dielectric layer is not constant due to the variability of dielectric resistance causing a large deviation in leakage current and a reduction of yield as it will be demonstrated quantitatively in the following sections.

However, the value of the Off-current measured is important (in the range of 10 to 20 nA). The OTFTs studied have a built-in conduction channel (they are normally-On OTFTs). The Off-current (I_{DS} at V_{GS}=0 V) can be substantially reduced by driving the transistor under depletion (positive gate bias).

The off-current, is usually caused by a conduction path parallel to the accumulation channel. This means that although OSC layer is just some hundreds of nanometers thick, it is doped with a significant free charge density resulting in a conductive material. The ability to modulate the channel with an external gate voltage is severely hampered by this off-current, as it can be seen in Figure 5.13b and Figure 5.16b. Since only the charge in first monolayers is controlled by the gate-voltage, the other layers cause parallel conductance reducing the On/Off current ratio of the device dramatically [142] as it can be observed in Table 5.4.

A Threshold voltage between -0.9 and -1.4V was found for the fresh transistors characterized. These values are better than the obtained by the reference design fabricated by ENEA as they are closer to 0V as expected in an organic semiconductor.

Both structures show a high On-current. I_{DS} of 1.76 μA for the short-fingers structure and 1.16 μA in the large-fingers structure have been achieved for V_{DS}=-40V and V_{GS}=-40v.

Mobility in both devices has been extracted both in saturation and linear regime. The different parameters considered to calculate the mobility are listed in Table 5.3 and Table 5.4.

Table 5.4. Summary of the all-inkjet printed OTFT parameters measured.

	Max drain current	**Saturation mobility**	**Linear mobility**	**Threshold voltage**	**Off-current**	**On/Off current ratio**	**S**
	[μA]	**[cm²/Vs]**	**[cm²/Vs]**	**[V]**	**[nA]**		**[V/dec]**
	V_{DS}=-40V V_{GS}=-40V				V_{DS}=-30V	V_{DS}=-30V, 0V	
Large fingers	1.16	$1.9 \cdot 10^{-4}$	$1.8 \cdot 10^{-9}$	-0.9	10.25	49.4	34.17
Short fingers	1.76	$3.4 \cdot 10^{-4}$	$35.6 \cdot 10^{-6}$	-1.4	18.24	46.1	25.56

The best value of the semiconductor mobility is slightly higher than those obtained in the silicon reference fabrication by ENEA. It is remarkable that the mobility is almost identical in all the OTFTs.

Extraction of mobility from transfer curves in the saturation region is more appropriate because of contact effects at the OTFTs electrodes. Carrier injection limitation from the

source terminal is more noticed for low drain-source bias distorting the transfer curves in the linear regime and leading to wrong estimations of the charge carrier linear mobility.

But the performance of all the OTFTs manufactured (based on the method explained) was very limited due to charge trapping (small On-Off current ratio). A maximum I_{ON}/I_{OFF} ratio of 49.4 is observed. In future sections, better I_{ON}/I_{OFF} ratios will be reported up to 150, but far from the value of 10^3 obtained in the ENEA's silicon reference fabrication and the average value of 10^4 reported in literature by using inkjet printing. The ideal I_{ON}/I_{OFF} ratio is $>10^4$ which reduces the static power dissipation in a logic circuit.

Nevertheless, the dielectric c-PVP has a low yield, so for all the devices fabricated not all of them were working properly. This is the huge constraint of the c-PVP and a challenge for research. In later sections OTFT yield will be analysed in detail.

5.4. Stability of OTFTs under bending strain

The key advantage of OTFTs compared to traditional silicon electronics is attributed to the compatibility with flexible substrates such as plastics or paper, with regard to low temperature processing. Many examples with special emphasis on the processing of flexible substrates have been demonstrated e.g.: display backplanes, detector skin, or radio frequency circuits. However, the required "stable operation" of the devices under bending strain is still challenging due to the impact of that strain on drain current, Threshold voltage and long term stability [165].

In this section, we report the study on electrical performance of flexible OTFTs during convex bending. The bending experiments were performed on the reported OTFTs using the same materials for dielectric and semiconductor.

The different bending radii in convex direction were generated using a custom-built bending cylinder, and the electrical characteristics were measured while the devices were being bent. The electrical measurements were carried out in ambient air and at room temperature.

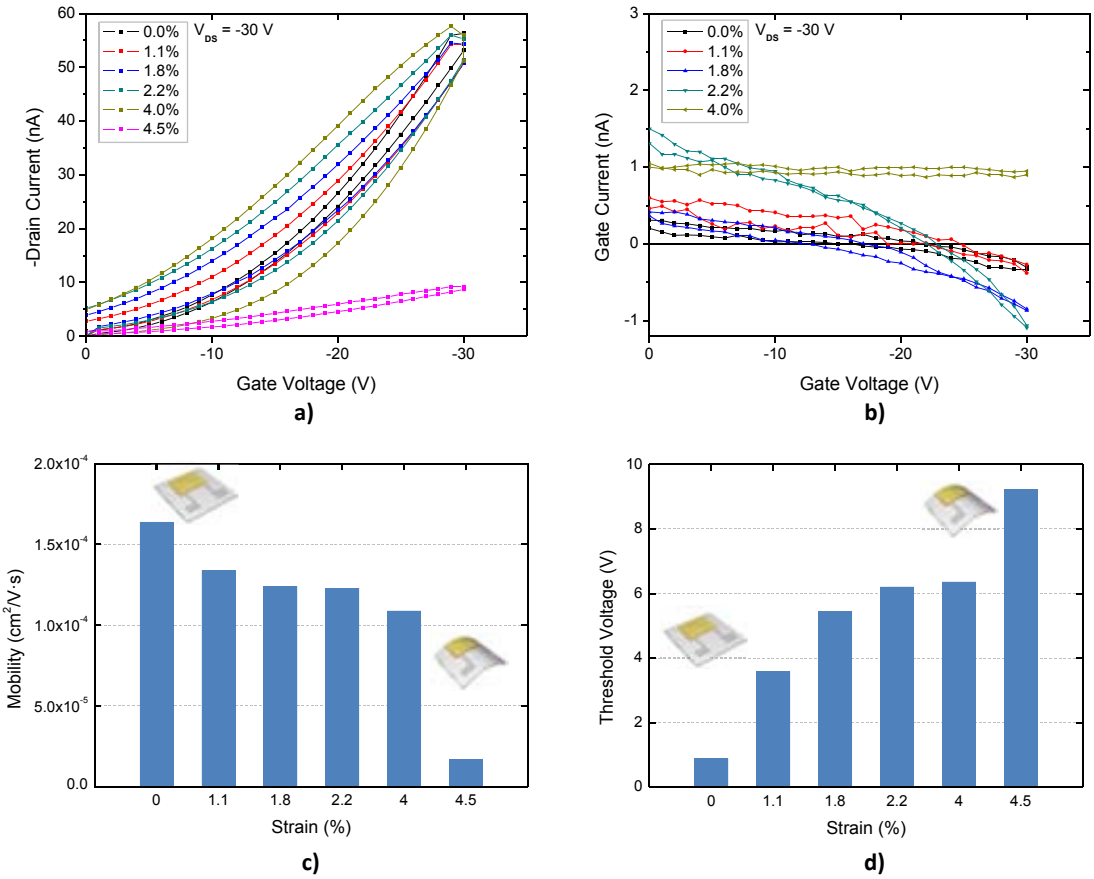


Figure 5.19. a) Transfer curve characteristics at different strains; b) gate current at different strains; c) mobility; and d) Threshold voltage of the OTFT as a function of bending radii.

The electrical characteristics for each OTFTs in function of the bending radius were performed with a convex direction with radii R of approximately 1.4 mm, 1.6 mm, 2.8 mm, 3.5 mm and 5.5 mm, corresponding to strains S of approximately 4.5%, 4%, 2.2%, 1.8%, and 1.1%, respectively (S =d / 2R, d the thickness of the substrate). Then for higher S values, lower is the bending curvature.

Figure 5.19 show the transfer characteristic, gate current, the mobility and Threshold voltage of the OTFT in function of bending radii. Before bending, good average mobility was observed according to our technology. As shown in Figure 5.19c, when the strain induced increases, the mobility on the interface c-PVP-semiconductor decreases approximately 90% (from $1.64 \cdot 10^{-4}$ $cm^2/V \cdot s$ to $1.65 \cdot 10^{-5}$ $cm^2/V \cdot s$) for a strain such as 4.5 % corresponding to a radius of 1.4 mm. Nevertheless, for low strains from 1.1 % up to 4 %, the decrease of the mobility is not significant. In contrast, the Threshold voltage increases approximately 10 V for higher strain values, as shown in Figure 5.19d. This result is in accordance with the literature [166].

5.5. Operational Stability and Reliability of all-inkjet OTFTs

One of the important questions is whether gate-bias stress effects are mainly caused by extrinsic factors, such as oxidation, presence of moisture, chemical impurities, and structural or energetic disorder of the organic semiconductor and specific structural defects causing charge trapping [152].

The choice of gate dielectric is a key factor but the polarity of the gate dielectric has a pronounced effect on the sensitivity of the device stability to moisture and ion migration. Zilker et al. [167] found device instabilities to be more pronounced in humid atmosphere than in vacuum. In a photoresist-based polymer dielectric, exposure to humidity was found to increase ion migration in the gate dielectric. In contrast to the behaviour discussed in the previous section, this causes the Threshold voltage to shift opposite to the polarity of the gate bias, that is, a negative gate-bias stress results in a positive ΔV_T, as negative ions migrate towards the active interface. Polar polymer gate dielectrics, such as PVP, are particularly prone to this effect [168], while low-k, apolar polymer dielectrics do not usually exhibit this behaviour [152].

This is closely related to the phenomenon of hysteresis observed in many OFET structures. There is clear evidence in many systems that hysteresis is due to the moisture uptake in the polar polymer dielectric. It was postulated that the common origin of charge trapping is residual water present in the organic-semiconductor films or at the active interface. Noh et al. [169] showed that the hysteresis observed in a pentacene FET with a PVP gate dielectric disappears upon annealing the device at 120 ºC in vacuum, and reappears upon subsequent exposure to moisture. We observed the same behaviour annealing the device at 100 ºC without vacuum and the procedure was used to characterize circuits that require longer characterization processes.

Other molecules diffusing into the organic semiconducting film, such as solvent molecules [170] or trace impurities in the atmosphere, can have similar effects on the bias stress stability.

5.5.1. OTFT stability over time

For a proper integration in future electronic circuits, the electrical properties of the OTFTs need to be stable over a long period of time, otherwise the lifetime of the end product would be too short to be commercially viable.

The high sensitivity of most organic semiconductors to ambient conditions or environmental influences, such as oxygen, humidity, light, and temperature, creates a huge limitation on

the performance and stability of OTFTs [171]. For example, atmospheric oxygen and moisture, as well as photo-induced oxidation have a doping effect on the organic material, causing an increase in the conductivity, which degrades the I_{ON}/I_{OFF} ratio.

Two different aspects of device stability should be considered. One is storage stability, i.e. when the semiconductor is in the neutral state. Instabilities arise when there is a thermodynamically favourable electrochemistry with oxygen and water. To avoid this, the semiconductor is designed to have low lying electronic energy levels. Thus, commercial semiconducting polymers need to be stable in ambient air and moisture.

Second is operational stability because the semiconductor here is in the charged state. Barrier layers are required to avoid reactions with oxygen and moisture since interactions with the dielectric, etc… give rise to instabilities. This can manifest in devices as hysteresis, Threshold voltage shifts and Off-current increases. Often these are not caused by the semiconductor but the dielectric or stack integrity.

Device degradation is commonly manifested as a shift of the Threshold voltage, an increase in the sub-threshold slope, a reduction of the field-effect mobility, an increase of the Off-current, and/or increased hysteresis between subsequent measurements of the transfer characteristics with increasing and decreasing gate voltage [152].

The purpose of this section is to perform a stability analysis over the time in non-coated OTFTs, being always exposed to ambient air and light. Devices fabricated were tested over three weeks until they failed to work. During that time, the devices were stored in typical ambient conditions, i.e. normal indoor light, temperature about 18-26ºC and relative humidity of 30-45%. Temperature and humidity were recorded continuously. An average of the daily temperature and humidity is shown in Figure 5.20.

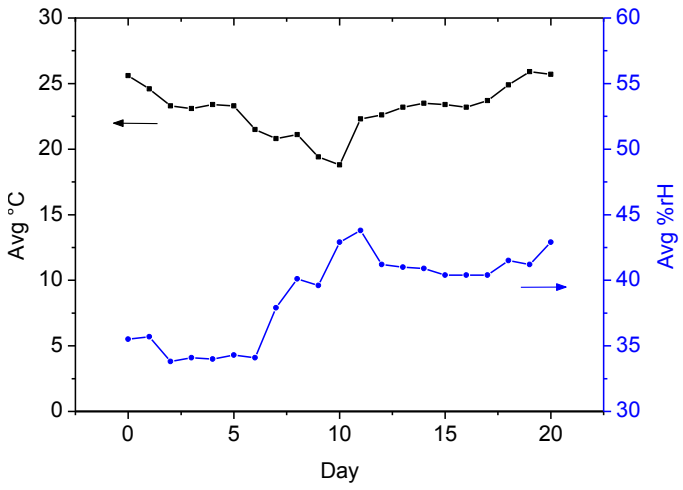


Figure 5.20. Daily temperature and humidity average.

The influence of environmental conditions over the duration OTFT of this behaviour can be easily observed in the change of the environmental conditions on the 10th day. This short change of 2 days in average temperature and humidity can be observed below drain On-current measured.

From the above results, it is clear that ingress of moisture into the organic semiconductor or presence of moisture at the interface with the gate dielectric is an important factor that degrades the bias-stress stability of many organic semiconductors.

Many polymer semiconductors easily absorb oxygen and water molecules in air and they become increasingly p-type doped. As a result of this oxidative doping, the free carrier density increases and the conductivity of the material increases resulting in a higher Off-current and lower On/Off current ratio. This effect can be observed in Figure 5.21. Off-current clearly increases during the observation period from 4.63 nA (day 0) to 55.21 nA the day before OTFT dies (day 20th).

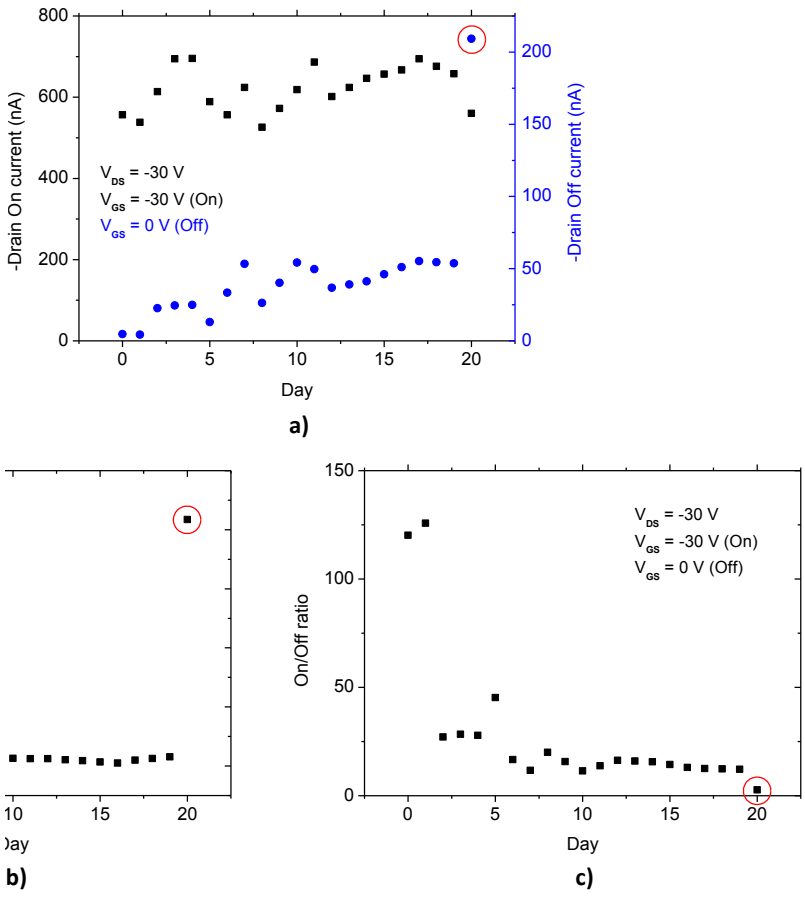


Figure 5.21. a) Drain On- and Off-currents; b) gate leakage current; and c) On/Off drain current ratio.

As expected and based on existing literature [172], after prolonged exposure to oxygen and moisture the proper transistor behaviour was lost. Oxidative doping upon air and moisture

results in an uncontrolled increase in the conductivity losing the channel modulation property of the organic semiconductor as shown in the measurements made on the day 20th. Off-current increases up to 209.15 nA reducing drastically the On/Off current ratio up to 2.68 and declaring OTFT non-functional.

Nevertheless, the main change in the transistor behavior starts just 48 hours after its fabrication and exposure to air and moisture. Although a big change in mobility and the drain current at On-state cannot be observed, this change appears in Off-current and Threshold voltage. Initially, V_T is close to zero and increases to -6.6V after 48h of exposure to ambient conditions. After that, the parameter slowly increases up to -11V after 20 days of exposure.

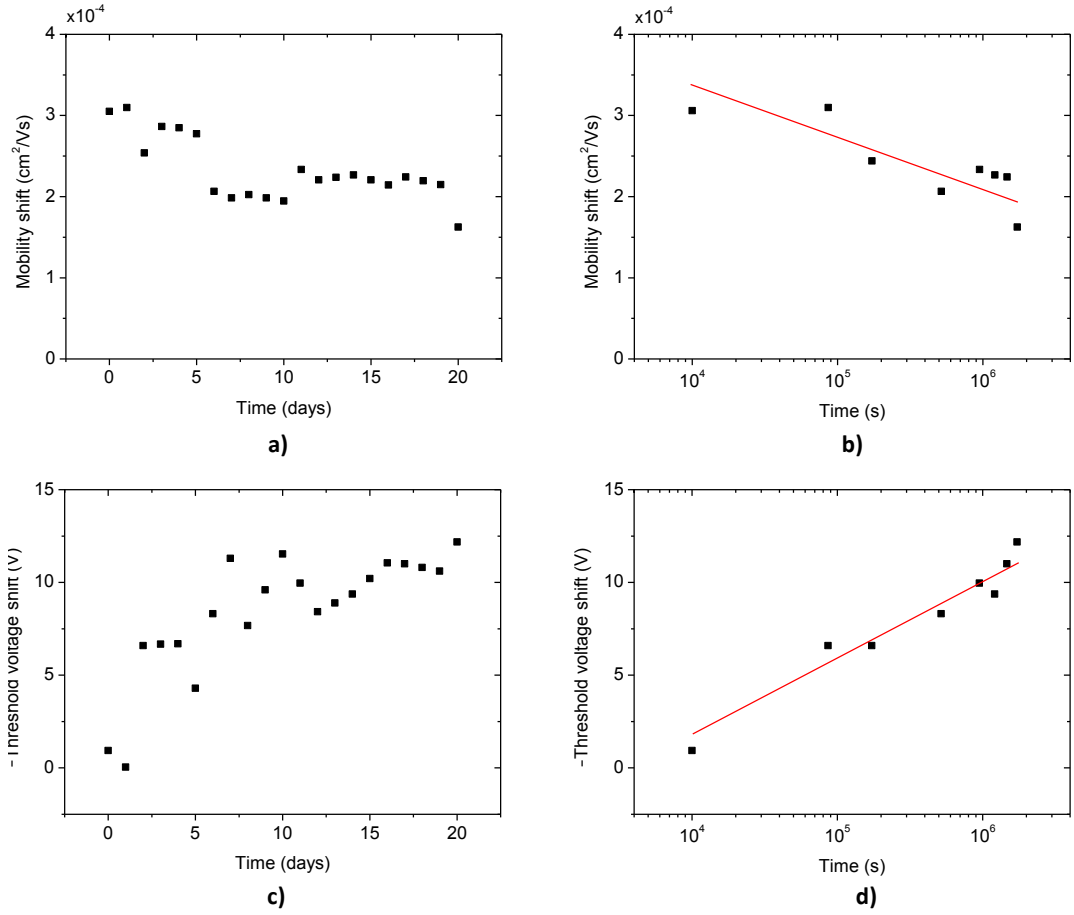


Figure 5.22. Mobility and V_T shift *vs* time by static bias stress: a) mobility shift in linear scale; b) mobility shift in Log scale; c) Threshold voltage shift in linear scale; and d) Threshold voltage shift in Log scale.

Off-current have a similar behavior as Threshold voltage. During the initial period of exposure it remains constant (4.2 - 4.6 nA). After 48h of oxygen and moisture exposure it increases up to 22 nA and continues slightly increasing up to 55.21 nA after 20 days of exposure.

By static bias stress analysis the V_T and mobility shift over the time were extracted and shown in Figure 5.22 both in linear and log scale.

As previously reported in [172], a prolonged OTFT exposure to oxygen and moisture decreases the charge carrier mobility of the organic semiconductor material. This effect can be observed in Figure 5.22a and Figure 5.22b showing a small reduction of the mobility parameter from $3 \cdot 10^{-4}$ to $2.1 \cdot 10^{-4}$ $cm^2/V \cdot s$.

The mobility shift is not significant but the Threshold voltage shift is an important stability issue. It is well-know that V_T follows a stretched exponential behavior upon time. V_T follows the exponential law (in accordance with the literature of Weibull distribution):

$$\Delta V_T = V_0 \left\{ 1 - exp\left[-\left(\frac{t}{\tau}\right)^{\beta} \right] \right\} \qquad \textit{Eq. 5.4}$$

where β=0.66 and $\tau = 5.6 \cdot 10^5$ sec. Previously, the characterization of reference transistors using conventional SiO_2 test vehicles gave β=0.56 and $\tau = 2.1 \cdot 10^4$ sec. The relaxation time τ increases one order of magnitude showing more stable operation than those fabricated using the SiO_2 dielectric structure. The V_T value increases probably for memory effect induced by the light illumination.

The magnitude of Threshold voltage shift was similar for SiO_2 (ENEA reference structure) and c-PVP gate dielectrics, suggesting that trapping occurs in defect states in the semiconductor [173].

To reduce the degradation induced by atmospheric factors, fabrication and processing can be done in an inert environment (e.g. vacuum, nitrogen). Most of the high performance solution-processed OTFTs reported in the literature involved fabrication and measurement in an inert environment to reduce unwanted doping effects.

However, long term degradation of OTFT is inevitable; thus, passivation/encapsulation layers and other strategies must be considered to extend the device lifetime.

5.6. Large-scale characterization of inkjet-printed OTFTs

Process variations present during transistor fabrication lead to a certain variability on the resulting transistor parameters. The structural disorder inherent in thin-film semiconductor leads to challenges in the design and fabrication of robust OTFT circuits, because the disorder limits charge transport and reduces uniformity across devices [152].

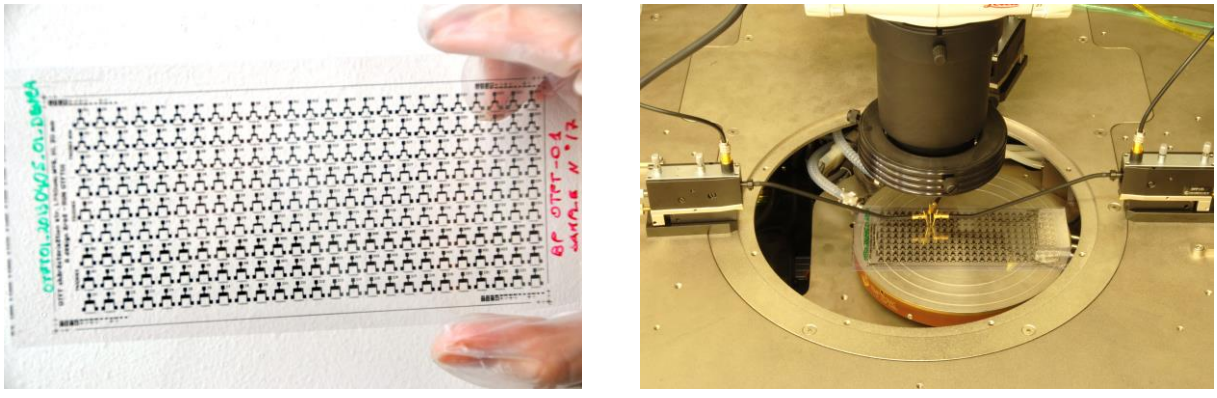
In addition, dynamic trapping of mobile charge in band-tail states results in decreasing channel current at constant bias over time [138][174]. Device variability and bias-stress instability are measured and accounted for the development of accurate device models, which in turn facilitate the design of robust circuits.

In this work, we will use the methodology to account for local parameter variations and transistor mismatch known in Si CMOS technologies applied to organic thin-film transistor technologies, and we will present a design case that makes use of design for variability [175].

In literature, considerable parameter variations have been reported for organic thin-film transistors.

5.6.1. Large-scale fabrication of inkjet-printed OTFTs

In the framework of the TDK4PE FP7 EU project, a large batch of devices was fabricated and characterized in order to analyze the scalability, variability and yield of all-inkjet printed OTFTs. OTFTs were fabricated in the consortium and characterized at IMB-CNM[37] facilities using a semiautomatic probe station. Figure 5.23 shows a printed foil and the characterization setup.



a) b)

Figure 5.23. a) Printed OTFT foil; and b) semiautomatic characterization setup.

[37]IMB-CNM: Institut de Microelectrònica de Barcelona – Centre Nacional de Microelectrònica (CSIC).

Based on the literature review, to analyse device variability and local parameter variations, we should take in account three groups of test structures:

- Matching parameters evaluation: using transistors with same channel length but different channel width.
- Matching at constant area: transistors with different aspect ratio and same channel area (short- versus large-fingers).
- Matching direction: pairs of transistors with different channel directions.

Different designs were fabricated with two different device geometries (short- and large-fingers) and different W/L ratios. The designs are shown in Annex C.11. Table 5.5 summarizes the fabricated transistors. T40/5E3sl and T40/30E3sl are short-fingers OTFT designs, and the rest are large-fingers designs.

Pairs of transistors with different channel directions were not fabricated as printing fine lines in counter direction results in very low yield devices with non-uniform channels, as already demonstrated in Chapter 2.

Table 5.5. OTFT geometries and W/L ratios fabricated in the OTFT foil design.

OTFT reference	L [µm]	finger length	# fingers	W [µm]	W/L ratio
T40/5E3sl	40	1000	6	5E3	125
T40/10E3	40	2000	6	10E3	250
T40/20E3	40	2000	11	20E3	500
T40/30E3	40	2000	16	30E3	750
T40/30E3sl	40	1000	31	30E3	750
T40/40E3	40	2000	21	40E3	1000

150 transistors of each design were fabricated totaling 900 transistors. Figure 5.24 shows some examples of the transistors printed in the OTFT foil. In the following sections the characterized devices will be analyzed.

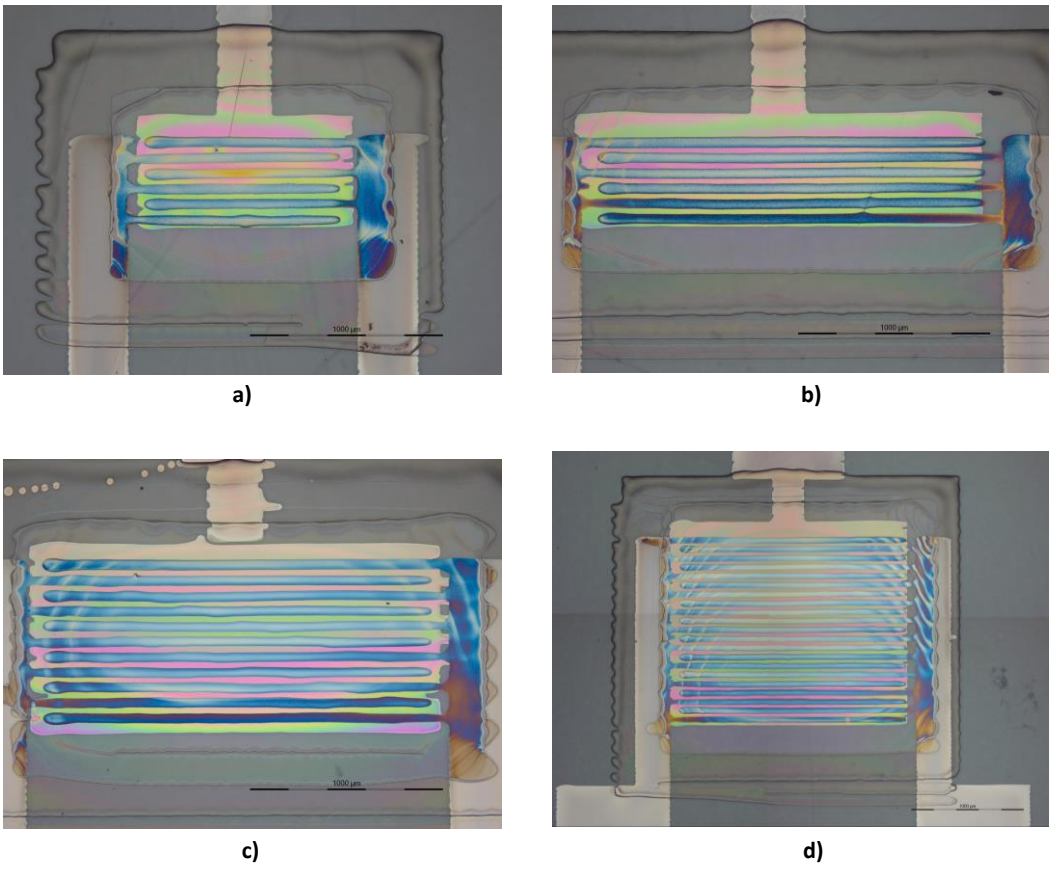


Figure 5.24. Example of OTFTs printed in the OTFT foil design: a) T40/5E3sl; b) T40/10E3; c) T40/20E3; and d) T40/30E3. Note: Pictures are not at the same scale.

In order to extract the electrical parameters, the dielectric thickness was measured by mechanical profilometer. Table 5.6 summarizes the measured dielectric size, area and thickness.

Table 5.6. Dielectric pattern size and thickness for OTFT01 design.

OTFT reference	width [µm]	length [µm]	Area [mm²]	thickness [nm]
T40/5E3sl	2000	1420	2.84	1222 ± 329
T40/10E3	3000	1420	4.26	651 ± 96
T40/20E3	3000	1820	5.46	390 ± 89
T40/30E3	3000	2220	6.66	361 ± 68
T40/30E3sl	2000	3420	6.84	360 ± 76
T40/40E3	3000	2600	7.8	300 ± 54

Although dielectric area grows linearly (as shown in Figure 5.25a) the dielectric thickness decreases exponentially (as shown in Figure 5.25b). This effect was previously identified in the Chapter 3 when MIM structures were developed and characterized.

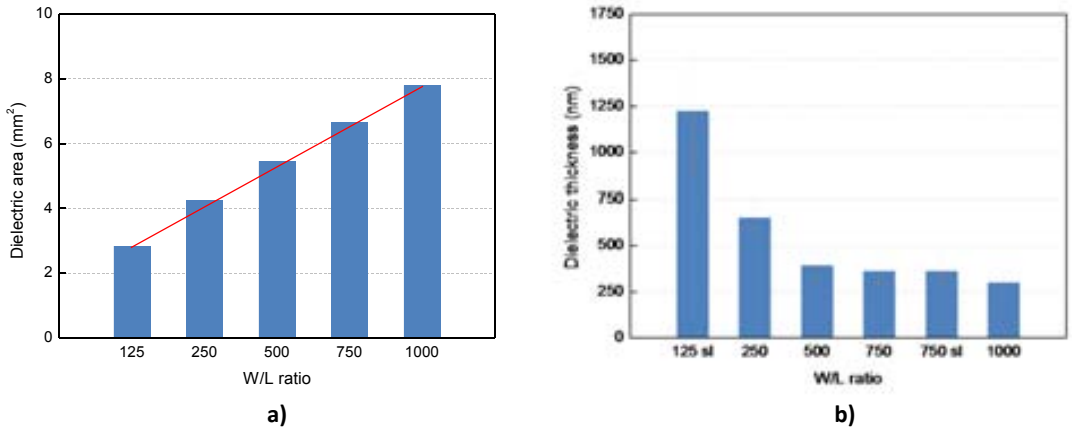


Figure 5.25. a) Dielectric area *vs* W/L ratio; and b) dielectric thickness *vs* W/L ratio.

The relation between dielectric area and thickness is a key effect that needs to be taken in account for the proper extraction of electrical parameters in OTFTs with an inkjet printed dielectric layer.

5.6.2. OTFT yield

Figure 5.26a shows the yield of the large batch of devices fabricated as a function of the W/L ratio. Transistors with higher W/L ratios have lower yield percentages. The result is clearly showing that increasing the number of fingers (higher W/L ratios) equals to higher chances of non-working devices.

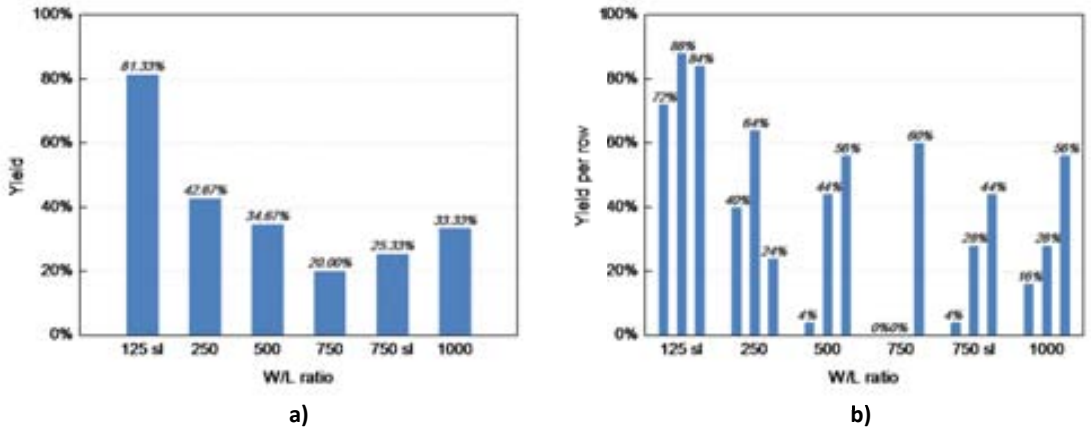


Figure 5.26. Yield versus W/L ratio: a) yield vs W/L ratio and b) yield as a function of printed row grouped by W/L ratios.

However, the yield is not only related to W/L ratio or transistor geometry. Printing effects are mostly governing the final yield. Figure 5.26b presents the yield per printed row grouped by W/L ratios. The distribution of failures per row is not uniform. Some rows show very low yields (any or just some OTFTs working) decreasing the yield of the W/L ratio row group. E.g. the W/L ratio of 750 with large-fingers has two rows without a single working OTFT and the third row with a 60% of yield closer to the average, as shown in Figure 5.27.

It is important to remember that the printing direction is from left to right row by row. The deposition of the different layers is usually done with a number of nozzles ranging from 3 to 12 depending on the materials deposited, and that periodically the printhead is purged and cleaned. That means that if some nozzles clogs, deviated drops or satellite drops appears in some moment of the printing process, this problem is not solved until the next cleaning process, affecting a complete row of OTFTs.

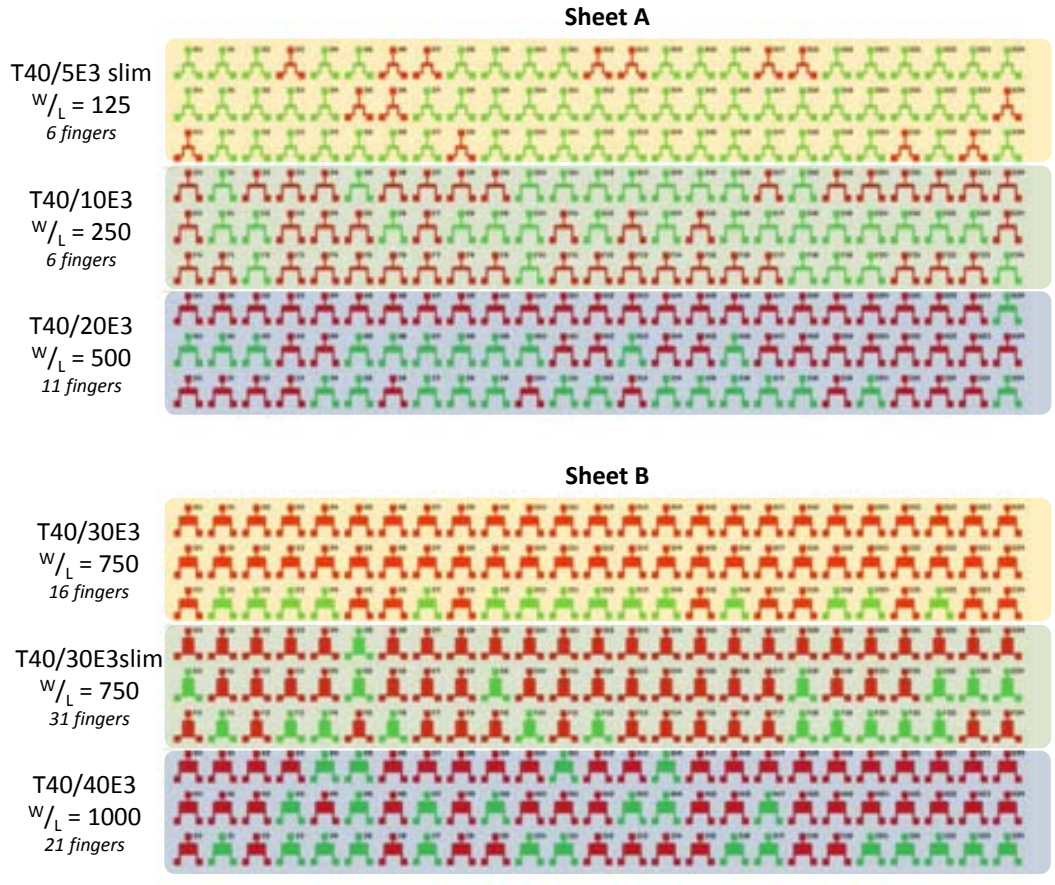


Figure 5.27. Spatial distribution of good and bad OTFTs.

Figure 5.27 shows the spatial distribution of the bad OTFTs marked on the printed layout. The layout confirms that the distribution of failures per row is not uniform. A little reduction is shown due to the increase of W/L ratio starting from a maximum yield of 88% (W/L ratio of

125 with short-fingers) to a percentage of 56% in OTFTs with a W/L ratio of 1000 and large-fingers.

From Figure 5.26 and Figure 5.27, it is clear that comparing the estimated yield with and without area dependent variability results in large differences, especially for inkjet printing technology as non-parallel deposition system. This demonstrates the importance of proper printing technology tuning and characterization prior to the implementation of complex circuits.

A summary of the origin of failures for our experiment is shown in Figure 5.28. Figure shows the percentage of devices which suffer from: (i) short-circuit between D&S, (ii) short-circuit between gate and D&S, (iii) lower resistance, (iv) open circuits, (v) unstable OTFTs (susceptible to develop shorts across the dielectric) and working OTFT (final yield).

For this particular case the principal origin for failures is open-circuits between D&S due to printing effects. Other types of failures are residual.

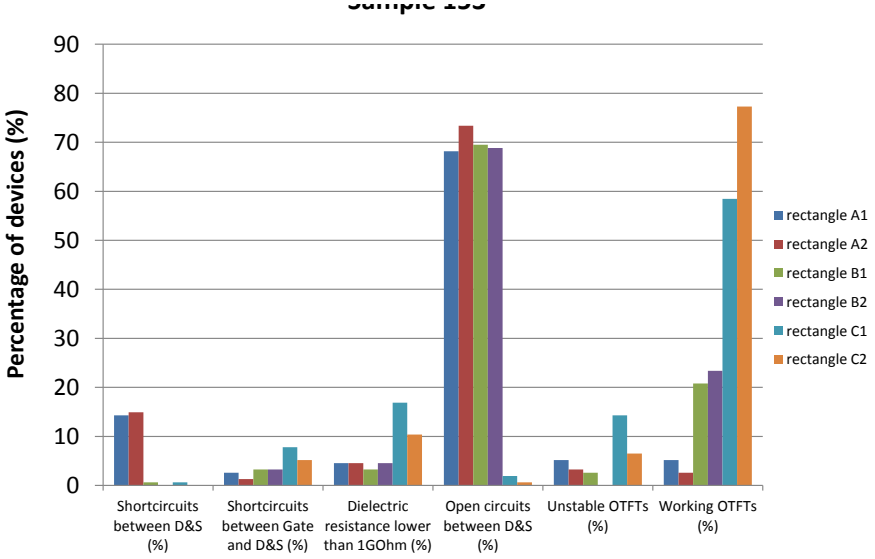


Figure 5.28. Origin of failures as a function of device geometry.

5.6.3. Variability of all-inkjet OTFTs

Considerable parameter variations have been reported for OTFTs [176][49][18]. These variations have their origin in the organic materials employed and the immature printing technology. The used materials have a direct impact on one or more parameters of the saturation current equation of OTFT as shown in the following equation.

$$I_{DS_{sat}} = \frac{1}{2}\mu C_i \left(\frac{W}{L}\right)(V_{GS} - V_T)^2 \qquad Eq.\ 5.5$$

Where L, W, C_i, μ and V_T have their usual meaning [177]. Variations in the Threshold voltage V_T affect the saturation current of the transistor quadratically, while variations in C_i, μ and device geometry influence the saturation current only linearly [175].

At first, we will demonstrate dependencies of parameter variation with respect to the geometric size of the transistor (shown as a function of W/L ratio in the following graphs).

The OTFTs fabricated were only modified on its channel width (W). Increasing the channel length (L) resulted in longer channels since the used L cannot be more reduced. Thus, channel length was fixed to the minimum value obtained having a good yield.

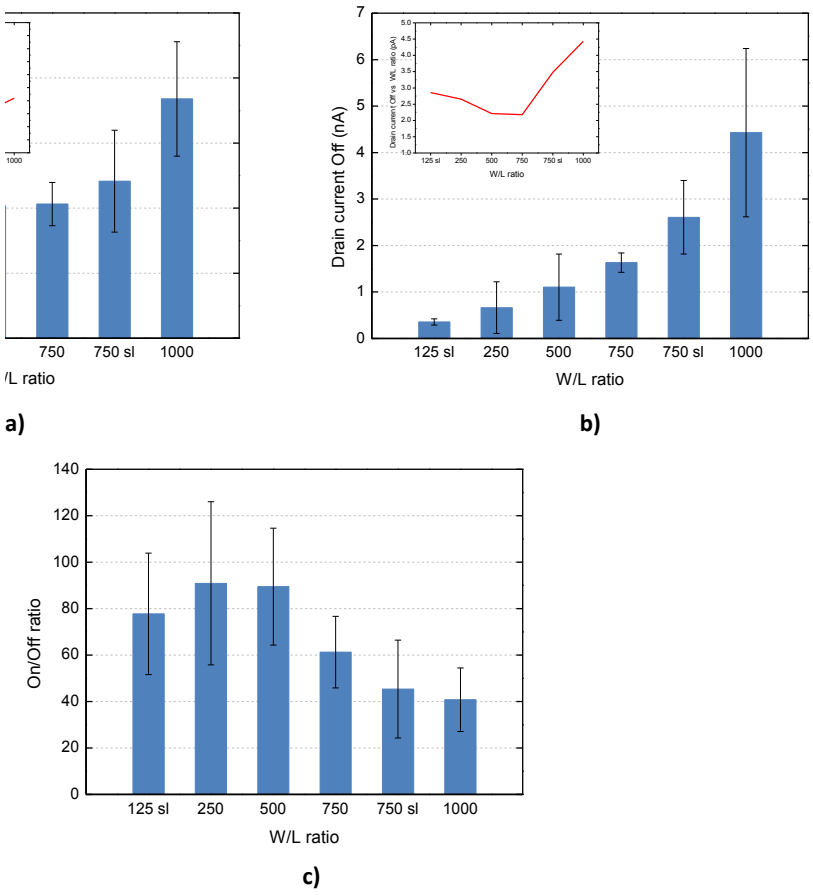


Figure 5.29. a) Drain current at On-state; b) drain current at Off-state; and c) On/Off drain current ratio as a function of W/L ratio.

Figure 5.29a and Figure 5.29b depicts the transfer characteristics operated in saturation regime: I_{ON} and I_{OFF} currents for different W/L ratios. Both increases linearly following the W/L ratio increase. Inset graphs show the normalized On- and Off-current value per W/L ratio to compare different OTFT sizes and evaluate scalability. In both cases, the normalized current can be considered close to constant coefficients resulting proportional to transistor area. Differences can arise by geometric effects. One reason is that current density extends beyond of the region of drain and source electrode overlap (lateral conduction effects),

resulting in an increase of the effective width of the device. The current density flowing outside the electrode overlap depends on the channel length (L) and on the device structure.

Figure 5.29c shows the I_{ON}/I_{OFF} ratio as a function of W/L ratio. Smaller transistors exhibit better I_{ON}/I_{OFF} ratios because I_{OFF} current is lower than in larger transistors. While in larger transistors the drain current at On-state increase, the Off-state current also increases lowering the I_{ON}/I_{OFF} ratio.

Figure 5.30a shows the decrease of the mobility proportionally to the W/L ratio since dielectric thickness decreases according to the dielectric area. Analysing the graph, it is clear that the variability of the transistor mobility is smaller for larger devices. In terms of absolute values, the smaller device (125sl) exhibits a standard deviation on mobility $\sigma(\mu) = 8.59 \cdot 10^{-5}$ cm²/V·s, while a device with a W/L ratio of 1000 has $\sigma(\mu) = 5.22 \cdot 10^{-5}$ cm²/V·s.

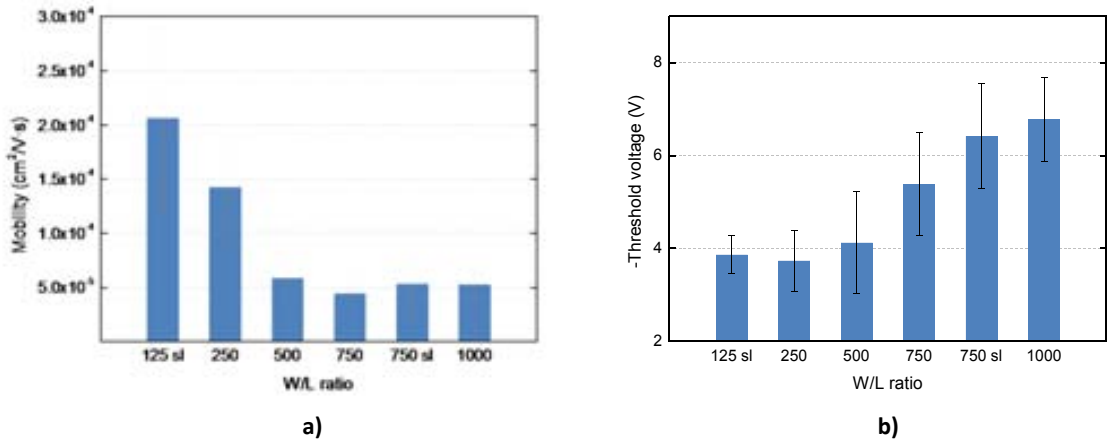


Figure 5.30. a) Mobility; and b) Threshold voltage as a function of W/L ratio.

Regarding Threshold voltage, from Figure 5.30b we can conclude that the variation on the V_T in function of the W/L ratio does not show any clear tendency in terms of absolute values.

Figure 5.31 shows the spatial distribution of the mobility and the yield of printed transistors in the two sheets composing one foil design.

From the variability point of view, we studied the variation of transistor performance proportional to the transistor area. We focused on intra-foil variations (currently named within- or intra-die WID variations), which are categorized as deviations of the transistor parameters in the same foil. However, variations between different foils (die-to-die variation) are not considered because only one fabricated foil had enough working transistors for this study. For a reliable technology in, e.g. display applications, the absolute value and the spread on On- and Off-current, V_T and mobility at large negative V_{GS} values are key parameters.

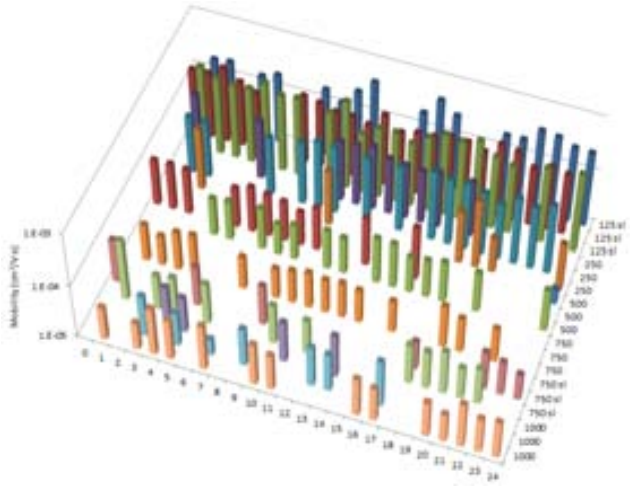


Figure 5.31. Mobility of the working transistors in OTFT foil. Note: the position in the graph corresponds to the physical position in the printed the foil.

For Si-CMOS technologies, Pelgrom et al. concluded that the variance of the Threshold voltage and the current factor between two adjacent and closely spaced devices are inversely proportional to the square root of the transistor area [178].

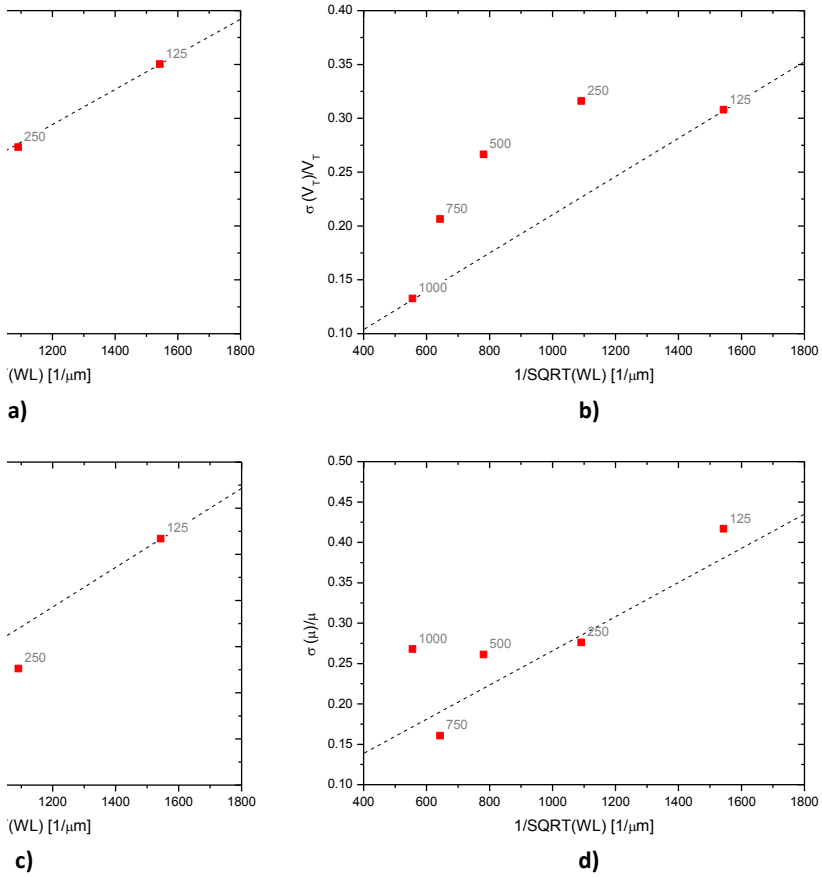


Figure 5.32. Intra-foil standard deviation of parameters of the p-type organic TFT plotted versus the inverse square root of the transistor area, measured on one sheet: a) On-state current (I_{ON}); b) Threshold voltage; c) Off-state current (I_{OFF}); and d) mobility. The dots are the obtained measurements; the dashed line is the corresponding fit. The label of the red dots shows the W/L ratio for each OTFT.

Figure 5.32a and Figure 5.32b depicts the ratio between standard deviation on I_{ON} (or V_T) and the average of I_{ON} (or V_T) versus the transistor area respectively. We can observe that the percentage of spread in I_{ON}, I_{OFF} mobility and V_T increases linearly with decreasing square root of transistor area.

The statistical analysis of the electrical characteristics of the OTFTs will be depicted in Figure 5.33.

Histograms show the spread of different electrical parameters for all the devices. The distribution is observed to be more confined for some parameters as V_T and On/Off drain current ratio. Mobility and On-current show bigger spreads. Better thickness uniformity should improve characteristics as the parameter spread is partially dependent on semiconductor thickness [176]. This should be taken into account in the next chapter when transistors will be improved using different approaches.

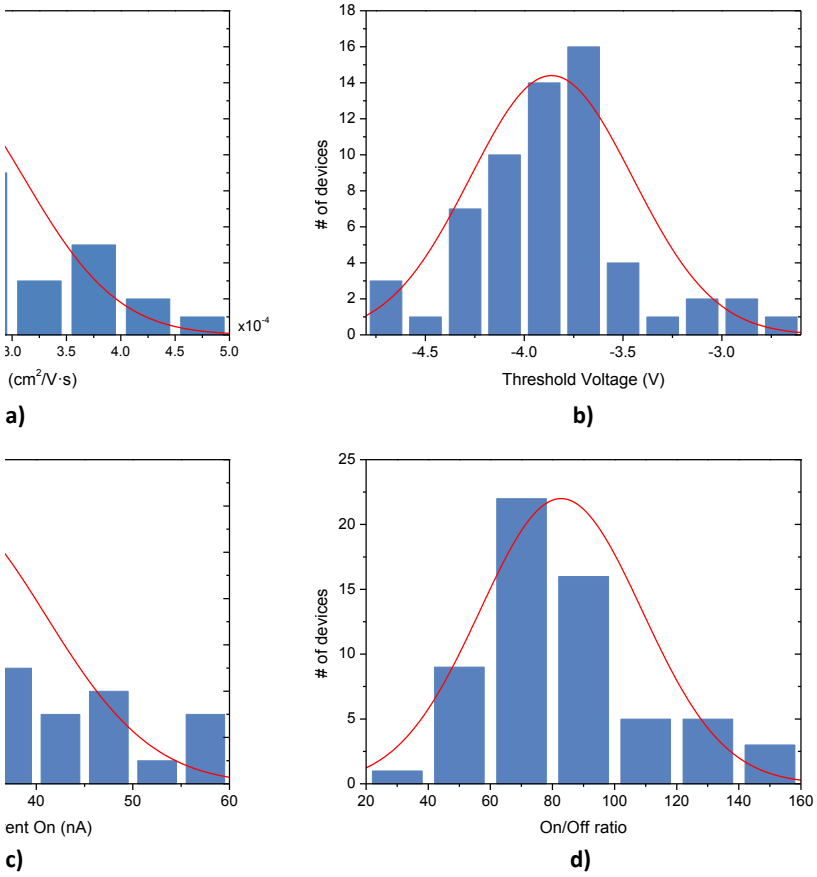


Figure 5.33. Statistical analysis of the electrical characteristics of 180 working OTFTs fabricated: a) mobility; b) Threshold voltage; c) drain current at On-state; and d) On/Off ratio.

To minimize variability, large W and L are attractive. But, this strategy does not mean that the use of very large transistors will, in practice, guarantee the ability to integrate large number of transistors, as larger transistors increases the chance of non-working circuits due

to printing effects and other type of hard faults. Furthermore, cost and power consumption are directly proportional to circuit area. Finally, large L will imply slower circuit speed.

These trade-off considerations cannot be transferred into design rules unless all above considerations were quantified [175]. Intra-foil (WID) variations of transistor parameters should be included in the design flow by means of Montecarlo simulations. Current investigations in data on parameter variation for different transistor sizes are a start for this task.

Results obtained are similar than those presented on the state-of-the-art by H. Klauk et al [179]. The obtained results suggests that Pelgrom's mismatch law derived for Si CMOS technologies is also valid for evaporated OTFTs already demonstrated by Myny et al. [175].

5.7. Summary and conclusions

Several hundreds of OTFTs were manufactured by S2S inkjet printing, all of them fully inkjet-printed. All of the devices were fully characterized obtaining yields up to 78% for a fixed design.

The all-inkjet OTFTs were fabricated on flexible PEN substrate using the dielectric c-PVP and an active semiconductor layer FS0027 with short- and large-finger geometries. These transistors are similar than both partly- and all-inkjet printed transistors published in the literature [176]. Transistors based on polycrystalline films of pentacene, set the benchmark for OTFT performance, displaying values of μ in excess of 1 $cm^2/V \cdot s$, $I_{ON}/I_{OFF} > 10^8$, and V_T near 0V [180]. The OTFTs characterized displays values of μ around $2 \cdot 10^{-4}$ $cm^2/V \cdot s$, $I_{ON}/I_{OFF} \sim 10^2$, and V_T ranging from 0 to 8V, but they are all-inkjet printed and fabricated at room conditions.

In comparison with SiO_2 reference structures, all-inkjet printed devices showed a higher On/Off current ratio, better saturation characteristics, and linear contact behaviour. However, all-inkjet printed devices on PEN showed higher mobility. Similar levels of gate leakage current were observed for the SiO_2 and PEN samples. Overall, there is a substantial reduction in device performance for OTFTs on plastic substrates when compared to OTFTs on rigid substrates. This reduction can be attributed to the higher surface roughness. Nevertheless, the experiments demonstrated the feasibility of fabricating OTFTs with organic semiconductor and dielectric materials on plastic substrates.

Our results show that the c-PVP ink formulation is not optimal. The solvent used has good properties for stable drop ejection using inkjet printing, but final electrical characteristics are not totally satisfactory.

Degradation on On/Off current ratio is caused by a residual off-current between drain and source terminals. This Off-current is due to the thickness of the active semiconductor channel. Strategies should be considered to reduce this current it an increase the OTFT On/Off current ratio is needed for correct circuit behaviour.

Concerning operational stability, we observed that the OTFTs require at least two days to start the degradation. Therefore, compared with the literature, OTFTs can be considered quite stable in air conditions although the devices suffer from gate-bias stress effects and non-linear I-V curves near the origin caused by series resistance effects due to the presence of traps.

The primary sources of the variability are variations in morphology and thickness in the deposited functional layers, which are more pronounced in inkjet printed than in photolithographic processes.

Intra-Foil (WID) variations of transistor parameters are a key to design and simulate organic full integrated circuits. In order to perform these simulations, data on parameter variation for different transistor sizes have been investigated. The obtained data suggests that Pelgrom's mismatch law derived for Si CMOS technologies is also valid for OTFTs. Larger devices exhibit less variation concerning the active area.

However, the general understanding of reliability issues in OTFTs is complex due to the high wide variety of organic semiconductors with different chemical structures and varying levels of chemical purity. Therefore the comparison of the results coming from different research groups is very difficult since they use also using different device architectures, gate dielectrics, and bias stress conditions.

6. STRATEGIES FOR THE IMPROVEMENT OF INKJET PRINTED ORGANIC THIN FILM TRANSISTORS

The present chapter reports the proposal, implementation and results of different strategies for the improvement of the OTFTs in S2S by using inkjet printing technologies. The bases for the improvements are the devices fabricated in Chapter 3 and the constraints in OTFT performance and behaviour identified in Chapter 4.

The constraints identified could be summarized as:

- Low performance. Maximum drain current is low and operating voltages are high in all-inkjet OTFTs due to the OSC material performance itself but also the dielectric layer thickness.
- Excessive Off-current and therefore reduced On/Off current ratio. The ideal On/Off current ratio is $>10^4$ which reduces the static power dissipation in a logic circuit.
- High overlap capacitance leading in low speed circuit operation.
- Low stability over time, working life less than one month. The lifetime and reliability of organic electronics are a critical concern.

Different improvement strategies will be addressed in the current chapter:

- Different encapsulation strategies to improve the lifetime and unwanted doping in BG-BC (bottom-gate bottom-contact) inkjet-printed OTFTs.
- Improvement of functional layers deposition focused by lowering the dielectric and OSC thicknesses. I_{OFF} can be reduced and cut-off frequency can be significantly enhanced when the overlap capacitances are minimized.
- Optimization of OTFTs by design. Different approaches will be studied changing design parameters, geometries and layer patterns in order to improve OTFT behaviour.

In the following sections, the different proposed approaches and their results will be analysed in detail and compared with the results obtained in the previous chapter.

6.1. OTFT Encapsulation Strategies

Since many organic semiconductors and conductive polymers are easily influenced by moisture, oxygen, and other environmental elements present in ambient conditions, the lifetime, and reliability of organic electronics are a critical concern. Improving operational stability is a key issue because the semiconductor is in the charged state and thus it is mandatory to avoid reactions with oxygen and moisture the addition of barrier layers.

For this reason, passivation and encapsulation play an important role in extending the lifetime and stability of OTFTs leading to a significant reduction in the degradation and failure of devices [181][182][183][133]. Therefore, the passivation of the OTFT is necessary to lengthen its lifetime [184].

The proper encapsulation method for OTFTs should meet the following basic criteria [133]:

- low-temperature curing to enable direct deposition on temperature-sensitive organic devices.
- intrinsically defect-free films to provide a reliable barrier against moisture and oxygen.
- minimal effect on device performance.
- low cost and good durability.

6.1.1. MMAcoMAA as barrier layer

BG-BC transistors present several advantages in terms of fabrication as already discussed in this work, but some important drawbacks as well such as the sensibility of the Off-current due to the degradation of the OSC material. In our architecture, the OSC is directly exposed to the ambient conditions: temperature, moisture and so on, and therefore the I_{OFF} will be affected due to this unwanted doping.

In this section we present a successful prevention technique against the degradation of OSC and an improvement of the I_{OFF} electrical parameter of the OTFT. A coating layer was deposited on top of the OSC layer in order to reduce all those drawbacks. The OTFTs used have the same structures fabricated in Chapter 4, but with a dielectric thickness of 1µm showing a reduced performance compared with the previously characterized. This difference is not critical because the objective of the experiments was to characterize the stability of the OSC layer with and without a coating layer. The material used for coating is MMAcoMAA dielectric and it was deposited by inkjet printing as shown in Figure 6.1.

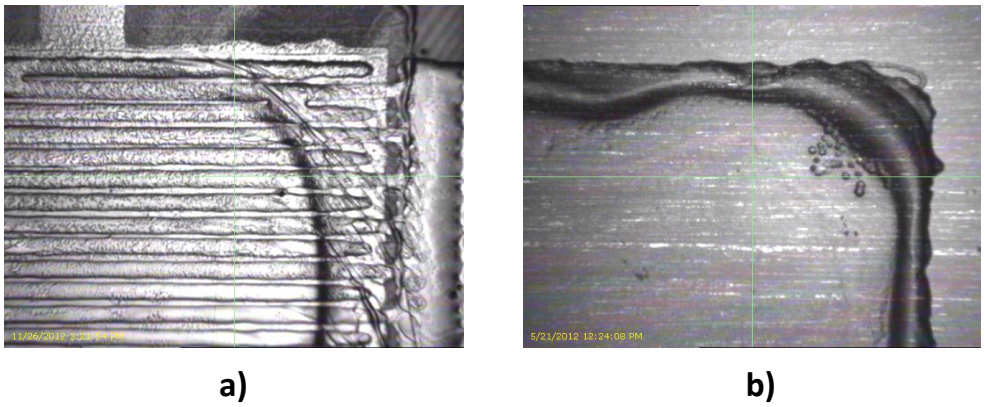


Figure 6.1. Image of the MMAcoMAA layer deposited by inkjet printing: a) on top of the OSC layer and b) on top of the PEN substrate.

Microchem MMA(8.5)MAA organic copolymer solution was used as barrier layer. This material was selected after the study of different coatings, due to the fact that, although it has never been used as dielectric in Organic Electronics technology, this family of compounds forms the basis of many positive resists having high resolution and good adhesion to metallic and semiconducting supports, as well as good resistance to solvents and reagents. However, an additional optimization was needed to achieve a proper MMAcoMAA layer thickness to assure device protection.

Electrical characterization in air and at room temperature was performed to assess the effect of depositing the coating layer on the mobility and I_{OFF} parameters after degradation. OTFTs were exposed several days at room conditions.

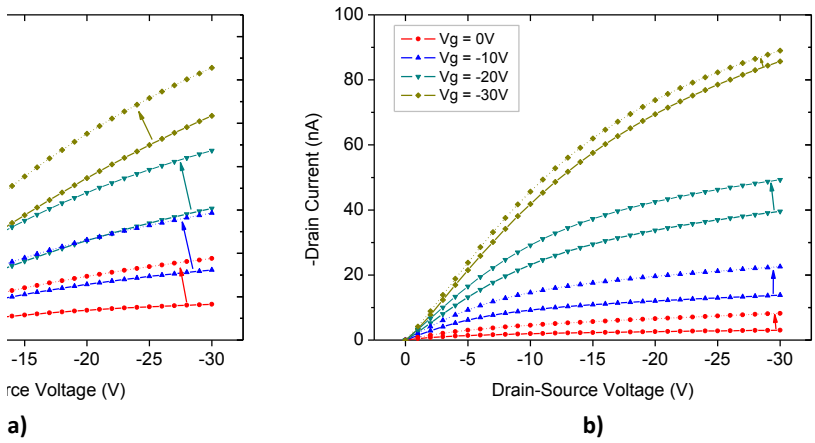


Figure 6.2. Output characteristics: a) without coating layer, and b) with coating layer (solid line: fresh, dashed line: after degradation exposure).

Figure 6.2a show the output characteristic of the OTFT without coating layer before (solid line) and after (dashed line) exposition to degradation respectively. A significant increase of

the I_{OFF} is observed, up to three times more, for OTFT without coating layer after degradation. Figure 6.2b shows the output characteristics for the OTFT protected by the MMAcoMAA coating layer before and after the degradation respectively. Interesting results were obtained for OTFT with coating layer in terms of I_{OFF}. The I_{OFF} current almost does not increase under degradation conditions. Moreover, the mobility of OSC with coating layer is not altered, just a slight change from $14 \cdot 10^{-6}$ to $32 \cdot 10^{-6}$ $cm^2/V \cdot s$ after the deposition of the coating layer.

Table 6.1 shows the I_{OFF} for OTFT devices with and without coating layer before and after degradation conditions.

Table 6.1. I_{OFF} (V_G=0V V_D=-30V)

	Fresh devices	**After degradation**
OTFT without coating layer	16.4 nA	37.6 nA
OTFT with coating layer	3 nA	8.2 nA

A reduction of I_{OFF} current is achieved thanks to the coating layer allowing an increase of I_{ON}/I_{OFF} current ratio, as shown in Table 6.2. However, the difference between I_{ON}/I_{OFF} ratio for devices without coating layer under degradation and fresh is the same as OTFT with coating layer. This means that the I_{OFF} current is reduced by the coating layer, but the degradation affects indistinctly the I_{ON}/I_{OFF} ratio.

Table 6.2. I_{ON}/I_{OFF} ratio

	Fresh devices	**After degradation**
OTFT without coating layer	6.29	3.33
OTFT with coating layer	28.37	10.83

For extracting the electrical property of the OSCs, the resistance between the S/D terminals was measured, followed by the resistance measurement along with the MMAcoMAA coating layer printed on top of it. The resistance between silver source/drain electrodes of the non-coated OTFT was found to be 270 ± 53 Mohm (two probe measurement). The resistance measured after depositing the MMAcoMAA coating layer on top of the OSC was found to be 392 ± 110 Mohm. It can be seen that the resistance values between the source/drain electrodes increases when depositing the MMAcoMAA coating layer on top. The increase of the resistance is due to the MMAcoMAA deposition on the OSC bulk, clearly affecting the I_{OFF} current since it is caused by the bulk resistance parallel to the OTFT channel.

However, the increase in mobility by ˜230% and the I_{ON}/I_{OFF} ratio increase up to ˜440% of the original value observed after the encapsulation step, suggests undesirable interaction between the photoresist and the organic semiconductor film.

6.1.2. SU8 as barrier layer

Microchem SU8 EPR-127 (specially designed for jetting in piezo-nozzle printers) was also used as barrier layer. The resist cross-links with UV curing exposure at 365nm wavelength and heat to provide a material for permanent epoxy structures. EPR-127 is currently in its development phase with customization available.

This material was chosen for its good resistance to solvents and reagents. The ink used is an experimental product optimized by Microchem to be used in inkjet printing. To avoid damaging the OSC film the crosslinking by UV light was skipped.

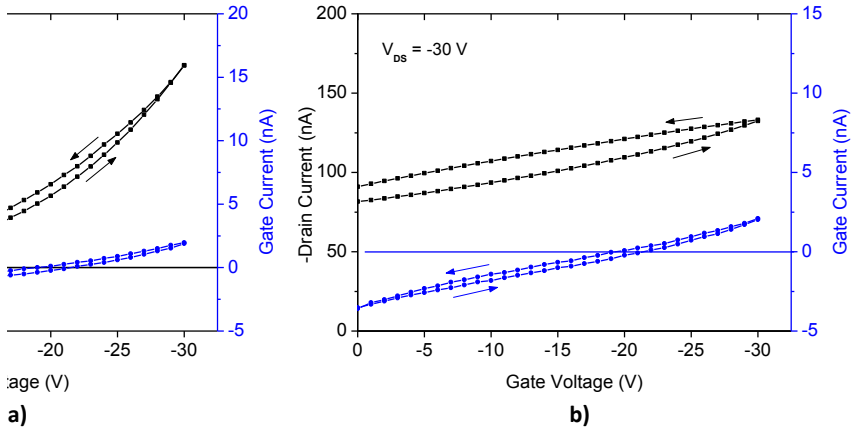


Figure 6.3. Transfer characteristic and gate current: a) without SU8 coating layer, and b) with SU8 coating layer.

The transfer characteristics for the OTFT protected by the SU8 coating layer before and after the coating are shown in Figure 6.3a and Figure 6.3b respectively. Gate current does not change after the deposition of SU8 coating, but there is a significant change in the transistor transfer characteristics. As shown in Figure 6.3b, the OSC is doped by the SU8 photoresist resulting in a high increase of I_{OFF} and I_{ON} currents and the loss of the transistor behavior.

6.2. Improvement of functional layers deposition

In previous chapters the improvement of the deposition of the source, drain and gate contacts was studied in order to assure a high fabrication yield through the deposition of homogeneous and reliable source/drain fingers without shortcuts and with a minimal channel length (L) to reach high On-currents on the fabricated devices.

On this section, the deposition of dielectric and OSC material will be improved through a better control of its thickness exclusively done by printing means.

6.2.1. Dielectric thickness reduction

In order to make this experiment, a new foil was designed formed by identical small transistors (T40/5E3sl size) with a W/L ratio of 125 and with increasing dielectric sizes. The design is shown in Annex C.12 and was focused in the study of the effect of the dielectric thickness in the electrical characteristics of the OTFT.

In the Chapter 3 it was already demonstrated that one layer of c-PVP dielectric with a drop spacing of 20 µm was the best choice to increase layer isolation and device yield. The same chapter also demonstrates that the modification of the dielectric area had a direct influence on dielectric thickness without changing the printing drop space or the c-PVP solution composition. This is an indirect method suitable for our purposes.

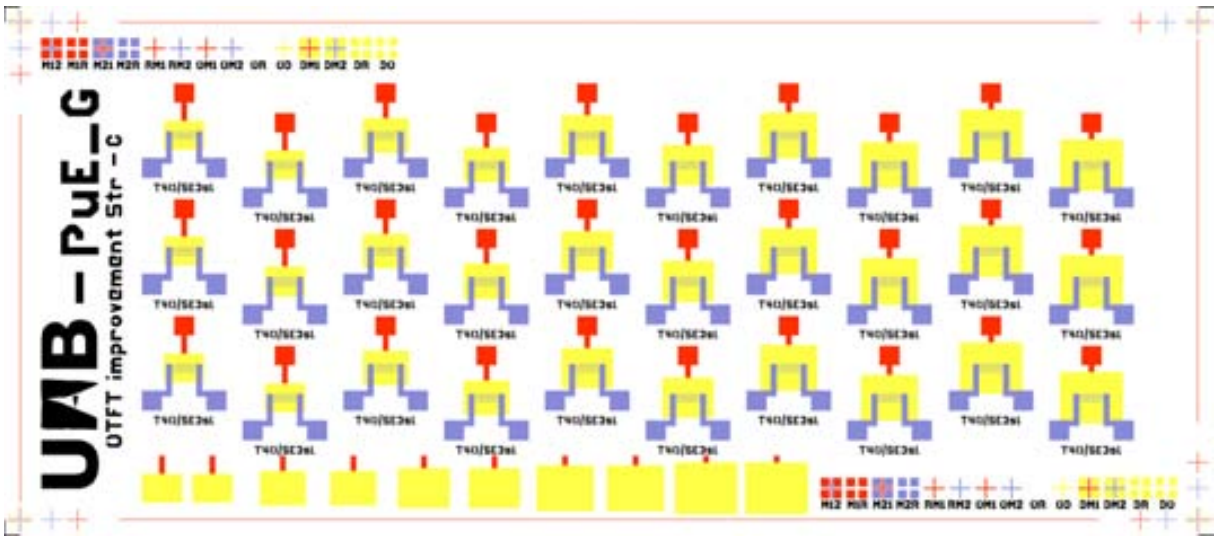


Figure 6.4. Layout of the foil designed to study the effect of the dielectric thickness on the electrical characteristics of OTFTs.

Groups of six transistors were fabricated increasing dielectric size in 280 µm on each direction compared with the previous ones. The dielectric areas and thickness are shown in Table 6.3 and covers a sufficient range to study the effect of the dielectric thickness.

Table 6.3. Dielectric pattern sizes, areas and thicknesses obtained.

Dielectric area reference	Width [µm]	Height [µm]	Area [mm²]	Area increase	Thickness [nm]
A	2000	1420	2.84		295
B	2280	1700	3.88	+135%	315
C	2560	1980	5.07	+180%	322
D	2840	2260	6.42	+225%	330
E	3120	2540	7.93	+280%	345

The fabrication followed the recipe of transistors previously developed in previous chapters, depositing the dielectric layer with a drop spacing of 20 µm without any additional pre- or post-treatment.

Figure 6.5 depicts the gate-to-S/D capacitance and layer thickness for the different dielectric pattern sizes deposited. As expected, increasing dielectric area results in a layer thickness increase thus reducing parallel plate capacitance and therefore the transistor gain.

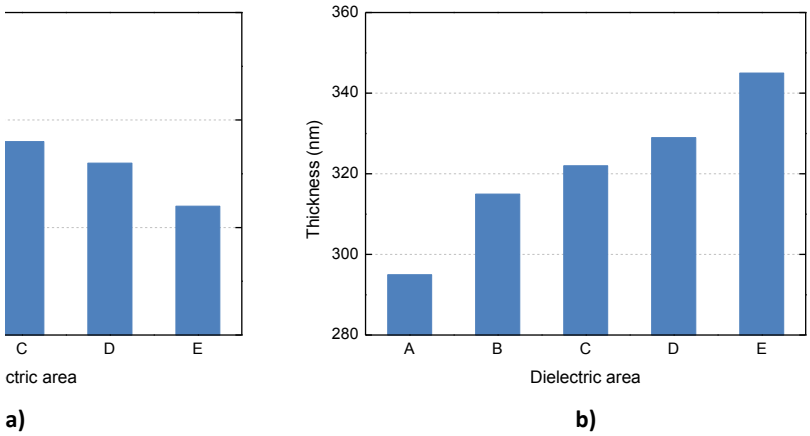


Figure 6.5. a) Gate-to-S/D capacitance, and b) dielectric layer thickness for the different dielectric pattern sizes deposited.

This is an important result in terms of the compromise required between a small dielectric area (reduced thickness) and design rules requirements to assure a high device yield.

Regarding yield, any significant correlation between yield and dielectric thickness is observed for this range of thicknesses. The yield is not modified compared with the results obtained in previous chapters.

Figure 6.6 shows different electrical parameters of OTFTs for the different dielectric pattern sizes deposited.

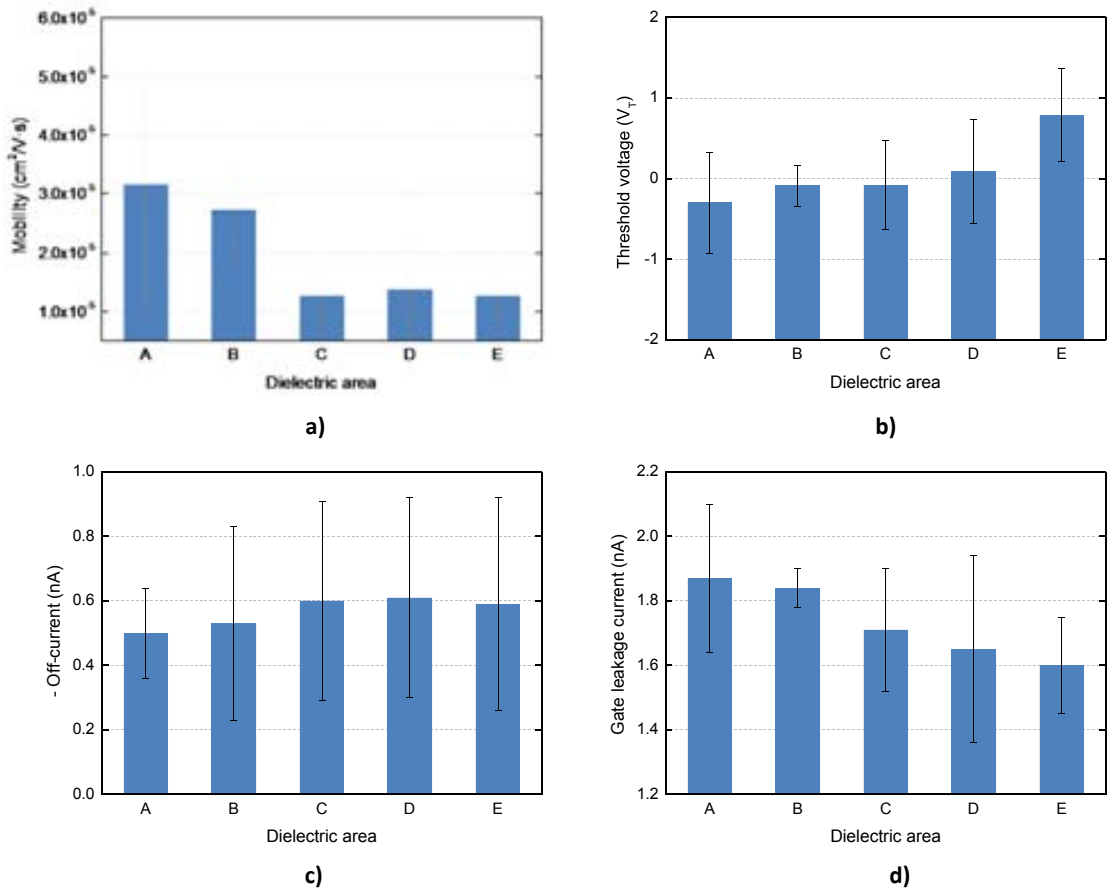


Figure 6.6. Electrical parameters of OTFTs for the different dielectric pattern sizes deposited: a) mobility; b) Threshold voltage (V_T); and c) Off-current; and d) gate leakage current.

It was expected that a decrease in dielectric thickness would result in an increase in gain and a reduction of the Threshold voltage (V_T). Figure 6.6a and Figure 6.6b shows this effect measured in the transistors fabricated in this work.

Figure 6.6d shows an obvious result because the gate leakage current decreases when the dielectric thickness increase. But Figure 6.6c shows an interesting effect regarding the Off-current that decreases when dielectric thickness is reduced. But as the currents measured are in lower than 1 nA the data variability can distort the veracity or accuracy.

Summarizing, we can affirm that the reduction of the dielectric thickness improves the electrical characteristics of the OTFTs. An interesting approach has been demonstrated on this section: a fine control of the dielectric thickness can be performed through the control of the dielectric pattern area without any loss of device yield.

6.2.2. Organic Semiconductor layer thickness reduction

The objective of this experiment is the study of the electrical parameters of the OTFTs and concretely of the I_{OFF} parameter as a function of the OSC layer thickness.

In order to perform this experiment, a previously designed foil formed by different OTFT sizes and with W/L ratios ranging from 125 to 1000 was used. The design is shown in Annex C.10 and it was printed several times using different drop spacing (25, 30 and 35 µm) for the deposition of the OSC layer. The increase of the drop space will result in a reduction of the OSC layer thickness. For a drop spacing of 25 µm a thickness of 580 nm was measured. A thickness of 480 and 400 nm were obtained for drop spacing of 30 and 35 µm, respectively.

The number of working transistors for each drop space used is shown in Table 6.4. 34 working OTFTs from the 180 fabricated were obtained with an average yield of a 20%. This poor yield is mainly due to printing effects occurred in this experiment.

Table 6.4. Number of working OTFT with different drop spacings (DS) used.

OTFT Reference	W/L ratio	DS 25 µm	DS 30 µm	DS 35 µm
T40/5E3sl	125	2	3	1
T40/10E3	250	2	3	2
T40/20E3	500	2	4	2
T40/30E3	750	1	4	1
T40/40E3	1000	2	4	2

Figure 6.7 shows some of the electrical parameters extracted and their variation as a function of the OSC drop space used. Figure 6.7a, Figure 6.7b and Figure 6.7c shows the reduction of the OSC layer thickness (after DS increase) resulting in a reduction of the I_{ON} and I_{OFF}. The values of I_{ON} and I_{OFF} in the graphs are normalized with the W/L ratio to independent values from OTFT sizes. Because I_{OFF} is bigger than I_{OFF} reduction, the I_{ON}/I_{OFF} ratio increases.

The reduction of I_{OFF} confirms the hypothesis that part of the off-current created is flowing through the bulk as the electric field created by the gate is not able to completely close the OSC channel because of the high thickness of the OSC layer. An additional work should be done to reduce more the OSC thickness to achieve lower I_{OFF} values thus improving I_{ON}/I_{OFF} ratio through the modification of the OSC solution formulation. An additional increase of the drop spacing used on the OSC layer deposition results in a discontinued surface as drop space is too large.

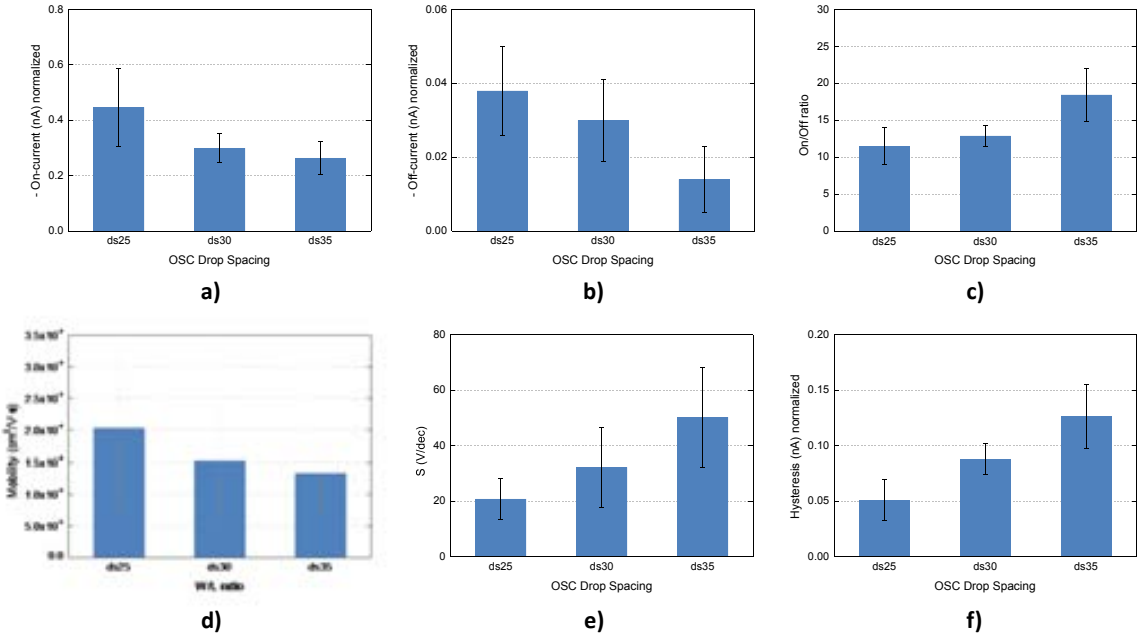


Figure 6.7. Electrical parameters of OTFTs for the different OSC layer thicknesses obtained for different drop spaces used during printing: a) normalized On-current; b) normalized Off-current; c) On/Off current ratio; d) mobility; e) subthreshold slope (S); and f) normalized hysteresis.

Among the rest of electrical parameters characterized, we can observe that the V_T remains constant (not shown in Figure) but the mobility (Figure 6.7d) decreases with the reduction of the OSC layer thickness. The subthreshold slope (Figure 6.7e) increases and the hysteresis in saturation regime also increases showing that more traps are present in the dielectric-OSC interface. The reasons for those changes are unclear and could be explained by printing effects instead of OSC thickness reasons. Each foil with a different OSC drop spacing is a different batch and slight changes can appear between fabrication batches.

6.3. Optimization of OTFTs by design

The goal of this experiment was the study of the effect of OTFT device topologies and geometries different than the ones used in chapter 4. Several approaches were studied changing design parameters, orientations and layer patterns in order to study the effect of these parameters on final transistor behaviour.

Mainly, four different strategies were studied in order to improve OTFTs by:

6. Changing finger width and length (wider or narrower transistor geometries).
7. Reducing the gate overlap area.
8. Stacking source and drain electrodes (vertical transistors).
9. Using a second gate to control OTFT behaviour (dual gate transistors).

A new OTFT foil was designed and fabricated with different topologies and two different W/L ratios: 250 (columns from 1 to 6) and 1000 (columns from 7 to 10) although only W/L ratio of 250 was used to evaluate results. The layout is shown in Annex C.10.

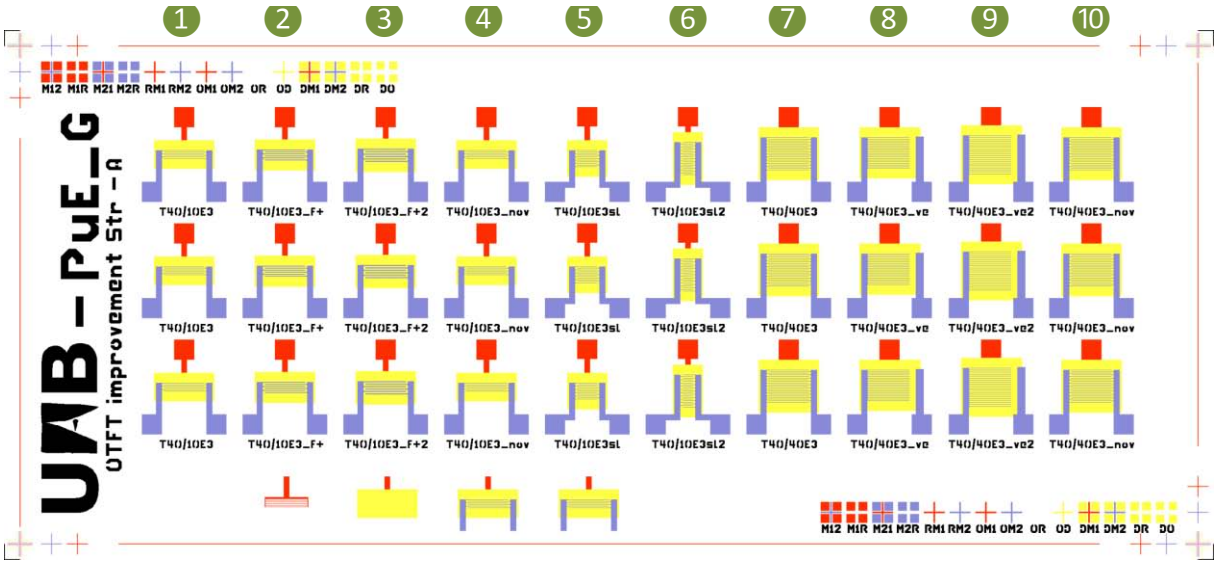


Figure 6.8. New foil with different OTFT topologies changing design parameters, orientations and layer patterns.

In the following sections the characterization results for these transistors will be reviewed organized by categories.

An OTFT numbered T40/10E3 (column ❶) was used as a reference design to compare with the others proposed. Figure 6.9a shows the layout of the reference OTFT with a W/L ratio of 250 and 6 large fingers of 2000 µm length each. Figure 6.9c, Figure 6.9d, Figure 6.9e and Figure 6.9f shows the extracted layers with their physical dimensions.

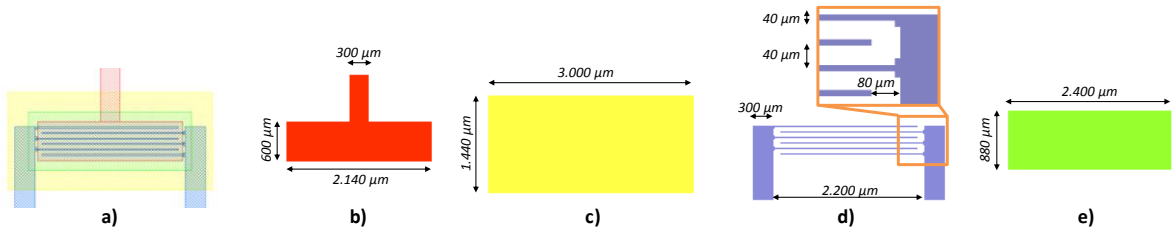


Figure 6.9. Layout of the *reference* OTFT with a W/L ratio of 250: a) stacked layout; b) metal_1; c) dielectric; d) metal_2; and e) OSC.

This is the same layout design fabricated and characterized in Chapter 4 and Chapter 5.

6.3.1. Improving OTFTs by changing finger width

This approach changed the finger width of the transistors keeping constant finger length.

The fabricated transistors (columns ❷ and ❸ of Annex C.10 design) were compared with the reference transistor (column ❶). Both transistors have a W/L ratio of 250 and similar areas of dielectric and OSC. Difference resides in finger width. Reference OTFT has a theoretical finger width of 40 µm using large fingers (2000 µm). *T40/10E3_f+* have a finger width of 2 pixels using 20 µm drop spacing with a theoretical width of 60 µm. *T40/10E3_f+2* have a finger width of 3 pixels using 20 µm drop spacing with a theoretical width of 80 µm. *T40/10E3_f+2* finger pattern uses a compensated structure to reduce the amount of ink to avoid shortcuts between source and drain electrodes by ink coalescence. Table 6.5 shows the specifications of the fabricated transistors for the current experiment.

Table 6.5. OTFT topologies and W/L ratios fabricated in fx119 design for the current experiment.

OTFT Reference	finger length [µm]	finger width [µm]	L [µm]	W [µm]	W/L ratio
T40/10E3	2000	40 (1px)	40	10E3	250
T40/10E3_f+	2000	60 (2px)	40	10E3	250
T40/10E3_f+2	2000	80 (3px compensated)	40	10E3	250

Figure 6.10 shows the finger layout of the OTFTs proposed for this experiment. To adapt the design to the biggest area occupied by the finger electrodes, the gate, dielectric and OSC layers increased their vertical dimensions on 120 µm for the *T40/10E3_f+* design and 240 µm for the *T40/10E3_f+2* design compared with the dimensions shown in Figure 6.9.

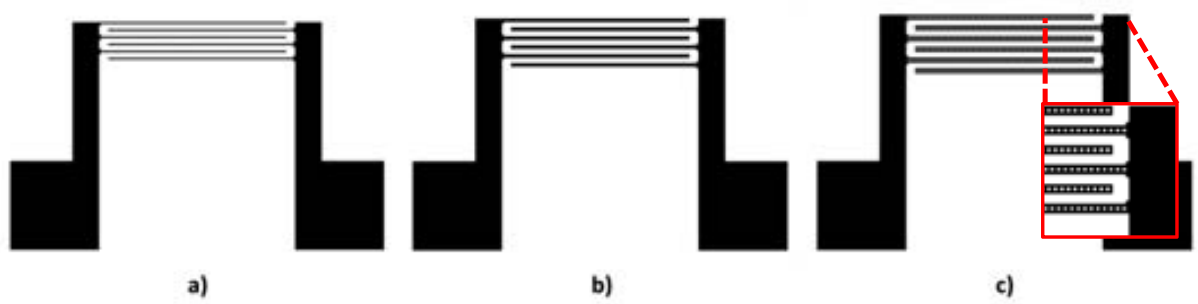


Figure 6.10. Finger layout (metal_2 layer) for: a) *T40/10E3*; b) *T40/10E3_f+*; and c) *T40/10E3_f+2* with compensated fingers.

The channel length (L) was designed to be 40 µm. But as previously showed, due to ink coalescence and surface tension of the dielectric, the final channel length had an average of 19.1 ± 3.4 µm for the *T40/10E3* design as already measured. For the *T40/10E3_f+* (hereinafter named as *f+*) and *T40/10E3_f+2* (hereinafter named as *f+2*) designs, the measured average channel was 30.2 ± 4.53 µm and 43.9 ± 5.5 µm respectively, as shown in Figure 5.12b for *f+*. Dielectric thickness is similar in the three designs with an average of 525.5 ± 21.4 nm. These values will be used to extract the OTFT electrical parameters.

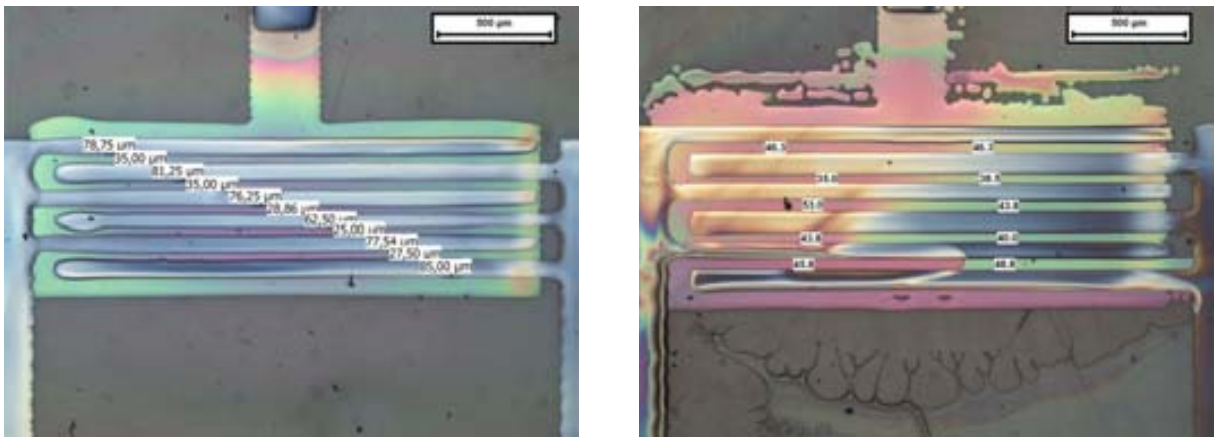


Figure 6.11. Drain and source interdigitated electrodes of the printed OTFT: a) design marked as *f+*; and b) design marked as *f+2*. The measurements of L were performed by optical microscope.

It can be observed that by increasing the finger width the channel length (L) also increases. This is caused because wider fingers are more homogeneous, as shown in Figure 5.12b because larger patterns (in our case S/D fingers) control better ink coalescence than smaller ones.

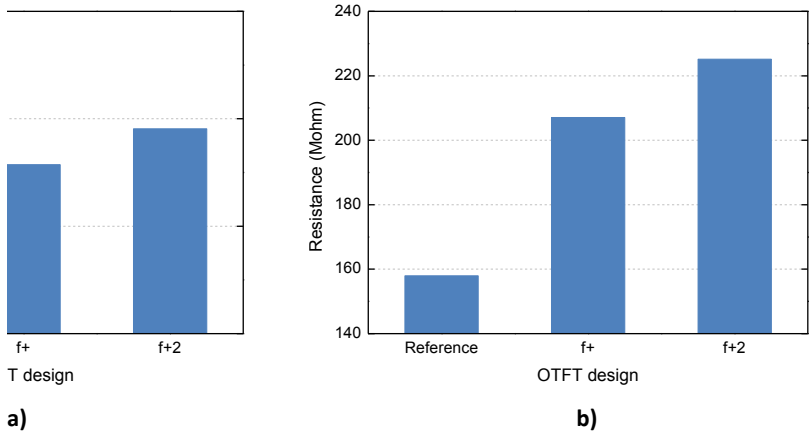


Figure 6.12. Gate to source/drain: a) Capacitance; and b) resistance.

Figure 6.12 shows the vertical capacitance (parallel-plate) and resistance measured between gate and S/D electrodes. As expected, wider S/D fingers increase the overlapping area thus increasing the gate-to-S/D capacitance and resistance.

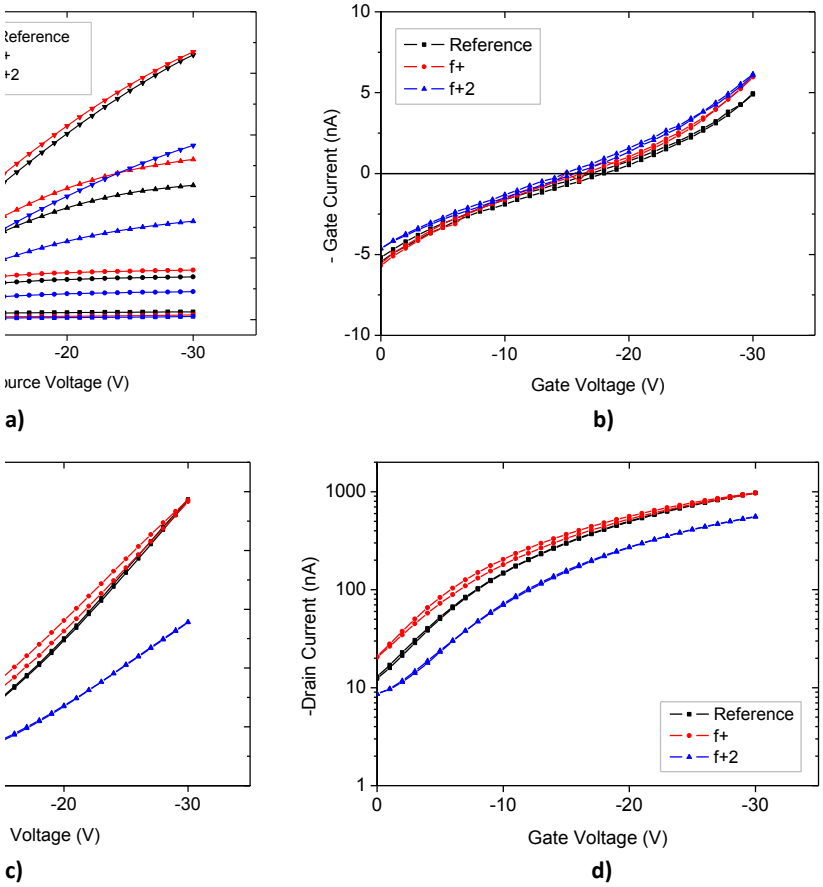


Figure 6.13. Drain-source current and gate current for Transfer and Output curves for different OTFT topologies with V_{GS} ranging from 0 to -30V: a) Output curves; b) Leakage current with V_{DS} = -30V; c) Transfer curve in saturation region with V_{DS} = -30V; and d) Transfer semilog curve with V_{DS} = -30V.

The comparative output, transfer curves and extracted electrical parameters are shown in Figure 6.13 and Figure 6.14. *Reference* and *f+* designs show similar behaviours as shown in Figure 6.13a. Both reach high On-current levels (as shown in Figure 6.14a compared with *f+2* design, although it seems that *f+* design suffers less of contact resistance compared with *reference* as shown in Figure 5.13a.

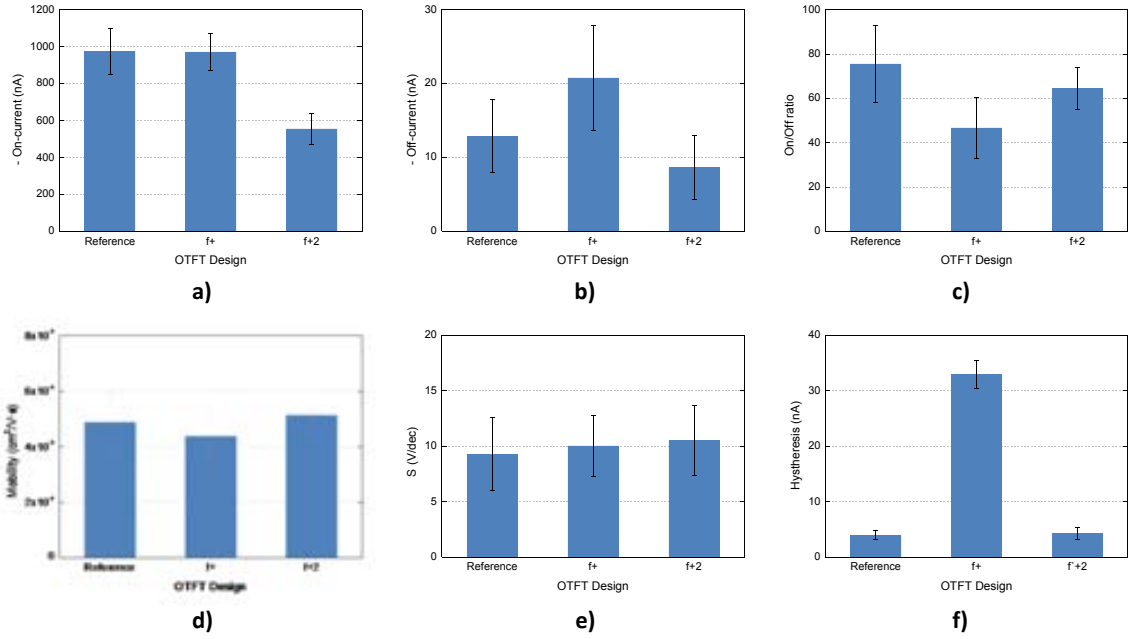


Figure 6.14. Electrical parameters extracted for the different transistor geometries proposed: a) On-current; b) Off-current; c) On/Off current ratio; d) mobility; e) Subthreshold slope (S); and f) hysteresis.

Gate current (I_G) are quite similar in all designs. *Reference* design is maybe slightly better as shown in Figure 6.13b because narrower fingers reduce the overlapping area between S/D and gate electrodes thus reducing the quantity of conductive paths.

Figure 5.13c and Figure 6.13d shows the transfer curves in linear and semilog scale. Based on these results it can be observed a large hysteresis for the *f+2* design as show in Figure 6.14f. Also, a large Off-current can be observed for the *f+2* design as show in Figure 6.13b and Figure 6.14b. The *f+* design shows the smaller Off-current level compared with *reference* and *f+2* designs.

The reason of both results is unclear but it cannot be attributed to printing reasons because the transistors used for this analysis were fabricated and characterized at same time and belong to the same fabrication batch. It is important to note that the different designs were distributed in the foil in order to reduce the consideration of temporary printing effects.

Finally, Figure 6.14d and e shows the mobility and the subthreshold slope for the topologies studies. Only slight variations can be observed maybe due to intrinsic data variation.

So, any significant advantage can be seen in using devices with wider fingers instead of the minimal ones (one-pixel fingers). Best results are obtained with the *Reference* design. This is an important result in the sense that justifies the use of minimum width fingers that also allow increasing the transistor density through the fabrication of reduced size OTFTs.

6.3.2. Improving OTFT by changing finger length

This approach changed the finger length of the transistors keeping constant finger width (one-pixel width). This approach was previously partly analysed in Chapter 5 when best characterized transistors were introduced.

The new transistors fabricated (columns ❺ and ❻ of Annex C.10 design) were compared with the reference transistor (column ❶ reference *T40/10E3*).

Table 6.6. OTFT topologies and W/L ratios fabricated in the design for the current experiment.

OTFT reference	L [µm]	finger length [µm]	# of fingers	W [µm]	W/L ratio
T40/10E3	40	2000	6	10E3	250
T40/10E3sl	40	1000	11	10E3	250
T40/10E3sl2	40	500	21	10E3	250

All transistors have a W/L ratio of 250 and similar areas of dielectric and OSC, as shown in Table 6.6. Main difference resides in transistor orientation. First one has a horizontal topology having large fingers (2000 µm), a second one having a more vertical topology with shorter fingers (1000 µm) and named *slim* (*sl* in the OTFT reference), and a third one having the shortest fingers (500 µm) and named *slim2* (*sl2* in the OTFT reference).

To adapt the design to the biggest area occupied by the finger electrodes, the gate, dielectric and OSC layers were modified through their vertical and horizontal dimensions compared with the dimensions shown in Figure 6.9. i.e. the dielectric areas changes from 3000x1420 µm (4.26 mm^2) for the *reference* design, to 2000x1820 µm (3.64 mm^2) for the *sl* design and 1500x2620 µm (3.93 mm^2) for the *sl2* design. OSC layer follows similar changes.

Figure 6.15 shows the simplified layout of the three different device geometries used in the current experiment. OSC layer is omitted for clarity of the schema.

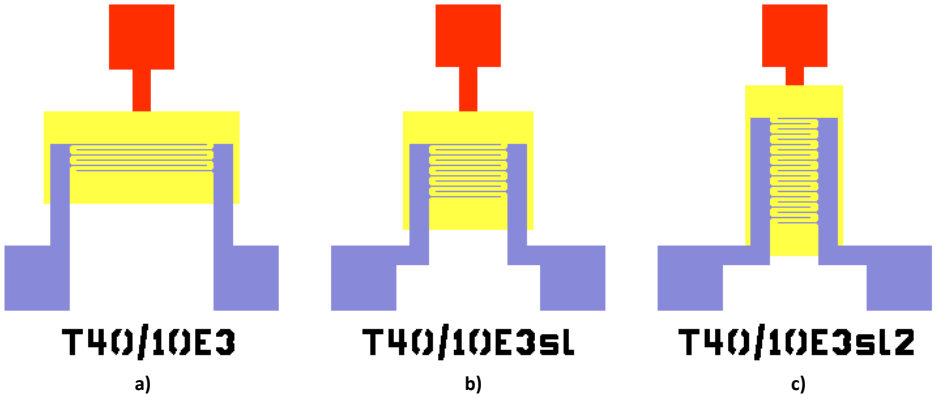


Figure 6.15. a) *Reference* design with finger length of 2000 µm; b) *sl* design with finger length of 1000 µm; and c) *sl2* design with finger length of 500 µm.

Again, the channel length (L) was designed to be 40 µm. But as previously demonstrated, due to ink coalescence the final dimensions for the *reference* design had an average of 19.1 ± 3.4 µm with a dielectric thickness of 525.5 ± 21.4 nm. For the *T40/10E3sl* (hereinafter named as *sl*) and *T40/10E3sl2* (hereinafter named as *sl2*) designs, the measured channel length was 29 ± 3 µm with a dielectric thickness of 601 ± 34.9 nm and 22.6 ± 3.2 µm with a dielectric thickness of 527 ± 24.9 nm respectively. Figure 6.16b shows the *sl* design and channel and finger measurements. The *sl2* design was measured in Section 5.3.1.2. These values will be used as channel length to extract OTFT electrical parameters.

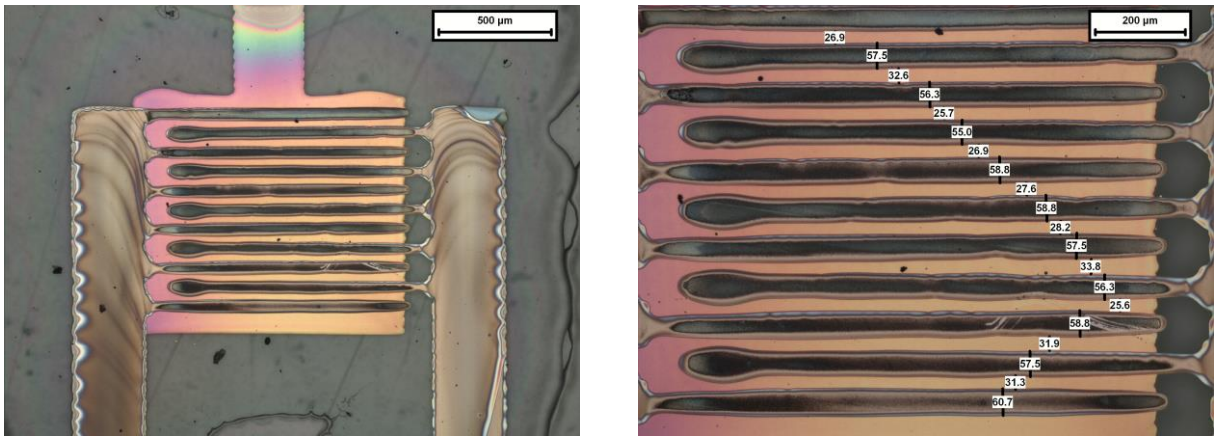


Figure 6.16. a) Picture of a slim OTFT (marked as *sl*); and b) drain and source interdigitated electrodes of the printed OTFT. The measurements of L were performed by optical microscope.

Figure 6.17 shows the vertical capacitance and resistance measured between gate and S/D electrodes. All of them show similar capacitances with a slight reduction for the slim transistors. This is due to the fact that the number of fingers does not increase linearly with the linear reduction of the finger length as shown in Table 6.6.

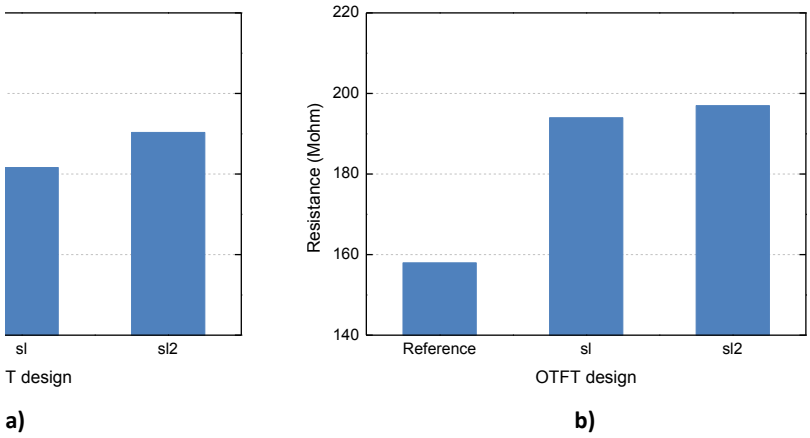


Figure 6.17. Gate to source/drain: a) Capacitance and b) Resistance.

Thus, the overlapping area slightly reduces and consequently the vertical capacitance between gate and S/D electrodes. The reasons for the parallel resistance increase are unclear although it increases with the same proportion of the overlapping area.

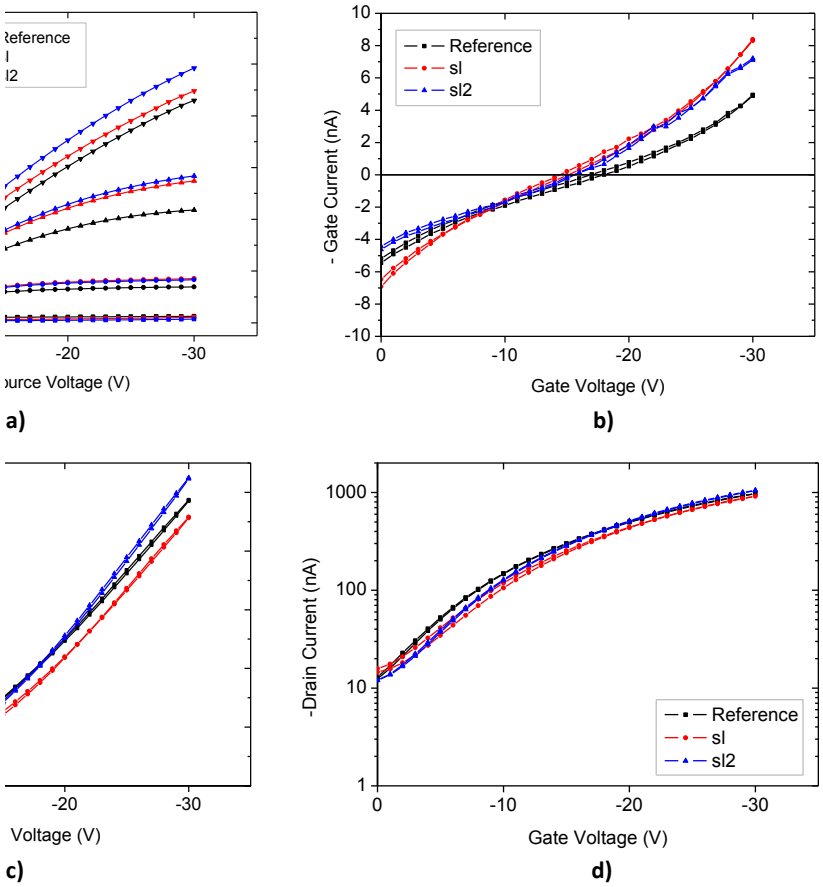


Figure 6.18. Drain-source current and gate current for Transfer and Output curves for different OTFT topologies with V_{GS} ranging from 0 to -30V. a) Output curves, b) Leakage current with V_{DS} = -30V, c) Transfer curve in saturation region with V_{DS} = -30V; and d) Transfer semilog curve with V_{DS} = -30V.

Comparative output, transfer curves and extracted electrical parameters are shown in Figure 6.17 and Figure 6.18.

From the graphs we can observe that narrower transistors (*sl2*) show better behavior than the wider one (*reference*). All of them reach high On-current levels, as shown in Figure 6.18a and Figure 6.18c, but *sl2* design shows the best performance. Figure 6.19d shows an important increase (up to ˜146%) in mobility for narrower transistors compared with *reference*.

Figure 6.18c and d shows the transfer curves in linear and semilog scale. Based on these results we can observe a larger hysteresis for the *sl* design as shown in Figure 6.19f although the increase is not significant. Also, similar Off-currents can be observed for all the designs as show in Figure 6.18d and Figure 6.19b, although narrower transistors shows a slightly smaller Off-current level compared with *reference*. This causes an increase in the I_{ON}/I_{OFF} ratio for the *sl2* design as shown in Figure 6.19f.

Gate current (I_G) is slightly bigger in slim designs. The reason is unclear and could be related to thinner layers or inhomogeneous morphology in the active area due to stretch. This should be studied more deeply although it is not an easy task to evaluate the uniformity of the whole dielectric area.

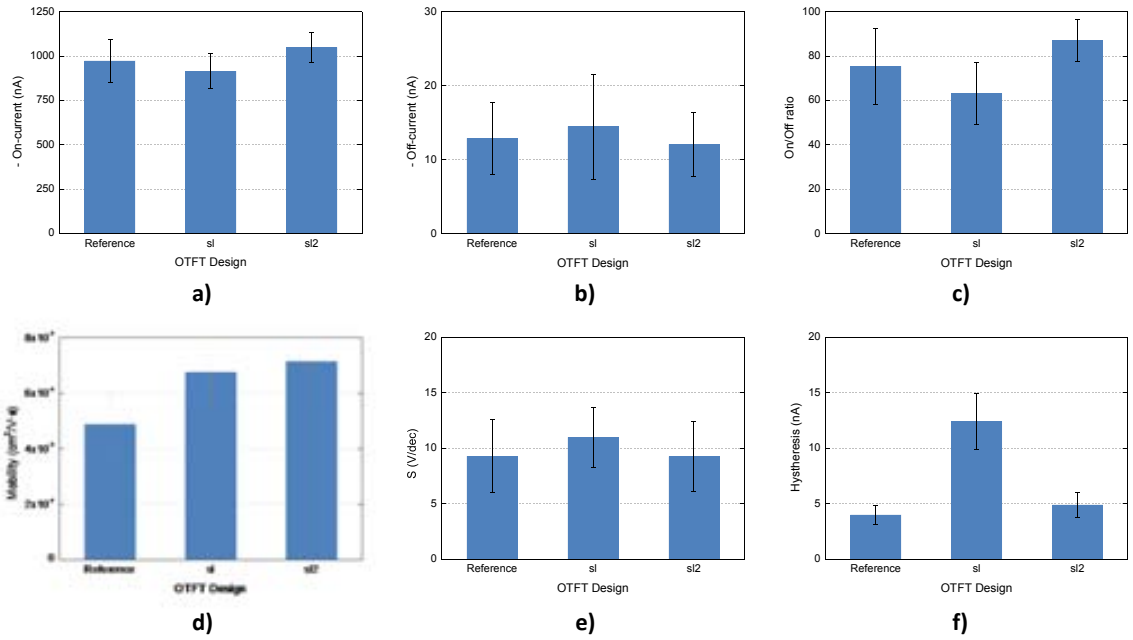


Figure 6.19. Electrical parameters of OTFTs for the different topologies changing the transistor width: a) On-current; b) Off-current; c) On/Off current ratio; d) mobility; e) Subthreshold slope (S); and f) hysteresis.

Finally, Figure 6.19e shows the subthreshold slope for the topologies studied. Only slight variations can be observed maybe due to the intrinsic data range.

It is worth to note that all the transistors used for this analysis were fabricated and characterized at same time and belong to the same fabrication batch. Different topologies were uniformly distributed in the foil in order to reduce the consideration of temporary printing effects. Thus, a clear significant advantage can be seen in using narrower fingers instead of the wider ones (*reference*). Best results are clearly obtained with the *sl2* design.

6.3.3. Non-overlapped gate OTFTs

Printed devices typically suffer from degraded performance due to poor material quality and very high overlap capacitance [71][185][52][54], limited by the poor layer-to-layer registration of printing techniques. While material quality has improved, registration remains a tremendous bottleneck in printed devices. Some efforts have been made to realize self-aligned devices but processes are still complex as they depend on wetting and dewetting processes compromising device variability and yield.

In this section, we fabricated all-inkjet devices using a patterned gate electrode, resulting in significant improvement of the overlap capacitance and thus, device performance. The use of the patterned electrode reduces the gate overlap and at same time contributes to the self-alignment of S/D electrodes.

For this experiment, a transistor (column ❶ marked *T40/10E3*) was used as a reference design to compare with the non-overlapped device (column ❹ marked *T40/10E3nov*), as shown in Table 6.7.

Table 6.7. OTFT topologies and W/L ratios fabricated for the current experiment.

OTFT reference	L [µm]	finger length [µm]	# of fingers	W [µm]	W/L ratio
T40/10E3	40	2000	6	10E3	250
T40/10E3nov	40	2000	6	10E3	250

All transistors have a W/L ratio of 250, same areas of dielectric and OSC and same S/D pattern (metal2), thus they are exactly having same dimensions for the entire layer stack. Main difference resides on the patterned gate as shown in Figure 6.20. Only metal1 and metal2 layer are shown for clarity of the layout.

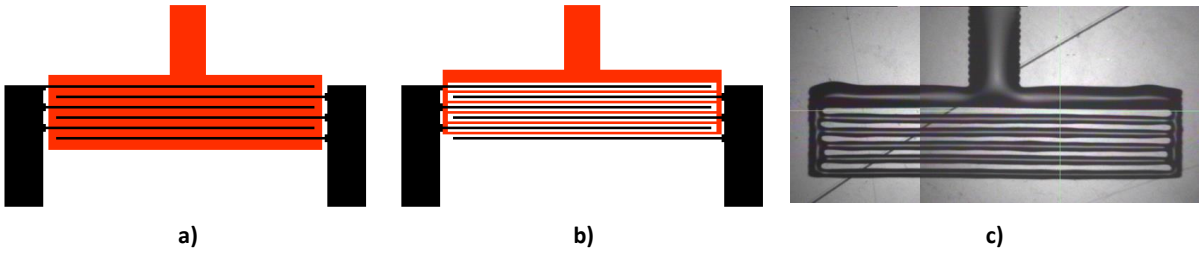


Figure 6.20. a) Gate and S/D layouts of the *reference* OTFT; b) gate and S/D layouts of the *non-overlapped* OTFT; and c) picture of the printed *non-overlapped* gate.

The channel length (L) was designed to be 40 µm being 19.1 ± 3.4 µm the effective values as shown in Figure 5.12b.

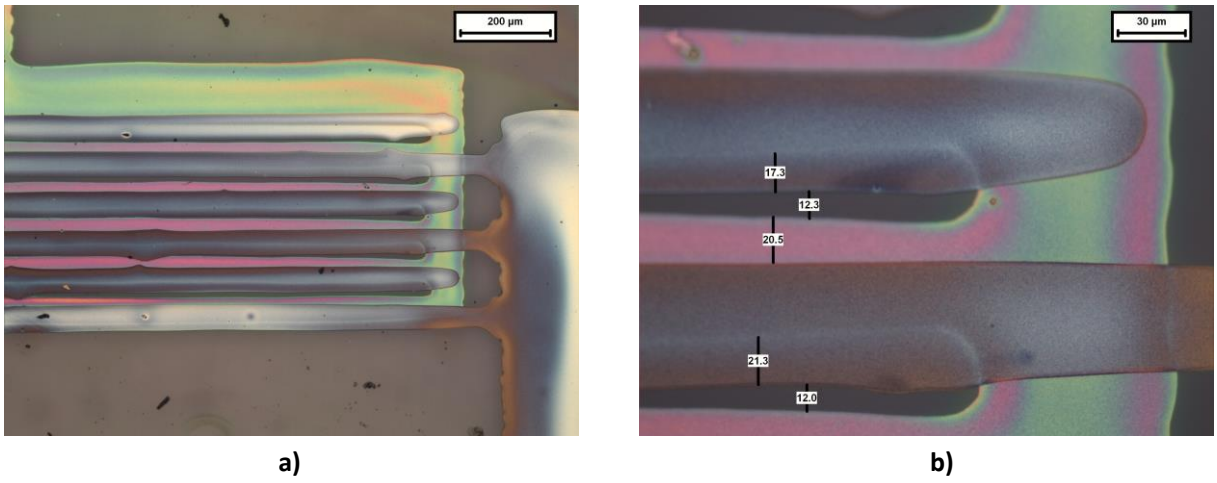


Figure 6.21. a) Picture of a non-overlapped OTFT; and b) drain and source interdigitated electrodes of the printed OTFT and their misalignment. The measurements of L were performed by optical microscope.

The L values were also measured for the *T40/10E3nov* design appearing to be larger due to the self-alignment process with an average of 19.1 ± 3.4 µm as shown in Figure 6.21b. Source and drain are have a bigger separation due to the underneath gate height that facilitates S/D ink dewetting. Figure 6.22 shows FIB-cuts performed at Fraunhofer ENAS facilities[38]. Figure 6.22a shows the source and drain fingers on top of the fingered gate. Gate finger width is 50.79 µm. Source and drain slightly overlap the finger gate but with a reduction of 30% compared with the solid pattern used in the *reference* design.

[38] Fraunhofer ENAS located in Chemnitz (Germany)

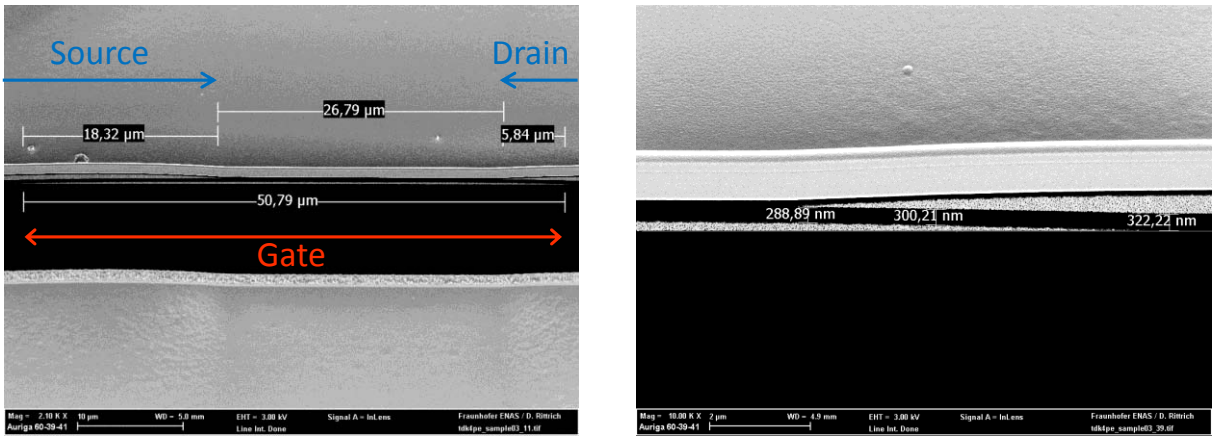


Figure 6.22. a) FIB-cut of a complete gate finger with the measures of overlap, separation and gate width; and b) FIB-section of the S/D to gate overlap.

Figure 6.23 shows the vertical capacitance and resistance measured between gate and S/D electrodes. There is an important reduction in the capacitance (up to ˜78%) due to the reduction of the overlapping area (up to ˜72%). The difference between both values can be originated by the capacitance of the surroundings of the gate area, not only by the overlapping area itself.

Figure 6.22b depicts the different dielectric thicknesses measured in the overlapping area between S/D and gate layers. It can be observed that the dielectric thickness is not constant in this area. An accumulation of dielectric appears in the valleys compared with the gate peak. Thickness suffers a reduction of a 10% between the beginning and the end of the overlapping area. This difference demonstrates a non-uniform distribution of the dielectric layer over its area due to the patterned gate layer.

Moreover, Figure 6.22a shows a misalignment of 6.24 µm in the vertical direction due to intrinsic printer misalignment.

Similar important results are obtained with respect to the resistance. An increase up to ˜394% is obtained resulting in a reduction in gate leakage current as shown in Figure 6.24b. These were the main objectives of this experiment and obtained results demonstrate that the approach was successful.

Comparative output, transfer curves and extracted electrical parameters are shown in Figure 6.23 and Figure 6.24.

Figure 6.25d shows similar mobilities for both transistor topologies. Figure 6.24c and Figure 6.24d shows the transfer curves in linear and semilog scale. Based on these results we can observe similar hysteresis levels for both designs as quantified in Figure 6.25f.

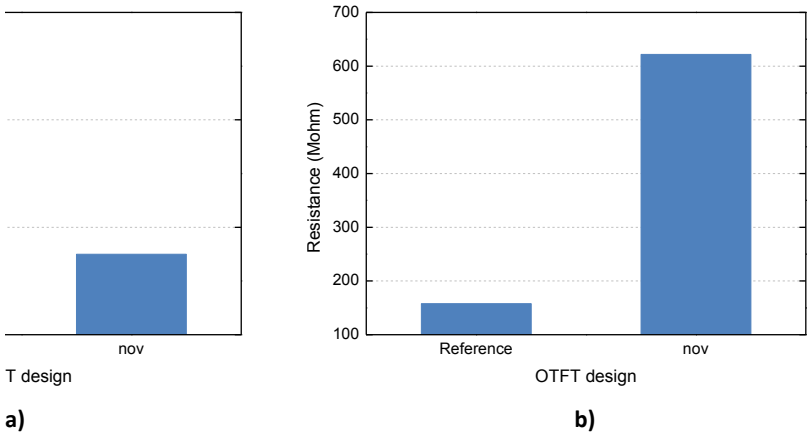


Figure 6.23. Gate to source/drain: a) capacitance and b) resistance.

From the graphs, we can observe that non-overlaped transistors show better behavior than the *reference* one in output curves but not in transfer curves.

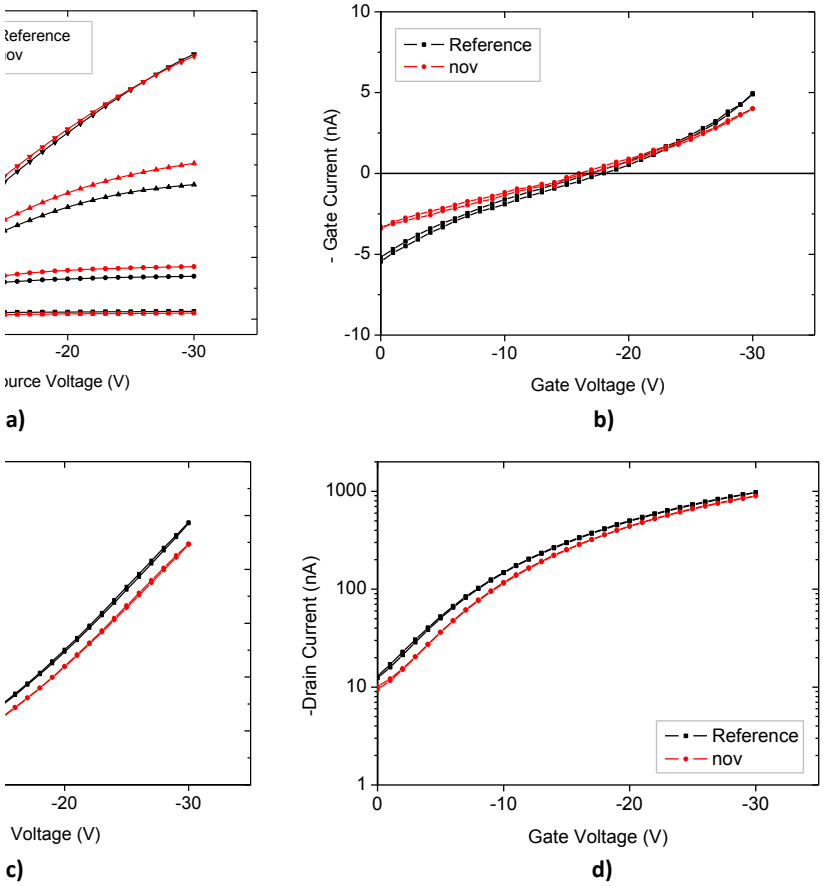


Figure 6.24. Drain-source current and gate current for Transfer and Output curves for the OTFTs under study: a) Output curves; b) Leakage current with V_{DS} = -30V; c) Transfer curve in saturation region with V_{DS} = -30V; and d) Transfer curve in semilog scale with V_{DS} = -30V.

As already demonstrated, this effect is typical in organic transistors due to bias stress. Nevertheless, we can conclude that from a performance point of view they show similar behaviors although best advantage is the reduction of gate capacitance, increase of gate resistance and thus the reduction in Off-current and gate leakage current.

Also, similar Off-currents can be observed for all the designs as show in Figure 6.24d and Figure 6.25b, although non-overlaped transistors shows a slightly smaller Off-current level compared with *reference* causing an increase in the I_{ON}/I_{OFF} ratio as shown in Figure 6.25f.

Finally, Figure 6.25e shows the subthreshold slope for the topologies studied with similar results.

It is worth to note again that all the transistors used for this analysis were fabricated and characterized at same time and belong to the same fabrication batch.

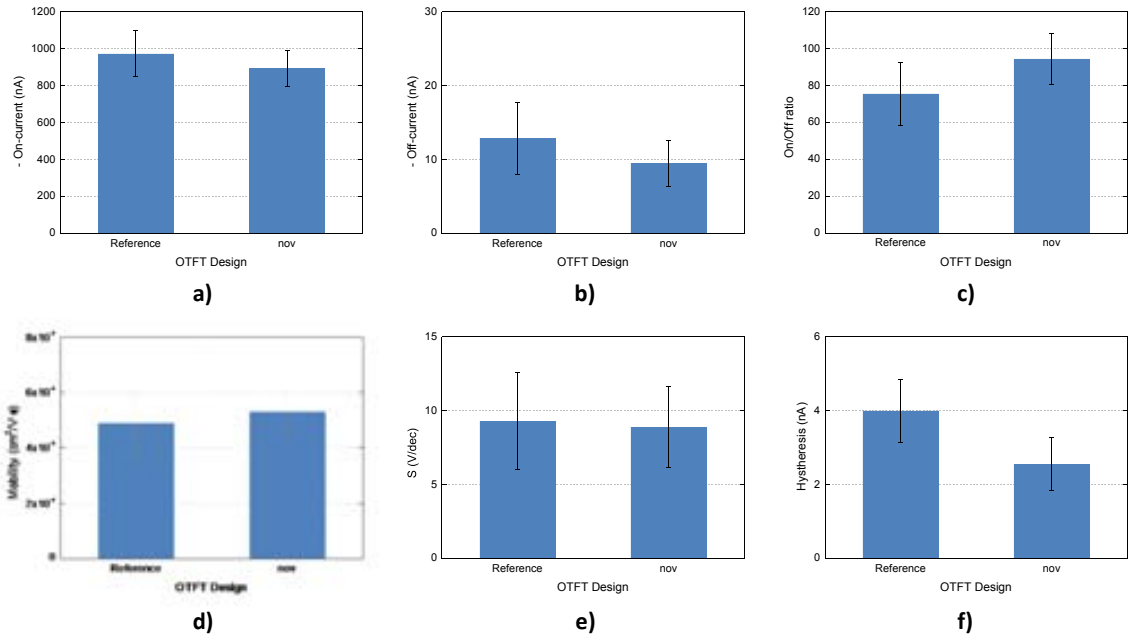


Figure 6.25. Electrical parameters of OTFTs for the different OSC layer thicknesses obtained for different drop spaces used during printing: a) On-current; b) Off-current; c) On/Off current ratio; d) mobility; e) Subthreshold slope (S); and f) hysteresis.

Some clear advantages can be seen in using non-overlaped devices instead of the normal ones (*reference*). Main advantages are the reduction in gate-to-S/D capacitance and the increase of gate resistance thus reducing the gate leakage current. This is an interesting result in terms that these parameters have been improved just changing the gate patterns without any other change in transistor fabrication neither functional materials development. That means that this improvement can be added to the previous ones without any additional costly change on them.

6.4. Summary and conclusions

We have reported the development of different strategies for the improvement of the inkjet-printed transistors developed in the Chapter 4.

Three different improvement strategies were studied on the current chapter:

10. OTFT Encapsulation Strategies.
11. Improvement of functional layers deposition.
12. Optimization of OTFTs by design.

We have demonstrated that using a MMAcoMAA coating layer improves the lifetime and I_{OFF} current in inkjet-printed transistors using a BG-BC topology. But the MMAcoMAA deposition on the OSC bulk clearly affects the I_{OFF} current and mobility of devices suggesting undesirable interaction between the photoresist and the organic semiconductor film.

It was clearly demonstrated that the gate dielectric thickness can be tuned through the design dimensions of the dielectric pattern area. This result, added to the previous results shown in Chapter 3 about the yield and performance of dielectric layer in capacitors, provide a good methodology to improve the performance of the device due to this essential layer in active devices as transistors.

The experiments made shows how the reduction of the OSC layer thickness (DS increase) results in a reduction of both I_{ON} and I_{OFF}. But since I_{OFF} reduction is larger than I_{OFF} reduction, the final I_{ON}/I_{OFF} ratio increases.

The reduction of I_{OFF} confirms the theory that the Off-current is partly created by the current flowing through the bulk as the electric field created because the gate is not being able to close completely the OSC channel due to the high thickness of the OSC layer. An additional work should be done to lower the OSC thickness thus reducing the I_{OFF} and improving I_{ON}/I_{OFF} ratio. This reduction should be obtained through the modification of the OSC solution formulation because an increase of the drop spacing used on the OSC layer deposition results in a discontinued surface.

Finally, the approach to improve OTFTs by changing its design geometries and topologies was also successful. Different approaches were studied changing design parameters, orientations and layer patterns in order to study the effect of these parameters on final transistor behaviour.

The strategy of using wider or narrower transistors changing finger width and length. Using devices with wider fingers instead of the minimal ones (one-pixel fingers) did not produce any significant advantage. Best results were obtained with the *Reference* design (the one

used in chapter 4). This is an important result in the sense that justifies the use of minimum width fingers allowing the increase of transistor density through the fabrication of reduced size OTFTs.

A clear significant advantage was observed when narrower devices were used instead of the wider ones (*reference*). Best results were clearly obtained with the *sl2* design.

Important results were obtained in using non-overlaped devices instead of the wider ones (*reference*). Main advantages were the reduction in gate-to-S/D capacitance and the increase of gate resistance thus reducing the gate leakage current. This is an interesting result in terms that these parameters have been improved just changing the gate patterns without any other change in transistor fabrication neither functional materials development.

As a result, the cut-off frequency of the printed transistor is significantly enhanced since the overlap capacitances are minimized.

Summarizing, the following ideas can be considered to improve OTFTs performance and behavior:

- The use of MMAcoMAA resin to improve device stability over time and reduce I_{OFF}.
- The reduction of the gate dielectric thickness through the design dimensions of the dielectric pattern area improves the electrical parameters associated.
- The reduction of the I_{OFF} parameter through the reduction of the OSC layer thickness by printing methods (change in drop spacing).
- Narrowing transistors results in better performances and behaviour thus improving integration density.
- Using non-overlaped devices in order to reduce gate-to-S/D capacitance and increase gate resistance thus reducing the gate leakage current.

In conclusion, the current experiments gave us an update to the recipe developed in Chapter 4 giving us better transistors than those obtained before.

7. ALL-INKJET CIRCUITS AND SYSTEMS

In this chapter, we introduce circuit concepts and propose implementations for OTFT-based logic gates starting from all-inkjet inverters.

A standard procedure will be used for characterizing OTFT-based logic circuits by using different methods of assessing robustness and timing-related performance figures of logic gates [186]. Procedures for characterizing static and dynamic behaviour of basic logic circuits are discussed and used. The scope of this chapter is to obtain figures of merit quantifying the performance of certain OTFT generations.

Finally, an adaptive backend strategy for low-yield OTFT digital circuits for digital cells based on pseudo-pMOS logic using inkjet printed interconnections will be presented. The approach is based on a novel interdigitated OTFT design layout with unconnected fingers having different lengths and the standard-cell concept. Fingers and NAND2 standard-cells are individually connected to customize gates and increase OTFT and circuit yield.

7.1. Introduction to Logic Circuits

Logic gates are the principal building blocks of digital logic circuits. They can be considered as combinations of "switching elements" used in Boolean algebra to perform computing operations.

7.1.1. Basic circuits concepts

The most basic logic gate in a logic family is the inverter. In OTFT-based logic circuits, it is commonly represented in the form of a pull-down and a pull-up element switching the inverter's output to ground (GND) or to the supply voltage (V_{DD}) via a low-resistance path. Figure 7.1 shows the schematics of commonly-used configurations of inverters.

Circuits using only one type of semiconductor (either n-type or p-type) require a combination of one pull-up (n) or pull-down (p) "load" transistor that is always in its On-state and an input-controlled "drive" transistor that changes the output of the inverter by logically inverting its input [187][39][188]. Therefore a low voltage (logic level 0) at the input generated produces a high voltage (logic level 1) at the output and vice-versa [186].

The "load" transistor can be connected to its source, to its drain or to an independent bias voltage source as shown in Figure 7.1a, Figure 7.1b and Figure 7.1c. If the gate is connected to its source (as shown in Figure 7.1a) a fixed gate-source voltage V_{GS} = 0 V results. This is the most popular configuration and will only work if the transistor is switched On (V_T < 0V) and is referred to as normally-On or depletion mode in literature [189]. A normally-On transistor in this configuration yields an approximately constant drain current as long as it operates in the saturation region. Hence, the configuration of a load transistor with the gate connected to its source is referred to as current-source load (CSL) configuration [190][53].

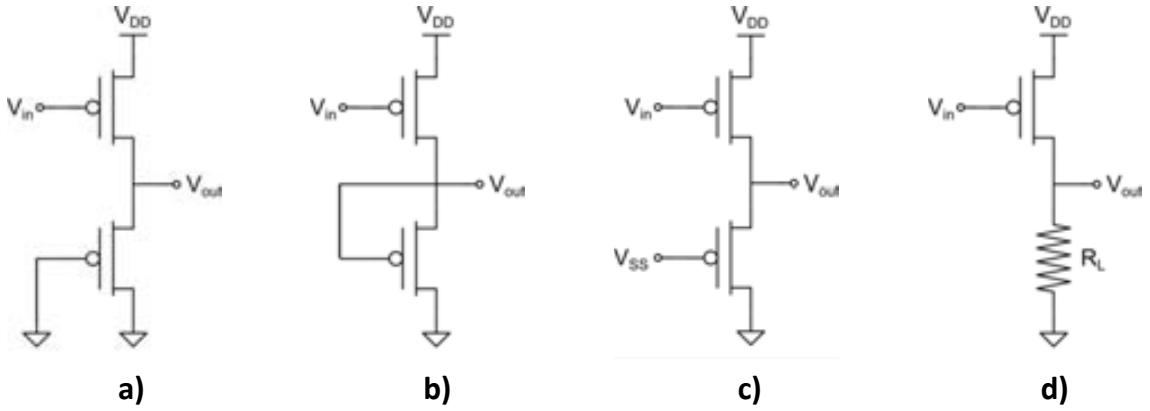


Figure 7.1. Basic configurations of OTFT design styles for basic inverters: a) current-source load (CSL) configuration; b) Load transistor in diode load (DL) configuration; c) Ratioed pMOS Logic with 2 supply voltages; and d) resistor load (RL) configuration.

If the gate of the load transistor is connected to the drain, a fixed gate-drain voltage V_{GD} = 0V results in a transforming the transistor into a diode for the "load", as shown in Figure 7.1b. Therefore, this configuration is referred to as diode load (DL) or depletion-mode load configuration [191][173].

The fact that most organic semiconductor materials exhibit weakly normally-on or weakly normally-off behaviour (high Off-current) leads to poor performance of the input transistor as it can only be switched Off bringing the transistor into depletion mode, e.g. by biasing it in negative voltages for p-type semiconductor, as shown in Figure 7.1c.

Figure 7.1d uses a resistor as the pull-up element connecting the output to the supply rail V_{DD}. Several examples of circuits utilizing resistor can be found in the literature [53].

Figure 7.2 shows the relationship between the voltage transfer curve (VTC) for p-type OTFT, which is the plot of the output voltage as a function of the input voltage.

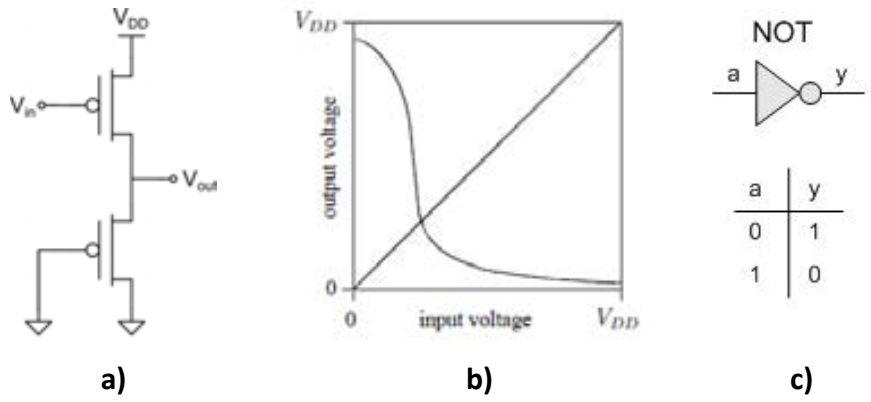


Figure 7.2. a) Schematic of a CSL-type inverter; b) Voltage Transfer Characteristics (VTC); and c) Inverter symbol and its corresponding truth table.

The output voltage is determined by the ratio between the channel resistance of the drive transistor at a given input voltage and the resistance value of the load element. For this reason these gate topologies are called ratioed logic.

This ratioed behaviour has also consequences on the circuit speed. High resistance element (load) will charge the output capacitance slower than the low resistance one (drive) what will let to different propagation delays for propagating 1 and 0 logic levels.

The inverter gate is a circuit that gives the inverse logic output of its input, as shown in its truth table in Figure 7.2c. The truth table gives us a first glance of the behavior of this logic gate. Boolean logic is based on two logic levels: '0' and '1' where (in positive logic) '0' should be a voltage level close to 0 V also referred as GND (or lower reference voltage) and '1' means the existence of a positive voltage closed to V_{DD} (the upper reference voltage).

7.2. Circuit characterization

In the domain of logic circuits and gates, the following figures of merit need to be characterized [186][192]:

- Robustness, i.e. valid logic levels and noise margin.
- Timing, including rise/fall times, transition times and clocking requirements.
- Driving capability, i.e. fan out characterization.
- Input capacitance.
- Power consumption.

These characteristics and especially the first two (logic levels/noise margin and timing) can also be used for evaluating the performance of any OTFT gate implementation. Therefore, it is worth to take a closer study at the mechanisms of the characterization process.

The unity-gain method is the standard procedure for analysing noise margins of logic circuits can only be applied with care.

One important characteristic of logic circuits is their robustness because most OTFT-based logic circuits suffer from non-ideal VTCs [186]. Robustness defines the ability of a logic circuit to detect and issue valid voltage levels for the different logic states in the presence of noise at the input signals. In a general way, noise is defined as any deviation from nominal voltages [193], and can be caused by [194]:

- Device variability owing to fabrication process or operating point.
- Spurious signals or crosstalk.

For OTFT-based logic circuits, the contribution of device variations is more important than spurious signals due to the low packing density of organic logic circuits, the immaturity in the fabrication technology and the high voltage being applied (compared of what is common in silicon logic). Several possibilities exist to derive information on the robustness of logic circuits. A selection of these will be used in the following sections.

7.3. All-inkjet printed Inverter

In this section we report on the fabrication and characterization of all-inkjet printed inverters implemented with pseudoPMOS logic style.

7.3.1. Proposed circuit structure

The design of the inverter logic gate uses one p-type OTFT for logic control connected to another p-type OTFT acting as a load. We will use this approach by applying a positive voltage (bias) at its gate (V_{SS}), as shown in Figure 7.3. This configuration allows the analysis of the inverter structure using different configurations.

The advantage of the use of an OTFT as a load is the implementation of an equivalent resistor without increasing the stack of materials[39]. The resistor behavior is obtained from the resistance of the channel in saturation region. This design style is called pseudo-pMOS (coming from its silicon origin name) or Ratioed pMOS Logic with 2 supply voltages [195].

The resistance of the channel in saturation region must be high enough to ensure the given ratio between drive and load transistors. Fixing the channel length L to the minimum value provided by the technology, the resistance of the channel will directly depend on the channel width W. This will allow setting the right ratio between (W/L) of both transistors to assure that the voltage divider provides the expected output.

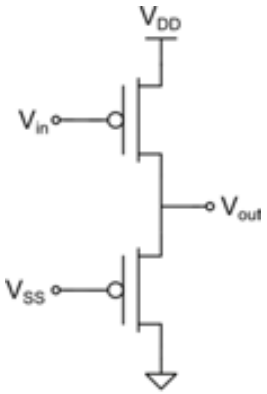


Figure 7.3. Schematic of the inverter circuit used.

The load is always a single p-type transistor, whose gate is biased to remain On continuously. The drive p-type transistor creates a conducting path from the output to V_{DD} when the input is '0' producing a '1' at the output. When the drive transistor has a '1' in its

[39] Due to the fact that a new material would be needed to implement the resistor since the required resistance implemented with metals would have too large area compared with the transistor.

gate closes the conducting path to V_{DD} and, thus, the load p-type transistor pulls the output to '0'.

The relative sizing of the drive and load networks is critical, since the load transistor is always biased On. When the drive should pull the output to logic 1, the load network will still be trying to pull down the output to logic 0. In our process, the W/L ratio of the drive transistors is always sized with a width of 8 to 15 times bigger than the W/L ratio of the load transistors.

7.3.2. All-inkjet inverter fabrication

By using the same OTFT fabrication procedure developed in Chapter 4, we fabricated several all-inkjet printed inverters on PEN flexible plastic substrate, as shown in Figure 7.4, consisting of one load OTFT and one or two drive OTFT for obtaining different W/L load/drive ratios. Figure 7.4a show an inverter consisting of one load and two drivers. Figure 7.4b shows a group of three inverters in cascade to obtain a ring oscillator.

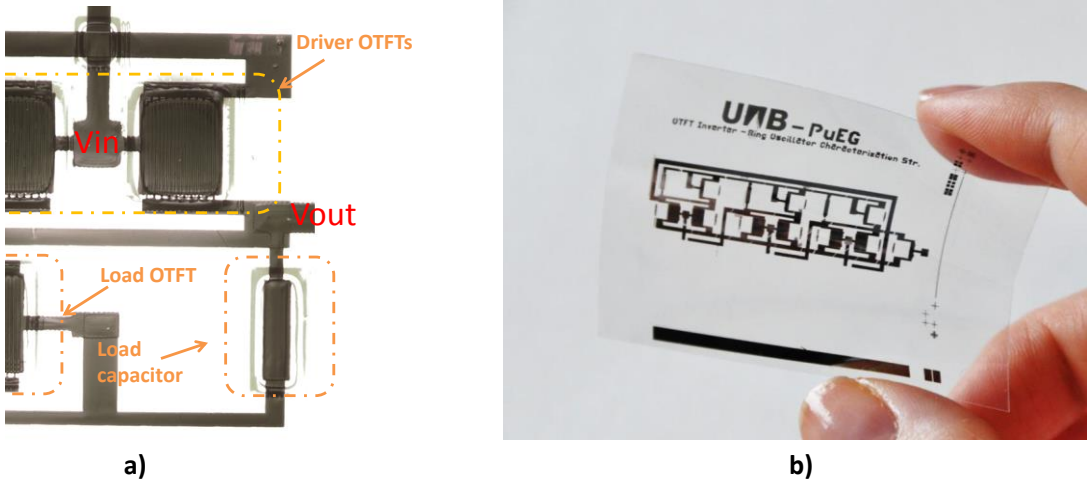


Figure 7.4. a) An all-inkjet organic inverter, b) Picture of a group of three inverters in cascade to obtain a ring oscillator.

Layouts of fabricated sheets are shown in Annex C.13. The different inverter structures were characterized in the following sections.

7.3.3. DC analysis

Different analyses were performed to obtain the best configuration, load/drive ratio and circuit parameters. The biggest challenge building logic circuits with the all-inkjet OTFTs developed in the current work is their low I_{ON}/I_{OFF} ratio. The transistors used to build

inverters and logic gates presented ON/OFF current ratios of 200-300, quite far from the 10^3-10^4 considered as a minimum to obtain suitable digital circuits [133].

The main challenge is to reduce the I_{OFF} drain current improving the device structure or, in case of pseudoPMOS logic, straggling the load OTFT by inverting V_{SS} to move the OTFT to depletion, thus, reducing the normally-On state. Figure 7.5b shows the drain current curve on a logarithmic scale (black, left axis) and the gate current (blue, right axis). The graph shows that the OFF current is reduced in a factor of 4 closing the channel at 0V or at 15V, so an important increase in I_{ON}/I_{OFF} ratio can be obtained by just controlling the gate voltage of the load transistor.

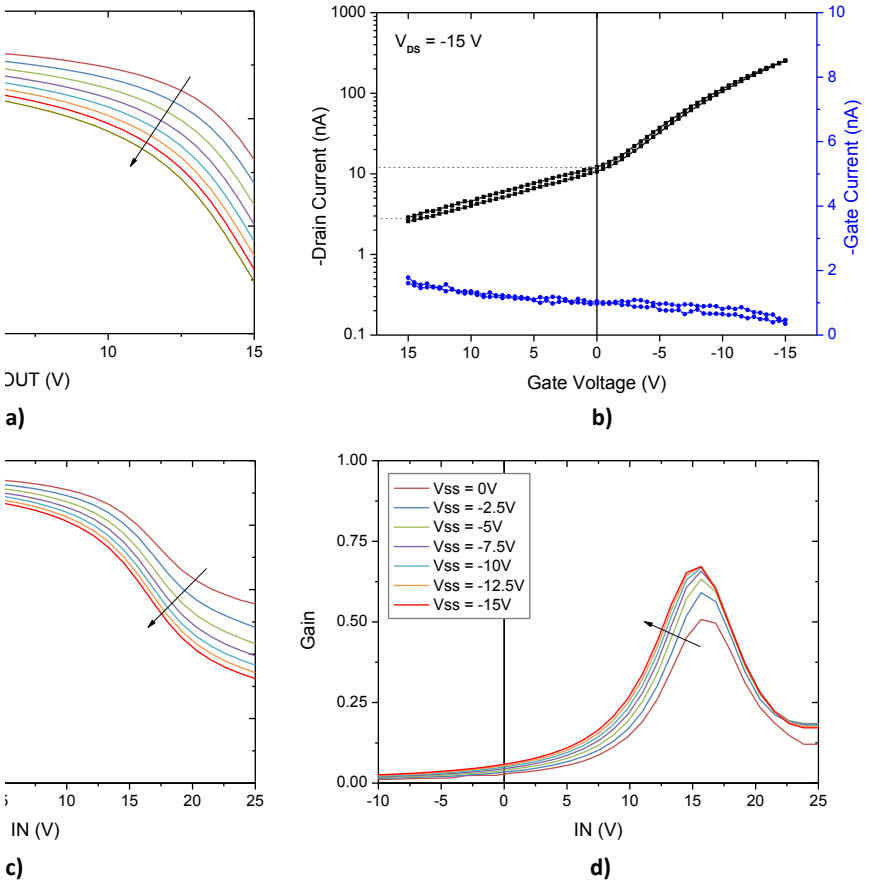


Figure 7.5. a) VTC for different V_{SS} (V_{DD}=15V and V_{in} ranging from 0 to 15V); b) Transfer characteristics (I_D) on a logarithmic scale (black, left axis) and gate current in a linear scale (blue, right axis); c) VTC; and d) Gain VTC for different V_{SS} (V_{DD}=12.5V and V_{in} ranging from -10 to 25V).

Figure 7.5a shows the Vin/Vout (hereinafter referred as Voltage Transfer Characteristic or VTC) for a fabricated inverter structure. Operation conditions are V_{DD}=15V, V_{in} ranging from 0V up to 15V and V_{SS} from 0 to -14V in -2V steps. It can be observed we improve significantly the inverter behavior by reducing the I_{OFF} current.

Figure 7.5c shows the VTC for an inverter with V_{DD}=12.5V, V_{in} from -10V up to 25V and V_{SS} ranges from 0 to -15V in -2.5V steps. In this configuration we can see a clearer inverter behavior. Although this is a typical manner to illustrate an inverter behavior in the literature, it is a useless approach as those operation conditions does not allow connecting gates in cascade to build up larger circuits. Nevertheless, we can observe that larger Vin values help obtaining successful inverter behaviors.

Figure 7.6 shows the VTC and the Gain for an inverter structure with several V_{DD} values from 8V to 15V, and V_{in} ranging from -10V up to 20V. Figure 7.6b shows that higher V_{DD} results in higher inverter gains.

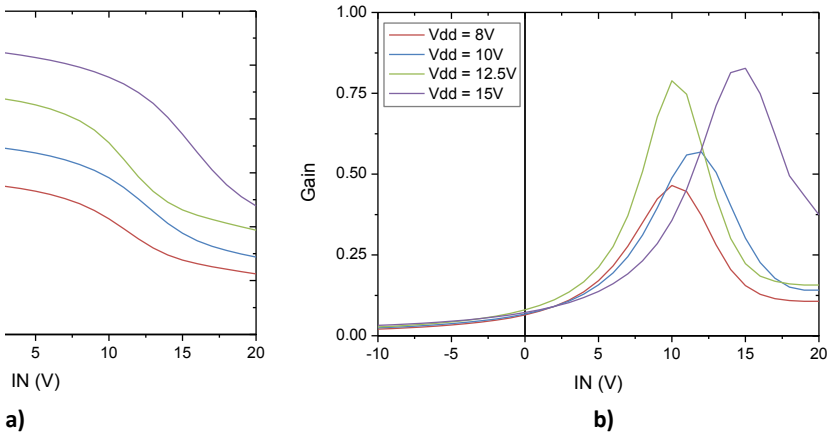


Figure 7.6. a) VTC; and b) Gain for different V_{DD} values (V_{in} ranging from -10 to 20V and Vss=0V).

Finally, inverters with different drive/load W/L ratios were measured, as shown in Figure 7.7. As already mentioned, the resistance of channel in saturation region must be high enough to ensure a relation about several times between drive and load transistors.

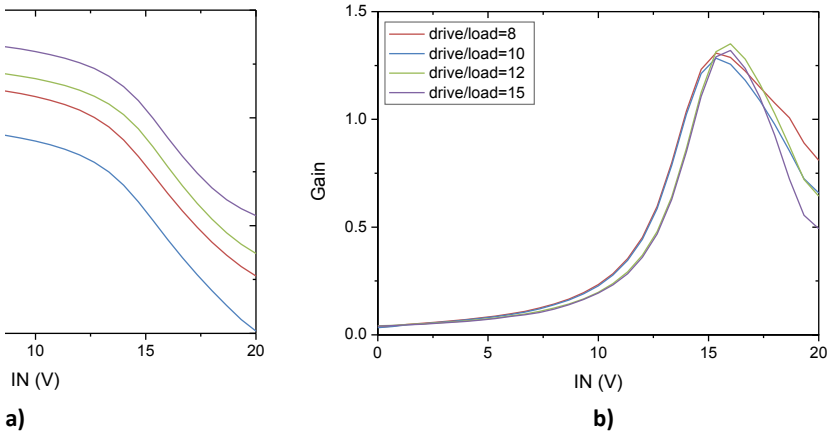


Figure 7.7. a) VTC; and b) Gain for different drive/load ratios (Vin ranging from 0 to 20V, V_{DD}=20V and Vss=0V).

However, due to the poor quality of the inverter structures fabricated, no special differences can be observed in Gain.

Figure 7.8 shows the experimental results for the best fabricated inverter structure for V_{DD}=28V and V_{in} ranging from 0V up to 28V. The inverter VTC is shown in Figure 7.8a. A clear inverter behavior is obtained and a voltage gain with a maximum value of 2.3 as shown in Figure 7.8b.

The voltage gain ($\Delta V_{out}/\Delta V_{in}$ ~ 2.3) is larger than 1, implying that this gate (also according to its output range) can be used to switch subsequent stages in more complex logic circuits without voltage degradation.

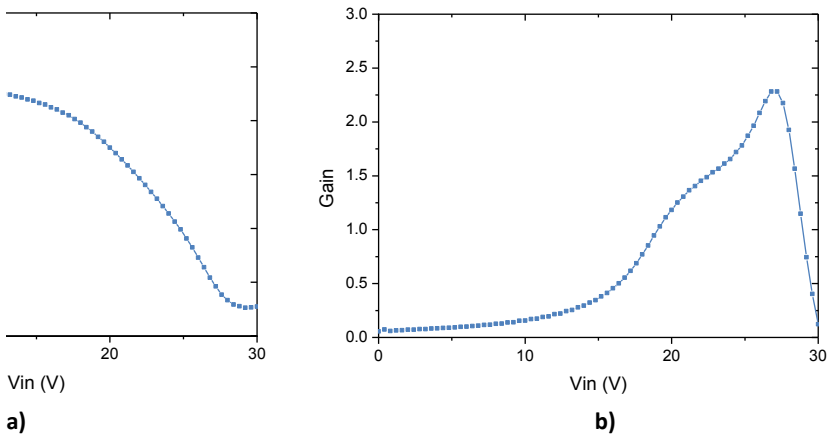


Figure 7.8. Experimental results of the all-inkjet organic inverter: a) VTC characteristics; and b) Gain.

As shown in Figure 7.8b, the peak in the gain is shifted to higher values of the input voltage. Although gain value is good, this shift is not interesting from the circuit behaviour point of view because it means that noise margins are not comparable resulting in this non-optimal inverter behaviour.

From Figure 7.9 we can extract some parameters related to the inverter robustness. VNM_H (High-state Noise Margin Voltage) and VNM_L (Low-state Noise Margin Voltage) are defined as the maximum noise signal which can be superimposed on the input without causing a malfunction in the circuit. These parameters give us a figure of merit of the robustness of the inverter circuit [196][197][198].

V_{IL} (Input Low Voltage), V_{IH} (Input High Voltage), V_{OL} (Output Low Voltage), V_{OH} (Output High Voltage) values are extracted at the point where slope is -1. These points are marked with a red square in Figure 7.9a. V_{IL} corresponds to the value such that if Vin < V_{IL} we have a logic 0. In a similar way, V_{IH} corresponds to the value such that if Vin > V_{IH} we have a logic 1. In Figure 7.9a we can observe that the "0" and "1" regions are not similar, and in the case

of the "1" region its width is not enough to ensure a proper operation when connecting inverters in cascade. Table 7.1 shows these values and also, the calculated Voltage Noise Margins. This behaviour can be observed in Table 7.1 because the High Noise Margin is negative, when it should be positive and, when possible, similar to the Low Noise Margin.

Analysing robustness by the method of squares, as shown in Figure 7.9b is even worst, resulting in a non-existing noise margins for the best fabricated inverter. The maximum square noise margin can be calculated by rotating the true and reflected VTCs by 45° and then calculating the differences between the two curves. These differences are equivalent to the diagonals of the squares between diagonal points of the two VTCs. Nevertheless, in our case differences cannot be observed and squares cannot be drawn.

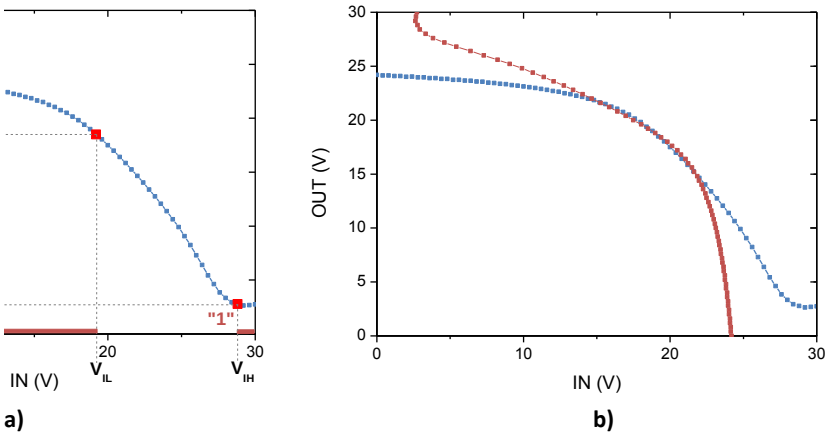


Figure 7.9. a) Noise margins of an inverter; b) Graphical extraction of maximum-square noise margin.

Table 7.1. Voltage Noise margins measured

Parameter	Value
V_{IH}	*28.8*
V_{OH}	*18.49*
$VNM_H = V_{OH} - V_{IH}$	***-10.31***
V_{IL}	*19.2*
V_{OL}	*2.77*
$VNM_L = V_{IL} - V_{OL}$	***16.43***

Usually, we desire a large VNM_H and VNM_L values for best noise immunity.

7.3.4. Dynamic analysis

Other types of analysis are usually performed on OTFT circuits such as AC, transient and noise analysis. AC and Noise analysis are quite specific for analog devices that operate on continuous signals and they do not apply for logic circuits (especially for high supply voltage).

Transient analysis is critical for digital circuits since it gives the maximum processing speed reachable. Figure 7.10 shows the transient output of the inverter when a square signal with a period of 200ms is applied at the input of the inverter circuit.

In order to avoid the fast degradation of the organic semiconductor, a maximum V_{DD} of 10V was used and V_{SS}=-15V.

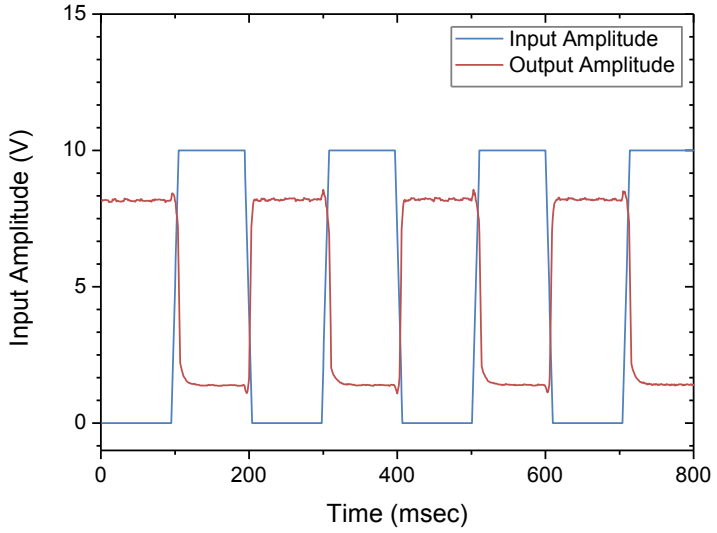


Figure 7.10. Transient output of the inverter circuit when a square signal of t=200ms is applied at the input.

The ratioed nature of the pseudo-pMOS circuit produces that the rising transitions of the output voltage (from '0' to '1') were much faster that falling transitions (from '1' to '0'). This is due to the fact that load OTFTs (discharging path) are worse conductors than drive transistors (charging path).

The rise time is defined as the time between 10% and 90% of the voltage swing (V_{OH}-V_{OL}) at the rising edge. Fall time is the similar concept for the falling edge, in this case from 90% to 10%.

The dynamic performance of a logic circuit family is characterized by propagation delay of its basic inverter. The average propagation delay is defined as the average of low-to-high and the high-to-low propagation delays. The Falling Propagation Delay (T_{pHL}) is the time needed from rising input to falling output measured at the 50% of its signal swing and the Rising Propagation Delay (T_{pLH}) is the time needed from falling input to rising output measured in

the same conditions. The propagation delay increases as the fan-out increases. Therefore, the maximum fan-out is defined according to the maximum acceptable propagation delay time that is an arbitrary number.

Figure 7.11 shows the dynamic parameters on the transient curves captured for the inverter characterized. Table 7.2 shows the measured values for rise and fall times and propagation delays.

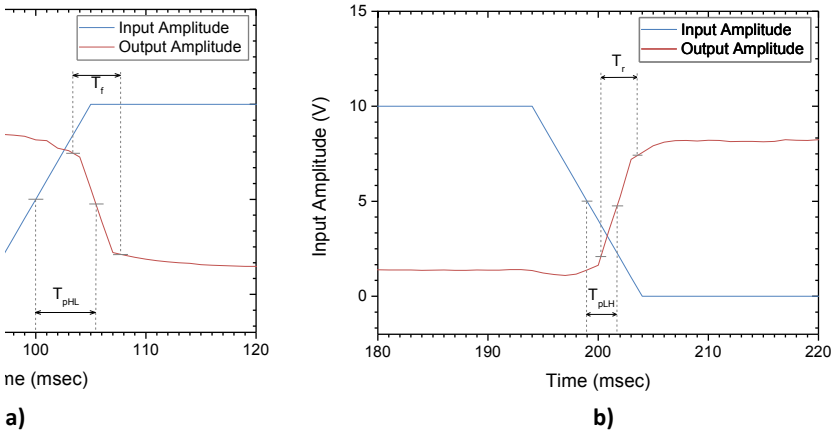


Figure 7.11. Dynamic parameters extraction for logic gates.

An inverter with a rise time (T_r) of 3,5ms, and a falling time (T_f) of 4,4ms and a maximum switching frequency of 126 Hz has been obtained, fabricated using the process technology developed in chapter 4 with a coating layer of MMAcoMAA.

Table 7.2. Dynamic parameters for the all-inkjet inverter.

Parameter	Value [ms]
T_{pHL}	*5.3*
T_f	*4.4*
T_{pLH}	*1.9*
T_r	*3.5*

In literature, inkjet-printed inverters have been reported with switching frequencies up to a few hundred hertz. The fall time (T_f) is determined by the On-current of the input transistor and by the load capacitance of our measurement setup (~100pF). The rise time (T_r) was designed to be comparable to the fall time by adjusting the load resistance through the drive/load ratio.

Further improvements could be done by increasing polymer mobility and reducing channel length and source/drain-to-gate overlap capacitance.

Figure 7.12a shows a 3-stage inverter circuit schema to evaluate the signal propagation through a chain of inverters. Figure 7.12b shows the output of each stage. Due to the shift of the VTC related to variability reasons, the signal degradation is significant after the first inverter stage, therefore losing the inverter behavior after the second stage. This result justifies that any functioning ring oscillator has been obtained in this thesis work by using the OTFTs fabricated.

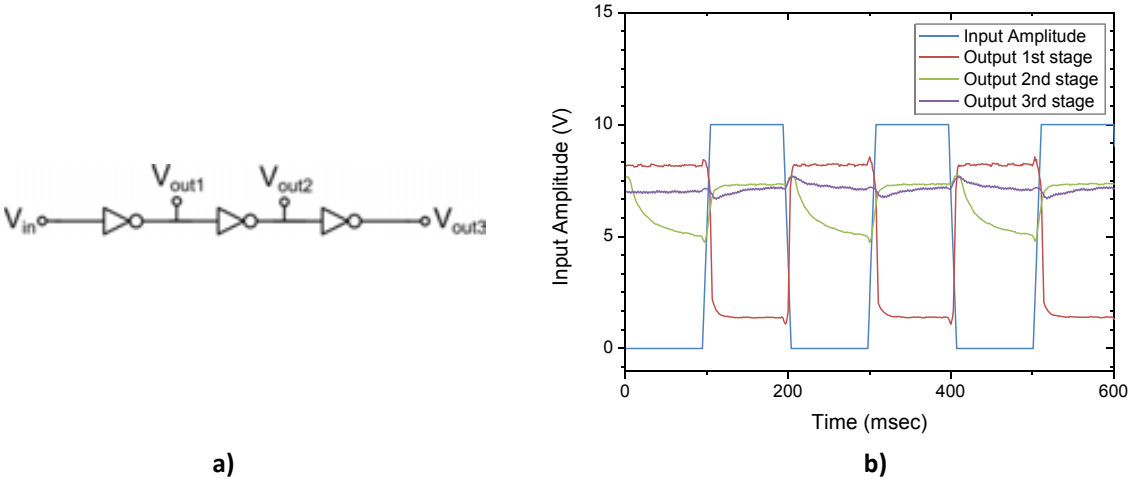


Figure 7.12. a) 3-inverter stage; b) (blue) Input amplitude of the ring oscillator, (red) output amplitude for the 1st stage of the ring oscillator (V_{out1}), (green) output amplitude for the 2nd stage of the ring oscillator (V_{out2}), (purple) output amplitude for the 3rd stage of the ring oscillator (V_{out3}).

7.3.5. All-inkjet NAND2 circuit

A NAND2 circuit is a NAND gate with two inputs. It produces and output that is '0' only if both inputs are '1'. From a circuit point of view, it can be considered as an inverter with two inputs with their corresponding drive transistors in parallel. Figure 7.13a depicts the electric schema of a NAND2 circuit. Figure 7.13b shows the corresponding symbol and truth table.

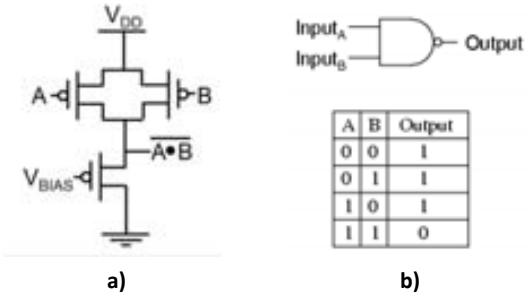


Figure 7.13. a) NAND2 schematic; and b) NAND2 symbol and truth table.

Figure 7.14 shows the transient output of a NAND2 circuit when a pulsed signal of T=200 ms and 10V is applied at the input with V_{DD} = 10V and V_{SS} = -15V. As depicted in the figure,

output is '0' when both inputs are '1'. The output when one of the inputs is set to '1' and the other one is switching is similar to those obtained for the inverter circuit in the previous section, as depicted in Figure 7.10. In the case that one of the inputs is fixed to '0', the output signal is not able to keep a good logic 1 degrading its value over the time, as shown in the right part of Figure 7.14 (IN B equals '0'). Value results stable after 2 sec of operation.

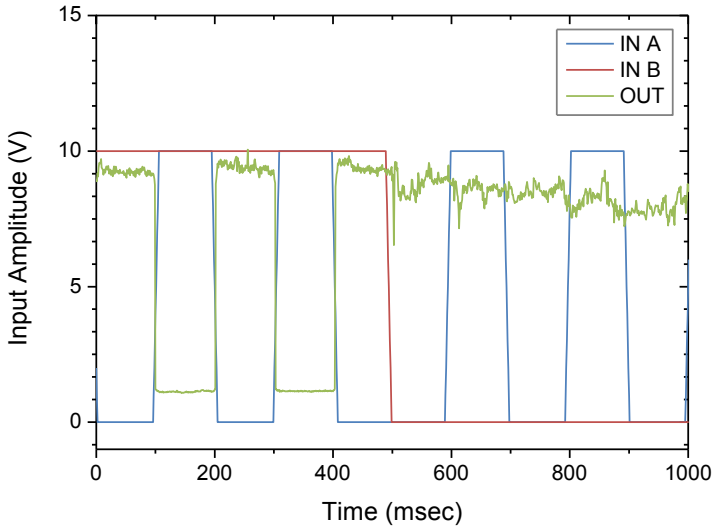


Figure 7.14. Transient output of the NAND2 circuit when a square signal of T=200 ms is applied at the input.

Nevertheless, the achievement of a functional NAND2 gate is a good conclusion for the current work.

7.4. An inkjet adaptive backend strategy for low-yield OTFT digital circuits

This section describes and illustrates an adaptive backend strategy for low-yield OTFT digital circuits to build digital cells based on pseudo-pMOS logic using inkjet printed interconnections.

This approach is based on a novel interdigitated OTFT design layout with unconnected fingers having different lengths. Fingers are individually connected to customize W/L ratio and avoiding failures, thus increasing OTFT yield.

As a first step, each transistor in the fabricated array is characterized finger by finger to identify the partially working devices and obtaining a map of Known Good OTFTs (KGOs) with an associated range of valid W/L ratios. As a second step, a modified standard cell approach is used for generating low-cost, quick turnaround and custom logic circuits. The standard cell concept is based on basic NAND2 cells with configurable drive/load ratios based on the KGOs map. And finally, a third step consists in connecting selected fingers on KGOs and designing the routing for the matrix connections.

An inkjet deposition process connects working transistors to form individual gates and finally, the desired circuit functionality. With this methodology, suitable logic circuits could be obtained based on low yield fabrication processes.

7.4.1. Configurable OTFTs

As discussed in the previous chapters, the variability of the devices and the relative low-yield is a drawback to use this technology to build successful circuits and systems. Nevertheless, the possibility to use inkjet printing as a mask-less deposition process to connect working transistors to form individual gates and finally, the desired circuit functionality, is an interesting approach. With this methodology, suitable logic circuits can be obtained based on low yield fabrication processes, as inkjet printing.

7.4.1.1. Design of configurable OTFTs

This new approach proposes a novel interdigitated OTFT design layout with unconnected fingers having different channel widths. Fingers are individually connected to customize W/L ratio and discarding non-functional fingers, thus increasing OTFT yield.

Thus, the scope of building configurable OTFTs is double. For one side, we can tune-up the OTFT W/L ratio with a reduced number of transistor geometries. As it will be demonstrated, with only two OTFT designs we can set-up transistors with W/L ratios from 1.1 to 36.7. So,

variability in OTFTs can be compensated by modifying the finger connection to obtain the right drive/load OTFT ratio in logic gates.

Additionally, a short circuit between two fingers or a low-resistivity or short-circuit from S/D-to-gate, does not invalidate the entire OTFT, increasing device yield despite of a change on its W/L ratio.

For this purpose, two different topologies of transistors were designed: a small transistor for 'load', and a large transistor for 'drive'. The fingers are unconnected and have different widths to combine and to increase the number of possible combinations to achieve.

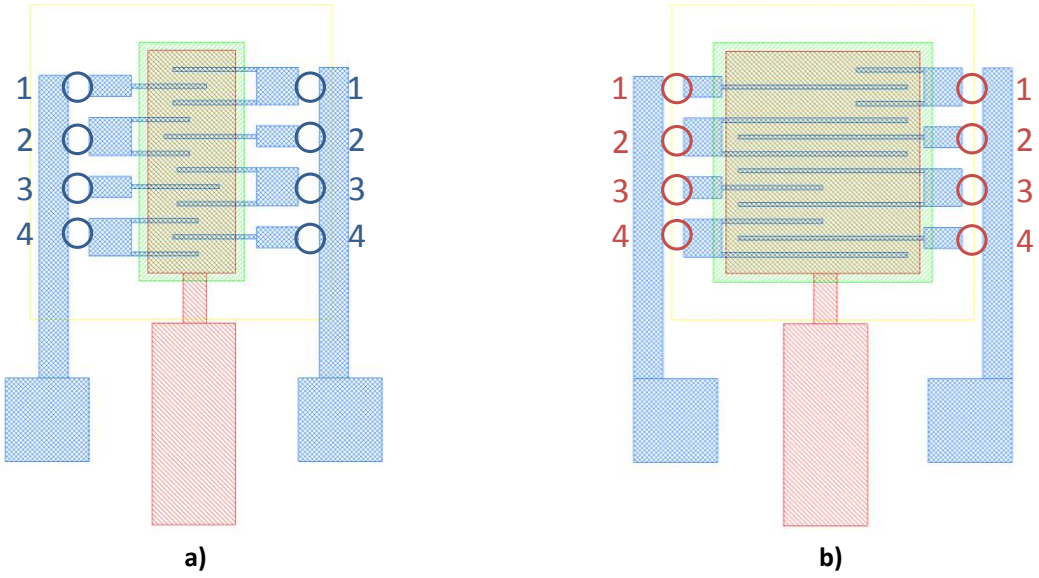


Figure 7.15. Two OTFTs designs layouts with unconnected fingers: a) small OTFT for load; and b) large OTFT for drive.

The fingers have a small pad on source/drain and a large vertical pad for the gate. As probe needles need to move from top S/D pads (numbered 1) to bottom pads (numbered 4) without changing the distance between probes, a large gate pad is required.

Fingers or group of fingers can be connected individually. Both source and drain fingers with the same number need to be connected at same time. A single drop placed on the circles connects the finger with the device pad. Therefore, each group of fingers is characterized and connected individually (1, 2, 3 and/or 4). With this approach, by using only two OTFT topologies we can obtain up to 26 different channel lengths (W).

Figure 7.16 show all the possible combination of fingers and channel widths (W) obtained. The different finger combinations results in 26 different channel widths by using the two OTFT designs depicted in Figure 7.15.

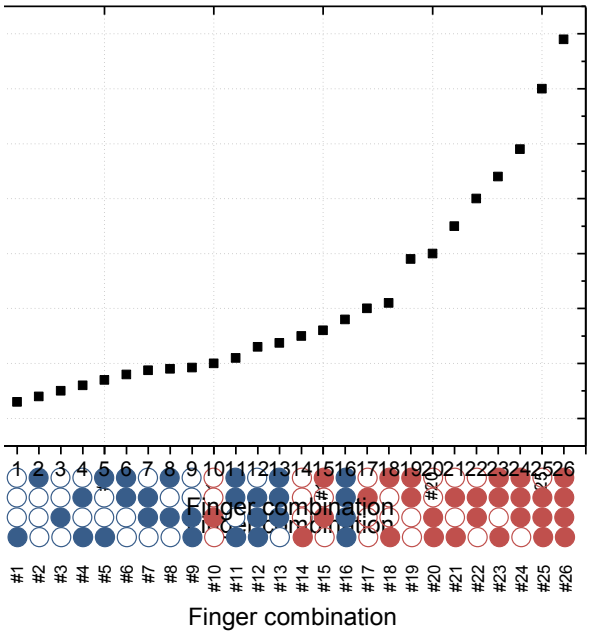


Figure 7.16. The different finger combinations offers 26 different channel lengths (W) with only two OTFT topologies.

By using these two OTFT topologies as load and drive transistors in a logic gate, e.g. an inverter, we can obtain up to 196 combinations creating up to 60 different W/L ratios from 1.1 to 36.7.

Figure 7.17. 196 combinations creating up to 60 different W/L ratios from 1.1 to 36.7.

7.4.1.2. Fabrication and characterization of configurable OTFTs

In the framework of the TDK4PE FP7 EU project, a large batch of devices was fabricated at TUC[40] during a research stage and characterized in order to analyze the scalability, variability and yield of the configurable OTFTs. OTFTs were characterized at IMB-CNM[41] facilities using a semiautomatic probe station. Figure 7.18 shows the small and large configurable OTFTs.

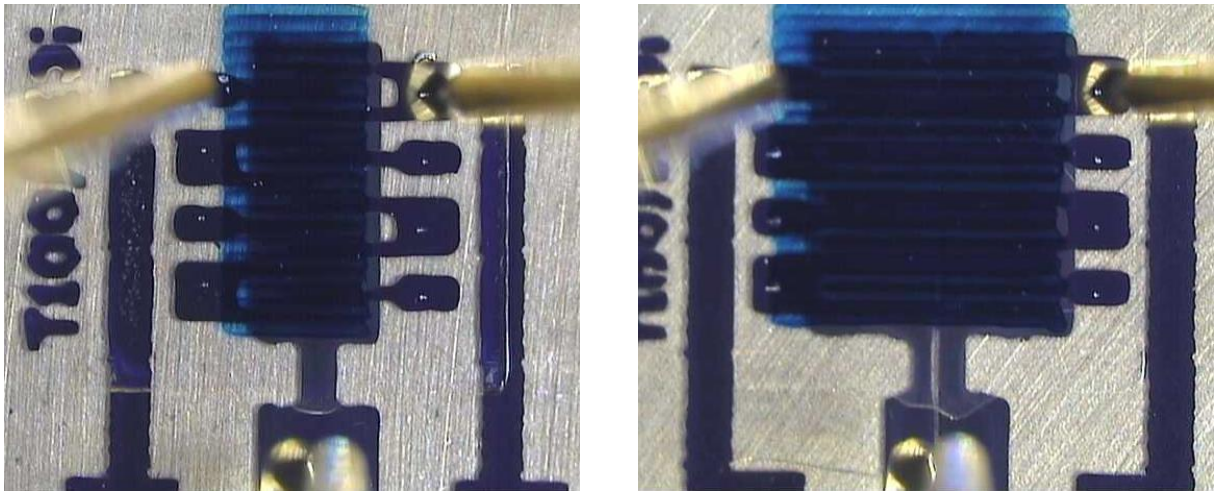


Figure 7.18. Pictures of the configurable OTFTs with unconnected fingers: a) small OTFT for load; and b) large OTFT for drive.

10 foils containing 798 OTFTs resulting in 3192 sub-devices (each OTFT has 4 groups of unconnected fingers) were printed and characterized. The fabricated OTFTs used an Organic Semiconductor (FS0096 from Flexink Inc).

Figure 7.19 shows the characterization results of a single sheet (A4) of configurable OTFTs. Figure 7.19a and Figure 7.19b shows the failure origin for small and large configurable OTFTs. As depicted in both graphs, the failure origin can be diverse already shown in previous chapters.

Figure 7.19c and Figure 7.19d shows the yield related to working sub-devices (each configurable OTFT consists of 4 sub-devices or groups of unconnected fingers). Only a small portion of configurable OTFTs shows 4 working sub-devices (all the configurable OTFT). This means that using normal transistors (with connected fingers) the yield of the small and large

[40] TUC: Technical University of Chemnitz
[41] IMB-CNM: Institut de Microelectrònica de Barcelona- Centre Nacional de Microelectrònica, Barcelona, CSIC.

OTFTs should be 22% and 16% respectively. Other OTFTs have between one, two, three or four non-working sub-devices.

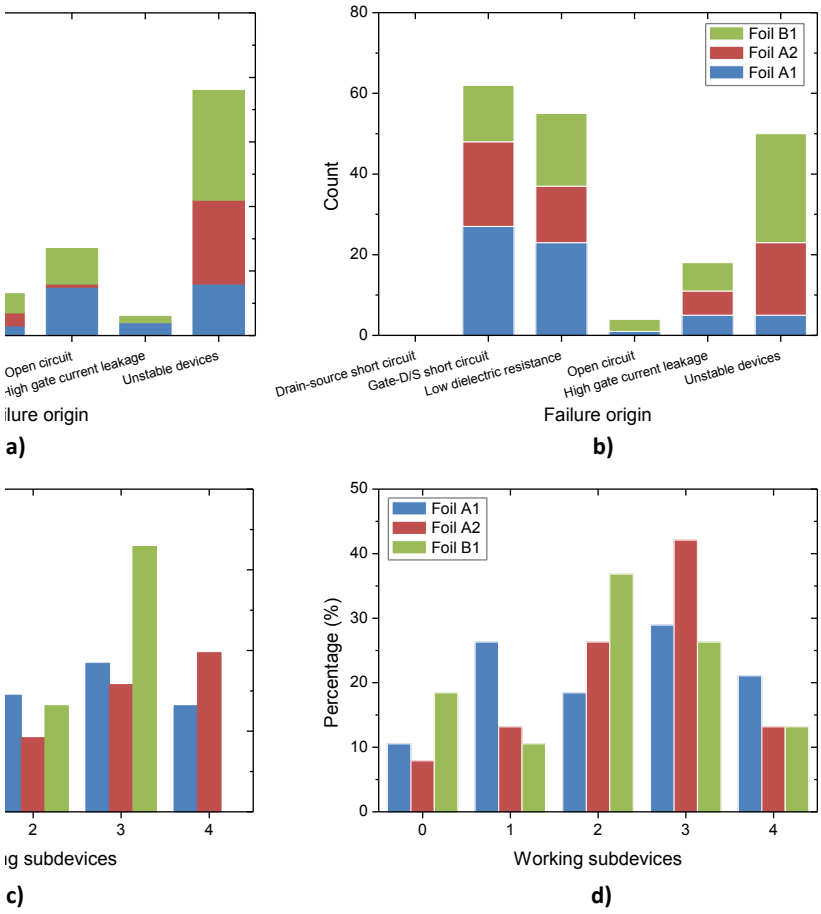


Figure 7.19. Failure origin for: a) small configurable OTFTs and b) large configurable OTFTs; and percentage of working sub-devices for: c) small configurable OTFTs and d) large configurable OTFTs.

Transistors with at least one non-working sub-device are still operative although its W/L ratio has been modified. The corresponding W/L drive to load transistor ratio will need to be modified to keep the requirements for proper gate operation. By using this approach, the yield of the configurable OTFTs is increased in small and large transistors up to 94.7% and 87.7% respectively.

These results demonstrate the validity of the approach, especially important in a low-yield technology as inkjet printing.

7.4.2. Standard-cell logic circuits using configurable OTFTs

This section describes and illustrates the adaptive backend strategy proposed for low-yield OTFT digital circuits when using digital cells based on pseudo-pMOS logic. This is only a

proposed methodology. Although the designs were fabricated and the configurable OTFTs characterized, any circuit more complex than a NAND2 gate was obtained.

7.4.2.1. Facing device variability and yield by Standard-cell approach

The standard cell concept is based on basic NAND2 cells using configurable OTFTs. Figure 7.20a and Figure 7.20b shows the NAND2 schema and its corresponding layout using configurable OTFTs. Figure 7.20c shows the position of the NAND2 cell with its associated interconnection matrix.

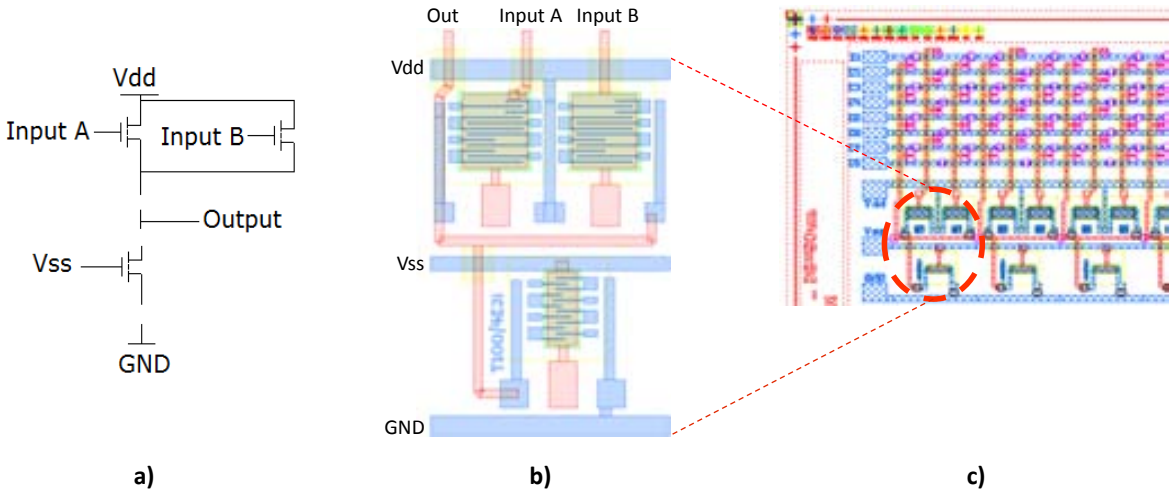


Figure 7.20. NAND2 Standard-Cell: a) schematic; b) standard cell with unconnected fingers and transistors; and c) NAND2 standard-cell and associated interconnection matrix.

As a first step, each transistor in the fabricated array is characterized finger by finger to identify the working sub-devices (or partially working devices) and obtaining a map of KGOs with an associated range of valid W/L ratios.

In this thesis, the first step was done by using a semiautomatic characterization set-up extracting all the curves from each sub-device and extracting the related transistor electrical parameters that will be used in a backend process to identify the KGOs and also, which ranges of W/L ratios and drive/load ratios can be obtained by using the working sub-devices in the standard-cell NAND2 circuit. Figure 7.21a and Figure 7.21b shows the semi-automatic characterization setup [199], measured curves and a map of KGOs. Figure 7.21c depicts an example of NAND2 standard cell with non-working sub-devices (marked with a red cross) and the connected working sub-devices to obtain a given load/drive ratio based on the curves and the KGO map.

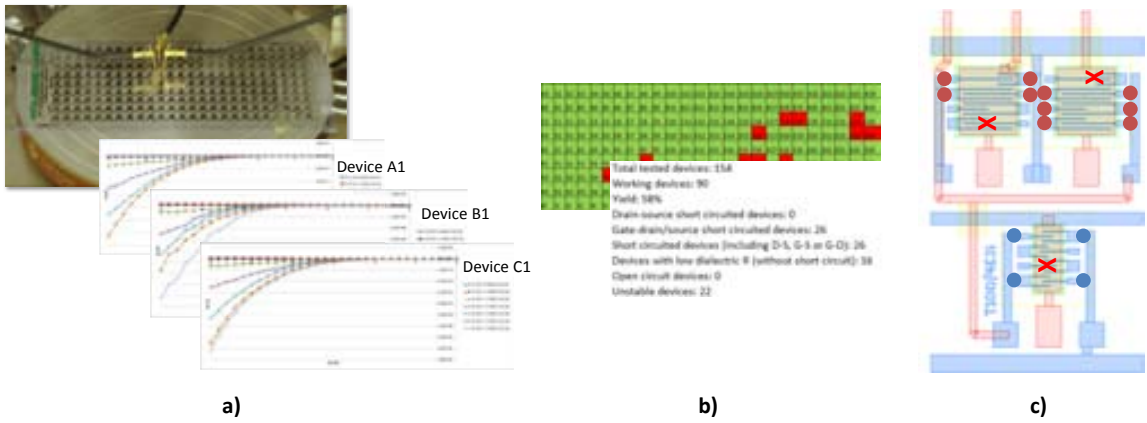


Figure 7.21. a) Semi-automatic characterization setup and measured curves; b) map of KGTs; and c) example of standard-cell connection.

Then by using the mapping of working OTFTs, the routing of (1) OTFT selected fingers of the NAND2 and (2) matrix interconnections is done through the deposition of silver nanoparticle ink drops by selective inkjet printing technique.

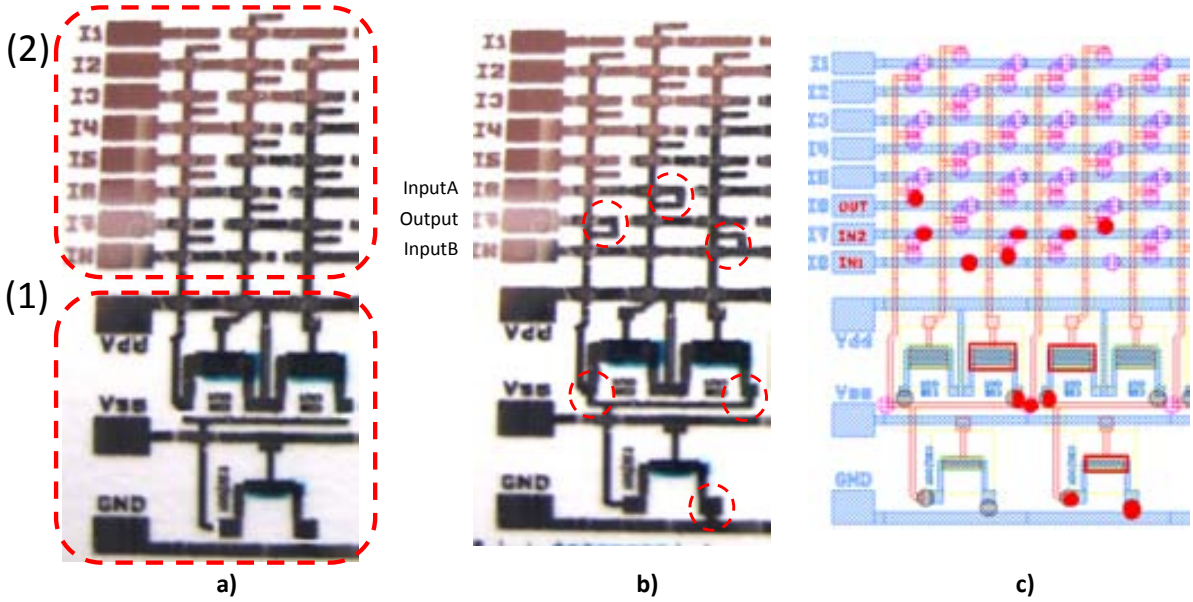
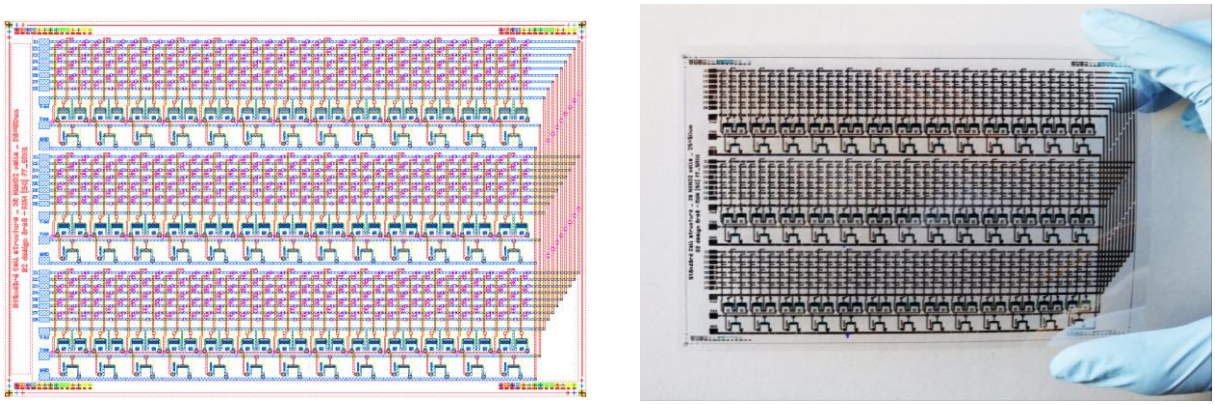


Figure 7.22. Vertical and horizontal interconnection matrix lines and OTFTs are initially unconnected: a) unconnected NAND2 cell and interconnection matrix; b) connected NAND2 cell and interconnection matrix; and c) layout of a NAND2 gate by using different OTFTs and connected through the interconnection matrix.

Figure 7.22 illustrates this process. Figure 7.22a show the connected configurable OTFTs (red square labelled 1). Based on the working OTFTs with configurable drive/load ratios based on the KGTs map and the required interconnections to wire the proposed circuit, the interconnection matrix is used. Then, an additional step consists in designing the routing for

the matrix connections in order to wire the required transistors to form a specific gate, e.g. a NAND2 gate as shown in Figure 7.22c.

With this methodology, suitable logic circuits could be obtained based on low yield fabrication processes. Figure 7.23 shows the layout of the design consisting of 39 NAND2 standard-cell circuits and the picture of an A5-size fabricated standard-cell design at TUC capable to build digital circuits using NAND2 gates design-style.



a) b)

Figure 7.23. Layout of the design consisting of 39 NAND2 standard-cell circuits; and b) picture of an A5-size fabricated standard-cell design.

7.4.2.2. Fabricated example

As an example of the design methodology, an A5-size fabricated standard-cell design was fully characterized and resulting on the KGOs map and the available transistors, a 4-bit shift register circuit was designed using the standard-cell layout.

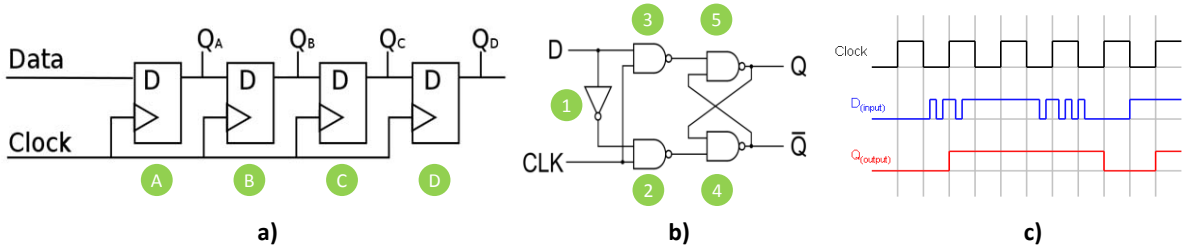


Figure 7.24. a) 4-bit shift register circuit consisting in four D flip-flop sub-circuits; b) schematic of a D-flip-flop; and c) timing diagram.

Figure 7.24 shows the 4-bit shift-register and the D flip-flop circuits and its corresponding timing diagram. Figure 7.25 illustrates the resulting interconnections based the KGO map. The green circles indicate each stage of the flip-flop (labelled from A to D) and each NAND2

gate composing each D flip-flop (labelled from 1 to 4). Red market OTFTs indicates non-working transistors.

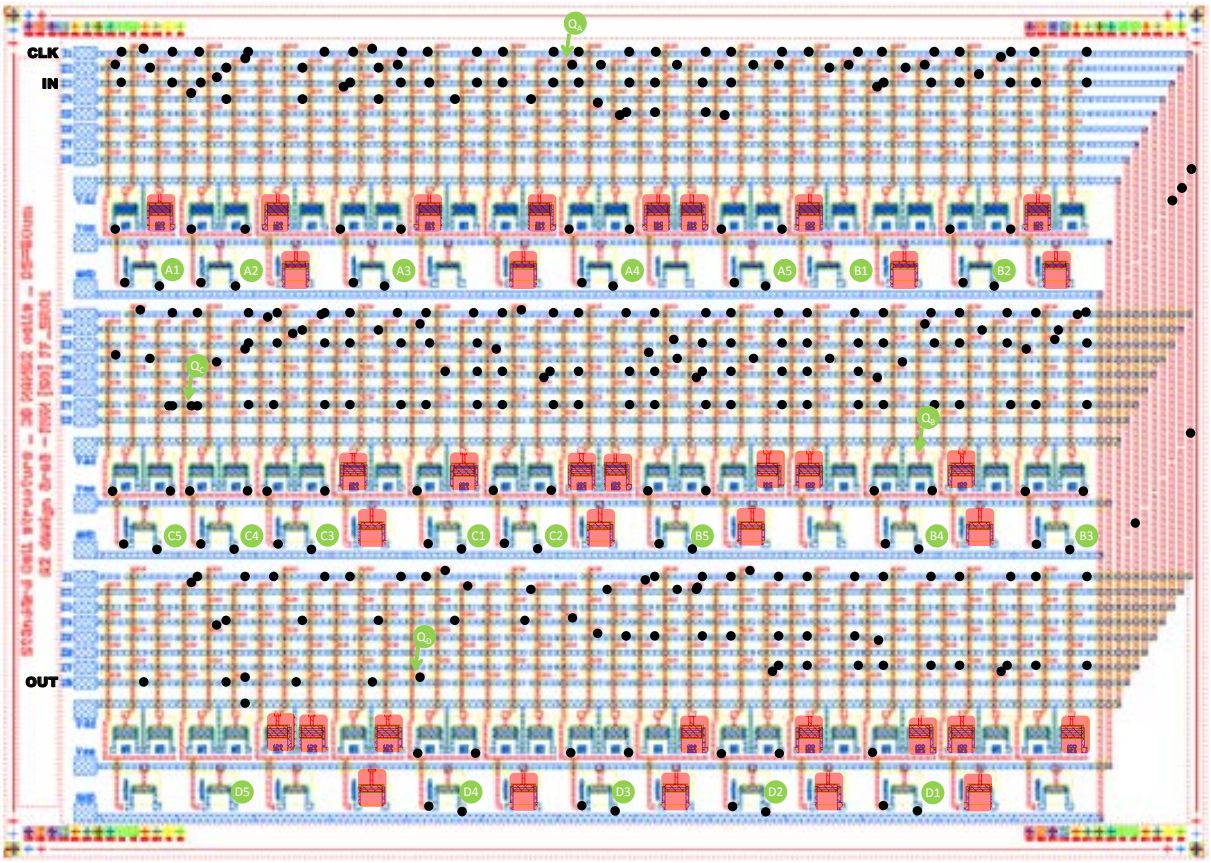


Figure 7.25. Example of wiring for a 4-bit shift register circuit by sing the standard-cell approach.

7.5. Summary and conclusions

Electrical properties of the inverter have been presented in the current chapter. Static and dynamic analysis shows how all-inkjet inverters work without enough performance to build more complex circuits when more than one single stage is required. Functional NAND2 gates have also been demonstrated. Main weakness is related to OTFT performance. The low On/Off drain current ratio is a key issue in the design using pMOS-only logic, as the load transistor is always ON, thus reducing output swing.

OTFT stability plays also an important role. Threshold voltage variations affect the noise margins of the logic gates are and the optimal drive/load ratio. Thus high variability can be transformed into a severe limitation of the number of logic gate stage that can be chained. This limits the amount of circuits that can be implemented. Lack of stability also plays an important role in a circuit that use to work in continuous operation.

A new methodology is presented for circuit design to implement circuits taking into account the poor yield and high variability in Printed Electronics. The methodology proposed is based on Standard Cells and configurable OTFTs. NAND2 is proposed as a basic logic gate for Standard Cell. Initially, NAND2 OTFTs and matrix interconnections are unconnected being adaptive to the fabrication yield. Finally, the routing of OTFTs and matrixes is done by inkjet printing.

8. CONCLUSIONS AND FUTURE WORK

This short chapter shows the general conclusions related to this thesis dissertation compared with the initial objectives, and afterwards, it lists open issues and potential future research directions on the area following this research.

8.1. Overview and General Conclusions

A new technology for low-cost and large area applications is emerging to cover the cost and technological gaps associated with conventional microelectronic processing techniques. The research, as well as the industry community, is working to lead the next electronic revolution at low cost: Flexible, Organic and Large Area Electronics (FOLAE).

Over the past two decades a big effort have been dedicated for substituting the inorganic semiconductors, silicon dioxide insulator and the metals for organic materials. The low thermal budget and the high degree of mechanical flexibility open new opportunities to produce soft, lightweight, environmentally friendly and flexible thin films for electronics applications over a small, medium (sheet-to-sheet manufacturing) or large areas (roll-to-roll manufacturing) by using conventional printing technologies.

Among these, inkjet printing is a challenging and attractive technique due to its additive and contact-less processing that is leading a new paradigm in digital fabrication through the construction of electronic devices and circuits drop by drop. Moreover, the inherent flexibility of inkjet printing technology has significantly reduced the research time required from idea to proof-of-concept demonstration in a laboratory setting. Its low performance and low integration density are its principal handicaps but different production cost base capable of highly customized runs and small batch sizes facilitating disposable electronics.

The main objectives of this thesis work have been amply achieved, although some of the functional materials used cannot be considered optimal. This drawback is a limitation to manufacture devices with enough performance to implement successful electronic circuits. Nevertheless, this dissertation provides a set of contributions to the scientific and industrial communities to face the challenges associated with the manufacturing of all-inkjet microelectronic devices and circuits.

The amount of samples manufactured and analysed can be considered as an outstanding achievement that can be interesting from a scale-up point of view:

- A baseline inkjet printing process characterization to provide methodologies and design rules extraction in order to improve device performance, process reproducibility, and increasing yield thus allowing a more aggressive scaling down and higher integration density.
- The development of passive and active devices. The development of a suitable and simple manufacturing process for all-inkjet printed devices along with their physical and electrical characterization and the introduction of different strategies and approaches in order to improve devices.
- The static and dynamic characterization over time as well as statistical analysis on scalability and variability of devices. There is no literature in such analysis related to all-inkjet printed OTFTs. This Thesis is contributing to the State-of-the-Art on this topic.
- The development of simple circuits as a demonstration of the technology developed as well as an adaptive backend strategy for low-yield circuits as a solution to overcome one of the main drawbacks of inkjet printed devices, the low yield and variability due to printing effects.

This thesis dissertation explores these challenges and proposes methodologies, new topologies and a suitable and simple manufacturing process for all-inkjet printed devices and circuits. By using a reduced set of materials and processes, this thesis dissertation proposes new approaches that can be useful for the mail objective of this work: the successful fabrication of all-inkjet electronic circuits and systems.

More in detail, in Chapter 2, the dissertation has discussed the extraction and characterization of geometric design rules and the application of compensation techniques for inkjet manufacturing of reliable and precise OTFT structures from a morphological point of view to improve device performance, process reproducibility, and increasing yield thus allowing a more aggressive scaling down and higher integration density. Our contribution is a clear methodology to characterize the materials individually onto different substrates/layers to obtain optimal morphologies, for example, to source and drain electrodes. Also, a methodology to apply compensation techniques have been proposed to obtain minimum dimensions and improve shapes such as junctions and corners markedly deteriorated due to ink coalescence. This contribution [94] has received the 2014 Charles E. Ives Journal Award from the Society for Imaging Science & Technology[42].

In Chapter 3, we have reported about the manufacturing of passive electronic devices using fully S2S inkjet printing. We have developed manufacturing process operations for inkjet printing and post-treatment methods based on the evaluated materials. The focus was set on conductive lines, resistors and capacitors. Conductive lines were characterized as a first step

[42] IS&T – Society for Imaging Science & Technology – www.imaging.org

towards the fabrication of more complex devices. Based on these experiments, inorganic-based resistors were fabricated and characterized. Large quantities of resistors were fabricated to analyze yield, variability and reliability. Variability was considered excessive (~50%) despite the advantage of its simple manufacturing. From the experimental results of the inorganic resistors made by using semi-sintered silver nanoparticle ink, a rapid electrical sintering (RES) method has been demonstrated for the fabrication of fully inkjet printed programmable Write-Once-Read-Many (WORM) memories. Organic resistors made by using PEDOT:PSS as resistive materials and c-PVP as a barrier layer were also developed by using novel fabrication strategies to improve line homogeneity and reduced variability. Variability down to 8% was obtained. MIM capacitors have been implemented in this thesis work as a first step towards the fabrication of more complex devices as OTFTs. The deposition of the c-PVP was improved in order to obtain suitable electric devices in terms of dielectric strength, yield, variability and reliability. Nevertheless, the results in this thesis work show that the c-PVP ink still has several disadvantages. Although electrical characteristics are satisfying, film formation is very complex due to the strong coffee-ring effect and its low breakdown voltage limits its application. Additionally, large quantities of devices were manufactured in order to analyze the variability and scalability of the capacitors developed. An average parallel capacitance per area of 60 pF/mm^2 and yield of 80% were obtained. A simple low-pass RC circuit was presented with a cut-off frequency of 14 KHz to demonstrate that the all-inkjet organic capacitors and resistors can further find its application to the low-cost all-organic circuit industry.

In Chapter 4, we explored the fabrication process to obtain organic transistors in detail. A complete manufacturing process operation for inkjet printing including curing procedures has been developed based on the evaluated materials. Lab scale DMP2831 inkjet printing equipment from Fujifilm Dimatix was used as manufacturing system. The development of a suitable fabrication process obtained after large number of experiments, material evaluations and characterizations can be considered as an outstanding result. Several hundreds of fully inkjet-printed OTFTs were manufactured using the proposed recipe. All devices were fully characterized and we obtained dielectric thicknesses down to 380 nm and yields up to 78% for a fixed design.

In Chapter 5, several hundreds of OTFTs fabricated by S2S inkjet printing were characterized. These transistors have similar performances than both partly- and all-inkjet printed transistors published in the literature. The OTFTs fabricated and characterized displays values of μ around $2 \cdot 10^{-4}$ $cm^2/V \cdot s$, $I_{ON}/I_{OFF} \sim 10^2$, and V_T ranging from 0 to 8V, but they are all-inkjet printed, fabricated at room conditions and in large quantities. Concerning to the operational stability, we can consider OTFT highly stable in air conditions although

the devices suffer from gate-bias stress effects and non-linear I-V curves near the origin caused by series resistance effects due to the presence of traps. Intra-Foil (WID) variations of transistor parameters are a key to design and simulate organic full integrated circuits. The results suggest that Pelgrom's mismatch law is also valid for OTFTs. Larger devices exhibit less variation concerning the active area. The ingress of moisture into the organic semiconductor or presence of moisture at the interface with the gate dielectric is an important factor that degrades the bias-stress stability of many organic semiconductors not protected by a barrier layer. Nevertheless, we obtained OTFTs working up to 21 days.

In chapter 6, we have reported the development of strategies for the improvement of the inkjet-printed transistors. Three different improvement strategies were studied on the current chapter: (1) OTFT encapsulation strategies, (2) the improvement of functional layers deposition and (3) the optimization of OTFTs by design. We have demonstrated that using a MMAcoMAA coating layer improves the lifetime and I_{OFF} current in inkjet-printed transistors using a BG-BC topology. Related to layer improvement, it was clearly demonstrated that the gate dielectric thickness can be tuned through the design dimensions of the dielectric pattern area. This result provides a good methodology to improve the performance of the device due to this essential layer in active devices as transistors. The experiments made shows how the reduction of the OSC layer thickness results in a reduction of both I_{ON} and I_{OFF}. The reduction of I_{OFF} confirms the theory that the Off-current is partly created by the current flowing through the bulk as the electric field created because the gate is not being able to close completely the OSC channel due to the high thickness of the active layer. Finally, the approach to improve OTFTs by novel design geometries and topologies was also successful. Different approaches were studied changing design parameters, orientations and layer patterns in order to study the effect of those parameters on final transistor behaviour. A significant advantage was observed when narrower devices were used instead of the wider ones. Important results were also obtained in using non-overlapped devices. Main advantages were the reduction in gate-to-S/D capacitance and the increase of gate resistance thus reducing the gate leakage current despite the fact that they can suffer from lower yield due to misalignments.

Finally, in Chapter 7, the electrical characterization of an all-inkjet inverter has been presented. Static and Dynamic analysis shows working inverters but without enough performance to build more complex circuits when more than one single stage is required. A voltage gain ~ 2.3 and a maximum switching frequency of 126 Hz have been obtained with a maximum V_{DD} of 10V and V_{SS}=-15V. These results are similar than those that can be found in literature. Additionally, a Functional NAND2 logic gate has been demonstrated. Also, we have addressed the poor yield and high variability in Printed Electronics, which affects the

implementation of circuits, by developing a new methodology of circuit design and characterization. The methodology proposed is based on Standard Cells and reconfigurable OTFTs approach. Initially, the NAND2 OTFTs and matrix interconnections are unconnected being adaptive to the fabrication yield. Finally, the routing of OTFTs and matrix is done by inkjet printing.

Even if further investigations are required, this thesis dissertation is a contribution in the long way required for the scale-up of the all-inkjet printed technology. The different manufacturing strategies, characterization & improvement methodologies proposed and the large quantity of devices fabricated and analysed can be considered as an outstanding result of this thesis work.

8.2. Open Issues and Future Work

At the conclusions at the end of each chapter, there are few specific proposals for future work according to each specific topic presented in this thesis work. The future work in FOLAE technologies is huge and we still have a long way ahead. Nevertheless, the open issues related to the results developed in this thesis work give us a first impression to continue.

In Chapter 2, the main open issue is to apply the methodologies developed to other materials in the layer stack and the extraction of design rules in multilayer structures. A SW tool able to simulate the ink behaviour could speed up the advances in inkjet printing technology. Otherwise, experiments are time-consuming and labour-intensive.

In Chapter 3 and 4, the most important enhancement as future work should be the development of better materials to be used as resistive and dielectric layers. Major part of dielectric materials haven't been developed for this purpose, they use to be materials developed as coating layers and reused for a new market. This important drawback is delaying the take-off of the all-inkjet FOLAE technology. Also, inks need to be developed for a specific inkjet printheads in order to improve its ejection and deposition. Inks that "can be jetted" are complex to use and their results do not have high reproducibility.

In Chapter 5, as future work, the main target is to reduce the thickness of the active semiconductor channel thus reducing the Off-current and improving the On/Off current ratio needed to build successful circuits. Also, by using better and thinner dielectrics the interface dielectric-OSC will improve thus reducing the number of traps what will let to better OTFT performance at lower voltage. Barrier layers or the use of Top Gate configuration can help improving the lifetime and reliability of devices.

In Chapter 6, as future research, there's still a lot of room in vertical, self-aligned OTFT or dual-gate topologies among others. New layouts as the ones to reduce fringing effects were started when this thesis dissertation was already written.

Finally, in Chapter 7, the manufacturing of an all-inkjet Ring Oscillator is still an unsolved challenge in the literature. This is a required step for the future development of more complex circuits. A lot of efforts need to be dedicated basically by improving materials and processes.

This is the remaining drawback of the current FOLAE technologies. From the "electronic engineering" point of view, new topologies and geometries can help but cannot solve the important drawbacks related to materials and processes. Nevertheless, some first steps in the long way to the fabrication of all-inkjet organic electronic circuits can contribute to wake up the interest of the industry thus speeding up the grow of a future FOLAE market.

ANNEXES

Annex A. References

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Annex B. Author relevant publications

Journal publications

[1] **Eloi Ramon**, Carme Martínez-Domingo, Jordi Carrabina, "Geometric Design & Compensation Rules Generation and Characterization for all-Inkjet Printed Organic Thin Film Transistors", Journal of Imaging Science and Technology (doi: 10.2352/J.ImagingSci.Technol.2013.57.4.040402.), Volume 57, 4, 2013, 40402-1.

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Conference proceedings

[4] **Eloi Ramon**, Carme Martínez-Domingo, Ana Alcalde-Aragonés, Adrià Conde, Jofre Pallarès, Lluís Terés, Jordi Carrabina, "Large-scale fabrication of all-inkjet printed organic thin film transistors: a quantitative study", 30th International Conference on Digital Printing Technologies and Digital Fabrication 2014, Philadelphia (USA) 2014.

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[20] Jordi Mujal, **Eloi Ramon**, Jordi Carrabina, "Methodology and Tools for Inkjet Process Abstraction for the Design of Flexible and Organic Electronics", International Symposium on FLEXIBLE ELECTRONICS 2010 (ISFE'10), Palma de Mallorca.

[21] A.González-Álvarez, L.Francesch, L. López, **E. Ramon**, J. Mujal, J. Carrabina, "Printed Electronics aplicada al desarrollo de dispositivos flexibles", Proceedings of XI Congreso Nacional de Materiales 2010, Zaragoza.

Poster presentations

[22] Enrico Sowade, **Eloi Ramon**, Kalyan Yoti Mitra, Fulvia Villani, Rocco Kundt, Tino Petsch, Henrique L. Gomes, Lluis Teres Teres, Jordi Carrabina, Reinhard R. Baumann, "Manufacturing of electronic devices using laboratory inkjet printing and basic approaches towards industrial up-scaling", Poster at LOPE-C, 6th International Conference and Exhibition for the Organic and Printed Electronics Industry 2013, Munchen (Germany), June 2013.

[23] Carme Martínez-Domingo, **Eloi Ramon**, Ana Alcalde-Aragonés, Jordi Carrabina, "Inkjet Geometric Design Rules Generation and Characterization", Poster, LOPE-C, 20-21 June 2012, Munich.

[24] **Eloi Ramon**, Jordi Mujal, Jordi Carrabina, Laia Francesch, Laura López, Cristina Casellas, Raul Fernández, Ignasi Gil, "Inkjet Printed Organic RF Structures", Poster at Plastic Electronics Europe 2009, Dresden (Germany).

Other papers were technology developed during the thesis has been used but results are not included in thesis dissertation:

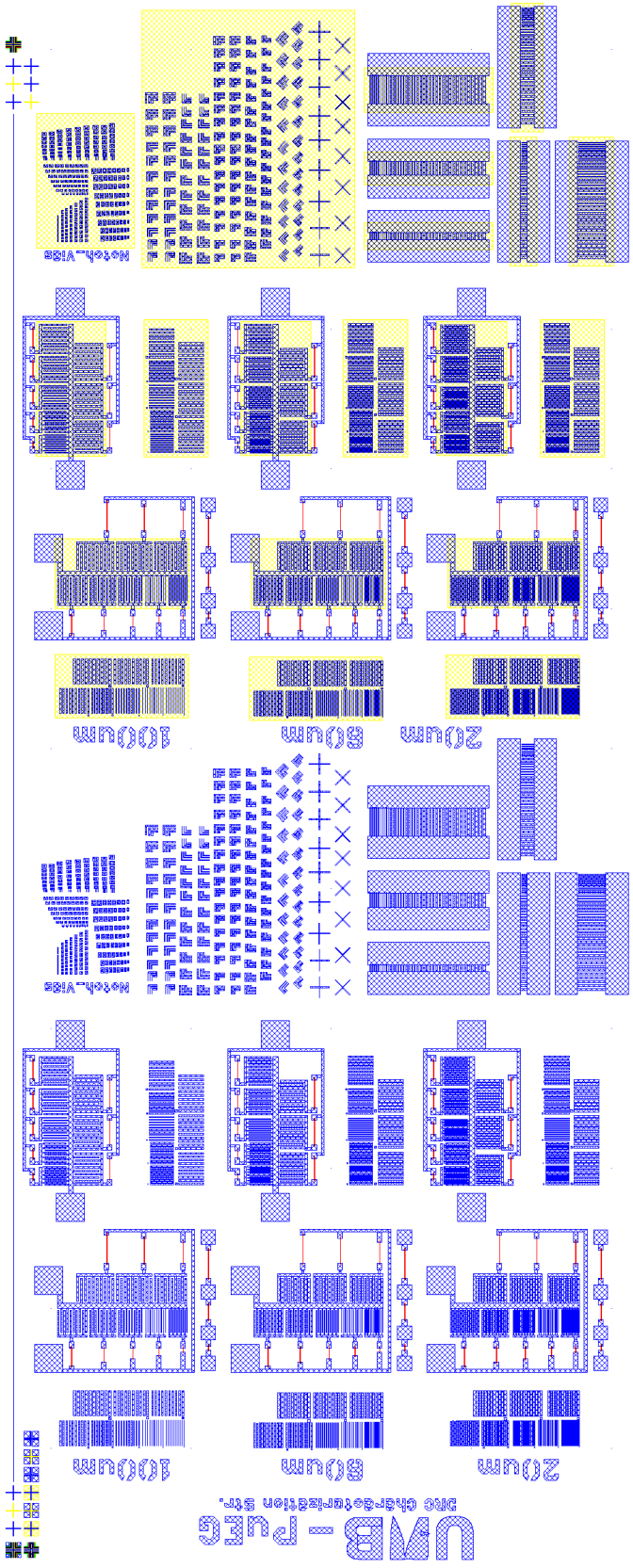
[25] M. Medina-Sánchez, C. Martínez-Domingo, **E. Ramon**, S. Miserere, A. Alcalde-Aragonés, J. Carrabina & A. Merkoçi , "Ink-jet printed FET for biosensing applications", Proceedings of microTAS 2012, Okinawa (Japan)

[26] Ana Alcalde-Aragonés, **Eloi Ramon**, Mariana Medina-Sánchez, Carme Martínez-Domingo, Sandrine Miserere, Arben Merkoçi and Jordi Carrabina, "New materials for biosensing", Poster at ISFOE 2012, Thessaloniki (Greece), July 2012.

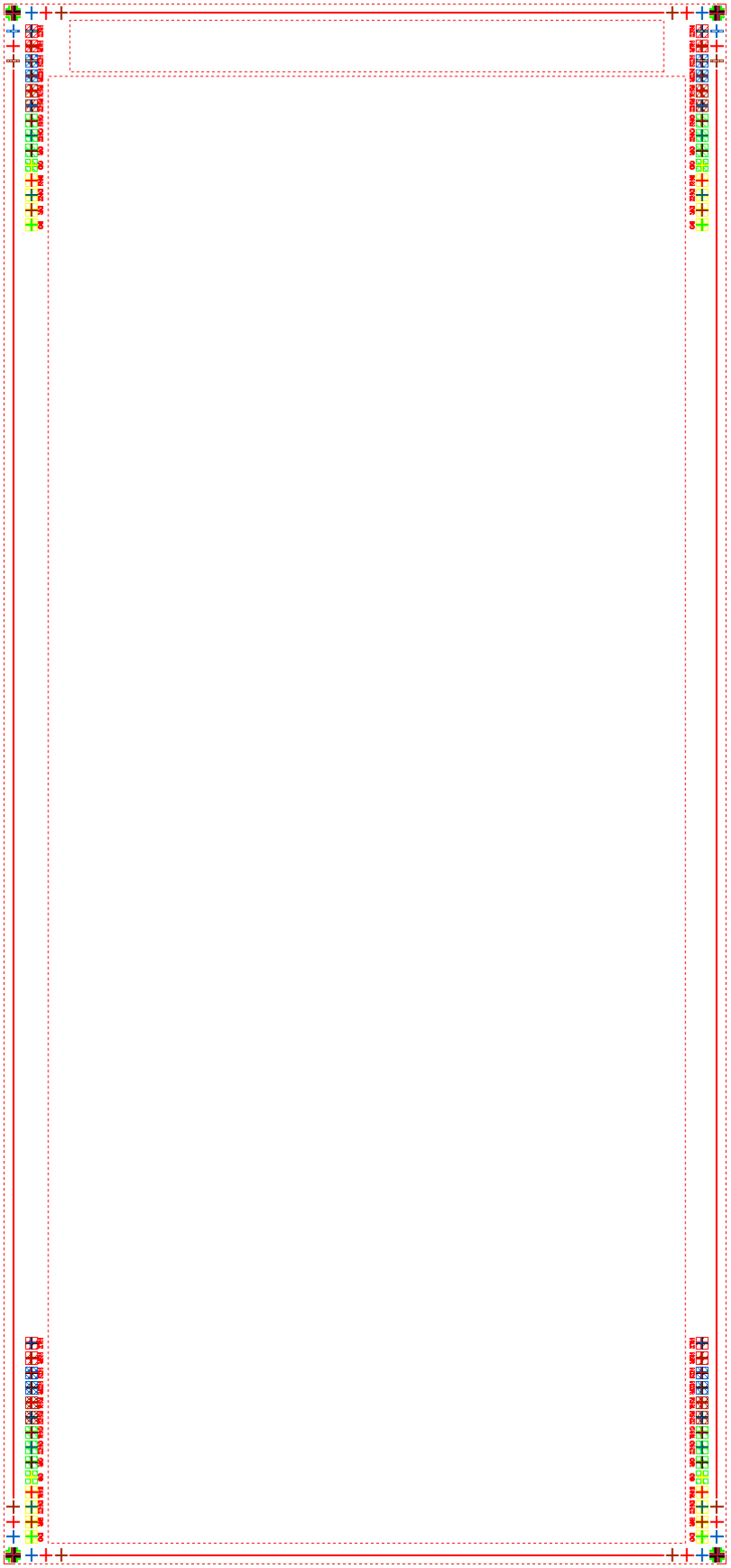
[27] Mariana Medina-Sánchez, **Eloi Ramon**, Ana Alcalde-Aragonés, Sandrine Miserere, Carme Martínez-Domingo, Jordi Carrabina, Arben Merkoçi, "Ink-jet printed FET for biosensing applications", Poster at Biosensors 2012, Cancun (Mexico).

Annex C. Layouts

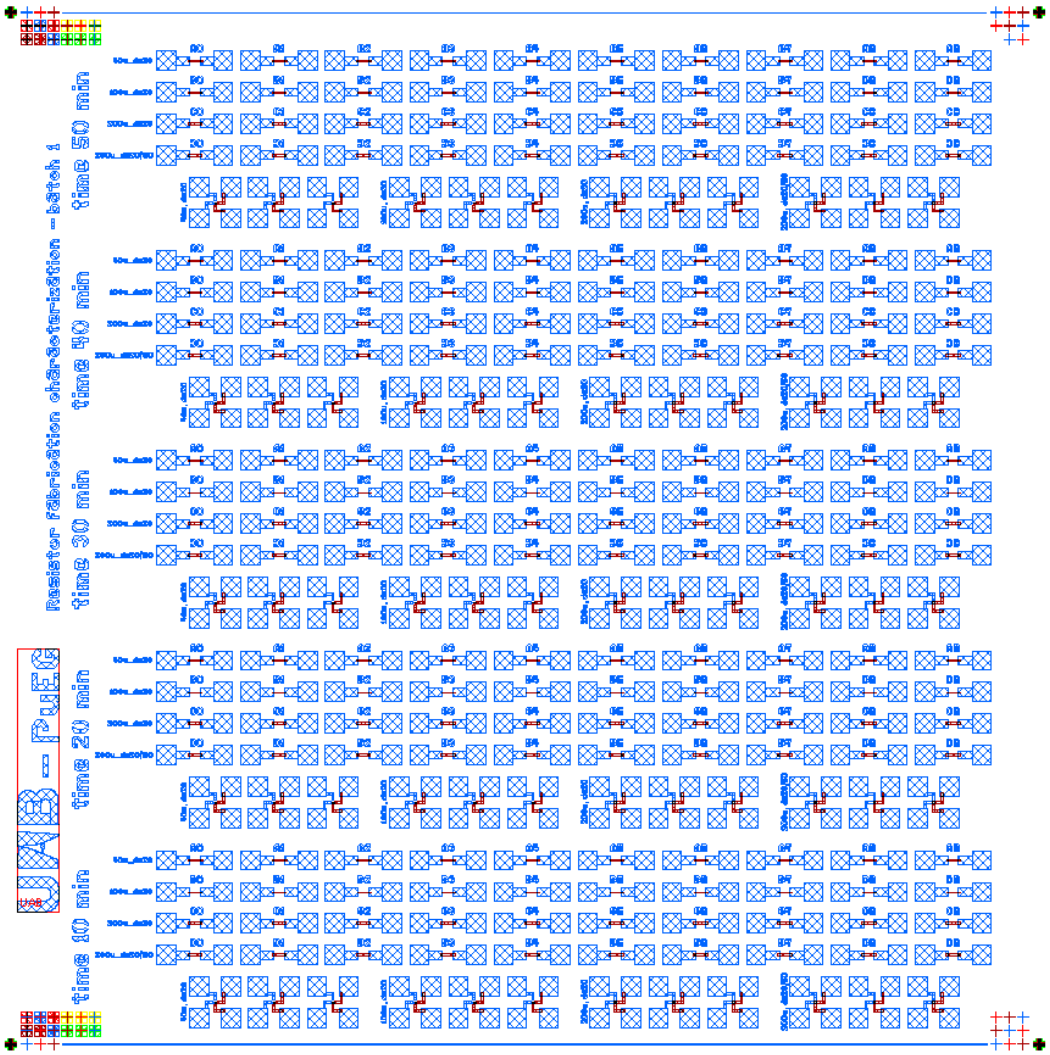
C.1. Layout for ink characterization on substrate and insulator.



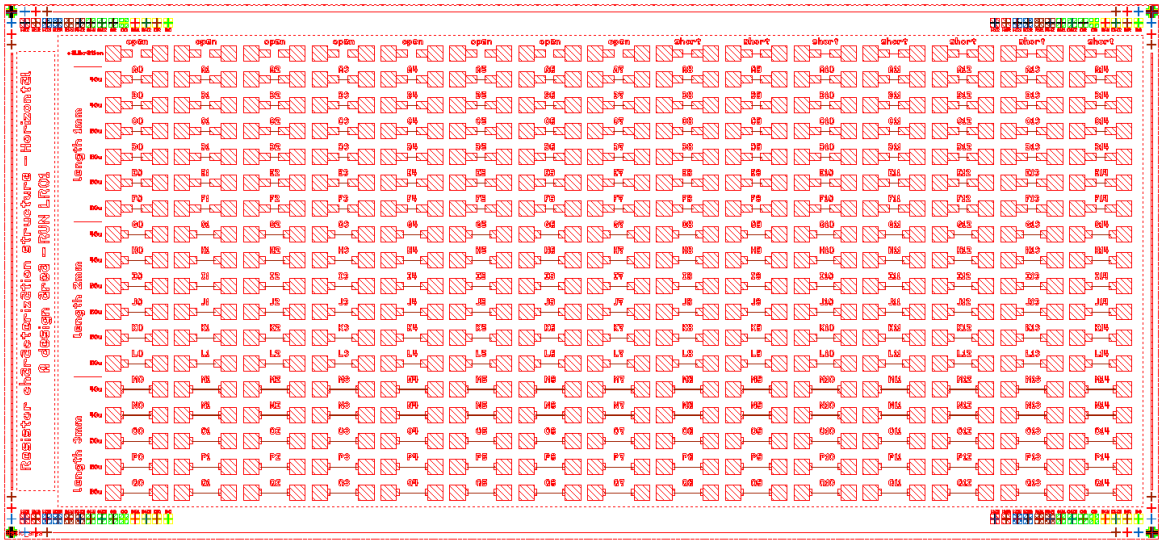
C.2. Test mask for pattern and overlay.

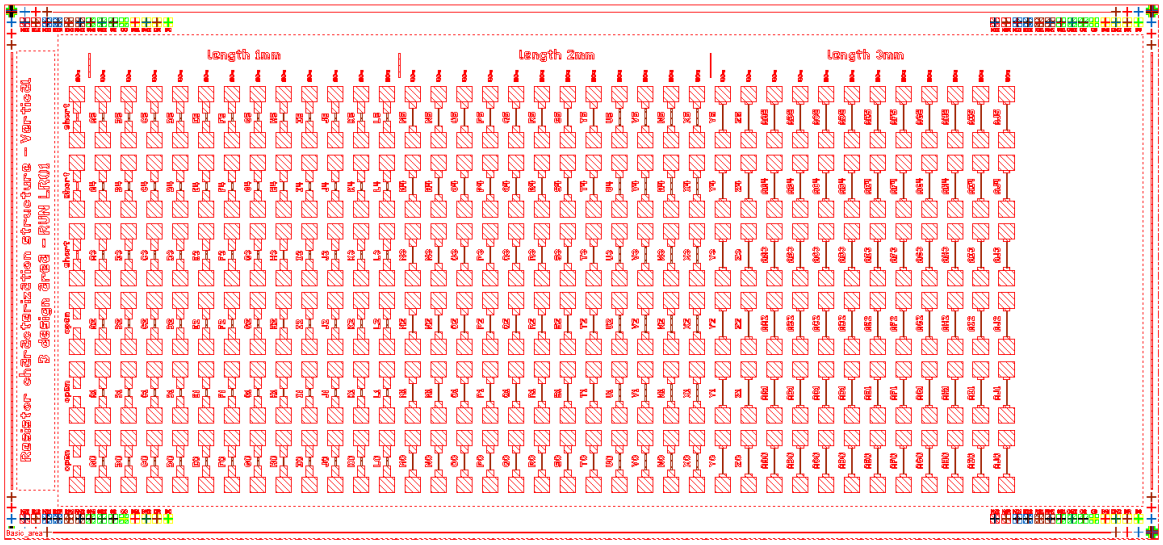


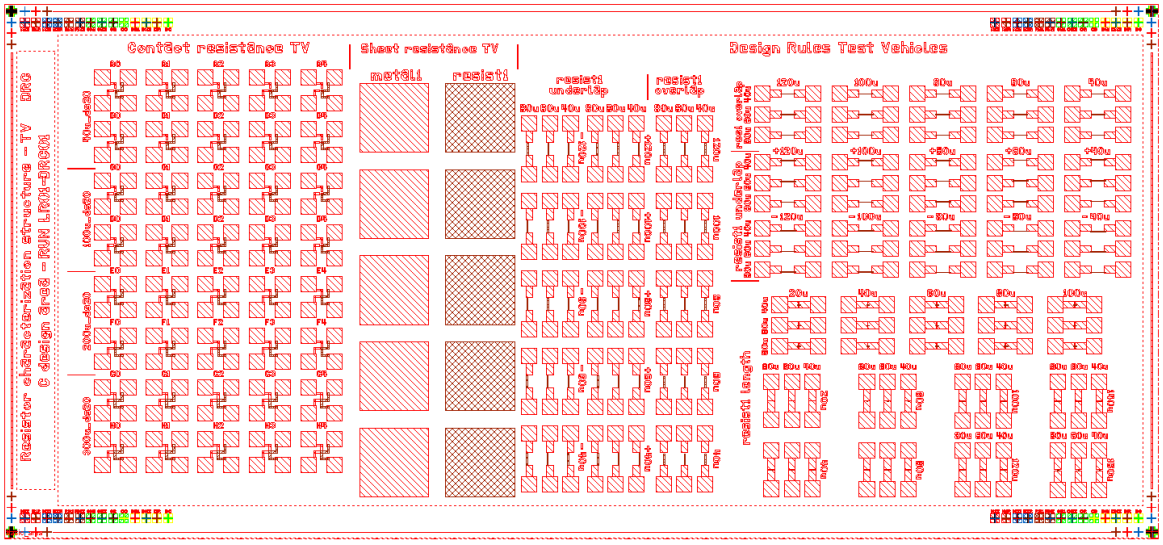
C.3. Resistor characterization layout.



C.4. Resistor characterization layout (linear resistors)

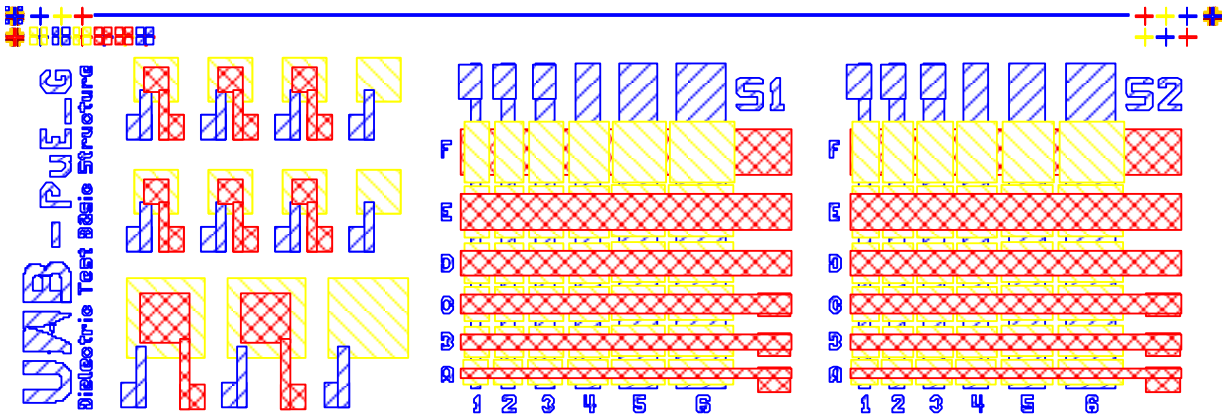




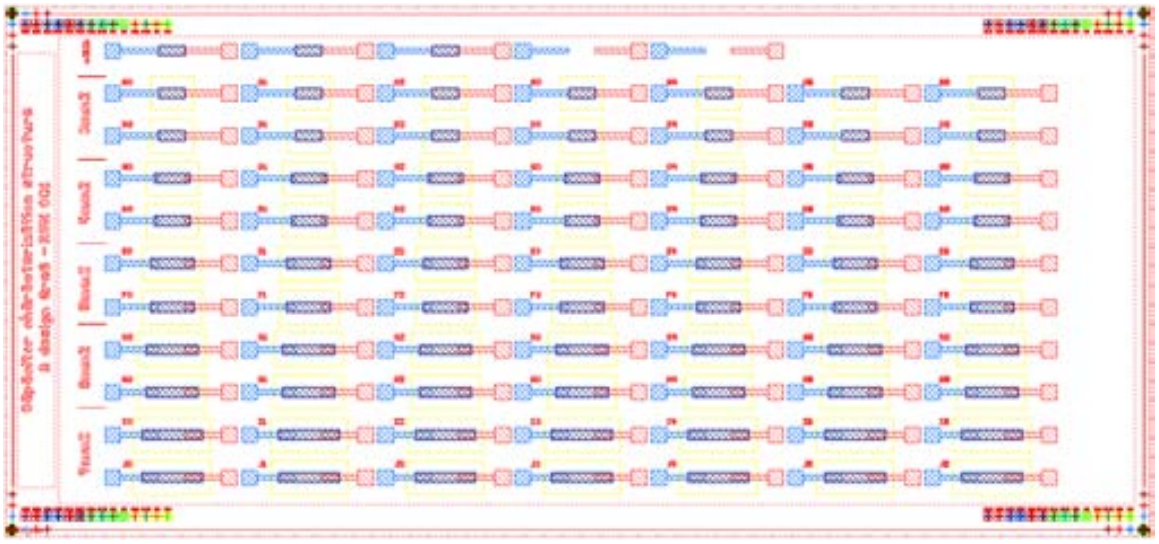


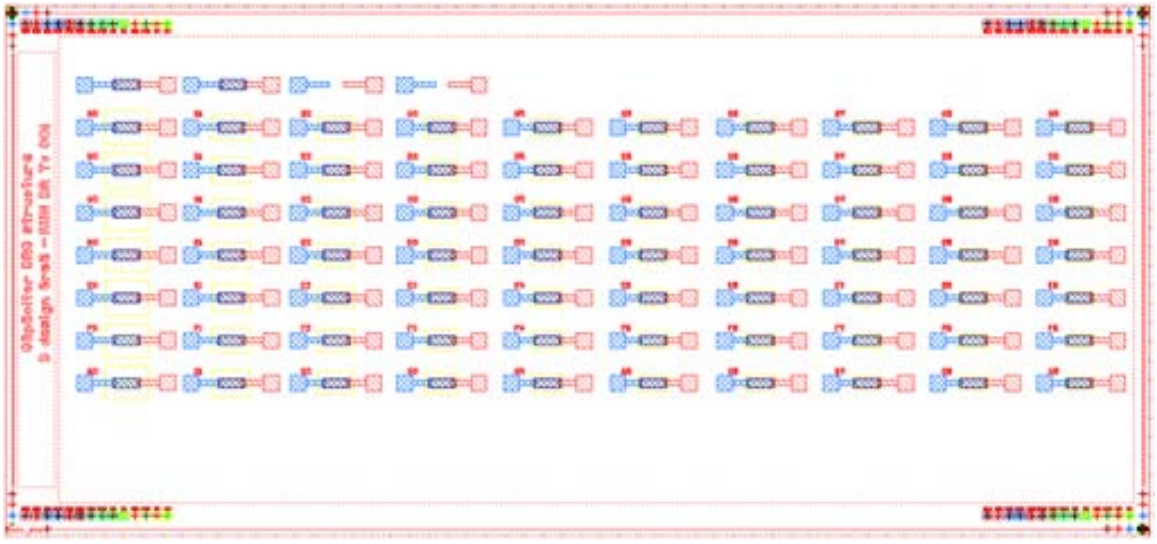
C.5. Resistor characterization layout (snake resistors)

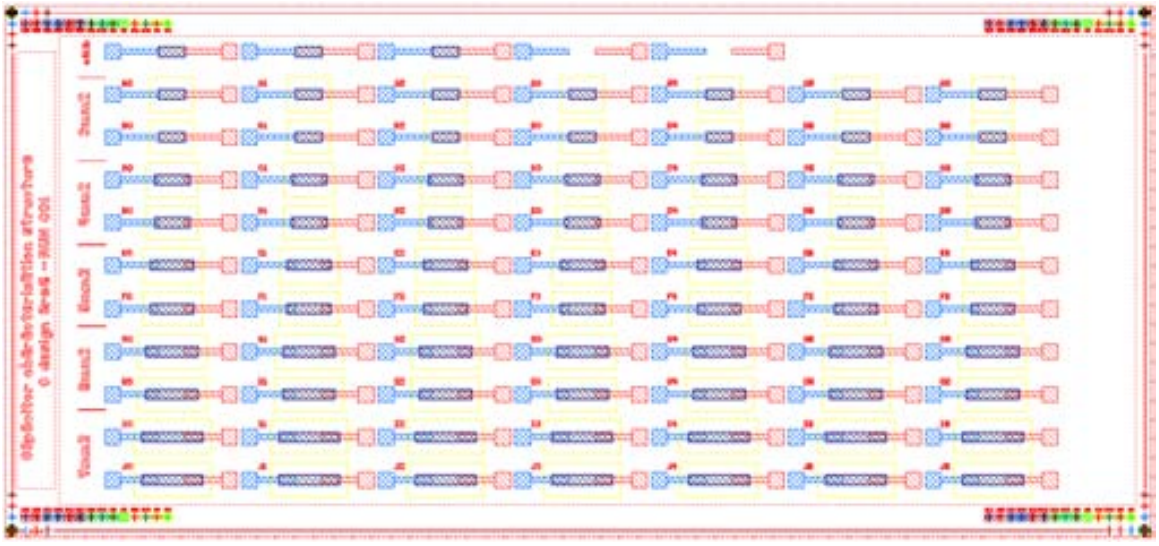
C.6. Capacitor characterization layout



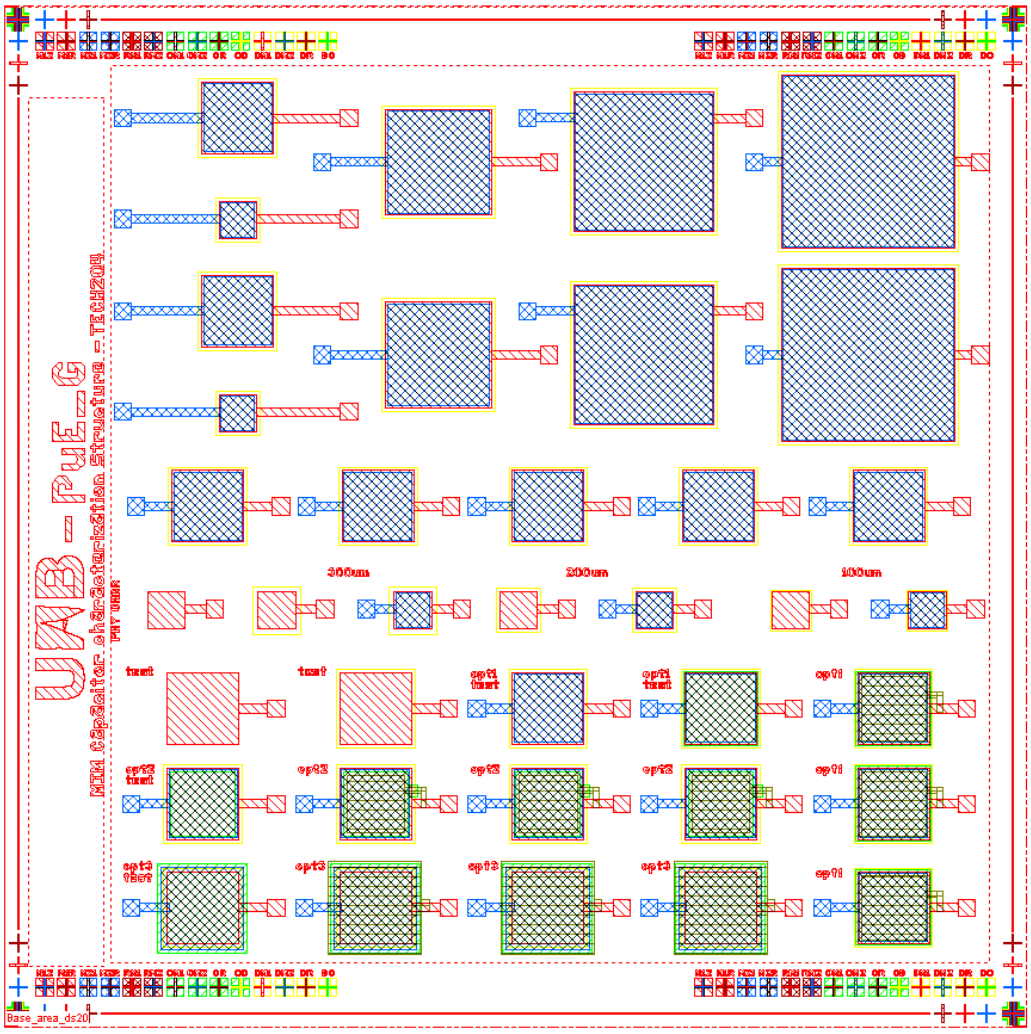
C.7. Capacitors characterization layout.



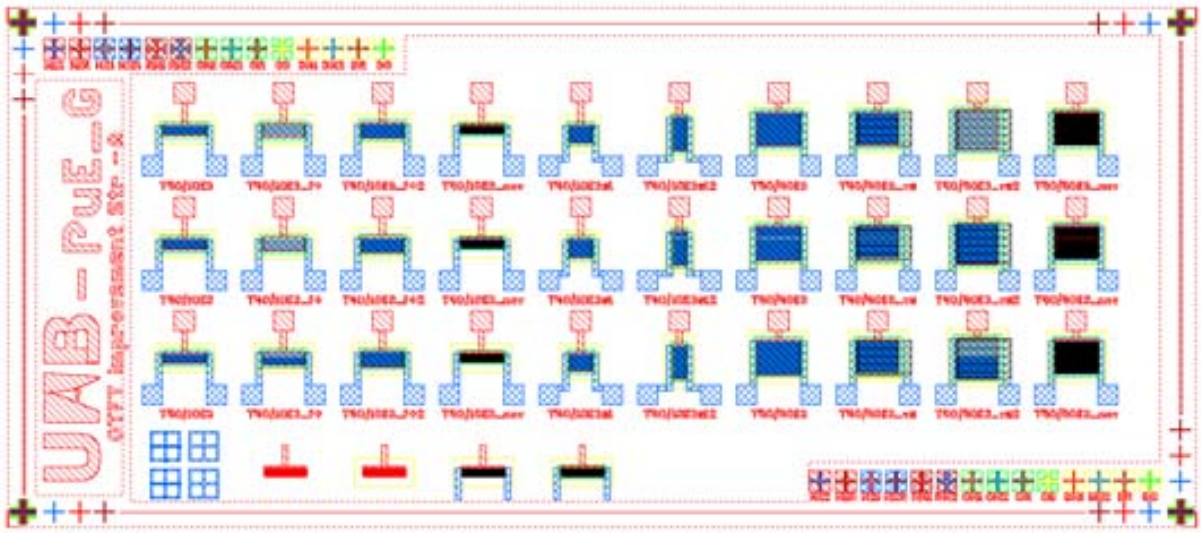




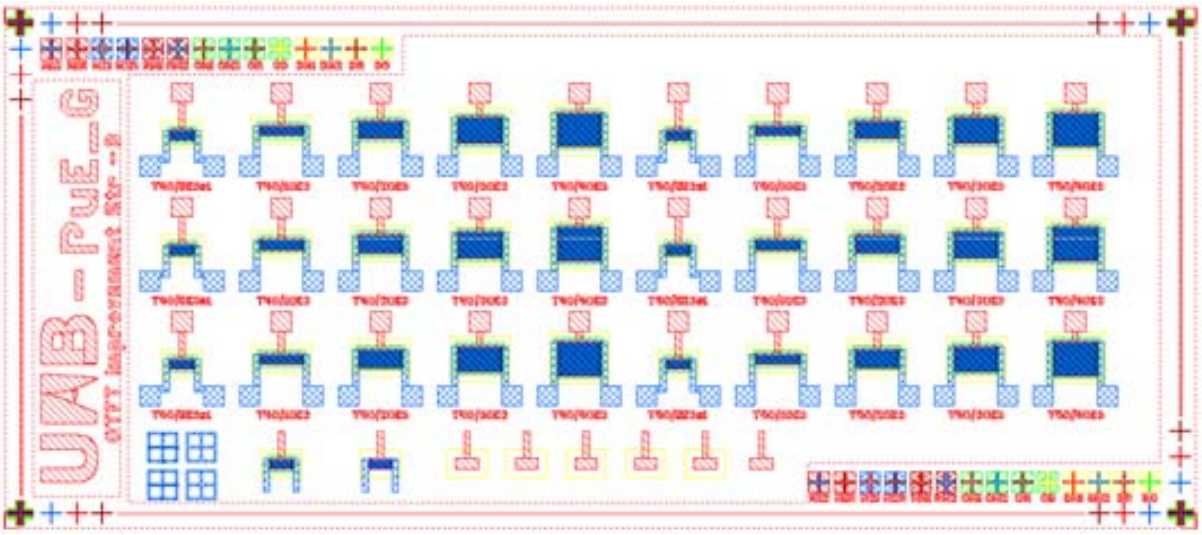
C.8. Small capacitor characterization layout.



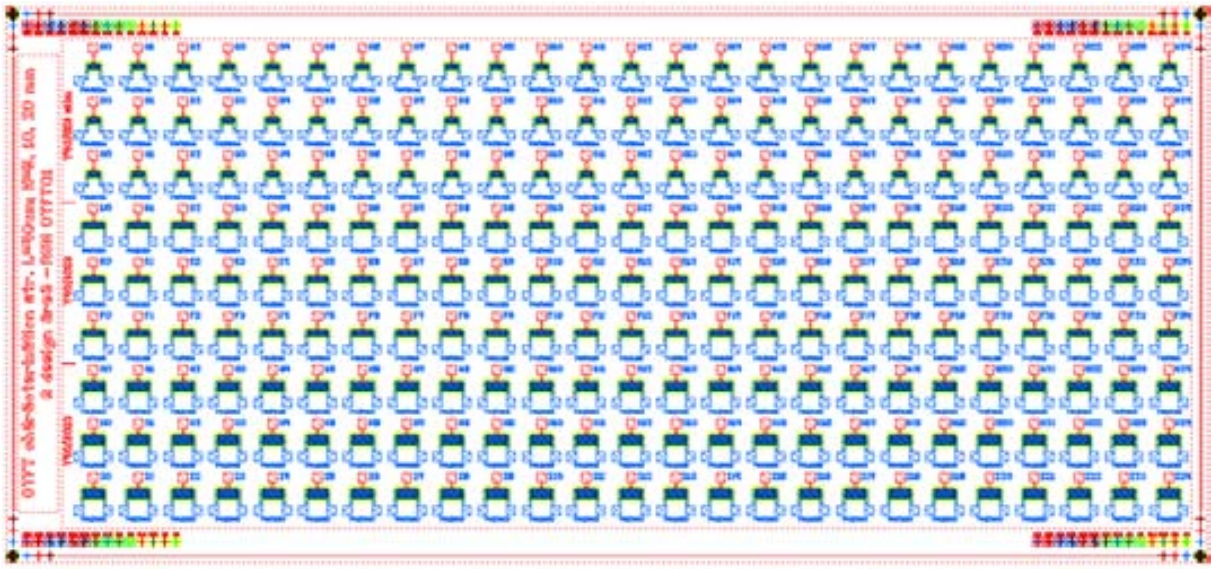
C.9. Layout of OTFT characterization structure (fx118)

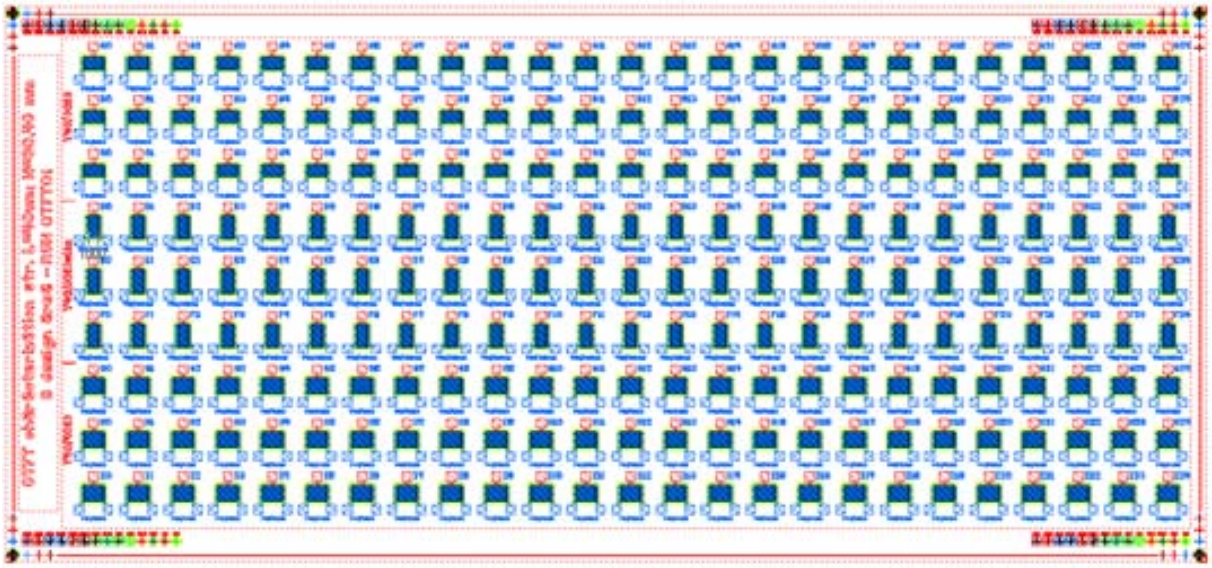


C.10. Layout of OTFT characterization structure (fx119)

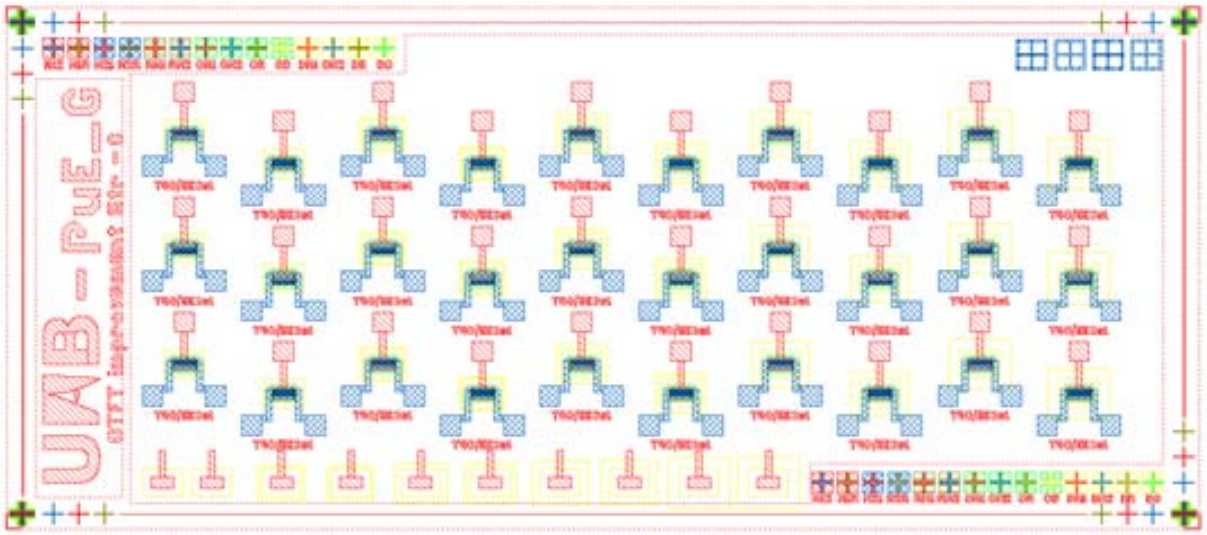


C.11. OTFT01 design

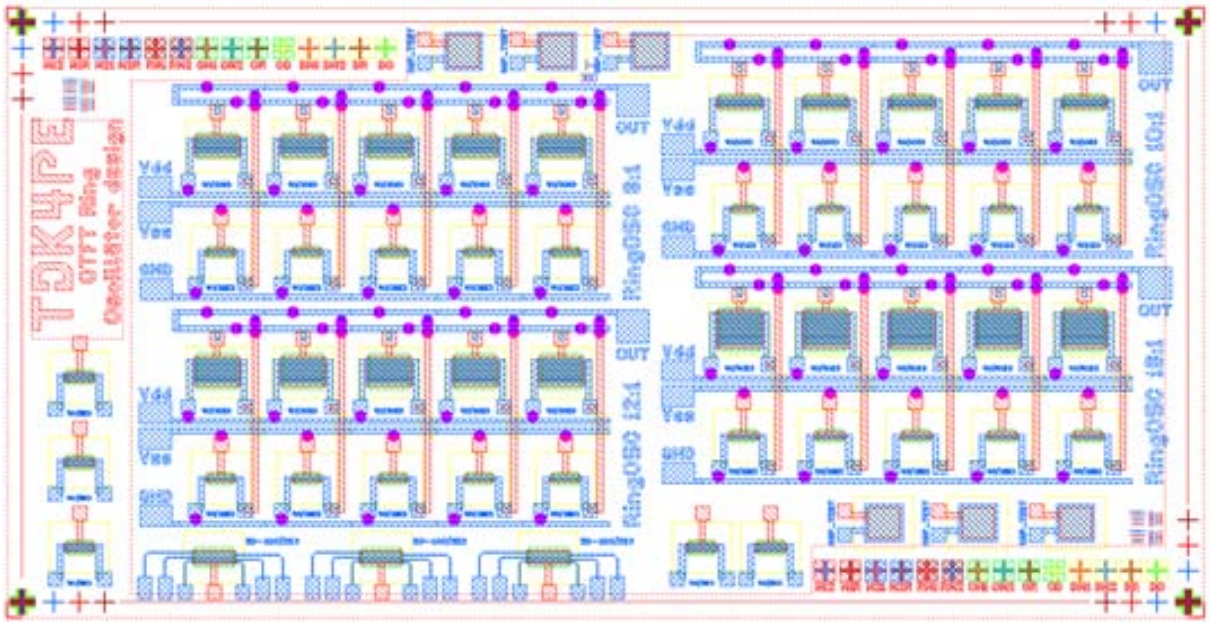




C.12. Dielectric thickness variation



C.13. Inverter / NAND2 Characterization structure



Note: Pink dots represent unconnected contacts depending on the individual characterization of each device. First, we characterized each OTFT individually to select which inverters were suitable to build a ring oscillator.

Annex D. DuPont Teijin Teonex® Q65FA specifications

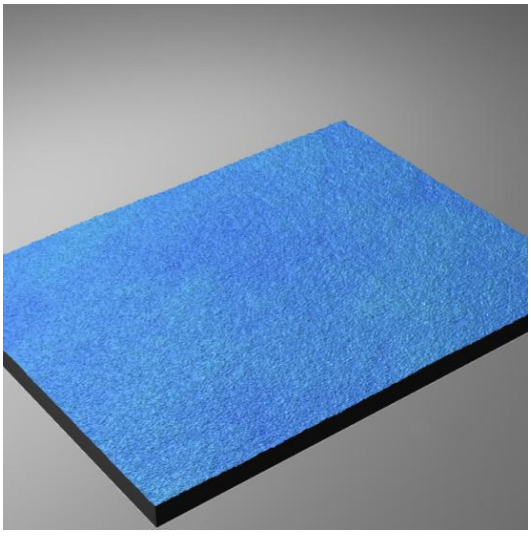
Illustrative Planarised Teonex ® PEN Performance Data

Property	Test Method	Unit	Value
General			
Polyester film thickness		microns	125
Thermal			
Melting point	BS2782	°C	269
Coefficient of thermal expansion (betw een 20 and 50°C)		cm/cm deg C	19 x 10^{-6} (MD)
Residual Shrinkage (after 30mins at 150°C)	DTF Method	%	MD* 0.09 TD** 0.08
Residual Shrinkage (after 30mins at 180°C)	DTF Method	%	MD* 0.21 TD** 0.20
Optical			
Haze	ASTM D 1003-78 (measured on Gardner Hazemeter)	%	0.9 +/- 0.3
Total Light Transmission	ASTM D1003-77 (measured on Gardner Hazemeter)	%	90.5 +/- 1
Yellowness Index	ASTM D1925		7.78
Physical			
Adhesion	ASTM F2296-04 (crosshatch using TESA 4104 tape)	-	100% PASS
Mean Surface Roughness (Ra)	White Light Interferometry	nm	0.41
Abrasion Resistance	ASTM D1044	%	1.4 +/- 0.5
Pencil Hardness	ASTM D3363-05	-	3H
Water Vapour Transmission Rate	Lyssy 38°C / 90% rh	g/m^2/day	1.3
Oxygen Tranmission Rate	Oxtran 23°C / 60-70% rh	cc/m^2/day	0.07
Mechanical			
Tensile strength at break	ASTM D 882	kgf/mm^2	MD 17 TD 18
Elongation at break	ASTM D 882-83	%	MD 90 TD 80
Youngs Modulus	ASTM D 882	kgf/mm^2	MD 470 TD 475

1 micron = 0.001 mm approx. 4 gauge, *MD = Machine Direction, **TD = Transverse Direction

White Light Interferometry
Image of Planarised Surface
400 x 600 micron

Mean R_a = 0.41 nm



Annex E. OTFT printing recipe

The technical specifications of each ink are described as Supporting Information.

A. Deposition of the bottom gate and S/D electrodes

Prior to printing, the substrate (PEN foil 125 µm thickness) is cleaned with ethanol for a few seconds, and then dried under nitrogen to remove any remaining particles.

The bottom gate is deposited onto the substrate by inkjet printing of a silver nanoparticle solution. Prior to start, the ink is filtered by using a Nylon base (PTFE filters) filter with a pore size of 0.2 µm (Sigma Aldrich). The cartridge and platen temperature is set at room temperature and 40ºC respectively. The S/D electrodes are deposited onto the dielectric layer. Prior to start, the ink is filtered by using a Nylon base (PTFE filters) filter with a pore size of 0.45 µm (Sigma Aldrich). The cartridge and platen temperature is set at room temperature and 60ºC respectively. Drop spacing of 20 µm by using a 10 pL cartridge is established, and the jetting frequency and voltage is 10 KHz and around 22-23 V each. The resulting layer is sintered at 130 ºC for 30 min in a convection oven.

Silver nanoparticle ink from Sunchemical - http://www.sunchemical.com/product/suntronic/

Silver Nanoparticle Ink Suntronic EMD-5603	
Characteristics	**Description**
Form	*Dispersion*
Concentration	*20 wt. % dispersion in organic solvent (ethanol and ethanediol)*
Volume resistivity	*5-30 µΩ·cm, after annealing @ 150-300 °C*
Particle size	*<150 nm (DLS)*
Surface tension	*28.0-31.0 mN m^{-1}*
Viscosity	*10-13 cP*
Inkjet Printer Parameters	
Characteristics	**Description**
Substrate pretreatment	*None*
Cartridge temperature	*Room temperature*
Platen temperature	*40°C for gate layer, 60°C for Source/Drain layer*
Drop spacing	*20 µm*
Nozzle size	*10 pL drop volumes (Orifice size silicon nozzle of 21.5 µm)*
Frequency	*10 KHz*
Voltage	*22-23V*
Curing temperature	*130°C @ 30 min oven*

B. Deposition of the bottom insulator

Cross-linked PVP (Poly(vinyl phenol), Aldrich, Mw=25000) is prepared by dissolving PVP in PGMEA (propylene glycol monomethyl ether acetate)(Aldrich) at room temperature.

The resulting solution is stirred for 30 min and, to obtain c-PVP with the desired properties for jetting is subsequently filtered (PVDF (polyvinylidene difluoride) 0.45µm filter). The bottom insulator is deposited by inkjet printing of the previously prepared c-PVP solution at room temperature (cartridge and platen), with a drop spacing of 20 µm by using also a 10 pL cartridge, being the jetting frequency and voltage 10 KHz and around 23-26 V respectively.

The exact recipe for the cPVP is confidential. The composition of this material was given from ENEA-Portici Research Center (Dr. Fulvia Villani).

- PVP: http://www.sigmaaldrich.com/catalog/product/aldrich/436224?lang=es&region=ES

-PGMEA (solvent): http://www.sigmaaldrich.com/catalog/product/sial/484431?lang=es&region=ES

c-PVP Dielectric Ink	
Characteristics	**Description**
Form	*Crosslinked polymer*
Concentration	*Confidential*
Dielectric strength	*0.3 MV/cm*
Particle size	-
Surface tension	*Confidential. This information is provided from EU FP7 TFK4PE project partners.*
Viscosity	*4.78 cP*
Inkjet Printer Parameters	
Characteristics	**Description**
Substrate pretreatment	*None*
Cartridge temperature	*Room temperature*
Platen temperature	*Room temperature*
Drop spacing	*20 µm*
Nozzle size	*10 pL drop volumes (Orifice size silicon nozzle of 21.5 µm)*
Frequency	*10 KHz*
Voltage	*23-26V*
Curing temperature	*200°C @ 20 min convection oven*

C. Deposition of the semiconductor

Before deposition of the semiconductor, the source and drain electrodes layer is plasma-treated (O_2, 60%, 25 W) for 30 sec, and then cured on a hot plate for 15 min at 120 ºC. The semiconductive material is based on amorphous polymer FS0027 provided by Flexink and dissolved in tetralin (4 % proportion). The semiconductor layer is deposited onto the plasma-treated layer by inkjet printing, at room temperature (cartridge and platen), with a drop spacing of 25 µm by using also a 10 pL cartridge. The jetting frequency and voltage is 10 KHz and around 12-14 V each.

FS0027 Semiconductive Ink	
Characteristics	**Description**
Form	*Amorphous polymer*
Concentration	*Dissolved in tetralin (4 %)*
Volume resistivity	*340 ± 60 MΩ*
Particle size	-
Surface tension	*35.24 mN m^{-1}*
Viscosity	*3.96 cP at 25ºC*
Inkjet Printer Parameters	
Characteristics	**Description**
Substrate pretreatment	*Oxygen plasma 25W during 30 seconds*
Cartridge temperature	*Room temperature*
Platen temperature	*Room temperature*
Drop spacing	*25 µm*
Nozzle size	*10 pL drop volumes (Orifice size silicon nozzle of 21.5 µm)*
Frequency	*10 KHz*
Voltage	*12-14 V*
Curing temperature	*120ºC during 60 minutes oven or 120ºC during 15 minutes hot plate*