Regular Cell Design Approach Considering Lithography-Induced Process Variations

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Short abstract: The deployment delays for EUVL, forces IC design to continue using 193nm wavelength lithography with innovative and costly techniques in order to faithfully print sub-wavelength features and combat lithography induced process variations. The main objective of this dissertation lies in the proposal of regular litho-friendly layout design styles, referred as Adaptive Lithography Aware Regular Cell Designs (ALARCs), in order to combat these printability variations in advanced technology nodes while at the same time reducing manufacturing costs. This thesis also proposes a layout quality metric (LQM) which considering several metrics, including a lithography parametric yield estimation model, provides a single score to globally evaluate and compare the regular layout designs proposed with traditional 2D standard cell designs. The layout evaluation of several benchmark circuits shows that regular layouts can outperform other 2D standard cell design implementations.

Keywords: Design for manufacturability, layout regularity, lithography printability, layout evaluation, systematic parametric yield.

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Abstract

Upcoming technology node shrinking is becoming more and more challenging due to lithography tools are being pushed to operate at their resolution limit. Due to a number of technical reasons, the light wavelength is very hard to scale down, being currently and for the next CMOS generations fixed at 193nm. The deployment delays for extreme ultraviolet (EUV) lithography (13nm), is forcing IC design to continue using 193nm immersion lithography with innovative and costly techniques in order to faithfully print sub-wavelength features.

The effect of the lithography gap in current and upcoming technologies is to cause severe distortions due to optical diffraction in the printed patterns and thus degrading manufacturing yield. Using 193-nm lithography with double patterning and the increasing number of process variations forces chip makers to use more restrictive design rules. Therefore, a paradigm shift in layout design is mandatory towards more regular litho-friendly cell designs in order to combat lithography induced process variations.

Regular litho-friendly layout design styles are being proposed to obtain faithfully printed feature sizes much smaller than the light wavelength. It is largely demonstrated in the literature, the manufacturability benefits of employing regular litho-friendly layout features at the expense of area penalty. However, it is still unclear the amount of layout regularity that can be introduced and how to measure the benefits of a regular implementation with respect to a standard cell design.

This dissertation is focused on searching the degree of layout regularity necessary to combat lithography variability and outperform the layout quality of a design. The four main contributions that have been addressed to accomplish this objective are: (1) the definition of several layout design guidelines to mitigate lithography variability on IC designs; (2) the proposal of a parametric yield estimation model to evaluate the lithography impact on layout design; (3) the development of a global Layout Quality Metric (LQM) including a Regularity Metric (RM) to capture the degree of layout regularity of a layout implementation and; (4) the creation of different layout architectures exploiting the benefits of layout regularity to outperform line-pattern resolution, referred as Adaptive Lithography Aware Regular Cell (ALARC) Designs.

The first part of this thesis provides several regular layout design guidelines derived from lithography simulations so that several important lithography related variation sources are minimized. The lithography imperfections have a direct impact on transistor channel length of devices and even for regular designs, the gate length must be appropriately configured to not jeopardize the electrical characteristics of a cell design. A design level methodology, referred as gate biasing, is proposed to overcome systematic layout dependent variations, across-field variations and the non-rectilinear gate effect (NRG) applied to regular fabrics by properly configuring the drawn transistor channel length. The gate biasing technique is applied to an AND2 logic gate and delay and power evaluation is performed to illustrate the impact of lithography variations on layout design.

The main objective of the second part of this dissertation is to present a lithography yield estimation model to predict the amount of lithography distortion expected in a printed layout due to lithography hotspots. An efficient lithography hotspot framework to identify the

different layout pattern configurations, simplify them to ease the pattern analysis and classify them according to the lithography degradation predicted using lithography simulations is presented. The lithography hotspot classification and the pattern simplification are key aspects of the framework so the lithography distortion can be captured with a reduced set of lithography simulations. The yield model is calibrated with delay measurements of a reduced set of identical test circuits implemented in a CMOS 40nm technology and thus actual silicon data is utilized to obtain a more realistic yield estimation. The application of the yield model is demonstrated for different layout configurations showing that a certain degree of layout regularity improves the manufacturing yield and increases the number of good dies per wafer.

The third part of this thesis presents a configurable Layout Quality Metric (LQM) that considering several layout aspects provides a global evaluation of a layout design with a single score. The LQM can be leveraged by assigning different weights to each evaluation metric or by modifying the parameters under analysis. The LQM is here employed following two different sets of partial metrics. The (LQM-S) employs simple measurements to give a preliminary analysis of a layout design and the (LQM-E) considers more elaborated measurements to provide a more detailed analysis of the benefits and weaknesses of a design. Note that both sets of measurements include a regularity metric, RM, (a simplified version in the LQM-S and a more precise version in the LQM-E) in order to capture the usage of litho-friendly regular patterns and thus it captures the degree of layout regularity applied in a layout implementation.

Lastly, this thesis presents the Adaptive Lithography Aware Regular Cell (ALARC) templates proposed to outperform 2D standard cell designs for advanced technology nodes. Different ALARC proposals using different degrees of layout regularity and different area overheads are provided. Several cell layout libraries for a 40nm technology node are automatically created to evaluate the regular templates proposed.

The quality of the gridded regular templates is demonstrated by automatically creating a library containing 266 cells including combinational and sequential cells and synthesizing several ITC'99 benchmark circuits. Area, lithographic yield, pattern complexity, wire-length, electrical characterization and other parameters are employed to evaluate the different designs. Furthermore, the LQM is employed to provide a single-score to evaluate the different proposals. Note that the regular cell libraries only present a 9% area penalty compared to the 2D standard cell designs used for comparison and thus providing area efficient designs. The evaluation of the libraries and circuits using the LQM-E shows that regular layouts can be competitive compared to 2D standard cell designs depending on the layout implementation since the best regular design, the BHF1 with a regularity index of 97.5%, outperforms other 2D designs, the F2D and the BMF2.

Dedicated to my beloved ones.

1

Introduction

Higher device density circuits with enhanced performance, but with reduced cost per transistor has been the driving motivation for the semiconductor industry to continue the technology node shrinking for very large scale integrated circuits (VLSI) with advanced lithography. This non stoppable scaling, while posed to continue according to the ITRS roadmap [1] is becoming more and more challenging due to increasing process variations occurring in IC manufacturing. One source of process variations is the impact of layout dependent effects (LDE) variability [2] on designs coming mainly from lithography imperfections resulting in the degradation of printed layout patterns. Hence, the employment of purely unidirectional patterns will become mandatory for future technology nodes in order to maintain pattern fidelity. In summary, the challenges in advanced IC designs to combat the increasing number of process variations, especially those related to lithography distortion, and the need to change the IC traditional layout design style towards more regular litho-friendly designs are provided in this chapter. Lastly, a detailed description of the main research goals pursued throughout this dissertation is provided.

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1.1 Motivation

Over the years, CMOS technology has not ceased to scale down and has enabled the production of increasingly complex products at lower cost. However, technology scaling is becoming more and more challenging for each new technology node. Deep sub-micron technologies have entailed an increase of the design-process inter-dependencies causing larger systematic and random variations that impact significantly the device behavior in terms of performance, power and yield. Throughout this section, variability in CMOS technologies, especially lithography layout dependent effects (LDE) which comes from manufacturing challenges and lithography distortions will be analyzed in detail. Thereby, justifying the need to counteract the lithography variations expected for current technologies and beyond.

1.1.1 The end of the technology scaling?

Gordon Moore was the first to realize that as more transistors are placed into an Integrated Circuit (IC), the cost to manufacture each transistor decreases. Back in 1965, he predicted that the number of transistors on an IC doubles every year [3]. Although Moore altered the magnitude of his predictions in 1975, stating that the number of transistors on an IC doubles approximately every two years. This statement is well-known as the Moore's law. Note that remarkably the fundamental economic justifications of the Moore's law have remained unchanged over the years providing a path for technology scaling for the last four decades.

The golden days of technology scaling ceased at the beginning of the last decade due to industry pushed lithography tools to operate at their resolution limit [4, 5]. Due to a number of technical reasons, the light wavelength is very hard to scale down, being currently and for the next CMOS generations fixed at 193nm. Starting from the 180nm logic node, IC design entered into the *sub-wavelength* era where the features being patterned are much smaller than the light wavelength of the illumination light source. Figure 1.1 depicts the increasing gap between the light wavelength and the feature size for each new technology node.

Resolution enhancement techniques ($RETs$) to enhance the printability of design features such as Optical proximity corrections (OPC), phase shift masks (PSM), sub-resolution assisted features ($SRAF$) and off-axis illumination (OAI) are being used to print sub-100nm features [7–10]. The complexity of these techniques has as a consequence an increase in cost [11]. Below 65nm, Design for Manufacturability (DFM) techniques have been in order to sustain the scaling trend [7, 11]. The DFM methodology includes a set of techniques to modify IC designs in order to make them more manufacturable, i.e., to improve their functional yield, parametric yield, or their reliability. For instance, the employment of lithography simulations to better predict circuit's behavior, wire widening or via redundancy are some DFM techniques employed to enhance IC designs.

Below the 32nm technology node, power, performance and area scaling beyond simple lithographic pitch reduction with traditional lithography put the technology scaling at risk.

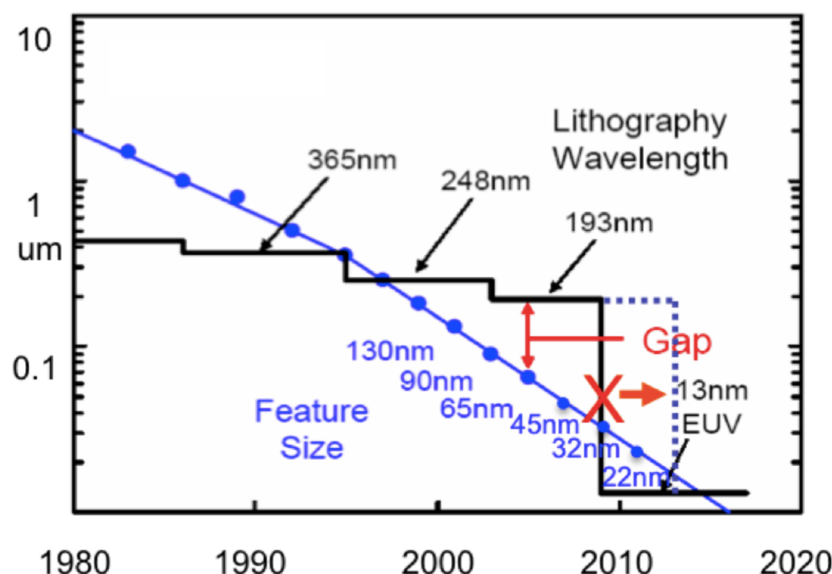


Figure 1.1: The lithography wavelength roadmap and the delayed next generation nanolithography EUVL system [6].

In order to continue the ITRS scaling roadmap, leading-edge foundries are using today's 193-nm wavelength lithography to print features more smaller than the wavelength (for instance 45nm, 32nm, 22nm and beyond) with many innovative techniques. These techniques include immersion lithography with double (or multiple) patterning (DPT/MPT) [6], more sophisticated resolution enhancement techniques [6], restrictive design rules [12, 13] and advanced source-mask optimization (SMO) [14].

The promising alternative printing engine, the Extreme ultraviolet lithography (EUVL) with a much shorter wavelength of 13.5 nm, still faces considerable burdens for production for the 14 nm and thus it is still not ready to replace the 193-nm lithography [15]. Figure 1.1 depicts the lithography roadmap during the last decades and the delayed next generation nanolithography EUVL system [6]. There are still considerable technical issues (power sources, resists, and defect-free masks) and economic issues that delayed the EUVL adoption and thus currently it is still not an option for production. The lithography roadmap predicts that EUV will be firstly introduced at the 10 nm node in 2015 [16]. However, due to the technical and economic issues, EUV will coexist with the 193-nm lithography with higher order frequency multiplication techniques like self-aligned double/quadruple patterning (SADP/SAQP) [17] or directed self-assembly (DSA) [18] to scale beyond the 10nm. Note that, SAQP and DSA have been proved to print only unidirectional features at sub 40nm pitches (sub 10 nm node) [19].

Despite the new and sometimes costly innovative techniques introduced to handle the complexities of semiconductor development that permit extending the lifetime of existing process technologies, the deep sub-micron regime has introduced new design challenges in the form of increased variability. In order to not jeopardize circuit performance, power and yield, these variations must be mitigated or at least taken into account during the design of an IC to fully realize the circuit's potential.

1.1.2 Variability in CMOS technologies

Process variations being more and more critical for each new technology node in IC design, they force either unacceptable design margins sacrificing performance, or the implementation of corrective design techniques [20] that might also have some overhead in terms of area or performance. This design overhead is unavoidable in present and future technologies, but efforts must be taken to minimize the amount of design margin necessary to cope with the source of variations. Characterizing variability accurately would allow designers to minimize the impact of variability and the employment of a more precise amount of margins to achieve an optimal design that enhances performance, power and yield.

On-chip variations are generally classified in two categories, random and systematic [21, 22]. Random or statistical process variations are related to atomistic effects inherent in nanoscale devices. Line Edge Roughness (LER), Random Dopant Fluctuations (RDP) or Interface Roughness (IR) are some sources of circuit degradation caused by this type of variation [23,24]. This kind of variations can only be tolerated and not minimized because their ultimate cause is based on fundamental physics behind the geometrical scaling down of devices and interconnects. On the other hand, systematic variations refer to critical process limitations and different manufacturing process conditions.

At the same time, systematic variations can be divided in two groups, across-field (position in reticle) and layout-dependent variations (layout structure and the surrounding topological environment). Across-field (position in reticle) variations are related to photo-lithographic and etching process parameters such as non-uniformities in photo-resist thickness, material deposition thickness, dose, focus and exposure variations, lens aberrations, mask errors and variations in etch loading. These kind of variations exhibit strong spatial correlation and they can be modeled by embedding test structures at several locations in the reticle. Across-field variations give rise to on-chip and chip-to-chip variations causing identical devices placed at different positions to behave differently.

On the other hand, layout-dependent variations or effects (LDE) which are predictable and can be modeled as a function of deterministic factors, can cause two different layout implementations of the same device to behave differently even when the two instances are placed nearby. Despite advances in resolution enhancement techniques [10], lithographic variation due to layout pattern-neighborhood dependent effects continues to be a major source of circuit's degradation. Several aspects can cause a device's behavior to be layout pattern dependent such as poly pitch variation, poly corner rounding and orientation which cause channel length variations or also referred as critical dimension (CD) variations.

Aggressive technology scaling has also entailed in many non-lithographic sources of systematic layout-dependent variations. Stress variation in strained silicon substrate is another source of layout-dependent variation that induces deviations in threshold voltage (V_{th}) and mobility of transistors [25]. Well proximity effect (WPE) is yet another well-known source of transistor's behavior degradation in terms of local layout-dependent V_{th} variation [26]. Rapid thermal anneal (RTA) also causes layout-dependent intra-die variations on the (V_{th}) and the extrinsic

resistance of the devices [27]. Pattern-dependent dishing and oxide erosion during copper Chemical Mechanical Polishing (CMP) is another source of variation [28].

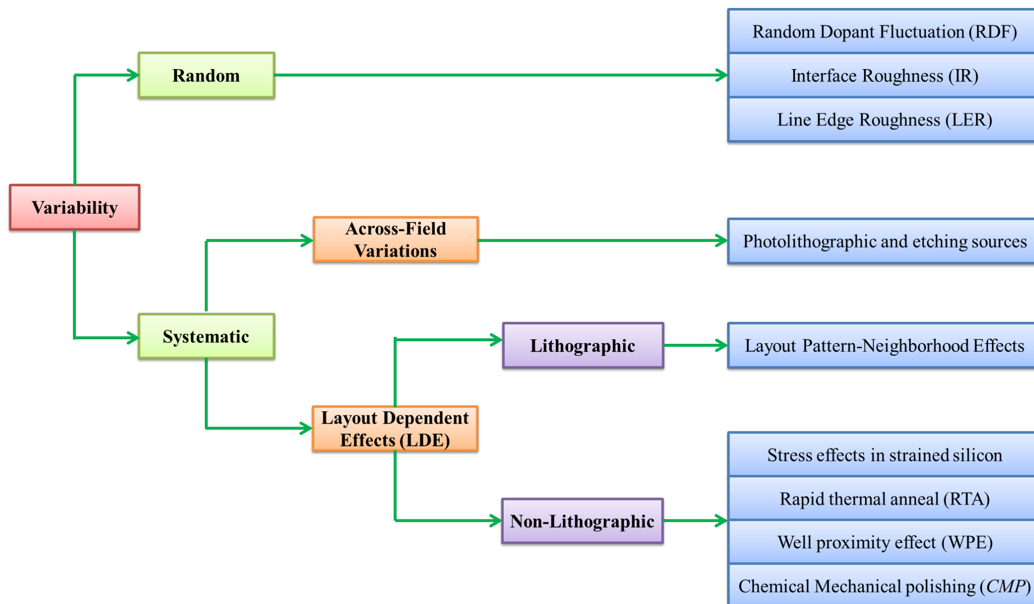


Figure 1.2: Variability sources.

It is important to highlight that systematic variations, unlike random variations which are unpredictable, can be reduced using improved process control techniques or Design For Manufacturing techniques. Figure 1.2 illustrates a summary of the different kinds of variations that must be characterized and modeled in current and future technology nodes to improved IC design manufacturing. Characterizing all these variations presents several and very different challenges and thus this thesis is mainly focused on addressing the lithography impact on systematic layout-dependent variations as detailed in the next section.

1.1.3 Lithographic layout-dependent variability

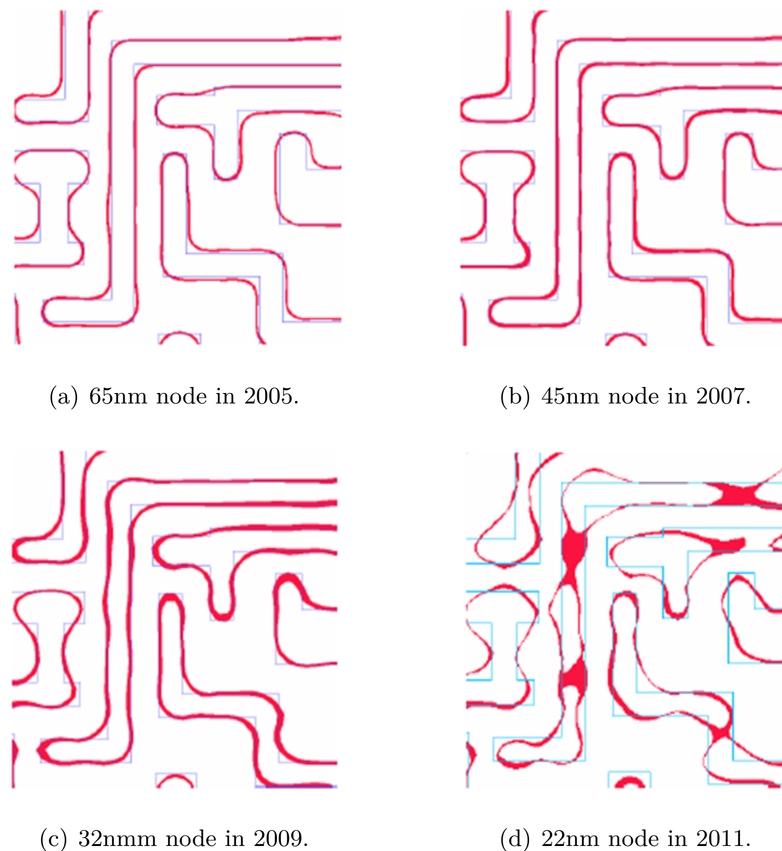
In the nano-scale era, the major source of circuit performance and power degradation associated to layout-dependent variations comes from lithography imperfections; printability becomes highly hampered and neighborhood-pattern dependent due to lithography tools are being pushed to operate at their resolution limit. According to the Rayleigh criteria, the resolution or minimum pitch, p_{min} of the lithography system can be expressed as [10]:

$$p_{min} = k_1 \frac{\lambda}{NA} \tag{1.1}$$

where λ is the wavelength of light, NA is the numerical aperture of the optical system, and k_1 is a proportionality constant related to the lithographical system.

As previously detailed, the light wavelength is very difficult to scale down, being currently and for the forthcoming years fixed at 193nm. The effect of the lithography gap in current and upcoming technologies is to cause severe distortions due to optical diffraction in the

printed patterns and thus manufacturing yield is degraded [29]. Figure 1.3 illustrates the printability degradation for different technology nodes. These distortions produce a change in the expected circuit parameters (transistor dimensions, wire resistance and capacitance, contact resistances, etc.) causing deviations in the overall circuit specifications of performance and power [30]. This leads to hotspots, corner rounding or poor Across Chip Line-Width Variation (ACLV) among other undesirable perturbations which result in systematic yield losses [31, 32]. Hence, the increasing impact of manufacturing variability on performance, power consumption and yield at each new technology node is affecting margins, silicon utilization, silicon failure, and timing closure.



(a) 65nm node in 2005.

(b) 45nm node in 2007.

(c) 32nmm node in 2009.

(d) 22nm node in 2011.

Figure 1.3: Lithography printed patterns across different process nodes [12, 33]

As technology scales down, achieving resolutions below wavelength requires a more sophisticated set of computational lithography techniques known as resolution Enhancement Techniques (RETs) as well as improvements in the numerical aperture (immersion lithography) to correct pattern distortion and reduce variability. This has forced the industry to employ costly pitch split double or multiple patterning techniques (MPL) which repeats the single patterning lithography by multiple mask/patterning process of a decomposed layout and then combining them to form the original pattern geometry. At 10nm node, MPL combined with techniques like sidewall image transfer (SIT) can print restricted bidirectional patterns at a minimum pitch down to 40nm at the cost of increasing the number of masks and thereby resulting in an increase of the final cost of an IC design [19]. For instance, at the 10nm node, at least 5 masks might be required to not jeopardize pattern fidelity if traditional bidirectional patterns are utilized. However, highly complex techniques, such as

self-aligned quadruple patterning (SAQP) or directed self-assembly (DSA), are required to scale below the 10nm node.

Note that even with all corrections and improvements, a highly pattern-dependent and neighborhood-dependent variation still remains in the printed features [34, 35]. Thus, existing design rules cannot guarantee a design that fully exploits the benefits of RETs since an efficient analysis of traditional layout patterns during the design optimization stage is difficult to perform. An advantage of lithography induced variations compared to random variations is that they can be modeled and optimized as a function of deterministic aspects such as layout structure and the surrounding neighborhood. Hence, the employment of purely litho-friendly unidirectional patterns will become mandatory to counteract the increase in the process complexity, to outperform pattern fidelity and to reduce the number of masks.

1.2 New layout designs and device technologies

The layout-dependent effects (LDE) are directly related to the configuration of the layout and the surrounding neighborhood, therefore new design strategies towards more regular layout designs must be adopted to cope with the increase in lithography variability. Lastly, despite this dissertation is focused in bulk CMOS transistors, alternative technologies are appearing in the recent years (finFETs and Fully depleted silicon on insulator devices, FD-SOI) to reduce variability. In this section, a description of these new devices and an explanation on how to extend the work of this thesis to future technologies is also provided.

1.2.1 1D regular patterning

IC design is becoming increasingly complex for either application-specific integrated circuit (ASIC) and system-on-chip (SoC) design flows in the presence of lithography induced variations. As previously described, process technology is being strongly limited by physics (wavelength) and layout design constrained by complexity, variability and cost. Conventional standard cell designs have been employing arbitrary layout patterns for decades as long as the patterns have been printed faithfully. However, for each new process node, the manufacturability of bidirectional patterns is becoming more challenging in terms of complexity and cost. Thus, as lithography advances into the 45nm technology node and beyond, a paradigm shift in design style is required to drive higher performance with smaller circuit features.

1D regular gridded cell design has emerged as an alternative to traditional 2D standard cells towards a more lithography-friendly design style [13, 31, 36–38]. 2D layout designs with bended polygons, multiple pitches and no restrictions where features are placed result in larger rules, non-optimal illumination, and little control of layout context dependent hotspots. The employment of Restrictive Design Rules (RDRs) to continue printing smaller sub-wavelength features was a middle step between regular and traditional 2D design, where practical restrictions in layout design (for instance, limiting the bends of layout features)

where applied to reduce layout pattern complexity [12]. However, despite the pattern restrictions, a large number of layout pattern configurations can still cause a considerable systematic shift in the device characteristics. Therefore, the employment of more regular implementations is necessary in order to achieve the cost reduction along with enhanced transistor performance, low power consumption, higher yields and improved functionality.

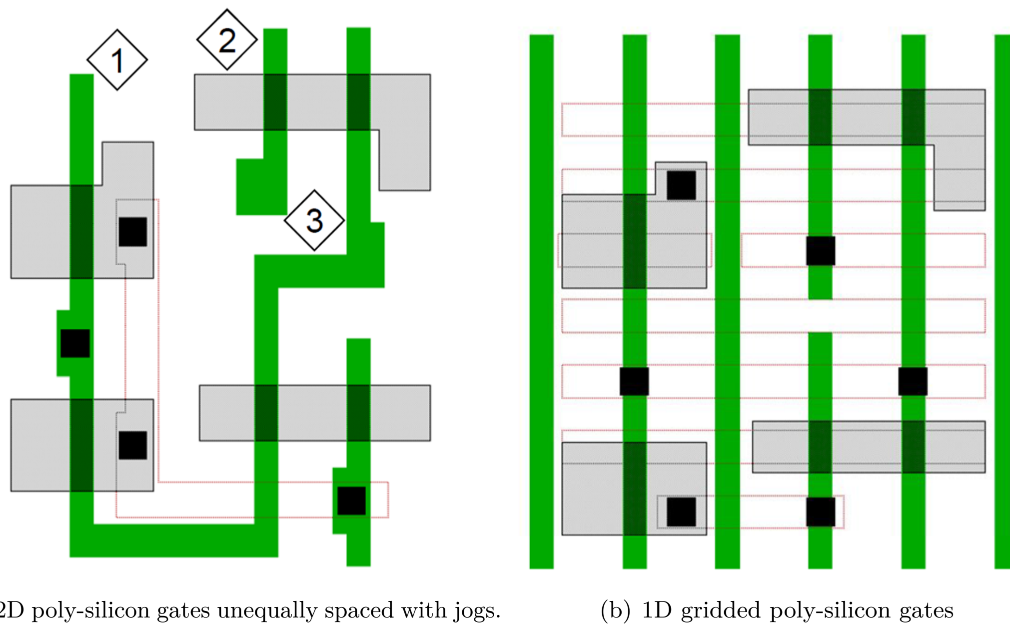
The concept of *layout regularity* can be defined as the set of fixed rules that configures a layout with all layout features belonging to the same layer being identical, unidimensional, unidirectional and equally surrounded. Therefore, a regular layout is composed by parallel straight lines (in vertical or horizontal direction) with gaps (or commonly called cuts) as required to implement circuit functions. Regularity is related to the context dependency problem, which refers to the fact that identical shapes (belonging to the same layer) printed in different locations of a cell will actually print differently if they are not equally surrounded.

The concept of *gridding* is directly associated to a regular layout since it consists in restricting the placement of any shape to specific points [39]. Hence, gridding of critical layers significantly reduces the available physical design space to place the layout features. A regular layout is therefore a gridded layout by definition, but a gridded layout does not necessary need to be regular, e.g., a layout with jogged patterns placed at specific locations.

The authors in [40], highlighted the main problems of traditional standard cell designs using 2D poly-silicon (poly) gates: (1) an isolated poly gate will have a different process window than a gate line surrounded side by side by another poly gate; (2) poly gates differently spaced from their poly neighbors will have a reduced process window; (3) 2D poly-silicon gates with jogs, besides requiring additional design rules, will also have an smaller process window. Note that the process window is defined as the range of exposure, dose and defocus within which acceptable CD tolerance is kept. Hence, a reduced process window will imply a larger amount of variations and lower manufacturing yield. Figure 1.4(a) illustrates a capture of a conventional layout where these three problems are highlighted and Figure 1.4(b) depicts a similar layout capture where this problems have been solved by introducing 1D poly-silicon gates.

The adoption of the 1D layout design style started by employing 1D poly-silicon gates in order to combat the gate length variations which resulted in excessive leakage consumption and performance deviations in the circuit. The employment of 1D poly-silicon gates is the preferred option to create cell libraries for the 32/28nm, 22/20nm and beyond technology nodes [41]. Thereby, using 1D layout designs with equally spaced and surrounded poly gates, several lithography induced perturbations can be dramatically decreased and manufacturability is enhanced due to the reduced number of geometry patterns and lithography interactions that must be analyzed.

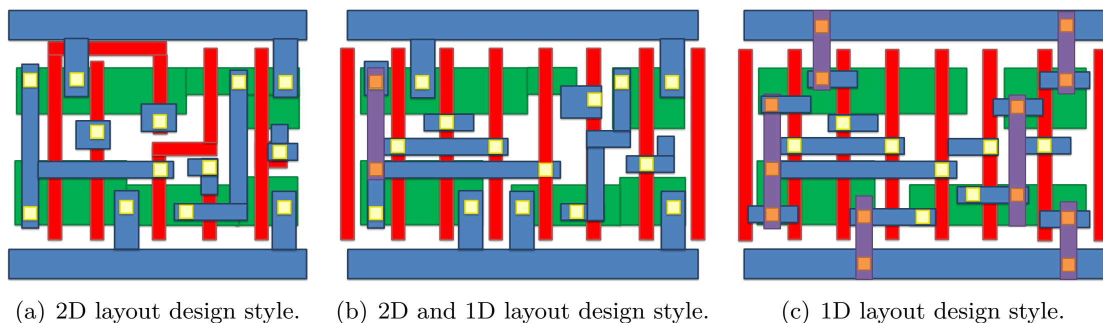
For future technology nodes (16 nm, 10nm and beyond), the employment of unidirectional-metal1 features to create standard cells is becoming a real option since besides the superior manufacturability, lower variability, better yield, lower layout complexity, more robustness and easier scalability compared to bidirectional metal1 cells, unidirectional designs may have similar design efficiency in terms of performance and area depending on the scenario under analysis. Hence, novel 1D layout designs avoiding lithography-unfriendly patterns can help to mitigate silicon printability challenges and make layouts better accommodate the



(a) 2D poly-silicon gates unequally spaced with jogs. (b) 1D gridded poly-silicon gates

Figure 1.4: Layout representation of poly-silicon gates (in green) highlighting the main problems of 2D poly-silicon gates [40].

underlying process restrictions [19, 29, 39]. Figure 1.5 depicts three layout design styles: (Fig. 1.5(a)) a fully 2D layout design style where all layers are 2D; (Fig. 1.5(b)) a layout design style with regular 1D poly-silicon gates and metal1 and diffusion 2D; (Fig. 1.5(c)) a fully regular layout design style with all layers 1D.



(a) 2D layout design style. (b) 2D and 1D layout design style. (c) 1D layout design style.

Figure 1.5: Different layout implementations from a traditional 2D layout design style towards a litho-friendly 1D style. The layer mapping is as follows: (red) poly; (green) diffusion; (yellow) contact; (blue) metal1; (orange) via12; (purple) metal2.

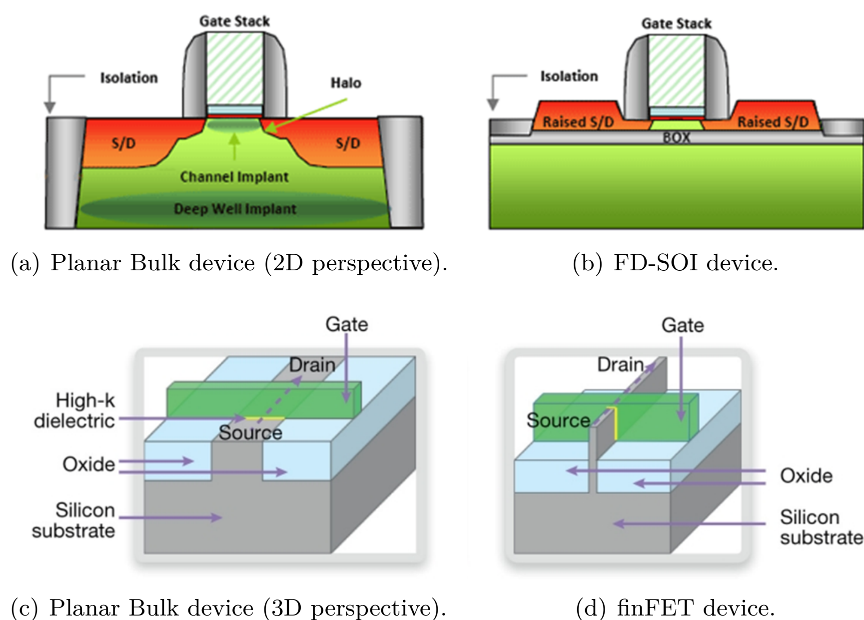
Implementing circuits other than memories following regular layout design styles may lead to significant area overhead, according to [13, 35, 42]. This overhead may be caused by the layout architecture and the limitations of traditional computer-aided design tools that are not optimized to fulfill regular design requirements. Thus, regular layouts must be properly adjusted to minimize area penalty while at the same time maximizing circuit printability and performance. Additionally, transistor ordering and intra-cell routing algorithms must be enhanced in order to minimize the area penalty that regular constraints might cause. Throughout this thesis, different degrees of layout regularity and gridding will be explored to improve layout design.

1.2.2 Alternative future technologies

Despite this thesis is focused on planar bulk CMOS designs, this dissertation can be extended to alternative future technologies that have appeared recently to overcome technology scaling barriers. In this section, a brief discussion on how to extend planar bulk CMOS layout designs to layouts employing new transistor devices is provided.

As the minimum feature size of planar CMOS transistors has fallen below 90 nm, transistors are not behaving as perfect On/Off switches due to the increasing reduction of the channel length being of the same order of magnitude as the depletion-layer widths (source and drain). As consequence, this channel length reduction is causing the so called *short-channel effects*, e.g., threshold voltage roll-off, drain-induced barrier lowering (DIBL), charge mobility degradation and threshold voltage variation [43]. Short channel effects, such as the increase of leakage power consumption, have undermined the benefits of technology scaling from 28nm to 20nm putting at risk the economic viability of planar semiconductor and thus forcing the industry to adopt new technology devices for process at 20nm and below.

New device structures are being introduced by the industry to mitigate the short channel effects, known as Fully Depleted Silicon on Insulator (FD-SOI) devices [44–46] and finFET devices [19, 50]. The silicon-on-insulator transistor is rather similar to a planar device whose channel is deposited in an insulator shallow silicon layer (buried oxide) and thus the gate can maintain a full electrostatic control of the charge carriers in it. On the other hand, finFET transistors are known as 3D devices since the channel is moved out of the bulk silicon into a vertical fin and wraps it on three sides with a gate and therefore improving the electrostatic control of the channel. Figure 1.6 depicts a diagram of these new devices compared to planar bulk CMOS transistors.



(a) Planar Bulk device (2D perspective).

(b) FD-SOI device.

(c) Planar Bulk device (3D perspective).

(d) finFET device.

Figure 1.6: Comparison of alternative future devices (FD-SOI, finFET) with respect to traditional planar bulk CMOS [43, 47].

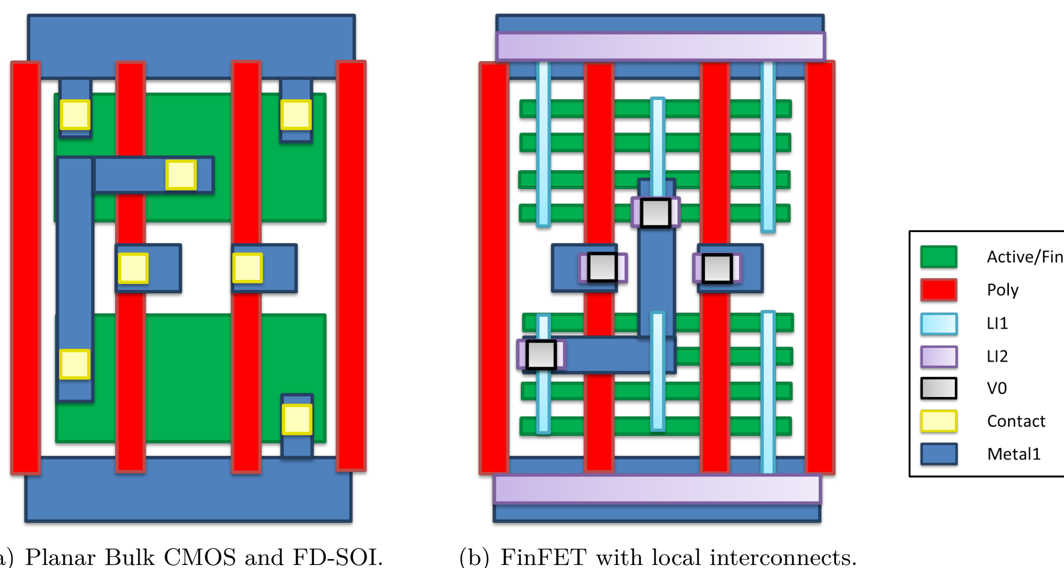
Both alternative devices present several advantages compared to bulk CMOS [43, 48]. Both architectures provide a significant reduction in the power consumption and faster switching speed. FD-SOI presents a better leakage control, even though for dynamic power mitigation, voltage scaling is probably better with finFET. FD-SOI is easier to manufacture compared to finFET since it can be fabricated following standard manufacturing processes, even though the cost of the SOI wafer is higher. FinFETs can achieve an effective speed/power trade-off by employing multi-V_{th} and also strain engineering is available for finFETs. However, for FD-SOI multi-V_{th} is more complex to implement and strain engineering is not available.

Availability to dynamically back-bias the channel (body biasing techniques) to better control the V_{th} and improving the device switching speed and no doping variability are other strengths of the FD-SOI. The main drawback of finFETs is the restrictive design options (especially for analog) due to transistor drive strength is quantized to multiples of a single fin width. One of the weaknesses of both devices is related to V_{th} variability; in FD-SOI is due to variations in the thickness of silicon thin-film; in finFETs is related to the fin width variability and the edge quality. Concluding, both devices present several advantages and still have several weaknesses or challenges to be overcome in the near future. Industry will substitute planar bulk CMOS for these two new devices, but still is unclear which one of them will be the most used for future technologies.

The key aspect to highlight of these new device architectures related to this dissertation is the layout design. FD-SOI cell libraries are compatible with existing planar bulk libraries and thus it is possible to directly port a library from a bulk process on to an FD-SOI process since the layout design is exactly the same. However, in order to take advantage of the reduced variability of the undoped channel and the different balance of capacitances in the FD-SOI transistors the cell library must be re-characterized to fully exploit the capabilities of these devices. On the other hand, the main difference in terms of layout design between finFET based design and standard cell design with 1D poly-silicon gates is the discretization of the effective transistor width defined as the number of fins added during the layout design for each finFET device. The device drive strength becomes quantized as function of the number of fins, but still it is possible to migrate circuits created for planar devices to finFETs with a lot of modeling and simulation to characterize the circuit performance.

A new layout feature to create cells with finFETs is the employment of local interconnect layers (LI) [19, 49, 50] or also referred as intermediate metallization layers, although LI layers could be also utilized in bulk and FD-SOI devices. Two LI layers placed on top of each other are employed to replace contact connections to access the diffusion or the poly-silicon layers (reducing channel strain caused by contacts). The top LI layer is linked to metal1 connections with a via (V0). Figure 1.7 depicts how the layout of the different device architectures looks like. Note that for the finFET implementation, local interconnect layers have been employed to connect the active fins and to establish power rail to active connections [19]. The employment of local interconnects to improve layout design is out of the scope of this dissertation, although it could be a possible expansion of this work.

In this dissertation, the gridded regular layout designs provided for bulk CMOS transistors will be configured with a discrete transistor size and therefore the layouts here created can be perfectly ported to create cell libraries with either FD-SOI or finFET devices. Moreover, the lithography evaluation provided throughout this work will be valid also for both devices,



(a) Planar Bulk CMOS and FD-SOI. (b) FinFET with local interconnects.

Figure 1.7: Layout designs using the different device architectures. $LI1, LI2$ represents the local interconnect layers.

with the exception of channel length variations that will be only valid for FD-SOI due to the 3D nature of the poly-silicon gates in finFETs. Concluding, it is important to highlight that still faithfully lithography patterning resolution is the key enabler for all these technology elements to be printed in advanced technology nodes and it still remains a major scaling bottleneck in terms of lithography variability.

1.3 Dissertation outline

This dissertation is focused on addressing future generation challenges in the semiconductor industry by developing cell *layout designs* and *layout evaluation* methodologies considering a *layout analysis* in terms of lithography variability. The research leading to accomplish some of the objectives of this dissertation are related to the tasks of the SYNAPTIC project (SYNthesis using Advanced Process Technology Integrated in regular Cells, IPs, architectures, and design platforms) under supervision of the European Community Seventh Framework Programme (FP7/2007-2013) [51]. In this section, the key avenues of research analyzed throughout this thesis are detailed.

1.3.1 Dissertation leitmotiv

The main goal of this dissertation is to give an answer to the following question.

> Which is the degree of **layout regularity** necessary to combat **lithography variability** and outperform the **layout quality** of a design?

In order to give an answer to this question, 3 key aspects must be addressed.

1. *Layout Regularity*: A metric to capture the degree of layout regularity, previously defined in 1.2.1, must be provided to differentiate between distinct layout configurations.

2. *Lithography Variability*: A complete analysis of the lithography impact on line-pattern resolution must be provided in order to firstly justify the need of layout regularity and secondly evaluate the impact of lithography variation on the printed patterns.

3. *Layout Quality*: The benefits of employing a layout template over another is difficult to evaluate since they can be optimized according to several purposes. Therefore, it is necessary a single metric which provides an exhaustive evaluation of the characteristics and usefulness of a layout design, i.e., the quality of the layout.

It is largely demonstrated in the literature, the manufacturability benefits of employing regular litho-friendly layout features at the expense of area overhead [13]. However, it is still unclear the amount of layout regularity that can be introduced and how to measure the benefits of a regular implementation with respect to a standard cell design. Hence, the main focus of this dissertation can be outlined as follows.

Propose different **layout architectures** exploiting the benefits of **layout regularity** and an **evaluation framework** to provide a comprehensive analysis of any layout design template.

Analysis of the lithography impact on layout design, the development of layout evaluation metrics and the creation of layout design templates are the three main aspects that will be addressed throughout this dissertation to accomplish this objective.

1.3.2 Research goals and contributions

In order to achieve the main objective of this dissertation, the present work has been focused on pursuing the following research goals and deriving their corresponding contributions as stated next.

1. Propose several layout design guidelines to mitigate lithography distortion.

   Despite regular designs outperform line-pattern resolution compared to traditional 2D designs by reducing layout dependent variations, a regular design does not directly imply that all lithography imperfections have been eliminated. Hence, lithography simulations are required to identify places in a layout where optical effects may affect functionality. Using the lithography information to highlight several common imperfections caused by sub-wavelength lithography, several layout design guidelines to mitigate the effect of lithography related process variations in layout designs are proposed.

2. Present a lithography parametric yield estimation model to predict the amount of lithography distortion expected in a printed layout due to lithography hotspots.

   A yield estimation model to analyze the impact of lithography on yield depending on the layout pattern configuration and therefore capture the link between layout design (regularity) and lithography is provided. The goal of the lithography yield model is not to give a perfect prediction of yield impact but to have an objective way of evaluating the layout quality in terms of lithography distortion with a simplified set of lithography simulations and with a reduced set of costly information obtained from silicon data. In order to do so, an efficient lithography hotspot framework to identify the different layout pattern configurations occurred in a layout design, simplify them to ease the pattern analysis and classify them according to the lithography degradation predicted using lithography simulations is proposed.

3. Evaluate the degree of layout regularity and the layout pattern complexity of a design implementation.

   In order to capture the pattern complexity of a layout design and better assess the pattern differences between layout implementations new metrics must be provided. Two metrics are proposed, the *Regularity Metric (RM)* which computes the usage of litho-friendly regular patterns and the *Pattern Construct Complexity (PCC)* metric that evaluates the level of complexity of the layout patterns employed in a design by analyzing their different geometric configurations. The aim of these metrics is not to give a perfect evaluation of the pattern complexity in terms of computational lithography complexity, but to have a framework to fairly differentiate between different layout configurations in terms of strictly layout design.

4. Provide a configurable Layout Quality Metric (LQM) to obtain an evaluation of a layout design with a single score metric.

   The lack of a layout design metric in the literature to properly compare different layout strategies, makes it difficult to evaluate the benefits and weaknesses of different layout implementations. In this thesis, a Layout Quality Metric (LQM) that taking into account several layout parameters provides a single score metric to compare different layout implementations is proposed. The aim of this metric is to present a versatile evaluation methodology which allows the designer to assess the potential capabilities of a layout design with a single score.

   The LQM is here employed following two different set of partial metrics. On the one hand, a simple layout quality metric ($LQM - S$) is presented based on the measurements of a simple set of aspects that can be computed by inspection of the layout implementation and thus it serves to give a preliminary insight about the "goodness" of a design. On the other hand, a more elaborated layout quality metric ($LQM - E$) is proposed which considering measurements of more elaborated partial metrics provides a more detailed analysis of the benefits and weaknesses of a design.

5. Create regular gridded litho-friendly layout design templates to outperform line-pattern resolution compared to traditional 2D standard cell designs.

Regular gridded layout design templates, referred as Adaptive Lithography Aware Regular Cell (ALARC) designs, are proposed to outperform traditional 2D standard cell designs. Different ALARC proposals using different degrees of layout regularity and distinct area penalty are provided. For instance, layout regularity is slightly jeopardized by introducing unidimensional rectangular metal1 connections in both vertical and horizontal directions to ease the routability of a cell. Several cell layout libraries for a 40nm technology node are automatically created to evaluate the regular templates proposed. Additionally, enhanced libraries are created by combining the compatible libraries (same cell height), but implemented with a different layout configuration. Lastly, 2D layout designs are also automatically created in order to better illustrate the benefits and weaknesses of regular layout designs.

6. Provide gridded layout design rules suitable for special transistor placement and routing algorithms to automatically generate gridded cell layout libraries.

   In a collaborative work, transistor placement and intra-cell routing algorithms [52, 53] are tuned to automatically create several layout libraries with different degrees of layout regularity. The work related to this dissertation is the creation of the design rules (for regular and non-regular designs) which guide the placement and routing algorithms to create the layout design templates proposed and the layout generation in GDS format. The design rules are modeled to create regular layout designs and traditional 2D standard cell implementations. Thus, by creating all layouts using the same routing tool, a fair comparison between the different layout design styles can be performed since results will be independent of the algorithms employed. The creation of the algorithms is out of the scope of this dissertation.

Figure 1.8 depicts an outline of the main contributions provided throughout this work divided in three main areas. Firstly, a *layout analysis* of the lithography variability impact on layout design is presented. Secondly, a *layout evaluation* framework that provides a single score quality metric to globally study the characteristics of any layout design, including a yield model to capture the lithography variations and a regularity metric, is proposed. Thirdly, the *layout design* of regular gridded litho-friendly layout structures with enhanced manufacturing yield are automatically created. Lastly, considering all the previous contributions, the demonstration that regular layouts with a certain degree of layout regularity can produce better cells in terms of overall quality is provided.

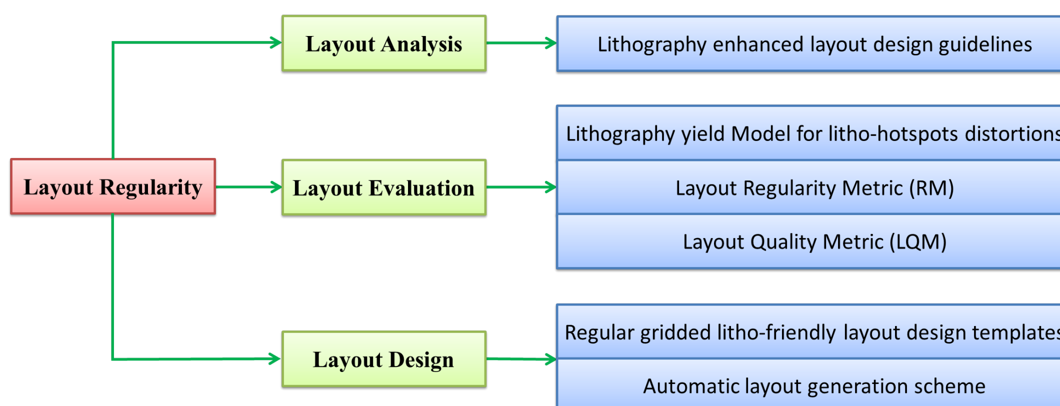


Figure 1.8: Summary of the research objectives of this dissertation.

1.3.3 Dissertation organization

This PhD dissertation is organized as follows.

Chapter 2 shows a review of the most relevant state of the art related to this dissertation. Firstly, it describes previous works that analyze the impact of lithography variability on layout design. Secondly, layout evaluation metrics such as a yield estimation model or a regularity metric are outlined. Thirdly, several regular layout implementations are detailed in order to justify the need of layout regularity. Lastly, the implications on layout design in future technologies are also provided.

A detailed analysis on how printability variations affect to layout design is presented in Chapter 3. Firstly, several lithography effects affecting to regular layout designs and the layout design guidelines to combat these lithography effects are provided. Secondly, the impact of applying the mitigation layout design guidelines is widely analyzed. Lastly, a gate biasing technique to combat channel length variations and its implications in terms of power and performance are detailed.

A parametric yield estimation model to predict the impact of lithography hotspot distortions for any layout design style is proposed in Chapter 4. Firstly, the yield formulation model and how to capture the lithography distortion through lithography simulations are explained. Secondly, the pattern construct identification, simplification and classification and how to determine if a pattern construct is considered a hotspot are described. Lastly, the yield model is calibrated using test chip measurements and it is applied to compare different layout design styles.

Chapter 5 proposes a layout evaluation framework to highlight the benefits and weaknesses between different layout design templates. Firstly, a configurable Layout Quality Metric (LQM) that combining several partial metrics enables a fairly evaluation between different layout implementations with a single-score is presented. Secondly, a simple set of measurements that can be computed by layout inspection is employed for an early layout evaluation with the layout quality metric (LQM-S). Lastly, more elaborated measurements, including metrics such as lithography yield, pattern complexity metrics, power, performance and others, are provided to more precisely evaluate a layout implementation (LQM-E).

All the previous knowledge on lithography aware design and layout evaluation is employed to propose the final regular layout designs in Chapter 6, referred as Adaptive Lithography Aware Regular Cell (ALARC) designs. Firstly, the preliminary four regular gridded cell templates manually created are outlined and evaluated using the S-LQM. Secondly, based on the previous evaluation, two improved regular layout design templates (F1D and H1D) are proposed to outperform 2D layout designs. Moreover, other two layout design templates using 2D metal1 features (M2D and F2D) are provided to compare the regular layouts with respect to more traditional 2D designs. Thirdly, a complete cell library is automatically created for these four layout implementations with different degrees of layout regularity. Fourthly, the library creation flow to create these libraries is described outlining how to create the different cell choices and how to obtain enhanced libraries by combining the compatible ones. Fifthly, several benchmark circuits are synthesized to better assess the

impact of applying layout regularity. Lastly, area, yield, pattern complexity, wire-length, power, performance and other parameters are employed to evaluate the different designs. Additionally, the LQM-E is used to finally provide a single-score in order to select the best layout design template among the different proposals.

This thesis concludes in Chapter 7 outlining the main aspects and contributions proposed throughout this dissertation and providing some interesting future avenues of research.

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2

State of the art

The lithographic gap between the light wavelength and the minimum feature size in current and future manufacturing process is causing an increase on lithography related variability in IC design. Layout regularity at cell level has emerged as an alternative layout design style to combat printability degradation instead of using complex bidirectional patterns that have been employed during decades. The most significant state of the art related to the research goals of this thesis is presented next. In this chapter, design methodologies to either evaluate or counteract lithographic layout dependent effects are analyzed. Moreover, several studies proposed different regular layout design styles to outperform line pattern resolution and the most significant layout strategies are described in this chapter. Lastly, this chapter concludes outlining the main contributions found in the literature on litho-friendly layout design and the still opened research avenues related to this dissertation are highlighted.

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2.1 Lithography variability analysis and layout evaluation

The continue advancements of semiconductor industry to manufacture smaller technology nodes have entailed several challenges in terms of layout design and lithography degradation inter-dependencies to continue the technology scaling. From the point of view of layout design, methodologies to, firstly, combat the increasing number of litho-induced process variations and, secondly, evaluate the remaining degradation suffered in layout designs must be provided to outperform the characteristics of circuits.

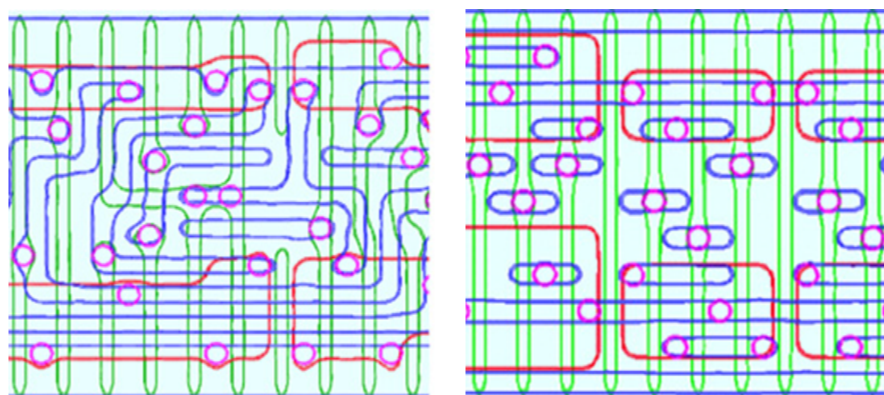
2.1.1 Lithography induced variations

In the nanoscale era, one major source of circuit performance degradation comes from lithography imperfections; printability becomes highly hampered and neighborhood-pattern dependent due to lithography tools are being pushed to operate at their resolution limit. This means that achieving resolutions for upcoming technologies requires a sophisticated set of computational lithography techniques, collectively known as Resolution Enhancement Techniques (*RETs*) [1], to improve line-pattern resolution.

The complexity of these techniques has as a consequence an increase in design cost [2]. Note that even with all corrections and improvements, there still remains a highly process variation impact in the printed features [3,4]. This leads to hotspots, line-end pull-back or poor Across Chip Line-width Variation (ACLV) among other undesirable perturbations which result in systematic yield losses [5]. Thus, existing design rules cannot guarantee a design that fully exploits the benefits of RETs since it is difficult to perform an efficient analysis of layout patterns during the design optimization stage. The work in [6] discusses some lithography effects, but applied to conventional 2D standard cells to improve line-pattern resolution.

At smaller technology nodes, lithography simulations are required to identify places in a layout where optical effects may affect functionality and thus lithography prediction has become a necessary stage of the design flow in order to better predict circuit yield, power consumption and performance of a layout design. Lithography simulations enable the possibility to properly configure a layout design to mitigate lithography induced variations and therefore not jeopardize the circuit's potential. The authors in [7], perform lithography simulations to highlight the line-pattern resolution improvement achieved with a 1D litho-friendly layout design compared to a more traditional 2D implementation, as depicted in Figure 2.1.

The gap between the drawn layout geometries and the silicon printed shapes is becoming more and more significant due to the increase in the number of lithography variations. For instance, as a result, power consumption measurement based on ideal layout is not an accurate metric, especially for low power designs, where excessive power consumption is critical. This phenomenon is mainly caused by the difference between the drawn gate length and the printed gate length which produces a considerable increase in the leakage power consumption [8].



(a) Traditional 2D layout design style. (b) Litho-friendly 1D layout design style.

Figure 2.1: Lithography simulations of two different layout implementations. The layer mapping is as follows: (red) diffusion; (green) poly; (blue) metal1; (purple) contact [7].

The best method to decrease the gate length distortion is to diminish the number of geometrical cases by making layout design to be as regular as possible and thus reducing layout dependent variations. In [9], Choi et al., present an estimation of how non-regular layout designs impact transistor channel length and thereby justifying the need of layout regularity, although they do not use lithography simulations to better estimate the impact of having non-regular features in a cell design.

Despite regular designs outperforms line-pattern resolution compared to traditional 2-D designs by reducing layout dependent variations, a regular design does not directly imply that all lithography imperfections have been eliminated. Drawn transistor channel length and poly gate spacing even for regular layouts must be properly specified in order to avoid unexpected deviations on transistor's performance. Moreover, the poly gate shape, which is supposed to be rectangular in a layout device, is severely distorted at the gate edge and the end of the gate due to the lithography process. This distortion is referred as the non-rectilinear gate (NRG) effect [10].

Lastly, variations in dose and focus, must be also captured in order to properly configure a regular layout and thereby avoiding unexpected deviations on circuit performance (delay and leakage power). Subramaniam et al. in [8], propose a systematic procedure to optimize several layout parameters in regular layouts considering layout dependent variations and the NRG effect to compensate the leakage consumption at the expense of extra area and speed overhead. In [11], the authors propose to apply small biases to the transistor gate length in order to further reduce the leakage power consumption correlating the results with the actual printed gate length. These works will be extended in this thesis, providing a more detailed gate length configuration methodology considering also dose and focus variations.

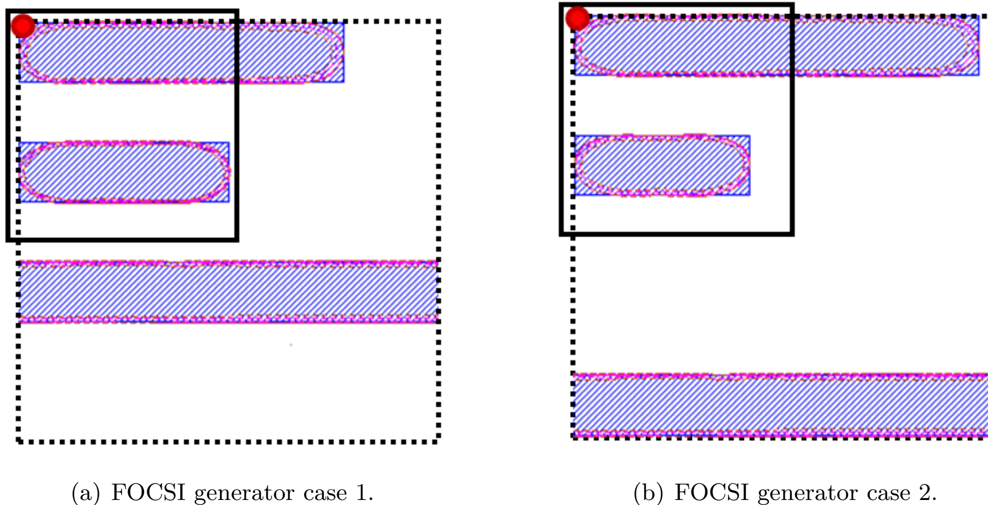
2.1.2 Layout Regularity Metric

In order to enhance layout printability, regular litho-friendly cell designs are being proposed to simplify as much as possible the complexity of layouts avoiding lithography-unfriendly

patterns. However, it is still not clear the degree of layout regularity that must be employed to overcome the lithography printability variations while at the same time not causing an excessive area overhead.

A regular layout design is composed by unidimensional and unidirectional straight rectangles (in vertical or horizontal direction) with gaps (or commonly called cuts) as required to implement circuit functions. In order to capture the diversity of the patterns of any layout design and thus capture the pattern differences between distinct layout implementations (either following the same layout design style but differently routed or different layout configurations), layout pattern complexity metrics must be provided. In [5], a 2D Fourier transform is used to evaluate the degree of layout regularity and it perfectly distinguishes between regular and non-regular layout designs. However, the graphical inspection of the Fourier graphs does not give enough information to compare layouts with a similar degree of regularity.

The authors in [12], propose another layout metric called Fixed Origin Corner Square Inspection (FOCSI) to quantify the amount of layout regularity. The FOCSI metric splits the layout in square areas considering all the upper left corners as the origin to determine the different pattern configurations (generators) and then the layout regularity is measured counting the amount of generators. Nevertheless, this metric only analyzes the repetition of the square areas (which depends on the size of the square area) and it does not capture the nature or complexity of each pattern configuration. Moreover, the FOCSI metric fails to link lithography degradation with layout regularity as depicted in Figure 2.2. Figure 2.2 illustrates two different layout generators considering two distinct square regions. For both square regions, both layout configurations suffer the same lithography distortion, but the FOCSI metric considers them as different generators. Therefore, a different number of generators does not necessary mean a different lithography degradation.



(a) FOCSI generator case 1. (b) FOCSI generator case 2.

Figure 2.2: Two different FOCSI generators with two different square areas configured. In both cases, the layout generators suffer the same degradation as can be depicted from the printed contours, but are considered as different generators.

A regularity metric serves to analyze the diversity and complexity of the pattern configurations used to create a layout and also to estimate the robustness to lithography variations of a

layout design. In that sense, more metrics to further evaluate the complexity of the patterns and capture the degradation of each pattern configuration are required to more precisely link layout regularity with lithography distortion.

2.1.3 Yield estimation models and hotspot detection methods

The effect of the lithography gap in current technologies and beyond is to cause severe distortions due to optical diffraction in the printed patterns and thus manufacturing yield is degraded [13]. The overall manufacturing yield is composed by a combination of yield due to hard defects and yield due to lithography effects. The first component is the traditional way of estimating yield and it can be represented with the Poisson model as a function of the critical area [14], as detailed in section 4.1. However, the yield due to hard defects does not capture the dependency on lithography and printability variations that also affect yield. Hence, a new yield model considering lithography variations must be provided in order to better evaluate a circuit design.

The estimation of the lithography impact on yield can be mathematically related to a probability of non-failure of lithography hotspots. Kyoh, Kobayashi et al. propose a systematic yield model which considers lithography hotspots to evaluate the degradation of a circuit [15] and a layout optimization scheme using this yield model to modify a layout in order to enhance the final yield of the circuit [16]. In this yield model, lithography simulations are performed under several process conditions to identify the degraded regions (hotspots) and thereby obtaining the critical dimension of them (minimum wire width and minimum spacing between layout patterns in the hotspot) to compute the probability of failure of a hotspot. This yield model only considers the critical dimension in a hotspot and thus it does not take into account the overall degradation suffered in the hotspot. Moreover, they do not analyze the configuration of the hotspots nor provide any method to decrease the amount of lithography simulations required to estimate the yield of a circuit. Lastly, their layout enhancement methodology optimizes an already created 2D layout using the yield model, whereas the methodology proposed in this thesis, directly creates yield-optimized layouts by applying layout regularity and thus minimizing lithography degradation by construction.

Those layout patterns with excessive variation under lithography printing, i.e., the lithography hotspots, must be identified and redesigned in order to not jeopardize the manufacturing yield of a circuit. Consequently, precise lithography hotspot identification and evaluation become a major concern in both layout design and manufacturing. Computational lithography, i.e., lithography simulations can be employed to identify hotspots and evaluate their distortion in an small layout region, but detecting all of them in a full chip scale it would require an impractical CPU time. A survey on lithography hotpot detection can be found in [17].

A significant work on this field, the EPIC framework, is proposed by Ding et al. in [18]. EPIC presents a unified scheme which combines the strength features of different hotspot detection methods, such as machine learning (deals with unknown patterns) and pattern matching (detects modeled patterns). This methodology evaluates a lithography hotspot based on the edge placement error (EPE) [19], which is basically the critical dimension (CD) error at one

edge and thus the EPE does not capture the total degradation of the hotspot. The overall distortion can be analyzed using the PVI score from Mentor Graphics [20]. Figure 2.3 depicts how to compute these two lithography degradation scores. Additionally, the EPIC employs a complex weighted function that must be properly calibrated to determine whether the layout patterns identified using several hotspot detection models are considered hotspots or not. In this thesis, instead of using a complex weighted function that needs to be calibrated experimentally, hotspots are identified using the degradation information obtained through lithography simulations (PVI score) of the most significant layout patterns.

$$EPE = \|Edge_{drawn} - Edge_{printed}\|$$

(a) EPE error computed using the Manhattan distance between the drawn edge and the printed edge (in nm) [21].

$$PVI = \frac{Area_{deg}}{Area_{drawn}}$$

(b) PVI score relating the original drawn layout with respect to the printed shape (no units).

Figure 2.3: Comparison of EPE and PVI lithographic degradation scores.

In this dissertation, the purpose of the layout pattern analysis and hotspot detection method is not to obtain a fast hotspot identification model, but to obtain a complete layout analysis of all layout pattern configurations occurred in a layout. For instance, Kahng et al. propose a fast hotspot identification method by decreasing the amount of layout area to be analyzed, without significantly compromising the detection accuracy [22]. Finally, note that this thesis focus its attention on how to characterize the layout patterns in terms of lithography distortion without using an excessive number of lithography simulations in order to properly estimate the yield loss in a layout design.

2.1.4 Layout Evaluation Frameworks

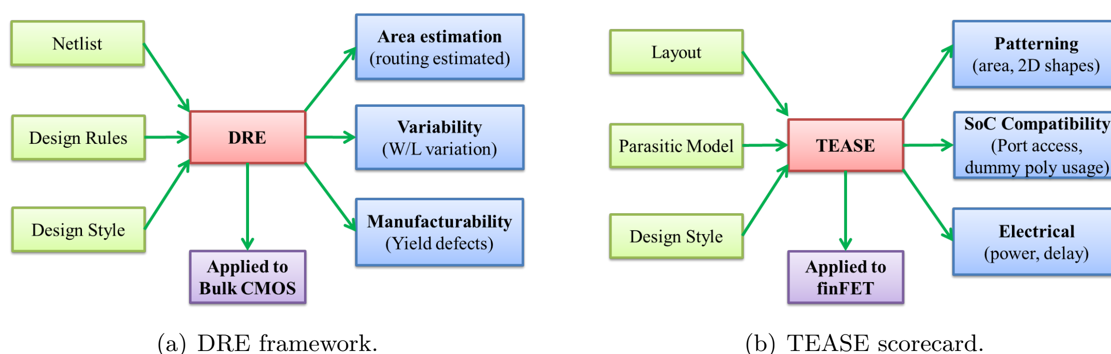
The introduction of layout regularity to modify the layout characteristics of cell design, requires new evaluation methodologies to evaluate the benefits and weaknesses of different layout implementations. For instance, Ghaida et al. propose a framework, referred as Design-Rule Evaluator (DRE) [24], for an early and systematic evaluation of design rules and layout design styles applied to the 45nm open-source FreePDK process [23].

The DRE approach analyzes a design in terms of area, manufacturability and variability. Firstly, the area estimation is performed by computing the transistor placement and estimating the cell routing and the metal congestion. For an early evaluation of complex cells requiring excessive time for routing it could be useful, but if the placement and routing

algorithms are efficient, the area can be directly obtained from the routed cell. Moreover, an early estimation of the cell height of a cell library (the cell width is computed by finding the placement), can be obtained by finding the routing of the most complex cell. Secondly, the manufacturability metric is based on computing the functional yield due to several failure sources like random particle defects or contact defects, but it does not include a yield loss analysis from lithography induced systematic failures which is one of the main objectives of this dissertation. Thirdly, the variability index analyzes the variation associated to the channel width and channel length due to poly and diffusion corner rounding and poly line-end pull-back. This metric is not useful when using 1D poly-silicon gates to reduce the excessive degradation introduced by poly corner rounding nor to analyze finFET layouts with a totally different transistor structure (3D gate and fins instead of diffusion regions). Lastly, this approach provides three individual scores analyzed independently and thus no single metric is provided to select the best library that outperforms the combination of all metrics.

Another evaluation framework named TEASE (Technology Exploration and Analysis for SoC-level Evaluation) is presented in [26]. The TEASE evaluation method is a scorecard based approach that analyzes several interesting aspects of layout designs applied to 14nm finFETS. For instance, it evaluates layout patterning complexity (cell area, 2D pattern occurrence, minimum metal area patterns, etc), SoC compatibility (local interconnects at the cell boundaries, port accessibility, dummy poly penalty...) and electrical behavior (power rail width, power, delay...). Some of these parameters are objectively quantified, but others are just qualitatively analyzed in terms of best, medium or worst score. This approach could be useful for an early evaluation of totally different layout design styles, but a comparison between rather similar designs following the same layout strategy, e.g., layouts differently routed, is difficult with this subjective evaluation. Additionally, they do not introduce a global layout design metric that considering all the aspects gives an score to decide which is the best layout design considering an overall evaluation.

Figure 2.4 outlines the main aspects of these two evaluation frameworks. In summary, the DRE method proposes an early evaluation of new layout design rules applied to bulk CMOS technology without creating the final layout and TEASE presents an scorecard analysis approach to evaluate already created finFET layout designs. In this thesis, the final layout designs are directly evaluated like the TEASE method, but providing quantitative results of all parameters under analysis like the DRE approach.



(a) DRE framework.

(b) TEASE scorecard.

Figure 2.4: Summary of the main characteristics of the two layout evaluation approaches analyzed.

2.2 Layout Designs: The need of layout regularity

The manufacturability of bidirectional patterns is becoming more challenging in terms of complexity, printability and cost for each new technology node. Several studies have addressed the regular design style as an alternative to traditional 2D standard cells toward a more lithography-friendly design style in order to combat the increase in litho-induced process variations. In this section, the most significant layout implementations developed under regularity constraints are outlined.

2.2.1 Tela innovations and TSMC

Tela innovations company [27], more specifically, Michael C. Smayling, has shown the benefits of regularity and the implications of optical lithography in circuit design in several articles [28–34]. Tela innovations has patented a lithography optimized gridded regular fabric, referred as one-dimensional gridded design rule (1D GDR), that employs 1D layout structures resulting in significant improvements in variability, performance, power and area.

The 1D GDR cells are mainly characterized by the employment of equally spaced 1D poly-silicon gates instead of traditional 2D poly-silicon gates unevenly spaced and the usage of 1D metal1 connections. Moreover, the fabric is gridded, i.e., all layers lie over a routing grid with a fixed pitch in the x and y axis and not being necessarily the same in both directions. Figure 2.7 depicts a simple layout representation of this gridded regular layout strategy where the active region is the only 2D layer.

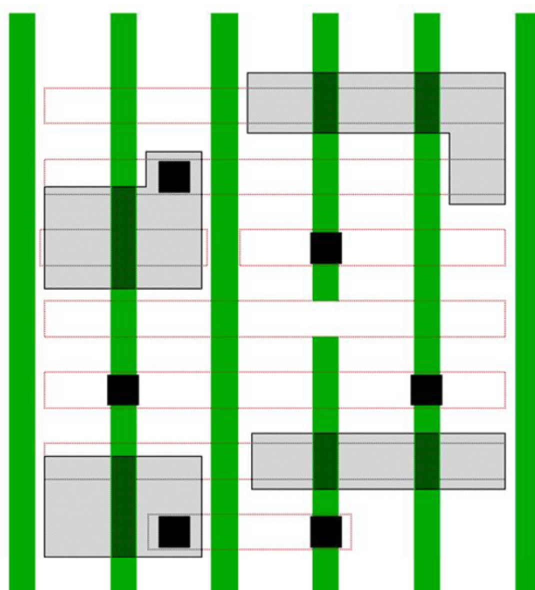


Figure 2.5: Layout representation following the 1DGDR layout design style [27]. The layer mapping is as follows: (grey) active; (green) poly; (black) contact; (white) metal1.

In [28], Smayling states that the 1D GDR cells have several advantages over 2D complex design rule cells, including smaller area, better gate CD control and elimination of hotspots and thus regular designs are expected to more easily scale in terms of lithography complexity. Smayling compares the 1D GDR layouts with traditional 2D standard cell designs for several circuits at technology nodes from 90nm to 45nm and he states that the 1D layouts achieve 5% to 17% smaller areas for allowed design rules. However, the author does not provide details about the layout configuration of the 1D GDR nor the configuration of the 2D layout design for the comparison and therefore it is difficult to extract conclusive area results. Moreover, Smayling proves that 1D designs achieve better gate CD uniformity by showing the gate CD distribution of a 1D and 2D implementation of a D Flip Flop logic cell under worst-case simulated exposure conditions, as illustrated in Figure 2.6. The regular design presents a tight CD distribution compared to the sparse and lower gate length distribution of the 2D design and thus resulting in better leakage current control due to the lower variations suffered (50% reduced leakage using the 1D on a 45nm test circuit).

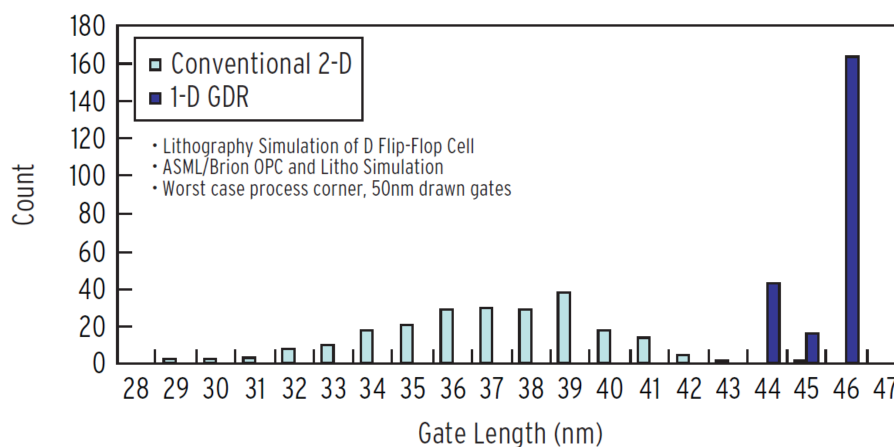


Figure 2.6: Gate length CD distribution for the 1D GDR and 2D layout design styles.

Other interesting results come from the collaboration work between Tela innovations and Taiwan Semiconductor Manufacturing Company Ltd. (TSMC) [35]. They implemented two microprocessor cores (ARM9 and ARM11) for a 65nm technology library implemented following the Tela 1D GDR and using 2D TSMC standard cells with equivalent performance and power configuration and they achieved a 15% area reduction in both processors. Note that this 1D design employs unidirectional poly on a fixed pitch, but no specification of the metal1 configuration is provided. Lastly, the most recent and detailed layout design provided by Tela is provided in [27], as illustrated in Figure 2.7. In this case, the company implemented a D Flip Flop for a 28nm technology node following a 1D layout design style for poly-silicon gates, but with a 2D metal1 configuration. Therefore, the company proposes designs with different degrees of layout regularity.

Concluding, Tela innovations have shown in several articles that regular designs can lead to significant area reduction, but few details are provided about the degree of layout regularity applied in each layout design. Therefore, regular designs can be competitive in the near future compared to standard cell designs in terms of area and also in gate CD variability reduction. However, some other authors state that circuits other than memories designed

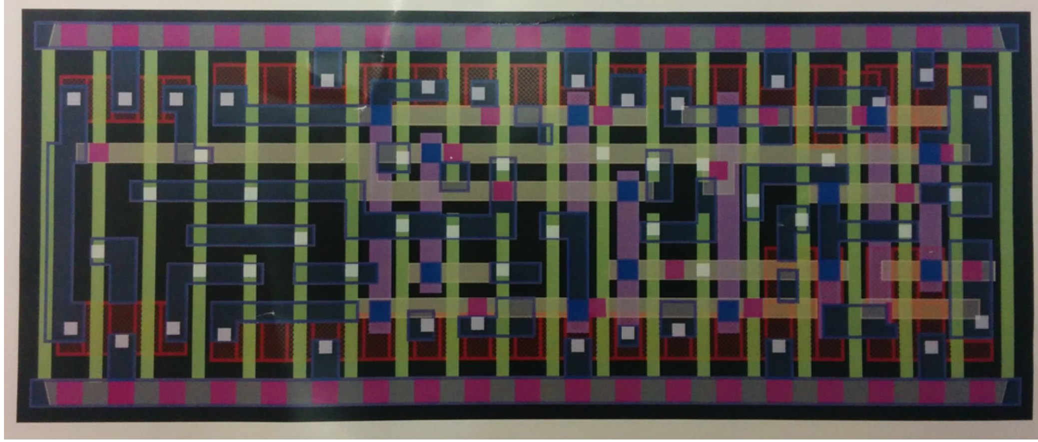


Figure 2.7: Example of a 28nm SDFF layout following the 1D GDR layout design style [27]. The layer mapping is as follows: (red) active; (green) poly; (white) contact; (dark blue) metal1; (pink) via1; (purple) metal2; (blue) via2; (grey) metal3.

following ultra-regular layout design styles might suffer excessive area overhead due to the tight layout structure, as analyzed in the following sections. In fact, Tela 1D GDR is not an ultra-regular design, hence a trade-off between regularity and area penalty might be necessary for current and future technologies to outperform layout design.

2.2.2 PDF solutions, IBM Microelectronics and Carnegie Mellon University

Jhaveri et al. propose a design framework that improves cell printability by applying layout regularity [5, 7, 36–39]. This methodology is based on three steps. (1) *Regular fabrics*, definition of the pattern constraints and the layout configuration such as the cell pitch; (2) *templates*, set of single stage logic functions based on the regular fabrics constraints; (3) *standard cell libraries*, templates are assembled into larger functions of a functional cell library, including traditional standard cells as well as larger application-specific functions known as *bricks*. The most important aspect of this design flow is the proper definition of the fabrics to create the templates, even though the templates might have limited relaxed fabric constraints, like permitting some 2D patterns. Therefore, templates are co-optimized in terms of layout design and lithography printability in order to enable die cost scaling and satisfy circuit specifications. Lastly, note that the creation of both the logic templates and the application specific bricks is beyond the scope of this thesis.

In [7], Jhaveri et al. provide three gridded regular fabrics configured to meet different product requirements and process goals. All these fabrics aim to reduce systematic layout dependent variability on poly-silicon gates by prohibiting non-unidirectional layout patterns on the poly layer. The specific characteristics of each regular fabric are outlined next.

1. **Back end of line (BEOL) limited regular design fabric**.

   The BEOL aims to ease contact redundancy by defining the metal1 layer parallel to the poly-silicon gates and defining the poly pitch as twice the metal1 pitch, as shown in

Figure 2.8(a). This fabric has significant area overhead since the poly pitch is defined 50% larger than the allowed contacted gate pitch.

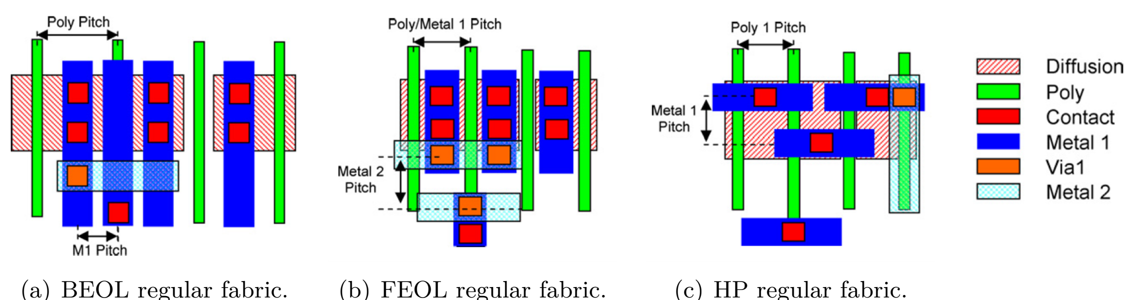
2. **Front end of line (FEOL) limited regular design fabric**.

   The FEOL seeks to achieve similar area results than conventional designs by defining the poly pitch equal to the contacted gate pitch. This fabric also employs metal1 parallel to poly to enable redundant contact and vias, but in this fabric the metal1 is drawn at a larger pitch equal to the poly pitch, as illustrated in Figure 2.8(b). As a consequence, a metal1 connection on adjacent vertical locations is forbidden; for instance, a metal1 connection that joins the PMOS and the NMOS network, blocks the adjacent routing track to access to the poly-silicon gates in between active regions. Despite this metal1 configuration seems to be challenging in terms of printability, simulations performed and silicon data showed that it is actually printability friendly.

3. **High-performance (HP) limited regular design fabric**.

   The HP fabric also defines the contacted gate pitch for the poly layer as the FEOL fabric to enable compact designs. However, the metal1 configuration of the HP fabric is the opposite as the other fabrics since metal1 is placed perpendicular to poly. This metal1 configuration forces the transistor active region to have at least two metal1 rows of size in order to ensure the minimum metal1 area requirements of adjacent connections, as depicted in Figure 2.8(c). Lastly, note that contact redundancy is difficult to apply in this fabric.

Layout captures highlighting the main aspects of these manufacturability friendly layout designs are provided in Figure 2.8.

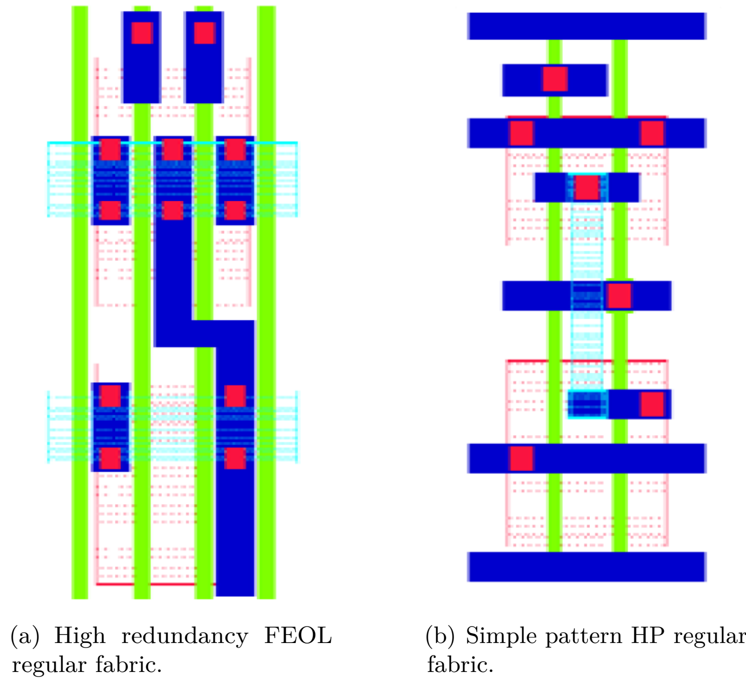


(a) BEOL regular fabric. (b) FEOL regular fabric. (c) HP regular fabric.

Figure 2.8: Layout capture of the regular design fabrics proposed in [7].

As a mode of example, a NAND2 logic template optimized to meet design requirements for a 32nm technology node following the FEOL and the HP regular fabrics is depicted in Figure 2.9. Observe from Figure 2.9(a) that the FEOL template employs on-grid 2D metal1 patterns in order to reduce the number of single vias, whereas the HP fabric only employs 1D metal1 connections.

In terms of manufacturability, one advantage of simple unidimensional patterns is the possibility to use *pushed rules* in order to reduce the area penalty introduced by layout regularity. A pushed rule is a relaxed specification of a conventional rule, e.g., shorter spacing between layers. In [5], the authors compare a D Flip Flop (DFF) cell in a 65nm



(a) High redundancy FEOL regular fabric.

(b) Simple pattern HP regular fabric.

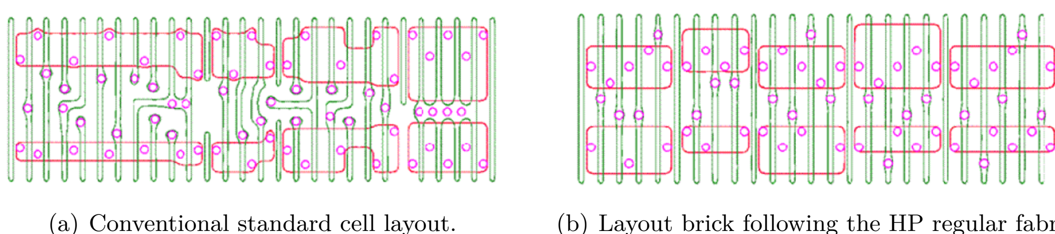
Figure 2.9: NAND2 logic templates following the FEOL and the HP regular fabrics for a 32nm technology node [39].

technology node implemented in a regular fabric with respect to an implementation using conventional standard cells (employing 2D off-grid poly, 2D metal and diffusion routing) considering design-compliant rules and pushed rules. The regular fabric is optimized for manufacturability whereas the standard cell design is optimized for compactness. Using lithography simulations they show that the regular fabric using design compliant rules has 72.8% area penalty and 2x Across Chip Line-width Variation (ACLV) improvement compared to the standard cell design, whereas the pushed rule regular fabric only has 12.25% area overhead and an slightly lower value of ACLV improvement of 1.76x due to the reduced process window observed. Therefore, the employment of pushed rules for regular fabrics significantly reduces the area overhead, but it requires an area-manufacturability trade-off optimization in order to save area while keeping the manufacturability of the design.

In the same work, they also perform a second experiment to validate silicon manufacturability and yield improvement of using pushed rules by implementing a full-adder brick configured as a ring oscillator in a 65nm bulk CMOS technology. The employment of pushed rules on the regular fabric design produces a 2.2% of area improvement. Additionally, the standard cell implementation suffers excessive delay propagation variability on 4.53% of all tested dies and 4.99% of the dies fail due to leakage current variability. On the other hand, the regular fabric does not suffer from delay variations and leakage variations only produce 2.72% of the dies to fail. Therefore, the number of good dies per wafer considering the power and performance metrics for the regular fabric is 97.28%, whereas for the standard cell design is only 90.48%. The employment of pushed rules is out of the scope of this dissertation, but it is important to highlight that the results presented throughout this thesis could benefit for the usage of pushed rules and thus improving the area penalty introduced by regular designs.

Layout regularity must be applied to an entire IC design in order to more precisely evaluate its potential benefits. A discussion on the area overhead and routing capabilities of a DFF illustrates the worst case scenario for a given layout style, but it does not provide a complete picture of the problem. L. Liebmann, T. Jhaveri, et al. show the benefits of layout regularity by implementing two processors. Firstly, an ARM926EJ processor in a bulk low power 65nm process is implemented using the FEOL regular fabric and their application-specific methodology (bricks) [7]. This design uses sixteen bricks, seven templates, three different D flip flops (DFFs), inverters and buffers and thus a small library is required to implement the processor. The regular implementation of the processor using pushed rules but not logic optimization leads to 6.67% utilized area overhead compared to the standard cell design implementation using design-compliant rules.

Secondly, a 65nm PowerPC405s core is redesigned using, in this case, the HP regular fabric with all layers unidimensional and using the brick framework [7, 37]. The main advantages of the regular implementation with respect to the traditional one are outlined next: (1) *area reduction*, sequential logic area is identical and combinatorial logic decreases by 25% due to the usage of pushed rules and application-specific logic cell functions; (2) *hotspot reduction*: patterning robustness is improved by not using complex 2D layout shapes that could lead to yield losses; (3) *variability improvement*: the employment of simple unidimensional patterns highly reduces variations such as channel length variability and thus providing a significant improvement in manufacturing yield; (4) *design simplicity improvement*: the usage of simple regular layout patterns enables the possibility of fast creation and optimization of cells and more specifically, the creation of application-specific logic cells to further improve the IC design. Figure 2.10 depicts the predicted lithography contours of the regular layout implementation and the standard cell design, showing the hotspot reduction and variability improvement achieved with the regular design.



(a) Conventional standard cell layout. (b) Layout brick following the HP regular fabric.

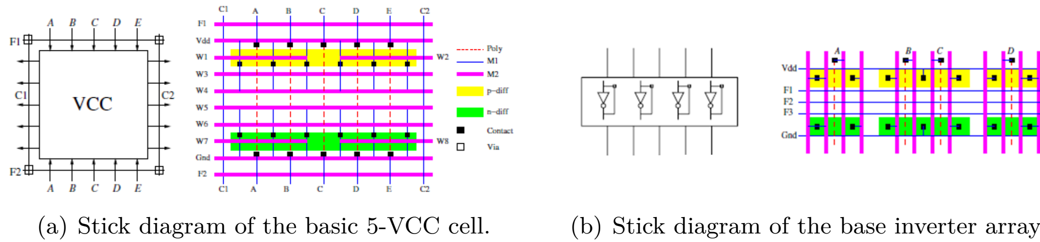
Figure 2.10: Lithography simulation of a layout capture of the 65nm PowerPC405s circuit [37]. The layer mapping is as follows. (red) Diffusion; (green) poly; (pink) contact.

All the previous advantages, perfectly summarize the benefits of employing layout regularity. Note that these regular fabrics are just an initial point for process-design co-optimization and they must be properly configured to meet specific area, power, performance and manufacturing yield targets considering technology specific constraints. The gate pitch, metal and poly extensions, poly channel length, metal width and spacing, diffusion configuration, contact and via enclosures and the use of metal1 non regularities are examples of technology needs. All these parameters are technology dependent and they must be configured using lithography simulations. Finally, it is important to highlight that an study on how to configure these regular fabrics and the degree of layout regularity, i.e., the amount of irregularities admitted for each template is not provided by the authors.

2.2.3 University of Santa Barbara and Universitat Politècnica de Catalunya

The employment of repetitive layout instances with identical pattern configuration placed in a spatially periodic location might permit for reuse of prior design and manufacturing results and therefore decreasing the cost of the IC design. Next, two layout proposals that have addressed IC design seeking to maximize layout regularity by repetitive usage of a basic layout structure with interconnect regularity complete (all the routing channels are implemented and configured using vias) are outlined.

Ran et al. from the University of Santa Barbara are the authors of a regular fabric called Via-Configurable Gate Array (VCGA) [40–43]. The VCGA cell structure is composed by multiple instances of a basic logic element (BLE) that consists of a via-configurable functional cell (VCC) and two neighboring inverter arrays. Each BLE contains a fixed number of layout patterns including transistors with a fixed size and all routing channels with pre-placed metal1 and metal2 connections. Hence, only vias must be configured to implement the cell functionality. Figure 2.11 depicts the components of the VCGA for a 5-VCC structure. Note that the VCC can be parametrized depending on the number of transistor pairs that it contains, but the same size is used in the whole array as illustrated in Figure 2.12.



(a) Stick diagram of the basic 5-VCC cell. (b) Stick diagram of the base inverter array.

Figure 2.11: Basic logic element (BLE) components of the VCGA [40].

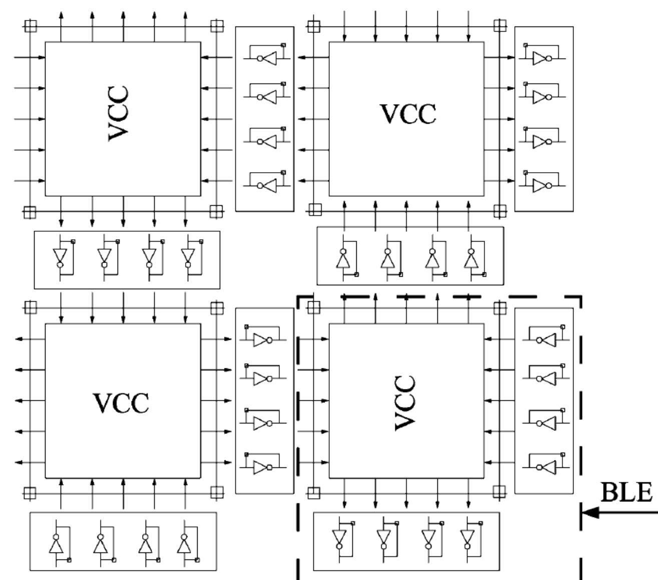
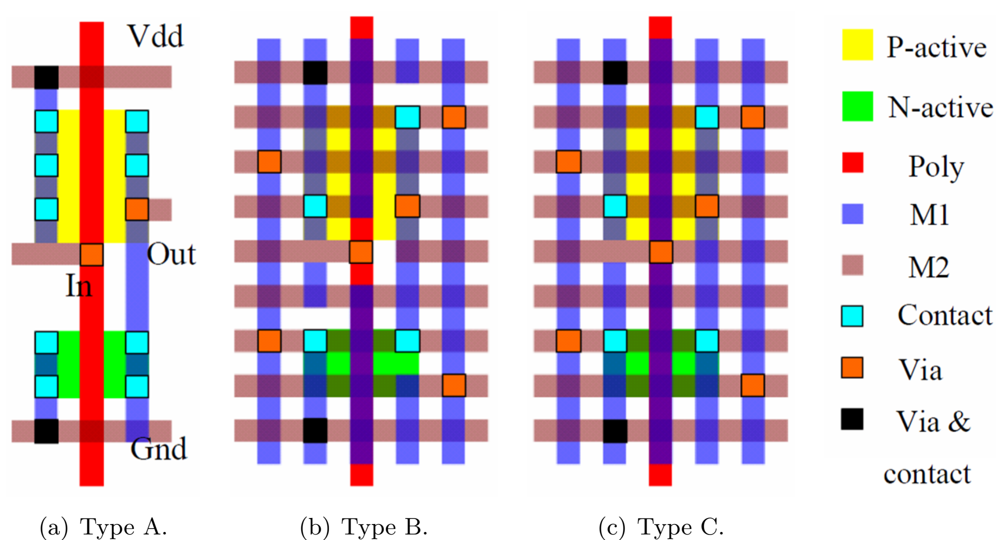


Figure 2.12: Via-configurable gate array (VCGA) [43].

Experimental results over a 180nm technology node on several benchmark circuits, show that the VCGA fabric with an 85% of transistor utilization on average presents an area overhead of 116%, a 33% of performance degradation and a 17% extra power consumption compared to a standard cell design. Thus, despite the manufacturability enhancement achieved by employing a regular layout configuration with the repetition of identical blocks, the VCGA produces designs with large deviations on area, performance and power compared to traditional designs.

Maly et al. from Carnegie Mellon University in collaboration with people from University of Santa Barbara presented in [44], a performance and area evaluation of three regular gridded fabrics with different degrees of layout regularity. These layout designs are not created by the repetition of a basic layout structure, instead they are more closer to a standard cell design layout with a specific pattern configuration to augment layout regularity. All designs are composed by equally sized transistors with vertical 1D poly-silicon gates and logic functions are created by introducing metal cuts, vias, or contacts. The main differences of these fabrics are detailed next: *Type A*, minimum 1D metal connections are employed like a traditional standard cell design; *Type B*, all routing channels are occupied, with the exception of metal cuts with minimum size to separate connections; *Type C*, all routing resources are maximally utilized and metal cuts, vias and contacts are minimized and uniformly distributed. Figure 2.13 illustrates the main characteristics of these three on-grid layout designs by implementing an inverter logic function.



(a) Type A. (b) Type B. (c) Type C.

Figure 2.13: Inverter layouts following different regular structures [44].

Average delay, area, and power of six functional cells using these three regular layout structures for a 130nm technology node are analyzed. Type A cells have the best results in all these three parameters due to the most versatile customization. The area penalty of Type B and C is approximately 24% compared to Type A. The average delay and power of Type B and C cells are 12% and 30% worse respectively compared to Type A. The power and performance overhead of Type B and C designs are caused by additional coupling capacitance introduced by floating wires and besides the overhead is even larger for Type C due to the employment of extended wires to minimize the metal cuts. Despite the reduced set of data

used in these experimental results, it can be concluded that the employment of extra metal connections to maximize layout regularity and thus simplify the metal masks, produces a large overhead in terms of power, performance and area.

The VCTA proposal, described in [45], is a regular implementation following a rather similar layout strategy as the VCGA cell design. The VCTA is based on the repetition of a single basic cell (BC) that can synthesize different functions by placing contacts and vias in different locations. The BC is configured with a regular interconnection grid with metal connections from metal1 to metal3 and with all transistors having the same width. A 6-VCTA block is composed of six PMOS transistors and one dummy transistor (DT) at each end of the diffusion strip and the same structure is used for the NMOS transistors, as depicted in Figure 2.12. Note that dummy transistors are not used to implement the cell functionality, but instead they are placed so each transistor in the BC has a transistor at both sides and thus channel length variations are reduced.

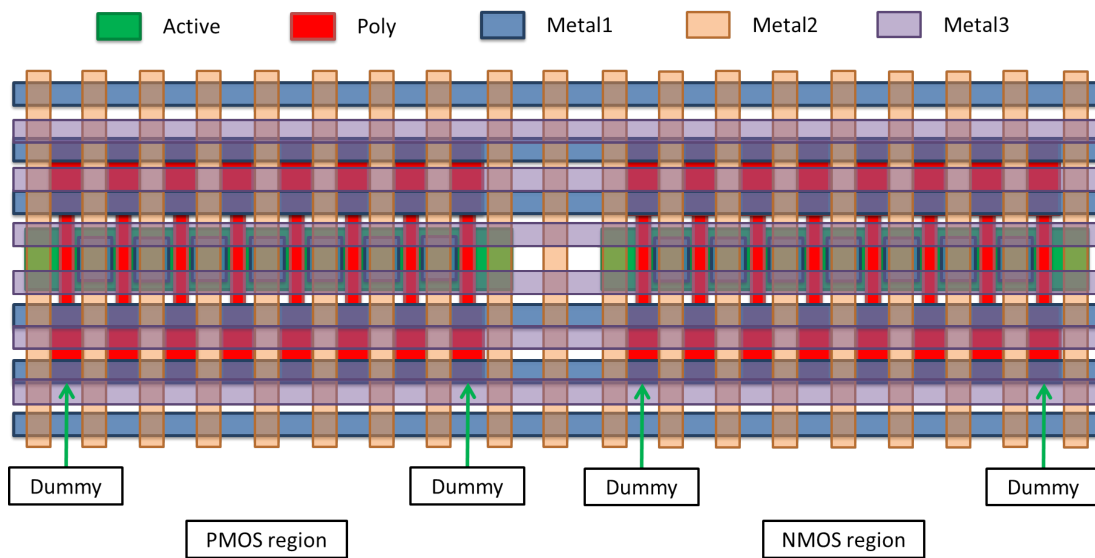


Figure 2.14: Basic VCTA cell structure. Metal1 and metal3 run horizontally and metal2 and poly run vertically. A VCTA array is formed by placing on top, bottom and at both sides any number of VCTA cells [45].

Experimental results over a 32-bit Carry-Lookahead adder (CLA32) and over a 32-bit Kogge-Stone adder (KS32) for a 90nm technology show a large penalty in terms of area, power and performance compared to a traditional standard cell design. In average, the VCTA presents a 2x performance degradation, a 2.3x larger energy consumption and 2.3x area overhead with respect to the same benchmarks but implemented with a commercial standard cell library.

The main advantages of the VCTA fabric are undoubtedly the simplicity of the layout configuration of the basic cell and thus its easy scalability, and the amount of layout regularity employed in order to reduce lithography variability. On the other hand, the main disadvantages of this fabric are the area, power and performance degradation. These drawbacks come from the employment of dummy transistors and the unused transistors that introduce excessive area overhead, the rigid and large metal grid distribution that causes a large parasitic capacitance and the fixed transistor size that requires excessive fingering to accommodate cells with large transistor sizes.

Concluding, it is important to highlight that despite the undoubtedly printability and cost benefits of using full regular layouts, the large penalty in terms of power, performance and area requires some regularity trade-offs in order to obtain competitive results. This kind of structures aims to maximize regularity at cell and circuit level, however the dense and large parallel interconnection grid causes performance losses related to large parasitic coupling capacitance. Moreover, despite the high configurability of this type of designs, a 100% utilization is difficult to achieve in practice. Therefore, regular designs that follow a more similar layout strategy compared to a traditional standard cell design, seem to be a more efficient configuration despite following a less simple layout design.

2.2.4 Nangate Inc. gridded regular cell libraries

This section briefly outlines the most significant features of a traditional 2D standard cell design and a half 1D design employing 1D poly-silicon gates proposed by Nangate Inc [46] for a 40nm commercial technology node. The information of these libraries is the only complete layout and circuit data available for analysis and thus it will be taken as reference to compare the quality of the regular designs provided throughout this dissertation. Note that only the indispensable characteristics of these two layout templates are provided.

1. Traditional Nangate layout design style with all shapes 2D (NA2D).

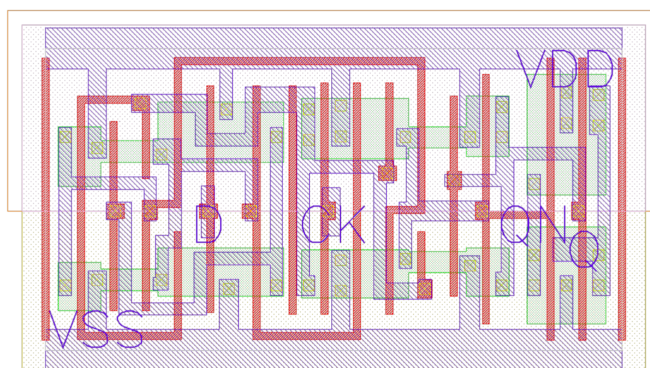
   This layout design style aims to produce competitive cells in terms of area and metal utilization by using a totally 2D layout design style and thus this template is more susceptible to layout dependent variations, e.g., channel length degradation and metal distortions. The most representative features of this 12 track template are detailed next. Firstly, this template follows a traditional 2D standard cell design and it employs 2D layout patterns for poly, diffusion and metal1 connections. Secondly, layout patterns are not placed in specific grid points and thus they can be placed at any location. Thirdly, the cell pitch in the vertical axis is the minimum specified in the technology between horizontal metal1 connections and the pitch in the horizontal axis is variable and it can be bigger than the minimum. Fourthly, poly-silicon gates are not always equally spaced and therefore this template is more susceptible to channel length degradations. Lastly, this layout design style does not require the employment of metal2 nor metal3 connections to route a cell library including combinational and sequential cells. Hence, cells from this library will not suffer from via reliability issues since vias are not required inside the cell.

2. Poly 1D gridded layout design style (NP1D).

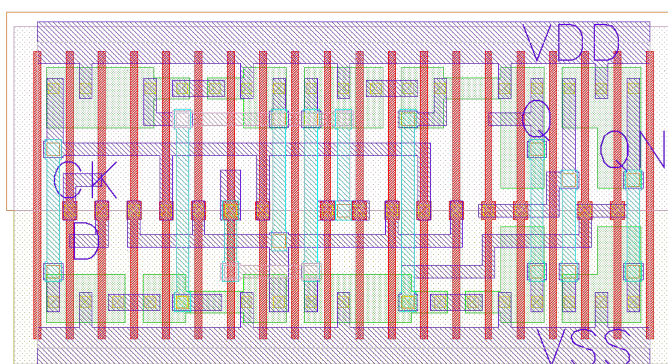
   This layout implementation aims to produce competitive cells in terms of area and poly-silicon manufacturability by penalizing arbitrary layout pattern design in order to reduce channel length variations. The most significant aspects of this 10 track template are detailed next. Firstly, this template follows a more traditional 2D layout design style using 2D features for metal1 connections and diffusion, although poly-silicon gates, metal2 and metal3 employs 1D layout patterns. Secondly, all layout features are placed over a routing grid and therefore poly-silicon gates are equally spaced by

definition. Thirdly, the cell pitch in the vertical axis is bigger than the minimum and the pitch in the horizontal axis is set to the minimum determined by the poly-silicon design rules. Lastly, 1D metal2 connections are slightly employed to route the cells and thus reducing the via usage, and metal3 connections are occasionally employed in a few cells only when routability becomes unfeasible otherwise.

Figure 2.15 depicts a D Flip Flop logic cell implementation following the two layout design styles previously described. An evaluation of these layout templates in terms of lithography, pattern complexity and area is provided in Chapter 4.



(a) Traditional 2D layout design style.



(b) Litho-friendly 1D poly-silicon layout design style.

Figure 2.15: D Flip Flop cell created following the Nangate layout design styles. The layer mapping is as follows: (red) poly ; (green) diffusion; (yellow) contact; (blue) metal1; (orange) via1; (light blue) metal2; (grey) via1; (pink) metal3.

2.3 Layout design in future technologies

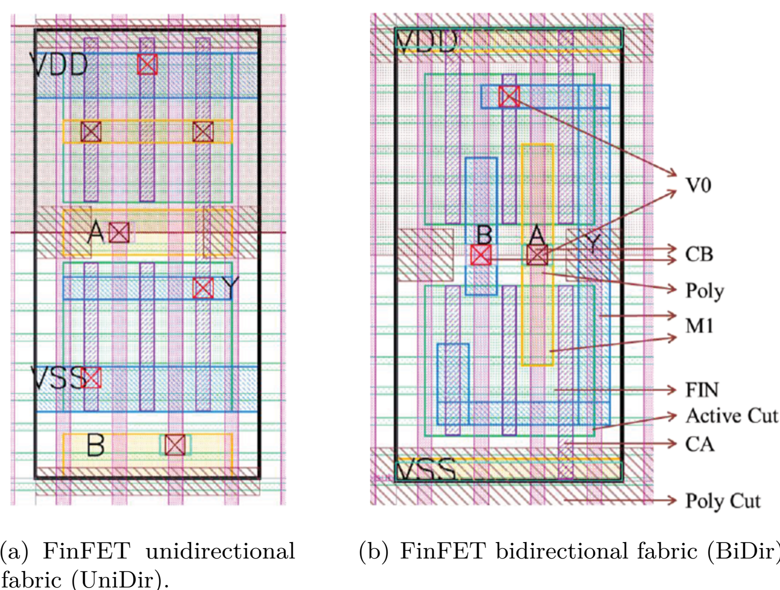
New devices are being proposed by the semiconductor industry to overcome the drawbacks of bulk CMOS technology such as short channel effects. As detailed in section 1.2.2, IC design in future technology nodes will be based on FD-SOI or finFET devices. Despite this thesis is related to bulk CMOS technology, a brief description of the state of the art of future

layout designs is provided in order to illustrate how this dissertation can be extended to the next generation of layout devices.

In terms of layout design, FDSOI cell libraries are compatible with existing planar bulk libraries and thus it is straight forward to port a library from a bulk process on to an FDSOI process since the layout design remains unchanged. Hence, all layout design styles found in the literature for CMOS layout design can be simply extended to FDSOI, even though power and performance must be re-characterized. A recent work on FDSOI devices comes from CEA-LETI-Minatec and STmicroelectronics [48]. The authors show that FDSOI devices can operate at a frequency up to 30% faster for a given power budget and the power consumption can be reduced up to 30% for the same speed than a bulk CMOS design and thus proving the benefits of using this enhanced devices. The application of the regular layout design templates proposed in this thesis extended to FDSOI devices, could be a future avenue of research derived from this dissertation.

Conversely, cell libraries for finFET devices can not be directly ported from bulk designs, especially when local interconnects are employed to replace the contact layer. The main difference between finFET layout based design and conventional standard cell design lies in the discretization of the effective transistor width in terms of number of fins for each finFET device, instead of the single traditional rectangular active region for a bulk or FDSOI device, as depicted in Figure 1.7. Furthermore, local interconnects are new layers used for intra-cell routing, e.g., local interconnects are employed to connect the active fins.

In [49], Vaidyanathan et al. extend their finFET layout approaches outlined in [13] and the resulting cell layout designs for an IBM 14nm process are illustrated in Figure 2.16. The authors propose two layout implementations: (1) a *unidirectional gridded regular fabric* (UniDir), where metal1 is regular; (2) a *bidirectional gridded fabric* (BiDir), where the metal1 is placed only over the routing grid, but 2D jogs are permitted.

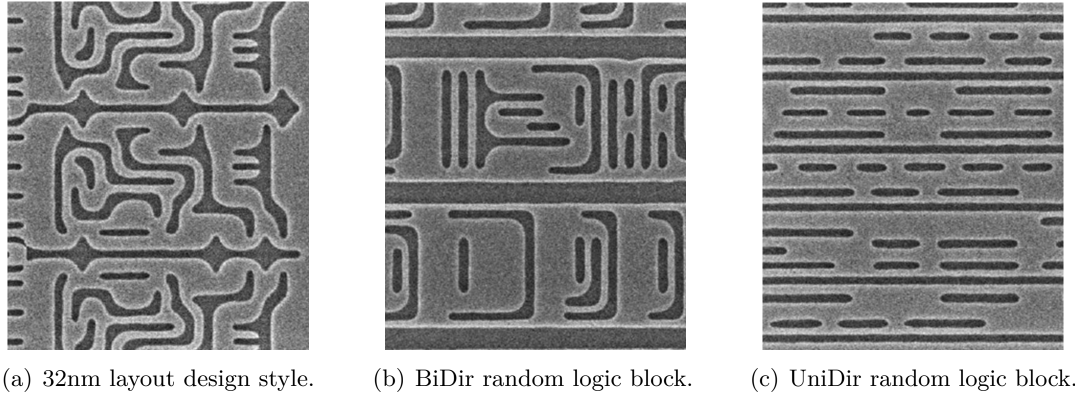


(a) FinFET unidirectional fabric (UniDir).

(b) FinFET bidirectional fabric (BiDir).

Figure 2.16: Layout examples showing finFET based implementations [49]. The layer mapping is as follows: (green) active fins; (pink) poly; (purple) local interconnect CA; (green) local interconnect CB; (red) via0; (blue, yellow) metal1.

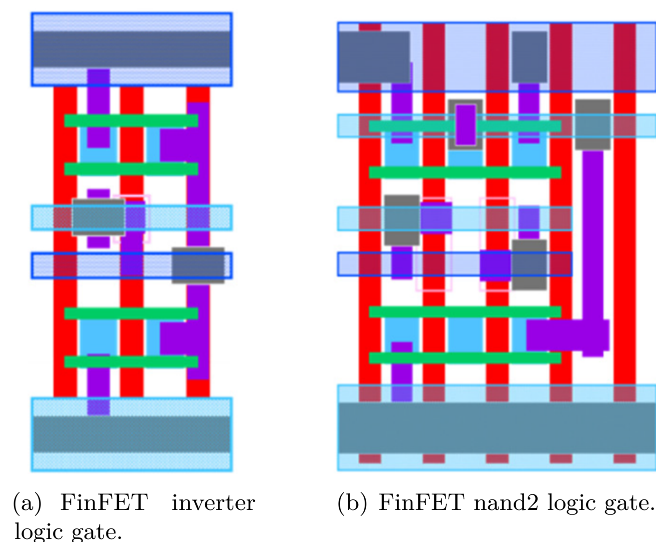
Vaidyanathan et al. compare the lithography impact of a 32nm layout design style with respect to the 14nm fabrics proposed using scanning electron microscope (SEM) images [49], as detailed in Figure 2.17. The BiDir fabric which employs a limited set of metal1 patterns shows a better pattern fidelity than a traditional random metal1 design style, although there is still a large amount of variation on the corner shapes. On the other hand, the UniDir fabric presents the best printability results. As more regularity is applied, better printed image is obtained for the 14nm technology node and thus justifying the need of layout regularity.



(a) 32nm layout design style. (b) BiDir random logic block. (c) UniDir random logic block.

Figure 2.17: SEM pattern images for a 32nm and 14nm technology nodes [49].

Lastly, another recent layout analysis of finFET devices for a 14nm technology node can be found in [26]. The authors study different layout implementations using regular and non regular metal1, varying the number of fins inside the cell or applying different strategies to use the interconnect layers. Then, based on the TEASE evaluation framework, previously detailed in section 2.1.4, they provide an optimized finFET template combining the benefits of the different layout strategies proposed, as shown in Figure 2.18. This layout template employs metal1 with jogs, but with a limited number of occurrences.



(a) FinFET inverter logic gate. (b) FinFET nand2 logic gate.

Figure 2.18: Layout examples showing finFET based implementations [26]. The layer mapping is as follows: (green) active fins; (red) poly; (light blue) local interconnect CA; (purple) local interconnect CB; (black) via0; (dark blue) metal1.

Concluding, a priori this dissertation can be more easily extended in the FDSOI direction rather than in the finFET direction. Although the different metal1 configurations provided in this thesis can be also applied to finFET designs. The regular gridded layout design styles proposed in this dissertation employ transistors with a discrete transistor size and thus they can be easily extended to finFET devices by only adding the local interconnect layers.

2.4 Conclusions

Several studies have addressed the lithography variability implications on layout design, as widely detailed throughout this chapter. Although a lot of research challenges still remain open in order to outperform line-pattern resolution on current and future technology nodes. These challenges can be categorized in three main areas: analysis, evaluation and design.

Lithography printability on layout patterns must be properly analyzed using lithography simulations in order to predict line-pattern distortions, especially, those litho-induced variations causing excessive channel length degradation. Hence, a comprehensive study on the lithography effects associated to different layout pattern configurations and a more exhaustive gate length configuration methodology considering several kind of variations must be proposed.

In order to better propose new layout configurations, comprehensive evaluation metrics must be provided. Layout metrics to assess the complexity of the different geometric patterns used in a layout are necessary to more precisely evaluate a design. Moreover, a yield estimation metric combined with lithography simulations must be also employed to more accurately capture the lithography induced variations suffered due to the pattern configuration utilized. Lastly, to the best of author's knowledge, the lack of a single layout quality metric in the literature to properly compare different layout strategies, makes it difficult to decide the best layout design configuration considering several evaluation aspects. Therefore, new metrics must be proposed in order to better illustrate the potential benefits of regular layouts.

Combining the study of the lithography effects and the evaluation frameworks, new layout designs can be provided justifying the need of layout regularity to combat lithography induced variations. Regular layouts simplify the layout patterns by completely eliminating all complex two-dimensional geometries that could lead to yield losses. Consequently, regular designs present an undoubtedly improved patterning robustness, hotspot reduction, variability improvement and design simplicity. The lithography printability and cost benefits of ultra regular layouts are undoubtedly, however the excessive overhead in terms of power, performance and area suggests that some regularity trade-offs must be considered in order to obtain more competitive results. Hence, a regular implementation that follows a rather similar layout configuration compared to a standard cell design, but using one-dimensional features is a more efficient strategy despite not following the simplest layout design configuration.

Concluding, regular designs can be competitive in the near future compared to traditional 2D standard cell designs in terms of area and yield. Several companies and research groups have proposed different regular implementations that lead to significant area reduction

compared to full regular layouts, but not too many details are provided about the degree of layout regularity applied in each layout design. Hence, regular layouts still must be further investigated to properly configure the degree of layout regularity to outperform the trade-off between area, yield, power, performance and pattern complexity among other metrics, i.e., the trade-off among all the aspects that define the layout quality of an IC design.

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3

Modeling Lithography induced Variations in Layout Design

As technology advances into the nanoscale era, one major source of circuit degradation comes from lithography printability variations. Regular layouts have been proposed in the literature to overcome the increasing number of layout dependent effects. However, despite the undoubted manufacturability benefits of layout regularity, several lithography induced-variations are still present in the layout and they must be properly capture in order to outperform line-pattern resolution. The main objective of this chapter is to highlight several common imperfections caused by sub-wavelength photolithography that affect both functionality and performance of layout designs.

Regular layout design guidelines are derived from lithography simulations so that several important lithography related variation sources are minimized. Furthermore, the geometrical constraints of new regular cell structures, referred as Adaptive Lithography Aware Regular Cell (ALARC), that minimize these manufactured distortions and improve design predictability are presented. The ALARC templates proposed are created to illustrate the main benefits and weaknesses when considering the layout design guidelines provided. Lastly, printability, area, delay and power analysis of a common AND2 logic gate are performed in order to evaluate the characteristics of the regular templates proposed.

The lithography imperfections have a direct impact on transistor channel length of devices and even for regular designs, the gate length must be appropriately configured to not jeopardize the electrical characteristics of a cell design. This chapter proposes a design level methodology, referred as gate biasing, to overcome systematic layout dependent variations, across-field variations and the non-rectilinear gate effect (NRG) applied to regular layouts by properly configuring the drawn transistor channel length. The gate biasing technique is applied to an AND2 logic gate and delay and power evaluation is performed to illustrate the impact of lithography variations on layout design.

In order to model lithography perturbations and identify places in a layout where optical effects may affect functionality, a Calibre Litho-Friendly Design (LFD) [1] rule deck provided by North Carolina State University (NCSU) based on an open-source 45nm technology Physical Design Kit (FreePDK45) [2] is used. Note that the version of the base-kit employed in this chapter is the 1.3 and the version of the lithography simulation kit and the optical models used for the lithography simulations (LithoSim kit) is the 1.1, both from 2009.

This PDK uses a Predictive Technology Model (PTM) that provides customizable and predictive model files for future transistor and interconnect technologies. Note that in the provided LFD deck, only *active*, *contact*, *poly*, and *metal1* layers are currently supported,

which correspond to the smallest features in this technology. Nevertheless, in order to obtain a more accurate lithography simulation, *metal2* and *via1* PV-band layers (lithography process variation band) have been also added into the LFD deck. In order to do so, the information of the *metal1* PV-band is used to create the *metal2* PV-band and similarly the *via1* PV-band is obtained considering in this case the *contact* PV-band. Additionally, note that only two PV-bands for two different process conditions which represent the maximum and minimum edge displacement considering different across-field variations (dose and focus variations) are employed.

The last important aspect to highlight is that the electrical characterization is performed using the lithographic channel length predictions obtained with Calibre LFD 2007 version from Mentor Graphics [1]. In this Calibre version, the printed channel length obtained is only suitable for delay and energy calculations considering the Ion, as explained in [4]. Since Ion and Ioff currents of a transistor normally have different sensitivities to channel length variations, a different effective gate length for timing and leakage must be employed. Therefore, for leakage calculations which are computed using the Ioff current, another value of the printed channel length must be considered according to the literature [5, 6]. However, using two gate lengths for simulation is less practical and therefore a single gate length model more suitable for characterization that combines the gate length models of the Ion and Ioff currents are proposed [7, 8]. According to [4], more recent versions of the Calibre LFD tool uses a calibration table (LUT) that outputs a channel length that is good for both Ion and Ioff calculations. Concluding, the leakage results shown during this chapter will not be accurate, even though results are sufficient to illustrate the layout design methodologies.

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3.1 Lithography effects on regular layout designs

The manufacturability benefits of regular layouts are based on their lower sensitivity to lithography distortions, however a regular design does not directly imply that all lithography imperfections have been eliminated. In this section, this assertion is illustrated through lithography simulations, outlining the effects of some lithography perturbations and how to correct them or at least how to mitigate their undesirable effects. Based on common layout situations where these optical effects are highlighted, the potential lithography constraints that have to be taken into consideration during the design stage to minimize lithography variations are here depicted. Observe that the designer must decide the trade-off between area penalty and lithography accuracy.

3.1.1 Isolated gates: gate narrowing effect

At sub-wavelength transistor size with small Rayleigh k_1 lithography factor, the line-width is critically determined by its proximity to neighboring lines, i.e., the pattern density across the chip. This proximity might benefit or deteriorate the line-width of layers and thus causing the phenomenon commonly called across-chip line-width variation (ACLV) which results in systematic yield losses. Spacing between shapes belonging to the same layer must be properly adjusted to reduce the ACLV. More specifically, printed transistor channel length depends on the distance of adjacent poly-silicon stripes and besides the expected channel length degrades rapidly with this distance directly affecting delay and leakage power consumption. A set of lithography simulations has been performed in order to show the amount of channel narrowing due to this effect, as depicted in Figure 3.1.

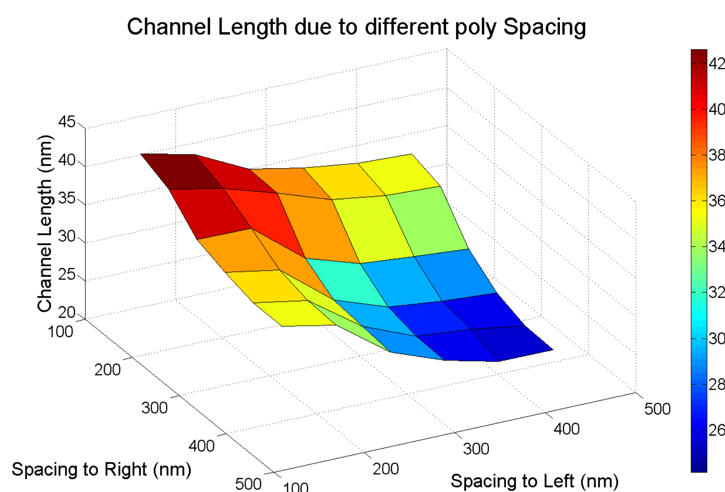
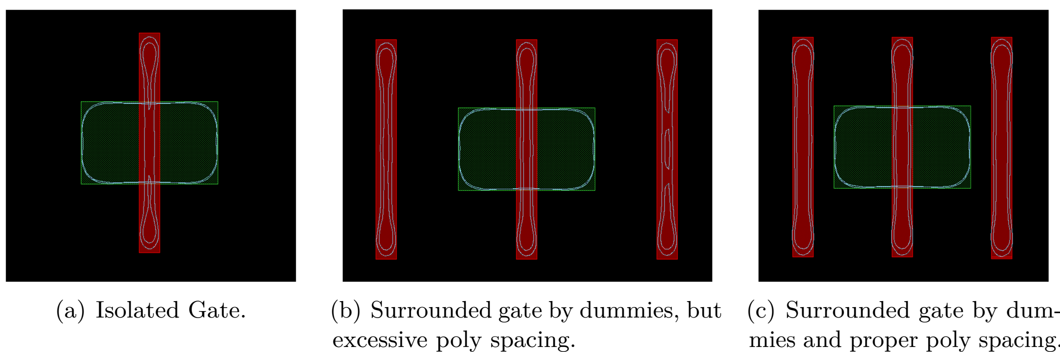


Figure 3.1: Lithography simulations illustrating that transistor channel length significantly degrades with respect to the distance to contiguous neighbors.

Analyzing the poly spacing from the point of view of isolation, i.e., the poly gate isolation problem, two cases might occur to consider that a gate is isolated: (1) gates that are not surrounded side by side by poly lines (a transistor placed at the end of an active region) or (2) excessive spacing between contiguous poly lines. Both situations produce the gate narrowing phenomenon; the poly line width variation is highly incremented all along its length dimension.

In the first case, the gate narrowing problem can be solved by adding dummy poly lines and by properly adjusting the spacing between poly gates. While the use of dummy elements may in principle imply an excessive penalty in area, this is not necessarily the case when all lithography constraints are jointly considered. In the layout designs presented along this chapter, the area penalty is minimal since other cell constraints give almost enough room to place the dummy poly lines. Hence, a dummy poly line has to be placed at both ends of each active region in order to avoid the undesirable gate narrowing. Finally, observe that a dummy poly line can be shared by two consecutive active regions.

In the second case, poly lines must be equally spaced as a requirement in regular designs and poly spacing must be properly established as the minimum poly spacing that satisfies all the design rules and lithography constraints. Observe from Figure 3.1, the importance of using poly-silicon gates to be equally spaced so lithography variations will affect similarly to each gate and thus justifying the need of layout regularity. Figure 3.2 depicts a layout example of regular poly gates with and without dummy poly lines and properly and not properly spaced. Lithography simulations clearly reveal that using dummy poly lines and properly spacing poly gates, transistor gate length variation is reduced. Consequently, it is obtained much more control of the transistor channel length and better predictability of the leakage power consumption.



(a) Isolated Gate.

(b) Surrounded gate by dummies, but excessive poly spacing.

(c) Surrounded gate by dummies and proper poly spacing.

Figure 3.2: Gate narrowing perturbation due to isolated gates.

3.1.2 Contacts and vias: non-enclosure effect

Despite the line-pattern resolution of a layout feature might be satisfied even though its printed shape is slightly hampered, it might happen that the combination of two different patterns causes a lithography distortion. This phenomenon is rather critical for contacts and

vias that might fall outside the layer placed below or above them, if contacts and vias are not properly enclosed. Next several cases where the contact and via enclosures might fail if the layout is not properly configured are enumerated.

1. *Diffusion Contacts*: Source/Drain (SD) contacts must be properly enclosed by the active region in order to avoid them to fall outside the oxide strip. For this reason, the active region must be sufficiently extended all along the SD contact, except one edge thereof that can be minimally extended (10nm), as depicted in Figure 3.3.
2. *Poly contacts*: Poly contacts must be perfectly surrounded by the poly region extension created for this connection to enhance the reliability of the input connection. This enclosure must ensure that contacts do not fall outside the poly region and it must be the minimum necessary, firstly to minimize the area penalty due to the minimum spacing required between contiguous poly features and secondly to minimize the irregularity caused by the gate enclosure with respect to the poly channel. Contacts are printed inside the poly region by setting the poly around contact enclosure as 10nm.
3. *Vias*: Metal lines must be wide enough so vias do not fall outside the metal layers. The metal enclosure around contacts and vias in metal routing tracks must be at least 5nm bigger, which implies that the metal width must be bigger than the minimum to ensure via reliability.
4. *Power rail vias*: When connecting the power rails using a via, the via might extend outside the power rail if it is placed at the boundary of the power supply connection despite its wide wire width. 5nm of metal enclosure around vias are not enough for wide wires and at least 10nm of enclosure are necessary in this technology. In order to avoid this problem, vias can be connected on top of the substrate contacts, i.e., centered with respect to the power supply rail so vias will be inside the power supply.

Figure 3.3 depicts the four cases previously outlined that evince the non-enclosure effect and additionally it shows how to modify the layout design to mitigate this distortion.

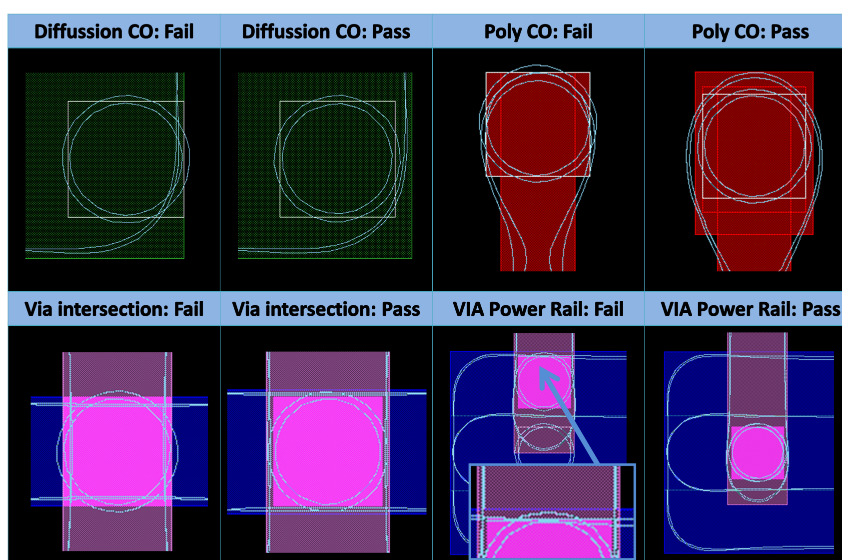
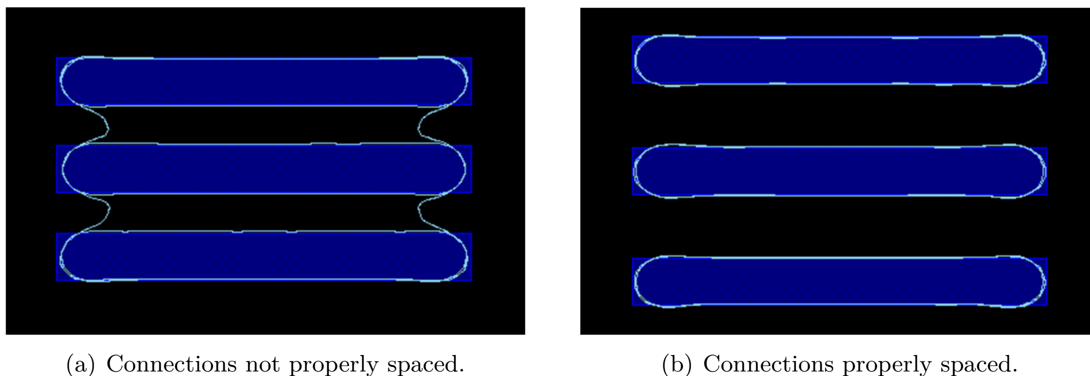


Figure 3.3: Four occurrences where the non-enclosure effect is evinced.

3.1.3 Metal layers: proximity effect

The proximity effect is the lithography perturbation caused by the lack of space between two elements in the same layer. Metal connections are likely to suffer this perturbation if spacing is not properly adjusted. Recalling section 3.1.2, it was detailed that the width of metal layers should be bigger than the minimum to avoid contacts and vias to fall outside the metal. Thus, augmenting the metal width requires an increase of the spacing between metal lines in order to avoid shorts between contiguous metal lines as they may be printed together due to its proximity. Figure 3.4 depicts how shorts are produced between contiguous metal1 connections if spacing between lines is not properly set. Note that, the increase in spacing causes an increase of the vertical cell pitch and thus in area. Finally, this distortion is analogous for metal2 connections.

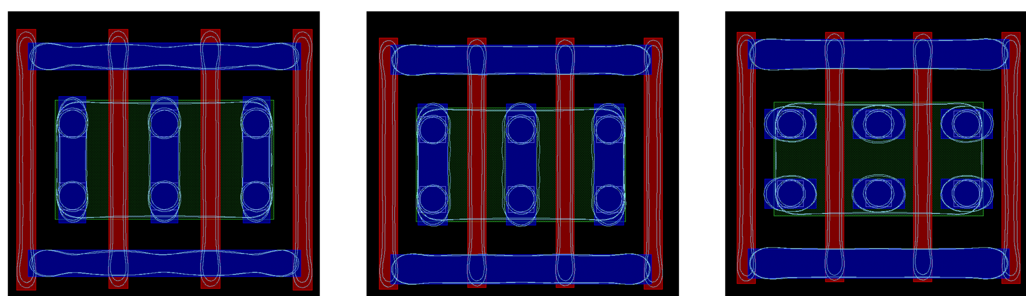


(a) Connections not properly spaced. (b) Connections properly spaced.

Figure 3.4: Proximity effect which causes shorts between contiguous metal lines.

Metal connections are likely to suffer from other proximity effects if spacing, size and placement are not set properly. Figure 3.5 depicts different strategies to connect the metal1 layer which evinces the proximity effect. In Figure 3.5(a), it is shown a weakened metal line more likely to pinch due to the *undulating-line* effect caused by the sharp metal1 shape used to create a SD connection. In this case, metal1 connections are horizontal for intra-cell routing and vertical for diffusion contact enclosures. This perturbation affects the interconnect reliability causing either a broken wire or an increase on the expected wire resistance and thus the electrical behavior of devices might be off target. This phenomenon occurs if the metal1 lines are drawn with minimal width, although this distortion is almost negligible if the wire width is augmented in order to avoid the non-enclosure effect, as stated in the previous section. Figure 3.5(b) illustrates the lithography improvement achieved by augmenting the wire width of metal connections.

A more regular implementation is illustrated in Figure 3.5(c) that completely solves this perturbation and simplifies the metal1 layout patterns by employing all metal1 wires horizontally. In this case, metal1 lines suffer a *line-end pullback* due to the proximity of metal1 lines from contiguous SD contacts, although lithography requirements, such as contact enclosures, are still verified.



(a) Layout design version 1: minimum metal width and vertical contact enclosures.
(b) Layout design version 2: wider metal wires and vertical contact enclosures.
(c) Layout design version 3: wider metal wires and horizontal contact enclosures.

Figure 3.5: (a) Metal connections suffer the undulating-line effect; (b) almost negligible undulating-line effect; (c) metal connections suffer a line-end pullback.

3.1.4 Poly contacts: channel narrowing

Poly contacts are the only 2D feature permitted in the design. This irregularity is mandatory because the poly channel is narrower than the poly extension needed to create a contact. Note that this 2D shape may cause a narrowing in the channel region if the poly contact enclosure is not properly designed and placed. The channel narrowing effect increases the transistor threshold voltage and reduces its current driving capability. To maintain the desired channel length all along the channel region the following guidelines must be considered.

Firstly, the shape of the poly contact enclosure should be rectangular, aligned with the poly shape and avoiding an abrupt change in poly width which causes *bottlenecking*. The minimum width of the poly enclosure is established as the minimum width that ensures the connectivity of inputs, as previously detailed in section 3.1.2. In current cell designs, this perturbation is alleviated by using Optical Proximity Correction (OPC); OPC is used to correct systematic and stable within-field patterning distortions caused by proximity effects to minimize the ACLV. For instance, OPC utilizes small features to make smoother an abrupt change between shapes belonging to the same layer. In standard cells, poly lines are dramatically hampered due to its irregular shape and thus a vast OPC effort is required. Thus, taking advantage that all gates in a regular design have the same enclosure, in order to maximize regularity, small poly features can be added to create the poly enclosure during the design stage and thus a considerable amount of time during the OPC stage can be saved since this distortion would be already corrected. Figure 3.6 illustrates different poly shapes that evince the bottlenecking problem. The shape that achieves a lower gate narrowing is the enlarged poly enclosure with the extra small poly features (shape C).

The poly gate length can be drawn bigger than the minimum in order to reduce the channel length variations and thus leakage power is also decreased. In this case, the wider poly gate length fully corrects the bottlenecking distortion. For instance, the gate length can be drawn at 60nm instead of 50nm and thereby the channel length variation is mitigated, as depicted in Figure 3.6 (shapes D and E).

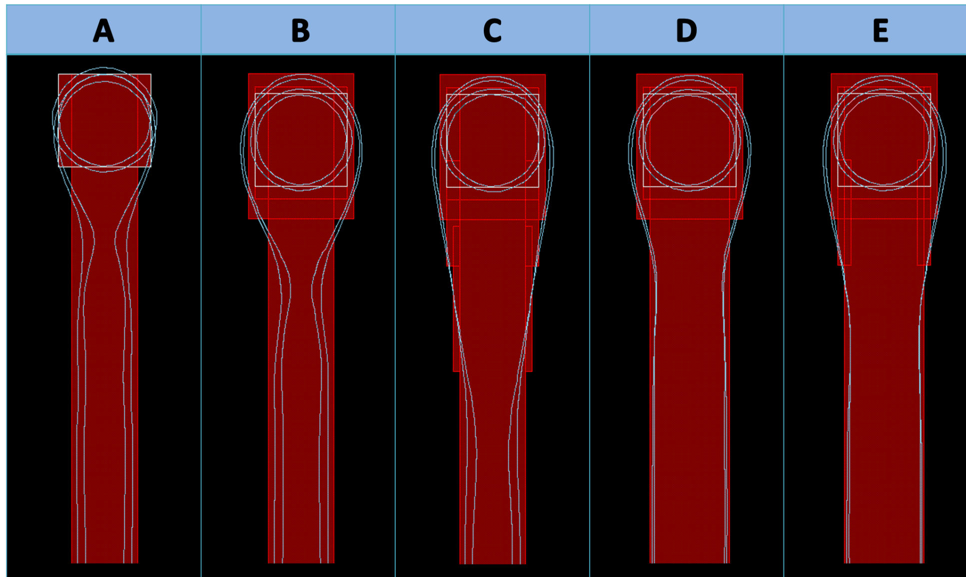


Figure 3.6: Different types of poly enclosure. (A) Minimum poly enclosure; (B) enhanced poly enclosure; (C) enhanced poly enclosure plus systematic correction; (D) enhanced poly enclosure for gates drawn at 60nm; (E) enhanced poly enclosure for gates drawn at 60nm plus systematic correction.

Secondly, the number of poly contacts in the cell design must be minimized to diminish the number of poly irregularities. For instance, in case of dual-network topologies, the Euler-path method (or sub-Euler-paths) serves as a good method to obtain a gate ordering that produces a small layout area to which the pull-up and the dual pull-down network have an identical ordering of input labels. Hence, besides the advantage of simple routing of signals, and correspondingly, more compact layout area and smaller parasitic capacitance, both networks can share the same poly gate and hence only one poly contact is required.

Thirdly, poly contacts are preferably placed at the ends of the poly gate to avoid the double narrowing/widening effect. In that case, the narrowing/widening would only affect toward one direction, as shown in Figure 3.7 (region 1). As a disadvantage, accessing the poly-silicon gates from the ends of the poly might cause a different delay to switch on the PMOS and the NMOS, switching on firstly the closer transistor to the poly contact. Hence, this constraint must be omitted whether this delay is significant or when the routability is prohibitively difficult (excessive wire-length or oversized cell area) at the cost of larger variations.

Fourthly, although the previous irregularities are alleviated, they are not completely eliminated and thus the poly contacts still affect the channel region if they are not properly located. Poly contacts must be placed sufficiently far away from the active region so the channel narrowing can be avoided; a narrowing in the poly line is undesirable, but it is highly more harmful to have this irregularity inside the active region than outside. Thereby, channel length degradation is minimized (apart from random perturbations) by moving the poly contacts further away from the diffusion strip, as highlighted in Figure 3.7 (region 2).

Finally, the poly gate end without a poly contact suffers from line-end rounding. Hence, the poly extension on the active area must be larger than the minimum specified by design rules to correct this channel length distortion, as shown in Figure 3.7 (region 3). Thereby,

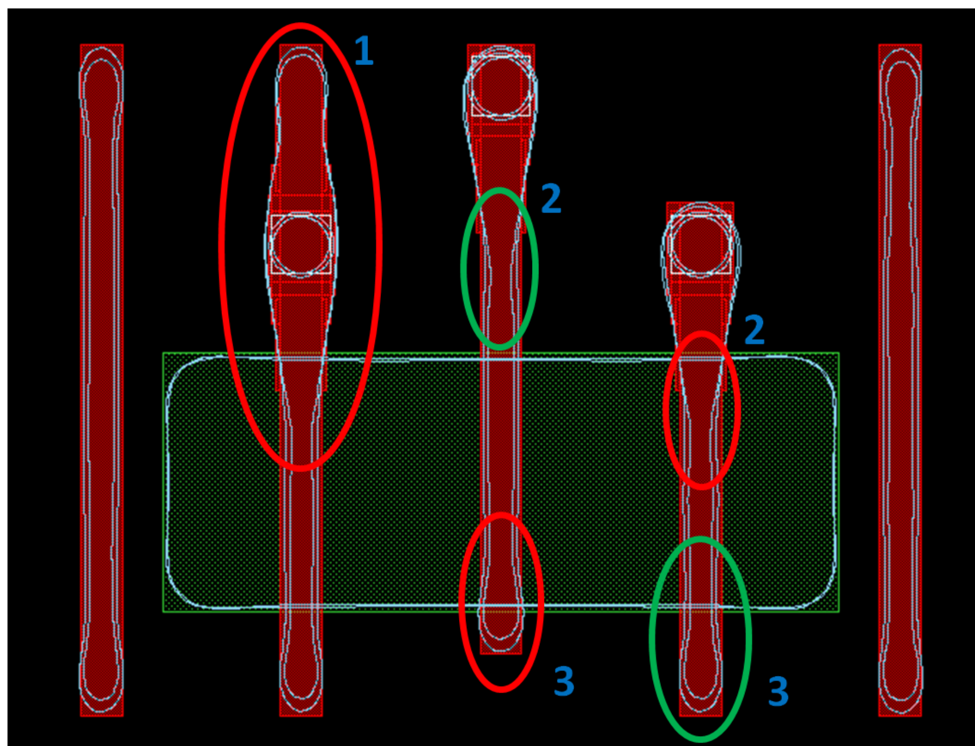


Figure 3.7: (1) Double narrowing/widening effect; (2) channel narrowing perturbation; (3) poly line-end rounding causing channel width variations.

the channel length can be completely regular, i.e, the channel does not suffer systematic lithography variations and voltage threshold and leakage variations can be minimized.

Take into account that some of these constraints are subjected to the technology and the lithography estimation tool employed. Hence, the important idea to remark is that lithography determines several layout features. Each designer must adjust these constraints (such as poly enclosure) to minimize litho-perturbations and maximize circuit yield for the specific technology.

3.1.5 Outline of the layout design guidelines to combat the lithography effects

A brief summary of all the previous lithography constraints that must be taken into account during the design stage to reduce lithography variations is outlined next.

1. Channel length line-pattern resolution.

    a) Gates must be surrounded side by side by other poly lines to minimize the gate length narrowing.

    b) All diffusion strips must be surrounded side by side by dummy poly lines.

c) Drawn gate length becomes directly dependent on poly gate spacing and thus poly lines must be equally spaced so systematic poly-induced variations affect equally throughout all poly lines (regularity constraint).

d) An excessive poly pitch between contiguous poly lines dramatically augments the gate length degradation and thus poly pitch must be properly specified.

2. Contact and via enclosures.

   a) *Diffusion Contacts*: SD contacts must be properly enclosed by the active region in order to avoid them to fall outside the oxide strip.

   b) *Poly contacts*: Poly contacts must be perfectly surrounded by the poly region extension created specifically for this connection to enhance the reliability of the input connection.

   c) *Vias and contacts*: Metal lines must be wide enough so vias and contacts do not fall outside the metal layers.

   d) *Power rail vias*: Wider metal lines, e.g., the power supply rails, require a wider enclosure to avoid vias falling outside the metal layer. In order to avoid this problem, vias can be connected centered with respect to the power supply rail so vias will be perfectly enclosed.

3. Metal connections.

   a) All metal shapes are unidirectional in order to avoid the corner rounding distortion or pinching due to sharp shapes.

   b) As metal width increases, lower is the degradation suffered due to pinching of sharp shapes.

   c) Spacing must be properly designed in order to avoid shorts between contiguous metal lines.

   d) Metal lines must be equally spaced in order to first maximize regularity and second to ease routability.

4. Input placement.

   a) The shape of the poly contact enclosure should be rectangular, aligned with the poly shape and avoiding an abrupt change in poly width which might cause the poly gate to pinch.

   b) The number of poly contacts must be minimized in order to decrease the number of poly irregularities.

   c) Poly contacts are preferably placed at the ends of the poly gate to avoid the double narrowing/widening effect.

   d) Inputs should be placed far enough from the active region in order to obtain a regular line-pattern resolution in the channel region.

   e) The poly gate end without a poly contact should be sufficiently extended so the line-end rounding will fall outside the active region.

3.2 Impact of the lithography effects on layout design

A regular litho-friendly design presents an undoubted advantage compared to traditional standard cell designs; the effort of resolution enhancement techniques such as optimal proximity correction (RET-OPC) is dramatically reduced since all lithography imperfections can be fast identified and corrected during the creation of the cell design template. In this section, the layout design guidelines that must be jointly considered to minimize lithography perturbations are mapped into different layout design templates. These regular templates are analyzed in terms of area, lithography printability, delay and power in order to evaluate the potential benefits and weaknesses of regular layouts.

3.2.1 Regular layout design templates (ALARC) to compensate litho-effects

Regular designs tend to be rather similar at first glance, for instance, all regular designs contain unidimensional poly gates. The difference between regular design styles lies in small details that configure and determine the characteristics of the cell. Adaptive Lithography Aware Regular Cell (ALARC) structures that takes into account the lithography constraints previously outlined are presented next.

The main objective of this regular gridded layout strategy is to reduce lithography perturbations, generating cells that are DRC clean by construction. This is achieved by confining the allowed layout patterns to a subset of patterns and by defining a cell grid that implicitly respect all the design rules. Note that, the ALARC templates are structurally similar to a standard cell approach, attempting to give more versatility to implement any kind of logic function than a regular transistor array, detailed in section 2.2.3. The common characteristics of the ALARC structures are described next.

1. All NMOS transistors lie in a single row near the bottom of the cell and all PMOS transistors lie in a single row near the top of the cell.
2. Active regions can contain any number of equal width transistors, but each diffusion strip can have a different transistor width.
3. All contacts, vias, poly-silicon and metal wires should be placed on the routing grid.
4. Poly-silicon gates are 1D layout features equally spaced and equally surrounded.
5. Dummy poly-silicon lines are placed between different active regions and at the cell boundaries.
6. The cell height of each cell template is defined based on the routing resources required to route a DFFRS cell using the available routing layers and allowed directions and the specified lithography constraints.
7. Power rails are created in the metal1 layer and displaced half track with respect to the last routing track.

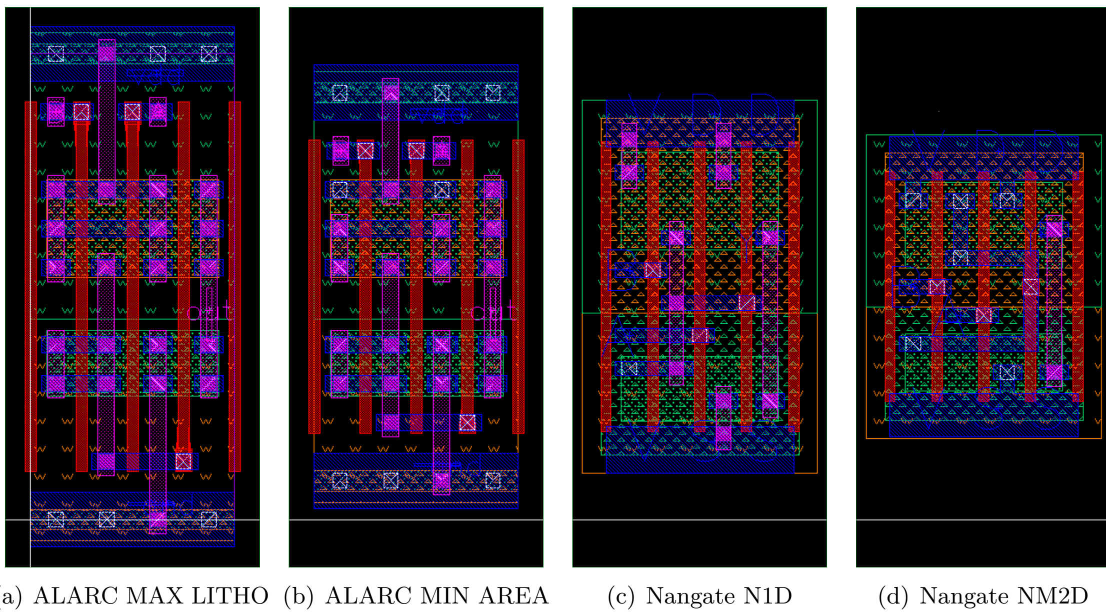
8. Metal1 lines are used for horizontal connections and metal2 for vertical ones.
9. Substrate or polarization contacts (used to connect the bulk of transistors to the power supply) are placed over the power supply rails.
10. Metal wire width is set to compensate the lithography effects detailed in section 3.1.
11. Poly-silicon gates can be set from 50nm to 60nm in order to compensate channel length variations, as justified in the electrical analysis in section 3.2.4. Moreover, a channel length optimization methodology is described in section 3.3.

By considering all the previous characteristics, two regular cell architectures are defined to optimize different cell parameters. The *ALARC MAX LITHO* takes lithography constraints to the limit to enhance at maximum line-pattern resolution. On the other hand, the *ALARC MIN AREA* aims to minimize cell area penalty by alleviating lithography constraints. The differences between these two ALARC variants are detailed next.

1. **ALARC MAX LITHO**.
   a) The number of cell tracks specified is 12.
   b) Inputs must be placed at the ends of poly-silicon gates.
   c) The minimum spacing between a poly-silicon-input connection and its respective active region is established as 260nm. This is equivalent as not allowing any active region on the closest horizontal routing track from any poly-silicon contact.
   d) Poly-silicon contact enclosures are optimized to completely wipe out the narrowing/widening suffered inside the channel region.
2. **ALARC MIN AREA**.
   a) The number of cell tracks configured is 10.
   b) Inputs are preferably placed at both ends of poly-silicon gates, although they may be placed in any other location except over the channel.
   c) The spacing restriction between poly-silicon contacts and active regions can be omitted only if routability is not satisfied otherwise.
   d) Poly-silicon contact enclosures depend on the spacing with respect to the active region. Thus, when the previous spacing restriction is not verified, an alternative enclosure is used that reduces the channel narrowing/widening distortion.

Figure 3.8 depicts an implementation of both ALARC design templates. Two other layout designs from Nangate are also shown to illustrate the area overhead of the ALARC templates. Further details about the Nangate templates are detailed in section 3.2.2.

Cell size of the ALARC structure is determined by the minimum horizontal and vertical pitches that satisfy design rules, enable the vertical routing grid to be equally spaced and verify all lithography constraints. Thereby, the horizontal pitch (P_X) is determined by the combination of the following constraints: (1) active region extension from contact, established in the ALARC structure as 10nm (CO2OD); (2) poly to active region spacing set to 50nm (PO2OD); (3) equally spaced metal2 connections and; (4) equally spaced poly lines. Figure



(a) ALARC MAX LITHO (b) ALARC MIN AREA (c) Nangate N1D (d) Nangate NM2D

Figure 3.8: AND2 logic gate designed following ALARC and Nangate templates.

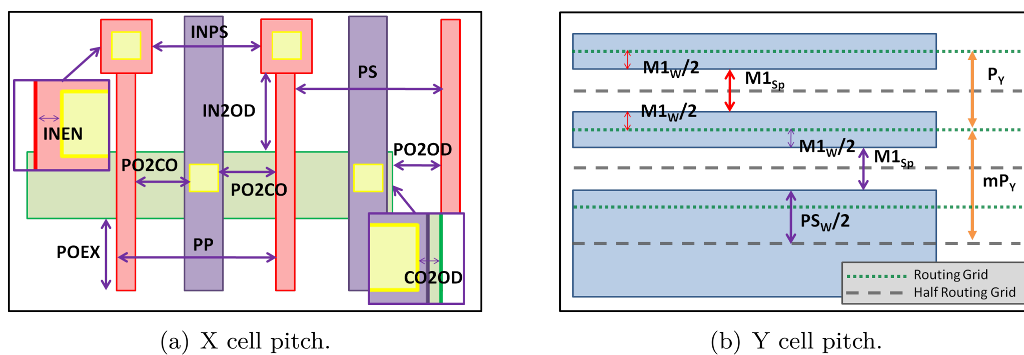
3.9(a) illustrates how these design rules are implemented in the ALARC cell. The horizontal pitch P_X corresponds to the metal2 pitch which by construction is equal to the poly pitch PP of the cell, as detailed in Equation 3.1.

$$P_X = PP = PS + L = 2 \cdot PO2CO + CO_W + L \tag{3.1}$$
$$PO2CO = PO2OD + CO2OD$$

The vertical cell pitch is ascertained by the minimum pitch that ensures that vias and contacts are properly enclosed by metal1 lines and at the same time avoids the metal1 proximity effect. Expression 3.2 shows how to compute the vertical cell pitch (P_Y).

$$P_Y = M1_W + M1_{Sp} \tag{3.2}$$

Figures 3.9(a) and 3.9(b) show how these design rules are implemented in the ALARC templates and Table 3.1 lists all parameters necessary to compute the cell pitches.



(a) X cell pitch. (b) Y cell pitch.

Figure 3.9: Design rules that determine the ALARC cell size.

Table 3.1: Cell size parameters where X represents that this rule is not established in the design rule deck (DRC) and some values varies depending on the channel length specified. Note that the $INEN$ rule only applies to the ALARC MAX LITHO.

Design rule (nm)	**Acronym**	**Minimum DRC rules**	**ALARC rules**
Poly pitch	$PP = P_X$	190	240/250
Poly spacing	PS	140	190
Input poly spacing	$INPS$	140	150/160
Poly gate length	L	50	50-60
Minimum poly extension	$POEX$	55	140
Gate poly to contact spacing	$PO2CO$	35	60
Poly to active spacing	$PO2OD$	50	50
Enclosure of poly around contact	$INEN$	0	10
Enclosure of poly around active	$CO2OD$	0	10
Poly input to active spacing	$IN2OD$	X	260
Vertical pitch	P_Y	130	190
Metal1 width	$M1_W$	65	80
Metal1 spacing	$M1_{Sp}$	65	110
Metal2 width	$M2_W$	70	80
Metal2 spacing	$M2_{Sp}$	70	160
Power supply width	PS_W	70	270

The power supply rails are equally spaced with respect to metal1 connections and they are displaced half track from the routing grid in order to increase its wire width. Power supply lines should be wider than metal1 connections in order to decrease its wire resistance and thus the IR drop is reduced. Figure 3.9(b) illustrates how the power supply is placed on the ALARC templates and Equation 3.3 shows how to compute its wire width.

$$PS_W = 2 \cdot (m-1) \cdot P_Y + M1_{Sp} \;\; | \;\; (2m-1) \; \in \; \mathbb{N} \tag{3.3}$$

where the parameter m is established as 1.5 in order to reduce the IR drop compared to a thin wire, but without excessive area penalty.

Table 3.1 shows the parameters that configure the ALARC cell templates and its minimum value according to the design rules. ALARC values are the minimum necessary to satisfy all ALARC lithography constraints, although these rules can be alleviated depending on the design requirements. Finally, the employment of either the *MAX LITHO* or the *MIN AREA* template depends on the designer; the limit between area penalty and lithography accuracy varies according to the overall circuit requirements.

3.2.2 Area impact analysis of the ALARC templates

Area overhead is one of the major concerns when analyzing regular design approaches. Two different gridded cell architectures from Nangate are employed to analyze the area impact

of the ALARC templates previously outlined. These gridded cell architectures created also using the FreePDK45 technology [2] represent a trade-off between layout regularity and cell density. Note that these templates are different from the ones detailed in section 2.2.4, since these ones are created using the FreePDK45 technology. The main aspects that these Nangate templates have in common are detailed next.

1. Characteristics from 1 to 7 of the ALARC templates also applies to the Nangate designs.
2. Substrate contacts are not placed inside the logic gates and require special cells to placed them.
3. Poly-silicon, metal1 (with the exception of power rails) and metal2 wires have always the minimum allowed technology width.
4. The horizontal cell pitch is defined as the minimum pitch that satisfies design rules and enables the vertical routing grid to be equally spaced.

Taking into account all the previous outlined specifications, two design templates with a different degree of layout regularity are proposed. The Nangate NM2D that employs metal1 bidirectional with jogs in order to minimize area penalty and the Nangate M1D that only uses layout features unidimensional. Both designs do not consider the lithography constraints of the ALARC templates and thus these layout configurations suffer more printability variations. The different characteristics of these templates are described next.

1. ***Nangate 9 tracks (NM2D)***
    a) The number of cell tracks configured is 9.
    b) The metal1 layer is used for both horizontal and vertical routing.
    c) The metal2 layer is used for vertical connections only.
    d) Inputs are placed in two rows between the NMOS and PMOS transistors.
    e) The vertical cell pitch is defined in such a way that two horizontal metal1 wires can be placed in adjacent rows with the same x coordinates.
2. ***Nangate 10 tracks (N1D)***
    a) The number of cell tracks specified is 10.
    b) The metal1 layer is used for horizontal connections only.
    c) The metal2 layer is used for vertical routing only.
    d) Inputs are placed in three rows between the NMOS and PMOS transistors.
    e) The vertical cell pitch is defined in such a way that two vias can be placed in adjacent rows with the same x coordinate.

Figure 3.8 depicts an AND2 logic gate implemented using the ALARC and the Nangate templates which qualitatively evinces the area penalty of the ALARC cells (all cells are equally scaled). Table 3.2 shows an area comparison of two representative common logic functions, an AND2 and a DFFSR logic gates, in order to analyze quantitatively the area overhead of the ALARC templates. These designs are compared with respect to cells created using a real commercial 40nm technology node. Note that the area results are normalized with respect to the Nangate NM2D design.

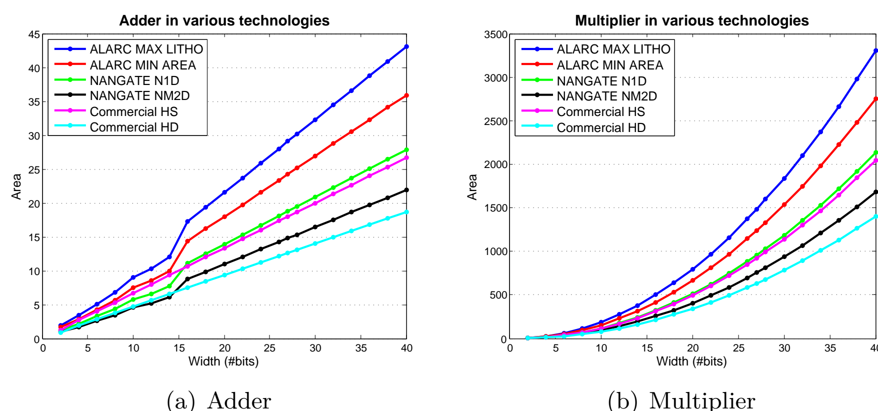
Table 3.2: Cell area comparison between different designs for an AND2 and a DFFSR logic gates.

Architecture	**AND2**	**DFFSR**	**Tracks**	**Pitch X**	**Pitch Y**
Nangate NM2D	1	1	9	230	140
Nangate N1D	1,27	1,27	10	230	160
ALARC MAX LITHO	1,97	1,97	12	250	190
ALARC MIN AREA	1,64	1,64	10	250	190
Commercial HS (High Speed)	1,22	1,11	9	-	-
Commercial HD (High Density)	0,97	0,99	14	-	-

The area impact of using all regular features for Nangate N1D is about 27% with respect to Nangate NM2D. This area penalty is mainly caused by the employment of unidimensional metal1 shapes and the increase in the vertical cell pitch and number of tracks. Observe that Nangate N1D has up to 30% area penalty when comparing it to the Commercial HD, although Nangate NM2D architecture does not have any area overhead. When considering lithography effects to enhance circuit printability, the area overhead augments up to 64% for the ALARC MIN AREA compared to both Nangate NM2D and Commercial HD. This overhead is related to the 1D layout design style and the increase in both cell pitches to accommodate the lithography constraints. Observe that the area is almost doubled (100% area penalty) when boosting line-pattern resolution for the ALARC MAX LITHO.

The area analysis of a circuit level implementation gives a more realistic area estimation. Figure 3.10 shows an area comparison of adders and multipliers with different number of bits for various layout design styles. Note that the area results for both circuits are normalized using the Nangate NM2D 2 bits adder and the Nangate NM2D 2 bits multiplier respectively. The ALARC designs present an area overhead compared to the Commercial HD of 135% for the ALARC MAX LITHO and a 100% area penalty for the ALARC MIN AREA. Observe that slight area penalty is suffered by Nangate N1D compared to the Commercial HS, approximately 4%, although it increases up to 52% when considering the Commercial HD.

A significant difference compared to the cell area study lies between the Nangate NM2D and the Commercial HD. The area increases about 20% in the circuit implementation, whereas the area overhead was almost negligible in the cell analysis. The area penalty discrepancies with respect to the cell analysis might be caused by different intra-cell routing, i.e., the Commercial HD might use less metal resources or better input allocation that favours place and route of the complete circuit. Moreover, note that the Commercial designs use a different technology compared to the other fabrics that utilize the FreePDK45 design kit and thus part of the area discrepancy might be caused by differences in the design rules.

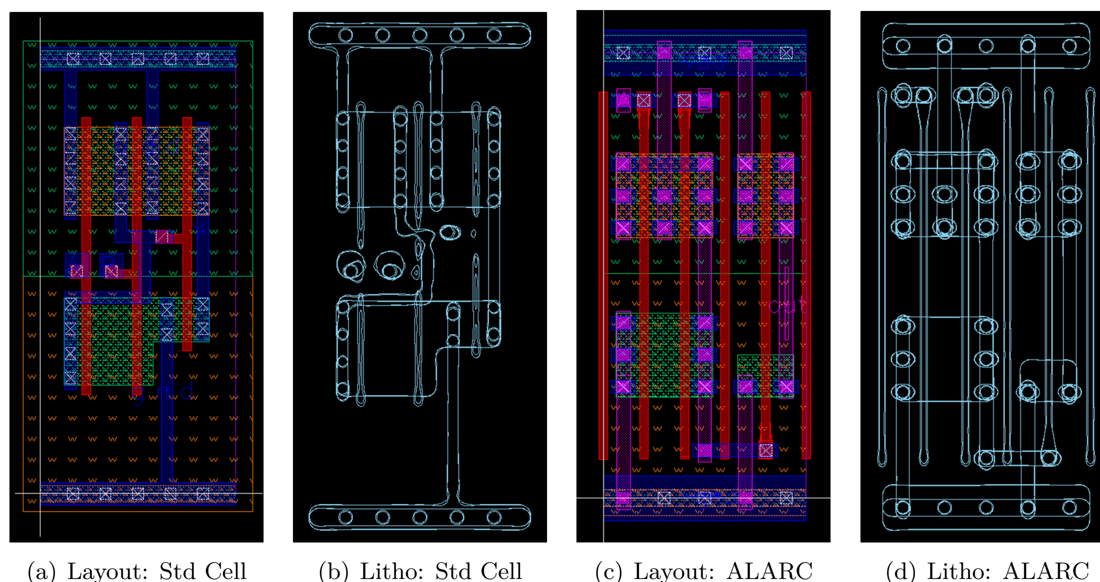


(a) Adder (b) Multiplier

Figure 3.10: Circuits implemented using various layout design styles and technologies.

3.2.3 Lithography comparison with a non-regular cell

In this section, the impact of mapping a typical logic function (AND2) following the ALARC MAX LITHO structure is compared with respect to an AND2 standard cell provided in the FreePDK45 technology kit [2]. The considerable improvement in terms of printability and better variability control between ALARC and 2D standard cells is shown in Figure 3.11.



(a) Layout: Std Cell (b) Litho: Std Cell (c) Layout: ALARC (d) Litho: ALARC

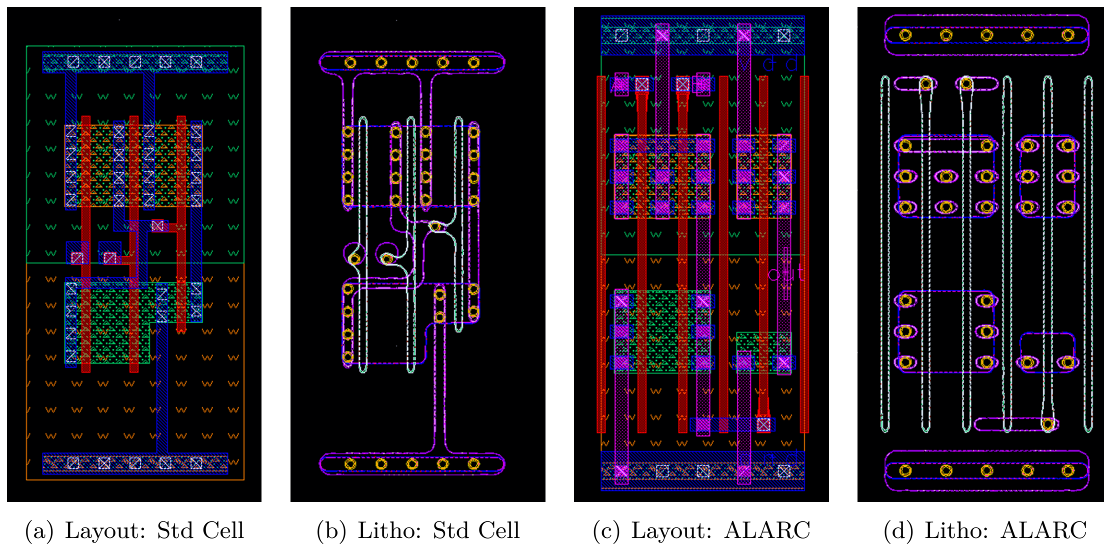
Figure 3.11: AND2 logic gate implemented using a 2D standard cell design and the ALARC MAX LITHO structure using the FreePDK45. The layer map is as follows: (red): poly; (green) active; (white) contact; (blue) metal1; (filled pink) via1; (pink) metal2.

Lithography simulations clearly reveal that the AND2 standard cell is unfeasible in terms of lithography; besides the undulating-line effect suffered by metal1 connections, the poly gate lines are not only narrowed, but they are split. Gates are dramatically hampered mainly

because the spacing between poly lines is not properly adjusted and the input poly enclosure is not enhanced to reduce the abrupt change between the channel and the poly enclosure.

A drawback of the ALARC AND2 cell is the area penalty suffered to keep the same transistor sizes used in the 2D standard cell design, as shown in Figure 3.11. Diffusion breaks are introduced to implement different transistor sizes with its consequent area overhead in order to avoid the diffusion rounding problem, specially for narrow transistors where this effect is more significant. An alternative design solution for regular designs to save area and enhance lithography printability is to apply a transistor equalization at the cost of different power and performance characterization with respect to the original 2D standard cell.

Note that the version of the lithography simulation kit and the optical models used for the lithography simulations throughout this chapter was proposed in 2009 (FreePDK45) [2]. An enhanced version of the lithography kit with significant updates to the optical models improving layout printability was created in 2011 (FreePDK45v2) [3]. Figure 3.12(d) illustrates the lithography simulations of this new kit with alleviated lithography distortions. Note that, in this case, metal2 and via1 simulations are not shown, although the lithography patterns are equivalent to the metal1 and contact shapes respectively.



(a) Layout: Std Cell (b) Litho: Std Cell (c) Layout: ALARC (d) Litho: ALARC

Figure 3.12: AND2 logic gate implemented using a 2D standard cell design and the ALARC MAX LITHO structure using the enhanced FreePDK45v2. The layer map is as follows: (red): poly; (green) active; (white) contact; (blue) metal1; (filled pink) via1; (pink) metal2.

In this lithography kit, poly gate lines are not broken, but the poly corner rounding still causes channel length variations. On the other hand, the layout patterns of the regular layout have been also improved, but the difference, in this case, is not that significant compared to the standard cell case. There lies one of the main advantages of the ALARC designs and also of regular designs in general; simpler layout patterns require less lithographic effort and less complex models compared to 2D standard cell designs in order to obtain a feasible line-pattern resolution. In that sense, regular design is the best layout option for new technology nodes where the lithography process is not mature enough causing a large amount of lithography perturbations.

3.2.4 Effect on leakage and delay of lithography effects

The characterization of an AND2 logic gate implemented following the ALARC MAX LITHO template (depicted in Figure 3.11(c)) based on the drawn shapes and based on the predicted printed patterns is provided next. The channel length of the ALARC template is the key parameter that must be properly configured in order to optimize the cell characterization. Analyzing the channel length using only the layout shapes leads to bad layout configurations due to the amount of channel length variations, therefore lithography predictions are necessary to properly configure the ALARC structure. A comparative analysis between an AND2 cell using the minimum transistor channel length specified by the design rules in this technology (50nm, which is supposed to print a 45nm channel) and a bigger channel length of (60nm) is discussed hereafter. Note that no comparison with the AND2 standard cell is possible with this lithography kit (FreePDK45) because the gates are broken when lithography simulation is applied, as shown in the previous section.

Feeding LFD contour data (lithography predictions) forward into timing and power analysis is made possible by the LFD commands CSG (Contour Simplification for Gates) and CSI (Contour Simplification for Interconnect) which translate lithography simulations data into data that can be directly fed into the RC extraction tools [1]. Table 3.3 shows a comparison between the AND2 ALARC cell simulating the drawn and lithography predictions with parasitic extraction for two different channel length configurations. Values for worst case leakage, worst case delay and worst case energy are presented. The energy is computed considering a continuous toggling output with 2ns period during a 20ns integration time.

Table 3.3: Comparative analysis of the AND2 ALARC MAX LITHO regular cell considering the drawn shapes (layout) and the predicted printed shapes (litho) for two different channel length configurations.

Design metric	Layout	Litho	Layout	Litho
Channel Length [nm]	50	40.65 (-18.7%)	60 (+20%)	55.46 (+10.9%)
Leakage [nA]	4.54	259.01 (+57x)	1.99 (-56%)	3.32 (-27%)
Rise time [ps]	34.5	19.82 (-43%)	45.09 (+31%)	42.52 (+23%)
Fall time [ps]	37.13	21.82 (-41%)	52.65 (+42%)	53.61 (+44%)
Low to High delay [ps]	56.07	28.69 (-49%)	80.81 (+44%)	74.48 (+33%)
High to Low delay [ps]	89.32	32.19 (-64%)	147.28 (+65%)	129.86 (+45%)
Energy consumption [fJ] (T = 20 ns)	54.53	66.8 (+23%)	49.81 (-8,7%)	50.37 (-7,6%)

Lithography simulations reveal that considering only lithography variations in the interconnection layers (metal1 and metal2) do not produce variations in terms of leakage, delay and energy, due to the proper placement and sizing of metal wires in the ALARC structure. Results are not provided since all parameters are deviated less than 1% with respect to the characterization obtained with the AND2 drawn shapes detailed in Table 3.3. Therefore, gate length variation dominates, leakage power, delay and energy variations. In consequence, only poly-silicon and diffusion variations are necessary in the ALARC templates to properly characterize a cell design, reducing the simulation time to perform the lithography analysis.

Table 3.3 shows that leakage dramatically increases considering lithography pattern prediction, because gates are significantly hampered (-18.7% gate length reduction). The excessive poly pitch necessary to accomplish all lithography constraints produces an important increase of the leakage power consumption (57x), although the smaller gate length also provides a considerable reduction of the cell delay (-64%). Energy consumption is higher (+23%) due to the increase in the static power consumption. Hence, proposing a method to compensate delay variations to meet timing constraints and at the same time reduce leakage consumption due to shortened transistor gate lengths, specially for low power purposes, is necessary.

Gates are also drawn at 60nm in order to properly configure the ALARC template to be immune to both lithography distortions and leakage variations. The only difference lies on the 20% increase on the drawn transistor gate (the resulting printed gate length is only 10.9% larger) and the consequent increase in the horizontal cell pitch (4.17% area penalty) to accomplish the design rules. The horizontal cell pitch is increased from 240nm to 250nm to satisfy the manufacturing grid (established as 5 nm) and at the same time maintain the symmetry of the design (metal2 connections equally spaced in between poly-silicon gates). Despite the area overhead introduced by using this larger pitch, the poly contact irregularity is alleviated and consequently the *bottlenecking* effect is reduced. Lastly, none of the two channel length configurations achieves a printed channel of 45nm, which is the target for this technology, and thus a more precise channel length adjustment is required.

Table 3.3 shows a significant leakage reduction (-27%) and energy reduction (-7.6%) when using this new configuration compared to the ALARC cell with minimum transistor size at the cost of extra delay (worst case, 45%). Consequently, a precise adjustment of the transistor channel length is mandatory to sustain the expected cell characterization without excessively degrading either power or performance. In the next section, a comprehensive methodology to properly configure the drawn channel length to combat line pattern resolution and thus optimize the characteristics of regular layout designs is widely described.

3.3 Gate biasing technique to combat channel length variations

Gate length biasing provides an alternative to achieve leakage power savings while also addressing all design robustness constraints detailed in this chapter. In [10], the authors proposed to apply small biases to the transistor gate length in order to further diminish the leakage power consumption. In this section, this technique is introduced as a method to combat leakage variability due to lithography imperfections in the channel length. For instance, an increase on the poly gate spacing was required in order to properly fit the regularity constraints and the ALARC lithography corrections. This increase is directly translated into significant degradation on the expected transistor channel length, as depicted in Figure 3.13. Thereby, increasing the drawn gate length, improves the gate length printability while at the same time provides substantial leakage power savings with the cost of some extra delay and dynamic power penalties.

The aim of the gate biasing technique is to present a design methodology to properly estimate a single-value gate length for all transistors in a regular fabric which compensates

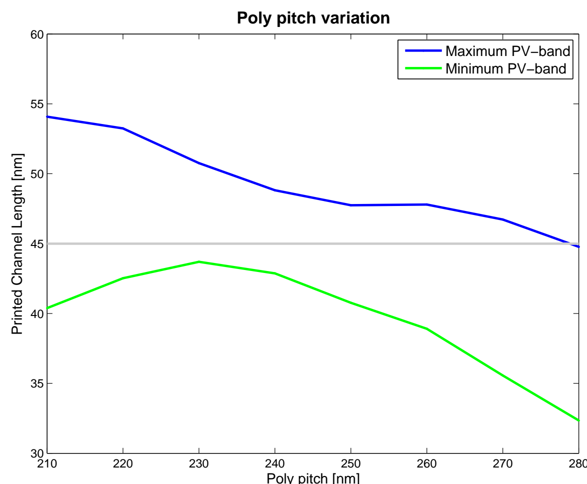


Figure 3.13: Printed gate length variation due to different poly spacing obtained from lithography simulation. In this example, the drawn gate length is set to 55nm.

the non-rectilinear gate effect (NRG) and both systematic layout dependent and across-field variations. The transistor gate length will vary whether leakage, delay or a trade-off between delay and leakage is intended to be compensated given a specific cell purpose. Note that this transistor channel length correction is usually performed during the OPC RET-design stage. However, when using regular equally spaced poly gates, this correction can be directly applied during the layout design stage and thus the OPC effort can be significantly simplified.

3.3.1 Design methodology flow

The gate biasing technique can be easily incorporated in an automatic layout creation procedure without requiring any time consumption, with the exception of a preliminary configuration. The design flow is divided in two main stages. First, the *set up* stage which is only executed at the beginning of the flow and its main objective is the creation of the gate length look-up-table (LUT) considering the regularity constraints of the templates described in this chapter. The LUT is created using lithography simulations in a layout test structure (detailed in section 3.3.2). Figure 3.14 illustrates how the gate-length LUT is added into a layout creation flow.

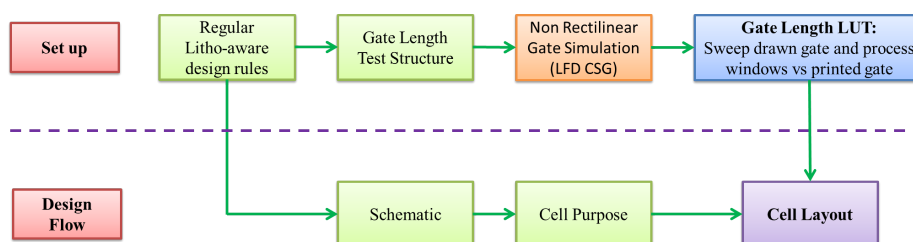


Figure 3.14: Design Methodology Flow

Second, the *design flow* stage where any kind of function can be automatically generated considering the regular litho-friendly rule deck, the cell purpose and the gate-length LUT. Note

that, the cell purpose determines whether a cell design aims to optimize power consumption, performance or a trade-off between power-performance and therefore defines the gate length that must be configured. Lastly, for the 45nm process utilized in this study, channel length is biased from 1nm to 10nm (layout grid is set to 5nm) in steps of 1nm.

3.3.2 Gate length test structure

The employment of equally spaced poly gates, besides reducing gate CD variability, allows the possibility of performing lithography simulations directly in a simple test case structure. This section details how to configure a test case structure to obtain the necessary single-value drawn gate length (L_D) considering the NRG effect, layout dependent and dose/focus variations. Thereby, the single gate-length for the whole layout must consider all these effects in order to better compensate channel length variations.

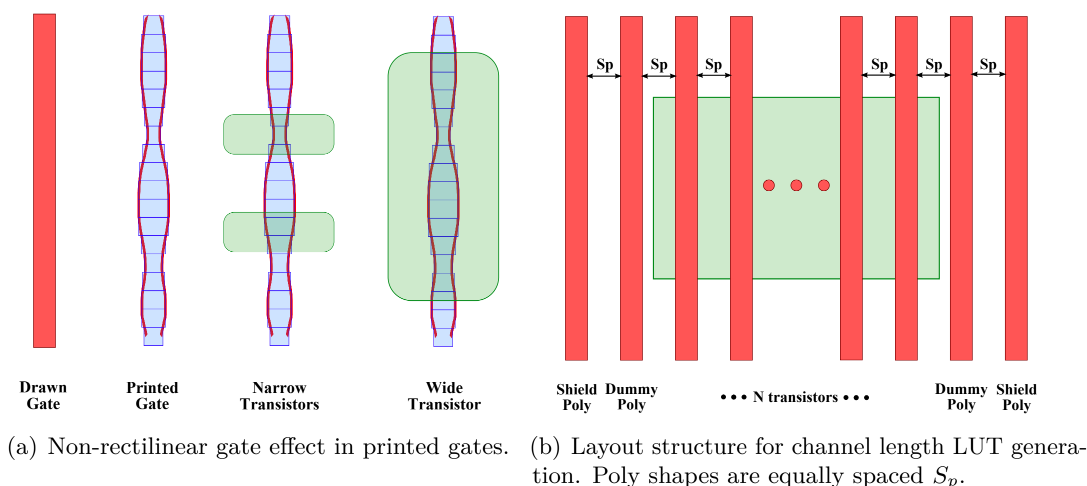
Despite that the exact variation can not be predicted, the amount of variation can be bounded quite accurately and thereby unexpected deviations on circuit performance can be mitigated (delay and leakage power). Systematic layout dependent variations are almost mitigated by using regular layout features with the exception of the poly spacing induced degradation that must be corrected, as shown in Figure 3.13. Moreover, this methodology aims to compensate the inherent variations introduced by the non-rectilinear gate effect (NRG) [11]; due to lithography process, the poly gate shape, which is supposed to be rectangular in a layout device, is severely distorted at the gate edge and the end of the gate. Lastly, across field layout variations, such as variations in dose and focus, must be also captured to properly configure a regular layout. Figure 3.15(a) shows the difference between the drawn gate and the litho-predicted printed gate that would be obtained. The configuration of the test structure is detailed next and the layout implementation is illustrated in Figure 3.15(b).

1. *Regular structure.* Unidimensional equally spaced poly gates and rectangular diffusions are used to configure the cell template and thus the corner rounding effect on both layers is eliminated. This is an inherent advantage of using regular layouts: the gate length obtained in the test structure is valid for any transistor in the layout. In a non-regular design, the corner rounding effect should be considered when computing the L_D. Moreover, the L_D computation directly depends on the poly spacing (Sp), as shown in Figure 3.13, and thus results are particular to the spacing selected.

2. *Number of shield transistors.* Any cell is surrounded side by side by a dummy poly line. However, in order to simulate a more realistic environment (either cells or filler cells are placed at both sides of a cell), extra dummy poly lines (referred as shield transistors) must be added at both sides of the test structure. For this technology, only 1 shield transistor is needed.

3. *Number of transistors.* A sufficiently large number of identical transistors must be simulated in order to predict the effect of the parametric variations in lithography simulations. Thereby, the printed channel-length mean (L_P) and deviation (σ) are more accurately predicted.

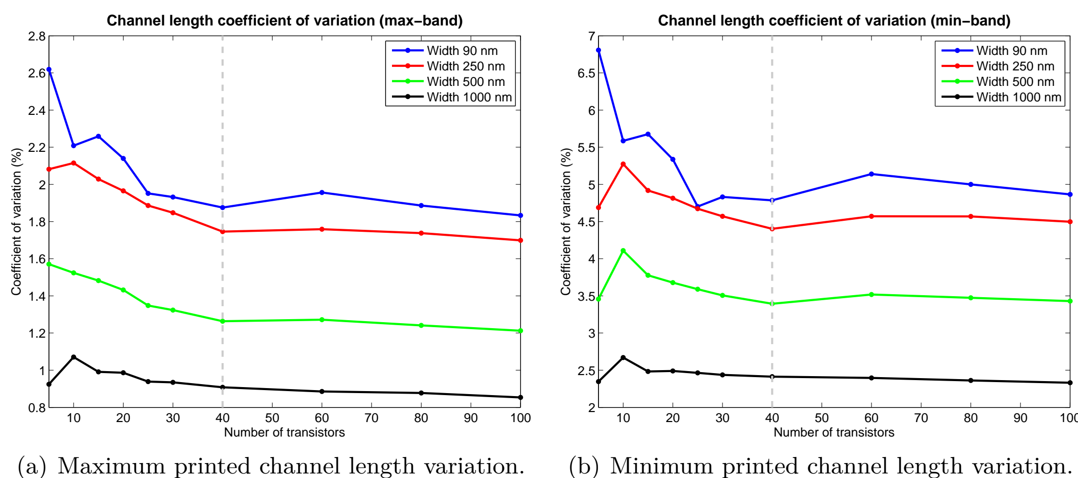
4. *Transistor width.* The roughness (NRG effect) in the printed gates affects more narrow transistors than wide transistors, as depicted in Figure 3.15(a). Therefore, the L_P is obtained using a wide transistor and the σ depends on the transistor width considered.



(a) Non-rectilinear gate effect in printed gates. (b) Layout structure for channel length LUT generation. Poly shapes are equally spaced S_p.

Figure 3.15: Regular layout test structure configuration.

Figure 3.16 shows the coefficient of variation ($\frac{\sigma}{L_P}$) of the test structure for a different number of transistors and different transistor widths. It can be observed that wide transistors ($1\mu m$ width) reduce gate-length variations and thereby the average printed gate length can be more accurately predicted.



(a) Maximum printed channel length variation. (b) Minimum printed channel length variation.

Figure 3.16: Channel length coefficient of variation ($\frac{\sigma}{L_P}$) depending on the transistor width and the number of transistors simulated and considering two different process windows (across-field variation corners).

3.3.3 Gate length discovery methodology

Gate biasing is a technique used for low power purposes that focuses its attention on using the transistor channel length larger than the minimum to compensate leakage consumption.

In this methodology, the drawn transistor channel length is biased in order to obtain the expected printed channel length specified in the technology, in this case 45nm, and also to combat lithography related line-pattern variations.

The printed channel length directly depends on the poly spacing as detailed in Figure 3.13. Note that in this case, poly pitch is established as 250nm so that other lithography perturbations are eliminated, as widely detailed in this chapter. Moreover, 40 equally spaced transistors of $1\mu m$ width are employed in order to more accurately predict the expected average printed gate length (L_P) given a drawn poly gate (L_D). Figure 3.17 illustrates the expected printed channel length depending on the drawn channel length for two different process windows. Observe that the printed channel length increases approximately linearly with respect to the drawn channel length.

The selection of the drawn channel length directly depends on the cell purpose. Moreover, the different process windows must be considered in order to compute the required L_D for a specific cell purpose. Note that, in this case, a minimum and maximum PV-band (Process Variation band) windows are considered. Next, the three types of cells that can be created during the design flow are detailed.

- *Low power (LP)*: In order to ensure that leakage power will not overpass a specific target, the drawn channel length must be adjusted considering the minimum PV-band. In this case, the target is specified so that the printed channel length is 45nm ($L_{P,target}$). Note that the $L_{D-ongrid,LP}$ must be approximated as the smallest integer greater than or equal to $L_{D,LP}$ in order to verify the design rules (denoted as upper square brackets).

$$L_{D,LP} \mid L_{P,min-band} - 3 \cdot \sigma = L_{P,target} \tag{3.4}$$

$$L_{D-ongrid,LP} = \lceil L_{D,LP} \rceil \tag{3.5}$$

- *High Speed (HS)*: In order to ensure that worst-case delay will not overpass a specific target, the drawn channel length must be adjusted considering the maximum PV-band and the $L_{P,target}$. Note that the $L_{D-ongrid,HS}$ must be approximated to the highest integer less than or equal to $L_{D,HS}$ in order to satisfy the design rules (denoted as lower square brackets).

$$L_{D,HS} \mid L_{P,max-band} + 3 \cdot \sigma = L_{P,target} \tag{3.6}$$

$$L_{D-ongrid,HS} = \lfloor L_{D,HS} \rfloor \tag{3.7}$$

- *Typical (TYP)*: Trade-off between leakage power consumption and delay which represents the average channel length considering all corners of variation. The corners of variation are detailed next. (1) Maximum power consumed when ensuring leakage target, v_0 ($L_{D,LP}$); (2) minimum power consumed when ensuring leakage target, v_1 ($L_{D,LP}$); (3) minimum delay when ensuring delay target, v_2 ($L_{D,HS}$); (4) maximum delay when ensuring delay target v_3, ($L_{D,HS}$). Note that, the region of variation can be approximated as a 4-vertices polygon due to the quasi linear behavior of the printed channel length with respect to the drawn channel length (see Figure 3.17). Hence, the centroid of the polygon formed by the four corners of variation gives the transistor

channel length which represents the trade-off between leakage and delay. The centroid is obtained as follows [12].

$$L_{P,LP-best} = L_{P,max-band}(L_{D,LP}) + 3 \cdot \sigma_i$$
$$L_{P,HS-best} = L_{P,min-band}(L_{D,HS}) - 3 \cdot \sigma_i$$

Then, the vertices of the polygon are defined as $v_i(x, y)$ where x represents L_D and y represents L_P.

$$v_0 = (L_{D,LP}, L_{P,target}),\ v_1 = (L_{D,LP}, L_{P,LP-best})$$
$$v_2 = (L_{D,HS}, L_{P,HS-best}),\ v_3 = (L_{D,HS}, L_{P,target})$$
$$A = \frac{1}{2}\sum_{i=0}^{n-1}(x_i, y_{i+1} - x_{i+1}y_i)$$
$$C_x = \frac{1}{6A}\sum_{i=0}^{n-1}(x_i + x_{i+1})(x_i, y_{i+1} - x_{i+1}y_i) \tag{3.8}$$
$$C_y = \frac{1}{6A}\sum_{i=0}^{n-1}(y_i + y_{i+1})(x_i, y_{i+1} - x_{i+1}y_i) \tag{3.9}$$

Lastly, the $L_{D,TYP}$ is obtained by approximating the centroid coordinates to the closest integer value.

$$L_{D-ongrid,TYP} = \lfloor C_x + 0.5 \rfloor \tag{3.10}$$

where σ_i is the deviation introduced by the lithography system. Figure 3.17 depicts how to find the different biased lengths.

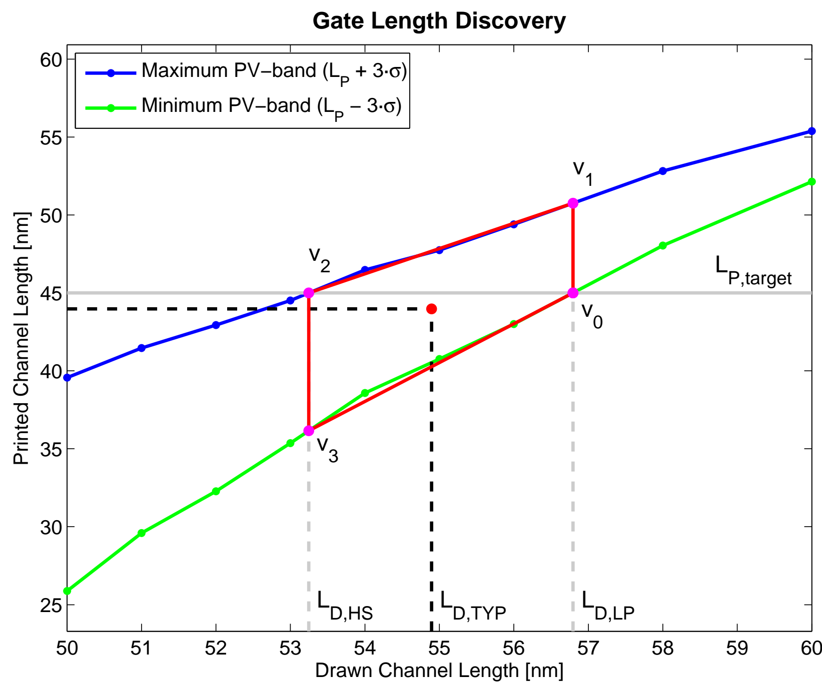


Figure 3.17: Gate length discovery considering the best-case deviation (σ_{bc}).

This σ_i deviation depends on the transistor width used in the cells and the process window. Since cells might have a wide range of transistor width, four strategies can be applied.

- *Simple-case*: Considers that the variation introduced by the lithography system is negligible, thereby the standard deviation is set to 0.

$$\sigma_{sc} = 0 \tag{3.11}$$

- *Worst-case*: Considers that all transistors in a cell are small for the worst process window (minimum PV-band), Figure 3.16(b). This case represents the most pessimistic scenario, where the standard deviation is the maximum expected.

$$\sigma_{wc} = \sigma_{min-band}(W_{min}) \tag{3.12}$$

- *Best-case*: Considers that all transistors in a cell are wide for the best process window (maximum PV-band), Figure 3.16(a). This case represents the most optimistic scenario, where the standard deviation is the minimum expected. Note that the different biased lengths illustrated in Figure 3.17, are computed considering this deviation (σ_{bc}).

$$\sigma_{bc} = \sigma_{max-band}(W_{max}) \tag{3.13}$$

- *Average* (*wc*, *bc* and *typ*): Considers the average channel length standard deviation between all transistors in a cell. Note that the deviation for each transistor depends on its respective width. Moreover, three cases must be considered depending on the process window used: (1) minimum (*wc*); (2) maximum (*bc*); and (3) typical (*typ*), which represents the average between the minimum and maximum.

$$\sigma_{avg\{wc,bc,typ\}} = \frac{1}{N}\sum_{i=1}^{N}\sigma_i(W_i) \tag{3.14}$$

$$\sigma_i(W_i) = \begin{cases} \sigma_{min-band}(W_i) & wc \\ \sigma_{max-band}(W_i) & bc \\ \dfrac{\sigma_{min-band}(W_i) + \sigma_{max-band}(W_i)}{2} & typ \end{cases} \tag{3.15}$$

Figure 3.16 depicts the coefficient of variation of the channel length, i.e., the normalized deviation with respect to the channel length for the worst-case and the best-case (the average case, depends on the logic gate under analysis). Note that, empirically, this deviation is roughly independent with respect to the drawn channel length range used in this study. Thus, an arbitrary channel length (inside the range of simulation) can be employed to compute this deviation. In this study, this deviation is obtained for a 50nm drawn channel length. Lastly, Table 3.4 shows the drawn channel lengths obtained depending on the cell type chosen and their respective printed lengths. In the next section, this gate biasing technique is applied to an AND2 logic gate, showing the electrical characteristics for each gate length configuration.

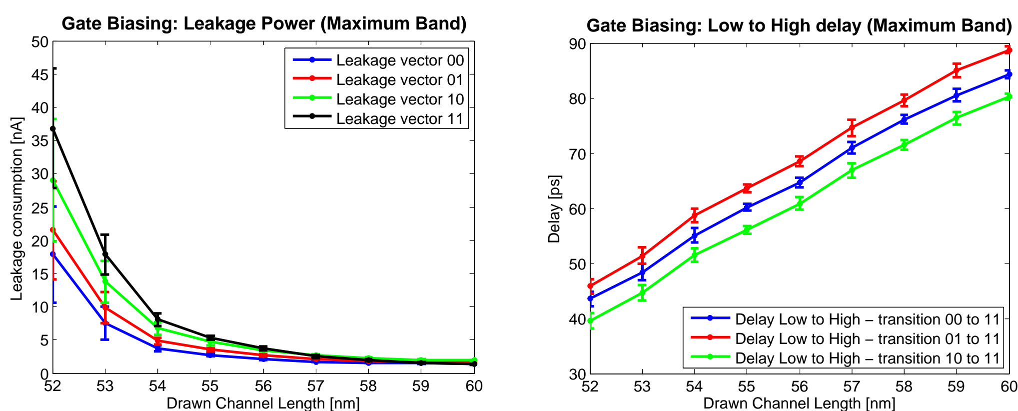
Table 3.4: Transistor channel length drawn and printed obtained using the gate biasing technique.

Purpose	Drawn Length [nm]	Printed Length [nm]
High Speed (HS)	53	35.4-44.5
Typical (TYP)	55	40.8-47.8
Low Power (LP)	57	45.6-51.1

3.3.4 Electrical analysis of the gate biasing technique

The electrical analysis of 20 identical AND2 logic gates implemented following the ALARC MAX LITHO template (depicted in Figure 3.8(a)) are employed to illustrate the gate biasing technique. The characterization is performed using the printed patterns obtained from lithography simulations with parasitic extraction (as described in section 3.2.4) over the 20 replicas of the AND2 logic gates which are randomly distributed in the same layout.

Figure 3.18 shows the average leakage and the average low to high delay for the AND2 logic gates for different channel length configurations considering the maximum process band. As expected, the leakage currents follows an exponential reduction as the channel length increases, whereas the delay augments linearly with the gate length. It is important to highlight that for the leakage case, the worst case leakage changes depending on the channel length configuration. For drawn channel lengths up to 57nm the worst case leakage occurs when the voltage at both inputs is high and for channel lengths from 57nm the worst case happens when the voltage of only one of the inputs is high and the other is low. Moreover, Figure 3.18 shows that the deviation on the average delay is rather similar for all the gate lengths whereas the deviation on the leakage consumption is more significant for smaller gate lengths with higher leakage values.



(a) Leakage power (best process windows). (b) Low to high delay (best process windows).

Figure 3.18: Electrical analysis of an AND2 gate implemented following the ALARC MAX LITHO template for different drawn gate length configurations considering the maximum process window.

A summary of several electrical parameters showing the average values among all the AND2 gates for worst case leakage, worst case delay and worst case energy are detailed in Table 3.5. The energy is computed considering a continuous toggling output with 2ns period

during a 20ns integration time. Moreover, the electrical values are computed for both process windows (minimum band and maximum band) considering that the deviation introduced by the system for the $L_{D-ongrid,type}$ is computed for the best-case (σ_{bc}). Therefore, the results show the minimum and maximum electrical values expected for the gate length configured.

Table 3.5: AND2 ALARC MAX LITHO using the different gate length configurations obtained with the gate biasing technique. The target design is computed for a 45nm drawn gate length without applying lithography simulations. The 'X' value denotes an unreasonable upper or lower bound.

Design metric	Target	High Speed	Typical	Low Power
Drawn Length [nm]	45	53	55	57
Printed Length [nm]	-	35.3-44.5	40.7-47.8	45.6-51.2
Leakage [nA]	16.42	17.8-X	5.4-184.9	2.7-9.2
Rise time [ps]	31.8	X-31.5	25.5-35.9	32.9-43
Fall time [ps]	26.7	X-26.5	21.5-31.9	30.3-35.4
Low to High delay [ps]	51.7	X-53.4	38.7-63.6	57-74.6
High to Low delay [ps]	51.3	X-50.9	34.3-70.3	59.6-87.4
Energy consumption [fJ] (T = 20 ns)	47.1	X-45.8-X	44.6-44.8	44.5-46.13

Table 3.5 shows that the High Speed configuration presents an excessively smaller printed gate length which leads to unreasonable electrical values (denoted as 'X' in the results). For the Typical configuration, delay results are perfectly bounded between the specific target results, however the upper bound leakage is excessively large. Lastly, the Low Power configuration, despite obtaining performance results larger than the objective delays, leakage power consumption is even reduced compared to the target design. In terms of energy consumption, results are rather independent of the gate length configuration. Consequently, for the 45nm target, the best configuration is the Low Power, the Typical can still be employed if power consumption is not a concern, but the High Speed is not a good option due to the excessive shrinkage of the channel length for the minimum process window. Hence, configurations that lead to excessively smaller gate lengths must be discarded during the gate length biasing discovery.

As explained at the beginning of this chapter, the printed gate length used is not accurate for leakage computation and excessive variations (due to the exponential behavior of the leakage current) are obtained. Note that the difference in leakage consumption between the distinct gate length configurations should be more similar to the delay differences. Therefore, the printed channel length appropriate for both delay and leakage calculations should take higher values in order to obtain more realistic measurements, even though the results here presented are sufficient to illustrate the gate biasing technique.

3.4 Conclusions

A regular litho-friendly design presents an undoubted advantage compared to bidirectional designs; all lithography imperfections can be fast identified and corrected during the creation

of the cell design template using lithography simulations and thus the OPC effort is simplified. For instance, channel length variations must be overcome in order to avoid excessive leakage power and delay variations. In this chapter, the layout design guidelines that must be jointly considered to minimize lithography perturbations even for regular litho-friendly design styles were mapped into different layout design templates. Hence, Adaptive Lithography Aware Regular Cell (ALARC) structures that tackles lithography difficulties were presented. The ALARC templates were analyzed in terms of area, lithography printability, delay and power to evaluate the potential benefits and weaknesses of regular layouts. More specifically, a common AND2 logic gate was implemented to show how the ALARC structures can be used to map logic functions and it was proved that the ALARC designs outperform line-pattern resolution compared to a 2D standard cell.

Observe that a regular design does not directly imply an excessive area penalty compared to a standard cell design, as described in Chapter 2. However, restricting the layout design with all lithography constraints can lead to an unfeasible signal routing given a fixed area or to a prohibitive cell area. The regular lithography-aware AND2 designs proposed in this chapter, presented an area overhead of 135% when considering all the lithography constraints (ALARC MAX LITHO) and an area penalty of 100% for the regular design that alleviates these printablity guidelines (ALARC MIN AREA) compared in both cases to the Commercial HD standard cell implementation. The excessive area penalty found in the ALARC MAX LITHO suggests that considering all the lithography constraints is not the best method to obtain a cost-efficient layout design. Therefore, the designer must decide which lithography constraints can be omitted to obtain more competitive area results.

The electrical analysis of the AND2 logic gates implemented following the ALARC MAX LITHO template based on the predicted shapes demonstrated that drawn gate length must be properly specified to avoid unexpected deviations on power and performance. A design level methodology to compensate this channel length variations in regular designs that considers the non-rectilinear gate effect (NRG) and both layout dependent and across field variations was proposed. This gate biasing method is a fast and simple layout technique to estimate the best single-gate length configuration that compensates channel length variations. Results over AND2 logic gates showed that the gate biasing technique provides gate lengths that are robust to process variations with good trade-offs between leakage and performance. However, configurations that lead to excessively shorter channel lengths must be discarded to not jeopardize the electrical characteristics of a circuit.

The lithography benefits of regular layouts were illustrated through precise and costly lithography simulations. Lithography simulations clearly reveal that functions implemented following the ALARC structures, present a regular channel length and thus a reduced channel length variability between transistors. However, performing lithography simulations for a full chip is too expensive in time and therefore a complete characterization using the printed shapes for all the patterns in a layout is not practical. Additionally, the relation between layout printability variations and lithography yield degradation was not addressed in this chapter. Therefore, a new yield estimation method to ease the characterization of layout designs with a reduced set of lithography information is necessary to evaluate the yield improvements of regular layouts. Chapter 4 widely analyzes the proposal of a new yield model to evaluate the lithography distortions on layout designs.

Concluding, the regular layouts detailed throughout this chapter and their evaluation are particular to the technology employed and thus the regular layout implementations must be re-evaluated for each new technology node. The numerical values for the ALARC designs are based on the FreePDK45 technology kit [2] and they may differ from a real technology. For other technologies, lithography simulations should be run to determine appropriate parameters for the ALARC structures. Moreover, this technology includes a rather simple set of design rules which leads to an easier intra-cell routing compared to a real technology. A more comprehensive evaluation of the implications of using regular patterns on layout design must be performed using a real technology. Chapter 6 details litho-friendly regular designs for a 40nm real technology that combine the potential benefits of the regular implementations here presented. Lastly, for smaller technology nodes, more lithography printability variations are expected and thus the benefits of layout regularity will be more significant.

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4

Parametric Yield Estimation model for lithography hotspot distortions

The most significant drawback of regular layouts is that they might introduce area overhead in order to outperform line pattern resolution. Hence, it is necessary a methodology to properly evaluate different layout design styles to find a trade-off between the manufacturability benefits and the area penalty of regular layouts that outperforms traditional 2D IC designs. In this chapter, a lithography evaluation framework is provided to better assess the benefits of the regular layouts proposed in this dissertation.

The main objective of this chapter is to present a lithography parametric yield estimation model to assess the lithography distortion in a printed layout. This chapter proposes an efficient lithography hotspot framework to identify the different layout pattern configurations, simplify them to ease the pattern analysis and classify them according to the lithography degradation predicted using lithography simulations. The lithography hotspot classification and the pattern simplification are key aspects of the framework so the lithography distortion can be captured with a reduced set of lithography simulations. The yield model is calibrated with delay measurements of a reduced set of identical test circuits implemented in a CMOS 40nm technology and thus actual silicon data is utilized to obtain a more realistic yield estimation.

In this chapter, the lithography estimation values are obtained using a 45nm open-source design kit (FreePDK45v2) [1] provided by North Carolina State University (NCSU) which includes a lithography design kit to perform lithography simulations with the Calibre Litho-Friendly Design (LFD) tool [2]. Note that the version of the base-kit employed in this chapter is the 1.4 and the version of the lithography simulation kit and the optical models used for the lithography simulations (LithoSim kit) is the 1.2, both from 2011. This version of the lithography kit includes significant updates to the optical models improving line-pattern resolution and thereby it presents less variations compared to the 2009 version employed in the previous chapter.

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4.1 Parametric yield formulation model

A parametric yield estimation model to assess the lithography distortion in a printed layout is a useful and objective way to compare different layout implementations using physical effects as a basis for evaluation. The goal of this work is to provide an objective way of evaluating the lithography distortion and its impact on yield. In this section, the proposed yield formulation model and how to capture the lithography distortion into the yield model are described.

4.1.1 Yield definition

Yield is defined as the ratio of the number of circuits that are functionally correct and meet the target specifications to the number of manufactured circuits [3]. Yield can be classified in two different types. *Catastrophic yield loss* refers to circuits that suffer from functional failures, such as opens or shorts that cause part of the circuit to not work properly. This kind of failures are traditionally caused by particle defects that falls down into the circuit, as depicted in Figure 4.1. Critical area analysis is used to predict this kind of yield loss [4]. The other type of yield is referred as *parametric yield loss*. In this case, the circuit is functionally correct but it fails to satisfy either performance or power specifications due to deviations in the circuit parameters. Parametric failures may be caused by process variations, including printed pattern variations.

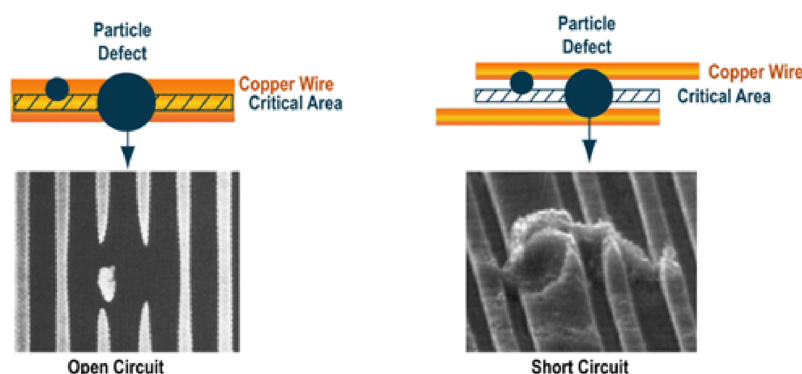


Figure 4.1: Example of particle defects causing catastrophic yield failures [5].

The effect of the lithography gap in current and future technologies is to cause a distortion of the shapes actually printed on silicon. For instance, instead of the designed rectangular shapes, rounded shapes are actually printed. This distortion causes a change in the expected parameters of the circuit: transistor dimensions, wire resistance and capacitance, contact resistances, etc. Finally, the change in parameters modifies the overall circuit specifications of performance and power.

Excessive lithography variations in a poorly controlled process might also cause a wire to break (causing an open circuit) or to merge with a neighboring wire (a short circuit) and

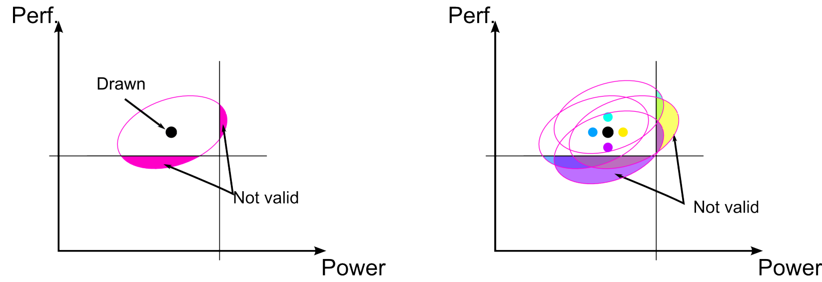


Figure 4.2: Region of invalid circuits for drawn circuit (left) and distorted versions of circuit (right) considering power and performance.

thus cause catastrophic yield losses. However, the lithography simulations performed on the 45nm technology node considered in this work produces layout with no catastrophic failures. Therefore, while certainly lithography hotspots may also induce catastrophic failures, especially in smaller technology nodes, only yield losses associated to parametric failures are considered in this work.

In an ideal process without printed shape distortion there would still be several other sources of variability (for instance, random dopant fluctuations, environmental conditions, and so on) which equally apply to real processes that present some degree of lithography distortion. In the case of an ideal design with no distortion, the parametric yield depends on the proximity of the design at nominal conditions (no variations) to the specification limits. In general, lithography process variations will create a multiplicity of nominal conditions, one for each lithography process condition (see Figure 4.2). Therefore, parametric yield will be affected. It is generally assumed that distortion is larger for non-regular, 2D layouts [6, 7] and this is the ultimate basis for the efforts in the literature in designing cells with more regular (equidistant, 1D) layout features.

In summary, the idea behind the yield model here presented is to capture the systematic lithography variability that will produce losses on the parametric yield of a circuit. Note that, hereafter, all the yield references correspond to parametric yield.

4.1.2 Parametric yield model

The reasoning behind the yield model here proposed is based on the fact that each individual shape in the layout contributes in some way to the overall circuit specification. The problem is that it is difficult to say how the distortion of each individual shape will influence the overall specification. In fact, the same amount of distortion in a given pattern construct can be bad in one node and good in another, or have no effect at all. For this reason, the effect of each lithography hotspots on the overall specification is considered in the model here presented as a random process with a probability of non-failure, i.e. that the circuit is still valid. Therefore, the overall effect is understood as an accumulative probability that depends on the identification of those distortions that produce a significant impact on circuit characteristics (for example, increasing RC constant of wires, or decreasing channel length).

In this proposal, layout quality is then evaluated by counting the number of such cases and rating them to obtain a quantification metric.

Total yield can be expressed as a combination of yield due to catastrophic and parametric faults. The first component is the conventional way of estimating yield and it can be represented with the Poisson model as a function of the critical area [4].

$$Y_{A_{cr}} = e^{-A_{cr} \cdot D_d} \tag{4.1}$$

where $Y_{A_{cr}}$ denotes the critical area yield, A_{cr} is the critical area and D_d is the density of defects.

Equation 4.1 does not capture the dependency on lithography and printability variations that also affect both catastrophic and parametric yield. In order to take into account the effect of lithography distortion on yield, the impact of lithography hotspots (lh) needs to be analyzed. A lithography hotspot is defined as a pattern construct in a layout susceptible to suffer excessive variation under lithography printing [8]. As already explained, even though lithography hotspots may contribute to catastrophic yield loss, this work only considers the parametric yield loss component.

The parametric yield formulation here presented is based on the probability p that a particular lithography hotspot in the layout and its associated distortion still makes the circuit valid, i.e., it still complies with the specification. This mathematical model is based on the assumption that the effect of each hotspot on the overall performance is a random process statistically independent of the effect of the other hotspots. While this may be considered as a controversial assumption, it merely reflects the impossibility to accurately model the effect on performance of each individual hotspot. Note that even though the hotspots themselves are physically correlated (for example, in a given process corner all rectangles may become wider), in some nodes this variation may be detrimental reducing the performance margin while in other nodes it may increase the margin. The correlation is on the distortion, but its effect on performance is assumed to be uncorrelated.

With this assumption the yield due to a number of hotspots can be calculated as the product of the probability p_i of each hotspot. The expression of yield for a layout with N_h number of hotspots is:

$$Y_{lh} = p_1 \cdot p_2 \cdots p_{N_h} = \prod_{i}^{N_h} p_i \tag{4.2}$$

Thus, $p_i = 1$ means that hotspot i has so small distortion that with all certainty it causes the circuit to be inside specifications. Therefore, if all the hotspots had this value, it would mean that there is no (parametric) yield loss due to lithography. Putting Equation 4.2 in exponential form:

$$Y_{lh} = e^{-\sum_{i=1}^{N_h} \lambda_i} \tag{4.3}$$

where the parameter λ_i (lambda) represents the difficulty to print the hotspot (distortion).

Lambda is related to the probability of non-failure as:

$$\lambda_i = -ln(p_i) \tag{4.4}$$

Lambda is a real positive number, with 0 meaning that the hotspot distortion does not affect yield at all and large values meaning a large impact on yield. Note that the lambda parameter must capture two important aspects. The first aspect is the distortion and variability introduced by lithography and the second aspect is the tolerance of the specifications, i.e., the design margin. The lambda parameter will be the basis of the proposed yield estimation metric, to which it is necessary to relate an objective measurement of lithography distortion.

4.1.3 Lambda model

The lambda parameter is associated to the probability of non-failure of a lithography hotspot. However, it is not possible to have a true analytical expression for yield loss and associated probability. In the proposed model, the lambda parameter is related to a measurement of the amount of distortion of a lithography hotspot.

The lambda parameter is obtained following several steps. The first step is to have an evaluation of the distortion based on lithography simulations. For this purpose, the LFD tool from Mentor Graphics [2] is used. This tool calculates the printed contours of a layout for different process conditions, known as a process window. From this process window a maximum and minimum printed edge placement are calculated. From these, maximum variation between printed and drawn layout is obtained, which is called Absolute PV-bands. The LFD tool can then calculate the area of the absolute PV-bands (degraded area, $Area_{deg}$) in a defined region of interest (*analysis window*) and compare it to the area of the original layout ($Area_{drawn}$) in the same analysis window in order to obtain a measure of the amount of distortion and variation expected in the printed layout. Figure 4.3 depicts how the distorted area is obtained in the analysis window. With the obtained data, the LFD tool defines a distortion index (Process Variation Index^{TM}, PVI) as follows:

$$PVI = \frac{Area_{Abs_PVband}}{Area_{layout}} = \frac{|Area_{drawn} - Area_{printed}|}{Area_{drawn}} = \frac{Area_{deg}}{Area_{drawn}} \tag{4.5}$$

This index is a real positive value. Value 0 means a perfect printing and no distortion. In the case of printed contours inside the drawn layout, value 1 is an extreme case that implies that an inner printed shape is not printed and results in null area. For printed contours outside the drawn shapes, the PVI could be even larger than 1 for excessively uncontrolled processes. Nevertheless, 1 is considered as the practical limit of PVI that can be achieved in reasonably controlled processes.

The proposed yield model uses the PVI score as an objective measure of the severity of each hotspot and the lambda parameter is calculated from this index. The relation between both magnitudes is based on the observation that lambda, defined by Equation 4.4, is a number between 0 (for 'perfect' hotspots, not giving any yield loss due to distortion) and, in

principle, infinity. On the other hand, the PVI score is bounded between 0 (no distortion) and 1 (maximum distortion in a controlled process).

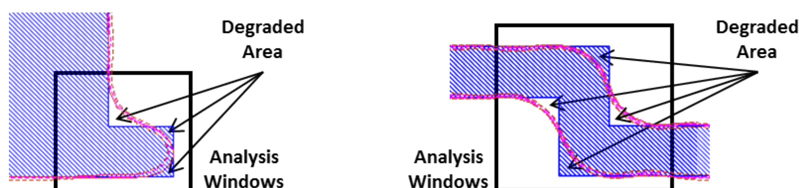


Figure 4.3: Lithography distortion of different hotspots and their respective areas of printed (simulated) and drawn layout.

Considering that a certain level of distortion is unavoidable, but does not produce any yield loss, a simple function that relates the lambda index of hotspot i (and ultimately, the yield estimation) with the PVI score obtained from the LFD is defined as follows.

$$\lambda_i = \begin{cases} 0 & PVI_i \leq PVI_{min} \\ S \cdot \frac{PVI_i - PVI_{min}}{1 - PVI_i} & PVI_{min} < PVI_i < 1 \end{cases} \tag{4.6}$$

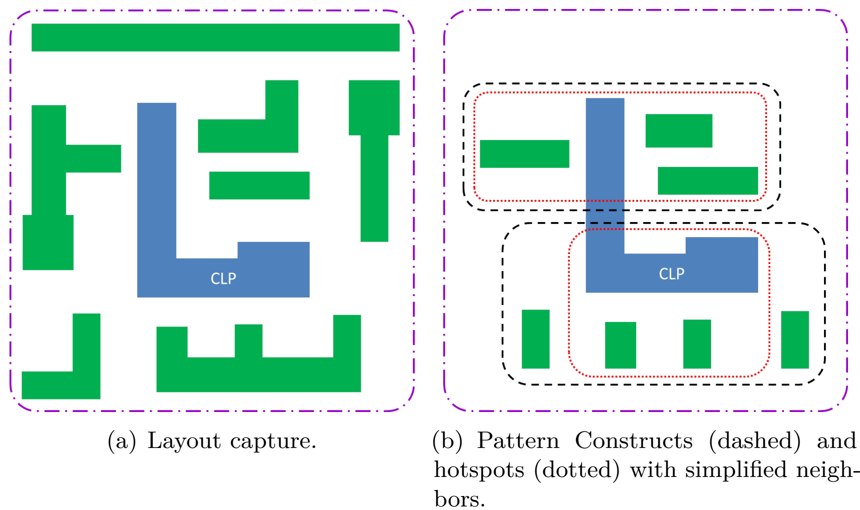
This generic function maps the PVI_i number between 0 and 1 to a new number between 0 and infinity. The PVI_{min} parameter refers to the minimum tolerable lithography distortion of the printed layout patterns that does not degrade the lithography yield. The parameter S is a scaling factor that must be adjusted to give reasonable estimates of yield loss according to the technology employed, the design margin and the layout design style. The calibration of the yield model using silicon data is illustrated with an example in Section 4.3.

4.2 Pattern construct - hotspot identification

The concept of a lithography hotspot is related to the concept of Pattern Construct (PC): a PC contains a central layout polygon (CLP) or part of it and all the neighboring edges within a specific distance of interaction. The concept of a hotspot and a pattern construct with simplified neighbors are depicted in Figure 4.4.

Pattern construct identification is required in order to analyze the different layout shapes employed in a design and calculate their PVI and lambda indexes. This work presents a methodology based on an exhaustive search of all pattern constructs. Computing the PVI score for each pattern construct is impractical due to the huge number of different patterns in a typical layout. Hence, a pattern simplification is applied in this paper to decrease the amount of lithography simulations, as will be explained in Section 4.2.3. Moreover, the PVI score of *compound* pattern constructs can be approximated by combining the lithography information of previously known *basic* pattern constructs and thereby the amount of lithography simulations can be further decreased, as detailed in Section 4.2.5.

With this methodology a cell library composed of a few hundred cells can be analyzed in some minutes, and a complete circuit with many thousands of gates require a few hours.



(a) Layout capture.

(b) Pattern Constructs (dashed) and hotspots (dotted) with simplified neighbors.

Figure 4.4: Examples of pattern constructs and hotspots. The Central Layout Polygon (CLP) is depicted in blue and neighbors in green. The simulated contours of these examples are illustrated later in Figure 4.8.

Several other more efficient and sophisticated approaches for pattern discovery than this proposal are also possible, such as those based on machine learning and/or pattern matching techniques [8, 9]. Note that the proposed methodology is aimed at the 45/40nm node where the main interaction occurs between nearest neighbors. For future technologies with more complex interactions, the presented methodology might be updated to incorporate new lithography distortion effects at the cost of increased complexity.

4.2.1 Pattern construct discovery flow

The evaluation framework for hotspot identification and assignment of a severity index is divided in two parts. Firstly, a preliminary *technology characterization* based on accurate lithography simulations where a pattern construct class library is generated, containing the PVI score of the most significant identified pattern construct classes for each layer. Once this library is obtained, the *evaluation flow* applies this information to the layout under analysis without the need to undertake lithography simulations for their evaluation. The different steps needed to obtain the evaluation of a layout are explained in Figure 4.5.

The first part of the design flow is referred to as the technology characterization stage. The aim of this stage is to obtain a library containing the most significant pattern construct classes with its respective lithography evaluation score obtained using lithography simulations. The pattern construct class library can be obtained using as input a small set of training cells with different representative layout configurations. The procedure to find all pattern constructs and classify them into groups is the same as in the evaluation flow and it will be described in the next two sections. Once the pattern constructs are identified and classified, lithography simulations are performed to calculate the PVI score for each of them. Using this PVI score, only those pattern constructs that suffer excessive variation are considered as hotspots, i.e., those with a PVI score larger than a minimum degradation threshold

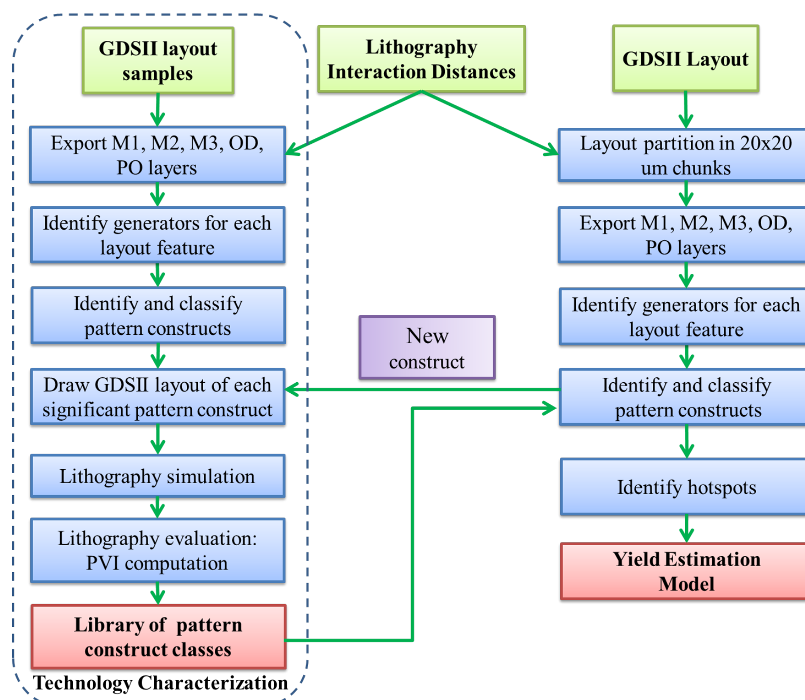


Figure 4.5: Steps needed to obtain the evaluation of a layout.

(PVI_{min}). After the technology characterization phase, the pattern construct class library that will be used during the evaluation flow is created. Note that the class library is updated in case that a new significant pattern construct is identified in a new layout.

The evaluation flow extracts all the pattern constructs of the GDSII layout under analysis and then, using the library of pattern construct classes, all hotspots are identified and assigned the previously obtained PVI score. The advantage of the previous technology characterization stage is that costly lithography simulations are only performed at that stage and thus the lithography evaluation is highly simplified. Note that if multiple patterning techniques are applied in the manufacturing processing, each GDSII layout will only contain the patterns belonging to the same printing mask. As a final step, the yield estimation model takes the number and type of hotspots as the basis to estimate the impact of lithography printability on layout design.

4.2.2 Pattern construct identification

The analysis of the layout implies the identification of geometric pattern constructs that will be later classified as hotspots, or not, depending on their severity. This analysis requires two inputs: a GDSII file of the layout and a set of lithography interaction distances (LID) as detailed in Figure 4.6. The LID must be pre-characterized for each layer using lithography simulations for the technology of interest.

The pattern construct search starts finding all the *generators* of a GDSII layout for each layer. A generator is a rectangular area of a layout which contains all the layout polygons

within a specific distance of interaction (d_{int}) from each edge around a central layout polygon (CLP), as depicted in Figure 4.4(a). The d_{int} is obtained using the equation detailed next:

$$d_{int} = max\,\{d_4 + d_{11}, d_4 + d_{12}\} \tag{4.7}$$

where the d_i are the lithography interaction distances to properly capture the pattern neighborhood detailed in Figure 4.6. This distance d_{int} is configured based on the lithography interactions observed between the different layout patterns in the 45nm technology employed. For smaller nodes like 32nm, 22nm or 14nm, this distance might be enlarged, thus increasing the size of the layout generators.

The pattern construct recognition takes vertexes (V) and edges (E) as the primitive geometries within which the pattern constructs are analyzed. In each generator, one or more pattern constructs may be identified according to the following attributes:

- Type of layout pattern construct.
- Vertexes and angles of the layout patterns in the pattern construct.
- The lithography interaction distances of the layout patterns in the pattern construct.
- Relation of the central pattern with closest neighbors: whether they are placed contiguously or oppositely with respect to it and other neighbors.

d_i	Description
1	Max interaction between consecutive V.
2	Max interaction between non consecutive V.
3	Min edge length to suffer degradation.
4	Max external distance of interaction.
5	Max degradation that extends from a V.
6	Max extension of degradation caused by a N.
7	Max distance to consider contiguous neighbors (d_7 = 2d_6)
8	Max distance to consider opposite N (side direction) (d_7=d_8).
9	Max distance to consider opposite N (front direction) (d_9=2d_4 + W_{max}).
10	Max distance that a N affecting an E can affect a V (d_{10} = d_5 + d_6).
11	Min edge extension of a N to cause distortion.
12	Maximum width to consider a N harmful.
13	Line-End layout extension for contacts.
W_{max}	Max width of any E affected by a N.

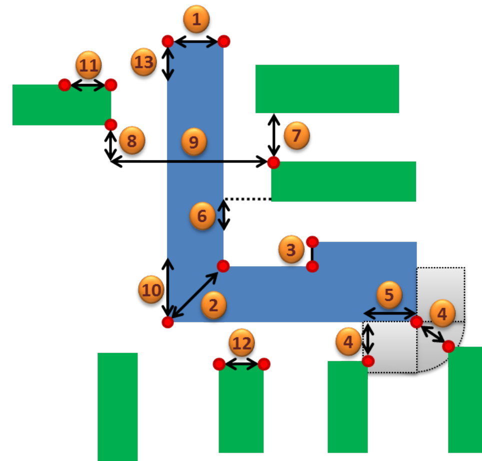


Figure 4.6: Lithography Interaction Distances (LID). (V) Vertexes; (E) Edges; (N) Neighbors.

Once a pattern construct is identified, it is classified in terms of its difficulty to be printed with the PVI score. The value of the obtained PVI score depends on the number of shapes and vertexes involved as well as their angles and relative distance. Hotspots are then detected as those pattern constructs with a PVI score above a given threshold. The steps of the pattern construct discovery and the hotspot detection are described in Figure 4.7. The different types of pattern constructs identified are described in the following sections.

This pattern construct discovery algorithm was built using a custom software implemented in Matlab and C.

```
1:  D = Lithography Interaction Distances;
2:  C = GDSII layout Circuit;
3:  L = Pattern construct class Library;
4:  for all layers ∈ C do
5:    for all fragments ∈ C do
6:      G = Identify Generators(fragments);          ▷ Each G can have several PCs;
7:      for all Generators ∈ G do
8:        V(D, CLP) = Identify group of vertexes affecting each other in CLP;
9:        NV(D, V) = Identify group of neighbors that affects V;
10:       NE(D, E) = Identify group of neighbors that affects E;
11:       Analyze relation between N;   ▷ Opposite N, contiguous N, N affecting EaV;
12:       pcV2V(NV) = Identify Vertex Layout Patterns;
13:       pcV2E(NE) = Identify Edge Layout Patterns;
14:       pcEaV(pcV2V, pcV2E) = Identify combined pcV2V and pcV2E;
15:       PC_basic = Identify basic PC classes;
16:       PC_compound = Identify compound PC classes;
17:       PC_new(PC_basic, PC_compound) = Identify new high occurrence PC classes;
18:       Update_PClib(L,PC_new);
19:       lh(PC_basic, PC_compound) = Identify hotspots(L);
20:       Yield(lh) = Compute yield estimation;
```

Figure 4.7: Steps of the hotspot detection.

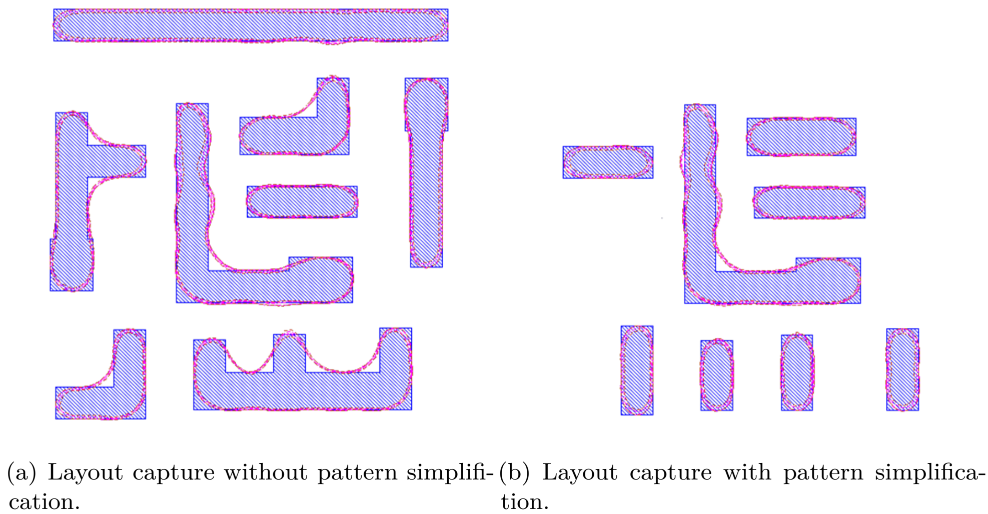
4.2.3 Lithography pattern construct classification

In a typical layout there are millions of different pattern constructs and thus hotspot configurations. This is especially true for traditional standard cell designs with non-regular patterns and in this sense the use of regular design styles greatly facilitates the lithographic analysis needed for layout characterization.

Some simplifications are considered in the pattern construct classification algorithm that are aimed at reducing the number of different pattern constructs. First, the neighboring layout polygons are simplified by only considering the edges affecting the central layout polygon instead of the complete neighboring layout polygons. This simplificaton, as shown in Figure 4.8, shows that very similar lithography results on the central pattern are obtained, compared to the results of the original layout. Second, two pattern constructs are considered equal if they have the same geometric configuration (*class*), independently of the exact distances and dimensions of each element. For instance, a line-end with two different edge lengths are considered to belong to the same class.

These simplifications might be inaccurate for smaller technology nodes. The aim of this proposal was to minimize as much as possible the lithography effort considering the technology node available (45/40nm).

The different pattern constructs are distributed into classes according to the PC attributes described in Section 4.2.2 considering the following criteria. Firstly, patterns constructs are



(a) Layout capture without pattern simplification.

(b) Layout capture with pattern simplification.

Figure 4.8: Layout capture with lithography simulations to illustrate the pattern neighborhood simplification.

classified considering the number of consecutive vertexes of the central layout pattern and their respective angles. However, consecutive vertexes with a small distance between them are discarded in the classification since they obey to special design rules (typically, contact and via enclosures) that improve the printed shape. Secondly, non-consecutive vertexes close to each other (typically, an L shape as depicted in Figure 4.9) are grouped together as part of a pattern construct. Thirdly, neighboring pattern edges within the range of interaction to one of the vertexes or to one of the edges are also included in a pattern construct.

The enumeration of the basic pattern construct classes is graphically depicted in Figure 4.9 and their explanation is detailed in Table 4.1. The lithography evaluation of the pattern constructs is described in Section 4.2.4.

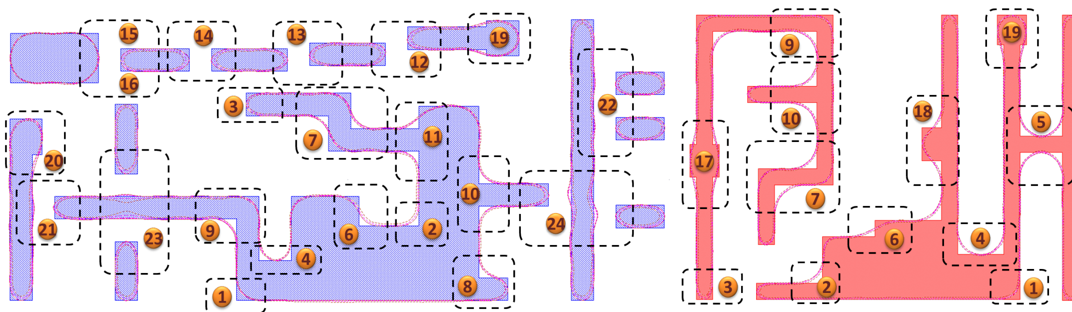


Figure 4.9: Lithography Classes. (Left) Diffussion and Metal classes; (right) PO classes.

The classification shown in Table 4.1 has been obtained analyzing the layout of 24 basic cells designed in different layout styles and it has been tested for 9 benchmark circuits implemented also with different layout configurations. New classes appearing frequently in the layout are characterized and added to the library of simulated classes. The most significant cases depend first on the technology, and second, on the layer analyzed. For example, the poly layer, in general, has more simple constructs than the metal1 layer. Again, it should be noted that for future technology nodes with more complex interactions the

Table 4.1: Pattern construct classes description.

Class	Name	Description
1	In-vertex	Single 90° corner.
2	Out-vertex	Single 270° corner.
3	Line-end (LE)	Two consecutive 90° vertexes.
4	Out-U	Two consecutive 270° vertexes.
5	H	Two consecutive 270° vertexes placed closed by another two consecutive 270° vertexes.
6	Snake	A 90° vertex followed by a 270° vertex.
7	Double Snake	A 90° vertex followed by a 270° vertex placed closed by another 90° vertex followed by a 270° vertex.
8	Toe	90°, 90°, 270° vertexes placed closed by a 90° vertex.
9	L	90° vertex placed closed by a 270° vertex.
10	T	270° vertex placed closed by a 270° vertex.
11	T-Hammer	A 90° vertex followed by a 270° vertex placed closed by a 270° vertex.
12	LE Pull-back Short	Two LE placed in front of each other when less than half of the opposite edges interact between each other.
13	LE Pull-back Long	Two LE placed in front of each other when more than half but less than all of the opposite edges interact between each other.
14	LE Pull-back All	Two LE placed in front of each other when both edges with equal length interact between each other with all its length.
15	LE Pull-back Big Neighbor	Two LE placed in front of each other with the neighboring edge bigger interact between each other with all its length.
16	LE Pull-back Small Neighbor	Two LE placed in front of each other with the neighboring edge smaller interact between each other with all its length.
17	Edge Center Enclosure	270°, 90°, 90°, 270° vertexes placed closed by another 270°, 90°, 90°, 270° vertexes, forming an enclosure
18	Edge Displaced Enclosure	270°, 90°, 90°, 270° vertexes placed consecutively. Enclosure displaced to one side of the edge.
19	LE Center Enclosure	270°, 90°, 90°, 90°, 90°, 270° vertexes. An enclosure placed at the end of an edge, i.e, in a LE.
20	LE Displaced Enclosure	270°, 90°, 90°, 90°, 90°, 270° vertexes. An enclosure displaced to one side of the LE.
21	Sharp Neigh	Neighboring sharp edge placed towards a layout edge.
22	Sharp CONT Neighs	Two neighboring sharp edges placed consecutively towards a layout edge.
23	Sharp Opposite (OP) Neighs	Two neighboring sharp edges placed in front of each other with a layout edge in between.
24	Sharp DIAG OP Neighs	Two neighboring sharp edges placed each other in one side of a layout edge, but not in front of each other.

proposed classification should be increased in order to more accurately estimate the yield losses.

4.2.4 PVI computation of basic classes

In addition to the basic pattern constructs shown in Figure 4.9, some shapes in the layout can be considered as combinations of simpler pattern constructs. These complex shapes are called *compound* pattern constructs (see Figure 4.12 for an example). Basic pattern constructs are simulated to calculate their PVI score. In the case of compound pattern

constructs, their PVI score is calculated from a combination of the PVI of the basic pattern constructs that they are composed of. This is explained in Section 4.2.5.

For each identified basic pattern construct class, a representative layout is created to apply a lithography simulation and obtain its PVI score. The representative layout takes into account the minimum distances and dimensions allowed by the technology. In this way, slightly different pattern constructs that belong to the same class differing only in dimensions (within the lithography interaction distance of the technology) are assigned the same value of the PVI and thereby the number of required lithography simulations to characterize the library is greatly reduced. It has to be noted that this simplification will produce more precise results for regular designs with a small set of possible geometric configurations of pattern constructs.

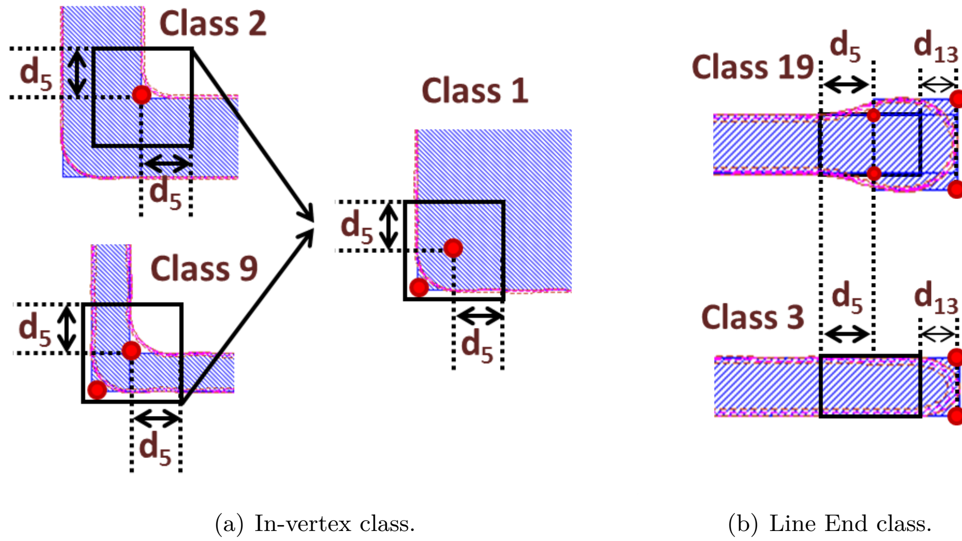
In order to compute the PVI it is necessary to define a geometric region called *analysis window*. This region is initially defined by a rectangular region defined by the outermost vertexes in the pattern construct, and then enlarged by displacing each edge of the region up to a distance where the lithography degradation is negligible. Two examples of common analysis windows are depicted in Figure 4.10(a) for classes 2 and 9. Once the appropriate analysis window is defined for each class, a lithography simulation is performed and the PVI is calculated.

There are two special cases, classes In-vertex (1) and Line-end (3), where the conventional way of defining the analysis window produces unreasonable PVI values compared to other classes. These two cases must be analyzed separately studying the utilization of each pattern construct and the geometries of similar patterns. On the one hand, class 1 has a similar class, class Out-vertex (2), and another class, class L (9), can be thought of as a combination of classes 1 and 2. Therefore, the analysis window for class 1 is defined with the same region used for class 2 and class 9. On the other hand, Class 3 (Line End) is similar to Class 19 corresponding to a contact enclosure and therefore, in order to have a fair comparison between these two classes, their analysis window should be the same. Figure 4.10 illustrates these two special classes comparing them to the related classes.

4.2.5 PVI computation of compound classes

Additional pattern constructs can be considered as a combination of basic classes, giving rise to compound classes. In order to avoid the lithography simulation of compound classes, their PVI can be estimated using the degraded area of the basic classes. In a pattern construct, the following types are identified depending on the different interactions between the central layout polygon and the neighbors:

- **Vertex to Vertex pattern constructs ($pcV2V$)**: Pattern constructs composed by a set of vertexes that affect each other. For instance, a line-end or a line-end Pull Back Long are two examples detailed in Table 4.1.



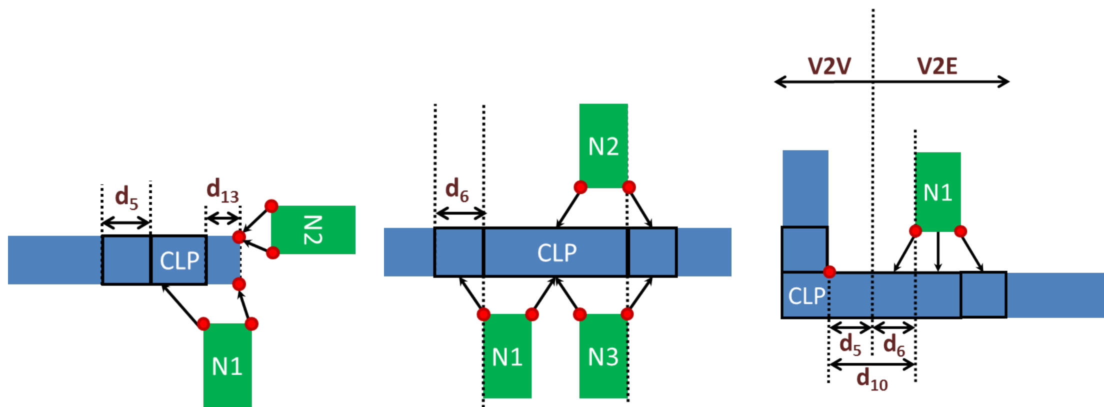
(a) In-vertex class. (b) Line End class.

Figure 4.10: Special pattern construct classes with specific analysis windows. Drawn layout and lithography contours.

- **Vertex to Edge pattern constructs** ($pcV2E$): Pattern constructs formed by neighbors that affect an edge. Multiple contiguous and/or opposite neighbors are identified in this category, as described in Table 4.1.

- **Edge and Vertex pattern constructs** ($pcEaV$): Pattern constructs composed by a combination of vertex to vertex ($pcV2V$) and vertex to edge ($pcV2E$) pattern constructs. The union is produced when the degradation of a neighbor that affects an edge is merged with the degradation extended from a vertex.

Figure 4.11 depicts an example of these three types of pattern constructs.



(a) Vertex to Vertex PC ($pcV2V$). (b) Vertex to Edge PC ($pcV2E$). (c) Edge and Vertex PC ($pcEaV$).

Figure 4.11: Examples of pattern constructs. Central layout polygon (CLP) is depicted in blue and neighbors in green. The interaction distances d_i are detailed in Figure 4.6.

The compound PVI is computed differently according to these three main categories of pattern constructs. The equations for the estimation of the PVI are detailed next:

- **Vertex to Vertex pattern constructs ($pcV2V$)**: The degraded area is estimated as the sum of the degraded area of the central layout polygon (CLP) without any neighbor ($Area_{deg_{CLP}}$) and NV (number of neighboring vertexes) times the degradation introduced by only one neighbor to a vertex ($Area_{deg_{NV}}$). The PVI score is then estimated as this degraded area over the original drawn area of the CLP:

$$PVI_{pcV2V} = \frac{Area_{deg_{CLP}} + NV \cdot Area_{deg_{NV}}}{Area_{drawn_{CLP}}} \tag{4.8}$$

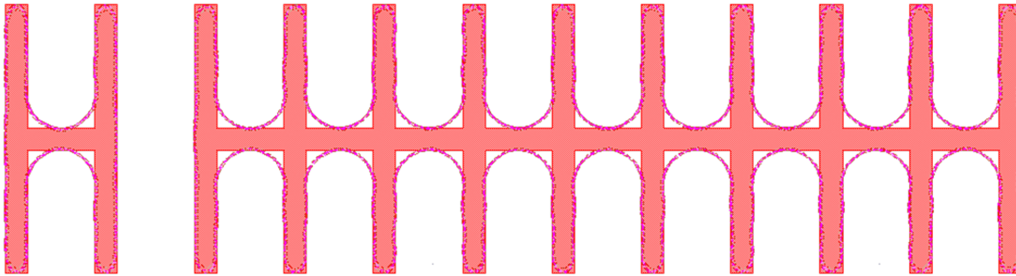
- **Vertex to Edge pattern constructs ($pcV2E$)**: The degraded area is estimated as NE (number of neighboring edges) times the degradation introduced by only one neighbor to an edge ($Area_{degNE}$). The PVI score is then approximated as this degraded area over the original drawn area of the CLP:

$$PVI_{pcV2E} = \frac{NE \cdot Area_{deg_{NE}}}{Area_{drawn_{CLP}}} \tag{4.9}$$

- **Edge and Vertex pattern constructs ($pcEaV$)**: In this case, the degraded area is estimated as the sum of the degraded area of the central layout polygon (CLP) without any neighbor ($Area_{deg_{CLP}}$) and NV and NE times the degradation introduced by only one neighbor to a vertex ($Area_{degNV}$) and to an edge ($Area_{degNE}$) respectively. The PVI score is then estimated as this degraded area over the original drawn area of the CLP:

$$PVI_{pcEaV} = \frac{Area_{deg_{CLP}} + NV \cdot Area_{deg_{NV}} + NE \cdot Area_{deg_{NE}}}{Area_{drawn_{CLP}}} \tag{4.10}$$

An additional correction is needed when dealing with large pattern constructs which are the repetition of smaller ones, as for example the one shown in Figure 4.12. In that example, all close vertexes are within the lithography interaction distance and therefore it has to be considered as a single large pattern construct. Consequently, the analysis window is also very large. The result is that the resulting PVI score is unrealistically small.



(a) Basic PC class. (b) Compound PC class composed by multiple instances of a Basic PC.

Figure 4.12: Layout capture with lithography simulations showing two similar PCs with similar PVI, but totally different area drawn.

In order to counteract this effect, the PVI score of this kind of compound pattern constructs is computed as N_{EPC} (number of equivalent pattern constructs) times the PVI score of

the basic pattern construct it is made of. This parameter must be adjusted depending on the layer under analysis, the pattern construct class library utilized and the PVI results obtained.

4.3 Yield model calibration and test

The aim of the proposed parametric yield estimation model is to provide a new quantification metric that enables the possibility to objectively compare the lithography impact on different layout design implementations. The framework here proposed serves as vehicle to determine the best layout implementation or to quantify the amount of regularity that can be admitted in a design while at the same time maximizing the amount of Good Dies Per Wafer(GDPW).

In this section, the parametric yield model is calibrated against silicon measurements for different design margins. With the obtained parameters, the yield model is applied to evaluate three different layout styles. These layout styles are: (1) all uni-dimensional layout (F1D), a layout configuration using only 1D shapes in all layers; (2) half unidimensional layout (NP1D), a layout style using 1D shapes for poly and metal2 and 2D shapes for the rest of the layers; (3) fully two dimensional layout (NA2D), a layout design using all shapes 2D. The NP1D and the NA2D are two layout design implementations from Nangate that were previously detailed in Chapter 2. On the other hand, the F1D is a regular layout design based on Template A and widely detailed in Section 6.1, but automatically created using Nangate placement and routing algorithms. Three benchmark circuits have been created using these layout styles and routed using either 1D or 2D metal connections as required.

4.3.1 Parametric yield measurements

The parameters of the yield estimation model must be calibrated in order to give reasonable values of yield loss according to the technology employed, the layout design style and the design margin. This calibration ensures that the ultimate goal of comparing different layout styles is based on real measurements and not only on a theoretical model. In this section, it is described how the yield estimation model can be calibrated with silicon data using as reference several test circuits implemented in a CMOS single patterning 40nm technology [11]. In this case, delay measurements are used as vehicle to illustrate the calibration methodology but any other metric can be employed, such as power measurements. This section shows that the yield model can be calibrated according to any yield curve obtained from real chip measurements and then these measurements can be related to an estimation of the lithography degradation of a layout design style.

The measurements were made on a test chip composed of 8 instances of voltage controlled delay line (VCDL). The VCDLs were implemented following two different layout styles: a totally regular 1D layout and a non-regular 2D layout. Transistors were sized sufficiently large to decrease the effect of random variations and therefore, the main source of variability

was the systematic lithography distortion associated to layout dependent variations. The delay of 176 VCDL circuits (8 per chip and 22 chip samples) per layout design style was measured and the distribution of delay was computed as a percentage of the mean (assumed to be nominal) delay. Figure 4.13 depicts the delay histogram of the 176 VCDL instances where lithography variations make this delay different for each instance.

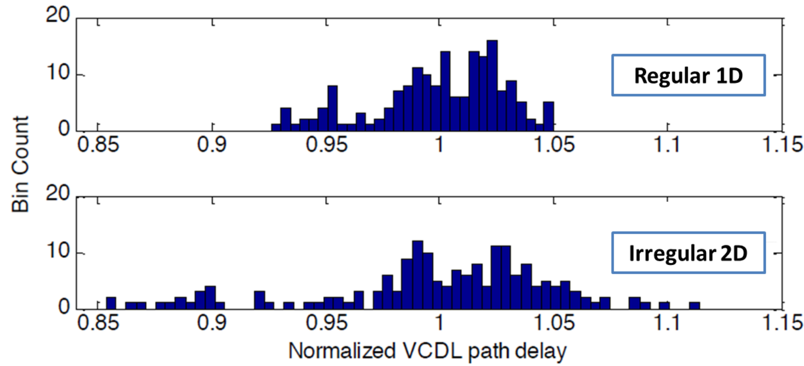


Figure 4.13: Histogram of the normalized VCDL path delay for a regular 1D and a non-regular 2D layout design styles.

From the delay distribution, the *yield curve* is computed as the percentage of VCDL circuits with a delay larger or smaller than the nominal delay considering different delay boundaries. The latter boundaries can be interpreted as the necessary delay margin to ensure specification compliance of the circuit or, in other words, the amount of delay variation such that it still meets the timing constraints. Therefore, the yield is computed as the ratio of valid circuits (inside the delay target boundaries) and the total instances manufactured.

It is important to clarify that the delay-based yield measurements analyze the dispersion of the delay with respect to the nominal delay. In other words, the parametric yield measurements mainly captures the impact of lithography and other sources of variability on the circuit delay. The resulting delay-based yield measurements curves are shown in Figure 4.14. As obtained from measurements, the curve corresponding to a regular layout presents a higher yield for any delay margin (*Design Margin, DM*) as a result of reduced dispersion in the delay among the samples. The measurements for a non-regular layout presents the lowest yield. Additionally, the mean between these two measurements is computed in order to obtain a third yield curve (*Average*).

4.3.2 Yield model calibration

The calibration of the parametric yield model is made by means of finding suitable values of parameters S and PVI_{min} of Equation 4.6, in order to match the theoretical model to the values obtained from measurements. The PVI_{min} is adjusted based on lithography simulations and the S parameter is adjusted using the yield curves corresponding to measured yield from a circuit. The model is employed to compute the yield for three benchmark circuits: a Multiplier (*MUL*), an Image and Video Processor (*IVP*) and a Network-On-Chip Router (*NOCR*).

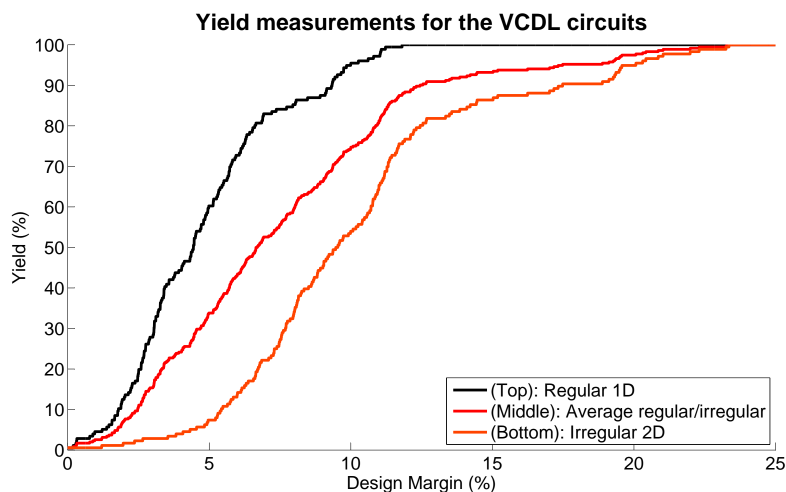


Figure 4.14: Parametric yield measurements for the VCDL circuits implemented in silicon.

Yield measurements for the benchmark circuits under analysis are not available and without loss of generality, it is assumed that the critical delay distribution of one of the benchmark circuits is very similar to the available yield measurements (VCDL circuits). In particular, in order to illustrate the methodology it is assumed that the measured yield curves (Y_m) of the VCDL circuits correspond to the *MUL* benchmark. The measured yield obtained from the regular implementation of the test circuit is used as reference for the implemented Multiplier following the F1D layout design style and the measured yield from the non-regular implementation as reference for the NA2D. Moreover, another layout configuration is implemented, the NP1D, which based on the observations made from the layouts, it should take yield values in between the regular and the non-regular implementations and thus the *Average* yield curve is used as reference. The yield for the other circuits is subsequently computed using the calibrated model derived from this adjustment.

As previously explained, the value of the PVI_{min} parameter captures the minimum tolerable distortion that does not degrade the parametric yield. This parameter is related to the set of minimum patterns necessary to construct a layout design. The minimum set of patterns corresponds to the set of regular pattern constructs which includes edges, line-ends and enclosures (classes 1, 3, 14, 17 and 19 detailed in Table 4.1). These patterns are practically perfectly printed in this technology and it is assumed, without loss of generality, that a small distortion on the printed patterns does not cause parametric yield losses. Based on this consideration, the PVI_{min} is computed as the maximum PVI value of the regular set of patterns. According to the lithography simulations performed to analyze the pattern constructs in this technology, the value of the PVI_{min} parameter for all the layers, that is, the maximum tolerable distortion that gives perfect yield, is 0.02. Note that any other pattern construct has a PVI score that is equal or larger than this PVI_{min}.

The scaling parameter S must be adjusted for each design margin and for each layout design style. To do so, it is considered a scenario where all hotspots (N_h) of the Multiplier have the same reference PVI number (PVI_{ref}), computed as the average PVI for the N_h hotspots in the Multiplier for each design style. Thereby, the scaling parameter S for each layout design

style (DS) and each design margin (DM) using Eq. 4.3 and 4.6 is computed as follows:

$$S(DM, DS) = -\frac{ln(Y_m(DM, DS))}{N_h(DS)} \cdot \frac{1 - PVI_{ref}(DS)}{PVI_{ref}(DS) - PVI_{min}} \quad (4.11)$$

The parameter S serves to model the lambda factor which relates the PVI score into a degradation score (lambda) that will give a reasonable estimation of parametric yield loss. In other words, it adjusts the yield model with respect to real yield measurements. Thus, this adjustment calibrates the lambda equation to give yield values in consonance with other layout designs with similar pattern configurations that have been experimentally tested in silicon.

Figure 4.15 shows the different values of the S parameter for the different design margins and layout design styles. Observe that as the design margin increases, the S factor of the different layout styles presents more similar values reflecting the same trend in the yield curves of Figure 4.14.

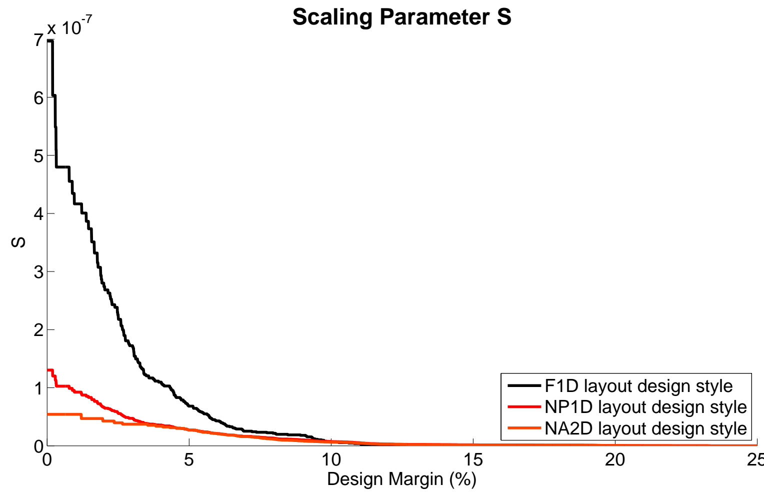
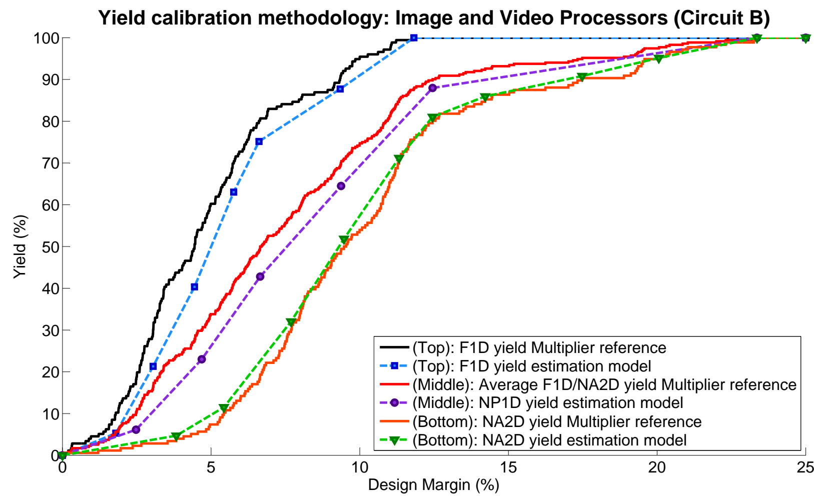


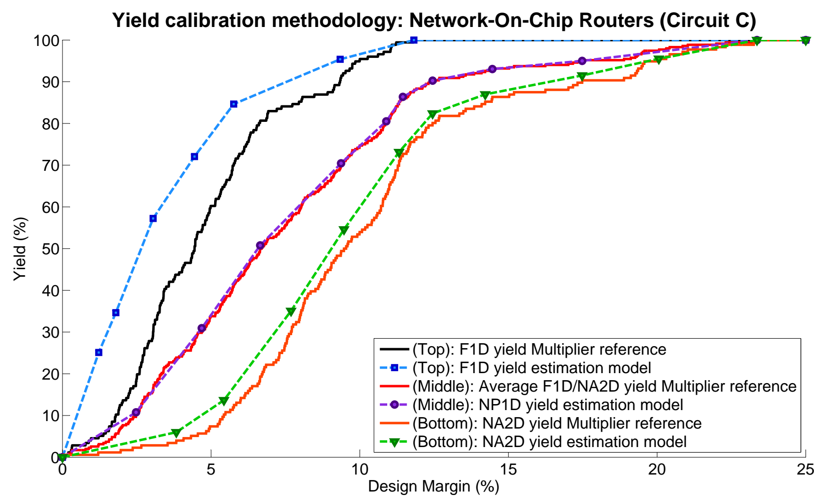
Figure 4.15: Scaling parameter S for the different layout design styles.

The value of S obtained from the calibration process using the MUL circuit is applied to the model in Equation 4.6 for the IVP and $NOCR$ circuits following again the three layout implementations, F1D, NP1D and NA2D. As it can be observed in Figure 4.16, the obtained yield for the IVP benchmark is slightly below that of the MUL benchmark, while the yield of the $NOCR$ is above that of the MUL benchmark. This differences in yield values obtained with these two circuits compared to the MUL reference are mainly caused by the different number of hotspots occurring in each circuit (the number of hotspots in each circuit is shown in Table 4.2). This difference is even larger for the $NOCR$ circuit, specially for the F1D design, since this circuit contains approximately half of the number of hotspots of the reference multiplier.

In order to analyze if these differences are in agreement with the model, a scaled yield curve for these circuits can be computed taking into account the different characteristics of the IVP and $NOCR$ circuits with respect to the MUL circuit. Assuming that for the same layout styles there is the same average PVI (PVI_{ref}) for any circuit and correspondingly an average λ_{ref}, it is easy to scale any yield curve Y_{m_0} by knowing the relation between the



(a) Image and Video Processors (Circuit B)



(b) Network-On-Chip Routers (Circuit C)

Figure 4.16: Yield estimation using the calibration methodology for different design margins and layout design styles.

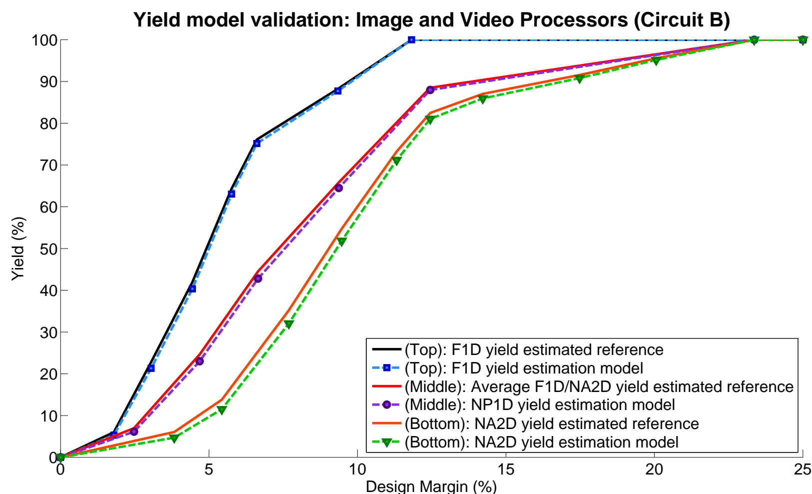
number of hotspots of each circuit, based on Eq. 4.3.

$$Y_{m_i}(DM, DS) \cong e^{-\lambda_{ref} \cdot N_{hi}} = Y_{m_0}(DM, DS)^{\frac{N_{hi}}{N_{h0}}} \tag{4.12}$$

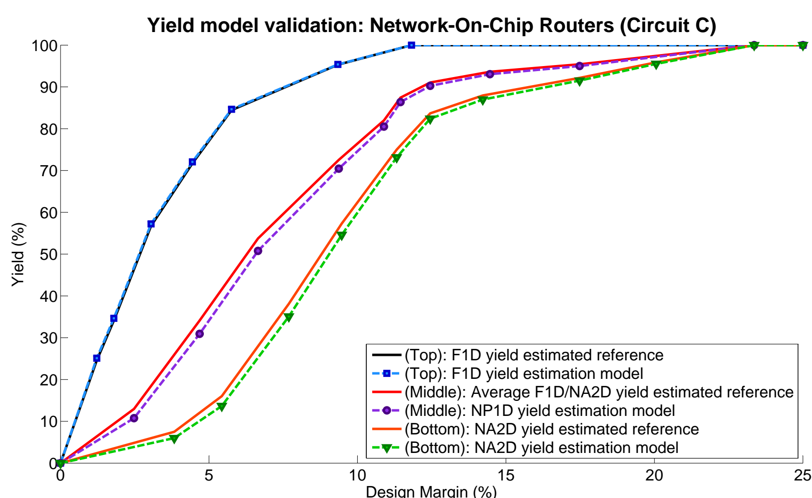
Figure 4.17 shows that the scaled measured curves (*estimated reference* in the legend) are in good agreement with the points calculated using the S parameter and the summation of all hotspots with corresponding PVI.

4.3.3 Layout evaluation using the proposed parametric yield model

In this section, the parametric yield model previously calibrated is applied to the three benchmark circuits under analysis for a specific design margin of 11%. These circuits are



(a) Image and Video Processors (Circuit B)



(b) Network-On-Chip Routers (Circuit C)

Figure 4.17: Yield model validation using the yield estimated reference for different design margins.

composed by thousands of instances of the same circuit so that the NA2D implementation gives an area of 1 cm^2. Note that several instances of the same circuit must be jointly considered since the small area of one single circuit would suffer a parametric yield loss practically negligible. The number of Good Dies Per Wafer ($GPDW$) for a wafer of radius 150 mm is computed in order to better capture the trade-off between area penalty and yield degradation. Also, in order to differentiate the degree of layout regularity employed in each design, a Regularity Metric (RM) is computed as the ratio between the number of simple regular patterns constructs (classes 1, 3, 14, 17 and 19 detailed in Table 4.1) and the number of all the pattern constructs used in the layout. Further details on how to compute the GDPW and the RM metrics can be found in Chapter 5.3.

Observe from Table 4.2 that the results clearly show that the three circuits implementations following the F1D layout design style, in agreement with Figure 4.16, present a better yield than styles with more complex layout patterns (NP1D, NA2D), but at the cost of extra area. Considering the $GDPW$ metric, the NP1D designs give the highest number of $GPDW$ and

thus provide the best area/yield ratio. This advantage in *GDPW* is in turn at the cost of using a larger number of complex pattern constructs compared to the most regular design style, the F1D, as the *RM* index indicates.

Table 4.2: Lithography evaluation metrics. Area, number of pattern constructs (N_{PC}), number of hotspots (N_h), *PVI* mean, regularity index (*RM*), yield estimation and Good Dies Per Wafer (*GDPW*).

Circuit	**Multipliers (A)**			**Image and video processors (B)**			**Network-On-Chip routers (C)**		
Instances	2500			3900			6950		
Layout	F1D	NP1D	NA2D	F1D	NP1D	NA2D	F1D	NP1D	NA2D
Area (cm^2)	1.69	1	1	1.56	1	1	1.36	1	1
N_{PC} x10^6	4127	2577	2363	3954	2764	2427	3085	2313	1974
N_h x10^6	142	759	763	175	886	663	67	680	613
PVI_{mean}	0.069	0.073	0.129	0.069	0.069	0.136	0.065	0.071	0.135
RM (%)	94.41	74.56	69.02	92.83	72.75	73.70	96.33	75.49	70.99
Yield (%)	97.02	78.72	64.74	96.36	77.55	66.80	98.67	81.63	68.97
GDPW	355	504	414	384	496	428	456	522	441

As observed in Table 4.2, the yield of these circuits is rather similar across the benchmarks and mostly dependent on the layout design style. Hence, the yield model presented in this work is mostly a means to take informed decisions on what is the most suitable library to use in order to increase the *GDPW* of the circuits. Also note that the numeric results of yield directly depend on the design margin specified for the design and thus they are particular for that case. However, the qualitative results to decide the best library choice in terms of yield or *GDPW* remain generally valid.

The pattern construct simplification used to decrease the number of lithography simulations make the lithography evaluation for complex 2D designs (NP1D, NA2D) less accurate than the evaluation for regular designs (F1D). Hence, one of the advantages of regular designs is that the yield can be calculated with less effort since most of the pattern constructs are regular and the lithography simulations are done for the specific pattern construct used in these designs.

4.4 Conclusions

This chapter presented a new layout quantification metric based on a parametric yield estimation model that enables the possibility to objectively analyze and compare different layout implementations in terms of lithography degradation. A lithography hotspot discovery algorithm was implemented in order to capture the lithography distortion of a layout with a reduced set of lithography simulations. The goal of this lithography evaluation framework is not to give a perfect prediction of yield impact, but to have an objective way of assessing the layout quality in terms of lithography distortion without an excessive number of lithography simulations and with reduced information from silicon data.

The lithography evaluation framework can be used to compare different layout implementations and also capture those patterns that excessively degrades manufacturing yield. The yield model was demonstrated for three different benchmark circuits and three different layout design styles. Despite the lithography evaluation framework has been only applied to evaluate circuits, it could be also used for cell or library characterization, as shown in Chapter 6.

The yield estimation model is based on the assumption that the effect of each hotspot on performance is statistical in nature. For this reason, the model requires a calibration procedure taking as a reference parametric yield measurements (e.g. delay or power) of different layout styles. The value of parameter S as a function of design margin and layout style is obtained from this calibration procedure and applied to any circuit. Since the model is calibrated using either delay or power yield measurements, it is expected that the model numerical results depend on the magnitude used in the calibration. However, for the purpose of layout printability evaluation this dependence is not important. The use of the model as prediction of the actual parametric yield would need to be validated with an extensive set of measurements and should therefore be the object of future work.

The yield model tested on different benchmark circuits shows that the unidimensional designs evaluated in this chapter potentially present an enhanced parametric yield compared to traditional 2D designs at the cost of an excessive area penalty. Layouts with an intermediate degree of layout regularity can benefit from a certain yield enhancement and similar area compared to fully 2D styles, thus producing designs with a higher number of $GDPW$.

Chapter 6, provides more regular layout design styles with different degrees of layout regularity aiming to produce better GDPW results compared to the designs used in this chapter. Note that, hereafter the NA2D layout design style is discarded for further comparison with respect to regular layouts since the NP1D clearly outperforms the yield and the GDPW results without area penalty.

Using the pattern construct information extracted to estimate the yield, additional metrics to capture the pattern complexity of a layout and to better assess the pattern differences between layout design implementations can be extracted. Chapter 5 details how to compute two additional metrics, the Regularity Metric (RM) which evaluates the usage of litho-friendly regular patterns and the Pattern Construct Complexity metric (PCC) that computes the number of corrections in each different pattern construct.

Lastly, the yield model here proposed serves to assess the lithography impact on layout design, but more metrics should be employed in order to globally evaluate a layout implementation. Other metrics such as via usage, wire-length, pattern complexity and electrical characterization must be jointly considered in order to obtain a more comprehensive evaluation of a layout design style. However, it is difficult to compare distinct layout designs taking into account several aspects, when none of the designs present the best results for all the metrics. Hence, a global layout quality metric that will enable a designer to select the best layout design with a single-score value considering several metrics is provided in the next chapter.

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5

Layout Quality Metric

During this dissertation, several flavors of layout regularity aiming to outperform traditional 2D standard cell designs are proposed. However, optimizing layout printability can produce cells that might be globally less efficient than others. The lack of a layout design metric in the literature to properly compare different layout strategies, makes it difficult to evaluate the benefits and weaknesses of different templates. Hence, a layout quality metric is required to fairly compare cells, libraries or circuits implemented following distinct layout designs.

This chapter presents a versatile Layout Quality Metric (LQM) that will allow designers to easily compare different layout implementations. The LQM serves to globally evaluate a layout design template using several layout aspects, referred as partial metrics. Moreover, the LQM metric can be differently configured with different sets of partial metrics depending on the design requirements or the layout design stage where it is employed.

The LQM is here configured following two different set of partial metrics. On the one hand, a Simple Layout Quality Metric (LQM-S) is presented based on the measurements of simple partial metrics that can be computed by inspection of the layout design and thus it serves to give an initial evaluation of a given template. On the other hand, a more Elaborated Layout Quality Metric (LQM-E) is proposed based on more elaborated measurements to provide a more detailed analysis of the benefits and weaknesses of a design.

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5.1 Layout Quality Metric (LQM)

Layout design can be focus on optimizing different cell aspects, such as power, performance, area or lithography variability among others and thus producing rather distinct cell designs. In practice, it is difficult to say which is the best layout implementation in order to obtain the most efficient design considering several layout characteristics. In that sense, this section proposes a Layout Quality Metric (LQM) that taking into account several layout parameters (referred as partial metrics) provides a single value to compare different layout implementations.

The Layout Quality Metric (LQM) combines the evaluation of individual measurements into a single-score metric to assess a layout design. More specifically, the metric here proposed, analyzes the loss of each specific aspect, but since the parameters under evaluation can take totally different values, they are normalized with respect to a reference. Note that, this overhead is computed differently whether the parameter is better as highest or lowest values takes. Therefore, the loss $Q_j(i)$ for each metric M_j of a library i is calculated as follows.

$$Q_j(i) = \begin{cases} \left(\frac{M_j(i)-M_{best}}{M_{best}}\right) \cdot 100 & M_{best} = min(M_j(i)) \; \forall i \\ \left(\frac{M_{best}-M_j(i)}{M_{best}}\right) \cdot 100 & M_{best} = max(M_j(i)) \; \forall i \end{cases} \tag{5.1}$$

For some evaluation metrics, e.g., the usage of metal3 wires inside a cell, a partial metric can take a value of 0 and therefore the loss Q_j with respect to a non zero value would take an score of infinity. In those cases, instead of computing the overhead with respect to a reference value, the $Q_j(i)$ score penalty is directly obtained as the absolute value as detailed next.

$$Q_j(i) = M_j(i) \;\; if \;\; \forall i \; \exists \; M_j(i) = 0 \tag{5.2}$$

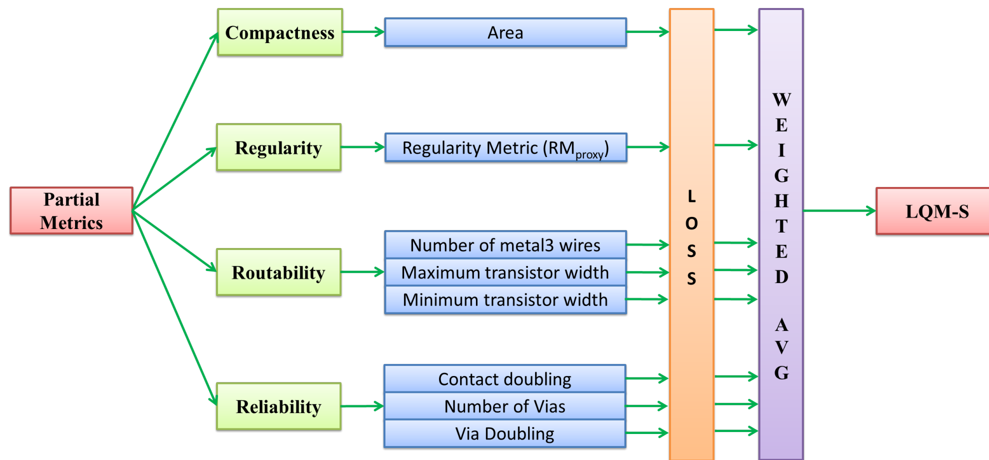
Using the loss computed for each aspect, a global Layout Quality Metric (LQM) which considers several layout parameters can be extracted. However, this score penalty can still take excessively different values and besides the relative importance of each parameter can be different. Thereby, the LQM is computed as the weighted sum of the amount of loss of each parameter under evaluation. The LQM is calculated using the following equation.

$$LQM = \sum_{j=1}^{N_Q} \alpha_j Q_j(i) \tag{5.3}$$

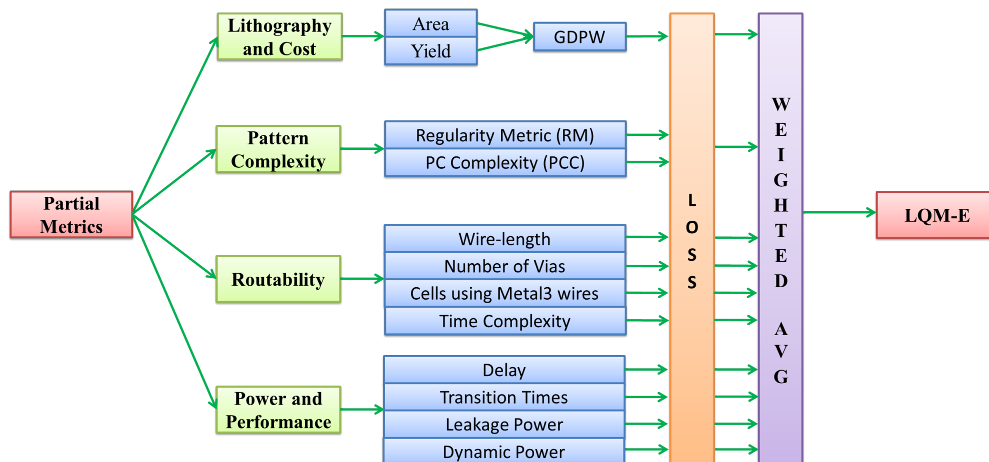
where the N_Q is the number of design metrics and α_i is the associated weight to each different aspect Q_j. Note that the LQM metric is bounded between 0 and infinity, where 0 represents the highest quality. The single-score LQM directly depends on the weighted distribution assigned to the α_i parameter and thus it can be set up differently depending on the relative importance assigned to each of the parameters.

The LQM can be configured using any set of partial metrics in order to evaluate a layout design. In this dissertation, the LQM is used with two different set of measurements. The

$LQM - S$ will refer to the LQM computed using the simple set of aspects detailed in section 5.2. On the other hand, the $LQM - E$ will be obtained using a more elaborated set of measurements described in section 5.3. Figure 5.1 illustrates a summary of the two different set of partial metrics here considered to configure the LQM. Lastly, note that the set of metrics used in each case can be perfectly modified in order to better accommodate the partial measurements to the design requirements.



(a) Layout Quality Metric using Simple measurements (LQM-S).



(b) Layout Quality Metric using Elaborated measurements (LQM-E).

Figure 5.1: Layout Quality Metrics (LQM).

5.2 Layout Quality Metric using simple measurements (LQM-S)

The Layout Quality Metric is based on computing an average weighted sum of different cell parameters. In this section, simple evaluation measurements that can be obtained by inspection of the layout are proposed in order to provide an initial analysis of cell designs. The configuration of the LQM using the simple set of metrics is referred as the $LQM - S$.

The simple set of partial metrics for a template i is divided in four different categories as described next.

1. *Compactness*: This metric evaluates the area of a design obtained directly by inspection of the cell height and cell width. Two aspects determine the compactness of a layout design: (1) *cell pitch* that must be adjusted according to the design rules and the area impact and; (2) *number of tracks* that must be configured according to the size of transistors, metal3 usage and area overhead.

$$Area(i) = cell_{height}(i) \cdot cell_{width}(i) \tag{5.4}$$

2. *Regularity*: A simplified regularity metric (RM_{proxy}) is here proposed to capture the pattern complexity of a layout configuration. The RM_{proxy} is based on the observation on how each layer is defined and thereby it tries to capture how regular is the metal1, metal2, diffusion and poly layers in the design considering different aspects. Note that if a template does not use one of these layers, it is considered that this layer is totally regular.

    a) *Pattern nature*: 1 if the layer shapes are restricted to a few patterns, 0 if arbitrary patterns are used.

    b) *Unidirectional*: 1 if the shapes of a given layer run in only one direction, 0 if they run in both directions.

    c) *One-dimensional* (1D): 1 if the layer shapes are 1D and 0 if any shape is 2D.

    d) *Single Grid or Equal Spacing*: 1 if the shapes of a given layer are placed in a single grid location for each direction, 0 if they are placed in more than one grid location. For instance, poly gates placed vertically from top to bottom of the cell and equally spaced in the horizontal direction will take a score of 1.

    The previous rules can be formally expressed with equation 5.5.

$$rg_j(i) = \begin{cases} 1 & rule\ verified \\ 0 & otherwise \end{cases} \tag{5.5}$$

    Thus, the average regularity metric per layer is computed as follows.

$$RG_{layer}(i) = \frac{1}{rules} \left(\sum_{j=1}^{rules} rg_j(i) \right) \tag{5.6}$$

    Lastly, the regularity metric of the cell is computed as the average regularity metric among all layers being evaluated.

$$RM_{proxy}(i) = \frac{1}{layers} \left(\sum_{j=1}^{layers} RG_{layer}(i) \right) \tag{5.7}$$

3. *Routability*: The routability metric computes the complexity to route a given cell. Firstly, it analyzes the need of using metal3 lines inside the cell. Secondly, it evaluates

the capability of the cell to be routed using wide transistors for high performance purposes or small transistors for low power circuits. This metric is also divided in several parameters.

a) *Number of metal3 wires*: Evaluates the need of using metal3 (M3) connections inside the cell by counting the number of metal3 wires used ($N_{wiresM3}$).

$$M3_{wires}(i) = \#N_{wiresM3}(i) \tag{5.8}$$

b) *Maximum transistor pair width*: Measures the maximum active area width (considering a pair of PMOS and NMOS) that fits inside the cell while at the same time ensuring the routabilty of the cell. It is computed considering the arithmetic mean among all NMOS (Wn_j) and all PMOS (Wp_j) maximum oxide diffusion areas (OD) independently and then adding the average active areas of both PMOS and NMOS.

$$W_{OD,max}(i) = \frac{1}{n}\sum_{j=1}^{n} max(Wn_j) + \frac{1}{p}\sum_{j=1}^{p} max(Wp_j) \tag{5.9}$$

where Wp_j and Wn_j is the active area width of a PMOS and NMOS transistor j and p and n is the number of PMOS and NMOS transistors respectively.

c) *Minimum transistor pair width*: Captures the smallest oxide diffusion area width (considering a pair of PMOS and NMOS) that ensures the routability of the cell. This metric calculates the arithmetic mean among all NMOS (Wn_j) and all PMOS (Wp_j) minimum oxide diffusion areas (OD) independently and then adding the average active areas of both PMOS and NMOS.

$$W_{OD,min}(i) = \frac{1}{n}\sum_{j=1}^{n} min(Wn_j) + \frac{1}{p}\sum_{j=1}^{p} min(Wp_j) \tag{5.10}$$

4. *Reliability*: The reliability metric evaluates the contact and via usage of a given design.

a) *Contact Doubling*: Analyzes the possibility of using two contacts to access to the diffusion region. Note that the N_{CO} computes the number of contacts used in the cell and the N_{SD} counts the number of source and drain connections considering that each access to diffusion should be contacted twice.

$$CO_{double}(i) = \frac{N_{CO}(i)}{N_{SD}(i)} \tag{5.11}$$

b) *Number of Vias*: The risk of via failure augments as the number of vias increases and thus this metric evaluates the reliability of a template in terms of via usage. Observe that N_{Vias} refers to the amount of vias used inside the cell without considering via redundancy.

$$Via_{total}(i) = \#N_{Vias}(i) \tag{5.12}$$

c) *Via Doubling*: This metric evaluates the possibility of doubling a via, i.e., the possibility of having via redundancy in order to increase the via reliability of a template. Note that the N_{2Vias} refers to the number of vias after doubling as maximum as possible the number of vias in template i.

$$VIA_{double}(i) = \frac{N_{2Vias}(i)}{N_{Vias}(i)} \tag{5.13}$$

This simple set of partial metrics enables a fast evaluation of initial layout templates without requiring an electrical characterization nor a lithography evaluation. The LQM-S will be employed in Chapter 6.1 to evaluate the potential benefits and weaknesses of the preliminary regular templates also presented in Chapter 6.1. In the next section, more elaborated metrics are proposed to provide a more precise analysis of the final regular layout templates detailed in Chapter 6.2.

5.3 Layout Quality Metric using elaborated metrics (LQM-E)

The LQM-S using the simple set of partial quality metrics serves as a fast evaluation framework to obtain an early assessment of cell libraries. However, more elaborated metrics are required to more precisely analyze the impact of applying layout regularity in circuit design. This set of measurements includes aspects such as the lithography parametric yield evaluation detailed in the previous chapter and power and performance analysis. The configuration of the LQM using the elaborated set of measurements is referred as the LQM-E. These elaborated partial metrics are divided in four categories as described in this section. Note that, the LQM-E is used in Chapter 6.4 to evaluate the potential benefits and weaknesses of the final regular templates proposed in Chapter 6.2.

5.3.1 Lithography and cost evaluation metric

The area impact is one of the most important parameters that must be evaluated in a circuit design. However, analyzing the area without considering the yield loss might lead to an unfair comparison with respect to other layout designs. Area and yield must be jointly considered to compare different layout designs and thus obtain the layout implementation that reduces the final cost of the IC design.

In Chapter 4, a lithography estimation model was presented in order to capture the printability distortions occurred in IC designs. This yield model serves as a good approximation to estimate the lithography degradation in circuits, but to properly compare the impact of using different layout design styles, the trade-off between area and yield must be jointly analyzed in order to obtain conclusive results. The area and yield trade-off is here captured by computing the number of Good Dies Per Wafer (GPDW). The GDPW relates the number

of dies or circuits (DPW) with area A_{die} within a wafer of radius R_w (set to 150 mm for all the analysis in this thesis) with respect to the yield as follows.

$$GDPW = Y_{lh} \cdot DPW = Y_{lh} \cdot 2 \cdot \pi \cdot R_w \cdot \left(\frac{R_w}{2 \cdot A_{die}} - \frac{1}{\sqrt{2 \cdot A_{die}}} \right) \tag{5.14}$$

Figure 5.2 illustrates the theoretical trade-off between area and yield and the resulting Good Dies per Wafer for arbitrary areas from $1cm^2$ to $2cm^2$. This result perfectly shows that extreme ultra regular layouts with a huge area penalty, despite its manufacturability benefits, will not produce efficient circuits in terms of GDPW. In that sense, the trade-off between area and lithography degradation, i.e., the GDPW, must be properly analyzed to exploit the benefits of layout regularity due to the non linear relation between area and yield loss. For instance, a design with a 40% yield loss without area penalty will produce similar results as a design with a 60% area penalty without yield loss. Hence, it is preferable a certain amount of area penalty in exchange of lower yield degradation when designing an IC design. During this dissertation, several circuits are analyzed in order to illustrate the relation between the GDPW and the layout regularity.

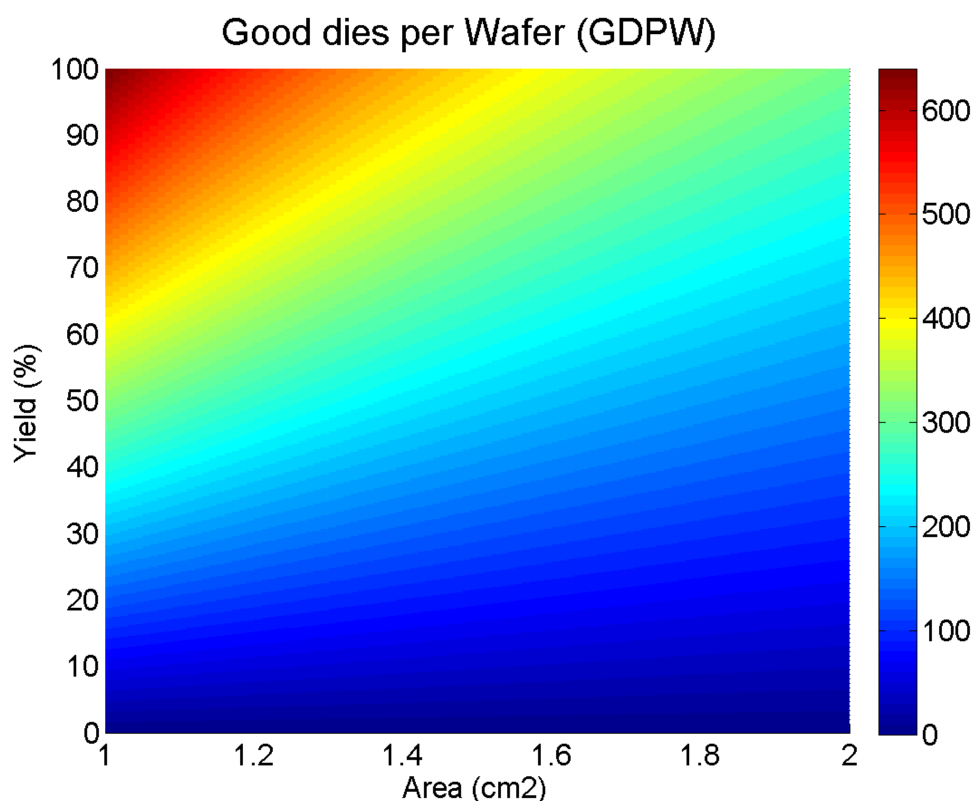


Figure 5.2: Trade-off between yield and area in terms of Good Dies per Wafer for arbitrary areas from $1cm^2$ to $2cm^2$.

Concluding, the area analysis evaluates the compactness of a layout implementation, the yield estimation model captures the relation between layout design and manufacturability and the GDPW analyzes the trade-off between manufacturability and area and thus relating lithography to cost.

5.3.2 Pattern complexity metrics

In the previous section, a simple regularity metric (RM_{proxy}) was proposed to give an initial evaluation of the types of patterns employed in an IC design. The identification of all pattern constructs (PC) that forms a layout design to compute the yield of a circuit in Chapter 4, enables the possibility to analyze the pattern complexity from the point of view of the geometric layout configuration. Thereby, two metrics are proposed in order to quantify the complexity of the layout patterns in terms of lithography complexity.

The first one, is the *Regularity Metric* (RM) which relates the amount of regular pattern constructs with respect to all the pattern constructs employed to create a layout design. The RM tries to capture the usage of the simplest pattern constructs used to build a layout, considered as "regular pattern constructs". The RM is computed as follows.

$$RM = \sum_{i=1}^{layers} \frac{\sum_{j=1}^{N_{Reg_PC}} Reg_PC(i,j)}{\sum_{j=1}^{N_{PC}} PC(i,j)} \tag{5.15}$$

where the Reg_PC represents the amount of regular pattern constructs and PC all the pattern constructs. In this thesis, the minimum set of regular pattern constructs is defined as the minimum group of pattern constructs that enables the possibility to create 1D layouts for a 40nm technology node. The regular patterns here considered are listed next and depicted in Figure 5.3 (and also illustrated in Figure 4.1 in Chapter 4).

1. Class 1: Inside degradation vertex.
2. Class 3: Line-End.
3. Class 14: Line-End Pull Back.
4. Class 17: Poly Edge Center Enclosure.
5. Class 19: Poly Line-End Center Enclosure.

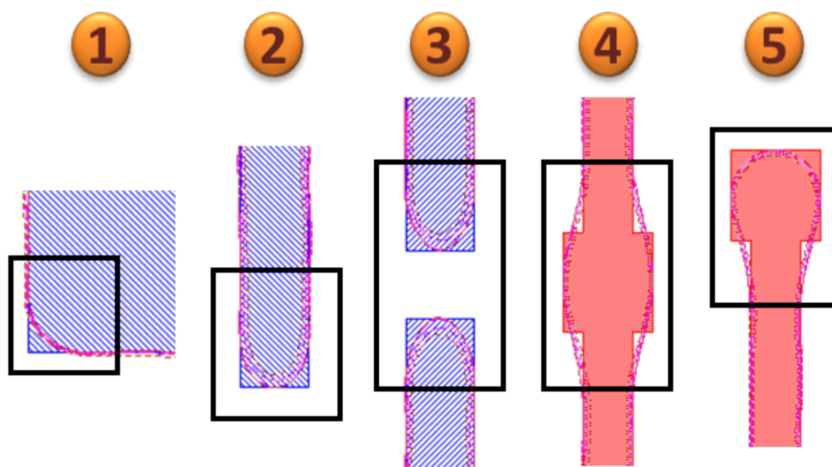


Figure 5.3: Set of regular pattern constructs.

Note that the regular set of pattern constructs can be modified according to the technology employed to better capture the complexity of the layout patterns. This metric, besides illustrating the complexity of the pattern constructs necessary to build an IC design, it also serves to evaluate the degree of layout regularity used in a layout design.

The second metric is the *Pattern Construct Complexity* (PCC). The PCC computes the number of different corrections (NC) of all pattern constructs, i.e., the number of vertexes in the central layout pattern and the number of neighboring edges that form each pattern construct (the definition of a pattern construct is detailed in Chapter 4.2). Note that each different pattern construct is only counted once to compute this metric. This metric tries to capture the complexity of each pattern construct in a layout considering that each element needs a lithography correction in the OPC process. Therefore, simple constructs with fewer vertexes and neighbors are preferred since they will need fewer corrections and will simplify the OPC. The PCC is computed as follows:

$$PCC = \sum_{i=1}^{N_{PC}} NC(i) \tag{5.16}$$

$$NC(i) = \sum V(i) + \sum N(i) \tag{5.17}$$

where the N_{PC} represents the number of different pattern constructs in all layers, the NC is the number of corrections, V is the number of vertexes and N is the number of neighboring edges in each pattern construct.

In summary, the Regularity Metric identifies the amount of simple and non-harmful litho-friendly pattern constructs used in a layout implementation. On the other hand, the Pattern Construct Complexity captures the level of complexity of the pattern construct library used to create a layout design and thus evaluates the complexity of the 2D pattern constructs employed. Moreover, the PCC gives a qualitatively estimation of the OPC effort in a layout design by analyzing the layout variety, i.e., the complexity of each different pattern construct employed in the layout. Therefore, the pattern complexity of different layout implementations can be fairly compared by combining these two metrics.

5.3.3 Routability quality metrics

The routability quality metrics analyze the efficiency of the routing solution of a cell library or a circuit. Firstly, the wire-length of all connections inside the layout is computed. Secondly, the amount of vias employed is calculated. Thirdly, only for cell library evaluation, the number of cells using metal3 in a cell library is analyzed. Lastly, only for cell library analysis, the amount of time that the routing algorithm needs to route a complete library is taken into account. These metrics are detailed next.

1. *Wire-length*: Two wire-length computation strategies are employed whether a cell library or a circuit is analyzed. For cell library analysis, the wire-length (WL) is computed as the minimum wire distance to connect all routing terminals (endpoints of a wire net) of all wire nets in a cell. This WL metric serves to better capture the

impact of using different pattern strategies to route a cell. Hence, the minimum WL can be computed using the following equation:

$$WL(i) = \sum_{i=0}^{N} min(d(i_o, i_e)) \tag{5.18}$$

where N represents the number of nets inside a cell and $d(i_o, i_e)$ is the Manhattan distance between the origin terminal (i_o) and the ending terminal (i_e). On the other hand, the wire-length of a circuit is computed as the overall usage of metal wires since all circuits under analysis in this thesis are routed using the same layout strategy. In this case, the wire-length is directly obtained from the inter-cell routing tool as the overall metal wires used to route a circuit.

Figure 5.4 illustrates in dashed red line the minimum wire-length distance to connect a net starting and ending in the diffusion region (OD) compared to the overall wire-length drawn as a continuous black line. Note that the extra metal wires are necessary to verify the minimum metal area design rules, but they are not considered to compute the wire-length of a cell library.

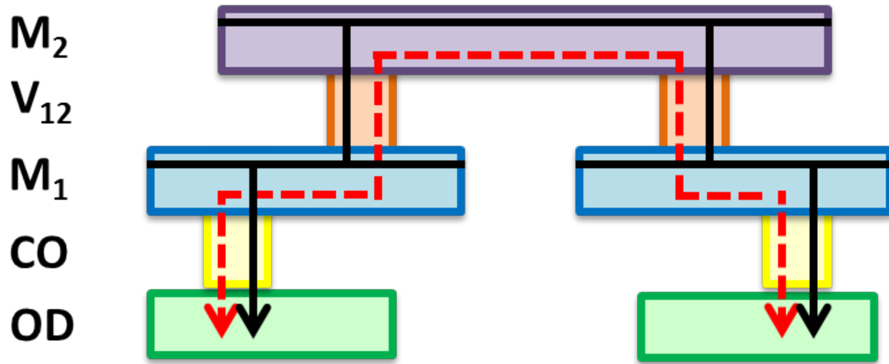


Figure 5.4: Wire-length computation methods: (black line) overall wire-length for circuits; (dashed red line) minimum wire-length for cells; (OD) diffusion; (CO) contact; (M_1) metal1; (V_{12}) via; (M_2) metal2.

2. *Number of Vias*: The via usage is an important parameter to evaluate the efficiency of the routing solution since it evinces the capability of the routing algorithm to maximize the usage of lower metal layers. Additionally, as the number of vias augments, the risk of via failure also increases. Hence, this metric evaluates the routability and reliability of a layout design in terms of vias. For library analysis, this metric only considers the intra-cell vias from metal1 to metal2 (V_{12}) and from metal2 to metal3 (V_{23}). For circuits, the via metric calculates all the vias used in a design.

$$Via_{total}(i) = \#N_{Vias}(i) \tag{5.19}$$

3. *Cells using metal3 (M3)*: Evaluates the number of cells using metal3 in a cell library. Note that the usage of metal3 is only analyzed for cells.

$$M3_{cells}(i) = \#N_{cellsM3}(i) \tag{5.20}$$

4. *Time Complexity (TC)*: Computational time necessary to route a complete cell library. Hence, this metric evaluates the algorithmic complexity of the layout pattern configuration used to route a cell library. Note that more pattern restrictions indicate less possible solutions and normally less computational time. This metric is only applied to cell libraries.

Lastly, in this elaborated evaluation, the via usage is analyzed inside the routability category since it also denotes the efficiency of the routing solution to maximize the usage of lower metals. Even though the via usage can be also analyzed as a reliability aspect as done in the simple layout quality metric detailed in the previous section. Note that via and contact redundancy are other related metrics that can be employed to provide an even more comprehensive evaluation of a design. However, this metrics are not here considered since this elaborated evaluation will be employed in Chapter 6 to compare different layout design libraries that does not employed either via nor contact redundancy.

5.3.4 Power and Performance

The last set of metrics considered for the complete evaluation of the layout is the power and performance measurements. For the cell library case, these measurements are obtained from the library characterization performed with the Cadence ALTOS library Characterizer tool [1]. The parameters computed for each cell are the leakage or static power (P_{leak}), the dynamic power (P_{dyn}), the transition time (rise and fall transition delays, $trans$) and the $delay$ (low to high and high to low delays). Note that the dynamic power measurements include: (1) the *short circuit power* (P_{sc}) which considers the short-circuit power from vdd to gnd and (2) the *switching power* (P_{sw}) due to charging and discharging of internal nodes.

The circuits under analysis in Chapter 6 are created for an specific working frequency and ensuring timing closure (no hold and setup violations) and therefore the delay is not analyzed for circuits. In this case, the Cadence Encounter Digital Implementation System [2], provides measurements for the short-circuit power (P_{sc}), the switching power (P_{sw}) and the leakage power (P_{leak}) consumption. The dynamic power is also computed as the sum of the short-circuit power and the switching power in order to be consistent with the library analysis and besides to fairly compare library and circuits. Hence, the dynamic power is obtained as detailed next.

$$P_{dyn}(i) = P_{sc}(i) + P_{sw}(i) \tag{5.21}$$

5.4 Conclusions

The aim of the Layout Quality Metric (LQM) is to present a versatile and complete metric which allows the designer to globally evaluate the potential capabilities of a layout cell, library or circuit with a single-score taking into account multiple aspects. Versatile since

any parameter can be easily added to the metric and complete since it evaluates all aspects that determine the characteristics of a layout design. The LQM can be leverage by assigning different weights to each evaluation aspect or by modifying the parameters under analysis. Additionally, partial metrics are useful to detect which are the strong and weak points of each layout implementation and therefore decide which cell, library or circuit is the most suitable depending on the product target.

The approach of a single-value to measure the quality of a design can be utilized at several stages of the design flow synthesis to evaluate different library choices. The LQM provides a complete evaluation which allows a designer to discard those layout implementations that do not meet certain requirements at any step of the design flow just by computing several parameters. Moreover, the parameters being analyzed during each phase of the design flow must be properly specified to improve or simplify the evaluation of an IC design during each stage of the layout creation.

In this chapter, two different set of partial metrics are proposed. The LQM-S configured with a simple set of measurements, serves as an easy evaluation framework to provide a simple and fast analysis of a layout design. This set of metrics includes parameters such as area, transistor width size, pattern configuration and via usage. The LQM-S is simple since a small set of parameters is needed to fairly evaluate different layout templates and fast since the parameters are obtained by cell inspection without requiring complex computations.

The yield analysis and the identification of all pattern constructs in Chapter 4, allow the employment of more metrics for layout evaluation in terms of lithography cost considering the GDPW and pattern complexity taking into account the Regularity Metric (RM) and the Pattern Construct Complexity (PCC). Moreover, an electrical characterization of a design enables a more accurate evaluation of the characteristics of a cell or a circuit. Thus, the LQM-E configured with the elaborated set of measurements, provides a deeper insight of the benefits and weaknesses of a layout implementation. Elaborated since it provides a detailed and comprehensive evaluation of a layout design by computing more complex metrics.

In Chapter 6, the LQM metric using both set of measurements is applied to evaluate different library choices with totally different pattern configurations. The LQM is employed to evaluate and compare the regular templates proposed in this dissertation with respect to more traditional 2D standard cell designs. It is important to highlight that the LQM metric is totally independent of the layout template being analyzed and thus it can compare either totally different layouts or rather similar design implementations.

As a future avenue of research, additional measurements can be considered to properly evaluate and compare any layout design. For instance, stress evaluation or double/multiple patterning capabilities are additional aspects that can be used to compute the LQM. Lastly, via and contact redundancy are two other aspects that can be added to the LQM-E, but they are not here considered since the LQM-E will be used in Chapter 6 to evaluate design libraries that does not utilize neither via nor contact redundancy.

5.5 Bibliography

[1] *Cadence Virtuoso Liberate (ALTOS library Characterizer)*, Cadence, 2014. [Online]. Available: http://www.cadence.com/products/cic/liberate/pages/default.aspx

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6

Adaptive Lithography Aware Regular Cell (ALARC) Designs

In this chapter, several 1D layout design styles are proposed with different degrees of layout regularity to outperform traditional 2D standard cell designs for advanced technology nodes. Different trade-offs in terms of area, lithographic yield degradation and pattern complexity are analyzed to evaluate the impact of using layout regularity. However, it is difficult to compare different layout implementations considering several aspects and thus decide the best layout implementation. The Layout Quality Metric (LQM) using two different set of measurements (the LQM-S and the LQM-E) proposed in Chapter 5, is here employed to rank the different designs with a single-score to obtain the best layout design.

Several regular layout design templates with different area impact are firstly introduced. The LQM-S is employed to study the benefits and weaknesses of the preliminary layout implementations. Based on the LQM-S scores, several cell layout libraries following different degrees of layout regularity are proposed for a 40nm technology node, referred as the final Adaptive Lithography Aware Regular Cell (ALARC) Designs. More traditional 2D standard cell libraries are also created in order to analyze the impact of using different pattern strategies. The characteristics of all layout designs implemented vary from a design that uses all layers 1D up to a design where metal1 and diffusion are 2D.

All layout libraries are implemented following the automatic placement and routing scheme described in [1, 2]. Observe that the description of these algorithms is out of the scope of this dissertation, although the definition of the design rules that the routing algorithm requires to implement the different layout design templates is an important aspect detailed in this chapter. The routing scheme is demonstrated to obtain competitive results in terms of computational complexity and wire-length optimization [2]. Thus, by creating all layouts using the same routing tool, a fair comparison can be extracted between the different layout styles since results will be independent of the routing tool employed. Moreover, improved libraries in terms of routability are created by combining the compatible libraries (libraries containing cells with the same height) created with different pattern configurations.

The regular cell libraries created following the final ALARC layout design templates are fully characterized and used to synthesize several ITC'99 benchmark circuits [3]. Area, lithographic yield, pattern complexity, wire-length, electrical characterization and other parameters are employed to compare the different designs. Lastly, the elaborated LQM-E is employed to provide a single-score to evaluate the different proposals.

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6.1 Preliminary regular gridded cell templates

This section details the configuration of several regular gridded cell layouts created manually for a 40nm commercial technology node and used as a starting point to create the final ALARC designs. The Layout Quality Metric using the simple set of measurements (LQM-S), detailed in Chapter 5, is applied to each template in order to evaluate the potential capabilities of each design. Note that, all cells under comparison are routed manually and thus the cell characteristics might be enhanced if a routing algorithm is employed.

6.1.1 Initial regular gridded cell templates

Different regular layout design templates are proposed in order to analyze the effect of pattern regularity on layout design. Each regular template aims to enhance one different layout aspect without using two-dimensional (2D) features: (1) *regularity*, using the most simplistic set of patterns over a single routing grid; (2) *contact redundancy*, aiming to ease the access through multiple contacts; (3) *routability*, simplifying the intra-cell routing with less design rules and; (4) *compactness*, trying to minimize the area penalty. Firstly, the most significant characteristics that these regular templates have in common are outlined next.

- All shapes in the layout are one-dimensional (squares or rectangles), except for poly contact enclosures that contain small jogs to meet design technology requirements.
- All PMOS transistors lie near the top of the cell and all NMOS transistors lie near the bottom of the cell.
- Poly gates are equally spaced shapes placed vertically from top to bottom of the cell.
- All routing layers are placed over a routing grid and thereby each routing layer has an associated fixed pitch.
- The horizontal cell pitch is bigger than the minimum (200nm instead of 180nm) to ease horizontal metal connections.
- Substrate contacts are placed over the power rails on the boundaries of the cells.

These guidelines are used as a starting point to create several layout implementations aiming to enhance different cell aspects. The specific layout design constraints defined for each template are described next.

1. *Template A (referred as F1D in Chapter 4) - Focus on Regularity*: This 14 track template aims to maximize layout regularity at the cost of area penalty compared to less regular designs as detailed next. Firstly, all transistors in the layout have the same width. Secondly, metal1 is used for horizontal connections and metal2 for the vertical ones. Thirdly, it only utilizes metal1 and metal2 shapes with minimum width and variable length. The minimum area rule for metal1 connections with minimum width

forces a large metal1 shape and a consequent placement restriction on the adjacent OD contact connections and thus the access to diffusion through multiple contacts is difficult to achieve.

Some routing difficulties arise due to the minimum cell pitch used in the vertical axis. For instance, it is not possible to place a S/D contact on the first routing track that occupies the diffusion region of a transistor when the poly-silicon gate of that transistor is contacted at minimum distance to the active region. On the other hand, this pitch configuration avoids conflicts with power supply connections from adjacent cells. These two features are illustrated in Figure 6.1.

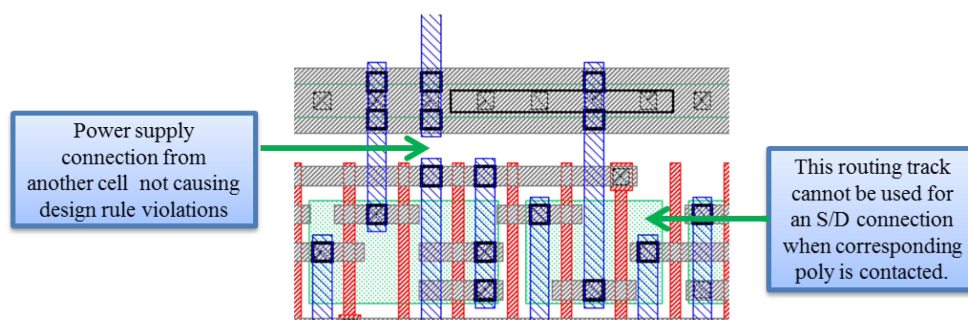


Figure 6.1: S/D contact placement limitation and inter-cell power supply routing without conflicts.

2. *Template B - Focus on Contact Redundancy*: This 14 track template is configured to maximize layout regularity while at the same time improving contact redundancy as described next. Firstly, the major difference with respect to the other designs lies in the direction used for metal connections, i.e., metal1 is used for vertical connections and metal2 for the horizontal ones. This metal configuration makes the access to diffusion through multiple contacts easier to achieve in practice for this template. Note that the employment of multiple contacts minimizes current losses when accessing to diffusion and combats CMP resistance variations [4].

   Secondly, the cell pitch in the vertical axis is the minimum. Thirdly, metal3 is utilized occasionally for complex cells in the vertical direction. Fourthly, this template aims to maximize regularity by having a common transistor size and the same wire width for all connections in a metal layer. The metal1 layer uses wide metal1 connections in order to better satisfy design technology rules. Lastly, metal1 requires two vertical routing grids in order to contact poly gates and diffusion. The employment of these two metal1 grids makes hard to contact the poly gates in between active regions and it makes difficult the access to the power supply rails through a direct metal1 vertical connection.

3. *Template C - Focus on Routability*: This 11 track template simplifies the intra-cell routing by increasing the cell pitch in the vertical axis and despite this increase, cell area can be reduced by diminishing the number of cell tracks as outlined next. Firstly, this pitch configuration eliminates the restriction of not being able to place a S/D contact on the first routing track that occupies the diffusion region of a transistor when its poly gate is contacted at minimum distance to the active region, as depicted in Figure 6.2. Secondly, metal1 is used for horizontal connections and metal2 for the

vertical ones. Thirdly, regularity is slightly sacrificed in order to simplify the intra-cell routing: (1) two different metal2 widths are utilized where the wider metal2 wires serve to avoid conflicts with power supply connections from adjacent cells (as shown in Figure 6.2) and; (2) active regions can contain any number of equal width transistors, but each diffusion strip can have different widths. Lastly, it uses the same metal1 configuration as template A, i.e., metal1 shapes with minimum width and variable length.

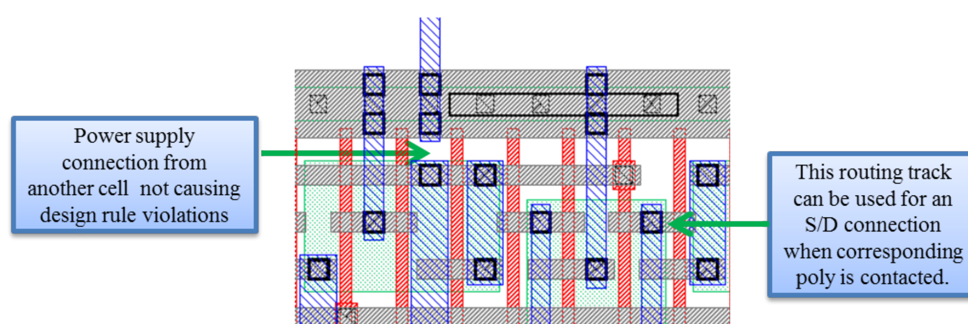
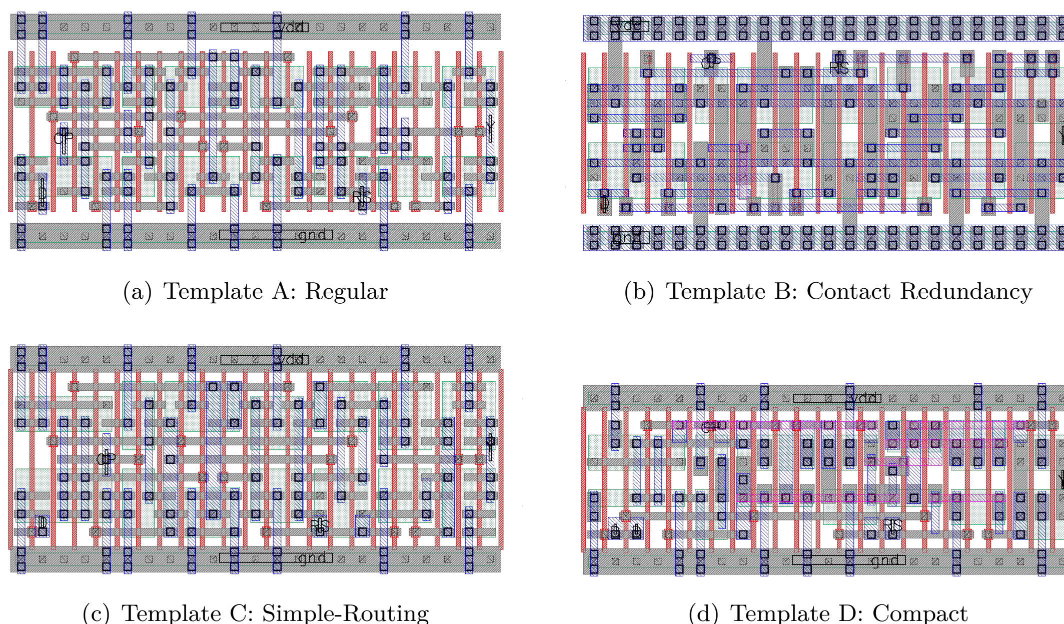


Figure 6.2: Inter-cell power supply routing without conflicts due to the employment of wider metal2 wires and the S/D contact placement without limitations.

4. *Template D - Focus on Area*: This 9 track template seeks to create more compact cells by penalizing inter-cell routing capabilities and by sacrificing metal1 regularity as analyzed next. Firstly, the cell pitch in the vertical axis is bigger than the minimum. Secondly, the configuration of metal1 connections is slightly different; vertical connections uses wide metal1 shapes and horizontal connections uses narrow or wide metal1 shapes. Note that despite using metal1 connections in both vertical and horizontal directions, lithography interactions between those patterns do not cause significant lithography imperfections due to the proper configuration of metal1 widths and the sufficient spacing between the wide and narrow connections, as proved in section 6.2.

   Thirdly, metal2 shapes, used for vertical connections, have two different widths. Fourthly, horizontal metal3 connections are used when intra-cell routing becomes infeasible due to the reduced number of horizontal routing resources available (lower number of tracks). Note that increasing the number of tracks would decrease the usage of metal3 connections and besides metal3 is only required for the case of complex cells. Lastly, active regions can contain any number of equal width transistors, but each diffusion strip can have a different width.

Figure 6.3 depicts a D Flip Flop with reset created following the regular templates detailed throughout this section. In this preliminary study where the layouts are created manually, only a D Flip Flop is analyzed since creating all cells manually is impractical. Note that this cell represents one of the most complex logic gates used in a library and thus it determines the cell height of the library (and consequently the area) and besides its complex intra-cell routing serves to evaluate several other layout aspects captured with the LQM-S. In the next section, the LQM-S is employed to evaluate the different D Flip Flops with reset created to evince the characteristics of the different layout design styles.



(a) Template A: Regular

(b) Template B: Contact Redundancy

(c) Template C: Simple-Routing

(d) Template D: Compact

Figure 6.3: D Flip Flop with reset created following different regular templates. The layer mapping is as follows; (red) poly; (green) diffusion; (grey) metal1; (dark blue) metal2; (pink) metal3.

6.1.2 Layout Quality Metric (LQM-S) Evaluation

The Layout Quality Metric using the simple evaluation metrics (LQM-S) is here employed to analyze the potential capabilities to create a D Flip Flop with reset for a 40nm commercial technology node using the regular layout templates previously outlined. Moreover, the NP1D layout design style from Nangate that employs 2D metal1 and diffusion (previously detailed in section 2.2.4) is used for comparison with respect to the regular templates here proposed.

Table 6.2 shows the main characteristics of the D Flip Flops with reset previously detailed. In this table, the weak and strong aspects of each template can be perfectly observed. In terms of compactness, the best results are obtained with template D and NP1D. Template D minimizes the area overhead by smartly employing metal1 vertical and horizontal and thus penalizing layout regularity and by using metal3 inside the cell. On the other hand, template NP1D produces compact cells due to the employment of 2D metal1 and diffusion shapes at the cost of less layout regularity.

In terms of routability, templates A and C do not employ any metal3 connection inside the cell and thus more routing resources are reserved for the inter-cell routing. Although considering other routability metrics, the most versatile design that admits bigger and smaller transistors is template NP1D. In terms of reliability, template B has the highest contact redundancy ratio, template NP1D employs the lowest number of vias and all templates have practically the same via redundancy ratio, with the exception of template B where less via connections can be duplicated.

Table 6.2 shows the weighted impact of each partial metric computed to obtain the LQM-S for the different D Flip Flops with reset. Note that the LQM-S (in general, the LQM) is

Table 6.1: Main characteristics of the D Flip Flop with reset.

Characteristics	Category	A	B	C	D	NP1D
$Area\ (um^2)$	Compactness	9.02	9.02	8.6	7.04	7.04
RM_{proxy}	Regularity	0	6.25	6.25	12.5	43.75
$M3_{wires}$	Routability	0	1	0	6	4
$W_{OD,max}\ (nm)$	Routability	760	1040	1030	620	1240
$W_{OD,min}\ (nm)$	Routability	760	240	502	276	240
CO_{double}	Reliability	1.29	2	1.54	1.49	1.59
Via_{total}	Reliability	57	63	60	57	23
Via_{double}	Reliability	1.7	1.27	1.68	1.68	1.7

lower bounded by 0, representing the maximum quality that can be achieved for both the partial metrics and the LQM-S. The weights have been adjusted so the 4 categories under evaluation have similar relative importance into the final score.

Table 6.2: Layout Quality Metric using the simple measurements (LQM-S) applied to a D Flip Flop with reset.

LQM-S	Category	α	A	B	C	D	NP1D
Q_{Area}	Compactness	1.9	53.4	53.4	42.22	0	0
$Q_{RM_{proxy}}$	Regularity	1.25	0	7.81	7.81	15.63	54.69
$Q_{M3_{wires}}$	Routability	3	0	3	0	18	12
$Q_{W_{OD,max}}$	Routability	0.35	13.55	5.65	5.93	17.5	0
$Q_{W_{OD,min}}$	Routability	0.08	17.33	0	8.73	1.2	0
$Q_{CO_{double}}$	Reliability	0.5	17.68	0	11.59	12.81	10.33
$Q_{Via_{total}}$	Reliability	0.1	14.78	17.39	16.09	14.78	0
$Q_{Via_{double}}$	Reliability	0.7	0	17.77	0.76	0.72	0.25
$LQM-S$	-	-	116.75	105.01	93.13	80.63	77.26
$Best$	-	-	5	4	3	2	1

In general, the 2D NP1D standard cell design achieves the best results in more individual aspects than any of the other templates at the cost of a bad layout regularity score. Considering only the regular designs (templates A-D), each template obtains its best score for its respective aspect aimed to be enhanced. However, it is difficult to assure which is the best template just analyzing individually each metric and thus the LQM-S is required to extract a more conclusive assessment of the different layout design templates.

The best layout template with the lowest LQM-S score is template NP1D, although template D has approximately the same quality, as detailed in Table 6.2. Observe that template NP1D presents a bad score in terms of layout regularity which will be translated into higher yield loss, whereas template D penalizes the routability and reliability aspects in order to avoid area penalty at the cost of an slight decrease of the layout regularity. Templates A and B obtains the worst layout quality scores, despite of having the best regularity and contact redundancy scores respectively. Template C achieves better scores than templates A and B,

but worse results compared to template D. Lastly, the main problem of templates A, B and C is the excessive area penalty compared to templates D and NP1D.

6.1.3 Preliminary layout design templates selected

The layouts proposed throughout this section have been the first attempt to study the impact of layout regularity in cell design. The analysis of the main characteristics of each template and the application of the LQM-S permit to select the best layout implementations to be explored in an automatic environment.

The main drawback of most of the regular designs (templates A, B and C) is the excessive area penalty introduced in order to map a complex cell design like a D Flip Flop with reset. An enhanced version of template C with lower area overhead by reducing the horizontal pitch and adding more layout regularity by using single width wires per layer is proposed in the next section. Moreover, template D that slightly sacrifices layout regularity in order to be more competitive in terms of area is also improved by reducing the horizontal cell pitch. Therefore, an enhanced version of templates C and D are the designs selected to be created automatically.

The layout templates proposed in this section are designed for the minimum cell height necessary to route a complex cell (D Flip Flop with reset) using the maximum transistor size that fits inside the cell. This configuration provides an analysis of the minimum area that ensures the routability of a cell without considering transistor sizes, i.e., without considering neither performance nor power consumption. Therefore, the regular designs proposed in the next section are created using the same transistor netlist as the original NP1D Nangate library in order to take into account both power and timing in the same conditions.

Finally, the LQM-S has been employed to have an early evaluation of a complex cell with different template implementations, but a complete cell library and circuits must be also analyzed to have a deeper insight of the potential capabilities of each layout design style. Moreover, more elaborated measurements, such as power, performance and yield must be considered to more precisely compare regular and traditional non-regular designs.

6.2 Adaptive Lithography Aware Regular Cell (ALARC) designs

This section details the configuration of the final regular gridded cell layouts automatically created for a 40nm commercial technology node, referred as the Adaptive Lithography Aware Regular Cell (ALARC) designs. Adaptive, since these regular implementations are not created based on a fixed structure like regular via-configurable designs detailed in Chapter 2.2.3, instead they are configurable like a standard cell design. Note that different degrees of layout regularity are analyzed in this section, except for poly-silicon gates that preserve 1D in order to reduce channel length variations [5].

All layout designs here presented are automatically implemented using competitive transistor placement and routing algorithms detailed in [1, 2]. Although the explanation of these algorithms is out of the scope of this dissertation.

The regular gridded templates proposed are a more efficient layout configuration of templates C and D presented in the previous section. Moreover, two other layout designs using bidirectional metal1 connections are also detailed. Firstly, the main modifications that all theses templates share are outlined.

- Poly-silicon gates can only be contacted between both active regions (not allowing contacts at the end of the poly gates augments the transistor width).
- Cell pitch in the vertical axis is bigger than the minimum in order to simplify cell routing at the cost of extra area overhead.
  - This pitch simplifies the design rules, e.g., reduces contact placement restrictions.
  - It allows the possibility to use horizontal wires wider than the minimum width and thus reducing the minimum length of an horizontal wire that verifies the minimum area rule.
- Power supply rails are displaced half track from the last routing track in order to better accommodate the power rails.
- Cell pitch in the horizontal axis is the minimum pitch determined by the poly-silicon gate design rules (180nm). This aspect is the most significant difference with respect to the templates described in the previous section which permits more compact designs.
- Signal pins are placed on metal2 and power/ground pins are placed over the supply wires on metal1.
- Metal2 connections can only be placed on columns that enable the access to diffusion. This configuration simplifies the routing by limiting the space of possible metal2 connections without affecting the feasibility of the routing solution.
- Metal3 is only employed when intra-cell routing becomes infeasible otherwise.

These layout design constraints are used as a basis to create different templates. The specific layout design guidelines are detailed next.

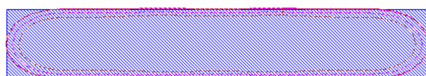
1. *Template F1D - Full 1D*: Template F1D is based on template C which is mainly characterized by the simplicity of its pattern constructs, i.e., it aims to maximize regularity to its maximum expression at the cost of some area penalty compared to less regular designs. The main modifications of this template are provided next. It only uses one single metal1 wire width and one single metal2 wire width and both can have variable length. Metal1 wire width is increased above the minimum and thus alleviating the placement restriction on the adjacent OD contact connections when using large metal1 shapes to satisfy the minimum metal1 area rule, as can be observed from Figure 6.5(a).

   The large metal1 shapes force the transistor size (diffusion regions) to occupy at least two rows in order to ensure the routability of a cell, as depicted in Figure 6.5(a). Hence,

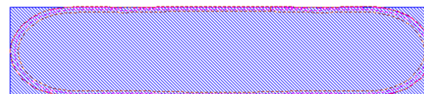
minimum transistor size can not be employed in this template. The access with metal1 to poly gates between active regions is difficult without allowing metal1 jogs and thus two rows must be reserved between them in order to contact the gates.

2. *Template H1D - Half 1D*: Template H1D is based on template D which seeks to improve two disadvantages of the F1D template by sacrificing layout regularity. On the one hand, this template enables the possibility of using minimum size transistors, i.e., it can employ diffusion regions that occupy 1 cell row. On the other hand, this template eases the access to diffusion through multiple contacts.

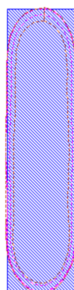
   Vertical connections use wide metal1 shapes (not that wide compared to template D) and horizontal connections use only narrow metal1 shapes. As the width of the vertical wire augments, the interaction towards the horizontal wire is lower; as the width of the horizontal wire increases, the degradation suffered on this wire is less significant and; as the spacing augments, the degradation on the horizontal wire decreases. Figure 6.4 depicts a wire configuration with minimum width and spacing design rules that suffers lithography degradation and it also illustrates the wire width and spacing configuration used in this template that does not suffer significant lithography distortion. Lastly, despite using a metal configuration more flexible than template F1D, it also requires two rows in between the active regions in order to contact the poly gates.

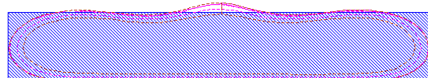


(a) Minimum design rule wire. The width of the horizontal wire is 70nm.

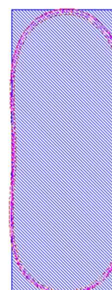


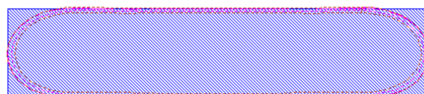
(b) Configured wire. The width of the horizontal wire is 90nm.





(c) Minimum design rule wire with an opposite neighbor. The width of the vertical wire is 70nm and the spacing is 70nm.





(d) Configured wires with an opposite neighbor. The width of the vertical wire is 110nm and the spacing is 80nm.

Figure 6.4: Comparison of different metal wire configurations. Layout is drawn in blue and simulated contour in purple. (a,c) Minimum design rule wire widths and spacing; (b,d) Configured wire widths and spacing for template H1D.

3. *Template M2D - Metal1 2D*: Template M2D aims to produce more competitive cells in terms of area by penalizing layout regularity. This layout design style also utilizes the same regular diffusion as the previous designs but it uses metal1 2D connections running in both directions, vertical and horizontal, and it permits the employment of jogs. The wire width is the same utilized in the previous template, and therefore the lithography interactions between horizontal and vertical wires do not cause harmful degradation. The lithography distortion will come from the corners introduced to ease the routability. Note that this metal configuration, only requires one row between active regions in order to contact the poly gates.

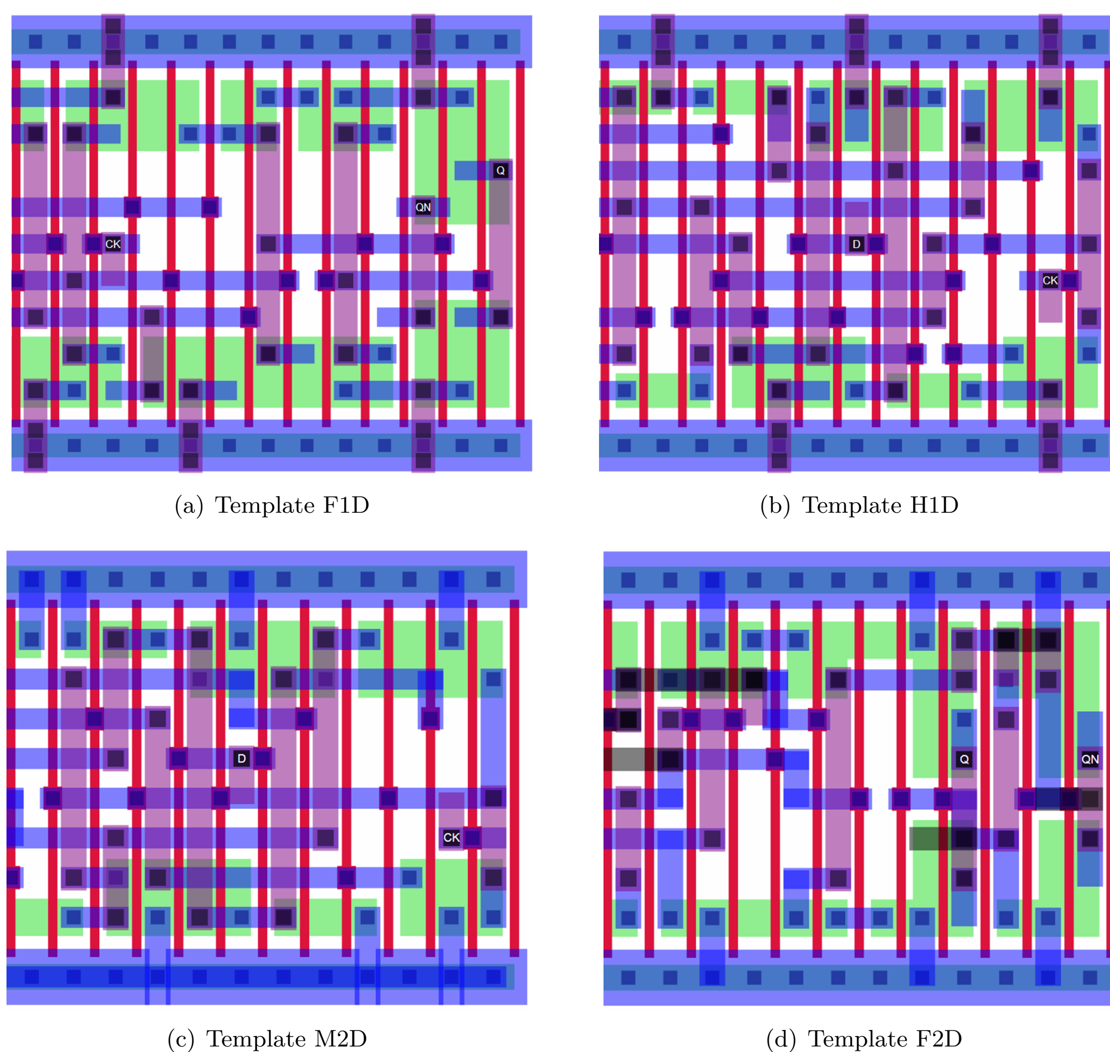
   The difference between this template and traditional bidirectional metal1 designs lies in the limited metal1 wire width configuration. The M1D template only employs a single wire width for horizontal connections and another wire width for vertical connections, whereas traditional designs employ arbitrary metal1 wire widths. This configuration reduces the amount of different pattern configurations, simplifies the automatic generation of this layout template and it also eases the printability prediction.

4. *Template F2D - Fully 2D*: This template is rather similar to template M2D, with the exception that it enables the possibility to employ 2D diffusion regions when needed in order to decrease the cell width. Template F2D is taken as reference to compare the quality of the different regular designs previously detailed with respect to more traditional 2D layout designs. This template mimics the placement of the NP1D 40nm layout design library detailed in section 2.2.4, but it is routed using the same routing tool as the previous templates. The placement is preserved to obtain a realistic area comparison with respect to a commercial design library. However, the intra-cell routing is modified, so all cell libraries under comparison are created with the same routing engine [2] and thus results will be independent of the efficiency of the routing scheme.

Figure 6.5 illustrates part of a D Flip Flop created following the templates outlined throughout this section. The next section details how to convert these design template guidelines into a set of gridded design rules that can be employed in a gridded routing algorithm to obtain a layout cell library. Using these templates, several cell libraries will be created to evaluate the implications of layout regularity on cell design in section 6.4.

6.3 Automatic regular layout library creation

Using the layout design styles detailed in the previous section, several standard cell libraries are created in order to test their efficiency to map different benchmark circuits. This section firstly describes how to convert the layout design guidelines into simple gridded design rules to be employed in a cell router [2]. Then, the design flow to automatically create the cell libraries with different degrees of layout regularity is briefly outlined. Lastly, this section details how to combine the compatible cell libraries to obtain improved libraries.



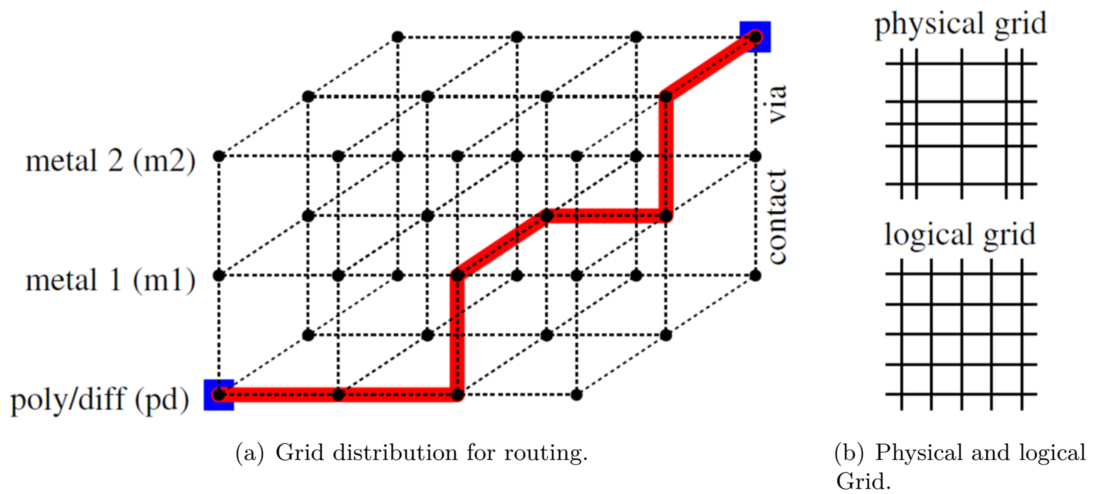
(a) Template F1D (b) Template H1D

(c) Template M2D (d) Template F2D

Figure 6.5: Part of a D Flip Flop created following different regular templates. The layer mapping is as follows; (red) poly; (green) diffusion; (blue) metal1; (purple) metal2; (black) metal3.

6.3.1 Design rules methodology

This section details how the design template guidelines previously outlined are specified as design rules that can be utilized in the grid-based router described in [2]. The design rules are constructed based on the graph definition of the routing problem where the routing region is represented by a 3D grid graph, as depicted in Figure 6.6(a). The grid graph is defined as a set of vertexes (logical grid points) and edges that connect these grid points. Even though the logical grid assumes unit-length edges, the physical grid might have rows and columns separated by different distances depending on the layout design guidelines specified, as depicted in Figure 6.6(b). Thereby, an edge of N_{GU} grid units in the logical grid is equivalent as an edge of N_{PU} physical units in the physical grid layout. Using the physical to logical conversion units, the grid-less design rules described in *nm* in the design rule manual are transformed into logical grid units in order to be mapped in the router engine.



(a) Grid distribution for routing.

(b) Physical and logical Grid.

Figure 6.6: 3D gridded routing model.

The design rules used to create the different templates are outlined in Table 6.3 and some examples are depicted in Figure 6.7. Two different types of design rules are considered, the *mandatory rules* (1-30) and the *recommended rules* (31-34). The first set of rules are the necessary rules that must be utilized to verify the technology design rule constraints (DRC) provided in the design rule manual. On the other hand, the recommended rules are optional rules that are utilized to ease the routing of a cell by limiting the space of solutions. For example, the diffusion region and the power rails are only allowed to be connected from the first available row in the active region since connecting them from other diffusion rows is less efficient in terms of routing resources and wire-length. As a future avenue of research, more recommended rules can be added, for instance, the usage of contact or via redundancy.

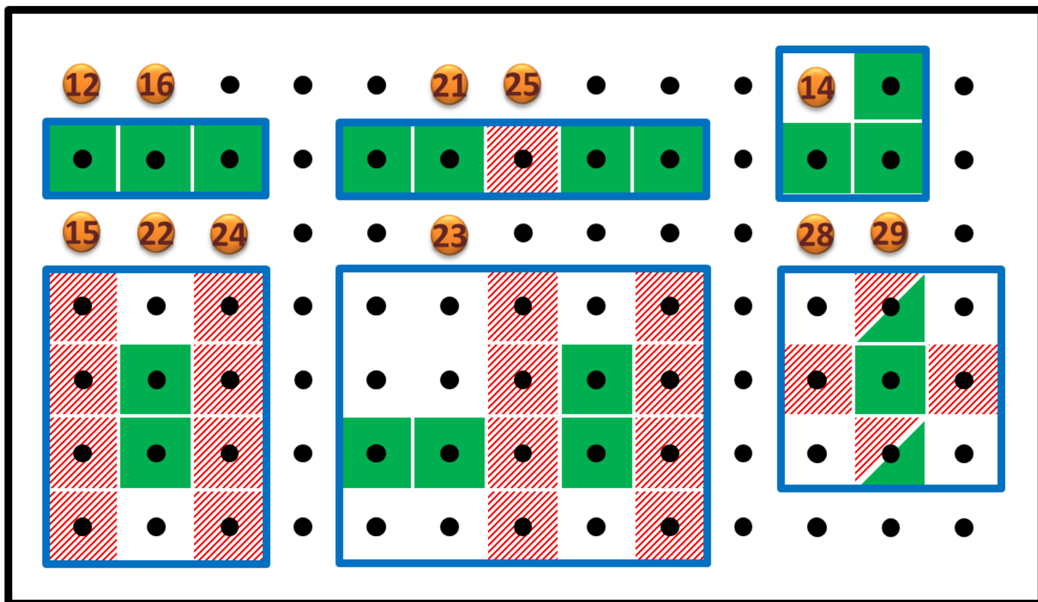


Figure 6.7: Graphical representation of some gridded design rules. The green filled color represents a pattern that occupies a grid point; the red diagonal lines prohibit the placement of a pattern of the same layer; the red/green (diagonal/filled) indicates that only a pattern belonging to the same net connection can be placed at that grid point.

Table 6.3: Gridded design rules used for the cell library creation. (In green) mandatory rules; (in blue) recommended rules.

#	Design Rule	F2D	M2D	H1D	F1D
1	1D poly-silicon gates are placed on odd columns in the vertical direction.	green	green	green	green
2	1D diffusion; transistors in the same active strip must have the same width.		green	green	green
3	2D diffusion permitted; transistors can have different sizes in the same strip.	green			
4	M1 can only be routed with 1D rectangular segments.			green	green
5	M1 can only be routed in the horizontal direction.				green
6	M1 can be routed in the horizontal and vertical direction.	green	green	green	
7	M2 can only be routed in the vertical direction.	green	green	green	green
8	Signal pins must be placed in M2 in even columns (over active).	green	green	green	green
9	Power/Ground pins must be placed in M1 over the power rails.	green	green	green	green
10	M3 can only be routed in the horizontal direction.	green	green	green	green
11	M3 horizontal can not be placed over power rails.	green	green	green	green
12	M1 horizontal wire segments must have at least length 2.	green	green	green	green
13	M1 vertical wire segments must have at least length 1.	green	green	green	green
14	M1 vertical and horizontal (L shapes) must have at least length 1 in both directions.	green	green		
15	M2 vertical wire segments must have at least length 1.	green	green	green	green
16	M3 horizontal wire segments must have at least length 2.	green	green	green	green
17	M1 horizontal is thin.	green	green	green	green
18	M1 vertical is thick.	green	green	green	green
19	M2 vertical is thick.	green	green	green	green
20	M3 horizontal is thin.	green	green	green	green
21	The space between two horizontal M1 wire segments in the same row must be at least two grid units.	green	green	green	green
22	M1 vertical wires cannot have another neighboring wire in the 4 surrounding rows in the previous and following columns.	green	green	green	green
23	The space between a vertical M1 wire segment and a horizontal M1 wire segment must be at least two grid units in the horizontal axis.	green	green		
24	M2 vertical wires cannot have another neighboring wire in the surrounding columns.	green	green	green	green
25	The space between two horizontal M3 wire segments in the same row must be at least two grid units.	green	green	green	green
26	A contact implies: (Bottom) PO/DIFF; (Top) M1.	green	green	green	green
27	A VIA_MXMY implies: (Bottom) metal MX; (Top) metal MY.	green	green	green	green
28	A contact (or via) cannot have any other contact (or via) in the adjacent vertical surrounding grid points unless they belong to the same net.	green	green	green	green
29	A contact (or via) cannot have any other contact (or via) in the adjacent horizontal surrounding grid points.	green	green	green	green
30	Omit rule 28 when considering the power rail row and the adjacent row if the power rails are displaced half track.	green	green	green	green
31	Supply connections from diffusion to power rails can only be made from the first diffusion row in M1.	blue	blue		
32	Supply connections from diffusion to power rails can only be made from the first diffusion row in M2.			blue	blue
33	A contact cannot have any other contact in the adjacent vertical surrounding grid points in the poly layer.	blue	blue	blue	blue
34	M2 can only be placed in even columns, i.e., only over diffusion (simplifies routing).	blue	blue	blue	blue
Total number of rules		30	30	29	29

The employment of a gridded router where most of the design rules are already verified by construction of the layout grid reduces the number of design rules required to create these templates. Hence, converting a layout into a grid vastly simplifies the rule definition of any kind of layout design. Moreover, the total number of design rules used to create each template is practically the same independently if the layout is more or less regular. Thus, the pattern complexity of a set of design rules must be analyzed in terms of computational complexity, i.e., computing the time that the routing algorithm needs to obtain a feasible solution given a set of design rules. In the library analysis (section 6.4), the time complexity to create the cell libraries is evaluated.

6.3.2 Design Flow

The layout design templates and the design rules are used to create different cell libraries to analyze the implications of using layout regularity. A 40nm 10 track cell library from Nangate based on template NP1D, described in section 2.2.4, is selected as a starting point to create the layout libraries for the F1D, H1D, M2D and F2D designs. The cell library is composed of 266 instances including logic and sequential cells. Note that the F2D directly extracts the placement from the NP1D library. Figure 6.8 depicts the flow to synthesize a cell starting from the SPICE netlist or GDSII layout of a cell of the NP1D library and ending in a GDSII layout. The steps of the design flow are described next.

1. **Discretization of the Netlist:** The grid-less SPICE transistor netlist of the NP1D library specified in nm (W_{nm}) is transformed into a gridded netlist in grid units (W_{GU}) using the following equation:

$$W_{GU} = \left[\frac{W_{nm} - 2 \cdot OD_{ext}}{pitch_Y}\right] \tag{6.1}$$

   where the OD_{ext} is the diffusion extension in the vertical direction from the last track occupied by the diffusion and the $pitch_Y$ is the separation between rows in the cell. The W_{GU} is the nearest integer in order to obtain a netlist as similar as possible to the original one. Note that the highest integer should be selected for a high performance configuration and the lowest for low power purposes. Thus, the netlist is transform into logic units which represent the number of tracks or rows that each transistor occupies in the layout. Lastly, the minimum value of W_{GU} depends on the layout design style and the technology rules and thus the W_{GU} of transistors too small must be normalized to a valid minimum value. In this work, only template F1D requires transistors with a minimum value of W_{GU} of 2 since it requires at least two tracks to contact the diffusion; all other templates can have transistors of W_{GU} of 1.

2. **Transistor Folding**: A transistor folding algorithm detailed in [1] is applied for netlists with transistors not fitting in the cell height. The width of large transistors is folded into small fingers equalizing the width of all transistors in the same P or N strip. The transformation is done in such a way that the total width of each group of identical transistors is as similar as possible to the original width.

3. **Placement and Routing**: The transistor placement and routing (P&R) is done utilizing the algorithms presented in [2].

4. **Layouter**: The Layouter transforms the logical representation of a cell obtained from the P&R algorithms in grid units into a GDSII layout in *nm* units.

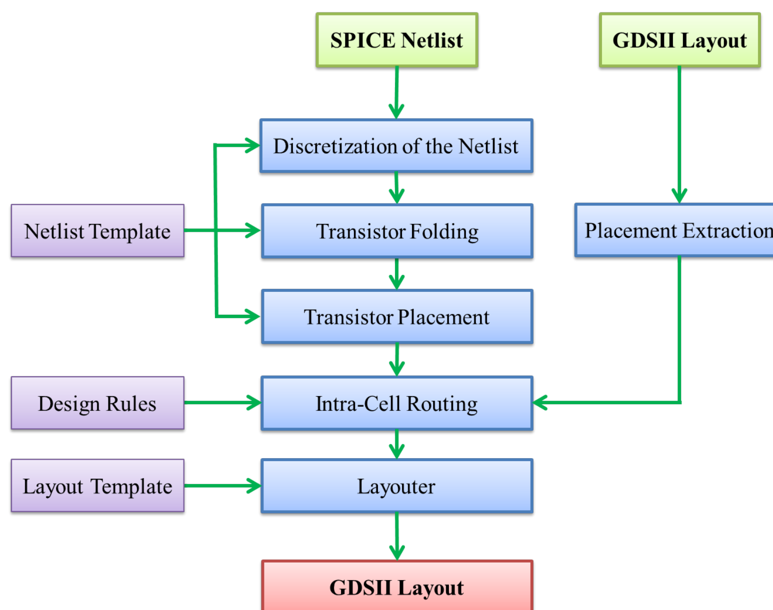


Figure 6.8: Library creation flow: from netlist to GDSII layout.

Each step requires some specific inputs: (1) the *Netlist Template* includes specific cell aspects such as the cell height, distribution of P and N transistors, number of tracks, pitches and all the necessary parameters to configure the size of transistors; (2) the *Design Rules* (detailed in section 6.3.1) are the necessary layout design guidelines that the intra-cell router must follow to create a cell according to the design style specified and; (3) the *Layout Template* contains the sizes of each layout feature to be drawn in the GDSII in *nm* and it also includes specific design rules that can be applied outside the routing algorithm, such as the size of a wire in a specific direction or the usage of multiple vias over the power supply rails.

It is important to highlight that as many design rules are mapped into the Layout Template, less rules are applied to the routing algorithm and thus the cell routing is simplified. Lastly, all GDSII cells are DRC (Design Rule Checker) clean by construction and thus verification time is reduced. Although DRC and LVS (Layout Versus Schematic or Netlist) is automatically checked for all cells in order to ensure that cells are perfectly routed and they correspond to the specified netlist.

6.3.3 Methodology to combine compatible libraries

Improved libraries in terms of routability (wire-length, number of vias, etc.) can be created by combining cells from different libraries in order to improve the overall characteristics of the libraries by sacrificing a design constraint. Libraries with the same cell height can

be combined into a new library with improved aspects at the cost, for instance, of layout regularity. Therefore, a reference library can be improved with cells from other libraries that ameliorate any of the routing criteria.

The methodology to obtain the improved libraries is as follows. Considering all the compatible libraries, one of the libraries is taken as the reference one. Then, each cell in the reference library is compared to the same cell in other compatible libraries. If the cell from the other libraries verifies one of the routing criterion as long as the previous criteria are not worst compared to the reference cell, the resulting improved library will select the cell from the compatible library. Otherwise, the resulting improved library will contain the reference cell. Therefore, cells selected from compatible libraries will always be better for a given criteria, equal to the previous criteria with higher priority and might be worse or better than the other criteria with less priority compared to the reference cells. The routing criteria to select the best cell sorted from most to less priority are enumerated next:

1. Wire-length reduced and ViasM2-M3 and ViasM1-M2 not increased.
2. ViasM2-M3 reduced.
3. M3 reduced and ViasM1-M2 not increased.
4. ViasM1-M2 reduced.
5. M2 reduced.
6. M1 vertical reduced.
7. M1 horizontal reduced.

The highest priority is set to minimize the wire-length of the layout as long as the number of vias is not increased. Note that more priority is given to reduce the metal1 vertical over the metal1 horizontal in order to decrease the number of corners. These priorities aim to outperform the global characteristics of a cell library, but they can be sorted differently according to the design requirements.

The libraries previously outlined in section 6.2 were created for a specific degree of layout regularity and here the compatible ones are combined into new libraries with improved routing characteristics. The F2D and the M2D libraries can be combined into a new library since both have 10 tracks as the original NP1D library, as shown in Table 6.4. On the other hand, the number of tracks of the H1D and the F1D libraries is increased to 11 tracks since the constraint of needing two rows between the active regions to contact the poly gates requires an extra track compared to the NP1D design. Hence, two additional libraries are created, the BMF2 library formed combing the best cells from the M2D and the F2D library, and the BHF1 created with cells from the H1D and the F1D library.

In the BMF2 case, the M2D is used as reference library since it employs the same transistor placement as the regular designs and besides the M2D presents better printability due to the employment of a more regular pattern configuration. In the BHF1 case, the H1D is used as reference since this template does not have the F1D library restriction of not using minimum size transistors and besides the decrease in layout regularity does not introduce lithography distortions.

6.4 ALARC designs evaluation

In this section, a detailed analysis of the ALARC templates proposed in this dissertation for a commercial 40nm technology node is presented. Firstly, the different cell libraries are evaluated considering different metrics. Secondly, several ITC'99 benchmark circuits [3] are created using these cell libraries in order to assess the potential characteristics of each library. Thirdly, a more comprehensive analysis of the ITC'99 b17 benchmark circuit is provided. Lastly, the layout quality metric is employed to evaluate globally the characteristics of the cell libraries and the b17 circuit.

6.4.1 Cell library analysis

A library of 266 instances including combinational and sequential cells for each different layout design style described in section 6.2 is created. Moreover, two additional libraries are obtained by combining the previous libraries as detailed in section 6.3.3. All cell libraries are created using as reference the same SPICE netlists from the 40nm NP1D library. The electrical characterization has been obtained considering the RC parasitic extraction of the GDSII layouts. The steps to perform the library characterization are detailed next.

1. The *.lef* technology information is generated using the Cadence Abstract Generator from the GDSII library database [6].
2. The interconnect parasitic extraction (RC) is performed for each cell using the Interconnect Extractor tool StarRC from Synopsys which creates SPICE netlists from a GDSII database [7].
3. The required electrical views (timing and power) in *.lib* format based on the current source delay data advanced timing models CCS (Composite Current Source) are created using the Cadence Virtuoso Liberate (ALTOS library Characterizer) [8].

An early estimation of yield has been performed over 117680 replicas of the same library in order to obtain a global area around a 1 cm^2. The configuration of the yield model is the same explained in Chapter 4, where the most regular designs (F1D, H1D and BHF1) are adjusted following the same strategy as the most regular design, template A (referred as F1D in Chapter 4), and the other less regular designs (M2D, F2D and BMF2) are calibrated considering the same configuration as the NP1D design. The design margin considered, an 11%, is the same chosen for the layout evaluation in section 4.3.3.

Table 6.4 details the characteristics of the 6 libraries showing that the regular implementations outperform the manufacturing yield at the cost of around 9% of area overhead. Although the resulting good dies per wafer is higher in the regular layouts and thus justifying the area increase. In terms of pattern complexity, both metrics, the PCC and the RM, show that the regular layouts will require a smaller OPC effort compared to the 2D designs.

Table 6.4: Cell library evaluation. Yield related analysis (first group) is applied to 117680 instances (N_i) of each library, other results are computed for only one library.

LQM	BMF2	F2D	M2D	BHF1	H1D	F1D
$Area\ (um^2)$	849.8	851.9	837.5	920.3	920.6	920.3
$Area_{Ni}\ (cm^2)$	1	1	0.99	1.08	1.08	1.08
PVI_{mean}	0.108	0.107	0.108	0	0	0
$N_h\ x10^8$	3.81	3.98	3.73	0	0	0
Y_{lh}	82.11	81.61	82.34	100	100	100
$GDPW$	525	521	535	588	588	588
PC_{types}	174	184	179	20	25	4
PCC	1026	1184	1054	68	91	14
$RM(\%)$	84.22	84.04	84.07	97.50	95.96	100
$Cell\ tracks$	10	10	10	11	11	11
$Cells\ M3$	6	10	18	3	3	4
$WL\ (um)$	1780	1832	1999	1774	1841	1786
$Vias$	1218	1283	1742	1681	1841	1711
$TC\ (h)$	3.72	1.76	1.96	1.75	1.2	0.55
$Delay\ (a.u.)$	1.00	1.041	1.003	0.997	0.998	0.997
$Trans\ (a.u.)$	1.00	1.062	1.003	1.002	1.003	1.003
$P_{leak}\ (a.u.)$	1.00	0.934	0.999	1.081	1.083	1.080
$P_{dyn}\ (a.u.)$	1.00	0.972	1.013	1.023	1.022	1.024

The employment of metal3 inside a cell must be kept at minimum during cell design in order to reserve resources for the inter-cell routing. In these libraries, the number of cells using metal3 is lower for the more regular libraries. This metal3 reduction is directly associated to the cell height increase necessary in the regular implementations (F1D, H1D and BHF1) to route the cells. Note that increasing the number of tracks would decrease the usage of metal3 connections in the less regular designs (M2D, F2D and BMF2) at the cost of extra area overhead. Although this metal3 usage is justified since it is only required for the case of complex cells and the area benefits are more important, as shown in the circuit analysis.

It is important to highlight that the pattern restriction applied on regular layouts, vastly simplifies the space of routing solutions to create a cell and thus layouts with simpler pattern configurations are routed faster. The routing algorithmic effort reduction is a significant advantage of regular designs, specially to create application specific cells [5] (logic cells created specifically for a given circuit) instead of traditional standard cell libraries.

The power and performance evaluation shows that regular designs present around an 8% more leakage power consumption, whereas the dynamic power is only increased a 2% compared to the non-regular designs, the M2D and the BMF2. In terms of performance, the delay is practically the same in all regular designs with respect to the same 2D libraries, the M2D and the BMF2. However, when considering the F2D library which mimics the placement of the commercial NP1D design, the leakage power consumption is decreased a 15% and the dynamic power is reduced a 5% with respect to the regular layouts at the cost of a 4% larger delay and a 6% larger transition times. This power and performance differences are

probably caused by the distinct transistor placement algorithm employed to create the F2D library. Although the results are coherent since the lower power consumption derived into larger delays as expected.

The cell library analysis has shown that regular layouts outperform 2D designs in some aspects, but not in all of them as expected. However, it is difficult to say which is the best library considering individually all these parameters. Moreover, a cell library evaluation does not provide a complete picture of the characteristics of a library, as shown in the next section. Thus, a more detailed evaluation considering a circuit analysis and a comprehensive layout quality metric are necessary to select the best library option, as detailed in section 6.4.5.

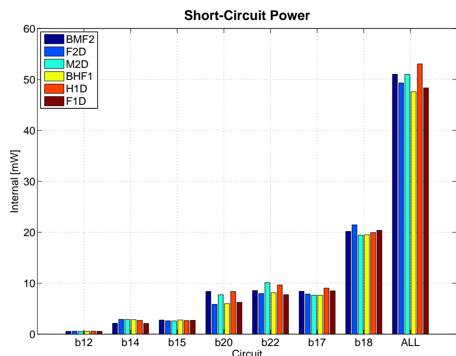
6.4.2 ITC'99 benchmark circuits evaluation

Several circuits from the ITC'99 benchmarks [3] are placed and routed with Cadence EDI system [9] to test the cell libraries. The procedure to implement these circuits is as follows.

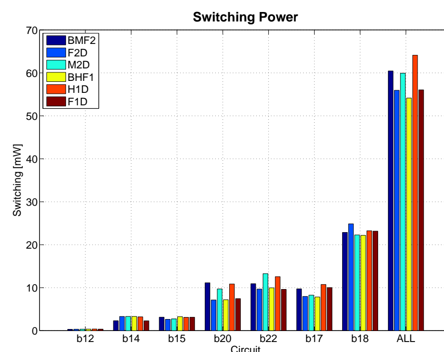
1. The different circuits are synthesized using the Encounter RTL Compiler [10] for a working frequency of 500 Mhz using *.lib* and the *.lef* library data.
2. The Place and Route (P&R) of all synthesized circuits is performed with the Encounter Digital Implementation (EDI) System from Cadence [9].
3. The circuit density is fixed at 70% for all benchmarks.
4. All circuits are optimized to correct glitch and setup/hold violations caused by incremental delays due to coupling capacitance in the 40nm technology node and thus timing closure is verified for all designs.
5. All circuits are checked for geometrical errors (design rules) and connectivity (all nets routed).

Figure 6.9 illustrates several circuit characteristics obtained directly from the EDI system for seven ITC'99 benchmark circuits. Note that *ALL* represents the overall results by adding the results of each of the circuits. As can be observed from Figure 6.9, results vary slightly from circuit to circuit and thus they are particular to the circuit under analysis. This might happen due to the different selection of logic cells during the synthesis of a circuit and the efficiency of the Place and Route algorithm to construct the layout of a circuit and satisfy the timing closure. Therefore, the main conclusions with respect to the different layout design templates are based on the analysis of the overall results.

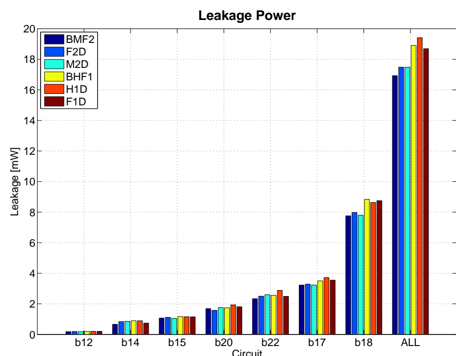
In terms of area overhead, between 12.5% to 18% area penalty is obtained with the regular layout designs with respect to the best 2D layout (M2D). The area penalty is higher than the area overhead obtained with the library analysis where a 9% area penalty was observed. The routing metrics are similar to the area analysis where the regular designs present an overhead between 3% to 9% in the via usage and a larger wire-length between 3% to 11.5% compared to the less regular implementations.



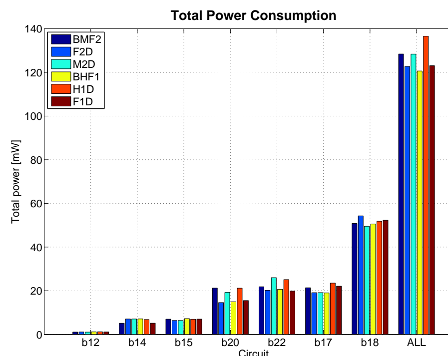
(a) Short-Circuit Power.



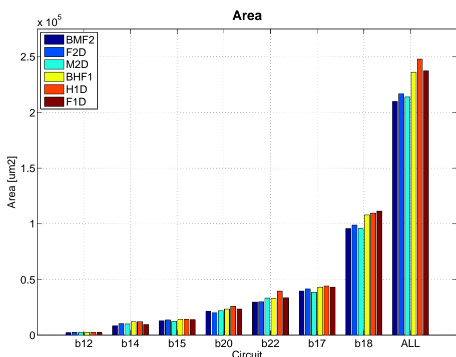
(b) Switching Power.



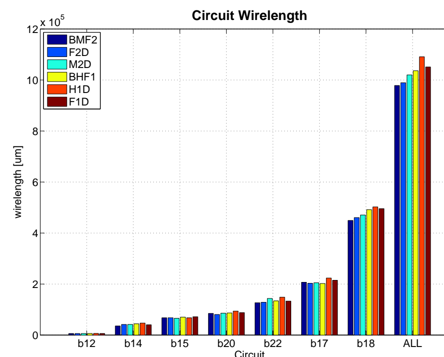
(c) Leakage Power.



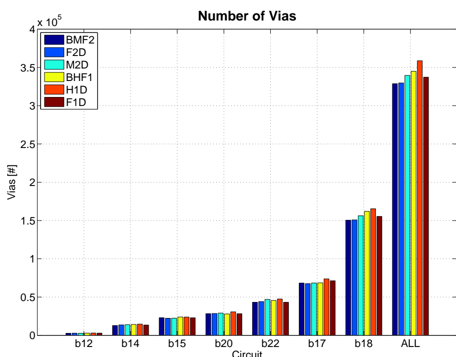
(d) Total Power.



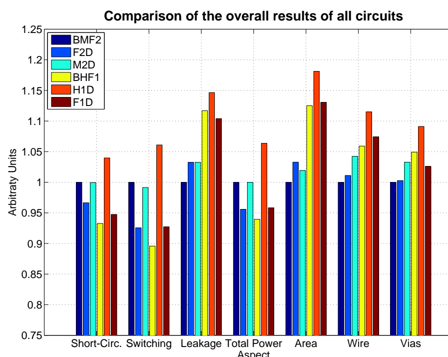
(e) Area.



(f) Wire-length.



(g) Via Usage.



(h) Summary of the *ALL* results normalized with respect to the BMF2.

Figure 6.9: ITC'99 benchmark circuit analysis. *ALL* represents the overall results by adding the results of each of the circuits.

Regular layouts are also the designs with more leakage power consumption with a 10% to 15% increase. However, different results are obtained compared to the library analysis when evaluating the dynamic power consumption. In this case, the dynamic power consumption is independent of the layout design style employed, having both layout design styles, libraries with high and low dynamic power consumption. The design with the lowest dynamic power consumption considering both the short-circuit (1.5% to 11% reduction) and the switching power (3% to 17% reduction) is the regular BHF1. Although in the library analysis, this design had a 5% higher dynamic power with respect to the best design, the F2D.

The differences observed between the regular and the non-regular designs when considering the circuit evaluation are not the same presented in the library analysis. In some aspects, such as area and leakage consumption, the results are slightly higher for the circuit analysis, but following the same trend. However, the results are different in terms of dynamic power, via usage and wire-length. Considering the area and the routability metrics, the 2D designs are better, but taking into account the overall power consumption, the 1D templates obtain better results. Therefore, the results depend on the synthesized circuit, the design style in some cases and the final routed layout.

In conclusion, selecting the best design library analyzing only the library results is not enough to properly evaluate a layout design style at least when comparing libraries that present small differences between them. Therefore, a comprehensive circuit analysis is necessary to better capture the potential benefits and weaknesses of a layout design style. In the next section, the b17 benchmark circuit is analyzed in more detail by providing also a yield and a pattern complexity evaluation.

6.4.3 Density analysis based on the b17 benchmark circuit

In this section, a density analysis based on the b17 benchmark circuit is provided. The 70% fixed density (space occupied by the cells not considering fillers nor buffers) is increased to evaluate if this configuration is significant in terms of area overhead. Cells with a bigger cell area have more routing resources and thus the circuit might be routed for a higher density. However, the increase in the circuit density, might lead to other errors such as timing violations (paths not meeting the setup or hold time), unrouted nets and geometrical (design rule) errors. Figure 6.10 illustrates the amount of errors and the area of the b17 benchmark circuit implemented following the BMF2 and the BHF1 layout design styles for different circuit densities. Note that, for all densities, the b17 circuit is optimized to meet the timing constraints by correcting glitch and setup/hold violations.

The density analysis clearly shows that the difference in area of the b17 circuit between the two design styles is the same independently of the density specified. Thus, the 70% configured density perfectly serves to compare the area of the different implementations.

In terms of violations, for densities above 90%, the amount of errors is so high that makes the routing solution totally infeasible. For densities below 90%, the timing closure is assured for both designs and the geometrical and routing errors are reduced, but not always fully corrected with a lower number of errors in the BHF1 implementation. In these cases, the

number of errors does not follow any trend, e.g., the BHF1 for 90% density has no errors but for 87.5% or 85% it has errors despite more routing resources are available for smaller densities. Therefore, for densities smaller than 90%, the number of errors depends more on the routing tool than in the layout design style. Moreover, the amount of errors is so small that probably these errors can be corrected manually. In conclusion, the bigger area of the regular cells does not provide any benefit to route the b17 circuit.

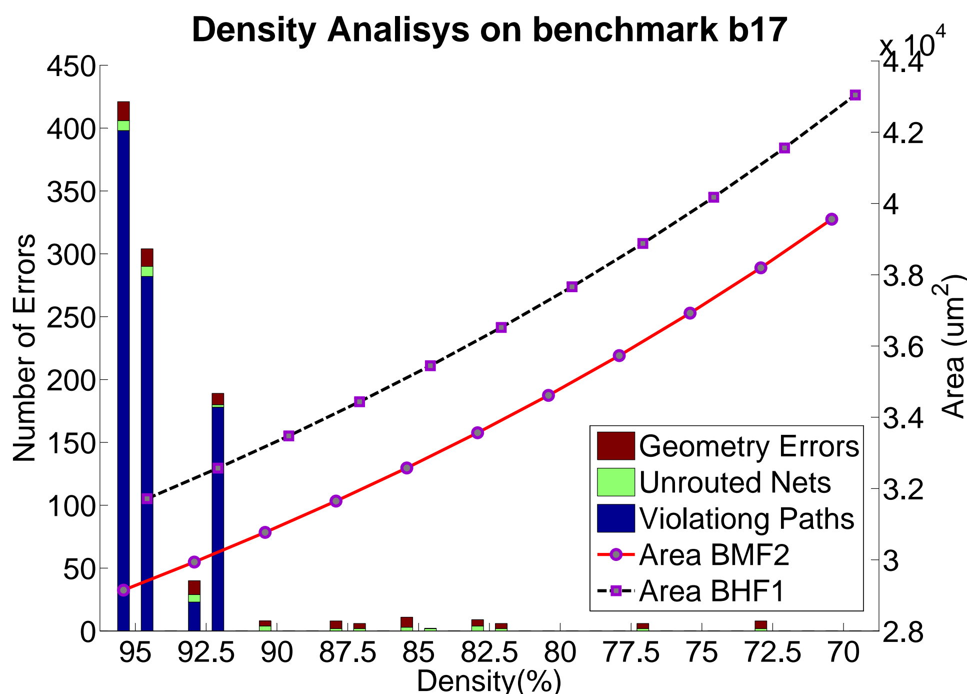


Figure 6.10: Density impact on violations and area. For each density, the bar on the left side corresponds to the BMF2 design style and the bar on the right side corresponds to the BHF1. The *violating paths*: paths not meeting hold/setup timing; the *unrouted nets*: nets not completely connected and; the *geometry errors*: violations on the design rules.

6.4.4 A detailed evaluation of the b17 benchmark circuit

Table 6.5 shows the lithography, pattern complexity, routability and electrical evaluation of the b17 circuit. Note that the yield model used to evaluate the b17 benchmark circuit is calibrated for a specific design margin of 11%, as detailed in Chapter 4.3. In this case, the regular b17 implementations present a lower yield compared to the library analysis (5% yield loss) whereas the 2D designs present a better yield (5% improvement). This difference in yield is totally reasonable because the inter-cell routing to create the circuits is configured to preferably use regular patterns, but 2D patterns are allowed. Consequently, the inter-cell routing uses more complex patterns than the regular design libraries, but less complex than the 2D libraries. This causes a yield reduction for the 1D circuits and a yield improvement for the 2D circuits compared to the library prediction.

In terms of area penalty, the regular layouts have between 12% to 15% more area than the best 2D layout design, the M2D. This area overhead is slightly higher than the area penalty

found in the library analysis (around 9%). However, when comparing the regular layouts with respect to the F2D design, the area penalty is between 4% to 7% which is smaller than the expected from the library analysis. When considering both the yield and the area results, the best design in terms of GDPW is the M2D, when in the library analysis the best designs were the most regular layouts (BHF1, H1D and F1D). The worst circuit in terms of GDPW is the F2D design like in the library analysis. In summary, considering the circuit analysis, regular layouts are not the best option in terms of manufacturing cost, but not the worst designs. Note that the precision of the yield results depends on the yield calibration and the silicon data available as detailed in Chapter 4.3.

Table 6.5: b17 benchmark circuit evaluation. Yield related analysis (first group) is applied to 2528 instances of each b17 circuit, other results are computed for one circuit.

LQM	BMF2	F2D	M2D	BHF1	H1D	F1D
$Area\ (cm^2)$	1	1.05	0.97	1.09	1.12	1.09
PVI_{mean}	0.103	0.101	0.108	0.107	0.105	0.118
$N_h\ x10^8$	2.62	2.91	2.47	1.28	1.32	1.06
Y_{lh}	87.11	86.35	88.64	95.15	95.09	95.44
$GDPW$	557	525	585	557	542	558
PC_{types}	1241	1181	1221	959	967	712
PCC	10184	9631	9814	7862	8008	5871
RM	81	81.01	80.9	88.28	87.46	91.47
$WL\ (mm)$	207	203.1	205.1	202.2	223.8	215
$Vias\ x10^3$	68.3	67.6	68.4	68.5	73.8	71.3
$P_{leak}\ (mW)$	3.23	3.29	3.23	3.5	3.72	3.55
$P_{sc}\ (mW)$	8.42	7.87	7.65	7.65	9.05	8.52
$P_{sw}\ (mW)$	9.73	7.97	8.27	7.84	10.75	10.03
$P_{dyn}\ (mW)$	18.15	15.84	15.92	15.49	19.8	18.55

The pattern construct complexity metric shows that the amount of unique corrections necessary for the regular layouts has increased due to the employment of 2D features for the inter-cell routing. Although the PCC shows that the regular implementations still require less OPC effort than the 2D layouts. The usage of 2D patterns in the regular layouts can be clearly appreciated with the regularity metric; the regularity metric for regular layouts has decreased from 100% to approximately 89%. Additionally, the lack of a full regular inter-cell routing tool (the EDI system introduces jogs in the inter-cell routing even if regular patterns are the preferred option), makes not possible to evaluate a fully regular layout implementation.

The via and wire-length usage for regular layouts are higher compared to the non-regular cases, with the exception of the BHF1 design that presents the smallest wire-length. Leakage consumption as was expected from the previous results, it is also higher for the regular implementations and thus it depends on the layout design style. On the contrary, the dynamic power consumption directly depends on the circuit implementation more than in the layout design template

The particular results of the b17 circuit are not exactly the same as the overall results for all circuits. As depicted in Figure 6.9, the circuit under analysis directly influences the layout design style evaluation, although the detailed analysis of the b17 circuit serves to illustrate how layout regularity affects to a circuit of a considerable size. These results have evinced that in some aspects the regular layouts present better evaluation metrics than the 2D layouts and besides none of the layout design styles outperform the others in all aspects. Hence, a global layout quality metric that combines several aspects is required to finally decide between one design style over another.

6.4.5 Layout Quality Metric Evaluation

The Layout Quality Metric (LQM-E) described in Chapter 5.3, enables the possibility to globally evaluate libraries and circuits with a single-score considering individually different weighted aspects. Table 6.6 shows the evaluation of the different cell libraries and the b17 benchmark circuit, where the lowest Q indicates the best design. Note that the α weight is configured to give more importance to the good dies per wafer since it includes the area and yield analysis, and the other weights are adjusted to give a reasonable score between the library and the circuit analysis.

The library analysis (Table 6.6(a)) indicates that the regular cells are globally more efficient than the 2D layout designs when considering all the library aspects (Q_{libA}) and the reduced subset used to evaluate the circuits (Q_{lib}). More specifically, the F1D presents the best score, although the BHF1 practically achieves a similar score. In this case, the complete and the reduced evaluation give similar results. On the other hand, the non-regular F2D library design presents the worst quality, although the M2D has practically the same score. However, in this case, the best 2D design is the F2D when considering all the library aspects, whereas the best design is the BMF2 with the reduced set of metrics.

The circuit analysis evinces the need of evaluating circuit designs in order to properly select the best layout design style. Table 6.6(b) clearly shows that the best circuit is implemented following the M2D library and the second best is the BHF1 library as the Q_{b17} indicates. This change in the scores is mainly caused by the different values obtained in the good dies per wafer metric; regular libraries have the highest amount of GDPW, whereas this metric is better for 2D layout designs in the circuit analysis.

Observe that each circuit implementation has its benefits and weaknesses and the best circuit does not outperform all aspects, even though globally is the best option. Hence, it is important to highlight that it is up to the designer to properly configure the weights assigned to each evaluation metric depending on the requirements of a design and the characteristics of the technology employed. Consequently, the best layout option might be different depending on the weight distribution. Lastly, note that the LQM-E is only applied to the b17 circuit and this layout design evaluation might vary depending on the circuit under analysis.

Table 6.6: Layout Quality Metric with the elaborated set of measurements (LQM-E). The Q_{lib} metric includes the same parameters as the Q_{b17} and the Q_{libA} considers more evaluation metrics for the library analysis.

(a) Library analysis.

C-LQM	α	BMF2	F2D	M2D	BHF1	H1D	F1D
Q_{GDPW}	4	42.8	45.9	36.3	0	0.16	0
Q_{PCC}	0.001	7.2	8.4	7.4	0.4	0.6	0
Q_{RM}	0.4	6.3	6.4	6.4	1	1.6	0
Q_{WL}	0.4	0.14	1.3	5.1	0	1.5	0.3
Q_{Vias}	0.2	0	1.1	8.6	7.6	10.2	8.1
$Q_{P_{leak}}$	1	7.1	0	7	15.8	15.9	15.7
$Q_{P_{dyn}}$	1	2.9	0	4.2	5.2	5.1	5.3
Q_{Delay}	2	0.6	8.8	1.2	0	0.3	0.1
Q_{Trans}	2	0	12.3	0.6	0.4	0.7	0.6
Q_{TC}	0.01	5.8	2.2	2.6	2.2	1.2	0
Q_{M3}	0.01	1	2.3	5	0	0	0.3
Q_{lib}	-	66.5	63.0	75	29.9	35.1	29.4
Best	-	5	4	6	2	3	1
Q_{libA}	-	73.8	88.6	84.3	32.5	37.3	30.4
Best	-	4	6	5	2	3	1

(b) b17 benchmark evaluation.

C-LQM	α	BMF2	F2D	M2D	BHF1	H1D	F1D
Q_{GDPW}	4	19.1	40.9	0	19.3	29.3	18.3
Q_{PCC}	0.1	7.4	6.4	6.7	3.4	3.6	0
Q_{RM}	0.4	4.6	4.6	4.6	1.4	1.8	0
Q_{WL}	0.4	0.94	0.17	0.58	0	4.3	2.5
Q_{Vias}	0.2	0.22	0	0.23	0.28	1.8	1.1
$Q_{P_{leak}}$	1	0	1.9	0	8.4	15.2	9.9
$Q_{P_{dyn}}$	1	17.2	2.3	2.8	0	27.8	19.8
Q_{b17}	-	49.3	56.1	14.9	32.7	83.8	51.6
Best	-	3	5	1	2	6	4

6.4.6 ALARC templates conclusions

Selecting one layout design style over another is rather difficult in practice if circuit design evaluation is not performed. For the 40nm technology node employed, layout regularity can outperform traditional 2D standard cell design depending on the circuit implementation. It is important to remark that none of the layouts under analysis uses 2D poly gates, since layouts with this configuration are expected to suffer large channel length printability variations and thus they degrade excessively the manufacturing yield (as previously shown in Chapter 4).

The best results are obtained for the M2D design library that employs metal1 2D and the rest of the layers 1D. Although the BHF1 library that uses all patterns 1D, but metal1 running in both directions for some cells also achieves very good results. The other 2D libraries (F2D and BMF2) obtain worse global scores than the BHF1 and therefore showing that 2D layouts not always lead to the best solutions. Note that for the regular case, the improved regular library BHF1 achieves the best global results for the b17 circuit among the regular designs, whereas the BMF2 does not provide the best non-regular design. Therefore, the usage of the enhanced libraries can be useful depending on the circuit implementation.

One of the main problems of layout regularity is the area penalty. This area overhead directly depends on the requirements of the netlists. This layout evaluation uses a netlist which represents a trade-off between a low power library (9 tracks) and a high performance library (14 tracks) compared to other commercial libraries using the same technology here employed. For high performance cells that require big transistors, the higher cell height gives more room to use regular patterns. On the other hand, 2D patterns and metal3 inside the cell are necessary to route compact cells using small size transistors for low power purposes. Thus, the results here presented clearly evince that for high performance cells, regular layouts are the best option, but for low power cells 2D patterns and more intra-cell metal3 are needed to obtain more compact cells.

The yield loss suffered in the layout designs evaluated is not that significant, since the 40nm technology node is a mature process and the amount of degradation (without considering 2D poly-silicon gates) is not that critical. However, considering the impact of lithography imperfections on future technology nodes, more degradation in the printed patterns is expected, as detailed in Chapter 1 in Figure 1.3. Therefore, the good dies per wafer in future technologies will increase for the regular layout implementations and decrease for the non regular designs due to the higher lithography printability degradation expected for complex patterns. Consequently, the regular designs will obtain much better scores and then layout regularity should be employed to achieve a better pattern resolution without requiring complex patterning techniques with a higher mask complexity.

6.5 Conclusions

In this chapter, the final Adaptive Lithography Aware Regular Cell Design (ALARC) templates for a real 40nm technology node were proposed. These templates were used to synthesize and characterize a library containing 266 cells including combinational and sequential cells. The layout design styles with different degrees of layout regularity were evaluated, among other parameters, in terms of area, lithographic yield, pattern complexity, wire-length, power and performance. In addition to all these metrics, the single-score layout quality metric (LQM) was employed to provide a global evaluation of the different designs.

The layout quality metric evinced that a library analysis is not sufficient to determine the efficiency of a design and thus justifying the need of a benchmark circuit evaluation to properly select the best layout design implementation. The analysis of the benchmark circuits showed that regular layout designs can globally outperform the 2D designs depending

on the final routed and timing optimized circuit. Thus, the choice of a layout design style directly depends on the efficiency to map a given circuit, specially when small differences between the different libraries were observed (all libraries were created using the same SPICE netlists, but with small modifications to adapt them to the specific layout configuration).

The regular libraries only presented a 9% area penalty with respect to the libraries using bidirectional metal1. The b17 benchmark circuit implemented with the BHF1 and the F1D presented a 4%, 9% and 12% area penalty with respect to the non-regular layout designs using bidirectional metal1, the F2D, the BMF2 and the M2D respectively. In terms of manufacturing yield, the regular libraries obtained around an 18% yield improvement compared to the libraries using bidirectional metal1, whereas the b17 analysis showed only a 7% yield improvement.

The LQM-E evinced that the best layout implementation for the b17 circuit corresponded to template M2D which employs all layers 1D with the exception of metal1 bidirectional. Although the difference with respect to the best 1D design, the BHF1, is not significant and it is mainly caused by the lower number of GDPW obtained. Moreover, regular layouts can outperform 2D standard cell designs according to the LQM-E results depending on the layout implementation since the BHF1 design with a regularity index of 97.5% outperformed the other 2D designs, the F2D and the BMF2.

The different circuits implemented showed that the choice of the best layout design style directly depends on the efficiency to map a given circuit, specially when small differences exist between the different libraries. Furthermore, the efficiency of the synthesis tools to create a circuit is also important and thus a more efficient logic synthesis considering printability metrics can outperform the implementation of a circuit.

The layout evaluation was particular to the 40nm technology node used where the benefits of layout regularity in terms of manufacturability are not that significant. The important aspect to highlight is that a regular design with a yield improvement higher than the area overhead in percentage will produce designs with a higher number of good dies per wafer. Hence, repeating the same study for smaller technology nodes where higher printability variations are expected, causing a lower yield for complex patterns, might show that future IC designs must be created using a more regular layout design style.

Future avenues of research might include the creation of new layout designs with a pattern restriction for specific geometries that would cause excessive lithography degradation, but allowing some 2D shapes in order to reduce the area penalty and achieve a better global layout quality metric. Layout designs can be also improved by considering contact and via redundancy in the routing algorithm. The benefits of using a litho-optimized logic synthesis using the layout quality metric might be also another interesting topic of research. Moreover, the routing algorithm enables the possibility to define design rules for multiple patterning techniques. Thus, the definition of the design rules for regular layouts to create multiple patterning friendly libraries by construction, ensuring that the complete circuit is multiple patterning friendly, could be another topic of research. Lastly, the most important avenue of research would be to test the benefits of these regular layout implementations in smaller technology nodes.

In conclusion, the employment of layout regularity led to competitive results being in several cases better than 2D designs, e.g, the b17 circuit based on the BHF1 library obtained better results than the b17 implementation using the F2D library. Thus, for future technology nodes were more printability variations are expected, layout regularity might become the preferred option to continue driving high performance and power efficient devices at lower cost.

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7

Conclusions

This thesis was focused on addressing future generation challenges in the semiconductor industry by developing regular cell *layout designs* and *layout evaluation* methodologies considering a *layout analysis* in terms of lithography variability. This section summarizes the main contributions of this dissertation, outlines the publications and conference participations derived from this thesis and concludes providing some interesting future avenues of research and a final remark on layout regularity on future technology nodes.

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7.1 Key Contributions

The main goal of this dissertation was to find the degree of layout regularity necessary to combat lithography variability and at the same time not jeopardize the overall layout quality of a design. The four main contributions that have been addressed in this thesis in order to accomplish this objective were: (1) the definition of several layout design guidelines to mitigate lithography variability on IC designs; (2) the proposal of a parametric yield estimation model to evaluate the lithography impact on layout design; (3) the development of a global Layout Quality Metric (LQM) including a Regularity Metric (RM) to capture the degree of layout regularity of a layout implementation and; (4) the creation of gridded regular layout design templates to outperform line-pattern resolution, referred as Adaptive Lithography Aware Regular Cell (ALARC) designs.

Firstly, a complete evaluation of the lithography variability impact on line-pattern resolution was provided in order to firstly justify the need of layout regularity and secondly evaluate the impact of lithography variation on the printed patterns. Using lithography simulations to highlight several common imperfections caused by sub-wavelength lithography, several layout design guidelines that must be considered to minimize lithography perturbations even for regular litho-friendly design styles were provided. Furthermore, a gate biasing methodology to compensate channel length variations in regular fabrics that considers the non-rectilinear gate effect (NRG) and both layout dependent and across field variations was proposed. This design level methodology provides a fast and simple layout technique to estimate the best single-gate length configuration to compensate channel length variations and not jeopardize the electrical characteristics of a circuit.

Secondly, a parametric lithography yield estimation model to predict the amount of lithography distortion expected in a printed layout due to lithography hotspots was presented. The lithography degradation was captured using a lithography hotspot framework that identifies the different layout pattern configurations occurred in a layout design, simplifies them to ease the pattern analysis and classifies them according to the lithography degradation predicted using lithography simulations. Additionally, a methodology to calibrate the yield model using actual silicon data was proposed in order to obtain a more realistic yield estimation. The main goal of this parametric yield estimation model is to provide a layout quantification metric that enables the possibility to objectively compare the lithography impact on different layout design implementations without an excessive number of lithography simulations and with reduced information from silicon data. In summary, this yield metric serves to capture the relation between layout design and manufacturability.

Thirdly, a configurable Layout Quality Metric (LQM) that considers several layout parameters to obtain a global evaluation of a layout design was proposed. The LQM provides a versatile evaluation methodology which allows the designer to assess the potential capabilities of any layout implementation with a single score. The LQM can be leveraged by assigning different weights to each evaluation aspect or by modifying the parameters under analysis. The LQM is here employed following two different set of partial metrics. The LQM-S uses simple measurements to give a preliminary analysis of a layout design and the LQM-E employs more

elaborated measurements to give a more detailed analysis of the benefits and weaknesses of a design. Note that both sets of measurements include a regularity metric, RM, (a simplified version in the LQM-S and a more precise version in the LQM-E) in order to capture the usage of litho-friendly regular patterns and thus it captures the degree of layout regularity applied in a layout implementation.

Fourthly, Adaptive Lithography Aware Regular Cell Design (ALARC) templates for a real 40nm technology node were proposed to outperform line-pattern resolution compared to traditional 2D standard cell designs. Different ALARC proposals using different degrees of layout regularity and different area overheads were provided. The regular templates were converted into gridded layout design rules suitable for special transistor placement and routing algorithms to automatically generate gridded cell layout libraries. The quality of the gridded regular templates were demonstrated by automatically creating a library containing 266 cells including combinational and sequential cells and synthesizing several ITC'99 benchmark circuits. Note that the regular cell libraries only presented a 9% area penalty compared to the 2D standard cell designs used for comparison and thus providing area competitive designs. The evaluation of the libraries and circuits using the LQM-E proved that regular layouts were competitive compared to 2D standard cell designs depending on the layout implementation since the best regular design, the BHF1 with a regularity index of 97.5%, outperformed other 2D designs, the F2D and the BMF2.

7.2 Publications and Conferences

The list of publications and conference papers related to this dissertation are outlined in this section.

7.2.1 Journal papers

The list of journal papers is detailed next.

1. *Article in Refereed Journal:* Sergio Gomez and Francesc Moll, "Lithography aware regular cell design based on a predictive technology model (extended version)", Journal of Low Power Electronics, 6(4):1– 14, 2010.

2. *Article in Refereed Journal:* S. Gomez, F. Moll, "Yield estimation model for lithography hotspot distortions", Electronic Letters, IET Digital Library, v.49 n. 17, June 2013.

3. *Article in Refereed Journal:* J. Mauricio, F. Moll, and S. Gomez, "Measurements of process variability in 40-nm regular and non-regular layouts", Electron Devices, IEEE Transactions on, vol. 61, no. 2, pp. 365–371, 2014.

4. *Article in Refereed Journal:* J. Cortadella, J. Petit, S. Gomez and F. Moll, "A Boolean Rule-Based Approach for Manufacturability-Aware Cell Routing", Computer-Aided

Design of Integrated Circuits and Systems, IEEE Transactions on, vol.33, no.3, pp. 409-422, March 2014.

5. *Article in Refereed Journal (to be published in autumn 2014):* S. Gomez, F. Moll and J. Mauricio, “Lithography parametric yield estimation model to predict layout pattern distortions with a reduced set of lithography simulations”, Journal of Micro/Nanolithography, MEMS and MOEMS, SPIE, 2014.

7.2.2 Conference papers

The list of conference papers is provided next.

1. *Article in Refereed Workshop:* Sergio Gomez and Francesc Moll, “Lithography aware regular cell design based on a predictive technology model”, VARI 2010 workshop, Montpellier, France, 2010.

2. *Article in Refereed Workshop:* Sergio Gomez, Francesc Moll, Antonio Rubio, Nigel Woolaway, Martin Elhøj, Guilherme Schlinker, “Design Guidelines toward Compact Litho-Friendly Regular cells”, ERDIAP 2011 workshop, Como, Italy.

3. *Article in Refereed Workshop:* S. Gomez, M. Pons, J. Mauricio, F. Moll and A. Rubio, “Channel Length Variations estimation: the need for layout regularity”, in Second European workshops on CMOS Variability, VARI 2011, (Grenoble, France), 2011.

4. *Article in Refereed Workshop:* S. Gomez, F. Moll, L. Garcia-Leyva and A. Rubio, “Design Methodology to compensate Transistor Channel Length litho-induced Variations”, 5th IEEE International Workshop on Design for Manufacturability and Yield”, DFM&Y 2011, (California, United States), 2011.

5. *Article in Refereed Workshop:* S. Gomez, F. Moll, “Methodology to Combat Channel Length litho- induced Variations at Layout Level”, Workshop on Variability modelling and mitigation techniques in current and future technologies, VAMM , Dredsen, Germany, 2012.

6. *Article in Refereed Workshop:* S. Gomez, F. Moll, “Evaluation of Layout Regularity Trade-offs using a Quality Design Metric”, 6th IEEE International Workshop on Design for Manufacturability and Yield”, DFM&Y 2012, (San Francisco, United States), 2012.

7. *Article in Refereed Conference:* S. Gomez, F. Moll, “Evaluation of Layout Design Styles using a Quality Design Metric”, IEEE International System On Chip Conference, Proceedings International SOC Conference, Niagara Falls, NY, USA, September 2012.

8. *Article in Refereed Workshop:* S. Gomez, F. Moll, “Yield Estimation Model using a Lithography Hotspot Classifier”, 7th IEEE International Workshop on Design for Manufacturability and Yield”, DFM&Y 2013, (Austin, United States), 2013.

9. *Article in PhD forum:* S. Gomez, “Regular Cell Design Approach Considering Litho-Induced Process Variations”, PhD Forum at DAC 2014 (Austin, United States), 2013.

10. *Article in Refereed Workshop:* S. Gomez, F. Moll, “Yield Estimation Model using a Lithography Hotspot Classifier”, 4rd European Workshop on CMOS Variability (VARI) 2013, VARI 2013, (Karlsruhe, German), 2013.
11. *Article in Refereed Conference:* S. Gomez, F. Moll, J. Mauricio, “Lithography yield estimation model to predict layout pattern distortions with a reduced set of lithography simulations”, Proceedings SPIE Advanced Lithography 2014 (San José, United States), 2014.

7.3 Future avenues of research

A future avenue of research derived from this dissertation, might be the application of the regular layout design methodologies for advanced technology nodes where lithography variations are expected to be larger. The definition of new layout design guidelines to combat printability variations in future nodes might be an interesting topic for research. Additionally, the regular layout designs proposed in this thesis might be extended to create layouts using either FDSOI or FinFET devices. Another aspect that can be further investigated might include the development of new layout designs with a pattern restriction for specific geometries that would cause excessive lithography degradation, but allowing some 2D shapes in order to reduce area overhead and improve the overall layout quality of a design.

Moreover, the routing algorithm employed in this dissertation enables the possibility to define design rules for multiple patterning techniques. Hence, the definition of design rules for the regular layouts to create multiple patterning friendly libraries ensuring that a synthesized circuit is multiple patterning friendly by construction could be another topic of research.

The parametric yield estimation model framework proposed to compare different layout implementations in terms of lithography variation could be employed to evaluate newer technology nodes. In that sense, more pattern constructs can be perfectly added to the pattern construct library to more precisely assess the overall degradation expected for a layout implementation.

Another aspect of improvement, might be the inclusion of additional measurements to properly evaluate and compare any layout design. For instance, yield due to critical area, stress evaluation or double/multiple patterning capabilities are additional metrics that can be considered to compute the LQM. Lastly, the benefits of using a litho-optimized logic synthesis using the Layout Quality Metric might be also another interesting topic of research.

7.4 Conclusions

This dissertation proposed different layout architectures exploiting the benefits of layout regularity, referred as ALARC designs, and an evaluation framework (LQM) including a lithography yield estimation model to provide a comprehensive analysis of any kind of layout

design template. Despite the printability benefits of applying layout regularity to cell design, other aspects are penalized, such as area penalty and therefore a global evaluation considering several metrics is required to properly assess the benefits of regular designs.

The ALARC cell libraries here proposed only presented a 9% area penalty compared to the 2D standard cell designs used for comparison and thus providing area efficient designs. The analysis of the regular layout design templates demonstrated that the employment of layout regularity might lead to competitive results compared to more traditional 2D standard cell designs, being in several cases better than 2D designs. The evaluation of the libraries and circuits using the Layout Quality Metric showed that regular layouts can outperform 2D standard cell designs using bidirectional metal1 depending on the layout implementation since the best regular design proposed, the BHF1 with a regularity index of 97.5%, outperformed other 2D designs, the F2D and the BMF2. Although the M2D design using regular poly and diffusion and bidirectional metal1 was a bit better compared to the BHF1 design.

For future technology nodes where larger printability variations are expected compared to the 40nm node here employed to illustrate the advantages of layout regularity, regular layouts will become even more competitive compared to 2D standard cell designs. Therefore, layout regularity should become the preferred option for layout designers in the near future to overcome printability variations and continue driving high performance and power efficient devices at lower cost. That means that the contributions of this dissertation will be important for layout design in future technology nodes.

I would like to conclude this dissertation with a few words of Albert Einstein.

Everything should be made as simple as possible,
but not one bit simpler.

These words can be perfectly understood in the sense that layout design should employ simple regular layout patterns in order to keep the technology scaling and combat the lithography-induced variations. Although at the same time, regular layout designs must keep the same complex functionality and characteristics of IC designs created with traditional 2D standard cell designs. Hence, this dissertation has served to prove that regular designs are competitive compared to 2D standard cells and besides regular layouts will be even more competitive in future technology nodes.