ANALYTICAL COMPACT MODELING OF NANOSCALE MULTIPLE-GATE MOSFETS.

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DOCTORAL THESIS

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I STATE that the present study, entitled: "ANALYTICAL COMPACT MODELING OF NANOSCALE MULTIPLE-GATE MOSFETS", presented by Thomas Holtij for the award of the degree of the Doctor, has been carried out under my supervision at the Department of Electronic, Electrical and Automatic Control Engineering of this university, and that it fulfills all the requirements to be eligible for the European Doctorate Award.

Tarragona (Spain), August 19, 2014

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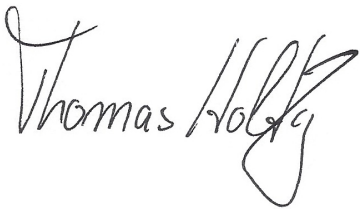

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... and many others...

"Where Do We Come From? What Are We? Where Are We Going?"

Paul Gauguin

List of Publications

Journals

- T. Holtij, M. Graef, A. Kloes, B. Iñíguez, "3-D Compact Model for Nanoscale Junctionless Triple-Gate Nanowire MOSFETs, Including Simple Treatment of Quantization Effects", submitted to: Special Issue of Solid-State Electronics, dedicated to EUROSOI 2014
- T. Holtij, M. Graef, A. Kloes, B. Iñíguez, "Modeling and Performance Study of Nanoscale Double Gate Junctionless and Inversion Mode MOSFETs Including Carrier Quantization Effects", available online and accepted for publication in a future issue of: Elsevier Microelectronics Journal
- T. Holtij, M. Graef, F. Hain, A. Kloes, B. Iñíguez, "Compact Model for Short-Channel Junctionless Accumulation Mode (JAM) Double Gate MOSFETs", IEEE Trans. Electron Devices, Vol. 61, No 2, February 2014, Special Issue on Compact Modeling of Emerging Devices
- T. Holtij, M. Schwarz, A. Kloes, B. Iñíguez, "Threshold Voltage, and 2D Potential Modeling Within Short-Channel Junctionless DG MOSFETs in Subthreshold Region", Solid State Electron, Vol. 90, pp. 107-115, December 2013, Selected Papers from EUROSOI 2012
- T. Holtij, M. Schwarz, A. Kloes, B. Iñíguez, "2D Analytical Calculation of the Parasitic Source/Drain Resistances in DG MOSFETs Using the Conformal Mapping Technique", IETE Journal of Research, Vol. 38, No. 3, 2012

Conferences

- T. Holtij, M. Graef, A. Kloes, B. Iñíguez, "3-D Compact Model for Nanoscale Junctionless Triple-Gate Nanowire MOSFETs", accepted for an oral presentation at ESSDERC/ESS-CIRC 2014, Venice, Italy, 2014
- T. Holtij, M. Graef, F. Hain, A. Kloes, B. Iñíguez, "Modeling of Quantization Effects in Nanoscale DG Junctionless MOSFETs", EuroSOI 2014, Tarragona, Spain, 2014

- T. Holtij, M. Schwarz, M. Graef, F. Hain, A. Kloes, B. Iñíguez, "Unified Charge Model for Short-Channel Junctionless Double Gate MOSFETs", MIXDES 2013, Gdynia, Poland, 2013
- T. Holtij, M. Schwarz, M. Graef, F. Hain, A. Kloes, B. Iñíguez, "Model for investigation of Ion/Ioff ratios in short-channel junctionless double gate MOSFETs", ULIS 2013, Warwick, UK, 2013
- T. Holtij, M. Schwarz, M. Graef, F. Hain, A. Kloes, B. Iñíguez, "2D Current Model for Junctionless DG MOSFETs", EuroSOI 2013, Paris, France, 2013
- T. Holtij, M. Schwarz, A. Kloes, B. Iñíguez, "Analytical 2D Modeling of Junctionless and Junction-Based Short-Channel Multigate MOSFETs", ESSDERC/ESSCIRC 2012, Bordeaux, France, 2012
- T. Holtij, M. Schwarz, A. Kloes, B. Iñíguez, "2D Analytical Potential Modeling of Junctionless DG MOSFETs in Subthreshold Region Including Proposal for Calculating the Threshold Voltage", ULIS 2012, Grenoble, France, 2012
- T. Holtij, M. Schwarz, A. Kloes, B. Iñíguez, "2D Analytical Modeling of the Potential within Juntionless DG MOSFETs in the Subthreshold Regime", EuroSOI 2012, Montpelier, France, 2012
- T. Holtij, M. Schwarz, A. Kloes, B. Iñíguez, "2D Analytical Modeling of the Potential in Doped Multiple-Gate-FETs Including Inversion Charge", ESSDERC/ESSCIRC 2011, Helsinki, Finland, 2011
- T. Holtij, M. Schwarz, A. Kloes, B. Iñíguez, "2D Analytical Calculation of the Source/ Drain Access Resistance in DG MOSFET Structures", ULIS 2011, Cork, Ireland, 2011

Contents

List of Symbols

Symbol	Description	Unit
C_{dep}	Depletion capacitance per unit area	[F/cm^2]
C_{eff}	Effective gate capacitance per unit area	[F/cm^2]
C_{ext}	Extrinsic capacitances	[F]
C_{if}	Inner fringing capacitance per unit width	[F/μm]
C_{ij}	Intrinsic or trans-capacitance (i,$j = G$,S,D)	[F]
C_{of}	Outer fringing capacitance per unit width	[F/μm]
C_{ov}	Gate overlap capacitance per unit width	[F/μm]
C_{ox}	Oxide capacitance per unit area	[F/cm^2]
$\tilde{C}$	Modified effective oxide capacitance per unit area	[F/cm^2]
D_{ox}	Dielectric displacement density	[C/cm^2]
E_c	Energy level for the lower edge of the conduction band	[eV]
E_{crit}	Critical electric field	[V/cm]
E_f	Fermi-energy or Fermi level	[eV]
$E_{f,m}$	Fermi-energy or Fermi level of gate electrode	[eV]
$E_{f,Si}$	Fermi-energy or Fermi level of silicon	[eV]
E_g	Energy gap of semiconductor	[eV]
E_i	Intrinsic energy level	[eV]
E_p	Electric field at pinch-off point	[V/cm]
E_v	Energy level for the lower edge of the valence band	[eV]
$\vec{E}$	Electric field in the space charge region	[V/cm]
E_0	Electric field at silicon-to-oxide interface	[V/cm]
E_1	First discrete sub-band energy level	[eV]
g_d	MOSFET small signal drain conductance	[A/V]
g_m	MOSFET small signal transconductance	[A/V]
h	Planck's constant	[Js]
H_{ch}	Effective channel height	[nm]
I_{ds}	Drain current in a 2-D or 3-D MOSFET structure	[A/μm] or [A]
I_{off}	Off-current (2-D or 3-D structure)	[A/μm] or [A]

I_{on}	On-current (2-D or 3-D structure)	[A/μm] or [A]
k	Boltzmann constant	[J/K]
L_d	Gate overlap region	[nm]
L_g	Effective channel length	[nm]
L_{sd}	Effective source/drain length	[nm]
m_e	Longitudinal effective mass of electrons	[kg]
m_0	Free-electrons mass	[kg]
n_i	Intrinsic carrier concentration	[cm^{-3}]
N_a	Impurity (acceptor) doping concentration in p-type silicon	[cm^{-3}]
N_b	Impurity doping concentration in n- or p-type silicon	[cm^{-3}]
N_d	Impurity (donor) doping concentration in n-type silicon	[cm^{-3}]
N_{sd}	Impurity (donor) doping concentration in source/drain	[cm^{-3}]
q	Magnitude of electronic charge	[C]
Q_d	Mobile charge density at drain end per unit area	[C/cm^2]
Q_f	Fixed charge per unit area	[C/cm^2]
Q_m	Mobile charge per unit area	[C/cm^2]
$Q_{m,acc}$	Mobile charge in accumulation per unit area	[C/cm^2]
$Q_{m,dep}$	Mobile charge in depletion per unit area	[C/cm^2]
$Q_{m,Q}$	Quantum corrected mobile charge per unit area	[C/cm^2]
Q_s	Mobile charge density at source end per unit area	[C/cm^2]
Q_C	Total charge inside channel region	[C]
Q_D	Total charge at drain	[C]
Q_F	Total fixed charge inside channel region	[C]
Q_G	Total charge at gate	[C]
Q_{OX}	Total fixed charge at silicon-to-oxide interface	[C]
Q_S	Total charge at source	[C]
S	Subthreshold slope	[mV/dec]
T	Absolute temperature	[K]
T_{ch}	Effective channel thickness	[nm]
T_{gate}	Effective gate thickness	[nm]
T_{ox}	Effective oxide thickness	[nm]
$\tilde{T}_{ox}$	Scaled effective oxide thickness	[nm]
v_{sat}	Carrier saturation velocity	[cm/sec]
V_{bi}	Built-in potential	[V]
$V_{bi,eff,s/d}$	Effective built-in potential at source/drain	[V]
V_d	Drain potential	[V]
V_{ds}	Drain to source voltage	[V]
V_{dsat}	Drain saturation voltage	[V]

V_{dss}	Saturation voltage	[V]
$\tilde{V}_{dss}$	Modified saturation voltage	[V]
V_{fb}	Flat-band voltage	[V]
V_{fit}	Transition voltage between depletion and accumulation region (Junctionless MOSFET)	[V]
V_g	Gate potential	[V]
V_{gs}	Gate to source voltage	[V]
$\tilde{V}_{gs}$	Gate to source voltage at extracted I_{on}	[V]
V_g^*	Gate voltage in subthreshold region	[V]
V_s	Source potential	[V]
V_{th}	Thermal voltage (kT/q)	[V]
V_{ox}	Voltage drop across the oxide	[V]
V_{DD}	Power supply voltage (Voltage drain drain)	[V]
V_T	Threshold voltage	[V]
$V_{T,Q}$	Quantum corrected threshold voltage	[V]
W_{ch}	Effective channel width	[μm]
x_m	Position of potential barrier within the channel region	[nm]
α	Subthreshold slope degradation factor	[-]
$\tilde{\alpha}$	Modified subthreshold slope degradation factor	[-]
Δy	Geometry parameter for the conformal mapping technique	[nm]
ΔE_Q	Difference between conduction band and first discrete sub-band energy level inside channel region at the potential barrier	[eV]
ΔV_T	Threshold voltage roll-off	[V]
ε	Material dependent permittivity	[F/cm]
ε_{ox}	Dielectric permittivity of oxide	[F/cm]
ε_{Si}	Dielectric permittivity of silicon	[F/cm]
ε_0	Permittivity of vacuum	[F/cm]
θ	Mobility degradation factor	[1/V]
λ	1-D natural length	[nm]
μ	Effective channel mobility	[cm^2/Vs]
μ_0	Low-field channel mobility	[cm^2/Vs]
$\mu_\perp$	Mobility below threshold	[cm^2/Vs]
Ξ	Electric flux	[C]
ρ	Space charge density	[C/cm^{-3}]
ϕ	Electrostatic potential	[V]
ϕ_c	Electrostatic potential at channel center (center potential)	[V]
ϕ_{fn}	Electron quasi-Fermi level	[V]
ϕ_n	Difference between Fermi level and conduction band inside channel region at potential barrier	[V]

ϕ_p	Electrostatic potential of particular solution	[V]
ϕ_s	Electrostatic potential at silicon-to-oxide interface (surface potential)	[V]
ϕ_T	Difference between Fermi level in source region and intrinsic level inside channel region at potential barrier	[V]
φ	Electrostatic potential of Laplace solution	[V]

Acronyms

Symbol	Description
ADG	Asymmetric double-gate
CLM	Channel length modulation
CMOS	Complementary metal oxide semiconductor
CMP	Chemical mechanical polishing
CPU	Central processing unit
DG	Double-gate
DGM	Density gradient model
DIBL	Drain-induced barrier lowering
EDA	Electronic design automation
EI	Electrostatic integrity
EOT	Equivalent oxide thickness
FEM	Finite-element-method
FET	Field-effect transistor
GAA	Gate-all-around
GCA	Gradual-channel approximation
GIDL	Gate-induced drain leakage
IC	Integrated circuit
ITRS	International technology roadmap for semiconductors
HDL	Hardware description language
IFM	Impedance-field method
IM	Inversion mode
JAM	Junctionless accumulation mode
JL	Junctionless
JLT	Junctionless transistor
JNT	Junctionless nanowire transistor
LDD	Lightly-doped drain
LSPE	Lateral solid-phase epitaxy
LTO	Low temperature oxide

MOSFET	Metal-oxide-semiconductor field-effect transistor
NQS	Non-quasi-static
NR	Newton-Raphson
NW	Nanowire
PDE	Partial differential equation
PP	Perturbation potential
QE	Quantization effect
QG	Quadruple-gate
QHO	Quantum harmonic oscillator
QME	Quantum mechanical effect
QS	Quasi-static
QW	Quantum well
UTB	Ultra-thin body
RF	Radio frequency
RDF	Random dopant fluctuation
RSD	Raised source/drain
SB	Schottky barrier
SCE	Short-channel effect
SEG	Selective epitaxial growth
SDG	Symmetric double-gate
SOI	Silicon on insulator
TCAD	Technology computer aided design
TG	Triple-gate
VLSI	Very-large-scale integration

CHAPTER 1

Introduction

The continuous development of very-large-scale integrated (VLSI) devices has a significant impact on the semiconductor technology. In that field, the metal-oxide-semiconductor field-effect transistor (MOSFET) is the most promising device, due to its good scalability, high performance and low power consumption in standby mode. To improve the performance of the MOSFET, its channel length has been reduced from μm to the sub 20 nm region during the past 30 years. Modern central processing units (CPUs) can therefore contain more than two billion (US) transistors [1]. For that reason, circuit design without the help of device simulators, which for example use the finite element method (FEM) and circuit simulators like SPICE [2] or ELDO [3] has become impossible nowadays.

This chapter introduces the reader to the history of the semiconductor technology, its continuous development process, current MOSFET technologies, circuit design and the special demands on the device modeling. In the last section of this chapter the thesis' challenges and its outline are discussed.

1.1 History of Semiconductor Technology

Over the past nine decades the semiconductor technology was boosted by inventions like a patent called: "Method and Apparatus for Controlling Electric Currents", from Julius Edgar Lilienfeld in 1926 [4]. He proposed a three-electrode structure using copper-sulfide semiconductor material, but at this time was unable to fabricate working devices. Today his idea is formally known as the field-effect transistor.

Later, derived from Ohl's serendipitous discovery of the pn-junction in 1940 [5, 6], William Shockley presented a pn-junction based transistor in 1948 [7, 8]. This device became the most common form of rectifier used in the electronics industry and has since grown to a key element in the design of semiconductor devices. The first bipolar junction-based transistor was then successfully manufactured in 1951 at Bell Laboratories [9].

In 1958, Jack Kilby of Texas Instruments demonstrated the first integrated circuit (IC) and

an amplifier [10]. Two years after John Atalla and Dawon Kahng fabricated working metal-oxide semiconductor field-effect transistors and demonstrated the first successful MOS field-effect amplifier [11], which today is one of the most common devices used in electrical circuits. In the same year Texas Instruments introduced its first commercial device, the Type 502 Binary Flip-Flop and in 1961, the Series 51 DCTL "fully-integrated circuit" family [12].

The complementary MOS circuit was invented by C. T. Sah and Frank Wanlass, who were with the Fairchild R & D laboratory in 1963 [13, 14]. They showed that logic circuits, combined of p- and n-channel MOS transistors in symmetric, complementary circuits, do not suffer from power losses in standby mode. Today this ground-breaking concept is called CMOS technology.

A very important step in the development of integrated circuits was done by Gordon Moore in 1965. He claimed that the number of components per chip would double every 12 months [15]. This idea was edited for publication with title: "Cramming more components onto integrated circuits" [16]. Later in 1975 he corrected his claim by saying the number of components will double every 24 months [17]. This prediction is commonly known as Moore's law nowadays and is still used as a guideline in the semiconductor industry.

The first integrated microprocessors were fabricated in 1971. One of them was Intel's 4004, developed by Ted Hoff and Stanley Mazor [18–20]. The device contained 2300 transistors in a 16-pin package and can be recognized as the first commercial microprocessor available. Compared to these days' state-of-the-art technology, where Intel launches microprocessors containing more than two billion (US) transistors on a single chip [1], the ongoing development process in that area becomes clearly visible.

1.2 Current MOSFET Technologies

One of the most important challenges in recent semiconductor research is to increase the number of devices on a single chip, the storage density of memories and to raise the speed (clock frequency). At the same time the power consumption must be reduced to prevent operational failures, due to self-heating problems. To stand the pace with these requirements, which are stated by the International Technology Roadmap for Semiconductors (ITRS) [21], the dimensions of the MOSFET are continuously shrunk (device scaling) even below 20 nm channel length [1].

At this point, the close proximity between the source and the drain regions of such devices reduces the ability of the gate electrode to sufficiently control the potential distribution and the flow of current in the device's channel region. For that reason, undesired short-channel effects (SCEs) start to bother the device's electrostatic characteristics immensely [22]. Like for example, the threshold voltage roll-off due to the charge sharing effect, the subthreshold slope degradation caused by the punch-through effect or the drain-induced barrier lowering (DIBL) caused by the close proximity of the source and drain, resulting in a decreased barrier formation for electron injection from source into the channel region [23]. In order to cope with

these problems multiple-gate structures, such as the double-gate (DG), the triple-gate (TG) and the quadruple-gate (QG) MOSFET [24, 25], which are illustrated in Fig. 1.1, were analyzed, modeled and fabricated [26–30]. These new devices are reported to have vastly improved electrostatic characteristics (less SCEs) compared to their single-gate counterparts, since the increased electric field of the multiple-gates and therefore, the control of the channel by the gates is stronger than in bulk MOSFETs [26]. This fact makes the multiple-gate MOSFET

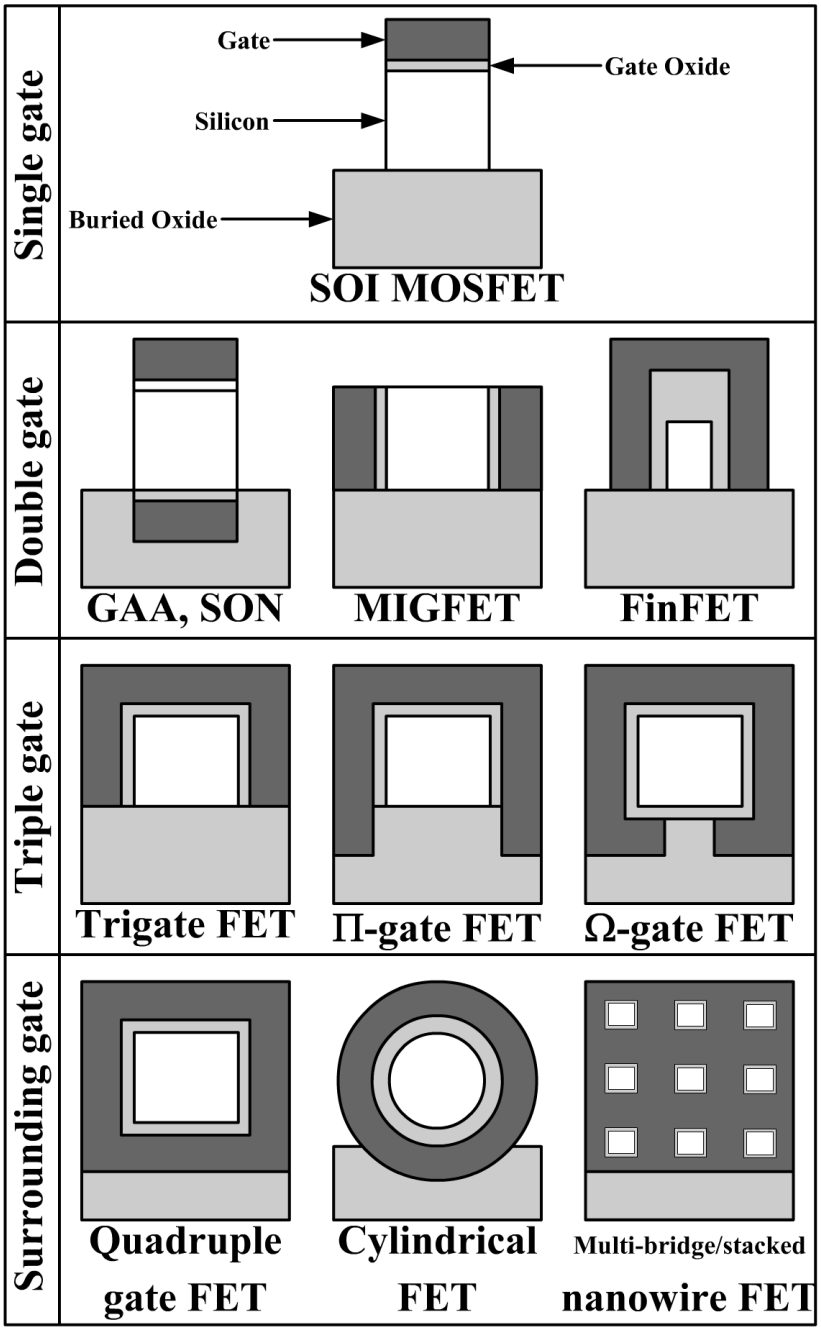


Figure 1.1: Possible device and gate structures [26].

an attractive candidate to improve the performance of future CMOS technology. Additionally to SCEs, quantization effects (QEs) must be taken into account in such scaled devices if their channel thickness ranges in the same order of magnitude as the de Broglie wavelength of the charge carriers [31], which complicates the understanding and manufacturing of such devices even more.

Another big challenge remaining is the fabrication of such devices at the nanometer scale. Novel doping and ultra-fast annealing techniques are required to form the ultra-shallow and abrupt pn-junctions in order to avoid a possible fluctuation of dopants from the source/drain into the channel region [32]. This fact gives rise to the development of new, more simple, device structures like the junctionless transistor [33].

The reader can find detailed information about the state-of-the-art technologies and models of the different devices in sections 2.2 and 2.4.

1.3 Circuit Design and Device Modeling

A major challenge of nowadays circuits, which contain millions or even billions of connected transistors, is the designing and manufacturing time and also the production costs. To reduce both time and costs several software tools for high-level digital design, mask level synthesis, simulation and modeling of discrete devices are available (electronic design automation (EDA) tools). These tools enable the chip designer to analyze entire semiconductor chips. To ensure proper function, the device or the circuit is running through a bunch of simulation cycles until all malfunctions are eliminated. The advantage of such an EDA tool is that any possible environment can be simulated, like: altering temperature, illumination, variations in the power supply, the influence of statistical variations due to line-edge roughness or random dopant fluctuation effects [34].

1.3.1 Device and Circuit Simulations

Some of the most important discrete device simulators are ATLAS [35], TCAD Sentaurus [34] and Minimos-NT [36]. They provide the user with the ability to simulate a broad range of fully featured 2-D and 3-D devices. These simulators incorporate advanced physical models and robust numeric methods for the simulation of most common types of semiconductor device. Based on a 2-D or 3-D surface or volume grid, respectively, each point on the grid is solved with the help of a partial differential equation (PDE) solver, using certain iteration steps. If a 3-D structure is considered, this method can take several hours or even days depending on the applied settings for the desired accuracy for the results. For that reason, this iterative method is not suitable for circuit simulations, wherefore compact models are commonly used to approximate the device's electrical and thermal behavior as accurate as possible.

Nowadays, the most famous circuit simulators are SPICE [2] and ELDO [3]. For both exist a

wide range of different models, which take into account different physical effects. These models can be divided into three groups [37]:

- **Threshold voltage V_T based models** assume that the surface potential is a simple function of input voltage V_{gs}: constant if $V_{gs} > V_T$ and linear if $V_{gs} < V_T$. This results in separate solutions for the different operating regimes and therefore, requires smoothing functions in order to connect the regions. Such models were successfully used in BSIM3 [38], BSIM4 [39] and MOS Model 9 [40].
- **Surface-potential-based models** solve for the input equation the surface potential at the two ends of the device's channel. The terminal charges, the current and its derivatives are then calculated from the solution of the surface potential. Examples are the SP model [41], MOS Model 11 [42], HiSIM [43–46] and PSP [47, 48].
- **Charge-based models** find the density of the inversion charge at the two ends of the device's channel and express the model outputs in terms of these charge densities. The conductance and the capacitances are directly derived from the calculated charge densities. Examples for such models are the EKV [49], ACM [50] and BSIM5 [51] and BSIM6 [52] model.

1.3.2 Properties of Models for Circuit Simulators

Generally, compact models for circuit simulations should describe the electrical behavior of the transistor in all operating regimes as good as possible. The compact models can be separated into three categories [22, 53, 54]:

- **Physical-based models** only use physics-based equations to describe the behavior of the transistor. Such models have the advantage that even downscaled devices can be described. In literature, physics-based models without empirical parameters are often introduced to describe the behavior of long-channel devices or single electrical device characteristics, like threshold voltage and subthreshold slope.
- **Numerical-fit models** use mathematical expressions without any relation to the physics of the device. By introducing many fitting parameters, the expression is fit to the result from the simulation. On the one hand, this process is technology independent, but on the other hand this approach gives no physical insight into the behavior of the device. Additionally, the model validity outside the data range is uncertain.
- **Empirical-based models** represent a combination of the physical-based and numerical-fit models. In addition to the physical equations, numerical fitting parameters are added. This reduces the complexity of the model in order to enhance its performance. However, the disadvantage, due to the fitting parameters, is the reduced ability to predict the transistors behavior when the device physics are changed.

It should be clarified that a compact model, to be used in a circuit simulator, should always meet the following requirements [22, 55]:

- High accuracy in order to properly predict the electrical behavior of the transistor over all regions of device operation.
- Not only being accurate, but simple as well (trade-off between accuracy and simplicity).
- To avoid convergence problems, the drain current expressions must prove continuity in its derivative of first-order (for analog applications up to third-order).
- A single model should fit all device sizes used in state-of-the-art design practice.

1.4 Challenges and Outline of Thesis

In this thesis the main focus is on the development of an analytical, physics-based and predictive compact model for nanoscale multiple-gate MOSFETs, which should be derived in closed-form to be suitable for circuit simulators. The investigated devices are the standard inversion mode (IM) MOSFET and a new device concept called junctionless (JL) MOSFET. The main scientific objectives are:

- Development of a complete DC model for nanoscale multiple-gate MOSFETs (1-D, 2-D and 3-D MOSFET structures). The model must be derived in closed-form in order to be suitable for circuit simulators. If possible, fitting parameters should be avoided.
- Based on the solutions obtained from the DC model, a charge-based AC model should be derived by using the Ward-Dutton partition method [56].
- Since downscaling does not only affect the device's channel length, quantization effects must be taken into account when the channel thickness is scaled below 10 nm [31].
- Verification of the developed model versus TCAD simulation data. Additionally, the 3-D model is to be compared versus measurement data of nanoscale triple-gate nanowire (TG-NW) MOSFETs.

Briefly, the physics-based model for the potential is derived with the help of Poisson's equation and the conformal mapping technique by Schwarz-Christoffel [57]. From this closed-form solution, simple equations for the calculation of the threshold voltage V_T and the subthreshold slope S are derived. By using Lambert's W-function and a smoothing function to model the transition between the device's different operating regimes, a unified charge density model valid in all regions of device operation is developed. A modified drain current expression is presented and a dynamic model is derived based on the calculated charge densities inside the device. The dependencies between the physical device parameters and their impact on the

device performance are worked out. Important device characteristics such as threshold voltage V_T, drain-induced barrier lowering (DIBL), subthreshold slope S and the I_{on}/I_{off} ratios are addressed and discussed. Additionally, symmetry around $V_{ds} = 0\,\mathrm{V}$ and continuity of the drain current I_{ds} at derivatives of higher-order (up to third-order) are in focus of this work.

To stand the pace with recent ITRS [21] requirements for future CMOS technology, we, among other things, will target extremely scaled devices with a minimum channel length of 16 nm and thicknesses down to 3 nm. At this point quantization effects (QEs) play an important role, whereby in the case of a junctionless device, the modeling of QEs differs from their common treatment in inversion mode devices and therefore, requires some special attention. A performance comparison between the inversion mode and the junctionless MOSFET is performed. Finally, an extension for 3-D triple-gate nanowire devices is presented and discussed. Throughout the thesis, intermediate results such as electrostatics and drain current are verified versus TCAD simulations and measurement data.

In chapter 2 the basics of the inversion mode and the junctionless MOSFET are detailed, as well as their operation principles. A complete overview of the state-of-the-art technologies and models is presented to the reader.

Poisson's equation and the complex potential theory are discussed in chapter 3. The conformal mapping technique by Schwarz-Christoffel [57] and the required potential transformation are addressed. The decomposition strategy of Poisson's equation and the solution of Poisson's integral in the upper half of the w-plane are discussed.

In chapter 4 the development of the 2-D compact DC model for the inversion mode and junctionless MOSFET is presented. This means the voltages applied at the terminals of the device remain constant and do not vary with time. The chapter contains explanations about the introduced model simplifications and the usage of the conformal mapping technique. A detailed description of how the 2-D potential is derived in closed-form is presented. The electrical model parameters, the unified charge density model and the new drain current expression are presented followed by extensively verifications versus TCAD simulation data.

In chapter 5 a dynamic model (AC model), which is applicable when the device terminal voltages are varying with time, is developed. Based on the DC model, the quasi-static assumption and by using the Ward-Dutton linear charge partition scheme, the total charges at gate, source and drain are derived. The intrinsic capacitances are then readily obtained from these total charges. The extrinsic capacitances are modeled separately, whereby the bias dependence of the gate overlap and the inner fringing capacitance is inherently included. The AC model is finalized by adding an expression for the outer fringing capacitance. The model is compared against TCAD simulation data.

Carrier quantization effects in both inversion mode and junctionless MOSFETs are modeled and investigated in chapter 6. The performance of both device types is compared and summarized.

Chapter 7 comprises the development of an extension to account for 3-D effects in triple-gate MOSFET structures. The enhanced model is explained step by step and verified versus 3-D TCAD data and additionally, versus measurement data of nanoscale junctionless triple-gate nanowire MOSFETs. Finally, an overall conclusion is drawn in chapter 8.

CHAPTER 2

MOSFET Basics

This chapter comprises a detailed description of the MOSFET's operation principle, state-of-the-art technologies and modeling approaches. The main focus is on the standard inversion mode (IM) and the junctionless (JL) MOSFET in double-gate configuration (2-D structures), whereby an extension for triple-gate devices (3-D structures) is presented and discussed in chapter 7. Figure 2.1 schematically depicts these 2-D and 3-D device structures.

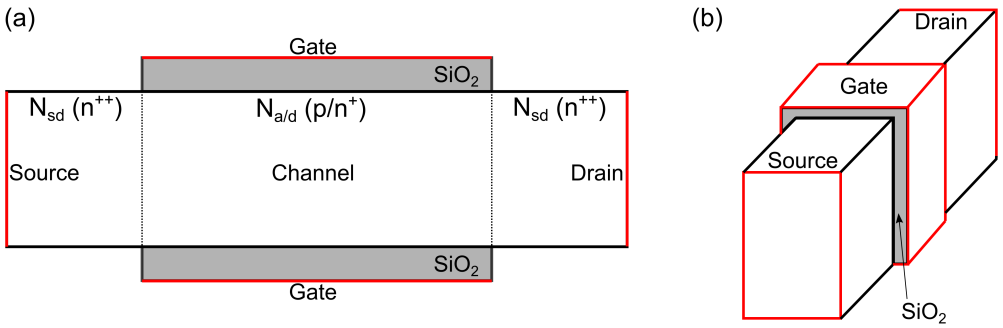


Figure 2.1: (a) Longitudinal cross-section of the IM DG and JL DG MOSFET showing its physical device dimensions and doping profiles. $N_{a/d}$ is the channel doping concentration of the IM and JL device, respectively. N_{sd} is the source/drain doping concentration. (b) Illustration of the triple-gate structure. The gate surrounds the device's channel region from three sides. The red lines represent the source, drain and gate electrodes, respectively.

2.1 Operation Principle of Inversion Mode MOSFETs

The conventional MOSFET can be considered as an active device commonly used to construct integrated circuits. The device consists of different materials such as poly-Si, or aluminum for the gate, SiO_2 as insulator (or high-k materials) and two n- and one p-doped regions (n-MOSFET) forming the so called pn-junctions. Generally, the inversion mode MOSFET has three operating states [22]. For a better understanding, the corresponding band diagrams are

detailed in Fig. 2.2.

- *Accumulation mode*: if a negative or a very low gate-source voltage V_{gs} is applied (Fig. 2.2(a)). Negative charge is on the gate and positive charged holes are accumulated beneath the gate. Under this condition no flow of current can be observed. At a certain V_{gs} the band structure is flat. This voltage is referred to as the flat-band voltage V_{fb}.

- *Depletion mode*: if $V_{gs} < V_T$ and $V_{ds} \neq 0$ is valid, where V_T is the threshold and V_{ds} the drain-source voltage, a negative charge is build up at the silicon surface. This charge is called depletion charge. Under this condition the only flow of current is a leakage current (Fig. 2.2(b)).

- *Inversion mode*: if $V_{gs} > V_T$ and $V_{ds} \neq 0$ holds, a conducting channel with a negative mobile charge is formed beneath the gate. This channel is often referred to as the inversion channel. With increasing V_{ds}, a current I_{ds} will flow from the source to the drain region, due to the carriers nature of diffusion. If $V_{gs} > V_T$ and $V_{ds} > V_{d_{sat}}$, where V_{dsat} is the saturation voltage ($= V_{gs} - V_T$), the device operates in strong inversion (Fig. 2.2(c)).

The assumption that the variation of the electric field in the x-direction (along the channel) is much less than the corresponding variation of the electric field in the y-direction (perpendicular to the channel) is called the gradual-channel approximation (GCA) [22]. If the GCA is valid along the whole length of the channel, then the drain current I_{ds} can be expressed as [58]:

$$I_{ds} = \mu \frac{W_{ch}}{L_g} \int_{V_s}^{V_d} Q_m \, dV, \tag{2.1}$$

where W_{ch} is the device's width and Q_m the mobile charge density (per unit area). Thus, to calculate the drain current one needs to calculate Q_m first. This calculation is content of section 4.5.

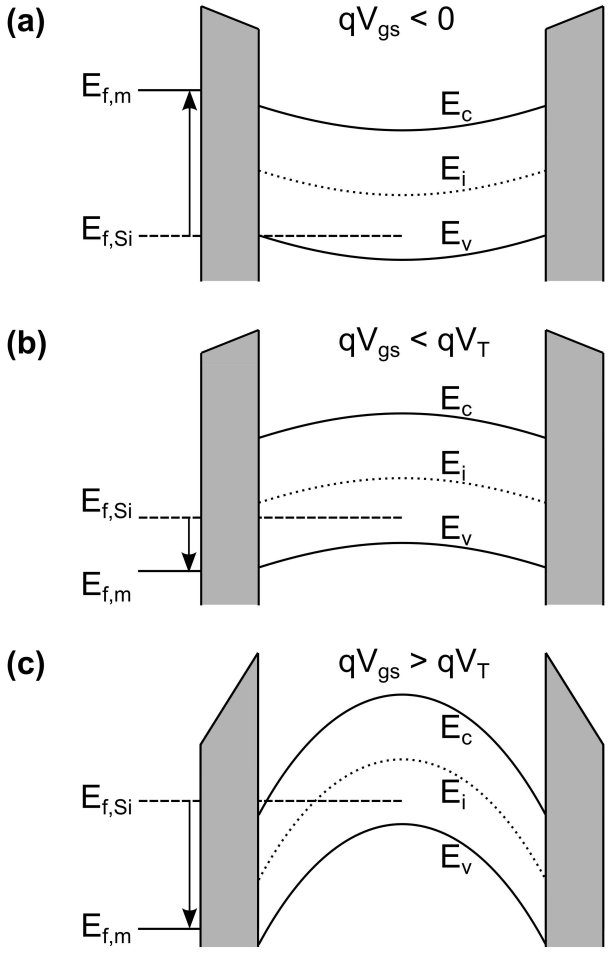


Figure 2.2: Band diagram from gate to gate of the inversion mode DG MOSFET shown in Fig. 2.1, with N_a as the channel doping concentration. E_c is the conduction and E_v the valence band. $E_{f,Si}$, $E_{f,m}$ and E_i are the Fermi level of silicon, Fermi level of gate and intrinsic level, respectively. The device operates in: (a) accumulation, (b) depletion and (c) strong inversion region.

2.2 State-of-the-Art - Inversion Mode MOSFETs

Models for Undoped Devices

Mostly, the models presented in literature ignore the effects which occur in relation with high channel doping concentrations. Instead, they refer to undoped or lightly doped devices for the following reasons [59], [60]:

- Undoped devices can avoid the dopant fluctuation effect, which contributes to the variation

of the threshold voltage and the drive current.

- Undoped devices can enhance the carrier mobility owing to the absence of depletion charges (which significantly contributes to the effective electric field, thus degrading the mobility and the drain current).

In [61] a one-dimensional analytic model for undoped symmetric and asymmetric DG MOSFETs is derived by incorporating only the mobile charge term in Poisson's equation. In addition, a capacitance model was derived. An advanced continuous, analytical model for the drain current was proposed by the same group [62]. It is derived from closed-form solutions of Poisson's equation and the current continuity equation without the charge-sheet approximation, whereby the drain current is derived by using Pao-Sah's integral. A long-channel model for the same device, which also accounts for volume inversion in the subthreshold region is detailed in [63]. The resulting analytical expressions of the drain current, terminal charges, and capacitances are continuous in all operation regions.

A design oriented charge-based model for undoped symmetrical DG MOSFETs was presented in [58]. They emphasize a link between their approach and the EKV formalism derived for bulk MOSFETs, which leads to a unique g_m/I_d design methodology for DG architectures.

An analytical, explicit and continuous-charge model for undoped symmetrical DG MOSFETs was presented in [64]. Based on an unified-charge control model derived from Poisson's equation it is valid from below to well above threshold voltage. The transition between the different regimes is smoothed. The drain current, charges and capacitances are written as continuous explicit functions of the applied bias. Different device setups were tested.

In [65] a compact quantum model for both the electrostatic potential and electric charge in thin-film symmetric DG MOSFETs with undoped body was presented. As a novelty, both the resulting potential and charge have explicit expressions on bias and geometrical parameters. A comparison of the model has been performed versus self-consistent numerical solutions of Schroedinger-Poisson equations.

In [66] the electrical properties of the DG MOSFET were investigated. A compact model which accounts for charge quantization within the channel, Fermi statistics, and non-static effects in the transport model was worked out.

In [67] quantum effects have been incorporated in an analytic potential model for DG MOSFETs. From extensive solutions to the coupled Schroedinger and Poisson equations, threshold voltage shift and inversion layer capacitance were extracted as closed-form functions of silicon thickness and inversion charge density.

The comparison of all these models versus numerical simulation data - obtained from TCAD Sentaurus (Synopsys) [34], or ATLAS (Silvaco) [35] - showed a good match. However, the discussed models are mostly valid for long-channel considerations and can therefore not be used to predict the electrostatics of nowadays device structures. In addition, due to technological constraints in real devices, one always faces the problem of having dopants inside the channel

region, which influence the device's electrostatic behavior. Dopants can cause a threshold voltage shift, worsen the subthreshold slope and reduce the carrier mobility [68]. Hence, an urgent task is the development of compact models, which are able to predict the electrostatic behavior of such, especially, short-channel devices.

Models for Doped Devices

High channel doping concentrations are generally used to reduce the depletion width and therefore, to reduce short-channel effects in MOSFETs. Also the threshold voltage is adjusted by using additional implants in the device's channel region. However, doping the MOSFET's channel region produces several side effects regarding its performance. These effects are all the more different when considering long- or short-channels. Therefore, the most important effects will be pointed out, considering an n-MOSFET.

- *Long-channel devices*: the major effect is the increase of the threshold voltage as the doping level increases. At low doping levels, the threshold voltage shift (ΔV_T) is linear dependent on the doping level. At high doping concentrations the device becomes partly depleted. Under this condition ΔV_T is no longer a linear function of the doping level. Also, the subthreshold slope is affected by the doping. First, in subthreshold region it remains unchanged, but starts to deteriorate (degrades) when the doping reaches a certain level [68].

- *Short-channel devices*: high doping can impact the threshold voltage, the subthreshold slope and the DIBL. When the doping is high, the carrier mobility is strongly degraded by the additional dopants inside the channel region. Another effect is the increase of the normal electric field component caused by depletion charges, thus decreasing the carrier mobility [68]. Also, high doping concentrations cause band-to-band tunneling from the body to the drain, which can be a significant source of leakage current [69]. In addition, body doping gives rise to a discrete dopant fluctuation effect, which might contribute to another threshold voltage variation [70].

For these reasons different models, which include the effect of high channel doping concentrations, are discussed. A model for the calculation of the electrostatic potential was presented in [71]. The semiconductor body was described by a complete 1-D Poisson equation with the contributions of electrons, holes, acceptor and donator charge. After some calculations, a relation between the surface and center potential was obtained. The potentials were calculated using the Newton-Raphson (NR) method for a given electron quasi-Fermi potential, whereby the continuous bulk surface potential solution was used as the initial guess. A loop continued until convergence.

Analytical expressions to model the surface and center potential as a function of silicon layer impurity concentration, gate dielectric thickness, silicon layer thickness and applied voltages

in DG MOSFETs were discussed [72]. The doped silicon layer's doping concentration ranged between $1 \cdot 10^{14}$ and $3 \cdot 10^{18}\,\mathrm{cm}^{-3}$. The threshold voltage was calculated using the derived expressions for the potential.

A continuous compact model for the drain current, including short-channel effects and carrier quantization in DG MOSFETs was developed in [73]. The model was adapted to ultra-scaled devices, with short channel lengths and ultra-thin silicon films. The drain current model was supplemented by a node charge model and the resulting DG model was successfully implemented in Eldo IC analog simulator.

In [23] several approximations were used to derive analytical solutions of Poisson's equation for doped and undoped devices. The need for self-consistency with Schroedinger's equation and with the current continuity equation resulting from the transport models was addressed. Techniques to extend the compact modeling to the high-frequency regime to study the RF performance, including noise, was presented.

An analytical, continuous model for highly-doped DG SOI MOSFETs, targeting the electrical simulation of baseband analog circuits, was presented in [74]. A unified charge control model was derived for the first time for doped DG transistors. It's validity was confirmed from below to well above threshold voltage, whereby small-signal parameters were also obtained from the model.

Another approach to calculate the channel potential of doped DG MOSFETs was shown in [75]. It is called the equivalent-thickness concept. Considering a long-channel device, the doping in the channel was converted to an equivalent silicon thickness. From the expressions for the potential a complete model for the drain current was obtained. The disadvantage of this model is that, it is only valid until the semiconductor becomes almost undepleted and it is not valid when operating near flat-band voltage, because then impurities are no longer fully ionized.

A 2-D surface potential-based model for fully-depleted symmetrical DG strained-Si MOSFETs was proposed in [76]. The parabolic potential approximation was utilized to solve 2-D Poisson's equation in the channel region. The model incorporates the effect of both positive as well as negative interface charges.

All presented models were validated using rigorous numerical or experimental measurements for different device setups, several DG structure dimensions and applied voltages. The models were shown to be in good agreement compared to the reference data. However, some of the presented models only show solutions for the potential in these devices and no analytical expressions for the drain current. Others are valid from below to above threshold voltage, but concentrate on 1-D solutions. Only in [23] a review on an IM DG MOSFET model, which is also valid for short-channel devices, is presented. Nevertheless, in this review and the original work from [77], no higher derivatives of the current (up to third-order) are shown and no symmetry-test [78] is performed. Both are important criteria for a compact model and must be fulfilled to ensure proper functionality when the model is being implemented into a circuit simulator.

Technologies

In this part, current device technologies for the inversion mode DG MOSFET are presented. In general, this device can be fabricated using a planar or non-planar technology [60], whereby the fabrication process is not straight forward.

- *Planar structures*: advantage of better channel thickness uniformity, because the film thickness on the plane of the wafer has the best uniformity and controllability. Anyway, planar structures suffer from a difficult fabrication of a back-gate with thin gate dielectric. In addition, the access of the bottom gate from the top surface, for device wiring, complicates the fabrication and could have negative impact on the device density.

- *Non-planar structures*: easier access and formation of both gates on crystalline channels with thin gate dielectrics. Uniformity of the channel might be worse than in planar devices, since the channel thickness is defined by lithography and patterning techniques (e.g. reactive ion etching).

A manufacturing process of a planar IM DG structure was processed in [79], which is now shortly reviewed step by step. Figure 2.3(a) illustrates the etching of the 190 nm SOI layer and part of the BOX to form the 300 nm deep trench; (b) depositing a 20 nm Si_3N_4 and 400 nm low temperature oxide (LTO) and planarizing the surface, using chemical mechanical polishing (CMP); (c) removing Si_3N_4 on the surface in hot H_3PO_1, depositing a layer of 150 nm amorphous silicon, implanting high dose Si and Ge ions and furnace annealing at 600° C for 8 hours; (d) depicts thinning down the crystallized film to 100 nm, defining the crystallized layer and removing the dummy oxide and Si_3N_4 under the channel region; (e) growing 110 Å gate oxide, depositing 250 nm in-situ phosphorus-doped poly-silicon gate and defining the gate; (f) depositing 500 nm LTO, opening contact, metal sputtering and patterning. The fabricated n-MOS transistors provided good device characteristics including high drive currents, steep subthreshold slopes and high I_{on}/I_{off} ratios. The devices also had better threshold voltage roll-off characteristics and DIBL effects compared to their conventional single-gate counterparts. It can be stated that, the lateral solid-phase epitaxy (LSPE) process is very simple and compatible with bulk CMOS technology and it can be used directly in mixed bulk/SOI circuits as well as 3-D stacked circuits, which might be of great importance in view of the future semiconductor technology.

A manufacturing process for a non-planar IM DG MOSFET was presented by Jakub Kedzierski *et. al.* [80], which is now reviewed. They fabricated DG FinFETs with symmetric (SDG) and asymmetric (ADG) poly-silicon gates. The symmetric gate devices showed drain currents competitive with conventional, bulk silicon technologies. The asymmetric gate devices obtained $|V_T| \sim 0.1\,\mathrm{V}$, with off-currents less than $100\,\mathrm{nA}/\mu\mathrm{m}$ at $V_{gs} = 0\,\mathrm{V}$. The SDG started on SOI wafers with a 65 nm thick Si-layer topped by a 50 nm oxide hard mask. The fin layer was defined using optical lithography and a hard mask trimming technique. The gate stack

consisted of a 1.6 nm thermal gate oxynitride, an undoped poly-silicon gate and an oxide hard mask. Extension regions were implanted at a high tilt angle of 45°, with 4 different wafer twists. Following spacer formations, the source/drain regions of some of the SDG devices were expanded using a selective epitaxy growth (SEG) raised source/drain (RSD) process. The fabricated devices demonstrated drive currents rivaling conventional bulk and SOI, as well as that of current double-gate devices.

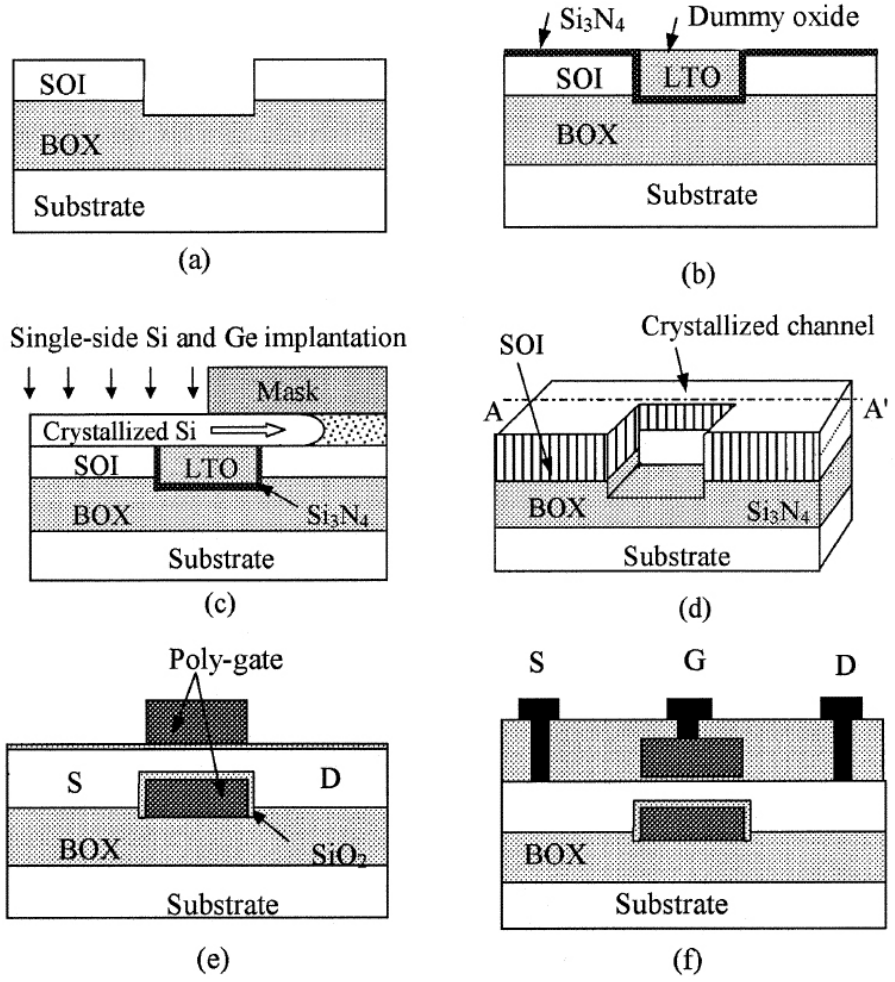


Figure 2.3: Major fabrication steps for the planar IM DG MOSFET using the LSPE process [79].

2.3 Operation Principle of Junctionless MOSFETs

Junctionless transistors (JLTs), also called gated resistor or vertical-slit FET, are new candidates to handle upcoming manufacturing problems related to abrupt pn-junctions in state-of-the-art CMOS technology. Many research groups are focusing on this not long ago presented device concept as it might become a breakthrough to the frontiers of nanoscale MOSFETs.

The first work on JLTs was done by J.-P. Colinge *et. al.* [33]. They presented a simulation study showing a device, which indicated the advantages of leaving pn-junctions in future CMOS technology behind. More work on this new concept was done by [32, 81, 82], including a detailed description of the JLTs operation principle. In general, this device is heavily doped (the type of doping in the channel region is the same as in the source/drain regions), has no junctions, no doping concentration gradients and provides full CMOS process compatibility. The JLT is turned on when operating at flat-band condition and turned off by complete depletion of its channel region, which is caused by the workfunction difference between the gate material and the doped channel region of the JLT. Therefore, the cross-section of the device must be small enough in order to deplete its channel region. It was shown that improved electrostatic characteristics such as reduced SCEs, an excellent subthreshold slope, low leakage currents, high I_{on}/I_{off} ratios, a low DIBL and less variability are key benefits of JLTs [32, 33, 81–85].

In contrast to conventional inversion mode MOSFETs, where a current flow in a conducting channel at the silicon-to-oxide interface (surface conduction) prevails, in JLTs the bulk current (volume conduction) is a conduction mechanism that cannot be neglected - indeed it is dominant in the subthreshold and near threshold regime. Worries about degraded mobilities, due to the high doping concentration in JLTs were shown to be less significant, since the almost zero electric field in the center of their channel is beneficial to the carrier mobility. Additionally, straining techniques could be applied to enhance the carrier mobility further [32].

Similar to the inversion mode MOSFET the junctionless transistor has different operating regimes, which are depicted in Fig. 2.4 and Fig. 2.5 for an n-channel device.

- *Depletion mode*: if $V_{gs} < V_T$ the channel is fully depleted and the device is turned off (off-state, Fig. 2.4(a)).
- *Bulk current mode*: if $V_T < V_{gs} < V_{fb}$ the channel is partly depleted and a small bulk current starts to flow in the middle of the channel (from source to drain, Fig. 2.4(b)).
- *Flat-band mode*: if $V_{gs} = V_{fb}$ the device operates in flat-band mode (Fig. 2.4(c)). The channel region of the device is now completely neutral. Under this bias condition the JLT is fully turned on. The dominant conduction mechanism is a bulk current (volume conduction; on-state).
- *Accumulation mode*: occurs for $V_{gs} > V_{fb}$. Charge carriers are accumulated beneath the silicon-to-oxide interface. This is not suitable for optimum device operation, since the accumulated charges face the problem of surface roughness scattering at the oxide interface, which reduces the mobility of the carriers and hence the maximum output current (surface conduction, Fig. 2.4(d)).

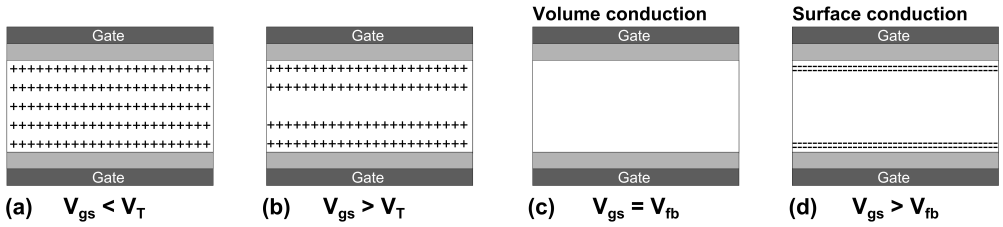


Figure 2.4: (a) For $V_{gs} < V_T$ the device operates in depletion mode and the device is turned off. (b) $V_T < V_{gs} < V_{fb}$ is called bulk current mode. (c) $V_{gs} = V_{fb}$ is the flat-band mode, where the device is fully turned on. (d) $V_{gs} > V_{fb}$ is referred to as the accumulation mode. The source/drain regions are not shown to simplify matters.

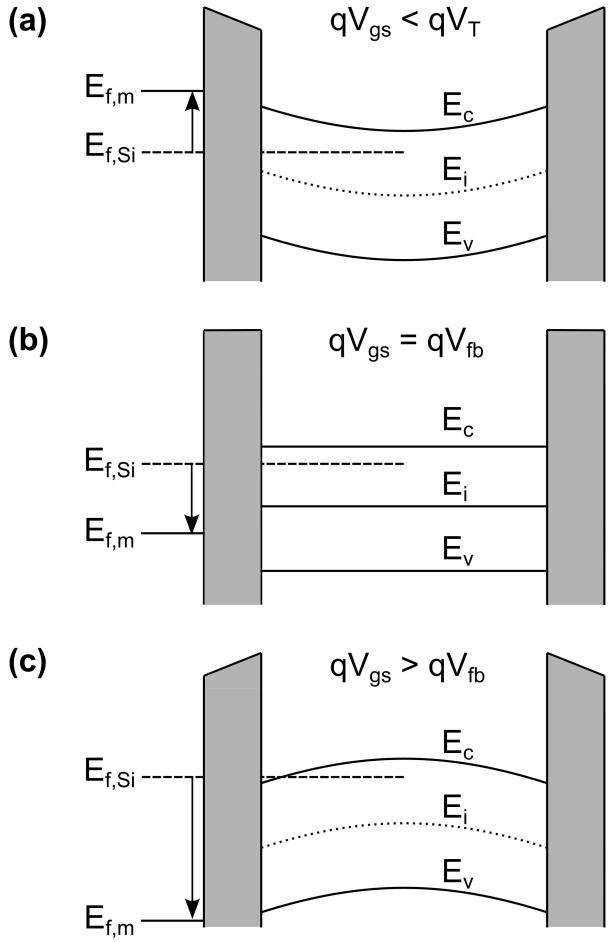


Figure 2.5: Band diagram from gate to gate of the junctionless DG MOSFET shown in Fig. 2.1, with N_d as the channel doping concentration. The device operates in: (a) depletion, (b) flat-band and (c) accumulation mode.

It is important to note that the transition from the depletion to the accumulation mode creates two distinct slopes in the charge-voltage (dQ_m/dV_{gs}) characteristics and therefore, results in two different effective gate capacitances (per unit area) C_{eff} and C_{ox}, respectively [86]. $C_{eff} = (1/C_{ox} + 1/C_{dep})^{-1}$ represents the effective gate capacitance in depletion with $C_{dep} = (4\,\varepsilon_{Si}/T_{ch})$ as the depletion capacitance, whereby ε_{Si} is the permittivity of silicon. This effect must carefully be taken into account when modeling the physics of the JLT.

As in the case of an inversion mode MOSFET the drain current can be calculated assuming that the GCA is valid and by expressing the current as a function of the mobile charge carriers (per unit area). However, in junctionless MOSFETs the drain current must be derived taking into account its two main important operating modes (volume and surface conduction). This results in separate expressions for the current in depletion and accumulation. The developed, new drain current expression is continuous and valid from below to well above threshold voltage (see section 4.6).

2.4 State-of-the-Art - Junctionless MOSFETs

1-D Models

A very important task is the development of models to describe the behavior of JLTs in a physical manner. Different models and approaches were published, which warrant a discussion.

In [86] a compact model for the JL DG MOSFET valid in all operating regimes was presented. Their approach led to simple equations compared to other models, while the high accuracy and physical consistency was retained. The model reproduces the two discussed conduction modes well. In order to find closed-form expression for the current, they introduce some mathematical manipulations.

A model for junctionless nanowire FETs was proposed in [87], where the current is calculated in the separated operating regimes and then superposed. The device variability and the parasitic source/drain resistances were identified as the most important limitations of the JL nanowire field-effect transistor.

An analytical model for symmetric junctionless DG MOSFETs was derived in [88]. By using charge-based expressions, a continuous current model was derived. The occurrence of two distinct slopes in the charge-voltage dependence, which constitutes a major difference compared to junction-based MOSFETs, was well covered by their model. However, at this point, their results for the current showed inaccuracies in the depletion region, whose origins were yet not clarified.

An advanced model for the DG structure, where most parameters were related to physical magnitudes, was shown to be in excellent agreement with the simulation data [89]. The effect of the series resistance and the fulfillment of the requirement of being symmetrical with respect to $V_{ds} = 0\,\mathrm{V}$ was discussed.

In [90] quantum mechanical effects (QMEs), which are obtained under two different quantum confinement conditions, were included. It was shown that the quantum confinement is higher in JL than in IM DG MOSFETs, regardless of the channel thickness. Nevertheless, this model is only valid in the subthreshold regime.

A physics-based model for the UTB SOI-FET, which is based on an improved depletion approximation and which provides a very accurate solution of Poisson's equation was discussed in [91]. A computation method of the substrate, as well as the Si-body's lower- and upper-surface potentials by an iterative procedure, which accounts for the backoxide (BOX) charge and thickness and the potential drop within the substrate was presented.

The trade-off between the electrostatic control and the current drivability was evaluated by Matthieu Berthomé *et. al.* [92]. The focus was on various MOSFET architectures based on single-gate, double-gate and Gate-All-Around (GAA) transistors. The model permits a first-order description of the drain current, the pinch-off and flat-band voltages.

A physics-based, analytical model for the drain current in junctionless nanowire transistors (JNTs) was addressed in [93]. The proposed model is continuous from the subthreshold region to the saturation. The derived charge density was expressed as the sum of charge densities in two separate channel regions, which were connected by using a smoothing function later on.

[94] presents a full-range drain current model for long-channel double-gate junctionless transistors. Including dopant and mobile carrier charges, a continuous 1-D charge model was derived by extending the concept of parabolic potential approximation for the subthreshold and the linear regions. Based on the charge model, the Pao-Sah integral was analytically carried out and a continuous drain current model was obtained.

A continuous model for the drain current of junctionless cylindrical surrounding-gate Si nanowire MOSFETs was proposed in [95]. The model is based on an approximated solution of Poisson's equation considering both body doping and mobile charge concentrations and did not introduce any empirical fitting parameters.

In [96] a surface potential based model for symmetric long-channel junctionless double-gate MOSFETs was developed. The relations between surface potential and gate voltage were derived from effective approximations to Poisson's equation for deep depletion, partial depletion, and accumulation conditions. However, no closed-form expressions for the drain current were presented.

In [97] the depletion width equation was simplified by the unique characteristic of junctionless transistors (high channel doping concentration). From the depletion width formula, the bulk current model was constructed using Ohm's law. An analytical expression for subthreshold current was derived. The model was validated for different device setups.

F. Jazaeri *et. al.* [98] developed a closed-form solution for trans-capacitances in long-channel junctionless DG MOSFETs. The model was derived from a coherent charge-based model. A complete intrinsic capacitance network was obtained, which represented an important step toward AC analysis of circuits, based on junctionless devices. The Ward-Dutton partitioning

principle and a cubic function were applied to derive the model for the trans-capacitances.

R. D. Trevisoli *et. al.* were focusing on the threshold voltage in JNTs and presented some analytical models for their description and an extraction method in [99] and [100], respectively. A simple modification to account for QMEs in such devices was included. The corner capacitances were addressed in their work, as well as temperature effects on the threshold voltage. The model was compared versus numerical and experimental data.

Yuan Taur *et. al.* discussed the on-off charge-voltage characteristics and dopant number fluctuation effects in JL DG MOSFETs in [101]. A first-order analytic expression showed that the one-sigma threshold fluctuation is proportional to the square root of doping concentration. They stated that the effect of dopant number fluctuations on the threshold voltage is a serious problem in JL devices, due to the high channel doping concentration.

A. Cerdeira *et. al.* presented a new charge-based analytical compact model for symmetric double-gate junctionless transistors [102]. The model is physics-based and considers both the depletion and accumulation operating conditions including the series resistance effects. Additionally, a symmetry test around $V_{ds} = 0\,\mathrm{V}$ was performed.

So far, all mentioned models are only valid for long-channel devices (1-D), which clearly indicates the need for an analytical, physical compact model valid for short-channel JL devices as well.

2-D Models

Recently, some 2-D models were published for different device geometries. An analytical subthreshold behavior model for junctionless cylindrical surrounding gate MOSFETs was developed in [103], whereby 2-D Poisson's equation was solved in cylindrical coordinates. The subthreshold characteristics were investigated in terms of the channel's electrostatic potential distribution, subthreshold current and slope.

A 2-D semi-analytical solution for the electrostatic potential valid for junctionless symmetric DG MOSFETs in subthreshold regime was proposed by A. Gnudi *et. al.* [104]. It is based on the parabolic approximation for the potential and therefore, removed previous limitations. A semi-analytical expression for the current was derived. Relevant SCEs, such as threshold voltage roll-off, DIBL and inverse subthreshold slope were evaluated.

In [105] an analytical threshold voltage model for a junctionless DG MOSFET with localized charges was developed. It was derived from 2-D Poisson's equation using the parabolic potential approximation. Threshold voltage dependencies on various device parameters were worked out and analyzed.

R. D. Trevisoli *et. al.* [106] proposed a drain current model for triple-gate n-type JNTs. First, the 2-D Poisson equation was used to obtain the effective surface potential for long-channel devices, which was used to calculate the charge density along the channel and the drain current. The solution of the 3-D Laplace equation was then added to the 2-D model in order to account

for the SCEs. To obtain the drain current including SCEs, the surface potential was recalculated for a modified gate voltage (iteration).

In 2014 Guangxi Hu *et. al.* [107] published a paper, where they present an analytical model for the electric potential, threshold voltage and subthreshold swing of junctionless surrounding-gate transistors. They solved the 2-D Poisson equation in a manner that the gradual-channel approximation is not needed.

The models presented in [103–105] and [107] are only valid in subthreshold region and do therefore, not properly describe the complete device behavior. In [106] a complete 2-D model was presented. However, their modeling approach requires iterations, they do not show derivatives of higher-order of the drain current and they do not perform a symmetry-test. Similar to inversion mode devices, both tests must be addressed in a full compact model.

Technologies

A complete fabrication process of a junctionless multiple-gate MOSFET was detailed in [81], which is briefly reviewed here considering an n-channel transistor. The devices were made on a standard SOI wafer. The SOI layer was thinned down to $10-15\,\mathrm{nm}$ and patterned into nanowires using an e-beam lithography. After performing the gate oxidation, an ion implantation was used to dope the devices uniformly $n+$ with a concentration of $1-2\cdot10^{19}\,\mathrm{cm}^{-3}$. A $p+$ poly-silicon gate was used. No additional source/drain implants were used after patterning the gate. The oxide was deposited and etched to form contact holes and a $TiW+Al$ metalization completed the process. The nanowires were fabricated with thicknesses ranging from 5 to 10 nm, a width ranging from 20 to 40 nm and a gate oxide thickness of 10 nm. Similar devices with additional source/drain implants were also fabricated to reduce the parasitic access resistances, which improved the drain current.

J.-P. Colinge *et. al.* [82, 84] found that the JNT has very small short-channel effects, high drive currents and a lower input gate capacitance compared to inversion mode devices, which increases its switching speed. The perspectives for CMOS logic was addressed in [32]. These devices offer full CMOS functionality, but contain no junctions or doping gradients and are therefore, much less sensitive to thermal budget issues than regular CMOS devices.

R. T. Doria *et. al.* [85] presented the evaluation of the analog properties of n-MOS JL multiple-gate transistors. The study was performed for devices operating in saturation as single transistor amplifiers, whereby the dependence of the analog properties on fin width and temperature was taken into account. JL devices were shown to have both larger Early voltage V_{EA} and intrinsic voltage gain A_V than IM devices of similar dimensions. They found that, V_{EA} and A_V were always improved in JL devices when the temperature was increased, whereas IM devices present a maximum value at room temperature. In addition, the JL device was able to provide a constant drain current over a wide temperature range, unlike IM devices, where a degradation of I_{ds} results when maintaining a fixed g_m/I_{ds} value when the temperature is

increased. It can be pointed out that JL devices presented better analog properties than their inversion mode counterparts in low-moderate frequencies of operation. The JL transistor was therefore encouraged to be applied mainly in baseband current-biased circuits.

Other groups dedicated their work to the impact of the series resistances in the current-voltage characteristics of JNTs and its dependence on the temperature [108]. A low-temperature electrical characterization of JL transistors was done by [109]. The electron mobility in heavily doped junctionless nanowire SOI MOSFETs was investigated in [110] and the electrical characteristics of JNTs at a channel length of 20 nm were studied in [111]. A parameter extraction methodology for electrical characterization of JLTs was presented in [112]. The impact of substrate bias on the steep subthreshold slope in junctionless multiple-gate FETs was subject of [113]. An investigation of the zero temperature coefficient in JNTs was done by R. D. Trevisoli *et. al.* [114] and a comparison of manufactured junctionless versus conventional triple-gate transistors with channel lengths down to 26 nm was performed in [115]. Also, the variability of the drain current, induced by random doping fluctuation, of junctionless nanoscale double-gate transistors was intensively investigated by Gino Giusi *et. al.* [116]

In 2014, Changjin Wan *et. al.* [117] presented a study where the junctionless transistor was applied in the field of associative learning in neuromorphic engineering. Indium-zinc-oxide based electric-double-layer junctionless transistors gated by nanogranular SiO_2 proton conducting electrolyte films were proposed. They found out that such proton conductor gated transistors with associative learning functions are promising candidates in neuromorphic circuits.

For the first time, III-V junctionless transistors were experimentally demonstrated in [118]. The source/drain resistances and the thermal budget were minimized by using metal-organic chemical vapor deposition instead of an implantation process. The fabricated devices exhibited very good g_m linearity at low biases, which is favorable for low-power RF applications.

CHAPTER 3

Mathematical Basics

The steady miniaturization and its related new multidimensional effects in state-of-the-art MOSFET structures, which mainly occur due to the inhomogeneous electric field within these devices, are reasons for the permanent development of new physics-based, mathematical and analytical models. In this thesis, in order to find closed-form expressions for the electrostatics inside the channel and oxide regions of the MOSFET, the complex potential theory and the conformal mapping technique are applied to solve the related partial differential equations (PDEs). This section is mainly based on references [57] and [119–121].

3.1 Poisson's and Laplace's Equation

There exist two important equations which are commonly used to solve potential problems in electrostatics, mechanics and physics. The first one is the Poisson equation, a PDE based on Maxwell and the second one is the Laplace equation. For the calculation of the electrostatics, the potential is related to the charge density ρ along a gradient r which gives rise to it. Its electric field $\vec{E}$ is related to the charge density by the divergence relationship.

$$\nabla \cdot \vec{E}(r) = \frac{\rho(r)}{\varepsilon}, \tag{3.1}$$

where ε is the material dependent permittivity. The electric field of the inhomogeneous Poisson equation then reads as:

$$-\nabla \cdot \vec{E} = \Delta\phi(r) = -\frac{\rho(r)}{\varepsilon_0\,\varepsilon_{Si}}. \tag{3.2}$$

The potential ϕ and the charge ρ are three-dimensional dependent. Therefore, by using the Laplace operator Δ one obtains:

$$\Delta = \frac{\partial^2}{\partial x^2} + \frac{\partial^2}{\partial y^2} + \frac{\partial^2}{\partial z^2} \tag{3.3}$$

and finally the Poisson equation.

$$\Delta\phi(x,y,z) = -\frac{\rho(x,y,z)}{\varepsilon} \tag{3.4}$$

A formal solution to Poisson's equation is obtained by adding a volume integral over all space charge elements ρ inside the considered volume and an integral over the surface charge density σ along the boundary of the region [57].

$$\phi(x,y,z) = \frac{1}{4\,\pi\,\varepsilon}\iiint\limits_{\tau}\frac{\rho}{r}\,d\tau + \frac{1}{4\,\pi\,\varepsilon}\iint\frac{\sigma}{r}\,dS, \tag{3.5}$$

where r can be described as the distance from the point at which $\phi(x,y,z)$ is being computed to the charge elements.

If a charge free region of space is considered ($\rho = 0$), the homogeneous Laplace equation is obtained.

$$\Delta\phi(x,y,z) = 0 \tag{3.6}$$

This Laplace equation is a special case of the Poisson equation. Any function $\vec{E}(x,y,z)$, which has continuous second-order derivatives in x, y and z, that satisfy the Laplace equation (3.6), is called an harmonic function within the region where that is true. These harmonic functions have some specific properties [57, 119]:

1. Superposition principle holds.

2. Dirichlet condition (boundary value problem of first kind): an harmonic function ϕ in an enclosed area V, which gets predetermined values ϕ_a, when approaching the edge of V. This boundary condition is - if at all - solvable.

3. Neumann condition (boundary value problem of second kind): an harmonic function ϕ in an enclosed area V, which gets a predetermined normal derivative $n \cdot \nabla\phi$, when approaching the edge of V, whereby n is the unit normal vector. This boundary condition, except for one constant, is - if at all - solvable.

In general, also mixed boundary conditions, where a part of the edge can be a Dirichlet and the other one a Neumann condition, do exist.

3.2 Complex Potential Theory

In particular, the complex potential theory deals with analytical functions of complex variables. Due to the fact that the separable real and imaginary parts of any analytical function must satisfy Laplace's equation, the complex potential theory is commonly used to solve two-dimensional problems. By giving every complex number of the variable z the value of a variable w, using

$w = P(z) = \phi(x,y) + i\Xi(x,y)$, then w is called a complex function of the complex variable z, where

$$z = x + iy. \tag{3.7}$$

A complex function can therefore be represented by the sum of the real part $u(x,y)$ and the imaginary part $iv(x,y)$ with u and v as real functions.

$$f(z) = f(x + iy) = u(x,y) + iv(x,y) \tag{3.8}$$

It maps all points within an area V from z-plane to points of an area V^* in w-plane [120]. To solve two-dimensional problems, one often uses the differentiability of complex functions, whereby the limit

$$\lim_{z\to 0} \frac{f(z) - f(z_0)}{z - z_0} \tag{3.9}$$

must exist.

$$\frac{df}{dz} = \lim_{\Delta x\to 0} \frac{f(z_0 + \Delta x) - f(z_0)}{\Delta x} = \frac{\partial u}{\partial x} + i\frac{\partial v}{\partial x} \tag{3.10}$$

$$\frac{df}{dz} = \lim_{\Delta y\to 0} \frac{f(z_0 + i\Delta y) - f(z_0)}{i\Delta y} = -i\frac{\partial u}{\partial y} + \frac{\partial v}{\partial y} \tag{3.11}$$

From the partial derivatives of u and v we receive the Cauchy-Riemann conditions.

$$\frac{\partial u}{\partial x} = \frac{\partial v}{\partial y} \qquad \text{and} \qquad \frac{\partial u}{\partial y} = -\frac{\partial v}{\partial x} \tag{3.12}$$

Differentiating twice finally leads to the result that every complex function $f(z)$, which is differentiable, is harmonic and therefore a solution of the Laplace equation.

$$\frac{\partial^2 u}{\partial x^2} + \frac{\partial^2 u}{\partial y^2} = 0 \qquad \text{and} \qquad \frac{\partial^2 v}{\partial x^2} + \frac{\partial^2 v}{\partial y^2} = 0 \tag{3.13}$$

Assume that, in electrostatics the real part u of the complex function $f(z)$ is defined as the electric potential $\phi(x,y)$. The corresponding vector field of the electric field strength is then given by:

$$\vec{E} = E_x\,\vec{e}_x + E_y\,\vec{e}_y = -\nabla\phi \tag{3.14}$$

with

$$E_x = -\frac{\partial \phi}{\partial x} \qquad \text{and} \qquad E_y = -\frac{\partial \phi}{\partial y}. \tag{3.15}$$

From equations (3.12) and (3.15) follows:

$$E = E_x + iE_y = -\frac{\partial \phi}{\partial x} + i\frac{\partial \phi}{\partial y} = -\overline{\left(\frac{dP}{dz}\right)}. \tag{3.16}$$

The dielectric flow between two points A and B might then be calculated with the help of the complex potential theory to:

$$\int_A^B (D_x\, dy - D_y\, dx) = \varepsilon\,(\Xi_A - \Xi_B). \tag{3.17}$$

The function

$$P(z) = \phi(x,y) + i\Xi(x,y) \tag{3.18}$$

is called complex potential function. The real part describes the electric potential and the imaginary part the electric flux. This function can be used to calculate either the characteristics of the equipotential lines ($\phi(x,y) = \text{const.}$), or the characteristics of the field lines ($\Xi(x,y) = \text{const.}$) as shown in Fig. 3.1.

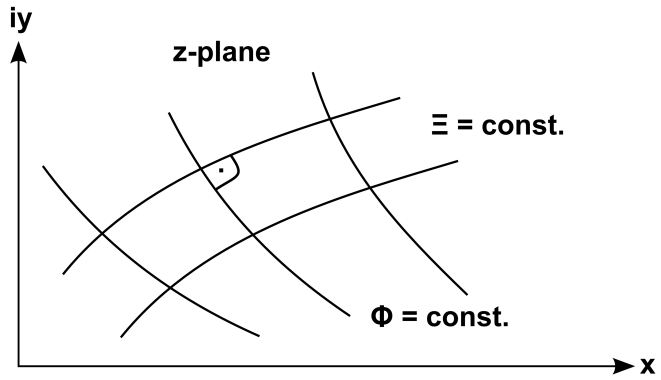


Figure 3.1: Set of curves of a complex potential function $w = P(z) = \phi(x,y) + i\Xi(x,y)$. Due to the fact that $\partial u/\partial x \cdot \partial v/\partial x + \partial u/\partial y \cdot \partial v/\partial y = 0$, the curves of the real part (equipotential lines) are always perpendicular to the imaginary part (field lines).

3.3 Conformal Mapping Technique

Conformal mapping means to map a complex geometry from one plane to a geometry with less complexity into another plane with the help of an analytical function $w = f(z)$. Let us therefore call these planes z and w, which are defined as:

$$z = x + iy \tag{3.19}$$

$$w = u + iv. \tag{3.20}$$

After mapping into the w-plane, the desired potential can be calculated more easily. This process is also called transformation [121]. If a set of curves in z-plane, where the field lines are perpendicular to the equipotential lines, is transformed to w-plane, the set of curves are still

perpendicular to each other. Otherwise the transformation is not analytic and therefore not conformal.

3.3.1 Transformation of a Potential

If a transformation of equation (3.18) to w-plane is done, we receive [57]:

$$\tilde{P}(u,v) = \tilde{\phi}(u,v) + i\tilde{\Xi}(u,v), \tag{3.21}$$

where $\tilde{\phi}(u,v)$ and $\tilde{\Xi}(u,v)$ still are harmonic functions. The absolute value of the field strength is therefore scaled with respect to the geometry.

$$|E|_{(z)} = |E|_{(w)} \cdot \left|\frac{dw}{dz}\right| \tag{3.22}$$

An integration along a line in z-plane has therefore the same results as an integration along a line in the transformed w-plane. If considering Poisson's equation, the space charge ρ needs a scaling as well, because Poisson's equation must be invariant regarding the conformal mapping [120].

$$\rho_{(w)} = \frac{\rho_{(z)}}{\left|\frac{dw}{dz}\right|^2} \tag{3.23}$$

3.3.2 Transformation of a Closed Polygon

In the next step the conformal mapping technique by Schwarz-Christoffel is applied to map a geometry from z-plane, with polygon shaped boundaries, into a w-plane with the help of an analytical function $z = f(w)$. That means, a complex geometry from z-plane is mapped to a geometry with less complexity into the upper half of the w-plane. Then, in w-plane, all boundaries are located on the real axis and so, the desired values can be solved more easily (Figure 3.2). For these calculations one has to set up the differential $\frac{dz}{dw}$ of this function [57].

$$\frac{dz}{dw} = C \cdot (w - w_1)^{-\gamma_1} (w - w_2)^{-\gamma_2} ... (w - w_\nu)^{-\gamma_\nu} ... = C \cdot \prod_{(\alpha)} (w - w_\alpha)^{-\gamma_\alpha}, \tag{3.24}$$

where the constant C acts as scale and rotation factor. From equation (3.24) follows:

$$z = C \cdot \int \prod_{(\alpha)} (w - w_\alpha)^{-\gamma_\alpha} \, dw + D, \tag{3.25}$$

where D is an integration constant, which represents the origin of the coordinate system in z-plane and γ as the change of angle at the vertex α of the geometry. The remaining parameters

can then be calculated via:

$$z'_\nu - z''_\nu = -i\,\pi\,C \cdot \prod_{\alpha \neq \nu} (w_\nu - w_\alpha)^{-\gamma_\alpha}, \tag{3.26}$$

with $\gamma_\nu = +1$ and the point $z_\nu = \infty$. If in addition $u_\nu = \pm\infty$ is valid, equation (3.26) simplifies to:

$$z'_\nu - z''_\nu = i\pi\,C. \tag{3.27}$$

A polygon with N vertexes has w_α points and together with the integration constants C and D there are $N + 2$ unknown parameters left to be determined. Because only three parameters can be chosen freely, $N - 1$ parameters have to be solved by making use of equation (3.26) and (3.27) [57].

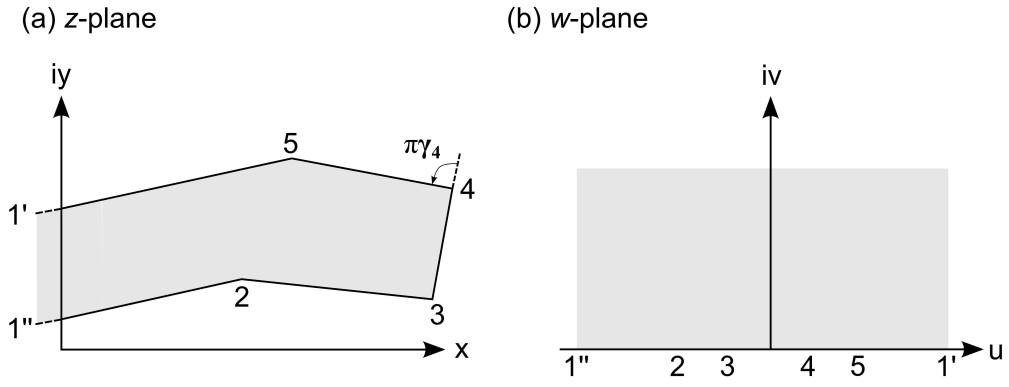


Figure 3.2: Transformation from (a) z-plane into (b) w-plane.

3.4 Strategy of Decomposition

The general aim of the work is to find closed-form solutions to Poisson's equation in order to properly describe the device's electrical behavior. Depending on the complexity of the structure, in which the Laplace equation is to be conformal mapped, this aim might not be fulfilled. In addition, if one takes into account the space charge ρ, the probability of finding an analytical, closed-form expression approaches zero. Nevertheless, in order to calculate the potential two-dimensionally, the solution of Poisson's equation can be decomposed into separate parts: a two-dimensional solution $\varphi(x,y)$ of the homogeneous Laplacian differential equation and a one-dimensional particular solution $\phi_p(y)$, which only depends on one coordinate [122].

$$\Delta\phi(x,y) = -\frac{\rho}{\varepsilon} = \Delta\varphi(x,y) + \Delta\phi_p(y), \tag{3.28}$$

whereby the decomposed parts are:

$$\Delta\varphi(x,y) = 0 \tag{3.29}$$

$$\Delta\phi_p(y) = -\frac{\rho(y)}{\varepsilon}. \tag{3.30}$$

Accordingly, the boundary conditions of Poisson's equation have to be transformed with respect to the one-dimensional particular solution.

$$\varphi(x,y) = \phi(x,y) - \phi_p(y) \tag{3.31}$$

This simplification enables us to only apply the conformal mapping technique to the Laplace solution without the necessary scaling of the space charge ρ.

3.5 Potential Solution of Boundary Value Problems of First Kind

Generally, mixed boundary problems occur through solving the potential solution for MOSFETs. In this thesis, the structures to be solved only requires Dirichlet boundary conditions, so that Neumann boundaries do not play any role. This fact reduces the time of finding a potential solution enormously. The presented strategies for solving 2-D boundary conditions are valid for Laplace problems, but by applying the mentioned decomposition strategy (see section 3.4), they can also be applied to solve Poisson's equation in 2-D [120].

3.5.1 Single Vertex Approach

The solution of a potential problem in closed-form within z-plane, via a transformation using the conformal mapping technique (section 3.3), presupposes, that this potential problem can also be calculated in closed-form within w-plane. Figure 3.3(a) shows two electrodes on the u-axis having a potential difference $d\varphi$ and an infinitesimal gap $w = \overline{u}$. This gap leads to:

$$P = \phi + i\Xi = d\varphi + i\frac{d\varphi}{\pi}\,\ln(w - \overline{u}). \tag{3.32}$$

This approach was successfully used and verified versus 2-D numerical simulation data in [123–128]. However, the single vertex approach is analytical, but does not represent a closed-form solution of the potential. Therefore, another solution is proposed in the next section which is based on Poisson's integral.

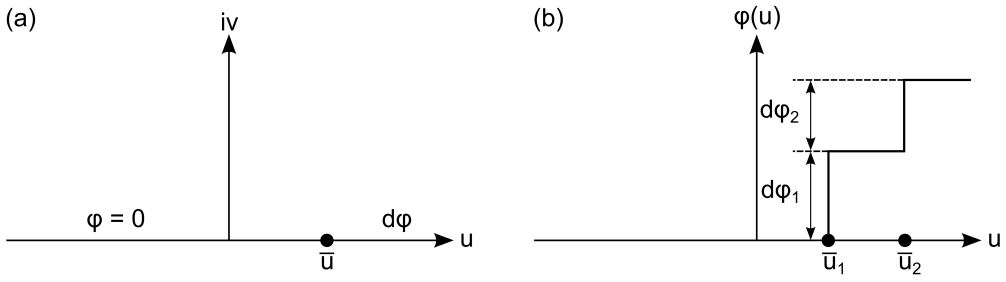


Figure 3.3: (a) Shows two electrodes having a potential difference $d\varphi$ and an infinitesimal gap at position $\overline{u}$. The potential solution of this problem will be used to calculate the solution of a problem with boundary conditions as shown in (b). This is done by the superposition of the two electrodes with different $\overline{u}$ and $d\varphi$.

3.5.2 Poisson's Integral in W-Plane

The potential solution of boundary value problems of first kind in w-plane can be solved in closed-form by using the following Poisson integral [57].

$$\varphi(u,v) = \frac{1}{\pi} \int_{-\infty}^{+\infty} \frac{v}{(u-\overline{u})^2 + v^2} \cdot \varphi(\overline{u})\, d\overline{u}, \tag{3.33}$$

with $\varphi(\overline{u})$ as the mapped boundary condition along the considered geometry.

$$\varphi(\overline{u}) = \varphi(f^{-1}(\overline{z})). \tag{3.34}$$

In this thesis, the potential problems are preferably solved by using Poisson's integral, since it leads to analytical, closed-form expressions for the device's electrostatics in 2-D and 3-D.

CHAPTER 4

DC Model

In this chapter the development of the 2-D compact DC model for the inversion mode and junctionless MOSFET is presented. That is, the voltages applied at the terminals of the device remain constant and do not vary with time. The derivation of the closed-form solution of the 2-D potential, as well as the derivation of the electrical model parameters, such as threshold voltage, drain-induced barrier lowering and subthreshold slope are presented. The calculation of the mobile charge density is addressed and a modified current equation for junctionless MOSFETs is presented. The analytical model is verified by comparisons with 2-D TCAD simulation data. The device structure is shown in Fig. 4.1, with L_g as the gate/channel and L_{sd} the source/drain length, T_{ch} as the channel and T_{ox} the oxide thickness. For simplicity, the channel length is assumed to be identical with the gate length, i.e. no gate over-lap, or under-lap regions are considered. The model will be verified for different channel lengths from 100 nm down to 22 nm and different channel doping concentrations ($N_{a/d} = 1 \cdot 10^{15}\,\mathrm{cm}^{-3}$ to $N_{a/d} = 2 \cdot 10^{19}\,\mathrm{cm}^{-3}$).

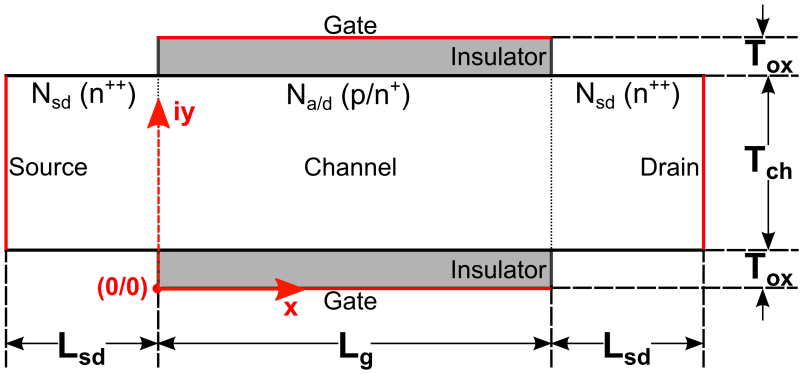


Figure 4.1: Longitudinal cross-section of the IM DG and JL DG MOSFET showing its physical device dimensions and doping profiles. $N_{a/d}$ is the channel doping concentration of the IM and JL device, respectively, and N_{sd} the source, drain doping concentration. The red lines represent the source/drain and gate electrodes.

4.1 Modeling Preliminaries

This section describes the necessary steps prior to the calculation of the electrostatic potential. Some details about the Poisson's equation are presented, as well as the simplifications which are used in the model in order to arrive at a closed-form solution. The usage of the conformal mapping technique and Poisson's integral in w-plane are explained.

4.1.1 Poisson's Equation

The main goal is to develop closed-form expressions that describe the electrical properties of IM and JL DG n-MOSFETs. The depletion approximation is applied, wherefore 2-D Poisson's equation inside the channel region reduces to:

$$\Delta\phi(x,y) = -\frac{\rho}{\varepsilon_{Si}}. \tag{4.1}$$

ρ is the space charge and ε_{Si} the permittivity of the silicon. The difference between an inversion mode and a junctionless MOSFET are the differently charged implants. Therefore, the reversed sign of the depletion charge in the channel region, $\rho = -qN_a$ (acceptors) is used in case of the inversion mode and $\rho = +qN_d$ (donors) in the case of the junctionless MOSFET. For the calculations the solution of Poisson's equation is decomposed into a 1-D particular solution $\phi_p(y)$ and a 2-D solution $\varphi(x,y)$ of the homogeneous Laplacian differential equation [122].

$$\Delta\phi(x,y) = \Delta\varphi(x,y) + \Delta\phi_p(y), \tag{4.2}$$

with

$$\Delta\varphi(x,y) = 0 \tag{4.3}$$

$$\Delta\phi_p(y) = -\frac{\rho}{\varepsilon_{Si}}. \tag{4.4}$$

This allows us to apply the conformal mapping technique to the Laplace part only, whereby the absence of the space charge ρ simplifies the calculations. In that case, ρ has to be constant along the x-direction [122]. By using the afore mentioned decomposition a transformed boundary condition for the calculation of the Laplace solution must be derived.

$$\varphi(x,y) = \phi(x,y) - \phi_p(y) \tag{4.5}$$

4.1.2 Model Simplifications

In a first step QEs are neglected, because the channel thickness is assumed to be at least 10 nm [31]. Then, even though the parasitic resistances play an important role, especially at short-channel sizes [129], the source and drain regions of the DG device are cut out to simplify matters.

Instead, a 1-D effective built-in potential at the source/drain-channel junctions ($V_{bi,eff,s/d}$) is used to account for the potential drop within the highly doped source/drain regions and its effect on the device's electrostatic behavior and performance. In order to avoid discontinuities of the dielectric flux and the electric field E_0 at the silicon-to-oxide interface, which is caused by the different permittivities of the silicon and the oxide, a scaled oxide thickness is introduced [122].

$$D_{ox} = \varepsilon_0 \varepsilon_{Si} \cdot E_0 = \varepsilon_0 \varepsilon_{ox} \cdot E_{ox} = \varepsilon_0 \varepsilon_{ox} \cdot \frac{V_{ox}}{T_{ox}}, \tag{4.6}$$

where D_{ox} represents the dielectric displacement density and V_{ox} the voltage drop across the oxide. Then T_{ox} is scaled by:

$$\tilde{T}_{ox} = \frac{\varepsilon_{Si}}{\varepsilon_{ox}} \cdot T_{ox}, \tag{4.7}$$

using a high-k dielectric ($\varepsilon_{ox} = 7\,\varepsilon_0$). Finally, the discontinuity of the electric field E_0 can be avoided with

$$D_{ox} = \varepsilon_0 \varepsilon_{Si} \cdot E_0 = \varepsilon_0 \varepsilon_{Si} \cdot \frac{V_{ox}}{\tilde{T}_{ox}}. \tag{4.8}$$

This scaled oxide thickness concept is valid and therefore applicable for $L_g >> T_{ox}$ [122]. The resulting simplified device structure is presented in Fig. 4.2.

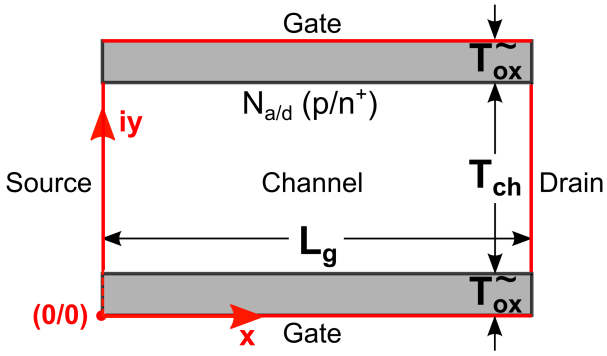


Figure 4.2: Simplified model structure showing coordinate system and boundaries (red lines).

For the calculation of the 2-D Laplace solution $\varphi(x,y)$ within the channel region of the device the 4-corner structure from Fig. 4.2 is decomposed into two 2-corner structures, namely the source related case φ_{source} and drain related case φ_{drain}, which will be solved in the same manner and where only the boundary conditions have to be changed [123]. This decomposition is valid as long as the channel length is larger than the channel thickness ($L_g > T_{ch}$) [130]. It is illustrated in Fig. 4.3, also showing the necessary transformed boundaries (see Table 4.1). By using this decomposition strategy, short-channel effects are still taken into account. Both the source and drain related cases are then solved with the help of the conformal mapping technique.

Electrode	Boundary
Top Gate	$V_1 = 0$
Bottom Gate	$V_1 = 0$
Source	$V_2 = V_s + V_{bi} - \phi_p(y)$
Drain	$V_3 = V_d + V_{bi} - \phi_p(y)$

Table 4.1: Summary of the boundary conditions of the two 2-corner problems from Fig. 4.3. V_{bi} represents the built-in potential and $\phi_p(y)$ corresponds to the 1-D particular solution.

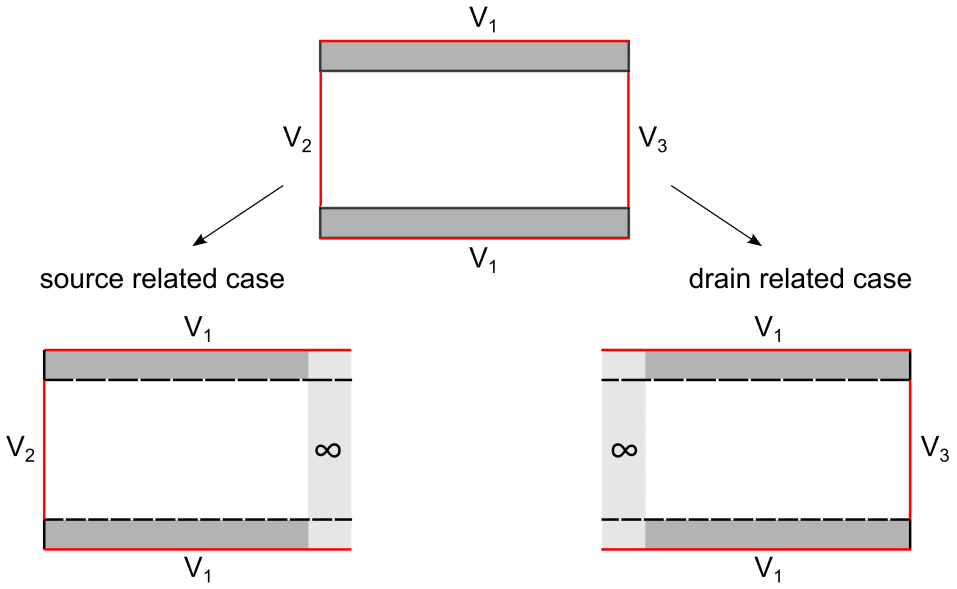


Figure 4.3: The boundaries of the Laplacian differential equation of the 4-corner problem are decomposed into two 2-corner problems in order to ease the calculations. V_1, V_2 and V_3 denote the related boundary conditions (listed in Table 4.1). The red lines represent the contacts of source, drain and gate, respectively.

4.1.3 Conformal Mapping of the Device Structure

To illustrate the utilization of the conformal mapping technique and to explain this transformation, the source related case of the decomposed 4-corner structure (Fig. 4.3) is consulted as an example. The drain related case is calculated analogously by applying the corresponding boundary conditions. Through applying the Schwarz-Christoffel transformation the whole structure from the current z-plane is conformally mapped into a new defined w-plane, whereby the boundaries are now located on the real axis of the w-plane, easing the calculations. The inner region of the structure is transformed onto the upper half of the w-plane.Table 4.2 contains the corresponding relations between the points in z-plane, their values in w-plane and their

associated change of angle at the vertexes of the polygon and Fig. 4.4 depicts the whole transformation process.

$\overline{u}$	$w_{\overline{u}}$	$z_{\overline{u}}$	$\pi\gamma_{\overline{u}}$	$\gamma_{\overline{u}}$
1	$\pm\infty$	$+\infty$	$+\pi$	$+1$
2	-1	z_2	$+\frac{\pi}{2}$	$+\frac{1}{2}$
5	$+1$	z_5	$+\frac{\pi}{2}$	$+\frac{1}{2}$

Table 4.2: Relations between the points in z-plane, their values in w-plane and associated change of angle (see Fig. 4.4).

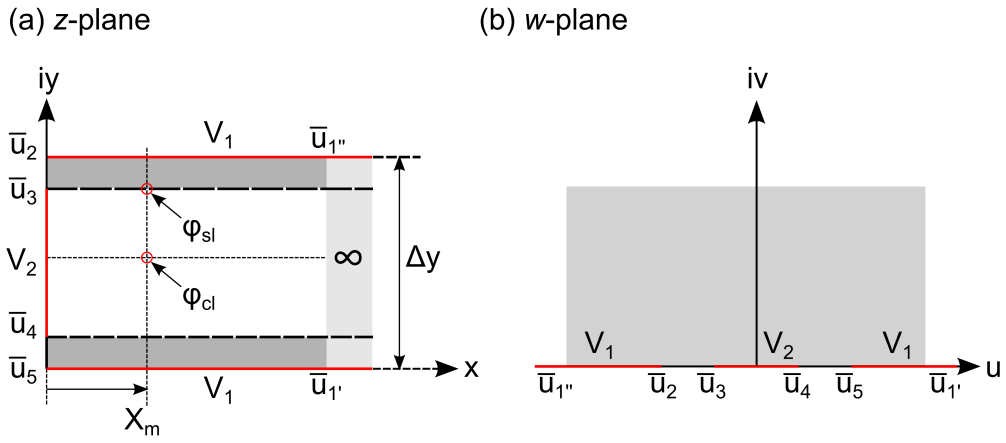


Figure 4.4: (a) Source related case of the decomposed 2-D Laplace solution in z-plane. $\overline{u}_{1''}$ to $\overline{u}_{1'}$ mark the integration borders and V_1 and V_2 denote the boundary conditions. φ_{sl} and φ_{cl} represent the surface and center potential of the Laplacian solution, respectively. x_m denotes the position of the potential barrier inside the channel region (from source-channel junction). $\overline{u}_{1''}$ and $\overline{u}_{1'}$ lie in infinity. Δy is a geometry parameter for the conformal mapping technique. (b) Transformed source related case in w-plane. The boundaries are now located on the u-axis only.

By using equation (3.24) the desired differential is obtained.

$$\frac{dz}{dw} = \frac{C}{\sqrt{w-1}\sqrt{w+1}} \tag{4.9}$$

The integration of equation (4.9) leads then to:

$$z = f(w) = 2\,C \ln\left(\sqrt{w-1} + \sqrt{w+1}\right) + D, \tag{4.10}$$

with D chosen to be 0, because the absolute coordinates are not relevant in this particular case. The constant C is determined with the help of equation (3.27).

$$z_1'' - z_1' = i\Delta y = i\pi\, C \implies C = \frac{\Delta y}{\pi} \tag{4.11}$$

After all parameters are known, the inverse function of equation (4.10) is needed to map all points from the z-plane into the w-plane.

$$w = f^{-1}(z) = u + iv = \cosh\left(\frac{\pi\, z}{\Delta y}\right) = \cosh\left(\frac{\pi\,(x + iy)}{\Delta y}\right), \tag{4.12}$$

with

$$\Delta y = 2\,\tilde{T}_{ox} + T_{ch} \tag{4.13}$$

determined from the given device structure.

4.1.4 Application of Poisson's Integral in W-Plane

The potential solution of boundary value problems of first kind in w-plane (transformed plane) can then be solved by using the following Poisson integral [57].

$$\varphi(u,v) = \frac{1}{\pi}\int_{-\infty}^{+\infty} \frac{v}{(u-\overline{u})^2 + v^2} \cdot \varphi(\overline{u})\, d\overline{u}, \tag{4.14}$$

with $\varphi(\overline{u})$ as the mapped boundary condition along the considered geometry.

4.2 Closed-Form Solution of the 2-D Potential

This section highlights the calculation of the 2-D potential in closed-form. An exact solution for the effective built-in potentials at the source/drain-channel junctions ($V_{bi,eff,s/d}$) is presented. In addition, the calculation of the position of the potential barrier (x_m) within the channel region, at which the potential is calculated, is detailed. According to Eq. (4.2), three major steps have to be performed.

- Calculate the 1-D particular solution $\phi_p(y)$.
- Use the conformal mapping technique in order to calculate the 2-D Laplace solution $\varphi(x,y)$.
- Superpose the 1-D and 2-D solutions.

The following sections focus on these three major steps. To simplify matters and to avoid long naming conventions, the modeling approach is presented for the junctionless DG MOSFET. However, this approach and the derived solutions are also valid for inversion mode devices, if the sign of the depletion charge is reversed accordingly (see section 4.1.1).

Both devices are mainly controlled by their surface and center potentials ϕ_s and ϕ_c, respectively. The accurate calculation of these potentials is therefore of great importance, since the whole model relies on them.

4.2.1 1-D Particular Solution

In the first step, the 1-D particular solution $\phi_p(y)$, which represents the long-channel potential solution, is approximated by a parabolic function. This common method yields the following relations [131, 132]:

$$\phi_{sp} = V_g' - V_{ox} \tag{4.15}$$

$$V_{ox} = -\frac{q\,N_d\,T_{ch}}{2\,C_{ox}}, \tag{4.16}$$

where ϕ_{sp} is the long-channel surface potential, V_{ox} the voltage drop within the oxide, $C_{ox} = \varepsilon_{ox}\,/\,T_{ox}$ the oxide capacitance (per unit area) and $V_g' = V_{gs} - V_{fb}$. V_{gs} denotes the gate-source voltage and V_{fb} the flat-band voltage. The long-channel center potential ϕ_{cp} is then calculated from (compare with Fig. 4.6):

$$\phi_p\left(y = \tilde{T}_{ox}\right) = -\frac{q\,N_d}{2\,\varepsilon_{Si}} \cdot \left(y - \frac{T_{ch}}{2} - \tilde{T}_{ox}\right)^2 + \phi_{cp} = \phi_{sp}. \tag{4.17}$$

Rearranging Eq. (4.17) for ϕ_{cp} then leads to:

$$\phi_{cp} = V_g' - V_{ox} - \left(-\frac{q\,N_d\,{T_{ch}}^2}{8\,\varepsilon_{Si}}\right). \tag{4.18}$$

4.2.2 2-D Laplace Solution

The 2-D Laplace solution is solved at the potential barrier x_m within the channel region, using the conformal mapping technique by Schwarz-Christoffel. Here, the approach is illustrated for the source related case, whereby the drain related case is calculated in the same manner using the corresponding boundary conditions. First, the boundary conditions and then the integration borders according to the device's physical dimensions are defined. Figure 4.5 shows the source related case of the decomposed 2-D Laplace solution, which has the following boundary conditions:

$$V_1 = 0 \tag{4.19}$$

$$V_2 = V_{s/d} + V_{bi} - \phi_p(y), \tag{4.20}$$

with V_{bi} as the built-in potential, and V_s and V_d as the source and drain potential, respectively. For simplicity the boundary within the oxides is assumed to be behave linear, which was confirmed by TCAD Sentaurus simulations [34].

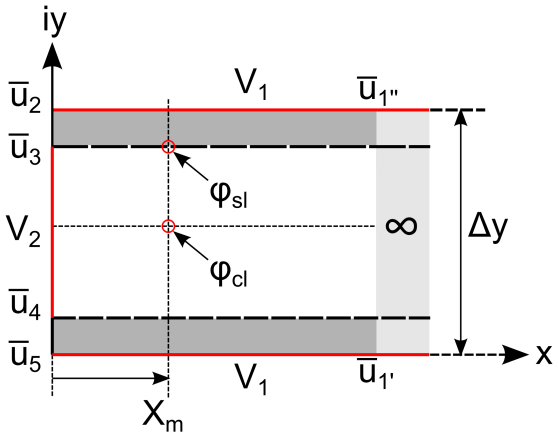


Figure 4.5: Source related case of the decomposed 2-D Laplace solution in z-plane. $\overline{u}_{1''}$ to $\overline{u}_{1'}$ mark integration borders and V_1 and V_2 denote the boundary conditions. φ_{sl} and φ_{cl} represent the surface and center potential of the Laplacian solution, respectively. x_m denotes the position of the potential barrier inside the channel region (from source-channel junction). $\overline{u}_{1''}$ and $\overline{u}_{1'}$ lie in infinity. Δy is a geometry parameter for the conformal mapping technique.

Effective Built-in Potentials

Since the effect of the parasitic source/drain resistances and the influence of the gate electrode on these regions is neglected in the model structure, the built-in potential at the source/drain boundaries is replaced with an effective built-in potential $V_{bi,eff,s/d}$, which depends on the physical device dimensions, source/drain doping concentration N_{sd} and applied voltages. To take into account this important effect, the following set of equations, which originally were derived for conventional inversion mode DG MOSFETs [133, 134] is applied to the model. Since it is assumed that the origin of the coordinate system is located at the silicon-to-oxide interface in their work, the following relation is introduced here:

$$i\hat{y} = iy - \tilde{T}_{ox}. \tag{4.21}$$

By applying some minor modifications, these equations can be adapted to the modeling approach.

$$\lambda_1 = \sqrt{\frac{\varepsilon_{Si}\, T_{ox}\, T_{ch}}{2\,\varepsilon_{ox}} \left(1 + \frac{\varepsilon_{ox}}{\varepsilon_{Si}} \frac{\hat{y}}{T_{ox}} - \frac{\varepsilon_{ox}}{\varepsilon_{Si}} \frac{\hat{y}^2}{T_{ox}\, T_{ch}}\right)} \tag{4.22}$$

$$\Delta V_{bi,s/d} = V_{bi} + V_{s/d} - \phi_{cp/sp} + {\lambda_1}^2 \cdot \frac{q\, N_{sd}}{\varepsilon_{Si}} \cdot \left[1 - \sqrt{1 + \frac{2 \cdot \left(V_{bi} + V_{s/d} - \phi_{cp/sp}\right)}{{\lambda_1}^2 \cdot \frac{q\, N_{sd}}{\varepsilon_{Si}}}}\right], \tag{4.23}$$

with λ_1 as the 1-D natural length, which depends on the channel and oxide thickness, where $\hat{y} = T_{ch}/2$ in the case of the junctionless device, because the focus is on the depletion regime

where the dominating part of the current flows in the channel's center (volume conduction). And with $\hat{y} = 0$ in the case of the inversion mode device, because the dominating current flows in a conducting channel beneath the oxide (surface conduction). The effective built-in potential at the source/drain-channel junctions is then calculated to:

$$V_{bi,eff,s/d} = V_{bi} - \Delta V_{bi,s/d}. \tag{4.24}$$

Replacing V_{bi} in Eq. (4.20) with the effective built-in potentials $V_{bi,eff,s/d}$, leads to accurate results for the potential in the subthreshold regime.

$$V_2 = V_{s/d} + V_{bi,eff,s/d} - \phi_p(y). \tag{4.25}$$

Position of Potential Barrier

Before the integration borders and boundary conditions are defined, the exact position x_m of the potential minimum (or potential barrier) within the channel region must be calculated. This is mandatory since the surface and center potentials are calculated at this position, which has a strong influence on the threshold voltage, charges and the drain current. x_m strongly depends on the channel length, the applied biases and the effective built-in potentials at the source/drain-channel junctions. A simple solution for the calculation of the position of the surface potential minimum, within standard DG inversion mode devices, was derived in [135]. By assuming that the potential minimum in the center of the device is located at the same position as the potential minimum at the surface (Fig. 4.5), this expression can be adapted to the model of this work.

$$x_m|_{\varphi_{sl}} \approx x_m|_{\varphi_{cl}} \tag{4.26}$$

The following relations for x_m are obtained:

$$x_m = \frac{1}{2}\left[L_g - \lambda_2 \ln\left(\frac{\phi_{ss} - \phi_{dd}\,\exp\left(\frac{L_g}{\lambda_2}\right)}{\phi_{dd} - \phi_{ss}\,\exp\left(\frac{L_g}{\lambda_2}\right)}\right)\right], \tag{4.27}$$

with

$$\phi_{ss} = V_s + V_{bi,eff,s} + {\lambda_2}^2\,\beta \tag{4.28}$$

$$\phi_{dd} = V_d + V_{bi,eff,d} + {\lambda_2}^2\,\beta \tag{4.29}$$

$$\beta = -\frac{q\,N_d}{\varepsilon_{Si}} - \frac{1}{{\lambda_2}^2}\,V_g' \tag{4.30}$$

and

$$\lambda_2 = \lambda_1|_{\hat{y}=0} = \sqrt{\frac{\varepsilon_{Si}\,T_{ox}\,T_{ch}}{2\,\varepsilon_{ox}}}. \tag{4.31}$$

Integration Borders

In the second step, in order to calculate the potential at the surface and the center of the channel, the following equation, which is defined according to Eq. (4.12), is used.

$$w_{\varphi_{sl}/\varphi_{cl}} = \cosh\left(\frac{\pi\left(\theta_1 + i\theta_2\right)}{\Delta y}\right), \tag{4.32}$$

with $\theta_1 = x_m$ for the source and $\theta_1 = L_g - x_m$ for the drain related case, respectively, as well as $\theta_2 = \tilde{T}_{ox}$ for the surface and $\theta_2 = \tilde{T}_{ox} + T_{ch}/2$ for the center potential (see Fig. 4.5). The corresponding integration borders are then given as:

$$\overline{u}_{1''} = \cosh\left(\frac{\pi\left(3\,L_g + i\left(2\,\tilde{T}_{ox} + T_{ch}\right)\right)}{\Delta y}\right) \tag{4.33}$$

$$\overline{u}_{2} = \cosh\left(\frac{\pi\left(0 + i\left(2\,\tilde{T}_{ox} + T_{ch}\right)\right)}{\Delta y}\right) \tag{4.34}$$

$$\overline{u}_{3} = \cosh\left(\frac{\pi\left(0 + i\left(\tilde{T}_{ox} + T_{ch}\right)\right)}{\Delta y}\right) \tag{4.35}$$

$$\overline{u}_{4} = \cosh\left(\frac{\pi\left(0 + i\,\tilde{T}_{ox}\right)}{\Delta y}\right) \tag{4.36}$$

$$\overline{u}_{5} = \cosh\left(\frac{\pi\left(0 + i\,0\right)}{\Delta y}\right) \tag{4.37}$$

$$\overline{u}_{1'} = \cosh\left(\frac{\pi\left(3\,L_g + i\,0\right)}{\Delta y}\right). \tag{4.38}$$

Since $\overline{u}_{1''}$ and $\overline{u}_{1'}$ are located at the infinity, one can take three times the channel length $(3 \cdot L_g)$ for their x-coordinate in the implementation.

Boundary Conditions

After these preparations, closed-form expressions for the different boundary conditions must be developed. A solution for constant boundaries φ_{const} (along the source, drain and gate electrode) was derived as [136]:

$$\varphi_{const}(w_{\varphi_{sl}/\varphi_{cl}},\phi_{bnd},\overline{u}_a,\overline{u}_b) = -\frac{\phi_{bnd}\cdot\arctan\left(\frac{u-\overline{u}}{v}\right)}{\pi}\Bigg|_{\overline{u}_a}^{\overline{u}_b}, \tag{4.39}$$

where ϕ_{bnd} is the corresponding boundary condition, and $\overline{u}_a$ and $\overline{u}_b$ are the integration borders.

A solution for linear boundaries φ_{lin} (linear approximation is assumed along the oxide regions) was derived by Schwarz *et. al.* in [136]. In order to find closed-form expressions for

such kind of potential problems, a square root approximation was applied, which was shown to return accurate results [136, 137].

$$\varphi_{lin}(w_{\varphi_{sl}/\varphi_{cl}}, \phi_{bnd}, \overline{u}_a, \overline{u}_b, a, b) = \pm \frac{i \arctan\left[\frac{(a\cdot u\cdot\sigma_1\cdot\sigma_3 - a\cdot b\cdot\sigma_1\cdot\sigma_3 + i\cdot a\cdot v\cdot\sigma_1\cdot\sigma_3)}{\sigma_4}\right]\cdot\sigma_3}{\pi} + \frac{i \arctan\left[\frac{(a\cdot b\cdot\sigma_1\cdot\sigma_2 - a\cdot u\cdot\sigma_1\cdot\sigma_2 + i\cdot a\cdot v\cdot\sigma_1\cdot\sigma_2)}{\sigma_4}\right]\cdot\sigma_2}{\pi}\Bigg|_{\overline{u}_a}^{\overline{u}_b}, \tag{4.40}$$

where $\pm$ depends on the applied bias conditions, with

$$\sigma_1 = \sqrt{-\frac{b-\overline{u}}{a}} \tag{4.41}$$

$$\sigma_2 = \sqrt{-\frac{u-b+iv}{a}} \tag{4.42}$$

$$\sigma_3 = \sqrt{\frac{b-u+iv}{a}} \tag{4.43}$$

$$\sigma_4 = b^2 - 2\,b\,u + u^2 + v^2, \tag{4.44}$$

and the parameters a and b as:

$$a = \frac{\overline{u}_{step} - b}{(\phi_{bnd2} - \phi_{bnd1})^2} \tag{4.45}$$

$$b = \overline{u}_{peak}. \tag{4.46}$$

In order to take into account the parabolically shaped potential profile at the source/drain boundaries, which arises due to the 1-D particular solution, a third equation to boundary problems of parabolic shape φ_{para} is incorporated [138]. Originally, this parabolic solution was derived to describe the potential distribution from gate to gate. However, this approach can be applied to the model if $T_{ch} >> \tilde{T}_{ox}$, even though the potential in the oxide is assumed to be linear.

$$\varphi_{para}(w_{\varphi_{sl}/\varphi_{cl}}, \varphi_{bnd}) = \varphi_{bnd}\cdot\left[\frac{1}{2}\left(\sqrt{1-(u-iv)^2} + \sqrt{1-(u+iv)^2}\right) - v\right], \tag{4.47}$$

with the corresponding boundary condition:

$$\varphi_{bnd} = V_g' - \phi_{cp}. \tag{4.48}$$

The 2-D Laplace solution can now be calculated in closed-form by using the following equations. The calculations are done along the defined integration borders and their related boundary condition. The source and drain related case of the decomposed 4-corner structure

(see section 4.1.2) are calculated analogously by using V_s and V_d in Eq. (4.25), respectively, and the corresponding values for $w_{\varphi_{sl}/\varphi_{cl}}$ in Eq. (4.32). Since the potentials for constant boundaries φ_{const} with V_1 as boundary condition are zero, they can be neglected here.

$$\overline{u}_2 \rightarrow \overline{u}_3 : \varphi_{lin}\left(w_{\varphi_{sl}/\varphi_{cl}}, V_{const}, \overline{u}_2, \overline{u}_3, a, b\right) \tag{4.49}$$
$$a = \frac{\overline{u}_3 - b}{(V_{const} - V_1)^2}$$
$$b = \overline{u}_2$$
$$\overline{u}_3 \rightarrow \overline{u}_4 : \varphi_{const}\left(w_{\varphi_{sl}/\varphi_{cl}}, V_{const}, \overline{u}_3, \overline{u}_4\right) + \varphi_{para}\left(w_{\varphi_{sl}/\varphi_{cl}}, \varphi_{bnd}\right) \tag{4.50}$$
$$\overline{u}_5 \rightarrow \overline{u}_4 : \varphi_{lin}\left(w_{\varphi_{sl}/\varphi_{cl}}, V_{const}, \overline{u}_5, \overline{u}_4, a, b\right) \tag{4.51}$$
$$a = \frac{\overline{u}_4 - b}{(-V_{const} - V_1)^2}$$
$$b = \overline{u}_5,$$

where

$$V_{const} = V_{s/d} + V_{bi,eff,s/d} - V_g'. \tag{4.52}$$

The surface and center potential of the 2-D Laplace solution is finally obtained by adding φ_{source} and φ_{drain}, respectively, calculated with equations (4.49) - (4.51).

$$\varphi_{sl} = \varphi_{source}|_{w_{\varphi_{sl}}} + \varphi_{drain}|_{w_{\varphi_{sl}}} \tag{4.53}$$
$$\varphi_{cl} = \varphi_{source}|_{w_{\varphi_{cl}}} + \varphi_{drain}|_{w_{\varphi_{cl}}} \tag{4.54}$$

4.2.3 Superposed 2-D Potential Solution

In a final step, the complete 2-D closed-form solution for the potential is found by the superposition principle with respect to Eq. (4.2). The 2-D surface and center potential ϕ_s and ϕ_c, respectively, which is calculated at the bias dependent position of the potential minimum x_m, is then given by:

$$\phi_s = \varphi_{sl} + \phi_{sp} \tag{4.55}$$
$$\phi_c = \varphi_{cl} + \phi_{cp}. \tag{4.56}$$

For clarity, Fig. 4.6 illustrates the complete superposition procedure at the source boundary of the device. All separate solutions are shown in full profile, including their boundary conditions, recalling that the calculations are done at discrete positions in the channel region of the device (at surface and center).

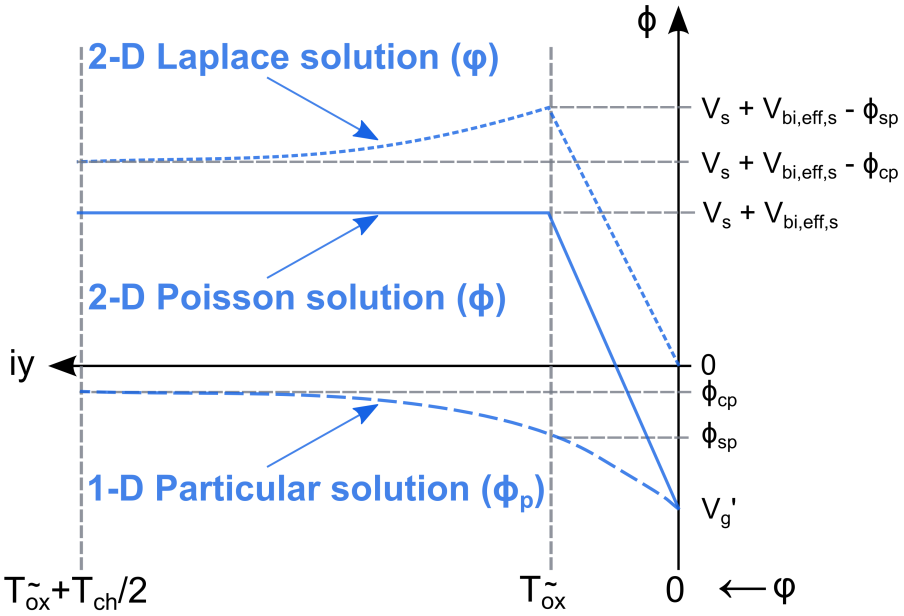


Figure 4.6: Illustration of the potentials at the source boundary in subthreshold region (from gate to channel center). The different closed-form solutions are superposed. The final 2-D potential ϕ has the boundary condition $V_s + V_{bi,eff,s}$ at source, $V_d + V_{bi,eff,d}$ at drain and V_g' at the gate electrode.

4.3 2-D Potential Model Verification

In this section the results for the 2-D potential are presented. The model is compared versus numerical 2-D TCAD Sentaurus simulation data [34]. The devices under investigation have various channel lengths and doping profiles, with a device width of $W_{ch} = 1\,\mu$m. The simulations were done at $T = 300\,$K. Table 4.3 contains the applied settings used in the simulations and in the model. First, the results for the potential in long-channel devices and then in short-channel devices are detailed. The IM MOSFET has a channel doping concentration up to $N_a = 1 \cdot 10^{18}\,\text{cm}^{-3}$. The JL's channel doping concentration is varied up to $N_d = 1 \cdot 10^{19}\,\text{cm}^{-3}$. Additionally, to avoid high parasitic access resistances and to increase the conductivity of these regions [81], additional source/drain implants were used, which also eliminates the need to consider incomplete ionization effects [108]. In the case of the IM or the JL MOSFET, the SlotBoom or the del Alamo model, respectively, is activated in the simulations and in the model to account for the band gap narrowing effects, which are due to the high doping concentrations. In the following, the results are detailed for low and high drain voltages. To obtain the results for the short-channel devices only the flat-band voltage V_{fb} was slightly adjusted (in the mV range).

Parameter	Value
V_{gs}	variable
V_{ds}	$0.05\,\mathrm{V}$ and $1\,\mathrm{V}$
V_{fb}	$\pm 0.01\,\mathrm{V}$
N_d	$1 \cdot 10^{18}\,\mathrm{cm}^{-3}$ and $1 \cdot 10^{19}\,\mathrm{cm}^{-3}$
N_a	$1 \cdot 10^{15}\,\mathrm{cm}^{-3}$ and $1 \cdot 10^{18}\,\mathrm{cm}^{-3}$
N_{sd}	$1 \cdot 10^{20}\,\mathrm{cm}^{-3}$
L_g	$22\,\mathrm{nm}$ and $100\,\mathrm{nm}$
L_{sd}	$10\,\mathrm{nm}$
T_{ch}	$10\,\mathrm{nm}$
T_{ox}	$2\,\mathrm{nm}$
ε_{ox}	$7 \cdot \varepsilon_0$

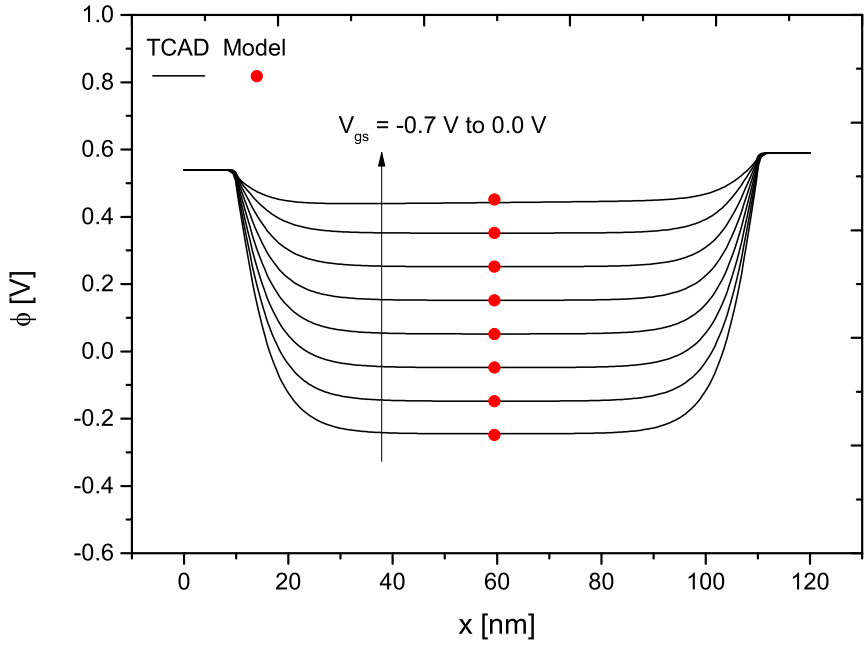
Table 4.3: Simulations and model settings.

4.3.1 2-D Potential of Junctionless DG MOSFETs

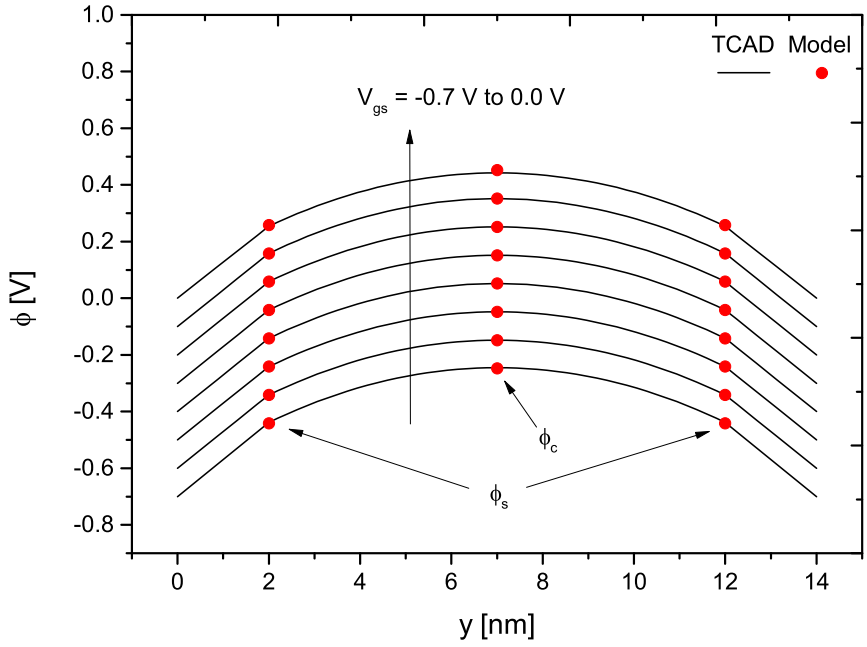
The potential distribution of the long-channel junctionless DG MOSFET is detailed for two slices inside the channel region, at low and high drain voltages. In the following the 2-D model for the potential is extensively verified for different electrical and structural device setups.

Starting at low drain voltages, one can see that the model matches well with the simulation data (Fig. 4.7). In (a) the potential distribution is detailed in the middle of the channel from source to drain, whereby the gate voltages was ramped from $V_{gs} = -0.7\,\mathrm{V}$ to $0.0\,\mathrm{V}$ at $V_{ds} = 0.05\,\mathrm{V}$. It can be observed that the position of the minimum potential $\phi_c(x_m)$ remains constant. It is insensitive to the applied biases. This behavior is confirmed by the simulations. Part (b) illustrates the potential profile from gate to gate. The surface and center potential, which are of main importance are well predicted over a wide voltage range. In particular in the subthreshold region, which is mandatory for the latter calculations of the electrical parameters, charges and drain current, the model agrees well with the reference data.

At higher drain voltages (Fig. 4.8(a)) one can see that the model is still in good agreement with the TCAD simulation data. When V_{gs} increases beyond $0.1\,\mathrm{V}$, the transistor approaches weak accumulation, in which the potential slightly saturates. This effect is not covered by the model since the mobile charges are neglected.Another important aspect is that the shifting position of the potential minimum $\phi_c(x_m)$ is well predicted by the model. It correctly takes into account the dependencies on the applied biases. From Fig. 4.8(b), which details the potential distribution from gate to gate in the middle of the device's channel, it is possible to extract the surface and center potential ϕ_s and ϕ_c, respectively.

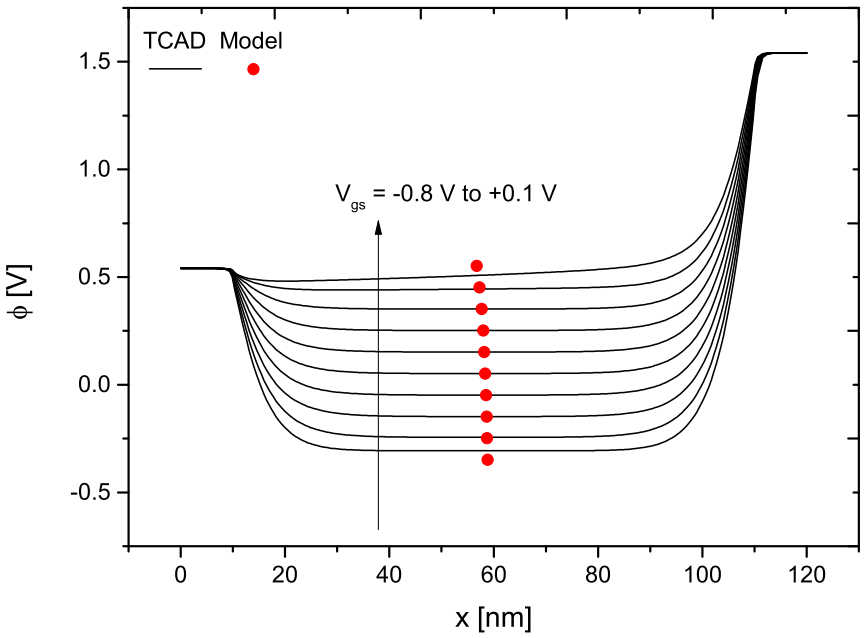


(a)

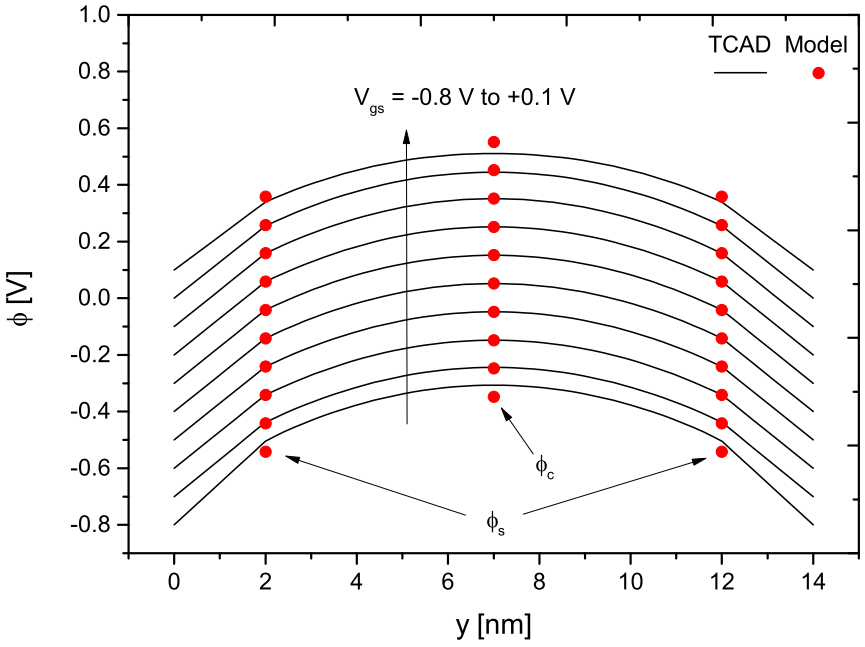


(b)

Figure 4.7: Junctionless DG MOSFET. Potential distribution in the middle of the channel: (a) from source to drain ($\phi_c(x_m)$) and (b) from gate to gate. Parameters: $N_d = 10^{19}\,\mathrm{cm}^{-3}$, $V_{gs} = -0.7\,\mathrm{V}$ to $0.0\,\mathrm{V}$, stepping $0.1\,\mathrm{V}$, $V_{ds} = 0.05\,\mathrm{V}$, $L_g = 100\,\mathrm{nm}$, $L_{sd} = 10\,\mathrm{nm}$, $T_{ch} = 10\,\mathrm{nm}$, $T_{ox} = 2\,\mathrm{nm}$. Lines TCAD; Symbols model.



(a)



(b)

Figure 4.8: Junctionless DG MOSFET. Potential distribution in the middle of the channel: (a) from source to drain ($\phi_c(x_m)$) and (b) from gate to gate. Parameters: $N_d = 10^{19}\,\mathrm{cm}^{-3}$, $V_{gs} = -0.8\,\mathrm{V}$ to $0.1\,\mathrm{V}$, stepping $0.1\,\mathrm{V}$, $V_{ds} = 1\,\mathrm{V}$, $L_g = 100\,\mathrm{nm}$, $L_{sd} = 10\,\mathrm{nm}$, $T_{ch} = 10\,\mathrm{nm}$, $T_{ox} = 2\,\mathrm{nm}$. Lines TCAD; Symbols model.

When plotting ϕ_s and ϕ_c against the gate voltage V_{gs} (Fig. 4.9) both potentials are parallel to each other until V_{gs} increases above some gate voltage. Then the potentials start to converge, whereby at some higher gate bias a point of intersection between both (flat-band condition) will occur. This effect is strongly dependent on the channel's doping concentration. Note that, in the long-channel case the potential in the middle of the channel is not affected by 2-D effects.

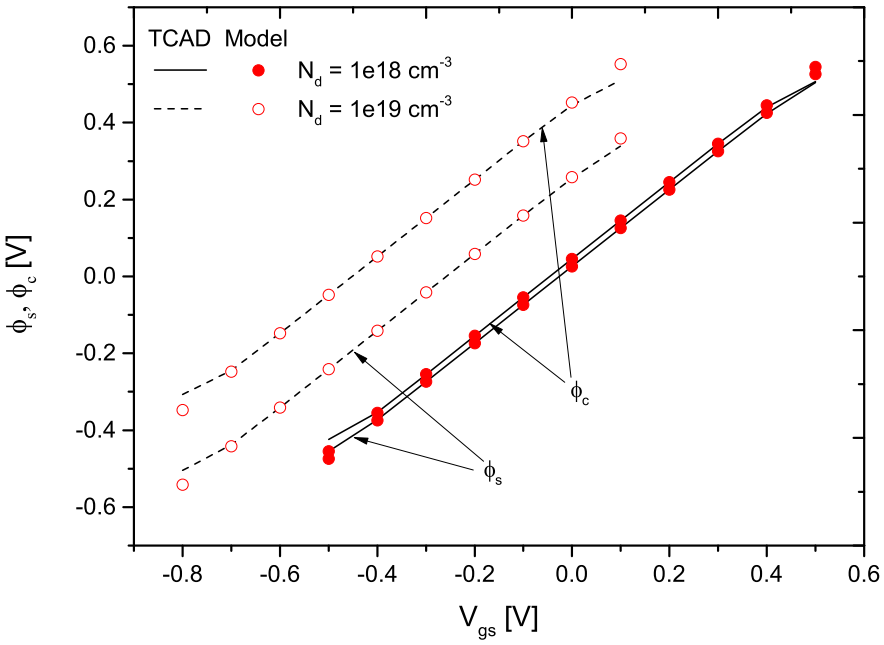
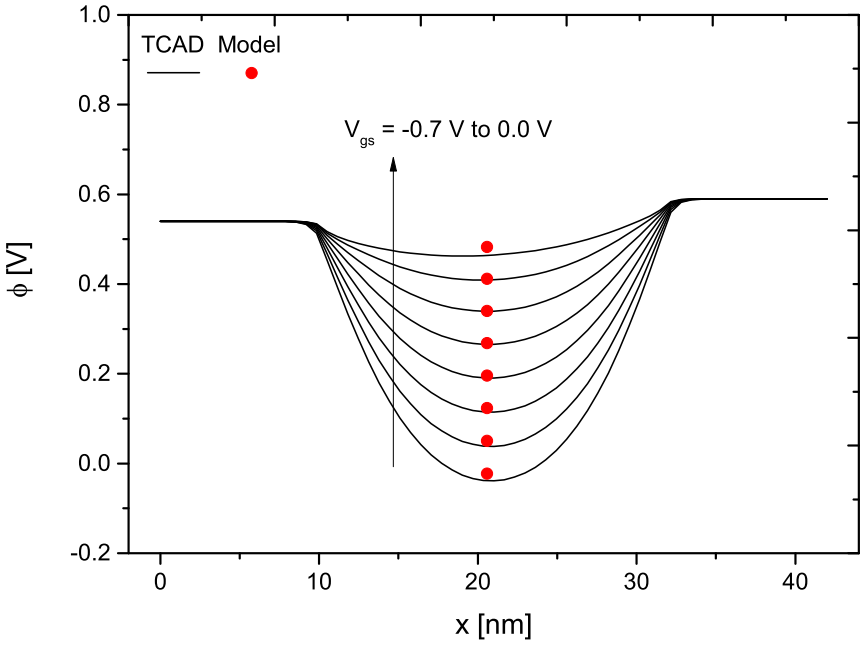


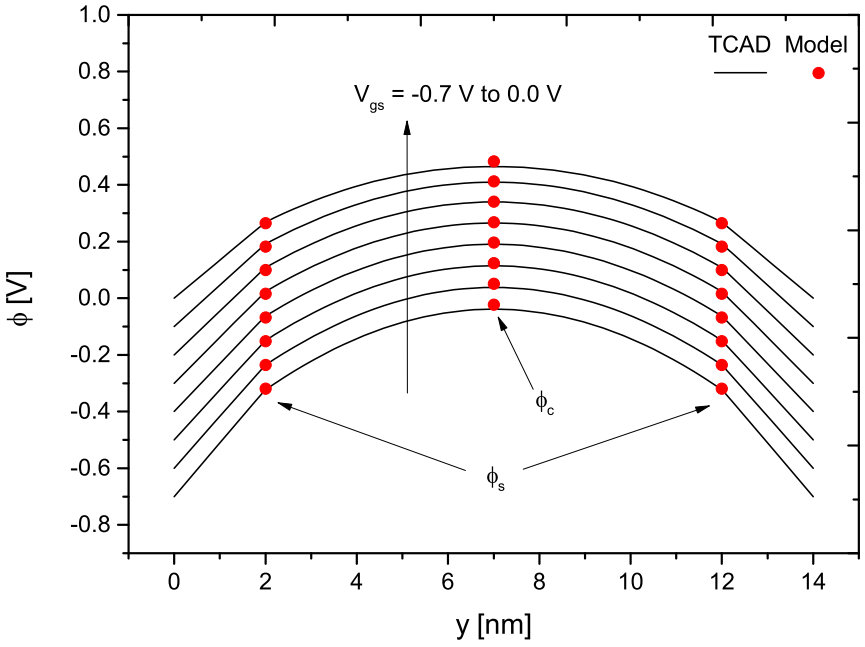
Figure 4.9: Junctionless DG MOSFET. 2-D potentials ϕ_s and ϕ_c at $L_g = 100\,\text{nm}$ with $N_d = 10^{18}\,\text{cm}^{-3}$ and $10^{19}\,\text{cm}^{-3}$ versus gate voltage. All other parameters are given in Fig. 4.8.

By decreasing L_g down to 22 nm, the potential in the middle of the channel is visibly affected by SCEs (Fig. 4.10), which are correctly predicted by the model. In part (a), at low $V_{ds} = 0.05\,\text{V}$, the position of the minimum potential remains almost unchanged as in the long-channel case. From (b) it can be observed that both the surface and center potentials are well predicted from the depletion to the weak accumulation region. Also, as mentioned before, the assumption of a linear potential drop inside the oxide regions is proved to be correct.

It can be noticed that, at high $V_{ds} = 1\,\text{V}$, the position of the potential minimum is shifted towards the source end of the device's channel, as the gate voltage increases (Fig. 4.11(a)). This behavior is due to the increased electrostatic influence of the drain region onto the channel region. The model agrees very well with the 2-D simulation data over a wide gate voltage range, enabling us to extract the potentials ϕ_s and ϕ_c from Fig. 4.11(b) in order to investigate their behavior when plotted against the gate voltage.

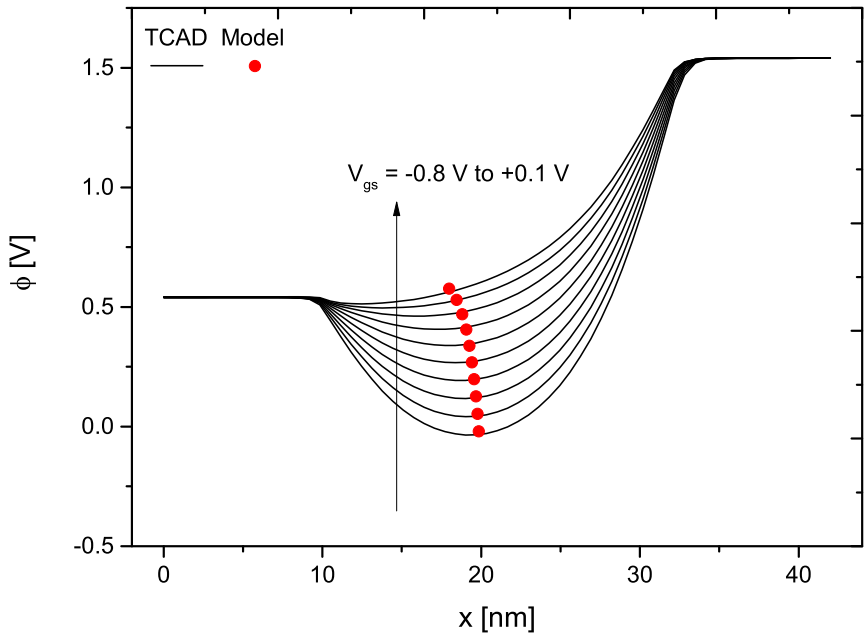


(a)

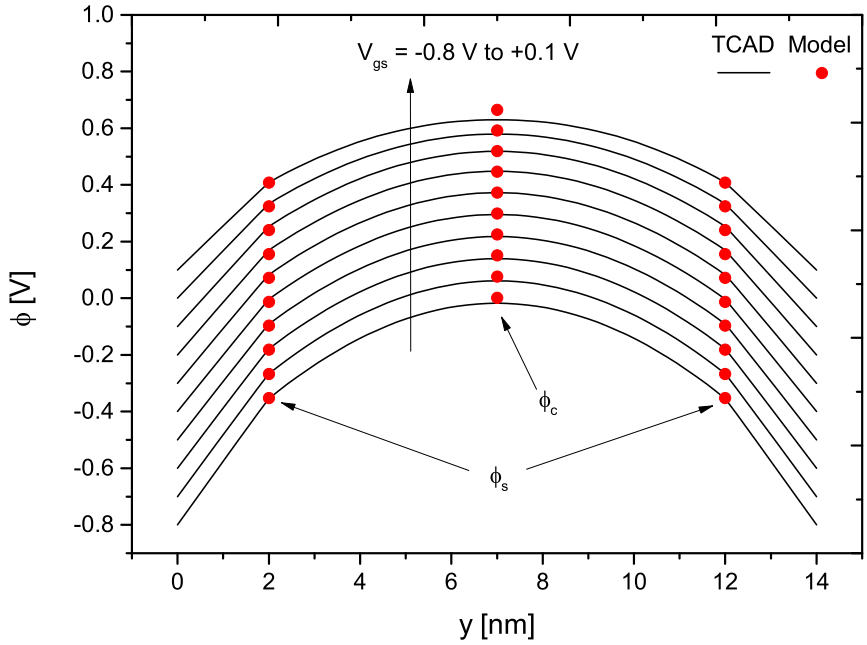


(b)

Figure 4.10: Junctionless DG MOSFET. Potential distribution in the middle of the channel: (a) from source to drain ($\phi_c(x_m)$) and (b) from gate to gate. Parameters: $N_d = 10^{19}\,\mathrm{cm}^{-3}$, $V_{gs} = -0.7\,\mathrm{V}$ to $0.0\,\mathrm{V}$, stepping $0.1\,\mathrm{V}$, $V_{ds} = 0.05\,\mathrm{V}$, $L_g = 22\,\mathrm{nm}$, $L_{sd} = 10\,\mathrm{nm}$, $T_{ch} = 10\,\mathrm{nm}$, $T_{ox} = 2\,\mathrm{nm}$. Lines TCAD; Symbols model.



(a)



(b)

Figure 4.11: Junctionless DG MOSFET. Potential distribution in the middle of the channel: (a) from source to drain ($\phi_c(x_m)$) and (b) from gate to gate. Parameters: $N_d = 10^{19}\,\mathrm{cm}^{-3}$, $V_{gs} = -0.8\,\mathrm{V}$ to $0.1\,\mathrm{V}$, stepping $0.1\,\mathrm{V}$, $V_{ds} = 1\,\mathrm{V}$, $L_g = 22\,\mathrm{nm}$, $L_{sd} = 10\,\mathrm{nm}$, $T_{ch} = 10\,\mathrm{nm}$, $T_{ox} = 2\,\mathrm{nm}$. Lines TCAD; Symbols model.

In Fig. 4.12, with increasing gate biases, the potential starts to saturate. If V_{gs} is increased beyond a certain voltage, flat-band condition is reached (as in the long-channel case), whereby a point of intersection between ϕ_s and ϕ_c will occur. Another important observation is that the difference between the ϕ_s and ϕ_c increases with N_d, because of the stronger band bending in the higher doped case.

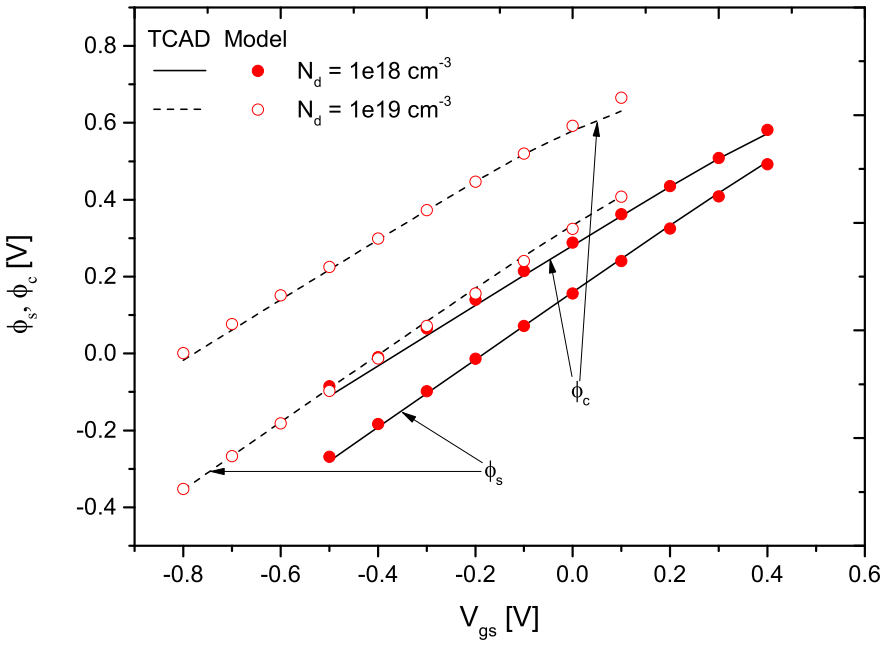
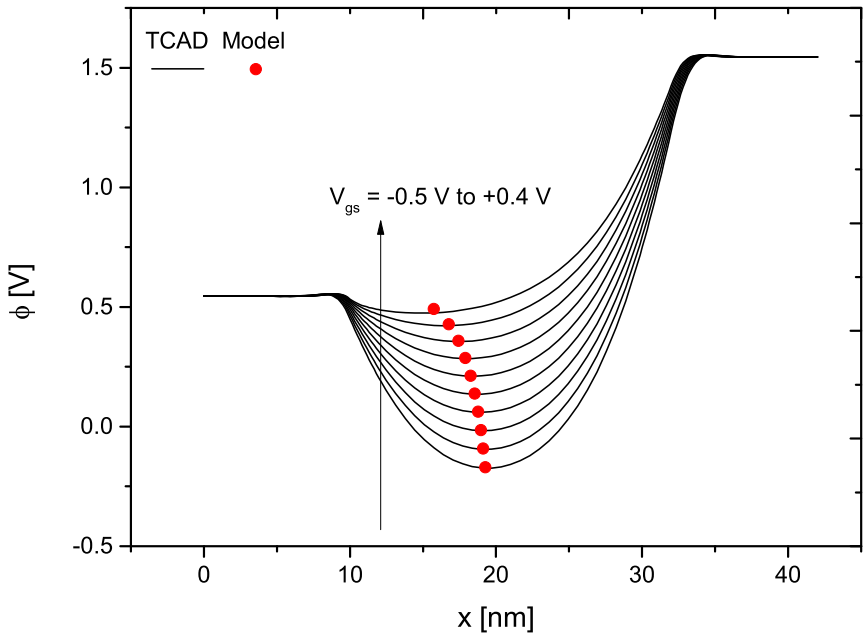


Figure 4.12: Junctionless DG MOSFET. 2-D potentials ϕ_s and ϕ_c at $L_g = 22\,\text{nm}$ with $N_d = 10^{18}\,\text{cm}^{-3}$ and $10^{19}\,\text{cm}^{-3}$ versus gate voltage. All other parameters are given in Fig. 4.11.

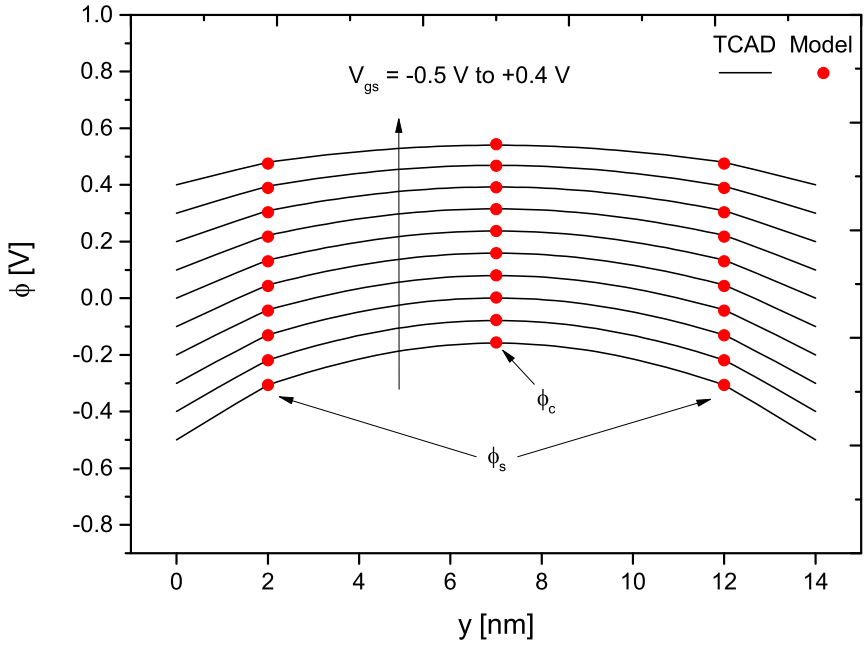
4.3.2 2-D Potential of Inversion Mode DG MOSFETs

In this section the results of the 2-D potentials are shown for the inversion mode DG MOSFET. The focus is directly on the short-channel devices, because a long-channel model verification was already performed for junctionless devices. Figure 4.13(a) illustrates the potential distribution in the middle of the channel from source to drain and Fig. 4.13(b) from gate to gate. The considered devices are lightly doped with $N_a = 10^{15}\,\text{cm}^{-3}$. The 2-D effects are correctly predicted over a wide gate voltage range, validating the correctness of the analytical compact model. The surface and center potentials match very well the TCAD data.

The same device is investigated in Fig. 4.14(a, b), considering a highly doped channel region with $N_a = 10^{18}\,\text{cm}^{-3}$. The model correctly takes into account the effect of body doping and reproduces the device's electrostatic behavior well. The position of the potential barrier inside the channel region and its related center potential is well predicted. This ensures a correct modeling of the electrical device parameters, such as threshold voltage and subthreshold slope.

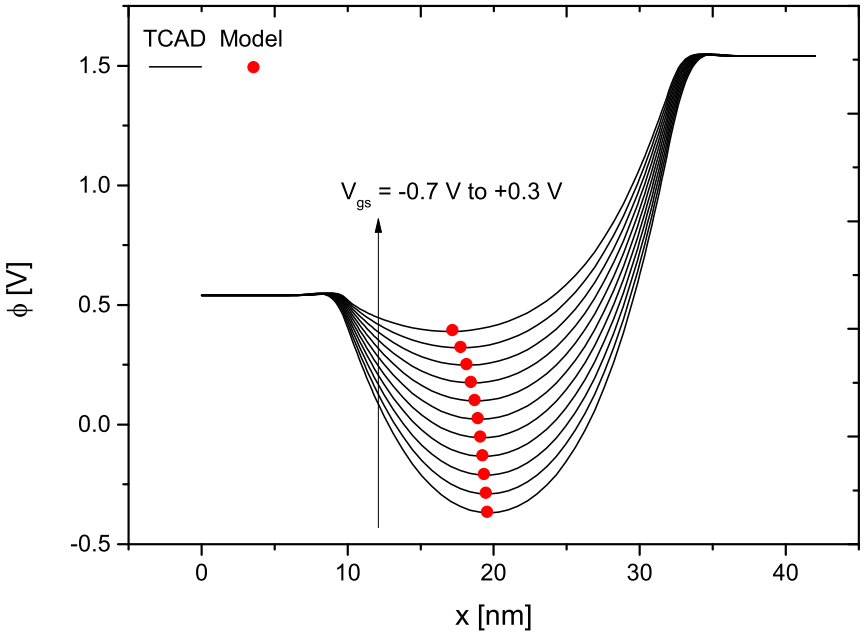


(a)

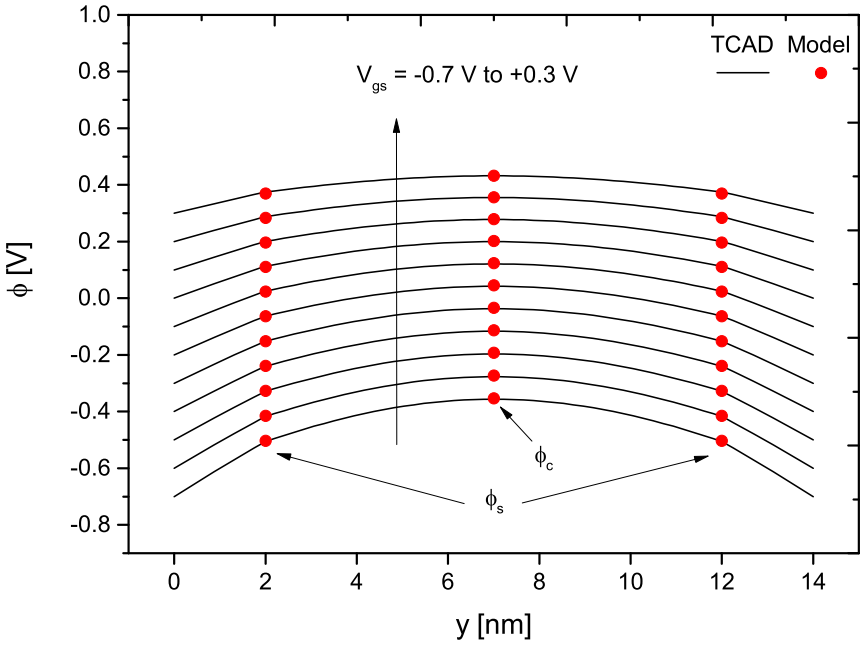


(b)

Figure 4.13: Inversion mode DG MOSFET. Potential distribution in the middle of the channel: (a) from source to drain ($\phi_c(x_m)$) and (b) from gate to gate. Parameters: $N_a = 10^{15}\,\mathrm{cm}^{-3}$, $V_{gs} = -0.5\,\mathrm{V}$ to $0.4\,\mathrm{V}$, stepping $0.1\,\mathrm{V}$, $V_{ds} = 1\,\mathrm{V}$, $L_g = 22\,\mathrm{nm}$, $L_{sd} = 10\,\mathrm{nm}$, $T_{ch} = 10\,\mathrm{nm}$, $T_{ox} = 2\,\mathrm{nm}$. Lines TCAD; Symbols model.



(a)



(b)

Figure 4.14: Inversion mode DG MOSFET. Potential distribution in the middle of the channel: (a) from source to drain ($\phi_c(x_m)$) and (b) from gate to gate. Parameters: $N_a = 10^{18}\,\mathrm{cm}^{-3}$, $V_{gs} = -0.7\,\mathrm{V}$ to $0.3\,\mathrm{V}$, stepping $0.1\,\mathrm{V}$, $V_{ds} = 1\,\mathrm{V}$, $L_g = 22\,\mathrm{nm}$, $L_{sd} = 10\,\mathrm{nm}$, $T_{ch} = 10\,\mathrm{nm}$, $T_{ox} = 2\,\mathrm{nm}$. Lines TCAD; Symbols model.

An interesting observation can be done by plotting ϕ_s and ϕ_c of both devices versus the gate voltage V_{gs} (see Fig. 4.15). In contrast to the junctionless device, the IM MOSFET's surface and center potential decreases with an increasing channel doping concentration. That means, increasing N_a will reduce the maximum output current I_{ds} of the IM device, due to increased scattering mechanisms inside the channel region and the resulting reduced carrier mobility.

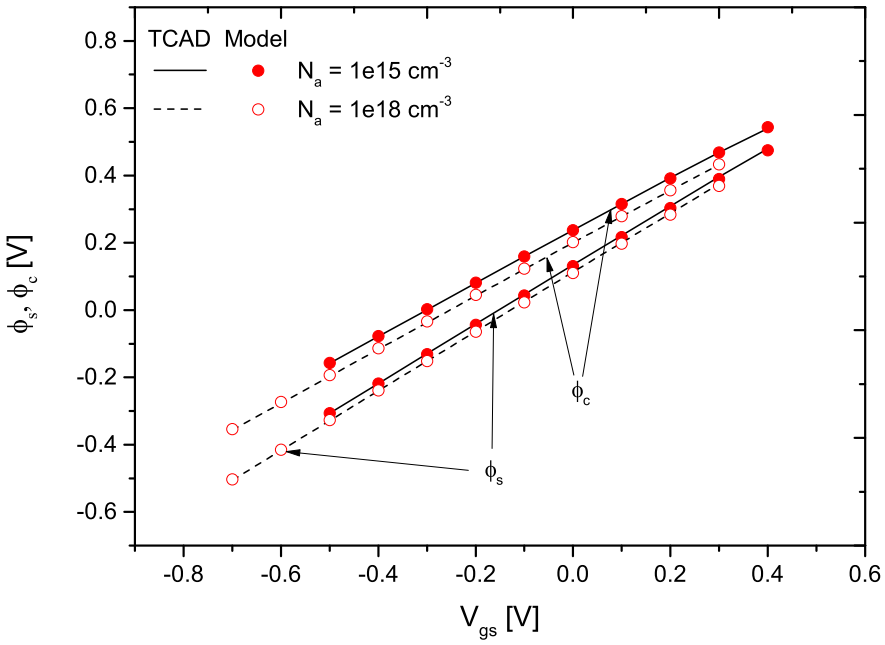


Figure 4.15: Inversion mode DG MOSFET. 2-D potentials ϕ_s and ϕ_c at $L_g = 22\,\text{nm}$ with $N_a = 10^{15}\,\text{cm}^{-3}$ and $10^{18}\,\text{cm}^{-3}$ versus gate voltage. All other parameters are given in Fig. 4.14.

4.4 Electrical Model Parameters

This section intends to explain how the electrical model parameters are derived and verified. The parameters addressed are the threshold voltage V_T, the drain-induced barrier lowering (DIBL) and the subthreshold slope S. Beside their derivation, an intensive verification versus TCAD simulation data is performed. Important effects are worked out and discussed.

4.4.1 Threshold Voltage

Threshold voltage models, for instance for junctionless transistors, with different device structures (i.e. nanowire FETs, and DG MOSFETs) were proposed in [87, 94, 99]. All of them assume a channel length of 200 nm up to 1μm. By using the approach below, it is possible to calculate V_T for long- and short-channel devices with L_g down to 22 nm.

The threshold voltage V_T is defined as the gate bias at which the value of a minimum potential $\phi(V_g^*)$ equals the value of the potential ϕ_T (Fig. 4.16) [127]. Or in other words, threshold voltage occurs at that point where the mobile charge density equals the fixed charge density.The position of the minimum potential x_m inside the channel region is calculated by equation (4.27). The potential called ϕ_T is approximated by:

$$\phi_T \approx V_{th} \ln\left(\frac{N_{a/d}}{n_i}\right). \tag{4.57}$$

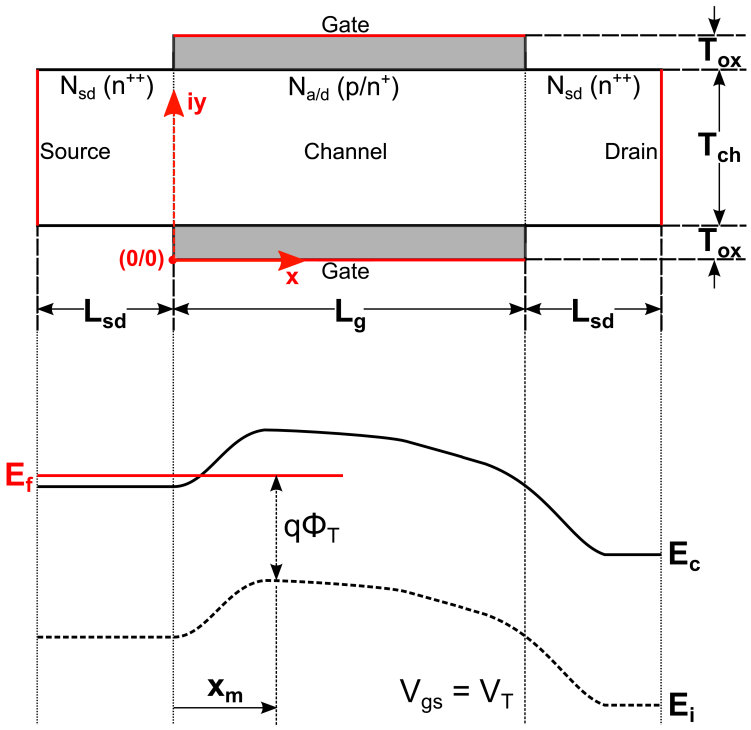


Figure 4.16: The upper figure shows the longitudinal cross-section of a DG device including its doping profile. The band diagram from source to drain at threshold voltage is schematically drawn below, whereby the parameter ϕ_T is defined as the difference between the Fermi level E_f in source region and intrinsic level E_i at the potential barrier x_m inside the channel region.

It should be noted that the Fermi level E_f in source region lies above the conduction band E_c due to the very high doping concentration ($N_{sd} = 10^{20}\,\mathrm{cm}^{-3}$), which leads to a degenerate semiconductor [22]. The difference between both (E_f and E_c) is 0.03 eV, whereby this value was found and extracted from TCAD simulations. Assuming a linear relation between $\phi(V_{gs})$ and the voltage V_{gs} in subthreshold region, the threshold voltage V_T is obtained trough extrapolating to higher gate biases [27]. The expression for the threshold voltage is derived from Fig. 4.17 in terms of the applied gate bias V_{gs}, the potential ϕ_T and $\phi(V_{gs})$ [127].

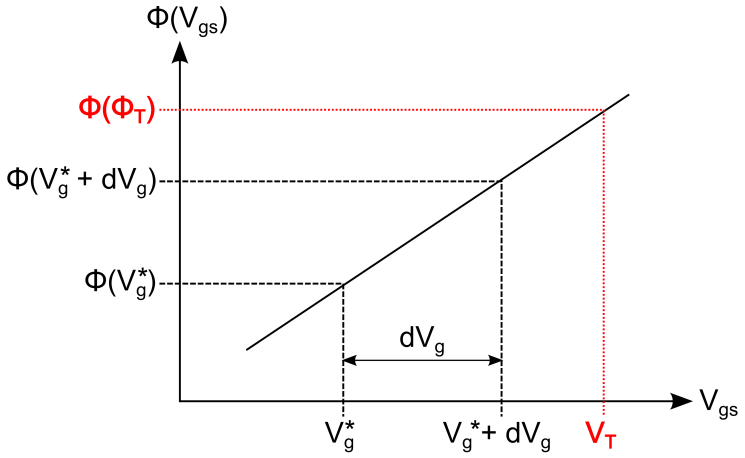


Figure 4.17: The threshold voltage is defined as $V_{gs} = V_T$ at $\phi(\phi_T) = \phi(V_{gs})$, with dV_g as the voltage difference between the two chosen gate voltages.

Since the main conduction mechanism of an IM MOSFET relies on a surface current, V_T is defined in terms of the 2-D surface potential ϕ_s. In contrast, the main conduction mechanism in JL MOSFETs relies on a bulk current, wherefore V_T is defined in terms of the 2-D center potential ϕ_c. For the implementation dV_g is set to 0.01 V. It was experimentally found that, if the value of dV_g is too large, the accuracy for the calculation of V_T decreases. V_g^* is a given gate-source voltage in the subthreshold regime.

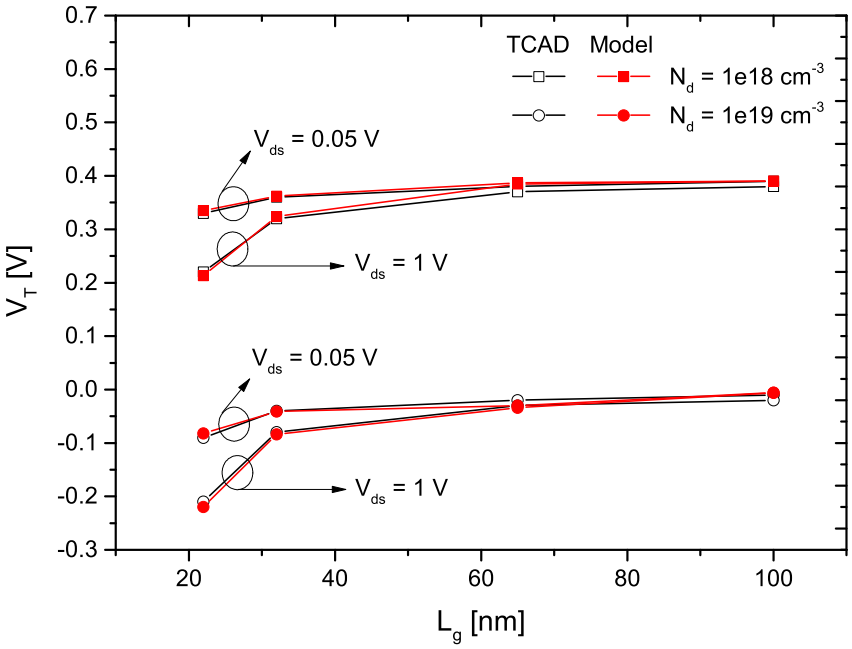
$$V_{T(JL/IM)} = V_g^* + dV_g \left(\frac{\phi_T - \phi_{(c/s)}(V_g^*)}{\phi_{(c/s)}(V_g^* + dV_g) - \phi_{(c/s)}(V_g^*)} \right) \tag{4.58}$$

Threshold Voltage Verification - Junctionless DG MOSFET

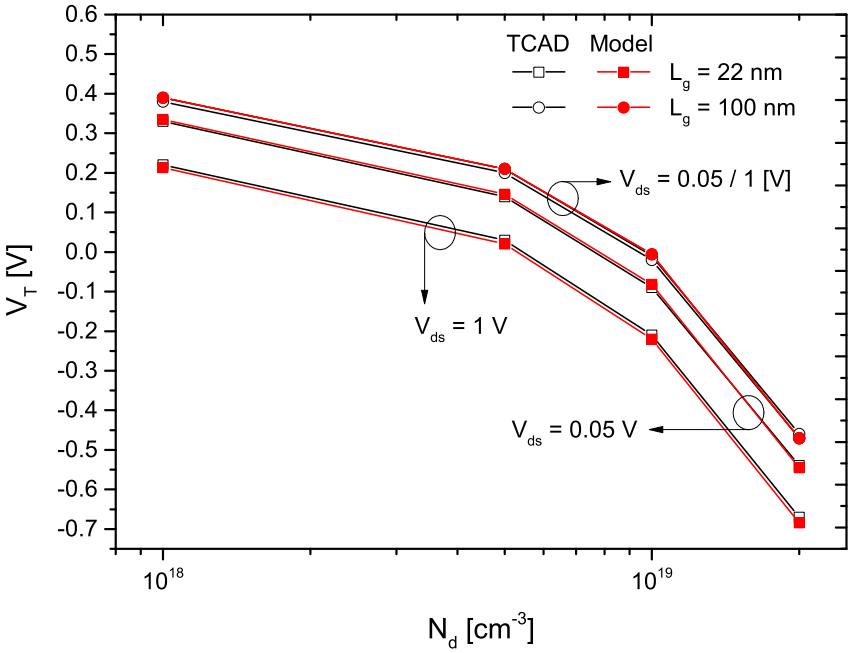
In the following, the results for the modeled threshold voltage are presented. The model is compared versus TCAD simulations, whereby the threshold voltage from TCAD was extracted by using the constant current method at matched $I_{off} = 100\,\text{nA}$. All other TCAD simulation setups are described in section 4.3.

$$V_{T,TCAD} = V_{gs}|_{I_{ds}=I_{off}\cdot\frac{W_{ch}}{L_g}} \tag{4.59}$$

From Fig. 4.18(a) one can see that the threshold voltage model is in good agreement with the 2-D simulation data. It is clearly shown that the threshold voltage is strongly influenced by the device's channel length. As expected V_T decreases with L_g. This effect is even more pronounced at high V_{ds}, due to the reduced potential barrier at source, which results in an increased injection of electrons into the channel region and therefore gives higher currents. Another effect is, that the threshold voltage decreases with an increasing doping concentration.



(a)



(b)

Figure 4.18: Junctionless DG MOSFET. (a) Threshold voltage V_T versus channel length L_g. (b) V_T versus doping concentration N_d. Parameters: $N_d = 1 \cdot 10^{18}\,\mathrm{cm}^{-3}$ to $2 \cdot 10^{19}\,\mathrm{cm}^{-3}$, $V_{ds} = 0.05\,/\,1\,[\mathrm{V}]$, $L_g = 22\,\mathrm{nm}$ to $100\,\mathrm{nm}$, $L_{sd} = 10\,\mathrm{nm}$, $T_{ch} = 10\,\mathrm{nm}$, $T_{ox} = 2\,\mathrm{nm}$.

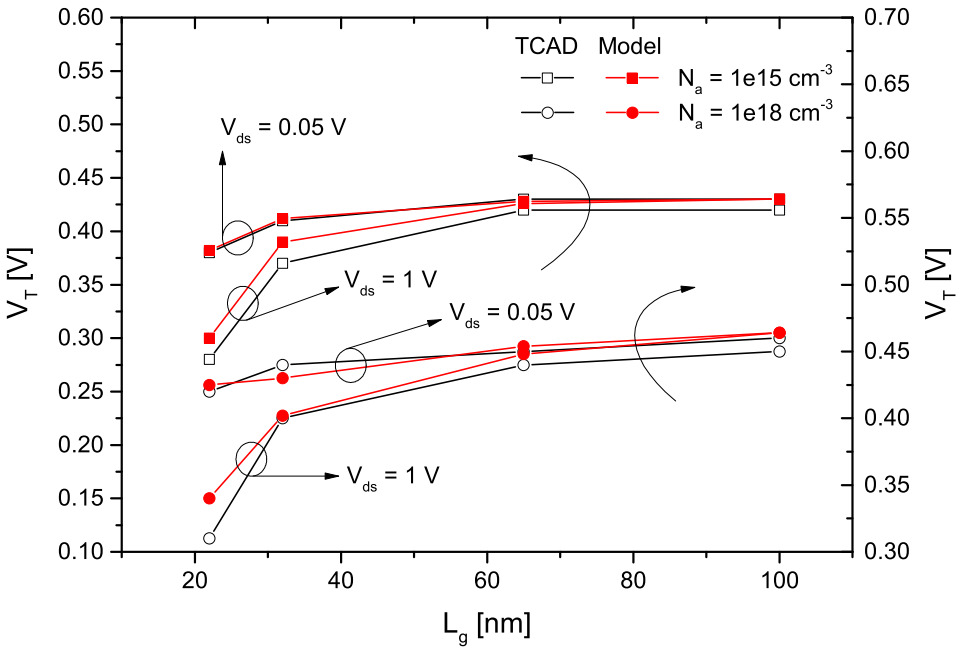
Investigating the V_T for different doping concentrations (Fig. 4.18(b)) shows that V_T is strongly degraded for doping concentrations exceeding $N_d = 1 \cdot 10^{19}$ cm^{-3}. This effect was also shown in [88]. To achieve suitable positive threshold voltages for such highly doped devices, a gate material ($p+$ poly-Si) with a very high work function is needed [32]. At a channel length about 22 nm and drain voltage of 1 V, the threshold voltage drops to $V_T \approx -0.7$ V. Under the same conditions, $V_T \approx -0.5$ V for a device with a channel length about 100 nm. When $L_g = 100$ nm, an increasing drain voltage has less influence on V_T than in the case of $L_g = 22$ nm. All calculated and simulated threshold voltages are summarized in Table 4.4.

L_g [nm]	N_d [cm^{-3}]	$V_{T,Model}$ [V]	$V_{T,TCAD}$ [V]
22	$1 \cdot 10^{18}$	0.335 / 0.213	0.33 / 0.22
22	$5 \cdot 10^{18}$	0.146 / 0.020	0.14 / 0.03
22	$1 \cdot 10^{19}$	-0.082 / -0.220	-0.09 / -0.21
22	$2 \cdot 10^{19}$	-0.545 / -0.684	-0.54 / -0.67
32	$1 \cdot 10^{18}$	0.362 / 0.324	0.36 / 0.32
32	$1 \cdot 10^{19}$	-0.041 / -0.084	-0.04 / -0.08
65	$1 \cdot 10^{18}$	0.387 / 0.385	0.38 / 0.37
65	$1 \cdot 10^{19}$	-0.032 / -0.034	-0.02 / -0.03
100	$1 \cdot 10^{18}$	0.390 / 0.390	0.39 / 0.39
100	$5 \cdot 10^{18}$	0.210 / 0.210	0.21 / 0.20
100	$1 \cdot 10^{19}$	-0.006 / -0.006	-0.01 / -0.02
100	$2 \cdot 10^{19}$	-0.471 / -0.471	-0.46 / -0.47

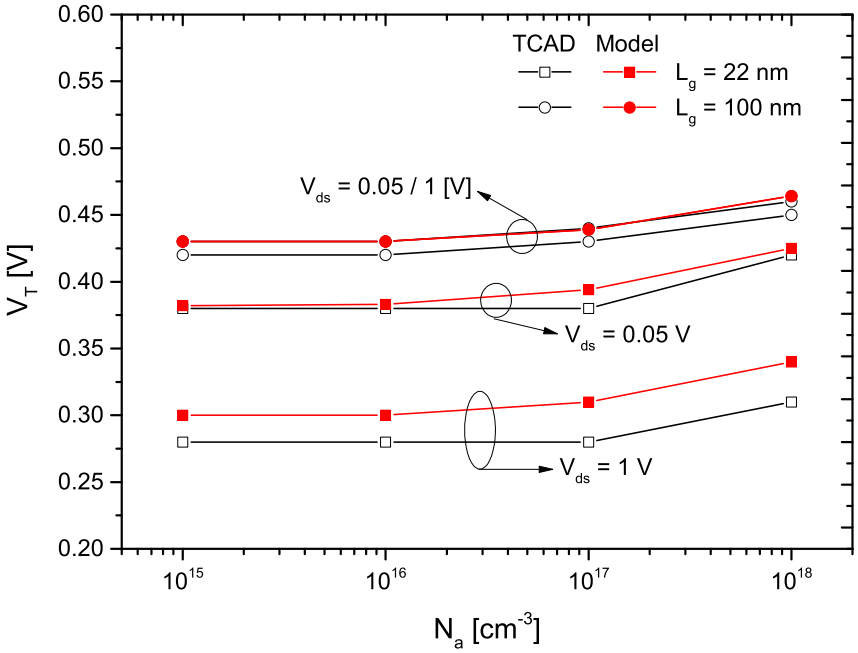
Table 4.4: Calculated and simulated threshold voltage extracted from Fig. 4.18. With V_T at $V_{ds} = 0.05 \,/\, 1$ [V].

Threshold Voltage Verification - Inversion Mode DG MOSFET

The IM devices show a different behavior of V_T when plotted against L_g (Fig. 4.19(a)). V_T decreases with L_g, whereby this effect is even stronger with an increasing V_{ds}. However, contrary to junctionless devices, the threshold voltage is less, almost not, affected by altering channel doping concentrations N_a (it must be noted that two ordinates are used to display the results for V_T). Investigating the threshold voltage detailed versus the channel doping concentration N_a (Fig. 4.19(b)) it becomes apparent that, the effect of an altering N_a on V_T is negligible. Even when increasing N_a from an lightly doped channel region ($N_a = 1 \cdot 10^{15}$ cm^{-3}) to highly doped ($N_a = 1 \cdot 10^{18}$ cm^{-3}), the threshold voltage does not vary much. The difference in V_T at $L_g = 100$ nm and $L_g = 22$ nm with $V_{ds} = 1$ V is then around 0.03 V. All threshold voltages are finally summarized in Table 4.5.



(a)



(b)

Figure 4.19: Inversion mode DG MOSFET. (a) Threshold voltage V_T versus channel length L_g. (b) V_T versus doping concentration N_a. Parameters: $N_a = 1 \cdot 10^{15}\,\mathrm{cm}^{-3}$ to $1 \cdot 10^{18}\,\mathrm{cm}^{-3}$, $V_{ds} = 0.05\,/\,1\,[\mathrm{V}]$, $L_g = 22\,\mathrm{nm}$ to $100\,\mathrm{nm}$, $L_{sd} = 10\,\mathrm{nm}$, $T_{ch} = 10\,\mathrm{nm}$, $T_{ox} = 2\,\mathrm{nm}$.

L_g [nm]	N_a [cm^{-3}]	$V_{T,Model}$ [V]	$V_{T,TCAD}$ [V]
22	$1 \cdot 10^{15}$	0.382 / 0.300	0.38 / 0.28
22	$1 \cdot 10^{16}$	0.382 / 0.300	0.38 / 0.28
22	$1 \cdot 10^{17}$	0.394 / 0.310	0.39 / 0.28
22	$1 \cdot 10^{18}$	0.412 / 0.340	0.40 / 0.31
32	$1 \cdot 10^{15}$	0.412 / 0.390	0.41 / 0.37
32	$1 \cdot 10^{18}$	0.430 / 0.402	0.44 / 0.40
65	$1 \cdot 10^{15}$	0.428 / 0.426	0.43 / 0.42
65	$1 \cdot 10^{18}$	0.454 / 0.448	0.45 / 0.44
100	$1 \cdot 10^{15}$	0.430 / 0.430	0.43 / 0.42
100	$1 \cdot 10^{16}$	0.430 / 0.430	0.43 / 0.43
100	$1 \cdot 10^{17}$	0.439 / 0.439	0.44 / 0.43
100	$1 \cdot 10^{18}$	0.464 / 0.464	0.46 / 0.45

Table 4.5: Calculated and simulated threshold voltage extracted from Fig. 4.19. With V_T at $V_{ds} = 0.05 \,/\, 1$ [V].

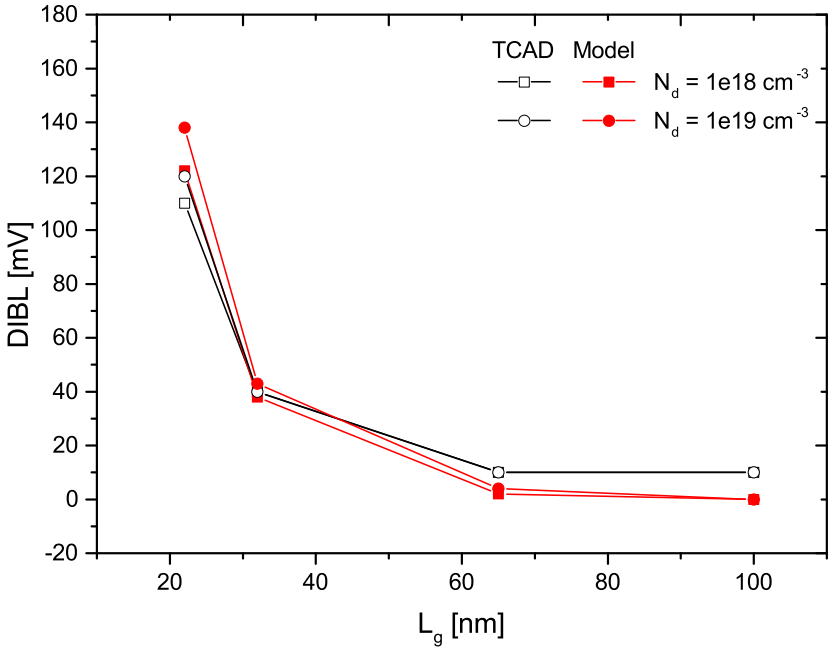
4.4.2 Drain-Induced Barrier Lowering

The drain-induced barrier lowering effect is defined in terms of a threshold voltage shift. By using the calculated and simulated values of the threshold voltage of both device types, namely the inversion mode and the junctionless DG MOSFET, it is possible to investigate the device's electrostatic behavior in the subthreshold region.

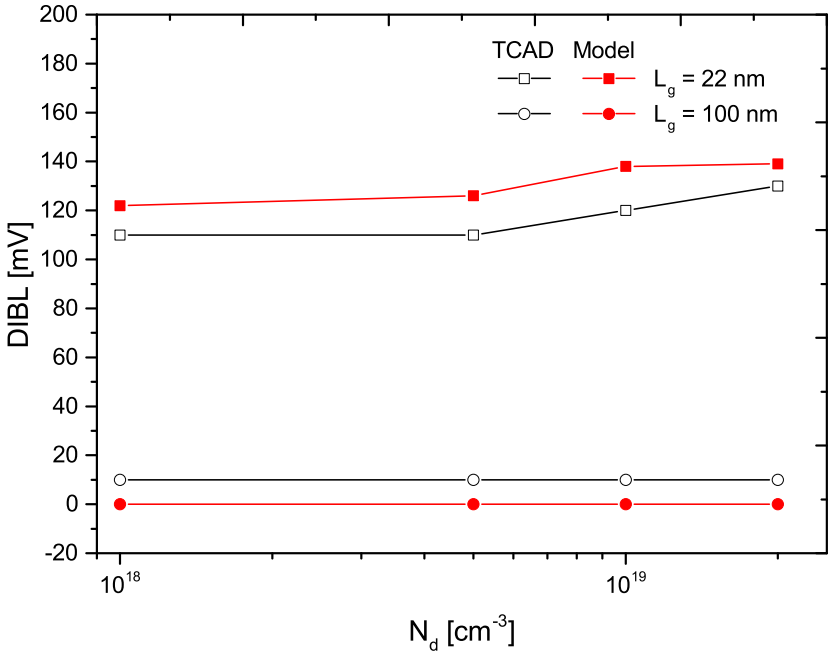
$$\mathrm{DIBL} = V_T|_{V_{ds}=0.05\,\mathrm{V}} - V_T|_{V_{ds}=1\,\mathrm{V}} \tag{4.60}$$

DIBL Verification - Junctionless DG MOSFET

From Fig. 4.20 one can see that the calculated DIBL is in good agreement with the simulation data. The results prove that the DIBL increases with a decreasing channel length (Fig. 4.20(a)). Since the difference in DIBL, at a channel length of 22 nm, between a doping concentration about $N_d = 1 \cdot 10^{18}$ cm^{-3} and $N_d = 1 \cdot 10^{19}$ cm^{-3} is relatively small (i.e. 0.017 V), one can estimate that an increasing doping concentration has less influence towards the DIBL than a decreasing channel length [127]. A prove of this estimation can be found from Fig. 4.20(b). One can see that the DIBL does not change (approximately 1 mV) at $L_g = 100$ nm and a doping concentration varying from $N_d = 1 \cdot 10^{18}$ cm^{-3} to $N_d = 2 \cdot 10^{19}$ cm^{-3}. This behavior in DIBL is due to the device's long-channel nature. By scaling the channel length down to 22 nm, using the same range for the doping concentration, the DIBL starts to vary slightly up to values about 15 mV, whereby the DIBL increases continuously with the doping concentration. This behavior was also shown in [115].



(a)



(b)

Figure 4.20: Junctionless DG MOSFET. (a) Behavior of DIBL versus channel length L_g, which is varied from 22 nm to 100 nm. (b) DIBL versus doping concentration N_d, altered from $N_d = 1 \cdot 10^{18}$ cm^{-3} to $N_d = 2 \cdot 10^{19}$ cm^{-3}. Parameters: $V_{ds} = 0.05\,/\,1$ [V], $L_{sd} = 10$ nm, $T_{ch} = 10$ nm, $T_{ox} = 2$ nm.

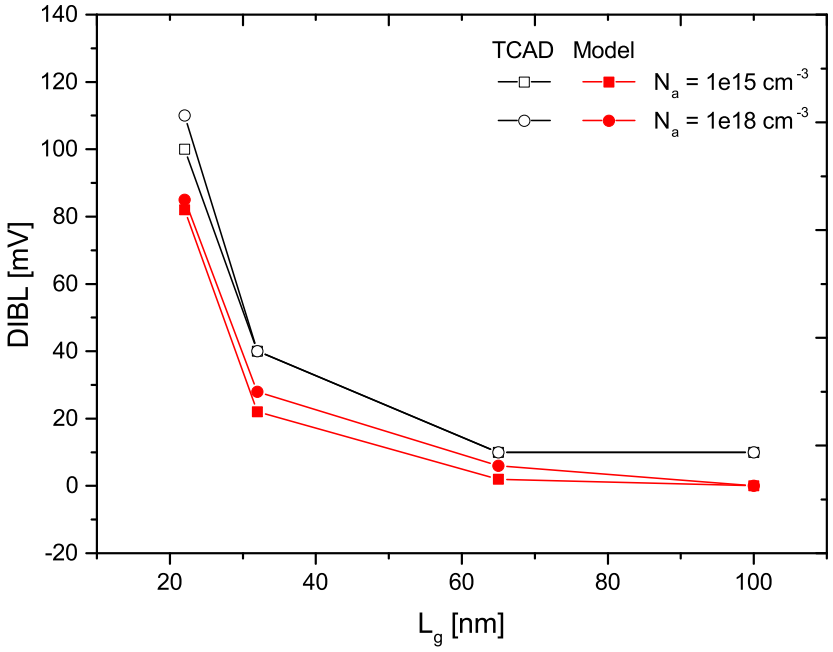
The investigation of the DIBL, especially at short-channel sizes, is therefore an important task in order to prevent operational failures in such devices due to the SCEs [127]. Table 4.6 summarizes the calculated and simulated values for the DIBL of the junctionless DG MOSFET.

L_g [nm]	N_d [cm^{-3}]	$DIBL_{Model}$ [mV]	$DIBL_{TCAD}$ [mV]
22	$1 \cdot 10^{18}$	122	110
22	$5 \cdot 10^{18}$	126	110
22	$1 \cdot 10^{19}$	138	120
22	$2 \cdot 10^{19}$	139	130
32	$1 \cdot 10^{18}$	38	40
32	$1 \cdot 10^{19}$	43	40
65	$1 \cdot 10^{18}$	2	10
65	$1 \cdot 10^{19}$	4	10
100	$1 \cdot 10^{18}$	0	10
100	$5 \cdot 10^{18}$	0	10
100	$1 \cdot 10^{19}$	0	10
100	$2 \cdot 10^{19}$	0	10

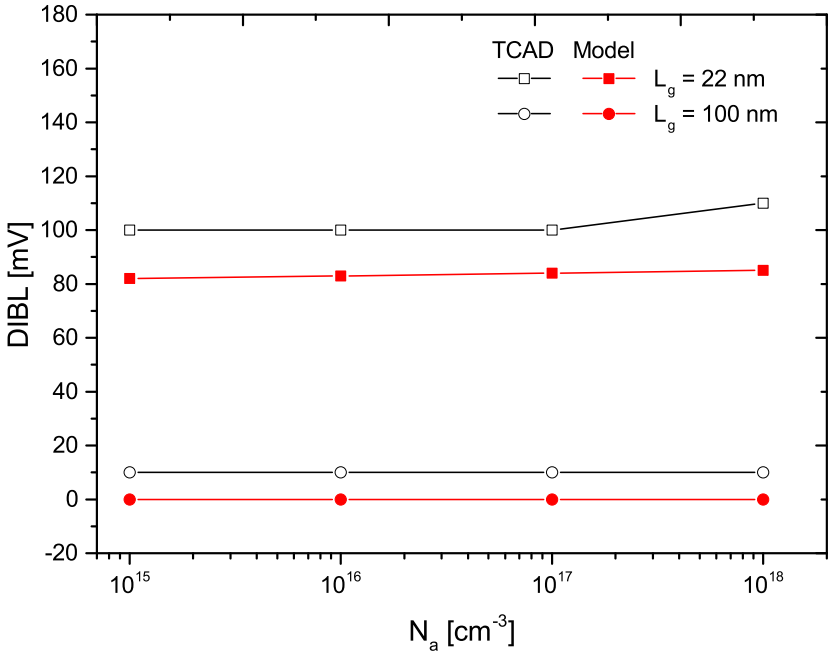
Table 4.6: Calculated and simulated DIBL extracted from Fig. 4.20.

DIBL Verification - Inversion Mode DG MOSFET

A close observation of the DIBL in inversion mode DG MOSFETs shows, that its subthreshold characteristics are slightly better than in the previously discussed junctionless device (see Fig. 4.21). In (a) the DIBL is plotted versus the channel length. The model matches well the TCAD data, whereby it slightly underestimates the DIBL (mV range). The DIBL increases with decreasing L_g, whereby an altering N_a has only a minor influence. In (b) the results are shown for DIBL versus N_a. As mentioned, the DIBL is almost not affected when the channel doping concentration is increased from lightly to highly doped values ($N_a = 1 \cdot 10^{15}$ cm^{-3} to $N_a = 1 \cdot 10^{18}$ cm^{-3}). Even by shrinking the channel length down to 22 nm, the DIBL remains nearly unchanged. The difference is around 10 mV over the entire range of N_a. Table 4.7 summarizes the corresponding calculated and simulated values.



(a)



(b)

Figure 4.21: Inversion mode DG MOSFET. (a) Behavior of DIBL versus channel length L_g, which is varied from 22 nm to 100 nm. (b) DIBL versus doping concentration N_a, altered from $N_a = 1 \cdot 10^{15}$ cm^{-3} to $N_a = 1 \cdot 10^{18}$ cm^{-3}. Parameters: $V_{ds} = 0.05\,/\,1$ [V], $L_{sd} = 10$ nm, $T_{ch} = 10$ nm, $T_{ox} = 2$ nm.

L_g [nm]	N_a [cm^{-3}]	$DIBL_{Model}$ [mV]	$DIBL_{TCAD}$ [mV]
22	$1 \cdot 10^{15}$	82	100
22	$1 \cdot 10^{16}$	83	100
22	$1 \cdot 10^{17}$	84	100
22	$1 \cdot 10^{18}$	85	110
32	$1 \cdot 10^{15}$	22	40
32	$1 \cdot 10^{18}$	28	40
65	$1 \cdot 10^{15}$	2	10
65	$1 \cdot 10^{18}$	6	10
100	$1 \cdot 10^{15}$	0	10
100	$1 \cdot 10^{16}$	0	10
100	$1 \cdot 10^{17}$	0	10
100	$1 \cdot 10^{18}$	0	10

Table 4.7: Calculated and simulated DIBL extracted from Fig. 4.21.

4.4.3 Subthreshold Slope

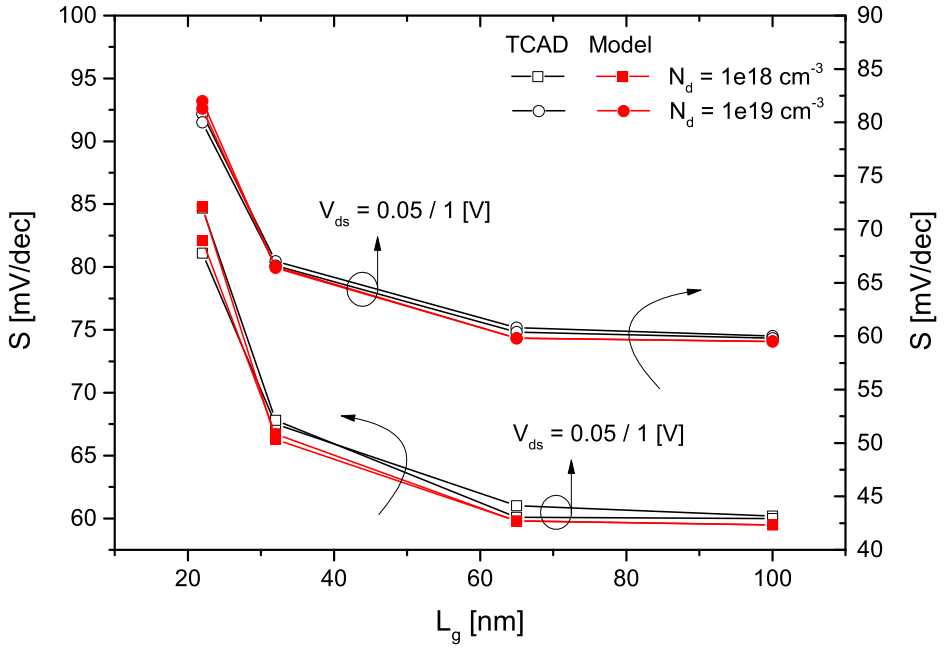
The 2-D subthreshold slope S is modeled by the expressions presented in [27] and [139]. S is expressed in terms of the surface or the center potential, depending on the device type, at two distinct gate biases ((V_g^*) and ($V_g^* + dV_g$)). Again, dV_g is set to 0.01 V (compare with section 4.4.1).

$$S_{(JL/IM)} = V_{th}\ \ln(10) \cdot \left(\frac{dV_g}{\phi_{(c/s)}(V_g^* + dV_g) - \phi_{(c/s)}(V_g^*)} \right), \tag{4.61}$$

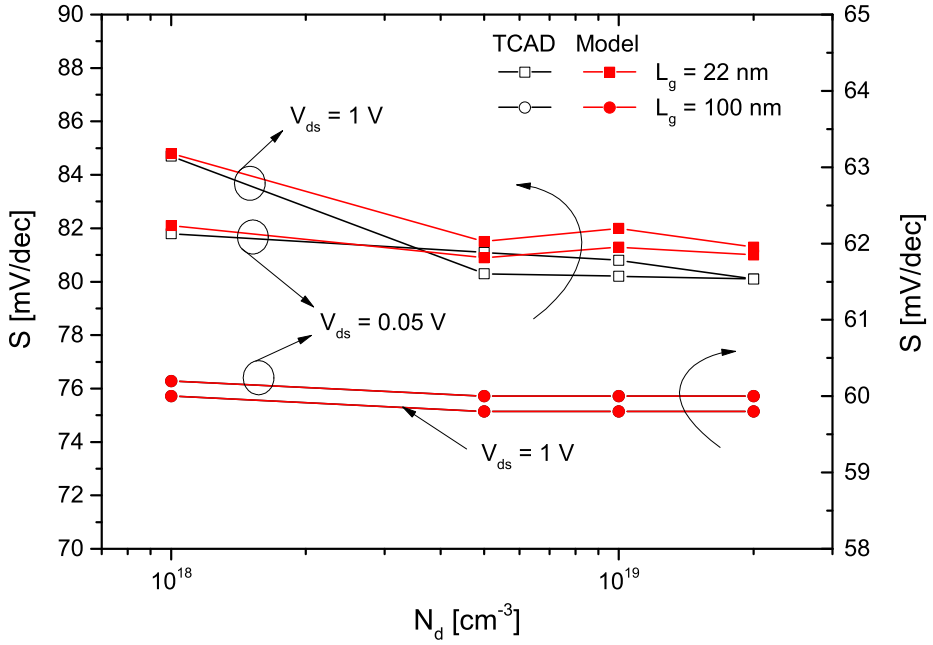
where $V_{th} = k\,T/q$ is the thermal voltage. From equation (4.61) one can see that the accuracy of the modeled potentials is essential, in order to correctly predict the subthreshold slope.

Subthreshold Slope Verification - Junctionless DG MOSFET

To validate the predictive ability of the model Fig. 4.22(a) (it must be noted that two ordinates are used to display the results for S) and Fig. 4.22(b) show the subthreshold slope S as a function of channel length and doping concentration, respectively. The close proximity of the source/drain depletion regions, at short-channel sizes, reduces the ability of the gate electrode to sufficiently control the channel region, thus worsening the subthreshold slope. Here, the SCEs on S are well covered by the model. Additionally, it is found that S does not differ much between low and high drain biases. The change in S when the channel doping concentration is varied is negligible, as confirmed by Fig. 4.22(b). Table 4.8 summarizes the calculated and simulated values for S of the junctionless DG MOSFET.



(a)



(b)

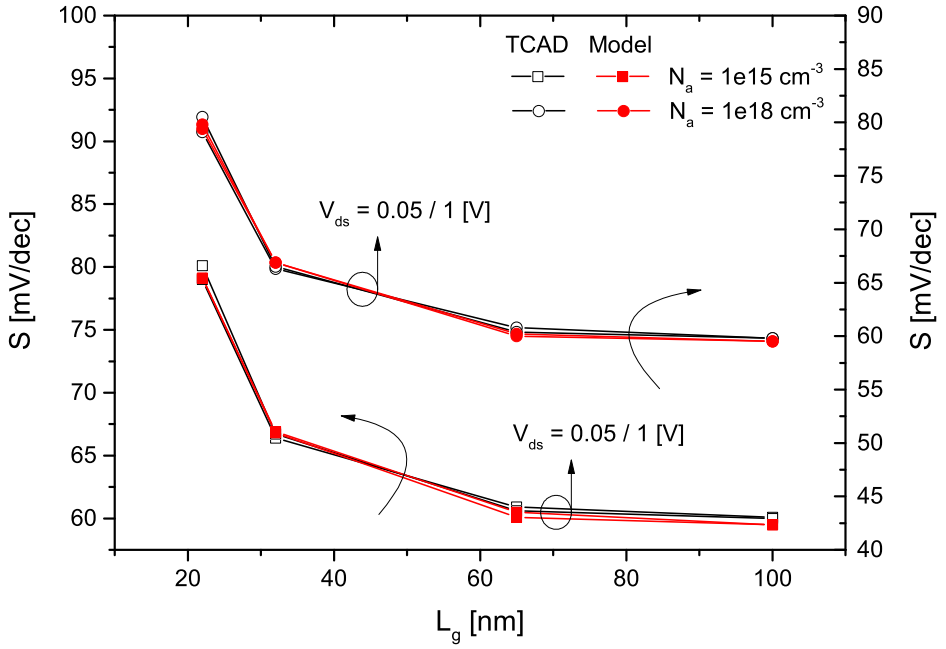
Figure 4.22: Junctionless DG MOSFET. (a) Behavior of S versus channel length L_g, which is varied from 22 nm to 100 nm. (b) S versus doping concentration N_d, altered from $N_d = 1 \cdot 10^{18}$ cm^{-3} to $N_d = 2 \cdot 10^{19}$ cm^{-3}. Parameters: $V_{ds} = 0.05\,/\,1$ [V], $L_{sd} = 10$ nm, $T_{ch} = 10$ nm, $T_{ox} = 2$ nm.

L_g [nm]	N_d [$\mathrm{cm^{-3}}$]	S_{Model} [mV/dec]	S_{TCAD} [mV/dec]
22	$1 \cdot 10^{18}$	82.1 / 84.8	81.8 / 84.7
22	$5 \cdot 10^{18}$	80.9 / 81.5	81.1 / 80.3
22	$1 \cdot 10^{19}$	81.3 / 82.0	80.8 / 80.2
22	$2 \cdot 10^{19}$	81.0 / 81.3	80.1 / 80.1
32	$1 \cdot 10^{18}$	66.7 / 66.3	67.5 / 67.8
32	$1 \cdot 10^{19}$	66.5 / 66.4	67.0 / 66.6
65	$1 \cdot 10^{18}$	59.8 / 59.8	61.0 / 60.1
65	$1 \cdot 10^{19}$	59.8 / 59.8	60.8 / 60.4
100	$1 \cdot 10^{18}$	59.5 / 59.5	60.2 / 60.0
100	$5 \cdot 10^{18}$	59.5 / 59.5	60.0 / 59.8
100	$1 \cdot 10^{19}$	59.5 / 59.5	60.0 / 59.8
100	$2 \cdot 10^{19}$	59.5 / 59.5	60.0 / 59.8

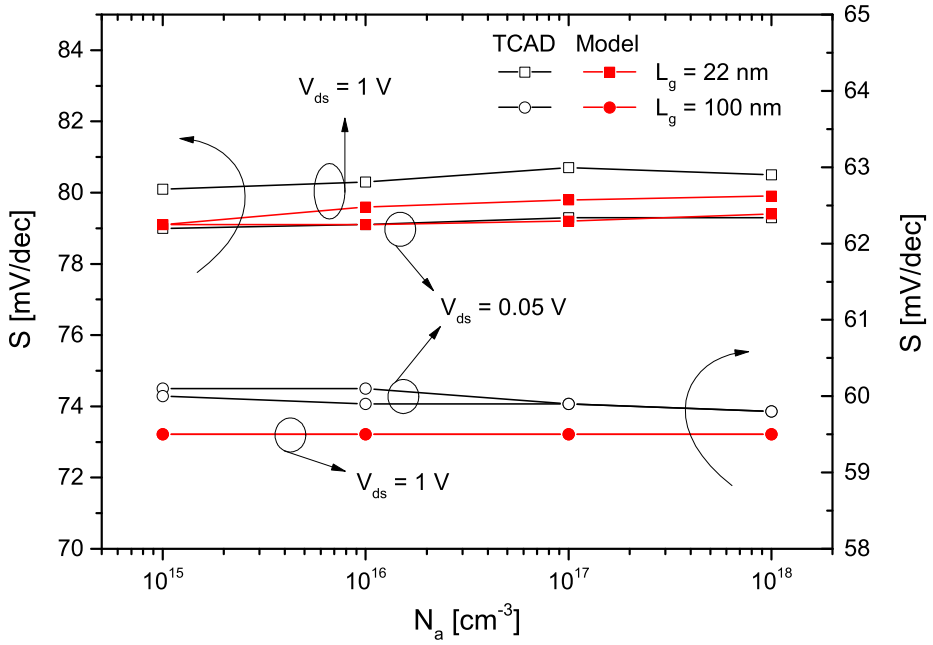
Table 4.8: Calculated and simulated values of the subthreshold slope extracted from Fig. 4.22. With S at $V_{ds} = 0.05 \,/\, 1\,[\mathrm{V}]$.

Subthreshold Slope Verification - Inversion Mode DG MOSFET

When plotting the subthreshold slope S as a function of the channel length L_g one can see that the subthreshold slope worsens with a shortening L_g (see Fig. 4.23(a)). S decreases from a nearly ideal value of $S \approx 60\,\mathrm{mV/dec}$ at $L_g = 100\,\mathrm{nm}$ to $S \approx 80\,\mathrm{mV/dec}$ at $L_g = 22\,\mathrm{nm}$. Only a minor change in S can be observed when the channel doping concentration is increased from $1 \cdot 10^{15}\,\mathrm{cm^{-3}}$ to $1 \cdot 10^{18}\,\mathrm{cm^{-3}}$. From Fig. 4.23(b) it becomes clear that increasing N_a does not affect the device's subthreshold slope. Even highly doped channels show almost the same value for S as do the lightly doped ones. On the other hand, a shortening channel length strongly affects the device's subthreshold characteristics, due to SCEs. For a better overview, all calculated and simulated values of the subthreshold slope of the inversion mode DG MOSFET are summarized in Table 4.9.



(a)



(b)

Figure 4.23: Inversion mode DG MOSFET. (a) Behavior of S versus channel length L_g, which is varied from 22 nm to 100 nm. (b) S versus doping concentration N_a, altered from $N_a = 1 \cdot 10^{15}$ cm^{-3} to $N_a = 1 \cdot 10^{18}$ cm^{-3}. Parameters: $V_{ds} = 0.05\,/\,1$ [V], $L_{sd} = 10$ nm, $T_{ch} = 10$ nm, $T_{ox} = 2$ nm.

L_g [nm]	N_a [cm^{-3}]	S_{Model} [mV/dec]	S_{TCAD} [mV/dec]
22	$1 \cdot 10^{15}$	79.1 / 79.1	79.0 / 80.1
22	$1 \cdot 10^{16}$	79.1 / 79.6	79.1 / 80.3
22	$1 \cdot 10^{17}$	79.2 / 79.8	79.3 / 80.7
22	$1 \cdot 10^{18}$	79.4 / 79.8	79.3 / 80.5
32	$1 \cdot 10^{15}$	66.9 / 66.8	66.4 / 66.7
32	$1 \cdot 10^{18}$	66.9 / 66.9	66.3 / 66.5
65	$1 \cdot 10^{15}$	60.5 / 60.1	60.9 / 60.6
65	$1 \cdot 10^{18}$	60.2 / 60.0	60.8 / 60.4
100	$1 \cdot 10^{15}$	59.5 / 59.5	60.1 / 60.0
100	$1 \cdot 10^{16}$	59.5 / 59.5	60.1 / 59.9
100	$1 \cdot 10^{17}$	59.5 / 59.5	59.9 / 59.9
100	$1 \cdot 10^{18}$	59.5 / 59.5	59.8 / 59.8

Table 4.9: Calculated and simulated values of the subthreshold slope extracted from Fig. 4.23. With S at $V_{ds} = 0.05 \,/\, 1$ [V].

4.5 Unified Charge Density Model

First of all, let's recall that the current in JL MOSFETs differs between depletion and in accumulation mode, which corresponds to volume and surface conduction, respectively. Therefore, each mode has its own effective gate capacitance - C_{eff} and C_{ox}, respectively [86]. The effective gate capacitance (per unit area) is then given as:

$$C_{eff,JL} = (1/C_{ox} + 1/C_{dep})^{-1}, \tag{4.62}$$

with $C_{dep} = (4\,\varepsilon_{Si}/T_{ch})$ as the depletion capacitance (per unit area). If an IM MOSFET is considered, the effective gate capacitance simply equals the oxide capacitance.

$$C_{eff,IM} = C_{ox}. \tag{4.63}$$

In the following, the charge density model is derived for the case of a JL device, whereby it is also applicable for IM MOSFETs if the sign of the depletion charge is reversed accordingly (compare with section 4.1.1).

To realize a smooth transition between the depletion and the accumulation regime the

functions V_{g1} and V_{g2} are introduced [27].

$$V_{g1} = V_{fit} + \left(\frac{\ln\left(1 + \exp\left(C_1\left(V_g' - V_{fit}\right)\right)\right)}{\ln\left(1 + \exp(C_1)\right)} \right) \tag{4.64}$$

$$V_{g2} = V_g' - V_{g1} + V_{fit}, \tag{4.65}$$

where V_{fit} is the voltage at which the transition between both operating regimes occurs and

$$C_1 = \frac{\ln(10)}{2\,S}. \tag{4.66}$$

Below V_{fit} on x-axis (Fig. 4.24), V_{g1} takes the value of V_{fit} and above it increases to $V_{gs,max}$. On the opposite side, V_{g2} takes the value of V_{fit} above V_{fit} on x-axis and below it decreases to $V_{gs,min}$. By applying these smoothing functions continuity at flat-band condition is guaranteed [140].

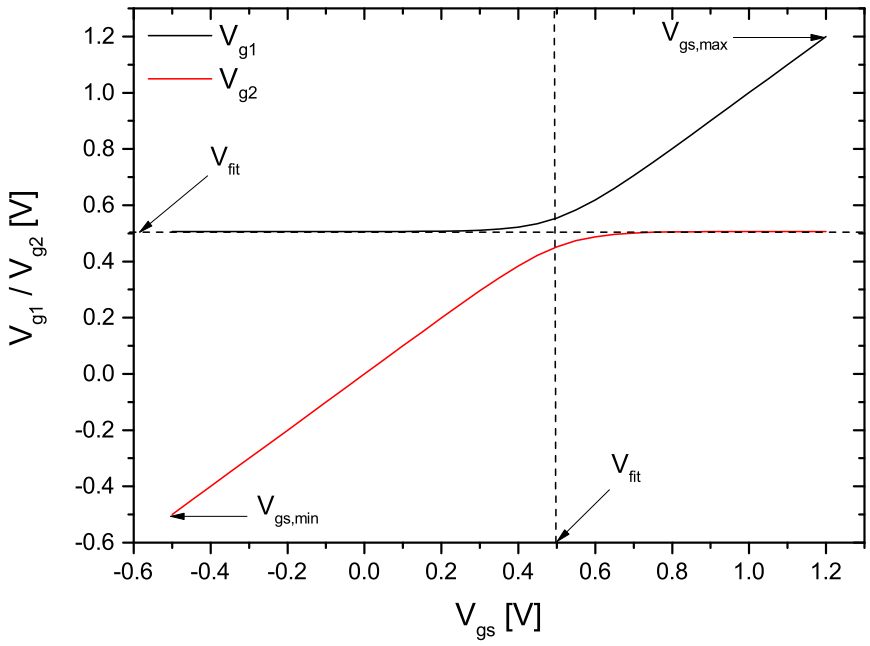


Figure 4.24: Illustration of the smoothing functions V_{g1} and V_{g2}.

So far, V_{fit} is treated as an adjustable parameter which depends on the doping concentration N_d within the channel region, the device's gate length L_g and the drain voltage V_{ds}. Besides, V_{fit} does not change much when considering small channel thicknesses (around 10 nm) and doping concentrations up to $N_d = 10^{19}\,\mathrm{cm}^{-3}$, but remains close to the value of V_T and therefore requires only minor adjustments. In the case of inversion mode transistors V_{fit} is set to infinity, since only surface conduction is considered and the bulk current is of minor importance.

By assuming that only the charge carriers, which are able to overcome the potential barrier inside the device's channel region contribute to the total current I_{ds}, the integral mobile charge $Q_{m,2D}$ (per unit area) - at the potential barrier (position x_m) at threshold voltage V_T - is derived by using Boltzmann statistics for a parabolic approximation of the potential profile within a double-gate device [27]. Here, the discrete 2-D solutions for the surface and center potential ϕ_s and ϕ_c, respectively, are inherently included in the calculations for the charges.

$$Q_{m,2D}(V_T) = q\, n_i \cdot f_{Q_{m,2D}} \cdot \exp\left(\frac{\phi_s(V_T)}{V_{th}}\right) \tag{4.67}$$

$$f_{Q_{m,2D}} = \exp(g_{Q_{m,2D}}) \cdot \left(\frac{\sqrt{\pi}\, T_{ch}/2}{2\sqrt{g_{Q_{m,2D}}}}\right) \cdot \operatorname{erf}\left\{\sqrt{g_{Q_{m,2D}}}\right\} \tag{4.68}$$

$$g_{Q_{m,2D}} = \operatorname{abs}\left(\frac{\phi_c(V_T) - \phi_s(V_T)}{V_{th}}\right) \tag{4.69}$$

In the next step, the derivation of the 1-D mobile charge is addressed. By assuming volume conduction and without considering 2-D effects the 1-D mobile charge Q_m can be expressed as:

$$Q_m = q \int_{-T_{ch}/2}^{T_{ch}/2} n_i \cdot \exp\left(\frac{\phi_{avg}}{V_{th}}\right) dy = q\, n_i\, T_{ch} \cdot \exp\left(\frac{\phi_{avg}}{V_{th}}\right). \tag{4.70}$$

The potential ϕ_{avg} represents an average potential, which is assumed to be constant from gate to gate. Solving for $\partial Q_m/\partial\phi_{avg}$ then leads to:

$$\frac{\partial Q_m}{\partial \phi_{avg}} = \frac{q\, n_i\, T_{ch}}{V_{th}} \cdot \exp\left(\frac{\phi_{avg}}{V_{th}}\right) = \frac{Q_m}{V_{th}}. \tag{4.71}$$

By relating the charge per gate to the electric field strength in the oxide, 1-D Poisson's equation can be written in terms of 1-D mobile charge and fixed donor charge.

$$\frac{Q_m}{2} + \frac{Q_f}{2} = \frac{q\, n_i\, T_{ch}}{2} \cdot \exp\left(\frac{\phi_{avg}}{V_{th}}\right) + \left(-\frac{q\, N_d\, T_{ch}}{2}\right) = C_{ox}\, \left(V_g' - (\phi_{avg} - \phi_{fn})\right), \tag{4.72}$$

with ϕ_{fn} as the electron quasi-Fermi level (see section 4.5.1, Fig. 4.25).

$$\phi_{fn} = V_{th} \ln\left(\frac{N_d}{n_i}\right) \tag{4.73}$$

From Eq. (4.72) one obtains:

$$V_g = \left(\frac{q\, n_i\, T_{ch}}{2} \cdot \exp\left(\frac{\phi_{avg}}{V_{th}}\right) - \frac{q\, N_d\, T_{ch}}{2}\right) \frac{1}{C_{ox}} + V_{fb} + (\phi_{avg} - \phi_{fn}), \tag{4.74}$$

and

$$\frac{\partial V_g}{\partial \phi_{avg}} = \frac{q\, n_i\, T_{ch}}{2\, C_{ox}\, V_{th}} \cdot \exp\left(\frac{\phi_{avg}}{V_{th}}\right) + 1. \tag{4.75}$$

Solving for $\partial Q_m / \partial V_g$ with Eq. (4.71) and (4.75) yields:

$$\begin{aligned} \frac{\partial Q_m}{\partial V_g} &= \frac{\partial Q_m}{\partial \phi_{avg}} \cdot \frac{\partial \phi_{avg}}{\partial V_g} \\ &= \frac{Q_m}{V_{th}} \cdot \frac{1}{\frac{Q_m}{2\, C_{ox}\, V_{th}} + 1}. \end{aligned} \tag{4.76}$$

4.5.1 Charges in Depletion

For a better understanding, a detailed sketch of the corresponding band diagram, from gate to gate, of a JL DG n-MOSFET is given in Fig. 4.25. For $\phi_{avg} < \phi_{fn}$ in Eq. (4.72) the device operates in the depletion regime.

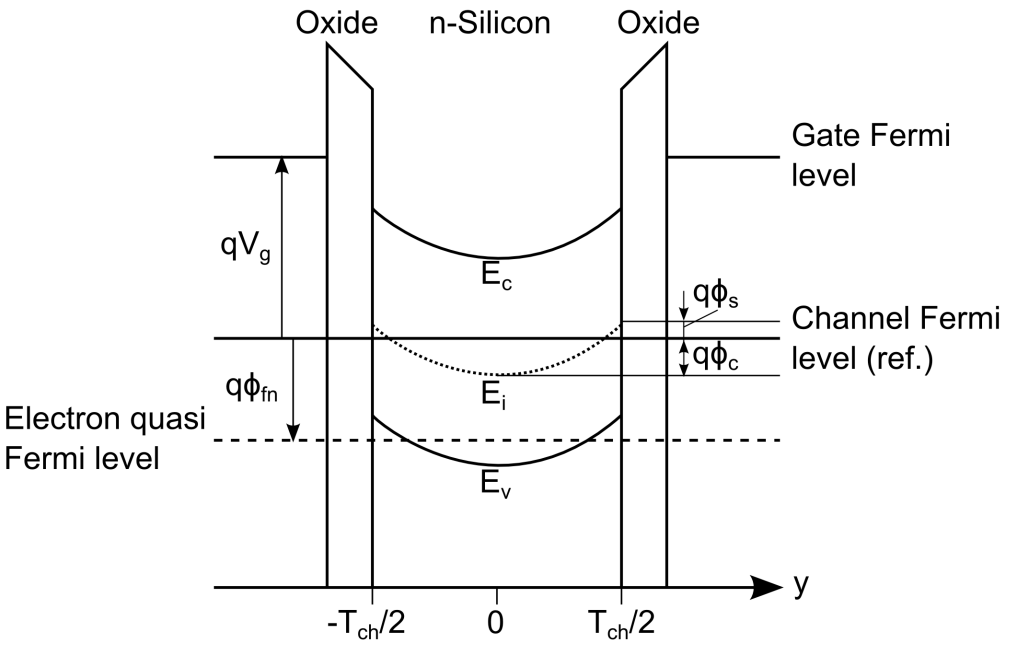


Figure 4.25: Sketch of the energy band diagram of the JL DG n-MOSFET in depletion region. The Fermi level in the channel is used as reference.

So far, Eq. (4.76) lacks of a proper description for subthreshold slope degradation due to SCEs. For that reason, an empirical modification in order to account for subthreshold slope degradation and volume conduction in that regime is introduced. This is the factor α and the effective gate capacitance C_{eff}, respectively [28, 86]. The effective gate capacitance C_{eff}

compensates for the non-constant potential profile in depletion, which was assumed in Eq. (4.70). The ratio α of the degraded slope and the ideal slope (slope degradation factor) is defined as:

$$\alpha = \frac{S}{S_{1D}} = \frac{S}{60\,\mathrm{mV/dec}}, \tag{4.77}$$

where S represents the subthreshold slope from Eq. (4.61), which includes the two-dimensional effects. Equation (4.76) then modifies to:

$$\frac{\partial Q_{m,dep}}{\partial V_{g,dep}} = \frac{Q_{m,dep}}{V_{th}} \cdot \frac{1}{\frac{Q_{m,dep}}{2\,C_{eff}\,V_{th}} + \alpha}, \tag{4.78}$$

with $Q_{m,dep}$ as the mobile charge in depletion region. By rearranging Eq. (4.78) for ∂V_g one gets:

$$\partial V_{g,dep} = \left(\frac{\alpha\, V_{th}}{Q_{m,dep}} + \frac{1}{2\,C_{eff}} \right) \partial Q_{m,dep}. \tag{4.79}$$

In order to include 2-D effects, the expression for the mobile charge at the potential barrier ($Q_{m,2D}(V_T)$) is introduced to the integral. The charges in depletion region are then obtained by integrating and solving for $Q_{m,dep}$ afterwards.

$$\int_{V_T}^{V_{g2}} dV_{g,dep} = \int_{Q_{m,2D}(V_T)}^{Q_{m,dep}} \left(\frac{\alpha\, V_{th}}{Q_{m,dep}} + \frac{1}{2\,C_{eff}} \right) dQ_{m,dep} \tag{4.80}$$

$$V_{g2} - V_T = \alpha\, V_{th} \ln\left(\frac{Q_{m,dep}}{Q_{m,2D}(V_T)} \right) + \frac{Q_{m,dep} - Q_{m,2D}(V_T)}{2\,C_{eff}} \tag{4.81}$$

To derive the expression for $Q_{m,dep}$, which incorporates 2-D effects, the first branch of Lambert's W-function $\mathcal{L}$ is applied to Eq. (4.81), leading to:

$$Q_{m,dep} = 2\,C_{eff}\,V_{th}\,\alpha \times \mathcal{L}\left(\frac{Q_{m,2D}(V_T) \cdot \exp\left(\frac{Q_{m,2D}(V_T) - 2\,C_{eff}\,(V_T - V_{g2})}{2\,C_{eff}\,V_{th}\,\alpha} \right)}{2\,C_{eff}\,V_{th}\,\alpha} \right). \tag{4.82}$$

4.5.2 Charges in Accumulation

The device operates in accumulation region if the potential ϕ_{avg} from Eq. (4.72) is larger than the electron quasi-Fermi potential ϕ_{fn} ($\phi_{avg} > \phi_{fn}$; see Fig. 4.26). To describe the charges in the accumulation regime the approach from Eq. (4.70) is used. The reason is that flat-band condition in JL devices occurs well above V_T, almost in the accumulation regime, making them easy to model. It is assumed that no SCEs are present in the accumulation region and that the current relies on surface conduction, which corresponds to the effective gate capacitance C_{ox}. These assumptions lead to the following modification of Eq. (4.76), where $Q_{m,acc,s}$ represents

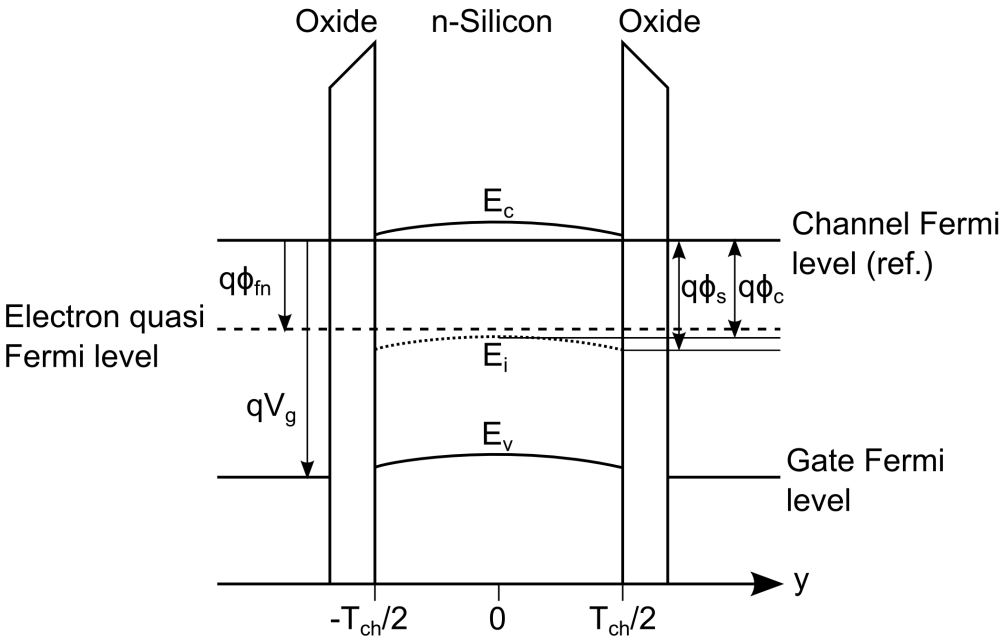


Figure 4.26: Sketch of the energy band diagram of the JL DG n-MOSFET in accumulation region. The Fermi level in the channel is used as reference.

the mobile charge in accumulation region at the source end of the channel.

$$\frac{\partial Q_{m,acc,s}}{\partial V_{g,acc}} = \frac{Q_{m,acc,s}}{V_{th}} \cdot \frac{1}{\frac{Q_{m,acc,s}}{2\,C_{ox}\,V_{th}} + 1}, \tag{4.83}$$

with

$$\partial V_{g,acc} = \left(\frac{V_{th}}{Q_{m,acc,s}} + \frac{1}{2\,C_{ox}} \right) \partial Q_{m,acc,s}. \tag{4.84}$$

$Q_{m,acc,s}$ is derived by using the following integral together with the smoothing function V_{g1} and $Q_{m,dep}(V_{fit})$.

$$\int_{V_{fit}}^{V_{g1}} dV_{g,acc} = \int_{Q_{m,dep}(V_{fit})}^{Q_{m,acc,s}} \left(\frac{V_{th}}{Q_{m,acc,s}} + \frac{1}{2\,C_{ox}} \right) dQ_{m,acc,s} \tag{4.85}$$

$$V_{g1} - V_{fit} = V_{th} \ln \left(\frac{Q_{m,acc,s}}{Q_{m,dep}(V_{fit})} \right) + \frac{Q_{m,acc,s} - Q_{m,dep}(V_{fit})}{2\,C_{ox}}. \tag{4.86}$$

Applying the first branch of Lambert's W-function $\mathcal{L}$ leads finally to:

$$Q_{m,acc,s} = 2\,C_{ox}\,V_{th}\;\times \mathcal{L}\left(\frac{Q_{m,dep}(V_{fit})\cdot\exp\left(\frac{Q_{m,dep}(V_{fit})-2\,C_{ox}\left(V_{g1}-V_{fit}\right)}{2\,C_{ox}\,V_{th}}\right)}{2\,C_{ox}\,V_{th}}\right). \tag{4.87}$$

The mobile charge in accumulation region at the drain end of the channel $Q_{m,acc,d}$ is then computed to:

$$Q_{m,acc,d} = Q_{m,acc,s} - \left(2\,C_{ox}\,\tilde{V}_{dss}\right), \tag{4.88}$$

where $\tilde{V}_{dss}$ represents a modified saturation voltage, which is used to smoothly limit V_{dss} to its lower bound $V_{dss,Q_{m,acc,s}}$ [28].

$$\tilde{V}_{dss} = V_{dss,Q_{m,acc,s}}\cdot\left[1-\frac{1}{B_1}\cdot\ln\left(1+\exp\left(A_1\cdot\left(1-\frac{V_{dss}}{V_{dss,Q_{m,acc,s}}}\right)\right)\right)\right], \tag{4.89}$$

with

$$B_1 = \ln\left(1+\exp(A_1)\right) \tag{4.90}$$

and

$$V_{dss,Q_{m,acc,s}} = \frac{Q_{m,acc,s}}{2C_{ox}}\cdot\left(1-\exp\left(-\frac{V_{ds}}{V_{th}}\right)\right). \tag{4.91}$$

The function V_{dss}, which smooths the linear to the saturation region is given by:

$$V_{dss} = V_{dsat}\cdot\left[1-\frac{1}{B_2}\cdot\ln\left(1+\exp\left(A_2\cdot\left(1-\frac{V_{ds}}{V_{th}}\right)\right)\right)\right], \tag{4.92}$$

where

$$B_2 = \ln\left(1+\exp(A_2)\right) \tag{4.93}$$

The parameters A_1 and A_2 are adjustable which range between 1 and 5. The equation of the saturation voltage is readily obtained from a standard text book [22]:

$$V_{dsat} = \frac{V_{g1}-V_T+L_gE_p}{E_p/E_{crit}-1}\cdot\left(\sqrt{1+\frac{2(V_{g1}-V_T)L_gE_p(E_p/E_{crit}-1)}{(V_{g1}-V_T+L_gE_p)^2}}-1\right), \tag{4.94}$$

with E_p as the electric field at pinch-off point and E_{crit} as the critical electric field.

$$E_{crit} = \frac{v_{sat}}{\mu_0}, \tag{4.95}$$

whereby v_{sat} and μ_0 represent the saturation velocity of the charge carriers and the low-field mobility, respectively.

In Fig. 4.27 the separated components of the calculated mobile charge $Q_{m,acc}$ at zero drain voltage are illustrated. The modeled charges incorporate the smoothing functions V_{g1} and V_{g2}

from equations (4.64) and (4.65), respectively (which were illustrated in Fig. 4.24). To visualize the transition point, $Q_{m,dep}$ which is saturated above V_{fit} and the component $(Q_{m,acc} - Q_{m,dep})$ which is saturated below V_{fit} are displayed.

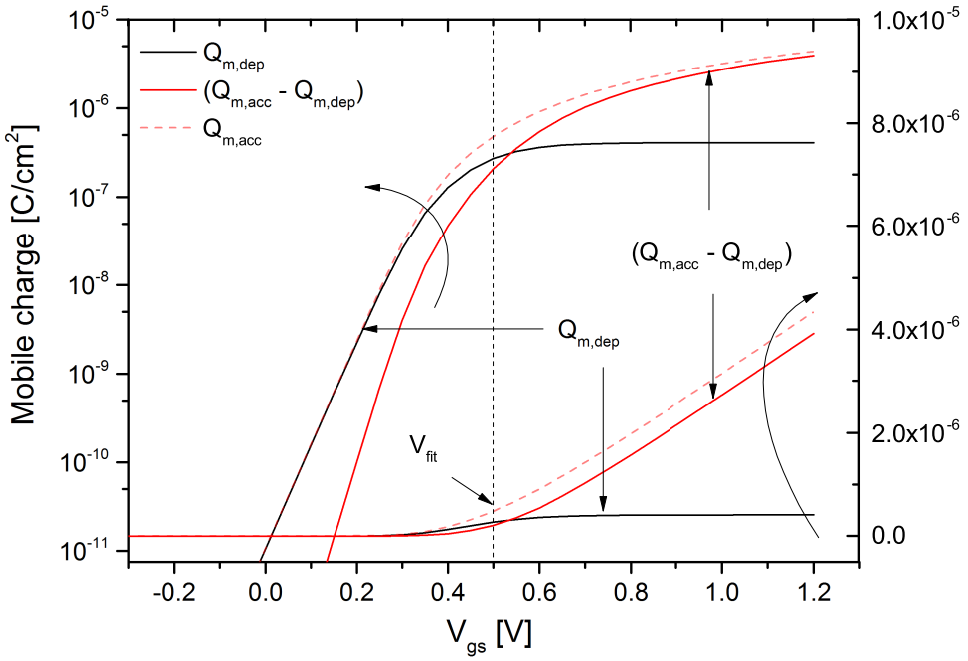


Figure 4.27: Illustration of the mobile charge and its separated components. Device parameters: $V_{ds} = 0\,\mathrm{V}$, $N_d = 1 \cdot 10^{18}\,\mathrm{cm}^{-3}$, $L_g = 22\,\mathrm{nm}$, $L_{sd} = 10\,\mathrm{nm}$, $T_{ch} = 10\,\mathrm{nm}$, $T_{ox} = 2\,\mathrm{nm}$.

4.6 Modeling the Drain Current

By redefining $Q_{m,acc,s}$ and $Q_{m,acc,d}$ (from equations (4.87) and (4.88)) as Q_s and Q_d, respectively, the final current equation, which is valid in all operating regions, takes the simple form [141]:

$$I_{ds} = \frac{\mu\, W_{ch}}{L_g} \left[V_{th}\, (Q_s - Q_d) + \frac{\left({Q_s}^2 - {Q_d}^2 \right)}{4\, C_{ox}} \right], \tag{4.96}$$

with W_{ch} as the device's width. Equation (4.96) was shown to fit very well for standard inversion mode DG MOSFETs. However, if a junctionless device is considered a modification, which accounts for the different operating modes (volume and surface conduction), is mandatory in order to correctly model the drain current in such devices. To maintain continuity of the drain current, even at derivatives of higher-order, a simple hyperbolic tangent function is introduced.

$$f = a - b \cdot \tanh\left(c \cdot (x - d)\right) \tag{4.97}$$

To account for subthreshold slope degradation in the depletion regime, the parameters a, b, c and d from Eq. (4.97) are determined as:

$$a_{\tilde{\alpha}} = \left(\frac{\alpha}{2} + \frac{1}{2}\right) \tag{4.98}$$

$$b_{\tilde{\alpha}} = \left(\frac{\alpha}{2} - \frac{1}{2}\right) \tag{4.99}$$

$$c_{\tilde{\alpha}} = 3 \tag{4.100}$$

$$d_{\tilde{\alpha}} = V_{fit} \tag{4.101}$$

and $x = V_{gs}$. Using these relations in Eq. (4.97) leads to:

$$\tilde{\alpha} = \left(\frac{\alpha}{2} + \frac{1}{2}\right) - \left(\frac{\alpha}{2} - \frac{1}{2}\right) \cdot \tanh\left(3 \cdot (V_{gs} - V_{fit})\right). \tag{4.102}$$

The effect of volume conduction in the depletion region is taken into account by replacing C_{eff} with $\tilde{C}$ (per unit area) in the drain current expression (Eq. (4.96)). The usage of the tangent hyperbolic function gives:

$$a_{\tilde{C}} = \left(\frac{\alpha}{2} + \frac{\alpha}{1}\right) \tag{4.103}$$

$$b_{\tilde{C}} = \left(\frac{\alpha}{2} - \frac{\alpha}{1}\right) \tag{4.104}$$

$$c_{\tilde{C}} = c_{\tilde{\alpha}} \tag{4.105}$$

$$d_{\tilde{C}} = d_{\tilde{\alpha}} \tag{4.106}$$

$$\tilde{C} = \left(\frac{C_{eff}}{2} + \frac{C_{ox}}{2}\right) - \left(\frac{C_{eff}}{2} - \frac{C_{ox}}{2}\right) \cdot \tanh\left(3 \cdot (V_{gs} - V_{fit})\right). \tag{4.107}$$

This modification allows us to smoothly and continuously model the drain current in the depletion and the accumulation operating regime. If $V_{gs} < V_{fit}$, the effective gate capacitance is expressed as $\tilde{C} = C_{eff}$ and the subthreshold slope degradation factor as $\tilde{\alpha} = \alpha$. If $V_{gs} > V_{fit}$, the parameter $\tilde{C}$ is expressed as $\tilde{C} = C_{ox}$ and the effect of the subthreshold slope degradation vanishes with $\tilde{\alpha} = 1$. The final drain current equation, which can be used for both device types, the inversion mode and the junctionless transistor, finally reads as:

$$I_{ds} = \frac{\mu\, W_{ch}}{L_g} \left[V_{th}\, \tilde{\alpha}\, (Q_s - Q_d) + \frac{\left({Q_s}^2 - {Q_d}^2\right)}{4\, \tilde{C}} \right], \tag{4.108}$$

whereby in the case of an inversion mode device $\tilde{C}$ is always expressed as $\tilde{C} = C_{ox}$. It should be noted that Eq. (4.108) inherently includes all 2-D effects through the charge density model. In Fig. 4.28 the effective gate capacitance is displayed applying the explained modification.

Even the derivative of third-order of $\tilde{C}$ does not show any discontinuities. In the same way $\tilde{\alpha}$ is taken into account.

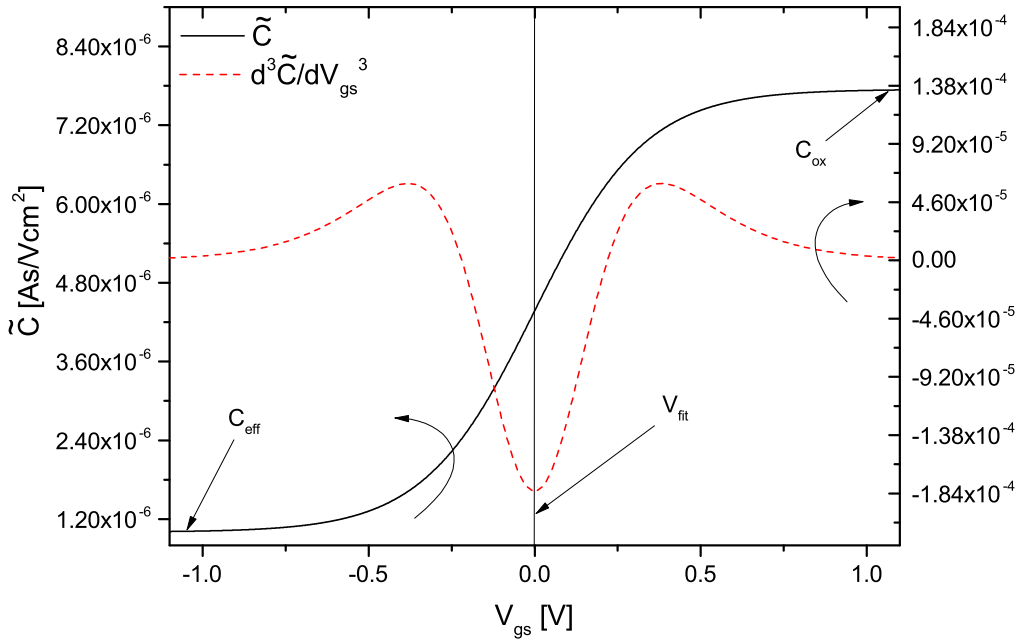


Figure 4.28: Illustration of the modified effective gate capacitance $\tilde{C}$ and its third derivative versus gate-source voltage V_{gs}. The transition from the depletion to the accumulation regime is smoothly modeled by the tangent hyperbolic function.

4.7 DC Model Validation and Discussion

The DC model is compared versus numerical 2-D TCAD Sentaurus simulation data [34]. The devices under investigation have various channel lengths and doping profiles, with a device width of $W_{ch} = 1\,\mu$m. The simulations are done at $T = 300\,$K, using a standard drift-diffusion transport model. Quantization effects are neglected in the following considerations since the channel thickness is at least $T_{ch} = 10\,$nm [31]. For simplicity a constant mobility $\mu = 300\,\text{cm}^2/\text{Vs}$ is assumed in the simulations and in the model. Important compact model metrics, such as continuity of the drain current even at derivatives of higher-order (up to third-order) and symmetry around $V_{ds} = 0\,$V are addressed and discussed.

4.7.1 Drain Current in Junctionless DG MOSFETs

Figure 4.29 shows the normalized transfer characteristics at $L_g = 22\,$nm and $100\,$nm in linear and logarithmic scale. At first sight, one can observe that the model agrees well with the

simulation data. Second, it becomes clear that the channel length has a noticeable influence on the device performance. At short channel sizes the current is very high, but at the cost of the performance below threshold voltage. The electrical parameters S, V_T and DIBL, as well as the slope degradation factor α of both the long and the short-channel device are summarized in Table 4.10, whereby the DIBL is defined by equation (4.60).

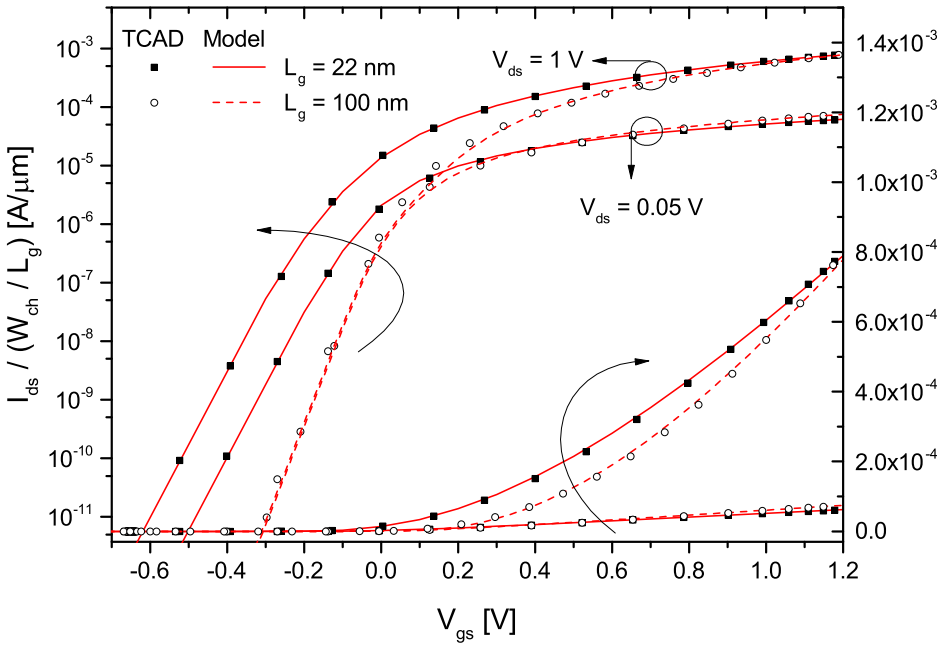


Figure 4.29: Transfer characteristics of the JL DG n-MOSFET with I_{ds} normalized by (W_{ch}/L_g). Parameters: $V_{ds} = 0.05\,/\,1$ [V], $N_d = 10^{19}\,\mathrm{cm}^{-3}$, $L_g = 22\,/\,100$ [nm], $L_{sd} = 10$ nm, $T_{ch} = 10$ nm, $T_{ox} = 2$ nm. Symbols TCAD; lines model.

L_g [nm]	V_T [V]	DIBL [mV]	S [mV/dev]	α [–]
22	-0.082 / -0.220	138	81.3 / 82.0	1.36 / 1.37
100	-0.006 / -0.006	0	59.5 / 59.5	0 / 0

Table 4.10: Extracted electrical parameters of Fig. 4.29. With V_T, S and α at $V_{ds} = 0.05\,/\,1$ [V].

One can see from Fig. 4.30 that compared to TCAD simulations, the model returns well matching results over the device's complete operating regime. The normalized output characteristic shows that, in the case of $L_g = 100$ nm the performance is worse than for $L_g = 22$ nm. On the other hand, the non-saturating current at $L_g = 22$ nm at high V_{gs} and V_{ds} indicates the presence of SCEs, which arise mainly due to the increased impact of the drain depletion region onto the channel region.

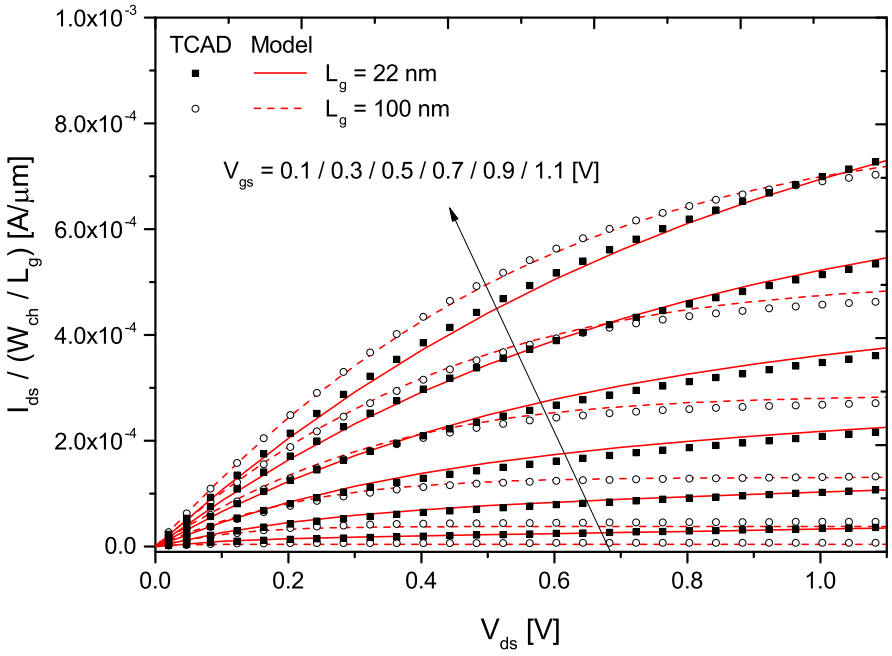


Figure 4.30: Output characteristics of the JL DG n-MOSFET with I_{ds} normalized by (W_{ch}/L_g). Parameters: $V_{gs} = 0.1\,\text{V}$ to $1.1\,\text{V}$ stepping $0.2\,\text{V}$, $N_d = 10^{19}\,\text{cm}^{-3}$, $L_g = 22\,/\,100\,[\text{nm}]$, $L_{sd} = 10\,\text{nm}$, $T_{ch} = 10\,\text{nm}$, $T_{ox} = 2\,\text{nm}$. Symbols TCAD; lines model.

The influence of an altering channel doping concentration N_d on the device performance is investigated in Fig. 4.31. N_d is altered, whereby the source/drain doping concentrations N_{sd} are kept constant. Table 4.11 contains the extracted electrical parameters, with $V_{ds} = 1\,\text{V}$. From the results one can identify a strong dependency of V_T on N_d. V_T is strongly degraded when $N_d > 10^{19}\,\text{cm}^{-3}$, or in other words V_T rolls-off (ΔV_T) and tends to be negative [88]. This effect implies that JL DG n-MOSFETs are rather not immune to variability due to the possible random dopant fluctuation (RDF) effect, which is one of their major issues up-to-date [101, 116]. The modeled results were obtained by slightly adjusting the saturation velocity, ϕ_T and V_{fit} in the model, which is plausible since an altering N_d directly impacts these parameters. The subthreshold slope S for the presented cases was found to remain almost unchanged - even for very high channel doping concentrations.

$N_d\,[\text{cm}^{-3}]$	$1 \cdot 10^{18}$	$5 \cdot 10^{18}$	$1 \cdot 10^{19}$	$2 \cdot 10^{19}$
V_T [V]	0.213	0.020	-0.220	-0.684
S [mV/dec]	84.4	81.5	82.0	81.3
α [−]	1.41	1.36	1.37	1.36

Table 4.11: Extracted electrical parameters of Fig. 4.31. With V_T, S and α at $V_{ds} = 1\,\text{V}$.

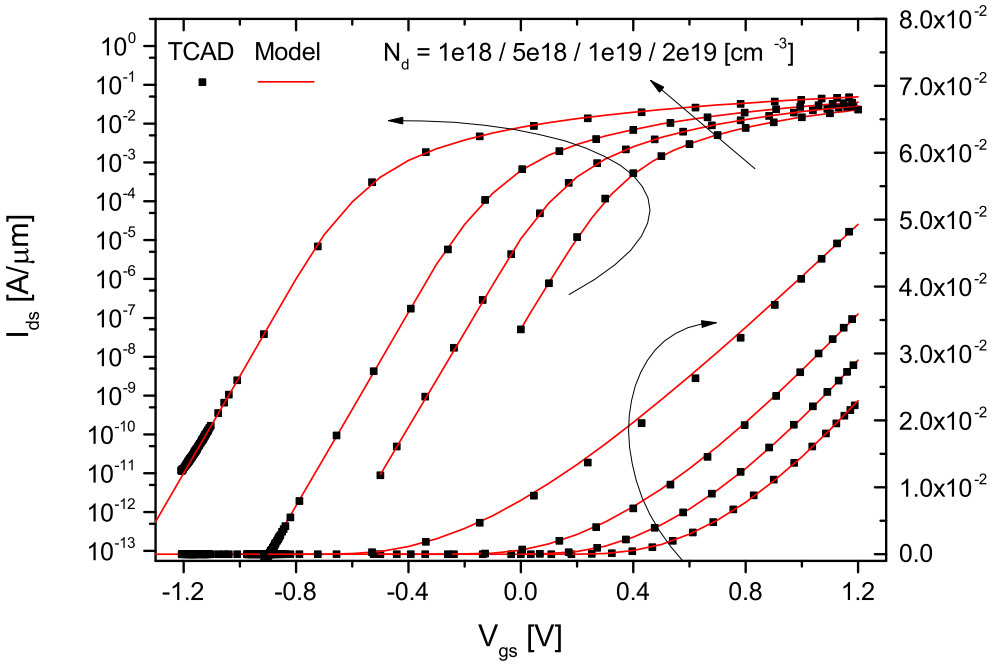


Figure 4.31: Transfer characteristics of the JL DG n-MOSFET. Parameters: $V_{ds} = 1\,\mathrm{V}$, $N_d = 1 \cdot 10^{18} \,/\, 5 \cdot 10^{18} \,/\, 1 \cdot 10^{19} \,/\, 2 \cdot 10^{19}\,[\mathrm{cm}^{-3}]$, $L_g = 22\,\mathrm{nm}$, $L_{sd} = 10\,\mathrm{nm}$, $T_{ch} = 10\,\mathrm{nm}$, $T_{ox} = 2\,\mathrm{nm}$. Symbols TCAD; lines model.

By altering the channel length L_g of the JL DG n-MOSFET one can observe some important effects (Fig. 4.32). Focusing on $L_g = 22$ and $32\,\mathrm{nm}$, one can observe strong differences in SCEs (Table 4.12). The threshold voltage roll-off and the slope degradation are much less for $L_g = 32\,\mathrm{nm}$, while maintaining a large ON-current at this channel length.

L_g [nm]	22	32	65	100
V_T [V]	-0.220	-0.084	-0.034	-0.006
S [mV/dec]	82.0	66.4	59.8	59.5
α [−]	1.37	1.11	≈ 1	1

Table 4.12: Extracted electrical parameters of Fig. 4.32. With V_T, S and α at $V_{ds} = 1\,\mathrm{V}$.

Fig. 4.33 shows the gate transconductance g_m for a 22 nm short-channel device with $N_d = 10^{19}\,\mathrm{cm}^{-3}$ at low and high drain biases. Some discrepancies with the simulated TCAD data and the model occur in the saturation regime at high V_{gs}. However, no discontinuities are observed in the model. For convenience the absolute values of the second- and third-order derivatives of the same device are detailed in Figs. 4.34(a) and 4.34(b), respectively.

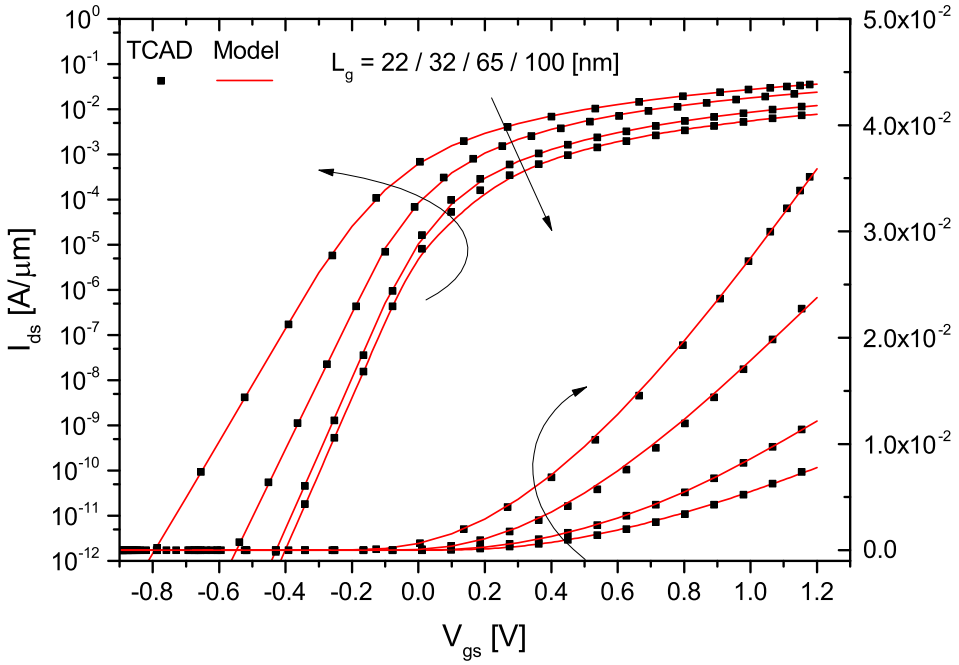


Figure 4.32: Transfer characteristics of the JL DG n-MOSFET. Parameters: $V_{ds} = 1\,\mathrm{V}$, $N_d = 10^{19}\,\mathrm{cm}^{-3}$, $L_g = 22\,/\,32\,/\,65\,/\,100\,[\mathrm{nm}]$, $L_{sd} = 10\,\mathrm{nm}$, $T_{ch} = 10\,\mathrm{nm}$, $T_{ox} = 2\,\mathrm{nm}$. Symbols TCAD; lines model.

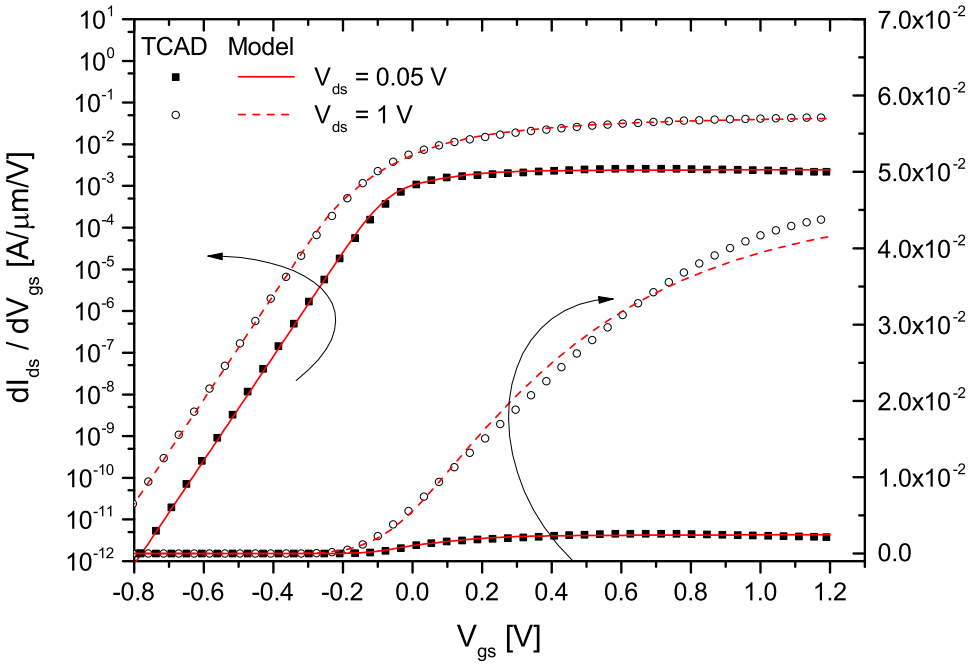
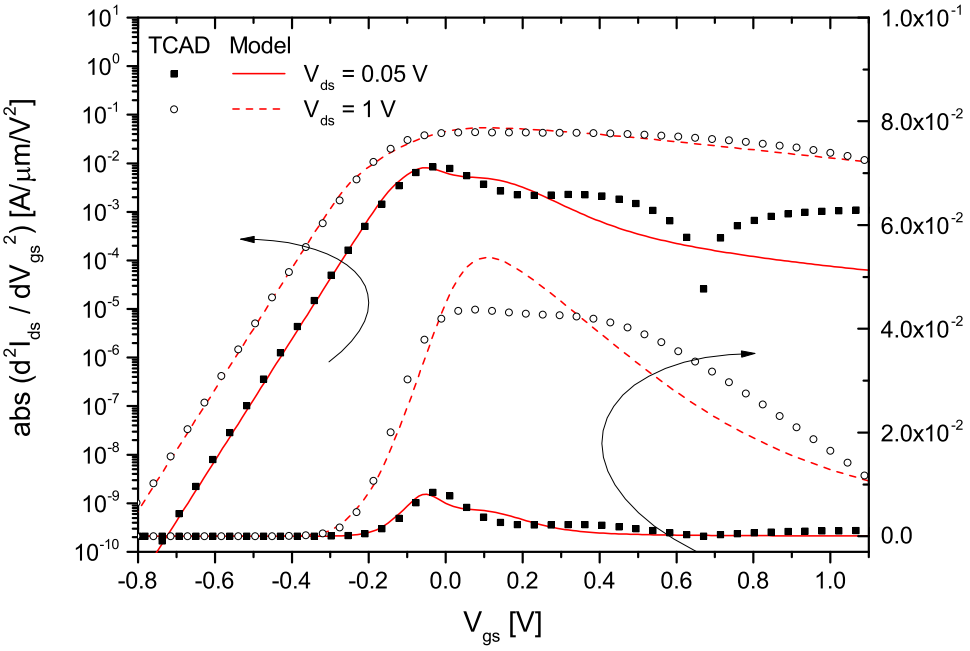
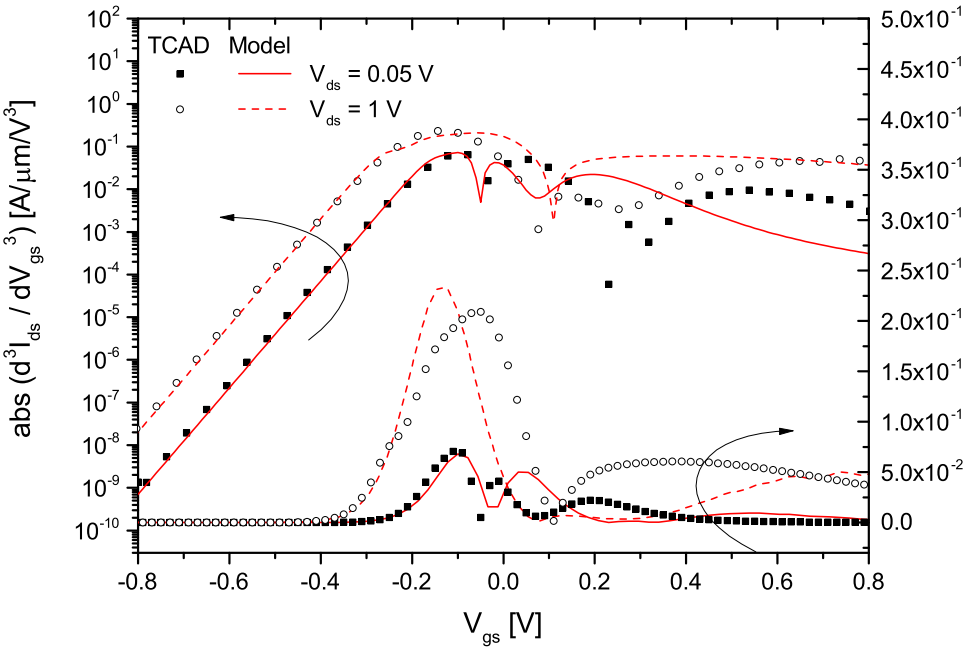


Figure 4.33: Gate transconductance g_m of the JL DG n-MOSFET. Parameters: $V_{ds} = 0.05\,/\,1\,[\mathrm{V}]$, $N_d = 10^{19}\,\mathrm{cm}^{-3}$, $L_g = 22\,\mathrm{nm}$, $L_{sd} = 10\,\mathrm{nm}$, $T_{ch} = 10\,\mathrm{nm}$, $T_{ox} = 2\,\mathrm{nm}$. Symbols TCAD; lines model.



(a)



(b)

Figure 4.34: Absolute values of: (a) Second-order derivative of the JL DG n-MOSFET. (b) Third-order derivative of the same device. Parameters: $V_{ds} = 0.05\,/\,1\,[\mathrm{V}]$, $N_d = 10^{19}\,\mathrm{cm}^{-3}$, $L_g = 22\,\mathrm{nm}$, $L_{sd} = 10\,\mathrm{nm}$, $T_{ch} = 10\,\mathrm{nm}$, $T_{ox} = 2\,\mathrm{nm}$. Symbols TCAD; lines model.

Concerning the drain conductance g_d, a fairly good agreement between the model and the data from TCAD can be observed (Fig. 4.35).

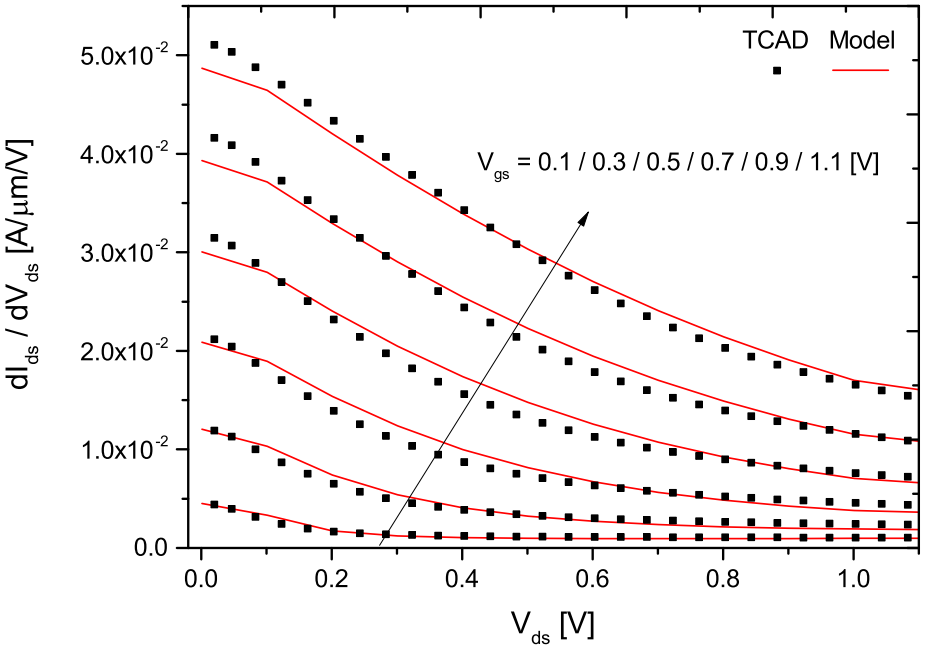


Figure 4.35: Drain conductance g_d of the JL DG n-MOSFET. Parameters: $V_{gs} = 0.1\,\mathrm{V}$ to $1.1\,\mathrm{V}$ stepping $0.2\,\mathrm{V}$, $N_d = 10^{19}\,\mathrm{cm}^{-3}$, $L_g = 22\,\mathrm{nm}$, $L_{sd} = 10\,\mathrm{nm}$, $T_{ch} = 10\,\mathrm{nm}$, $T_{ox} = 2\,\mathrm{nm}$. Symbols TCAD; lines model.

Since symmetry around $V_{ds} = 0\,\mathrm{V}$ is a key property of compact models, it is addressed in the following. The model is verified with respect to a source/drain reversal test [78], showing the drain current I_{ds} and its first derivative (Fig. 4.36). The results are plotted versus voltage V_x, which is asymmetrically biasing the source and drain contacts with $V_{source} = -V_x$ and $V_{drain} = +V_x$, respectively. Even at $L_g = 22\,\mathrm{nm}$, where SCEs play an important role, I_{ds} and also its derivative are symmetric in the detailed regime, which proves that the developed model passes the symmetry test.

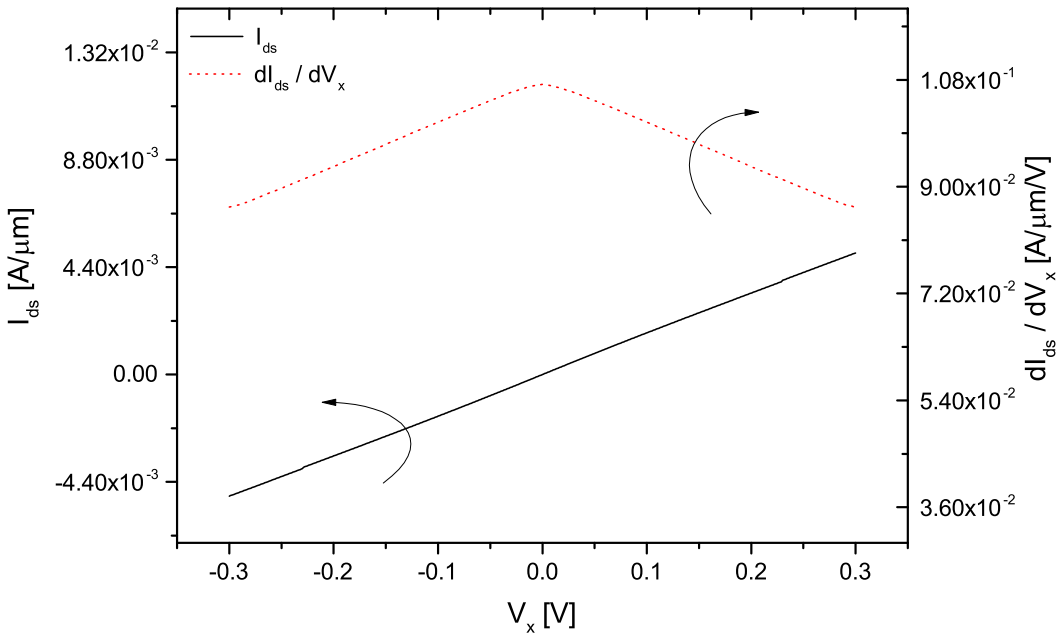


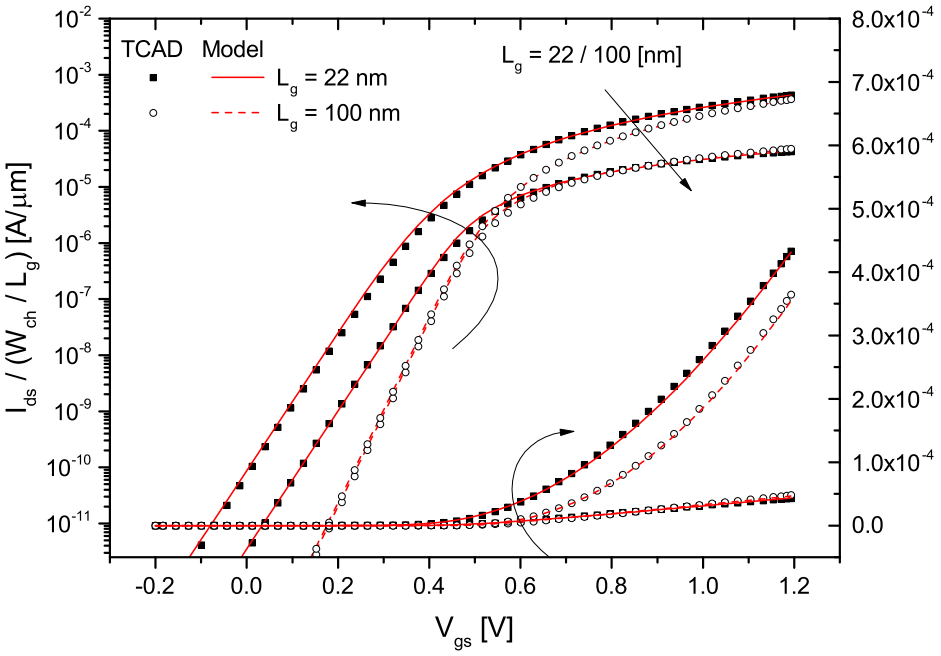
Figure 4.36: Source-drain symmetry test. The drain current I_{ds} and its first derivative are plotted versus voltage V_x. Parameters: $V_x = -0.3\,\mathrm{V}$ to $0.3\,\mathrm{V}$, $V_{gs} = 1\,\mathrm{V}$, $N_d = 10^{19}\,\mathrm{cm}^{-3}$, $L_g = 22\,\mathrm{nm}$, $L_{sd} = 10\,\mathrm{nm}$, $T_{ch} = 10\,\mathrm{nm}$, $T_{ox} = 2\,\mathrm{nm}$.

4.7.2 Drain Current in Inversion Mode DG MOSFETs

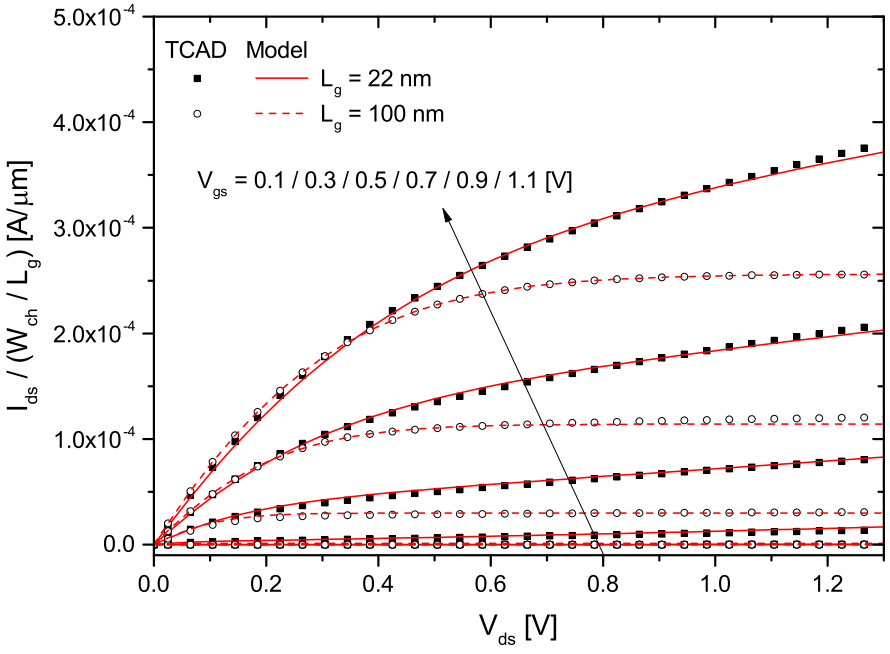
The drain current model for the standard inversion mode DG MOSFET is investigated in this section. Starting with the comparison of the performance of a long- and short-channel device, one can see that it all concerns about trade-off between subthreshold and above threshold performance (Fig. 4.37(a)). The long-channel device ($L_g = 100\,\mathrm{nm}$) scores with an ideal S and very low DIBL, i.e. almost no threshold voltage roll-off exists. On the other hand, at $L_g = 22\,\mathrm{nm}$, the performance above V_T is much better. The ON-current is much larger, compared to its long-channel counterpart, but the OFF-current increases, which leads to an increased power consumptions due to larger leakage currents in such devices. Table 4.13 summarizes their electrical parameters. The output characteristics of the same devices are shown in Fig. 4.37(b).

L_g [nm]	V_T [V]	DIBL [mV]	S [mV/dev]	α [–]
22	0.412 / 0.340	85	79.4 / 79.8	1.33 / 1.34
100	0.464 / 0.464	0	59.5 / 59.5	0 / 0

Table 4.13: Extracted electrical parameters of Fig. 4.37. With V_T, S and α at $V_{ds} = 0.05\,/\,1\,[\mathrm{V}]$.



(a)



(b)

Figure 4.37: (a) Transfer characteristics of the IM DG n-MOSFET with I_{ds} normalized by (W_{ch}/L_g). (b) Output characteristics of the same device. Parameters: $V_{ds} = 0.05\,/\,1\,[\mathrm{V}]$, $N_a = 10^{18}\,\mathrm{cm}^{-3}$, $L_g = 22\,/\,100\,[\mathrm{nm}]$, $L_{sd} = 10\,\mathrm{nm}$, $T_{ch} = 10\,\mathrm{nm}$, $T_{ox} = 2\,\mathrm{nm}$. Symbols TCAD; lines model.

A very important effect in the transfer characteristics can be observed when focusing on Fig. 4.38. Contrary to junctionless devices, the shift in threshold voltage (ΔV_T) in inversion mode transistors, when altering the channel doping concentration, is almost not worth mentioning it ($\Delta V_T \approx 0.03\,\mathrm{V}$). This behavior was already discussed and illustrated in section 4.4, Fig. 4.19(b). It becomes clear that IM transistors can handle dopant fluctuations inside the channel region better than JL devices. In addition, one can observe that the subthreshold performance and the DIBL are not affected by varying N_a (see Table 4.14).

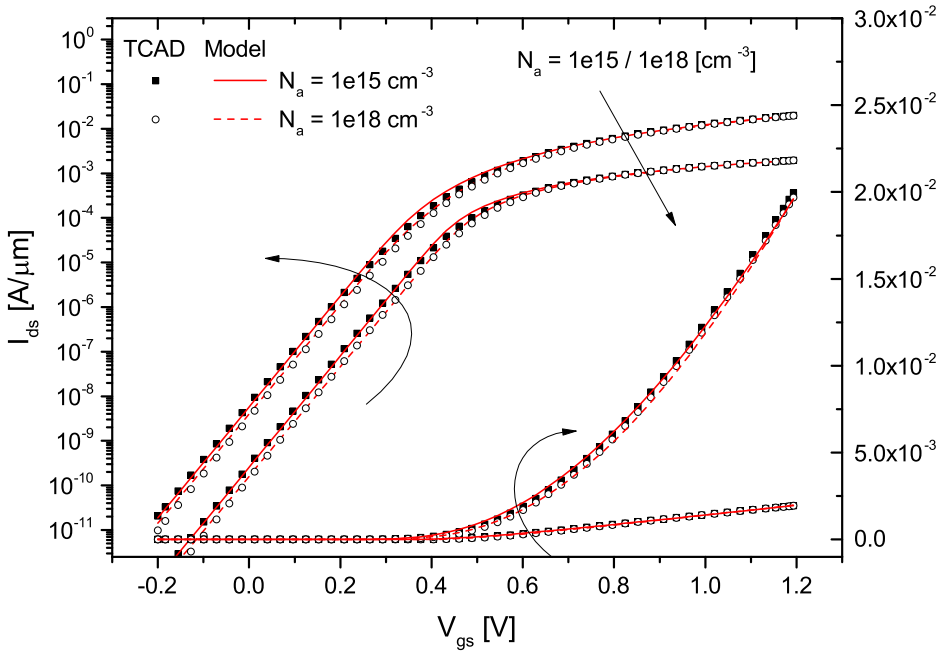


Figure 4.38: Transfer characteristics of the IM DG n-MOSFET. Parameters: $V_{ds} = 0.05\,/\,1\,[\mathrm{V}]$, $N_a = 1 \cdot 10^{15}\,/\,1 \cdot 10^{18}\,[\mathrm{cm}^{-3}]$, $L_g = 22\,\mathrm{nm}$, $L_{sd} = 10\,\mathrm{nm}$, $T_{ch} = 10\,\mathrm{nm}$, $T_{ox} = 2\,\mathrm{nm}$. Symbols TCAD; lines model.

$N_a\,[\mathrm{cm}^{-3}]$	$1 \cdot 10^{15}$	$1 \cdot 10^{18}$
$V_T\,[\mathrm{V}]$	0.382 / 0.300	0.412 / 0.340
DIBL [mV]	82	85
$S\,[\mathrm{mV/dec}]$	79.1 / 79.1	79.4 / 79.8
$\alpha\,[-]$	1.32 / 1.32	1.33 / 1.34

Table 4.14: Extracted electrical parameters of Fig. 4.38. With V_T, S and α at $V_{ds} = 0.05\,/\,1\,[\mathrm{V}]$.

In Figure 4.39, the impact of different channel lengths L_g on the device performance is investigated. Therefore, I_{ds} is plotted against V_{gs} for a varying L_g at $V_{ds} = 1\,\mathrm{V}$. The model correctly predicts the drain current for all presented cases. In log-scale, one can see that the subthreshold slope S is a strong function of L_g. S worsens (increases) with decreasing L_g, due to the increased electrostatic impact of the source/drain regions onto the channel area (which can be considered as a short-channel effect). In linear-scale, the maximum drain current is observed to correlate with L_g as well. The shorter the channel, the higher is the drain current, because of the reduction of the device's channel resistance. Details about the electrical parameters of this example can be found in Table 4.15.

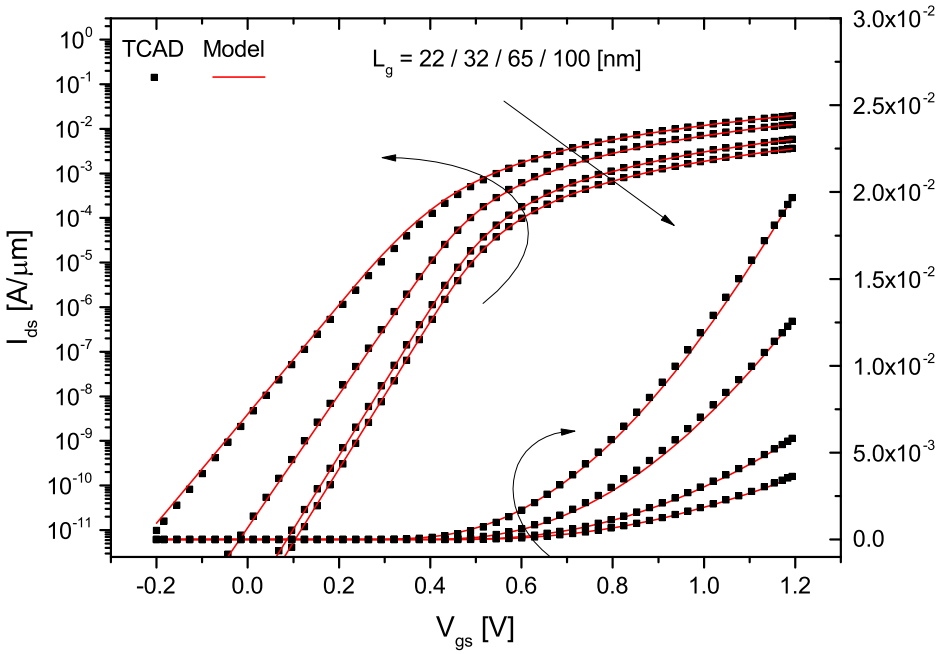


Figure 4.39: Transfer characteristics of the IM DG n-MOSFET. Parameters: $V_{ds} = 1\,\mathrm{V}$, $N_a = 1 \cdot 10^{18}\,\mathrm{cm}^{-3}$, $L_g = 22\,/\,32\,/\,65\,/\,100\,[\mathrm{nm}]$, $L_{sd} = 10\,\mathrm{nm}$, $T_{ch} = 10\,\mathrm{nm}$, $T_{ox} = 2\,\mathrm{nm}$. Symbols TCAD; lines model.

L_g [nm]	22	32	65	100
V_T [V]	-0.220	-0.084	-0.034	-0.006
S [mV/dec]	82.0	66.4	59.8	59.5
α [−]	1.37	1.11	≈ 1	1

Table 4.15: Extracted electrical parameters of Fig. 4.39. With V_T, S and α at $V_{ds} = 1\,\mathrm{V}$.

CHAPTER 5

AC Model

As discussed in the previous chapter, a DC model is applicable when the applied terminal voltages do not vary with time. In this chapter a dynamic model (AC model), which is applicable when the terminal voltages are varying with time, is developed. This dynamic behavior is a direct result of the MOSFET's capacitive effects. These are related to the charges stored in the device, which require an accurate description of how they depend on the terminal voltages. The mentioned stored charges in the device are the mobile charge Q_m in the channel region, the gate charge Q_g at the gate terminal and the source/drain charges due to the pn-junctions. For developing dynamic or transient models, one divides the device into the intrinsic and the extrinsic part [22, 142].

- *The intrinsic part*: is mainly responsible for the transistor action. The responsible charges are the gate, the mobile and the source/drain charges due to the pn-junctions (Fig. 5.1(a)). The capacitances arising from these charges are called intrinsic or trans-capacitances. They are normally derived from the charges which are used to calculate the steady-state current I_{ds}.

- *The extrinsic part*: includes C_{ov} which is the parallel plate capacitance associated with the electric field in the gate to source/drain overlap region. C_{if} as the inner fringing capacitance associated with the inner electric field originating from the metallurgical junction of the source/drain, ending beneath the gate electrode. And C_{of} as the outer fringing capacitance associated with the electric field originating from the side of the gate electrode and ending at the source/drain regions (Fig. 5.1(b)). All of these capacitances, except for C_{of}, are bias dependent and must be taken into account properly in order to correctly model the capacitive effects in MOSFETs.

The capacitive characteristics of the MOSFET are then the sum of the intrinsic and the extrinsic parts. These capacitances are responsible for limiting the overall device performance in terms of device switching speed [22].

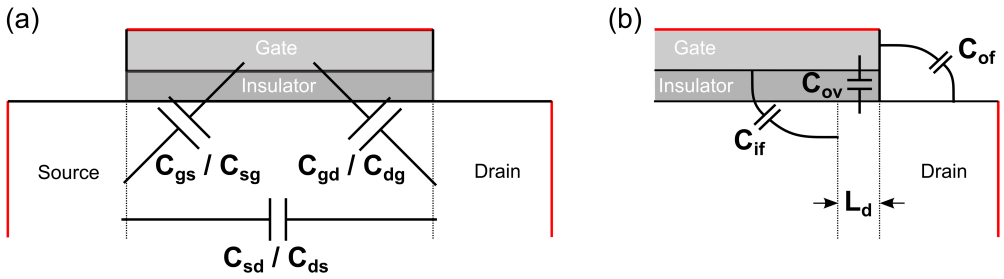


Figure 5.1: Illustration of the (a) intrinsic and (b) extrinsic capacitances of a MOSFET. L_d denotes the gate overlap region.

5.1 Charge-Based Capacitance Models

Since the terminal charges Q_j are a function of the applied terminal voltages (V_g, V_s, V_d) the terminal current i_j can generally be expressed as [22]:

$$i_j = \frac{dQ_j}{dt} = \frac{\partial Q_j}{\partial V_g}\frac{\partial V_g}{\partial t} + \frac{\partial Q_j}{\partial V_s}\frac{\partial V_s}{\partial t} + \frac{\partial Q_j}{\partial V_d}\frac{\partial V_d}{\partial t}, \tag{5.1}$$

where $j = G, S, D$. A three-terminal device, such as the DG MOSFET, therefore consists of nine nonreciprocal capacitances, which must be described in an appropriate manner in order to run small-signal simulations. These capacitances are defined as:

$$C_{ij} = \begin{cases} -\dfrac{\partial Q_i}{\partial V_j}, & \text{if } i \neq j \quad i,j = G,S,D \\ +\dfrac{\partial Q_i}{\partial V_j}, & \text{if } i = j, \end{cases} \tag{5.2}$$

whereby this expression can be rewritten in form of a capacitance matrix.

$$C_{ij} = \begin{bmatrix} C_{gg} & -C_{gd} & -C_{gs} \\ -C_{dg} & C_{dd} & -C_{ds} \\ -C_{sg} & -C_{sd} & C_{ss} \end{bmatrix} \tag{5.3}$$

Each element C_{ij} of this capacitance matrix describes the dependence of the charge at the terminal i with respect to the voltage applied at the terminal j, while all other voltages remain unchanged. Applying the charge conservation law [143, 144], the following relations between the capacitances can be derived from the above matrix.

$$C_{ss} = C_{sd} + C_{sg} = C_{ds} + C_{gs} \tag{5.4}$$

$$C_{gg} = C_{gs} + C_{gd} = C_{sg} + C_{dg} \tag{5.5}$$

$$C_{dd} = C_{ds} + C_{dg} = C_{sd} + C_{gd} \tag{5.6}$$

One can see that only four capacitances are left independent from each other, which simplifies the calculations. The capacitances C_{ss}, C_{gg} and C_{dd} are referred to as the terminal capacitances (source, gate and drain) and the others are called intrinsic or trans-capacitances.

The following charge-based model for the capacitances will be derived under the assumption that the quasi-static (QS) condition holds. That is, the terminal voltages vary sufficiently slow so that the stored charges can follow variations in the terminal voltages. Nevertheless, if the parasitic capacitances are low and if the changes in the input waveforms are too fast, the assumption of quasi-static operation is invalid, wherefore a non-quasi-static (NQS) model should be applied [22, 145].

5.2 Modeling the Total Charges

The DG MOSFET is a three terminal device. Therefore, only three terminal charges, i.e. Q_G, Q_D and Q_S, associated with gate, drain, and source, respectively, must be calculated. The total channel charge is obtained by integrating the channel charge density along the channel. The total charges at drain and source are obtained by adapting Ward-Dutton's linear charge partition method. This method is widely accepted and was shown to return accurate results in bulk MOSFETs [56, 146].

$$Q_C = -W_{ch} \int_0^{L_g} Q \, dx \tag{5.7}$$

$$Q_D = W_{ch} \int_0^{L_g} \frac{x}{L_g} Q \, dx \tag{5.8}$$

$$Q_S = W_{ch} \int_0^{L_g} \left(1 - \frac{x}{L_g}\right) Q \, dx, \tag{5.9}$$

with Q_C as the total channel charge. Adopting the drift-diffusion model, and rearranging for dx results in:

$$dx = \left(-\frac{W_{ch}\,\mu}{I_{ds}} \cdot Q\right) dV. \tag{5.10}$$

dV is represented by equation (4.79) and reads as:

$$dV = \left(\frac{\tilde{\alpha}\, V_{th}}{Q} + \frac{1}{2\,\tilde{C}}\right) dQ, \tag{5.11}$$

whereby $\tilde{\alpha}$ and $\tilde{C}$ are given by equations (4.102) and (4.107), respectively. Substituting dx and dV into Eq. (5.7) allows the integral to be carried out.

$$\begin{aligned} Q_C &= -W_{ch} \int_0^{L_g} Q \, dx \\ &= -W_{ch} \int_0^{V_{ds}} Q \cdot \left(-\frac{W_{ch}\,\mu}{I_{ds}} \cdot Q \right) dV \\ &= -W_{ch} \int_{Q_s}^{Q_d} Q \cdot \left(-\frac{W_{ch}\,\mu}{I_{ds}} \cdot Q \right) \cdot \left(\frac{\tilde{\alpha}\, V_{th}}{Q} + \frac{1}{2\,\tilde{C}} \right) dQ \\ &= \frac{{W_{ch}}^2\,\mu}{I_{ds}} \int_{Q_s}^{Q_d} Q^2 \left(\frac{\tilde{\alpha}\, V_{th}}{Q} + \frac{1}{2\,\tilde{C}} \right) dQ \\ &= \frac{{W_{ch}}^2\,\mu}{I_{ds}} \left[\frac{Q^3}{6\,\tilde{C}} + \frac{Q^2\,\tilde{\alpha}\, V_{th}}{2} \right]_{Q_s}^{Q_d} \end{aligned} \tag{5.12}$$

Q_s and Q_d represent the charge densities at source and drain, respectively, and I_{ds} the drain current. The resulting expression of Q_C is given in appendix A. The total gate charge Q_G is finally obtained from the charge neutrality condition.

$$Q_G = -Q_C - Q_{OX} - Q_F, \tag{5.13}$$

where $Q_{OX} \approx 0$ and Q_F are the total fixed charges at the silicon-to-oxide interface and in the channel region, respectively.

$$Q_F = W_{ch}\, L_g \cdot (\pm q\, N_b\, T_{ch}), \tag{5.14}$$

where the $(+)$ sign is for p-type semiconductors ($N_b = N_a$) and the $(-)$ sign is for n-type semiconductors ($N_b = N_d$).

Preliminary to the calculation of the total charges at drain and source (Q_D and Q_S), equation (5.10) is integrated along the channel to yield x, whereby dV from Eq. (5.11) is directly substituted. The rest of the calculations then follow the same principle as presented for Q_C.

$$\begin{aligned} \int_0^x dx &= -\frac{W_{ch}\,\mu}{I_{ds}} \int_{Q_s}^{Q} Q \cdot \left(\frac{\tilde{\alpha}\, V_{th}}{Q} + \frac{1}{2\,\tilde{C}} \right) dQ \\ x &= -\frac{W_{ch}\,\mu}{I_{ds}} \int_{Q_s}^{Q} \left(\tilde{\alpha}\, V_{th} + \frac{Q}{2\,\tilde{C}} \right) dQ \end{aligned}$$

$$x = +\frac{W_{ch}\,\mu}{I_{ds}}\left[\tilde{\alpha}\,V_{th}\,Q + \frac{Q^2}{4\,\tilde{C}}\right]_Q^{Q_s} \tag{5.15}$$

By using dx, dV and x in Eq. (5.8) and (5.9) the integrals can be solved for Q_D and Q_S.

$$\begin{aligned} Q_D &= W_{ch}\int_{Q_s}^{Q_d}\frac{W_{ch}\,\mu}{I_{ds}\,L_g}\left[\tilde{\alpha}\,V_{th}\,Q + \frac{Q^2}{4\,\tilde{C}}\right]_Q^{Q_s}\cdot Q\cdot\left(-\frac{W_{ch}\,\mu}{I_{ds}}\cdot Q\right)\cdot\left(\frac{\tilde{\alpha}\,V_{th}}{Q}+\frac{1}{2\,\tilde{C}}\right)\,dQ \\ &= -\frac{{W_{ch}}^3\,\mu^2}{{I_{ds}}^2\,L_g}\int_{Q_s}^{Q_d} Q^2\left[\tilde{\alpha}\,V_{th}\,Q + \frac{Q^2}{4\,\tilde{C}}\right]_Q^{Q_s}\cdot\left(\frac{\tilde{\alpha}\,V_{th}}{Q}+\frac{1}{2\,\tilde{C}}\right)\,dQ \end{aligned} \tag{5.16}$$

$$\begin{aligned} Q_S &= W_{ch}\int_{Q_s}^{Q_d}\left(1-\frac{W_{ch}\,\mu}{I_{ds}\,L_g}\left[\tilde{\alpha}\,V_{th}\,Q + \frac{Q^2}{4\,\tilde{C}}\right]_Q^{Q_s}\right)\cdot Q\cdot\left(-\frac{W_{ch}\,\mu}{I_{ds}}\cdot Q\right)\cdot\left(\frac{\tilde{\alpha}\,V_{th}}{Q}+\frac{1}{2\,\tilde{C}}\right)\,dQ \\ &= -\frac{{W_{ch}}^2\,\mu}{I_{ds}}\int_{Q_s}^{Q_d} Q^2\left(1-\frac{W_{ch}\,\mu}{I_{ds}\,L_g}\left[\tilde{\alpha}\,V_{th}\,Q + \frac{Q^2}{4\,\tilde{C}}\right]_Q^{Q_s}\right)\cdot\left(\frac{\tilde{\alpha}\,V_{th}}{Q}+\frac{1}{2\,\tilde{C}}\right)\,dQ \end{aligned} \tag{5.17}$$

The solutions of equations (5.16) and (5.17) are given in appendix A. Instead of solving the complex integral (5.9), Q_S could also be obtained through the following relation (based on the charge conservation law), which leads exactly to the same result:

$$Q_S = Q_C - Q_D. \tag{5.18}$$

It should be noted that when $V_{ds} = 0\,\mathrm{V}$, the numerator and the denominator of the expressions for the charges become zero. This fact will obviously cause numerical problems which must be overcome. A possible solution is to switch to the asymptotic value of the gate charge as V_{ds} approaches zero. The total charges at source and drain have then half of the negative magnitude of the total gate charge [63].

$$Q_G(V_{ds} = 0\,\mathrm{V}) = W_{ch}\,L_g\,Q_s \tag{5.19}$$

$$Q_C(V_{ds} = 0\,\mathrm{V}) = -Q_G(V_{ds} = 0\,\mathrm{V}) \tag{5.20}$$

$$Q_D(V_{ds} = 0\,\mathrm{V}) = \frac{-Q_G(V_{ds} = 0\,\mathrm{V})}{2} \tag{5.21}$$

$$Q_S(V_{ds} = 0\,\mathrm{V}) = \frac{-Q_G(V_{ds} = 0\,\mathrm{V})}{2} \tag{5.22}$$

Figure 5.2 shows the terminal charges plotted versus the drain voltage, whereby at $V_{ds} = 0\,\mathrm{V}$ the total source/drain charges are equal. In the saturation region these charges stay constant with a ratio $Q_D/Q_S = 40/60$, as expected from the linear charge partition method.

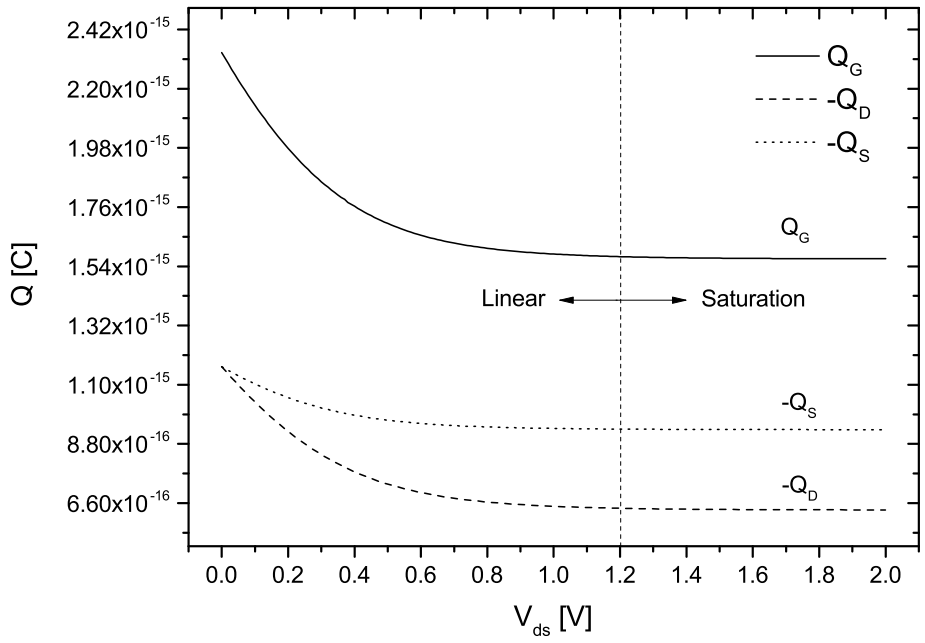


Figure 5.2: Terminal charges of an IM DG n-MOSFET plotted against drain voltage. Parameters: $V_{gs} = 1\,\mathrm{V}$, $N_a = 10^{15}\,\mathrm{cm}^{-3}$, $L_g = 100\,\mathrm{nm}$, $L_{sd} = 10\,\mathrm{nm}$, $T_{ch} = 10\,\mathrm{nm}$, $T_{ox} = 2\,\mathrm{nm}$. Lines model.

5.3 Capacitance Modeling

As discussed in the beginning of this chapter, the sum of the intrinsic and extrinsic parts determine the capacitive behavior of the device. Therefore, both parts must be taken into account in order to arrive at a complete capacitance model.

5.3.1 Intrinsic Capacitances

Only four out of the nine intrinsic capacitances must be calculated directly. The rest of them can readily be obtained from the relations (5.4) to (5.6). These four capacitances can be

$$C_{gg} = +\frac{dQ_G}{dV_g} \tag{5.23}$$

$$C_{dg} = -\frac{dQ_D}{dV_g} \tag{5.24}$$

$$C_{dd} = +\frac{dQ_D}{dV_d} \tag{5.25}$$

$$C_{gd} = -\frac{dQ_G}{dV_d}, \tag{5.26}$$

whereby the total terminal charges are differentiated with respect to the corresponding voltage. The remaining capacitances are then calculated to:

$$C_{gs} = C_{gg} - C_{gd} \tag{5.27}$$
$$C_{ds} = C_{dd} - C_{gd} \tag{5.28}$$
$$C_{ss} = C_{sd} - C_{sg} \tag{5.29}$$
$$C_{sg} = C_{gg} - C_{dg} \tag{5.30}$$
$$C_{sd} = C_{ss} - C_{sg}. \tag{5.31}$$

Given that the source terminal is used as the reference for the potentials, only six intrinsic capacitances exist, namely C_{gg}, C_{dg}, C_{sg}, C_{dd}, C_{gd} and C_{sd}.

To avoid numerical instability when the drain voltage $V_{ds} = 0\,\mathrm{V}$, one could switch to the asymptotic value of the corresponding capacitance [63, 64]. If V_{ds} is zero, the gate-channel capacitance is constant along the channel. Since there is no difference between the source and drain potential, the quasi-Fermi level is constant throughout the entire device and the gate charge density equals to the channel charge density, wherefore by using Eq. (5.11), C_{gg} will equal:

$$\begin{aligned} C_{gg}(V_{ds} = 0\,\mathrm{V}) &= W_{ch}\, L_g \cdot \frac{\partial Q_s}{\partial V_s} \\ &= W_{ch}\, L_g \cdot \left(\frac{\tilde{\alpha}\, V_{th}}{Q_s} + \frac{1}{2\,\tilde{C}} \right)^{-1}. \end{aligned} \tag{5.32}$$

Therefore, when $V_{ds} = 0\,\mathrm{V}$, the rest of the intrinsic capacitances can be computed to [147]:

$$C_{gg}(V_{ds} = 0\,\mathrm{V}) = 2\,C_{gd} = 2\,C_{dg} = 2\,C_{gs} = 2\,C_{sg} = -6\,C_{ds} = -6\,C_{sd} = 3\,C_{ss} = 3\,C_{dd} \tag{5.33}$$

5.3.2 Extrinsic Capacitances

The extrinsic capacitive part (C_{ext}) is described by the bias dependent gate overlap and inner fringing capacitance C_{ov} and C_{if}, respectively, as well as an outer fringing capacitance C_{of} (see Fig. 5.1).

$$C_{ext} = 2 \cdot (C_{ov}(V_g) + C_{if}(V_g) + C_{of}) \tag{5.34}$$

The outer fringing capacitance can be modeled using the relation given in [22]:

$$C_{of} = \frac{\varepsilon_0\, \varepsilon_{ox}}{\pi/2}\, \ln\left(1 + \frac{T_{gate}}{T_{ox}}\right), \tag{5.35}$$

where T_{gate} is the thickness of the gate. C_{of} is independent of the applied bias and it was shown that it becomes very significant for short-channel devices [142]. In contrast, modeling the inner fringing capacitance requires some more attention since it is a direct function of V_g.

A model which takes into account this bias dependence was presented in [142]. C_{if} between the gate and source regions is defined as:

$$C_{if} = C_{if,max} \cdot \exp\left[-\left(\frac{V_{gs} - V_{fb} - \phi_T/2}{3\,\phi_T/2}\right)^2\right], \tag{5.36}$$

where $C_{if,max}$ is treated as an adjustable parameter. Depending on the applied gate voltage, the device operates in depletion or accumulation. In between both operating regimes C_{if} takes its maximum value, given by $C_{if,max}$. At very small or large V_{gs} the inner fringing capacitance tends towards zero, because an inversion layer is build up which electrically disconnects the channel side fringing components.

The gate overlap capacitance between gate and source was modeled by [142], where L_d and δ represent the gate overlap region and an adjustable parameter which depends on the channel doping concentration, respectively.

$$C_{ov} = C_{ox}\left(\frac{L_d}{1 - \delta \cdot V^*}\right). \tag{5.37}$$

In order to make the bias dependent overlap capacitance converging to its maximum value, a smoothing function is introduced.

$$V^* = V_{gs} - 0.5 \cdot V_{gs} - 0.5\sqrt{{V_{gs}}^2 + 0.05}, \tag{5.38}$$

whereby, the value 0.05 describes a parameter which controls the transition from the subthreshold to above threshold regime. Well above threshold, V^* tends towards zero, wherefore $C_{ov} \approx W_{ch}\,C_{ox}\,L_d$, as expected [74]. C_{ov} decreases with V_{gs} (compare with Eq. (5.37)) and is approximatively zero well below threshold. Fig. 5.3 illustrates the behavior of C_{if} and C_{ov} plotted against V_{gs}.

The complete model for the extrinsic capacitances between gate and source, which must be added to the intrinsic part, is calculated to:

$$\begin{aligned} C_{ext,gs} = 2 \cdot W_{ch} \Bigg[& C_{ox}\left(\frac{L_d}{1 - \delta \cdot V^*}\right) \\ & + C_{if,max} \cdot \exp\left[-\left(\frac{V_{gs} - V_{fb} - \phi_T/2}{3\,\phi_T/2}\right)^2\right] \\ & + \frac{\varepsilon_0\,\varepsilon_{ox}}{\pi/2}\,\ln\left(1 + \frac{T_{poly}}{T_{ox}}\right)\Bigg]. \end{aligned} \tag{5.39}$$

Likewise, the extrinsic capacitance between the gate and drain ($C_{ext,gd}$) can be calculated by replacing V_{gs} with $V_{gd} = V_g - V_d$ in equations (5.36) to (5.39). The expressions $C_{ext,gs}$ and $C_{ext,gd}$ are then added to the expressions of the intrinsic capacitances C_{gs}, C_{sg} and C_{gd}, C_{dg}, respectively.

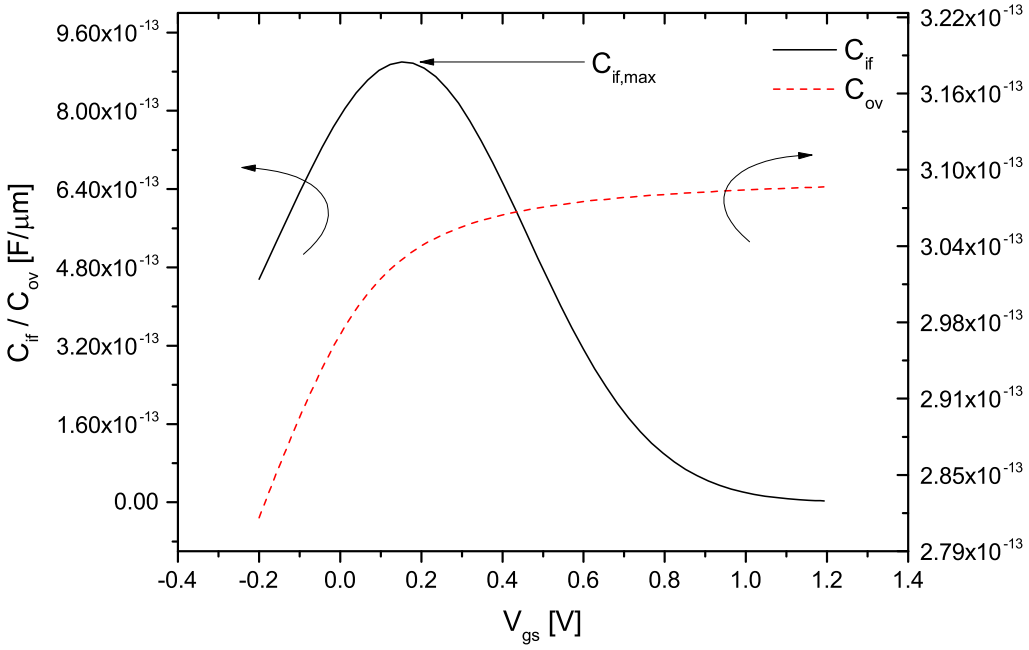


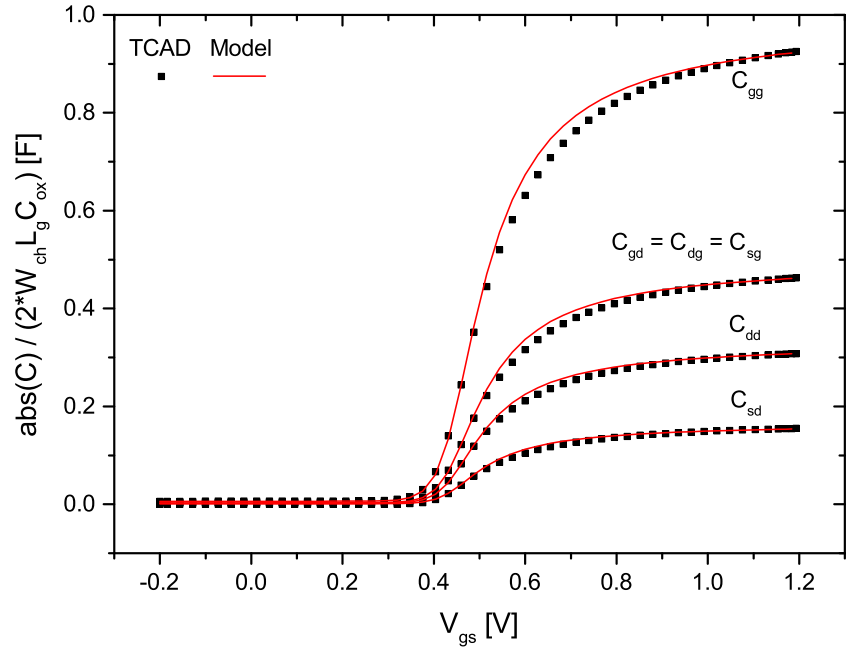
Figure 5.3: Inner fringing and gate overlap capacitance of an IM DG n-MOSFET. Parameters: $V_{ds} = 0.05\,\mathrm{V}$, $V_{gs} = -0.2\,\mathrm{V}$ to $1.2\,\mathrm{V}$, $N_a = 10^{15}\,\mathrm{cm}^{-3}$, $L_g = 100\,\mathrm{nm}$, $L_{sd} = 10\,\mathrm{nm}$, $T_{ch} = 10\,\mathrm{nm}$, $T_{ox} = 2\,\mathrm{nm}$. In this example L_d was set to 1 nm. Lines model.

5.4 AC Model Validation and Discussion

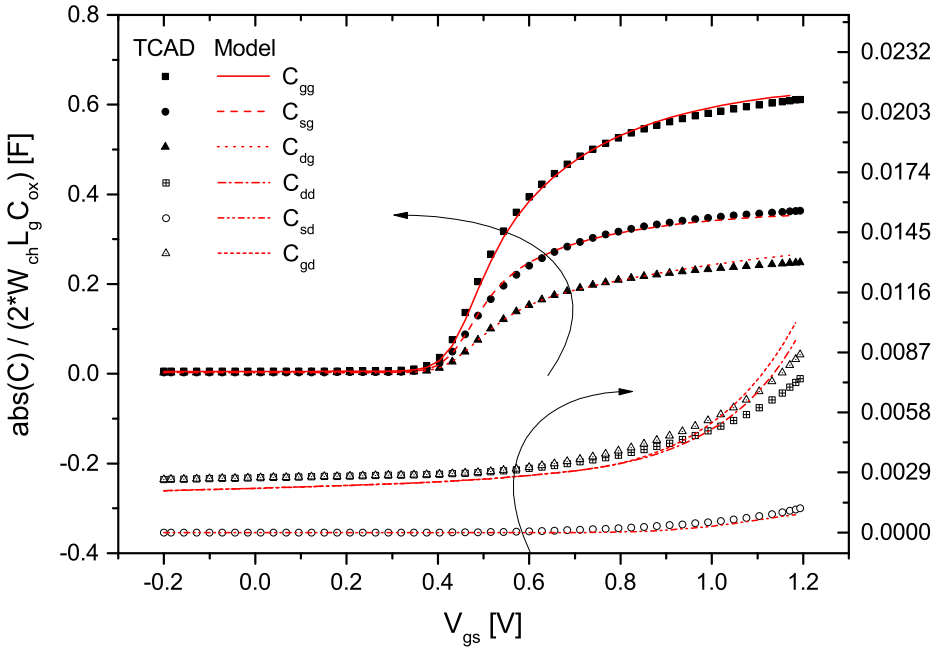
The following figures show the behavior of the capacitances of inversion mode and junctionless DG MOSFETs. The capacitances are shown in absolute values and are normalized by $(2 \cdot W_{ch}\, L_g\, C_{ox})$. The adjustable parameters for the calculation of the extrinsic capacitances are kept constant in all cases ,i.e. $L_d = 3\,\mathrm{nm}$, $\delta = 0.1$ and $C_{if,max} = 3 \cdot 10^{-14}\,\mathrm{F}$. The outer fringing capacitance C_{of} is calculated to zero due to the ideal device structure, where the gate electrodes are directly placed on top of the insulator without using any gate stack ($T_{gate} = 0\,\mathrm{nm}$). The AC model is compared versus numerical 2-D TCAD Sentaurus simulation data [34]. To ensure that the quasi-static condition holds, the frequency in the simulations is set to $f = 1\,\mathrm{MHz}$. The devices under investigation have various channel lengths, whereby $W_{ch} = 1\,\mu\mathrm{m}$. The simulations are done at $T = 300\,\mathrm{K}$, using a standard drift-diffusion transport model. QEs are neglected and a constant mobility $\mu = 100\,\mathrm{cm}^2/\mathrm{Vs}$ is assumed in the simulations and in the model.

5.4.1 Capacitances in Inversion Mode DG MOSFETs

Figure 5.4 shows the capacitances of an inversion mode DG MOSFET with a gate length equal to its width ($L_g = W_{ch} = 1\,\mu\mathrm{m}$). The n-type source/drain doping is $N_{sd} = 1 \cdot 10^{20}\,\mathrm{cm}^{-3}$.



(a)



(b)

Figure 5.4: Normalized capacitances (absolute values) of the IM DG MOSFET. (a) $V_{ds} = 0\,\mathrm{V}$ and (b) $V_{ds} = 1\,\mathrm{V}$ with: $N_a = 1 \cdot 10^{15}\,\mathrm{cm}^{-3}$, $L_g = 1000\,\mathrm{nm}$, $L_{sd} = 10\,\mathrm{nm}$, $T_{ch} = 10\,\mathrm{nm}$, $T_{ox} = 2\,\mathrm{nm}$. Symbols TCAD; lines model.

The investigations are done for two cases: (a) zero drain voltage, where the capacitance is described by its asymptotic value and (b) high drain voltage. A very good agreement can be observed between the analytical model and the reference data. In part (b) of Fig. 5.4, the capacitances C_{dd}, C_{sd} and C_{gd} are related to the right y-axis, using a smaller scale to detail their behavior.

By decreasing the channel length down to $L_g = 100\,\text{nm}$, the model still matches well the TCAD data. At zero drain voltage (Fig. 5.5), the asymptotic value of the capacitances describes the capacitive behavior of the MOSFET sufficiently accurate. By investigating the subthreshold characteristics, it is obvious that the extrinsic capacitances must be taken into account in order to have a complete model. If the extrinsic parts would have been neglected, the capacitances would be zero in the subthreshold operating regime. Additionally, the extrinsic capacitances' gate bias dependency is well predicted by the model. The model predicts the capacitive behavior for high drain bias (Fig. 5.6) that is accurate enough except for some minor deviations around V_T.

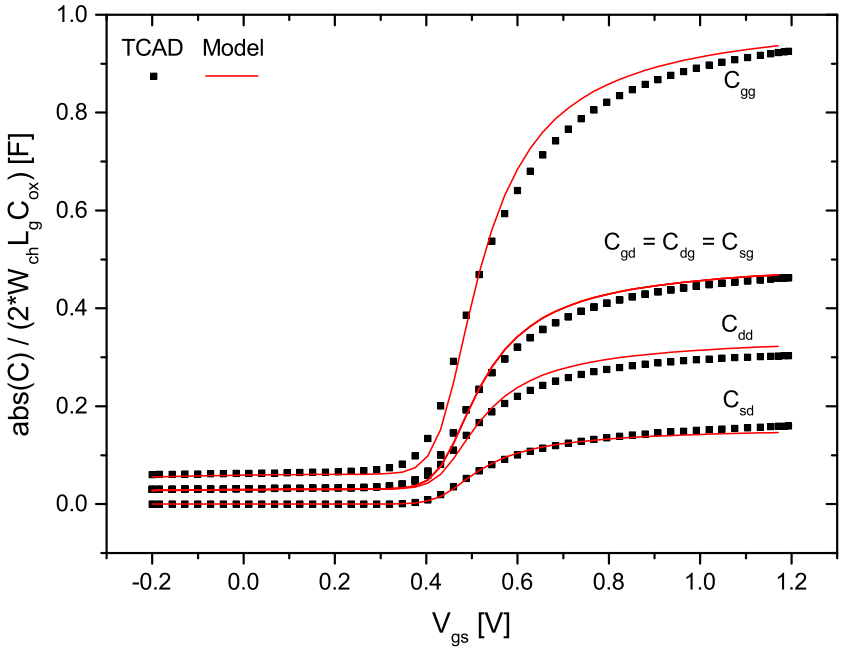


Figure 5.5: Normalized capacitances (absolute values) of the IM DG MOSFET. $V_{ds} = 0\,\text{V}$ with: $N_a = 1 \cdot 10^{15}\,\text{cm}^{-3}$, $L_g = 100\,\text{nm}$, $L_{sd} = 10\,\text{nm}$, $T_{ch} = 10\,\text{nm}$, $T_{ox} = 2\,\text{nm}$. Symbols TCAD; lines model.

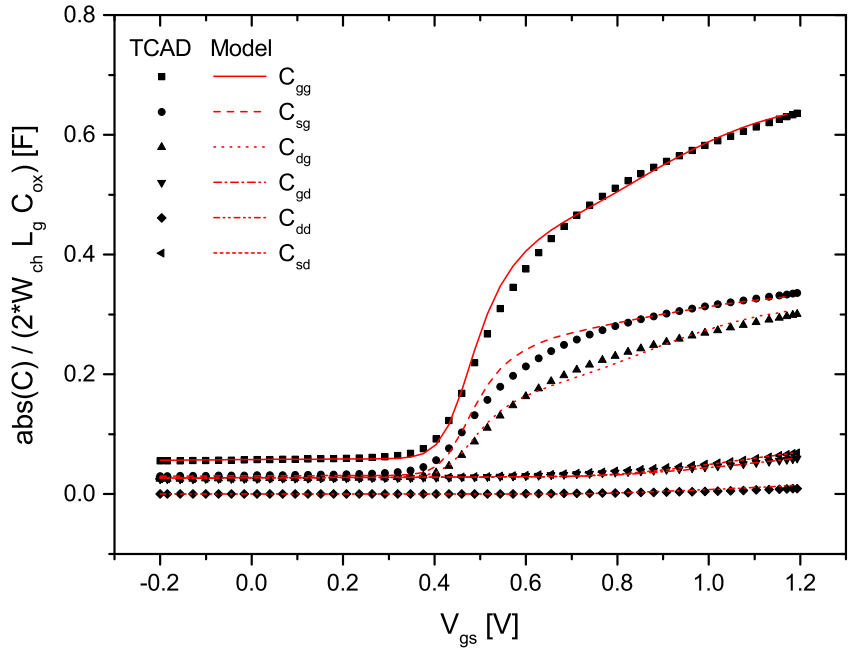
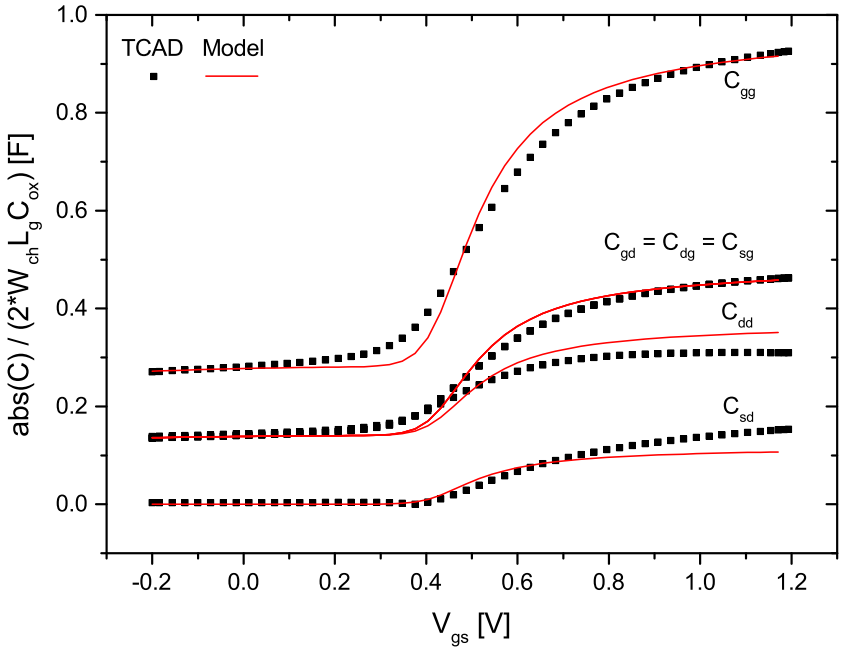
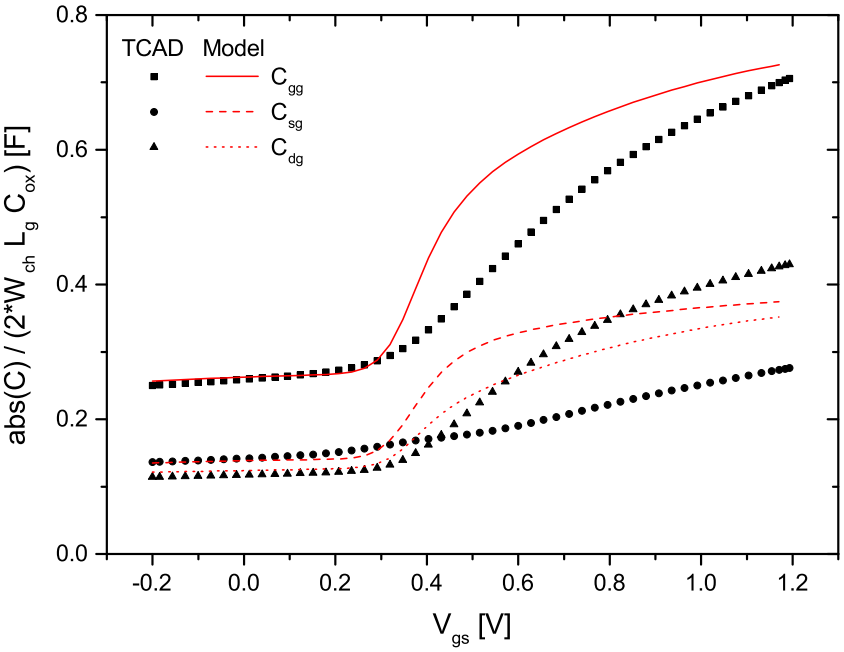


Figure 5.6: Normalized capacitances (absolute values) of the IM DG MOSFET. $V_{ds} = 1\,\mathrm{V}$ with: $N_a = 1 \cdot 10^{15}\,\mathrm{cm}^{-3}$, $L_g = 100\,\mathrm{nm}$, $L_{sd} = 10\,\mathrm{nm}$, $T_{ch} = 10\,\mathrm{nm}$, $T_{ox} = 2\,\mathrm{nm}$. Symbols TCAD; lines model.

At very short channel sizes the developed AC model reaches its limits. At $V_{ds} = 0\,\mathrm{V}$, the model gives acceptable results compared to the simulation data (Fig. 5.7(a)). At high V_{ds} (Fig. 5.7(b)) the modeled capacitive characteristics are correctly predicted for below threshold voltage. However, the model needs additional improvements for above threshold voltage (recalling that the drain current was shown to be in good agreement with TCAD data over the entire operating regime; compare with section 4.7.2). The increased impact of the drain depletion region onto the channel and in particular onto the total charges at the source modifies the capacitive behavior of the device. In particular, effects like the intersection of the source-gate and drain-gate capacitance curves, at some gate voltage, is not covered by the model. This might be due to the fact that the linear charge partition method does not hold for channel sizes where multidimensional effects cannot be ignored. A possible way to overcome these challenges is to use the conformal mapping technique for modeling the capacitances in such short-channel devices, as done in [148]. Their model was shown to compare well with the simulation data. But unfortunately, they did not present model results for high drain voltages, which is the crucial part as can be seen from Fig. 5.7(b).



(a)



(b)

Figure 5.7: Normalized capacitances (absolute values) of the IM DG MOSFET. (a) $V_{ds} = 0\,\mathrm{V}$ and (b) $V_{ds} = 1\,\mathrm{V}$ with: $N_a = 1 \cdot 10^{15}\,\mathrm{cm}^{-3}$, $L_g = 22\,\mathrm{nm}$, $L_{sd} = 10\,\mathrm{nm}$, $T_{ch} = 10\,\mathrm{nm}$, $T_{ox} = 2\,\mathrm{nm}$. Symbols TCAD; lines model.

5.4.2 Capacitances in Junctionless DG MOSFETs

In the next figures the results for the different capacitances for the junctionless DG MOSFET are detailed for two different channel lengths ($L_g = 1\,\mu$m and 100 nm), as a function of the gate voltage. The drain voltage is set to 0 V and to 1 V, whereby the channel doping concentration is equal to $N_d = 1 \cdot 10^{19}\,\mathrm{cm}^{-3}$. The n-type source/drain doping is unchanged $N_{sd} = 1 \cdot 10^{20}\,\mathrm{cm}^{-3}$.

Figure 5.8 shows the capacitances at zero drain voltage. The capacitances are described by their asymptotic value (compare with Eq. 5.33). First, the characteristic S-shape, typical for JL devices, is clearly visible. It arises due to the transition from the depletion to the accumulation regime (volume to surface conduction) where the effective gate capacitance is described by C_{eff} and C_{ox}, respectively. Second, some deviations between the model and the TCAD data can be noticed in the partly depleted regime of the JL device, which is $V_T < V_{gs} < V_{fb}$. These deviations might be owed to the non-quadratic Q-V relationship which is used in the developed model (as it was described in [98]). However, by focusing on the same capacitances at high $V_{ds} = 1$ V, one can observe a better agreement between both the model and the simulation data.

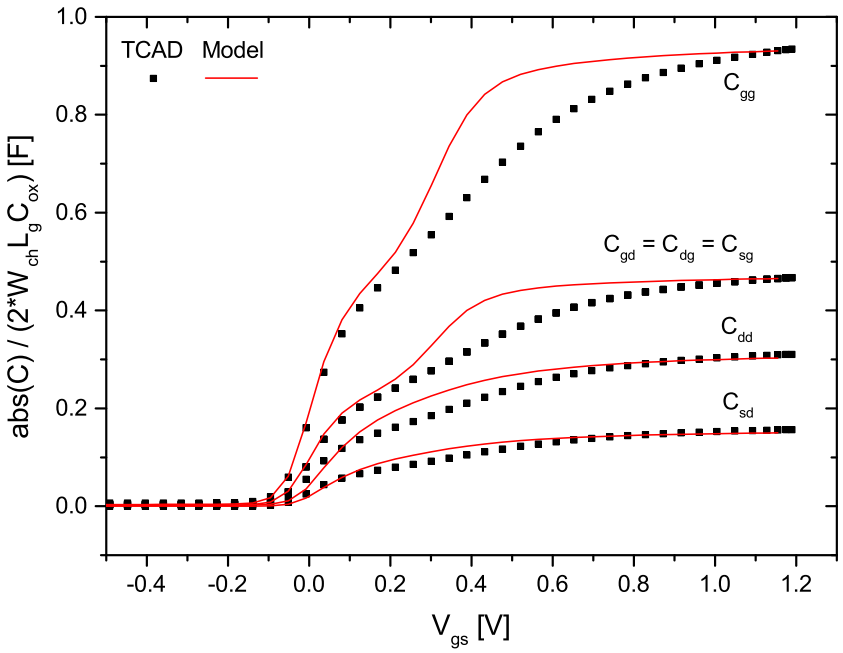


Figure 5.8: Normalized capacitances (absolute values) of the JL DG MOSFET. $V_{ds} = 0$ V with: $N_d = 1 \cdot 10^{19}\,\mathrm{cm}^{-3}$, $L_g = 1000$ nm, $L_{sd} = 10$ nm, $T_{ch} = 10$ nm, $T_{ox} = 2$ nm. Symbols TCAD; lines model.

The capacitances of the same device at $L_g = 100$ nm are shown in Figs. 5.10 and 5.11. The model shows some inaccuracies in the partly depleted operating regime at $V_{ds} = 0$ V.

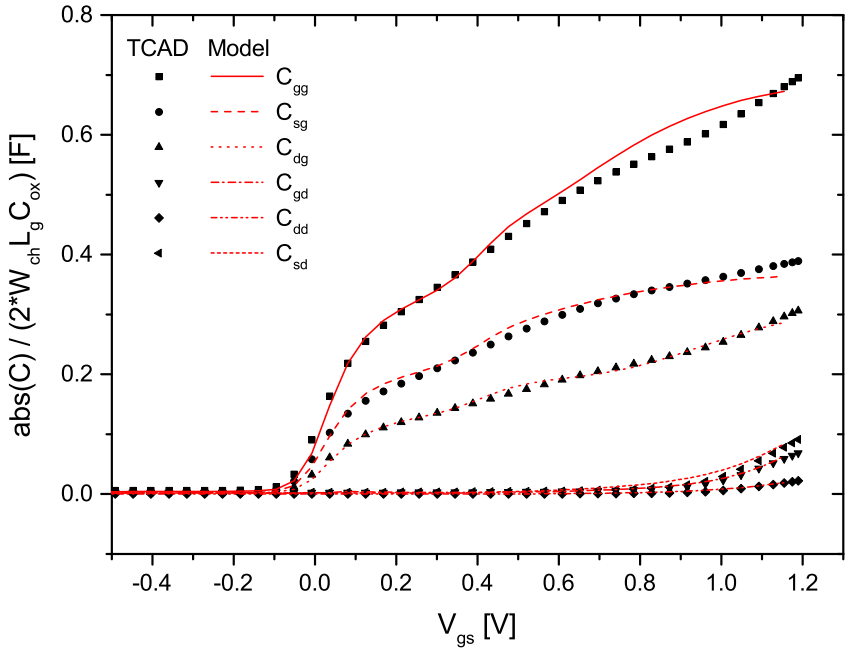


Figure 5.9: Normalized capacitances (absolute values) of the JL DG MOSFET. $V_{ds} = 1\,\mathrm{V}$ with: $N_d = 1 \cdot 10^{19}\,\mathrm{cm}^{-3}$, $L_g = 1000\,\mathrm{nm}$, $L_{sd} = 10\,\mathrm{nm}$, $T_{ch} = 10\,\mathrm{nm}$, $T_{ox} = 2\,\mathrm{nm}$. Symbols TCAD; lines model.

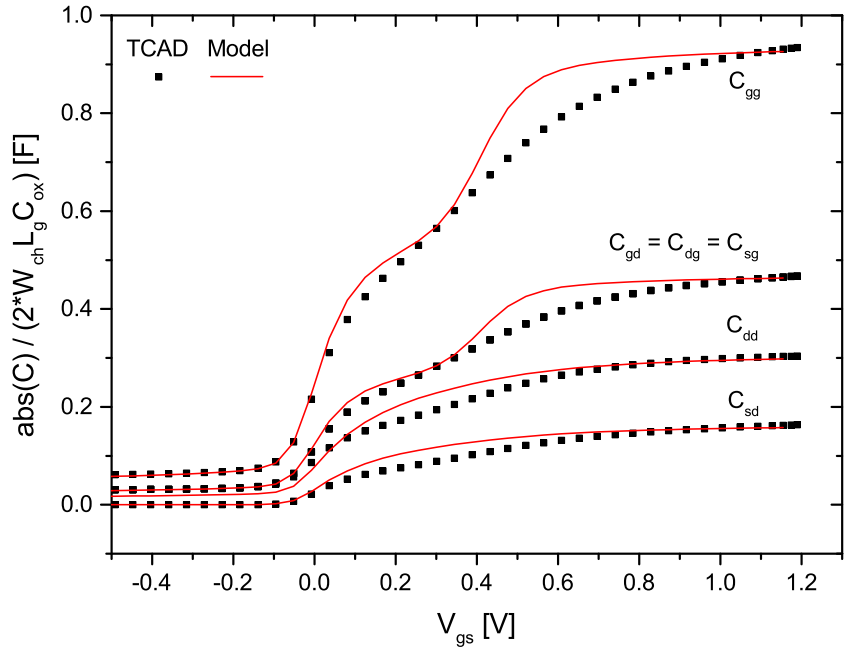


Figure 5.10: Normalized capacitances (absolute values) of the JL DG MOSFET. $V_{ds} = 0\,\mathrm{V}$ with: $N_d = 1 \cdot 10^{19}\,\mathrm{cm}^{-3}$, $L_g = 100\,\mathrm{nm}$, $L_{sd} = 10\,\mathrm{nm}$, $T_{ch} = 10\,\mathrm{nm}$, $T_{ox} = 2\,\mathrm{nm}$. Symbols TCAD; lines model.

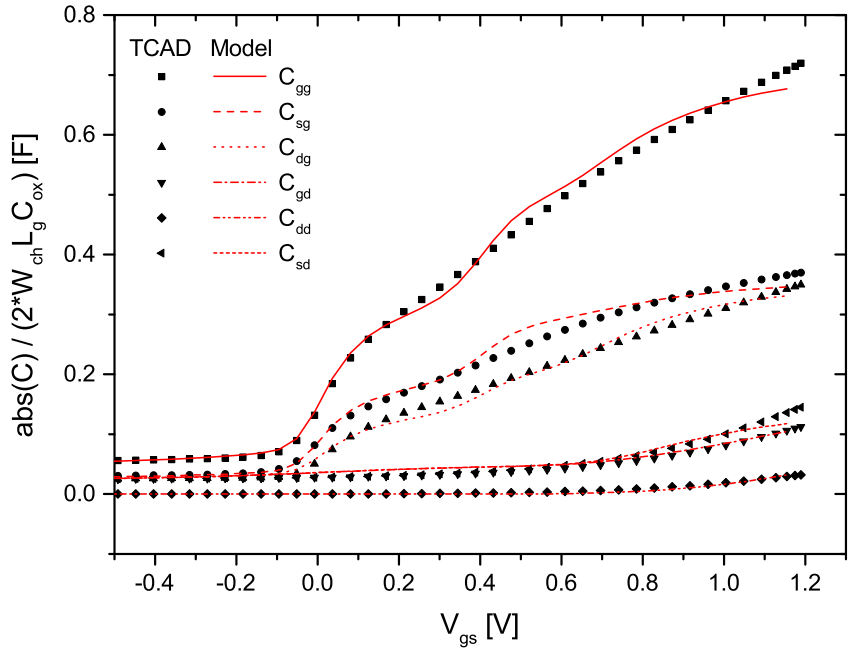


Figure 5.11: Normalized capacitances (absolute values) of the JL DG MOSFET. $V_{ds} = 1\,\mathrm{V}$ with: $N_d = 1 \cdot 10^{19}\,\mathrm{cm}^{-3}$, $L_g = 100\,\mathrm{nm}$, $L_{sd} = 10\,\mathrm{nm}$, $T_{ch} = 10\,\mathrm{nm}$, $T_{ox} = 2\,\mathrm{nm}$. Symbols TCAD; lines model.

CHAPTER 6

Quantization Effects in Nanoscale DG MOSFETs

This chapter focuses on the performance of nanoscale junctionless and inversion mode double-gate MOSFETs regarding quantization effects (QEs). The study is performed using the 2-D analytical model approach presented in chapter 4, and an extension for the inclusion of carrier quantization effects. The model itself is physics-based, predictive and valid in all operating regimes. Important device characteristics such as the drain-induced barrier lowering, subthreshold slope, the I_{on}/I_{off} ratios and continuity of the drain current I_{ds} at derivatives of higher-order (up to third-order) are in focus and discussed. The model is compared against 2-D numerical simulation results from TCAD Sentaurus [34]. To stand the pace with recent ITRS requirements for future CMOS technology [21], devices with a minimum channel length of 16 nm and channel thicknesses down to 3 nm are targeted. The performances of both device types will be compared and investigated. The purpose of this chapter is to gain knowledge about the device's performance at such aggressively scaled dimensions. In order to support the technology development and optimization and to reduce time and costs, the development of compact models which account for carrier quantization effects, in particular for such devices, is an urgent task.

6.1 Modeling of Carrier Quantization Effects

The aggressive scaling of nowadays MOSFETs requires ultra-thin oxides and high channel doping levels for minimizing the drastic increase of short-channel effects. The direct consequence is a strong increase of the electric field at the silicon-to-oxide interface, which creates a steep potential well. Therein the carrier energy is quantized, wherefore the charge carriers are confined in a vertical direction in a quantum well. This effect gives rise to a splitting of the energy levels into sub-bands. The lowest of the allowed energy levels in the well does therefore not coincide with the bottom of the conduction or the top of the valence band (see Fig. 6.1) [149–151].

In DG MOSFETs this potential well is defined by the tow gates. The carriers are confined due to two main phenomena: 1) strong electric field at the interface leading to electric field-

induced quantum confinement and 2) structural confinement due to the narrow potential well defined by the channel thickness [151]. For that reason, not only SCEs such as the V_T roll-off, S degradation and DIBL are to be considered, but also quantization effects if the channel thickness T_{ch} is in the same order of magnitude as the de Broglie wavelength of the charge carriers. This usually happens for $T_{ch} < 10$ nm [31].

In order to account for QEs in such structures, a quantization correction term for both the JL and the IM DG MOSFET must be considered in the calculations. In the following, the main focus is on the threshold voltage V_T and the 2-D integral mobile charge density $Q_{m,2D}$, which are given by equation (4.58) and (4.67), respectively, since these parameters are mainly affected by carrier quantization effects. A previous comparison between the classical and the quantum approach clearly showed that, QEs must be taken into account in order to obtain a correct and predictive compact model for such devices [90].

The V_T correction term for the IM device is calculated from the distance of the first sub-band from the conduction band in an infinite potential well (assuming a flat bottom potential energy) [28].

$$\Delta E_{Q(IM)} = \frac{h^2}{8\, m_e\, {T_{ch}}^2}, \tag{6.1}$$

where h is Planck's constant and $m_e = 0.916 \cdot m_0$ is the longitudinal effective mass of electrons (with $m_0 = 9.11 \cdot 10^{-31}$ kg).

Contrary, it was shown that quantization effects in JL devices cannot be treated in the same manner, since in subthreshold region their channel is fully depleted, which leads to a bent potential in their cross-section [90]. Here, QEs are considered by decoupling Schroedinger's equation from Poisson's equation in subthreshold region and by neglecting the mobile charges. Schroedinger's equation is then solved for two extreme cases.

1. *Large* T_{ch}: the system behaves like a quantum harmonic oscillator (QHO) and the discrete sub-band energy is mainly confined between the bent conduction band and boundaries. The effective-mass approximation is applied.

2. *Small* T_{ch}: the discrete sub-band energy is mainly confined between the side potential barriers. This makes the system behave like a quantum well (QW) surrounded by high potential barriers including a bottom perturbation potential (PP). The PP is obtained from the first-order of the time-independent perturbation theory [66].

For these two cases one obtains the following relations [90]:

$$\Delta E_{Q(JL),QHO} = \left((n-1) + \frac{1}{2}\right) \frac{h}{2\,\pi} \sqrt{\frac{q^2\, N_d}{m_e\, \varepsilon_{Si}}} \tag{6.2}$$

$$\Delta E_{Q(JL),QW+PP} = \frac{h^2\, n^2}{8\, m_e\, {T_{ch}}^2} + \frac{q^2\, N_d\, {T_{ch}}^2}{24\, \varepsilon_{Si}} \left(1 - \frac{6}{(n\,\pi)^2}\right), \tag{6.3}$$

where n is the quantum number (n = 1,2,3,...) and N_d is the channel doping concentration of the JL MOSFET. The transition between both cases can easily be calculated by solving $dE_{Q(JL),QW+PP}/dT_{ch} = 0$ for a given n and N_d.

$$T_{ch,trans} = \left(\frac{3\,\varepsilon_{Si}\,h^2\,n^2}{q^2\,N_d\,m_e\,a} \right)^{1/4} \tag{6.4}$$

$$a = \left(1 - \frac{6}{(n\,\pi)^2} \right) \tag{6.5}$$

Figure 6.1 schematically depicts the band diagram of a JL DG MOSFET, including the important parameters for the consideration of carrier QEs.

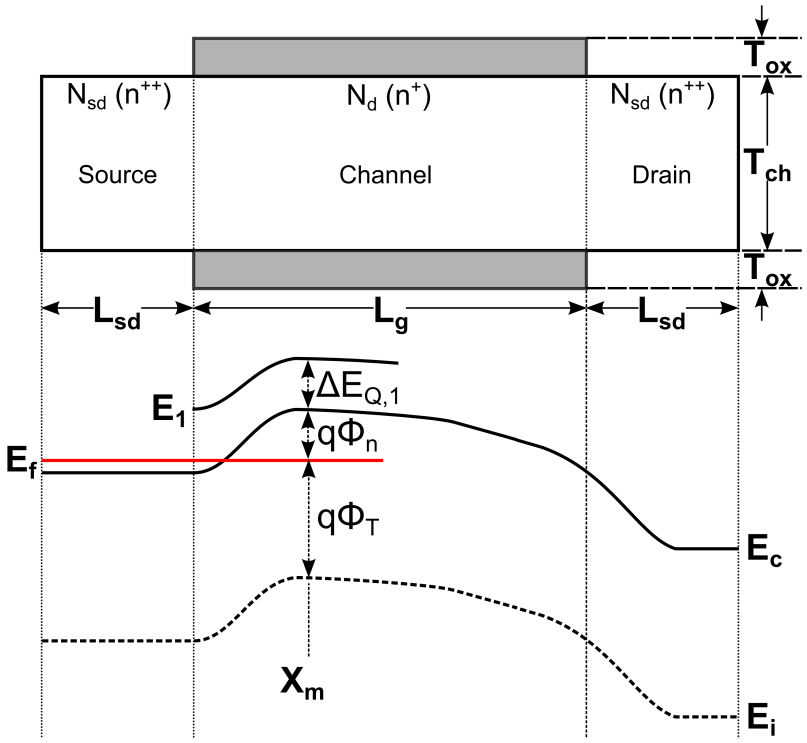


Figure 6.1: The upper figure shows the longitudinal cross-section of a JL DG MOSFET including its doping profile. The band diagram from source to drain is schematically drawn below, whereby the parameter ϕ_T is defined by equation (4.57). It should be noted that the Fermi level in source region lies above the conduction band, due to the high source/drain doping concentration. The parameter ϕ_n represents the difference between the Fermi level E_f and the conduction band E_c, and $\Delta E_{Q,1}$ between the conduction band E_c and the first discrete sub-band energy level E_1 inside the channel region at the potential barrier. x_m represents the position of the potential barrier inside the channel region (from source-channel junction).

6.1.1 Quantum Corrected Threshold Voltage

By adapting equations (6.1), (6.2) or (6.3) - depending on the device type and the given channel thickness - to Eq. (4.58), one gets a quantum corrected threshold voltage model $V_{T,Q}$. Since the main conduction mechanism of an IM MOSFET relies on a surface current, $V_{T,Q}$ is defined in terms of the 2-D surface potential ϕ_s. In contrast to the standard IM MOSFET, the main conduction mechanism in JL MOSFETs relies on a bulk current, wherefore $V_{T,Q}$ is defined in terms of the 2-D center potential ϕ_c instead of the surface potential. $V_{T,Q}$ is then calculated to:

$$V_{T,Q(JL/IM)} = V_g^* + dV_g \left(\frac{\left(\phi_T + \left(\Delta E_{Q(JL/IM)}/q\right)\right) - \phi_{(c/s)}(V_g^*)}{\phi_{(c/s)}(V_g^* + dV_g) - \phi_{(c/s)}(V_g^*)} \right), \tag{6.6}$$

whereby the parameter ϕ_T is approximated by equation (4.57).

6.1.2 Quantum Corrected 2-D Mobile Charge Density

To take into account carrier quantization effects in the 2-D integral mobile charge density equations (6.1), (6.2) or (6.3) are adapted, wherefore the 2-D quantum corrected integral mobile charge density $Q_{m,2D,Q}$ (per unit area) for both device types is received.

$$Q_{m,2D,Q(JL/IM)}\left(V_{T,Q(JL/IM)}\right) = q\, n_i \cdot f_{Q_{m,2D}} \cdot \exp\left(\frac{\left(\phi_s\left(V_{T,Q(JL/IM)}\right) - \left(\Delta E_{Q(JL/IM)}/q\right)\right)}{V_{th}} \right) \tag{6.7}$$

$$f_{Q_{m,2D}} = \exp(g_{Q_{m,2D}}) \cdot \left(\frac{\sqrt{\pi}\, T_{ch}/2}{2\sqrt{g_{Q_{m,2D}}}} \right) \cdot \operatorname{erf}\left\{ \sqrt{g_{Q_{m,2D}}} \right\} \tag{6.8}$$

$$g_{Q_{m,2D}} = \operatorname{abs}\left(\frac{\phi_c\left(V_{T,Q(JL/IM)}\right) - \phi_s\left(V_{T,Q(JL/IM)}\right)}{V_{th}} \right) \tag{6.9}$$

From Eq. (6.9) one can see that, including QEs in the calculations results in a reduced number of charge carriers, which is consistent with what is generally expected. From a physical point of view, the first sub-band is located above the edge of the conduction band E_c, leading to a smaller number of charge carriers. Or in other words, the first sub-band considered is located farer away from the electron quasi-Fermi level in the channel region than E_c, giving rise to the mentioned effect (compare with Fig. 6.1). In order to calculate the drain current including carrier quantization effects, equation (4.67) from section 4.5 is replaced by Eq. (6.9).

It will be proved that, compared to TCAD simulation data, the simple modification of the threshold voltage and the 2-D integral mobile charge density returns accurate results. The developed QE model is therefore verified in all regions of device operation for both the JL and the IM DG MOSFET.

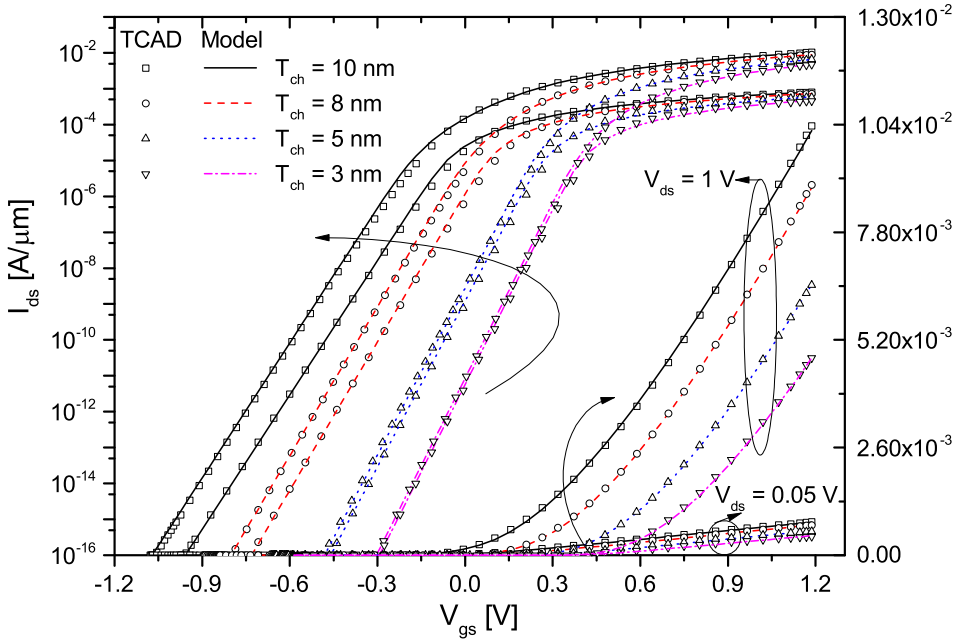
6.2 Performance Analysis and Discussions

In this section the model versus the simulation results are presented. A comparison of the performances of both devices is performed. Important device parameters such as S, DIBL and the I_{on}/I_{off} ratios are in focus of the discussion. For the JL device a channel doping concentration $N_d = 10^{19}\,\mathrm{cm}^{-3}$ (highly doped) is chosen and for the IM device $N_a = 10^{15}\,\mathrm{cm}^{-3}$ (lightly doped). All other parameters (structural and electrical) are identical - in the model and the simulations. As references serve 2-D TCAD Sentaurus simulations with an activated density gradient model (DGM) to take into account QEs. The following settings are applied to the simulations and to the model: constant mobility ($\mu = 100\,\mathrm{cm}^2/\mathrm{Vs}$), $T = 300\,\mathrm{K}$, del Alamo band gap narrowing model (in case of JL MOSFETs) and a device width of $W_{ch} = 1\,\mu\mathrm{m}$. The gate tunneling current and wave-function penetration into the dielectric are not considered in order to simplify the issue. For the calculation of QEs we will only focus on the first sub-band, where most of the charge carriers are confined [151]. Both devices have a $\langle 100 \rangle$ crystal orientation.

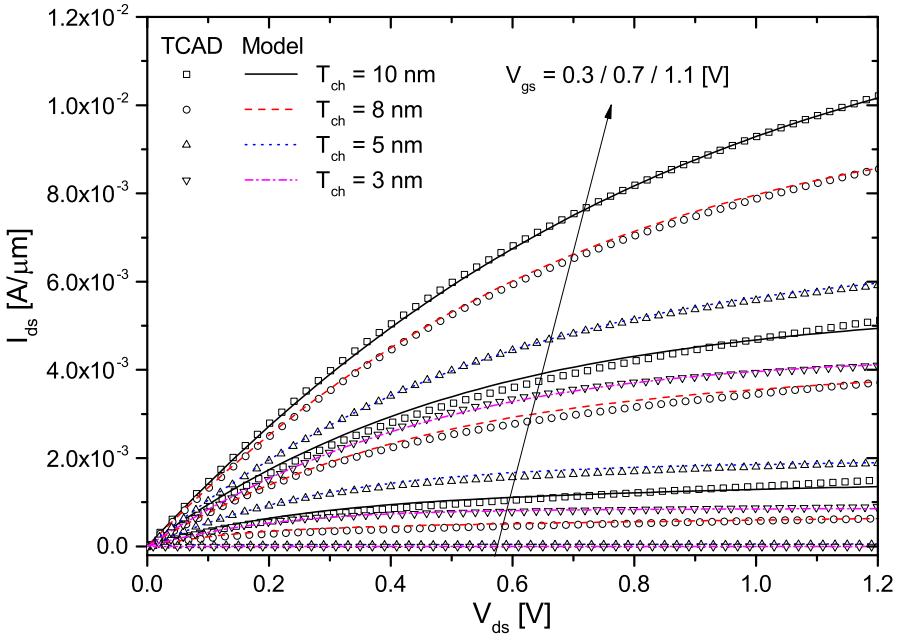
By focusing on the following Figures, one can see that the model matches well with the simulation data for the JL and the IM DG MOSFET. To pinpoint the effect of QEs on both devices the channel thickness is scaled from 10 nm down to 3 nm, where it can be observed that the applied quantum models are valid for all presented cases. Through downscaling T_{ch}, the subthreshold slope and the threshold voltage are strongly affected, as one can see in the log-scale of Fig. 6.2(a). Additionally, the DIBL is found to be improve significantly. On the other hand, a decreasing T_{ch} increases the series resistances (since the device's cross-section area is reduced), which significantly lowers the maximum current I_{on} (to be observed in lin-scale).

The $I_{ds} - V_{ds}$ characteristics of the same device are content of Fig. 6.2(b), where the drain voltage is swept up to 1.2 V for various gate-source voltages. The non-saturating current at high V_{ds} and V_{gs} for all addressed channel thicknesses indicates, that SCEs are present. They arise mainly due to the increased impact of the drain depletion region onto the channel area. Some minor deviations between the model and the TCAD data for $T_{ch} = 10\,\mathrm{nm}$ at $V_{gs} = 0.3\,\mathrm{V}$ and $0.7\,\mathrm{V}$ can be observed, where the simulated results are more linear than the analytical model characteristics. However, it should be noticed that only the channel thickness was altered to obtain the results. All other model parameters were kept constant for all setups, as required for a predictive compact model.

In comparison, Fig. 6.3(a) and Fig. 6.3(b) detail the results of the transfer and output characteristics of the IM DG MOSFET, respectively. The calculated device parameters of the model are detailed in Table 6.1. The DIBL is defined by Eq. (4.60) and the slope degradation factor α by Eq. (4.77).

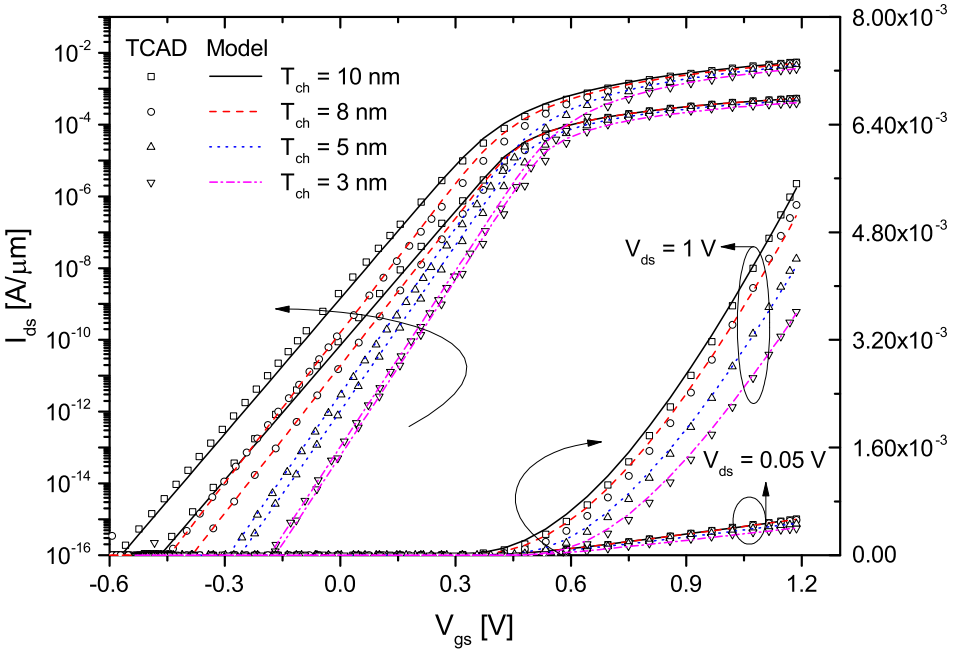


(a)

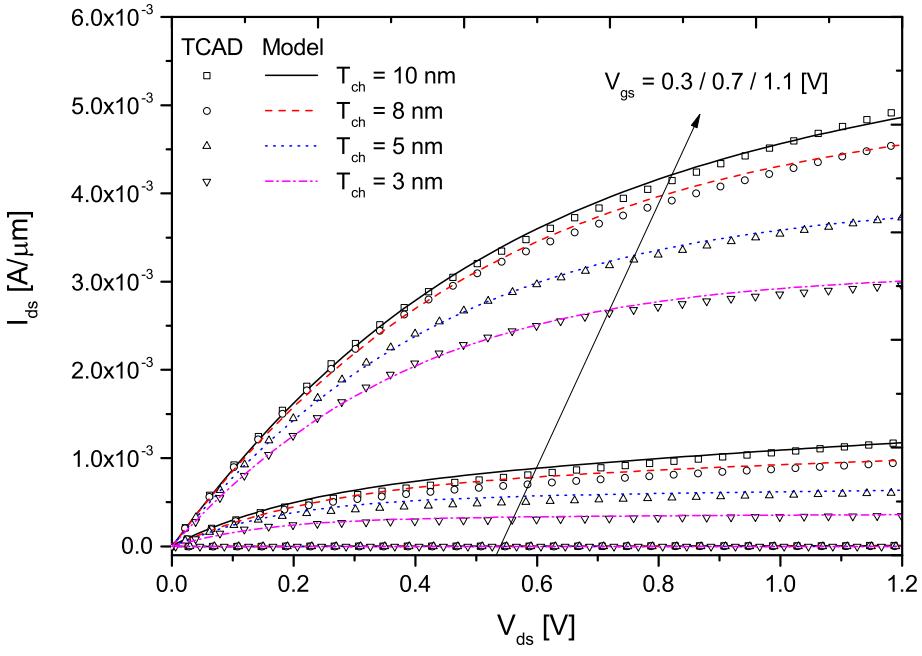


(b)

Figure 6.2: (a) $I_{ds} - V_{gs}$ characteristic of the JL DG MOSFET with: $N_d = 10^{19}\,\mathrm{cm}^{-3}$, $V_{ds} = 0.05\,/\,1\,[\mathrm{V}]$, $L_g = 22\,\mathrm{nm}$, $L_{sd} = 10\,\mathrm{nm}$, $T_{ch} = \mathrm{var.}$, $T_{ox} = 2\,\mathrm{nm}$. (b) $I_{ds} - V_{ds}$ characteristic of the device shown in (a). Symbols TCAD; lines model.



(a)



(b)

Figure 6.3: (a) $I_{ds} - V_{gs}$ characteristic of the IM DG MOSFET with: $N_a = 10^{15}\,\mathrm{cm}^{-3}$, all other parameters are identical to them of Fig. 6.2(a). (b) $I_{ds} - V_{ds}$ characteristic of the device shown in (a). Symbols TCAD; lines model.

Device	T_{ch} [nm]	V_T [V]	DIBL [mV]	S [mV/dev]	α [–]
JL	10	-0.036 / -0.176	140	80.1 / 79.7	1.35 / 1.34
IM	10	0.202 / 0.141	61	80.1 / 79.6	1.35 / 1.34
JL	8	0.108 / 0.022	86	72.6 / 72.4	1.22 / 1.22
IM	8	0.211 / 0.165	46	73.0 / 72.4	1.23 / 1.22
JL	5	0.302 / 0.265	37	64.9 / 64.7	1.09 / 1.09
IM	5	0.242 / 0.219	23	65.0 / 64.8	1.09 / 1.09
JL	3	0.409 / 0.395	14	61.6 / 61.5	1.03 / 1.03
IM	3	0.274 / 0.263	11	61.1 / 61.0	1.03 / 1.03

Table 6.1: Extracted electrical parameters from the model for the devices shown in Fig. 6.2(a) and 6.3(a). With V_T, S and α at $V_{ds} = 0.05 \,/\, 1\,[\mathrm{V}]$.

If the electrical parameters of both device types considered are directly compared (see Table 6.1) one finds that, in JL devices:

- V_T increases much stronger (V_T roll-off) with decreasing T_{ch} compared to their classical IM counterparts. In general, two reasons contribute to this behavior. First, the contribution of the last term of Eq. (6.3) which accounts for the PP and where the device's doping concentration is taken into account. This is not the case when considering IM devices (Eq. (6.1)). The term $(\Delta E_{Q(JL/IM)}/q)$ then has a much bigger influence on the calculations of V_T in Eq. (6.6). Second, the improved electrostatic control over the channel region due to its smaller cross section in both device types. From a physical point of view, the increase in V_T is the results of the minimized number of charge carriers when QEs are considered (compare with Eq. (6.9)). Anyway, this effect is not beneficial from the technology point of view, as the power supply voltages drop to lower levels in state-of-the-art MOSFET devices.

- The DIBL at $T_{ch} = 10\,\mathrm{nm}$ is approximately 140 mV compared to 61 mV in the IM device. As T_{ch} is scaled down, the DIBL in both devices improves significantly. At $T_{ch} = 3\,\mathrm{nm}$ this short-channel effect is less pronounced in both transistor types (14 mV compared to 11 mV). It is interesting to see that, at large channel thicknesses the DIBL in JL MOSFETs is much worse than in their IM counterparts, but improves quickly when scaling down T_{ch}.

- The subthreshold characteristics are almost identical with the one in IM devices. Hence, one can observe a similar behavior for the slope degradation factor α. Both devices show a near-ideal subthreshold slope S through scaling T_{ch} down to 3 nm. Noticeable is that, even though QEs come into play the subthreshold characteristics improve largely.

The overall effect when scaling down the channel thickness in the regime where QEs cannot be neglected is that, the device characteristics approach that of a long-channel device, i.e.,

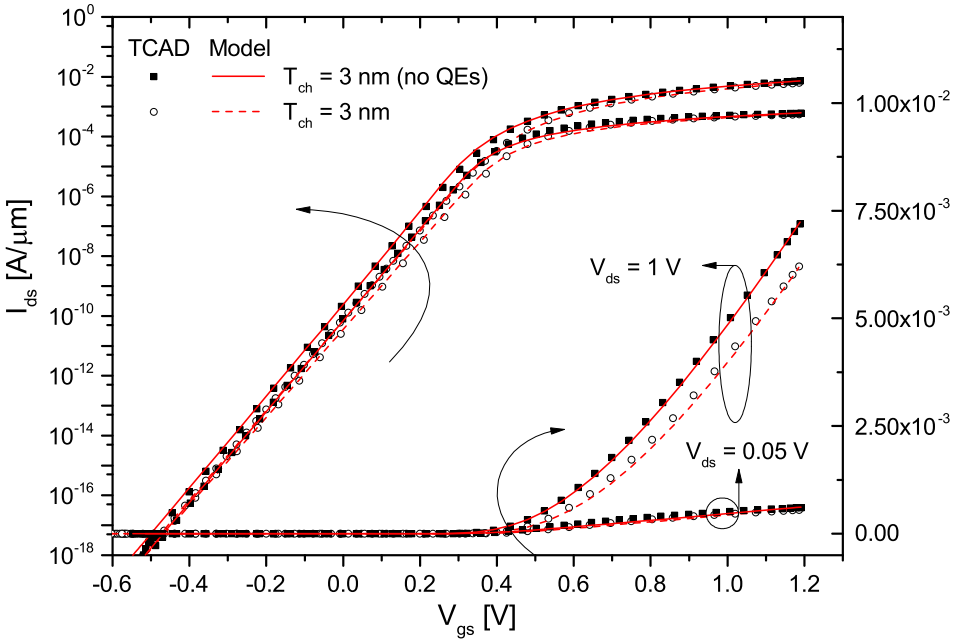
increased V_T, better DIBL and S. This happens although devices in the nanoscale regime are considered here. The reason for this behavior is that, as T_{ch} is reduced the close proximity of the source/drain depletion regions is widened and the space charge regions are decoupled, wherefore the center of the device's channel is depleted of charge carriers - which is comparable to the behavior of long-channel devices. Or in other words, the general electrical behavior of a short-channel device with a very small channel thickness is similar to that of a long-channel device. At the same time, in the case of JL devices (bulk conduction) the effect when scaling down the channel thickness is more clearly visible, because an effective cross-section area of the device is approximately proportional to T_{ch}. In the case of IM devices (surface conduction) the thinner ones almost operate in volume inversion mode, so for these devices the T_{ch} effect is stronger than for the thicker ones.

To pinpoint the necessity of considering QEs, the current characteristics for a JL DG MOSFET are presented, whereby the quantum model is switched on or off in both the TCAD simulator and the analytical model (Fig. 6.4(a) and 6.4(b)). A JL DG MOSFET with $L_g = 16\,\text{nm}$ and $T_{ch} = 3\,\text{nm}$ is targeted. On first sight, the model matches well the simulation data. Second, the shift in $V_T \approx 40\,\text{mV}$ (at $T_{ch} = 3\,\text{nm}$) and the related change in the current characteristic, when QEs are switched on or off, prove that one must take into account QEs at such small channel thicknesses. In addition, the DIBL and S are found to be not affected by QEs (see Table 6.2). Moreover, their improvement, as discussed previously, is a direct result of the downscaling channel thickness [152].

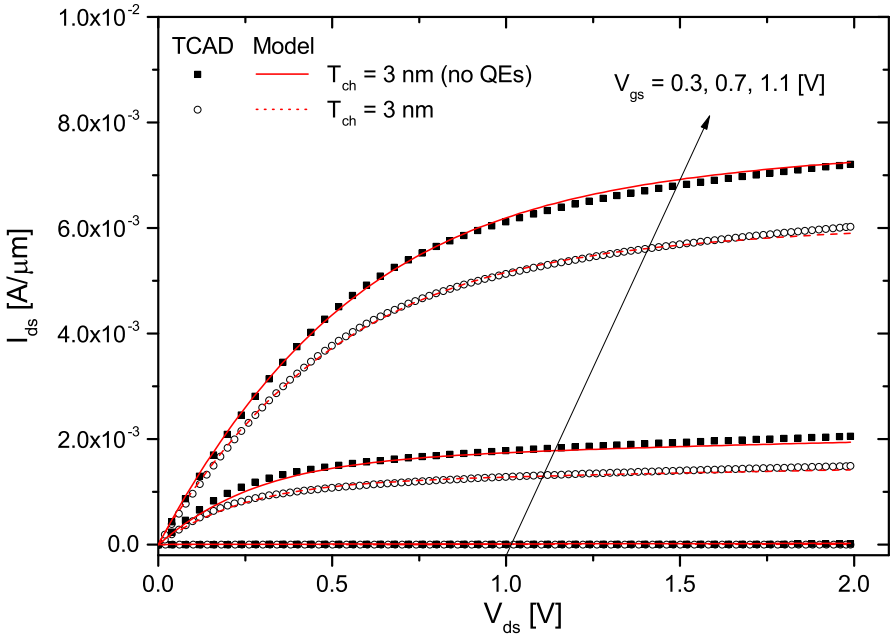
Device	T_{ch} [nm]	V_T [V]	DIBL [mV]	S [mV/dev]	α [–]
JL (no QEs)	3	0.36 / 0.31	50	65.7 / 65.3	1.10 / 1.08
JL	3	0.40 / 0.35	50	66.0 / 65.3	1.10 / 1.08

Table 6.2: Extracted electrical parameters from the model for the devices shown in Fig. 6.4(a) and 6.4(b). With V_T, S and α at $V_{ds} = 0.05\,/\,1\,[\text{V}]$.

Fig. 6.5(a) details the gate transconductance g_m for a 16 nm short-channel device with $N_d = 10^{19}\,\text{cm}^{-3}$ at low and high drain bias. Some discrepancies with the simulated TCAD data and the model occur in the saturation regime at high V_{gs}. However, no discontinuities are observed in the model. Concerning the drain conductance g_d, one can observe a fairly good agreement between the model and the TCAD data over the device's entire operating regime (Fig. 6.5(b)). For convenience the second- and third-order derivatives (in absolute values) of the same device are detailed in Figs. 6.6(a) and 6.6(b), where the model is shown to be still continuous.

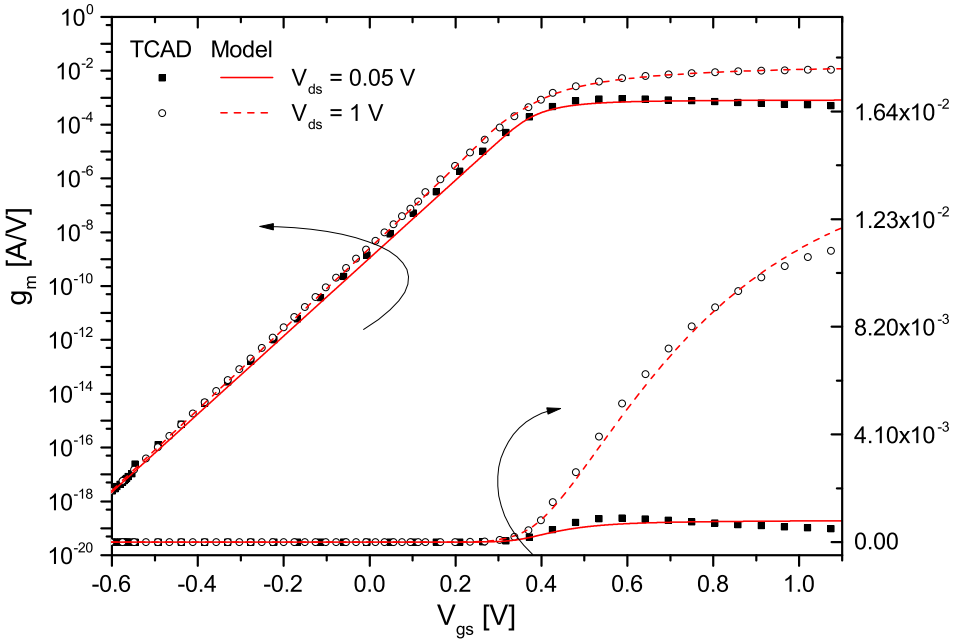


(a)

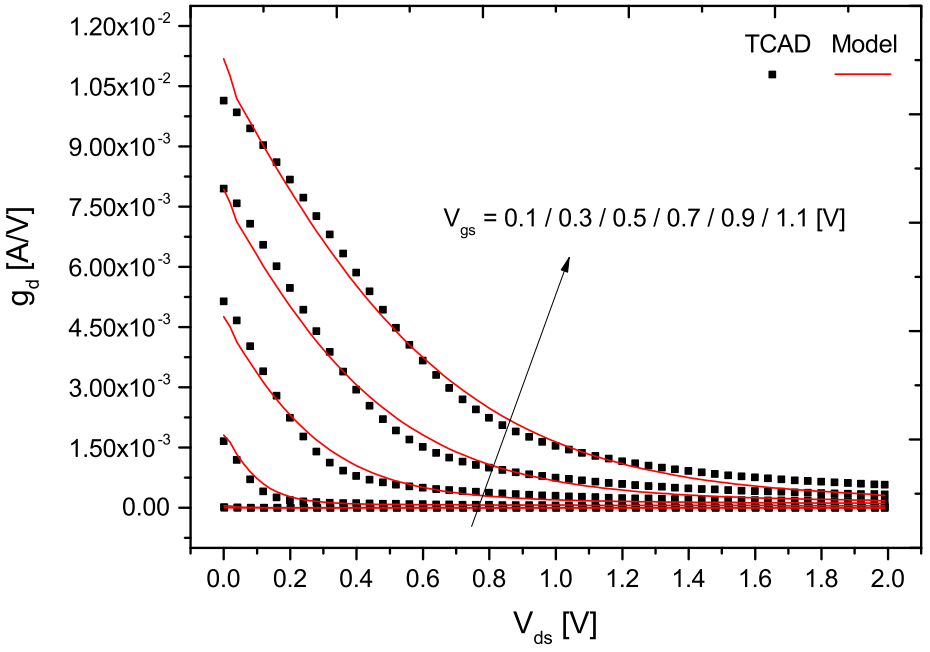


(b)

Figure 6.4: Difference between classical and quantum approach. (a) $I_{ds} - V_{gs}$ characteristic of the JL DG MOSFET with: $N_d = 10^{19}\,\mathrm{cm}^{-3}$, $V_{ds} = 0.05\,/\,1\,[\mathrm{V}]$, $L_g = 16\,\mathrm{nm}$, $L_{sd} = 10\,\mathrm{nm}$, $T_{ch} = 3\,\mathrm{nm}$, $T_{ox} = 2\,\mathrm{nm}$. (b) $I_{ds} - V_{ds}$ characteristic of the device shown in (a). Symbols TCAD; lines model.

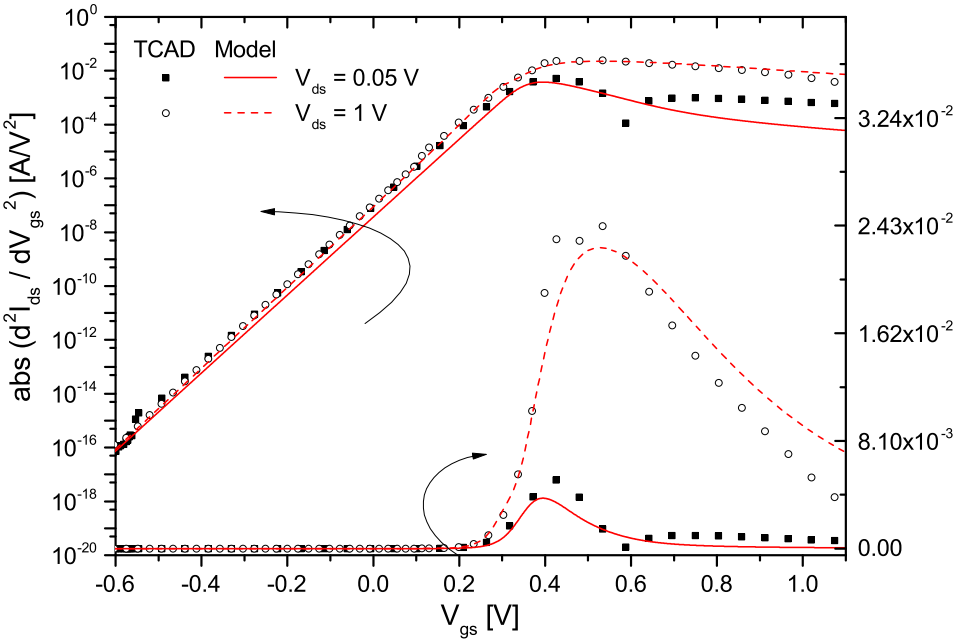


(a)

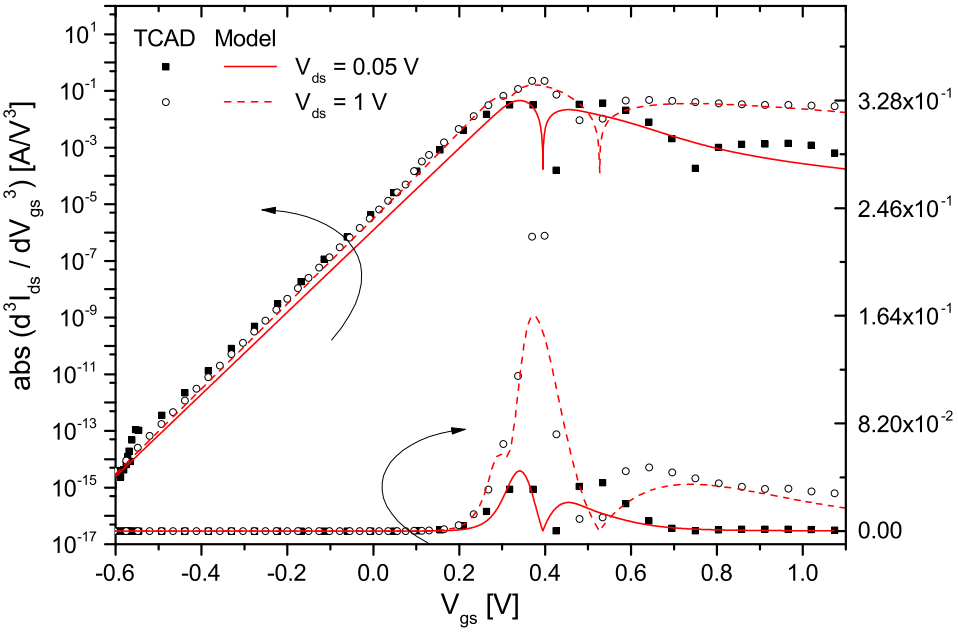


(b)

Figure 6.5: (a) Gate transconductance g_m of the JL DG MOSFET with: $V_d = 0.05\,/\,1\,[\mathrm{V}]$, $N_d = 10^{19}\,\mathrm{cm}^{-3}$, $L_g = 16\,\mathrm{nm}$, $L_{sd} = 10\,\mathrm{nm}$, $T_{ch} = 3\,\mathrm{nm}$, $T_{ox} = 2\,\mathrm{nm}$. (b) Drain conductance g_d of the same device with: $V_{gs} = 0.1\,\mathrm{V}$ to $1.1\,\mathrm{V}$ stepping $0.2\,\mathrm{V}$. Symbols TCAD; lines model.



(a)



(b)

Figure 6.6: (a) Second- and (b) third-order derivatives (absolute values) of the transfer characteristics of the device presented in Fig. 6.5(a). Symbols TCAD; lines model.

To obtain information about the I_{on}/I_{off} performances, their extraction method is presented as next. Having the aim to find the maximum current ratio within the whole gate voltage range for both the JL and IM DG MOSFET, a standard CMOS inverter (Fig. 6.7) is consulted, whereby $V_{DD} = 1$ V. Depending on the input voltage, the p-MOS or the n-MOS transistor will be conductive. The voltage drop at the conducting transistor is then assumed to be 0.2 V and 0.8 V at the other one. The voltage difference is then 0.6 V (ΔV_{gs}), which ensures a safe switching behavior [153].

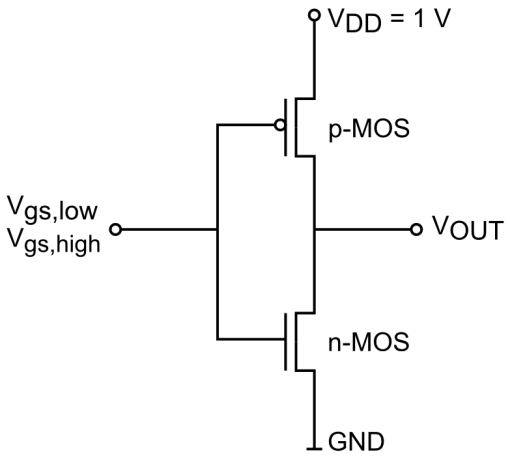


Figure 6.7: Standard CMOS inverter with V_{gs} as input and V_{OUT} as output voltage.

To maintain this safe switching behavior, the mentioned conditions are applied to the model, wherefore the following relations are obtained (Fig. 6.8). The OFF-current I_{off} in this example is given at $V_{gs} = 0.0$ V with $V_{ds} = 0.8$ V and the ON-current I_{on} at $V_{gs} = 0.6$ V with $V_{ds} = 0.2$ V. To get the maximum I_{on}/I_{off} ratio, the points $V_{g,low}$ and $V_{g,high}$ are shifted over the whole gate voltage range while maintaining $\Delta V_{gs} = 0.6$ V.

Figures 6.9(a) and 6.9(b) show the I_{on}/I_{off} ratios plotted over $\tilde{V}_{gs}$ (which is V_{gs} at extracted I_{on}) for various channel thicknesses from $T_{ch} = 10$ nm down to $T_{ch} = 3$ nm. On first sight, good ratios in both devices and for all presented cases are achieved. They are in the range of $1.2 \cdot 10^6$ up to $3.1 \cdot 10^9$, which is indeed very high. Second, it should be noticed that the maximum ON/OFF-current ratio is not located at a stationary gate voltage, but alters with T_{ch} (a similar behavior was found for an altering N_d in [153]). For that reason, work function engineering will be required to adjust the maximum ON/OFF-current ratio to desired values in the operating regime. Third, the maximum ratios in the IM devices are located slightly above threshold voltage. Contrary, in the JL devices they are located slightly below V_T, which is a results of the different device physics (see Table 6.3). In JL MOSFETs the main conduction mechanism relies on a bulk current (volume conduction), wherefore the device turns on earlier, without creating a surface accumulation layer as it is the case in IM MOSFETs (surface conduction). Equation

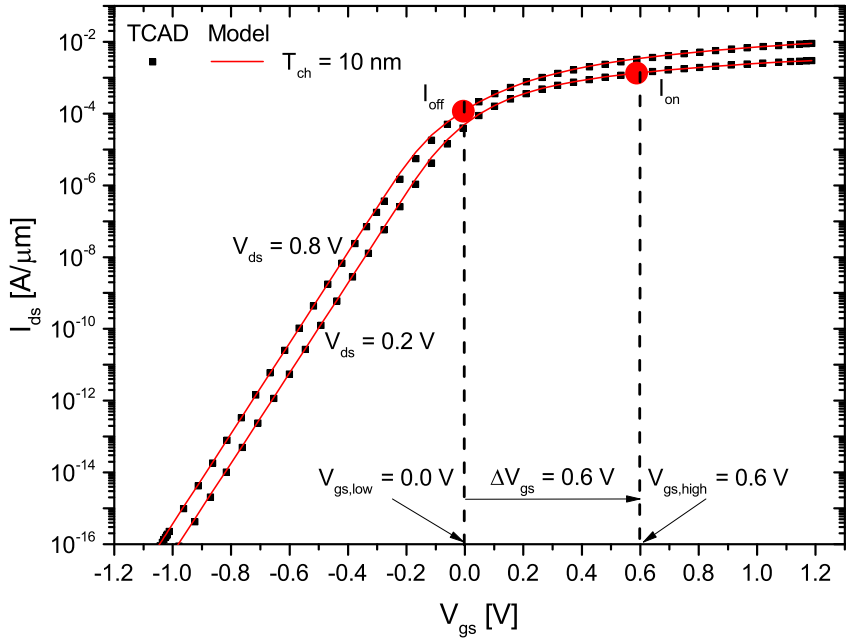
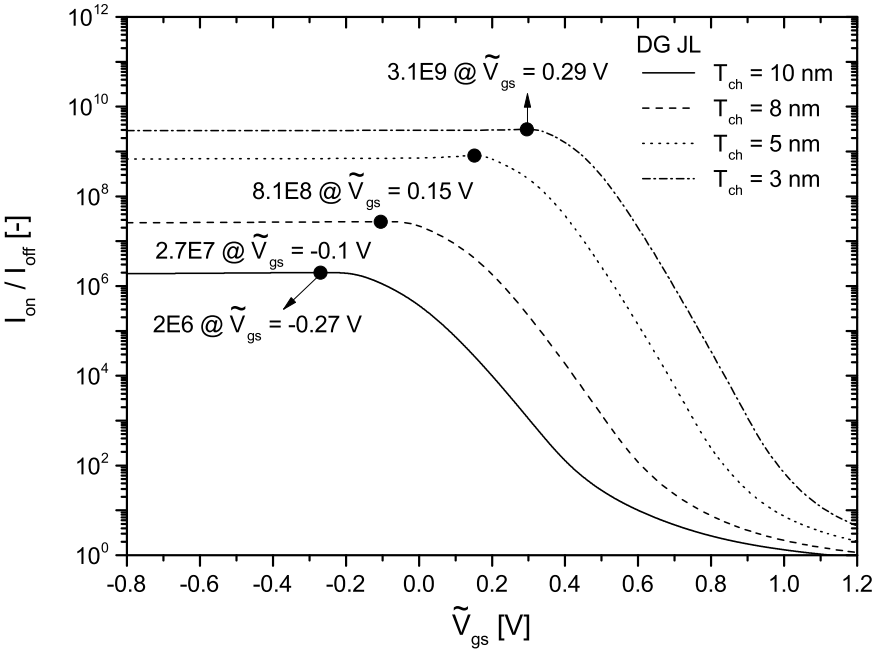


Figure 6.8: The I_{on}/I_{off} ratios of both device types are calculated from their $I_{ds} - V_{gs}$ characteristics. Parameters: $N_d = 10^{19}\,\mathrm{cm}^{-3}$, $V_{ds} = 0.2\,/\,0.8\,[\mathrm{V}]$, $L_g = 22\,\mathrm{nm}$, $L_{sd} = 10\,\mathrm{nm}$, $T_{ch} = 10\,\mathrm{nm}$, $T_{ox} = 2\,\mathrm{nm}$. Symbols TCAD; lines model.

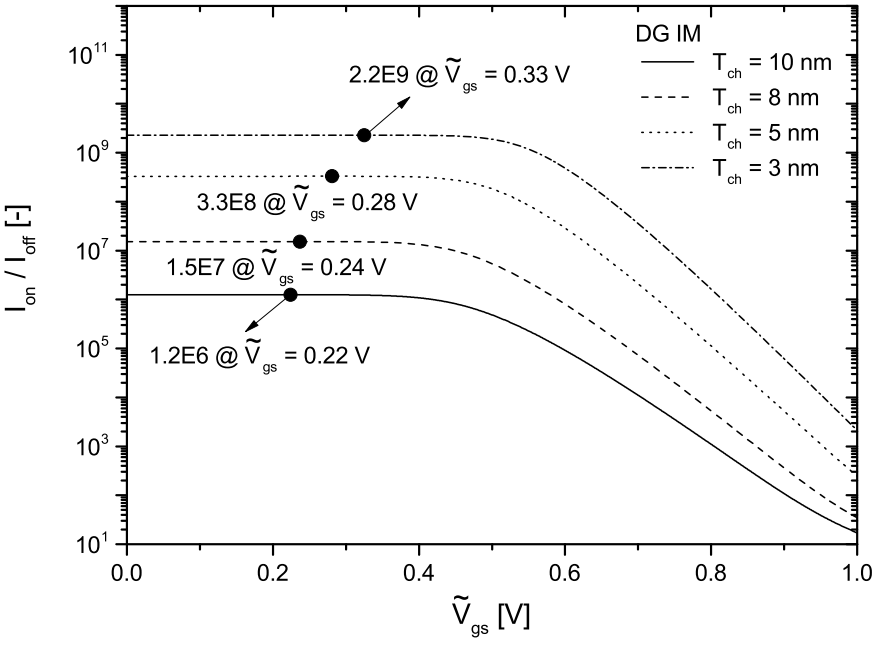
(6.6) is completely consistent with that fact. In addition, reducing the channel thickness is found to improve the ratios significantly. This is because S improves with decreasing T_{ch} and since the maximum I_{on}/I_{off} ratios are located around V_T, so that the decreased maximum output current, due to the increasing device resistances, is not of importance here.

Device	T_{ch} [nm]	V_T [V]	$\tilde{V}_{gs}$ at max. I_{on}/I_{off} [V]
JL	10	-0.036 / -0.176	-0.27
IM	10	0.202 / 0.141	0.22
JL	8	0.108 / 0.022	-0.1
IM	8	0.211 / 0.165	0.24
JL	5	0.302 / 0.265	0.15
IM	5	0.242 / 0.219	0.28
JL	3	0.409 / 0.395	0.29
IM	3	0.274 / 0.263	0.33

Table 6.3: V_T from the model in comparison with $\tilde{V}_{gs}$ at maximum I_{on}/I_{off} ratio. With V_T at $V_{ds} = 0.05\,/\,1\,[\mathrm{V}]$.



(a)



(b)

Figure 6.9: (a) JL DG MOSFET's, (b) IM DG MOSFET's I_{on}/I_{off} ratios plotted versus $\tilde{V}_{gs}$. The dots on the lines mark the value of the maximum ratio achievable for different channel thicknesses and the corresponding voltage. Lines model.

By applying the mentioned extraction method also to the simulation data obtained from TCAD one can observe that, by extracting and reorganizing the maximum I_{on}/I_{off} ratios of both devices, a direct comparison reveals that JL devices offer higher ratios than IM MOSFETs (Fig. 6.10). One can see that the model agrees well with the simulation data for all presented cases. From $T_{ch} = 10\,\text{nm}$ down to $T_{ch} = 3\,\text{nm}$ only small mismatches for both devices can be observed, whereby the predicted ratio is still in the same order of magnitude compared to TCAD data - keeping in mind that, slightest mismatches between the modeled and simulated current characteristics would produce large errors in the I_{on}/I_{off} ratios.

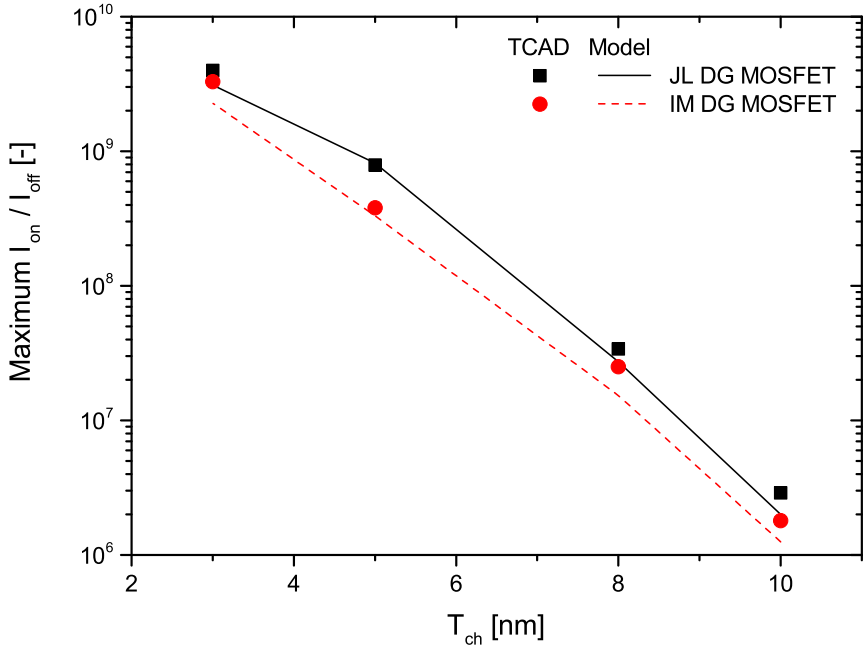


Figure 6.10: Maximum I_{on}/I_{off} ratios for both device types for different channel thicknesses T_{ch}. Symbols TCAD; lines model.

CHAPTER 7

Modeling of Nanoscale Junctionless Triple-Gate Nanowire MOSFETs

Compared to its double-gate counterparts the triple-gate MOSFET holds a much better electrostatic integrity (EI), due to the three gate electrodes, which surround the channel region of the device. For this reason it is considered as the most promising candidate in future CMOS technology [26]. Such kind of 3-D devices, which are also called FinFETs, were recently introduced in Intel's new microprocessors with codename: "Ivy bridge" [1]. Their channel length is shrunk down to 22 nm. An example of this device is depicted in Fig. 7.1.

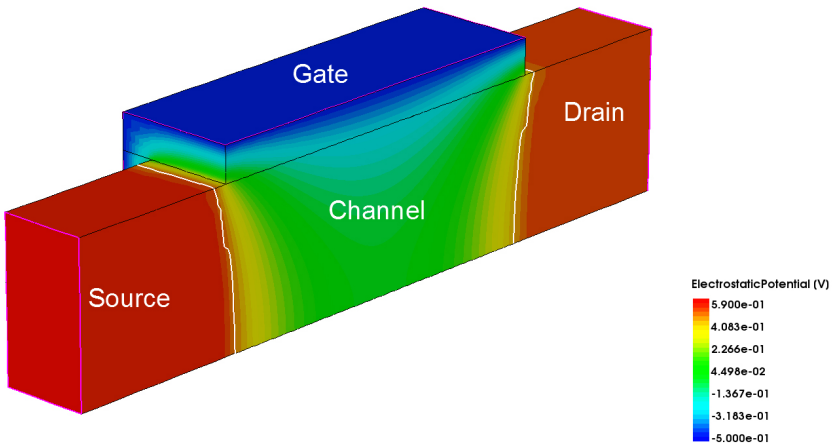


Figure 7.1: TCAD simulation of an ultra-scaled triple-gate nanowire MOSFET. Only half of the device structure is shown to allow for an insight into the device's channel region.

In this chapter a modeling extension for 3-D junctionless (JL) triple-gate nanowire (TG-NW) MOSFETs is presented. The model itself is physics-based and derived in closed-form, based on the model presented in chapter 4. Important short-channel and carrier quantization effects are directly taken into account. The model is verified versus TCAD simulation data [34] and measurement data, which were provide through the "SQWIRE" project, by the LETI in Grenoble, France. Additionally, important device characteristics such as symmetry around $V_{ds} = 0\,\mathrm{V}$ and continuity of the drain current I_{ds} are in focus.

7.1 Device Analysis

In this section a brief analysis of the mentioned device's electrostatic behavior is presented to the reader. Since junctionless devices have high channel doping concentrations, one might wonder if their electrical behavior is still similar to that of standard lightly-doped inversion mode triple-gate MOSFETs, or not. The investigations are done by analyzing a cross-sectional cut inside the device's channel center.

At first, the potential distribution inside the channel region is investigated. In Fig. 7.2 the gate voltage approximatively equals the threshold voltage ($V_{gs} = 0.0\,\mathrm{V} \approx V_T = -0.03\,\mathrm{V}$). One can see that the potential has its maximum at the bottom center inside the channel region, which means that the most leaky path is located there (one should remember that only half of the device structure is displayed). This behavior is identical to that of junction-based TG MOSFETs [138].

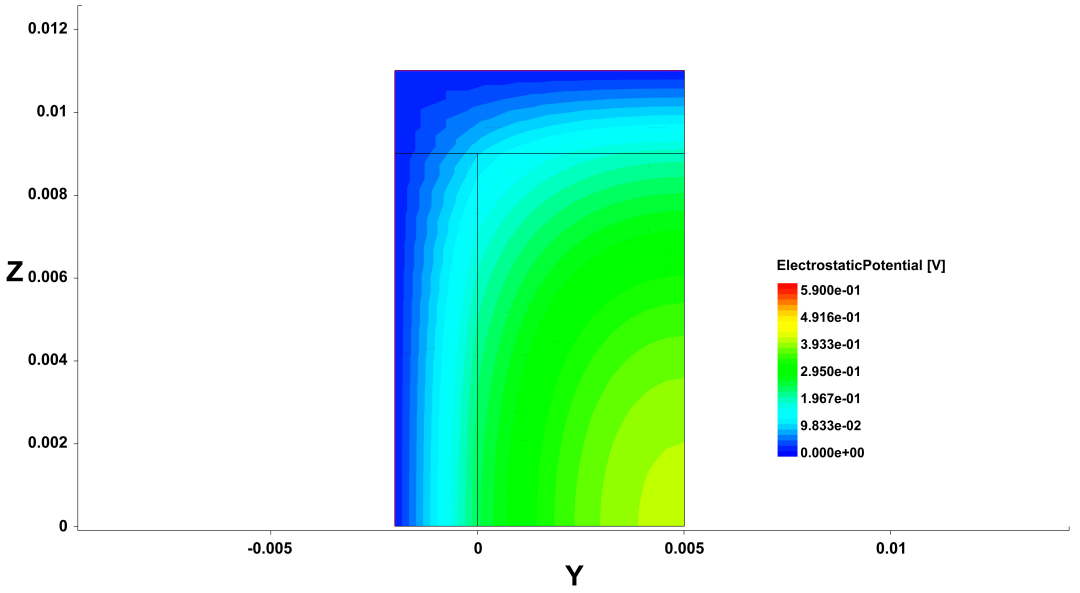


Figure 7.2: TCAD simulation results for the potential distribution of a JL TG-NW MOSFET, with $V_{gs} \approx 0\,\mathrm{V} \approx V_T$. Parameters: $N_d = 1 \cdot 10^{19}\,\mathrm{cm}^{-3}$, $V_{ds} = 0.05\,\mathrm{V}$, $L_g = 22\,\mathrm{nm}$, $L_{sd} = 10\,\mathrm{nm}$, $T_{ch} = 10\,\mathrm{nm}$, $T_{ox} = 2\,\mathrm{nm}$, $H_{ch} = 9\,\mathrm{nm}$.

As the gate voltage is increased to values well above threshold voltage ($V_{gs} = 0.5\,\mathrm{V} > V_T = -0.03\,\mathrm{V}$), the potential is almost evenly distributed over the entire channel region (Fig. 7.3). In this case the device is driven by a current flow in the entire channel cross-section (volume conduction).

By focusing on the electron current density (electrons are the majority charge carriers) at the same bias conditions, one can observe that the main current flow starts at the bottom center inside the device's channel region (Fig. 7.4), as expected from the previous analysis. And at larger gate biases the current density is evenly distributed over the entire channel cross-section

(Fig. 7.5). The outcome of this short analysis allows us to model the 3-D electrostatics in a similar way as presented in [27], where a lightly doped junction-based FinFET was considered.

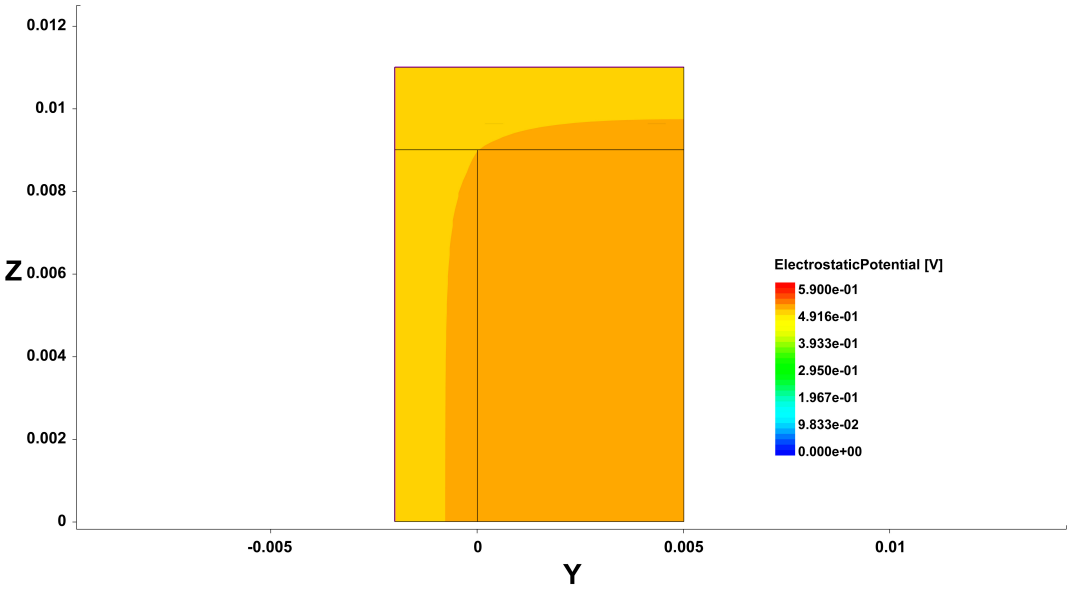


Figure 7.3: TCAD simulation results for the potential distribution of a JL TG-NW MOSFET, with $V_{gs} > V_T$. Parameters as in Fig. 7.2.

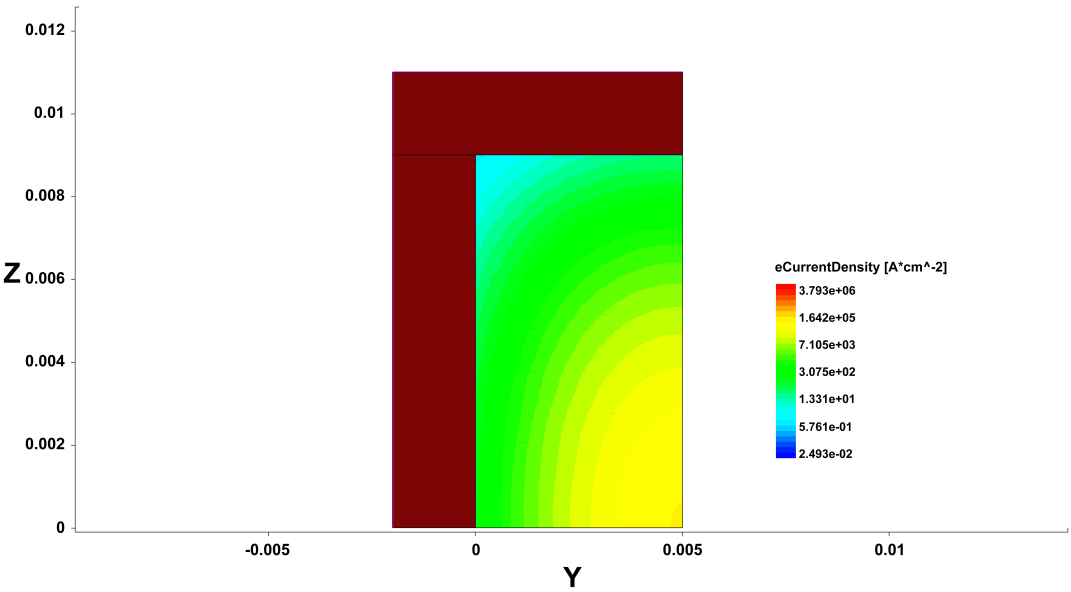


Figure 7.4: TCAD simulation results for the electron current density of a JL TG-NW MOSFET, with $V_{gs} \approx V_T$. Parameters as in Fig. 7.2.

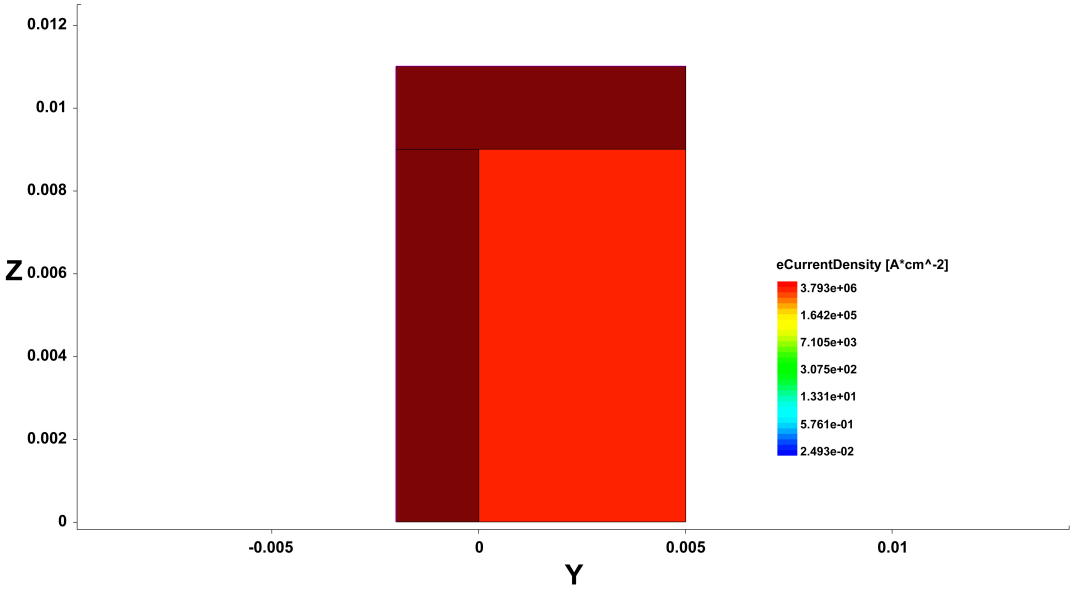


Figure 7.5: TCAD simulation results for the electron current density of a JL TG-NW MOSFET, with $V_{gs} > V_T$. Parameters as in Fig. 7.2.

7.2 3-D Potential Modeling Extension

Based on the development process for the double-gate device (chapter 4) an enhanced model valid for 3-D MOSFET structures, considering an additional top-gate, is presented (see Fig. 7.6) [154]. The new model accounts for 3-D effects in triple-gate structures using the conformal mapping technique by Schwarz-Christoffel [57], whereby a similar procedure for lightly-doped junction-based devices was presented in [27]. The starting point is 3-D Poisson's equation, which is expressed as:

$$\Delta\phi(x,y,z) = -\frac{\rho(x,y,z)}{\varepsilon_{Si}}. \tag{7.1}$$

In a very simple way Poisson's equation can be simplified in order to achieve an analytical closed-form expression for the potential. The solution of Poisson's equation is therefore split into three separate problems. These will be called the source, drain and top-gate related case. For more detailed information concerning this decomposition strategy the reader is kindly asked to refer to [27]. Applying this decomposition strategy, the result for the 3-D solution of the electrostatic potential can be written as:

$$\phi(x,y,z) = \phi_{2D}(x,z) + \varphi_{top}(y,z), \tag{7.2}$$

where ϕ_{2D} and φ_{top} represent the contributions of the decomposed potential problems related to source/drain and top-gate, respectively. In the following, the contributions of the source/drain-related cases (ϕ_{2D}) are expressed in terms of the 2-D surface and center potentials $\phi_{s/c,2D}$ at

the potential barrier inside the channel region (equation (4.55) and (4.56), respectively).

The device current below threshold voltage is dominated by a current in the device's center and at the silicon-to-oxide interface, at the bottom of the channel region (compare with section 7.1). Therefore, the 3-D surface and center potentials $\phi_{s,3D}$ and $\phi_{c,3D}$, respectively, at the bottom of the channel and the corresponding gate voltage $V_g' = V_{gs} - V_{fb}$, are then calculated by adding the contributions of the 2-D solution for source/drain and the electrostatic influence of the device's top-gate.

$$\phi_{s/c,3D}(V_g') = \phi_{s/c,2D}(V_g') + \varphi_{s/c,top}(V_g') \tag{7.3}$$

By assuming that the oxide thickness at the side and top of the device are equal, the contributions of the source/drain-related cases are readily obtained from a parabolically shaped approximation of the potential (from gate to gate) as [27]:

$$\phi_{s/c,2D}(V_g') = \phi_{c,2D}(V_g') + \frac{\phi_{bnd}}{\left(T_{ch}/2 + \tilde{T}_{ox}\right)^2} \cdot \zeta^2, \tag{7.4}$$

$$\phi_{bnd} = V_g' - \phi_{c,2D}(V_g') \tag{7.5}$$

$$\tilde{T}_{ox} = \frac{\varepsilon_{Si}}{\varepsilon_{ox}} \cdot T_{ox}. \tag{7.6}$$

ζ in Eq. (7.4) is set to $\zeta = T_{ch}/2$ and $\zeta = 0$ when calculating the surface and center potential, respectively. The contribution of the top-gate influence (φ_{top}) at surface and center is then calculated to:

$$\varphi_{s/c,top}(V_g') = \phi_{bnd} \cdot \left[\frac{1}{2}\left(\sqrt{1-(u-iv)^2} + \sqrt{1-(u+iv)^2}\right) - v\right]. \tag{7.7}$$

The parameters u and v originate from the conformal mapping technique as:

$$w = u + iv = \cosh\left(\pi \frac{\left(\tilde{T}_{ox} + H_{ch}\right) + i \cdot (z)}{2\,\tilde{T}_{ox} + T_{ch}}\right), \tag{7.8}$$

with $z = \tilde{T}_{ox}$ for the surface and $z = \tilde{T}_{ox} + T_{ch}/2$ for the calculation of the center potential. The complete 3-D potential at surface and center ($\phi_{s/c,3D}$) is finally obtained by substituting the solutions of Eq. (7.4) and (7.7) in (7.3).

The quantum corrected threshold voltage model from Eq. (6.6), which now incorporates the 3-D potential solution, modifies to:

$$V_{T,Q} = V_g^* + dV_g \left(\frac{\left(\phi_T + \left(\Delta E_{Q(JL)}/q\right)\right) - \phi_{c,3D}(V_g^*)}{\phi_{c,3D}(V_g^* + dV_g) - \phi_{c,3D}(V_g^*)}\right), \tag{7.9}$$

whereby the parameter $\Delta E_{Q(JL)}$ is described by Eq. (6.2) and Eq. (6.3), depending on T_{ch}.

7.3 Mobile Charge Density and Drain Current Model

After calculating the 3-D potential, the mobile charge density in the 3-D structure needs to be calculated accordingly. If the channel height of the JL TG-NW MOSFET is very large compared to its channel thickness, the 3-D quantum corrected mobile charge $Q_{m,3D,Q}$ is separated into a top and bottom charge.

$$Q_{m,3D,Q} = Q^{top}_{m,3D,Q} + Q^{bot}_{m,3D,Q} \tag{7.10}$$

Assuming a parabolic potential profile at the potential barrier, at threshold voltage $V_{T,Q}$ from Eq. (7.9), the mobile charge in the top square of the channel with a height equivalent to its thickness can be approximated by [155]:

$$Q^{top}_{m,3D,Q}(V_{T,Q}) = q\, n_i \cdot \frac{\sqrt{\pi}\ H_{ch} \cdot \mathrm{erf}\left\{\frac{1}{2}\sqrt{\ln(f(y=0)) - \ln(f(y=T_{ch}))}\right\}}{\sqrt{\ln(f(y=0)) - \ln(f(y=T_{ch}))}}$$
$$\times\, f(y=0) \cdot \exp\left(\frac{\left(\phi_{s,3D}\left(V_{T,Q}\right) - \left(\Delta E_{Q(JL)}/q\right)\right)}{V_{th}}\right). \tag{7.11}$$

The mobile charge in the remaining part of the device's channel cross-section (at bottom) is approximated by a 1-D parabolic function as:

$$Q^{bot}_{m,3D}(V_{T,Q}) = (H_{ch} - T_{ch})\ q\, n_i \cdot f(y=0) \cdot \exp\left(\frac{\left(\phi_{s,3D}\left(V_{T,Q}\right) - \left(\Delta E_{Q(JL)}/q\right)\right)}{V_{th}}\right), \tag{7.12}$$

with

$$f(y) = \exp(g(y)) \cdot \left(\frac{\sqrt{\pi}\, T_{ch}/2}{2\sqrt{g(y)}}\right) \cdot \mathrm{erf}\left\{\sqrt{g(y)}\right\} \tag{7.13}$$

$$g(y) = \mathrm{abs}\left(\frac{\phi_{c,3D}(V_{T,Q}) - \phi_{s,3D}(V_{T,Q})}{V_{th}}\right)\left(1 - \left(\frac{y}{H_{ch}}\right)^2\right). \tag{7.14}$$

If $H_{ch} \approx T_{ch}$ the total mobile channel charge is expressed by Eq. (7.11), whereby the influence of Eq. (7.12) vanishes. The mobile charges Q_s and Q_d at the source and drain end of the device's channel region, respectively, are then calculated in the same way as discussed in section 4.5, by replacing Eq. (4.67) with Eq. (7.10). The final current equation, which is continuous and valid from depletion to accumulation region, then reads as:

$$I_{ds} = \frac{\mu\,(H_{ch} + T_{ch}/2)}{L_g}\ \left[V_{th}\,\tilde{\alpha}\ (Q_s - Q_d) + \frac{\left({Q_s}^2 - {Q_d}^2\right)}{4\,\tilde{C}}\right], \tag{7.15}$$

where $\tilde{\alpha}$ and $\tilde{C}$ are introduced to account for subthreshold slope degradation and the effect of

volume conduction in the depletion region, respectively (compare with section 4.6). The drain current equation of nanoscale TG-NW MOSFETs is defined by the unified charge-based equation (4.108) of short-channel DG MOSFETs valid in all regions of operation [156], considering that each half of the top-gate thickness T_{ch} contributes to the side gate of height H_{ch}. Therefore, the effective channel width of the TG-NW MOSFET is defined as $W_{ch} = H_{ch} + T_{ch}/2$ [155, 157].

In order to account for mobility degradation effects the carrier mobility μ is expressed in terms of the normal and lateral gate electric field and additionally, includes velocity saturation (v_{sat}) effects, whereby v_{sat} is treated as an adjustable parameter [22, 27]. The mobility below threshold is given as:

$$\mu_{\perp} = \frac{\mu_0}{1 + \theta \left(V_{g,eff} - V_{T,Q}\right)}, \tag{7.16}$$

and the effective mobility is calculated to:

$$\mu = \frac{\mu_{\perp}}{\left(1 + \frac{\mu_{\perp} V_{dss}}{v_{\mathrm{sat}} L_g}\right)}, \tag{7.17}$$

whereby the saturation voltage V_{dss} is given by Eq. (4.92), θ represents the mobility degradation factor and the effective gate bias $V_{g,eff}$ is expressed as:

$$V_{g,eff} = V_{T,Q} + \left(\frac{\ln\left(1 + \exp\left(C_1 \left(V_g' - V_{T,Q}\right)\right)\right)}{\ln\left(1 + \exp(C_1)\right)} \right) \tag{7.18}$$

The values of the low-field mobility μ_0 were extracted from [109] and [112], where similar structures with identical N_d were presented and analyzed. The corresponding, approximated values are summarized in Table 7.1.

L_g [nm]	$\mu_0 \mid_{N_d=1\cdot10^{19}\,\mathrm{cm}^{-3}}$	$\mu_0 \mid_{N_d=2\cdot10^{19}\,\mathrm{cm}^{-3}}$
92	105	-
90	-	95
72	80	-
70	-	90
42	50	-
40	-	55
22	40	-
16	30	-

Table 7.1: Low-field mobility values for various L_g and N_d.

7.4 3-D Model Validation and Discussion

The model is compared versus measurement data, which were provided through the "SQWIRE" project. The measuring was done by S. Barraud *et. al.*, who is with the LETI in Grenoble, France. For details about the device fabrication, the reader is kindly asked to refer to [158]. The considered JL TG-NW MOSFET is schematically drawn in Fig. 7.6. The devices under test have various L_g and N_d. The fabricated gate stack gives an $EOT \approx 1.2\,\text{nm}$ and the source/drain lengths are $L_{sd} = 150\,\text{nm}$. The measuring was done at $T = 300\,\text{K}$. In the model, the del Alamo model for the consideration of band gap narrowing effects is included [34]. So far, the model does not include the effect of gate-induced drain leakage (GIDL) current.

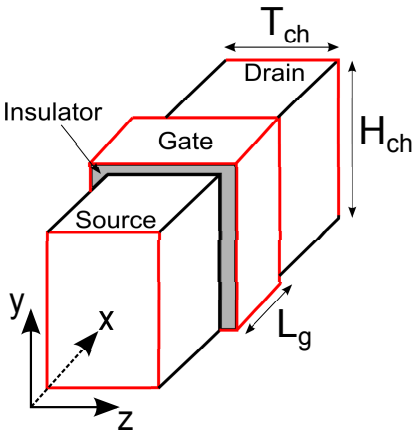
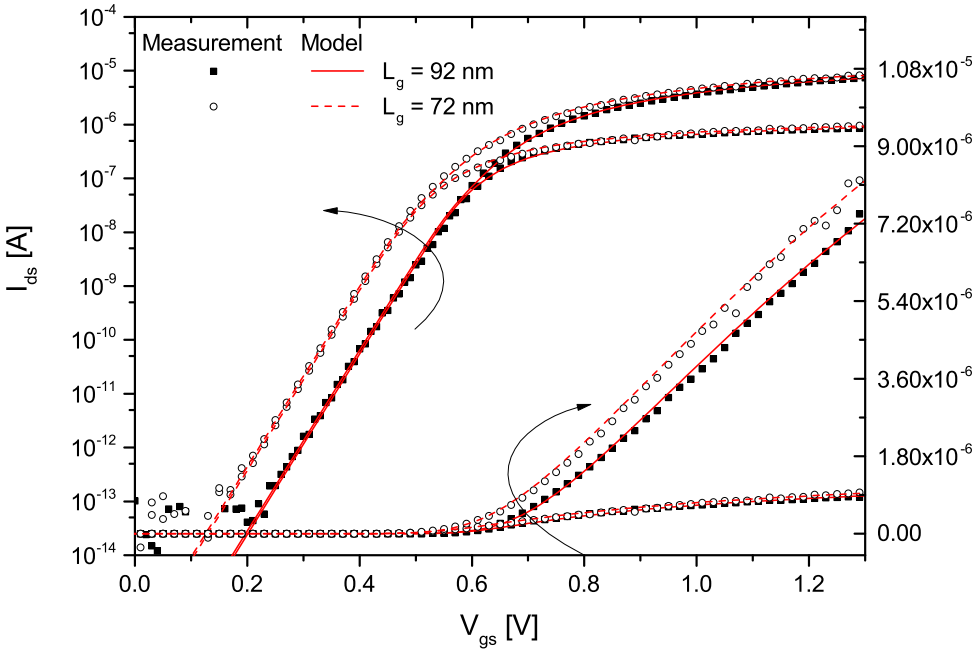


Figure 7.6: Illustration of the JL TG-NW MOSFET including its coordinate system. Red lines represents the source, drain and gate electrode, respectively.

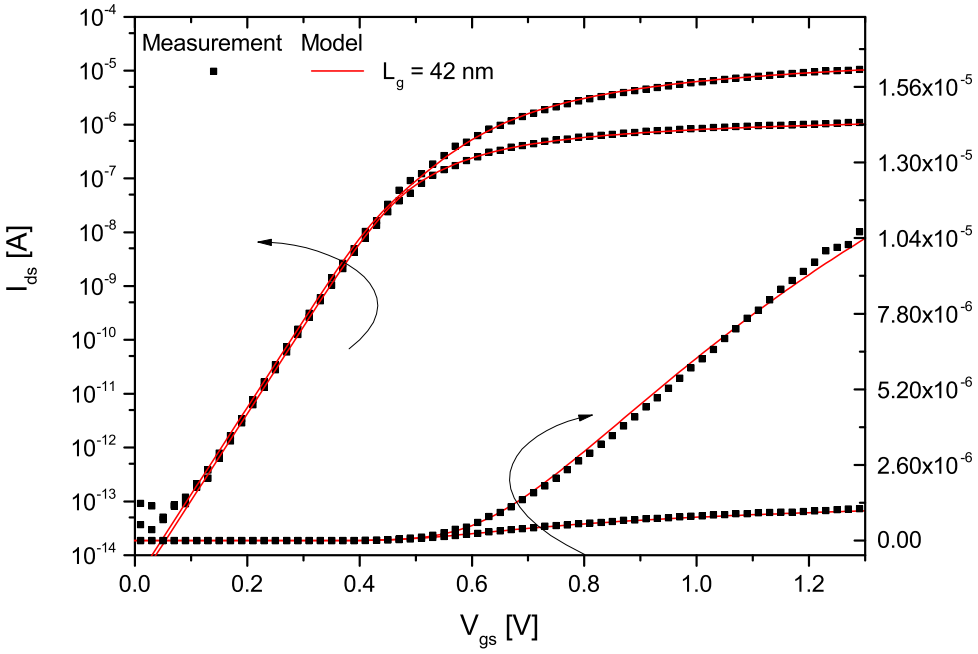
Figure 7.7(a) depicts the transfer characteristics of the JL TG-NW MOSFET. On first sight, one can see that the model matches well the measurement data from the depletion to the accumulation region. Important electrical parameters such as the V_T, DIBL and S are well predicted. Here, the DIBL is defined as:

$$\text{DIBL} = V_T|_{V_{ds}=0.05\,\text{V}} - V_T|_{V_{ds}=0.9\,\text{V}}\,. \tag{7.19}$$

By decreasing L_g down to 42 nm, V_T slightly rolls-off, as expected (Fig. 7.7(b)). However, the DIBL is still very low (around 10 mV) and S is insignificantly affected. A similar device behavior was shown in [158]. Since the model matches well with the measurement data, one can estimate that the electrical model parameters are identical to the measured ones. Unlike in DG devices [139], the V_T roll-off, through downscaling L_g, is much lower in TG transistors, due to the increased electrostatic control of the gate electrodes on the device's channel region (reduced SCEs).



(a)



(b)

Figure 7.7: (a) Transfer characteristics of the JL TG-NW MOSFET with: $N_d = 1 \cdot 10^{19}\,\mathrm{cm}^{-3}$, $V_{ds} = 0.05\,/\,0.9\,[\mathrm{V}]$, $L_g = 92\,/\,72\,[\mathrm{nm}]$, $L_{sd} = 150\,\mathrm{nm}$, $T_{ch} = 10\,\mathrm{nm}$, $EOT = 1.2\,\mathrm{nm}$, $H_{ch} = 9\,\mathrm{nm}$. (b) Transfer characteristics of the same device with: $L_g = 42\,\mathrm{nm}$. Symbols measurement; lines model.

The transfer characteristics of the JL TG-NW MOSFET at an increased $N_d = 2 \cdot 10^{19}\,\mathrm{cm}^{-3}$, for various L_g, are detailed in Fig. 7.8. In logarithmic-scale it can be observed that S is correctly predicted by the model for both channel lengths and drain voltages. The measurement data shows some dispersions in that region, but nonetheless they can be used for the verification. In linear-scale the maximum output current of the model matches well that of the reference data, which proves the good quality of the model.

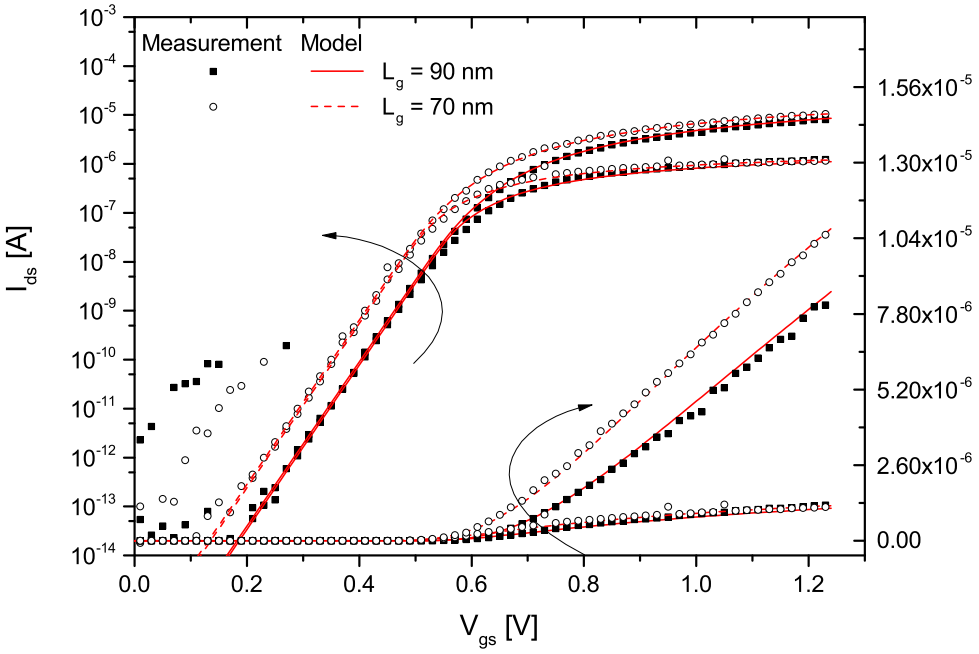


Figure 7.8: Transfer characteristics of the JL TG-NW MOSFET with: $N_d = 2 \cdot 10^{19}\,\mathrm{cm}^{-3}$, $V_{ds} = 0.05\,/\,0.9\,[\mathrm{V}]$, $L_g = 90\,/\,70\,[\mathrm{nm}]$, $L_{sd} = 150\,\mathrm{nm}$, $T_{ch} = 10\,\mathrm{nm}$, $EOT = 1.2\,\mathrm{nm}$, $H_{ch} = 9\,\mathrm{nm}$. Symbols measurement; lines model.

A close look at Fig. 7.9 indicates that SCEs are increasing with the reduction of L_g. V_T shifts and the DIBL increases. Even though the subthreshold slope worsens, this effect is still negligible.

The model is compared versus 3-D TCAD simulations using the same device parameters, but shorter channel lengths (Fig. 7.10). The subthreshold performance worsens, whereby the ON-current increases. The model shows some discrepancies at $L_g = 16\,\mathrm{nm}$, because in this case L_g is close to T_{ch} and H_{ch}, which is not covered by the conformal mapping technique due to the introduced decomposition into source and drain related cases. The calculated electrical parameters are summarized in Table 7.2. By comparing them it becomes clear that an increasing N_d does not affect the subthreshold performance and the DIBL of JL TG-NW MOSFETs significantly.

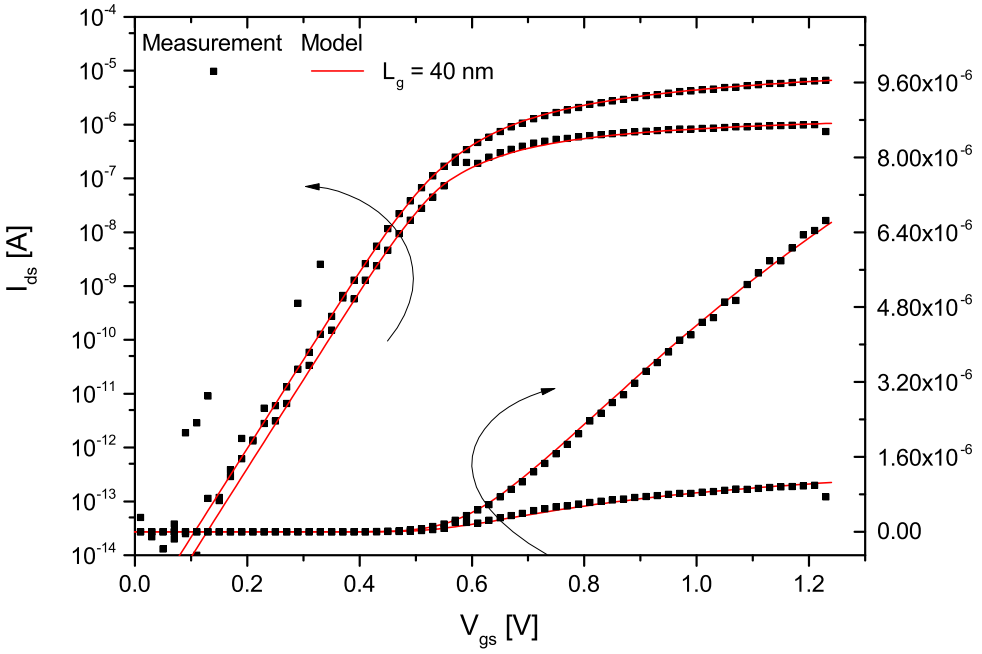


Figure 7.9: Transfer characteristics of the JL TG-NW MOSFET. Parameters as in Fig. 7.8 with: $L_g = 40\,\text{nm}$. Symbols measurement; lines model.

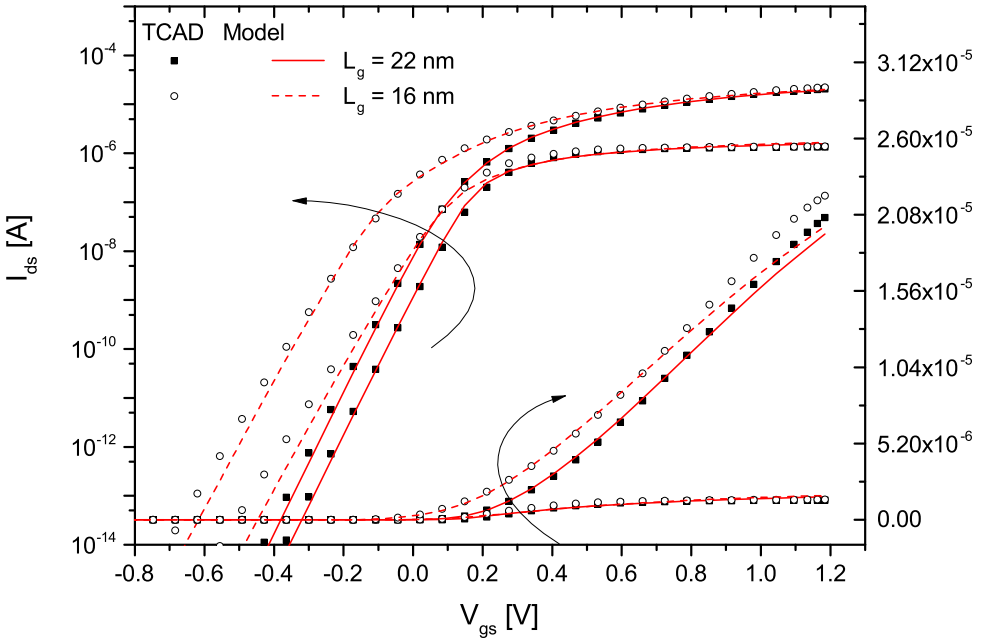


Figure 7.10: Transfer characteristics of the JL TG-NW MOSFET. Parameters as in Fig. 7.7(a) with: $L_g = 22\,/\,16\,[\text{nm}]$. Symbols TCAD; lines model.

L_g [nm]	V_T [V]	DIBL [mV]	S [mV/dec]
92	0.443 / 0.442	1	59.5 / 59.5
90	0.439 / 0.438	1	59.5 / 59.5
72	0.402 / 0.401	1	59.5 / 59.5
70	0.400 / 0.399	1	59.5 / 59.5
42	0.381 / 0.373	8	61.8 / 61.8
40	0.392 / 0.381	11	60.6 / 60.6
22	0.155 / 0.117	38	68,7 / 68.4
16	0.005 / -0.105	110	76.3 / 75.7

Table 7.2: Calculated V_T, DIBL and S. With V_T and S at $V_{ds} = 0.05\,/\,0.9\,[\mathrm{V}]$.

By downscaling T_{ch} to 3 nm, at $L_g = 16\,\mathrm{nm}$, one can see that the predicted transfer characteristics are still in good agreement with the data obtained from 3-D TCAD quantum simulations (Fig. 7.11). The calculated electrical parameters are $V_T = 0.33\,\mathrm{V}\,/\,0.32\,\mathrm{V}$ and $S = 62.5\,\mathrm{mV/dec}$ and $62.1\,\mathrm{mV/dec}$ at $V_{ds} = 0.05\,/\,0.9\,\mathrm{V}$. The DIBL is around 10 mV. By investigating the gate transconductance g_m (Fig. 7.12), one can observe some deviations around V_T between the model and the reference data. Nevertheless, the model accurately predicts the subthreshold behavior and no discontinuities in I_{ds} can be found.

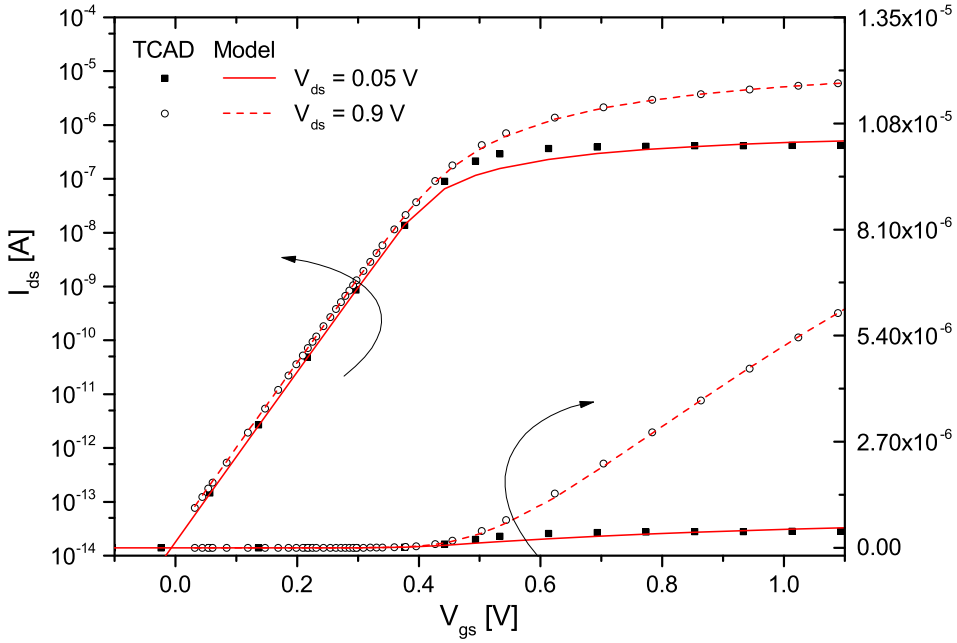


Figure 7.11: Transfer characteristics of the JL TG-NW MOSFET with: $N_d = 1 \cdot 10^{19}\,\mathrm{cm}^{-3}$, $V_{ds} = 0.05\,/\,0.9\,[\mathrm{V}]$, $L_g = 16\,\mathrm{nm}$, $L_{sd} = 150\,\mathrm{nm}$, $T_{ch} = 3\,\mathrm{nm}$, $EOT = 1.2\,\mathrm{nm}$, $H_{ch} = 9\,\mathrm{nm}$. Symbols TCAD; lines model.

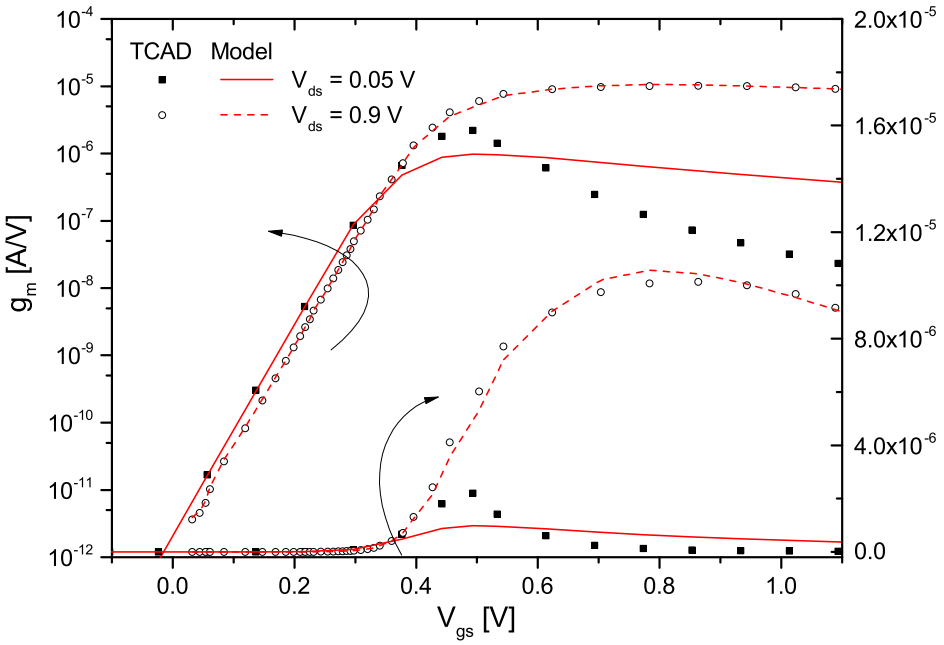


Figure 7.12: Gate transconductance g_m of the device shown in Fig. 7.11. Symbols TCAD; lines model.

Since symmetry around $V_{ds} = 0\,\mathrm{V}$ is a key property of compact models, it is addressed in the following. The model is verified with respect to a source/drain reversal test [78], displaying the current I_{ds} and its 1st derivative (Fig. 7.13). The results are plotted versus the voltage V_x, which is asymmetrically biasing the source and drain contacts with $V_{source} = -V_x$ and $V_{drain} = +V_x$, respectively. Even at such extremely scaled dimensions with $L_g = 16\,\mathrm{nm}$ and $T_{ch} = 3\,\mathrm{nm}$, where short-channel as well as quantization effects play a major role, the drain current and also its derivative are symmetric in the detailed regime, which proves that the developed model passes the symmetry test.

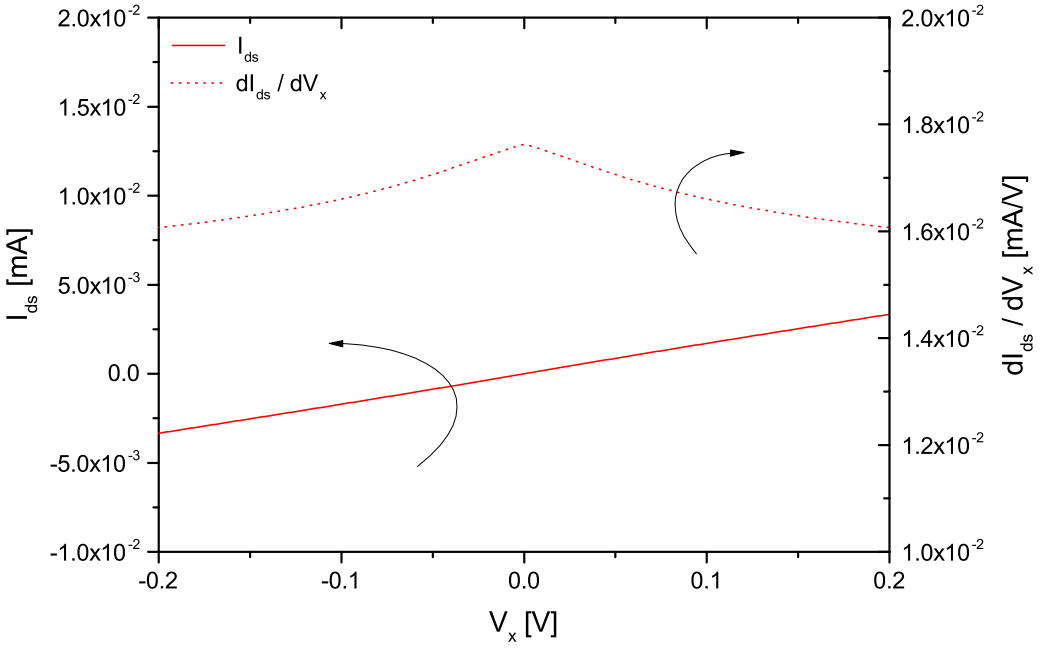


Figure 7.13: Source-drain symmetry test. Drain current I_{ds} and its 1st derivative are plotted versus V_x for validation. Parameters: $V_x = -0.2\,\mathrm{V}$ to $0.2\,\mathrm{V}$, $V_{gs} = 1\,\mathrm{V}$, $N_d = 10^{19}\,\mathrm{cm}^{-3}$, $L_g = 16\,\mathrm{nm}$, $L_{sd} = 150\,\mathrm{nm}$, $T_{ch} = 3\,\mathrm{nm}$, $EOT = 1.2\,\mathrm{nm}$, $H_{ch} = 9\,\mathrm{nm}$.

CHAPTER 8

Conclusion

An analytical, physics-based and predictive compact model for nanoscale multiple-gate junctionless and inversion mode MOSFETs was developed in this doctoral study. A new drain current expressions for junctionless MOSFETs was presented, whereby its accuracy was verified from the depletion to the accumulation region. The developed model is valid in all regions of device operation and was proved to predict the electrical behavior of most practical present and future device structures well. The developed model equations are in strong relation to the device physics, whereby the number of adjustable parameters was kept at a minimum level. Throughout the thesis the model was compared versus numerical TCAD simulation data [34] and additionally, in the case of the junctionless triple-gate device, versus measurement data. Several important physical effects were included in the modeling approach in order to keep pace with the strong requirements of the ITRS [21].

A charge-based AC model was derived based on the Ward-Dutton partition method and verified versus numerical TCAD simulation data. It was found that for relatively long channels this method returns well matching results. But for short-channel devices the predictive ability of this method diminishes. Additionally, in junctionless devices, it was found that some deviations occur in their partly depleted operating regime, which might be owed to the non-quadratic Q-V relationship which was assumed in the developed model.

A performance study for both device types in 2-D was carried out, whereby important device characteristics such as the drain-induced barrier lowering, subthreshold slope and the I_{on}/I_{off} ratios were analyzed and discussed. In both device types it was found that: quantization effects have a strong influence on the threshold voltage and that the subthreshold characteristics were largely improved through scaling down the channel thickness - even though QEs affected their performances. The junctionless device provided higher maximum current ratios compared to its inversion mode counterpart. In addition, the I_{on}/I_{off} ratios were shown to improve largely through scaling down T_{ch}.

A complete 3-D compact model for nanoscale junctionless triple-gate nanowire MOSFETs was presented. The predictive ability of the analytical and physics-based model was proved for

several cases, such as different doping profiles and levels, device dimensions and electrical setups. No structural fitting was used in the model, i.e. the structural model parameters equaled the values given by the fabricated devices. The low-field mobility was not fitted, but extracted from state-of-the-art publications and adapted to the model. Only the mobility degradation factor, the saturation velocity of the charge carriers and the flat-band voltage were adjusted to match the reference data. The threshold voltage, the DIBL and the subthreshold slope were shown to be correctly predicted by the model. Additionally, continuity of the drain current was demonstrated by showing the derivatives up to third-order. The 3-D model passed the symmetry test, which is a key property for compact models. Carrier quantization effects were taken into account in a very simple way by introducing a quantum correction term in the threshold voltage and the mobile charge density expression.

Limitations of the Model

In order to find a closed-form solution for the electrostatics and the drain current, some simplifications were introduced to the analytical model. Therefore, it is limited to some range of validity. This is for example if the oxide thickness becomes very thick, wherefore the approximation of a linear potential drop in that area fails. Likewise, if the channel length becomes comparable to its height the decomposition of the four-corner structure into source and drain related cases fails as well. However, this case is not desired in today's, or future devices as a proper device operation would be jeopardized. Another point is that the current in junctionless devices was described by a quadratic Q-V dependency in the partly depleted region in [88], which is not taken into account in the developed model. This quadratic dependency was shown to significantly impact the double-gate device's electrical behavior if the channel thickness and at the same time its doping concentration is large ($\geq T_{ch} = 20\,\mathrm{nm}$ and $N_d = 2 \cdot 10^{19}\,\mathrm{cm}^{-3}$). Also, concerning the junctionless' dynamic operation mode, the quadratic Q-V relation should be taken into account in order to predict its capacitive behavior more precisely [98].

Future Prospects

So far, the developed model does not take into account effects like: temperature variations, ballistic transport mechanisms, gate-induced drain leakage currents or the effect of the parasitic source/drain access resistances. Additionally, a Verilog-A implementation for circuit simulators is still to be done. These subjects are part of the future work.

Since an IC is generally specified to be functional in a certain temperature range (i.e. -50°C to +125°C), the modeling of **temperature effects** is of great importance. Temperature affects a lot of different device parameters such as the band gap energy E_g, which decreases as the temperature increases. The threshold voltage is temperature dependent since it is a function of the flat-band voltage, the Fermi potential and others, which again depend on T. The mobility in semiconductor devices is a strong function of T and therefore, the drain current I_{ds}, which varies according to the ambient temperature and self-heating effects inside a MOSFET [22].

In long-channel MOSFETs the charge carriers experience a lot of scattering events, which decrease the drain current when they are traveling through the channel region. In this case the drain current can be described by a drift-diffusion transport mechanism. In nanoscale MOSFETs with channel lengths less than 50 nm, the relaxation times of the carriers indicate that the drain current will have an intermediate character between drift-diffusion and **ballistic/quasi-ballistic transport** [23]. Or in other words, a significant fraction of the charge carriers traverse the channel region without undergoing scattering events. This ballistic component is expected to increase with further down scaling and to dominate over the drift-diffusion component in devices with channel lengths shorter than 30 nm [159, 160].

The minimization of the MOSFET's off-state leakage current is an important issue, in particular for low-power circuit applications. A large component of the off-state leakage current originates from the **gate-induced drain leakage (GIDL)** current. It is caused by a band-to-band tunneling effect in the drain region underneath the gate. If a large gate to drain bias is applied, the band bending in that area, near the silicon-to-oxide interface, enables valence band electrons to tunnel into the conduction band. Because the voltage required to cause this band-to-band tunneling decreases with the gate oxide thickness, this leakage current imposes a constraint for gate oxide thickness scaling [161].

As the ITRS predicts shrinking devices sizes, down to $L_g = 16\,\text{nm}$, the **parasitic source and drain access resistances** become an important fraction of the device's total resistance. Therefore, these parasitic resistances must be taken into account as they are one of the major factors limiting the overall performance of scaled MOSFETs [22].

Finally, the developed model is to be implemented into a circuit simulator. This is preferably done using the hardware description language (HDL) **Verilog-A**, which has become a standard in the field of circuit simulator models. The most challenging part will be the translation and implementation of the developed potential solution, which contains complex functions. So far, such complex functions are not recognized by Verilog-A, wherefore a work around is mandatory. Additionally, the efficient and accurate reproduction of Lambert's W-function is of importance, since it is decisive for the calculation of the charge densities at the source and the drain end of the channel region and therefore, is strongly linked to the drain current of the device.

For upcoming nanoscale MOSFET generations with extremely high package densities and at the same time, the demand for high performances, it will be of great importance to gain knowledge about the device's electrical behavior. In particular, the correct treatment of short-channel as well as new physical effects, such as charge carrier quantization, is crucial. For that reason, this topic is target of up-to-date worldwide research, which must be pushed with special emphasis. The developed 2-D and 3-D predictive compact models for junction-based and the newly introduced junctionless MOSFET is in fact an important contribution to the continuous development process in that field.

APPENDIX A

Equation Package

The solution for the total channel charge Q_C (Eq. (5.12)) is:

$$Q_C = \frac{{W_{ch}}^2\,\mu}{I_{ds}}\left(\frac{{Q_d}^3}{6\,\tilde{C}} - \frac{{Q_s}^3}{6\,\tilde{C}} + \frac{{Q_d}^2\,V_{th}\,\tilde{\alpha}}{2} - \frac{{Q_s}^2\,V_{th}\,\tilde{\alpha}}{2}\right). \tag{A.1}$$

The solution for the total charge at drain Q_D (Eq. (5.16)) is:

$$\begin{aligned} Q_D = -\frac{{W_{ch}}^3\,\mu^2}{{I_{ds}}^2\,L_g}\Bigg(&\frac{{Q_d}^3\,{Q_s}^2}{24\,\tilde{C}^2} - \frac{{Q_s}^5}{60\,\tilde{C}^2} - \frac{{Q_d}^5}{40\,\tilde{C}^2} - \frac{{Q_d}^3\,{V_{th}}^2\,\tilde{\alpha}^2}{3} - \frac{{Q_s}^3\,{V_{th}}^2\,\tilde{\alpha}^2}{6} \\ &- \frac{3\,{Q_d}^4\,V_{th}\,\tilde{\alpha}}{16\,\tilde{C}} - \frac{5\,{Q_s}^4\,V_{th}\,\tilde{\alpha}}{48\,\tilde{C}} + \frac{{Q_d}^2\,Q_s\,{V_{th}}^2\,\tilde{\alpha}^2}{2} + \frac{{Q_d}^2\,{Q_s}^2\,V_{th}\,\tilde{\alpha}}{8\,\tilde{C}} + \frac{{Q_d}^3\,Q_s\,V_{th}\,\tilde{\alpha}}{6\,\tilde{C}}\Bigg), \end{aligned} \tag{A.2}$$

and the integral solution for the total charge at drain Q_S (Eq. (5.17)) is:

$$\begin{aligned} Q_S = \frac{{W_{ch}}^2\,\mu}{I_{ds}}\Bigg(&\frac{{Q_d}^3}{6\,\tilde{C}} - \frac{{Q_s}^3}{6\,\tilde{C}} + \frac{{Q_d}^2\,V_{th}\,\tilde{\alpha}}{2} - \frac{{Q_s}^2\,V_{th}\,\tilde{\alpha}}{2} + \frac{{Q_d}^5\,W_{ch}\,\mu}{40\,\tilde{C}^2\,I_d\,L_g} + \frac{{Q_s}^5\,W_{ch}\,\mu}{60\,\tilde{C}^2\,I_d\,L_g} \\ &- \frac{{Q_d}^3\,{Q_s}^2\,W_{ch}\,\mu}{24\,\tilde{C}^2\,I_d\,L_g} + \frac{{Q_d}^3\,{V_{th}}^2\,W_{ch}\,\tilde{\alpha}^2\,\mu}{3\,I_d\,L_g} + \frac{{Q_s}^3\,{V_{th}}^2\,W_{ch}\,\tilde{\alpha}^2\,\mu}{6\,I_d\,L_g} \\ &+ \frac{3\,{Q_d}^4\,V_{th}\,W_{ch}\,\tilde{\alpha}\,\mu}{16\,\tilde{C}\,I_d\,L_g} + \frac{5\,{Q_s}^4\,V_{th}\,W_{ch}\,\tilde{\alpha}\,\mu}{48\,\tilde{C}\,I_d\,L_g} - \frac{{Q_d}^2\,Q_s\,{V_{th}}^2\,W_{ch}\,\tilde{\alpha}^2\,\mu}{2\,I_d\,L_g} \\ &- \frac{{Q_d}^2\,{Q_s}^2\,V_{th}\,W_{ch}\,\tilde{\alpha}\,\mu}{8\,\tilde{C}\,I_d\,L_g} - \frac{{Q_d}^3\,Q_s\,V_{th}\,W_{ch}\,\tilde{\alpha}\,\mu}{6\,\tilde{C}\,I_{ds}\,L_g}\Bigg), \end{aligned} \tag{A.3}$$

whereby the integration of Q_D and Q_S was carried out using the software Matlab [162].

References

[1] Intel, "Online in internet: www.intel.com," 2014.

[2] Univeristy California, *SPICE3 Version 3e User's Manual*, 1991.

[3] Anacad GmbH, *ELOD User's Manual*, 2005.

[4] J. E. Lilienfeld, "Method and Apparatus for Controlling Electric Currents," January 1930.

[5] J. H. Shaff and R. Ohl, "Development of silicon crystal rectifiers for microwave radar receivers," *Bell System Technical Journal*, vol. 26, 1947.

[6] R. Ohl, "Light-Sensitive Electric Device," June 1946.

[7] W. Shockley, "Circuit Element Utilizing Semiconductive Material," September 1948.

[8] W. Shockley, "The Theory of P-N Junctions in Semiconductors and P-N Junction Transistors," *Bell System Technical Journal*, vol. 28, 1949.

[9] W. Shockley, M. Sparks, and G. K. Teal, "p-n Junction Transistors," *Physical Review*, vol. 83, no. 1, pp. 151–162, 1951.

[10] J. S. Kilby, "Invention of the integrated circuit," *IEEE Transactions on Electron Devices*, vol. 23, no. 7, pp. 648–654, 1976.

[11] M. M. J. Atalla and D. Kahng, "Electric field controlled semiconductor device," May 1963.

[12] T. J. Tsvedos, "Introduction to Microsystems and the RCA Micromodule," in *The RCA Micromodule Program: Components and Application AIEE Electronics Division*, May 1961.

[13] F. Wanlass and C. Sah, "Nanowatt logic using field-effect metal-oxide semiconductor triodes," in *Solid-State Circuits Conference. Digest of Technical Papers. 1963 IEEE International*, vol. VI, pp. 32–33, 1963.

[14] F. M. Wanlass, "Low Stand-By Power Complementary Field Effect Circuitry," December 1967.

[15] G. Moore, "The Future of Integrated Electronics," tech. rep., Fairchild Semiconductor, 1964.

[16] G. E. Moore, "Cramming more components onto integrated circuits," *Electronics*, vol. 38, April 1965.

[17] G. Moore, "Progress in digital integrated electronics," in *Electron Devices Meeting, 1975 International*, vol. 21, pp. 11–13, 1975.

[18] F. Faggin, J. Hoff, M. E., S. Mazor, and M. Shima, "The history of the 4004," *IEEE Micro*, vol. 16, no. 6, pp. 10–20, 1996.

[19] F. Faggin, M. Shima, M. Hoff, H. Feeney, and S. Mazor, "THE MCS-4 - An LSI micro computer system [reprint]," *Solid-State Circuits Magazine, IEEE*, vol. 1, no. 1, pp. 55–60, 2009.

[20] J. Hoff, M.E., S. Mazor, and F. Faggin, "Memory system for a multi-chip digital computer [United States Patent 3,821,715]," *Solid-State Circuits Magazine, IEEE*, vol. 1, no. 1, pp. 46–54, 2009.

[21] "International Technology Roadmap for Semiconductors (ITRS)," 2012 Update.

[22] N. Arora, *MOSFET Models for VLSI Circuit Simulation*. Springer-Verlag, Wien, 1993.

[23] B. Iniguez, T. Fjeldly, A. Lazaro, F. Danneville, and M. Deen, "Compact-Modeling Solutions For Nanoscale Double-Gate and Gate-All-Around MOSFETs," *Electron Devices, IEEE Transactions on*, vol. 53, no. 9, pp. 2128–2142, 2006.

[24] J.-P. Colinge, M. H. Gao, A. Romano-Rodriguez, H. Maes, and C. Claeys, "Silicon-on-insulator 'gate-all-around device'," in *Electron Devices Meeting, 1990. IEDM '90. Technical Digest., International*, pp. 595–598, 1990.

[25] J.-P. Colinge, "Multiple-gate soi mosfets," *Solid-State Electronics*, vol. 48, pp. 897–905, June 2004.

[26] J.-P. Colinge, *FinFETs and Other Multi-Gate Transistors*. Springer, 2007.

[27] A. Kloes, M. Schwarz, and T. Holtij, "MOS3: A New Physics-Based Explicit Compact Model for Lightly Doped Short-Channel Triple-Gate SOI MOSFETs," *Electron Devices, IEEE Transactions on*, vol. 59, no. 2, pp. 349–358, 2012.

[28] A. Kloes, M. Schwarz, T. Holtij, and A. Navas, "Quantum Confinement and Volume Inversion in MOS3 Model for Short-Channel Tri-Gate MOSFETs," *Electron Devices, IEEE Transactions on*, vol. 60, no. 8, pp. 2691–2694, 2013.

[29] A. Yesayan, F. Pregaldiny, N. Chevillon, C. Lallement, and J.-M. Sallese, "Physics-based compact model for ultra-scaled FinFETs," *Solid-State Electronics*, vol. 62, no. 1, pp. 165 – 173, 2011.

[30] J. Larson and J. P. Snyder, "Overview and status of metal S/D Schottky-barrier MOSFET technology," *Electron Devices, IEEE Transactions on*, vol. 53, no. 5, pp. 1048–1058, 2006.

[31] Y. Omura, S. Horiguchi, M. Tabe, and K. Kishi, "Quantum-mechanical effects on the threshold voltage of ultrathin-SOI nMOSFETs," *IEEE Electron Device Letters*, vol. 14, no. 12, pp. 569–571, 1993.

[32] J.-P. Colinge, C.-W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, P. Razavi, B. O'Neill, A. Blake, M. White, A.-M. Kelleher, B. McCarthy, and R. Murphy, "Nanowire transistors without junctions," *Nat Nano*, vol. 5, pp. 225–229, Mar. 2010.

[33] C.-W. Lee, A. Afzalian, N. D. Akhavan, R. Yan, I. Ferain, and J.-P. Colinge, "Junctionless multigate field-effect transistor," *Applied Physics Letters*, vol. 94, no. 5, pp. 97–103, 2009.

[34] Synopsys, Inc., *TCAD Sentaurus*, C-2012.06 ed.

[35] SILVACO, Inc., *ALTAS User's Manual Device Simulation Software*, September 2010.

[36] K.-T. Grasser, "Minimos-NT Device and Circuit Simulator," September 2002.

[37] J. Watts, C. McAndrew, C. Enz, C. Galup-Montoro, G. Gildenblat, C. Hu, R. van Langevelde, M. Miura-Mattausch, R. Rios, and C.-T. Sah, "Advanced Compact Models for MOSFETs," *NSTI-Nanotech*, 2005.

[38] Y. Cheng, M.-C. Jeng, Z. Liu, J. Huang, M. Chan, K. Chen, P. Ko, and C. Hu, "A physical and scalable I-V model in BSIM3v3 for analog/digital circuit simulation," *Electron Devices, IEEE Transactions on*, vol. 44, no. 2, pp. 277–287, 1997.

[39] X. Xi, M. Dunga, J. He, W. Liu, K. M. Cao, X. Jin, J. J. Ou, M. Chan, A. M. Niknejad, and C. Hu, *BSIM4.3.0 MOSFET Model - User's Manual*. Department of Electrical Engineering and Computer Sciences, University of California, Berkeley, 2003.

[40] R. Velghe, D. Klaassen, and F. Klaassen, "MOS Model 9," tech. rep., Philips Electronics N.V., 1994.

[41] G. Gildenblat, "The SP Model," *IEEE JSSC*, vol. 39, 2004.

[42] R. van Langevelde, A. Scholten, and D. Klaassen, "MOS Model 11," tech. rep., Philips Electronics N.V., 2005.

[43] H. Mattausch, M. Miura-Mattausch, H. Ueno, S. Kumashiro, T. Yamaguchi, K. Yamashita, and N. Nakayama, "HiSIM: The first complete drift-diffusion MOSFET model for circuit simulation," in *International Conference on Solid-State and Integrated-Circuit Technology*, 2001.

[44] M. Miura-Mattausch, H. Ueno, J. Mattausch, S. Kumashiro, T. Yamaguchi, K. Yamashita, and N. Nakayama, "HiSIM: Self-Consistent Surface-Potential MOS-Model Valid Down to Sub-100 nm Technologies," in *Technical Proceedings of the International Conference on Modeling and Simulation of Microsystems*, 2002.

[45] M. Miura-Mattausch, H. Ueno, M. Tanaka, H. Mattausch, S. Kumashiro, T. Yamaguchi, K. Yamashita, and N. Nakayama, "HiSIM: a MOSFET model for circuit simulation connecting circuit performance with technology," in *IEDM Technical Digest. International Electron Devices Meeting*, 2002.

[46] H. Mattausch, M. Miyake, D. Navarro, N. Sadachika, T. Ezaki, M. Miura-Mattausch, T. Yoshida, and S. Hazama, "HiSIM2 Circuit simulation - Solving the speed versus accuracy crisis," *IEEE Circuits and Devices Magazine*, vol. 22, no. 5, pp. 29–38, 2006.

[47] A. Scholten, G. Smit, B. De Vries, L. Tiemeijer, J. Croon, D. Klaassen, R. van Langevelde, X. Li, W. Wu, and G. Gildenblat, "(Invited) The new CMC standard compact MOS model PSP: advantages for RF applications," in *IEEE Radio Frequency Integrated Circuits Symposium*, 2008.

[48] G. Gildenblat, X. Li, W. Wu, H. Wang, A. Jha, R. van Langevelde, G. Smit, A. Scholten, and D. Klaassen, "PSP: An Advanced Surface-Potential-Based MOSFET Model for Circuit Simulation," *IEEE Transactions on Electron Devices*, vol. 53, no. 9, pp. 1979–1993, 2006.

[49] E. V. C. Enz, F. Krummenacher, "An analytical MOS transistor model valid in all regions of Operation and dedicated to low-voltage and low-current applications," *Journal on Analog Integrated Circuits and Signal Processsing, Kluwer Academic Publishers*, pp. 83–114, July 1995.

[50] C. Galup-Montoro, M. C. Schneider, A. I. A. Cunha, F. R. de Sousa, H. Klimach, and O. F. Siebel, "The Advanced Compact MOSFET (ACM) Model for Circuit Analysis and Design," in *IEEE 2007 Custom Intergrated Circuits Conference (CICC)*, 2007.

[51] J. He, J. Xi, M. Chan, H. Wan, M. Dunga, B. Heydari, A. Niknejad, and C. Hu, "Charge-based core and the model architecture of BSIM5," in *Sixth International Symposium on Quality of Electronic Design*, 2005.

[52] M. Chalkiadaki, A. Mangla, C. C. Enz, Y. S. Chauhan, M. A. Karim, S. Venugopalan, A. Niknejad, and C. Hu, "Evaluation of the bsim6 compact mosfet model's scalability in

40nm cmos technology," in *ESSCIRC (ESSCIRC), 2012 Proceedings of the*, pp. 34–37, 2012.

[53] T. Grasser, *Advanced Device Modeling and Simulation*. World Scientic, 2003.

[54] D. Vasileska and S. Goodnick, *Computational Electronics*. Morgan & Claypool, 2006.

[55] Y. Tsividis, *Operational Modeling of the MOS Transistor*. McGraw-Hill, 1999.

[56] D. Ward and R. Dutton, "A charge-oriented model for MOS transistor capacitances," *Solid-State Circuits, IEEE Journal of*, vol. 13, no. 5, pp. 703–708, 1978.

[57] E. Weber, *Electromagnetic Fields: Theory and Applications*. No. 1 in Electromagnetic Fields, Polytechnic Institute of Brooklyn: Wiley, 3 ed., April 1950.

[58] J.-M. Sallese, F. Krummenacher, F. Pregaldiny, C. Lallement, A. Roy, and C. Enz, "A design oriented charge-based current model for symmetric DG MOSFET and its correlation with the EKV formalism," *Solid-State Electronics*, vol. 49, no. 3, pp. 485 – 489, 2005.

[59] R. W. Keyes, "Effect of randomness in the distribution of impurity ions on FET thresholds in integrated electronics," *IEEE Journal of Solid-State Circuits*, vol. 10, no. 4, pp. 245–247, 1975.

[60] M. Ieong, H.-S. P. Wong, E. Nowak, J. Kedzierski, and E. C. Jones, "High performance double-gate device technology challenges and opportunities," in *Quality Electronic Design, 2002. Proceedings. International Symposium on*, pp. 492–495, 2002.

[61] Y. Taur, "Analytic solutions of charge and capacitance in symmetric and asymmetric double-gate MOSFETs," *IEEE Transactions on Electron Devices*, vol. 48, no. 12, pp. 2861–2869, 2001.

[62] Y. Taur, X. Liang, W. Wang, and H. Lu, "A continuous, analytic drain-current model for DG MOSFETs," *IEEE Electron Device Letters*, vol. 25, no. 2, pp. 107–109, 2004.

[63] H. Lu and Y. Taur, "An analytic potential model for symmetric and asymmetric DG MOSFETs," *IEEE Transactions on Electron Devices*, vol. 53, no. 5, pp. 1161–1168, 2006.

[64] O. Moldovan, D. Jimenez, J. R. Guitart, F. A. Chaves, and B. Iniguez, "Explicit Analytical Charge and Capacitance Models of Undoped Double-Gate MOSFETs," *IEEE Transactions on Electron Devices*, vol. 54, no. 7, pp. 1718–1724, 2007.

[65] F. Chaves, D. Jimenez, and J. Sune, "Explicit quantum potential and charge model for double-gate MOSFETs," *Solid-State Electronics*, vol. 54, no. 5, pp. 530 – 535, 2010.

[66] G. Baccarani and S. Reggiani, "A compact double-gate MOSFET model comprising quantum-mechanical and nonstatic effects," *IEEE Transactions on Electron Devices*, vol. 46, no. 8, pp. 1656–1666, 1999.

[67] W. Wang, H. Lu, J. Song, S.-H. Lo, and Y. Taur, "Compact modeling of quantum effects in symmetric double-gate MOSFETs," *Microelectronics Journal*, vol. 41, no. 10, pp. 688 – 692, 2010.

[68] H. Lu, W.-Y. Lu, and Y. Taur, "Effect of body doping on double-gate MOSFET characteristics," *Semiconductor Science and Technology*, vol. 23, 2008.

[69] Y. Taur, C. Wann, and D. Frank, "25 nm CMOS design considerations," in *Electron Devices Meeting, 1998. IEDM '98. Technical Digest., International*, pp. 789–792, 1998.

[70] D. J. Frank, R. H. Dennard, E. Nowak, P. M. Solomon, Y. Taur, and H.-S. P. Wong, "Device scaling limits of Si MOSFETs and their application dependencies," *Proceedings of the IEEE*, vol. 89, no. 3, pp. 259–288, 2001.

[71] H. Jin, L. Feng, Z. Xing-Ye, Z. Jian, and Z. Li-Ning, "A continuous analytic channel potential solution to doped symmetric double-gate MOSFETs from the accumulation to the strong-inversion region," *Chinese Physics B*, vol. 20, no. 1, p. 016102, 2011.

[72] A. Cerdeira, O. Moldovan, B. Iniguez, and M. Estrada, "Modeling of potentials and threshold voltage for symmetric doped double-gate MOSFETs," *Solid-State Electronics*, vol. 52, no. 5, pp. 830 – 837, 2008.

[73] D. Munteanu, J.-L. Autran, X. Loussier, S. Harrison, R. Cerutti, and T. Skotnicki, "Quantum Short-channel Compact Modelling of Drain-Current in Double-Gate MOSFET," *Solid-State Electronics*, vol. 50, no. 4, pp. 680 – 686, 2006. Special Issue: Papers Selected from the 35th European Solid-State Device Research Conference - ESSDERC.

[74] O. Moldovan, A. Cerdeira, D. Jimenez, J.-P. Raskin, V. Kilchytska, D. Flandre, N. Collaert, and B. Iniguez, "Compact model for highly-doped double-gate SOI MOSFETs targeting baseband analog applications," *Solid-State Electronics*, vol. 51, no. 5, pp. 655 – 661, 2007.

[75] J. M. Sallese, N. Chevillon, F. Pregaldiny, C. Lallement, and I. B., "The Equivalent-Thickness Concept for Doped Symmetric DG MOSFETs," *Electron Devices, IEEE Transactions on*, vol. 57, no. 11, pp. 2917–2924, 2010.

[76] S. Sarangi, A. Santra, S. Bhushan, K. Gopi, S. Dubey, and P. Tiwari, "An analytical surface potential modeling of fully-depleted symmetrical double-gate (DG) strained-Si MOSFETs including the effect of interface charges," in *Engineering and Systems (SCES), 2013 Students Conference on*, pp. 1–5, 2013.

[77] T. A. Fjedly, S. Kolberg, and B. Iniguez, "Precise 2D Compact Modeling of Nanoscale DG MOSFETs Based on Conformal Mapping Techniques," *NSTI-Nanotech*, vol. 3, pp. 668 – 673, 2006.

[78] C. Mcandrew, "Validation of MOSFET model Source-Drain Symmetry," *Electron Devices, IEEE Transactions on*, vol. 53, no. 9, pp. 2202–2206, 2006.

[79] H. Liu, Z. Xiong, and J. K. O. Sin, "Implementation and characterization of the double-gate MOSFET using lateral solid-phase epitaxy," *IEEE Transactions on Electron Devices*, vol. 50, no. 6, pp. 1552–1555, 2003.

[80] J. Kedzierski, D. Fried, E. Nowak, T. Kanarsky, J. Rankin, H. Hanafi, W. Natzle, D. Boyd, Y. Zhang, R. Roy, J. Newbury, C. Yu, Q. Yang, P. Saunders, C. Willets, A. Johnson, S. P. Cole, H. E. Young, N. Carpenter, D. Rakowski, B. Rainey, P. Cottrell, M. Ieong, and H. S. P. Wong, "High-performance symmetric-gate and CMOS-compatible Vt asymmetric-gate FinFET devices," in *Electron Devices Meeting, 2001. IEDM '01. Technical Digest. International*, pp. 19.5.1–19.5.4, 2001.

[81] C.-W. Lee, I. Ferain, A. Afzalian, R. Yan, N. D. Akhavan, P. Razavi, and J.-P. Colinge, "Performance estimation of junctionless multigate transistors," *Solid-State Electronics*, vol. 54, pp. 97–103, 2 2010.

[82] J.-P. Colinge, A. Kranti, R. Yan, C. Lee, I. Ferain, R. Yu, N. D. Akhavan, and P. Razavi, "Junctionless Nanowire Transistor (JNT): Properties and design guidelines," *Solid-State Electronics*, vol. 65-66, pp. 33–37, 2011.

[83] J.-P. Colinge, C.-W. Lee, I. Ferain, N. D. Akhavan, R. Yan, P. Razavi, R. Yu, A. N. Nazarov, and R. T. Doria, "Reduced electric field in junctionless transistors," *Applied Physics Letters*, vol. 96, no. 7, p. 073510, 2010.

[84] J.-P. Colinge, I. Ferain, A. Kranti, C.-W. Lee, N. D. Akhavan, P. Razavi, R. Yan, and R. Yu, "Junctionless Nanowire Transistor: Complementary Metal-Oxide-Semiconductor Without Junctions," *American Scientific Publishers*, vol. 3, pp. 477–482, 2011.

[85] R. Doria, M. Pavanello, R. Trevisoli, M. De Souza, C.-W. Lee, I. Ferain, N. Akhavan, R. Yan, P. Razavi, R. Yu, A. Kranti, and J. Colinge, "Junctionless Multiple-Gate Transistors for Analog Applications," *Electron Devices, IEEE Transactions on*, vol. 58, no. 8, pp. 2511–2519, 2011.

[86] F. Lime, E. Santana, and B. Iñiguez, "A simple compact model for long-channel junctionless Double Gate MOSFETs," *Solid-State Electronics*, vol. 80, pp. 28–32, 2 2013.

[87] E. Gnani, A. Gnudi, S. Reggiani, and G. Baccarani, "Theory of the Junctionless Nanowire FET," *IEEE Trans. Electron Devices*, vol. 58, no. 9, pp. 2903–2910, 2011.

[88] J.-M. Sallese, N. Chevillon, C. Lallement, B. Iniguez, and F. Pregaldiny, "Charge-Based Modeling of Junctionless Double-Gate Field-Effect Transistors," *IEEE Trans. Electron Devices*, vol. 58, no. 8, pp. 2628–2637, 2011.

[89] A. Cerdeira, M. Estrada, B. Iniguez, R. D. Trevisoli, R. T. Doria, M. de Souza, and M. A. Pavanello, "Charge-based continuous model for long-channel Symmetric Double-Gate Junctionless Transistors," *Solid-State Electronics*, vol. 85, pp. 59–63, 7 2013.

[90] J. P. Duarte, M.-S. Kim, S.-J. Choi, and Y.-K. Choi, "A Compact Model of Quantum Electron Density at the Subthreshold Region for Double-Gate Junctionless Transistors," *IEEE Transactions on Electron Devices*, vol. 59, no. 4, pp. 1008–1012, April 2012.

[91] E. Gnani, A. Gnudi, S. Reggiani, and G. Baccarani, "Physical Model of the Junctionless UTB SOI-FET," *Electron Devices, IEEE Transactions on*, vol. 59, no. 4, pp. 941–948, April 2012.

[92] M. Berthome, S. Barraud, A. Ionescu, and T. Ernst, "Physically-based, multi-architecture, analytical model for junctionless transistors," in *Ultimate Integration on Silicon (ULIS), 2011 12th International Conference on*, pp. 1–4, 2011.

[93] R. Trevisoli, R. Doria, M. De Souza, and M. Pavanello, "Drain current model for junctionless nanowire transistors," in *Devices, Circuits and Systems (ICCDCS), 2012 8th International Caribbean Conference on*, pp. 1–4, 2012.

[94] J. P. Duarte, S.-J. Choi, and Y.-K. Choi, "A Full-Range Drain Current Model for Double-Gate Junctionless Transistors," *IEEE Trans. Electron Devices*, vol. 58, no. 12, pp. 4219–4225, 2011.

[95] J. Xiao-Shi, L. Xi, K. Hyuck-In, and L. Jong-Ho, "A Continuous Current Model of Accumulation Mode (Junctionless) Cylindrical Surrounding-Gate Nanowire MOSFETs," *Chinese Physics Letters*, vol. 30, no. 3, p. 038502, 2013.

[96] Z. Chen, Y. Xiao, M. Tang, Y. Xiong, J. Huang, J. Li, X. Gu, and Y. Zhou, "Surface-Potential-Based Drain Current Model for Long-Channel Junctionless Double-Gate MOSFETs," *Electron Devices, IEEE Transactions on*, vol. 59, no. 12, pp. 3292–3298, Dec. 2012.

[97] J. Duarte, S.-J. Choi, D.-I. Moon, and Y.-K. Choi, "Simple Analytical Bulk Current Model for Long-Channel Double-Gate Junctionless Transistors," *Electron Device Letters, IEEE*, vol. 32, no. 6, pp. 704–706, 2011.

[98] F. Jazaeri, L. Barbut, and J.-M. Sallese, "Trans-Capacitance Modeling in Junctionless Symmetric Double-Gate MOSFETs," *Electron Devices, IEEE Transactions on*, vol. 60, no. 12, pp. 4034–4040, 2013.

[99] R. D. Trevisoli, R. T. Doria, M. de Souza, and M. A. Pavanello, "Threshold voltage in junctionless nanowire transistors," *SEMICONDUCTOR SCIENCE AND TECHNOLOGY*, vol. 26 (2011), 2011.

[100] R. D. Trevisoli, R. T. Doria, M. de Souza, and M. A. Pavanello, "A physically-based threshold voltage definition, extraction and analytical model for junctionless nanowire transistors," *Solid-State Electronics*, vol. 90, pp. 12 – 17, 2013. Selected papers from EUROSOI 2012.

[101] Y. Taur, H.-P. Chen, W. Wang, S.-H. Lo, and C. Wann, "On-Off Charge-Voltage Characteristics and Dopant Number Fluctuation Effects in Junctionless Double-Gate MOSFETs," *Electron Devices, IEEE Transactions on*, vol. 59, no. 3, pp. 863–866, 2012.

[102] A. Cerdeira, F. Avila, B. Iniguez, M. de Souza, M. Pavanello, and M. Estrada, "Compact core model for Symmetric Double-Gate Junctionless Transistors," *Solid-State Electronics*, vol. 94, no. 0, pp. 91 – 97, 2014.

[103] C. Li, Y. Zhuang, S. Di, and R. Han, "Subthreshold Behavior Models for Nanoscale Short-Channel Junctionless Cylindrical Surrounding-Gate MOSFETs," *Electron Devices, IEEE Transactions on*, vol. 60, no. 11, pp. 3655–3662, 2013.

[104] A. Gnudi, S. Reggiani, E. Gnani, and G. Baccarani, "Semianalytical Model of the Subthreshold Current in Short-Channel Junctionless Symmetric Double-Gate Field-Effect Transistors," *Electron Devices, IEEE Transactions on*, vol. 60, no. 4, pp. 1342–1348, 2013.

[105] J.-H. Woo, J.-M. Choi, and Y.-K. Choi, "Analytical Threshold Voltage Model of Junctionless Double-Gate MOSFETs With Localized Charges," *Electron Devices, IEEE Transactions on*, vol. 60, no. 9, pp. 2951–2955, 2013.

[106] R. Trevisoli, R. Doria, M. De Souza, S. Das, I. Ferain, and M. Pavanello, "Surface-Potential-Based Drain Current Analytical Model for Triple-Gate Junctionless Nanowire Transistors," *Electron Devices, IEEE Transactions on*, vol. 59, no. 12, pp. 3510–3518, 2012.

[107] G. Hu, P. Xiang, Z. Ding, R. Liu, L. Wang, and T.-A. Tang, "Analytical Models for Electric Potential, Threshold Voltage, and Subthreshold Swing of Junctionless Surrounding-Gate Transistors," *Electron Devices, IEEE Transactions on*, vol. 61, no. 3, pp. 688–695, 2014.

[108] R. T. Doria, R. D. Trevisoli, and M. A. Pavanello, "Impact of the Series Resistance in the I-V Characteristics of nMOS Junctionless Nanowire Transistors," *ECS Transactions*, vol. 39, pp. 231–238, Sept. 2011.

[109] D.-Y. Jeon, S. J. Park, M. Mouis, S. Barraud, G.-T. Kim, and G. Ghibaudo, "Low-temperature electrical characterization of junctionless transistors," *Solid-State Electronics*, vol. 80, no. 0, pp. 135 – 141, 2013.

[110] T. Rudenko, A. Nazarov, R. Yu, S. Barraud, K. Cherkaoui, P. Razavi, and G. Fagas, "Electron mobility in heavily doped junctionless nanowire SOI MOSFETs," *Microelectronic Engineering*, vol. 109, no. 0, pp. 326 – 329, 2013. Insulating Films on Semiconductors 2013.

[111] C.-H. Park, M.-D. Ko, K.-H. Kim, R.-H. Baek, C.-W. Sohn, C. K. Baek, S. Park, M. Deen, Y.-H. Jeong, and J.-S. Lee, "Electrical characteristics of 20-nm junctionless Si nanowire transistors," *Solid-State Electronics*, vol. 73, pp. 7–10, 2012.

[112] D.-Y. Jeon, S. Park, M. Mouis, M. Berthome, S. Barraud, G.-T. Kim, and G. Ghibaudo, "Revisited parameter extraction methodology for electrical characterization of junctionless transistors," *Solid-State Electronics*, vol. 90, pp. 86 – 93, 2013. Selected papers from EUROSOI 2012.

[113] S. M. Lee and J. T. Park, "The Impact of Substrate Bias on the Steep Subthreshold Slope in Junctionless MuGFETs," *Electron Devices, IEEE Transactions on*, vol. 60, no. 11, pp. 3856–3861, 2013.

[114] R. Doria Trevisoli, R. Trevisoli Doria, M. de Souza, S. Das, I. Ferain, and M. Antonio Pavanello, "The zero temperature coefficient in junctionless nanowire transistors," *Applied Physics Letters*, vol. 101, no. 6, 2012.

[115] R. Rios, A. Cappellani, M. Armstrong, A. Budrevich, H. Gomez, R. Pai, N. Rahhal-orabi, and K. Kuhn, "Comparison of Junctionless and Conventional Trigate Transistors With Lg Down to 26 nm," *Electron Device Letters*, vol. 32, no. 9, pp. 1170 – 1172, 2011.

[116] G. Giusi and A. Lucibello, "Variability of the Drain Current in Junctionless Nanotransistors Induced by Random Dopant Fluctuation," *Electron Devices, IEEE Transactions on*, vol. 61, no. 3, pp. 702–706, 2014.

[117] C. Wan, J. Zhou, Y. Shi, and Q. Wan, "Classical Conditioning Mimicked in Junctionless IZO Electric-Double-Layer Thin-Film Transistors," *Electron Device Letters, IEEE*, vol. 35, no. 3, pp. 414–416, 2014.

[118] Y. Song, C. Zhang, R. Dowdy, K. Chabak, P. Mohseni, W. Choi, and X. Li, "III-V Junctionless Gate-All-Around Nanowire MOSFETs for High Linearity Low Power Applications," *Electron Device Letters, IEEE*, vol. 35, no. 3, pp. 324–326, 2014.

[119] K. Simonyi, *Theoretische Elektrotechnik*. Deutscher Verlag der Wissenschaften, 1976.

[120] A. Kloes, *Analytische modellierung mehrdimensionaler effkte in submikron-mosfet's*. PhD thesis, Technische Hochschule Darmstadt, 1997.

[121] I. N. Bronstein and K. A. Semendjajew, *Bronstein Taschenbuch der Mathematik*. Harri Deutsch, 1995.

[122] A. Kloes and A. Kostka, "A new analytical method of solving 2D Poisson's equation in MOS devices applied to threshold voltage and subthreshold modeling," *Solid-State Electronics*, vol. 39, no. 12, pp. 1761 – 1775, 1996.

[123] M. Schwarz, M. Weidemann, A. Kloes, and B. Iniguez, "2D analytical calculation of the electrostatic potential in lightly doped Schottky barrier Double-Gate MOSFET," *Solid-State Electronics*, vol. 54 (11) (2010), 2010.

[124] M. Schwarz, T. Holtij, A. Kloes, and B. Iniguez, "2D analytical calculation of the electric field in lightly doped Schottky barrier double-gate MOSFETs and estimation of the tunneling/thermionic current," *Solid-State Electronics*, vol. 63, no. 1, pp. 119 – 129, 2011.

[125] T. Holtij, M. Schwarz, A. Kloes, and B. Iniguez, "2D Analytical Modeling of the Potential in Doped Multiple-Gate-FETs Including Inversion Charge," in *Fringe Poster Session at ESSDERC/ESSCIRC, Helsinki, Finland, 2011*, 2011.

[126] T. Holtij, M. Schwarz, A. Kloes, and B. Iniguez, "2D Analytical Modeling of the Potential within Juntionless DG MOSFETs in the Subthreshold Regime," in *Eighth Workshop of the Thematic Network on Silicon on Insulator technology, devices and circuits, EUROSOI*, 2012.

[127] T. Holtij, M. Schwarz, A. Kloes, and B. Iniguez, "2D analytical potential modeling of junctionless DG MOSFETs in subthreshold region including proposal for calculating the threshold voltage," in *Ultimate Integration on Silicon (ULIS), 2012 13th International Conference on*, pp. 81–84, 2012.

[128] T. Holtij, M. Schwarz, A. Kloes, and B. Iniguez, "Analytical 2D Modeling of Junctionless and Junction-Based Short-Channel Multigate MOSFETs," in *Fringe Poster Session at ESSDERC/ESSCIRC, Bordeaux, France, 2012*, 2012.

[129] T. Holtij, M. Schwarz, A. Kloes, and B. Iniguez, "2D Analytical Calculation of the Parasitic Source/Drain Resistances in DG-MOSFETs Using the Conformal Mapping Technique," *IETE Journal of Research*, vol. 58, pp. 205 – 213, 2012.

[130] D. B., "ETSOI technology tutorial, EUROSOI, Granada, Spain," in *Seventh Workshop of the Thematic Network on Silicon on Insulator technology, devices and circuits, EUROSOI*, 2012.

[131] T. Holtij, M. Schwarz, A. Kloes, and B. Iniguez, "Threshold voltage, and 2D potential modeling within short-channel junctionless DG MOSFETs in subthreshold region," *Solid-State Electronics*, vol. 90, pp. 107 – 115, 2013. Selected papers from EUROSOI 2012.

[132] T. Holtij, M. Schwarz, M. Graef, F. Hain, A. Kloes, and B. Iniguez, "2D Current Model for Junctionless DG MOSFETs," in *Ninth Workshop of the Thematic Network on Silicon on Insulator Technology, Devices and Circuits, EuroSOI 2013*, 2013.

[133] A. Tsormpatzoglou, C. Dimitriadis, R. Clerc, Q. Rafhay, G. Pananakakis, and G. Ghibaudo, "Semi-Analytical Modeling of Short-Channel Effects in Si and Ge Symmetrical Double-Gate MOSFETs," *Electron Devices, IEEE Transactions on*, vol. 54, no. 8, pp. 1943–1952, 2007.

[134] T. Dutta, Q. Rafhay, G. Pananakakis, and G. Ghibaudo, "Modeling of the Impact of Source/Drain Regions on Short Channel Effects in MOSFETs," in *ULIS, Warwick, 2013*, 2013.

[135] F. Djeffal, Z. Ghoggali, Z. Dibi, and N. Lakhdar, "Analytical analysis of nanoscale multiple gate MOSFETs including effects of hot-carrier induced interface charges," *Microelectronics Reliability*, vol. 49, no. 4, pp. 377 – 381, 2009.

[136] M. Schwarz, M. Weidemann, A. Kloes, and B. Iniguez, "Analytical compact modeling framework for the 2D electrostatics in lightly doped double-gate MOSFETs," *Solid-State Electronics*, vol. 69, no. 0, pp. 72 – 84, 2012.

[137] M. Schwarz, T. Holtij, A. Kloes, and B. Iniguez, "Compact modeling solutions for short-channel SOI Schottky barrier MOSFETs," *Solid-State Electronics*, vol. 82, pp. 86 – 98, 2013.

[138] A. Kloes, M. Weidemann, D. Goebel, and B. Bosworth, "Three-Dimensional Closed-Form Model for Potential Barrier in Undoped FinFETs Resulting in Analytical Equations for V_T and Subthreshold Slope," *Electron Devices, IEEE Transactions on*, vol. 55, pp. 3467 –3475, dec. 2008.

[139] T. Holtij, M. Graef, F. Hain, A. Kloes, and B. Iniguez, "Compact Model for Short-Channel Junctionless Accumulation Mode Double Gate MOSFETs," *Electron Devices, IEEE Transactions on*, vol. 61, no. 2, pp. 288–299, 2014.

[140] T. Holtij, M. Graef, F. Hain, A. Kloes, and B. Iniguez, "Unified charge model for short-channel junctionless double gate MOSFETs," in *Mixed Design of Integrated Circuits and Systems (MIXDES), 2013 Proceedings of the 20th International Conference*, pp. 75–80, 2013.

[141] J. He, X. Xuemei, M. Chan, C.-H. Lin, A. Niknejad, and C. Hu, "A non-charge-sheet based analytical model of undoped symmetric double-gate MOSFETs using SPP approach," in *Quality Electronic Design, 2004. Proceedings. 5th International Symposium on*, pp. 45 – 50, 2004.

[142] F. Pregaldiny, C. Lallement, and D. Mathiot, "A simple efficient model of parasitic capacitances of deep-submicron LDD MOSFETs," *Solid-State Electronics*, vol. 46, no. 12, pp. 2191 – 2198, 2002.

[143] T. Smedes and F. Klaassen, "Effects of the lightly doped drain configuration on capacitance characteristics of submicron mosfets," in *Electron Devices Meeting, 1990. IEDM '90. Technical Digest., International*, pp. 197–200, 1990.

[144] K. A. Sakallah, Y. T. Yen, and S. S. Greenberg, "A first order charge conserving MOS capacitor model," *IEEE Trans. Computer-Aided Design*, vol. 9, pp. 99–108, 1990.

[145] Z. Zhu, G. Gildenblat, C. Mcandrew, and I.-S. Lim, "Modeling the frequency dependence of MOSFET gate capacitance," in *Microelectronic Test Structures (ICMTS), 2011 IEEE International Conference on*, pp. 13–18, 2011.

[146] S.-Y. Oh, D. Ward, and R. Dutton, "Transient analysis of MOS transistors," *Electron Devices, IEEE Transactions on*, vol. 27, no. 8, pp. 1571–1578, 1980.

[147] B. Yu, W.-Y. Lu, H. Lu, and Y. Taur, "Analytic Charge Model for Surrounding-Gate MOSFETs," *Electron Devices, IEEE Transactions on*, vol. 54, no. 3, pp. 492–496, 2007.

[148] H. Borli, S. Kolberg, and T. A. Fjeldly, "Capacitance modeling of short-channel double-gate MOSFETs," *Solid-State Electronics*, vol. 52, no. 10, pp. 1486 – 1490, 2008. Papers Selected from the International Semiconductor Device Research Symposium 2007 at ISDRS 2007.

[149] Y. Taur and T. H. Ning, *Fundamentals of Modern VLSI Devices*. Cambridge University Press, 1998.

[150] S. Hareland, S. Jallepalli, W.-K. Shih, H. Wang, G. Chindalore, A. Tasch, and C. Maziar, "A physically-based model for quantization effects in hole inversion layers," *Electron Devices, IEEE Transactions on*, vol. 45, no. 1, pp. 179–186, 1998.

[151] A. Amara and O. Rozeau, eds., *Planar Double-Gate Transistor - From Technology to Circuit*. Springer Netherlands, 2009.

[152] T. Holtij, M. Graef, F. M. Hain, A. Kloes, and B. Iniguez, "Modeling of Quantization Effects in Nanoscale DG Junctionless MOSFETs," in *Tenth Workshop of the Thematic Network on Silicon on Insulator Technology, Devices and Circuits, EuroSOI 2014*, 2014.

[153] T. Holtij, M. Schwarz, M. Graef, F. Hain, A. Kloes, and B. Iniguez, "Model for investigation of Ion/Ioff ratios in short-channel junctionless double gate MOSFETs," in *Ultimate Integration on Silicon (ULIS), 2013 14th International Conference on*, pp. 85–88, 2013.

[154] T. Holtij, M. Graef, A. Kloes, and B. Iniguez, "3-D Compact Model for Nanoscale Junctionless Triple-Gate Nanowire MOSFETs." accepted for presentation at: ESSDERC/ESSCIRC, Venice, Italy, 2014, 2014.

[155] A. Kloes, M. Weidemann, and M. Schwarz, "Analytical current equation for short channel SOI multigate FETs including 3D effects," *Solid-State Electronics*, vol. 54, no. 11, pp. 1408 – 1415, 2010.

[156] K. Papathanasiou, C. Theodorou, A. Tsormpatzoglou, D. Tassis, C. Dimitriadis, M. Bucher, and G. Ghibaudo, "Symmetrical unified compact model of short-channel double-gate MOSFETs," *Solid-State Electronics*, vol. 69, no. 0, pp. 55 – 61, 2012.

[157] N. Fasarakis, A. Tsormpatzoglou, D. Tassis, I. Pappas, K. Papathanasiou, M. Bucher, G. Ghibaudo, and C. Dimitriadis, "Compact Model of Drain Current in Short-Channel Triple-Gate FinFETs," *Electron Devices, IEEE Transactions on*, vol. 59, no. 7, pp. 1891–1898, 2012.

[158] S. Barraud, M. Berthome, R. Coquand, M. Casse, T. Ernst, M. P. Samson, P. Perreau, K. Bourdelle, O. Faynot, and T. Poiroux, "Scaling of Trigate Junctionless Nanowire MOSFET With Gate Length Down to 13 nm," *Electron Device Letters, IEEE*, vol. 33, no. 9, pp. 1225–1227, 2012.

[159] M. Lundstrom and Z. Ren, "Essential physics of carrier transport in nanoscale MOSFETs," *Electron Devices, IEEE Transactions on*, vol. 49, no. 1, pp. 133–141, 2002.

[160] A. Rahman and M. Lundstrom, "A compact scattering model for the nanoscale double-gate MOSFET," *Electron Devices, IEEE Transactions on*, vol. 49, no. 3, pp. 481–489, 2002.

[161] Y.-K. Choi, D. Ha, T.-J. King, and J. Bokor, "Investigation of Gate-Induced Drain Leakage (GIDL) Current in Thin Body Devices: Single-Gate Ultra-Thin Body, Symmetrical Double-Gate, and Asymmetrical Double-Gate MOSFETs," *Japanese Journal of Applied Physics*, vol. 42, no. 4S, p. 2073, 2003.

[162] MathWorks, *Matlab 2013b*, August 2013.