UNIVERSITAT POLITÈCNICA
DE CATALUNYA
BARCELONATECH

DEPARTAMENT D'ENGINYERIA ELECTRÒNICA

Variability and Reliability Analysis of Carbon Nanotube Technology in the Presence of Manufacturing Imperfections

by

Carmen G. Almudéver

A thesis submitted in partial fulfillment
for the degree of Doctor of Philosophy
in the Universitat Politécnica de Catalunya
within the Doctoral Program in Electronic Engineering

Thesis advisor: **Antonio Rubio**

June 2014

A Vic y Áurea. Mis amores, mi alegría, mi vida.

UNIVERSITAT POLITÈCNICA DE CATALUNYA

Abstract

Departament d'Enginyería Electrònica

Doctor of Philosophy

by Carmen G. Almudéver

In 1925, Lilienfeld patented the basic principle of field effect transistor (FET). Thirty-four years later, Kahng and Atalla invented the MOSFET. Since that time, it has become the most widely used type of transistor in Integrated Circuits (ICs) and then the most important device in the electronics industry. Progress in the field for at least the last 40 years has followed an exponential behavior in accordance with Moore's Law. That is, in order to achieve higher densities and performance at lower power consumption, MOS devices have been scaled down. But this aggressive scaling down of the physical dimensions of MOSFETs has required the introduction of a wide variety of innovative factors to ensure that they could still be properly manufactured. Transistors have experienced an amazing journey in the last 10 years starting with strained channel CMOS transistors at 90nm, carrying on the introduction of the high-k/metal-gate silicon CMOS transistors at 45nm until the use of the multiple-gate transistor architectures at 22nm and at recently achieved 14nm technology node. But, what technology will be able to produce sub-10nm transistors?

Different novel materials and devices are being investigated. As an extension and enhancement to current MOSFETs some promising devices are n-type III-V and p-type Germanium FETs, Nanowire and Tunnel FETs, Graphene FETs and Carbon Nanotube FETs. Also, non-conventional FETs and other charge-based information carrier devices and alternative information processing devices are being studied.

This thesis is focused on carbon nanotube technology as a possible option for sub-10nm transistors. In recent years, carbon nanotubes (CNTs) have been attracting considerable attention in the field of nanotechnology. They are considered to be a promising substitute for silicon channel because of their small size, unusual geometry (1D structure), and extraordinary electronic properties, including excellent carrier mobility and quasi-ballistic transport. In the same way, carbon nanotube field-effect transistors (CNFETs) could be potential substitutes for MOSFETs. Ideal CNFETs (meaning all CNTs in the transistor behave as semiconductors, have the same diameter and doping level, and are aligned and well-positioned) are predicted to be 5x faster than silicon CMOS, while consuming the same power. However, nowadays CNFETs are also affected by manufacturing variability, and several significant challenges must be overcome before these benefits can be achieved. Certain CNFET manufacturing imperfections, such as CNT diameter and doping variations, mispositioned and misaligned CNTs, high metal-CNT contact resistance, the presence of metallic CNTs (m-CNTs), and CNT density variations, can affect CNFET performance and reliability and must be addressed.

The main objective of this thesis is to analyze the impact of the current manufacturing challenges on multi-channel CNFET performance from the point of view of variability and reliability and at different levels, device and circuit level. Assuming that CNFETs are not ideal or non-homogeneous because of today CNFET manufacturing imperfections, we propose a methodology of analysis that based on a CNFET ideal compact model is able to simulate heterogeneous or non-ideal CNFETs; that is, transistors with different number of tubes that have different diameters, are not uniformly spaced, have different source/drain doping levels, and, most importantly, are made up not only of semiconducting CNTs but also metallic ones. This method will allow us to evaluate how CNT-specific variations [1] affect CNFET device characteristics and parameters and CNFET digital circuit performance. Furthermore, we also derive a CNFET failure model and propose an alternative technique based on fault-tolerant architectures to deal with the presence of m-CNTs, one of the main causes of failure in CNFET circuits.

[1] CNT-specific variations are variations resulting from CNFET manufacturing imperfections. These include CNT diameter, doping, alignment, CNT type variations (m-CNT or s-CNT), and CNT density variations.

Acknowledgements

Con estas palabras me gustaría agradecer a toda aquella gente que me ha acompañado durante esta increíble etapa.

A mi director de tesis Antonio Rubio, por transmitirme parte de su inmenso conocimiento y su entusiasmo por la investigación. Gracias por todos estos años; por tu apoyo, tu generosidad y tu ilusión.

To Alexandre Schmid, for the amazing stay at EPFL and his valuable advice.

To Sorin Cotofana, for his useful visits and nice talks.

A Montse Nafria, Rosana Rodriguez y Javier Martin por su colaboración y su buen hacer.

A Francesc Perez-Murano y a la gente del CNM por su colaboración.

A mis compañeros del grupo HIPICS, Nivard, Jordi, Esteve, Sergio, Peyman, Gerhard, Francesc y Antonio por su gran ayuda.

A mis compañeras de Departamento de Ingeniería Electrónica, Gema, Mónica C., Mónica, Sandra y Ana por las risas y las divertidas cenas de chicas.

En general a toda la gente del departamento, estudiantes de doctorado, profesores, técnicos y gente de administración por el día a día y hacer que mi paso por el departamento haya sido una experiencia inolvidable.

A mis amigos y mi gente de Barcelona. Amparo, Alex, Elena, María, Mari, Topi, Patri, Gochi, Iván, Jordi, Aida, Figs y Silvia.

A mi familia. Mis padres, Paco y Alicia y mis hermanas, María y Lola. Gracias por creer siempre en mi y vuestro apoyo incondicional. Us estime.

A mi otra familia, Auri, Vicente, Mario, Carmen, Daniela, Inma, Jaime y Conchín. Gracias por vuestra generosidad y estar siempre.

Finalmente, a mi marido Vic y a la niña de mis ojos Áurea. Mi mejor y gran apoyo. Sin vosotros nada de esto tiene sentido.

Contents

List of Figures

List of Tables

Abbreviations

CMOS	**C**omplementary **M**etal **O**xide **S**emiconductor
CNT	**C**arbon **N**anotube
CVD	**C**hemical **V**apor **D**eposition
CNFET	**C**arbon **N**anotube **F**ield-**E**ffect **T**ransistor
EDP	**E**nergy- **D**elay **P**roduct
ERD	**E**merging **R**esearch **D**evices
FET	**F**ield-**E**ffect **T**ransistor
GNR	**G**raphene **N**anoribbon
GNRFET	**G**raphene **N**anoribbon **F**ield-**E**ffect **T**ransistor
IC	**I**ntegrated **C**ircuit
ITRS	**I**nternational **T**echnology **R**oadmap for **S**emiconductors
m-CNT	**M**etallic **C**arbon **N**anotube
MIPS	**M**illion **I**nstructions **P**er **S**econd
MOS	**M**etal **O**xide **S**emiconductor
MOSFET	**M**etal **O**xide **S**emiconductor **F**ield-**E**ffect **T**ransistor
NM	**N**oise **M**argin
MWNT	**M**ulti **W**alled **C**arbon **N**anotube
NWFET	**N**anowire **F**ield-**E**ffect **T**ransistor
QCE	**Q**uantum **C**onfinement **E**ffect
RF	**R**adio **F**requency
s-CNT	**S**emiconducting **C**arbon **N**anotube
S/D	**S**ource/**D**rain
SB	**S**chottky **B**arrier
SNM	**S**tatic **N**oise **M**argin
SRAM	**S**tatic **R**andom **A**ccess **M**emory

SS	**S**ubthreshold **S**lope
SDB	**S**ingle **D**evice **B**reakdown
SWNT	**S**ingle **W**alled **C**arbon **N**anotube
VLSI	**V**ery **L**arge **S**cale **I**ntegration
VMR	**V**LSI-compatible **M**etallic-CNT **R**emoval
VTC	**V**oltage **T**ransfer **C**haracteristic

Chapter 1

Introduction

The idea of a technology roadmap for semiconductors can be traced back to a paper by Gordon Moore in 1965 [1], in which he stated that the number of devices that could be incorporated per integrated circuit would increase exponentially over time. Since 1970, the number of components per chip has doubled every two years. This trend has become known as Moore's Law.

The down-scaling of the transistors has been the most important and effective way for achieving higher chip densities and performance logic CMOS operation with low power and then the principal driver for the semiconductor technology roadmap for more than 40 years. But since the Nanoage begun, where transistors' dimensions are below the 100nm range, the dimensional scaling of CMOS is approaching a supposed fundamental limit; as devices advance toward a few tens of nanometers "the conventional scaling" of devices is not enough. This is driving interest in new technologies for heterogeneous integration of multiple functions (labeled as "More than Moore"), and new information processing devices and architectures (also known as "Beyond CMOS") [2].

This chapter reviews the evolution of the transistors in the last 10 years in Section 1.1 and the most relevant emerging research devices in Section 1.2, respectively. The outline of the thesis is presented in Section 1.3.

1.1 From Microelectronics to Nanoelectronics

Silicon-based ICs have experienced an extraordinary growth since the invention and demonstration of the first bipolar transistor in 1947 [3], the first planar IC in 1961 [4], and the first MOSFET in 1964 [5]. From then on, the semiconductor industry has invested billions and billions of dollars to improve their products, and its technological progress is exemplified by leading edge products such as microprocessors containing billions of transistors and operating at 1GHz or more.

This rapid technological progress has been possible thanks to the reduction of the transistor dimensions. With each new generation of technology, not only does the manufacturing process become more economical, but the individual transistors also become smaller and faster, and require less power. This dimensional scaling of the devices has allowed achieving higher and higher chip density and performance and they have been doubled every two years as Gordon Moore predicted in 1965 in his Moore's Law [1], as illustrated in Figure 1.1.

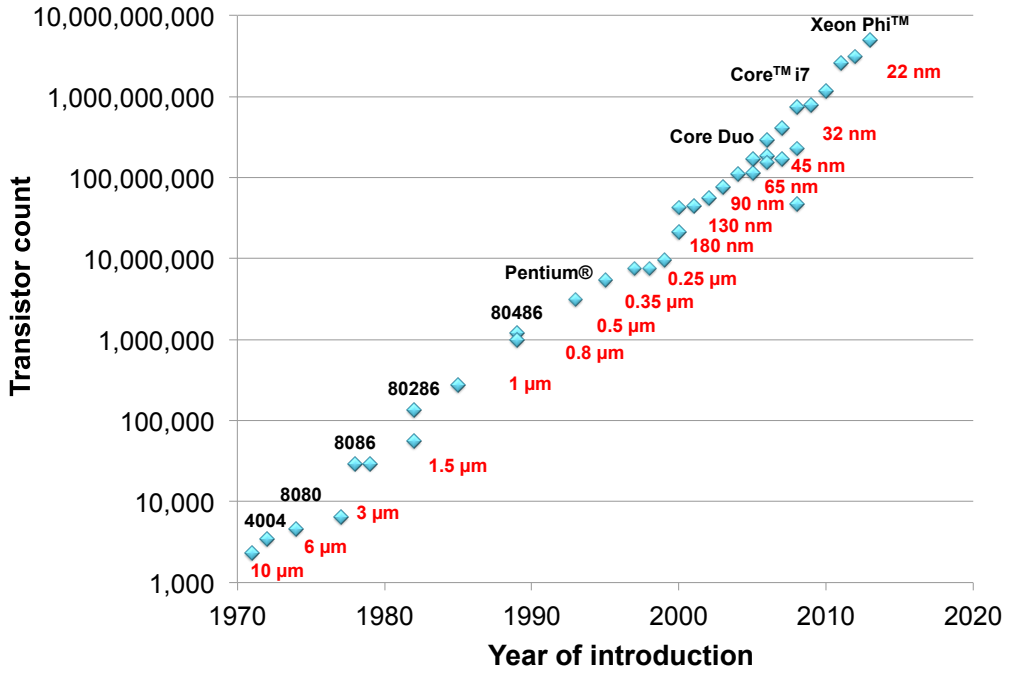


FIGURE 1.1: Transistor count of Intel's processors and sizes of semiconductor manufacturing process nodes against dates of introduction. (Source: Intel Corporation)

Whereas the first microprocessor (4004 delivered in 1971) had a complexity of 2.300 transistors with a minimum feature size of 10 μm, and a maximum clock speed of 1 MHz, today's state-of-the-art microprocessors are made up of more than 1 billion of transistors with a minimum featured size of 22 nm, which operate 50,000 times faster than the early transistors. It is worth noting that Intel presented its first 14nm processor, called Core M, in the last Computex computer trade show (June 4, 2014), but it will not be commercialized until October-December of this year.

However, since the industry went into the current Nano Era in which the devices dimensions are smaller than 100nm, the performance enhancement of CMOS through the device scaling such as shrinking the gate length and thinning the gate oxide has become more and more difficult and challenging, because of several physical limitations in miniaturization of MOSFETs. Thus, the introduction of new device technologies and materials has been required. In the past decade, the semiconductor industry has implemented several innovations to help continue to meet the Moore's Law. As it is shown in Figure 1.2, in 2003 the 90-nm technology node used strain engineering to further increase the performance of silicon transistors, in 2007 high-k metal gate was introduced in 45-nm technology node, multigate structures were used in 22nm and also in the recent 14nm. At this point, different new devices for information processing and memory, new technologies for heterogeneous integration of multiple functions, and new paradigms for systems architecture are being investigated [6]- [9]. In the next section the main emerging research logic devices will be reviewed.

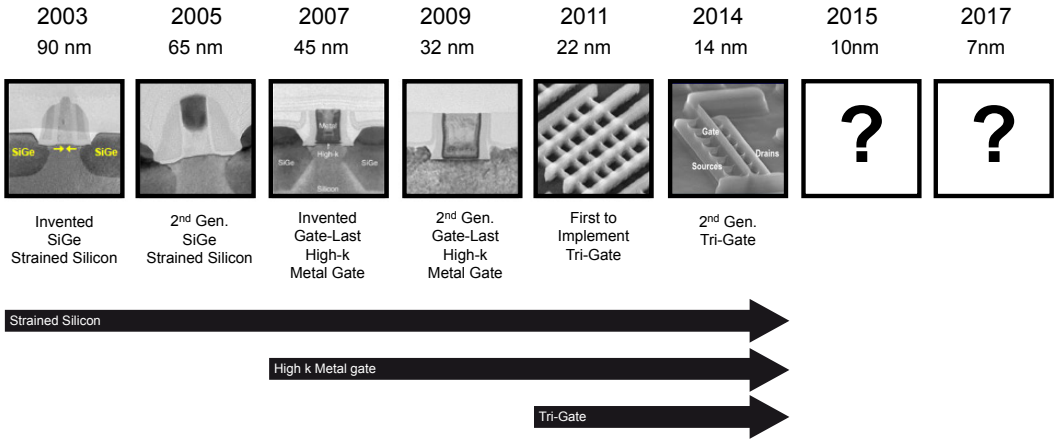


FIGURE 1.2: Intel technology roadmap. (Source: Intel Corporation)

1.2 Nanodevices

Several nanodevices are being investigated today as a possible replacement of Si-transistors for both memory and logic. In this section we will focus on these emerging research logic devices. The International Technology Roadmap for Semiconductors (ITRS) [2] classifies these logic devices in three categories (Figure 1.3): 1) MOSFETs: Extending MOSFETs to the end of the roadmap, 2) Charge based beyond CMOS: Non-Conventional FETs and other Charge-based Information Carrier Devices, and 3) Alternative Information Processing Devices. In the following subsections we present a review of the devices that belong to group 1 because they are the most likely candidates for the next generation of transistors.

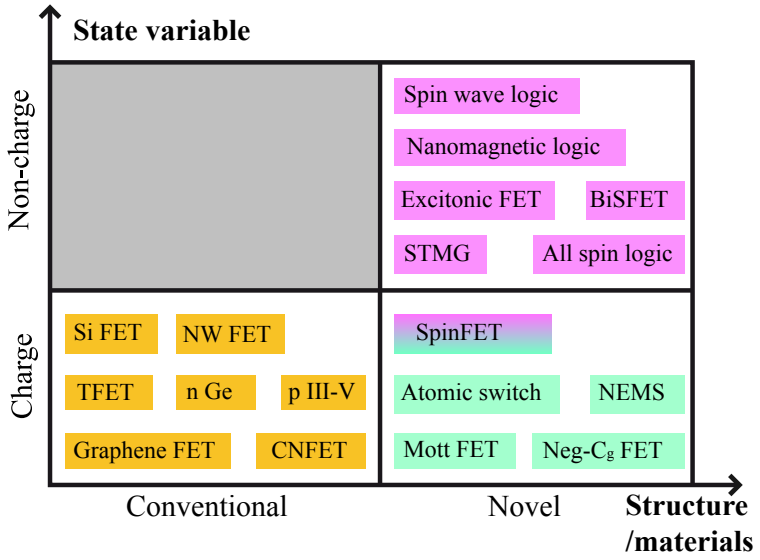


FIGURE 1.3: Taxonomy of options for emerging logic devices. (Source: ITRS 2013)

1.2.1 Alternative Channel MOSFETs

1.2.1.1 N-type III/V and Ge Channel Replacement Devices

Recently, there has been focused interest in the solid-state device community in researching the use of non-silicon materials that have high-mobility charge carriers (Table 1.1), to replace the current silicon-based transistor channel such as germanium and III-V compounds.

TABLE 1.1: Carrier mobility of Si, Ge and a few III-V compounds.

Semiconductor	Electron mobility (cm^2/Vs)	Hole mobility (cm^2/Vs)
Si	1,500	450
Ge	3,900	1,900
GaAs	8,500	400
InAs	33,000	460
InSb	80,000	1,250
InP	4,600	150

Use of III-V compound semiconductors as n-type channel replacement materials has attracted great attention because of their extraordinary electron mobilities. In InGaAs or InAs, the electron mobility is more than ten times higher than in silicon (10000 $cm^2V^{-1}s^{-1}$ and 33000 $cm^2V^{-1}s^{-1}$, respectively). In addition, Sb-based compound semiconductors show both high electron and high hole mobility, such as InSb that exhibits electron mobility of 80000 $cm^2V^{-1}s^{-1}$ and hole mobility of 1250 $cm^2V^{-1}s^{-1}$. The outstanding frequency response of III-V transistors is also frequently invoked. For example, current-gain and power-gain cutoff frequencies of InGaAs-based high-electron-mobility transistors (HEMTs) exceed 600 GHz and 1 THz, respectively [10]-[12]. There have already been experimental demonstrations on PMOS transistors using III-V compounds (GaAs, InGaAs, GaSb or InGaSb) and it has been also demonstrated that their hole mobility can be improved by introducing strain [13]. However, the development of III-V p-channel MOSFETs lags behind. At the moment, it does not seem that any III-V PMOS transistor will have a performance advantage over a Ge device. Although III-V compound semiconductor n-channel MOSFETs are considered viable candidates to extend CMOS to the end of the Roadmap, the high volume production of III-V devices presents several challenges: 1) the need for high quality, 2) low EOT gate dielectrics, 3) damage-free low resistivity junctions, and 4) hetero-integration on a VLSI compatible silicon substrates.

Germanium has the highest p-type mobility of all of the known semiconductor materials. Compared to Si, pure Ge offers 2x higher mobility for electrons (3900 $cm^2V^{-1}s^{-1}$) and 4x higher mobility for holes 1900 $cm^2V^{-1}s^{-1}$. The operation of short-channel Ge pFETs with gate lengths of less than 80nm have been reported, but functioning Ge nFETs still needs to be demonstrated [13]. The actual electron mobility of n-type Ge in MOSFETs is much worse than electron mobility of n-type Si FET applications. The

key to enhancing the mobility is the improvement of Ge/dielectric interface quality. Different techniques such as high-temperature oxidation, high pressure oxidation, and ozone oxidation, of Ge have been proposed to enhance the Ge/oxide interface [15]-[17] and as a result excellent electron mobility n-type Ge MOSFETs have been obtained [18][19]. Another path for improving performance of Ge n-channel MOSFETs is the optimization of the surface/directional crystal orientation. In addition to the electron mobility issue, the n-type Ge devices faces other challenges: 1) EOT scaling, and 2) development of lower-resistivity diffusion layers with lower-resistivity metal contacts.

Consequently, future CMOS technology is envisioned as co-integrating III-V compounds (n-channel) and Ge (p-channel) on Si substrates as it is shown in Figure 1.4.

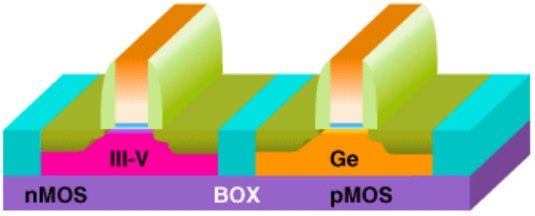


FIGURE 1.4: Combining III-V compounds (nMOS) and Ge (pMOS).

1.2.2 Nanowire/Tube MOSFETs

1.2.2.1 Nanowire Field-Effect Transistors (NWFETs)

A nanowire is a nanostructure that have a thickness or diameter constrained to tens of nanometers or less and an unconstrained length. The nanowires may be composed of a wide variety of materials, including silicon, germanium, different III-V compound semiconductors, II-VI materials, as well as semiconducting oxides.

Nanowire field-effect transistors (NWFETs), gate-all-around or surround gate FETs with a thin nanowire channel, have drawn much attention and have been considered as promising candidates for continuous CMOS scaling since their nonplanar geometry provides superior electrostatic control of the channel than the conventional planar structures. The increasing attention in nanowire research stems from several key factors: their high-yield reproducible electronic properties, cost-effective bottom-up fabrication which circumvents some fabrication challenges, higher carrier mobility by means of the reduction of scattering resulting from the crystalline structure, smooth surfaces and the ability

to produce radial and axial nanowire heterostructures, and better scalability resulting from the fact that diameter of nanowires can be controlled down to well below 10 nm.

Different nanowire transistor structures have been studied, such as junctionless nanowire transistors [20][21], multiple-gate nanowire transistors [22][23] and vertical multi-wire gate-all-around transistor [24] (Figure 1.5). In addition, circuit and system functionality of nanowire devices have been demonstrated, including ring oscillators [25][26], and reconfigurable NWFETs [27] and programmable arrays of non-volatile nanowires that allow to implement different logic gates and digital circuits [23][28].

At low diameters, these nanowires exhibit quantum confinement behavior, i.e, 1-D conduction, that may permit the reduction of short channel effects and other limitations to the scaling of planar MOSFETs, but variations in nanowire dimensions due to fabrication imperfections can lead to perturbations in the carrier potential and scattering that degrade the charge transport characteristics. Also, variations in nanowire diameters may lead to a variation in FET threshold voltage. Then, reducing variability is a key challenge in making nanowire FETs a viable technology [29].

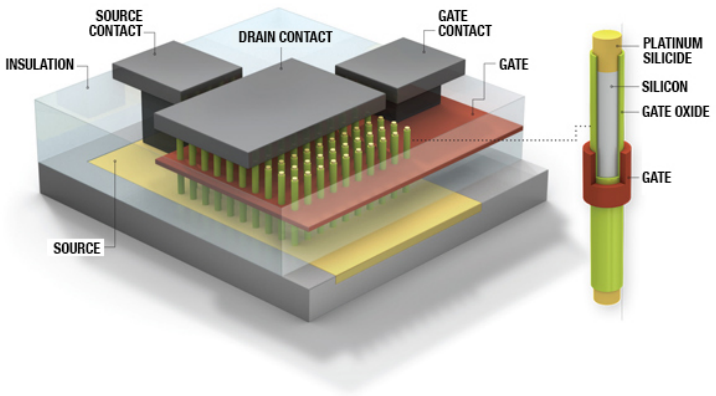


FIGURE 1.5: Structure of a vertical nanowire (multi-tube) FET. (Source: A. Hellemans, IEEE Spectrum [30])

1.2.2.2 Graphene Nanoribbon Field-Effect Transistors (GNRFETs)

Graphene, a single atomic layer of carbon atoms arranged into a two-dimensional (2D) hexagonal lattice shows great potential for nanoelectronic devices. Graphene is of great interest for electronic devices because of its extraordinary properties, including high

carrier mobility for ballistic transport, high carrier velocity for fast switching, and excellent thermal conductivity and mechanical stability. However, the intrinsic zero bandgap (E_G) makes it very difficult to achieve the high on/ off current ratio required from field-effect transistors. Etching or patterning graphene into a few nanometer wide graphene nanoribbon (GNR), a band-gap can be induced [31]-[34].

Graphene Nanoribbon is one of the promising materials for future non-classical devices and nanoelectronic circuits because of its exceptional electronic properties such as the large carrier mobility, the possibility of band gap engineering, and planar structure [35]. On one hand, GNR field-effect transistors (GNRFETs, Figure 1.6) can provide high I_{ON}/I_{OFF} current ratio by introducing non-zero band gap at the expense of reducing the carrier mobility of graphene [36]. On the other hand, GNR FETs still have a problem with low on/off current ratio in the case of wider graphene nanoribbon (high mobility) with the channel length below 10nm [37] and in nanoribbon array devices [38]-[39]. In addition, it is worth noting that due to the atomically thin and nanometer-wide geometries of GNRs, variability and defects are projected to have a larger impact on GNRFET circuit performance and reliability in comparison to the conventional silicon devices [40]. Although the GNR material promises ultra-small, fast, and low-energy FETs, two key effects of variability and defects - leakage and low noise margins - are significant. So, more efforts are required to realize GNR transistors for CMOS.

An important application space for graphene may be radio frequency (RF) with discrete elements and high linearity requirements. There have been many studies aiming at such high-frequency applications [41]-[42].

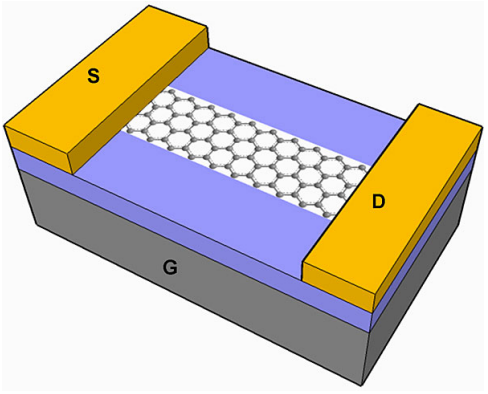


FIGURE 1.6: Schematic of a GNRFET

1.2.2.3 Carbon Nanotube Field-Effect Transistors (CNFETs)

A carbon nanotube (CNT) is a single (single-walled, SWNT) or multiple (multi-walled, MWNT) graphene sheets rolled up to form a hollow cylinder. With diameters of the order of a few nanometers and up to some millimeters in length, CNT is essentially a nearly ideal one-dimensional object. CNTs are characterized by the chiral or roll-up vector (n, m) that is the angle of the atom arrangement along the tube. The chirality determines the kind of CNT, wether it is semiconducting (s-CNT) or metallic (m-CNT) and the diameter (in the nanometer range) of the CNT.

Semiconducting SWNTs (s-CNTs) are considered as a promising replace for silicon due to their small size and excellent carrier mobility and improved electrostatics that are result of their 1D structure. The 1D carrier transport implies a reduced phase space for scattering of the carriers and opens up the possibility of ballistic transport and consequently lower power dissipation. Furthermore, the ultra-thin 1D structure can suppress the short channel effect (SCE) in ultra-short channel devices in terms of electrostatics. Hence, s-CNTs have been used to fabricate Field Effect Transistors.

Carbon nanotube field effect transistors (CNFETs), in which the channel material is made up of one or more CNTs, could be potential substitutes for MOSFETs (Figure 1.7). Exceptional I-V characteristics have been demonstrated in "ideal" CNFET technology (meaning all CNTs in the transistor are semiconducting, have the same diameter and are aligned and well-positioned) [43]. However, there are multiple challenges to achieving this, including: 1) the ability to control de bandgap energy (control of chirality) that results in a mixture of s-CNTs and m-CNTs and CNT diameter variations, 2) positioning of CNTs in required locations and directions, 3) the achievement of uniform spacing between CNTs and high CNT density, 4) controlling the CNT doping process, and 5) formation of low resistance electrical contacts.

In the past years, significant advances have been made in fabricating and characterizing CNFETs. CNFETs with sub-10 nm channel lengths have been demonstrated [44]. Such devices exhibit an impressive subthreshold slope (SS) of 94 $mVdec^{-1}$, current on/off ratio of 10^4, and on-current density of 2.41 $mA/\mu m$, which outperform silicon FETs with comparable channel length. Complementary gate-all-around FETs were fabricated [45]. CNT based ICs including basic logic and arithmetic circuits were demonstrated working under a supply voltage low as 0.4 V [46]. Furthermore, high-performance single-walled

carbon nanotube thin-film transistors were fabricated by single-pass inkjet printing of SWCNTs [47]. The resulting devices exhibit excellent performance with mobility and on/off current ratio exceeding 30 $cm^2V^{-1}s{-}1$ and 10^5, respectively, at low operating voltages. In the last year Stanford's group has developed a carbon nanotube mini computer composed of 178 CNFETs, demonstrating the first time the feasibility of using CNFETs and the related logic circuits to build an operating computer unit [48].

In addition, continuous progress has been achieved for the remaining challenges including: 1) nearly perfectly linear ($> 99.9\%$) aligned arrays of CNTs grown on quartz substrates and CNFET circuits immune to such mispositioned CNTs; 2) multiple-growth and multiple-transfer techniques to increase the CNT density; 3) Enhanced CNT growth methods, sorting CNT techniques and m-CNT removal processes to improve the purity of single chiral semiconducting nanotubes to $\sim 99\%$; 4) the use of low-work-function metal contacts and ALD-based electrostatic doping to achieve functional n-type CNFETs; and 5) the use of graphitic carbon interfacial layers and the selection of a proper work-function metal contact to achieve a low metal-to-CNT contact resistance.

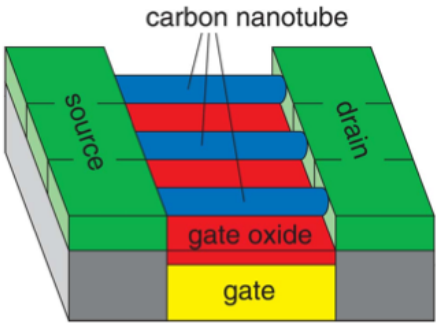


FIGURE 1.7: Schematic of a multi-tube CNFET

1.3 Outline of the Thesis

This thesis aims at providing a complete variability and reliability analysis of CNFET devices and circuits in the presence of CNFET manufacturing imperfections, giving a realistic view of the challenges that CNT technology faces today and evaluating its viability as a possible replacement for silicon devices. The organization of this work is as follows. In chapter 2, the motivation for this thesis and the main objectives are presented. Chapter 3 presents an overview of CNT transistors, showing the evolution of CNFET

technology and its current challenges. In Chapter 4 a methodology for multi-channel CNFET variability estimation is proposed. It is used to analyze the impact of CNFET manufacturing imperfections on CNFET devices in Chapter 4 and on CNFET digital circuits performance in Chapter 6. In Chapter 5, the reliability of CNFET devices in the presence of m-CNTs and CNT density and count variations is discussed. A CNFET device failure model is derived. In Chapter 6 a variability analysis of CNFET digital circuits affected by CNT-specific variations is presented. In Chapter 7 an analysis about how metallic CNTs affect CNFET circuits is presented and a fault-tolerant architecture as a technique to improve their reliability is proposed. Finally, concluding remarks are presented in Chapter 8.

Chapter 2

Thesis Motivation and Objectives

Since the semiconductor industry went into the sub-100nm era and as it moves forward smaller and smaller devices, the use of conventional scaling (dimensional scaling) as a method to enhance the CMOS performance will not be enough. In other words, the dimensional scaling of CMOS is approaching a supposed fundamental limit and as we have seen in the previous Chapter novel high mobility materials and technologies are required to continue with the Moore's Law. One possible and promising alternative is the use of carbon nanotubes as a channel material in MOSFETs. But, as any new technology, it still has several manufacturing issues that must be solved before.

The objective of this thesis is to evaluate the carbon nanotube technology as a possible substitute of silicon devices, showing a realistic view of the main challenges that this technology faces nowadays. Based on the most recent novel experimental results and achievements in the field of CNT growth process and device/chip integration, the effect that the main CNFET manufacturing imperfections or related CNT-specific variations have on CNFET device characteristics and parameters and on CNFET-based circuits performance and reliability is analyzed.

In order to present in a more detailed way the specific aims of this thesis, we list in the following a set of fundamental questions that summarize the challenges of this work. Some of them can be answered by analyzing the state of the art of CNT technology, other questions are developed in different parts of this thesis.

- **Why carbon nanotube technology as a possible replacement of silicon technology?**

  In the previous chapter we presented the main characteristics, achievements and challenges of the most likely technologies that will be used in the next generations of transistors. We have chosen to investigate carbon nanotube technology because CNTs are a completely different material to silicon with a totally different structure (1D). Furthermore, they posses extraordinary electrical properties such as ballistic transport and excellent carrier mobility, excellent electrostatics, and good scalability. They are predicted to surpass the performance of MOSFETs. A sub-10nm CNFET, which outperforms its competing Si devices by more than four times in terms of normalized current density at low operating voltages of 0.5V was experimentally demonstrated two years ago [44].

- **Which is the current state of carbon nanotube technology? Which are the main sources of variability/failure?**

  As any technology that is in development, CNFET fabrication process still have some imperfections. We review the main CNFET manufacturing challenges of carbon nanotube technology (and related-CNT-specific variations) and the most novel approaches proposed to overcome them. We also analyze the relevance of each source of variation from the point of view of CNFET variability and reliability/yield (failure).

- **How can we characterize, model and simulate these CNFET manufacturing imperfections?**

  Based on the last CNT growth process experimental results and using the CNFET compact model of Stanford University (HSPICE model), we develop a realistic CNFET variability script and a CNFET device failure model to simulate and characterize carbon nanotube devices.

- **How do these CNFET manufacturing imperfections affect CNFET circuits? How can the variations caused by CNFET manufacturing imperfections be alleviated?**

  We analyze the impact of CNFET imperfections on a CNFET inverter (chain), and on a pair of cross-coupled CNFET inverters. We investigate the effect that CNT-specific variations have on different important circuit parameters such as the

noise margins, figure of merit of robustness, and delay, figure of merit of speed. Moreover, different design styles are implemented and studied as a mechanism to reduce the variability of CNFET circuits in the presence of CNT-specific variations.

We also discuss the effect that CNT-specific variations have on one of the most critical module of a computing system such as the SRAM memory. We analyze the variability of write delay and read delay of a CNFET 6T SRAM affected by CNT-specific variations and compare them with the delay variability of a MOSFET 6T SRAM cell affected by process variations.

- **How do these CNFET imperfections jeopardize the reliability of CNFET circuits? How can the reliability/yield of CNFET circuits be enhanced?**

  We investigate which is the main cause of CNFET circuit failure as well as which are the main techniques to deal with them. In this sense, we review the most recent methodologies proposed to deal with CNFET circuit failures and we propose the use of fault-tolerant architectures based on redundancy as a mechanism to improve the reliability of CNFET circuits.

Chapter 3

Carbon Nanotube Technology

As CMOS technology is approaching to its presumed physical limits, nanoelectronic technology communities are making huge efforts to develop new nanometer-sized information processing devices. Their research is focused on alternative high mobility materials and structures, and novel devices. Different devices are being investigated and developed as an extension and enhancement to conventional MOSFETs; these include, III-V and Ge devices, Tunnel FETs, Nanowire FETs and Carbon Nanotube FETs.

In this chapter, a detailed overview of carbon nanotube technology is presented. The concept and the main properties of carbon nanotubes are commented in Section 3.1. A review of carbon nanotube state-of-the-art transistors is provided in Section 3.2. The evolution and the last achievements in CNFETs, the types of CNFETs, the CNFET models for circuit simulation as well as the main challenges that they face nowadays are presented. A summary of the Chapter is presented in Section 3.3.

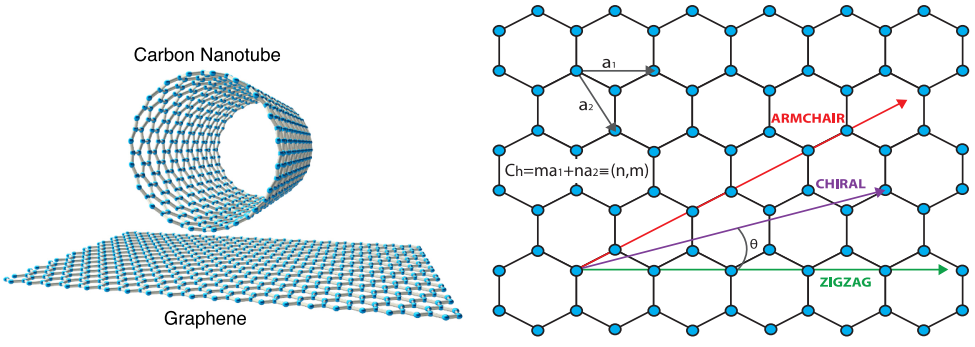
3.1 Carbon Nanotubes: Concept and Properties

Carbon Nanotubes (1D allotropes of carbon) are hollow cylinders composed by one (single-walled, SWNTs) or more (multi-walled, MWNTs) concentric layers of carbon atoms in a honeycomb lattice arrangement. Diameters of SWNTs and MWNTs are typically 0.8 to 2nm and 5 to 20nm, respectively, although MWNT diameters can exceed 100nm. CNT lengths range from less than 100nm to several centimeters, thereby bridging molecular and macroscopic scales.

A SWNT is a graphene sheet that has been rolled up into cylinder (Figure 3.1(a)). With diameters of the order of a few nanometers and up to some millimeters in length, CNT is essentially a nearly ideal one-dimensional object. CNTs are characterized by the chiral or roll-up vector that is the angle of the atom arrangement along the tube: $C_h = na_1 + ma_2 = (n, m)$, where m and n (wrapping indices) are integers and a_1 and a_2 are the unit vectors of the grapheme lattice as shown in Figure 3.1(b). The relationship between n and m defines three categories of CNTs: 1) armchair (n=m and chiral angle equal to 30°), 2) zigzag (n=0 or m=0 and chiral angle equal to 0°), and (iii) chiral ($n \neq m \neq 0$ and chiral angle between 0° and 30°). The chirality is also responsible for the diameter and the behavior of the CNT. The diameter of a CNT can be obtained as $D_{CNT} = (\sqrt{3}/a_0)\sqrt{(n^2 + m^2 + nm)}$, where $a_0 = 0.142nm$ is the nearest-neighbor carbon atom distance. Furthermore, a nanotube is metallic if $n = m$ or $n - m = 3i$ and it is semiconducting if $n - m \neq 3i$, where i is an integer.

Metallic CNTs, particularly MWNTs, have been suggested as an interconnect material because of their high thermal and mechanical stability, high thermal conductivity (as high as 5800 W/mK) and large current-carrying capacity (current densities as high as $10^{10} A/cm^2$)[49], [50]; whereas semiconducting CNTs, specially SWNTs, are considered to be a promising substitute for silicon in field-effect transistors. The advantages of s-CNTs over other conventional semiconductors are multifold:

1. Excellent carrier mobility: the carrier mobility of semiconducting nanotubes is experimentally measured to be $> 10,000\ cm^2V^{-1}s^{-1}$ at room temperature which is higher than the state-of-the-art silicon transistors (10-1500 $cm^2V^{-1}s^{-1}$) [51].



(a) (b)

FIGURE 3.1: (a) Schematic representation of the construction of a single-walled nanotube by rolling-up a graphene sheet. (b) The chiral angle and chirality (n,m) describe all the types of nanotubes.

2. Ballistic transport: the charge carriers in carbon nanotubes have long mean free paths, on the order of a few hundred nanometers for acoustic phonon scattering mechanism. As a result, scattering-free ballistic transport of carriers at low electric fields can be achieved in carbon nanotubes at moderate channel lengths (e.g., sub-100nm) [52].

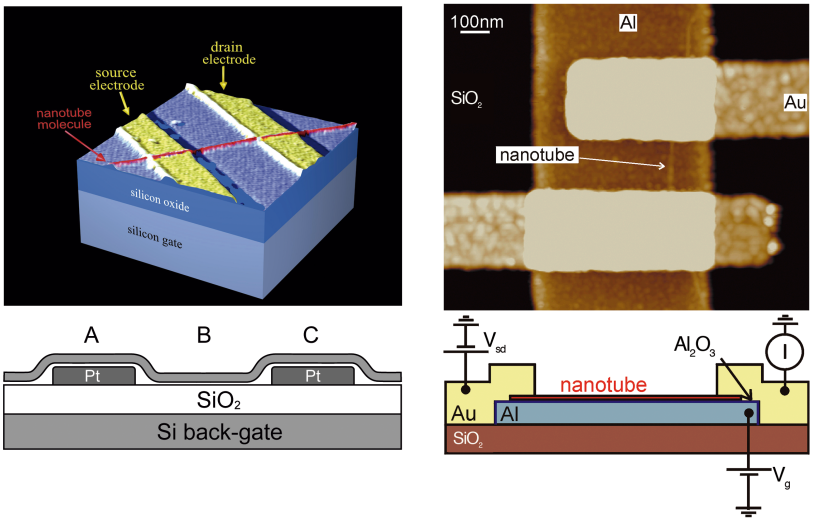
3. Small size: their small diameters enable excellent electrostatics with efficient gate control of the channel for highly miniaturized devices.

3.2 Carbon Nanotube Field-Effect Transistors (CNFETs)

3.2.1 Progress and Prospects of CNFETs

In a CNFET the role of the channel is played by one or more CNTs. The first carbon nanotube transistor was fabricated in 1998 [53]. In this CNFET, an individual semiconducting carbon nanotube bridged two platinum source and drain electrodes patterned on the silicon substrate which was thermally coated by a thick silicon dioxide layer (Figure 3.2(a)). Since this first demonstration of a CNFET tremendous progress has been made in improving the electrical characteristics of the transistor, as well as, its structure.

This first CNFET used a back-gate dielectric that consisted of a thick silicon dioxide layer (300nm). This back gate structure presented several disadvantages. First, the use of a conductive substrate as a back-gate electrode, usually with gate dielectric of a considerable thickness, makes that high voltages are required to switch the device ON. Second, all the devices are turned on simultaneously because the gate is shared by all the devices on the substrate. And third, the exposure of the CNT to air also inevitably results in a p-type characteristic [54]. This structure was improved by Bachthold et al. [55]. They replaced the silicon dioxide dielectric by a thin native Al_2O_3 layer on top of a patterned Al-gate and were able to low the gate voltage, to increase the transconductance and to allow the integration of multiple CNFETs in the same chip (Figure 3.2(b)). Furthermore, they succeeded to build different CNFET circuits that exhibited a range of digital logic operations, such as an inverter, a logic NOR, a static random-access memory cell, and a ring oscillator.



(a) (b)

FIGURE 3.2: (a) First CNFET [53]. It consist of one semiconducting SWNT connected to two metal electrodes. (b) CNFET based on a single CNT used to demonstrate logic circuits [55].

A further step was done by the introduction of a top gate device [56], [57]. Top gate CNFETs allow: 1) a reduction of the gate dielectric thickness, 2) a gate biasing at low voltage, 3) individual addressability of devices, 4) high speed switching and 5) high integration density. Additional progress was made by the creation of the first CMOS-like device. Derycke et al. [54] proposed the first CMOS-like device by producing n-type CNFETs by annealing in a vacuum and doping with potassium a section of a nanotube. They built the first CMOS-like inverter. Chen et al. [58] proposed a complete integrated logic circuit assembled with single CNTs. Since then, excellent single-channel (one CNT) and multi channel (networks or arrays of CNTs) CNFETs have been demonstrated and used for digital circuit implementation and integrated circuits as we mentioned in the previous chapter (Section 1.2.2.3) [44]-[48]. One of the last achievements is the experimental demonstration of the first CNT computer (Figure 3.3). The mini-computing system is composed of 178 CNT FETs, with each FET comprising about 10 to 200 nanotubes. Even though the fabrication is not optimized, they have achieved 1 kHz operating computing unit to execute simple million instructions per second (MIPS) instructions.

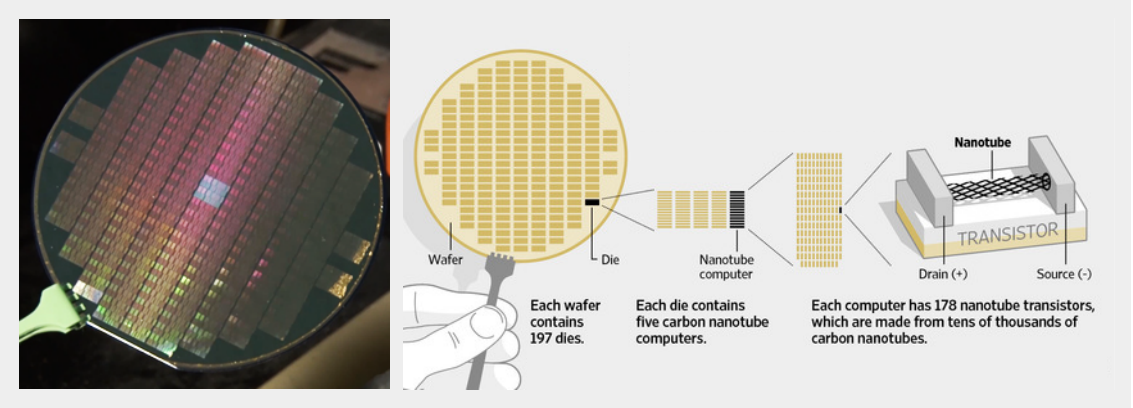


FIGURE 3.3: First CNT computer [48]. (Source: Stanford University)

3.2.2 Types of CNFETs

The two main types of CNFETs are: 1) Schottky-barrier (SB) CNFET and 2) doped-Source/Drain (S/D) CNFET or MOSFET-like CNFET.

SB-CNFETs (Figure 3.4(a)) are fabricated using direct contact of metal with the CNT and consequently Schottky barriers are formed at nanotube-metal junction. They work on the principle of direct tunneling through an Schottky barrier at the source-channel junction, that is, the barrier width is modulated by the application of gate voltage. It is worth noting that the presence of Schottky barriers severely limits the transconductance of the nanotube transistors in the ON state and reduces the current. Furthermore, SB-CNFETs exhibit strong ambipolar characteristics.

MOSFET-like CNFETs (Figure 3.4(b)) are composed of three regions. The region below the gate is intrinsic in nature and the two ungated regions are heavily n-type or p-type doped. They operate in a pure p- or n-type enhancement-mode or in a depletion-mode, based on the principle of barrier height modulation when applying a gate potential. This type of CNFETs are promising because: 1) they show unipolar characteristics unlike SB-CNFETs; 2) the absence of SB reduces the OFF leakage current; 3) they are more scalable compared to their SB counterparts; and 4) in ON-state, the source-to-channel junction has a significantly higher ON current.

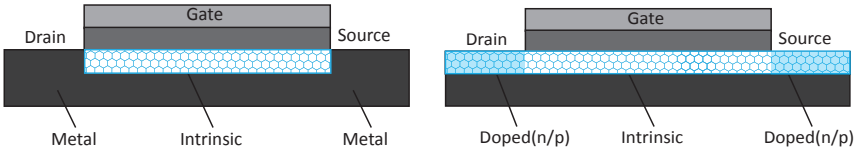


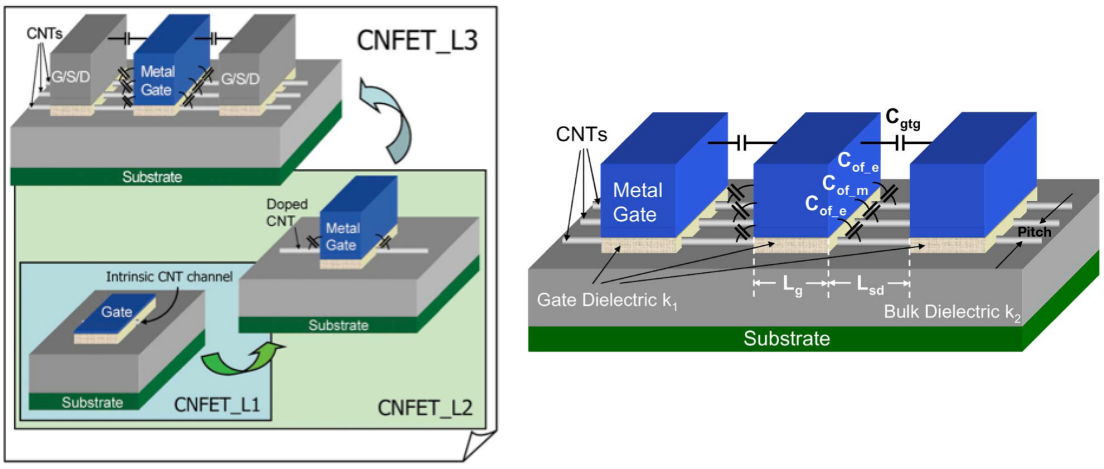
FIGURE 3.4: (a) Schottky-barrier (SB) CNFET. (b) Doped-Source/Drain (S/D) CNFET or MOSFET-like CNFET.

3.2.3 CNFET Compact Model for Circuit Simulation

The development of new technology requires tools at all levels of abstraction. Modeling tools for detailed calculations of the energy band diagrams and device current-voltage characteristics [59] are essential first steps for device physics understanding. At the same time, modeling tools at higher levels of abstraction are required for device design space exploration and circuit design. As an example, for Si CMOS technology, industry-standard tools such as PISCES [60] and SPICE [61] are essential for device design and circuit simulation, respectively. Higher level abstraction tools are used to describe and synthesize circuits at the system level.

Considerable effort has been put on modeling CNFETs [62]-[65]. There are generally two approaches in modeling CNFETs: 1) the more numerically intensive non-equilibrium Greens function (NEGF) approach and 2) a simpler modeling methodology based on ballistic transport assumption. In our work we focus on the compact HSPICE model for MOSFET-like CNFET device and circuit simulation developed by Stanford University [66]-[69] (a model based on ballistic transport assumption). Figure 3.5 shows the complete CNFET device model. It is implemented hierarchically in three levels. Device non-idealities are included hierarchically at each level. The first level denoted as CNFET-L1, models the intrinsic behavior of MOSFET-like CNFET. It is the core of the model and it is used to describe the portion of the SWNT under the metal gate, which forms the CNFET channel region. This level assumes near ballistic-transport, with acoustic and optical phonon scattering, and includes parasitic capacitances and resistance. The second level, denoted as CNFET-L2, builds upon Level 1 by including effects (e.g. parasitic capacitances and resistance) from the highly doped S/D carbon nanotube regions. It also includes SB resistances from the S/D contacts to the S/D CNT regions. The first two levels deal with only one CNT under the gate. The top level, denoted as CNFET-L3, models the interface between the CNFET device and the CNFET

circuits. This level deals with multiple CTNs per device and includes the parasitic gate capacitance and screening due to the adjacent CNTs.



(a) (b)

FIGURE 3.5: (a) Complete CNFET device model. (b)Three-dimensonal device structure of CNFET [68].

It should be noted that this model allows to simulate 1-tube CNFET as well as multi-tube (array of CNTs) CNFET but all the CNTs must be semiconducting and have the same diameter, doping level and spacing between them (pitch).

3.2.4 CNFET Manufacturing Challenges

For CNFET digital logic applications, multi-channel CNFETs are required because they provide higher current densities than single-tube CNFETs. In addition to the commonly known silicon CMOS process variations such as channel length, oxide thickness and threshold voltage variations, CNFETs are also subject to CNT-specific variations [70]-[71] (Figure 3.6). Whereas conventional process variations have a minor impact on CNFET performance due to its inherent device structure and geometric properties [72], CNT-specific variations can lead nor only significant circuit performance fluctuations, but also complete failure of CNFETs. In this thesis we focus on CNT-specific variations (Figure 3.6) that result from a still imperfect CNFET manufacturing process. The main CNFET manufacturing challenges are:

- The alignment and positioning of the CNTs during the CNT growth process: CNTs grown on quartz substrates can yield nearly perfectly linear ($> 99.9\%$) aligned arrays of CNTs [73], but remains a non-negligible fraction of mispositioned CNTs that can interfere with the logic functionality. Nevertheless, CNFET circuits immune to such mispositioned CNTs have been developed [74].

- CNT diameter variations: Chirality is responsible for the CNT diameter. Since the band-gap of CNTs is strongly dependent on diameter, accurate control of the diameter is essential to the performance of CNFETs. Diameter variations cause fluctuations in the CNFET's threshold voltage and drive current. Typical CNT growth techniques produce CNTs with diameters ranging from 0.5 to 3nm, but the standard deviation of the CNT diameter can often be controlled within 10% of the mean diameter [73].

- CNT density variations [75], [76]: These variations are due to the non-uniform spacing between CNTs (non-uniform pitch) during CNT growth, resulting in variations in the number of CNTs in the transistor (also called *CNT count*). Not only do they cause large variations in CNFET performance, but they also lead to a significant probability of complete failure in cases where there are no CNTs present in the CNFET (opens).

- Increased CNT density: The most common method for growing CNTs is chemical vapor deposition (CVD). CNT arrays are grown on a quartz wafer. They are then transferred onto a target substrate (e.g., a silicon wafer) for circuit fabrication. The average CNT density obtained today with this technique is in the range of 1-10 CNTs/μm. Multiple-growth or multiple-transfer techniques [77], [78] can increase the CNT density up to 45-55 CNTs/μm. However, that is still significantly lower than the CNT density required for logic circuits, i.e., 250 CNTs/μm. This notwithstanding, higher CNT densities (more than 500 CNTs/μm) can be obtained using other techniques, as will be discussed later.

- The presence of metallic CNTs among semiconducting CNTs: Metallic CNTs should not be used to make CNFETs because their high conductivity makes it impossible to control the current with the gate, thereby causing source-to-drain shorts in the CNFET. In a typical CNT synthesis process, 1/3 of CNTs are metallic

and 2/3 are semiconducting. In order to reduce the proportion of m-CNTs, different processing options can be used. One option is to grow predominantly s-CNTs. Enhanced CNT growth methods can be used to achieve a percentage of s-CNTs between 90% and 96% [79], [80]. Another alternative is to separate the m-CNTs from the s-CNTs after the CNT growth to obtain mostly s-CNTs. In this regard, a considerable reduction in the percentage of m-CNTs (to 1%-5% m-CNTs) has also been achieved with CNT self-sorting techniques [81]. However, this improvement in the percentage of m-CNTs is not enough for very-large-scale integration (VLSI) digital circuits. For high-performance logic applications, which would require billions of transistors, the impurity concentration of m-CNTs would need to be less than 0.0001%. A third processing option is thus to remove the m-CNTs after the CNT growth. Existing techniques for m-CNT removal include single-device electrical breakdown (SDB) [82], gas-phase and chemical-reaction-based removal techniques [83], and VLSI-compatible metallic-CNT removal (VMR) [84]. SDB removes $\sim 100\%$ of m-CNTs, but it is not VLSI-compatible. Gas-phase chemical-reaction-based removal techniques are highly compatible with VLSI semiconductor processing, but m-CNT removal depends on CNT diameters, and a narrow CNT diameter distribution is required. Finally, VMR is VLSI-compatible but can impose area penalties. Furthermore, non of all these m-CNT removal techniques is perfect; some m-CNTs still survive after m-CNT removal, while a non-negligible fraction (typically, 10%-40%) of the s-CNTs can accidentally be eliminated during the process. As a result, the number of CNTs in the transistor or *CNT count* decreases, thereby increasing the likelihood of failure (opens). A novel and promising approach for m-CNT removal called thermocapillary-resist was recently presented in [85]. This technique has been used to achieve the highly selective of m-CNTs from the full length of an aligned array of CNTs on a chip without damaging the s-CNTs. However, it must be improved before it can be used with very high CNT densities. On the other hand, a technique called ACCNT have been proposed as a solution to m-CNTs problem in CNFET circuits [86]-[87]. It uses asymmetrically CNTs to achieve metallic-nanotube tolerance, but it still needs to be improved.

It should de noted that all of the above CNT imperfections are typical of the CVD method. Another approach is to use solution-processed CNTs [88]. With this method, the CNTs are first suspended in solution, and then separated, assembled, and deposited

onto substrates for device fabrication. This process offers unique processing advantages over the CVD method, including the capabilities of separating nanotubes by electronic type (with s-CNT purity of over 99%) and depositing them onto various substrates in the form of ultradensely aligned arrays at low temperature, and the preparation of tube densities of more than 500 CNTs/μm using methods such as the Langmuir–Schaefer technique [89]. However, long-channel CNFETs that use solution-processed CNTs generally show inferior device performance due to the presence of a higher number of structural defects induced during nanotube suspension and purification processes such as misaligment defects.

Additional CNFET manufacturing challenges include:

- Controlling the CNT doping process: Digital circuits require n-type and p-type CNFETs. High-performance p-type CNFETs have been developed using high-work-function metal contacts, but the development of n-type CNFETs that are stable in ambient air remains a challenge. However, recent studies have demonstrated functional n-type CNFETs using low-work-function metal contacts [90] and ALD-based electrostatic doping [91].
- Achieving low metal-to-CNT contact resistance: The lowest theoretically achievable contact resistance is 6.5$k\Omega$, the quantum limit. However, this resistance is hard to achieve because of the poor wetting properties of metal to CNTs and the presence of Schottky barriers between the CNT and the metal due to band misalignment. Solutions include the use of graphitic carbon interfacial layers to increase the contact area between the metal and the CNT [92] and the selection of a proper work-function metal contact [93] to reduce the SB.

In this thesis we present a research about the impact of CNT-specific variations on CNFET devices and circuits from the point of view of variability and reliability (failure).

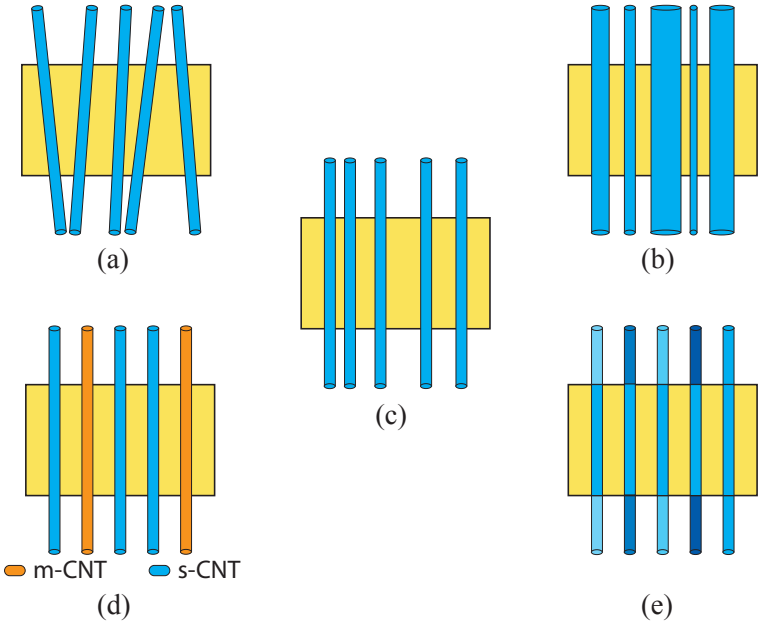


FIGURE 3.6: CNT-specific variations. (a) CNT alignment variations. (b) CNT diameter variations. (c) CNT density variations. (d) CNT type variations. (e) CNT S/D doping variations.

3.3 Summary

In this Chapter a complete overview of carbon nanotube technology was presented.

The main electronic properties of semiconducting CNTs that make them a promising substitute for silicon are reviewed. They include: 1) excellent carrier mobility, 2) ballistic transport and, 3) very small size.

The evolution of CNFETs and the last achievements in CNT technology are presented. Excellent multi-channel CNFETs have already been shown and used for digital circuit implementation and integrated circuits, as well as, the first CNT computer has been experimentally demonstrated.

The main and most used CNFET model for device and circuit simulation is introduced. It is a MOSFET-like CNFET compact model developed by Stanford University. It allows to simulate 1-tube CNFET as well as multi-tube (array of CNTs) CNFET but all the CNTs must be semiconducting and have the same diameter, doping level and spacing between them (pitch).

Finally, the main CNFET manufacturing imperfections/challenges that results in CNT-specific variations are reviewed. These include: 1) CNT alignment and positioning, 2) CNT diameter variations, 3) CNT density variations, 4) the need of an increased CNT density, 5) presence of metallic CNTs, 6) CNT doping variations and, 7) low metal-to-CNT contact resistance.

Chapter 4

Variability in CNFET Devices

Carbon Nanotube devices could be potential substitutes for MOSFETs. Experimentally, it has been shown that carbon nanotube field-effect transistors with sub-10nm channel length can provide the highest drive current density compared to other technologies such as Si nanowire and ETSOI [44]. CNFETs have also been shown to operate at a low supply voltage of 0.4V [46]. But, as any technology that is still in progress of manufacturing maturity, the CNFET manufacturing process has significant challenges that must be solved. Multi-channel CNFETs are subject to imperfections-related to CNT synthesis process and CNT device integration that results in CNT alignment, CNT diameter, CNT density, CNT type (m- or s-CNT), and CNT doping variations (CNT-specific variations). These variations may strongly affect not only the CNFET performance, but also can be cause of CNFET failure jeopardizing its applicability.

In this chapter an analysis of the impact of the main CNT-specific variations on CNFET characteristics presented. The organization of the chapter is as follows. In Section 4.1 the CNFET nominal device used in this research and its main parameters (nominal values) are shown. In Section 4.2 the relevance of each source of variability on drive current and ON-OFF current ratio of a multi-channel CNFET is evaluated. A methodology for analyzing the effect that CNFET manufacturing imperfections have on CNFET performance (based on Monte Carlo simulations) and the simulation results are presented in Section 4.3. In Section 4.4 a CNFET variability analysis is presented; the impact of CNT-specific variations on key transistor parameters is evaluated. Conclusions and a summary of the Chapter are presented in Section 4.5.

4.1 Nominal CNFET Device

As we mentioned in Chapter 3, Section 3.2.3, in our work we use the CNFET compact model developed by Stanford University because it is the most appropriate model for device and circuit simulation and it can be easily included in an electronic simulation tool such as HSPICE [66]-[69]. It is a MOSFET-like CNFET that uses a top-gate structure (Figure 4.1). It consists of N perfectly aligned and positioned semiconducting CNTs whose section under the gate is intrinsic and whose source/drain extension regions are n- or p-doped (p-type or n-type transistors). We will consider as nominal (without variability) a CNFET that is composed by 8 s-CNTs with a diameter of ∼1.5 nm (chirality (19,0)) and an inter-CNT spacing or pitch of 4nm which translates to a density of 250 CNTs/μm. It is worth noting that the CNT-to-CNT charge screening effect is taken into account in our nominal device; it is negligible for pitch $> 20nm$. This effect strongly affects the gate capacitance and the drive current of the transistor and then the CNFET performance [66], [67]. The length of the gate, source, and drain (L_{ch}, L_{ss}, L_{dd}) is 16 nm and the oxide thickness (T_{ox}) is 4nm. We assumed ohmic metal contacts (as with high CNT doping of $\sim 0.8\%$ and similar metal and CNT work functions, Φ_C=Φ_M=4.5 eV, the SB resistance could be suppressed to a low value of $< 1K\Omega$). These and other parameters are shown in Table 4.1.

Figure 4.2 shows the output and transfer characteristics of a n-type CNFET obtained using the CNFET HSPICE simulation model. The key nominal transistor parameters are: $I_{ON} = 66.18\mu A$, $I_{ON}/I_{OFF} = 1\times10^6$ and $V_{TH} = 0.29V$. The ON current (I_{ON}) and the ON-OFF current ratio (I_{ON}/I_{OFF}) were extracted from I-V characteristics. I_{ON} is the current when $V_{DS} = V_{GS} = 0.9V$, and I_{OFF} is the current when $V_{DS} = 0.9V$ and $V_{GS} = 0V$. The threshold voltage (V_{TH}) was obtained using the well-known expression [69]

$$V_{TH} = \frac{E_g}{2q} = \frac{\sqrt{3}}{3}\frac{aV_\pi}{eD_{CNT}} \tag{4.1}$$

where $a = 2.49\mathring{A}$ is the carbon-to-carbon-atom distance, $V_\pi = 3.033eV$ is the carbon $\pi - \pi$ bond energy in the tight bonding model, e is the unit electron charge, and D_{CNT} is the CNT diameter.

Note that this equation calculates the threshold voltage of the intrinsic channel (portion of the CNT under the gate) and then it only depends on CNT diameter; it does not take into account other CNFET geometrical parameters and effects such as electrostatic doping that also may affect the V_{TH}.

It should be pointed out that the Stanford CNFET model does not include variability aspects. In other words, it can only be used to simulate transistors with one or more semiconducting tubes with the same diameter, doping and homogeneous inter-CNT spacing.

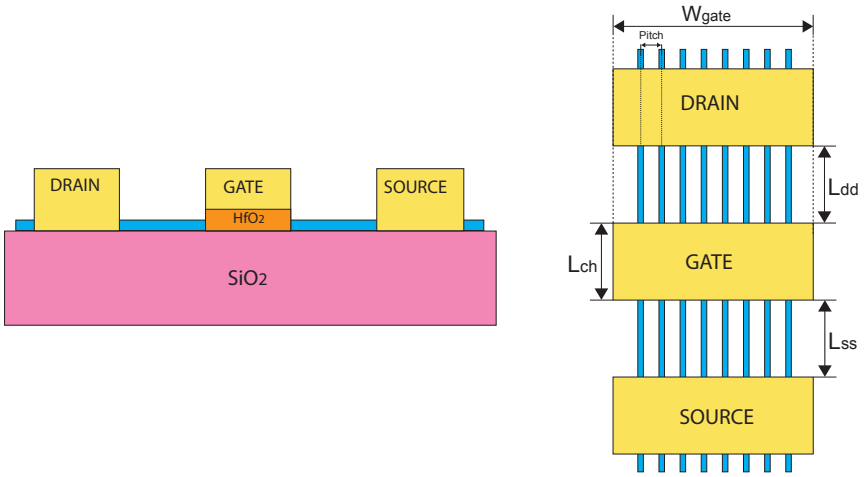
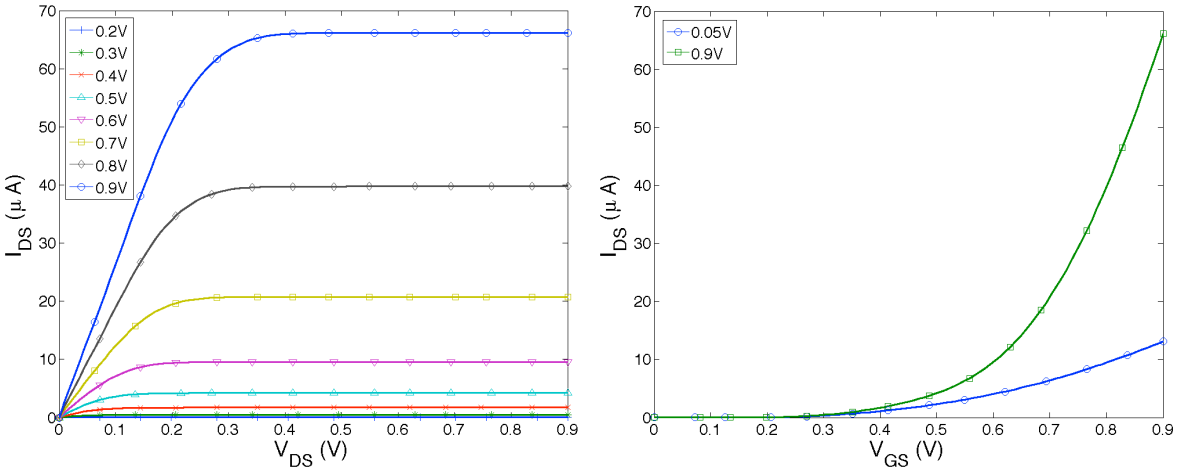


FIGURE 4.1: CNFET structure showing a front-view (left) and a top-view (right) sections.

TABLE 4.1: Structural and electrical parameters for n-type CNFET

Parameters	**Value**
Number of CNTs	8
Chirality (n,m)	(19,0), s-CNT, diameter $\sim 1.5nm$
Inter-CNT spacing (Pitch)	4 nm
CNT doping level	1% ($\sim 0.66eV$)
Oxide thickness (T_{ox})	4 nm
Dielectric constant of high-K gate oxide material (K_{ox})	12 (HfO_2)
Dielectric constant of substrate material (K_{sub})	4 (SiO_2)
Gate/Source/Drain length (L_{ch}, L_{ss}, L_{dd})	16 nm
Gate width (W_{gate})	32 nm



(a) (b)

FIGURE 4.2: (a)Output characteristic of a 8-tube n-type CNFET. (b) Transfer characteristic of a 8-tube n-type CNFET.

4.2 Relevance of CNFET Variations

In this section we evaluate the contribution of each CNT-specific variation to multi-channel CNFET parameters variability.

Previous publications have analyzed the impact of some of these CNT-specific variations at device level. Some of them analyze CNFETs that contain a single CNT. In [72], the impact of process/conventional variations such as channel length and oxide thickness and CNT-specific variations (specially CNT diameter variations) are compared. They conclude that CNFETs are less sensitive to conventional variations than to CNT-specific variations because good electrostatic control and near-ballistic transport in CNFETs can significantly minimize the impact of such conventional variation sources. It is also suggested that single-tube CNFETs are strongly affected by diameter variations because CNT diameter directly modulates the band gap of a CNT, and therefore modifies the threshold voltage of transistor (see Equation 4.1). For example, if a CNT diameter variation of $\sigma/\mu = 10\%$ is considered, then the CNFET ON current (I_{ON}) is predicted to vary $\sigma/\mu \approx 15\%$ [72].

But, as we mentioned in Section 3.2.4, for logic circuit applications multi-channel CNFETs are required. They provide higher current than single-channel CNFETs and in addition they are useful for reducing the impact of variations due to statistical averaging effects. Previous publications have shown that statistical averaging can significantly

alleviate the impact of CNT diameter variations and alignment variations [94]-[95]. For example, if CNT diameter variation has $\sigma/\mu = 10\%$ and a CNFET contains 100 CNTs, then the CNFET I_{ON} only has σ/μ of less than 2%.

Most of these works assume a specific and known number of CNTs per CNFET, and focus on discussing the impact of CNT diameter, doping and alignment fluctuations. Zhang in his work also studied the impact of *CNT count variations* [96]. *CNT count* is defined as the number of CNTs that completely bridge the source and the drain of the transistor. Then, CNT count variations are those that affect the number of CNTs in the transistor and can be caused by both: 1) grown CNT density variations, and 2) m-CNT-induced count variations that are due to the presence of m-CNTs and the subsequently application of a m-CNT removal process.

Using the nominal CNFET device showed in the previous Section, we examine the individual contribution of CNT-specific variations as well as conventional-related variations (oxide thickness, T_{ox}, and channel length, L_{ch}) to I_{ON} and I_{ON}/I_{OFF} variations. As we mentioned, Stanford CNFET model is a uniform and homogeneous model. That is, only allows the simulation of multi-channel CNFETs in which all CNTs are semiconducting and perfectly aligned, have the same diameter, same pitch and identical S/D doping level. We have gone one step further, and managed to simulate heterogeneous CNFETs with statistical variability. For this purpose, we treat each CNT component as an individual transistor, so a transistor composed by n CNTs can be split into n parallel 1-tube CNFET that will have different characteristics (Figure 4.3). In other words, the current delivered by an n-tube CNFET is calculated as the sum of the currents of n 1-tube CNFETs. We use this approach to analyze the individual impact of the sources of variation as well as in our complete variability analysis (Section 4.3).

Figures 4.4 and 4.5 compare the CNFET I_{ON} and I_{ON}/I_{OFF} variations caused by CNT doping, alignment (channel length), diameter and oxide thickness, density (pitch) and m-CNT induced count variations, respectively. The probability distributions used in the simulations are listed in Table 4.2. Note that alignment variations are treated as channel length variations (possible crossing are not considered) and oxide thickness variations that are caused by diameter variations are taken into account. In this analysis, m-CNT induced count variations are those due to the application of an ideal m-CNT removal process, in which all m-CNTs are removed whereas all s-CNTs keep intact. Furthermore,

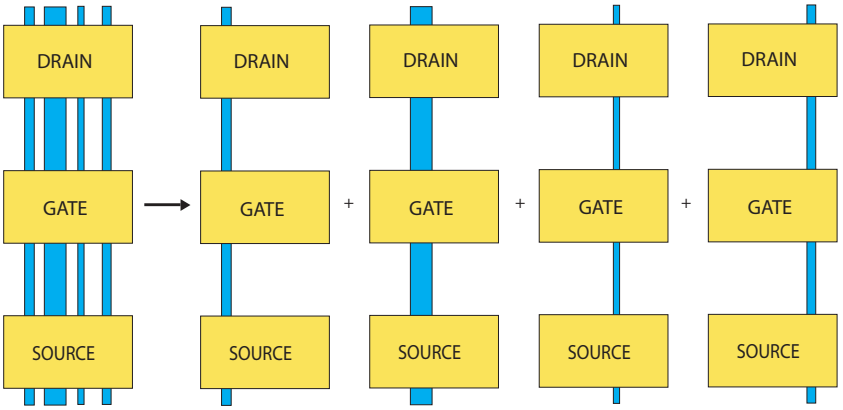


FIGURE 4.3: A 4-tubes CNFET whose CNTs have different diameters can be split into 4 parallel 1-tube CNFET for device simulation.

these variations have been analyzed for different m-CNT probabilities (p_m): $p_m = 33\%$ (typical CNT growth methods), $p_m = 10\%$, $p_m = 5\%$ and, $p_m = 1\%$ (enhanced CNT synthesis methods and self-sorting techniques). So, the greater the p_m, the higher the m-CNT induced count variation will be. As shown in Figures 4.4 and 4.5, CNT count variations caused by CNT density and m-CNT induced count variations when $p_m = 33\%$ are the main sources of I_{ON} and I_{ON}/I_{OFF} variability. Note that m-CNT induced count variations can be significantly increase if a non-ideal m-CNT removal process is considered, all m-CNT are removed but also some s-CNTs are accidentally eliminated. Diameter, alignment and, doping have a minor impact because of statistical averaging.

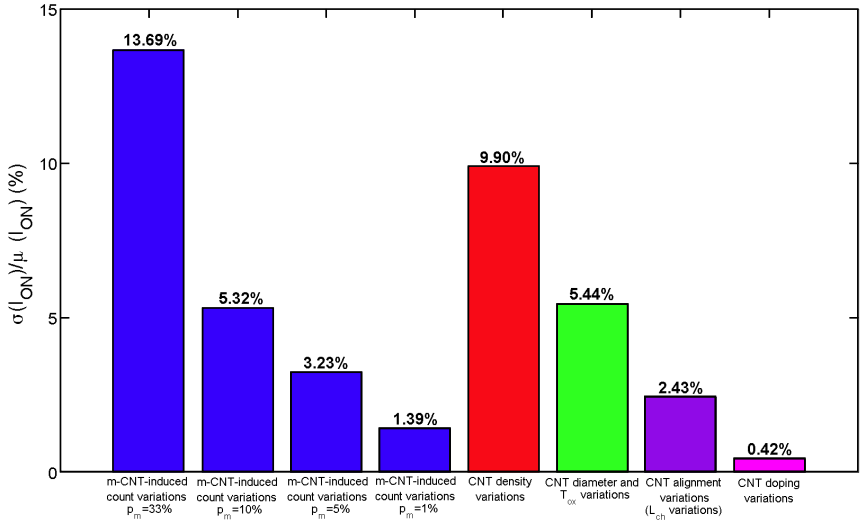


FIGURE 4.4: Individual contribution of CNT-specific variations as well as conventional-related variations to I_{ON} variations.

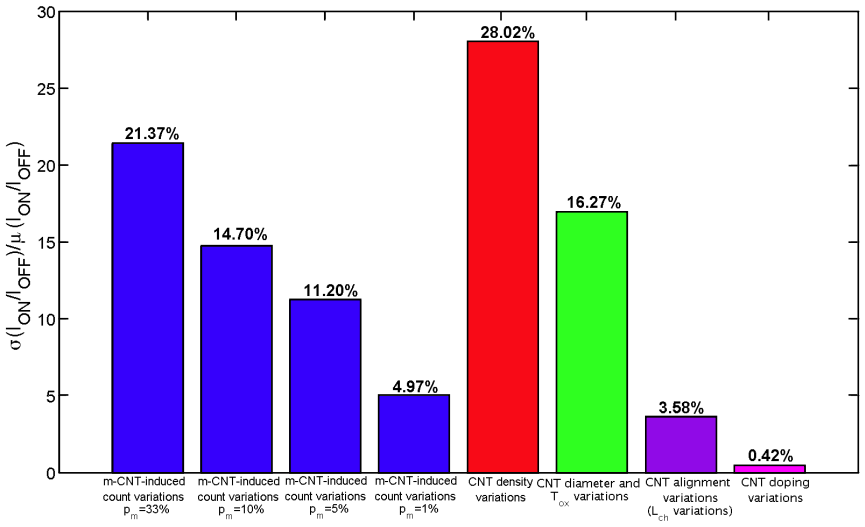


FIGURE 4.5: Individual contribution of CNT-specific variations as well as conventional-related variations to I_{ON}/I_{OFF} variations.

TABLE 4.2: Probability distributions of CNT-specific variations used in Figures 4.4 and 4.5 and references

CNT-specific variations	**Distribution**	**Ref.**
S/D doping variations	Normal: $\mu_{dop} = 1\%$, $\sigma_{dop} = 0.1\%$	[95]
CNT alignment variations	Normal: $\mu_{align} = 0$ degree, $\sigma_{align} = 10\%$ degrees (only 5% of CNTs are misaligned)	[71] [73]
CNT diameter variations	Normal: $\mu_{dia} = 1.5nm$, $\sigma_{dia} = 0.1nm$	[73]
CNT density (Pitch) variations	Chi^2: $\mu_{pitch} = 4nm$, $\sigma_{pitch} = 2.83nm$	[75]

4.3 Procedure for Analyzing CNFET Manufacturing Variability

4.3.1 Monte Carlo Variability Evaluation Tool

Monte Carlo (MC) analysis is frequently used for calculating device variability [97]. The CNFET compact model of Stanford University does not allow to simulate variability in multi-channel CNFETs as we used to make in MOSFET models. So, a procedure using MC, HSPICE and Matlab was developed in order to automate the variability analysis process in CNFETs. It was used to analyze the variability of transistor characteristics and parameters due to the following CNFET manufacturing imperfections: 1) variations in CNT diameter and oxide thickness; 2) variations in CNT count due to CNT density and m-CNT-induced variations; 3) variations in the percentage of m-CNTs present in the

transistor; 4) variations in CNT doping; and 5) variations in CNT alignment (channel length variations).

In addition, this CNFET variability estimation methodology is suitable for different m-CNT removal scenarios: 1) no m-CNT removal; 2) non-ideal m-CNT removal processes in which some s-CNTs are removed and all or nearly all m-CNTs are removed; and 3) ideal m- CNT removal techniques that remove all m-CNTs but leave all s-CNTs intact.

The variability procedure works as follows (Figure 4.6). In the CNFET sample extraction stage, the initial number of CNTs (N) in the transistor is obtained for given gate width (W_{gate}) and pitch distribution ($pitch$). The proportion of m-CNTs and s-CNTs is then established using a given probability that a CNT is metallic (p_m) and for given diameter (dia), alignment ($align$) and doping (dop) distributions (Table 4.2). In step 3, the final number of CNTs is determined (n) for a given a probability of an m-CNT (p_{mR}) or s-CNT (p_{sR}) being removed. The pitch of the remaining CNTs is then recalculated. Hence, the result of the CNFET sample extraction stage is a sample of n-tube CNFET, with a mixture of m-CNTs and s-CNTs with different diameters, different S/D doping levels, different orientation (different channel length), and different inter-CNT spacing.

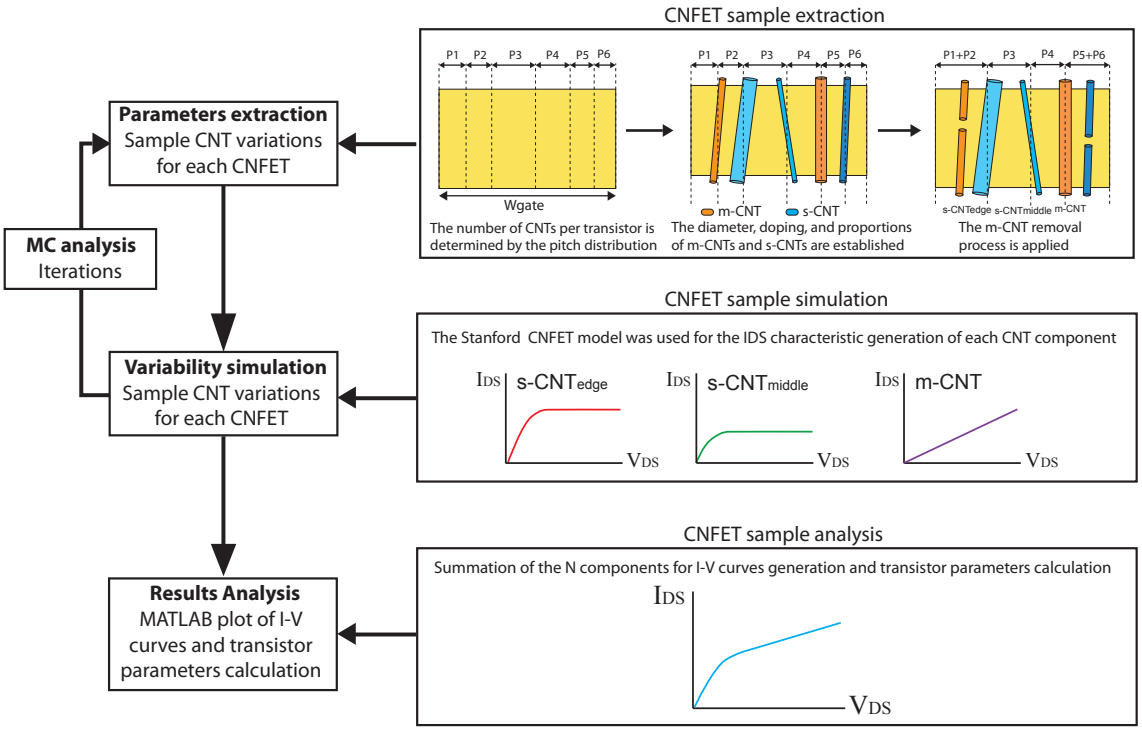


FIGURE 4.6: MC flow for CNFET device variability/reliability.

In the CNFET sample simulation phase, the I-V characteristics of the n-tube CNFET sample were obtained. This was done through the summation of the n I_{DS} current components (each CNT forming the CNFET) obtained with the Stanford CNFET model, taking into account the charge screening effects and the tube's position in the transistor (edge or middle). Note that for CNFET with multiple parallel CNTs and an inter-CNT pitch smaller than 20nm, the CNT-to-CNT screening affects both the gate-to-channel electrostatic capacitance and the drive current. The current delivered by each m-CNT was calculated based on equations presented in [67] and [68].

4.3.2 Simulation Results: Variability of Current Characteristics

Using the procedure described in the previous Section and the distributions shown in Table 4.2, we performed 1000 MC simulations for a multi-channel CNFET and we considered the following three cases of m-CNT removal:

1. No m-CNT removal ($p_{mR} = p_{sR} = 0\%$).
2. Non-ideal m-CNT removal technique: all m-CNTs and some s-CNTs are removed ($p_{mR} = 100\%$ and $p_{sR} = 10\% - 40\%$) or just a small portion of the m-CNTs survives ($p_{mR} = 99.99\%$ and $p_{sR} = 10\% - 40\%$).
3. Ideal m-CNT removal technique ($p_{mR} = 100\%$ and $p_{sR} = 0\%$).

Moreover, for each m-CNT removal scenario, we considered four different m-CNT probabilities: $p_m = 33\%$ (typical CNT growth methods) and $p_m = 10\%$, $p_m = 5\%$, and $p_m = 1\%$ (enhanced CNT synthesis methods and self-sorting techniques).

The current characteristics ($I_{DS} - V_{DS}$ and $I_{DS} - V_{GS}$) of a n-type CNFET for all three m-CNT elimination scenarios and for the worst case of m-CNT probability ($p_m = 33\%$) are shown in Figure 4.7 (the variability analysis for a p-type CNFET is equivalent). The results of these simulations will be analyzed in the following Section, from the point of view of device variability, and in Chapter 5, Section 5.3, from the point of view of device reliability.

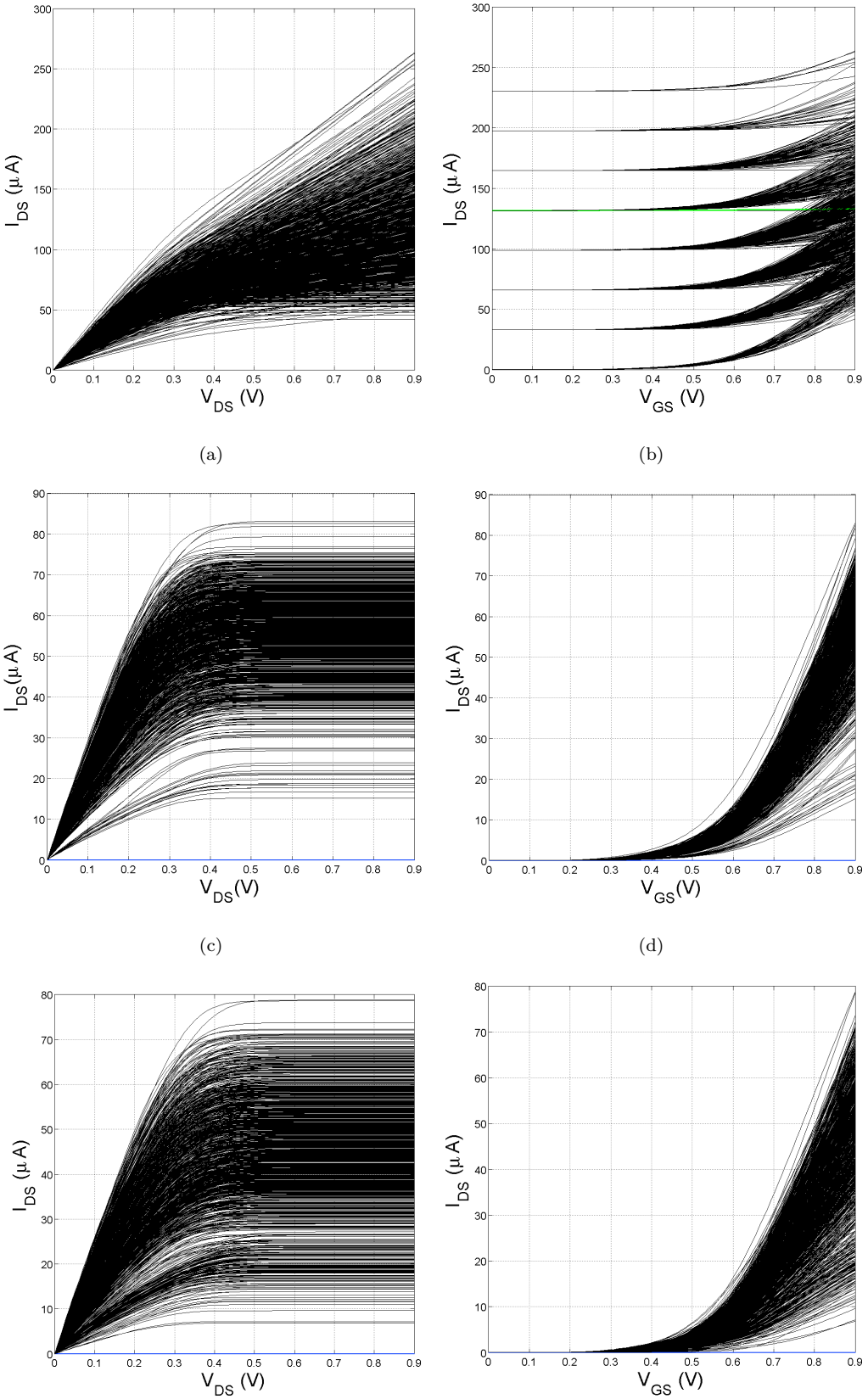


FIGURE 4.7: I-V CNFET characteristics for an n-type CNFET and $p_m = 33\%$ when no m-CNT removal technique is used ((a) and (b)) and when ideal ($p_{mR} = 100\%$ and $p_{sR} = 0\%$) and non-ideal m-CNT ($p_{mR} = 100\%$ and $p_{sR} = 40\%$) removal technique is considered ((c) and (d) and (e) and (f), respectively). The curves for the 1000 simulated devices (black curves) are shown. The green line and blue line is shorts and opens, respectively.

4.4 Variability Analysis: Impact on CNFET Key Parameters

Based on the $I_{DS} - V_{GS}$ current distributions obtained with the CNFET manufacturing variability methodology presented in Section 4.3.2, and taking into account only the functional transistors when an ideal m-CNT removal technique is applied (i.e., ignoring opens), we calculated the mean (μ) and standard deviation (STD, σ) for several key transistor parameters: I_{ON}, I_{ON}/I_{OFF} and V_{TH} (Table 4.3).

With regard to the behavior of μ and σ vs. p_m, it can be seen that in the case of I_{ON}, the mean increases slightly as p_m decreases, whereas the standard deviation decreases. For I_{ON}/I_{OFF}, both the mean and the STD decrease slightly as p_m decreases. Finally, V_{TH} remains constant for all four p_m as in this analysis we considered it to be affected only by diameter variations. However, in terms of variability, the I_{ON} and I_{ON}/I_{OFF} parameters are highly affected by CNT-specific variations, yielding variability values ($3\sigma/\mu$) between 57.20% and 134.70% ($p_m = 33\%$) and 33.97% and 97.49% ($p_m = 1\%$), respectively. Threshold voltage shows a more moderate fluctuation of about 11%. Note that, as we mentioned in Section 4.1, this is the threshold voltage fluctuation of the intrinsic channel (portion of the CNT that is under the gate) and it is only affected by diameter variations.

TABLE 4.3: Mean and STD when ideal m-CNT removal technique is applied (only functional transistors)

	$p_m = 33\%$		$p_m = 10\%$		$p_m = 5\%$		$p_m = 1\%$	
	μ	σ	μ	σ	μ	σ	μ	σ
I_{ON} (μA)	55.49	10.58	60.02	7.92	61.18	7.61	61.74	6.99
I_{ON}/I_{OFF} ($\times 10^5$)	12.65	5.68	9.64	3.58	9.35	3.41	8.77	2.85
V_{TH} (V)	0.27	0.01	0.27	0.01	0.27	0.01	0.27	0.01

It should be pointed out that in the case considered (ideal m-CNT removal method, $p_{mR} = 100\%$), it is possible to achieve a very high I_{ON}/I_{OFF} in the order of 10^5-10^6. However, the presence of m-CNTs severely degrades it. As shown in [98], the I_{ON}/I_{OFF} ratio of a CNFET composed of a mixture of s-CNTs and m-CNTs can be calculated as:

$$\frac{I_{ON}}{I_{OFF}} = \frac{N_s I_{s,on} + N_m I_m}{N_s I_{s,off} + N_m I_m} \tag{4.2}$$

where N_s and N_m are the number of s-CNTs and m-CNTs, respectively; $I_{s,on}$ and $I_{s,off}$ are the ON and OFF currents of an s-CNT as defined in Section 4.1 above; and I_m is the current delivered by an m-CNT when $V_{DS} = 0.9V$, and it is the same for both the ON and OFF states.

When the CNFET circuit level is considered (for multiple transistors), the most adequate parameter is the ratio of the mean values of I_{ON} and I_{OFF}:

$$\frac{\mu(I_{ON})}{\mu(I_{OFF})} = \frac{\mu(N_s)\mu(I_{s,on}) + \mu(N_m)\mu(I_m)}{\mu(N_s)\mu(I_{s,off}) + \mu(N_m)\mu(I_m)} \tag{4.3}$$

where

$$\frac{\mu(N_s)}{\mu(N_m)} = \frac{p_s(1-p_{sR})}{p_m(1-p_{mR})} \tag{4.4}$$

when an m-CNT removal process is applied.

Using these equations and the mean of the ON and OFF currents obtained through the 1000 MC simulations, Fig. 4.8 illustrates how the presence of m-CNTs in the transistors affects the average I_{ON}/I_{OFF} ratio for the four p_m probabilities assumed and for different p_{sR}. It should be observed that the average ratio improves as p_m and p_{sR} decrease and p_{mR} increases as expected. It should likewise be noted that this ratio remains almost constant once p_{mR} approaches 100%. Moreover, it is in the range of $10^5 - 10^6$ (inset in Fig. 4.8) and fluctuates slightly as the p_m changes, as seen in Table 4.3.

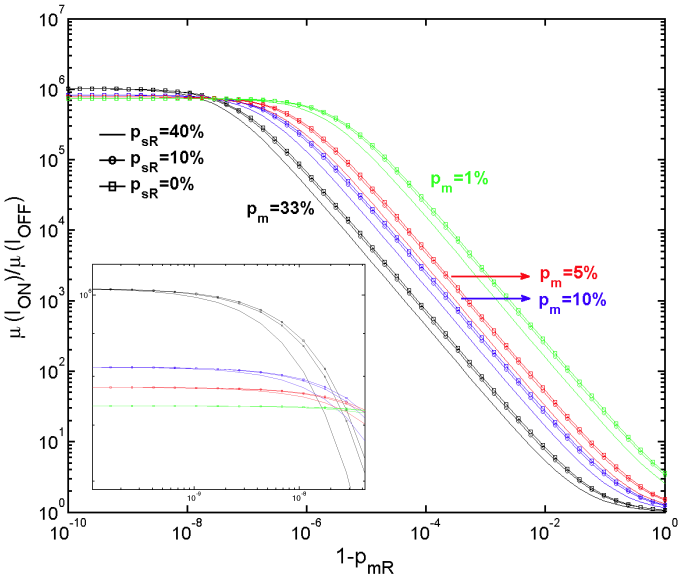


FIGURE 4.8: Average I_{ON}/I_{OFF} ratio vs. probability of m-CNT survival. (Inset) Zoom when $1 - p_{mR}$ is between 10^{-7} and 10^{-10}.

4.5 Summary and Conclusions

Multi-channel CNFETs are subject to CNFET manufacturing imperfections that result in CNT-specific variations that affect their parameters/characteristics and then their performance. These CNT-specific variations include: 1) CNT alignment variations, 2) CNT doping variations, 3) CNT diameter variations, 4) CNT density variations due to a non-uniform inter-CNT spacing, and 5) CNT type variations that result in a mixture of m-CNTs and s-CNTs leading to a possible decrease in the CNT count when a m-CNT removal process is applied (m-CNT induced variations).

In this chapter a detailed variability analysis of CNFET devices in the presence of CNT-specific variations was presented. Important results, conclusions and contributions are summarized in the following.

In the first part of the Chapter, the contribution of each source of variation to ON current (I_{ON}) and current ratio (I_{ON}/I_{OFF}) variations of a multi-channel CNFET is analyzed. For this purpose, we are able to simulate heterogenous CNFETs with statistical variability using an uniform an homogeneous model such as the CNFET compact model of Stanford University. Furthermore, in our MC simulations not only CNT-specific variations are considered but also CNT-related conventional variations such as oxide thickness and channel length fluctuations. Regarding the results, we demonstrate that CNT count variations that are due to CNT density variations and m-CNT induced count variations contribute most significantly to the overall I_{ON} and I_{ON}/I_{OFF} variations.

In the second part, a methodology for multi-channel CNFET variability estimation is presented for the first time. Based on MC, HSPICE and Matlab scripts, this variability procedure is used to obtain the fluctuation of transistor characteristics (curves I-V) in the presence of CNFET manufacturing imperfections (CNT-specific variations all together) and under the consideration of different m-CNT removal scenarios. We analyze the fluctuation of key transistor parameters (I_{ON}, I_{ON}/I_{OFF}, and V_{TH}) when an ideal m-CNT removal process is considered. We show that I_{ON} and I_{ON}/I_{OFF} parameters are highly affected by CNT-specific variations, yielding variability values of 57.20% and 134.70% for the worst p_m case (33%), respectively, whereas the V_{TH} of the intrinsic channel presents a more moderate fluctuation of about 11%. Finally, is is worth noting that if all m-CNTs are removed, it is possible to achieve a very high I_{ON}/I_{OFF} in the

order of $10^5 - 10^6$. However the presence of m-CNTs severely degrades it; if a very small percentage of m-CNTs survives, just a 0.01% (1-p_{mR}=10^{-4}), the I_{ON}/I_{OFF} is reduced by up to 3 orders on magnitude, from 10^6 to 10^3.

To conclude, CNFET manufacturing imperfections can result in significant CNFET parameter variations and then in CNFET circuit performance variations. Therefore, analyzing the impact of them at device level as well as at circuit level is very important: 1) to understand the current state of carbon nanotube technology, 2) to evaluate its viability as possible technology for sub-10nm transistors and 3) to see how to enhance CNFET circuits performance.

Chapter 5

Reliability of CNFET Devices

CNT-specific variations not only affect the CNFET parameters (transistor variability) as we have demonstrated in the previous Chapter, but also can be cause of CNFET failure. The catastrophic failures in CNFET devices and circuits are due to the presence of open and short defects. An open defect may occur when there is no CNT bridging the source and the drain of the transistor. It can be caused by both CNT density variations and m-CNT-induced count variations because of the application of an m-CNT removal process (CNT count variations) [96]. Whereas, a short defect may occur when there are one or more metallic CNTs in the transistor.

In this chapter an analysis of the impact of CNT count variations and the presence of m-CNTs on CNFET device (from the point of view of reliability/yield) is presented. The organization of the chapter is as follows. In Section 5.1 the causes of failure in CNFETs and the main works related to the functional yield of CNFETs are reviewed. In Section 5.2 our CNFET failure model is derived and applied to different m-CNT removal scenarios and m-CNT probabilities. In Section 5.3 a CNFET reliability analysis based on MC simulations is discussed. Finally, in Section 5.4, our results are summarized and concluding remarks are made.

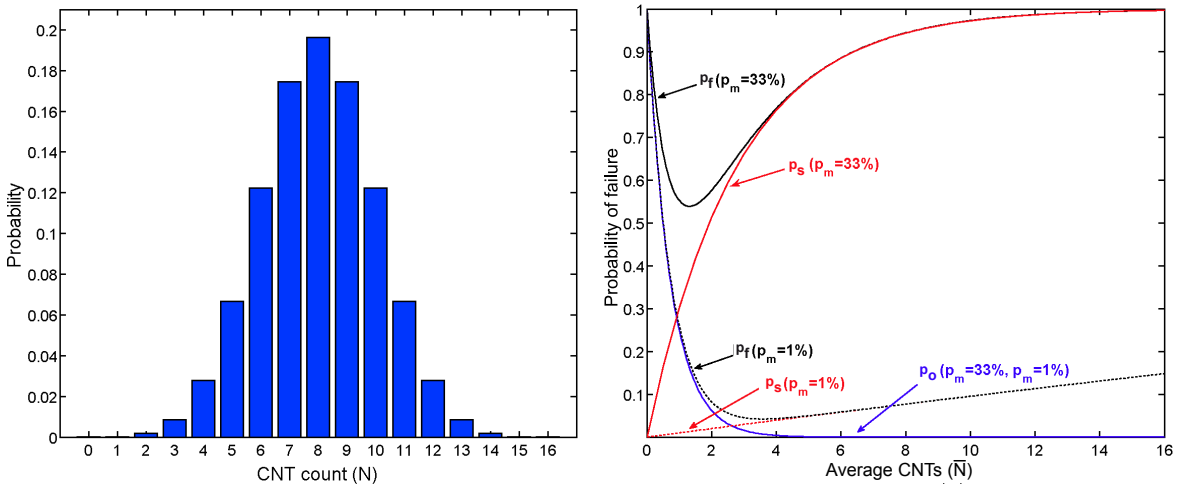
5.1 Causes of Failure in CNFETs: Analytical Models

As we mentioned in the previous Chapter, CNT-specific variations cause fluctuations in the drive currents of CNFETs, which lead to circuit characteristics variations and/or logic failures. CNT count variations and the presence of undesirable metallic CNTs are cause of CNFET failure.

CNT count variations are caused by both CNT density variations that are due to the non-uniform spacing between CNTs during CNT growth process and m-CNT-induced count variations because of the presence of m-CNTs in the transistor and the subsequently application of an m-CNT removal process. CNT count is defined as the number of CNTs that completely bridge the source and drain of the CNFET. Then, a "CNT-count failure" appears when there is no CNT, or no continuous CNT, in the active region (channel) of a CNFET. This failure can be abstracted as an *open defect*, resulting in an *stuck-off fault*. On the contrary, the presence of one or more m-CNTs in the CNFET creates *source-drain short defects*, resulting in an *stuck-on fault*.

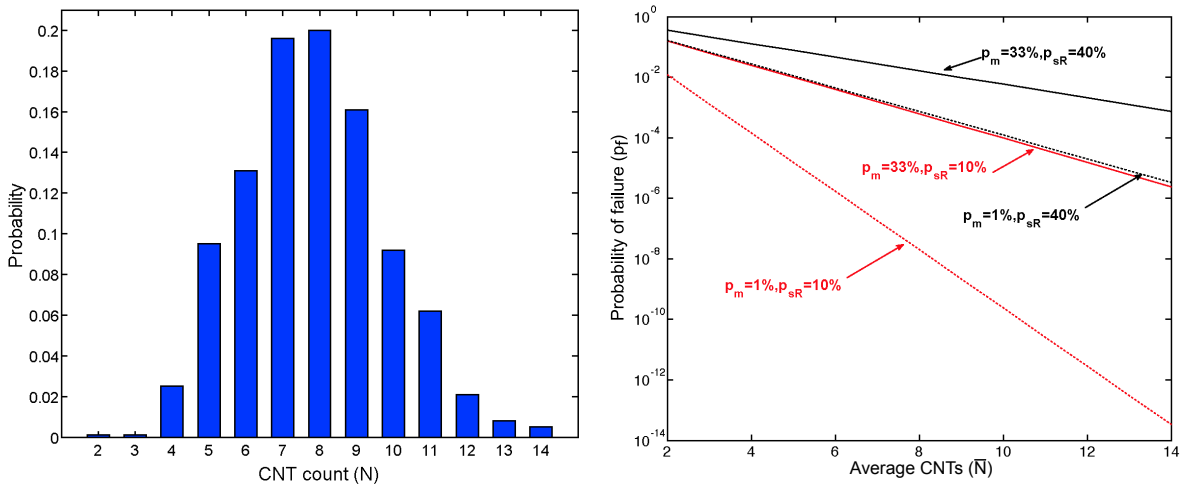
Many publications have presented analytical models to evaluate the impact of CNT density variations, CNT count variations or of m-CNTs on multi-channel CNFET devices and circuits. Compact models for probability of failure in CNFETs that includes CNT density variations and metallic CNTs were presented in [99] and [100]. Both models are able to calculate the probability of a "void CNFET" (open) due to CNT density fluctuations and short defects due to the presence of one or more m-CNTs in the CNFET. No m-CNT removal process is considered in these works. In [75], a probabilistic framework for modeling the CNT count distribution in a CNFET of a given width was developed. It is used to estimate the CNT count yield (CNT count failure) due to CNT count variations. Moreover, this model is only valid when all m-CNTs are removed and then takes only open defects into account. It is worth noting that all these models are gate width (W_{gate}) dependent.

Figures 5.1 and 5.2 show the CNT count distribution and the probability of failure of a CNFET using the models developed in [99] and [75], respectively. Note that both CNT count distributions depend on the W_{gate} and the CNT density distribution (CNT pitch distribution) and could be approximated to a Gaussian distribution as it was demonstrated in [75].



(a) (b)

FIGURE 5.1: (a) Assumed CNT count distribution (binomial distribution) for a $W_{gate} = 32nm$ and an average number of CNTs of $\bar{N} = 8$ ($\mu_{pitch} = 4nm$). (b) Probability of failure (p_f), probability of open (p_o) and probability of short (p_s) in function of average CNTs for $p_m = 33\%$ and $p_m = 1\%$. These both graphs have been obtained using the model presented in [99].



(a) (b)

FIGURE 5.2: (a) CNT count distribution for a $W_{gate} = 32nm$ and using the distribution for CNT density variations shown in Table 4.2. (b) Probability of failure (probability of open) in function of average CNTs for $p_m = 33\%$ and $p_m = 1\%$ and $p_{sR} = 40\%$ and $p_{sR} = 10\%$. This graph has been obtained using the model presented in [75].

In Figure 5.1(b) the probability of failure (p_f) is the sum of the probability of open (or probability of "void CNFET", p_o) and the probability of short (p_s): $p_f = p_o + p_s$. They, p_o and p_s, exhibit opposite behaviors with respect to a change in CNT count; that is, p_o decreases whereas p_s increases as $\bar{N}$ increases. Observe that in p_f for small number of CNTs, the probability of open defect is the dominant component,

and for a large number of CNTs, the probability of short defect is the dominant one. Furthermore, the probability of open is the same for both m-CNT probability (p_m) values considered because it only depends on CNT density variations (no m-CNT removal) but the probability of short increases as p_m increases (red curves), as expected. In Figure 5.2(b) the probability of failure is the probability of open due to CNT density variations and to the application of an imperfect m-CNT removal process in which all m-CNT and some s-CNTs are removed ($p_{mR} = 100\%$ and $p_{sR} = 10 - 40\%$). So p_f decreases as the average number of CNTs increases; or in other words the wider the gate width, the smaller the probability of failure is.

5.2 Derivation of a CNFET Failure Model

As we mentioned in Section 5.1, CNFET failure models presented in previous works include: 1) open and short defects due to CNT density variations and the presence of m-CNTs in the transistor, respectively [99] or 2) only open defects because of CNTs count variations that are caused by density fluctuations and the subsequently application of an imperfect m-CNT removal process in which all m-CNTs and some s-CNTs are removed [75].

As an enhancement/extension of these two previous CNFET failure models, a CNFET failure model that includes both short and open defects is derived and presented in this Section. This model is good for all three m-CNT removal scenarios considered and showed in Section 4.3.2.

Let us consider that a CNT has a probability of being metallic p_m and of being semiconducting $p_s = 1 - p_m$. For an N-tube CNFET, the transistor manifests a short failure when there are one or more m-CNTs. In other words, the device is "not short" only when all the CNTs are semiconducting. We can derive the probability of a transistor's being short ($p_{short_{Ntubes}}$) from the probability of all CNTs being semiconducting [99]

$$p_{short_{Ntubes}} = 1 - p_s^N = 1 - (1 - p_m)^N \tag{5.1}$$

where N is the number of CNTs that forms the transistor.

Let us further consider that the probability of removal during the m-CNT removal process is p_{sR} for s-CNTs and p_{mR} for m-CNTs. So, if a m-CNT removal process is applied,

$$p_{short_{Ntubes}} = 1 - (1 - p_m(1 - p_{mR}))^N \tag{5.2}$$

In contrast, an open occurs when all the CNTs are later removed. Based on [75], the probability of an open for an N-tube CNFET can be calculated as

$$p_{open_{Ntubes}} = (p_m p_{mR} + p_s p_{sR})^N \tag{5.3}$$

Equations 5.2 and 5.3 do not take into account CNT density variations. That is, they assume uniform CNT density. If CNT density variations are considered and based on [99], these two last equations can be rewritten as

$$p_{short_{Ntubes}} = \sum_{k=1}^{2\bar{N}} [(1 - (1 - p_m(1 - p_{mR}))^k) f_{CNT}(k)] \tag{5.4}$$

$$p_{open_{Ntubes}} = \sum_{k=0}^{2\bar{N}} [(p_m p_{mR} + p_s p_{sR})^k f_{CNT}(k)] \tag{5.5}$$

where $\bar{N}$ is the average (or expected) number of CNTs in the CNFET for a given W_{gate} and $f_{CNT}(k)$ is the CNT count probability density distribution or in other words, the probability of having k CNTs under the CNFET gate. It has been taken from [99] and it is given by

$$f_{CNT}(k) = \frac{(2\bar{N})!}{k!(2\bar{N} - k)!}(0.5)^{2\bar{N}} \tag{5.6}$$

Therefore, the overall probability of failure of a single N-tube CNFET is given by

$$p_f = p_{short_{Ntubes}} + p_{open_{Ntubes}} \tag{5.7}$$

Note that 5.7 includes both open and short defects in the presence of CNT-count variations (CNT density variations + m-CNT-induced count variations) and then it is good for both an ideal or non-ideal m-CNT removal processes.

When no m-CNT removal process is applied, the overall probability of a single failure of a N-tube CNFET is

$$p_{f_{without-removal}} = p_{short_{Ntubes}} + f_{CNT}(0) \tag{5.8}$$

where $f_{CNT}(0)$ is the probability of open due to CNT density variations (also called probability of "void CNFET").

Using Equations 5.7 and 5.8, Figure 5.3 shows the probability of CNFET failure (p_f) versus the average number of CNTs in the channel ($\bar{N}$) for the three m-CNT removal cases shown in Chapter 4, Section 4.3.2 and for different p_m.

When m-CNTs are not eliminated (Figure 5.3(a)), the probability of failure is the sum of the probability of a short and the probability of open ("void CNFET") and then it behaves similar to Figure 5.1(b), declining sharply at the outset, before gradually rising back up. At first the probability of an open is the dominant component, but, as the average number of CNTs increases, the probability of a short becomes dominant. Furthermore, it is worth noting that there is an optimum average number of CNTs that minimize the probability of failure. In this particular case the minimum probability of failure (p_{fmin}) is $4 \cdot 10^{-2}$ (for $p_m = 1\%$) and $54 \cdot 10^{-2}$ (for $p_m = 33\%$), which occurs at optimum point of $\bar{N} = 4$ and $\bar{N} = 1$ respectively. These values are certainly unacceptable for any VLSI design application today because it means a circuit yield near to 0%. So, m-CNTs must be removed.

In the case of an ideal m-CNT removal process ($p_{mR} = 100\%$ and $p_{sR} = 0\%$), the p_f is the probability of an open. As shown in Figure 5.3(b), it is much lower than in the previous case and it decreases as $\bar{N}$ becomes bigger. Therefore, in this case upsizing CNFETs is an effective but expensive way to reduce p_f.

When a non-ideal m-CNT removal technique is applied, two different behaviors can be observed. If we consider that all m-CNTs and some s-CNTs are removed ($p_{mR} = 100\%$ and $p_{sR} = 10\% - 40\%$), p_f is once again the probability of an open, as shown in Figure 5.3(c). This is similar to Figure 5.3(b), but presents higher values. In contrast, if a small portion of the m-CNTs survives ($p_{mR} = 99.99\%$ and $p_{sR} = 10\% - 40\%$), the probability of CNFET failure is the sum of p_{open} and p_{short} (Figure 5.3(d). It behaves similar to Figure 5.3(a) but shows smaller p_f values. It should moreover be noted that

the probabilities of failure are different for a single p_m for the two p_{sR} considered when $\bar{N}$ is small, but that they become identical as of a given value of $\bar{N}$. Finally, it is worth noting that there is again a minimum probability of failure for each case considered but it is still too high for VLSI systems (e.g. p_{fmin}=10^{-5} for $p_m = 1\%$ and $p_{sR} = 10\%$).

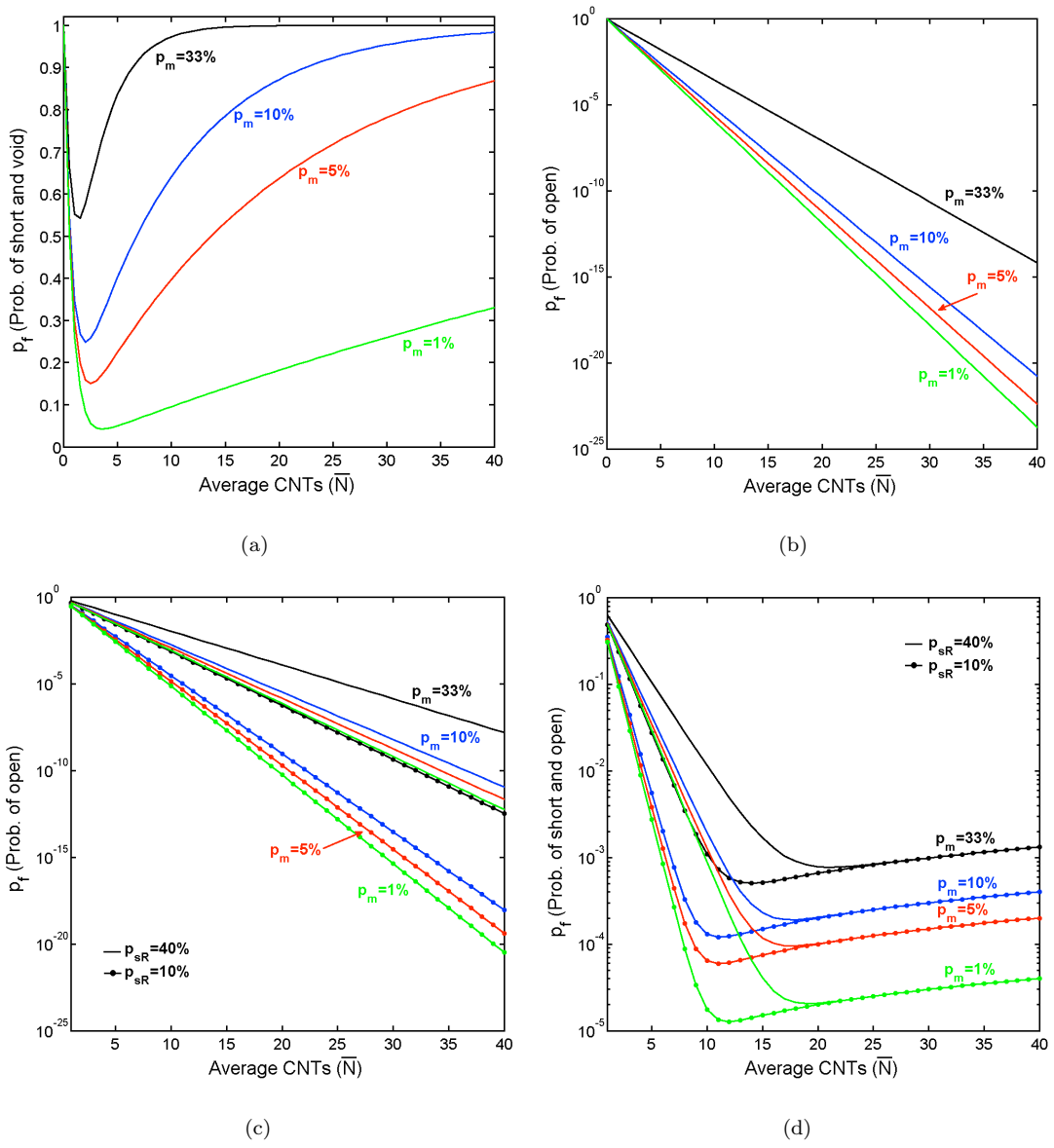


FIGURE 5.3: Probability of CNFET failure vs. average CNTs: (a) when no m-CNTs are removed; (b) when an ideal m-CNT removal process is considered; and (c) and (d) when a non-ideal m-CNT removal process is applied for $p_{mR} = 100\%$ and $p_{mR} = 99.99\%$, respectively.

As we mentioned, the probabilities of failure shown in Equations 5.7 and 5.8 are for a single multi-channel CNFET, but it is also interesting to evaluate the probability of failure at circuit level. For this purpose, we consider a chip of M transistors. If we

assume that they are independent of each other (uncorrelated devices), the circuit-level probability of failure is

$$Pf_{uncorrelated} = 1 - \prod_{i=1}^{M}(1 - p_{f_i}) \tag{5.9}$$

where p_{f_i} is the probability of failure of a single N-tube CNFET shown in Equation 5.7 (or in Equation 5.8).

However, correlation between CNFETs can be used a technique to reduce the CNFET circuit's probability of failure and then to improve their yield [101]. If a correlated design is used, in which CNFETs are distributed in C columns and R rows [101]; and it is assumed that the CNFETs in the same column are perfectly correlated (CNFETs that share CNTs), whereas the CNFETs taken from different columns do not share common CNTs and are therefore independent with each other, the circuit-level probability of failure can be rewritten as

$$Pf_{correlated} = 1 - \prod_{i=1}^{C}(1 - p_{f_i}) \tag{5.10}$$

where C is the number of columns, and can be calculated as C=M/R.

5.3 Analysis of the Probability of CNFET Failure: Simulation Results

Using the MC procedure shown in Figure 4.6, Section 4.3.1, a CNFET device reliability analysis has been made. For this purpose, 10000 MC simulations (10000 CNFET samples) are run. The average number of CNTs/CNFET is $\bar{N}$=8. The percentage of non-functional (CNFETs that have short and open defects) and functional transistors (CNFETs free of defects) can be observed in Tables 5.1, 5.2, 5.3, and 5.4.

If m-CNT are not removed (Table 5.1), only shorts are observed. Note that opens could be also appear if $\bar{N}$ is smaller. Obviously, the percentage of non-functional transistors increases as p_m increases, being of 93.9% for p_m = 33%. Shorts are also illustrated in Figure 4.7(b). The black curves representing a very high I_{OFF} ($\sim 10^{-6}A$) are shorts when one or more CNTs are metallic, whereas the green line is a short when all CNTs

are metallic. They are called *Drain Source Soft Short* (DSSS) and *Drain Source Hard Short* (DSHS), respectively.

When an ideal m-CNT removal technique is considered, 100% of transistors are functional except for $p_m = 33\%$ in which a very low percentage of CNFETs present an open failure (0.1 %, Table 5.2). These opens can also be observed in Figure 4.7(d), blue lines. As we pointed out before, shorts can not occur because all m-CNTs are eliminated, only s-CNTs survive.

TABLE 5.1: Percentage of functional and non-functional transistors when no m-CNT removal process is applied (10000 CNFET samples, $\bar{N}$=8)

	No m-CNT removal		
	Non-functional CNFETs		Functional CNFETs
	Shorts	Opens	
$p_m = 33\%$	93.9 %	0 %	6.1 %
$p_m = 10\%$	55.2 %	0 %	44.8 %
$p_m = 5\%$	32.1 %	0 %	67.9 %
$p_m = 1\%$	8.0 %	0 %	92.0 %

TABLE 5.2: Percentage of functional and non-functional transistors when an ideal m-CNT removal process is applied (10000 CNFET samples, $\bar{N}$=8)

	Ideal m-CNT removal		
	Non-functional CNFETs		Functional CNFETs
	Shorts	Opens	
$p_m = 33\%$	0 %	0.1 %	99.9 %
$p_m = 10\%$	0 %	0 %	100 %
$p_m = 5\%$	0 %	0 %	100 %
$p_m = 1\%$	0 %	0 %	100 %

If non-ideal m-CNT removal method is applied, more than 96% of CNFETs are functional for both p_{mR} cases considered (Tables 5.3 and 5.4). And again, the higher the p_{sR} and p_m, the greater the percentage of failures. When $p_{mR} = 100\%$ only a small percentage of opens appears being the worst case 3.2% of failures. With a probability of a m-CNT is removed very close to 100% ($p_{mR} = 99.99\%$) a very small percentage of shorts can be observed in some cases (Table 5.4). These results seem to be quite good, however using our failure probability model and for an CNT average of 8, the total failure probability of a CNFET is in order of 10^{-4} for the best case of p_m (Figure

5.3(d)). This is a high failure probability if we think that VLSI integrated circuits have billions of transistors.

TABLE 5.3: Percentage of functional and non-functional transistors when a non-ideal m-CNT removal process is applied ($p_{mR} = 100\%$, 10000 CNFET samples, $\bar{N}$=8)

		Non-ideal m-CNT removal ($p_{mR} = 100\%$)		
		Non-functional CNFETs		Functional CNFETs
		Shorts	Opens	
$p_m = 33\%$	$p_{sR} = 40\%$	0 %	3.2 %	96.8 %
	$p_{sR} = 10\%$	0 %	0.4 %	99.6 %
$p_m = 10\%$	$p_{sR} = 40\%$	0 %	0.8 %	99.2 %
	$p_{sR} = 10\%$	0 %	0.05 %	99.95 %
$p_m = 5\%$	$p_{sR} = 40\%$	0 %	0.5 %	99.5 %
	$p_{sR} = 10\%$	0 %	0.01 %	99.99 %
$p_m = 1\%$	$p_{sR} = 40\%$	0 %	0.5 %	99.5 %
	$p_{sR} = 10\%$	0 %	0 %	100 %

TABLE 5.4: Percentage of functional and non-functional transistors when a non-ideal m-CNT removal process is applied ($p_{mR} = 99.99\%$, 10000 CNFET samples, N=8)

		Non-ideal m-CNT removal ($p_{mR} = 99.99\%$)		
		Non-functional CNFETs		Functional CNFETs
		Shorts	Opens	
$p_m = 33\%$	$p_{sR} = 40\%$	0.03 %	3.0 %	97 %
	$p_{sR} = 10\%$	0.04 %	0.3 %	99.7 %
$p_m = 10\%$	$p_{sR} = 40\%$	0.02 %	0.8 %	99.2 %
	$p_{sR} = 10\%$	0 %	0 %	100 %
$p_m = 5\%$	$p_{sR} = 40\%$	0 %	0.4 %	99.6 %
	$p_{sR} = 10\%$	0 %	0 %	100 %
$p_m = 1\%$	$p_{sR} = 40\%$	0 %	0.4 %	99.6 %
	$p_{sR} = 10\%$	0 %	0 %	100 %

5.4 Summary and Conclusions

In this chapter a complete reliability analysis of CNFET devices in the presence of CNT-specific variations was presented.

The causes of failure in CNFET devices and circuits are: 1) CNT density variations that are due to the non-uniform spacing between CNTs during the CNT synthesis, 2) CNT count variations that are caused by CNT density variations and by the elimination of some CNTs when a m-CNT removal process is applied (m-CNT induced count

variations), and 3) the presence of m-CNTs in the transistor. The first two may produce *open defects*, when there is no CNT bridging the source and the drain of the CNFET, whereas the latter may cause *short defects* when there are one or more metallic CNTs in the transistor, resulting in *stuck-off* and *stuck-on faults*, respectively.

In first place, we review the most recent CNFET failure models. Some of them include both open and short defects due to CNT density variations and the presence of m-CNTs; that is, no m-CNT removal process is considered. In other failure model, only open defects due to CNT count variations are taken into account; that is, an imperfect removal process in which all m-CNTs and also some s-CNTs are removed is considered. Based on these analytical models for CNFET failure, we derive a CNFET failure model that includes both open and short defects that are caused by CNT count variations (CNT density variations + m-CNT induced count variations) and the presence of m-CNTs and is acceptable for no m-CNTs removal as well as an ideal or non-ideal m-CNT removal is assumed.

Using this model we show that metallic CNTs must be eliminated because they result in short defects. In 1-tube CNFETs, there is a 1% probability of short with just a 1% probability of m-CNT ($p_m = 1\%$); this probability grows higher in multi-channel CNFETs, reaching a value of $\sim 100\%$ when $p_m = 33\%$ and the average number of CNTs (N) exceeds 13. Different m-CNT removal techniques are used to reduce the probability of a CNFET short, but their use increases the variations in CNT count; in other words, by reducing the average number of CNTs in the transistor, they increase the probability of an open defect. If a non-ideal m-CNT removal process is used, in which some s-CNTs are eliminated and a small percentage of m-CNTs survives ($p_{mR} = 99.99\%$); there is a unique optimum average number of CNTs. It should be noted that for the best case considered ($p_m = 1\%$, $p_{mR} = 99.99\%$, and $p_{sR} = 10\%$), the minimum probability of CNFET failure was in the order of 10^{-4}, which is very high for VLSI systems that are composed of billions of transistors. If an ideal m-CNT removal process could be achieved, in which all m-CNTs were removed whereas all s-CNTs kept intact, between 16 ($p_m = 1\%$) and 26 CNTs ($p_m = 33\%$) would be required to ensure a $p_f = 10^{-10}$ and, thus, a yield of $\sim 100\%$. This average number of CNTs could be reduced if a uniform CNT density could be obtained; in that case, only between 5 and 20 CNTs would be needed to reach such p_f.

In second place, using the MC procedure presented in the previous chapter (Section 4.3.1), we obtain the percentage of functional and non-functional transistors (CNFETs with short defects or open defects) for all three m-CNT removal scenarios and for the different p_m. If m-CNTs are not removed, only short defects are observed. The percentage of short defects decreases as p_m decreases, being of 8% for $p_m = 1\%$, that is similar to the p_f showed using our CNFET failure model (for N=8 and $p_m = 1\%$, the $p_f = 7.7\%$). If an ideal m-CT removal is considered, only open defects appear when $p_m = 33\%$ (0.1% of non-functional transistors). Finally, if the m-CNT removal process is non-ideal, in which all ($p_{mR} = 100\%$) or almost all ($p_{mR} = 99.99\%$) m-CNTs are eliminated, more than 96% of CNFETs are functional. These results seem to be acceptable, however if only a 0.01% of m-CNTs survives to the m-CNT removal process, the p_f is $\sim 10^{-4}$ for a CNT average of $\bar{N} = 8$, $p_m = 1\%$ and $p_{sR} = 10\%$ that is unacceptable for VLSI systems, as we mentioned. Note, that these percentages of functional and non-functional transistors are for the case that all CNFETs are independent or uncorrelated. But, the percentage of functional CNFETs can be improved considering correlation between CNFETs. In other words, correlation between the CNFETs that form a chip can be used as a technique to reduce the CNFET circuit's probability of failure and then enhance its yield.

To conclude, it is worth noting that m-CNTs are the major "problem" in CNFET manufacturing from the point of view of reliability because they result in higher probability of device failure (probability of short) than CNT density variations (probability of open) and they are not only cause short defects but also may be cause of open defects when they are removed. So, the following efforts need to be made in CNFET technology to improve its yield: 1) to enhance CNT synthesis techniques to reach a 100% of s-CNTs with uniform CNT density, 2) to improve m-CNT removal techniques to eliminate all m-CNTs and no s-CNTs, 3) to optimize circuit design techniques and to develop defect and fault tolerant techniques for CNFET circuits in order to deal with the possible presence of a small percentage of m-CNTs.

Chapter 6

Variability in CNFET Circuits

CNFET-based digital systems fabricated with perfect CNT synthesis are predicted to be 5x faster than silicon CMOS while consuming the same power at 16nm technology node; or in other words, they can potentially provide more than an order of magnitude benefit in *Energy-Delay Product* (EDP) over silicon CMOS at highly-scaled technology nodes [43], [102]. But, CNT-specific variations cause fluctuations in the drive current of multi-channel CNFET and affect its gate capacitance, which lead to delay and noise margin variations in CNFET logic gates degrading their performance and robustness.

In this chapter the circuit level performance of CNFET technology in the presence of CNT manufacturing imperfections is evaluated. The impact of CNT-specific variations on CNFET digital circuits is investigated by induced threshold voltage fluctuations. The chapter is organized as follows. In Section 6.1, the impact of such V_{TH} variations on a CNFET inverter (chain) and on a pair of cross-coupled CNFET inverters is analyzed. A procedure to translate the CNT-specific variations to equivalent V_{TH} variations is presented. The variability of some important metrics of logic circuits that includes the delay, figure of merit of logic speed, and the noise margin, figure of merit of logic robustness, is analyzed. In Section 6.2 the write and read delay variation of a CNFET 6T SRAM cell in the presence of CNT-specific variations is evaluated and compared with the delay variability of a MOSFET 6T SRAM cell affected by process variations. Finally, conclusions and a summary of the Chapter are presented in Section 6.3.

6.1 CNFET Inverter

6.1.1 Delay

The inverter propagation delay is the time delay between the input and output signals. The propagation delay times can be obtained graphically from the input and output signals as illustrated in Figure 6.1. t_{PHL} is the propagation delay from high-to-low between 50% points and t_{PLH} is the propagation delay from low-to-high between 50% points.

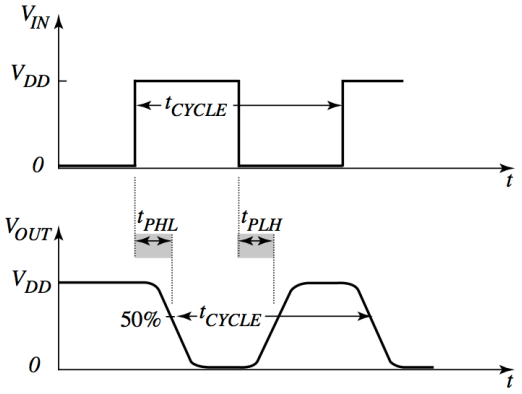


FIGURE 6.1: Propagation delay times.

The analytical expression for the propagation delay of a logic gate was derived in [43]. The propagation delay ($\tau_{CNFET,N}$) through a CNFET with N parallel semiconducting CNTs can be estimated from the drive current of the CNFET ($I_{CNFET,N}$) and the capacitance of the subsequent CNFET gate that is driven ($C_{CNFET,N}$) as [43]

$$\tau_{CNFET,N} \propto \frac{C_{CNFET,N} V_{supply}}{I_{CNFET,N}} \tag{6.1}$$

The ON current for a CNFET with a single CNT ($I_{CNFET,1}$) can be expressed as

$$I_{CNFET,1} = g_{CNT}(V_{supply} - V_{SS'} - V_{th,CNT}) \tag{6.2}$$

where $V_{th,CNT}$ is the threshold voltage, g_{CNT} is the transconductance per CNT, and $V_{SS'}$ is the voltage drop across the doped CNT source region.

For a CNFET with N CNTs, the drive current ($I_{CNFET,N}$) can be expressed as [43]

$$I_{CNFET,N} = N g_{CNT}(V_{supply} - V_{SS'} - V_{th,CNT}) \tag{6.3}$$

Then, gate drive current variations in a N-tube CNFET are mainly due to CNT-specific variations as we have demonstrated in Chapter 4 but also because of changes in other transistor parameters such as supply voltage and the length of the doped CNT source region [43].

The capacitance of a N-tube CNFET ($C_{CNFET,N}$) is approximately equal to its gate capacitance ($C_{g-total(CNT),N}$), $C_{CNFET,N} \approx C_{g-total(CNT),N}$ since the CNT source-to-substrate and CNT drain-to-substrate capacitances are small [67].

For a CNFET with a single CNT, the CNFET gate capacitance $C_{g-total(CNT),1}$ can be divided in two components [43]:

1. $C_{g-CNT,1}$ expressed as capacitance per CNT per unit gate length (L_g). This includes the gate-to-CNT channel capacitance ($C_{g-intrinsic}$) and the gate-to-doped CNT source and drain capacitance ($C_{g-doped}$).

2. $C_{g-parasitic}$ expressed as capacitance per unit gate width. This includes coupling capacitance between the gate and adjacent contacts (or adjacent gates) ($C_{g-contact}$) and the gate-to-substrate capacitance (C_{g-sub}).

$$C_{g-CNT,1} = C_{g-intrinsic} + C_{g-doped} \tag{6.4}$$

$$C_{g-parasitic} = C_{g-contact} + C_{g-sub} \tag{6.5}$$

Then, the total gate capacitance for a CNFET with a single CNT can be approximated by

$$C_{g-total(CNT),1} = C_{g-CNT,1} L_{g,CNT} + C_{g-parasitic} W_{g,CNT} \tag{6.6}$$

where $W_{g,CNT}$ is the width and $L_{g,CNT}$ is the length of the lithographically defined gate.

For a CNFET with N parallel CNTs under a gate of width $W_{g,CNT}$, the gate capacitance can be expressed as

$$C_{g-total(CNT),N} = C_{g-CNT,N} L_{g,CNT} + C_{g-parasitic} W_{g,CNT} \tag{6.7}$$

where $C_{g-CNT,N} = N \cdot C_{g-CNT,1}$.

The expressions for all these capacitances, $C_{g-intrinsic}$, $C_{g-doped}$, $C_{g-contact}$, and C_{g-sub}, can be found in [66]. In this work the dependence of such capacitances on some CNFET structural parameters is shown. For example, both the gate-to-CNT channel capacitance $C_{g-intrinsic}$, and the gate-to-doped CNT source and drain capacitance $C_{g-doped}$, depend on CNT diameter, pitch, oxide thickness, and substrate dielectric constant, among others. But, note that they are especially affected by the number of CNTs and its position in the array on CNTs, *edge* or *middle*, because of charge screening effect [66]; that is, both $C_{g-intrinsic}$ and $C_{g-doped}$ can be divided in two groups: edge and middle and their expression for a N-tube CNFET ($N \geq 2$) is

$$C_{g-intrinsic} = 2C_{g-intrinsic-edge} + (N-2)C_{g-intrinsic-middle} \tag{6.8}$$

$$C_{g-doped} = 2C_{g-doped-edge} + (N-2)C_{g-doped-middle} \tag{6.9}$$

From this analytical delay model we can conclude that CNT density variations together with m-CNT induced count variations when a m-CNT removal process is applied constitute the most prominent sources of both drive current variations (as we demonstrated in Chapter 4) and capacitance variations and then delay fluctuations. So, at his point, we find it interesting that the behavior of ON current and delay in the presence of CNT density variations is shown and analyzed. Figure 6.2 shows I_{ON} in function of pitch (inter-CNT spacing) and the number of CNTs per transistor. For a particular and fixed pitch, I_{ON} increases as the average number of CNTs increases (that implies an increased W_{gate}); for a given number of CNTs, I_{ON} increases as pitch increases as illustrated in Figure 6.2. Observe that from a certain pitch value ($\sim 20nm$) the I_{ON} keeps almost constant. This is because multi-channel CNFETs suffer the called charge screening effect when the distance between CNTs is smaller than 20nm, affecting the drive current of the transistor, as we mentioned in Chapter 4, Section 4.1.

The impact of charge screening effect on I_{ON} can also be observed in Figure 6.3. For a given W_{gate}, the I_{ON} initially increases due to the increased number of CNTs. The I_{ON} subsequently decreases as a result of smaller and smaller pitch and then increased inter-CNT electrostatic charge screening effects. Therefore, there is a clear trade-off between the pitch and the number of CNTs in the transistor. But, exits an optimum number of CNTs (N_{opt}) per CNFET that maximizes the drive current (e.g. for $W_{gate} = 16nm$, the optimum number of CNTs is $N_{opt} = 3$). A similar behavior can be observed in

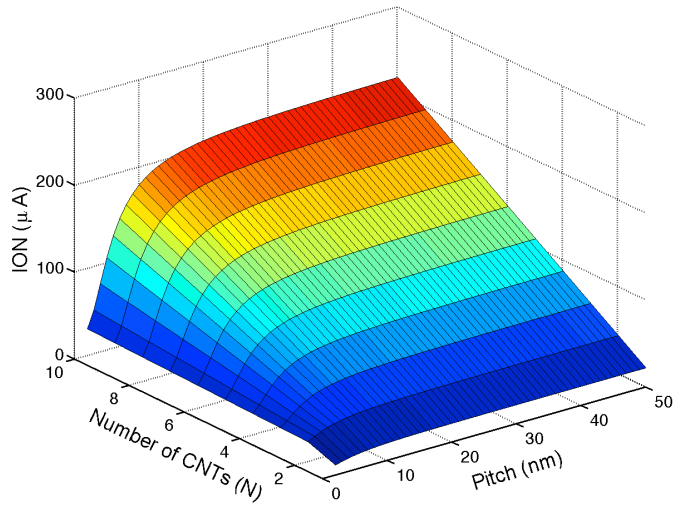


FIGURE 6.2: Drive current in function of inter-CNT spacing and the number of CNTs per transistor.

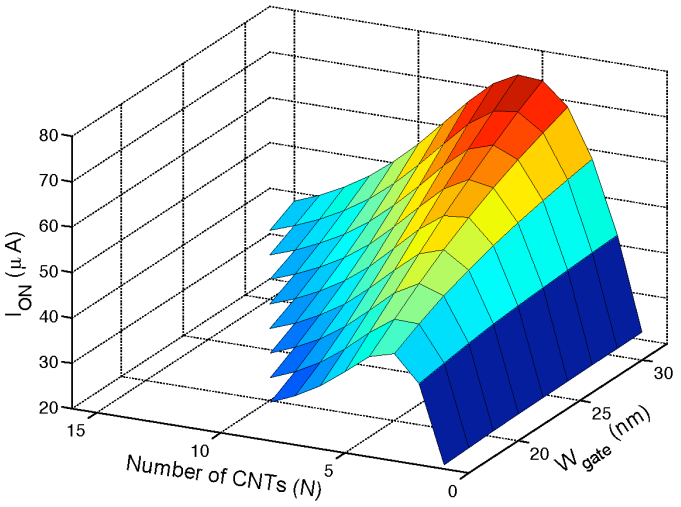


FIGURE 6.3: Drive current in function of the number of CNTs per transistor and W_{gate} (from 16nm to 32nm). For $W_{gate} = 16nm$, the maximum number of tubes is 8 (minimum pitch is 2nm) and N_{opt}=3. For $W_{gate} = 32nm$, the maximum number of tubes is 16 and N_{opt}=6.

the propagation delay of a CNFET inverter. Figure 6.4, shows the delay of a CNFET inverter in function of N and W_{gate}. And again, there is an optimum number of CNTs for each gate width that minimizes the delay (e.g. 6 CNTs per 32nm of gate width gives optimal delay).

Some previous works focus on CNT density and m-CNT induced count variations to quantify their impact on the overall delay variations of CNFET digital circuits. For the first time, in [96] the impact of CNT count variations on circuit delay was evaluated. They adapted an existing Monte Carlo-based statistical static timing analysis approach

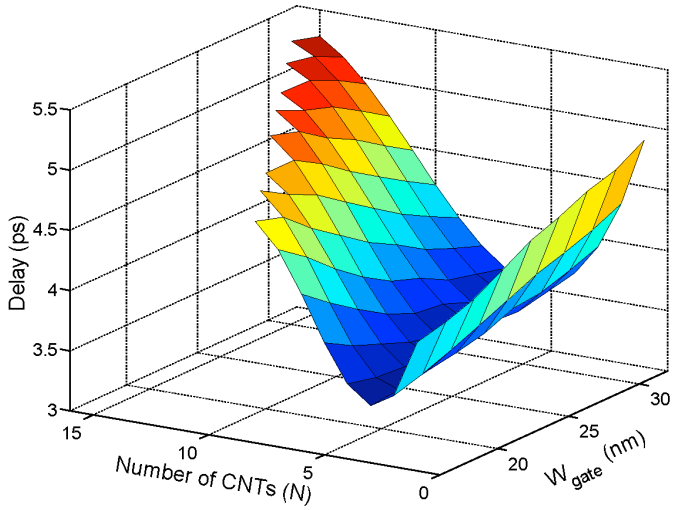


FIGURE 6.4: Average propagation delay ($t_p = (t_{PHL} + t_{PLH})/2$) of a CNFET inverter in function of the number of CNTs per transistor and W_{gate} (from 16nm to 32nm). For $W_{gate} = 16nm$, the maximum number of tubes is 8 (minimum pitch is 2nm) and N_{opt}=3. For $W_{gate} = 32nm$, the maximum number of tubes is 16 and N_{opt}=6.

by using variation-aware timing model for CNFET logic gates based on CNFET device model (Stanford model) and CNT count variations model [75] (shown in Figure 5.2). However, this model is not analytical and it depends on the CNT spacing distribution. In [103] an analytical model for prediction of gate-delay variation in CNFETs that is caused by CNT density variation was developed. This model is based on their previously derived CNT density distribution model [99] (shown in Figure 5.1). Finally, in [43] a delay analytical model was presented and used to discuss delay improvement of CNFET technology over silicon CMOS as a function of technology node and for different CNT densities. In our work, we simulate and evaluate the impact of not only CNT density and m-CNT count variations but also the rest of CNT-specific variations, CNT doping, alignment and diameter variations, on the delay of a CNFET inverter (chain).

6.1.2 Noise Margin

The *Noise Margin* (NM) is another important metric in logic circuits because it describes the robustness or stability of a logic gate or memory cell. The concept of the noise margin was developed by Hill in the late 1960s [104]. Noise margin was originally defined as "the maximum allowable spurious signal that can be accepted by a device when used in a system while still giving correct operation".

In this work, we use two different approaches to evaluate the noise margin of digital circuits: 1) High and Low Noise Margins (NM_H and NM_L) of a CNFET inverter and 2) Static Noise Margin (SNM) of a cross-coupled CNFET inverters.

6.1.2.1 High and Low Noise Margins

For an inverter, it is possible to define the high and low voltages V_{OH} and V_{OL}, where V_{OH} is the minimum output high voltage and V_{OL} is the maximum output low voltage. Furthermore, one can define the transition points V_{IH} and V_{IL}, where V_{IH} is the minimum input high voltage that can be treated as a high voltage at the input of an inverter and V_{IL} is the maximum input low voltage that can be treated as a low voltage at the input of an inverter. If one has an inverter satisfying the relationships

$$V_{in} \leq V_{IL} \Rightarrow V_{out} \geq V_{OH} \tag{6.10}$$

$$V_{in} \geq V_{IH} \Rightarrow V_{out} \leq V_{OL} \tag{6.11}$$

$$V_{IH} > V_{IL} \tag{6.12}$$

with V_{in} being the input voltage and V_{out} the output voltage of the inverter, then the high- and low-state noise margins (NM_H and NM_L, respectively) can be defined mathematically as

$$NM_H = V_{OH} - V_{IH} \tag{6.13}$$

$$NM_L = V_{IL} - V_{OL} \tag{6.14}$$

The V_{OH}, V_{OL}, V_{IH}, and V_{IL} values can be obtained graphically from the voltage transfer characteristic (VTC) of the inverter as shown in Figure 6.5.

It is worth noting that CNT density (and count) variations, the most prominent source of drive current variations, seems to have a minor impact on noise margin as shown in Figure 6.6. It depicts NM_H and NM_L of a CNFET inverter, in which both p-CNFET and n-CNFET have the same number of tubes, as a function of the number of CNTs per transistor and W_{gate}; both NMs suffer a little increase as N increases. However, the effect of CNT density variations on noise margin gains importance when p- and n-CNFET do

not have the same number of CNTs (they are uncorrelated) as we will demonstrate in Section 6.1.3.2.

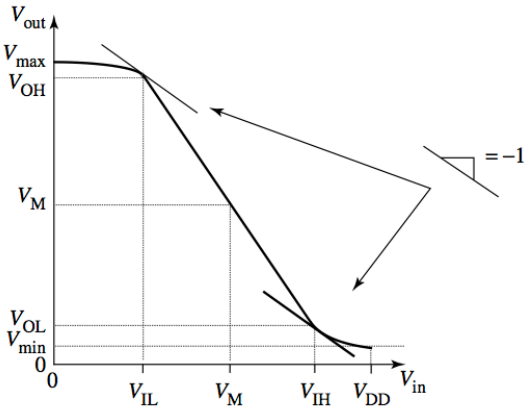
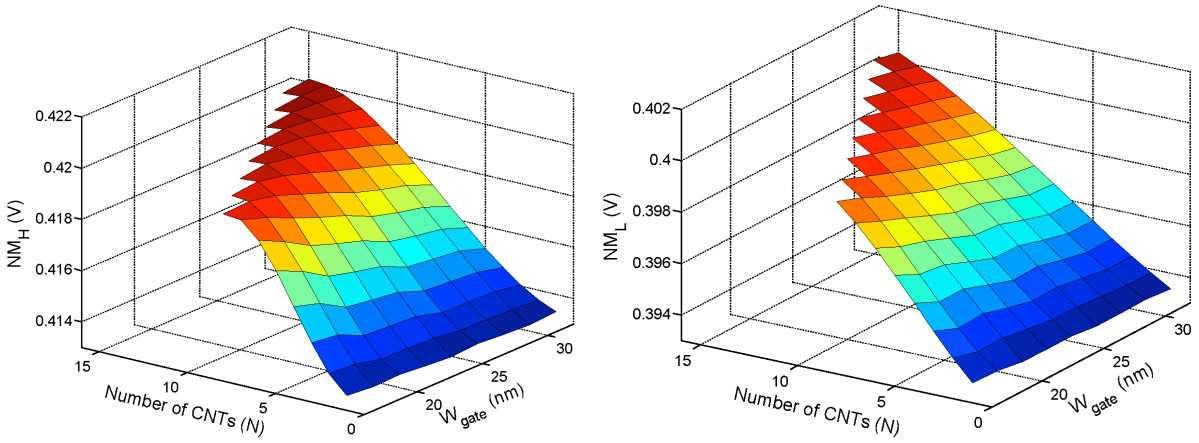


FIGURE 6.5: The voltage transfer characteristic of an inverter.

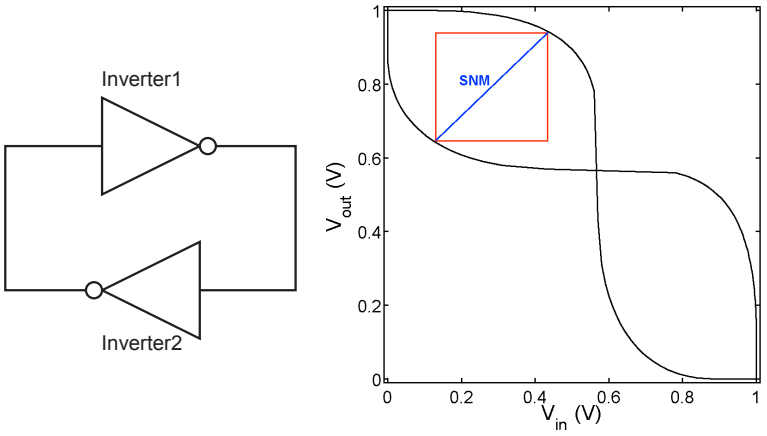


(a) (b)

FIGURE 6.6: (a) NM_H and (b) NM_L of a CNFET inverter in function of the number of CNTs per transistor and W_{gate}.

6.1.2.2 Static Noise Margin

The SNM is the maximum amount of noise voltage that can be tolerated at the inputs of the cross-coupled inverters in different direction while inverters still maintain bi-stable operating points. The most common way of representing the SNM graphically is shown in Figure 6.7(b); it plots the two curves representing the VTC of the inverters that are inverted form each other. The resulting two-wing curve is called *butterfly curve* and is used to determine the SNM. The SNM is defined as the length of the side of the largest nested square that can be embedded inside smaller wind of the butterfly curve.



(a) (b)

FIGURE 6.7: (a) Cross-coupled CNFET inverters (b) SNM graphical definition.

To the best of our knowledge, there is no any previous work that analyzes the variation of noise margin due to CNT-specific variations. In this thesis, we analyze the impact of all CNT-specific variations (CNT density variations, m-CNT induced variations and CNT alignment, doping, and diameter variations) on delay and noise margin of a CNFET inverter (chain), and static noise margin of a pair of cross-coupled CNFET inverters when an ideal m-CNT removal process is considered.

6.1.3 Delay and Noise Margin Variations: Simulation Results

In this Section, we discuss the noise margin and delay variation of a CNFET inverter (chain) and the SNM variation of a pair of cross-coupled CNFET inverters in the presence of CNT-specific variations. As we will see, CNT-specific variations are studied by induced threshold voltage fluctuations.

At this point, it should be pointed that correlation between CNFETs can be used as a technique to improve the SNM [75] and also to improve the yield of CNFET circuits as we have shown in Chapter 5. In this section we will analyze if such correlation can be also used to reduce the variability in CNFET circuits in the presence of CNT-specific variations.

6.1.3.1 CNFET Circuit Variability: From I_{ON} Variations to Equivalent V_{TH} Variations

Often, the impact of process variations such as oxide thickness in MOSFET circuits is analyzed by induced threshold voltage fluctuations [105]. In our work we use this approach to analyze the variability of CNFET circuits under CNT-specific variations caused by CNFET manufacturing imperfections; that is, CNT-specific variations will be reflected into equivalent V_{TH} variations in CNFET logic circuits. For this purpose, we use the nominal CNFET device and the I_{ON} variability results presented in Chapter 4, Section 4.1 and Section 4.4, respectively and translate these I_{ON} variations (Figure 6.8) into ΔV_{TH} fluctuations (Figure 6.9).

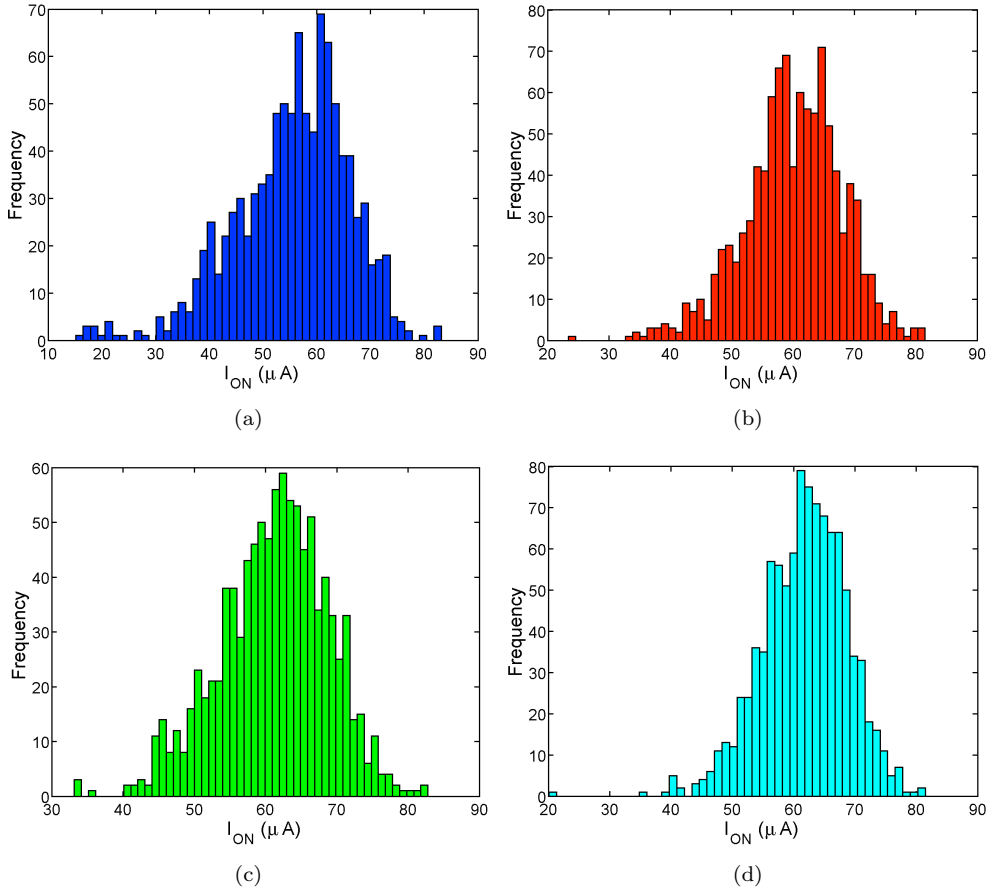


FIGURE 6.8: I_{ON} distribution of the n-type CNFET (nominal device) affected by CNT-specific variations and for (a) $p_m = 33\%$, (b) $p_m = 10\%$, (c) $p_m = 10\%$ and, (d) $p_m = 1\%$.

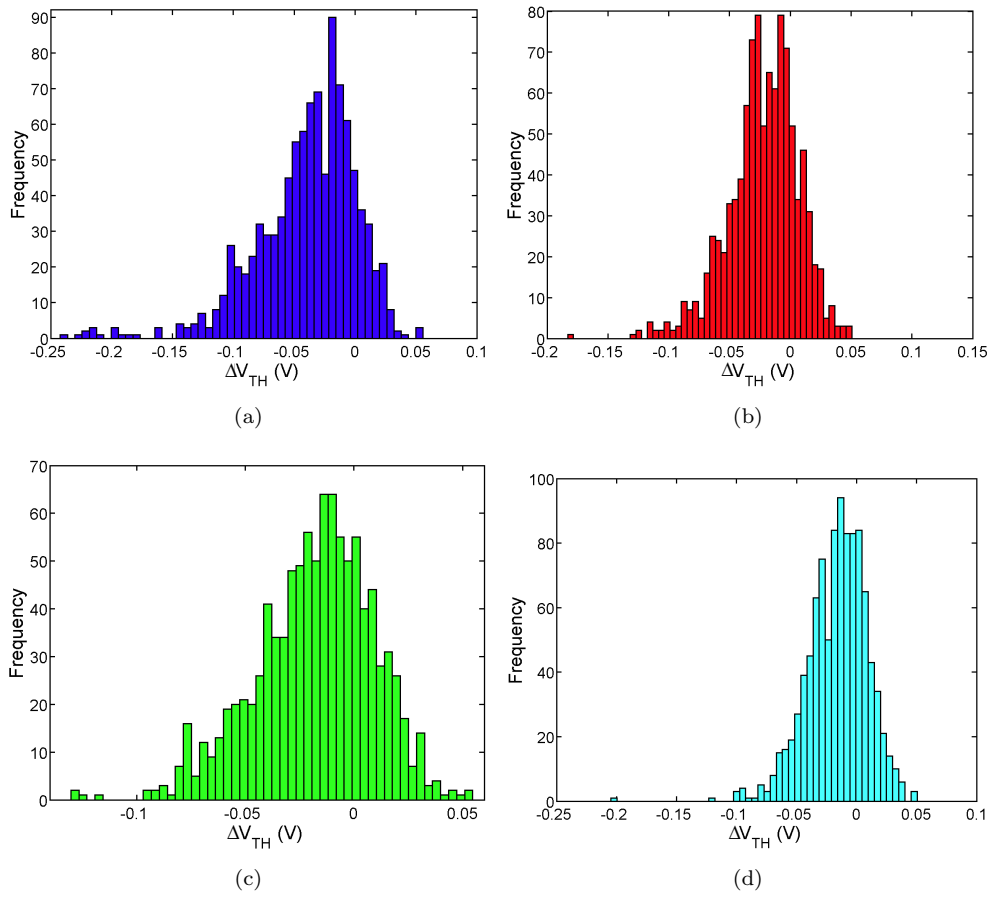


FIGURE 6.9: ΔV_{TH} distribution obtained from I_{ON} distribution and for (a) $p_m = 33\%$, (b) $p_m = 10\%$, (c) $p_m = 10\%$ and, (d) $p_m = 1\%$.

The flow chart for translating the I_{ON} distributions showed in Figure 6.8 into threshold voltage distributions (Figure 6.9) is illustrated in Figure 6.10. First, an I_{ON} sample is taken from the I_{ON} distribution. Then, the V_{TH} of our nominal CNFET device is changed (ΔV_{TH} application) and the related I_{ON} is measured ($I_{ON-measured}$). This last step is repeated until the measured I_{ON} is identical to the initial I_{ON} taken from our distribution. Finally, the ΔV_{TH} distribution is obtained. Figure 6.8 and 6.9 show the I_{ON} distributions of an n-type CNFET affected by CNT-specific variations and their corresponding ΔV_{TH} distributions for different p_m, respectively. Note that these I_{ON} distributions are for the case when an ideal m-CNT removal process is applied, so it is assumed that all m-CNTs are removed. Then in this Chapter p_m means the initial proportion of m-CNTs that are subsequently removed.

From now on, for variability simulation of CNFET digital circuits we use the nominal CNFET device presented in Chapter 4, Section 4.1 and applied the ΔV_{TH} distribution obtained in this Section.

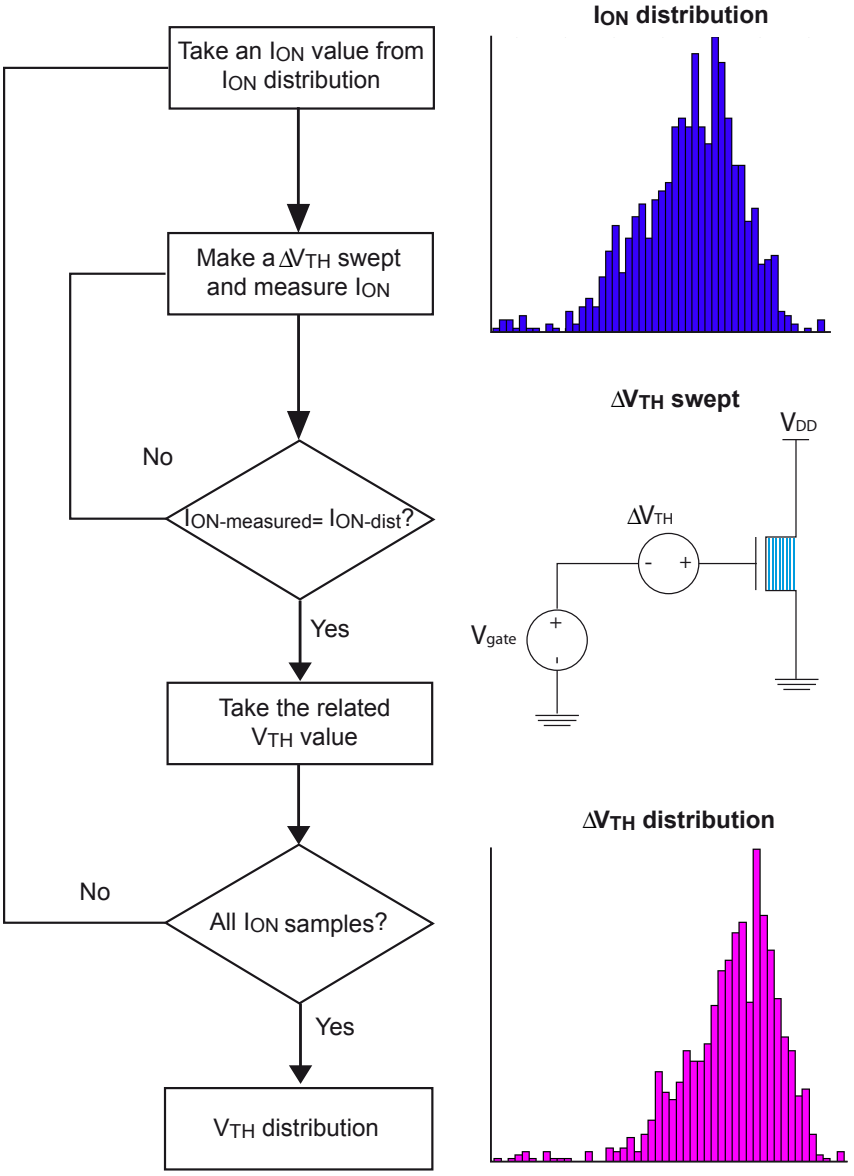


FIGURE 6.10: Flow chart to translate I_{ON} variations into V_{TH} fluctuations.

6.1.3.2 Delay and Noise Margin Variability of a CNFET Inverter

We initially simulate a CNFET inverter using the two possible design styles, correlated and uncorrelated. In correlated style, p- and n-type CNFETs are aligned and then share CNTs, whereas in uncorrelated style p-CNFETs and n-CNFETs contain uncorrelated CNTs since the CNFETs are laid out perpendicular to the direction of CNT growth (Figure 6.11).

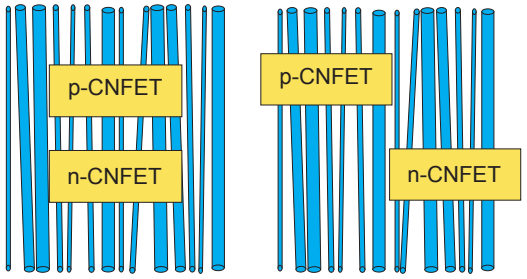


FIGURE 6.11: (a) Correlated CNFETs vs. (b) uncorrelated CNFETs.

Figure 6.12 plots the variation of the output signal and VTC of the simulated CNFET inverter for the case $p_m = 33\%$ (worst case) and for both uncorrelated and correlated design styles (1000 MC). Observe that the variation of rise and fall edges (insets in Figures 6.12(a) and 6.12(b)) is a little bit larger for uncorrelated design. The same occur for the voltage transfer curve; but in this case the difference of VTC variability between the correlated and uncorrelated design is more noticeable.

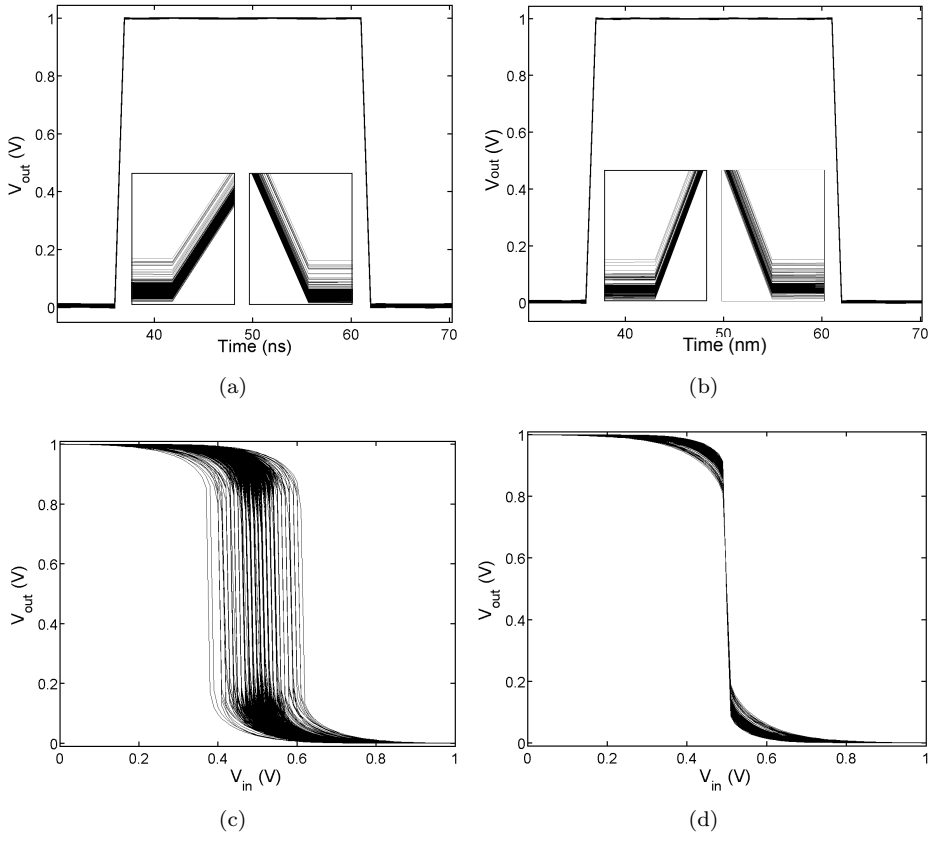


FIGURE 6.12: (a)(b) Output variation and (c)(d) VTC variation of a CNFET inverter in the presence of CNT-specific variations ($p_m = 33\%$) for uncorrelated ((a),(c)) and correlated ((b),(d)) design styles. (Insets) in (a) and (b) are zooms of the variation in rising and falling edges.

Figures 6.13 and 6.14 show the noise margins (NM_H and NM_L) and delay (t_{PLH} and t_{PHL}) variability levels of a CNFET inverter for correlated vs. uncorrelated transistors, respectively. Both the noise margin and the delay fluctuation increases as p_m increases because an increase in m-CNT induced count variations, and present a smaller variability level when a correlated CNFET design is used (red bars), as expected. Focus on NMs, both NM_H and NM_L shows similar variation levels and there is a considerable improvement of noise margin variation using a correlated design ($\sim 3.5\times$ smaller). Regarding the delays, t_{PLH} has bigger variability than t_{PHL}, which means that p-CNFET is more affected by V_{TH} fluctuations. Furthermore, there is a minor enhancement of the delay variation when a correlated design is used.

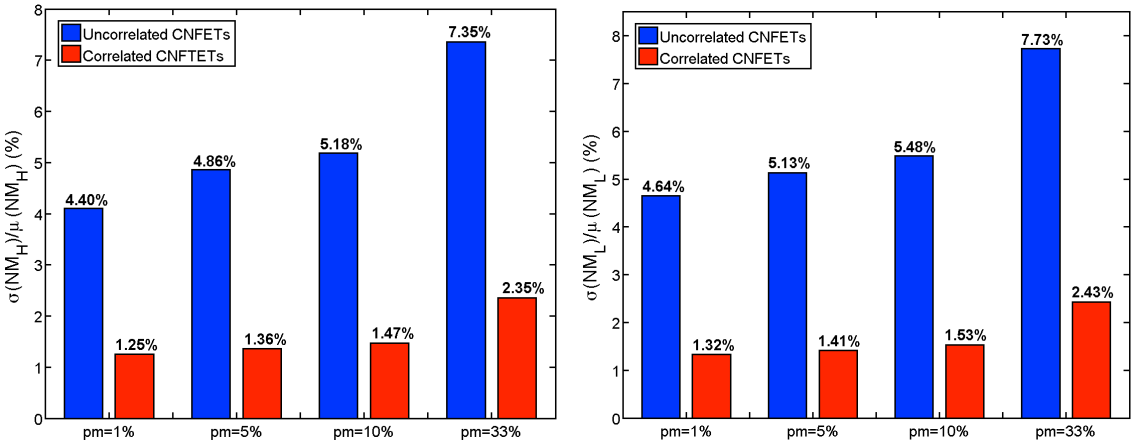


FIGURE 6.13: (a) NM_H and (b) NM_L variability of a CNFET inverter for correlated vs. uncorrelated layout styles and different p_m.

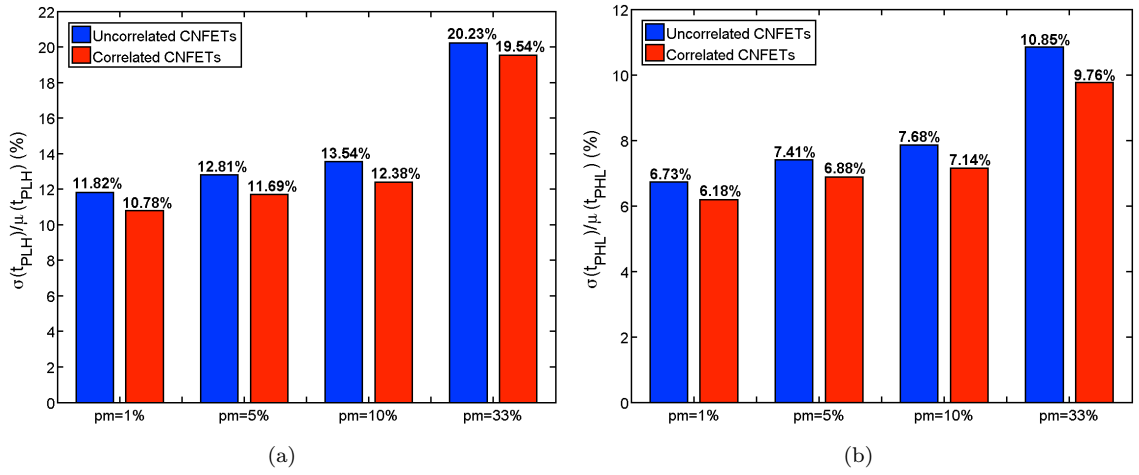


FIGURE 6.14: (a) t_{PLH} and (b) t_{PHL} variability of a CNFET inverter for correlated vs. uncorrelated layout styles and different p_m.

6.1.3.3 Delay Variability of a CNFET Inverter Chain and SNM Variability of a Pair of Cross-Coupled Inverters

In [76] the use of different layout styles with different degrees of CNT correlation is explored as a technique to improve the noise immunity of CNFET circuits. We simulate a five stage CNFET inverter chain and two cross-coupled CNFET inverters and measured the delay propagation and the SNM, respectively. In both cases we consider four possible correlated and uncorrelated styles that were also proposed in [76] (Figure 6.15): 1) *CICT*, Correlated Inverters and Correlated Transistors, has perfect correlation between all CNFETs; 2) *UICT*, Uncorrelated Inverters and Correlated Transistors, has perfect correlation between the p-CNFET and n-CNFET of each inverter, while the CNFETs in the different inverters are uncorrelated; 3) *CIUT*, Correlated Inverters and Uncorrelated Transistors, has perfect correlation between the p-CNFET of one inverter and the p-CNFET of the others inverter and similarly for the n-CNFETs; and 4) *UIUT*, Uncorrelated Inverters and Uncorrelated Transistors, all CNFETs are completely uncorrelated.

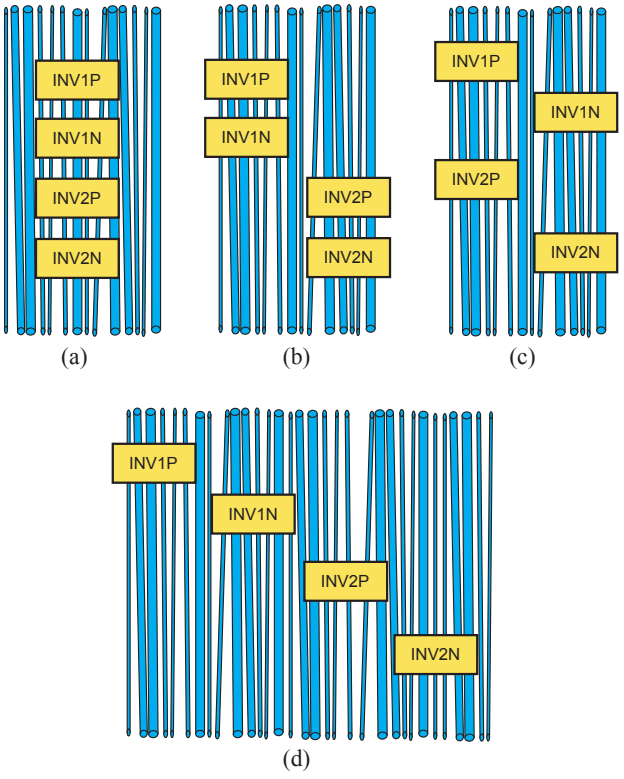


FIGURE 6.15: The four correlated/uncorrelated design styles considered for CNFET inverter chain and cross-coupled inverter. (a) CICT, (b) UICT, (c) CIUT and (d) UIUT.

Figure 6.16 shows the delay variability of a five stage CNFET inverter chain for all 4 design styles inverters and for $p_m = 1\%$ and $p_m = 33\%$ (1000 MC). The delay was measured at the output of the third stage (minimum delay). Firstly, observe that delay variability increases as the percentage of m-CNT removed increases but both cases $p_m = 1\%$ and $p_m = 33\%$ show similar values. It is because of "compensation effects" between the inverters of the chain. Secondly, it should be pointed out that the variation of the delay is quite similar for all 4 possible designs, but the minimum and the maximum delay variability is for CICT and CIUT designs, respectively. In addition, better delay results are obtained when transistors are correlated.

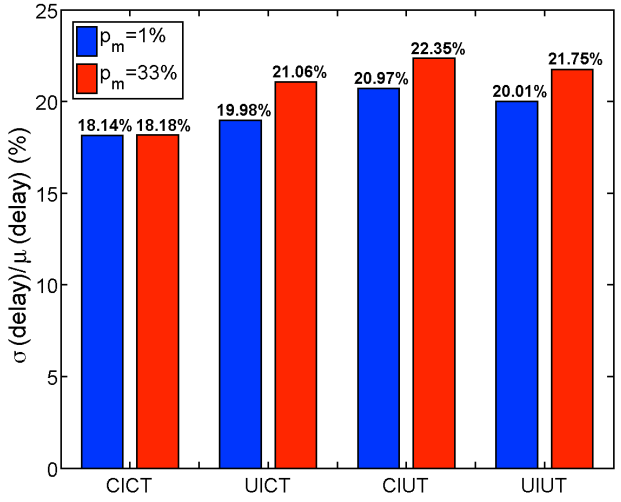


FIGURE 6.16: Delay variation of a 5 stages CNFET inverter for all 4 layout styles and (a) $p_m = 1\%$ and (b) $p_m = 33\%$.

Now, we analyze the impact of CNT-specific variations on the SNM of a pair of a cross-coupled CNFET inverters. Figure 6.17 depicts the variation of the SNM (VTC curves variation) of the simulated cross-coupled CNFET inverter for the case $p_m = 33\%$ and all four layout styles (1000 MC). Obviously, the two VTCs that forms the "butterfly" are identical when inverters are correlated (Figure 6.17(a) (inset) and Figure 6.17(b)), and they are different when inverters are uncorrelated (Figure 6.17(c) (inset) and Figure 6.17(d)). Note that the CICT, CIUT and UICT designs ensure symmetry between the two lobes of the "butterfly", whereas UIUT design causes the anti-symmetry in the VTC curves. It means that CICT, CIUT, and UICT give better SNM values than UIUT design.

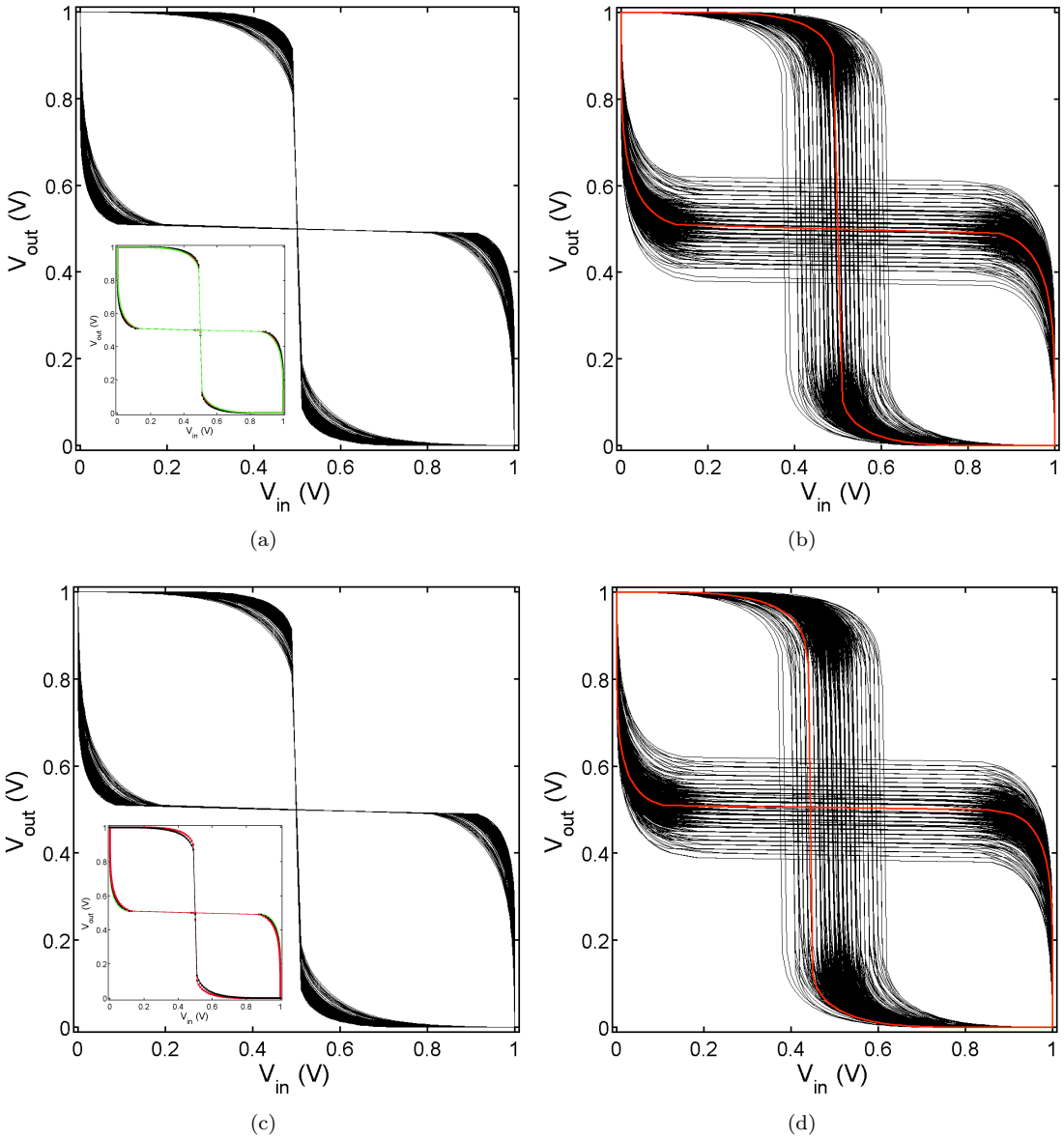


FIGURE 6.17: SNM variation of a pair of cross-coupled CNFET inverters in the presence of CNT-specific variations ($p_m = 33\%$) for (a) CICT, (b) CIUT, (c)UICT and (d) UIUT design styles.

Figure 6.18 shows the variability level of the SNM for all 4 design styles and for $p_m = 1\%$ and $p_m = 33\%$. The variation of SNM is higher for $p_m = 33\%$ than for $p_m = 1\%$, as expected. Regarding the layout designs, the best design option to reduce the SNM variability is uncorrelated inverters and correlated CNFETs (UICT); followed by CIUT and CICT designs that show similar variation levels because of the correlation of the inverters. Finally, UIUT presents the maximum SNM variability.

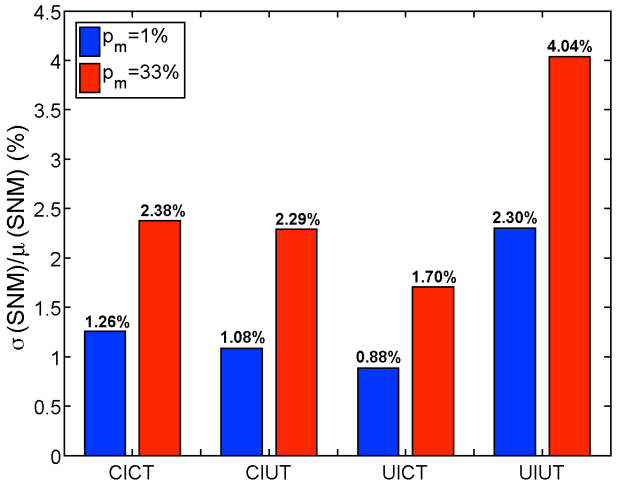


FIGURE 6.18: SNM variability of a pair of a cross-coupled CNFET inverter for all 4 deign styles and $p_m = 1\%$ and $p_m = 33\%$.

6.2 6T SRAM memory

Memories are among the most variability sensitive modules of a processing system. The reason is that most of the transistors in a memory are minimum-sized and are thus more prone to variability. Additionally, memories are dominated by parallel paths (word lines and bit lines), hence timing can be severely degraded by variability due to the dominance of a worst-case path over the rest.

As a part of my collaboration in the european project called TRAMS (Terascale Reliable Adaptive Memory System)[106], we also analyzed the write and read delay variation of a CNFET 6T SRAM cell in the presence of CNT-specific variations. In this Section, we show how CNFET manufacturing imperfections (or related CNT-specific variations) affect the Write and Read Access time of a CNFET 6T SRAM cell. A comparative analysis of CNFET SRAM cell and CMOS SRAM cell is also presented.

6.2.1 Model, Parameters, and Metrics Definition for 6T SRAM Cell

A typical 6T SRAM cell is shown in Figure 6.19. This cell has been implemented using different CMOS technology nodes, 16nm, 22nm and 32nm and, CNFET technology. The width (W, in nm) and length (L, in nm) ratio of each transistor for CMOS technologies are also shown in Figure 6.19 (in red), where T is the Technology parameter and depends on the technology node (its value is technology node/2). For CNFET technology, all transistors have the same size, $W_{gate} = 32nm$ (8 tubes and pitch=4nm) and $L_{ch} = 16nm$,

that is, all of them have the structural and electrical parameters of the nominal CNFET device shown in Chapter 4, Section 4.1. Monte Carlo simulations are performed using Berkeley high-performance Predictive Technology Models (PTM) [107] for 32nm, 22nm and 16nm, and the CNFET model of Stanford University [66]-[69]. We consider parasitic capacitances corresponding to an array of 256 cells. Furthermore, as in the previous case of study, the process variations of CMOS technologies and CNT-specific variations of CNFET technology are studied by induced equivalent threshold voltage variations.

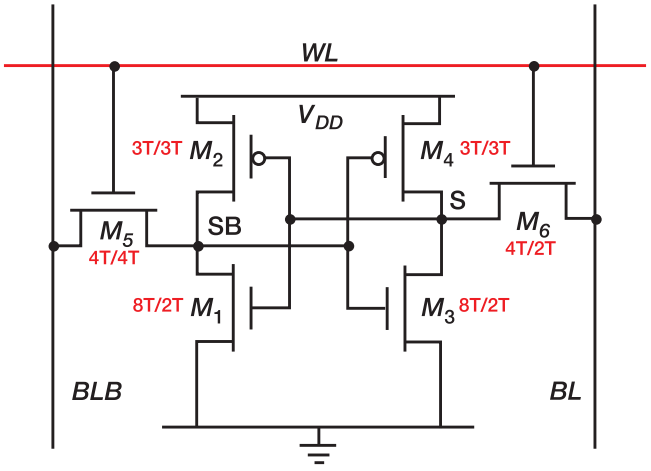


FIGURE 6.19: Schematic of a typical 6T SRAM cell.

Write Access Time (WAT) and Read Access Time (RAT) are two important metrics for assessing the performance of a SRAM cell. In this thesis, the WAT is defined as the time required for changing the cell contents (store node reaches $0.6V_{DD}$ for write '1' or $0.4V_{DD}$ for write '0') after the wordline is turned on (Voltage(WL)=$0.5V_{DD}$). The RAT is defined as the time required for producing a prespecified voltage difference (0.1V) between BL and BLB after the wordline is turned on. This voltage difference is sensed by sense amplifier. Figure 6.20 shows the WAT and the RAT of a 6T SRAM cell for different CMOS technology nodes and CNFET technology. As can be observed both times decrease as the technology node decreases for CMOS technology. CNFET technology shows the least WAT (7.77ps) and RAT (57.42ps).

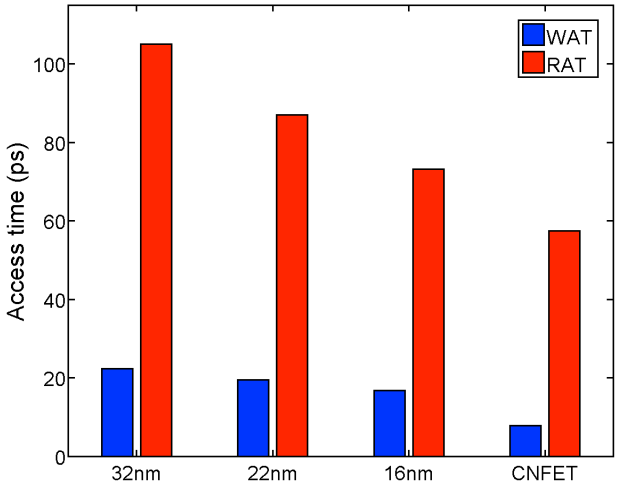


FIGURE 6.20: WAT and RAT of a 6T SRAM cell for different CMOS technologies node and CNFET technology.

6.2.2 WAT and RAT Variations: Simulation Results

As mentioned in the previous Section, the process variations of CMOS technologies and CNT-specific variations of CNFET technology are studied by induced threshold voltage variations. For CMOS technology we take into account the scenarios shown in Table 6.1, moderated (m), high (h) and very high (vh).

TABLE 6.1: V_{TH} variability scenarios in 6T SRAM cell

Technology	**Scenario**	V_{TH} **variation (min. size)**	V_{TH} **variation (normalized)**
32nm	moderated	6%	4.24%
	high	15%	10.61%
22nm	moderated	8%	5.66%
	high	15%	10.61%
	very high	30%	21.21%
16nm	moderated	10%	7.07%
	high	20%	14.14%
	very high	40%	28.28%
CNFET	high	-	16.63%

In column 3 the percentage of V_{TH} variation ($100 \times \sigma/\mu$) for minimum transistor size is shown; in order to adapt it to our transistor size, we have corrected these values with $percentage/\sqrt{WL}$. Final values of V_{TH} variability used in this thesis are shown in column 4. For CNFET we consider 16.63% of V_{TH} variation. This value has been obtained from the mean and the standard deviation of the dV_{TH} shown in Figure 6.9

for $p_m = 33\%$. We also analyze the impact of these variations for three different temperatures: 25 °C, 60 °C and 100 °C.

Figure 6.21 depicts the variability of both WAT and RAT of a 6T SRAM cell implemented using different CMOS technology nodes under different variability scenarios and CNFET technology for temperatures of 25 °C and 100 °C.

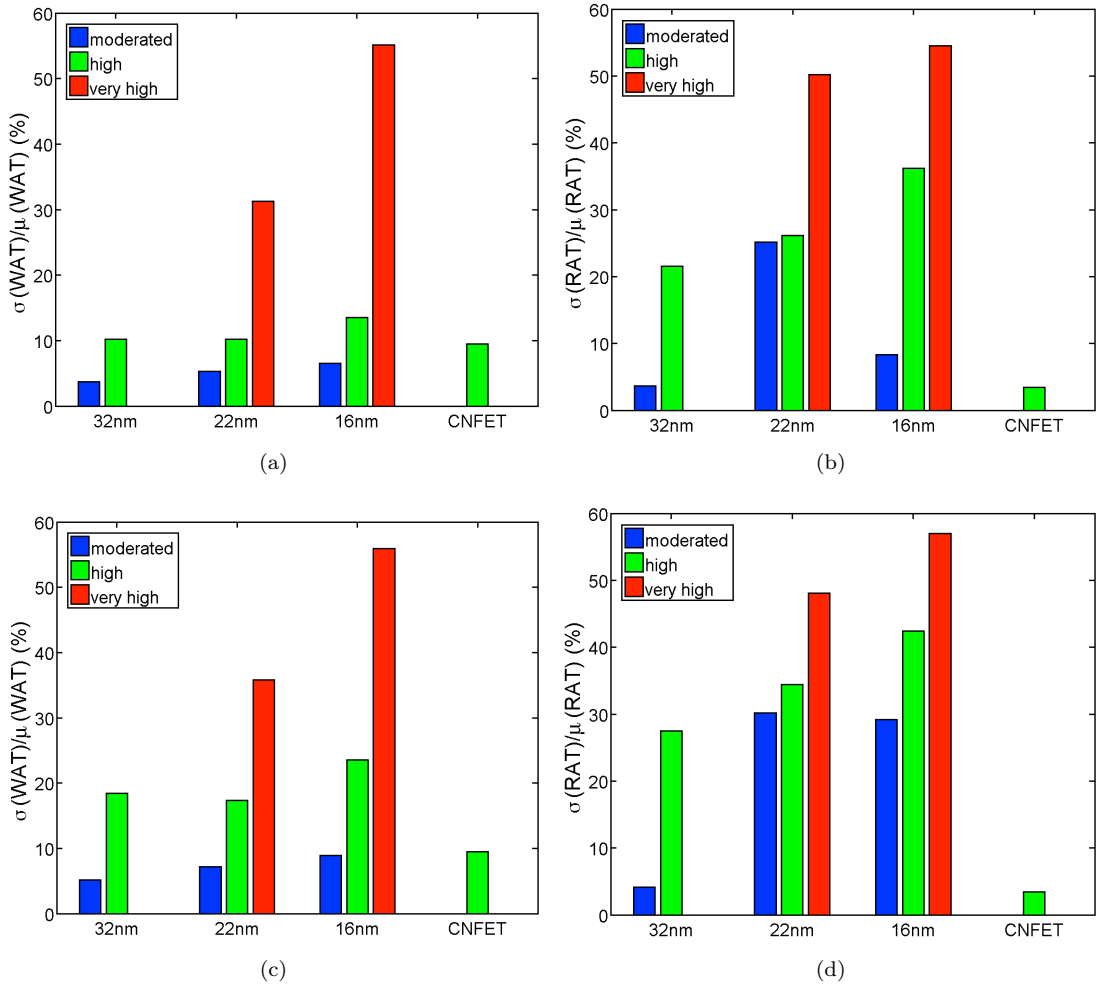


FIGURE 6.21: (a)(c) WAT and (b)(d) RAT variation of a 6T SRAM cell implemented with different technologies and for different variability scenarios and temperatures of (a)(b) 25 °C and (c)(d) 100 °C.

Observe that in general for CMOS technologies the variability of both times increases as the technology size decreases. Obviously, the worse the scenario, the higher the percentage of variation. Focusing on temperature, the variability increases as the temperature increases. Regarding CNFET technology, variability for WAT (9.50%) is similar to 16nm in a moderated scenario and 100 °C (8.89%), whereas variability in RAT (3.44%) is really close to 32nm in a moderated scenario and 25 °C (3.62%). Note that temperature

has a minor impact on WAT and RAT in CNFET technology (these values are kept for the three temperatures) due to the high thermal stability of CNFETs [108], [109].

It is worth noting that m-CNT specific variations and process variations in CNFET and CMOS technologies, respectively may result in write and read (W/R) delay faults because an excessive time and flipping faults in which the value stored in the cell is lost. The percentage of total W/R faults that includes both W/R delay and flipping faults are shown in Table 6.2. As expected for CMOS technology, the percentage of both W/R faults increases as the scenario gets worse, as the temperature increases and as the technology size decreases. In Write faults, the maximum percentage of total faults is to 16nm, 100 °C and a very high variability scenario (47%). The same occurs in Read faults in which the maximum percentage of total faults is 46.2%. Finally, the percentage of W/R faults for CNFET technology is 0 (no faults) for all temperatures.

TABLE 6.2: Variability in Write Access time and Read Access time and percentage of W/R faults

	Tech.	**32nm**		**22nm**			**16nm**			**CNFET**
	Scenario	**m**	**h**	**m**	**h**	**vh**	**m**	**h**	**vh**	**16.58%**
Write faults %	25 °C	0	0	0	0.4	11	1.2	11.6	30.4	0
	60 °C	0	0.2	0	1.2	17	5.6	20.2	40	0
	100 °C	0	1	0	3.2	23.4	12.2	26.6	47	0
Read faults %	25 °C	0	0.8	0.2	2.8	19.4	1.8	14.2	34.6	0
	60 °C	0	1.8	0.2	4.4	24.8	5.6	22.4	42.4	0
	100 °C	0	3.4	0.2	7.6	31.8	14.2	29	46.2	0

6.3 Summary and Conclusions

In this Chapter a detailed variability analysis of CNFET logic circuits in the presence of CNT-specific variations was presented. Important results, conclusions and contributions are summarized in the following.

In the first Section, the impact of CNT-specific variations on a CNFET inverter (chain) and two cross-coupled CNFET inverters is analyzed. For this purpose, important metrics of logic circuits, such as delay, figure of merit of logic speed, and noise margin, figure of merit of robustness, are evaluated.

Firstly, the behavior of delay in the presence of only CNT density variations is analyzed. The delay is closely linked to drive current, it is inversely proportional to I_{ON}; then it is mainly affected by CNT density variations and also by m-CNT induced variations if a m-CNT removal process is applied, because they are the most prominent sources of drive current (I_{ON}) fluctuations. The delay of a CNFET inverter with a fixed gate widths initially improves as the number of CNTs/CNFET increases because of the increased total drive current due to the increased number of CNTs. The delay subsequently worsens due to the reduced drive current per CNT as a result of increased inter-CNT electrostatic image charge screening effects. This means that for each gate width, there is an optimum number of CNTs/CNFET that maximizes the drive current and then minimizes the delay (e.g. the optimum number of CNTs/CNFET is $N_{opt} = 3$ for a $W_{gate} = 16nm$).

Then, the effect that all CNT-specific variations have on CNFET circuits is evaluated by induced threshold voltage fluctuations. For this reason, we develop and present a methodology to translate the drive current variations of a CNFET device, caused by density variations, diameter, doping, and alignment variations and m-CNT induced variations due to the application of an ideal m-CNT removal process, into V_{TH} fluctuations. How these V_{TH} variations affect the delay and noise margin of a CNFET inverter is analyzed for two design styles, correlated and uncorrelated CNFETs, and for different initial proportions of m-CNTs. Both the noise margin and the delay fluctuation increases as the proportion of m-CNT, which are subsequently removed, increases; in other words, their variability grow as CNT count variations increases. Delay is more affected by CNT-specific variations than noise margins, reaching values as high as 20% for the worst case ($p_m = 33\%$ and uncorrelated CNFETs). Furthermore, we show that the variability of NMs and delay can be reduced using correlation between p-CNFET and n-CNFET, but this variability enhancement is more considerable for noise margin.

Secondly, the variability that CNT-specific variations cause on propagation delay of a five stages CNFET inverter chain and on static noise margin of a pair of cross-coupled CNFET inverters is analyzed. In this both cases, different p_m are considered and also four design styles are implemented: *CICT*, Correlated Inverters and Correlated Transistors; 2) *UICT*, Uncorrelated Inverters and Correlated Transistors; 3) *CIUT*, Correlated Inverters and Uncorrelated Transistors; and 4) *UIUT*, Uncorrelated Inverters and Uncorrelated Transistors. Focus on delay, it shows similar variation values for $p_m = 1\%$ and

$p_m = 33\%$, because there is a "compensation effect" between the inverters of the chain. In addition, its variability is similar for all four designs considered (between $18\% - 22\%$), even though designs in which transistors are correlated, CICT and UICT, give the smallest delay variation. Regarding the SNM, its variability increases as p_m increases, but it is minor than delay. It is worth noting that those designs that ensure symmetry between the two lobes of the"butterfly" (CICT, CIUT and UICT), give better SNM values than those that causes anti-symmetry in the VTC curves (UIUT). Moreover, the best and the worst design option to reduce the SNM variability is uncorrelated inverters and correlated transistors (UICT), and uncorrelated inverters and uncorrelated transistors (UIUT).

Finally, the write and read delay variation of a CNFET 6T SRAM cell in the presence of CNT-specific variations is analyzed and compared with the delay variability of a MOSFET 6T SRAM cell affected by process variations. Different variability scenarios for Si-bulk technology (moderate, high and very high) and temperatures (25 °C, 60 °C and 100 °C) are considered. The variability 6T SRAM cell analysis shows as a promising prospect, that even for todays CNFETs performance, the variability in CNFET cell is comparable with that of Si-MOS cells in the most favorable scenario (moderated). Moreover, CNFET memory cell is not affected by temperature variations because the high thermal stability of CNFETs and it is able to work correctly (no faults) even though the presence of manufacturing imperfections.

To conclude, CNT-specific variations, and mainly CNT density variations and m-CNT induced variations caused by an ideal m-CNT removal process, lead to CNFET circuit performance degradation in terms of speed and robustness. They have a major impact on delay propagation, because its strong dependence on drive current, than on noise margin; as we will see in the next Chapter, the main cause of noise margin variations and degradation is the presence of m-CNTs. But note that, the correlation between transistors can be used as a technique to reduce the variability of both delay and noise margin.

Chapter 7

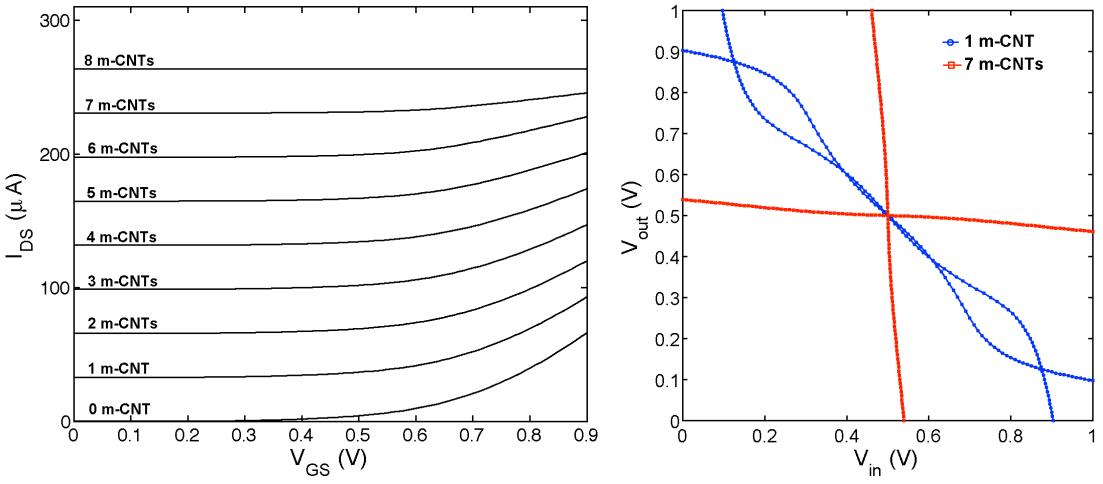
Reliability of CNFET Circuits

Metallic CNTs are the major concern in CNFET manufacturing process from the point of view of reliability. Their presence in CNFETs cause short defects and their elimination after the CNT growth may cause an open defect together with the impact of variability in the drop of performance. For a growth process that yields uniformly distributed chiralities, one-third of CNTs will be metallic and two-thirds will be semiconducting. As we have seen in Chapter 3 several techniques and methods have been proposed to improve the percentage of s-CNTs such as enhanced CNT growth methods, CNT self-sorting techniques and m-CNT removal processes. However, none of these solutions has yet demonstrated sufficient robustness and scalability to be used in practical circuit applications.

In this Chapter, the impact of the presence of m-CNT on CNFET logic circuits is analyzed and alternative methods (different from m-CNT sorting or elimination) to deal with metallic CNTs are proposed. The organization of the chapter is as follows. In Section 7.1 the effect that m-CNTs have on CNFET devices and circuits is shown. In Sections 7.2 and 7.3 alternative solutions to the m-CNT problem are presented. First, a design methodology that uses asymmetrically correlated CNTs to create CNFETs that are tolerant to metallic CNTs is reviewed. Then, the use of fault-tolerant architectures is proposed as a technique to improve CNFET circuits reliability [110]. Finally, in Section 7.4, our results are summarized and concluding remarks are made.

7.1 Impact of the Presence of m-CNTs in CNFET Devices and Circuits

Depending on the chiriality of the CNT, it can either be metallic or semiconducting. Metallic CNTs can not be used to make CNFETs because their high conductivity makes it impossible to control the current with the gate; that is, they behave like metallic wires. A CNFET made entirely from m-CNTs will have a current that is only dependent on the drain-source voltage, not on the gate voltage, whereas CNFETs that consist of a mix of m-CNTS and s-CNTs can still show a I-V transistor characteristic but present an extremely low ON-OFF current ratio as shown in Figure 7.1(a) (e.g. the ON-OFF current ratio of a 8-tube CNFET that only consists of s-CNTs is 1×10^6, whereas the current ratio of a 8-tube CNFET that has 1 m-CNT and 7 s-CNTs is 2.83). Then, using such CNFETs to construct an inverter, the inverter will have very little swing and no noise margin (Figure 7.1(b)).



(a) (b)

FIGURE 7.1: (a) $I_{DS} - V_{GS}$ curve of a 8-tube n-type CNFET ($V_{DS} = 0.9V$) with different proportions of m-CNTs (1-8 m-CNTs).(b) Simulated VTC of a two cross-coupled CNFET inverters whose transistors are composed by 8 CNTs and for different proportions of m-CNTs.

Furthermore, as we have seen in Chapter 5, the presence of m-CNTs in the transistor may cause *Drain Source Hard Short* (all CNTs are metallic) or *Drain Source Soft Short* (a mix of m-CNTs and s-CNTs) resulting in stuck-on fault and partial stuck-on fault, respectively. These faults may lead to logic failures (incorrect operation) in CNFET digital circuits as we will demonstrate in the next Sections.

There are many ongoing endeavors toward solving the metallic-CNT issue, and almost all focus on introducing a new process to the CNFET fabrication procedure that will eliminate or breakdown the metallic CNTs, leaving only the semiconducting CNTs behind for device fabrication. As mentioned in Chapter 4, these processes includes CNT self-sorting techniques, selective etching of m-CNTs, and electrical burning of m-CNTs. However, all of them present several issues and challenges that must be solved before they can be used in practical circuits applications. Then, alternative and/or supplementary solutions to the "metallic CNT problem" must be proposed.

In the following Sections we will review and propose different techniques to improve the reliability of CNFET circuits in the presence of undesired m-CNTs.

7.2 Yield Improvement of CNFET Circuits: Correlation of CNFETs

As we have mentioned in the previous Chapter, correlation between CNFETs and/or logic gates can be used as a method to reduce the CNFET circuit variability and improve their robustness and speed. But such correlation between CNFETs can be also used as a design technique to create CNFETs that are tolerant to m-CNTs, and then to improve even more the yield of CNFET circuits. In [86] a metallic-CNT-tolerant design methodology called ACCNT was presented. It uses asymmetrically correlated CNTs to allow proper functionality of CNFETs and CNT circuits, despite the presence of metallic CNTs. In other words, the ACCNT design strategically employs correlated redundancies; it connects statistically independent/uncorrelated CNFETs in series and statistically correlated CNFETs in parallel. In addition, in doing so, it achieves both metallic-CNT tolerance and high current drive; Figure 7.2 summarizes the ACCNT design.

However, this m-CNT tolerant methodology design still presents two important challenges that need to be investigated:

- ACCNT uses asymmetric correlations to achieve metallic-CNT tolerance, but in reality, the correlations will never be ideal. Nonideal correlations may slightly

diminish the effectiveness of ACCNT, and then it will be important to investigate the impact of them.

- ACCNT trades area to achieve metallic-CNT tolerance. That is, its implementation results in a overhead of area.

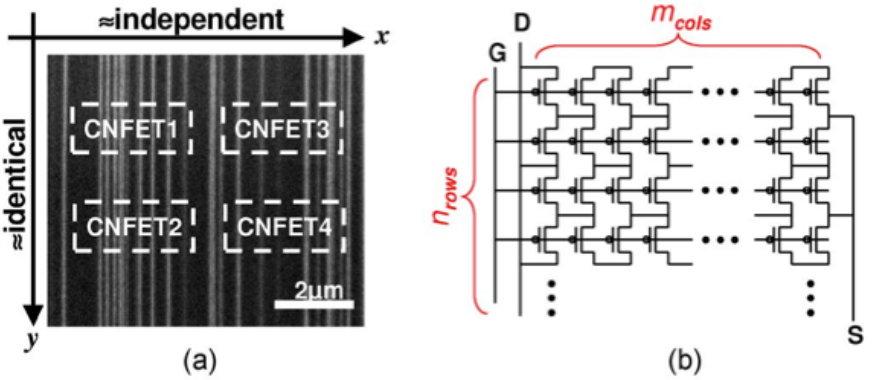


FIGURE 7.2: Summary of ACCNT [86]. (a) ACCNT uses asymmetric correlations present in aligned arrays of CNTs. (b) By connecting independent CNFETS in series, ACCNT achieves m-CNT tolerance. By connecting identical CNFETs in parallel, ACCNT achieves high current drive without compromising m-CNT tolerance.

In [87] the ACCNT tradeoffs and optimizations were analyzed. Although ACCNT was initially proposed as a alternative technique to metallic removal or breakdown solutions [86], in [87] it is concluded that ACCNT must be used in conjunction with other metallic-CNT mitigation solutions, such as CNT sorting, selective etching, and electrical burning, because its area cost is too large for the current p_m. Only once the semiconducting-CNT percentage is improved to 99.9%, ACCNT will offer a solution to significantly reduce the "metallic-CNT-induced yield loss". Furthermore, it was also demonstrated that the ACCNT area costs can significantly be reduced by optimizing the ACCNT design; they found that ACCNT can improve the chip yield of a one-million transistor chip from 0% (that using a conventional design) to 99% with an area overhead of about 3.3×.

It is worth noting that this design methodology based on correlation is similar to layout techniques used in analog circuits, such as interdigitated layout and common centroid layout. They use "matched devices" to reduce the effect of possible variations [111].

7.3 Yield Improvement of CNFET Circuits: Fault Tolerant Architecture

In this Section we propose and analyze the use of a fault-tolerant architecture as a possible solution to mitigate the "m-CNT problem" and then as possible technique to improve the yield of CNFET circuits in the presence of metallic CNTs.

7.3.1 Fault-Tolerant Architectures

The well-known approach for developing fault-tolerant architectures in the face of uncertainties (both permanent and transient faults) consists of incorporating redundancy [110]. Redundancy can be either static (in space, time, or information) or dynamic (requiring fault detection, location, containment, and recovery):

- Static redundancy techniques, also called masking or massive redundancy techniques, in which fault tolerance is implemented into the system structure and is therefore inherent to the operation of the system. They are able to mask all types of faults (permanent and transient) and can be classified into three categories: hardware, time, and information redundancy techniques.
- Dynamic redundancy techniques, also called selective, stand-by or sparing redundancy techniques, are based on fault detection, location, containment, and recovery. These techniques are not useful for transient faults because they need significant amount of time to detect a fault and activate the corresponding circuitry to perform the corrective action. The main benefit of dynamic redundancy is higher reliability for permanent and multiple faults and lower overhead than static techniques.

In this thesis, we focus on hardware redundancy techniques. Hardware redundancy generally means replicating the functional processing module and providing a voting circuit (also called voter) to decide the correct output value based on redundant module outputs (Figure 7.3). When a redundant component fails, the voter can decide the correct output based on the results of other redundant modules. The basic principle can be used at many different abstraction levels; the modules can be not only as simple as

single gates but also as complex as whole processors or even larger constructions. The voter can be a simple bitwise hardware implementation or software algorithm running on a processor.

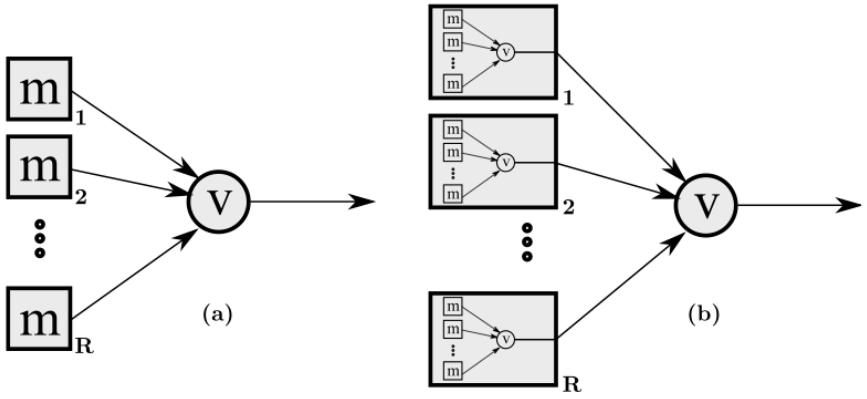


FIGURE 7.3: (a) R-fold Modular Redundancy (RMR); and (b) Cascaded R-fold Modular Redundancy (CRMR) schematic.

Note that the whole system reliability highly depends on the performance of the voter, and therefore, there is a great interest in their design. Two well-known voters are the majority gate and the averaging cell (Figure 7.4). The majority gate (MAJ), was first introduced by Von Neumann [110]. It outputs the logic value carried by the majority of its inputs. The number of inputs per MAJ may vary, but should always be an odd number in order to avoid ties (R = 3, 5, 7,...). The Averaging Cell (AVG), graphically depicted in Figure 3.8, is an analog approach to the majority voting. While the MAJ operates in the digital domain, the AVG performs a weighted average of the replicated inputs in the analog domain, thus is potentially more robust. The AVG stems from the perceptron, the McCulloch-Pitts neuron model [112], [113] and it is widely known for its application in the four-layer reliable hardware architecture (4LRA) [114].

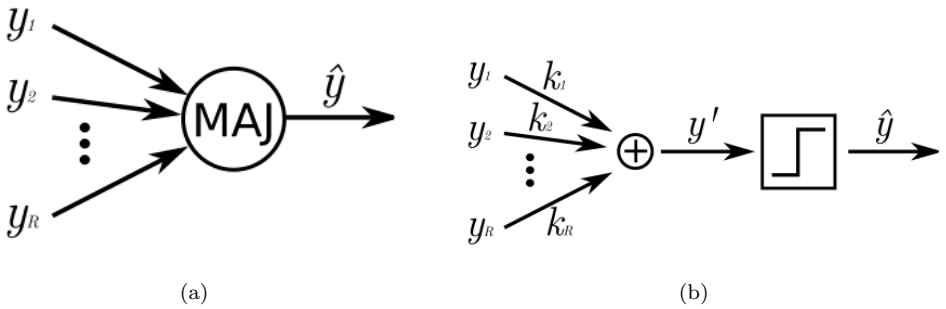


FIGURE 7.4: (a) Majority Gate (MAJ) and (b) Averaging Cell (AVG) schematic.

As mentioned at the beginning of the Section, we investigate the implementation of a fault-tolerant hardware architecture as a mechanism to deal with m-CNTs. For this purpose, we decide to use the four-layer fault-tolerant hardware architecture proposed in [115]. Figure 7.5 shows the four-layer reliable architecture (4LRA). It consists of four layers in which data are strictly processed in a feed-forward manner. The first layer (LY1) is denoted as the input layer, accepting conventional Boolean (binary) signal levels. The core operation is performed in the second layer (LY2), which consists of a number of identical, redundant units each implementing the desired logic function. The fault immunity increases with the number of redundant units, yet the operation is quite different from the classical majority-based redundancy. The third layer (LY3) receives the outputs of the redundant logic units in the second layer, creating a weighted average with rescaling to match the full range of signals (e.g., in the voltage domain). Note that the output of the third layer becomes a multiple-valued logic level. Finally, the fourth layer (LY4) is the decision layer where a binary output value is extracted using a simple threshold function.

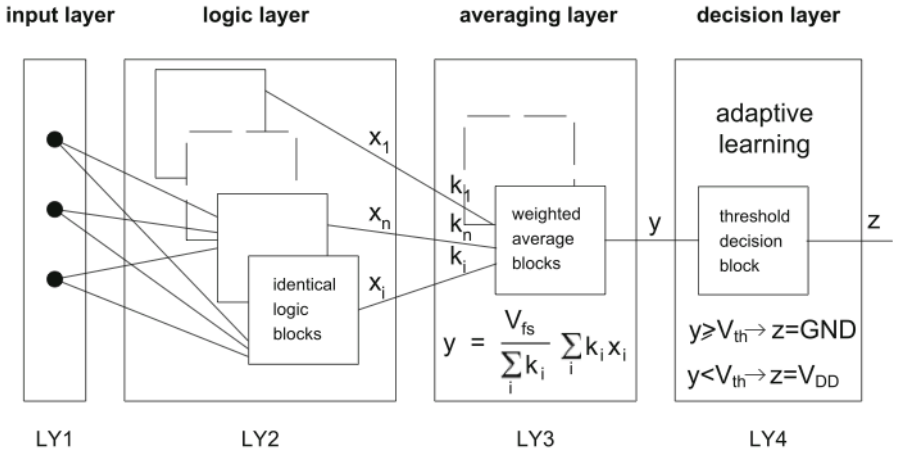
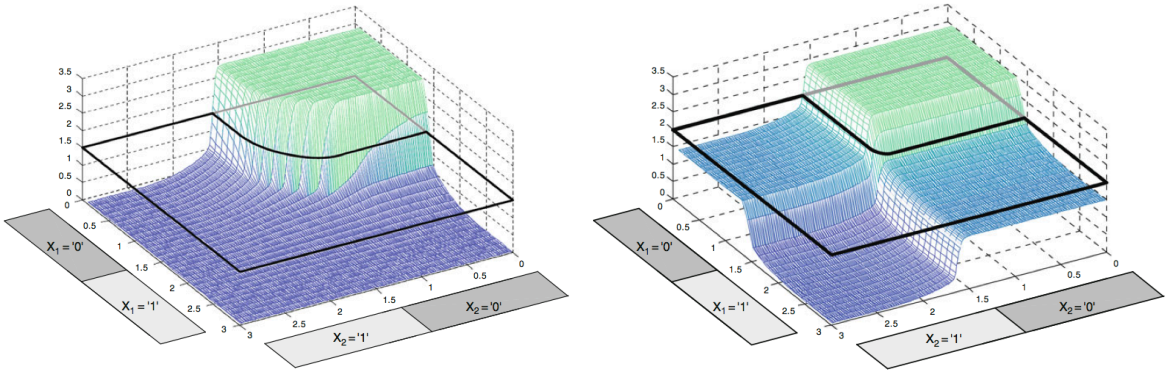


FIGURE 7.5: The fault-tolerant architecture based on multiple layers [115].

As as example of how the 4LRA works, Figure 7.6 shows the output transfer function generated by the averaging layer along with the decision threshold (black line). When there are not device failures, the transfer function surface generated at the output of the averaging block clearly reproduces the expected 2-input NOR function (Figure 7.6(a)). If some device failures in second-layer logic blocks are assumed (Figure 7.6(b)), the output transfer function generated by LY3 does not match what is shown in Figure 7.6(a). But, the correct output behavior can be extracted by setting the decision threshold level as shown.



(a) (b)

FIGURE 7.6: Output transfer function generated by the averaging layer (output of the third layer) of the 2-input NOR circuit with two redundant units, (a) assuming no device failures and (b) assuming some device failures in second-layer logic blocks [115].

Once the operation of the 4LRA have been explained, the main characteristics of this fault-tolerant approach must be pointed out:

1. The 4LRA does not require a high number of replicas to enable correct circuit operation (e.g. it has probability of correct operation of 90% when the probability of transistor fault is 25% with only 2 redundant units [115]).

2. The 4LRA always enables correct circuit operation if at least one replica works correctly. It is worth noting that it could also make possible correct circuit operation even though all replicas have faults, but just in case the faults are placed in different transistors in each replica. That is, assuming a redundancy of three (three replicas) and three faults, the 4LRA will not be able to recover a situation where the each of the three faults causes malfunction of the transistor that is in the same location in each replica. However, if the faults are distributed among transistors then a chance exists that the function may be recovered. Finally, if at least one replica works properly, then the correct operation should be recovered by the 4LRA.

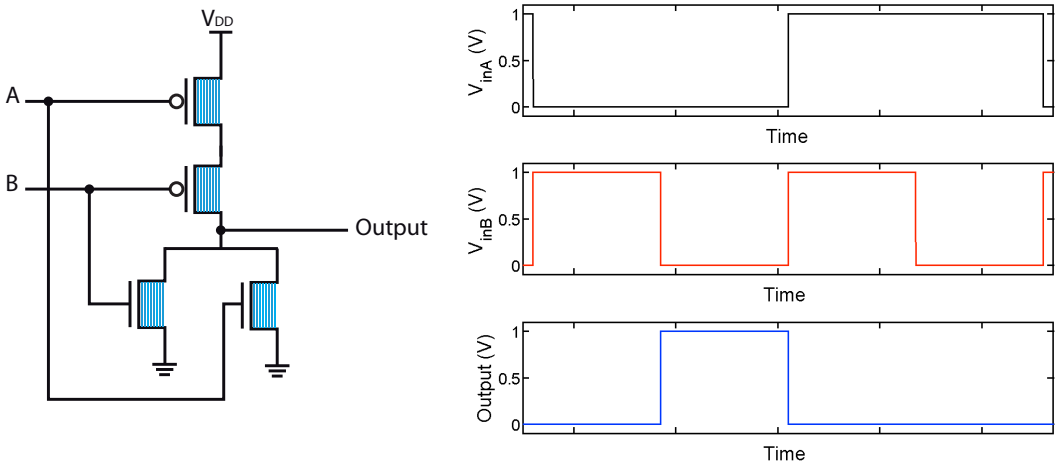
3. The performance of 4LRA can be improved by using an adaptable decision threshold.

7.3.2 Analysis of CNFET Digital Circuits in the Presence of m-CNTs

In this Section we will analyze the impact of m-CNTs (when they are not removed) on the reliability of CNFET digital circuits and the use of the 4LRA system as a mechanism to enhance their yield. For this purpose, we first implement a CNFET NOR gate and then a CNFET 1-bit full adder. In both circuits, we use the nominal device described in Chapter 4, Section 4.1, but assuming that $p_m \neq 0$; that is, all CNFETs will be composed by 8 CNTs that are a mixture of s-CNTs and m-CNTs. In addition, all CNFETs are uncorrelated but have the same p_m because they are placed in the same CNT growth sample.

7.3.2.1 CNFET NOR Gate

Figure 7.7 depicts the transistor level diagram of a CNFET NOR gate, whose transistors only have s-CNTs and its transient response.

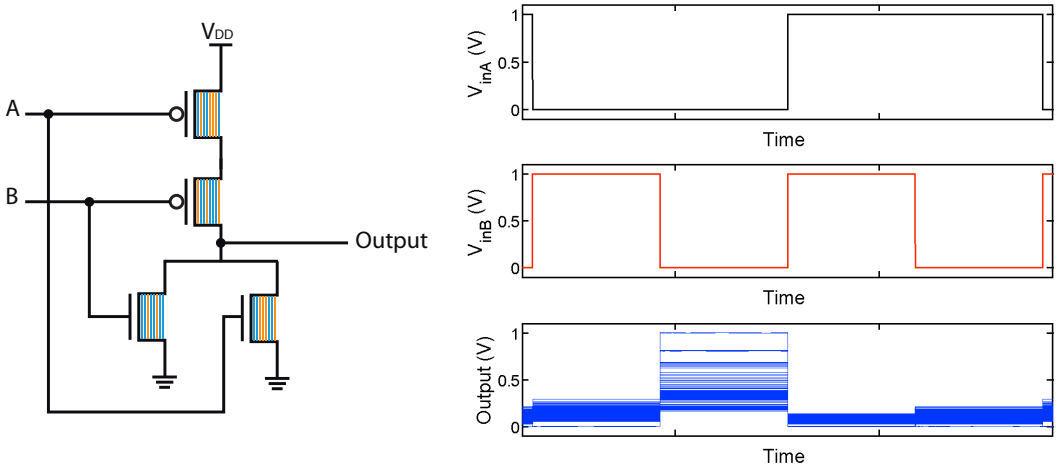


(a) (b)

FIGURE 7.7: (a) Transistor level schematic of a NOR gate, whose CNFETs only have s-CNTs. (b) Transient response of a CNFET NOR gate without m-CNTs.

Figure 7.8(a) shows the transistor level diagram of a CNFET NOR gate, whose transistors are composed by a mix of s-CNTs and m-CNTs. We performed 1000 Monte Carlo simulations of a NOR gate for different m-CNT probabilities because it is important to analyze the failure pattern before applying a fault-tolerant architecture. Figure 7.8(b) shows the output voltage of a NOR gate for all four possible input combinations ('00', '01', '10', and '11') and when all transistors have an m-CNT probability of 33% (worst

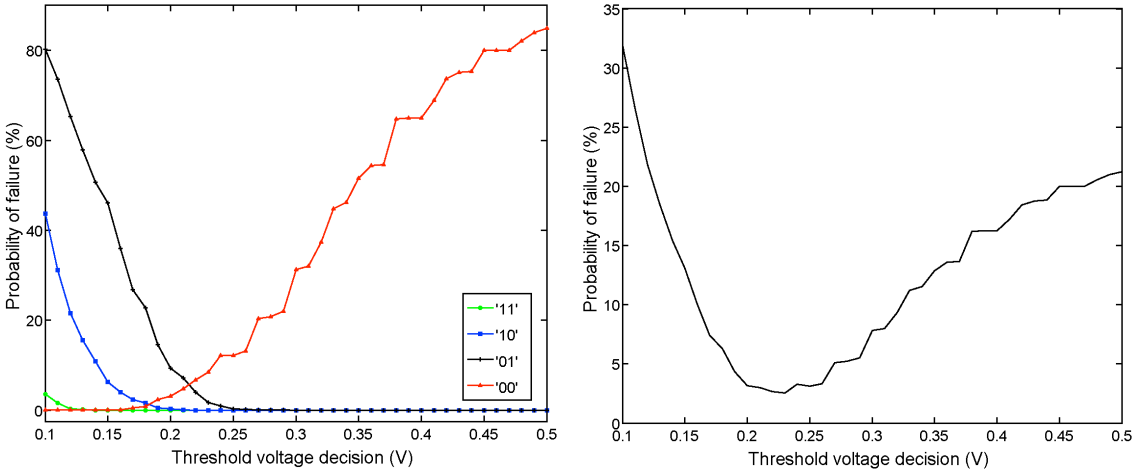
case considered). Note that there is a fluctuation of the output voltage for all input combinations, but no stuck-at zero or stuck-at one faults are observed. So, in this particular case the reliability of a NOR gate could be improved just using a threshold decision block at the output of the NOR gate block. That is, the averaging layer (LY3 in Figure 7.5) would not be required.



(a) (b)

FIGURE 7.8: (a) Transistor level schematic of a NOR gate, whose CNFETs have both s-CNTs and m-CNTs. (b) Transient response of a CNFET NOR gate with m-CNTs ($p_m = 33\%$).

It is worth noting that in case that a threshold decision block is used as a fault-tolerant technique, the reliability of the circuit strongly depends on such threshold voltage decision (V_{thD}). Figure 7.9(a) shows the probability of failure of a NOR gate with $p_m = 33\%$ in function of the threshold voltage decision for each possible input combination. It can be seen that the probability of NOR failure for inputs '11', '10' and '01', whose expected output is '0', decreases as the V_{thD} increases and it becomes zero from a particular V_{thD} level- e.g. the probability of failure of the NOR gate is zero from $V_{thD} = 0.3V$ when the input is '01'-. On the contrary, the probability of NOR failure for input '00', whose expected output is '1', increases as V_{thD} becomes higher. Note that this is the input combination resulting in more failures. Figure 7.9(b) shows the probability of failure of a NOR gate with $p_m = 33\%$ in function of the threshold voltage decision for all four possible input combinations. In this particular case, the threshold voltage level that minimizes the probability of NOR gate failure and then maximizes its yield is $V_{thD} = 0.23V$; using this V_{thD} its probability of failure is 2.55%.

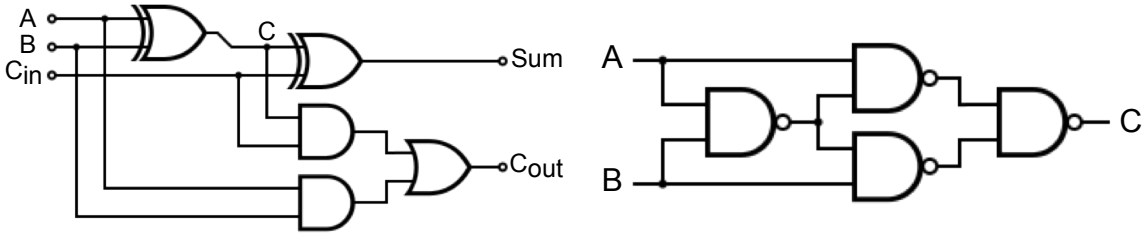


(a) (b)

FIGURE 7.9: (a) Probability of failure of a NOR gate with $p_m = 33\%$ vs. the threshold voltage decision for each possible input combination (1000 MC). (b) Probability of failure of a NOR gate with $p_m = 33\%$ vs. the threshold voltage for all possible input combinations (4000 MC). All input combinations are equiprobable.

7.3.2.2 CNFET 1-bit Full Adder

The gate level schematic of a 1-bit full adder is depicted in Figure 7.10. The XOR gate was implemented using NAND gates as shown in Figure 7.10(b). The transient responses of a CNFET 1-bit full adder whose transistors do not have m-CNTs and whose transistors have a mixture of m-CNTs and s-CNTs, are illustrated in Figure 7.11 and 7.12, respectively. It is worth noting the presence of stuck-at 1, stuck-at 0, and stuck-at intermediate voltage levels faults at both sum and carry outputs (Figure 7.12). Then, in this particular case of a 1-bit full adder, the implementation of the complete 4LRA system could be used as a technique to improve its yield.



(a) (b)

FIGURE 7.10: (a) Gate level schematic of a 1-bit full adder. (b) XOR gate implemented using NAND gates.

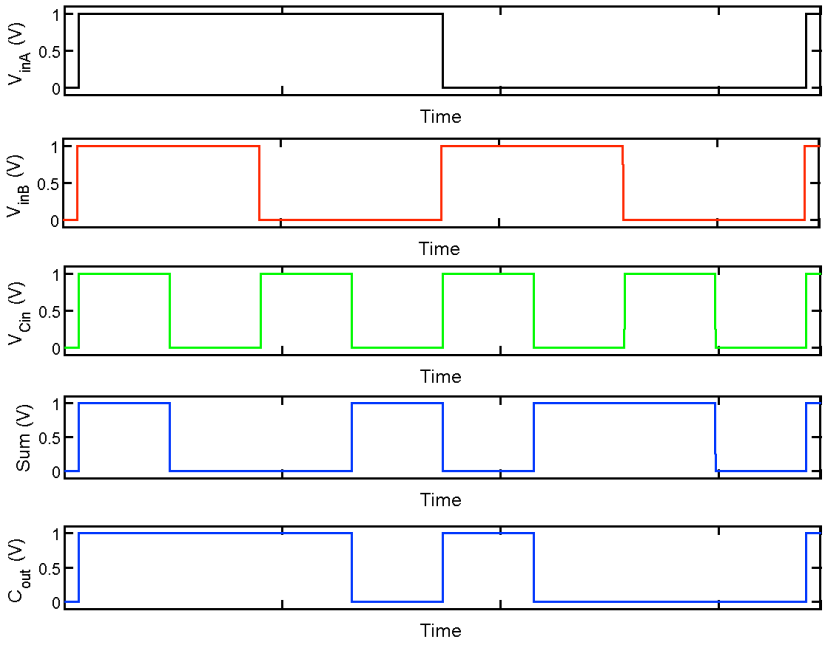


FIGURE 7.11: Transient response of a 1-bit full adder, whose CNFETs are only composed by s-CNTs.

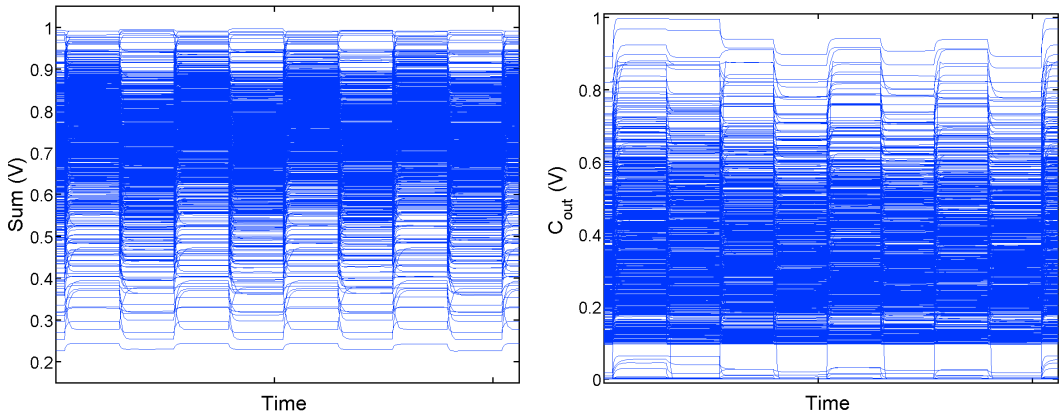
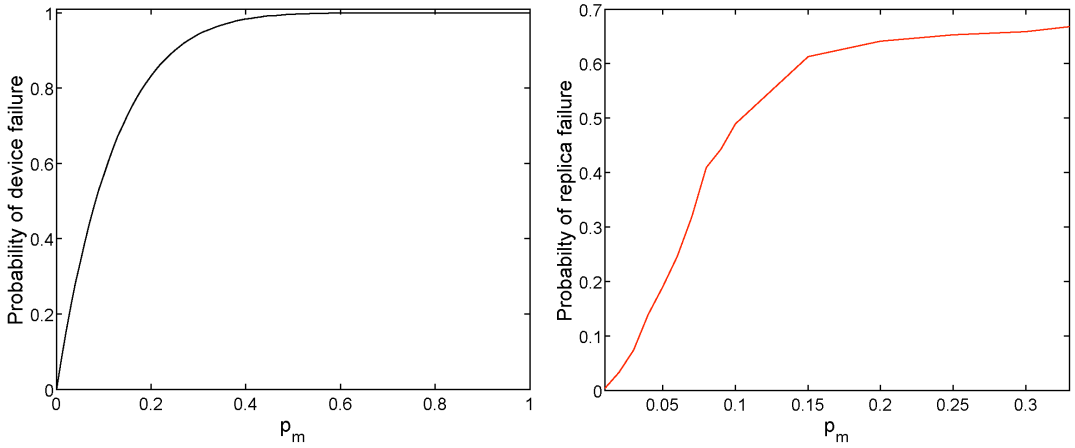


FIGURE 7.12: (a) Sum output and (b) carry output of a CNFET 1-bit full adder with $p_m = 33\%$.

The level of immunity of the four-layer reliable architecture against device failures depends on the m-CNT probability that gives the probability of CNFET failure, and the number of replicas as we demonstrate below. The probability of a N-tube CNFET or device failure ($p_{f-device}$) when m-CNTs are not removed (probability of a transistor's being short) can be calculated using the Equation 5.1, shown in Chapter 5, Section 5.2 ($p_{shortNtubes} = 1 - (1 - p_m)^N$). In the same way, the probability of replica or 1-bit full adder failure ($p_{f-replica}$) depends on the probability of device failure. In order to obtain this probability of replica failure, 1000 MC iterations were run. Figure 7.13 shows the

probability of 8-tube CNFET failure and the probability of 1-bit full adder failure in function of the m-CNT probability. Obviously, both probabilities of failure increases as p_m grows. The values of $p_{f-device}$ and $p_{f-replica}$ for the p_ms considered in this work are depicted in Table 7.1.



(a) (b)

FIGURE 7.13: a) Probability of device failure and (b) probability of replica failure vs. p_m.

TABLE 7.1: Probability of device and replica failure

p_m	**Probability of device failure**	**Probability of replica failure**
1%	7.73%	0.40%
5%	33.66%	19%
10%	56.95%	48.90%
33%	95.94%	66.80%

On the other hand, as we pointed out at the end of Section 7.3.1, the 4LRA always enables correct circuit operation if at least one replica works correctly because it is fault-free or it has device failures but still works properly. Then, the probability of correct circuit operation when the 4LRA system is used can be calculated as the probability of one or more replicas operate well ($p_{1-or-more-replicas-work-correctly}$). It is expressed as

$$p_{1-or-more-replicas-work-correctly} = 1 - (p_{f-replica})^R \tag{7.1}$$

where R is the number of redundant units or replicas.

Using this last equation, the probability correct circuit operation vs. the probability of replica failure when the 4LRA system is used for different redundancy factors, is depicted in Figure 7.14. Observe that the level of fault immunity improves as the number of replicas increases and it gets worse as the probability of replica failure grows (as p_m increases). Vertical dotted lines are the related probabilities of replica failure for the different p_m and horizontal dotted lines indicate the probability of correct circuit of 90% and 95%. Note that for the best case $p_m = 1\%$, the probability of correct replica operation is higher than 99% ($p_{f-replica}$=0.4%), then no fault-tolerant architecture would be required; whereas, at least 6 and 8 replicas would be needed to achieve a probability of correct operation of the 1-bit full adder circuit higher than 90% and 95%, respectively when $p_m = 33\%$ ($p_{f-device}$=95.94%). It should be also pointed out that the four-layer reliable architecture does not require a high number of replicas to make possible correct circuit even when the circuits a high rate of device failures - e.g. the probability of device failure for $p_m = 10\%$ is 56.95%, that gives a probability of 1-bit full adder failure of 48.9% (yield of 51.1%); using the 4LRA with just 5 replicas, the yield of the full adder can achieve the 97%-. And last but not least, Figure 7.14 can be used as a design circuit guide which could allow the designers to specify an operating point in terms of different parameters such as redundancy factor, probability of device/circuit failure, m-CNT probability and circuit yield.

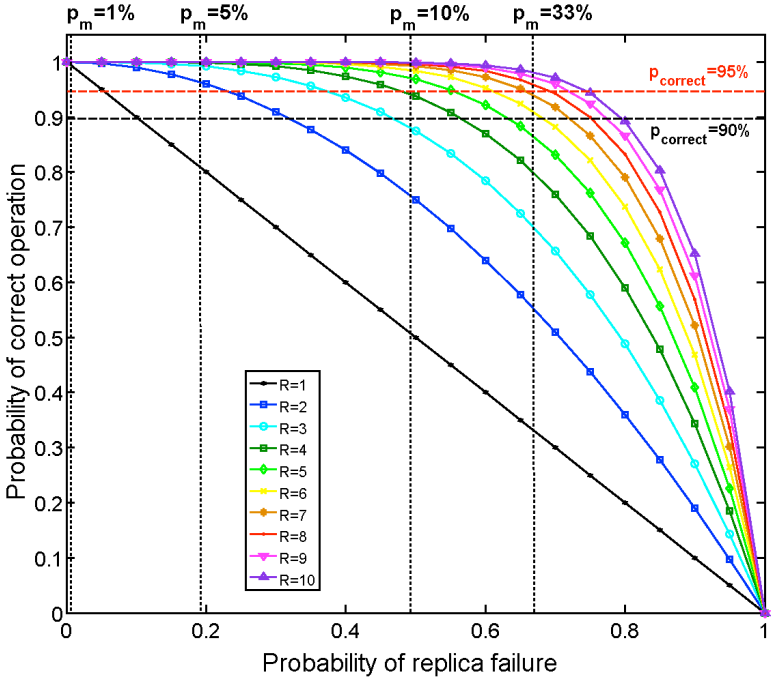


FIGURE 7.14: Probability of correct circuit operation as a function the replica failure probability for different redundant units in the second layer.

To demonstrate the operation and the effectiveness of the 4LRA and its immunity against the presence of m-CNTs, some simple examples are presented in which the 1-bit full adder is used as logic block. The first example consist of a 4LRA architecture with two identical blocks in the second layer and two averaging blocks in the third layer, one for the sum output and other for the carry output. It is assumed that the averaging blocks are also realized with carbon nanotube technology and they are fault-free. Each 1-bit full adder block in the LY2 receives three binary inputs and produces two binary outputs. The outputs of the second layer are further processed in the averaging blocks to produce the multiple-valued output. Figure 7.15 shows the output level of the averaging blocks for correct operation. The transfer function surface generated at the output of the averaging layer clearly reproduces the expected 3-input 1-bit full adder function for sum and carry outputs.

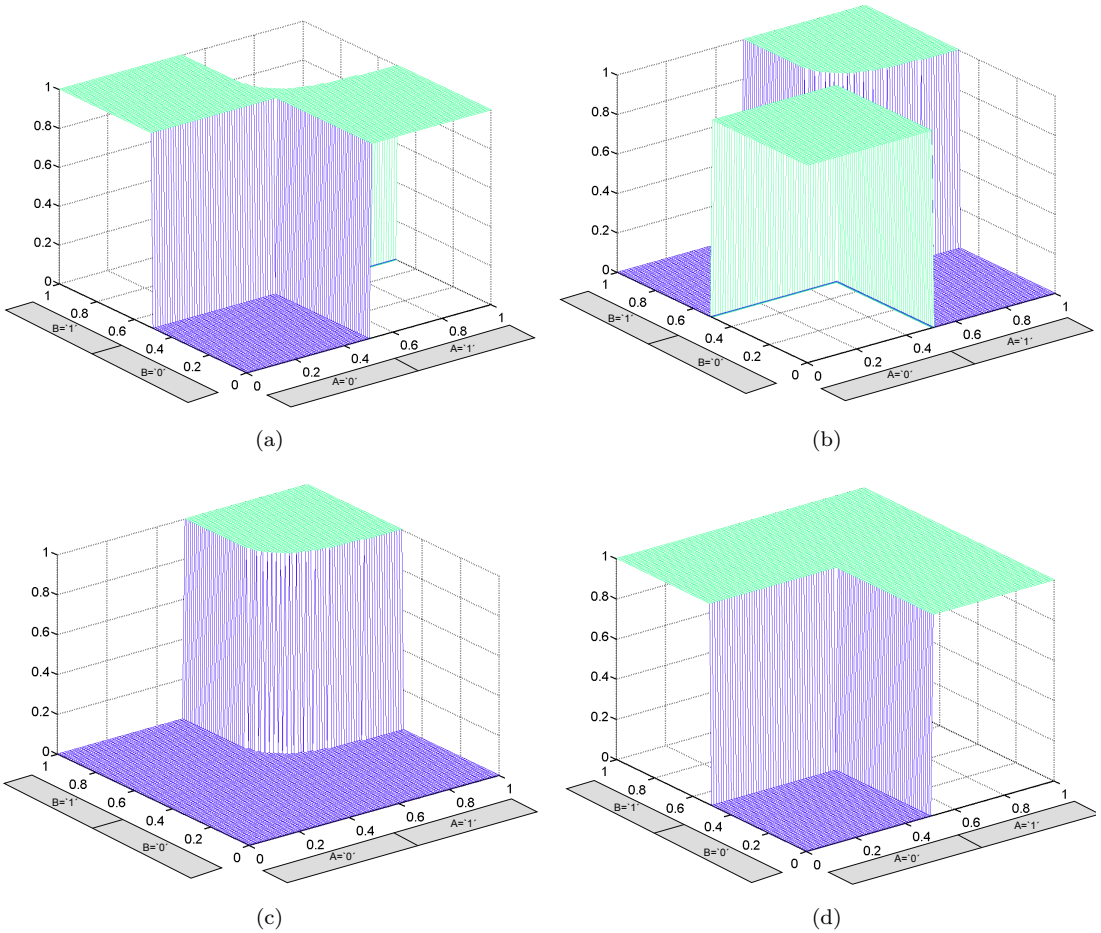


FIGURE 7.15: Output transfer function generated by the averaging layer of the 1-bit full adder circuit with 2 redundant units, showing correct operation (no device failures) for (a) sum output when carry input='0', (b) sum output when carry input='1', (c) carry output when carry input='0' and, (d) carry output when carry input='1' .

As a second example, we implemented the 4LRA architecture with two 1-bit full adders in LY2 but in this case one of the replica is fault-free and the other replica have a $p_m = 33\%$. Figure 7.16 depicts the LY3 output transfer function of the 1-bit full adder circuit with to redundant logic units for both sum and carry outputs, under the assumption of all CNFETs of one of the replicas have a m-CNT probability of $p_m = 33\%$. The multiple-valued output level of the averaging block is capable of preserving the essential function, and the correct binary output can be extracted by applying an appropriate decision threshold, however, at the expense of reduced noise margins.

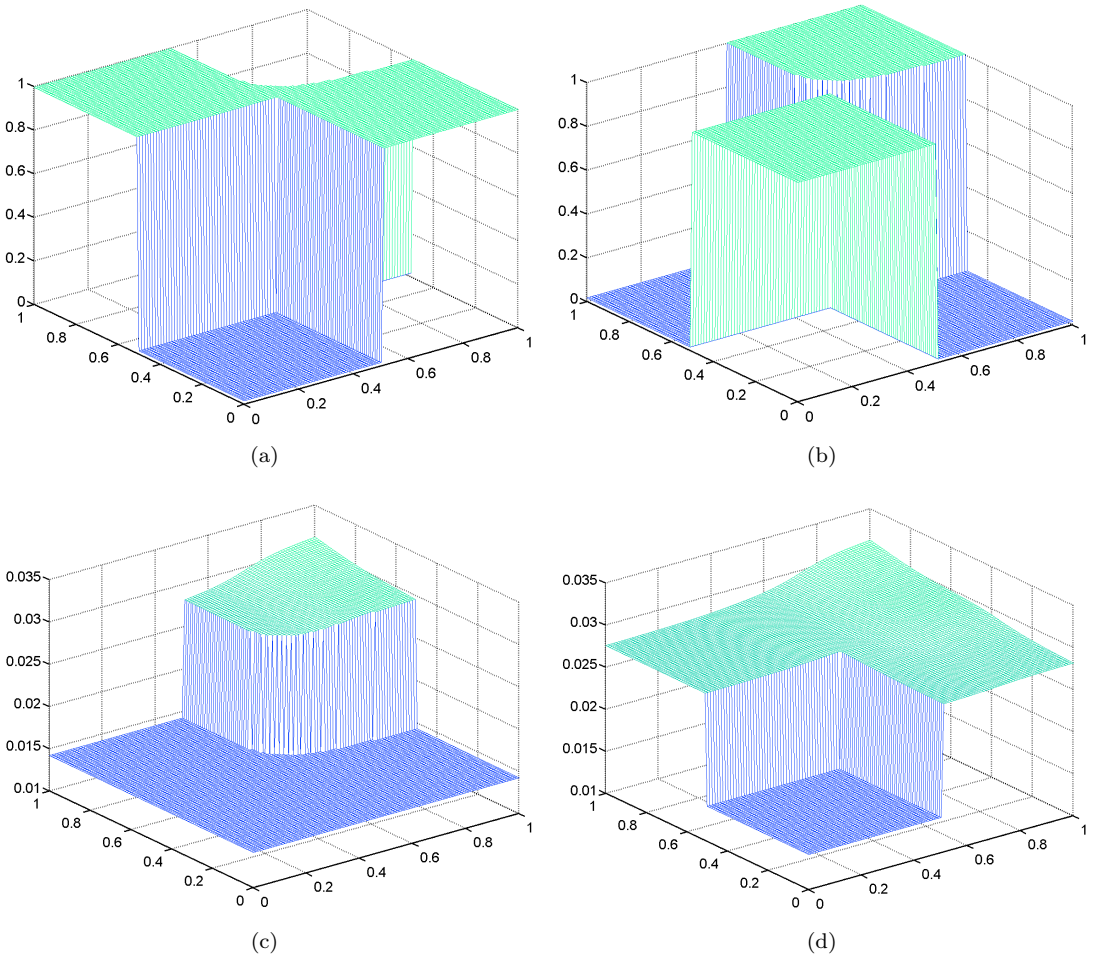


FIGURE 7.16: Output transfer function generated by the averaging layer of the 1-bit full adder circuit with 2 redundant units, in which one replica all CNFETs have a $p_m = 33\%$ whereas the other one is fault-free : (a) sum output when carry input='0', (b) sum output when carry input='1', (c) carry output when carry input='0' and, (d) carry output when carry input='1' .

7.4 Summary and Conclusions

In this chapter a complete reliability analysis of CNFET logic circuits in the presence of metallic CNTs was presented.

M-CNTs are the main challenge of CNT technology from the point of view of reliability/yield. The presence of m-CNTs in the transistor not only degrades the performance of CNFET circuits but also may lead to logic failures (incorrect operation). The techniques used nowadays to deal with the "metallic problem" such as CNT self-sorting techniques, selective etching of m-CNTs, and electrical burning of m-CNTs, should be improved and at the moment, they are not enough. Then, alternative and/or supplementary solutions to the "metallic CNT problem must be proposed.

Up to now, only one alternative technique called ACCNT have been suggested to improve the yield of CNFET circuits in the presence of m-CNTs. It is a geometric method that takes the advantage of correlation between transistors to create CNFETs that are tolerant to m-CNTs. In this Chapter, we present other possible solution to the "m-CNT problem". We propose and investigate the use of fault-tolerant architectures as a mechanism to deal with m-CNTs. We focus our work in a particular fault-tolerant system called four-layer reliable architecture (4LRA) because is has several advantages that includes: 1) it enables correct circuit operation with a low number of redundant units, 2) it always makes possible correct logic operation if at least one replica works correctly, and 3) its performance can be improved by using an adaptable decision threshold. For this purpose, we simulate different logic circuits, a NOR gate and a 1-bit full adder under different failure scenarios (different p_m). Our results show that in case of simple circuits (NOR gate), a simple threshold decision block could improve its yield. We note, for example, that the probability of failure of a NOR gate with $p_m = 33\%$ can be minimized to 0.03 by applying a threshold voltage decision of 0.23V. If a more complex circuit is studied, such as a 1-bit full adder, the implementation of the full 4LRA system is required to enhance its reliability. We propose a method to estimate the optimum redundancy factor based on the m-CNT probability (or probability of device/replica failure). We demonstrate that this architecture exhibits a good performance at low levels of redundancy against different m-CNT probabilities (e.g. for a $p_m = 5\%$ only two replicas are required to ensure a probability of correct circuit operation of 95%). Moreover, our conclusions may orient system designers to maximize the benefits of such

redundancy system. Finally, the effectiveness and the immunity of the 4LRA system against the presence of m-CNTs is demonstrated with some simulation examples.

To conclude, just note that both proposed techniques, correlation between CNFETs and fault-tolerant architectures, could be also used to deal CNT density and m-CNT induced variations, that is, to deal with open defects that results in stuck-off faults.

Chapter 8

Summary and Final Conclusions

The constant evolution of electronic technology systems has been tied to silicon technologies for manufacturing since its beginning: since 1959, when the first MOS transistor was manufactured with dimensions around 50 μm, the technology has been constantly improving the manufacturing process until the recent presented 14 nm MOS technology, roughly doubling the device density every two years following Moore's law. So, the sustaining of Moore's Law requires transistor scaling and the introduction of new materials and structures in the last years. However, the technology advance is jeopardized by the physical limitations of the underlying transistors. Predictions indicate that the MOS device is very close to the device physical and theoretical limits. Therefore, alternative technologies and materials need to be investigated to keep the technology evolution pace. One possible alternative technology is carbon nanotube.

This thesis examines important issues related to carbon nanotube transistors manufacturing process and aims at providing a complete variability and reliability analysis of CNFET devices and circuits in the presence of manufacturing imperfections, giving a realistic view of the challenges that CNT technology faces today and evaluating its viability as a possible replacement for silicon devices. Furthermore, already proposed techniques such as CNFET correlation is analyzed as a method to reduce the variability of CNFET circuits and new alternative methods like fault-tolerant architectures are investigated as an alternative solutions to enhance the yield of CNFET circuits.

8.1 Variability and Reliability of CNFET Devices and Circuits

This thesis presents a wide overview of variability and reliability issues of CNFET devices and circuits, and solutions which have been proposed.

In the first place, CNFET manufacturing imperfections and challenges, related CNT-specific variations, as well as results of the latest research in CNT technology have been introduced and investigated. We have proposed a methodology that based on Monte Carlo simulations, an homogeneous CNFET HSPICE model, and Matlab Scripts, is able to estimate the variability of multi-channel CNFETs in the presence of doping variations, alignment (channel length) variations, diameter and oxide thickness-related variations, m-CNT count induced variations and CNT density variations. Results obtained from Monte Carlo simulations proved that drive current and ON-OFF current ratio parameters are highly affected by CNT-specific variations, being m-CNT induced count variations and CNT density variations the most prominent sources of their fluctuation. The proposed methodology is also good to analyze the reliability/yield of CNFET devices, that is, to evaluate the probability of functional transistors and non-functional transistors because of the appearance of open and shorts defects caused by CNT count variations (CNT density variations + m-CNT induced variations) and the presence of m-CNTs, respectively. Based on previous analytical models for CNFET failure, we subsequently presented a CNFET failure model that includes both open and short defects and is acceptable for no m-CNTs removal as well as when an ideal or non-ideal m-CNT removal is assumed. It demonstrates that the presence of m-CNTs is the most important issue of CNFET devices from the point of view of reliability because they results in higher probability of device failure (probability of short) than CNT density or count variations (probability of open) and they are not only cause of short defects but also may be cause of open defects when they are removed.

In the second place, we have also analyzed the impact of CNT-specific variations on CNFET circuits performance by induced equivalent threshold voltage fluctuations. Important metrics of logic circuits, such as delay of an inverter (chain), figure of merit of logic speed, and noise margin of a two cross-coupled inverters, figure of merit of robustness, have been analyzed under different design styles, correlated vs. uncorrelated.

Monte Carlo simulations have proved that delay propagation shows a higher variability levels than noise margin because its strong dependence on drive current. Furthermore, the variability of both metrics can be mitigated using correlation between transistors. We have also investigated the variability of a 6T SRAM cell that has been implemented using different CMOS technology nodes (32nm, 22nm and 16nm) under different variability scenarios and CNFET technology for different temperatures. The simulation analysis has demonstrated that even for the current CNFET manufacturing imperfections, the variability level in CNFET cell is comparable with that of Si-MOS cells in the most favorable scenario (moderated). Furthermore, CNFET SRAM cell shows better tolerance against temperature changes and a better robustness against possible faults resulting from variations than MOSFET SRAM cells.

Finally, we focused on the "m-CNT problem" in CNFET logic circuits. We have proposed the use of fault-tolerant architectures to deal with the low reliability/yield of CNFET circuits in the presence of m-CNTs. We have used a particular fault-tolerant system, the 4LRA system, and we have provided a design circuit guide which could allow the designers to specify an operating circuit point in terms of different parameters such as redundancy factor and circuit yield.

8.2 Thesis Contributions

The main contributions of this thesis can be summarized as follows:

- A methodology for multi-channel CNFET variability estimation has been presented, for the first time, to analyze the effect of the main CNT-specific variations. This method uses distributions based on experimental results and can be easily utilized for device-level performance evaluation.
- The CNFET device failure models proposed in previous works have been extended to different m-CNT removal scenarios, that includes: 1) no m-CNT removal, 2) ideal m-CNT removal and, 3) non-ideal m-CNT removal.
- A methodology to evaluate the variability of CNFET circuits in the presence of CNT doping, alignment and diameter variations, and CNT density and m-CNT induced count variations when all m-CNTs are eliminated have been presented.

It allows to analyze the impact of these variations on different CNFET circuit parameters such as noise margins and delay.

- Different design styles with different degrees of CNT correlation have been explored as a technique to reduce CNFET circuits variability.

- A comparative variability analysis of a CNFET 6T SRAM cell affected by CNT-specific variations and a MOSFET 6T SRAM cell affected by process variations has been presented. Their write and read time delays have been evaluated under different variability scenarios and different temperatures.

- The use of fault-tolerant techniques as a mechanism to deal with m-CNTs, the main cause of device and circuit failure, has been proposed. The application of the four-layer reliable architecture, 4LRA, to CNFET circuits with m-CNTs has been explored. Furthermore, a method to estimate the optimum redundancy factor based on the m-CNT probability (or probability of device/replica failure) has been presented.

8.3 Future work

In the following list, we summarize some interesting ideas that we wish to expand upon in the future:

- Further developing of our CNFET variability estimation methodology that includes other CNFET manufacturing imperfections such as the presence of Schottky barriers between the CNT and the metal (Schottky barrier CNFETs) and the electrostatic doping of the channel due to environmental interactions.

- Extending the analysis of CNFET circuits variability to a non-ideal m-CNT scenario. To explore which is the optimal number of CNTs per device (optimal CNT density) that given a p_m and a $p_{mR} \neq 1$ and $p_{sR} = 0$ or $p_{sR} \neq 0$ still ensures correct circuit operation and investigate the related noise margin and delay variations.

- Analyzing the application of the 4LRA not only to the presence of stuck-on faults because of m-CNTs but also to the presence of stuck-off faults because of CNT

density and/or m-CNT induced variations. And investigating other 4LRA configurations that may include: 1) usage of different circuit design styles, each resisting some classes of faults in a better way (e.g., CMOS in replica 1, current steering logic in replica 2, and STSCL in replica 3); 2) the use of different number of transistors or transistor sizes in each replica, assuming that the voter cancels incurring different delays; 3) geometric mixing of the replicas; and 4) dynamic adaptation of weights (in our work faults are geometrically distributed in a balanced way, and the circuits are all identical, then weights should also be identical).

Appendix A

Publications Related to this Thesis

Below we present a list of publications resulting from work in this thesis.

A.1 Journal papers

- **C. García**, and A. Rubio,"New Electronic System Design Paradigms in the Technology of the year 2020," International Journal of the Society of Materials Engineering for Resources, 2009.

A.2 Chapters in books

- **C.G. Almudéver**, and A. Rubio,"Impact of Carbon Nanotube Growth Process Imperfections on CNFET Performance," 2nd edition of the Dekker Encyclopedia of Nanoscience and Nanotechnology, October 2012.

A.3 Conference papers

- **C. García**, and A. Rubio,"Manufacturing Variability Analysis in Carbon Nanotube Technology: a comparison with bulk CMOS in 6T SRAM scenario," in

Proc. IEEE 14th International Symposium on Design and Diagnostics of Electronic Circuit and Systems (DDECS), pp.249-254, Cottbus, Germany, April 2011.

- **C.G. Almudéver**, and A. Rubio,"Device variability analysis in carbon nanotube technology," in European workshop on CMOS variability (VARI), Grenoble, France, June 2011.

- **C.G. Almudéver**, and A. Rubio,"A Comparative Variability Analysis for CMOS and CNFET 6T SRAM cells," in Proc. IEEE 54th International Midwest Symposium on Circuits and Systems (MWSCAS), pp. 1-4, Seoul, Korea, August 2011.

- **C.G. Almudéver**, and A. Rubio,"Carbon nanotube growth process-related variability in CNFETs," in Proc. 11th IEEE Conference on Nanotechnology (IEEE-NANO), pp. 1084-1087, Portland, USA, August 2011.

- **C.G. Almudéver**, and A. Rubio,"Variability and Reliability Analysis of CNFET in the presence of Carbon Nanotube Density Fluctuations," in Proc. International Conference on Mixed Design of Integrated Circuits and Systems (MIXDES), pp. 124-129, Warsaw, Poland, May 2012.

- **C.G. Almudéver**, I. Martín-Fernández, M. Sansa, E. Lora-Tamayo, P. Godignon, A. Rubio, and F. Pérez-Murano,"Variability Analysis of Carbon Nanotube Field Effect Transistors," in 38th International Conference on Micro and Nano Engineering (MNE), Toulouse, France, September 2012.

- **C.G. Almudéver**, and A. Rubio,"Impact of manufacturing imperfections on CNFET performance," in Intel Ireland Research Conference (IIRC), Dublin, Ireland, November 2013.

A.4 Deliverables of TRAMS project

- Deliverable D1.2. PDK for sub 16 nm CNT transistors including statistical variability and reliability.

- Deliverable D3.6. Report of the effect of environmental and process parameters on the variability of memory cells and systems.

Appendix B

Other Publications

Below we present a list of publications resulting from work in collaboration with the members of Reliability of Electron Device and Circuits (REDEC) Group of Universitat Autònoma de Barcelona and with other HIPIC group members.

B.1 Journal papers

- E. Amat, **C.G. Almudéver**, N. Aymerich, R. Canal, and A. Rubio,"Impact of FinFET technology introduction in the 3T1D-DRAM memory cell," IEEE Trans. on Device and Materials Reliability, vol.13, no. 1, pp. 287-292, 2013.
- E. Amat, **C.G. Almudéver**, N. Aymerich, R. Canal, and A. Rubio,"Variability mitigation mechanisms in scaled 3T1D DRAM memories to 22nm and beyond," IEEE Trans. on Device and Materials Reliability, vol.13, no. 1, pp. 103-109, 2013.
- E. Amat, E. Amatllé, S. Gómez, N. Aymerich, **C.G. Almudéver**, F. Moll, and A. Rubio,"Systematic and random variability analysis of two different 6T-SRAM layout topologies," Microelectronics Journal, vol.44, no. 9, pp. 787-793, 2013.
- E. Amat, A. Calomarde, **C.G. Almudéver**, N. Aymerich, R. Canal, and A. Rubio,"Impact of FinFETs and III-V/Ge technology on logic and memory cell behavior," IEEE Trans. on Device and Materials Reliability, vol. 14, no.1, pp. 344-350, 2014.

- J. Martin-Martinez, **C.G. Almudéver**, A. Crespo-Yepes, R. Rodriguez, M. Nafria, and A. Rubio,"A shapeshifting evolvable hardware mechanism based on reconfigurable memFETs crossbar architecture," Microelectronics Reliability, available online 5 May 2014.

- E. Amat, **C.G. Almudéver**, N. Aymerich, R. Canal, and A. Rubio,"Suitability of the FinFET 3T1D cell beyond 10nm," IEEE Trans. on Nanotechnology, accepted.

B.2 Conference papers

- **C. García**, and A. Rubio,"Electronic Design under New Alternatives to Solid-State Semiconductors," in Proc. International Conference on Materials and Reliability (ICMR), Akita, Japan, October 2009.

- **C. García**, F. Moll, and A. Rubio,"Design of boolean functions and memory units based on Resistive Switching Devices," in Conference on Design of Circuits and Integrated Systems (DCIS), Lanzarote, Spain, November 2010.

- E. Amat, **C.G. Almudéver**, N. Aymerich, R. Canal, and A. Rubio,"Strain Relevance on the Improvement of the 3T1D Cell Performance," in Proc. International Conference on Mixed Design of Integrated Circuits and Systems (MIXDES), pp. 120-123, Warsaw, Poland, May 2012.

- **C.G. Almudéver**, J. Martin-Martinez, A. Crespo-Yepes, R. Rodriguez, M. Nafria, and A. Rubio,"Shape-Shifting Digital Hardware Concept: Towards a New Computing System," in Proc. NASA/ESA Conference on Adaptive Hardware and Systems (AHS), pp. 167-173, Nuremberg, Germany, June, 2012.

- J. Martin-Martinez, **C.G. Almudéver**, A. Crespo-Yepes, R. Rodriguez, M. Nafria, X. Aymerich, and A. Rubio,"memFET: a new multi-purpose resistive switching device," in 17th Workshop on Dielectrics in Microelectronics (WoDiM), Dresden, Germany, June 2012.

- E. Amat, **C.G. Almudéver**, N. Aymerich, R. Canal, and A. Rubio,"Impact of bulk/SOI 10nm FinFETs on 3T1D-DRAM cell performance," in Proc. IEEE International Conference on Solid-State and Integrated Circuits (ICSICT), pp.1-3, Xian, China, October 2012.

- E. Amat, **C.G. Almudéver**, N. Aymerich, R. Canal, and A. Rubio,"Mitigation strategies of the variability in 3T1D cell memories scaled beyond 22nm," in Conference on Design of Circuits and Integrated Systems (DCIS), Avignon, France, November 2012.

- J. Martin-Martinez, **C.G. Almudéver**, A. Crespo-Yepes, R. Rodriguez, M. Nafria, X. Aymerich, and A. Rubio,"memFET: from Gate Dielectric Breakdown to System Reconfigurability," in Proc. IEEE International Reliability Physics Symposium (IRPS), Monterey, CA, USA, April 2013.

- E. Amat, **C.G. Almudéver**, N. Aymerich, R. Canal, and A. Rubio,"Variability Robustness Enhancement for 7nm FinFET 3T1D-DRAM Cells," in Proc. IEEE 56th International Midwest Symposium on Circuits and Systems (MWSCAS), Columbus, OH, USA, August 2013.

- E. Amat, A. Calomarde, **C.G. Almudéver**, N. Aymerich, R. Canal, and A. Rubio,"Impact of FinFETs and III-V/Ge technology on 3T1D cell behavior," in Intel Ireland Research Conference (IIRC), Dublin, Ireland, November 2013.

- E. Amat, A. Calomarde, **C.G. Almudéver**, N. Aymerich, R. Canal, and A. Rubio,"FinFET introduction in 3T1D-DRAM cells," in Conference on Design of Circuits and Integrated Systems (DCIS), Donosti, Spain, November 2013.

Bibliography

[1] G. E. Moore. Cramming more components onto integrated circuits. *Electronics Magazine*, 38(8), April 1965.

[2] International Technology Roadmap for Semiconductors. URL `http://public.itrs.net/`.

[3] W. Shockley. The path to the conception of the junction transistor. *IEEE Trans. on Electron Devices*, 23(7):597–620, July 1976.

[4] G. E. Moore. The role of Fairchild in silicon technology in the early days of "Silicon Valley". *Proceedings of IEEE*, 86(1):53–62, January 1998.

[5] R. G. Arns. The other transistor: early history of the metal-oxide semiconductor field-effect transistor. *Engineering Science and Education Journal*, 7(5):233–240, October 1998.

[6] H. Iwai. Roadmap for 22 nm and beyond. *Microelectronic Engineering Journal*, 86 (7-9):1520–1528, September 2009.

[7] K. J. Kuhn. Technology options for 22nm and beyond. *International Workshop on Junction Technology (IWJT)*, May 2010.

[8] J. A. Hutchby, G. I. Bourianoff, V. V. Zhirnov, and J. E. Brewer. Extending the road beyond CMOS. *IEEE Circuits and Devices Magazine*, 18(2):28–41, March 2002.

[9] T. Skotnicki, J. A. Hutchby, Tsu-Jae King, and H. -S.P. Wong. The end of CMOS scaling: toward the introduction of new materials and structural changes to improve MOSFET performance. *IEEE Circuits and Devices Magazine*, 21(1):16–26, February 2005.

[10] D. -H. Kim et al. 50-nm E-mode $In_{0.7}Ga_{0.3}As$ PHEMTs on 100-mm InP substrate with $f_{max} > 1THz$. *IEEE Int. Electron Devices Meeting (IEDM)*, 692–695, 2010.

[11] D. -H. Kim and J. A. del Alamo. 30-nm InAs PHEMTs with $f_T = 644GHz$ and $f_{max} = 681GHz$. *IEEE Electron Device Letter*, 31(8):806–808, August 2010.

[12] A. Leuther et al. 20 nm Metamorphic HEMT with 660 GHz f_T. *Int. Conference Indium Phosphide and Related Materials*, 1–4, 2011.

[13] J. A. del Alamo Nanometre-scale electronics with III-V compound semiconductors. *Nature*, 479:317–323, November 2011.

[14] R. Pillarisetty. Academic and industry research progress in germanium nanodevices. *Nature*, 479:324–328, November 2011.

[15] H. Matsubara, T. Sasada, M. Takenaka, and S. Takagi. Evidence of low interface trap density in GeO2/Ge metal-oxide-semiconductor structures fabricated by thermal oxidation. *Apply Physics Letters*, 31(3):032104–032104-3, July 2008.

[16] C. H. Lee et al. Ge/GeO2 interface control with high-pressure oxidation for improving electrical characteristics. *Apply Physics Express*, 2(7):071404, 2009.

[17] D. Kuzum et al. High-Moblity Ge N-MOSFETs and Mobility Degradation Mechanisms. *IEEE Electron Device Letter*, 58(1):59–66, January 2011.

[18] S. Kabuyanagi, T. Nishimura, K. Nagashio and A. Toriumi. High Electron Mobility in Germanium Junctionless n-MOSFETs. *ECS Trans.*, 58(9):309–315, 2013.

[19] M. Takenaka, R. Zhang, and S. Takagi. MOS interface engineering for high-mobility Ge CMOS. *IEEE Int. Reliability Physics Symposium*, 4C.1.1–4C.1.8, 2013.

[20] C. H. Su et al. Gate-All-Around Junctionless Transistors With Heavily Doped Polysilicon Nanowire Channels. *IEEE Electron Device Letters*, 32(4):521–523, April 2011.

[21] J. P. Coligne et al. Nanowire transistors without junctions. *Nature Nanotechnology*, 5:225–229, February 2010.

[22] R. Coquand et al. Scaling of high-k/metal-gate TriGate SOI nanowire transistors down to 10 nm width. *Solid-State Electronics*, 88:32–36, 2013.

[23] L. Amarú, P. E. Gaillardon, and G. de Michelli. Efficient Arithmetic Logic Gates Using Double-Gate Silicon Nanowire FETs. *Int. New Circuits and Systems Conference (NEWCAS)*, 1–4, 2013.

[24] K. Tomioka, M. Yoshimura, and T. Fukui. A IIIV nanowire channel on silicon for high-performance vertical transistors. *Nature*, 488(7410):189–192, August 2012.

[25] J. W. Sleight et al. Gate-All-Around Silicon Nanowire MOSFETs and Circuits. *Device Research Conference (DRC)*, 269–272, 2010.

[26] S. Bangsaruntip et al. Gate-all-around Silicon Nanowire 25-Stage CMOS Ring Oscillators with Diameter Down to 3 nm. *Symposium on VLSI Technology (VLSIT)*, 21–21, 2010.

[27] A. Heinzig, S. Slesazeck, F. Kreupl, T. Mikolajick and W M. Weber. Reconfigurable Silicon Nanowire Transistors. *Nano Letters*, 12(1):119–124, November 2011.

[28] H. Yan et al. Programmable nanowire circuits for nanoprocessors. *Nature*, 470 (7333):240–244, February 2011.

[29] Y. Liu et al. Design Optimization for Digital Circuits Built With Gate-All-Around Silicon Nanowire Transistors. *IEEE Trans. on Electron devices*, 59(7):1844–1850, July 2012.

[30] A. Hellemans. Ring around the nanowire [news]. *IEEE Spectrum*, 50(5):14–16, May 2013.

[31] L. Jiao, L. Zhang, X. Wang, G. Diankov, and H. Dai. Narrow graphene nanoribbons from carbon nanotubes. *Nature*, 458:877–880, February 2009.

[32] D. V. Kosynkin et al. Longitudinal unzipping of carbon nanotubes to form graphene nanoribbons. *Nature*, 458:872–876, February 2009.

[33] J. Cai et al. precise bottom-up fabrication of graphene nanoribbons. *Nature*, 466: 470–473, July 2010.

[34] T. H. Vo et al. Large-scale solution synthesis of narrow graphene nanoribbons. *Nature Communications*, 5(3189), February 2014.

[35] R. Grassi et al. Tight-binding and effective mass modeling of armchair graphene nanoribbon FETs. *Solid-state electronics*, 53(4):462–467, April 2009.

[36] X. Li, X. Wang, Li Zhang, S. Lee, and H. Dai. Chemically Derived, Ultrasmooth Graphene Nanoribbon Semiconductors. *Science*, 319:1229, January 2008.

[37] Y. Ouyang, Y. Yoon, and J. Guo. Scaling Behaviors of Graphene Nanoribbon FETs: A Three-Dimensional Quantum Simulation Study. *IEEE Trans. on Electron Devices*, 54(9):2223–2231, September 2007.

[38] X. Liang, and S. Wi. Transport Characteristics of Multichannel Transistors Made from Densely Aligned Sub-10 nm Half-Pitch Graphene Nanoribbons. *ACS Nano*, 6 (11):9700–9710, 2012.

[39] M. Son et al. Sub-10 nm Graphene Nanoribbon Array Field-Effect Transistors Fabricated by Block Copolymer Lithography. *Advanced Materials*, 25(34):4723–4728, September 2013.

[40] M. R. Choudhury, Y. Yoon, J. Guo, and K. Mohanram. Graphene Nanoribbon FETs: Technology Exploration for Performance and Reliability. *IEEE Trans. on Nanotechnology*, 10(4):727–736, July 2011.

[41] R. Sordan, and A. C Ferrari. Gigahertz Multi-Transistor Graphene Integrated Circuits. *Technical Digest-International Electron Devices Meeting (IEDM)*, 1–1, 2013.

[42] J. Zheng et al. precise bottom-up fabrication of graphene nanoribbons. *Nature*, 3 (1314), February 2013.

[43] N. Patil, J. Deng, S. Mitra, and H -S.P. Wong. Circuit-Level Performance Benchmarking and Scalability Analysis of Carbon Nanotube Transistor Circuits. *IEEE Trans. on Nanotechnology*, 8(1):37–45, January 2009.

[44] A. D. Franklin et al. Sub-10 nm Carbon Nanotube Transistor. *Nano Letters*, 12 (2):758–762, January 2012.

[45] A. D. Franklin et al. Carbon Nanotube Complementary Wrap-Gate Transistors. *Nano Letters*,13(6):2490–2495, May 2013.

[46] L. Ding et al. Carbon nanotube based ultra-low voltage integrated circuits: Scaling down to 0.4 V. *Apply Physics Letters*, 100(26):263116–263116-5, June 2012.

[47] B. Kim et al. Low voltage, high performance inkjet printed carbon nanotube transistors with solution processed ZrO2 gate insulator. *Apply Physics Letters*, 103(8): 082119–082119-4, 2013.

[48] M. M. Shulaker et al. Carbon nanotube computer. *Nature*, 501(7468):526–530, September 2013.

[49] H. Li, W. Liu, A. M. Cassell, F. Kreupl, and K. Banerjee. Low-resistivity long-length horizontal carbon nanotube bundles for interconnect applications. Part I: Process development. *IEEE Trans. on Electron devices*, 60(9):2862–2869, September 2013.

[50] H. Li, W. Liu, A. M. Cassell, F. Kreupl, and K. Banerjee. Low-resistivity long-length horizontal carbon nanotube bundles for interconnect applications. Part II: Characterization. *IEEE Trans. on Electron devices*, 60(9):2870–2876, September 2013.

[51] T. Durkop, S. A. Getty, E. Cobas, and M.S.. Fuhrer. Extraordinary mobility in semiconducting carbon nanotubes. *Nano Letters*,4(1):35–39, May 2004.

[52] A. Javey, J. Guo, Q. Wang, M. Lundstrom, and H. Dai. Ballistic carbon nanotube field-effect transistors. *Nature*, 424(6949):654–657, August 2003.

[53] S. Tans, A. Verschueren and C. Dekker. Room-temperature transistor based on a single carbon nanotube. *Nature*, 49(393):49–52, May1998.

[54] V. Derycke, R. Martel, J. Appenzeller and Ph. Avouris. Carbon Nanotube Inter- and Intramolecular Logic Gates. *Nano Letters*, 1(9):453–456, 2001.

[55] A. Bachtold, P. Hadley, T. Nakanishi and C. Dekker. Logic circuits with carbon nanotube transistors. *Science*, 294(5545):1317–1320, November 2001.

[56] S. J. Wind, J. Appenzeller, R. Martel, V. Derycke and Ph. Avouris. Vertical scaling of carbon nanotube field-effect transistors using top gate electrodes. *Applied Physics Letters*, 80(20):3817, May 2002.

[57] S. J. Wind, J. Appenzeller, R. Martel, V. Derycke and P. Avouris. Fabrication and electrical characterization of top gate single-wall nanotube field-effect transistors. *Journal of Vacuum Science Technology B*, 20(6):2798, December 2002.

[58] Z. Chen et al. An Integrated Logic Circuit Assembled on a Single Carbon Nanotube. *Science*, 311(5768):1735, March 2006.

[59] M. Lundstrom, J. Guo, S. Datta, and M.P. Anantram. Toward multiscale modeling of carbon nanotube transistors. *The International Journal of Multiscale Computer Engineering*, 2(2):257–277, 2004.

[60] R. Dutton. TCAD Tools at Stanford University: PISCES. URL `http://www-tcad.stanford.edu/tcad/programs/pisces.html`.

[61] The SPICE Page. URL `http://bwrcs.eecs.berkeley.edu/Classes/IcBook/SPICE/`.

[62] S. Datta, J. Guo, and M. Lundstrom. A numerical study of scaling issues for Schottky-barrier carbon nanotube transistors. *IEEE Trans. on Electron Devices*, 51 (2):172–177, February 2004.

[63] A. Raychowdhury, S. Mukhopadhyay, and K. Roy. A Circuit-Compatible Model of Ballistic Carbon Nanotube Field-Effect Transistors. *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, 23(10):1411–1420, October 2004.

[64] S. Sinha, A. Balijepalli, and Y. Cao. Compact Model of Carbon Nanotube Transistor and Interconnect. *IEEE Trans. on Electron Devices*, 56(10):2232–2242, October 2009.

[65] M. Najari,S. Fregonèse, N. Masmoudi, and T. Zimmer. Schottky Barrier Carbon Nanotube Transistor: Compact Modeling, Scaling Study, and Circuit Design Applications. *IEEE Trans. on Electron Devices*, 58(1):195–205, January 2011.

[66] J. Deng and H. -S. P. Wong. Modeling and Analysis of Planar-Gate Electrostatic Capacitance of 1-D FET With Multiple Cylindrical Conducting Channels. *IEEE Trans. on Electron Devices*, 54(9):2377–2385, September 2007.

[67] J. Deng and H. -S. P. Wong. A compact SPICE model for carbon-nanotube field-effect transistors including nonidealities and its application Part I: Model of the intrinsic channel region. *IEEE Trans. on Electron Devices*, 54(12):3186–3194, December 2007.

[68] J. Deng and H. -S. P. Wong. A compact SPICE model for carbon-nanotube field-effect transistors including nonidealities and its applicationPart II: Full device model and circuit performance benchmarking. *IEEE Trans. on Electron Devices*, 54(12): 3195–3205, December 2007.

[69] (2008) The Stanford University CNFET model website. [Online]. Available: http://nano.stanford.edu/model.php?id=23.

[70] C. G. Almudever, and A. Rubio Carbon nanotube growth process-related variability in CNFETs. *Proc. of IEEE Conference on Nanotechnology (IEEE-NANO)*, 1084–1087, 2011.

[71] A. Raychowdhury et al. Variation Tolerance in a Multichannel Carbon-Nanotube Transistor for High-Speed Digital Circuits. *IEEE Trans. on Electron Devices*, 56(3): 383–392, March 2009.

[72] B. Paul et al. Impact of a Process Variation on Nanowire and Nanotube Device Performance. *IEEE Trans. on Electron Devices*, 54(9):2369–2376, September 2007.

[73] N. Patil et al. Wafer-scale growth and transfer of aligned single-walled carbon nanotubes. *IEEE Trans. on Nanotechnology*, 8(4):498–504, July 2009.

[74] N. Patil, A. Lin, E. R. Myers, H. -S.P. Wong, and S. Mitra. Integrated Wafer-scale Growth and Transfer of Directional Carbon Nanotubes and Misaligned- Carbon-Nanotube-Immune Logic Structures. *Proc. of Symposium on VLSI Technology*, 205–206, 2008.

[75] J. Zhang, N. P. Patil, A. Hazeghi, H. -S.P.Wong, and S.Mitra. Characterization and Design of Logic Circuits in the Presence of Carbon Nanotube Density Variations. *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, 30(8): 1103–1113, August 2011.

[76] C. G. Almudever, and A. Rubio. Variability and Reliability Analysis of CNFET in the Presence of Carbon Nanotube Density Fluctuations. *Proc. of Conference on Mixed Design of Integrated Circuits and Systems (MIXDES)*, 124–129, 2012.

[77] S. W. Wong, T. Banks, and J. -A. Rogers. Improved density in aligned arrays of single-walled carbon nanotubes by sequential chemical vapor deposition on quartz. *Advanced Materials*, 22(45):1826–1830, April 2010.

[78] M. M. Shulaker at el. Linear Increases in Carbon Nanotube Density Through Multiple Transfer Technique. *Nano Letters*, 11(5):1881–1881, April 2011.

[79] L. Qu, D. Feng, and L. Dai. Preferential Syntheses of Semiconducting Vertically Aligned Single-Walled Carbon Nanotubes for Direct Use in FETs. *Nano Letters*, 8 (9):2682–2687, July 2008.

[80] T. Mizutani, H. Ohnaka, Y. Okigawa, S. Kishimoto, and Y. Ohno. A study of preferential growth of carbon nanotubes with semiconducting behavior grown by plasma-enhanced chemical vapor deposition. *Journal of Applied Physics*, 106(7): 073705–073705-5, October 2009.

[81] M. LeMieux et al. Self-sorted, aligned nanotube networks for thin-film transistors. *Science*, 321(5885):101-104, July 2008.

[82] P. Collins, S. Arnold, and P. Avouris. Engineering carbon nanotubes and nanotube circuits using electrical breakdown. *Science*, 292(5517):706-709, April 2001.

[83] G. Zhang et al. Selective etching of metallic carbon nanotubes by gas-phase reaction. *Science*, 314(5801):974–977, November 2006.

[84] H. Wei at al. Efficient Metallic Carbon Nanotube Removal Readily Scalable to Wafer-Level VLSI CNFET Circuits. *Proc. of Symposium on VLSI Technology*, 237–238, 2010.

[85] S. H. Jin et al. Using nanoscale thermocapillary flows to create arrays of purely semiconducting single-walled carbon nanotubes. *Nature Nanotechnology*, 8:347-355, April 2013.

[86] A. Lin, N. Patil, H. Wei, S. Mitra, and H. -S.P.Wong. ACCNT–A Metallic-CNT-Tolerant Design Methodology for Carbon-Nanotube VLSI: Concepts and Experimental Demonstration. *IEEE Trans. on Electron Devices*, 56(12):2969–2978, December 2009.

[87] A. Lin, J. Zhang, N. Patil, H. Wei, S. Mitra, and H. -S.P.Wong. ACCNT: A Metallic-CNT-Tolerant Design Methodology for Carbon Nanotube VLSI: Analyses and Design Guidelines. *IEEE Trans. on Electron Devices*, 57(9):2284–2295, September 2010.

[88] Q. Cao, S. -J. Han, G. S. Tulevski, A. D. Franklin, and W. Haensch. Evaluation of Field-Effect Mobility and Contact Resistance of Transistors That Use Solution-Processed Single-Walled Carbon Nanotubes. *ACS Nano*, 6(7):6471–6477, June 2012.

[89] Q. Cao et al. Arrays of single-walled carbon nanotubes with full surface coverage for high-performance electronics. *Nature Nanotechnology*, 8:180-186, January 2013.

[90] D. Shahrjerdi et al. High-Performance Air-Stable n-Type Carbon Nanotube Transistors with Erbium Contacts. *ACS Nano*, 7(9):8303–8308, September 2013.

[91] H. Wei, H. -Y. Chen, L. Liyanage, H. S. Wong, and S. Mitra. Air-Stable Technique for Fabricating n-Type Carbon Nanotube FETs. *Proc. of International Electron Device Meeting (IEDM)*, 23.2.1–23.2.4, 2011.

[92] Y. Chai et al. Low-Resistance Electrical Contact to Carbon Nanotubes With Graphitic Interfacial Layer. *IEEE Trans. on Electron Devices*, 59(1):12–19, January 2012.

[93] Z. Chen, J. Appenzeller, J. Knoch, Y. -Ming. Lin and P. Avouris. The role of metal-nanotube contact in the performance of carbon nanotube field-effect transistors. *Nano Letters*, 5(7):1497–1502, June 2005.

[94] S. Borkar, A. Keshavarzi, J. Kurtin, and K. De Vivek. Statistical circuit design with carbon nanotubes. United States Patent Application 2007015506.

[95] N. Patil, J. Deng, S. Mitra, and H. -S.P.Wong. Circuit-Level Performance Benchmarking and Scalability Analysis of Carbon Nanotube Transistor Circuits. *IEEE Trans. on Nanotechnology*, 8(1):37–45, January 2009.

[96] J. Zhang, N. Patil, H. -S.P.Wong, and S. Mitra. Overcoming Carbon Nanotube Variations through Co-optimized Technology and Circuit Design. *International Electron Devices Meeting (IEDM)*, 4.6.1–4.6.4, 2011.

[97] S. Sharifzadeh, J.R. Koehler, A.B. Owen, and J.D. Shott. Using simulators to model transmitted variability in IC manufacturing. *IEEE Trans. on Semiconductor Manufacturing*, 2(3):82–93, August 1989.

[98] J. Zhang, N. Patil, and S. Mitra. Probabilistic analysis and design of metallic-carbon-nanotube-tolerant digital logic circuits. *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems*, 28(9):1307–1320, September 2009.

[99] P. Zarkesh-Ha, and A. -A.M. Sashi. Stochastic Analysis and Design Guidelines for CNFETs in Gigascale Integrated Systems. *IEEE Trans. on Electron Devices*, 58(2): 530–539, February 2011.

[100] B. Ghavami, M. Raji, H. Pedram, and M. Pedram. Statistical Functional Yield Estimation and Enhancement of CNFET-Based VLSI Circuits. *IEEE Trans. on Very Large Scale Integration (VLSI) Systems*, 21(4):887–900, May 2013.

[101] J. Zhang et al. Carbon Nanotube Correlation: Promising Opportunity for CNFET Circuit Yield Enhancement. *Proc. of Design Automation Conference (DAC)*, 889–892, 2010.

[102] L. Wei, D.J. Frank, L. Chang, and H. -S.P.Wong. A Non-iterative Compact Model for Carbon Nanotube FETs Incorporating Source Exhaustion Effects. *International Electron Devices Meeting (IEDM)*, 1–4, 2009.

[103] A. Arabi, M. Sashi, and P. Zarkesh-Ha. Prediction of gate delay variations for CNFET under CNT density variation. *IEEE International Symposium on Defect and Fault Tolerance in VLSI and Nanotechnology Systems (DFT)*, 140–145, 2012.

[104] C.F. Hill. Definitions of noise margin in logic systems. *Mullard Tech. Commun*, (89):239–245, September 1967.

[105] A. Asenov. Random dopant induced threshold voltage lowering and fluctuations in sub-0.1 MOSFET's: A 3-D"atomistic" simulation study. *IEEE Trans. on Electron Devices*, 45(12):2505–2513, December 1998.

[106] Terascale Reliable Adaptive Memory Sytems Project. TRAMS. URL `https://trams-project.upc.edu/`.

[107] PTM models. URL `http://ptm.asu.edu/`.

[108] J. G. Delgado-Frias, Z. Zhang, and M. A. Turi. Low power SRAM cell design for FinFET and CNTFET technologies. *International Conference on Green Computing*, 547–533, 2010.

[109] K.B.K. Teo et al. Carbon nanotube technology for solid state and vacuum electronics. *IEEE Procc. on Circuits, Devices and Systems*, 151(5):443–451, October 2004.

[110] J. von Neumann. Probabilistic logics and the synthesis of reliable organisms from unreliable components. *Automata Studies*, (34):43–89,1956.

[111] J. Bastos, M. Steyaert, B. Graindourze, and W. Sansen. Matching of MOS transistors with different layout styles. *Proc. of Int. Conference on Microelectronic Test Structures (ICMTS)*, 17–18, 1996.

[112] W.S. McCulloch and W. Pitts. A logical calculus of the ideas immanent in nervous activity. *Bull. Math. Biophys.*, (5):115–133,1943.

[113] W.S. McCulloch and W. Pitts. How we know universals: The perception of auditory and visual forms. *Bull. Math. Biophys.*, (9):127–147,1947.

[114] M. Stanisavljevic, A. Schmid, and Y. Leblebici Optimization of the averaging reliability technique using low redundancy factors for nanoscale technologies. *IEEE Trans. on Nanotechnology*, 8(3):379–390, May 2009.

[115] M. Stanisavljevic, A. Schmid, and Y. Leblebici Reliability of Nanoscale Circuits and Systems. *Springer*, 2011.