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Advanced AlGaN/GaN HEMT technology, design, fabrication and characterization

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- La millor part d'aquest gran esforç es arribar a la meta i saber que tu i la petita m'esteu esperant. -

Dedicat en especial a tu Laura, i a la petita Martina!

- Gràcies als meus, als que han fet possible que arribés fins aquí i a la meva família. -

Abstract

Nowadays, the microelectronics technology is based on the mature and very well established silicon (Si) technology. However, Si exhibits some important limitations regarding its voltage blocking capability, operation temperature and switching frequency. In this sense, Gallium Nitride (GaN) $-$ $based$ high electron mobility transistors ($HEMTs$) devices have the potential to make this change possible. The unique combination of the high-breakdown field, the high-channel electron mobility of the two dimensional electron gas ($2DEG$), and high-temperature of operation has attracted enormous interest from social, academia and industry and in this context this PhD dissertation has been made. This thesis has focused on improving the device performance through the advanced design, fabrication and characterization of $AlGaN/GaN$ $HEMTs$, primarily grown on Si templates.

The first milestone of this PhD dissertation has been the establishment of a $know - how$ on GaN $HEMT$ technology from several points of view: the device design, the device modeling, the process fabrication and the advanced characterization primarily using devices fabricated at Centre de Recherche sur l'Hétéro-Epitaxie ($CRHEA - CNRS$) (France) in the framework of a collaborative project. In this project, the main workhorse of this dissertation was the explorative analysis performed on the $AlGaN/GaN$ $HEMTs$ by innovative electrical and physical characterization methods. A relevant objective of this thesis was also to merge the nanotechnology approach with the conventional characterization techniques at the device scale to understand the device performance.

A number of physical characterization techniques have been imaginatively used during this PhD determine the main physical parameters of our devices such as the morphology, the composition, the threading dislocations density, the nanoscale conductive pattern and others. The conductive atomic force microscopy ($CAFM$) tool have been widely described and used to understand the conduction mechanisms through the $AlGaN/GaN$ Ohmic

contact by performing simultaneously topography and electrical conductivity measurements. As it occurs with the most of the electronic switches, the gate stack is maybe the critical part of the device in terms of performance and longtime reliability. For this reason, how the $AlGaN/GaN\ HEMT$ gate contact affects the overall $HEMT$ behaviour by means of advanced characterization and modeling has been intensively investigated.

It is worth mentioning that the high-temperature characterization is also a cornerstone of this PhD. It has been reported the elevated temperature impact on the forward and the reverse leakage currents for analogous Schottky gate $HEMTs$ grown on different substrates: Si, $sapphire$ and free-standing GaN ($FS-GaN$). The $HEMT$' forward-current temperature coefficients (T^{α}) as well as the thermal activation energies have been determined in the range of $25-300$ °C. Besides, the impact of the elevated temperature on the Ohmic and gate contacts has also been investigated.

The main results of the $gold-free\ AlGaN/GaN\ HEMTs$ high-voltage devices fabricated with a 4 $inch\ Si\ CMOS$ compatible technology at the clean room of the CNM in the framework of the industrial contract with ON semiconductor were presented. We have shown that the fabricated devices are in the state-of-the-art ($gold-free$ Ohmic and Schottky contacts) taking into account their power device figure-of-merit ($V_B^2/R_{on,sp}$) of $4.05\times10^{8}\ W/cm^{2}$. Basically, two different families of $AlGaN/GaN-on-Si\ MIS-HEMTs$ devices were fabricated on commercial 4 $inch$ wafers: (i) using a thin $ALD\ HfO_2$ (deposited on the CNM clean room) and (ii) thin in-situ grown Si_3N_4, as a gate insulator (grown by the vendor). The scientific impact of this PhD in terms of science indicators is of 17 journal papers (8 as first author) and 10 contributions at international conferences.

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This thesis has been carried out during my stay at $IMB - CNM - CSIC$ from October 2009 to July 2013. In the framework of two collaborative projects, the most part of the device fabrication work has been performed at the Centre de Recherche sur l'Hétéro-Epitaxie (Centre National de la Recherche Scientifique) ($CRHEA - CNRS$). Analogously, high-voltage $HEMT$ devices have been developed in a collaborative industrial project with ON semiconductor at the CNM.

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Chapter 1

Introduction

1.1. Motivation

Power electronics plays a key role in the generation-storage-distribution cycle of the electric energy. This is because the main portion of the generated electric energy is consumed after undergoing several transformations, many of them carried out by power electronic converters. Examples of this can be found in all ranges of power levels (from a few watts to mega-watts), and they include many types of different equipment (power supplies for computers, industrial and telecommunication systems, domestic appliances, motor drives, industrial converters and others). The largest portion of the power losses in these power electronic converters are dissipated in their power semiconductor devices.

Nowadays, these devices are based on the mature and very well established silicon (Si) technology. However, Si exhibits some important limitations regarding its voltage blocking capability, operation temperature (T) and switching frequency. Therefore, a new generation of power devices must be developed for power converters in applications where converters based on traditional Si power devices cannot operate. The use of these new power semiconductor devices will allow increasing the efficiency of the electric energy transformations achieving a more rational use of the electric energy.

Novel and innovative power devices based on wide band gap (WBG) semiconductors can play a main role in energy efficient systems. Among the possible candidates to be the base materials for these new power devices, silicon carbide (SiC) and gallium nitride (GaN) present the better trade-off between theoretical characteristics (high-voltage blocking capability, high-temperature operation and high-switching frequencies) and real commercial availability of the starting material (wafers) and maturity of their technological processes. GaN process technologies are becoming very mature and, therefore, attractive from the device manufacturer's perspective, especially for high-power and high-temperature electronics.

The backbone of the electronics market, the semiconductor industry generates revenues of $\sim \$250\ B$ annually and is undoubtedly one of the most important and innovative electronics market segments.[1] The total market for semiconductor devices (discretes, modules and integrated circuits (ICs)) dedicated to the power electronics industry has reached $\sim \$20\ B$ in 2012.[2] Already well established in the market, Si insulated gate bipolar transistors ($IGBTs$) account for $\sim \$1.6\ B$ in the medium to high-voltage range. It has been estimated that the super junction metal oxide semiconductor field effect transistor ($SJ - MOSFET$) market reached $\sim \$567\ M$ by the end of 2012, according to the Yole Développement market research.[2] The radio frequency (RF) components market for consumer electronics was valued at $\sim \$6\ B$ in 2011 and is expected to reach $\sim \$17\ B$ by 2017 at an estimated compound annual growth rate ($CAGR$) of 19.4% from 2012 to 2017. The demand of RF components is due to the launch of new devices which contains advance features such as virtual communication, haptics reorganization from a distance and so on.[3] Regarding the optoelectronic market, Navigant research forecasts that annual revenue from light emitting diode (LED) lamps will grow from just over $\sim \$1.5\ B$ in 2013 to more than $\sim \$8.5\ B$ in 2021.[4]

In this context, the overall GaN market revenue (including both, power and optoelectronic segments) stood at $\sim \$240\ M$ in 2011 globally, (non-optoelectronic GaN device market was just $\sim \$75\ M$ in 2010)[5] which is expected to cross $\sim \$350\ M$ by the end of 2012.[6] Among the potential application sectors for $GaN - based$ devices, the largest shares are occupied by the consumer electronics sector (due to $LEDs$ and lighting), information and communication technologies (ICT) (due to RF), and industrial, power, solar and wind sector (due to power applications), together grabbing

roughly 70% of the market currently with numerous upcoming applications such as consumer lighting, RF amplifiers, RF switching devices, power factor correction systems, power distribution systems, smart grid, high voltage direct current ($HVDC$), industrial motor drives, solar panels, photovoltaic inverters, wind power systems, and so on. The fast growing and upcoming application sectors are automotive and military, defense and aerospace sectors, with upcoming application fields such as electric and hybrid electric vehicles ($HEVs$) in the former and electronic warfare, radar communication electronics in the latter.[6]

In the short term, international rectifier and efficient power conversion corporation (EPC) remain the two main vendors of GaN power devices in early 2012. The market is likely to stay below ~ \$10 M for devices in 2012, with the rest being made through $R\&D$ sales.[7] The optimistic projection of Lux research's from, "Beyond Si: Plotting GaN and $SiC's$ path within the ~ \$15 B power electronics market," reports the project the market for discrete power electronic components in these industry segments will reach ~ \$15 B in 2020, and SiC and GaN devices will account for ~ \$3.3 B, 22% of the total.[8]

GaN can offer better high-frequency and high-voltage performances, but the availability of good quality large area self-standing (or homoepitaxial) substrates is a disadvantage for vertical devices. Among all the potential GaN devices, heterostructure field effect transistors ($HFET$) or high electron mobility transistors ($HEMTs$) based on the gallium nitride aluminum and GaN ($AlGaN/GaN$) material system have demonstrated an order of magnitude better power handling capabilities than Si or gallium arsenide ($GaAs$) for RF power and high-voltage switching applications. Recently, there has also been interest in the use of GaN $HEMTs$ for robust low-noise applications, high-voltage switching applications, and high-temperature digital applications, owing to the superior properties of this material.

To date, the main effort on GaN electronics has been focused towards depletion mode ($D-mode$) devices. The enhanced mode ($E-mode$) devices, which are much more difficult to implement, are attractive for low power digital applications, for $normally-off$ power switches as well as for high-efficiency RF applications. Integration of $E-mode$ and $D-mode$ devices on the same circuit would enhance the functionality of GaN integrated circuits.

The social, academic and industrial interest is therefore very remarkable for the $GaN\ HEMT$ devices and is in this scenario that I have been working towards my PhD. The first milestone has been the establishment the $know-how$ on $GaN\ HEMT$ technology from several points of view: the device design, the device modeling, the process fabrication and the advanced characterization primarily using devices fabricated at the Centre de Recherche sur l'Hétéro-Epitaxie and Centre National de la Recherche Scientifique ($CRHEA-CNRS$) in the framework of a collaborative project. A relevant objective of my thesis was also to merge the nanotechnology approach with the conventional characterization techniques at the device scale to understand the device performance. In addition, full characterization methods as automatic wafer maps test have been accomplished to obtain a preliminary idea of the yield. Besides you will find the main experimental results of a collaborative industrial project with ON semiconductor and Centre Nacional de Microelectrònica (CNM). I've been paid primarily to work in this project but due to non-disclosure agreements the amount of information coming out of this is a relatively small part of the dissertation.

1.2. ORGANIZATION AND STRUCTURE OF THE DOCUMENT

Table 1-1 presents an overview of each chapter. My dissertation describes the advanced design, fabrication and characterization of $AlGaN/GaN\ HEMTs$. $Chapter$ 1 and 2 are introductory. $Chapter$ 3 presents methods and materials. $Chapter$ 4 and 5 are devoted to the optimization and understating of the Ohmic and gate contact, respectively. In $chapter$ 6 we evaluate the performance of the $HEMT$ in high-voltage and high-temperature ambient. $Chapter$ 7 is a review of the $normally-off$ strategies.

Further in detail, in the $chapter$ 1, the thesis motivation and outline is presented in order to give to the reader a widely point of view of the aims of this project and the milestones to achieve.

In the $chapter$ 2, a review of GaN material history, material properties and a list of $GaN-based$ devices applications is presented. In addition, GaN properties such as the piezoelectric and spontaneous polarization fields and two dimensional electron gas ($2DEG$) formation in the $AlGaN/GaN$ heterostructure is widely described. Finally, the principle of $HEMT$ operation and a summary of the $GaN-based\ HEMTs$ applications are presented.

$Chapters$	$Title$	$Key\ words$
1	$Introduction$	$Thesis\ motivation, outline\ and\ structure.$
2	$Why\ AlGaN/GaN\ HEMTs?$	$GaN\ history\ and\ properties.$ $HEMT\ device, operation\ and\ applications.$
3	$Fabrication\ and$ $Characterization\ Overview$	$Fabrication\ process.$ $CRHEA\ and\ CNM - ON\ semiconductor\ HEMTs.$ $Characterization\ method.$
4	$AlGaN/GaN\ HEMT$ $Ohmic\ Contact$	$Ohmic\ contact.$ $HEMT\ vs\ Implanted.$ $Spiking\ Mechanism.$ $Au - free\ contacts.$
5	$AlGaN/GaN\ HEMT$ $Gate\ Contact$	$Schottky\ gate.$ $HEMT\ vs\ MIS - HEMT.$ $Dynamic\ I - V.$ $Gate\ traps\ characteristics.$
6	$AlGaN/GaN\ HEMT$ $High - Voltage\ and$ $High - Temperature$	$ON\ semiconductor\ Power\ HEMTs.$ $R_{on,sp}\ vs\ V_B.$ $High\ Temperature\ behavior.$
7	$AlGaN/GaN\ HEMT$ $Normally - off\ Strategies$	$Normally - off\ state - of - the - art\ .$ $AlGaN\ barrier\ thining\ TCAD\ simulations.$ $Hybrid\ MOS - HEMT\ Modeling.$
8	$Conclusions\ and\ Future\ Lines$	$Suggestion\ for\ future\ work.$
9	$Appendix\ A$	$Publication\ list\ of\ the\ author.$
10	$Appendix\ B$	$List\ of\ acronyms.$
11	$Appendix\ C$	$List\ of\ symbols.$

Table 1-1. Quickly view of the chapter contents.

In the $chapter\ 3$, the $AlGaN/GaN\ HEMTs$ (on Si, $sapphire$ and $Free-Standing\ GaN\ (FS-GaN)$) fabrication process and physical and electrical characterization methods are presented. Regarding gate architecture, three types of devices are fabricated and investigated during this thesis, $HEMT, i-HEMT$ and $MIS-HEMT$. Finally, we present nano-electronics methods that are the key of our advanced characterization, such as focused ion beam (FIB), atomic force microscopy (AFM) and conductive $(CAFM)$ of the $AlGaN/GaN\ HEMTs$.

In the $chapter\ 4$, the fundamentals of the Ohmic formation are discussed. A conventional Ohmic contact to bulk GaN is investigated through the temperature dependence study of Al/Ti contacts to $Si\ \ Implanted\ N^+\ GaN - on - sapphire$. Next, the submicron features of a typical $Ti/Al/Ni/Au$ Ohmic contact to $AlGaN/GaN$, with a reduced contact resistance (R_c) of $0.2\ \Omega mm$, are investigated in detail, to understand the conduction mechanisms. Moreover, $Au-free$ contacts characteristics are investigated. The $GaN-on-Si$ wafers allow the highly production of $AlGaN/GaN\ HEMTs$ in some of the many complementary metal oxide semiconductor $(CMOS)$ fabs, traditionally used for the processing of Si devices. A R_c map comparing $Au-$

$free$ and Au content contacts, further corroborates the relevant role of gold in the achievement of low resistance to the $2DEG$ at the $AlGaN/GaN$ interface.

In the $chapter$ 5, the fundamentals of the $AlGaN/GaN$ $HEMT$ on Si gate stack are discussed. It is investigated the Ohmic and Schottky currents at the micro and nanometric scale. This included current *vs* voltage characteristic curve $(I\text{–}V)$, transmission line method (TLM) and a range of physical analysis tools including scanning electron microscopy (SEM), FIB and transmission electron microscopy (TEM). In particular, the nanoscale features of the Schottky contact to an $AlGaN/GaN$ $HEMT$ are investigated in detail by means of the $CAFM$ technique. Afterwards, It is presented a compact set of analytical closed-form expressions for the computation of the drain current, the transfer current and the transconductance of $AlGaN/GaN$ $HEMTs$. On the other hand, the impact of introducing a thin gate dielectric in these devices is investigated; by modifying the previous model this being the basis of a $MIS-HEMT$ device. It is numerically investigated the drain current, saturation current and transconductance properties of a $MIS-HEMT$ using silicon oxide (SiO_2), silicon nitride (Si_3N_4), $sapphire$ (Al_2O_3) and hafnium oxide (HfO_2) as gate insulators. The experimental results on $MIS-HEMT$ and passivated Schottky gate $i-HEMT$ structures are comparatively studied under bias and temperature stress conditions. Finally, the gate trap properties of $HEMT$ and a $MIS-HEMT$ are analyzed by means of the C/G vs ω techniques (conductance analysis).

In the first part of $chapter$ 6, the main results of the $AlGaN/GaN$ $HEMTs$ power switches fabricated at the clean room of the CNM are presented in the framework of the industrial contract with ON semiconductor. The extensive characterization of our $AlGaN/GaN$ $HEMTs$ devices is done by means of DC characterization ($On-state$ and $Off-state$), DC wafer mappings, reverse and breakdown voltage (V_B) in $Galden\ bath$ and $high-T$ stress. Basically, two different families of $GaN-on-Si$ $AlGaN/GaN$ $MIS-HEMTs$ devices are fabricated on commercial 4 $inches$ wafers: (i) using a thin atomic layer deposition (ALD) HfO_2 (deposited on the CNM clean room) and (ii) thin in-situ grown Si_3N_4, as a gate insulator (grown by the vendor). The large area/large current devices can be defined with both gate architectures in spite that the $Au-free$ contact complementary metal oxide semiconductor ($CMOS$) compatible results in higher on-resistance (when compared with traditional $HEMTs$).

In the second part of $chapter$ 6, it is reported the elevated T impact on the forward and the reverse leakage currents for analogous Schottky gate $HEMTs$ grown on different substrates: Si, $sapphire$ and $FS - GaN$. These devices are fabricated in the clean room of the $CRHEA - CNRS$. A gate insulator also has a relevant impact on the T behaviour of a $HEMT$ device. A MIS gate architecture can be very effective in suppressing both the drain and gate off-state leakage. Finally, preliminary high-temperature reliability stability assessment of the $ALD\ HfO_2$ device is presented.

In the $chapter$ 7, we make a critical review of the several approaches for converting the $AlGaN/GaN\ HEMTs$ from the conventional $normally - on$ mode ($D - mode$) to the desired $normally - off$ mode ($E - mode$). Several techniques for the $normally - off$ operation have been reported so far, such as using a thin $AlGaN$ barrier, a recessed gate structure, a fluoride-based plasma treatment, a $p - type$ gate structure or using a non-polar $a - plane$ channel. In order to know the recess gate capabilities for converting the $AlGaN/GaN\ HEMTs\ D - mode$ to $E - mode$, it has successfully simulated a $HEMT$ with a recessed gate, obtaining a shift towards $normally - off$ behavior with the thinning of the $AlGaN$ barrier. Finally, we propose an analytical model for the hybrid $AlGaN/GaN\ HEMT$.

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Chapter 2

Why AlGaN/GaN HEMTS?

2.1. INTRODUCTION

As microelectronic loads proliferate and the desire for high-performance as well as mobile computing accelerates, there is an increasing demand for high-density power conversion solutions. At the same time, social and economic pressures are mounting to increase the power delivery efficiency. Of course, these two performance metrics, efficiency and density are in conflict. As $Si - based$ technology is reaching maturity, a truly revolutionary change in this performance trade off requires that a fundamentally new power device technology platform be introduced. In this sense, $GaN - based\ HEMT$ devices will be presented as the improved technology.

The $AlGaN/GaN\ HEMTs$ have been demonstrated a great potential in the field of high-power, $high - T$ and high-frequency electronics. The performance advantages of $HEMTs$ power devices over the incumbent Si based alternatives derives mainly from two fundamental characteristics. The first is the inherently lower specific on-resistance $(R_{on,sp})$, due to the higher majority carrier electron mobility (μ_n) in the $HEMTs$ $2DEG$ and the smaller source-drain spacing of the $HEMT$ for a given operating voltage capability, made possible by the WBG nature of the materials involved. Due to their WBG, $AlGaN/GaN\ HEMTs$ are also excellent candidates for high-power and

high-frequency applications at elevated temperatures.[1,2] The second is the significantly lower switching charge due to the reduced terminal overlaps present in the lateral $HEMT$ structure compared to the vertical Si device, as well as the shorter gate length, also due to the higher field withstand capability of the WBG structure. The combination of these inherent advantages leads to revolutionary improvements in performance of power conversion circuitry, which utilizes $GaN - based$ power devices.

In recent years, $GaN - based\ HEMTs$ have attracted great attention due to their impressive maximum frequency of oscillations, low $R_{on,sp}$ and remarkably high V_B.[3-5] Since the demonstration of the first $GaN - based\ HEMT$ switches, impressive progress has been made in the development of these devices.[6] The solid-state switch $V_B/R_{on,sp}$ trade-off already outperforms the best-in-class Si equivalent (such as super-junction devices), rapidly approaching the SiC theoretical limit.[4,7]

With very high-mobility, fewer carriers are required to achieve these low conduction losses which translates into low charge and low switching losses as well. Overall, there is a virtuous combination of material properties adding to superior efficiency, density and (with commercialization hurdles conquered) cost for power conversion solutions. The unique combination of the high-breakdown field, the high-channel electron mobility of the $2DEG$ (μ_{2DEG}), and $high - T$ of operation has attracted enormous interest from academia and from industry.

In this chapter, a brief history of the GaN technology will be introduced describing the main milestones from the pioneering work of Juza *et al.*[8] investigation in 1938. Nowadays, four basic ($Si, sapphire, SiC\ and\ FS - GaN$) substrates for GaN epitaxial growth have been used in $AlGaN/GaN$ fabrication process. A detailed comparison will be presented in this section between these substrates.

Then, the material and electric properties of GaN will be introduced and compared with other commonly used semiconductors as $Si, GaAs\ and\ SiC$ from the literature. In addition, a summary of the $GaN - based$ market applications will be presented in this section. Regarding the GaN material properties, the GaN crystal wurtzite structure and gallium face ($Ga - face$) polarity will be explained. In addition, both piezoelectric and spontaneous polarization dipoles in the $AlGaN/GaN$ heterostructure grown $c - plane$ in a $Ga - face$ crystal will be described. Moreover, we will explain the $2DEG$

formation in the $HEMT$ channel due to the carrier accumulation along the heterojunction in a quantum well using the band diagram of the $AlGaN/GaN$ heterostructure.

In addition, the basic $GaN-based\ HEMTs$ principles of operation will be describe in terms of Ohmic and Schottky contacts biasing and the current flow through the $2DEG$ formation in the $AlGaN/GaN$ heterostructures. The $GaN\ HEMT$ devices, with a wider bandgap than Si have much higher critical field. Together with high-carrier concentration and high-mobility, GaN devices have attracted most attention with impressive trade-off between $V_B/R_{on,sp}$ rating. The development of high-power $AlGaN/GaN\ HEMTs$ devices has progressed extraordinarily rapidly over the last few years and commercialization of devices and circuits based on this technology is now a reality. This is favored by the fact that $GaN-on-Si$ wafers (up to $8\ inch$) are commercially available from several vendors, with buffers capable of withstanding high-voltages.

2.2. A BRIEF HISTORY OF GaN

Early reports on GaN are dated from 1938 by Juza and Hahn[8] by passing ammonia over liquid gallium at elevated temperatures reported the first synthesis of GaN. In 1968, a first report on hydride vapor phase epitaxy ($HVPE$) approach to grow centimeter sized GaN layers on $sapphire$ substrates was released.[9] All GaN films grown at that time showed very high-electron concentrations ($1.0 \times 10^{20} cm^{-3}$) even without intentional doping. The responsible $n-type$ donors were believed to be nitrogen vacancies, a concept that has caused a lot of controversy over the years.

Eventually, oxygen has been proposed as the responsible donor. In order to create a $p-n-junction$ a suitable $p-type$ dopant was required. Despite these difficulties Pankove *et al.*[10] achieved the first $GaN\ LED$ in 1971. Although $Mg-doped$ devices ($GaN{:}Mg$) were much brighter than their $Zn-doped$ equivalents, they were never very efficient ($< 1\%$) and no successful commercial LED was viable.

Nevertheless, $Mg-doping$ has remained in the basis of all current commercial $GaN-based\ LEDs$ and laser diodes (LDs). In the late $1970s$, GaN research virtually ceased because of the continuing difficulties encountered with the growth of high-quality films needed for device development. Remaining issues were the choice and

availability of a suitable substrate, how to control the very high-intrinsic $n - type$ conductivity, and difficulties with obtaining conducting $p - type$ GaN films.

The situation changed dramatically in 1986 when Amano *et al.*[11] reported high-quality GaN films grown by metal organic chemical vapor deposition ($MOCVD$) on $sapphire$ substrates through the use of a low temperature aluminum nitride (AlN) nucleation layer (NL). It was in 1989 when eventually was found a high-performance conducting $p - type$ GaN films.[12]

Those breakthroughs result in an absolute boom of the GaN applications in the early $1990s$. The definitive impulse was achieved in 1991 when Khan *et al.*[13] reported the first evidence of the spontaneous formation of the $2DEG$ at the interface of $AlGaN$ and GaN.The first GaN metal semiconductor field effect transistor ($MESFET$) and $HFET$ were reported in 1993 and 1994, respectively by Khan *et al.*[14,15] In 1993, Nakamura *et al.*[16] demonstrated the first high-brightness blue double-heterostructure GaN $LEDs$.

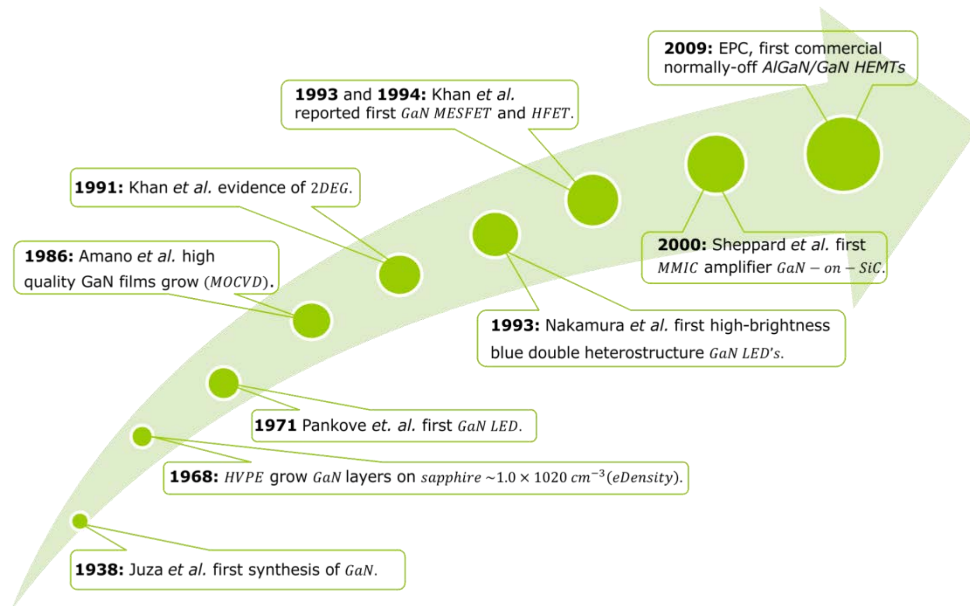

Figure 2-1. Milestones of $GaN - based$ material and devices.

Since these giant steps in material and device development, both research and commercial GaN activities have gained enormous attention $GaN - based$ optical applications have first reached the stage of commercialization while microwave high-power electronics are on the verge of their commercial breakthrough, as presented in the figure 2-1.

Very recently the power device community has shown a strong interest in the new devices implemented in GaN. The GaN power devices have already demonstrated to have better performances that the state-of-the-art Si power devices in terms of $V_B/R_{on,sp}$ characteristics. Also it was firmly demonstrated that, after crystal growth advances, $GaN-on-Si$ is a plausible commercial option. The $GaN-on-Si$ definitively opens the door of this technology to the commercialization. Adapted from Kikkawa *et al.*[17] and Yole Développement,[18] in the table 2-1 is presented a short application list of $GaN-based$ devices (some commercial devices are already in the market).[19-22]

Type	*GaN Devices*	*Area*	*Applications*
Optoelectronics	*LEDs*	*Smart lighting*	*Mobile backlighting* *Traffic signals* *Displays panels* *Illumination* *UV detectors*
	Blue Laser diodes	*ICT*	*Data storage (Blue Ray)* *Display Laser TV & Screens*
Microelectronics	*AlGaN/GaN HEMTs*	*ICT Radio Frequency Electronics*	*Telecom base stations* *WiMAX* *4G or Long Term Evolution* *Radar* *Space Electronics com.* *Fixed wireless com.* *Interbase station com.*
		Power management	*Power Correction Systems* *PC AC Adapters* *Hybrid/Electric Vehicle* *Electronic appliances*
		Power Industrial	*Factory Automation* *Railway* *Motor control* *DC/AC; DC/DC inverters*
		Energy Generation & Distribution	*Photovoltaic generation* *Photovoltaic inverters* *Smart Grid* *High Voltage Direct Current* *Wind Power*

Table 2-1. Target applications of $GaN-based$ devices.

This table has been split in two main solid-state semiconductor fields: *optoelectronics* and *microelectronics*. The most relevant $GaN-based$ electronic devices such as $LEDs$, blue LDs and $AlGaN/GaN$ $HEMTs$ have been assigned to different areas to

enumerate the main potential applications. Among the wide range of potential application areas we have included the smart lighting, ICT, RF electronics, power management, power industrial and energy generation and distribution.

The figure 2-2 illustrates the main $AlGaN/GaN$ $HEMTs$ devices applications fields.

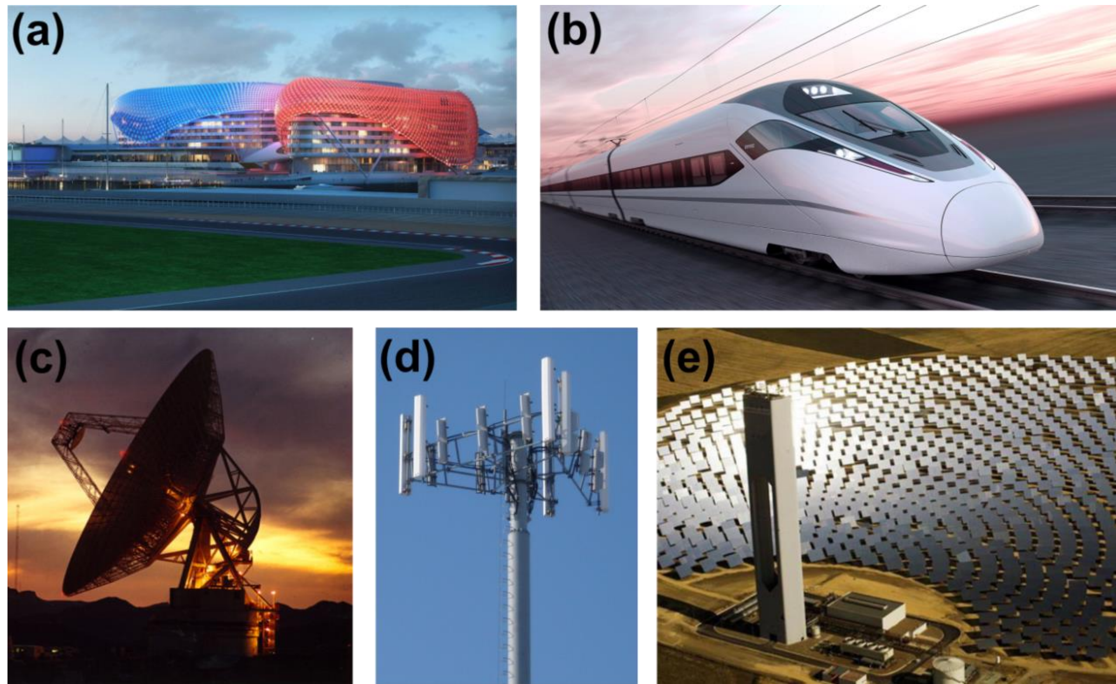

Figure 2-2. Different $AlGaN/GaN$ $HEMTs$ applications. (a) Solid state lighting using ($LEDs$) (in the photograph The Yas Hotel in Abu Dhabi).[23] (b) Power electronics conversion (such as high-speed railways).[24] (c) RF (high cut-off frequency, L, S, C, X and Ku) as radar.[25] (d) ICT (information and communication technologies) applications as mobile phone base stations.[26] (e) Smart energy generation as the photovoltaic inverter circuits applications in a solar concentrating photovoltaic plant.[27]

2.3. GaN MATERIAL PROPERTIES

It is generally assumed that the new generation of power devices for power converters will be based on the WBG semiconductors such as SiC or GaN. The material advantages allows use the WBG of the $GaN-based$ devices to replace traditional Si power switches. The use of the GaN power semiconductor material will allow increasing the efficiency of the electric energy transformations for a more rational use of electric energy thus reducing carbon footprint.

In the table 2-2, the main material and electric properties of GaN have been introduced and compared with other commonly used semiconductors form literature.[9,28-35]

Parameter	Symbol	Units	Si	GaAs	SiC	GaN
Bandgap energy	E_g	eV	1.12[1]	1.43[2]	3.26[1]	3.39[2]
Critical electric field	E_{crit}	V/cm	3.0×10^5	6.5×10^5	2.0×10^6	3.3×10^6
Optical Phonon Energy	$\hbar\omega_O$	meV	62.9	33.2	95.0	91.2
Dielectric constant	ε_r	ε_0	11.7	12.5	10	8.9
Bulk electron mobility	μ_B	cm^2/Vs	1450	6000	720	900
Saturation drift velocity	v_{sat}	cm/s	1.0×10^7	1.3×10^7	2.0×10^7	2.5×10^7
Thermal conductivity	k	W/mK	148	50	400	260
Intrinsic carrier density	n_i	cm^{-3}	1.5×10^{10}	1.8×10^6	8.2×10^{-9}	1.9×10^{-10}
Johnson's FM High f.	JM	$(E_c v_{sat}/2\pi)$	1	7.1	180	760

Table 2-2. The material and electrical properties of GaN and other semiconductors.

From table 2-2 both GaN and SiC have a large bandgap energy which results in high-breakdown electric field ten times lager when compared to Si which naturally enables the high-voltage applications. Also, it leads to low intrinsic carrier generation at $high-T$. These parameters allow $GaN-based$ devices having the potential to operate at higher temperatures, at higher switching frequencies and due its WBG they are radiation hard semiconductors, thus improving upon many of the limitations associated with Si electronics.

On the other hand, GaN and SiC bulk presents lower electron mobility values than Si. For the $GaN-based$ devices, this lack is mitigated by the $2DEG$ formation at the $AlGaN/GaN$ heterostructure with high sheet carrier concentration $(n_s) \sim 1.0 \times 10^{13} cm^{-2}$ and very high electron mobility $(\mu_n) \sim 1600-2000\ cm^2/Vs$ compared to the value of the bulk GaN. This is the key advantage to understand $GaN\ HEMT$ devices. In the next section this will be explained widely.

The heat is the one of most important inconvenient that appear in the electronic devices. For this reason the capability to conduct the heat in a semiconductor material is described by the thermal conductivity (k). Usually, the traditional semiconductors are poor thermal conductors, in particular $GaAs$. Beyond, the GaN is comparable with Si, which is the best of the conventional semiconductors and SiC is an excellent thermal conductor. The typical values of k given in the literature are 148 W/mK for the Si, 35 W/mK for $sapphire$ and 160 W/mK for GaN. It is worth mentioning that, this

[1] In the table 2-2 bandgap energy as indirect gap.
[2] In the table 2-2 bandgap energy as direct gap.

value rises up to 400 W/mK for SiC, but the ultimate substrate is diamond, with the highest thermal conductivity of 2200 W/mK among materials. Device oriented polycrystalline diamond k is typically $3-4$ times that of SiC, though. However, it has been suggested that GaN bulk thermal conductivity would be greater than what is currently generally accepted. Recently, it has been reported bulk GaN thermal conductivities larger than 260 W/mK (the theoretical value for k would be as high as 410 W/mK), which suggests the $FS-GaN$ an interesting alternative to the excellent (but otherwise prohibitively expensive yet) SiC substrates.

These material properties make $GaN-based$ devices excellent candidates for the next generation of highly efficient and eco-friendly electronic power devices.[36,37] Table 2-3 presents a comparison of the main substrate properties for the GaN growth ($Si, sapphire, SiC\ and\ FS-GaN$).

Substrate properties	Symbol	Units	Si	sapphire	SiC	GaN
$Lattice\ constant$	a_0	Å	3.846	4.758	3.081	3.189
$Lattice\ mismatch$	$a_0/a_{0,GaN}$	%	-17	-33	3.5	0.0
$Thermal\ exp. coef.$	α_T	K^{-1}	2.6	7.3	4.5	5.6
$Thermal\ mismatch$	$\alpha_T/\alpha_{T,GaN}$	%	116	-23	24	0.0
$Thermal\ conductivity$	k	W/mK	148	35	400	260[3]
$Wafer\ size$ (2012)		$inch$	8	6	4	2
$Price$			low	$medium$	$very\ high$[4]	$very\ high$[5]

Table 2-3. Comparison the substrate properties for epitaxial growth of GaN.[38] (Adapted from Visalli PhD dissertation 2011).

In the table 2-3 the $GaN-on-Si$ available up to 12 $inch$ and demonstrated on 8 $inch$.[39,40] For the $GaN-on-sapphire$ demonstrated on 6 $inch$ and in the near future 8 $inch$.[41,42,43] For the $GaN-on-SiC$ wafer from $CREE$ available up to 6 $inch$.[44] For the $GaN-on-GaN$ 4 $inch$ under development.[45]

2.3.1. GaN MATERIAL STRUCTURE

The group of III-nitride, can crystallize in three crystal structures: wurtzite, zinc-blende and rock-salt. The GaN has two thermodynamically stable phases: cubic and wurtzite phase. After few studies the wurtzite phase, as shown in figure 2-3, was find out as a

[3] In the table 2-3 typical value of the literature is $150-160$ W/mK (i.e., very similar to Si) but recent reports indicate that GaN thermal conductivity is higher than 260 W/mK.
[4] In the table 2-3 SiC starting material increases the price.
[5] In the table 2-3 homoepitaxial GaN substrate still under development.

more suitable phase thanks to the less concentration of defects in the GaN layer.[46] For this reason the $AlGaN/GaN\ HEMTs$ is usually grown on the wurtzite phase.

The wurtzite GaN structure has a hexagonal unit cell and consists of two intercepting hexagonal closed packed sub-lattice. The wurtzite structure is characterized by two unstrained lattice constants a_0 and c_0 (ideal ratio $c_0/a_0 \approx 1.63$)[47] and by the polarity. The a_s constant is the strained lattice constant and c_s constant is the hexagonal strained lattice constant.[48]

The wurtzite GaN crystal has two distinct faces, named as $Ga - face$ (0001) and nitrogen face ($N - face$) $(000\bar{1})$ polarity crystalline faces. The occurrence of $Ga - face$ or $N - face$ depends on the growth conditions. Each sub-lattice is constituted by one type of atoms which are shifted with respect to each other along the c axis by the amount $u_0 = 3/8$ of the unit cell internal parameter in fractional coordinates.

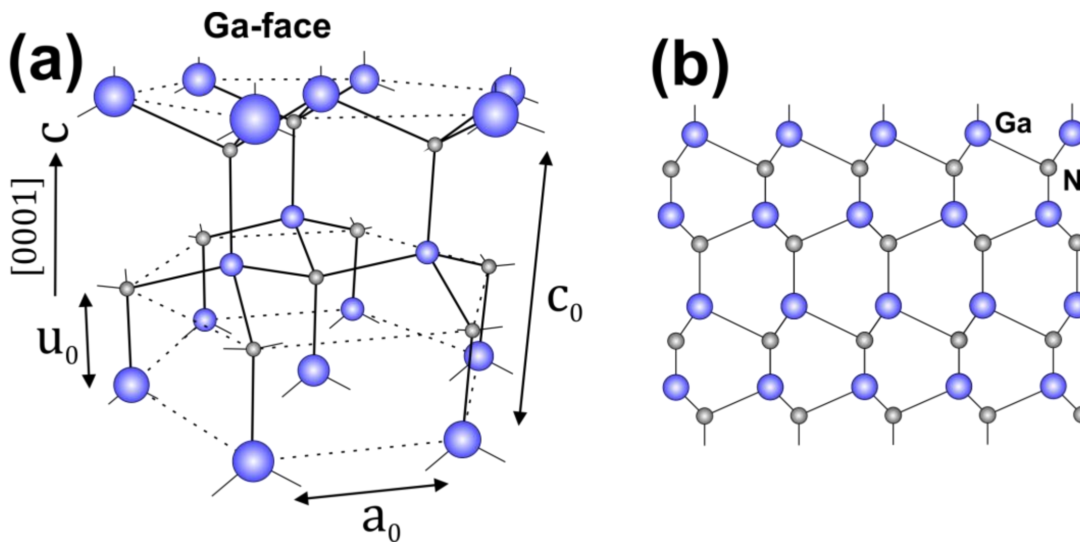

Figure 2-3. Ideal structure of (a) $Ga - face$ in a wurtzite structure and (b) Atomic arrangement of Ga and N atoms net in GaN crystal.

2.3.2. POLARIZATION FIELDS

In the III-nitride group (AlN, GaN and InN) the nitrogen is the element that provides the strong iconicity. In addition, the wurtzite III-nitride does not have inversion symmetry along the [0001] direction. Both facts, results in a strong macroscopic polarization along this axis. The polarization fields in GaN and $AlGaN$ materials[49] play an important role, due to the potential profile and amount of charges induced at the $AlGaN/GaN$ heterostructure. The GaN is a strongly polar material and this polarization takes place in the equilibrium lattice at zero strain due to the lack of symmetry, it is

named a spontaneous polarization (P_s), as shown in figure 2-4, which leads to sheet charge accumulation on the $Ga - face$ crystal of the GaN and $AlGaN$ grown on a $c - plane$.[47,49]

These sheet charges are equal in magnitude and opposite in sign to maintain overall charge neutrality. The $AlGaN$ also has a spontaneous polarization, similar to GaN but of different magnitude (in fact, a function of the aluminum content of the ternary). As a result, there is a discontinuity of the spontaneous polarization vector at the $AlGaN/GaN$ heterostructure. Basic electrostatics states that such a discontinuity results in an interface charge proportional to the polarization difference.

Furthermore, the tensile strain resulting from growing lattice-mismatched $AlGaN$ on GaN results in piezoelectric polarization (P_z), as shown in figure 2-4, field that contributes with the total polarization filed, which give rise to more electrons in the $2DEG$.[47,49]

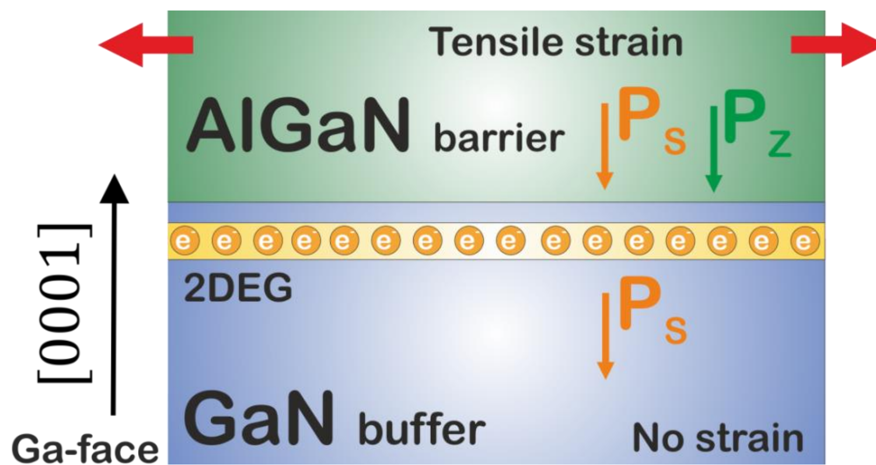

Figure 2-4. Combined piezoelectric and spontaneous polarization dipole in an $AlGaN/GaN$ structure grown on $c - plane$ in a $Ga - face$ crystal.

2.3.3. $2DEG$ $AlGaN/GaN$ HETEROSTRUCTURES

As commented above, GaN and SiC bulk presents lower electron mobility values than Si. For the $GaN - based$ $HEMT$ devices, this lack is mitigated by the $2DEG$ formation at the $AlGaN/GaN$ heterostructure with high-charge density and very high-mobility. The $2DEG$ formation in the $HEMT$ channel is due to the carrier accumulation along the heterojunction in a quantum well.[50] Inside this quantum well, the $2DEG$ channel generated at the interface of an $AlGaN/GaN$ heterostructures, offering high $\mu_n \sim 1600 - 2000\ cm^2/Vs$ and high $n_s \sim 1.0 \times 10^{13}\ cm^{-2}$ (is about ten times as large

as that of Si) without modulation doping. This carrier accumulation is mainly due to spontaneous and piezoelectric polarization charge effect developed along the heterojunction.

These carrier accumulation show enhanced mobility due to significantly reduced Coulomb scattering as they are separated from the top supply layer atoms from which they stem. Moreover, mobility is further enhanced because of strongly reduced impurity scattering as the quantum well resides in the unintentionally doped (UID) material. The enhanced electron mobility is the key feature that differentiates $HEMTs$ from other devices. These features makes the $2DEG\ HEMT$ an unique conductive layer with a reduced sheet resistance (R_{sh}) of $\sim 1/(q\mu_n n_s)$, typically in the range of $200 - 400\ \Omega/sq$.

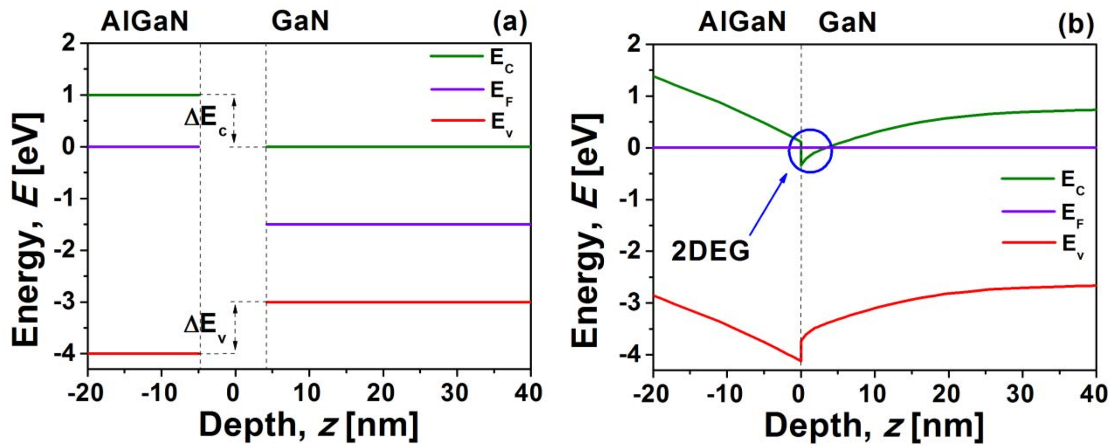

Figure 2-5. Band diagram of the $AlGaN/GaN$ heterostructure (a) $AlGaN$ and GaN semiconductors before their Fermi level alignment and (b) together in thermo-dynamical equilibrium where the $2DEG$ in the $AlGaN/GaN$ interface has been formed.

The principle operation of the $AlGaN/GaN\ HEMT$ device, from a physical point of view, is presented in figure 2-5 from the literature.[51] In the figure 2-5 (a) the $AlGaN$ and GaN semiconductors are separated and the Fermi level (E_F) do not coincide. Then, figure 2-5 (b) shows the band-structure under zero bias (no gate voltage), in this scenario a quantum well is present at the $AlGaN/GaN$ hetero interface, where the bands are bending to achieve a unique E_F. The heterostructure results in the formation of a discontinuity through the conduction band (E_c) and valence band (E_v) of the two semiconductors determines a charge transfer, creating the quantum well. The term $2DEG$ can be described as a condition where the carriers have quantized energy levels in $z - axis$ with the possibility to move in two other directions parallel to the interface.

2.4. THE $HEMT$ DEVICES AND PRINCIPLES OF OPERATION

The $HEMT$ device is basically a three terminal device, as shown in figure 2-6, with two Ohmic ($source$ and $drain$) and one Schottky ($gate$) contacts. The basic principle of operation is explained when the source to drain pads are biased and then the current flow through the device channel by the $2DEG$ electrons. The electron transport is controlled by applying of a bias in the gate pad; it can behave like a switch. The gate voltage necessary to stop the current flow from source to drain is defined as the threshold voltage (V_{th}).

The usually working mode for the $AlGaN/GaN$ $HEMT$ is the $normally-on$ or $D-mode$, that is to say, when the V_{th} is negative (the system needs additional circuit to give negative gate voltage to drive the device). In this mode, for this gate bias condition $(V_g < V_{th})$, the depletion region starts to penetrate into the $2DEG$ and stops the channel, as shown in figure 2-6 (a). However, the current flow through the device without an external gate biasing $(V_g = 0\,V)$. Then the depletion region under the Schottky contact allows the electron transport. In this case the structure is in the thermo-dynamical equilibrium, as shown in figure 2-6 (b).

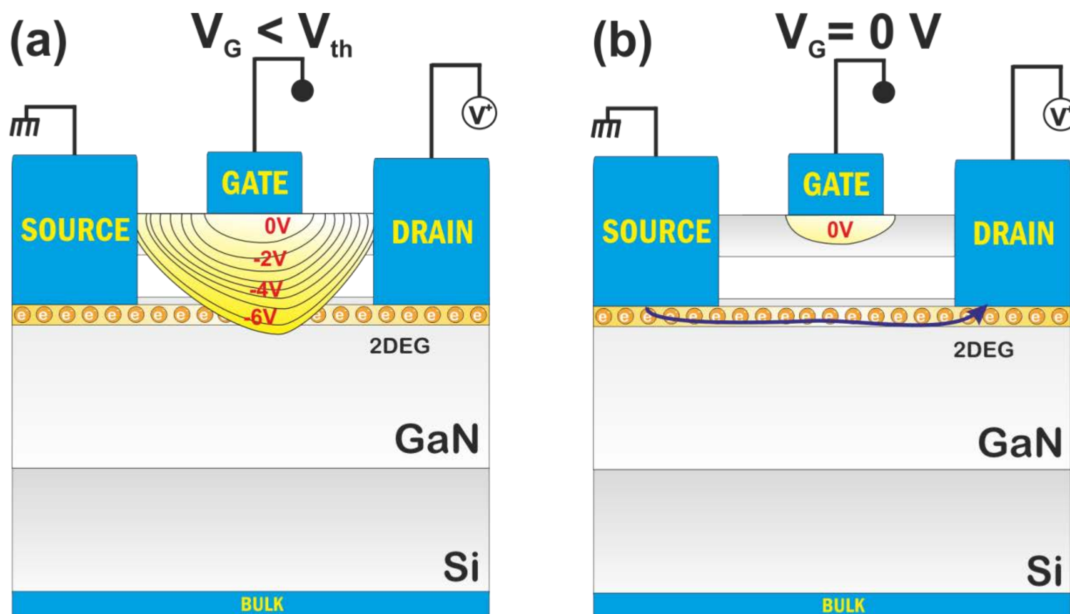

Figure 2-6. $AlGaN/GaN$ $HEMT$ **schematic cross-section (a)** $Off-state$ **and (b)** $On-state$.

2.5. SUMMARY

Why $AlGaN/GaN\ HEMTs$? As $Si - based$ microelectronics technology is reaching maturity, a truly revolutionary performance improvement fundamentally requires the introduction of a new device technology platform. In this sense, $GaN - based$ devices (and particularly $GaN\ HEMTs$) have the potential to make this change possible. Since the demonstration of the first $GaN - based\ HEMT$ switches, impressive progress has been made in the development of these devices. The unique combination of the high-breakdown field, the high-channel electron mobility of the $2DEG$, and $high - T$ of operation has attracted enormous interest from academia and from industry and in this context this PhD dissertation has been made.

To illustrate this impressive GaN technology evolution, it has been reviewed the history of GaN material from the pioneering work of Juza and Hahn (first synthesis of GaN in 1938), the Nakamura's first high-brightness blue double-heterostructure $GaN\ LEDs$ and the first $2DEG\ HEMT$ achievements in early $1990s$ to the apparition of the first generation of $200\ V$ commercial power devices from EPC in 2009.

The GaN material properties have been compared with other commonly used semiconductors such as $Si, GaAs\ and\ SiC$. The GaN crystal wurtzite structure was particularly described. In addition, both piezoelectric and spontaneous polarization dipoles in the $AlGaN/GaN$ heterostructure grown $c - plane$ in a $Ga - face$ crystal have been described. The $2DEG$ formation in the $HEMT$ channel due to the carrier accumulation along the heterojunction in a quantum well using the band diagram of the $AlGaN/GaN$ heterostructure was also briefly described.

These extraordinary material properties are in the basis of the $GaN\ HEMTs$ principles of operation and the current flow through the $2DEG$ formation in the $AlGaN/GaN$ heterostructures. The $GaN\ HEMT$ devices, with a wider bandgap than Si have much higher critical field, higher carrier concentration and higher electron mobility. Their $V_B/R_{on,sp}$ trade-off already outperforms the best-in-class Si equivalent (such as super-junction devices), rapidly approaching the SiC theoretical limit. The $GaN - based$ devices find their place in two of the main solid-state semiconductor fields: $optoelectronics$ and $microelectronics$. The most relevant $GaN - based$ electronic devices such as $LEDs$, blue LDs and $AlGaN/GaN\ HEMTs$ have been assigned to

different areas to enumerate the main potential applications. Among the wide range of potential application areas we have included the smart lighting, ICT, RF electronics, power management, power industrial and energy generation and distribution further suggesting the unprecedent versatility of this material.

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Chapter 3
Fabrication and characterization overview

3.1. INTRODUCTION

In this chapter, the fabrication process and the different characterization methods will be presented. The standard $HEMT$ technology process will be described detailing the three basic steps of micro-fabrication; $HEMT$ isolation, Ohmic and Schottky contact levels. These steps are in the basis of the fabricated $AlGaN/GaN\ HEMTs$ grown on Si, $sapphire$ and $FS-GaN$ in the $CRHEA-CNRS$ and CNM ($Au-free$ devices $CMOS$ compatible) clean rooms.

The $CRHEA-CNRS$ devices were entirely molecular beam epitaxy (MBE) grown in their own epitaxial facilities. In addition to the $AlGaN/GaN\ HEMT$ active layer fabrication process, the GaN buffer and the $AlGaN$ layers were grown by MBE and this process has been described onto Si, $sapphire$ and $FS-GaN$. On the other hand, commercial $AlGaN/GaN$ wafers have been used for the definition of the $HEMT$ devices fabricated on the CNM clean room.

Starting from the basic $HEMT$ structure we have introduced different gate architecture modifications to achieve the $MIS-HEMT$ and $i-HEMT$ devices. The $MIS-HEMT$ is a way to further reduce the gate leakage current introducing a thin dielectric between the gate metal and the GaN surface. Both, thin $ALD\ HfO_2$ and in-situ Si_3N_4 have been used as an insulator. The $i-HEMT$ was achieved by thin chemical vapor deposition (CVD) Si_3N_4 as passivation between gate and drain/source spacing. The $i-HEMT$ structure reduces the leakage current between Ohmic and Schottky contacts and improves the breakdown capabilities.

Finally, we will briefly describe the different types of measurements and physical characterization methods that we have been used to investigate the $AlGaN/GaN\ HEMTs$ and the laboratory facilities and equipment's to characterize our GaN devices. In particular, the AFM tool will be widely described and used to understand the conduction mechanisms through the $AlGaN/GaN$ Ohmic and Schottky contact because the relevance of the results obtained in the framework of this dissertation.

3.2. FABRICATION $AlGaN/GaN\ HEMT$ PROCESS

A summary of the fabricated samples is presented in the table 3-1. The first sets of devices were fabricated at the $CRHEA-CNRS$ clean room with a conventional $gold-based$ gate and Ohmic stack.

	ID	Clean Room	Type	Gate Insulator	Substrates
$Au-Based$	$C02$	$CRHEA$	$HEMT$		$MBE\ GaN-on-Si$
	$C03$	$CRHEA$	$MIS-HEMT$	$CVD\ Si_3N_4$	$MBE\ GaN-on-Si$
	$C04$	$CRHEA$	$HEMT$		$MBE\ GaN-on-sapphire$
	$C05$	$CRHEA$	$HEMT$		$MBE\ GaN-on-FS-GaN$
$Au-Free$	$A04$	CNM	$i-HEMT$[1]		4" $GaN-on-Si\ vendor\ A$
	$A03b$	CNM	$MIS-HEMT$	$ALD\ HfO_2$	4" $GaN-on-Si\ vendor\ A$
	$E08$	CNM	$MIS-HEMT$	$in-situ\ Si_3N_4$	4" $GaN-on-Si\ vendor\ B$

Table 3-1. Summary of the $Au-based$ $(Ti/Al/Ni/Au)$ $HEMTs$ fabricated in the $CRHEA-CNRS$ clean room and the $Au-Free$ $(Ti/W/Al)$ $HEMTs$ fabricated in the CNM clean room during this dissertation.

[1] In the table 3-1 isolation between the gate and source/drain is achieved by $CVD\ Si_3N_4$.

On the framework of the industrial contract with ON semiconductor a basic $AlGaN/GaN$ $HEMT$ technology process has been successfully developed for Si substrate in the clean room of the CNM. This section gives an insight into the standard $HEMT$ technology process, the three basic fabrication steps, device isolation, Ohmic and Schottky contacts. Table 3-1 summarizes the fabricated samples. Three types of gate engineering had been used; three conventional $HEMTs$ $(CRHEA - CNRS)$, one passivated $i - HEMT$ (CNM) and four $MIS - HEMTs$ $(CRHEA - CNRS/CNM)$. The basic substrate is Si, but we have investigated devices on Si, $sapphire$ and $FS - GaN$.

3.2.1. $HEMT$ FABRICATION BASIC PROCESS FLOW

Figure 3-1 presents a cross-sectional image of the three different type of $HEMT$ fabricated, regarding their gate engineering.

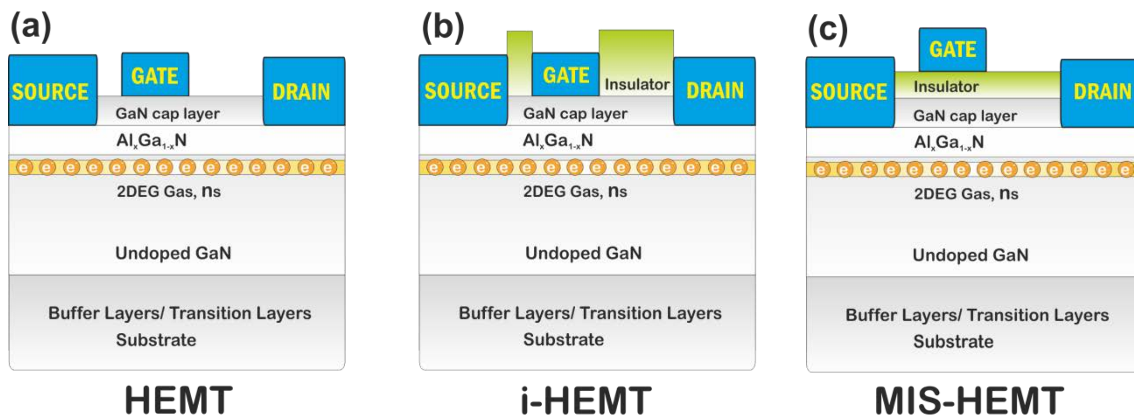

Figure 3-1. Cross section of the fabricated $AlGaN/GaN$ devices for (a) $HEMT$, (b) $i - HEMT$ and (c) $MIS - HEMT$.

Starting from the basic $HEMT$ structure we have introduced different gate architecture modifications to achieve the $MIS - HEMT$ and $i - HEMT$ devices. The $MIS - HEMT$ is a way to further reduce the gate leakage current introducing a thin dielectric between the gate metal and the GaN surface. Both, thin ALD HfO_2 and in-situ Si_3N_4 have been used as an insulator. The $i - HEMT$ was achieved by thin CVD Si_3N_4 as passivation between gate and drain/source spacing. The $i - HEMT$ structure reduces the leakage current between Ohmic and Schottky contacts and improves the breakdown capabilities.

3.2.1.1. EPITAXIAL DEFINITION OF THE GaN BUFFER AND $AlGaN$ BARRIER

In this section, the GaN buffer and $AlGaN$ barrier epitaxial $CRHEA - CNRS$ definition is explained.

3.2.1.1.1. MBE ON Si

Schottky gate $HEMTs$ layers were defined on a previously optimized stack to obtain a crack-free GaN layer up to $2 - 3\ \mu m$ thick on commercial $Si(111)$.[1-3] The GaN buffer and $AlGaN$ barrier layers were grown by MBE using ammonia as the nitrogen precursor in a Riber Compact 21 MBE system on the $CRHEA - CNRS$ facilities. The GaN and Si nucleation layers was basically formed by depositing thin layer of $40\ nm$ of AlN, $250\ nm$ of GaN and $250\ nm$ of AlN grown at $920\ ℃$. These engineered nucleation layers were used to overcome the formation of cracks, which are due to the large difference in the thermal expansion coefficient between GaN and Si. Then, a $1.7\ \mu m$ GaN (0001) buffer was grown on the nucleation layers at $800\ ℃$, followed by the active layers of the $HEMT$. The active layer (for the fabrication of $HEMTs$) consists of a $1\ nm$ AlN spacer to reduce alloy scattering and to enhance the electron mobility,[4] and a $21\ nm$ undoped $AlGaN$ barrier with 0.28 Al mole fraction. Finally, the structure was covered with an additional $5\ nm$ GaN cap layer. The GaN cap layer is used to improve the carrier confinement of the $2DEG$.

3.2.1.1.2. MBE ON $sapphire$ AND $FS - GaN$

Analogously, the $AlGaN/GaN$ layers were grown by MBE on commercial $c - sapphire$ $(\alpha - Al_2O_3)$ and GaN (0001) substrate. Figure 3-1 (a) shown cross section of the fabricated $HEMT$. The $sapphire$ and $FS - GaN$ $HEMT$ hetero-structures also require highly resistive GaN buffer layers to deliver high-power at high-frequencies and to sustain high-breakdown voltages. Here, the growth of a good quality highly resistive buffer is more difficult due the presence of oxygen (and other contaminant species) diffusing from the substrate. The residual concentrations of impurities in the major part of a MBE grown GaN layer on top of $sapphire$ (and $FS - GaN$) are typically below the detection limit of secondary ion mass spectrometry ($SIMS$), low enough to obtain semi-insulating GaN. However, the reduction in threading dislocations (due to the lower lattice mismatches) make it necessary to compensate for the $n - type$ conductivity in

the substrate/GaN interface region, where the GaN layer is often doped with O or Si impurities. One solution involves doping the GaN buffer layer with deep acceptors like iron (Fe), but such an element was not available in the $CRHEA - CNRS$ MBE growth reactor. For this reason, the structure was regrown by MBE (following a procedure as described in Cordier *et al.*[5]) on an iron-doped GaN template obtained by $MOCVD$. By carefully designing the $MOCVD$ GaN template Fe doping profile and by optimizing the MBE regrowth conditions, high-quality highly-resistive GaN buffer layers can be achieved on these $MOCVD$ templates. The $GaN - on - sapphire$ template consists of $4\ \mu m$ thick GaN epilayers grown on 2 $inch$ (0001) $sapphire$ by low pressure metalorganic vapour phase epitaxy ($MOVPE$) in a close-coupled showerhead Thomas Swan reactor with a $3 \times 2''$ capacity graphite susceptor. These templates were doped with Fe using a Cp_2Fe precursor (ferrocene), resulting in good-quality material with a low threading dislocation density ($4 - 8\ \times 10^8\ cm^{-2}$) and with a square resistance of $1.0 \times 10^{10}\ \Omega/sq$.

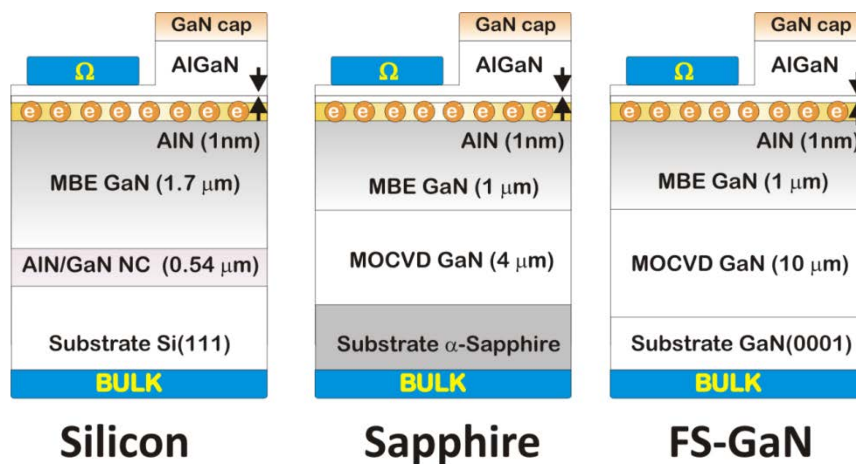

Figure 3-2. Cross-sectional description of the vertical structures under study.

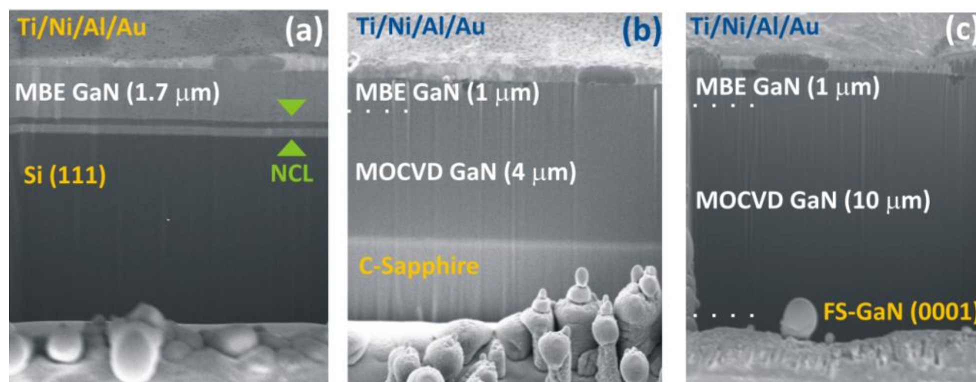

Figure 3-3. SEM micrograph of the different GaN buffers cross-section (a) on Si, (b) on $sapphire$, and (c) on $FS - GaN$. The Ohmic contact of $Ti/Ni/Al/Au$. NL is Si/GaN nucleation layer.

Interface contamination was not detectable with mercury probe capacitance vs voltage ($Hg - CV$) scans. The $Hg - CV$ measurements indicated a residual charge below $1.0 \times 10^{13}\ cm^{-3}$ in the deeper regions of the $MOCVD$ template. To achieve the same residual doping on the $Free\ Standing$ substrate, the $FS - GaN\ MOCVD$ template thickness was increased up to 10 μm thick. The back-side of the substrates was coated with molybdenum in an e-beam evaporator in order to enhance heating and to allow good temperature control during the MBE growth. A 1 μm thick undoped $MBE\ GaN$ buffer was then grown at $780 - 800$ °C (the growth rate for the GaN buffer was 0.6 $\mu m/h$ and no peculiar behavior was noticed by reflection high energy electron diffraction ($RHEED$) observation during the regrowth). The GaN buffer grown on optimized $MOCVD\ Fe - doped$ templates exhibit very low isolation currents with a square sheet resistance of $\sim 5.0 \times 10^{10}\ \Omega/sq$. In the figure 3-2 and figure 3-3 are presented different GaN buffers cross-section on Si, on $sapphire$ and on $FS - GaN$.

3.2.1.1.3. COMMERCIAL $GaN - on - Si$

The devices available from $CRHEA - CNRS$ were basically defined for $RF\ HEMTs$ so the buffer was not optimized for high-voltage operation. For the high-voltage power $HEMT$ fabrication, we have used material 4 $inch$ ($GaN - on - Si$) from two state-of-the-art European suppliers for high-voltage $HEMT$ in the ON semiconductor project framework.

These commercial GaN wafer has been used for the definition of the $HEMT$ devices fabricated on the CNM (that has no epitaxial growth facilities). The clean room facility of CNM includes equipment for micro and nanofabrication processes based on Si, SiC and GaN technology. Its structure allows a highly flexible operation, which makes it especially well-suited for $R + D + I$ projects. The Integrated micro and nanofabrication clean room has a surface of $1{,}500\ m^2$. The clean room is class $100 - 10{,}000$ depending on the areas.

3.2.1.2. $HEMT$ DEFINITION

In this section, we describe the basic fabrication process used for the standard $AlGaN/GaN\ HEMT$devices which consist in three steps, device isolation, Ohmic and Schottky contacts definition.

A. Device Isolation

The device isolation (for $CRHEA - CNRS\ HEMTs$) was achieved by means of a $150\ nm$ deep mesa etch, performed by Cl_2/Ar reactive ion etching (RIE) (figure 3-4 (a)). The mesa isolation was used to isolate the individual devices from each other. Otherwise you would find contribution of the $2DEG$ all over the wafer and your channel would never be able to stop the electron channel flow.

B. Ohmic Contact

This is the best way to ensure best connection to $2DEG$ with the lowest possible resistance. The R_c has been extracted by means of TLM to be as low as $0.2\ \Omega mm$.[6] The analysis of the Ohmic contact will be extensively studied in $chapter\ IV$. As shown in figure 3-4 (b), Ohmic contacts were formed via the deposition of a $Ti/Al/Ni/Au$ stack ($CRHEA - CNRS$), after which the structure was annealed at 750 °C for 30 s. by rapid thermal annealing (RTA) system. For some of the samples, just before the Ohmic metal deposition by sputtering, a short RIE was also performed in order to remove the GaN cap and partially etch away three quarters of the 21 nm $AlGaN$ layer.

C. Gate Contact

Schottky contact is formed between the Ohmic contacts as the electrode which allows controlling the drain current flow. The $HEMT$ gate contact was made with a Ni/Au bilayer ($CRHEA - CNRS$). Figure 3-4 (c) presents the fabricated $HEMT$ following the steps explained above. The analysis of the gate stack will be extensively studied in $chapter\ V$.

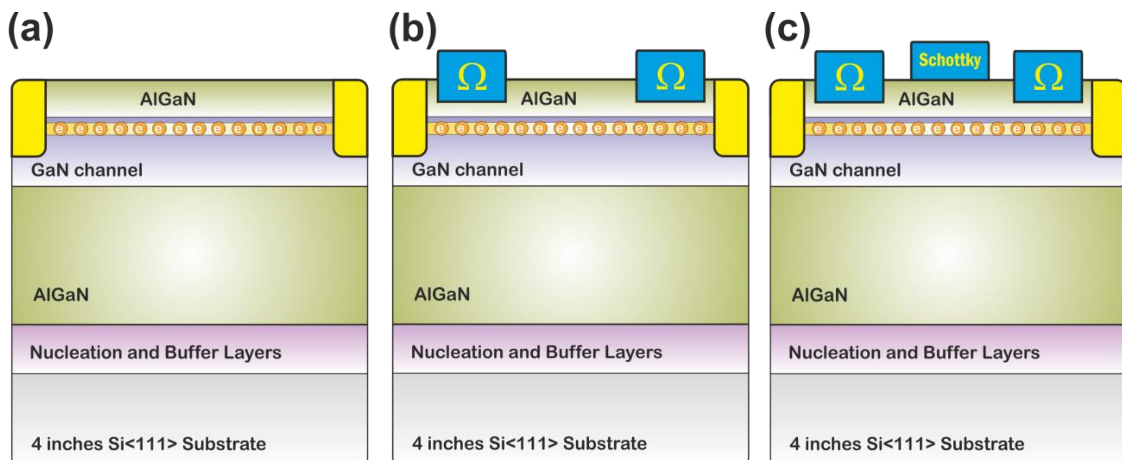

Figure 3-4. Basic $AlGaN/GaN\ HEMT$ fabrication steps (a) isolation (b) Ohmic and (c) Schottky contacts fabrication.

3.2.1.3. $MIS-HEMT$ DEFINITION

As mentioned before, a way to further reduce the gate leakage current is the introduction of a thin dielectric between the gate metal and the GaN surface in an approach known as metal insulated gate $HEMT$ ($MIS-HEMT$) (figure 3-1 (c)). $HEMTs$ were conceived to work in RF application. However, in the framework of the industrial contract with ON semiconductor $HEMTs$ are fabricated for power electronics applications. The main reason to use a thin dielectric under the gate as insulator is to reduce the losses, form the $On-state$, the drain-source voltage must be minimum to obtain a low on-resistance. On the other hand, the $Off-state$ drain-source and gate-source current must be mitigated to obtain a low leakage current and high-breakdown voltage.

3.2.1.3.1. $ALD\ HfO_2\ MIS-HEMT$

The $CNM\ MIS-HEMTs$ were fabricated using an HfO_2 as a gate insulator on 4 $inch$ wafer $AlGaN/GaN-on-Si$ commercial substrates. The thin insulator below the gate metal was achieved by thin $ALD\ HfO_2$. The thin HfO_2 was deposited onto the samples using a $Savannah-200$ ALD system from Cambridge NanoTech Inc. The ALD system is based on precursor wave propagation and is carried out in a small profile chamber at a controlled temperature and vacuum. The system is provided with deionized H_2O or O_3 as oxygen precursors together with tetrakis (dimethylamido) hafnium for HfO_2 deposition. N_2 was the carrier/purging gas.

3.2.1.3.2. IN-SITU $Si_3N_4\ MIS-HEMT$

A further step for improving the robustness of the passivated $HEMT$ is to grow the Si_3N_4 layer epitaxially in-situ just after the $AlGaN$ barrier definition. Thin in-situ Si_3N_4 deposition on $AlGaN/GaN\ HEMT$ structures was recently shown to be feasible and advantageous mainly due to reduced $AlGaN$ relaxation, increased sheet carrier concentration, improved Ohmic contacts and surface protection during processing.[7-10]

The in-situ passivation combined with the GaN buffer optimization yielded extremely low surface (gate) and bulk currents and are purchased directly from a commercial vendor.

3.2.1.4. $Au - free\ CMOS$ COMPATIBLE $HEMT$ DEFINITION

The GaN technology becomes cheaper than other $III - nitride$ materials when it's growth on a Si substrate which the wafers are available in $4 - 6\ inch$. Ideally, the $GaN - on - Si$ based $HEMTs$ can be processed in a standard $CMOS$ compatible line to obtain the same high-throughput and high-yielding process technologies as used for $Si - based$ devices. The Ohmic contacts were formed after annealing a $CMOS$ compatible $Au - free$ metal stack of Ti, Al and W. The gate metal was $W - Al$.[11] The isolation was achieved by N implantation. The passivation of the $i - HEMT$ was achieved by a thin layer of $CVD\ Si_3N_4$. In the CNM clean room, we have demonstrated a fully $CMOS$ compatible GaN process on 4 $inch$ on Si substrates.[12]

3.3. CHARACTERIZATION METHODS

In this section, we will briefly describe the different characterization methods to analyze the $AlGaN/GaN\ HEMTs$. A broad range of measurement has been used to investigate our devices. Well known physical characterization methods have been used for determine the main physical parameters of the structure. Although the physical characterization methods can be regarded as conventional, their applications in the context of the $AlGaN/GaN\ HEMTs$ analysis have been proved to be very innovative and educational for the most of the situations.

Electrical characterization methods include transfer curves, TLM, lateral and vertical leakage currents, forward $I - V$, reverse lateral and vertical leakage currents, reverse breakdown voltage, reliability tests, $dynamic\ I - V$, $C - V$, etc. On the other hand, we will briefly describe the measurement equipment and processing data software. Finally, we will summarize the different types of tests used for measuring the horizontal and vertical buffer and breakdown voltage.

3.3.1. PHYSICAL CHARACTERIZATION

Table 3-2 shown different physical characterization tools used during this thesis to investigate the $AlGaN/GaN\ HEMTs$. The physical characterization methods are addressed to establish the morphology, the composition, the threading dislocations density, the nanoscale conductive pattern and others.

Physical Analysis Tool	*Application*	*HEMT Parameter Extraction*
SEM	*Microscopy Surface*	*Morphology, fabrication verification, yield*
TEM	*Microscopy X − Section*	*Cross − sectional analysis Ohmic contact, GaN Threading Dislocations Density*
AFM	*Nano − topology, Nano − Conductivity*	*RMS, Nanoscale conductive pattern*
EDX	*Composition analysis*	*Identification of metallic compounds*
FIB	*Microscopy X − Section TEM Lamela preparation*	*GaN buffer MBE layer thicknesses*

Table 3-2. Summary of physical analysis tools used to investigate the *AlGaN/GaN HEMTs*.

A number of physical characterization techniques were used during my *PhD* including *CAFM*, *SEM*, *FIB*, *TEM* and energy dispersive x-ray spectroscopy (*EDX*). Some of these techniques were done in collaboration with different laboratories (the *REDEC*, the Servei de Microscòpia, etc.). Among these techniques of particular relevance was *FIB* and *CAFM*.

3.3.1.1. FOCUSED ION BEAM

The *FIB* physical analysis tool has been used to investigate the morphology and the cross-section of the different *AlGaN/GaN* layers.

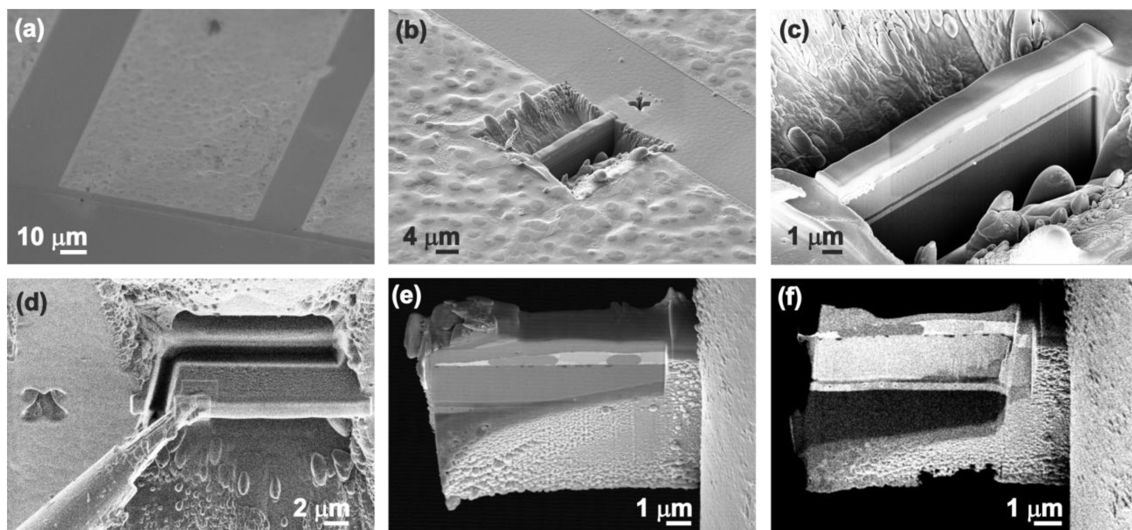

Figure 3-5. *SEM* view of *FIB* machined *TEM* lamella (a) top view of the Ohmic contact before *FIB* mill. (b) *FIB* mill of the Ohmic contact area. (c) Cross-section detail of the lamella with the platinum on the top before the lift-off. (d) Top view of the lamella lift-off. (e) Mounting the lamella on *Cu* holder and (f) Polishing the lamella up to 50 *nm* thick before *TEM* investigation.

The FIB was also used for machining the different TEM lamellas used in this investigation. Figure 3-5 describes the process to obtain a lamella section. Figure 3-5 (a) presents a view of the Ohmic contact. Then in the figure 3-5 (b) is shown a lamella FIB machined from the Ohmic contact area. Cross-section detail of the lamella with the platinum on the top before the lift-off is presented in the figure 3-5 (c) and the top view of the lamella lift-off (figure 3-5 (d)). After mounting the lamella on Cu holder (figure 3-5 (e)) the lamella is polished up to 50 nm thick before TEM investigation have been done as shown in figure 3-5 (f). After conventional TEM analysis, the lamella was wire bonded to the Cu holder to analyze with $CAFM$ the cross-sectional conductive pattern as will be shown in $chapter\ V$.

3.3.1.2. CONDUCTIVE ATOMIC FORCE MICROSCOPY

The other piece of equipment which we have extensively used was the $AFM/CAFM$ setup of the $REDEC$ within the electronic engineering department of the Universitat Autònoma de Barcelona.[13] The AFM is a measuring instrument that belongs to the scanning probe microscopy (SPM) family which, allows obtaining topographical images of a given surface when an extremely sharp tip scans the sample to obtain information about the sample's surface.

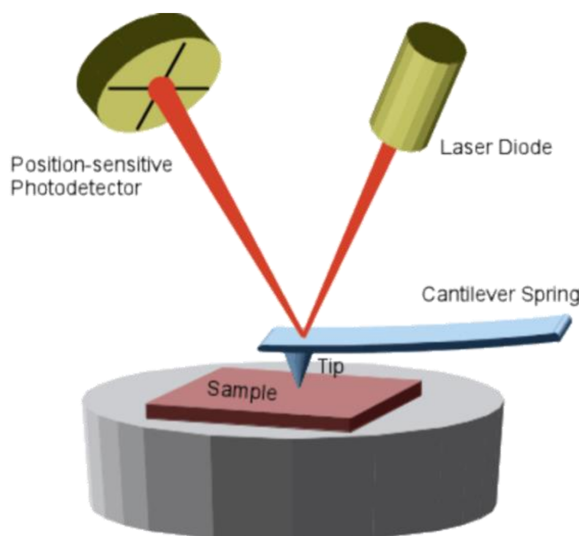

Figure 3-6. Adapted from Biophysics and Soft Matter, University of Greifswald. Basic schematic of an AFM equipment. The optical system is used to detect the cantilever deflection when the tip contacts the surface. The optical system consists of a laser diode that is focused on the back of the cantilever. The reflected beam (which gives information about the cantilever bending) is detected by a photosensitive detector.

The information gathered from the probe's interaction with the surface can be as simple as physical topography or as diverse as measurements of the material's physical, magnetic, or chemical properties. These data are collected as the probe is scanned in a raster pattern across the sample to form a map of the measured property relative to the $X - Y$ position. Thus, the AFM microscopic image shows the variation in the measured property, e.g., height or magnetic domains, over the area imaged.

The AFM probe has a tip at the end of a small cantilever beam. The probe is attached to a piezoelectric scanner tube, which scans the probe across a selected area of the sample surface. Its work principle is based on the measurement of the interaction forces that appear between the tip and the sample when the distance between both is in the nanometric range. Since the tip is located at the end of a cantilever, any force applied to the tip causes a deflection of the cantilever, Δx, which is proportional to the force according to the Hooke's law, $F = -k\Delta x$ (where k is the spring constant of the cantilever). This deflection is detected by an optical system, which reflects a laser beam off the back of the cantilever. The reflected laser beam strikes a position-sensitive photodetector consisting of four side-by-side photodiodes that allows measuring the vertical and lateral deflections. The signal received by the four photodiodes indicates the position of the laser spot on the detector and consequently the deflection of the cantilever. This deflection can be registered during the scan of the sample, performed by a tube scanner (made from piezoelectric materials) as a $3D$ image that represents the surface of the sample (figure 3-6).

The $CAFM$ is an AFM based technique that allows to perform simultaneously topography and electrical conductivity measurements, enabling to correlate spatial features on the sample with its conductivity. To carry out this kind of measurements, a conductive tip is absolutely necessary as well as a very low noise preamplifier, which works as an $I - V$ converter that collects the current flowing through the tip. The $CAFM$ is basically an AFM with the additional elements: a conductive tip, a preamplifier and a voltage source to bias the sample.

The $CAFM$ is normally used to obtain electrical information through the measurement of current maps in a given area (simultaneously with the topographical images) or $I - V$ curves at fixed locations of the sample. Current maps allow to analyze the conductivity changes and homogeneity on a selected area. This test is performed by applying a

constant voltage to the sample meanwhile the tip scans the analyzed area. Therefore, in $CAFM$ experiments, contact mode is required to achieve a good contact between tip and sample to perform conductivity measurements.

During this thesis AFM has been used for revealing the surface topography of the $AlGaN/GaN\ HEMTs$. The $CAFM$ technique has been used to correlate the nanoscale conductive pattern and microelectronic device characteristics as described in the next section. To analyze the samples with the AFM, usually we use two tips natures. The first one is a Pt/Ir with a very sharp tip, with $\sim 25\ nm$ of the diameter and high-resolution scanning for reduced scanned areas ($1 \times 1\ \mu m^2$). The other one is a doped diamond tip (Si doped like $Carbon$) with a $\sim 100\ nm$ of the diameter. The diamond tip presents less resolution but high-resistance than Pt/Ir tip. This characteristic allows us to scan large areas ($10 \times 10\ \mu m^2$). Figure 3-7 presents the commonly view of AFM tip.

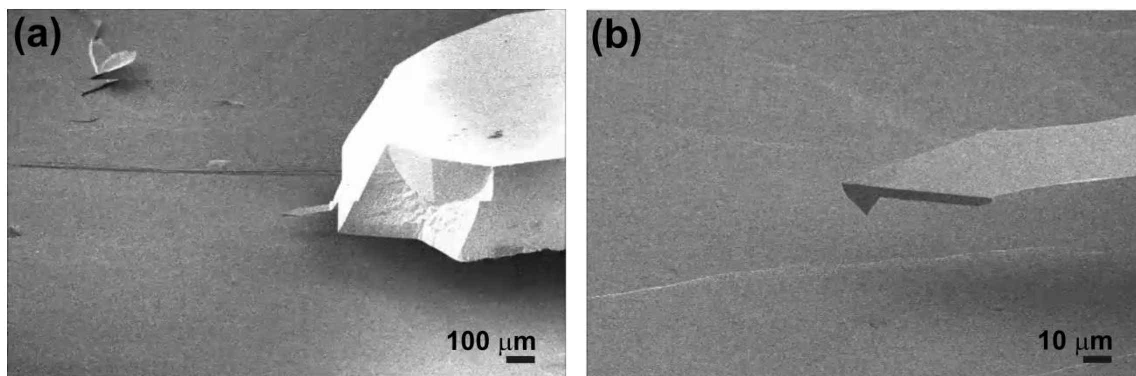

Figure 3-7. Adapted from DME Nanotechnologie GmbH information. (a) Cantilever holder with AMF tip probe and (b) detail of the tip probe.

3.3.1.2.1. OPERATION MODES

Depending on the distance between tip and sample, two different operation modes can be described: contact mode (repulsive regime) and non-contact mode (attractive regime).

Contact mode

The atoms at the end of the tip are close enough to the sample surface ($1 - 3$ Å) and interact with the superficial atoms of the sample in the repulsive regime. One of the main drawbacks of this method is the tip wearing, due to the continuous "contact" with the surface during the scan.

Non-contact mode

In this mode, the tip is operating in the attractive regime, quite close to the sample, but without being in contact. Therefore, the tip-sample contact is minimized, avoiding to damage the surface and the tip. The forces between tip and sample are quite low, of the order of pico-Newton ($1.0 \times 10^{-12}\ N$). Consequently, the vertical resolution obtained in non-contact mode is lower than that obtained in contact mode.

Tapping mode

Tapping mode is an intermediate method between contact and non-contact mode which overcomes the problems associated with friction and electrostatic forces related to contact mode and, on the other hand, offers a very high-resolution. In this case, the cantilever is oscillating close to its resonance frequency and the tip intermittently contacts or "taps" the surface. During tapping mode operation, the cantilever oscillation amplitude is maintained constant by the feedback loop and the force on the sample is automatically set and maintained at the lowest possible level. Therefore, when, for example, the tip scans a protuberance on the surface, the tip-sample distance and the amplitude of the oscillation decreases while when the tip scans a depression, the amplitude increases since the tip-sample distance increases.

3.3.2. ELECTRICAL CHARACTERIZATION

A summary of the different types of electrical measurements that have been used to analyze $AlGaN/GaN\ HEMTs$ is shown in the table 3-3. Basically, the $On-state$ is characterized by two measurements; (1) The gate transfer curve ($I_{ds}-V_{gs}$), presented in the figure 3-8 (a), is a basic measurement in the transistors devices. Besides, the transfer curve provides us of the basic subthreshold parameters too such as the drain-source leakage current ($I_{ds,off}$) and gate-source leakage current ($I_{gs,off}$) when the transistor is off. This leakage current should be very low in order to reduce the standby power consumption. Other important parameter is the V_{th} in order to know what is the voltage which the transistors turn from $Off-state$ to $On-state$ and the gate transconductance (g_m) which is the ratio of the drain current change at the output port to the gate voltage change at the input port. On the other hand, transfer curve hysteresis can be regarded as a reliability measurement, revealing if the V_{th} is shifted due to cumulative stress.

$Name$	$Setup$	$Type$	$Extracted\ Parameters$
$On-state$ $Transfer\ curve$	$3-Ter, WM$[2]	$I_{ds}, I_{gs}\ vs\ V_{gs}\ at\ T$[3]	$g_m, I_{ds,off}, I_{gs,off}, V_{th}, hysteresis$
$Current\ vs\ Voltage$	$3-Ter, WM$	$I_{ds}\ vs\ V_{ds}\ at\ T\ and\ \Delta V_{gs}$	$R_{on}, T^{\propto}, I_{ds,sat}, \mu_n, n_s$
$Off-state$ $Lateral\ leakage\ current$	$3-Ter, WM$	$I_{ds}, I_{gs}\ vs\ V_{ds}\ at\ T$	E_a
$Vertical\ leakage\ current$	$2-Ter, WM$	$I_{db}, I_{gb}\ vs\ V_{db}\ at\ T$	E_a
$Breakdown\ Voltage$	$3-Ter, WM$	$I_{ds}, I_{gs}\ vs\ V_B$	$R_{on}\ vs\ V_B$
$Others$ TLM	$4-Ter, WM$	$I-V\ vs\ T$	$R_T, R_{sh}, R_c, T^{\propto}$
$Current\ vs\ time$	$3-Ter$	$I_{ds}, I_{gs}\ vs\ t\ at\ T$	$Reliability$
$Dielectric\ stress$	$2-Ter$	$I_{gs}\ vs\ V_{gs}\ at\ T$	$Reliability$
$Charge\ trapping$	$2-Ter$	$V_g\ vs\ t$	$Reliability$
$Positive\ gate\ bias$	$2-Ter$	$I_{gd}\ vs\ V_{gd}\ at\ +V_g$	$Reliability$
$Dynamic\ I-V\ (Q\ points)$	$3-Ter$	$I_{ds}\ vs\ V_{ds}\ at\ V_{ds_Q}, V_{gs_Q}$	$Current\ collapse$
$Capacitance\ vs\ Voltage$	$2-Ter$	$I_{ds}\ vs\ V_{ds}, C\ vs\ V_{gd}$	$C/G_w, G_p/w, E_f_E_0, t_p, D_{it}, \sigma_s$

Table 3-3. Overview of the types of electrical measurements used to analyze the $AlGaN/GaN\ HEMTs$.

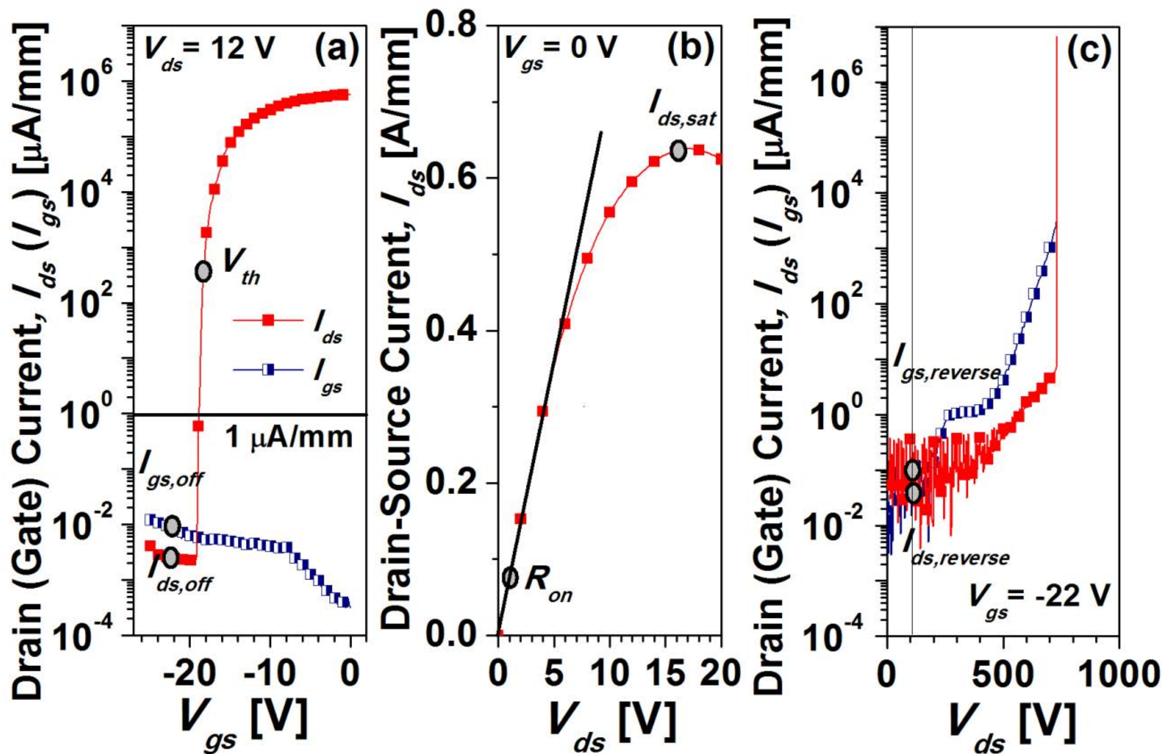

Figure 3-8. Representation of main $HEMT$ parameters. (a) $I_{ds,off}$, $I_{gs,off}$ and V_{th} from the transfer curve, (b) R_{on} and $I_{ds,sat}$ from the $I_{ds}-V_{ds}$ curve and (c) reverse leakage currents and breakdown voltage.

[2] In the table 3-3 for the setup column Ter denotes Terminal electrode and WM denotes wafer mapping.
[3] In the table 3-3 for the type and the extracted parameters columns T denotes Temperature.

(2) The current *vs* voltage ($I_{ds} - V_{ds}$) forward curve, as shown in the figure 3-8 (b). From this curve we can extract basic parameters such as the R_{on} −that in our case should be very low in order to decrease the conduction losses− and the drain-source saturation current ($I_{ds,sat}$) to know the maximum drain current given by the device.

The $Off - state$ or (lateral) $HEMT$ leakage current is given by the reverse gate-source current ($I_{gs,reverse}$) and the reverse drain-source current ($I_{ds,reverse}$) as shown in the figure 3-8 (c). The gate is biases under the V_{th} (so the channel is depleted) and then the drain is biased positively (figure 3-9 (a)). If a breakdown phenomenon is achieved then this curve is known as V_B curve which would eventually cause the reverse bias breakdown due to impact ionization. Related with the $HEMT$ reverse current, the vertical leakage current, denoted as drain-bulk current (I_{db}), as shown in the figure 3-9 (b), is the current flowing through the heterostructure when the substrate is grounded and the drain is positively biased. The back contact was made directly contacting the different wafers with the chuck of the probe station. This measurement is important to know conductive or insulating nature of the substrates.

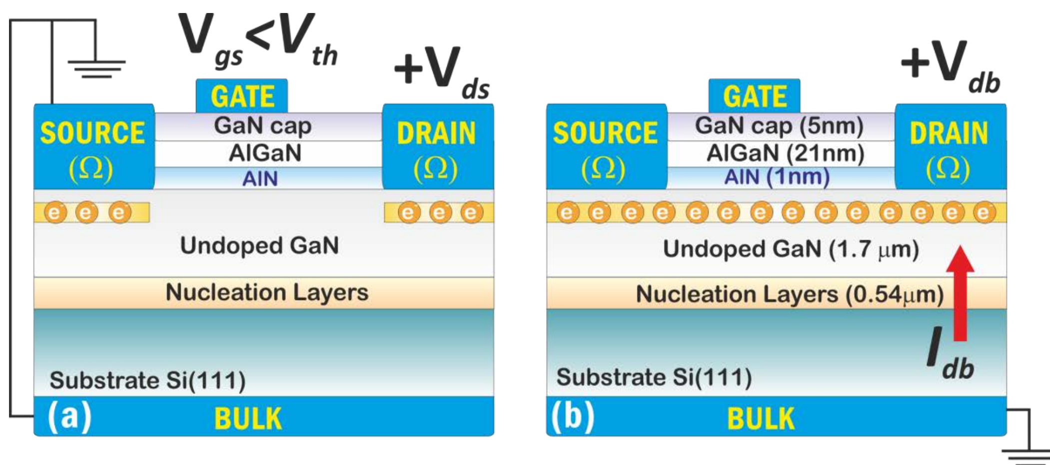

Figure 3-9. Cross-sectional view (not to scale) of the $Si - based\ HEMT$. In (a) it is also shown the configuration for a $HEMT$ reverse measurement. There the $2DEG$ is depleted ($V_{gs} < V_{th}$), the source grounded and the drain electrode positively biased. In (b) it is also shown the I_{db} which is the two terminals current between the drain and the grounded back of the wafer.

Any of the previous measurements can be analyzed at different temperatures which gives a valuable insight of the physical phenomena taking place within the structure. In general, from the subthreshold current $vs\ T$ plots we can extract the thermal activation energies (E_a) assuming a rate-limited thermally activated process following an Arrhenius law.

In addition, we have made use of other well-known device characterization techniques such as the TLM which is a well-established technique to determine the specific contact resistivity of metal Ohmic contacts to semiconductors. The $HEMT$ gate insulators films have been further characterized by a range of techniques including current vs time, dielectric stress, charge trapping, positive gate bias, dynamic $I-V$ as it will be largely described in $chapter\ V$ and $chapter\ VI$.

3.3.2.1. ELECTRIC CHARACTERIZATION SET-UP AND METHODS

Arrange of electrical characterization equipment was available to analyze the $HEMT$ devices (some of them are presented in figure 3-10). For example, the $I-V$ characterization was performed using a $Keithley$ family test system to drive the four electrodes $(source, drain, gate\ and\ bulk)$ of a $HEMT$ devices. High-voltage measurements require further attention during the breakdown voltage measurements. The devices were characterized immersed in $Galden\ oil$ bath to avoid the arcing otherwise the breakdown voltage was limited to $\sim 400\ V$ in any case. The higher voltage characterization was performed using a $Keithley\ 2410$ test system up to $1.1\ kV$. In this particular case, to measure the breakdown voltage, three terminals measurements were performed to drive the device in the $Off-state$, when the gate was biased below the threshold voltage value. In addition, we have used the probe station model $S200$ from $Wentworth\ laboratories$ where we have carried out temperature characterization up to 300 °C.

Figure 3-10. On-wafer measurement equipment (left) $Keithley$ rack and (right top) Probe station $S200$ and (right down) 300 ℃ heating chuck system.

All equipment in the laboratory can be controlled from a one computer by switching a $GPIB$ bus. End-user characterization interfaces such as $ICS\ Metrics$ and $LabView$ have been used to extract the data from electronic characterization. In addition, full wafer mapping have been done using $ICS\ Metrics$ by sequence steps programming and probe cards customized by $High\ Tech\ Trade\ GmbH$.

3.4. SUMMARY

In this chapter, the fabrication process of the $AlGaN/GaN\ HEMTs$ has been presented. The three basic steps of micro-fabrication; $HEMT$ isolation and the Ohmic and Schottky contacts, were briefly presented. These fabrication steps are in the basis of the fabricated $AlGaN/GaN\ HEMTs$ grown on Si, $sapphire$ and $FS-GaN$substrates at the $CRHEA-CNRS\ HEMTs$ which are the main devices investigated thorough this dissertation.

In the framework of the industrial contract with ON semiconductor a basic $AlGaN/GaN\ HEMT$ technology process has been successfully developed for Si substrate in the clean room of the CNM. One of the main challenges in the processing technology of $HEMTs$ based in different substrate materials is the adaptation the standard process to $GaN-based$ systems. Two $MIS-HEMTs$ and one $i-HEMT\ \ Au-free$ devices have been obtained by $CMOS$ compatible line. Starting from the basic $HEMT$ structure we have introduced different gate architecture modifications to achieve the $MIS-HEMT$ and $i-HEMT$. The $MIS-HEMT$ is a way to further reduce the gate leakage current introducing a thin dielectric (HfO_2) between the gate metal and the GaN surface. The $i-HEMT$ was achieved by thin Si_3N_4 as passivation between gate and drain/source spacing. This structure reduces the leakage current between Ohmic and Schottky contacts and improves the breakdown capabilities.

The main workhorse of this dissertation was the explorative analysis performed on the $AlGaN/GaN\ HEMTs$ by innovative electrical and physical characterization methods. A number of physical characterization techniques have been imaginatively used during my PhD including $CAFM$, SEM, FIB, TEM and EDX to determine the main physical parameters of our devices such as the morphology, the composition, the threading dislocations density, the nanoscale conductive pattern and others. Among these techniques of particular relevance was FIB and $CAFM$. The FIB physical analysis tool

has been used to investigate the morphology and the cross-section of the different $AlGaN/GaN$ layers. In addition, FIB machined process to obtain the lamella on Cu holder has been explained in detail. The AFM and $CAFM$ tools have been widely described and used to understand the conduction mechanisms through the $AlGaN/GaN$ Ohmic contact by the perform simultaneously topography and electrical conductivity measurements. A detailed $AFM/CAFM$ equipment (laser diode, cantilever, conductive tip, photodetector, preamplifier and others) and work principles (deflection of the cantilever) have been explained.

A wide range of $On-state$ and $Off-state$ electrical measurements have been also carried out. The gate transfer curve has been measured to provide us the basic subthreshold parameters such as the threshold voltage, the g_m and the hysteresis. The current vs voltage forward curve has been used to extract the R_{on} and the $I_{d,sat}$. The $HEMT$ leakage current is given by the reverse drain/gate-source current regarding the breakdown phenomenon. The $HEMT$ vertical leakage current, denoted as I_{db}, has been obtained to know conductive or insulating nature of the substrates. In addition, TLM has been used a well-established technique to determine the specific contact resistivity of metal Ohmic contacts to semiconductors. The $HEMT$ gate insulators films have been further characterized by a range of techniques including current vs time, dielectric stress, charge trapping, positive gate bias, $dynamic\ I-V$ and others. Finally, the electric characterization set-up and methods used have been explained to analyze $HEMT$ devices, such as $I-V$ curves using a $Keithley$ family instruments or high-voltage measurements, where the devices were characterized immersed in $Galden\ Oil$ bath to avoid the arcing in air. In addition, we have used the probe station model $S200$ from $Wentworth\ laboratories$ where we have carried out temperature characterization up to 300 °C. It is worth mentioning that the $high-T$ characterization is also a cornerstone of my PhD.

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Chapter 4

AlGaN/GaN HEMT Ohmic contact

4.1. INTRODUCTION

Commercial Si transistors reach their normal operational temperature limits at approximately $125°C$, typically have a switching limit in the range of a few GHz, and are highly susceptible to harsh environments. The $GaN-based$ devices have the potential to operate at temperatures higher than $500°C$, at switching frequencies much higher and due its WBG is a radiation hard semiconductor, thus improving upon many of the limitations associated with Si electronics. Besides, $high-T$ logic has been already proposed which could result in a dramatic simplification of the current power systems. The GaN smart power chip technology has been demonstrated by using $D-mode$ and $E-mode$ $HEMTs$.[1-3] However, due to its $normally-off$ operation, GaN $MOSFET$ logic is more attractive due to its natural enhancement mode operation with lower gate leakage and better $high-T$ performance.[4] Nevertheless, before obtaining fully functional systems, many technological challenges have to be overcome. Among these, the Ohmic contacts formation to implanted GaN layers, with low contact resistance, is of particular importance.

For a given metal barrier height it would be easier to contact to $n-type\ GaN$ layer rather than a Si layer. This is due to the smaller reported electron effective mass for GaN.[5] Paradoxically, the WBG which is responsible for many of the key advantages of GaN with respect to Si solid-state devices result also in larger Schottky barrier (SB) heights and deeper donor levels. GaN thermal stability and chemical inertness also give rise to difficulties in Ohmic contact formation. High-annealing temperatures, usually over 800°C, and active metal species with low work functions, such as Ti and Al, are required to achieve acceptable contact performance on GaN.[6] Additionally, it is more difficult to form Ohmic contacts to GaN because there is poorer dopant activation and ionization due to the fact that the donor levels lie deep in the bandgap. This means that there are less carriers available for current transport at room temperature (R_T) and it is more difficult to achieve a high-doping concentration in comparison to other semiconductor materials such as Si. There are very few reports available of the electrical properties of metal-semiconductor ($M-S$) Ohmic contacts to implanted GaN layers.[7-10] It should be stressed that the transport properties of Si implanted GaN are much worse than those obtained from epitaxially grown $n-GaN$ films with a comparable carrier concentration. This is generally attributed to the high-impurity incorporation (i.e., Mg and Si) and the unrecoverable ion-implanted damage.[11] Sheet and contact resistance of the implanted region will be explored in the temperature range 25– 300°C to gain further understanding of the mechanisms that take place in the $M-S$ transport.

4.2. OHMIC CONTACT FORMATION TO BULK GaN

4.2.1. TLM $I-V$ vs T CHARACTERISTICS

The TLM is a well-established technique first proposed by Shockley[12] to determine the specific contact resistivity of metal Ohmic contacts to semiconductors. The basic idea of the TLM is to plot the resistance of metallic contacts strips with a constant width separated by varying lengths of semiconductor material (figure 4-1 (a)). Within two metal strips of width Z with spacing d, when current flows (choosing the path of least resistance) it encounters the R_c and the semiconductor R_{sh}. In a bilayer model for homogeneous Ohmic contact to a semiconductor, the R_{sh} of this semiconductor below and between the TLM strips is considered to be the same.

The potential distribution under the contact is determined by both R_c and R_{sh}. The specific contact resistivity (ρ_c) is defined as:

$$\rho_c = R_c A \quad (4\text{-}1)$$

Where ρ_c is a normalized value of the R_c, which makes it independent of the contact area (A). The slope of the resulting line is a function of the bulk film resistivity while the intercept is the R_c. The total (front) resistance (R_T) could be expressed:[13]

$$R_T = \frac{R_{sh} d}{Z} + 2R_c \approx \frac{R_{sh}}{Z}(d + 2L_T) \quad (4\text{-}2)$$

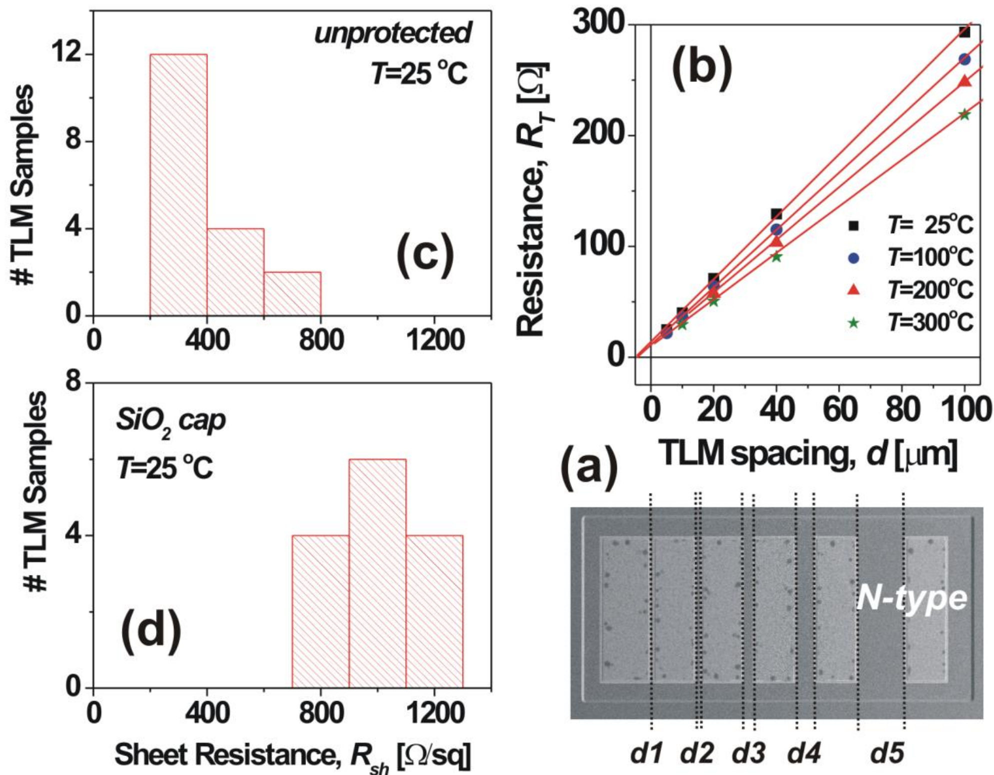


Figure 4-1. (a) Fabricated TLM. (b) Typical $I - V$ vs T measurement (c and d) R_{sh} histograms revealing inhomogeneities (measured at RT).

The slope leads to the R_{sh} and the intercept is $2R_c$ giving the contact resistance. A transfer length (L_T):

$$L_T = \sqrt{\rho_c / R_{sh}} \quad (4\text{-}3)$$

Where L_T was defined and can be thought of as that distance over which most of the current transfers from the semiconductor into the metal. This transfer length is typically

under 1 μm for good Ohmic contacts. This leads to the specific contact resistivity determination with R_{sh} known from the slope of the plot. The total resistance is measured for various contact spacings and plotted vs d as illustrated in figure 4-1 (b). The slope leads to the sheet resistance. The intercept is $2R_c$ giving the contact resistance. In the simplest bilayer model for homogeneous Ohmic contact to a semiconductor the sheet resistance of the semiconductor below and between the TLM strips is considered to be the same. This leads to the ρ_c determination with R_{sh} known from the slope of the plot. However, on a micro-nanoscale, the concept of an uniform sheet resistance for the alloyed layer should be not appropriate.

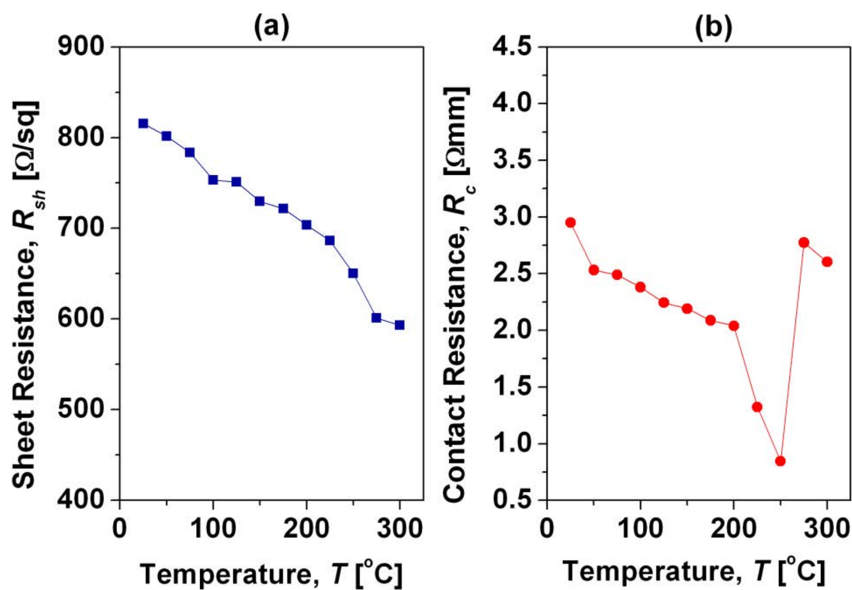


Figure 4-2. Experimental data extracted from TLM $I-V$ vs T (a) implanted layer sheet resistance and (b) contact resistance *vs* temperature.

This non-uniformity has been corroborated by measuring several TLM structures at different positions on the wafer (figure 4-1 (c) and (d)). Experimental details of the fabricated contact are given elsewhere.[14] The best results in ρ_c were obtained for the uncapped layer, but with very low reproducibility.[14] In contrast, the SiO_2 cap layer has demonstrated greater uniformity, producing a relatively low ρ_c around $\sim 10^{-5} \Omega cm^2$. Figure 4-2 presents the sheet and the contact resistance extracted for a typical SiO_2 capped TLM structure measured in the temperature range of $25-300$ °C. It is clearly observed that both, R_{sh} and R_c decrease with T. A more physical insight into the reason for this temperature dependence is given in the next sections. The contact resistance strongly increases for temperatures higher than 250 °C. A physical degradation of the

Ti/Al metal stack was observed, with the metal starting to soften below the tips. Tungsten, Tantalum or Molybdenum could be used as a final metal to make the contacts more insensitive to the $high - T$.

4.2.2. SHEET RESISTANCE

The sheet resistance is a measure of the resistivity averaged over the sample thickness. The sheet resistance of a non-uniform layer of thickness $(t - z)$ is given by: [13]

$$R_{sh} = \frac{1}{q\int_z^t [n(z)\mu_n(z) + p(z)\mu_p(z)]dz} \underset{N_D \gg N_A}{\simeq} \frac{1}{q\int_z^t [n(z)\mu_n(z)]dz} \quad (4\text{-}4)$$

Where z is the depth from the surface into the semiconductor, n and p are the free electron and hole densities respectively, μ_n and μ_p are the electron and hole mobilities. For $n - type$ material $(N_D \gg N_A)$, this equation can be simplified to the right expression. It is routinely assumed, in Ohmic contact analysis that there is complete ionization of the donor (or acceptor) impurities, i.e., $n = N_D$. This approach, while appropriate for Si, may be inadequate for semiconductors such as GaN, where the impurity levels are deeper and hence are not fully ionized at RT. For a partially-compensated $n - type$ semiconductor, the free carrier concentration $(n(z) \simeq N_D^+(z) - N_A^-(z))$ in the bulk taking into account incomplete ionization of dopant impurities is given by:[15]

$$n(z,T) = \frac{2(N_D(z) - N_A)}{1 + \alpha_D N_A + \sqrt{(1 + \alpha_D N_A)^2 + 4\alpha_D (N_D(z) - N_A)}} \quad (4\text{-}5)$$

$$where \ \alpha_D = (2/N_c)exp[E_d/k_B T] \quad (4\text{-}6)$$

The conduction-band density of states (N_c) expressed by:

$$N_c = 2(2\pi m^* k_B T/h^2)^{3/2} \quad (4\text{-}7)$$

Where h is Planck's constant, $m^*$is the effective mass for electrons, q is the electron charge, k_B denotes the Boltzman constant and E_d (in fact, $E_d = E_c - E_d$) is donor level energy with respect to the conduction band energy E_c. A single donor level is assumed within the bandgap, whose occupation is described by the position of the Fermi level (E_F). Here, the hole density has been ignored and the acceptors are assumed to be fully ionized since the Fermi energy is expected to be above the energy of even the deepest

acceptors. For a higher degree of accuracy in the degenerate range, the formalism given by Arnold[15] could be used:

$$n(deg) = 2\pi^{-1/2} n e^{-\eta_F} F_{1/2}(\eta_F) \quad (4\text{-}8)$$

Where $F_{1/2}(\eta_F)$ is the Fermi integral, the normalized Fermi energy is computed with:

$$\eta_F = \ln(n/n_i) + (E_i - E_c/k_B T) \quad (4\text{-}9)$$

Where n_i the intrinsic carrier concentration and E_i the intrinsic energy level. In our case, for defining the N^+ region for Ohmic contact, a Si implantation at 160 keV with a dose of 3.0×10^{15} cm^{-2} was performed.

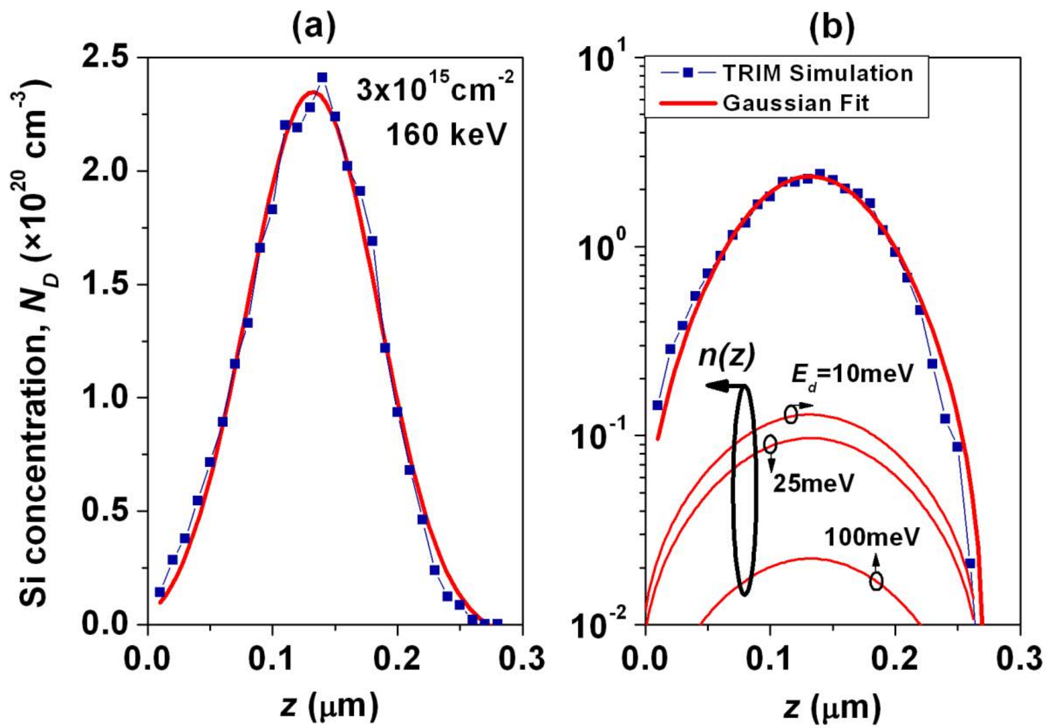


Figure 4-3. (a) Implantation profile (square symbols) of Si into the GaN epilayer simulated by $TRIM$ [160 keV and fluence of 3.0×10^{15} cm^{-2}] and the fitting (solid line) using a Gaussian function. (b) Free carrier concentration in the bulk taking into account incomplete ionization of dopant impurities for different values of donor ionization energy, $E_d = 10\ meV, 25\ meV\ and\ 100\ meV$.

The transport of ions in matter $(TRIM)$[16] Monte-Carlo simulation predicted a 0.25 μm deep implanted region, with a doping peak concentration, at the mean projected range of 2.0×10^{20} cm^{-3}. The donor impurity concentration $N_D(z)$ distribution can be fitted by means of a Gaussian distribution as shown in figure 4-3 (a).

$$N_D(z) = N_{D,0} + \frac{N_{D,1}}{\sigma_D\sqrt{2\pi}} e^{-2(\frac{z-z_{peak}}{\sigma_D})^2} \tag{4-10}$$

Where $N_{D,0} = -6.7 \times 10^{18}\, cm^{-3}$, $N_{D,1} = 3.18 \times 10^{19}\, \mathrm{cm}^{-3}$, $\sigma_D = 0.105$ and $z_{peak} = 0.132\, \mu m$. The acceptor doping is the doping of the $p - epi$ layer GaN, $N_A = 1.9 \times 10^{17}\, cm^{-3}$. Figure 4-3 (b) shows the calculated free carrier concentration *vs* depth for different values of the donor energy level. From figure 4-3 (b) it can be seen that the donor energy level has a great impact on the number of ionized impurities effectively contributing to the doping concentration. The higher the implantation dose and energy, the larger the effect of that non-negligible donor level energy gap. If the donor lever is deeper the electrical activation is poorer, dropping dramatically for $E_d > 100\, meV$. The number of electrically active centres is also a function of temperature. In the simplest approximation for a relatively highly doped $n - type$ layer ($N_D - N_A \simeq N_D\ and\ (1 + \alpha N_A) \ll 4\alpha N_D$), it can be demonstrated that the free carrier concentration due to active ionized impurities, n, follows an Arrhenius law for a single rate-limited thermally activated process:

$$n(T) \simeq \sqrt{\frac{N_D}{\alpha_D}} = \sqrt{(N_c/2) N_D e^{-\frac{E_d}{2k_B T}}} \tag{4-11}$$

Where it is considered that the temperature dependence of N_c is small compared with the exponential term. The bulk electron mobility (μ_B) for any semiconductor is a function of the temperature and doping concentration. The bulk mobility can be described by the well-known empirical derived formulation of $Caughey–Thomas$:[15-17]

$$\mu_B(C_i, T) = \mu_{min}(T) + \frac{\mu_{max}(T) - \mu_{min}(T)}{1 + (C_i/C_r(T))^{b_1}} \tag{4-12}$$

Where C_i is the concentration of ionized impurities and μ_{max}, μ_{min}, C_r, are fitting parameters which depend on the lattice temperature:

$$\mu_{max}(T) = \mu_{max,0} \left(\frac{T}{300}\right)^{b_2} \tag{4-13}$$

$$\mu_{min}(T) = \mu_{min,0} \left(\frac{T}{300}\right)^{b_2} \tag{4-14}$$

$$C_r(T) = C_{r,0} \left(\frac{T}{300}\right)^{b_3} \tag{4-15}$$

Parameters	Units	Values
$\underline{Low\ field\ channel\ mobility}$		$\underline{on\ GaN}$
$\mu_{max,0}$	cm^2/Vs	150
$\mu_{min,0}$	cm^2/Vs	100
$C_{r,0}$	cm^{-3}	3.0×10^{17}
b_1		0.7
b_2		-0.5
b_3		4.4
$\underline{Material\ parameters}$		
$\varepsilon/\varepsilon_0$		9.5
m^*/m_0		0.23
N_A	cm^{-3}	2.0×10^{17}

Table 4-1. Parameters used in the computation of R_{sh} and R_c.

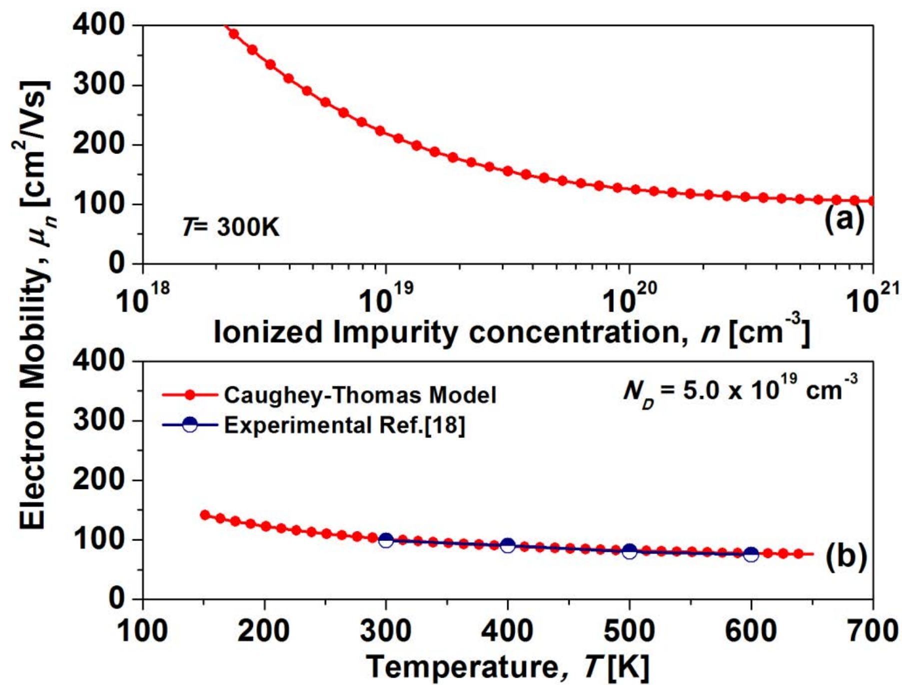


Figure 4-4. GaN **bulk electron mobility modeling (a)** vs **doping (b)** vs **temperature. Values for the electron bulk mobility** $Caughey - Thomas$ **model are fitted from the reference.[18]**

Table 4-1, summarizes the values used for the computation of the bulk mobility which is plotted in figure 4-4. These values have been adapted fitting Hall mobility reported values for Si implanted GaN doped regions.[17-19]

4.2.3. CONTACT RESISTANCE

The theory of the Ohmic contact interface is very similar to that of the Schottky interface. This is because all Ohmic contacts inevitably form initially as Schottky barriers. Methods are deployed in order to manipulate the band structure so that the tunneling transport mechanism can dominate. The three current transport processes with respect to an Ohmic contact interface are then:[20,21] (i) Thermionic emission (TE) of carriers over the potential barrier, (ii) Thermionic field emission (TFE) or tunneling of carriers through the depletion at the top of the barrier, and (iii) Field emission (FE) or tunneling of carriers through the potential barrier. This is the desirable current transport process with respect to Ohmic contact formation. The contact resistance ($R_c = [\partial V/\partial I]_{V\to 0}$) under the TE, TFE and FE models could be determined by means of analytical expressions:

$$\text{TE} \quad R_c = R_0 e^{\frac{\Phi_B}{k_B T}} \tag{4-16}$$

$$\text{TFE} \ R_c = k_B T R_0 \frac{\sqrt{E'_{00}}}{E_{00}\sqrt{\pi(\Phi_B + E_{f0})}} \cosh\left(\frac{E_{00}}{k_B T}\right) e^{\left[\frac{\Phi_B + E_{f0}}{E'_{00}} - \frac{E_{f0}}{k_B T}\right]} \tag{4-17}$$

$$\text{FE} \quad R_c = k_B T R_0 \left[\frac{\pi k_B T}{sin(\pi c_1 k_B T)} e^{\left(\frac{-\Phi_B}{E_{00}}\right)} - \frac{1}{c_1} e^{\left(\frac{-\Phi_B}{E_{00}} - c_1 E_{f0}\right)}\right]^{-1} \tag{4-18}$$

$$Where \ R_0 = \frac{k_B}{qAA^*T} \quad and \quad A^* = 4\pi q k_B m^* h^{-3} \tag{4-19}$$

Where A is the area of the contact, A^* is the $Richardson$ constant (27.6 $A/cm^2\,K^2$ for GaN) and ε is the dielectric constant and h is $Planck's$ constant. E_{00} is known as the characteristic energy:

$$E_{00} = \frac{qh}{4\pi} \sqrt{\left(\frac{n}{m^*\varepsilon}\right)} \tag{4-20}$$

The characteristic energy is an important parameter as it can inform one of which current transport regime the carriers are subjected to. E_{00} is a function of the donor doping ($n - type$ semiconductor). A plot of E_{00} vs doping concentration can yield the mode of current transport (TE, TFE or FE) when E_{00} is compared to the thermal energy $k_B T$.[20] Depending on the characteristic energy we define the variables E'_{00} and c_1 as:

$$E'_{00} = E_{00} \coth\left(\frac{E_{00}}{k_B T}\right) \quad and \quad c_1 = \frac{1}{2E_{00}} \ln\left(\frac{4\Phi_B}{E_{f0}}\right) \tag{4-21}$$

Where E_{f0} is the energy difference between the conduction band-edge (bulk) and the Fermi level. A useful approximate expression applicable to degenerate semiconductors was obtained by Nilsson[22] and is given for electrons by:

$$\frac{E_{f0}}{k_B T} = \frac{ln\, r}{1-r} + \left(\frac{3r\sqrt{\pi}}{4}\right)^{2/3} + \frac{8r\sqrt{\pi}}{3\left(4 + r\sqrt{\pi}\right)^2} \quad where \quad r = n/N_c \tag{4-22}$$

Where $n \simeq N_D^+ - N_A^-$ is the free carrier concentration in the bulk and Φ_B is the Schottky barrier height. n and Φ_B are both the magnitudes describing the transport phenomena across the contact. A closer examination of the theoretical expressions for the different current mechanism gives the functional dependence on n and Φ_B.

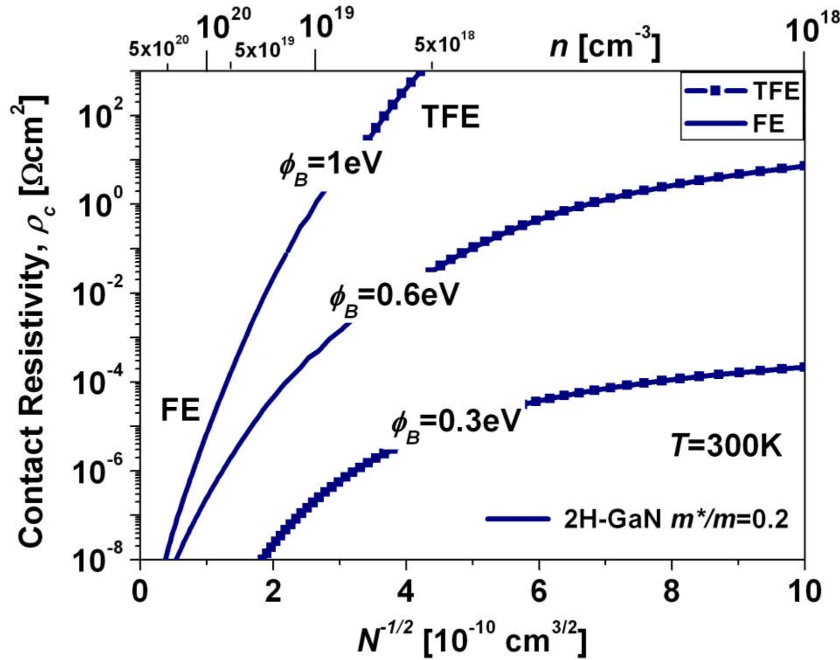


Figure 4-5. Computed contact resistivity vs donor doping at *RT* for different homogeneous Schottky barrier heights(Φ_B). *TFE* refers to the thermionic field emission mechanism and *FE* refers to field emission (tunneling) mechanism. Depending on the doping, *TFE* or *FE* dominates for a given Φ_B.

The functional dependence is $\exp(\Phi_B/k_B T), \exp\left(\Phi_B/\sqrt{n}\coth(E_{00}/k_B T)\right)$ and $\exp\left(\Phi_B/\sqrt{n}\right)$ for TE, TFE and FE ($E_{f0}c_1 > 1$), respectively. Figure 4-5 shows the $\ln(R_c)$ vs $1/\sqrt{n}$ curve for TFE and FE. The TE mechanism (which would result in a rectifying contact) is assumed to be independent of the doping and the value of the

contact resistivity predicted is well above 1 Ωcm^2, for a typical barrier height of $\Phi_B = 0.6 - 1\ eV$. A $\Phi_B = 0.3\ eV$ is also included, showing the effect of a reduced barrier height which would arise from an inhomogeneous distribution of barriers in the $M{-}S$ contact after annealing.

4.2.4. TEMPERATURE DEPENDENCE

As described in the previous section, the implanted GaN layer sheet resistance could be determined as:

$$R_{sh}^{-1}(T) = q \int_z^t [n(z,T) \times \mu_n(n(z),T)]\, dz \tag{4-23}$$

Numerical computation of the integral (integrand coming from $eqs.$ (4-5), (4-10) and (4-12)) for each temperature[23] leads to the determination of the theoretical R_{sh} vs T of the implanted GaN layer between TLM strips shown in figure 4-6 (a). The experimental value R_{sh} is significantly higher than the theoretical value (figure 4-6 (a)) if the donor level energy is equal to the value commonly reported in the literature ($E_d = 10 - 25\ meV$).[18,23,24] A poorer activation with deeper energy levels results in higher R_{sh} but does not explain well the temperature dependence depicted in figure 4-6 (a). An effective value of the peak doping of roughly 15% of $2.0 \times 10^{20}\ cm^{-3}$ ($4.0 \times 10^{19}\ cm^{-3}$) with and activation energy of 10 meV fits more accurately the experimental value for the capped R_{sh}. Again, this activation value is consistent with previous works.[18,25] In particular, Iucolano *et al.*[25] reported for $80/180\ keV$ (fluence of $2.7 \times 10^{14}\ cm^{-2}$) Si electrically active fractions of 18% annealing at 1100 °C. Analogously, the ionization energy was determined to be 20 meV extracted from scanning capacitance microscopy. The uncapped R_{sh} of approximately 400 Ω/sq is closer to the value predicted by integrating $eq.$(4-4) with the doping profile given by $TRIM$ simulations. The decrease of the R_{sh} with T is explained by the fact that more free electrons are available at the higher temperatures, diminishing the effect of carrier freeze-out of at RT.

4.2.5. $Implanted\ N^+ GaN$ CONTACTS

The $N - vacancies$ formation and/or the lowering of the Φ_B, via intermediate metallic compounds $Ti/Al - based$ multilayer structures, are regarded as the standard Ohmic contacts formation mechanisms to $n - type\ GaN$. Ti reacts with GaN and forms TiN at

elevated temperatures due to an exchange reaction mechanism. This reaction should extract N from GaN and generates $N-vacancies$ in the GaN layer. $N-vacancies$ act in turn as an $n-type$ dopant and create a highly doped region in the proximity of the interface, which lays the foundation for tunneling contact mechanism.[6] Figure 4-6 (b) shows the effect of the lowering of the Schottky barrier effect. $M-S$ transport mechanisms, specifically TE and TFE are strongly affected by the lattice temperature. This is because thermionic emission over the potential barrier into the metal has an exponential dependence on the thermal energy, which varies as a function of $1/k_BT$.[20] On the contrary, if complete ionization of carriers is considered, the tunneling based mechanism FE is virtually independent of temperature. If partial activation of impurities is considered then FE also depends on the temperature as shown in figure 4-6 (b).

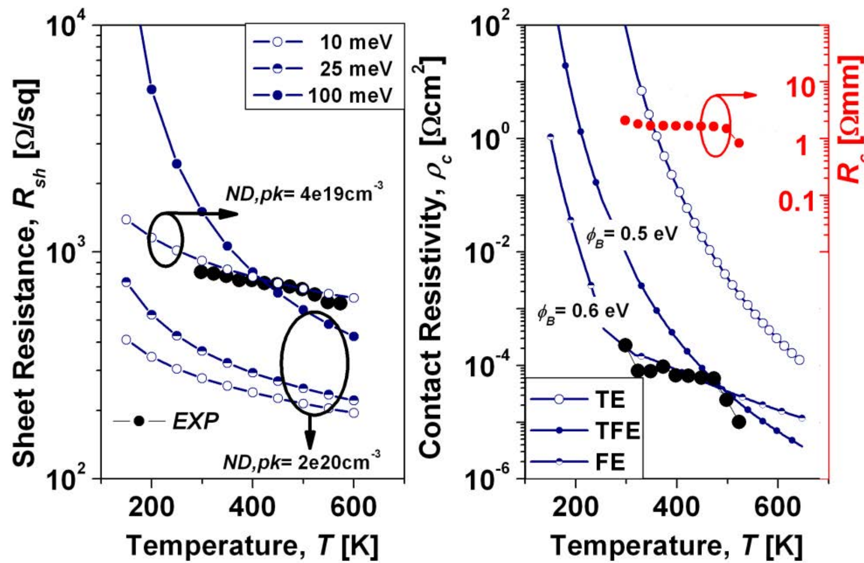


Figure 4-6. Experimental and simulation characteristics vs the temperature of the Si implanted N^+ GaN region (a) sheet resistance and, (b) $M-S$ contact resistance to the i implanted N^+ GaN well. For R_{sh}, $E_d = 10, 25$ and 100 meV are the simulated donor levels with a peak value concentration of (full activated) $N_{D,pk} = 2.0 \times 10^{20}$ cm^{-3} or with an activation of 15% ($N_{D,pk} = 4.0 \times 10^{19}$ cm^{-3}). Φ_B is the barrier height. For ρ_c, $N_{D,pk} = 4.0 \times 19$ cm^{-3} and $E_d = 10$ meV.

Tunnelling is improved with T as more dopants become active thus further reducing the barrier thickness. We suggest that the experimental T dependence of the contact resistance could be explained by a combination of FE and TFE depending on the T range. Both FE and TFE may coexist with the mechanism displaying the lowest resistance becoming dominant at a given temperature. *Eqs*.(4-16)-(4-18) have been

solved taking into account the doping peak and the donor level extracted from the sheet resistance analysis and the partial activation of doping.

As stated before, it is difficult to form Ohmic contacts to GaN because there is poor dopant activation due to the fact that the donor levels lie deep in the bandgap. This means that there are less carriers available for current transport at RT and it is more difficult to achieve a high-doping concentration in comparison to other semiconductor materials such as Si. For GaN with significant partial dopant activation, tunneling is improved with temperature as many dopants become active thus further reducing the barrier thickness. For the contact resistance simulations, $E_d = 10\ meV$ is the simulated donor level with a peak value concentration of $N_{D,pk} = 4.0 \times 10^{19}\ cm^{-3}$ and Φ_B is a varying barrier height. From the peak value concentration, the free carrier concentration at a given temperature is computed. This value of n is then used in eqs. (4-16)-(4-18). Hence, figure 4-6 (b) presents the theoretical minimum value of the contact resistance as it is computed for the doping Gaussian profile peak (not the value of the doping at the $M-S$ interface). As significant inter-diffusion of metals take place after high-temperature contact annealing[6] this hypothesis seems, in our opinion, plausible. The intermediate metallic nitrides formed after annealing are believed to reduce the barrier height and, in turn, they further reduce the contact resistance. This would be the origin of the reduced $\Phi_B = 0.5 - 0.6\ eV$ extracted from the fitting of the experimental $I\text{–}V\ vs\ T$. We suggest that the experimental temperature dependence of the contact resistance could be explained by a combination of FE and TFE depending on the temperature range. Both mechanisms may coexist, the one with the lower resistance for a given temperature dominating.

4.3. $HEMT\ vs\ Implant$

As described in the previous section, the performance and understanding of the Ohmic $M\text{–}S$ junction contact is of great importance as it influences the overall performance of a semiconductor device. There are several processes to obtain an Ohmic $M\text{–}S$ junction contact for $GaN - based$ devices (figure 4-7). The most common process to obtain an Ohmic $M\text{–}S$ junction contact is highly doping the semiconductor region, named $Implanted\ N^+GaN$ contact (N^+ for $n - type$) (figure 4-7 (a)). This contact has been investigated in the previous section (sample $C02$; sample list given in $chapter\ III$).

When the semiconductor has been highly doped, the depletion barrier becomes as thin as $\sim 3\ nm$, enabling electrons to tunnel through. $GaN - based$ devices are not an exception to this rule.[14] The scenario for contact to a polar heterojunction (HJ) $AlGaN/GaN$, (where a $2DEG$ has been formed), may be regarded as analogous to the N^+ contact.

Here, named $HJ\ AlGaN/GaN$ contact, the thinning of the barrier is achieved by recessing the $AlGaN$ barrier,[26-28] further doping[29,30] and/or selecting the metal stack[6,31,32] that will react after $high - T$ anneal, in an effort to further improve the contact resistivity. The TLM technique[33] is used again to investigate the effect of the T on the contact properties for both, $Implanted\ N^+GaN$ and $HJ\ AlGaN/GaN$ contacts, as shown in figure 4-7 (a) and figure 4-7 (b) respectively. Fabrication details have been widely described in $chapter\ III$.

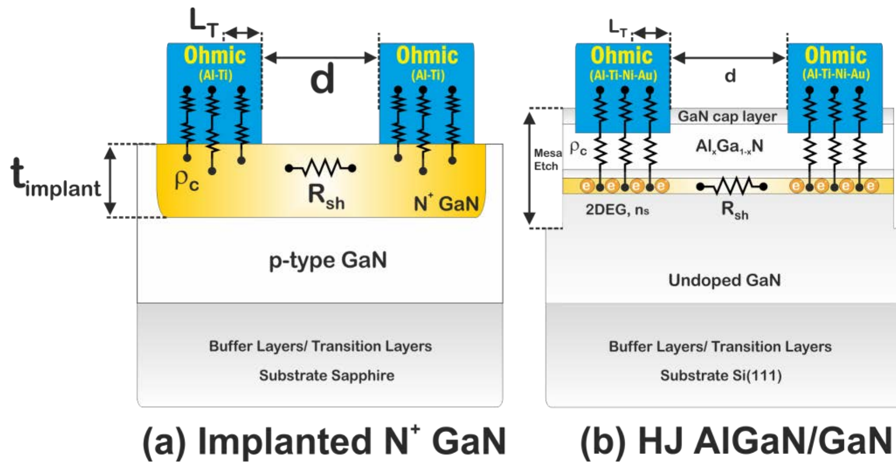


Figure 4-7. Cross section of the fabricated Al/Ti based Ohmic contacts TLM for (a) $Implanted\ N^+GaN$ and (b) $HJ\ AlGaN/GaN$.

4.3.1. EXPERIMENTAL RESULTS

The current–voltage curve ($I-V$), depicted in figure 4-8, show the characteristics between two contact pads ($d = 10\ \mu m$) for various temperatures. Also in figure 4-8, a different saturation behavior may be observed for each contact type. For the $HJ\ AlGaN/GaN$ contact the saturation-like characteristic is due to the pinch-off of the (few nanometers wide) $2DEG$ channel. In contrast, however for the $Implanted\ N^+GaN$ contact it could be consider the current flows through the $N^+\ GaN$ region ($t_{implant}$ width on figure 4-7 (a), [typically several hundreds of nanometers]). There, the saturation behavior was not observed.

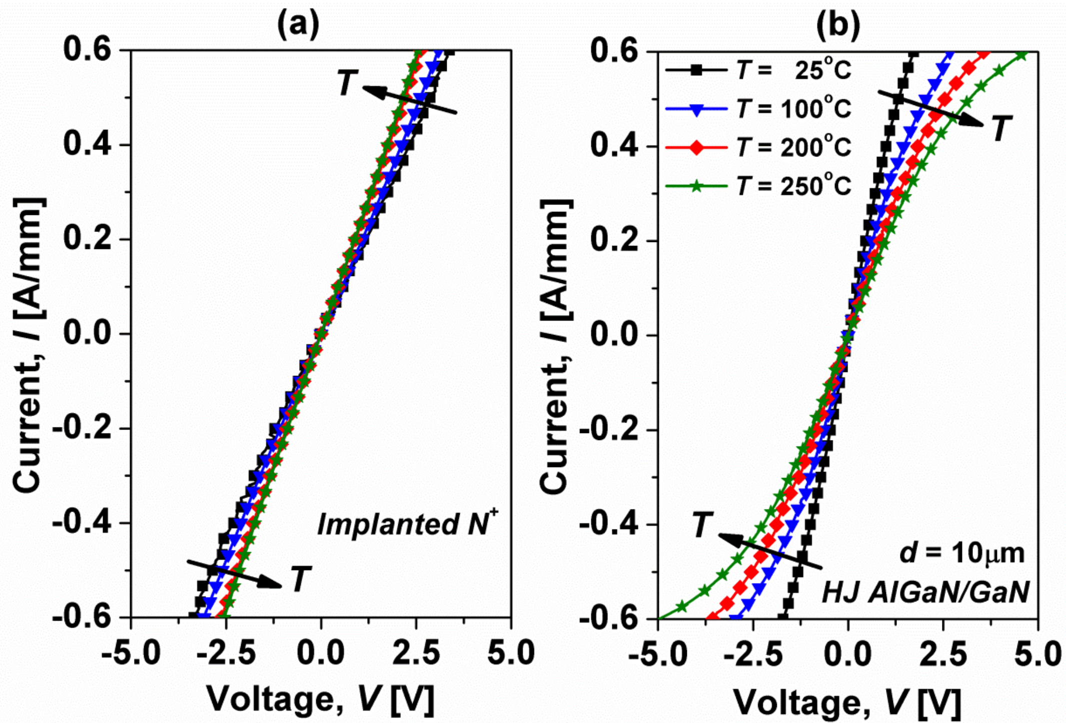


Figure 4-8. *TLM* current–voltage characteristics at different temperatures for (a) *Implanted* N^+GaN contacts and (b) *HJ AlGaN/GaN*.

Experimental TLM plots are presented for both, $Implanted\ N^+GaN$ and $HJ\ AlGaN/GaN$ contacts. At a given voltage, the current decreases or increases with T and hence, the $R_T\ vs\ T$, as shown in the figure 4-9, measured for several d and W for different temperatures. From these plots, the R_{sh} and R_c may be determined as shown in figure 4-10. For the $Implanted\ N^+GaN$ contacts, both R_{sh} and R_c decrease with T as shown in figure 4-10. Our $Implanted\ N^+GaN$ type contact is significantly resistive. At RT, the contact presents high-values for both R_{sh} and R_c, $850\ \Omega/sq$ and $2.2\ \Omega mm$ respectively and ρ_c of $4.6 \times 10^{-5}\ \Omega cm^2$.

We believe that these relatively high-values of R_{sh} and R_c may be due to a poor activation of dopants under the contact, as it will be pointed out further on. Conversely, for the $HJ\ AlGaN/GaN$ contacts, R_{sh} increases with T (figure 4-10), while R_c has a weaker dependence upon T (a slight increase). At $RT\ HJ\ AlGaN/GaN$ the contact resistance is lower with values of $400\ \Omega/sq$ and $0.2\ \Omega mm$ for both R_{sh} and R_c, respectively corresponding to ρ_c of $9.0 \times 10^{-7}\ \Omega cm^2$.

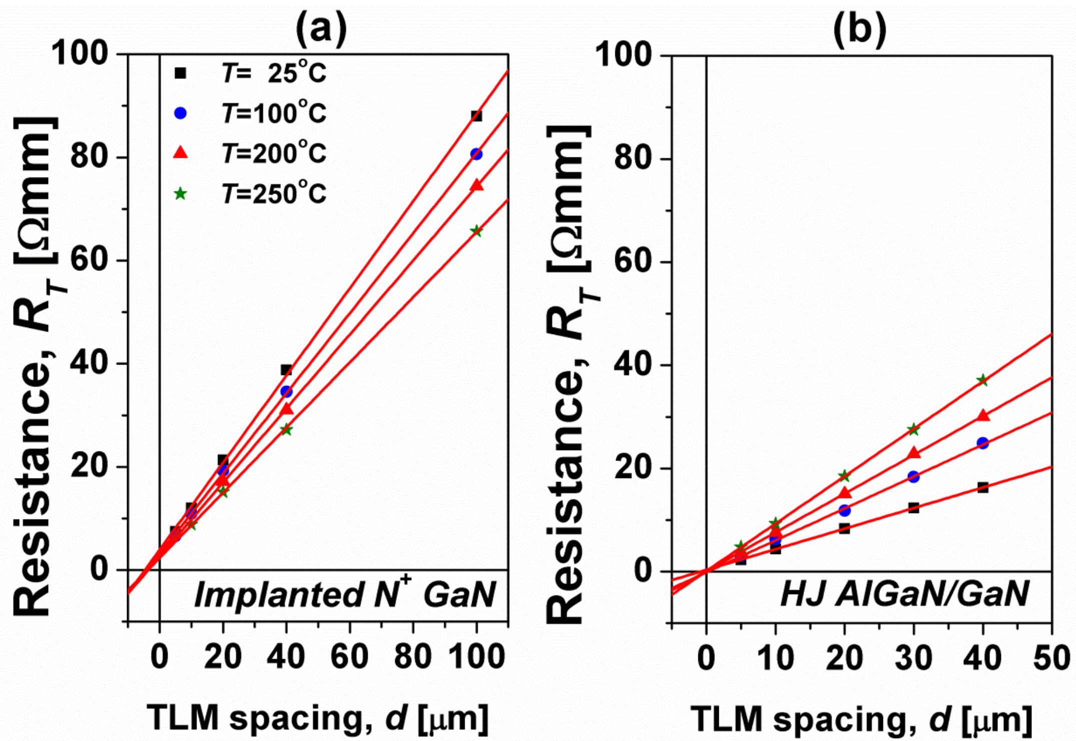


Figure 4-9. TLM total resistance plot R_T (in Ωmm) for (a) $Implanted\ N^+GaN$ contacts and for (b) $HJ\ AlGaN/GaN$ in the temperature range of $25-250$ ℃.

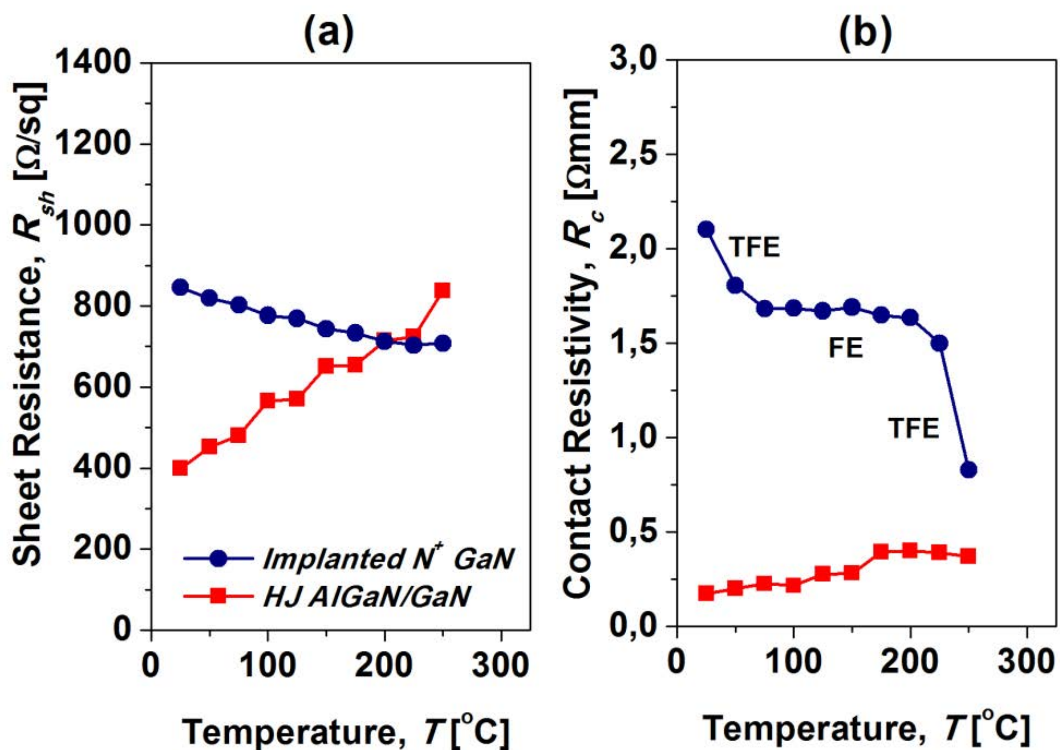


Figure 4-10. Experimental (a) R_{sh} and (b) R_c vs T for both types of $Al/Ti-based$ Ohmic contacts $Implanted\ N^+GaN$ $(MOSFET)$ and $HJ\ AlGaN/GaN$ $(HEMT)$.

4.3.2. *Heterojunction* $AlGaN/GaN$ CONTACTS

For a $HJ\ AlGaN/GaN$ based contacts, it may be considered that the R_{sh} between the TLM strips would be the resistance of the electrons in the $AlGaN/GaN$ $2DEG$ channel.[34]

Therefore,

$$R_{sh}(T) \simeq \frac{1}{q\mu_{2DEG}(T)n_s(T)} \tag{4-24}$$

Where μ_{2DEG} is the $2DEG$ channel electron mobility and n_s is the $2DEG$ sheet carrier concentration. At RT the value of the R_{sh} is consistent with an $n_s = 1.0 \times 10^{13} cm^{-2}$ and μ_{2DEG} of 1400 cm^2/vs. It has been reported that n_s is a weak function of temperature.[35,36] Therefore, it may be considered, in first approximation, that the R_{sh} dependence with T would be established by the mobility of the electrons in the $2DEG$. In the $HJ\ AlGaN/GaN$ channel, the lattice vibrations due to polar-optical-phonons scattering on the non-intentionally doped GaN layer are the mobility limitation factor at elevated T. The polar-optical-phonon scattering is the dominant scattering mechanism for the $2DEG$ in a wide T range since the impurity scattering is minimized due to the spatial separation of electrons and ionized impurities; this being especially true for temperatures above 300 K.

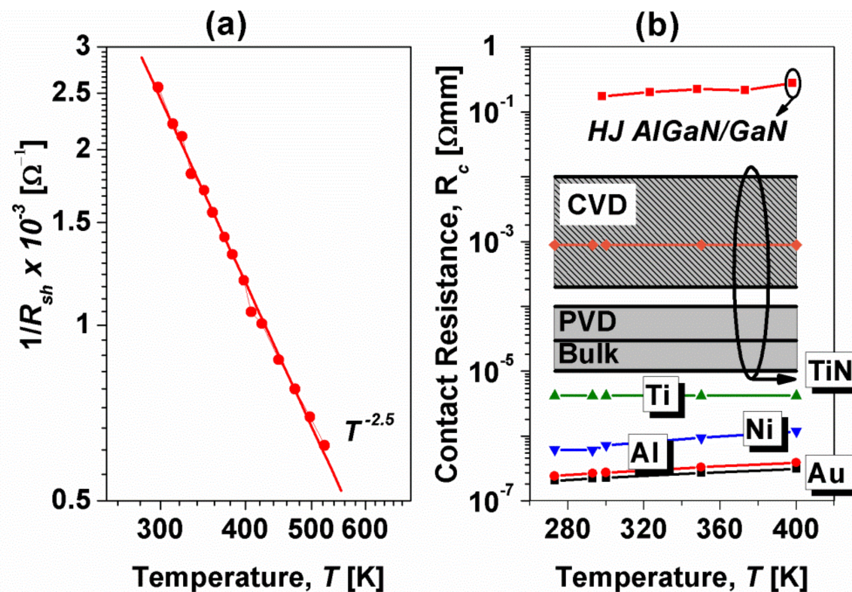


Figure 4-11. $HJ\ AlGaN/GaN$ characteristics for (a) $1/R_{sh}$ and (b) R_c. The contact resistivity is compared with reported values for Au, Al, Ni, Ti *and* TiN resistivity *vs* T.[37-39]

This polar-optical phonon mobility depends on T (mainly because phonons follow the $Bose-Einstein$ distribution function of occupancy) and $2DEG$ sheet charge density.[36,40,41] The increase of R_{sh} with T is consistent with the mobility limitation discussed above, and can be fitted by a power law relation, as shown in figure 4-11 (a). When the T increases the lattice vibrations are effectively increased. This causes a reduction of the mobility of the carriers in the $AlGaN/GaN$ channel which result in turn in an increase of the R_{sh}.

Regarding the R_c for the HJ $AlGaN/GaN$ based contacts, two mechanisms have been reported as the methods deployed to get an Ohmic contact to $AlGaN/GaN$.[31] Again, the low Schottky-barrier mechanism is also a possible pathway for low resistance Ohmic contact formation, where TiN is believed to have a lower work function than Ti, and therefore, a lower contact resistance can be achieved.[42] Recessing the $AlGaN$ layer make this barrier thinner, enhancing the carrier tunneling probability.[27] A direct electron path mechanism (or spike contact) has also been proposed as a potential contact mechanism in the HJ $AlGaN/GaN$ based contacts[6,42,43], which would be more efficient than the tunneling mechanism. TiN protrusions, formed along dislocations and penetrating through the $AlGaN$ barrier layer, have been shown to establish a direct link between the $2DEG$ and the metal so that electrons are able to freely flow in both directions, as shown in the TEM of the HJ $AlGaN/GaN$ presented in figure 4-12. This would explain the more metallic-like dependence and the reduced resistance.

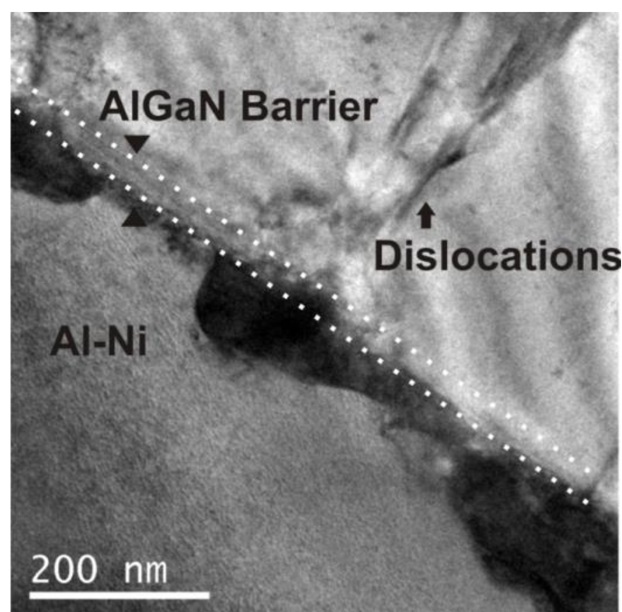


Figure 4-12. TEM image of the Ohmic contact HJ $AlGaN/GaN$.

Reported TiN resistivity is $10^{-2} - 10^{-5}\Omega mm$ range[37-39] which is much higher than pure $Ti, Ni, Al, or\ Au$ (which are the metal stack of our contact), as shown in figure 4-11 (b). The resistivity of TiN depends on if it is bulk material or the method of growth with different values depending if the growth is physical vapor deposition (PVD) or CVD based.[38] These protrusions would only contact the $2DEG$ in small areas which could well explain the lower R_c achieved for $HEMT$ type contacts and its correlation with temperature.

Comparing our results with previous works investigating the $R_c\ vs\ T$ behavior, the $Implanted\ N^{+}GaN$ contacts corroborate the very well-known tunneling based contact, just like in Si technology. The implanted Ohmic contact mechanism is in this case independent of the type of substrate ($Si, SiC\ or\ sapphire$) and/or the metallic stack ($Al\text{–}Ti$ is by far the most used). The contact resistance value obviously would change depending on the fabrication process and the resulting alloys after the contact annealing, but the physics behind the contact would remain the same: FE or TFE dominating depending on the doping and the barrier height.[44]

For our $HJ\ AlGaN/GaN$ a based contact, the contact resistance temperature dependence (the slightest increase with T) is evidently in conflict with the previous well-known theory. This is not a universal result for every kind of contact to $HEMT$ devices. In fact, there are reports which claim $TFE - like$ dependence of the contact resistance with the temperature.[45,46] Some other reports however, usually showing lower contact resistance $R_c < 0.5\ \Omega mm$, are believed to be due to other completely different Ohmic contact formation mechanism:[6,45] The ''spiking'' mechanism or the metallurgical union of the $2DEG$ electrons and the contact metals. We believe that this mechanism is virtually independent of the starting substrate: $Si, SiC, or\ sapphire$, if you are able to promote the metal alloys sufficiently near towards the $2DEG$ electrons. This makes the barrier for electrons (if any) remarkable thin and, as for contacts following the theoretical pure FE mechanism, the contact resistance should be almost temperature independent.[27,23,45] In this sense, we believe that the reduced contact resistance for our $HJ\ AlGaN/GaN$ contacts $R_c = 0.2\ \Omega mm$ (compared with the $R_c = 2.2\ \Omega mm$ for the implanted) should be related to this very thin barrier between the $2DEG$ electrons and the metal stack forming the Ohmic metals. This mechanism is much more efficient since, even considering the fact that you have only a small fraction of the contact area really

contacting to the $2DEG$, the resistance of the metallic nitrides or any metallic compound at the interface is very small. The reported pure TiN resistivity from the literature (figure 4-11 (b)) is in the range of $10^{-6} - 10^{-2}\ \Omega mm$, which is much smaller than the state-of-the art contact to GaN implanted layers (which very rarely drop under 1 Ωmm, due to the poor activation of dopants). It is worth mentioning that the four probes test carried out on wafer for our HJ $AlGaN/GaN$ TLM samples is maybe quite stressful for the metal stack integrity resulting somehow in a degradation of the contact resistance with temperature ($R_c = 0.4\ \Omega mm$ at 300 °C). In this sense, previous works[47] with very similar metal stack (but for $AlGaN/GaN-on-SiC$ with much better thermal conductivity than Si) have reported excellent thermal stability of the metal stack at temperatures up to 500 °C.

4.4. SPIKING MECHANISM

The objective of this investigation is to analyze at the submicron scale, a typical $Ti/Al/Ni/Au$ Ohmic contact to an $AlGaN/GaN$ substrate with a state-of-the-art $(0.2\ \Omega mm)$ R_c.[6,45,46,48,49] A range of physical analysis tools including SEM, FIB, TEM, EDX and $CAFM$ are used to investigate the morphology and composition of the Ohmic contacts. Figure 4-13 shows the schematic cross-section of the fabricated device and the $CAFM$ configuration. $HEMT$ DC device characteristics (forward and reverse) were measured at 15 °C intervals, from $25-310$ °C, on a $Wentworth$ $s200$ probe station with a heated chuck system. The high-voltage characterization was performed using a $Keithley$ 2410 test system. The Si substrate was floating during the $HEMT$ DC tests. Two $I-V$ vs T measurements were also made across the drain–bulk and the gate–bulk to determine the vertical drain–bulk and gate–bulk currents, respectively. This was investigated further by means of a set standard test devices with $4/4/5\ \mu m$ of source–gate (L_{gs}) and gate–drain (L_{gd}) spacing and gate length (L_g).

The $I-V$ curve, depicted in figure 4-14 (a), shows the characteristics between the two contact pads $(d = 5\mu m)$ for various temperatures. At a given voltage, the current decreases with increasing temperature, and hence, the R_T increases with temperature, as shown in the figure 4-14 (b). Figure 4-14 (c) presents the contact parameters with the temperature evolution extracted from the TLM data in figure 4-14 (b). A low R_c (in the range of 0.2 Ωmm) was determined at RT. The R_{sh} increases with T.

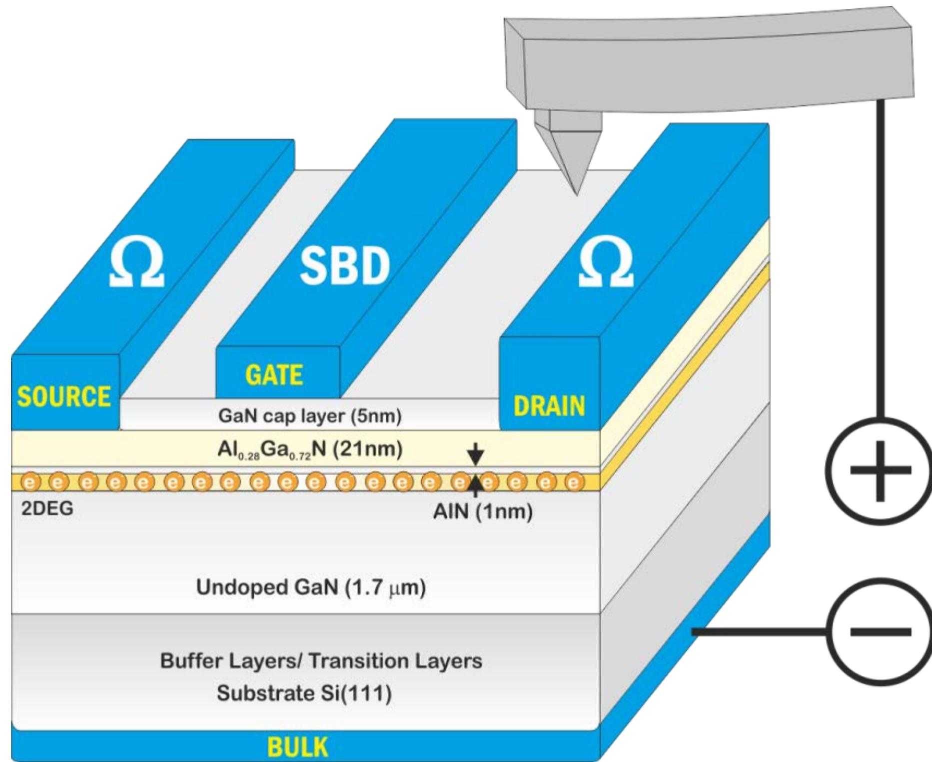


Figure 4-13. Cross-section of the $AlGaN/GaN-on-Si\ HEMT$ transistor under study. Ω symbolizes Ohmic contact and SBD indicates the gate Schottky barrier diode on the GaN cap.

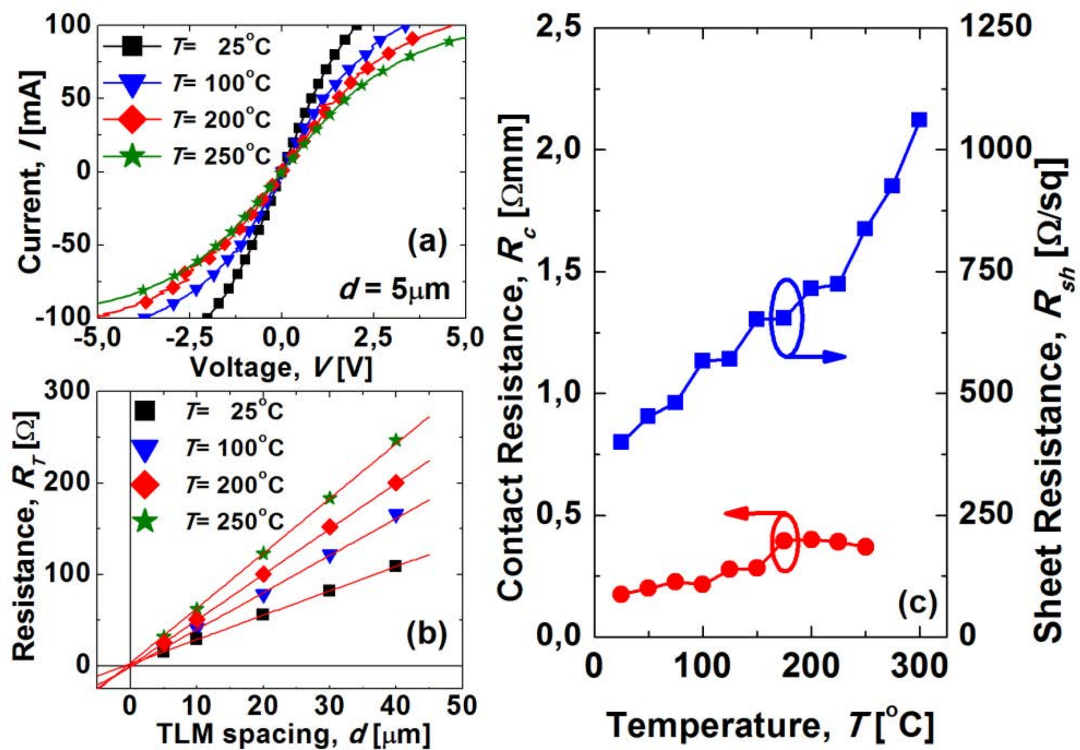


Figure 4-14. (a) Typical $I-V\ vs\ T$ measurement and (b) and (c) shows the R_T, R_{sh} and R_c evolution with temperature.

We suggest that this is likely due to the increase in phonon scattering with T.[34] It was also observed that R_c slightly increases with T, which appears to be in conflict with the traditional current transport mechanisms for metal-semiconductor contacts.[20] TFE has an exponential dependence on the thermal energy $(1/k_B T)$, and hence, a decrease in R_c with T is the commonly reported behavior for an Ohmic contact to $AlGaN/GaN$ heterostructures,[45,46] $n-type\ GaN$,[44,50,51] or $p-type\ GaN$.[52] If the complete ionization of carriers is considered, the pure tunnelling mechanism, FE, is virtually temperature independent.[23]

For the $AlGaN/GaN$ system, two mechanisms have been reported as the methods employed to form an Ohmic contact to epitaxial GaN or $AlGaN/GaN$.[6] These are the formation of $N-vacancies$ and/or the lowering of the Schottky barrier via intermediate metallic compounds.[48,51,53] As mentioned before, $Ti/Al-based$ multilayer structures are regarded as the standard Ohmic contacts for $n-type\ GaN$. Ti reacts with GaN and forms TiN at elevated temperatures due to an exchange reaction mechanism. This reaction should extract N from GaN generating $N-vacancies$ in the GaN layer. $N-vacancies$ act in turn as a $n-type$ dopant and create a highly doped region in the proximity of the interface, which lays the foundation for FE tunneling contact mechanism. The lowering of the SB may also explain the low resistance Ohmic contact, as TiN is believed to have a lower work function than Ti. Recessing the $AlGaN$ layer makes this barrier thinner, and this is regarded as a common method used to enhance the carrier tunneling probability.[27] In either case, a thinner (high-doping) or a smaller barrier (SB, lowering) to the electrons would help to reduce R_c.

A direct electron path mechanism (or *spike* contact) has also been proposed[6,43] as a potential contact mechanism in the $AlGaN/GaN$ heterojunction, which would be more efficient than the FE tunneling mechanism. TiN protrusions, formed along dislocations and penetrating through the $AlGaN$ barrier layer, have been shown to establish a direct link between the $2DEG$ and the metal, so that electrons are able to freely flow in both directions. To understand the R_c dependence with temperature, we made a closer look at the TLM cross section, as it is shown in figure 4-15. This figure shows three different SEM images of the same Ohmic contact region for an intact, FIB machined, sample (before the $TLM-T$ measure but after the 750 °C RTA annealing process).

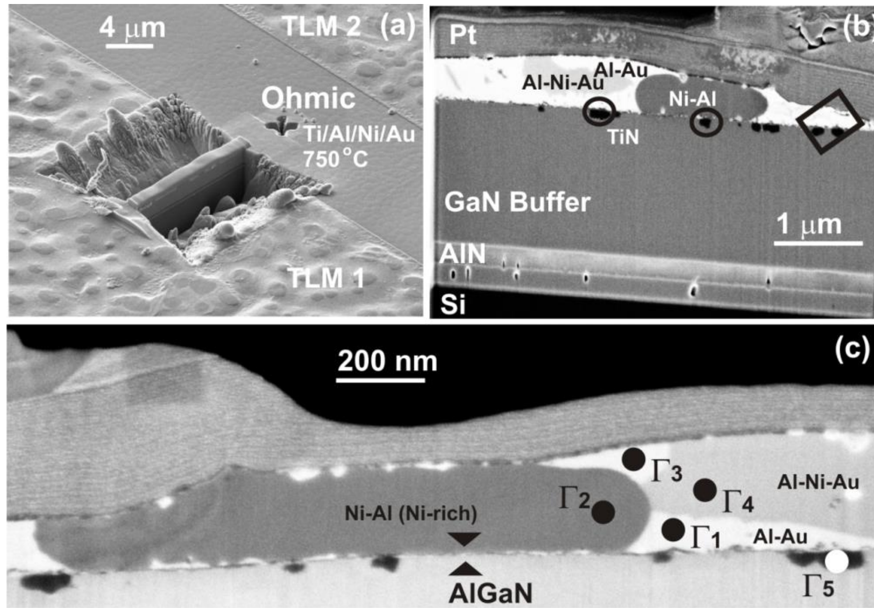
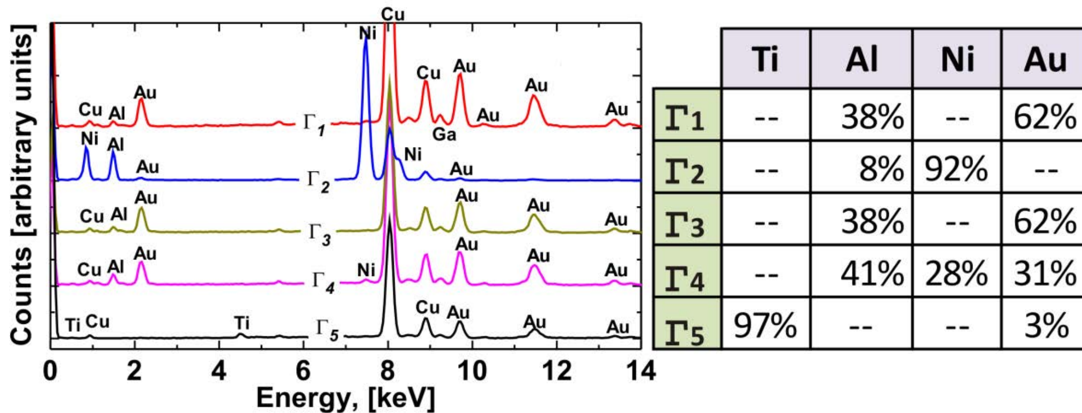


Figure 4-15. TLM SEM **cross section images of the** $Ti/Al/Ni/Au$ **Ohmic contact annealed at 750 ℃ for 30** s. **(a) View of the** FIB **machined lamella still anchored, (b) detailed view of the different layers, and (c) zoom in the Ohmic contact area.**



	Ti	Al	Ni	Au
Γ1	--	38%	--	62%
Γ2	--	8%	92%	--
Γ3	--	38%	--	62%
Γ4	--	41%	28%	31%
Γ5	97%	--	--	3%

Figure 4-16. EDX **analyses at five distinct Ohmic contact regions named** Γ_1, Γ_2, Γ_3, Γ_4, **and** Γ_5 **(depicted in figure 4-15 (c)).** EDX **relative composition for** $Ti, Al, Ni, and\ Au$ **is included in the table on the right.**

The rough morphology of the alloy surface can be observed after RTA annealing. Figure 4-15 (a) shows the TEM lamella still anchored. Figure 4-15 (b) shows a detailed SEM cross section of the lamella. The black square denotes the approximate area where the $CAFM$ study was carried out, which will be further discussed later. It has been reported that metal-nitride clusters (such as TiN) that penetrate through the $AlGaN$ barrier layer are the direct link between the $2DEG$ and the metal.[6] Usually TiN is observed at the interface of $Ti-based$ contacts,[32,54] this being the principal metallic alloy that helps in

lowering the R_c value. Figure 4-15 (c) shows, in detail, the zone where EDX analysis has been carried out in order to investigate the composition of different layers. Figure 4-16 presents the EDX scans along with a table showing the relative abundance of $Ti/Al/Ni/Au$. Each region investigated is identified by labels $\Gamma_1 - \Gamma_5$ (figure 4-15 (c)). EDX scans indicate that Γ_1 and Γ_3 have a similar composition based-on $Al - Au$. However, a small amount of Ni was found in Γ_1 when compared with Γ_3, but it was within the experimental error. The relative abundance of $Ti/Al/Ni/Au$ seems to suggest that Ni has a tendency to stick together (in the areas marked as Γ_2) resulting in the rough surface.[55,56] Corroborating this point, Au signal is clearly visible in all the metallic alloys with the exception of these $Ni - rich$ clusters. Hence, it appears that $gold$ has a strong propensity to inter-diffuse all over the metallic layers, whilst it is also located at the $metal/AlGaN$ interface (Γ_5). In addition, region Γ_5 alone contains Ti which remains in the $AlGaN$ interface forming TiN compounds. In figure 4-16, the Cu signal comes through from the sample holder.

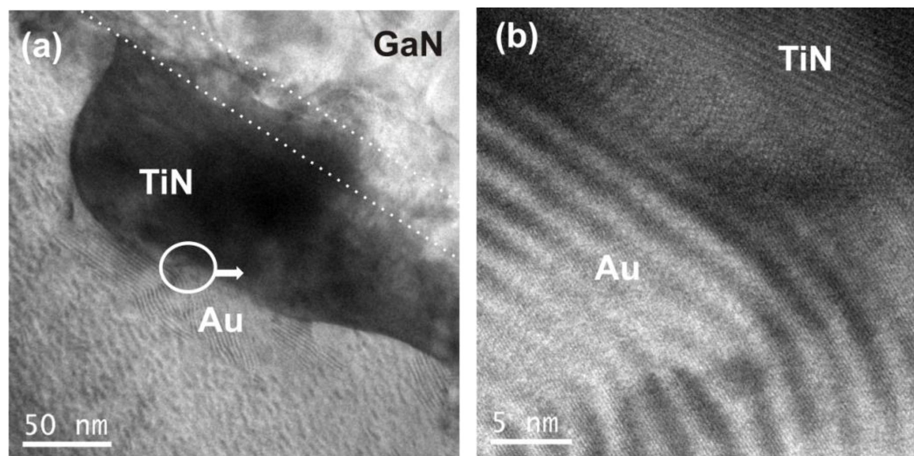


Figure 4-17. Cross sectional TEM images of the (a) $Ti/Al/Ti/Au$ contact annealed at 750 °C for 30 s. and (b) detailed image of region Γ_5.

Figure 4-17 depicts a TEM cross-section of region Γ_5. Different crystal planes may be observed with different net orientation. This thin layer of TiN has been reported[32,57] to be responsible for the Schottky to Ohmic transition that occurs at the annealing temperature of 750 °C. To verify this, we have used the technique known as $CAFM$.[43,57,58] The TLM sample was biased at $-4.2\ V$ and the surface was scanned with the tip grounded. The scan was performed in tapping mode across a scan size of $1.0 \times 0.5\ \mu m^2$, at a frequency of 0.5 Hz. The samples were in a dry nitrogen ambient, whilst the entire system works inside a Faraday chamber to minimize external interference.

Figure 4-18 (a) shows the morphological image of the sample. The surface is far from flat, with a root mean square (RMS) roughness of 25.7 nm for the scanned area. Figure 4-18 (b) presents the current map for the surface. Conductive areas, denoted as clear (white), means higher current through the tip ($\sim 10\ nA$), though this represents just 5% of the measured area $1.0\ \times 0.5\ \mu m$. Meanwhile, the significant dark areas signify current values of $1\ nA$ or less. Therefore, the surface $CAFM$ results suggest that there are preferential spots for the current flow in agreement with the spiking mechanism.[43] It is worth mentioning that the TLM surface, as shown in figure 4-18 (c), was not uniformly alloyed; a FIB etch ($30\ kV - 2\ nA$) of 0.5 μm depth further revealing the inhomogeneous nature of the contact. It appears that the $Ni - rich$ regions are more resistant to the etch.

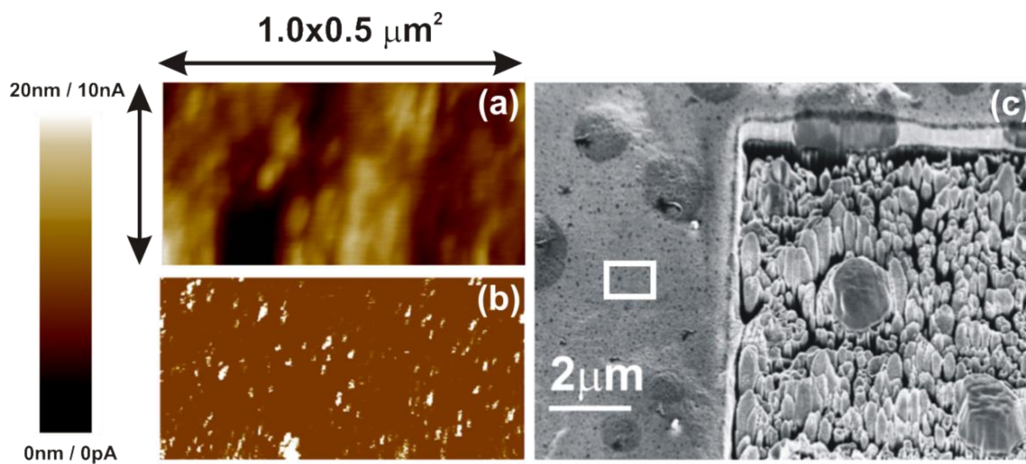


Figure 4-18. (a) Topography and (b) current map of TLM surface taken with the $CAFM$ for the $1.0\ \times 0.5\ \mu m^2$ scan. (c) SEM image of FIB partial etch on TLM surface.

Analogously, a $CAFM$ study of the lamella cross section from figure 4-15 (b) is depicted in figure 4-20. This figure shows a detailed zoom of the heterostructure of $AlGaN/GaN$. The lamella was wire bonded to the Cu lamella holder (where the lamella is attached by Pt) to achieve a good electrical contact. The recess etch of the contact was selective and the gate area was protected during the RIE process. Therefore, the rest of the GaN cap surface was negligibly damaged during the contact recess etch. Besides, the effect of the Ni clustering after the RTA annealing is well illustrated in figure 4-19. Figure 4-19 (a) shows an Ohmic contact strip after the RTA annealing. The mean size of the regular Ni cluster was 2 μm distributed in a fairly homogeneous pattern. Figure 4-19 (b) shows the same strip area after a Ga^+ on FIB etch ($30\ \text{kV}: 20\ \text{nA}$). The Ni clusters are much more resistant to the etch behaving as a self-

aligned mask. If the FIB etch conditions are changed to 30 kV: 10 nA, but increasing the etching time, a much more intricate texture of Ni nanopillars is revealed (Figure 4-19 (c)). Figure 4-20 (a) shows the morphology of the lamella cross section revealing high-RMS roughness ($369\ nm$) due to the FIB sectioning. However, the current map, figure 4-20 (b), reveals a clear transition region (dark line), which we believe corresponds to the Ohmic $metal/AlGaN$ interface. This region is significantly less conductive. The current density of the interfacial areas has been calculated to be between just 0.1 and 1 $\mu A/cm^2$. This tallies with the previous $CAFM$ results of figure 4-18, as it again accounts for just 5% of the conductive interface spots across the $0.6\ \mu m$ scanned. It is worth mentioning that there is no correlation between the roughness and the $CAFM$ measurements, with only a small part of the interface actually conductive.

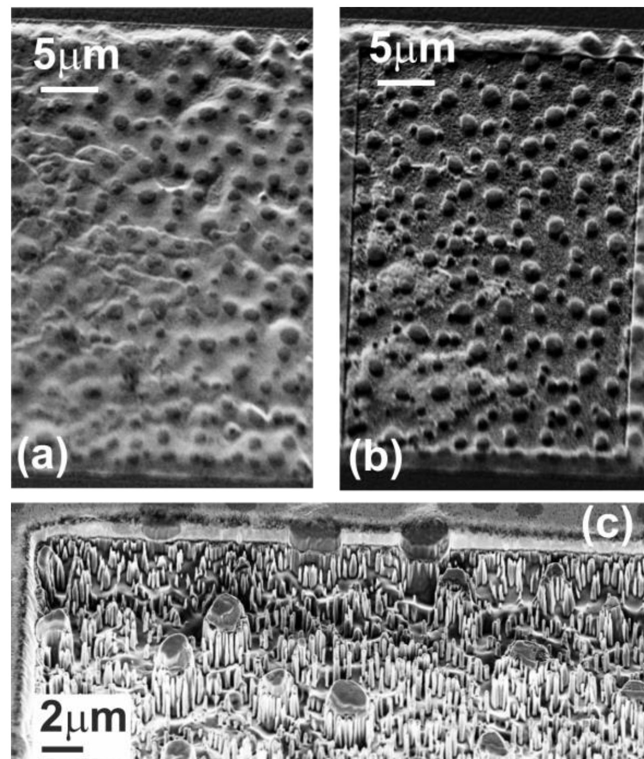
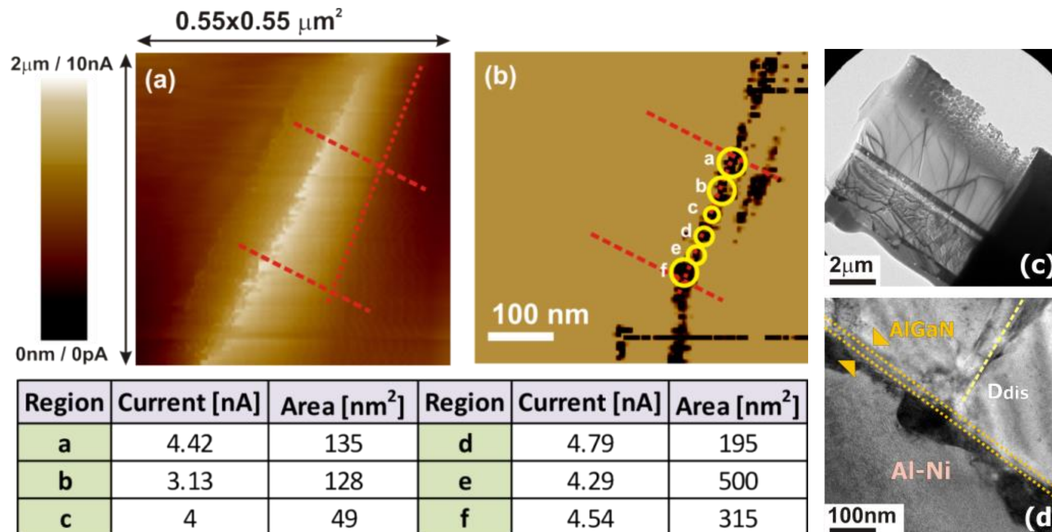


Figure 4-19. (a) Ohmic metal strip after RTA annealing. (b) The same region after a ($30\ kV$: $20\ nA$) FIB etch where the Ni clusters were isolated. (c) Changing the FIB etch conditions, smaller nanopillars can be created.

This seems to correlate with the $CAFM$ study on the surface and the $TLM\ vs\ T$ electrical results. Figure 4-20 (c) and figure 4-20 (d) present a general view of lamella mounted in the holder and the $AlGaN$ active layer respectively.



Region	Current [nA]	Area [nm^2]	Region	Current [nA]	Area [nm^2]
a	4.42	135	d	4.79	195
b	3.13	128	e	4.29	500
c	4	49	f	4.54	315

Figure 4-20. (a) Topography and (b) current map of lamella cross section taken with the $CAFM$ for the $0.55 \times 0.55\ \mu m^2$ scan. (c) A micrograph of the TEM lamella mounted in the Cu holder ready for inspection. (d) A micrograph of the $AlGaN$ active layer with the Ohmic contacts on top.

4.5. AU-FREE CONTACTS

The fabrication of Au Ohmic contacts using $Ti/Al/Ni/Au$ stack, is widely used Ohmic metal scheme for the fabrication of GaN devices.[56,59,60] A contact resistance below 0.6 Ωmm is commonly obtained in this metallization form.[60] The Au layer is believed to improve the contact resistance by forming Ga vacancies in the semiconductor and by preventing the oxidation of the metal surface. However, long-term Au diffusion has been proposed as an important degradation mechanism for Ohmic contacts.[59] Besides, the use of gold to from low resistance contacts requires a dedicated production line, since Au represents a contaminant element in the standard $CMOS$ fabs.[61] The possibility of transferring $GaN - on - Si$ technology from research to industry enables the development with a strong reduction of costs and high-performance power components for highly efficient power switching. This is the key point why the process would like to avoid $gold$ to obtain $GaN\ HEMT$ devices. The latter requires that the process is $gold - free$, and that the flow and substrates are compatible with the typical $CMOS$ tool set and contamination status.

Nowadays, the challenges of the processing $Au - free\ GaN - on - Si$ wafers, with large diameter ($6 - inch$), have been addressed, with respect to the growth of high-quality $AlGaN/GaN$ epitaxy, the processing in typical $CMOS$ fabs, the impact of Ga contamination on the tools, the evolution of the wafer bow throughout the process, and others, are commercially available.

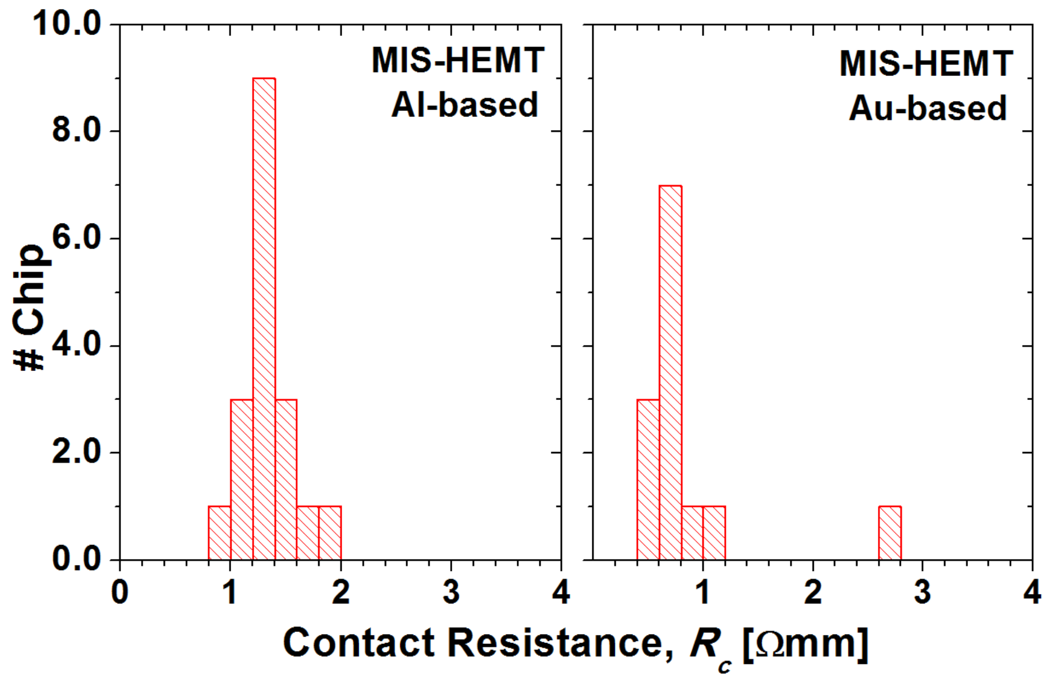


Figure 4-21. Contact resistance distribution for $Al - based$ contact *vs* $Au - based$ contact. The current $Al - based$ Ohmic contact module yields a contact resistance of $1.32 \pm 0.26\ \Omega mm$, compared to $0.86 \pm 0.58\ \Omega mm$ for a reference Au-based metallization scheme. Contact resistance is extracted from TLM data.

$GaN - on - Si$ wafers allow the highly-production of $AlGaN/GaN\ HEMTs$ in some of the many $CMOS$ fabs, traditionally used for the processing of Si devices.[62] This flexibility is an important consideration for these devices to be able to compete with Si power devices in terms of cost. Conventional metallization in III–V semiconductors is, however, based on $Au - contacts$, which are not allowed in Si fabs due to contamination issues.[63]

In the framework of the ON semiconductors project, $Au - free$ and $Au - based$ samples from $AlGaN/GaN - on - Si$ $MIS - HEMT$ have been fabricated with a $4 - inch\ Si\ CMOS$ compatible technology. Both samples have been investigated to compare the R_c behavior. The $Al - based$ contact resistance maps yield reduced R_c of $1.32 \pm 0.26\ \Omega mm$ for $Au - free$ compared to $0.86 \pm 0.58\ \Omega mm$ for conventional $Au - based$ Ohmic metallization scheme (figure 4-21). The higher contact resistance for the $Au - free\ HEMT$ is consistent with literature data[63] and clearly indicates the relevant role of gold in the achievement of low resistance to the $2DEG$ at the $AlGaN/GaN$ interface. In our investigation , the $Au - free$ contacts were not recessed which is regarded as an effective to method to reduce the contact resistance. Future works are expected in this topic.

4.6. SUMMARY

In this chapter the fundamentals of the Ohmic contact optimization have been discussed. The Ohmic contact formation to GaN has been investigated through the temperature dependence study of Al/Ti contacts to $Si\ Implanted\ N^{+}bulk\ GaN - on - sapphire$ substrate. Over a temperature range of $25 - 250$ °C, both the R_{sh} and the R_c decreases with temperature. For temperatures higher than 250 °C, the R_c abruptly increases which is linked with the physical degradation of the metal stack. Computed R_{sh} is significantly lower than the experimentally extracted R_{sh} suggesting partial activation of the dopants. The temperature dependence could be well fitted by the partial activation of dopants enhancement with the temperature with a donor level of 10 meV. It was suggested that, depending on the temperature range, TFE or FE dominates the transport across the metal–semiconductor interface yielding a contact resistance of $10^{-5} - 10^{-4}\ \Omega cm^2$.

The contact resistance temperature dependence was also investigated for an Ohmic contact to $HJ\ AlGaN/GaN\ HEMT$. For $Implanted\ N^{+}GaN$ contact both, R_{sh} $(850/700\ \Omega/sq)$ and R_c $(2.2/0.7\ \Omega mm)$ decrease with T $(25/250\ °C)$. Conversely, for $HJ\ AlGaN/GaN$ contacts, R_{sh} $(400/850\ \Omega/sq)$ and R_c $(0.2/0.4\ \Omega mm)$ increase with temperature. Physical models and nano-characterization techniques were used to fit the experimental resistance behavior. The submicron features of a typical $Ti/Al/Ni/Au$ Ohmic contact to $AlGaN/GaN$, with reduced R_c of $0.2\ \Omega mm$, have been investigated in detail, to understand the conduction mechanisms (spiking mechanism). This included $TLM\ vs\ T$ $(25 - 300\ °C)$ and a range of physical analysis tools like $SEM, FIB, TEM, and\ CAFM$. The results suggest that the preferential contact mechanism is a direct electron path between the electrons of the $2DEG$ and the metal stack, though only a small part of the contact is actually conducting.

Moreover, $Au - free$ contacts characteristics have been investigated. $GaN - on - Si$ wafers allow the highly-production of $AlGaN/GaN\ HEMTs$ in some of the many $CMOS$ fabs, traditionally used for the processing of Si devices. But contacts to $AlGaN/GaN$ must be $gold - free$ in a $CMOS$ line. A R_c map comparing $Au - free$ and Au content contacts, further corroborates the relevant role of $gold$ in the achievement of low resistance to the $2DEG$ at the $AlGaN/GaN$ interface.

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Chapter 5
AlGaN/GaN HEMT gate contact

5.1. INTRODUCTION

In this chapter the $AlGaN/GaN\ HEMT$ gate stack will be analyzed. The gate leakage current is an important limitation of the III–V $HEMTs$. In particular, minimizing the $Off-state$ leakage currents in $AlGaN/\ GaN\ HEMT$ is primordial to their implementation into systems with low noise and low power consumption.[1] This is particularly true when the GaN buffer is grown on Si. Its narrow bandgap, together with the lattice mismatch and the thermal expansion coefficient difference, makes the $AlGaN/GaN-on-Si$ stack challenging for sustaining high-voltages with low leakage.

To further understand the leakage origin and to investigate the gate area at the nanoscale, AFM is regarded as a unique tool for nano-characterization owing to its ability to locally deliver a desired stimulus to a very small area of the sample surface.[2,3] Furthermore, AFM has been successfully employed in several nanofabrication processes such as anodic oxidation or nanostructure direct writing by means of an adequate precursor. The AFM is also an ideal tool to link the nanoscale properties of solid-state

devices with behavior of the final device, the size of which is larger than a micron. In this sense, $AlGaN/GaN$ $HEMTs$ are devices which are greatly affected by the surface properties such as donor states, roughness or any kind of inhomogeneity.[4] The $2DEG$ (with excellent mobility and sheet concentration, typically 1600 cm^2 $V^{-1}s^{-1}$ and 1.0×10^{13} cm^{-2}) is only a few nanometers away from the surface and the transistor's forward and reverse currents are considerably affected by any variation of the surface property on the atomic scale. GaN technology continues to gain popularity and the $AlGaN/GaN$ $HEMT$ has emerged as one of the preferred power switches with a great potential for many applications.[1,5-8] It has therefore become necessary to control the Ohmic and gate contact properties and to improve the consistency of devices across a whole wafer.

A thin dielectric oxide layer is often introduced between the gate metal and the $AlGaN$ barrier layer resulting in a device known as a $MIS-HEMT$, which significantly suppresses gate leakage. It is also well known that a thin gate dielectric has a beneficial effect on the reliability of a transistor, the mitigation against current collapse being one such effect.[9,10] A number of gate dielectrics have already been investigated as the gate insulator for $AlGaN/GaN$ $MIS-HEMTs$ and in particular, SiO_2, Si_3N_4, Al_2O_3, and HfO_2.[9,11-15] Furthermore, it should be mentioned that many other insulators have been evaluated as the $HEMT$ surface passivation or the gate insulator, including $Sc_2O_3, Ga_2O_3, Gd_2O_3$ or NiO.[16-18]

Particularly, the attention will be focused in the experimental $HEMT$ and $MIS-HEMT$ comparison (i.e. $dynamic$ $I-V$ or traps characteristics $C-V$). HfO_2 has recently been demonstrated as a very promising gate dielectric candidate for $GaN-based$ high-power RF and high-voltage switches. Transistors with thin HfO_2 gate insulator have already exhibited minimal current slump, low $R_{on}, high-V_B$, and ultra-low leakage currents.[9,19-21]

In this sense, it had been analyzed the effect of introducing a HfO_2 gate dielectric on the electrical performance of the $HEMT$. The positive gate bias extended gate operation of the $MIS-HEMT$ and the effect of the gate insulator during a $dynamic$ $I-V$ stress test had been investigated. The DC, and $high-T$ stress tests have been performed and the HfO_2 based $MIS-HEMT$ approach yields the most promising results.

Since the $AlGaN/GaN\ HEMTs$ technology is still in its infancy, the long term reliability of the devices remains an open issue. It is well known that the hetero-structure contains surface states, deep traps levels, and traps at the hetero-interfaces that can drastically deteriorate the device robustness. Several approaches have been used to investigate the trap profile and to estimate the trap density by means of spectroscopy,[23] transient,[24] and steady-state electrical methods,[25-33] in particular, the investigation into the gate admittance varying with frequency.[29-33] This last approach is analogous to the well-known conductance method (first proposed by Nicollian and Goetzberger[34] in 1967) for MIS structures. Using the frequency dependent conductance analysis, it had been mapping the parallel conductance vs gate bias/frequency and further analyze the $slow$ and $fast$ traps as a function of the Fermi level for different gate architectures (Schottky and MIS). Besides, the variance in the band bending for fresh and stressed devices is determined.

In summary, the gate contact has an important role in the device performance and reliability, representing the most critical $HEMT$ element.

5.2. $HEMT$ SCHOTTKY GATE

In this section, $AlGaN/GaN-on-Si\ HEMT$ sample $C02$ was investigated by the macroscopic $I-V\ vs\ T$ approach and scanning probes at the nanoscale. Fabrication details are given in $chapter\ III$.

5.2.1. CONVENTIONAL DC ANALYSIS

At the macroscale, $HEMT\ \ DC$ device characteristics (forward and reverse) were measured at 15 °C intervals, from 25– 310 °C (figure 5-2 (a)) on a $Wentworth\ s200$ probe station with a heated chuck system. A $Keithley$ 2420 device analyzer for biasing the gate pad was used. The high-voltage characterization was performed using a $Keithley$ 2410 test system. The Si substrate was floating during the $HEMT\ DC$ tests. Two $I-V\ vs\ T$ measurements were also made across the drain–bulk and the gate–bulk to determine the vertical drain–bulk and gate–bulk currents, respectively. This was investigated further by means of a set standard test devices with $4/4/5\ \mu m$ for $L_{gs}/L_{gd}/L_g$. The device W was 150 μm. Typical forward $I-V$ curves for the $HEMTs$ under investigation are presented in figure 5-1 (a). The $HEMT\ \ RT$ drain-source

saturation current $(I_{ds,sat})$ at $V_{gs} = 0\ V$ is as high as $350\ mA/mm$. Figure 5-1 (b) shows the transfer curve $(I_{ds} - V_{gs})$ and its respective gate-source leakage current $(I_{gs} - V_{gs})$ for the $HEMT$. I_{gs} was determined to be in the range of $0.01 - 10\ \mu A/mm$ (depending on the temperature and the gate bias). The I_{ds} in the $Off - state$ was determined to be in the range of $10\ \mu A/mm$. The maximum transconductance value may be extracted from the derivative of the transfer curve as:

$$g_m = \partial I_{ds}/\partial V_{gs} \quad (5\text{-}1)$$

The maximum saturation transconductance $(g_{m,max})$ at $V_{ds} = 12\ V$ was determined to be $101\ mS/mm$. The relatively large value of $I_{ds,sat}$, (together with the $g_{m,max}$) correlates well with the low contact resistance value of $0.2\ \Omega mm$ described in the previous chapter. Reverse currents in the $Off - state$ are shown in figure 5-1(c) showing large drain-source voltages due to the WBG nature of the undoped GaN buffer. The breakdown voltage of this non-optimized high-voltage device was determined to be $\sim 400\ V$. The reverse $I - V$ (and vertical $I - V\ vs\ T$) tests were limited to $150\ V$ to avoid any degradation of the device during the test.

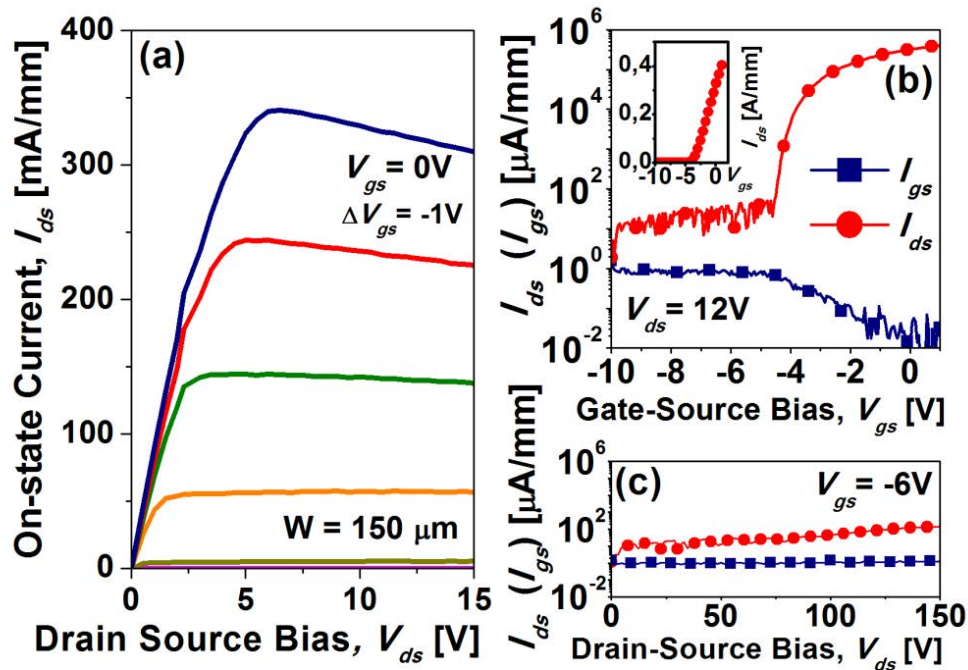

Figure 5-1. (a) $AlGaN/GaN$ $HEMT$ transistor forward $I - V$ curve at RT. (b) Typical transfer curve showing also the gate leakage current. (c) $AlGaN/GaN$ $HEMT$ transistor reverse currents with the gate biased at the $Off - state$.

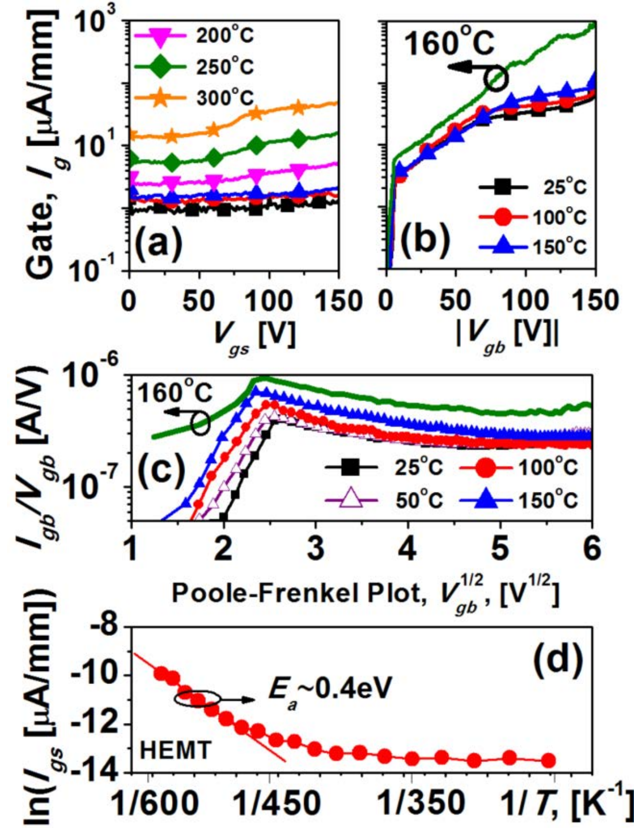

Figure 5-2. (a) Three terminals gate-source leakage current (for different temperatures) during the $Off-state$ reverse bias. (b) Two terminal gate-bulk reverse current showing severe degradation for $T > 160$ ℃ .(c) $Poole-Frenkel$ plot of the gate-bulk reverse current at varying T. (d) Arrhenius plot for the reverse gate current at $V_{ds} = -150\ V$ with activation energy of $E_a = 0.4\ eV$.

At elevated temperatures, the R_{on} is increased following a power law versus T, the exponent of which has been determined to be 1.4. The drain reverse current presents a double slope (linear/logarithmic) for each T, turning around 75 V of the reverse bias. The gate leakage does not depend on the reverse bias or the temperature up to 150 ℃. Then, I_{gs} appears to be constant $(V_{ds} < 75\ V)$ but strongly depending on T, thus suggesting a thermally activated process which follows an Arrhenius law:

$$I = I_0 \exp\left(-\frac{E_a}{k_B T}\right) \tag{5-2}$$

where E_a is the activation energy and k_B is the Boltzmann constant. From the Arrhenius plot $\log\{I_{ds}\}\ vs\ 1/T$, the activation energy can be determined as $E_a \sim 0.40\ eV$ (figure 5-2 (d)). Analogously, two terminals gate-bulk current $(I_{gb})\ I-V\ vs\ T$ measurements were also performed to determine the vertical I_{gb} (figure 5-2 (b)). The I_{gb} and I_{db} currents are relatively small as shown in figure 5-3.

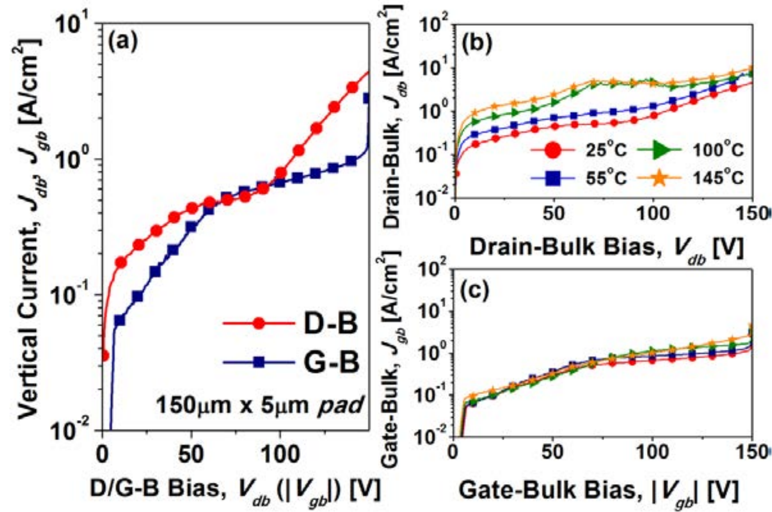

Figure 5-3. (a) Vertical drain–bulk and gate–bulk current density. (b) Drain–bulk current density (J_{db}) vs temperature. (c) Gate–bulk current density (J_{gb}) vs temperature.

Drain and gate leakage currents can be described in terms of an activation energy assuming a rate-limited thermally activated process following an Arrhenius law.[1] For $T < 150$ °C the leakage current exhibits a weak increase with T with $E_a \sim 0.02\ eV$. At higher temperatures the activation energy is much higher with $E_a \sim 0.20\ eV$ and $0.40\ eV$ for drain and gate leakage currents, respectively. In this case, I_{gb} greatly degrades when the current is forced through the $AlGaN$ region for $T > 160$ °C .The fact that the vertical I_{gb} is nearly independent of T suggests the tunneling as the dominant transport mechanism of the current flow. Indeed, a plot of $\log\{J/V^2\}$ vs $1/V$ (Flowler-Nordheim plot)[22] confirms the very weak temperature dependence. For the smaller gate-to-bulk bias $(V_{gb} < 10\ V)$, the measured macroscopic current densities are observed to be dependent on both the voltage and temperature. I_{gb} seems to follow the $Poole-Frenkel$ mechanism,[35-38] being linear in a $\log\{J/V\}$ vs $V^{1/2}$ plot (figure 5-2 (c)). The experimental emission barrier height was determined to be $\Phi_t = 0.3\ eV$, 25% lower than the one determined from the $HEMT's$ reverse thermal activation. In any case, it is believed that the emission is from a trap state to a continuum band of states, located somewhere within the bandgap associated with threading screw conductive dislocations.[35] This has been investigated at the nanoscale by means of the $CAFM$ technique.[39-41] Typical $AlGaN/GaN$ $HEMT$ Schottky gate contact was investigate of via $CAFM$ and high-resolution electron microscopy. These techniques allow us to observe the nanometric patterns of the current flow and to correlate them with the electrical device characteristics.

5.2.2. NANOSCALE *HEMT* CHARACTERIZATION

As mentioned before, $AlGaN/GaN$ $HEMTs$ are devices which are greatly affected by surface properties such as donor states, roughness or any kind of inhomogeneity. With the $2DEG$ charge centroid located around $4\ nm$ below the $AlGaN/AlN$ interface, the transistor forward and reverse currents are considerably affected by any variation of the surface properties on the atomic scale. Consequently, it has characterized the Ohmic and Schottky contacts on the nanometer scale using $CAFM$.[39-45] Here, it has attempted to understand and map the mechanisms involved in the current transport across the device terminals at the atomic scale.

At the nanoscale, the nano-electrical measurements were carried out with an AFM $Agilent$ 5100 (from Scientec), equipped with a conductive tip and a picoamplifier with an overall amplification of $10^{12}\ V/A$. An additional pA booster provided low pass filtering with a bandwidth of $400\ Hz$. The voltage output of the pA booster is sampled by the analog–digital converter of the AFM controller with a sampling rate of $65\ kHz$, yielding an rms noise level less than $30\ fA$. In this investigation, it has used Si tips coated by a metallic layer of Co/Cr and bulk diamond tips doped with boron (Boron $6000-8000\ ppms$) with a radius of $\sim 100\ nm$. The scan was performed in contact mode at a frequency of $0.5\ Hz$. To protect the samples from oxidation, the experiments were performed in dry nitrogen ambient, whilst the entire system is located within a Faraday chamber, thus minimizing any external interference. In these experiments, the surface was scanned with the tip grounded by applying a positive bias to the Si substrate; hence, the electrons were normally injected from the substrate to the tip.

A set of ~ 50 devices were completely characterized in the DC mode. We present a typical $HEMT$ device behavior in figure 5-1. Attending to the on–off ratio and low R_{on}, the device presented in figure 5-1 was one of the best devices, although all the set was comparable. Then we measured the TLM by the $HEMT$ (to extract the R_c) and we choose one of the best for the TEM cross-section and FIB machining. The Ohmic $CAFM$ measurement was made in several regions of this selected TLM device to ensure consistency. The Schottky $CAFM$ was performed in the selected device presented in figure 5-1.

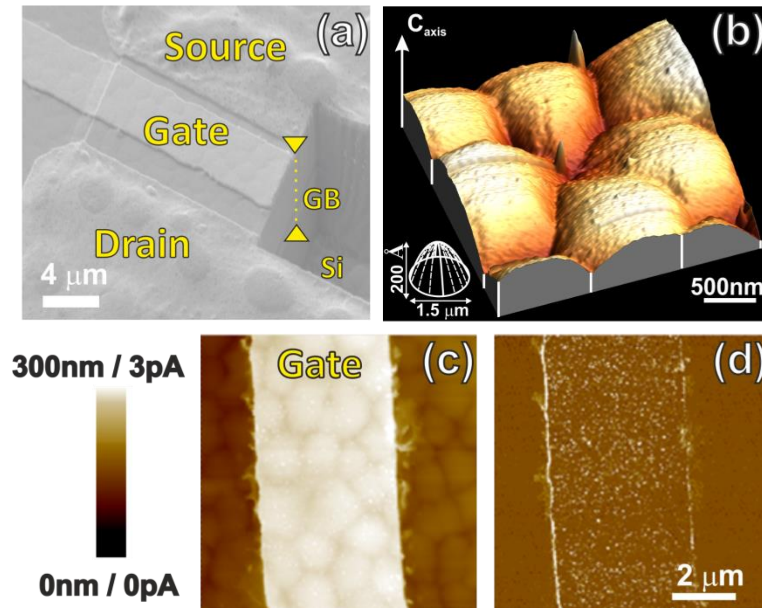

Figure 5-4. (a) SEM image of the $HEMT$ device. The FIB partial etch shows the depth of the GaN buffer. (b) $3D$ topographic image of the $HEMT$ surface. (c) Topography and (d) current map of $HEMT$' gate surface taken with the $CAFM$ for the $10 \times 10\ \mu m^2$ scan.

Again, a number of different regions and polarization conditions were used to be sure of the consistency. Figure 5-4 (a) presents a SEM view of the $HEMT$ surface and a FIB cross-section, where the Ohmic and the Schottky gate pads can be seen. A FIB etch on the gate region shows the GaN buffer (delimited by arrows) and the Si substrate. Rough, pitted morphologies were revealed from the $3D$ AFM shown in figure 5-4 (b). The surface roughness, calculated using a RMS function, is $5.1\ nm$ on a $10 \times 10\ \mu m^2$ scan area. The AFM image shows a pitted surface characterized by monolayer high-terraces, similar to those reported for growth on Si substrates.[46,47] The surface is composed of mounds, in the form of a truncated elliptic parabolic corresponding to the morphological pattern, schematized in the inset of figure 5-4 (b).

The mound size distribution is rather uniform with, on average, a base of $1.5\ \mu m$ and a height of $100 - 200$ Å (peak to valley distance). The GaN buffer mode of growth is a complex process from spiral growth to kinetic roughening resulting in the mound topography.[47] The strain in the upper AlN layer is almost totally relaxed and the $1.7\ \mu m$ thick GaN buffer layer is grown compressively strained. In the first stages of growth (below $0.7\ \mu m$), surface diffusion can be enhanced by the compressive strain, leading to spiral formation via a Burton, Cabrera and Frank (BCF) mode of growth. A coarsening of the growth mounds was observed and correlated to the dislocation density increase. It

is believed that the misfit strain due to the heteroepitaxial growth plays a key role in the crossover from screw dislocation induced spiral growth to kinetic roughening. As the growth proceeds, the strain relaxation increases and the surface diffusion decreases. This leads to a transition from step flow-dominated growth mode to a mixed growth mode, where $2D$ nucleation is sufficiently active to give rise to kinetic roughening. Therefore, for thickness above $0.7\ \mu m$, the mode of growth turns to a kinetic roughening characterized by the scaling behavior of the surface. After that, the MBE growth temperature is sufficiently low for avoiding thickness and composition modulation in the cap and barrier films.

Figure 5-4 (c) shows the morphological image of the gate region. The white area corresponds to the gate strip. Figure 5-4 (d) shows the current map of the gate region (gate electrode was floating). The current was found to be superior in the pad strip, when compared with the GaN cap surface, probably due to an improved drainage of electron in the vicinity of the tip. The high-current in the boundaries of the gate is believed to be due to a measurement effect. Higher resolution images of the gate pad area or the gate-to-drain source show that, with the application of sufficient vertical reverse voltage $(\sim -2\ V)$, there are preferential spots for the electron flow. This correlates with the vertical I_{gb} in figure 5-2 (b), (being actually $-V_{gb}$ the gate pad is depleting the $GaN\ cap/AlGaN/GaN$ surface).

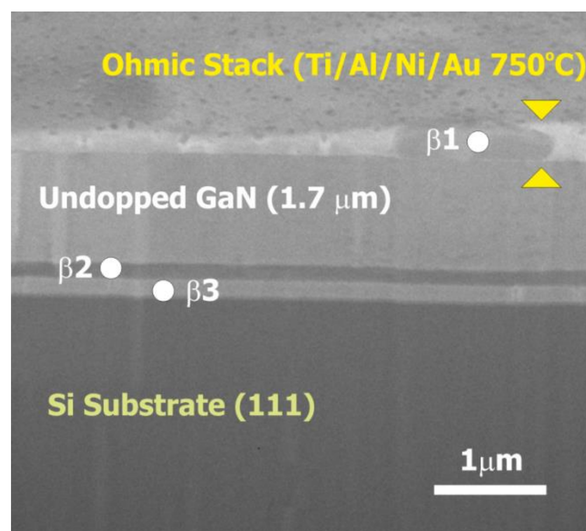

Figure 5-5. *SEM* cross-sectional image of the *AlGaN/GaN* active layers on the Ohmic contact region. β1 denotes the *Ni* clusters formed in the Ohmic region during the 750 ℃ contact annealing, which result in the relevant surface roughness. β2 and β3 are the *AlN* and *GaN* buffer growing layers respectively.

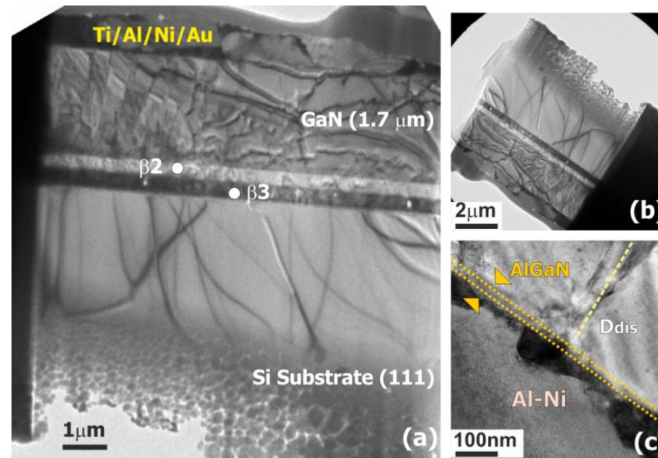

Figure 5-6. (a) TEM image of the $AlGaN/GaN-on-Si$ transistor showing the visible dislocations in the undoped GaN buffer and extending towards the Si substrate. (b) A micrograph of the TEM lamella mounted in the Cu holder ready for inspection. (c) A micrograph of the $AlGaN$ active layer with the Ohmic contacts on top.

This vertical current flows through a series of different materials and interfaces as depicted in the SEM and TEM images of figure 5-5 and figure 5-6. In the SEM image, $\beta 1$ denotes the Ni clusters formed in the Ohmic region during the 750 ℃ contact annealing. The relative abundance (determined by EDX) of $Ti/Al/Ni/Au$ seems to suggest that Ni has a tendency to stick together (in the areas marked as $\beta 1$), resulting in the rough surface.[48] We corroborated the presence of Au all over the metallic alloy except in the $Ni-rich$ clusters. It therefore appears that gold has a strong propensity to interdiffuse throughout the metallic layers, while it is also located at the $metal/AlGaN$ interface. $\beta 2$ and $\beta 3$ are the AlN and GaN buffer layers respectively (described in the device fabrication section). This multilayer stacking sequence makes the interpretation of the current mechanisms through the vertical Ohmic and the Schottky contacts rather difficult, but nevertheless some relevant facts can be pointed out.

Regarding AFM measurements configuration, we put a positive bias on the back of the Si and we ground the AFM tip. This is analogous to put a negative bias at the tip contact, and hence the $V_{tip} = -2\ V$ and $V_{tip} = -10\ V$ notation. Topographical images ($2.8 \times 2.8\ \mu m^2$) obtained with the AFM of the $HEMT$ surface (gate-drain spacing) are shown in figure 5-7 (a). The current profile of the same area, obtained with $CAFM$, shows the conductance distribution of the surface in figure 5-7 (b). It is then possible to obtain different current signals along any line, showed in figure 5-7 (c) for the biasing tip voltage of $-2\ V$ (right) and $-10\ V$ (felt). At$-2\ V$, the current flow is concentrated

within reduced areas, which appear as white spots in the image, (as in figure 5-7 (b)) uniformly located. In principle, depressions in the topography are somehow correlated with the current peaks in the current map (figure 5-7 (c)). Conductive areas in figure 5-7 (b), denoted as clear (white), means higher current through the tip ($\sim 6\ pA$) , thought this represents just 7% of the measured area $2.8\ \times 2.8\ \mu m^2$. Despite this, the current density of the conductive has been calculated to be as high as $2\ A/cm^2$ ($CAFM$ tip area was $\sim 300\ nm^2$).

As the $CAFM$ bias voltage increases up to $-10\ V$ (which is the maximum of the measurement set-up), this correlation between the topography and current becomes more evident which is clearly visible in bottom current map of figure 5-7. In this case, the mean current is $\sim 1\ pA$ with maximum current of $2.6\ pA$. The correlation, discussed previously, between the vertical reverse current and the gate-drain spacing are still valid for the tip biasing conditions of $2\ V$ and $10\ V$.

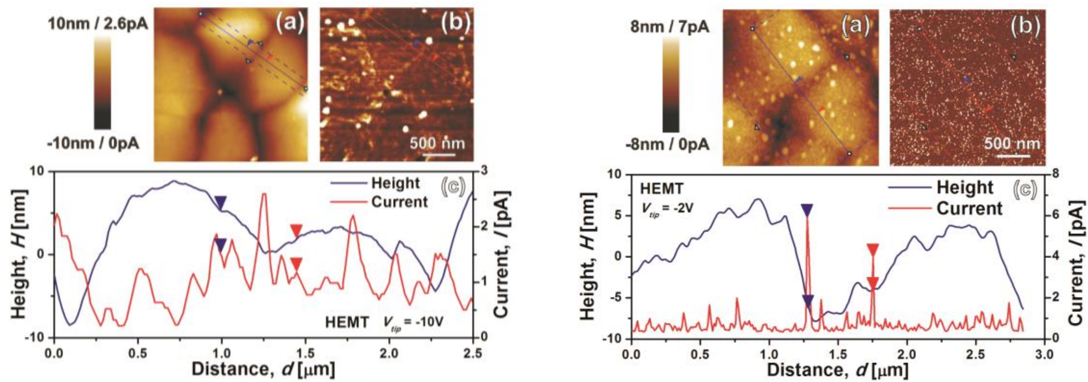

Figure 5-7. Conductive *AFM* scans of the *HEMT* surface in the drain-gate spacing with (a) topography and (b) current map of surface taken with the *CAFM* for the $2.8\ \times 2.8\ \mu m^2$ scan; (c) Respective cross-sectional profiles along the solid lines marked in (a) and (b) biased at $-2\ V$ (right) and $-10\ V$ (left).

However, neither all the depressions exhibit large local leakage nor all the mounds are immune to some current spike. This is shown in figure 5-8 (a) and figure 5-8 (b) along the lines $L1 - L10$ (the area scanned in figure 5-8 (b) is the same as in figure 5-7 (b) again with $V_{tip} = -10\ V$). The relative peaks (maxima) of any of the scan lines are identified as Δ_i. In some of the scans (such scan number $L7$ depicted in figure 5-8 (d)), some of the Δ_i peaks exhibit significantly higher current ($I\ > 5\ pA$) , when compared with any of the other relative current peaks. These peaks are labeled as Γ_i.

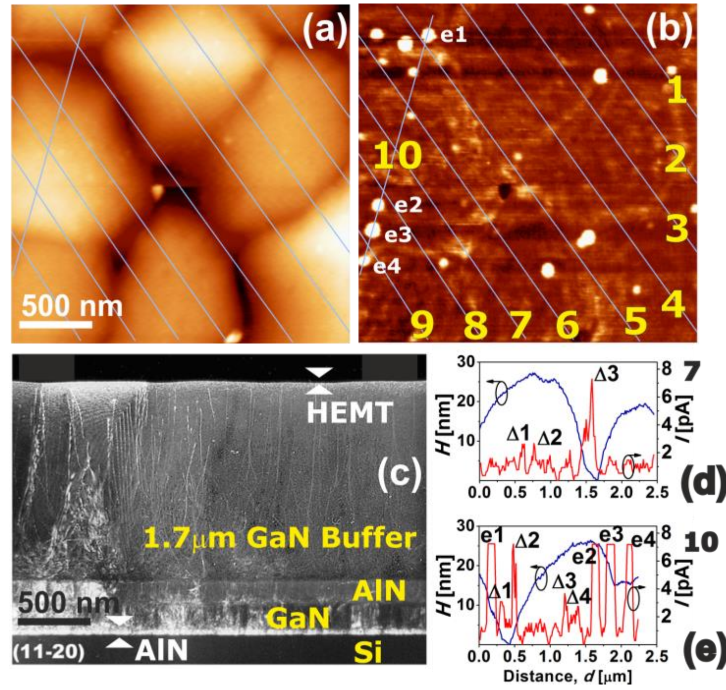

Figure 5-8. $CAFM$ **(a) topographic and (b) current map** $(V_{tip} = -10\ V)$ **showing the scan lines for the investigation of the correlation depressions vs leakage spots. (c) Cross-sectional** TEM **image of the** MBE GaN **grown on** AlN**. (d) Detailed scan through** $L7$ **showing the relative peaks** ($\Delta 1$, $\Delta 2$ and $\Delta 3$)**. (e) Detailed scan through line** $L10$ **where four high-current spots are found** ($e1 - e4$)**.**

We have observed that (for $L1 - L9$) the 67% of Γ_i peaks take place in depressions between mounds, formed during the first spiral growth stages. However, only the 36% of the Δ_i peaks correlate with a depression. These results suggest that, indeed, there is some correlation between large current peaks and depressions (as suggested in the $CAFM$ map of figure 5-8 (a) and figure 5-8 (b)), but in any case, the correlation is unique.

It is well know that there are many threading dislocations in GaN epitaxial layers and, these threading dislocations, create the boundaries of the network of the sub-grains, which enable the conductive vertical path. The dislocation density can be determined by either plain-view TEM or near-field AFM microscopy. Using both methods, the density of threading dislocations in our MBE GaN layers can be estimated to be $5 - 7 \times 10^9\ cm^{-2}$.[47] The presence of small pits or depression is associated with the emergence of threading dislocations. Depressions linked to two (or a multiple of two) molecular step edge are associated with screw-type dislocations, while the other are connected to edge-type dislocations located at the crystallographic sub-grain boundaries. GaN mounds (also known as hillocks) form around pure screw and/or mixed dislocations. It

has been widely reported[46,49-53] that spots with enhanced conductivity are related with threading dislocations. In our case, these conductive dislocations appear to have a certain tendency to appear in the depressions, but one only can expect to find them all over the surface. This can be explained by the GaN buffer mode of growth.[47] In a similar $CAFM$ study carried out in $GaN - on - sapphire$ ($350\ nm\ MBE\ GaN$), it was found that only $\sim 10\%$ of growth mounds exhibited current leakage paths.[53] It was postulated then that $\sim 90\%$ of hillocks grown around mixed dislocations, while the remaining $\sim 10\%$ grow around pure screw dislocations. These pure screw dislocations (with a density of $\sim 5.0 \times 10^8\ cm^{-2}$) were the solely responsible of the observed leakage paths. The two-regimen mode of growth of the $GaN - on - Si$ can explain this difference. As stressed before, when the $GaN\,(0001)$ is MBE grown on the AlN layer, screw dislocation induced spiral growth takes place up to a thickness of $0.7\ \mu m$. Then, the screw dislocation induced spiral growth turns to kinetic roughening and the threading pits are visible no more on the top of the mounds (the final GaN thickness was of $1.7\ \mu m$).

One additional feature is clearly visible in the figure 5-8 (b) scan. The line $L10$ analyzes four ($e1$– $e4$) of the strongly conductive spots in figure 5-8 (e) (these spots are not visible when the tip is biased at $-2\ V$ (figure 5-7 (b) top)). These spots have a diameter of $130 - 140\ nm$ and the current peak is larger than the saturation established at $7.5\ pA$. The frequency of these spots is significantly lower than the expected for the threading dislocations (the estimated density according the $CAFM$ map would be $\sim 6\ \mu m^{-2}$). Both the size and the density of the highly conductive spots appear to correlate with the reported distribution of nanopipes.[47]

These nanopipes were commonly observed (with a density of $\sim 2.0\ \times 10^8\ cm^{-2}$ and a diameter of $100 - 200\ nm$) in the first stages of the heteroepitaxial growth of GaN regardless the growth method and the substrate used.[46,47] They are systematically ignored as they vanished for thickness larger than $0.7\ \mu m$, again when the screw dislocation induced spiral growth turns to kinetic roughening. However, these nanopipes present in the bulk of the GaN layer may enable highly conductive path when the vertical current is sufficiently high. It should be noted that the spots are not visible when the scan is performed at $-2\ V$ (figure 5-8 (c) top). The fact of having these nanopipe-conduction paths active for tip voltages larger than $V_{tip} = -10\ V$ correlates well with the double

conduction mechanism observed during the $I-V\ vs\ T$ microscale measurements resulting in dislocation related $Poole-Frenkel\ (-V_{gb} < 10\ V)$ and $Flowler-Nordheim$ tunnelling $(-V_{gb} > 10\ V)$, respectively.

Another significant difference comes from the fact that, in our experiments, the $CAFM$ current is analyzed using a vertical configuration (forcing the electrons though the entire GaN buffer), rather than in the commonly reported lateral configuration. Pure edge-type dislocations located at the crystallographic sub-grain boundaries may be more effective in this case. To further analyze the current mechanisms through the $AlGaN/GaN$ buffer we have made $I-V\ vs\ T$ measurements through the I_{gb} (figure 5-3 (c)). It has been suggested that only a negligible contribution to the reverse-bias current comes from thermionic emission over the Schottky barrier due to the large barrier heights typical in GaN.[22] For the smaller gate-to-bulk bias $(-V_{gb} < 10\ V)$, the measured macroscopic current densities are observed to be dependent on both the electric field and temperature. In this case, I_{gb} can be fitted by using the $Poole-Frenkel$ mechanism or emission either into or from dislocation-related trap states or conduction along dislocation lines.[35-38] A high-density of dislocations within the GaN stacked structure is visible from TEM images depicted in figure 5-6. $Poole-Frenkel$ emission is a trap-mediated carrier transport mechanism where the carrier density depends exponentially on the activation energy of the traps, which is corrected for the electric field, such that the current density is given by:

$$\frac{J}{E} \sim exp\left(-\left(q\Phi_t/k_BT - m_{PF}\sqrt{E}\right)\right) \quad where \quad m_{PF} = \sqrt{\left(q/\pi\varepsilon_{s,\infty}\varepsilon_0\right)/k_BT} \tag{5-3}$$

Where $\varepsilon_{s,\infty}$ is the high-frequency relative dielectric permittivity, ε_0 the permittivity of free space and Φ_t the barrier height for electron emission from a trap state. The linear dependence of $\log J/V$ on $\sqrt{V}$ is an indication of the validity of the trap assisted conduction mechanism model. The emission barrier height was measured as $\Phi_t = 0.3\ eV$, 25% lower than the one determined from the $HEMT's$ reverse thermal activation. It is believed that the emission is from a trap state to a continuum of states located somewhere within the bandgap associated with threading screw conductive dislocations.[35] This dislocation/trap assisted mechanism correlates mainly with the depressive regions of the surface maps of the $CAFM$ technique (being approximately 10% of the surface area).

For $-V_{gb} < 10\ V$, the vertical I_{gb} appears to be weakly dependent on T, suggesting that tunneling is likely to be the dominant current transport mechanism. Hence, the current density can be described by the $Fowler-Nordheim$ equation,[22] which describes the field emission of quantum tunneling electrons from bulk metals as:

$$\frac{J}{E^2} \sim exp(-m_{FN}/E) \ \ where \ m_{FN} = (3qh)^{-1} 8\pi \sqrt{2m^*(q\Phi_B)^3} \qquad (5\text{-}4)$$

Where E is the electric field in the semiconductor barrier, q is the electronic charge, Φ_B is the effective barrier height at the Schottky contact and m^* is the GaN effective mass.[4] It is then possible to plot a log-scale plot of J/V as a function of $1/V$, which confirms a very weak temperature dependence. In a totally crude approximation, if we only consider the GaN buffer as the conductive layer, some evaluation of the effective barrier height can be done. Assuming an effective mass of $0.22m_0$ the average effective barrier height was determined to be in the range of $0.7\ eV$.

5.3. $HEMT$ MODELING

In the previous section it has been described the main properties of the $HEMT'$ gate contact at micro and nanoscale. In this section, how this gate drives the $HEMT$ is analyzed by physical based modeling.

It had been characterized $HEMT\ C02$ in the temperature range of $25 - 300$ °C. Then, simple analytical closed-form expressions for the $HEMT$ transfer, drain saturation and gate transconductance are proposed. These closed forms are based on physical modeling of the $2DEG$. The model includes the effect of the source–drain series resistance along with the self-heating. The fit with the experimental results is remarkably good, as it will be shown further on.

5.3.1. EXPERIMENTAL $HEMT$

The $AlGaN/GaN\ HEMT$ experimental saturation current and transconductance $vs\ T$ have been characterized. Typical forward $I-V$ curves for the $HEMTs$ under investigation are presented in figure 5-9. The device dimensions are $4/4/5\ \mu m$ for $L_{gs}/L_{gd}/L_g$. The gate W is $150\ \mu m$. $HEMT$ device characteristics were obtained in the temperature range of $25-310$ °C on a probe station $Wentworth\ s200$ with heating chuck system, using an incremental ΔT of 15 °C. Figure 5-9 (a) and (b) show typical

$I_{ds} - V_{ds}$ and $I_{ds} - V_{gs}$ $vs\ T$ curves. The $HEMT\ RT\ I_{ds,sat}$ at $V_{gs} = 0\ V$ is $350\ mA/mm$, while at 300 °C, $I_{ds,sat}$ is reduced to $100\ mA/mm$ (figure 5-9 (b)). The V_{th} remains remarkably constant at $V_{th} \sim -4.2\ V$ regardless of the elevated T. This small variation of the V_{th} with T is consistent with the fact that the polarization field is weakly dependent on the temperature[54] and hence, the sheet carrier concentration is virtually temperature independent. The temperature dependence of the $I_{ds,sat}$ and (saturation) transconductance, expressed by:

$$g_m = \partial I_{ds}/\partial V_{gs} \tag{5-5}$$

at $V_{ds} = 12\ V$ are shown in figure 5-9 (c) and (d), respectively. g_m has been fitted by an inverse power law with the temperature $T^{-\alpha}$ in which temperature coefficient (α) was determined to be 1.1. This α value is in agreement with previous reports for $AlGaN/GaN\ HEMTs - on - Si$. Tan *et al.*[55] reported a temperature dependence of the saturation current as a power law of $T^{-\alpha}$, with α depending on the channel length. For a gate length in the range of 1– 10 μm, α was found to be in the 0.8– 1.4 range ($T^{-1.5}$ for $L_g = 100\ \mu m$). Nevertheless, for submicron gate lengths, it was found that α was only 0.5.

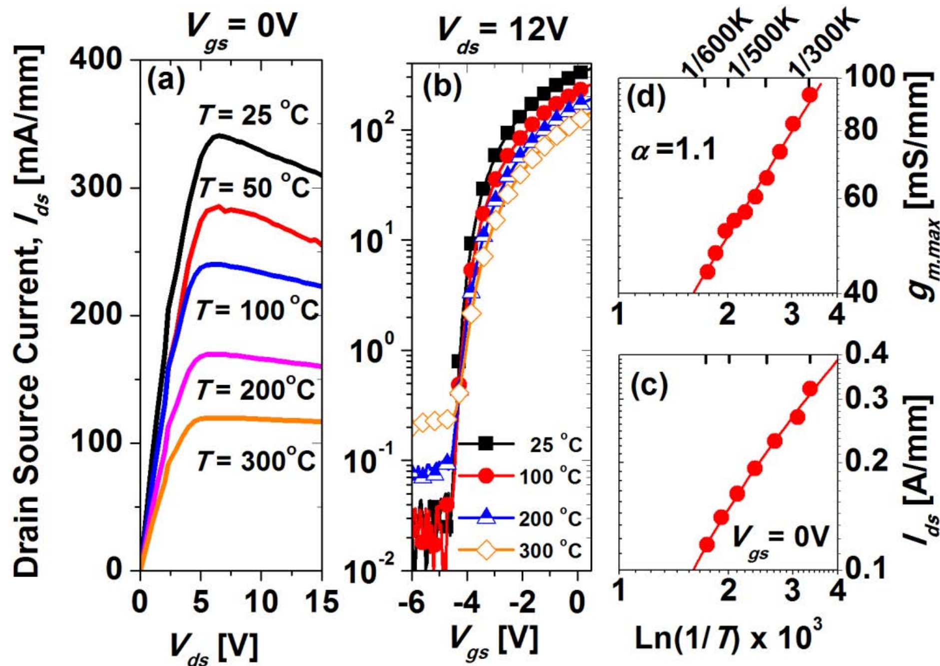

Figure 5-9. Experimental (a) drain current I_{ds}–V_{ds} and (b) I_{ds}–V_{gs} in the temperature range of $5 - 300$ °C . Experimental (c) saturation current $(I_{ds,sat})$ versus temperature at $V_{gs} = 0\ V$ and $V_{ds} = 12\ V$ and (d) maximum gate transconductance $(g_{m,max})$ versus temperature. α indicates the temperature dependence as $g_{m,max} \sim T^{-\alpha}$.

However, it is worth mentioning that there is a relevant dispersion of the reported α values given in the literature[56] (and references therein) which apparently depends on the substrate ($Si, SiC\ or\ sapphire$), the presence of AlN spacing, the criteria to determine the saturation current and others.

5.3.2. IDEAL *HEMT*

In this section, a closed-form expression for the $HEMT$ saturation current and transconductance will be presented. The model includes the effect of the source–drain series resistance along with the self-heating in a simple closed-form analytical formula for the $I_{ds,sat}$. It is well known that the ideal $HEMT$ drain current (figure 5-10) can be determined along the channel from the source side of the gate edge ($z = 0$) by:[54,57]

$$I_{ds}(z) = qWv(z)n_s(z) \tag{5-6}$$

Where W is the channel width, $n_s(z)$ is the electron sheet carrier concentration and q is the electron charge. $v(z)$ is the electron drift velocity along the channel which, using the field-dependent-mobility model, can be expressed by:

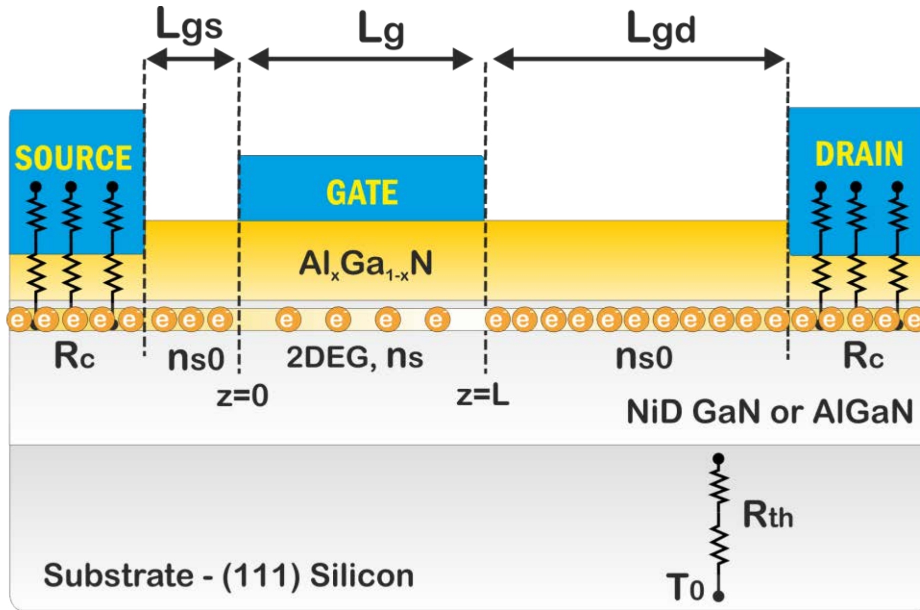

Figure 5-10. Schematic cross-sectional view of the $AlGaN/GaN$ $HEMT$ under investigation.

$$v(z) = \frac{\mu_n(z)E(z)}{1 + a\,E(z)/E_{crit}} \tag{5-7}$$

Here, μ_n is the electron mobility in the $2DEG$ channel, E is the electric field along the channel, a is an adjustable parameter and E_{crit} is the critical electrical field. Performing

integration of the electric field of *eq.* (5-6) between the limits $0 < z < L_g$, the drain current could be determined. The critical electric field and the saturation carrier mobility are then related by:

$$2v_{sat} = \mu_n E_{crit} \tag{5-8}$$

Where v_{sat} has been determined by Monte Carlo simulations[54] as being:

$$v_{sat} = v_0 + \xi_0 T \tag{5-9}$$

Where $v_0 = 2.87 \times 10^7\ cm/s$ and $\xi_0 = -9.8 \times 10^3\ Kcm/s$. Therefore, the computation of the model requires formulation for the electron mobility and the $2DEG$ sheet carrier concentration.

5.3.2.1. $2DEG$ MOBILITY

The main scattering mechanisms in a $2DEG$ channel are well reported.[58] The $2DEG$ mobility is modeled analytically as the sum of several contributions following the Mathiessen rule.

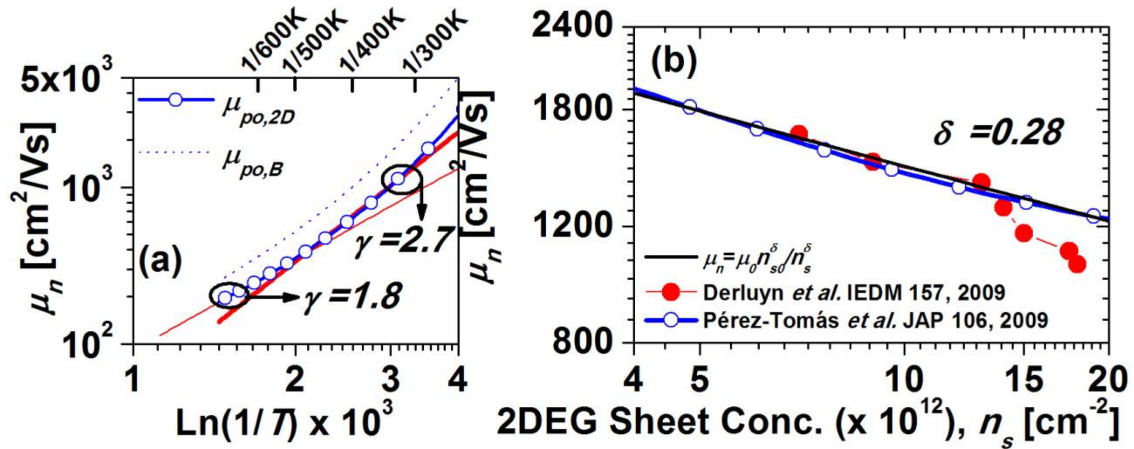

Figure 5-11. Simulated $2DEG$ mobility (bulk and $2DEG$) dependence on (a) the temperature ($n_s = 1.0 \times 10^{13}\ cm^{-2}$) and (b) the sheet carrier concentration ($T = 300$ ℃).

However, the polar optical phonon scattering ($\mu_n \simeq \mu_{po}$) is the dominant scattering mechanism for the $2DEG$ in a wide temperature range. At elevated T the impurity scattering is minimized due to the spatial separation of electrons and ionized impurities, being especially true for temperatures above $300\ K$.[58,59] Equations in[59,60] describe this mobility for a $2DEG$, using the conventional relaxation-time approximation, for the case

when the optical-phonon energy is greater than the thermal energy. Simple empirical relationships for the polar-optical mobility have been proposed in previous works:[61,62]

$$\mu_n \simeq \mu_{po} = \frac{C}{n_s^{\delta} T^{\gamma}} = \mu_0 \left(\frac{n_{ref}}{n_s}\right)^{\delta} \left(\frac{T_{ref}}{T}\right)^{\gamma} \tag{5-10}$$

Where C, δ and γ are empirical constants for describing the dependence on the n_s vs T. C can also be expressed in terms of the reference $2DEG$ concentration (n_{ref}), temperature (T_{ref}) and its reference mobility (μ_0) as $C = \mu_0 n_{ref}^{\delta} T_{ref}^{\gamma}$. In practice, $T_{ref} = 300\ K$ and $\mu_0 = \mu_n(V_{gs} = 0\ V)$ then, $n_{ref} = n_s(V_{gs} = 0\ V) = n_{s,0}$. This expression for the low field mobility is very useful since it relates μ_n to n_s (and hence, V_{gs}) and the temperature. Mobility constants of $\gamma = 1.8 - 2.7$ (figure 5-11 (a)) and $\delta = 0.28$ (figure 5-11 (b)) have been fitted to the theoretical computed $\mu_{2DEG,po}$[61,63] of with $(\hbar_{\omega 0} = 91.2\ MeV,\ m^*/m_0 = 0.2,\ \varepsilon_s = 8.9\ and\ \varepsilon_{s,\infty} = 5.35)$ for $n_s = 1.0 \times 10^{13} cm^{-2}$ and $T = 300\ K$, respectively.

Nevertheless, it is also well known[59] that GaN optical-phonon energy $(\hbar_{\omega 0} \sim 90\ MeV)$ is high-compared to the energy separation of the sub-bands. The energy separation between all sub-bands, except for the first and second, is very small $(< 1 MeV)$ resulting in a highly inelastic nature of polar optical scattering. This could make the total scattering rate to be the sum of many intersub-band and intrasub-band scattering processes, when the n_s concentration is high. This would result in a depreciation of the characteristic features of the $2DEG$, in particular, the density of electrons within the potential well. For this reason, the relaxation time for scattering of electrons in this $2DEG$ by optical phonons would tend to the bulk relaxation time. Therefore, electron mobility may be described, in that case, using any of the expressions for polar optical scattering in bulk semiconductor $\mu_{B,po}$ electron mobility.[59] As it can be inferred from figure 5-11 (a), the theoretical dependence of the electron mobility on the temperature does not differ substantially if a quantified $2DEG$ or bulk polar phonons are considered. It is worth mentioning that the value of γ is significantly higher than the experimental value extracted from the g_m variation with T. Nevertheless, the value of $\delta = 0.28$ is in agreement with previous works reported in the literature.[63]

5.3.2.2. $2DEG$ SHEET CHARGE DENSITY AND V_{th}

In first approximation, the sheet-carrier density n_s, for a given gate bias and for low electric fields, can be approximated by:[64]

$$n_s = \frac{C_b}{q}\left[V_{gs} - V_{th}\right] \tag{5-11}$$

Where C_b is the gate capacitance. Taking into account the different band discontinuities, the gate capacitance is the sum of several contributions:

$$C_b^{-1} = C_{cap}^{-1} + C_{barrier}^{-1} + C_{spacing}^{-1} + C_{\Delta d}^{-1} \tag{5-12}$$

including the GaN cap, the $AlGaN$ barrier, the AlN spacer layer and the contribution of the distance of the electron gas from the spacer layer $C_{\Delta d}$. Each of these contributions is of the form $C_i = \varepsilon_i/d_i$. The dielectric constant ε_i for the GaN and $Al_xGa_{1-x}N$ can be determined from the approximation $\varepsilon(x) = -0.5x + 9.5$.[65] The polarization-induced charge into the calculation of the threshold voltage is given by:

$$V_{th} = \Phi_B - \Delta E_c - qC_b^{-1}P_T \tag{5-13}$$

Here, Φ_B is the Schottky barrier height, ΔE_c is the conduction band offset at the $AlGaN/GaN$ interface and P_T is the total polarization charge. It is worth mentioning that according to the exact self-consistent solution of the $1D$ Poisson's and Schrödinger equations,[57,65] the sheet carrier concentration is:

$$n_s = C_b q^{-1}\left[V_{gs} - V_{th} - E_F(n_s)\right] \tag{5-14}$$

Where E_F is a function of n_s. A polynomial approximation for E_F in terms of n_s as $E_F = k_1 + k_2\sqrt{n_s} + k_3 n_s$ has been proposed.[57] This expression includes three temperature-dependent parameters k_1, k_2 and k_3, which have been numerically determined.[54] It can be demonstrated, by performing some algebra of $n_s(E_F)$, that n_s can still be described as an analytical function of the gate voltage as:

$$n_s = \frac{1}{4\Gamma^2}\left[-k_2 + \sqrt{k_2^2 + 4\Gamma\left(V_{gs} + V_{th} + k_1\right)}\right]^2, where\ \Gamma = \left(k_3 + qC_b^{-1}\right) \tag{5-15}$$

In any case, as stressed before, the polarization field is a weak function of the temperature. Therefore, V_{th} and n_s can be considered weakly dependent on the temperature, as it was experimentally assessed (figure 5-9 (b)).

5.3.2.3. INTRINSIC DRAIN CURRENT

If no extrinsic source and drain resistance are considered, the sheet carrier concentration along the channel could be described as:[57]

$$n_s = \varepsilon_r/qd\left[V_{gs} - V_{th} - V(z)\right] \tag{5-16}$$

Rearranging *eq.* (5-6) and (5-7), including the low-field electron mobility *eq.* (5-10) and then performing integration between the limits $0 < z < L_g$, the drain current could be expressed as:

$$I_{ds} = \frac{C_b W C E_{crit} V_{ds}}{2T^{\gamma}\left(V_{ds} + aE_{crit}L_g\right)}\left[\frac{2q}{C_b} n_s^{1-\delta} - V_{ds} n_s^{-\delta}\right] \tag{5-17}$$

The drain-source saturation voltage ($V_{ds,sat}$) current can be determined assuming the condition of $\partial I_{ds}/\partial V_{ds} = 0$ (i.e. at the knee voltage establishing the onset of the saturation), with:

$$V_{ds,sat} = \sqrt{\left(L_g E_{crit}\right)^2 + 2L_g E_{crit}\left(V_{gs} - V_{th}\right)} - L_g E_{crit} \tag{5-18}$$

After performing some algebra it is possible to arrive at the expression: [66]

$$I_{ds,sat} = \frac{2WC_b}{L_g}\mu_n\left(V_{gs} - V_{th}\right)^2\left[1 + \sqrt{\left(1 + \frac{2\mu_n\left(V_{gs} - V_{th}\right)}{\upsilon_{sat}L_g}\right)}\right]^{-2} \tag{5-19}$$

For long-channel $HEMTs$, in first approximation, it can be considered that the Shockley model (constant-electron-mobility model) may be assumed, yielding the well-known simplified expression: [66]

$$I_{ds,sat} = \mu_n \frac{WC_b}{2L_g}\left(V_{gs} - V_{th}\right)^2 \tag{5-20}$$ [66]

Then, considering $n_s = q^{-1}C_b\left(V_{gs} - V_{th}\right)$ and $\mu_n = C/n_s^{\delta}T^{\gamma}$, we can rewrite the previous equation as:

$$I_{ds,sat} = i_0 = \frac{q^2 CW}{2C_b L_g T^{\gamma}} n_s^{2-\delta} \tag{5-21}$$

Derivating this expression it is possible to obtain an expression for the intrinsic transconductance g_{m0} as:

$$g_{m,sat} = g_{m0} = \frac{qCW}{2L_g T^{\gamma}} (2-\delta) n_s^{1-\delta} \tag{5-22}$$

5.3.2.4. EXTRINSIC DRAIN CURRENT

Using this extremely simple equation, the experimental versus simulated fitting is only good for the smallest $V_{gs} - V_{th}$ (where the intrinsic and the extrinsic transconductance are not substantially different). For larger V_{gs}, the model could be improved to take into account gate-drain series resistance, self-heating and other degradation mechanisms. To take into account the series resistance, the saturation voltage in the definition of *eq.* (5-21) can be substituted by:

$$V_{ds} = V'_{ds} - I_{ds} R_{DS} \tag{5-23}$$

The total resistance (R_{DS}) is:

$$R_{DS} = 2R_c + R_{sg} + R_{gd} \;\; where \; R_{sg} = R_{sh}(L_{gs} W); \;\; R_{gd} = R_{sh}(L_{gd} W) \tag{5-24}$$

The $2DEG$ channel sheet resistance (R_{sh})is expressed by:

$$R_{sh} = \frac{1}{q n_{s0} \mu_n} \tag{5-25}$$

Where n_{s0} is the electron sheet carrier concentration at $V_{gs} = 0\,V$. It can be then demonstrated that *eq.* (5-21) modifies to:

$$I_{ds,sat} = i_{0,R_{DS}} = i_0/(1+\Delta) \quad \text{where} \quad \Delta = \frac{qCW}{2L_g T^{\gamma}} R_{DS} n_s^{1-\delta} \tag{5-26}$$

5.3.2.5. $HEMT$ WITH EXTRINSIC RESISTANCES

There are several ways to include the effect of the extrinsic source and drain resistances in the $HEMT$ drain current.

Here, we use the drain voltage and gate voltage substitution by:

$$V_{ds} = V'_{ds} - I_{ds}R_{DS} \;\; and \; V_{gs} = V'_{gs} - I_{ds}R_S \tag{5-27}$$

The total access resistance R_{DS} is the sum of the source to gate and gate to drain regions contributions:

$$R_{DS} = R_S + R_D = 2R_c + R_{sg} + R_{gd} \tag{5-28}$$

Applying this substitution to *eq.*(5-17) and rearranging, the *HEMT* current can be determined by:

$$I_{ds,R} = \left[\frac{2I_3}{I_2 + \sqrt{I_2^2 - 4I_1I_3}}\right] \tag{5-29}$$

$$I_1 = \beta(2R_SR_{DS} - R_{DS}^2) + aR_{DS} \tag{5-30}$$

$$I_2 = (L_gE_{crit} + aV_{ds}) - \beta\left(2V_{ds}R_{DS} - 2V_{ds}R_S - 2R_{DS}\frac{qn_s}{C_b}\right) \tag{5-31}$$

$$I_3 = \beta\left(\frac{2qn_s}{C_b}V_{ds} - V_{ds}^2\right) \tag{5-32}$$

$$where \;\; \beta = \frac{C_bWE_{crit}C}{2n_s^{\delta}T^{\gamma}} \;\; ; \;\; \frac{qn_s}{C_b} = (V_{gs} - V_{th}) \tag{5-33}$$

$I_{ds,R}$ reduces to *eq.* (5-17) for R_{DS} and $R_S \rightarrow 0$. For the saturation current in particular, it can be demonstrated that, after performing simple algebra in *eq.* (5-6), *eq.* (5-23) can be rewritten as, (applying again the simplification $n_s = 0$ for $V_{sat}(L)$):

$$I_{ds,sat,R} = \frac{i_0}{1+\Delta} = \left[1 + \left(\frac{qCW}{2L_gT^{\gamma}}R_{DS}n_s^{1-\delta}\right)\right]^{-1} \frac{q^2CW}{2C_bL_gT^{\gamma}}n_s^{2-\delta} \tag{5-34}$$

Where Δ is defined as $\Delta = \left(\frac{qCW}{2L_gT^{\gamma}}R_{DS}n_s^{1-\delta}\right)$. The intrinsic saturation gate transconductance can be determined from the derivative of this expression:

$$g_{m,sat,R} = \frac{\lambda C_b}{q(1 + \varphi n_s^{1-\delta})^2}\left[(2-\delta)n_s^{1-\delta} + \varphi n_s^{2-2\delta}\right] \tag{5-35}$$

$$where \;\; \lambda = \frac{q^2CW}{2C_bL_gT^{\gamma}} \; ; \; \varphi = \frac{\Delta}{n_s^{1-\delta}} = \frac{qCW}{2L_gT^{\gamma}}R_{DS} \tag{5-36}$$

5.3.2.6. $2DEG$ CHANNEL SELF-HEATING

The $2DEG$ channel self-heating usually has a strong effect on the effective channel temperature of the $HEMT$ which can be, in turn, significantly greater than the ambient (or chuck) temperature. Therefore, self-heating is a virtually unavoidable parameter affecting the $high-T$ performance of any $HEMT$, particularly when biased in the saturation regimen. Besides, due to the high-level of power handled by the $2DEG$ channel in the $AlGaN/GaN$ $HEMTs$, self-heating effects may become very relevant for relatively small drain/gate bias (depending on $I_{ds}-V_{ds}$). Basically, the self-heating increases the channel temperature to an effective temperature $\left(T_{eff}\right)$. This effective temperature depends on the dissipated power, the thermal impedance (R_{th}) and the substrate temperature (T_{sub}) as: [54]

$$T_{eff} = R_{th} I_{ds} V_{ds} + T_{sub} \tag{5-37}$$

The substrate temperature (at the substrate bottom) also increases linearly with the temperature depending on the thermal resistance of the package $\left(\lambda_p\right)$. In many practical cases, such as during on-wafer measurements, it is reasonable to consider the substrate temperature as the heat-sink temperature:

$$T_{sub} = T_0 + \lambda_p I_{ds} V_{ds} \simeq T_0 \tag{5-38}$$

Considering that the $HEMT$ active layers (GaN cap, $AlGaN$ buffer, GaN channel, buffer layers, etc) are very thin compared with the total substrate thickness, they can be neglected in the computation of the thermal impedance of the structure. R_{th} may be roughly approximated by: [54,67]

$$R_{th} = \frac{1}{\pi k} \ln \frac{8 d_{sub}}{\pi L_g} \tag{5-39}$$

Where d_{sub} is the substrate thickness, L_g is the channel length and kappa (k) is the thermal conductivity of the substrate. The thermal conductivity has been experimentally assessed for SiC, $sapphire$ and Si substrates as: [67,68]

$$k_{SiC} = 3.4\left(\frac{T}{300}\right)^{-1.5} \quad k_{sapphire} = 0.49\left(\frac{T}{300}\right)^{-1.0} \quad k_{Si} = 1.57\left(\frac{T}{300}\right)^{-1.4} \tag{5-40}$$

It is well known that SiC material exhibits better thermal conductivity when compared to Si and, in particular, to $sapphire$. The value of the thermal conductivity at room temperature is 3.4 W/cmK, 0.49 W/cmK and 1.57 W/cmK, for SiC, $sapphire$, and Si.[68] It should be mentioned that the value of kappa slightly varies depending on the reference[69-71] but still, from the point of view of the heat spreading, SiC is the better substrate and $sapphire$ is the worst, with the device on Si being somewhere in the middle. The effect of the self-heating could be analytically estimated for the saturation current in *eq.*(5-34). The saturation current suffering self-heating effects, $I_{ds,SH}^{sat}$, could be expressed of the form:

$$I_{ds,SH}^{sat} T^{\gamma} + I_{ds,SH}^{sat} \Delta' = i_0' \; where \; i_0' = i_0 T_0^{\gamma} \; and \; \Delta' = \Delta T_0^{\gamma} \tag{5-41}$$

Then, from *eq.* (5-37):

$$I_{ds,SH}^{sat} \left(1 + \alpha_{SH} I_{ds,SH}^{sat}\right)^{\gamma} + I_{ds,SH}^{sat} \Delta = i_0 \quad where \quad \alpha_{SH} = R_{th} V_{ds} / T_0 \tag{5-42}$$

This non-linear equation is not analytical. Nevertheless, it could be approximated by the three first terms of the binomial series (which is the Taylor series for small y) of the function $(a + y)^n$:[72]

$$(a + y)^n = a^n + n a^{n-1} y + \frac{n(n-1)}{2!} a^{n-2} y^2 + \frac{n(n-1)(n-2)}{3!} a^{n-3} y^3 + \cdots \tag{5-43}$$

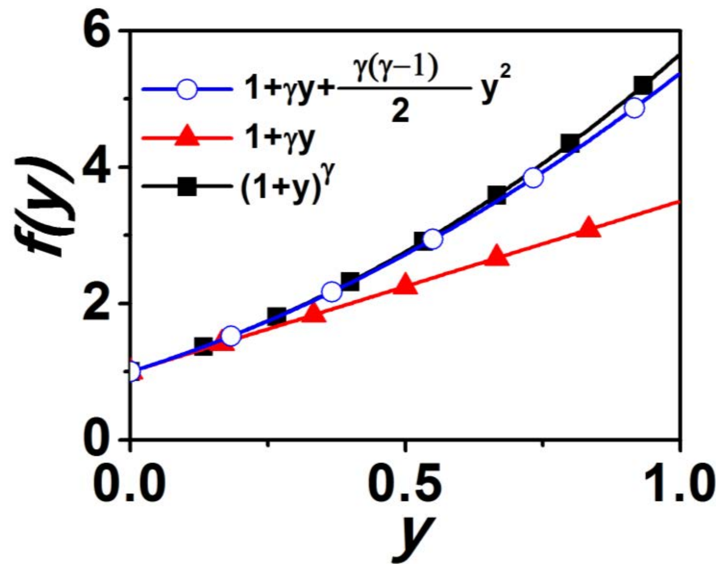

Figure 5-12. The binomial series approximation of $(a + y)^n$.

Therefore, for relatively small dissipated power, i.e. $\alpha_{SH}I_{ds}^{sat} \leq 1$ the function $\left(1 + \alpha_{SH}I_{ds,SH}^{sat}\right)^{\gamma}$ is relative well approximated by the three first terms of the series (figure 5-12) *eq.* (5-41) is then of the form:

$$\frac{\gamma(\gamma-1)}{2}\alpha_{SH}{}^{2}\left(I_{ds,SH}^{sat}\right)^{3} + \gamma\alpha_{SH}\left(I_{ds,SH}^{sat}\right)^{2} + (1+\Delta)I_{ds,SH}^{sat} - i_0 = 0 \tag{5-44}$$

I_{ds}^{sat} could then be solved as the root of the cubic equation. After some algebra, it is possible to arrive to the analytical expression:

$$I_{ds,SH}^{sat} = \frac{3i_0}{(1+\Delta) + I_4 + I_5} \tag{5-45}$$

$$where\ I_4 = \sqrt[3]{\frac{1}{2}\left(R + \sqrt{R^2 - 4Q^3}\right)} \qquad and \qquad I_5 = \sqrt[3]{\frac{1}{2}\left(R - \sqrt{R^2 - 4Q^3}\right)} \tag{5-46}$$

$$R = 2(1+\Delta)^3 + 3\gamma\alpha_{SH}i_0\left(3(1+\Delta) + \tfrac{9}{2}i_0\gamma(\gamma-1)\alpha_{SH}\right) \tag{5-47}$$

$$Q = (1+\Delta)^2 + 3\gamma\alpha_{SH}i_0 \tag{5-48}$$

5.3.2.7. EXPERIMENTAL SATURATION CURRENT AND TRANSCONDUCTANCE FITTING

The extrinsic g_m is simulated from the derivative of *eq.* (5-45), where an analytical close form for g_m can be computed. The physical layout parameters used in the simulations are $L_g = 4\ \mu m$, $W = 150\ \mu m$, $C_0 = 2.99 \times 10^{-7}\ Fcm^{-2}$, $L_{gs} = 4\ \mu m$ and $L_{gd} = 5\ \mu m$. The contact resistance is $R_c = 0.5\ \Omega mm$. The threshold voltage value of $V_{th} = -4.18\ V$ is described by $\Phi_B = 1.48\ eV$, $\Delta E_c = 0.39\ eV\ (x = 0.28)$ [65] and $P_T = 9.63 \times 10^{12} qcm^{-2}$, which results in $n_{s0} = 9.93 \times 10^{12} cm^{-2}$. The $2DEG$ channel mobility is described by $\delta = 0.28$ where the mobility constant is $4.21 \times 10^{11} cm^{2+\delta}T^{\gamma}/Vs$ $(\mu_0 = 1620\ cm^2\ V/s\ and\ T_0 = 300\ K)$. γ is determined from the fit to the experimental g_m to be $\gamma = 1.93$. The thermal resistance is also a fit parameter with a value of $R_{th} = 76.9\ K/W\ (k = 1.6\ W/cmK)$ at room temperature and $V_{ds} = 12\ V$. This R_{th} value agrees reasonably well with experimental/theoretical values previously reported.[73,74]

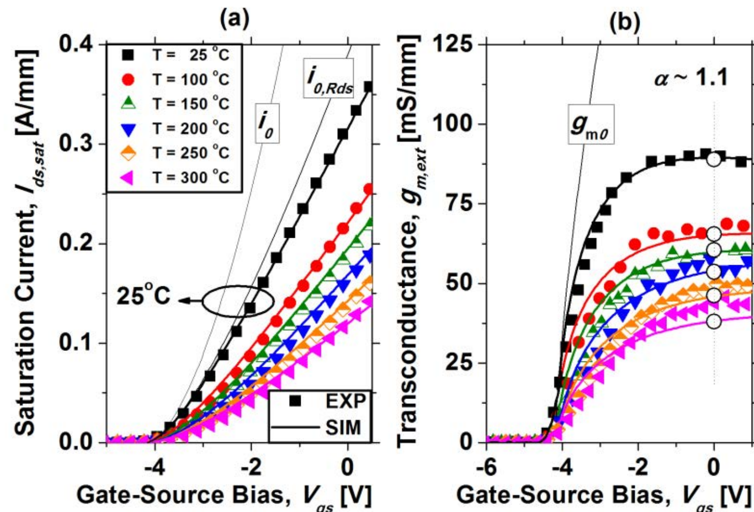

Figure 5-13. Simulated (solid lines) versus experimental (symbols) for (a) drain current and (b) transconductance in the temperature range of $25–300$ °C showing good agreement. The drain bias is $V_{ds} = 12\ V$ and g_{m0} is the simulated intrinsic transconductance.

As it can be inferred from figure 5-13, we have obtained a good fit for both, the saturation current and the transconductance in the temperature range of $25–300$ °C. The value of the g_m temperature exponent ($g_m \sim T^{-\alpha}$) given by the simulations is in agreement with the value experimentally extracted of $\alpha = 1.1$. The model has been further validated in a wider range of saturation voltages, in particular, for $V_{ds} = 6\ V$, $V_{ds} = 9\ V$ and $V_{ds} = 15\ V$.

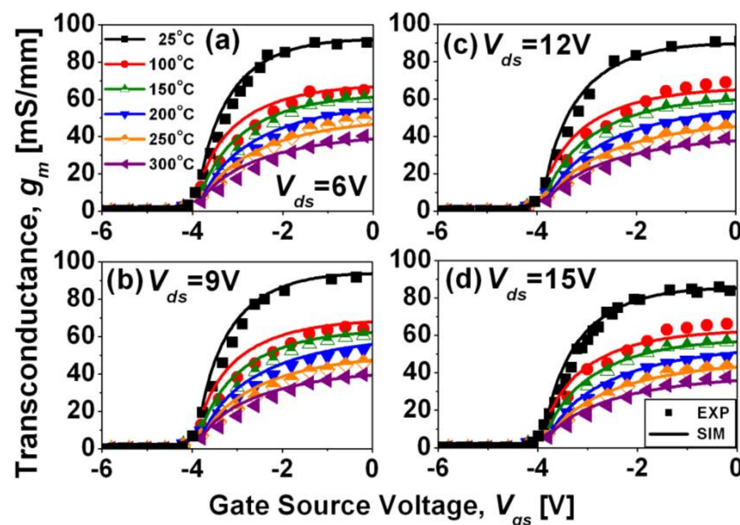

Figure 5-14. Simulated (solid lines) *vs* experimental (symbols) transconductance in the temperature range of $25–300$ °C for different saturation drain–source biases, $V_{ds} = 6\ V$ (a), $V_{ds} = 9\ V$ (b), $V_{ds} = 12\ V$ (c) and $V_{ds} = 15\ V$ (d). The g_m temperature coefficient is $\alpha = 1.1–1.2$ ($V_{gs} = 0\ V$) for all the saturation voltage range.

As it can be inferred from figure 5-14, the temperature dependence is virtually identical at varying V_{ds}, being the g_m temperature coefficient $\alpha = 1.1 - 1.2$ ($V_{gs} = 0\ V$) for all the saturation voltage range. Nevertheless, the electron mobility dependence on the temperature ($\mu_n \sim T^{-\gamma}$) was established to be $\gamma = 1.93$ (in accordance with the typical value from physical modeling of the optical phonons scattering mechanism). According to this model, the intrinsic transconductance g_{m0} at room temperature (without taking into account source–drain resistances and self-heating) can be as high as 375 mS/mm (four times larger than the experimental g_m value).

5.4. $HEMT$ vs $MIS - HEMT$ MODELING

5.4.1. ANALYTICAL TRANSCONDUCTANCE MODEL

The introduction of a gate insulator affects the operation of a simple Schottky gate $HEMT$. The parallel capacitance associated with the gate insulator capacitor and the $AlGaN$ buffer capacitor diminishes the effective gate capacitance of a $MIS - HEMT$. In this dissertation, the influence of this thin insulator on the $On - state$ electrical characteristics of a device is evaluated numerically. In particular, we have investigated the effect of using a thin insulator based on $SiO_2, Si_3N_4, Al_2O_3, and\ HfO_2$ on the saturation current and transconductance. To accomplish this objective, we have developed a very simple analytical set of closed-form expressions for the saturation current, based on physically modeling the electron mobility in a $HEMT$ channel described in the previous section. This simplified model is used to understand the effect of varying gate capacitance in an "ideal" $HEMT$ transistor. In the following section, the basic model is improved by including the effect of the extrinsic source and drain resistances. In the last section, we consider self-heating and briefly discuss its effect on the maximum transconductance. This is analyzed for several different substrates upon which GaN is currently grown, namely: SiC, Si and sapphire.

Presented in figure 5-15 is the cross-sectional view of our simplified reference $MIS - HEMT$. What we call here the "$AlGaN$ buffer" is really composed of a carefully engineered layer stack which is normally formed by a GaN cap on top of two or more $Al_xGa_{1-x}N$ layers with different $n - type$ doping or Al content (x). To make the model as simple as possible, this stack is effectively described by a gate $HEMT$ capacitance C_H of thickness d_H and permittivity $\varepsilon_{r,H}$.

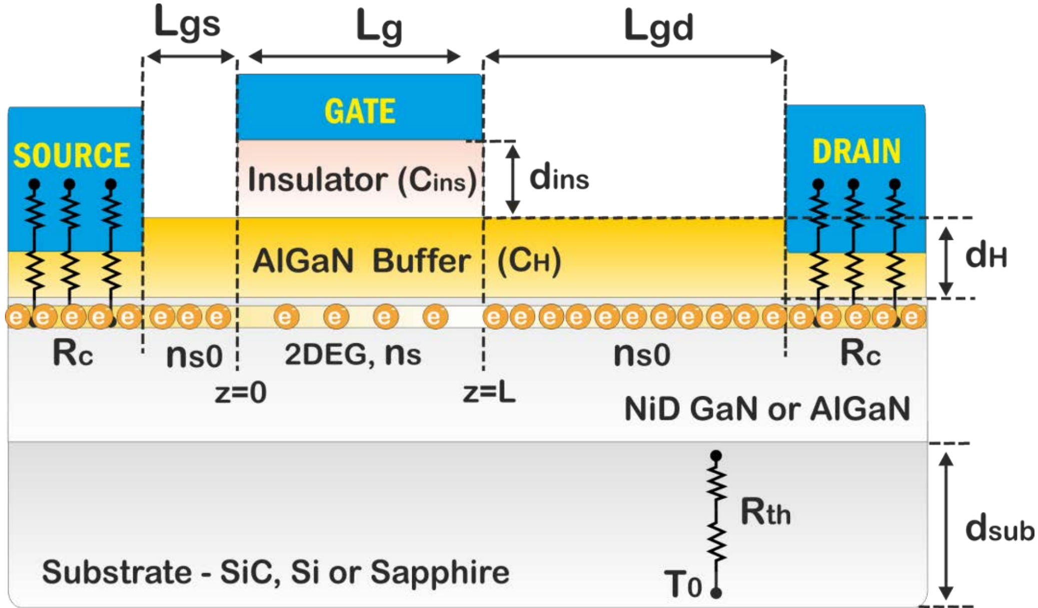

Figure 5-15. Cross-sectional view of the simulated $MIS - HEMT$. C_{ins} and d_{ins} are the insulator capacitance and thickness. C_H and d_H are the $AlGaN$ *buffer* capacitance and thickness. R_c is the contact resistance, n_s is the $2DEG$ sheet carrier concentration, R_{th} is the thermal resistance and T_0 is the bulk temperature (at the bottom). L_g, L_{gs} and L_{gd} are the gate length, the gate-source and gate-drain spacing, respectively.

Donor-like levels from the surface of the $AlGaN$ buffer surface, together with a strong polarization field are believed to be the source of the electrons in the $2DEG$ channel, which is roughly described by a total polarization charge parameter, P_T. It is worth mentioning that there are detailed models for both C_H and P_T to take into account the complex structure of the GaN buffer.[54] However, this high-degree of accuracy in the description of the $HEMT$ capacitance and polarization fields, only results in very small deviations compared to what is obtained taking into account an effective $AlGaN$ buffer.[54] As stressed before, the introduction of the gate insulator affects the Schottky gate capacitance of the $HEMT$. The $MIS - HEMT$ gate capacitance (C_b) is now the parallel sum of the contribution of C_H and the gate oxide (C_{ins}):

$$\frac{1}{C_b} = \frac{1}{C_H} + \frac{1}{C_{ins}} \qquad (5\text{-}49)$$

Where $C_H = \varepsilon_{r,H}/d_H$ and $C_{ins} = \varepsilon_{r,ins}/d_{ins}$. $\varepsilon_{r,H}, \varepsilon_{r,ins}$, d_H and d_{ins} are the dielectric constants and thicknesses of the $AlGaN$ buffer layer and the insulator, respectively. The dielectric constants used in the simulations are $3.9, 7.4, 10\ and\ 20$ for $SiO_2, Si_3N_4, Al_2O_3, and\ HfO_2$, respectively.[61] This simple gate capacitance

approximation can be naturally improved to take into account the different discontinuities present in the structure. For example, considering the different band discontinuities, the gate capacitance is the sum of several contributions:

$$C_H^{-1} = C_{cap}^{-1} + C_{barrier}^{-1} + C_{spacing}^{-1} + C_{\Delta d}^{-1} \quad (5\text{-}50)$$

including the GaN cap, the $AlGaN$ barrier, the AlN spacer layer and the contribution of the distance of the electron gas from the spacer layer $C_{\Delta d}$. Each of these contributions is of the form $C_i = \varepsilon_i/d_i$. The dielectric constant ε_i for the GaN and $Al_xGa_{1-x}N$ can be determined from the approximation $\varepsilon_i(x) = -0.5x + 9.5$.[65] The model presented in this investigation is assumed to be valid at room and elevated temperatures, (where mobility may be well approximated by the phonon scattering) and for long channel $HEMTs$ which make the degradation of the quantum capacitance and/or fringing capacitance negligible in a first approximation.[75,76]

5.4.2. $MIS-HEMT$ MODELING

The set of equations, presented in section 5.3, form an analytical closed-form method to numerically evaluate the effect of a thin gate oxide on the electrical properties of the $MIS-HEMT$. In the following sections we will investigate the effect of the insulator on the threshold voltage, the saturation current and the transconductance. The parameters used in the simulations are listed in table 5-1.

The simulated large channel $HEMT$[77] has a conventional layout of $4/5/4\ \mu m$ for $L_{gs}/L_{gd}/L_g$ respectively. Insulator thickness is varied in the range of $0-20\ nm$ for SiO_2, Si_3N_4, Al_2O_3 and HfO_2.

We have simplified the $AlGaN$ buffer structure to the point to make this a single layer (the simplest general case). The gate capacitance (C_b) may be established experimentally, from the $C-V$ measurement (gate-drain) of the device.[12] If an effective dielectric constant of $\varepsilon_{r,H}(x) = 9.36\ (x = 0.28)$ is assumed, the equivalent buffer thickness would be $d_H = 26\ nm$ $\left(C_b = \varepsilon_{r,H}/d_H\right)$.

Parameter	Value	Units
Intrinsic		
L_g	4	μm
W	150	μm
$C_H = \varepsilon_{r,H}/d_H$	3.75×10^{-7}	F/cm^2
C	3.68×10^{11}	$cm^{2+\gamma}T^{\gamma}/Vs$
δ	0.28	
γ	1.93	
Φ_B	1.48	eV
ΔE_c	0.39^a	eV
P_T	9.63×10^{12}	qcm^{-2}
k_1	-0.0802^b	V
k_2	$1.04 \times 10^{7\,b}$	Vcm
k_3	$1.05 \times 10^{14\,b}$	Vcm^2
Extrinsic		
n_{s0}	9.93×10^{12}	cm^{-2}
R_c	0.5	Ωmm
L_{gs}	4.0	μm
L_{gd}	5.0	μm

Table 5-1. Parameters [a] and [b] for the simulation of the $MIS-HEMT$ from the literature.[65,54]

5.4.2.1. THRESHOLD VOLTAGE

The basic $HEMT$ design nowadays is $normally-on$ (although techniques do exist to make it $normally-off$).[78] A $normally-on$ device is the type considered in our simulations. This means that one must apply a negative bias of a few volts to the gate in order to deplete the $2DEG$ channel of confined electrons and to suppress the passage of current in the channel flowing from source to drain. Therefore, the threshold voltage is strongly dependent on the gate capacitance. As it can be seen in figure 5-16 (a), the lower the gate capacitance, the more negative the threshold voltage is. This is a relevant implication of the use of insulator layers in the gate of the $HEMT$.

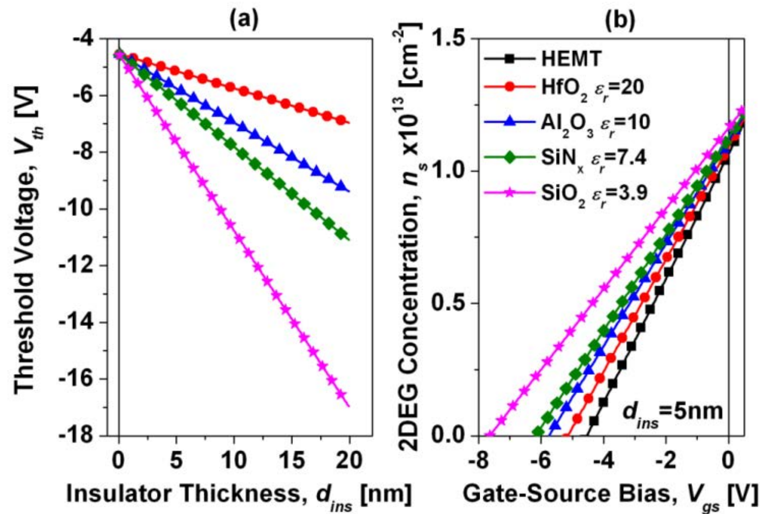

Figure 5-16. (a) Simulated threshold voltage *vs* insulator thickness and (b) $2DEG$ concentration for a Schottky gate $HEMT$ (labeled $HEMT$) and MIS-HEMT with SiO_2, Si_3N_4, Al_2O_3 and HfO_2 as the gate insulator.

Increasingly negative threshold voltages mean a higher amount of power consumed during the on/off state transition. The way to increase the gate capacitance while maintaining a fixed insulator thickness (to prevent Schottky gate leakage) is to change the dielectric to one with a higher dielectric constant. This is one of the reasons why engineers often prefer to use other dielectrics, with higher dielectric constant that SiO_2, for the $MIS - HEMT$ structure. Si_3N_4 is popular because it matches well with $GaN - based$ materials, both being nitride based.[79] However, in the case of Al_2O_3, the dielectric constant is still relatively low.

Recently, there is a strong interest in HfO_2 based MIS structures which exhibit a remarkably high ε_r of 20. In fact, a very thin layer of any insulator, typically around 5 nm, has been demonstrated to effectively reduce the leakage current through the gate for negative gate bias.[11] Nevertheless, there is a trade-off between the dielectric constant and the insulator's critical electric field. For example, the critical electric field for SiO_2 is around 10 MV/cm while for HfO_2 is typically $2 - 3$ MV/cm.[80] This is a detrimental factor for the use of HfO_2 if positive gate voltages are desired. In contrast to what happens with Si or SiC technology, unfortunately, the quality of the thermal oxide of GaN is incomparable with the successful SiO_2 thermal oxide, making its application generally considered as commercially impractical.

For a given gate bias, the sheet carrier concentration (figure 5-16 (b)) also depends on the thin insulator properties, especially for the smaller $V_{gs}-V_{th}$. In fact, the slope of the sheet concentration may be approximated as:

$$\partial n_s/\partial V_{gs}=q^{-1}C_b \tag{5-51}$$

In other words, the steepest slope is obtained for the thinner/$high-k$ insulators. However, in the vicinity of $V_{gs}=0\ V$, n_s is approximately the same for any $HEMT$ or $MIS-HEMT$ since, in general,

$$q^{-1}C_b(\Phi_B-\Delta E_c)\ll P_T \tag{5-52}$$

Here, we have assumed that the total polarization charge remains basically unaffected by the insulator deposition.[12] This assumption has been made to keep the model as simple as possible and it agrees with some previously reported works.[12,19,81] However, in general, it may be observed that a relatively small increase or decrease ($\sim 1-10\%$) of the $2DEG$ carrier concentration occurs due to the action of the passivation of surface charges, thereby affecting somehow the $AlGaN$ polarization charge.[82,83] The variety of gate insulators and deposition techniques has resulted in a strong dispersion of the available data in the literature.[19,56,81-87] In this sense, it is worth mentioning that some authors have reported more relevant differences in n_s and μ_n when comparing Schottky and MIS gate $HEMTs$.[84,85] On top of that, the introduction of the MIS layer may subtly also affect other device parameters such as the contact resistance. For example, if it is not completely and homogeneously removed from the source/drain area, an ultra-thin layer could act as an additional barrier thus increasing the R_{on}. As the wafer scale maps are uncommon in the literature,[86,87] the differences obtained for a small population of devices could easily bring inconclusive statements. Furthermore, insulator deposition techniques have inherently some drift in their dielectric constant and/or thickness. On the other hand, the $2DEG$ is separated from the MIS interface by the $AlGaN$ buffer which would make it inherently less sensitive to any surface charge variation. In general, the electron mobility differences between *identical* $HEMT$ and $MIS-HEMTs$ are reported to be even smaller than for n_s.[19,81] Donoval *et al.*[56] have reported the same temperature dependence for $I_{ds,sat}$ and g_m $HEMT$ and $MIS-HEMT$ as $T^{-1.5}$, suggesting that phonon scattering is the predominant effect, regardless of the gate stack architecture. The hypothesis of the electron mobility conservation seems plausible.

In contrast to what happens with other $GaN-based$ transistors such as $MESFETs$ or metal oxide semiconductor field effect transistor ($MOSFETs$), the threshold voltage for a $HEMT$ with a Schottky gate is remarkably stable with the temperature (up to, at least, 300 °C).[88] This is due to the fact that the polarization field has a very weak dependence on the temperature and hence, n_s is also a weak function of the temperature. It must be mentioned that, in many practical situations, there is a number of interface $(Q_{it,MIS})$ and/or bulk traps (Q_{ins}) created during insulator deposition.[89] This would provoke a shift of the threshold voltage towards more negative or more positive values (depending on the nature of these traps, acceptors or donor, positive or negative ions, etc.). This added charge could be taken into account with an additional term in eq.(5-13):

$$V_{th,MIS} = V_{th} - C_{ins}^{-1}(Q_{ins} + Q_{it,MIS}) \quad (5\text{-}53)$$

These traps could also be much more sensitive to any temperature change.[90] On GaN $MOSFET$ devices, the D_{it} has a major affect on the on-state current of the device, as Coulomb scattering greatly reduces the field-effect mobility.[89] Within the MIS structure of GaN $HEMTs$, the presence of a large amount of interface traps have been extensively demonstrated.[19,82] However, these traps do not greatly affect the $HEMT$ mobility as the $2DEG$ charge centroid is separated from the MIS interface by the $AlGaN$ buffer and the AlN spacer.[58] The MIS interfacial traps impact the $On-state$ of a $HEMT$ primarily inducing a trap threshold shift, while the subthreshold slope is likely also to be degraded.[28] In the first instance, this is easily accounted for in the model by adding a new term into eq.(5-13). However, significant amount of work must still be performed to understand the D_{it} profile within the hetero-structure bandgap, how these traps would interact with channel electrons, the different chemical nature of these traps (which are currently viewed as slow and fast traps)[30] or the implication in the long term reliability of the device.

5.4.2.2. DRAIN AND SATURATION CURRENT

The R_{on} value is a fundamental parameter of any power device. Together with the reverse bias breakdown voltage, the $V_B^2/R_{on,sp}$ ratio is considered the power device figure of merit. $AlGaN/GaN$ $HEMTs$ have been reported with $V_B^2/R_{on,sp}$ as high as $1.2 \times 10^9\ V^2\Omega^{-1}cm^{-2}$.[11,91]

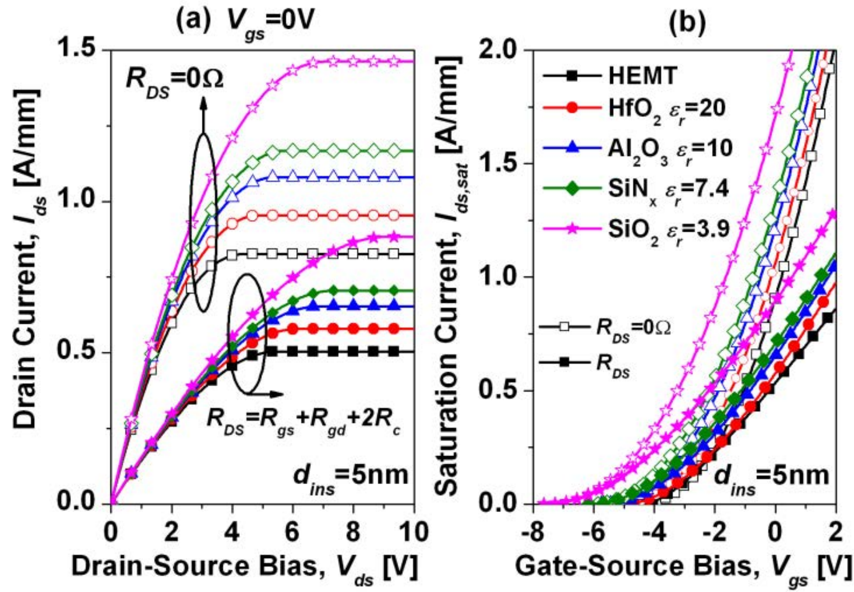

Figure 5-17. (a) Simulated drain current $(I_{ds} - V_{ds})$ for $V_{gs} = 0\ V$ and (b) saturation drain current $(I_{ds} - V_{gs})$ for a Schottky gate $HEMT$ (labeled $HEMT$) and $MIS - HEMT$ with SiO_2, Si_3N_4, Al_2O_3 and HfO_2 as the gate insulator. Note that the ideal saturation current $I_{ds,sat}$ and $I_{ds,sat,R}$ do not depend on V_{ds}.

In the case of the $normally - on\ HEMTs$ this is usually measured at zero or small positive gate bias. The simulated drain current for $V_{gs} = 0\ V$ is presented in figure 5-17 (a) for different $MIS - HEMTs$ with 5 nm of gate insulator. As mentioned before, the n_s value for $V_{gs} = 0\ V$ is similar regardless the MIS properties:

$$n_s = n_{s0} \simeq q^{-1} P_T \quad (5\text{-}54)$$

This results in similar on-resistance ($R_{on}^{-1} = \partial I_{ds}/\partial V_{ds}$) characteristics in the linear range. Therefore, for ideal $HEMTs$, simulations suggest that the introduction of an insulator has a weak effect on the R_{on} value when it is estimated at $V_{gs} = 0\ V$. The DC saturation current is also a key parameter in establishing the maximum RF power output for $HEMT$ devices. This current increases with increasingly positive gate voltages, until it saturates with a maximum value. However, for Schottky gate $HEMTs$, a gate voltage in excess of $+1\ V$ results in excessive gate leakage current, consequently increasing the noise factor significantly. The introduction of the MIS insulation would enable the use of higher positive gate voltage. Furthermore, for zero or small positive V_{gs}, the introduction of the thin insulator increases the saturation current by a factor of approximately C_b/C_H. Therefore, there is a significant difference in the saturation current value depending on the type of insulator (for a given insulator thickness) used in

the MIS gate stack, as can be seen in figure 5-17 (b). Analogously, the saturation voltage also increases, being, to first approximation, a value close to $-V_{th}$. The introduction of the source and drain series resistance in the computation of I_{ds} and $I_{ds,sat}$ significantly reduces the $HEMT$ drain current but the previous arguments are still totally valid, as it can be inferred from figure 5-17.

5.4.2.3. TRANSCONDUCTANCE

The gate transconductance (g_m) of the transistor is one of the most important indicators of the device quality for microwave application, critically affecting the cut-off frequency and the maximum frequency of the device. Besides, g_m is used in the small-signal model of the $HEMT$. Therefore, it is one of the most used figures of merit of this kind of transistors, usually expressed in mS/mm. Conversely to what happens with the saturation current, the intrinsic saturation gate transconductance converges (figure 5-18 (a)), regardless the gate insulator, to a fixed value of $\sim qW\mu_n(2-\delta)P_T/2L_g$ for $V_{gs}=0\,V$ and small ($+1\,V/+2\,V$) positive gate bias. Therefore, as happens with the on-resistance, the intrinsic saturation transconductance, for $V_{gs}\sim 0\,V$, should not depend on the insulator. The introduction of the source-drain series resistance greatly affects the value of the extrinsic transconductance as shown in figure 5-18 (b), reducing its value to the more common values of 120 mS/mm for $L_{ds}=14\,\mu m$.[13]

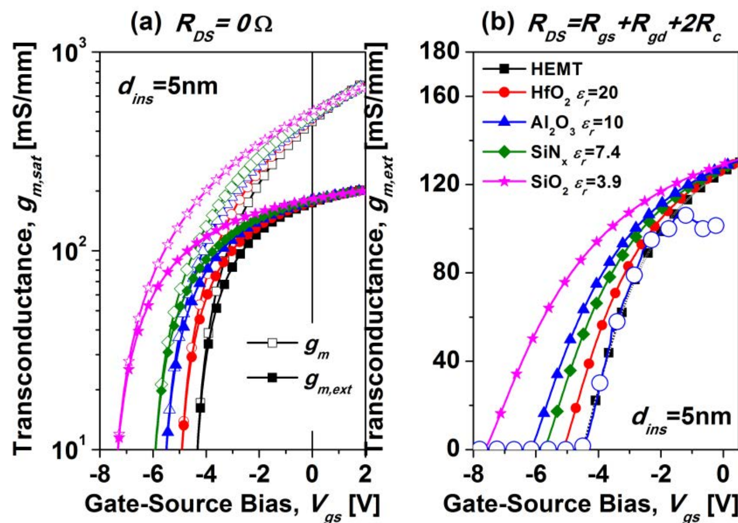

Figure 5-18. (a) Simulated intrinsic and extrinsic transconductance vs V_{gs} for $R_{DS}=0\,\Omega$ and (b) extrinsic transconductance vs V_{gs} taking into account drain-source series resistance for a Schottky gate $HEMT$ (labeled $HEMT$) and $MIS-HEMT$ with SiO_2, Si_3N_4, Al_2O_3 and HfO_2 as gate insulator. Note that the ideal saturation transconductance $g_{m,sat}$ and $g_{m,sat,R}$ do not depend on V_{ds}. Empty circles denoted experimental $HEMT$ data.[77]

Nevertheless, even introducing a potential source-drain series resistance, the previous set of equations is not able to reproduce the typical behavior of the maximum transconductance.[11,13,15] The transconductance curve, especially when measured at room temperature, exhibits a $g_{m,max}$ that usually takes place for few voltages from the threshold voltage $\left(V_{gs} - V_{th} \sim 2 - 3\ V\right)$. Then, $g_{m,ext}$ diminishes for greater gate bias. Therefore, we suggest that in order to explore the dependence of the transconductance on the gate insulator, this should be measured for small $V_{gs} - V_{th}$ where, experimentally, the maximum transconductance value is achieved. In this sense, figure 5-19 (b) shows the value of the transconductance for $V_{gs} - V_{th} = 2\ V$ for $SiO_2, Si_3N_4, Al_2O_3, and\ HfO_2$. As can be inferred from the figure, $g_{m,ext}$ diminishes as the insulator thickness increases (figure 5-20), when it is considered a fixed $V_{gs} - V_{th}$. Besides, the greater the dielectric constant, the greater $g_{m,ext}$ is. This is a result which fits well with the commonly reported behavior, when “identical” $HEMT$ and $MIS - HEMT$ devices are compared, i.e., the gate insulator is detrimental for RF applications. Effectively, the fit to the experimental data is good for relatively small $V_{gs} - V_{th}$ (open circles of figure 5-18 (b) are from the experimental data).[77]

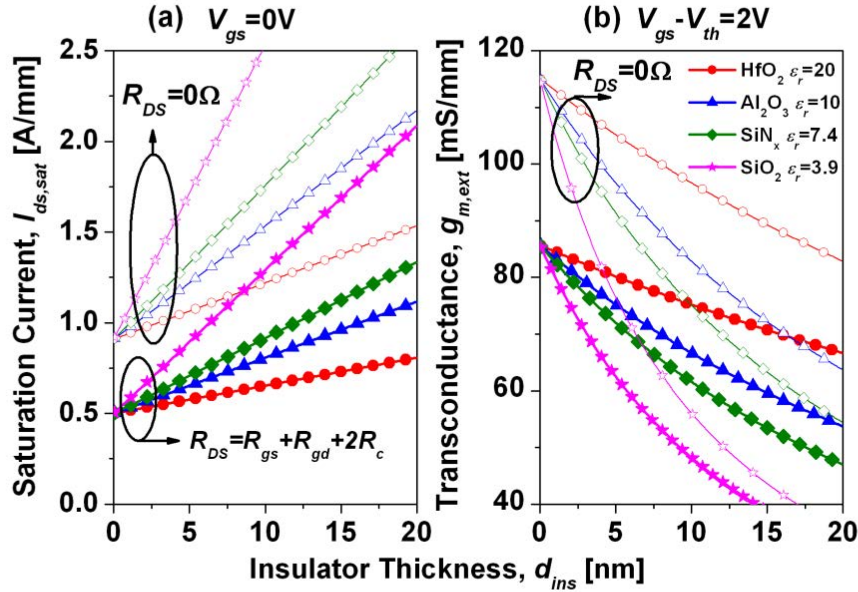

Figure 5-19. (a) Simulated saturation current (with and w/o drain-source series resistance) *vs* insulator thickness for $V_{gs} = 0\ V$ and (b) Simulated extrinsic transconductance *vs* insulator thickness (with and w/o drain-source series resistance) at $V_{gs} - V_{th} = 2\ V$ for a $MIS - HEMT$ with $SiO_2, Si_3N_4, Al_2O_3\ and\ HfO_2$ as gate insulator.

However, the introduction of series resistance is still unable to explain the maximum transconductance experimentally observed (the g_m *vs* V_{gs} curve usually has a parabolic-

like curve with a maximum). We propose that other relevant sources of power dissipation must be taken into account: i.e. self-heating.

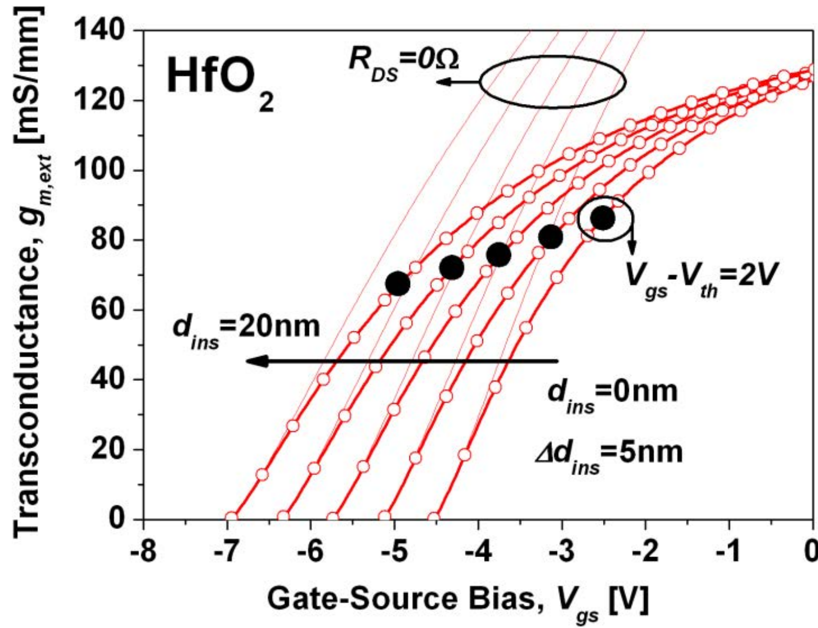

Figure 5-20. HfO_2 $MIS-HEMT$ simulated intrinsic ($R_{DS} = 0\ \Omega$) and extrinsic transconductance for different gate insulator thicknesses displaying the decrease of the $g_{m,ext}$ vs insulator thickness for a given $V_{gs} - V_{th}$. The transconductance is simulated for an HfO_2 thickness (d_{ins}) in the range of $0 - 20\ nm$ with an interval of $\Delta d_{ins} = 5\ nm$.

5.4.3. SELF-HEATING

As described in 5.3.2.6, figure 5-21 (a) shows the simulated effect of the self-heating in the saturation current. $d_{sub} = 350\ \mu m$ is typical for a SiC substrate. The transconductance from the derivate of $I_{ds,sat,SH}$ is presented in figure 5-21 (b). It can be seen that a maximum transconductance value can be obtained (for a given gate bias of few volts after the threshold) which replicate the experimental results much better. Figure 5-21 (b) shows the simulated external transconductance for a $HEMT$ (dots) and a HfO_2 $MIS-HEMT$ (solid lines) with gate oxide thicknesses of 5 and 20 nm. Due to self-heating, the maximum transconductance diminishes with the insulator thickness, in agreement with the general observation. There is a strong influence from the substrate ($SiC, Si\ or\ sapphire$) on both the saturation current and the extrinsic transconductance.

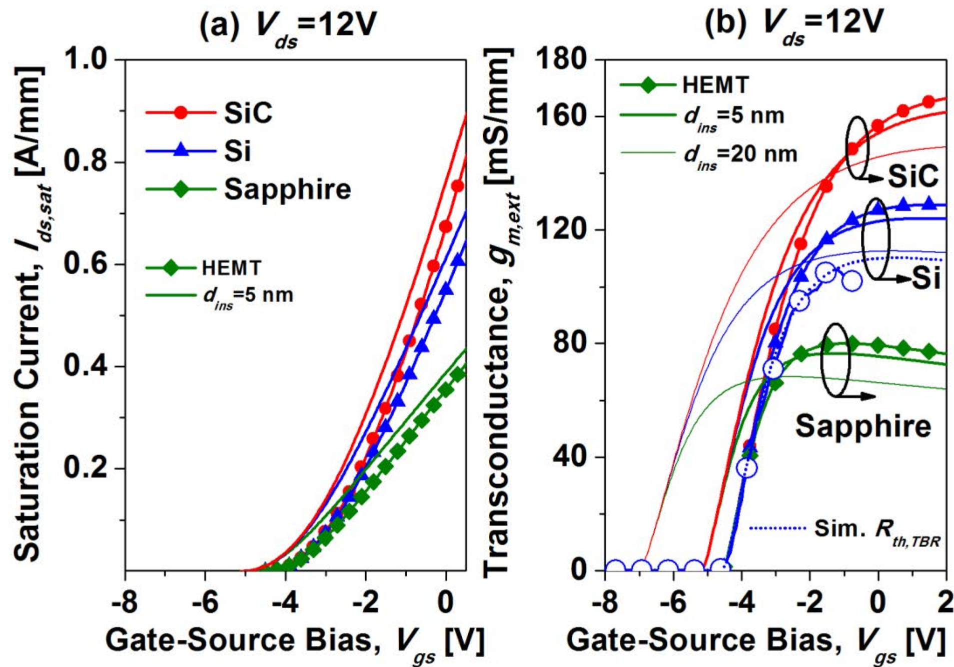

Figure 5-21. (a) Simulated (with self-heating) saturation current for a Schottky gate $HEMT$ and a $MIS - HEMT$ ($5\ nm\ HfO_2$). (b) Extrinsic transconductance vs V_{gs} taking into account the self-heating for a Schottky gate $HEMT$ and $MIS - HEMTs$ ($5\ nm\ and\ 20\ nm$ of HfO_2). Note that $g_{m,sat,SH}$ depends on V_{ds}. Empty circles denoted experimental $HEMT$ data.[77] The simulated fit to the experimental data (dashed blue line in the on-line version) takes into account the additional thermal boundary resistances, $R_{th,TBR}$. Simulated $d_{ins} = 5\ nm$ and $d_{ins} = 20\ nm$ solid lines are computed without taking into account the thermal boundary resistance (TBR), directly using $eq.$(5-39) and $eq.$(5-40) and a fixed $d_{sub} = 350\ \mu m$.

As one would expect, the higher the thermal conductivity, the higher the maximum transconductance is. Therefore, the model suggests that self-heating has a relevant role in reducing the g_m value. For a given MIS/GaN active layer structure, effectively, the different substrate thermal conductivity would be the main factor which establishes the channel temperature (as a function of R_{th}which depends in turn on $kappa$). It is worth mentioning that, in practice, the heat flow in the hetero-structure is more complex because between the substrate and the GaN active layers there are in general a number of interfacial layers which result in additional thermal boundary resistances.[73,92] Recently, bulk GaN thermal conductivities larger than 2.6 W/cmK have been reported[93] (the theoretical value for GaN bulk $kappa$ would be as high as 4.1 W/cmK),[94] which suggests that $FS - GaN$ is an interesting alternative to the excellent SiC substrates. Furthermore, the additional resistance associated with thermal boundary impedance may be naturally mitigated. Indeed, the temperature impact of the $On - state$ characteristics

of a $HEMT$ on $FS-GaN$ seems to be significantly better when compared with Si or $sapphire$ due to the lower thermal impedance of the substrate.[95] For a given substrate conductivity, the channel temperature would be given by the dissipated power:

$$P_d = I_{d,sat}V_{ds} \quad and \quad T_{eff} = R_{th}I_{d,sat}V_{ds} + T_{sub} \qquad (5\text{-}55)$$

This effective temperature increase significantly degrades the electron mobility (promoted by phonon scattering). For a given saturation drain voltage, (in our case, simulations in figure 5-21 have been carried out at $V_{ds} = 12\,V$), the saturation drain current increases as the gate capacitance decreases, as suggested by $eq.$ (5-21) and implicitly in $eq.$(5-45). The gate capacitance significantly decreases with insulator thickness, which in turns affects the value of the transconductance peak. This is the reason why, according to this model, the g_m peak value differs so much between $d_{ins} = 5\,nm\ and\ d_{ins} = 20\,nm$.

Also presented is the simulation/experimental fitting data from section 5.3.1.[77] It have included this experimental curve to benchmark the reference Schottky $HEMT\,g_m$, assuming the conservation of the electron mobility and the polarization fields when it is moved to a $MIS-HEMT$ approach. From this fit, it can theorize as to what the effect would be of varying the gate insulator and the substrate. The accuracy of the most simplified approach may be questionable in some cases, (we have discussed briefly before the $n_{s,0}$ variation due to the passivation of surface states reported by several authors), but it still could bring a qualitative insight into the effect of different insulators on the $On-state$ of the $HEMT$. As also stressed before, the accuracy of the method can be easily improved introducing a few experimental correction factors in $eq.$ (5-10) and $eq.$ (5-13) once it is know if there is a variation ($HEMT\ vs\ MIS-HEMT$) in the $n_{s,0}$ and/or μ_0. We have used the simplified R_{th} equations given in reference[68] for theoretically computing the effect of the self-heating for a given substrate thickness. For Si, the fit does not match directly the experimental values since the R_{th} does not take into account the additional thermal boundary resistance. We may use again a correction factor of $R_{th,TBR} = a_3 \times R_{th}$, a_3 being 1.4. For our reference $HEMT$, the Si/GaN nucleation layers were formed by $40\ nm$ of AlN, $250\ nm$ of GaN and $250\ nm$ of AlN grown at 920 °C. These nucleation layers are used to overcome the formation of cracks, which are due to the large difference in the thermal expansion coefficient between GaN and Si. Then, a 1.7 μm GaN (0001) buffer layer was grown at 800 °C, followed by the active layers. This correction factor value would be again sample dependent.

5.5. $HEMT\ vs\ MIS - HEMT$ EXPERIMENTAL

In this thesis three gate architectures have been investigated (figure 5-22). The basic $HEMT$ has been described in the previous chapters. A modification of the basic $HEMT$ consists in introducing a thin dielectric between the gate-source and the gate-drain pads. This device is known as passivated $HEMT$ or $i - HEMT$.

A way to further reduce the gate leakage current is the introduction of a thin dielectric between the gate metal and the GaN surface in an approach known as metal insulated gate ($MIS - HEMT$). The effect of introducing (or not) this dielectric has been theoretically studied by physical-based modeling in section 5.3 and 5.4. This sections present the experimental results from a different set of $HEMT$, $i - HEMT$ and $MIS - HEMT$ devices.

Although partially passivated, the core of a $i - HEMT$ device is in practice a converted Schottky gate device. Figure 5-23 (a) and (b) shown the transfer curves characteristic of a $HEMT\ vs\ MIS - HEMT$ with $45\ nm\ Si_3N_4$ gate oxide and for the Schottky gate $i - HEMT$ with gate leakage current of $\sim 1\ \mu A/mm$ $(W = 150\ \mu m)$ .The $MIS - HEMT$ gate current was effectively reduced one order of magnitude.

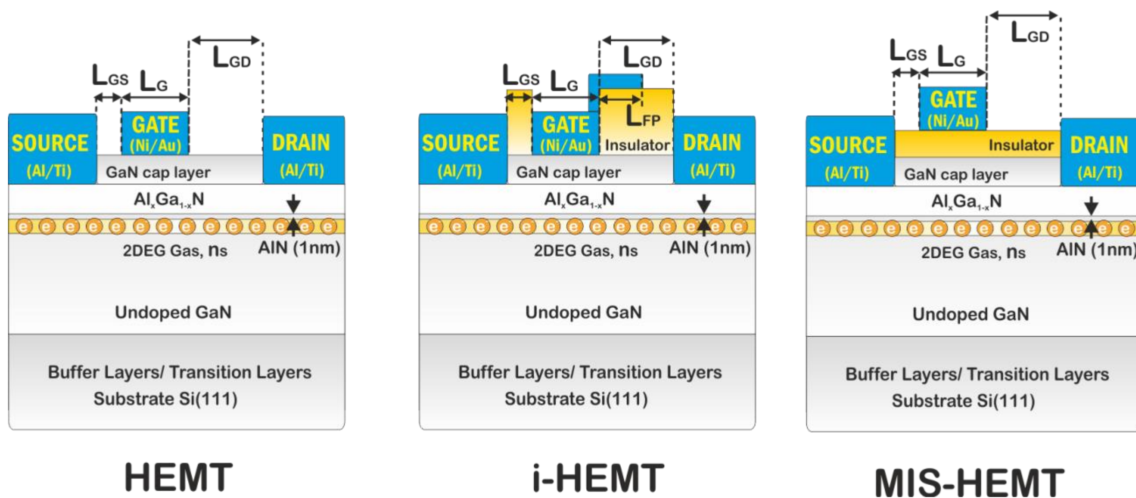

Figure 5-22. Attending to the gate engineering, three different type of devices had been fabricated $HEMT, i - HEMT$ and $MIS - HEMT$.

As pointed out in the previous section, HfO_2 has recently been demonstrated as a very promising gate dielectric candidate and passivation for $GaN - based$ high-power RF and high-voltage switches. Transistors with HfO_2 gate insulator have already exhibited minimal current slump, low R_{on}, high-breakdown voltage, and ultra-low leakage

currents.[9,19,20,21] In the frame work of the ON semiconductor project, it had been analyzed the effect of introducing a thin HfO_2 gate dielectric on the electrical performance of the $HEMT$ at the wafer scale. For gate engineering, two different types of $HEMT$, $A04$ and $A03b$, have been fabricated as commented in the fabrication process section. Both a Schottky gate Si_3N_4 passivated $i-HEMT$ and a thin HfO_2 based $MIS-HEMT$ were fabricated on two different 4 $inch$ state-of-the-art commercial $AlGaN/GaN-on-Si$ wafers. It is well-known that HfO_2 has many desirable properties, such as a relatively large bandgap (5.65 eV) or a $high-k$ dielectric constant (~20) which make this gate insulator very effective in realizing $HEMT$ devices with a large transconductance while keeping the gate leakage current low.[9] As shown in figure 5-23, the introduction of the thin HfO_2 based MIS approach results in a remarkably small V_{th} shift (see figure 5-16 and figure 5-24) and transconductance reduction, but in an improved gate stability under positive gate bias stress. In addition, no hysteresis is observed after subsequent $I-V$ stress test at RT (figure 5-25).

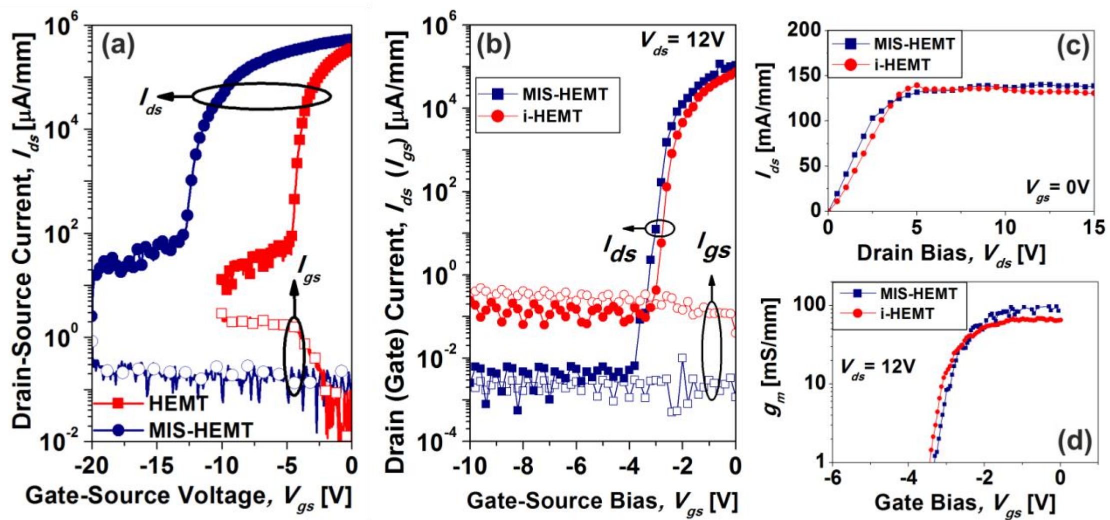

Figure 5-23. (a) $HEMT\ vs\ MIS-HEMT$ gate dielectric comparison with Si_3N_4 gate oxide (45 nm). $HEMT\ vs\ i-HEMT$ with ultra thin gate dielectric HfO_2 (few nanometers). Typical (b) $i-HEMT\ vs\ MIS-HEMT$ transfer curves $I_{ds}, I_{gs}\ vs\ V_{gs}$ showing the reduced $MIS-HEMT$ gate current. (c) $I-V$ forward curve and (d) g_m comparison extracted from the derivative of the transconductance curve.

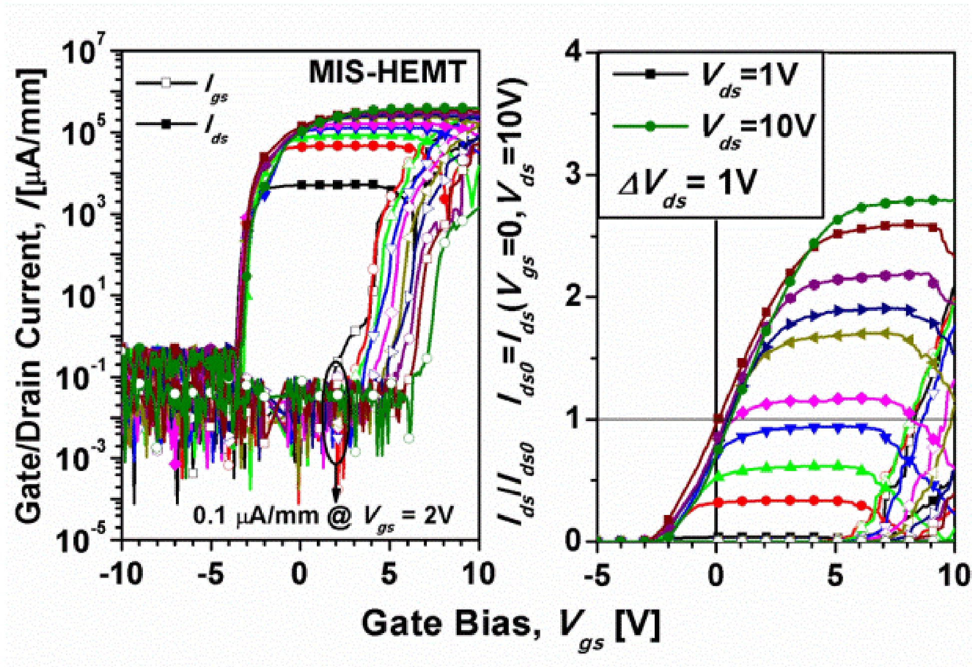

Figure 5-24. Saturation drain and gate current for pinch-off/positive gate bias. The $MIS - HEMT$ gate architecture allows extending the positive gate bias range before relevant gate current injection. At $V_{gs} = 1\ V$ and $2\ V$, the on-state current is 30% and 60% higher compared to $V_{gs} = 0\ V$, respectively.

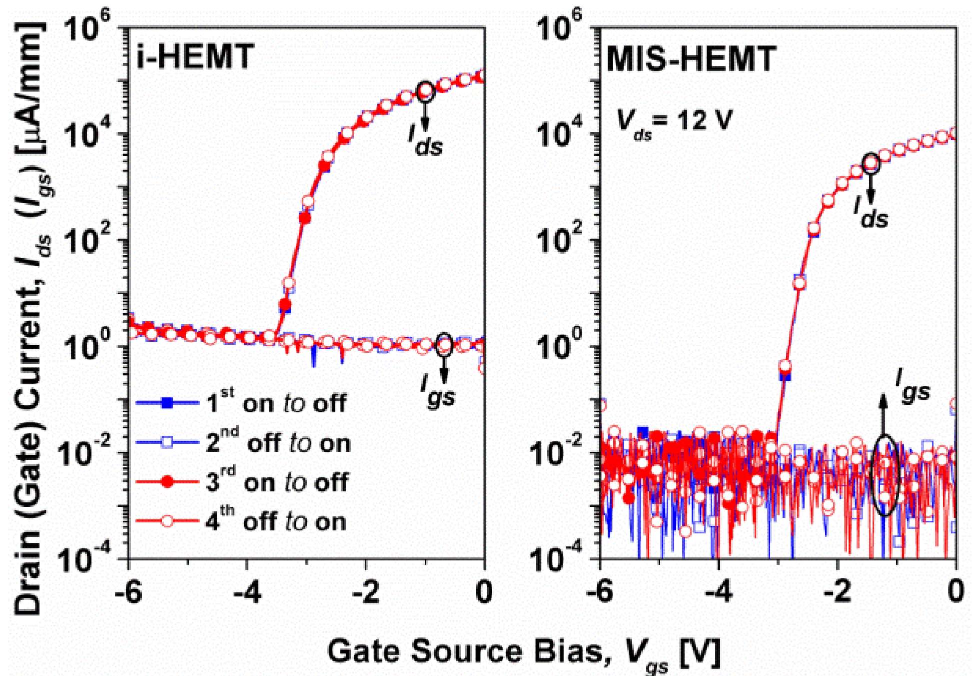

Figure 5-25. $i - HEMT$ and $MIS - HEMT$ $I_{ds} - V_{gs}$ after subsequent transconductance stress on/off showing no hysteresis. Note the very low gate leakage current for the HfO_2 $MIS - HEMT$.

When full-wafer maps are carried out (figure 5-26) this threshold shift can be quantified as small as $\Delta V_{th} = 0.3\,V$. The average V_{th} obtained for the sensible population of devices was $V_{th} = -2.7 \pm 0.3\,V$ and $V_{th} = -3.0 \pm 0.3\,V$ for the $i - HEMT$ and $MIS - HEMT$, respectively.

However at the lower gate bias, the $i - HEMT$ leakage was significantly higher than the one from the $MIS - HEMT$. To explore the origin of the leakage at the low bias we have used two terminal wafer maps up to $100\,V$. The gate–drain two terminal reverse current is presented in figure 5-27. The gate pad is negatively biased and drain was grounded. The $I - V$ tests are then recorded for the 4 $inch$ wafer and the value of the current at $100\,V$ is recorded in the plots.

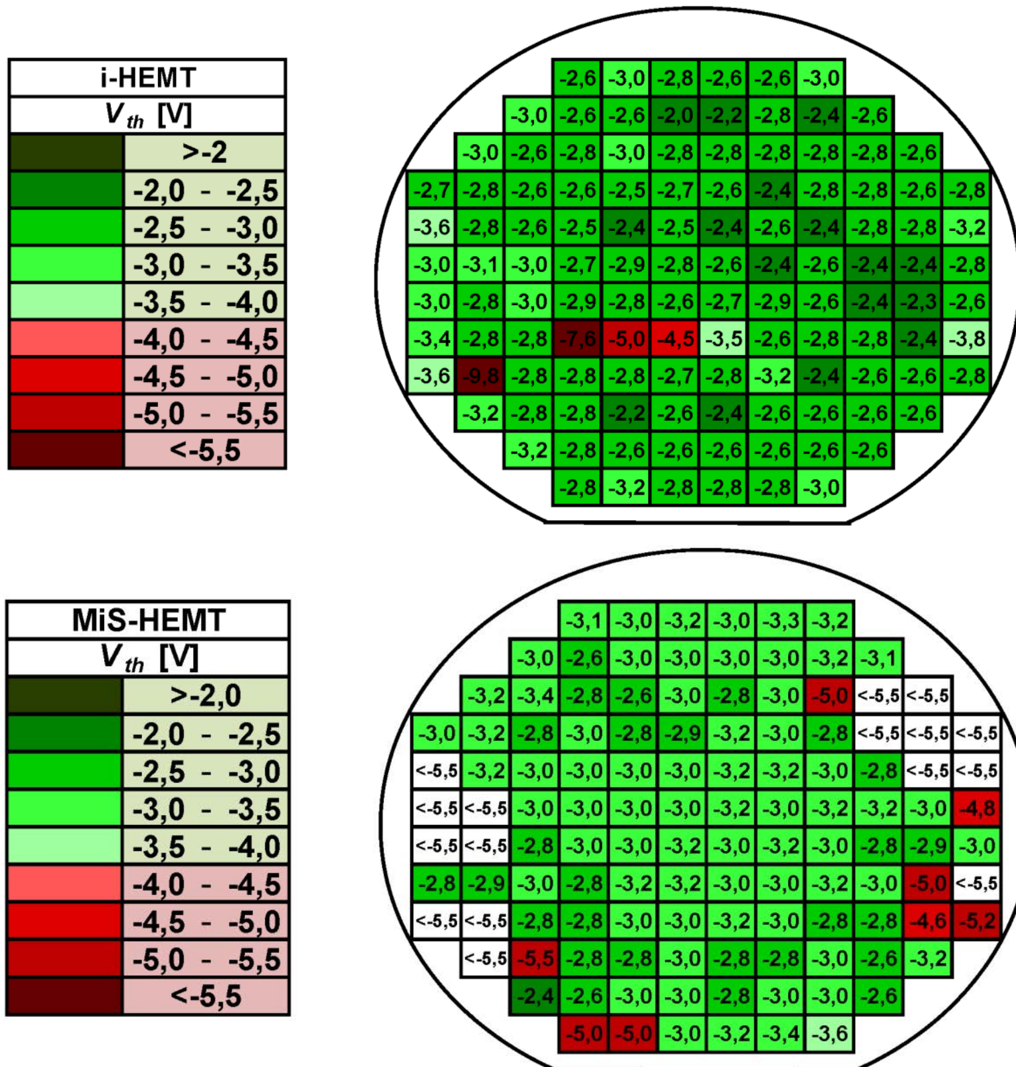

Figure 5-26. 4 $inch$ wafer scale maps for the (top) $i - HEMT$ and (bottom) $MIS - HEMT$ where a remarkably homogeneous V_{th} was determined ($-2.7 \pm 0.3\,V$ and $-3.0 \pm 0.3\,V$ for the $i - HEMT$ and $MIS - HEMT$, respectively).

Regarding extended positive gate bias operation, the thin HfO_2 based MIS approach also results in improved gate stability under positive gate bias as shown in figure 5-28. The Schottky injection was mitigated when the thin insulator was introduced with a forward voltage drift of $\Delta V_F = 1\,V$ for $I_{gd} = 10\,\mu A$. The extended positive gate bias stability is also evident when performing a full scale wafer map. The forward voltage drop at $10\,\mu A$ was determined to be $V_F = 2.1 \pm 0.8\,V$ and $3.2 \pm 0.6\,V$ for the $i - HEMT$ and $MIS - HEMT$, respectively. Two terminals I_{gd} suggest that a thin insulator prevents any Schottky injection for few positive volts $(\sim 2\,V)$. These few positive volts of margin appear to be consistent with the fact that the dielectric breakdown field of HfO_2 is $2 - 3\,MV/cm$.

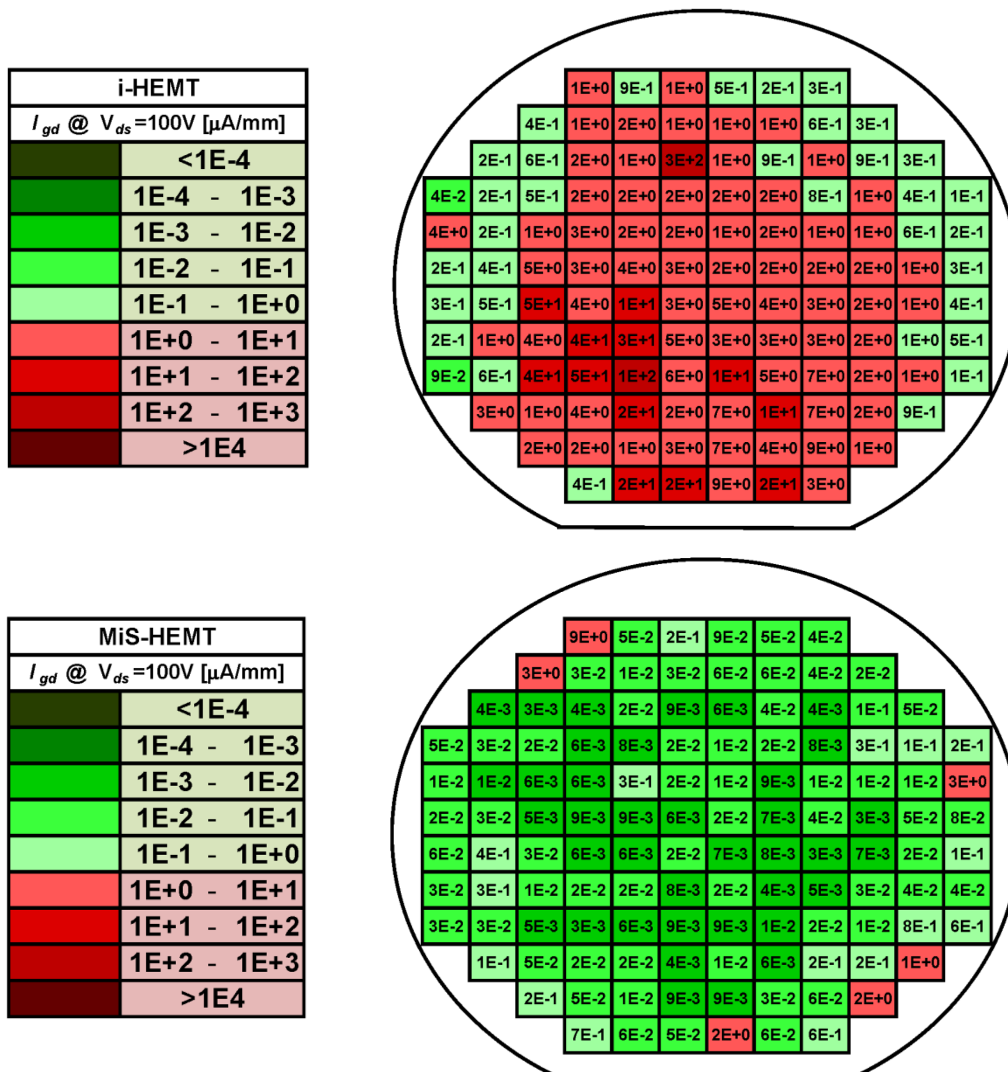

Figure 5-27. 4 $inch$ wafer scale maps for the 2-terminal gate-drain current. The mean current obtained for the $MIS - HEMT$ ($70 \pm 13\,nA/mm$) was significantly lower than for that obtained for the $i - HEMT$ ($2.0 \pm 1.9\,\mu A/mm$). Questionable edge device were excluded for the calculation.

When the $CAFM$ tests are performed on the $MIS-HEMT$ surface, as described in section 5.2.2, the current at the nanoscale is also significantly suppressed as shown in figure 5-29. At $-2\ V$, there is no correlation between the topography and the AFM tip current being this current, of $\sim 0.3\ pA$ (virtually negligible). Nevertheless, it was observed after intensive testing that if the bias is increased and a weak point within the insulator is located, then again the AFM current and topography would partially correlate in the same fashion as described in section 5.2.2.

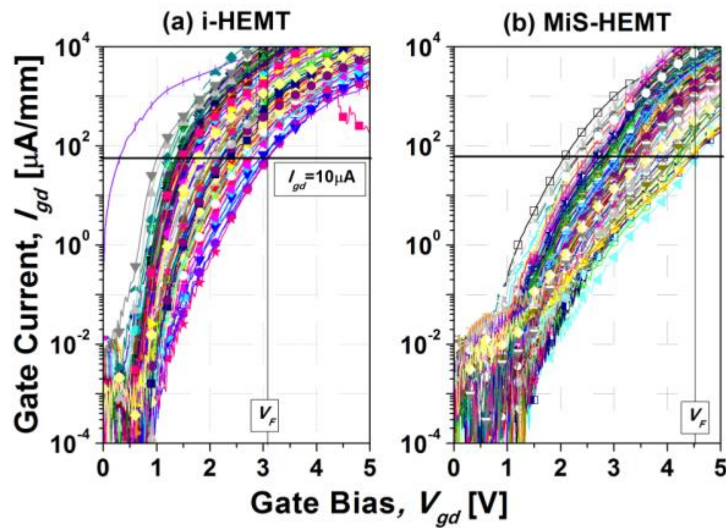

Figure 5-28. Comparison of the (a) $i-HEMT$ vs (b) $MIS-HEMT$ gate–drain current (I_{gd}) with the gate positively biased. The Schottky injection was mitigated when the thin insulator was introduced with a forward voltage drift of $\Delta V_F = 1\ V$ for $I_{gd} =\ 10\ \mu A$.

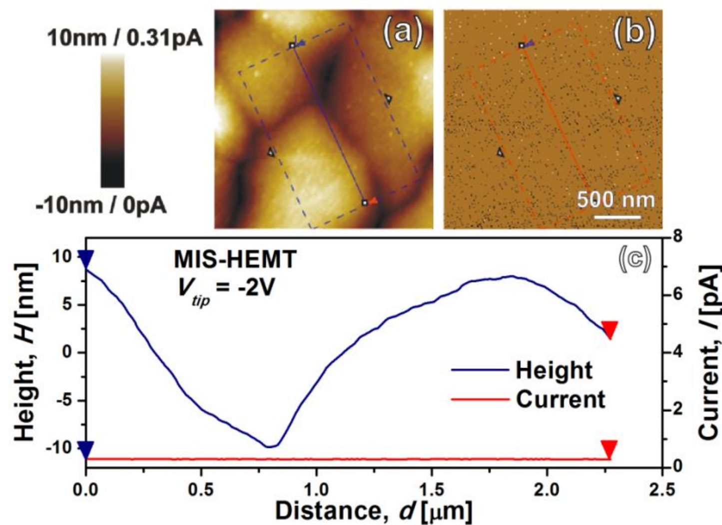

Figure 5-29. $CAFM$ scans of the $MIS-HEMT$ surface in the drain-gate spacing with (a) topography and (b) current map of surface taken with the $CAFM$ for the $2.8\ \times 2.8\ \mu m^2$ scan; (c) Respective cross-sectional profiles along the solid lines marked at $-2\ V$.

5.6. $Dynamic\ I - V$

Trapping phenomena represents a main limitation on $AlGaN/GaN$ based devices. $Dynamic\ I - V$ test is a measurement for revealing the discrepancy between conventional DC and pulsed analysis. Usually, $dynamic\ I - V$ tests are based in to apply pulsed signal from specifics quiescent points to drive the devices to points of the $I - V$ plane in order to recreate the $dynamic\ I - V$ characteristic. The current collapse, or also named dispersion, current compression, power slump, etc, is caused by deep traps in the material, especially by surface traps. It is measured as the discrepancy between the DC and pulse measurements. We also investigate the effect of the gate insulator during $dynamic\ I - V$ stress tests by using an $APMS2010RA$ system. The pulse width is 10 μs and the pulse separation is 100 μs. In this case, different quiescent points were evaluated as shown in table 5-2.

$Quiescent\ points$	$Pulsed\ I - V\ Measurements$			
$V_{ds}\ [V]$	0	20	50	110
$V_{gs}\ [V]$	-4	-4	-4	-4

Table 5-2. The drain lag was evaluated with pulsed I– V measurements from different quiescent points.

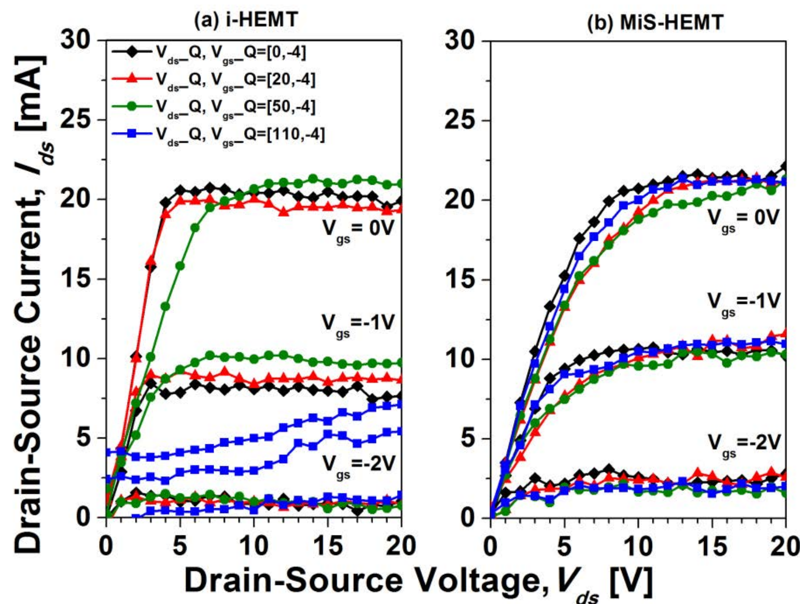

Figure 5-30. $MIS - HEMT\ vs\ i - HEMT\ dynamic\ I$– V characteristics. $MIS - HEMT$ showed no current collapse at $V_{ds} = 110\ V$. The drain lag was evaluated with pulsed I– V measurements from different quiescent points $[V_{ds}, V_{gs}]$, $[0, -4]$, $[20, -4]$, $[50, -4]$ and and $[110, -4]$ and a pulse length of 10 μs. Device characteristics were measured on test devices ($W = 150\ \mu m$).

Surface passivation technique using various dielectrics has been found to effectively relieve the current collapse issue by reducing the density of surface states. In this sense, the $dynamic\ I-V$ characteristics of the $MIS-HEMT$ for current collapse assessment are presented in figure 5-30.

A thin HfO_2 layer was very effective in reducing the current collapse when compared to the $i-HEMT$, suggesting an effective passivation of surface traps.[9,19,96] Gate and drain leakage currents as well as $dynamic\ I-V$ trapping were significantly improved with the $MIS-HEMT$ architecture with almost no trade-off to the $On-state$.

5.7. TRAPS CHARACTERISTICS $C-V$

Heterojunction device-based $AlGaN/GaN$ $HEMTs$ have already demonstrated outstanding performances on high-power and high-frequency applications.[1,97]

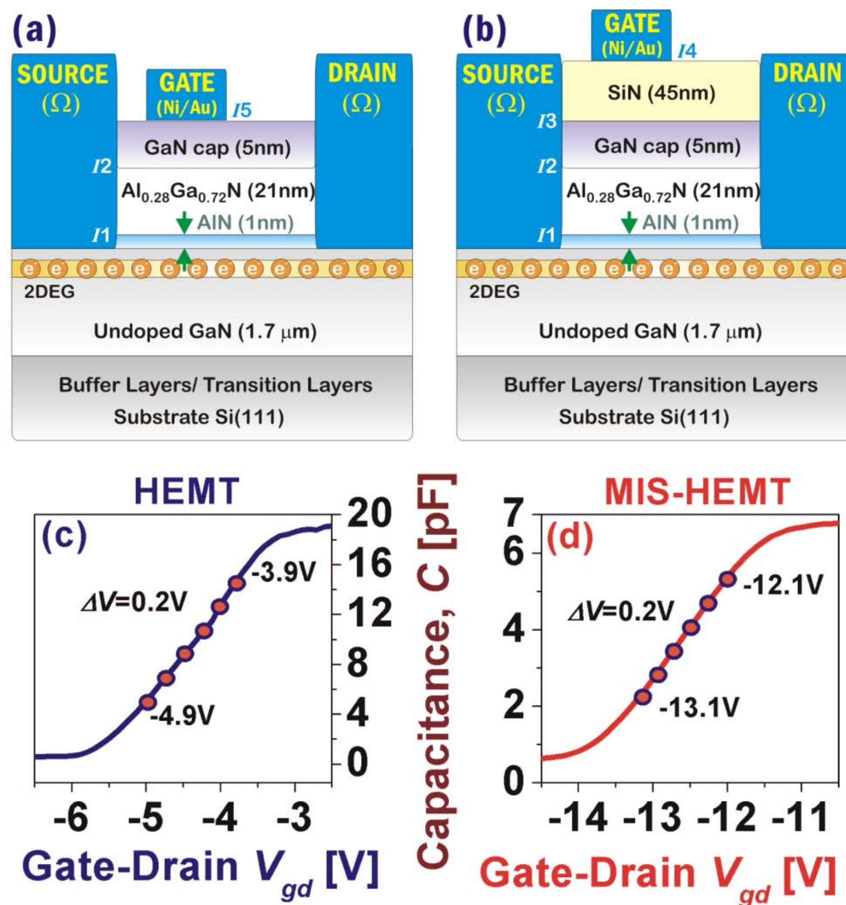

Figure 5-31. Cross-sectional view of the (a) $HEMT$ and (b) $MIS-HEMT$. High-frequency ($100\ kHz$) gate-drain $C-V$ for (c) the $HEMT$ and (d) the $MIS-HEMT$. Gate biases ($\Delta V = 0.2\ eV$) were selected for the conductance $G_p-\omega$ investigation.

The unique combination of the high-breakdown field, the high-mobility of the $2DEG$, and high-temperature of operation has attracted enormous interest from academia and from industry.

Since the technology is still in its infancy, the long term reliability of the devices remains an open issue. It is well known that the hetero-structure contains surface states, deep traps levels, and traps at the hetero-interfaces that can drastically deteriorate the device robustness. Several approaches have been used to investigate the trap profile and to estimate the trap density by means of spectroscopy,[23] transient,[24] and steady-state electrical methods,[25-33] in particular, the investigation into the gate admittance varying with frequency.[28-33] This last approach is analogous to the well-known conductance method (first proposed by Nicollian and Goetzberger[34] in 1967) for MIS structures. In this work, using the frequency dependent conductance analysis, we map the parallel conductance vs gate bias/frequency and further analyze the $slow$ and $fast$ traps as a function of the Fermi level for different gate architectures (Schottky and MIS). Besides, the variance in the band bending for fresh and stressed devices is determined.

Two $AlGaN/GaN - on - Si\ HEMT$ gate architectures (figure 5-31 (a) and (b)) were investigated, samples $C02$ and $C03$, a Schottky gate ($HEMT$) and a MIS gated $HEMTs$ ($MIS - HEMT$) respectively. Both fabrication details are explained in $chapter\ III$.

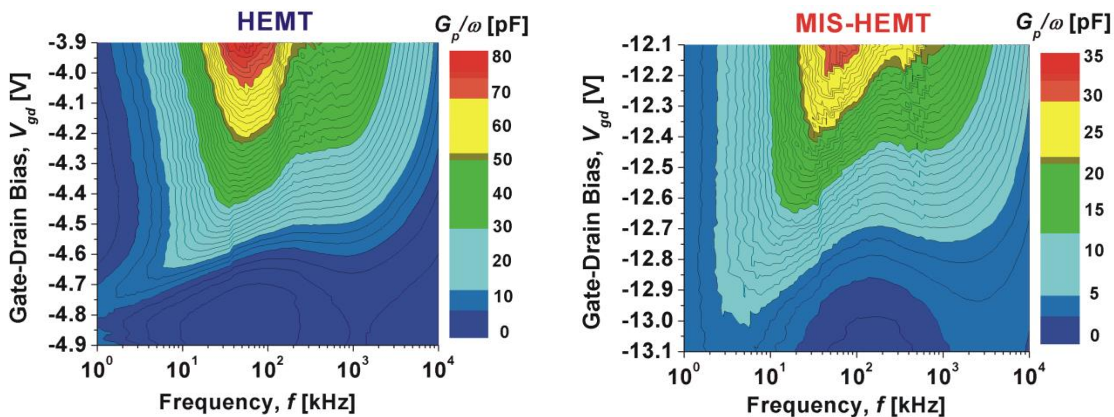

Figure 5-32. Reference $HEMT$ and $MIS - HEMT$ parallel conductance maps as a function of the gate bias and the frequency. Note the larger values of G_p/ω ($0 - 80\ pF$) for the $HEMT$ device. The peak value of G_p/ω increases with V_{gd} presenting two peaks which correspond to $fast$ and $slow$ gate traps.

It is well known that the passivation of the surface states with dielectric layers results in a reduction of interface traps.[31,82] This correlates well with the fact that $MIS-HEMT$ devices are reported to greatly mitigate the current collapse effect as well as reducing the gate leakage current. These facts make the $MIS-HEMT$ gate architecture more adequate for power switching applications. The mitigation of the conductance peaks (related with electron trapping at the interfaces) has been effectively corroborated for the $MIS-HEMT$ architecture as shown in figure 5-32.

$HEMT$ gate-drain (gate area $40 \times 150\ \mu m$) capacitance voltage (figure 5-31 (c) and (d)) and conductance voltage ($C/G-\omega$) measurements were performed ($1\ kHz$ to $10\ MHz$) at RT. The amplitude of the ac signal was $80\ mV$. The conductance method is regarded as the most accurate and sensitive of the small-signal steady-state methods,[60,98] whereby small AC variations in the gate voltage result in changes of the interface trap occupancy, and the resulting losses are detected. This energy loss is measured as an equivalent conductance (G_p). The parallel conductance G_p/ω maps shown in figure 5-32 have been determined after 51 $C/G-\omega$ measurements with $\Delta V_{gd}=0.02V$ ($1\ kHz$ to $10\ MHz$) in the gate-drain voltage (V_{gd}) range of $-4.9\ V/-3.9V$ for the $HEMT$ device and $-13.1\ V/-12.1\ V$ for the $MIS-HEMT$ (the V_{gd} range is illustrated in figure 5-31 (c) and (d)).

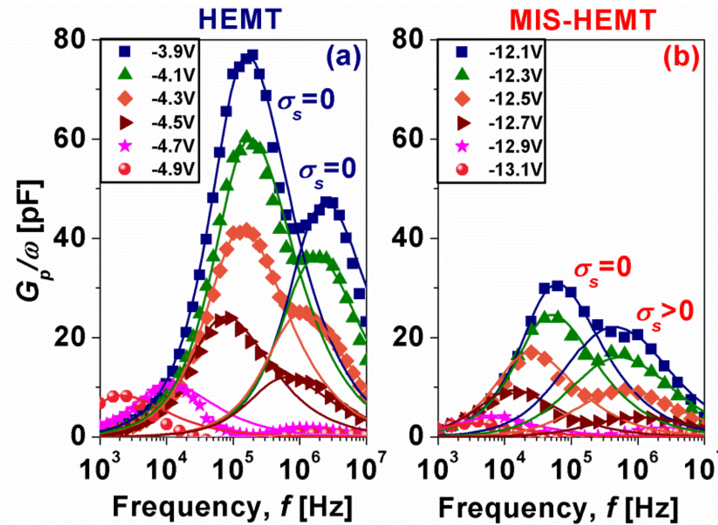

Figure 5-33. Experimental data (solid points) and fitting (solid lines) of $\langle G_p \rangle/\omega$ vs frequency for the (a) $HEMT$ and (b) $MIS-HEMT$ peaks (for the selected gate biases of figure 5-31 (c) and (d)). All the $HEMT$ peaks (as well as $MIS-HEMT$ $slow$ traps peaks) have been fitted with no band-bending fluctuations ($\sigma_s=0$). $MIS-HEMT$ $fast$ traps peaks exhibit non-negligible bandbending fluctuations (broadening).

The reduction of the conductance peak values (× 2.3 in the scale) for the MIS gate (as well as a shift of the peak frequency) is clearly visible from the experimental maps. In any case, the G_p/ω peak value always increases with increasing V_{gd}. Assuming a continuum of traps levels (but no trap time constant dispersion), G_p can be expressed as:[98]

$$\frac{\langle G_p \rangle}{\omega} = \frac{AqD_{it}}{2\omega\tau_p}\ln\left(1+\omega^2\tau_p^2\right) \tag{5-56}$$

Where A is the area, τ_p is the trap state time constant, and $\omega = 2\pi f$ is the angular velocity. $Eq.$ (5-56) has been used in previous works for extracting the D_{it} of $slow$ and $fast$ traps.[29-33] Nevertheless, a significant error can be made in extracting interface trap level density and time constant from a measured G_p/ω vs $\ln(f)$ curve if the interface trap time constant dispersion is not taken into account. As shown in the figure 5-33 (a), the band bending fluctuations may be ignored for the Schottky gate $HEMT$ device at the first instance (all the $HEMT$ curves were fitted using the $\sigma_s = 0$ model). This is also the case of $MIS-HEMT$ device $slow$ traps.

However, the $MIS-HEMT$ $fast$ traps (figure 5-33 (b)) could present significantly broadening of the G_p/ω peaks. A distribution of band bending over the interfacial plane caused by a random distribution of discrete charge in the interface is usually used to explain the experimental time constant dispersion. A time constant dispersion broadens the G_p/ω vs $\ln(f)$ curve, reduces the peak height for the same value of D_{it}, and increases the value of $\omega\tau_p$ at which the curve peaks. Assuming a continuous distribution of interface traps within the semiconductor bandgap and with band-bending (U_s) fluctuations at the heterointerface interface, G_p can be described as:[98]

$$\frac{\langle G_p \rangle}{\omega} = \frac{qA}{2}\int_{-\infty}^{\infty}\frac{D_{it}}{\omega\tau_p}\ln\left(1+\omega^2\tau_p^2\right)P(U_s)dU_s \tag{5-57}$$

The most common distribution characterized by only its mean and variance is the Gaussian and thus G_p/ω is of the form:[98]

$$\frac{\langle G_p \rangle}{\omega} = \frac{qAD_{it}(2\pi\sigma_s^2)^{-1/2}}{2\xi}\int_{-\infty}^{\infty} exp\left(-\frac{\eta^2}{2\sigma_s^2}\right)\times exp(-\eta)\ln(1+\xi^2 exp2\eta)d\eta \tag{5-58}$$

Where σ_s is the standard deviation of the band-bending and $\xi \equiv \omega\tau_p$. The procedure to determine σ_s is to measure the amplitude of change of this curve either between the points f_p (peak frequency) and f_p/n or between f_p and $n \times f_p$ (typically $n = 1/5$ or $n = 5$). Once experimentally determined the ratio of $[\langle G_p\rangle/\omega]_{nf_p}/[\langle G_p\rangle/\omega]_{f_p}$ this value is interpolated into the previously computed plot of $[\langle G_p\rangle/\omega]_{nf_p}/[\langle G_p\rangle/\omega]_{f_p}$ *vs* σ_s, for a given n and ξ (typically $\xi = 2.5$). Once σ_s has been determined, the interface state density, D_{it}, may be evaluated numerically by integrating *eq.*(5-58) at $\xi = \xi_p$, with $\left(\langle G_p\rangle/\omega\right)_{f_p}$. The condition $d/d\xi\left[\left(\langle G_p\rangle/\omega\right)_{f_p}\right]$ is used to determine τ_p and then:[98]

$$\int_{-\infty}^{\infty} exp\left(-\frac{\eta^2}{2\sigma_s^2}\right) exp(-\eta)\left[\frac{2\xi_p^2 exp2\eta}{1+\xi_p^2 exp2\eta} - \left(1+\xi_p^2 exp2\eta\right)\right]\times d\eta = 0 \quad (5\text{-}59)$$

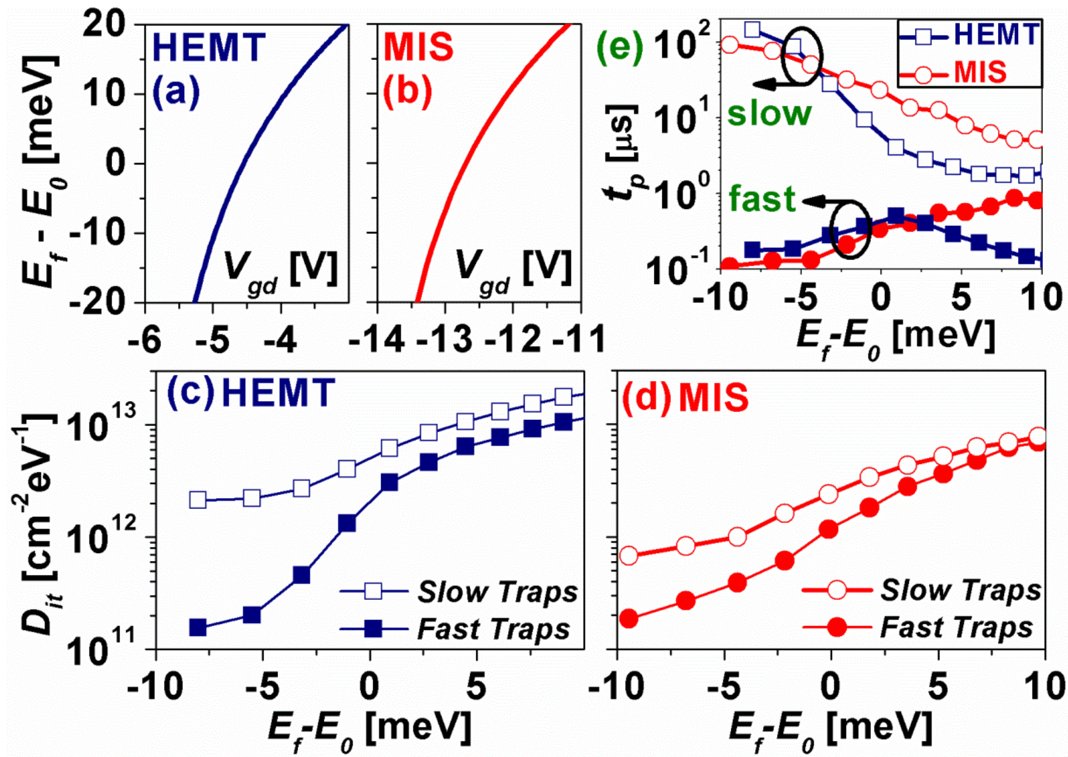

Figure 5-34. Fermi level position relative to the position of the $2DEG$ quantum well first sub-band ($E_f - E_0$) vs the gate-drain bias (V_{gd}) for the (a) $HEMT$ and (b) $MIS-HEMT$. (c) $HEMT$ interface trap density vs the Fermi level determined from the conductance method with no band-bending fluctuations. (d) $MIS-HEMT$ interface trap density vs the Fermi level determined from the conductance method with band-bending fluctuations for the fast traps. (e) Characteristic trap time constant vs $E_f - E_0$ for the different conductance peaks.

Solving $eq.$(5-59) numerically (for example, using the Newton-Raphson algorithm) yields ξ_p as a function of σ_s. Then, from the relation $\xi_p = \omega_p\tau_p$, the interface trap level time constant can be extracted. σ_s is a measure of the width of the experimental G_p/ω vs $\ln(f)$. If those curves are narrow, band-bending fluctuations can be neglected ($\sigma_s \approx 0$) and then $\langle G_p\rangle/\omega$ reduces to $eq.$(5-56).

The experimental values of σ_s, D_{it}, and τ_p are shown in figure 5-34 and figure 5-35. The x-scale ($E_f - E_0$) is the relative voltage Fermi level position relative to the position of the $2DEG$ quantum well first sub-band from the on-set of the $2DEG$ formation.

We have used the approximation given by Khandelwal *et al.*[99] for the numerical computation of Fermi level position as:

$$E_f = V_{g0}\frac{\beta\ln(\alpha_1 V_{g0}) + \gamma_0\left(q^{-1}C_{gd}V_{g0}\right)^{2/3}}{V_{g0} + \beta + (2/3)\gamma_0\left(q^{-1}C_{gd}V_{g0}\right)^{2/3}} \tag{5-60}$$

Where $\beta = k_BT/q$ is the thermal energy, $V_{g0} = V_{gd} - V_{th}$ is the normalized gate voltage respect to the threshold voltage (V_{th}), $\alpha_1 = C_{gd}/(q\Delta\beta)$ where C_{gd} is the gate-drain capacitance, Δ and γ_0 are numerical constants from literature.[99] The position of the first sub-band E_0 can be computed from the $2DEG$ sheet density (n_s) as $E_0 = \gamma_0 n_s^{2/3}$. Solving the Schrödinger equation n_s is related to E_f by the well-known expression $n_s = q^{-1}C_{gd}(V_{g0} - E_f)$. We assume zero current flow through the hetero-layers under all static bias, i.e., the semiconductor always remain in equilibrium independent of the V_{gd}.

A bias applied to the gate causes potential drops and conduction (and valence) band bending interior to the structure. In the case of the $MIS-HEMT$, the gate capacitance (C_{MIS}) is coupled with the insulator capacitance (C_{ins}) as $C_{gd} = C_{MIS}C_{ins}/(C_{ins} - C_{MIS})$. The insulator capacitance depends on the Si_3N_4 dielectric constant and thickness (d) as $C_{ins} = \varepsilon_r/d$. Computed $E_f - E_0$ vs V_{gd} are presented in figure 5-34 (a) and (b) for the $HEMT$ and $MIS-HEMT$, respectively. The D_{it} for the $HEMT$ and $MIS-HEMT$ as a function of the relative position of E_F is presented in figure 5-34 (c) and (d). For the gate biases closest to the V_{th}, $slow$ traps ($\tau_p \sim 0.1\ ms$) and $fast$ traps ($\tau_p \sim 0.1\ \mu s$) were revealed (figure 5-34 (e)) for both the $HEMT$ and $MIS-HEMT$ devices, the band-bending being irrelevant in either case.

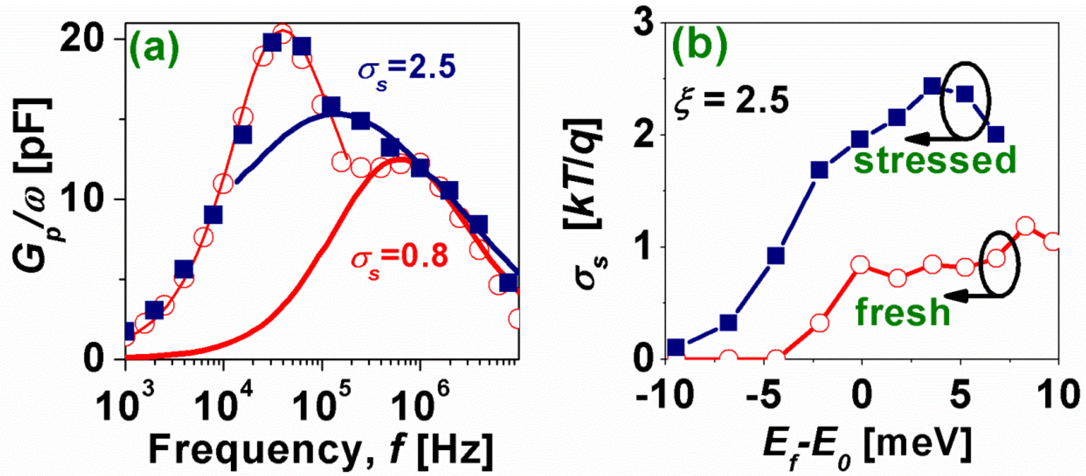

Figure 5-35. (a) Comparison of the conductance $fast$ traps peaks before $\sigma_s = 0.8\,k_BT/q$ and after stress $\sigma_s = 2.5\,k_BT/q$ for a $MIS-HEMT$ $\left(V_{gd} = -12.4\,V\;\; E_F - E_0 = 5.2\,meV\right)$. (b) Fresh and stressed $MIS-HEMT$ variance of the band bending for different Fermi level energies.

However, τ_p is progressively reduced for larger gate biases (particularly for the $HEMT$) up to $1\,\mu s$. The density of the $slow$ traps is significantly lower for the $MIS-HEMT(D_{it} \sim 7.0\times10^{11} - 5.0\times10^{12}cm^{-2}eV^{-1})$, when compared with the $HEMT$ $(D_{it} \sim 2.0\times10^{12} - 2.0\times10^{13}cm^{-2}eV^{-1})$, in agreement with the current view that (a number of) these traps are surface related, and that the MIS structure effectively passivates the traps. As gate voltage increases, the conductance peaks are shifted in frequency, and the G_p/ω peak value increases.

All the $HEMT$ $fast$ trap G_p/ω peaks can also be closely fitted by the trap time constant model $(\sigma_s = 0)$ with $(D_{it} \sim 2.0\times10^{11} - 7.0\times10^{12}cm^{-2}eV^{-1})$. However, the band bending fluctuations shown in figure 5-35 would indicate the presence of additional longer-range fluctuations in the interfacial charge (and insulator charge) for the $MIS-HEMT$. When $\sigma_s = 0$, one can think of traps randomly situated but with a short range variation from one another on the interfacial plane (and closely spaced in energy distributed through the entire bandgap). Larger values of σ_s (as shown in figure 5-35 (b) up to $\sim 1.1\,k_BT/q$) would suggest longer-wavelength interfacial charge nonuniformities. The depletion width would be effectively modulated (which is known as the parallel array model)[100] and the gate area capacitor can be divided into patches. In each patch, the depletion layer width would be nearly uniform, responding only to spatial variations of interface charge that extend over comparable distances to that width. If we assume an applied voltage of V_{th}, a depletion width will form comparable

to the $AlGaN$ buffer,[101] and it can be suggested that the wavelength of the MIS-related traps will be several tens of nanometers. Any $MIS-HEMT$ thin gate dielectric layer is prone to degrade easily during low to moderate stress tests. This is particularly true when the gate is positively biased (hot carrier injection) during $HEMT$ operation, or when a current (even a small current) is forced to flow through the gate dielectric. Stressed $HEMTs$ are reported to have increased trap densities.[28] In this experiment, the $MIS-HEMT$ device was degraded by performing subsequent transfers ($I_{ds}-V_{gs}$) from $V_{gs}=-25\ V$ up to $10\ V$ at intervals of $0.5\ V$. It was observed that the stress-induced additional states (figure 5-35 (a)) could present significantly broader peaks. The broader conductance peaks and the larger band bending fluctuations ($\sigma_s{\sim}2.5\ k_BT/q$) would indicate the presence of additional longer-range fluctuations in the interfacial charge (and insulator charge) that would suggest longer-wavelength interfacial charge nonuniformities.

5.8. SUMMARY

In this chapter the fundamentals of the $AlGaN/GaN\ HEMT$ gate contact have been reviewed. As it occurs with the most of the electronic switches, the gate stack is maybe the critical part of the device in terms of performance and longtime reliability. This chapter is devoted to the investigation of how the gate (composition, materials, defects and others) affects the overall $HEMT$ behaviour by means of advanced characterization and modeling.

First, the nanoscale features of a typical Schottky contact to an $AlGaN/GaN\ HEMT$ have been investigated in detail by means of the $CAFM$ technique. The $MBE\ AlGaN/GaN-on-Si\ HEMT$ surface is composed of mounds, in the form of a truncated elliptical parabola corresponding to the morphological pattern. This complex relationship is attributed to the inhomogeneous distribution of threading dislocations (with a density of $\sim 70\ \mu m^{-2}$) formed during the double spiral $BCF-kinetic\ mode$ of growth and the fact of analyzing the vertical current. The mound size distribution is fairly uniform with, on average, a base of $1.5\ \mu m$ and a height of 100 Å (peak to valley distance). At the nanoscale, depressions in the topography appear to partially correlate with the current peaks in the current map. Conductive areas represented just 7% of the measured area. However, the current density of the conductive areas has been calculated to be as high as $2\ A\ cm^{-2}$. However, neither all the depressions exhibit large local

leakage nor all the mounds are immune to some current spike. Besides, when the tip is biased at $-2\ V$ and $-10\ V$, it seems to correlate with the macroscopic $I - V\ vs\ T$ tests of the vertical Schottky gate produced values of $\Phi_B = 0.7\ eV$ and $\Phi_t = 0.3\ eV$ fitted with $Poole\text{–}Frenkel$ $\left(-V_{gb} < 10\ V\right)$ and $Fowler\text{–}Nordheim$ tunneling $\left(-V_{gb} > 10\ V\right)$, respectively, which, in turn, would be threading dislocation and/or nanopipe assisted conduction mechanism, respectively. A thin dielectric can effectively mitigate this leakage current also at the nanoscale. This concept has been further elaborated in the next section.

A thin insulator is often introduced between the gate metal and the $AlGaN$ barrier layer resulting in a device known as a $MIS - HEMT$, which significantly suppresses gate leakage. It is also well known that a thin gate dielectric has a beneficial effect on the reliability of a transistor, the mitigation against current collapse being one such effect. Therefore, the $MIS - HEMT$ concept has been intensively investigated in this chapter.

First, it has been presented a compact set of analytical closed-form expressions for the numerical computation of the drain current, the transfer current and the transconductance of $AlGaN/GaN$ $HEMTs$. The g_m temperature dependence as $T^{-1.1}$ was apparently not in agreement with the one expected from the polar-optical phonon dependence. To further investigate this, a closed-form analytical expression (based on the $2DEG$ channel physical modeling) for the intrinsic and extrinsic transconductance of $AlGaN/GaN$ $HEMTs$ was proposed. The model includes access resistance and self-heating effects. The simulation values reproduce reasonably well the experimental values using meaningful physical parameters.

Afterwards, the impact of introducing a thin gate dielectric in these devices has been investigated; by modifying the previous model this being the basis of a $MIS - HEMT$ device. It have been numerically investigated the drain current, saturation current and transconductance properties of a $MIS - HEMT$ using SiO_2, Si_3N_4, Al_2O_3 and HfO_2 as gate insulators. It has been also evaluated again the effect of the source and/or the source-drain series resistance along with self-heating. The simulation results explain reasonably well the general experimental set of results: The $MIS - HEMT$ (when compared to an identical $HEMT$) presents the same on-resistance (at $V_{gs} = 0\ V$), higher saturation current (also at $V_{gs} = 0\ V$) but lower experimental saturation

transconductance. For a given $I_{ds,sat}$ increases as the gate capacitance decreases. Gate capacitance decreases with insulator thickness and/or with lower dielectric constant which, in turn, has an impact on the V_{th} and the $I_{ds,sat}$ peak for the different insulators (in our case SiO_2, Si_3N_4, Al_2O_3 and HfO_2). The model also suggests that self-heating has a relevant role in reducing the saturation $On-state$ current. The thermal impedance (R_{th}) of the substrate (SiC, Si or $sapphire$) has a strong influence on both $I_{ds,sat}$ and g_m. R_{th} depends on the substrate thermal conductivity and thermal boundary resistances, elevating the channel temperature to an effective temperature. This effective temperature increase significantly degrades the electron mobility (promoted by phonon scattering) and hence, $I_{ds,sat}$ and g_m. As the MIS gate capacitance provokes an increase of I_{ds}, the g_m would be further reduced for a $MIS-HEMT$ for a given V_{ds} (i.e., larger dissipated power increasing the channel effective temperature for a given saturation drain voltage).

From an experimental standpoint, several $MIS-HEMT$ and Schottky gate $HEMTs$ have been comparatively studied under bias and temperature stress conditions. Several test, as DC , $dynamic\ I-V$ and $high-T$ stress tests for a stable $800V/300°C$ $Au-free\ GaN-on-Si\ HEMT\ 4-inch\ Si\ CMOS$ compatible technology was presented. The thin HfO_2 layer is very effective in reducing the current collapse when compared to the $i-HEMT$, suggesting an effective passivation of surface traps. The introduction of the thin HfO_2 only caused a small V_{th} drift to negative values while other forward characteristics ($g_m, I_{ds,sat}, etc.$) only exhibit minor changes. It has been verified that the introduction of the thin insulator had a marked beneficial role in reducing the gate leakage current all over the wafer. The thin HfO_2 based MIS approach also resulted in improved gate stability under positive gate bias. The Schottky injection was mitigated when the thin insulator was introduced.

Finally, the gate trap properties of $HEMT$ and a $MIS-HEMT$ have been analyzed by means of the C/G vs ω techniques (conductance analysis). The effect of low-moderate MIS gate stress is also analyzed. D_{it}, τ_p, and σ_s have been investigated for a large range of gate biases for $slow$ and $fast$ traps. The density of the $slow$ traps is significantly lower for the $MIS-HEMT$ ($D_{it} \sim 7.0 \times 10^{11} - 5.0 \times 10^{12} cm^{-2}eV^{-1}$), when compared with the $HEMT$ ($D_{it} \sim 2.0 \times 10^{12} - 2.0 \times 10^{13} cm^{-2}eV^{-1}$). All the $HEMT$ $fast$ trap G_p/ω peaks can also be closely fitted considering $\sigma_s = 0$ ($D_{it} \sim 2.0 \times 10^{11} -$

$7.0 \times 10^{12} cm^{-2} eV^{-1}$). However, non-negligible peak broadening would indicate the presence of longer-range fluctuations in the interfacial charge (and insulator charge) for the $MIS - HEMT\ fast$ traps. Additional gate stress appears to have a notable effect on the fast trap profile of the MIS, not only in the D_{it} value (which is slightly increased), but in the increase of σ_s up to $\sigma_s \sim 2.5\ k_B T/q$. This large value of σ_s would suggest the presence of additional larger-wavelength defective sites after the stress.

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Chapter 6

AlGaN/GaN HEMT high-voltage and high-temperature

6.1. INTRODUCTION

The $AlGaN/GaN\ HEMTs$ presents excellent proprieties as potential power switch device for high-voltage, high-frequency and $high-T$ applications. $GaN\ HEMTs$ have attracted great attention due to their low gate charge and reverse recovery charge, a low $R_{on,sp}$ and high V_B.[1-3] From a device engineer point of view, low R_{on}, gate charge (Q_g) and drain and gate leakage currents together with a high-manufacturing yield are required.

In the first section of this chapter we will present a summary of the main results from the fabricated power $HEMTs$ in the framework of the industrial contract with ON semiconductor. The fabricated devices were close to the state-of-the-art taking into account their power device figure-of-merit ($V_B^2/R_{on,sp}$). This trade-off figure has been presented for our $GaN\ HEMTs$ and has been compared with other similar devices from the literature.

The second part of this chapter is devoted to the analysis of which is the effect of the elevated temperature on a $HEMT$ device. Uncooled electronics is the typical niche application for power $GaN\ HEMTs$. A key advantage of GaN power devices over traditional Si devices is the $high-T$ of operation. Traditional Si devices cannot operate at temperatures higher than 180 °C while GaN power devices can work correctly at much higher temperature than 300 °C (this temperature limit is actually due to the packaging rather than the device itself which is able to work at much higher temperatures). The WBG of the semiconductor enables the operation at elevated temperatures without suffering intrinsic inter-band conduction. This opens the door to uncooled converters to be implemented in more efficient, lighter and eco-friendly systems.[4] How the elevated temperature impacts on the performance of a GaN solid-state device is therefore a critical issue. Several authors[5-8] have addressed this topic with some degree of detail. One can assume that, as the temperature increases, the electron mobility decreases due to several carrier scattering unavoidable effects and, in particular, due to the polar-optical phonons.[9] The temperature dependence of this degradation would directly depend on the effective temperature in the $2DEG$ channel. In addition, the effective temperature on the channel may be significantly higher due to the self-heating.[10,11]

Therefore, as the temperature increases, the $On-state$ and $Off-state$ currents of $AlGaN/GaN$ heterojunction transistors are degraded. In the last section it will be presented the impact of the different substrates (Si, $shappire$ and $FS-GaN$) on the forward and the reverse leakage currents (gate, drain and bulk). In addition, preliminary assessment of the device $Off-state$ reliability has been performed at elevated temperatures up to 300 °C.

6.2. HIGH-VOLTAGE POWER $HEMT$

The main results out of the ON semiconductor project will be presented in this section. Device were made at CNM during $2008-2012$. The characterization was, (for the $AlGaN/GaN$ devices designed for high-voltage), by means of DC wafer mappings, reverse and breakdown voltage in $Galden\ bath$ and $high-T$ stress. Two batches of $AlGaN/GaN-on-Si\ MIS$ gated $HEMTs$ devices were fabricated (i) using a thin $ALD\ HfO_2$ (deposited in the CNM clean room) and (ii) thin in-situ grown Si_3N_4 (from the vendor) as a gate insulator on 4 $inch$ wafers.

Here we only present the main results of the project but a large amount of work has been performed for the optimization of the Ohmic and Schottky contact. My role in the project was mainly the characterization of the wafers.

Full 4 $inch$ wafer scan mapping in terms of $R_{on,sp}$,V_{th}, I_{gd}, $I_{ds,off}$ and $I_{gs,off}$ (V_{ds} at $100\ V$) and the forward and reverse measurements in large $HEMTs$ will be presented. Finally, gate stability under large positive gate bias have been investigated to know the device gate degradation. The wafer-level analysis was investigated with 120 test devices across the 4 $inch$ wafer with a $3/(8-12)/3\ \mu m$ for $L_{gs}/L_{gd}/L_g$, respectively. The device W was $150\ \mu m$ in all cases.

6.2.1. THIN $ALD\ HfO_2\ AlGaN/GaN$ POWER $MIS-HEMT$

6.2.1.1. DC CHARACTERIZATION ($On-state$)

When compared to the Schottky gate solution in the same wafer, gate and drain leakage currents were significantly improved with the $MIS-HEMT$ architecture, (thin HfO_2 as the gate insulator); with almost no trade-off to the $On-state$. Figure 6-1 shows $On-state$ results for thin HfO_2 $MIS-HEMT$ sample ($A03b$). The gate and drain leakage currents were significant lower than $10\ nA/mm$. The threshold voltage was around $-3.8\ V$ and the relation on/off is of more of 7 orders of magnitude. The transconductance peak ($g_{m,max}$) is in the order of $100\ mS/mm$.

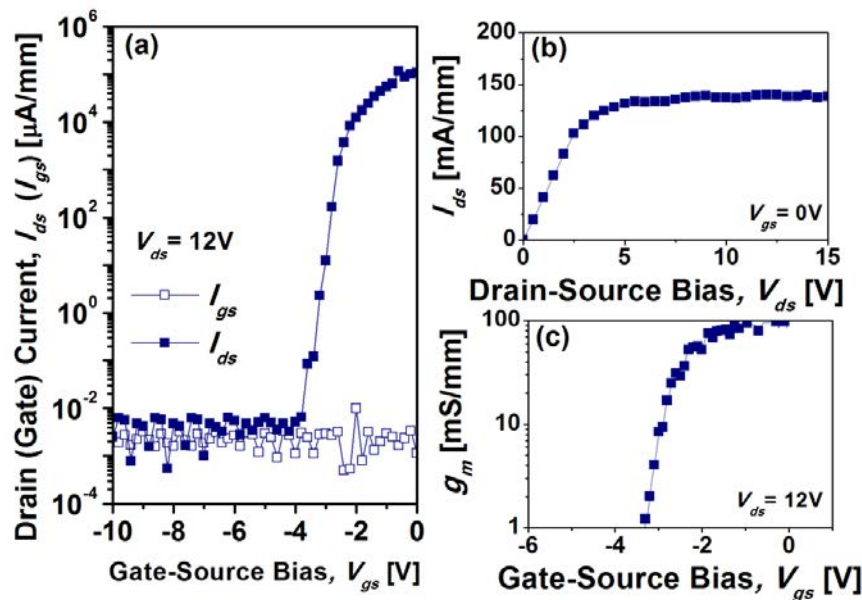

Figure 6-1. Typical HfO_2 $MIS-HEMT$ (a) transfer curve showing the reduced gate and drain currents. (b) $I-V$ forward curve and (c) transconductance comparison extracted from the derivative of the transfer curve.

6.2.1.2. DC CHARACTERIZATION $(Off - state)$

The DC reverse characterization was carried out using a $Galden\ bath$ to avoid arcing in air (figure 6-2). The maximum breakdown voltage achieved was $750\ V$. The fabrication process was stable with a high-number of devices with $V_B > 700\ V$ for L_{gd} over $10\ \mu m$.[12]

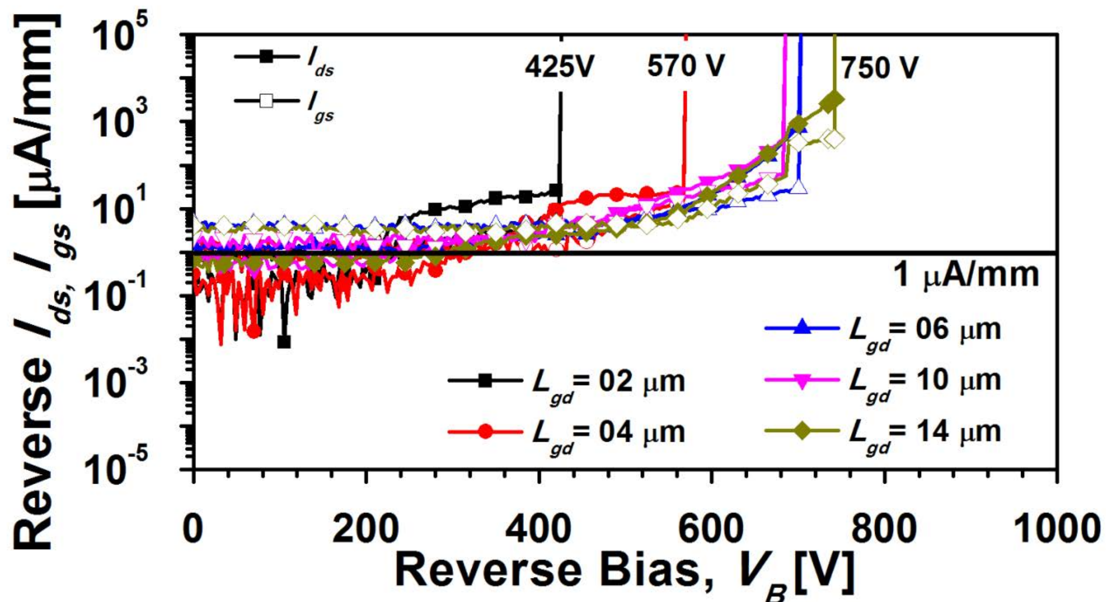

Figure 6-2. HfO_2 $MIS - HEMT$ **gate and drain (**I_{gs} **and** I_{ds}**) reverse characteristics for different gate–drain spacings. The breakdown voltage value approaches** $750\ V$ **for** $L_{gd} = 14\ \mu m$**.**

6.2.1.3. HIGH-CURRENT $HEMTs$

As presented in the $chapter\ III$, ideally the $HEMT - on - Si$ fabrication process should be $gold - free$. In particular the Ohmic contacts should be $Au - free$.

As shown in figure 6-3 (a), $Au - free$ large area $HEMTs$ ($W = 31\ mm$) yield more than $18\ A$, with an on-resistance of $0.4\ \Omega$ for $V_{gs} = 0\ V$. A thicker second metal level was deposited on top of the $Au - free$ Ohmic contacts to achieve a current of several amperes. Figure 6-3 (b) presents the reverse characteristics showing leakage currents below $1\ \mu A/mm$ up to $500\ V$.

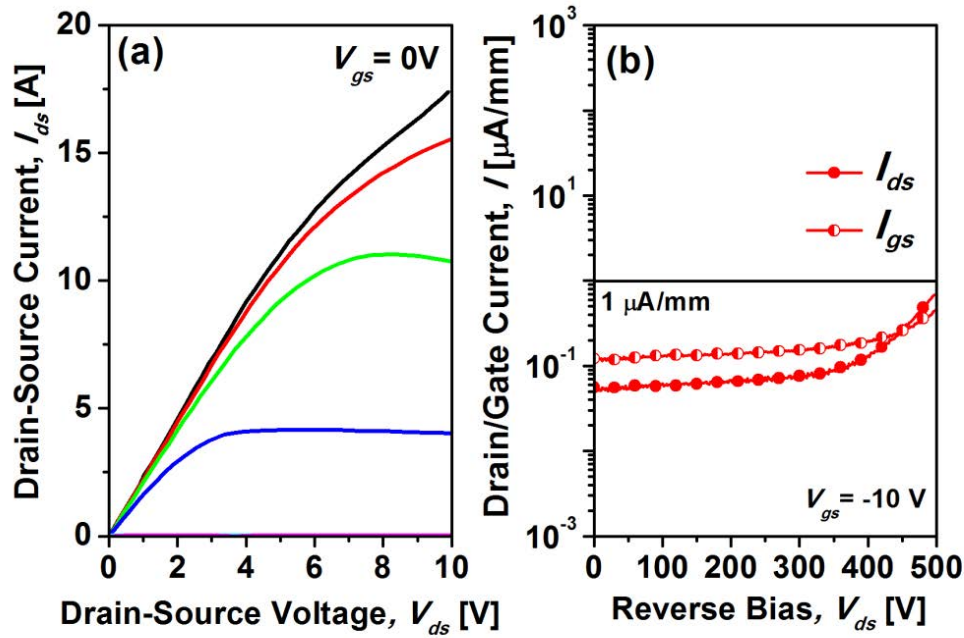

Figure 6-3. HfO_2 $MIS-HEMT$ (a) Output DC characteristics of a large area $AlGaN/GaN$ $HEMT$ and (b) Reverse characteristics of the device showing leakage currents below $1\ \mu A/mm$ up to $500\ V$.

6.2.1.4. POSITIVE GATE BIAS

In addition, positive gate-source voltage study has been analyzed in terms to investigate how the gate leakage current affects the normal transistor operation. As shown in figure 6-4 (a), in that case "normal operation" was achieved to, say $V_g = +4.5\ V$. From this value, it is evident the effect of the leakage current on the $I_{ds} - V_{ds}$ characteristic.

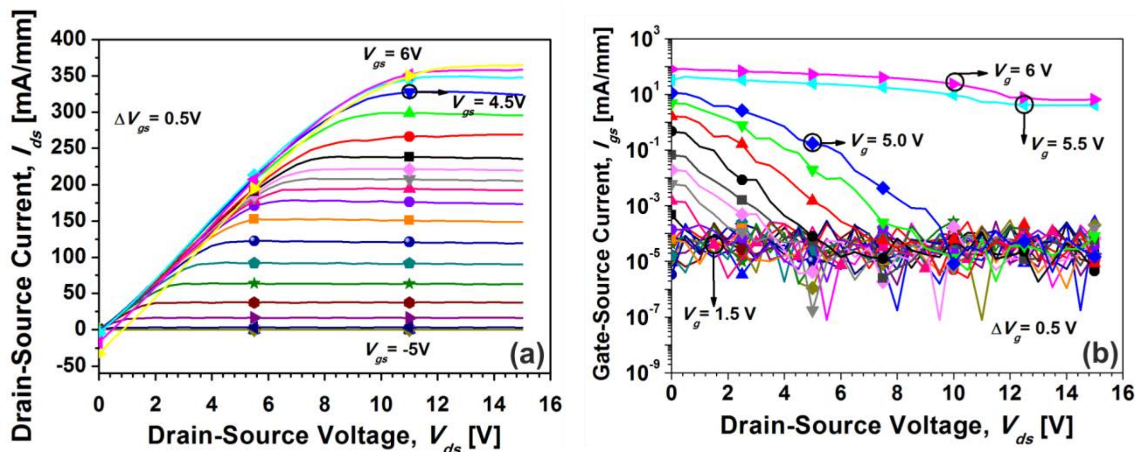

Figure 6-4. HfO_2 $MIS-HEMT$ for positive V_{gs} ($\Delta V_{gs} = 0.5\ V$) (a) drain source current *vs* drain source voltage and (b) gate source current *vs* drain source voltage.

It was observed in figure 6-4 (b), a strong degradation effect for large positive gate voltages (gate breakdown). This was observed for $V_{gs} > 5.5\,V$. In figure 6-5 after transconductance curve for "large" $+V_{gs}$ that Schottky gate injection occurs depending on V_{ds}.

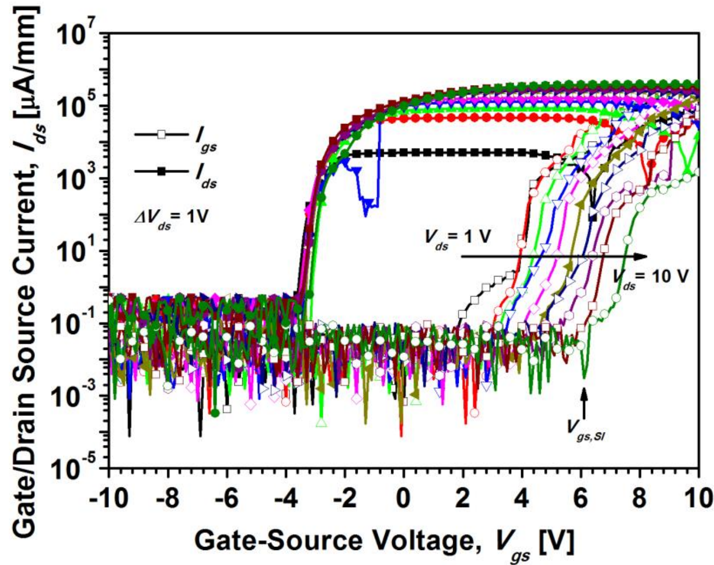

Figure 6-5. HfO_2 $MIS-HEMT$ up to $V_{gs} = 10\,V$ ($\Delta V_{ds} = 1\,V$) drain I_{ds} vs V_{gs}.

6.2.1.5. 4 $inch$ WAFER MAPPING

For the HfO_2 $MIS-HEMT$, extensive DC forward characterization was performed at 4 $inch$ wafer scale, in terms of $R_{on,sp}$, V_{th}, two terminals I_{gd}. Figure 6-6 presents the $R_{on,sp}$ mapping which the mean value is around $2.8 \pm 0.35\ m\Omega cm^2$.

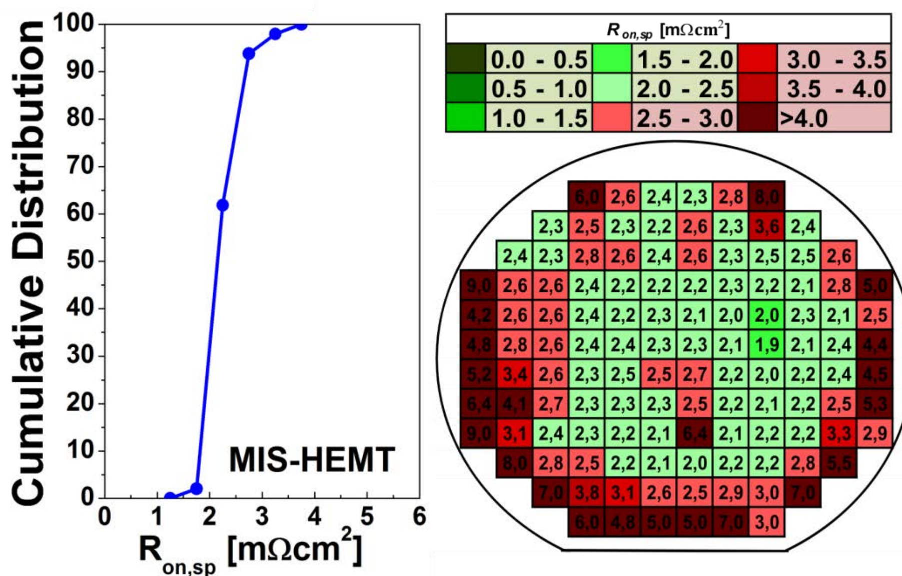

Figure 6-6. HfO_2 $MIS-HEMT$ wafer map for $R_{on,sp}$ at $V_{ds} = 1\,V$ with $3/8/3\ \mu m$ for $L_{gs}/L_{gd}/L_g$.

When full-wafer maps are carried out (figure 6-7) this threshold shift can be quantified as small as $\Delta V_{th} = 0.3\ V$.

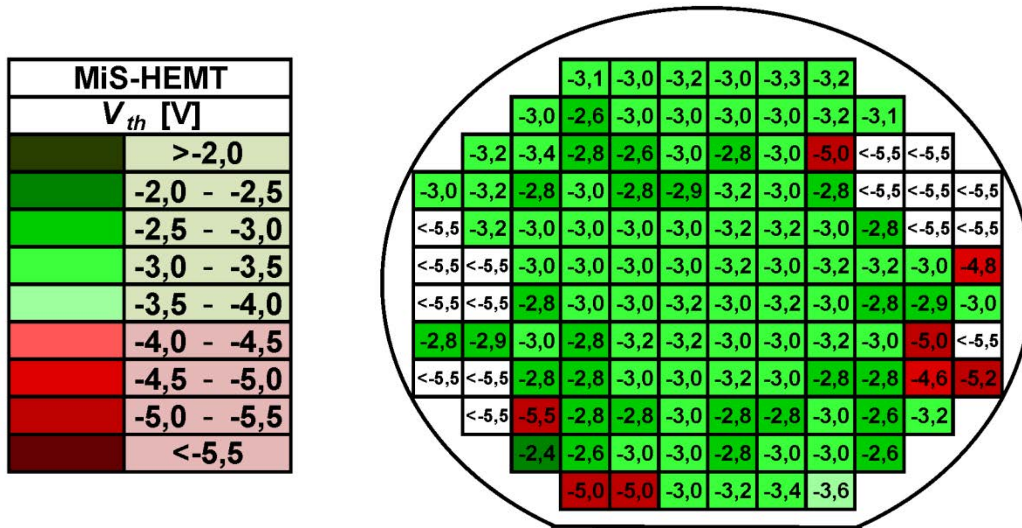

Figure 6-7. HfO_2 $MIS-HEMT$ **wafer scale map for the remarkably homogeneous** V_{th} **was determined** $-3.0 \pm 0.3\ V$**.**

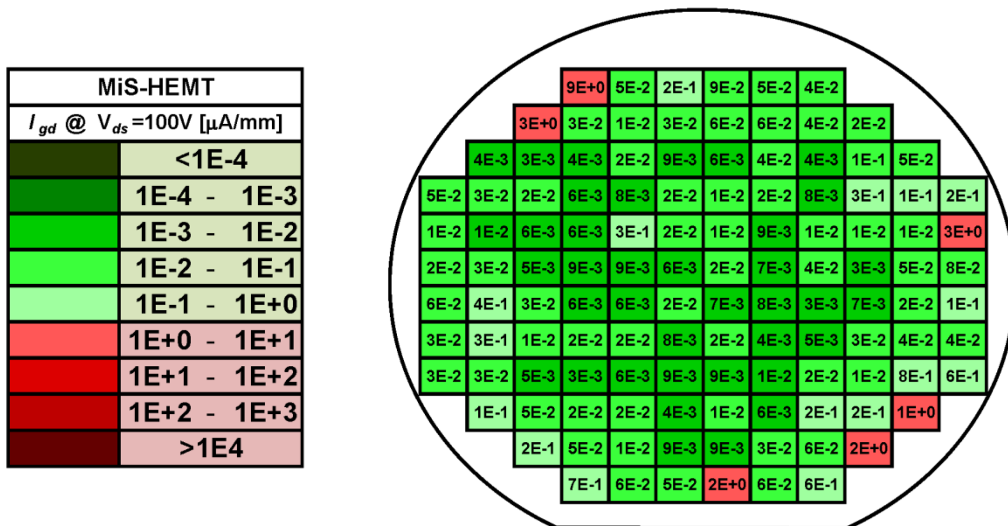

Figure 6-8. HfO_2 $MIS-HEMT$ **wafer scale map for the 2-terminal gate-drain current. The mean current obtained is 70** $\pm$ **13** nA/mm**.**

To further analyze the leakage of the low bias we have used two terminal wafer map up to $100\ V$. The gate-drain two terminal reverse current is presented in figure 6-8. Then, the introduction of the thin insulator has a marked of beneficial role in reducing the gate leakage current all over the wafer.

6.2.2. THIN IN-SITU GROWN Si_3N_4 POWER $AlGaN/GaN\ HEMT$

In-situ Si_3N_4 deposition on $AlGaN/GaN\ HEMT$ structures was recently shown to be feasible and advantageous mainly due to reduced $AlGaN$ relaxation, increased n_s, improved Ohmic contacts and surface protection during processing.[13-16]

For in-situ Si_3N_4 $MIS-HEMT$ (sample $E08$), focus had been put on the device reproducibility where 4 $inch$ wafer-scale DC parametric mapping revealed minimal dispersion and remarkable stability of the $MIS-HEMTs$ electrical parameters across the wafer. The Si_3N_4 isolated gate also allows operation at larger positive gate bias voltages and hence, reduces the on-resistance and increases the saturation current.

6.2.2.1. DC CHARACTERIZATION ($On-state$)

Figure 6-9 shows $On-state$ results for in-situ Si_3N_4 $MIS-HEMT$. For the gate and drain leakage currents are significant lower than 100 nA/mm. The threshold voltage is around $-7.0\ V$ and the relation on/off is of more of 6 orders of magnitude. The transconductance peak ($g_{m,max}$) is in the order of 80 mS/mm.

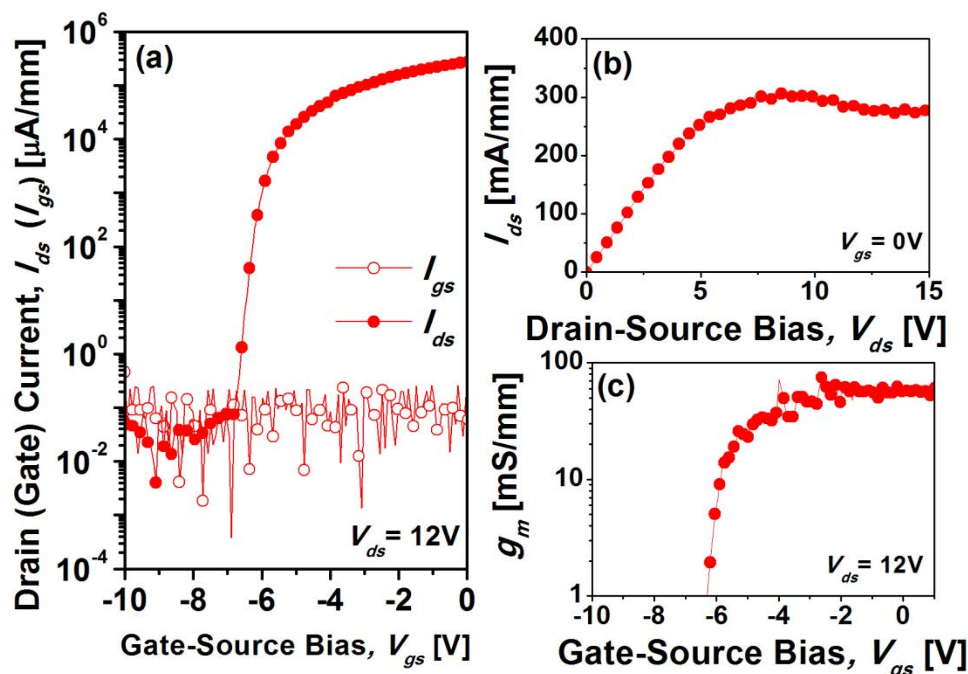

Figure 6-9. Typical in-situ Si_3N_4 $MIS-HEMT$ (a) transfer curve showing the reduced gate and drain currents. (b) $I-V$ forward curve and (c) transconductance comparison extracted from the derivative of the transfer curve.

6.2.2.2. DC CHARACTERIZATION $(Off - state)$

As shown in figure 6-10, the typical drain/gate reverse current characteristic showed a saturation of the breakdown voltage for $V_B \sim 900\ V$ $(L_{gd} > 8 - 10\ \mu m)$ and $V_B > 600\ V$ for gate-drain distance of $L_{gd} > 5\ \mu m$. The drain and gate leakage current was below $1\ \mu A/mm$ at $600\ V$.

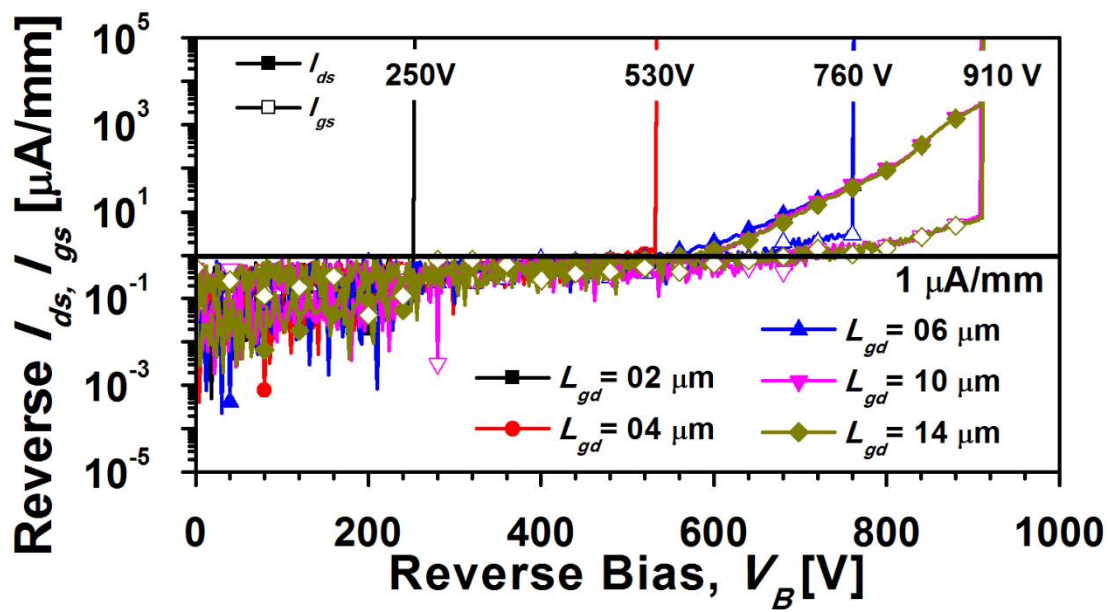

Figure 6-10. In-situ Si_3N_4 $MIS - HEMT$ typical drain/gate current reverse characteristic showing the saturation of the breakdown voltage for $V_B \sim 900\ V$ and $V_B > 600\ V$ for gate-drain distance of $L_{gd} = 5\ \mu m$. Gate and drain leakage current is maintained in any case below $1\ \mu A/mm$ at $V_{ds} = 600\ V$.

The extracted specific on-resistance was found to be very stable across the wafer with $R_{on,sp} = 2.5 \pm 0.3\ m\Omega cm^2$ at $V_{gs} = 0\ V$. We believe that the relatively large value of the specific on-resistance is linked with the $CMOS$ compatible $gold - free$ technology.

6.2.2.3. HIGH-CURRENT $HEMTs$

In spite of this slightly large value of the $R_{on,sp}$ $gold - free$ large area $HEMTs$ exhibited a large $On - state$ forward current as shown in figure 6-11 (a). The $gold - free$ contact solution did not affect the leakage current behavior where it was found to be remarkably low, less than $1\ \mu A/mm$ up to $600\ V$ as shown in figure 6-11 (b).

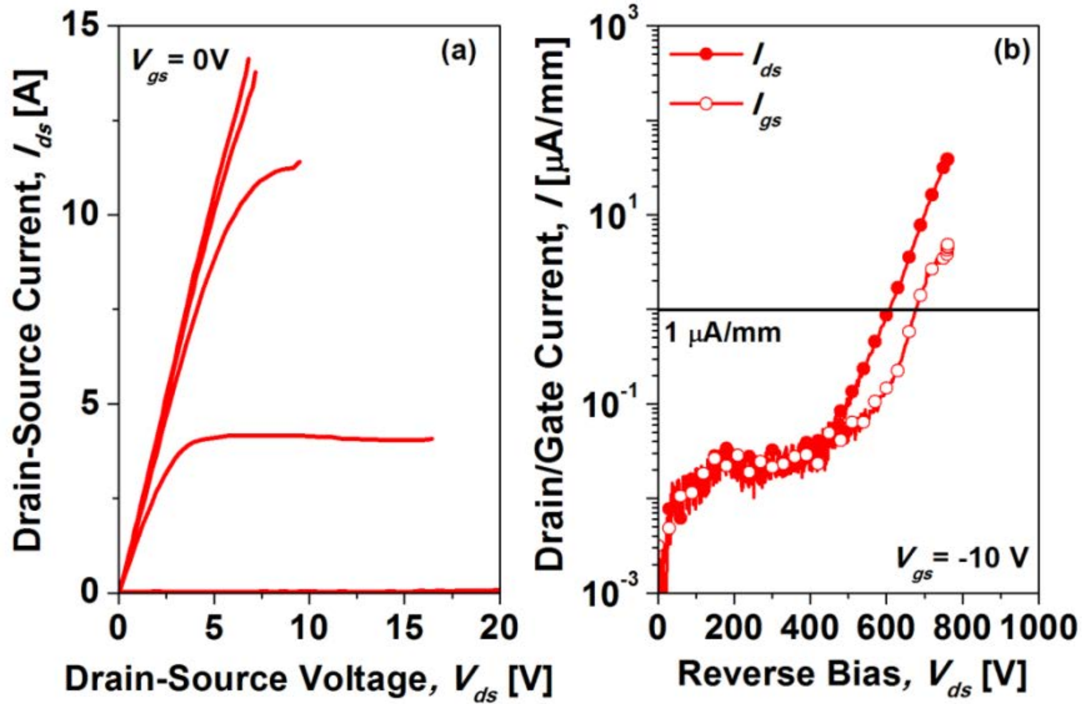

Figure 6-11. In-situ Si_3N_4 $MIS-HEMT$ (a) Output DC characteristics of a large area $AlGaN/GaN$ $HEMT$ ($W = 31\ mm$). A thicker second metal level was deposited on top of the $gold-free$ Ohmic contacts. (b) Reverse characteristics (substrate floating) of the device showing leakage currents below 1 $\mu A/mm$ up to 600 V.

6.2.2.4. POSITIVE GATE BIAS

The thin in-situ deposited $Si_3N_4-based$ MIS approach also results in improved gate stability under large positive gate bias. The Schottky injection is mitigated when the thin insulator is introduced, with negligible gate-source current flow with a forward $I-V$ sweep up to $V_{gs} = 9\ V$. As shown in figure 6-12, irreversible device degradation (gate dielectric damage) was observed to occur at $V_{gs} = 13-14\ V$. Both the saturation current and specific on-resistance are significantly enhanced when they are measured at a large positive gate bias. At $V_{gs} = 9\ V$ the $R_{on,sp}$ value drops to $R_{on,sp} = 1.9 \pm 0.3\ m\Omega cm^2$ (wafer maps are presented in the next section). In the same sense, the maximum saturation current (which was found to be very uniform across a wafer with $I_{ds,sat} = 296 \pm 33\ mA/mm$ measured at $V_{gs} = 0\ V$) increased significantly to $I_{ds,sat} = 603 \pm 44\ mA/mm$ at $V_{gs} = 9\ V$.

Figure 6-12. In-situ Si_3N_4 $MIS-HEMT$ (a) Typical forward $I-V$ drain-source current for gate bias up to $V_{gs}=+14\,V$. (b) Gate-source current during the same bias. It was observed negligible gate current up to $V_{gs}=+9\,V$ and the device gate degradation was observed at $V_{gs}=+13\,V$.

6.2.2.5. 4 *inch* WAFER MAPPING

For the in-situ Si_3N_4 $MIS-HEMT$, extensive DC forward characterization was performed at wafer scale, in terms of $R_{on,sp}$, V_{th}, reverse-biased gate and drain reverse currents at $V_{ds}=100\,V$. Figure 6-13 presents the $R_{on,sp}$ mapping which the mean value around $2.5\pm0.3\,m\Omega cm^2$.

Figure 6-13. In-situ Si_3N_4 $MIS-HEMT$ wafer mapping for $R_{on,sp}$ at $V_{ds}=1\,V$. $R_{on,sp}$ has been determined by means of $I_{ds}-V_{ds}$ curve for $V_g=0\,V$. The mean value and the dispersion was determined from the data statics to be $R_{on,sp}=2.5\pm0.3\,m\Omega cm^2$.

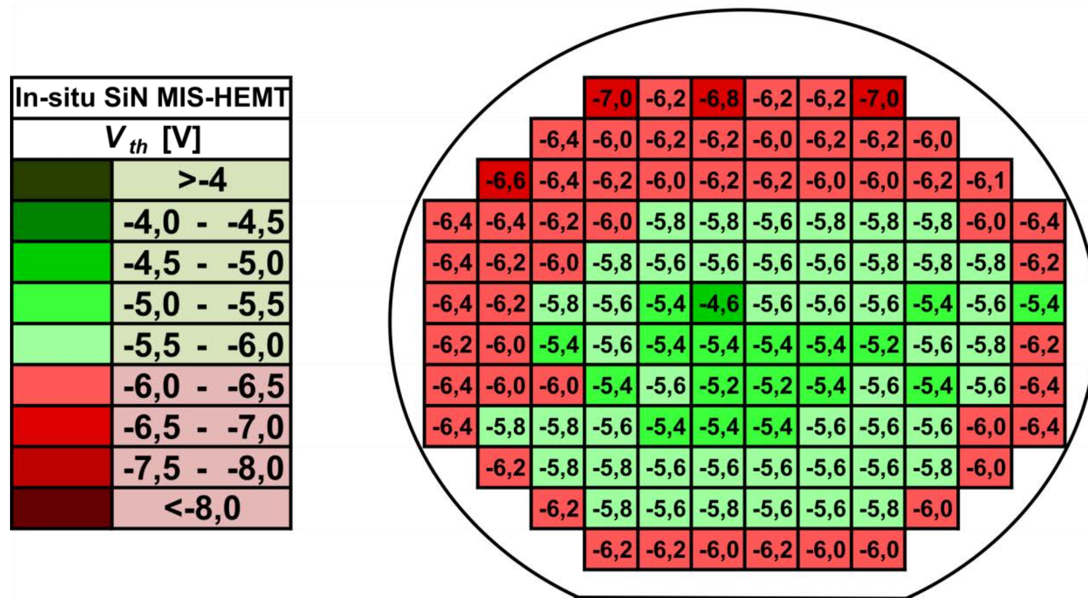

Figure 6-14. In-situ Si_3N_4 $MIS-HEMT$ wafer mapping for V_{th} has been determined by means of extract the gate voltage that corresponds to $I_{ds} = 1.0 \times 10^{-6}\ \mu A/mm$ of the $I_{ds} - V_{gs}$ curve. The dispersion is remarkably low.

When full wafer transfer curve maps were produced the threshold voltage value was found to be very homogeneous across the full wafer (figure 6-14). The average obtained for the population of devices was $V_{th} = -5.8 \pm 0.3\ V$. Again, this indicated the good homogeneity of the epitaxial material with in-situ Si_3N_4 deposition.

The introduction of the thin insulator has a marked beneficial role in reducing the gate and drain leakage currents all over the wafer. Figure 6-15 and figure 6-16 present the wafer maps of the reverse-biased gate and drain reverse currents at $V_{ds} = 100\ V$.

The yield of devices exhibiting currents lower than $1\ \mu A/mm$ at $V_{ds} = 100\ V$ was as high as 99%. The drain leakage current was in the range of $2 - 50\ nA/mm$. In the same sense the reverse gate current wafer map showed a yield of 95% for yield criteria of $I_{gs} < 1\ \mu A/mm$ at $V_{ds} = 100\ V$. The gate leakage current for these devices was in the range of $4 - 50\ nA/mm$. It is worth noting that only six devices on the wafer periphery exhibited a high-gate leakage current which is an indication of the homogeneity of the in-situ Si_3N_4 passivation and the process uniformity.

In-situ SiN MIS-HEMT	
I_{ds} @ V_{ds}=100V [µA/mm]	
	$<10^{-4}$
	10^{-4} - 10^{-3}
	10^{-3} - 10^{-2}
	10^{-2} - 10^{-1}
	10^{-1} - 10^{+0}
	10^{+0} - 10^{+1}
	10^{+1} - 10^{+2}
	10^{+2} - 10^{+3}
	$>10^{+3}$

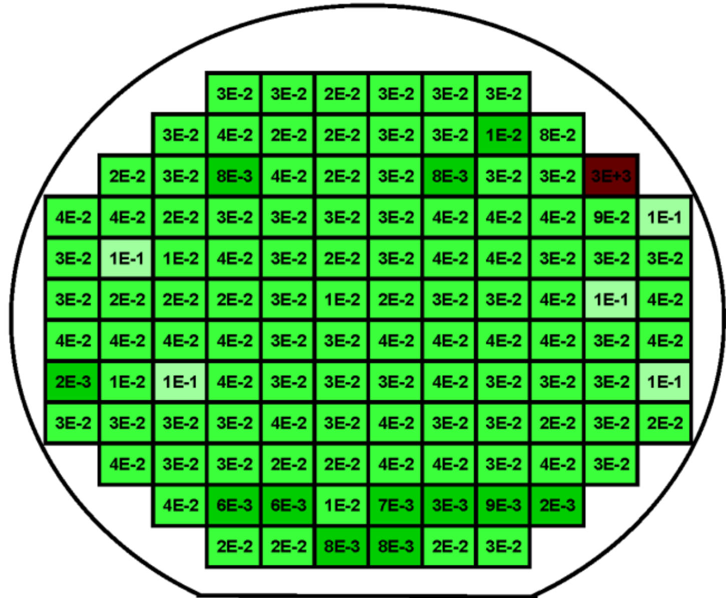

Figure 6-15. In-situ Si_3N_4 $MIS-HEMT$ wafer mapping for reverse drain current ($V_{ds}=100\ V$) with $L_{gs}=L_g=3\ \mu m$ and $L_{gd}=8\ \mu m$ measured at $V_{gs}=-10\ V$. The yield of devices at $V_{ds}=100\ V$ with leakage currents lower than $1\ \mu A/mm$ was as high as 99%. The drain leakage current for these devices was in the range of $2-50\ nA/mm$.

In-situ SiN MIS-HEMT	
I_{gs} @ V_{ds}=100V [µA/mm]	
	$<10^{-4}$
	10^{-4} - 10^{-3}
	10^{-3} - 10^{-2}
	10^{-2} - 10^{-1}
	10^{-1} - 10^{+0}
	10^{+0} - 10^{+1}
	10^{+1} - 10^{+2}
	10^{+2} - 10^{+3}
	$>10^{+3}$

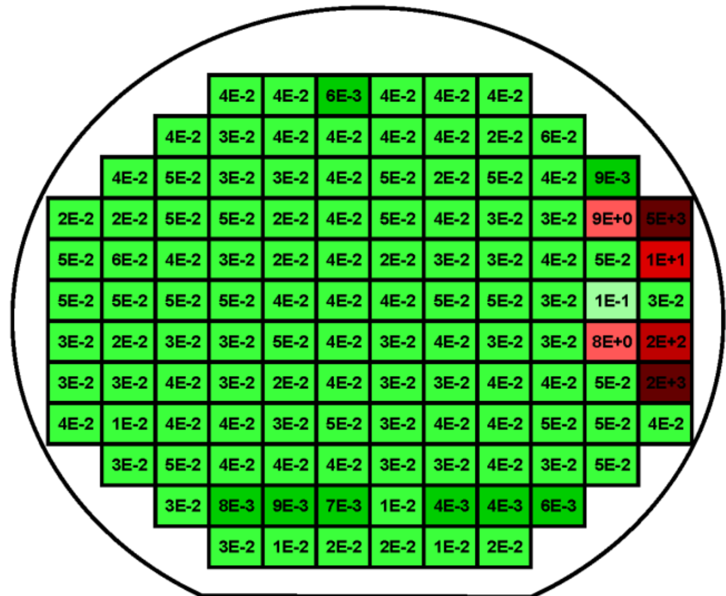

Figure 6-16. In-situ Si_3N_4 $MIS-HEMT$ wafer mapping for reverse-bias gate current ($V_{ds}=100\ V$) with $L_{gs}=L_g=3\ \mu m$ and $L_{gd}=8\ \mu m$ measured at $V_{gs}=-10\ V$. The yield at $I_{gs}<1\ \mu A/mm$ at $V_{ds}=100\ V$ in this case is 95%. The gate leakage current for these devices was in the range of $4-50\ nA/mm$. Only six devices on the wafer periphery exhibited a high-gate leakage current which is an indication of the homogeneity and robustness of the in-situ Si_3N_4 passivation.

6.3. TRADE OFF V_B vs $R_{on,sp}$

The remarkable material proprieties of GaN and AlN, such as WBG and high-critical electric field, make these semiconductors and (their alloys) very interesting for the basis of a new generation of more efficient power devices. Besides, a large conduction band discontinuity together with the presence of polarizations fields on GaN based heterojunctions allow a large $2DEG$ concentration to be confined. This results in $HEMTs$ offering a virtually unbeatable specific on-resistance vs breakdown voltage trade-off.[1,2,17-19]

The figure of merit (FOM) that measures the performance of a power device is the product of R_{on} and gate charge at a given breakdown voltage. The $R_{on,sp}$ is defined as the product of the on-resistance and the area of the device ($R_{on} \times Area$). FOM from Baliga[20] ($BFOM$) for a vertical device structure with a uniform doping profile that defines the intrinsic limit of a power semiconductor expressed by:

$$\frac{V_B^2}{R_{on,sp}} = \frac{\varepsilon_r \mu_n E_{crit}^3}{4} \; [W/cm^2] \qquad (6\text{-}1)$$

Where μ_n is the electron mobility and E_{crit} is the critical electrical breakdown electric field. The GaN $HEMT$, as a lateral device, has different properties: the conductive channel is a two-dimensional charge, and this $2DEG$ is not related to any doping in the material. From Zhang thesis dissertation,[21] the GaN $HEMT$ power device FOM can be expressed by:

$$\frac{V_B^2}{R_{on,sp}} = \theta \mu_n E_{crit}\left(E_{crit}^2 - E_p^2\right) \; [W/cm^2] \qquad (6\text{-}2)$$

Where θ is a constant with a unit of $[F/cm]$ and E_p is the polarization field in the $AlGaN$. The specific on-resistance of GaN $HEMTs$ is about 50 times lower than that of SiC devices for the same breakdown voltage, that is to say, the power device FOM is 50 times larger.[21] Figure 6-17 show the semiconductor limits explained above and the most recently literature and our obtained results.

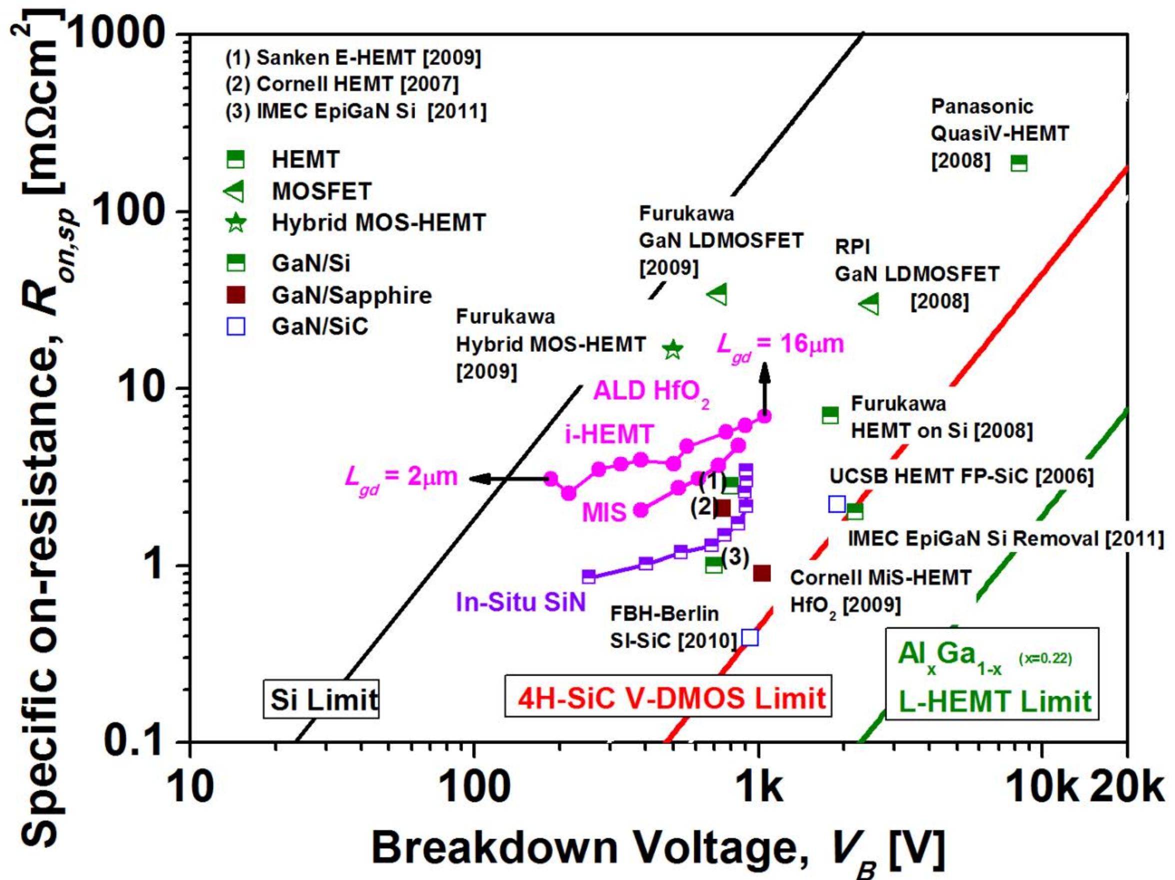

Figure 6-17. Fabricated $HEMTs$, $MOSFET$ and hybrid $MOS-HEMTs$ based in $GaN-on-Si$, on $sapphire$ and on SiC in terms of $R_{on,sp}$ vs V_B from recently literature and our obtained results.

The fabrication process was shown to be stable with a large number of devices showing excellent $On-state$ characteristics and breakdown voltages $V_B > 750$ V for gate-drain length over $L_{gd} = 10\ \mu m$. The specific on-resistance is extracted at $V_{gs} = 0\ V$. The Ohmic contact area was included in the device pitch calculation and pads areas were excluded from the device area calculation.

The fact of having lager $R_{on,sp}$ for the HfO_2 devices are due to several reasons: (i) the higher R_{sh} of the $2DEG$ for the first vendor and (ii) the high R_c when the HfO_2 is being removed from the contact area. HfO_2 is in fact difficult to remove from the contact area this being a possible reason of the higher contact resistance due to the persistence of ultra-thin HfO_2 beneath the Ohmic stack.

Figure 6-17 shows the specific on-resistance vs breakdown voltage state-of-the-art comparison. Figure 6-18 presents a comparison of $GaN\ HEMT$ fabrication with a $CMOS$ compatible $gold-free$ process.

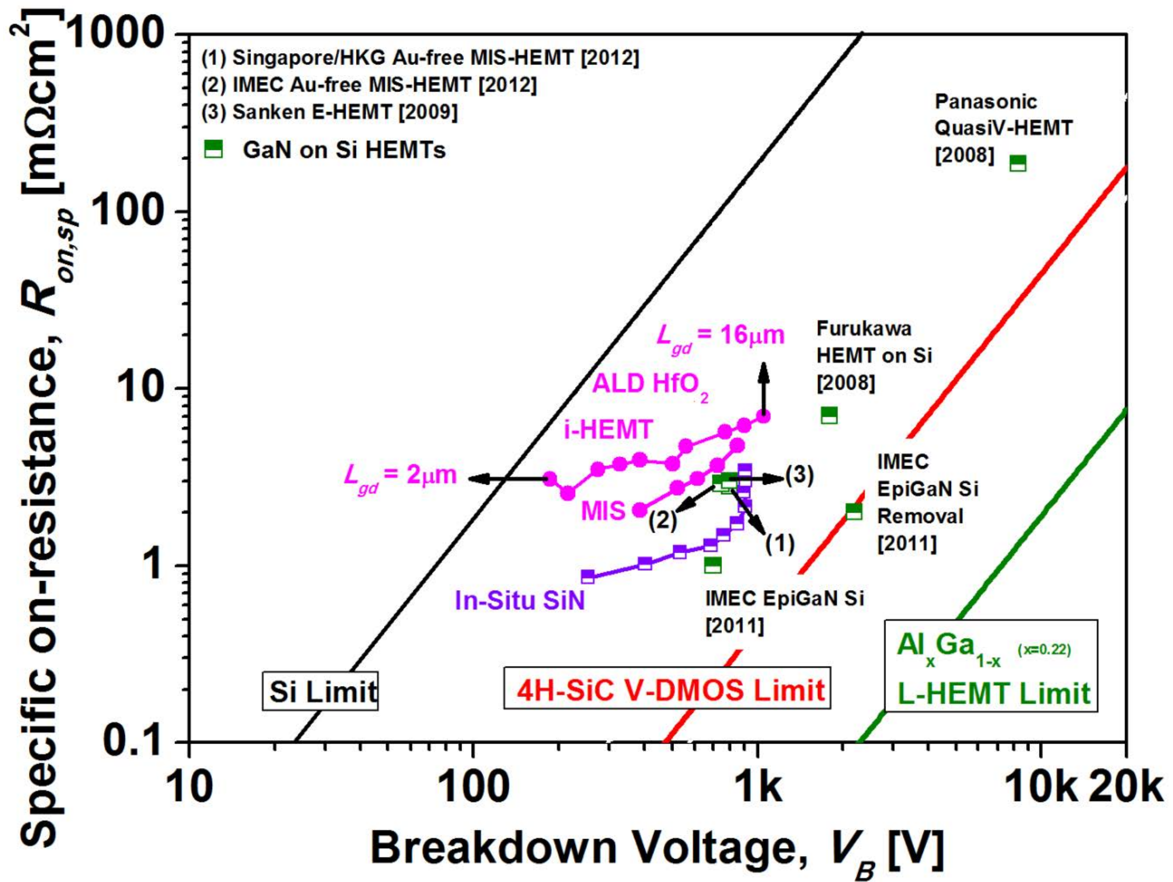

Figure 6-18. Fabricated $HEMTs$ based in $GaN-on-Si$ in terms of $R_{on,sp}\ vs\ V_B$ from recently literature results. (No-$CMOS$ lines and $gold-free$ process results.)

There, two main results have been included as a main reference for our $GaN\ gold-free$ devices, Van Hove *et al.*[22] ($IMEC$) and Liu *et al.*[23] ($Singapore/HKG$). Our results are in the state-of-the-art.

6.4. HIGH TEMPERATURE BEHAVIOR

As mentioned before, GaN power devices can work correctly at temperature higher than $300\ ℃$. However, as the temperature increases the $On-state$ and $Off-state$ currents of $AlGaN/GaN$ heterojunction transistors are, in general, severely degraded. Besides, the effective channel temperature (always higher than the bulk temperature due to the self-heating effect) also depends on how the different bulk materials dissipate the heat. In this section, it is exploratively presented the elevated temperature impact on the forward and the reverse leakage currents for analogous $HEMTs$ grown on different substrates: Si, $sapphire$ and $FS-GaN$. In this sense, it is necessary to evaluate the device performance at elevated temperatures ($25-310$ ℃) to provide reliable transistors

for demanding applications. This includes the achievement of low leakage currents when the transistor is in $Off-state$ to minimize losses. In addition, it have been investigated the impact of the high-temperature on the reverse leakage currents I_{gs}, I_{ds} and I_{db} of an $AlGaN/GaN\ HEMT$.

6.4.1. $On-state$

In this section, the bulk temperature impact is evaluated for three $identical\ AlGaN/GaN\ HEMTs$ grown on different commercial substrates. Three different substrates, as shown in figure 6-19, ($C01$, $C04$ and $C05$ respectively) namely Si,[1] $sapphire$[17] and $FS-GaN$,[24,25] where an $AlGaN/GaN\ HEMT$ has been defined.[26,27] It had also been investigated the thermal impedance (R_{th}) of the different substrates layers to evaluate the $On-state$ current reduction with temperature.

Since the nitride substrates are still under development as well as being very expensive, commercial $GaN-based$ devices are grown typically on $sapphire$, SiC or Si substrates. Among these, GaN epilayers grown on Si substrates offer a lower cost technology compared to the other substrates as well as allowing material growth on large diameter substrates up to 200 mm.[1] Nevertheless, the growth of GaN layers on Si is still challenging and these precarious growth conditions result in $GaN-on-Si\ HEMT$ devices which are still vulnerable to parasitic currents. The high-temperature can accelerate this thermal degradation, as more carriers are thermally injected over the barriers particularly from the Si substrate.

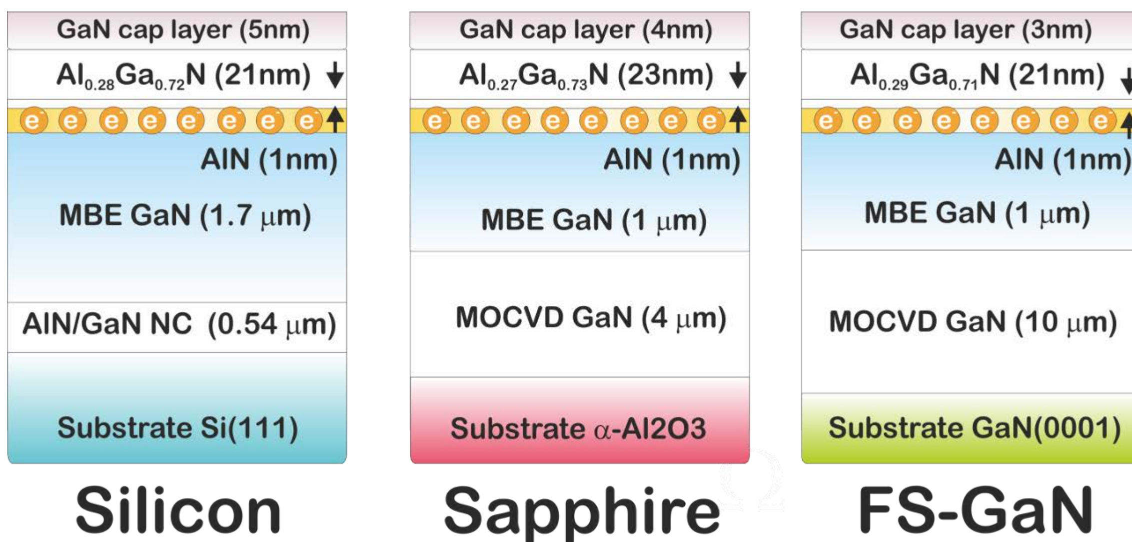

Figure 6-19. Cross-sectional description of the fabricated $HEMTs$.

On the other hand, $GaN-on-sapphire$ exhibits an interesting trade-off between the currently expensive SiC substrates and Si but with much better epitaxial matching, as well as a naturally insulating substrate.[17,28]

In any case, a high-quality $2DEG$ was formed in the $AlGaN/GaN$ heterojunction. The R_{sh}, the n_s and the μ_n were obtained via $Hall$ measurements. Table 6-1 summarizes the main $2DEG$ parameters.

$HEMT\ substrate$	$R_{sh}\ [\Omega/sq]$	$n_s\ [cm^{-2}]$	$\mu_n\ [cm^2/Vs]$
Si	350	9.6×10^{12}	1980
$Sapphire$	328	8.8×10^{12}	2163
$FS-GaN$	270	1.1×10^{12}	2110

Table 6-1. Summary of obtained results.

The temperature has a well know detrimental effect on the carrier mobility, as several scattering phenomena (in particular those related with phonons) increase with the temperature.[9] This, in turn, implies a reduction of the $On-state$ current of the device with temperature as shown in figure 6-20 and figure 6-21. Also well-known is the strongest temperature dependence of the $HEMT-on-sapphire$ due to the Al_2O_3 substrate lower thermal conductivity[10] (figure 6-20 (b)).

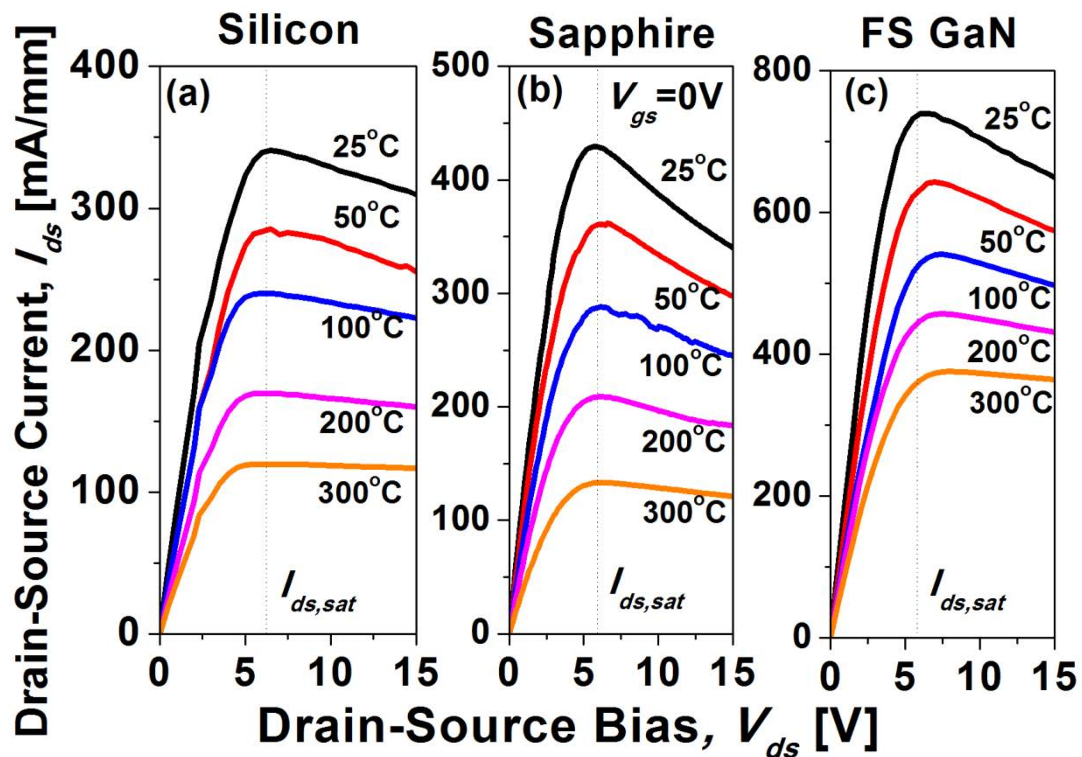

Figure 6-20. $AlGaN/GaN$ $HEMT$ **forward drain current** *vs* **drain voltage (at** $V_{gs}=0\ V$**) at varying temperatures for the** $HEMT$ **transistor, (a) on** Si**, (b) on** $sapphire$**, and (c) on** $FS-GaN$**.**

The temperature coefficient (figure 6-22) is an effective way of describing the temperature impact on the main parameters of the transistor, such as the on-resistance ($R_{on} = R_{on,0}\,T^{\alpha}$), the saturation current ($I_{ds,sat} = I_{ds,sat,0}\,T^{\alpha}$) or the maximum transconductance $g_{m,max} = g_{m,max,0}\,T^{\alpha}$).[6-8] In the temperature range of typical applications (25– 300 °C), the simple power law approximation appears to be sufficiently accurate. In this temperature range, the n_s is generally considered as virtually temperature independent.[9]

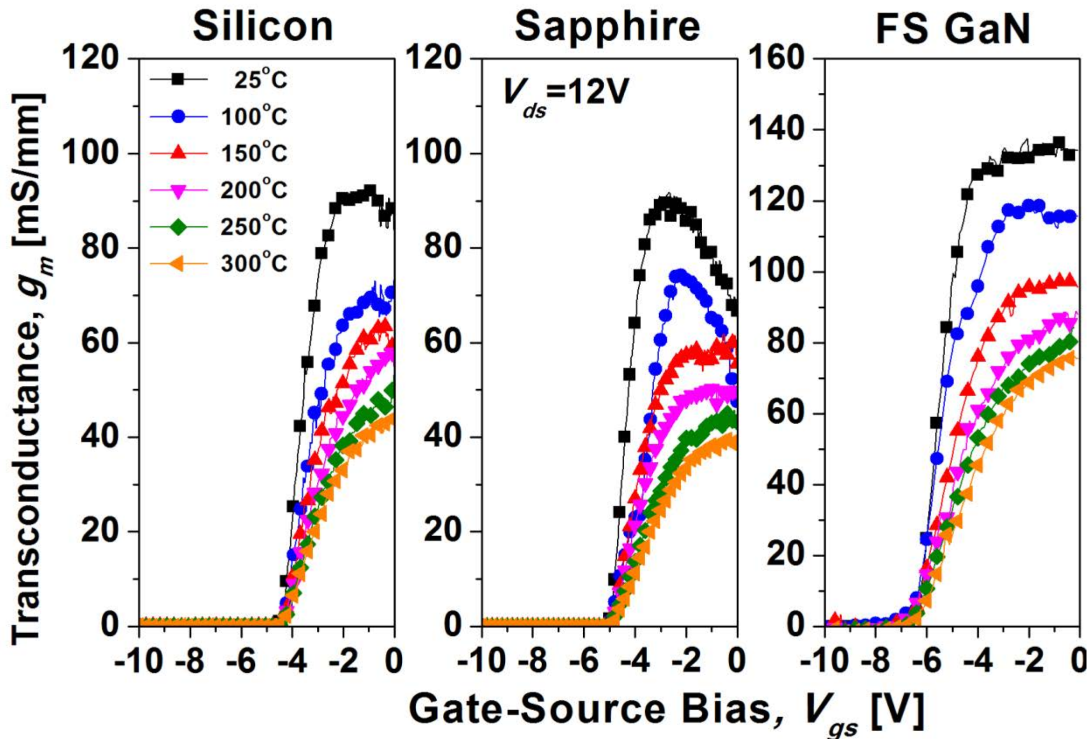

Figure 6-21. $AlGaN/GaN$ $HEMT$ saturation drain transconductance *vs* gate voltage (at $V_{ds} = 12\ V$) at varying temperatures for the $HEMT$ transistor, (a) on Si, (b) on $sapphire$, and (c) on $FS - GaN$.

This is due to the weak dependence of the polarization fields on the temperature, which results in an exceptional stability of the $HEMT$ threshold voltage with temperature (figure 6-22 (d)). The typical temperature coefficients (α) obtained for the three types of $HEMTs$ are present in table 6-2.

$HEMT\ substrate$	$\alpha(R_{on})$	$\alpha(I_{ds,sat})$	$\alpha(g_{m,max})$
Si	1.33	−1.53	−1.08
$Sapphire$	1.83	−1.78	−1.33
$FS - GaN$	1.29	−1.48	−0.99

Table 6-2. Summary of obtained temperature coefficients.

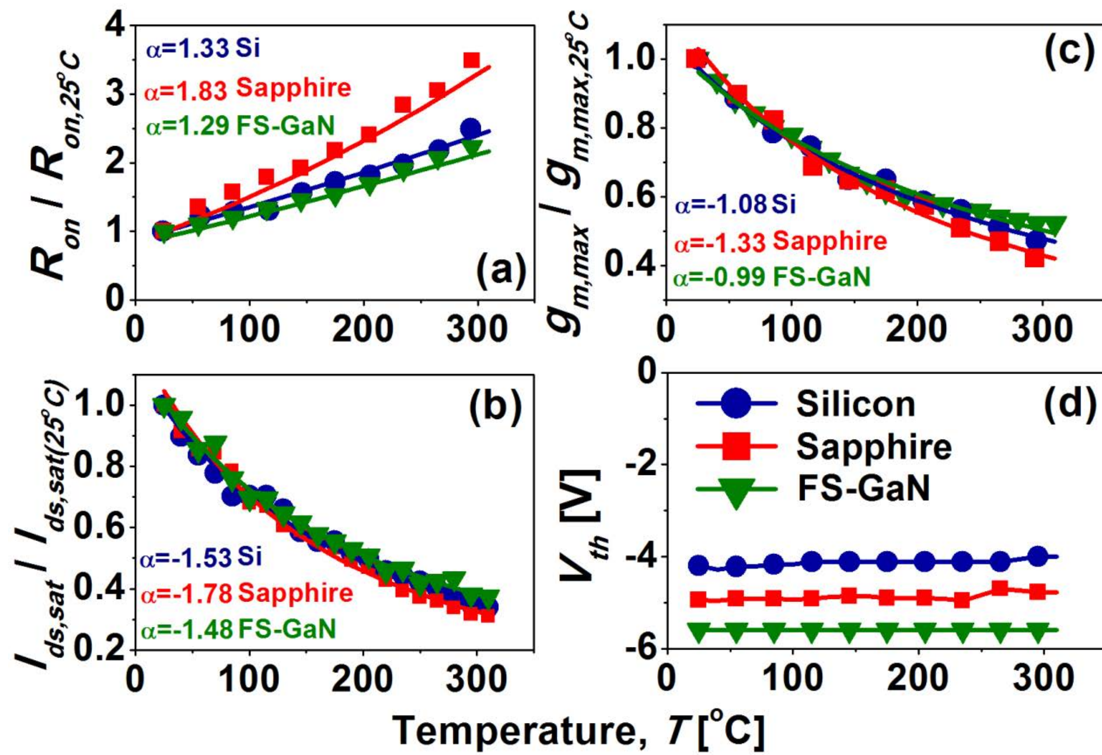

Figure 6-22. $HEMT$ **forward current temperature dependence for (a) on-resistance, (b) saturation current and (c) maximum transconductance. From these temperature dependences, the temperature coefficient (T^{α}) can be evaluated. (d) Temperature stability of the threshold voltage.**

The Si and $FS-GaN$ coefficients appear to be somehow similar. Nevertheless, it was determined a slightly better temperature behavior (more stable with temperature) for the $HEMT-on-FS-GaN$.

The temperature coefficient values are in agreement with previously reported α for $HEMTs-on-Si$[6-8] and $HEMT-on-sapphire$.[29] However, it is worth mentioning that *Tan et al.*[6] have reported remarkably smaller α (~ 0.5– 0.7) when the channel length is reduced to the submicronic scale. In our case the channel lengths were $L_g = 2-4\ \mu m$. The excellent threshold stability has also been reported to be lineal with reduced interfacial trapping phenomena.[29]

In contrast, the temperature coefficients of $FS-GaN$ $HEMTs$ are only very scarcely reported. Our results seem to indicate that, effectively, the GaN bulk exhibits better thermal conductivity than Si and/or the absence of thermal boundaries between different epilayers significantly favors the heat dissipation.

For further investigating this, we have adapted a dc method[30] for the estimation of the $HEMT$ thermal impedance. This method is based on the fact that the DC output characteristics may show a substantial drop in the saturation current (with increased drain voltage) and a negative differential resistance may appear ($\Delta I_{ds,sat}$). Due to the high-level of power handled by the $2DEG$, self-heating effects may become very relevant. Basically, the self-heating increases the channel temperature to an effective temperature T_{eff}.[10] This effective temperature depends on the dissipated power, the thermal resistance R_{th} and the substrate temperature, T_{sub} as:

$$T_{eff} = R_{th} I_{ds,sat} V_{ds} + T_{sub} \tag{6-3}$$

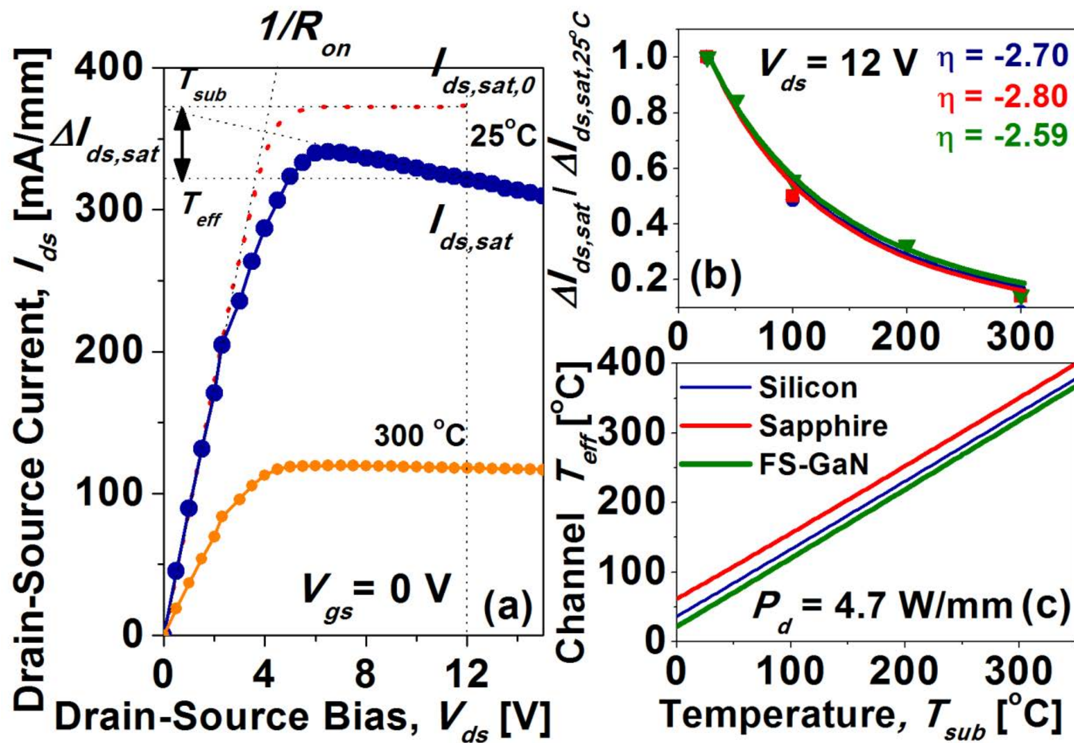

Figure 6-23. (a) $AlGaN/GaN\ HEMT-on-Si$ forward current ($V_{gs} = 0\ V$) where the definition of $\Delta I_{ds,sat}$ is shown. (b) $\Delta I_{ds,sat}$ dependence with the substrate temperature. (c) Computed channel temperature *vs* T_{sub} from the $\Delta I_{ds,sat}$ *vs* T_{sub} dependence.

Figure 6-23 (a) illustrates how the $I_{ds,sat}(T_{sub})$ is defined. $I_{ds,sat}(T_{sub})$ would be the extrapolation of the saturation drain current at $V_{ds} = 0\ V$ and $\Delta I_{ds,sat}$ is defined as $\Delta I_{ds,sat}(T_{sub}) = I_{ds,sat}(T_{eff}) - I_{ds,sat}(T_{sub})$. The red curve of figure 6-23 (a) is an idealization of the forward $I_{ds} - V_{ds}$ without taking into account self-heating effects, parasitic contact or drain/source resistances, leakage through the substrate, variation of the saturation drift velocity (Δv_{sat})[8,30] and any variation of the threshold voltage (ΔV_{th}).

If it is assumed power laws for $\Delta I_{ds,sat}$, ($\Delta I_{ds,sat}(T) = \Delta I_{ds,sat,0}T^{\eta}$), we can rewrite $\Delta I_{ds,sat}$ as $\Delta I_{ds,sat}(T_{sub}) = I_{ds,sat,0}\left(T_{eff}^{\alpha} - T_{sub}^{\alpha}\right)$ yielding:

$$T_{eff} = \left(T_{sub}^{\alpha} - \Gamma_1 T_{sub}^{\eta}\right)^{1/\alpha} \tag{6-4}$$

Where $\Gamma_1 = \Delta I_{ds,sat,0}/I_{ds,sat,0}$ or as a function of the $HEMT$ at 25 °C , $\Gamma_1 = T_0^{\alpha/\eta}(\Delta I_{ds,sat,25°C}/I_{ds,sat,25°C})$ ($T_0 = 300$ K) and hence:

$$R_{th} = \frac{T_0^{\alpha}}{I_{ds,sat,25°C}\,V_{ds}}\left(\frac{T_{eff} - T_{sub}}{T_{eff}^{\alpha}}\right) \tag{6-5}$$

Thermal resistances of $AlGaN/GaN\ HEMTs$ on different substrates (Si, $sapphire$, GaN, SiC and diamond) have already been investigated.[31-33] In particular, this topic has been investigated for the $AlGaN/GaN\ HEMT - on - SiC$ which is the most accepted substrate for RF applications (due its higher thermal conductivity k). A number of experimental techniques (including $\mu - Raman$, photocurrent or scanning thermal microscopy) have been utilized to measure the channel temperature.[34-36] Besides, finite difference simulations and analytical models have also been widely used to investigate the nature of heat flow within the $HEMT$ heterostructure.[37,38] Both, experimental and simulation approaches, have indicated that the materials with better k are the superior choice, due its improved heat dissipation.

However, there is a significant discrepancy of the values given for R_{th} in the literature. Defective substrate dislocations (in particular for $FS - GaN$ or diamond), the presence of nucleation layers, different active layer composition (GaN cap, $AlGaN$ thickness and Al content, GaN buffer doping and thickness) the different device layout (channel length, number of fingers and others), access or contact resistances may play a role. These differences make the comparison somewhat confusing. In particular, nucleation layers are considered as essential to accommodate the lattice mismatch between GaN and the substrate. This would give rise to an additional thermal boundary resistance (TBR) when heat is conducted across the heterostructure.[39-42] It have been used virtually identical active layers (GaN buffer, $AlGaN$ barrier and GaN cap), processing (identical Ohmic metal, i.e., contact resistance and Ni/Au gate metal) and device layout on the three substrates. Therefore, the differences on R_{th} would come solely from the substrate or nucleation layers.

For the computation of R_{th} is then required the determination of $\Delta I_{ds,sat}$ $(V_{ds} = 0\ V)$, and the corresponding $\Delta I_{ds,sat}$, for each bulk temperature γ was determined for several drain-source saturation voltages as shown in figure 6-23 (b). The parameters for a computation the R_{th} model are summarized in table 6-3.

$HEMT$	η	Γ at RT	T_{eff}[°C] at RT	R_{th}[°C/(W/mm)] $RT \rightarrow$ 300°C
Si	-2.70	123.7 $K^{\alpha/\eta}$	62.4	7.6 → 16.3
$sapphire$	-2.83	110.2 $K^{\alpha/\eta}$	86.7	12.9 → 31.0
$FS - GaN$	-2.65	75.6 $K^{\alpha/\eta}$	48.1	4.4 → 9.8

Table 6-3. Summary of parameters to computation of R_{th}.

Therefore, (as shown in figure 6-20), the negative differential resistance slope has a strong temperature dependence. For example, $\Delta I_{ds,sat}$ decreases from 130 mA/mm (25 °C) to 19 mA/mm (300 °C) for sapphire ($V_{ds} = 13\ V$). We choose for the evaluation of the thermal resistance a set of V_{ds} values ($15\ V, 13\ V$ and $6.5\ V$) which dissipated power ($P_d \sim 4.7\ W/mm$) was similar for the three substrates. The pitch of the $HEMT$ device (source-drain) is 9 μm (14 μm for Si) and the device W is 150 μm.

When compared with the literature, the values of T_{eff} and R_{th} extracted with the DC method appear to be somehow underestimated, with the thermal resistance of the $FS - GaN$ (4.4 °C/(W/mm)) in the order of the state-of-the-art $HEMT$ on diamond.[32] One partial explanation (a part of the questionable accuracy of the method) is the fact of dealing with conventional single finger $HEMTs$ with rather large length gates. Besides, parasitic resistances would significantly reduce the $I_{ds,sat}$ value. However, as mentioned before, $HEMTs$ are virtually identical on the three substrates and hence, this would affect in the same fashion the drain current, regardless the substrate.

More interesting are the experimental R_{th} ratios among the different substrates. The thermal resistance of the device grown on Si appears to be 1.67 times lower than on $sapphire$, which perfectly fits with the previous literature.[35] Normalizing R_{th} with respect to the $FS - GaN$ value (at RT), it was observed a factor of improvement of $\times$ 1.6 and $\times$ 2.7 compared to Si and $sapphire$, respectively. The effective temperature would depend mainly on the different k (substrate thermal conductivity) for a given power density and substrate thickness. The typical values of k for different substrates given in the literature are summarized in table 6-4.[38]

$Substrate$	$k\ [W/mK]$
Si	148
$sapphire$	35
GaN	160
SiC	400
$Diamond$	2200

Table 6-4. Summary of typical values of k for different substrates.

It is worth mentioning that, this value rises up to 400 W/mK for SiC, but the ultimate substrate is diamond, with the highest thermal conductivity of 2200 W/mK among materials. Device oriented polycrystalline diamond k is typically $3-4$ times[33] that of SiC, though. Normalizing the theoretical k values again to GaN, it would give factor of improvements of $\times$ 1.1 (Si) and $\times$ 4.6 ($sapphire$). Hence, the thermal behavior should be very similar for Si and $FS-GaN$, with the device on $sapphire$ being remarkably worse. Indeed, we observe the $HEMT-on-sapphire$ being the worst (but only to some extent) and the $FS-GaN$ being the most stable with T. In addition, there is a relevant difference between the thermal behavior of the device on $FS-GaN$ and Si.

We suggest that this important gap between Si and $FS-GaN$ would come from the nucleation layer TBR depicted in figure 6-19 for Si. It has been reported that optimized nucleation layers ($GaN-on-SiC$)[39-42] can reduce the channel T up to 40% or even more.[39] Other explanation would come from the fact that the GaN bulk thermal conductivity would be greater than what is currently generally accepted. Recently, it has been reported bulk GaN thermal conductivities larger than 260 W/mK[43] (the theoretical value for k would be as high as 410 W/mK),[44] which suggests the $FS-GaN$ an interesting alternative to the excellent (but otherwise prohibitively expensive yet) SiC substrates. In addition, the TBR additional resistance may be naturally mitigated.

6.4.2. $Off-state$

$GaN-based$ power switches are expected to play a key role in uncooled electronics at elevated temperatures. Nevertheless, the implication of the elevated temperature in the $Off-state$ device performances is not completely understood. In this section, it had been explored the leakage thermal activation mechanisms taking place in *analogous* $AlGaN/GaN$ $HEMT$ grown on Si and $sapphire$. This comparison reveals interesting facts such as the strong temperature dependence of the drain current on/off ratio or the different thermal activation energy ranges for Si, depending on temperature.

6.4.2.1. LEAKAGE CURRENT THERMAL ACTIVATION

The thermal activation energy provides valuable information of how a device performs at high-temperature. The temperature on/off ratio of a power electronic switch, for example, is a critical figure of merit for industrial applications such as power converters,[4] but it is broadly unknown. WBG semiconductors, such as GaN, are ideally suited for working at elevated temperatures since the large bandgap makes the intrinsic carrier concentration irrelevant for temperatures below 300 °C.[5] However, the electrons on the $2DEG$ of the $AlGaN/GaN\ HEMTs$ generally suffer from undesirable and persistent parasitic leakage. This occurs for a number of reasons, in particular the narrow and defective $AlGaN$ buffer layer, and the inhomogeneous nature of the Schottky gate contact with a number of leakage paths, with reduced Schottky barrier height.[45]

Therefore, in this section it had been investigated the temperature impact on the $AlGaN/GaN\ HEMT$' forward and leakage currents where the thermal activation pattern was also determined. A highly resistive GaN buffer layer is required to achieve low leakage $HEMT$ devices when biased in the $Off-state$. This is accomplished using the thick nucleation top AlN layer which is a barrier for electrons. On $sapphire$ substrates the growth of good quality highly resistive buffer is more difficult due the presence of oxygen diffusing from the substrate. The same AlN nucleation technique has not been replicated yet on $sapphire$ to have sufficient quality to act as an electron barrier. A solution consists in doping the GaN buffer layer with deep acceptors like iron, but such element was not available in the MBE growth reactor. For these reasons, the structure was regrown by MBE on an iron-doped $GaN-on-sapphire$ template obtained by $MOCVD$ following a procedure as described in literature.[46]

The device dimensions was $4/5/4\ \mu m$ for $L_{gs}/L_{gd}/\ L_g$ and $W = 150\ \mu m$. This very conventional layout has been chosen to avoid premature breakdown phenomena and to guarantee the constant electron mobility model to be valid. Temperature is well known to have a detrimental effect on the carrier mobility as several scattering phenomena (in particular those related to phonons) increase with the temperature.[9] This, in turn, implies a reduction of the $On-state$ current of the device with T as shown in the insets of figure 6-24 (a) and (b). Also well-known is the strong T dependence of the $HEMT-on-sapphire$ due to the low thermal conductivity of Al_2O_3 (figure 6-24 (b)).[10]

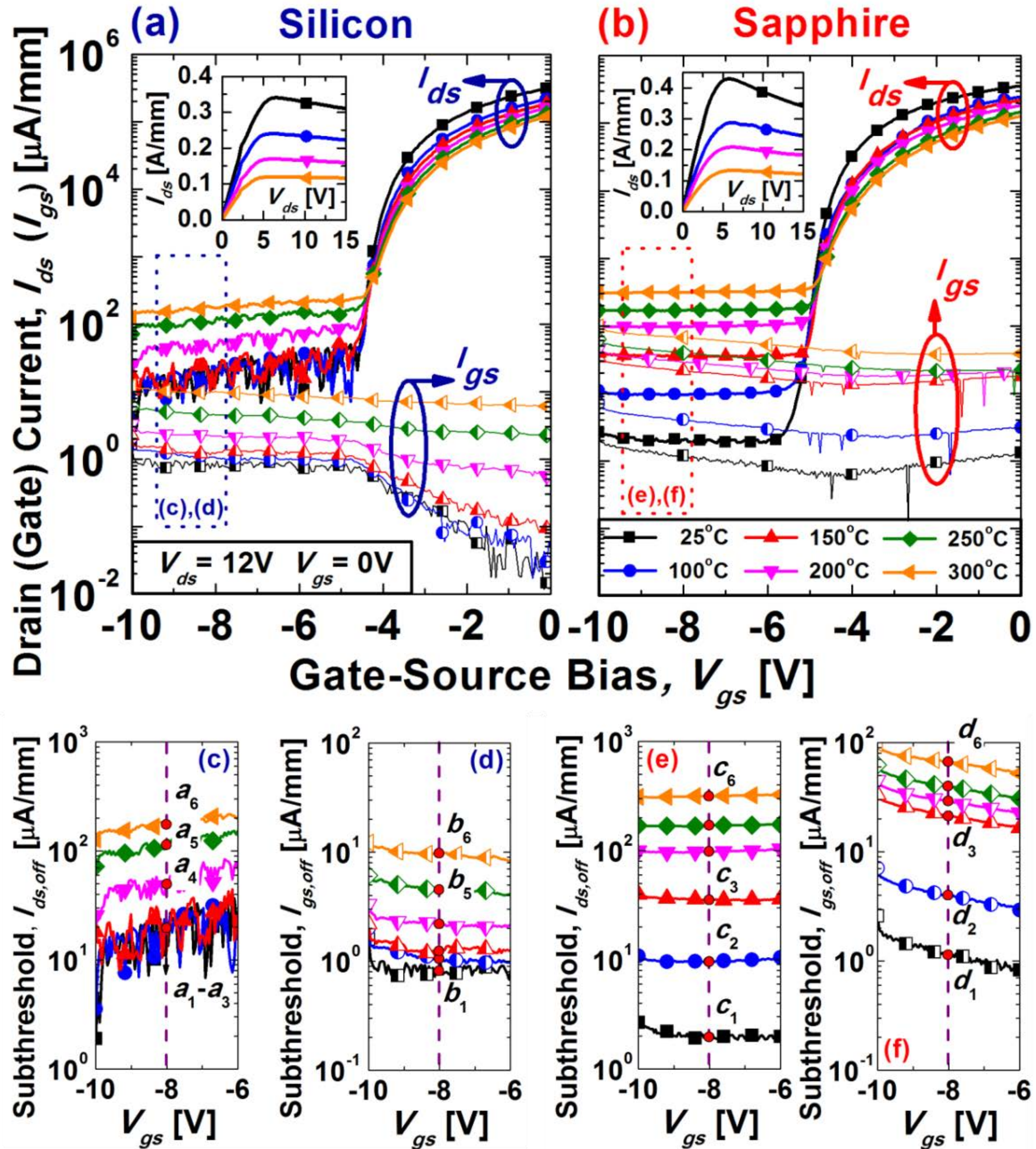

Figure 6-24. Transfer curve ($V_{ds} = 12\ V$) showing the drain and gate currents at varying T for a heterojunction transistor on Si (a) and on $sapphire$ (b). In the inset, forward $I_{ds} - V_{ds}$ for $V_{gs} = 0\ V$ at 25 ℃, 100 ℃, 200 ℃ and 300 ℃ for Si (a) and $sapphire$ (b). Detail of the transfer curve subthreshold currents (drain, $I_{ds,off}$ and gate, $I_{gs,off}$) for the Si (c), (d) and the $sapphire$ $HEMT$ (e), (f). a_1, a_2, a_3, a_4, a_5, a_6 refer to $I_{ds,off}$ ($V_{gs} = -8\ V$) at 25 ℃, 100 ℃, 150 ℃, 200 ℃, 250 ℃ and 300 ℃. Idem for $b_1 - b_6$, $c_1 - c_6$ and $d_1 - d_6$.

Regarding $I_{ds,sat}$ if we assume the constant electron mobility model, a linear relationship between mobility and saturation current can be obtained.[11,47] The temperature dependence of $I_{ds,sat}$ could be derived by the temperature dependence of the electron mobility, as in the case of the R_{on} (see $chapter\ III$).

The subthreshold gate and drain current increases with T (figure 6-24 (c)-(f)). In the case of the $HEMT-on-sapphire$ the subthreshold current increase is linear from room temperature up to 300 °C. For the $HEMT-on-Si$, two different temperature regimes were observed with a turning point at a temperature of about 150 °C. For the lower temperature range the gate and drain current only weakly depend on the temperature. For $T>150$ °C the temperature dependence is that expected from a trap assisted mechanism.[48] Figure 6-25 (a) and (b) show the activation energies ($V_{gs}=-8\,V, V_{ds}=12\,V$) assuming a rate-limited thermally activated process following an Arrhenius law ($I=I_0\exp(-E_a/k_BT)$),[49,50] where E_a is the activation energy and k_B is the Boltzmann constant. The thermal activation energy can be determined from the Arrhenius plot ($\ln I$ vs $1/T$).

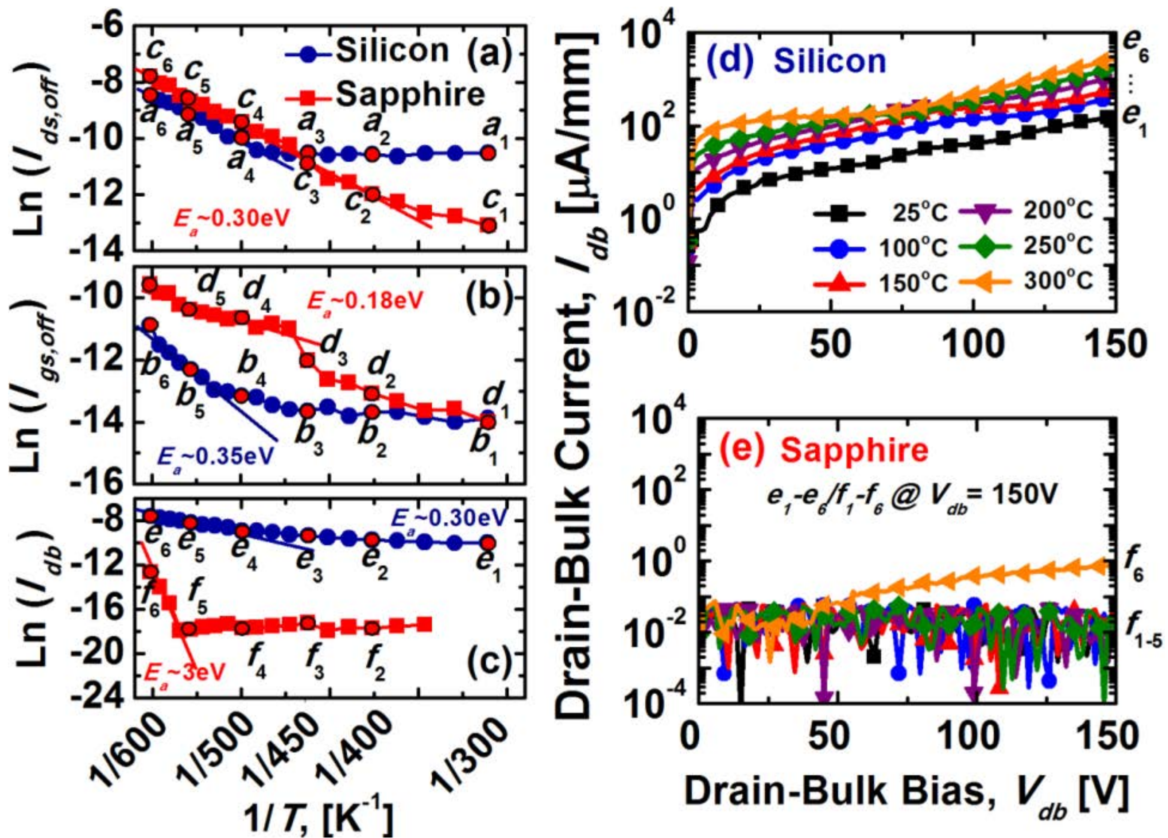

Figure 6-25. $HEMT-on-Si$ **or** $on-sapphire$ **Arrhenius plots for (a) the subthreshold drain current (**$I_{ds,off}$**) at** $V_{gs}=-8\,V$**, (b) the subthreshold gate current (**$I_{gs,off}$**) at** $V_{gs}=-8\,V$**, and (c) the vertical drain-bulk current (**I_{db}**) at** $V_{db}=150\,V$**. The reference currents** a_1-a_6**,** b_1-b_6**,** c_1-c_6 **and** d_1-d_6 **are defined in figure 6-24. Vertical drain-bulk current** vs V_{db} **at varying** T **for (d)** Si **and (e)** $sapphire$ **substrates. Vertical drain-bulk set-up is illustrated in figure 6-26 (b).** e_1-e_6 **and** f_1-f_6 **points illustrate the drain-bulk current at** $V_{db}=150\,V$ **for 25 °C, 100 °C, 150 °C, 200 °C, 250 °C and 300 °C for** Si **and** $sapphire$**, respectively.**

The subthreshold drain current $(I_{ds,off})$ E_a has been determined to be 0.30 eV for the $HEMT - on - sapphire$. On Si, E_a is remarkably smaller (0.02 eV) for $T < 150$ °C. Nevertheless, the thermal activation energy rises again up to 0.30 eV for larger temperatures. Therefore, it appears that for $T > 150$ °C, the drain leakage current temperature behavior is similar for the GaN buffer on Si and $sapphire$, which would be an indication of similar conduction mechanisms.

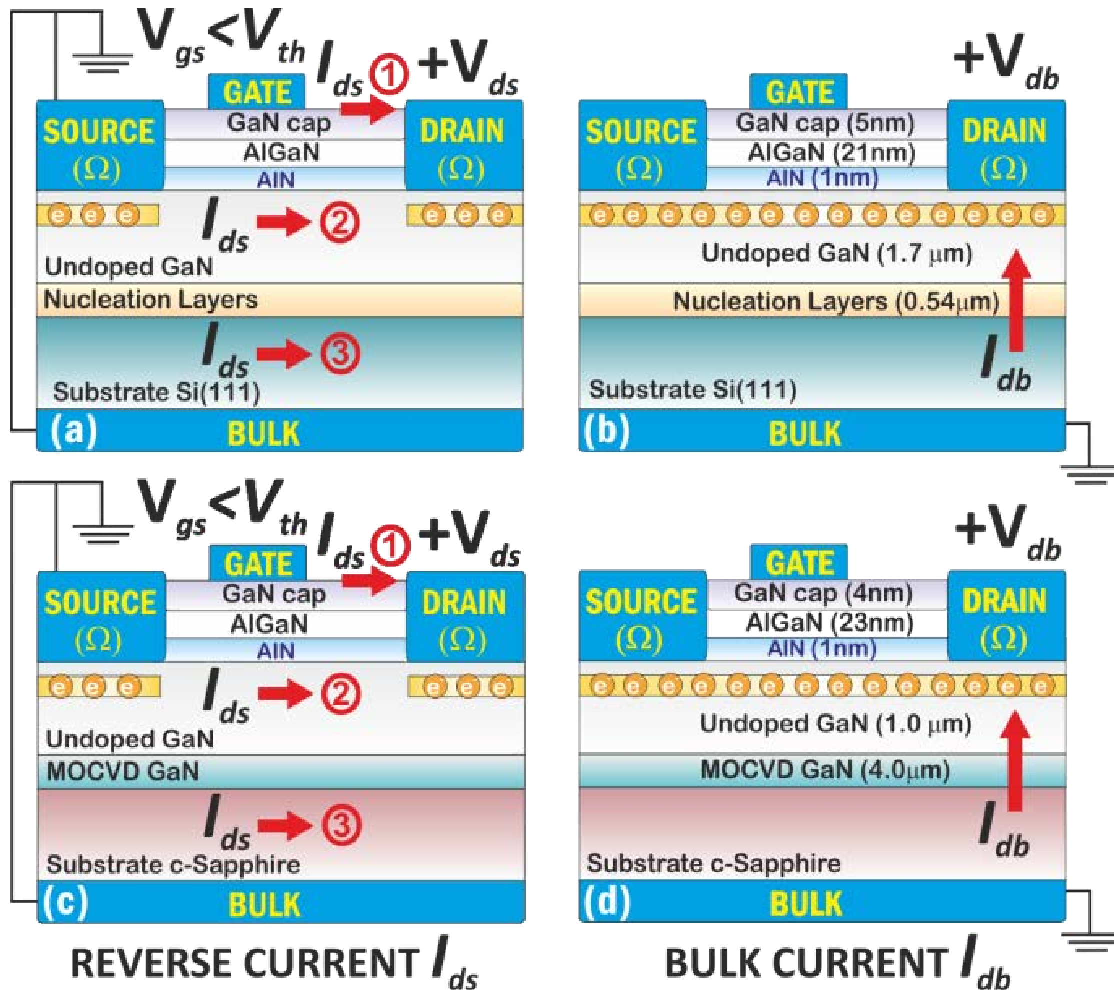

Figure 6-26. Cross-sectional view (not to scale) of the $HEMT$ on (a), (b) Si and (c), (d) $sapphire$. In (a) and (c) it is also shown the suggested drain leakage paths during a $HEMT$ reverse measurement. There the $2DEG$ is depleted $(V_{gs} < V_{th})$, the source grounded and the drain electrode positively biased. The substrate can also be grounded (our case) or floating. In (b) and (d) it is also shown the substrate (or bulk) current (I_{db}) which is the two terminals current between the drain and the grounded back of the wafer. Note that both reverse I_{ds} and I_{db} have been evaluated for the Si and $sapphire$ $HEMT$ at varying T.

It has been reported[2,51] that the reverse (or subthreshold) drain leakage (figure 6-26 (a)) for the $GaN-on-Si\ HEMTs$ is due to the injection of the electrons into the GaN buffer layer ($path$ 2 and $path$ 3 in figure 6-26 (a)) and the tunnelling leakage current of the Schottky-gate reverse bias ($path$ 1 in figure 6-26 (a)). The poor isolation of the GaN buffer and the Si substrate would be in the origin of the injection of carriers into the GaN buffer. Lu *et al.*[51] have suggested hole generation in the buffer and electron injection from the Si substrate into the buffer, which would eventually cause the reverse bias breakdown due to impact ionization. Therefore, the vertical drain-bulk current (figure 6-26 (b) and (d)), (substrate grounded and the drain positively biased), $I_{db} vs\ T$ has been evaluated for the $HEMT-on-Si$ and $sapphire$, (figure 6-25 (d) and (e)).

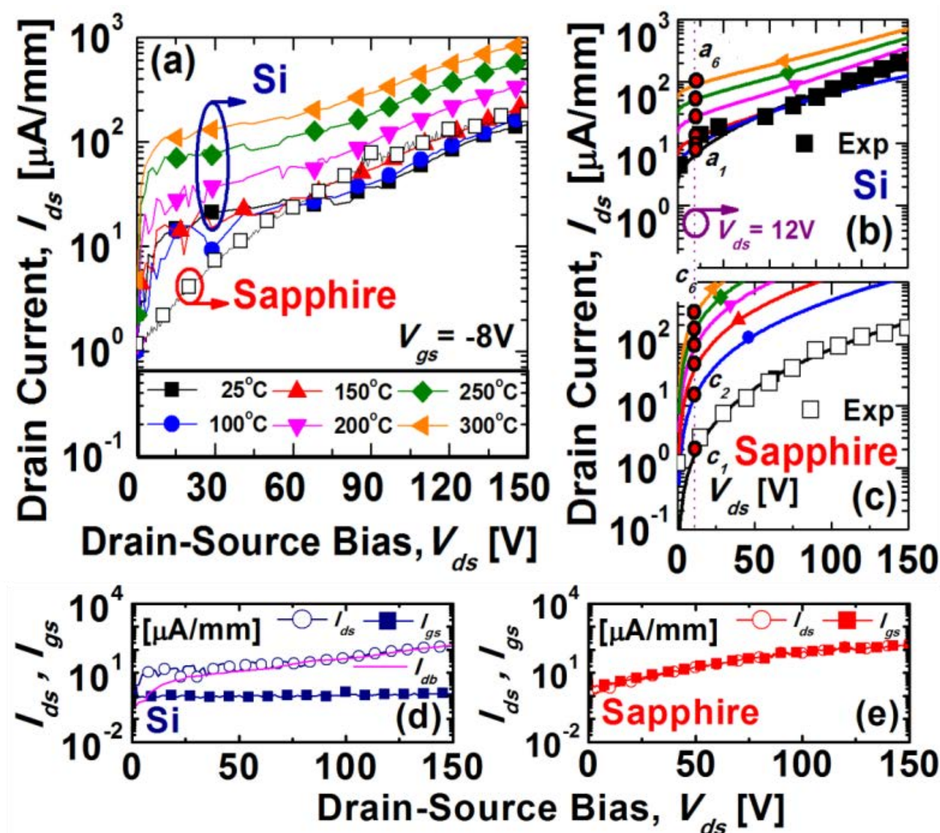

Figure 6-27. (a) Experimental $HEMT$ reverse current $I_{ds}\ vs\ T$ (see figure 6-26 for the definition of the set-up). (b) Simulated reverse $I_{ds}-V_{ds}\ vs\ T$ using the experimental activation energies for the $Si\ HEMT$. In this case we suggest a close fit with a combination of Schottky emission ($V_{ds} < 80\ V$) and $Poole-Frenkel$ ($V_{ds} > 80\ V$). (c) Simulated revers $I_{ds}-V_{ds}\ vs\ T$ using the experimental activation energies for the $sapphire\ HEMT$. In this case a simple $Poole-Frenkel$ approximation seems valid for almost the entire range of V_{ds} and T. a_1-a_6 and c_1-c_6 are defined in figure 6-24 being the transfer $I_{ds}-V_{gs}$ subthreshold current at $V_{ds}=12V$. (d) Si and (e) $sapphire\ HEMT$ reverse I_{ds} (open symbols) and I_{gs} (solid symbols) currents at 25 ℃. For Si the bulk current I_{db} is also plotted (solid line).

The insulating nature of the $sapphire$ substrate (figure 6-25 (e)) prevents the vertical current flow up to 250 °C (the resolution of our measurement set-up was of $\sim 10\ nA/mm$). Therefore, for the $HEMT-on-sapphire$, the substrate injection does not contribute to the subthreshold drain currents during the $HEMT$ transfer or reverse measurement. This would suggest that the $HEMT$ leakage currents are rather related to the Schottky gate reverse injection ($path$ 1 in figure 6-26 (c)). However, it is worth mentioning the high-value of the $sapphire$ I_{db} activation energy as $E_a \sim 3\ eV$ for $T >$ 250 °C.

To further investigate the origin of the subthreshold currents we have evaluated the $HEMT$ reverse currents *vs* temperature (up to $V_{ds} = 150\ V$), as shown in figure 6-26 (a) and (c) (for the set-up) and figure 6-27 (a). In this study the reverse bias range has been established to avoid degradation after subsequent measurements. It is worth mentioning that neither the nucleation layers, the GaN buffer nor the $AlGaN$ were optimized for very high-voltage operation. This can be achieved, for example, by the use of $AlGaN$ back barriers, inactive $Mg-doped\ GaN$ or gate dielectric passivation.[1,2,17] Again, I_{ds} strongly increases with T for the $sapphire$ device while there is a double regime ($T <$ 150 °C) for the Si device. Analogously, the $HEMT-on-sapphire$ exhibits what appears to be a single conduction $I_{ds}-V_{ds}$ mechanism. Here, a plot of $log\{I_{ds}/V\}$ vs $V^{1/2}$ depicts linearity suggesting $Poole-Frenkel$ mechanism.[52] The $HEMT-on-sapphire$ reverse drain current is closely fitted (figure 6-27 (c)) with an expression of the form:

$$I_{ds} = \alpha_1 V_{ds} \exp(-E_a/k_B T) \exp(\alpha_2 V_{ds}^{1/2}/k_B T) \qquad (6\text{-}6)$$

Being E_a the activation energy previously determined. α_1 is a prefactor fitting constant and α_2 would be the drain bias $Poole-Frenkel$ exponential coefficient. The $AlGaN/GaN$ $HEMT$ localized states can act as charge trapping centres, which occasionally emit thermal electrons. The mechanism of the field-assisted emission is known as the $Poole-Frenkel$ effect, where the barrier decreases by an amount of:

$$\Delta\emptyset_{PF} = \alpha_2\sqrt{V_{ds}} \quad where \quad \alpha_2 = \sqrt{q^3/d\pi\varepsilon_r\varepsilon_0} \qquad (6\text{-}7)$$

Where, ideally, ε_r is the high frequency dielectric constant and ε_0 is the vacuum permittivity. The ionization energy of these traps $E_i = E_a - \alpha_2 E^{1/2}$ becomes field

dependent. Note that the electric field (i.e. V_{ds}/d) within the complex hetero-structure is unknown. Therefore α_2 is maintained as a fitting constant also. The activation energy value (in the range of $\sim 0.3\ eV$) is completely in agreement with previous works.[48,49] Given the emission barrier height of $\sim 0.3\ eV$, it is unlikely that the process governing the leakage current density is emission of carriers from a dislocation-related trap state into the semiconductor conduction band.[48] Rather, it is believed that the emission is from a trap state to a continuum of states located somewhere within the bandgap associated with threading screw conductive dislocations.[53-55]

If this defective $AlGaN$ buffer/Schottky interface model is presumed valid for the $HEMT-on-sapphire$ for all the temperature range ($25-300$ °C), it evidently fails for $T < 150$ °C for the $HEMT-on-Si$. In this case, another leakage mechanisms are taking place, (which is much less temperature dependent), and is maintaining the subthreshold drain current above $10\ \mu A/mm$. In addition, the $log\{I_{ds}/V\}\ vs\ V^{1/2}$ depicts still linearity but it also clearly shows two distinct behaviors depending on V_{ds}. For $V_{ds} > 80\ V$, the $Poole-Frenkel$ slope is analogous for the $HEMT-on-sapphire$ and on Si, while the $Poole-Frenkel$ plot is not linear for the smallest drain voltages. In this sense, it was investigated if these differences are due to the additional leakage $path(s)$ present in the Si substrate or the nucleation layers related to the Si/GaN poor isolation ($path$ 2 and $path$ 3 in figure 6-26 (a) and (c)). Space-charge-limited, hopping and $Fowler-Nordheim$ expressions[52] (or a combination of them) were intensively tested to try to reproduce the particular experimental $GaN-on-Si$ experimental reverse $I_{ds}-V_{ds}$ behavior without adequate precision. However a Schottky emission equation (considering as the Schottky barrier the small thermal activation energy of $\sim 0.02\ eV$ experimentally determined):

$$I_{ds} = \alpha_3 T^2 \exp(-E_a/k_B T) \exp(\alpha_4 V_{ds}^{1/2}/k_B T) \tag{6-8}$$

Again closely fits the experimental results, as shown in figure 6-27 (b), for both $V_{ds} > 80\ V$ and $T < 150$ °C. In this case, the electric field reduces the small surface barrier by an amount of:

$$\Delta\emptyset_{SE} = \alpha_4 \sqrt{V_{ds}} \quad where \quad \alpha_4 = \sqrt{q^3/d4\pi\varepsilon_r\varepsilon_0} \tag{6-9}$$

As mentioned before, a trap assisted conduction mechanism was used for fitting the experimental characteristics of the $HEMT - on - sapphire$ $(25 - 300\ °C)$. As the reverse drain and the reverse gate currents are analogous (figure 6-27 (e)), I_{ds} is believed to take place following mainly $path\ 1$. The vast majority of the carriers contributing to the reverse and subthreshold currents are believed to be injected across the non-idealities of the reverse biased Schottky gate. Then carriers are transported thorough the $AlGaN$ barrier and/or the upper part of the GaN buffer via the trap assisted conduction with an emission barrier height of $\sim 0.3\ eV$ associated with threading screw conductive dislocations. For the $HEMT - on - Si$, the I_{ds} leakage current mechanism seems to be somehow similar (for $T > 150\ °C$ and $V_{ds} > 80\ V$), as it could be derived from the similar thermal activation energies and similar slopes required to fit the reverse $I_{ds} - V_{ds}$ characteristics.

However a careful analysis of the bulk current indicates that, for a broad range of V_{ds}, the drain reverse current is well reproduced by the bulk current (figure 6-27 (d)), suggesting $path\ 3$ as preferential. In this case, it seems reasonable to consider that electrons are injected from the source into the Si and nucleation layers, (across the GaN buffer), and then collected at the drain electrode assisted again by threading dislocations. This would explain the similarities with the Si device in terms of the characteristic trap energy and the $Poole - Frenkel$ slope. Additional GaN buffer background currents present in the $Si\ HEMT$ explains the distinct behavior for $T < 150\ °C$ and $V_{ds} < 80\ V$. The reduced low temperature characteristic trap energy of $\sim 0.02\ eV$ would be an indication of the spatial proximity of defects on the buffer and nucleation layers, but the transport mechanism correlates with Schottky emission rather than with $Poole - Frenkel$. As the reverse I_{gs} is significantly lower than I_{ds} (figure 6-27 (d)), the $path\ 1$ contribution appears to be small when compared with the injection from the Si substrate. Therefore this background Schottky emission should not be taking place in the depleted gate region but in the depletion region across one or more heterojunctions present in the nucleation layer. When analyzed the values that are required to fit the data (considering $\varepsilon_r = 9$), an electric field of $E \sim 0.5 \times 10^5\ V/cm$ was determined for the Schottky emission. Larger fields of $E \sim 4 \times 10^5\ V/cm$ were extracted for the $Poole - Frenkel$ mechanism. This would suggest again that Schottky emission localized states may be located deeper in the GaN buffer or in the nucleation/substrate region.

As shown in figure 6-27 (b) and (c), it can be clearly seen that, due to the different nature of the conduction mechanisms observed, the Si device is less sensitive to the elevated temperature (although it presents higher subthreshold current at room temperature). When the drain current on/off ratio is analyzed from figure 6-25 (a) and (b), it becomes also evident that the temperature impact ($\alpha \sim -9.4$) is more relevant when compared with the typical mobility related coefficients ($\alpha = 1.5 - 2.0$). For example, the on-resistance increases ($25 - 300$ °C) by a factor $\times 3$, while the subthreshold currents increase by several orders of magnitude (for the $HEMT - on - sapphire$). From the $I_{ds,sat}$ and the $HEMT$ reverse current expressions it can be derived an analytical expression relating the $I_{ds,on}/I_{ds,off}$ ratio to the $HEMT$ main physical parameters, namely L_g,W, C_b, $E_a(I_{ds,off})$, V_{th}, μ_n, R_{ds} and R_{th}. In our case we have the same layout $\left(L_g/W\right)$ and C_b for the Si and $sapphire$ $HEMT$. Analogously, V_{th}, R_{ds} and μ_n are very similar for both substrates. Therefore, it can be concluded that the most distinct parameters are E_a and R_{th}. The different E_a explains the different variation of the drain subthreshold currents shown in figure 6-24, and the different on/off ratio slopes shown in figure 6-25 (c) as the higher R_{th} is in the basis of the higher α for the $sapphire$ device. As the methods and substrates to fabricate a $HEMT$ device notably varies from one lab to another, the temperature coefficients, thermal activation energies or thermal impedances may vary accordingly from wafer to wafer.

However the qualitative description, the physical models and the methodology that we have presented before in this dissertation can be virtually applied to any $HEMT$ in any substrate. For example, in reference[56] it is reported a $MIS - HEMT$ passivated with an in-situ grown Si_3N_4 cap layer from a commercial vendor. The optimized high-voltage substrate together with the in-situ gate passivation explains the mitigated thermal activation of the device. The temperature coefficients for R_{on} ($\alpha = 0.93$) and $I_{ds,sat}$ ($\alpha = -1.31$) are significantly smaller (in particular for R_{on}). This is due to the $CMOS$ compatible $gold - free$ Ohmic contact technology which present much higher contact resistance than the typical $Ti/Ni/Al/Au$ stack. The contact resistance temperature dependence is competing with the mobility degradation with temperature (R_c is also diminishing with temperature), resulting in the unusual low value of α.

6.4.2.2. $MIS - HEMT\ vs\ T$: $ALD\ HFO_2$ AND IN-SITU Si_3N_4

6.4.2.2.1. THIN $ALD\ HfO_2$ $AlGaN/GaN$ POWER $MIS - HEMT$

Figure 6-28 (a) and (b) present the temperature dependence (up to 300 ℃) of the transconductance curve for typical fabricated $HEMTs$ ($A04\ i - HEMT$ and $A03b\ HfO_2\ MIS - HEMT$ respectively). At room temperature, it is clear that the MIS gate architecture also reduces both the drain and gate $Off - state$ leakage due to the insulator effect.[17,57-60]

From $HfO_2\ MIS - HEMT$ and $i - HEMT$ samples, the threshold voltage presents a small drift with the temperature of $500\ mV$, as shown in figure 6-29 (a), other than a Schottky gate $HEMT$ which is independent of the temperature.[11]

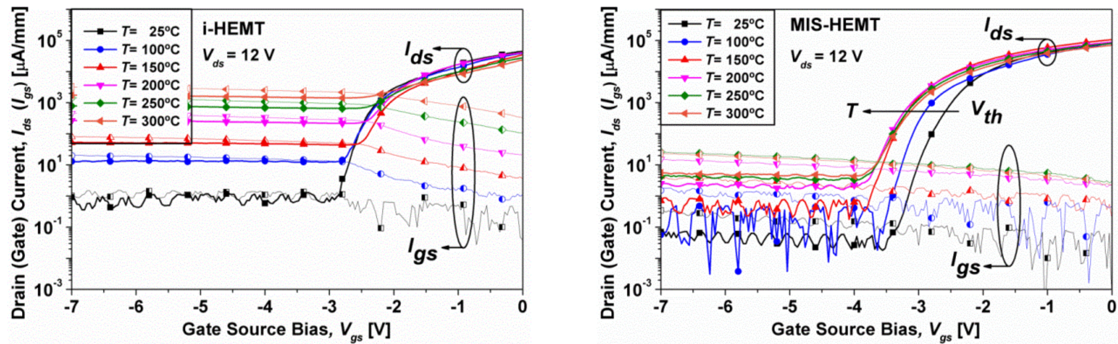

Figure 6-28. Transconductance curve (drain/gate current *vs* gate-source) for different temperatures (a) $i - HEMT$ and (b) $HfO_2\ MIS - HEMT$.

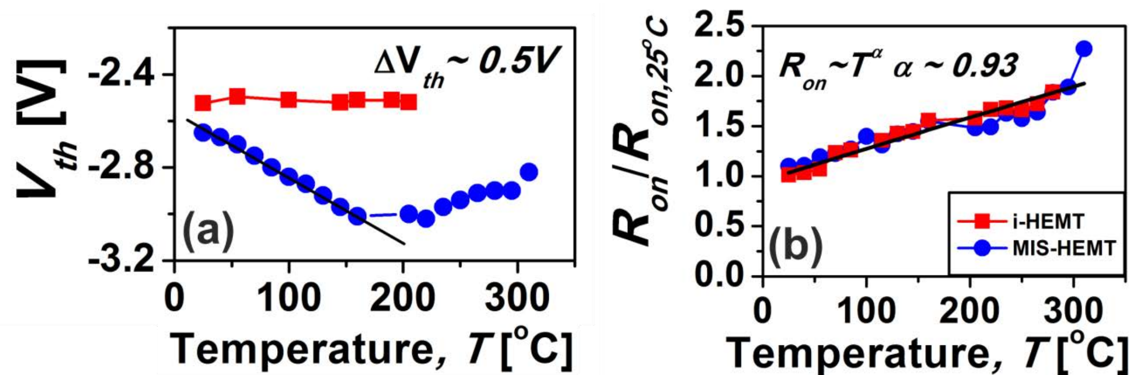

Figure 6-29. For the $i - HEMT$ and the $HfO_2\ MIS - HEMT$ (a) Threshold voltage and (b) on-resistance *vs* temperature.

The temperature dependence of the on-resistance can be fitted with a power law $R_{on}\ \alpha\ T^{\alpha}$ with $\alpha = 0.93$ which is agreement with figure 6-29 (b).

6.4.2.2.2. THIN IN-SITU GROWN Si_3N_4 POWER $AlGaN/GaN$ $HEMT$

From in-situ Si_3N_4 $MIS-HEMT$ ($E08$ sample), high-temperature device performance was also investigated. Figure 6-30 presents the temperature stability of the transconductance for a typical $MIS-HEMT$ device. The MIS gate architecture was very effective in suppressing both the drain and gate $Off-state$ leakage up to ~250 °C (figure 6-30 (c)). A negligible shift in the V_{th} was observed within experimental error (figure 6-30 (a)). This indicates that the amount of mobile charge present in the gate insulator was also negligible. In any case, the forward current decreased with the temperature as can be seen in figure 6-30 (b).

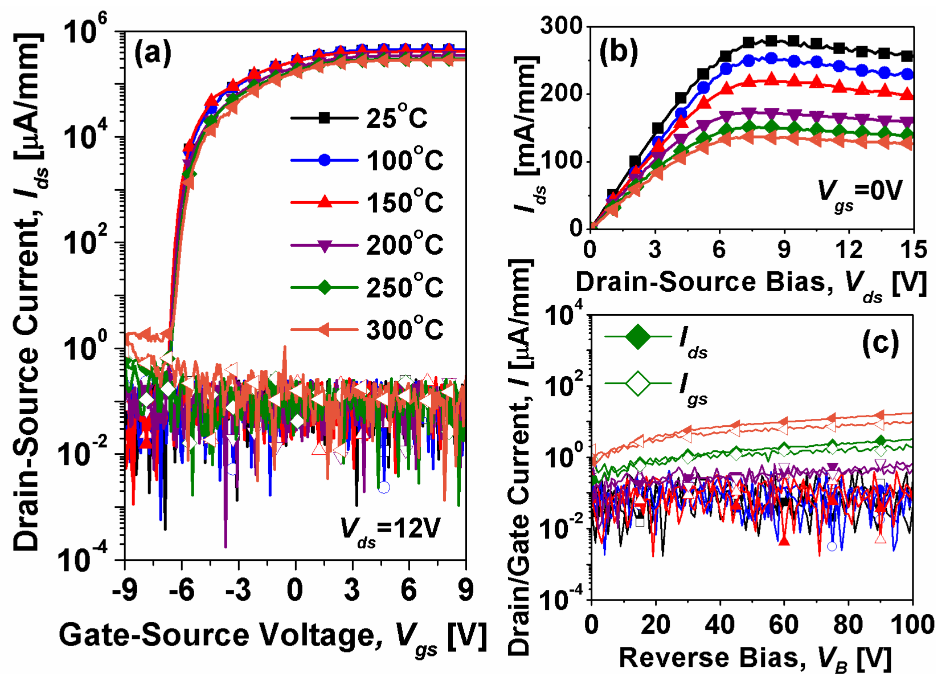

Figure 6-30. (a) In-situ Si_3N_4 $MIS-HEMT$ transconductance curve (drain/gate current *vs* gate-source) for different temperatures ($25-300$ °C). A negligible shift in the threshold voltage was observed within the experimental error. (b) Drain current characteristics at varying temperatures. (c) The in-situ passivation along with the optimized GaN buffer resulted in $HEMT$ drain/gate leakage currents with exceptionally temperature-independent behavior up to ~250 °C.

From in-situ Si_3N_4 $MIS-HEMT$ sample, the R_{on} increased by ~80% from RT to 300 °C as shown in figure 6-31 (a). The R_{on} increase (R_{on}^{-1}~$q\mu_n n_s$) is attributable to the reduction of the μ_n with temperature since the n_s is generally considered as virtually temperature independent. In the $AlGaN/GaN$ heterojunction, lattice vibrations due to polar-optical phonons in the non-intentionally doped GaN layer strongly increase with temperature and hence reduced the mobility at elevated temperatures.[9]

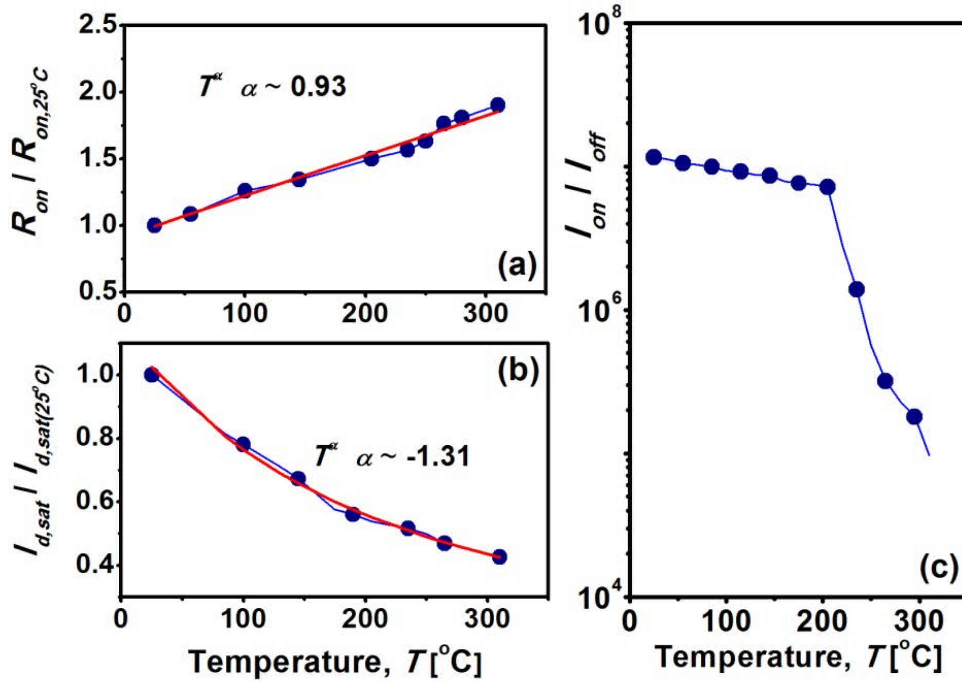

Figure 6-31. In-situ Si_3N_4 $MIS-HEMT$ (a) on-resistance *vs* temperature where the R_{on} increased by ~80% from RT to 300 °C. The R_{on} increase $\left(R_{on}{}^{-1} \sim q\mu_n n_s\right)$ is due to the reduction of the n_s with T although the n_s is generally considered as virtually temperature independent.[9,11,61] (b) Saturation current versus temperature where the self-heating effects showed a greater sensitivity to the temperature than R_{on}. (c) The transconductance I_{on}/I_{off} ratio is $\sim 1.0 \times 10^7$ up to ~220 °C where it started to decrease sharply down to $\sim 1.0 \times 10^5$ at ~300 °C.

For the saturation current (figure 6-31 (b)), the temperature coefficient can be fitted with $\alpha = -1.31$. In figure 6-31 (c) the transconductance I_{on}/I_{off} ratio is $\sim 1.0 \times 10^7$ up to ~220 °C where it starts to decrease sharply down to $\sim 1.0 \times 10^5$ at ~300 °C.

6.4.2.2.3. REVERSE LEAKAGE THERMAL ACTIVATION

From HfO_2 $MIS-HEMT$ and $i-HEMT$ samples, the $HEMT$ leakage currents increase with the temperature, which is typical of a rate-limited thermally activated process following an Arrhenius law ($I = I_0 exp[-E_a/k_B T]$), up to a saturation regime.

From the I vs $1/k_B T$ (in the linear range), the activation energy (of the gate/drain current) can be determined, being $E_a = 0.4$ and $0.3\ eV$ for the $i-HEMT$ ($75-300$ °C) and the $-HEMT$ ($75-210$ °C), respectively (figure 6-32 (a) and (b)). Differently, as shown in figure 6-32 (c), for the in-situ Si_3N_4 $MIS-HEMT$ it was observed that the leakage currents were negligible up to ~250 °C (using a $V_{ds} = 0-100\ V$ reverse sweep).

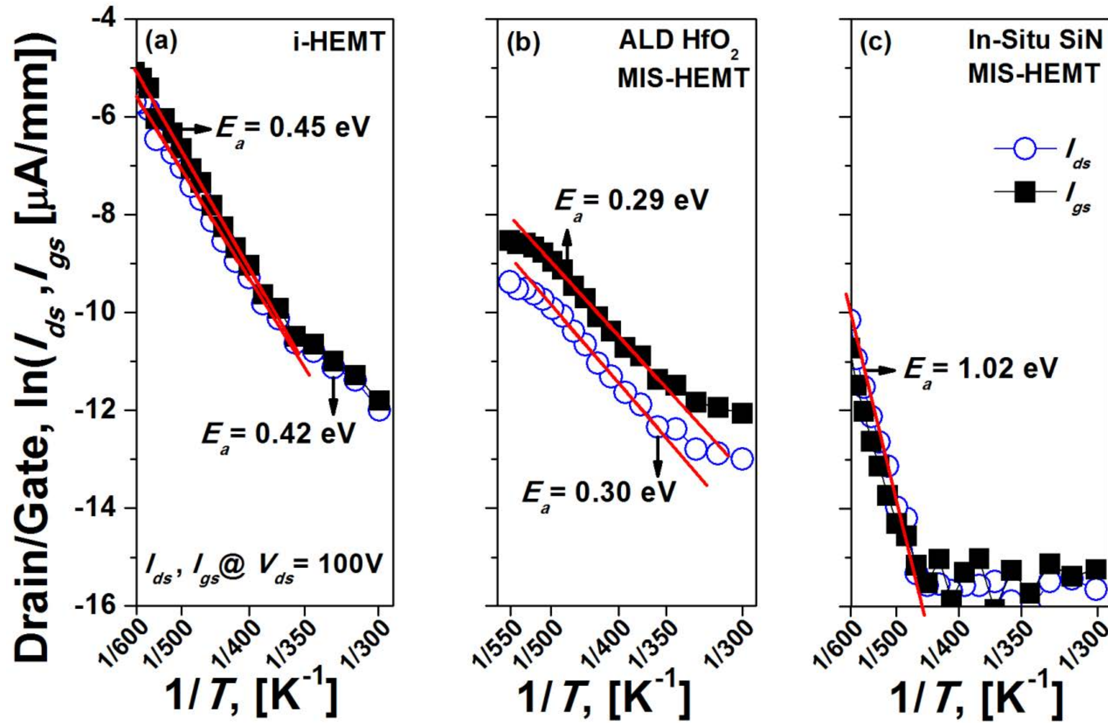

Figure 6-32. Reverse drain and gate source current at $V_{ds} = 100\ V$. Arrhenius plot for the (a) $i - HEMT\ (A04)$. (b) $HfO_2\ MIS - HEMT\ (A03b)$ showing the I_{ds} and $I_{gs}\ E_a$. The gate-drain leakage on the $MIS - HEMT$ is due to improper passivation on top of the HfO_2. (c) An Arrhenius plot showing the E_a for the in-situ $Si_3N_4\ MIS - HEMT$ of $E_a \sim 1.02\ eV$ for $T > 200$ ℃.

The activation energy was determined to be as high as $E_a \sim 1.02\ eV$. We suggest that this larger value of the thermal activation energy is related to the larger effective heterojunction electron barriers achieved by the in-situ passivation along with the optimized GaN buffer.

6.4.3. HIGH TEMPERATURE RELIABILITY

As mentioned before, benefiting from its WBG power $AlGaN/GaN\ HEMT$ devices can work up to high-operating temperature and present good radiation hardness. For example, Maeda *et al.*[62] reported excellent $I_{ds,sat}$ and acceptable pinch-off characteristics up to 400 °C for $AlGaN/GaN\ HEMTs$. They observed a decrease in the saturated drain current by about one-third by increasing temperature from $25 - 400$ °C. In the same sense, Daumiller *et al.*[63] measured $I - V$ characteristics of $AlGaN/GaN\ HEMTs$ at temperatures up to 800 °C and reported stable device operation without irreversible degradation up to 600 °C.

High-device performance is a good point to achieve working devices, but is not enough for a technology to be successful, since a reliability stress test must also be assure. For this reason preliminary $Off-state$ stress tests ($V_{gs} = -6\,V$) were performed at elevated temperatures showing no degradation at a reverse bias of $V_{ds} = 200\,V$ and 310 °C for a drain–gate spacing of $8\,\mu m$, as shown in figure 6-33 (a) for the HfO_2 $MIS-HEMT$. At 200 °C and 200 V the gate and drain are still coupled. However, at 310 °C the drain current was greater than the gate current. We believe that at 310 °C the drain current was greater than the gate current due to Si substrate bulk current thermal activation.

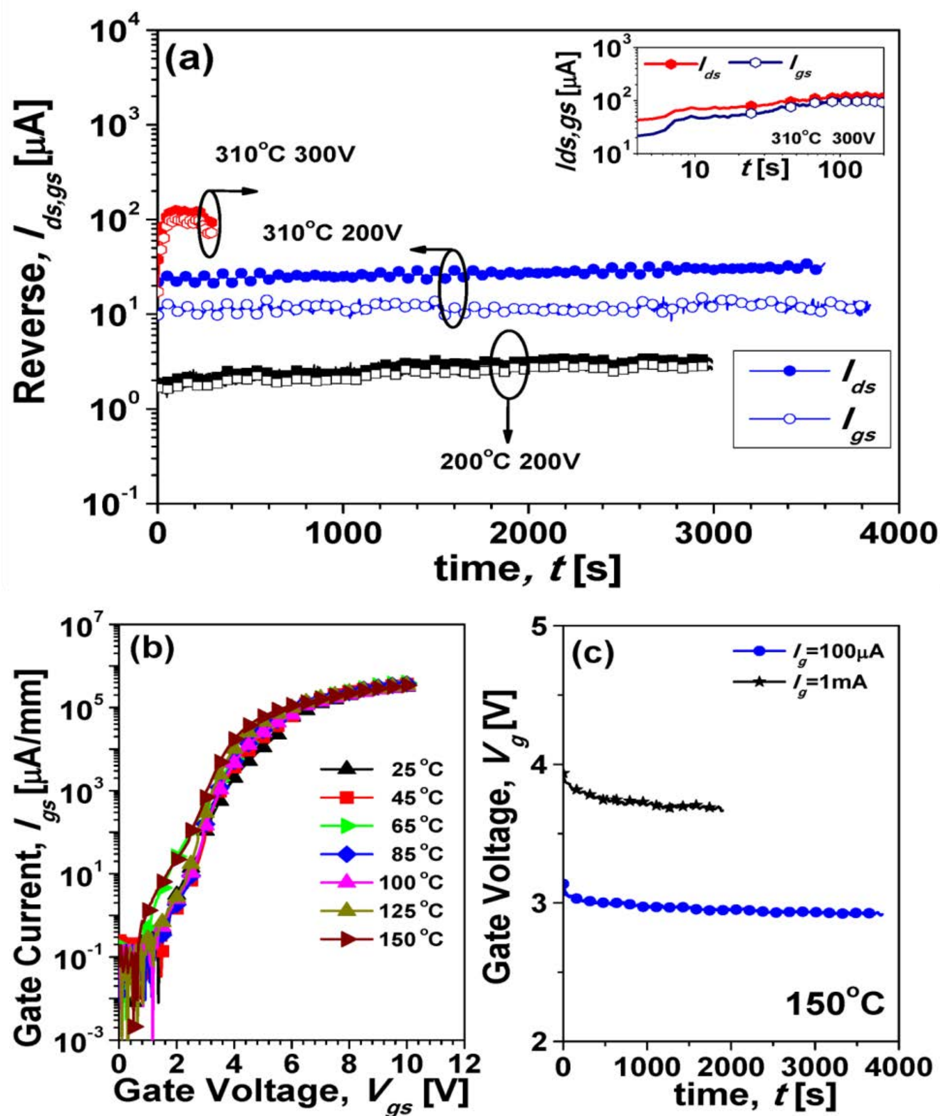

Figure 6-33. HfO_2 $MIS-HEMT$ $(A03b)$ **(a) gate/drain** $Off-state$ **current** *vs* **time stress. In the inset, magnification of the stress effects at** 310 ℃ **at** $300\,V$**. (b) Dielectric stress tests at high-temperature. (c)** Q_{bd} **constant current stress is applied, showing some charge trapping at** $I_g = 1\,mA$**, and negligible charge trapping at** $I_g = 100\,\mu A$.

When the device was stressed at a reverse bias of $300\ V$ at $310\ °C$ a sudden increase of the leakage current was observed with stabilization after few seconds (inset figure 6-33 (a)). When the transconductance curve was analyzed after stress testing, it appears that devices stressed at $200\ °C/200\ V$ have survived with no remarkable shift in either the threshold voltage or the $Off-state$ current.

Devices stressed at $310\ °C/200\ V$ survived (same low $Off-state$ current before/after) but when the gate was biased at small positive gate bias, we observed a sudden increase of the gate current. Therefore, it appears that the gate insulator has been degraded somehow. Devices stressed at $310\ °C/300\ V$ were severely damaged and the gate current in the $Off-state$ increased up to four orders of magnitude after stress.

In addition, the HfO_2 gate insulator leakage current is weakly dependent on the temperature, which suggests a trap-assisted tunneling or tunneling assisted mechanism and is relatively stable under constant current Q_{bd} stress (figure 6-33 (b) and (c)). We have observed that in both cases ($1\ mA$ and $0.1\ mA$) the devices survived. However, we have observed for both cases a positive threshold shift of the transconductance towards positive values ($\sim 0.75\ V$) and an increase of the $Off-state$ currents (gate and drain). Before stress, the $Off-state$ gate and drain current (at $150\ °C$) was determined to be $0.1\ \mu A/mm$. In the case of Q_{bd} at $0.1\ mA$, this gate leakage increased up to $5\ \mu A/mm$ while for $1\ mA$ this value further increased up to $500\ \mu A/mm$.

6.5. SUMMARY

Due to the WBG of GaN, $AlGaN/GaN\ HEMT$ power devices can sustain very high-voltages when biased in a reverse configuration and can work correctly at temperature higher than $300\ °C$. In the first part of the chapter the main results of the $AlGaN/GaN\ HEMTs$ power switches fabricated at the clean room of the CNM have been presented in the framework of the industrial contract with ON semiconductor. We have shown that the fabricated devices are in the state-of-the-art ($gold-free$ Ohmic and Schottky contacts) taking into account their power device figure-of-merit ($V_B^2/R_{on,sp}$) of $4.05 \times 10^8\ W/cm^2$. The extensive characterization of our $AlGaN/GaN\ HEMTs$ devices was done by means of DC characterization ($On-state$ and $Off-state$), DC wafer mappings, reverse and breakdown voltage in $Galden\ bath$ and $high-T$ stress.

Basically, two different families of $AlGaN/GaN - on - Si\ MIS - HEMTs$ devices were fabricated on commercial 4 $inch$ wafers: (i) using a thin $ALD\ HfO_2$ (deposited on the CNM clean room) and (ii) thin in-situ grown Si_3N_4, as a gate insulator (grown by the vendor).

Extensive DC characterization $Off - state$ tests for thin $ALD\ HfO_2\ Au - free\ GaN - on - Si\ HEMT$ 4 $inch$ was investigated by means of wafer-level mapping. The typical drain and gate reverse current characteristics exhibited breakdown voltage saturation for $V_B \sim 700\ V$ for $(L_{gd} > 6 - 14\ \mu m)$. The yield of devices at $V_{ds} = 100\ V$ exhibiting gate currents lower than $1\ \mu A/mm$ was as high as 95%. The gate leakage current for these devices was in the range of $70 \pm 13\ nA/mm$. The thin $ALD\ HfO_2$ based MIS approach also resulted in improved gate stability and robustness under positive gate bias. Negligible gate current flow was found at $V_{gs} = +1.5\ V$. Irreversible degradation of the gate structure and device performance was observed at $V_{gs} = +5.5\ V$. The specific on-resistance value was very uniform across the wafer with $R_{on,sp} = 2.8 \pm 0.3\ m\Omega cm^2$. The maximum saturation current was also very uniform across the wafer with $I_{ds,sat} = 125 \pm 12\ mA/mm$ measured at $V_{gs} = 0\ V$. At $V_{gs} = 9\ V$ this value increased significantly to $I_{ds,sat} = 350 \pm 24\ mA/mm$. In addition, a remarkably homogeneous threshold voltage of $V_{th} = -3.0 \pm 0.3\ V$ was determined.

The device reproducibility of $900\ V - class\ \ MIS - HEMTs$ with a thin in-situ grown Si_3N_4 gate insulator was investigated by means of wafer-level mapping. The typical drain and gate reverse current characteristics exhibited breakdown voltage saturation for $V_B \sim 900\ V$ for $(L_{gd} > 8 - 10\ \mu m)$ and $V_B > 600\ V$ for gate-drain length of $L_{gd} > 5\ \mu m$. The gate leakage current was maintained in all cases below $1\ \mu A/mm$ at $V_{ds} = 600\ V$. The yield of devices at $V_{ds} = 100\ V$ exhibiting drain currents lower than $1\ \mu A/mm$ was as high as 99%. The drain leakage current for these devices was in the range of $2 - 50\ nA/mm$. For the gate current, the yield with $I_{gs} < 1\ \mu A/mm$ at $V_{ds} = 100\ V$ was 95%. The gate leakage current for these devices was in the range of $4 - 50\ nA/mm$.

The thin in-situ Si_3N_4 based MIS approach also resulted in improved gate stability and robustness under positive gate bias. Negligible gate current flow was found at $V_{gs} = +9.0\ V$. Irreversible degradation of the gate structure and device performance was

observed at $V_{gs} = +13.0\ V$. The specific on-resistance value was very uniform across the wafer with $R_{on,sp} = 2.5 \pm 0.3\ m\Omega cm^2$. The maximum saturation current was also very uniform across the wafer with $I_{ds,sat} = 325 \pm 33\ mA/mm$ measured at $V_{gs} = 0\ V$. At $V_{gs} = 9\ V$ this value increased significantly to $I_{ds,sat} = 603 \pm 44\ mA/mm$. In addition, a remarkably homogeneous threshold voltage of $V_{th} = -5.8 \pm 0.3\ V$ was determined. Large area/large current devices can be defined with both gate architectures in spite that the $Au-free$ contact $CMOS$ compatible results in higher on-resistance (when compared with traditional $HEMTs$). In particular, for in-situ grown Si_3N_4, large area $HEMTs$ ($W = 31\ mm$) yield more than $18\ A$, with an on-resistance of 0.4 Ω for $V_{gs} = 0\ V$. A thicker second metal level was deposited on top of the $Au-free$ Ohmic contacts to achieve a current of several amperes. These devices also exhibited low leakage currents below 1 $\mu A/mm$ up to $500\ V$ biased in reverse.

In the second part of this chapter, it has been reported the elevated temperature impact on the forward and the reverse leakage currents for analogous Schottky gate $HEMTs$ grown on different substrates: Si, $sapphire$ and $FS-GaN$. These devices have been fabricated in the clean room of the $CRHEA-CNRS$. The temperature has a well know detrimental effect on the carrier mobility, as several scattering phenomena increase with the temperature. This, in turn, implies a reduction of the $On-state$ current of the device with temperature. Also well-known is the strongest temperature dependence of the $HEMT-on-sapphire$ due to the Al_2O_3 substrate lower thermal conductivity. The forward-current T^{α} have been determined on three different substrates for $Si, sapphire\ and\ FS-GaN$ in the range of $25-300$ ℃. The typical temperature coefficients (α) for $R_{on,sp}$, $I_{ds,sat}$ and $g_{m,max}$ have been determined 1.33, -1.53 and -1.08 for Si, 1.83, -1.78 and -1.33 for $sapphire$ and 1.29, -1.48 and -0.99 for $FS-GaN$ respectively. The greatest thermal stability has been observed for the $FS-GaN$ device, while the device in $sapphire$ is the worst. This fact is explained in terms of an improved thermal conductivity of the $FS-GaN$ substrate. Normalizing R_{th} with respect to the $FS-GaN$ value (at RT), it was observed a factor of improvement of × 1.6 and × 2.7 compared to Si and $sapphire$, respectively.

The elevated temperature also degrades, in general, the $Off-state$ current of the $HEMTs$ devices. This has been comparatively studied for the $HEMT-on-Si$ and $sapphire$. For the $HEMT-on-sapphire$, the $Off-state$ subthreshold current

increase with temperature ($25-300$ °C) is linear $E_a\sim 0.3\ eV\ (I_{ds,off})$. For the $HEMT-on-Si$, it was observed two different temperature regimes, being basically temperature independent up to 150 °C and then, $E_a\sim 0.3\ eV\ (I_{ds,off})$. A single trap assisted conduction mechanism ($Poole-Frenkel$) was used to fit the experimental characteristics of the $HEMT-on-sapphire$ ($25-300$ °C). As the bulk current is negligible up to 250 °C, it is suggested that the origin of the subthreshold currents comes from the defective $AlGaN$ buffer/Schottky interface. For the $HEMT-on-Si$, the presence of additional leakage from the substrate and/or nucleation layers modifies substantially the $Off-state$ thermal characteristics of the device, particularly for the smallest drain voltages. Although the methods and substrates to fabricate $AlGaN/GaN$ $HEMTs$ notably vary from one lab to another and the thermal coefficients may be different from wafer to wafer, we believe that the methodology described in this dissertation can be virtually applied to any $HEMT$ in any substrate.

A gate insulator also has a relevant impact on the temperature behaviour of a $HEMT$ device. A MIS gate architecture can be very effective in suppressing both the drain and gate $Off-state$ leakage. For the in-situ Si_3N_4 $MIS-HEMT$ it was observed that the leakage currents were negligible up to ~250 °C (using a $V_{ds}=0-100\ V$ reverse sweep). A negligible shift in the V_{th} was observed within experimental error. This indicates that the amount of mobile charge present in the gate insulator was also negligible.

The activation energy was determined to be as high as $E_a=1.02\ eV$. We suggest that this larger value of the thermal activation energy is related to the larger effective heterojunction electron barriers achieved by the in-situ passivation along with the optimized GaN buffer. Analogously, the ALD HfO_2 solution also mitigates to some extent the gate leakage with the elevated temperature. The reverse bias leakage current E_a (gate and drain) was determined to be $E_a=0.4\ eV$ and $0.3\ eV$ for the $i-HEMT$ ($75-300$ °C) and the $MIS-HEMT$ ($75-210$ °C), where leakage saturation was observed for $T>210$ °C for the $MIS-HEMT$.

Finally, preliminary $high-T$ reliability stability assessment of the ALD HfO_2 device has presented. The $Off-state$ stress tests ($V_g=-6\ V$) showed no degradation at a reverse bias of $V_{ds}=200\ V$ and 310 °C for a drain-gate spacing of $8\ \mu m$. When the device is stressed at a reverse bias of $300\ V$ at 310 °C it was observed a sudden increase

of leakage current with a stabilization after few seconds. When the g_m curve is analyzed after stress test, it appears that devices stressed $200\ V$ at $200\ ℃$ have survived with no remarkable shift in either the V_{th} or the $Off-state$ current. The devices stressed $200\ V$ at $310\ ℃$ survived (same low $Off-state$ current before/after) but when the gate is biased at small positive gate bias, we observed a sudden increase of the gate current. Therefore, it appears that effectively the gate insulator has been degraded somehow. Devices stressed $300\ V$ at $310\ ℃$ were severely damaged and the gate current in the $Off-state$ increases up to four orders of magnitude after stress.

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Chapter 7
AlGaN/GaN HEMT normally-off strategies

7.1. Introduction

Most of the $AlGaN/GaN\ HEMTs$ presents $normally-on$ operation because the $2DEG$ exist under the gate at $0\ V$ gate bias voltage. For power electronics applications, $normally-off$ operation is required to simplify the design of driving circuits. However, $HEMT$ devices are generally $normally-on$ devices and it is difficult to convince power systems designers and final users to use these $normally-on$ switches.

In this chapter, we will review the state-of-the-art of the $normally-off\ AlGaN/GaN\ HEMTs$ strategies. This section analyzed several techniques to obtain the $normally-off$ operation for $AlGaN/GaN\ HEMTs$ such as using a thin $AlGaN$ barrier, a recessed gate structure, a fluoride-based plasma treatment, a $p-type$ gate structure or using a nonpolar $a-plane$ channel.

In addition, a theoretical study based on multidimensional Synopsys $TCAD$ is done on semiconductors devices. These numerical simulations are focused in $AlGaN/GaN$ recess in order to analyze the impact of thinner barrier in terms of the positive shift

threshold voltage, the transconductance increase, the band diagram ($2DEG$ properties), the electron density and the $2DEG$ sheet carrier concentration behavior.

Finally, we will present an analytical model for an hybrid $AlGaN/GaN\ HEMT$. The methodology presented in this section, can aid the designers to understand the physics and to electrically characterize the new generation of GaN based devices. The models proposed here can also easily be implemented in $TCAD$ simulation packages where models for GaN devices are not mature yet.

7.2. STATE-OF-THE-ART

In this section, a review of the strategies for converting conventional $normally-on\ (D-mode)$ to $normally-off\ (E-mode)\ AlGaN/GaN\ HEMT$ will be presented. Recently different approaches have been demonstrated to achieve $normally-off$ devices.[1-8]

Several techniques for the $normally-off$ operation have been reported so far, such as using a thin $AlGaN$ barrier, a recessed gate structure, a fluoride-based plasma treatment, a $p-type$ gate structure or using a non-polar $a-plane$ channel, as shown in table 7-1.

1. **Thinning $AlGaN$ barrier**
   1.1. $AlGaN$ recess
   1.2. $AlGaN$ thin MBE growth
2. **CF_4 Fluoride based plasma**
   2.1. Pure CF_4
   2.2. Fluoride and recess
3. **$p-type$ on $AlGaN$**
   3.1. $pn-junction$
   3.2. GIT conductivity Modulation
   3.3. NiO_x gate (and recess)
4. **Hybrid $MOS-HEMT$**
5. **$AlGaN$ buffer engineering**
   5.1. $GaN-AlN$ stacks
   5.2. $AlGaN$ buffer
   5.3. $InGaN$ cap layer
   5.4. Nonpolar $AlGaN/GaN$

Table 7-1. Different strategies for achieving an $AlGaN/GaN\ HEMT\ normally-off$.

7.2.1. THINNING OF THE $AlGaN$ BARRIER

Enhancement mode on $AlGaN/GaN\ HEMTs$ was first reported by Khan *et al.*[9] in 1996. Since then, some $normally-off\ AlGaN/GaN\ HEMTs$ have been reported with several nanometers-thick $AlGaN$ layer to reduce the $2DEG$ density along the entire $2DEG$ channel between source and drain.

In the standard $AlGaN/GaN\ HEMT$ heterostructure, where Al composition is in the range of $15-35\%$ and the $AlGaN$ barrier thickness is around $20\ nm$, the reduction in the $AlGaN$ thickness by a gate etch, results in a reduced polarization-induced $2DEG$ density and with the help of the gate-metal work function, the V_{th} can be shifted positively. With a deep-enough gate-recess etching, the V_{th} can reach positive value and $E-mode\ HEMTs$ are formed. So, reducing the thickness of the $AlGaN$ is a viable approach to shift the V_{th} to positive values.[10] However, it could also result in high-parasitic resistances, larger gate leakage and high-on-state resistance values.

For conventional $GaAs$ and $InP-based\ HEMTs$, there are sufficient highly selective chemical wet-etching recipes that can be applied to achieve a well-controlled recess etching. However, due to its high-chemical inertness on the $AlGaN/GaN$ technology, commonly, it is used an inductively coupled plasma $(ICP)\ or\ RIE$ based recess which could result in low control, low selective and local damage. The RTA at 700 °C was found to be able to repair damages. However this RTA could be no compatible with gate metals such as Ni/Au. Schottky gate $HEMTs$ or $i-HEMTs$ are the devices generally reported with this technique.

For example, Derluyn *et al.*[11] achieve a $normally-off$ device with state-of-the-art performances by selective removal of in-situ grown Si_3N_4. By removing the in-situ Si_3N_4 under the gate electrode prior to Ni/Au metallization, they locally modify the $AlGaN$ surface potential. As a result, the channel is depleted under the gate while low access resistance is maintained in the L_{gs} and L_{gd} areas.

In this work, it appears that $AlGaN$ barrier is recessed up to a remaining $4\ nm$ but using a reduced power etch (from $50-5W\ RF$) in ICP with $SF6$ chemistry. The reduced power etch was performed in order to avoid the incorporation of $F-ions$ that improves the V_{th} towards more positive values but also causing instabilities of the threshold voltage.

It is worth mentioning that the use of $4\ nm$ thin $Al_{45}GaN_{55}$ top barrier layer does not degrade the breakdown behavior and even at high-drain bias, the leakage current remains low. In this structure also the $Al_{18}GaN_{82}$ back barrier is very efficient in confining the electrons at the $2DEG$, preventing them from overflowing into the buffer and towards the Si substrate.

Recessed $MIS - HEMTs$ have been also proposed Nakayama *et al.*[12] but the objective of the reported devices is not to make the device $normally - on$ but increase the transconductance of $MIS - HEMTs$ or reducing its gate leakage. Oka *et al.*[2] propose a recessed $MIS - HEMT$ but the $AlGaN$ barrier is pretty thick and in addition it resembles more to a hybrid $MIS - HEMT$.

7.2.2. FLUORINE PLASMA

Cai *et al.*[13,14] proposed in 2005 the fluoride-based plasma treatment for achieve a $normally - off$ operation. No change in $AlGaN$ thickness is required in this method. The control of the V_{th} was realized through a modulation of energy band by $F - ions$ implanted in the $AlGaN/GaN$ heterojunction during the plasma treatment.

The fluorine ions have a strong electronegativity and are negatively charged, effectively raising the potential in the $AlGaN$ barrier and the $2DEG$ channel. As a result, the V_{th} can be shifted to positive values. A post-gate annealing at 400 °C proves to be effective in recovering the plasma-induced damage. In 2006, the same authors[15] demonstrated a $MIS - HEMT$ combined with plasma treatment technique. The $MIS - HEMT$, when $E - mode$ operation is possible, can provide several benefits in its applications.

As demonstrated in the previous chapters, $MIS - HEMTs$ are preferred for high-temperature operation, because the additional insulator between the gate electrode and III-nitride semiconductor provides an additional potential barrier between the gate electrode and the channel, which then suppress the thermionic emission and tunnelling at $high - T$ and keep the gate voltage swing reasonably large for proper circuit operation. The increased gate turn-on voltage can facilitate the accommodation of a more positive V_{th}, which is preferred not only for assuring the complete turn-on of the device at zero bias, but also for providing improved device safety for certain circuits such as power switches.

In the literature,[15] the first $E - mode$ $Si_3N_4/AlGaN/GaN\ MIS - HFETs$ with two-steps Si_3N_4 process which features a thin layer of Si_3N_4 $(15nm)$ under the gate and a thick layer of $Si_3N_4(125\ nm)$ in the access region. The fluoride-based plasma treatment technique was adopted to convert the device from $D - mode$ to $E - mode$. Also in 2006, Palacios *et al.*[16] reported the use of gate recess combined with fluorine-based surface treatment under the gate achieving very high-transconductance.

It has been suggested that a major drawback of the fluorine process is that $F - ions$ are not stable under thermal stress and other reliability issues still unexplored. However, Boutros *et al.*[3] developed a fluorine-based process for $normally - off\ GaN - on - Si\ HEMTs$ which enabled high-breakdown voltage ($V_B > 1100\ V$), low-leakage ($< 10\ \mu A/mm\ at\ V_B/2$), high-peak current ($I_{max} = 5\ A$), and the highest $V_B^2/R_{on,sp}$ ratio of $272\ MW/cm^2$. Authors claimed that this performance is comparable to mature SiC and is × 2 better than $Si\ IGBT$. Large periphery, 5 A devices were tested in 200 kHz boost converter at 360 V and 180 W output power with and efficiency of $\eta > 96\%$ for voltages up to 200 V.

7.2.3. $p - type$ ON $AlGaN$

7.2.3.1. SELECTIVELY GROWN $pn - junction$ GATE

$E - mode\ AlGaN/GaN\ HEMTs$ have also been demonstrated using a $pn - junction$ gate. In 2000, Hu *et al.*[17] proposed and enhancement mode $AlGaN/GaN\ HEMT$ with selectively grown $pn - junction$ gate. At zero gate bias, the device channel was depleted due to the high-built-in potential of the gate-channel junction. The $p - GaN$ layers for the gate were grown in selective areas defined by openings in an SiO_2 mask. $Mg - doped$ 100 nm thick $p - GaN$ ($1.0 \times 10^{17} cm^{-3}$) was selectively grown using 10 $\mu m \times 150\ \mu m$ openings in a 100 nm thick masking layer.

7.2.3.2. PANASONIC GIT – CONDUCTIVITY MODULATION

In 2006, Uemoto *et al.*[4] demonstrated a new operation principle of a $GaN - based\ normally - off$ transistor with high-drain current, which was called gate injection transistor (GIT). The GIT utilizes hole injection from the $p - type$ gate to the $2DEG$ region bringing out the conductivity modulation as observed in $IGBTs$. This new concept enables both $normally - off$ operation and high-current driving capability by applying high-positive gate voltage with low gate current.

The process flow of the GIT is summarized as follows. A $p - AlGaN/i - AlGaN/GaN$ heteroepitaxial structure for the GIT is grown on a Si substrate with buffer layers consisting of the GaN/AlN multilayers on top of the $AlGaN/AlN$ initial layers. Both layers effectively relieve the strain in the overgrown GaN caused by the lattice and thermal mismatch between GaN and Si. The total thickness of the nitride epitaxial layer

is 4.7 μm. To realize the $normally-off$ operation, the Al mole fraction and the thickness of $i-AlGaN$ are optimized to be 15% and 25 nm. The $p-type$ gate is formed by the selective etching of the $p-AlGaN$. The Al mole fraction and the thickness of the $p-AlGaN$ are chosen to be 15% and 100 nm. After the formation of the device isolation area, the Ti/Al source/drain and Pd gate metals are formed. As a passivation film, 400 nm thick Si_3N_4 was deposited by $PECVD$. Au interconnections are made by electroplating.

The $p-AlGaN$ lifts up the potential at the channel, which enables $normally-off$ operation. At the gate voltage of 0 V, the channel under the gate is fully depleted, and the drain current does not flow. At the gate voltages up to the forward built-in voltage (V_F) of the $p-n-junction$, the GIT is operated as a FET. Further increase of the gate voltage exceeding the V_F results in the hole injection to the channel from the $p-AlGaN$. Note that the injection of the electrons from the channel to the gate is well suppressed by the hetero-barrier at $AlGaN/GaN$. The injected holes accumulate the equal number of electrons that flow from the source to keep charge neutrality at the channel. The accumulated electrons are moved by the drain bias with high-mobility, while the injected holes stay around the gate because the hole mobility is at least two orders of magnitude lower than that of the electron. This conductivity modulation results in a significant increase of the drain current, which keeps low the gate current.

7.2.3.3. NiO_x GATE WITH RECESS

This method was proposed by Kaneko *et al.*[18] based in the idea of improving the recess $normally-off$ operation of a $HEMT$. They claimed that by forming recess structure only under the gate electrode, the V_{th} can be moved to the vicinity of 0 V without a remarkable increase in R_{on}. The complete $normally-off$ characteristic cannot be obtained only by the recess structure. Then, they formed the NiO_x as a gate electrode in addition to the recess structure. The NiO_x gate electrode operates as a $p-type$ material. The complete $normally-off$ characteristic then is due to the combination of both structures.

7.2.4. $AlGaN$ BUFFER ENGINEERING

Therefore, several approaches have been developed for converting the $GaN\ HEMTs$ from the conventional $normally-on$ mode to the desired $normally-off$ mode.

One approach is to employ a recessed-gate structure so that the $AlGaN$ under the gate is too thin to induce a $2DEG$. Another approach is to introduce a $p-doped\ GaN$ or $AlGaN$ cap layer to deplete the $2DEG$ underneath. A third approach is to use fluorine-based plasma to bombard the semiconductor under the gate metal, so that acceptors are formed in this region, effectively depleting the $2DEG$.

Each of these approaches has its own pros and cons, and extensive studies are underway to examine the suitability of each approach for applications in $high-T\ ICs$ and high-power electronics.

The $AlGaN$ buffer engineering (which could be used in combination with some of the aforementioned techniques), have been reported in several papers to achieve $normally-off\ HEMTs$. These techniques include deep-recess $V-gate$ technology,[19] a piezo neutralization layer formed at the bottom of the gate recess,[20] $Cat-CVD\ Si_3N_4$ or in situ Si_3N_4 cap layer in combination with AlN thin barrier.[21,22] $n-GaN/i-AlN/n-GaN$ triple cap layer, a recessed-gate structure, and $high-k$ gate dielectrics showed high-drain current ($800\ mA/mm$) and complete enhancement-mode operation with a $high-V_{th}$ ($V_{th}=3\ V$) .[5] Mizutani *et al.*[23] proposed to implement the $normally-off\ HEMTs$ with a thin $InGaN$ cap layer. The key idea is to employ the polarization-induced field in the $InGaN$ cap layer, by which the conduction band is raised, which leads to the $normally-off$ operation.

Conventional $GaN-based$ transistors have been $HFETs$ using (0001) $c-plane$, on which polarization-induced charges produce a high-sheet carrier concentration at the hetero-interface as $2DEG$, even without any intentional doping. In the case of $-plane$ $AlGaN/GaN\ HFETs$, a $2DEG$ is naturally induced by positive polarization sheet charges at the $AlGaN/GaN$ hetero-interface. Therefore, it is difficult to achieve an $E-mode$ operation with $V_{th}>3\ V$.

On the other hand, $AlGaN/GaN$ heterostructures grown on nonpolar planes such as $m-$ and $a-planes$ have no polarization field. Thus, these planes are useful for realizing $E-mode\ AlGaN/GaN\ HFETs$ with $high-V_{th}$. Complete $normally-off$ operation of the $a-plane$ and $m-plane$ $AlGaN/GaN\ HFETs$ with a recessed $MIS-gate$ structure has been reported.[24,25]

7.2.5. $MOS-HEMT$

For $normally-off$ operation, $GaN\ MOSFETs$ are attractive since the operation of these is theoretically enhancement mode. $GaN\ MOSFETs$ can also realize lower gate leakage current compared with $AlGaN/GaN\ HFETs$. It has been demonstrated that it is possible to obtain good $normally-off$ operation and achieve high-breakdown voltages. As for these $MOSFETs$, reduced surface field ($RESURF$) zones were formed by ion implantation techniques. $RESURF$ zones are necessary to realize high-breakdown voltage of these devices. However, the resistance of $RESURF$ zones formed by ion implantation techniques was significantly high, because the activation of implanted ions was insufficient.

From 2008, by incorporating the merits of both a MOS channel and an $AlGaN/GaN$ heterostructure with high-mobility $2DEG$, $normally-off\ AlGaN/GaN$ metal oxide semiconductor hybrid field effect transistors ($MOSHFETs$) have been proposed.[2,26] This structure can obtain $normally-off$ operation by applying MOS channel, and it does not need to form $RESURF$ zone by ion implantation technique. Therefore, this structure has the possibility to realize $normally-off$ operation, low R_{on} and high-breakdown voltage.

Successful devices have been reported using this technique. In particular, Kambayashi *et al.*[6] reported an $AlGaN/GaN\ MOSHFETs$ on Si substrate with maximum drain current of over $100\ A$ the $R_{on,sp}$ of $9.3\ m\Omega cm^2$ and the breakdown voltage of over $600\ V$ were achieved. An analytical model for this device will be presented on section 1.4.

7.3. SENTAURUS $TCAD$ SIMULATIONS

To achieve and to optimize any of the aforementioned $normally-off$ techniques, it is very convenient and very useful to perform $2D\ TCAD$ simulations to predict the behavior of the device. Here we present an example of simulation for the first $normally-off$ strategy which is based on the gate recess.

7.3.1. INTRODUCTION

Synopsys $TCAD$ is a software suite that can perform multidimensional simulations on semiconductors devices, from the detailed design to the electrical characterization. The

device design devoted tool, Sentaurus Structure Editor, is able to create a multidimensional model with accurate reproduction of regions and profile placements. This multidimensional model can be inserted in the Sentaurus Device tool, to perform electrical simulations.

Sentaurus Device makes use of finite element techniques and several physical models to resolve the Poisson *eq.* (7-1) coupled with the current continuity *eq.*(7-2) and (7-3):[27]

$$\nabla \cdot \varepsilon \nabla \phi = -q(p - n + N_D - N_A) - \rho_{trap} \tag{7-1}$$

$$\nabla \cdot \overrightarrow{J_n} = qR_{net} + q\frac{\partial n}{\partial t} \tag{7-2}$$

$$-\nabla \cdot \overrightarrow{J_p} = qR_{net} + q\frac{\partial p}{\partial t} \tag{7-3}$$

Where R_{net} accounts for the net electron–hole recombination rate and the current density values are obtained from the drift-diffusion model.[28]

The challenge is not only technologic but also in the understanding and modeling of these devices. For example, $TCAD$ simulators include no model for $E - mode\ HEMTs$ or hybrid $MOS - HEMTs$. Even the physics of such devices must be further investigated.

7.3.2. $AlGaN/GaN$ BARRIER THINNING $TCAD$ SIMULATION (GATE RECESS)

This technique is based on the reduction of the $AlGaN$ barrier up to few nanometers-thick $AlGaN$ layer to reduce the $2DEG$ density (figure 7-1) and hence causing a shift of the V_{th} towards more positive values.

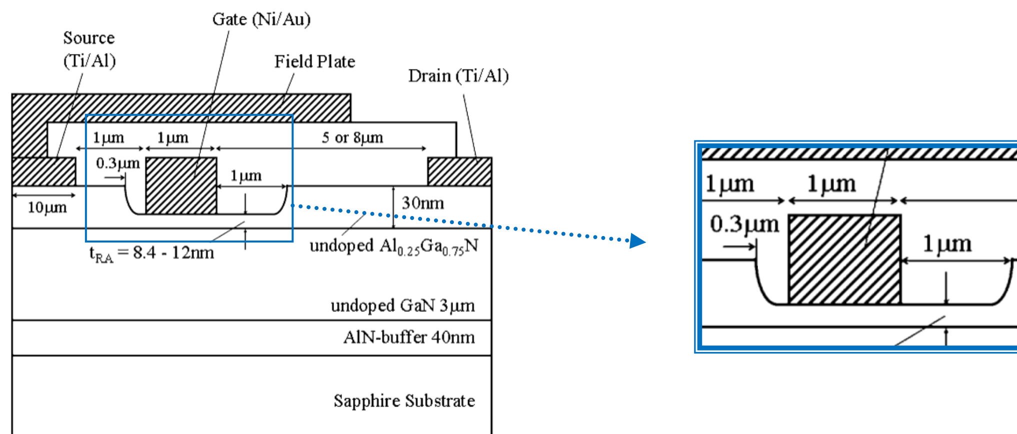

Figure 7-1. Adapted from Saito *et al.*[10] cross-section of fabricated $AlGaN/GaN\ HEMT$ with recessed-gate structure.

The original thickness of the $AlGaN$ layer (t_b) was in the order of $\sim 22\ nm$. The next simulation steps were further reducing this layer thickness to obtain a smooth right shift to $normally-off$ behavior. As shown in table 7-2, the expected right shift was achieved up to $t_b = 4\ nm$ which seems to be too small for either, the definition of the grid or typical tunneling distance are starting to play a role.

The V_{th} right shift progression is presented on figure 7-2 (a). It has been shown the nearly $normally-off$ performance for $t_b = 6\ nm$. Figure 7-2 (b) shown the simulated transconductance behavior for the $AlGaN$ thickness recess. The transconductance values increases when the $AlGaN$ layer is thinner due to the reduction of the gate capacitance in the $AlGaN$ barrier.

$Parameters$	$AlGaN/GaN\ HEMT$			
$t_b\ [nm]$	22	11	7	6
$V_{th}\ [V]$	−4.26	−1.42	−0.37	−0.18
$g_m\ [mS/mm]$	238	326	386	407

Table 7-2. V_{th} and g_m evolution with the $AlGaN$ thickness.

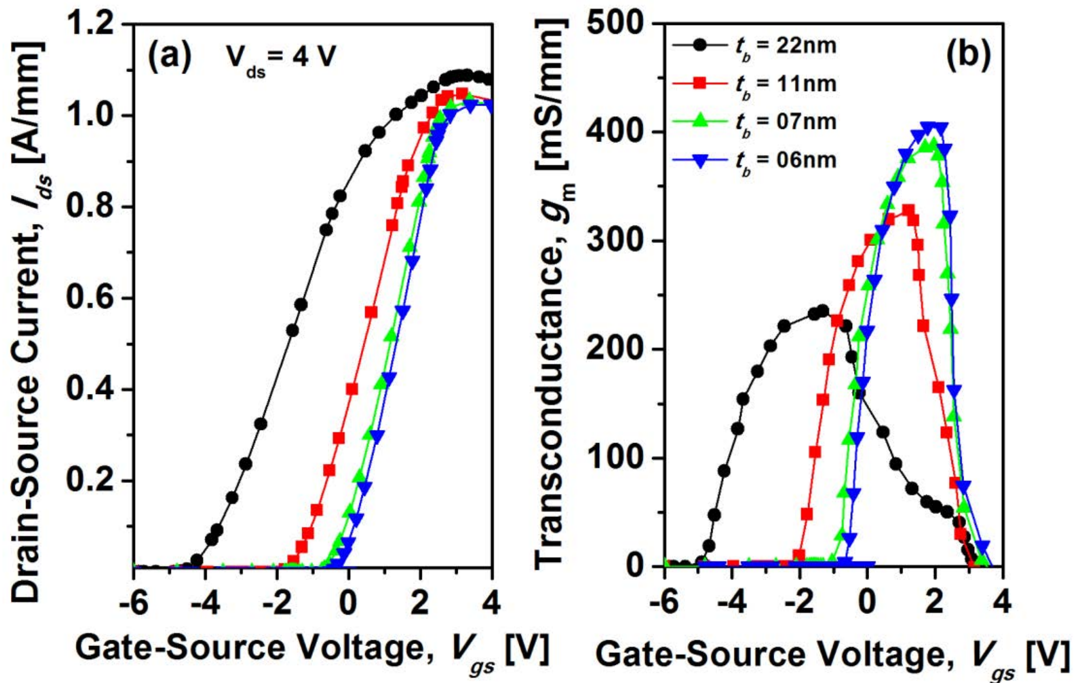

Figure 7-2. Simulated transfer curve with an $AlGaN$ thickness recess from 22 nm to 6 nm: (a) V_{th} drift to positive values and (b) transconductance value increases when thickness is reduced.

The simulation has been carried out in order to visualize the effect of reducing the $AlGaN$ barrier in the $2DEG$ properties. We explored the structures for the simplest case of $V_g = V_{ds} = 0\ V$.

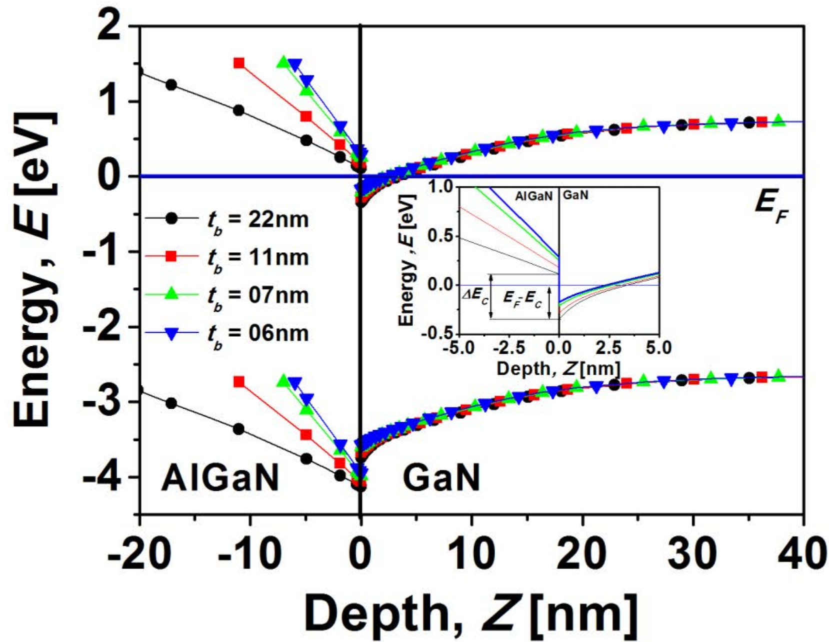

Figure 7-3. Simulated band diagram of the recessed $HEMTs$.

Figure 7-3 presents the different simulated band diagram of the recessed $HEMTs$. It can be seen that a t_b reduction results in a reduction of the quantum well energy $(E_c - E_F)$ for a given gate bias. The conduction band offset remains constant.

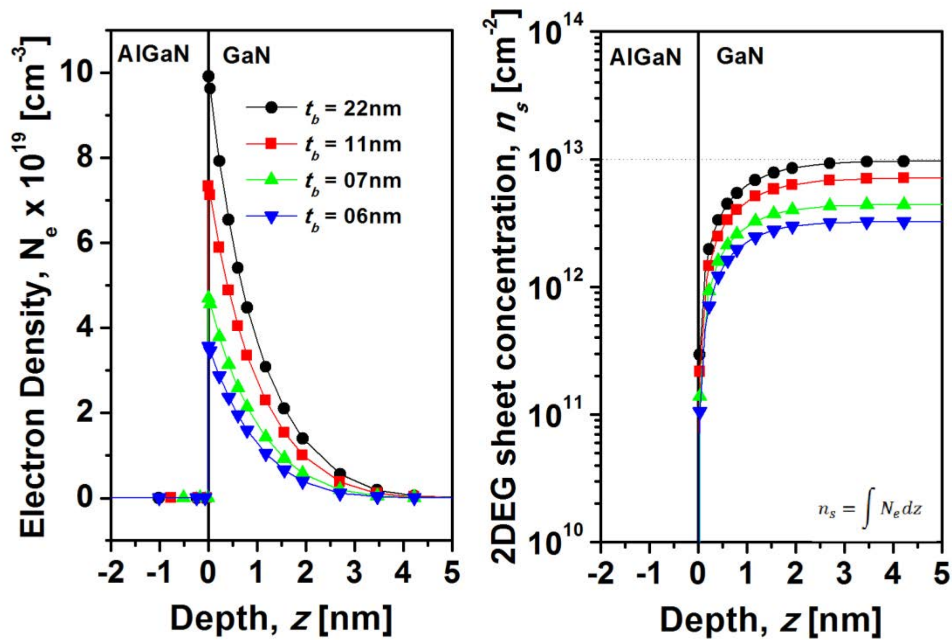

Figure 7-4. Simulated electron density and n_s.

This implies a reduction of the $2DEG$ electron density a sheet concentration, as it can be seen in figure 7-4 and figure 7-5.

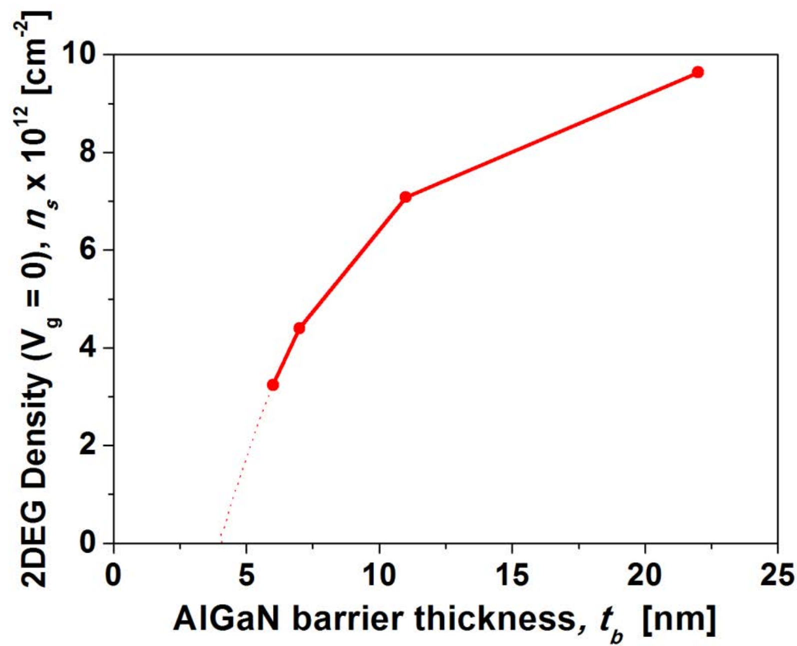

Figure 7-5. Simulated $2DEG$ density *vs* $AlGaN$ barrier thickness.

7.3.3. V_{th} vs BARRIER THICKNESS

The threshold voltage has been extracted from the slope of the transconductance of the figure 7-2. Then the V_{th} vs t_b plot was depicted.

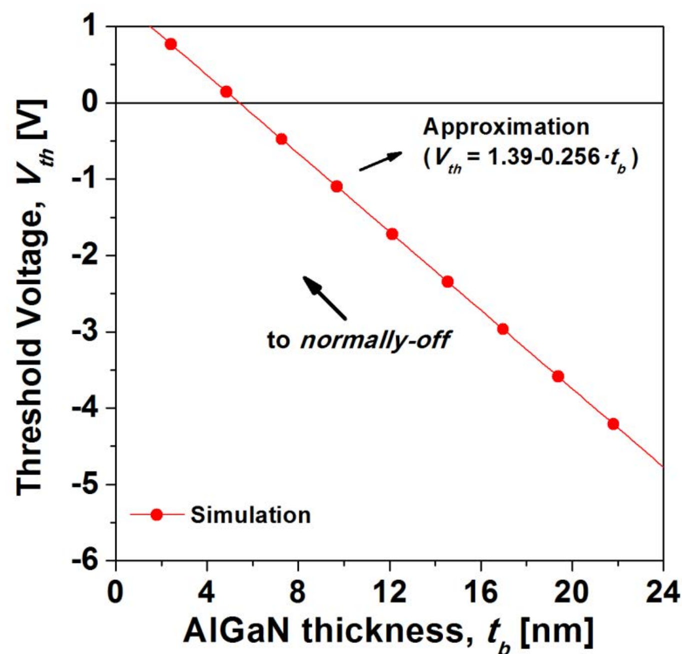

Figure 7-6. Simulation of the V_{th} vs t_b to achieve $normally-off$ mode.

As it is shown in figure 7-6 $normally - off$ mode is obtained for $V_{th} > 0\,V$ at $t_b < 5.3\,nm$. The predicted shift (extracted from the slope) was around $0.26\,V$ for every micron of recess.

$$\mathrm{V}_{th} = 1.39 - 0.256 \cdot t_b \tag{7-4}$$

7.3.4. DERIVATION OF THE PHYSICAL MODEL OF THE V_{th}

7.3.4.1. POLARIZATION FIELDS IN SENTAURUS $TCAD$

In Sentaurus $TCAD$[27] the strain model is based in the work of Ambacher *et al.*[29] Here, it captures the first-order effect of polarization vectors in $AlGaN/GaN\ HEMTs$: The interface charge induced due to the discontinuity in the vertical component of the polarization vector of material interfaces. The polarization vector is computed as follows:

$$\begin{bmatrix} P_x \\ P_y \\ P_z \end{bmatrix} = \begin{bmatrix} P_x^{sp} \\ P_y^{sp} \\ P_z^{sp} + 2d_{31}strain(c_{11} + c_{12} - 2c_{13}^2/c_{33}) \end{bmatrix} \tag{7-5}$$

Where P_j^{sp} denotes the spontaneous polarization vector, d_{31} is a piezoelectric coefficient $[cm/V]$, and c_{ij} are stiffness constants $[Pa]$. The value of the strain is computed as:

$$strain = (1 - relax)(a_0 - a)/a \tag{7-6}$$

Where a_0 represents the unstrained lattice constant [Å], a_s is the strained lattice constant [Å], and "relax" denotes a relaxation parameter. The quantities P_j^{sp}, d_{31}, and c_{ij} are defined by the crystal system. The polarization vector is first computed in crystal coordinates and is converted to simulation coordinates afterwards.

$$Q_{PE} = -\nabla P \tag{7-7}$$

Based on the polarization vector, the piezoelectric charge is computed according to *eq.* (7-7) and is added to the right-hand side of the Poisson equation:

$$\nabla \varepsilon \cdot \nabla \phi = -q(p - n + N_D - N_A + Q_{PE}) \tag{7-8}$$

The diagonal stress tensor is hence in the basis of the strain-induced polarization. The ground-state properties in the strain-free case are obtained by a minimization of the total energy with respect to the two strained lattice constant c_s and a_s as well as the unit cell internal parameter u_0 of the wurtzite structure. As perturbations we consider biaxial or uniaxial strain (or stress) with an orientation parallel to the c axis of the crystal. The accompanying deformations conserve the C_{6v}^4 space-group symmetry. Consequently, the strain tensor ε_{ij} is diagonal and possesses the components:

$$\varepsilon_{xx} = \varepsilon_{yy} = (a - a_0)/a_0 \quad (7\text{-}9)$$

$$\varepsilon_{zz} = (c - c_0)/c_0 \quad (7\text{-}10)$$

In the limit of small deviations from the equilibrium, Hooke's law gives the corresponding diagonal stress tensor σ_{ij} with the elements:

$$\sigma_{xx} = \sigma_{yy} = (c_{11} + c_{12})\varepsilon_{xx} + c_{13}\varepsilon_{zz} \quad (7\text{-}11)$$

$$\sigma_{zz} = 2c_{13}\varepsilon_{xx} + c_{33}\varepsilon_{zz} \quad (7\text{-}12)$$

In the previous equations four of the five independent stiffness constants c_{ij} of the considered wurtzite crystal occur. The modifications of the σ_{ij} relationships by the built-in electric field due to the spontaneous and piezoelectric polarization are neglected because of their smallness. A homogeneous biaxial stress in the plane perpendicular to the c axis of the wurtzite lattice is described by constant forces in this plane, $\sigma_{xx} = \sigma_{yy}$, and vanishing forces along the c axis, $\sigma_{zz} = 0$. Then Hooke's law gives a relationship between the strain components:

$$\varepsilon_{zz} = -R^B\varepsilon_{xx} = -\frac{2c_{13}}{c_{33}}\varepsilon_{xx} \quad (7\text{-}13)$$

Likewise, this deformation is also referred to as biaxial strain. In order to determine the biaxial relaxation coefficient R^B, we choose lattice constants a close to the equilibrium one and, in each case, minimize the total energy of the system with respect to the hexagonal strained lattice constant c_s and the unit cell internal parameter u_0 to obtain the unstrained lattice value of c_0. The $in-plane$ stress is related to the $in-plane$ strain by the biaxial modulus. This reads $\sigma_{xx} = Y\varepsilon_{xx}$, and the biaxial modulus is given in terms of the elastic stiffness constants as:

$$Y = c_{11} + c_{12} - \frac{2c_{13}^2}{c_{33}}\varepsilon_{xx} \quad (7\text{-}14)$$

7.3.4.2. CLOSE-FORM FOR THE $2DEG$ DENSITIES vs POLARIZATION FIELDS

Free electrons tend to compensate the high-positive polarization induced sheet charge at the $AlGaN/GaN$ interface. The maximum sheet carrier concentration located at these interfaces of the nominally undoped structures is expected to be:

$$n_s(x) = \frac{P_T(x)}{q} - \left(\frac{\varepsilon_0 \varepsilon(x)}{t_b\, q^2}\right)[\Phi_B(x) + E_F(x) - \Delta E_C(x)] \tag{7-15}$$

Where P_T is the piezoelectrically induced charge density, t_b is the width of the $Al_xGa_{1-x}N$ barrier, Φ_B is the Schottky barrier of a gate contact, E_F is the Fermi level with respect to the GaN conduction band edge energy, and ΔE_C is the conduction band offset at the $AlGaN/GaN$ interface. Some useful approximations can be used to compute the sheet carrier concentration:

$$\varepsilon(x) = -0.5x + 9.5 \tag{7-16}$$

$$\Phi_B(x) = 1.3x + 0.84 \tag{7-17}$$

$$E_F(x) = E_0(x) + \frac{\pi\hbar^2}{m^*} n_s(x) \quad and \quad E_0(x) = \left[\frac{9\pi\hbar e^2}{8\varepsilon_0\sqrt{8m^*}} \frac{n_s(x)}{\varepsilon(x)}\right]^{2/3} \tag{7-18}$$

$$\Delta E_c(x) = 0.7\left[E_g(x) - E_g(0)\right] \tag{7-19}$$

$$E_g(x) = \; xE_{g,AlN} - (1-x)E_{g,GaN} - x(1-x) \tag{7-20}$$

Numerical computation leads to the extraction of the value of n_s.

7.3.4.3. SIMPLIFIED, IDEAL V_{th} VS $2DEG$ DENSITY

In a first appoximation[30] the intercept point is the gate barrier height plus the conduction band offset which is consistent with the default value of $\Phi_B = 1.5\ eV$ given by the simulator.

$$V_{th} = \Phi_B - \Delta E_c - \frac{qP_T}{\varepsilon}\, t_b \tag{7-21}$$

The $2DEG$ carrier density is given by (in analogy to a $MOSFET$ device):

$$n_s = \frac{\varepsilon\left(V_{gs} - V_{th}\right)}{qt_b} \tag{7-22}$$

Derived from a simplifier approximation of the Ambacher *et al.*[29] procedure and neglecting the Fermi energy value for $V_g = 0$.

$$V_{th} = -\frac{q\,t_b}{\varepsilon} n_s \tag{7-23}$$

$$V_{th}(x) = \Phi_B(x) - \Delta E_C(x) - \frac{qP_T}{\varepsilon} t_b \tag{7-24}$$

Hence in first approximation the threshold voltage of an $AlGaN\ HEMT$ depend on the following parameters: the barrier height, the conduction band-offset, the $AlGaN/GaN$ barrier thickness and the polarization induced charges. This very simple equation has been used in the $HEMT$ model expression given in $chapter\ V$.

7.3.4.4. Vth EXPRESSION INCLUDING REAL EFFECTS

In this model the effect of the surface traps, bulk traps or the doping has not been considered. From Cai *et al.*[14] a more complete expression for the threshold voltage was given by:

$$\mathrm{V}_{th} = \Phi_B/q - \frac{qP_T}{\varepsilon} t_b - \Delta E_c/q + E_{f0}/q - \frac{q}{\varepsilon}\int_0^{t_b} dz \int_0^{z} N_{si}(z)dz - qt_b n_{st}/\varepsilon - qn_b/C_b \tag{7-25}$$

Where E_{f0} is the difference between the intrinsic E_F and the conduction band edge of the GaN channel. The $N_{si}(z)$ is the Si-doping concentration, ΔE_c is the conduction-band offset at the $AlGaN/GaN$ heterojunction, ε is the dielectric constant of $AlGaN$, n_{st} net-charged surface traps per unit area, n_b is the effective net-charged buffer traps per unit area and C_b effective buffer-to-channel capacitance per unit area.

7.4. HYBRID $MOS-HEMT$ MODELING

7.4.1. INTRODUCTION

Since the demonstration of the first $GaN-based\ HEMT$ switches,[31] rapid progress has been made in the development of $GaN-based\ HEMT$ devices. Lateral $GaN\ MOSFETs$ with relatively high-channel mobility (a peak of $170\ cm^2/Vs$) and high-blocking voltage ($2.5\ kV$) have been demonstrated[32] with an acceptable quality SiO_2/GaN interface are viable.

Therefore GaN $MOSFET$ has the advantages of $normally - off$ operation without current collapse problems. However, GaN $MOSFET$ currently exhibits (and probably it will be an unsolved major problem as in the case of SiC) modest inversion channel mobility (below 300 cm^2/Vs) due to the presence of interface states, surface roughness and other scattering mechanisms. A way to around this could be the incorporation of $AlGaN/GaN$ heterostructure into the $RESURF$ region of GaN $MOSFETs$. A hybrid $MOS - HEMT$[2,6,7,26] has the advantage of both the MOS gate control and the high-mobility $2DEG$ in $AlGaN/GaN$ drift region. A cross-section of the hybrid $MOS - HEMT$ analyzed here is presented in figure 7-7. This hybrid $MOS - HEMT$ has a tremendous potential to be one of the key advanced $GaN - based$ power switches.

In this section, we present simple analytical modeling for understanding the influence of the main design parameters on the R_{on} of a hybrid $MOS - HEMT$. Our starting point is physical based models for $HEMT$ and $MOSFETs$ which are subsequently combined to determine the R_{on} of the hybrid $MOS - HEMT$.

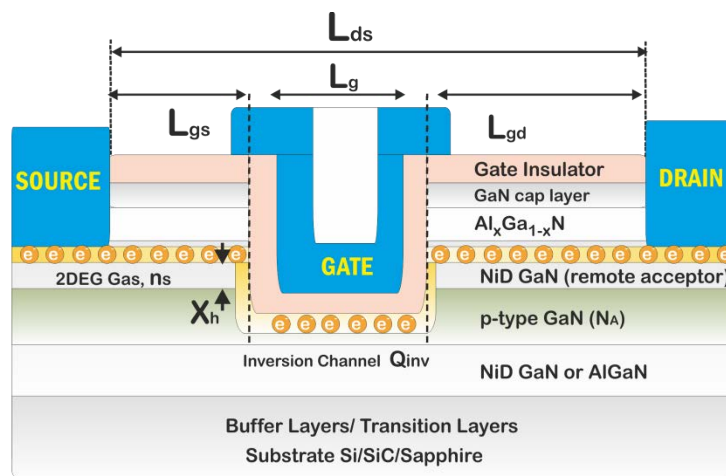

Figure 7-7. Cross-sectional view of a hybrid $MOS - HEMT$

7.4.2. GaN $MOSFET$ AND $AlGaN/GaN$ $HEMT$ R_{on}

One great advantages of GaN as power semiconductor substrate is that transistor effect could be achieved by defining the inversion channel under a MOS gate or by taking advantage of the hetero-interface $2DEG$ charge centroid (figure 7-8). Both mechanisms are discussed briefly in the next section. In $MOSFET$ and $HEMT$ transistors R_{on} have been linked to the channel layout and electron mobility properties by analytical relationships for low transverse fields:[33]

$$R_{on}(MOSFET) = R_{on,M} = \left[\frac{L_{ch}}{\mu_n C_{ins}(V_{gs} - V_{th})} + \frac{L_D}{q\mu_B N_D X_j}\right](L_{ch} + L_D) \quad (7\text{-}26)$$

$$R_{on}(HEMT) = R_{on,H} = \frac{L_{ds}^2}{q\mu_{2DEG} n_s} \quad (7\text{-}27)$$

Where μ_n is the mobility of carriers in the inversion channel, V_{gs} the gate to source voltage and V_{th} is the threshold voltage. The gate insulator capacitance per unit area is named C_{ins} and expressed by:

$$C_{ins} = \varepsilon_r \varepsilon_0 t_{ins}^{-1} \quad (7\text{-}28)$$

Where ε_r is the gate insulator dielectric constant and t_{ins} is the gate insulator thickness.

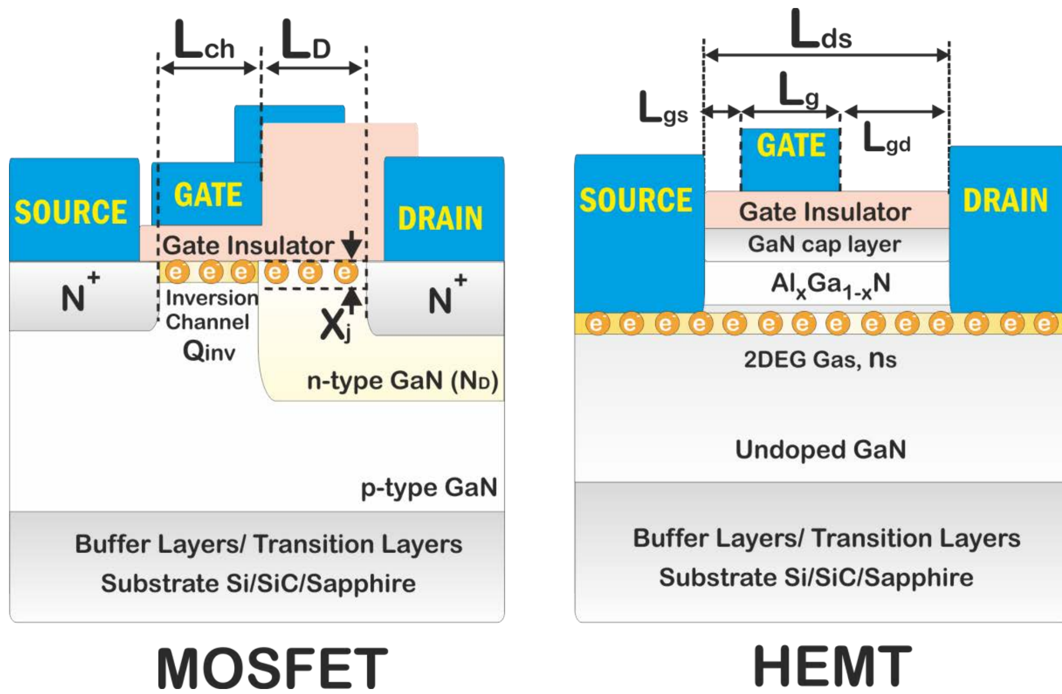

Figure 7-8. Cross-sectional view of a power $LD-MOSFET$ and a power $HEMT$.

The second term of R_{on} $(MOSFET)$ is included if a low doped drift region (or extended drain) to improve the breakdown voltage is considered $(LD-MOSFET)$. There, L_D is the drift region length, N_D is the doping of the drift region, μ_B is the bulk $n-type$ extended drain mobility (μ_B is a function of N_D and the temperature) and X_j is the carrier flow depth in the extended drain region. For the $HEMT$, the sheet carrier density on the $2DEG$ (n_s) may be determined by means of Hall bar measurements and/or capacitance measurements. The μ_{2DEG} is in this case the mobility of electrons in the $2DEG$ channel. The C_{ins} is the gate oxide capacitance per unit area.

7.4.3. MOS INVERSION CHANNEL MOBILITY

The $MOSFET$ principle of operation in GaN is not substantially different from one transistor defined on Si which is well known. The main but crucial difference is the lack of a high-quality native thermal oxide which results in a poor interface. The mobility of carriers in the inversion channel of a $MOSFET$ device is always a part of the μ_B. The widely accepted model consisting of the first three terms of $eq.$ (7-29) provides a good description of channel mobility for Si $MOSFETs$:[34]

$$\mu_{MOS} = \left[\frac{1}{\mu_B} + \frac{1}{\mu_{ac}} + \frac{1}{\mu_{sr}} + \frac{1}{\mu_c}\right]^{-1} \tag{7-29}$$

There, μ_{ac} is the carrier mobility limited by the acoustic phonons scattering and μ_{sr} is the carrier mobility limited by surface roughness scattering. It has been proposed[34-36] mobility models for describing the mobility degradation observed in $MOSFET$ devices due to Coulomb scattering effects at interface traps. Generally, in GaN and SiC $MOSFETs$ this interface trap Coulomb scattering limiting mechanism is so relevant that the approximation $\mu_n(MOSFET) \simeq \mu_c$ could be used, in particular at the lower gate bias and at low temperature ($T = 25$ °C). Phenomenologically, it had been demonstrated[34] that MOS inversion mobility in a highly defective $GaN/insulator$ interface could be well fitted by determining Q_{inv} and Q_{trap}:

$$\mu_c = T\frac{A}{Q_{trap}} + NT^{\alpha_c}\frac{Q_{inv}^{\beta_c}}{Q_{trap}} \simeq NT^{\alpha_c}\frac{Q_{inv}^{\beta_c}}{Q_{trap}} \tag{7-30}$$

Where A and N are fitting constants, α_c and β_c are empirical constants for describing the screening of the scattering charges by the mobile charges in the inversion layer and experimentally determined to be $\alpha_c = \beta_c \approx 1$. This expression is in complete agreement with complex theoretical models. For example, if one assume a fixed charge distribution of ionized traps on the interface and treating the random spatial fluctuations of charge density as a quantum mechanics perturbation.[37] The free carrier screening effect introduces the dependence on the inversion charge.[35] It is worth to mention that a peculiarity of the MOS system in GaN is the possible presence of polarization charges that also could provoke some additional deviations of the MIS classic theory.

7.4.4. $AlGaN/GaN$ $2DEG$ CHANNEL MOBILITY AT RT AND ABOVE

The physics behind the $HEMT$ transistor is notably different. It has been suggested[38] that surface $AlGaN$ donor-like traps are the source of the electrons in the $2DEG$ channel, being these electrons driven into the channel by the strong polarization fields. Effectively, the positively charged donors in the $AlGaN$ produce an electric field which creates a potential well in the GaN buffer, confining electrons to a narrow strip at the interface, and leading to a quantization of the energy-band structure into sub-bands. The main scattering mechanisms in a $2DEG$ channel are well reported.[38] The $2DEG$ mobility is modelled analytically as the sum of several contributions including acoustic deformation-potential, piezoelectric, polar optic phonon, alloy disorder, interface roughness, dislocation and remote modulation doping scattering. Therefore, the total relaxation time could be calculated as the sum of the relaxation times due to each scattering process following again the Matthiessen's Rule. At temperatures above 80 K, the validity of this relation becomes questionable due to the relaxation-time approximation made for inelastic optical phonon scattering. However, the polar optical phonon scattering ($\mu_n(HEMT) \simeq \mu_{po}$) is the dominant scattering mechanism for the $2DEG$ in a wide temperature range since the impurity scattering is minimized, due to spatial separation of electrons and ionized impurities, being especially true for temperatures above 300 K.

Eq. (7-31) describes this mobility for a $2DEG$ using the conventional relaxation-time approximation for the case when the optical-phonon energy is greater than the thermal energy:[39]

$$\mu_{2DEG,po} = \frac{\left(\varepsilon_{s,\infty}^{-1} - \varepsilon_s^{-1}\right)^{-1} k_0 \hbar^2}{2\pi q \omega_0 m^{*2} F(k_0)} \left(e^{\frac{\hbar\omega_0}{k_B T}} - 1\right) \left(1 + m^* k_B T \left(\frac{1 - e^{-\frac{\pi\hbar^2 n_s}{m^* k_B T}}}{\pi\hbar^2 n_s}\right)\right) \tag{7-31}$$

$$where\ F(k_0) = \frac{b(8b^2 + 9k_0 b + 3k_0^2)}{8(k_0 + b)^3} \quad and \quad b = \left(\frac{33\pi m^* q^2 n_s}{2k_o \hbar^2}\right)^{1/3} \tag{7-32}$$

Here $\varepsilon_{s,\infty}$ is the permittivity of the semiconductor at high-frequencies and $\hbar\omega_0$ is the energy of the polar optical phonon. The wave vector of the polar optical phonon is computed by:

$$k_0 = \sqrt{2m^* \omega_0 / \hbar} \tag{7-33}$$

In this case, the form factor $F(k_0)$ depends on the channel geometry and in the narrow channel near the hetero-interface. As for the case of $MOSFETs$, simpler empirical relationships for the polar-optical mobility have been proposed:[40]

$$\mu_{2DEG,po} \simeq \frac{C}{n_s^{\delta 1} T^{\gamma 1}} + \frac{D}{n_s^{\delta} T^{\gamma}} \simeq \frac{C}{n_s^{\delta} T^{\gamma}} \tag{7-34}$$

Eq. (7-34) may be considered as an interpolation between the temperature dependence near $77\ K$ $(\delta 1;\ \gamma 1)$ and the temperature dependence near $300\ K$ $(\delta;\ \gamma)$. At elevated temperatures, *eq.* (7-31) simplifies then to the last term.

7.4.5. $MOSFET\ vs\ HEMT$

Eqs. (7-30) and (7-34) are physical-based expressions for describing the electron transistor mobility on the MOS inversion and $2DEG$ channel at elevated temperatures, respectively. Q_{trap} and Q_{inv} may be calculated following the procedure described in the literature.[34] A charge-sheet model simplifies the calculation of inversion charge assuming that the inversion layer is a charge sheet of infinitesimal thickness. The charge-sheet model equations are also used to compute the average effective field in the inversion layer.

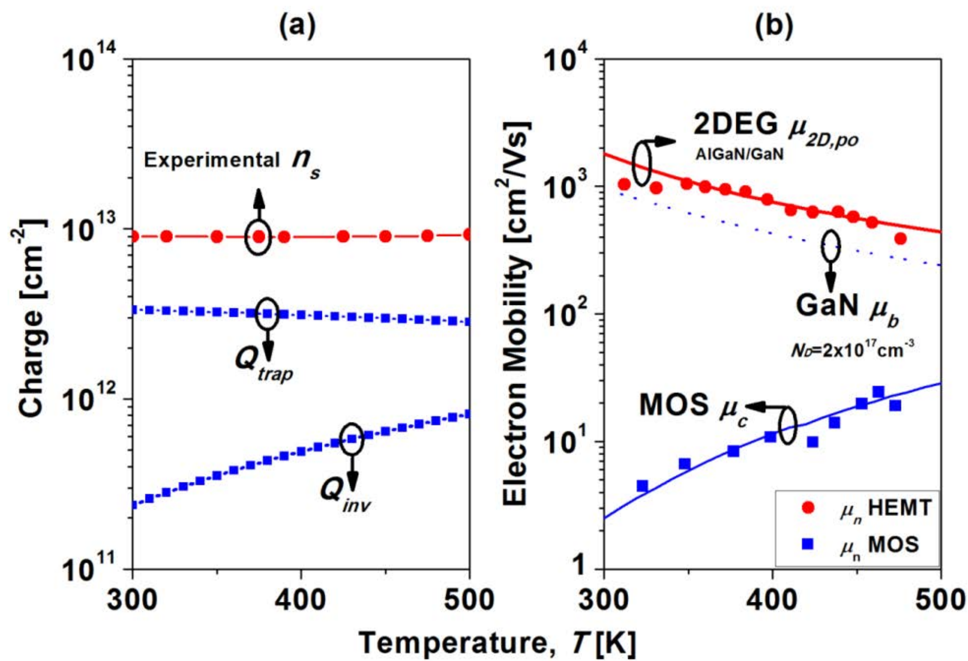

Figure 7-9. (a) Computed Q_{trap} and Q_{inv} and experimental[41] n_s vs temperature. (b) Experimental (symbols) vs simulated (solid lines) electron mobility for $MOSFETs$ and $HEMTs$.

The reason for the large mobility difference depicted in figure 7-9 is that, in the $MOSFET$, conduction electrons occupy the same space region than ionized impurities and hence, channel mobility is limited (in the ideal case of a perfect MOS interface) at least by μ_B.The $MOSFET$ mobility is in practice a fraction of the semiconductor bulk mobility due to scattering effects at the MOS interface, mainly Coulomb scattering at interface traps, that is dramatically relevant in $GaN-based$ $MOSFETs$. In $HEMTs$ polar optical phonon limited mobility is already higher than the bulk mobility for GaN under the same transverse electric field.

7.4.6. $AlGaN/GaN$ HYBRID $MOS-HEMT$ ANALYTICAL MOBILITY MODEL

The hybrid $MOS-HEMT$ model presented here is based in the assumption that the device is formed by $2DEG$ channels between source/gate and gate/drain in series with the inversion channel below the gate. In the structures proposed by Kambayashi *et al.*[6] the MOS channel is formed in a Mg $doped$ $p-type$ region with a doping of $1.0\times 10^{17}cm^{-3}$. Therefore the expression for the $R_{on,sp}$ can be rewritten as the sum of the different terms contributing to the R_{on} hybrid $MOS-HEMT$ $\left(R_{on}(HMOS\text{–}HEMT) = R_{on,HM-H}\right)$:[10]

$$R_{on,HM-H} = \left[\frac{L_{gs}}{q\mu_n n_s} + \frac{L_{gd}}{q\mu_n n_s} + \frac{L_g}{\mu_n C_{ins}(V_{gs}-V_{th})} + 2R_h\right] \times \left(L_{gs}+L_{gd}+L_g+2X_h\right) \tag{7-35}$$

Parameters	Units	Values	References
HEMT			
L_{gs}	μm	1.5	
L_{gd}	μm	6.0	
μ_{2DEG}	cm^2/Vs	1400	$Typical$
n_s	cm^{-2}	1.0×10^{13}	$Typical$
MOSFET			
L_g	μm	1.0	
μ_{MOS}	cm^2/Vs	$20-200$	[7,2,32,34]
C_{ins}	F/cm^2	8.6×10^{-8}	$(40\ nm\ SiO_2)$
V_{th}	V	1.0	

Table 7-3. Parameters included in the computation of the $R_{on,sp}$ of the hybrid $MOS-HEMT$.

The term R_h describes the additional resistance coming from the inversion channel formed on the non-intentionally doped (NiD) GaN region between the $2DEG$ and the $p - type$ GaN of length X_h (figure 7-7). In the simplest picture it could be considered that the NiD region is thin enough for being comparable to the quantum well width where is confined the $2DEG$ and $2X_h \ll L_{gs} + L_{gd} + L_g$. Therefore, attending to this simplified view we consider that there is direct contact between the $2DEG$ below the $AlGaN$ and the inversion channel on the $p - type$ region. Then the previous equation can be reduced to:

$$R_{on,HM-H} \simeq \left[\frac{L_{gs} + L_{gd}}{q\mu_{2DEG}n_s} + \frac{L_g}{\mu_{MOS}C_{ins}(V_{gs} - V_{th})}\right](L_{gs} + L_{gd} + L_g) \quad (7\text{-}36)$$

The hybrid $MOS - HEMT$ $R_{on,sp}$ depends on the layout parameters $(L_{gs}, L_g\ and\ L_{gd})$, the $n_{s,2DEG}$ and in the inversion channel $(C_{ins}(V_{gs} - V_{th}))$ and their respective mobility values, μ_{2DEG} and μ_{MOS}. In the simplest of $MOSFET$ theories (which is in the basis of the MOS term of $eq.$ (7-26))[42] Q_{inv} is obtained from a standard parallel-plate capacitor where the charge on the capacitor plates is equal to the capacitance times the voltage drop between the plates, expressed by:

$$Q_{inv} = q^{-1}C_{ins}(V_{gs} - V_{th}) \quad (7\text{-}37)$$

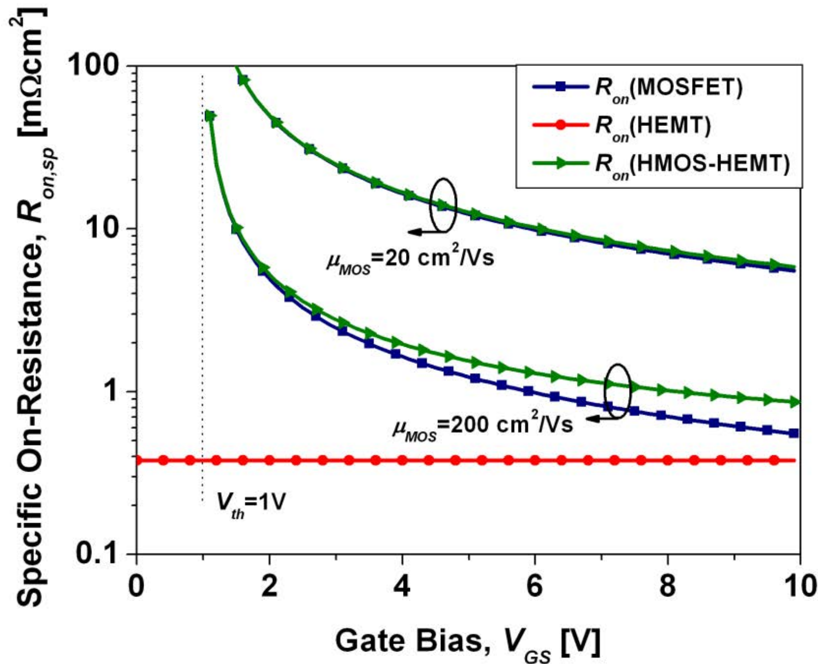

Figure 7-10. Computed specific on-resistance *vs* gate bias or the $MOSFET$, $HEMT$ and hybrid $MOS - HEMT$ for MOS mobilities of 20 cm^2/s and 200 cm^2/s.

The charge added to the gate is balanced by an increase in the inversion layer charge. This expression is already useful because can provide valuable information to the device designers. Computations have been performed taking into account the values commonly reported on the literature on the previous values and listed in table 7-3.

A conventional device layout of $1.5/6.0/1.0\ \mu_m$ $(L_{gs}/L_{gd}/L_g)$ has been chosen which is typical of power $HEMTs$ for the range of the $600\ V$. For a given gate bias, the hybrid $MOS-HEMT$ is strongly dependent on MOS channel mobility which is presumably the more difficult parameter to control.

As it can be seen in figure 7-10 the R_{on} increases as the channel mobility reduces from the state-of-the-art value of $200\ cm^2/Vs$[32] to values of $20-100\ cm^2/Vs$. To deposit an oxide on the selectively etched channel region would result in an oxide interface with rougher interfaces and with a higher density of interface states. For this reason the channel mobility should be lower than in the best epi GaN material.

One straightforward method of reducing the on-resistance is to reduce the MOS channel length for a given MOS mobility as it is shown in figure 7-11. It can be seen from the figure that for the smaller MOS gates ($L_g < 1\ \mu_m$) the R_{on} value approaches to the one from the $HEMT$ even for a reduced value of the channel electron mobility of $200\ cm^2/Vs$. A way of reducing further the channel R_{on} is shown in figure 7-12 using insulators with higher dielectric constant. It has been calculated the R_{on} for an hybrid $MOSHEMT$ ($L_g = 1\ \mu_m\ and\ \mu_{MOS} = 50\ cm^2/Vs$) for SiO_2 and different common $high-k$ dielectrics. The dielectric constant is 7.4, 10.0 and 20.0 for Si_3N_4, Al_2O_3 and HfO_2, respectively.[43-45] For a given gate insulator thickness the lower R_{on} is achieved for the dielectrics with the higher dielectric constant.

For investigating the temperature behavior of the R_{on}, it is required to make use of the physical models as the described previously section. If we assume that all the scattering mechanism in the MOS channel is Coulomb scattering in the interfacial traps, the hybrid $MOS-HEMT\ R_{on}$ is:

$$R_{on,HM-H} \simeq \left[C'\left(L_{gs}+L_{gd}\right)\frac{T^{\gamma}}{qn_s^{1-\delta}(T)} + N'L_g\frac{Q_{trap}(T)}{qQ_{inv}^2(T)T^{\alpha_c}}\right]\left(L_{gs}+L_{gd}+L_g\right) \tag{7-38}$$

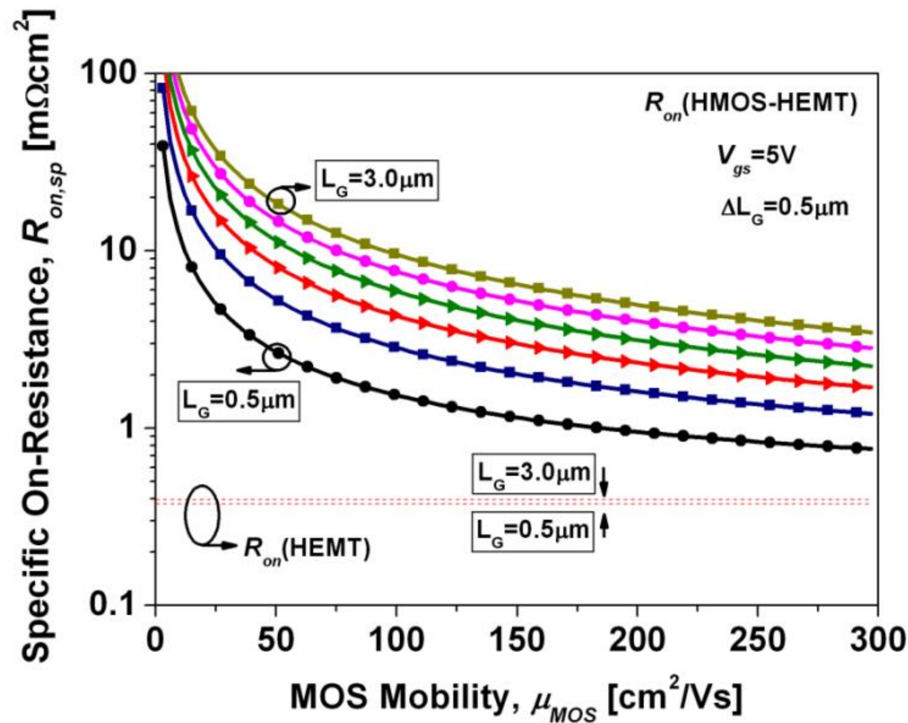

Figure 7-11. Hybrid $MOS - HEMT$ computed $R_{on,sp}$ vs MOS mobility value for different channel lengths.

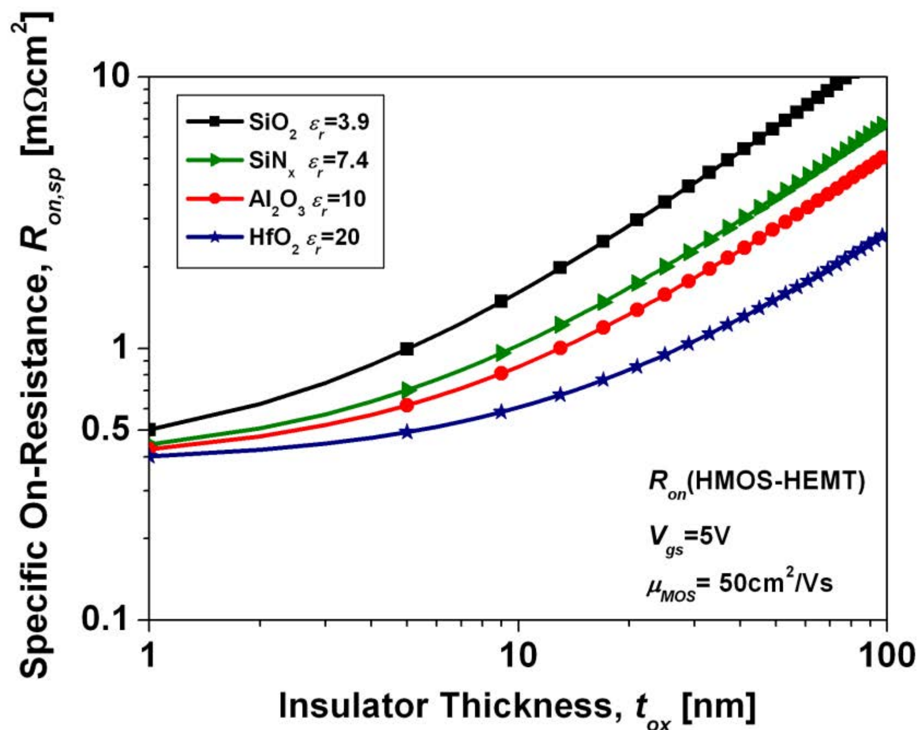

Figure 7-12. Hybrid $MOS - HEMT$ computed $R_{on,sp}$ vs insulator thickness for different dielectrics (SiO_2, Si_3N_4, Al_2O_3 and HfO_2).

In figure 7-9 (a) is presented the typical temperature dependence of $Q_{trap}(T)$, $Q_{inv}(T)$ and $n_s(T)$. It can be seen that both $n_s(T)$ and $Q_{trap}(T)$ are a weak function of the

temperature, which has been verified experimentally.[41] In the case of $Q_{trap}(T)$ the temperature dependence is due to the band-gap narrowing with temperature, which is considered a second order effect in this model. For $Q_{inv}(T)$ it has been defined a power law of the form:

$$Q_{inv}(T) = Q_{inv,0}(T/T_0)^{\zeta} \tag{7-39}$$

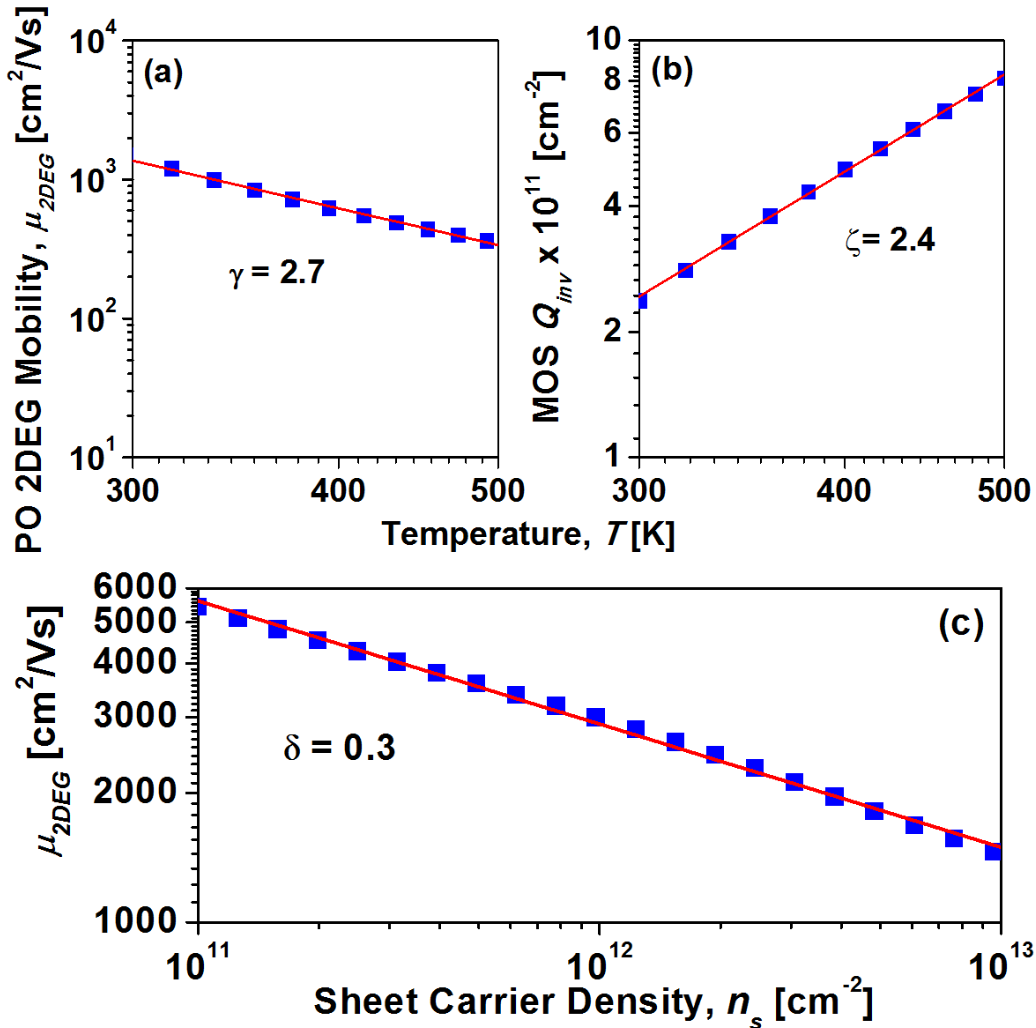

Figure 7-13. $HEMT$ **mobility dependence on: (a) Temperature and (c)** n_s**. (b)** $MOS\ Q_{inv}$ **dependence on temperature.** $Q_{inv}(T)$ **is computed by a temperature dependent charge-sheet model for** $V_{gs}-V_{th}=4\,V$ **giving a value of** $\zeta = 2.4$**.[34]** $HEMT$ **mobility constants** $\gamma = 2.7$ **and** $\delta = 0.3$ **have been fitted to the computed** *eq.* **(7-31) for** $n_s = 1.0\times10^{13}cm^{-2}$ **and** $T = 300\ K$**, respectively.**

Where $T_0 = 300\ K$. $Q_{inv}(T)$ is computed by temperature dependent charge-sheet model for $V_{gs} - V_{th} = 4\,V$ giving a value of $\zeta = 2.4$.[34] $HEMT$ mobility constants $\gamma = 2.7$ and $\delta = 0.3$ have been fitted to the computed *eq.* (7-31) $(\hbar\omega_0 = 91.2\ meV,$

$m^*/m_0 = 0.2\,, \varepsilon_s = 8.9\ and\ \varepsilon_{s,\infty} = 5.35\,)$ for $n_s = 1.0 \times 10^{13}\ cm^{-2}$ and $T = 300K$, respectively (figure 7-13). The hybrid $MOS - HEMT$ R_{on} is then:

$$R_{on,HM-H} \simeq \left[C'(L_{gs} + L_{gd})\frac{T^{\gamma}}{qn_s^{1-\delta}} + N'L_g\frac{Q_{trap}}{Q_{inv,0}^2 T^{1+2\zeta}}\right](L_{gs} + L_{gd} + L_g) \quad (7\text{-}40)$$

In figure 7-14 is simulated presented the dependence of the R_{on} with temperature for $R_{on,H}$, $R_{on,M}$ and $R_{on,HM-H}$. Table 7-4 shown the parameters used in the simulations:

Parameter	Units	Value
n_s	cm^{-2}	1.0×10^{13}
$C' = C^{-1}$	$Vs/cm^{2+\delta}K^{\gamma}$	1.84×10^{-14}
$\mu_{2DEG,po}$	cm^2/Vs	1400
$Q_{inv,0}$	cm^{-2}	2.4×10^{11}
$\underline{High}$		
$Q_{trap,High}$	cm^{-2}	1.5×10^{12}
$\mu_{MOS,High}(300K)$	cm^2/Vs	50
$N'_{High} = N_{High}^{-1}$	$K^{\alpha}V\,s/cm^2$	1.04
$\underline{Limit}$		
$Q_{trap,Limit}$	cm^{-2}	0.7×10^{12}
$\mu_{MOS,Limit}(300K)$	cm^2/Vs	200
$N'_{Limit} = N_{Limit}^{-1}$	$K^{\alpha}V\,s/cm^2$	0.52

Table 7-4. Summary of the parameters used in the simulations.

As it can be inferred from figure 7-14, the simulations suggest that the hybrid $MOS - HEMT$ exhibits better stability at elevated temperatures than the $MOSFET$ and the $HEMT$. The reason is that we have two competing mechanisms (that have the opposite behavior with temperature) establishing the forward current in the hybrid $MOS - HEMT$.

The MOS Coulomb scattering mobility has a positive behavior with T which gives the reduction of the on-resistance with T. Oppositely, $HEMT$ phonon scattering mobility has a negative behavior with T and the hybrid $MOS - HEMT$ dependence should be determined by the trade-off between both mechanisms.

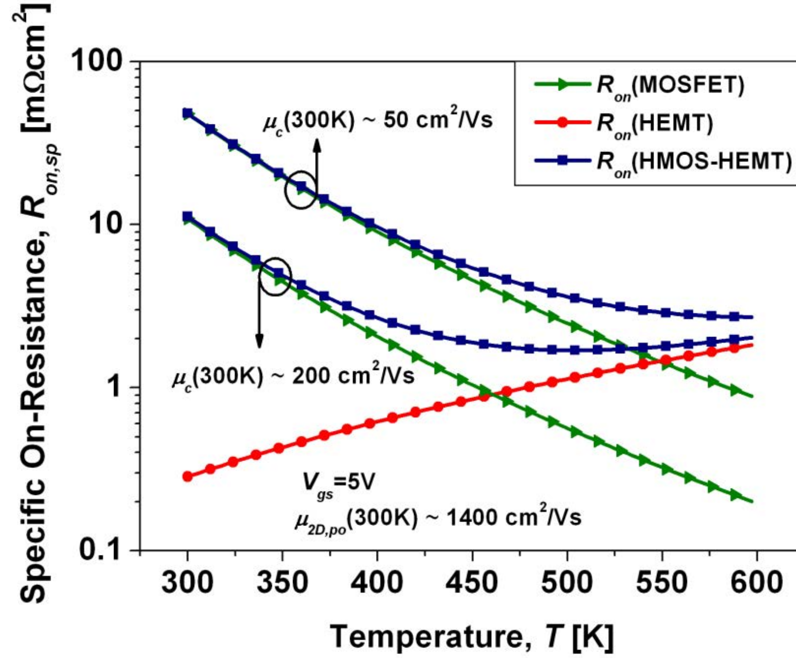

Figure 7-14. Computed $R_{on,sp}$ vs temperature for the $MOSFET$, $HEMT$ and hybrid $MOS-HEMT$.

In fact, this temperature behavior competition within the hybrid $MOS-HEMT$ may be engineering somehow to mitigate the temperature degradation inevitable in pure $HEMT$ devices due to the phonons and then, resulting in enhanced thermal stability. Oka *et al.*[2] presented a mobility profile extracted from the transconductance:

$$g_m = \frac{\partial I_{ds}}{\partial V_{gs}} = V_{ds}W\left(L_{gs} + L_{gd} + L_g\right)\frac{\partial(R_{on}^{-1})}{\partial V_{gs}} \tag{7-41}$$

Which shows a $120\ cm^2/Vs$ mobility peak at $V_{gs} = 6\ V$ and then abruptly decreases to around $60\ cm^2/Vs$ at $V_{gs} = 10\ V$. This μ_{FE} profile may be considered as an indication of surface roughness scattering mechanism, expressed by:

$$\mu_{FE} = \frac{L_g}{WC_{ins}V_{ds}}\, g_m \tag{7-42}$$

Then, an additional term should be included to the μ_{MOS} equation taking into account the surface roughness scattering mechanism:

$$\mu_{MOS}^{-1} \approx \mu_{SR}^{-1} + \mu_C^{-1} \tag{7-43}$$

Matsumoto *et al.*[46] reported a very simple and popular approximation for the surface roughness mobility:

$$\mu_{sr}(E_{\perp}) = \frac{D}{E_{\perp}^{2}} \tag{7-44}$$

Where $E_{\perp}$ is the perpendicular electric field, and D is a fitting parameter. The effective field at the interface could be determined by:

$$E_{\perp} = \varepsilon_{s}^{-1}\left(Q_{inv}/2 + Q_{dep}\right) \tag{7-45}$$

Where ε_{s} is the permittivity of the semiconductor which can be calculated following the procedure described in the literature.[47] Surface roughness scattering increases with temperature and if this mechanism is relevant $R_{on,M}$ (and hence $R_{on,HM-H}$) will also increase with temperature.

7.5. SUMMARY

In this chapter, we have reviewed the developed strategies for converting the $AlGaN/GaN\ HEMTs$ from the conventional $normally-on$ mode ($D-mode$) to the desired $normally-off$ mode ($E-mode$). One approach is to employ a recessed-gate structure so that the $AlGaN$ under the gate is too thin to induce a $2DEG$. A second approach is to use fluorine-based plasma to bombard the semiconductor under the gate metal, so that acceptors are formed in this region, effectively depleting the $2DEG$. The third approach is to introduce a $p-doped\ GaN$ or $AlGaN$ cap layer to deplete the $2DEG$ underneath. It is possible to include the $MOS-HEMT$ as a technique for getting a $E-mode\ HEMT$ as an structure combining the $HEMT\ 2DEG$ current capability and the $MOS\ normally-off$ operation. A combination or the previous techniques with a customized growth of the $AlGaN/GaN$ stack also allow us to improve the performances of the $E-mode\ HEMTs$.

Each of these approaches has its own pros and cons in particular if you have no access to a customized MBE facility. It seems that the most used technique to achieve a $normally-off\ HEMT$ is the gate recess, which was the first proposed technique. It appears that the $AlGaN$ gate recess technique is not compatible with the fabrication $MIS-HEMT$. In contrast, the fluorine-based plasma is compatible with $MIS-HEMT$ but you introduce $F-ions$ that may be detrimental for the reliability of the $HEMT$. The channel mobility in hybrid $MOS-HEMT$ should always be limited by the mobility in the MOS region that will be hardly higher than $200\ cm^{2}/Vs$ due to the inherent interfacial traps in the $WBG\ MOS$ system.

Therefore, for converting the $AlGaN/GaN\ HEMTs\ D-mode$ to $E-mode$, it has successfully simulated a $HEMT$ with a recessed gate. We have obtained the expected shift towards $normally-off$ behavior with the thinning of the $AlGaN$ barrier. The physically-based modeling has also been used to understand the simulation results. We have obtained a $0.26\ V$ of $normally-off\ V_{th}$ shift for every nanometer of recess.

Finally, we have presented an analytical model for the ($On-state$) hybrid $AlGaN/GaN\ HEMT$. A hybrid $MOS-HEMT$ has the advantage of both the MOS gate control and the high $2DEG$ mobility in $AlGaN/GaN$ drift region. We have presented simple analytical modelling for understanding the influence of the main design parameters on the R_{on}. In particular we have been investigated the effect of the layout, the reduced MOS channel mobility, the influence of different $high-k$ dielectrics and the temperature by means of physical models for $MOSFET$ and $HEMT$ devices.

It was concluded that an hybrid $MOS-HEMT$ is still competitive in terms of R_{on} if the gate length is maintained sufficiently small even for modest MOS channel mobilities below $100\ cm^2/V$. A $high-k$ dielectric could even improve this figure. The methodology presented here can aid the designers to understand the device physics and the model can also easily be implemented by Synopsys $TCAD$ simulation packages, where models for GaN devices are not mature yet.

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Chapter 8
Conclusions and future lines

8.1. CONCLUSIONS

As $Si-based$ microelectronics technology is reaching maturity, a truly revolutionary performance improvement fundamentally requires the introduction of a new device technology platform. In this sense, $GaN-based$ devices (and particularly $GaN\ HEMTs$) have the potential to make this change possible. Since the demonstration of the first $GaN-based\ HEMT$ switches, impressive progress has been made in the development of these devices. The unique combination of the high-breakdown field, the high-channel electron mobility of the $2DEG$, and $high-T$ of operation has attracted enormous interest from academia and from industry and in this context this PhD dissertation has been made. This thesis has focused on improving the device performance through the advanced design, fabrication and characterization of $AlGaN/GaN\ HEMTs\ Si-based$.

The $GaN\ HEMT$ impressive electrical features already outperforms the best-in-class Si equivalent (such as super-junction devices), rapidly approaching the SiC theoretical limit. Besides, the $GaN-based$ devices find their place in two of the main solid-state semiconductor fields: *optoelectronics* and *microelectronics*.

Table 8-1 presents a summary of the main contributions of this thesis to the $AlGaN/GaN\ HEMTs$ devices.

$Research\ Area$	$Contribution$
$Fabrication\ process$	$Collaboration\ in\ the\ stabliment\ of\ an\ Au-free\ CMOS\ compatible.$ $4-inch\ GaN-on-Si\ technology\ in\ the\ clean\ room\ of\ the\ CNM.$
$Characterization\ methods$	$Automatic\ full\ wafer\ scale\ research.$ $High-Temperature\ HEMT.$ $FIB/CAFM\ physical\ analysis.$
$AlGaN/GaN\ HEMT$ $Ohmic\ Contact$	$Temperature\ R_{sh}\ and\ R_c\ research.$ $Physical\ models\ to\ fit\ the\ experimental\ R\ behavior.$ $Nanoscale\ Ohmic\ contact\ analyze.$ $Understand\ the\ conduction\ mechanisms.$
$AlGaN/GaN\ HEMT$ $Gate\ Contact$	$Nanoscale\ gate\ current\ analysis.$ $Conduction\ mechanisms\ identication.$ $Topography\ and\ leakage\ current\ correlation.$ $Effect\ of\ introducing\ a\ thin\ dielectric\ in\ the\ gate\ (Exp.vs\ modeling).$ $Analysis\ of\ the\ gate\ traps.$
$AlGaN/GaN\ HEMT$ $High-Voltage$ $High-Temperature$	$Temperature\ impact\ to\ reverse\ leakage\ current\ (25-300\ °C).$ $Thermal\ activation\ mechanisms\ on\ Si\ and\ sapphire\ (E_a).$ $On-state\ temperature\ impact\ on\ Si, sapphire\ and\ FS-GaN\ (T^{\alpha}).$
$AlGaN/GaN\ HEMT$ $Normally-off\ Strategies$	$AlGaN\ barrier\ thining\ TCAD\ simulation.$ $Hybrid\ MOS-HEMT\ analytical\ modelling.$

Table 8-1. Synopsis of my PhD milestones and main contributions.

The most relevant $GaN-based$ electronic devices such as $LEDs$, blue LDs and $AlGaN/GaN\ HEMTs$ are being successfully applied to a wide range of potential application areas such as smart lighting, ICT, RF electronics, power management, power industrial and energy generation and distribution further suggesting the unprecedent versatility of this material.

The main workhorse of this dissertation was the explorative analysis performed on the $AlGaN/GaN\ HEMTs$ by innovative electrical and physical characterization methods. A number of physical characterization techniques have been imaginatively used during my PhD including $CAFM$, SEM, FIB, TEM and EDX to determine the main physical parameters of our devices such as the morphology, the composition, the threading dislocations density, the nanoscale conductive pattern and others. Among these techniques of particular relevance was FIB and $CAFM$. The AFM and $CAFM$ tools have been widely described and used to understand the conduction mechanisms through the $AlGaN/GaN$ Ohmic contact by the perform simultaneously topography and electrical conductivity measurements.

A wide range of $On-state$ and $Off-state$ electrical measurements have been also carried out. The gate transfer curve $\left(I_{ds}, I_{gs}\ vs\ V_{ds}\right)$ has been measured to provide us the basic subthreshold parameters such as the threshold voltage (V_{th}), the transconductance (g_m) and the hysteresis. The current vs voltage $(I-V)$ forward curve has been used to extract the R_{on} and the $I_{ds,sat}$. The $HEMT$ leakage current is given by the reverse drain/gate-source current regarding the breakdown phenomenon. The $HEMT$ vertical leakage current, denoted as drain-bulk current (I_{db}), has been obtained to know conductive or insulating nature of the substrates. In addition, TLM has been used a well-established technique to determine the specific contact resistivity of metal Ohmic contacts to semiconductors. The $HEMT$ gate insulators films have been further characterized by a range of techniques including current vs time, dielectric stress, charge trapping, positive gate bias, $dynamic\ I-V$ and others. Finally, the electric characterization set-up and methods used have been explained to analyze $HEMT$ devices, such as $I-V$ curves using a $Keithley$ family instruments or high-voltage measurements, where the devices were characterized immersed in $Galden\ Oil$ bath to avoid the arcing in air. In addition, we have used the probe station model $S200$ from $Wentworth\ laboratories$ where we have carried out temperature characterization up to 300 °C. It is worth mentioning that the $high-T$ characterization is also a cornerstone of my PhD. The performances of the critical steps of the $HEMT$ micro-fabrication, namely Ohmic and gate contacts, were particularly investigated during my PhD. These fabrication steps are in the basis of the fabricated $AlGaN/GaN\ HEMTs$ grown on $Si, sapphire$ and $FS-GaN$ substrates at the $CRHEA-CNRS\ HEMTs$ which are the main devices investigated thorough this dissertation.

Ohmic contact

The Ohmic contact formation to GaN has been investigated through the temperature dependence study of Al/Ti contacts to $Si\ Implanted\ N^{+}bulk\ GaN-on-sapphire$ substrate. Over a temperature range of $25-250$ °C, both the R_{sh} and the R_c decreases with temperature. For temperatures higher than 250 °C, the R_c abruptly increases which is linked with the physical degradation of the metal stack. Computed R_{sh} is significantly lower than the experimentally extracted R_{sh} suggesting partial activation of the dopants. The temperature dependence could be well fitted by the partial activation of dopants enhancement with the temperature with a donor level of $10\ meV$. It was suggested that,

depending on the temperature range, TFE or FE dominates the transport across the $M-S$ interface yielding a contact resistance of $10^{-5} - 10^{-4}\,\Omega cm^2$.

The contact resistance temperature dependence was also investigated for an Ohmic contact to $HJ\ AlGaN/GaN\ HEMT$. For $Implanted\ N^{+}GaN$ contact both, R_{sh} $(850/700\ \Omega/sq)$ and R_c $(2.2/0.7\,\Omega mm)$ decrease with T $(25/250\ ℃)$. Conversely, for $HJ\ AlGaN/GaN$ contacts, R_{sh} $(400/850\ \Omega/sq)$ and R_c $(0.2/0.4\,\Omega mm)$ increase with temperature. Next, the submicron features of a typical $Ti/Al/Ni/Au$ Ohmic contact to $AlGaN/GaN$, with reduced R_c of $0.2\,\Omega mm$, have been investigated in detail, to understand the conduction mechanisms (spiking mechanism). This included $TLM\ vs\ T$ $(25-300\ ℃)$ and a range of physical analysis tools like $SEM, FIB, TEM, and\ CAFM$. The results suggest that the preferential contact mechanism is a direct electron path between the electrons of the $2DEG$ and the metal stack, though only a small part of the contact is actually conducting.

Moreover, $Au-free$ contacts characteristics have been investigated. $GaN-on-Si$ wafers allow the highly-production of $AlGaN/GaN\ HEMTs$ in some of the many $CMOS$ fabs, traditionally used for the processing of Si devices. But contacts to $AlGaN/GaN$ must be $gold-free$ in a $CMOS$ line. A R_c map comparing $Au-free$ and $Au-content$ contacts, further corroborates the relevant role of $gold$ in the achievement of low resistance to the $2DEG$ at the $AlGaN/GaN$ interface.

Gate contact

As it occurs with the most of the electronic switches, the gate stack is maybe the critical part of the device in terms of performance and longtime reliability. For this reason how the $AlGaN/GaN\ HEMT$ gate contact (composition, materials, defects and others) affects the overall $HEMT$ behaviour by means of advanced characterization and modeling have been investigated.

The nanoscale features of a typical Ohmic and Schottky contact to an $AlGaN/GaN\ HEMT$ have been investigated in detail by means of the $CAFM$ technique. The $MBE\ AlGaN/GaN-on-Si\ HEMT$ surface is composed of mounds, in the form of a truncated elliptical parabola corresponding to the morphological pattern. This complex relationship is attributed to the inhomogeneous distribution of threading dislocations (with a density of $\sim 70\ \mu m^{-2}$) formed during the double spiral $BCF-kinetic\ mode$ of

growth and the fact of analyzing the vertical current. The mound size distribution is fairly uniform with, on average, a base of 1.5 μm and a height of 100 Å (peak to valley distance). At the nanoscale, depressions in the topography appear to partially correlate with the current peaks in the current map. Conductive areas represented just 7% of the measured area. However, the current density of the conductive areas has been calculated to be as high as $2\ Acm^{-2}$. However, neither all the depressions exhibit large local leakage nor all the mounds are immune to some current spike. Besides, when the tip is biased at $-2\ V$ and $-10\ V$, it seems to correlate with the macroscopic $I-V\ vs\ T$ tests of the vertical Schottky gate produced values of $\Phi_B = 0.7\ eV$ and $\Phi_t = 0.3\ eV$ fitted with $Poole\text{–}Frenkel$ $\left(-V_{gb} < 10\ V\right)$ and $Fowler\text{–}Nordheim$ tunneling $\left(-V_{gb} > 10\ V\right)$, respectively, which, in turn, would be threading dislocation and/or nanopipe assisted conduction mechanism, respectively. A thin dielectric can effectively mitigate this leakage current also at the nanoscale.

A thin insulator is often introduced between the gate metal and the $AlGaN$ barrier layer resulting in a $MIS-HEMT$, which significantly suppresses gate leakage. It is also well known that a thin gate dielectric has a beneficial effect on the reliability of a transistor, the mitigation against current collapse being one such effect.

First, it has been presented a compact set of analytical closed-form expressions for the numerical computation of the drain current, the transfer current and the transconductance of $AlGaN/GaN\ HEMTs$. The g_m temperature dependence as $T^{-1.1}$ was apparently not in agreement with the one expected from the polar-optical phonon dependence. To further investigate this, a closed-form analytical expression (based on the $2DEG$ channel physical modeling) for the intrinsic and extrinsic transconductance of $AlGaN/GaN\ HEMTs$ was proposed. The simulation values reproduce reasonably well the experimental values using meaningful physical parameters.

Afterwards, the impact of introducing a thin gate dielectric in these devices has been investigated; by modifying the previous model this being the basis of a $MIS-HEMT$ device. It have been numerically investigated the drain current, saturation current and transconductance properties of a $MIS-HEMT$ using SiO_2, Si_3N_4, Al_2O_3 and HfO_2 as gate insulators. It has been also evaluated again the effect of the source and/or the source-drain series resistance along with self-heating. The simulation results explain reasonably well the general experimental set of results: The $MIS-HEMT$ (when

compared to an identical $HEMT$) presents the same on-resistance (at $V_{gs} = 0\ V$), higher saturation current (also at $V_{gs} = 0\ V$) but lower experimental saturation transconductance. For a given drain-source saturation current, $I_{ds,sat}$ increases as the gate capacitance decreases. Gate capacitance decreases with insulator thickness and/or with lower dielectric constant which, in turn, has an impact on the V_{th} and the $I_{ds,sat}$ peak for the different insulators. The model also suggests that self-heating has a relevant role in reducing the saturation on-state current. The thermal impedance (R_{th}) of the substrate (SiC, Si or $sapphire$) has a strong influence on both $I_{ds,sat}$ and g_m. R_{th} depends on the substrate thermal conductivity and thermal boundary resistances, elevating the channel temperature to an effective temperature. This effective temperature increase significantly degrades the electron mobility (promoted by phonon scattering) and hence, $I_{ds,sat}$ and g_m. As the MIS gate capacitance provokes an increase of I_{ds}, the g_m would be further reduced for a $MIS-HEMT$ for a given V_{ds}.

From an experimental standpoint, several $MIS-HEMT$ and Schottky gate $HEMTs$ have been comparatively studied under bias and temperature stress conditions. Several test, as DC, $dynamic\ I-V$ and $high-T$ stress tests for a stable $800V/300\ ℃$ $Au-free\ GaN-on-Si\ HEMT\ 4-inch\ Si\ CMOS$ compatible technology was presented. The thin HfO_2 layer is very effective in reducing the current collapse when compared to the $i-HEMT$, suggesting an effective passivation of surface traps. The introduction of the thin HfO_2 only caused a small V_{th} drift to negative values while other forward characteristics ($g_m, I_{ds,sat}\ and\ others$) only exhibit minor changes. It has been verified that the introduction of the thin insulator had a marked beneficial role in reducing the gate leakage current all over the wafer. The Schottky injection was mitigated when the thin insulator was introduced.

Finally, the gate trap properties of $HEMT$ and a $MIS-HEMT$ have been analyzed by means of the C/G vs ω techniques (conductance analysis). The effect of low-moderate MIS gate stress is also analyzed. D_{it}, τ_p, and σ_s have been investigated for a large range of gate biases for $slow$ and $fast$ traps. The density of the $slow$ traps is significantly lower for the $MIS-HEMT$ ($D_{it} \sim 7.0 \times 10^{11} - 5.0 \times 10^{12} cm^{-2}eV^{-1}$), when compared with the $HEMT$ ($D_{it} \sim 2.0 \times 10^{12} - 2.0 \times 10^{13} cm^{-2}eV^{-1}$). All the $HEMT$ $fast$ trap G_p/ω peaks can also be closely fitted considering $\sigma_s = 0$ ($D_{it} \sim 2.0 \times 10^{11} - 7.0 \times 10^{12} cm^{-2}eV^{-1}$). However, non-negligible peak broadening would indicate the

presence of longer-range fluctuations in the interfacial charge (and insulator charge) for the $MIS - HEMT\ fast$ traps. Additional gate stress appears to have a notable effect on the fast trap profile of the MIS, not only in the D_{it} value (which is slightly increased), but in the increase of σ_s up to $\sigma_s \sim 2.5\ k_B T/q$. This large value of σ_s would suggest the presence of additional larger-wavelength defective sites after the stress.

High-Voltage $HEMT$: ON semiconductor collaboration

Due to the WBG of GaN, $AlGaN/GaN\ HEMT$ power devices can sustain very high-voltages when biased in a reverse configuration and can work correctly at temperature higher than $300\ ℃$. The main results of the $AlGaN/GaN\ HEMTs$ power switches fabricated at the clean room of the CNM have been presented in the framework of the industrial contract with ON semiconductor. We have shown that the fabricated devices are in the state-of-the-art ($gold - free$ Ohmic and Schottky contacts) taking into account their power device figure-of-merit ($V_B^2/R_{on,sp}$) of $4.05 \times 10^8\ W/cm^2$. The extensive characterization of our $AlGaN/GaN\ HEMTs$ devices was done by means of DC characterization ($On - state$ and $Off - state$), DC wafer mappings, reverse and breakdown voltage in $Galden\ bath$ and $high - T$ stress. Basically, two different families of $AlGaN/GaN - on - Si\ MIS - HEMTs$ devices were fabricated on commercial $4\ inch$ wafers: (i) using a thin $ALD\ HfO_2$ (deposited on the CNM clean room) and (ii) thin in-situ grown Si_3N_4, as a gate insulator (grown by the vendor).

Extensive DC characterization $Off - state$ tests for thin $ALD\ HfO_2\ Au - free\ GaN - on - Si\ HEMT$ $4\ inch$ was investigated by means of wafer-level mapping. The typical drain and gate reverse current characteristics exhibited breakdown voltage saturation for $V_B \sim 700\ V$ for $\left(L_{gd} > 6 - 14\ \mu m\right)$. The yield of devices at $V_{ds} = 100\ V$ exhibiting gate currents lower than $1\ \mu A/mm$ was as high as 95%. The gate leakage current for these devices was in the range of $70 \pm 13\ nA/mm$. The thin $ALD\ HfO_2$ based MIS approach also resulted in improved gate stability and robustness under positive gate bias. Negligible gate current flow was found at $V_{gs} = +1.5\ V$. Irreversible degradation of the gate structure and device performance was observed at $V_{gs} = +5.5\ V$. The specific on-resistance value was very uniform across the wafer with $R_{on,sp} = 2.8 \pm 0.3\ m\Omega cm^2$. The maximum saturation current was also very uniform across the wafer with $I_{ds,sat} = 125 \pm 12\ mA/mm$ measured at $V_{gs} = 0\ V$. At $V_{gs} = 9\ V$ this value

increased significantly to $I_{ds,sat} = 350 \pm 24\, mA/mm$. In addition, a remarkably homogeneous threshold voltage of $V_{th} = -3.0 \pm 0.3\, V$ was determined.

The device reproducibility of 900 V-class $MIS-HEMTs$ with a thin in-situ grown Si_3N_4 gate insulator was investigated by means of wafer-level mapping. The typical drain and gate reverse current characteristics exhibited breakdown voltage saturation for $V_B \sim 900\, V$ for $(L_{gd} > 8-10\, \mu m)$ and $V_B > 600\, V$ for gate-drain length of $L_{gd} > 5\, \mu m$. The gate leakage current was maintained in all cases below $1\, \mu A/mm$ at $V_{ds} = 600\, V$. The yield of devices at $V_{ds} = 100\, V$ exhibiting drain currents lower than $1\, \mu A/mm$ was as high as 99%. The drain leakage current for these devices was in the range of $2-50\, nA/mm$. For the gate current, the yield with $I_{gs} < 1\, \mu A/mm$ at $V_{ds} = 100\, V$ was 95%. The gate leakage current for these devices was in the range of $4-50\, nA/mm$.

The thin in-situ Si_3N_4 based MIS approach also resulted in improved gate stability and robustness under positive gate bias. Negligible gate current flow was found at $V_{gs} = +9.0\, V$. Irreversible degradation of the gate structure and device performance was observed at $V_{gs} = +13.0\, V$. The specific on-resistance value was very uniform across the wafer with $R_{on,sp} = 2.5 \pm 0.3\, m\Omega cm^2$. The maximum saturation current was also very uniform across the wafer with $I_{ds,sat} = 325 \pm 33\, mA/mm$ measured at $V_{gs} = 0\, V$. At $V_{gs} = 9\, V$ this value increased significantly to $I_{ds,sat} = 603 \pm 44\, mA/mm$. In addition, a remarkably homogeneous threshold voltage of $V_{th} = -5.8 \pm 0.3\, V$ was determined.

Large area/large current devices can be defined with both gate architectures in spite that the $Au-free$ contact $CMOS$ compatible results in higher on-resistance (when compared with traditional $HEMTs$). In particular, for in-situ grown Si_3N_4, large area $HEMTs$ ($W = 31\, mm$) yield more than $18\, A$, with an on-resistance of $0.4\, \Omega$ for $V_{gs} = 0\, V$. A thicker second metal level was deposited on top of the $Au-free$ Ohmic contacts to achieve a current of several amperes. These devices also exhibited low leakage currents below $1\, \mu A/mm$ up to $500\, V$ biased in reverse.

Hight-Temperature $HEMT$

It has been reported the elevated temperature impact on the forward and the reverse leakage currents for analogous Schottky gate $HEMTs$ grown on different substrates: Si, $sapphire$ and $FS-GaN$.

The temperature has a well know detrimental effect on the carrier mobility, as several scattering phenomena increase with the temperature. This, in turn, implies a reduction of the $On-state$ current of the device with temperature. Also well-known is the strongest temperature dependence of the $HEMT-on-sapphire$ due to the Al_2O_3 substrate lower thermal conductivity. The forward-current temperature coefficients (T^{α}) have been determined on three different substrates for $Si, sapphire\ and\ FS-GaN$ in the range of $25-300$ °C. The typical temperature coefficients (α) for R_{on}, $I_{ds,sat}$ and $g_{m,max}$ have been determined 1.33, -1.53 and -1.08 for Si, 1.83, -1.78 and -1.33 for $sapphire$ and 1.29, -1.48 and -0.99 for $FS-GaN$ respectively. The greatest thermal stability has been observed for the $FS-GaN$ device, while the device in $sapphire$ is the worst. This fact is explained in terms of an improved thermal conductivity of the $FS-GaN$ substrate. Normalizing R_{th} with respect to the $FS-GaN$ value (at room temperature), it was observed a factor of improvement of $\times$ 1.6 and $\times$ 2.7 compared to Si and $sapphire$, respectively.

The elevated temperature also degrades, in general, the $Off-state$ current of the $HEMTs$ devices. This has been comparatively studied for the $HEMT-on-Si$ and $sapphire$. For the $HEMT-on-sapphire$, the $Off-state$ subthreshold current increase with temperature ($25-300$ °C) is linear $E_a\sim 0.3\ eV$ ($I_{ds,off}$). For the $HEMT-on-Si$, it was observed two different temperature regimes, being basically temperature independent up to 150 °C and then, $E_a\sim 0.3\ eV$ ($I_{ds,off}$). A single trap assisted conduction mechanism ($Poole-Frenkel$) was used to fit the experimental characteristics of the $HEMT-on-sapphire$ ($25-300$ °C). As the bulk current is negligible up to 250 °C, it is suggested that the origin of the subthreshold currents comes from the defective $AlGaN$ buffer/Schottky interface. For the $HEMT-on-Si$, the presence of additional leakage from the substrate and/or nucleation layers modifies substantially the $Off-state$ thermal characteristics of the device, particularly for the smallest drain voltages. Although the methods and substrates to fabricate $AlGaN/GaN\ HEMTs$ notably vary from one lab to another and the thermal coefficients may be

different from wafer to wafer, we believe that the methodology described in this dissertation can be virtually applied to any $HEMT$ in any substrate.

A gate insulator also has a relevant impact on the temperature behaviour of a $HEMT$ device. A MIS gate architecture can be very effective in suppressing both the drain and gate $Off-state$ leakage. For the in-situ Si_3N_4 $MIS-HEMT$ it was observed that the leakage currents were negligible up to ~ 250 °C (using a $V_{ds} = 0 - 100\ V$ reverse sweep). A negligible shift in the V_{th} was observed within experimental error. This indicates that the amount of mobile charge present in the gate insulator was also negligible. The activation energy was determined to be as high as $E_a = 1.02\ eV$. We suggest that this larger value of the thermal activation energy is related to the larger effective heterojunction electron barriers achieved by the in-situ passivation along with the optimized GaN buffer. Analogously, the ALD HfO_2 solution also mitigates to some extent the gate leakage with the elevated temperature. The reverse bias leakage current activation energy (gate and drain) was determined to be $E_a = 0.4\ eV$ and $0.3\ eV$ for the $i-HEMT$ $(75-300$ °C) and the $MIS-HEMT$ $(75-210$ °C), where leakage saturation was observed for $T > 210$ °C for the $MIS-HEMT$.

Finally, preliminary $high-T$ reliability stability assessment of the ALD HfO_2 device has presented. The $Off-state$ stress tests showed no degradation at a reverse bias of $V_{ds} = 200\ V$ and 310 °C. When the device is stressed at a reverse bias of $300\ V$ at 310 °C it was observed a sudden increase of leakage current with a stabilization after few seconds. When the transconductance curve is analyzed after stress test, it appears that devices stressed $200\ V$ at 200 °C have survived with no remarkable shift in either the threshold voltage or the $Off-state$ current. The devices stressed $200\ V$ at 310 °C survived (same low $Off-state$ current before/after) but when the gate is biased at small positive gate bias, we observed a sudden increase of the gate current. Therefore, it appears that effectively the gate insulator has been degraded somehow. Devices stressed $300\ V$ at 310 °C were severely damaged and the gate current in the $Off-state$ increases up to four orders of magnitude after stress.

$Normally - off\ HEMT$

We have reviewed the developed strategies for converting the $AlGaN/GaN\ HEMTs$ from the conventional $normally - on$ mode ($D - mode$) to the desired $normally - off$ mode ($E - mode$). One approach is to employ a recessed-gate structure so that the $AlGaN$ under the gate is too thin to induce a $2DEG$. A second approach is to use fluorine-based plasma to bombard the semiconductor under the gate metal, so that acceptors are formed in this region, effectively depleting the $2DEG$. The third approach is to introduce a $p - doped\ GaN$ or $AlGaN$ cap layer to deplete the $2DEG$ underneath. It is possible to include the $MOS - HEMT$ as a technique for getting a $E - mode$ $HEMT$ as an structure combining the $HEMT\ 2DEG$ current capability and the $MOS\ normally - off$ operation. A combination or the previous techniques with a customized growth of the $AlGaN/GaN$ stack also allow us to improve the performances of the $E - mode\ HEMTs$.

It seems that the most used technique to achieve a $normally - off\ HEMT$ is the gate recess, which was the first proposed technique. Therefore, for converting the $AlGaN/GaN\ HEMTs\ D - mode$ to $E - mode$, it has successfully simulated a $HEMT$ with a recessed gate. We have obtained the expected shift towards $normally - off$ behavior with the thinning of the $AlGaN$ barrier. We have obtained a $0.26\ V$ of $normally - off$ V_{th} shift for every nanometer of recess.

Finally, we have presented an analytical model for the ($On - state$) hybrid $AlGaN/GaN\ HEMT$. A hybrid $MOS - HEMT$ has the advantage of both the MOS gate control and the high $2DEG$ mobility in $AlGaN/GaN$ drift region. We have presented simple analytical modelling for understanding the influence of the main design parameters on the R_{on}. In particular we have been investigated the effect of the layout, the reduced MOS channel mobility, the influence of different $high - k$ dielectrics and the temperature by means of physical models for $MOSFET$ and $HEMT$ devices.

It was concluded that an hybrid $MOS - HEMT$ is still competitive in terms of R_{on} if the gate length is maintained sufficiently small even for modest MOS channel mobilities below 100 cm^2/V. A $high - k$ dielectric could even improve this figure.

8.2. SUGGESTIONS FOR FUTURE WORK

A first expected goal of the research is to continue with the advanced characterization and modeling of $AlGaN/GaN\ HEMTs$ on Si, $sapphire$ and $FS-GaN$ substrates with different dislocations and trapping profiles. This devices are expected to be $C-V$ analyzed, to compare the Dit profile, the effect of the dislocations, the mobility at low temperature, the $dynamic\ I-V$, the trap characteristic time, the band-bending fluctuations and other characteristics for the different substrates. In addition to this analysis, the $C-V\ vs\ T$ should be measured to determine the trap cross-section.

A second expected goal of the research is to determine the properties of the different Schottky barrier diodes on the different GaN substrates. In order to know the Schottky barrier height, the inhomogeneities, the ideality factor, the conduction mechanisms and other parameters. Besides, this work will contribute to the exploration of the Schottky gate inhomogeneities understanding to be $I-V\ vs\ T$ investigated and modeled using inhomogeneities models such as the Tung model.

A third research line is to further insight of $TCAD$ physical simulation for understanding the high-voltage features and the piezoelectric effect at atomic scale. For example the current $TCAD$ models have no properly addressed the threading density network of the real GaN structures. The generation of carriers is trap assisted by theses dislocations (via $Poole-Frenkel$) rather than mobility limited so giving rise to unrealistic high-voltage breakdown values when you make a conventional simulation. In the same sense, the effect of the threading dislocation density, the local polarization field, etc, on the $high-T\ HEMT$ mobility is a field that may be further explored by advanced modeling techniques.

A fourth expected goal deals with the nano-characterization of $HEMTs$. The $high-T$ $CAFM$ characterization of Si and $FS-GaN\ HEMTs$ is new research line that we have a particular interest to explore. It should be mentioned that the nano-characterization of $HEMTs-on-$ sapphire via $CAFM$ requires a preliminary sample preparation (wire-bonding). In addition to the nanoscale research, the investigation of the Al content (i.e., x composition) in order to know the micro and nanoscale properties of the $AlGaN/GaN\ HEMT$ is an important milestone. Also, at the nanoscale the investigation of the conductive pattern of FIB is a way to define nanowires on GaN structure.

A fifth point in the research is focused in the development of an integral reliability test battery at elevated temperature. For example, different temperature lifetime test such as the drop of the output current respect to the initial value during constant bias stress for different temperatures, the failure times during temperature stress and other type of lifetime test. Finally, the expected goal (related with the previous points) is the DC comparison of $AlGaN/GaN\ HEMTs$ before and after the neutron or proton irradiations via $C-V$, $I-V$ and nanoscale analysis.

Appendix A

Publication list of the author

1.1. JOURNAL CONTRIBUTIONS

1. M. Placidi, A. Constant, **A. Fontserè**, E. Pausas, I. Cortes, Y. Cordier, N. Mestres, R. Pérez, M. Zabala, J. Millán, P. Godignon and A. Pérez-Tomás, "Deposited thin SiO_2 for gate oxide on *n-type* and *p-type* GaN," *Journal of the Electrochemical Society* **157,** H1008 (2010).

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Appendix B

List of acronyms

$2DEG$	Two dimensional electron gas
AFM	Atomic force microscopy
Al_2O_3	Sapphire
ALD	Atomic layer deposition
$AlGaN$	Gallium nitride aluminum
AlN	Aluminum nitride
BCF	Burton, Cabrera and Frank
$CAFM$	Conductive atomic force microscopy
$CAGR$	Compound annual growth rate
$CMOS$	Complementary metal oxide semiconductor
CNM	Centre Nacional de Microelectrònica
$CNRS$	Centre National de la Recherche Scientifique
$CRHEA$	Centre de Recherche sur l'Hétéro-Epitaxie
$C-V$	Capacitance vs voltage characteristic curve

CVD	Chemical vapor deposition
DC	Direct Current
$D-mode$	Depletion mode
EDX	Energy dispersive x-ray spectroscopy
$E-mode$	Enhanced mode
EPC	Efficient power conversion corporation
FE	Field emission
FET	Field effect transistor
FIB	Focused ion beam
FOM	Figure of merit
$FS-GaN$	Free Standing $-GaN$
$GaAs$	Gallium arsenide
$Ga-face$	Gallium face
GaN	Gallium nitride
GIT	Gate injection transistor
$HEMT$	High electron mobility transistor
HEV	Hybrid electric vehicle
$HFET$	Heterostructure field effect transistor
HfO_2	Hafnium oxide
$Hg-CV$	Mercury probe $C-V$
HJ	Heterojunction
$HVPE$	Hydride vapor phase epitaxy
$HVDC$	High voltage direct current
IC	Integrated circuit
ICP	Inductively coupled plasma

ICT	Information and communication technologies
$IGBT$	Insulated gate bipolar transistor
$i-HEMT$	Passivated $HEMT$
$I-V$	Current vs voltage characteristic curve
JM	Johnson's figure of merit
LD	Laser diode
LED	Light emitting diode
MBE	Molecular beam epitaxy
$MESFET$	Metal semiconductor field effect transistor
$MIS-HEMT$	Metal insulator semiconductor $HEMT$
$MOCVD$	Metal organic chemical vapor deposition
$MOSHFET$	Metal oxide semiconductor hybrid field effect transistor
$MOSFET$	Metal oxide semiconductor field effect transistor
$MOVPE$	Metalorganic vapour phase epitaxy
$M-S$	Metal-semiconductor
$N-face$	Nitrogen face
NiD	Non-intentionally doped
NL	Nucleation layer
$PECVD$	Plasma enhanced chemical vapor deposition
PVD	Physical vapor deposition
RF	Radio frequency
$RESURF$	Reduced surface field
RIE	Reactive ion etching
$RHEED$	Reflection high energy electron diffraction
RMS	Root mean square

RTA	Rapid thermal annealing
RT	Room temperature
SB	Schottky barrier
SEM	Scanning electron microscopy
SiC	Silicon carbide
$SIMS$	Secondary ion mass spectrometry
Si_3N_4	Silicon nitride
SiO_2	Silicon oxide
SPM	Scanning probe microscopy
$SJ-MOSFET$	Super junction metal oxide semiconductor field effect transistor
TBR	Thermal boundary resistance
TE	Thermionic emission
TEM	Transmission electron microscopy
TFE	Thermionic field emission
TLM	Transmission line method
$TRIM$	Transport of ions in matter
UID	Unintentionally doped
WBG	Wide band gap

Appendix C
List of mathematical symbols

This appendix contains a list of mathematical symbols used in this thesis.

a_0	Unstrained lattice constant	Å
a_s	Strained lattice constant	Å
a	Electron drift velocity adjustable parameter	
A^*	Richardson constant	A/cm^2K^2
A	Area	cm^2
b_i	$Caughy - Thomas$ fitting parameter	
C	$\mu_{2DEG,po}$ fitting parameter	$Vs/cm^{2+\delta}K^{\gamma}$
c_0	Unstrained lattice constant	Å
c_s	Hexagonal strained lattice constant	Å
C_i	Concentration of ionized impurities	cm^{-3}
C_r	μ_B $Caughy - Thomas$ fitting constant	cm^{-3}
c_{ij}	Stiffness constant	Pa
C_b	Gate capacitance	F/cm^2
C_{ins}	Gate insulator capacitance	F/cm^2
C_H	Gate $AlGaN$ buffer capacitance ($HEMT$)	F/cm^2
ΔE_C	Conduction band offset at the $AlGaN/GaN$	eV
d	Distance of two metal strips TLM	μm
d_{sub}	Substrate thickness	μm
d_{31}	Piezoelectric coefficient	cm/V
D_{it}	Interfacial trap density	$cm^{-2}eV^{-1}$
E_a	Activation energy	eV
E_c	Conduction band energy	eV
E_v	Valence band energy	eV
E_F	Fermi level energy	eV
E_g	Bandgap energy	eV

E_i	Intrinsic level energy	eV
E_d	Donor level energy	eV
E_0	2DEG first sub-band energy	eV
E_{00}	Schottky contact characteristic energy	eV
E	Electric field	V/cm
E_p	Polarization field	V/cm
$E_\perp$	Perpendicular electric field	V/cm
E_{crit}	Critical electric field	V/cm
$F_{1/2}$	Fermi integral	
F	Electron mobility form factor	
G_p	Equivalent conductance	F/s
G_p/ω	Parallel conductance	F
g_m	Gate transconductance	mS/mm
h	Planck constant	eVs
$\hbar$	Reduced Planck constant	eVs
$\hbar\omega_O$	Optical phonon energy	meV
I_{db}	Drain-bulk current	A
I_{ds}	Drain-source current	A
I_{gb}	Gate-bulk current	A
I_{gs}	Gate-source current	A
$I_{ds,sat}$	Drain-source saturation current	A
$\vec{J}$	Current density	A/m^2
$\overrightarrow{J_n}$	Electron current density	A/m^2
$\overrightarrow{J_p}$	Hole current density	A/m^2
L_{ch}	$MOSFET$ channel lenght	μm
L_D	$MOSFET$ drift region lenght	μm
L_g	Gate length	μm
L_{gd}	Gate-drain spacing	μm
L_{ds}	Drain-source spacing	μm
L_{gs}	Gate-source spacing	μm
L_s	Source length	μm
L_T	Transfer length	μm
m^*	Effective mass	m_0
m_0	Electron mass	kg
N'	μ_c fitting parameter	$K^\alpha V\,s/cm^2$
N_A	Acceptor impurity concentration	cm^{-3}
N_D	Donor impurity concentration	cm^{-3}
$N_{D,pk}$	(Gaussian) Donor peak value concentration	cm^{-3}
N_c	Conduction band density of states	cm^{-3}
n_i	Intrinsic carrier density	cm^{-3}
n	Free electron density	cm^{-3}
n_b	The effective net-charged buffer traps per unit area	cm^{-2}
n_{st}	Net-charged surface traps per unit area	cm^{-2}
n_s	$2DEG$ sheet carrier concentration	cm^{-2}
p	Free hole density	cm^{-3}

P_z	Piezoelectric polarization	C/cm^2
P_j^{sp}	Spontaneous polarization	C/cm^2
P_s	Spontaneous polarization	C/cm^2
P_T	Polarization induced charge density	cm^{-2}
R^B	Biaxial relaxation coefficient	
q	Elementary electronic charge	C
Q_{PE}	Piezoelectric charge	cm^{-2}
Q_{dep}	MOS depletion charge	cm^{-2}
Q_{inv}	MOS inversion charge	cm^{-2}
Q_{trap}	MOS interface trap charge	cm^{-2}
R_T	Total (front) resistance	Ω
R_c	Contact resistance	Ωmm
R_{DS}	Drain-source HEMT access resistance	Ω
R_S	Source-gate access resistance	Ω
R_{gd}	Gate-drain resistance	Ω
R_{sg}	Source-gate resistance	Ω
R_{on}	On-resistance	Ω
$R_{on,sp}$	Specific on-resistance	$m\Omega cm^2$
R_{sh}	Sheet resistance	Ω/sq
R_{th}	Thermal resistance	K/W
R_{net}	Electron-hole recombination rate	s/cm^3
T	Temperature	K
t	Time	s
t_{ins}	Gate insulator thickness	μm
t_b	$AlGaN$ barrier thickness	μm
u_0	Unit cell internal parameter	Å
V_{ds}	Drain-source voltage	V
$V_{ds,sat}$	Drain-source knee voltage at the onset of saturation	V
V_{gd}	Gate-drain voltage	V
V_{gs}	Gate-source voltage	V
V_{db}	Drain-bulk voltage	V
V_{th}	Threshold voltage	V
V_B	Breakdown voltage	V
V_F	Forward built-in voltage	V
v	Electron drift velocity	cm/s
v_{sat}	Saturation drift velocity	cm/s
x	Aluminum content	
X_h	Hybrid $MOS - HEMT\ NiD$ channel lenght	μm
X_j	MOS Inversion channel depth	μm
W	Device width	μm
Z	TLM metal strips width	μm

α	Temperature coefficient	
α_D	Partial activation effective volume	cm^{-3}
α_T	Thermal expansion coefficient	K^{-1}
α_c	Interface trap scattering coefficient	
β_c	Interface trap scattering coefficient	
γ	Polar optical phonon temperature coefficient	
ΔE_c	$AlGaN/GaN$ conduction band offset	eV
δ	Polar optical phonon $2DEG$ n_s coeficient	
ε	Electrical permittivity	F/m
ε_0	Electrical permittivity of vacuum	F/m
ε_r	Relative dielectric constant	
ε_s	Permittivity of the semiconductor	
$\varepsilon_{s,\infty}$	Permittivity of the semiconductor at high freq.	
ε_{jj}	Strain tensor	
η_F	Normalized Fermi energy	eV
k	Thermal conductivity	W/mK
k_O	Polar optical phonon wave vector	m^{-1}
k_B	Boltzman constant	eV/K
λ_p	Thermal resistance of the package	℃
μ_{2DEG}	$HEMT$ $2DEG$ electron mobility	cm^2/Vs
$\mu_{2DEG,po}$	$2DEG$ polar optical phonon electron mobility	cm^2/Vs
$\mu_{B,po}$	Bulk semiconductor polar optical mobility	cm^2/Vs
μ_{ac}	Acoustic phonon scattering mobility	cm^2/Vs
μ_B	Bulk electron mobility	cm^2/Vs
μ_c	Interface traps Coulomb scattering mobility	cm^2/Vs
μ_{FE}	Hybrid $MOS-HEMT$ field-effect mobility	cm^2/Vs
μ_{max}	μ_B $Caughy-Thomas$ fitting constant	cm^2/Vs
μ_{min}	μ_B $Caughy-Thomas$ fitting constant	cm^2/Vs
μ_{MOS}	$MOSFET$ field effect mobility	cm^2/Vs
μ_n	Electron mobility	cm^2/Vs
μ_p	Hole mobility	cm^2/Vs
μ_{sr}	Surface roughness mobility	cm^2/Vs
ξ	μ_c inversion charge Tcoefficient	
ρ_c	Specific contact resistivity	Ωcm^2
ρ_{trap}	Charge density by traps and fixed charges	C/cm^{-3}
σ_{jj}	Diagonal stress tensor	Pa
σ_D	Standard deviation of the doping profile	
σ_s	Standard deviation of the band-bending	
τ_p	Trap state time constant	s
ϕ	Quasi-Fermi potential	eV
Φ_B	Schottky barrier height	eV
Φ_t	Barrier height for electron emission	eV
ω	Angular velocity	s^{-1}
ω_0	Angular velocity of the polar optical phonon	s^{-1}