COMPACT DC MODELING OF TUNNEL-FETS

Fabian Horst

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Compact DC Modeling of Tunnel-FETs

FABIAN HORST

DOCTORAL THESIS
2019

Fabian Horst

COMPACT DC MODELING OF TUNNEL–FETS

DOCTORAL THESIS

Supervised by Prof. Dr. Benjamín Iñíguez
and Prof. Dr.-Ing. Alexander Kloes

Department of Electronic,
Electrical and Automatic Control Engineering

UNIVERSITAT ROVIRA I VIRGILI

Tarragona
2019

Statement of Supervision

Department of Electronic, Electric
and Automatic Engineering (DEEEA)
Av. Paisos Catalans 26, Campus Sescelades
43007, Tarragona, Spain
Phone: +34 977 558524
Fax: +34 977 559605

I STATE that the present study, entitled: "COMPACT DC MODELING OF TUNNEL–FETS", presented by Fabian Horst for the award of the degree of the Doctor, has been carried out under my supervision at the Department of Electronic, Electrical and Automatic Control Engineering of this university, and that it fulfills all the requirements to be eligible for the European Doctorate Award.

Tarragona, Spain, August 30, 2019

Prof. Dr. Benjamín Iñíguez, Doctoral Thesis Supervisor

Prof. Dr.-Ing. Alexander Kloes, Doctoral Thesis Co-Supervisor

Statement of Authorship

Research Group Nanoelectronics / Device Modeling
Wiesenstrasse 14
35390, Giessen, Germany
Phone: +49 641 309-1968
Fax: +49 641 309-2901

I STATE that this document has been composed by myself and describes my own work, unless otherwise acknowledged in the text. Parts that are direct quotes or paraphrases are identified as such. It has not been accepted in any previous application for a degree. All sources of information have been specifically acknowledged.

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Fabian Horst, M. Sc.

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List of Symbols

Latin Alphabet

Symbol	Description	Unit
A	Complex constant of the 1D wavefunction Ψ	$[1/\sqrt{\text{cm}}]$
$A_1^{\text{s/d}}$	Area under the band diagram, used in the AE WKB approach	[J cm]
$A_2^{\text{s/d}}$	Area of the triangle, used in the AE WKB approach	[J cm]
a_L	Parameter of the potential solution for a piecewise linear boundary	$[\text{cm}/\text{V}^2]$
$a_{\text{s/d}}$	Parameter of the compact potential in S/D region	$[\text{V}/\text{cm}^2]$
B	Complex constant of the 1D wavefunction Ψ	$[1/\sqrt{\text{cm}}]$
b_L	Parameter of the potential solution for a piecewise linear boundary	[cm]
$b_{\text{s/d}}$	Parameter of the compact potential in S/D region	$[\text{V}\,\text{cm}^{-1}]$
C	Complex constant of the 1D wavefunction Ψ	$[1/\sqrt{\text{cm}}]$
$C_{1,2}$	Complex constants of the Schwarz-Christoffel transformation	[cm]
C'_ox	Gate oxide capacitance per gate area	$[\text{F}/\text{cm}^2]$
$c_{\text{s/d}}$	Parameter of the compact potential in S/D region	[V]
D	Complex constant of the 1D wavefunction Ψ	$[1/\sqrt{\text{cm}}]$
D_{12}, D_{13}	Simplification in the calculations of the compact potential in the channel region	$[\text{V}\,\text{cm}^{-1}]$
D_ox	Dielectric displacement	$[\text{As}/\text{cm}^2]$
E	Considered energy level	[J]
$\vec{E}$	Electric field vector	$[\text{V}\,\text{cm}^{-1}]$
E_c	Conduction band energy	[J]
E_f	Fermi energy level	[J]

E_g	Band gap energy	[J]
$E_\mathrm{s/d}$	Energy difference due to the degeneration of the semiconductor	[J]
E_v	Valence band energy	[J]
E_vac	Energy of the vacuum level	[J]
$E_{x,y,z}$	x,y,z component of the electric field vector	[$\mathrm{V\,cm^{-1}}$]
F	Complex constant of the 1D wavefunction Ψ	[$1/\sqrt{\mathrm{cm}}$]
F_{φ_ch}	Smoothing function of the 1D channel surface potential	[V]
$\mathcal{F}_n$	Fermi-Dirac integral of order n	[−]
f	Fermi-Dirac distribution	[−]
f_t	Probability that a trap state is occupied	[−]
G_t	TAT generation rate	[$\mathrm{s^{-1}cm^{-3}}$]
g	3D density of states in momentum space	[$\mathrm{cm^{-3}}$]
h	Planck's constant	[J s]
$\hbar$	Reduced Planck's constant	[J s]
I_ds	Resulting device current of the TFET	[A]
J_cp	Compact current density along the y-axis	[$\mathrm{A/cm^2}$]
J_tun	Tunneling current density	[$\mathrm{A/cm^2}$]
J_y	Tunneling current density along the y-axis	[$\mathrm{A/cm^2}$]
j	Imaginary number	[−]
$K_1^\mathrm{s/d}$	Simplification in the calculations of the tunneling length	[V]
k, $k_{1,2,3}$	Wave vector of the 1D wavefunction Ψ along the x-axis	[$\mathrm{cm^{-1}}$]
$\vec{k}$	Wave vector of the 3D wavefunction Ψ	[$\mathrm{cm^{-1}}$]
k_b	Boltzmann constant	[$\mathrm{J\,K^{-1}}$]
$k_\mathrm{s/d}$	Parameter of the compact potential in channel region	[V cm]
$k_{x,y,z}$	Wave vector component of the 3D wavefunction Ψ	[$\mathrm{cm^{-1}}$]
$\vec{k}_\rho$	To x-axis parallel wave vector of the 3D wavefunction Ψ	[$\mathrm{cm^{-1}}$]
L	Length of a cube	[cm]
l_ch	Channel length of the TFET device	[nm]
$l_\mathrm{s/d}$	Parameter of the compact potential in channel region	[cm]
l_sd	Length of source/drain region of the TFET device	[nm]
l_tun	Tunneling length	[cm]
m^*	Effective carrier mass	[kg]
$m_\mathrm{s/d}$	Parameter of the compact potential in channel region	[V]

$\mathcal{N}$	Supply function	[J]
N_{inv}	Inversion charge density	$[\text{cm}^{-3}]$
$N_{\text{s,ch,d}}$	Doping concentration of source, channel and drain region	$[\text{cm}^{-3}]$
N_{t}^{0}	Maximum interface trap density	$[\text{cm}^{-2}]$
N_{t}	Interface trap density at a considered energy	$[\text{cm}^{-2}]$
n, n_1	Electron carrier concentration	$[\text{cm}^{-3}]$
n_{diode}	Quality factor of the parasitic diode	[−]
n_{i}	Intrinsic electron concentration in Silicon	$[\text{cm}^{-3}]$
$\bar{P}$	Complex Potential function	[V]
$P_i^{\text{s/d}}$	Potential point for the compact potential solution	[nm, V]
p, p_1	Hole carrier concentration	$[\text{cm}^{-3}]$
q	Elementary charge	[A s]
r	Radius	[cm]
T	Temperature	[K]
TGR	Tunneling generation rate	$[\text{s}^{-1}\text{cm}^{-3}]$
T_{tun}	Tunneling probability	[−]
t_{ch}	Channel thickness of the TFET device	[nm]
t_{ox}	Gate oxide/insulator thickness	[nm]
$\tilde{t}_{\text{ox}}$	Scaled gate oxide/insulator thickness	[nm]
$U(x)$	Energy barrier shape depending on x	[J]
U_0	Amplitude of a constant energy barrier	[J]
$U_{\text{bar}}^{\text{s/d}}$	Tunneling energy barrier height in the AE WKB approach	[J]
ΔU	Energy difference	[J]
v	Carrier velocity	$[\text{cm}\,\text{s}^{-1}]$
V_{ds}	Drain-source voltage	[V]
V_{fb}	Flat band voltage	[V]
V_{gs}	Gate-source voltage	[V]
$V_{\text{gs,eff}}$	Effective gate-source voltage	[V]
V_{ox}	Voltage drop across the gate oxide	[V]
V_{s}	Source voltage	[V]
V_{th}	Threshold voltage	[V]
u	Real part of the complex variable / function $\bar{w}$	[cm] / [TBD]
u	Normalized potential value	[−]

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$u_{\mathrm{s/c}}$	Normalized surface/center potential value	[−]
u'	Integration variable along the u-axis	[cm]
v	imaginary part of the complex variable / function $\bar{w}$	[cm] / [TBD]
W	Width of a rectangular energy barrier	[cm]
$\bar{w}$	Complex variable in $\bar{w}$-plane / Complex function	[cm] / [TBD]
$\bar{w}_{\mathrm{s/d}}$	Mapping function for the source/drain related case	[−]
w_{ch}	Channel width of the TFET device	[nm]
x	Cartesian coordinate	[cm]
$x_i^{\mathrm{s/d}}$	x values for the compact potential approximation	[nm]
$x_{\mathrm{t}}^{\mathrm{s/d}}$	Specific x-position at which the tunneling length is derived	[cm]
$x_{\mathrm{t,1,2}}^{\mathrm{s/d}}$	Integration limits of the B2B tunneling generation rate	[cm]
$x_{\mathrm{B2B/TAT,max}}^{\mathrm{s/d}}$	x-position of the maximum TGR value (B2B/TAT)	[cm]
y	Cartesian coordinate	[cm]
z	Cartesian coordinate	[cm]
$\bar{z}$	Complex variable in $\bar{z}$-plane	[cm]

Greek Alphabet

Symbol	**Description**	**Unit**
$\Gamma^{\mathrm{s/d}}$	Approximated field-effect enhancement factor in the compact model	[−]
$\Gamma_{\mathrm{e/h}}$	Field-effect enhancement factor for electrons/holes	[−]
γ	Body factor	[$\sqrt{\mathrm{V}}$]
γ	Phase angle of the longitudinal wave vector $\vec{k}_\rho$	[rad]
γ_i	Phase angle of the Schwarz-Christoffel transformation	[−]
Δ	Laplace operator	[−]
$\Delta E_{\mathrm{g}}^{\mathrm{s/d}}$	Band gap difference due to band gap narrowing	[J]
δ_y	Exponent of the compact potential along the y-axis	[−]
ε	Permittivity	[$\mathrm{A\,s\,V^{-1}\,cm^{-1}}$]
$\eta^{\mathrm{s/d}}$	Standard deviation of the compact current density approximation, adjustable parameter	[cm]
$\Theta(x)$	Amplitude function of the 1D wavefunction Ψ	[$1/\sqrt{\mathrm{cm}}$]
ϑ_1	Simplification in the calculation of $x_{\mathrm{B2B,max}}^{\mathrm{s/d}}$	[V^2]
ϑ_2	Simplification in the calculation of $x_{\mathrm{B2B,max}}^{\mathrm{s/d}}$	[cm^3]

ϑ_3	Simplification in the calculation of $x^{\mathrm{s/d}}_{\mathrm{B2B,max}}$	[cm^2]
$\varkappa^{\mathrm{s/d}}_{\mathrm{TAT}}$	Fitting parameter to adjust the slope of the TAT current part	[−]
ζ	Electric flux	[A s]
λ	Wavelength	[cm]
$\lambda^{\mathrm{s/d}}_{\mathrm{fit}}$	Adjustable parameter to tune the screening length	[−]
$\lambda^{\mathrm{s/d}}_{\mathrm{ln,fit}}$	Adjustable parameter to tune the influence of inversion charges on the potential solution	[−]
λ, $\tilde{\lambda}_{\mathrm{s/d}}$	Screening length at source/drain-to-channel junction	[cm]
Ξ	Electric flux function	[V cm^{-1}]
ϱ	Space charge	[As/cm^3]
$\sigma^{\mathrm{s/d}}_{\mathrm{B2B}}$	Standard deviation of B2B TGR approximation, adjustable parameter	[cm]
$\sigma_{\mathrm{L,1,2,3}}$	Parameter of the potential solution for a piecewise linear boundary	[V]
$\sigma_{\mathrm{L,4}}$	Parameter of the potential solution for a piecewise linear boundary	[cm^2]
$\sigma^{\mathrm{s/d}}_{\mathrm{TAT}}$	Standard deviation of TAT TGR approximation, adjustable parameter	[cm]
$\varsigma_{\mathrm{e/h}}$	Electron/hole generation lifetime	[s]
$\tau^{\mathrm{s/d}}_{\mathrm{TAT}}$	Capture cross section	[cm^2]
Φ	Electrostatic potential	[V]
$\Phi^{\mathrm{s/d}}_{\mathrm{bi}}$	Built-in potential of the source/drain region	[V]
$\Phi^{\mathrm{s/d}}_{\mathrm{bi,eff}}$	Effective built-in potential at the source/drain-to-channel junction	[V]
$\Phi^{\mathrm{s/d}}_{\mathrm{C}}$	Constant boundary condition of the 2D channel potential	[V]
$\Phi^{\mathrm{s/d}}_{\mathrm{cen}}$	Compact potential in the channel center for any x-position	[V]
$\Phi^{\mathrm{s/d}}_{\mathrm{L}}$	Linear boundary condition of the 2D channel potential	[V]
$\Phi^{\mathrm{s/d}}_{\mathrm{P}}$	Parabolic boundary condition of the 2D channel potential	[V]
$\Phi^{\mathrm{s/d}}_{\mathrm{sur}}$	Compact potential at the channel surface for any x-position	[V]
ϕ	Phase function of the 1D wavefunction Ψ	[−]
ϕ	Phase angle	[rad]
$\phi^{i}_{\mathrm{C,L,P}}$	Potential solution for a piecewise constant, linear, parabolic boundary	[V]

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$\varphi_{\mathrm{C,L,P}}$	2D electrostatic solution for a constant, linear, parabolic boundary condition	[V]
$\varphi_{\mathrm{c}}^{\mathrm{1D}}$	1D channel center potential	[V]
$\varphi_{\mathrm{s}}^{\mathrm{1D}}$	1D channel surface potential	[V]
$\varphi_{\mathrm{s,dep/inv}}^{\mathrm{1D}}$	1D channel surface potential in depletion/inversion mode	[V]
$\varphi_{x}^{\mathrm{s/ch/d}}$	Compact potential solution along the x-axis	[V]
φ_{y}	Compact potential solution along the y-axis	[V]
$\varphi_{\mathrm{2D}}^{\mathrm{ch}}$	2D closed-form channel potential solution	[V]
χ	Electron affinity	[J]
Ψ	1D wavefunction	[$1/\sqrt{\mathrm{cm}}$]

Other

Symbol	**Description**	**Unit**
∇	Nabla operator	[−]
∂	Partial differential operator	[−]

List of Acronyms

Symbol	Description
1D	One-dimensional
2D	Two-dimensional
3D	Three-dimensional
AC	Alternating current
AE	Area-equivalent
AlGaSb	Aluminum-Gallium antimonide
AT	Access transistors
B2B	Band-to-band
BGN	Band gap narrowing
Ch	Channel
ConB	Conduction band
cp	Compact
D	Drain
DC	Direct current
DG	Double-gate
DIBL	Drain-induced barrier lowering
EUV	Extreme ultraviolet lithography
FEM	Finite element method
FET	Field-effect transistor
F-N	Fowler-Nordheim
G	Gate
GAA	Gate-all-around
GaAs	Gallium arsenide
GaSb	Gallium antimonide
Ge	Germanium
HfO_2	Hafnium dioxide

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H/R	Hold/read
IC	Integrated circuit
IC-CAP	IC-Characterization and Analysis Program
InAs	Indium arsenide
ITRS	International technology roadmap for semiconductors
La_2O_3	Lanthanum oxide
MESFET	Metal-semiconductor field-effect transistor
MOSFET	Metal-oxide-semiconductor field-effect transistor
MuGFET	Multiple-gate FET
NC	Negative capacitance
NEGF	Non-equilibrium Green's function
$NiSi_2$	Nickel Silicide
NW	Nanowire
PD	Pull-down
PU	Pull-up
S	Source
SB	Single-band
SCE	Short-channel effect
SD	Source-to-drain
Si	Silicon
SiGe	Silicon-germanium
SNM	Static noise margin
SOI	Silicon on insulator
SRAM	Static random-access memory
sSi	Strained Silicon
Ta_2O_5	Tantalum pentoxide
TAT	Trap-assisted tunneling
TCAD	Technology computer-aided design
TFET	Tunnel field-effect transistor
TGR	Tunneling generation rate
TiO_2	Titanium dioxide
ValB	Valence band
VTC	Voltage transfer characteristics
W	Write
WKB	Wentzel-Kramers-Brillouin
Y_2O_3	Yttrium oxide

CHAPTER 1

Introduction

Looking back at the last five decades of the development in the semiconductor industry, one can see an outstanding technical improvement in all kinds of electronic devices. At the same time, society's demands for these electronic devices have increased over the years. In modern daily life it is totally usual to have a computer, laptop, smartphone or various consumer electronic products at home and use them several times a day. This rapid development is due to the efforts of the entire scientific community around the world. At the moment, the metal-oxide-semiconductor field-effect transistor (MOSFET) is the technologically most advanced semiconductor device and is the most common transistor in digital and analog circuits. Due to the growing demands regarding the speed of the chips, efficiency and size, the transistor density on a chip also increases, which means the single transistor size decreases. Concerning the shrinking size of a transistor, the MOSFET technology is going to reach its physical limitations. Consequently, the scientific community is looking for an alternative to the MOSFET technology having a steeper switching behavior, a smaller supply voltage or a lower OFF-current. One promising candidate that offers all these advantages is the tunnel field-effect transistor (TFET). For this reason, a compact DC TFET current model is introduced in this work.

The following sections give a brief overview of the history of semiconductor devices (Sec. 1.1) and the technological evolution from the MOSFETs to the current TFETs in Sec. 1.2. Furthermore, the relevance of device simulation and the importance of compact modeling in the semiconductor development are introduced in Sec. 1.3. A state-of-the-art overview of the compact TFET models reported in the literature is presented in Sec. 1.4, followed by the challenges and outline of this dissertation in Sec. 1.5.

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1.1 History of Semiconductor Devices

The first innovation in electronic devices was made by Julius Edgar Lilienfeld in 1926, when he introduced the first patents that describe the working principle of a transistor [1, 2]. In his patents he described a three terminal electric device in which two contacts were connected with a compound of copper and sulfur. The third contact was used to apply an electrostatic potential between the other two contacts that controls or influences the resulting current. It is to say that this device was in the broadest sense comparable to certain today's field-effect transistors like the metal-semiconductor field-effect transistor (MESFET). In the time of his patent invention, it was not feasible to manufacture or implement such a device.

In 1934, the German physicist Oskar Heil developed the first semiconductor field-effect transistor (FET) having an insulated gate contact [3]. Four years later, Boris Davydov [4], Nevill Mott [5] and Walter Schottky [6] independently rectified the work of Oskar Heil. After the detection of the p–n junction by Russel Ohls in 1940, the first concepts of bipolar transistors, so-called point-contact transistors, were invented by the researchers of the Bell Telephone Laboratories William Shockley, John Bardeen and Walter Brattain [7–10]. In 1951, only three years later, the first bipolar junction (p-n) transistors were introduced by Shockley [11]. The first integrated circuit was developed by Jack Kilby of Texas Instruments in 1958 [12]. It was a flip-flop, based on two bipolar transistors.

In the same year, Leo Esaki invented the tunneling diode during his PhD studies in 1958 [13], which was based on the theory of Zener reported in 1934 [14]. The tunneling diode is essentially a p-n junction with a highly n- and p-doped region and a sharp doping transition. The doping concentration must be so high that both regions are in degeneration [15, 16]. In 1973 he was awarded with the Nobel Prize in Physics for the experimental demonstration of the quantum mechanical effect of electron tunneling in solids. The tunneling diode and thus the band-to-band (B2B) tunneling effect was first used commercially in the year 1976 [16].

The today's most important device, the MOSFET, was firstly invented by the Bell Telephone Laboratories engineers Dawon Kahng and Mohamed Atalla in 1959. They developed an electric field controlled semiconductor device that was also the first FET with an insulated gate [17]. Based on different doping processes (nMOS and pMOS), Frank Wanlass and Chih-Tang Sah from Fairchild Semiconductor published the idea of a complementary-MOS (CMOS) technology in 1963 [18]. The CMOS technology enables a low standby power consumption [19] and has become the state-of-the-art in circuit design which is still used.

In 1965 Gordon E. Moore established the theory that the transistor count in fixed-size ICs will increase exponentially [20]. Moore's law predicts that the transistor count on an IC would double every 12 months. Ten years later he rectified his theory and said that the transistor count would double in a time period of two years [21]. Moore's law predicted this development very well but today, considering this law is coming to its end, innovations in terms of device structure and materials are required [22, 23].

With the invention of the CMOS logic in 1963, it was only a matter of time before the first

microprocessor was developed. The first commercially available microprocessor was introduced in November 1971 by Intel. It was the Intel 4004, a 4-Bit-processor with a transistor amount of 2300 and a maximum CPU clock frequency of 740 kHz [24].

In the following years more and more complex ICs were developed, which became smaller and smaller in size with a simultaneously increasing number of transistors on them. As a result, the transistors had to become continuously smaller and therefore some challenges arose in the MOSFET technology that had to be considered in the MOSFET and circuit design. These challenges are accounted in the following section.

1.2 From MOSFET to TFET Technology

The first conventional MOSFET circuits like the Intel 4004 were based on the planar manufacturing process, which was invented by Jean Hoerni in 1959 [25, 26]. Based on Moore's statement, the count of transistors in ICs increased exponentially and thus, the transistor size shrank with the increasing count. The so-called transistor scaling based on Silicon went on for about 30 years and ended at the beginning of the 2000s with the 70 nm node [27]. From this point, the leakage current of the transistors reached an unsustainable amount and negatively affected the switching behavior of the devices. This problem was solved by changing the gate insulator material from SiO_2 to high-κ materials and also using strained Silicon technology [28], so the planar transistor scaling continued for several more years.

Simultaneously to the scaling process, researchers were looking for alternative transistor structures to improve the behavior of the devices. They introduced transistors with more than one gate, the so-called multiple-gate FETs (MuGFETs), in order to enhance the electrostatic control of the transistor channel region and thus to reduce the leakage current [29, 30]. It is to say that MuGFETs are good candidates to reduce the parasitic effects occurring in transistors with a channel length below 100 nm. These parasitic impacts are called short-channel effects (SCEs) [31]. Two examples of SCEs are the threshold voltage roll-off and the drain-induced barrier lowering (DIBL). The first one describes the channel length dependent reduction of the threshold voltage V_{th}. The DIBL characterizes the reduction of the energy barrier within the channel region of the MOSFET in dependency of the drain voltage and therefore, a reduced threshold voltage V_{th}. It should be noted that the reduction of V_{th} causes an unwanted increased OFF-current [32].

A revolutionary invention was presented by Intel in 2011: The 22 nm tri-gate MOSFET [33]. This was the first commercially available 3D device and due to its three gates, SCEs were reduced, the subthreshold slope was improved and the transistor could operate at lower supply voltages which results in reduced power consumption. By introducing the 14 nm process technology in 2014, Intel was able to improve its transistor technology again [34–37]. Based on these technologically improved devices, in 2015 the community of the international technology roadmap for semiconductors (ITRS) tried to predict future technologies in 2015 and intends to lead industry and the research community in this direction. In the ITRS roadmap, a future

with the combination of 3D devices with low power devices has been predicted and has been called “3D Power Scaling” [38]. Nevertheless, Intel continued with research and presented the 3$^{\text{rd}}$ FinFET generation with a 10 nm node [39, 40], which is scheduled to go into series production by the end of 2019. In April 2019, Samsung announced that they have successfully completed their EUV development for the 5 nm FinFET process technology and is ready for costumers' samples [41].

There is going to be a big dilemma in the future in terms of the MOSFET scalability. As the devices are further minimized and the supply voltage is reduced due to lower power consumption, additional parasitic effects occur. The first group is atomic structure related effects like random dopants [42, 43] or gate line edge roughness [44] that negatively influence the transistor behavior. The quantum mechanical effects are the second group that affects the MOSFET performance. When it comes to very thin device thicknesses, quantum confinement negatively influences the threshold voltage V_{th} [45]. For a channel length less than $l_{\text{ch}} < 10$ nm, source-to-drain (SD) tunneling starts to worsen the resulting OFF-state current and the threshold voltage V_{th} [46–48].

Even before the quantum mechanical effects have been observed in fabricated MOSFET technology, researchers tried to take advantage of these parasitic effects. The reason for this is that in the CMOS technology the minimum subthreshold slope S_{th} is physically limited to 60 mV/dec at room temperature due to the thermionic-emission based current transport [49]. Regarding the low power applications in CMOS technology, which means a reduction of the supply voltage, the leakage current in MOSFETs increases due to the DIBL effect and therefore worsens the $I_{\text{ON}}/I_{\text{OFF}}$ ratio. In order to avoid these effects, the community looked for a device whose switching steepness is not affected by a supply voltage reduction. These transistors are called steep slope devices, since they make it possible to obtain resulting subthreshold slopes < 60 mV/dec. One of these devices is the TFET [50–53].

After the commercialization of the Esaki tunneling diode, in 1987 first attempts were made to use the B2B tunneling effect in a MOS capacitor acting like a three terminal tunneling device [54]. The tunneling current between the drain and the substrate was controlled by a gate contact. The TFET, which is basically a gated p-i-n diode, was firstly fabricated and reported independently by two research groups in 2004. The first one was published by Wang from TU Munich, which was based on the planar technology [55] and the second one introduced by Appenzeller of IBM had a carbon nanotube channel and a resulting subthreshold slope of 40 mV/dec [56]. Based on these ideas, the TFET became more attractive and some research groups like IBM, CEA-LETI, IMEC, Forschungszentrum Jülich and the university of Tokyo started to focus on this device. Silicon and SiGe TFETs based on various fabrication technologies and with a subthreshold slope < 60 mV/dec were reported between 2007 and 2013 [57]. For example, IBM reported in 2008 a fabricated Silicon nanowire with a resulting subthreshold slope of 100 mV/dec and an $I_{\text{ON}}/I_{\text{OFF}}$ ratio of about six decades [58, 59]. An other example was shown by Knoll of the Forschungszentrum Jülich in 2013. He reported a fabricated complementary TFET inverter based on Strained Silicon with a smallest S_{th} of 30 mV/dec at

room temperature and ON-currents $I_{\text{ON}} > 10\,\mu\text{A}/\mu\text{m}$ at $V_{\text{ds}} = 0.5\,\text{V}$ [60, 61].

Considering the feasibility to exceed the subthreshold slope limit of 60 mV/dec at room temperature and the full CMOS compatibility, the TFETs are handled as a successor of the conventional MOSFET technology [50, 62]. In general, the TFET is a good candidate for low power applications, but there are still some challenges to be solved. The first one is obtaining an acceptably high I_{ON}, secondly a low S_{th} over several decades and thirdly a low I_{OFF} [63]. A possible way to enhance the TFET performance is the choice of the transistor material. By using heterostructures, which means a different material in the source than in the channel and drain region, all three problems can be improved. One possibility is a combination of a small effective band gap at the source-to-channel junction to obtain a high I_{ON} with a high effective band gap at the drain-to-channel junction to reduce I_{OFF} [63]. In 2011, Dewey from Intel published a III-V heterostructure TFET with a high I_{ON} and a subthreshold slope $< 60\,\text{mV/dec}$ in the range of two decades [64]. Researchers from IBM published in 2016 two different complementary III-V heterostructure TFETs, which unfortunately show a relatively high $S_{\text{th}} \approx 70\,\text{mV/dec}$, but an ON-current of $4\,\mu\text{A}/\mu\text{m}$ in the p-type device [65, 66].

Nonetheless, in these presented TFETs the I_{OFF} was too high and therefore, the parasitic effect of trap-assisted tunneling (TAT) could be seen. The TAT effect occurs mainly in the TFET OFF-state and causes an I_{OFF} and subthreshold slope degradation [67–69]. To this day, many attempts have been made to eliminate this effect and improve the TFET performance. Some possibilities are switching to 2D materials [70, 71], using dopant pockets at the source-to-channel junction [63, 72] or line tunneling [73–75]. In addition, it is possible to combine the advantages of the TFET technology with for instance the negative capacitance (NC) FET as it is shown in [76]. In conclusion, it can be said that the development of the TFET technology is still in its early stages and that further improvements in the technology could make the TFET a very promising candidate in the field of low power applications.

1.3 Device Simulation and the Importance of Compact Modeling

To this day the complexity of ICs has steadily increased and therefore the transistor count on a single chip. Looking back at the first commercialized microprocessor, the Intel 4004 with a transistor count of 2300 [24], it was a big challenge for the engineers to design this chip by hand. In the today's chip design with a transistor density of $37.22\,\text{MT/mm}^2$ (Million transistors per square millimeter) in the 14 nm node of Intel [39] or a density of $100.76\,\text{MT/mm}^2$ in the 10 nm node of Intel [77], it is totally impossible to design a new chip manually. For this reason, it is indispensable to design the chips with the help of a computer-aided program. This was already recognized at the end of the 1960s and therefore, the first computer-aided automatic design program was introduced in [78]. This tool reduced the design errors and the design time.

Due to the high transistor density on a chip and the associated high fabrication costs, nowadays a new chip design is simulated and tested for its functionality before production. For this simulation purpose, compact models are required to describe the behavior of the

used transistors and other components. Compact models are simple mathematical or physical equations for a very time-saving simulation of e.g. novel transistors. Numerical finite element method (FEM) simulations of the novel device are performed to verify the compact models. These numerical simulations also provide an insight into the physical behavior of the device. After a positive evaluation of the device performance in FEM simulations, first device samples can be fabricated to validate and refine the compact models or device simulations. Hence, it can be seen that the development of a compact model is an iterative process and takes some time before it can be commercially utilized.

Device Simulation

In order to improve the performance of existing semiconductor devices or to develop new devices, it is now widely practiced to perform FEM simulations before the novel devices are manufactured. The main advantage of simulating with the FEM method is that the physical behavior of the semiconductor device can be investigated and evaluated before fabrication. Considering the fact that producing novel devices is very expensive, device simulation is a very useful tool to avoid extra costs, in case of a inoperable device, and also helps to save time in the development process.

The device simulation is commonly done in Technology Computer Aided Design (TCAD) programs, like TCAD Sentaurus [79], Silvaco Atlas [80], NDS from Global TCAD solutions [81], DEVSIM TCAD [82] or Cogenda Visual TCAD [83]. In these device simulation tools, the user is able to generate a virtual 2D or 3D device containing the information about geometrical parameters, materials and doping, which is afterwards meshed into small grid points, where within a single grid point all physical quantities are assumed to be constant. After the meshing of the device, every single grid point is iteratively solved with the help of partial differential equation solvers. The simulations of a single device can last from minutes to several days or weeks, depending strongly on the resulting mesh grid and thus the accuracy and the applied physical models. Once the simulation is done, it is possible to investigate for instance the electrostatic potential, electric field or current density within the device. This allows the possible weaknesses such as leakage currents of the device to be detected in the simulation results and by readjusting the device geometry or parameters, the device performance can be enhanced. Considering the fact that the simulations are accurate but very time-consuming, these tools are not suitable to perform complex circuit simulations.

Compact Modeling

In the design of novel semiconductor chips, the engineers are not interested in the detailed device physics as it can be investigated in single device simulations, they rather prefer a simple model that characterizes the DC, AC and transient device behavior very time-efficiently and as accurately as possible. This type of device description is known as the compact model and

bridges the gap between the single device simulation and the simulation of complex electronic circuits.

The computer-aided circuit design and simulation using compact models has become an essential tool for several reasons [31]:

- Designers can reduce errors in the chip design of complex circuits.
- Designers are able to simulate their chips under worst case conditions to consider deviations in the chip fabrication. To do so, they can give a proper statement whether the chip will work or not.
- With the help of the simulations, designers are able to predict the circuit performance and even optimize or enhance the performance.

Some established simulation tools are for instance SPICE [84] from the UC Berkeley, the Quite Universal Circuit Simulator (Qucs) [85] from Mike Brinson's research group or Cadence Virtuoso [86]. A useful tool to extract the compact model parameters is IC-Characterization and Analysis Program (IC-CAP) form Keysight Technologies [87].

Since the compact models are used to predict the behavior of a novel circuit before fabrication, there are some requirements that a compact model has to satisfy [31, 88]:

- A compact model has to reproduce the device terminal current-voltage (I-V) characteristics over all regions of operation of interest accurately and quickly.
- A compact model should include accurate descriptions of the capacitance-voltage (C-V) characteristics, since the model will be used in both static and dynamic circuits simulations.
- In transient simulations, the compact model is probably executed thousands of times and therefore, it is mandatory that the compact model is both computationally efficient and accurate. In addition, it should be as simple as possible but at the same time as accurate as possible. There is always a trade-off between accuracy and simplicity.
- The compact modeling equations should be derived in a form that they can easily be implemented into a SPICE engine or in the hardware description language Verilog-A [89, 90].
- An accuracy of about 5% between the current and capacitance measurements and the compact model is sufficient for use in circuit simulations.
- The device behavior should be described with the help of mathematical equations that are continuous, with continuous first derivatives, although not necessarily in a strictly mathematical sense. The degree of discontinuity must be so small that the resulting errors can be captured by the overall error tolerances of the simulator.

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- A compact model should be scalable in terms of device dimensions and doping concentrations.

Basically, it is possible to distinguish between the following three categories of compact models [31, 88, 91]:

1. *Physics-based analytical models*: In the physics-based models, all modeling equations are derived analytically on the basis of physical laws. In addition, the modeling equations are related to physical parameters of the device such as geometry or doping. However, it should be noted that the model equations must not cover only a certain bias range, rather they have to be continuous from e.g. a MOSFET's subthreshold to above threshold regime. It is also important that a physics-based model behaves "decently" for bias conditions far away from the practical working region of the device, since the compact model may be confronted with unrealistic and impractical conditions during the iteration process of the simulator and this must not endanger the convergence.

   The main advantages of this model type are the feasibility to forecast the electrical device behavior for varying parameters in the physical process, which is very helpful in the parameter extraction and in the circuit design. Furthermore, the rules of geometrical scaling can be confidently applied. The drawbacks of physics-based models are that they are technology dependent and it takes a lot of time (∼years) to develop novel models. Moreover, new devices or alternative structures often require major model modifications or even new modeling approaches.

2. *Table lookup models*: In table lookup models the I-V and C-V characteristics are discretely stored in a database for different bias points and device geometries. The table can be filled with measurements or simulation data obtained by FEM or TCAD simulations. If the table model is executed, the simulator searches for the handover bias point and if this bias point is not included in the table, a spline interpolation between the adjacent points is conducted. The main advantage of a table lookup model over the physics-based model is that they are technology independent and can be developed in relatively short time. The disadvantages are that there is no possibility to get a physical insight into the device physics and the table model is only valid in the measured or simulated bias range. The interpolations outside this range are uncertain and if accuracy is one of the requirements, memory storage size will lead to problems.

3. *Empirical behavior models*: In the empirical behavior model, the derived analytical modeling equations have no relation to the device physics. This model is often used to fit the discrete data in lookup tables in order to eliminate the spline interpolations. The main advantage is the reduced development time in comparison to the physics-based models and the reduced data storage with respect to the table lookup model. The disadvantage is that this model type is not technologically independent to predict changes in the geometrical scaling and the correct correlation between parameters.

In the simulations of a novel circuit it is advantageous to use a physics-based analytical model, if one is available, due to its flexibility in predicting changes in the device parameters. On the other hand, if no physics-based model of a novel device is developed yet, it is more time-efficient to use a table lookup or an empirical behavioral model.

1.4 State of the Art in TFET Compact Modeling

Since the TFET is of interest as a possible successor of the MOSFET technology, many researchers have started to focus on the compact modeling of TFETs. The fundamentals for the mathematical and physical description of the tunneling effect in semiconductors were introduced by E. Kane in 1960 [92, 93]. In 1973, the so-called Tsu-Esaki formula was introduced which describes the tunneling in a superlattice [94], whereby this approach was originally proposed by Duke in 1969 [95]. Most of the today's TFET compact models are based on these approaches.

Because most of the TFET compact model presented in the following are derived for a special device geometry and are not yet suitable for circuit simulations, some research groups used table lookup TFET models [96, 97] or empirical models [98] in order to simulate TFET-based circuits.

In 2008, a research group from IMEC in Belgium published an analytical DC model for a double-gate (DG) TFET considering point and line B2B tunneling and extended the model for single-gate and gate-all-around (GAA) TFETs in 2010 and 2011, respectively [99–101]. Their modeling approach is based on Kane's model, the effect of inversion charges on the potential is neglected and SCEs are not considered in the calculations. Bardon, also part of IMEC, published in 2010 a pseudo-two-dimensional DC model for DG TFETs, which additionally considers the source and drain depletion regions [102]. The electrostatics were solved analytically in two dimensions, where the resulting DC current was obtained by numerical calculations which forbids a usage in circuit simulations. This is also the case in the aforementioned papers.

A surface potential based DC model for a planar TFET was reported in 2011 by Wan et al. [103]. Bhushan et al. presented in 2012 a physics-based analytical model for a planar SOI TFET which includes both the AC and DC behavior of the TFET [104]. The 1D calculations were based on Landauer's tunneling approach and included the parasitic TAT effect as well as SCEs, whereby the AMBIPOLAR behavior was not included in the approach. Due to the characterization of the AC and DC behavior, the model would be suitable for circuit simulations, but the authors did not show any simulation results.

In 2012, a generalized scaling theory for DG interband TFETs was reported by Liu et al. [105]. The B2B tunneling current calculations were based on a 2D analytical potential solution. SCEs are included but inversion charges are neglected, which led to inaccuracies in the above threshold regime of the TFET. In the same year, Gnani et al. presented an analytical DC model for the drain-conductance optimization in nanowire (NW) TFETs [106, 107]. The calculations were based on Landauer's tunneling formula and a simplified band diagram model.

From 2012 to 2014, Zhang et al. from HKUST published several modeling parts of a DG

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TFET, which were combined to an overall TFET model implemented in SPICE [108, 109]. The model includes both the AC and DC behavior of the TFET and first simulations of basic TFET circuits were performed. The presented model provided a good accuracy in terms of the potential and B2B tunneling current. However, the 1D modeling approach did not consider the influence of TAT and the AMBIPOLAR behavior as well as SCEs. Nevertheless, this modeling approach was extended for the consideration of hetero-junctions in 2016 by Dong [110] and the influence of a gate-drain underlap on the B2B tunneling current by Xu in 2017 [111].

Gholizadeh et al. presented a 2D analytical model for DG TFETs in 2014, which incorporated the source and drain depletion regions but neglected the AMBIPOLAR-state of the TFET [112]. In the same year, Vishnoi et al. introduced a compact analytical DC model for dual material gate SOI TFETs, based on a surface potential modeling approach [113]. This approach was extended by the consideration of band gap narrowing and non-abrupt doping profiles [114] and the considerations of inversion charges [115]. In addition, the model was transferred to a GAA structure [116] and to a DG TFET considering the source and drain depletion regions and the AMBIPOLAR behavior of the TFET [117]. Unfortunately, no circuit simulations were performed to demonstrate the model capabilities.

In 2015, several modeling approaches were reported in literature. A simple analytical TFET model for circuit simulations was introduced by Lu et al. in [118]. Taur et al. introduced a hetero-junction DG TFET model [119] and Wu et al. presented an analytical model to consider SCEs in DG TFETs [120]. A Verilog-A implemented AC and DC DG TFET compact model was introduced in the same year by Biswas et al. [121], which was based on the approaches presented in [122, 123]. The depletion regions in source and drain are neglected in the calculations of the 1D surface potential, which limits the model to homo-junction devices. However, it was possible to perform basic TFET circuit simulations in the sense of a benchmarking of homo-junction NW TFETs for basic analog functions [124]. Here, the model was calibrated with measurements of fabricated TFETs.

An analytical DC model of GAA hetero-junction TFETs was reported by Guan et al. in 2018 [125], which is partly based on the work of Vishnoi.

Our workgroup started to focus on the modeling of DG TFETs in 2013. Graef et al. introduced a DC DG TFET model, which was based on an analytical closed-form potential solution and a numerical calculation of the B2B tunneling and TAT current [126–131]. The potential calculations included the depletion regions in source and drain and Gaussian shaped doping profiles of the source and drain regions, but inversion charges were not taken into account. The model also included the consideration of hetero-junctions. Due to the numerical calculations of the device current, circuit simulations were not possible. In 2017, Hosenfeld et al. presented an alternative non-iterative non-equilibrium Green's function (NEGF) based model for the B2B tunneling current in DG TFETs [132].

The model of Graef was transferred to a compact DC model in 2016, where the impact of inversion charges on the electrostatics was considered in the compact model [133]. This compact model opens the possibility to perform the first DC circuit simulations in terms of

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a single-stage TFET inverter [133] and an TFET-based SRAM cell [134]. The compact DC model was extended by an area equivalent WKB approach to calculate the B2B tunneling current more time-efficiently [135], the consideration of hetero-junctions [136] and the TAT effect [137]. In parallel to the development of the DC model, a compact modeling approach of the intrinsic capacitances in DG TFETs was introduced by Farokhnejad et al. [138, 139]. The combination of both model parts AC and DC allowed for the transient simulation and analysis of basic TFET circuits [140, 141].

1.5 Challenges and Outline of the Thesis

This dissertation introduces an innovative 2D compact model for the device current calculation in n-type DG TFETs. The aim of the modeling approach is to find a closed-form equation package, which is based on an analytical-numerical modeling approach presented in [129, 131]. Thus, the following scientific objectives are defined:

1. Derivation of a compact 2D potential solution for the entire device and all operation regimes of the TFET. The calculations of the potential should be done using an existing 2D closed-form solution of the electrostatics in a DG TFET. In addition, the effect of inversion charges and their influence on the electrostatics should be taken into account.

2. The potential solution should be used to derive compact expressions for the band diagram. The considerations of band gap narrowing and of hetero-junctions should be included in the calculations.

3. Deriving a compact expression for the current density in the DG TFET, which includes a closed-form calculation of the tunneling length and tunneling probability. These calculations should include 2D effects.

4. Finding a compact and closed-form integration of the current density to obtain the resulting device current. The device current should include the effect of B2B tunneling and TAT.

5. All modeling equations should be implemented in the hardware description language Verilog-A for a usage in circuit simulations.

6. The compact model should be verified by TCAD Sentaurus simulations and measurement data of fabricated TFETs to identify possible fields of application.

7. The continuity and numerical stability of the compact model should be demonstrated in terms of simulations of basic TFET circuits.

In order to capture all these scientific objectives, the outline of the thesis is presented in the following. After the introduction showing the scientific field in which this work can be classified, the used mathematical and physical preliminaries are introduced in Chap. 2. In this

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chapter, Poisson's and Laplace's equation, the complex potential theory and the conformal mapping technique are explained in detail. These techniques are very useful to solve arbitrary electrostatic problems.

In order to get a solid grasp of the TFET, the fundamentals of this semiconductor device are outlined in Chap. 3. Within this chapter, the quantum mechanical effect of tunneling is introduced and the various tunneling events occurring in semiconductor devices are explained. The investigated device geometry and the working principle of the TFET are also considered in this chapter.

Chapter 4 reviews and also extends the existing 2D closed-form electrostatic potential of the DG TFET [128]. The existing potential solution is derived by solving Laplace's equation with the help of the conformal mapping technique and is therefore only valid in the subthreshold regime of the TFET. In order to extend the model for the above threshold regime of the TFET, the effect of inversion charges is considered in the 2D calculations of the potential. The validity of the model extension and the entire 2D closed-form potential solution is determined with the help of TCAD Sentaurus simulations at the end of this chapter.

In Chap. 5, the compact DC modeling approach is presented. At first, a compact description of the potential within the device is derived in terms of approximations with mathematical functions. The characteristic points and properties of these functions are calculated by means of the 2D potential solution from Chap. 4. After that, the band diagram and a compact equation for the electric field are determined. The compact current density derivation is separated into two parts: In the first part, the compact current density derivation for the B2B tunneling effect is explained in detail. Secondly, the TAT current density expression part is presented. The derivation of a compact equation for the device current including 2D effects finishes this chapter.

The verification of the compact modeling approach is presented in Chap. 6. Firstly, TCAD simulations of the DG TFET are performed to verify the electrostatic potential, band diagram, electric field, tunneling barrier and tunneling generation rate as a part of the modeling approach. The device current is then validated for various device parameter setups. In a second step, the compact model is verified by measurements of fabricated complementary NW GAA TFETs.

In order to demonstrate the numerical robustness and flexibility of the modeling approach, basic TFET circuit simulations are performed in Chap. 7. In this chapter, the compact DC model is used to simulate a single-stage TFET inverter and a TFET-based SRAM cell. The combination of the DC model with an AC model opens up the possibility of performing a transient simulation of an 11-stage ring oscillator.

Chapter 8 concludes and reflects the presented dissertation and presents an outlook on research perspectives in order to further improve the compact model in the future.

CHAPTER 2

Mathematical and Physical Preliminaries

In order to calculate the tunneling current of TFETs, it is essential to have an accurate electrostatic solution. In this chapter the mathematical and physical basics are introduced, which are used in characterizing the electrostatics of a TFET. The Poisson and the Laplace equation are presented in Sec. 2.1, which are well-known equations to describe electrostatic problems. Subsequently, the complex potential theory is introduced in Sec. 2.2, which characterizes a way to describe Laplace's equation in a 2D complex plane. In order to simplify finding a closed-form electrostatic solution within a 2D plane, the conformal mapping technique is detailed in Sec. 2.3.

2.1 Poisson's and Laplace's Equation

The solution of a potential for a given electrostatic problem can be found by solving a partial differential equation on the basis of Maxwell's equations. One of Maxwell's equations is the so-called Gaussian law that relates the electric field $\vec{E}$ to the charge density ϱ:

$$\nabla \cdot \vec{E}(r) = \frac{\varrho(r)}{\varepsilon}, \tag{2.1}$$

where ε represents the constant permittivity of the homogeneous material [142, 143]. The electric field and the potential have also a divergence relationship as follows:

$$\vec{E}(r) = -\,\mathrm{grad}\left(\Phi(r)\right) = -\nabla\Phi(r). \tag{2.2}$$

A combination of Eq. (2.1) and Eq. (2.2) leads to the so-called Poisson equation which defines the correlation between the electrostatic potential and the charge density [143]:

$$\Delta\Phi(r) = -\frac{\varrho(r)}{\varepsilon}, \tag{2.3}$$

whereby Δ describes the Laplace operator. The electrostatic problems in this thesis are 2D or 3D problems and for this reason the Laplace operator is written in Cartesian coordinates [142]:

$$\Delta = \nabla \cdot \nabla = \frac{\partial^2}{\partial x^2} + \frac{\partial^2}{\partial y^2} + \frac{\partial^2}{\partial z^2}, \tag{2.4}$$

so the Poisson equation in Cartesian coordinates yields:

$$\Delta \Phi(x,y,z) = -\frac{\varrho(x,y,z)}{\varepsilon}. \tag{2.5}$$

In the special case that there is no space charge existing ($\varrho = 0$), Poisson's equation is called the Laplace equation [143]:

$$\Delta \Phi(x,y,z) = 0. \tag{2.6}$$

Laplace's equation is a very important special case because it is quite easy to solve electrostatic problems analytically.

Poisson's and Laplace's equation have in general an infinite count of solutions. In order to solve Laplace's equation (Eq. (2.6)), the potential $\Phi(x,y,z)$ must have continuous second-order derivatives in x, y and z and needs to satisfy the Laplace equation. The solutions of Laplace's equation are called *harmonic functions* and hold the principle of superposition [143]. The general solution together with some specific boundary conditions yield to a particular solution of the electrostatic problem. The boundary conditions are distinguished between the Dirichlet condition and the Neumann condition [142]:

1. Dirichlet condition (Boundary value problem of the first kind): The harmonic function $\Phi(x,y,z)$ in an enclosed area A, reaches predetermined values Φ_A at the boundary of A. This boundary value problem is -if at all- clearly solvable.
2. Neumann condition (Boundary value problem of the second kind): The harmonic function $\Phi(x,y,z)$ in an enclosed area A, reaches a predetermined normal derivative $\partial\Phi/\partial\vec{n}|_\mathrm{A}$, where $\vec{n}$ defines the normal vector. This boundary value problem is -if at all- clearly solvable except of one single constant.

In principle, a mixture of both boundary conditions is possible, where one part of the boundary is determined by Dirichlet conditions and the other part of the boundary is defined by Neumann conditions.

2.2 Complex Potential Theory

With the help of the 2D complex potential theory it is possible to find analytical solutions for given 2D field problems more straightforward. The aim of this theory is to find an expression for a complex function in a 2D plane. This function has to fulfill Poisson's or Laplace's equation in the real and imaginary part to obtain an electrostatic solution for given boundary conditions.

In case of the Laplace equation, the derivation starts with the electric field in a region free of space charges in Cartesian coordinates which is given by:

$$\nabla \cdot \vec{E} = \frac{\partial E_x}{\partial x} + \frac{\partial E_y}{\partial y} = 0, \tag{2.7}$$

where the z component of the electric field is constant in space region and thus, not of interest. The electric field components can also be described by the potential, which leads to [144]:

$$E_x = -\frac{\partial \Phi}{\partial x}, \quad E_y = -\frac{\partial \Phi}{\partial y} \;\rightarrow\; E = -\nabla \Phi. \tag{2.8}$$

In addition, the components of the electric field are also expressible by an electric flux function Ξ as follows:

$$E_x = -\frac{\partial \Xi}{\partial y}, \quad E_y = \frac{\partial \Xi}{\partial x} \;\rightarrow\; E = -\nabla \times (\Xi \cdot \vec{e}_z). \tag{2.9}$$

The electrostatic potential Φ and the electric flux function Ξ describe the same electric field. Both terms are dependent from each other, they are linked by the so-called CAUCHY-RIEMANN differential equations:

$$\frac{\partial \Phi}{\partial x} = \frac{\partial \Xi}{\partial y}, \quad \frac{\partial \Phi}{\partial y} = -\frac{\partial \Xi}{\partial x}. \tag{2.10}$$

With the electric flux function, the dielectric flux ξ in z-direction can be determined between two points 1 and 2 as follows:

$$\xi = \varepsilon \int_A E \,\mathrm{d}A = -\varepsilon \cdot \Delta z \cdot (\xi_1 - \xi_2). \tag{2.11}$$

Since the potential $\Phi(x,y)$ and the electric flux function $\Xi(x,y)$ are both dependent on x and y, the following complex variable can be introduced as:

$$\bar{z} = x + \mathrm{j}y, \tag{2.12}$$

which characterizes an arbitrary point P in the complex $\bar{z}$-plane[1] as it is depicted in Fig. 2.1(a). Since complex numbers form a closed number system, it is possible to interpret any function $f(\bar{z}) = \bar{w}$ again as covering a plane with $\bar{w} = u + \mathrm{j}v$. In this case, any point $P'(u,v)$ in $\bar{w}$-plane is then the image of the point $P(x,y)$ within $\bar{z}$-plane, as it is illustrated in Fig. 2.1(b). The following function introduces a complex combination of two real functions, where each function depends on the real variables x and y [143]:

$$\bar{w} = \bar{w}(\bar{z}) = u(x,y) + \mathrm{j}v(x,y). \tag{2.13}$$

The complex function must be regular and analytic, which means it requires single valuedness, continuity and differentiability within the region of interest. The continuity requires that a

1 $\bar{z}$ is not related to the Cartesian coordinate z in the following.

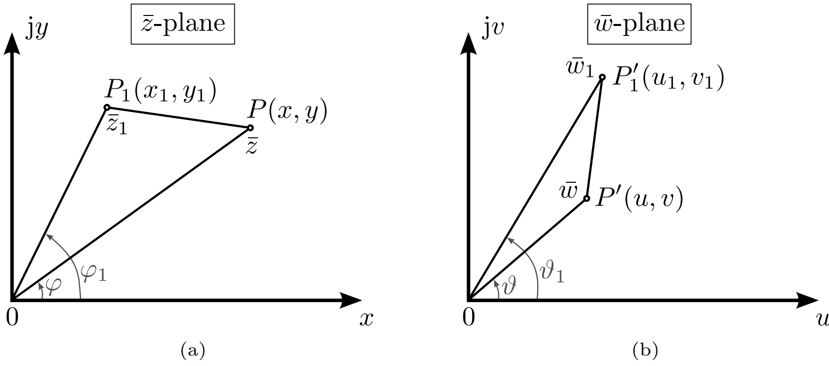

Figure 2.1.: Schematic illustration of a function of a complex variable (a) in $\bar{z}$-plane and (b) the image of the complex function in $\bar{w}(\bar{z})$-plane.

change in $\bar{z}$-plane $\Delta\bar{z}$ is clearly and uniquely related to a change $\Delta\bar{w}$ in $\bar{w}$-plane. On the other hand, differentiability implies that the first partial derivatives of u and v exist, with respect to x and y, and are also continuous. Furthermore the expression $\mathrm{d}\bar{w}/\mathrm{d}\bar{z}$ must exist. This derivative is obtained by:

$$\begin{aligned}\frac{\mathrm{d}\bar{w}}{\mathrm{d}\bar{z}} &= \lim_{\Delta\bar{z}\to 0} \frac{\bar{w}(\bar{z}+\Delta\bar{z}) - \bar{w}(\bar{z})}{\Delta\bar{z}} \\ &= \lim_{\Delta x, \Delta y \to 0} \frac{\left(\frac{\partial u}{\partial x} + \mathrm{j}\frac{\partial v}{\partial x}\right)\cdot\Delta x + \mathrm{j}\left(-\mathrm{j}\frac{\partial u}{\partial y} + \frac{\partial v}{\partial y}\right)\cdot\Delta y}{\Delta x + \mathrm{j}\Delta y}, \end{aligned} \tag{2.14}$$

wherein only if the this derivative is independent from the direction of $\Delta\bar{z}$, then the function is unique. Defining $\Delta y = \alpha\Delta x$ [144], then α identifies the $\Delta\bar{z}$ direction and the derivative yields:

$$\frac{\mathrm{d}\bar{w}}{\mathrm{d}\bar{z}} = \lim_{\Delta x\to 0} \frac{\left(\frac{\partial u}{\partial x} + \mathrm{j}\frac{\partial v}{\partial x}\right) + \mathrm{j}\left(-\mathrm{j}\frac{\partial u}{\partial y} + \frac{\partial v}{\partial y}\right)\alpha}{1+\mathrm{j}\alpha}, \tag{2.15}$$

where $\mathrm{d}\bar{w}/\mathrm{d}\bar{z}$ is only independent from α if the terms in the parentheses in the numerator are equal:

$$\frac{\partial u}{\partial x} + \mathrm{j}\frac{\partial v}{\partial x} = -\mathrm{j}\frac{\partial u}{\partial y} + \frac{\partial v}{\partial y}. \tag{2.16}$$

Rearranging Eq. (2.16) leads again to the CAUCHY-RIEMANN differential equations [144]:

$$\frac{\partial u}{\partial x} = \frac{\partial v}{\partial y}, \quad \frac{\partial u}{\partial y} = -\frac{\partial v}{\partial x}. \tag{2.17}$$

The complex function $\bar{w}(\bar{z})$ is called analytical if the CAUCHY-RIEMANN conditions are fulfilled and furthermore, the derivation at singular points fulfills the conditions $\mathrm{d}\bar{w}/\mathrm{d}\bar{z} \neq 0$ and $\mathrm{d}\bar{w}/\mathrm{d}\bar{z} \neq \infty$. If $\bar{w}$ is analytical, then the real and imaginary part of the complex function fulfill Laplace's equation, which can be proven by taking the derivative of the CAUCHY-RIEMANN conditions in

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Eq. (2.17) with respect to x and y. It follows:

$$\frac{\partial^2 u}{\partial x^2} = \frac{\partial^2 v}{\partial x \partial y}, \quad \frac{\partial^2 u}{\partial y^2} = \frac{\partial^2 v}{\partial x \partial y} \tag{2.18}$$

and eliminating the mixed derivatives regarding x and y, yields:

$$\frac{\partial^2 u}{\partial x^2} + \frac{\partial^2 u}{\partial y^2} = 0, \quad \frac{\partial^2 v}{\partial x^2} + \frac{\partial^2 v}{\partial y^2} = 0. \tag{2.19}$$

Both functions u and v can represent the potential solution of a 2D electrostatic problem. If u is the potential, then v represents the electric flux function and vice versa. The electric field is then directly obtained by the complex function $\bar{w}$, which is also called *complex potential.* The complex electric field in general is written as:

$$\bar{E} = E_x + \mathrm{j}E_y \tag{2.20}$$

and rewriting Eq. (2.13) in terms of the potential function and electric flux function leads to:

$$\bar{w}(\bar{z}) = \varPhi(x,y) + \mathrm{j}\varXi(x,y). \tag{2.21}$$

In the case that u is the potential function ($u = \varPhi$), the electric field is determined by:

$$\bar{E} = -\frac{\partial \varPhi}{\partial x} - \mathrm{j}\frac{\partial \varPhi}{\partial y} = -\left(\frac{\partial \varPhi}{\partial x} - \mathrm{j}\frac{\partial \varXi}{\partial x}\right) = -\left(\frac{\mathrm{d}\bar{w}}{\mathrm{d}\bar{z}}\right)^*, \tag{2.22}$$

where $\bar{w}^*$ is the complex conjugate value of $\bar{w}$.

2.3 Conformal Mapping Technique

The conformal mapping is a transformation technique, which allows to transfer a potential problem of a geometry in the complex $\bar{z}$-plane into the complex $\bar{w}$-plane and vice versa using an analytic function $\bar{w} = f(\bar{z})$. If the field lines $\varPhi$ in $\bar{z}$-plane are perpendicular to the equipotential lines $\varXi$ (see Fig. 2.2(a)), the field lines $\varPhi'$ in $\bar{w}$-plane must also be orthogonal to the equipotential lines $\varXi'$ (see Fig. 2.2(b)), otherwise the transformation is not analytic and therefore not conformal.

The conformal mapping simplifies finding a closed-form solution of the complex potential problem in $\bar{w}$-plane, by transforming the complex geometrical problem in $\bar{z}$-plane into a much easier problem in $\bar{w}$-plane [143]:

$$\bar{P}(\bar{w}) = \varPhi'(u,v) + \mathrm{j}\varXi'(u,v), \tag{2.23}$$

where the real part $\varPhi'$ and the imaginary part $\varXi'$ both are still harmonic functions and fulfill the Laplace equation as it is mentioned in the complex potential theory (see Sec. 2.2). Since Laplace's equation is invariant to conformal mapping, the electric field in $\bar{w}$-plane is required

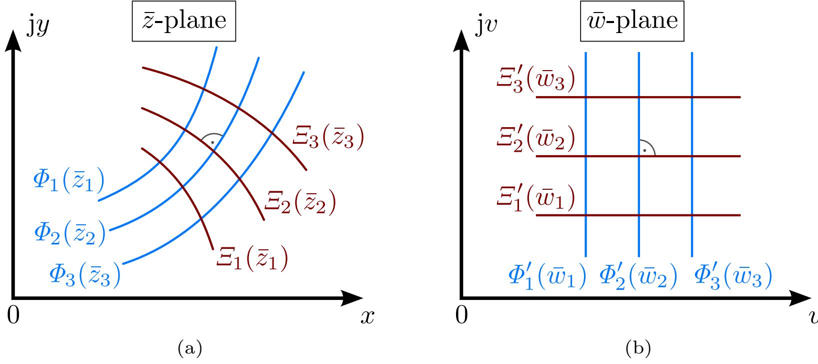

Figure 2.2.: Complex potential problem within (a) the $\bar{z}$-plane that is imaged with the help of the mapping function $\bar{w} = f(\bar{z})$ into $\bar{w}$-plane shown in (b).

to be scaled with respect to the geometry to obtain the electric field in $\bar{z}$-plane [143]:

$$|\vec{E}|_{(\bar{z})} = |\vec{E}|_{(\bar{w})} \cdot \left|\frac{\mathrm{d}\bar{w}}{\mathrm{d}\bar{z}}\right|. \tag{2.24}$$

When considering Poisson's equation, the space charge ϱ also needs to be scaled by:

$$\varrho_{(\bar{z})} = \varrho_{(\bar{w})} \cdot \left|\frac{\mathrm{d}\bar{w}}{\mathrm{d}\bar{z}}\right|^{-2} \tag{2.25}$$

since Poisson's equation must be invariant regarding the conformal mapping [143].

2.3.1 Mapping of a Closed Polygon

In a 2D potential problem the geometry of a transistor can be specified by a closed polygon in the complex $\bar{z}$-plane as it is illustrated in Fig. 2.3(a). In order to simplify the solution of Poisson's or Laplace's equation, the Schwarz-Christoffel transformation maps the boundary value problem in $\bar{z}$-plane into the upper half of the complex $\bar{w}$-plane. The Schwarz-Christoffel transformation is defined by [143]:

$$\frac{\mathrm{d}\bar{z}}{\mathrm{d}\bar{w}} = C_1 \cdot (\bar{w} - \bar{w}_1)^{-\gamma_1} \cdot (\bar{w} - \bar{w}_2)^{-\gamma_2} \ldots (\bar{w} - \bar{w}_n)^{-\gamma_n} = C_1 \cdot \prod_{i=1}^{n} (\bar{w} - \bar{w}_i)^{-\gamma_i} \tag{2.26}$$

and maps the real u-axis of the $\bar{w}$-plane (see Fig. 2.3(b)) into the boundary lines of the polygon in $\bar{z}$-plane (see Fig. 2.3(a)). The term $(\bar{w} - \bar{w}_i)$ changes its sign at every single point $\bar{w}_i$ that forms the polygon. This causes an angle change in $\mathrm{d}\bar{z}$ by exactly $\alpha_i = \pi\gamma_i$, whereby the direction is indicated by the sign of γ_i. The constant C_1 describes a factor which includes the scale and rotation and is determined by the correlation of one of the polygon sides $(\bar{z}_i - \bar{z}_{i+1})$ with its image $(\bar{w}_i - \bar{w}_{i+1})$. In order to come to the mapping function $\bar{z} = f(\bar{w})$ and to solve

for the constant C_1, Eq. (2.26) needs to be integrated. The integration yields to:

$$\bar{z}(\bar{w}) = C_1 \cdot \int \prod_{i=1}^{n} (\bar{w} - \bar{w}_i)^{-\gamma_i} \, \mathrm{d}\bar{w} + C_2, \tag{2.27}$$

where the integration constant C_2 essentially indicates the origin of the $\bar{z}$-plane. Solving the integral in Eq. (2.27) for a given boundary value problem, it is possible to map every single point from the $\bar{w}$-plane into the complex $\bar{z}$-plane. In order to find a solution for the boundary value problem it is necessary to know the function that maps an arbitrary point $\bar{z}$ from the $\bar{z}$-plane into the $\bar{w}$-plane. This needed expression is obtained by finding the inverse function of the solution of Eq. (2.27):

$$\bar{w}(\bar{z}) = f^{-1}(\bar{z}) \tag{2.28}$$

and is called inverse mapping function.

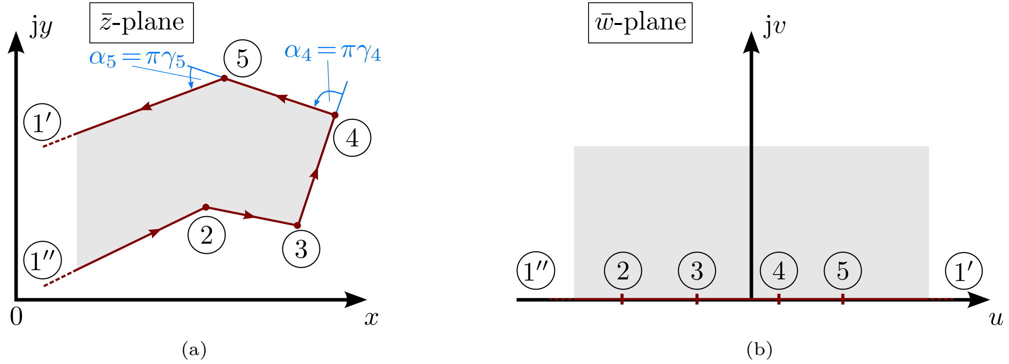

Figure 2.3.: Complex potential problem within (a) the $\bar{z}$-plane that is imaged with the help of the mapping function $\bar{w} = f(\bar{z})$ into $\bar{w}$-plane shown in (b).

For a practical and easy application of the Schwarz-Christoffel function the following points should be considered [143]:

1. The order of vertex points in the $\bar{z}$-plane must be in the same order as in the $\bar{w}$-plane.
2. The region to be transformed in $\bar{z}$-plane is at the left of the polygon lines (see Fig. 2.3(a)).
3. All angles γ_i are counted positive counterclockwise.
4. Three of the vertex images $\bar{w}_i$ can be chosen freely by a conformal mapping in the upper half of the $\bar{w}$-plane. It is to say, that the vertex images should be set that Eq. (2.27) is solvable as easy as possible.
5. The vertex image $\bar{w} = \pm\infty$ does not occur in Eq. (2.26).
6. An angle of $\gamma_k = +1$ represents a vertex at $\bar{z}_k = \infty$ or an intersection of two parallel lines.

The distance between these two parallel lines is then defined by:

$$\bar{z}_k'' - \bar{z}_k' = -\mathrm{j}\pi C_1 \cdot \left[\prod_{k\neq i}(\bar{w}_k - \bar{w}_i)^{-\gamma_i}\right], \tag{2.29}$$

whereby, if the corresponding vertices in $\bar{w}$-plane are chosen to be $\bar{w}_k' = +\infty$ and $\bar{w}_k'' = -\infty$, Eq. (2.29) is simplified to:

$$\bar{z}_k'' - \bar{z}_k' = \mathrm{j}\pi C_1. \tag{2.30}$$

2.3.2 Potential Solution for Boundary Conditions of First Kind

In case of a more general geometry defined by any closed curve or domain without ordinary double points[1], the interior space can be mapped into the interior space of the unit circle (see Fig. 2.4(a)) in a one-to-one conformal manner. This technique is called Riemann's fundamental theorem [143]. In fact it is challenging to find a suitable mapping function for the original boundary curve, therefore, in practice several mappings or approximations should be performed.

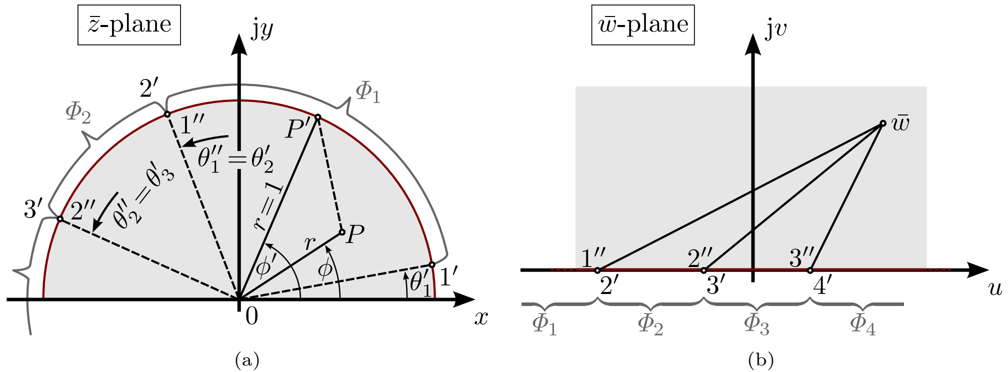

Figure 2.4.: (a) Complex potential solution of a Dirichlet boundary problem on a unit circle. (b) Conformal mapped solution of a first kind boundary condition. The unit circle is mapped in the upper half of the complex $\bar{w}$-plane.

If a function exists, which maps a general geometry into a unit circle, then it would be possible to solve any potential problem with Dirichlet boundary conditions given by means of Poisson's integral:

$$\Phi = \frac{1}{2\pi} \cdot \int_0^{2\pi} \frac{1 - r^2}{1 - 2r \cdot \cos(\phi - \phi') + r^2} \cdot \Phi(\phi')\,\mathrm{d}\phi', \tag{2.31}$$

whereby the complex variable in $\bar{z}$-plane is defined by $\bar{z} = r \cdot \exp(\mathrm{j}\phi)$ and shows an arbitrary point P within the unit circle (see Fig. 2.4(a)) and ϕ' describes a point P' on the unit circle

1 It means that the curve does not intersects itself.

with $r = 1$.

Using the complex potential function of Schwarz for an application in $\bar{z}$-plane leads to:

$$\bar{P} = \frac{1}{2\pi} \cdot \int_{0}^{2\pi} \frac{\exp(\mathrm{j}\phi') + \bar{z}}{\exp(\mathrm{j}\phi') - \bar{z}} \cdot \Phi(\phi')\,\mathrm{d}\phi' \equiv \Phi + \mathrm{j}\Xi, \tag{2.32}$$

where the real part Φ is defined by Eq. (2.31).

For the most mapping problems it is easier to map in the upper half of the $\bar{w}$-plane than mapping upon the unit circle. Therefore, the unit circle is mapped into the upper half $\bar{w}$ with the help of the following function:

$$\bar{w}(\bar{z}) = \mathrm{j}\frac{1 - \bar{z}}{1 + \bar{z}}. \tag{2.33}$$

The complex potential solution of Schwarz can be rearranged by applying:

$$\bar{z} = -\frac{\bar{w} - \mathrm{j}}{\bar{w} + \mathrm{j}}, \quad \exp(\mathrm{j}\phi') = -\frac{u' - \mathrm{j}}{u' + \mathrm{j}}, \quad \mathrm{d}\phi' = \frac{2\mathrm{d}u'}{1 + u'^2}, \tag{2.34}$$

which results in:

$$\bar{P} = \frac{\mathrm{j}}{\pi} \cdot \int_{-\infty}^{\infty} \frac{1 + u'\bar{w}}{(1 + u'^2) \cdot (\bar{w} - u')} \Phi(u')\,\mathrm{d}u' = \Phi + \mathrm{j}\Xi. \tag{2.35}$$

This is the general solution of a Dirichlet boundary problem in the upper half of the $\bar{w}$-plane. The term u' describes the integration variable along the u-axis and $\bar{w}$ is an arbitrary point where the potential $\bar{P}$ exists. The real part of Eq. (2.35) leads to the equivalent representation of Poisson's integral on the unit circle (see Eq. (2.31)):

$$\Phi = \frac{1}{\pi} \cdot \int_{-\infty}^{+\infty} \frac{v}{(u - u')^2 + v^2} \cdot \Phi(u')\,\mathrm{d}u', \tag{2.36}$$

thereby the term $\Phi(u')$ describes the conformal mapped boundary condition in the area of interest by using the inverse mapping function (see Eq. (2.28)):

$$\Phi(u') = \Phi\big(f^{-1}(\bar{z}')\big). \tag{2.37}$$

UNIVERSITAT ROVIRA I VIRGILI
COMPACT DC MODELING OF TUNNEL-FETS
Fabian Horst

CHAPTER 3

Fundamentals of the TFET

This chapter presents the fundamentals and the physical basics of TFETs. Regarding the fact that the current transport in TFETs is based on tunneling, firstly the quantum mechanical effect of tunneling through an energy barrier is considered. After that, the TFET device geometry is introduced and followed by its working principle. The working principle is explained in detail by presenting its three operation regimes and the occurring quantum mechanical effects.

3.1 Tunneling Effect

The tunneling effect can be described by highlighting the differences of classical mechanics and quantum physics. In this case a simple potential well is considered. Starting with classical mechanics, electrons with lower energy than the energy barrier are completely confined by the potential walls. The electrons that overcome the energy barrier of the potential wall are able to escape and contribute to the resulting current. This effect is called thermionic emission. In contrast to that, quantum mechanics opens the possibility that a carrier can penetrate into and through an energy barrier. This phenomenon is called quantum mechanical tunneling or tunneling effect. The effect is described by the fundamental statement that a carrier penetration through a barrier with a finite width and height has a nonzero tunneling probability [32, 145]. For this reason, the calculation of the tunneling probability is introduced in the following section for two basic exemplary energy barriers.

3.1.1 Tunneling Probability

In order to find a solution for the tunneling probability, the wavefunction Ψ has to be determined with the help of the 1D time-independent Schrödinger equation:

$$-\frac{\hbar^2}{2m^*} \cdot \frac{\mathrm{d}^2 \Psi(x)}{\mathrm{d}x^2} + U(x) \cdot \Psi(x) = E \cdot \Psi(x), \tag{3.1}$$

where $U(x)$ characterizes a general energy barrier, E defines the considered energy level of the carrier, $\hbar$ is the reduced Planck's constant and m^* is the effective carrier mass [145].

The determination of the wavefunction Ψ is derived for a rectangular and a triangular energy barrier in the following.

Rectangular Energy Barrier

At first a rectangular energy barrier with a height of U_0 and a width of W as it is shown in Fig. 3.1(a) is investigated. The carrier in Region I with its wavefunction Ψ_I incidents the energy barrier at the position x_1, penetrates into and tunnels through it and comes out at the position x_2. Due to the fact that a part of the incoming wave is reflected at x_1, the wavefunction coming out in Region II has a reduced amplitude.

The term describing the energy barrier $U(x)$ is defined by:

$$U(x) = \begin{cases} 0, & x < x_1 \\ U_0, & x_1 \leq x \leq x_2 \\ 0, & x > x_2 \end{cases} . \tag{3.2}$$

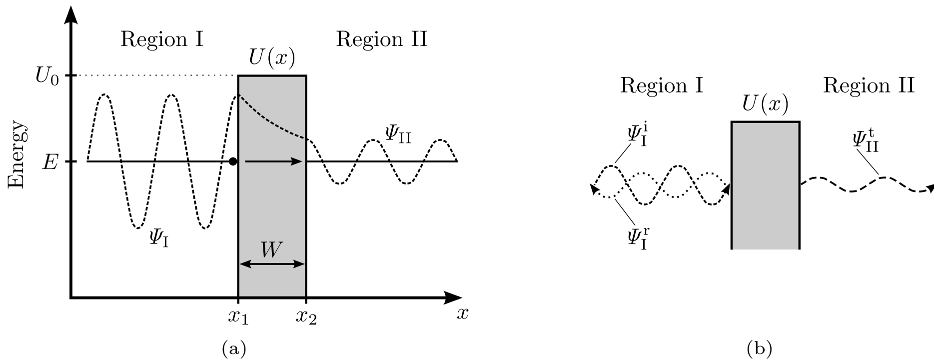

Figure 3.1.: (a) Wavefunctions illustrating carrier tunneling through a rectangular energy barrier [32]. (b) Wavefunction components [145].

As it can be seen in Fig. 3.1(b) the wavefunction Ψ_I consists of a linear superposition of two parts, the incoming wavefunction $\Psi_\mathrm{I}^\mathrm{i}$ and the reflected wavefunction $\Psi_\mathrm{I}^\mathrm{r}$. Therefore, the wavefunction Ψ_I in Region I results in the general solution of Schrödinger's equation for a free particle [145]:

$$\Psi_\mathrm{I}(x) = \Psi_\mathrm{I}^\mathrm{i}(x) + \Psi_\mathrm{I}^\mathrm{r}(x) = A \cdot \exp(+\mathrm{j}k_1 \cdot x) + B \cdot \exp(-\mathrm{j}k_1 \cdot x), \tag{3.3}$$

where A and B are complex constants. The wave vector k_1 is given by:

$$k_1 = \sqrt{\frac{2m^* \cdot E}{\hbar^2}}. \tag{3.4}$$

Schrödinger's equation within the energy barrier (I → II) using Eq. (3.1) is written as:

$$\frac{\hbar^2}{2m^*} \cdot \frac{\mathrm{d}^2 \Psi_{\mathrm{I}\to\mathrm{II}}(x)}{\mathrm{d}x^2} = \big(U(x) - E\big) \cdot \Psi_{\mathrm{I}\to\mathrm{II}}(x) \tag{3.5}$$

and by assuming that the considered energy of the carrier is smaller than the barrier height (i.e. $E < U_0$), the solution of the wavefunction is given by:

$$\Psi_{\mathrm{I}\to\mathrm{II}}(x) = C \cdot \exp(k_2 \cdot x) + D \cdot \exp(-k_2 \cdot x). \tag{3.6}$$

The parameters C and D are complex constants and the wave vector k_2 is defined by:

$$k_2 = \sqrt{\frac{2m^* \cdot (U_0 - E)}{\hbar^2}}. \tag{3.7}$$

In Region II, the wavefunction of the transmitted carrier can be solved by using Schrödinger's equation for a free particle again and since the carrier only has a positive momentum, the solution yields:

$$\Psi_{\mathrm{II}}(x) = \Psi^{\mathrm{t}}_{\mathrm{II}}(x) = F \cdot \exp(+\mathrm{j}k_1 \cdot x), \tag{3.8}$$

where F is a complex constant and k_1 is the wave vector defined in Eq. (3.4).

Now the wavefunctions of the three regions can be combined to:

$$\Psi(x) = \begin{cases} \Psi^{\mathrm{i}}_{\mathrm{I}}(x) + \Psi^{\mathrm{r}}_{\mathrm{I}}(x), & x < x_1 \\ \Psi_{\mathrm{I}\to\mathrm{II}}(x), & x_1 \le x \le x_2 \\ \Psi^{\mathrm{t}}_{\mathrm{II}}(x), & x > x_2. \end{cases} \tag{3.9}$$

The complex constants A, B, C, D and F of the wavefunction $\Psi(x)$ are solved by defining specific boundary conditions at the positions $x = x_1$ and $x = x_2$, assuming continuity and differentiability of the wavefunctions. Applying the first boundary condition at the position $x = x_1$ leads to:

$$\begin{gathered} \Psi_{\mathrm{I}}(x_1) = \Psi_{\mathrm{I}\to\mathrm{II}}(x_1) \\ A \cdot \exp(+\mathrm{j}k_1 \cdot x_1) + B \cdot \exp(-\mathrm{j}k_1 \cdot x_1) = C \cdot \exp(+k_2 \cdot x_1) + D \cdot \exp(-k_2 \cdot x_1) \end{gathered} \tag{3.10}$$

and the differentiability results in the second one:

$$\begin{gathered} \frac{\mathrm{d}\,\Psi_{\mathrm{I}}(x_1)}{\mathrm{d}x} = \frac{\mathrm{d}\,\Psi_{\mathrm{I}\to\mathrm{II}}(x_1)}{\mathrm{d}x} \\ \mathrm{j}k_1 \cdot \big(A \cdot \exp(+\mathrm{j}k_1 \cdot x_1) - B \cdot \exp(-\mathrm{j}k_1 \cdot x_1)\big) = k_2 \cdot \big(C \cdot \exp(+k_2 \cdot x_1) - D \cdot \exp(-k_2 \cdot x_1)\big). \end{gathered} \tag{3.11}$$

At the $x = x_2$, the first boundary condition reads as follows:

$$\begin{aligned} \Psi_{\mathrm{I}\to\mathrm{II}}(x_2) &= \Psi_{\mathrm{II}}(x_2) \\ C \cdot \exp(+k_2 \cdot x_2) + D \cdot \exp(-k_2 \cdot x_2) &= F \cdot \exp(+\mathrm{j}k_1 \cdot x_2). \end{aligned} \tag{3.12}$$

The second boundary condition at $x = x_2$ is defined by:

$$\begin{aligned} \frac{\mathrm{d}\,\Psi_{\mathrm{I}\to\mathrm{II}}(x_2)}{\mathrm{d}x} &= \frac{\mathrm{d}\,\Psi_{\mathrm{II}}(x_2)}{\mathrm{d}x} \\ k_2 \cdot \big(C \cdot \exp(+k_2 \cdot x_2) - D \cdot \exp(-k_2 \cdot x_2)\big) &= \mathrm{j}k_1 \cdot F \cdot \exp(+\mathrm{j}k_1 \cdot x_2). \end{aligned} \tag{3.13}$$

To solve the five unknown parameters one more boundary condition is considered by the ratio of the probability density of the incoming carrier $|\Psi_{\mathrm{I}}^{\mathrm{i}}|^2$ and the transmitted carrier $|\Psi_{\mathrm{II}}^{\mathrm{t}}|^2$. The probability density ratio characterizes the tunneling probability:

$$T_{\mathrm{tun}} = \frac{|\Psi_{\mathrm{II}}^{\mathrm{t}}|^2}{|\Psi_{\mathrm{I}}^{\mathrm{i}}|^2} = \frac{|F \cdot \exp(+\mathrm{j}k_1 \cdot x)|^2}{|A \cdot \exp(+\mathrm{j}k_1 \cdot x)|^2} = \frac{|F|^2}{|A|^2}, \tag{3.14}$$

which is simultaneously the ratio of squared amplitudes of the incoming and transmitted carrier wavefunction.

A solution for T_{tun} is found by applying the boundary conditions of Eq. (3.10) – (3.13) to Eq. (3.14) [145–147]. For the case $E < U_0$ follows:

$$\begin{aligned} T_{\mathrm{tun}} &= \frac{1}{1 + \left(\frac{k_1^2 + k_2^2}{2k_1 k_2}\right)^2 \cdot \sinh^2(k_2 \cdot (x_2 - x_1))} \\ &= \frac{1}{1 + \frac{U_0^2}{4E \cdot (U_0 - E)} \cdot \sinh^2\left(\frac{W}{\hbar} \cdot \sqrt{2m^* \cdot (U_0 - E)}\right)} \end{aligned} \tag{3.15}$$

and for $E > U_0$:

$$\begin{aligned} T_{\mathrm{tun}} &= \frac{1}{1 + \left(\frac{k_1^2 + k_2^2}{-2k_1 k_2}\right)^2 \cdot \sin^2(-k_2 \cdot (x_2 - x_1))} \\ &= \frac{1}{1 + \frac{U_0^2}{4E \cdot (U_0 - E)} \cdot \sin^2\left(\frac{W}{\hbar} \cdot \sqrt{2m^* \cdot (U_0 - E)}\right)}, \end{aligned} \tag{3.16}$$

whereby in the case $E > U_0$, T_{tun} describes the transmission coefficient, which is well known as thermionic emission.

Triangular Energy Barrier

The rectangular energy barrier is introduced as an initial example to understand the basics of tunneling. The most of the energy barriers do not have a rectangular shape, which means that the barrier shape $U(x)$ varies along the x-axis. Since the band diagram in a TFET is more

similar to a triangle than to a rectangular, the tunneling of carriers through a triangular shaped energy barrier is examined in this part. A schematic sketch of such a barrier is illustrated in Fig. 3.2. The solution of Schrödinger's equation for a varying U is mathematically very challenging, which brings us to the method developed by Wentzel [148], Kramers [149] and Brillouin [150], the so-called WKB approximation [151].

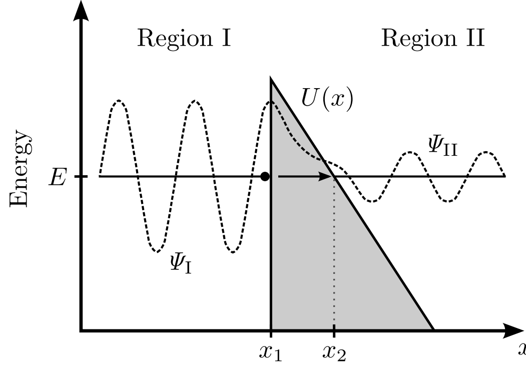

Figure 3.2.: Illustration of a carrier's wavefunction tunneling through a triangular energy barrier [146].

The essential idea of the WKB approach is that a carrier moves through a region with a "constant" external voltage $U(x)$, which is not constant. But if $U(x)$ varies only slowly in the distance of the wavelength $\lambda = {}^{2\pi}/_{k}$, then many full wavelengths are contained over a region and thus the potential is essentially constant and the solution remains practically exponential [151]. For the case that $E < U(x)$ the wavefunction Ψ is exponential within the energy barrier:

$$\Psi(x) = \Theta(x) \cdot \exp(\pm k_3(x)), \tag{3.17}$$

with:

$$k_3(x) = \sqrt{\frac{2m^* \cdot (U(x) - E)}{\hbar^2}} \tag{3.18}$$

and if $U(x)$ is not constant, but varies slowly in comparison with ${}^{1}/_{k_3(x)}$, the solution of the wavefunction stays practically exponential. Under this condition, both terms $\Theta(x)$ and $k_3(x)$ are a slowly varying functions in dependency of x.

The approach begins with rearranging Eq. (3.1) as:

$$\frac{\mathrm{d}^2\Psi(x)}{\mathrm{d}x^2} = \big(k_3(x)\big)^2 \cdot \Psi(x) \tag{3.19}$$

and rewriting the wavefunction in terms of its magnitude and phase:

$$\Psi(x) = \Theta(x) \cdot \exp\big(j\phi(x)\big), \tag{3.20}$$

where $\Theta(x)$ and $\phi(x)$ are both real functions of x. Substituting Eq. (3.20) in Eq. (3.19) yields:

$$\frac{\mathrm{d}^2\Theta}{\mathrm{d}x^2} + 2\mathrm{j}\cdot\frac{\mathrm{d}\Theta}{\mathrm{d}x}\cdot\frac{\mathrm{d}\phi}{\mathrm{d}x} + \mathrm{j}\Theta\cdot\frac{\mathrm{d}^2\phi}{\mathrm{d}x^2} - \Theta\cdot\left(\frac{\mathrm{d}\phi}{\mathrm{d}x}\right)^2 = k_3^2\cdot\Theta, \tag{3.21}$$

which is equivalent to two real equations describing the real and imaginary part separately:

$$\frac{\mathrm{d}^2\Theta}{\mathrm{d}x^2} - \Theta\cdot\left(\frac{\mathrm{d}\phi}{\mathrm{d}x}\right)^2 = k_3^2\cdot\Theta \;\Rightarrow\; \frac{\mathrm{d}^2\Theta}{\mathrm{d}x^2} = \Theta\cdot\left[\left(\frac{\mathrm{d}\phi}{\mathrm{d}x}\right)^2 + k_3^2\right] \tag{3.22}$$

and

$$2\mathrm{j}\cdot\frac{\mathrm{d}\Theta}{\mathrm{d}x}\cdot\frac{\mathrm{d}\phi}{\mathrm{d}x} + \mathrm{j}\Theta\cdot\frac{\mathrm{d}^2\phi}{\mathrm{d}x^2} = 0 \;\Rightarrow\; \frac{\mathrm{d}}{\mathrm{d}x}\left(\Theta^2\cdot\frac{\mathrm{d}\phi}{\mathrm{d}x}\right) = 0. \tag{3.23}$$

Solving Eq. (3.23) results in the relation between the amplitude Θ and the phase ϕ of the wavefunction Ψ shown in Eq. (3.20):

$$\Theta^2\cdot\frac{\mathrm{d}\phi}{\mathrm{d}x} = C^2 \Rightarrow \Theta = \frac{C}{\sqrt{\left|\frac{\mathrm{d}\phi}{\mathrm{d}x}\right|}}, \tag{3.24}$$

whereby C is a real constant. Equation (3.22) has no general solution and from this point of the derivation the approximation is introduced. Assuming that the amplitude $\Theta(x)$ varies slowly with x and for this reason the term ${}^{\mathrm{d}^2\Theta}/_{\mathrm{d}x^2}$ is approximately equal to zero. Hence, Eq. (3.22) is rewritten as:

$$\left(\frac{\mathrm{d}\phi(x)}{\mathrm{d}x}\right)^2 = -k_3^2. \tag{3.25}$$

The phase is solved as follows:

$$\phi(x) = \pm\,\mathrm{j}\int |k_3(x)|\,\mathrm{d}x \tag{3.26}$$

and by using this solution as well as Eq. (3.20) and Eq. (3.24), the wavefunction results in:

$$\Psi(x) \cong \frac{C}{\sqrt{|k_3(x)|}}\cdot\exp\left(\pm\int |k_3(x)|\,\mathrm{d}x\right). \tag{3.27}$$

By applying this solution, the wavefunction within the energy barrier (see Fig. 3.2) is given by:

$$\Psi_{\mathrm{I}\rightarrow\mathrm{II}}(x) \cong \frac{C}{\sqrt{|k_3(x)|}}\cdot\exp\left(+\int_x |k_3(x)|\,\mathrm{d}x\right) + \frac{D}{\sqrt{|k_3(x)|}}\cdot\exp\left(-\int_x |k_3(x)|\,\mathrm{d}x\right), \tag{3.28}$$

where C is the amplitude of the incoming wave component and D is the amplitude of the reflected wave component.

The tunneling probability is defined by the ratio of the probability density of the incident wave and the transmitted part ${}^{|F|^2}/_{|A|^2}$ (see Eq. (3.14)). By assuming an energy barrier with either a large barrier height or a large width, which is the case in most practical situations,

the wavefunction within the barrier is shaped like it is depicted in Fig. 3.3. Consequently, the increasing exponential term in Eq. (3.28), which is presented by the constant C, must be small in comparison to D. Thus, the amplitude ratio of the incoming and transmitted wave is determined by the decreasing term of Eq. (3.28) within the energy barrier:

$$\frac{|F|}{|A|} \propto \exp\left(-\int_{x_1}^{x_2} |k_3(x)|\,\mathrm{d}x\right). \tag{3.29}$$

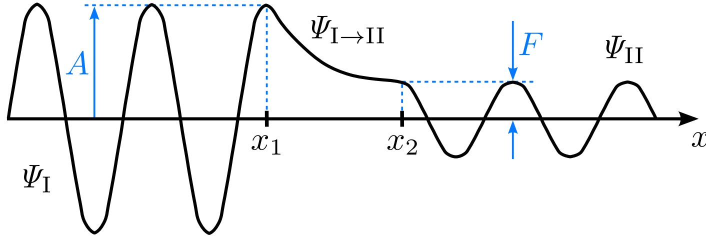

Figure 3.3.: Schematic wavefunction tunneling through a high or/and broad energy barrier, located between x_1 and x_2 [151].

Applying the preliminary considerations in Eq. (3.29) leads to the tunneling probability:

$$\begin{aligned} T_{\mathrm{tun}} = \frac{|F|^2}{|A|^2} &\cong \exp\left(-2\cdot\int_{x_1}^{x2} |k_3(x)|\,\mathrm{d}x\right) \\ &= \exp\left(-2\cdot\int_{x_1}^{x2} \left|\sqrt{\frac{2m^*\cdot(U(x)-E)}{\hbar^2}}\right|\,\mathrm{d}x\right). \end{aligned} \tag{3.30}$$

Up to this point the tunneling probability is derived for a energy barrier $U(x)$, that varies slowly along the x-axis. Now, considering a triangular energy barrier (see Fig. 3.2) represented by a linear function $U(x)$ between x_1 and x_2, the tunneling probability is given by:

$$\begin{aligned} T_{\mathrm{tun}} &= \exp\left(-2\cdot\int_{x_1}^{x_2} \left|\sqrt{\frac{2m^*}{\hbar^2}\cdot\left(\left[-\frac{U(x_1)-E}{x_2-x_1}\cdot x+E\right]-E\right)}\right|\,\mathrm{d}x\right) \\ &= \exp\left(-\frac{4}{3}\cdot\sqrt{\frac{2m^*}{\hbar^2}\cdot\frac{U(x_1)-E}{x_1-x_2}}\cdot\left(x_2^{3/2}-x_1^{3/2}\right)\right). \end{aligned} \tag{3.31}$$

3.1.2 Landauer's Tunneling Formula

Landauer's tunneling formula [152] connects the quantum mechanical effect of carrier tunneling with the classical mechanics, i.e. the band structure and material. This approach allows for a calculation of the current in a system.

The basic idea of this approach is that carriers can only move from Region I to Region II and vice versa if there is an energy difference between the two regions. That means that there are empty states available in the opposite region. For the case that the Fermi energy of both regions are on the same level (Fig. 3.4(a)), no empty states are available and thus, no carriers are able to tunnel into the other region. In Fig. 3.4(b) the Fermi energy of Region II is lower than Region I , which in this case allows an electron to tunnel from Region I into an empty state in Region II .

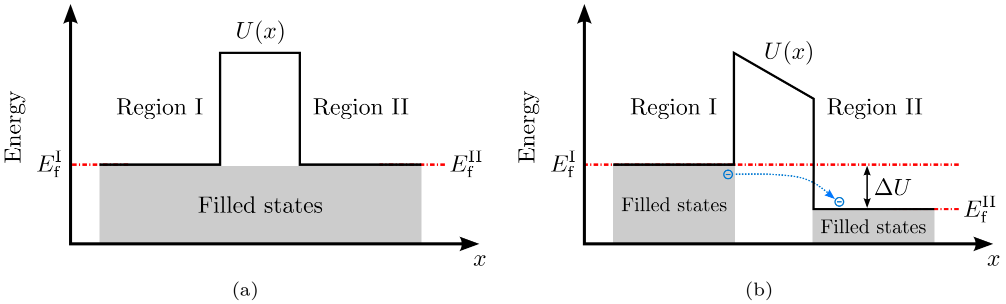

Figure 3.4.: Regions divided by an energy barrier $U(x)$. (a) Fermi energy of Region I and Region II are in equilibrium ($E_f^I = E_f^{II}$). In Region II there are no empty states to which e.g. an electron could tunnel. (b) Fermi energy difference between Region I and Region II ($E_f^I > E_f^{II}$), which opens the possibility for an electron to tunnel from Region I in an empty state of Region II [145].

In order to use Landauer's tunneling equation in compact models some necessary assumptions are made in the following derivation [153]:

- One constant effective mass m^* instead different masses corresponding to the band diagram.
- The dispersion relation in the semiconductor is approximated by parabolic bands:

$$E = \frac{\hbar^2 \cdot \vec{k}^2}{2m^*} = \frac{\hbar^2 \cdot (k_x^2 + k_y^2 + k_z^2)}{2m^*}, \tag{3.32}$$

  with the wave vector $\vec{k} = k_x\vec{e}_x + k_y\vec{e}_y + k_z\vec{e}_z$.

- Only transitions along the x-axis are considered, therefore the parallel wave vector $\vec{k}_\rho = k_y\vec{e}_y + k_z\vec{e}_z$ is not changed by the tunneling process.

The net tunneling current density from Region I to Region II is defined as the difference

between the current density flowing from Region I to Region II and vice versa [94, 153]:

$$J_{\text{tun}} = J_{\text{tun}}^{\text{I}\to\text{II}} - J_{\text{tun}}^{\text{II}\to\text{I}}. \tag{3.33}$$

The tunneling current density of the two regions depends on the vertical element of the wave vector k_x, the tunneling probability T_{tun}, the vertical carrier velocity v_x, the density of states $g_{\text{I/II}}$ as well as the Fermi-Dirac distribution $f_{\text{I/II}}$ in both regions. Now the changes in the current density are defined by:

$$\mathrm{d}J_{\text{tun}}^{\text{I}\to\text{II}} = q \cdot T_{\text{tun}}(k_x) \cdot v_x \cdot g_{\text{I}}(k_x) \cdot f_{\text{I}}(E) \cdot (1 - f_{\text{II}}(E))\,\mathrm{d}k_x \tag{3.34}$$

$$\mathrm{d}J_{\text{tun}}^{\text{II}\to\text{I}} = q \cdot T_{\text{tun}}(k_x) \cdot v_x \cdot g_{\text{II}}(k_x) \cdot f_{\text{II}}(E) \cdot (1 - f_{\text{I}}(E))\,\mathrm{d}k_x. \tag{3.35}$$

The density of states only depends on the x component of the wave vector which leads to:

$$g_{\text{I/II}}(k_x) = \int_0^\infty \int_0^\infty g(k_x,k_y,k_z)\,\mathrm{d}k_y\,\mathrm{d}k_z, \tag{3.36}$$

with the 3D density of states in momentum space $g(k_x,k_y,k_z)$. By considering the quantized wave vector components within a cube having a length of L:

$$\Delta k_x = \frac{2\pi}{L}, \quad \Delta k_y = \frac{2\pi}{L}, \quad \Delta k_z = \frac{2\pi}{L}, \tag{3.37}$$

the 3D density of states within a cube is given by:

$$g_{\text{I/II}}(k_x) = 2 \cdot \frac{1}{\Delta k_x \Delta k_y \Delta k_z} \cdot \frac{1}{L^3} = \frac{1}{4\pi^3}, \tag{3.38}$$

where the factor 2 is caused by the spin degeneracy. The velocity as well as the energy components in the direction of tunneling are obtained from Eq. (3.32):

$$v_x = \frac{1}{\hbar} \cdot \frac{\mathrm{d}E}{\mathrm{d}k_x} = \frac{\hbar \cdot k_x}{m^*}, \quad E_x = \frac{\hbar^2 \cdot k_x^2}{2 \cdot m^*}, \quad v_x\,\mathrm{d}k_x = \frac{1}{\hbar} \cdot \mathrm{d}E_x. \tag{3.39}$$

Now, Eq. (3.34) and (3.35) are written as:

$$\mathrm{d}J_{\text{tun}}^{\text{I}\to\text{II}} = \frac{q}{4\pi^3 \cdot \hbar} \cdot T_{\text{tun}}(E_x)\,\mathrm{d}E_x \cdot \int_0^\infty \int_0^\infty f_{\text{I}}(E) \cdot (1 - f_{\text{II}}(E))\,\mathrm{d}k_y\,\mathrm{d}k_z, \tag{3.40}$$

$$\mathrm{d}J_{\text{tun}}^{\text{II}\to\text{I}} = \frac{q}{4\pi^3 \cdot \hbar} \cdot T_{\text{tun}}(E_x)\,\mathrm{d}E_x \cdot \int_0^\infty \int_0^\infty f_{\text{II}}(E) \cdot (1 - f_{\text{I}}(E))\,\mathrm{d}k_y\,\mathrm{d}k_z. \tag{3.41}$$

By rewriting the parallel wave components in polar coordinates:

$$k_y = k_\rho \cdot \cos(\gamma), \quad k_z = k_\rho \cdot \sin(\gamma), \tag{3.42}$$

$$k_\rho = \sqrt{k_y^2 + k_z^2}, \quad \gamma = \arctan\left(\frac{k_z}{k_y}\right), \tag{3.43}$$

$$\mathrm{d}k_y\,\mathrm{d}k_z = k_\rho \cdot \mathrm{d}k_\rho\,\mathrm{d}\gamma \tag{3.44}$$

and splitting the total energy E into its longitudinal E_ρ and its transversal component E_x:

$$E_\rho = \frac{\hbar^2 \cdot (k_y^2 + k_z^2)}{2m^*} = \frac{\hbar^2 \cdot k_\rho^2}{2m^*}, \quad \mathrm{d}E_\rho = \frac{\hbar^2 \cdot k_\rho}{m^*} \cdot \mathrm{d}k_\rho, \quad E_x = \frac{\hbar^2 \cdot k_x^2}{2m^*}, \tag{3.45}$$

the current density $J_{\mathrm{tun}}^{\mathrm{I}\to\mathrm{II}}$ is written as:

$$\begin{aligned} J_{\mathrm{tun}}^{\mathrm{I}\to\mathrm{II}} &= \frac{q}{4\pi^3 \cdot \hbar} \cdot \int\limits_{E_x} T_{\mathrm{tun}}(E_x)\,\mathrm{d}E_x \cdot \int\limits_0^\infty \int\limits_0^{2\pi} f_{\mathrm{I}}(E) \cdot (1 - f_{\mathrm{II}}(E)) \cdot k_\rho \cdot \mathrm{d}\gamma\,\mathrm{d}k_\rho \\ &= \frac{q}{4\pi^3 \cdot \hbar} \cdot \int\limits_{E_x} T_{\mathrm{tun}}(E_x)\,\mathrm{d}E_x \cdot 2\pi \cdot \int\limits_0^\infty f_{\mathrm{I}}(E) \cdot (1 - f_{\mathrm{II}}(E)) \cdot k_\rho \cdot \frac{\mathrm{d}E_\rho}{\mathrm{d}E_\rho}\,\mathrm{d}k_\rho \\ J_{\mathrm{tun}}^{\mathrm{I}\to\mathrm{II}} &= \frac{q \cdot m^*}{2\pi^2 \cdot \hbar^3} \cdot \int\limits_{E_x} T_{\mathrm{tun}}(E_x)\,\mathrm{d}E_x \cdot \int\limits_0^\infty f_{\mathrm{I}}(E) \cdot (1 - f_{\mathrm{II}}(E))\,\mathrm{d}E_\rho. \end{aligned} \tag{3.46}$$

Similarly, for $J_{\mathrm{tun}}^{\mathrm{II}\to\mathrm{I}}$ follows:

$$J_{\mathrm{tun}}^{\mathrm{II}\to\mathrm{I}} = \frac{q \cdot m^*}{2\pi^2 \cdot \hbar^3} \cdot \int\limits_{E_x} T_{\mathrm{tun}}(E_x)\,\mathrm{d}E_x \cdot \int\limits_0^\infty f_{\mathrm{II}}(E) \cdot (1 - f_{\mathrm{I}}(E))\,\mathrm{d}E_\rho. \tag{3.47}$$

Evaluating Eq. (3.33) leads to the net tunneling current density:

$$\begin{aligned} J_{\mathrm{tun}}(E_x) &= \frac{q \cdot m^*}{2\pi^2 \cdot \hbar^3} \cdot \int\limits_{E_{\min}}^{E_{\max}} T_{\mathrm{tun}}(E_x)\,\mathrm{d}E_x \cdot \int\limits_0^\infty \big(f_{\mathrm{I}}(E) - f_{\mathrm{II}}(E)\big)\,\mathrm{d}E_\rho \\ J_{\mathrm{tun}}(E_x) &= \frac{q \cdot m^*}{2\pi^2 \cdot \hbar^3} \cdot \int\limits_{E_{\min}}^{E_{\max}} T_{\mathrm{tun}}(E_x) \cdot \mathcal{N}(E_x)\,\mathrm{d}E_x, \end{aligned} \tag{3.48}$$

where $\mathcal{N}(E_x)$ is the supply function depending on E_x and for this reason it is written inside the integral over E_x. The supply function using the Fermi-Dirac distribution is defined by [153]:

$$\mathcal{N}(E_x) = \int\limits_0^\infty \big(f_{\mathrm{I}}(E) - f_{\mathrm{II}}(E)\big)\,\mathrm{d}E_\rho = k_{\mathrm{b}}T \cdot \ln\left(\frac{1 + \exp\left(-\frac{E_x - E_{\mathrm{f}}^{\mathrm{I}}}{k_{\mathrm{b}}T}\right)}{1 + \exp\left(-\frac{E_x - E_{\mathrm{f}}^{\mathrm{II}}}{k_{\mathrm{b}}T}\right)}\right). \tag{3.49}$$

The values for E_{min} and E_{max} as well as the Fermi-Dirac distribution depend on the considered tunneling process:

- In case of electron tunneling E_{min} is defined by the lowest conduction band (ConB) energy in Region II $E_{\mathrm{c}}^{\mathrm{II}}|_{\mathrm{min}}$ and the highest valence band (ValB) edge in Region I $E_{\mathrm{v}}^{\mathrm{I}}|_{\mathrm{max}}$. The Fermi-Dirac distribution is calculated for electrons.
- On the other hand, for hole tunneling the energy integration limits are defined as for electrons, whereby the sign of the integration is changed. Furthermore, the Fermi-Dirac distribution is calculated for hole carriers.

3.1.3 Tunneling Events

Regarding the tunneling effect, a distinction between two types of tunneling is made. The first one is the so-called single-band (SB) tunneling and the second one is the band-to-band (B2B) tunneling.

SB tunneling occurs for example at a Schottky barrier or a Silicon-Insulator-Silicon structure as it is shown in Fig. 3.5(a). In the SB tunneling process there are three different types of tunneling: Fowler-Nordheim (F-N) tunneling [32], direct tunneling [32] and trap-assisted tunneling (TAT) [154].

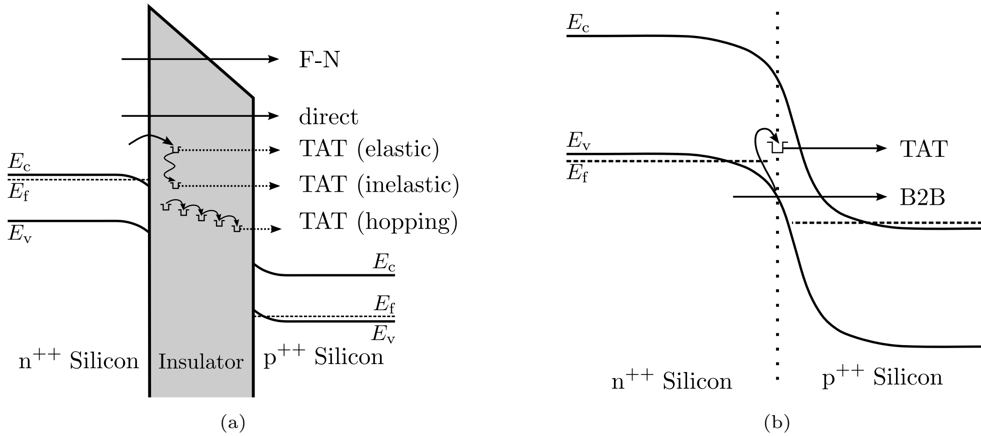

Figure 3.5.: (a) Tunneling events in a Silicon-Insulator-Silicon structure [153]. (b) Tunneling processes at a n^{++}/p^{++} - Silicon junction, which characterize the current transport in TFETs.

The F-N tunneling is defined by the carrier tunneling through a triangular shaped energy barrier, whereby the carrier tunnels only through a part of the insulator layer. The triangular part of the barrier in Fig. 3.5(a) is mainly affected by the electric field and less by the thickness of the insulator layer. The insulator thickness only indirectly affects the tunneling process by influencing the electric field. F-N tunneling can occur in thick insulator layers, i.e. $> 5\,\mathrm{nm}$ [32]. The tunneling probability in this case is calculated with the help of the WKB approximation.

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The phenomenon of direct tunneling comes into play for insulator thicknesses $\leq 5\,\mathrm{nm}$. Even for low electric fields, carriers are able to tunnel directly through the insulator [32]. In addition to direct tunneling, the effect of TAT occurs in this kind of structure. Traps are defined as defects within the band gap of the material, which are caused by the fabrication process or repeated voltage stress [153]. TAT can be separated into three different types: the elastic TAT event, where a carrier tunnels to a trap within the insulator at the same energy and then has the chance to tunnel through the insulator without losing energy. Second, the carrier occupies a trap, loses energy by phonons emission and then tunnels through the insulator. This is known as inelastic TAT. The third one happens in an insulator with a high defect or trap density. In this case carriers are able to hop from trap to trap and subsequently tunnel through the insulator [153].

In case of a n^{++}/p^{++} - Silicon junction the tunneling process is caused by carriers that tunnel from either the ValB to the ConB or vice versa. The tunneling event is called B2B tunneling if a carrier tunnels directly from one band to the other. This effect describes the main current transport mechanism in a TFET device. The B2B tunneling current is influenced by the band gap and the effective carrier mass of the chosen device material as well as by the externally applied bias. For instance, if the bias at the p^{++} side increases the resulting tunneling distance decreases which causes an increase of the B2B tunneling current. Beside the advantageous B2B tunneling current, in highly doped junctions the TAT effect has to be taken into account. Since in highly doped junctions the depletion layer thickness is very small, the tunneling distance is also very small and thus the tunneling probability in the OFF-state increases to non negligible values [154, 155]. The TAT current determines the OFF current of a TFET and as a consequence directly influences the resulting subthreshold slope [50].

3.2 Device Geometry

In the following the TFET device geometry is introduced which is under investigation in the entire thesis. Figure 3.6 illustrates the 3D DG TFET device, whereby a distinction is made between the n-type TFET (see Fig. 3.6(a)) and the p-type device (see Fig. 3.6(b)). The source, channel and drain region are out of Silicon, except it is mentioned. The device can also be built up by hetero-junction materials to enhance the device performance. The insulator is chosen to be a high-κ material (HfO_2 or Ta_2O_5) in order to improve the electrostatic control of the channel region. The gate contact is made of metal.

Regarding the n-type device, the source region is highly p-doped, the channel stays intrinsic and the drain region is highly n-doped. In general, the n-type TFET is a gated p-i-n diode. In case of the p-type device, the source is highly n-doped and the drain is highly p-doped, so the p-type TFET is a gated n-i-p diode.

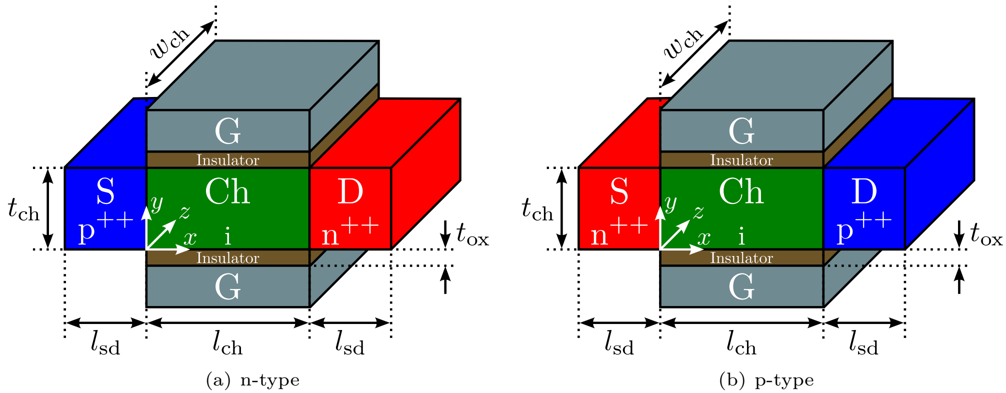


Figure 3.6.: 3D Schematic of (a) an n-type and (b) a p-type DG TFET structure. The structural parameters are defined as follows: l_{ch} – channel length, t_{ch} – channel thickness, w_{ch} – channel width, t_{ox} – gate insulator (oxide) thickness, l_{sd} – length of source (S)/drain (D) region.

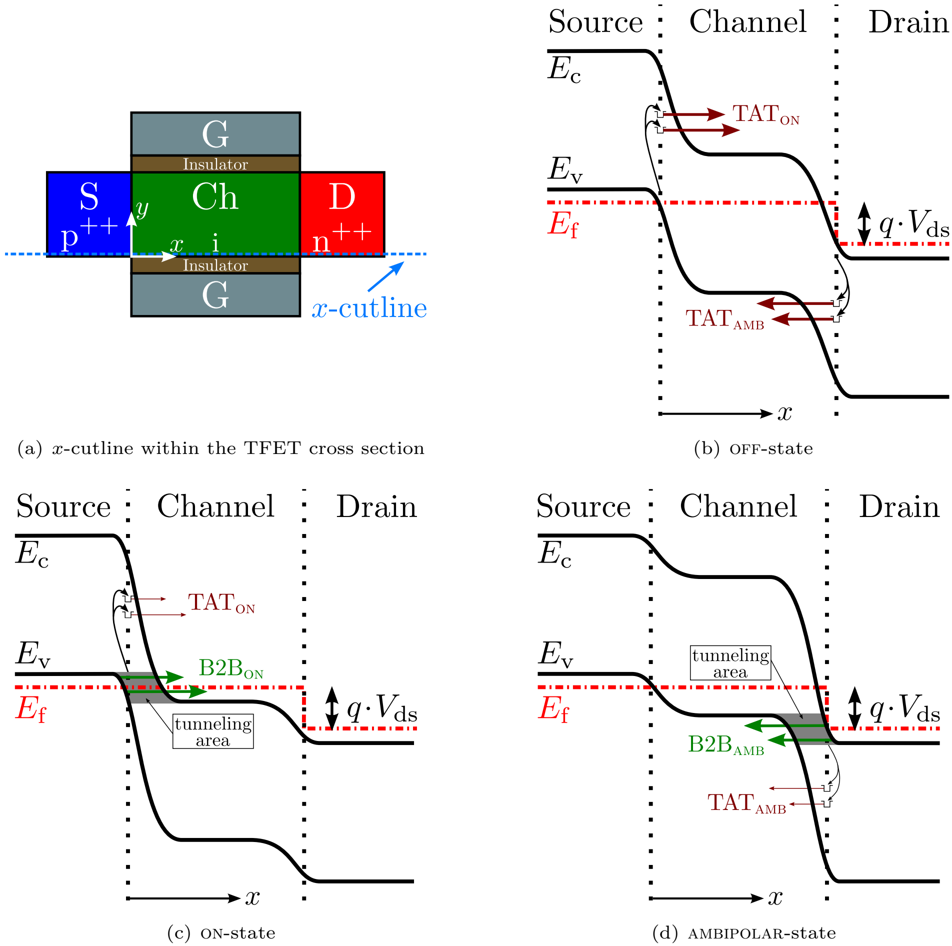
In literature various kinds of TFET geometries can be found, e.g. gate-all-around or nanowires, which are all 3D multiple-gate devices. Using multiple gate structures enhances the performance of TFETs. The DG structure represents a good candidate, in order to find a reasonable trade-off between the complexity of the device and the mathematical practicability.

3.3 Working Principle

The basic working principle of an n-type TFET is detailed in the following. Except for the different polarity of the charge carriers, p-type and n-type TFETs work in the same way.

Regarding the TFET and its structure, there are three different operation states. These states are called the OFF-, the ON- and the AMBIPOLAR-state. These three states are successively introduced with the help of the band diagram along the x-axis within the TFET cross section (see Fig. 3.7(a)). The selected x-cutline is directly below the gate insulator, since at this position the gates have the biggest electrostatic influence on the channel region. For this reason, the current has its highest density at this y-position. Furthermore, the applied gate bias determines the state of the TFET, whereby these distinctions are explained in the next three subsections.

Subsequently, the effect of the channel potential pinning and the influence of the drain voltage V_{ds} on the device behavior are investigated. The typical unidirectionality of the TFET current and its effect on the current characteristics is also discussed at the end of this section.



(a) x-cutline within the TFET cross section (b) OFF-state (c) ON-state (d) AMBIPOLAR-state

Figure 3.7.: (a) Cross section of the 3D n-type TFET geometry to illustrate the TFET working principle using the cutline along the x-axis. (b) OFF-state of the TFET, only TAT current occurs at the channel junctions. In (c) the ON-state and (d) the AMBIPOLAR-state B2B tunneling occurs at the source-to-channel and the drain-to-channel junction, respectively. In these cases, the B2B tunneling current dominates, but the TAT current is still present. Dark red arrows: TAT. Green arrows: B2B.

3.3.1 OFF-State

Considering the schematic band diagram illustrated in Fig. 3.7(b), the TFET is in the OFF-state when all of the following conditions are fulfilled:

1. A positive drain-source voltage $V_{ds} > 0\,\text{V}$ is applied,
2. the ConB in channel, determined by the applied gate bias V_{gs}, and the ValB in source do not overlap and

3. the ConB in drain does not overlap the ValB in the channel region.

In this case, there are no empty states within the channel region available that would allow for B2B tunneling.

On the other hand, carriers are able to hop into an empty trap at the channel junctions by thermionic emission and from there tunnel to an empty state within the channel. So, the OFF-state current is determined by the TAT current, whereby the TAT current is a compound of TAT_{ON}, occurring at the source-to-channel junction and TAT_{AMB} appearing at the drain-to-channel junction. The current part TAT_{ON} occurring at the source-to-channel junction for a higher V_{gs} is determined electrons. By reducing the gate bias, the TAT_{ON} decreases and goes over into a hole based current TAT_{AMB} at the drain-to-channel junction.

The OFF-state current has a direct influence on the resulting subthreshold slope. That means, the more defects or midgap traps are located at the channel junctions, the higher the TAT current is and therefore the subthreshold slope worsens.

3.3.2 ON-State

Figure 3.7(c) depicts the ON-state of the TFET. The applied drain-source voltage is positive $V_{ds} > 0\,V$. From a certain gate bias when the ConB in the channel starts to overlap the ValB in source ($E_c^{ch} < E_v^{s}$), the TFET is in the ON-state. With regards to Landauer's tunneling formula (see Sec. 3.1.2), empty states are available in the channel and electrons are able to tunnel directly from source into the channel. The higher V_{gs}, the larger the tunneling area becomes, simultaneously the tunneling distance decreases and thus, the amount of the ON-state B2B tunneling current $B2B_{ON}$ increases. The tunneling area is defined by the ValB edge in source and the ConB edge in the channel.

The TAT current that characterizes the OFF-state current is still present in the ON-state. For an increasing V_{gs}, the TAT_{ON} part becomes several orders of magnitude smaller than the B2B part and thus does not significantly influence the resulting tunneling current. The TAT current at the drain-to-channel junction TAT_{AMB} decreases for an increasing V_{gs} and therefore is negligible.

3.3.3 AMBIPOLAR-State

The TFET is in the AMBIPOLAR-state when the applied drain-source voltage is greater than zero ($V_{ds} > 0\,V$) and the ValB in the channel region starts to overlap the ConB edge in the drain region. A schematic band diagram showing the AMBIPOLAR-state is given in Fig. 3.7(d). The AMBIPOLAR-state takes place when the gate bias V_{gs} is decreased to small or rather to negative values. In this operation regime, hole tunneling occurs at the drain-to-channel junction. For this reason, $B2B_{amb}$ is a hole based tunneling current part. By further reduction in V_{gs}, the tunneling area is increased, the tunneling distance is reduced and hence, the $B2B_{amb}$ current part is also increased.

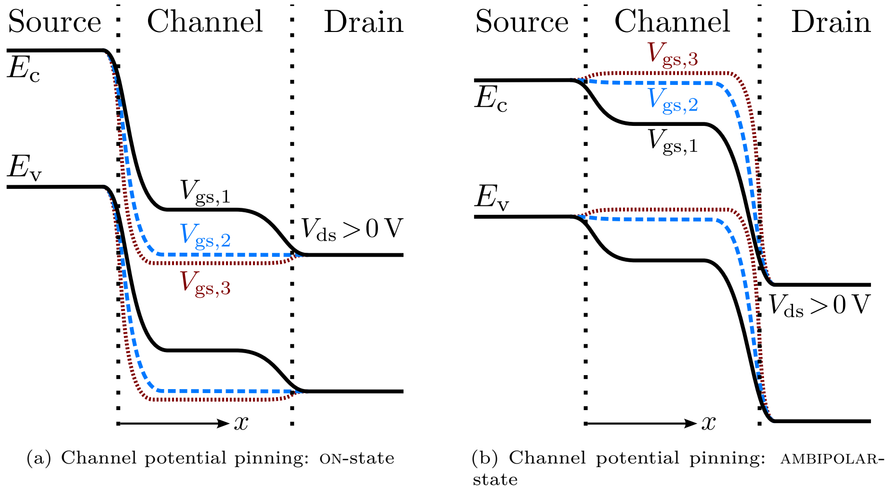
The TAT current part $\mathrm{TAT}_{\mathrm{AMB}}$ also occurs in the AMBIPOLAR-state. For reduced or negative V_{gs} values it is still possible, that a hole can hop on an empty trap and tunnel from the junction into the channel. But $\mathrm{TAT}_{\mathrm{AMB}}$ has a minor impact on the total tunneling current as it is mentioned in the previous subsection.

3.3.4 Channel Potential Pinning

The channel potential pinning in the ON-state of the TFET takes place when the gate bias V_{gs} is increased above the applied drain-source voltage ($V_{\mathrm{gs}} > V_{\mathrm{ds}}$). For that case, an electron inversion charge layer begins to form within the channel region that effectively shortens the channel length. Hence, the channel potential saturates approximately to the applied V_{ds} or in other words, the channel potential is "pinned" to the drain-source voltage [145].

Figure 3.8(a) illustrates this effect for three various gate-source voltages, where $V_{\mathrm{gs},1} < V_{\mathrm{ds}} < V_{\mathrm{gs},2} < V_{\mathrm{gs},3}$. In the first case, $V_{\mathrm{gs},1}$ is smaller than V_{ds} and for this reason, the channel potential follows V_{gs} so it is not pinned. Here, the depletion region at the drain-to-channel-junction allows a steeper tunneling current. In the second case, it can be seen that the channel potential pinning approximately starts from the point ($V_{\mathrm{gs},2} \approx V_{\mathrm{ds}}$). In the third case the gate bias $V_{\mathrm{gs},3}$ is greater than V_{ds} and the channel potential does not follow V_{gs} any more. It is pinned due to the inversion charge layer. In general, the channel potential increases only slightly for an increasing V_{gs} and thus the tunneling current. Nevertheless, the tunneling current still increases for higher V_{gs} due to the steeper gradient and therefore a smaller tunneling distance at the source-to-channel junction. As it can be seen in Fig. 3.9(b), the slope of the current transfer curve worsens in the ON-state when the channel potential pinning ($V_{\mathrm{gs}} > V_{\mathrm{ds}}$) comes into play and the depletion region at the drain-to-channel junction disappears.

The effect of the channel potential pinning also occurs in the AMBIPOLAR-state as it is depicted in Fig. 3.8(b). By decreasing V_{gs} to small or negative values, the channel potential is pinned to the voltage in source region V_{s} in the same way that is mentioned in the previous paragraph. Figure 3.8(b) presents a schematic band diagram for three gate biases, where $V_{\mathrm{gs},1} > V_{\mathrm{s}} > V_{\mathrm{gs},2} > V_{\mathrm{gs},3}$. In the first case, the channel potential follows $V_{\mathrm{gs},1}$, where the depletion region at the source-to-channel junction leads to a steep tunneling current. In the second scenario ($V_{\mathrm{gs},2} \approx V_{\mathrm{s}}$), the potential in the channel starts to be pinned to the source voltage. Lastly, the channel potential loses its control by V_{gs} when $V_{\mathrm{gs},3}$ falls below V_{s} and thus, the tunneling current only rises by the increasing potential gradient and the subsequent decrease of the tunneling distance at the drain-to-channel junction. The current transfer curve slope also decreases in the AMBIPOLAR-state if the gate-source voltage falls below the source potential (see Fig. 3.9(b)). At the source-to-channel junction, the depletion region has disappeared, which causes a nearly constant voltage and thus a negligible resistance and also a worsening of the current gradient.



(a) Channel potential pinning: ON-state

(b) Channel potential pinning: AMBIPOLAR-state

Figure 3.8.: Schematic band diagram to point out the effect of the channel potential pinning caused by inversion charges in (a) the ON-state and (b) the AMBIPOLAR-state of the TFET. ON-state: $V_{gs,1} < V_{ds} < V_{gs,2} < V_{gs,3}$. AMBIPOLAR-state: $V_{gs,1} > V_s > V_{gs,2} > V_{gs,3}$.

3.3.5 Drain-Source Voltage Influence

A variation of the drain-source voltage effectively influences the behavior of the TFET device. In the ON-state of the TFET, two different cases can occur for a V_{ds} variation. In the first case when $V_{ds,1} > V_{gs}$, as shown in Fig. 3.9(a), the channel potential pinning does not take place and therefore the existing depletion region at the drain-to-channel junction allows for a nearly unrestricted electron current flow. So, a high V_{ds} value offers a wide V_{gs} range with no channel potential pinning and therefore a steeper tunneling current. This case can be seen in the current transfer curve in Fig. 3.9(b). In the second case when $V_{ds,3} < V_{ds,2} < V_{gs}$ (see Fig. 3.9(a)), the channel potential pinning occurs and reduces the gradient of the tunneling current. The effect can be seen better in the current transfer curve (see Fig. 3.9(b)). In case of channel potential pinning in the ON-state, a smaller V_{ds} causes a degradation of the tunneling current slope. On the other hand if $V_{ds} > V_{gs}$, no channel potential pinning occurs and hence, the resulting subthreshold slope of the tunneling current, occurring at the source-to-channel junction, is nearly not affected by V_{ds}.

The influence of a drain voltage variation can be seen better in the AMBIPOLAR-state. Here, the tunneling process is located at the drain-to-channel junction. An increase of V_{ds} causes a downshift of the energy bands in the drain region, thus, the resulting tunneling area is increased, the tunneling distance is decreased and the tunneling current increases. The influence can be seen well in the current transfer curve as it is shown in Fig. 3.9(b). By applying a higher drain voltage $\mathrm{V}_{ds,1}$, the AMBIPOLAR-state current in the transfer curve shifts along the V_{gs}-axis in the direction of the ON-state. In case of a smaller $V_{ds} = V_{ds,3}$, the AMBIPOLAR tunneling

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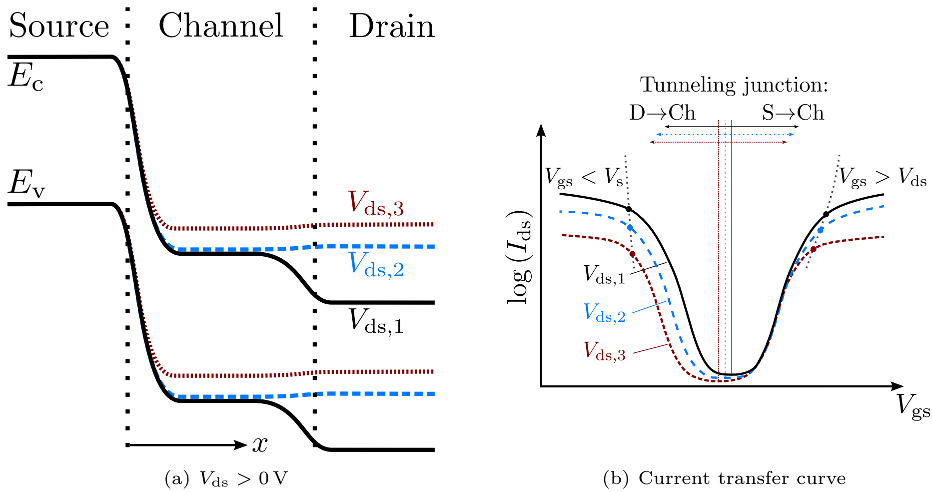


(a) $V_{ds} > 0\,\mathrm{V}$ (b) Current transfer curve

Figure 3.9.: Illustration of a drain voltage variation on the device behavior in (a) the band diagram and (b) the current transfer curve, showing I_{ds} in logarithmic scale. In both plots: $V_{ds} > 0\,\mathrm{V}$ and $V_{ds,1} > V_{ds,2} > V_{ds,3}$. (b) Gray dashed lines: transition to channel potential pinning.

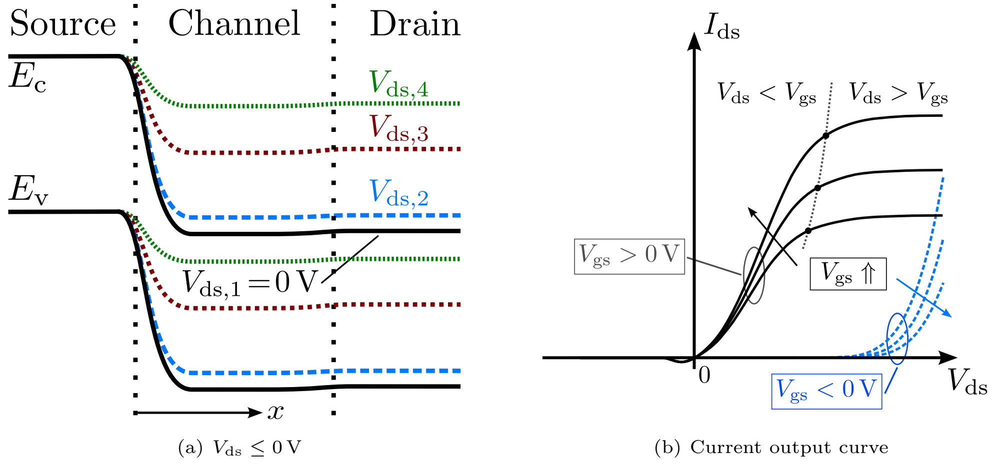
current part is shifted leftwards along the V_{gs}-axis and the AMBIPOLAR behavior is reduced. The resulting subthreshold slope is not affected by a change in V_{ds}, since channel potential pinning is not yet taking place.

3.3.6 Unidirectional Behavior of the Current

Beside the drain-induced shift of the AMBIPOLAR-state tunneling current, there is another phenomenon occurring in TFETs. It is the unidirectional current behavior. This effect appears by applying negative drain voltages, whereby the considered gate-source voltage V_{gs} is not relevant.

In order to explain the unidirectional behavior, Fig. 3.10(a) illustrates the band diagram for various V_{ds}. It can be seen that at $V_{ds,1} = 0\,\mathrm{V}$ the bands at the source-to-channel junction have an overlap but due to Landauer's tunneling formula the resulting tunneling current equals zero. By reducing V_{ds} to a small negative value $V_{ds,2}$, the channel potential is also shifted upwards due to the potential pinning and the band overlap still causes a small negative tunneling current. This negative current only appears in a small V_{ds} range and decreases quickly to zero. By further reduction of V_{ds} to $V_{ds,3}$ the band overlap disappears and thus the tunneling current turns to zero, which can be seen in the current output curve in Fig. 3.10(b). But in case of $V_{ds,4}$ the energy barrier between source and drain is reduced so much, that a negative thermionic emission based current can flow. So the TFET turns into a parasitic p/n diode, which has to taken into account in the design of logic circuits [156, 157]. The unidirectionality of the device is also characterized by the AMBIPOLAR-state current in the output curve (see Fig. 3.10(b)). For

negative V_{gs} and an increasing V_{ds} the current increases exponentially with the same polarity as the ON-state current.



(a) $V_{ds} \leq 0\,V$

(b) Current output curve

Figure 3.10.: Visualization of the effect of the current unidirectionality in (a) the band diagram ($V_{ds,1} = 0\,V > V_{ds,2} > V_{ds,3} > V_{ds,3}$) and (b) the current output curve. (b) Black solid lines: ON-state, $V_{gs} > 0\,V$. Blue dashed lines: AMBIPOLAR-state, $V_{gs} < 0\,V$.

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CHAPTER 4

2D Electrostatic Potential Solution

In this chapter, a closed-form 2D analytical electrostatic potential solution for the DG TFET is derived. The potential solution forms the basis of the band diagram calculation, and since the tunneling probability is calculated as a function of the band diagram, an accurate electrostatic solution is essential to properly calculating the tunneling current of a DG TFET. In order to solve the device electrostatics in the channel region, some preliminary considerations are made in Sec. 4.1, from which 2D potential solution is derived in Sec. 4.2. The verification of the derived potential model is done in Sec. 4.3, where the modeling results are compared with TCAD Sentaurus simulation data.

4.1 Preliminary Modeling Considerations

Before the closed-form 2D electrostatic potential solution is derived some preliminaries are considered to keep mathematics as simple as possible and to obtain a stable potential model. Firstly, the Laplace equation is introduced in Sec. 4.1.1. The influence of inversion charges on the electrostatics is detailed in Sec. 4.1.2, followed by the scaling of the gate insulator in Sec. 4.1.3. The decomposition and the boundary conditions of the DG device are explained in Sec. 4.1.4, where the conformal mapping of the device structure is derived in Sec. 4.1.5.

4.1.1 Laplace's Equation

Solving an electrostatic potential problem in general needs for a solution of Poisson's equation as it is shown in Eq. (2.3). Finding a closed-form solution of Poisson's equation is very challenging and a numerical solution is not suitable for a usage in compact models. Due to the intrinsic channel of the DG TFET the neglect of inversion charges is acceptable. Then, the Poisson equation reduces to Laplace's equation:

$$\mathit{\Delta\Phi}(x,y) = -\frac{\varrho(x,y)}{\varepsilon_{\mathrm{ch}}} \quad \rightarrow \quad \mathit{\Delta\Phi}(x,y) \approxeq 0. \tag{4.1}$$

Since neglecting inversion charges in the electrostatics is only valid in the OFF-state of the TFET, a modeling approach to consider inversion charges in the ON- and AMBIPOLAR-state is introduced in Sec. 4.1.2

4.1.2 Inversion Charges

The consideration of inversion charges and their influence on the device electrostatics is a very important issue. As it was mentioned in Sec. 3.3.4 and 3.3.5, the channel potential is pinned to the applied drain-source voltage V_{ds} or the applied gate-source voltage V_{gs}. The channel potential pinning effect has a direct impact on the resulting tunneling current.

In order to capture the effect of inversion charges on the device behavior, a 1D surface potential model for planar TFETs is introduced in the following, which has been reported in [158]. This 1D potential at the surface of the channel is analytically solved, but it is not sufficient for an adaption in the 2D electrostatic solution of a DG TFET. For this reason, a DG TFET surface potential denoted as $V_{\mathrm{gs,eff}}$ in the following and including 2D effects is derived based on the 1D potential solution in the surface and the center of the TFET.

1D Surface Potential Solution

The 1D surface potential to screen the gate modulation can be calculated by [158]:

$$\Phi_1 = \frac{k_{\mathrm{b}}T}{q} \cdot \ln\left(\frac{N_{\mathrm{ch}} \cdot N_{\mathrm{inv}}}{n_{\mathrm{i}}^2}\right), \tag{4.2}$$

with the intrinsic electron concentration in Silicon n_{i}, the channel doping concentration N_{ch} and N_{inv} is the inversion charge density which is empirically set to $1.6 \cdot 10^{18}\mathrm{cm}^{-3}$.

In the case when the 1D surface potential is in the V_{gs}-control regime which is qualitatively shown in Fig. 4.1(a), the influence of inversion charges and the drain voltage are negligible and $\varphi_{\mathrm{s}}^{\mathrm{1D}}$ in depletion region reads as:

$$\varphi_{\mathrm{s,dep}}^{\mathrm{1D}} = \left(\sqrt{V_{\mathrm{gs}} - V_{\mathrm{fb}} + \frac{\gamma^2}{4}} - \frac{\gamma}{2}\right)^2, \tag{4.3}$$

where V_{fb} is the flat band voltage and the term γ characterizes the body factor and is calculated by:

$$\gamma = \frac{\sqrt{2 \cdot \varepsilon_{\mathrm{ch}} \cdot q \cdot N_{\mathrm{ch}}}}{C'_{\mathrm{ox}}}, \tag{4.4}$$

with the gate oxide capacitance per gate area $C'_{\mathrm{ox}} = \varepsilon_{\mathrm{ox}}/t_{\mathrm{ox}}$.

Inversion charges come into play when V_{gs} reaches or overcomes the applied drain-source voltage V_{ds}, as can be seen qualitatively in Fig. 4.1(b) denoted as V_{ds}-control. In this case, the

1D surface potential is calculated in dependency of V_{gs} and V_{ds} as follows [158]:

$$\varphi_{\mathrm{s,inv}}^{\mathrm{1D}} = (V_{\mathrm{ds}} + \Phi_1) + \frac{k_{\mathrm{b}}T}{q} \cdot \ln\left\{ \frac{q}{k_{\mathrm{b}}T} \cdot \left[\frac{k_{\mathrm{b}}T}{q} + \frac{\sqrt{V_{\mathrm{ds}} + \Phi_1}}{\sqrt{V_{\mathrm{ds}} + \Phi_1} + \gamma} \cdot (V_{\mathrm{gs}} - V_{\mathrm{fb}} - V_{\mathrm{ds}} - \Phi_1) + \frac{1}{2} \cdot \left(\frac{V_{\mathrm{ds}} + \Phi_1}{(\sqrt{V_{\mathrm{ds}} + \Phi_1} + \gamma)^2} - \frac{\gamma \cdot (V_{\mathrm{ds}} + \Phi_1 - 2)}{2 \cdot (\sqrt{V_{\mathrm{ds}} + \Phi_1} + \gamma)^3} \right) \cdot (V_{\mathrm{gs}} - V_{\mathrm{fb}} - V_{\mathrm{ds}} - \Phi_1)^2 \right] \right\}. \tag{4.5}$$

In order to find a closed-form expression for the 1D surface potential, a continuous function has to be found which connects the depletion with the inversion regime. The following function changes smoothly from $\varphi_{\mathrm{s,dep}}^{\mathrm{1D}}$ to the transition point $V_{\mathrm{ds}} + \Phi_1$:

$$F_{\varphi_{\mathrm{s}}} = \frac{1}{2} \cdot \left(V_{\mathrm{ds}} + \Phi_1 + \varphi_{\mathrm{s,dep}}^{\mathrm{1D}} - \sqrt{(\varphi_{\mathrm{s,dep}}^{\mathrm{1D}} - V_{\mathrm{ds}} - \Phi_1)^2 + \delta^2} \right), \tag{4.6}$$

where δ is a constant term for a smooth transition. With the help of this connection function, the surface potential is calculated by:

$$\varphi_{\mathrm{s}}^{\mathrm{1D}}(V_{\mathrm{gs}}, V_{\mathrm{ds}}) = F_{\varphi_{\mathrm{s}}} + \frac{k_{\mathrm{b}}T}{q} \cdot \ln\left\{ \frac{q}{k_{\mathrm{b}}T} \cdot \left[\frac{k_{\mathrm{b}}T}{q} + \frac{\sqrt{F_{\varphi_{\mathrm{s}}}}}{\sqrt{F_{\varphi_{\mathrm{s}}}} + \gamma} \cdot (V_{\mathrm{gs}} - V_{\mathrm{fb}} - F_{\varphi_{\mathrm{s}}}) + \frac{1}{2} \cdot \left(\frac{F_{\varphi_{\mathrm{s}}}}{(\sqrt{F_{\varphi_{\mathrm{s}}}} + \gamma)^2} - \frac{\gamma \cdot (F_{\varphi_{\mathrm{s}}} - 2)}{2 \cdot (\sqrt{F_{\varphi_{\mathrm{s}}}} + \gamma)^3} \right) \cdot (V_{\mathrm{gs}} - V_{\mathrm{fb}} - F_{\varphi_{\mathrm{s}}})^2 \right] \right\}. \tag{4.7}$$

1D Center Potential Solution

The 1D potential in the center of the TFET can be adapted from the center potential of DG MOSFET with an undoped body. The 1D center potential follows approximately the applied gate-source voltage V_{gs} and saturates to a constant value when the effect of inversion charges come into play. The constant saturation voltage is dependent from the applied drain-voltage V_{ds} and is defined by [159]:

$$\varphi_{\mathrm{c,sat}}(V_{\mathrm{ds}}) = \frac{k_{\mathrm{b}}T}{q} \cdot \ln\left(\frac{2\pi^2 \cdot \varepsilon_{\mathrm{ch}} \cdot k_{\mathrm{b}}T}{q^2 \cdot N_{\mathrm{ch}} \cdot t_{\mathrm{ch}}^2} \right) + V_{\mathrm{ds}}. \tag{4.8}$$

The smoothing function presented in [160] is used for a continuous transition of the linear V_{gs} dependency and the constant saturation voltage $\varphi_{\mathrm{c,sat}}$ of the 1D center potential. It follows:

$$\varphi_{\mathrm{c}}^{\mathrm{1D}}(V_{\mathrm{gs}}, V_{\mathrm{ds}}) = \varphi_{\mathrm{c,sat}} \cdot \left[1 - \frac{1}{\ln(1 + \exp(15))} \cdot \ln\left(1 + \exp\left(15 \cdot \left(1 - \frac{V_{\mathrm{gs}} - V_{\mathrm{fb}}}{\varphi_{\mathrm{c,sat}}} \right) \right) \right) \right]. \tag{4.9}$$

Surface Potential Including 2D Effects

The DG TFET surface potential including 2D effects is derived hereinafter and is named as the effective gate voltage $V_{\mathrm{gs,eff}}$ in the following. It should be noted that the consideration of 2D effects means to take into account the potential change along the y-axis. The TFET surface potential is obtained by solving the 1D Poisson equation in y-direction at $x = {}^{l_{\mathrm{ch}}}/_{2}$ with Fermi-Dirac statistics as follows [109]:

$$\frac{\mathrm{d}^2 u}{\mathrm{d}y^2} = \left(\frac{1}{2} \cdot \frac{2q^2 \cdot n_{\mathrm{i}}}{\varepsilon_{\mathrm{ch}} \cdot k_{\mathrm{b}}T}\right) \cdot \frac{\mathcal{F}_{1/2}\left(u - v_{\mathrm{ch}} - \frac{E_{\mathrm{g}}^{\mathrm{ch}}}{2 \cdot k_{\mathrm{b}}T}\right)}{\mathcal{F}_{1/2}\left(-\frac{E_{\mathrm{g}}^{\mathrm{ch}}}{2 \cdot k_{\mathrm{b}}T}\right)}, \tag{4.10}$$

whereby $\mathcal{F}_{1/2}$ is the Fermi-Dirac integral[1] of order 1/2, u is the normalized potential by ${}^{k_{\mathrm{b}}T}/_{q}$, v_{ch} is the normalized quasi-Fermi potential and $E_{\mathrm{g}}^{\mathrm{ch}}$ is the band gap of the channel material. An integration of Eq. (4.10) results in the vertical electric field at the surface as follows:

$$\left.\frac{\mathrm{d}u}{\mathrm{d}y}\right|_{y=0} = \sqrt{\frac{2q^2 \cdot n_{\mathrm{i}}}{\varepsilon_{\mathrm{ch}} \cdot k_{\mathrm{b}}T}} \cdot \sqrt{\frac{2}{3} \cdot \frac{\left.\mathcal{F}_{3/2}\left(u - \frac{E_{\mathrm{g}}^{\mathrm{ch}}}{2 \cdot k_{\mathrm{b}}T}\right)\right|_{u_{\mathrm{c}}}^{u_{\mathrm{s}}}}{\mathcal{F}_{1/2}\left(-\frac{E_{\mathrm{g}}^{\mathrm{ch}}}{2 \cdot k_{\mathrm{b}}T}\right)}}, \tag{4.11}$$

with the Fermi-Dirac integral $\mathcal{F}_{3/2}$ of order 3/2. The normalized surface potential u_{s} and the normalized center potential u_{c} are calculated by applying Eq. (4.7) and (4.9) as follows:

$$u_{\mathrm{s}} = \varphi_{\mathrm{s}}^{\mathrm{1D}} \cdot \frac{q}{k_{\mathrm{b}}T}, \tag{4.12}$$

$$u_{\mathrm{c}} = \varphi_{\mathrm{c}}^{\mathrm{1D}} \cdot \frac{q}{k_{\mathrm{b}}T}. \tag{4.13}$$

The normalized surface potential u_{s} in dependency of the applied V_{gs} can also be expressed by the following expression [109]:

$$(V_{\mathrm{gs}} - V_{\mathrm{fb}}) \cdot \frac{q}{k_{\mathrm{b}}T} - u_{\mathrm{s}} = \frac{\varepsilon_{\mathrm{ch}}}{C'_{\mathrm{ox}}} \cdot \left.\frac{\mathrm{d}u}{\mathrm{d}y}\right|_{y=0}. \tag{4.14}$$

Since this equation has no closed form solution, a first order Newton correction is performed to improve accuracy. The function for the Newton method reads as:

$$f(u_{\mathrm{s}}) = (V_{\mathrm{gs}} - V_{\mathrm{fb}}) \cdot \frac{q}{k_{\mathrm{b}}T} - u_{\mathrm{s}} - \frac{\varepsilon_{\mathrm{ch}}}{C'_{\mathrm{ox}}} \cdot \sqrt{\frac{2q^2 \cdot n_{\mathrm{i}}}{\varepsilon_{\mathrm{ch}} \cdot k_{\mathrm{b}}T}} \cdot \sqrt{\frac{2}{3} \cdot \frac{\mathcal{F}_{3/2}\left(u_{\mathrm{s}} - \frac{E_{\mathrm{g}}^{\mathrm{ch}}}{2 \cdot k_{\mathrm{b}}T}\right) - \mathcal{F}_{3/2}\left(u_{\mathrm{c}} - \frac{E_{\mathrm{g}}^{\mathrm{ch}}}{2 \cdot k_{\mathrm{b}}T}\right)}{\mathcal{F}_{1/2}\left(-\frac{E_{\mathrm{g}}^{\mathrm{ch}}}{2 \cdot k_{\mathrm{b}}T}\right)}} \tag{4.15}$$

1 A Verilog-A suitable approximation of the Fermi-Dirac integral is presented in App. B.1

and for the derivative follows:

$$f'(u_\mathrm{s}) = -1 - \frac{\varepsilon_\mathrm{ch}}{C'_\mathrm{ox}} \cdot \sqrt{\frac{2q^2 \cdot n_\mathrm{i}}{\varepsilon_\mathrm{ch} \cdot k_\mathrm{b}T}} \cdot \sqrt{\frac{2}{3 \cdot \mathcal{F}_{1/2}\left(-\frac{E_\mathrm{g}^\mathrm{ch}}{2 \cdot k_\mathrm{b}T}\right)}}$$
$$\times \frac{3 \cdot \mathcal{F}_{1/2}\left(u_\mathrm{s} - \frac{E_\mathrm{g}^\mathrm{ch}}{2 \cdot k_\mathrm{b}T}\right)}{4 \cdot \sqrt{\mathcal{F}_{3/2}\left(u_\mathrm{s} - \frac{E_\mathrm{g}^\mathrm{ch}}{2 \cdot k_\mathrm{b}T}\right) - \mathcal{F}_{3/2}\left(u_\mathrm{c} - \frac{E_\mathrm{g}^\mathrm{ch}}{2 \cdot k_\mathrm{b}T}\right)}}. \qquad (4.16)$$

Now, the normalized surface potential is calculated by:

$$u_\mathrm{s,n} = u_\mathrm{s,n\text{-}1} - \frac{f(u_\mathrm{s,n\text{-}1})}{f'(u_\mathrm{s,n\text{-}1})}, \quad (n = 1, 2, 3), \qquad (4.17)$$

using the normalized 1D surface potential solution u_s shown in Eq. (4.12) as an initial guess for $u_\mathrm{s,1}$ in the Newton method. After three iterations, the surface potential u_s is obtained with a sufficient accuracy and can be used in the further calculations, where it is denoted as the effective gate-source voltage $V_\mathrm{gs,eff}$ in the following:

$$V_\mathrm{gs,eff}(V_\mathrm{gs}, V_\mathrm{ds}) = \frac{k_\mathrm{b}T}{q} \cdot u_\mathrm{s,3}. \qquad (4.18)$$

A schematic shape of $V_\mathrm{gs,eff}$ in dependency of V_gs for various V_ds is shown in Fig. 4.1(a). It can be seen that the smaller V_ds the smaller is the range where $V_\mathrm{gs,eff}$ follows V_gs. In the V_ds control regime, the effective gate-source voltage follows the drain-source voltage. If V_gs falls below the source voltage V_s, $V_\mathrm{gs,eff}$ is under control of V_s. Figure 4.1(b) illustrates the V_ds dependency on $V_\mathrm{gs,eff}$, where it can be seen that in the control regime of V_ds the effective gate-source voltage follows the applied V_ds and in the V_gs control regime $V_\mathrm{gs,eff}$ saturates to the applied gate-source voltage.

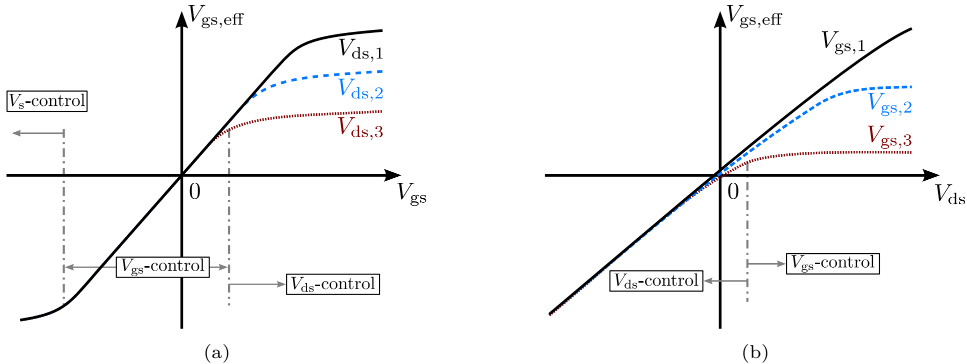

Figure 4.1.: Schematic shape of the effective gate-source voltage $V_\mathrm{gs,eff}$ in dependency of (a) the gate-source voltage V_gs and (b) the drain-source voltage V_ds. In (a): $V_\mathrm{ds,1} > V_\mathrm{ds,2} > V_\mathrm{ds,3}$. In (b): $V_\mathrm{gs,1} > V_\mathrm{gs,2} > V_\mathrm{gs,3}$.

The verification of the effective gate-source voltage $V_{gs,eff}$ and the channel potential φ_c^{1D} is presented in Sec. 4.3.1.

4.1.3 Scaling of the Gate Insulator

The second simplification is made because of the different dielectric permittivities of the gate insulator (ε_{ox}) and the channel material (ε_{ch}) as it is shown in Fig. 4.2(a). The different permittivities lead to discontinuities of the electric field at the channel-insulator interface which complicate the conformal mapping technique and should be avoided. It is to say that the conformal mapping technique needs a homogeneous permittivity in the area of interest. Assuming a constant electric field across gate insulator, which means that the potential drop is linear, the normal component of the dielectric displacement is described by:

$$D_{ox} = \varepsilon_0 \cdot \varepsilon_{ch} \cdot E_0 = \varepsilon_0 \cdot \varepsilon_{ox} \cdot E_{ox} = \varepsilon_0 \cdot \varepsilon_{ox} \cdot \frac{V_{ox}}{t_{ox}}, \tag{4.19}$$

with the voltage drop over the insulator V_{ox}, the normal component of the electric field in the channel E_0 and the electric field across the insulator E_{ox}.

To avoid discontinuities in the electric field the gate insulator or oxide thickness t_{ox} is scaled as follows (see Fig. 4.2(b)):

$$\tilde{t}_{ox} = \frac{\varepsilon_{ch}}{\varepsilon_{ox}} \cdot t_{ox} \tag{4.20}$$

and D_{ox} yields:

$$D_{ox} = \varepsilon_0 \cdot \varepsilon_{ch} \cdot \frac{V_{ox}}{\tilde{t}_{ox}}. \tag{4.21}$$

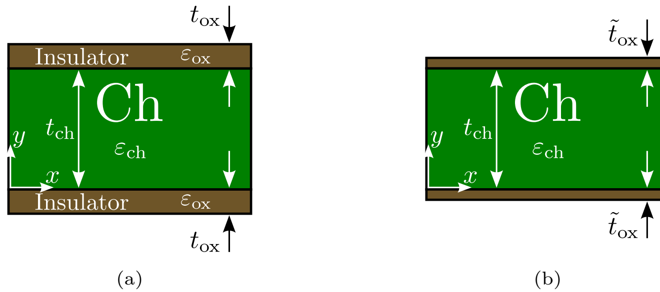

Figure 4.2.: (a) Default device structure with a gate insulator thickness of t_{ox} and two different permittivities ε for the channel and the gate insulator. (b) Adapted device structure with a scaled gate insulator thickness $\tilde{t}_{ox}$ and a uniform permittivity ε_{ch}.

It should be noticed that this assumption is only valid if the channel length is much bigger than the gate insulator thickness $l_{ch} \gg t_{ox}$ [161] and if inversion charges are negligible.

For the case that inversion charges come into play, the gate insulator thickness has to be scaled in dependency of the effective gate-source voltage $V_{gs,eff}$. At first, the screening length at the channel surface that characterizes the potential bending in x-direction is expressed in

terms of $V_{\mathrm{gs,eff}}$:

$$\tilde{\lambda}_{\mathrm{s/d}}(V_{\mathrm{gs,eff}}) = \lambda_{(V_{\mathrm{ds}}=0)} + \left(\lambda_0 - \lambda_{(V_{\mathrm{ds}}=0)}\right) \times \left(1 - \exp\left[-\ln\left(\frac{V_{\mathrm{ds}}}{|V_{\mathrm{gs}} - V_{\mathrm{gs,eff}}|} + 1 + \lambda_{\mathrm{ln,fit}}^{\mathrm{s/d}}\right)\right]\right), \tag{4.22}$$

whereby $\lambda_{\mathrm{ln,fit}}^{\mathrm{s/d}}$ is a fitting parameter to tune the influence of the inversion charges and the screening length at $V_{\mathrm{ds}} = 0$ is given by [122, 162]:

$$\lambda_{(V_{\mathrm{ds}}=0)} = \sqrt{\left(\frac{1}{\lambda_0} + \frac{8 \cdot 2 \cdot C'_{\mathrm{ox}} \cdot [V_{\mathrm{gs}} - V_{\mathrm{gs,eff}}(V_{\mathrm{ds}} = 0)]}{\varepsilon_{\mathrm{ch}} \cdot t_{\mathrm{ch}} \cdot V_{\mathrm{gs,eff}}(V_{\mathrm{ds}} = 0)}\right)^{-1}}. \tag{4.23}$$

The factor 8 in this expression is taken from [162], the factor 2 accounts for the DG structure in comparison to a SG device in the calculations of C'_{ox}. The natural screening length at the channel surface is defined by [163]:

$$\lambda_0 = \sqrt{\frac{\varepsilon_{\mathrm{ch}} \cdot t_{\mathrm{ch}} \cdot t_{\mathrm{ox}}}{2 \cdot \varepsilon_{\mathrm{ox}}}}. \tag{4.24}$$

Now, the gate insulator thickness t_{ox} can be expressed in terms of $\tilde{\lambda}_{\mathrm{s/d}}$:

$$t_{\mathrm{ox}}(V_{\mathrm{gs,eff}}) = 2 \cdot \frac{\left(\tilde{\lambda}_{\mathrm{s/d}}(V_{\mathrm{gs,eff}})\right)^2 \cdot \varepsilon_{\mathrm{ox}}}{t_{\mathrm{ch}} \cdot \varepsilon_{\mathrm{ch}}}. \tag{4.25}$$

By inserting Eq. (4.25) in Eq. (4.20), the scaled gate insulator thickness $\tilde{t}_{\mathrm{ox}}$ is expressed in terms of $V_{\mathrm{gs,eff}}$:

$$\tilde{t}_{\mathrm{ox}}(V_{\mathrm{gs,eff}}) = 2 \cdot \frac{\left(\tilde{\lambda}_{\mathrm{s/d}}(V_{\mathrm{gs,eff}})\right)^2}{t_{\mathrm{ch}}}. \tag{4.26}$$

The obtained expression is suitable for all operation regimes of the DG TFET and is used in the further calculations.

4.1.4 Decomposition of the Device Structure and Boundary Conditions

The device channel electrostatics of the DG TFET is a 4-corner problem as it is depicted in Fig. 4.3(a). Solving for the potential solution of the 4-corner structure is mathematically very challenging and often no closed-form solutions are found. For this reason, the device is decomposed into 2-corner structures to simplify finding a potential solution. This approximation is suitable if the channel length is bigger than the channel thickness ($l_{\mathrm{ch}} > t_{\mathrm{ch}}$) [164].

Regarding the boundaries of the DG TFET channel and gate insulator region, there is a constant boundary condition at the gate insulator interfaces $V_{\mathrm{gs,eff}}$ (see Fig. 4.3(a)). At the source-to-channel and drain-to-channel junction are parabolic boundaries which are denoted as

the effective built-in potentials $\varPhi_{\mathrm{bi,eff}}^{\mathrm{s/d}}$ (see Fig. 4.3(a)) and are given by [128, 165]:

$$\varPhi_{\mathrm{bi,eff}}^{\mathrm{s/d}}(y) = \varPhi_{\mathrm{bi}}^{\mathrm{s/d}} + V_{\mathrm{s/d}} \pm \Delta\varPhi_{\mathrm{bi,eff}}^{\mathrm{s/d}}(y), \tag{4.27}$$

with:

$$\Delta\varPhi_{\mathrm{bi,eff}}^{\mathrm{s/d}}(y) = \left|V_{\mathrm{gs,eff}} - \varPhi_{\mathrm{bi}}^{\mathrm{s/d}} - V_{\mathrm{s/d}}\right| + \frac{q\cdot\lambda_{\mathrm{s/d}}^{2}(y)}{\varepsilon_{\mathrm{s/d}}\cdot N_{\mathrm{s/d}}} \times \left(1 - \sqrt{1 + \frac{2\cdot\varepsilon_{\mathrm{s/d}}\cdot\left|V_{\mathrm{gs,eff}} - \varPhi_{\mathrm{bi}}^{\mathrm{s/d}} - V_{\mathrm{s/d}}\right|}{\lambda_{\mathrm{s/d}}^{2}(y)\cdot q\cdot N_{\mathrm{s/d}}}}\right), \tag{4.28}$$

using the source/drain doping concentration $N_{\mathrm{s/d}}$, the permittivity of the source/drain region $\varepsilon_{\mathrm{s/d}}$, the built-in potentials of source/drain $\varPhi_{\mathrm{bi}}^{\mathrm{s/d}}$ and the source/drain bias $V_{\mathrm{s/d}}$. The sign of $\Delta\varPhi_{\mathrm{bi,eff}}^{\mathrm{s/d}}$ in Eq. (4.27) is negative when $(\varPhi_{\mathrm{bi}}^{\mathrm{s/d}} + V_{\mathrm{s/d}}) > V_{\mathrm{gs,eff}}$ and positive for all other cases. The screening length $\lambda_{\mathrm{s/d}}$ characterizes the potential bending along the x-axis and is defined by [128, 166]:

$$\lambda_{\mathrm{s/d}}(y) = \lambda_{\mathrm{fit}}^{\mathrm{s/d}} \cdot \sqrt{\frac{\varepsilon_{\mathrm{ch}}\cdot\tilde{t}_{\mathrm{ox}}\cdot t_{\mathrm{ch}}}{2\cdot\varepsilon_{\mathrm{ox}}}\cdot\left(1 + \frac{\varepsilon_{\mathrm{ox}}}{\varepsilon_{\mathrm{ch}}\cdot\tilde{t}_{\mathrm{ox}}}\cdot y - \frac{\varepsilon_{\mathrm{ox}}}{\varepsilon_{\mathrm{ch}}\cdot\tilde{t}_{\mathrm{ox}}\cdot t_{\mathrm{ch}}}\cdot y^{2}\right)}, \tag{4.29}$$

whereby $\lambda_{\mathrm{fit}}^{\mathrm{s/d}}$ is an adjustable parameter. The built-in potential $\varPhi_{\mathrm{bi}}^{\mathrm{s/d}}$ is calculated as follows:

$$\varPhi_{\mathrm{bi}}^{\mathrm{s/d}} = \mp\frac{1}{q}\cdot\left(E_{\mathrm{s/d}} + \frac{E_{\mathrm{g}}^{\mathrm{s/d}}}{2}\right). \tag{4.30}$$

The term $E_{\mathrm{s/d}}$ describes the difference of the S/D Fermi energy level and the ValB/ConB at the source/drain edge, whose values are listed in Tab. 5.1 for various $N_{\mathrm{s/d}}$. This difference is caused by the high doping concentrations of the S and D region and is called degeneration.

Based on this equations, the 4-corner structure in Fig. 4.3(a) is decomposed in six 2-corner structures. This simplification can be done since the method of superposition is valid. The boundary condition at the source-to-channel junction is separated into a constant boundary $\varPhi_{\mathrm{bi,eff}}^{\mathrm{s}}(0)$ (see Fig. 4.3(b)) and a parabolic one $\Delta\varPhi_{\mathrm{bi,eff}}^{\mathrm{s}}(y)$ as it is shown in Fig. 4.3(d). The constant boundary condition at the gate insulator interface $V_{\mathrm{gs,eff}}$ is applied in the 2-corner problem in Fig. 4.3(b). Regarding the drain-to-channel junction, the boundary condition is also separated into a constant one $(\varPhi_{\mathrm{bi,eff}}^{\mathrm{d}}(0) - V_{\mathrm{gs,eff}})$ and a parabolic one $\Delta\varPhi_{\mathrm{bi,eff}}^{\mathrm{d}}(y)$ which are depicted in Fig. 4.3(c) and 4.3(e).

The boundary condition across the gate insulator is assumed to be linear and is also separated into a source (see Fig. 4.3(f)) and drain related case as it can be seen in Fig. 4.3(g). The linear boundary can be expressed in terms of the electric field along the gate insulator interface as follows [167]:

$$\varPhi_{\mathrm{L}}^{\mathrm{s/d}}(\bar{z}) = E_{\mathrm{ox}}\cdot x. \tag{4.31}$$

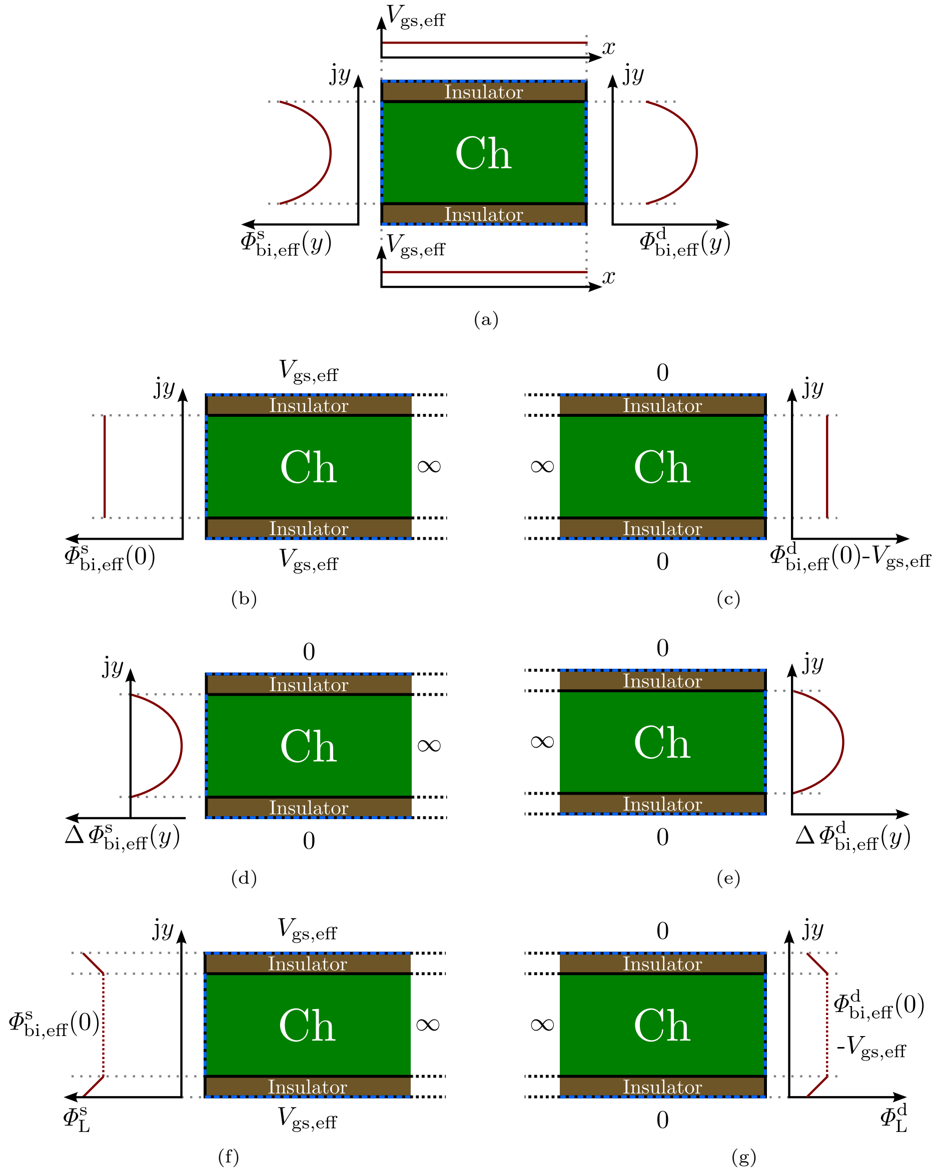

Figure 4.3.: Decomposition of the DG structure to simplify the conformal mapping and to separate the boundary conditions. (a) DG 4-corner structure with its original boundary conditions, that are a mixture of parabolic and constant boundaries. (b) Constant boundary for the source related case and (c) drain related case. (d) Parabolic boundary condition for the source related case and (e) drain related case. (f) Linear boundary condition across the gate insulator for the source related case and (g). (b)-(g): For a better overview, only the various boundary conditions at the source and drain end of the channel are illustrated. However, the constant boundary condition along the gate insulator is still valid.

4.1.5 Mapping of the Device Structure

In order to find an analytical solution of the 2D electrostatic potential of the TFET, the device structure is conformally mapped from the complex $\bar{z}$-plane into the upper half of the $\bar{w}$-plane. Since the DG TFET structure can be characterized by two closed polygons as it is depicted in Fig. 4.4, the Schwarz-Christoffel transformation (see Eq. (2.26)) is used to conformally map the given geometry.

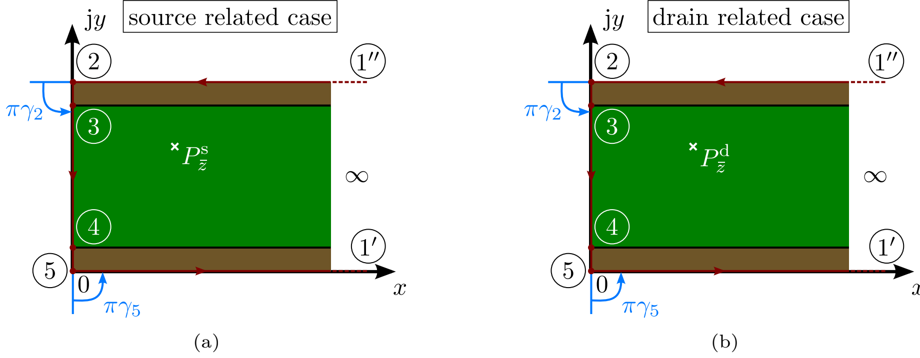

Figure 4.4.: (a) Source related and (b) drain related polygon to map the DG structure from the complex $\bar{z}$ into the upper half of the $\bar{w}$-plane.

Applying the vertices defined in Tab. 4.1 and using Eq. (2.26), the conformal mapping function yields:

$$\frac{\mathrm{d}\bar{z}}{\mathrm{d}\bar{w}} = C_1 \cdot (\bar{w}-1)^{-\frac{1}{2}} \cdot (\bar{w}+1)^{-\frac{1}{2}} = \frac{C_1}{\sqrt{\bar{w}-1} \cdot \sqrt{\bar{w}+1}}. \tag{4.32}$$

Table 4.1.: Definition of the vertices to map the DG structure.

i	w_i	z_i	$\alpha_i = \pi\gamma_i$	γ_i
$1''$	$-\infty$	$\infty + \mathrm{j}(2\tilde{t}_{\mathrm{ox}} + t_{\mathrm{ch}})$	$+\pi$	$+1$
2	-1	$0 + \mathrm{j}(2\tilde{t}_{\mathrm{ox}} + t_{\mathrm{ch}})$	$+\pi/2$	$+1/2$
3	—	$0 + \mathrm{j}(\tilde{t}_{\mathrm{ox}} + t_{\mathrm{ch}})$	0	0
4	—	$0 + \mathrm{j}\tilde{t}_{\mathrm{ox}}$	0	0
5	$+1$	$0 + \mathrm{j}0$	$+\pi/2$	$+1/2$
$1'$	$+\infty$	$+\infty + \mathrm{j}0$	$+\pi$	$+1$

An integration of Eq. (4.32) leads to:

$$\bar{z}(\bar{w}) = C_1 \cdot \ln\left(\left|\bar{w} + \sqrt{\bar{w}^2 - 1}\right|\right) + C_2 = C_1 \cdot \cosh^{-1}(\bar{w}) + C_2, \tag{4.33}$$

where the integration constant C_2 defines the origin of the $\bar{z}$-plane. Since the origin is defined by the vertex 5, the integration constant results in: $C_2 = 0 + \mathrm{j}0$. The scale and rotation constant

C_1 is calculated in terms of Eq. (2.30) since the vertices $1'$ and $1''$ in Fig. 4.4 are parallel lines:

$$\bar{z}_{1''} - \bar{z}_{1'} = \mathrm{j}\pi C_1 = \lim_{z_{\mathrm{Re}} \to \infty} \big(z_{\mathrm{Re}} + \mathrm{j}(2\tilde{t}_{\mathrm{ox}} + t_{\mathrm{ch}}) - (z_{\mathrm{Re}} + \mathrm{j}0)\big) = \mathrm{j}(2\tilde{t}_{\mathrm{ox}} + t_{\mathrm{ch}})$$
$$\Rightarrow C_1 = \frac{2\tilde{t}_{\mathrm{ox}} + t_{\mathrm{ch}}}{\pi} = \frac{\Delta y}{\pi}, \tag{4.34}$$

with the channel thickness t_{ch} (see Fig. 3.6) and the scaled gate insulator thickness $\tilde{t}_{\mathrm{ox}}$ as it is shown in Eq. (4.26). Now, the final function to map a point in $\bar{w}$-plane into $\bar{z}$-plane is defined by:

$$\bar{z}(\bar{w}) = \frac{\Delta y}{\pi} \cdot \cosh^{-1}(\bar{w}). \tag{4.35}$$

With the help of the inverse function of Eq. (4.35), the DG structure is mapped from the $\bar{z}$- into the upper half of the $\bar{w}$-plane as follows:

$$\bar{w}(\bar{z}) = f^{-1}(\bar{z}) = \cosh\left(\frac{\pi}{\Delta y} \cdot \bar{z}\right) = \cosh\left(\frac{\pi}{\Delta y} \cdot (x + \mathrm{j}y)\right). \tag{4.36}$$

Equation (4.36) can be applied in order to map an arbitrary point $P_{\bar{z}}^{\mathrm{s}}$ within the channel (see Fig. 4.4(a)) of the source related case into $\bar{w}$-plane by:

$$\bar{w}_{\mathrm{s}}(\bar{z}) = \cosh\left(\frac{\pi}{\Delta y} \cdot (x + \mathrm{j}y)\right). \tag{4.37}$$

On the other hand, in the drain related case (see Fig. 4.4(b)) an arbitrary point in the channel $P_{\bar{z}}^{\mathrm{d}}$ is mapped into $\bar{w}$-plane by:

$$\bar{w}_{\mathrm{d}}(\bar{z}) = \cosh\left(\frac{\pi}{\Delta y} \cdot (l_{\mathrm{ch}} - x + \mathrm{j}y)\right), \tag{4.38}$$

which is the solution for the source related case mirrored on the y-axis.

By using the inverse mapping function (see Eq. (4.36)) the vertices of the 2-corner structure in $\bar{z}$-plane are mapped onto the real u-axis of the $\bar{w}$-plane. In order to represent both points $1'', 1'$, whose real values are lying in infinity, the x-values are chosen to be three times the value of the channel length l_{ch} [167]. Mapping the vertices in Tab. 4.1 for the source and drain related case yields:

$$u'_{1''} = \cosh\left(\frac{\pi}{\Delta y} \cdot \left[3 \cdot l_{\mathrm{ch}} + \mathrm{j}(2\tilde{t}_{\mathrm{ox}} + t_{\mathrm{ch}})\right]\right), \quad u'_2 = \cosh\left(\frac{\pi}{\Delta y} \cdot \left[0 + \mathrm{j}(2\tilde{t}_{\mathrm{ox}} + t_{\mathrm{ch}})\right]\right) = -1,$$
$$u'_3 = \cosh\left(\frac{\pi}{\Delta y} \cdot \left[0 + \mathrm{j}(\tilde{t}_{\mathrm{ox}} + t_{\mathrm{ch}})\right]\right), \quad u'_4 = \cosh\left(\frac{\pi}{\Delta y} \cdot \left[0 + \mathrm{j}\tilde{t}_{\mathrm{ox}}\right]\right),$$
$$u'_5 = \cosh\left(\frac{\pi}{\Delta y} \cdot \left[0 + \mathrm{j}0\right]\right) = +1, \quad u'_{1'} = \cosh\left(\frac{\pi}{\Delta y} \cdot \left[3 \cdot l_{\mathrm{ch}} + \mathrm{j}0\right]\right). \tag{4.39}$$

4.2 Closed-Form Potential Solution for the Channel Region

The closed-form potential solution within the channel region of a DG TFET is introduced in the following. The electrostatic solutions for the various boundary conditions mentioned in Sec. 4.1.4 are presented separately.

The 2D channel potential $\varphi_{\mathrm{2D}}^{\mathrm{ch}}$ is obtained by solving Poisson's integral in the complex $\bar{w}$-plane and superposing the electrostatic solutions $\varphi_{\mathrm{C,P,L}}$ for constant boundary conditions Φ_{C}, parabolic ones Φ_{P} and linear boundary conditions Φ_{L}:

$$\varphi_{\mathrm{2D}}^{\mathrm{ch}}\left(\bar{w}_{\mathrm{s/d}}(\bar{z})\right) = \varphi_{\mathrm{C}}\left(\bar{w}_{\mathrm{s/d}}(\bar{z})\right) + \varphi_{\mathrm{P}}\left(\bar{w}_{\mathrm{s/d}}(\bar{z})\right) + \varphi_{\mathrm{L}}\left(\bar{w}_{\mathrm{s/d}}(\bar{z})\right), \tag{4.40}$$

where $\bar{z} = x + \mathrm{j}y$ defines an arbitrary point within the channel region of the DG TFET.

4.2.1 Solution for a Piecewise Constant Boundary

A solution for a piecewise constant boundary condition Φ_{C} in an interval between two arbitrary points u'_{a} and u'_{b} is found by solving Poisson's integral (see Eq. (2.36)) in the complex $\bar{w}$-plane as follows:

$$\phi_{\mathrm{C}}\left(\bar{w}_{\mathrm{s/d}}(\bar{z})\right) = \frac{1}{\pi} \cdot \int_{u'_{\mathrm{a}}}^{u'_{\mathrm{b}}} \frac{v}{(u-u')^2 + v^2} \cdot \Phi_{\mathrm{C}} \,\mathrm{d}u' = -\frac{\Phi_{\mathrm{C}}}{\pi} \cdot \arctan\left(\frac{u-u'}{v}\right)\Bigg|_{u'_{\mathrm{a}}}^{u'_{\mathrm{b}}}. \tag{4.41}$$

The potential solutions for the piecewise constant boundary conditions ϕ_{C} are obtained by applying the parameter listed in Tab. 4.2 to Eq. (4.41). It should be noted that the potential solutions $\phi_{\mathrm{C}}^{\mathrm{s,1}}$ and $\phi_{\mathrm{C}}^{\mathrm{s,3}}$ are part of the linear boundary conditions (see Fig. 4.3(f) and 4.3(g)) and describe the constant offset of the linear potential solution. Now, the potential solution for piecewise constant boundary conditions is obtained by superposition:

$$\varphi_{\mathrm{C}}\left(\bar{w}_{\mathrm{s/d}}(\bar{z})\right) = \phi_{\mathrm{C}}^{\mathrm{g,1}} + \phi_{\mathrm{C}}^{\mathrm{g,2}} + \phi_{\mathrm{C}}^{\mathrm{s,1}} + \phi_{\mathrm{C}}^{\mathrm{s,2}} + \phi_{\mathrm{C}}^{\mathrm{s,3}} + \phi_{\mathrm{C}}^{\mathrm{d}}. \tag{4.42}$$

Table 4.2.: Potential solutions for the piecewise constant boundaries between the points u'_{a} and u'_{b}.

ϕ_{C}	$\bar{w}_{\mathrm{s/d}}(\bar{z})$	Φ_{C}	u'_{a}	u'_{b}
$\phi_{\mathrm{C}}^{\mathrm{g,1}}$	$\bar{w}_{\mathrm{s}}(\bar{z})$	$V_{\mathrm{gs,eff}}$	$u'_{1''}$	u'_2
$\phi_{\mathrm{C}}^{\mathrm{g,2}}$	$\bar{w}_{\mathrm{s}}(\bar{z})$	$V_{\mathrm{gs,eff}}$	u'_5	$u'_{1'}$
$\phi_{\mathrm{C}}^{\mathrm{s,1}}$	$\bar{w}_{\mathrm{s}}(\bar{z})$	$V_{\mathrm{gs,eff}}$	u'_2	u'_3
$\phi_{\mathrm{C}}^{\mathrm{s,2}}$	$\bar{w}_{\mathrm{s}}(\bar{z})$	$\Phi_{\mathrm{bi,eff}}^{\mathrm{s}}(0)$	u'_3	u'_4
$\phi_{\mathrm{C}}^{\mathrm{s,3}}$	$\bar{w}_{\mathrm{s}}(\bar{z})$	$V_{\mathrm{gs,eff}}$	u'_4	u'_5
$\phi_{\mathrm{C}}^{\mathrm{d}}$	$\bar{w}_{\mathrm{d}}(\bar{z})$	$\Phi_{\mathrm{bi,eff}}^{\mathrm{d}}(0) - V_{\mathrm{gs,eff}}$	u'_3	u'_4

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4.2.2 Solution for a Piecewise Parabolic Boundary

The parabolic boundary problem is solved by using Poisson's integral and applying the geometry dependent boundary condition. The parabolic shaped boundary problem in $\bar{z}$-plane needs to be mapped in $\bar{w}$-plane, which is approximated by an elliptical shape [168]:

$$\Phi_{\mathrm{P}}(u') = \Delta\Phi_{\mathrm{P}} \cdot \sqrt{1-(u')^2}, \tag{4.43}$$

where this approximation is valid for $l_{\mathrm{ch}} \gg t_{\mathrm{ch}}$ [168]. $\Delta\Phi_{\mathrm{P}}$ is the difference of the effective built-in potentials and is given by:

$$\Delta\Phi_{\mathrm{P}}^{\mathrm{s/d}} = \Phi_{\mathrm{bi,eff}}^{\mathrm{s/d}}(y = {}^{t_{\mathrm{ch}}}/_{2}) - \Phi_{\mathrm{bi,eff}}^{\mathrm{s/d}}(y=0). \tag{4.44}$$

Now, solving Poisson's integral leads to the potential solution for a parabolic boundary condition:

$$\begin{aligned}\phi_{\mathrm{P}}\left(\bar{w}_{\mathrm{s/d}}(\bar{z})\right) &= \frac{1}{\pi} \cdot \int_{-1}^{1} \frac{v}{(u-u')^2+v^2} \cdot \Delta\Phi_{\mathrm{P}} \cdot \sqrt{1-(u')^2}\,\mathrm{d}u' \\ &= \Delta\Phi_{\mathrm{P}} \cdot \left[\frac{1}{2} \cdot \left(\sqrt{1-(u-\mathrm{j}v)^2} + \sqrt{1-(u+\mathrm{j}v)^2}\right) - v\right].\end{aligned} \tag{4.45}$$

Since there is a source and drain related case of the parabolic boundary condition (see Fig. 4.3(d) and (e)), Eq. (4.45) is calculated for both cases as follows:

$$\phi_{\mathrm{P}}^{\mathrm{s}}\left(\bar{w}_{\mathrm{s}}(\bar{z})\right) = \Delta\Phi_{\mathrm{P}}^{\mathrm{s}} \cdot \left[\frac{1}{2} \cdot \left(\sqrt{1-(u-\mathrm{j}v)^2} + \sqrt{1-(u+\mathrm{j}v)^2}\right) - v\right] \tag{4.46}$$

$$\phi_{\mathrm{P}}^{\mathrm{d}}\left(\bar{w}_{\mathrm{d}}(\bar{z})\right) = \Delta\Phi_{\mathrm{P}}^{\mathrm{d}} \cdot \left[\frac{1}{2} \cdot \left(\sqrt{1-(u-\mathrm{j}v)^2} + \sqrt{1-(u+\mathrm{j}v)^2}\right) - v\right] \tag{4.47}$$

Finally, the potential solution for a piecewise boundary condition yields:

$$\varphi_{\mathrm{P}}\left(\bar{w}_{\mathrm{s/d}}(\bar{z})\right) = \phi_{\mathrm{P}}^{\mathrm{s}} + \phi_{\mathrm{P}}^{\mathrm{d}}. \tag{4.48}$$

4.2.3 Solution for a Piecewise Linear Boundary

The potential drop across the gate insulator is assumed to be linear as it is depicted in Fig. 4.3(f) and (g). In order to solve Poisson's integral, the linear boundary condition in Eq. (4.31) is mapped in $\bar{w}$-plane [167]:

$$\Phi_{\mathrm{L}}(u') = E_{\mathrm{ox}} \cdot \frac{t_{\mathrm{ox}}}{\pi} \cdot \cosh^{-1}(u'). \tag{4.49}$$

The Poisson integral is rewritten as:

$$\phi_{\mathrm{L}}\left(\bar{w}_{\mathrm{s/d}}(\bar{z})\right) = \frac{1}{\pi} \cdot \int_{u'_{\mathrm{a}}}^{u'_{\mathrm{b}}} \frac{v}{(u-u')^2+v^2} \cdot E_{\mathrm{ox}} \cdot \frac{t_{\mathrm{ox}}}{\pi} \cdot \cosh^{-1}(u')\,\mathrm{d}u', \tag{4.50}$$

where this expression has no analytical solution. For this reason, the boundary condition is approximated by a square root function:

$$E_{\mathrm{ox}} \cdot \frac{t_{\mathrm{ox}}}{\pi} \cdot \cosh^{-1}(u') \approx \pm\sqrt{\frac{u' - b_{\mathrm{L}}}{a_{\mathrm{L}}}} \tag{4.51}$$

and inserted into Poisson's integral which leads to:

$$\begin{aligned} \phi_{\mathrm{L}}\left(\bar{w}_{\mathrm{s/d}}(\bar{z})\right) &= \frac{1}{\pi} \cdot \int_{u'_{\mathrm{a}}}^{u'_{\mathrm{b}}} \frac{v}{(u-u')^2 + v^2} \cdot \pm\sqrt{\frac{u' - b_{\mathrm{L}}}{a_{\mathrm{L}}}}\,\mathrm{d}u' \\ &= \pm\frac{\mathrm{j}}{\pi}\left[\sigma_{\mathrm{L},3} \cdot \arctan\left(\frac{a_{\mathrm{L}} \cdot u \cdot \sigma_{\mathrm{L},1} \cdot \sigma_{\mathrm{L},3} - a_{\mathrm{L}} \cdot b_{\mathrm{L}} \cdot \sigma_{\mathrm{L},1} \cdot \sigma_{\mathrm{L},3} + \mathrm{j} \cdot a_{\mathrm{L}} \cdot v \cdot \sigma_{\mathrm{L},1} \cdot \sigma_{\mathrm{L},3}}{\sigma_{\mathrm{L},4}}\right)\right. \\ &\quad \left.\left. + \ \sigma_{\mathrm{L},2} \cdot \arctan\left(\frac{a_{\mathrm{L}} \cdot b_{\mathrm{L}} \cdot \sigma_{\mathrm{L},1} \cdot \sigma_{\mathrm{L},2} - a_{\mathrm{L}} \cdot u \cdot \sigma_{\mathrm{L},1} \cdot \sigma_{\mathrm{L},2} + \mathrm{j} \cdot a_{\mathrm{L}} \cdot v \cdot \sigma_{\mathrm{L},1} \cdot \sigma_{\mathrm{L},2}}{\sigma_{\mathrm{L},4}}\right)\right]\right|_{u'_{\mathrm{a}}}^{u'_{\mathrm{b}}}, \end{aligned} \tag{4.52}$$

with:

$$\begin{gathered} \sigma_{\mathrm{L},1} = \sqrt{-\frac{b_{\mathrm{L}} - u'}{a_{\mathrm{L}}}}, \quad \sigma_{\mathrm{L},2} = \sqrt{\frac{b_{\mathrm{L}} - u - \mathrm{j}v}{a_{\mathrm{L}}}}, \quad \sigma_{\mathrm{L},3} = \sqrt{\frac{b_{\mathrm{L}} - u + \mathrm{j}v}{a_{\mathrm{L}}}}, \\ \sigma_{\mathrm{L},4} = b_{\mathrm{L}}^2 - 2 \cdot b_{\mathrm{L}} \cdot u + u^2 + v^2. \end{gathered} \tag{4.53}$$

The sign of the square root is determined by the boundary potentials $\Phi_{\mathrm{L},1}$ and $\Phi_{\mathrm{L},2}$. The sign is positive when $\Phi_{\mathrm{L},1} \leq \Phi_{\mathrm{L},2}$ and negative for $\Phi_{\mathrm{L},1} > \Phi_{\mathrm{L},2}$. The parameter a_{L} is defined by [167]:

$$a_{\mathrm{L}} = \frac{u'_{\mathrm{step}} - b_{\mathrm{L}}}{(\Phi_{\mathrm{L},2} - \Phi_{\mathrm{L},1})^2}. \tag{4.54}$$

For a detailed derivation of the potential solution for a piecewise linear boundary condition the reader is kindly asked to refer to [167].

Table 4.3.: Potential solutions and applied parameters for the piecewise linear boundary conditions between the points u'_{a} and u'_{b}.

ϕ_{L}	$\bar{w}_{\mathrm{s/d}}(\bar{z})$	u'_{step}	b_{L}	$\Phi_{\mathrm{L},1}$	$\Phi_{\mathrm{L},2}$	u'_{a}	u'_{b}
$\phi_{\mathrm{L}}^{\mathrm{s},1}$	$\bar{w}_{\mathrm{s}}(\bar{z})$	u'_3	u'_2	$V_{\mathrm{gs,eff}}$	$\Phi^{\mathrm{s}}_{\mathrm{bi,eff}}(y=0)$	u'_2	u'_3
$\phi_{\mathrm{L}}^{\mathrm{s},2}$	$\bar{w}_{\mathrm{s}}(\bar{z})$	u'_4	u'_5	$V_{\mathrm{gs,eff}}$	$\Phi^{\mathrm{s}}_{\mathrm{bi,eff}}(y=0)$	u'_4	u'_5
$\phi_{\mathrm{L}}^{\mathrm{d},1}$	$\bar{w}_{\mathrm{d}}(\bar{z})$	u'_3	u'_2	0	$\Phi^{\mathrm{d}}_{\mathrm{bi,eff}}(y=0) - V_{\mathrm{gs,eff}}$	u'_2	u'_3
$\phi_{\mathrm{L}}^{\mathrm{d},2}$	$\bar{w}_{\mathrm{d}}(\bar{z})$	u'_4	u'_5	0	$\Phi^{\mathrm{d}}_{\mathrm{bi,eff}}(y=0) - V_{\mathrm{gs,eff}}$	u'_4	u'_5

The linear potential solution ϕ_{L} at an arbitrary point $\bar{z}$ is now calculated with the help of the parameters listed in Tab. 4.3 applied to Eq. (4.52):

$$\varphi_{\mathrm{L}}\left(\bar{w}_{\mathrm{s/d}}(\bar{z})\right) = \phi_{\mathrm{L}}^{\mathrm{s},1} + \phi_{\mathrm{L}}^{\mathrm{s},2} + \phi_{\mathrm{L}}^{\mathrm{d},1} + \phi_{\mathrm{L}}^{\mathrm{d},2}. \tag{4.55}$$

4.3 Potential Model Verification

The verification of the derived potential model is done with the help of numerical TCAD Sentaurus simulation data [79]. TCAD simulations are performed with the configuration described in Sec. 6.1. At first, the effective gate-source voltage $V_{\mathrm{gs,eff}}$ and the center potential $\varphi_{\mathrm{c}}^{\mathrm{1D}}$ are verified in Sec. 4.3.1. The 2D channel potential solution verification is presented in Sec. 4.3.2.

4.3.1 Verification of the Effective Gate-Source Voltage & Center Potential

The effective gate-source voltage $V_{\mathrm{gs,eff}}$ is applied as a boundary condition in the 2D potential solution in order to consider the effect of inversion charges in the potential calculations. For this reason, $V_{\mathrm{gs,eff}}$ is verified by TCAD simulations to ensure a correct modeling approach. It should be kept in mind that the effective gate-source voltage $V_{\mathrm{gs,eff}}$ denotes the surface potential of the TFET in the middle of the channel ($x = {}^{l_{\mathrm{ch}}}/_{2}$). Since $V_{\mathrm{gs,eff}}$ is calculated in dependency of $\varphi_{\mathrm{c}}^{\mathrm{1D}}$, the center potential is also verified. The TCAD potential values for $V_{\mathrm{gs,eff}}$ and $\varphi_{\mathrm{c}}^{\mathrm{1D}}$ are extracted at the positions as it is depicted in Fig. 4.5.

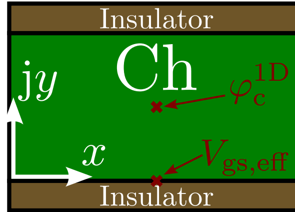


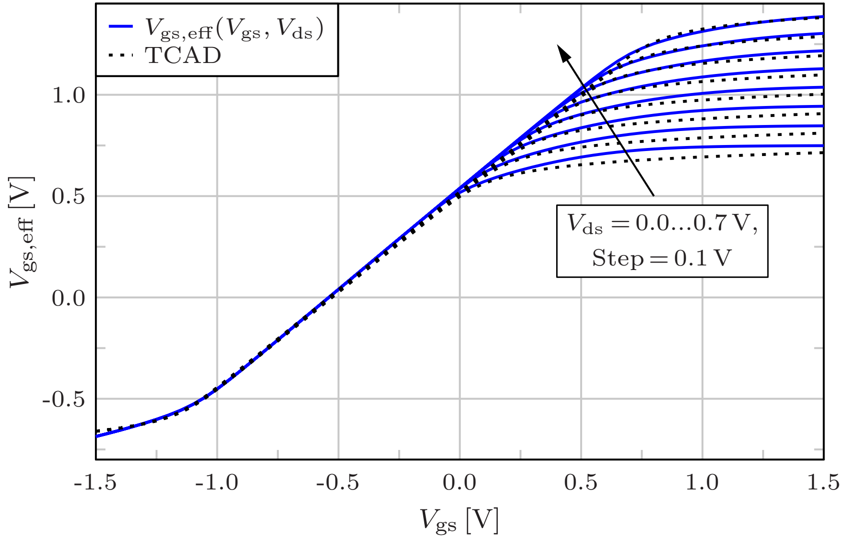
Figure 4.5.: DG TFET channel region sketch which highlights the positions from which the effective gate-source voltage and the center potential is extracted. Both values are taken from the position $x = {}^{l_{\mathrm{ch}}}/_{2}$, where $V_{\mathrm{gs,eff}}$ is extracted directly under the gate insulators ($y = 0\,\mathrm{nm}$) and $\varphi_{\mathrm{c}}^{\mathrm{1D}}$ at ($y = {}^{t_{\mathrm{ch}}}/_{2}$).

At first, the effective gate-source voltage $V_{\mathrm{gs,eff}}$ is simulated in dependency of V_{gs} for various fixed drain-source voltages V_{ds}. The modeling results of $V_{\mathrm{gs,eff}}$ vs. V_{gs} are shown in Fig. 4.6(a) by applying a flat band voltage of $V_{\mathrm{fb}} = -0.54\,\mathrm{V}$. The effective gate-source voltage matches well in comparison with TCAD simulations for various V_{ds}. It can be seen that $V_{\mathrm{gs,eff}}$ follows the applied gate-source voltage when the TFET is in the V_{gs}-control regime as it is depicted in Fig. 4.1(a). At a drain-source voltage of $V_{\mathrm{ds}} = 0\,\mathrm{V}$ the TFET is under V_{gs}-control in the range from $V_{\mathrm{gs}} = -1.1\,\mathrm{V}$ to $0\,\mathrm{V}$ and by increasing V_{ds} to $0.7\,\mathrm{V}$ the V_{gs}-control range expands to $[-1.1\,\mathrm{V} \leq V_{\mathrm{gs}} \leq 0.7\,\mathrm{V}]$. If the gate-source voltage overcomes the applied V_{ds}, $V_{\mathrm{gs,eff}}$ is under control of the drain-source voltage (see Fig. 4.1(a)). For a gate-source voltage $V_{\mathrm{gs}} < -1.1\,\mathrm{V}$, $V_{\mathrm{gs,eff}}$ is under control of V_{s}.

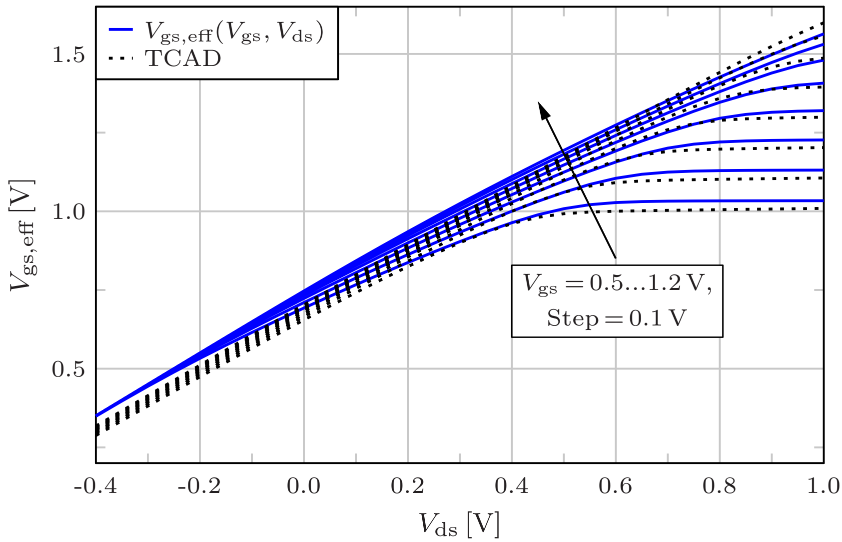
Figure 4.6(b) presents the modeling results of $V_{\mathrm{gs,eff}}$ vs. V_{ds} for various fixed gate-source voltages V_{gs}. It can be seen that the effective gate-source voltage follows the drain-source voltage when $V_{\mathrm{ds}} < V_{\mathrm{gs}}$, so $V_{\mathrm{gs,eff}}$ is in the V_{ds}-control regime (see Fig. 4.1(b)). For instance at

$V_{\mathrm{gs}} = 0.5\,\mathrm{V}$, the effective gate-source voltage switches at $V_{\mathrm{ds}} = 0.4\,\mathrm{V}$ from V_{ds}-control to the V_{gs}-control regime. It can be seen that the $V_{\mathrm{gs,eff}}$ modeling approach shows a good fit compared to the TCAD simulations with some small deviations occurring for negative V_{ds} values. These deviations are acceptable since the n-type TFET is driven for positive V_{ds}.

In a next step, the potential in the center of the channel $\varphi_{\mathrm{c}}^{\mathrm{1D}}$ is verified in dependency of the gate-source voltage for drain-source voltages from $V_{\mathrm{ds}} = 0\,\mathrm{V}$ to $0.7\,\mathrm{V}$. The modeling results are depicted in Fig. 4.7(a) and it can be seen that the modeling approach fits well for various V_{ds} values compared with TCAD data. Finally, the drain-source voltage V_{ds} is used as the sweep variable for different fixed V_{gs} values. The results are depicted in Fig. 4.7(b) and show a good match in comparison to the TCAD data for a gate-source voltage range from $V_{\mathrm{gs}} = 0.5\,\mathrm{V}$ to $1.2\,\mathrm{V}$.



(a) $V_{gs,eff}$ vs. V_{gs} for various V_{ds}.



(b) $V_{gs,eff}$ vs. V_{ds} for various V_{gs}.

Figure 4.6.: Model results of the effective gate-source voltage $V_{gs,eff}$, where in (a) V_{gs} is used as the sweep variable and V_{ds} is fixed. In (b) V_{ds} is used as the sweep variable and V_{gs} is fixed for different values. The results of Eq. (4.18) are illustrated in blue solid lines and TCAD simulation results are highlighted in black dashed lines.

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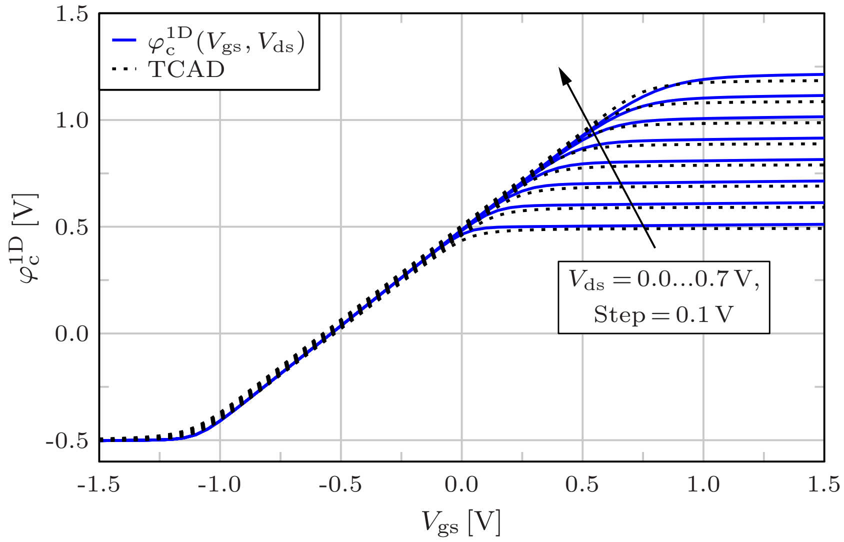
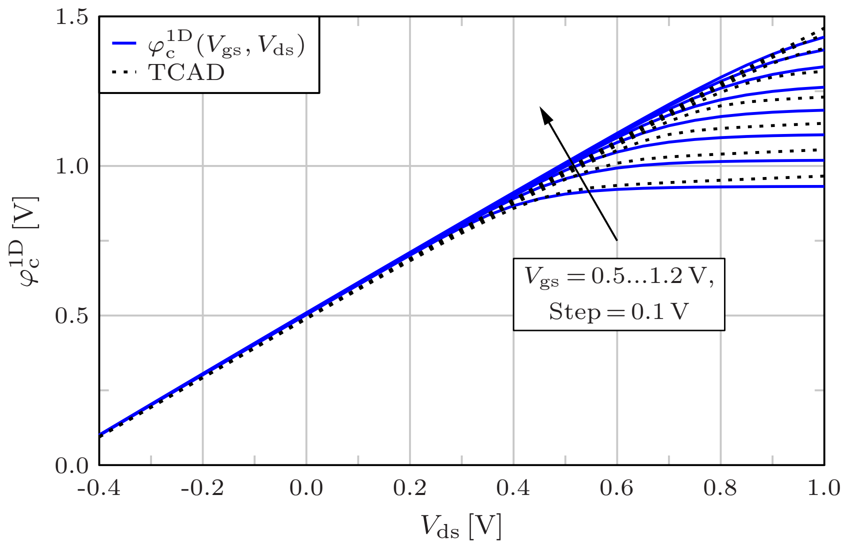


(a) φ_c^{1D} vs. V_{gs} for various V_{ds}.



(b) φ_c^{1D} vs. V_{ds} for various V_{gs}.

Figure 4.7.: Center potential φ_c^{1D} in dependency of (a) the gate-source voltage V_{gs} and various fixed V_{ds} values and (b) the drain-source voltage V_{ds} and different fixed V_{gs} values. The modeling results are calculated by Eq. (4.9) and shown in blue solid lines. TCAD data are plotted in black dashed lines.

4.3.2 Verification of the 2D Channel Potential Solution

The closed-form 2D potential solution within the channel region of the DG TFET is also verified by TCAD Sentaurus simulation data. The 2D electrostatic potential is calculated along the x-axis at two characteristic y-positions, the surface ($y = 0\,\text{nm}$) and the center of the channel region as it is illustrated in Fig. 4.8. Simulations are performed for gate-source voltages from $V_{\text{gs}} = -1.5\,\text{V}$ to $1.5\,\text{V}$ in order to verify the potential solution in the ON-, OFF- and AMBIPOLAR-state at $V_{\text{ds}} = 0.1\,\text{V}$ and $0.7\,\text{V}$. The adjustable parameters for all simulations are as follows: $\delta = 0\,\text{V}$, $V_{\text{fb}} = -0.54\,\text{V}$, $\lambda_{\text{ln,fit}}^{\text{s/d}} = 0.2$ and $\lambda_{\text{fit}}^{\text{s/d}} = 1.0$.

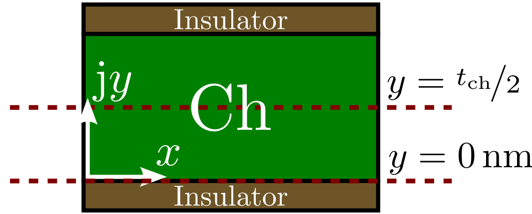


Figure 4.8.: Sketch of the DG TFET channel region where the 2D electrostatic potential is solved. The cutlines show the surface ($y = 0\,\text{nm}$) and center ($y = t_{\text{ch}}/2$) of the channel region.

The modeling results at the channel surface are shown in Fig. 4.9(a) and the results in the center of the channel are depicted in Fig. 4.9(b). In both cases simulations are performed at a drain-source voltage $V_{\text{ds}} = 0.7\,\text{V}$ in the aforementioned gate-source voltage range.

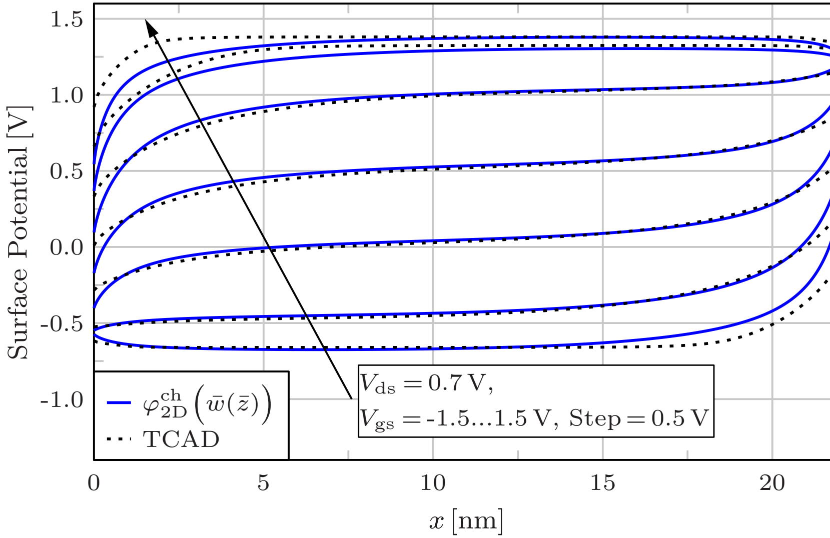
In Fig. 4.9(a) it can be seen that the surface potential matches well in comparison to the TCAD simulations from $V_{\text{gs}} = -1\,\text{V}$ to $1\,\text{V}$ with some small deviations occurring at the channel junctions. These deviations could be avoided by decreasing the parameter $\lambda_{\text{fit}}^{\text{s/d}}$, whereby the decrease of $\lambda_{\text{fit}}^{\text{s/d}}$ would increase the deviations of the potential solution at the junctions in the channel center. Thus, the chose of $\lambda_{\text{fit}}^{\text{s/d}} = 1$ represents a good compromise. At the gate-source voltages $V_{\text{gs}} = -1.5\,\text{V}$ and $1.5\,\text{V}$ one can see that the channel potential pinning occurs. For $V_{\text{gs}} = 1.5\,\text{V}$ (ON-state) some inaccuracies occur between $x = 0\,\text{nm}$ and $5\,\text{nm}$ and at $V_{\text{gs}} = -1.5\,\text{V}$ (AMBIPOLAR-state) there are some deviations in the range of $x = 15\,\text{nm}$ and $22\,\text{nm}$, which are caused by the parameter $\lambda_{\text{ln,fit}}^{\text{s/d}}$. Increasing this parameter would improve the fit at these biases but on the other hand worsens the potential solutions for $V_{\text{gs}} < 1.5\,\text{V}$ and $> -1.5\,\text{V}$.

Figure 4.9(b) presents the results of the center potential and it can be seen that the modeling approach shows a good fit compared to the TCAD simulation data. Some small deviations occur at the channel junction due to the chosen value of $\lambda_{\text{fit}}^{\text{s/d}}$ as it is mentioned in the previous paragraph. The channel potential pinning comes into play for $V_{\text{gs}} > 1\,\text{V}$ and $V_{\text{gs}} < -1\,\text{V}$ and some small inaccuracies occur in the range of $x = 4\,\text{nm}$ to $18\,\text{nm}$. These deviations are to explain by solving Laplace's equation instead of Poisson's equation and using the effective gate-source voltage $V_{\text{gs,eff}}$ to consider inversion charges. This simplification causes the biggest error in the channel center and decreases towards the channel surface.

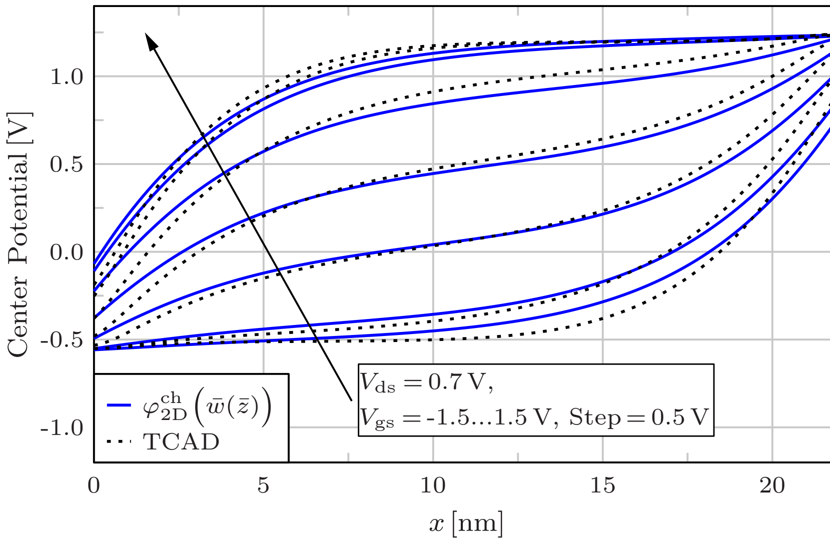
The results of the potential solution at the channel surface for $V_{\text{ds}} = 0.1\,\text{V}$ are illustrated in

Fig. 4.10(a). The comparison with TCAD data shows a good agreement in the whole applied V_{gs} range. At this V_{ds} value it can be seen that the potential pinning in the ON-state occurs already from $V_{gs} = 0.5\,V$ as it has been shown in Fig. 4.6(a). The potential solution in the AMBIPOLAR-state, i.e. $V_{gs} \leq -0.5\,V$, is not affected by the potential pinning effect. Regarding the channel junctions some small deviations can be seen which are to explain by the choice of the parameter $\lambda_{fit}^{s/d}$ as it is mentioned in the last paragraph.

Finally, the potential solution in the center of the channel ($y = t_{ch}/2$) is verified for $V_{ds} = 0.1\,V$. The modeling results compared to numerical TCAD data are depicted in Fig. 4.10(b), where the 2D potential solutions correlate well with the TCAD simulations. In the ON-state one can see the potential pinning effect again for $V_{gs} \geq 0.5\,V$. The occurring inaccuracies can be ascribed to $\lambda_{fit}^{s/d} = 1$ as it has been described in the paragraphs before.



(a) Surface Potential ($y = 0$ nm).



(b) Center Potential ($y = t_{ch}/2$).

Figure 4.9.: 2D closed-form potential modeling results for $V_{ds} = 0.7$ V at (a) the surface of the channel and (b) the channel center. The 2D potential solution (blue solid lines) is compared to TCAD simulation data (black dashed lines).

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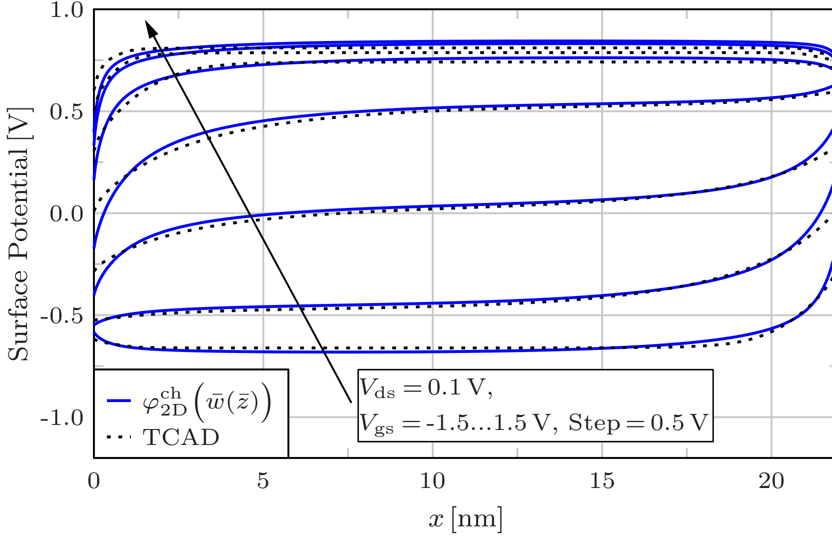
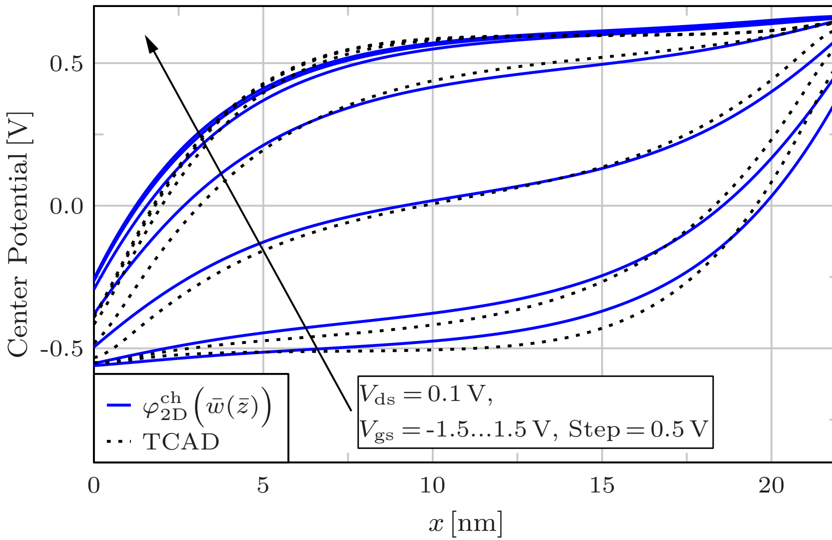


(a) Surface Potential ($y = 0$ nm).



(b) Center Potential ($y = t_{ch}/2$).

Figure 4.10.: Modeling results of the 2D closed-form potential at (a) the surface of the channel and (b) the channel center for a drain-source voltage $V_{ds} = 0.1$ V and compared to TCAD data. 2D potential solution: blue solid lines. TCAD simulations: black dashed lines.

CHAPTER 5

Compact DC Model

The direct current (DC) in the DG TFET between the source and drain contact (see Fig. 5.1) is composed of the B2B tunneling and the TAT effect. For this reason, it is required to have an accurate and simultaneously a numerically efficient electrostatic potential solution, which is introduced in Sec. 5.1. The compact potential solution is used to estimate the device band diagram in Sec. 5.2. Based on the potential solution, a compact expression for the electric field is derived in Sec. 5.3. A compact description of the B2B tunneling current density is detailed in Sec. 5.4, where an expression for the TAT current density is introduced in Sec. 5.5. Finally, the total tunneling current of the DG TFET is presented in Sec. 5.6.

All derived compact model equations are in closed-form and are suitable for an implementation in the hardware description language Verilog-A. Altogether, this chapter connects all single modeling parts that has been published in [133, 135–137, 169].

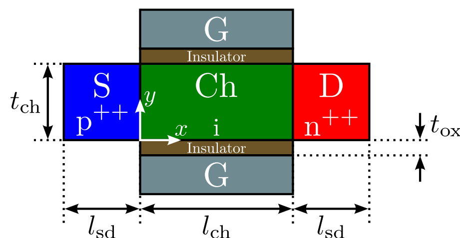


Figure 5.1.: 2D sketch of the n-type DG TFET device geometry, showing the channel thickness t_{ch}, the channel length l_{ch}, the gate oxide thickness t_{ox} and the length of the S/D region l_{sd}. Source (S) and drain (D) region are highly p/n-doped with a doping concentration $N_{s/d}$.

5.1 Compact Electrostatic Potential Solution

The compact electrostatic potential solution of the DG TFET device is introduced in the following. Compact expressions are derived separately for the S, D and Ch region, whereby the channel potential is divided in an expression which characterizes the source-to-channel junction

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(ON-state) and an expression to define the AMBIPOLAR-state addressed at the drain-to-channel junction. A schematic potential shape along the x-axis is depicted in Fig. 5.2. The ON- and the

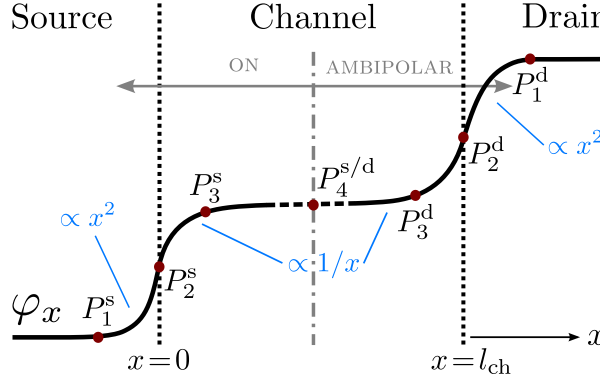


Figure 5.2.: Schematic electrostatic potential φ_x of the DG TFET along the x-axis for an arbitrary y-position. The compact potential within S and D region is characterized by a parabolic function ($\propto x^2$). A compact expression to define the potential within Ch region is found by a rational function $\propto 1/x$. The compact potential expressions are derived by applying the characteristic points $P_i^{\mathrm{s/d}}$.

AMBIPOLAR-state compact potential are modeled separately. The expressions are based on the characteristic potential points $P_i^{\mathrm{s/d}}$ (see Fig. 5.2), which are calculated by the 2D electrostatic potential solution presented in Chap. 4. For a Verilog-A implementation of this 2D complex potential solution, it is necessary to separate the real and imaginary part, since Verilog-A is not able to handle complex values. The separation of the complex electrostatic solution is detailed in App. A.

In the calculations of the compact electric field it is necessary to include the y component of the potential. For this reason, a compact modeling approach of the potential along the y-axis is introduced in Sec. 5.1.3.

5.1.1 ON-State Compact Potential

The main part of tunneling in the ON-state occurs at the source-to-channel junction and therefore, the compact electrostatic potential along the x-axis for any y-position is characterized within two separate intervals. In the first interval the source potential is approximated and in the second one the potential in the channel is defined, which are derived in the following.

Source Potential

The potential in the S region can be described in the interval $[-x_1^{\mathrm{s}}(y) \leq x < 0\,\mathrm{nm}]$ by a parabola as follows:

$$\varphi_x^{\mathrm{s}}(x,y) = a_{\mathrm{s}}(y) \cdot x^2 + b_{\mathrm{s}}(y) \cdot x + c_{\mathrm{s}}(y). \tag{5.1}$$

The unknown parameters a_s, b_s and c_s are determined with the help of the potential points P_1^s and P_2^s (see Fig. 5.2) and the first derivative at P_1^s, which read as:

$$P_1^\mathrm{s}(y) = \left(x_1^\mathrm{s}(y),\ \Phi_\mathrm{bi}^\mathrm{s}\right), \tag{5.2}$$

$$P_2^\mathrm{s}(y) = \left(x_2^\mathrm{s},\ \Phi_\mathrm{bi,eff}^\mathrm{s}(y)\right), \tag{5.3}$$

$$\frac{\mathrm{d}\varphi_x^\mathrm{s}\left(x_1^\mathrm{s}(y)\right)}{\mathrm{d}x} = 0, \tag{5.4}$$

whereby x_2^s describes the x-position of the source-to-channel junction and is therefore set to zero. The x-value x_1^s characterizes the x-position, where the potential bending equals zero [128]:

$$x_1^\mathrm{s}(y) = \lambda_\mathrm{s}(y) - \sqrt{\lambda_\mathrm{s}^2(y) \pm \frac{2 \cdot \varepsilon_\mathrm{s} \cdot (\Phi_\mathrm{bi}^\mathrm{s} + V_\mathrm{s} - V_\mathrm{gs,eff})}{q \cdot N_\mathrm{s}}}, \tag{5.5}$$

using the screening length λ_s at the source-to-channel junction (see Eq. (4.29)), the source built-in potential $\Phi_\mathrm{bi}^\mathrm{s}$, the permittivity ε_s in S, the source voltage V_s, the doping concentration N_s in S region and the effective gate-source voltage $V_\mathrm{gs,eff}$. To ensure only positive values in the argument of the square root, the sign in front of the fraction within the square root is positive if $(\Phi_\mathrm{bi}^\mathrm{s} + V_\mathrm{s}) > V_\mathrm{gs,eff}$ and negative for the other case.

By applying Eqs. (5.2)–(5.4), a linear equation system is set up to solve for the needed parameters $a_\mathrm{s}, b_\mathrm{s}$ and c_s:

$$\left| \begin{array}{rcccccc} \Phi_\mathrm{bi}^\mathrm{s} & = & a_\mathrm{s}(y) \cdot (x_1^\mathrm{s})^2 & + & b_\mathrm{s}(y) \cdot x_1^\mathrm{s} & + & c_\mathrm{s}(y) \\ \Phi_\mathrm{bi,eff}^\mathrm{s}(y) & = & a_\mathrm{s}(y) \cdot (x_2^\mathrm{s})^2 & + & b_\mathrm{s}(y) \cdot x_2^\mathrm{s} & + & c_\mathrm{s}(y) \\ 0 & = & 2 \cdot a_\mathrm{s}(y) \cdot x_1^\mathrm{s} & + & b_\mathrm{s}(y) & & \end{array} \right|. \tag{5.6}$$

Solving the linear equation system results in:

$$a_\mathrm{s}(y) = \frac{\Phi_\mathrm{bi,eff}^\mathrm{s}(y) - \Phi_\mathrm{bi}^\mathrm{s}}{\left(x_2^\mathrm{s} - x_1^\mathrm{s}(y)\right)^2}, \tag{5.7}$$

$$b_\mathrm{s}(y) = -\frac{2 \cdot x_1^\mathrm{s}(y) \cdot \left(\Phi_\mathrm{bi,eff}^\mathrm{s}(y) - \Phi_\mathrm{bi}^\mathrm{s}\right)}{\left(x_2^\mathrm{s} - x_1^\mathrm{s}(y)\right)^2}, \tag{5.8}$$

$$c_\mathrm{s}(y) = \Phi_\mathrm{bi}^\mathrm{s} + x_1^\mathrm{s}(y) \cdot \frac{\Phi_\mathrm{bi,eff}^\mathrm{s}(y) - \Phi_\mathrm{bi}^\mathrm{s}}{\left(x_2^\mathrm{s} - x_1^\mathrm{s}(y)\right)^2}. \tag{5.9}$$

Channel Potential (Source Related)

After investigating the potential shape in TCAD simulation results, the compact potential in the channel at the source-to-channel junction is approximated by a rational function. So, the potential in the interval $[0 \leq x \leq l_\mathrm{ch}/2]$ is defined by:

$$\varphi_x^\mathrm{ch,s}(x,y) = \frac{k_\mathrm{s}(y)}{x - l_\mathrm{s}(y)} + m_\mathrm{s}(y). \tag{5.10}$$

The three unknown parameters k_s, l_s and m_s are solved with the help of three characteristic potential points P_i^s in the first half of the channel. The points are chosen to be (see Fig. 5.2):

$$P_2^\mathrm{s}(y) = \left(x_2^\mathrm{s},\ \Phi_\mathrm{bi,eff}^\mathrm{s}(y)\right), \tag{5.11}$$

$$P_3^\mathrm{s}(y) = \left(x_3^\mathrm{s},\ \varphi_\mathrm{2D}^\mathrm{ch}(x_3^\mathrm{s}, y)\right), \tag{5.12}$$

$$P_4^\mathrm{s/d}(y) = \left(x_4^\mathrm{s/d},\ \varphi_\mathrm{2D}^\mathrm{ch}(x_4^\mathrm{s/d}, y)\right), \tag{5.13}$$

where $x_4^\mathrm{s/d}$ is set to $l_\mathrm{ch}/2$. In order to consider the influence of the gate insulator thickness t_ox and the channel length l_ch on the electrostatics, the x-value of P_3^s is empirically defined by:

$$x_3^\mathrm{s} = 2 \cdot t_\mathrm{ox} \cdot \left(\frac{l_\mathrm{ch}}{22\,\mathrm{nm}}\right)^3, \tag{5.14}$$

using a channel length of 22 nm as a reference. That means, for a smaller l_ch the value of x_3^s decreases to cover the potential drop at the source-to-channel junction. The potential values in P_3^s and $P_4^\mathrm{s/d}$ are calculated with the help of the 2D electrostatic potential solution (see Eq. (4.40)).

With the help of these three potential points the following linear equation system can be defined to solve for the unknown parameters:

$$\left|\begin{array}{rclcl} \Phi_\mathrm{bi,eff}^\mathrm{s}(y) & = & \frac{k_\mathrm{s}(y)}{x_2^\mathrm{s} - l_\mathrm{s}(y)} & + & m_\mathrm{s}(y) \\ \varphi_\mathrm{2D}^\mathrm{ch}(x_3^\mathrm{s}, y) & = & \frac{k_\mathrm{s}(y)}{x_3^\mathrm{s} - l_\mathrm{s}(y)} & + & m_\mathrm{s}(y) \\ \varphi_\mathrm{2D}^\mathrm{ch}(x_4^\mathrm{s/d}, y) & = & \frac{k_\mathrm{s}(y)}{x_4^\mathrm{s/d} - l_\mathrm{s}(y)} & + & m_\mathrm{s}(y) \end{array}\right|. \tag{5.15}$$

The first unknown parameter l_s results in:

$$l_\mathrm{s}(y) = -\frac{D_{13} \cdot \left(x_2^\mathrm{s} + x_4^\mathrm{s/d}\right) - D_{12} \cdot \left(x_2^\mathrm{s} + x_3^\mathrm{s}\right)}{2 \cdot (D_{12} - D_{13})} \pm \sqrt{\left(-\frac{D_{13} \cdot \left(x_2^\mathrm{s} + x_4^\mathrm{s/d}\right) - D_{12} \cdot \left(x_2^\mathrm{s} + x_3^\mathrm{s}\right)}{2 \cdot (D_{12} - D_{13})}\right)^2 - x_2^\mathrm{s} \cdot \frac{D_{12} \cdot x_3^\mathrm{s} - D_{13} \cdot x_4^\mathrm{s/d}}{D_{12} - D_{13}}}, \tag{5.16}$$

with:

$$D_{12}(y) = \frac{\varphi_\mathrm{2D}^\mathrm{ch}(x_3^\mathrm{s}, y) - \Phi_\mathrm{bi,eff}^\mathrm{s}(y)}{x_2^\mathrm{s} - x_3^\mathrm{s}}, \quad D_{13}(y) = \frac{\varphi_\mathrm{2D}^\mathrm{ch}(x_4^\mathrm{s/d}, y) - \Phi_\mathrm{bi,eff}^\mathrm{s}(y)}{x_2^\mathrm{s} - x_4^\mathrm{s/d}}. \tag{5.17}$$

It should be noted that the parameter l_s must be negative and therefore, the sign of the square root in Eq. (5.16) must also be negative. The y-dependency of l_s is obtained by the y-dependency of the potential values considered in D_{12} and D_{13}. Now, solving for the next unknown parameter yields:

$$k_\mathrm{s}(y) = \frac{\varphi_\mathrm{2D}^\mathrm{ch}(x_3^\mathrm{s}, y) - \Phi_\mathrm{bi,eff}^\mathrm{s}(y)}{\frac{1}{x_3^\mathrm{s} - l_\mathrm{s}(y)} - \frac{1}{x_2^\mathrm{s} - l_\mathrm{s}(y)}} \tag{5.18}$$

and the last one is given by:

$$m_{\mathrm{s}}(y) = \Phi^{\mathrm{s}}_{\mathrm{bi,eff}}(y) - \frac{k_{\mathrm{s}}(y)}{x^{\mathrm{s}}_{2} - l_{\mathrm{s}}(y)}. \tag{5.19}$$

Now, the compact potential solution at the source-to-channel junction can be calculated in dependency of x and y and the applied bias V_{gs} and V_{ds}.

5.1.2 AMBIPOLAR-State Compact Potential

In contrast to the ON-state, the tunneling events in the AMBIPOLAR-state occur at the drain-to-channel junction. For this reason, the electrostatic potential along the x-axis for an arbitrary y-position is characterized by an approximation in the drain region and one in the channel region. These approximations are done in the same way as in the ON-state and are introduced in the following.

Drain Potential

The electrostatic potential in the D region follows approximately a parabolic shape and therefore the potential in the interval $[l_{\mathrm{ch}} < x \leq x^{\mathrm{d}}_{1}(y)]$ is defined as:

$$\varphi^{\mathrm{d}}_{x}(x,y) = a_{\mathrm{d}}(y) \cdot x^{2} + b_{\mathrm{d}}(y) \cdot x + c_{\mathrm{d}}(y), \tag{5.20}$$

where x^{d}_{1} defines the x-position at which the potential bending equals zero [128]:

$$x^{\mathrm{d}}_{1}(y) = l_{\mathrm{ch}} - \lambda_{\mathrm{d}}(y) + \sqrt{\lambda^{2}_{\mathrm{d}}(y) \pm \frac{2 \cdot \varepsilon_{\mathrm{d}} \cdot (\Phi^{\mathrm{d}}_{\mathrm{bi}} + V_{\mathrm{ds}} - V_{\mathrm{gs,eff}})}{q \cdot N_{\mathrm{d}}}}. \tag{5.21}$$

In this equation λ_{d} is the screening length at the drain-to-channel junction (see Eq. (4.29)), $\Phi^{\mathrm{d}}_{\mathrm{bi}}$ shows the built-in potential , N_{d} represents the doping concentration of the drain and ε_{d} is the dielectric permittivity of the D region. The sign before the fraction within the square root is positive for the case $(\Phi^{\mathrm{d}}_{\mathrm{bi}} + V_{\mathrm{ds}}) > V_{\mathrm{gs,eff}}$ and negative in the other case.

Similar to the source potential approximation, the unknown parameters a_{d}, b_{d} and c_{d} are specified by the potential points P^{d}_{1} and P^{d}_{2} as follows:

$$P^{\mathrm{d}}_{1} = \left(x^{\mathrm{d}}_{1}(y), \Phi^{\mathrm{d}}_{\mathrm{bi}}\right), \tag{5.22}$$

$$P^{\mathrm{d}}_{2} = \left(x^{\mathrm{d}}_{2}, \Phi^{\mathrm{d}}_{\mathrm{bi,eff}}(y)\right), \tag{5.23}$$

$$\frac{\mathrm{d}\varphi^{\mathrm{d}}_{x}\left(x^{\mathrm{d}}_{1}(y)\right)}{\mathrm{d}x} = 0. \tag{5.24}$$

The x-value x^{d}_{2} is located at the drain-to-channel junction and therefore is equal to the channel length l_{ch}.

With the help of these three boundary conditions, similar to Eq. (5.6) a linear equation

system is set up to determine the unknown parameters which results in:

$$a_{\mathrm{d}}(y) = \frac{\Phi_{\mathrm{bi,eff}}^{\mathrm{d}}(y) - \Phi_{\mathrm{bi}}^{\mathrm{d}}}{\left(x_2^{\mathrm{d}} - x_1^{\mathrm{d}}(y)\right)^2}, \tag{5.25}$$

$$b_{\mathrm{d}}(y) = -\frac{2 \cdot x_1^{\mathrm{d}}(y) \cdot \left(\Phi_{\mathrm{bi,eff}}^{\mathrm{d}}(y) - \Phi_{\mathrm{bi}}^{\mathrm{d}}\right)}{\left(x_2^{\mathrm{d}} - x_1^{\mathrm{d}}(y)\right)^2}, \tag{5.26}$$

$$c_{\mathrm{d}}(y) = \Phi_{\mathrm{bi}}^{\mathrm{d}} + x_1^{\mathrm{d}}(y) \cdot \frac{\Phi_{\mathrm{bi,eff}}^{\mathrm{d}}(y) - \Phi_{\mathrm{bi}}^{\mathrm{d}}}{\left(x_2^{\mathrm{d}} - x_1^{\mathrm{d}}(y)\right)^2}. \tag{5.27}$$

Channel Potential (Drain Related)

The channel potential for the AMBIPOLAR-state at the drain-to-channel junction in the interval $[{}^{l_{\mathrm{ch}}}/_2 < x \leq l_{\mathrm{ch}}]$ is approximated by a rational function ($\propto 1/x$) as it is shown in Fig. 5.2:

$$\varphi_x^{\mathrm{ch,d}}(x,y) = \frac{k_{\mathrm{d}}(y)}{x - l_{\mathrm{d}}(y)} + m_{\mathrm{d}}. \tag{5.28}$$

In order to solve the three unknown parameters k_{d}, l_{d} and m_{d}, three potential points P_i^{d} in the second half of the channel are applied, which are defined as follows:

$$P_2^{\mathrm{d}}(y) = \left(x_2^{\mathrm{d}}, \Phi_{\mathrm{bi,eff}}^{\mathrm{d}}(y)\right), \tag{5.29}$$

$$P_3^{\mathrm{d}}(y) = \left(x_3^{\mathrm{d}}, \varphi_{\mathrm{2D}}^{\mathrm{ch}}(x_3^{\mathrm{d}}, y)\right), \tag{5.30}$$

$$P_4^{\mathrm{s/d}}(y) = \left(x_4^{\mathrm{s/d}}, \varphi_{\mathrm{2D}}^{\mathrm{ch}}(x_2^{\mathrm{s/d}}, y)\right), \tag{5.31}$$

thereby x_3^{d} is defined by $l_{\mathrm{ch}} - x_3^{\mathrm{s}}$ (see Eq. (5.14)) and $x_4^{\mathrm{s/d}} = {}^{l_{\mathrm{ch}}}/_2$. The associated potential values of P_3^{d} and P_4^{d} are calculated in terms of the 2D electrostatic potential solution presented in Eq. (4.40).

A linear equation system is set up to determine the three unknown parameters in the same way as it is done in Eq. (5.15). The first unknown parameter is given by:

$$l_{\mathrm{d}}(y) = -\frac{D_{13} \cdot \left(x_2^{\mathrm{d}} + x_4^{\mathrm{s/d}}\right) - D_{12} \cdot \left(x_2^{\mathrm{d}} + x_3^{\mathrm{d}}\right)}{2 \cdot (D_{12} - D_{13})} \pm \sqrt{\left(-\frac{D_{13} \cdot \left(x_2^{\mathrm{d}} + x_4^{\mathrm{s/d}}\right) - D_{12} \cdot \left(x_2^{\mathrm{d}} + x_3^{\mathrm{d}}\right)}{2 \cdot (D_{12} - D_{13})}\right)^2 - x_2^{\mathrm{d}} \cdot \frac{D_{12} \cdot x_3^{\mathrm{d}} - D_{13} \cdot x_4^{\mathrm{s/d}}}{D_{12} - D_{13}}}, \tag{5.32}$$

using:

$$D_{12}(y) = \frac{\varphi_{\mathrm{2D}}^{\mathrm{ch}}(x_3^{\mathrm{d}}, y) - \Phi_{\mathrm{bi,eff}}^{\mathrm{d}}(y)}{x_2^{\mathrm{d}} - x_3^{\mathrm{d}}}, \quad D_{13}(y) = \frac{\varphi_{\mathrm{2D}}^{\mathrm{ch}}(x_4^{\mathrm{s/d}}, y) - \Phi_{\mathrm{bi,eff}}^{\mathrm{d}}(y)}{x_2^{\mathrm{d}} - x_4^{\mathrm{s/d}}}. \tag{5.33}$$

In this case, the parameter $l_{\mathrm{d}} > l_{\mathrm{ch}}$ and therefore the sign of the square root in Eq. (5.32) must

be positive. The next parameter is determined as follows:

$$k_{\mathrm{d}}(y) = \frac{\varphi_{\mathrm{2D}}^{\mathrm{ch}}(x_3^{\mathrm{d}}, y) - \Phi_{\mathrm{bi,eff}}^{\mathrm{d}}(y)}{\frac{1}{x_3^{\mathrm{d}} - l_{\mathrm{d}}(y)} - \frac{1}{x_2^{\mathrm{d}} - l_{\mathrm{d}}(y)}}. \tag{5.34}$$

Solving for the last parameter results in:

$$m_{\mathrm{d}}(y) = \Phi_{\mathrm{bi,eff}}^{\mathrm{d}}(y) - \frac{k_{\mathrm{d}}(y)}{x_2^{\mathrm{d}} - l_{\mathrm{d}}(y)}. \tag{5.35}$$

5.1.3 Compact Potential Solution Along the y-Axis

A compact description of the potential along the y-axis is needed to find a compact expression for the electric field in y direction. The shape of the potential along the y-axis has been investigated in TCAD Sentaurus simulations at several x-positions. The results show that the potential in the ON-state is schematically shaped as it is shown in Fig. 5.3. The potential shape in the AMBIPOLAR-state looks similar to that in the ON-state, with the difference that in this case $\Phi_{\mathrm{sur}} < \Phi_{\mathrm{cen}}$. In the regime of V_{gs}-control, the surface potential or the effective gate-source voltage $V_{\mathrm{gs,eff}}$ is under the control of the applied gate-source voltage. In this state, the TFET channel is in depletion region and the potential along the y-axis follows nearly a parabolic shape ($\propto y^2$), as it is illustrated in terms of the black curve in Fig. 5.3. When inversion charges come into play, the shape of the potential changes. The potential at the surface as well as the gradient around the surface increases. The center potential stays constant and the slope around the center potential decreases.

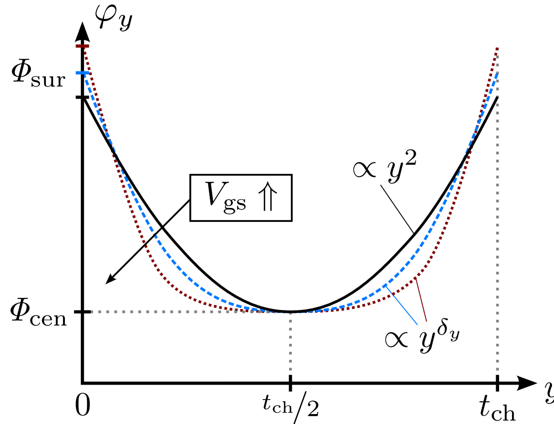


Figure 5.3.: Sketch of the potential shape φ_y along the y-axis showing the influence of an increasing V_{gs} and therefore the existence of inversion charges on the curve shape of φ_y. In depletion region (black solid line) the potential follows nearly a parabola. In inversion mode (blue and red dashed lines) the potential is proportional to y^{δ_y}.

The influence of inversion charges on the potential shape is modeled by the following

expression:

$$\varphi_y^{\mathrm{s/d}}(x,y) = \frac{\Phi_{\mathrm{sur}}^{\mathrm{s/d}}(x) - \Phi_{\mathrm{cen}}^{\mathrm{s/d}}(x)}{\left({}^{t_{\mathrm{ch}}}/_{2}\right)^{\delta_y}} \cdot \left(y - {}^{t_{\mathrm{ch}}}/_{2}\right)^{\delta_y} + \Phi_{\mathrm{cen}}^{\mathrm{s/d}}(x), \tag{5.36}$$

in which the potential values $\Phi_{\mathrm{sur}}^{\mathrm{s/d}}$ and $\Phi_{\mathrm{cen}}^{\mathrm{s/d}}$ are respectively calculated for a specific x-position at the channel surface ($y = 0\,\mathrm{nm}$) and center ($y = {}^{t_{\mathrm{ch}}}/_{2}$), using the compact potential expressions derived in Sec. 5.1. The exponent in Eq. (5.36) takes empirically into account the influence of inversion charges on the potential shape and is defined by:

$$\delta_y = 2 + \frac{2 \cdot (V_{\mathrm{gs}} - V_{\mathrm{gs,eff}})}{1\,\mathrm{V}}. \tag{5.37}$$

In this equation, when inversion charges come into play, the difference between the applied gate-source voltage V_{gs} and the effective gate-source voltage $V_{\mathrm{gs,eff}}$ increases and hence, the exponent δ_y also increases and the resulting potential tends the expected curve shape.

5.2 Compact Band Diagram

In order to derive the tunneling probability T_{tun}, a compact description of the device band diagram is necessary. The calculation of the band diagram is based on the compact potential solution φ_x (see Sec. 5.1) and the material parameters electron affinity χ and band gap E_{g}. It should be noticed that due to the high doping concentration of S/D, the effect of band gap narrowing (BGN) has to be taken into account. A schematic band diagram of the DG TFET along the x-axis is depicted in Fig. 5.4. The band diagram including the consideration of hetero-junctions is calculated as follows:

$$E_{\mathrm{c}}^{\mathrm{s}}(x,y) = -q \cdot \varphi_x^{\mathrm{s}}(x,y) + \frac{E_{\mathrm{g}}^{\mathrm{s}}}{2}, \tag{5.38}$$

$$E_{\mathrm{v}}^{\mathrm{s}}(x,y) = -q \cdot \varphi_x^{\mathrm{s}}(x,y) - \frac{E_{\mathrm{g}}^{\mathrm{s}}}{2}, \tag{5.39}$$

$$E_{\mathrm{c}}^{\mathrm{ch,s}}(x,y) = -q \cdot \varphi_x^{\mathrm{ch,s}}(x,y) + \chi_{\mathrm{s}} - \chi_{\mathrm{ch}} + \frac{E_{\mathrm{g}}^{\mathrm{ch}}}{2}, \tag{5.40}$$

$$E_{\mathrm{v}}^{\mathrm{ch,s}}(x,y) = -q \cdot \varphi_x^{\mathrm{ch,s}}(x,y) + \chi_{\mathrm{s}} - \chi_{\mathrm{ch}} - \frac{E_{\mathrm{g}}^{\mathrm{ch}}}{2}, \tag{5.41}$$

$$E_{\mathrm{c}}^{\mathrm{ch,d}}(x,y) = -q \cdot \varphi_x^{\mathrm{ch,d}}(x,y) + \chi_{\mathrm{s}} - \chi_{\mathrm{ch}} + \frac{E_{\mathrm{g}}^{\mathrm{ch}}}{2}, \tag{5.42}$$

$$E_{\mathrm{v}}^{\mathrm{ch,d}}(x,y) = -q \cdot \varphi_x^{\mathrm{ch,d}}(x,y) + \chi_{\mathrm{s}} - \chi_{\mathrm{ch}} - \frac{E_{\mathrm{g}}^{\mathrm{ch}}}{2}, \tag{5.43}$$

$$E_{\mathrm{c}}^{\mathrm{d}}(x,y) = -q \cdot \varphi_x^{\mathrm{d}}(x,y) + \chi_{\mathrm{s}} - \chi_{\mathrm{d}} + \frac{E_{\mathrm{g}}^{\mathrm{d}}}{2}, \tag{5.44}$$

$$E_{\mathrm{c}}^{\mathrm{d}}(x,y) = -q \cdot \varphi_x^{\mathrm{d}}(x,y) + \chi_{\mathrm{s}} - \chi_{\mathrm{d}} - \frac{E_{\mathrm{g}}^{\mathrm{d}}}{2}, \tag{5.45}$$

with the electron affinity in source χ_{s}, in the channel χ_{ch} and in drain χ_{d}. The band gap considering BGN in source $E_{\mathrm{g}}^{\mathrm{s}}$, channel $E_{\mathrm{g}}^{\mathrm{ch}}$ and drain region $E_{\mathrm{g}}^{\mathrm{d}}$.

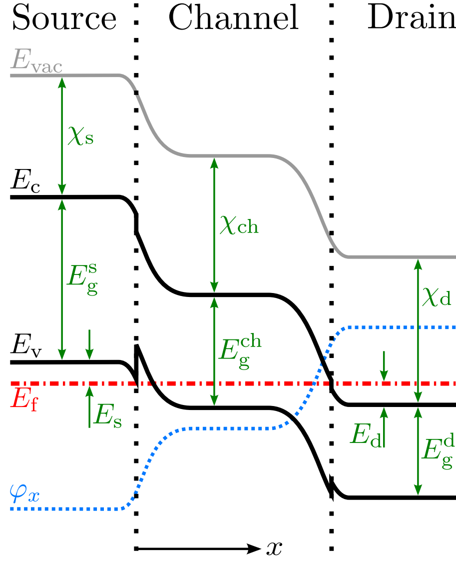


Figure 5.4.: Schematic band diagram of the n-type DG TFET along the x-axis for an arbitrary y-position, which is based on the compact potential solution φ_x. The plot shows the Fermi energy E_{f}, the ConB E_{c}, the ValB E_{v} and the device material parameters. The kink at the source-to-channel junction indicates a hetero-junction.

The BGN effect in the p-doped S region is considered in terms of the model of Slotboom [170], which characterizes the band gap reduction in dependency of the acceptor (source) doping concentration N_{s}. For the band gap in source follows:

$$E_{\mathrm{g}}^{\mathrm{s}} = E_{\mathrm{g}}^{\mathrm{s},0} - \Delta E_{\mathrm{g}}^{\mathrm{s},0}, \tag{5.46}$$

with the intrinsic band gap of source $E_{\mathrm{g}}^{\mathrm{s},0}$ at the considered temperature T and:

$$\Delta E_{\mathrm{g}}^{\mathrm{s},0} = 6.72 \cdot 10^{-3}\mathrm{eV} \cdot \left[\ln\left(\frac{N_{\mathrm{s}}}{1.3 \cdot 10^{17}\mathrm{cm}^{-3}} \right) + \sqrt{\left(\ln\left(\frac{N_{\mathrm{s}}}{1.3 \cdot 10^{17}\mathrm{cm}^{-3}} \right)\right)^2 + \frac{1}{2}} \right]. \tag{5.47}$$

Due to the high n-doping concentration N_{d}, the BGN effect in D region is calculated by the model of Del Alamo [171]:

$$E_{\mathrm{g}}^{\mathrm{d}} = E_{\mathrm{g}}^{\mathrm{d},0} - \Delta E_{\mathrm{g}}^{\mathrm{d},0}, \tag{5.48}$$

using the intrinsic band gap in D region $E_{\mathrm{g}}^{\mathrm{d},0}$ at the considered temperature T and the band gap difference, which is defined by:

$$\Delta E_{\mathrm{g}}^{\mathrm{d},0} = \begin{cases} 18.7 \cdot 10^{-3}\mathrm{eV} \cdot \ln\left(\frac{N_{\mathrm{d}}}{7.0 \cdot 10^{17}\mathrm{cm}^{-3}} \right) & , \quad N_{\mathrm{d}} \geq 7.0 \cdot 10^{17}\mathrm{cm}^{-3} \\ 0\,\mathrm{eV} & , \quad \text{otherwise}. \end{cases} \tag{5.49}$$

In the calculations of the built-in potentials $\Phi_{\mathrm{bi}}^{\mathrm{s/d}}$ (see Eq. (4.30)), it is important to know

the difference between the Fermi level and the ValB/ConB at the S/D edge. This energy difference is denoted as $E_{\mathrm{s/d}}$. Due to the high doping concentrations, the semiconductor is degenerated which needs to be taken into account. The values are extracted from TCAD Sentaurus simulation results for various doping concentrations $N_{\mathrm{s/d}}$ and are listed in Tab. 5.1.

Table 5.1.: Energy difference $E_{\mathrm{s/d}}$ in dependency of the doping concentration $N_{\mathrm{s/d}}$. $E_{\mathrm{s/d}}$ is applied in Eq. (4.30).

N_{s} [cm^{-3}] (p-type)	E_{s} [meV]	N_{d} [cm^{-3}] (n-type)	E_{d} [meV]
$1.0 \cdot 10^{19}$	−29.289	$1.0 \cdot 10^{19}$	−27.150
$3.0 \cdot 10^{19}$	−0.886	$3.0 \cdot 10^{19}$	1.253
$5.0 \cdot 10^{19}$	12.320	$5.0 \cdot 10^{19}$	14.459
$7.0 \cdot 10^{19}$	21.018	$7.0 \cdot 10^{19}$	23.157
$9.0 \cdot 10^{19}$	27.515	$9.0 \cdot 10^{19}$	29.654
$1.0 \cdot 10^{20}$	30.239	$1.0 \cdot 10^{20}$	32.378
$1.1 \cdot 10^{20}$	32.703	$1.1 \cdot 10^{20}$	34.842
$1.2 \cdot 10^{20}$	34.952	$1.2 \cdot 10^{20}$	37.091
$1.5 \cdot 10^{20}$	40.721	$1.5 \cdot 10^{20}$	42.860

5.3 Compact Electric Field Solution

The compact electric field solution which is introduced in the following, is based on the potential solution presented in Sec. 5.1. The electric field is needed in the calculations of the tunneling current density, which is defined within the channel region $[0 \leq x \leq l_{\mathrm{ch}}]$ and therefore, the electric field is also defined in this interval. By taking advantage of the electrostatic potential solution in the channel along the x-axis (see Eq. (5.10) and (5.28)), the x component of the electric field reads as:

$$E_x^{\mathrm{s/d}}(x,y) = -\frac{\mathrm{d}\,\varphi_x^{\mathrm{ch,s/d}}(x,y)}{\mathrm{d}x} = -\frac{\mathrm{d}}{\mathrm{d}x}\left(\frac{k_{\mathrm{s/d}}(y)}{x - l_{\mathrm{s/d}}(y)} + m_{\mathrm{s/d}}(y)\right) = -\frac{k_{\mathrm{s/d}}(y)}{\left(x - l_{\mathrm{s/d}}(y)\right)^2}. \tag{5.50}$$

The y component of the electric field is obtained by deriving Eq. (5.36), which results in:

$$\begin{aligned} E_y^{\mathrm{s/d}}(x,y) &= -\frac{\mathrm{d}\,\varphi_y^{\mathrm{s/d}}(x,y)}{\mathrm{d}y} = -\frac{\mathrm{d}}{\mathrm{d}y}\left(\frac{\Phi_{\mathrm{sur}}^{\mathrm{s/d}}(x) - \Phi_{\mathrm{cen}}^{\mathrm{s/d}}(x)}{({}^{t_{\mathrm{ch}}}/_2)^{\delta_y}} \cdot (y - {}^{t_{\mathrm{ch}}}/_2)^{\delta_y} + \Phi_{\mathrm{cen}}^{\mathrm{s/d}}(x)\right) \\ &= -\frac{\Phi_{\mathrm{sur}}^{\mathrm{s/d}}(x) - \Phi_{\mathrm{cen}}^{\mathrm{s/d}}(x)}{({}^{t_{\mathrm{ch}}}/_2)^{\delta_y}} \cdot \delta_y \cdot \left(|y - {}^{t_{\mathrm{ch}}}/_2|\right)^{\delta_y - 1}, \end{aligned} \tag{5.51}$$

with the surface potential Φ_{sur} and center potential Φ_{cen} at the considered x-position, calculated separately for the ON- and AMBIPOLAR-state with the help of Eq. (5.10) and (5.28).

The absolute value of the electric field, considering the x and y component, is calculated as follows:

$$|\vec{E}^{\mathrm{s/d}}(x,y)| = \sqrt{\left(E_x^{\mathrm{s/d}}\right)^2 + \left(E_y^{\mathrm{s/d}}\right)^2}. \tag{5.52}$$

5.4 Band-to-Band Tunneling Current Density

The B2B tunneling current density along the transversal energy component E_x can be expressed in terms of the Tsu-Esaki formula [94, 153], which was originally proposed by Duke [95]. It follows from Eq. (3.48):

$$J_{\text{tun}}(E_x) = \frac{q \cdot m^*}{2\pi^2 \cdot \hbar^3} \cdot \int_{E_{\text{min}}}^{E_{\text{max}}} T_{\text{tun}}(E_x) \cdot \mathcal{N}(E_x)\, \mathrm{d}E_x. \tag{5.53}$$

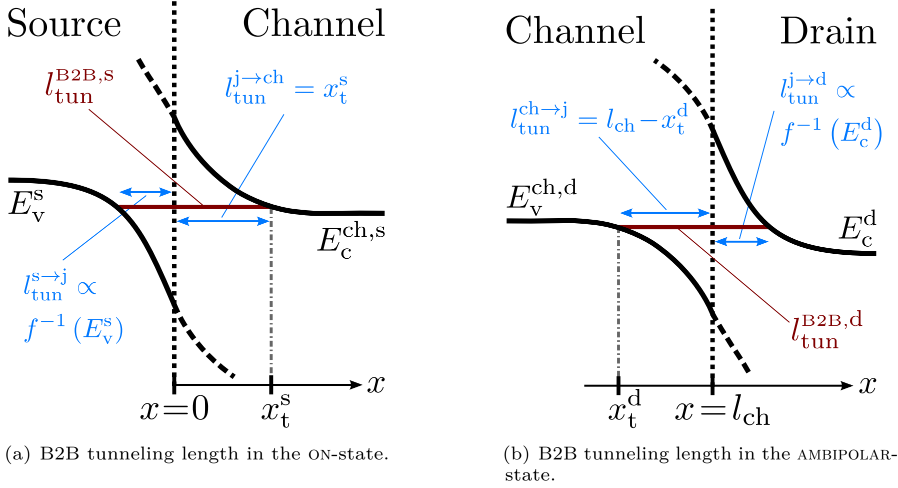
Since the calculations of the electrostatics are derived in dependency of x and y, the integration over energy E_x in Eq. (5.53), which indicates the energy shape in x direction, is replaced by an integration along the x-axis. The current density is rewritten as follows:

$$\begin{aligned} J_{\text{tun}}(E_x) &= q \cdot \int_{E_{\text{min}}}^{E_{\text{max}}} \frac{m^*}{2\pi^2 \cdot \hbar^3} \cdot T_{\text{tun}}(E_x) \cdot \mathcal{N}(E_x)\, \mathrm{d}E_x \cdot \frac{\mathrm{d}x}{\mathrm{d}x} \\ &= q \cdot \int_{x_1}^{x_2} \frac{m^*}{2\pi^2 \cdot \hbar^3} \cdot T_{\text{tun}}\big(E(x,y)\big) \cdot \mathcal{N}\big(E(x,y)\big) \cdot \frac{\mathrm{d}E_x}{\mathrm{d}x}\, \mathrm{d}x, \quad \text{with: } \frac{\mathrm{d}E_x}{\mathrm{d}x} = -q \cdot \frac{\mathrm{d}\varphi}{\mathrm{d}x} = q \cdot |\vec{E}^{\text{s/d}}| \\ J_{\text{tun}}(y) &= q \cdot \int_{x_1}^{x_2} \frac{m^*}{2\pi^2 \cdot \hbar^3} \cdot T_{\text{tun}}\big(E(x,y)\big) \cdot \mathcal{N}\big(E(x,y)\big) \cdot q \cdot |\vec{E}^{\text{s/d}}(x,y)|\, \mathrm{d}x, \end{aligned} \tag{5.54}$$

whereby the integration limits $x_1(E_{\text{min}})$ and $x_2(E_{\text{max}})$ substitute the minimum and maximum energy E_{min} and E_{max}, respectively. The electric field $|\vec{E}^{\text{s/d}}|$ is calculated with the help of Eq. (5.52). The expression $\mathcal{N}$ defines the supply function (see Eq. (3.49)), whereby a compact expression for the tunneling probability T_{tun} is derived in the following. Both expressions are now dependent on the band diagram, which is on the other hand dependent on specific x and y coordinates.

5.4.1 Tunneling Length (B2B)

In order to estimate the B2B tunneling probability $T_{\text{tun}}^{\text{B2B}}$, it is essential to know the tunneling length l_{tun} in the ON- and the AMBIPOLAR-state of the DG TFET. The estimation of the tunneling length is done in terms of the device band diagram as it is depicted in Fig. 5.5. The tunneling length represents the distance between the overlapping energy bands at one specific x-position. The derivation of $l_{\text{tun}}^{\text{B2B}}$ is separately presented for the ON-state and the AMBIPOLAR-state in the following.



(a) B2B tunneling length in the ON-state.

(b) B2B tunneling length in the AMBIPOLAR-state.

Figure 5.5.: Schematic band diagram of (a) source-to-channel junction (ON-state) showing the B2B tunneling length $l_{\text{tun}}^{\text{B2B,s}}$ and (b) the drain-to-channel junction to illustrate the B2B tunneling length $l_{\text{tun}}^{\text{B2B,d}}$ in the AMBIPOLAR-state.

On-State

The tunneling length in the ON-state of the device, which is located at the source-to-channel junction, consists of two parts as it is shown in Fig. 5.5(a). The tunneling length is derived at a specific x-position x_{t}^{s}, on which the tunneling event takes place. The first part describes the distance from the ValB in source, which is on the same energy level as the ConB in the channel, to source-to-channel junction. By forming the inverse function of E_{v}^{s} one obtains:

$$x(E_{\text{v}}^{\text{s}}) = f^{-1}\left(E_{\text{v}}^{\text{s}}\right) = f^{-1}\left(-q \cdot \varphi_x^{\text{s}}(x,y) - \frac{E_{\text{g}}^{\text{s}}}{2}\right) = f^{-1}\left(-q \cdot \left(a_{\text{s}} \cdot x^2 + b_{\text{s}} \cdot x + c_{\text{s}}\right) - \frac{E_{\text{g}}^{\text{s}}}{2}\right)$$
$$= -\frac{b_{\text{s}}}{2a_{\text{s}}} \pm \sqrt{\frac{1}{a_{\text{s}}} \cdot \left(-\frac{E_{\text{v}}^{\text{s}}}{q} + \frac{b_{\text{s}}^2}{4a_{\text{s}}} - c_{\text{s}} - \frac{E_{\text{g}}^{\text{s}}}{2q}\right)}. \tag{5.55}$$

The first part of $l_{\text{tun}}^{\text{B2B,s}}$ is given by assuming $E_{\text{v}}^{\text{s}} = E_{\text{c}}^{\text{ch,s}}(x_{\text{t}}^{\text{s}})$. It follows:

$$l_{\text{tun}}^{\text{s}\to\text{j}}(x_{\text{t}}^{\text{s}},y) = -\frac{b_{\text{s}}}{2a_{\text{s}}} + \sqrt{\frac{1}{a_{\text{s}}} \cdot \left(-\frac{E_{\text{c}}^{\text{ch,s}}(x_{\text{t}}^{\text{s}})}{q} + \frac{b_{\text{s}}^2}{4a_{\text{s}}} - c_{\text{s}} - \frac{E_{\text{g}}^{\text{s}}}{2q}\right)} \tag{5.56}$$

and by applying Eq. (5.40) together with Eq. (5.10) yields:

$$l_{\mathrm{tun}}^{\mathrm{s}\to\mathrm{j}}(x_{\mathrm{t}}^{\mathrm{s}},y) = -\frac{b_{\mathrm{s}}}{2a_{\mathrm{s}}} + \sqrt{\frac{1}{a_{\mathrm{s}}}\cdot\left(\frac{k_{\mathrm{s}}}{x_{\mathrm{t}}^{\mathrm{s}}-l_{\mathrm{s}}} + m_{\mathrm{s}} + \underbrace{\frac{b_{\mathrm{s}}^2}{4a_{\mathrm{s}}} - c_{\mathrm{s}} + \frac{\chi_{\mathrm{ch}}-\chi_{\mathrm{s}}}{q} - \frac{E_{\mathrm{g}}^{\mathrm{ch}}+E_{\mathrm{g}}^{\mathrm{s}}}{2q}}_{K_1^{\mathrm{s}}}\right)}$$

$$= -\frac{b_{\mathrm{s}}}{2a_{\mathrm{s}}} + \sqrt{\frac{1}{a_{\mathrm{s}}}\cdot\left(\frac{k_{\mathrm{s}}}{x_{\mathrm{t}}^{\mathrm{s}}-l_{\mathrm{s}}} + m_{\mathrm{s}} + K_1^{\mathrm{s}}\right)}, \tag{5.57}$$

whereby the needed distance is contained in the positive square root and $x_{\mathrm{t}}^{\mathrm{s}} \in \{0 \ldots {}^{l_{\mathrm{ch}}}/_{2}\}$.

The second part of the tunneling length at the source-to-channel junction is defined by the specific x-position $x_{\mathrm{t}}^{\mathrm{s}}$ since it refers to the distance from the origin to the chosen position. The second term is given by:

$$l_{\mathrm{tun}}^{\mathrm{j}\to\mathrm{ch}}(x_{\mathrm{t}}^{\mathrm{s}}) = x_{\mathrm{t}}^{\mathrm{s}}. \tag{5.58}$$

By adding these two values and considering an arbitrary x-value as $x_{\mathrm{t}}^{\mathrm{s}}$ one receives a closed-form expression, which describes the resulting tunneling length in the ON-state:

$$l_{\mathrm{tun}}^{\mathrm{B2B,s}}(x,y) = -l_{\mathrm{tun}}^{\mathrm{s}\to\mathrm{j}}(x,y) + l_{\mathrm{tun}}^{\mathrm{j}\to\mathrm{ch}}(x)$$

$$= x + \frac{b_{\mathrm{s}}}{2a_{\mathrm{s}}} - \sqrt{\frac{1}{a_{\mathrm{s}}}\cdot\left(\frac{k_{\mathrm{s}}}{x-l_{\mathrm{s}}} + m_{\mathrm{s}} + K_1^{\mathrm{s}}\right)}, \tag{5.59}$$

here it should be noted that the first part is negated to obtain a positive tunneling distance. The reason for that is that Eq. (5.57) defines the x-value at the ValB edge and is always negative.

AMBIPOLAR-State

The tunneling length at the drain-to-channel junction is derived in a similar way as $l_{\mathrm{tun}}^{\mathrm{B2B,s}}$ in the ON-state. Figure 5.5(b) illustrates a sketch of the band diagram at the considered junction showing the tunneling length $l_{\mathrm{tun}}^{\mathrm{B2B,d}}$. It also consists of two parts, the distance between the ConB in D region and the junction ($x = l_{\mathrm{ch}}$) and the distance between the junction and the ValB in the channel.

The first tunneling length part is derived by finding the inverse function of the ConB in D region:

$$x(E_{\mathrm{c}}^{\mathrm{d}}) = f^{-1}\left(E_{\mathrm{c}}^{\mathrm{d}}\right) = f^{-1}\left(-q\cdot\varphi_x^{\mathrm{d}}(x,y) + \frac{E_{\mathrm{g}}^{\mathrm{d}}}{2} + \chi_{\mathrm{s}} - \chi_{\mathrm{d}}\right)$$

$$= f^{-1}\left(-q\cdot(a_{\mathrm{d}}\cdot x^2 + b_{\mathrm{d}}\cdot x + c_{\mathrm{d}}) + \frac{E_{\mathrm{g}}^{\mathrm{d}}}{2} + \chi_{\mathrm{s}} - \chi_{\mathrm{d}}\right)$$

$$= -\frac{b_{\mathrm{d}}}{2a_{\mathrm{d}}} \pm \sqrt{\frac{1}{a_{\mathrm{d}}}\cdot\left(-\frac{E_{\mathrm{c}}^{\mathrm{d}}}{q} + \frac{b_{\mathrm{d}}^2}{4a_{\mathrm{d}}} - c_{\mathrm{d}} + \frac{E_{\mathrm{g}}^{\mathrm{d}}}{2q} + \frac{\chi_{\mathrm{s}}-\chi_{\mathrm{d}}}{q}\right)} \tag{5.60}$$

and assuming an equal energy level ($E_{\mathrm{c}}^{\mathrm{d}} = E_{\mathrm{v}}^{\mathrm{ch}}(x_{\mathrm{t}}^{\mathrm{d}})$) at the specific x-position $x_{\mathrm{t}}^{\mathrm{d}}$, where tunneling length is calculated, yields:

$$l_{\mathrm{tun}}^{\mathrm{j}\to\mathrm{d}}(x_{\mathrm{t}}^{\mathrm{d}},y) = -\frac{b_{\mathrm{d}}}{2a_{\mathrm{d}}} - \sqrt{\frac{1}{a_{\mathrm{d}}} \cdot \left(-\frac{E_{\mathrm{v}}^{\mathrm{ch}}(x_{\mathrm{t}}^{\mathrm{d}})}{q} + \frac{b_{\mathrm{d}}^2}{4a_{\mathrm{d}}} - c_{\mathrm{d}} + \frac{E_{\mathrm{g}}^{\mathrm{d}}}{2q} + \frac{\chi_{\mathrm{s}} - \chi_{\mathrm{d}}}{q}\right)} - l_{\mathrm{ch}}, \tag{5.61}$$

in which the required distance is obtained by using the negative square root and subtracting the channel length l_{ch}. Inserting Eq. (5.43) and (5.28) into Eq. (5.61) leads to the final expression:

$$\begin{aligned} l_{\mathrm{tun}}^{\mathrm{j}\to\mathrm{d}}(x_{\mathrm{t}}^{\mathrm{d}},y) &= -\frac{b_{\mathrm{d}}}{2a_{\mathrm{d}}} - \sqrt{\frac{1}{a_{\mathrm{d}}} \cdot \left(\frac{k_{\mathrm{d}}}{x_{\mathrm{t}}^{\mathrm{d}} - l_{\mathrm{d}}} + m_{\mathrm{d}} + \underbrace{\frac{b_{\mathrm{d}}^2}{4a_{\mathrm{d}}} - c_{\mathrm{d}} + \frac{\chi_{\mathrm{ch}} - \chi_{\mathrm{d}}}{q} + \frac{E_{\mathrm{g}}^{\mathrm{ch}} + E_{\mathrm{g}}^{\mathrm{d}}}{2q}}_{K_1^{\mathrm{d}}}\right)} - l_{\mathrm{ch}} \\ &= -\frac{b_{\mathrm{d}}}{2a_{\mathrm{d}}} - \sqrt{\frac{1}{a_{\mathrm{d}}} \cdot \left(\frac{k_{\mathrm{d}}}{x_{\mathrm{t}}^{\mathrm{d}} - l_{\mathrm{d}}} + m_{\mathrm{d}} + K_1^{\mathrm{d}}\right)} - l_{\mathrm{ch}}, \end{aligned} \tag{5.62}$$

with $x_{\mathrm{t}}^{\mathrm{d}} \in \{{}^{l_{\mathrm{ch}}}/_2 \ldots l_{\mathrm{ch}}\}$.

The second part of the tunneling length $l_{\mathrm{tun}}^{\mathrm{B2B,d}}$ at the drain-to-channel junction is given by the distance to the junction and the specific x-value $x_{\mathrm{t}}^{\mathrm{d}}$:

$$l_{\mathrm{tun}}^{\mathrm{ch}\to\mathrm{j}}(x_{\mathrm{t}}^{\mathrm{d}}) = l_{\mathrm{ch}} - x_{\mathrm{t}}^{\mathrm{d}}. \tag{5.63}$$

A summation of Eq. (5.62) and (5.63) and considering an arbitrary x-position lead to the final expression for the tunneling length in the AMBIPOLAR-state:

$$\begin{aligned} l_{\mathrm{tun}}^{\mathrm{B2B,d}}(x,y) &= l_{\mathrm{tun}}^{\mathrm{j}\to\mathrm{d}}(x,y) + l_{\mathrm{tun}}^{\mathrm{ch}\to\mathrm{j}}(x) \\ &= -x - \frac{b_{\mathrm{d}}}{2a_{\mathrm{d}}} - \sqrt{\frac{1}{a_{\mathrm{d}}} \cdot \left(\frac{k_{\mathrm{d}}}{x_{\mathrm{t}}^{\mathrm{d}} - l_{\mathrm{d}}} + m_{\mathrm{d}} + K_1^{\mathrm{d}}\right)}. \end{aligned} \tag{5.64}$$

5.4.2 Tunneling Probability (B2B)

The B2B tunneling probability is calculated with the help of an area-equivalent (AE) WKB approach, which has been proposed in [135, 136]. The main goal of this approach is to define the triangular energy barrier shape used in the WKB approximation with the help of an area equivalence of the triangle area and the area of the energy barrier formed by the band diagram. Looking back to Sec. 3.1.1, the general equation to calculate the transmission coefficient using the WKB is defined by (see Eq. (3.30)):

$$T_{\mathrm{tun}} \approx \exp\left(-2 \cdot \int_{x_1}^{x_2} \left|\sqrt{\frac{2 \cdot m^*}{\hbar^2} \cdot [U(x) - E]}\right| \mathrm{d}x\right). \tag{5.65}$$

In the following, the tunneling energy barrier shape $U(x)$, that defines the tunneling barrier of the DG TFET in the ON- and AMBIPOLAR-state, is expressed in terms of the area of the tunneling barrier. In addition, the term ($\propto \sqrt{U(x)}$) must be solvable in a closed-form to obtain a compact expression for the tunneling probability $T_{\mathrm{tun}}^{\mathrm{B2B}}$. Figure 5.6(a) illustrates a sketch of the band diagram at the source-to-channel junction showing the tunneling energy barrier at one specific x-position $x_{\mathrm{t}}^{\mathrm{s}}$ in the ON-state of the TFET. On the other hand the tunneling energy barrier at a chosen x-value $x_{\mathrm{t}}^{\mathrm{d}}$ in the AMBIPOLAR-state at the drain-to-channel junction is depicted in Fig. 5.6(b). In both cases the area of the tunneling barrier is highlighted by red solid lines (hatched areas A_1^{s} and A_1^{d}).

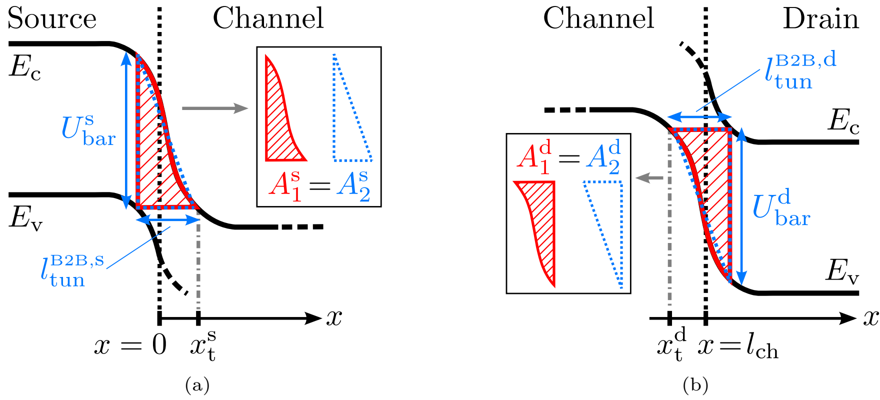


Figure 5.6.: Band diagram sketch of (a) the source-to-channel junction and (b) drain-to-channel junction, showing the shape of the tunneling barrier (red solid lines) of the DG TFET at $x = x_{\mathrm{t}}^{\mathrm{s/d}}$ for an arbitrary y-position. The enclosed area $A_1^{\mathrm{s/d}}$ (red hatched area) as well as the AE triangle (blue dashed area $A_2^{\mathrm{s/d}}$) with its energy barrier height $U_{\mathrm{bar}}^{\mathrm{s/d}}$ and the tunneling length $l_{\mathrm{tun}}^{\mathrm{B2B,s/d}}$ are illustrated for both cases.

In order to come to a numerically robust modeling approach, the energy barrier height $U_{\mathrm{bar}}^{\mathrm{s/d}}$ is calculated in terms of an AE derivation. In Fig. 5.6, it can be seen that the tunneling barrier (red hatched area $A_1^{\mathrm{s/d}}$), which is formed by the band diagram, equals the area of a triangle (blue dashed area $A_2^{\mathrm{s/d}}$). In the first step, the area of the energy triangle is described by:

$$A_2^{\mathrm{s/d}}(x,y) = \frac{U_{\mathrm{bar}}^{\mathrm{s/d}} \cdot l_{\mathrm{tun}}^{\mathrm{B2B,s/d}}(x,y)}{2}. \tag{5.66}$$

Now, assuming an area equivalence $A_1 = A_2$, the area $A_1^{\mathrm{s/d}}$ has to be determined in order to replace $A_2^{\mathrm{s/d}}$ in Eq. (5.66). The area A_1^{s} (see Fig. 5.6(a)) of the tunneling barrier in the

ON-state is formed by the ConB and is calculated by:

$$\begin{aligned} A_1^{\mathrm{s}}(E_\mathrm{c}) &= \int_{x_\mathrm{t}^\mathrm{s}-l_\mathrm{tun}^\mathrm{B2B,s}}^{x_\mathrm{t}^\mathrm{s}} \left(E_\mathrm{c}(x,y) - E_\mathrm{c}^\mathrm{ch,s}(x_\mathrm{t}^\mathrm{s},y)\right) \mathrm{d}x \\ &= \int_{x_\mathrm{t}^\mathrm{s}-l_\mathrm{tun}^\mathrm{B2B,s}}^{0} E_\mathrm{c}^\mathrm{s}(x,y)\,\mathrm{d}x + \int_{0}^{x_\mathrm{t}^\mathrm{s}} E_\mathrm{c}^\mathrm{ch,s}(x,y)\,\mathrm{d}x - \int_{x_\mathrm{t}^\mathrm{s}-l_\mathrm{tun}^\mathrm{B2B,s}}^{x_\mathrm{t}^\mathrm{s}} E_\mathrm{c}^\mathrm{ch,s}(x_\mathrm{t}^\mathrm{s},y)\,\mathrm{d}x, \end{aligned} \tag{5.67}$$

the $E_\mathrm{c}^\mathrm{ch,s}(x_\mathrm{t}^\mathrm{s},y)$ defines an ConB offset at the specific x-position x_t^s for a correct area calculation under the curves and to avoid negative area values. Inserting the compact band diagram expressions (see Eqs. (5.38) and (5.40)) in Eq. (5.67) leads to:

$$\begin{aligned} A_1^\mathrm{s}(x,y) =\ & q \cdot \left[\frac{a_\mathrm{s}}{3} \cdot \left(x_\mathrm{t}^\mathrm{s} - l_\mathrm{tun}^\mathrm{B2B,s}\right)^3 + \frac{b_\mathrm{s}}{2} \cdot \left(x_\mathrm{t}^\mathrm{s} - l_\mathrm{tun}^\mathrm{B2B,s}\right)^2 + \left(c_\mathrm{s} - \frac{E_\mathrm{g}^\mathrm{s}}{2q}\right) \cdot \left(x_\mathrm{t}^\mathrm{s} - l_\mathrm{tun}^\mathrm{B2B,s}\right)\right. \\ & \left. + k_\mathrm{s} \cdot \ln\left(\frac{l_\mathrm{s}}{l_\mathrm{s} - x_\mathrm{t}^\mathrm{s}}\right) + \left(-m_\mathrm{s} + \frac{E_\mathrm{g}^\mathrm{ch}}{2q} + \frac{\chi_\mathrm{s} - \chi_\mathrm{ch}}{q}\right) \cdot x_\mathrm{t}^\mathrm{s}\right] - E_\mathrm{c}^\mathrm{ch,s}(x_\mathrm{t}^\mathrm{s},y) \cdot l_\mathrm{tun}^\mathrm{B2B,s}, \end{aligned} \tag{5.68}$$

where the tunneling length is calculated with the help of Eq. (5.59).

The tunneling energy barrier in the AMBIPOLAR-state is formed by the ValB as it is shown in Fig. 5.6(b). The area A_2^d is defined by:

$$\begin{aligned} A_1^\mathrm{d}(E_\mathrm{v}) &= \int_{x_\mathrm{t}^\mathrm{d}}^{x_\mathrm{t}^\mathrm{d}+l_\mathrm{tun}^\mathrm{B2B,d}} \left(E_\mathrm{v}(x,y) - E_\mathrm{v}^\mathrm{ch,d}(x_\mathrm{t}^\mathrm{d},y)\right) \mathrm{d}x \\ &= \int_{x_\mathrm{t}^\mathrm{d}}^{l_\mathrm{ch}} E_\mathrm{v}^\mathrm{ch,d}(x,y)\,\mathrm{d}x + \int_{l_\mathrm{ch}}^{x_\mathrm{t}^\mathrm{d}+l_\mathrm{tun}^\mathrm{B2B,d}} E_\mathrm{v}^\mathrm{d}(x,y)\,\mathrm{d}x - \int_{x_\mathrm{t}^\mathrm{d}}^{x_\mathrm{t}^\mathrm{d}+l_\mathrm{tun}^\mathrm{B2B,d}} E_\mathrm{v}^\mathrm{ch,d}(x_\mathrm{t}^\mathrm{d},y)\,\mathrm{d}x. \end{aligned} \tag{5.69}$$

The last term $E_\mathrm{v}^\mathrm{ch,d}(x_\mathrm{t}^\mathrm{d},y)$ is used to compensate the ValB offset at the position x_t^d to obtain the correct tunneling area. Solving the integrals with the help of Eqs. (5.43) and (5.45) leads to:

$$\begin{aligned} A_1^\mathrm{d}(x,y) = q \cdot & \left[k_\mathrm{d} \cdot \ln\left(\frac{l_\mathrm{d} - x_\mathrm{t}^\mathrm{d}}{l_\mathrm{d} - l_\mathrm{ch}}\right) + \left(-m_\mathrm{d} - \frac{E_\mathrm{g}^\mathrm{ch}}{2q} + \frac{\chi_\mathrm{s} - \chi_\mathrm{ch}}{q}\right) \cdot \left(l_\mathrm{ch} - x_\mathrm{t}^\mathrm{d}\right)\right. \\ & + \frac{a_\mathrm{d}}{3} \cdot \left(l_\mathrm{ch}^3 - \left(x_\mathrm{t}^\mathrm{d} + l_\mathrm{tun}^\mathrm{B2B,d}\right)^3\right) + \frac{b_\mathrm{d}}{2} \cdot \left(l_\mathrm{ch}^2 - \left(x_\mathrm{t}^\mathrm{d} + l_\mathrm{tun}^\mathrm{B2B,d}\right)^2\right) \\ & \left. - \left(-c_\mathrm{d} + \frac{\chi_\mathrm{s} - \chi_\mathrm{d}}{q} - \frac{E_\mathrm{g}^\mathrm{d}}{2q}\right) \cdot \left(l_\mathrm{ch} - \left(x_\mathrm{t}^\mathrm{d} + l_\mathrm{tun}^\mathrm{B2B,d}\right)\right)\right] - E_\mathrm{v}^\mathrm{ch,d}(x_\mathrm{t}^\mathrm{d},y) \cdot l_\mathrm{tun}^\mathrm{B2B,d}. \end{aligned} \tag{5.70}$$

In order to calculate the tunneling length in the AMBIPOLAR-state, Eq. (5.64) is used. It should be noted that Eq. (5.70) results in a negative area and for this reason, the absolute value of A_1^{d} is used in the following to ensure the absolute value within the integral in Eq. (5.65).

With the help of the equal areas $|A_1^{\mathrm{s/d}}| = A_2^{\mathrm{s/d}}$ and by rearranging Eq. (5.66), the energy barrier height is determined as:

$$U_{\mathrm{bar}}^{\mathrm{s/d}}(x,y) = \frac{2 \cdot \left|A_1^{\mathrm{s/d}}(x,y)\right|}{l_{\mathrm{tun}}^{\mathrm{B2B,s/d}}(x,y)}. \tag{5.71}$$

In the next step, the energy barrier shape $U^{\mathrm{s/d}}(x,y)$ along the x-axis for an arbitrary y-position is defined by a linear function:

$$U^{\mathrm{s/d}}(x,y) = -\frac{U_{\mathrm{bar}}^{\mathrm{s/d}}(x,y)}{l_{\mathrm{tun}}^{\mathrm{B2B,s/d}}(x,y)} \cdot x + E_{\mathrm{c/v}}^{\mathrm{ch,s/d}}(x_{\mathrm{t}}^{\mathrm{s/d}},y), \tag{5.72}$$

with the term $E_{\mathrm{c/v}}^{\mathrm{ch,s/d}}$ that represents the energy offset at the position $x_{\mathrm{t}}^{\mathrm{s/d}}$.

The linear function in Eq. (5.72) is inserted in the general tunneling probability equation (see Eq. (5.65)). Now, the transmission coefficient is derived separately for the ON- and AMBIPOLAR-state. Firstly, for the ON-state follows:

$$\begin{aligned}
T_{\mathrm{tun}}^{\mathrm{B2B,s}}(x,y) &= \exp\left(-2 \cdot \int_{x_{\mathrm{t}}^{\mathrm{s}}-l_{\mathrm{tun}}^{\mathrm{B2B,s}}}^{x_{\mathrm{t}}^{\mathrm{s}}} \sqrt{\frac{2 \cdot m_{\mathrm{s}}^*}{\hbar^2} \cdot \left[\left(-\frac{U_{\mathrm{bar}}^{\mathrm{s}}(x,y)}{l_{\mathrm{tun}}^{\mathrm{B2B,s}}(x,y)} \cdot x + E_{\mathrm{c}}^{\mathrm{ch,s}}(x_{\mathrm{t}}^{\mathrm{s}},y)\right) - E_{\mathrm{c}}^{\mathrm{ch,s}}(x_{\mathrm{t}}^{\mathrm{s}},y)\right]}\, \mathrm{d}x\right) \\
&= \exp\left(-2 \cdot \sqrt{\frac{2 \cdot m_{\mathrm{s}}^*}{\hbar^2}} \cdot \left[\frac{2}{3} \cdot x \cdot \sqrt{-\frac{U_{\mathrm{bar}}^{\mathrm{s}}(x,y)}{l_{\mathrm{tun}}^{\mathrm{B2B,s}}(x,y)} \cdot x}\right]\Bigg|_{x_{\mathrm{t}}^{\mathrm{s}}-l_{\mathrm{tun}}^{\mathrm{B2B,s}}}^{x_{\mathrm{t}}^{\mathrm{s}}}\right) \\
&= \exp\left(-\frac{4}{3} \cdot \sqrt{\frac{2 \cdot m_{\mathrm{s}}^*}{\hbar^2} \cdot U_{\mathrm{bar}}^{\mathrm{s}}(x,y) \cdot l_{\mathrm{tun}}^{\mathrm{B2B,s}}(x,y)}\right),
\end{aligned} \tag{5.73}$$

the parameter m_{s}^* describes the effective carrier mass of the S region.

Similar to the ON-state expression, the AMBIPOLAR-state tunneling probability is calculated by using the parameters describing the drain-to-channel junction, which results in:

$$\begin{aligned}
T_{\mathrm{tun}}^{\mathrm{B2B,d}}(x,y) &= \exp\left(-2 \cdot \int_{x_{\mathrm{t}}^{\mathrm{d}}}^{x_{\mathrm{t}}^{\mathrm{d}}+l_{\mathrm{tun}}^{\mathrm{B2B,d}}} \sqrt{\frac{2 \cdot m_{\mathrm{d}}^*}{\hbar^2} \cdot \left[\left(-\frac{U_{\mathrm{bar}}^{\mathrm{d}}(x,y)}{l_{\mathrm{tun}}^{\mathrm{B2B,d}}(x,y)} \cdot x + E_{\mathrm{v}}^{\mathrm{ch,d}}(x_{\mathrm{t}}^{\mathrm{d}},y)\right) - E_{\mathrm{v}}^{\mathrm{ch,d}}(x_{\mathrm{t}}^{\mathrm{d}},y)\right]}\, \mathrm{d}x\right) \\
&= \exp\left(-2 \cdot \sqrt{\frac{2 \cdot m_{\mathrm{d}}^*}{\hbar^2}} \cdot \left[\frac{2}{3} \cdot x \cdot \sqrt{-\frac{U_{\mathrm{bar}}^{\mathrm{d}}(x,y)}{l_{\mathrm{tun}}^{\mathrm{B2B,d}}(x,y)} \cdot x}\right]\Bigg|_{x_{\mathrm{t}}^{\mathrm{d}}}^{x_{\mathrm{t}}^{\mathrm{d}}+l_{\mathrm{tun}}^{\mathrm{B2B,d}}}\right) \\
&= \exp\left(-\frac{4}{3} \cdot \sqrt{\frac{2 \cdot m_{\mathrm{d}}^*}{\hbar^2} \cdot U_{\mathrm{bar}}^{\mathrm{d}}(x,y) \cdot l_{\mathrm{tun}}^{\mathrm{B2B,d}}(x,y)}\right),
\end{aligned} \tag{5.74}$$

with the effective carrier mass m_{d}^{*} of the drain region.

5.4.3 Tunneling Generation Rate (B2B)

The tunneling generation rate (TGR) defines the number of carriers generated per second and per volume in the ConB (ON-state) or ValB (AMBIPOLAR-state) of the channel by tunneling. The TGR for B2B tunneling is defined by the terms within the integral of Eq. (5.54):

$$J_{\mathrm{tun,B2B}}^{\mathrm{s/d}}(y) = q \cdot \int_{x_{\mathrm{t},1}^{\mathrm{s/d}}}^{x_{\mathrm{t},2}^{\mathrm{s/d}}} \underbrace{\frac{m_{\mathrm{s/d}}^{*}}{2\pi^{2} \cdot \hbar^{3}} \cdot T_{\mathrm{tun}}^{\mathrm{B2B,s/d}}(x,y) \cdot \mathcal{N}_{\mathrm{B2B}}^{\mathrm{s/d}}(x,y) \cdot q \cdot |\vec{E}^{\mathrm{s/d}}(x,y)|}_{\mathrm{TGR}_{\mathrm{B2B}}^{\mathrm{s/d}}(x,y)} \,\mathrm{d}x. \tag{5.75}$$

In this equation, the tunneling probability for the ON- and AMBIPOLAR-state is calculated by using Eq. (5.73) and (5.74), respectively. The supply function $\mathcal{N}$ has already been introduced in Eq. (3.49) and by applying the compact band diagram expressions (see Sec. 5.2), the supply function for the ON- and AMBIPOLAR-state yields:

$$\mathcal{N}_{\mathrm{B2B}}^{\mathrm{s}}(x,y) = k_{\mathrm{b}}T \cdot \ln\left(\frac{1+\exp\left(-\frac{E_{\mathrm{c}}^{\mathrm{ch,s}}(x,y)-E_{\mathrm{f}}^{\mathrm{s}}}{k_{\mathrm{b}}T}\right)}{1+\exp\left(-\frac{E_{\mathrm{c}}^{\mathrm{ch,s}}(x,y)-E_{\mathrm{f}}^{\mathrm{d}}}{k_{\mathrm{b}}T}\right)}\right), \tag{5.76}$$

$$\mathcal{N}_{\mathrm{B2B}}^{\mathrm{d}}(x,y) = k_{\mathrm{b}}T \cdot \ln\left(\frac{1+\exp\left(\frac{E_{\mathrm{v}}^{\mathrm{ch,d}}(x,y)-E_{\mathrm{f}}^{\mathrm{d}}}{k_{\mathrm{b}}T}\right)}{1+\exp\left(\frac{E_{\mathrm{v}}^{\mathrm{ch,d}}(x,y)-E_{\mathrm{f}}^{\mathrm{s}}}{k_{\mathrm{b}}T}\right)}\right), \tag{5.77}$$

considering the Fermi energy in source and drain, $E_{\mathrm{f}}^{\mathrm{s}}$ and $E_{\mathrm{f}}^{\mathrm{d}}$, respectively.

A schematic sketch of the B2B TGR along the x-axis for an arbitrary y-position is shown in Fig. 5.7(a). Both, the ON-state and the AMBIPOLAR-state are illustrated and the maximum TGR values are highlighted, which are used for a compact description of the TGR in the following. Figure 5.7(b) shows the corresponding band diagram for the TGR along the x-axis. In the ON-state ($V_{\mathrm{gs,ON}}$), a B2B tunneling area is formed at the source-to-channel junction in the interval $[x_{\mathrm{t},1}^{\mathrm{s}} \leq x \leq x_{\mathrm{t},2}^{\mathrm{s}}]$ and in the AMBIPOLAR-state ($V_{\mathrm{gs,AMB}}$) the resulting B2B tunneling area is located at the drain-to-channel junction defined in the interval $[x_{\mathrm{t},2}^{\mathrm{d}} \leq x \leq x_{\mathrm{t},1}^{\mathrm{d}}]$.

With the help of Eq. (5.75), it is possible to calculate the TGR in every single point within the channel region, but this equation is not integrable in a closed-form. This fact forbids a usage in compact models and therefore, the TGR has to be described by an analytical function. Considering Fig. 5.7(a), it can be seen that the TGR follows approximately a Gaussian

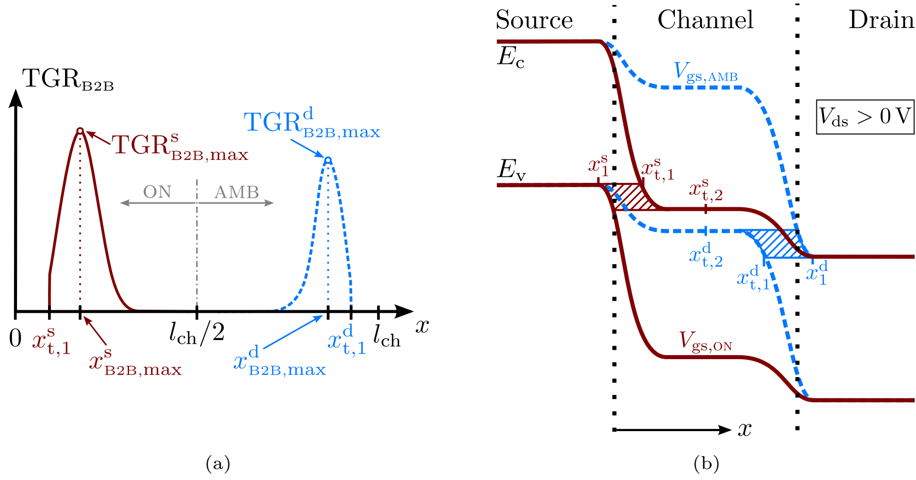


Figure 5.7.: (a) Schematic shape of the TGR along the x-axis and an arbitrary y-position, showing the maximum value of the TGR in the ON- and AMBIPOLAR-state of the DG TFET. (b) Band diagram sketch of the ON- and AMBIPOLAR-state to highlight the B2B tunneling areas at the channel junctions. The limits of the B2B tunneling areas are denoted as $x^{s/d}_{t,1}$ and $x^{s/d}_{t,2}$. The x-values, where band bending in S/D region equals zero, are denoted as $x^{s/d}_1$. In both plots: Red solid lines: ON-state. Blue dashed lines: AMBIPOLAR-state.

distribution function, hence a compact (cp) TGR expression is defined as:

$$\mathrm{TGR}^{s/d}_{\mathrm{cp,B2B}}(x,y) = \mathrm{TGR}^{s/d}_{\mathrm{B2B,max}}(y) \cdot \exp\left(-\frac{\left(x - x^{s/d}_{\mathrm{B2B,max}}\right)^2}{\left(\sigma^{s/d}_{\mathrm{B2B}}\right)^2}\right), \tag{5.78}$$

by using the variance $(\sigma^{s/d}_{\mathrm{B2B}})^2$ of the Gaussian distribution as an adjustable parameter. The maximum TGR value is calculated with the help of Eq. (5.75):

$$\mathrm{TGR}^{s/d}_{\mathrm{B2B,max}}(y) = \mathrm{TGR}^{s/d}_{\mathrm{B2B}}\left(x^{s/d}_{\mathrm{B2B,max}}, y\right), \tag{5.79}$$

whereby $x^{s/d}_{\mathrm{B2B,max}}$ defines the x-position of the maximum TGR value. It is assumed that the maximum TGR value is found at the x-position, where the tunneling length (see Eq. (5.59)) is the smallest and hence the first derivative of the tunneling length leads to the required x-value. For the ON-state follows:

$$\frac{\mathrm{d}\left(l^{\mathrm{B2B,s}}_{\mathrm{tun}}(x,y)\right)}{\mathrm{d}x} = \frac{\mathrm{d}}{\mathrm{d}x}\left(x + \frac{b_s}{2 \cdot a_s} - \sqrt{\frac{1}{a_s} \cdot \left(\frac{k_s}{x - l_s} + m_s + K^s_1\right)}\right) \overset{!}{=} 0$$

$$1 + \frac{k_s}{2 \cdot (x - l_s)^2 \cdot a_s \cdot \sqrt{\frac{1}{a_s} \cdot \left(\frac{k_s}{x - l_s} + m_s + K^s_1\right)}} \overset{!}{=} 0. \tag{5.80}$$

Solving Eq. (5.80) for x leads to the position of the maximum TGR in the ON-state:

$$x^{\mathrm{s}}_{\mathrm{B2B,max}}(y) = \frac{1}{2} \cdot \sqrt{\frac{\vartheta^{\mathrm{s}}_1}{12 \cdot \sqrt[3]{2} \cdot a_{\mathrm{s}} \cdot K^{\mathrm{s}}_1} + \frac{4 \cdot \sqrt[3]{2} \cdot k^2_{\mathrm{s}}}{\vartheta^{\mathrm{s}}_1} + \frac{\vartheta^{\mathrm{s}}_2}{2 \cdot \sqrt{\frac{\vartheta^{\mathrm{s}}_1}{\sqrt[3]{2} \cdot a_{\mathrm{s}} \cdot K^{\mathrm{s}}_1} - \frac{48 \cdot \sqrt[3]{2} \cdot k^2_{\mathrm{s}}}{\vartheta^{\mathrm{s}}_1} + \frac{3 \cdot k^2_{\mathrm{s}}}{(K^{\mathrm{s}}_1)^2}}} + \vartheta^{\mathrm{s}}_3}$$
$$+ \frac{1}{4 \cdot \sqrt{3}} \cdot \sqrt{\frac{\vartheta^{\mathrm{s}}_1}{\sqrt[3]{2} \cdot a_{\mathrm{s}} \cdot K^{\mathrm{s}}_1} - \frac{48 \cdot \sqrt[3]{2} \cdot k^2_{\mathrm{s}}}{\vartheta^{\mathrm{s}}_1} + \frac{3 \cdot k^2_{\mathrm{s}}}{(K_1)^2}} - \frac{k_{\mathrm{s}} - 4 \cdot K^{\mathrm{s}}_1 \cdot l_{\mathrm{s}}}{4 \cdot K^{\mathrm{s}}_1}, \tag{5.81}$$

using the abbreviations:

$$\vartheta^{\mathrm{s}}_1 = -\sqrt[3]{432 \cdot a^2_{\mathrm{s}} \cdot k^4_{\mathrm{s}} + \sqrt{186624 \cdot a^2_{\mathrm{s}} \cdot k^8_{\mathrm{s}} + 442368 \cdot a^3_{\mathrm{s}} \cdot k^6_{\mathrm{s}} \cdot (K^{\mathrm{s}}_1)^3}}, \tag{5.82}$$

$$\vartheta^{\mathrm{s}}_2 = \sqrt{3} \cdot \left(-\frac{(k_{\mathrm{s}} - 4 \cdot K^{\mathrm{s}}_1 \cdot l_{\mathrm{s}})^3}{(K^{\mathrm{s}}_1)^3} + \frac{12 \cdot (2 \cdot K^{\mathrm{s}}_1 \cdot l^2_{\mathrm{s}} - k_{\mathrm{s}} \cdot l_{\mathrm{s}}) \cdot (k_{\mathrm{s}} - 4 \cdot K^{\mathrm{s}}_1 \cdot l_{\mathrm{s}})}{(K^{\mathrm{s}}_1)^2} - \frac{8 \cdot (3 \cdot k_{\mathrm{s}} \cdot l^2_{\mathrm{s}} - 4 \cdot K^{\mathrm{s}}_1 \cdot l^3_{\mathrm{s}})}{K^{\mathrm{s}}_1} \right), \tag{5.83}$$

$$\vartheta^{\mathrm{s}}_3 = \frac{a_{\mathrm{s}} \cdot k_{\mathrm{s}} \cdot l_{\mathrm{s}} - 2 \cdot a_{\mathrm{s}} \cdot K^{\mathrm{s}}_1 \cdot l^2_{\mathrm{s}}}{a_{\mathrm{s}} \cdot K^{\mathrm{s}}_1} + \frac{(k_{\mathrm{s}} - 4 \cdot K^{\mathrm{s}}_1 \cdot l_{\mathrm{s}})^2}{2 \cdot (K^{\mathrm{s}}_1)^2} - \frac{3 \cdot (2 \cdot K^{\mathrm{s}}_1 \cdot l^2_{\mathrm{s}} - k_{\mathrm{s}} \cdot l_{\mathrm{s}})}{K^{\mathrm{s}}_1}. \tag{5.84}$$

The x-position, which refers to the maximum TGR in the AMBIPOLAR-state, is derived in a similar way. The first derivative of the tunneling length (see Eq. (5.64)) at the drain-to-channel junction yields:

$$\frac{\mathrm{d}\left(l^{\mathrm{B2B,d}}_{\mathrm{tun}}(x,y)\right)}{\mathrm{d}x} = \frac{\mathrm{d}}{\mathrm{d}x}\left(-x - \frac{b_{\mathrm{d}}}{2 \cdot a_{\mathrm{d}}} - \sqrt{\frac{1}{a_{\mathrm{d}}} \cdot \left(\frac{k_{\mathrm{d}}}{x^{\mathrm{d}}_{\mathrm{t}} - l_{\mathrm{d}}} + m_{\mathrm{d}} + K^{\mathrm{d}}_1 \right)} \right) \overset{!}{=} 0$$
$$\frac{k_{\mathrm{d}}}{2 \cdot (x - l_{\mathrm{d}})^2 \cdot a_{\mathrm{d}} \cdot \sqrt{\frac{1}{a_{\mathrm{d}}} \cdot \left(\frac{k_{\mathrm{d}}}{x - l_{\mathrm{d}}} + m_{\mathrm{d}} + K^{\mathrm{d}}_1 \right)}} - 1 \overset{!}{=} 0 \tag{5.85}$$

and solving for x leads to:

$$x^{\mathrm{d}}_{\mathrm{B2B,max}}(y) =$$
$$-\frac{1}{2} \cdot \sqrt{-\frac{\vartheta^{\mathrm{d}}_1}{12 \cdot \sqrt[3]{2} \cdot a_{\mathrm{d}} \cdot K^{\mathrm{d}}_1} + \frac{4 \cdot \sqrt[3]{2} \cdot k^2_{\mathrm{d}}}{\vartheta^{\mathrm{d}}_1} - \frac{\vartheta^{\mathrm{d}}_2}{2 \cdot \sqrt{\frac{\vartheta^{\mathrm{d}}_1}{\sqrt[3]{2} \cdot a_{\mathrm{d}} \cdot K^{\mathrm{d}}_1} - \frac{48 \cdot \sqrt[3]{2} \cdot k^2_{\mathrm{d}}}{\vartheta^{\mathrm{d}}_1} + \frac{3 \cdot k^2_{\mathrm{d}}}{(K^{\mathrm{d}}_1)^2}}} + \vartheta^{\mathrm{d}}_3}$$
$$-\frac{1}{4 \cdot \sqrt{3}} \cdot \sqrt{\frac{\vartheta^{\mathrm{d}}_1}{\sqrt[3]{2} \cdot a_{\mathrm{d}} \cdot K^{\mathrm{d}}_1} - \frac{48 \cdot \sqrt[3]{2} \cdot k^2_{\mathrm{d}}}{\vartheta^{\mathrm{d}}_1} + \frac{3 \cdot k^2_{\mathrm{d}}}{(K^{\mathrm{d}}_1)^2}} - \frac{k_{\mathrm{d}} - 4 \cdot K^{\mathrm{d}}_1 \cdot l_{\mathrm{d}}}{4 \cdot K^{\mathrm{d}}_1}, \tag{5.86}$$

with:

$$\vartheta_1^{\mathrm{d}} = -\sqrt[3]{432 \cdot a_{\mathrm{d}}^2 \cdot k_{\mathrm{d}}^4 + \sqrt{186624 \cdot a_{\mathrm{d}}^4 \cdot k_{\mathrm{d}}^8 + 442368 \cdot a_{\mathrm{d}}^3 \cdot k_{\mathrm{d}}^6 \cdot (K_1^{\mathrm{d}})^3}}, \tag{5.87}$$

$$\vartheta_2^{\mathrm{d}} = \sqrt{3} \cdot \left(-\frac{(k_{\mathrm{d}} - 4 \cdot K_1^{\mathrm{d}} \cdot l_{\mathrm{d}})^3}{(K_1^{\mathrm{d}})^3} + \frac{12 \cdot (2 \cdot K_1^{\mathrm{d}} \cdot l_{\mathrm{d}}^2 - k_{\mathrm{d}} \cdot l_{\mathrm{d}}) \cdot (k_{\mathrm{d}} - 4 \cdot K_1^{\mathrm{d}} \cdot l_{\mathrm{d}})}{(K_1^{\mathrm{d}})^2} - \frac{8 \cdot (3 \cdot k_{\mathrm{d}} \cdot l_{\mathrm{d}}^2 - 4 \cdot K_1^{\mathrm{d}} \cdot l_{\mathrm{d}}^3)}{K_1^{\mathrm{d}}} \right), \tag{5.88}$$

$$\vartheta_3^{\mathrm{d}} = \frac{a_{\mathrm{d}} \cdot k_{\mathrm{d}} \cdot l_{\mathrm{d}} - 2 \cdot a_{\mathrm{d}} \cdot K_1^{\mathrm{d}} \cdot l_{\mathrm{d}}^2}{a_{\mathrm{d}} \cdot K_1^{\mathrm{d}}} + \frac{(k_{\mathrm{d}} - 4 \cdot K_1^{\mathrm{d}} \cdot l_{\mathrm{d}})^2}{2 \cdot (K_1^{\mathrm{d}})^2} - \frac{3 \cdot (2 \cdot K_1^{\mathrm{d}} \cdot l_{\mathrm{d}}^2 - k_{\mathrm{d}} \cdot l_{\mathrm{d}})}{K_1^{\mathrm{d}}}. \tag{5.89}$$

5.4.4 Compact Current Density (B2B)

With the help of the closed-form expression for the B2B tunneling generation rate (see Eq. (5.78)), it is possible to find a compact expression for the B2B current density. An integration of Eq. (5.78) results in:

$$\begin{aligned} J_{y,\mathrm{B2B}}^{\mathrm{s}}(y) &= q \cdot \int_{x_{\mathrm{t},1}^{\mathrm{s}}}^{x_{\mathrm{t},2}^{\mathrm{s}}} \mathrm{TGR}_{\mathrm{cp,B2B}}^{\mathrm{s/d}}(x,y)\,\mathrm{d}x \\ &= q \cdot \frac{\sqrt{\pi} \cdot \sigma_{\mathrm{B2B}}^{\mathrm{s}} \cdot \mathrm{TGR}_{\mathrm{B2B,max}}^{\mathrm{s}}(y)}{2} \cdot \left[\mathrm{erf}\left(\frac{x - x_{\mathrm{B2B,max}}^{\mathrm{s}}}{\sigma_{\mathrm{B2B}}^{\mathrm{s}}} \right) \right] \Bigg|_{x_{\mathrm{t},1}^{\mathrm{s}}}^{x_{\mathrm{t},2}^{\mathrm{s}}}, \end{aligned} \tag{5.90}$$

$$\begin{aligned} J_{y,\mathrm{B2B}}^{\mathrm{d}}(y) &= q \cdot \int_{x_{\mathrm{t},2}^{\mathrm{d}}}^{x_{\mathrm{t},1}^{\mathrm{d}}} \mathrm{TGR}_{\mathrm{cp,B2B}}^{\mathrm{d}}(x,y)\,\mathrm{d}x \\ &= q \cdot \frac{\sqrt{\pi} \cdot \sigma_{\mathrm{B2B}}^{\mathrm{d}} \cdot \mathrm{TGR}_{\mathrm{B2B,max}}^{\mathrm{d}}(y)}{2} \cdot \left[\mathrm{erf}\left(\frac{x - x_{\mathrm{B2B,max}}^{\mathrm{d}}}{\sigma_{\mathrm{B2B}}^{\mathrm{d}}} \right) \right] \Bigg|_{x_{\mathrm{t},2}^{\mathrm{d}}}^{x_{\mathrm{t},1}^{\mathrm{d}}}, \end{aligned} \tag{5.91}$$

whereby the term "erf" describes the error function[1]. The integration limits in the both cases are calculated in dependency with the band diagram.

The limit $x_{\mathrm{t},1}^{\mathrm{s}}$ in the ON-state describes the x-position, where the ValB in source $E_{\mathrm{v}}^{\mathrm{s}}(x_1^{\mathrm{s}}, y)$ starts to overlap the ConB in the channel $E_{\mathrm{c}}^{\mathrm{ch,s}}(x_{\mathrm{t},1}^{\mathrm{s}}, y)$ as it is depicted in Fig. 5.7(b). Solving

1 A Verilog-A suitable approximation of the error function is presented in App. B.2

the expression $E_{\mathrm{v}}^{\mathrm{s}}(x_1^{\mathrm{s}}, y) = E_{\mathrm{c}}^{\mathrm{ch,s}}(x_{\mathrm{t},1}^{\mathrm{s}}, y)$ for the needed value $x_{\mathrm{t},1}^{\mathrm{s}}$ yields:

$$\begin{aligned} E_{\mathrm{v}}^{\mathrm{s}}(x_1^{\mathrm{s}}, y) &= E_{\mathrm{c}}^{\mathrm{ch,s}}(x_{\mathrm{t},1}^{\mathrm{s}}, y) \\ -q \cdot (\Phi_{\mathrm{bi}}^{\mathrm{s}} + V_{\mathrm{s}}) - \frac{E_{\mathrm{g}}^{\mathrm{s}}}{2} &= -q \cdot \left(\frac{k_{\mathrm{s}}}{x_{\mathrm{t},1}^{\mathrm{s}} - l_{\mathrm{s}}} + m_{\mathrm{s}} \right) + \chi_{\mathrm{s}} - \chi_{\mathrm{ch}} + \frac{E_{\mathrm{g}}^{\mathrm{ch}}}{2} \\ \Rightarrow x_{\mathrm{t},1}^{\mathrm{s}}(y) &= l_{\mathrm{s}}(y) + \frac{k_{\mathrm{s}}(y)}{\Phi_{\mathrm{bi}}^{\mathrm{s}} + V_{\mathrm{s}} - m_{\mathrm{s}}(y) + \frac{1}{q} \cdot \left(\frac{E_{\mathrm{g}}^{\mathrm{ch}} + E_{\mathrm{g}}^{\mathrm{s}}}{2} + \chi_{\mathrm{s}} - \chi_{\mathrm{ch}} \right)}, \end{aligned} \tag{5.92}$$

where the resulting value $x_{\mathrm{t},1}^{\mathrm{s}}$ must be greater or equal to parameter l_{s} ($x_{\mathrm{t},1}^{\mathrm{s}} \geq l_{\mathrm{s}}$). If the resulting x value falls below l_{s}, the integration limit is smoothly set to l_{s} ($x_{\mathrm{t},1}^{\mathrm{s}} = l_{\mathrm{s}}$) to avoid discontinuities.

In the AMBIPOLAR-state, the integration limit $x_{\mathrm{t},1}^{\mathrm{d}}$ is determined with the help of the condition $E_{\mathrm{c}}^{\mathrm{d}}(x_1^{\mathrm{d}}, y) = E_{\mathrm{v}}^{\mathrm{ch,d}}(x_{\mathrm{t},1}^{\mathrm{d}}, y)$. This condition describes the x-position in the channel, where the ConB in drain starts to overlap the ValB in the channel (see Fig. 5.7(b)). It follows:

$$\begin{aligned} E_{\mathrm{c}}^{\mathrm{d}}(x_1^{\mathrm{d}}, y) &= E_{\mathrm{v}}^{\mathrm{ch,d}}(x_{\mathrm{t},1}^{\mathrm{d}}, y) \\ -q \cdot \left(\Phi_{\mathrm{bi}}^{\mathrm{d}} + V_{\mathrm{ds}}\right) + \chi_{\mathrm{s}} - \chi_{\mathrm{d}} + \frac{E_{\mathrm{g}}^{\mathrm{d}}}{2} &= -q \cdot \left(\frac{k_{\mathrm{d}}}{x_{\mathrm{t},1}^{\mathrm{d}} - l_{\mathrm{d}}} + m_{\mathrm{d}} \right) + \chi_{\mathrm{s}} - \chi_{\mathrm{ch}} + \frac{E_{\mathrm{g}}^{\mathrm{ch}}}{2} \\ \Rightarrow x_{\mathrm{t},1}^{\mathrm{d}}(y) &= l_{\mathrm{d}}(y) - \frac{k_{\mathrm{d}}(y)}{\Phi_{\mathrm{bi}}^{\mathrm{d}} + V_{\mathrm{ds}} - m_{\mathrm{d}}(y) - \frac{1}{q} \cdot \left(\frac{E_{\mathrm{g}}^{\mathrm{d}} + E_{\mathrm{g}}^{\mathrm{ch}}}{2} - \chi_{\mathrm{d}} + \chi_{\mathrm{ch}} \right)}. \end{aligned} \tag{5.93}$$

In this expression, the resulting $x_{\mathrm{t},1}^{\mathrm{d}}$ must be smaller or equal to the parameter l_{d} ($x_{\mathrm{t},1}^{\mathrm{d}} \leq l_{\mathrm{d}}$). When $x_{\mathrm{t},1}^{\mathrm{d}}$ overcomes the value of l_{d}, it is smoothly set to l_{d}.

The second integration limit is in general set to $x_{\mathrm{t},2}^{\mathrm{s/d}} = {}^{l_{\mathrm{ch}}}/_{2}$ in case of $V_{\mathrm{gs,ON/AMB},1}$ (see Fig. 5.8), since from this x-position the contribution of the integration to the current density can be neglected. But in that case that the channel potential pinning or inversion charges come into play ($V_{\mathrm{gs,ON/AMB},2}$), the integration limit $x_{\mathrm{t},2}^{\mathrm{s/d}}$ shifts. In ON-state, if the ConB in the channel middle falls below the ConB at the drain region edge ($E_{\mathrm{c}}^{\mathrm{ch,s}}({}^{l_{\mathrm{ch}}}/_{2}, y) < E_{\mathrm{c}}^{\mathrm{d}}(l_{\mathrm{ch}} + l_{\mathrm{sd}}, y)$), as it is shown in Fig. 5.8(a), the limit $x_{\mathrm{t},2}^{\mathrm{s}}$ moves to the direction of the source-to-channel junction. This parameter is determined by the point, where the ConB in the channel equals the ConB at the drain edge. It follows:

$$\begin{aligned} E_{\mathrm{c}}^{\mathrm{d}}(l_{\mathrm{ch}} + l_{\mathrm{sd}}, y) &= E_{\mathrm{c}}^{\mathrm{ch,s}}(x_{\mathrm{t},2}^{\mathrm{s}}, y) \\ -q \cdot \left(\Phi_{\mathrm{bi}}^{\mathrm{d}} + V_{\mathrm{ds}}\right) + \chi_{\mathrm{s}} - \chi_{\mathrm{d}} + \frac{E_{\mathrm{g}}^{\mathrm{d}}}{2} &= -q \cdot \left(\frac{k_{\mathrm{s}}}{x_{\mathrm{t},2}^{\mathrm{s}} - l_{\mathrm{s}}} + m_{\mathrm{s}} \right) + \chi_{\mathrm{s}} - \chi_{\mathrm{ch}} + \frac{E_{\mathrm{g}}^{\mathrm{ch}}}{2} \\ \Rightarrow x_{\mathrm{t},2}^{\mathrm{s}}(y) &= l_{\mathrm{s}}(y) + \frac{k_{\mathrm{s}}(y)}{\Phi_{\mathrm{bi}}^{\mathrm{d}} + V_{\mathrm{ds}} - m_{\mathrm{s}}(y) - \frac{1}{q} \cdot \left(\frac{E_{\mathrm{g}}^{\mathrm{d}} - E_{\mathrm{g}}^{\mathrm{ch}}}{2} + \chi_{\mathrm{ch}} - \chi_{\mathrm{d}} \right)}. \end{aligned} \tag{5.94}$$

In the AMBIPOLAR-state, the second integration limit shifts when the ValB in the center of the channel overcomes the ValB at the S region edge ($E_{\mathrm{v}}^{\mathrm{ch,d}}({}^{l_{\mathrm{ch}}}/_{2}, y) > E_{\mathrm{v}}^{\mathrm{s}}(-l_{\mathrm{sd}}, y)$). In this

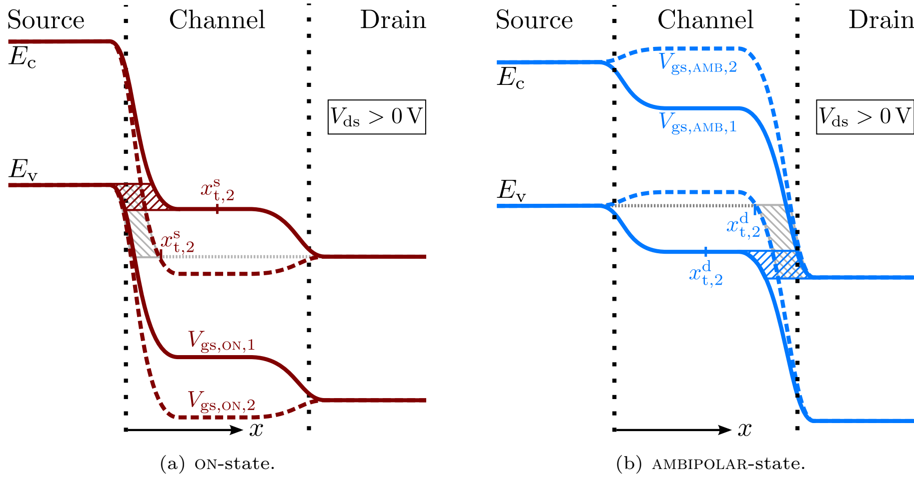


Figure 5.8.: Band diagram sketch showing the influence of channel potential pinning or inversion charges on the second integration limit of the B2B current density in (a) the ON-state ($V_{gs,ON,1} < V_{gs,ON,2}$) and (b) the AMBIPOLAR-state ($V_{gs,AMB,1} > V_{gs,AMB,2}$) of the DG TFET. In both cases $x^{s/d}_{t,2}$ moves to the tunneling junction for increasing/decreasing V_{gs}-values. Solid lines: No inversion charges and no channel potential pinning. Dashed lines: The effect of inversion charges causes the pinning of the channel potential.

case $x^d_{t,2}$ is given by:

$$E^s_v(-l_{sd}, y) = E^{ch,s}_v(x^d_{t,2}, y)$$
$$-q \cdot (\Phi^s_{bi} + V_s) - \frac{E^s_g}{2} = -q \cdot \left(\frac{k_d}{x^d_{t,2} - l_d} + m_d \right) + \chi_s - \chi_{ch} - \frac{E^{ch}_g}{2}$$
$$\Rightarrow x^d_{t,2}(y) = l_d(y) + \frac{k_d(y)}{\Phi^s_{bi} + V_s - m_d(y) - \frac{1}{q} \cdot \left(\frac{E^{ch}_g - E^s_g}{2} + \chi_{ch} - \chi_s \right)}, \tag{5.95}$$

in the other case, $x^d_{t,2}$ is defined by $^{l_{ch}}/_2$.

After deriving the integration limits for the tunneling areas shown in Fig. 5.8, the B2B tunneling current density can be calculated at any y-position in the channel. In order to characterize the B2B tunneling current, the current density has to be expressed by an analytical function that is integrable in closed-form. A schematic shape of the B2B current density is depicted in Fig. 5.9. It can be seen that $J_{y,B2B}$ follows approximately a Gaussian distribution function for both, the ON- and AMBIPOLAR-state. The maximum of the Gaussian distribution is assumed to be at the channel surface, since the highest electrostatic control is directly under the gate insulators. By picking only two points $J^{s/d}_{y,B2B}(y_1 = 0\,\text{nm})$ and $J^{s/d}_{y,B2B}(y_2 = {}^{t_{ch}}/_2)$, the compact B2B current density in the first half of the channel $[0 \le y \le {}^{t_{ch}}/_2]$ is expressed as

follows:

$$J^{\mathrm{s/d}}_{\mathrm{cp,B2B}}(y) = \left(J^{\mathrm{s/d}}_{y,\mathrm{B2B}}(y_1) - J^{\mathrm{s/d}}_{y,\mathrm{B2B}}(y_2)\right) \cdot \exp\left(-\frac{(y-y_1)^2}{(\eta^{\mathrm{s/d}})^2}\right) + J^{\mathrm{s/d}}_{y,\mathrm{B2B}}(y_2), \tag{5.96}$$

where the term $J^{\mathrm{s/d}}_{y,\mathrm{B2B}}(y_2)$ compensates the offset in the center of the channel. The variance $(\eta^{\mathrm{s/d}})^2$ of the Gaussian distribution is used as a fitting parameter. Due to the symmetry of the DG TFET, it is not necessary to model the second half of the channel. With the help of this compact B2B tunneling current density, it is possible to derive a closed-form expression for the B2B tunneling current of the DG TFET in Sec. 5.6.

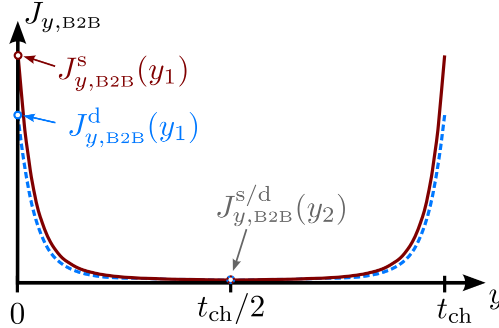


Figure 5.9.: Schematic shape of the B2B current density along the y-axis in the ON-state (red solid lines) and the AMBIPOLAR-state (blue dashed lines) obtained after careful TCAD investigations. The highlighted characteristic points $J^{\mathrm{s/d}}_{y,\mathrm{B2B}}(y_1)$ and $J^{\mathrm{s/d}}_{y,\mathrm{B2B}}(y_2)$ are used for a compact description of the current density.

5.5 Trap-Assisted Tunneling Current Density

In the calculations of the device current of TFETs, it is absolutely indispensable to consider the effect of TAT, which worsens the resulting subthreshold slope as well as the ON/OFF-ratio of the TFET [67, 68]. The following modeling approach was introduced in [137]. In order to take into account the effect of TAT in FEM device simulation, a generation model has been introduced by Hurkx [154]. The generation rate formula reads as:

$$G_{\mathrm{t}} = \frac{p \cdot n - n_{\mathrm{i}}^2}{\frac{\varsigma_{\mathrm{h}}}{1+\Gamma_{\mathrm{h}}} \cdot (n + n_1) + \frac{\varsigma_{\mathrm{e}}}{1+\Gamma_{\mathrm{e}}} \cdot (p + p_1)}, \tag{5.97}$$

$$n_1 = n_{\mathrm{i}} \cdot \exp\left(\frac{\Delta E_{\mathrm{fi}}}{k_{\mathrm{b}} T}\right), \quad p_1 = n_{\mathrm{i}} \cdot \exp\left(-\frac{\Delta E_{\mathrm{fi}}}{k_{\mathrm{b}} T}\right), \tag{5.98}$$

with the intrinsic carrier concentration n_{i}, the electron/hole carrier concentration n/p, the electron/hole generation lifetime $\varsigma_{\mathrm{e/h}}$ and the relative position of the trap energy level with respect to the intrinsic Fermi energy ΔE_{fi}. The parameter $\Gamma_{\mathrm{e/h}}$ describes the field-effect enhancement factor and covers the influence of both the Poole-Frenkel effect and the effect of

trap-assisted tunneling. This factor is given by [172]:

$$\Gamma_{\mathrm{e/h}} = \frac{1}{4 \cdot k_{\mathrm{b}}T} \cdot \int\limits_{E} \exp\left(\pm\frac{E_{\mathrm{c/v}} - E_x}{k_{\mathrm{b}}T}\right) \cdot T_{\mathrm{tun}}^{\mathrm{TAT}}(E_x)\,\mathrm{d}E_x, \tag{5.99}$$

where E_x is the energy to which an electron or hole is tunneling to and $T_{\mathrm{tun}}^{\mathrm{TAT}}$ is the tunneling probability that a carrier is able to tunnel from a trap state into the ConB/ValB.

By modifying Eq. (5.97), the generation rates for electrons and holes can separately be expressed as follows [173]:

$$G_{\mathrm{t}}^{\mathrm{e}} = \frac{n_1 \cdot (1 + \Gamma_{\mathrm{e}}) \cdot f_{\mathrm{t}}}{\varsigma_{\mathrm{e}}}, \tag{5.100}$$

$$G_{\mathrm{t}}^{\mathrm{h}} = \frac{p_1 \cdot (1 + \Gamma_{\mathrm{h}}) \cdot (1 - f_{\mathrm{t}})}{\varsigma_{\mathrm{h}}}, \tag{5.101}$$

using the probability f_{t} that a trap state at the considered energy is occupied. In case that electrons are dominating the TAT process, which means $\Gamma_{\mathrm{e}} \gg \Gamma_{\mathrm{h}}$, the term f_{t} can approximately be expressed by the Fermi-Dirac distribution for electrons [173].

In order to characterize the TAT current density along the y-axis similar to the B2B tunneling case for both the ON- and AMBIPOLAR-state, Landauer's tunneling formula (see Eq. (3.48) and (5.54)) is combined with Hurkx's TAT generation rate, which leads to [174]:

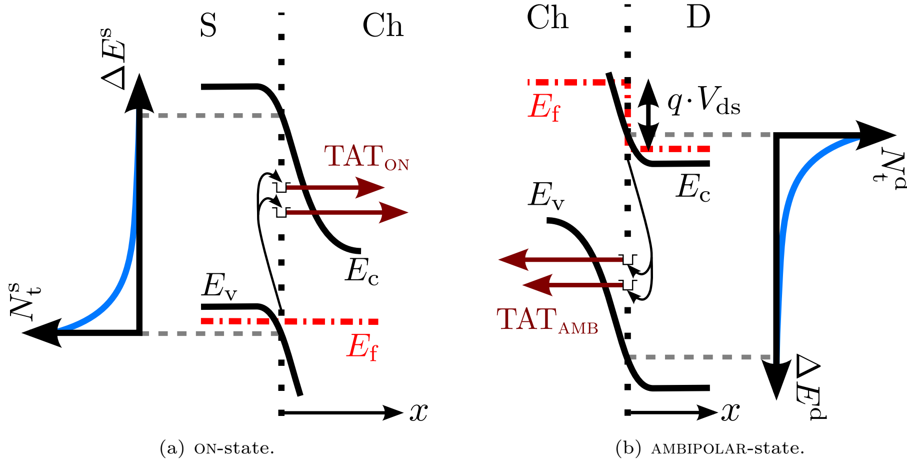
$$\begin{aligned} J_{\mathrm{tun,TAT}}^{\mathrm{s/d}}(y) &= q \cdot \int\limits_{x} \frac{m_{\mathrm{s/d}}^{*}}{2\pi^2 \cdot \hbar^3} \cdot \tau_{\mathrm{TAT}}^{\mathrm{s/d}} \cdot N_{\mathrm{t}}^{\mathrm{s/d}}(x,y) \cdot \mathcal{N}_{\mathrm{TAT}}^{\mathrm{s/d}}(x,y) \cdot \left[1 + \Gamma^{\mathrm{s/d}}(x,y)\right] \cdot q \cdot |\vec{E}^{\mathrm{s/d}}(x,y)|\,\mathrm{d}x, \\ &= q \cdot \int\limits_{x} \mathrm{TGR}_{\mathrm{TAT}}^{\mathrm{s/d}}(x,y), \end{aligned} \tag{5.102}$$

where $\mathrm{TGR}_{\mathrm{TAT}}^{\mathrm{s/d}}$ defines the TAT generation rate, by considering the capture cross section $\tau_{\mathrm{TAT}}^{\mathrm{s}}$, the supply function $\mathcal{N}_{\mathrm{TAT}}^{\mathrm{s/d}}$, the enhancement factor $\Gamma^{\mathrm{s/d}}$ including the tunneling probability $T_{\mathrm{tun}}^{\mathrm{TAT}}$ and the electric field $|\vec{E}^{\mathrm{s/d}}|$. The trap density $N_{\mathrm{t}}^{\mathrm{s/d}}$ is used in order to replace the carrier concentration n_1/p_1 in Eq. (5.100) and (5.101) and is introduced in the next section.

5.5.1 Interface Trap Density

The interface traps or midgap traps at the channel junctions determine the OFF-state current of the TFET as it is introduced in Sec. 3.3.1. The traps are a consequence of the high doping concentration of the S and D region and are assumed to be exponentially distributed along the junctions with respect to the energy as it is shown in Fig. 5.10.

Due to the high p-doping concentration of the S region, the maximum value of the exponential trap density is located at the ValB edge of the junction, which is shown in Fig. 5.10(a). In this case, the electrons can hop from the ValB onto an empty trap at the junction and from there they can tunnel into the ConB of the channel. On the other hand, Fig. 5.10(b) shows the



(a) ON-state.

(b) AMBIPOLAR-state.

Figure 5.10.: Schematic band diagram to show the working principle of the TAT process at the channel junctions. (a) Electrons are able to hop on an empty state at the source-to-channel junction and tunnel into the channel ConB. (b) Holes can hop on an empty state at the drain-to-channel junction and penetrate into the ValB of the channel. In both cases traps, are exponentially distributed regarding energy.

drain-to-channel junction, where due to the high n-doping concentration of the D region the maximum trap density is located at the ConB edge of the junction. Here, a hole is able to hop from the ConB onto an empty state at the junction and tunnel through the energy barrier into the ValB of the channel region. The trap density over energy is defined by:

$$N_{\mathrm{t}}^{\mathrm{s/d}}(x,y) = N_{\mathrm{t}}^{0} \cdot \exp\left(-\frac{\Delta E^{\mathrm{s/d}}(x,y)}{\varkappa_{\mathrm{TAT}}^{\mathrm{s/d}} \cdot k_{\mathrm{b}} T}\right), \tag{5.103}$$

by using the maximum trap density N_{t}^{0} and the adjustable parameter $\varkappa_{\mathrm{TAT}}^{\mathrm{s/d}}$ to tune the resulting slope of the TAT current, whose influence is shown in the model verification (see Chap. 6). The energy differences ΔE are given by:

$$\Delta E^{\mathrm{s}}(x,y) = E_{\mathrm{c}}^{\mathrm{ch,s}}(x,y) - E_{\mathrm{v}}^{\mathrm{ch,s}}(0,y), \tag{5.104}$$

$$\Delta E^{\mathrm{d}}(x,y) = E_{\mathrm{c}}^{\mathrm{ch,d}}(l_{\mathrm{ch}},y) - E_{\mathrm{v}}^{\mathrm{ch,d}}(x,y). \tag{5.105}$$

5.5.2 Field-Effect Enhancement Factor and Tunneling Probability (TAT)

The field-effect enhancement factor characterizes the influence of tunneling in Eq. (5.97). If the enhancement factor is small ($\Gamma \ll 1$), e.g. for weak electric fields, Eq. (5.97) reduces to the well-known SRH generation formula [154].

The tunneling probability that a carrier is able to tunnel from a trap to the ConB/ValB in the channel is calculated by using the AE WKB approach presented in Sec. 5.4.2. In case

of TAT, the tunneling length is adapted because here, the tunneling process starts from the channel junctions and ends in the channel. Hence, the part of the tunneling distance within the S/D region is equal to zero and therefore the tunneling length in Eq. (5.59) and (5.64) reduces to:

$$l_{\text{tun}}^{\text{TAT,s}}(x) = x, \quad l_{\text{tun}}^{\text{TAT,d}}(x) = l_{\text{ch}} - x. \tag{5.106}$$

So, the tunneling probability at the source-to-channel junction (ON-state) is calculated by replacing the $l_{\text{tun}}^{\text{B2B,s}}$ in Eq. (5.73) as follows:

$$T_{\text{tun}}^{\text{TAT,s}}(x,y) = \exp\left(-\frac{4}{3}\cdot\sqrt{\frac{2\cdot m_{\text{s}}^{*}}{\hbar^2}\cdot U_{\text{bar}}^{\text{s}}(x,y)}\cdot l_{\text{tun}}^{\text{TAT,s}}(x)\right). \tag{5.107}$$

In the AMBIPOLAR-state, $T_{\text{tun}}^{\text{TAT}}$ is obtained by replacing the tunneling length in Eq. (5.74):

$$T_{\text{tun}}^{\text{TAT,d}}(x,y) = \exp\left(-\frac{4}{3}\cdot\sqrt{\frac{2\cdot m_{\text{d}}^{*}}{\hbar^2}\cdot U_{\text{bar}}^{\text{d}}(x,y)}\cdot l_{\text{tun}}^{\text{TAT,d}}(x)\right). \tag{5.108}$$

Regarding Eq. (5.99) and inserting the compact expression for the TAT tunneling probability $T_{\text{tun}}^{\text{TAT}}$, it is not possible to find a closed-form solution for the integral over the energy. For this reason, it is necessary to approximate the enhancement factor. After some investigations using a numerical solution of Eq. (5.99), the enhancement factor along the x-axis in the ON-state follows approximately the expression:

$$\Gamma^{\text{s}}(x,y) \approxeq \exp\left(-\frac{\Delta E^{\text{s}}(x,y)}{\varkappa_{\text{TAT}}^{\text{s}}\cdot k_{\text{b}}T}\right)\cdot T_{\text{tun}}^{\text{TAT,s}}(x,y), \tag{5.109}$$

whereby for the AMBIPOLAR-state yields:

$$\Gamma^{\text{d}}(x,y) \approxeq \exp\left(-\frac{\Delta E^{\text{d}}(x,y)}{\varkappa_{\text{TAT}}^{\text{d}}\cdot k_{\text{b}}T}\right)\cdot T_{\text{tun}}^{\text{TAT,d}}(x,y), \tag{5.110}$$

where the parameters $\Delta E^{\text{s/d}}$ and $\varkappa_{\text{TAT}}^{\text{s/d}}$ are used in the same manner as in the calculations of the interface trap density.

5.5.3 Tunneling Generation Rate (TAT)

The number of carriers that are generated per second and volume by TAT are called TAT generation rate and can be determined by Eq. (5.102). A schematic sketch of the TGR along the x-axis is shown in Fig. 5.11(a) and the related band diagram, which addresses the tunneling areas for the ON- and AMBIPOLAR-state TAT current parts, is depicted in Fig. 5.11(b). With the help of the interface trap density, the field-effect enhancement factor and by considering the integration limits of the TAT process (see Fig. 5.11), Eq. (5.102) is rewritten for the ON-state

as follows:

$$J^{\mathrm{s}}_{\mathrm{tun,TAT}}(y) = q \cdot \int_{0}^{\frac{l_{\mathrm{ch}}}{2}} \frac{m^*_{\mathrm{s}}}{2\pi^2 \cdot \hbar^3} \cdot \tau^{\mathrm{s}}_{\mathrm{TAT}} \cdot N^{\mathrm{s}}_{\mathrm{t}}(x,y) \cdot \mathcal{N}^{\mathrm{s}}_{\mathrm{TAT}}(x,y) \cdot [1+\Gamma^{\mathrm{s}}(x,y)] \cdot q \cdot |\vec{E}^{\mathrm{s}}(x,y)| \, \mathrm{d}x$$

$$J^{\mathrm{s}}_{\mathrm{tun,TAT}}(y) = q \cdot \int_{0}^{\frac{l_{\mathrm{ch}}}{2}} \mathrm{TGR}^{\mathrm{s}}_{\mathrm{TAT}}(x,y) \, \mathrm{d}x. \tag{5.111}$$

For the AMBIPOLAR-state Eq. (5.102) leads to:

$$J^{\mathrm{d}}_{\mathrm{tun,TAT}}(y) = q \cdot \int_{\frac{l_{\mathrm{ch}}}{2}}^{l_{\mathrm{ch}}} \frac{m^*_{\mathrm{d}}}{2\pi^2 \cdot \hbar^3} \cdot \tau^{\mathrm{d}}_{\mathrm{TAT}} \cdot N^{\mathrm{d}}_{\mathrm{t}}(x,y) \cdot \mathcal{N}^{\mathrm{d}}_{\mathrm{TAT}}(x,y) \cdot \left[1+\Gamma^{\mathrm{d}}(x,y)\right] \cdot q \cdot |\vec{E}^{\mathrm{d}}(x,y)| \, \mathrm{d}x,$$

$$J^{\mathrm{d}}_{\mathrm{tun,TAT}}(y) = q \cdot \int_{\frac{l_{\mathrm{ch}}}{2}}^{l_{\mathrm{ch}}} \mathrm{TGR}^{\mathrm{d}}_{\mathrm{TAT}}(x,y) \, \mathrm{d}x, \tag{5.112}$$

whereby it should be noted that an integration over the half of the channel length is sufficient, since the tunneling length at bigger (ON-state) or smaller (AMBIPOLAR-state) x-positions increases and thus the tunneling probability $T^{\mathrm{TAT}}_{\mathrm{tun}}$ is almost equal to zero (see Fig. 5.11(b)).

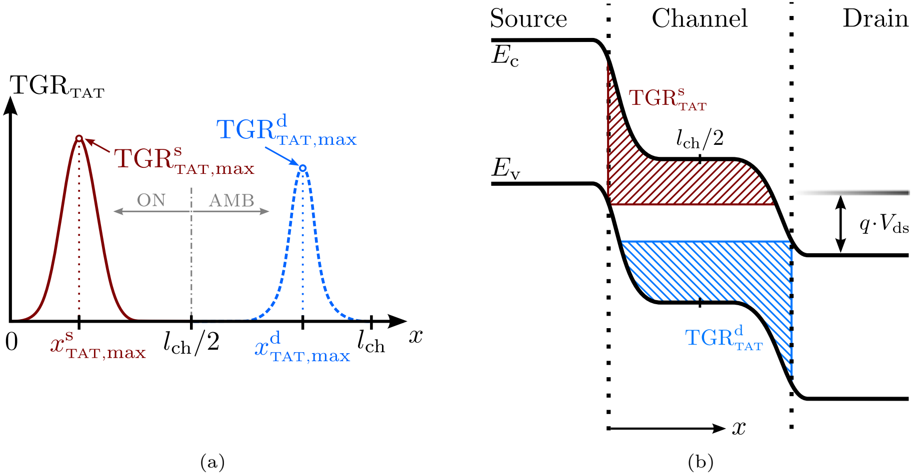


Figure 5.11.: (a) Sketch of the TAT generation rate along the x-axis for any y-position. The maximum TGR values for the ON- and AMBIPOLAR-state are separately illustrated. (b) Schematic band diagram to illustrate the areas, where TAT can occur are highlighted. In both figures: Red lines: ON-state. Blue lines: AMBIPOLAR-state.

The supply function $\mathcal{N}$ has been introduced in Sec. 5.4.3 and is adapted for the TAT model. It follows:

$$\mathcal{N}^{\mathrm{s}}_{\mathrm{TAT}}(x,y) = k_{\mathrm{b}}T \cdot \ln\left(\frac{1+\exp\left(-\frac{E^{\mathrm{ch,s}}_{\mathrm{c}}(x,y)-E^{\mathrm{s}}_{\mathrm{f}}}{\varkappa^{\mathrm{s}}_{\mathrm{TAT}}\cdot k_{\mathrm{b}}T}\right)}{1+\exp\left(-\frac{E^{\mathrm{ch,s}}_{\mathrm{c}}(x,y)-E^{\mathrm{d}}_{\mathrm{f}}}{\varkappa^{\mathrm{s}}_{\mathrm{TAT}}\cdot k_{\mathrm{b}}T}\right)}\right), \tag{5.113}$$

$$\mathcal{N}^{\mathrm{d}}_{\mathrm{TAT}}(x,y) = k_{\mathrm{b}}T \cdot \ln\left(\frac{1+\exp\left(\frac{E^{\mathrm{ch,d}}_{\mathrm{v}}(x,y)-E^{\mathrm{d}}_{\mathrm{f}}}{\varkappa^{\mathrm{d}}_{\mathrm{TAT}}\cdot k_{\mathrm{b}}T}\right)}{1+\exp\left(\frac{E^{\mathrm{ch,d}}_{\mathrm{v}}(x,y)-E^{\mathrm{s}}_{\mathrm{f}}}{\varkappa^{\mathrm{d}}_{\mathrm{TAT}}\cdot k_{\mathrm{b}}T}\right)}\right), \tag{5.114}$$

using the compact band diagram expressions for the ConB in the channel $E^{\mathrm{ch,s}}_{\mathrm{c}}$ (see Eq. (5.40)) and the channel ValB $E^{\mathrm{ch,d}}_{\mathrm{v}}$ (see Eq. (5.43)). The parameter $\varkappa^{\mathrm{s/d}}_{\mathrm{TAT}}$ is used to adapt the resulting slope of the TAT current as it has been mentioned in the previous section. Now, the generation rate due to TAT can be calculated at every x and y-position within the channel region.

In order to solve the integral of the current density in closed-form, it is necessary to approximate the $\mathrm{TGR}_{\mathrm{TAT}}$ along the x-axis for any y-positions in the channel.

After investigating the curve shape within the integral of Eq. (5.111) and (5.112), the $\mathrm{TGR}_{\mathrm{TAT}}$ can be approximated by a Gaussian distribution function (see Fig. 5.11(a)), which leads to the following compact expression:

$$\mathrm{TGR}^{\mathrm{s/d}}_{\mathrm{cp,TAT}}(x,y) = \mathrm{TGR}^{\mathrm{s/d}}_{\mathrm{TAT,max}}(y) \cdot \exp\left(-\frac{\left(x - x^{\mathrm{s/d}}_{\mathrm{TAT,max}}\right)^2}{\left(\sigma^{\mathrm{s/d}}_{\mathrm{TAT}}\right)^2}\right), \tag{5.115}$$

whereby the variance $(\sigma^{\mathrm{s/d}}_{\mathrm{TAT}})^2$ of the Gaussian distribution and the position of the maximum TGR value $x^{\mathrm{s}}_{\mathrm{TAT,max}}$ in the ON-state are used as adjustable parameters. This x-position in the AMBIPOLAR-state is defined by:

$$x^{\mathrm{d}}_{\mathrm{TAT,max}} = l_{\mathrm{ch}} - x^{\mathrm{s}}_{\mathrm{TAT,max}} \tag{5.116}$$

and the maximum TGR value is given by Eqs. (5.111) and (5.112):

$$\mathrm{TGR}^{\mathrm{s/d}}_{\mathrm{TAT,max}}(y) = \mathrm{TGR}^{\mathrm{s/d}}_{\mathrm{TAT}}\left(x^{\mathrm{s/d}}_{\mathrm{TAT,max}}, y\right). \tag{5.117}$$

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5.5.4 Compact Current Density (TAT)

The TAT current density along the y-axis is now obtained by integrating the compact TAT generation rate (see Eqs. (5.111) and (5.112)). The integrals read as:

$$J^{\mathrm{s}}_{y,\mathrm{TAT}}(y) = q \cdot \int_{0}^{\frac{l_{\mathrm{ch}}}{2}} \mathrm{TGR}^{\mathrm{s}}_{\mathrm{cp,TAT}}(x,y)\ \mathrm{d}x$$

$$= q \cdot \frac{\sqrt{\pi} \cdot \sigma^{\mathrm{s}}_{\mathrm{TAT}} \cdot \mathrm{TGR}^{\mathrm{s}}_{\mathrm{TAT,max}}(y)}{2} \cdot \mathrm{erf}\left(\frac{x - x^{\mathrm{s}}_{\mathrm{TAT,max}}}{\sigma^{\mathrm{s}}_{\mathrm{TAT}}}\right)\Bigg|_{0}^{\frac{l_{\mathrm{ch}}}{2}}, \tag{5.118}$$

$$J^{\mathrm{d}}_{y,\mathrm{TAT}}(y) = q \cdot \int_{\frac{l_{\mathrm{ch}}}{2}}^{l_{\mathrm{ch}}} \mathrm{TGR}^{\mathrm{d}}_{\mathrm{cp,TAT}}(x,y)\ \mathrm{d}x$$

$$= q \cdot \frac{\sqrt{\pi} \cdot \sigma^{\mathrm{d}}_{\mathrm{TAT}} \cdot \mathrm{TGR}^{\mathrm{d}}_{\mathrm{TAT,max}}(y)}{2} \cdot \mathrm{erf}\left(\frac{x - x^{\mathrm{d}}_{\mathrm{TAT,max}}}{\sigma^{\mathrm{d}}_{\mathrm{TAT}}}\right)\Bigg|_{\frac{l_{\mathrm{ch}}}{2}}^{l_{\mathrm{ch}}}, \tag{5.119}$$

with the error function erf. Due to the symmetry of the error function and by taking advantage of the dependency of $x^{\mathrm{d}}_{\mathrm{TAT,max}}$ on $x^{\mathrm{s}}_{\mathrm{TAT,max}}$, Eqs. (5.118) and (5.119) are rewritten as:

$$J^{\mathrm{s/d}}_{y,\mathrm{TAT}}(y) = q \cdot \frac{\sqrt{\pi} \cdot \sigma^{\mathrm{s/d}}_{\mathrm{TAT}} \cdot \mathrm{TGR}^{\mathrm{s/d}}_{\mathrm{TAT,max}}(y)}{2} \cdot \mathrm{erf}\left(\frac{x - x^{\mathrm{s}}_{\mathrm{TAT,max}}}{\sigma^{\mathrm{s/d}}_{\mathrm{TAT}}}\right)\Bigg|_{0}^{\frac{l_{\mathrm{ch}}}{2}}. \tag{5.120}$$

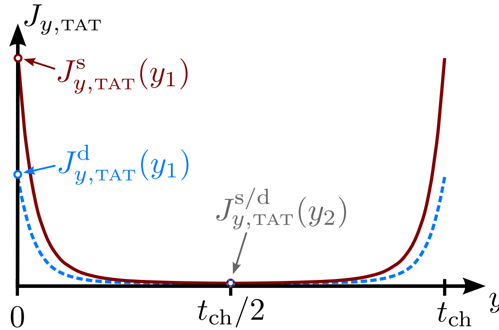

Figure 5.12.: Sketch of the TAT current density shape along the y-axis. The ON-state is shown in solid red lines and AMBIPOLAR-state in dashed blue lines. The shown points $J^{\mathrm{s/d}}_{y,\mathrm{TAT}}(y_1)$ and $J^{\mathrm{s/d}}_{y,\mathrm{TAT}}(y_2)$ are used for the compact current density expression.

In the next step, a closed-form expression for the TAT current density has to be found in the same way as it is mentioned in Sec. 5.4.4. The shape of the TAT current density along the y-axis is schematically shown in Fig. 5.12. That is to see, that the current density follows approximately a Gaussian distribution. For this reason, the compact TAT current density in

the first half of the channel $[0 \leq y \leq {}^{t_{\mathrm{ch}}}/_{2}]$ is defined by:

$$J^{\mathrm{s/d}}_{\mathrm{cp,TAT}}(y) = \left(J^{\mathrm{s/d}}_{y,\mathrm{TAT}}(y_1) - J^{\mathrm{s/d}}_{y,\mathrm{TAT}}(y_2)\right) \cdot \exp\left(-\frac{(y-y_1)^2}{\left(\eta^{\mathrm{s/d}}\right)^2}\right) + J^{\mathrm{s/d}}_{y,\mathrm{TAT}}(y_2), \tag{5.121}$$

using two points of the TAT current density calculated by Eq. (5.120). The first value is calculated at the channel surface ($y_1 = 0\,\mathrm{nm}$) and the second one is determined in the center of the channel at $y_2 = {}^{t_{\mathrm{ch}}}/_{2}$. The maximum of the Gaussian distribution is located at the channel surface due to the highest electrostatic control of the gate electrodes. The center TAT current density is used to compensate the offset in the middle of the channel. The variance $(\eta^{\mathrm{s/d}})^2$ of the Gaussian distribution is used as a fitting parameter and has the same value as the variance of the B2B tunneling current density shown in Eq. (5.96).

5.6 Tunneling Current

In the final step of the compact DC model, an expression for the total device current I_{ds} is derived. The device current considers the B2B tunneling as well as the parasitic TAT current part and is determined with help of the compact current density expressions for B2B tunneling (see Eq. (5.96)) and TAT (see Eq. (5.121)). In addition, due to the symmetry of the DG TFET, it is sufficient to calculate I_{ds} only for one half of the channel, which means an integration in the interval $[0 \leq y \leq {}^{t_{\mathrm{ch}}}/_{2}]$, and multiplying the resulting current by the factor 2. The device current is obtained by integrating the current densities and defined by:

$$I_{\mathrm{ds}} = I_{\mathrm{ds,B2B}} + I_{\mathrm{ds,TAT}} \tag{5.122}$$

$$= 2 \cdot w_{\mathrm{ch}} \cdot \int_0^{\frac{t_{\mathrm{ch}}}{2}} \left(J^{\mathrm{s}}_{\mathrm{cp,B2B}}(y) + J^{\mathrm{d}}_{\mathrm{cp,B2B}}(y)\right) + \left(J^{\mathrm{s}}_{\mathrm{cp,TAT}}(y) + J^{\mathrm{d}}_{\mathrm{cp,TAT}}(y)\right) \mathrm{d}y, \tag{5.123}$$

with the channel width w_{ch}. The integration results in:

$$\begin{aligned} I_{\mathrm{ds}} &= 2 \cdot w_{\mathrm{ch}} \\ &\times \Bigg[\frac{\sqrt{\pi} \cdot \eta^{\mathrm{s}} \cdot \left(J^{\mathrm{s}}_{y,\mathrm{B2B}}(y_1) - J^{\mathrm{s}}_{y,\mathrm{B2B}}(y_2)\right)}{2} \cdot \mathrm{erf}\left(\frac{y-y_1}{\eta^{\mathrm{s}}}\right) + J^{\mathrm{s}}_{y,\mathrm{B2B}}(y_2) \cdot y \\ &+ \frac{\sqrt{\pi} \cdot \eta^{\mathrm{d}} \cdot \left(J^{\mathrm{d}}_{y,\mathrm{B2B}}(y_1) - J^{\mathrm{d}}_{y,\mathrm{B2B}}(y_2)\right)}{2} \cdot \mathrm{erf}\left(\frac{y-y_1}{\eta^{\mathrm{d}}}\right) + J^{\mathrm{d}}_{y,\mathrm{B2B}}(y_2) \cdot y \\ &+ \frac{\sqrt{\pi} \cdot \eta^{\mathrm{s}} \cdot \left(J^{\mathrm{s}}_{y,\mathrm{TAT}}(y_1) - J^{\mathrm{s}}_{y,\mathrm{TAT}}(y_2)\right)}{2} \cdot \mathrm{erf}\left(\frac{y-y_1}{\eta^{\mathrm{s}}}\right) + J^{\mathrm{s}}_{y,\mathrm{TAT}}(y_2) \cdot y \\ &+ \frac{\sqrt{\pi} \cdot \eta^{\mathrm{d}} \cdot \left(J^{\mathrm{d}}_{y,\mathrm{TAT}}(y_1) - J^{\mathrm{d}}_{y,\mathrm{TAT}}(y_2)\right)}{2} \cdot \mathrm{erf}\left(\frac{y-y_1}{\eta^{\mathrm{d}}}\right) + J^{\mathrm{d}}_{y,\mathrm{TAT}}(y_2) \cdot y \Bigg]\Bigg|_0^{\frac{t_{\mathrm{ch}}}{2}}. \end{aligned} \tag{5.124}$$

It should be noted that the hardware description language Verilog-A does not have an implementation of the error function and therefore, a Verilog-A suitable approximation of the error function is introduced in App. B.2.

Furthermore, it should be noted that in order to ensure a decent model behavior for bias conditions far away from the practical working region of the TFET, the terminal voltages V_{ds} and V_{gs} are smoothly saturated to constant values. The smooth limitation of the terminal input voltages improves the convergence of the compact model during the simulation iterations and is presented in App. C.

In the case that the device is biased with negative drain-source voltages $V_{\mathrm{ds}} < 0\,\mathrm{V}$, the TFET turns into a parasitic forward-biased p/n diode (see Sec. 3.3.6), which is not considered in the compact modeling approach. In order to incorporate this effect, a simple equation to calculate the diode current is applied. It follows:

$$I_{\mathrm{diode}} = -J_{\mathrm{diode}} \cdot w_{\mathrm{ch}} \cdot \left[\exp\left(-\frac{q \cdot V_{\mathrm{ds,in}}}{n_{\mathrm{diode}} \cdot k_{\mathrm{b}} T}\right) - 1\right], \tag{5.125}$$

with the reverse bias saturation current density $J_{\mathrm{diode}} \approx 10^{-18}\mathrm{A/\mu m}$, the input terminal drain-source voltage $V_{\mathrm{ds,in}}$ and the quality factor n_{diode} of the diode. The resulting diode current is added to the compact tunneling current I_{ds} and ensures the model continuity for negative V_{ds} values.

The compact equations and expression of the tunneling current I_{ds} are derived for an n-type DG TFET, but are not limited to this type of device. The p-type TFET can simply be emulated from the equations of the n-type modeling approach.

CHAPTER 6

Modeling Results & Verification

The verification of the compact model derived in Chap. 5 is done in the following. First of all, the compact model is validated in Sec. 6.1 with the help of TCAD Sentaurus simulation data. Beside the resulting device current, partial results like electrostatics or tunneling generation rate are examined and verified. After the verification by TCAD simulations, the device current is validated by measurement data of complementary NW GAA TFETs in Sec. 6.2. The compact model simulations of the partial results are calculated in MATLAB [175]. The simulations of the I-V characteristics and their derivatives are performed with a Verilog-A implementation of the compact model equations in the IC-Characterization and Analysis Program (IC-CAP) from Keysight Technologies [87] and Cadence Virtuoso [86].

6.1 Verification by TCAD Sentaurus Simulation Data

In this section the compact modeling approach presented in Chap. 5 is verified with the help of 2D TCAD Sentaurus simulations of the n-type DG TFET shown in Fig. 6.1.

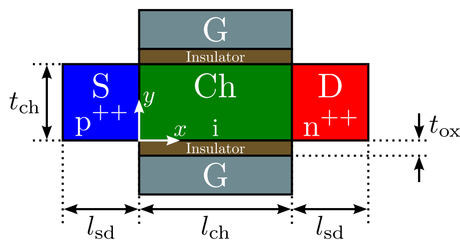

Figure 6.1.: 2D sketch of the n-type DG TFET device geometry, showing the channel thickness t_{ch}, the channel length l_{ch}, the gate oxide thickness t_{ox} and the length of the S/D region l_{sd}. Source and drain region are highly p/n-doped with a doping concentration $N_{s/d}$.

For verification a standard Silicon device (Si TFET) is defined with the geometrical dimensions and the doping concentrations listed in Tab. 6.1, where a homogeneous distribution of current density along the channel width w_{ch} is assumed. Furthermore, the standard device is

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made of Silicon, the gate insulator is HfO_2 and the gate contacts consist of Aluminum, unless otherwise is stated. TCAD simulations are performed by applying a non-local B2B tunneling model and the TAT model of Hurkx with a maximum interface trap density N_t^0 to consider the influence of the parasitic TAT effect [79, 154]. The values of the carrier rest masses $m^*_{e/h,TCAD}$ are also listed in Tab. 6.1, since the tunneling processes strongly depend on these masses. Due to the high doping concentration of the source and drain region, it is essential to consider the BGN effect in the numerical simulations of the DG TFET. The model of Slotboom is applied in TCAD simulations to capture the BGN effect in the highly p-doped source region [170], whereas the model of Del Alamo BGN is considered in the highly n-doped drain region [171]. The doping profiles at the channel junctions have a slight Gaussian shape with a standard deviation of 0.5 nm, thus they are almost abrupt. The effect of quantum confinement can be neglected in the numerical simulations due to the chosen channel thickness of $t_{ch} \geq 10$ nm [45]. Beside the Si TFET, further simulations are performed for various device dimensions, gate insulators and source materials to investigate the influence of varying device parameters on the TFET behavior. The corresponding values, e.g. dielectric permittivity ε, are also contained in Tab. 6.1.

Table 6.1.: TCAD Sentaurus simulation parameter set for simulating the n-type DG TFET.

Parameter	Value	Parameter	Value
l_{ch}	22 nm	t_{ox}	2 nm
l_{sd}	20 nm	t_{ch}	10 nm
w_{ch}	1 µm	N_s	10^{20} cm^{-3} (p^{++})
Drain Material	Silicon	N_d	10^{20} cm^{-3} (n^{++})
Channel Material	Silicon	N_t^0	10^{12} cm^{-2}

Insulator Material	ε_{ox} [A s/V cm]	Insulator Material	ε_{ox} [A s/V cm]
Y_2O_3	$15 \cdot \varepsilon_0$	La_2O_3	$30 \cdot \varepsilon_0$
HfO_2	$22 \cdot \varepsilon_0$	TiO_2	$80 \cdot \varepsilon_0$
Ta_2O_5	$26 \cdot \varepsilon_0$	—	—

Source Material	$m^*_{e,TCAD}$ [kg]	$m^*_{h,TCAD}$ [kg]	ε_s [A s/V cm]	χ_s [eV]	$E_g^{s,0}$ [eV]
Silicon	$0.26 \cdot m_0$	$0.36 \cdot m_0$	$11.70 \cdot \varepsilon_0$	4.05	1.124
Germanium	$0.15 \cdot m_0$	$0.17 \cdot m_0$	$16.20 \cdot \varepsilon_0$	4.00	0.664
SiGe	$0.18 \cdot m_0$	$0.20 \cdot m_0$	$13.95 \cdot \varepsilon_0$	4.04	0.830
GaAs	$0.065 \cdot m_0$	$0.30 \cdot m_0$	$13.18 \cdot \varepsilon_0$	4.07	1.620

The compact model simulations are performed by applying the same device parameters as in the TCAD setup except for the carrier rest mass $m^*_{s/d}$, which is used as an adjustable parameter. Despite the fact that the compact model equations are derived in closed-form, the usage of a handful of adjustable parameters is unavoidable. A list of the used fitting parameters is presented in Tab. 6.2, where it should be noted that the listed parameters are extracted to obtain a correct device current. In order to be able to carry out a parameter extraction, the

used adjustable parameters are explained in detail below:

- The parameters $\lambda_{\mathrm{fit}}^{\mathrm{s}}$ and $\lambda_{\mathrm{fit}}^{\mathrm{d}}$ can be used to tune the resulting screening length at the source-to-channel and drain-to-channel junction in the electrostatic potential model in weak inversion mode of the TFET. The screening length $\lambda_{\mathrm{s/d}}$ is calculated by Eq. (4.29). The typical range of $\lambda_{\mathrm{fit}}^{\mathrm{s/d}}$ is from 0.5 to 2.0.
- A smooth transition from weak to strong inversion in the 2D closed-form potential solution for the channel region is obtained by Eq. (4.22). The parameters $\lambda_{\mathrm{ln,fit}}^{\mathrm{s}}$ and $\lambda_{\mathrm{ln,fit}}^{\mathrm{d}}$ can be tuned to change the influence of the inversion charges on the resulting potential solution at the channel junctions. The parameters are defined in the interval $[0.2 \leq \lambda_{\mathrm{ln,fit}}^{\mathrm{s/d}} \leq \infty)$. The smaller the value of $\lambda_{\mathrm{ln,fit}}^{\mathrm{s/d}}$, the higher is the influence of the inversion charges on the electrostatics.
- The effective carrier masses m_{s}^* and m_{d}^* have a linear and an exponential impact on the TGR and therefore on the resulting B2B tunneling and TAT current. The TGR is linearly dependent on $m_{\mathrm{s/d}}^*$ and T_{tun} (see Eq. (5.75)), where the exponential dependency comes from. The effective carrier masses should be chosen in the range from $0.05 \cdot m_0$ to $0.7 \cdot m_0$.
- The variance $(\eta^{\mathrm{s/d}})^2$ of the B2B tunneling and TAT current density along the y-axis in the ON- and AMBIPOLAR-state occurs in the Eqs. (5.96), (5.121) and (5.124) and has a linear dependency on the device current and an inverse proportionality to the error function term in the current calculation. Since the error function saturates to the value 1, the linear dependency dominates in the calculations of the current. The value of the variance should be chosen to be $(\eta^{\mathrm{s/d}})^2 \leq t_{\mathrm{ch}}^2$, otherwise the influence on the current disappears.
- The variance $(\sigma_{\mathrm{B2B}}^{\mathrm{s/d}})^2$ of the B2B TGR along the x-axis occurs in Eq. (5.78) and has nearly the same influence on the resulting tunneling current in the ON- and AMBIPOLAR-state as the variance $(\eta^{\mathrm{s/d}})^2$ of the current density along the y-axis, but in this case only the B2B tunneling current part is tuned. The difference between $(\sigma_{\mathrm{B2B}}^{\mathrm{s/d}})^2$ and $(\eta^{\mathrm{s/d}})^2$ is how they affect the device current in the presence of the inversion charges. When these charges come into play and a too high value for $(\sigma_{\mathrm{B2B}}^{\mathrm{s/d}})^2$ is chosen, the B2B current saturates. Thus, the variance should be smaller than $({}^{l_{\mathrm{ch}}}/{}_4)^2$.
- The parameter $(\sigma_{\mathrm{TAT}}^{\mathrm{s/d}})^2$ is the variance of the TAT generation rate approximation along the x-axis in Eq. (5.115). The influence is the same as in the parameter $(\eta^{\mathrm{s/d}})^2$, with the difference that only the TAT current part is tuned. The value should be smaller than $(({}^{l_{\mathrm{ch}}}/{}_4)^2$.
- The fitting parameter $\varkappa_{\mathrm{TAT}}^{\mathrm{s/d}}$ can be used to tune the resulting slope of the TAT current part, separately for the ON- and AMBIPOLAR-state. The smaller the value of $\varkappa_{\mathrm{TAT}}^{\mathrm{s/d}}$, the steeper the resulting slope, whereby the amount of the TAT current has to be adapted by the parameter $\tau_{\mathrm{TAT}}^{\mathrm{s/d}}$ afterwards. This parameter is used in the Eqs. (5.103), (5.109), (5.110), (5.113) and (5.114). The parameter $\varkappa_{\mathrm{TAT}}^{\mathrm{s/d}}$ is in the range from 1.0 to 100.

- The capture cross section $\tau_{\mathrm{TAT}}^{\mathrm{s/d}}$ is used as a linear adjustable factor in the Eqs. (5.111) and (5.112). The amount of $\tau_{\mathrm{TAT}}^{\mathrm{s/d}}$ has to be positive and is typically in the range from $10^{-23}\mathrm{cm}^2$ to $10^{-18}\mathrm{cm}^2$.
- The flat band voltage V_{fb} is used to shift the applied gate-source voltage V_{gs} in order to consider a change in the work function of the gate contact material. A negative V_{fb} causes an increase of the applied V_{gs} and hence a shift to the left in n-type devices of the resulting I_{ds} in the current transfer curve. In p-type device the influence is vice versa. The flatband voltage is used in the calculations of the effective gate-source voltage in Sec. 4.1.2.
- The last adjustable parameter $x_{\mathrm{TAT,max}}^{\mathrm{s}}$ is the x-position of the TAT generation rate maximum and is valid in the range $[0 < x_{\mathrm{TAT,max}}^{\mathrm{s}} < {}^{l_{\mathrm{ch}}}/2]$. The influence of this parameter is as follows: If $x_{\mathrm{TAT,max}}^{\mathrm{s}}$ is increased starting from zero, then the TAT current increases up to the position where the $\mathrm{TGR}_{\mathrm{TAT}}$ in Eq. (5.111) has its maximum. After that, the TAT current decreases again.

The influence of these adjustable parameters on the transfer I-V characteristics is qualitatively demonstrated in App. D.

Table 6.2.: Adjustable parameters of the DG TFET compact model for the Silicon TFET (SI TFET) and TFETs with various source materials (Mat. S).

Parameter	Unit	Si TFET	Mat. S: Ge	Mat. S: SiGe	Mat. S: GaAs
$\lambda_{\mathrm{fit}}^{\mathrm{s}}$	[–]	1.47	1.20	1.35	1.40
$\lambda_{\mathrm{fit}}^{\mathrm{d}}$	[–]	1.39	1.25	1.25	1.13
$\lambda_{\mathrm{ln,fit}}^{\mathrm{s}}$	[–]	0.76	0.60	0.20	0.50
$\lambda_{\mathrm{ln,fit}}^{\mathrm{d}}$	[–]	0.25	0.40	0.40	0.40
m_{s}^{*}	[kg]	$0.26{\cdot}m_0$	$0.30{\cdot}m_0$	$0.24{\cdot}m_0$	$0.18{\cdot}m_0$
m_{d}^{*}	[kg]	$0.30{\cdot}m_0$	$0.30{\cdot}m_0$	$0.28{\cdot}m_0$	$0.30{\cdot}m_0$
$(\eta^{\mathrm{s}})^2$	[cm^2]	$3.65{\cdot}10^{-16}$	$1.20{\cdot}10^{-14}$	$5.90{\cdot}10^{-16}$	$3.80{\cdot}10^{-16}$
$\left(\eta^{\mathrm{d}}\right)^2$	[cm^2]	$3.50{\cdot}10^{-16}$	$4.00{\cdot}10^{-16}$	$6.50{\cdot}10^{-16}$	$5.60{\cdot}10^{-16}$
$(\sigma_{\mathrm{B2B}}^{\mathrm{s}})^2$	[cm^2]	$2.00{\cdot}10^{-14}$	$3.00{\cdot}10^{-15}$	$6.80{\cdot}10^{-14}$	$4.80{\cdot}10^{-14}$
$\left(\sigma_{\mathrm{B2B}}^{\mathrm{d}}\right)^2$	[cm^2]	$2.40{\cdot}10^{-14}$	$3.30{\cdot}10^{-14}$	$1.10{\cdot}10^{-14}$	$5.20{\cdot}10^{-14}$
$(\sigma_{\mathrm{TAT}}^{\mathrm{s}})^2$	[cm^2]	$1.00{\cdot}10^{-14}$	$5.00{\cdot}10^{-15}$	$8.00{\cdot}10^{-15}$	$1.80{\cdot}10^{-14}$
$\left(\sigma_{\mathrm{TAT}}^{\mathrm{d}}\right)^2$	[cm^2]	$1.00{\cdot}10^{-15}$	$1.00{\cdot}10^{-15}$	$1.00{\cdot}10^{-15}$	$1.00{\cdot}10^{-15}$
$\varkappa_{\mathrm{TAT}}^{\mathrm{s}}$	[–]	10.0	3.2	5.5	4.5
$\varkappa_{\mathrm{TAT}}^{\mathrm{d}}$	[–]	10.0	6.0	8.0	7.3
$\tau_{\mathrm{TAT}}^{\mathrm{s}}$	[cm^2]	$3.00{\cdot}10^{-21}$	$7.52{\cdot}10^{-18}$	$9.00{\cdot}10^{-19}$	$1.62{\cdot}10^{-18}$
$\tau_{\mathrm{TAT}}^{\mathrm{d}}$	[cm^2]	$4.30{\cdot}10^{-21}$	$8.08{\cdot}10^{-20}$	$1.00{\cdot}10^{-20}$	$2.25{\cdot}10^{-20}$
V_{fb}	[V]	−0.54	−0.54	−0.56	−0.50
$x_{\mathrm{TAT,max}}^{\mathrm{s}}$	[nm]	3.0	3.0	3.0	3.0

After introducing the applied fitting parameters, the compact modeling verification by TCAD data is presented in the following sections. At first, the compact electrostatic potential solution, the band diagram and the electric field results are verified in Sec. 6.1.1. Based on

the band diagram results, the verification of the AE WKB approach is presented in Sec. 6.1.2. The validity of the B2B TGR for different source materials is proven in Sec. 6.1.3. In the last part of the TCAD verification, the current characteristics of the DG TFET are investigated for various simulation setups like various terminal voltages or device parameters. The compact model is validated by numerical simulations in Sec. 6.1.4.

6.1.1 Electrostatic Potential, Band Diagram and Electric Field

The electrostatic potential forms the base of all further calculations of the device current I_{ds} and therefore, the compact modeling results of the potential solution are presented first. Since the current density $J^{\mathrm{s/d}}_{y,\mathrm{B2B/TAT}}$ is only needed at the surface ($y = 0\,\mathrm{nm}$) and the center ($y = {}^{t_{\mathrm{ch}}}/_{2}$) of the DG TFET as it has been introduced in Eq. (5.96) and (5.121), the potential along the x-axis is also only solved at these y-positions (see Fig. 6.2). The band diagram is then estimated at the same y-positions based on the potential solution. Since the potential solution in y direction is needed to calculate the electric field, the solution of $\varphi^{\mathrm{s/d}}_{y}$ is verified at the x-positions $x = 0\,\mathrm{nm}$, ${}^{l_{\mathrm{ch}}}/_{2}$ and l_{ch}. After this step, the electric field along the x-axis at the two y-positions is compared to numerical simulations. In all cases, the needed data are extracted exactly at the positions shown in Fig. 6.2.

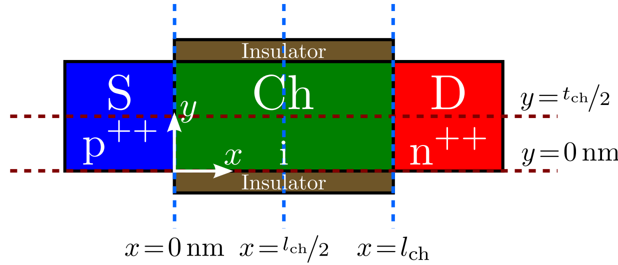

Figure 6.2.: Sketch of the DG TFET channel region, where the compact potential, band diagram and electric field along the x-axis are solved. The cutlines show the surface ($y = 0\,\mathrm{nm}$) and center ($y = {}^{t_{\mathrm{ch}}}/_{2}$) of the device. In addition, three cutlines in y direction are shown, where the potential along the y-axis is calculated.

Electrostatic Potential

The potential solution at the source-to-channel junction (ON-state) is obtained by applying Eqs. (5.1) and (5.10) and the potential at the drain-to-channel junction (AMBIPOLAR-state) is calculated with the help of Eqs. (5.20) and (5.28).

The modeling results at a drain-source voltage of $V_{\mathrm{ds}} = 0.7\,\mathrm{V}$ in a V_{gs} range from $-1.2\,\mathrm{V}$ to $1.0\,\mathrm{V}$ are presented in Fig. 6.3. It should be noted that the potential results for $x \leq {}^{l_{\mathrm{ch}}}/_{2}$ are assigned to the ON-state and the potential results for $x > {}^{l_{\mathrm{ch}}}/_{2}$ are related to the AMBIPOLAR-state. Figure 6.3(a) shows the potential at the surface of the TFET ($y = 0\,\mathrm{nm}$) and it can be seen that the ON-state and the AMBIPOLAR-state potential are very well predicted by the

compact model in comparison to TCAD data. In the case, when inversion charges come into play in the ON-state at $V_{gs} = 1.0\,V$, the compact potential shows a small deviation compared to TCAD data in the range of $x = 1\,nm$ to $9\,nm$. A similar deviation can be seen in AMBIPOLAR-state at $V_{gs} = -1.2\,V$ within the distance between $x = 13\,nm$ and $21\,nm$. At this voltage inversion charges get involved as it can also be seen in Fig. 4.6(a). These, deviations are a cause of the chosen values for the parameters $\lambda_{fit}^{s/d}$ and $\lambda_{ln,fit}^{s/d}$ to obtain a correct device current.

The compact potential results in the channel center $y = {}^{t_{ch}}/_{2}$ in the same V_{gs} voltage range are illustrated in Fig. 6.3(b). It can be seen that the compact model also fits well compared with the numerical simulations, where the same deviations at $V_{gs} = 1.0\,V$ and $-1.2\,V$ occur in comparison to the channel surface. These deviations are caused by the chosen fitting parameters $\lambda_{fit}^{s/d}$ and $\lambda_{ln,fit}^{s/d}$ to obtain a correct device current.

In a next step, the drain-source voltage is decreased to $V_{ds} = 0.1\,V$. The comparison of the compact modeling results and the TCAD simulations within the same V_{gs} range as in the plots before are depicted in Fig. 6.4. The potential at the device surface is presented in Fig. 6.4(a) and it can be seen that the compact potential solution fits very well in the voltage range from $V_{gs} = -1.2\,V$ and $0.4\,V$ in comparison to TCAD simulations. For an applied gate-source voltage of $V_{gs} > 0.4\,V$, inversion charges interfere (see Fig. 4.6(a)) and the channel potential in ON- and AMBIPOLAR-state is a bit overestimated. The compact potential in the center in Fig. 6.4(b) shows also a good fit compared to TCAD data, where some small deviations occur for $V_{gs} > 0.6\,V$ and $V_{gs} < -1.0\,V$. The inaccuracies are due to the applied aforementioned adjustable parameters.

Band Diagram

After proving the correctness of the electrostatic potential, the compact band diagram results are under investigation. The band diagram of the DG TFET is calculated with the help of the Eqs. (5.38)–(5.45).

For a better overview, the gate-source voltage range is separated into two parts for the applied V_{ds}. The first range, showing the ON-state of the TFET, is depicted in Fig. 6.5 for applied V_{gs} values from $0.0\,V$ to $1.0\,V$ and $V_{ds} = 0.7\,V$. The results at the surface $y = 0\,nm$ are illustrated in Fig. 6.5(a) and show a good match in comparison to TCAD. The small kinks occurring at the channel junctions are caused by applied band gap narrowing models (see Eqs. (5.46) and (5.48)). Figure 6.5(b) presents the band diagram at $y = {}^{t_{ch}}/_{2}$ and also shows a good match to the TCAD data. The occurring deviations at both y-positions are to explain in the same manner as in the compact potential verification. In the second V_{gs} range, the gate-source voltage is varied from $-1.2\,V$ to $-0.2\,V$ and the results of the band diagram at the surface and in the center are shown in Fig. 6.6(a) and (b). For the applied voltage values of V_{gs}, the TFET is in the AMBIPOLAR-state. Again, it is important to note that the parameters of the compact model are extracted to obtain an accurate device current, and nevertheless, the

results of the band diagram show a good agreement.

A reduction of the drain-source voltage to $V_{\mathrm{ds}} = 0.1\,\mathrm{V}$ affects the resulting band diagram. Considering the source-to-channel junction in the ON-state of the TFET (see Fig. 6.7), it can be seen that the area in which the bands overlap is reduced in comparison to the results shown inFig. 6.5. As a consequence of the V_{ds} reduction, inversion charges intervene and therefore, pin the channel potential for smaller V_{gs} values. At the surface band diagram shown in Fig. 6.7(a), there is still an acceptable overlap area close to the junction with a relatively short tunneling length. In the center band diagram of the device, which is depicted in Fig. 6.7(b), the potential does not vary much regarding the applied V_{gs} range and the overlap area of the bands is dramatically reduced and thus, the tunneling length results in a relatively high value. In this case the resulting tunneling probability decreases and the contribution of the center TGR to the current density shrinks. Concerning the influence of a V_{ds} reduction on the bands in the AMBIPOLAR-state of the TFET, it is to say that the overlap area at the drain-to-channel junction decreases. This effect is visible in the band diagram results at the surface shown in Fig. 6.8(a) and in the center shown in Fig. 6.8(b). Furthermore, a reduction in the overlap can be seen in comparison to the results presented in Fig. 6.6. A main advantage of a V_{ds} reduction is actually the suppression of the parasitic AMBIPOLAR effect of the TFET.

In order to increase the TFET performance, hetero-junctions are a good choice to increase the resulting device current and subthreshold slope. For this reason, band diagrams for various source materials are presented in the following. At first, Germanium is applied as the source material. This material has a reduced band gap in comparison to Silicon. Simulations for Germanium are performed by adapting the model parameters as it is listed in Tab. 6.2. The results of the band diagram at the surface for an applied $V_{\mathrm{ds}} = 0.7\,\mathrm{V}$ are shown in Fig. 6.9(a). The results in the center are illustrated in Fig. 6.9(b). At both y-positions the compact model predicts the band diagram very well in the applied V_{gs} range from $-0.1\,\mathrm{V}$ to $0.9\,\mathrm{V}$. The characteristic kinks due to the hetero-junction at the source-to-channel junction are also very well reproduced by the band diagram model equations.

Secondly, the band diagram for a SiGe–Si hetero-junction is presented in Fig. 6.10, where the modeled results are compared to TCAD data for various V_{gs} values at $V_{\mathrm{ds}} = 0.7\,\mathrm{V}$. By applying the adjustable parameters shown in Tab. 6.2 to the compact model, it is possible to reproduce the band diagram of this hetero-junction at the surface and in the center in an accurate way.

After that, the source material is changed to GaAs and the compact model parameters are tuned to the values listed in Tab. 6.2. The results are presented in Fig. 6.11 and compared to TCAD simulation results for $V_{\mathrm{ds}} = 0.7\,\mathrm{V}$, where V_{gs} is varied from $0.0\,\mathrm{V}$ to $1.0\,\mathrm{V}$. At both y-positions the model shows a good agreement. Due to the higher band gap of GaAs in comparison to Silicon, a lower tunneling current is expected and therefore a lower device performance. This influence will be investigated and discussed in Sec. 6.1.4.

Potential Along the y-Axis

Before the verification of the electric field, the electrostatic potential approximation along the y-axis is investigated since the electric field is calculated in terms of the potential in x and y direction. The potential in the direction of the y-axis is calculated with the help of Eq. (5.36) and is extracted at the three x-positions shown in Fig. 6.2.

The first results are determined at the source-to-channel junction ($x = 0\,\mathrm{nm}$) for various V_{gs} values at $V_{\mathrm{ds}} = 0.7\,\mathrm{V}$ and are illustrated in Fig. 6.12. At this x-position $\Phi^{\mathrm{s}}_{\mathrm{sur}}$ and $\Phi^{\mathrm{s}}_{\mathrm{cen}}$ are calculated by Eq. (5.10). It can be seen that the shape of the potential is well predicted, whereby a mismatch in the amount of the potential can be investigated. This deviation is a consequence of the chosen fitting parameter $\lambda^{\mathrm{s}}_{\mathrm{fit}} = 1.47$ to obtain an accurate device current. By slightly reducing this parameter, the amount of the potential φ_y would match better.

Figure 6.13 presents the potential modeling results at $x = {}^{l_{\mathrm{ch}}}\!/_{2}$ for the same applied voltages as in the previous plot. At this x-position the calculated potential stays in a good agreement with the TCAD simulations for the whole V_{gs} range from $-1.2\,\mathrm{V}$ to $1.0\,\mathrm{V}$. The change in the sign of the slope of the y potential, which is negative at $V_{\mathrm{gs}} = -1.2\,\mathrm{V}$ and positive at $V_{\mathrm{gs}} = 1.0\,\mathrm{V}$, is correctly predicted by the compact model.

The third potential in y direction is examined at the drain-to-channel junction ($x = l_{\mathrm{ch}}$), by applying the same voltage setup as before. For this reason the needed potentials $\Phi^{\mathrm{d}}_{\mathrm{sur}}$ and $\Phi^{\mathrm{d}}_{\mathrm{cen}}$ to characterize φ_y are determined with the help of Eq. (5.28). The compact modeling results are compared to TCAD simulations and are shown in Fig. 6.14. At this x-position the shape of the potential in y direction is very well reproduced by the compact model, whereby a mismatch in the amount can be seen. This mismatch is similar to the one occurring at the source-to-channel junction and is due to the fitting parameter $\lambda^{\mathrm{d}}_{\mathrm{fit}} = 1.39$ that is chosen to obtain a correct device current I_{ds}. A better accuracy could be achieved by slightly reducing the value of $\lambda^{\mathrm{d}}_{\mathrm{fit}}$.

Electric Field

After the verification of the potential along the x- and y-axis, the accuracy of the electric field approximation presented in Eq. (5.52) is proven in the following. Figure 6.15 presents the modeling results in a range of V_{gs} from $-1.2\,\mathrm{V}$ to $1.0\,\mathrm{V}$ and an applied V_{ds} of $0.7\,\mathrm{V}$. The results of the absolute value of the electric field at $y = 0\,\mathrm{nm}$ are depicted in Fig. 6.15(a) and show a good agreement in comparison to TCAD data in the whole V_{gs} range for both the ON- and the AMBIPOLAR-state. The small deviations occurring from $x = 5\,\mathrm{nm}$ to $15\,\mathrm{nm}$ are negligible since in the calculations of the TGR the applied x-values $x^{\mathrm{s/d}}_{\mathrm{max,B2B/TAT}}$ are always in a range close to the corresponding junction.

In the center of the channel (see Fig. 6.15(b)), the electric field results show also a match with the TCAD data. The small inaccuracies that can be seen in the ON-state for $V_{\mathrm{gs}} \geq 0.6\,\mathrm{V}$

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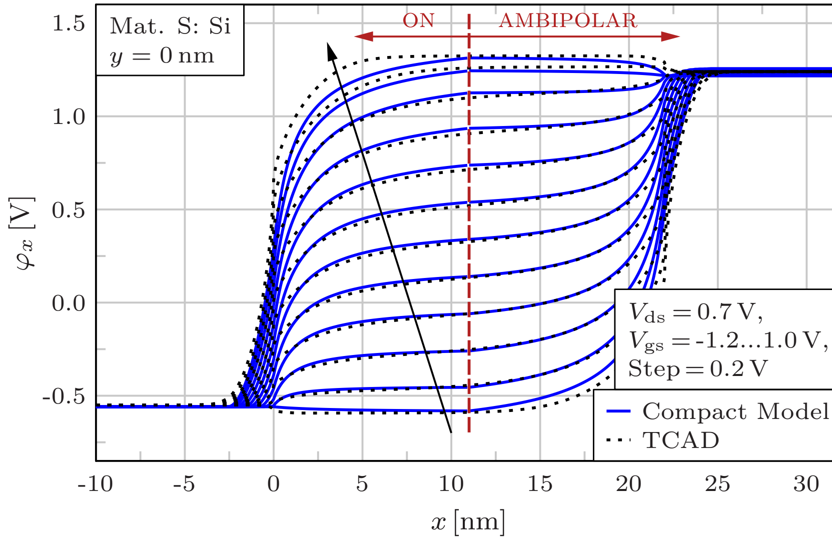
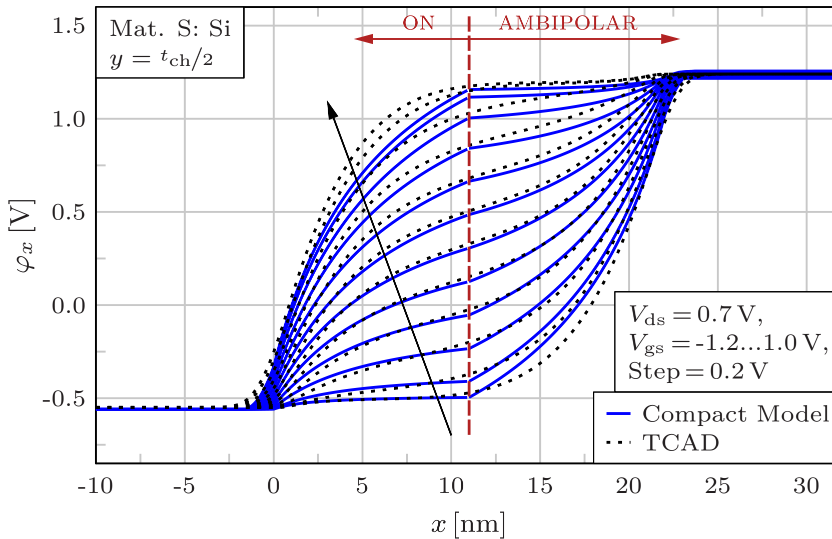
and in the AMBIPOLAR-state for $V_{gs} \leq -0.8\,V$ are a consequence of the mismatch in the potential approximation along the x-axis as it can be seen in Fig. 6.3(b).

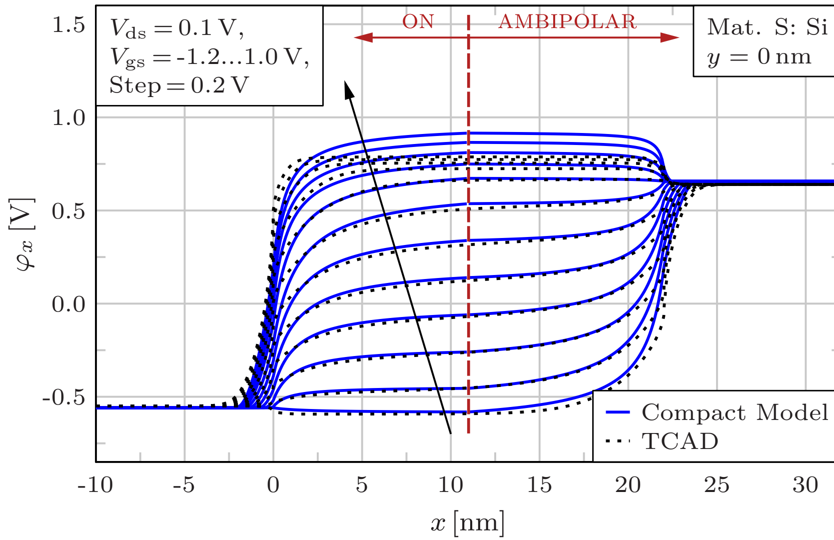


(a) $y = 0\,nm$.

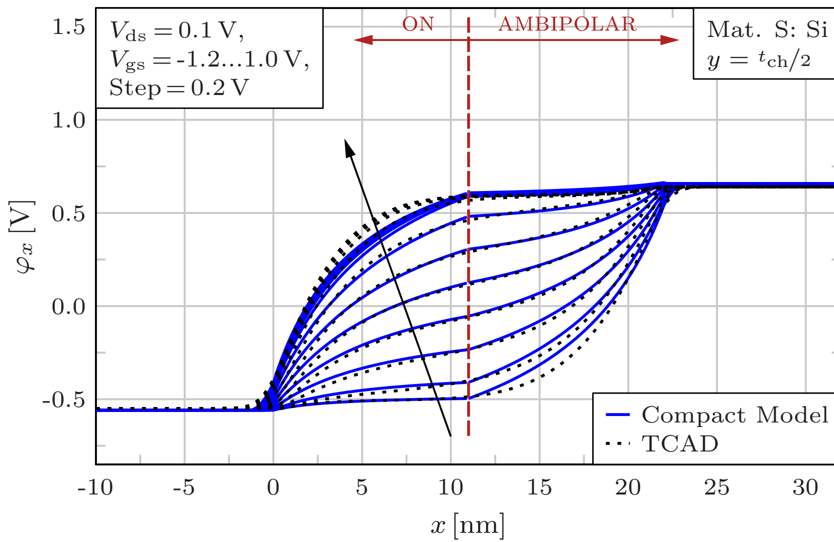


(b) $y = t_{ch}/2$.

Figure 6.3.: Electrostatic potential φ_x along the x-axis at $V_{ds} = 0.7\,V$ of the DG TFET at (a) the surface and (b) in the center of the device. The modeling results for the ON- and AMBIPOLAR-state are separately plotted and compared to TCAD data for various gate-source voltages V_{gs}.

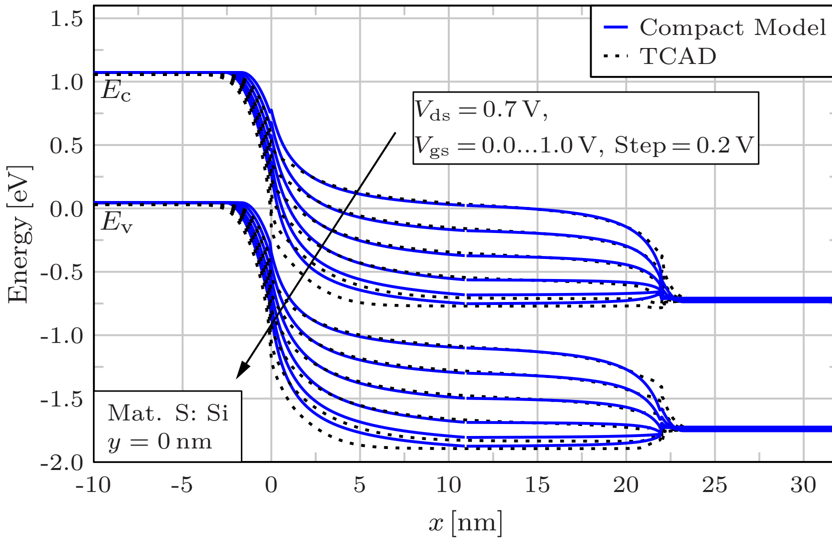


(a) $y = 0$ nm.

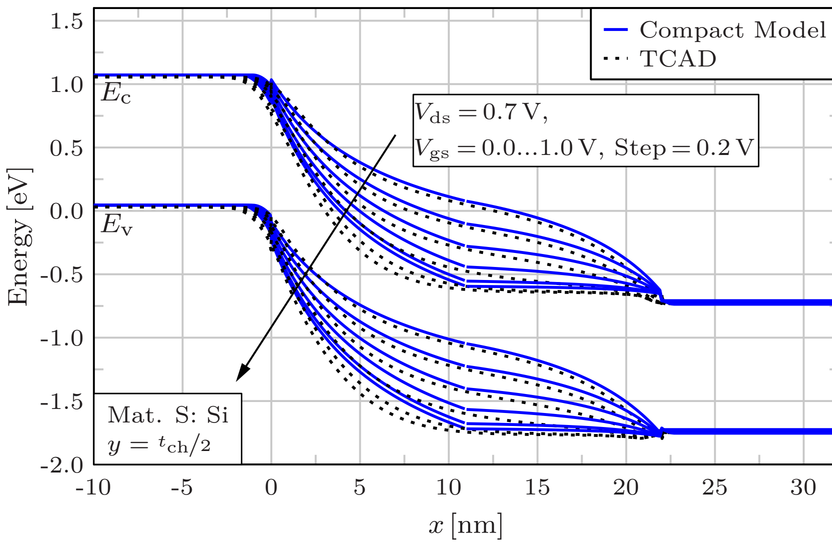


(b) $y = t_{ch}/2$.

Figure 6.4.: Potential solution along the x-axis of the DG TFET at (a) the surface and (b) in the channel of the device for an applied V_{ds} of 0.1 V. The compact model is compared to TCAD simulations for various V_{gs} values.

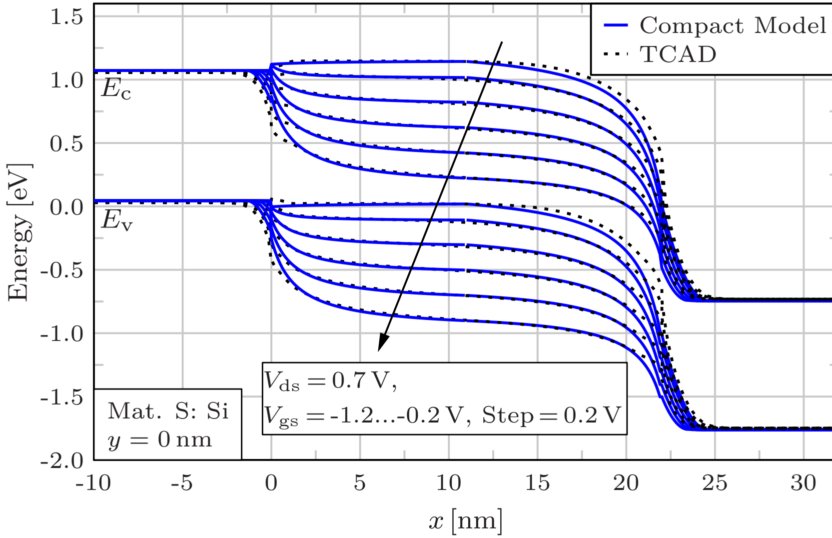


(a) $y = 0\,\text{nm}$.

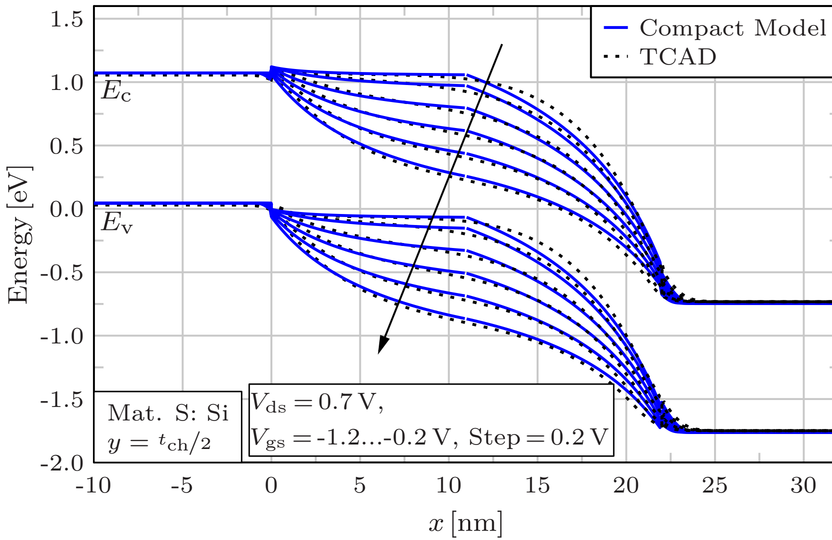


(b) $y = {}^{t_{ch}}/2$.

Figure 6.5.: Band diagram modeling results in the ON-state at $V_{ds} = 0.7\,\text{V}$ and various V_{gs} values are compared to TCAD simulations, where the results at the surface of the device are depicted in (a) and the results in the center of the device are illustrated in (b).

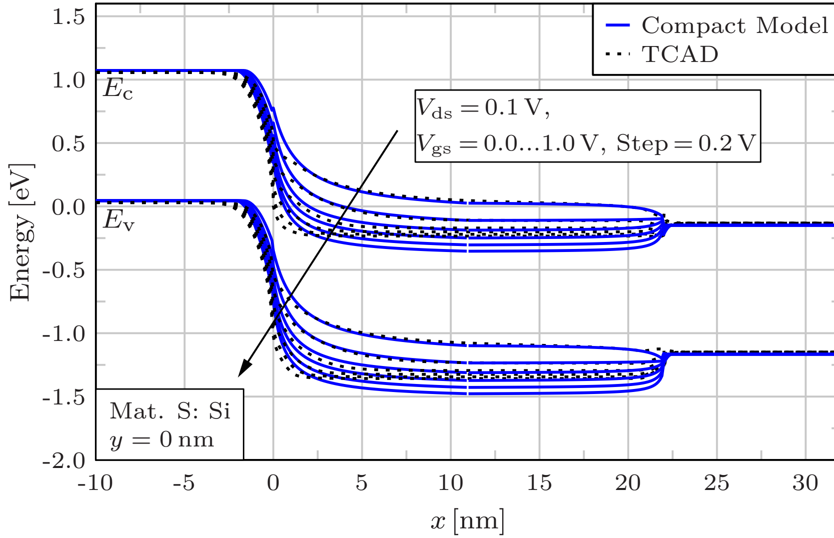


(a) $y = 0$ nm.

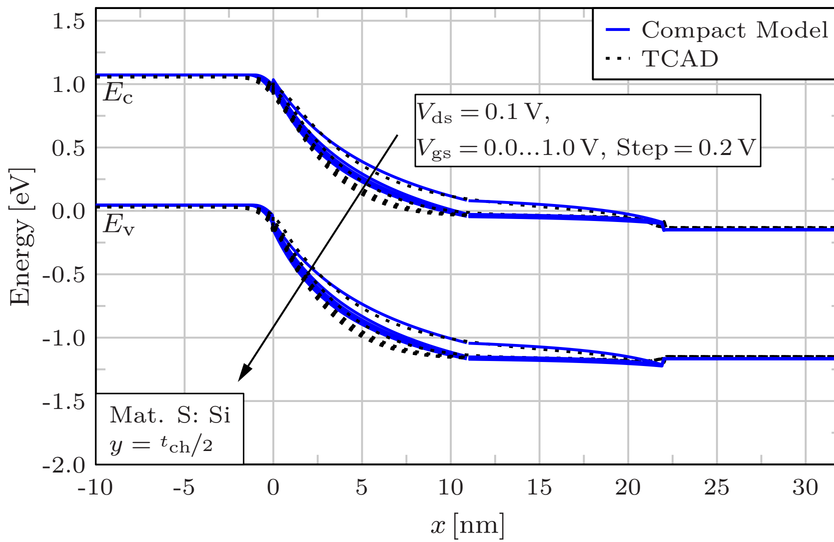


(b) $y = t_{ch}/2$.

Figure 6.6.: AMBIPOLAR-state band diagram for a drain-source voltage of 0.7 V and different V_{gs} values. (a) shows the modeling results at the device surface and (b) in the center of the device. In both cases the model is plotted against TCAD simulation data.

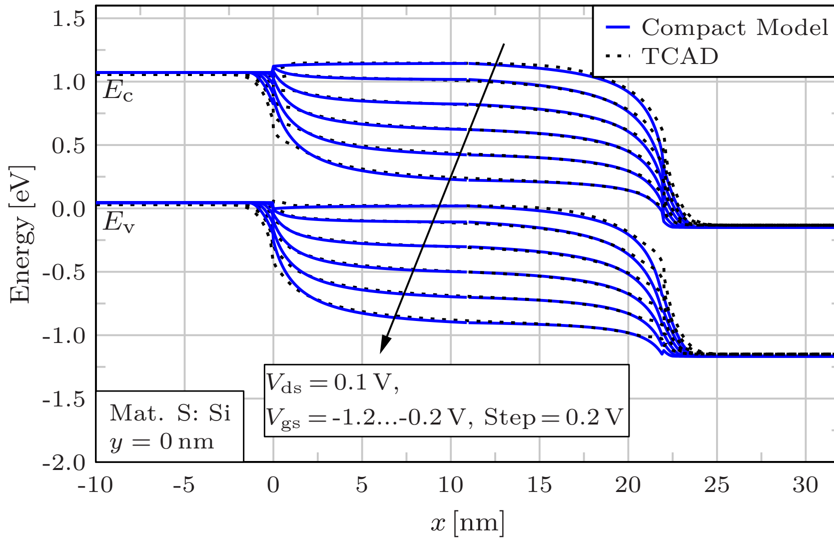


(a) $y = 0$ nm.

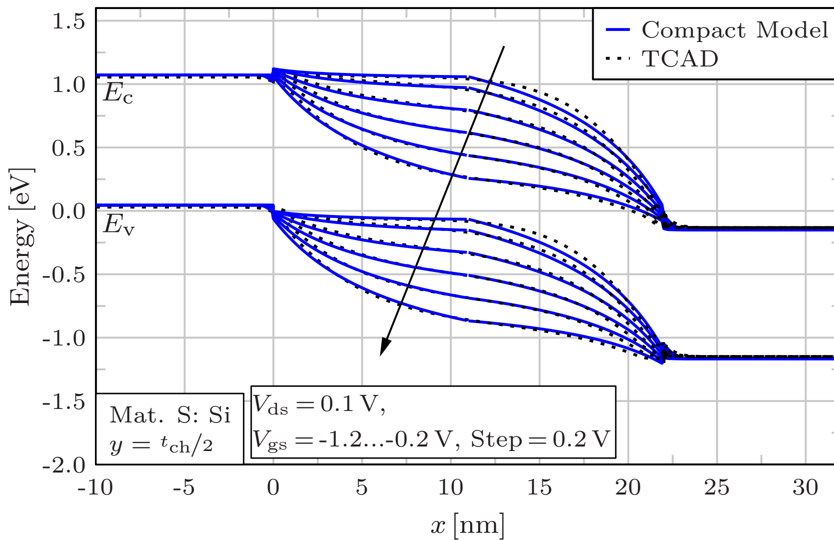


(b) $y = t_{ch}/2$.

Figure 6.7.: Band diagram in the TFET ON-state for various gate-source voltages and $V_{ds} = 0.1$ V at (a) the surface and (b) in the center. The results of the compact model are shown in comparison to numerical simulation data.

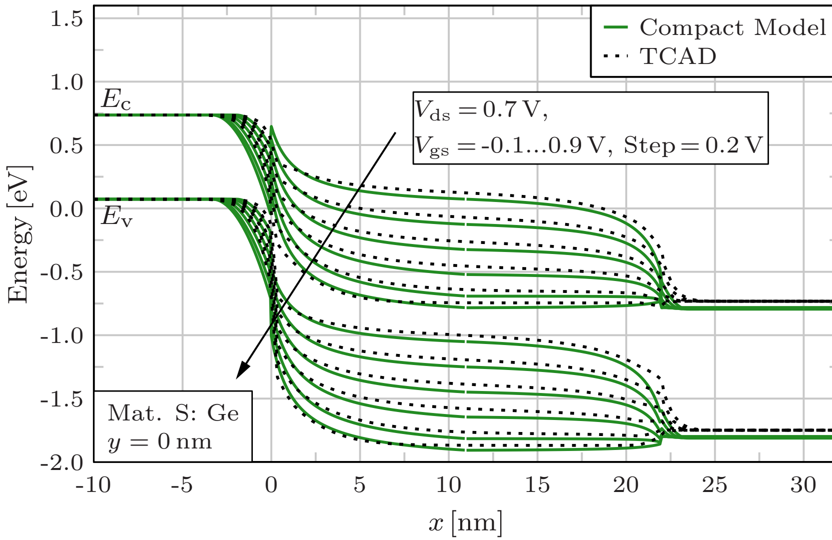


(a) $y = 0$ nm.

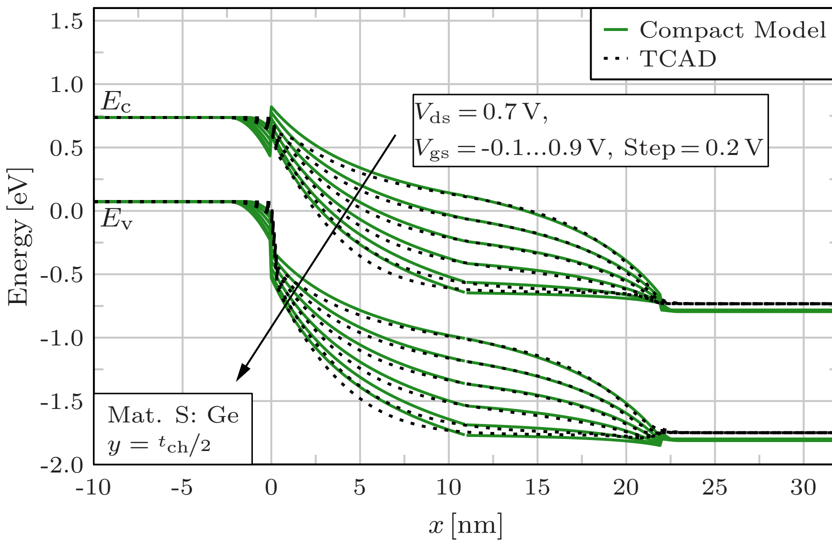


(b) $y = t_{ch}/2$.

Figure 6.8.: Compact band diagram at $V_{ds} = 0.1$ V, where (a) shows the results at the surface and (b) in the center of the TFET. The applied V_{gs} values indicate that the TFET is in the AMBIPOLAR-state.

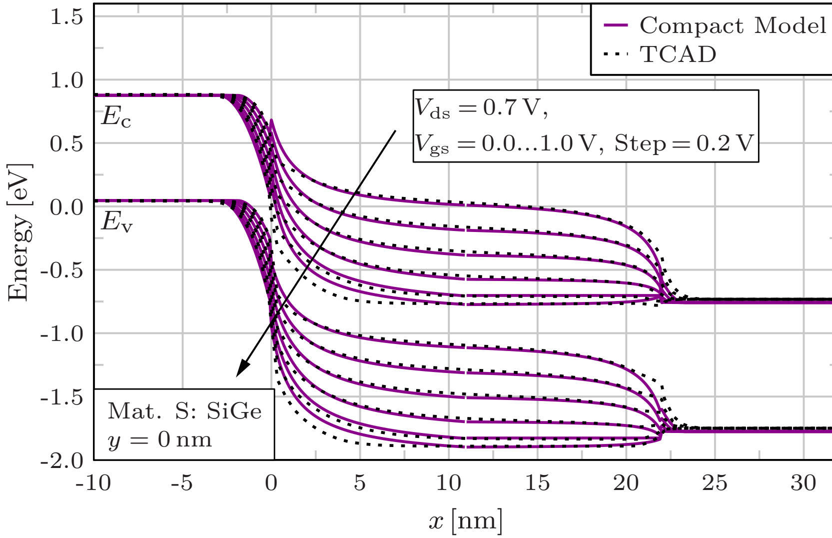


(a) $y = 0\,\mathrm{nm}$.

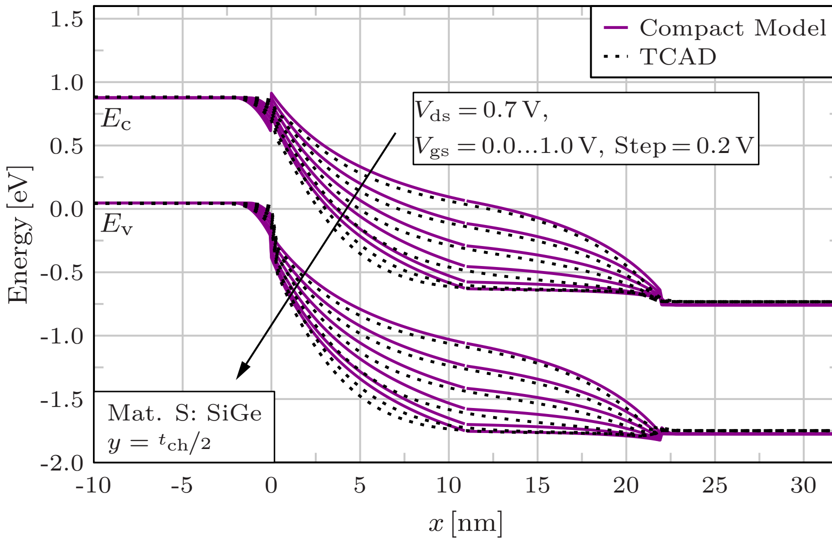


(b) $y = t_{ch}/2$.

Figure 6.9.: Band diagram of the Ge–Si hetero source-to-channel junction at (a) the surface and (b) in the center of the TFET. The modeling results are plotted versus TCAD simulations. The applied drain-source voltage is 0.7 V.

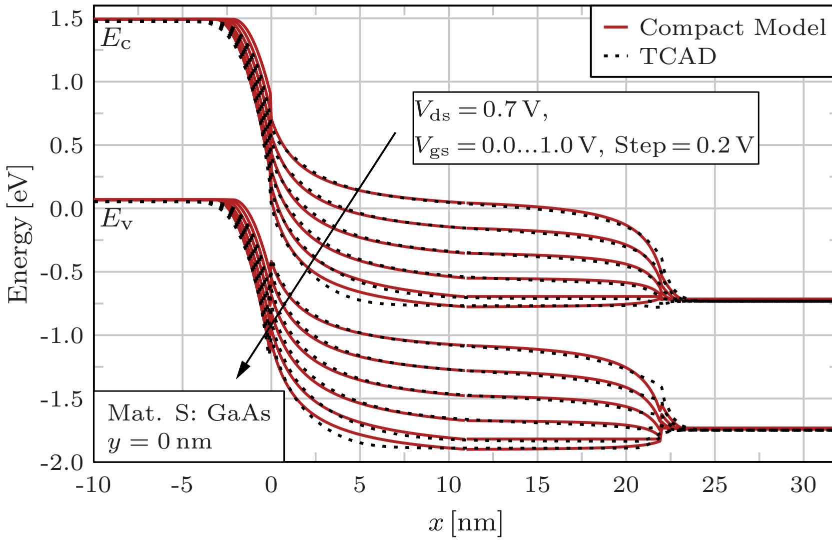


(a) $y = 0$ nm.

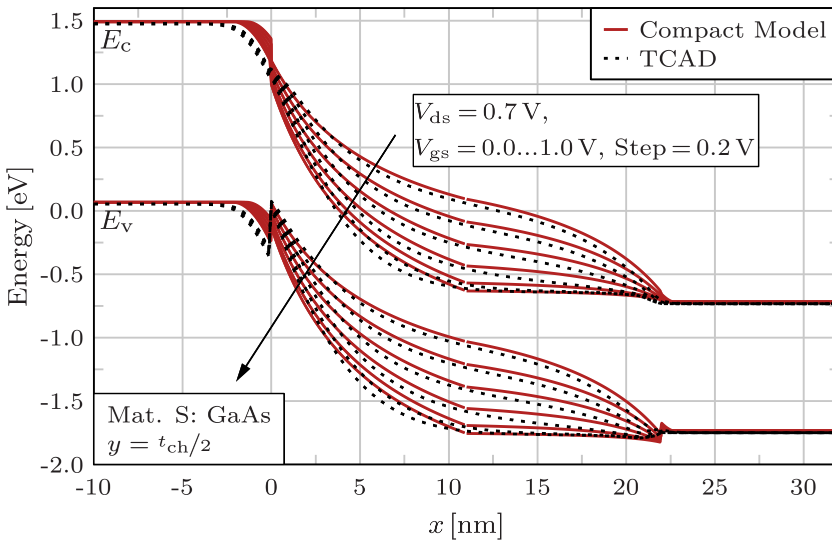


(b) $y = t_{ch}/2$.

Figure 6.10.: Compact model simulation results of a SiGe–Si source-to-channel junction for various V_{gs} values and $V_{ds} = 0.7$ V. The modeling results are plotted against TCAD data. (a) surface and (b) center of the TFET.



(a) $y = 0$ nm.



(b) $y = {}^{t_{ch}}/_{2}$.

Figure 6.11.: GaAs–Si hetero-junction band diagram for different V_{gs} and an applied drain-source voltage of 0.7 V. The compact model is verified by TCAD simulations, whereby the band diagram at the surface is shown in (a) and the center band diagram in (b).

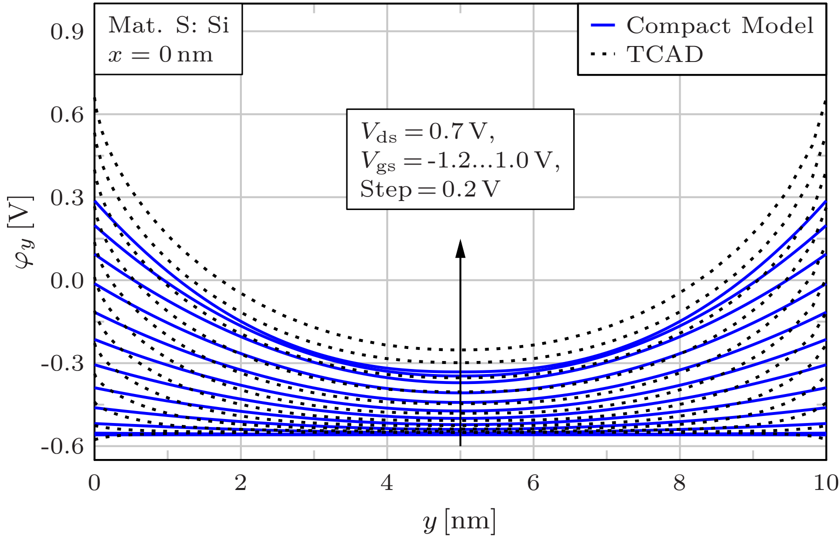


Figure 6.12.: Electrostatic potential along the y-axis at the source-to-channel junction ($x = 0\,\mathrm{nm}$) for $V_{\mathrm{ds}} = 0.7\,\mathrm{V}$ and various V_{gs} values. The compact model is compared to TCAD data.

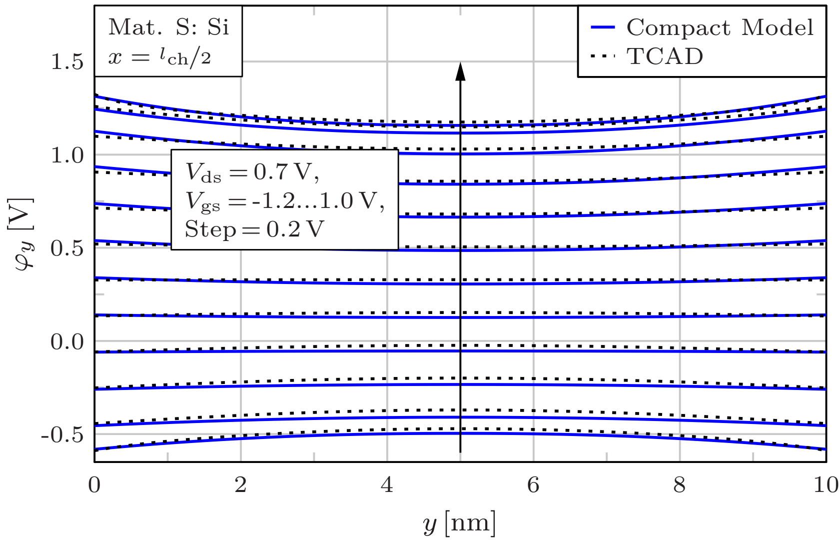


Figure 6.13.: Compact model results of the potential along the y-axis at $x = l_{\mathrm{ch}}/2$ and $V_{\mathrm{ds}} = 0.7\,\mathrm{V}$, which are plotted in comparison to TCAD simulations for various V_{gs} values. In this case, the needed potential values $\Phi^{\mathrm{s}}_{\mathrm{cen}}$ and $\Phi^{\mathrm{s}}_{\mathrm{sur}}$ to define φ_y are calculated with the help of Eq. (5.10).

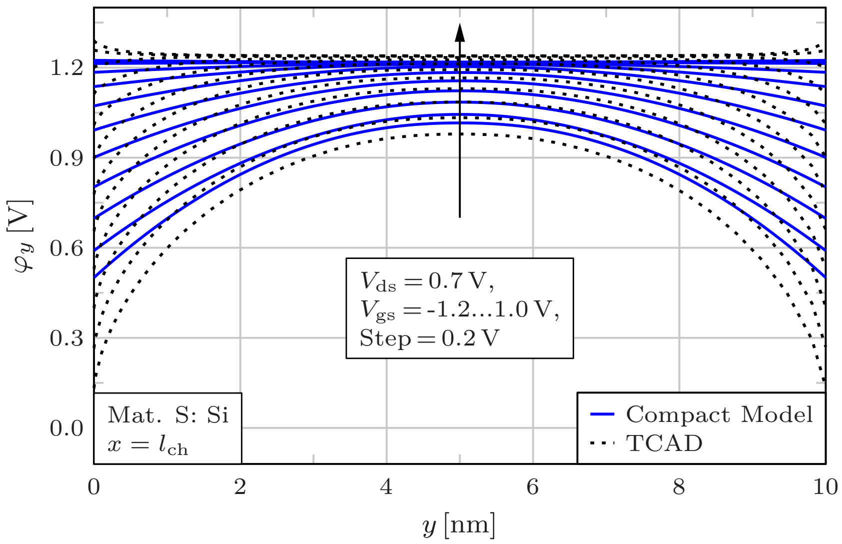
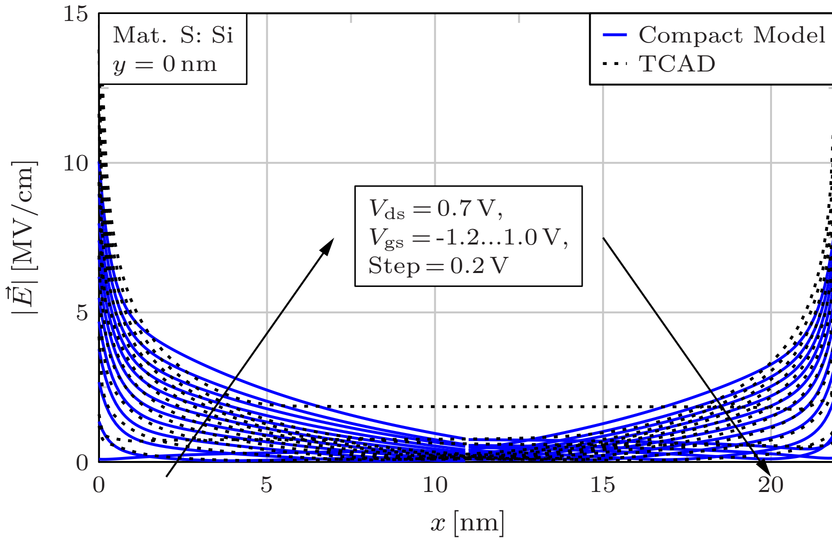
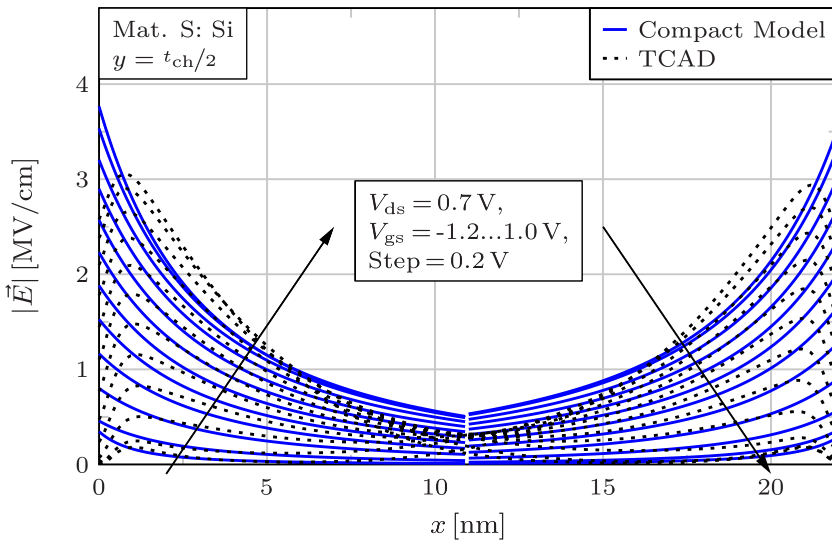


Figure 6.14.: Modeling results of the y potential at the drain-to-channel junction ($x = l_{\mathrm{ch}}$) for an applied V_{ds} of 0.7 V, which are plotted against TCAD simulation data.



(a) $y = 0\,\mathrm{nm}$.



(b) $y = t_{\mathrm{ch}}/2$.

Figure 6.15.: Electric field approximation for various V_{gs} values and $V_{\mathrm{ds}} = 0.7\,\mathrm{V}$ plotted along the x-axis. The modeling results at (a) the surface and (b) in the center of the channel are shown in comparison to TCAD simulations.

6.1.2 AE WKB Approach

The verification of the tunneling energy barrier can be done after demonstrating the validity of the compact modeling equations of the band diagram in the previous section. The tunneling energy barrier is determined by the AE WKB approach, which is derived in Sec. 5.4.2 for the B2B tunneling and in Sec. 5.5.2 for the TAT current part. Hereinafter, the accuracy of the tunneling energy barrier for B2B tunneling is examined. In doing so, Eqs. (5.73) and (5.74) are used to illustrate the approximated triangular energy barrier within the band diagram of the device at various external voltages. In literature, a quasi-2D approach for the WKB approximation assuming a triangular energy barrier shape was already published in [129]. In this approach, the tunneling barrier height U_{bar} was calculated in dependency of an analytical closed-form 2D electric field solution $\vec{E}_{\mathrm{2D}}$ [176], which is very time-consuming. Due to the facts that in the calculations of the 2D electric field solution the presence of inversion charges is neglected and the resulting barrier height depends only on the electric field at one single point, the quasi-2D approach is very sensitive to any inaccuracies. Therefore, this model is not appropriate for a robust compact model, but it can be used to demonstrate the advantages of the AE WKB approach in the following.

The first results for $V_{\mathrm{ds}} = 0.7\,\mathrm{V}$ and $y = 0\,\mathrm{nm}$ are presented in Fig. 6.16. At a gate-source voltage of 0.0 V shown in Fig. 6.16(a) it can be seen that the ConB in the channel region starts to overlap the ValB in source region and for this reason the maximum $x^{\mathrm{s}}_{\mathrm{B2B,max}}$ of the $\mathrm{TGR_{B2B}}$ approximation has its maximum close to $l_{\mathrm{ch}}/2$. The TFET is in the transition from the OFF- to the ON-state. For this special case, the triangular tunneling barrier shape is not very well suitable to reproduce the tunneling barrier formed by the band diagram. Nevertheless, in this case the tunneling length l_{tun} results in a high value and therefore, the tunneling probability anyhow tends to be very small. So, this occurring error can be accepted in the compact modeling purpose. By increasing the applied V_{gs} values to 0.5 V, 1.0 V and 1.5 V (see Fig. 6.16(b)–(d)), the band overlap area also increases. Now, the x-position $x^{s}_{\mathrm{B2B,max}}$ of the maximum TGR value can be found close to source-to-channel junction, the shape of the tunneling barrier formed by the band diagram becomes steeper and is very well approximable by the energy triangle of the AE WKB approach. In these cases, the tunneling energy barrier is reproduced well by the compact approach, whereby the quasi-2D approach overestimates the tunneling barrier height U_{bar} when inversion charges come into play ($V_{\mathrm{gs}} \geq 1\,\mathrm{V}$).

The results in the center of the channel for the same applied voltages as before are shown in Fig. 6.17. At the transition from the OFF- to the ON-state ($V_{\mathrm{gs}} = 0.0\,\mathrm{V}$), it can be seen that the bands have no overlap region, thus no B2B tunneling can occur and so no tunneling barrier height can be calculated ($U^{\mathrm{s}}_{\mathrm{bar}} = 0\,\mathrm{eV}$). In this special case, the AE WKB approach would result in a wrong $T^{\mathrm{s}}_{\mathrm{tun}} = 1$, hence if the bands have no overlap, the AE WKB approach smoothly sets the tunneling probability to 0. By increasing V_{gs} to ON-state values (see Fig. 6.17(b)–(d)), the AE WKB approximation shows a good match in comparison the tunneling barrier defined by

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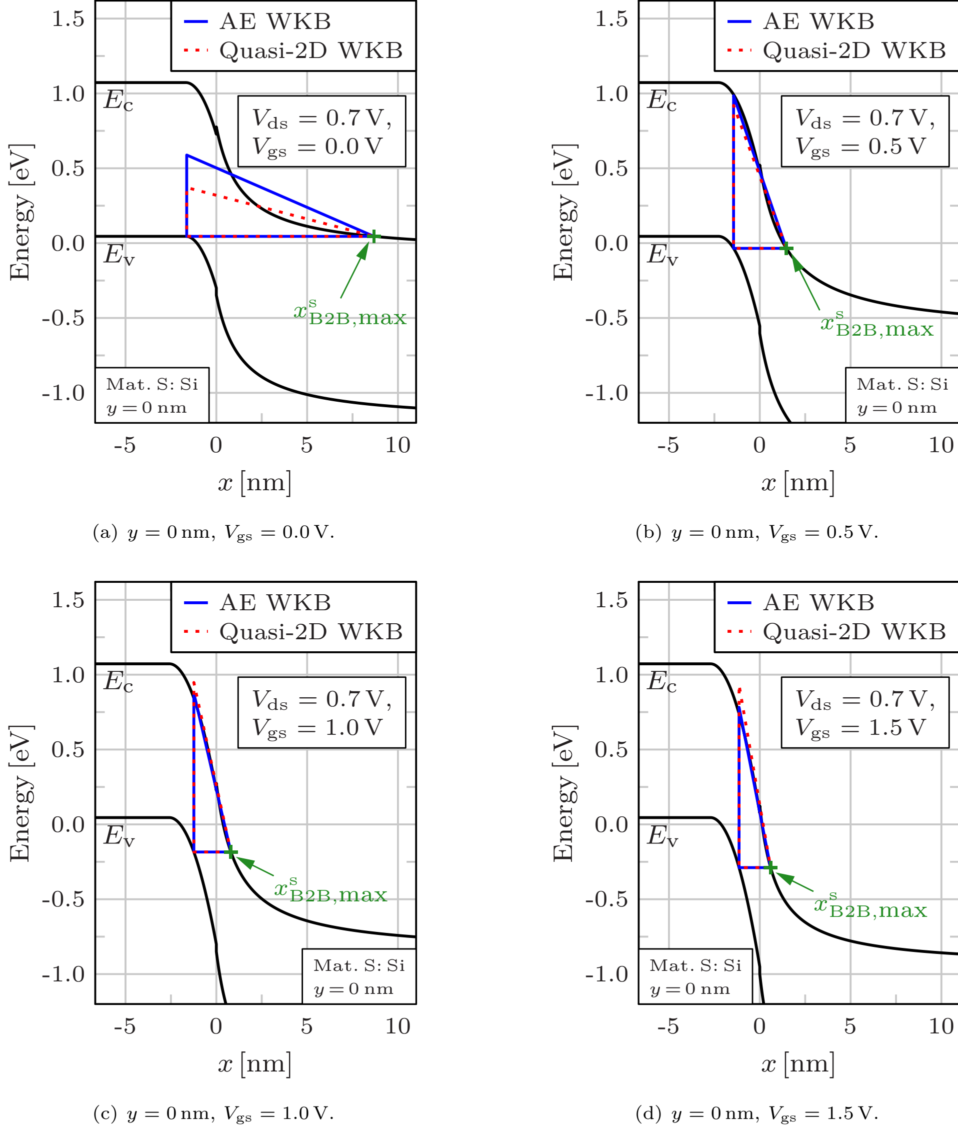
the band diagram. The quasi-2D WKB approach underestimates the tunneling barrier height U_{bar} in all cases, which consequently results in an overestimated tunneling probability.

Figure 6.18 illustrates the tunneling energy barrier at the channel surface for a reduced V_{ds} of 0.1 V. It can be seen that the AE WKB approach is able to cover the change in the drain-source voltage. In the TFET ON-state ($V_{\mathrm{gs}} = 0.5 \ldots 1.5\,\mathrm{V}$), the modeled energy barrier matches well in comparison the tunneling barrier formed by the band diagram. The deviations at $V_{\mathrm{gs}} = 0.0\,\mathrm{V}$ are to explain in the same manner than in Fig. 6.16(a).

The resulting tunneling energy barriers in the AMBIPOLAR-state of the TFET for various V_{gs} and V_{ds} values at $y = 0\,\mathrm{nm}$ are depicted in Fig. 6.19. Firstly, the validity of the AE WKB approach is investigated at $V_{\mathrm{ds}} = 0.7\,\mathrm{V}$, showing the results for $V_{\mathrm{gs}} = -0.5\,\mathrm{V}$ and $-1.0\,\mathrm{V}$ in Fig. 6.19(a) and (b), respectively. For the first gate-source voltage, a mismatch of the tunneling barrier height can be seen. At this bias, the TFET is at the transition from the OFF- to the AMBIPOLAR-state and the resulting T_{tun} tends to small amounts, so this occurring inaccuracy in the compact modeling approach is acceptable. The tunneling energy barrier is better reproduced at $V_{\mathrm{gs}} = -1.0\,\mathrm{V}$, where the TFET is in the AMBIPOLAR-state and the tunneling barrier shape defined by the band diagram is steeper and thus it can be approximated by a triangle. By reducing the applied V_{ds} to 0.1 V, the band overlap region at the drain-to-channel junction is reduced and the AMBIPOLAR-state is suppressed (see Sec. 3.3.5). For these reasons, the AE WKB approach is examined for $V_{\mathrm{gs}} = -1.0\,\mathrm{V}$ and $-1.5\,\mathrm{V}$, shown in Fig. 6.19(c) and (d). Here, one can see that the transition from OFF- to AMBIPOLAR-state takes place at the gate-source voltage of $-1.0\,\mathrm{V}$ and explains the underestimated tunneling barrier height in Fig. 6.19(c). The reduction of V_{gs} to $-1.5\,\mathrm{V}$ causes a better agreement of the modeled tunneling barrier and the one formed by band diagram.

In order to show the robustness and flexibility of the AE WKB approach, the resulting tunneling energy barriers in the hetero source-to-channel junctions are presented in Fig. 6.20. Simulations are performed at the channel surface for $V_{\mathrm{ds}} = 0.7\,\mathrm{V}$ and $V_{\mathrm{gs}} = 1.0\,\mathrm{V}$, so the TFET is in the ON-state. The Si TFET is shown in Fig. 6.20(a) as a reference. The tunneling barrier of the Ge–Si hetero-junction is depicted in Fig. 6.20(b) and it can be seen that the modeled tunneling barrier matches well in comparison to the barrier formed by the band diagram. Due to the lower band gap of Germanium and lower effective carrier mass, the resulting tunneling barrier height is lower than the one in Silicon. As a consequence, the tunneling probability and the device current increase for the same applied external voltages. A similar result is achieved in the investigations of a SiGe–Si hetero-junction shown in Fig. 6.20(c). In these two cases the quasi-2D approach overestimates the resulting tunneling barrier height and therefore underestimates the tunneling probability. In a last step, the source material is GaAs, which has a higher band gap E_{g} in comparison to Silicon. The tunneling energy barrier calculated by AE WKB approximation is shown in Fig. 6.20(d) and it can be seen that the model predicts the barrier defined by the bands very well with only a small overestimation of the amount. In

this case, the quasi-2D approach shows a better match to the tunneling barrier formed by the band diagram.



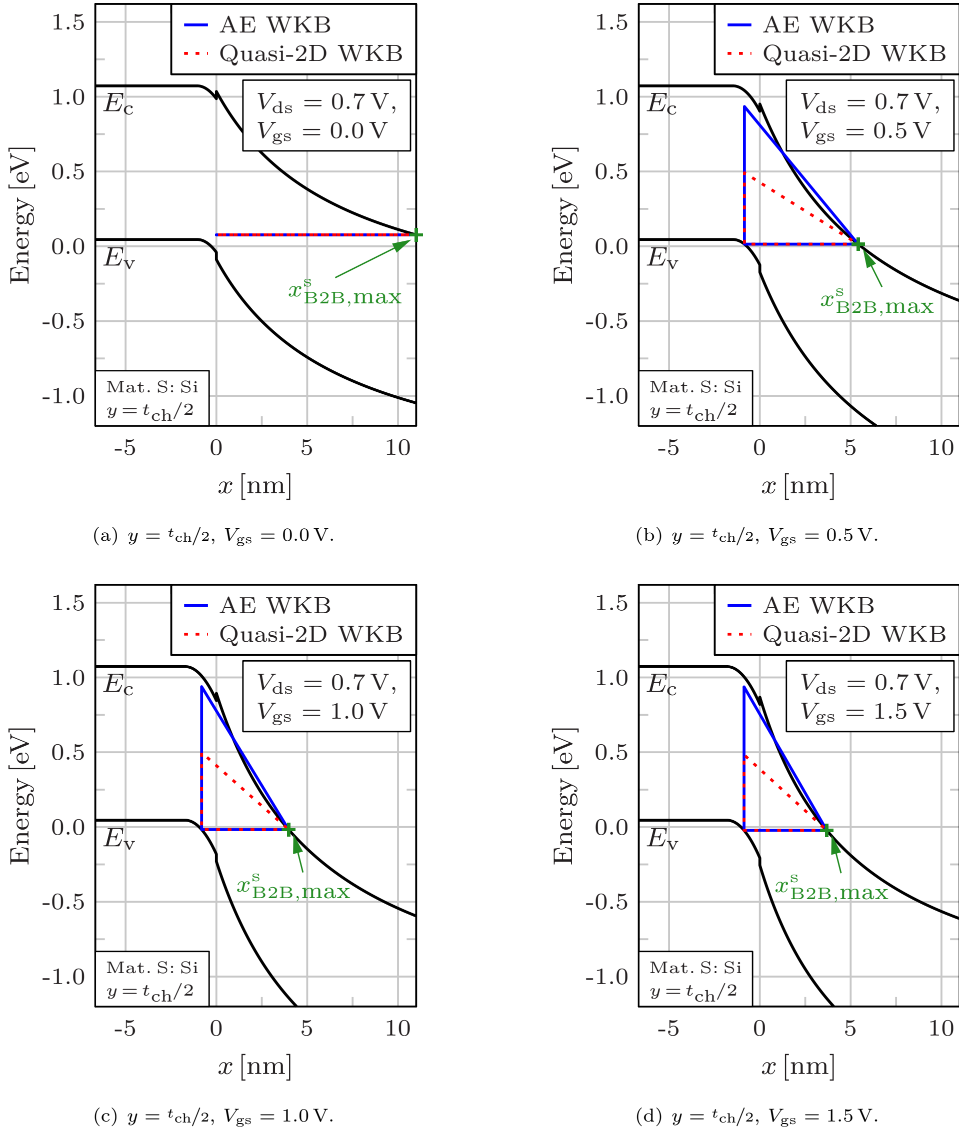
(a) $y = 0\,nm$, $V_{gs} = 0.0\,V$.

(b) $y = 0\,nm$, $V_{gs} = 0.5\,V$.

(c) $y = 0\,nm$, $V_{gs} = 1.0\,V$.

(d) $y = 0\,nm$, $V_{gs} = 1.5\,V$.

Figure 6.16.: Visualization of the AE WKB approach within the band diagram of the DG TFET at the surface of the channel region for $V_{ds} = 0.7\,V$. The applied V_{gs} in (a) is 0.0 V, (b) 0.5 V, (c) 1.0 V and 1.5 V in (d). In (a) the TFET is at the transition from the OFF- to the ON-state and in (b)-(d), the TFET is in the ON-state. The AE WKB approach is compared to a quasi-2D WKB approximation and the x-position of the maximum TGR_{B2B} value is highlighted by a green cross.



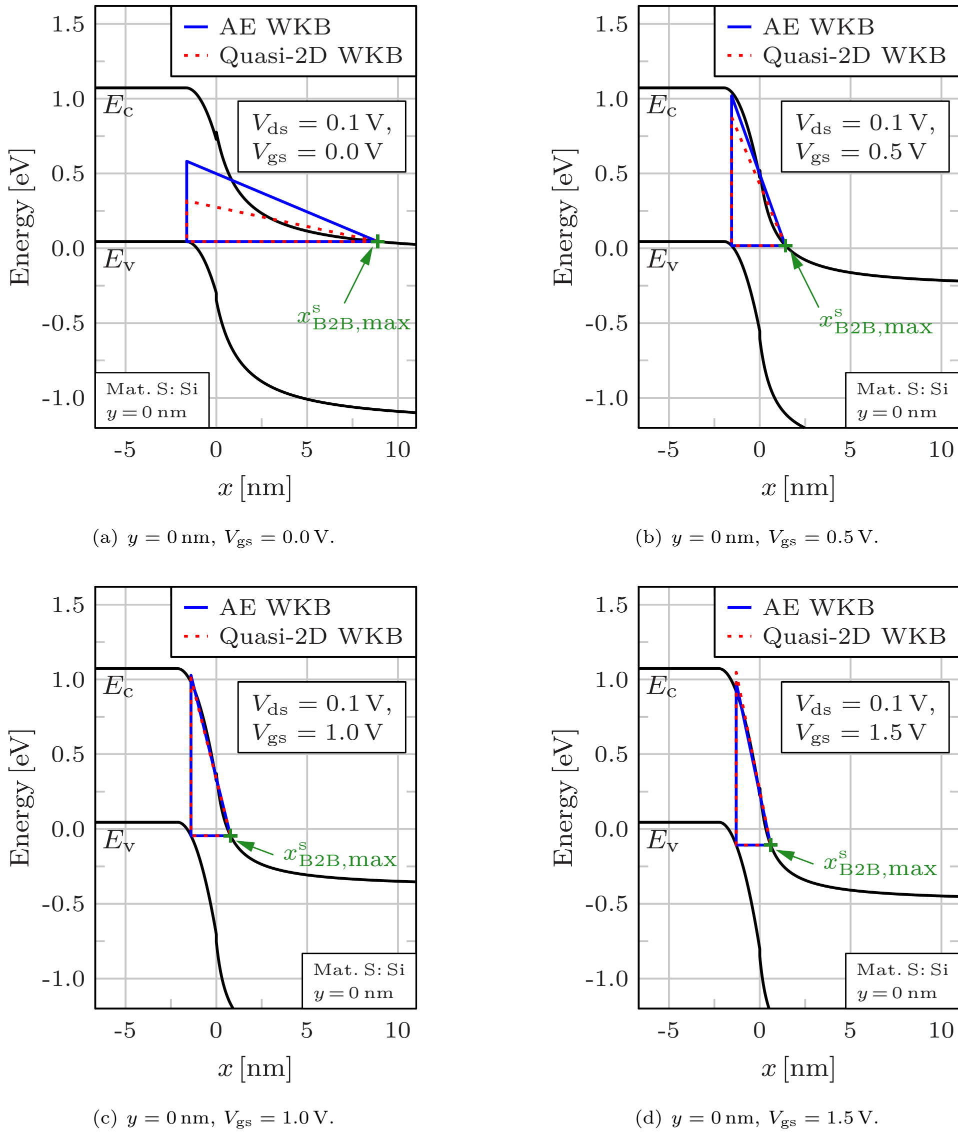
(a) $y = t_{ch}/2$, $V_{gs} = 0.0$ V.

(b) $y = t_{ch}/2$, $V_{gs} = 0.5$ V.

(c) $y = t_{ch}/2$, $V_{gs} = 1.0$ V.

(d) $y = t_{ch}/2$, $V_{gs} = 1.5$ V.

Figure 6.17.: AE WKB visualization in the center of the channel region ($y = t_{ch}/2$) for the same simulation setup shown in Fig. 6.16.



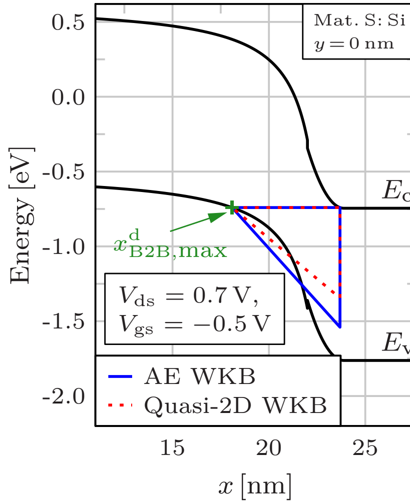
(a) $y = 0$ nm, $V_{gs} = 0.0$ V.

(b) $y = 0$ nm, $V_{gs} = 0.5$ V.

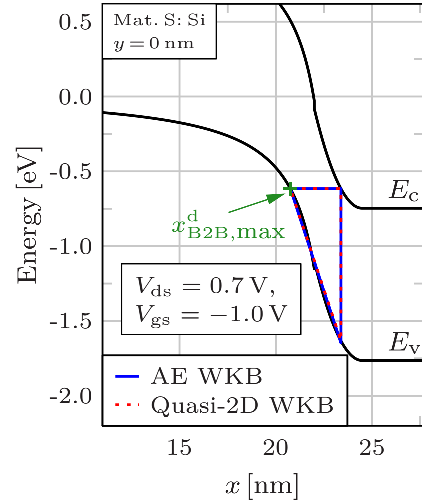
(c) $y = 0$ nm, $V_{gs} = 1.0$ V.

(d) $y = 0$ nm, $V_{gs} = 1.5$ V.

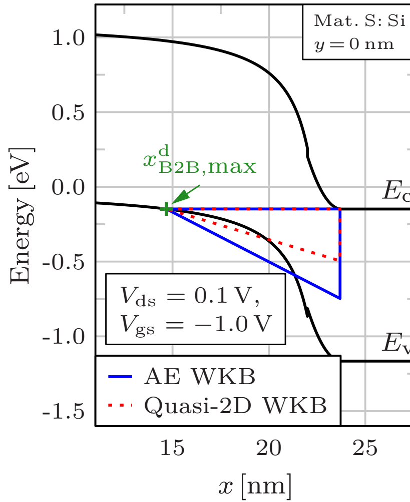
Figure 6.18.: Illustration of the resulting tunneling barrier at the channel surface using the AE WKB approach, examined for a drain-source voltage of $V_{ds} = 0.1$ V. The gate-source voltage is varied from 0.0 V in (a) to 1.5 V in (d) with a stepping of 0.5 V. The AE WKB approach is compared to a quasi-2D approximation.



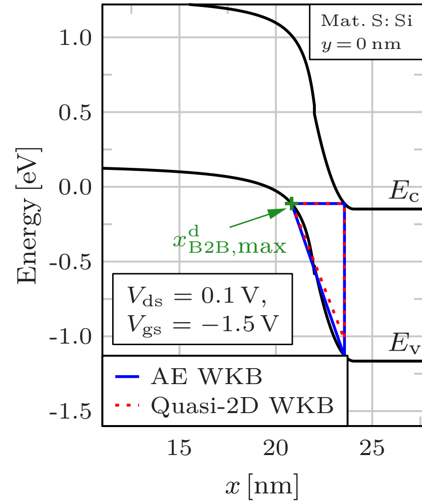
(a) $V_{ds} = 0.7\,\mathrm{V}$, $V_{gs} = -0.5\,\mathrm{V}$.



(b) $V_{ds} = 0.7\,\mathrm{V}$, $V_{gs} = -1.0\,\mathrm{V}$.

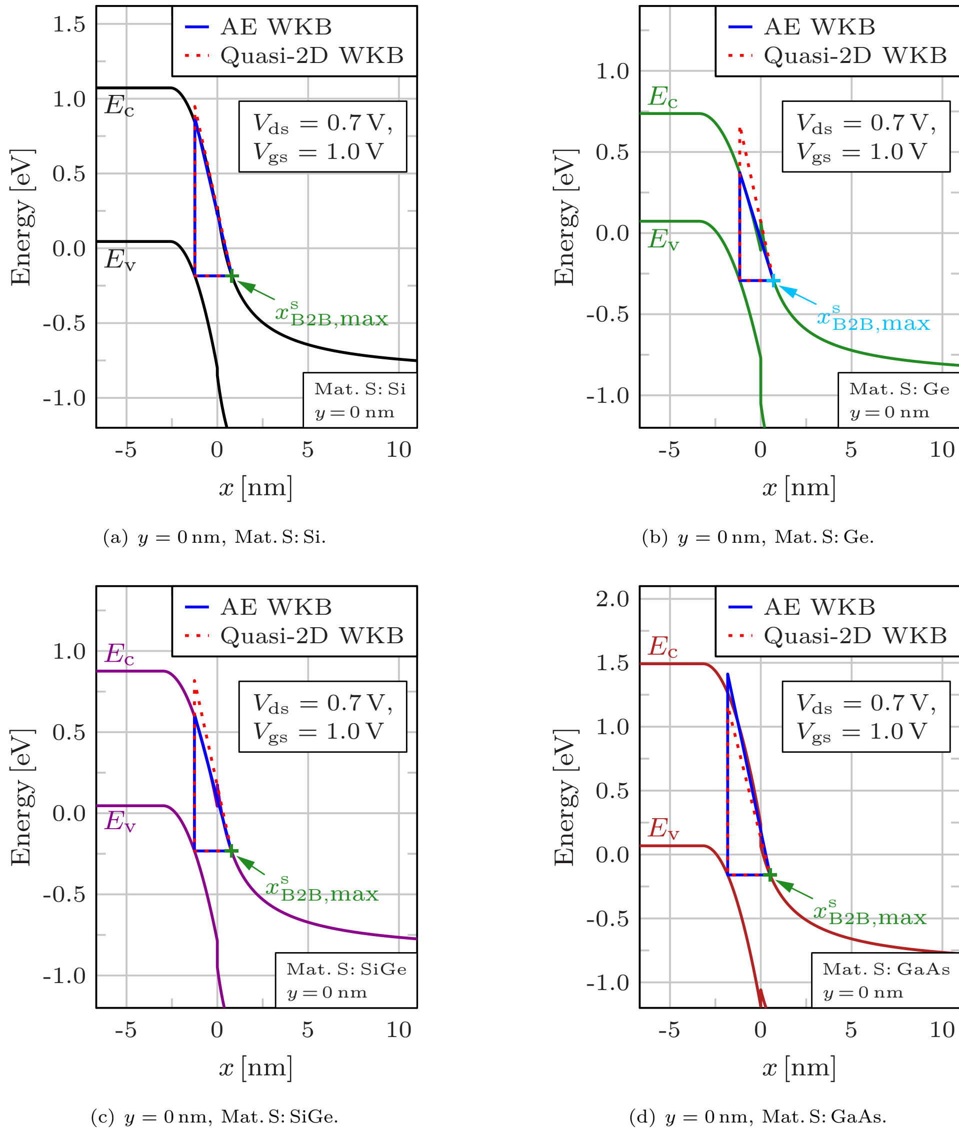


(c) $V_{ds} = 0.1\,\mathrm{V}$, $V_{gs} = -1.0\,\mathrm{V}$.



(d) $V_{ds} = 0.1\,\mathrm{V}$, $V_{gs} = -1.5\,\mathrm{V}$.

Figure 6.19.: AMBIPOLAR-state AE WKB modeling results at $y = 0\,\mathrm{nm}$, which are compared to a quasi-2D approach. (a): $V_{ds} = 0.7\,\mathrm{V}$ and $V_{gs} = -0.5\,\mathrm{V}$. (b): $V_{ds} = 0.7\,\mathrm{V}$ and $V_{gs} = -1.0\,\mathrm{V}$. (c): $V_{ds} = 0.1\,\mathrm{V}$ and $V_{gs} = -1.0\,\mathrm{V}$. (d): $V_{ds} = 0.1\,\mathrm{V}$ and $V_{gs} = -1.5\,\mathrm{V}$.



(a) $y = 0\,\mathrm{nm}$, Mat. S: Si.
(b) $y = 0\,\mathrm{nm}$, Mat. S: Ge.
(c) $y = 0\,\mathrm{nm}$, Mat. S: SiGe.
(d) $y = 0\,\mathrm{nm}$, Mat. S: GaAs.

Figure 6.20.: Visualization of the AE WKB approach for various materials of the source region, simulated at $V_\mathrm{ds} = 0.7\,\mathrm{V}$ and $V_\mathrm{gs} = 1.0\,\mathrm{V}$. The source material in (a) is Si, (b) Ge, (c) SiGe and GaAs in (d). The resulting tunneling barrier is shown in comparison to a quasi-2D WKB approach.

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6.1.3 Tunneling Generation Rate

In the next verification step, the tunneling generation rate for the B2B tunneling part is examined. The calculations of the TGR_{B2B} are done with the help of Eq. (5.75) in order to show the validity of the derived expression for the current density. Furthermore, the TGR is used to verify the AE WKB approach shown in previous section by numerical TCAD simulations, because in TCAD Sentaurus the transmission coefficient cannot be displayed. The TCAD tunneling generation rate for B2B tunneling is denoted as *eBarrierTunneling* and *hBarrierTunneling* for electrons and holes, respectively. The compact model simulations are performed with the parameters listed in Tab. 6.2 to obtain a correct device current, thus some deviations to TCAD data can occur in verification process of the TGR.

Figure 6.21 presents the results of the TGR in the ON-state of the TFET for an applied V_{ds} of 0.7 V and a V_{gs} range from 0.3 V to 0.6 V. The TGR modeling results at the surface of the channel are shown in Fig. 6.21(a) in comparison to the extracted *eBarrierTunneling* values from TCAD simulations. It can be seen that the shape and the amount of the modeled TGR matches very well with TCAD data, whereby a horizontal displacement along the x-axis can be observed. This mismatch can be explained by the inaccuracies in the compact band diagram and thus by the chosen fitting parameter $\lambda_{\text{fit}}^{\text{s}}$. It should be noted that the horizontal displacement has no influence on the resulting B2B current density, which is obtained by integration. The TGR in the channel center is shown in Fig. 6.21(b), examined for the same applied voltages as at the surface. Here, the amount of TGR is significantly underestimated, which is to explain by the applied adjustable parameter to obtain an accurate I_{ds}. In the verification of the modeled band structure (see Fig. 6.5(b)) one can see some small deviations that cause an overestimated value for the tunneling length l_{tun} and hence an underestimated tunneling probability since $T_{\text{tun}} \propto \exp(-l_{\text{tun}})$. In addition, the inaccuracies of the electric field in the channel center may cause consequential errors. Nevertheless, the TGR in the center of the channel is three orders of magnitude smaller than the surface TGR and thus, the contribution to the resulting B2B current density is small. It is to say that these inaccuracies in the center are tolerable in the entire current calculations.

The ON-state TGR at the surface of the TFET with a reduced applied V_{ds} of 0.1 V and the same V_{gs} values as before is illustrated in Fig. 6.22(a). It can be seen that the shape is well reproduced but a deviation in the amount and x-position can be investigated. As mentioned before, the horizontal displacement has no influence on the integration to obtain the current density. The error in the amount is due to the fitting parameter $\lambda_{\text{fit}}^{\text{s}}$.

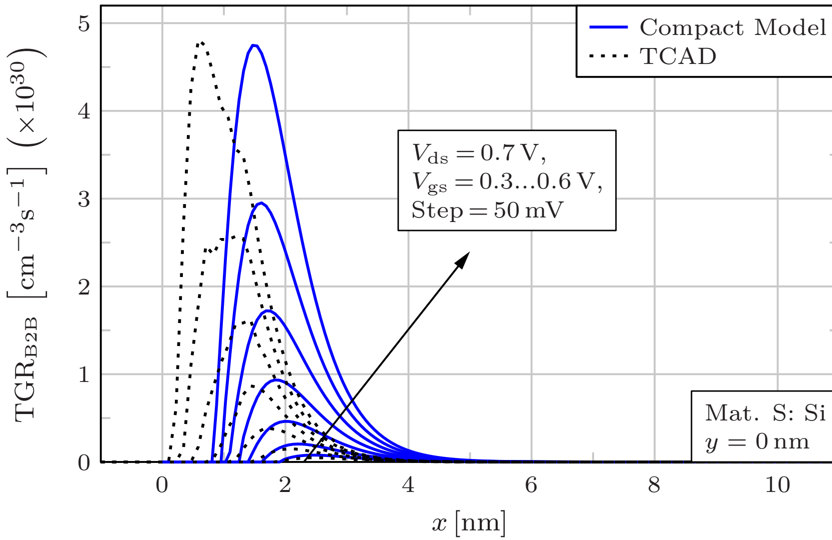
The extracted *hBarrierTunneling* values from TCAD are compared to the compact model in order to validate the TGR in the AMBIPOLAR-state of the device as it is presented in Fig. 6.22(b). The comparison shows the modeling results at $y = 0\,\text{nm}$ and $V_{\text{ds}} = 0.7\,\text{V}$. In the whole V_{gs} range from $-0.7\,\text{V}$ to $-1.0\,\text{V}$ the amount of TGR is underestimated which is the cause of the errors appearing in the calculations of the electric field as well as the band diagram. The chosen

adjustable parameter $\lambda_{\text{fit}}^{\text{d}} = 1.39$ also reduces the amount of the TGR in the AMBIPOLAR-state.

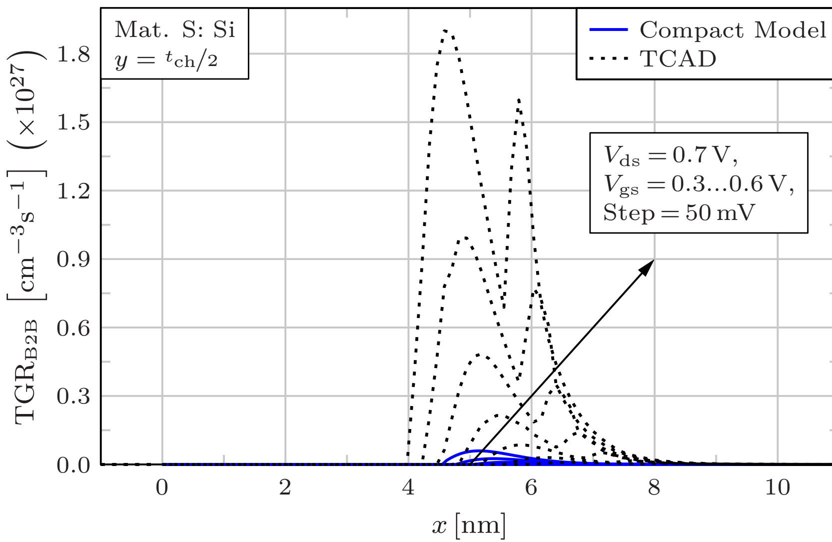
In the following, the source material is changed to a combination that forms a hetero-junction and the validity of the compact model is investigated. In Fig. 6.23, the results of the TGR at the channel surface of a Ge–Si hetero-junction in the TFET ON-state are depicted. It can be seen that also in this case the amount of the modeled TGR does not match with the TCAD simulation. The reasons for that can be found in the applied model parameters (see Tab. 6.2). For instance, the effective electron mass m_{s}^{*} is increased in comparison with the value $m_{\text{e,TCAD}}^{*}$ used in TCAD simulations to obtain a correct device current I_{ds}. If the TCAD value had been applied to the compact model, then the TGR would have resulted in the correct amount, but in this case it is not possible to achieve a good fit in I_{ds}.

An investigation of the SiGe–Si hetero-junction, which is depicted in Fig. 6.24, shows the same deviations at $y = 0\,\text{nm}$ in the amount of the TGR as in the aforementioned results. The reasons for the underestimated compact model TGR amount is the used effective electron mass m_{s}^{*} in combination with the applied parameter $\lambda_{\text{fit}}^{\text{s}}$. Nevertheless, using the parameters listed in Tab. 6.2 leads to a good fit in the current characteristics, which are shown in the next section.

The last examined source material is GaAs. The compact modeling results of this hetero-junction are presented in Fig. 6.25 and are compared to TCAD simulations. The results are obtained at the channel surface and the compact model shows a good match in the amount and x-placement in comparison to numerical data. Only small deviations occur in the part when the TGR starts to decrease again ($x \geq 2\,\text{nm}$). This is again a consequence of the chosen value of the parameter $\lambda_{\text{fit}}^{\text{s}}$, but in this case has only a minor impact on the resulting tunneling current density.

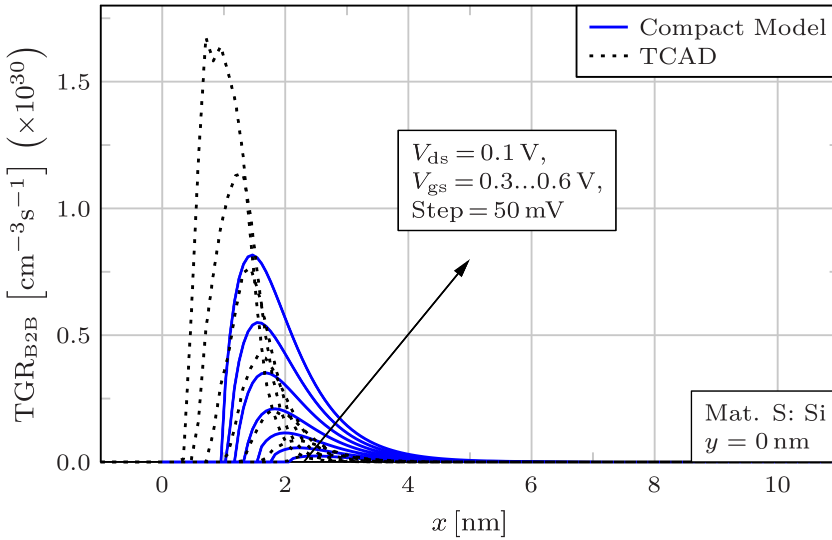


(a) $y = 0\,nm$.

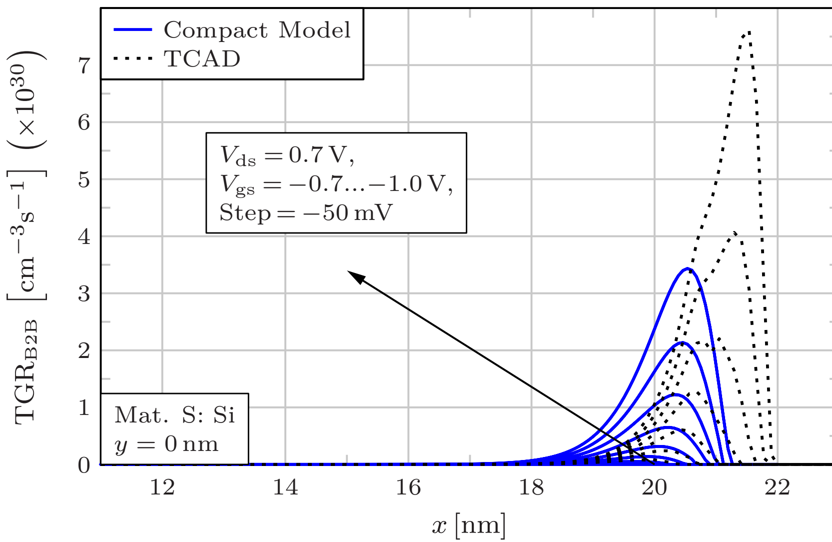


(b) $y = t_{ch}/2$.

Figure 6.21.: Compact model results of the TGR_{B2B} in the ON-state of the TFET at $V_{ds} = 0.7\,V$ and various gate-source voltages. (a) illustrates the results at the surface and (b) the results in the center of the device in comparison to TCAD data.



(a) ON-state.



(b) AMBIPOLAR-state.

Figure 6.22.: (a) ON-state B2B tunneling generation rate at $y = 0$ nm and $V_{ds} = 0.1$ V. (b) $\mathrm{TGR_{B2B}}$ in the AMBIPOLAR-state simulated at the surface of the TFET and $V_{ds} = 0.7$ V. Both result plots are simulated for various V_{gs} values and compared to numerical simulation results.

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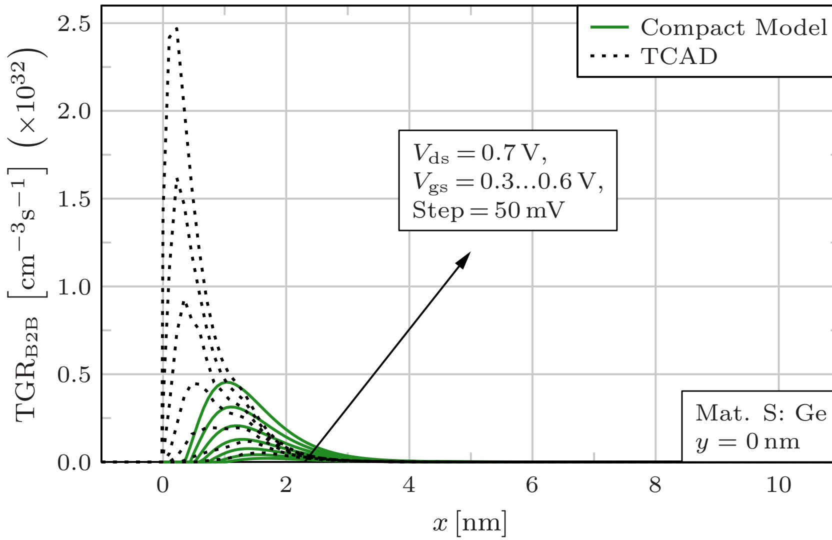


Figure 6.23.: Modeling results of the TGR^{s}_{B2B} of a Ge–Si hetero-junction at $y = 0\,nm$, an applied drain-source voltage of 0.7 V and various V_{gs} values. The compact model is shown in comparison with TCAD data.

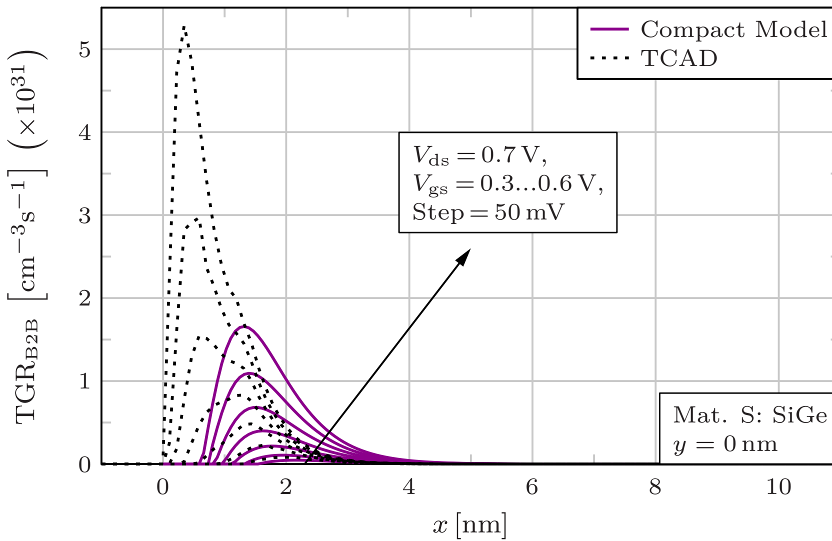


Figure 6.24.: SiGe–Si source-to-channel junction B2B tunneling generation rate in comparison to TCAD simulations. The simulation setup is the same as in Fig. 6.23.

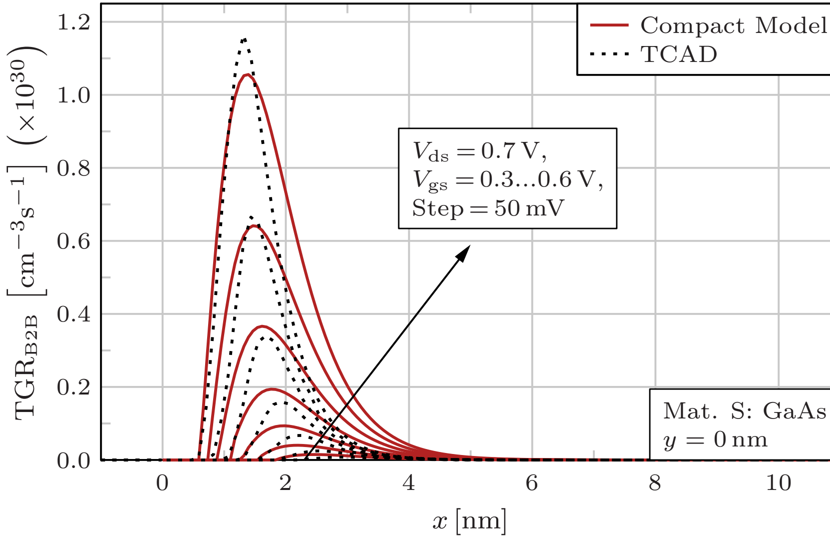


Figure 6.25.: Resulting B2B tunneling generation rate of the GaAs–Si hetero-junction at the surface of the channel for $V_{ds} = 0.7$ V and various V_{gs}. The compact model is compared to TCAD simulations.

6.1.4 Tunneling Current

In the last verification step by TCAD simulations, the tunneling current characteristics are under investigation, which is the most important step from a compact DC modeling point of view. At first, the current output characteristics and its first two derivatives are studied and verified by TCAD simulations. After that, the gate-source voltage V_{gs} is chosen as the sweep variable in order to prove the accuracy in terms of the current transfer characteristics and its first two derivatives. Finally, the TFET parameters, e.g. device dimensions, device materials or doping concentrations are varied to show and verify the flexibility of the compact DC modeling approach. The compact tunneling current I_{ds}, which considers both the B2B tunneling and TAT effect, is calculated with the help of Eq. (5.124) and by applying the parameters listed in Tab. 6.2.

Output I-V Characteristics and Derivatives

The current output curves of the DG TFET are illustrated in Fig. 6.26, where (a) shows the output I-V curves in the ON-state for various positive V_{gs} values and (b) the results of negative applied V_{gs}, where the TFET is in the AMBIPOLAR-state. In the ON-state output curve, the compact model stays in good agreement with the TCAD simulations in the shown V_{gs} range. The exponential increase of $I_{ds} \propto T_{tun}$, in case when no inversion charges exist, is very well reproduced by the modeling approach. The current starts to saturate when the inversion

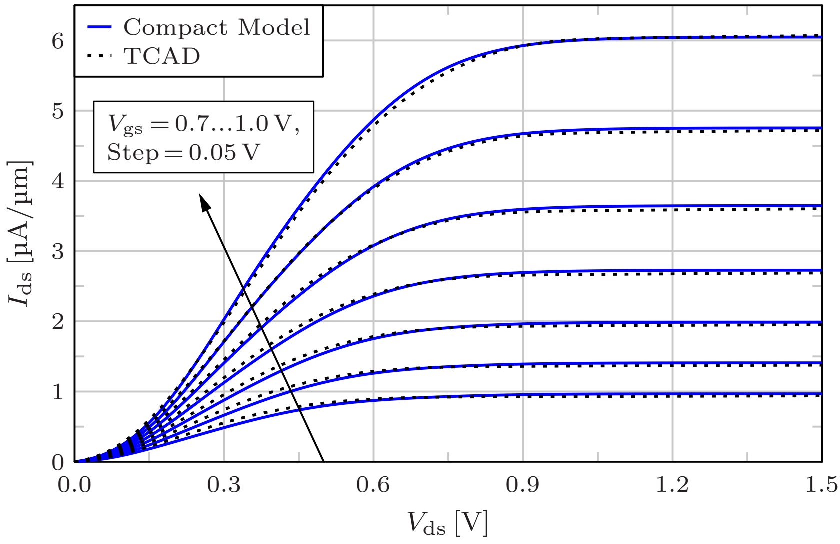
charges come into play as a consequence of the channel potential pinning (see Sec. 3.3.4).

In the AMBIPOLAR-state output curve (see Fig. 6.26(b)), one can see an exponential increase of I_{ds} over the whole applied V_{ds} range. In this case, B2B tunneling occurs at the drain-to-channel junction and at a fixed $V_{\mathrm{gs}} < 0$ no channel potential pinning can occur. Therefore, the effect of inversion charges does not play a role in this operating area of the TFET. The comparison to the reference data obtained by TCAD simualtions shows a good agreement.

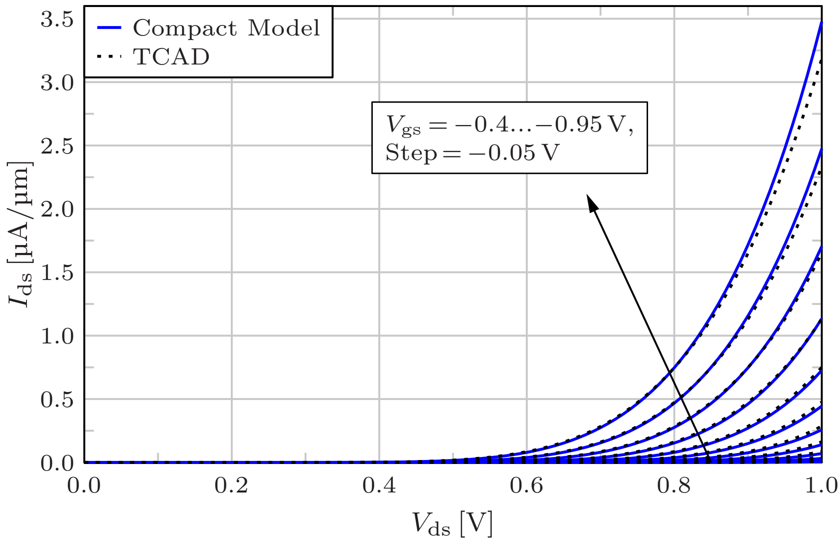
A very important aspect in the compact modeling is the numerical stability of the device current I_{ds} and for this reason the first two derivatives of I_{ds} with respect to V_{ds} are examined in the following. The ON-state output conductance $g_{\mathrm{ds}} = \partial I_{\mathrm{ds}}/\partial V_{\mathrm{ds}}$ is presented in Fig. 6.27(a). It can be seen that no kinks or any discontinuities appear in the first derivative. In addition, the compact model derivative shows a good agreement to the derivation extracted from TCAD data. An equally good match with TCAD simulations is achieved in the output conductance in the AMBIPOLAR-state, which is presented in Eq. (6.27(b)). In this plot, also no discontinuities occur in the whole V_{gs} range from $-0.4\,\mathrm{V}$ to $-0.95\,\mathrm{V}$ and the first derivative also follows an exponential shape.

Evaluating the second derivative of the output I-V curve is a next step to demonstrate the numerical robustness of the compact DC modeling approach. Therefore, the second derivative in the ON-state in the same applied V_{gs} range is depicted in Fig. 6.28(a). The results of the compact model show again no discontinuities or any kinks and are very consistent with the simulated results in TCAD Sentaurus. But at V_{ds} values from $0.3\,\mathrm{V}$ to $0.45\,\mathrm{V}$ one can see some extraordinary change in the slope of the curve, which can be interpreted as an inflection point. Here, the effect of inversion charges comes into play and shows some vulnerabilities of the modeling approach. This inaccuracy has no impact on simulating basic TFET circuits and is shown in Chap. 7. Figure 6.28(b) shows the second derivative of I_{ds} with respect to V_{ds} in the TFET AMBIPOLAR-state and one can see that the model is continuous in this operation regime of the TFET and fits well.

The presented continuity of the compact DC model in terms of the output characteristics is the first step for a usage of the model in circuit simulations. However, the continuity regarding the transfer I-V characteristics must still be checked, which is done in the next section.



(a) ON-state.



(b) AMBIPOLAR-state.

Figure 6.26.: Output I-V characteristics of the n-type DG TFET for (a) the ON- and (b) the AMBIPOLAR-state of the device. Simulations are performed for various V_{gs} values and compared to TCAD Sentaurus simulations.

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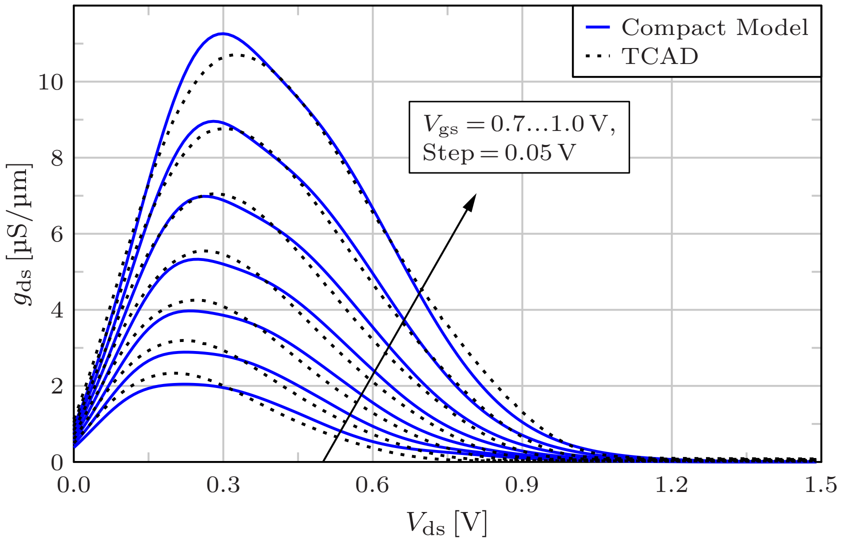
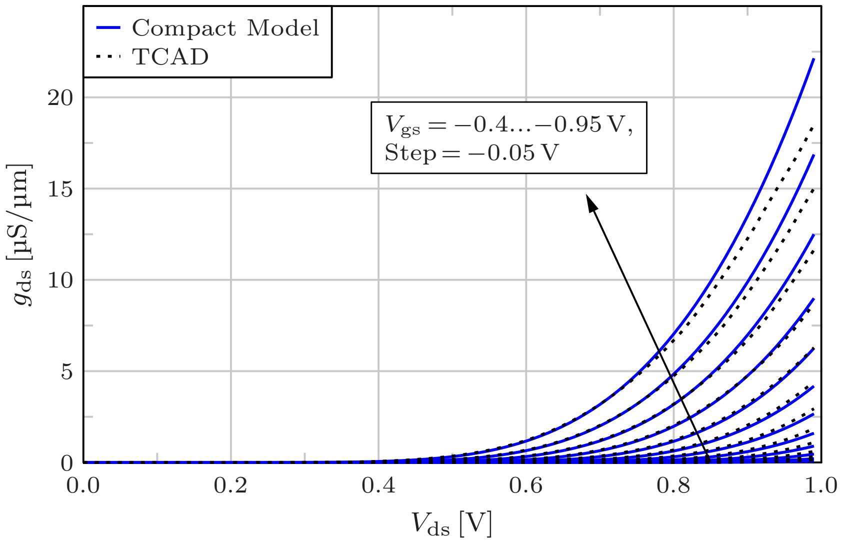
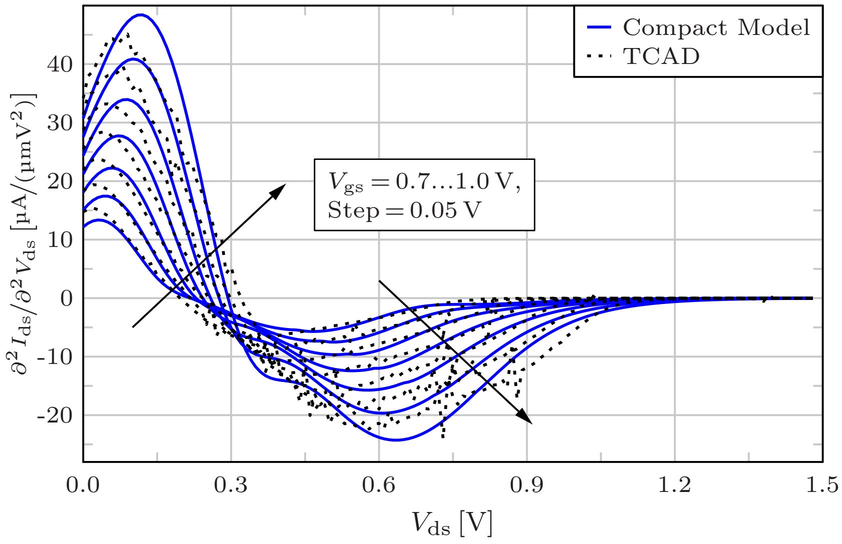


(a) ON-state.

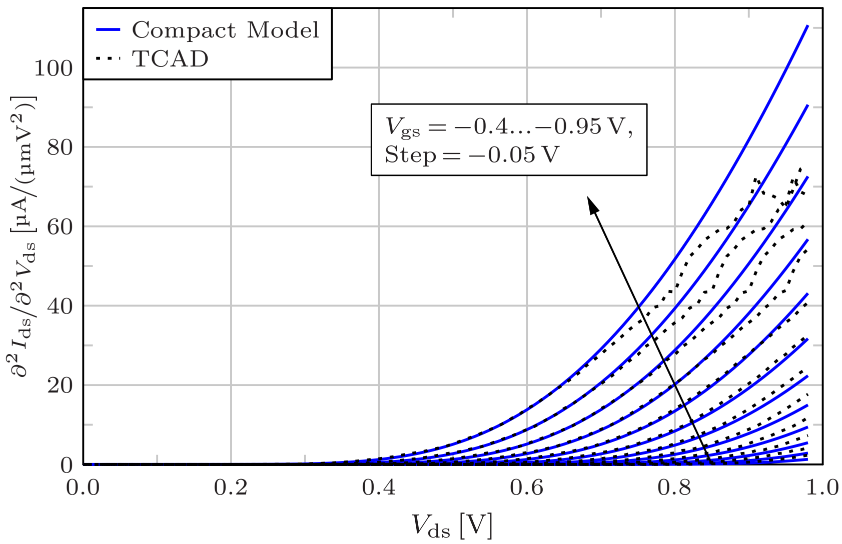


(b) AMBIPOLAR-state.

Figure 6.27.: Resulting output conductance g_{ds} of the DG TFET in comparison to TCAD data. The ON-state is shown in (a), where the AMBIPOLAR-state results are illustrated in (b).



(a) ON-state.



(b) AMBIPOLAR-state.

Figure 6.28.: Second derivative of the output I-V curve in a V_{gs} range from 0.7 V to 1.0 V. The compact model is verified by TCAD simulations. (a): ON-state. (b): AMBIPOLAR-state.

Transfer Characteristics and Derivatives

Before the compact model can be used in circuit simulations, the validity and continuity with respect to V_{gs} must be proven. For this reason, the transfer I-V curve in the gate-source voltage range from $-1.5\,\mathrm{V}$ to $1.5\,\mathrm{V}$ and various V_{ds} values is presented in Fig. 6.29. In order to better understand the influence of the two current components, the B2B and the TAT current part, Fig. 6.29(b) illustrates the separated current parts in comparison to TCAD simulations.

The results in Fig. 6.29(a) are plotted in linear and logarithmic scale and both show a good agreement with the TCAD simulations. It can be seen that an increasing V_{ds} does not much influence the ON-state subthreshold slope S_{th} and the threshold voltage V_{th}. For instance, the inverse slope at $V_{\mathrm{gs}} = 0.1\,\mathrm{V}$ changes only from $S_{\mathrm{th}}(V_{\mathrm{ds}} = 0.1\,\mathrm{V}) = 37.9\,\mathrm{mV/dec}$ to $S_{\mathrm{th}}(V_{\mathrm{ds}} = 0.7\,\mathrm{V}) = 37.5\,\mathrm{mV/dec}$. This effect is a consequence of the fact that in the ON-state, the B2B tunneling occurs at the source-to-channel junction and this junction is not affected by V_{ds} in the subthreshold regime of the TFET. But when the effect of inversion charges or the channel potential pinning comes into play, the source-to-channel junction is affected by the applied V_{ds}. At $V_{\mathrm{ds}} = 0.1\,\mathrm{V}$, this effect becomes visible at $V_{\mathrm{gs}} \approx 0.3\,\mathrm{V}$, where it can be seen that the slope of the transfer curve decreases and the B2B tunneling current saturates. For an increased V_{ds} of $0.3\,\mathrm{V}$, the effects of inversion charges affects the transfer I-V curve starting from $V_{\mathrm{gs}} \approx 0.6\,\mathrm{V}$, whereby the resulting current I_{ds} at $V_{\mathrm{gs}} = 1.5\,\mathrm{V}$ is ten times higher in comparison to $V_{\mathrm{ds}} = 0.1\,\mathrm{V}$. The effects of the slope degradation and current saturation diminish for an increasing V_{ds}.

In the AMBIPOLAR-state the increase of V_{ds} causes a shift to the right along the V_{gs}-axis in the amount of the increased V_{ds}, hence the AMBIPOLAR threshold voltage V_{th} is also shifted to more positive values. This impact is caused by the B2B tunneling occurring at the drain-to-channel junction, which is strongly influenced by the applied drain-source voltage. The amount of the AMBIPOLAR subthreshold slope is also less affected by the applied V_{ds} as it is observed in the ON-state. The slope at $V_{\mathrm{ds}} = 0.1\,\mathrm{V}$ and $V_{\mathrm{gs}} = -1.05\,\mathrm{V}$ results in $S_{\mathrm{th}} = 38.2\,\mathrm{mV/dec}$ and at $V_{\mathrm{ds}} = 0.7\,\mathrm{V}$ and $V_{\mathrm{gs}} = -0.45\,\mathrm{V}$ the subthreshold slope yields $S_{\mathrm{th}} = 40.8\,\mathrm{mV/dec}$. The difference in this case is caused by the parasitic TAT current part that has an increasing impact on the current for an increasing V_{ds}.

The OFF-state of the DG TFET is determined by the TAT effect and defines the transition from the ON- to the AMBIPOLAR-state. The range and the amount of the OFF-state depends on the applied V_{ds} as it can be seen in Fig. 6.29(a) and (b). For a drain-source voltage of $0.1\,\mathrm{V}$, the OFF-state range is from $-1.0\,\mathrm{V}$ to $0.05\,\mathrm{V}$ and the amount of the current is five times lower in comparison to the amount at $V_{\mathrm{ds}} = 0.7\,\mathrm{V}$. The reduced amount is caused by the decreased difference of the Fermi energy levels in source and drain region and therefore by the reduced electric field. In case of an applied V_{ds} of $0.7\,\mathrm{V}$, the range of the OFF-state is only from $V_{\mathrm{gs}} = -0.4\,\mathrm{V}$ to $0.05\,\mathrm{V}$. It should be noted that the TCAD simulations only consider the traps at the junction interfaces and the traps within the gate insulator material are neglected.

Due to this negligence, the TAT OFF-state current has a very flat steepness and the resulting subthreshold slope is not affected that much. By taking the gate leakage current into account, the very steep subthreshold slope would be worsened. But this effect is discussed in Sec. 6.2.

The numerical stability in terms of the transfer characteristics is under investigation in the following. First of all, the transconductance g_{m} is presented in Fig. 6.30 and in order to demonstrate the continuity of the modeling approach in all TFET operation regimes, the transconductance is plotted in linear scale in Fig. 6.30(a) and in logarithmic scale in (b). The compact modeling results are verified by TCAD data. It can be seen that g_{m} shows no kinks and discontinuities in linear scale. A small deviation in terms of a change of the curve shape occurs at $V_{\mathrm{ds}} = 0.7\,\mathrm{V}$ and an applied $V_{\mathrm{gs}} < -1.0\,\mathrm{V}$. The reason for that extraordinary slope change is again that inversion charges come into play and influence the electrostatic potential. In the transition area from subthreshold to the above threshold regime the compact model shows some inaccuracies, which are caused by the calculation of the screening length in dependency of $V_{\mathrm{gs,eff}}$ shown in Eq. (4.22). It should be noted that this small deviation has no impact on the TFET circuit simulation in Chap. 7. To inspect the continuity of the subthreshold regime of the TFET, g_{m} is shown logarithmic scale (see Fig. 6.30(b)) and one can see no kinks or discontinuities in both the ON- and AMBIPOLAR-state subthreshold regime. In the OFF-state, there seems to be a kink at the point, where the TAT current in the AMBIPOLAR-state switches to the ON-state TAT current. But looking at the second derivative of I_{ds} with respect to V_{gs} in Fig. 6.31(b), one can see that the compact model is continuous at this transition. The model transconductance shows a good agreement with the data extracted from TCAD simulations in linear and logarithmic scale for the whole examined V_{ds} and V_{gs} scope.

The second derivative of the transfer I-V curve is finally used to check the numerical stability of the compact model. Figure 6.31 presents the results of $\partial^2 I_{\mathrm{ds}}/\partial^2 V_{\mathrm{gs}}$ in (a) linear and (b) logarithmic scale and demonstrates the continuity of the compact model. In both pictures one can see that the second derivative of the modeling approach fits well in comparison to the data extracted from TCAD. Here, the inaccuracies of the screening length calculations are better visible. The extraordinary change in the curve shape can now even be observed at $V_{\mathrm{ds}} = 0.3\,\mathrm{V}$ and $0.5\,\mathrm{V}$ for an applied $V_{\mathrm{gs}} < -1.0\,\mathrm{V}$. However, these extraordinary changes have no impacts on the simulation of TFET circuits. The kinks that occur in the logarithmic plot at a gate-source voltage $V_{\mathrm{gs}} > 0.8\,\mathrm{V}$ are due to the changing sign of the second derivative and are not caused by compact model.

After stating the continuity of the compact model, the flexibility of the compact model is demonstrated in terms of device parameter variations in the next section.

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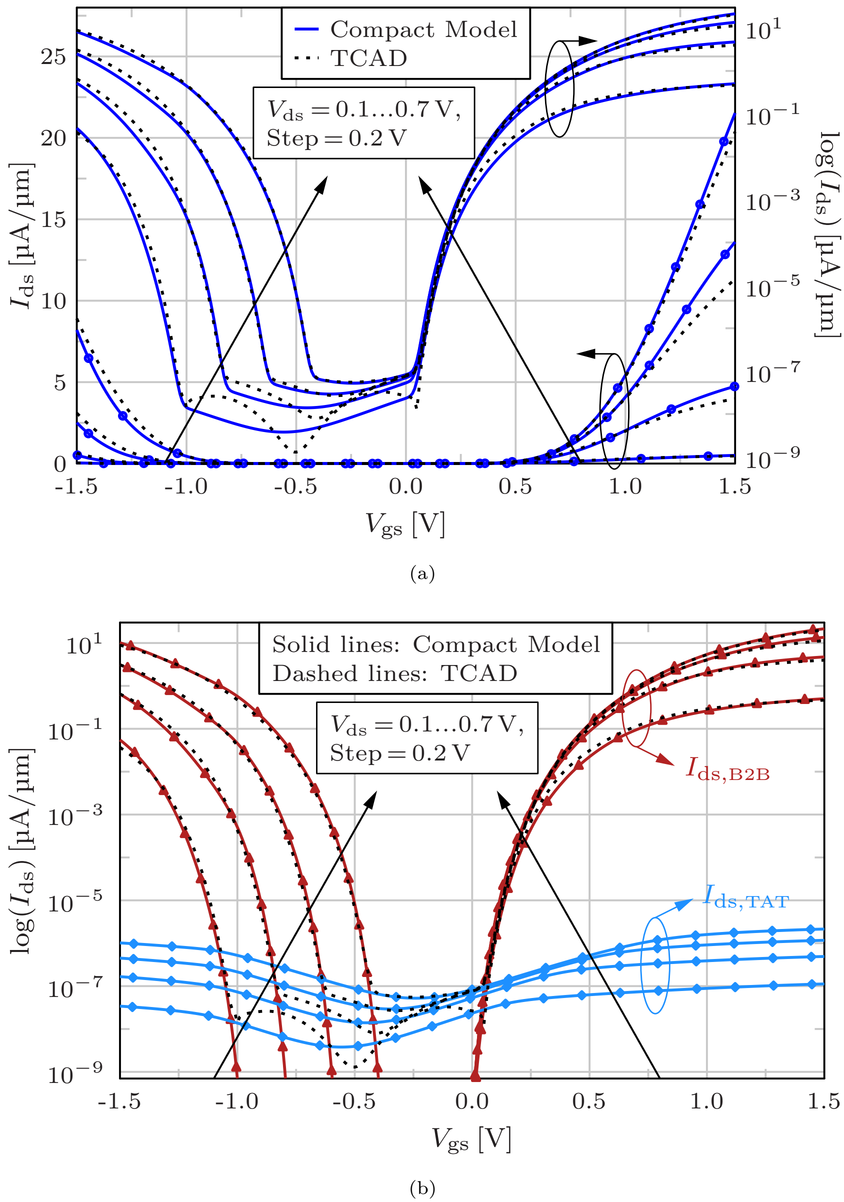
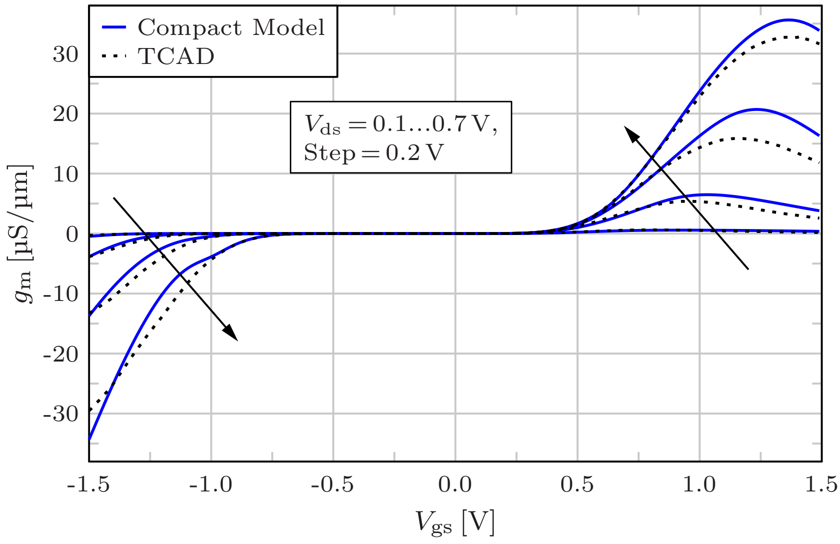
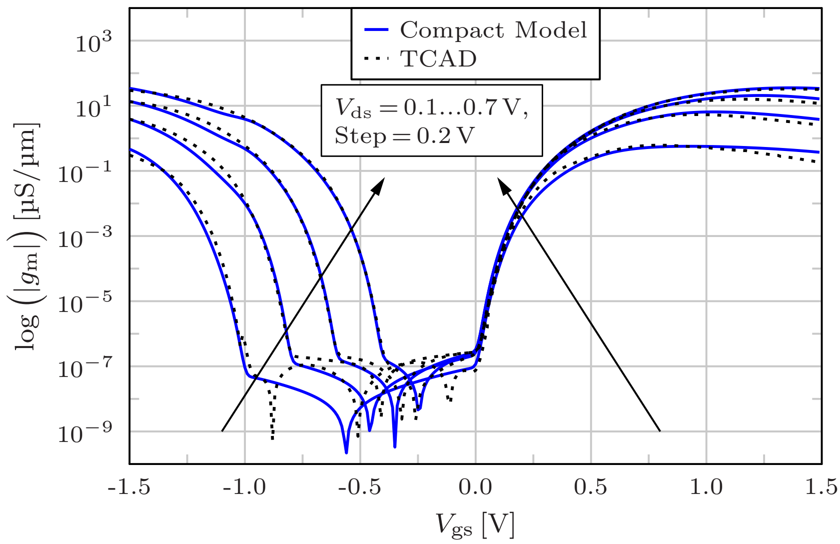


Figure 6.29.: (a) Current transfer characteristics of the DG TFET for various drain-source voltages V_{ds}. (b) Separated current parts of (a). In (b): Red lines with triangles: B2B current part. Blue lines with diamond symbols: TAT current part. In both plots: The compact model current $I_{ds} = I_{ds,B2B} + I_{ds,TAT}$ is shown in comparison to numerical simulation results obtained by TCAD Sentaurus.

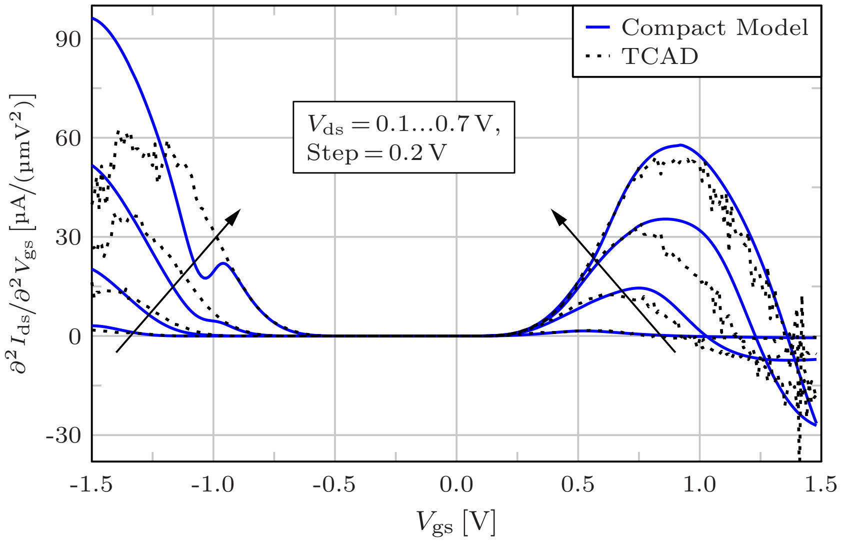


(a)

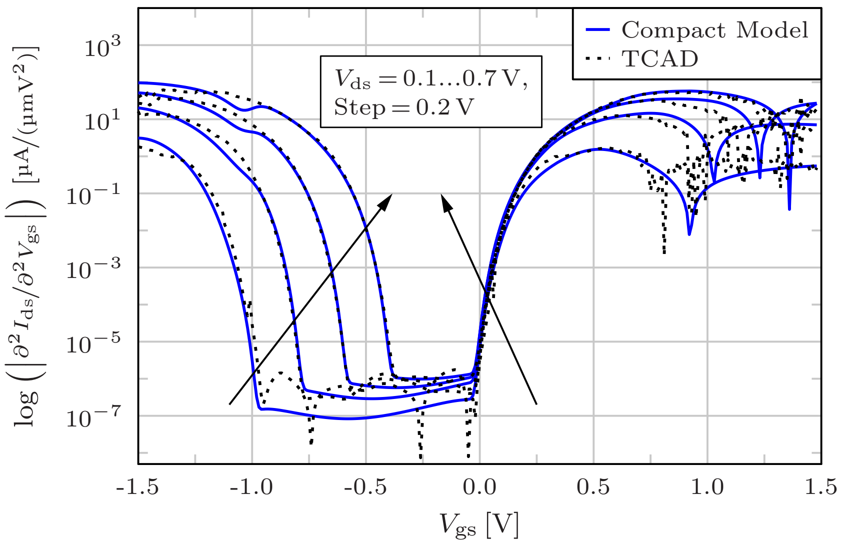


(b)

Figure 6.30.: Transconductance g_m of the DG TFET for various V_{ds} values, where (a) shows the simulation results in linear scale and (b) in logarithmic scale. The compact model is compared to TCAD simulations.



(a)



(b)

Figure 6.31.: The second derivative of the compact model transfer curve is shown in linear scale in (a) and in logarithmic scale in (b). TCAD simulations are used to verify the compact model.

Parameter Variation

In the first part of the parameter variation the device dimensions are changed in order to demonstrate the flexibility of the compact modeling approach in terms of variations in the fabrication process of TFETs. The values of the geometrical parameters l_{ch}, t_{ch} and t_{ox} are changed. The length of the S/D region l_{sd} is kept constant, because an influence on the resulting I_{ds} could only be seen by reducing l_{sd} to a few nanometers. So, from a fabrication point of view, the investigation of a varied l_{sd} is not necessary. For the device dimension variations in the compact model, only the related geometric parameters are varied and all other fitting parameters remain unchanged. Hence, the compact model is executed with the parameters extracted for the standard device (Si TFET) as shown in Tab. 6.2.

Firstly, the thickness of the gate insulator is varied in the range from $t_{\mathrm{ox}} = 1.0\,\mathrm{nm}$ to 3.0 nm. The resulting transfer I-V curves for $V_{\mathrm{ds}} = 0.7\,\mathrm{V}$ and 0.1 V are depicted in Fig. 6.32. The compact modeling approach shows a very good match to TCAD simulations for a varying t_{ox} in the applied V_{gs} and V_{ds} range, thus the influence of the gate insulator thickness on the device electrostatics is well represented in the modeling approach. A thinner gate insulator leads to an improved electrostatic control of the TFET channel region and for this reason, steeper subthreshold slopes and ON currents are achievable and for thicker t_{ox} values it is vice versa. At a drain-source voltage of 0.7 V (see Fig. 6.32(a)), the steepest subthreshold slope for $t_{\mathrm{ox}} = 1.0\,\mathrm{nm}$ is extracted at $V_{\mathrm{gs}} = 30\,\mathrm{mV}$ and yields $S_{\mathrm{th}} = 20.1\,\mathrm{mV/dec}$. The increase of t_{ox} to 3.0 nm worsens the steepest subthreshold slope to $S_{\mathrm{th}} = 50.7\,\mathrm{mV/dec}$, extracted at $V_{\mathrm{gs}} = 0.13\,\mathrm{V}$. In case of $t_{\mathrm{ox}} = 1.0\,\mathrm{nm}$ and $V_{\mathrm{ds}} = 0.1\,\mathrm{V}$, the compact model underestimates the device current in both the ON- and AMBIPOLAR-state, which is due to the model to consider inversion charges in the electrostatics (see Eq. (4.22)). By slightly increasing the parameter $\lambda_{\mathrm{ln,fit}}^{\mathrm{s/d}}$, these deviations would disappear. The OFF-state current is less influenced by a t_{ox} variation since the gate leakage current is not considered in the compact model. Here, some small deviations occur that could easily be adapted by slightly changing the parameter $\tau_{\mathrm{TAT}}^{\mathrm{s/d}}$.

In the next step, the channel thickness t_{ch} of the standard device is varied from 8 nm to 15 nm. The resulting current transfer curves for $V_{\mathrm{ds}} = 0.7\,\mathrm{V}$ is shown in Fig. 6.33(a) and for $V_{\mathrm{ds}} = 0.1\,\mathrm{V}$ in (b). In both cases, one can see a small increase in I_{ds} for a decreasing channel thickness, which is well predicted by the compact model and verified by TCAD data. That is to say, in practice a varying t_{ch} in the shown range has only a minor impact on the device current, neither in the ON- nor in the AMBIPOLAR or the OFF-state of the TFET. In addition, when t_{ch} falls below 10 nm, the effect of quantum confinement has to be taken into account [45]. In TCAD simulations and in the compact model, this effect is neglected and may cause the increasing I_{ds} for $t_{\mathrm{ch}} = 8\,\mathrm{nm}$.

As the last geometric parameter, the channel length l_{ch} is varied in the range from 14 nm to 65 nm and the influence on the device current is examined. The compact model is validated by TCAD simulation and the results for $V_{\mathrm{ds}} = 0.7\,\mathrm{V}$ and 0.1 V are illustrated in Fig. 6.34(a)

and (b). For a channel length of 14 nm the resulting ON- and AMBIPOLAR-state I_{ds} increases. Furthermore, the OFF-state current rises and worsens the subthreshold slope. These effects can be explained as a result of the relatively short l_{ch} that opens up the possibility of source-to-drain tunneling [46]. The deviations of the compact model could be minimized by slightly tuning the parameter $\varkappa_{\text{TAT}}^{\text{s/d}}$ to smaller values. The investigations of the channel lengths $l_{\text{ch}} = 32\,\text{nm}$, 45 nm and 65 nm show a nearly equal resulting I_{ds}, which is a bit higher in comparison to the device current for $l_{\text{ch}} = 22\,\text{nm}$. In a device with a channel length of 22 nm, the drain-source voltage has some impact on channel electrostatics that determines the tunneling process. This control disappears for an increasing channel length and thus, the tunneling process is only determined by the applied V_{gs} and hence, the tunneling current is able to increase a little bit [177]. Finally, it can be seen that the compact model represents the change in the channel length well for the applied V_{ds} values in comparison to TCAD simulation data.

After the variation of the device dimensions, the influence of a change in the permittivity ε_{ox} of the gate insulator material is under examination. The electrostatic control of the channel region is determined by the ratio of the gate insulator thickness and the permittivity of the material ($^{t_{\text{ox}}}/_{\varepsilon_{\text{ox}}}$). Due to this fact, the device performance can be enhanced by increasing the permittivity ε_{ox} instead of reducing t_{ox} (see Fig. 6.32). The influence of a varying ε_{ox} is evaluated for five different insulator materials that are listed in Tab. 6.1 and two drain-source voltages. The compact modeling results are again validated by TCAD simulations and are presented in Fig. 6.35. In Fig. 6.35(a), it can be seen that the compact model very well represents the permittivity change and shows a good match to TCAD data at $V_{\text{ds}} = 0.7\,\text{V}$ in the whole applied V_{gs} range, with one exception for $\varepsilon_{\text{ox}} = 80 \cdot \varepsilon_0$. In this special case, the compact model underestimates I_{ds} for $V_{\text{gs}} < -1.25\,\text{V}$ and $V_{\text{gs}} > 0.9\,\text{V}$, which is again a cause of the inversion charge model. By slightly tuning the parameter $\lambda_{\text{ln,fit}}^{\text{s/d}}$, these deviations would be improved. This effect can be seen better at a reduced V_{ds} of 0.1 V, which is depicted in Fig. 6.35(b). Another advantage of an increased insulator permittivity is the improvement in the resulting subthreshold slope and in the device current. A comparison of the ON-state inverse subthreshold slopes in Fig. 6.35(a) lead to $S_{\text{th}} = 15.0\,\text{mV/dec}$ at $V_{\text{gs}} = 10\,\text{mV}$ and $\varepsilon_{\text{ox}} = 80 \cdot \varepsilon_0$. Furthermore, the subthreshold slope at $V_{\text{gs}} = 0.13\,\text{V}$ and $\varepsilon_{\text{ox}} = 15 \cdot \varepsilon_0$ results in $S_{\text{th}} = 47.0\,\text{mV/dec}$. The ON-state current at $V_{\text{gs}} = 0.95\,\text{V}$ is 16 times higher when comparing the highest $(80 \cdot \varepsilon_0)$ and the lowest $(15 \cdot \varepsilon_0)$ permittivity ε_{ox}.

In the next variation step, the doping concentration of the source region is changed in the range from $N_{\text{s}} = 1 \cdot 10^{19}\text{cm}^{-3}$ to $1.5 \cdot 10^{20}\text{cm}^{-3}$. The transfer I-V curves for $V_{\text{ds}} = 0.7\,\text{V}$ and 0.1 V are depicted in Fig. 6.36(a) and (b), whereby the compact modeling results are shown in comparison with the results obtained by TCAD simulations. At both applied V_{ds} values one can see that a reduction of N_{s} to $1 \cdot 10^{19}\text{cm}^{-3}$ significantly reduces the ON-state current of the DG TFET and this variation cannot be captured by the compact model without readjusting the model parameters. Thus, the model parameters are extracted separately for any change in the source doping concentration and are listed in Tab. 6.3. However, it should be noted

that by changing N_s, the compact model shows the right trend but results in an error in the amount and subthreshold slope of the device current. After readjusting the necessary model parameters, the compact model shows a good match with TCAD data. In practice, the source doping concentration should be as high as possible in order to obtain a ON-state current that is higher than the I_{ds} in AMBIPOLAR-state.

Table 6.3.: Adapted fitting parameters for various doping concentrations of the source and drain region and various interface trap densities.

Various Source Doping Concentrations N_s								
N_s [cm^{-3}]	$\lambda^{s}_{ln,fit}$ [–]	m^{*}_{s} [kg]	$(\eta^{s})^{2}$ [cm^{2}]	$(\sigma^{s}_{B2B})^{2}$ [cm^{2}]	τ^{s}_{TAT} [cm^{2}]	τ^{d}_{TAT} [cm^{2}]	$\varkappa^{s}_{TAT}$ [–]	$\varkappa^{d}_{TAT}$ [–]
$1{\cdot}10^{19}$	3.0	$0.15{\cdot}m_0$	$7.0{\cdot}10^{-15}$	$9.6{\cdot}10^{-14}$	$2.3{\cdot}10^{-23}$	$2.0{\cdot}10^{-19}$	50	5
$3{\cdot}10^{19}$	1.3	$0.19{\cdot}m_0$	$4.0{\cdot}10^{-15}$	$5.6{\cdot}10^{-14}$	$8.4{\cdot}10^{-23}$	$3.5{\cdot}10^{-21}$	9.5	11
$5{\cdot}10^{19}$	0.85	$0.237{\cdot}m_0$	$4.0{\cdot}10^{-15}$	$2.7{\cdot}10^{-14}$	$1.2{\cdot}10^{-22}$	$4.3{\cdot}10^{-21}$	20	10.5
$7{\cdot}10^{19}$	0.85	$0.253{\cdot}m_0$	$2.0{\cdot}10^{-15}$	$2.0{\cdot}10^{-14}$	$8.0{\cdot}10^{-22}$	$2.5{\cdot}10^{-21}$	12	12
$9{\cdot}10^{19}$	0.55	$0.245{\cdot}m_0$	$2.5{\cdot}10^{-16}$	$3.0{\cdot}10^{-14}$	$1.4{\cdot}10^{-21}$	$3.2{\cdot}10^{-21}$	12	11
$1.2{\cdot}10^{20}$	0.69	$0.29{\cdot}m_0$	$3.65{\cdot}10^{-16}$	$2.0{\cdot}10^{-14}$	$3.2{\cdot}10^{-21}$	$2.0{\cdot}10^{-21}$	10	12
$1.5{\cdot}10^{20}$	0.70	$0.34{\cdot}m_0$	$3.65{\cdot}10^{-16}$	$2.0{\cdot}10^{-14}$	$7.6{\cdot}10^{-21}$	$2.3{\cdot}10^{-21}$	8	12

Various Drain Doping Concentrations N_d								
N_d [cm^{-3}]	$\lambda^{d}_{ln,fit}$ [–]	m^{*}_{d} [kg]	$(\eta^{d})^{2}$ [cm^{2}]	$(\sigma^{d}_{B2B})^{2}$ [cm^{2}]	τ^{s}_{TAT} [cm^{2}]	τ^{d}_{TAT} [cm^{2}]	$\varkappa^{s}_{TAT}$ [–]	$\varkappa^{d}_{TAT}$ [–]
$1{\cdot}10^{19}$	0.2	$0.16{\cdot}m_0$	$5.0{\cdot}10^{-13}$	$6.0{\cdot}10^{-15}$	$1.3{\cdot}10^{-19}$	$6.2{\cdot}10^{-23}$	5	50
$3{\cdot}10^{19}$	0.34	$0.185{\cdot}m_0$	$4.0{\cdot}10^{-14}$	$3.8{\cdot}10^{-15}$	$3.5{\cdot}10^{-21}$	$1.2{\cdot}10^{-22}$	9.5	11
$5{\cdot}10^{19}$	0.27	$0.24{\cdot}m_0$	$4.0{\cdot}10^{-14}$	$3.9{\cdot}10^{-15}$	$2.5{\cdot}10^{-21}$	$3.6{\cdot}10^{-22}$	10.5	10.5
$7{\cdot}10^{19}$	0.30	$0.265{\cdot}m_0$	$2.0{\cdot}10^{-14}$	$3.2{\cdot}10^{-15}$	$1.6{\cdot}10^{-21}$	$8.3{\cdot}10^{-22}$	12	12
$9{\cdot}10^{19}$	0.40	$0.29{\cdot}m_0$	$7.5{\cdot}10^{-15}$	$3.7{\cdot}10^{-15}$	$1.9{\cdot}10^{-21}$	$1.5{\cdot}10^{-21}$	11	12
$1.2{\cdot}10^{20}$	0.48	$0.325{\cdot}m_0$	$3.0{\cdot}10^{-15}$	$2.8{\cdot}10^{-15}$	$1.4{\cdot}10^{-21}$	$2.2{\cdot}10^{-21}$	12	12
$1.5{\cdot}10^{20}$	0.48	$0.36{\cdot}m_0$	$2.0{\cdot}10^{-15}$	$2.7{\cdot}10^{-15}$	$1.8{\cdot}10^{-21}$	$3.4{\cdot}10^{-21}$	11	11

Various Interface Trap Densities N^{0}_{t}				
N^{0}_{t} [cm^{-2}]	τ^{s}_{TAT} [cm^{2}]	τ^{d}_{TAT} [cm^{2}]	$\varkappa^{s}_{TAT}$ [–]	$\varkappa^{d}_{TAT}$ [–]
10^{10}	$1.1{\cdot}10^{-20}$	$1.7{\cdot}10^{-20}$	11	11
10^{11}	$4.95{\cdot}10^{-21}$	$7.3{\cdot}10^{-21}$	11	11
10^{13}	$1.4{\cdot}10^{-21}$	$2.1{\cdot}10^{-21}$	9.5	9.5
10^{14}	$2.3{\cdot}10^{-21}$	$3.3{\cdot}10^{-21}$	7	7
10^{15}	$2.45{\cdot}10^{-21}$	$3.95{\cdot}10^{-21}$	5.7	5.7
10^{16}	$9.3{\cdot}10^{-22}$	$1.55{\cdot}10^{-21}$	5.6	5.6
10^{17}	$1.9{\cdot}10^{-22}$	$1.65{\cdot}10^{-22}$	6.4	7.4
10^{18}	$1.1{\cdot}10^{-23}$	$2.6{\cdot}10^{-23}$	10	10

The TFET working principle is based on asymmetrical doping types of the source and drain region. For this reason, the TFET shows its typical AMBIPOLAR behavior, which is from a circuit designer's point of view an undesirable effect and should be suppressed. One possibility to suppress the AMBIPOLAR-state is the reduction of the drain region doping concentration.

Thus, a variation of the parameter N_d is examined in the following. Figure 6.37 presents the compact modeling results for $V_\mathrm{ds} = 0.7\,\mathrm{V}$ and $0.1\,\mathrm{V}$ in a N_d range from $1 \cdot 10^{19}\mathrm{cm}^{-3}$ to $1.5 \cdot 10^{20}\mathrm{cm}^{-3}$ in comparison with TCAD Sentaurus simulation data. As it can be seen, the modeling approach stays in a good agreement with the TCAD data, where it should be kept in mind that similar to the N_s variation, the model parameters are separately extracted for each N_d value. The extracted parameter values are shown in Tab. 6.3, whereby not all parameters had to be adapted. The not mentioned fitting parameters are the same as for the Si TFET (see Tab. 6.2). At a drain-source voltage of $V_\mathrm{ds} = 0.7\,\mathrm{V}$ (see Fig. 6.37(a)), a reduction in N_d of $1 \cdot 10^{19}\mathrm{cm}^{-3}$ suppresses the device current I_ds at $V_\mathrm{gs} = -1.5\,\mathrm{V}$ by factor $2.7 \cdot 10^{3}$ in comparison to the standard device and by further reducing N_d to $1 \cdot 10^{18}\mathrm{cm}^{-3}$ the resulting AMBIPOLAR-state current would be in the range of the OFF-state current. In Fig. 6.37(b), one can see that a reduction in V_ds of $0.1\,\mathrm{V}$ causes a left shift of the AMBIPOLAR-state along the V_gs-axis. In this case, the AMBIPOLAR-state is shifted out of the working area of the TFET. A combination of the left shift and the N_d reduction to $1 \cdot 10^{19}\mathrm{cm}^{-3}$ causes a suppression of the AMBIPOLAR-state current by factor $2 \cdot 10^{5}$ in contrast to the standard TFET. In conclusion, it can be said that the AMBIPOLAR-state can be suppressed by a trade-off of the used doping concentration N_d and the applied V_ds by keeping the standard TFET geometry. Nevertheless, the AMBIPOLAR-state is also suppressible by optimizing the TFET device geometry with e.g. a reduction of the gate length [178, 179], but this is not investigated in this work.

In order to show the influence of the interface trap density on the resulting transfer I-V characteristic, N_t^0 is varied in the range from $10^{11}\mathrm{cm}^{-2}$ to $10^{18}\mathrm{cm}^{-2}$. Because a varying trap density affects the resulting subthreshold slope, the model parameters to characterize the TAT current are extracted separately for each N_t^0 and shown in Tab. 6.3. The modeling results for $V_\mathrm{ds} = 0.7\,\mathrm{V}$ and $0.1\,\mathrm{V}$ are depicted in Fig. 6.38(a) and (b). The verification is done with the help of TCAD data. It can be seen that it is possible to capture the change in N_t^0 by the compact model and to obtain a good agreement to TCAD data for both drain-source voltages. The subthreshold slope degradation is well visible at $V_\mathrm{ds} = 0.7\,\mathrm{V}$. The steepest subthreshold slope for $N_\mathrm{t}^0 = 10^{10}\mathrm{cm}^{-2}$ is achieved at $V_\mathrm{gs} = 40\,\mathrm{mV}$ and yields $S_\mathrm{th} = 26.0\,\mathrm{mV/dec}$, whereas the steepest slope for $N_\mathrm{t}^0 = 10^{18}\mathrm{cm}^{-2}$ is $S_\mathrm{th} = 121.3\,\mathrm{mV/dec}$, extracted at $V_\mathrm{gs} = 0.26\,\mathrm{V}$. In addition, the ratio $I_\mathrm{ON}/I_\mathrm{OFF}$ is affected by the interface trap density. For a low N_t^0 of $10^{10}\mathrm{cm}^{-2}$, the ratio results in $I_\mathrm{ON}/I_\mathrm{OFF} = 1.2 \cdot 10^{9}$, whereby this ratio worsens to $I_\mathrm{ON}/I_\mathrm{OFF} = 1.7 \cdot 10^{4}$ by examining $N_\mathrm{t}^0 = 10^{18}\mathrm{cm}^{-2}$. The current value for I_ON is extracted at $V_\mathrm{gs} = 1.0\,\mathrm{V}$ and I_OFF at $V_\mathrm{gs} = 0.0\,\mathrm{V}$. By reducing V_ds to $0.1\,\mathrm{V}$, the $I_\mathrm{ON}/I_\mathrm{OFF}$-ratio is shrunk by the factor 10 for the both investigated trap densities. So, it can be concluded that the trap density has a higher impact on the TFET behavior when V_ds is reduced.

In the last step of the parameter variation, the source material is modified to enhance the performance of the DG TFET and to demonstrate the capability of the compact model in terms of simulating hetero-junctions. The three aforementioned source materials Ge, SiGe and GaAs are examined. The compact modeling results are obtained by applying the model

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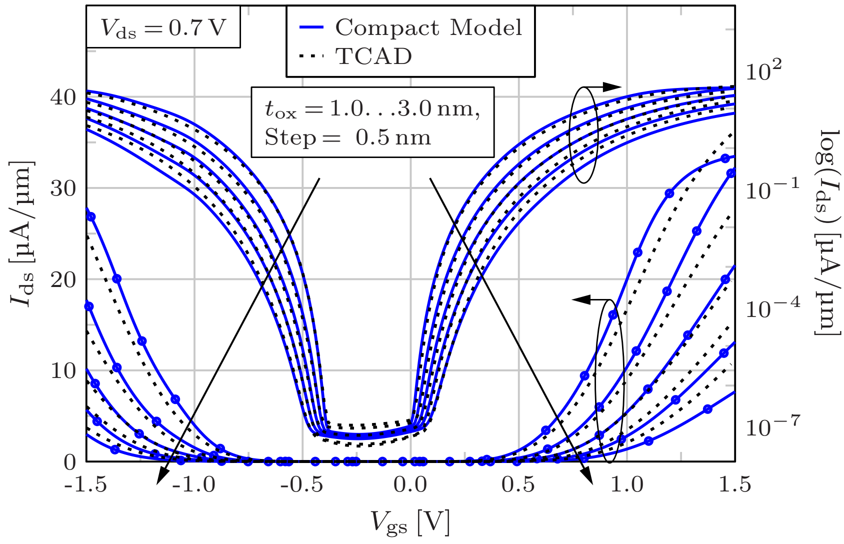
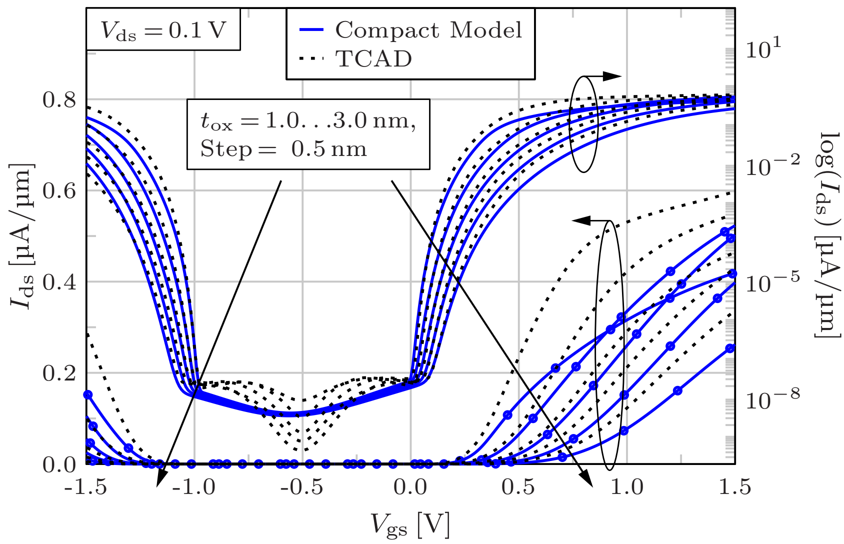
parameters listed in Tab. 6.2. The verification of the model is demonstrated with the help of TCAD simulations of transfer I-V curves at $V_{\mathrm{ds}} = 0.7\,\mathrm{V}$ and $0.1\,\mathrm{V}$. The comparison between the compact model and TCAD is presented in Fig. 6.39 and it can be seen that the model shows a good agreement with the numerical simulations for both applied V_{ds} values. A comparison of the steepest resulting subthreshold slope S_{th} at a certain voltage V'_{gs} and the resulting ON-state current for a drain-source voltage of 0.7 V is shown in Tab. 6.4. The subthreshold slope for Ge and SiGe results in nearly the same values in comparison to the Si TFET, where in case of GaAs the slope is 5 mV/dec worse than the subthreshold slope of the standard device. By applying a source material with a smaller band gap E_{g} than Si, one would expect a steeper subthreshold slope, but the TAT effect prevents this improvement. By comparing the ON-state current, it can be seen that the TFET with a Ge source region has the highest gain in I_{ds} at $V_{\mathrm{gs}} = 1.0\,\mathrm{V}$, which is 17 times higher than in the Si TFET. The ON-state I_{ds} is SiGe is little bit lower, but still 5.5 times higher than in the standard device. The chosen source material GaAs has a wider band gap compared to Si and the current in the ON-state is three times lower than in the standard device. In summary, it is to say that an improvement in the TFET performance is only achievable by choosing a III-V material as the source material [180]. Another improvement of the TFET performance could be achieved by applying III-V materials to the whole TFET device. Two possible combinations could be (S: p-GaSb, Ch: i-InAs, D: n-InAs) [181] or (S: p-AlGaSb, Ch: i-InAs, D: n-InAs) [97].

Table 6.4.: Comparison of the resulting subthreshold slope and ON-state current for various source materials and $V_{\mathrm{ds}} = 0.7\,\mathrm{V}$. V'_{gs} indicates the voltage value, where S_{th} is extracted.

Source Material	$S_{\mathrm{th}}(V'_{\mathrm{gs}})$ [mV/dec]	V'_{gs} [mV]	$I_{\mathrm{ds}}(V_{\mathrm{gs}} = 1.0\,\mathrm{V})$ [µA/µm]
Ge	38.6	10	93.6
SiGe	38.7	60	29.4
Si	37.5	100	5.43
GaAs	42.4	100	1.84

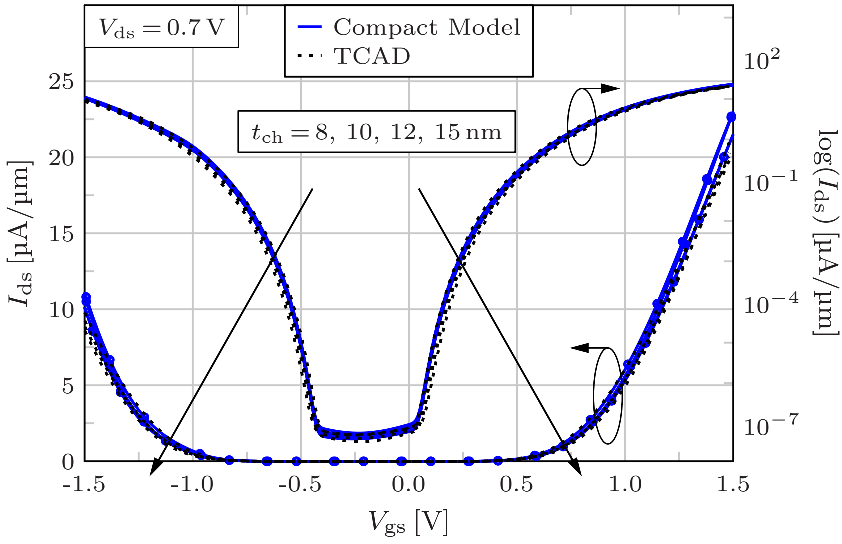


(a) $V_{ds} = 0.7$ V.

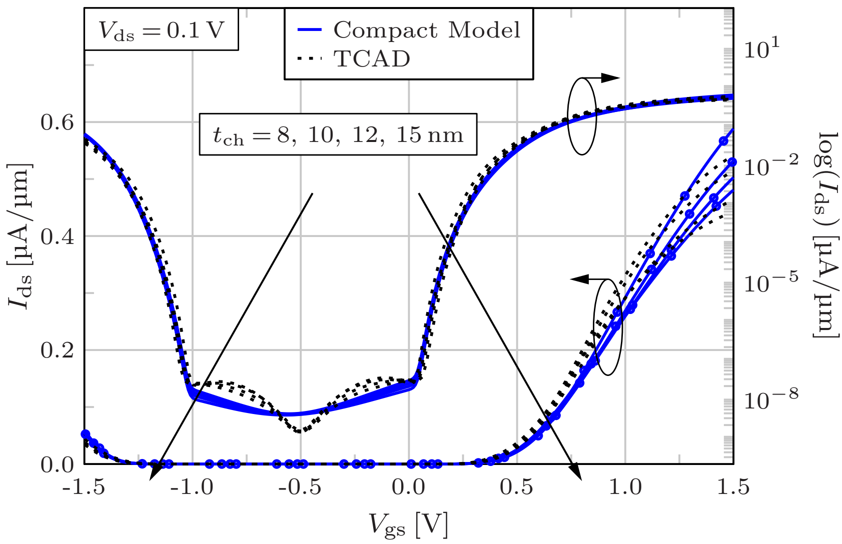


(b) $V_{ds} = 0.1$ V.

Figure 6.32.: Transfer I-V characteristics at (a) $V_{ds} = 0.7$ V and (b) $V_{ds} = 0.1$ V and various gate insulator thicknesses t_{ox}. The compact model is compared to TCAD data.

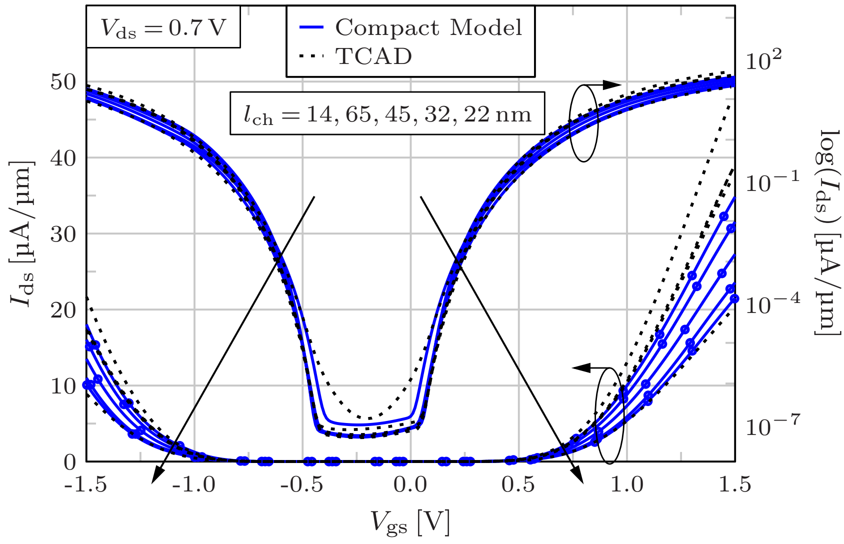


(a) $V_{ds} = 0.7$ V.

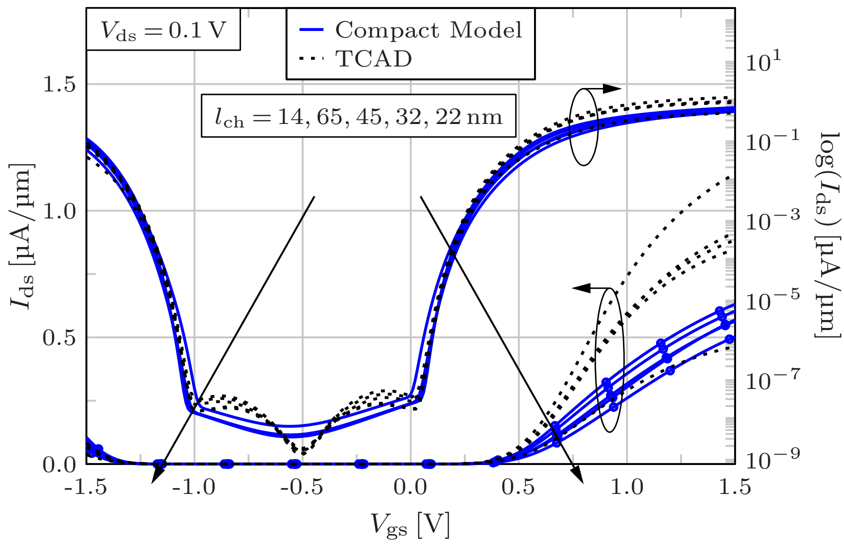


(b) $V_{ds} = 0.1$ V.

Figure 6.33.: Resulting transfer characteristics for a varied channel thickness t_{ch} at (a) $V_{ds} = 0.7$ V and (b) $V_{ds} = 0.1$ V. The compact model is shown in comparison to numerical data extracted from TCAD simulations.

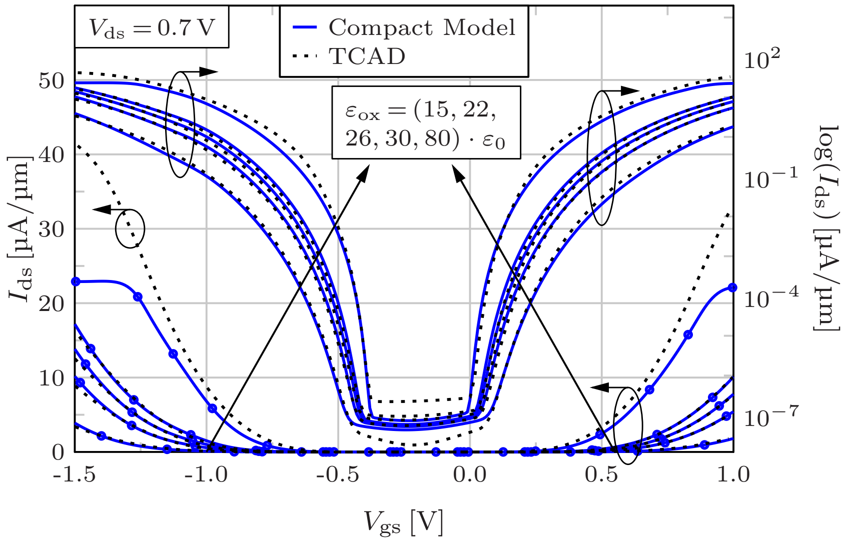


(a) $V_{ds} = 0.7$ V.

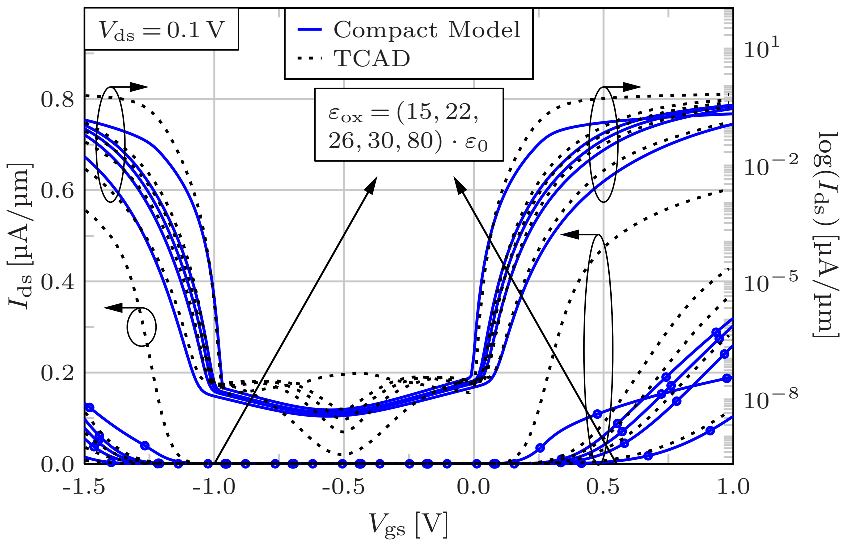


(b) $V_{ds} = 0.1$ V.

Figure 6.34.: Transfer characteristics for various channel lengths l_{ch} and V_{ds}. (a) shows the results obtained by the compact model for $V_{ds} = 0.7$ V and (b) for $V_{ds} = 0.1$ V in comparison to TCAD data.

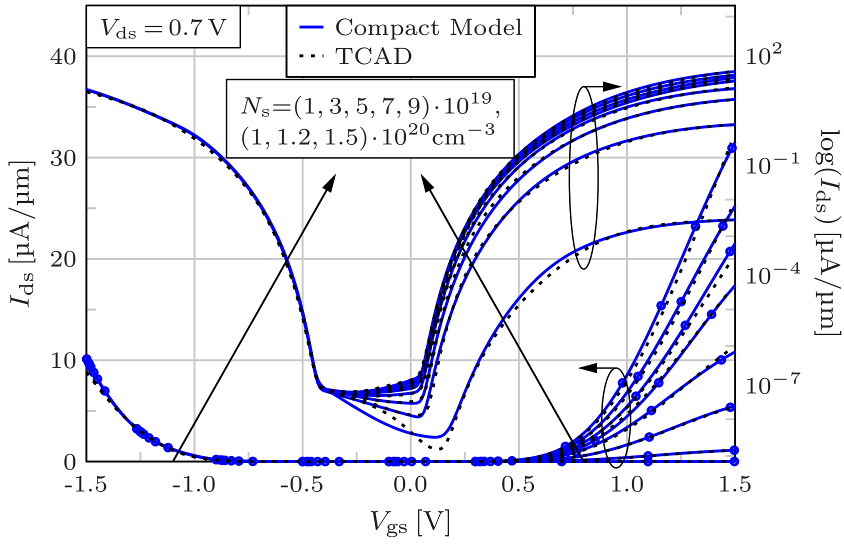


(a) $V_{ds} = 0.7$ V.

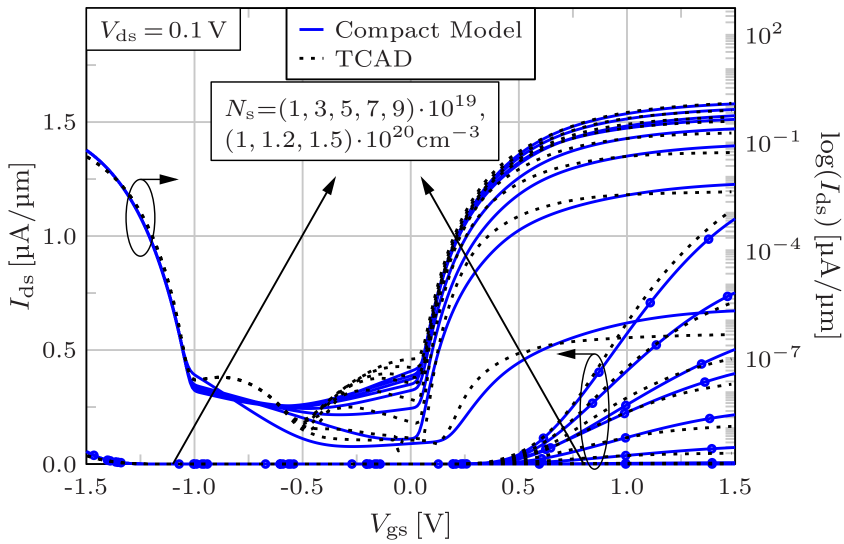


(b) $V_{ds} = 0.1$ V.

Figure 6.35.: Transfer curve modeling results for (a) $V_{ds} = 0.7$ V and (b) $V_{ds} = 0.1$ V shown in comparison to TCAD simulation. In addition, the permittivity ε_{ox} of the gate insulator is varied.

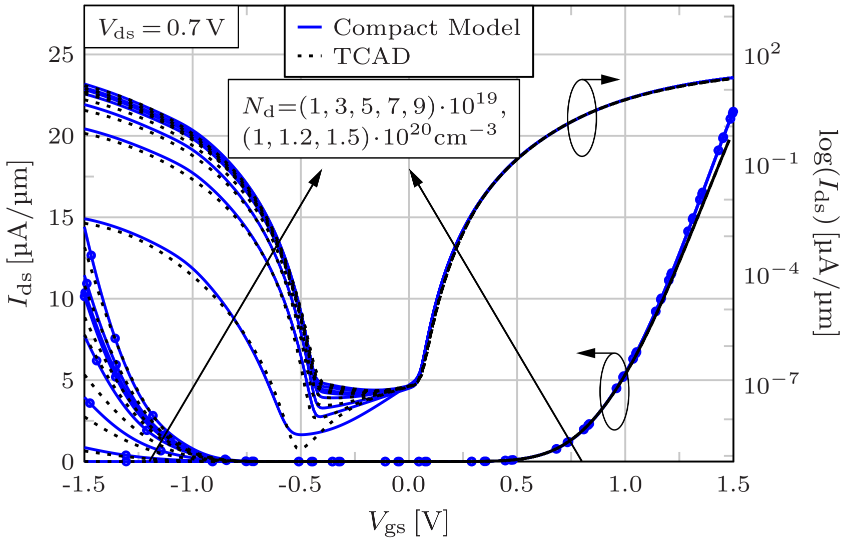


(a) $V_{ds} = 0.7\,V$.

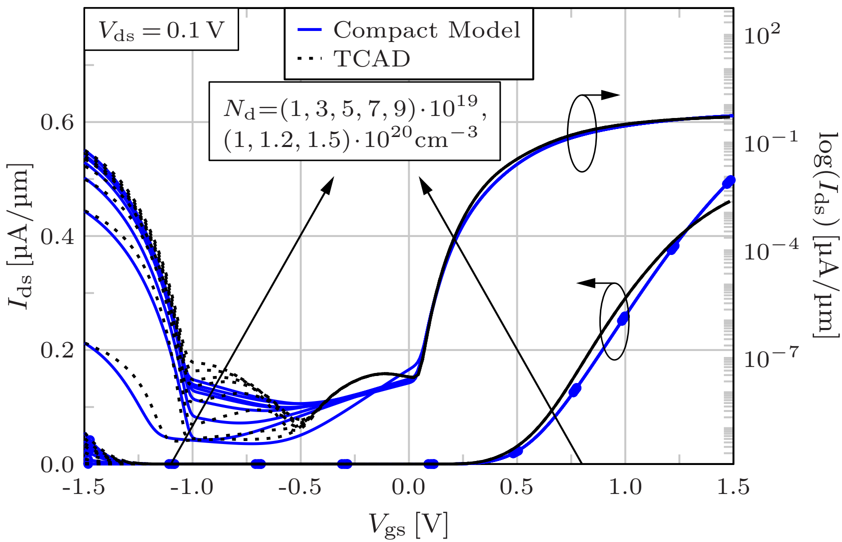


(b) $V_{ds} = 0.1\,V$.

Figure 6.36.: Simulation results of transfer I-V curves for various doping concentrations N_s of the source region for (a) $V_{ds} = 0.7\,V$ and (b) 0.1 V. Numerical simulation data are extracted from TCAD Sentaurus to verify the compact model. The compact model is separately fitted for every N_s value.

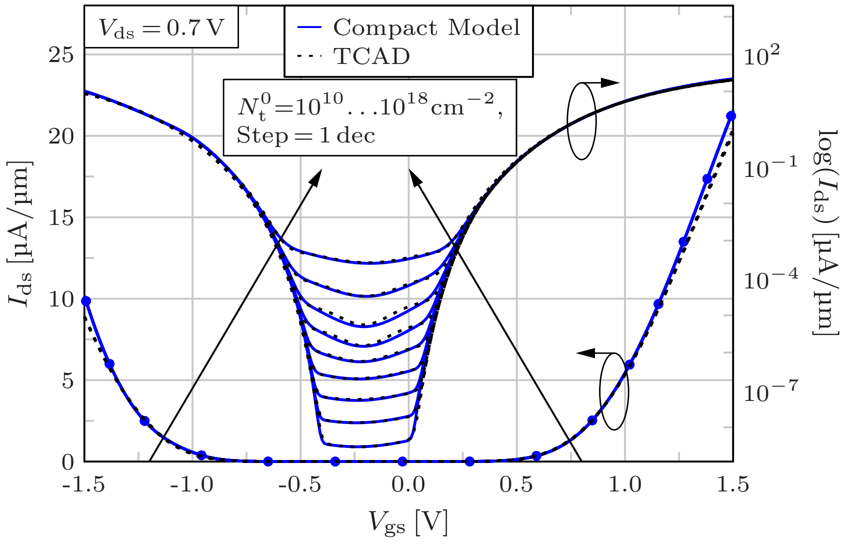


(a) $V_{ds} = 0.7$ V.

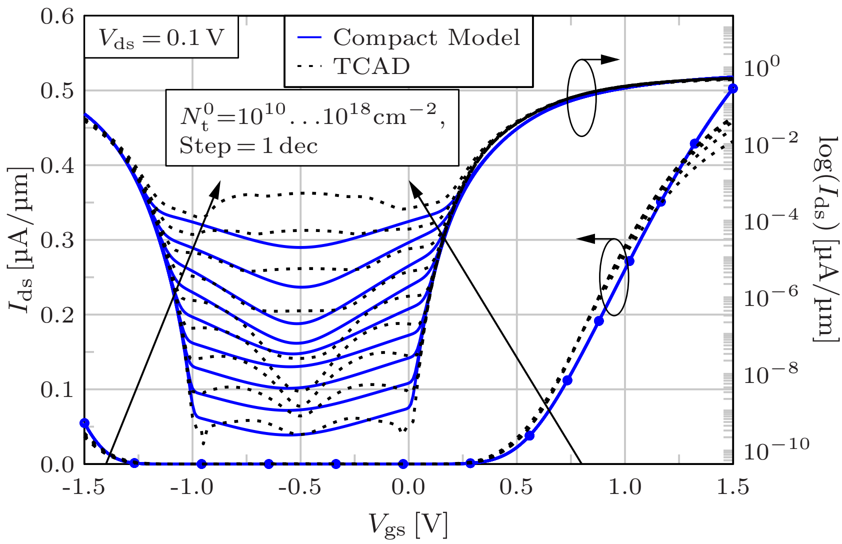


(b) $V_{ds} = 0.1$ V.

Figure 6.37.: Transfer curves at (a) $V_{ds} = 0.7$ V and (b) $V_{ds} = 0.1$ V and various drain region doping concentrations N_d. The compact modeling results are verified by TCAD simulations. For all applied N_d the compact model is separately adjusted.

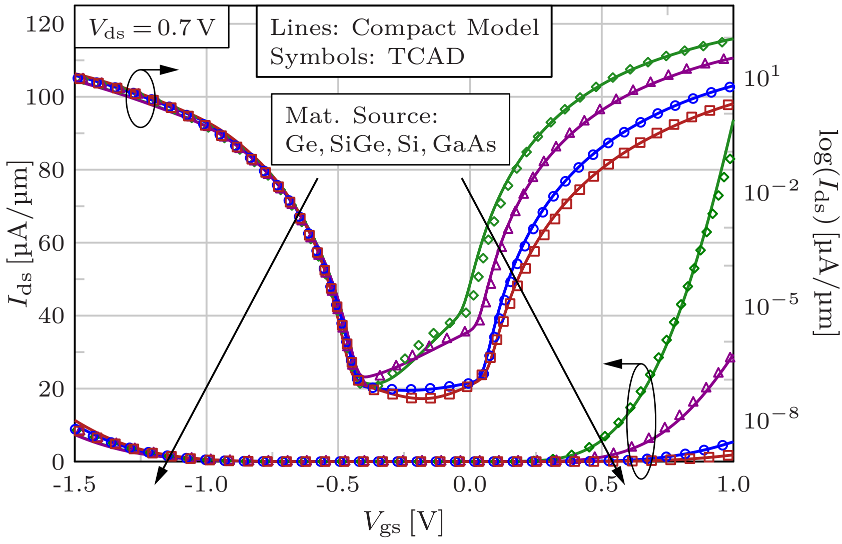


(a) $V_{ds} = 0.7\,V$.

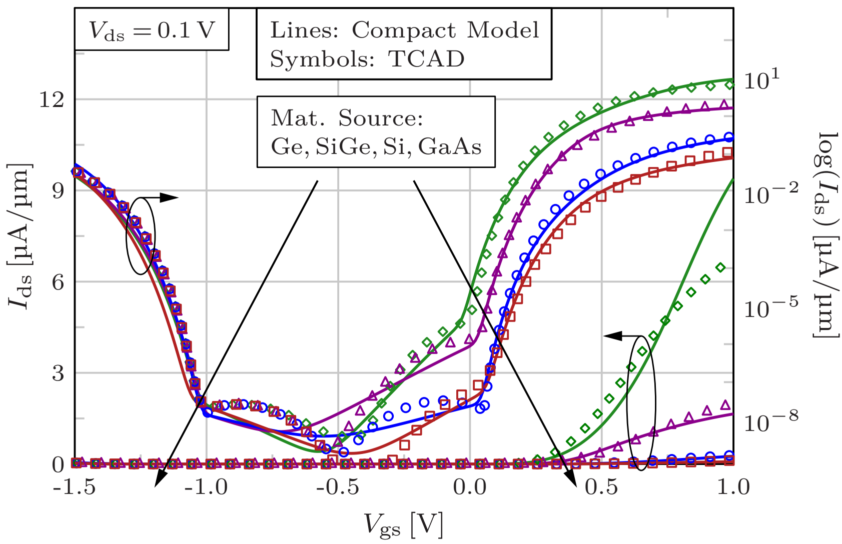


(b) $V_{ds} = 0.1\,V$.

Figure 6.38.: Varied interface trap concentration N_t^0 and its influence on the resulting OFF-state current. The validity of compact modeling approach is proven by TCAD data in terms of the current transfer characteristics. (a): $V_{ds} = 0.7\,V$. (b): $V_{ds} = 0.1\,V$.



(a) $V_{ds} = 0.7$ V.



(b) $V_{ds} = 0.1$ V.

Figure 6.39.: Transfer I-V curves for varied source materials and drain-source voltages. (a) presents the results for $V_{ds} = 0.7$ V and (b) shows the resulting curves at $V_{ds} = 0.1$ V. TCAD data are used to verify the compact model.

6.2 Verification by Measurement Data

After verifying the compact model by TCAD simulations of a DG TFET, the adaptability and flexibility of the modeling approach is demonstrated with the help of fabricated devices. The examined devices are complementary nanowire (NW) gate-all-around (GAA) TFETs, fabricated in the Forschungszentrum Jülich [182]. Figure 6.40(a) depicts a 3D sketch of both the n- and p-type NW GAA TFET, whereby both types consists of 60 parallel NWs per device. The source and drain region of the TFET consist of $NiSi_2$, whereby the junctions to the channel region are doped by an implantation process. In case of the n-type device, a high dose of Boron (BF_2^+) is implanted into $NiSi_2$ at the source-to-channel junction and the drain-to-channel junction is implanted with a high dose of Phosphorus (P^+). For p-type devices, the implantation process is done vice versa. The gate contact is TiN, the gate insulator material is HfO_2 and the channel is made of strained Silicon (sSi). A detailed explanation of the fabrication process can be found in [182].

The cross section within a single NW is illustrated in Fig. 6.40(b), with the implantation regions S and D highlighted in yellow and green, respectively. A single NW has the following device dimensions: $l_{\mathrm{ch}} = 350\,\mathrm{nm}$, $t_{\mathrm{ch}} = 5\,\mathrm{nm}$, $t_{\mathrm{ox}} = 3\,\mathrm{nm}$ and $w_{\mathrm{ch}} = 40\,\mathrm{nm}$. Regarding the cross section from gate to gate (cutline along the y-axis), the NW shows a rectangular shape and since the channel width is much bigger than the channel thickness ($w_{\mathrm{ch}} \gg t_{\mathrm{ch}}$), the compact model for a DG TFET can be applied to a single NW of the GAA device. The contributions of the gates at the front and backside of the NW to the device current are small and thus can be captured with the model parameter fitting. The total device current of the NW GAA TFET is obtained by multiplying the resulting current of a single NW by the count of the parallel NW as follows:

$$I_{\mathrm{ds,\,GAA\,TFET}} = 60 \cdot I_{\mathrm{ds,\,NW}}. \tag{6.1}$$

It should be noted that due to the implantation process of the S/D region, no precise information about the doping concentrations is available, so that the parameters N_{s} and N_{d} are used as adjustable values in the compact model.

The verification of the n-type NW GAA TFET for a V_{ds} range from 0.1 V to 0.5 V is presented in Fig. 6.41(a). This figure illustrates the measured device current (black dashed lines), the measurements of the gate leakage current $I_{\mathrm{g,leak}}^{\mathrm{meas}}$ (red triangles), the compact modeling results (magenta dashed lines with markers) and the blue solid lines shows the summation of the compact model I_{ds} and $I_{\mathrm{g,leak}}^{\mathrm{meas}}$. The compact model is simulated by applying the structural parameters of a single NW and with the help of the extracted model parameters listed in Tab. 6.5. The modeling results stay in a good agreement with the measured values for all applied V_{ds} values. Only a small deviation of the modeled and the measured I_{ds} occurs for $V_{\mathrm{ds}} = 0.1\,\mathrm{V}$ at the transition from the AMBIPOLAR- to the ON-state. As it can be seen, this

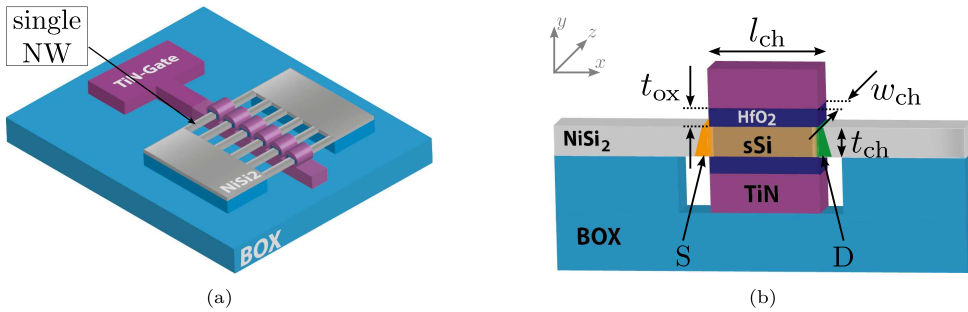


Figure 6.40.: (a) 3D sketch of the strained Si NW GAA TFET, whereby both n- and p-type TFET devices consist of 60 parallel NWs. (b). Cross section within a single NW, showing the structural parameters applied in the DG compact model. Material S and D region: $NiSi_2$. Gate material: Stack of TiN/HfO_2. Channel material: Strained Silicon (sSi) [182].

error is a cause of the gate leakage current $I_{g,leak}^{meas}$ and this effect is not yet considered in the compact model.

The results of the p-type device are shown in Fig. 6.41(b) for applied drain-source voltages from $V_{ds} = -0.1\,V$ to $-0.5\,V$. The compact model is executed by using the adjustable parameters listed in Tab. 6.5. The modeling approach shows a good match to the measured data in the ON- and AMBIPOLAR-state of the TFET. Some small inaccuracies occur in the OFF-state of the device for $V_{ds} = -0.1\,V$ and $-0.3\,V$ due to the reasons mentioned in the n-type verification. Adding the measured gate leakage current $I_{g,leak}^{meas}$ to the modeled I_{ds}, the results show a nearly perfect match. For this reason, a gate leakage current model should be considered in an extended version of the compact model in the future.

Table 6.5.: Compact model fitting parameters applied in the simulations of the fabricated complementary NW GAA TFETs.

Parameter	Unit	n-type	p-type
$\lambda_{\mathsf{fit}}^{\mathsf{s}}$	[–]	0.65	0.65
$\lambda_{\mathsf{fit}}^{\mathsf{d}}$	[–]	1.25	0.60
$\lambda_{\mathsf{ln,fit}}^{\mathsf{s}}$	[–]	0.95	0.90
$\lambda_{\mathsf{ln,fit}}^{\mathsf{d}}$	[–]	0.90	0.30
m_{s}^{*}	[kg]	$0.50{\cdot}m_0$	$0.49{\cdot}m_0$
m_{d}^{*}	[kg]	$0.525{\cdot}m_0$	$0.54{\cdot}m_0$
$(\eta^{\mathsf{s}})^2$	[cm^2]	$1.3{\cdot}10^{-14}$	$3.5{\cdot}10^{-15}$
$\left(\eta^{\mathsf{d}}\right)^2$	[cm^2]	$1.4{\cdot}10^{-13}$	$5.0{\cdot}10^{-15}$
$(\sigma_{\mathsf{B2B}}^{\mathsf{s}})^2$	[cm^2]	$6.0{\cdot}10^{-14}$	$8.6{\cdot}10^{-15}$
$\left(\sigma_{\mathsf{B2B}}^{\mathsf{d}}\right)^2$	[cm^2]	$8.6{\cdot}10^{-14}$	$3.0{\cdot}10^{-14}$
$(\sigma_{\mathsf{TAT}}^{\mathsf{s}})^2$	[cm^2]	$9.0{\cdot}10^{-16}$	$1.0{\cdot}10^{-14}$
$\left(\sigma_{\mathsf{TAT}}^{\mathsf{d}}\right)^2$	[cm^2]	$1.0{\cdot}10^{-14}$	$1.0{\cdot}10^{-15}$
$\varkappa_{\mathsf{TAT}}^{\mathsf{s}}$	[–]	3.2	2.8
$\varkappa_{\mathsf{TAT}}^{\mathsf{d}}$	[–]	2.2	2.8
$\tau_{\mathsf{TAT}}^{\mathsf{s}}$	[cm^2]	$6.19{\cdot}10^{-20}$	$6.11{\cdot}10^{-22}$
$\tau_{\mathsf{TAT}}^{\mathsf{d}}$	[cm^2]	$1.89{\cdot}10^{-15}$	$2.02{\cdot}10^{-23}$
V_{fb}	[V]	0.95	0.35
$x_{\mathsf{TAT,max}}^{\mathsf{s}}$	[nm]	4.0	1.8
N_{t}^{0}	[cm^{-2}]	$5{\cdot}10^{12}$	$5{\cdot}10^{12}$
N_{s}	[cm^{-3}]	$4{\cdot}10^{20}$	$3{\cdot}10^{20}$
N_{d}	[cm^{-3}]	$2{\cdot}10^{20}$	$3{\cdot}10^{20}$

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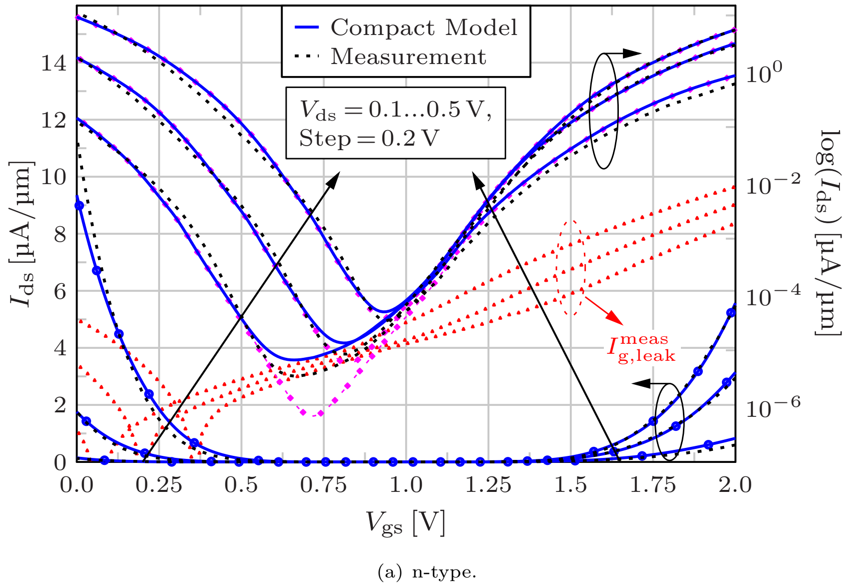
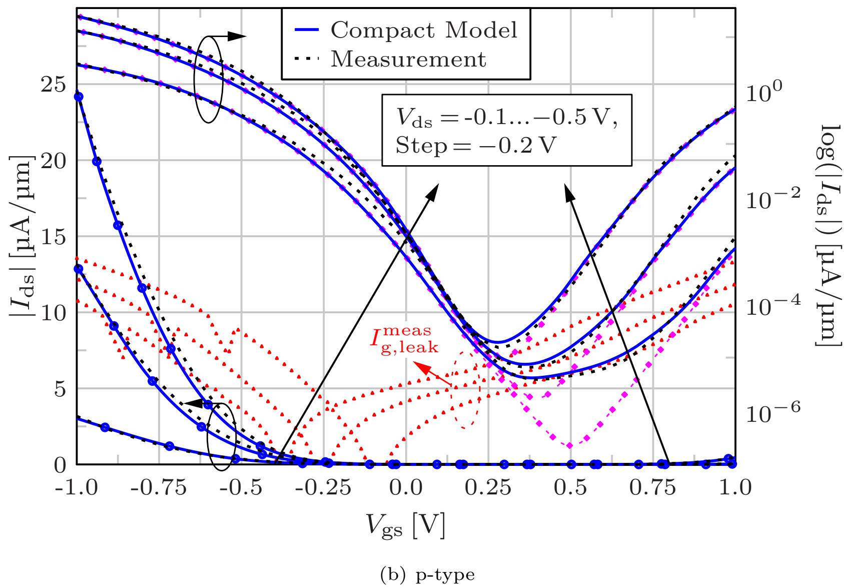


(a) n-type.



(b) p-type

Figure 6.41.: Transfer I-V characteristic measurements of the (a) n- and (b) p-type NW GAA TFETs to validate the compact modeling approach for various V_{ds}. Black dashed lines: Measurements of I_{ds}. Red triangles: Measured gate leakage current $I_{g,leak}^{meas}$. Blue solid lines: Compact model including $I_{g,leak}^{meas}$. Magenta dashed lines with markers: Compact model results.

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CHAPTER 7

Circuit Simulation & Performance Evaluation

In this chapter, the feasibility of using the Verilog-A compact model in basic TFET circuit simulations is demonstrated. The aim of this step is to show and prove the numerical stability, robustness and flexibility of the derived modeling approach. At first, a single-stage inverter is simulated and verified by measurements in Sec. 7.1. Based on the single-stage inverter, a TFET SRAM cell is under investigation in Sec. 7.2. Finally, in Sec. 7.3 an 11-stage ring oscillator simulation is performed to show the capability of the compact model in simulating multiple connected TFET devices. The circuit simulations are performed in the device modeling software IC-CAP from Keysight Technologies [87] and Cadence Virtuoso [86].

7.1 Single-Stage TFET Inverter

In [182], a fabricated single-stage inverter based on complementary TFET technology has been introduced. This is a very good possibility to demonstrate the numerical stability and robustness of the compact model. A schematic TFET inverter layout is shown in Fig. 7.1(a), where Fig. 7.1(b) depicts a microscope image of the fabricated inverter. Each of the fabricated devices, n- and p-type TFET, are verified in terms of the transfer I-V curves in Sec. 6.2.

The available DC measurements of the TFET inverter's voltage transfer characteristics (VTC) are used to verify the simulations using the compact model as it is shown in Fig. 7.2. The simulations are performed in a supply voltage range from $V_{\mathrm{dd}} = 0.6\,\mathrm{V}$ to $1.0\,\mathrm{V}$. It can be seen that the simulated results show a good agreement with the measured VTC for $[0.7\,\mathrm{V} \leq V_{\mathrm{dd}} \leq 0.9\,\mathrm{V}]$ in the whole input voltage range. At $V_{\mathrm{dd}} = 0.6\,\mathrm{V}$, a horizontal displacement of the inverter's switching voltage can be seen. This is maybe caused by the small inaccuracies of the current transfer curves (see Fig. 6.41) and the neglected gate leakage current in the compact model. However, it can be seen that the switching steepness is predicted correctly as well as the amount of the output voltage V_{out} in the high- and low-state of the inverter. For an applied supply voltage of $V_{\mathrm{dd}} = 1.0\,\mathrm{V}$ one can see a mismatch in the switching steepness of the inverter. The simulation results show a steeper switching behavior than the

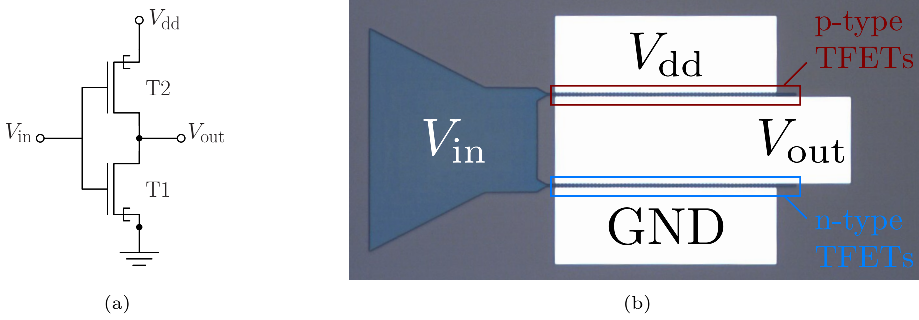

Figure 7.1.: (a) Schematic of the complementary TFET inverter layout, where T1 is the n- and T2 the p-type TFET. (b) Fabricated inverter layout, built with p- and n-type NW GAA TFETs with 60 parallel NWs per device. The source of the p-type TFET is connected to the supply voltage V_{dd} and the source of the n-type device is connected to ground level (GND). Both gates are connected to the inverter's input voltage V_{in}. The output of the inverter is marked by V_{out} [182].

measured VTC. This is caused by an underestimation of the TAT current in the compact model. In addition, the impact of the AMBIPOLAR TFET behavior becomes visible in the inverter's VTC in terms of a output voltage degradation in the low-state of the inverter. The output voltage V_{out} starts to re-increase when the inverter switches from the high- to the low-state for all applied V_{dd} values. In conclusion, it is possible to obtain simulation results with the compact model that are really close to the measurements of the fabricated TFET inverter.

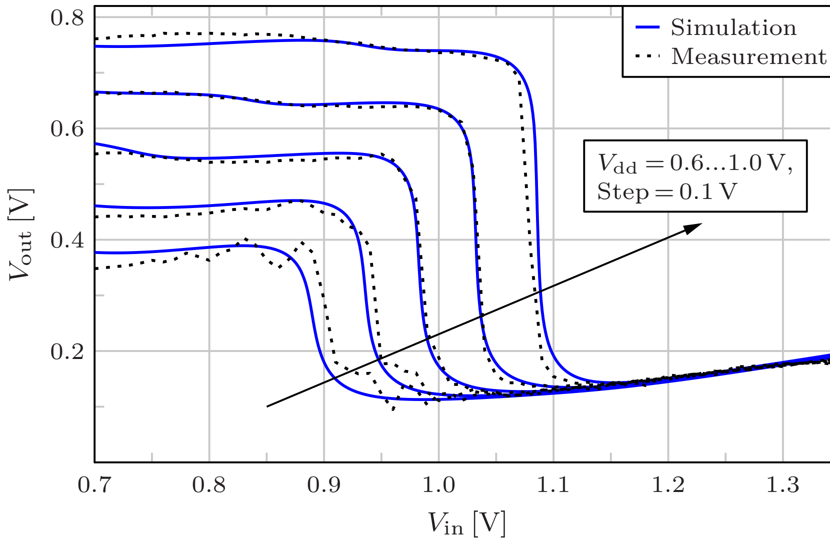

Figure 7.2.: Voltage transfer characteristic of the complementary single-stage TFET inverter for various supply voltages V_{dd}. The simulation results using the compact model are compared to measurement data of the fabricated inverter.

7.2 8T TFET SRAM Cell

After the validation of the transfer I-V curves of the fabricated TFETs and the single-stage TFET inverter, it is possible to simulate a TFET SRAM cell that shows a nearly realistic behavior. The layout of the SRAM cell is introduced in Sec. 7.2.1. The SRAM cell simulations and the cell performance evaluation in terms of the static noise margin (SNM) are presented in Sec. 7.2.2 for various operation regimes of the cell. This study is based on the work published in [134].

7.2.1 Cell Layout

The examined SRAM cell layout is introduced in this section. The circuit design of an SRAM cell using complementary TFET technology is a big challenge in the designers' community, since TFETs have an unidirectional device current and an AMBIPOLAR behavior in the current characteristics [157]. Due to these TFET properties, the conventional 6T SRAM cell layout cannot be applied. In [156, 183], an SRAM cell layout consisting of eight complementary TFETs is reported and successfully simulated. Based on these experiences, the 8T SRAM cell layout shown in Fig. 7.3 is investigated hereinafter.

The 8T TFET SRAM cell consists of two cross-coupled inverters, which are defined by the transistors T1 . . . T4. The transistors T1 and T3 are n-type pull-down (PD) TFETs, whereby T2 and T4 characterize the p-type pull-up (PU) TFETs of the inverters. The two inverters are biased with the supply voltage V_{dd} and controlled by the n-type access transistors (AT) T5 and T6. Due to the unidirectional device current of the TFETs, the ATs are outward-faced and thus enable a robust layout solution for writing operation of the SRAM cell [156]. The output and negated output of the SRAM cell are labeled Q and QB, respectively. The two remaining transistors T7 and T8 form the decoupled circuit for read operations and are both n-type TFETs.

Because of the additional two transistors that form the decoupled read circuit, it is mandatory to use an additional word- and bit line in comparison to the conventional 6T SRAM cell layout. The additional word line for read operations is denoted as $\mathrm{WL_R}$ and the bit line as $\mathrm{BL_R}$. The already existing lines in the conventional layout are used to perform write operations. Therefore, the word line is marked with $\mathrm{WL_W}$, the bit line with $\mathrm{BL_W}$ and the negated bit line with $\mathrm{BLB_W}$.

In the default simulation setup, the cell ratio $\mathrm{CR} = w_{\mathrm{PD}}/w_{\mathrm{AT}}$ is set to one. That means, the access transistors have the same channel width w_{AT} as the pull-down transistors w_{PD}. The reason for choosing a CR = 1 is to achieve simulation results close to the fabricated TFET devices. Since the n-type and p-type TFETs have the same device geometry parameters, all transistors T1 . . . T8 have the same device width $w_x = 40\,\mathrm{nm}$. In order to demonstrate the impact of the AT's device width on the resulting SNM, w_{AT} is varied by an integer multiple of the original device width: $w_{\mathrm{AT,var}} = n \cdot w_{\mathrm{AT}}$, with $(n = 1, 2, 3, \ldots)$.

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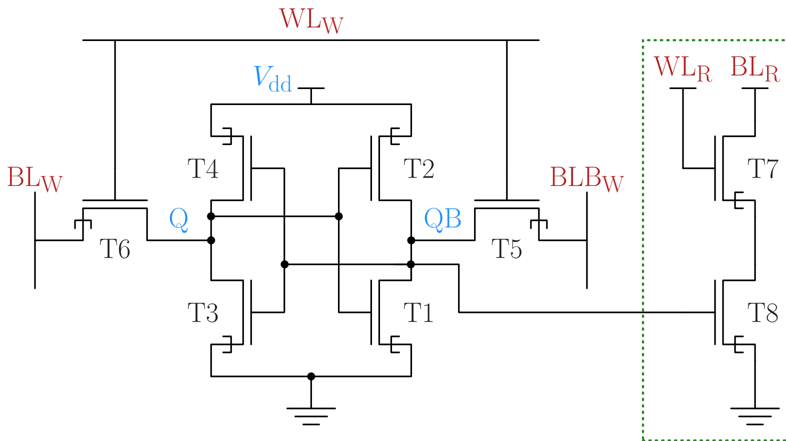

Figure 7.3.: Layout of the 8T TFET SRAM cell [156]. The cross-coupled inverters are made up of the TFETs T1 ... T4. The TFETs T5 and T6 describe the outward-faced access transistors. The decoupled read circuit is located in the dashed green box and is formed by the TFETs T7 and T8.

7.2.2 Simulation Setup and SNM Analysis

The first simulation step shows the analysis of the SNM of the SRAM cell for a hold/read (H/R) operation. In order to simulate a hold operation, at first, the supply voltage V_{dd} is applied, then all bit lines ($\mathrm{BL_W}$, $\mathrm{BLB_W}$ & $\mathrm{BL_R}$) and word lines ($\mathrm{WL_W}$ & $\mathrm{WL_R}$) are biased with zero volts. The state of the flip-flop is not of interest here since Q and QB are swept separately during the SNM analysis. The simulation of a read operation is done by biasing the word line $\mathrm{WL_R}$ with V_{dd} and pre-charging the bit line $\mathrm{BL_R}$ with $V_{\mathrm{dd}}/2$ due to the outward-faced ATs [156], thereby all other lines stay at zero volts.

In order to demonstrate the influence of neighboring SRAM cells on the $\mathrm{SNM_{H/R}}$ of the investigated cell, two additional simulations of a H operation are performed. Since several SRAM cells are connected in a matrix, the bit lines of all cells in a matrix are interconnected as well as the word lines. A possible scenario is that one cell is being read out while something is being written to the cell below. Thus, it can happen that during a read operation of a cell, the bit line $\mathrm{BL_W}$ or $\mathrm{BLB_W}$ is biased. As the word line of this cell is not biased, the values at the bit lines are not written to the cell. However, it has to be investigated, if the voltages at the bit lines have an influence on the cell. So, in the first simulation, V_{dd} is applied and the bit line $\mathrm{BL_W}$ is biased with $V_{\mathrm{dd}}/2$, whereby all other lines stay at zero volts. In the second one, the negated bit line $\mathrm{BLB_W}$ is biased with $V_{\mathrm{dd}}/2$, the cell is supplied with V_{dd} and all other lines stay at zero volts.

The simulated butterfly curves of the SRAM cell in H/R operation for a supply voltage of $V_{\mathrm{dd}} = 0.7\,\mathrm{V}$ are shown in Fig. 7.4(a). The results for hold and read operation are identical in

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consequence of the decoupled read circuit of the examined SRAM layout. The related H/R SNM is calculated as introduced in [184] and yields $\mathrm{SNM_{H/R}} = 121.5\,\mathrm{mV}$. The two additional hold operation simulations result in the same $\mathrm{SNM_H} = 121.5\,\mathrm{mV}$, so it can be seen that a W operation to a neighboring SRAM cell does not influence the cell under investigation. It should be noted that the output voltage degradation of the inverters' VTC rather reduce the resulting SNM, but this effect is not considered in the SNM calculation as it has been presented in [184].

In the next step, simulations are done in order to analyze the SNM for a write (W) operation of the SRAM cell. For this analysis, the inverter curves for writing a logical '1' and a logical '0' are simulated for a supply voltage $V_{\mathrm{dd}} = 0.7\,\mathrm{V}$. In order to write a logical '1', the bit line $\mathrm{BL_W}$ is pre-charged to $V_{\mathrm{dd}}/2$, the negated bit line $\mathrm{BLB_W}$ stays at zero volts, whereafter the writing word line $\mathrm{WL_W}$ is biased with V_{dd}. In the W operation of the SRAM cell the read lines $\mathrm{WL_R}$ and $\mathrm{BL_R}$ stay at zero volts. On the other side, to write a logical '0', the negated bit line $\mathrm{BLB_W}$ is pre-charged with $V_{\mathrm{dd}}/2$, the writing word line is set to $\mathrm{WL_W} = V_{\mathrm{dd}}$ and all other lines are biased with zero volts. The simulation results of the W operation of the SRAM cell are depicted in Fig. 7.4(b), whereby the resulting $\mathrm{SNM_W} = 88.9\,\mathrm{mV}$ is calculated in the same manner as mentioned above. The output voltage degradation of the inverters' VTC reduces the resulting $\mathrm{SNM_W}$ as mentioned above, which is not considered in the SNM calculation.

Based on the simulation setups for hold, read and write operation, the static noise margin is analyzed for various device widths of the ATs. This is done in order to show the influence of different w_{AT} on the resulting SNM. The simulation results are depicted in Fig. 7.5(a), thereby w_{AT} is varied in an integer multiple as it is mentioned in Sec. 7.2.1. It can be seen that the $\mathrm{SNM_{H/R}}$ stays constant for increasing w_{AT}, which is the cause of the decoupled read circuit. In the W operation, the $\mathrm{SNM_W}$ rises for an increasing $w_{\mathrm{AT}}/w_{\mathrm{PD}}$, due to the improved pull-down behavior of the cross-coupled inverters for a wider AT.

Similar to the previous simulation and analysis, now the supply voltage V_{dd} of the logic circuit is varied and the device width of the ATs w_{AT} is kept constant. This means that the simulations are performed with the default SRAM cell layout ($w_{\mathrm{AT}} = w_{\mathrm{PU}} = w_{\mathrm{PD}}$). The influence of the V_{dd} variation on the H/R butterfly curve of the SRAM cell is presented in Fig. 7.4(c). In this figure, the curves for $V_{\mathrm{dd}} = 0.6\,\mathrm{V}$ and $0.8\,\mathrm{V}$ are shown as well as the resulting $\mathrm{SNM_{H/R}}$ squares (1.) and (2.), respectively. The $\mathrm{SNM_{H/R}}$ value of square (1.) is $75.8\,\mathrm{mV}$ and $163.9\,\mathrm{mV}$ for square (2.). It can be seen, that a smaller supply voltage V_{dd} causes a reduced area within the butterfly curves and thus a smaller resulting $\mathrm{SNM_{H/R}}$.

The whole V_{dd} variation in the range from $0.5\,\mathrm{V}$ to $1.0\,\mathrm{V}$ and its influence on $\mathrm{SNM_{H/R}}$ and $\mathrm{SNM_W}$ is presented in Fig. 7.5(b). In Fig. 7.2 and 7.4(c), one can see that a higher supply voltage causes a higher ON/OFF ratio of the cross-coupled inverters, hence the $\mathrm{SNM_{H/R}}$ increases. The reduction of V_{dd} results in a smaller $\mathrm{SNM_W}$ caused by unidirectional device current of the ATs. This behavior deprives the push-pull action during the write operation of the SRAM cell [183]. Furthermore, the AMBIPOLAR behavior of TFETs causes an output

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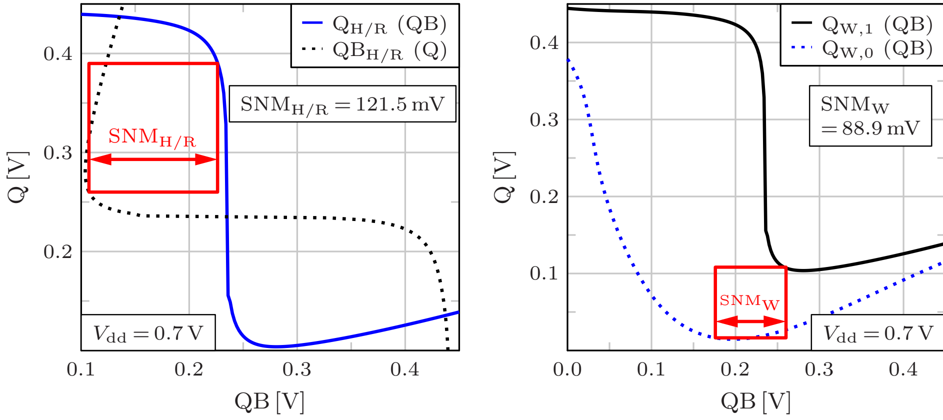
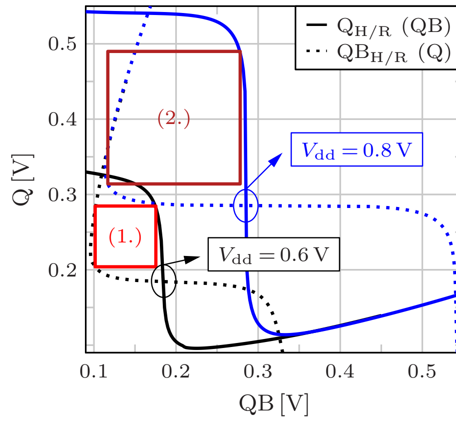
voltage degradation of the inverter's VTC as mentioned before.



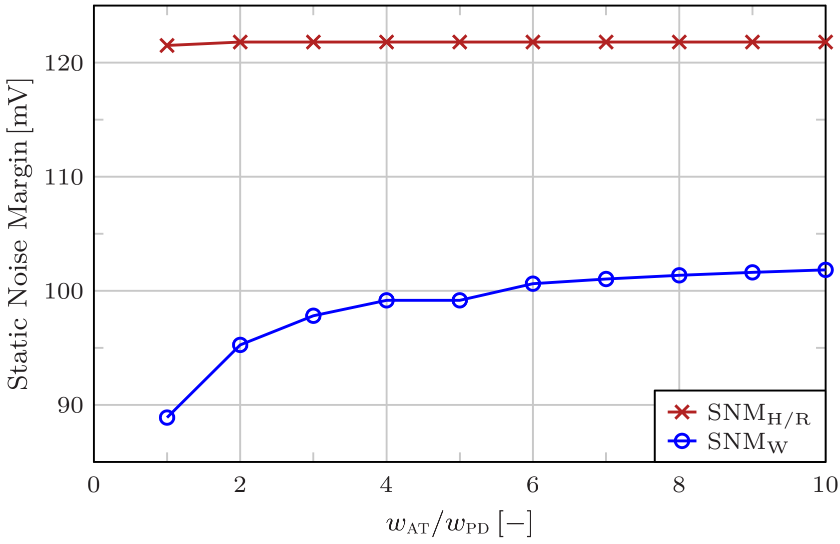
(a) Hold/Read operation, V_{dd} = 0.7 V.

(b) Write operation, V_{dd} = 0.7 V.

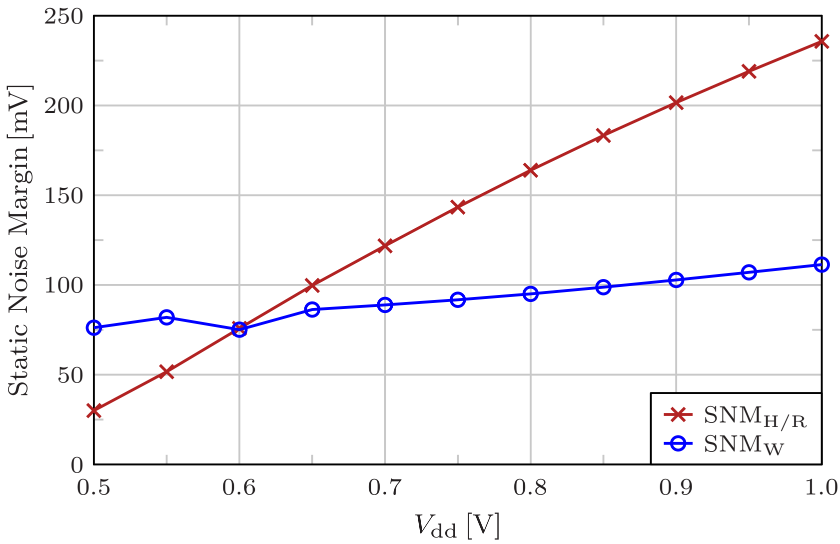


(c) Hold/Read operation, Various V_{dd}.

Figure 7.4.: (a) Simulation results of the butterfly curve for the 8T TFET SRAM cell in hold/read operation and a supply voltage V_{dd} = 0.7 V. The SNM square is highlighted by the red box. (b) Resulting inverter curves of the SRAM cell in write operation. The red square illustrates the resulting $\mathrm{SNM_W}$. Solid black line: Writing a logical '1'. Blue dashed line: Writing a logical '0'. (c) H/R butterfly curves for V_{dd} = 0.6 V and 0.8 V showing the resulting SNM squares.



(a)



(b)

Figure 7.5.: (a) Simulation results of the SNM for the SRAM cell in hold/read and write operation for a varying w_{AT}/w_{PD} ratio and a supply voltage of $V_{dd} = 0.7\,V$. Here, the width of the ATs w_{AT} is varied and the width of the PD and PU TFETs stays constant ($w_{PU} = w_{PD}$). (b) $SNM_{H/R}$ and SNM_W analysis for different supply voltages V_{dd} and the default SRAM cell layout ($w_{AT} = w_{PU} = w_{PD}$).

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7.3 Ring Oscillator

In the next simulation, the transient response of an 11-stage TFET ring oscillator is examined. For this purpose, the presented compact DC model is combined with a compact AC model of the intrinsic TFET capacitances published in [139]. The transient behavior of a TFET-based single-stage inverter for various device parameters has been investigated in [140] and has shown the capability of the combined compact AC and DC model. With the help of these simulation results it is also possible to simulate a TFET-based 11-stage ring oscillator shown in Fig. 7.6. The impact of the ON-state current on the ring oscillator's performance has been investigated in [141].

The results of the transient output voltage V_{out} and current I_{out} response are presented in Fig. 7.7, where it should be noted that the TFETs used in the inverters are single-gate devices [141]. In the transient simulation result one can see eleven switching processes in the output current I_{out} within one period of the output voltage V_{out}. Thus, every single inverter switches once within a period of V_{out}. At the applied supply voltage of $V_{\mathrm{dd}} = 0.4\,\mathrm{V}$, the output voltage period results in $T = 15\,\mathrm{ns}$. In addition to numerical stability and flexibility, these results also show the performance of the compact model when simulating multiple TFET devices. The transient response of the 11-stage ring oscillator including 22 TFET devices has been achieved in less than one minute.

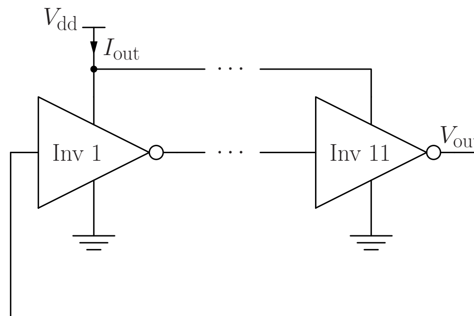

Figure 7.6.: Schematic of the 11-stage TFET ring oscillator showing the output voltage V_{out} and current I_{out}.

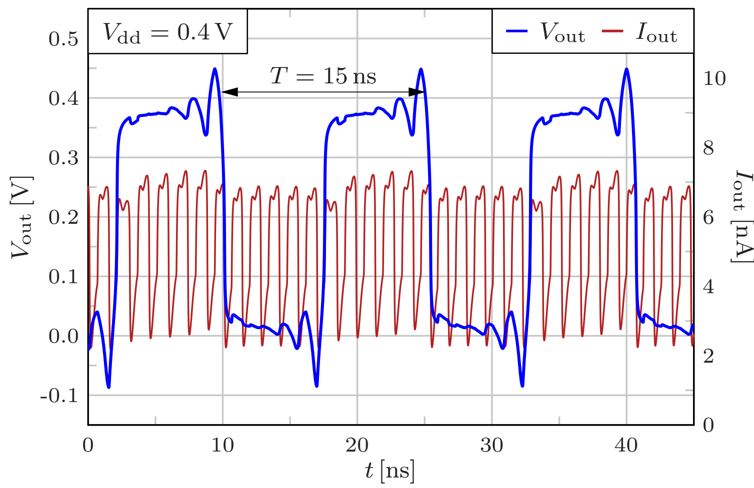

Figure 7.7.: Transient simulation results of the 11-stage TFET ring oscillator. The simulated inverters are based on single-gate TFETs. Left y-axis: Output voltage V_{out} (blue line) with a resulting period of one oscillation of $T = 15\,ns$. Right y-axis: Output current I_{out} (red line).

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CHAPTER 8

Conclusion

This dissertation presents a compact DC model for DG TFETs considering the B2B tunneling and the TAT effect in the calculations of the device current. All model equations are analytically solved, include 2D effects and allow for an implementation in the hardware description language Verilog-A.

The compact modeling approach is derived on the basis of an analytical-numerical 2D DG TFET model of our workgroup reported in [128, 129, 131]. It is essential to have an accurate solution of the electrostatics for the calculations of the device current in TFETs. Hence, the potential solution in the compact model is derived with the help of the 2D closed-form potential solution of the analytical-numerical model. However, this closed-form solution is not suitable for a time-efficient Verilog-A implementation and thus, the device potential in the compact model is approximated by mathematical functions. After carefully investigating the potential shape in TCAD Sentaurus simulation results, the potential along the x-axis within the channel of the TFET is approximated by a rational function $\propto {}^{1}/{x}$. The rational function is used to define the potential in the first and the second half of the channel separately. The potentials within the source and drain region are approximated by a parabolic function $\propto x^2$ in order to take into account the impact of the depletion regions on the resulting B2B tunneling current. The parameters that define the potential approximation functions are extracted by using seven potential values of the 2D analytical electrostatic potential solution. Based on the potential approximation along the x-axis, it is possible to describe the potential along the y-axis, which points in the direction of the channel thickness, by a polynomial function. The parameters of this function are determined by picking a potential value at the surface and the center of the channel and the exponent of the function is calculated considering the effect of inversion charges. For this reason, the analytical potential solution is extended by taking into account the effect of inversion charges on the electrostatics. Considering the first derivative of the potential in x and y direction, it is possible to find a compact description for the absolute value of the electric field.

The band diagram of the TFET is determined by an application of the compact potential solution. Due to the high doping concentrations of the source and drain region, the effect of band gap narrowing is taken into account. The compact equations also allow for a calculation of the consideration in heterostructure TFETs.

The tunneling probability for the B2B tunneling and TAT is calculated with the help of an area-equivalent WKB approach. In this model part, the tunneling energy barrier is approximated with the help of a triangular energy profile, which has an equal area as the energy barrier defined by the band diagram. In the calculations of the area-equivalent triangle, a compact expression describing the tunneling distance is used, which is derived on the basis of the band diagram.

Landauer's tunneling formula is applied to describe the B2B tunneling generation rate along the x-axis for an arbitrary y-position in the channel region of the DG TFET. A compact expression is found by approximating the TGR with a Gaussian distribution function, that allows a closed-form integration in order to obtain the tunneling current density along the y-axis. In case of TAT, the generation rate formula is rearranged by combining Landauer's tunneling formula and the TAT model of Hurkx, where a closed-form expression is obtained after an approximation by a Gaussian distribution function. The current density along the y-axis also needs to be approximated since a closed-form integration is not possible. A compact expression that characterizes the first half of the channel is also found by using a Gaussian distribution function. An integration of the compact current density results in the tunneling current of the DG TFET, including both the B2B tunneling and TAT current part in the ON- and AMBIPOLAR-state of the device. After finding a compact solution of the device current, the modeling equations are implemented in Verilog-A.

The compact DC model verification is firstly done with the help of TCAD Sentaurus simulations of an n-type DG TFET for various simulation parameter setups and secondly by measurements of complementary fabricated TFETs. The electrostatic potential, the band diagram and the absolute value of the electric field are extracted from the TCAD simulations to prove the accuracy of the derived compact potential model, the electric field solution and the band diagram model for various bias conditions and a varying source material. The comparison of the modeling results with TCAD data shows a good agreement in dependency of x and y.

After demonstrating the accuracy of the compact band diagram, the area-equivalent WKB approach is investigated. The resulting triangular tunneling energy barrier is illustrated within the band diagram in order to highlight the feasibility of this approach. The results shows that the AE WKB approach is very suitable to reproduce the tunneling energy barrier formed by the band diagram. Furthermore, the AE WKB approach is compared to a quasi-2D WKB approximation, where the AE WKB approach offers a better match in terms of the tunneling barrier height for various applied bias conditions and source materials. In contrast to the quasi-2D approximation, the AE WKB approach is suitable for a numerically robust implementation

in Verilog-A. In the next step, the B2B TGR is plotted against the TCAD simulation results and shows a good match for various bias conditions and materials of the source region.

The I-V characteristics of the DG TFET are used to show the flexibility of the compact DC model. Firstly, the compact model is verified by TCAD simulation data in terms of the current output characteristics and its first and second derivative for various applied bias conditions. In a second step, TCAD simulations of the current transfer curve are performed for different applied bias conditions and various device parameters, like geometrical dimensions, materials or doping concentrations. The comparison with TCAD data shows a good agreement even in the first and second derivative of the transfer I-V curve. In addition, the compact model offers a good scalability regarding a change in the device dimensions and in the gate insulator material without readjusting the extracted model parameters. Regarding a change in the source material to heterostructures, the compact model stays in a good agreement with the simulations in TCAD.

In order to highlight the feasibility of adapting the model approach to other geometries, the compact model parameters are readjusted so that a simulation of a nanowire gate-all-around TFET is possible. Here, the p-type model is emulated from the n-type modeling approach. With the help of transfer I-V curve measurements of fabricated complementary devices, the compact model validity is proven. The modeling results for various drain-source voltages shows a good match with the measured data for both the n- and p-type TFET.

Using the compact model parameters that are extracted for the fabricated TFETs, it is possible to perform a DC simulation of a single-stage TFET inverter. The simulations results for various supply voltages are compared to measurements of a fabricated TFET inverter and offer a good match, even the parasitic effects like TAT or the AMBIPOLAR behavior of the TFET are very well reproduced in the simulations. Furthermore, a DC simulation of a TFET-based SRAM cell is performed and analyzed in terms of the static noise margin. The simulations are done with the modeling parameters extracted for the fabricated devices in order to obtain nearly realistic simulation results. Finally, the DC model is extended by a compact AC model of the intrinsic capacitances in TFETs, which allows for a transient simulation of an 11-stage ring oscillator. All the simulations of basic TFET circuits demonstrate the numerical stability, continuity and flexibility of the compact model.

Finally, in conclusion it is to say that a compact DC model for TFETs is developed which offers a good possibility to perform TFET-based circuit simulations in a very time-efficient and accurate way. The modeling approach is derived for a DG TFET but is not limited to this device structure. Beside the B2B tunneling current model, the approach also considers the parasitic TAT effect.

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Regarding the state-of-the-art TFET technology, it is to say that there are a lot of problems to be solved concerning the enhancement of the ON-state current and at the same time the reduction of the traps at the channel junction. Another important issue is the suppression of the AMBIPOLAR-state current. The research community is still working in the optimization of the TFET as a possible successor of the conventional MOSFETs and the presented compact model allows a fast simulation and evaluation of single TFETs and TFET-based circuits.

Due to the fact that some effects influencing the TFET behavior are not included in the modeling approach, the compact model should be extended in future work. At first, the effect of the gate leakage current should be taken into account as it was reported in [185]. Secondly, a possible way to suppress the AMBIPOLAR-state of the TFET is to consider a gate underlap at the drain-to-channel junction as it has been demonstrated by TCAD simulations in [178, 179]. A possible model approach was introduced in [111]. A last possible step to extend the compact model could be the transformation of the DG structure into arbitrarily shaped structures with the help of scaling concepts as it was presented for MOSFET devices in [186, 187].

APPENDIX A

Separation of Real- and Imaginary Parts of the 2D Complex Potential

The compact DC model presented in Chap. 5 is derived in a way that it can easily be implemented in the hardware description language Verilog-A. For that purpose some complex equations of the 2D electrostatic potential solution must be rearranged, since Verilog-A is not able to handle complex expressions. The complex expressions are separated into their real and imaginary parts in the following, that allows a usage the Verilog-A language.

A.1 Conformal Mapping Function

The function to map an arbitrary point within the complex $\bar{z}$-plane into the upper half of the $\bar{w}$-plane has been introduced in Sec. 4.1.5.

Source Related Case

The mapping function for the source related case is given by (see Eq. (4.37)):

$$\bar{w}_{\mathrm{s}}(\bar{z}) = u + \mathrm{j}v = \cosh\left(\frac{\pi}{\varDelta y}\cdot(x+\mathrm{j}y)\right), \tag{A.1}$$

which can be separated into its real u and imaginary part v as follows:

$$u(\bar{z}) = \mathrm{Re}\{\bar{w}\} = \mathrm{Re}\left\{\cosh\left(\frac{\pi}{\varDelta y}\cdot(x+\mathrm{j}y)\right)\right\} = \cosh\left(\frac{\pi\cdot x}{\varDelta y}\right)\cdot\cos\left(\frac{\pi\cdot y}{\varDelta y}\right), \tag{A.2}$$

$$v(\bar{z}) = \mathrm{Im}\{\bar{w}\} = \mathrm{Im}\left\{\cosh\left(\frac{\pi}{\varDelta y}\cdot(x+\mathrm{j}y)\right)\right\} = \sinh\left(\frac{\pi\cdot x}{\varDelta y}\right)\cdot\sin\left(\frac{\pi\cdot y}{\varDelta y}\right). \tag{A.3}$$

Drain Related Case

The mapping function for the drain related case is presented in Eq. (4.38):

$$\bar{w}_{\mathrm{d}}(\bar{z}) = \cosh\left(\frac{\pi}{\varDelta y}\cdot(l_{\mathrm{ch}}-x+\mathrm{j}y)\right), \tag{A.4}$$

where a separation of the real and imaginary part yields:

$$u(\bar{z}) = \mathrm{Re}\{\bar{w}\} = \mathrm{Re}\left\{\cosh\left(\frac{\pi}{\mathit{\Delta} y}\cdot(l_{\mathrm{ch}} - x + \mathrm{j}y)\right)\right\}$$
$$= \cosh\left(\frac{\pi\cdot(l_{\mathrm{ch}} - x)}{\mathit{\Delta} y}\right)\cdot\cos\left(\frac{\pi\cdot y}{\mathit{\Delta} y}\right), \tag{A.5}$$

$$v(\bar{z}) = \mathrm{Im}\{\bar{w}\} = \mathrm{Im}\left\{\cosh\left(\frac{\pi}{\mathit{\Delta} y}\cdot(l_{\mathrm{ch}} - x + \mathrm{j}y)\right)\right\}$$
$$= \sinh\left(\frac{\pi\cdot(l_{\mathrm{ch}} - x)}{\mathit{\Delta} y}\right)\cdot\sin\left(\frac{\pi\cdot y}{\mathit{\Delta} y}\right). \tag{A.6}$$

A.2 Potential Solution for a Piecewise Parabolic Boundary

The potential solution for a piecewise parabolic boundary condition is introduced in Sec. 4.2.2. The electrostatic potential solution presented in Eq. (4.45) is separated into its real and imaginary part in the following. The solution reads as:

$$\phi_{\mathrm{P}}\left(\bar{w}_{\mathrm{s/d}}(\bar{z})\right) = \mathit{\Delta\Phi}_{\mathrm{P}}\cdot\left[\frac{1}{2}\cdot\left(\sqrt{1-(u-\mathrm{j}v)^2} + \sqrt{1-(u+\mathrm{j}v)^2}\right) - v\right]. \tag{A.7}$$

In the first step, the terms $(u \pm \mathrm{j}v)^2$ within the square roots are rewritten in complex polar coordinates:

$$(u\pm\mathrm{j}v)^2 = \left(\sqrt{(u^2+v^2)}\right)^2\cdot\exp\left(\pm 2\mathrm{j}\cdot\arctan\left(\frac{v}{u}\right)\right)$$
$$= \underbrace{\left(u^2+v^2\right)}_{M}\cdot\exp\left(\pm 2\mathrm{j}\cdot\underbrace{\arctan\left(\frac{v}{u}\right)}_{\delta}\right)$$
$$= M\cdot\exp\left(\pm 2\mathrm{j}\cdot\delta\right) = M\cdot\cos(2\delta)\pm\mathrm{j}M\cdot\sin(2\delta). \tag{A.8}$$

In the next step, the square roots are rearranged. It follows:

$$\sqrt{1-(u\mp\mathrm{j}v)^2} = \sqrt{1-M\cdot\cos(2\delta)\pm\mathrm{j}M\cdot\sin(2\delta)} = \sqrt{A\pm\mathrm{j}B} \tag{A.9}$$
$$= \sqrt[4]{A^2+B^2}\cdot\exp\left(\pm\frac{1}{2}\mathrm{j}\cdot\underbrace{\arctan\left(\frac{B}{A}\right)}_{\gamma}\right) = \sqrt[4]{A^2+B^2}\cdot\exp\left(\pm\mathrm{j}\cdot\frac{\gamma}{2}\right).$$

In the last step, Eq. (A.9) is applied to the potential solution in Eq. (A.7):

$$\begin{aligned}\phi_{\mathrm{P}}\left(\bar{w}_{\mathrm{s/d}}(\bar{z})\right) &= \mathit{\Delta\Phi}_{\mathrm{P}} \cdot \left[\frac{1}{2} \cdot \left(\sqrt[4]{A^2+B^2} \cdot \underbrace{\left[\exp\left(+\mathrm{j}\cdot\frac{\gamma}{2}\right) + \exp\left(-\mathrm{j}\cdot\frac{\gamma}{2}\right)\right]}_{2\cdot\cos\left(\frac{\gamma}{2}\right)}\right) - v\right] \\ &= \mathit{\Delta\Phi}_{\mathrm{P}} \cdot \left[\sqrt[4]{A^2+B^2} \cdot \cos\left(\frac{\gamma}{2}\right) - v\right] \end{aligned} \tag{A.10}$$

whereby the obtained equation allows for an implementation in Verilog-A.

A.3 Potential Solution for a Piecewise Linear Boundary

The complex solution for a piecewise linear boundary condition (see Eq. (4.52)) is separated into a real and imaginary part. The solution is given by:

$$\begin{aligned}\phi_{\mathrm{L}}\left(\bar{w}_{\mathrm{s/d}}(\bar{z})\right) = \pm\frac{\mathrm{j}}{\pi}&\left[\sigma_{\mathrm{L},3}\cdot\arctan\left(\frac{a_{\mathrm{L}}\cdot u\cdot\sigma_{\mathrm{L},1}\cdot\sigma_{\mathrm{L},3} - a_{\mathrm{L}}\cdot b_{\mathrm{L}}\cdot\sigma_{\mathrm{L},1}\cdot\sigma_{\mathrm{L},3} + \mathrm{j}\cdot a_{\mathrm{L}}\cdot v\cdot\sigma_{\mathrm{L},1}\cdot\sigma_{\mathrm{L},3}}{\sigma_{\mathrm{L},4}}\right)\right. \\ &\left.\left. + \;\sigma_{\mathrm{L},2}\cdot\arctan\left(\frac{a_{\mathrm{L}}\cdot b_{\mathrm{L}}\cdot\sigma_{\mathrm{L},1}\cdot\sigma_{\mathrm{L},2} - a_{\mathrm{L}}\cdot u\cdot\sigma_{\mathrm{L},1}\cdot\sigma_{\mathrm{L},2} + \mathrm{j}\cdot a_{\mathrm{L}}\cdot v\cdot\sigma_{\mathrm{L},1}\cdot\sigma_{\mathrm{L},2}}{\sigma_{\mathrm{L},4}}\right)\right]\right|_{u'_{\mathrm{a}}}^{u'_{\mathrm{b}}}, \end{aligned} \tag{A.11}$$

with:

$$\begin{aligned} \sigma_{\mathrm{L},1} = \sqrt{-\frac{b_{\mathrm{L}}-u'}{a_{\mathrm{L}}}}, \quad \sigma_{\mathrm{L},2} = \sqrt{\frac{b_{\mathrm{L}}-u-\mathrm{j}v}{a_{\mathrm{L}}}}, \quad \sigma_{\mathrm{L},3} = \sqrt{\frac{b_{\mathrm{L}}-u+\mathrm{j}v}{a_{\mathrm{L}}}}, \\ \sigma_{\mathrm{L},4} = b_{\mathrm{L}}^2 - 2\cdot b_{\mathrm{L}}\cdot u + u^2 + v^2. \end{aligned} \tag{A.12}$$

Firstly, the simplifications $\sigma_{\mathrm{L},2}$ and $\sigma_{\mathrm{L},3}$ are rewritten in complex polar form with their magnitude M_{L} and argument θ_{L}:

$$\begin{aligned}\sigma_{\mathrm{L},2/3} &= \sqrt[4]{\left(\frac{b_{\mathrm{L}}-u}{a_{\mathrm{L}}}\right)^2 + \left(\frac{v}{a_{\mathrm{L}}}\right)^2} \cdot \exp\left(\mp\mathrm{j}\frac{1}{2}\cdot\arctan\left(\frac{v}{b_{\mathrm{L}}-u}\right)\right) \\ &= M_{\mathrm{L}}\cdot\exp\left(\mp\mathrm{j}\theta_{\mathrm{L}}\right). \end{aligned} \tag{A.13}$$

Next, Eq. (A.11) is rewritten as:

$$\phi_{\mathrm{L}}\left(\bar{w}_{\mathrm{s/d}}(\bar{z})\right) = \pm\frac{\mathrm{j}}{\pi}\cdot\left.\left[\sigma_{\mathrm{L},3}\cdot\arctan\left(A_1+\mathrm{j}B_1\right) + \sigma_{\mathrm{L},2}\cdot\arctan\left(A_2+\mathrm{j}B_2\right)\right]\right|_{u'_{\mathrm{a}}}^{u'_{\mathrm{b}}}, \tag{A.14}$$

thereby:

$$\begin{aligned} A_1 &= \frac{a_\mathrm{L} \cdot u \cdot \sigma_{\mathrm{L},1} \cdot \sigma_{\mathrm{L},3} - a_\mathrm{L} \cdot b_\mathrm{L} \cdot \sigma_{\mathrm{L},1} \cdot \sigma_{\mathrm{L},3}}{\sigma_{\mathrm{L},4}} = \frac{a_\mathrm{L} \cdot \sigma_{\mathrm{L},1}}{\sigma_{\mathrm{L},4}} \cdot \sigma_{\mathrm{L},3} \cdot (u - b_\mathrm{L}) \\ &= \frac{a_\mathrm{L} \cdot \sigma_{\mathrm{L},1}}{\sigma_{\mathrm{L},4}} \cdot M_\mathrm{L} \cdot \exp(+\mathrm{j}\theta_\mathrm{L}) \cdot (u - b_\mathrm{L}) \\ &= \frac{a_\mathrm{L} \cdot \sigma_{\mathrm{L},1}}{\sigma_{\mathrm{L},4}} \cdot M_\mathrm{L} \cdot \cos(\theta_\mathrm{L}) \cdot (u - b_\mathrm{L}) + \mathrm{j}\frac{a_\mathrm{L} \cdot \sigma_{\mathrm{L},1}}{\sigma_{\mathrm{L},4}} \cdot M_\mathrm{L} \cdot \sin(\theta_\mathrm{L}) \cdot (u - b_\mathrm{L}), \end{aligned} \tag{A.15}$$

$$\begin{aligned} B_1 &= \frac{a_\mathrm{L} \cdot v \cdot \sigma_{\mathrm{L},1} \cdot \sigma_{\mathrm{L},3}}{\sigma_{\mathrm{L},4}} = \frac{a_\mathrm{L} \cdot v \cdot \sigma_{\mathrm{L},1}}{\sigma_{\mathrm{L},4}} \cdot M_\mathrm{L} \cdot \exp(+\mathrm{j}\theta_\mathrm{L}) \\ &= \frac{a_\mathrm{L} \cdot v \cdot \sigma_{\mathrm{L},1}}{\sigma_{\mathrm{L},4}} \cdot M_\mathrm{L} \cdot \cos(\theta_\mathrm{L}) + \mathrm{j}\frac{a_\mathrm{L} \cdot v \cdot \sigma_{\mathrm{L},1}}{\sigma_{\mathrm{L},4}} \cdot M_\mathrm{L} \cdot \sin(\theta_\mathrm{L}), \end{aligned} \tag{A.16}$$

$$\begin{aligned} A_2 &= \frac{a_\mathrm{L} \cdot b_\mathrm{L} \cdot \sigma_{\mathrm{L},1} \cdot \sigma_{\mathrm{L},2} - a_\mathrm{L} \cdot u \cdot \sigma_{\mathrm{L},1} \cdot \sigma_{\mathrm{L},2}}{\sigma_{\mathrm{L},4}} = \frac{a_\mathrm{L} \cdot \sigma_{\mathrm{L},1}}{\sigma_{\mathrm{L},4}} \cdot \sigma_{\mathrm{L},2} \cdot (b_\mathrm{L} - u) \\ &= \frac{a_\mathrm{L} \cdot \sigma_{\mathrm{L},1}}{\sigma_{\mathrm{L},4}} \cdot M_\mathrm{L} \cdot \exp(-\mathrm{j}\theta_\mathrm{L}) \cdot (b_\mathrm{L} - u) \\ &= \frac{a_\mathrm{L} \cdot \sigma_{\mathrm{L},1}}{\sigma_{\mathrm{L},4}} \cdot M_\mathrm{L} \cdot \cos(\theta_\mathrm{L}) \cdot (b_\mathrm{L} - u) - \mathrm{j}\frac{a_\mathrm{L} \cdot \sigma_{\mathrm{L},1}}{\sigma_{\mathrm{L},4}} \cdot M_\mathrm{L} \cdot \sin(\theta_\mathrm{L}) \cdot (b_\mathrm{L} - u), \end{aligned} \tag{A.17}$$

and

$$\begin{aligned} B_2 &= \frac{a_\mathrm{L} \cdot v \cdot \sigma_{\mathrm{L},1} \cdot \sigma_{\mathrm{L},2}}{\sigma_{\mathrm{L},4}} = \frac{a_\mathrm{L} \cdot v \cdot \sigma_{\mathrm{L},1}}{\sigma_{\mathrm{L},4}} \cdot M_\mathrm{L} \cdot \exp(-\mathrm{j}\theta_\mathrm{L}) \\ &= \frac{a_\mathrm{L} \cdot v \cdot \sigma_{\mathrm{L},1}}{\sigma_{\mathrm{L},4}} \cdot M_\mathrm{L} \cdot \cos(\theta_\mathrm{L}) - \mathrm{j}\frac{a_\mathrm{L} \cdot v \cdot \sigma_{\mathrm{L},1}}{\sigma_{\mathrm{L},4}} \cdot M_\mathrm{L} \cdot \sin(\theta_\mathrm{L}). \end{aligned} \tag{A.18}$$

It can be seen that the resulting expressions Eq. (A.15)–(A.18) still consist of complex values and therefore the expressions are reordered as follows:

$$\begin{aligned} A_1 + \mathrm{j}B_1 = &\underbrace{\frac{a_\mathrm{L} \cdot \sigma_{\mathrm{L},1} \cdot M_\mathrm{L}}{\sigma_{\mathrm{L},4}} \cdot \Big[(u - b_\mathrm{L}) \cdot \cos(\theta_\mathrm{L}) - v \cdot \sin(\theta_\mathrm{L})\Big]}_{C_1} \\ &+ \mathrm{j} \underbrace{\frac{a_\mathrm{L} \cdot \sigma_{\mathrm{L},1} \cdot M_\mathrm{L}}{\sigma_{\mathrm{L},4}} \cdot \Big[(u - b_\mathrm{L}) \cdot \sin(\theta_\mathrm{L}) + v \cdot \cos(\theta_\mathrm{L})\Big]}_{D_1}, \end{aligned} \tag{A.19}$$

$$\begin{aligned} A_2 + \mathrm{j}B_2 = &\underbrace{\frac{a_\mathrm{L} \cdot \sigma_{\mathrm{L},1} \cdot M_\mathrm{L}}{\sigma_{\mathrm{L},4}} \cdot \Big[(b_\mathrm{L} - u) \cdot \cos(\theta_\mathrm{L}) + v \cdot \sin(\theta_\mathrm{L})\Big]}_{C_2} \\ &+ \mathrm{j} \underbrace{\frac{a_\mathrm{L} \cdot \sigma_{\mathrm{L},1} \cdot M_\mathrm{L}}{\sigma_{\mathrm{L},4}} \cdot \Big[-(b_\mathrm{L} - u) \cdot \sin(\theta_\mathrm{L}) + v \cdot \cos(\theta_\mathrm{L})\Big]}_{D_2}. \end{aligned} \tag{A.20}$$

By inserting these expressions in Eq. (A.14) yields:

$$\phi_{\mathrm{L}}\left(\bar{w}_{\mathrm{s/d}}(\bar{z})\right) = \pm\frac{\mathrm{j}}{\pi}\cdot\left[\sigma_{\mathrm{L},3}\cdot\arctan\left(C_1+\mathrm{j}D_1\right)+\sigma_{\mathrm{L},2}\cdot\arctan\left(C_2+\mathrm{j}D_2\right)\right]\Bigg|_{u'_{\mathrm{a}}}^{u'_{\mathrm{b}}}, \tag{A.21}$$

whereby in the calculation of the parameters $C_1 \dots D_2$ in dependency of $\sigma_{\mathrm{L},1}$, it is distinguished between two cases:

Case I $(b_{\mathrm{L}}-u)/a_{\mathrm{L}} \leq 0$:

$$C_1 = \frac{a_{\mathrm{L}}\cdot\sigma_{\mathrm{L},1}\cdot M_{\mathrm{L}}}{\sigma_{\mathrm{L},4}}\cdot\left[(u-b_{\mathrm{L}})\cdot\cos(\theta_{\mathrm{L}})-v\cdot\sin(\theta_{\mathrm{L}})\right], \tag{A.22}$$

$$D_1 = \frac{a_{\mathrm{L}}\cdot\sigma_{\mathrm{L},1}\cdot M_{\mathrm{L}}}{\sigma_{\mathrm{L},4}}\cdot\left[(u-b_{\mathrm{L}})\cdot\sin(\theta_{\mathrm{L}})+v\cdot\cos(\theta_{\mathrm{L}})\right], \tag{A.23}$$

$$C_2 = \frac{a_{\mathrm{L}}\cdot\sigma_{\mathrm{L},1}\cdot M_{\mathrm{L}}}{\sigma_{\mathrm{L},4}}\cdot\left[(b_{\mathrm{L}}-u)\cdot\cos(\theta_{\mathrm{L}})+v\cdot\sin(\theta_{\mathrm{L}})\right], \tag{A.24}$$

$$D_2 = \frac{a_{\mathrm{L}}\cdot\sigma_{\mathrm{L},1}\cdot M_{\mathrm{L}}}{\sigma_{\mathrm{L},4}}\cdot\left[-(b_{\mathrm{L}}-u)\cdot\sin(\theta_{\mathrm{L}})+v\cdot\cos(\theta_{\mathrm{L}})\right]. \tag{A.25}$$

Case II $(b_{\mathrm{L}}-u)/a_{\mathrm{L}} > 0$: $\sigma_{\mathrm{L},1}$ is replaced by:

$$\sigma'_{\mathrm{L},1} = \sqrt{\frac{b_{\mathrm{L}}-u}{a_{\mathrm{L}}}} \tag{A.26}$$

and the parameters are calculated by:

$$C_1 = -\frac{a_{\mathrm{L}}\cdot\sigma'_{\mathrm{L},1}\cdot M_{\mathrm{L}}}{\sigma_{\mathrm{L},4}}\cdot\left[(u-b_{\mathrm{L}})\cdot\sin(\theta_{\mathrm{L}})+v\cdot\cos(\theta_{\mathrm{L}})\right], \tag{A.27}$$

$$D_1 = \frac{a_{\mathrm{L}}\cdot\sigma'_{\mathrm{L},1}\cdot M_{\mathrm{L}}}{\sigma_{\mathrm{L},4}}\cdot\left[(u-b_{\mathrm{L}})\cdot\cos(\theta_{\mathrm{L}})-v\cdot\sin(\theta_{\mathrm{L}})\right], \tag{A.28}$$

$$C_2 = \frac{a_{\mathrm{L}}\cdot\sigma'_{\mathrm{L},1}\cdot M_{\mathrm{L}}}{\sigma_{\mathrm{L},4}}\cdot\left[(b_{\mathrm{L}}-u)\cdot\sin(\theta_{\mathrm{L}})-v\cdot\cos(\theta_{\mathrm{L}})\right], \tag{A.29}$$

$$D_2 = \frac{a_{\mathrm{L}}\cdot\sigma'_{\mathrm{L},1}\cdot M_{\mathrm{L}}}{\sigma_{\mathrm{L},4}}\cdot\left[(b_{\mathrm{L}}-u)\cdot\cos(\theta_{\mathrm{L}})+v\cdot\sin(\theta_{\mathrm{L}})\right]. \tag{A.30}$$

Next, the arctan has to be solved for a complex value. The solution for the first term is given by:

$$\arctan(C_1+\mathrm{j}D_1) = E_1+\mathrm{j}F_1, \tag{A.31}$$

with:

$$E_1 = \mathrm{Re}\{\arctan(C_1 + \mathrm{j}D_1)\} = \begin{cases} \frac{\pi}{4} - \frac{1}{2} \cdot \arctan\left(\frac{1-C_1^2-D_1^2}{2 \cdot C_1}\right) & : \quad C_1 > 0 \\ -\frac{\pi}{4} - \frac{1}{2} \cdot \arctan\left(\frac{1-C_1^2-D_1^2}{2 \cdot C_1}\right) & : \quad C_1 > 0 \\ 0 & : \quad C_1 = 0,\ -1 \leq D_1 \leq 1 \\ \frac{\pi}{2} & : \quad C_1 = 0,\ D_1 > 1 \\ -\frac{\pi}{2} & : \quad C_1 = 0,\ D_1 < 1, \end{cases} \tag{A.32}$$

$$F_1 = \mathrm{Im}\{\arctan(C_1 + \mathrm{j}D_1)\} = \frac{1}{2} \cdot \tanh^{-1}\left(\frac{2 \cdot D_1}{C_1^2 + D_1^2 + 1}\right). \tag{A.33}$$

The second term is solved as follows:

$$\arctan(C_2 + \mathrm{j}D_2) = E_2 + \mathrm{j}F_2, \tag{A.34}$$

whereby:

$$E_2 = \mathrm{Re}\{\arctan(C_2 + \mathrm{j}D_2)\} = \begin{cases} \frac{\pi}{4} - \frac{1}{2} \cdot \arctan\left(\frac{1-C_2^2-D_2^2}{2 \cdot C_2}\right) & : \quad C_2 > 0 \\ -\frac{\pi}{4} - \frac{1}{2} \cdot \arctan\left(\frac{1-C_2^2-D_2^2}{2 \cdot C_2}\right) & : \quad C_2 > 0 \\ 0 & : \quad C_2 = 0,\ -1 \leq D_2 \leq 1 \\ \frac{\pi}{2} & : \quad C_2 = 0,\ D_2 > 1 \\ -\frac{\pi}{2} & : \quad C_2 = 0,\ D_2 < 1, \end{cases} \tag{A.35}$$

$$F_2 = \mathrm{Im}\{\arctan(C_2 + \mathrm{j}D_2)\} = \frac{1}{2} \cdot \tanh^{-1}\left(\frac{2 \cdot D_2}{C_2^2 + D_2^2 + 1}\right). \tag{A.36}$$

By applying these simplifications, Eq. (A.21) reduces to:

$$\phi_{\mathrm{L}}\big(\bar{w}_{\mathrm{s/d}}(\bar{z})\big) = \pm\frac{\mathrm{j}}{\pi} \cdot \left[\sigma_{\mathrm{L},3} \cdot (E_1 + \mathrm{j}F_1) + \sigma_{\mathrm{L},2} \cdot (E_2 + \mathrm{j}F_2)\right]\Big|_{u'_{\mathrm{a}}}^{u'_{\mathrm{b}}}. \tag{A.37}$$

Now, using the complex polar form of $\sigma_{\mathrm{L},2/3}$ (see Eq. (A.13)) in Eq. (A.37) leads to:

$$\begin{aligned}
\phi_{\mathrm{L}}\big(\bar{w}_{\mathrm{s/d}}(\bar{z})\big) &= \pm\,\frac{\mathrm{j}}{\pi}\cdot\Big[M_{\mathrm{L}}\cdot\exp\left(+\mathrm{j}\theta_{\mathrm{L}}\right)\cdot\left(E_1+\mathrm{j}F_1\right)+M_{\mathrm{L}}\cdot\exp\left(-\mathrm{j}\theta_{\mathrm{L}}\right)\cdot\left(E_2+\mathrm{j}F_2\right)\Big]\Big|_{u'_{\mathrm{a}}}^{u'_{\mathrm{b}}} \\
&= \pm\Big[\mathrm{j}\frac{M_{\mathrm{L}}}{\pi}\cdot\big(\cos(\theta_{\mathrm{L}})+\mathrm{j}\sin(\theta_{\mathrm{L}})\big)\cdot\left(E_1+\mathrm{j}F_1\right) \\
&\quad +\mathrm{j}\frac{M_{\mathrm{L}}}{\pi}\cdot\big(\cos(\theta_{\mathrm{L}})-\mathrm{j}\sin(\theta_{\mathrm{L}})\big)\cdot\left(E_2+\mathrm{j}F_2\right)\Big]\Big|_{u'_{\mathrm{a}}}^{u'_{\mathrm{b}}} \\
\phi_{\mathrm{L}}\big(\bar{w}_{\mathrm{s/d}}(\bar{z})\big) &= \pm\Big[\frac{M_{\mathrm{L}}}{\pi}\cdot\big[(E_2-E_1)\cdot\sin(\theta_{\mathrm{L}})-(F_1+F_2)\cdot\cos(\theta_{\mathrm{L}})\big] \\
&\quad +\mathrm{j}\frac{M_{\mathrm{L}}}{\pi}\cdot\big[(E_1+E_2)\cdot\cos(\theta_{\mathrm{L}})+(F_2-F_1)\cdot\sin(\theta_{\mathrm{L}})\big]\Big]\Big|_{u'_{\mathrm{a}}}^{u'_{\mathrm{b}}}.
\end{aligned} \tag{A.38}$$

Finally, applying the complex potential theory (see Sec. 2.2), the potential solution for a piecewise linear boundary condition between u'_{a} and u'_{b} is determined by the real part of Eq. (A.38). A separation of this equation into its real and imaginary part results in:

$$\mathrm{Re}\left\{\phi_{\mathrm{L}}\big(\bar{w}_{\mathrm{s/d}}(\bar{z})\big)\right\} = \pm\,\frac{M_{\mathrm{L}}}{\pi}\cdot\big[(E_2-E_1)\cdot\sin(\theta_{\mathrm{L}})-(F_1+F_2)\cdot\cos(\theta_{\mathrm{L}})\big]\Big|_{u'_{\mathrm{a}}}^{u'_{\mathrm{b}}}, \tag{A.39}$$

$$\mathrm{Im}\left\{\phi_{\mathrm{L}}\big(\bar{w}_{\mathrm{s/d}}(\bar{z})\big)\right\} = \pm\,\frac{M_{\mathrm{L}}}{\pi}\cdot\big[(E_1+E_2)\cdot\cos(\theta_{\mathrm{L}})+(F_2-F_1)\cdot\sin(\theta_{\mathrm{L}})\big]\Big|_{u'_{\mathrm{a}}}^{u'_{\mathrm{b}}}, \tag{A.40}$$

whereby the sign of the real and imaginary part is determined by the applied boundary conditions $\Phi_{\mathrm{L},1}$ and $\Phi_{\mathrm{L},2}$ as it is introduced in Sec. 4.2.3.

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APPENDIX B

Verilog-A Suitable Function Approximations

In order to implement the compact DC model (see Chap. 5) in Verilog-A, it is necessary to find a suitable approximation of the Fermi-Dirac integral and the error function. The approximations of these two functions are presented hereinafter.

B.1 Fermi-Dirac Integral

In order to consider the effect of inversion charges on the resulting TFET potential (see Sec. 4.1.2), it is necessary to have a compact description of the Fermi-Dirac integral. In general, the integral is defined by:

$$\mathcal{F}_j(\eta) = \int_0^{\infty} \frac{x^j}{\exp(x-\eta)+1}\,\mathrm{d}x, \quad (j > -1), \tag{B.1}$$

with the order j of the Fermi-Dirac integral and the variable η, where the integral is calculated. There is no closed-form solution of the integral and therefore an analytical approximation has been introduced by Aymerich-Humet [188]. The Fermi-Dirac integral for the whole range of η and any real value of j can be approximated by:

$$\mathcal{F}_j(\eta) \approxeq \frac{1}{\frac{(j+1)\cdot 2^{(j+1)}}{\left[b+\eta+(|\eta-b|^c+a^c)^{\frac{1}{c}}\right]^{(j+1)}} + \frac{\exp(-\eta)}{\Gamma(j+1)}}, \tag{B.2}$$

using the gamma function Γ and the unknown parameters are defined by:

$$a = \sqrt{1+\frac{15}{4}\cdot(j+1)+\frac{1}{40}\cdot(j+1)^2}, \tag{B.3}$$

$$b = 1.8 + 0.61\cdot j, \tag{B.4}$$

$$c = 2 + \left(2-\sqrt{2}\right)\cdot 2^{-j}. \tag{B.5}$$

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The approximation in Eq. (B.2) is suitable for an implementation of the Fermi-Dirac integral in Verilog-A.

B.2 Error Function

The error function is needed to calculate the compact tunneling current density in Sec. 5.4.4 and Sec. 5.5.4 as well as the compact tunneling current in Sec. 5.6. In [189] a closed-form approximation of the error function has been proposed which is defined in the interval $[0 \leq x \leq \infty]$. The approximation reads as:

$$\operatorname{erf}(x) = 1 - \left(a_1 \cdot t + a_2 \cdot t^2 + a_3 \cdot t^3\right) \cdot \exp\left(-x^2\right), \tag{B.6}$$

with the parameters:

$$t(x) = \frac{1}{1 + p \cdot x}, \tag{B.7}$$

$$p = 0.47047, \tag{B.8}$$

$$a_1 = 0.3480242, \tag{B.9}$$

$$a_2 = -0.0958798, \tag{B.10}$$

$$a_3 = 0.7478556. \tag{B.11}$$

By using the point reflection of the error function, which means $\operatorname{erf}(-x) = -\operatorname{erf}(x)$, the interval of this approximation can be extended to the interval $[-\infty \leq x \leq \infty]$. So, the approximation in Eq. (B.6) is appropriated for a closed-form implementation in Verilog-A.

APPENDIX C

Terminal Input Voltage Limitations

In order to ensure the continuity of the compact model for bias conditions far away from the practical working region of the TFET, the terminal input voltages must be smoothly saturated to a constant value [91]. The smooth limitation of the terminal voltages improves the convergence of the compact model during the simulation iterations.

At first, the input drain-source voltage $V_{\mathrm{ds,in}}$ is smoothly limited for negative and positive values. In the case of negative drain-source voltages $V_{\mathrm{ds}} < -0.1\,\mathrm{V}$, the TFET turns into a forward biased diode and this effect is not considered in the compact modeling approach. For this reason, negative V_{ds} values are limited by the following function [31, 160]:

$$V_{\mathrm{ds}}^{*} = V_{\mathrm{ds,sat}}^{(\text{-})} \cdot \left[1 - \frac{1}{\ln(1+\exp(A_{\mathrm{sat}}))} \cdot \ln\left(1 + \exp\left(A_{\mathrm{sat}} \cdot \left(1 - \frac{V_{\mathrm{ds,in}}}{V_{\mathrm{ds,sat}}^{(\text{-})}}\right)\right)\right)\right], \qquad \text{(C.1)}$$

where $V_{\mathrm{ds,sat}}^{(\text{-})}$ is set to $-0.1\,\mathrm{V}$ and the parameter $A_{\mathrm{sat}} \approx 10$. $V_{\mathrm{ds,in}}$ defines the non-saturated input terminal voltage. The obtained V_{ds}^{*} is subsequently saturated for positive values as follows:

$$V_{\mathrm{ds}} = V_{\mathrm{ds,sat}}^{(+)} \cdot \left[1 - \frac{1}{\ln(1+\exp(A_{\mathrm{sat}}))} \cdot \ln\left(1 + \exp\left(A_{\mathrm{sat}} \cdot \left(1 - \frac{V_{\mathrm{ds}}^{*}}{V_{\mathrm{ds,sat}}^{(+)}}\right)\right)\right)\right] \qquad \text{(C.2)}$$

and results in the drain-source voltage V_{ds} that is applied to the compact model in Chap. 5. The positive saturation voltage is set to $V_{\mathrm{ds,sat}}^{(+)} = 1.5\,\mathrm{V}$. The smoothly saturated drain-source voltages V_{ds}^{*} and V_{ds} are plotted against the input drain-source voltage $V_{\mathrm{ds,in}}$ in Fig. C.1(a).

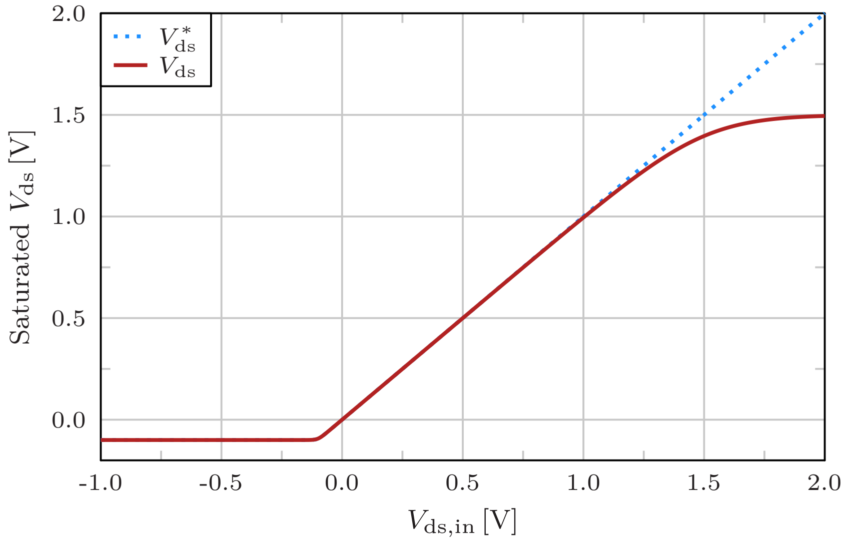
In the next step, the applied input gate-source voltage $V_{\mathrm{gs,in}}$ is smoothly limited for positive and due to the AMBIPOLAR behavior of the TFET also for negative values. The limitation is done by applying the aforementioned smoothing functions and hence, for negative values it follows:

$$V_{\mathrm{gs}}^{*} = -V_{\mathrm{gs,sat}} \cdot \left[1 - \frac{1}{\ln(1+\exp(A_{\mathrm{sat}}))} \cdot \ln\left(1 + \exp\left(A_{\mathrm{sat}} \cdot \left(1 + \frac{V_{\mathrm{gs,in}} - V_{\mathrm{fb}}}{V_{\mathrm{gs,sat}}}\right)\right)\right)\right], \quad \text{(C.3)}$$

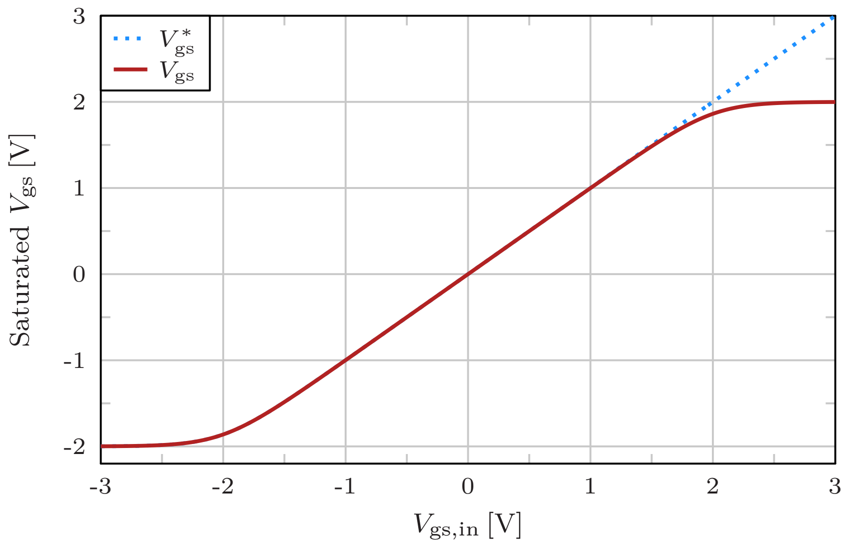
using the saturation voltage $V_{\mathrm{gs,sat}}$, the input gate-source voltage $V_{\mathrm{gs,in}}$ and the flat band voltage V_{fb}. The resulting value for V_{gs}^{*} is then applied to saturate positive applied input gate-source voltages which leads to:

$$V_{\mathrm{gs}} = V_{\mathrm{gs,sat}} \cdot \left[1 - \frac{1}{\ln(1+\exp(A_{\mathrm{sat}}))} \cdot \ln\left(1 + \exp\left(A_{\mathrm{sat}} \cdot \left(1 - \frac{V_{\mathrm{gs}}^{*}}{V_{\mathrm{gs,sat}}}\right)\right)\right)\right]. \quad \text{(C.4)}$$

Here, the saturation voltage is set to $V_{\mathrm{gs,sat}} = 2\,\mathrm{V}$. The resulting V_{gs} is applied to compact modeling approach in Chap. 5. Figure C.1(b) shows the obtained V_{gs}^{*} and V_{gs} in contrast to the input gate-source voltage $V_{\mathrm{gs,in}}$.



(a)



(b)

Figure C.1.: Smoothly saturated input terminal voltages, where (a) shows the saturated voltage for negative values V^*_{ds} and V_{ds} considers a smooth limitation for both positive and negative input voltages $V_{ds,in}$. In (b), the saturated V^*_{gs} (negative $V_{gs,in}$) and V_{gs} (negative & positive $V_{gs,in}$) are plotted against $V_{gs,in}$.

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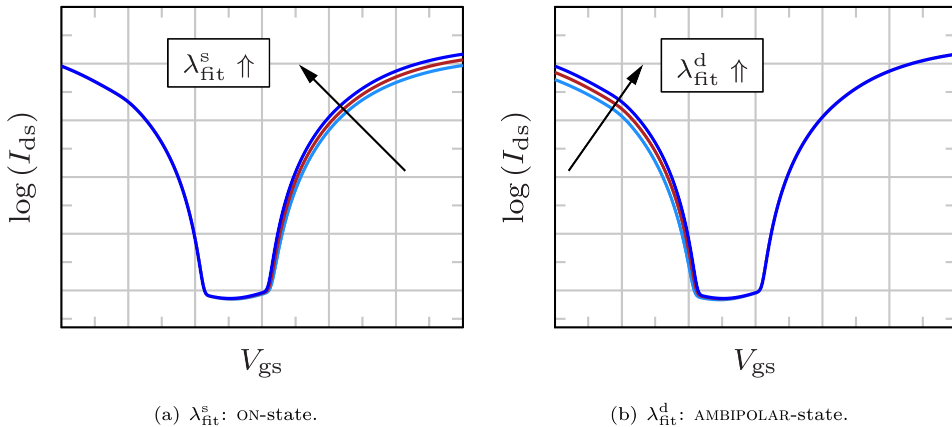
APPENDIX D

Impact of the Adjustable Model Parameters on the Transfer I-V Curve

In the derivation of the compact DC model several adjustable parameters are introduced that have differing influence on the TFET behavior. The impact of the adjustable model parameters, which are listed in Tab. 6.2, on the transfer I-V characteristics of the TFET is qualitatively presented in this chapter. Figures D.1 to D.8 show the influence of the corresponding parameter on the ON-state of transfer curve in (a), whereby the AMBIPOLAR-state influence in each case is shown in (b). In addition to the qualitative illustration of the parameter influence on the transfer curve, each parameter is explained in the corresponding figure caption including suitable parameter ranges.

Impact of the Parameter $\lambda_{\mathrm{fit}}^{\mathrm{s/d}}$:

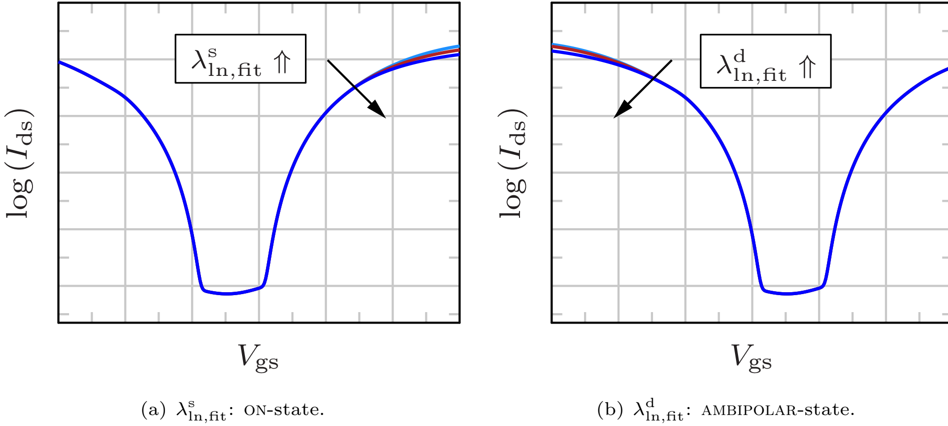


(a) $\lambda_{\mathrm{fit}}^{\mathrm{s}}$: ON-state.

(b) $\lambda_{\mathrm{fit}}^{\mathrm{d}}$: AMBIPOLAR-state.

Figure D.1.: The parameter $\lambda_{\mathrm{fit}}^{\mathrm{s/d}}$ is used to tune the resulting screening length $\lambda_{\mathrm{s/d}}$ at the channel junctions in the potential model of the TFET. For an increasing value, the transfer curve is fanned out and I_{ds} is increased. The typical range of $\lambda_{\mathrm{fit}}^{\mathrm{s/d}}$ is from 0.5 to 2.0.

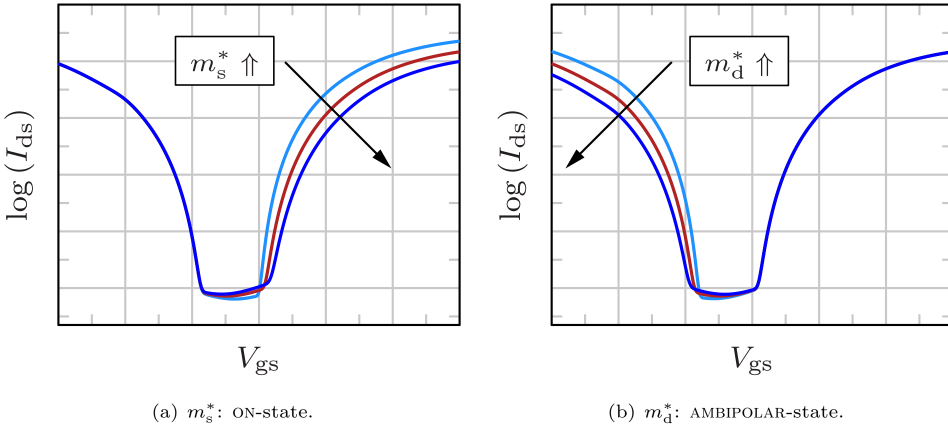
Impact of the Parameter $\lambda^{\mathrm{s/d}}_{\mathrm{ln,fit}}$:



(a) $\lambda^{\mathrm{s}}_{\mathrm{ln,fit}}$: ON-state. (b) $\lambda^{\mathrm{d}}_{\mathrm{ln,fit}}$: AMBIPOLAR-state.

Figure D.2.: The parameter $\lambda^{\mathrm{s/d}}_{\mathrm{ln,fit}}$ is applied to change the influence of the inversion charges on the resulting potential solution at the channel junctions. The parameters are defined in the interval $[0.2 \leq \lambda^{\mathrm{s/d}}_{\mathrm{ln,fit}} \leq \infty)$. The smaller the value of $\lambda^{\mathrm{s/d}}_{\mathrm{ln,fit}}$, the higher is the influence of inversion charges on the electrostatics and the transfer curve.

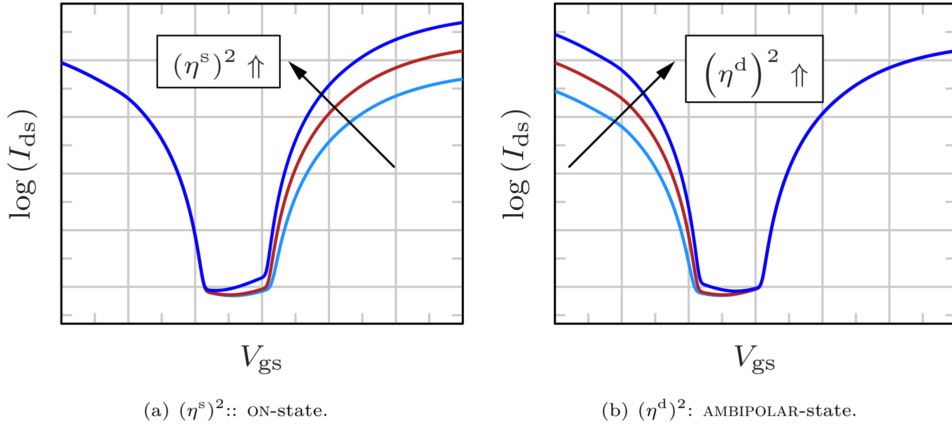
Impact of the Parameter $m^*_{\mathrm{s/d}}$:



(a) m^*_{s}: ON-state. (b) m^*_{d}: AMBIPOLAR-state.

Figure D.3.: The effective carrier masses $m^*_{\mathrm{s/d}}$ have a linear and an exponential impact on the TGR and therefore on the resulting B2B tunneling and TAT current. The TGR is linearly dependent on $m^*_{\mathrm{s/d}}$ and T_{tun} is exponentially dependent on $m^*_{\mathrm{s/d}}$. The effective carrier masses should be chosen in the range from $0.05{\cdot}m_0$ to $0.7{\cdot}m_0$.

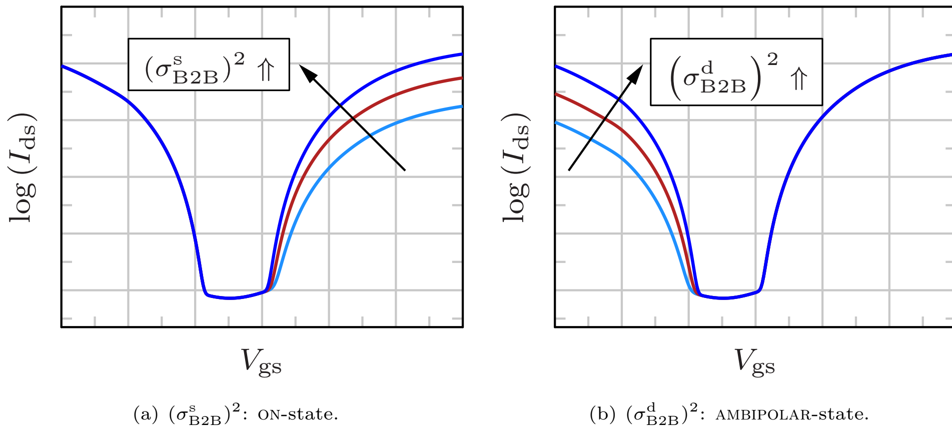
Impact of the Parameter $(\eta^{\mathsf{s/d}})^2$:



(a) $(\eta^{s})^2$:: ON-state. (b) $(\eta^{d})^2$: AMBIPOLAR-state.

Figure D.4.: The variance $(\eta^{s/d})^2$ occurs in the compact current density calculations along the y-axis and has a linear dependency on I_{ds} and an inverse proportional dependency in the error function term in the I_{ds} calculations. The linear dependency dominates in the case, when the error function saturates to the value 1. $(\eta^{s/d})^2$ is defined in the range $[0 < (\eta^{s/d})^2 \leq t_{ch}^2]$.

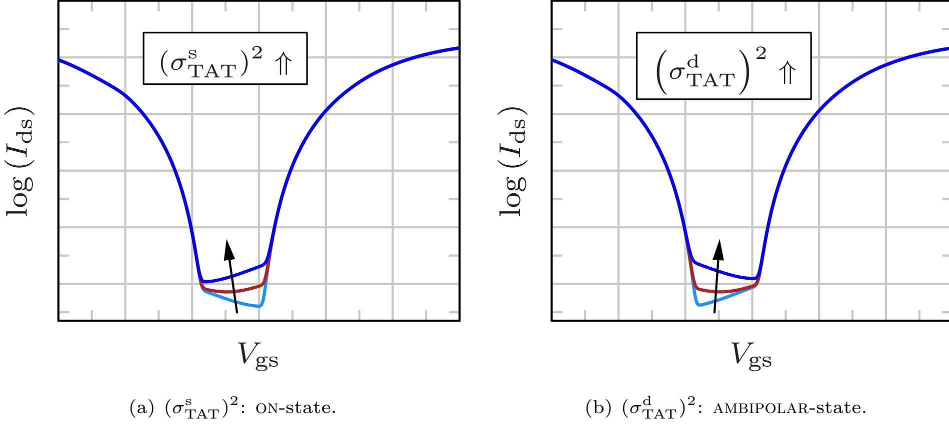
Impact of the Parameter $(\sigma_{\mathsf{B2B}}^{\mathsf{s/d}})^2$:



(a) $(\sigma^{s}_{B2B})^2$: ON-state. (b) $(\sigma^{d}_{B2B})^2$: AMBIPOLAR-state.

Figure D.5.: The variance $(\sigma_{B2B}^{s/d})^2$ occurs in the calculations of the B2B tunneling generation rate and has nearly the same influence on B2B tunneling part of I_{ds} as $(\eta^{s/d})^2$. The variance $(\sigma_{B2B}^{s/d})^2$ should smaller than $({}^{l_{ch}}/_{4})^2$.

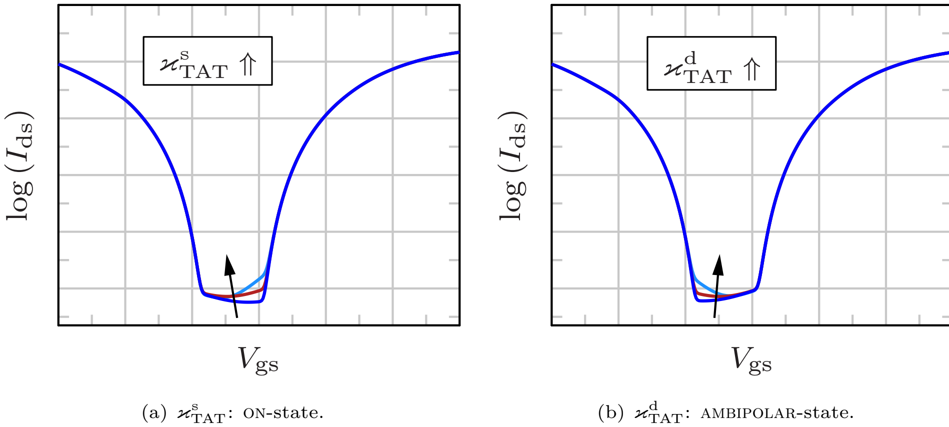
Impact of the Parameter $(\sigma_{\mathrm{TAT}}^{\mathrm{s/d}})^2$:



(a) $(\sigma_{\mathrm{TAT}}^{\mathrm{s}})^2$: ON-state. (b) $(\sigma_{\mathrm{TAT}}^{\mathrm{d}})^2$: AMBIPOLAR-state.

Figure D.6.: The variance $(\sigma_{\mathrm{TAT}}^{\mathrm{s/d}})^2$ is used in the TAT generation rate calculations along the x-axis and scales the resulting TAT current part in the same way than the variance $(\sigma_{\mathrm{B2B}}^{\mathrm{s/d}})^2$ in the B2B tunneling current calculation (see Fig. D.5).

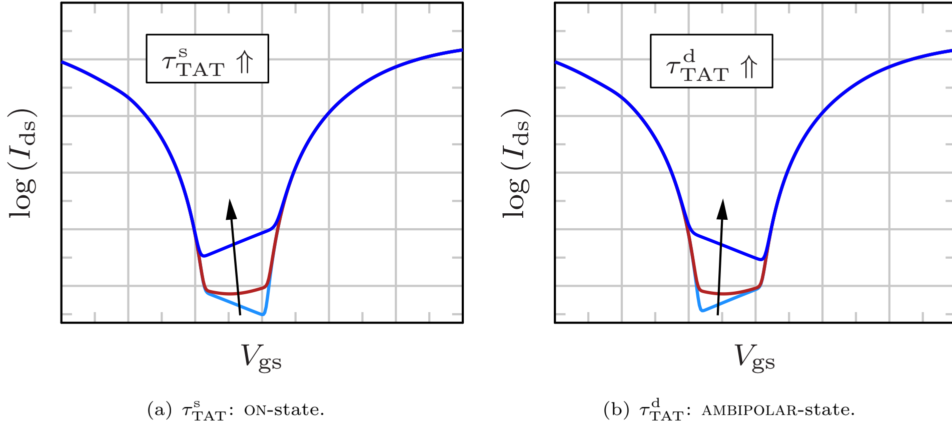
Impact of the Parameter $\varkappa_{\mathrm{TAT}}^{\mathrm{s/d}}$:



(a) $\varkappa_{\mathrm{TAT}}^{\mathrm{s}}$: ON-state. (b) $\varkappa_{\mathrm{TAT}}^{\mathrm{d}}$: AMBIPOLAR-state.

Figure D.7.: The fitting parameter $\varkappa_{\mathrm{TAT}}^{\mathrm{s/d}}$ can be used to tune the resulting slope of the TAT current part. The smaller the value of $\varkappa_{\mathrm{TAT}}^{\mathrm{s/d}}$, the steeper the resulting slope, whereby the amount of the TAT current has to be adapted by the parameter $\tau_{\mathrm{TAT}}^{\mathrm{s/d}}$ afterwards. The typical range is from 1.0 to 1000.

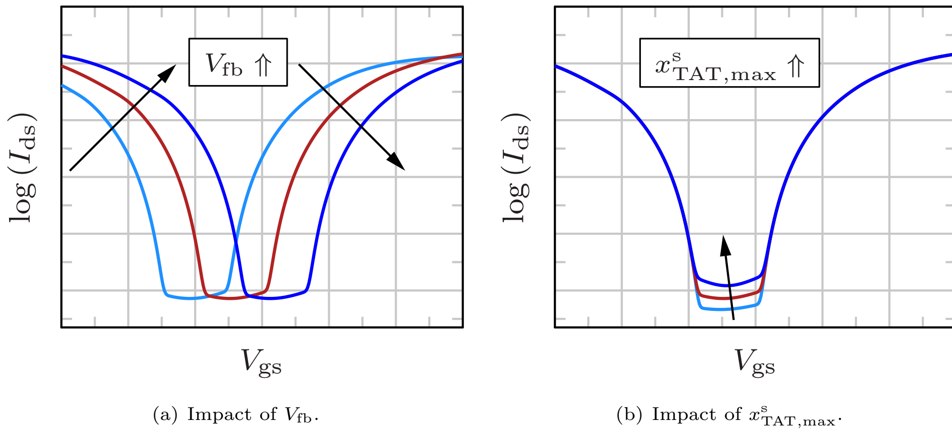
Impact of the Parameter $\tau_{\mathrm{TAT}}^{\mathrm{s/d}}$:



(a) $\tau_{\mathrm{TAT}}^{\mathrm{s}}$: ON-state. (b) $\tau_{\mathrm{TAT}}^{\mathrm{d}}$: AMBIPOLAR-state.

Figure D.8.: The capture cross section $\tau_{\mathrm{TAT}}^{\mathrm{s/d}}$ is used as a linear adjustable factor in the TAT current part calculations. The amount of the parameter has to be positive and has a typical range from $10^{-23}\mathrm{cm}^2$ to $10^{-18}\mathrm{cm}^2$.

Impact of the Parameters V_{fb} and $x_{\mathrm{TAT,max}}^{\mathrm{s}}$:



(a) Impact of V_{fb}. (b) Impact of $x_{\mathrm{TAT,max}}^{\mathrm{s}}$.

Figure D.9.: The flat band voltage V_{fb} in (a) is used to capture a change in the work function of the gate contact metal. An increasing V_{fb} causes a right shift of the transfer I-V curve. The parameter $x_{\mathrm{TAT,max}}^{\mathrm{s}}$ determines the x-position of the $\mathrm{TGR}_{\mathrm{TAT}}$ maximum. Typical range: $[0 < x_{\mathrm{TAT,max}}^{\mathrm{s}} < {}^{l_{\mathrm{ch}}}/2]$.

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