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Direct current control for grid connected multilevel inverters

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PhD thesis

Direct Current Control for Grid Connected Multilevel Inverters

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I would like to dedicate this thesis to my loving wife, my wonderful children and my parents

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Abstract

Control schemes for inverters of different topologies and various numbers of voltage levels are of great interest for many standard as well as special applications. This thesis describes a novel, robust and high-dynamic direct current control scheme for multilevel voltage source inverters. It is highly independent from load parameters and universally applicable. The new control method is examined and validated with real measurements.

The aim of the thesis is to establish and prove a new concept of a direct current control algorithm for multilevel inverter topologies for grid connected systems. This application is characterized by unknown grid conditions including failure modes and other distortions, complex inverter topologies and a large variety and complexity of current control algorithms for multilevel inverters. Therefore the complexity of the system needs to be reduced. Additionally, the advantages of multilevel inverters and the dynamic performance and robustness of direct current control techniques shall be combined. Starting from a detailed literature study on inverter topologies and direct as well as indirect current control methods, the thesis includes three chapters containing relevant contributions to the achievement of the objectives.

A method reducing the control-complexity of multilevel converters has been developed. The simplification method is based on a transformation that converts any three-phase voltage (or current) into a non-orthogonal coordinate system. This choice minimizes the complexity and effort to determine the location of those discrete voltage space vectors directly surrounding the required reference voltage vector. A further improvement is achieved by scaling all coordinates to integer values. This is advantageous for further calculations on microprocessors or FPGA based control systems.

The main contribution of this thesis is a new direct current control method minimizing the disadvantages of existing direct methods. At the same time advantages of other control algorithms shall be applied. The new method is based on a simple mathematical equation, that is, the solution of a scalar product, to always select the one inverter output voltage vector best reducing the actual current error. This results in the designation "Scalar Hysteresis Control - SHC". An advanced seeking algorithm ensures robust current control capability even in case of unknown, unsymmetrical or changing loads, in case of rapid set-point changes or in cases of unknown phase voltages.

The new method therefore shows excellent properties in terms of simplicity, robustness, dynamics and independence from the inverter level count and the hardware topology. The properties of the control method are verified by means of simulations and real measurements on two-, three- and five-level inverters over the complete voltage operating range.

Finally, all contributions are collected together and assessed with regard to the objectives. From the proposed control method new opportunities for future work, further developments and extensions are evolving for continuing scientific research.

Resum

Els sistemes de control d'inversors de diferents topologies i diferent varis nivells de tensió són de gran interès per moltes aplicacions estàndard i també per aplicacions especials. Aquesta tesi investiga sobre un mètode de control directe de corrent per convertidors multinivell en font de tensió que es mostra robust i presenta una elevada dinàmica en el control de corrent. El mètode és molt robust davant de canvies als paràmetres de la càrrega i aplicable a qualsevol tipus de convertidor. En aquesta tesi s'analitza el mètode i es valida mitjançant resultats experimentals.

L'objectiu d'aquesta tesi és establir i demostrar un nou de mètode i algorisme de control directe de corrent aplicat especialment a inversors connectats a la xarxa. L'aplicació es caracteritza per la desconeixença dels paràmetres de la xarxa, incloent diferents modes de falla i distorsions en la seva tensió i una varietat de tipologies de convertidors multinivell. El mètode de control busca simplificar l'algorisme i que pugui ser aplicat en aquest entorn de forma robusta, de forma que es pugui estendre l'ús dels convertidors multinivell sense afegir més complexitat als algorismes de control i modulació.

La tesi aborda el problema iniciant amb un anàlisi de la literatura existent en aquest tipus de mètodes de control directe i indirecte del corrent i els convertidors multinivell, per continuar amb l'anàlisi del mètode proposat i la seva demostració mitjançant resultats de simulacions i experimentals.

El mètode de simplificació està basat en una transformació que transforma qualsevol sistema trifàsic a un sistema de coordenades no-ortogonal. Escollir aquest sistema de coordenades redueix la complexitat i l'esforç per determinar la ubicació d'aquells vectors espacials que directament envolten el vector de referencia. A més, totes les coordenades s'escalen a valors enters, que permet la programació de l'algorisme en sistemes de control basats en microprocessadors o FPGAs.

La principal contribució d'aquesta tesi és un nou mètode de control de corrent que intenta minimitzar els desavantatges dels mètodes indirectes existents a l'actualitat, al mateix moment que s'intenta incorporar els avantatges dels mètodes indirectes. El mètode proposat es basa en una equació matemàtica simple, la solució d'un producte escalar, per trobar el vector de tensió espacial que minimitza l'error de corrent, en el que s'anomena ?Scalar Hysteresis Control? o SHC. L'algorisme assegura un control robust del corrent

sense la necessitat de conèixer la tensió de fase, o les càrregues, tant si són desequilibrades o canviants. També presenta una dinàmica molt elevada en cas de canvies en la referència. El nou mètode mostra unes propietats excel·lents en termes de simplicitat, robustesa, dinàmica i independència de la tipologia del convertidor i, en el cas de convertidors multinivell, del nombre de nivells. Les propietats del mètode de control són verificades mitjançant simulacions i resultats experimentals en convertidors de dos, tres i fins a cinc nivells de tensió en tot el rang d'operació, fins i tot en la zona de sobremodulació.

A partir del mètode de control proposat, s'estan desenvolupant noves aplicacions i extensions, continuant també la contribució a la recerca científica.

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Acronyms

AC	Alternating Current.
ANPC	Active Neutral Point Clamped.
DA	Digital to Analog.
DC	Direct Current.
DCI	Diode Clamped Inverter.
DPC	Direct Power Control.
DSP	Digital Signal Processor.
DTC	Direct Torque Control.
ECU	Electronic Control Unit / Microcontroller.
EV	Electric Vehicle.
FCI	Flying Capacitor Inverter.
FPGA	Field Programmable Gate Array.
H-Bridge	Half-Brdige.
HDD	Hard Disk Drive.
HV	High-Voltage.
HVDC	High-Voltage Direct Current.
IEEE	Institute of Electrical and Electronics Engineers.
IGBT	Insulated Gate Bipolar Transistor.
LSB	Least Significant Bit.
MMC	Modular Multilevel Converter.
MOSFET	Metal-Oxide-Semiconductor Field-Effect Transistor.
MSB	Most Significant Bit.

mSOGI	Multi Second Order Generalized Integrator.
NPC	Neutral Point Clamped.
PI	Proportinal-Integral.
PV	Photovoltaic.
PWM	Pulse-Width Modulation.
RAM	Random Access Memory.
RMS	Root Mean Square.
SCHB	Series Connected H-Bridge.
SDHC	Switched Diamond Hysteresis Control.
SHC	Scalar Hysteresis Control.
Si	Silicon.
SiC	Silicon Carbide.
SMC	Stacked Multicell Converter.
SOGI	Second Order Generalized Integrator.
SSD	Solid State Drive.
SV	Space Vector.
SVM	Space Vector Modulation.
SVPWM	Space Vector Pulse-Width Modulation.
THD	Total Harmonic Distortion.
TNPC	T-Type Neutral Point Clamped.
VHDL	Very High Speed Integrated Circuit Hardware Description Language.
VSI	Voltage Source Inverter.

List of Symbols

a_*, b_*, c_*	Normalised Components of the a_*b_* Coordinate System.
$\tilde{a}_*$, $\tilde{b}_*$, $\tilde{c}_*$	Components of the $\tilde{a}_*\tilde{b}_*$ System.
$\underline{a}$	Complex Phasor $\underline{a} = \mathrm{e}^{\frac{2\pi}{3}}$.
α, β, γ	Clarke components.
$\underline{B}$	Tolerance Boundary.
C	Capacitance.
δ	Radius of the Tolerance Band.
Δ	Delta.
e	Inner voltage source.
f	Frequency.
I	Current.
Im()	Imaginary Part.
i^*	Current Set-Point.
j	Imaginary Unit.
k	kth output voltage vector.
κ	Level Count Dependent Normalization Factor for $\tilde{a}_*\tilde{b}_* \rightarrow a_*b_*$.
λ	Power Factor.
L	Inductance.
L1, L2, L3	Phase L1, L2, L3.
M	Midpoint.

M	Modulation Index.
n	Level Count.
N	Neutral Point.
ω	Angular Frequency.
P	Active Power.
φ	Phase Difference Angle.
π	Pi - $\pi \approx 3.14159$.
Q	Reactive Power.
Re()	Real Part.
R	Resistance.
S	AC Power.
SV, $\vec{\text{SV}}$	Space Vector.
s, m	Switching Signal of Phase s_{P} or m_{P}.
S	Switching State (e.g. S_s [1 1 0 0]).
$\vec{S}$	Switching Signal Vector.
TABS	Number of Tables (SDHC method).
t	Time.
$\boldsymbol{T}$	Transformation Matrix $\boldsymbol{T}$.
T	Transition State (e.g. T_s [0 1 0 0]).
T	Sampling Time.
U	Voltage.
$\underline{Z}$	Complex Impedance.
$\underline{u}$, $\underline{i}$, $\underline{U}$, $\underline{I}$	Complex Value.
$\overline{\underline{u}}$, $\overline{\underline{i}}$	Complex Conjugate Value.
$\frac{\mathrm{d}}{\mathrm{d}t}u$, $\frac{\mathrm{d}}{\mathrm{d}t}i$	Derivative.
u, i	Instantaneous Value.
$\hat{U}$, $\hat{I}$	Peak Value.
U, I	RMS Value.
$\vec{u}$, $\vec{i}$, $\vec{U}$, $\vec{I}$	Vector.
Z	Impedance.

List of Subscripts

$\alpha\beta\tilde{a}_*\tilde{b}_*$	Transformation Matrix from $\alpha\beta \rightarrow \tilde{a}_*\tilde{b}_*$.
α, β, γ	Clarke Components.
a_*, b_*, c_*	Normalised Components of the a_*b_* Coordinate System.
$\tilde{a}_*\tilde{b}_*(\tilde{c}_*)$	Component in $\tilde{a}_*\tilde{b}_*$ Format.
$\tilde{a}_*$, $\tilde{b}_*$, $\tilde{c}_*$	Components of the $\tilde{a}_*\tilde{b}_*$ System.
base	Base Vector.
block	Block Time.
C	Related to Capacitance.
DC	Value Related to DC Side.
dead	Dead Time.
delay	Delay Time.
Δ	Delta.
D	Distortion.
e	Error Component.
F	Related to Filter.
FPGA	FPGA related.
gh	Normalised Component of the gh Coordinate System.
h	Harmonic Component.
ik	Phase to Phase $i, k = 1, 2, 3$ where $i \neq k$.
inv	Inverter Output Voltage.

i	Phase to Neutral $i = 1, 2, 3$.
k	Output Voltage Vector Index.
L	Related to Inductance.
load	Load Voltage.
L1, L2, L3	Phase.
max	Maximum.
mean	Mean.
M	Midpoint.
min	Minimum.
N	Neutral.
nL	Related to n-Level Inverter.
opt	Optimum.
o	Related to Outer Tolerance Band.
P, p	Phase Index.
pseudo	Pseudo Reference Voltage.
q	Denotes the qth Capacitor.
R	Related to Resistance.
red	Redundant Space Vector.
ref	Reference.
res	Resonance.
rms	Root Mean Square Value.
S	Related to Sampling Frequency/Period.
s	Switching Frequency.
U, V, W	Inverter Output Phase.
$*$	Component in a_*b_* Format.
$*0$	Component in a_*b_*0 Format.
(1), (2), (0)	Positive-, Negative-, Zero- Sequence Components.

Chapter 1

Introduction

1.1 Background

One of the major challenges of the 21st century is the transition of the energy system, especially the exit from nuclear and fossil-fuel energy to renewable energy sources like wind and solar power. On the one hand an affordable and reliable electrical power supply is required and on the other hand the climate and environmental protection need to be secured.

The continually growing fraction of renewable energy within the power grids motivates the need for optimization through the complete supply chain from producers to consumers. The German energy concept specifies some key challenges to ensure a successful energy transition [1]:

- Extension of wind power (off- and onshore).
- Sustainable use and production of biologic energy.
- More extensive use of renewable energy sources for cooling and warming systems.
- Securing a cost effective development.
- Demand oriented use and production of renewable energies.
- Optimal integration of renewable energy systems.
- A qualitative and quantitative upgrade of power supply systems.
- Development and support for new and effective storage technologies.

Power electronic components like inverters and filters can be referenced to most of these challenges. The impact of those components gets bigger as the requirements in terms of efficiency and reliability as well as cost efficiency and flexibility increase.

In the field of power electronic systems, permanent enhancements and especially improvements of semiconductor device properties have taken place. IGBTs as well as thyristor based technologies have received a lot of interest in industrial and energy supply applications. Within recent years, the state of the art two-level inverters have been replaced in some special applications. Inverter topologies like three-level inverters (solar energy) or modular multilevel inverters (HVDC) have increasingly come into operation [2, 3]. Solar three-level NPC inverters enable the possibility to reduce the size of passive components and thus to reduce costs. For HVDC applications high level systems were introduced to guarantee secure operations even under high voltages.

Surprisingly, the basic control techniques have not changed significantly since the 1990s. Concepts based on Pulse-Width Modulation (PWM), Space Vector Modulation (SVM) or Direct Tourque Control (DTC) are established and basic modulation techniques for inverters in todays applications. Most of the mentioned modulation techniques generate inverter output voltages to control grid or motor currents or to act as active filters [4, 5]. As the current is controlled indirectly using a PI-controller those methods are called indirect current control techniques within this thesis. The disadvantages of indirect current control methods are well-known and subject of intense research in the last decades. Problems occur, for example, if the inverter interacts with non-linear unknown changing loads or operates near limits or under failure conditions.

Early investigations on direct current control in the 1980s and 1990s [6] suffered from the need to use analogue techniques which were not able to assert itself compared to PWM which could easily be digitized. New enhancements in digital technology allow current measurements with high sample rates and their processing in real-time. This enables new possibilities for investigations in the field of direct current controlled inverters for various applications.

Compared to indirect modulation techniques like PWM and SVM, direct current control provides primary characteristics like fast dynamics, robustness, stability, universal applicability, independence of parameters, simplicity and others. They also enable secondary characteristics desirable for science and industry (active filtering, reduction of leakage currents, ...) [7].

1.2 Motivations for Research

In the 80s and the beginning of the 90s when both the first direct as well as indirect current control methods for three-phase voltage-source inverters (VSI) were developed most of the implementations used analogue techniques. Since the state of the art microprocessor and microcontroller technology at this time was already able to perform closed-loop current control algorithms and pulse-width modulation techniques in reasonable cycle-times, PWM controlled inverters with classical current-control schemes became the state of the art in most inverter applications. However, the rapid and ongoing advancement in digital techniques, the continuous increase of its performance and the trend towards decreasing costs for digital data processing devices are motivating to reconsider direct current control methods.

Depending on the application the supplied or consumed active and reactive power of a grid connected system, the torque of a motor drive, the efficiency of a system or any other feature is of primary interest. Such high-level control variables can be assumed to be the main control goals for the individual application. The inverter, however, is only able to apply discrete output voltages directly forcing the output current to change its direction and value. Thus, the physical variable to be directly controlled by the VSI is the inverter output current. The current can therefore be considered to be the inner or the most critical control-variable.

In order to regulate the current in grid connected systems various requirements regarding the grid conditions, engineering standards, application, flexibility, robustness, complexity, cost, etc. must be met. Those requirements are leading to individual solutions for different applications, different topologies and, finally, to the development of different and application-specific controllers, each having its own complexity and individual challenges. Unknown grid impedances, unexpected grid conditions or grid-failure events are creating relevant challenges for grid-connected inverter systems. Therefore, they should be designed such that they can

- react with a very fast dynamic response to changes in the set-point value,
- accurately control the grid currents,
- operate robustly and independently from changes in grid or load parameters,
- work with different, changing or unsymmetrical loads and

- comply with engineering standards and various grid filters.

The control system should be

- universal for the use in different inverter topologies,
- adaptable to multilevel inverter systems and
- of simple description.

1.3 Objectives of Research

The aim of the thesis is to establish and prove a new and universal concept for a direct current control algorithm for multilevel inverter topologies for grid connected systems. This application is characterized by unknown grid conditions including grid-failure modes and other grid-distortions, complex inverter topologies and a high variety and complexity of existing current control algorithms for multilevel inverters. Therefore the complexity of the multilevel inverter system and its description needs to be reduced. Additionally the technical advantages of both, the low-harmonics creating multilevel inverter as well as the excellent dynamic performance and robustness of the direct current control technique, shall be combined. The aim of the project leads to a set of objectives:

- Develop and validate a new and universal direct current controller which tracks the current precisely to a reference and with low harmonic content
- Develop and validate a new and universal direct current controller providing fast dynamic response and robustness as well as being able to operate under changing load, changing grid or fault conditions.
- Reduce the complexity of the multilevel inverter system and its description.
- Establish an easy problem-solving approach enabling simple implementation in digital devices.
- Ensure easy adaptation to inverters with different level counts and topologies by a universally-usable theory
- Integrate additional control features necessary to operate a laboratory five-level neutral-point-clamped (NPC) inverter such as DC-link voltage balancing.

1.4 Contributions of Research

The main contributions of the thesis which are derived from the objectives can be highlighted as follows:

- The thesis shows a method for reducing and thus simplifying the control complexity of multilevel inverters. By means of the structure of hexagonal lattices, known from crystallography, any three-phase voltage (or current) can be transformed into a non-orthogonal, 120-degree coordinate system. Scaling the system appropriately, the discrete voltage space vectors of inverter output voltages are located only at the integer-values of that grid. Thus, the orientation in the space-vector plane gets simple, fast and ready for digital implementation on microprocessors or FPGA based control systems. This choice of coordinate system minimizes the complexity and effort to determine the location of those discrete voltage space vectors directly surrounding the required reference voltage vector. Furthermore, the integer system enables easy calculations to determine the inverter switching signals and redundant space vectors.
- The main contribution of this thesis is a new, symmetrical and low-harmonic direct current control scheme minimizing known disadvantages of existing direct current controllers. In the steady state mode of operation the new method uses a universal algorithmic approach, i.e. the solution of the mathematical equation for a scalar product, to always select the one inverter output voltage vector (out of the neighboring ones) best reducing the actual current error. This results in the designation "Scalar Hysteresis Control - SHC".
- If not operated in the steady state an advanced seeking algorithm ensures robust current control capability even in case of unknown, unsymmetrical or changing loads, in case of rapid set-point changes or in cases of unknown phase voltages. The new method therefore shows excellent properties in terms of simplicity, robustness, dynamics and independence from the inverter level count and the hardware topology.
- Simulations and real laboratory measurements on two-, three- and five-level inverters over the complete voltage operating range are proving the properties of the control method in the steady state as well as dynamic mode of operation.

1.5 Thesis Outline

The subject of research in this thesis is related to direct current controllers for grid connected multilevel inverter systems.

Chapter 1 gives a brief introduction to the subject and shortly introduces the background of this thesis. Furthermore, the motivation, the objectives and the contributions of this thesis are summarised.

Chapter 2 summarises the state of the art of existing hardware topologies. Furthermore, an overview of the necessity of the conversion of energy is given and the inverter system components are briefly explained.

Chapter 3 describes different indirect and direct current control methods and estimates the implementation effort for the control of higher level inverters.

Chapter 4 shows existing simplification methods and describes the new method that simplifies the functional structure of a multilevel inverter system and its mathematical description in the space vector plane by reducing its complexity to universal space-vector unit cells.

Chapter 5 describes the derivation and the behaviour of the new direct current control method based on a geometric solution approach, the advantages of the seeking algorithm and the working behaviour of the advanced seeking algorithm.

Chapter 6 Describes the simulation and the measurements used to verify the new method for different applications and scenarios.

Chapter 7 concludes and summarises the thesis, shows the contributions provided by this thesis and gives opportunities and proposals for further research. A list of all publications and patent applications of the author can also be found at the end of this chapter.

Chapter 2

Conversion of Electrical Energy

2.1 Introduction

The interest to use power electronic components stems from the need to convert electrical energy from a defined source into a corresponding sink. The source and sink can each be either Alternating Current (AC) or Direct Current (DC) based, depending on the application and requirements.

Frequency converters enable systems of different frequencies, voltages and number of phases to be connected to each other via an intermediary energy store. Frequency inverters using a capacitor as the energy storage are usually configured as shown in Figure 2.1. On the grid side an AC-DC converter is used to convert energy from a fixed-frequency system to a DC voltage link, which is subsequently converted to a variable-frequency system via a DC-AC / DC-DC converter. In one of the illustrated scenarios, the voltage generated by the wind turbine is converted to the intermediate circuit voltage via a AC-DC converter in order to subsequently feed the generated energy into the grid via a DC-AC inverter. This is a typical application that is used ubiquitously in today's renewable generation. Other typical applications for frequency converters are, for example [8]:

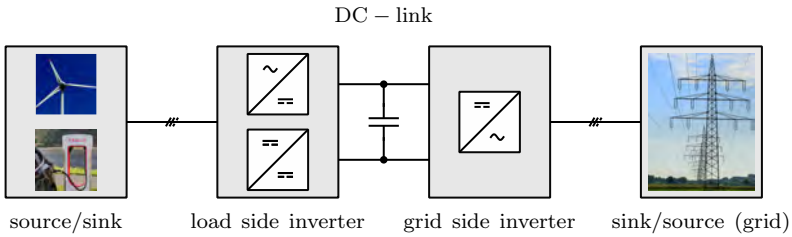


Figure 2.1: Typical example of a frequency inverter system

- Synchronous- and asynchronous machines for different applications.
- Supply of isolated networks.
- Energy transfer from one grid to another.
- Supply of AC loads.
- Feed of renewable energy systems into the grid.
- Short term energy storage or compensation of reactive power.
- Welding equipment.

The main research focus of this thesis is the conversion of electrical energy from an DC- to AC-system or from a AC to DC-system directly into or from the supply network. A so-called rectifier converts energy from an AC- to DC-system, which means that the energy flow takes place into a DC sink. Conversely, with a DC- to AC-system energy flow, the energy from a DC source is used to feed an AC sink. Since different names are used in the literature for the description of these applications, the notation inverter and converter is used in the same way to describe both systems and distinguish them only by the direction of the energy flow.

2.2 Grid Connected Voltage Source Inverters

The block diagram shown in Figure 2.2 gives a general but more detailed overview of the grid side VSI inverter with its components. The structure is basically composed of five components:

- The Voltage Source Inverter.
- The AC filter element used to absorb voltage ripples and to limit the rise of the current, which is crucial for the compliance with engineering standards.
- The DC filter element used to absorb current ripples and to decouple the AC and DC side and to store energy.
- The DC side which in this thesis is assumed to be an ideal source or sink.
- The AC side, which is either an AC source or sink (commonly, the grid).

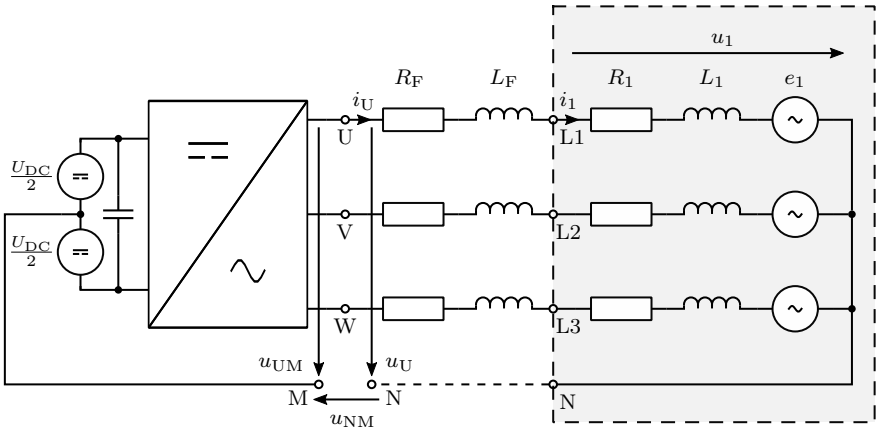


Figure 2.2: General structure of a grid connected VSI

2.2.1 AC Source/Sink

The basic equivalent circuit diagram of a standard AC source/sink is shown in Figure 2.3. This circuit example can either be considered when referring to AC-machines or when thinking about grid connected systems.

It is assumed that the AC voltage e_1 for the single-phase system and e_1, e_2 and e_3 (subsequently e_{123}) for a three-phase system have ideal sinusoidal waveforms with an arbitrary fixed amplitude and frequency. The impedance of Phase L1 is represented by L_1, which corresponds to the inductive element and R_1 the resistive element.

Single-Phase System

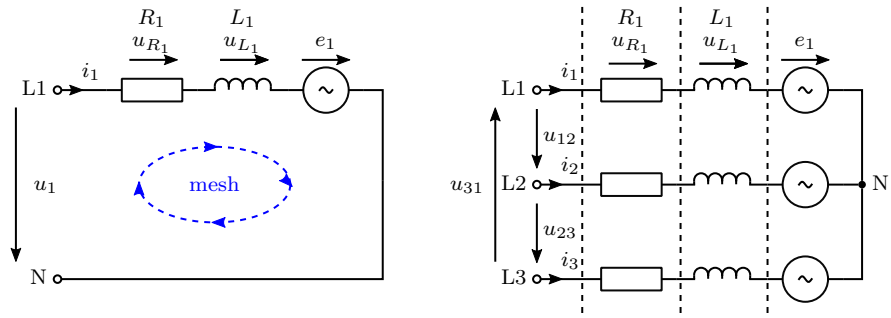
The voltage between the points L1 and N shown in Figure 2.3a can be calculated by means of a mesh equation and is defined as follows:

$$u_1 = u_{L_1} + u_{R_1} + e_1 \tag{2.1}$$

By substituting the standard component equations for u_{L_1} and u_{R_1}, this equation changes to:

$$u_1 = L_1 \frac{\mathrm{d}}{\mathrm{d}t} i_1 + R_1 i_1 + e_1. \tag{2.2}$$

Assuming a constant impedance ($L_1, R_1 = \text{const.}$) it is apparent that the voltage u_1 only depends on the current i_1 and the voltage e_1.



(a) Single-phase equivalent circuit (b) Three-phase equivalent circuit

Figure 2.3: Equivalent circuit of single-phase and three-phase AC source or sink

For the purpose of simplification, the three-phase equivalent circuit diagram from Figure 2.3b is assumed to be linear and symmetrical. Therefore all the distortions and asymmetries in such a system can directly be linked to the inverter and and its modulation algorithm used to generate the output voltages of the inverter. Since these distortions of current and voltage are of primary interest and the frequencies with which these distortions occur are substantially higher than the fundamental frequency, the ohmic component of the system can often be neglected. This simplification is possible due to the dominance of the inductive component at high frequencies. As a consequence, Equation 2.2 can be simplified to:

$$u_1 = L_1 \frac{\mathrm{d}}{\mathrm{d}t} i_1 + e_1 \tag{2.3}$$

Three-Phase System

Figure 2.3b shows the equivalent circuit diagram of a three-phase system with its components, connection points and resulting currents and voltages. The voltages between the points L1, L2, L3 and N are referred to as phase to ground voltages. Further, the voltages between the points L1, L2 and L3 are referred to as phase to phase voltages. In a symmetrical three-phase system (e.g. grid connected), the phase to ground voltages can be assumed as time-

dependent sinusoidal waveforms. These three voltages are phase shifted by 120° and they can be represented by the following equations:

$$u_1(t) = \hat{U}_1 \cdot \cos(\omega t) \tag{2.4}$$

$$u_2(t) = \hat{U}_2 \cdot \cos\left(\omega t - \frac{2\pi}{3}\right) \tag{2.5}$$

$$u_3(t) = \hat{U}_3 \cdot \cos\left(\omega t + \frac{2\pi}{3}\right) \tag{2.6}$$

where $\hat{U}_{123}$ are the amplitudes of the sinusoidal waves which is, exemplary for Phase L1, given by:

$$\hat{U}_1 = \sqrt{2} \cdot U_1 \tag{2.7}$$

In addition to the ideal sinusoidal voltages the grid may contain harmonic components which affect the ideal sinusoid disadvantageously. These harmonic components are usually modelled in the equivalent circuit diagrams by additional voltage sources with its corresponding amplitudes and frequencies. The harmonic components can be described for the source e_1 as follows:

$$e_1 = e_{10} + e_{11} + e_{12} + e_{13} + ... + e_{1h}, \text{ with } 0 < h < \infty \tag{2.8}$$

where the index h represents the hth harmonic of the voltage (or current) signal. Harmonic components occur in real grid applications. The dashed line in Figure 2.4 shows an ideal voltage with only the fundamental waveform and without harmonic components. The real voltage measured at the local grid connection point in the laboratory, which exhibits clear harmonic contents, is also shown in Figure 2.4.

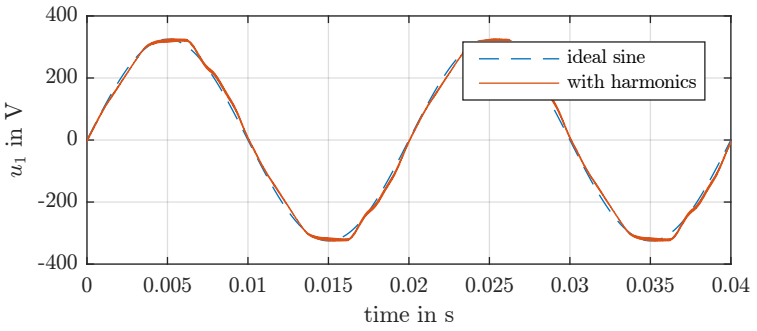


Figure 2.4: Ideal voltage (dashed) and measured voltage of phase L1

The corresponding spectrum in Figure 2.5 is normalized to the amplitude of the mains voltage. The dashed line shows the spectrum of the ideal 50 Hz sinusoidal voltage. It is apparent, that only the fundamental component at 50 Hz is present. In the measured real voltage, clear harmonic components can be seen at multiples of the fundamental frequency.

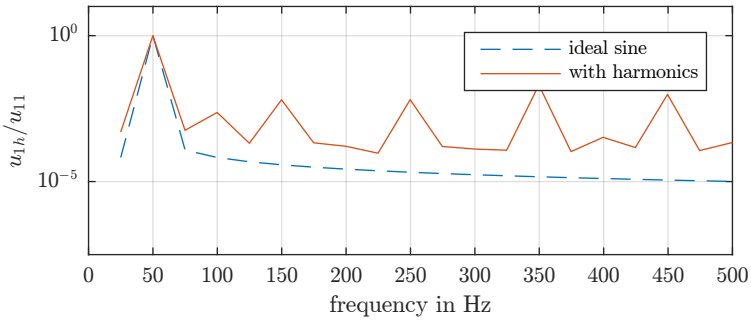


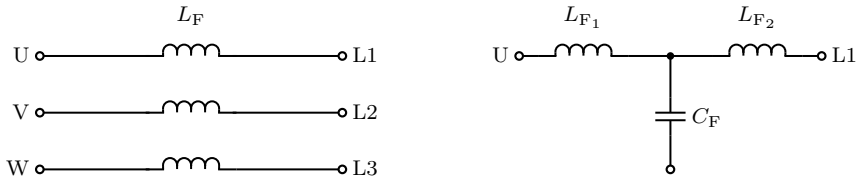
Figure 2.5: Ideal (dashed) and measured real voltage spectrum of phase L1

2.2.2 Filter Components

AC Filter

As mentioned above, filter elements are used in inverter systems to limit the effects of the switching mode of operation of the inverter and thus to limit the rise in current and the current ripple. Filter elements are needed to guarantee compliance with engineering standards and to serve as energy storage. Since standalone VSIs do not have the ability to output nearly undistorted sinusoidal waveforms which is required in some applications, filter mechanisms need to be implemented. In particular, grid connected systems have high requirements with regard to small current ripples. They require the use of additional passive filter elements in the overall circuit. In most cases third order filters (Fig. 2.6b) are nowadays used, which consist of two inductive elements and a capacitor for each phase. In order to further simplify the model of the overall system, first-order filters (Fig. 2.6a) consisting only of an inductive element will be assumed within this thesis.

When designing the filters, compliance with the requirements for the grid harmonics must be guaranteed. These requirements are specified for grid connected systems in various national and international standards [9, 10].



(a) First order L filter (b) Third order LCL filter

Figure 2.6: Typical three phase filter structures

Table 2.1 shows the distortion limits in the gird current for systems rated between 120 V and 69 kV which are applicable for most of the utility grids [9].

Table 2.1: Current harmonic limits in percentage of rated current amplitude according to IEEE-519

Maximum odd harmonic current distortion (in Percent) of the line current (I) for general distribution systems (120 V - 69 kV)					
I_{SC}/I_G	$h < 11$	$11 \leq h < 17$	$17 \leq h < 23$	$23 \leq h < 35$	$35 \leq h$
$< 20^*$	4.0	2.0	1.5	0.6	0.3
$20 < 50$	7.0	3.5	2.5	1.0	0.5
$50 < 100$	10.0	4.5	4.0	1.5	0.7
$100 < 1000$	12.0	5.5	5.0	2.0	1.0
> 1000	15.0	7.0	6.0	2.5	1.4

I_{SC}: grid short circuit current.
I_G: maximum demand grid current. (fundamental frequency component)
Even harmonics are limited to 25% of the odd harmonics.
*All power generation equipment is limited to these values of current distortion.

The individual components and the resonance frequency of a third-order filter can be defined according to the following relationship [11].

$$f_{res} = \frac{1}{2\pi} \cdot \sqrt{\frac{L_{F_1} + L_{F_2}}{L_{F_1} \cdot L_{F_2} \cdot C_F}} \tag{2.9}$$

Wherein the resonance frequency of the filter f_{res} should be at least ten times as big as the mains frequency f_e and is at most half as large as the average switching frequency f_{s} of the inverter.

$$10 f_e < f_{\mathrm{res}} < \frac{1}{2} f_{\mathrm{s}} \tag{2.10}$$

With the inclusion of various optimization criteria such as a minimum average stored energy in the filter element, minimal filter losses, minimum size, different production-technological boundary conditions, minimal costs and further boundary conditions, the optimum filter must be designed according to the grid codes. The transfer function that models the dynamic behaviour of a third order LCL filter is defined by [12]:

$$\frac{i}{u_{\mathrm{U}}} = \frac{1}{s^3 \cdot (L_{\mathrm{F}_1} \cdot L_{\mathrm{F}_2} \cdot C_F) + s \cdot (L_{\mathrm{F}_1} + L_{\mathrm{F}_2})} \tag{2.11}$$

One of the most important things for the optimal determination of the filter components is an exact knowledge about the switching frequency f_s of the inverter. In this case, PWM methods with their fixed switching frequency have an advantage over direct control methods, which in principle do not represent a unique switching frequency. For direct methods, however, it is possible to adjust an average fixed switching frequency by means of a variation of the current tolerance bands and thus enabling the design of a suitable filter.

DC Filter / DC-link Capacitor

The DC-link capacitors are mainly used for absorbing the DC current ripple and thus smoothing the DC-link voltage and for storing energy. By using these capacitors, decoupling of the DC side power from the AC side power is established. The decisive factor is the capacitance of the capacitor used. With higher capacitances, more energy can be temporarily stored in the capacitor, resulting in improved decoupling and better smoothing of the DC-link voltage. It is important to always take into account that a bigger sized capacitor will be more expensive. In most applications electrolytic capacitors are used on the DC side of the inverter due to their high energy storage capability [13].

2.2.3 DC Source/Sink

Depending on the application, different components are acting as DC sources or sinks. In the case of grid-connected applications, the following components are used, for example:

- DC sources

  Photovoltaic (PV) Panels.

  Battery systems e.g. home battery storage systems.

  DC-link capacitors connected to inverters for AC generators.

- DC sinks

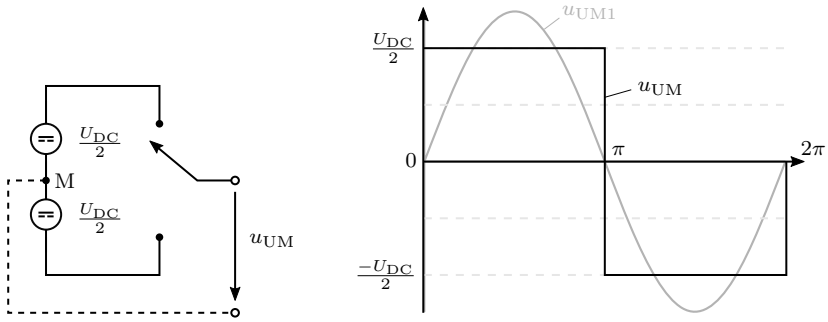
  Battery systems e.g. Electric Vehicle (EV) batteries.

  Capacitors connected to inverters driving electric AC machines.

All these components are initially assumed as ideal DC sources or sinks which are connected to the inverter and the complete system via the DC-link capacitor. In real applications, of course, additional requirements have to be included in the consideration and the equivalent circuit diagrams have to be expanded.

2.2.4 Voltage Source Inverters

In general, VSIs provide a stair-shaped output voltage which can be modelled by a series connection of several DC sources [14]. In literature, there are different topologies that provide two or more output voltages. Figure 2.7 shows the functionality of a single-phase two-level voltage source inverter via a simplified circuit diagram. The two series-connected DC voltage sources allow switching between the available output voltages. With respect to the midpoint M between the DC voltage sources, a two-level inverter can switch two output voltages: $\pm\frac{U_{DC}}{2}$. As an example, Figure 2.7b shows the rectangular output voltage for operation in square wave mode and its fundamental component. Inverters with higher level numbers can be modelled in the same way. For this purpose, additional DC voltage sources and switching positions can be added in the diagram.



(a) Simplified circuit (b) Output voltage levels

Figure 2.7: Circuit and output voltage of a single phase two-level VSI

2.2.5 VSI System Architecture

In the block diagram shown in Figure 2.2, a general overview of the main components of a two-level VSI is presented. Now that all components of a VSI system have been introduced, a simplified schematic of the complete system can be shown. This simplified circuit diagram is used to define all relevant parameters, that means all the required voltages and currents, which are necessary for further derivations in this thesis. The corresponding voltages, currents and other components used to describe the system are shown in Figure 2.8. In order to ensure clarity, only one phase is completely labelled.

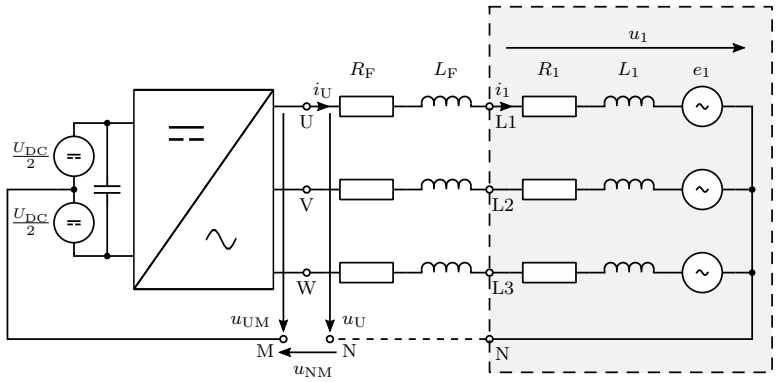
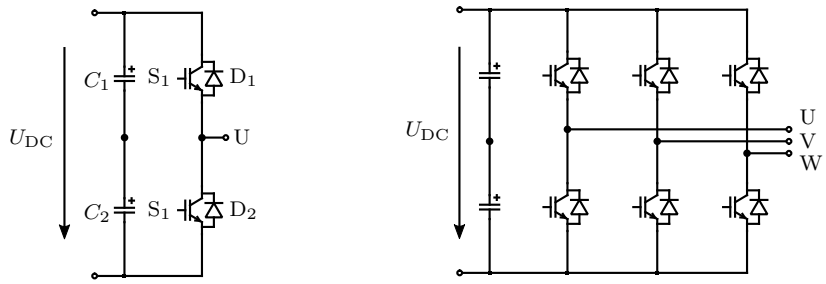


Figure 2.8: VSI system architecture and labels for all components, voltages and currents

2.3 Topologies

2.3.1 Two-level VSI

Realizing the two-level VSI from Figure 2.7a a real inverter topology needs to be built up. Figure 2.9a shows the circuit diagram of a single-phase half bridge inverter consisting of two switches with one anti-parallel diode each. In real applications different switching elements such as Silicon Carbide (SiC) and Silicon (Si) based components, like Insulated Gate Bipolar Transistors (IGBTs) or Metal-Oxide-Semiconductor Field-Effect Transistors (MOSFETs), are used [15]. The capacitor on the DC side of the half bridge is used to stabilize the voltage of the DC-link, to serve as an energy storage and to decouple the AC from the DC side.



(a) Single phase half bridge inverter (b) Three phase half bridge inverter

Figure 2.9: Two-level inverter structure

For applications connected to the grid three identical half-bridges are coupled together to a single DC-link. This leads to a total number of six switching elements and correspondingly six anti-parallel diodes as shown in Figure 2.9b. The phase tap is, as in the case of the single-phase half-bridge, between the two switches.

Since each phase of a three-phase two-level inverter can adopt two switching states, a total of eight different output combinations are possible. These eight output states lead to eight different voltage combinations, which are summarised in Table 2.2. This table shows that there are two switching levels with respect to the midpoint M of the inverter, five voltage levels as phase voltages, and four voltage levels between the neutral N and the midpoint M. The states 0 and 7 produce phase voltages of zero, which are referred to as zero voltage states.

Table 2.2: Switching states and voltages of a three-phase two-level VSI

State	S_U	S_V	S_W	u_{UM}	u_{VM}	u_{WM}	u_U	u_V	u_W	u_{NM}
0	−1	−1	−1	$-U_{DC}/2$	$-U_{DC}/2$	$-U_{DC}/2$	0	0	0	$-U_{DC}/2$
1	1	−1	−1	$U_{DC}/2$	$-U_{DC}/2$	$-U_{DC}/2$	$2U_{DC}/3$	$-U_{DC}/3$	$-U_{DC}/3$	$-U_{DC}/6$
2	1	1	−1	$U_{DC}/2$	$U_{DC}/2$	$-U_{DC}/2$	$U_{DC}/3$	$U_{DC}/3$	$-2U_{DC}/3$	$U_{DC}/6$
3	−1	1	−1	$-U_{DC}/2$	$U_{DC}/2$	$-U_{DC}/2$	$-U_{DC}/3$	$2U_{DC}/3$	$-U_{DC}/3$	$-U_{DC}/6$
4	−1	1	1	$-U_{DC}/2$	$U_{DC}/2$	$U_{DC}/2$	$-2U_{DC}/3$	$U_{DC}/3$	$U_{DC}/3$	$U_{DC}/6$
5	−1	−1	1	$-U_{DC}/2$	$-U_{DC}/2$	$U_{DC}/2$	$-U_{DC}/3$	$-U_{DC}/3$	$2U_{DC}/3$	$-U_{DC}/6$
6	1	−1	1	$U_{DC}/2$	$-U_{DC}/2$	$U_{DC}/2$	$U_{DC}/3$	$-2U_{DC}/3$	$U_{DC}/3$	$U_{DC}/6$
7	1	1	1	$U_{DC}/2$	$U_{DC}/2$	$U_{DC}/2$	0	0	0	$U_{DC}/2$

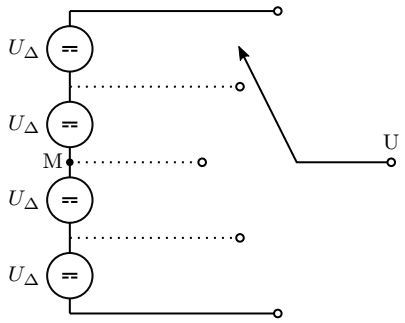
2.3.2 Multilevel Voltage Source Inverters

In 1975, a patent was published that for the first time described a topology using several inverter output voltages from multiple DC sources to provide a quasi-sinusoidal voltage to the load [16]. The focus of the scientists started decisively after the so-called Neutral Point Clamped (NPC) inverter was introduced in the year 1981 [17]. After this outstanding development, a multitude of different multilevel topologies have been developed. They all have implemented the same basic principle of taking advantage of the idea from 1975. The main advantages of using multilevel inverters as opposed to standard two-level types are exemplary presented in [18, 19] and can be summarised to:

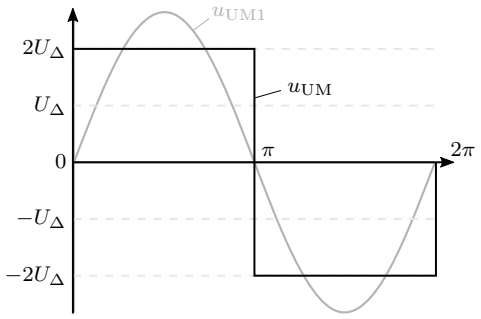
- **a more sinusoidal-shaped output waveform**: Due to more inverter output levels the generated output voltages cause lower distortions as well as a smaller $^{du}/_{dt}$ stress leading to reduced electromagnetic compatibility problems.
- **higher voltage capability**: More switches connected in series, each with similar voltage capability lead to higher voltage capability of the overall system without requiring High-Voltage (HV) switches.
- **lower switching losses:** Due to the high number of power semiconductors and due to lower voltage per semiconductor the switching losses per switch are reduced.

As mentioned before, multilevel inverters are based on the principle idea of achieving a staircase-shaped output voltage through a series connection of multiple DC sources. The number of possible output voltages is equal to

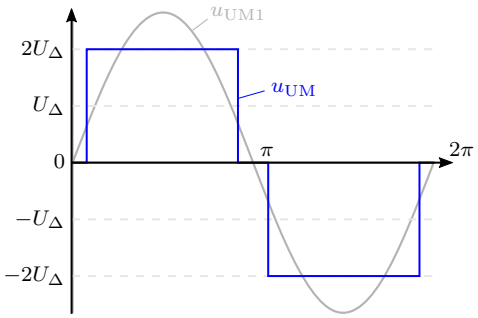
the level number of the inverter. Increasing the number of levels leads to a more sinusoidal-shaped output voltage, composed of small fractions of the DC-link voltage.



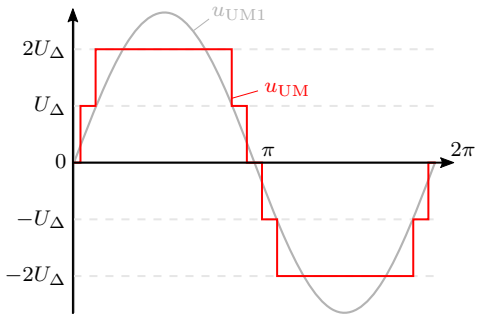
(a) Simplified circuit diagram



(b) Generated output voltage of a two-level inverter



(c) Generated output voltage of a three-level inverter



(d) Generated output voltage of a five-level inverter

Figure 2.10: Simplified circuit diagram and examples of the generated output voltages of a two-, three- and five-level inverter and their respective fundamental components

Figure 2.10 shows the simplified representation and the resulting output voltages of a two-, three- and five-level inverter. As shown in Figure 2.10b, a two-level inverter system allows two discrete output voltage levels, related to the midpoint M; a three-level system allows three (Fig. 2.10c), and a five-level system five (Fig. 2.10d) output voltage levels respectively. The

fractions of the total DC-link voltage provided at the output of the inverter with respect to its midpoint M can be calculated as follows

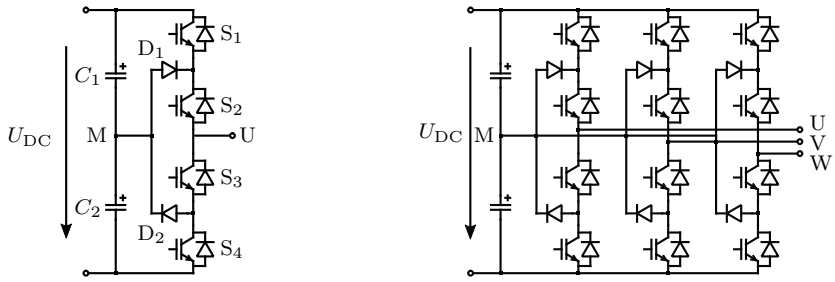
$$U_\Delta = \frac{U_{\mathrm{DC}}}{n-1}, \text{ where } \{n = 2x + 1 | x \in \mathbb{Z}\} \tag{2.12}$$

where n is the level count of the inverter, U_{DC} is the total DC-link voltage and U_Δ is the fraction of the DC source voltage. The number of possible phase output voltages U_{PM} of an n level inverter with respect to the neutral point is thus equal to n. The number of possible phase to phase voltages U_{PP} can be calculated as

$$x = 2 \cdot n - 1 \tag{2.13}$$

Diode Clamped Multilevel Inverter

As previously mentioned, the NPC inverter was one of the first multilevel converters introduced in [17]. Compared to ordinary two-level converters, the output voltage contains less harmonic content due to the higher number of output stages.



(a) Single-phase neutral point clamped inverter

(b) Three-phase neutral point clamped inverter

Figure 2.11: NPC inverter

Figure 2.11a shows one phase of a three-level NPC inverter. M is defined as the midpoint of the DC-link capacitors C_1 and C_2. The switches S_1 and S_4 are the main transistors which serve as switches for the modulation, whereas S_2 and S_3 are auxiliary transistors which connect the output potential together with the diodes D_1 and D_2 to the midpoint potential.

Table 2.3: Switching table of a 3l-NPC inverter

output voltage u_{UM}	S_1	S_2	S_3	S_4
$\frac{U_{\mathrm{DC}}}{2}$	1	1	0	0
0	0	1	1	0
$-\frac{U_{\mathrm{DC}}}{2}$	0	0	1	1

Table 2.3 represents the switching table for a three-level inverter. Unlike a two-level inverter that can only provide two output voltages $\pm\frac{U_{\mathrm{DC}}}{2}$, the NPC inverter allows three different output voltages $\pm\frac{U_{\mathrm{DC}}}{2}$ and 0 V.

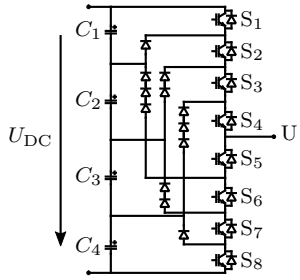


Figure 2.12: Single-phase five-level inverter

A single-phase five-level diode clamped inverter as shown in Figure 2.12 divides the total DC-link voltage into five different output voltages. These output voltages are realized by corresponding switching states as shown in Table 2.4.

Table 2.4: Switching table of a 5l-NPC inverter

output voltage u_{UM}	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
$\frac{U_{\mathrm{DC}}}{2}$	1	1	1	1	0	0	0	0
$\frac{U_{\mathrm{DC}}}{4}$	0	1	1	1	1	0	0	0
0	0	0	1	1	1	1	0	0
$-\frac{U_{\mathrm{DC}}}{4}$	0	0	0	1	1	1	1	0
$-\frac{U_{\mathrm{DC}}}{2}$	0	0	0	0	1	1	1	1

Diode clamped inverters with higher level numbers were introduced in [20]. In general, one can summarise that a three-phase n-level Diode Clamped Inverter (DCI) is composed of $3 \cdot 2 \cdot (n-1)$ switches and $n-1$ DC-link capacitors, each charged with an equal fraction of the DC-link voltage. The number of diodes needed depends on the reverse voltage blocking capability. Due to the operability and for economic reasons identical components are preferred. A series connection of diodes can be used to achieve a specific blocking capability. On the condition that one diode is selected to block the voltage U_Δ, the number of diodes can be calculated as $3 \cdot (n-1)(n-2)$ which is directly linked to the level count n of the inverter.

Flying Capacitor Multilevel Inverter

Another important and interesting topology is the so-called Flying Capacitor Inverter (FCI) which was introduced in [21]. Each phase of a three-level FCI consists of four transistors and an additional flying capacitor which is charged to $\frac{U_{\mathrm{DC}}}{2}$. Figure 2.13 shows a three-phase representation of the above-mentioned topology consisting of three identical elements for each phase that are coupled to a common DC-link. The transistors are grouped into pairs of two (S_1 and S_4, S_2 and S_3). This means, exemplary for S_1 and S_4, that if S_1 is conducting S_4 is not conducting and vice versa. Since the voltage across the non-conductive switch is $\frac{U_{\mathrm{DC}}}{2}$ and the voltage across the conductive switch is 0 V the possible output voltages of a three-level inverter related to the negative side of the DC-link are 0 V (S_1 and S_2 conducting), $\frac{U_{\mathrm{DC}}}{2}$ (S_1 and S_3 or S_2 and S_4 conducting), U_{DC} (S_3 and S_4 conducting).

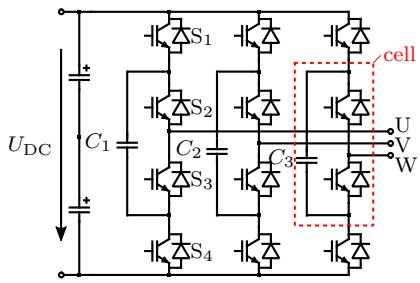


Figure 2.13: Three-phase flying capacitor inverter

As described in [21], the principle of the FCI can easily be adapted for higher level systems. To increase the number of levels, another cell consisting of two switches and a capacitor must be added to each phase of the system. In Figure 2.13, the next additional cell have to be inserted between the switches S2 and S3.

- Advantages

  Common DC source for all three phases.

  Easy adaption to higher levels.

- Disadvantages

  DC-link balancing required.

  Different blocking voltage capability of the single semiconductors.

  High monitoring effort.

Modular Multilevel Converter

The Modular Multilevel Converter (MMC), which consists of an arbitrary number of identical sub-modules, was presented in [22]. Each phase of a three-level structure of the mentioned MMC consists of $2(n-1)$ sub-modules as shown in Figure 2.14. Each sub-module is built up from two transistors and one capacitor which enables a very high modularity of the overall system. Figure 2.14 shows an example of a three-phase three-level inverter and the circuit of a sub-module

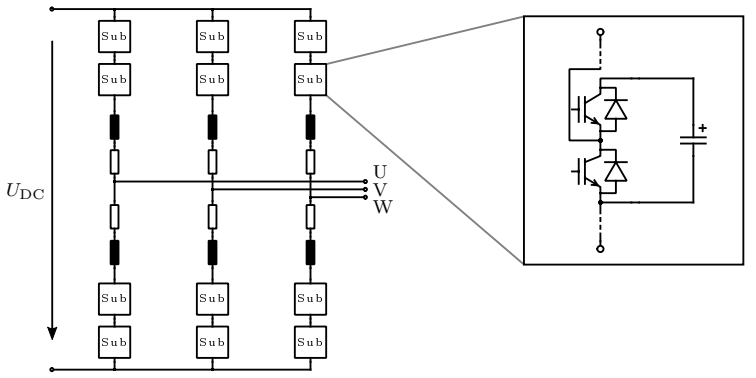


Figure 2.14: Three phase three-level MMC inverter with a sub-module circuit

- Advantages

  High modularity.

  State of the art topology for HVDC applications.

- Disadvantages

  High number of switches and components for low level numbers.

  DC-link balancing.

  High monitoring effort.

Comparison of Topologies

A comparison of the components needed for each of the topologies introduced above is shown in Table 2.5. In order to select the optimal topology for a specific application, the advantages and disadvantages must be weighted. Figure 2.15 shows the number of components and additional components

Table 2.5: Components needed per phase for different multilevel inverter topologies

	DCI	FCI	MMC
Switches	$2(n-1)$	$2(n-1)$	$4(n-1)$
DC-Link Capacitors	$n-1$	$n-1$	$2(n-1)$
Clamping Diodes/Capacitors	$(n-1)(n-2)$	$(n-2)\left(\frac{n-1}{2}\right)$	0

such as clamping diodes and capacitors that must be monitored depending on the number of levels for each of the three topologies. This can be used to select the topology that best satisfies the requirements, which are usually set by the application. In order to make a final decision, however, further parameters must be taken into account (DC-link balancing, voltage capability, quantity, power range, ...).

The solid lines show the number of all installed components required for the construction of the respective topology per phase. It is apparent that for small level counts the DCI and the FCI show advantages compared to the

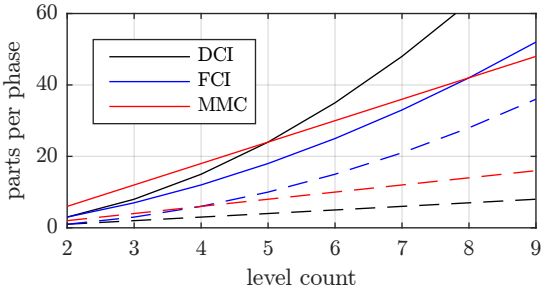


Figure 2.15: Total number of parts per phase / Number of parts to be monitored (dashed)

MMC topology. Due to the linearity of the number of components installed, the MMC topology has fewer components for higher levels ($n > 8$).

The dashed lines show the number of components which need to be monitored to operate the respective topology. In fact, this is the number of capacitors which cause a monitoring effort in order to avoid possible voltage asymmetries. Due to the modular concept each sub-module of the MMC topology requires its own capacitor, which must be monitored and controlled for potential asymmetries. The above table shows that the total number of capacitors is also higher for the FCI topology than for the DCI topology.

It becomes clear that the DCI topology has the largest number of components for level numbers greater than five, but a large amount of the components are diodes that do not need to be monitored and are not components to control. These facts give rise to the conclusions that if the level count of the inverter is less than or equal to five, the use of the DCI topology seems definitely appropriate.

In addition to the previously presented topologies, a large number of other circuits, which are partly based on one of the above, exist in the literature. Some are designed specifically for particular applications and others try to resolve drawbacks by adding additional active or passive elements. A more detailed explanation is omitted, since many publications describe and compare those topologies in detail [19, 23]. Some of the additional topologies, which are already used in real applications, are listed below.

- **T-Type Neutral Point Clamped (TNPC)**: This topology is based on a conventional two-level VSI topology but extended with an active, bidirectional switch to the DC-link midpoint [24].

- **Active Neutral Point Clamped (ANPC)**: This topology investigates the use of active neutral point clamped switches in the three-level NPC VSI to balance the losses among the semiconductors [25, 26, 27].
- **Series Connected H-Bridge (SCHB)**: This topology basically connects a series of single phase H-Bridges to generate the multilevel behaviour of the output [16, 28].
- **Stacked Multicell Converter (SMC)**: The SMC topology allows to increase the input voltage level, while decreasing the stored energy in the converter [29].

Figure 2.16 shows an overview of common multilevel topologies and their classification. The variants used for the experimental verification in this thesis are highlighted in red.

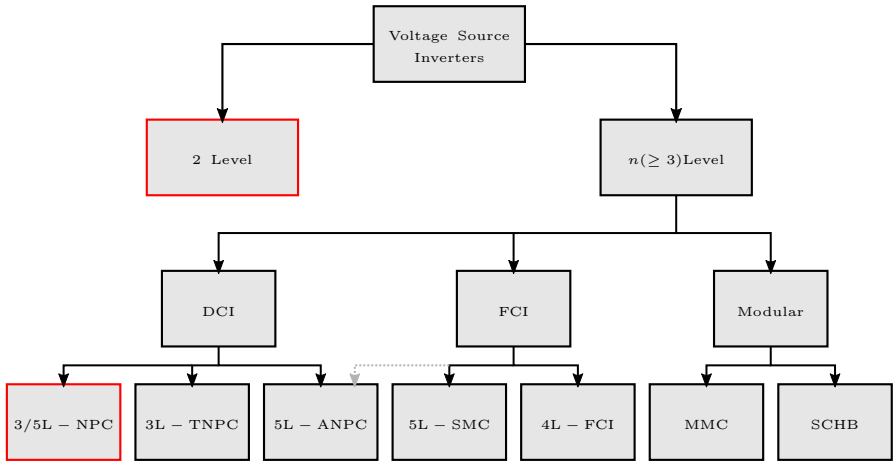


Figure 2.16: Multilevel Inverter Topologies

2.4 Diode Clamped Multilevel Inverters

As mentioned in the previous sections, DCIs have advantages compared to other topologies up to a level count of five. Moreover, the NPC inverter is already state-of-the-art in the field of grid-connected systems, due to the relatively simple realizability and the easy transferability of existing control algorithms. The advantages resulting from the use of this topology justify the additional expenses to implement the control methods.

DCIs for higher levels cause minor attention in literature since the standard implementation of this topology for a level number higher than three shows some challenges with regard to the DC-link symmetry that can not be solved with the state-of-the-art control algorithms. From [30, 31] it is known that standard modulation techniques are able to operate a five level DCI only up to a limited modulation index. Trying to use this topology above this operating point only works when considering various boundary conditions like the AC-side power factor. Nevertheless several researchers try to overcome this main disadvantage using a special circuitry or advanced modulation methods. The following shall be mentioned:

1. Operation with separate DC sources: Like in other concepts each capacitor of the DC-link could be connected to an individual DC source. This concept is only suitable for special applications as the sources are usually provided by phase-shifting transformers through diode bridge rectifiers leading to additional drawbacks [31].
2. Back-to-back operation: In back-to-back connected systems two identical DCIs are connected on the DC-side providing an AC to AC converter system. The DC-link is shared by both inverter modules. This structure allows to manipulate the common DC-link capacitors from both, the grid-connected and the load-connected, side. This additional degree of freedom enables voltage balancing using special modulation techniques [32, 33].
3. Special operating points and conditions: As mentioned above the limits of the DCI topology depend on boundary conditions like the modulation index. For some particular applications the operation within these limits is sufficient [34].

In addition to those special applications, the high dynamics and flexibility of direct control algorithms could overcome the DC-link balancing challenge in future applications. Although the investigation of the DC-link balancing is not part of this thesis, it is part of ongoing research for future considerations. Thus the main reasons for choosing the DCI topology is based on the following arguments:

- Compared to other topologies with a level number of five, a small number of components and a small number of components that need to be monitored and actively controlled are used.
- The limitation caused by the DC-link balancing problem can be overcome by various means and is subject of ongoing research.

2.5 Summary of Electrical Energy Conversion

The previous chapter gave an introduction and an overview of the need to convert electrical energy. The hardware components and topologies of a converter system necessary to perform this task were briefly presented and analysed. Since a variety of different topologies are existing in literature, from simple half-bridges to complex multilevel structures, a small selection has been introduced in more detail. On the basis of these topologies, a qualitative comparison was carried out, showing some advantages for the DCI structure for small level counts. The disadvantages of using the DCI topology were briefly discussed and existing solutions summarised. On the basis of various decision criteria, the DCI topology was selected as experimental platform for the presented thesis.

Finally, it should be mentioned that the control method presented in the following chapters is independent from the selected topology and can therefore be used with any topology. However, the experimental investigations are carried out using DCI-based inverter systems.

Chapter 3

Control of Voltage Source Inverters

Since several years, researchers discuss various modulation methods for two-level converters. A distinction is made between direct and indirect current control methods, where indirect methods are most frequently used in today's applications [8, 35]. Thinking about Pulse-Width Modulation (PWM)-based methods, the two most important concepts have been adapted for inverters with two or more levels. On the one hand, advanced carrier-based modulation methods, in which the pulses are generated by comparing one or more triangular waveforms with the reference signal, are commonly used techniques. On the other hand, the so-called Space Vector Modulation (SVM) techniques, in which the three-phase signals are transformed into an orthogonal coordinate system using the Clarke transformation, become more and more popular. Thinking about direct control methods, SVM based algorithms are the most common choice.

Since the new control technique introduced and analysed in this thesis is based on space vectors, the following chapter focuses only on space-vector-based methods but not carrier-based ones. First, a brief introduction about the differences between direct and indirect methods is given. In order to highlight the advantages and disadvantages and to explain the reasons for the relevance of further research in this area, some control methods are briefly introduced.

Figure 3.1 shows a tree diagram of different modulation methods [36, 37]. The classification of the various methods is clearly shown here, and the methods introduced in this chapter are highlighted in red.

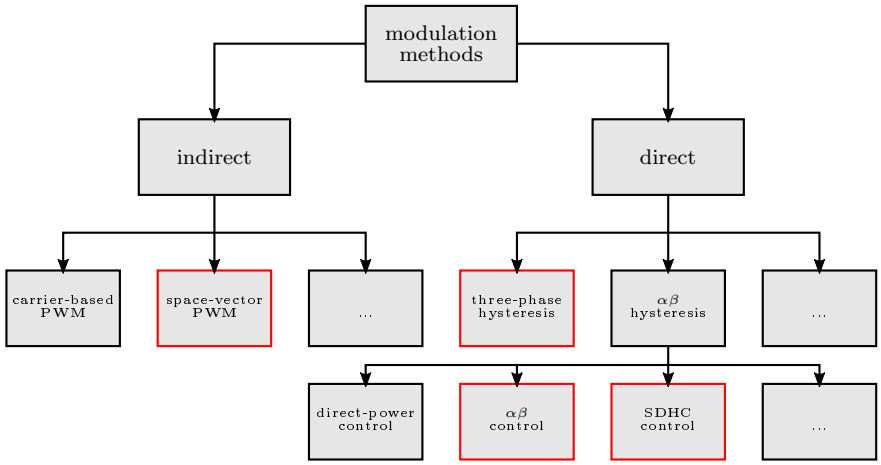


Figure 3.1: Direct and indirect current control methods

3.1 Space Vector Representation of Three-Phase Systems

Before presenting different indirect and direct SVM methods some basic concepts have to be introduced. The possibility of transforming a three-phase system into a two-dimensional orthogonal frame of reference was introduced for the first time in 1950 by Edith Clarke [38]. This transformation can be used to represent three-phase sinusoidal voltages and currents as a rotating vector in the $\alpha\beta$ coordinate system. In order to be able to better understand the relationships, the theoretical and geometric derivation of this transformation is briefly discussed below.

It is known that a set of three voltage or current vectors belonging to the phases of a three-phase system may be replaced by any number of different systems of component vectors. The Clarke transformation, also known as the $\alpha\beta$ transformation in the literature, transforms the currents and voltages of a three-phase system into an orthogonal system with three component vectors. The components of the transformation are denoted by α, β and 0 (or γ), whereby only α and β are important for standard $\alpha\beta$ controllers assuming that the neutral point is not connected. For this reason, the derivation of the third component is initially omitted.

Using complex numbers, the $\alpha\beta$ transformation of a three-phase voltage vector with the components u_i is defined as

$$\underline{u}_{\text{load}} = \frac{2}{3}(u_1 + a u_2 + a^2 u_3) \tag{3.1}$$

where $a = \mathrm{e}^{j\frac{2\pi}{3}}$ with j as the imaginary unit. By substituting a, the equation changes to:

$$\underline{u}_{\text{load}} = \frac{2}{3}(u_1 + u_2 \cdot \mathrm{e}^{j\frac{2\pi}{3}} + u_3 \cdot \mathrm{e}^{j\frac{4\pi}{3}}) \tag{3.2}$$

The mathematical relationships allow e^{jx} to be replaced by $\cos(x) + j\sin(x)$:

$$\underline{u}_{\text{load}} = \frac{2}{3}\left(u_1 + u_2 \cdot \left(-\frac{1}{2} + j\frac{\sqrt{3}}{2}\right) + u_3 \cdot \left(-\frac{1}{2} - j\frac{\sqrt{3}}{2}\right)\right) \tag{3.3}$$

In the case of ideal symmetrical sinusoidal voltages this conversion results in a space vector $\underline{u}_{\text{load}}$ of constant magnitude which rotates anticlockwise with a frequency ω in the complex plane. The $\alpha\beta$ plane corresponds to the complex plane where the α axis and β axis correspond to the real and imaginary axis, respectively. Thus, the α axis and β axis establish an orthogonal coordinate system.

The aim of the transformation is to convert a three-phase voltage into an $\alpha\beta$ voltage. Alternatively, this can be done by evaluating the following equation:

$$\begin{bmatrix} u_{\alpha\,\text{load}} \\ u_{\beta\,\text{load}} \end{bmatrix} = \boldsymbol{T}_{\alpha\beta} \cdot \begin{bmatrix} u_1 \\ u_2 \\ u_3 \end{bmatrix} \tag{3.4}$$

The transformation matrix $\boldsymbol{T}_{\alpha\beta}$ required for the conversion can be read directly from Equation 3.3. This results in the following transformation matrix:

$$\boldsymbol{T}_{\alpha\beta} = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix} \tag{3.5}$$

The factor $\frac{2}{3}$ scales the arbitrary-sized transformation so that the length of the space vector corresponds to the voltage amplitudes in the individual phases.

Assuming that $u_1+u_2+u_3=0$, the following simplification can be derived by replacing $u_3=-(u_1+u_2)$. Thus, the so-called two-phase transformation is given by

$$\begin{bmatrix} u_{\alpha\,\mathrm{load}} \\ u_{\beta\,\mathrm{load}} \end{bmatrix} = \boldsymbol{T}_{\alpha\beta} \cdot \begin{bmatrix} u_1 \\ u_2 \end{bmatrix} = \begin{bmatrix} 1 & 0 \\ \frac{1}{\sqrt{3}} & \frac{2}{\sqrt{3}} \end{bmatrix} \cdot \begin{bmatrix} u_1 \\ u_2 \end{bmatrix} \tag{3.6}$$

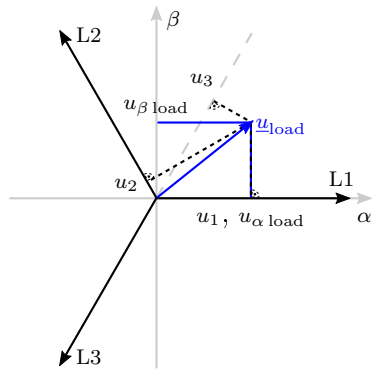


Figure 3.2: Geometrical representation of Clarke transformation

The geometric relationship of a three-phase system and the $\alpha\beta$ plane is shown in Figure 3.2. The three 120° phase-shifted voltages (or currents) can be assumed to be variable-length vectors. The space vector $\underline{u}_{\mathrm{load}}$ in $\alpha\beta$ coordinates is determined by the Clarke transformation of the three phases. The orthogonal projection from $\underline{u}_{\mathrm{load}}$ to the phase directions gives the actual amplitude of the phase voltages due to the factor $\frac{2}{3}$. In the illustrated case, the phase L1 with its voltage u_1 is the arbitrary reference phase for the Clarke transformation.

Space Vector Representation

The Clarke transformation derived above can be used to represent any three-phase voltage and current within the orthogonal coordinate system. Therefore it is possible to transfer the inverter output voltages (possible switching states of the inverter) into this coordinate system as well. From Table 2.2 we know all possible inverter output voltages. Transforming them into the $\alpha\beta$ plane leads to seven discrete voltage vectors. Using this relationship control algorithms could easily be depicted and derived. It should be noted that the space vector representation depends on the level count but not on the

hardware topology of the inverter. For this reason, control methods can be easily transferred between different topologies.

3.2 Current/Voltage Relationship

As already mentioned in the previous chapter, three-phase sinusoidal currents and voltages can be described in the complex plane. The sinusoidal current $\underline{i}(t) = i_1 + ai_2 + a^2 i_3 = \hat{I} e^{j(\omega t - \varphi)}$ has an adjustable phase shift φ against the voltage $\underline{u}_{\text{load}}(t) = \hat{U}_{\text{load}} e^{j(\omega t)}$ which depends on the respective application.

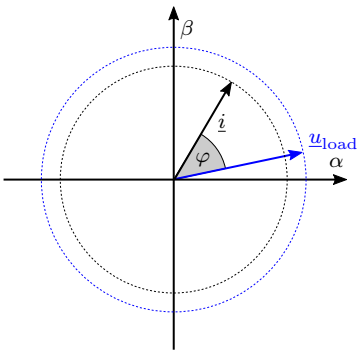


Figure 3.3: Relationship between current and voltage

Figure 3.3 shows an arbitrary vector of current and voltage in a complex diagram. A phase shift φ between the voltage and the current is apparent and can be used to determine the active and reactive power. For example, the active power is obtained when the Root Mean Square (RMS) value of the current and the voltage is multiplied by the cosine of the phase shift φ as shown in the following equation:

$$P = UI\cos(\varphi) \tag{3.7}$$

In many grid connected applications, the power factor $(\cos\varphi)$ is kept to a value close to ± 1 because this corresponds to the maximum active power. Modern inverters usually offer the possibility to set this factor individually. However, the power factor is also load-dependent. In the case of resistive loads, the current and the voltage are in phase whereas with a purely capacitive load the current leads the applied voltage by 90°, and with a purely inductive load the current lags behind the applied voltage by 90°.

3.3 System Definitions for Space Vector Based Control Algorithms

Similar to the introduction of the three-phase VSI system in Chapter 2, all currents and voltages that are required for a control algorithm must be defined. Figure 3.4 shows a simplified circuit diagram of a converter system with all relevant voltages and currents. Summarized, $\underline{U}_{\mathrm{inv}}$ is the inverter output voltage, $\underline{u}_{L_\mathrm{F}}$ is the voltage drop across the filter inductance, $\underline{u}_{\mathrm{load}}$ is the load voltage (at the grid connection point or the motor terminals), and $\underline{i}$ is the real current. As with the single-phase system, the currents and

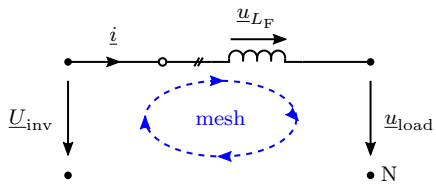


Figure 3.4: Simplified circuit of a VSI system with currents and voltages used for space vector based control algorithms

voltages can be determined by means of the mesh equation. That leads to

$$\underline{U}_{\mathrm{inv}} = \underline{u}_{L_\mathrm{F}} + \underline{u}_{\mathrm{load}} = L\frac{\mathrm{d}}{\mathrm{d}t}\underline{i} + \underline{u}_{\mathrm{load}}. \tag{3.8}$$

The current $\underline{i}$ is composed of two components, the set-point current and the error current, and is given by $\underline{i} = \underline{i}^* + \underline{i}_\mathrm{e}$. From this relationship and the component equation of the inductance, it can be seen that the voltage across the inductance can be divided into a set-point component and an error component.

$$\underline{u}_{L_\mathrm{F}} = \underline{u}^*_{L_\mathrm{F}} + \underline{u}_{L_\mathrm{F}\,\mathrm{e}} \tag{3.9}$$

The slightly adjusted equivalent circuit diagram is shown in Figure 3.5. Leading to the mesh equation for m1

$$\underline{U}_{\mathrm{inv}} = \underline{u}_{L_\mathrm{F}\,\mathrm{e}} + \underline{u} \tag{3.10}$$

and m2

$$\underline{u} = \underline{u}^*_{L_\mathrm{F}} + \underline{u}_{\mathrm{load}}. \tag{3.11}$$

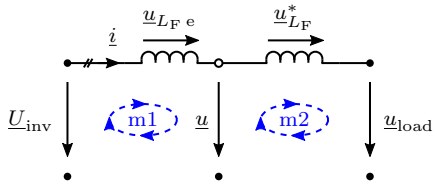


Figure 3.5: Simplified circuit of a VSI system set-point and error related inductive component

In this case, the voltage $\underline{u}$ corresponds to the averaged inverter output voltage which would have to be set to apply any set-point current $\underline{i}^*$ to the load. Thus, in space vector based methods, the voltage $\underline{u}$, which is used to select the sector, is not necessarily equal the load voltage $\underline{u}_{\mathrm{load}}$ and may be in a deviating sector. Therefore, the amplitude and phase errors depend on the amplitude and frequency of the current set-point and the inductive element. The space vector representation in Figure 3.6 shows the inverter output voltage $\underline{u}$ which results from the components $\underline{u}_{\mathrm{load}}$ and $\underline{u}^*_{L_{\mathrm{F}}}$.

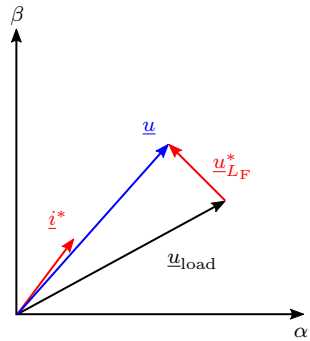


Figure 3.6: Space vector representation of averaged inverter output voltage $\underline{u}$

3.4 Indirect Current Control Techniques

Indirect current control schemes separate current error compensation and voltage modulation and exploit the advantages of open-loop modulators which are: constant switching frequency, well defined harmonic spectrum,

optimum switching pattern, and DC-link utilization [39]. Within the control loop of indirect current controllers the following disturbances can occur [7]:

- Conducting losses of semiconductors.
- Dead time of semiconductors.
- Delays and switching times which depend on the current.
- Non-linearities within the load circuit changing with current, temperature and the operating point.
- Limitations of the control element.

Despite some drawbacks compared to direct methods, the advantages of indirect methods outweighed their use in most applications today. Some of the reasons are: the simplified design of the filter components, the presence of suitable micro-controllers with PWM outputs, the presence of hardware that allows a simple digital implementation, and the many years of research that solved or circumvented many of the existing problems.

In recent decades, many methods have been developed depending on the application and they work very well. Even after the introduction of multilevel topologies, researchers have invented a lot of promising extensions. A well known representative of indirect methods is briefly introduced below.

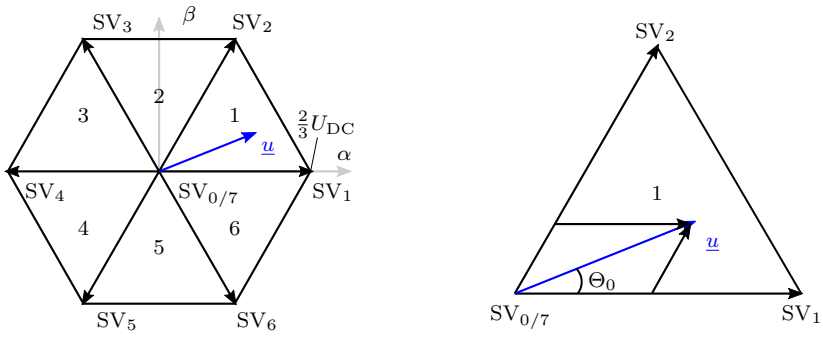
3.4.1 Space Vector Based PWM

As the name of this method suggests, this is a algorithm that uses space vectors to synthesise a certain inverter output voltage to describe the working behaviour [40].

With the help of the space vector representation of the VSI and the three-phase grid voltage, the system can be represented as shown in Figure 3.7a.

The main task of the Space Vector Pulse-Width Modulation (SVPWM) method is to generate three sinusoidal output voltages as a short term average vale of the seven space vectors which are feasible in a two-level inverter system. The required voltages are generated by suitable switching sequence of the seven space vectors for previously calculated periods. This task can be realized in practice by the execution of three steps as explained in more detailed in [35]:

1. Determination of the target space vector with a fixed sampling frequency f_S. Within each sampling period $T_S = \frac{1}{f_S}$, the set-point space-



(a) Space vector diagram with feasible output voltage vectors SV_k of two-level inverter and requried output voltage vector $\underline{u}$

(b) Geometric relationship and adjacent output voltage vectors SV_k in the first sector

Figure 3.7: Space vector diagram and sector used for SVPWM

vector is generated by the short-term average value of the switched space vectors.

2. As shown in Figure 3.7a, the seven possible output voltages of the inverter divide the space vector diagram into six sectors in the $\alpha\beta$ plane. Within each sector only the directly adjacent space vectors are used to generate the reference. This is done to achieve the smallest voltage errors and the lowest current distortions.

   As an example, the reference voltage $\underline{u}$ shown in Figure 3.7a can be generated by the following equation:

$$\underline{u} = \frac{T_{\mathrm{SV}_1}}{T_\mathrm{S}}\underline{U}_{\mathrm{SV}_1} + \frac{T_{\mathrm{SV}_2}}{T_\mathrm{S}}\underline{U}_{\mathrm{SV}_2} + \frac{T_{\mathrm{SV}_0}}{T_\mathrm{S}}\underline{U}_{\mathrm{SV}_0} + \frac{T_{\mathrm{SV}_7}}{T_\mathrm{S}}\underline{U}_{\mathrm{SV}_7} \tag{3.12}$$

   with the total sampling time

$$T_\mathrm{S} = T_{\mathrm{SV}_0} + T_{\mathrm{SV}_1} + T_{\mathrm{SV}_2} + T_{\mathrm{SV}_7} \tag{3.13}$$

   and where T_{SV_0}, T_{SV_1}, T_{SV_2} and T_{SV_7} represent the switch-on times of the space vectors $\underline{U}_{\mathrm{SV}_0}$, $\underline{U}_{\mathrm{SV}_1}$, $\underline{U}_{\mathrm{SV}_2}$ and $\underline{U}_{\mathrm{SV}_7}$. As $\underline{U}_{\mathrm{SV}_{0/7}}$ contribute zero voltage, Equation 3.12 can be simplified as follows:

$$\underline{u} = \frac{T_{\mathrm{SV}_1}}{T_\mathrm{S}}\underline{U}_{\mathrm{SV}_1} + \frac{T_{\mathrm{SV}_2}}{T_\mathrm{S}}\underline{U}_{\mathrm{SV}_2} \tag{3.14}$$

3. The third and last step involves the calculation of the switching times of the active and zero voltage vectors in a sector. By means of vector geometry (Fig. 3.7b), the switching times of the two active vectors can be calculated as

$$T_{\mathrm{SV_x}} = \frac{|\underline{u}\,(\Theta_0)|}{U_{\mathrm{DC}}}\sqrt{3}\cos\left(\Theta_0 + \delta_{\mathrm{SV}_k}\right) T_{\mathrm{S}} \tag{3.15}$$

where for the first sector:

$$\left\{\Theta_0 \in \mathbb{R} | 0 \leq \Theta_0 < \frac{\pi}{3}\right\},\ \delta_{\mathrm{SV_1}} = \frac{\pi}{6},\ \delta_{\mathrm{SV_2}} = -\frac{\pi}{2} \tag{3.16}$$

The magnitude value of the set-point vector can be calculated via $|\underline{u}\,(\Theta_0)| = \sqrt{u_\alpha^2 + u_\beta^2}$ and the angle Θ_0 in the first sector is given by $\Theta_0 = \arctan(\frac{u_\alpha}{u_\beta})$.

The time fraction of the sampling period for the zero voltage vectors can be determined by transforming Equation 3.13. This results in:

$$T_{\mathrm{SV_0}} + T_{\mathrm{SV_7}} = T_{\mathrm{s}} - T_{\mathrm{SV_1}} - T_{\mathrm{SV_2}} \tag{3.17}$$

In the literature, many different variations of this method have been presented, which bring improvements in some of the properties of the SVM method. For example, a reduction in the switching frequency can be achieved by the appropriate selection of the two zero voltage vectors.

All these extensions and the comparison with carrier-based procedures have been extensively studied by scientists in the past. The general principles and a comparison of different modulation methods based on PWM are investigated, e.g., in [41, 30]. Furthermore it is well established for two-level inverters that carrier-based and SVM methods create exactly the same phase leg switching sequences when appropriate zero sequence offsets are added to the reference waveforms for carrier modulation [42].

Higher Level Consideration

Particularly in the case of inverters with higher level counts, space vector modulation methods are commonly used. As mentioned above, this method allows a clear derivation of the problem to be solved. The time duration required to modulate the typically sinusoidal set-point voltage can then be

determined by simple geometry. Due to its simplicity and proven performance, this method has also been adapted to multilevel inverters [43, 44].

Problems occurring with increasing levels could be fixed by appropriate application-specific workarounds. An important point is the increasing complexity for which some solutions have already been presented. The majority of solutions, especially with respect to SVPWM, however, are application-oriented and can only be adapted and extended with additional efforts to other hardware topologies and level counts.

3.5 Direct Current Control Techniques

Direct current control methods attempt to directly impact the current signal without previously calculating the output voltage. One of the most important advantages of direct current control methods is its very fast dynamic performance and the fast response, even without accurate knowledge of the load parameters. Certainly, some of these methods also have disadvantages primarily with a variable and unsymmetrical switching frequency. Thus, as mentioned above, today's industrial applications are mostly based on indirect current control methods. Despite all its advantages, direct current controlled inverters are not often used for today's industrial applications. The advantages but also the not negligible disadvantages of such direct current control procedures have already been widely discussed and are presented in [4, 39, 41].

The most common advantages compared to conventional modulation techniques are:

- instantaneous control of arbitrary current waveforms and high control accuracy
- peak current protection
- overload rejection
- fast dynamics
- robustness against changes on AC or DC side

In addition, a number of basic requirements have been defined. They are not specific for current controlled systems and thus also valid for standard PWM inverters:

- ideal current tracking with no phase and no amplitude errors in a wide output frequency range

- fast response to provide high dynamic performance of the system
- limited or constant switching frequency to guarantee safe operation of power semiconductor switches
- good DC-link voltage utilization

Despite changing circumstances such as faster processors, the direct current control methods were almost not used in industrial applications yet. However, some direct methods, such as direct power control and direct torque control, have nevertheless successfully been established for some applications. In addition to the small number of already implemented methods, there are some others which also try to combine the advantages with those of multilevel inverters.

The basic principles of some direct current control methods are explained below. For purposes of illustration, the control techniques are introduced using a standard two-level system. An estimate for the implementation of higher level inverters is briefly discussed for each of the presented control methods.

3.5.1 Three-phase Hysteresis Current Controller

The three-phase hysteresis current controller is probably the simplest method of all direct current control methods [45]. Like almost all direct methods, this method works with hysteresis limits. Once one of the tolerance bands is touched, a switching operation is triggered which reduces the current error in the relevant phase of the inverter.

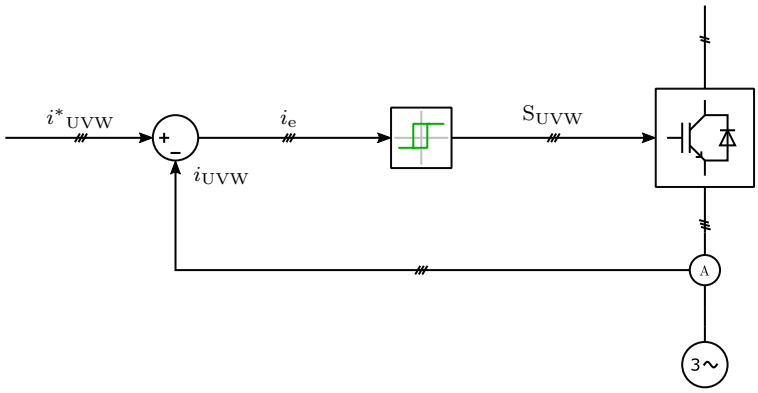


Figure 3.8: Simplified diagram of a three-phase hysteresis controller

In the case of a two-level inverter one two-stage relay is used per phase. It changes the direction of the current error as a function of the output state of the inverter. The relay can accordingly assume two states. As soon as the current error exceeds the upper or lower tolerance band, the inverter arm is switched to the positive or negative direction in order to reduce the current error. Since each phase is regulated independently from each other, the switching frequency is somewhat higher owed to the over-determination. This is caused by the use of three independent hysteresis controllers for a system with clear dependency. The simplified diagram in Figure 3.8 shows the working principle. The three phase currents i_{UVW} are measured and subtracted from the set-point currents $i^*{}_{\mathrm{UVW}}$. As explained above, the resulting error current i_{e} is fed into the relays leading to a switching state for the inverter when the tolerance band is touched or exceeded.

Figure 3.9 shows the operation using a simple example. To simplify matters, an ideal single-phase system was simulated, which controls a 10 A sinusoidal current. The red sawtooth-shaped waveform is the actual current and the three lines represent the set-point current with the upper and lower tolerance limits. Since the controller works equally for single-phase and three-phase systems, it is sufficient to consider only the single-phase case here. At time t_1, the inverter arm is in switching position 1 causing a rising current towards the upper tolerance limit. At time t_2, the upper tolerance band is reached, and a switching operation is subsequently performed. As it can be seen in Figure 3.9, the current error decreases. The next switching operation is not carried before the lower tolerance band is touched.

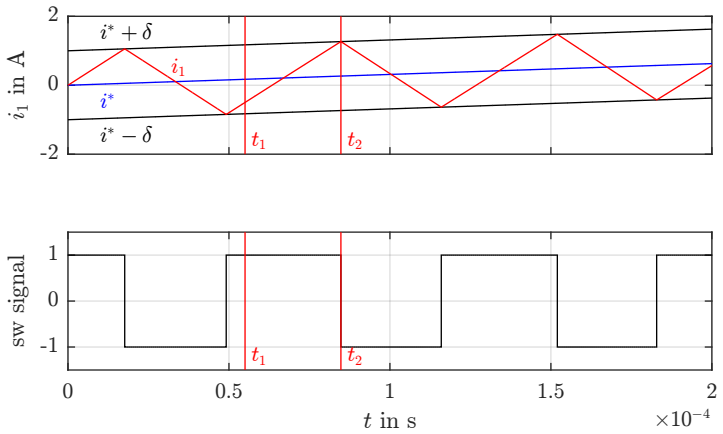


Figure 3.9: Time segment of hysteresis based controlled current with corresponding switching signal

Higher Level Consideration

Three- and single-phase hysteresis controllers are also suitable for higher levels. In this case, multi-stage relays must be used in order to cover all possible voltage steps [46, 47]. Since only two inverter output states are present in a two-level inverter, a two-stage relay is sufficient. For a five-level inverter, five output states must be mapped, and for an n level inverter, n output states. Additional hysteresis limits are used to switch between the multi-stage relays.

The current error is kept within a tolerance band of a defined size, same as in the case of the two-level three-phase hysteresis controller. This main tolerance band is, for example, set to a value $\pm\delta$ according to the requirements for the current distortion and the average switching frequency. Since five different output voltages can be selected for a five-level inverter, additional tolerance bands must be introduced to switch between those output voltages.

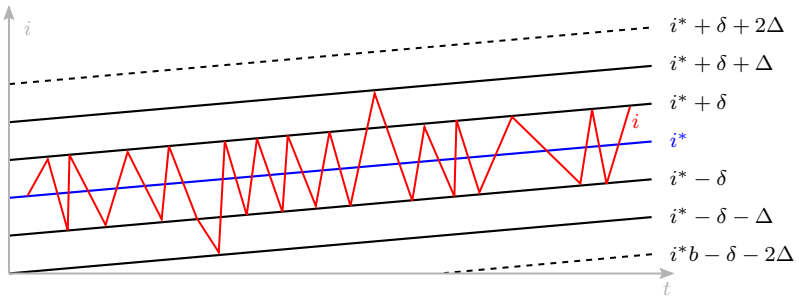


Figure 3.10: Tolerance bands of n level hysteresis controller

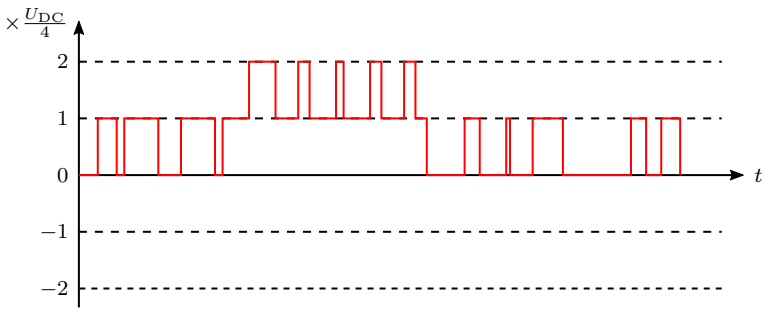


Figure 3.11: Output voltage levels of a single phase five level inverter

For example, assuming that the inverter output voltage level is initially in the range between 0 and 1, which corresponds to the output voltages 0 V and $\frac{+U_{\mathrm{DC}}}{4}$ for a five-level inverter. As soon as the current error reaches the upper tolerance band limit 0 and as soon as it reaches the lower tolerance band limit 1 is selected as the output state. If the selection of the two voltage states is not sufficient for keeping the current error within this inner tolerance band, the tolerance limit $i^* - \delta - \Delta$ will be reached (Fig. 3.10), resulting in a shift of the output voltage level into the range between 1 and 2 (corresponding output voltages: $\frac{+U_{\mathrm{DC}}}{4}$ and $\frac{+U_{\mathrm{DC}}}{2}$) as illustrated in Figure 3.11. Any exceeding of an outer tolerance band results in a change in the output voltage range. In addition to the main tolerance band and the outer tolerance band, more hysteresis limits can be introduced (as illustrated in Fig. 3.10) in order to ensure the highest possible dynamics, which, if reached, directly skips several output voltage stages.

Pros and Cons

The following advantages can be identified:

- Simple implementation for two-level inverters.
- Single phase and three phase implementation possible.

The following disadvantages are to be considered:

- The dependencies between the three phases are totally neglected which leads to considerably higher switching frequencies as necessary in a three phase symmetrical systems.
- The switching frequencies are not constant and directly depend on the modulation index.
- Increasing complexity with increasing number of levels.

3.5.2 $\alpha\beta$ Direct Current Control

This control method uses the relationship ($i_1 + i_2 + i_3 = 0$) between the three phases in a grid-connected inverter system and transforms the three-phase system into a two-phase $\alpha\beta$ representation using the Clarke transformation as previously derived. The controller uses multi-stage relays to react to current errors. As with the standard hysteresis controller, hysteresis limits, in this case separately for α and β, are used to select the different output states in

the space vector diagram. Based on switching tables, an appropriate vector is selected for each possible combination of current errors [45].

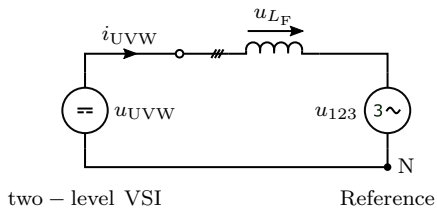


Figure 3.12: Simplified circuit of two-level inverter system

To simplify understanding, all the following methods are explained using the same basic inverter systems. This helps the comprehension and allows the small differences to be exhibited. A three-phase system is adopted which is constructed according to the previously derived simplified equivalent circuit diagram. Figure 3.12 shows the simplified representation of the three-phase structure. The system consists of a two-level inverter system with a first-order inductive filter connected to a sinusoidal reference voltage. This circuit serves as a starting point for all further considerations. The principle working behaviour of the $\alpha\beta$ control method is shown in Figure 3.13.

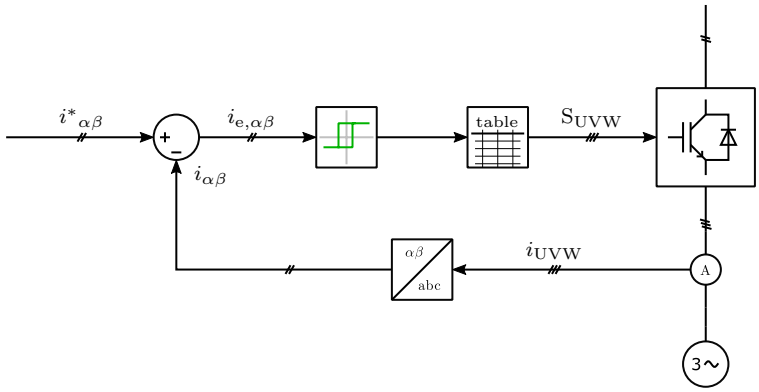


Figure 3.13: Working principle diagram of an $\alpha\beta$ controller

In order to control the current, both the α and β current are to be kept inside their tolerance bands $\pm\delta$. These two tolerance bands resulting in a

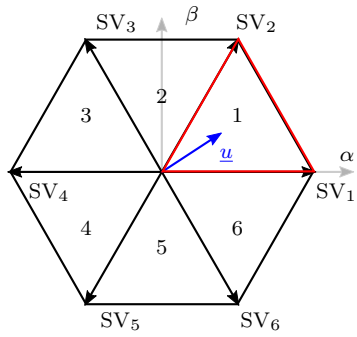


Figure 3.14: Two-level space vector diagram with $\alpha\beta$ voltage

rectangular tolerance area for the current as shown in Figure 3.15. Figure 3.14 shows the reference voltage in sector 1, which is adjoined by the space vectors SV_1, SV_2 and $SV_{0/7}$. Depending on the violated border of the tolerance band, a vector from the switching table belonging to sector 1 is selected. The switching table for sector 1 is shown in Table 3.1.

Table 3.1: Switching table of sector 1 for $\alpha\beta$-control

$\downarrow \beta$ / $\alpha \rightarrow$	$+$	$-$
$-$	SV_2	SV_2
$+$	$SV_{0/7}$	SV_1

Figure 3.15 shows the trajectory of the current error in the $\alpha\beta$ plane as a moving arrow at any time due to given switching conditions. Due to the direction of the current error it can be assumed that SV_1 was switched, which leads to the state $+\delta_\alpha$ and $-\delta_\beta$ in Table 3.1. As soon as the current error (arrow tip) touches the hysteresis limit, the state of the β boundary changes from $+\delta_\beta$ to $-\delta_\beta$ causing a change in the space vector to SV_2. Due to the sector geometry and the geometry of the tolerance band, there are only three different voltage vectors for four different states (Tab. 3.1). Note that the space vectors SV_0 and SV_7 are counted as one, since they produce the same inverter output voltage and thus have the same impact on the current. For this reason, the described system is under-determined, which can sometimes cause the current error to increase further after a switching operation. In the illustrated case, after the switching operation, the current error increases

in α and β direction until the positive α boundary is touched. After that a new vector is chosen which reduces the current error.

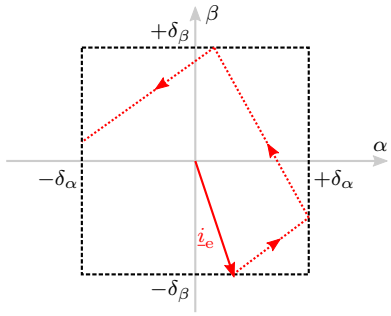


Figure 3.15: Current error and tolerance area

The principle described for one single sector can be extended to all six sectors in the space vector diagram. The combination of the switching tables can be simplified by the use of multi-stage relays for the α and β directions. Table 3.2 shows the combined switching table with all 12 possible output combinations. It becomes clear that for the α direction a four-stage relay and for the β direction a three-stage relay must be used to select the correct switching combination in the switching table.

Table 3.2: Combined switching table for $\alpha\beta$-control

$\downarrow \beta$ / $\alpha \rightarrow$	$++$	$+$	$-$	$--$
$-$	SV_3	SV_3	SV_2	SV_2
0	SV_4	$SV_{0/7}$	$SV_{0/7}$	SV_1
$+$	SV_5	SV_5	SV_6	SV_6

Figure 3.16 shows a period of an $\alpha\beta$ controlled inverter system. The upper part shows the $\alpha\beta$ currents with the corresponding tolerance band boundaries. It can clearly be seen that the current can be held within the tolerance band for most of the time. At the time t_1, the tolerance band is violated (more detailed in Fig. 3.17a), which is due to the fact that at this specific point in time the controller can not find a matching vector which can reduce the error. The space vectors are shown in the lower part of the picture. To simplify matters, only SV_0 was selected for the zero voltage vector.

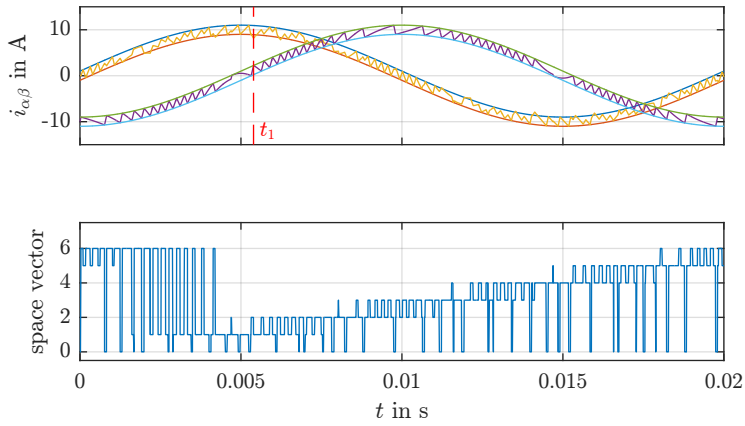
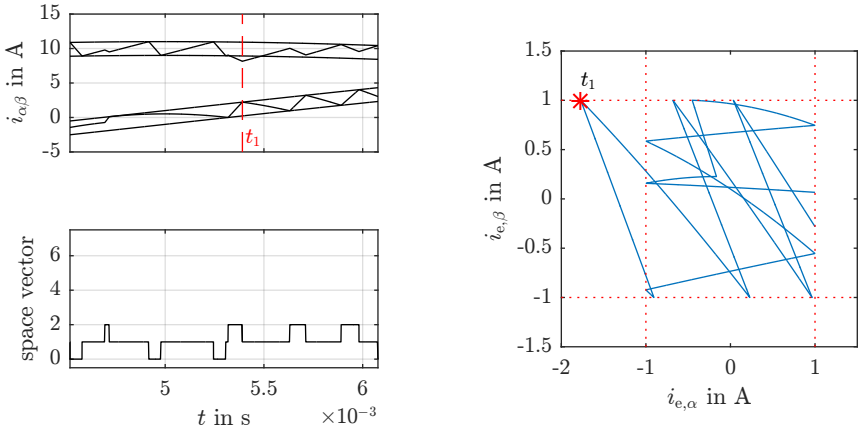


Figure 3.16: $\alpha\beta$-currents and corresponding space vectors

A time interval around the point t_1 allows a closer look and is shown in Figure 3.17. At the time t_1, a violation of the lower tolerance band in α direction can be seen in the upper part of Figure 3.17a. A look on the resulting xy graph of the current error for this time interval (Fig. 3.17b), this limit violation is shown even more clearly. This violation is caused by the under-determined concept of the standard $\alpha\beta$ control method. This means that the current controller can not find a space vector that directs the current error back into the rectangular error area.



(a) Time section for time t_1

(b) xy-plot of $\alpha\beta$-current error

Figure 3.17: Tolerance band violation during $\alpha\beta$ hysteresis control

Higher level consideration

A variety of extensions are available for this type of control method, which apply the concept to inverter systems with higher levels. All these methods are based on switching tables for the different triangular sectors in the $\alpha\beta$ plane. If the number of levels increases, the number of output states increases and thus the number of output combinations increases.

In case of a two-level system, twelve possible output combinations are used in the switching table, which results from a four-stage relay in the α axis and a three-stage relay in the β axis. Going to higher levels, the total number of switching combinations as well as the complexity of generating the switching tables and thus the complexity of the entire controller increases.

Particularly for special implementations of this type of direct current controllers such as the Direct Torque Control (DTC) or Direct Power Control (DPC), there are a large number of scientific studies focusing on specific applications and the reduction of the complexity at higher levels.

Pros and Cons

The following advantages can be identified:

- Simple implementation for two-level inverters.
- The relation ($i_1 + i_2 + i_3 = 0$) of the three phases is taken into account, resulting in a lower switching frequency compared to the three-phase hysteresis controller.
- High dynamics and robustness.

The following disadvantages need to be considered:

- Switching frequency between the three phases varies up to 30%.
- The switching frequencies are not constant and directly depend on the modulation index.
- Increasing complexity with increasing number of levels.

3.5.3 Switched Diamond Hysteresis Direct Current Control

The so-called Switched Diamond Hysteresis Controller (SDHC) adopts and extends the function of a standard $\alpha\beta$ controller [7, 48]. As with the previous control method, a hysteresis band is introduced for the α and β direction. As soon as the current error reaches a hysteresis limit, a switching operation is

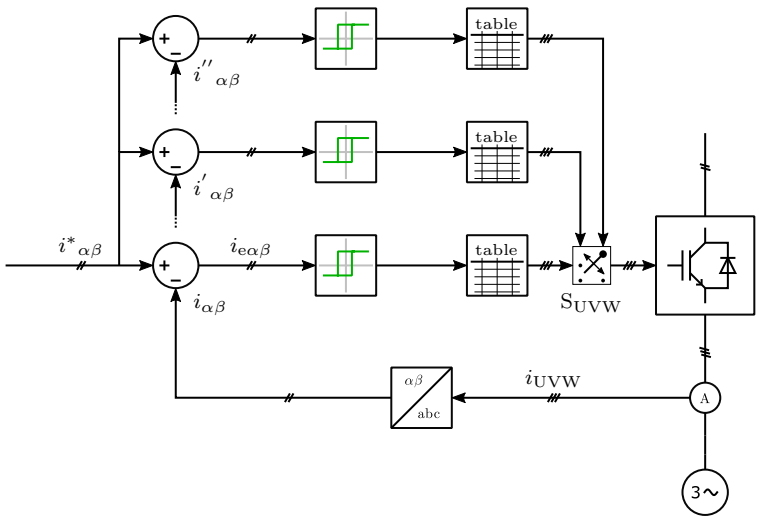


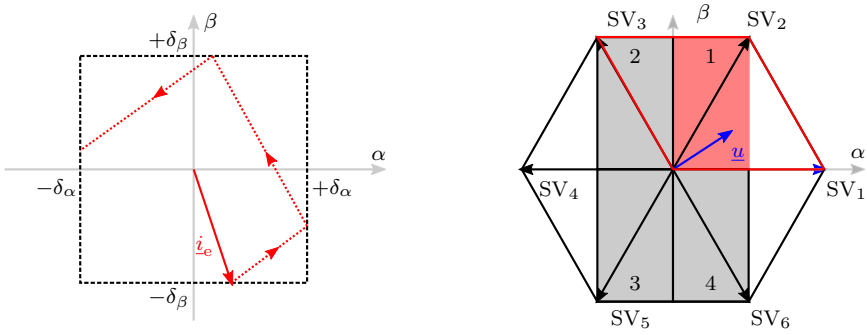
Figure 3.18: Principle diagram of a SDHC controller

executed which is intended to reduce the current error. The structure (Fig. 3.18) and the differences to the standard $\alpha\beta$ controller are briefly explained below.

The simplified three-phase structure, as shown in Figure 3.12, is also used as a basis for the derivation of this method. The hysteresis limits for α and β are set to $\pm\delta$. The rectangular tolerance area for the current error is therefore identical to the previous one and is shown in Figure 3.19a. The space vector diagram, the reference voltage and the sector geometry are illustrated in Figure 3.19b. It can be seen that this method uses a rectangular-shaped sector to control the current. In contrast to the standard method, four vectors arranged in a diamond shape are used for control, instead of using only three adjacent vectors. As a result of this sector geometry, a modified switching table for the selection of the space vector is obtained as shown in Table 3.3.

Table 3.3: Switching table of sector 1 for SDHC-control

$\downarrow \beta \ / \ \alpha \rightarrow$	$+$	$-$
$-$	SV3	SV2
$+$	SV0/7	SV1



(a) Current error

(b) Two-level space vector diagram with SDHC sectors

Figure 3.19: Current error and two-level SDHC space vector diagram

The functionality of the $\alpha\beta$ controller has already been explained. Depending on the state of the relays, a suitable space vector from a switching table is selected and used to reduce the current error. Unlike the standard $\alpha\beta$ controller, the SDHC controller has four space vectors in one sector to react to hysteresis faults. Due to the geometry, it is thereby always possible to select a vector which reduces the current error at any time. Figure 3.19b shows the four sectors in which the SDHC method works. Outside this area the functionality is not guaranteed. The question now is how the triangular edge regions can be included in the control in order to be able to use the full voltage operating range of the inverter. To circumvent this problem, the SDHC method uses the fact that the phase U is arbitrarily used as a reference for the Clarke transformation. Which in turn allows the two other phases to be also used as a reference for the transformation. This corresponds to a rotation of 120°. Recognizing that and rotating the coordinate system every 60°, all areas in the space vector diagram can be covered as shown in Figure 3.20. This results in a total of 12 sectors and thus also 12 different switching tables.

Setting up all the switching tables always works analogously, with the difference that the diamond-shaped arrangement in Figure 3.19b for the sectors 1 and 3 is left-aligned and right-aligned for the sectors 2 and 4. The switching tables for the rotated coordinate systems are issued analogously.

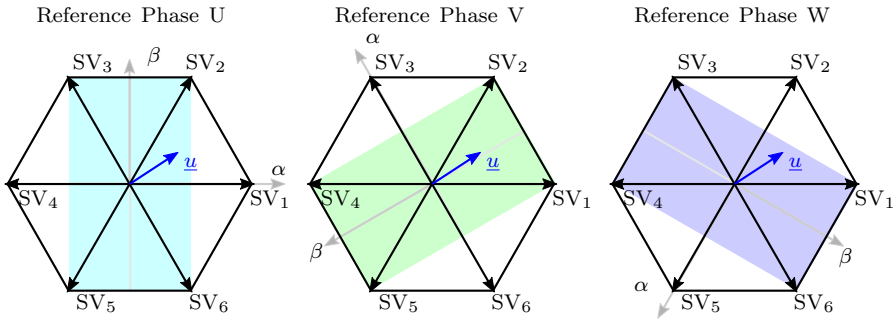


Figure 3.20: Two-level space vector diagram with rotated sectors

As already mentioned, the reference for the coordinate system is changed every 60°. Table 3.4 shows the valid reference phase for the Clarke transformation for each possible angular range of the reference voltage $\underline{u}$.

Table 3.4: Angular sectors of the reference voltage with corresponding reference phase for Clarke transformation

Angular range	**Reference phase**
0° - 60°	phase V
60° - 120°	phase U
120° - 180°	phase W
180° - 240°	phase V
240° - 300°	phase U
300° - 360°	phase W

Figure 3.21 shows one period of a SDHC controlled inverter system. The upper part shows the $\alpha\beta$ error current with the corresponding inner tolerance band boundaries. It is apparent that the current is kept within the tolerance band at all times. Since all system parameters were equated with those in the previously explained $\alpha\beta$ procedure where a border violation occurred at t_1, the location was also marked here. It can be seen that no limit violation occurs within the period when using the SDHC method. Even when looking more closely at the corresponding time segment around t_1 in Figure 3.22, it is apparent that no border violation occurs.

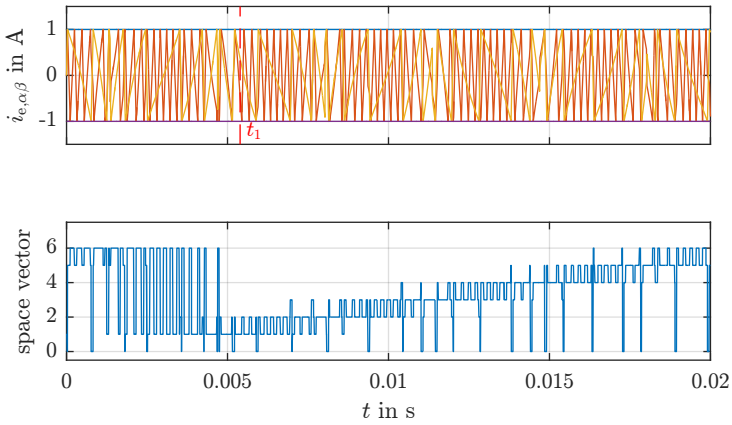
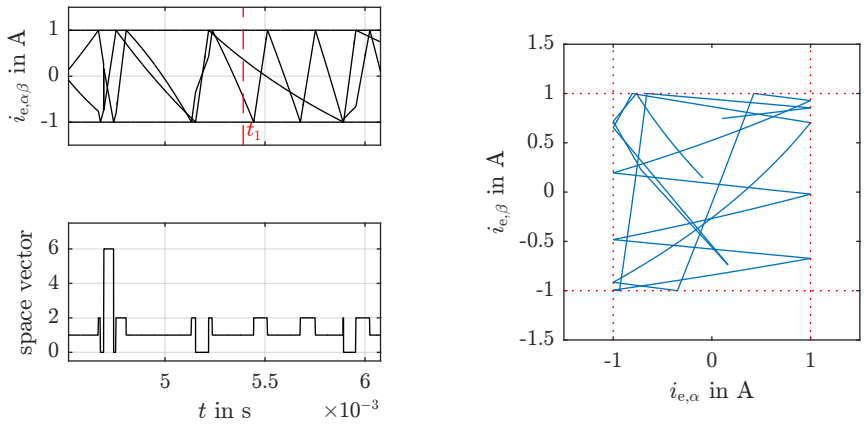


Figure 3.21: $\alpha\beta$-currents and corresponding space vectors



(a) Time section for time t_1

(b) xy-plot of $\alpha\beta$-current error

Figure 3.22: Time interval where tolerance band violation during $\alpha\beta$ hysteresis control occurred

Higher Level Consideration

The SDHC method shows some advantages compared to other direct current control methods. Adaptations to higher level numbers promise the possibility to combine the advantages of the method with the advantages of multilevel converters. An implementation on a three-level NPC inverter has already

been discussed and presented in [49]. Experimental results have confirmed the functionality, but also shown that the complexity increases significantly with rising level numbers.

Figure 3.23 shows the space vector diagram and the sector size for a two- and three-level inverter for the same application. It is apparent that the sectors become smaller and the number of sectors increases significantly. This fact has the consequence that more switching tables with a higher number of switching vectors have to be set up. The number of possible switching vectors $k_{\max}$ depends on the number of levels and is given by the following equation:

$$k_{\max} = n^3 \tag{3.18}$$

The number of switching tables to be set up can also be determined from the level number n. It turns out that 60 switching tables are necessary for a three-level inverter and 216 switching tables for a five-level inverter system. In general, the SDHC method requires

$$\text{TABS} = 3 \cdot 4 \cdot ((n-1)^2 + \frac{(n-1)}{2}) \tag{3.19}$$

switching tables. Depending on the selected hardware topology of the inverter, an additional DC-link balancing algorithm is required which must be taken into account when setting up the switching tables.

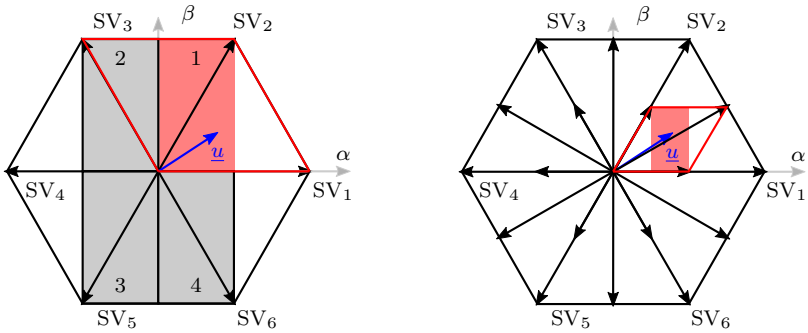


Figure 3.23: Two-level and three-level space vector diagram with reference voltage and corresponding rectangular sector

Pros and Cons

The following advantages can be identified:

- Excellent dynamic behaviour.
- Due to the rotation of the coordinate systems, the average switching frequency is the same in the three phases.
- At any time, an output space vector is set which can reduce the current error.

However, the following disadvantages should be considered:

- More switching tables and therefore higher error-proneness during design and implementation phase as well as more complex verification.
- The switching frequencies are not constant and directly depend on the modulation index.
- Increasing complexity with increasing number of levels.

3.5.4 Predictive Current Control

Predictive current control methods calculate the future behaviour of the current and thus also the current error. Using the exact knowledge of the load parameters and the instantaneous measured values, an optimal next output state of the inverter can be predicted. The effect of the individual space vectors can be calculated with individual complexity and the solution partly depends on the aim of the control. Predictive methods can, for example, be used to reduce the switching frequency of the converter or to regulate the switching frequency via a variation of the hysteresis band.

For this kind of method various procedures and extensions trying to eliminate disadvantages and to use existing advantages in a better way are propsed in literature. The quality of the control heavily depends on the quality of the load parameters which is the main limiting factor. A classification of several methods is presented in [50].

One of the first basic methods was presented in [51] and will be briefly explained in the following. Using the current set-point $\underline{i}^*$ and the actual current $\underline{i}$ at a time t_0, the future evolution of the trajectories can be determined. Starting from the standard equivalent circuit of a two-level inverter system the following steps need to be carried out.

The equation to calculate the complex values of all six non-zero output voltage vectors from the space vector diagram is given by:

$$\underline{U}_{\mathrm{inv}(k)} = \frac{2}{3} U_{\mathrm{DC}} \cdot e^{\frac{j \cdot k \cdot \pi}{3}} \tag{3.20}$$

where $\{k \in \mathbb{Z} | 1 \leq k \leq 6\}$. The zero voltage vectors for $k = 0/7$ are therefore:

$$\underline{U}_{\mathrm{inv}(0/7)} = 0 \text{ V} \tag{3.21}$$

The waveform and the behaviour of the desired set current is normally determined by the application and is known for the actual and future point of view or needs to be predicted. Thus, this set current can be described by the following equation:

$$\underline{i}^*(t) = \underline{i}^*(t_0) + \frac{\mathrm{d}}{\mathrm{d}t} \underline{i}^* |_{t=t_0} \cdot (t - t_0) \tag{3.22}$$

The actual current at the time $t = t_0$ is measured, while the future course, must be estimated via the system equations using the first-order approximation.

$$\underline{i}(t) = \underline{i}(t_0) + \frac{\mathrm{d}}{\mathrm{d}t} \underline{i} |_{t=t_0} \cdot (t - t_0) \tag{3.23}$$

with

$$\frac{\mathrm{d}}{\mathrm{d}t} \underline{i}(k) |_{t=t_0} = \frac{\underline{U}_{\mathrm{inv}(k)} - \underline{u}_{\mathrm{load}}(t_0)}{L_{\mathrm{F}}} \tag{3.24}$$

When the hysteresis band is exceeded, the current error triggers an action which is used to determine a new output state of the inverter. Each of the possible output states has a different effect on the actual current, which is illustrated in Figure 3.24a. The current error is determined by the following equation:

$$\underline{i}_{\mathrm{e}}(t, k) = \underline{i}^*(t) - \underline{i}(t, k) \approx \underline{i}_{\mathrm{e}}(t_0) + \frac{\mathrm{d}}{\mathrm{d}t} \underline{i}_{\mathrm{e}}(t_0, k) \cdot (t - t_0) \tag{3.25}$$

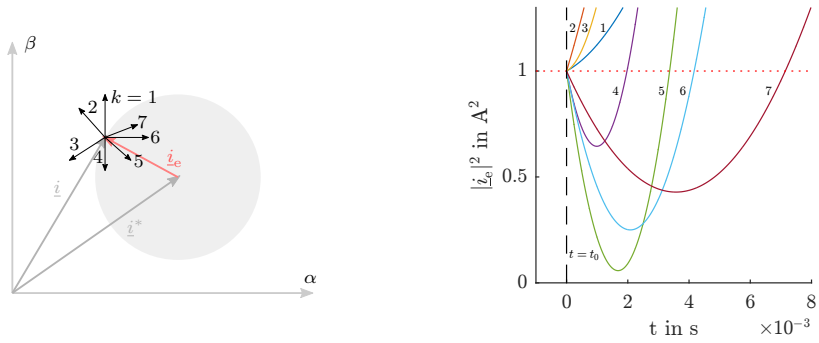
The square of the magnitude is used to determine a function which calculates the trajectories of the current error for all values of k until the hysteresis band is exceeded the next time. More specifically, this means which output state of the inverter has the desired effect on the current error. Figure 3.24b shows the trajectories for all values of k starting from time $t = t_0$. It can be seen that the inverter output voltages generated by the space vectors $1, 2, 3$ would further increase the current error. All other vectors reduce the current error

and cause the next limit violation at a later time. As apparent in Figure 3.24b space vector 7 would be the one keeping the current error as long as possible inside the tolerance area. The square of the magnitude of the current error is therefore given by:

$$|\underline{i}_e|^2(t,k) = |\underline{i}_e|^2(t_0) + a_1(t_0,k)\cdot(t-t_0) + a_2(t_0,k)\cdot(t-t_0)^2 \tag{3.26}$$

where a_1 and a_2 can be derived by simply squaring Equation 3.25. In conclusion, the time to the next boundary violation can be determined for all space vectors by equating the square of the magnitude of the current error at the actual and future point in time. After solving the equation, one obtains:

$$\Delta t(k) = -\frac{a_1(t_0,k)}{a_2(t_0,k)} \tag{3.27}$$



(a) Current vectors and predicted trajectories at $t = t_0$

(b) Error functions for all space vectors

Figure 3.24: Predictive current control

Higher level consideration

In literature there exist extensions of predictive control methods that consider inverter systems with higher levels [52]. Because of additional calculations and control parameters such as the DC-link balancing within the NPC topology, the algorithms become more complicated and require more computational effort. For this purpose, optimizing functions are often implemented

which, depending on the error, make the best choice of the next space vector regarding to the desired application and requirements.

Pros and Cons

The following advantages can be identified:

- Optimal (e.g. desired or minimal switching frequency) selection of the next voltage space vector.
- Improved stationary behaviour.

However, the following disadvantages must be considered:

- Accurate knowledge of the load parameters is essential.
- Under certain circumstances, high computing efforts.
- Increasing complexity and even higher computing costs with increasing number of levels.

3.6 Comparison of Control Techniques

In addition to the direct and indirect current control methods described here, a wide range of controllers have been investigated which all have individual advantages but also disadvantages. It is very difficult to implement a controller that meets all requirements in terms of complexity, dynamic behaviour, variation of switching frequency, stability and applicability to multilevel systems. Apart from the inaccuracy in the assessment of the conformity to the stated requirements, many additional parameters must be included in the selection of a suitable control method. For grid-connected systems, for example, extensions to the $\alpha\beta$ controller are suitable, such as the so-called DPC method, which allows direct control of the active and reactive power. These types of controllers are considered to be robust, since changes in the load parameters do not influence the stability. In case of the use of multilevel converters, the complexity of such methods can rise due to the variety of different switching tables and additional boundary conditions.

Table 3.5 attempts to give a qualitative assessment of different control methods with regard to complexity, dynamic behaviour, switching frequency, stability and adaptability to multilevel inverters [53, 54]. As a new $\alpha\beta$ controller for grid connected systems is presented in this thesis, the standard

$\alpha\beta$ hysteresis control method was chosen as the simplest representation of an $\alpha\beta$ based algorithm.

Table 3.5: Comparison of direct and indirect current controllers

	PWM	Predictive Control	$\alpha\beta$ Control
Complexity	medium	complex	simple
Dynamics	slow	fast	very fast
Switching frequency	constant	constant	spread
Stability	achievable	achievable	robust
Multilevel adaptability	complex	complex	complex

3.7 Summary of Control Techniques

This chapter provided a brief overview of the state of the art for indirect, but mainly for direct control methods. Since a space vector based method will be introduced in this thesis, the space vector representation of an inverter system was introduced in general.

In addition to an indirect SVM method, the so-called SVPWM, different direct methods were presented for comparability reasons and explained by means of examples. The advantages and disadvantages are presented for an ideal inverter and an assessment of the adaptability to multilevel inverters is given in a qualitative manner.

On the basis of various application-dependent advantages and disadvantages, it can be concluded that further research is necessary especially on adaptability to higher levels and the simplicity of the controller implementation.

Chapter 4

Simplified Space Vector Modulation Techniques

4.1 Problem Statement

In industrial applications where inverter systems are used, the expense factor is decisive for the integration of new components. Since passive components tend to become more expensive and active components are becoming more and more favourable, there is a tendency to replace passive by active elements. Examples which may be mentioned here are active filters or multilevel converters.

When using multilevel converters which are controlled by SVM methods, it has already been mentioned that the complexity increases because of the multiplicity of sectors with increasing number of levels. This fact and the potential need for real-time computing units such as Field Programmable Gate Arrays (FPGAs) justify more research to reduce the complexity of describing SVM-based systems.

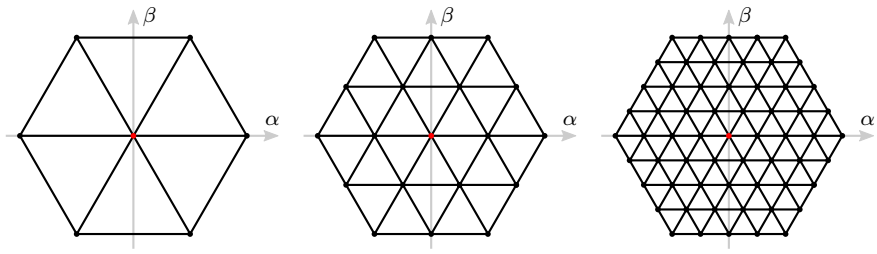


Figure 4.1: Space vector diagram for a two-, three- and five-level inverter

Figure 4.1 shows the space vector diagrams of a two-, three-, and five-level inverter. It can be seen that the number of triangular sectors increases with the number of levels. Each vertex of such a sector corresponds to an output voltage of the inverter and can, in exceptional cases, be generated by different output states. Considering inverter level counts $n \to \infty$, one would get an infinite number of output voltages, redundant switching vectors and gate signals. For these reasons, solutions are suggested in the literature by means of appropriate descriptions which are intended to reduce the complexity [55, 56, 57].

The following chapter shows the derivation of a new three-phase linear transformation matrix which can be used to determine all parameters necessary for a control method in a space vector diagram. The transformation allows the simple description and determination of the output states of the inverter, the redundant vectors and the gate signals, which are used by SVM-based modulation methods for controlling two-level and multilevel inverters. Further attention was paid to the fact that the transformation has been developed and optimized in a way that it can be used for fast computing units based on fixed-point systems such as FPGAs.

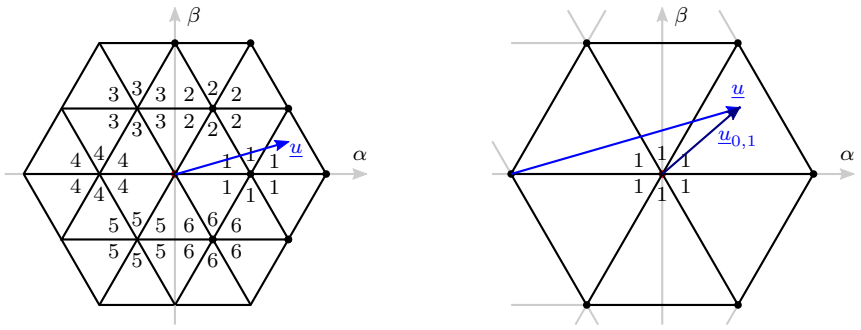
4.2 Existing Simplification Methods

Before the derivation of the new simplification method is carried out a summary of existing methods for simplification is presented.

Simplification Method I

The method presented in [58] has tried to reduce the complexity by simplifying the space vector diagram of a three-level inverter to that of a two-level inverter. Figure 4.2a shows the space vector diagram of a three-level inverter with the basic principle of the described method. The six small hexagons indicated by the corresponding numbers match the geometry of a two-level space vector diagram. As soon as the amplitude and phase of the voltage $\underline{u}$ is known, and thus the hexagon of the reference voltage, a correction of the actual value is made. This correction is achieved by subtracting the centre vector of one of the six hexagons from the reference voltage. The principle is shown graphically in Figure 4.2b.

This method is equally applicable to indirect and direct methods and allows the description of the subsystem as in a two-level inverter. For direct



(a) Three-level space vector diagram (b) Sector simplified to a two-level space vector diagram

Figure 4.2: Basic principle of simplification method I

methods, however, this method only simplifies the description and does not reduce the effort involved in setting up switching tables. Nevertheless, there are many multilevel control procedures in the literature which are based on this simplification method [59, 60].

Simplification Method II

This method proposes a transformation into a 60° coordinate system in order to describe all points in a space vector diagram with integer coordinates [61]. The simplification is described as a general algorithm which can be applied to inverters with any number of levels. It is noted that the steps necessary to find the adjacent three vectors do not depend on the number of levels, and the computational efficiency is very good for simulation tools to examine the properties of multilevel converters.

Figure 4.3 shows a three-level space vector diagram with the axes g and h of the 60° coordinate system. Furthermore, the resulting coordinates of the corner points of the triangles are correspondingly highlighted. The transformation and the transformation matrix for transforming any three-phase voltage into the gh-system is described by the following equation:

$$\vec{u}_{gh} = \boldsymbol{T}_{\mathrm{gh}} \cdot \vec{u} \tag{4.1}$$

with

$$\boldsymbol{T}_{\mathrm{gh}} = \frac{1}{3 \cdot U_{\mathrm{DC}}} \cdot \begin{pmatrix} 2 & -1 & -1 \\ -1 & 2 & -1 \end{pmatrix} \tag{4.2}$$

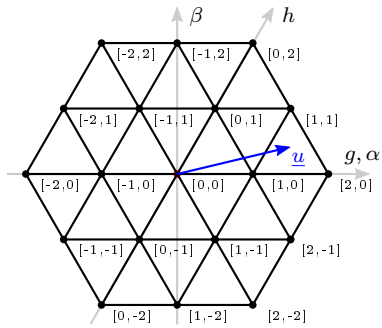


Figure 4.3: Basic principle of simplification method II

A similar approach was implemented in [62]. In contrast to the method shown, a 120° coordinate system is set up here. According to the authors, this method is suitable for converters with any number of levels and it shows the following main advantages:

- Convenient triangular sector selection of reference voltage
- Easy vector synthesizing

4.3 The Idea - Hexagonal Bravais Lattice

In many technical and mathematical disciplines, there are geometric shapes which correspond to those in the space vector diagram. The requirement for

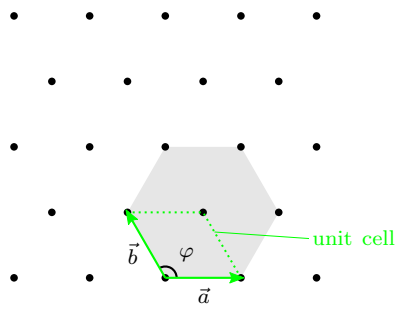


Figure 4.4: Two dimensional hexagonal bravais lattice

a suitable transformation matrix within the research question was to define uniform descriptions, if possible independent from the level number, in order to allow a general representation.

The hexagonal Bravais lattice is one of five fundamental two-dimensional Bravais lattices [63]. In crystallography, the Bravais lattice describes a set of points in the n-dimensional space with translational invariance under any conceivable shift of a lattice point to the origin. Figure 4.4 shows such a hexagonal Bravais lattice with all necessary parameters used for the description.

Space vector diagrams for a two-, three- and five-level inverter as used for SVM methods have already been shown in Figure 4.1. It is apparent that the geometry of the Bravais lattice and the hexagonal space vector diagram fit to each other. Assuming an n-level inverter the geometry of both is actually identical. This fact was one of the fundamental ideas to set-up a transformation matrix based on concepts of the Bravais lattice.

A Bravais lattice simplifies calculations by allowing a decomposition of the infinite plane into universal unit cells which are replicated at all lattice points. Thinking about a two-dimensional Bravais lattice, any point R on the lattice can be described by

$$\vec{R} = a\vec{a} + b\vec{b}, \tag{4.3}$$

where a and b are any integers and $\vec{a}$ and $\vec{b}$ are primitive vectors defining the unit cell. The conventional choice of basis vectors for the hexagonal lattice is

$$|\vec{a}| = |\vec{b}|, \varphi = 120°. \tag{4.4}$$

The idea is now to establish a suitable transformation with which the calculation rules and simplifications can be applied to the space vector diagram of inverter systems.

4.4 Derivation of a_*b_*-Transformation

To employ the characteristics of the Bravais lattices, the three-phase system needs to be transformed into a reference frame using the above described basis. The adoption of Equation 4.3 for an inverter system leads to

$$\vec{u} = u_{a_*}\vec{a}_* + u_{b_*}\vec{b}_* = \begin{pmatrix} u_{a_*} \\ u_{b_*} \end{pmatrix}_{a_*b_*} \tag{4.5}$$

where $\vec{u}$ is a space vector of the reference voltage, u_{a_*}, u_{b_*} are any real numbers and $\vec{a}_*$, $\vec{b}_*$ are the primitive vectors defining the unit cell within the defined a_*b_*-coordinate system.

Chapter 3.1 describes the $\alpha\beta$ transformation which is used to represent a three phase sinusoidal voltage (or current) in an orthogonal reference frame. In fact, a set of three voltage or current vectors which are part of a three-phase system can be replaced by any one of a number of different systems of component vectors as pointed out in [38]. Equation 4.6 shows that the voltage vector $\vec{u}$ can be represented either by $\alpha\beta$ or $\tilde{a}_*\tilde{b}_*$.

$$\vec{u} = \begin{pmatrix} u_\alpha \\ u_\beta \end{pmatrix}_{\alpha\beta} = \begin{pmatrix} u_{\tilde{a}_*} \\ u_{\tilde{b}_*} \end{pmatrix}_{\tilde{a}_*\tilde{b}_*} \tag{4.6}$$

This formula can be replaced by

$$\vec{u} = u_{\tilde{a}_*}\vec{\tilde{a}}_* + u_{\tilde{b}_*}\vec{\tilde{b}}_* = u_\alpha\vec{\alpha} + u_\beta\vec{\beta}. \tag{4.7}$$

Figure 4.5 shows the geometrical representation of formula 4.6. The contribution of vector $\vec{u}$ on the $\tilde{a}_*$-axis is obtained by the geometric interpretation of the $\alpha\beta$ components. The following equation can be derived from Figure 4.5.

$$u_{\tilde{a}_*} = u_\alpha + u_\beta \cdot \tan(30°) = u_\alpha + \frac{1}{\sqrt{3}}u_\beta \tag{4.8}$$

Analogously, the components $u_{\tilde{b}_*}$ can be determined from the geometric relationship.

$$u_{\tilde{b}_*} = u_\beta \cdot \frac{1}{\cos(30°)} = \frac{2}{\sqrt{3}}u_\beta \tag{4.9}$$

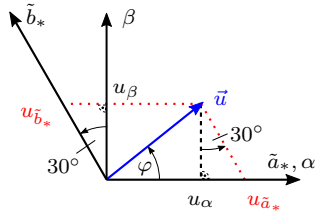


Figure 4.5: Geometric representation of the proposed transformation and relationship to $\alpha\beta$ transformation

The geometric derivation yields to two linear equations with the unknowns $u_{\tilde{a}_*}$ and $u_{\tilde{b}_*}$. Those linear equations (Eq. 4.8 and Eq. 4.9) can be represented with a matrix/vector equation of the form

$$\vec{u}_{\tilde{a}_*\tilde{b}_*} = \boldsymbol{T}_{\alpha\beta\tilde{a}_*\tilde{b}_*} \cdot \vec{u}_{\alpha\beta} \tag{4.10}$$

where $\vec{u}_{\tilde{a}_*\tilde{b}_*}$ is the two dimensional representation of $\vec{u}$ within the $\tilde{a}_*\tilde{b}_*$ system, $\vec{u}_{\alpha\beta}$ corresponds to the two dimensional representation of $\vec{u}$ within the $\alpha\beta$ system and $\boldsymbol{T}_{\alpha\beta\tilde{a}_*\tilde{b}_*}$ is the transformation matrix to transform values between both representations. The solution for $\boldsymbol{T}_{\alpha\beta\tilde{a}_*\tilde{b}_*}$ can now be read directly from Equation 4.8 and Equation 4.9. It follows

$$\begin{pmatrix} u_{\tilde{a}_*} \\ u_{\tilde{b}_*} \end{pmatrix} = \begin{pmatrix} 1 & \frac{1}{\sqrt{3}} \\ 0 & \frac{2}{\sqrt{3}} \end{pmatrix} \cdot \begin{pmatrix} u_\alpha \\ u_\beta \end{pmatrix} \tag{4.11}$$

and thus

$$\boldsymbol{T}_{\alpha\beta\tilde{a}_*\tilde{b}_*} = \begin{pmatrix} 1 & \frac{1}{\sqrt{3}} \\ 0 & \frac{2}{\sqrt{3}} \end{pmatrix} \tag{4.12}$$

The aim is to transform any three-phase voltage (or current) into the $\tilde{a}_*\tilde{b}_*$ coordinate system. Using the three phase Clarke transformation the following relationship can be derived from Equation 4.10.

$$\vec{u}_{\tilde{a}_*\tilde{b}_*} = \boldsymbol{T}_{\alpha\beta\tilde{a}_*\tilde{b}_*} \cdot \boldsymbol{T}_{\alpha\beta} \cdot \begin{pmatrix} u_1 \\ u_2 \\ u_3 \end{pmatrix} \tag{4.13}$$

The transformation matrix $\boldsymbol{T}_{\tilde{a}_*\tilde{b}_*}$ for transforming a three phase voltage into the $\tilde{a}_*\tilde{b}_*$ system is then

$$\boldsymbol{T}_{\tilde{a}_*\tilde{b}_*} = \boldsymbol{T}_{\alpha\beta\tilde{a}_*\tilde{b}_*} \cdot \boldsymbol{T}_{\alpha\beta} \tag{4.14}$$

By inserting $\boldsymbol{T}_{\alpha\beta\tilde{a}_*\tilde{b}_*}$ and $\boldsymbol{T}_{\alpha\beta}$ it follows

$$\boldsymbol{T}_{\tilde{a}_*\tilde{b}_*} = \begin{pmatrix} 1 & \frac{1}{\sqrt{3}} \\ 0 & \frac{2}{\sqrt{3}} \end{pmatrix} \cdot \frac{2}{3} \begin{pmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{pmatrix} = \frac{2}{3} \begin{pmatrix} 1 & 0 & -1 \\ 0 & 1 & -1 \end{pmatrix} \tag{4.15}$$

For a complete invertible transformation matrix $\boldsymbol{T}_{\tilde{a}_*\tilde{b}_*}$ must be square. This can be achieved by adding a row for the neutral point voltage, i.e. the 0-components of a three-phase system. To provide a consistent derivation,

$\tilde{c}_*$ is defined to be orthogonal with respect to the $\tilde{a}_*$ and $\tilde{b}_*$. Thus the transformation matrix is defined to be

$$\boldsymbol{T}_{\tilde{a}_*\tilde{b}_*\tilde{c}_*} = \frac{2}{3}\begin{pmatrix} 1 & 0 & -1 \\ 0 & 1 & -1 \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{pmatrix} \tag{4.16}$$

Finally, to transform a three-phase reference voltage vector into the non-orthogonal $\tilde{a}_*\tilde{b}_*$-coordinate system, the following equation needs to be applied

$$\vec{u}_{\tilde{a}_*\tilde{b}_*} = \boldsymbol{T}_{\tilde{a}_*\tilde{b}_*} \cdot \vec{u}_{\mathrm{UVW}} \tag{4.17}$$

Knowing that the maximum steps in the a_*- and b_*-direction are limited an additional multiplier is included to normalize the corresponding values. In the mentioned example of a two-level inverter 4.17 changes to

$$\vec{u}_{a_*b_*} = \kappa \cdot \boldsymbol{T}_{\tilde{a}_*\tilde{b}_*} \cdot \vec{u}_{\mathrm{UVW}},\ \kappa = \frac{3}{2 \cdot U_{\mathrm{DC}}} \tag{4.18}$$

To simplify the description, for the normalized voltage in the a_*b_* system and the normalized transformation matrix, the following notations will be used:

$$\vec{u}_* = \vec{u}_{a_*b_*} \tag{4.19}$$

and

$$\boldsymbol{T}_* = \kappa \cdot \boldsymbol{T}_{\tilde{a}_*\tilde{b}_*} \tag{4.20}$$

4.4.1 Multilevel a_*b_*-Transformation

As explained above the transformation is suitable to be used in multilevel systems. The derivation was based on a two-level inverter but the adoption to higher level systems can simply be achieved. To describe higher level systems the variable n is introduced describing the level count of an inverter.

Assuming an n-level inverter the equation used to transform and normalize a three phase reference voltage vector into the a_*b_*-coordinate system is now given by

$$\vec{u}_* = \boldsymbol{T}_* \cdot \vec{u}_{\mathrm{UVW}} = \kappa \cdot \boldsymbol{T}_{\tilde{a}_*\tilde{b}_*} \cdot \vec{u}_{\mathrm{UVW}} = \frac{3(n-1)}{2 \cdot U_{\mathrm{DC}}} \cdot \boldsymbol{T}_{\tilde{a}_*\tilde{b}_*} \cdot \vec{u}_{\mathrm{UVW}} \tag{4.21}$$

With this scaling all possible output space vectors can be enumerated in integers $\mathbb{Z}$ for n odd or half-integers $\mathbb{Z} + \frac{1}{2}$ for n even with simple boundary conditions. We define the limit

$$l = n - 1 \tag{4.22}$$

and the odd-even-correction

$$\delta_n = \begin{cases} \frac{1}{2} & \text{for } n \text{ even} \\ 0 & \text{for } n \text{ odd} \end{cases} \tag{4.23}$$

Then the boundary is given by

$$\left\{ a_*, b_* \in \mathbb{Z} + \delta_n \middle| -l \leq a_*, b_*, a_* - b_* \leq l \right\} \tag{4.24}$$

To exemplary show the conditions described by Equation 4.24 Figure 5.15 is used. Each vertex of the three-level space vector diagram is labelled with a_*b_* coordinates. The vertices highlighted in green meet the conditions from Equation 4.24 whereas the red one does not. Although the single coordinates for $a_* = -2$ and $b_* = 1$ are within the defined range the condition $a_* - b_* = -3$ is not. Using the conditions it is confirmed that the coordinate highlighted in red is out of the space vector diagram.

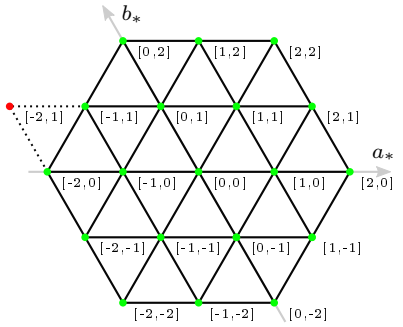


Figure 4.6: Example of a three-level space vector diagram with a_*b_* coordinates

This important property enables fast controller implementations in integer arithmetic, without the need for floating point operations or square roots.

4.5 Determination of Space Vectors and Switching Signals

One of the main outcomes of the transformation explained before is the easy determination of the space vectors needed and best suited for current control within the space-vector diagram especially when using fixed-point arithmetic. The unit cells defined within hexagonal Bravais lattices (Fig. 4.4) show some analogy to the space vectors which are used for effective control of an inverter.

4.5.1 Determination of space vectors

To control an inverter in the steady state, the space vectors that are located closest to the reference voltage vector should be selected. Within the three-level space vector diagram shown in Figure 4.7 the four space vectors form a diamond shaped unit cell are highlighted. Its base vector is defined to be on the lower left corner.

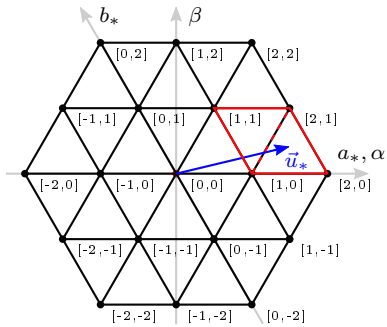


Figure 4.7: Three-level space vector diagram with unit cell (red) and its base vector $[1, 0]$

In this particular case, the coordinates of the base vector in the a_*b_*-coordinate system are [1 0]. Those base vector coordinates $\vec{U}_{*base}$ can simply be calculated from the transformed and normalized reference voltage vector $\vec{u}_*$ using the floor function, which rounds each element of a vector to the next integer which is less or equal to the original entry:

$$\vec{U}_{*\text{base}} = \lfloor \vec{u}_* \rfloor. \tag{4.25}$$

After the determination of the base vector the three missing vectors of the unit cell are calculated by a simple integer addition along the a_*b_* directions. With this knowledge a basic procedure to determine the nearest four space vectors to the reference voltage vector is as follows:

1. Transform and normalize the reference voltage vector using the a_*b_*-transformation.
2. Determine the base vector of the translated unit cell by using the floor function.
3. Calculate the three missing vectors by simply adding a positive unit step along a_*, b_* or both directions. For the example from Figure 4.7:

$$\begin{pmatrix}1\\0\end{pmatrix}+\begin{pmatrix}1\\0\end{pmatrix}=\begin{pmatrix}2\\0\end{pmatrix}\ ;\ \begin{pmatrix}1\\0\end{pmatrix}+\begin{pmatrix}0\\1\end{pmatrix}=\begin{pmatrix}1\\1\end{pmatrix}\ ;\ \begin{pmatrix}1\\0\end{pmatrix}+\begin{pmatrix}1\\1\end{pmatrix}=\begin{pmatrix}2\\1\end{pmatrix} \tag{4.26}$$

After applying those three steps, the four space vectors of the unit cell are identified and can be used for various control or modulation algorithms.

From space vector modulation it is known that three space vectors are sufficient to modulate the reference voltage. Thus, out of the two triangles constituting the unit cell the one containing the reference voltage vector has to be determined. This can be achieved by first calculating

$$\vec{u}_{*\mathrm{base}} = \vec{u}_* - \vec{U}_{*\mathrm{base}}. \tag{4.27}$$

The next step is to formally evaluate the sign of the following dot product of the vector to yield

$$\vec{u}_{*\mathrm{base}} \cdot \begin{pmatrix}1\\-1\end{pmatrix} > 0 \quad \Rightarrow \quad \text{right-side triangle } 0^\circ \text{ to } 60^\circ \tag{4.28}$$

$$\vec{u}_{*\mathrm{base}} \cdot \begin{pmatrix}1\\-1\end{pmatrix} < 0 \quad \Rightarrow \quad \text{left-side triangle } 60^\circ \text{ to } 120^\circ \tag{4.29}$$

4.5.2 Determination of switching signals

Typically, the switching signals of an inverter are indicated as a three-dimensional vector $\vec{S}$. In this case, the first element corresponds to the switching signal for phase U, the second element to the switching signal for phase V, and the third element to the switching signal for phase W. The value of the element corresponds to a defined output voltage at the corresponding phase of the inverter.

The inverter switching signals $[s_{\mathrm{U}}\ s_{\mathrm{V}}\ s_{\mathrm{W}}]$ are usually defined to be within the following limits

$$\{s \in \mathbb{Z} | -\frac{l}{2} \leq s \leq \frac{l}{2}\};\ l = n-1;\ n = \text{odd} \tag{4.30}$$

This results, for the example of a five-level inverter in $\{-2 \leq s \leq 2\}$ and for the example of a three-level inverter in $\{-1 \leq s \leq 1\}$. Using the integer coordinates of the space vectors within the a_*b_* coordinate system, one may easily calculate the appropriate state $\vec{S}$ for each space vector. Therefore $\vec{U}_* = [a_*\ b_*]$ is extended to $\vec{U}_{*0} = [a_*\ b_*\ 0]$ to calculate

$$\vec{S} = \vec{U}_{*0} - \left(\max(\vec{U}_{*0}) - \frac{l}{2}\right) \tag{4.31}$$

For example, for the base vector from Figure 4.7, that means

$$\vec{U}_* = \begin{pmatrix}1\\0\end{pmatrix} \rightarrow \vec{U}_{*0} = \begin{pmatrix}1\\0\\0\end{pmatrix} \rightarrow \vec{S} = \begin{pmatrix}1\\0\\0\end{pmatrix} \tag{4.32}$$

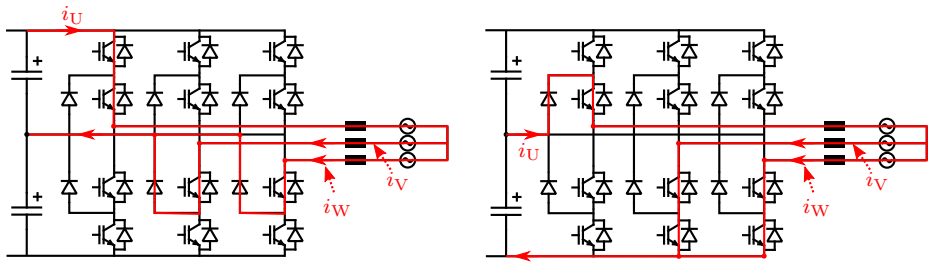
In the case of n-level topologies with an odd number for the level count, the described method works as explained. Implementing systems with an even number for the level count is solved by using half-integer numbers.

4.6 Redundant Space Vectors

There are different multilevel topologies that provide different switching vectors which, however, result in the same output voltage at the inverter. These switching states differ only in the energy source (capacitor) which is used to deliver energy to the load. In the case of a three-phase three-level NPC converter, the power source is either the upper or lower capacitor of the DC-link. These special space vectors are called redundant space vectors and they provide an additional degree of freedom that can be used by the control algorithm. In addition to optimizing the number of switching operations, redundant space vectors are used for DC-link balancing which is mandatory for some hardware topologies. DC-link balancing using redundant space vectors is well known and the focus of intensive research work [64, 65, 66, 67].

Figure 4.8 shows the current flow of redundant switching states of an NPC inverter as an example. Figure 4.8a represents the switching state

[1 0 0] (corresponds to $\vec{U}_* = [1\ 0]$) which implies that the upper two IGBTs of phase U and the center IGBTs of phase V and W are switched on. The current (red) flows into the midpoint M. Figure 4.8b represents the switching state [0 -1 -1] which implies that the middle IGBTs of phase U and the lower IGBTs of phase V and W are switched on. In this case the current flow is out of the midpoint. At this point it should be mentioned again that the inverter output voltages of both switching states are equal.



(a) Switching state [1 0 0] (b) Switching state [0 -1 -1]

Figure 4.8: Current flow for redundant switching states

Applying this definition, the redundant states are enumerated by simply adding or subtracting integer multiples of [1 1 1], as derived above, within the given limits. For the example of a three-level inverter the maximum and minimum values calculated with Formula 4.30 evaluate to $-1 \leq x \leq 1$. Taking the switching state $\vec{S} = [1\ 0\ 0]$, the redundant state vector is calculated as

$$\vec{S}_{\text{red}} = \vec{S} - [1\ 1\ 1] = [0\ -1\ -1] \tag{4.33}$$

4.7 Summary of Chapter 4

In the preceding chapter, a brief summary of existing methods to reduce the complexity of space-vector-based control methods was presented. These methods all have the aim of simplifying the description of the inverter output voltages so that the selection of more and more possibilities can be used in a suitable control method.

Subsequently, a transformation matrix, which can be used for simple and straightforward control procedures for multilevel inverters, has been derived.

Using the method presented, the complexity of space vector controlled n-level inverters can be reduced to a minimum. The special feature is that all coordinates are scaled to integers and can thus be used very easily for calculations by microprocessors and FPGAs.

It is clear that the quality of the determination of all necessary parameters depends very strongly on the accuracy of determining the voltage vector position and filter algorithms. The main focus, however, was to reduce the complexity of space vector-based methods by means of a suitable mathematical description. In addition to the simple description, the method can also be used to easily determine the switching states, the redundant switching states and the gate signals.

Chapter 5

Scalar Hysteresis Control

5.1 Introduction

The main objective of this thesis is the development of a direct current control method which, in the steady state, keeps the current inside a given hysteresis band using only three adjacent space vectors of a space vector diagram (like with standard SVPWM methods). As already mentioned in the previous chapters, there exist a number of direct, $\alpha\beta$-based methods all having advantages and real drawbacks. When using only three adjacent space vectors with the standard $\alpha\beta$ method, the system is undefined in some areas considering that none of the vectors is able to reduce both current errors in the α and β direction. Further developments (SDHC method) are always able to reduce the current error but only by the inclusion of a fourth additional space vector. This additional vector has the disadvantage of creating a higher voltage across the inductor, which in the worst case means a reduction of the quality of the current or voltage signal.

In addition to the main objective, secondary objectives were defined. Since direct methods are often implemented using switching tables, the expansion to inverter systems with higher level counts is rather complex. A generic approach is intended to provide a simple extension to systems with higher levels when using the new method. Moreover, some further problems which exist in principle in all $\alpha\beta$-based methods are solved by a suitable strategy, for example the issue of unsymmetrical switching frequency in the three phases. In all cases, however, the method should finally be described in a simple and, if possible, in a mathematical manner.

Since the basic function of the new control method is based on a geometric solution approach and can be traced back to the calculation of a scalar product, the new method is now referred to as *"Scalar Hysteresis Control - SHC"*.

5.2 Basic Considerations

5.2.1 System Description

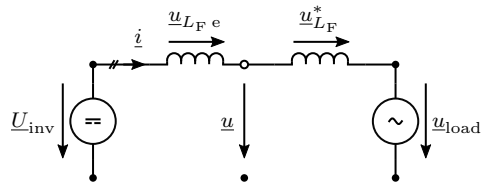


Figure 5.1: Simplified equivalent circuit of grid connected inverter systems

Figure 5.1 shows a simplified n-level system consisting of a VSI, an inductance and an ideal sinusoidal source. In this case, it is initially assumed that the VSI is supplied from an ideal DC voltage source with a constant voltage U_DC. The three currents i_UVW are the variable to be controlled and whose slope can be determined via the inductance L_F and the voltage u_{L_F} across the inductance. The reference voltages are assumed to be ideal three-phase sinusoidal voltages and are denoted by u_{123}. Since the newly derived method is a space vector-based direct modulation method, all system values (currents and voltages) are transformed into the complex $\alpha\beta$ system using the Clarke transformation. The system values are obtained according to the following equations. The complex current space vector $\underline{i}$ is calculated as

$$\underline{i} = \frac{2}{3}(i_\mathrm{U} + \underline{a} i_\mathrm{V} + \underline{a}^2 i_\mathrm{W}) \tag{5.1}$$

with $\underline{a} = \mathrm{e}^{j\frac{2\pi}{3}}$. Furthermore, the reference voltage vector $\underline{u}$ can be described by the following equation as derived in Section 3.3.

$$\underline{u} = \underline{u}^*_{L_\mathrm{F}} + \underline{u}_\mathrm{load}. \tag{5.2}$$

A requirement for the control method is using only those three space vectors directly adjacent $\underline{u}$. This requirement reduces the selection of the sectors to a triangular section in the space vector diagram for all level counts n. For the derivation of the method, a simple two-level inverter can be assumed for this reason. The transferability to inverters with higher levels is ensured since the triangular sector geometry does not change with an increased level

count. The number of possible output voltages of an n-level inverter can be determined by:

$$k_{\max} = n^3 \tag{5.3}$$

Considering a two-level inverter, the resulting eight space vectors SV_k from the space vector diagram correspond to six constant non-zero output voltages that will be described as

$$\underline{U}_{\mathrm{inv}(k)} = \frac{2}{3} U_{\mathrm{DC}} \mathrm{e}^{\frac{jk\pi}{3}}, \; k = 1, 2, 3, 4, 5, 6 \tag{5.4}$$

and the zero voltage vectors $\underline{U}_{\mathrm{inv}(0/7)}$ which are defined by:

$$\underline{U}_{\mathrm{inv}(0/7)} = 0 \text{ V} \tag{5.5}$$

Figure 5.2 shows the resulting space vector diagram of the system described above. The voltages from equations 5.4 and 5.5 correspond to the space vectors SV_k. The reference voltage $\underline{u}$ is shown and is located in sector 1. The voltage $\underline{u}_{L_{\mathrm{F}}\,\mathrm{e}}$, by which the current rise and its direction is determined, can be calculated from

$$\underline{u}_{L_{\mathrm{F}}\,\mathrm{e}} = \underline{U}_{\mathrm{inv}(k)} - \underline{u} \tag{5.6}$$

This voltage can be illustrated as the vector with the starting-point at the tip of the reference voltage leading to one specific output voltage of the inverter.

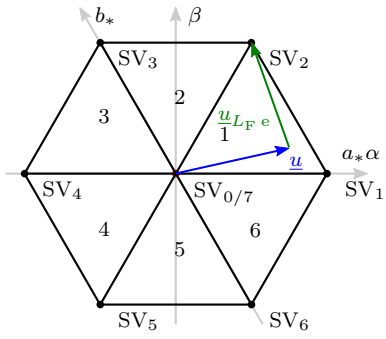


Figure 5.2: Two level space vector diagram with reference voltage

5.3 Sector and Tolerance Band Geometry

5.3.1 Sector Geometry

It is a fact that three space vectors are sufficient to modulate the reference voltage when using SVPWM. For this purpose, the reference voltage is modulated as a short-term average value of the discrete inverter output voltages within a single sector. The reason for choosing only three directly adjacent space vectors is that they produce the smallest possible voltage error and distortion.

Figure 5.3 shows one sector from a space vector diagram including the three possible output voltages and the reference voltage $\underline{u}$. In principle, the reference voltage $\underline{u}$ can be described as

$$\underline{u} = a_1\underline{U}_{\mathrm{inv}(1)} + a_2\underline{U}_{\mathrm{inv}(2)} + a_3\underline{U}_{\mathrm{inv}(3)} \tag{5.7}$$

where a_1, a_2 and a_3 correspond to the relative switch-on times of the respective space vectors. When using direct modulation methods the basis time interval is, unlike in SVPWM methods, random. Nevertheless, with respect to the time interval the following conditions must be guaranteed:

$$a_1 + a_2 + a_3 = 1,\ a_1, a_2, a_3 \geq 0 \tag{5.8}$$

For controllability, it must be further ensured that the short-term average value of the inverter output voltages can be anywhere around the load voltage. It must be guaranteed that the reference voltage is located inside the triangular sector.

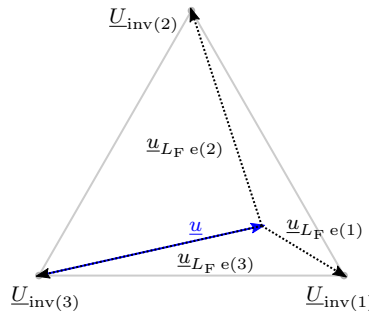


Figure 5.3: Sector geometry and resulting voltages

5.3.2 Tolerance Band Geometry

The choice of the tolerance band geometry has effects on the overall behaviour of the current controller. For example, it must be ensured that the three output voltages which correspond to the corner points in the equilateral triangular sector (see Fig. 5.3) are able to reduce the current error when the tolerance band is violated. As already mentioned before, at least one of the three output voltages are always able to reduce the error. Nevertheless, in standard implementations of the $\alpha\beta$ controller there are scenarios where no error reducing output voltage can be selected.

In the case of a separate consideration of α and β, as is established with standard methods, rectangular geometries are obtained for the tolerance bands (see Fig. 5.4). This property gives four possible fault conditions which must be taken into account by the control method. The current in the direction of

1. α and β too big
2. α and β too small
3. α too large and β too small
4. α too small and β too big

As shown in Figure 5.3, only three output voltages are available in a triangular sector. Since there are four fault conditions and only three space vectors the current error can not be reduced in each of the possible fault conditions.

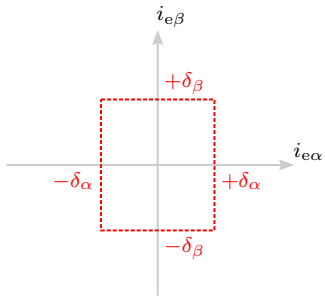


Figure 5.4: Rectangular current error tolerance area

From the previous assumption it can be derived, for standard implementations of the $\alpha\beta$ controller, that it is only possible to reduce the current error with three space vectors if the tolerance band geometry produces three

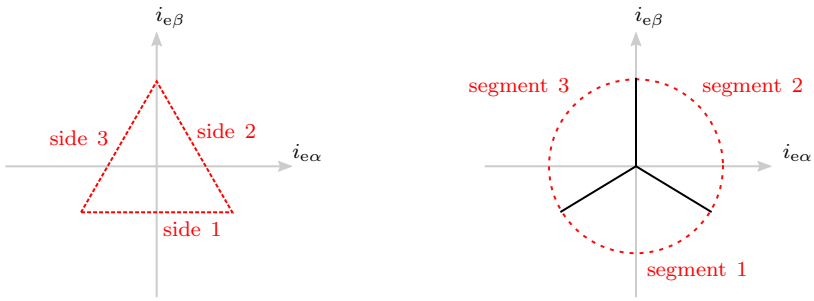
possible fault conditions. In the simplest case, this can be achieved if a triangular shape is selected as the tolerance band geometry. Figure 5.5a shows a triangular tolerance area geometry for the current error. This results in three possible fault conditions which must be considered by the control method.

1. Error occurs on triangle side 1
2. Error occurs on triangle side 2
3. Error occurs on triangle side 3

The description of the triangular tolerance area and the detection of a tolerance band violation is feasible with simple mathematical descriptions, but it is cumbersome in the implementation. For this reason, a circular geometry, which can be divided into three segments is proposed. As highlighted in Figure 5.5b, there are also three possible fault conditions which must be considered by the control method.

1. Error occurs on segment 1
2. Error occurs on segment 2
3. Error occurs on segment 3

In the illustrated case, the individual circular segments correspond to the angular range of 120° each. If an error occurs in a particular segment of the circle, an output voltage from the triangular sector can be selected which reduces the current error at any time. Further advantages when choosing a circular shaped tolerance area are the rotational-symmetric geometry, the simple mathematical representation, the geometric relationship to the sectors in the space vector diagram and the fact that the absolute value of the current error is equal in all directions.



(a) Triangular tolerance area geometry (b) Circular tolerance area geometry

Figure 5.5: Triangular and circular tolerance areas for the current error

5.3.3 Tolerance Area

Taking into account the above-described advantages and circumstances, a circular tolerance area is selected for the new control method. The tolerance boundary $\underline{B}$ can be assumed to be a circle with a defined radius centred at the tip of the time-variable set-point current. The tolerance circle can thus be described as follows:

$$\underline{B} = \underline{i}^* + \delta e^{j\varphi},\ 0 \leq \varphi < 2\pi \tag{5.9}$$

where $\delta \in \mathbb{R}^+$ is the radius and thus the limit of the tolerance band. Figure 5.5b shows the relationship between the currents and the tolerance area in the complex $\alpha\beta$ diagram. In this diagram $\underline{i}^*$ is the current set-point and $\underline{i}$ is the measured actual current. The deviation of the measured current value $\underline{i}$ from the set-point current value $\underline{i}^*$ corresponds to the error current $\underline{i}_\mathrm{e}$ which is also shown in the figure. The set-point is subtracted from the actual value to get the vector of the current error.

$$\underline{i}_\mathrm{e} = \underline{i} - \underline{i}^* \tag{5.10}$$

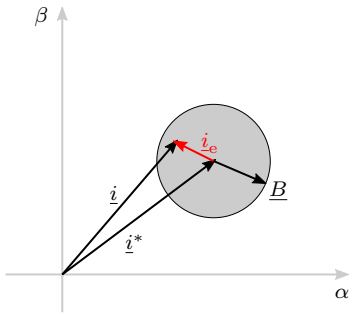


Figure 5.6: Current vectors, error current and tolerance band

5.4 Principle of the SHC Method

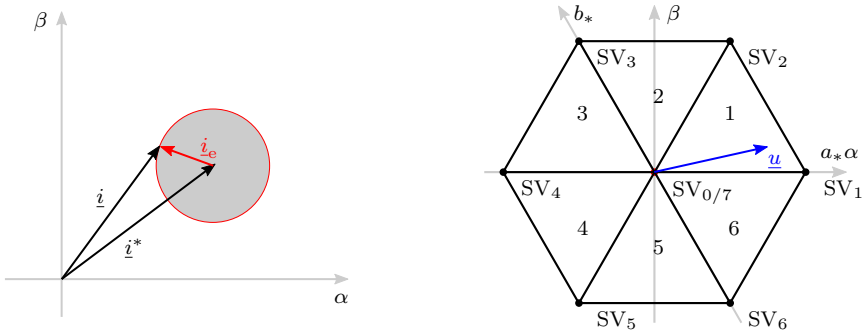
The basic structure of the SHC method is similar to other direct $\alpha\beta$ based methods. The three-phase output current of the inverter is measured and transformed into the $\alpha\beta$ system. The error current can then be calculated via the set-point and the measured value of the current. As soon as the hysteresis limit is reached, the method selects an output state which reduces the current error.

The derivation of the method is carried out with the help of a single triangular sector. Since this sector geometry is identical for all topologies and level numbers, the derivation is performed on a standard two-level inverter system. Furthermore, it is initially assumed that the exact position of the reference voltage is known and thus the correct sector is selected. Following to the general description, this condition can be omitted with the introduction of the seeking algorithm in Section 5.8.

5.4.1 Selection of Current Error Reducing Output Vector

Figure 5.7a shows the set-point and measured current as well as the resulting current error. At this point in time, the current error reaches the hysteresis limit leading to the selection of a new inverter output voltage that reduces the current error. On the other hand, Figure 5.7b shows the space vector diagram of a two-level inverter. The voltage $\underline{u}$ is associated to the point in time at which the current error triggers a new selection. In the illustrated case, the voltage is therefore in the first sector of the space vector diagram.

To simplify the explanation and to annotate all relevant voltages, Figure 5.8a shows only the first sector of the space vector diagram. As one can see, the reference voltage $\underline{u}$ is pointing to an arbitrary point in the triangular sector. Using the simplified circuit diagram shown in Figure 5.1 and Equation 5.6, the feasible voltages across the inductance correspond to space vectors with the starting point at the tip of $\underline{u}$ to the vertices of the triangle. The three available corner points offer the possibility to select one out of three different voltages across the inductance and thus three different choices to manipulate the direction of the current flow. Figure 5.8b shows the current error $\underline{i}_\mathrm{e}$ in the complex $\alpha\beta$ plane as an enlargement from Figure 5.7a. As the aim of the current controller is to keep the current error within a given tolerance band only the current error is shown.

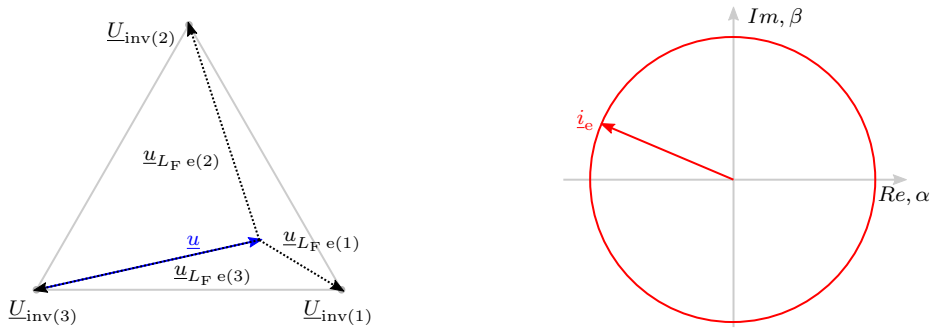


(a) Current vectors with tolerance band violation

(b) Two level space vector diagram with reference voltage

Figure 5.7: Current error and space vector diagram

The data from Figure 5.8 is now used to determine the optimal inverter output voltage which is selected to reduce the current error. The two figures can be linked together to better illustrate the geometric solution approach on which the new control method is based. For this reason, as shown in Figure 5.9, the two figures are combined so that the origin of the coordinate system of the current error is located on the tip of the reference voltage. This is reasonable because the inverter output voltages have a direct influence on the voltage across the inductor and thus also have a direct influence on the future behaviour of the current. The voltage across the inductance changes



(a) Triangular sector and corresponding voltages

(b) Current error in $\alpha\beta$ plane

Figure 5.8: Triangular sector and current error in $\alpha\beta$-plane

the direction and the slope of the current and thus also of the current error. Since the explanation is carried out using the example of a standard two-level inverter, the voltage $\underline{U}_{\mathrm{inv}(3)}$ is exactly opposing the reference voltage.

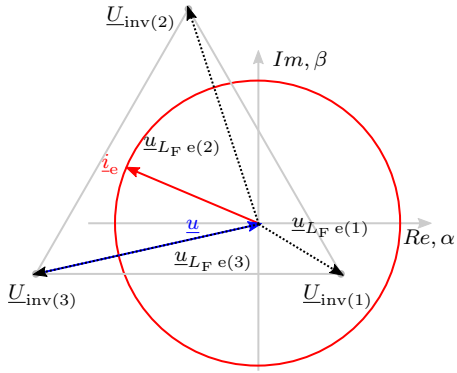


Figure 5.9: Combined representation of triangular sector and current error

As described the resulting voltages across the inductance for each of the three inverter output voltages can be determined with the system equation. They are given by:

$$\underline{u}_{L_\mathrm{F}\,\mathrm{e}(k)} = \underline{U}_{\mathrm{inv}(k)} - \underline{u} = \hat{U}_{L_\mathrm{F}\,\mathrm{e}(k)} \mathrm{e}^{j\varphi_{(k)}},\ k = 1, 2, 3 \tag{5.11}$$

where $\hat{U}_{L_\mathrm{F}\,\mathrm{e}(k)} \mathrm{e}^{j\varphi_{(k)}}$ is the polar form of the complex value $\underline{u}_{L_\mathrm{F}\,\mathrm{e}(k)}$. The magnitude $\hat{U}_{L_\mathrm{F}\,\mathrm{e}(k)}$ is a factor which influences the rate of change of the current vector and φ is the angle which determines the direction. Using the component equation of the inductance the rate of change is given by:

$$\frac{\mathrm{d}}{\mathrm{d}t} \underline{i}_{(k)} = \frac{\hat{U}_{L_\mathrm{F}\,\mathrm{e}(k)}}{L} \mathrm{e}^{j\varphi_{(k)}},\ k = 1, 2, 3 \tag{5.12}$$

In order to select the correct output voltage that produces a component best opposing the current error, the angle between the current error $\underline{i}_\mathrm{e}$ and the three possible voltages across the inductance $\underline{u}_{L_\mathrm{F}\,\mathrm{e}(k)}$ needs to be calculated. Figure 5.10 shows three coordinate systems each with the same error current, but with the three different voltages taken from Figure 5.9.

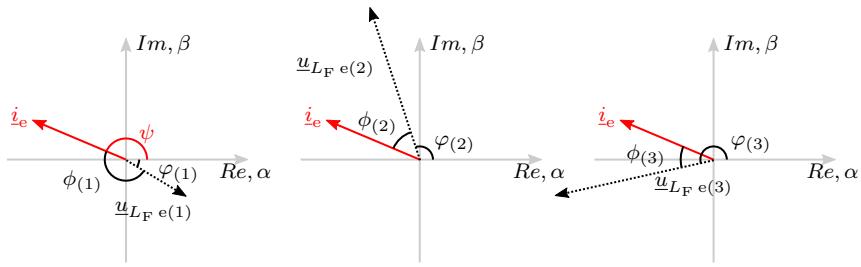


Figure 5.10: Voltage vectors and current error vector resulting from the triangular sector

The task is to select the case where the angle between the inductance voltage $\underline{u}_{L_F\,e(k)}$ and the error current $\underline{i}_e$ is nearest to $\pm 180°$. To calculate the angle $\phi_{(k)}$ between those vectors the following equation is used

$$\phi_{(k)} = \varphi_{(k)} - \psi \tag{5.13}$$

where ψ is the angle of the vector $\underline{i}_e$ and $\varphi_{(k)}$ are the angles of the vectors $\underline{u}_{L_F\,e(k)}$.

A computationally efficient way to find this optimum case can be specified using the complex scalar product between $\underline{u}_{L_F\,e(k)}$ and $\underline{i}_e$

$$\langle \underline{u}_{L_F\,e(k)}, \underline{i}_e \rangle = \underline{u}_{L_F\,e(k)} \cdot \bar{\underline{i}}_e \tag{5.14}$$

where $\bar{\underline{i}}_e$ denotes the complex conjugate of $\underline{i}_e$. Substituting the polar form of $\underline{u}_{L_F\,e(k)} = \hat{U}_{L_F\,e(k)} e^{j\varphi_{(k)}}$ and $\underline{i}_e = \hat{I}_e e^{j\psi}$ results in

$$\underline{u}_{L_F\,e(k)} \cdot \bar{\underline{i}}_e = \hat{U}_{L_F\,e(k)} \cdot \hat{I}_e e^{j(\varphi_{(k)} - \psi)}. \tag{5.15}$$

After applying Euler's formula this changes to

$$\underline{u}_{L_F\,e(k)} \cdot \bar{\underline{i}}_e = \hat{U}_{L_F\,e(k)} \cdot \hat{I}_e (\cos(\phi_k) + j \sin(\phi_k)). \tag{5.16}$$

From Equation 5.16 and due to the properties of the cosine function it is obvious that the case with the smallest real

$$\mathrm{Re}\{\underline{u}_{L_F\,e(k)} \cdot \bar{\underline{i}}_e\} = \hat{U}_{L_F\,e(k)} \cdot \hat{I}_e \cdot \cos(\phi_k) \tag{5.17}$$

corresponds to the requested case where $\phi_{(k)}$ is nearest to $\pm 180°$. Thus, the index k_{opt} of the next output voltage vector which is most suitable for reducing the current error can be determined according to

$$k_{\mathrm{opt}} = \underset{k\in\{1,2,3\}}{\arg\min} \left(\mathrm{Re}\{\underline{u}_{L_{\mathrm{F}}\,\mathrm{e}(k)} \cdot \bar{\underline{i}}_{\mathrm{e}}\} \right). \tag{5.18}$$

For the implementation, Equation 5.18 will usually be evaluated for $\underline{u}_{L_{\mathrm{F}}\,\mathrm{e}(k)}$ and $\bar{\underline{i}}_{\mathrm{e}}$ in component form where it simplifies to

$$k_{\mathrm{opt}} = \underset{k\in\{1,2,3\}}{\arg\min} \left(\mathrm{Re}(\underline{u}_{\mathrm{L_F\,e(k)}}) \cdot \mathrm{Re}(\underline{i}_{\mathrm{e}}) + \mathrm{Im}(\underline{u}_{\mathrm{L_F\,e(k)}}) \cdot \mathrm{Im}(\underline{i}_{\mathrm{e}}) \right). \tag{5.19}$$

Obviously this will not require to calculate any trigonometric functions.

The derivation shown above shows a geometric solution approach for the determination of the one space vector which best opposes the current error and thus reduces it to zero in the fastest way. It was shown that the problem can be reduced to the simple solution of a scalar product. Furthermore, it was shown that the best opposing space vector can be determined without the use of complex trigonometric functions.

5.5 Summary of the SHC Concept

In the previous sections the concept of the SHC controller was basically derived. The concept and the structure is summarized on the basis of a converter system as schematically shown in Figure 5.11.

In summary, the current error is calculated from the real measured current and the set-point current. As soon as the tolerance band is reached, a new error reducing space vector is selected (see Section 5.4.1). The selection of this space vector requires valid and exact information on the position of the reference voltage. Using a simplification algorithm, the three directly adjacent space vectors in a triangular sector are selected from the exact position of the reference voltage (see Section 4.5).

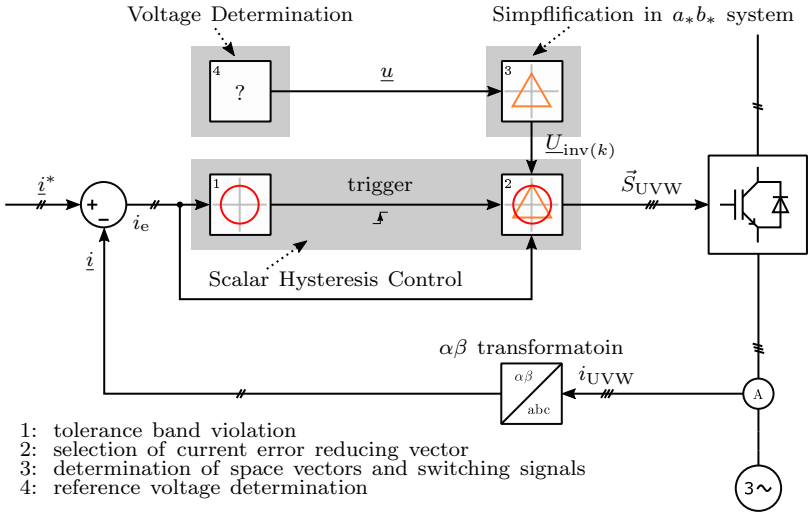


Figure 5.11: Basic concept and overview of the SHC controller

5.6 Simulations, Characteristics and Evaluation Criteria

Since most of the modulation methods are optimized for specific applications, it becomes very difficult to define clear and precise evaluation criteria. Within this section the functionality of the new current controller is analysed using an ideal inverter and by evaluating key characteristic data.

As mentioned, the simulations are carried out using an ideal two-level inverter system as shown in Figure 5.1. No dead-times and losses are implemented so that the working behaviour matches the theoretical considerations. The position of the reference voltage is assumed to be known for the following considerations so that the selected sector always corresponds to the actual sector with its three adjacent space vectors. This ensures that the functionality of the control method is guaranteed at all times.

For all the following simulations the relevant system parameters were adjusted to a specific operation point to guarantee a good comparability. The DC-link voltage was set to be 600 V and the amplitude of the three-phase sinusoidal set-point current was set to 30 A within the simulations.

Since direct current control methods depend very much on the degree of modulation, the result of the simulations will differ when changing that value. Therefore the results are shown for different degrees of modulation. The degree of modulation (modulation index) can be determined according to the following equation:

$$M = \frac{2\hat{U}}{U_{\mathrm{DC}}} \tag{5.20}$$

where $\hat{U}$ is the peak value of the three phase sinusoidal voltage and U_{DC} is the DC-link voltage of the inverter.

Stationary Operating Point

The simplest way to explain the new control method is a stationary operating point. The stationary voltage $\underline{U}_{\mathrm{load}}$ is set to the arbitrary DC value

$$\underline{U}_{\mathrm{load}} = \frac{2U_{\mathrm{DC}}}{5} \mathrm{e}^{j35^\circ} \tag{5.21}$$

The associated space vector diagram is shown in Figure 5.12. The voltage $\underline{U}_{\mathrm{load}}$ is located in sector 1 and the set-point current $\underline{i}^*$ is defined by a three

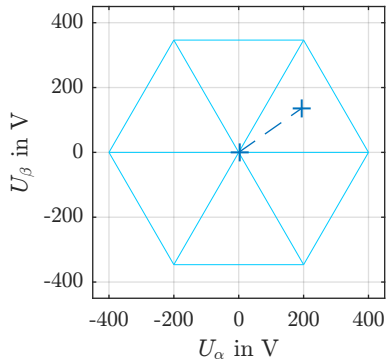


Figure 5.12: Two-level space vector diagram with stationary voltage $\underline{u}_{\text{load}}$

phase sinusoidal waveform with an amplitude of 30 A. The chosen parameters have the consequence that even the averaged inverter output voltage $\underline{u}$ is located in sector 1 and thus only the space vectors SV_1, SV_2 and $\text{SV}_{0/7}$ are used to control the current. Figure 5.13 shows one period of the inverter output current controlled by the proposed method. The error current which results from the difference of the inverter output and the set-point current is shown in Figure 5.14. As the proposed controller uses a circular tolerance area in the $\alpha\beta$ plane the maximum current error in the three phases is always equal to the radius of the circle. In the presented simulation, the radius of the tolerance band was chosen to be 1 A.

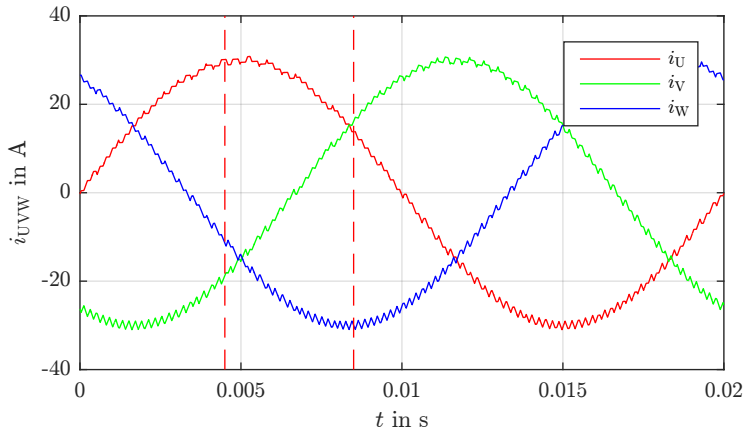


Figure 5.13: Inverter output current

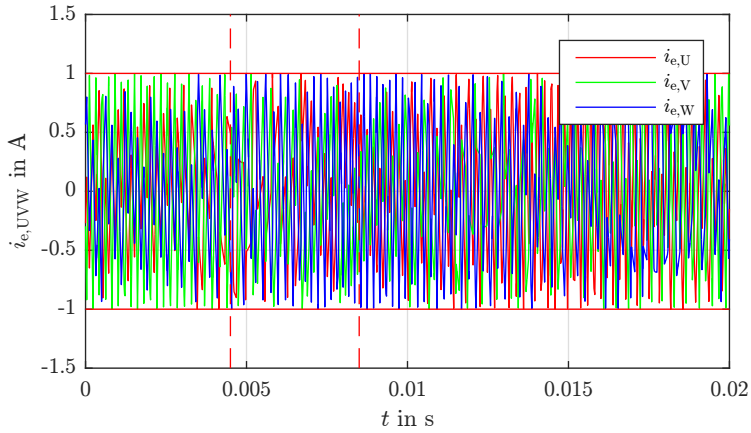
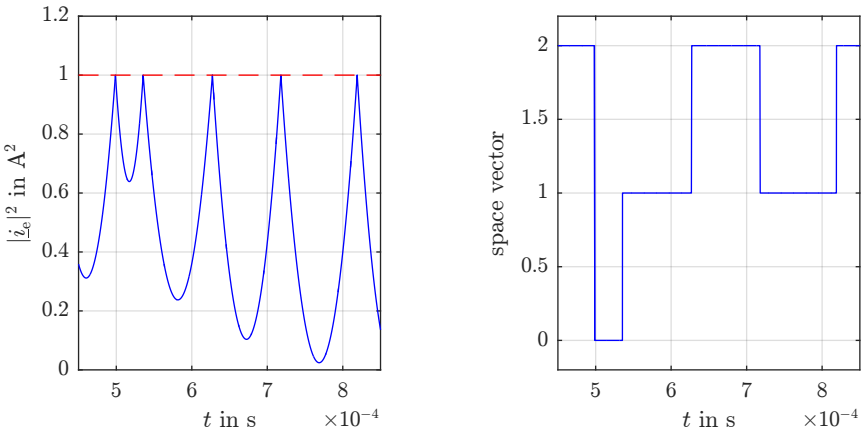


Figure 5.14: Three phase error current

As explained in section 5.4 the calculation of a new error reducing space vector is triggered by a hysteresis limit violation. Figure 5.15a shows the squared absolute value of the current error for the highlighted time segment from Figure 5.14. Each time this value reaches the hysteresis limit, a new output space vector is selected, as shown in Figure 5.15b.

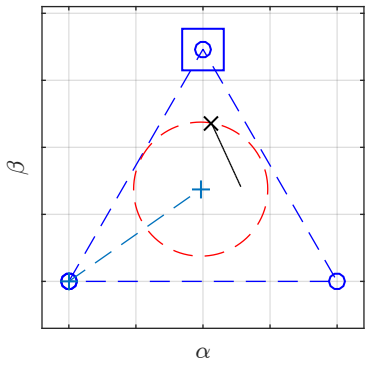


(a) Squared absolute value of the current error

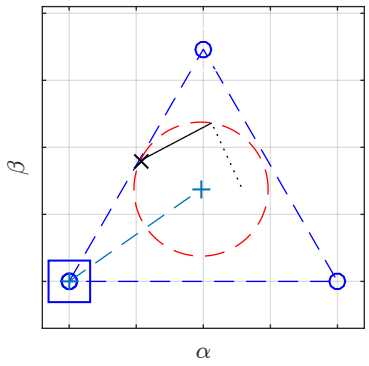
(b) Space vectors

Figure 5.15: Specific time section of stationary operating point

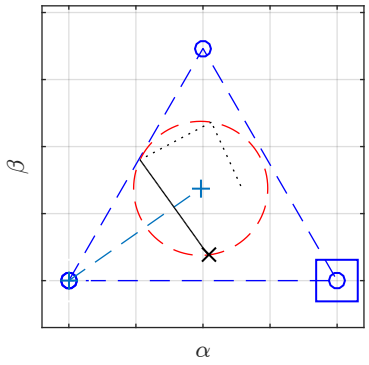
It is apparent that for this specific time segment three different space vectors are selected for six switching states and five switching operations are performed. To show the behaviour of the control method and the effect of each of the output space vectors on the current error, Figure 5.16 shows six different states. Each of the sub-figures shows the first sector of the space vector diagram, the hysteresis border and the current error. The black solid line with the **x** at the tip shows the trajectory of the current error assuming that a specific space vector (marked with the blue square) is selected. The black dotted lines show the previous trajectories. Exemplary Figure 5.16a shows current error trajectory for space vector SV_2. As soon as the current error reaches the tolerance band the space vector SV_0 is selected causing a change of the direction of the current error. The remaining sub figures illustrate the complete behaviour for the chosen time segment.



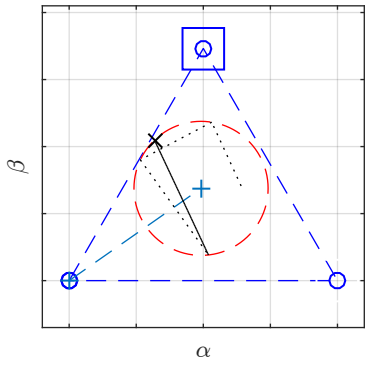
(a) First trigger position $\underline{U}_{\mathrm{inv}(2)}$



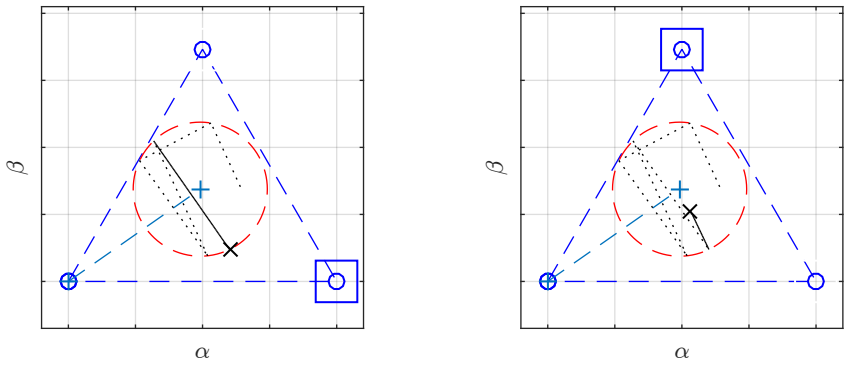
(b) Second trigger position $\underline{U}_{\mathrm{inv}(3)}$



(c) Third trigger position $\underline{U}_{\mathrm{inv}(1)}$



(d) Fourth trigger position $\underline{U}_{\mathrm{inv}(2)}$



(e) Fifth trigger position $\underline{U}_{\mathrm{inv}(1)}$ (f) Sixth trigger position $\underline{U}_{\mathrm{inv}(2)}$

Figure 5.16: Exemplary trigger positions for stationary operating point

Nominal Operating Point

As in grid connected systems, a three phase sinusoidal voltage with the amplitude of $\hat{U}_{\mathrm{load}} = 325$ V is assumed in this sections, which corresponds to the nominal operating point. In contrast to the stationary operating point, the $\alpha\beta$ representation is a rotating space vector running through each of the six sectors within one time period. Figure 5.17 shows the two-level space vector diagram including the grid voltage $\underline{u}_{\mathrm{load}}$.

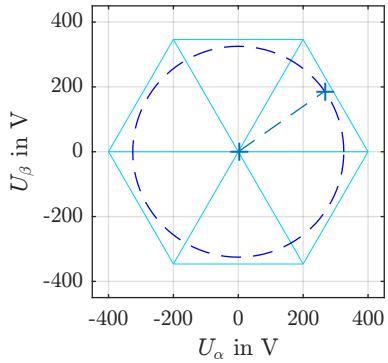


Figure 5.17: Two-level space vector diagram with grid voltage $\underline{u}_{\mathrm{load}}$

The output current of the inverter is shown in Figure 5.18. It becomes clear that the current control method works as expected. As in the case of the stationary operating point the current error is kept within the tolerance band. The only difference is that all six sectors are used for control (instead of only one in the stationary case).

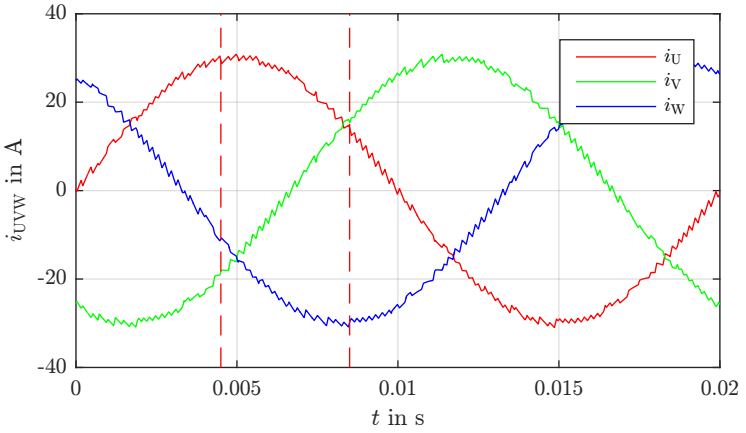


Figure 5.18: Inverter output current for nominal operating point

Figure 5.19 shows the selected space vectors for the time period in Figure 5.18. From this Figure it becomes clear that all vectors are used to control the current. The restriction is that as zero voltage vector only space vector SV_0 was selected for clarity reasons.

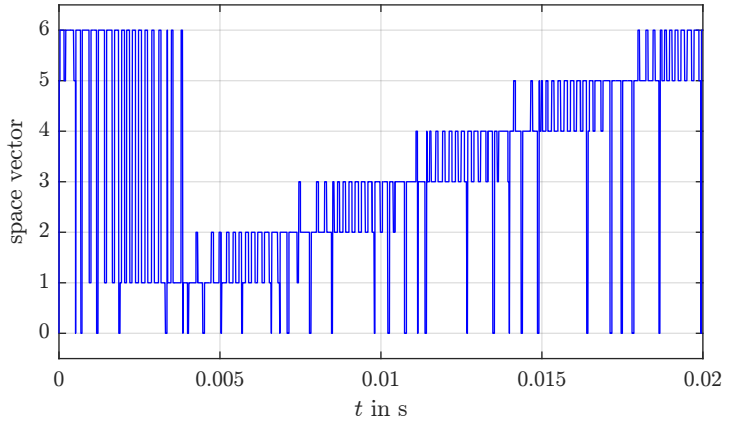


Figure 5.19: Space vectors for one period of nominal operating point

Switching Frequency Versus Modulation Index

Figure 5.20 shows the average switching frequencies of the inverter under varied modulation index for each of the three phases. The variation of the switching frequency is caused by the functional principle of the modulation method. As the voltage across the inductances and thus the resulting slope of the current directly depends on the modulation index, the minimum switching frequencies are located at points where the output voltage of the inverter is close to the reference voltage.

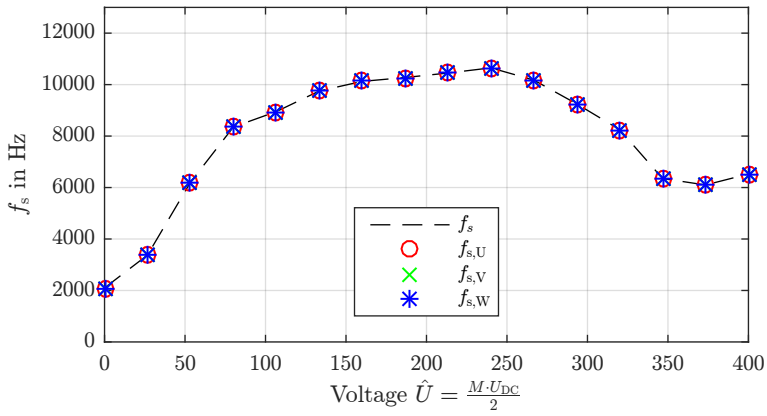


Figure 5.20: Average witching frequency per phase and total versus modulation index

It is known that $\alpha\beta$ hysteresis based controllers exhibit the disadvantage of unequal switching frequencies differing among the three phases by about 20% to 30%. From Figure 5.20 it is recognizable that the switching frequencies do not differ from each other. This is achieved by building up the proposed control method with a 3-fold rotational symmetry. In fact, the proposed method maintains a 6-fold rotational symmetry, of which 3-fold rotational symmetry is a subset. This simulation has proven that a circular tolerance band for the current error as well as switching vectors located around the reference voltage in an equilateral triangle lead to symmetric switching frequencies within the three phases.

Mean Value Versus Modulation index

The mean value of the current error should be zero over a period to ensure that no DC offset is present. An offset at this value leads to a sustained control deviation which may be disadvantageous. Figure 5.21 shows that there exists a small deviation in the mean value for the single phases. This can be attributed to the fact that, for the sake of simplicity, only one zero-voltage vector was used and that no common mode controller is implemented. However, the sum of all three error currents, and thus the sum of the mean value of the current error, is zero.

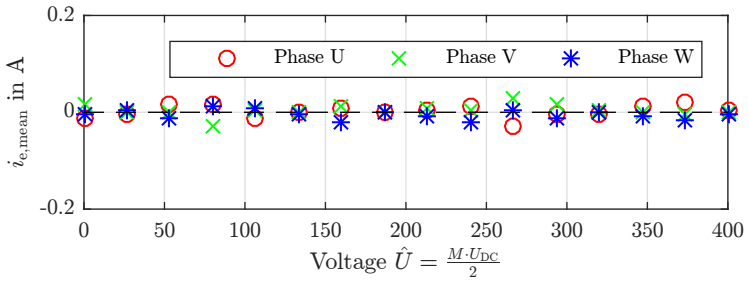


Figure 5.21: Mean value of current error versus modulation index

RMS Value Versus Modulation index

The RMS value of the current error should be independent from the operating point of the inverter. This allows to define the value as a function of the tolerance band. For a circular tolerance band with a radius of $|\underline{B}|$, the RMS value of the current error is given by the following equation [8]

$$I_{e,UVW} = \frac{2|\underline{B}|}{2\sqrt{3}} = \frac{|\underline{B}|}{\sqrt{3}} \tag{5.22}$$

The RMS values with varied modulation index and a fixed hysteresis of $|\underline{B}| = \sqrt{2}$ A are shown in Figure 5.22. Inserting the value into Equation 5.22 results in a calculated RMS value of $I_{e,rms,UVW} \approx 0.808$ A. From the figure it can be seen that the variation of the RMS value in the three phases is small and lower than the theoretical value.

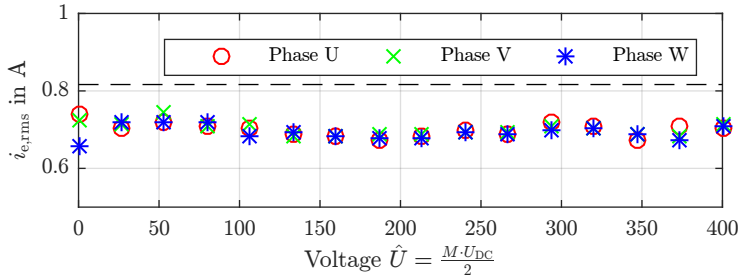
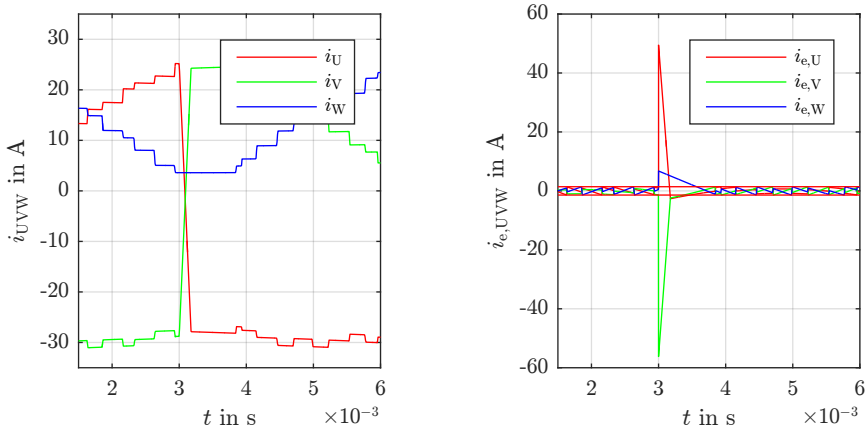


Figure 5.22: RMS value of current error versus modulation index

Dynamic Behaviour

Like all direct current control methods, the SHC algorithm has an excellent dynamic behaviour. In an ideal system a set-point change will immediately cause a violation of the tolerance band and thus the selection of an inverter output voltage that reduces the current error. As soon as the new set-point has been reached, the current is kept within the specified hysteresis limit. In contrast to indirect methods, no transient states can be detected after reaching the final value.



(a) Three phase current at set-point change

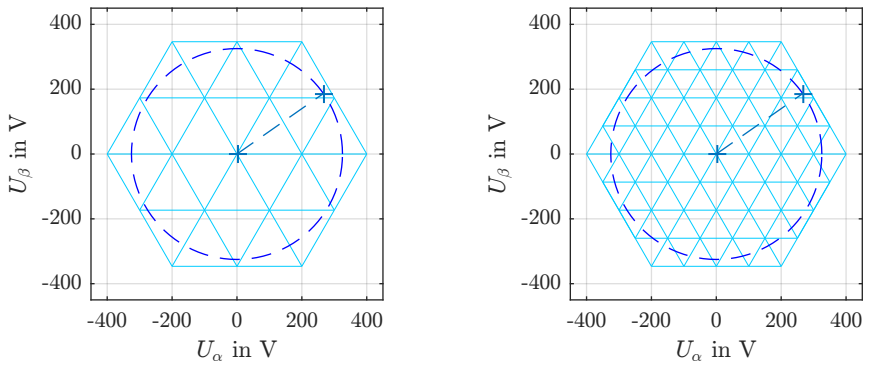
(b) Three phase current error at set-point change

Figure 5.23: Time interval where a set-point change from 30 A to -30 A occurs

Figure 5.23a shows a time section of the inverter output current for a set-point change from 30 A to -30 A. This step corresponds to a reversal of the power flow and shows that the SHC controller is able to operate in both power flow directions. Figure 5.23b shows the corresponding three-phase current error. From this figure it becomes clear that the error reducing vector is selected immediately after the step change and that the current error is held inside the tolerance band after $\Delta t < 1$ ms. Subsequent observations on the dynamic behaviour will show that the dynamics can be further improved by utilizing the complete voltage operation range of the inverter especially for higher level systems.

5.7 Higher Level Consideration

The control method introduced before is amongst other things characterized by its simple expandability to higher level systems. Since at higher levels only the number of triangular sectors increases, the SHC method can directly be applied to inverter systems with higher levels. For this purpose a three- and a five-level inverter are considered in this section. For a good comparability most of the system parameters are kept unchanged compared to the parameters used for the two-level simulations. The properties and the



(a) Three-level space vector diagram with load voltage

(b) Five-level space vector diagram with load voltage

Figure 5.24: Three- and Five-level space vector diagram

functionality of inverters with higher levels have already been described in detail in Chapter 2.3.

Figure 5.24 shows the space vector diagrams of a three- and a five-level inverter. Compared to the previously shown space vector diagram of a two-level inverter, it can be seen that the number of triangular sectors increases with the level count. However, for the functional principle of the proposed control method nothing changes because the shape of the sectors is always maintained. After the three surrounding space vectors have been determined with the aid of the coordinate system presented in Chapter 4, the effort is reduced to the simple geometric solution of the previously derived equation.

$$k_{\mathrm{opt}} = \underset{k\in\{1,2,3\}}{\arg\min} \left(\mathrm{Re}\{\underline{u}_{L_{\mathrm{F}}\,\mathrm{e}(k)} \cdot \bar{\underline{i}}_{\mathrm{e}}\} \right). \tag{5.23}$$

5.7.1 Three-Level Inverter System

Figure 5.25 shows the three phase sinusoidal inverter output currents. Analogously to the two-level inverter the current is kept within a specified tolerance band. To ensure comparability the inductive value was halved to

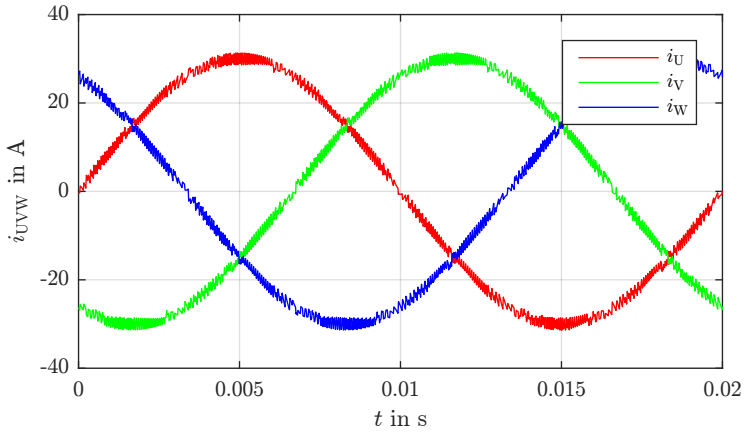


Figure 5.25: Three-level inverter output current

achieve similar switching frequencies at the nominal operating point of the inverter.

Switching Frequency Versus Modulation Index

As with the two-level inverter system the functional principle of the proposed method causes a variation in the switching frequency over the modulation index. As explained before the minimums of the switching frequency are located at points where the reference voltage is close to the inverter output voltages. This is caused by the resulting small voltage across the inductance at these areas.

Unlike two-level inverters, there are two maxima in the plot as shown in Figure 5.26. This behaviour can be explained by comparing the space vector diagrams of the two- and the three-level inverter system. Within the two-level inverter the reference voltage passes only a single triangular sector during its variation. In contrast to that within a three-level system the reference voltage passes two triangular sectors. As the maximum of the switching frequency is located between the edge points of the triangular sectors a three level inverter system generates two maxima. In addition to that Figure 5.26 also shows that the current control method keeps the switching frequency within the three phases almost constant. This simulation has proved that all assumptions made are also applicable to three-level inverter systems. It should be further recognized that in the case of a three-level inverter system the halved inductive element generates a similar switching frequency as shown for the two-level inverter.

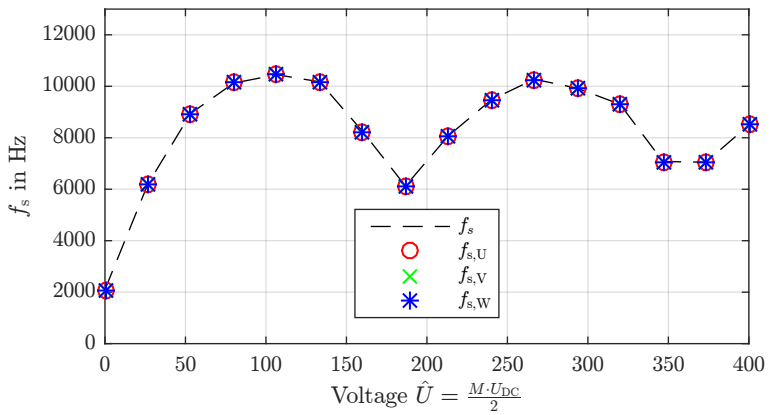
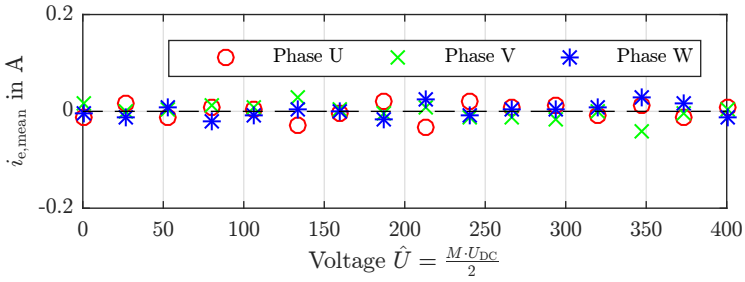


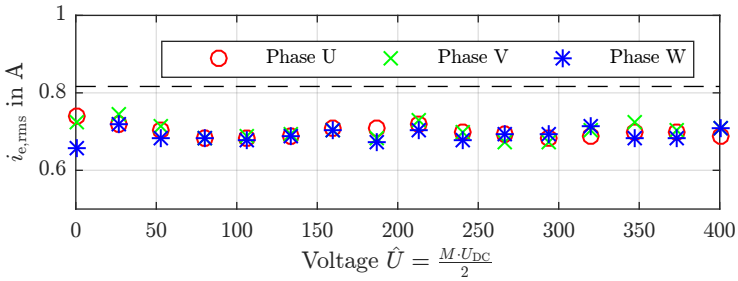
Figure 5.26: Switching frequency versus modulation index

Mean / RMS Value of the Current Error Versus Modulation Index

To complete the examination on the three-level inverter systems the RMS values and the mean values of the current error are plotted over the entire operating range analogously to the two-level inverter simulations. The results are, as expected, equal to that of the two-level inverter since the value of the tolerance band was kept constant.



(a) Mean value of current error versus modulation index



(b) RMS value of current error versus modulation index

Figure 5.27: Mean and RMS value of the current error of a three-level inverter versus modulation index

5.7.2 Five-Level Inverter System

As before the three-phase sinusoidal output currents of a five-level inverter, which are kept within the specified tolerance band, are shown in Figure 5.28. In order to achieve a good comparability, the value of the inductance was quartered in comparison to the inductance value of the two-level inverter simulations. This results in a comparable switching frequency at the nominal operating point of the inverter.

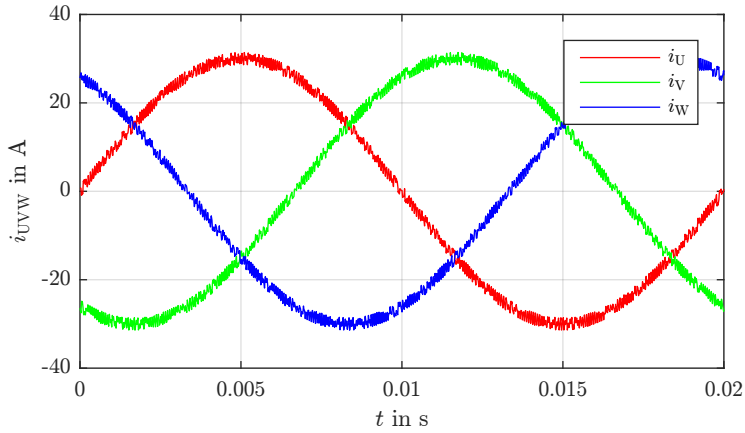


Figure 5.28: Five-level inverter output current

Switching Frequency Versus Modulation Index

As it can be expected, the triangular sectors that are relevant within a five-level inverter system result in 4 maxima in the plot of the switching frequencies versus the modulation index. As before, it can also be observed that the symmetry of the switching frequency is maintained in the three phases (see Fig. 5.29).

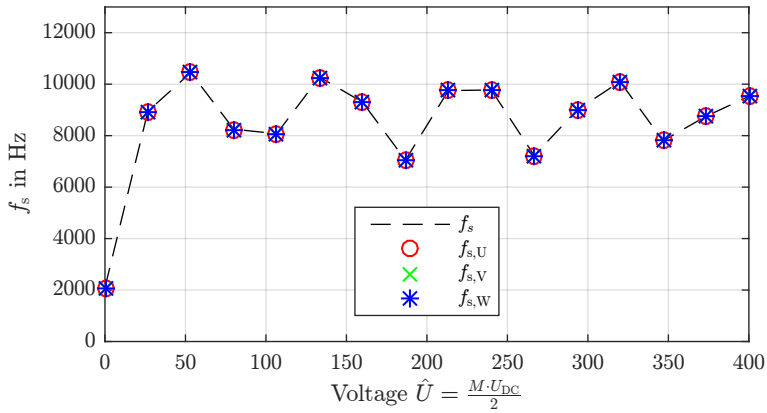
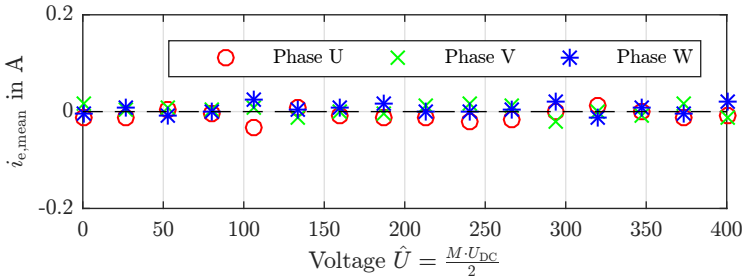


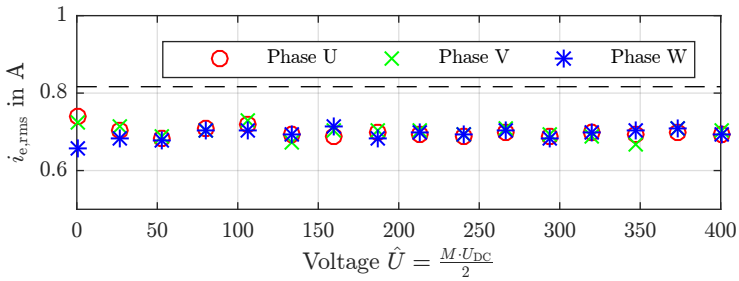
Figure 5.29: Switching frequency versus modulation index

Mean / RMS Value of the Current Error Versus Modulation Index

To complete the examination on the five-level inverter systems the mean values and the RMS values of the current error are plotted over the entire operating range analogously to the two-level inverter simulations. The results show the expected behaviour.



(a) Mean value of the current error versus modulation index



(b) RMS value of the current error versus modulation index

Figure 5.30: Mean and RMS value of the current error of a five-level inverter versus modulation index

5.8 Reference Seeking Algorithm

The SHC method relies on valid informations about the position of reference voltage in the $\alpha\beta$ plane to guarantee a correct sector selection and thus a proper functionality. Using an appropriate reference voltage measurement and synchronization method that determines the sector exactly, the three output states of the inverter used in a triangular sector are sufficient to control the current.

In case of inaccurate or unimplemented reference voltage measurement, fault cases (eg. grid faults) or set-point changes the proposed method is extended in a suitable manner to guarantee robust functionality even under this abnormal conditions. The basic idea of the extension is the fact that as long as the actual sector matches the location of the reference the three adjacent space vectors are able to keep the current error within the tolerance band. However, if one of the four cases occurs, the current error can no longer be reduced with the three surrounding space vectors.

5.8.1 Seeking Cases

Case 1 - Unimplemented Measurement: Case 1 assumes that no measurement is implemented to determine the correct sector of the reference voltage. Based on different initial states this case will occur on initialization and start-up of the inverter system and during operation. Figure 5.31 shows 120° of the space vector diagram of a three-level inverter system. The dashed line shows the trajectory of the reference voltage with its actual location in the sector where the associated vector points to. The actual and falsely selected sector is highlighted and differs from the sector of the reference voltage. This situation would cause an increase in the current error as the three vectors from the "wrong" sector are not able to keep the current error within the tolerance band.

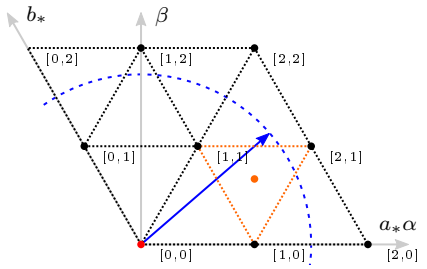


Figure 5.31: Seeking Case 1

Case 2 - Unimplemented Measurement 2: Case 2 is a specific variant of seeking case 1. The difference, as shown in Figure 5.32, is that the magnitude of the actual reference voltage is selected in a way that the trajectory passes the corner point of the triangular sector. It is observable that the actual sector of the reference and the actual selected sector differ from each other.

In contrast to case 1 the actual sector of the reference voltage is not a sector that directly adjoins on the actual selected sector.

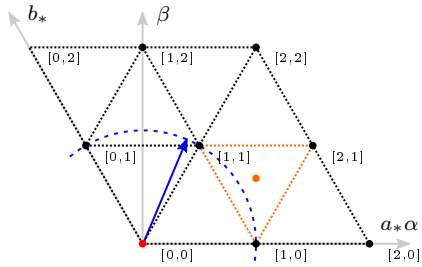


Figure 5.32: Seeking Case 2

Case 3 - Reference Fault: Case 3 assumes that a fault occurs on the reference. Before the fault takes place the actual sector of the reference and the selected sector fit to each other. At an arbitrary point in time a fault occurs causing an abrupt sector change of the reference voltage vector as sketched in Figure 5.33.

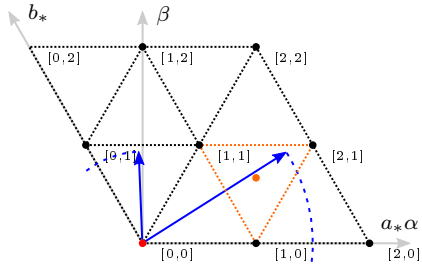


Figure 5.33: Seeking Case 3

Case 4 - Set-Point Change: Application dependent set-point changes can occur at any time. A set-point change will immediately cause a violation of the tolerance bands. As mentioned before the basic SHC controller is able to reduce the current error and to control the current with the three adjacent space vectors. In order to exploit a higher level of dynamics one can select vectors which are not directly adjacent to the reference.

5.8.2 Additional Hysteresis Limit

As introduced in the previous section, Equation 5.9 defines the hysteresis limit $\underline{B}$ which is used to trigger an event to select a new error reducing vector. An additional outer hysteresis limit is defined equally but with a greater magnitude. Therefore, the outer limit is given by:

$$\underline{B}_{\mathrm{o}} = \underline{i}^{*} + \delta_{\mathrm{o}} e^{j\varphi},\ 0 \leq \varphi < 2\pi \tag{5.24}$$

where δ_{o} is the magnitude of the outer hysteresis limit which is defined by

$$\delta_{\mathrm{o}} = \delta + \Delta, \Delta \in \mathbb{R}^{+} \tag{5.25}$$

Figure 5.34 shows all relevant vectors and hysteresis limits within the $\alpha\beta$ coordinate system. In addition to the nominal current and the actual current, the error current and the two tolerance areas are shown. Exceeding the first tolerance band triggers the selection of a new space vector from the actual sector to reduce the current error. However if this does not work the second tolerance band is reached and signals a potential sector error. A sector correction needs to be applied.

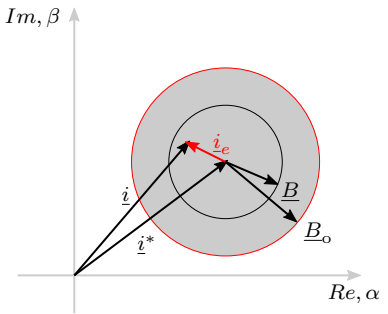


Figure 5.34: Current vectors, error current and tolerance bands

Determining the Size of the Outer Hysteresis Limit

To determine the outer hysteresis limit it must be ensured that, even in extreme cases, the outer limit is reached only if this is caused by the choice of an incorrect sector or a current set-point change. In the actual case of an ideal inverter it is necessary to know that a changeover to the current-reducing vector is carried out immediately and without a time delay. Thus,

ideally, a minimally larger outer tolerance band is sufficient, since the inner limit is only exceeded if a sector is selected which is not correct.

If a non-ideal system is considered, the inner tolerance band is exceeded due to the dead times of the inverter and the delay time of the controller. It must be ensured that the outer tolerance band is not reached by the additional current error caused by these delay times. Correspondingly, the additional current error to be expected must be taken into account when selecting the outer limit. The current rise is essentially determined by the converter output voltage, the reference voltage and the inductance. Assuming a linear and symmetrical load, the current rise can be determined according to the following equation:

$$\frac{\mathrm{d}}{\mathrm{d}t}\underline{i} = \frac{\underline{u}_{L_{\mathrm{F}}\,\mathrm{e}}}{L} = \frac{\underline{U}_{\mathrm{inv}} - \underline{u}}{L} \tag{5.26}$$

Since in the normal case an approximately constant inductance can be assumed, the current rise depends only on the voltage across the inductance. This voltage changes over time and reaches the maximum in a sector of a two-level converter when, for example, the reference voltage is zero and the output voltage of the inverter is at its maximum. For the illustrated scenario of a two-level system, the maximum slope is:

$$\frac{\mathrm{d}}{\mathrm{d}t}\underline{i} = \frac{1}{L} \cdot \frac{2}{3} \cdot U_{\mathrm{DC}} \tag{5.27}$$

By means of the maximum current rise, the additional current error to be expected can be estimated depending on the delay time. By rearranging the equation and considering Equation 5.24, the following can be assumed for the outer limit.

$$\delta_{\mathrm{o}} = \delta + \Delta, \Delta > \frac{2}{3L} U_{\mathrm{DC}} \cdot (t_{\mathrm{delay}}) \tag{5.28}$$

where t_{delay} is the delay time consisting of the delay caused by the inverter dead time and the delay caused by the implementation of the control algorithm.

At higher levels the maximum voltage across the inductor in a triangular sector becomes smaller compared to a two-level inverter. Depending on the level number, the magnitude of the outer limit can be determined as follows:

$$\delta_{\mathrm{o}} = \delta + \Delta, \Delta > \frac{2}{3L \cdot (n-1)} U_{\mathrm{DC}} \cdot (t_{\mathrm{delay}}) \tag{5.29}$$

where n is defined to be the level count of the inverter.

5.8.3 Selection of Next Sector

Similar to the selection process for the current error reducing vector the selection of the next sector is triggered by a violation of the outer hysteresis band. The method uses the midpoint of the actual sector, the midpoints of the neighbouring sectors and the current error to determine the next sector which can be used to keep the current within the tolerance band. Figure 5.35 shows a extract of a three-level space vector diagram. As the four highlighted triangular sectors are a subset of a space vector diagram for level numbers above three, they allow a derivation of the selection method in general manner. For two-level inverters the principle can be transferred with the restriction that there exist only six triangular sectors within the space vector diagram from which a maximum of two are directly neighbouring the actual sector.

As the proposed concept uses a voltage reference to determine the actual sector a pseudo-voltage $\underline{U}_{\text{pseudo}}$ which is arbitrarily set to be the centre point of the triangular sector, is generated. This pseudo-voltage is used as a reference voltage for determining the current error reducing vector. As long as the sector of the real reference voltage and the sector of the pseudo-voltage match a vector from that sector that keeps the current error within the specified tolerance band will be selected.

Assuming that the actual triangular sector chosen for control is not correct the selected output vector could lead to an error that increases. As the SHC method without extensions triggers the selection of a new output vector only

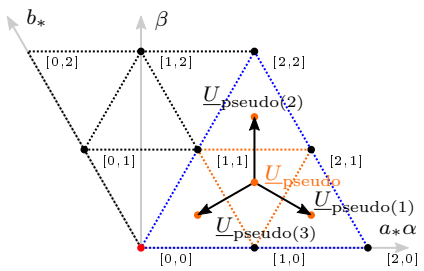


Figure 5.35: Extract of three-level space vector diagram

when the inner tolerance band is touched, this would lead to an instability. This problem is solved using an additional criterion (outer tolerance band) that generates a correction of the actual pseudo-voltage and thus a correction of the chosen triangle used for control. Based on the knowledge of the actual pseudo-reference voltage located in the centre point of the actual sector the midpoints of the surrounding triangular sectors can easily be determined. Using the a_*b_* coordinate system derived in Chapter 4.4, the midpoint coordinates within the actual sector highlighted in Figure 5.35 is determined by adding $(\frac{1}{3}, \frac{2}{3})$ to the base vector $(1, 0)$ of this sector. This coordinates now serves as the origin for the vectors pointing to the centre points of the neighbouring sectors. The endpoints can then simply be calculated by adding $(\frac{1}{3}, -\frac{1}{3})$ for $\underline{U}_{\text{pseudo}(1)}$, $(\frac{1}{3}, \frac{2}{3})$ for $\underline{U}_{\text{pseudo}(2)}$ and $(-\frac{2}{3}, -\frac{1}{3})$ for $\underline{U}_{\text{pseudo}(3)}$ to the actual midpoint. The resulting neighbouring pseudo-reference voltages are denoted by

$$\underline{U}_{\text{pseudo}(k)}, \;\; k = 1, 2, 3 \tag{5.30}$$

Figure 5.36 shows the combined figure of the space vector diagram and the current error as it was presented in the derivation of the basic SHC method. The origin of the coordinate system of the current error is at the tip of the actual reference voltage vector (in this case the actual pseudo-voltage). Furthermore, the tolerance band and the additional outer tolerance band are shown. It is sketched that the current error touches the inner tolerance band. This tolerance band violation chooses a new vector which is not able to reduce the current error causing a further increase and thus a violation of the outer hysteresis band. This violation triggers a calculation that is able to select the one of the three neighbouring pseudo voltages $\underline{U}_{\text{pseudo}(k)}$ that best opposes the current error. The apparent similarities to the selection of the current error reducing vector enable to use the same approach. Summarised, the answer to the problem can be simplified to a solution of a slightly adapted equation of 5.18. The equation changes to:

$$k_{\text{opt}} = \underset{k \in \{1,2,3\}}{\arg\min} \left(\text{Re}\{\underline{U}_{\text{pseudo}(k)} \cdot \bar{\underline{i}}_{\text{e}}\} \right). \tag{5.31}$$

Determining and using the minimum of the three dot products identifies the one pseudo reference voltage best opposing the current error. After finding the minimum the actual pseudo-reference voltage and consequently its corresponding triangle is changed and used to select an error reducing vector that keeps the current error within the tolerance band.

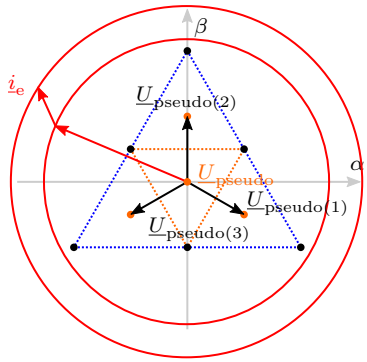
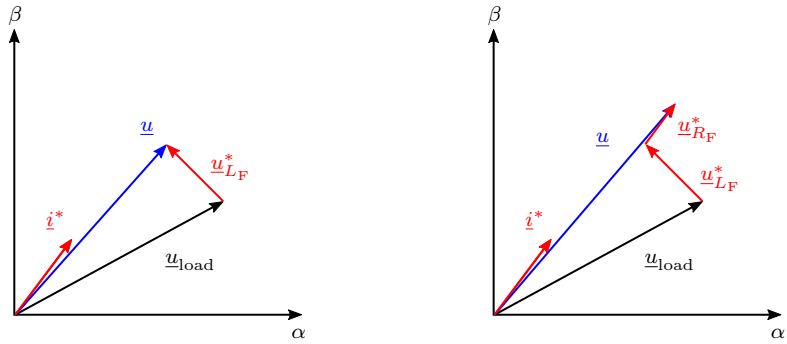


Figure 5.36: Geometrical representation of all voltage and current vectors needed for the selection of the next sector

5.8.4 Negligibility of the Ohmic Component

The seeking algorithm derived, shows that an accurate knowledge of the load is not absolutely necessary for robust operation and controllability. The estimation of whether the reference voltage is in the actual sector can be predicted by the trajectory of the current error. If the real reference voltage is in a deviating sector, the current error increases. As soon as the outer tolerance band is reached, a new sector is chosen by the seeking algorithm.

In the derivation of the SHC algorithm it was assumed, that the reference voltage $\underline{u}$ and thus the actual sector is exactly known. In the definition of this reference voltage in Section 3.3, the ohmic component was omitted since its influence is comparatively small. When the ohmic component is considered, the phase and amplitude error of the reference voltage to the load voltage varies current-dependent to the consideration of only the inductive element as shown in Figure 5.37. Since the seeking algorithm operates with a pseudo reference voltage which is located in the centre of a triangular sector at any time, the exact position of the reference voltage $\underline{u}$ for determining the current error reducing space vector is not mandatory. This also confirms the possibility of neglecting the ohmic component even for unrealistically high values.



(a) Space vector representation of averaged inverter output voltage $\underline{u}$ without ohmic component

(b) Space vector representation of averaged inverter output voltage $\underline{u}$ with ohmic component $\underline{u}^*_{R_\mathrm{F}}$

Figure 5.37: Averaged inverter output voltage $\underline{u}$

5.8.5 Summary of the SHC Concept with Reference Seeking Algorithm

In the previous sections the concept of the SHC controller and the reference seeking algorithm were basically derived. The concept and the structure is summarized on the basis of a converter system as schematically shown in Figure 5.38.

As before, the current error reducing space vector is determined from the current error after a trigger event (see Section 5.4.1). In the basic derivation of the SHC algorithm it was assumed that the exact position of the reference voltage is known. Using the reference seeking algorithm, the position of the reference voltage is estimated. As soon as an error in the estimated position is detected, a correction of the pseudo reference voltage is performed (see Section 5.8.3). The output voltages are determined from the pseudo reference voltage and the simplification algorithm (see Section 4.5).

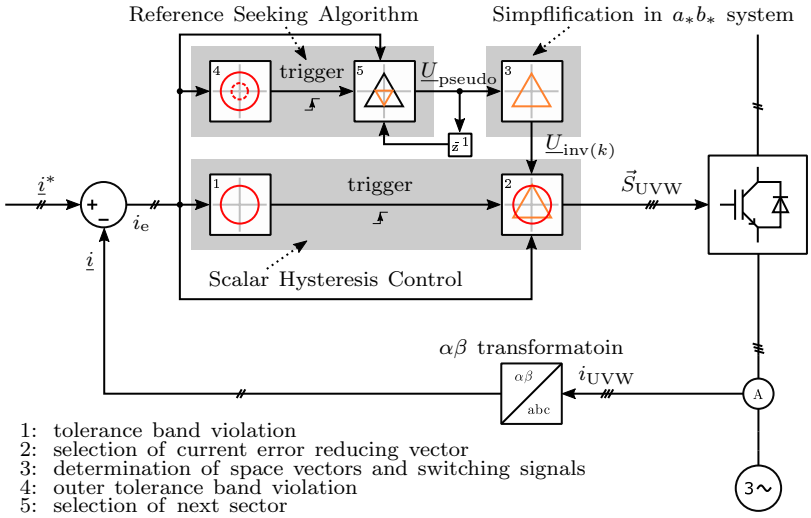


Figure 5.38: Basic concept and overview of the SHC controller

5.8.6 Simulations, Characteristics and Evaluation Criteria

To be able to cover all of the defined seeking cases the simulations are carried out using an ideal three-level inverter system. As before, no dead-times and losses are implemented to prove the theoretical considerations. In contrast to the simulative verification of the SHC method, the reference voltage $\underline{u}$ is assumed to be unknown. Instead, the pseudo-reference voltage is used which is set to be the midpoint of the actual sector. To enable comparability the system parameters were kept equal and an additional outer tolerance band was introduced.

Figure 5.39 shows the three-phase sinusoidal output currents of the inverter. The resulting squared absolute value of the current error is shown in Figure 5.40. As shown, the hysteresis bands were set to $\delta = \sqrt{2}$ for the inner and $\delta_o = \sqrt{4}$ for the outer limits. On closer inspection of the figure one can see that the outer hysteresis band is reached 18 times within a period. This value can be justified as the point of operation is in the outer area of the space vector diagram causing the reference voltage to pass 18 triangular sectors and thus needs at least 18 triggering points that cause a correction of the correct triangle via the pseudo reference voltages. The deviation between the pseudo-reference voltage, which is set to the midpoint of the triangular sectors, and the real reference voltage within is shown in Figure 5.41. It is apparent that the pseudo-reference voltage, which is used as input for the proposed control method, does not exactly match to the real reference volt-

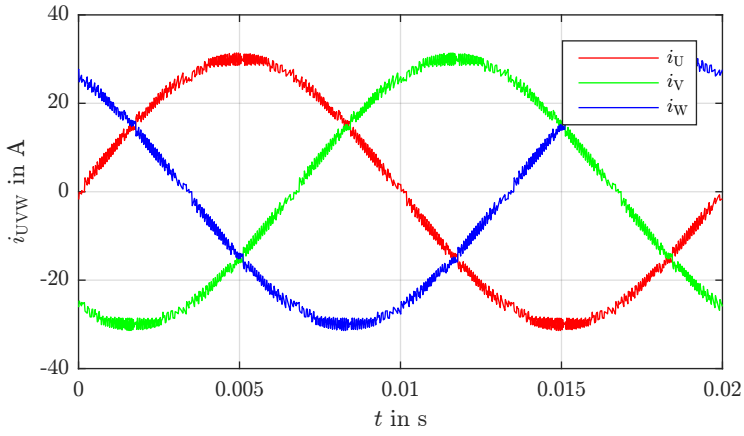


Figure 5.39: Inverter output current

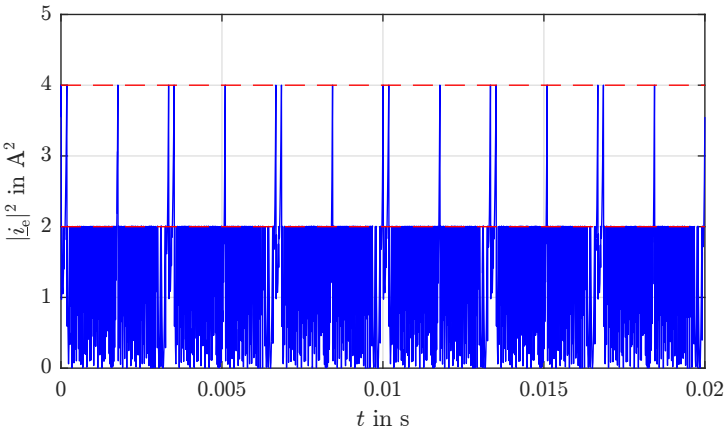


Figure 5.40: Squared absolute value of the current error

age. However, this characteristic does not have important negative effects on the control method when considering an ideal inverter system. As soon as the current error cannot be reduced any more, the outer hysteresis band is touched and the correction of the pseudo-reference voltage is carried out.

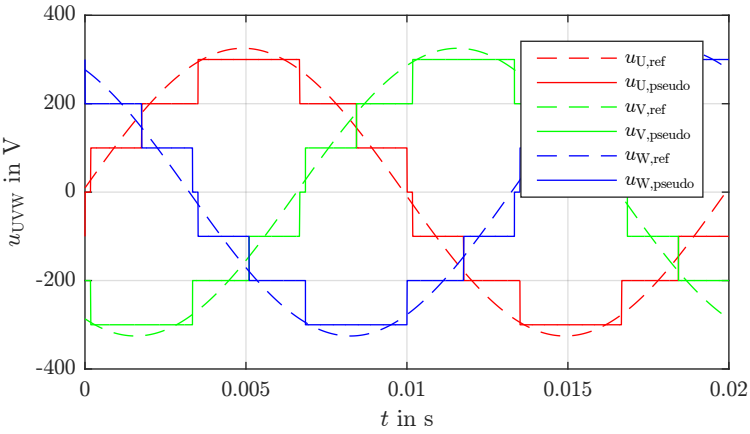
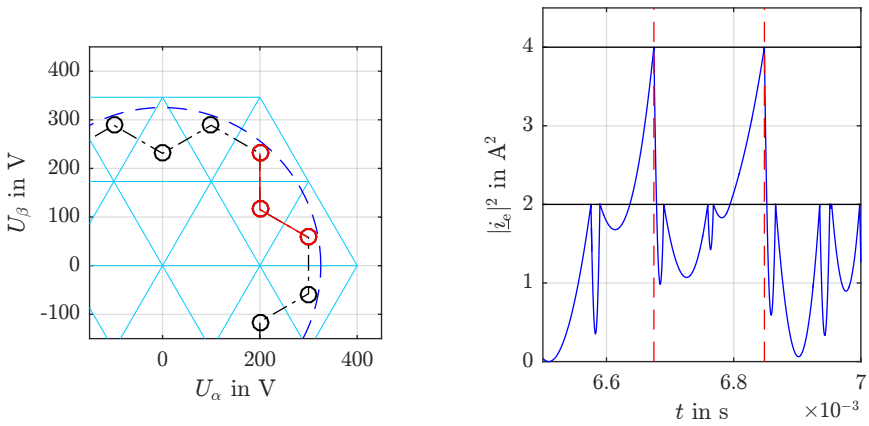


Figure 5.41: Three-phase pseudo reference voltage

Case 1: Unimplemented Measurement

The first seeking case was defined in Figure 5.31. The nominal operating point for a grid connected inverter system is assumed. The seeking algorithm has to recognize if the real value of the reference voltage is not in the actual sector and thus has to readjust the sector. Figure 5.42 shows a time segment of the pseudo-reference voltage in $\alpha\beta$ (Fig. 5.42a) and the corresponding value of the current error (Fig. 5.42b). The time segment includes three different zones related to two sector changes. As one can see the outer tolerance band is touched twice from which it can be deduced that two adjustments of the pseudo reference voltage take place. Furthermore, it can be seen that within the three zones the controllability with only three adjacent space vectors is guaranteed. Figure 5.42a shows an extract of the three-level space vector diagram. The dashed line corresponds to the real reference voltage whereas the circles specify the pseudo reference voltages of the sector. The red circular pseudo reference points correspond to the specific time segment.

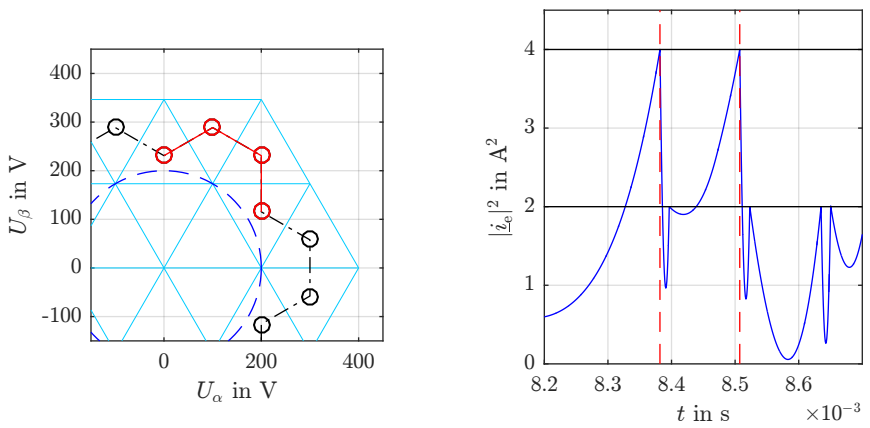


(a) Pseudo reference voltage in $\alpha\beta$ plane (b) Squared absolute value of the current error

Figure 5.42: Time segment with the three sectors (red) and two sector changes caused by the violation of the outer tolerance band for seeking case 1

Case 2: Unimplemented Measurement 2

The second case is characterized by the property that the reference voltage precisely intersects the corner points of the inner hexagon. As shown in Figure 5.43a, in a 120° sector of the space vector diagram, two triangular sectors are traversed by the reference voltage. As the seeking algorithm uses only the three neighbouring triangular sectors of the actual triangle, at least three sector changes are necessary to reach the correct sector. Figure 5.43b shows the value of the current error with the specified tolerance bands. Each time the outer hysteresis band is reached a sector change occurs. In this figure it seems that the outer tolerance band is reached only twice what, in fact, is not correct. The simulations were carried out using an ideal inverter system with no dead-times and losses. As soon as the outer hysteresis band is touched, a first sector change occurs. As the next sector is still wrong the current is still increasing which leads to an immediate additional change (no time delay) of the sector. The space vector which is selected in the second zone reduces the current error for a moment. As the pseudo reference voltage and the actual reference voltage are not in the same sector, another sector change is triggered leading to the third sector change which is finally correct.

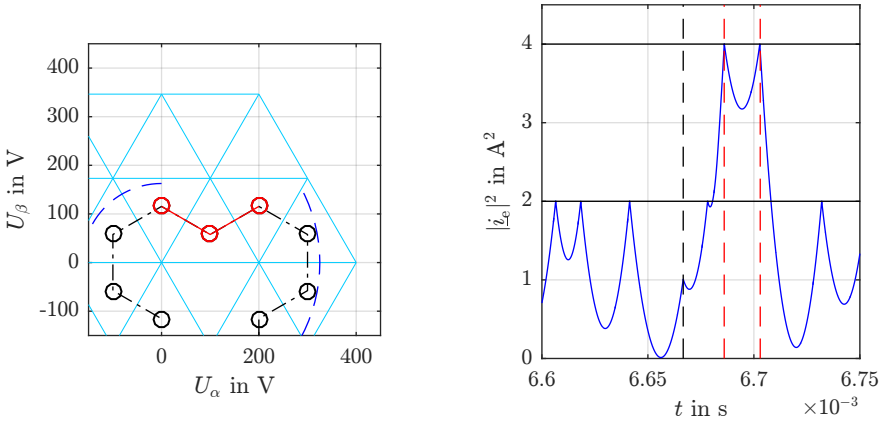


(a) Pseudo reference voltage in $\alpha\beta$ plane (b) Squared absolute value of the current error

Figure 5.43: Time segment for seeking case 2

Case 3: Reference Fault

Within this test case an amplitude and a phase fault were assumed. Until t_1 the amplitude was set to a value of $\hat{U}_{\text{load}} = 325$ V. After that the amplitude was halved and a phase shift of 60° was added. Figure 5.44a shows the corresponding segment of the space vector diagram. It is apparent that two sector changes are needed to find the correct location of the reference voltage. In Figure 5.44b the current error shows that the outer hysteresis limit is reached twice resulting in two sector changes. After those changes the algorithms shows the same behaviour as before.



(a) Pseudo reference voltage in $\alpha\beta$ plane (b) Squared absolute value of the current error

Figure 5.44: Time segment for seeking case 3

Case 4: Set-Point Change

The set-point change can be assumed as a special case for the seeking algorithm. The first three cases described an inaccuracy (unimplemented measurement), a special operating point or a reference fault of the corresponding reference voltage. Each of those cases used the outer tolerance band to correct the pseudo reference voltage in a way that the newly chosen sector matches the sector of the real reference voltage.

A change of the set-point value causes a violation of the outer tolerance band leading to a trigger event that corrects the pseudo-reference voltage as

explained before. Although the sector of the reference voltage is correct in the case of a set-point change, the proposed algorithm can be used to achieve a higher dynamic. After the set-point change occurs, the outer hysteresis band is reached and the seeking algorithm searches and finally can find the correct sector. This causes the current error to decrease and the actual current to reach the new set-point as shown in Figure 5.45.

Figure 5.46 shows the corresponding space vector diagram. The reference voltage was set to be within the inner hexagon of the space vector diagram and the outer hysteresis band was used to determine the location. At a specific point in time a set-point change was activated leading to a correction of the reference voltage. The red path shows the additional triangular sectors used to reduce the current error. As the new set-point is reached after 0.3 ms the sector of the reference voltage before and after the set-point change is identical. Thus, the path of the seeking algorithm starts and ends in the same sector.

The behaviour in the case of a set-point change can be further optimized. As it is very simple to detect a set-point change, this information could be used to jump into a sector that includes the one output voltage decreasing the current error as fast as possible. After the set-point is reached the sector is directly switched back to the one including the reference voltage.

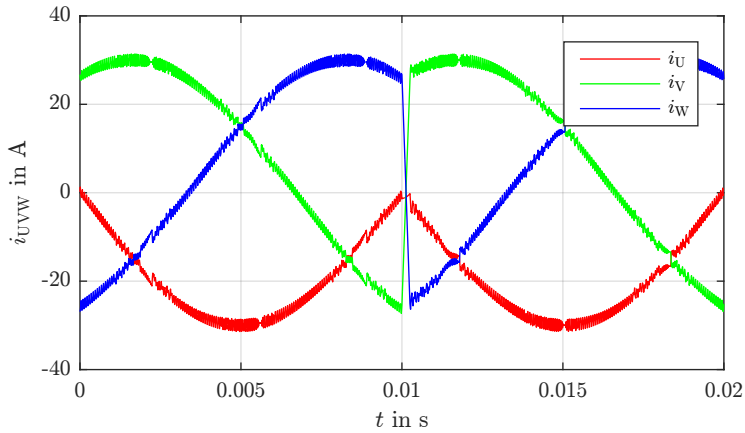


Figure 5.45: Three phase current with set-point change

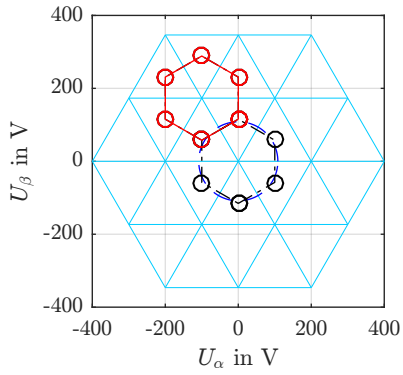


Figure 5.46: Pseudo reference voltage in $\alpha\beta$ plane for seeking case 4

5.8.7 Advanced Seeking Algorithm

A future sector change is already indicated before it really happens by a defined switching behaviour, frequent triggers or a specific current waveform. These informations can be used to optimize the sector change.

- First Possibility: In the case of the ideal system shown here, the outer limit could be defined to be minimally larger than the inner hysteresis band. Using this, a hysteresis violation of the outer tolerance band would be detected very quickly causing a fast correction of the sector. In a real system, this methodology is not suitable due to various boundary conditions.
- Second Possibility: Detecting switching operations with a very small or no effect. The theory of the controller states that after a switching operation the error should drop. If this is not the case and the current error is still rising or not noticeable decreasing it could be assumed that a wrong sector is active.

Since the first possibility can only be used with ideal inverter systems, the implementation of the second possibility is explained briefly. After a trigger, a switching operation is carried out via the algorithm described in this chapter. It redirects the current error and thus brings it back into the tolerance band. But if the error still increases, a sector change must occur. The implementation is carried out by monitoring the slope of the magnitude

of the current error. If a rising current error is detected according to the following mathematical relationship:

$$|\underline{i}_{\mathrm{e}}(t_0)| < |\underline{i}_{\mathrm{e}}(t_0 + \Delta t)| \tag{5.32}$$

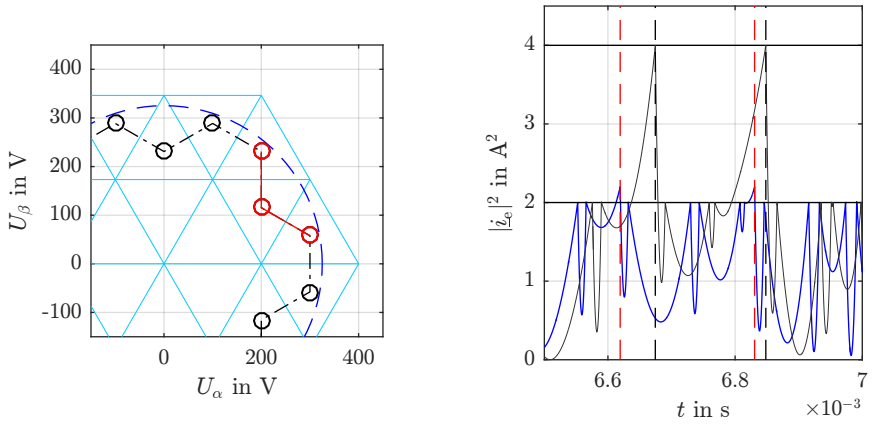
a correction of the sector can be carried out already before the outer boundary is reached.

The methodology described here can be applied to real systems which can lead to a noticeable improvement. Since additional problems like noise or other disturbances can still occur in real systems the outer tolerance band guarantees an absolutely robust operation.

Comparison of Seeking Case 1

Seeking Case 1 correspond to the scenario of a non-implemented or defective voltage measurement. To show the difference of the seeking and the advanced seeking algorithm, that evaluates the switching behaviour and the slope of the current error, an additional simulation of seeking case 1 was carried out.

The time segment used for a detailed comparison of the pseudo-reference voltage in the $\alpha\beta$ plane is shown in Figure 5.47. As apparent in the space



(a) Pseudo reference voltage in $\alpha\beta$ plane (b) Squared absolute value of the current error

Figure 5.47: Time segment with sector change of standard (black) and advanced (blue) seeking algorithm

vector diagram there are three sectors corresponding to that time interval resulting in two necessary sector changes. As one can see in Figure 5.47a the normal implementation of the seeking algorithm causes a current error that touches the outer hysteresis band twice which corresponds to two sector changes. Additionally, the improvement of the advanced seeking algorithm is shown in Figure 5.47b. There is also a greater current error, but not as large as for the standard implementation. The magnitude of the possible overshoot over the inner tolerance band depends on multiple parameters. Those parameters could be block- and dead-times, calculation times, quality and dynamics of current measurement and system parameters like the filter inductance.

5.9 Summary of Scalar Hysteresis Control

The previous chapter presented the main contribution of this thesis. The derivation, the mathematical and geometrical idea and the working behaviour were derived and demonstrated with the help of simulations on an ideal system. Initially, the new direct current control method was derived and the working behaviour was shown using one triangular sector. The independence from the level number was represented by simulations of a two-, three- and five-level inverter. The advantages in terms of the symmetrical switching frequency have been demonstrated by suitable simulations.

In order to prove the robustness even in the case of inaccurate or non-existent measurements, faults in the reference voltage and set-point changes different cases for a seeking algorithm have been defined. The presented algorithm allows the direct current control method to work even in the defined seeking cases according to the intended purpose. The seeking algorithm therefore estimates the position of the reference voltage. In addition, a higher dynamic performance is achieved by the seeking algorithm in the case of prompt set-point changes.

An advanced implementation of the seeking algorithm showed further improvements.

In summary one can say that a new direct current control algorithm which shows excellent properties in terms of

- simplicity
- robustness
- dynamics

- independence on the level count
- independence on the hardware topology

has been developed. The new direct current control algorithm is called "***S**calar **H**ysteresis **C**ontrol - **SHC***"

Chapter 6

Simulations and Experimental Verification

This chapter focuses on the realistic implementation and simulation as well on the experimental verification of the SHC method derived in Chapter 5. In reality additional side effects can have a detrimental effect on the control method. They need to be considered for a real implementation. The following effects may occur:

- Inaccuracies in the measurements for currents and voltages.
- Delays caused by the algorithms in the microprocessor or FPGA.
- Dead-times of the inverter.

In order to achieve the best possible comparability with the experimental verification, side effects, such as dead times, are also implemented within the simulation environment. The design of the entire inverter system was carried out in the MATLAB / SIMULINK environment, which on the one hand side allow realistic simulations to be carried out and, on the other hand, provides direct code generation capabilities for various platforms. To simulate the hardware components the Simscape Toolbox, specifically the SimPowerSystems package, was used.

The main simulations and the verification are initially carried out using a three-level inverter system as it was used in the derivation of the the proposed direct current control method. To show and verify the generic approach experimental results for a two- and five-level inverter system are also shown.

6.1 Simulation Results

To guarantee more realistic results than in the ideal simulation, hardware specific properties are implemented in the simulation model. The main effects

on the working behaviour correspond to the dead-times, to properties of the current measurement and to hardware topology related control needs. Therefore the following adaptations are added to the ideal simulation model:

1. **Dead-Time:** The dead-time of the inverter is introduced to ensure that no short-circuit and no forbidden switching states are generated. Before a switching operation is initiated a state-machine ensures that a new IGBT is not switched on before the switch off operation is completed.
2. **Block-Time:** After a switching operation the current and thus the current error, show an oscillation due to the various system capacitances. To avoid misinterpretations and thus unnecessary switching operations a block-time after the dead-time is introduced. This time blocks the current controller for a defined time. Those oscillation only appear within the real measurements as the relevant capacitances are not modelled within the realistic simulation environment.
3. **DC-link Balancing:** As a three-level NPC inverter is used to verify the concept, the DC-link unbalance needs to be taken into account. The balancing algorithm uses redundant switching states of the inverter. They can produce more switching operations during the selection of a new space vector. This could lead to additional delay times causing a slightly different working behaviour.
4. **FPGA Delay Times:** The control algorithm is based on various computing operations and comparisons carried out in an FPGA. It selects a particular switching operation, according to the SHC method, from different input variables. These operations as well as various filter mechanisms require computation time which adds up to a total delay time in the FPGA.

6.1.1 Dead-Time Generation

As is usual with all inverter systems, dead-times must be implemented when performing a switching event. When a new output state is requested one IGBT is turned off. Before the next IGBT is turned on, a certain time must be awaited.

In the case of converters with higher level numbers, this switching operation becomes increasingly complex and may generate several transition states before the new output state is reached. To show an example of the working behaviour of the dead-time generation state-machine, a three-level inverter

Table 6.1: Transitions to reach a specific final state for a three-level inverter system

	Final State		
Initial State	S_1	S_0	S_{-1}
S_1	–	T_1	T_1, T_2
S_0	T_1	–	T_2
S_{-1}	T_2, T_1	T_2	–

is considered. Table 6.1 shows the transition table of a three-level inverter. Starting at one of the three possible output states, it requires one or more transition states to reach the final state. After each of the transition states one dead-time unit must be observed. As highlighted in Figure 6.1 In the case of a switching operation from State S_1 to S_{-1} two dead-time units must be considered.

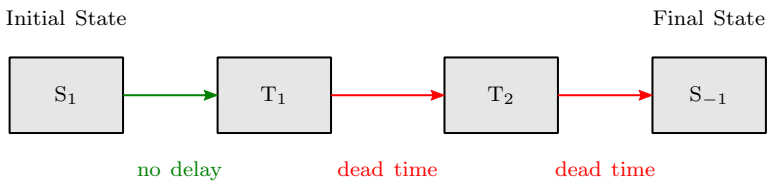


Figure 6.1: Transition example from initial State S_1 to final S_{-1}

Table 6.2 shows the meaning of the main inverter states S_x and the transition states T_x in terms of switches (IGBTs). The top IGBT of a phase within a three-level inverter corresponds to the MSB whereas the bottom IGBT corresponds to the LSB.

During the transition states, the current, and thus the current error, moves depending on its sign. This behaviour will affect the actual value of the current in a way that could be helpful or harmful.

Appendix B shows the state and transition table of a five-level inverter. The stateflow diagram which was implemented for the following simulations and measurements is also shown in Appendix B. Since the switch count of a two- and three-level inverter is a subset of the five-level inverter, the presented state machine can be used for all hardware variants.

Table 6.2: State and transition table of a three-level NPC inverter

S_x, T_x	Switched IGBTs (top to bottom)
S_1	11 00
S_0	01 10
S_{-1}	00 11
T_1	01 00
T_2	00 10

6.1.2 Block-Time

As summarised above, oscillations occur on the current, and thus on the current error, after a switching operations took place. Figure 6.2 shows a measurement of the current error during a switching operation. The oscillation, caused by the system capacitances, is apparent and needs some time to be damped. In addition to the dead-time, an additionally specified time (block-time) must be observed before the SHC algorithm can be activated to react to violations of the hysteresis band in order to detect whether the current error increases or not.

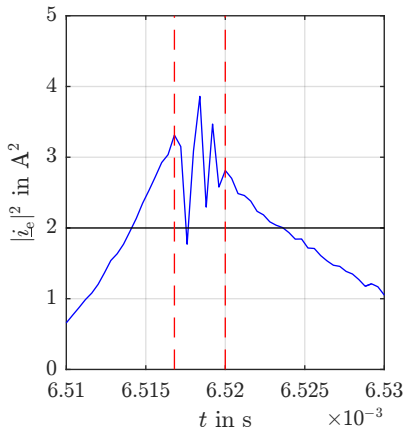


Figure 6.2: Oscillation of the current error and time segment in which the current controller should be de-activated

6.1.3 DC-Link Balancing

Using the diode-clamped inverter topology with the DC-link mid point connected, an imbalance of the DC-link capacitor voltages can occur due to the choice of switching states. Since multiple switching vectors can produce the same output voltage but with complementary effects on the DC-link capacitor voltage, a DC-link balancing algorithm can be applied. A balancing strategy which is based on the minimum stored energy of the capacitors for a back-to-back five-level HVDC converter system was proposed in [32].

To demonstrate the easy adaptability to higher level converters an algorithm for an n-level diode-clamped inverter with $n-1$ DC-link capacitors was derived. The derivation of the following equations is shown in Appendix A. For a controller with bounded DC capacitor voltages, no change is required in energy on average over time

$$\langle \frac{d}{dt} E_C \rangle \leq 0. \tag{6.1}$$

The change in energy $\frac{d}{dt}E_C$ is defined by

$$\frac{d}{dt} E_C = -\frac{1}{2} \sum_{p,q} \Delta U_{C,q} I_p \operatorname{sgn}(m_p - q). \tag{6.2}$$

where p is related to the phase, q denotes the capacitor C_q, $\Delta U_{C,q}$ is the capacitor voltage deviation, I_p is the current (positive current out of the inverter) on phase p and m_p is the switching state of on phase p.

To drive the capacitors towards the balanced state, Expression 6.2 needs to be calculated for each switching state that produces the output voltage selected by the current controller. This selects the inverter state that maximizes the rate of decrease of the asymmetry and thus keeps the DC-link capacitors in a balanced state. The selection of such a redundant switching state will sometimes cause the algorithm to switch an output state that needs two transitions. Therefore, as explained above, a waiting time of more than one dead-time might occur before the final state is reached.

6.1.4 FPGA Delay Times

In order to obtain comparable and realistic simulation results, all delay times generated by the control algorithm, which are generated in the FPGA by different computational operations, must be simulated. These delay times

influence the behaviour and can lead to irregularities if not considered properly. Furthermore, an exact timing must be ensured so that interdependent computing operations can be carried out with the correct inputs.

Gradient Detection

An important function implemented within the FPGA is the gradient detection of the current error. Since in reality signals are only available in noisy form, unwanted inaccuracies may occur. In order to keep these inaccuracies as low as possible, a moving average filter is additionally implemented. This type of filter simply averages the actual value of the measured current with a defined subset of previous measured values at every step in time.

6.1.5 Simulations, Characteristics and Evaluation Criteria

As the simulations are carried out using more realistic parameters they were set according to the following table. From here, on the basis of the previous

Table 6.3: Main Simulation Parameters

Paramter	Value
Grid voltage	$0 \rightarrow 400$ V(50 Hz)
Filter inductance	1.0 mH
DC-link voltage	600 V
Set current $\hat{I}$	20 A
Inner hysteresis δ	$\sqrt{2}$ A
Outer hysteresis δ_o	$\sqrt{16}$ A
Inverter dead-time	3 μs
Inverter block-time	3 μs

results, only the advanced seeking algorithm is used. The violation of the outer tolerance band should therefore only occur during set-point jumps and if the advanced seeking algorithm is not able to detect an upcoming sector change.

General Functionality and Generic Structure of the Algorithm

In order to show the general functionality and the generic structure of the control algorithm, the nominal point is assumed for a two-, three- and five-

level inverter. The system parameters have been set according to Table 6.3, resulting in different switching frequencies due to the constant values for the hysteresis limits and the inductance. Generally, one can say that the higher the number of levels, the lower is the switching frequency with constant parameters.

Figure 6.3 shows three periods of the direct controlled current value. The individual periods result from the control of a two- (first period), three- (second period) and five-level (third period) converter. As mentioned above, the switching frequency decreases as the number of levels increases, which is clearly recognizable.

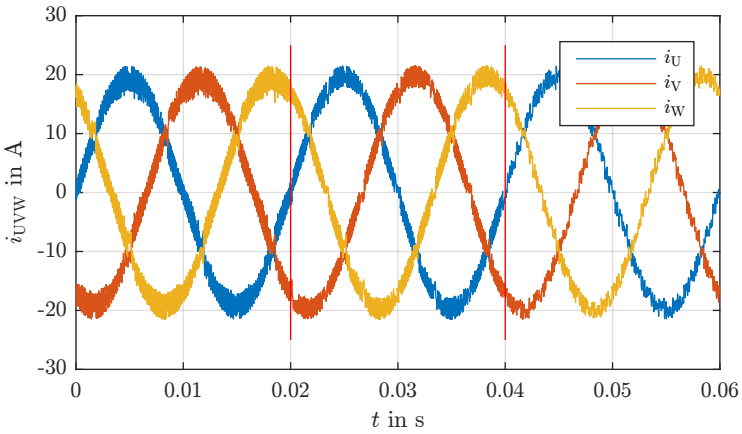


Figure 6.3: Inverter output currents of a two-, three- and five-level inverter

An advantage of converters with higher levels is the increased count of output voltages. Figure 6.4 shows the pseudo reference voltages as presented in Chapter 5. It can be seen that the number of voltage levels of a two-level inverter is 3 and rises to 15 with a five-level inverter. In this case, smaller voltage steps cause a smaller voltage across the inductance, which in turn results in smaller current rises. This fact could, for example, be used to reduce the size of the passive filter components.

The simulation results listed above show that the new direct current control method is capable of operating with inverters of different topologies and levels. For the different simulations, only the level parameter was varied, which is a proof of the generic approach. As the main inductive element is kept constant the squared absolute value of the current error exhibits a very different behaviour as it is shown in Figure 6.5.

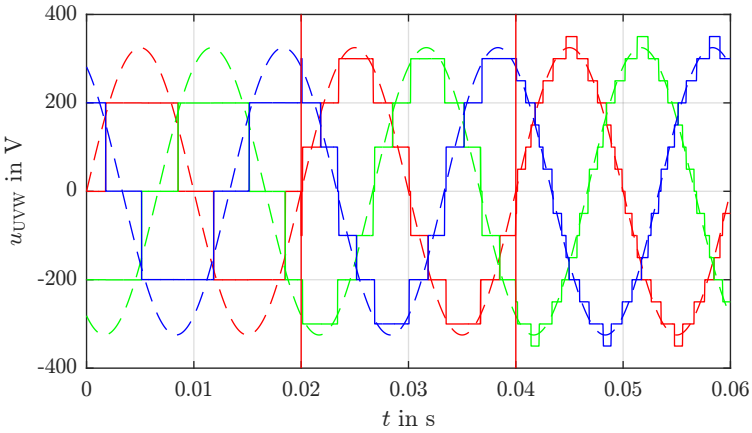


Figure 6.4: Pseudo reference voltage of a two-, three- and five-level inverter

Based on the small inductance and the resulting larger gradient of the current in the case of a two-level converter, the inner tolerance band and the outer tolerance band are exceeded several times. Nevertheless, the squared absolute value of the current error never rises above the value of $|\underline{i}_e|^2 = 25\ \mathrm{A}^2$. The overshoots are caused by the small inductance and the dead- and blocking times of the inverter.

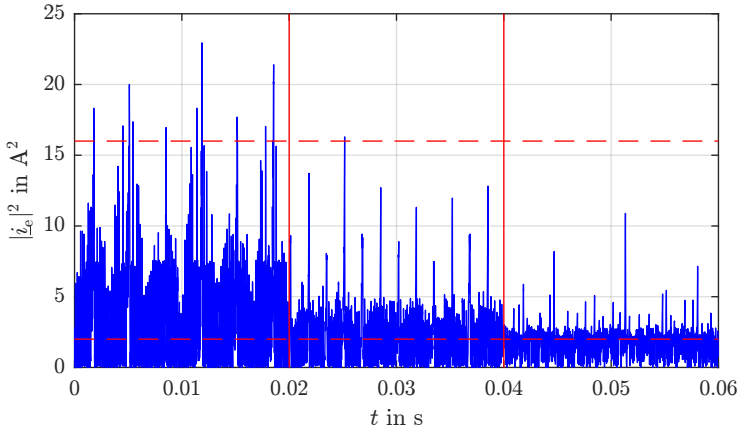


Figure 6.5: Squared absolute value of the current error of a two-, three- and five-level inverter system

Evaluation of a Switching Event

As mentioned above, in the more realistic simulation, effects such as delay times in the FPGA and dead times are considered. These times lead to a further increase in the current error after the violation of the tolerance band occurred. The speed with which the current error increases depends on the switched output voltage of the inverter and the inductance in the system.

To demonstrate the behaviour, Figure 6.6 shows a time section with several switching operations of a three-level inverter. The inner tolerance band is shown in dashed red. At time t_1, the tolerance band is touched and thus a switching operation is initiated. After a delay time caused by the FPGA, the state-machine is executed. Immediately after that, one of the intermediate states is applied which, depending on the sign of the current in the phases, has a positive or negative effect on the trajectory of the current error. After a time $\Delta t = t_2 - t_1$, the new switching state is applied and the current error is reduced. It can be seen that from the violation of the tolerance band until the new output voltage shows an effect, $\Delta t = 4.4\ \mu$s elapse. In this case, the current error is increased by further $\approx 0.9\ \mathrm{A}^2$ above the inner tolerance band. This fact must be taken into account when defining the tolerance bands.

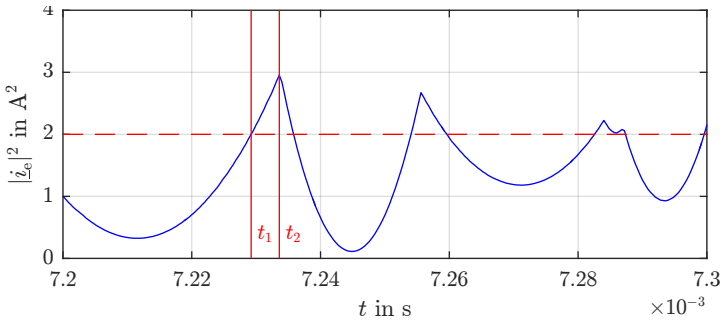


Figure 6.6: Time section of the squared absolute value of the current error

Knowing that the dead time of the inverter is $t_{\mathrm{dead}} = 3\mu$s and using the total time until the switching event is performed one can use the following equation to calculate the delay t_{FPGA} caused by the FPGA.

$$\Delta t = t_{\mathrm{dead}} + t_{\mathrm{FPGA}} \tag{6.3}$$

Reshaping and inserting results in

$$t_{\mathrm{FPGA}} = \Delta t - t_{\mathrm{dead}} = 4.4\mu\mathrm{s} - 3\mu\mathrm{s} = 1.4\mu\mathrm{s} \tag{6.4}$$

DC-link Balancing of the Three-Level NPC Inverter

The main contribution of this thesis is the direct current control algorithm presented in the previous chapter. Depending on the application and the topology used, however, additional control parameters must be considered. Since the NPC topology has been selected as the hardware for the three-level inverter, the interaction and functionality of the new control method can be tested and verified with a balancing algorithm, that is mandatory for NPC inverter systems. Figure 6.7 shows the two DC-link voltages of the three-level inverter. At time t_1, an offset of 5 V was added to the voltage U_{DC2}, which corresponds to an asymmetry in the DC-link. After the offset has reached its final value, the offset was removed. As it can be seen the voltages return to a balanced state due to the implemented balancing algorithm. The speed until the symmetry is reached depends mainly on the size of the DC-link capacitors, the phase current and the modulation index.

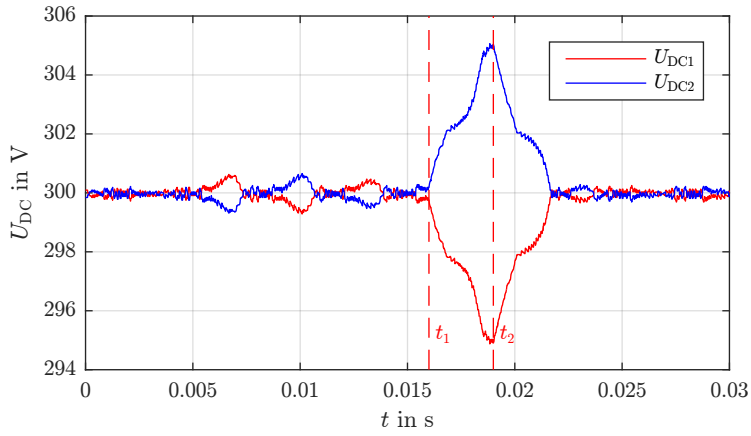


Figure 6.7: DC-link voltage balancing after asymmetry excitation

Switching Frequency Versus Modulation Index

As the working behaviour of direct current control methods depend strongly on the desired modulation index it is necessary to investigate the new algorithm over the complete operating range of the inverter. According to the derivation of the control algorithm with an ideal inverter system in Chapter 5, the analysis focusses on the switching frequency at different operating points of the inverter.

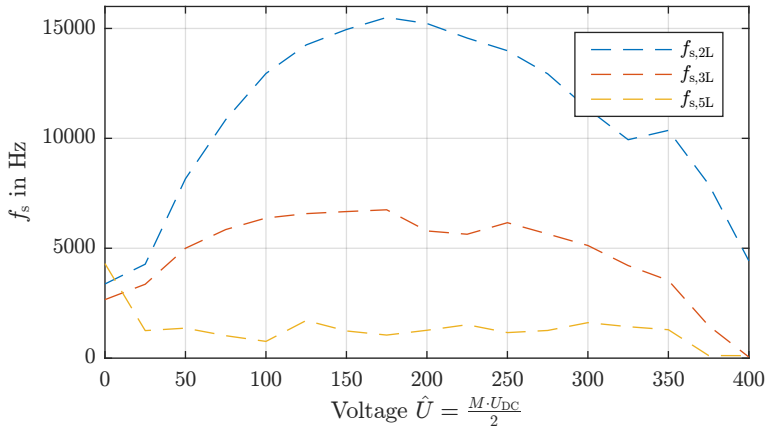


Figure 6.8: Switching frequency versus modulation index for a two-, three- and five-level inverter with constant inductance and parameters set according to Table 6.3

Figure 6.8 shows the average switching frequency of all three phases of a two-, three- and five-level inverter. The shape of the individual curves is similar to the ideal consideration of these three converter systems. Again, it is clear that the switching frequency of a two-level converter is the highest and of a five-level system the lowest. The difference to the simulations on a ideal inverter system is caused by the variation of the inductance. It should be noted that these curves also have a dependence on the amplitude of the set-point current and the load. Nevertheless, the basic shape remains similar.

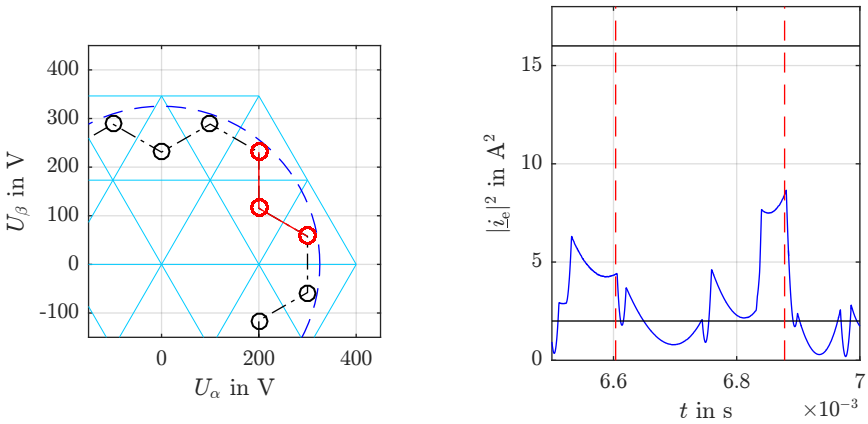
6.1.6 Seeking Cases

In Chapter 5.8.1, seeking cases were introduced which describe the functionality and the behaviour of the control method at its outer hysteresis limit. Apart from the standard case, special cases, such as grid faults, special operating points and set-point jumps were also specified. The following simulations show the behaviour for the cases in a more realistic environment.

Case 1: Unimplemented Measurement

As in the previous chapter the first seeking case is the nominal operating point of a grid connected inverter system. This is the simplest case for an

unimplemented measurement. As soon as the position of the actual reference voltage is no longer present in the actual sector, the three existing space vectors are no longer sufficient and the current error rises above the predetermined inner tolerance band. In the simplest case, the outer tolerance band is reached and a sector change is initiated.



(a) Pseudo reference voltage in $\alpha\beta$ plane (b) Squared absolute value of the current error

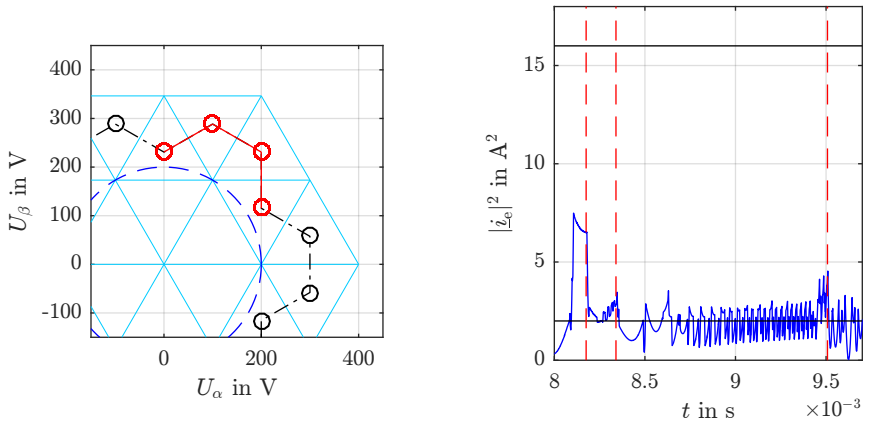
Figure 6.9: Time segment with sector change for seeking case 1

In Chapter 5.8.7, an advanced seeking algorithm is presented that determines whether a sector change must occur by evaluating the trajectory of the current error after a switching operation. Figure 6.9a shows the pseudo-reference voltage in $\alpha\beta$ plane of a specific time segment (red). The corresponding current error is shown in Figure 6.9b. Two things are clearly visible. The two vertical red lines indicate the points in time at which a sector change was detected and a correction of the sector was initiated. Since two sector changes are necessary for the illustrated time segment, two vertical time-lines are present. Furthermore, it can be seen that the sector changes are carried out without reaching the outer tolerance band. This shows the functional principle of the advanced seeking algorithm.

Case 2: Unimplemented Measurement 2

This case is characterized by the fact that the true voltage reference directly intersects the corner points of the triangles. One exemplary time segment

is shown in Figure 6.10. As the reference seeking algorithm is only capable to jump in one of the three neighbouring triangles at least three sector changes are necessary. Figure 6.10a highlights the involved pseudo reference voltages in $\alpha\beta$ representation. The corresponding current error is shown in Figure 6.10b. As in the previous case the advanced seeking algorithm triggers the sector correction before the outer hysteresis limit is reached. From the figure it becomes clear that after the first and second sector change the algorithm is still not in the correct sector as it is not possible to keep the current error permanently within the inner tolerance area. Only after the third sector change the sector of the pseudo reference voltage equals the sector of the reference voltage and the current control algorithm is able to keep the current error approximately within the hysteresis limit.



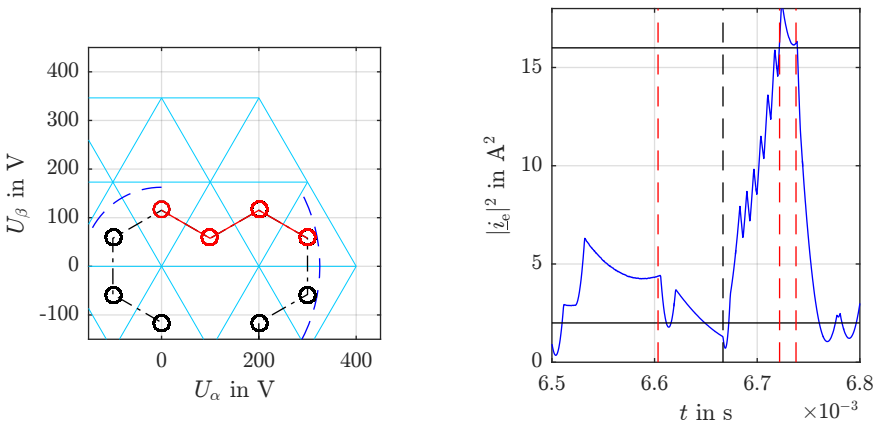
(a) Pseudo reference voltage in $\alpha\beta$ plane (b) Squared absolute value of the current error

Figure 6.10: Time segment with sector change for seeking case 2

Case 3: Reference Fault

In the third case shown in Figure 6.11, a grid fault was specified. In addition to halving the amplitude, a phase shift of 60° was added to the true reference voltage. This fault results in the trajectory of the pseudo reference voltage shown in Figure 6.11a. Figure 6.11b shows the current error. The sector changes are highlighted in red. In order to reach the target sector, at least three sector changes are necessary. Each dashed red line corresponds to a

sector change. The black line corresponds to the time when the grid fault occurs. In the case shown, a sector change took place before the occurrence of the grid fault. After the grid fault, it can be clearly seen that the current error increases and a correction is made after reaching the outer tolerance band. Since the error does not decrease as expected after the sector change, a further sector change is necessary.



(a) Pseudo reference voltage in $\alpha\beta$ plane (b) Squared absolute value of the current error

Figure 6.11: Time segment with sector change for seeking case 3

Case 4: Set-Point Change

Similar to the ideal view, one can achieve the highest possible dynamics at a set-point jump by using the known information and selecting the space vector which best reduces the current error. For converters with two- or three-levels, it is sometimes sufficient to use only the reference seeking algorithm. As soon as the set-point jump occurs, the outer tolerance band is reached and a space vector from an adjacent triangle is selected which best reduces the current error. As soon as the current error is back in the inner tolerance band, a further change may be necessary since the real reference voltage could still be in the starting sector. Therefore the seeking algorithm works as described above.

In the special case shown in Figure 6.12 a set-point change from 20 A $\rightarrow$ -20 A was carried out which corresponds to a phase shift of 180°. The

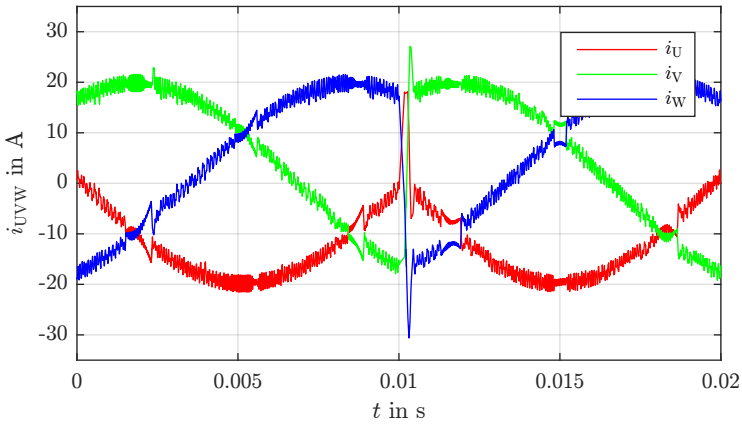


Figure 6.12: Three phase current with set-point change

resulting pseudo reference voltage is shown in $\alpha\beta$ plane in Figure 6.13. As it can be seen several sector changes are carried out until the pseudo reference voltage ends in the starting sector. In the case shown, the seeking algorithm has performed six sector changes in order to reach the new target value of the current. In this case, the true reference voltage has not moved out of the original sector.

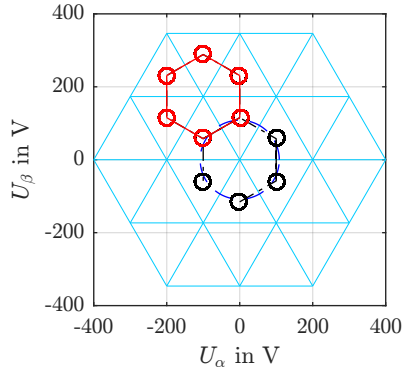


Figure 6.13: Pseudo reference voltage in $\alpha\beta$ plane for seeking case 4

6.2 Experimental Verification

To verify and confirm the functionality, the SHC, which was derived in Chapter 5, was also implemented on a real system. Since in reality additional disturbances and influences affect the overall system, the new method can only be finally evaluated under these conditions. In addition to the calculation times, dead times and block times that can also be simulated in a more realistic simulation (previous section), there are further effects that have to be taken into account in a real implementation. The following effects could have a negative impact:

- Inaccuracies in the measurements for current and voltage.
- Oscillations due to unknown system parameters.
- Additional delay times within the hardware components.
- Sudden changes or unknown loads.
- Grid faults in grid connected applications.

6.2.1 Experimental Setup

The basic structure of the entire hardware system used for experimental verification is schematically shown in Figure 6.14. In addition to the standard hardware components an FPGA system was used which offers new possibilities, not only in terms of speed. The advantage of the FPGA compared to standard microprocessors is based on its structure, which facilitates the

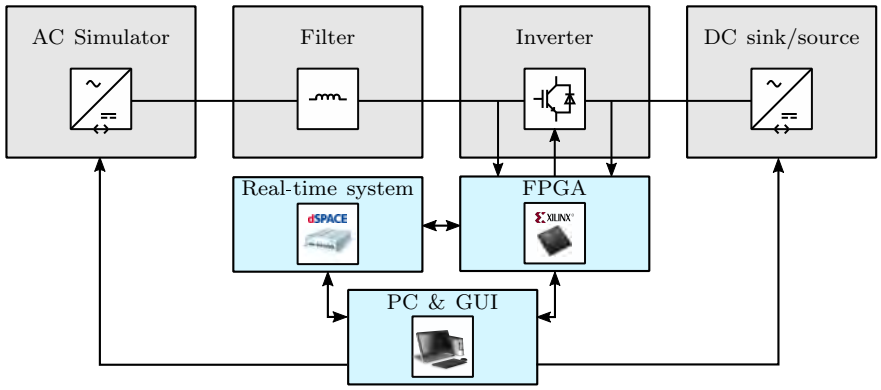


Figure 6.14: Basic structure of hardware system

realization of a fully synchronous operation and the use of the FPGA as a real-time system. Since all run times in the individual components implemented are exactly known, a precise prediction can be made over the signal propagation time, which plays an important role for control tasks. The possibility of parallelization is used in the presented work to read out, filter and process measured data and to use monitoring functions at the same time. The three main advantages offered by the FPGA system within this project are the parallelization and real-time capability as well as the flexible programmability.

Via various interfaces, which are necessary for the operation of different converter systems and for the exchange of relevant data, extensions can be connected to the FPGA system. The most important interfaces offered by the self-developed FPGA system are:

- Interface to a off-the-shelf two-level and three-level inverter system.
- Interface to self-developed five-level inverter system.
- Measurement interfaces for currents and voltages.
- DA (Digital to Analog) interface for fast output of FPGA internal data.

The implementation of the interfaces and the control method have been programmed in VHDL. Highly demanding parts were implemented directly using VHDL whereas other parts were generated using the MATLAB/SIMULINK environment using the automatic VHDL code generation capability.

A control PC in combination with a dSPACE system is used to display measured data and to set-up system parameters before and during operation. The AC and DC sources and sinks can also be individually controlled by this control PC.

In order to verify the functionality and show the working behaviour of the SHC algorithm different measurements on a two-, three- and five-level inverter were carried out. The main system parameters have been set according to Table 6.4 with some parameters being adapted for special measurements.

Hardware Components

In addition to the main part of the system, the FPGA board, further hardware components are used. Three different topologies, a two-, a three- and a five-level inverter, are provided as converters. The standard two-level and the NPC three-level converter are commercial modules from Semikron. The

Table 6.4: Main Parameters for Measurements

Paramter	Value
Grid voltage	$0 \rightarrow 400$ V(50 Hz)
Filter inductance	1.0 mH (three- and five-level)
Filter inductance	1.6 mH (two-level)
DC-link voltage	600 V
DC-link capacitance	7/2/1 mF (two-/three-/five-level)
Set current $\hat{I}$	10 A
Inner hysteresis δ	$\sqrt{2}$ A
Outer hysteresis δ_o	$\sqrt{16}$ A
Inverter dead-time	3 μs (Appendix C)
Inverter block-time	3 μs

five-level DCI inverter was designed and built up within the project. The parameters of the inverter systems are listed in Appendix C.

In order to be able to test the control method and the overall system according to engineering standards, a grid simulator is used as an AC source and sink. The simulator facilitates the possibility to set-up various special cases such as harmonic components, voltage dips, phase failures, etc.. A set of bi-directional DC sources and sinks allow a very flexible use. By means of the individually adjustable voltages, for example DC-link balancing methods can be effectively tested. The detailed system parameters can also be found in Appendix C.

As a line filter a first order inductive filter is used. In order to be able to set different inductance values, taps for 0.5, 1, 1.5, and 2 mH are available for the three- and five-level inverter and taps for 0.8, 1.6 mH for the two-level inverter. Within the filter set-up additional contactors for pre-charging and connecting to the mains are installed.

Structure and Requirements of the Current Measurement

An accurate and highly dynamic current control method sets high demands on the quality of the current measurement. In addition to the accurate and low-noise measurement of the actual signal, the current measurement path must be resistant to external interference and must provide a high dynamic. Since the quality of the current measurement depends on the

entire measuring chain, all components must be considered and evaluated, starting with the current sensor, via signal processing, digitization, isolation and digital filtering.

Four identical current transducers with a nominal current of 200 A_{rms} and a conversion ratio of 1:2000 are used for the experimental verification in this thesis. The analogue output of the current transducers are adapted and filtered on the hardware side before they are digitized via a 14-bit AD converter. After digital processing of the data streams in the FPGA, the current values are available with a sampling rate of 40 MHz. The described current measuring path causes a delay of approximately 300 ns. The exact type of the current transducer and of the AD converter are listed in Appendix C.

6.2.2 Measurements

General Functionality

Similar to the realistic simulations, the basic mode of operation of the various converter systems is shown in a combined view. For all inverter systems, the nominal operating point for grid connected systems was assumed. Figure 6.15 shows three periods of the current where the first period was measured on a two-level inverter, the second period on an NPC three-level inverter, and the third period on a five-level inverter. In this figure, there is only a little difference in the switching frequency of the first two periods since the two-level inverter has a higher inductance in comparison to the

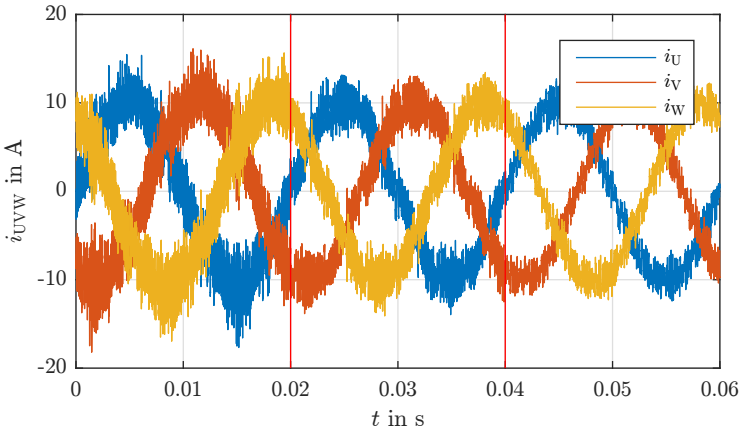


Figure 6.15: Inverter output current for a two-, three- and five-level inverter

three-level inverter. In the third period, a reduced switching frequency can be seen since the inductance for the five- and three-level converters has been kept constant.

The measurement results prove that the new control method works as intended for inverters of different topologies and levels. When the inverter system was changed, in addition to the exchange of the hardware, only the level parameter had to be modified in the controller set-up. This fact confirms the generic nature of the proposed method.

Figure 6.16 shows the squared absolute value of the current error. The first section corresponds to that of the two-level inverter, the second to that of the three-level converter, and the last to the five-level converter. Due to the topology and the selected inductance, the difference between the second and third sections is particularly noticeable. As the voltage across the inductance of the five-level system is halved, the overall error current is smaller than that of the three-level system. This property enables a further reduction of the inductance or the adjustment of the tolerance band to reduce the resulting distortion.

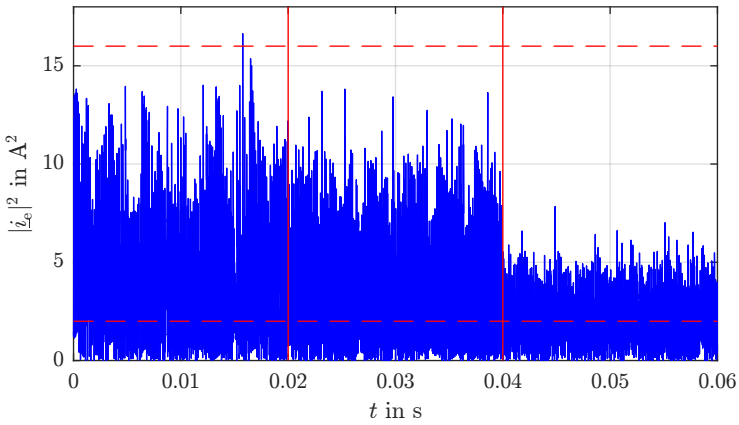


Figure 6.16: Squared absolute value of the current error for a two-, three- and five-level inverter

Five-Level Inverter Control with Smaller Tolerance Band

In order to illustrate the possibility of reducing the size of the tolerance band, the measurement at the nominal operating point for the five-level inverter system was repeated. The tolerance band for this measurement

was chosen to be half the size of the previous measurements. Figure 6.17 shows two periods of the three phase current. The corresponding squared absolute value of the current error is shown in Figure 6.18. The first time section corresponds to a tolerance band of $\sqrt{2}$ A and the second segment to a tolerance band of $\sqrt{0.5}$ A. It becomes clear that the distortion can be reduced in comparison with the previous measurement. The evaluation of the measurement has shown that the switching frequency is higher by a factor of 1.7 when halving the tolerance band, while simultaneously reducing the total harmonic distortion by approximately 42%.

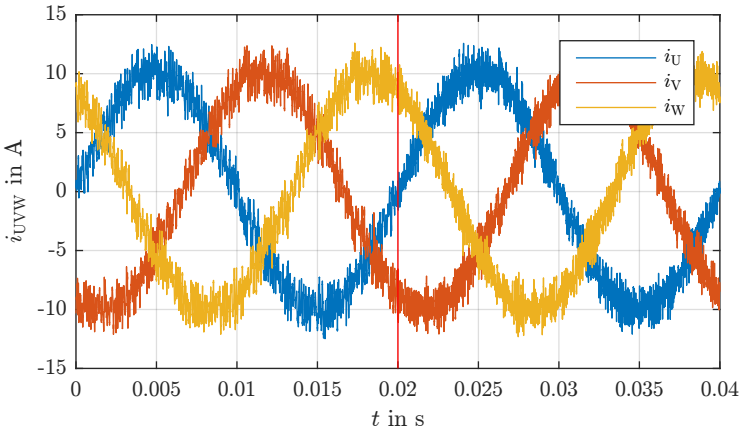


Figure 6.17: Three phase inverter output current for a five-level inverter with different sizes of tolerance band

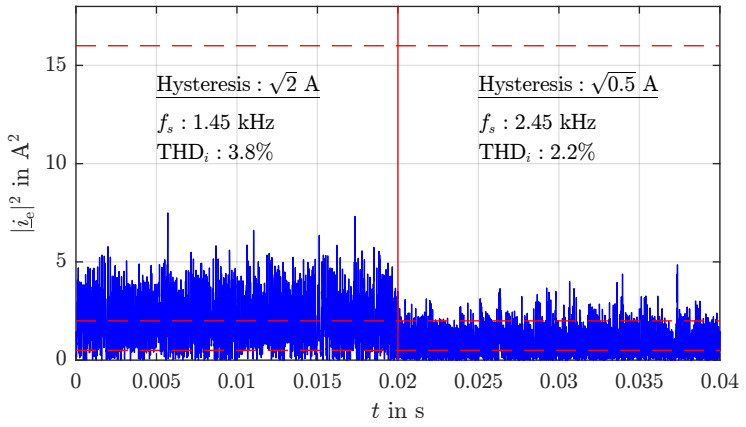


Figure 6.18: Squared absolute value of the current error of a five-level inverter

DC-link Balancing

When using a DCI, the DC-link symmetry must be actively maintained. In order to verify the functionality of the SHC in combination with the DC-link balancing algorithm, a conscious asymmetry in the DC-link circuit of the three-level inverter system was initially provoked. At time t_1 this asymmetry was removed, resulting in a gradual approach of the two DC-link voltages. After approximately 12 ms, the symmetry is restored as shown in Figure 6.19. The duration is decisively dependent on the set-point of the nominal current, the size of the DC-link capacitors and the operating point of the inverter.

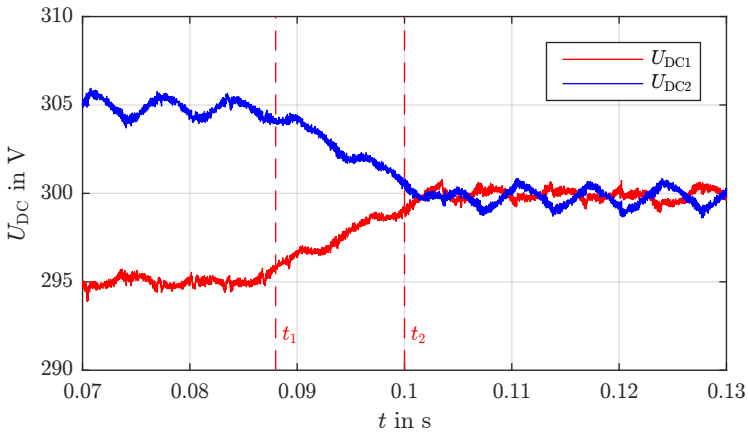


Figure 6.19: DC-link voltage with provoked offset

Evaluation of a Switching Event

Figure 6.6 was used to evaluate the approximate duration of a switching event within the realistic simulation environment. The basic principle and the need for the introduction of dead times and block times have already been explained in this chapter. As mentioned, however, there are in fact, additional delays due to delay times in the hardware and disturbances due to noise and capacitive effects.

To evaluate the duration of a real switching event Figure 6.20 shows a real measurement. The noise on the error signal and the oscillation caused by the system capacitances is clearly visible. At the time t_1 the inner tolerance band is reached. After approximately 4.3 µs the switching operation to set the new output voltage is performed causing an oscillation on the current

error. This oscillation is the reason for introducing a blocking time. At the earliest after additional 4.3 µs, in this particular case, it can be ensured that the evaluation of the trajectory of the current error is correct. If these times are poorly chosen, this could lead to additional switching operations.

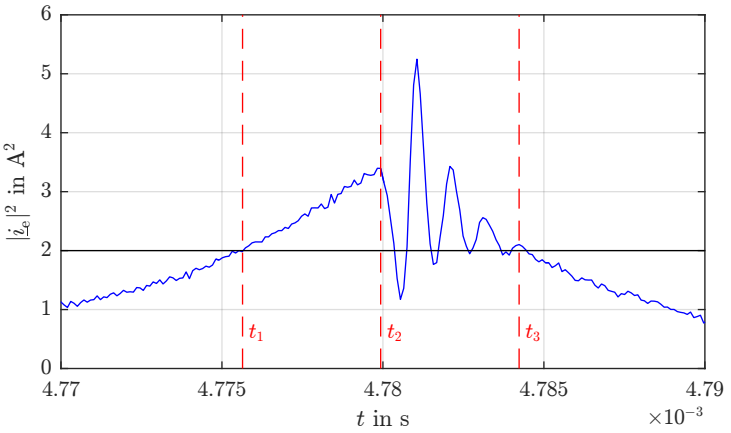


Figure 6.20: Time section after reaching the inner tolerance band limit of current error with dead-times and oscillation

Measurements Versus Modulation Index

As explained before the behaviour of direct current control methods depend on the operating point and the modulation index. To show the functionality of the proposed algorithm, measurements were carried out over the complete working range of a two-, three- and five-level inverter.

In the ideal and in the realistic simulation, it was determined that the switching frequency varies over the degree of modulation. The difference between the level numbers, while using the same inductance, were the switching frequency and the course of the frequency over the modulation index. For example, there was one maximum within a two-level inverter, two maxima for a three-level inverter, and four maxima for a five-level inverter system.

For the real measurements, the inductance could not be kept constant for all three inverter systems, since the passive components were already integrated in the test set-up. An inductance with 1.6 mH was selected for the two-level inverter system and an inductance with 1 mH for the three- and five-level inverter systems. Figure 6.21 shows the switching frequency

versus the modulation index for all three inverter systems. The curves are similar to those from the simulative verification. In all inverter systems, the maximum switching frequency occurs in the centre of a triangular sector. The switching frequency of the two-level inverter is somewhat lower to that of the realistic simulations. This is caused by the higher value of the inductive filter. Considering this measurement, it can be said that the new current control method in conjunction with the advanced seeking algorithm works in the entire voltage operating range of the inverter. The measurements in the overmodulation range, where $\hat{U}$ is greater than 350 V, and for the zero voltage mode were not part of this measurement but they are listed as additional measurements in Section 6.2.4.

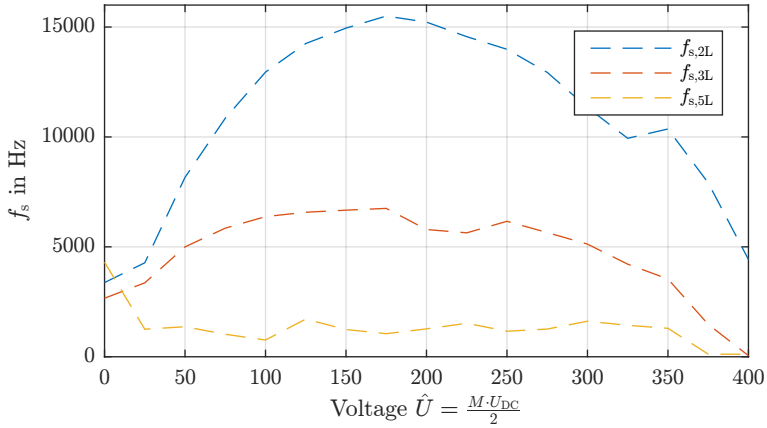


Figure 6.21: Switching frequency versus modulation index for a two-, three- and five-level inverter

6.2.3 Seeking Cases

The need for experimental verification of the SHC algorithm and the advanced seeking algorithm makes it necessary to replicate all previously defined seeking cases on a real test bench. As before, the proof of functionality and behaviour is performed using a three-level inverter system. In order to show the difference between an inverter with higher levels, the behaviour for seeking case 1 is additionally examined with a five-level inverter system.

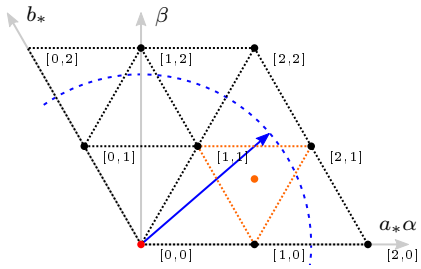
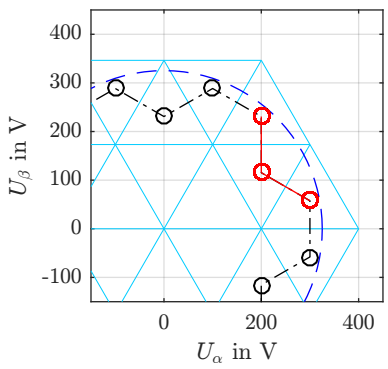


Figure 6.22: Seeking Case 1

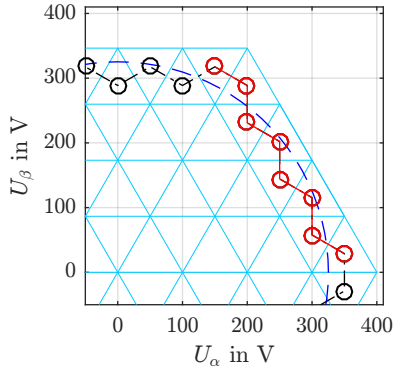
Case 1: Unimplemented Measurement

The first seeking case describes the nominal operating point of a grid connected inverter system (Fig. 6.22). As with the realistic simulation and the ideal consideration of a three-level inverter two sector changes have to be initiated (Fig. 6.23a). The advanced seeking algorithm evaluates the trajectory of the error current and the switching operations to predict a sector change before reaching the outer tolerance band. Figure 6.23c shows the points in time at which a sector change is performed.

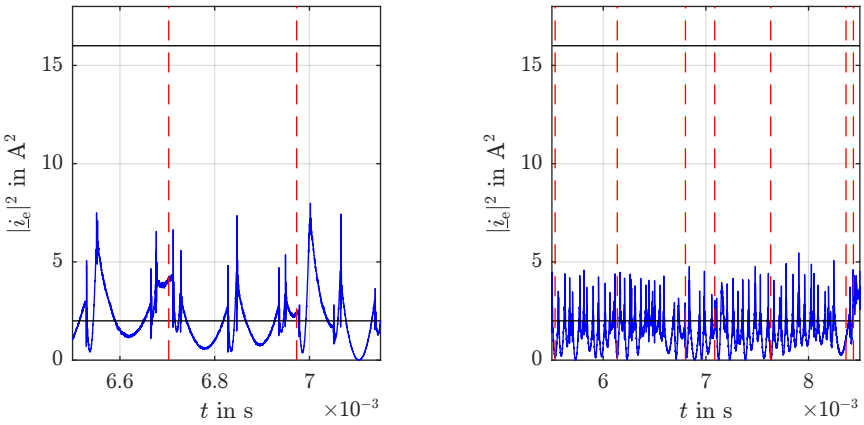
Figure 6.23b shows a similar time interval as before in the space vector diagram of a five-level inverter. It is apparent that the number of sectors is increasing. From this fact it follows that more sector changes are necessary



(a) Three-level pseudo reference voltage in $\alpha\beta$ plane for the three-level inverter



(b) Five-level pseudo reference voltage in $\alpha\beta$ plane for the five-level inverter



(c) Squared absolute value of the current error for the two-level system

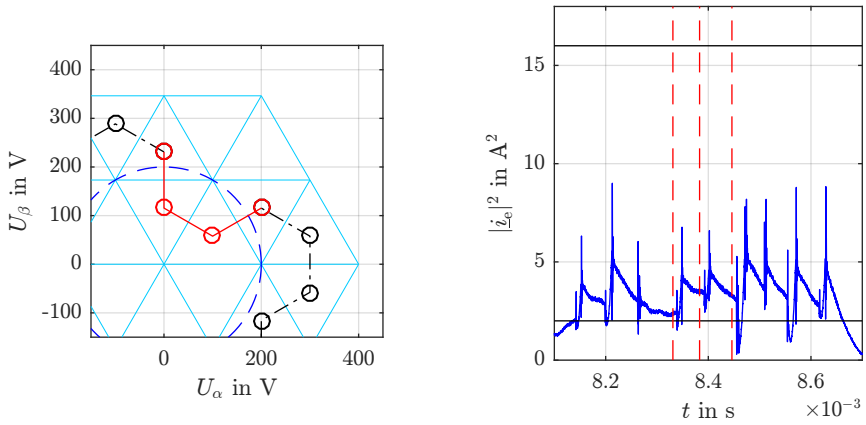
(d) Squared absolute value of the current error for the five-level system

Figure 6.23: Time segment with sector changes of a three- and five-level inverter system for seeking case 1

for a similar angular range of the reference voltage. Figure 6.23d shows, for the time interval of interest, the error current and the times at which a sector change is performed. From the figure it becomes clear that the number of sector changes increases. However, the advanced seeking algorithm works like expected for the three- and five-level inverter system.

Case 2: Unimplemented Measurement 2

Since the advanced seeking algorithm can only jump into adjacent triangles, the second seeking case represents a special operating point. According to the theory, at least three sector changes are necessary for the path shown in Figure 6.24a. Figure 6.24b shows the current error and that the seeking algorithm can deal with this special case. If one compares the figures from the ideal simulation and the reality one establishes that the pseudo reference voltage paths are different. This is due to the randomness of the position of the current error vector in the $\alpha\beta$ diagram.



(a) Pseudo reference voltage in $\alpha\beta$ plane (b) Squared absolute value of the current error

Figure 6.24: Time segment with sector changes for seeking case 2

Case 3: Reference Fault

This seeking case was adjusted in the same way as for the previous investigations. To illustrate this case, a simultaneous amplitude and phase error of the reference voltage was set. The path of the true reference and pseudo reference voltage is shown in Figure 6.25. It can be seen that several changes

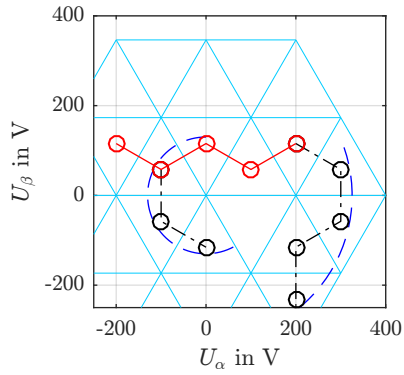


Figure 6.25: Pseudo reference voltage in $\alpha\beta$ plane for seeking case 3

in the pseudo reference voltage are necessary to compensate the reference fault. The resulting trigger times are shown in Figure 6.26. After three sector changes, the position of the pseudo reference voltage is the same as the actual voltage. However, since the current error is still outside the outer tolerance band, a further correction is carried out in order to reduce the error as quickly as possible. In this special case the algorithm requires seven sector changes and approximately 0.3 ms to reach the final sector and to reduce the current error to a level within the inner tolerance band.

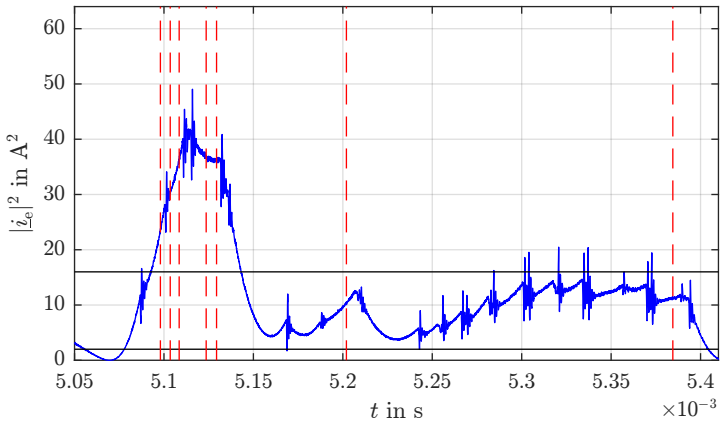


Figure 6.26: Squared absolute value of the current error for seeking case 3

Case 4: Set-Point Change

Figure 6.27 shows the inverter output current. At the time t_1 a set-point change was triggered resulting in a reversed power flow. As shown in Figure 6.28b there is no significant control deviation after 0.3 ms. The operation of the seeking algorithm for this case is shown in Figure 6.28a. In the time period shown, a large number of sector changes take place in order to reduce the current error as quickly as possible. After the current error is below the inner tolerance band, the pseudo reference voltage is back at the sector where it was before the set-point jump. Since a set-point jump is very easy to recognize, this information could be used to reduce the current error optimally and even faster. However, this seeking case is supposed to show how the algorithm responds to such a change.

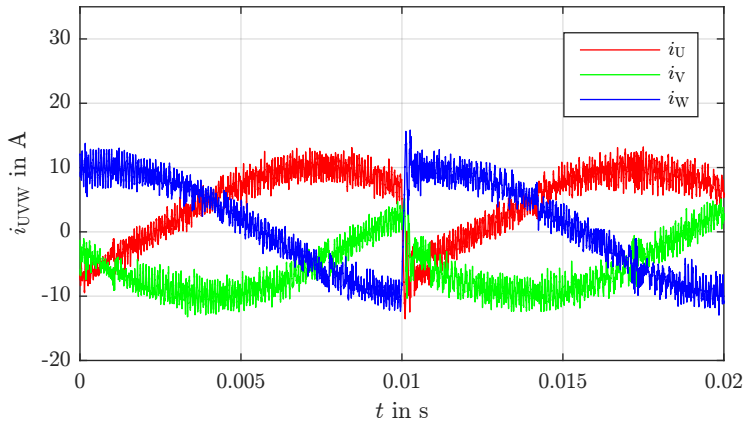
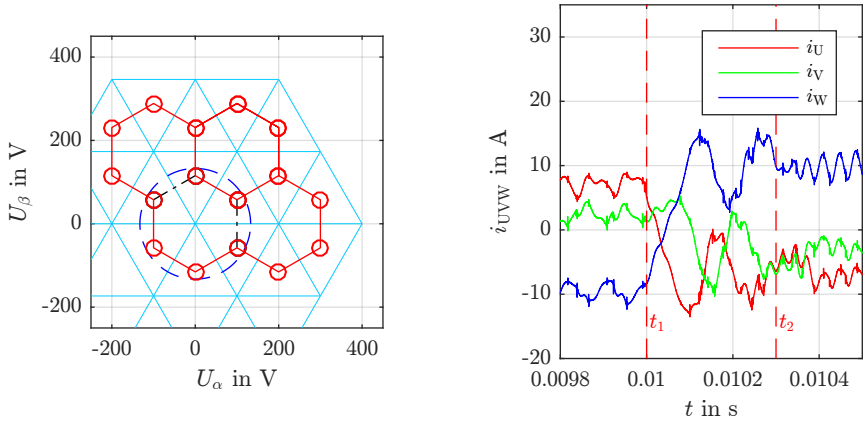


Figure 6.27: Three-phase current with set-point jump



(a) Pseudo reference voltage in $\alpha\beta$ plane (b) Zoom of the three-phase current

Figure 6.28: Time segment with sector changes for seeking case 4

6.2.4 Additional Measurements

In order to present the robustness, the independence from the load, but also the universal applicability and further possibilities for improvement, additional measurements were performed on the hardware components. In order to protect the laboratory hardware against unpredictable destruction some measurements were carried out with reduced voltages. Table 6.5 shows

an overview of all additional measurements, the used hardware platform and the DC-link voltage.

Table 6.5: Additional measurements

Measurement	Inverter	DC-link
Sensorless Synchronization	Five-level DCI	600 V
Usymmetrical Loads	Three-level NPC	600 V
Overmodulation / Square Wave Mode	Two-level	90 V
Low/Zero Voltage Mode	Two-level	90 V
Reference Frequency Variation	Three-level NPC	600 V
Reference Voltage with Harmonics	Three-level NPC	650 V
Reference Voltage with Single Phase Fault	Three-level NPC	650 V
Waveform Variation of Set-Point Current	Three-level NPC	180 V

Sensorless Synchronization

When the new current control method was introduced, a synchronization and phase detection procedure for the reference voltage $\underline{u}$ was intentionally omitted. In principle, the determination of the phase position and amplitude of the reference voltage provides the basis for higher level controllers, such as, for example, an active and reactive power control. With respect to the control method, an accurate knowledge of the position of the reference voltage in the space vector diagram can lead to further improvements [68]. Figure 6.29 shows one period of the current with the method presented in the thesis, without any knowledge of the position of the reference voltage $\underline{u}$, and a second period in which the position was determined by a synchronization method [69].

Figure 6.30 shows the squared absolute value of the current error corresponding to the two periods from Figure 6.29. Apparently, there are no significant deviations between those two methods. When evaluating the two measurements in more detail, it has been shown that the use of a suitable synchronization method improves the total harmonic distortion while simultaneously reducing the switching frequency. Thus, by using a suitable synchronization method, the switching frequency of a five-level inverter could be reduced by approximately 17% and the total harmonic distortion by about 34%. The improvement in the THD is justified by the fact that, unlike the advanced seeking algorithm, the exact position of the reference voltage is

included in the calculation of the error reducing space vector. This results in less switching operations, better reactions and an improved THD.

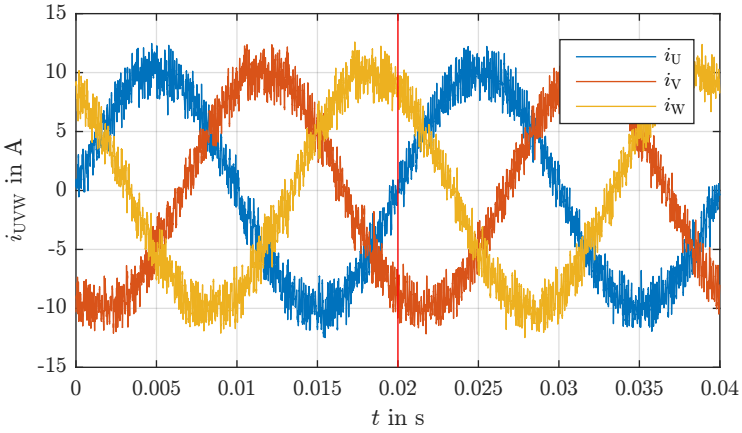


Figure 6.29: Three-phase inverter output current without (1st period) and with (2nd period) synchronization method

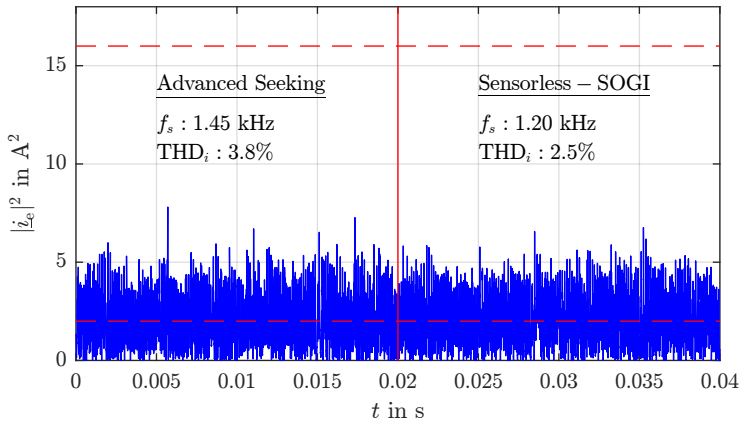
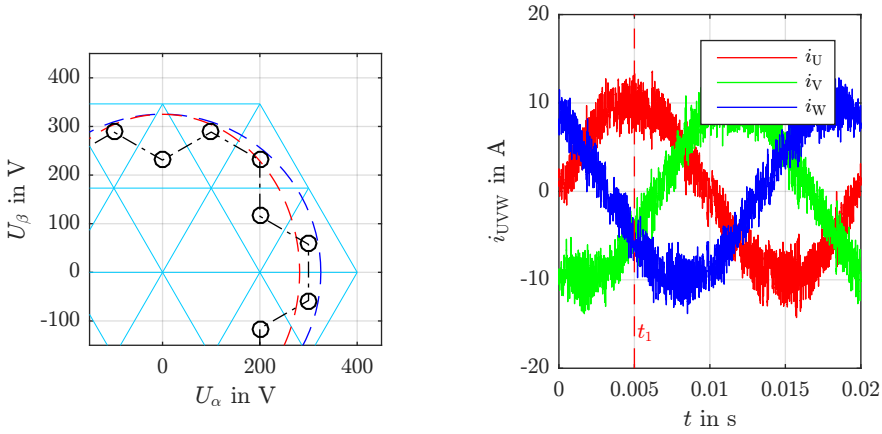


Figure 6.30: Squared absolute of the current error without and with synchronization method

Unsymmetrical Loads

As shown above and as known from literature, an advantage of direct current control methods compared to indirect ones is the ability to control unknown or even unbalanced loads. Figure 6.31a shows an $\alpha\beta$ trajectory of a balanced (blue) and an unbalanced load (red) as well as the pseudo reference voltage points. Figure 6.31b shows a time period of the three phase current. At time t_1 a voltage dip to 80% of the normal grid voltage of phase L1 was performed. It can clearly be seen that in spite of this asymmetry, the control of the three-phase line current works like expected.



(a) Pseudo reference voltage in $\alpha\beta$ plane (b) Three-phase inverter output current

Figure 6.31: Time segment with sector changes for measurements with an unsymmetrical load

Overmodulation and Square Wave Mode

The operating range of an inverter can basically be divided into three areas and described via the so-called modulation index. For grid-connected applications, the inverter usually operates in sinusoidal modulation mode. In cases of grid faults or other application areas (motor control), it is sometimes necessary to leave the sinusoidal modulating mode and change to the overmodulation mode or square wave mode. In square wave mode the inverter only changes its output voltage every 60° leading to a single switching operation every half period. Due to the working behaviour of the SHC con-

troller with its pseudo reference voltage located at the centre of a triangular sector, operation in square wave mode is only possible with small adaptations. Figure 6.32 shows the space vector diagram of a two-level inverter with the different modulation ranges. To investigate the behaviour of the SHC controller in these areas, additional measurements were carried out.

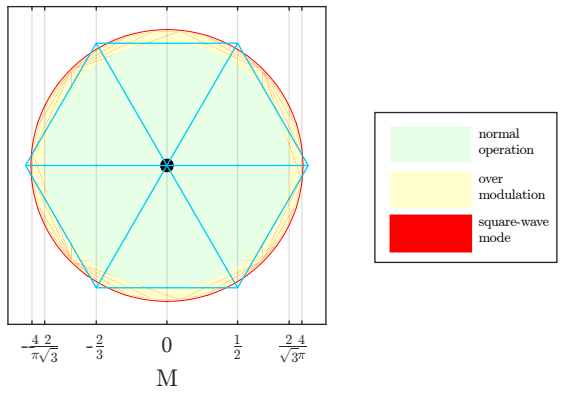


Figure 6.32: Space vector diagram and modulation areas

Figure 6.33 shows the three-phase currents for a two-level inverter. The load voltage was selected in such a way that a degree of modulation of $M = \frac{5}{4}$ results. This modulation index corresponds to the overmodulation area. It is apparent that the current control method is working even within this operating point. In some areas, the output voltage of the inverter is too small, resulting in an amplitude error. This amplitude error becomes clear when comparing the actual value of the measured current and the set-point current of phase U.

The measurements for overmodulation and the measurements versus modulation index have shown that the new control method works in the entire operating range of the inverter without further adjustments of system or control parameters. In summary, it can be said that the new method can be used not only for grid connected but also for other applications like motor control.

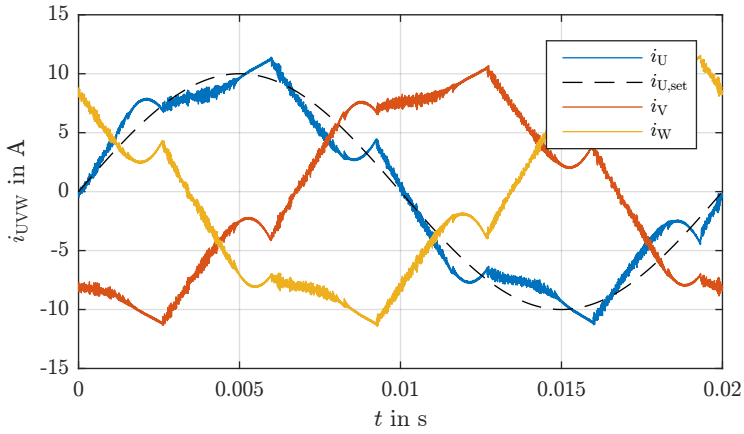


Figure 6.33: Measurement in overmodulation area $M = \frac{5}{4}$

Low/Zero Voltage Mode

Similar to the overmodulation range, the operating point with a load voltage of zero ($M = 0$) represents a special case. However, in some applications like motor drives, this operating point is common. Figure 6.34 shows the phase current resulting from the mentioned operating point. Due to the low switching frequency in areas where the voltage is close to a converter output voltage the tolerance band in this measurement was set to a smaller value (see Tab. 6.5) than for the previous measurements.

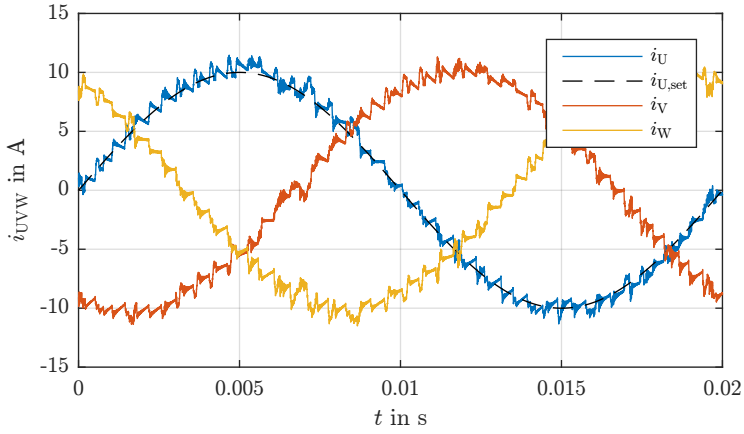


Figure 6.34: Three-phase current for zero reference voltage

Frequency Variation of Reference Voltage

The following measurement shows the behaviour of the direct current control method under the influence of a reference voltage with variable frequency. Variable frequencies of the reference voltage are particularly relevant for motor applications. Nevertheless, the measurement shown is an arbitrary operating point which is intended to illustrate the wide range of applications and robustness of the SHC method.

Three different variations of the frequency were executed for the measurement. After 40 ms the frequency of the reference voltage was increased from 25 Hz to 50 Hz. After further 40 ms, the frequency was increased again to 100 Hz. The corresponding reference voltage is shown in Figure 6.35. For this special test a manual phase setting with 50 Hz was selected for the set-point current. Figure 6.36 shows the three-phase output current of the inverter. At the times t_1 and t_2, at which the frequency of the reference voltage has been increased, no abnormal change in the current waveform can be detected. This fact allows to conclude that the direct current control method presented in this thesis can also be used for applications where the frequency of the reference voltage is not constant. It should be mentioned that no controller parameters have been changed for this measurement.

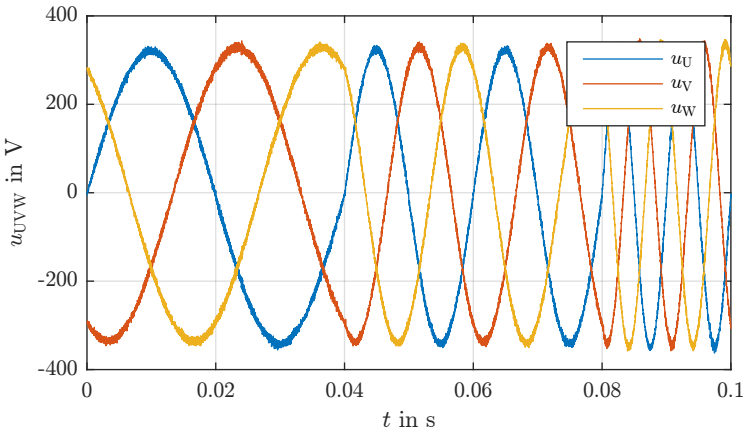


Figure 6.35: Reference voltage with frequency variation

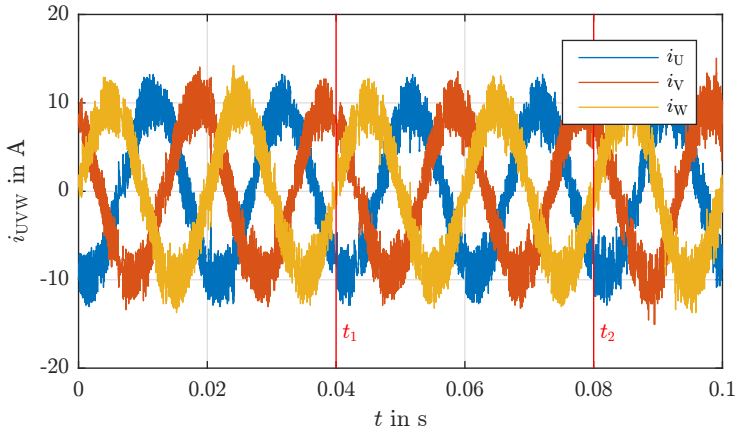


Figure 6.36: Three phase current under frequency variation of the reference voltage

Reference Voltage with Harmonics

Grid-connected inverters must comply with different grid codes. There are different test cases to ensure the operability of converter systems on the grid that need to be guaranteed. A special case in the grid codes specifies a reference voltage with harmonic components. More specifically the fundamental frequency component of the reference voltage is distorted with a seventh harmonic at 10% of the fundamental amplitude. Figure 6.37 shows the three-level space vector diagram with the corresponding true reference voltage and the resulting pseudo reference voltages. It is already apparent at

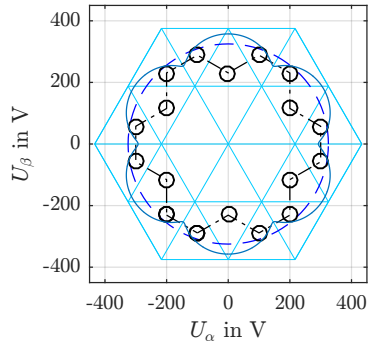


Figure 6.37: Pseudo and distorted reference voltage in $\alpha\beta$ plane

this point that this case is similar to seeking case 1 as there occur only standard sector changes. Figure 6.38 shows the output current of the inverter. As expected, the SHC method is able to work with distorted reference voltages.

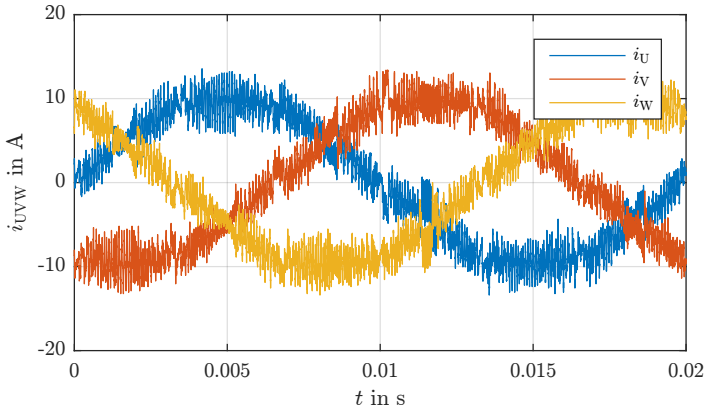


Figure 6.38: Three phase inverter output current

Reference Voltage with Single Phase Fault

A further test case for grid-connected inverter systems is a single phase fault. The corresponding space vector diagram is shown in Figure 6.39. As it is apparent, the shape of the circular trajectory changes to an oval. Within this special case different degrees of modulation are present within a single period. Thus the voltage control range must be utilized from a small to a large degree of modulation. This, on the one hand, causes a variation in the

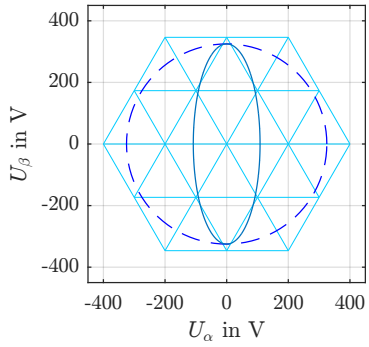


Figure 6.39: Reference voltage in $\alpha\beta$ plane

switching frequency and, on the other hand, the necessity of additional sector changes. The functional capability and the measured three-phase current at this operating point are shown in Figure 6.40.

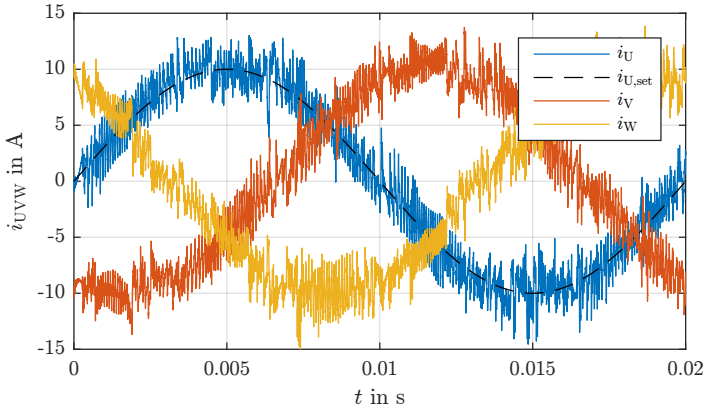


Figure 6.40: Three phase inverter output current

Waveform Variation of Set-Point Current

In order to show the dynamics, the robustness and the flexibility of direct control methods, the set-point current can be changed arbitrarily. In order to illustrate the behaviour of the SHC controller with different specifications for the set-point current, additional measurements were carried out. The results for a three-phase current are shown in Figure 6.41 and are defined as follows:

(**a**) Fig. 6.41a shows the current with equal amplitude and a phase shift of 120°.

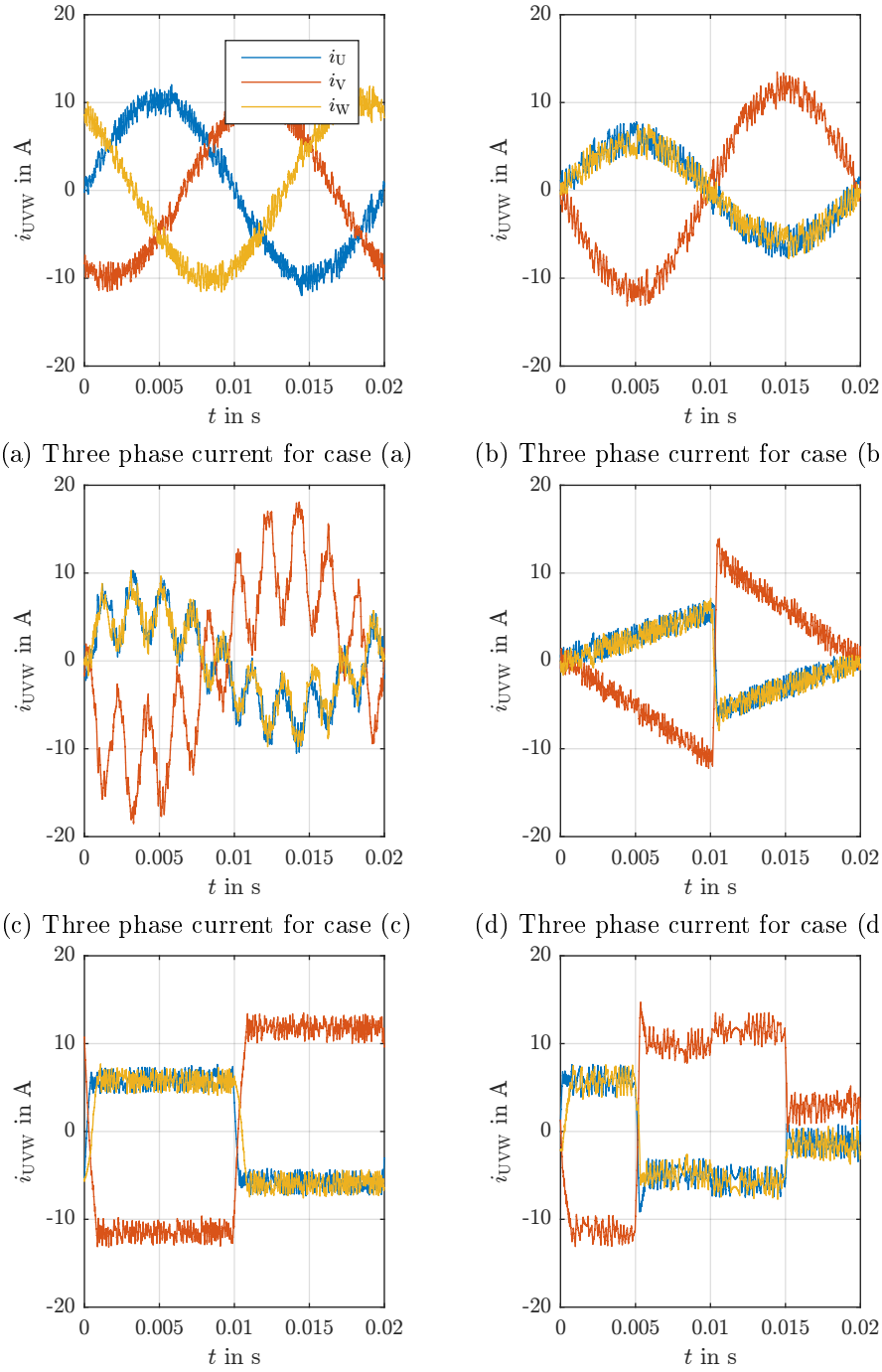
(**b**) Fig. 6.41b shows an arbitrary sinusoidal current with an amplitude and phase difference.

(**c**) Fig. 6.41c shows the identical current as before with an additional 50% harmonic sinusoid at 500 Hz.

(**d**) Fig. 6.41d shows an arbitrary sawtooth shape.

(**e**) Fig. 6.41e shows an arbitrary rectangular shape.

(**f**) Fig. 6.41f shows an arbitrary rectangular shape with a random change in the amplitude.



(a) Three phase current for case (a)

(b) Three phase current for case (b)

(c) Three phase current for case (c)

(d) Three phase current for case (d)

(e) Three phase current for case (e)

(f) Three phase current for case (f)

Figure 6.41: Waveform variation of set-point current

6.3 Summary of Simulation and Experimental Verification

In this chapter, the new direct current control method has been verified simulative and experimentally. For this purpose, a flexible hardware platform was introduced, which allows the control of inverters of different topologies. In addition to simulations and measurements in the entire voltage operation range of the inverter, some special cases were investigated. In summary, the control method shows excellent properties in terms of simplicity, robustness, dynamics and independence from the inverter level count and the hardware topology.

Chapter 7

Conclusion and Future Work

7.1 Conclusions and Contributions

Technology of power electronic systems in industry and energy production encompasses various inverter topologies ranging from two-, three- and higher level multilevel inverters to parallel-connected converters. They are normally voltage-controlled and operate with pulse-width or space vector modulation techniques. In those applications, only an indirectly controlled current is used. The combination of the above modulation techniques with indirect current control precludes full utilization of the inverter capabilities with regards to its dynamic response. Years of preliminary work on two-level inverters have proven that direct current control techniques show improved dynamics, robustness and stability with excellent static characteristics and a good harmonic distortion behaviour. They can be used universally, they are almost independent from load parameters and they are easy to use.

The SHC algorithm proposed within this thesis is a new and universal direct current control algorithm for multilevel inverter topologies. Various simulations and measurements showed its capability and effectiveness. The principle was fundamentally proved and evaluated qualitatively and quantitatively for current controlled grid connected inverters. A simplification method that reduces the complexity of multilevel systems to a minimum was proposed. The combination of the two different approaches of multilevel inverters with direct current control showed very good and promising results and facilitates opportunities of further research. In summary, the control method shows excellent properties and advantages which are briefly listed below:

- The selection of the controller geometry leads to symmetrical switching frequencies in the three phases.
- The independence from the level count.

- The independence from the topology.
- The easy expandability for secondary control targets such as switching frequency control, spread spectrum control, DC-link balancing, ...
- The design of the controller allows easy implementation on platforms such as microprocessors and FPGAs.
- No adjustment to control non-linear and unbalanced loads.
- The system parameters do not have to be exactly known.
- Exploiting high dynamics with further improvement capability.
- Control of non-sinusoidal signals is possible without any adaptation.
- It is not necessary to know the reference voltage to control the current.
- Particularly in the case of inverters with higher level counts, an estimation of the reference voltage is accurate.
- Functionality in overmodulation mode without adjustments.

Chapter 1 gave a brief introduction on the subject and shortly introduces the background of this thesis. It provides the motivation and the objectives for the research work.

Chapter 2 summarised the state of the art of existing hardware topologies. A qualitative analysis showed that the DCI structure has advantages particularly for converters with low number of levels. On the basis of different decision criteria, the DCI topology was chosen for simulations and measurements within this thesis.

Chapter 3 provided a literature overview and an introduction to current control methods for inverters. Since the proposed algorithm is a space vector based method, some of the existing SVM based algorithms are investigated in more detail. Estimates for converter systems with higher levels showed the necessity of further research.

Chapter 4 showed a selection of existing, state of the art simplification methods for control algorithms with higher levels. A new method is proposed that reduces the complexity of multilevel converters from any level count down to a basic unit cell. The integer based approach allows a optimized implementation on microprocessors and FPGAs.

Chapter 5 explained the working behaviour of the new direct current control method. The "Scalar Hysteresis Control - SHC" method and the seeking algorithm are derived from a purely mathematical and geometrical analysis of an ideal system and is described in detail.

Chapter 6 showed simulation and measurement results which were used to verify the theoretical assumptions made in Chapter 5. A flexible hardware system was introduced and measurements are showing the current controller performance on a two-, three- and five-level inverter system.

Chapter 7 concludes and summarises the thesis, shows the contributions provided by this thesis and gives opportunities and proposals for further research.

7.2 Future Work

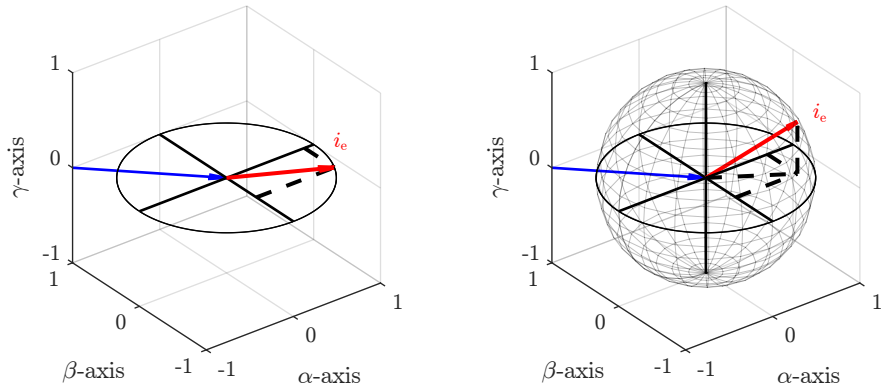
The new direct control method proposed in this thesis offers many continuation topics for future research. The following list describes a selection of relevant subjects:

Secondary Control Properties: In addition to the main control objective of keeping the current within a defined tolerance band, secondary control objectives could be implemented to further improve the quality, behaviour or characteristics of direct control methods. These secondary control targets can be implemented by a suitable variation of the size of the current error tolerance band. The following secondary objectives are of further interest:

- Constant Switching Frequency: The non-constant switching frequency of direct control methods seems, amongst others, disadvantageous for the design of filters. A switching frequency control can adapt the tolerance band width in such a way that the average switching frequency is constant.
- Spread Spectrum: Some applications presuppose a spectrum as widely distributed as possible. The spectrum, which is already distributed when using direct methods, can be further spread by adding a random dithering value on the hysteresis band.
- Compensation of Oscillation: Sometimes inverter switching operations can cause system oscillations e.g. with long shielded cables between

a inverter and the motor driven from that inverter. In order to prevent these oscillations, individual switching operations can be shifted arbitrarily by short-term adaptations of the tolerance band.

Parallelization of Inverters: The parallel connection of converters is used in various applications. For example, modular converter systems are connected in parallel in order to increase the overall power of the system or to actively filter current distortions [70, 71]. The main problems with a parallel connection of converters are the circulating currents and the increasing complexity of the control algorithm. Initial investigations have shown that the simplification method and the control method presented in this thesis can be adapted to be used for these kind of applications. Since the circulating currents appear in the γ component of the current, this can be included in the control method. Figure 7.1a shows a two-dimensional circular surface for the current error as presented in this thesis. If the γ component needs to be considered by the control method the tolerance area becomes spherical. The spherical error geometry to control the $\alpha\beta\gamma$ current error of a parallel connected inverter is shown in Fig. 7.1b. The space vectors selected by the current controller after a tolerance band violation must then be selected in such a way that, in addition to the α and β error, the γ error is also reduced.



(a) Circular current error area (b) Spherical current error area

Figure 7.1: Current error and tolerance bands for $\alpha\beta$ and $\alpha\beta\gamma$ control

Active and Reactive Power Control: The aim in grid connected applications is to regulate the active and/or reactive power supplied to or consumed from the grid. Using a suitable synchronization and power control method, the amplitude and phase for the set-point current can be predetermined and used as input variables for the direct current controller. This implementation is similar to the DPC method.

Torque and Rotationial Speed Motor Control: Similar to grid-connected applications, the amplitude and phase for the set-point current is determined by suitable controllers for torque and speed and used as input variables for the direct current controller. This implementation is similar to the DTC method.

7.3 Publications and Patent Applications of the Author

7.3.1 Results Related to Current Control Techniques for Multilevel Systems

1. M. Schaefer, W. Goetze, M. Hofmann, D. Montesinos-Miracle, A. Ackva, "Three Phase Transformation for Simplified Space Vector Control of Multilevel Inverters", *16th IEEE Workshop on Control and Modeling for Power Electronics, COMPEL 2015*

   Abstract - Multilevel inverters provide numerous advantages compared to standard type inverters, most importantly a line voltage with low harmonic distortion through multiple output voltage levels. The control of such a system with space vector modulation techniques leads to more complex algorithms for determining the correct switching behavior. This paper presents a new three phase transformation with the ability to simplify space vector based control schemes for multilevel inverters. Based on that transformation transistor switching states, redundant switching states and gate signals can easily be determined.

2. M. Schaefer, M. Hofmann, S. Raab, A. Ackva, "Multilevel direct current control for grid connected inverters", *17th European Conference on Power Electronics and Applications, EPE 2015*

   Abstract - One of the most important requirements for grid-connected inverters is an accurate control of the line currents. Applying the

?switched diamond hysteresis control (SDHC)? to multilevel inverters combines the advantages of both techniques and is an enabling step towards a better inverter performance than using state of the art controllers.

3. M. Hofmann, M. Schaefer, A. Ackva, "Optimization of direct current controlled multilevel inverters under distorted conditions" *18^{th} European Conference on Power Electronics and Applications, EPE 2016*

   Abstract - Nowadays current controlled inverters need to be dynamic and robust even under grid disturbances and different grid faults. Besides a robust control method the requirements for the synchronization of the system become more and more important especially when multilevel inverter topologies are used.

4. M. Schaefer, Wolf Goetze, M. Hofmann, F. Bayer, D. Montesinos-Miracle, A. Ackva, "Direct Current Control for Grid-Connected Diode-Clamped Inverters" *IEEE Transactions on Industrial Electronics, Volume: 64, Issue: 4, April 2017*

   Abstract - The accurate control of the line current, robust and dynamic behavior even under distorted grids and other system faults are the most important requirements for grid-connected inverters. Applying direct current control to multilevel inverters combines the advantages of both and is an enabling step towards improved inverter performance. Direct current controllers suffer from high complexity at increased level count, which is resolved by using geometrical principles and simple analytical calculations for switching vector selection within the space vector diagram. The simplified, novel parametric controller concept is scalable to inverters with arbitrary level count, which does not require any switching tables and the new fully symmetric setup guarantees equal switching frequencies among the three phases. The hypotheses are further confirmed on a real hardware test setup on the example of a three-level NPC inverter hardware and a Xilinx development platform. Experimental results prove the expected behavior of the direct current control under various conditions, which shows a general approach to balance the dc-link capacitors of diode-clamped inverters within the theoretical limits and demonstrates the benefits of using field programmable gate arrays as a controller platform.

5. M. Schaefer, M. Hofmann, S. Raab, A. Ackva, "FPGA Based Control of an Three Level Neutral Point Clamped Inverter" *Power conversion and Intelligent Motion Conference, PCIM Europe 2017*

Abstract - The accurate control of the line current, the robustness and the dynamic behavior are major factors when benchmarking grid connected inverters. Due to weak grids even fast reactions on distortions and other system faults are required properties. Direct current control in combination with multilevel inverters could combine the advantages and give opportunities for future systems designs. As the complexity, the speed and the calculation effort increases within those systems very fast data processing is indispensable. To meet the mentioned demands Field Programmable Gate Arrays (FGPAs) are an alternative to state of the art Microcontroller Units (MCUs).

6. M. Hofmann, M. Schaefer, A. Ackva, "Sensor-less Grid Voltage Synchronization of Direct Current Controlled Multilevel Converters" *19th European Conference on Power Electronics and Applications, EPE 17*

   Abstract - The accurate control of the line current, robust and dynamic behaviour even under distorted grids and the behaviour on other faults are important requirements for grid connected inverter systems. This paper presents a sensorless grid voltage determination system in combination with an direct current control method optimized for multilevel inverters.

7. M. Schaefer, M. Hofmann, S. Raab, A. Kraemer, A. Ackva, "Hochdynamisches und robustes Stromregelverfahren für Umrichter unterschiedlicher Topologien" *Elektrische Antriebstechnologie für Hybrid- und Elektrofahrzeuge HdT*

7.3.2 Results Related to Applications for Current Control Techniques

1. M. Hofmann, S. Raab, M. Schaefer, P. Ponomarov, A. Ackva, "Measurements on vehicle to grid application in industrial power grid for peak load reduction", *6th International Symposium on Power Electronics for distributed Generation Systems, Aachen, Germany*

   Abstract - The combination of "electric mobility" and "renewable energy production" heavily demands for energy storage systems. Investigations of technical possibilities to use the stored energy of electric vehicles (EV) and so called plug-in hybrid electric vehicles (PHEVs) for smoothing the grid load and reduce power peaks are inalienable. Within the limits given by the cars battery management system consumption driven charge and discharge signals could be used for effective

integration in V2G systems. This paper will give a detailed overview of a system for bidirectional charging in an industrial grid. First real measurements and test results are given to proof the concept and show the opportunities.

2. S. Raab, M. Hofmann, M. Schaefer, A. Ackva, "V2G-fähige bidirektionale Schnellladestation für Elektrofahrzeuge", *EMA-Nürnberg 2014 Elektromobilitätsausstellung und Fachtagung*

   Abstract - Die ungeregelte, wetterabhängige Einspeisung von Photovoltaikanlagen in das Energienetz sorgt für einen immensen Ausbaubedarf der Elektrizitätsversorgungsnetze. Dieser Ausbau kann durch den gezielten Einsatz von Speichersyste-men stark reduziert werden. Die Untersuchung der technischen Möglichkeiten, um Elektrofahrzeuge und auch Plug-In Hybridfahrzeuge, die über einen enorme Speicherkapazität verfügen, als Speichersysteme einzusetzen, wird somit unabdingbar. Innerhalb der vom fahrzeuginternen Batteriemanagementsystem vorgegebenen Grenzen kann der Fahrzeug akkumulator über verbrauchsgesteuerte Lade- und Entladesignale effektiv in zukünftige V2G-Systeme integriert werden. Um die technischen Möglichkeiten einer solchen Technologie auszuloten, wurde in der Hochschule für Angewandte Wissenschaften Würzburg - Schweinfurt der Prototyp einer V2G- fähigen, bidirektionalen Schnellladestation für Elektrofahrzeuge entwickelt.

3. M. Hofmann, M. Schaefer, A. Ackva, "Bi-directional charging system for electric vehicles", *3rd International Energy Transfer for Electric Vehicles Conference, Nuremberg, Germany*

   Abstract - The combination of "electric mobility" and "renewable energy production" heavily demands for energy storage systems. Investigations of technical possibilities to use electric vehicles (ev) and so called plug-in hybrid electric vehicles (phevs), containing a relevant amount of storage capacity, as storage systems are inalienable. Within the limits given by the car's battery management system consumption-driven charge and discharge signals could be used for effective integration in future V2G systems. This paper will give a detailed overview about a concept for bi-directional charging and first test results.

4. S. Raab, P. Ponomarov, M. Hofmann, M. Schaefer, A. Kraemer, A. Ackva, "Vehicle to Grid Anwendung zur Spitzenlastreduktion in Industrienetzen" *Elektrische Antriebstechnologie für Hybrid- und Elektrofahrzeuge HdT*

7.3.3 Patent Applications

1. Patent Application: M. Hofmann, J. Koch, L. Neumann, M. Schaefer, H. Wiessmann, "REGELUNG EINES DREI-LEVEL WECHSELRICHTERS", *Application Number: 16190787.8-1809*

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Appendix A

Generic DC-link balancing

To demonstrate the easy adaptability to higher level converters a DC-link balancing algorithm for an n-level diode-clamped inverter with $n-1$ DC-link capacitors was derived in [54]. Figure A.1 shows the graphical illustration of the nomenclature used for the derivation of the DC-link balancing of n-level NPC inverters.

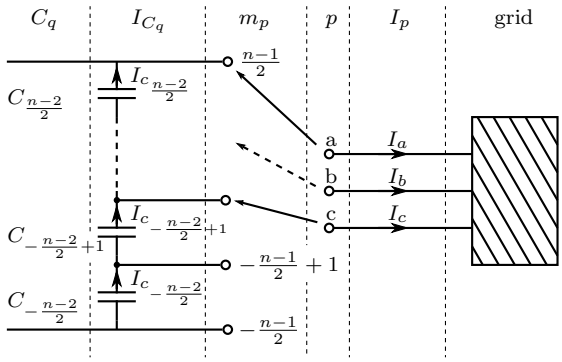

Figure A.1: Graphical illustration of the nomenclature of an n-level NPC inverter

We label the mth nominal output voltage on phase p as $U_{p,m}$:

$$U_{p,m} = \frac{mU_{\mathrm{DC}}}{n-1}, \tag{A.1}$$

where

$$\left\{ m \in \mathbb{Z} + \frac{n-1}{2} \middle| -\frac{n-1}{2} \leq m \leq \frac{n-1}{2} \right\}. \tag{A.2}$$

The current is defined as I_p (positive current flowing out of the inverter) on phase p.

Capacitors are labeled C_q where

$$\left\{ q \in \mathbb{Z} + \frac{n}{2} \middle| -\frac{n-2}{2} \leq q \leq \frac{n-2}{2} \right\}. \tag{A.3}$$

When the output is U_m, there are $\frac{n-1}{2} - m$ capacitors in series to the upper rail and $m - \frac{n-1}{2}$ capacitors in series to the lower rail.

Capacitor C_q supplies a current

$$I_{C,q} = \sum_p I_p \begin{cases} \frac{1}{2} - \frac{m_p}{n-1} & \text{for } q < m_p \\ -\frac{1}{2} - \frac{m_p}{n-1} & \text{for } q > m_p \end{cases} \tag{A.4}$$

$$= \sum_p I_p \left(\frac{1}{2} \operatorname{sgn}(m_p - q) - \frac{m_p}{n-1} \right) \tag{A.5}$$

The DC voltage U_{DC} is split over the capacitors. Each capacitor carries a voltage $U_{C,q}$ such that $U_{\mathrm{DC}} = \sum_q U_{C,q}$. The variance of all the capacitor voltages is

$$\sigma^2(U_C) = \frac{1}{n-1} \sum_q \left(U_{C,q} - \frac{U_{\mathrm{DC}}}{n-1} \right)^2 \tag{A.6}$$

$$= \frac{1}{n-1} \sum_q U_{C,q}^2 - \left(\frac{U_{\mathrm{DC}}}{n-1} \right)^2. \tag{A.7}$$

As the second term is constant, minimizing the variance is equivalent to minimizing the total stored energy in all capacitors

$$E_C = \frac{C}{2} \sum_q U_{C,q}^2. \tag{A.8}$$

The change of energy is given by

$$\frac{d}{dt} E_C = -\sum_q U_{C,q} I_{C,q}. \tag{A.9}$$

For a controller with bounded DC capacitor voltages, no change is required in energy on average over time

$$\langle \frac{d}{dt} E_C \rangle \leq 0. \tag{A.10}$$

We therefore want to minimize $\frac{d}{dt} E_C$ at every timestep. Combining (A.5) and (A.9)

$$\begin{aligned} \frac{d}{dt} E_C =& -\sum_{p,q} U_{C,q} I_p \left(\frac{1}{2} \operatorname{sgn}(m_p - q) - \frac{m_p}{n-1} \right) \\ =& -\frac{1}{2} \sum_{p,q} U_{C,q} I_p \operatorname{sgn}(m_p - q) + U_{\mathrm{DC}} \sum_p I_p \frac{m_p}{n-1}. \end{aligned} \tag{A.11}$$

In a system with disconnected neutral, the total current is zero, i.e. $\sum_p I_p = 0$. As the capacitors are approximately balanced, it is defined that

$$U_{C,q} = \frac{U_{\mathrm{DC}}}{n-1} + \Delta U_{C,q}. \tag{A.12}$$

Then

$$\begin{aligned} \frac{d}{dt} E_C =& \frac{U_{\mathrm{DC}}}{n-1} \left(-\frac{1}{2} \sum_{p,q} I_p \operatorname{sgn}(m_p - q) + \sum_p I_p m_p \right) \\ & - \frac{1}{2} \sum_{p,q} \Delta U_{C,q} I_p \operatorname{sgn}(m_p - q) \\ =& -\frac{1}{2} \sum_{p,q} \Delta U_{C,q} I_p \operatorname{sgn}(m_p - q). \end{aligned}$$

A simple algorithm to drive the capacitors towards the balanced state is therefore to calculate Expression (A.13) for each switching state that produces the output voltage selected by the current controller and to choose the inverter command that maximizes the rate of decrease of the asymmetry.

Appendix B

State Machine

State and transition table of a five-level diode clamped inverter with the main states S_x and the intermediate transitions states T_x:

Table B.1: State Transition Table of 5 Level DCI

S_x, T_x	Switched IGBTs (top to bottom)
S_2	1111 0000
S_1	0111 1000
S_0	0011 1100
S_{-1}	0001 1110
S_{-2}	0000 1111
T_1	0000 1110
T_2	0001 1100
T_3	0001 1000
T_4	0011 1000
T_5	0001 0000
T_6	0111 0000
T_7	0000 1100
T_8	0011 0000
T_9	0000 1000

The state machine used to handle inverter dead-times of a two-, three- and five level inverter are shown in Figure B.1

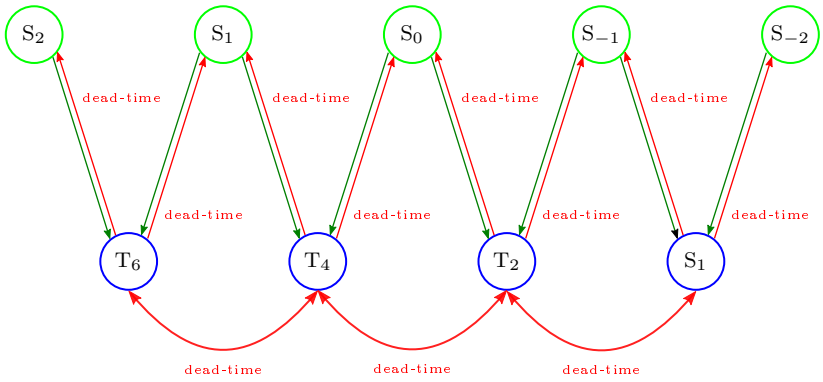

Figure B.1: Stateflow diagram used for two-, three- and five-level Inverter

Appendix C

Experimental Platform

The technical data of the hardware systems are shown in this Appendix.

FPGA Controller Platform

Table C.1: FPGA Controller board

Description	Value
Name/Type	FHWS-XC7A200
FPGA	Xilinx Artix-7 (XC7A200T-2FFG1156C)
Features	1 GB DDR3-SDRAM (800 Mb/s), 2 Gigabit Ethernet Ports, SATA (6 Gb/s), Flash (32 MB), EEPROM (1 MB), SD card slot, 250 IOs (120 LVDS pairs), 4 pairs with 6Gb/s, 12 V supply, 8 User LED and DIP switch, ...

The FHWS-XC7A200 is a development platform not only for research work on converters and control algorithms. The board is designed to be mounted into a 19 inch standard rack system where extension modules can be mounted and connected using a backplane. The FHWS-XC7A200 is a modular, general purpose FPGA based controller platform that allows the user to implement algorithms for any application. The system is designed to speed up complex control algorithms for any converter topology. Extension modules include high-speed voltage and current measurement, digital and analogue I/O expansion, communications interfaces and interface to standard

converters from Semikron as well as to experimental converters designed at the FHWS.

Figure C.1: FHWS FPGA development board

The core of the FHWS-XC7A200 is a XC7A100T FPGA from the Artix family from Xilinx. The FPGA from Xilinx includes:

- 215.360 Logic Cells
- 740 DSP Slices
- 13.140 kb internal Block RAM
- 16 GTP 6,6 Gb/s Transceivers
- 500 I/O Pins

The board includes a set of peripherals that enables it to implement high performance algorithms and to be used as a data logger for testing and evaluation purposes. Large data can be stored using the microSD memory and an optional Sata SSD or HDD. Communication with external devices is possible with two Gigabit Ethernet ports. Additionally, the board supports an ECU interface for connection with dSpace systems. The system backplane supports up to 10 extension cards for the FPGA controller board. It is also possible to extend the system with a second FPGA board on the same backplane with six additional extension slots. Communication and data exchange between the FPGAs is realized over the GTP Transceivers with a data rate up to 6Gb/s. The FHWS-XC7A200 can be programmed and debugged using the Vivado Design Suite software from Xilinx.

Current Measurement Path Components

Current Transducer The current transducer LEM LA 200-P with galvanic separation between the primary circuit and the secondary circuit, a nominal current of 200 A_{rms} and a conversion ration of 1:2000 was used.

AD Converter The AD9259 is a quad, 14-bit, 50 MSPS AD converter. This AD converter operates at a conversion rate of up to 50 MSPS and is optimized for dynamic performance and low power.

Inverter Hardware

Two-Level Skiip

Table C.2: Two-Level Inverter Data

Description	Value
Name/Type	SKiiP 613 GD123-3DUL V3
Supplier	Semikron
DC-link Voltage	900 V
Rated current	400 A
IGBT Blocking voltage	1200 V
DC-link Capacitance	7 mF
Interlock Time	2.3 μs
Maximum Switching Frequency	20 kHz

Three-Level Skiip

Table C.3: Three-Level Inverter Data

Description	Value
Name/Type	3L SKiiP28MLI07E3V1
Supplier	Semikron
DC-link Voltage	750V V
Rated current	100 A
IGBT Blocking voltage	1200 V
DC-link Capacitance	2 mF
Interlock Time	2.6 μs
Maximum Switching Frequency	20 kHz

Five-Level DCI Inverter

Table C.4: Five-Level Inverter Data

Description	Value
Name/Type	5L FHWS-5LDCI
IGBTs	IXYS IXYN100N120B3H1
DC-link Voltage	1800 V
Rated current	75 A
IGBT Blocking voltage	1200 V
DC-link Capacitance	1 mF
Interlock Time	< 2.6 μs
Maximum Switching Frequency	20 kHz

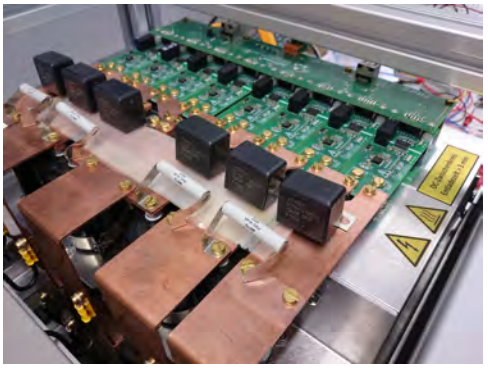

Figure C.2: FHWS five-level diode clamped inverter

Load and Sink

DC Cluster

The high-performance DC cluster is used for the individual and modular bi-directional provision of energy. Due to the modular design, different scenarios can be set-up. The DC cluster consists of four identical modules which can provide voltages up to 1 kV or currents up to 200 A, depending on the interconnection. The main system parameters are:

Table C.5: Parameters of a single DC source from Regatron

Description	Value
Power range	$0 - \pm 20$ kW
Voltage range	0 – 500 V DC
Current range	$0 - \pm 50$ A
Internal resistance range	$0 - 1000$ mΩ
Switchable output capacitance	0.09 mF/0.9 mF

Grid Simulator

The grid simulator can be used to simulate supply networks or machines. The parameters are freely adjustable and the system can specifically simulate disturbances such as, for example, voltage unbalances, short-time breakdowns or distortions due to harmonics. These properties can be used to test inverters for a wide range of applications. The main system parameters are:

Table C.6: Parameters of the grid simulator from Regatron

Description	Value
Output voltage RMS	$0 - 280$ V
Output current RMS	$0 - 72$ A
Power range	$0 - 50$ kVA
Power Factor	$0 \ldots 1$
Output frequency	$0 - 1000$ Hz

Figure C.3: Grid Simulator and DC Cluster