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DOCTORAL THESIS

ANALYSIS AND MODELING OF FILAMENTARY CONDUCTION IN HfO_2-BASED STRUCTURES

Author:
Alberto Rodríguez Fernández

Supervisors:
Dr. Enrique Miranda Castellano
Dra. Mireia Bargalló González

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Effect of the voltage ramp rate on the set and reset voltages of ReRAM devices

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Research paper

Effect of the voltage ramp rate on the set and reset voltages of ReRAM devices

A. Rodriguez-Fernandez [a,*], C. Cagli [b], L. Perniola [b], J. Suñé [a], E. Miranda [a]

[a] Departament d'Enginyeria Electrònica, Universitat Autònoma de Barcelona, Cerdanyola del Vallès, Spain
[b] CEA, LETI, MINATEC Campus, Grenoble, France

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ABSTRACT

The impact of the voltage ramp rate (*RR*) on the set and reset transition voltages of resistive RAM (ReRAM) devices that form part of one transistor-one resistor (1T1R) structures is investigated. Similar expressions for the set and reset voltages as a function of *RR* are found, which indicates a common physical origin. Constant voltage stress experiments were also carried out in order to obtain further insight into the acceleration law behind the formation and dissolution of the filamentary path spanning the oxide film. The obtained results seem to be consistent with the thermochemical model (*E*-model) of dielectric breakdown. The connection between the modification of the set/reset voltages with *RR* and the shifts of the memory map of the device (the so-called hysteron loop) is also discussed.

1. Introduction

It has been reported many times that the voltage ramp rate (*RR*) notably affects the set and reset voltages of HfO_2-based resistive memories [1,2]. This connection has been nicely captured by static as well as by dynamical models for the switching behavior of ReRAM devices [3,4]. A number of studies have revealed that lower *RR* values are in general associated with lower set (V_{SET}) and reset (V_{RESET}) voltages, following a logarithmic relationship [5,6]. In this work, the effect of *RR* was investigated for both the set and reset events separately varying *RR* in four orders of magnitude, from $5 \cdot 10^1$ Vs^{-1} to Vs^{-1} to $5 \cdot 10^4$ Vs^{-1}. It was found that the same empirical law applies for both events, which indicates that the generation and rupture of the conducting filament spanning the oxide film, while keeping their particular features, have a common origin. In order to confirm these results, additional experiments were conducted using constant voltage stress ($RR = 0$). Combining all these findings, an expression for the set time (t_{SET}) as a function of the applied voltage can be established. The corresponding acceleration law for degradation is consistent with the thermochemical model (*E*-model) for dielectric breakdown [7], which relates the applied oxide field to the breakdown of atomic bonds and the appearance of oxygen vacancies. In addition, the effect of *RR* on the memory map of the device (normalized current measured at a very low bias) and its connection with the hysteron loop of the memdiode model for memristive devices [8] was explored. It is shown that the hysteron reflects the modification of the set and reset voltages as a parallel shift of its transition edges, which provides some clues on how to integrate these effects in a compact model representation. Simulation results incorporating all the above discussed issues are also reported here.

2. Experimental details

The devices investigated in this work are 1T1R devices fabricated at LETI (CEA) (see Fig. 1(a)). The MIM structure, sketched in Fig. 1(b), is formed by a 10 nm-thick ALD HfO_2 layer sandwiched between two metal electrodes (Ti and TiN). To prevent irreversible cell breakdown and to control the low resistance state (LRS), an NMOS transistor is used in series with the ReRAM device. The scheme of the Set-up used for RS pulsed operation is shown in Fig. 1(c). The transistor does not play any role for the high resistance state (HRS). The current compliance level (I_C) is adjusted by setting the transistor gate voltage to 1.3 V for set and 4 V for reset condition, being their corresponding I_C levels 130 μA and 3.5 mA, respectively. To activate the switching property a forming step with gate voltage of 1.3 V is required. Quasi-static measurements were performed using the Keithley 4200-SCS semiconductor parameter analyzer equipped with a 4225-RPM PGU (pulse generator unit). *I-V-t* data were obtained using pulsed measurements with pulse widths ranging from 1 μs to 1 ms, which in combination with a ramp step voltage of 50 mV, yields *RR* values ranging from $5 \cdot 10^4$ Vs^{-1} to 50 Vs^{-1}, respectively. Typical *I-V* characteristics for the 1T1R configuration after the forming process are shown in Fig. 2, where fifty cycles were performed with $RR = 50$ Vs^{-1}. The heavy solid line represents the median curve of these cycles. As it can be seen, the devices exhibit bipolar switching with abrupt set and gradual reset transitions. In addition, V_{SET} and V_{RESET} are lower than 0.8 V, which suggests that the devices

* Corresponding author.
E-mail address: alberto.rodriguez@uab.cat (A. Rodriguez-Fernandez).

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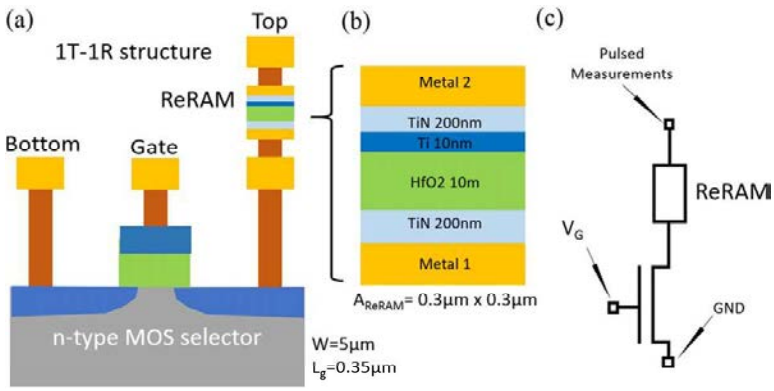

Fig. 1. (a) Schematic representation of the 1T1R structure. (b) Device stack. (c) Scheme of the Set-up used for RS pulsed operation.

investigated here are suitable for low voltage applications [9]. Notice also the transistor action for positive bias $V > 0.75$ V. The limit imposed by the transistor saturation current allows controlling the damage caused to the ReRAM during the set process. As it will be shown below, this damage is also determined by *RR* for identical current compliances. In what follows, the median curve corresponding to fifty complete cycles is shown in all the plots.

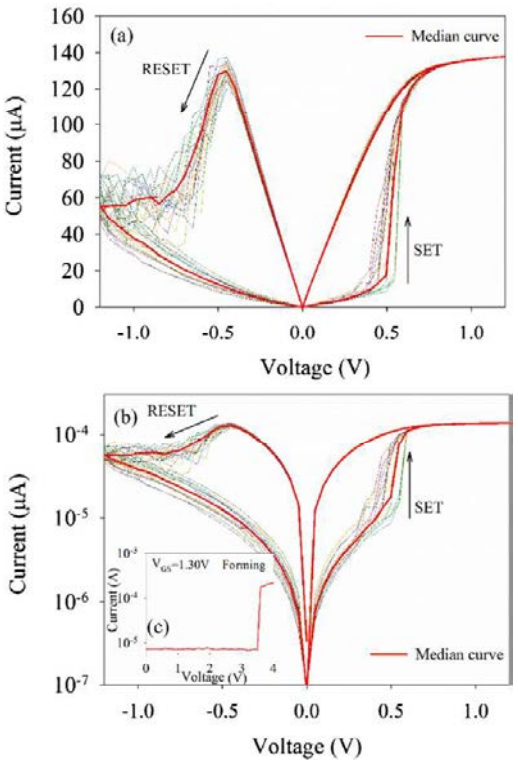

Fig. 2. *I–V* characteristics for quasi-static sweeps ($RR = 50\ \mathrm{Vs}^{-1}$). 50 curves (light solid lines) and its median (heavy solid line) in (a) linear representation, (b) semi-log representation. (c) *I-V* for forming process.

3. Data analysis and discussion

Fig. 3 illustrates the effects of *RR* on the set *I-V* characteristics. In this case, *RR* is modified for the set process only, keeping $RR = 50\ \mathrm{Vs}^{-1}$ fixed during the reset transition. As it can be observed, V_{SET} increases as *RR* increases, with *RR* ranging from $50\ \mathrm{Vs}^{-1}$ to $5 \cdot 10^4\ \mathrm{Vs}^{-1}$. In addition, in spite of the transistor action over the LRS current during the set process [5,10], it is demonstrated that *RR* also determines the maximum current allowed for lower biases. This can be seen as a reduction of the LRS current for higher *RR* values and in consequence as a reduction of V_{RESET} in the negative bias quadrant. From these observations, it is clear that a higher *RR* causes a lower accumulated damage to the structure. Similar results are shown in Fig. 4 for a sequence of *RR* values for the reset process. In this case, the set $RR = 50\ \mathrm{Vs}^{-1}$ remains fixed. It can be observed that V_{RESET} decreases for lower *RR* values. Notice also that there is a difference in the HRS currents but this is a consequence of incomplete resets. Higher negative voltages to completely reset the device can cause irreversible damage to the structure. These trends are well documented and are consistent with thermally activated set and reset mechanisms and with the progressive accumulation of damage [11,12]. A schematic of the memory state acquisition in between increasing pulses is illustrated in Fig. 5(a). In addition to the generation of the dynamic I-V curve, the current flowing through the ReRAM is also measured at a very low positive voltage (@0.1 V) in between the increasing/decreasing voltage pulses. This latest measurement when plotted as a function of the previous applied bias allows obtaining, after a proper normalization, the hysteron loop that represents the memory state of

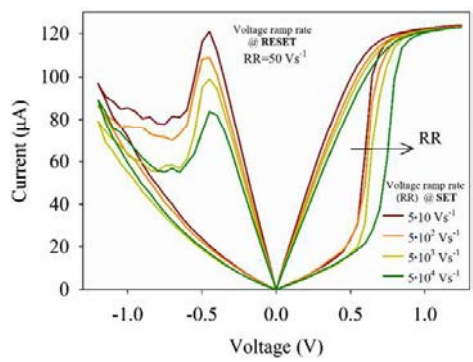

Fig. 3. Measured *I–V* characteristics for different *RR* values during the set process. The reset *RR* is kept constant at $50\ \mathrm{Vs}^{-1}$.

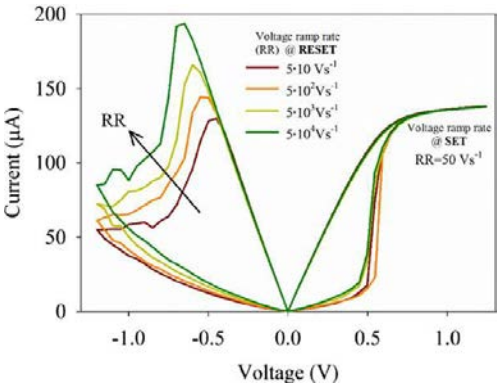

Fig. 4. Measured *I–V* characteristics for different *RR* values during the reset process. The reset *RR* is kept constant at 50 Vs^{-1}.

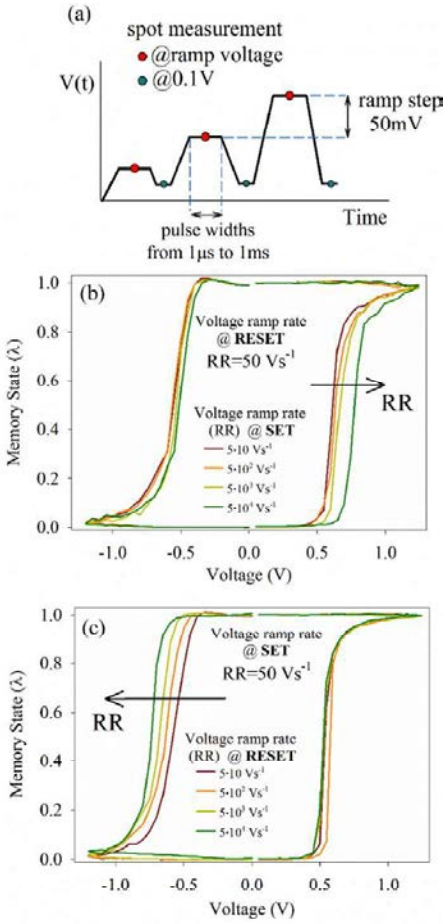

Fig. 5. (a) Schematic of the memory state acquisition in between increasing pulses. Normalized current @0.1 V as a function of the previous applied voltage: (b) set process, (c) reset process.

the device ($0 \le \lambda \le 1$) [8]. The hysteron map was extracted from the experimental data illustrated in Figs. 3 and 4 and represented in Fig. 5(b) and (c), respectively. The effects of RR on the hysteron's transition edges are clearly visible. These results will be used in Section 4 to simulate the I-V curves in connection with the memdiode model for ReRAM devices.

Fig. 6(a) and (b) illustrate the dependences of V_{SET} and V_{RESET} on *RR*. The obtained results can be summarized as follows:

$$V_{SET} = 0.021 \cdot \ln(RR) + 0.39 \quad [V] \tag{1}$$

$$V_{RESET} = 0.021 \cdot \ln(RR) + 0.49 \quad [V] \tag{2}$$

which are consistent with the relationships reported in [13]. It is worth pointing out that the slopes in (1) and (2) obtained by the least squares method (LSM) are identical (0.021) and the difference between the intercepts of about 0.1 V. This observation indicates that the set and reset conditions have a common root beyond the final physical mechanism responsible for the triggering of the switching event.

Constant electrical stress experiments were also performed. In this case, the experiment consisted in switching the state of the device from HRS to LRS (set condition) by means of a constant voltage stress (CVS). The switching from LRS to HRS was induced by a ramped voltage stress. These two stages build up a cycle. 100 cycles were performed per CVS at 5 different set voltages V_{CVS}: 0.45 V, 0.50 V, 0.55 V, 0.60 V and 0.65 V. During the CVS experiment the voltage was applied to the top electrode while the bottom electrode was grounded. The set time (t_{SET}) corresponds to the time required by the device to switch from HRS to LRS. Extrapolating (1) and (2) for a constant voltage, and using

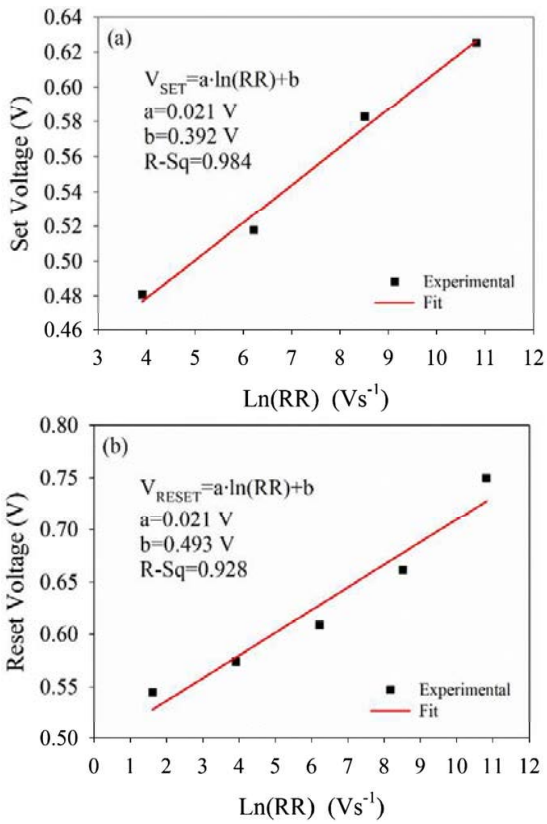

Fig. 6. Experimental data and trend line for (a) V_{SET} and (b) V_{RESET} as a function of *RR*.

the definition $RR = V/t$, we obtain for the set condition under CVS the relationship (see Fig. 7(a)):

$$V_{CVS} = 0.020 \cdot \ln(V_{CVS}/t_{SET}) + 0.41 \quad [V] \tag{3}$$

The slope and intercept in (3) were obtained by LSM and are in close agreement with the values considered in (1) and (2). Solving (3) for t_{SET}, it is found:

$$t_{SET} = 8 \cdot 108 \cdot V_{CVS} \cdot \ exp[-V_{CVS}/0.02] \sim \ exp[-45.27 \cdot V_{CVS}] \quad [s] \tag{4}$$

which is consistent with the thermochemical model of dielectric breakdown with an acceleration voltage factor $\gamma \approx 45.27\ V^{-1}$ (see Fig. 7(b)). For HfO_2, this γ value corresponds approximately to a 1 nm-width material gap along the filamentary path [14]. According to the *E*-model, weak bonding states can be broken by thermal means due to the strong dipolar coupling of defect states with the local electric field in the dielectric [15]. The model also suggest that oxygen vacancies play a fundamental role in the formation of the filamentary path. This is in total agreement with the set and reset processes occurring in ReRAMs.

4. Simulation results

The results obtained in the previous section were included in a recently proposed model for the *I-V* characteristic of voltage-driven memristive devices [8]. Briefly, the memdiode model considers two coupled equations: one for the electron transport based on the diode equation (*I-V*), expressed as:

$$I = (\alpha R)^{-1} W\{\alpha R I_0(\lambda)\ \exp[\alpha(V + R I_0(\lambda))]\} - I_0(\lambda) \tag{5}$$

where α is a fitting constant, R the series resistance, and $I_0(\lambda) = I_{0max}\lambda + I_{0min}(1-\lambda)$ the diode amplitude factor. I_{0max} and I_{0min} are the maximum and minimum values of I_0, respectively. For the memory map (λ-*V*), which controls $I_0(\lambda)$ in (5),

$$\lambda_t = \ \min\{\Gamma^{-}(V_t),\ \max[\lambda_{t-1}, \Gamma^{+}(V_t)]\} \quad t = 1, 2, 3, \ldots \tag{6}$$

is considered, where λ_t and V_t are the discretized values of state variable and input signal, respectively. $\Gamma^{\pm}$ are the ridge functions (hysteron's edges) which can move according to *RR* (see Fig. 5). Fig. 8(a) shows the simulated hysterons as a function of *RR* using expressions (1) and (2). Fig. 8(b) shows the simulated *I-V* curves. Model parameters for the curve shown in Fig. 8(b) are: $R_{on} = R_{off} = 100\ \Omega$ $\alpha_{on} = 1\ V^{-1}$, $\alpha_{off} = 1.49\ V^{-1}$, $I_{0max} = 4 \cdot 10^{-4}$A, $I_{0min} = 2.85 \cdot 10^{-5}$A, $\eta^{+} = 80\ V^{-1}$, $\eta^{-} = 10\ V^{-1}$. Importantly, the simulation results were not optimized since the transistor action was not taken into account for this exercise. As it can be seen, the proposed model is able to qualitatively reproduce the experimental results shown in Figs. (2) and (3).

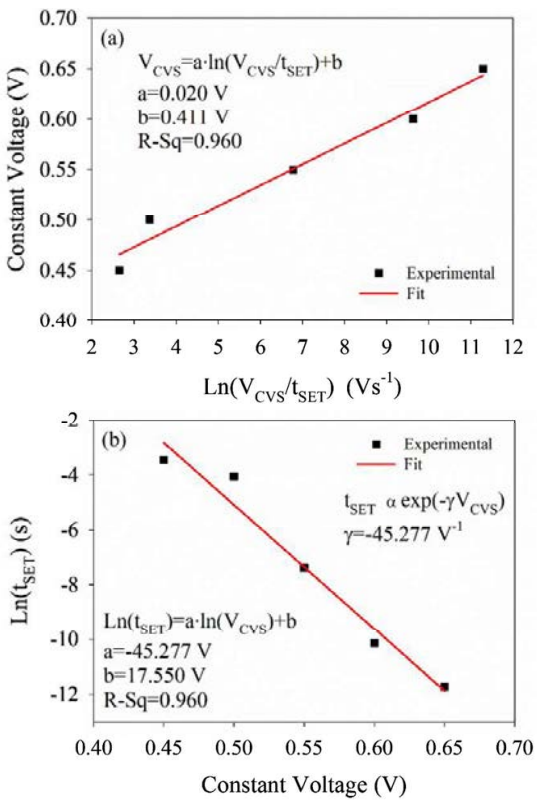

Fig. 7. (a) Constant voltage stress (V_{CVS}) as a function of $\ln(V_{CVS}/t_{SET})$ and (b) $\ln(t_{SET})$ as a function of V_{CVS}. γ is the voltage acceleration factor.

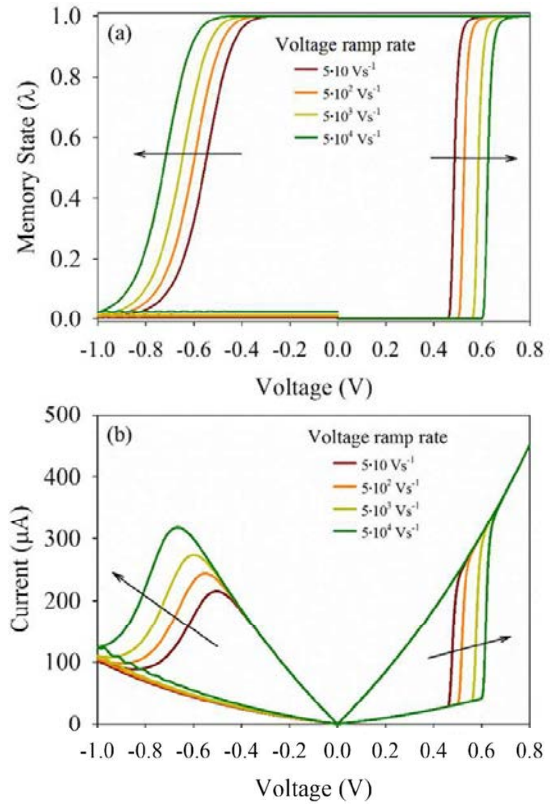

Fig. 8. (a) Simulated memory map (hysteron) as a function of the applied voltage. (b) Simulated *I–V* characteristics for different *RR* values.

5. Conclusions

We have investigated the influence of the voltage ramp rate on the set and reset transition voltages of ReRAM devices. It was shown that they can be described by the same relationship. This seems to indicate a common physical origin for both kind of transitions. Constant voltage stress experiments revealed that the acceleration law behind the formation and dissolution of the filamentary path is consistent with the thermochemical model for dielectric breakdown. Simulation results were also provided demonstrating the feasibility of incorporating the investigated effects in a compact approach such as the memdiode model.

Acknowledgements

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ARTICLE **MER17**

Identification of the generation/rupture mechanism of filamentary conductive paths in ReRAM devices using oxide failure analysis

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Identification of the generation/rupture mechanism of filamentary conductive paths in ReRAM devices using oxide failure analysis

A. Rodriguez-Fernandez [a,*], C. Cagli [b], L. Perniola [b], J. Suñé [a], E. Miranda [a]

[a] Departament d'Enginyeria Electrònica, Universitat Autònoma de Barcelona, Cerdanyola del Vallès, Spain
[b] CEA, LETI, MINATEC Campus, Grenoble, France

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ABSTRACT

Constant (CVS) and ramped (RVS) voltage stress data are combined with the aim of identifying the acceleration law that drives the generation and rupture of filamentary conductive paths in HfO_2-based ReRAM devices. The acceleration factor integral (AFI) method is used to find the equivalency between RVS and CVS in order to compare the SET and RESET events statistics and determine the adequacy of different degradation models frequently considered in oxide failure analysis: voltage power-law, *E*-model, and 1/*E*-model. The obtained results indicate that the *E*-model, with *E* the local electric field, exhibits the lowest dispersion in the acceleration factor values both for the SET and RESET transitions as well as the best overall consistency.

1. Introduction

Understanding the generation and rupture mechanisms of filamentary conductive paths in thin oxide films is of utmost importance for the application of these structures in resistive random access memories (ReRAM) [1]. This not only requires models able to describe the physics behind such events but also statistical tools appropriate for dealing with their intrinsic stochastic nature. The observed randomness is nothing but a consequence of cycle-to-cycle microscopic changes in these conductive paths. In this work, constant (CVS) and ramped (RVS) voltage stress data are conveniently combined with the purpose of identifying the most suitable acceleration law for the formation and rupture of conductive filaments (CF) in HfO_2-based ReRAM devices. The SET event is associated with the transition from the high (HRS) to the low resistance state (LRS), while the RESET event with the transition in the opposite direction. For the investigated devices, these events take place under opposite voltage polarities (bipolar switching). The models considered in this study are the power-law (V^{-n}) model, the *E*-model and the 1/*E*-model, where *V* and *E* are the applied voltage and the local electric field, respectively [2]. In order to compare CVS with RVS data for the SET and RESET events, the acceleration factor integral (AFI) method is considered [3–5]. This method allows assessing the adequacy of different degradation models and selecting the most reliable one in terms of overall consistency. Notice that these acceleration models are frequently applied to oxide layers which have not suffered a previous breakdown event, i.e. a forming process [6]. According to the obtained results, the *E*-model seems to be the best option, at least for the voltage range and ramp rates investigated here. The underlying physical picture for this model (also called thermochemical in oxide reliability analysis [7]) is consistent with current theories relating the formation and dissolution of CFs in ReRAMs with field and temperature-assisted atomic displacements [1]. Failure distributions are commonly used to identify the breakdown mechanism and calculate the acceleration parameters [8]. As it will be shown in this paper, similarly to what happens in oxide failure analysis, time-to-breakdown statistics using CVS in a narrow voltage window (set by practical limitations) does not yield conclusive results. In order to correctly identify the appropriate acceleration law, this information needs to be complemented with analysis arising from alternative approaches such as the AFI method for RVS. Ultimately, this kind identification can give further support or not to any of the proposed physical mechanism ascribed to the formation and dissolution of CFs.

2. Experimental details

The ReRAM cells investigated in this work were fabricated at LETI (CEA) and consist in 10 nm-thick atomic layer-deposited HfO_2 films sandwiched between Ti and TiN metal electrodes. The cell is connected in series with a NMOS transistor, embedding a one transistor-one resistor (1T1R) structure. The NMOS transistor is used to prevent irreversible cell breakdown by limiting the current in the RRAM low resistive state (LRS). An electroforming step with gate voltage $V_G = 1.3$ V is required to activate the switching property of the device. Quasi-static *I-V-t* measurements were performed using a Keithley 4200-SCS semiconductor parameter analyzer equipped with a 4225-RPM PGU (pulse generator

* Corresponding author.
E-mail address: alberto.rodriguez@uab.cat (A. Rodriguez-Fernandez).

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unit). Data were obtained using pulsed measurements ($\Delta V = 50$ mV) with pulse widths ranging from 1 μs to 1 ms corresponding to ramp rates (RR) in the range from 50 V s^{-1} to 50 KV s^{-1}. Fig. 1 shows typical bipolar resistive switching characteristics ($RR = 50$ V s^{-1}). The SET process exhibits a sharp transition. The current compliance level (I_C) is adjusted by setting $V_G = 1.3$ V. Instead, the RESET process is gradual. $V_G = 4$ V is used to avoid any current limitation during the transition. The corresponding I_C levels for both gate voltage conditions are 130 μA and 3.5 mA. The red solid line in Fig. 1 represents the median curve of 50 cycles. In what follows, all the *I-V* curves shown correspond to 50 cycles as well. Notice that V_{SET} and V_{RESET} are lower than 0.8 V, which suggests that the devices investigated here are suitable for low voltage applications [9]. Importantly, in the analysis performed, the voltage and not the electric field was used as the acceleration variable because the width of the insulating gap along the CF (when disrupted) does not necessarily coincide with the nominal oxide thickness.

3. Data analysis and discussion

To illustrate the effects of RR on the SET process, experimental *I-V* characteristics for different RR values are shown in Fig. 2.a. The RESET process is always performed with $RR = 50$ V s^{-1}. Clearly, V_{SET} increases as RR increases. Similar results are illustrated in Fig.2.b for the RESET process: V_{RESET} increases as RR increases. In this case, $RR = 50$ V s^{-1} is kept fixed for the SET process. In close agreement with the results reported in [10–15], V_{SET} and V_{RESET} follow the same logarithmic dependence with RR, which suggests that, beyond their particular features, the SET and RESET events share a common physical origin. The input signal (*V-t*) used to perform cycling at different RR are shown in the insets of Fig. 2. In addition, the SET time (t_{SET}) was determined using CVS. For the sake of clarity, the definitions used in this work for CVS and RVS are shown in Fig. 3. Fig. 4 illustrates a typical CVS experiment for the SET process (positive bias), from A to C with the corresponding RVS for the RESET process (negative bias), beginning at C and ending at A again. The experiment consists in 100 cycles performed per CVS at $V_{CVS} = 0.45$, 0.50, 0.55, 0.60, and 0.65 V. While the lower voltage limit is set by the measurement duration, the upper limit almost coincides with the sudden transition to LRS. Fig. 5.a shows Weibull plots for t_{SET} obtained by CVS. The associated Weibits can be expressed as:

$$\ln(-\ln(1-F)) = \beta \ln(t_{SET}/t_{63\%}) \quad (1)$$

where F is the cumulative distribution function, β the shape factor, and $t_{63\%}$ the scale factor. β values are in the range from 0.95 to 1.1 and increases with the applied voltage as it can be seen in Fig. 5.b and c.

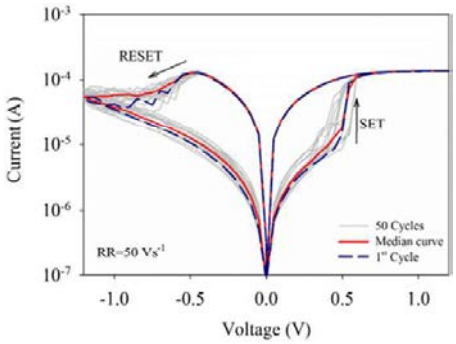

Fig. 1. Bipolar resistive switching behavior during successive set and reset cycles using quasi-static sweeps (RR = 50Vs^{-1}). First cycle (blue dashed line), 50 curves (grey solid lines) and its median (red heavy solid line) are shown.

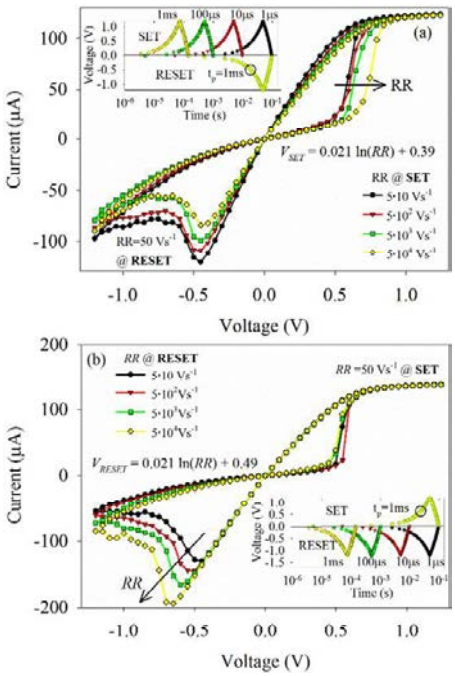

Fig. 2. Measured I-V characteristics for different RR values during: (a) set process and (b) reset process. The reset RR and the set RR are kept constant at 50 V s^{-1}, respectively. Insets show the input signal (V-t) used to perform cycling at different RR. Different width pulse times (t_p) ranging from 1 μs to 1 ms and a ramp step voltage of 50 mV are used.

Fig. 6 shows $t_{63\%}$ fitting results for the three voltage acceleration models under consideration. The *E*-model is expressed in terms of the applied voltage V_{CVS} as [16,17]:

$$E\text{-model}: \ \ln(t_{63\%}) = \ln(a) - \gamma V_{CVS} \quad (2)$$

where γ is the acceleration factor parameter and a a fitting constant. The power-law model reads:

$$\text{Power-law}: \ \ln(t_{63\%}) = b - n \cdot \ln(V_{CVS}) \quad (3)$$

where b is a fitting constant and n the acceleration factor. The 1/*E*-model is often assumed to be related to tunneling through the dielectric film and takes the form:

$$1/E\text{-model}: \ \ln(t_{63\%}) = c + \delta/V_{CVS} \quad (4)$$

where c is a fitting constant and δ the acceleration factor. Acceleration parameters $\gamma \sim 45.8$ V^{-1}, $n \sim 24.9$, and $\delta \sim 13.3$ V are found for the respective CVS fittings (see Table 1).

Fig. 7 shows the effects of RR on V_{SET}. Symbols are experimental data (50 cycles each point) and solid lines are guides to the eye corresponding to five different devices. Dotted, dashed, and dot-dashed lines correspond to simulated results obtained by the AFI method (see the Appendix). Briefly, the method consists in representing CVS data in terms of equivalent RVS data. Alternatively, it can be used to represent RVS data in terms of equivalent CVS. Although the simulated curves are in good agreement with the experimental data (see Fig. 7), deviations for the 1/*E*- and power-law models are detected at the highest RRs. On the contrary, the *E*-model follows a straight-line compatible with the whole set of observations. Reliable CVS data for the RESET transition is difficult to achieve since at the outset of the experiment the

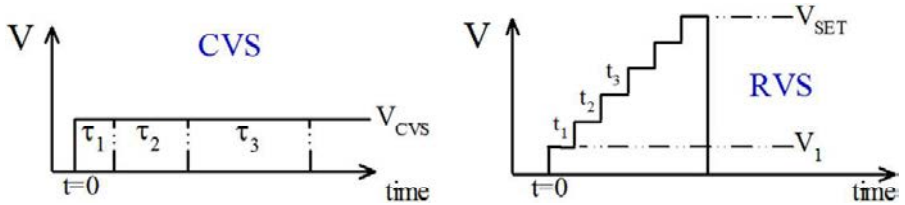

Fig. 3. Schematic for the different stress modes used in this report. CVS experiment (left) and the RVS experiment (right).

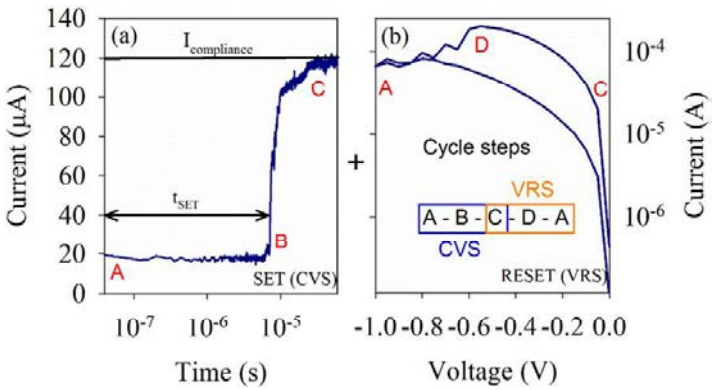

Fig. 4. Typical CVS experiment. A cycle is formed by two steps. Firstly, the set process (a) is performed by means of a CVS, from A to C. Subsequently, the reset process (b) is induced by a voltage ramp, from C to A.

device needs to be in LRS. No clear behavior was observed in that case. In order to complete the analysis, Fig. 8 shows statistical plots for V_{SET} and V_{RESET} obtained by RVS. In this case:

$$\ln(-\ln(1-F)) = \beta(V_{SET} - V_{SET,63\%}) \quad (5)$$

Slopes $\beta \approx 22$ and $\beta \approx 35$ are found for V_{SET} and V_{RESET}, respectively. The insets show lower V_{SET} and V_{RESET} dispersions for higher *RR*s. Again, the AFI method provides the connection between these distributions and the acceleration factors for each degradation model. The results are reported in Table 1. As a first observation, notice that the acceleration factor γ for the *E*-model seems to have the lowest dispersion compared with the corresponding parameters in the 1/*E*-model and power-law model. This indicates full consistency among CVS, RVS SET, and RVS RESET data. Importantly, notice that the standard plot t_{SET} vs V_{CVS} does not yield such conclusive results since the three models are consistent with the experimental data (see Fig.9.b). Recall that the voltage observation window is very narrow since we are dealing with a formed oxide. In oxide reliability analysis the *E*-model (or thermochemical model) assumes that weak bonding states are broken by thermal

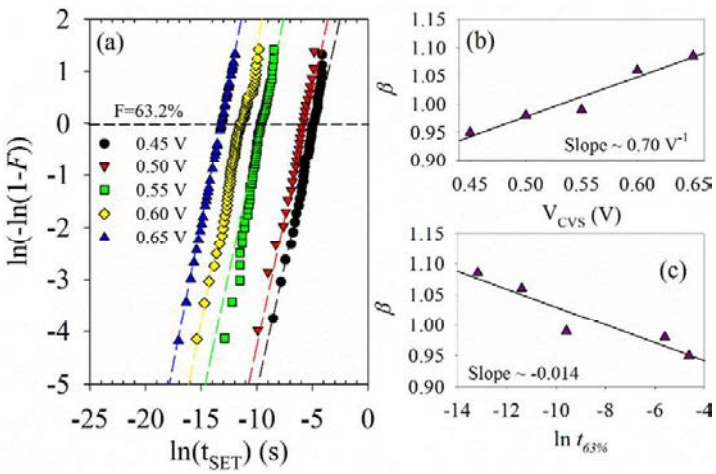

Fig. 5. (a) t_{SET} distributions for constant stress voltages ranging from 0.45 to 0.65 V. Weibull slopes are shown as a function of (b) V_{CVS} and (c) $\ln(t_{63\%})$.

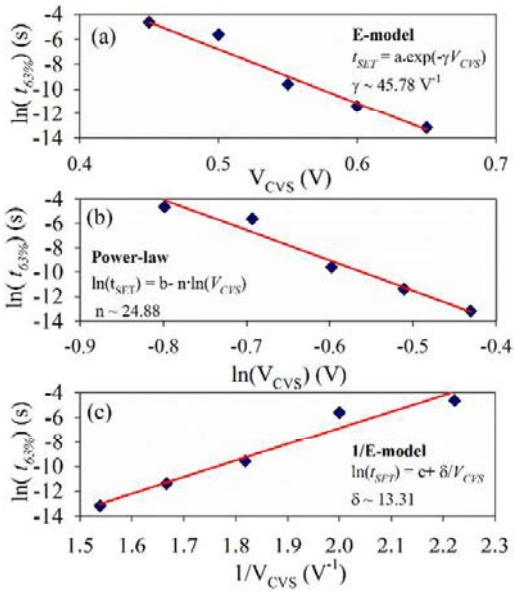

Fig. 6. $\ln(t_{63\%})$ values extracted from CVS experiments plotted as a function of the stress voltage (V_{CVS}) for different degradation models: (a) *E*-model, (b) power law and (c) 1/*E*-model.

means due to the strong dipolar coupling of defect states with the local electric field in the dielectric [7]. Although this mechanism is difficult to conceive for the RESET process, the model also suggests that displacement of oxygen vacancies play a fundamental role in the generation of CFs. At the root of this model is the Kramer's escape rate across a barrier [18] which also describes the ion hopping (redox) mechanism in resistive switching devices [19]. In other words, the connection between the thermochemical model and the set and reset processes resides in that they are all expressed by similar exponential relationships in which the electric field acts as the acceleration variable.

4. Conclusions

By means of a thorough analysis of CVS and RVS data obtained from ReRAM devices in 1T1R structures, it was shown that while standard oxide failure analysis techniques are not able to discriminate among different degradation models, the combination of these techniques by means of the AFI method allows to do so. In summary, it was found that the *E*-model (or thermochemical model in oxide reliability analysis) seems to be the best option for describing the reversible breakdown dynamics of our films. Two issues need to be taken into account: first, the acceleration models were applied to a formed oxide layer, not a fresh one, and second, the width of the switching gap along the conductive filament is unknown, so that the local electric field can be significantly different from the average electric field.

Table 1
Parameters extracted from *E*-model, Power-law and 1/*E*-model fitting for CVS, set (RVS) and reset (RVS) experiments.

	E-model	Power-law	1/*E*-model
CVS	$\gamma = 45.78$	$n = 24.88$	$\delta = 13.31$
SET	$\gamma = 41.17$	$n = 28.28$	$\delta = 15.04$
RESET	$\gamma = 44.26$	$n = 31.01$	$\delta = 14.09$

Acknowledgements

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Appendix A. Appendix

The AFI method is used to transform CVS data (V_{CVS}, t_{SET}) into its equivalent RVS data (V_{SET}, RR). Following [3], t_{SET} can be expressed as (see Fig.3):

$$t_{SET} = \sum_k \tau_k \tag{6}$$

where τ_k are the stress time for each voltage step V_k.

$$\tau_k = \Delta t_k \cdot A_f \tag{7}$$

where A_f is the acceleration factor and Δt_k the stress time per step during RVS. For the three models investigated here:

$$A_f(\text{E-model}) = \exp(\gamma[RR \cdot t - V_{CVS}]) \tag{8}$$

$$A_f(\text{power-law}) = \left(\frac{RR \cdot t}{V_{CVS}}\right)^n \tag{9}$$

$$A_f(1/\text{E-model}) = \exp\left(\delta\left[\frac{1}{V_{CVS}} - \frac{1}{RR \cdot t}\right]\right) \tag{10}$$

γ, n and δ are the corresponding acceleration factors. Converting the sum (6) into an integral with limits $t = 0$ and $t = t_{SET}$ yields:

$$t_{SET} = \frac{\exp(\gamma \cdot (RR \cdot t_{SET} - V_{CVS}))}{\gamma \cdot RR} \tag{11}$$

$$t_{SET} = \frac{V_{CVS}}{RR \cdot (n+1)}\left(\frac{RR \cdot t_{SET}}{V_{CVS}}\right)^{n+1} \tag{12}$$

$$t_{SET} = \exp\left(\frac{\delta}{V_{CVS}}\right) \cdot \left(\exp\left(\frac{-\delta}{RR \cdot t_{SET}}\right) t_{SET} - \frac{\delta \cdot \Gamma\left[0, \frac{\delta}{RR \cdot t_{SET}}\right]}{RR}\right) \tag{13}$$

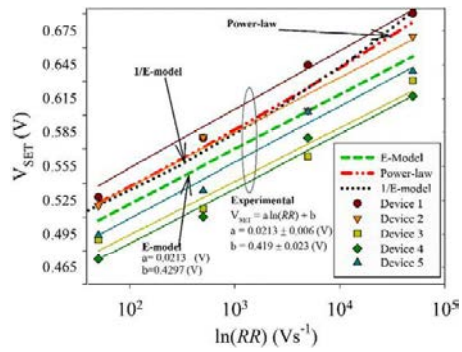

Fig. 7. V_{SET} as a function of RR for five different devices. Each solid line corresponds to the same device. Model results for the *E*-model, 1/*E*-model and power-law model are represented by dashed, dashed dotted, and dotted lines, respectively.

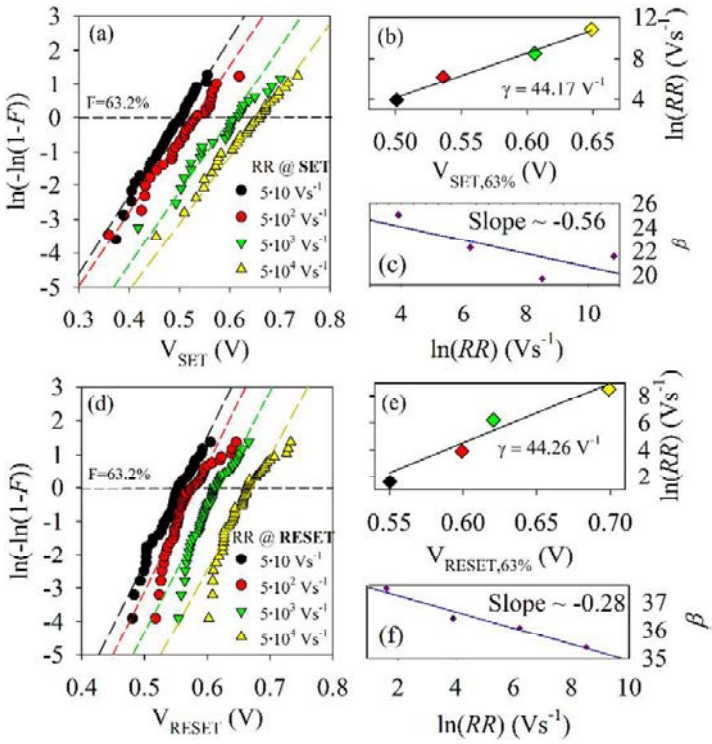

Fig. 8. (a) V_{SET} and (d) V_{RESET} distributions for ramp rates ranging from $50Vs^{-1}$ to $50KVs^{-1}$. (b) $V_{SET,63\%}$ and (e) $V_{RESET,63\%}$ values plotted versus the ramp rate demonstrating the suitability of the thermochemical model with an acceleration voltage factor $\gamma \sim 44.17\ V^{-1}$ and $\gamma \sim 44.26\ V^{-1}$, respectively. (c) and (f) Slopes as a function of the *RR*.

for the *E*-model, power-law, and 1/*E*-model respectively. Γ in (13) is the incomplete gamma function. Now, using the fitting constants reported in Fig.6, the relationships between V_{SET} and *RR* can be calculated from:

$$V_{SET} = \frac{\ln(RR)}{\gamma} + \frac{\ln a + \ln\gamma}{\gamma} \tag{14}$$

$$V_{SET} = \exp\left(\frac{\log(RR\cdot(n+1))}{n+1}\right)\cdot \exp(b/(n+1)) \tag{15}$$

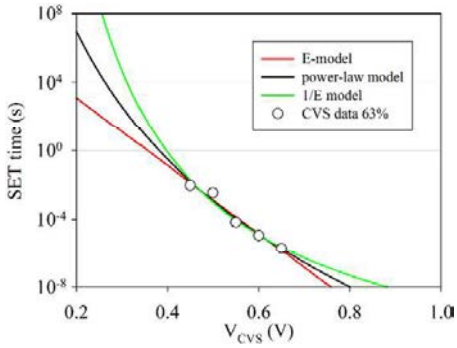

Fig. 9. Projection of set time for a CVS failure percentiles for the *E*-model, 1/*E*-model and power-law model. The symbols refer to the $t_{63\%}$ by multiples CVS.

$$\ln\left[V_{SET}\cdot \exp\left(\frac{-\delta}{V_{SET}}\right) - \delta\cdot\Gamma\left[0,\frac{\delta}{V_{SET}}\right]\right] = c + \ln RR \tag{16}$$

These expressions are represented in Fig.7. Expression (16) needs to be solved numerically.

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Resistive switching with self-rectifying tunability and influence of the oxide layer thickness in $Ni/HfO_2/n^+$-Si RRAM Devices

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Resistive Switching with Self-Rectifying Tunability and Influence of the Oxide Layer Thickness in Ni/HfO_2/n^+-Si RRAM Devices

Alberto Rodríguez-Fernández, Samuel Aldana, Francesca Campabadal, Jordi Suñé, *Fellow, IEEE*, Enrique Miranda, *Senior Member, IEEE*, Francisco Jiménez-Molinos, Juan Bautista Roldán, and Mireia Bargallo Gonzalez

***Abstract*— The impact of the dielectric thickness, forming polarity, and current compliance on the self-rectifying current–voltage (*I–V*) characteristics of Ni/HfO_2/n^+-Si resistive random access memory (RRAM) devices was investigated. The obtained results indicate that these three aspects not only play a role in the postforming currents but also affect the switching properties of the devices. In the case of 5-nm-thick oxide devices, a self-rectifying ratio of about three orders or magnitude is observed after substrate injection forming (SIF) with current compliance below 500 μA. However, similar devices subjected to gate injection forming (GIF) do not exhibit such rectifying feature. This distinctive behavior for SIF is ascribed to the formation of a Schottky-like contact in between the Ni-based conducting filament and the semiconductor electrode. For 20-nm-thick oxide devices, the forming voltage under GIF and the subsequent dielectric degradation are higher than for thinner oxide layers, resulting in a less resistive state, and a negligible role of the referred Schottky barrier. The effect of the temperature on the diffusion of the Ni ions that form the conducting path is also discussed.**

***Index Terms*— HfO_2, memristor, resistive switching (RS), resistive random access memory (RRAM).**

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A. Rodríguez-Fernández, J. Suñé, and E. Miranda are with the Departamento Enginyeria Electrònica Edifici, Universitat Autònoma de Barcelona, 08193 Bellaterra, Spain (e-mail: alberto.rodriguez@uab.es; jordi.sune@uab.es; Enrique.miranda@uab.es).

S. Aldana, F. Jiménez-Molinos, and J. B. Roldán are with the Departamento de Electrónica y Tecnología de Computadores, Facultad de Ciencias, Universidad de Granada, 18071 Granada, Spain (e-mail: samaldana@ugr.es; jmolinos@ugr.es; jroldan@ugr.es).

F. Campabadal and M. B. Gonzalez are with the Institut de Microelectrònica de Barcelona, IMB-CNM (CSIC), 08193 Bellaterra, Spain (e-mail: francesca.campabadal@csic.es; mireia.bargallo.gonzalez@csic.es).

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I. Introduction

RESISTIVE random access memory (RRAM) is one of the most promising technologies for nonvolatile memory devices due to its significant advantages concerning low power consumption, fast switching speed, high scalability, and 3-D integration feasibility over the widely used silicon-based flash memories [1]–[6]. However, one major issue that requires serious attention is the occurrence of multiple sneak paths between RRAM cells when placed in cross-bar array architectures. This can lead to severe readout errors [4], [7], [8]. To overcome this problem, an additional selector device, such as a rectifying diode or pass transistor needs to be integrated into each memory cell to suppress the crosstalk effect [8], [9]. This selector, however, significantly increases the unitary cell size and enhances the fabrication process complexity [10], [11]. In last years, an alternative solution to the use of a selector device, consisting in a RRAM cell with intrinsic self-rectifying properties, has emerged [10]–[16]. In this regard, several works have reported resistive switching (RS) behavior in CMOS compatible Ni-based HfO_2/n^+-Si [10]–[13] or HfO_2/n^+Ge [14] structures presenting Schottky-diode behavior, i.e., asymmetric electron transport.

The origin of the self-rectifying conduction characteristics in RRAM devices is often associated with the formation of nanocontacts between the conducting filaments (CF) and the electrodes. It is widely accepted that the unipolar RS behavior of Ni/HfO_2/n^+-Si devices relies on the formation and rupture of these oxygen vacancy atomic bridges and the subsequent Ni diffusion/migration from the metal electrode towards the bottom electrode [13], [17], [18]. The CF dissolution is often ascribed to thermally enhanced diffusion induced by Joule heating effects [19]–[22]. In addition, the forming polarity [23] and current compliance [17], [18] are known to significantly affect the size and composition of the CFs, which in turn determines the self-rectifying behavior.

In this paper, an in-depth investigation of the low-resistive state (LRS) currents and switching properties of Ni/HfO_2/n^+-Si devices with HfO_2 thickness ranging from 5 to 20 nm

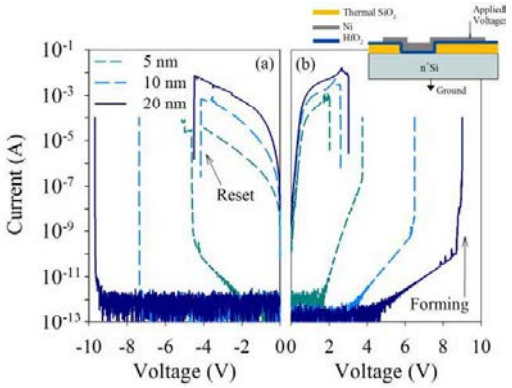

Fig. 1. *I–V* characteristics corresponding to Ni/HfO_2/n^+-Si devices with three different dielectric thicknesses: 5, 10, and 20 nm. The *I–V* curves correspond to a forming process with $I_C = 100\ \mu$A under (a) negative and (b) positive polarity and the subsequent LRS characteristics measured under the same polarity. The inset shows a schematic representation of the device cross section.

is performed. Special attention is given to the influence of the forming polarity and current compliance on the post-forming characteristics. The analysis carried out sheds light on the microscopic nature and properties of the CF pathway and the associated electron transport mechanism, providing a deeper understanding of the switching processes behind self-rectifying RRAM cells.

II. Experimental Details

Ni/HfO_2/n^+-Si devices were fabricated on (100) n-type CZ silicon wafers with resistivity between 0.007 and 0.013 $\Omega \cdot$cm following a field isolated process. After a standard wafer cleaning, a wet thermal oxidation process was carried out at 1100 °C leading to a 200-nm-thick SiO_2 layer. This field oxide was patterned by photolithography and wet etching. Prior to the HfO_2 deposition, a cleaning in H_2O_2/H_2SO_4 and a dip in HF (5%) were done. The HfO_2 layers with thickness ranging from 5 to 20 nm were grown by atomic layer deposition at 225 °C using TDMAH and H_2O as precursors, and N_2 as carrier and purge gas. The 200-nm-thick Ni electrode was deposited by magnetron sputtering and patterned by a lift-off process. The fabricated devices are square cells of $5 \times 5\ \mu m^2$. A schematic representation of the device cross section is shown in the inset of Fig. 1(b).

Current–voltage (I–V) measurements were performed using an HP-4155B semiconductor parameter analyzer. The voltage was applied to the top Ni electrode, while the Si substrate was grounded. During the forming step, the current was limited to prevent the irreversible breakdown of the dielectric material. In order to evaluate the influence of the current compliance on the LRS current, different limiting values (I_C) in the range 100 μA–10 mA were tested. In spite of parasitic effects like current overshoots exist during the set transient, especially for low current compliances, for the large current compliances used in this paper, parasitic overshoots likely play a minor role. Further experimental details about the switching properties of these devices can be found in [24]–[26].

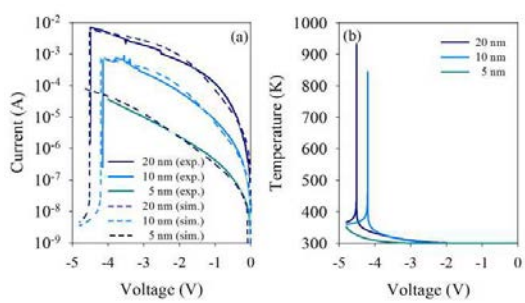

Fig. 2. (a) Current versus applied voltage for RRAMs with different oxide thickness. Experimental and simulated curves are shown. (b) Maximum temperature versus applied voltage for the simulations shown in Fig. 1(a).

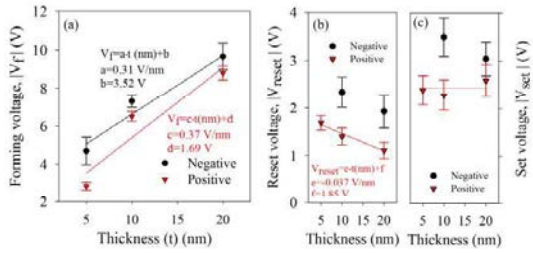

Fig. 3. (a) V_f as a function of the HfO_2 thickness (t) under both polarities, where 10 devices for each condition were measured. (b) V_{reset} and (c) V_{set} as a function of the HfO_2 thickness (t) under positive and negative unipolar switching operation. For each case, the forming was done under the same polarity as the set and reset curves. The current compliance employed during forming and set processes was $I_C = 100\ \mu$A. The values have been calculated from the results of 50-RS cycles in 10 different devices, where 20 cycles were first performed to stabilize the sample. The error bar represents the standard deviation.

III. Results and Discussion

A. Resistive Switching Assessment

In this section, the unipolar RS behavior of Ni/HfO_2/n^+-Si devices with oxides thickness of 5, 10, and 20 nm is presented and discussed. Fig. 1 shows typical I–V curves corresponding to a forming process with $I_C = 100\ \mu$A and the subsequent LRS characteristics measured under the same forming polarity. As shown in Fig. 1, and as expected, the forming voltage (V_f) increases with the HfO_2 thickness following a linear trend with slope ~0.3 V/nm [see Fig. 3(a)]. This breakdown strength is in close agreement with published results for HfO_2 [27]. In addition, Fig. 1 shows that in the case of 5-nm-thick oxides, the LRS current under negative stress polarity is not high enough to initiate a reset transition through Joule heating. Simulations results for the reset process using the macroscopic model developed in [20], [21], and [28], which includes filamentary transport with quantum effects, indicate that the temperature reached in the CF of the 5-nm-thick oxide device is significantly lower than in the rest of the devices [see Fig. 2(a) and (b)]. Therefore, the needed temperature to trigger the reset process it is not achieved for the 5-nm device formed under negative bias.

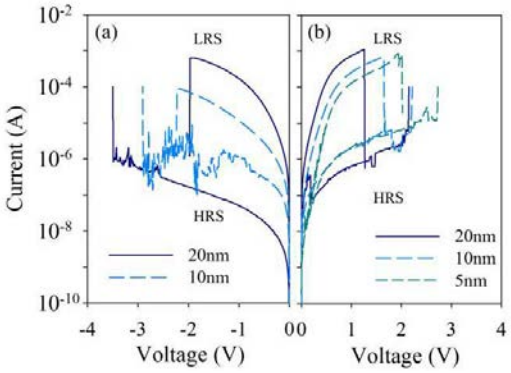

Fig. 4. Typical unipolar RS curves under (a) negative and (b) positive polarity for different HfO_2 thickness. In each case, the forming process was performed under the same polarity of the switching curves. The current compliance employed in the forming and set processes was $I_C = 100\ \mu$A.

In the case of 20-nm-thick HfO_2 layer, higher current levels are observed for both polarities [24], [25], [29], which favor the reset process. The higher LRS currents for thicker oxide films can be explained by the higher V_f required to activate the switching property of the device. It is surmised, therefore, that the larger dissipated power during the set process gives rise to an increased dielectric degradation [30]. Furthermore, higher reset voltages (V_{reset}) are observed in this first cycle than after the RS stabilization. A remarkable result is the observation that V_{reset} slightly decreases with the increase of the HfO_2 thickness with a coefficient $\sim$0.04 V/nm [Fig. 3(b)]. This dependence can be attributed to the higher LRS currents in thicker layers, which likely accelerates the thermochemical dissolution of the CF. However, no clear correlation of the set voltage (V_{set}) with the oxide thickness is detected [Fig. 3(c)], suggesting that after the reset process a partial dissolution of the CF at the HfO_2/n^+-Si interface takes place. As a consequence, the CF would need to be locally reconstructed instead of fully rebuilt [31]. Finally, it is worth noting that a decrease of the HfO_2 thickness implies a reduction of the memory window between LRS and HRS [31], this reduction being more significant for negative than for positive biases. Fig. 4 shows the typical RS behavior of our devices after sample stabilization (20-dc cycles). After these few cycles, a better control of the switching properties is achieved [25], [32], [33]. Remarkably, the I–V characteristics are nonpolar for 10- and 20-nm-thick HfO_2 layers in the sense that RS is observed under both polarities. On the contrary, the 5-nm-thick oxide devices only exhibit positive unipolar switching. It is worth mentioning that in both polarities abrupt resets are obtained due to thermally activated processes induced by Joule heating.

B. Impact of the Thickness and Forming Polarity on the Self-Rectifying Characteristics

In order to assess whether the current asymmetry for both polarities was induced by the forming step or is an intrinsic attribute of the conduction mechanism through the CF, the impact of the forming polarity on the postforming I–V characteristics was investigated. Fig. 5 shows the postforming LRS curves for both polarities in devices with 5-, 10-, and 20-nm HfO_2 thickness when a forming process with $I_C = 100\ \mu$A is performed under 1) negative polarity [gate injection forming (GIF)] and 2) positive polarity [substrate injection forming (SIF)]. The voltage ramps were stopped in this case at ± 1 V in order not to damage or alter the CF morphology.

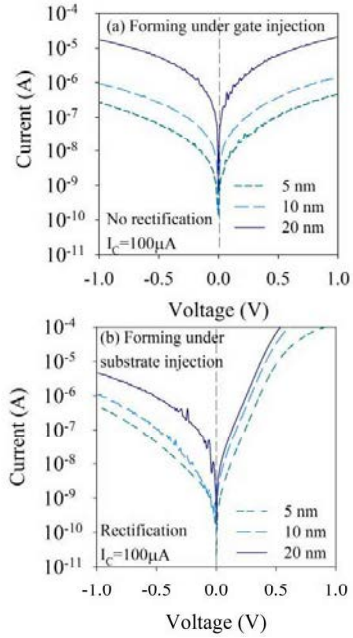

Fig. 5. I–V curves obtained after (a) negative forming (GIF) and (b) positive forming (SIF) for devices with 5-, 10-, and 20-nm HfO_2 thickness.

In the GIF case [Fig. 5(a)], it is observed that the current is symmetric with respect to the applied bias polarity and that it increases with the dielectric thickness. This current increase can be explained by the higher dielectric degradation induced by the required higher forming voltages. However, in the SIF case [Fig. 5(b)], a self-rectifying behavior is clearly observed with the reverse current being partially reduced by more than two orders of magnitude at ± 0.5 V. This current asymmetry is more pronounced for the 5-nm-thick case. The different behavior observed in Fig. 5(a) and (b) points out the impact of the forming polarity on the CF electron transmission properties. In this regard, the conduction characteristics after GIF can be understood using the quantum model for filamentary conduction developed in [34], while the curves after SIF require an additional rectifying element. This latest behavior seems to indicate the formation of a Schottky-like barrier between the metallic CF and the semiconductor electrode [14]–[16]. It is known that the presence of Ni in the dielectric can lead to Ni-based CFs and that they can be affected by the metal cation migration driven by the electric field and temperature

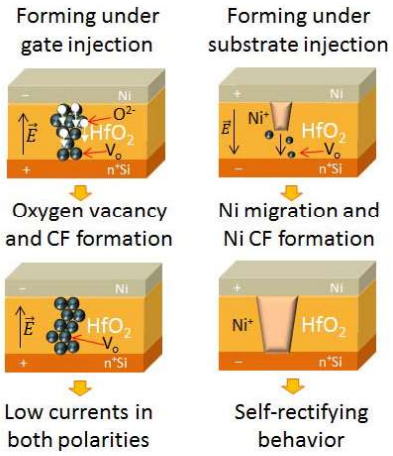

Fig. 6. Schematic representation of the sequence of CF formation for the studied Ni/5-nm-HfO_2/n^+-Si under (left) gate injection and (right) SIF processes with $I_C = 100\ \mu$A.

enhanced metal diffusion [35]–[38]. Recently, the impact of the forming polarity on the Ni electromigration process in TiN/HfO_2/Ni-silicide structures has been reported [39]. Larger Ni concentration in the dielectric was observed after a forming process with negative biased TiN electrodes than for positively biased, suggesting the impact of cation migration on the Ni-based CF formation [35]–[38]. Similarly, for Cu electrodes, metal cation migration has also been detected leading to Cu-based CFs [38], [40]. Notice that the I–V characteristics of Cu-based RRAM devices can exhibit a self-rectifying behavior as well [15], [16]. With the aid of simulations [20], [21], [28], we were able to extract the CF size needed to fit the forward regime of the curves shown in Fig. 5(b). The filaments were assumed to have truncated-cone shape with parameters (lower radius and upper radius): (19.5 and 18 nm) for $t_{ox} = 20$ nm, (9 and 4 nm) for $t_{ox} = 10$ nm, and (3 and 1 nm) for $t_{ox} = 5$ nm.

Fig. 6 shows a schematic representation of the CF formation in the studied Ni/HfO_2 (5 nm)/n^+-Si devices under GIF and SIF processes with $I_c = 100\ \mu$A. In both cases, oxygen atoms are expected to be displaced by the electric field generating oxygen vacancy rich paths [13]. However, in the case of SIF, Ni metallization of the percolation path is more favorable than in GIF due to cation migration [36]–[39]. In this latest case, a self-rectifying behavior is detected [see Fig. 5(b)], suggesting the formation of Ni-based CFs. In addition, in previous work on TiN/TaN/HfO_2-based MOSFETs [23], it was shown that Ta/Ta^+ metal filament formation of the breakdown path only takes place under substrate injection stress [23]. It is worth mentioning that in thicker layers, higher degradation occurs, being more favorable the thermal diffusion of Ni into the dielectric in both forming polarities.

C. Schottky-Diode Behavior

The study of the temperature dependence of the I–V characteristics in the LRS is a useful technique to evaluate

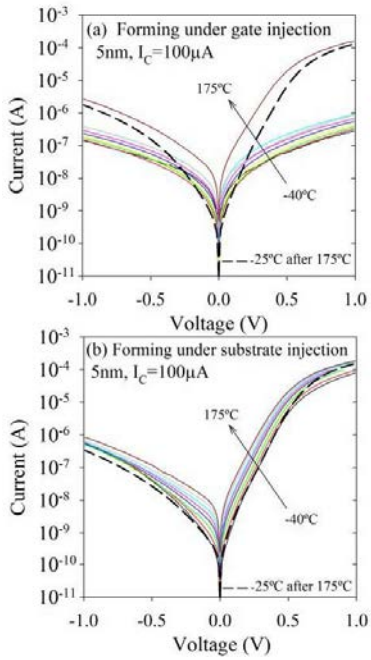

Fig. 7. Temperature dependence for I–V curves obtained after (a) negative forming (GIF) and (b) positive forming (SIF) for two different devices with 5 nm-thick HfO_2. The different curves have been measured with the sequence: −40 °C, −10 °C, 25 °C, 50 °C, 75 °C, 100 °C, 125 °C, 150 °C, 175 °C, and 25 °C again (dotted line).

the dominant conduction mechanism in this regime and gets further insight into the nature/size of the CF. The analysis will be focused on the 5-nm HfO_2-based devices, since this case exhibits the biggest differences in the LRS characteristics after GIF and SIF. Fig. 7 shows the impact of temperature on the postforming I–V characteristics after (a) GIF and (b) SIF. The measurements were performed in the temperature range from −40 °C to 175 °C. At the end of the experiment, the temperature was decreased again to 25 °C to perform the last I–V measurement with the purpose of evaluating the impact of the electrical stress and ambient temperature on the CF morphology. The experimental results show that for both injection polarities the LRS current increases with temperature. In the case of GIF [Fig. 7(a)], the current increases in a temperature range up to 150 °C suggesting the contribution of the quantum point contact conduction for atomic-sized constrictions [34], [41], In these constrictions, the first quantized subband behaves as a potential barrier for the transit of electrons, which is temperature dependent [34], [41]. This behavior has been recently observed in Ni/20 nm-HfO_2/n^+-Si devices under GIF and modeled taking into account the atom-sized aspect of the constriction [21], [22]. However, it is worth emphasizing that the almost symmetric conduction with respect to the applied bias after GIF is not observed when the temperature is raised to 175 °C. At this temperature, pretty similar self-rectifying I–V characteristics like those obtained

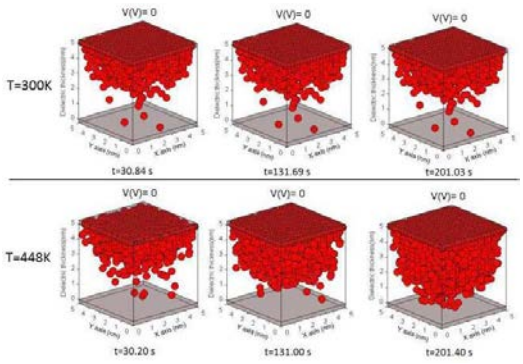

Fig. 8. Simulation of the RRAM under study for a null electric field for two different temperatures. Ni atoms are shown in red. The Ni ions movement in addition to oxidation/reduction reactions are described by means of a kinetic Monte Carlo algorithm coupled with the self-consistent solution of the 3-D Poisson and heat equations. The ions temporal evolution is due to diffusion since no external voltage is applied and, therefore, Ni ion field driven drift is negligible. At higher temperatures diffusion lets Ni ions go deeper in the dielectric from the Ni electrode where most of them are generated.

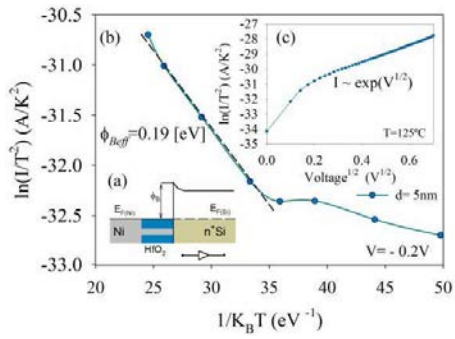

Fig. 9. (a) Schematic of the energy diagram of the Schottky barrier between the Ni-based CF and the n^+-Si substrate for Ni/5-nm-HfO_2/n^+-Si devices after SIF with $I_C = 100\ \mu$A. (b) Temperature dependence of reverse current at −0.2 V. (c) Reverse current of LRS characterized by the Schottky emission model.

under SIF are observed. After setting the device at 175 °C, the temperature was reduced again, and the self-rectifying behavior did not disappear indicating that a chemical or morphological change of the CF occurred at this temperature. This change indicates the thermal inducement of the self-rectifying mechanism, which can be explained by the impact of temperature on Ni migration/diffusion within the dielectric film [36]. In the case of GIF, the CF is formed by oxygen vacancies and Ni atoms. The movement of Ni ions is due to diffusion in the dielectric, from the region close to the Ni electrode toward the bottom electrode [13], [17], [18], [42]. Since the diffusion process is thermally controlled, a higher concentration of Ni ions in the CF is expected in a region closer to the silicon electrode. Consequently, a Schottky barrier could be formed at the interface between the CF and the bottom electrode at the highest temperatures.

In order to shed more light on this issue, a dynamical simulation for the CF generation was carried out. Simulations were based on a kinetic Monte Carlo algorithm to account for the metallic ion dynamics and the redox chemical reaction kinetics that oxidize and reduce the Ni atoms. The system is described by the coupled solution of the 3-D Poisson and heat equations. Qualitative results that help understanding the formation of a CF by means of Ni ions diffusion in a null electric field are shown in Fig. 8. In these simulations, a partially formed filament evolves at two different temperatures (300 and 448 K). As expected, the diffusion process is more efficient at higher temperatures. These results confirm the interpretation of the experimental data shown in Fig. 7.

In Fig. 7(b), the thermal dependence of the self-rectifying behavior observed at LRS suggests the formation of a Schottky barrier between a Ni-based CF and the semiconductor, generating an intrinsic diode with the n^+-Si. A schematic energy diagram of the Schottky barrier between the CF and the substrate is illustrated in Fig. 9(a). Notice that under SIF, the current increases with the temperature and decreases when the temperature is reduced again (dotted line), indicating no significant changes of the CF nature/size during the experiment.

The I–V characteristic for the Schottky emission mechanism is given by [43]

$$I = S \cdot A^* \cdot T^2 \cdot \exp\left[\frac{-q \cdot \phi_{B\text{eff}}}{K_B T}\right]$$
$$A^* = \frac{4\pi q K_B^2 m^*}{h^3} = \frac{120 m^*}{m_0}$$
$$\phi_{B\text{eff}} = \phi_B - \sqrt{qE/4\pi\varepsilon_r\varepsilon_0} \quad (1)$$

where I is the current, S the area, A^* is the effective Richardson constant, T is the absolute temperature, q is the electron charge, $\phi_{B\text{eff}}$ is the effective Schottky barrier height, K_B is the Boltzmann's constant, m^* is the effective electron mass in the dielectric, m_0 is the free electron mass, h is the Planck's constant, ϕ_B is the potential barrier height, E is the electric field, ε_0 is the vacuum permittivity, and ε_r is the optical dielectric constant. From (1), the plot $\ln(I/T^2)$ versus $V^{1/2}$ should be linear. Fig. 9(c) shows that the experimental data obtained above 0.2 V at high temperatures support the Schottky emission model. Furthermore, $\phi_{B\text{eff}}$, a parameter strongly related to the self-rectifying effect, can be estimated from the slope of the $\ln(I/T^2)$ versus $1/K_BT$ curve at fixed bias. $\phi_{B\text{eff}} \sim 0.19$ eV was obtained at −0.2V in the temperature range [50 °C–200 °C] [see Fig. 9(b)].

D. Influence of the Current Compliance on the Self-Rectifying Ratio

Since the current compliance [17], [18] significantly affects the size and composition of the CFs, it is worth investigating the effects of I_C on the device self-rectifying characteristics. Fig. 10 shows the self-rectifying ratio ($I_{\text{LRS}+}/I_{\text{LRS}-}$) versus $I_{\text{LRS}-}$ measured at $V = \pm 0.5$ V for devices with 5-, 10-, and 20-nm-thick HfO_2 layers. The $I_{\text{LRS}+}/I_{\text{LRS}-}$ value is obtained after a forming process under (a) GIF and (b) SIF, where three different I_c values were evaluated: 100 μA, 1, and 10 mA.

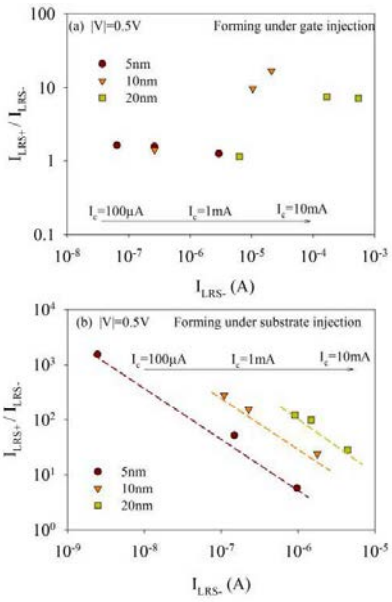

Fig. 10. Ratio between the positive (I_{LRS+}) and negative (I_{LRS-}) current versus I_{LRS-} obtained at $|V_{read}| = 0.5$ V after a forming process with $I_C = 100$ μA, $I_C = 1$ mA, and $I_C = 10$ mA under (a) gate injection and (b) substrate injection for devices with 5-, 10-, and 20-nm HfO_2. The values have been extracted from the postforming *I–V* characteristics of pristine devices, where two devices were measured at each condition, being the average value represented in the plots.

The distinctive behavior observed among devices subjected to GIF [Fig. 10(a)] and SIF [Fig. 10(b)] indicates that the degradation process is different for both injection polarities.

In the GIF case [Fig. 10(a)], the LRS characteristics do not show rectification, except for I_C values higher than 1 mA and HfO_2 layers thicker than 10 nm. Under this circumstance, larger thermal migration of Ni into the dielectric is expected [17], [18]. However, in the SIF case [Fig. 10(b)] higher ratios than those observed under GIF are observed for all the considered conditions. The largest ratio ($>10^3$ at ±0.5 V) was obtained for 5-nm-thick HfO_2 devices after a SIF process with $I_C \leq 500$ μA. Furthermore, Fig. 10(b) shows that I_{LRS+}/I_{LRS-} decreases for thicker dielectric layers and/or larger current compliances, or in other words, when longer metal filaments and higher currents are present in the dielectric. This fact can be explained in terms of the resulting physical damage at the CF/semiconductor interface [18], leading to a negligible impact of the Schottky barrier [44].

IV. Conclusion

In this paper, the RS effect in Ni/HfO_2/n^+-Si RRAM devices with self-rectifying tunability was investigated. The obtained results show that the forming conditions (compliance and polarity) as well as the HfO_2 thickness (5–20 nm) have a marked impact on the LRS currents and their self-rectifying behavior. In the 20-nm-thick oxide case, higher currents are observed after forming for both polarities, leading to a faster reset process through Joule heating. Data analysis reveals an increased self-rectifying ratio for devices subjected to a SIF process, suggesting the favored formation of metallic filaments. This observation could be explained by the Ni cation migration driven by the electric field and temperature enhanced Ni diffusion. Conduction measurements performed as a function of the temperature in 5-nm-thick oxide devices indicate that, depending on the forming polarity, the electron transport mechanism changes from tunneling-like through a narrow constriction under GIF, to Schottky emission under SIF owing to the presence of a barrier between the Ni-based CF and the n^+-Si. Finally, the roles played by the current compliance and dielectric thickness on the self-rectifying properties were investigated.

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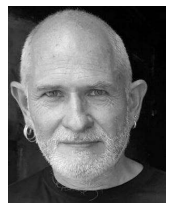
Alberto Rodríguez-Fernández was born in Zamora, Spain, in 1989. He received the B.S. degree in physics from the University of Salamanca, Salamanca, Spain, in 2013, and the M.S. degree in nanotechnology and material science from the Universitat Autònoma de Barcelona (UAB), Barcelona, Spain, in 2014, where he is currently pursuing the Ph.D. degree with a focus on resistive switching memories.

Samuel Aldana received the bachelor's degree in physics and the master's degree from the University of Granada, Granada, Spain, in 2014 and 2016, respectively, where he is currently pursuing the Ph.D. degree.

His current research interests include resistive RAMs and memristors physical simulation and compact modeling.

Francesca Campabadal received the Ph.D. degree in physics from the Universitat Autònoma de Barcelona, Barcelona, Spain, in 1986.

She joined the Institut de Microelectrònica de Barcelona, Consejo Superior de Investigaciones Científicas, Barcelona, Spain, in 1987, where she is currently a Research Professor. Her current research interests include the deposition of high-k dielectric layers, their electrical characteristics, and the resistive switching phenomena in RRAM devices.



Jordi Suñé (F'10) is currently a Professor of Electronics with the Universitat Autònoma de Barcelona, Barcelona, Spain. He has authored or co-authored more than 250 papers in international journals and relevant conferences. His current research interests include memristor physics and neuromorphic circuits for artificial intelligence applications.

Enrique Miranda (SM'10) received the Ph.D. degree in electronics engineering from the Universitat Autónoma de Barcelona (UAB), Barcelona, Spain, in 1999, and the Ph.D. degree in physics from the Universidad de Buenos Aires, Buenos Aires, Argentina, in 2001.

He has been a Professor with the Escola d'Enginyeria, UAB, since 2006. He has authored or co-authored around 200 papers, with most of them devoted to the electron-transport problem through the gate insulator in MIS and MIM devices.

Francisco Jiménez-Molinos was born in Granada, Spain, in 1975. He received the M.Sc. degree in physics, the M.Sc. degree in electronic engineering, and the Ph.D. degree from the University of Granada, Granada, Spain, in 1998, 2000, and 2002, respectively.

He is currently an Associate Professor with the Universidad de Granada. His current research interests include the simulation and modelling of resistive switching memories.

Juan Bautista Roldán received the bachelor's degree in physics and the Ph.D. degree from the University of Granada, Granada, Spain, in 1993 and 1997, respectively.

He is currently a Full Professor with the Electronics and Computer Technology Department, University of Granada. His current research interests include resistive RAMs and memristors physical simulation and compact modeling, simulation and modeling of nanometric conventional and multigate devices, CMOS photodiodes, and giant magnetoresistance current sensors.

Mireia Bargallo Gonzalez received the M.S. degree in physics from the University of Barcelona, Barcelona, Spain, and the Ph.D. degree from Katholieke Universiteit Leuven, Leuven, Belgium, in 2011, the Ph.D. degree with the Interuniversity Microelectronic Center, Leuven.

She is currently with the Institut de Microelectrònica de Barcelona, Barcelona, where she is involved in the electrical characterization, modeling and reliability of RRAM devices.

ARTICLE **EDL18**

Switching voltage and time statistics of filamentary conductive paths in HfO_2-based ReRAM Devices

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Switching Voltage and Time Statistics of Filamentary Conductive Paths in HfO_2-Based ReRAM Devices

A. Rodriguez-Fernandez, C. Cagli, J. Suñe, *Fellow, IEEE*, and E. Miranda, *Senior Member, IEEE*

***Abstract*— Switching voltage and time statistics of HfO_2-based one transistor-one resistor structures are investigated with the aim of clarifying the underlying physical mechanism that governs the formation and rupture of filamentary paths in the insulating layer. From the oxide reliability viewpoint, constant and ramped voltage stress experiments provide strong support to the so-called E-model, which is shown to be in line with current theories relating the reversibility of the conduction states in resistive random access memory devices to ionic drift and ultimately to Kramers' escape rate theory. It is shown how the switching statistics can be used to estimate the width and formation energy of the insulating gap along the filament as well as its temperature.**

***Index Terms*— ReRAM, resistive switching, oxide breakdown.**

I. Introduction

RESISTIVE random access memory (ReRAM) is among the most promising candidates to replace conventional nonvolatile memories for embedded applications [1], [2] owing to its high speed, high endurance, low power consumption, high scalability, and 3D integration feasibility [3]. The devices investigated in this work are 1T1R HfO_2-based structures that comply with the above requirements [4]–[6] and that have been thoroughly tested for intercell variability [7], forming conditions [8] and characterized using high speed dynamical techniques [6], [9]. The operational principle of ReRAMs relies on the repetitive formation (low resistance state, LRS) and rupture (high resistance state, HRS) of a conductive pathway spanning the oxide film. This pathway is formed by the local accumulation of oxygen vacancies and destroyed by a recombination process with oxygen ions. The transition from one state to the other is associated with the appearance and dissolution of a gap region in the formed filament whose width (t_{GAP}) is independent of the oxide layer thickness (t_{OX}) (see Fig. 1(a)). Within these processes, the oxide electric field plays a fundamental role as the driving force for the displacement of atomic species [10]. The stochastic nature of the atom rearrangements is reflected in the set/reset voltages and switching times of the devices. In this Letter, different acceleration models for the generation and rupture of the filamentary pathways are explored with the aim of clarifying their activation mechanism as well as the connection with oxide breakdown theories. The acceleration laws considered are: the V power-law, E-model, $E^{1/2}$-model and $1/E$-model, where $E$is the oxide electric field [11]. Instead of E, the applied voltage V is the variable used here for the analysis because of the initial uncertainty in t_{GAP}. The obtained results indicate that the E-model, often associated with the thermochemical model for dielectric breakdown [12], is closely connected with the formation and rupture of the atomic bridge that switchs the oxide conduction state. It is shown that the proposed approach provides an estimation of t_{GAP}, the activation energy E_A, and the temperature of the filament, crucial parameters for many memristive models [13], [14].

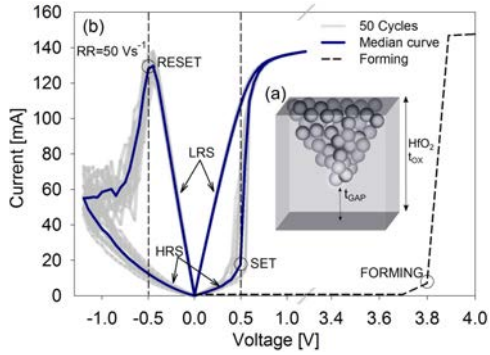

Fig. 1. (a) Schematic representation of the conductive path with t_{GAP} the gap width and t_{OX} the oxide thickness. (b) The grey lines are 50 quasi-static I-V characteristics ($RR = 50\text{Vs}^{-1}$). The heavy solid line is the median curve.

II. Devices and Experimental Details

Experimental data were obtained from ReRAM cells fabricated at LETI (CEA). The MIM structure consists in a 10 nm-thick atomic layer-deposited HfO_2 film sandwiched between

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A. Rodriguez-Fernandez, J. Suñe, and E. Miranda are with the Departament d'Enginyeria Electrònica, Universitat Autònoma de Barcelona, 08193 Bellaterra, Spain (e-mail: alberto.rodriguez@uab.cat).

C. Cagli is with CEA, 38054 Grenoble, France.

Color versions of one or more of the figures in this letter are available online at http://ieeexplore.ieee.org.

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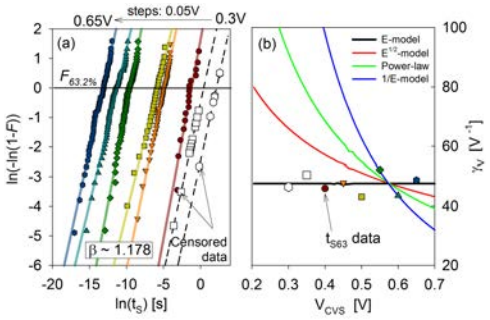

Fig. 2. (a) t_S distributions for CVS experiments. Symbols are experimental data. Solid and dashed lines are fitting results. F is the cumulative probability. (b) γ_V as a function of V_{CVS} for different acceleration models.

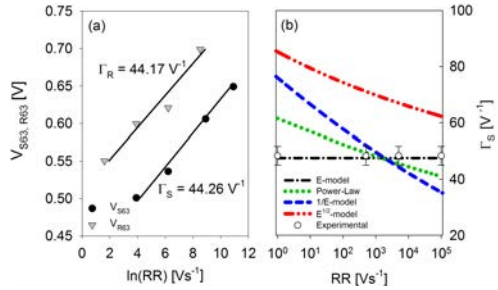

Fig. 3. (a) V_{S63} and V_{R63} as a function of ln(RR). (b) Γ_S as a function of RR for the different acceleration models under consideration.

Ti and TiN electrodes. The cell is connected in series with an n-type MOSFET ($W/L = 5\ \mu$m/0.35 μm), embedding a 1T1R structure. The transistor controls the maximum current that can flow through the memory cell which in turn determines the resistance window of the device [15]. Quasi-static *I-V-t* measurements were performed using a Keithley 4200-SCS equipped with a 4225-RPM pulse generator unit. As shown in Fig. 1(b), the forming event takes place at ≈3.8 V and the devices exhibit bipolar *I-V* characteristics. Notice that the median set and reset voltages are almost symmetric (≈±0.5V@50V/s). This indicates voltage controlled processes for HfO_2 in agreement with the results reported in [16]. Higher ramp rates (RR) yield higher set/reset voltages. Further details about the devices and experimental setup can be found in [17].

III. Switching Statistics

Devices in HRS were constant voltage stressed (CVS) with voltages in the range 0.30-0.65 V. As shown in Fig. 2(a), Weibull plots for the set switching time (t_S) exhibit average shape factor $\beta = 1.178$, which corresponds to a HfO_2 film with thickness $t_{OX} \approx 2$ nm [18]. Therefore a partially formed filament with an insulating region of about $t_{GAP} \approx 2$ nm can be assumed. The number of data points for 0.30 V and 0.35 V in Fig. 2(a) is low because of type I censoring effects (t_S longer than the time-of-test-termination). This uncertainty was taken into account using parametric survival analysis considering uniform acceleration (voltage-independent β) [19]. These latest statistics complement previously published data on the same devices [17]. Following McPherson's analysis for the breakdown of thin oxides [11], Fig. 2(b) shows $\gamma_V = -\mathrm{d}\ln(t_{S63})/\mathrm{d}V_{CVS}$ as a function of V_{CVS} for the acceleration models mentioned in Section I. Available data (symbols) confirm that the best fitting result corresponds to the E-model:

$$t_{S63} = t_0 \exp(-\gamma_V V_{CVS}) \tag{1}$$

which agrees with previous reports for RS devices [17]. A voltage acceleration parameter $\gamma_V = 47.59\ \mathrm{V}^{-1}$ is found. $t_0 = 3.49 \times 10^7$ s is a constant. Importantly, (1) is an empirical relationship that masks the temperature dependence. The non-Arrhenius behavior of γ_V has been extensively reviewed in [11] and [20].

Additionally, ramped voltage stress (RVS) experiments reveal that both the 63% set (V_{S63}) and reset (V_{R63}) voltages linearly increase with ln(RR) (see Fig. 3(a)). This indicates not only that a faster damaging process requires a higher field to meet the switching condition but also that the triggering mechanisms exhibit similar behaviour regardless of the bias sign (identical acceleration factor $\Gamma_{S,R} \approx 44.2\ \mathrm{V}^{-1}$) [16]. Data obtained from CVS and RVS experiments can be jointly assessed by means of the acceleration factor integral (AFI) method [17]. The method allows representing CVS data (t_S, V_{CVS}) in terms of its equivalent RVS data (V_S, RR). In particular, for the E-model, the AFI method reads [17]:

$$t_S = \int_0^{t_S} A_f dt = \int_0^{t_S} \exp\left[\Gamma_S\,(RR \cdot t - V_{CVS})\right] dt \tag{2}$$

where A_f is the acceleration law. Since $V_S = RR \cdot t_S$, (2) yields:

$$V_{S63} = \frac{l}{\Gamma_S}[\ln(RR) + \ln(t_0 \cdot \Gamma_S)] \tag{3}$$

which is consistent with the experimental data shown in Fig. 3(a). Figure 3(b) shows $\Gamma_S = \{\mathrm{d}V_{S63}/\mathrm{d}[\ln(RR)]\}^{-1}$ for the different acceleration models under consideration. Again, the E-model exhibits the best agreement with the experimental data (symbols).

IV. Ionic Transport

The reason behind the logarithmic and exponential dependences for the switching voltage and time statistics can be found in the migration of oxygen ions within the oxide layer through field-assisted and thermally-activated hopping [21], [22]. The ion current (i_{ion}) can be calculated from the generation probability of oxygen vacancies [23]. The charge required to reach the set condition, Q_S, is approximately given by:

$$Q_S = \int_0^{t_S} i_{ion} dt \approx \int_0^{t_S} i_0 \exp\left(\frac{\alpha z e}{k_B T} V\right) dt \tag{4}$$

where i_0 is a constant, $0 \le \alpha \le 1$ the symmetry factor, z the number of exchanged electrons, e the electron charge, and

k_BT the thermal voltage. From (4), t_S under CVS reads:

$$t_S = \frac{Q_S}{i_0}\exp\left(-\frac{\alpha z e}{k_B T}V_{CVS}\right) \quad (5)$$

which is formally equivalent to (1) for a fixed temperature. Assuming $z = 2$ and $T = 300$ K, $\alpha = 0.61$ is obtained. Similarly, for RVS, $dt = dV/RR$ so that (4) yields:

$$V_S = \frac{k_B T}{\alpha z e}\left[\ln(RR) + \ln\left(\frac{Q_S}{i_0}\cdot\frac{k_B T}{\alpha z e}\right)\right] \quad (6)$$

which closely resembles (3). In this case, for $z = 2$ and $T = 300$ K, $\alpha = 0.57$ is obtained. In both cases, $\alpha \neq 0.5$ indicates a slightly asymmetrical diffusion barrier for the ions. (5) and (6) express that a fixed ionic charge Q_S needs to be displaced for triggering the switching condition. Since both (1) and (5), and (3) and (6), share the same dependence with V_{CVS} and RR, respectively, it is worth discussing the physical connection between the E-model and the ion transport mechanism.

V. Discussion and Conclusion

According to McPherson-Berman's theory [24], for a variety of oxides, the product

$$\gamma_E E_{BD} = E_A/k_B T \quad (7)$$

is a constant independent of the material permittivity κ. γ_E is the field acceleration parameter and E_{BD} the breakdown field. E_A is the energy required for ion displacement from its normal local bonding environment in the absence of applied field. Experimentally, it is found [24], [25]:

$$\gamma_E = 1.58\kappa^{0.66}\ [cm/MV] \quad (8)$$

$$E_{BD} = 29.9\kappa^{-0.65}\ [MV/cm] \quad (9)$$

Since $\kappa \approx 22-25$ for HfO_2 [26], $\gamma_E = 12.15-13.22$ cm/MV and $E_{BD} = 3.7-4.0$ MV/cm are found from (8) and (9), respectively. This latest field range agrees with the electroforming field $E_{BD} = 3.8$ MV/cm obtained from Fig. 1(b). Now, using (1) and (8) and assuming that the applied voltage mainly drops across the gap region, $t_{GAP} \approx \gamma_E/\gamma_V = 2.55-2.77$ nm is obtained, which is consistent with the gap width extracted from the Weibull slope (Fig. 2(a)). Moreover, since $\beta \approx t_{GAP}/a_0$ [24], a percolation cell-size $a_0 = 2.17$ nm is found. In addition, from (7), E_A (300 K) = 1.25 eV is obtained, which coincides with the activation barrier height reported in [27]. From the oxide reliability viewpoint, the dissolution of the insulating gap can be regarded as a transition in the reaction space from a metastable state towards a degraded state characterized by a lower free energy (see Fig. 4(a)). This lower energy level arises from a molecular dipole-field interaction [24]. In the case of resistive switching materials this process can be reversed by the application of an opposite field. On the other hand, from the ion migration viewpoint, the formation/destruction of the conducting atomic bridge is the consequence of a thermal-assisted hopping mechanism with barrier lowering in the real space (see Fig. 4(b)). The link between both visions is ultimately Kramers' escape rate theory [25], [28] which relates the transitions to the probability of a particle, real or fictitious, jumping from one potential well to another by passing over a barrier. From Kramers' theory [29]:

$$t_S^{-1} \sim k = k_0 \exp\left[-(E_A - e\alpha V)/k_B T\right] \quad (10)$$

where k is the reaction rate and $k_0 \sim 7\times10^{13}$Hz is the Hf-O bond vibration frequency [30]. (10) arises from a diffusive dynamics with vertical thermalization (inside the well) much more rapid than the horizontal outflow [31]. Matching the empirical law (1) with the theoretical expression (10) provides an alternative method to estimate the filament temperature as a function of the applied voltage. This is the temperature required to switch the device on (HRS → LRS) in 63% of the CVS experiments. The obtained range, 300 K-600 K (see Fig. 4(c)), is consistent with classical thermal simulations [32].

In summary, our results seem to indicate that Kramers' theory provides a consistent framework for analyzing constant and ramped voltage stress experiments in the context of ReRAM devices. For the sake of clarity, the link among the corresponding models and equations are depicted in Fig. 4(d).

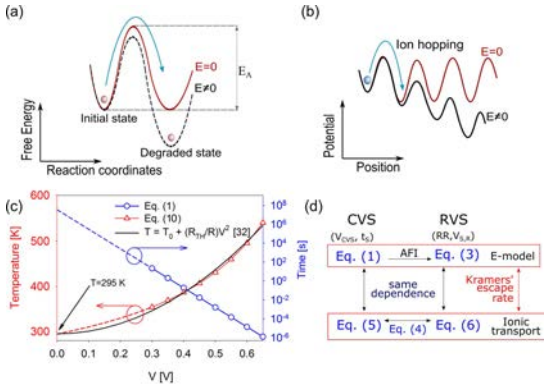

Fig. 4. (a) Free energy description associated with the material breakdown. (b) Schematic representation of random ionic jump over a potential barrier. (c) Filament temperature as a function of the applied voltage. $T_0 = 295$ K, $R_{TH}/R = 567$ K/V^2. (d) Schematic relationships between the model equations.

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Appendix II:
Other publications included in this Thesis

ARTICLE **ICS14**

On the properties of conducting filament in ReRAM

ON THE PROPERTIES OF CONDUCTING FILAMENT IN ReRAM

Xiaojuan Lian[1], Mario Lanza[2], Alberto Rodríguez[1], Enrique Miranda[1] and Jordi Suñé[1]*
[1]Departament d'Enginyeria Electrònica, Universitat Autònoma de Barcelona, 08193-Bellaterra, SPAIN
[2] Institute of Functional Nano & Soft Materials, Soochow University, 199 Ren-Ai Road, Suzhou Industrial Park, Suzhou, Jiangsu, 215123, China
*Corresponding Author's Email: jordi.sune @uab.cat

ABSTRACT

The conducting properties of resistive switching filaments in ReRAM are studied. Departing from first-principle simulations of electron transport along paths of oxygen vacancies in HfO_2, the Quantum Point Contact model is reformulated in terms of a bundle of such vacancy paths. By doing this, the number of model parameters is reduced and a much clearer link between the microscopic structure of the conductive filament and its electrical properties can be provided. As an example, a simple geometrical model for the microscopic structure of the CF is proposed and it is used to track the change of the conducting properties during the set/reset transitions. The model has been further checked by measurements at the nanoscale by means of CAFM.

INTRODUCTION

Resistive switching (RS) in metal-insulator-metal (MIM) devices is often based on the creation and partial destruction of a conductive filament (CF) of nanoscale dimensions. Therefore, understanding the conduction properties of the CF in the Low-Resistance State (LRS) and the High-Resistance State (HRS) and linking these properties to the shape and nature of the CF is of great importance to improve the understanding of RS and to boost Resistive Random Access Memories (ReRAM) applications.

Many different conduction models have been proposed for the HRS including trap-assisted tunneling [1], Poole-Frenkel conduction [2], thermally activated hopping [3], space-charge limited current [4], and the Quantum Point Contact model (QPC) [5, 6], among others. On the other hand, the experimental evidence of a CF behaving as a Quantum Wire (QW) in the LRS has been reported in a variety of ReRAMs, including HfO_2-based structures [7-10]. The single model which provides a smooth transition from tunneling to Ohmic conduction and which naturally explains conductance quantization effect is the QPC model, which is based on the Landauer transmission approach to conduction along narrow microscopic constrictions and it assumes that the CF is a quasi-one dimensional system of electron states.

THE THEORETICAL BASIS

Using a Green's function formalism coupled with a density functional theory code, the conductance of vacancy filaments of different width was calculated, showing that even one vacancy path can sustain a conductive channel, with conductance of the order of G_0[11] and each time a vacancy is removed from the single-vacancy filament, the conductance is reduced by a factor of ~10. Taking into account that the separation between vacancies is ~0.26 nm, the re-oxidation of a vacancy introduces a gap in the CF which acts as a potential barrier of about this thickness. Thus, the conductance exponentially decreases with t_{gap}, so $G = G_0 exp(-t_{gap}/t_0)$ with $t_0 = 0.12\ nm$.

According to the Landauer's approach, the current flowing through a CF with N vacancy paths can be calculated as [12]:

$$I(V) = \frac{2e}{h} N \int_{-\infty}^{\infty} T(E)\{ f(E - \beta eV) - f(E + (1-\beta)eV)\}\ dE \quad (1)$$

where E is the energy, $T(E)$ is the transmission probability, f is the Fermi-Dirac distribution function, e and h are the electron charge and the Planck constant, and V is assumed to drop at the cathode and anode interfaces in a fraction of β and (1- β) respectively. Assuming an inverted parabolic potential barrier allows to obtain an expression for the tunneling probability [13-15], $T(E) = \{1 + exp[-\alpha(E - \Phi)]\}^{-1}$, where Φ is the barrier height and $\alpha = t_{gap}\pi^2\hbar^{-1}\sqrt{2m^*/\Phi}$ is related to the inverse of the potential barrier curvature, m^* is the effective electron mass. Inserting the transmission coefficient into Eq (1):

$$I = \frac{2e}{h} N \left\{ eV + \frac{1}{\alpha} Ln\left[\frac{1+exp\{\alpha[\Phi-\beta eV]\}}{1+exp\{\alpha[\Phi+(1-\beta)eV]\}}\right]\right\} \quad (2)$$

This equation can be applicable to both the HRS and the LRS depending on the values of α and Φ, which describe the potential barrier. If there is a gap with a potential barrier, this equation is found to converge to $I \approx NG_0 \exp(-\alpha\Phi)V$ at low voltages so that the equivalent transmission probability is $T = \exp(-\alpha\Phi)$. Linking this to the thickness dependence obtained from the ab-initio results $T = \exp(-t_{gap}/t_0)$, we can obtain that $t_{gap} = t_0\alpha\Phi$ and $\Phi = 2\hbar^2/m^*\pi^2 t_0^2$. Assuming that $m^* \sim m_0$ results in a barrier height $\Phi \sim 1.16$ eV, which is a perfectly consistent value, given the large gap of HfO_2.

After reformulating the QPC model, only three free fitting parameters remain: the number of vacancy paths N with the constraint $N \geq 1$, the average t_{gap} in these paths and the average value of the asymmetry parameter

β, with the constraint $0 < \beta \leq 1$. However, in order to simplify the fitting process, we will usually assume a fixed value of β=0.5(symmetry) or β=1(asymmetry) and extract only N and t_{gap} from the experimental data using Least-square-estimation (LSE) method.

RESULTS AND DISCUSSION

Cycling experiments consisting of 1250 consecutive set/reset operations have been performed using the ramp voltage sweep (RVS) method in Pt/HfO_2/Pt structure operated under unipolar mode and Pt/Ti/HfO_2/Pt structure operated under bipolar switching mode.

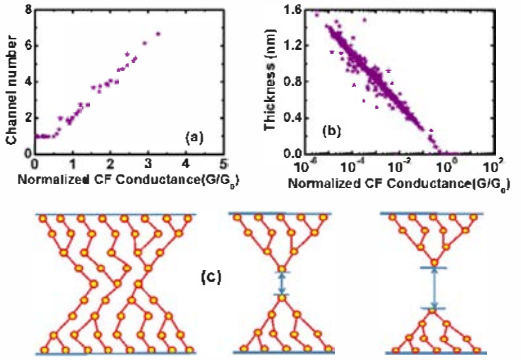

Figure 1: Extracted QPC model parameters of Pt/HfO_2/Pt structures: (a) Channel number and (b) Gap thickness versus CF conductance. (c) Schematic representation of the CF structure evolution from the LRS to the HRS.

The analysis of the properties of the CF in the HRS for Pt/HfO_2/Pt structures provides useful information. Fig. 1(a) and Fig. 1(b) show the extracted QPC model parameters for the Pt/HfO_2/Pt structures operated in the unipolar mode. Assuming $\beta = 0.5$ for this symmetric structure we have only extracted N and t_{gap}. As shown in Fig. 1(a), for CF conductance below G_0, the best fit is obtained for $N = 1$, while for $G > G_0$ the number of conducting channels perfectly correlates with the CF conductance. On the other hand, Fig. 1(b) shows that there is no barrier for $G > G_0$ (i.e. $t_{gap} = 0$), and the thickness of the gap shows a perfect exponential correlation with the CF conductance below G_0, as expected for tunneling through a potential barrier. Thus, we conclude that below G_0, the CF has a very narrow constriction with a spatial gap that ranges from 0 to 1.4 nm. This thickness range indicates that the gap can be estimated to be of up to ~6 re-oxidized vacancies in the least conductive CFs. The evolution of the geometry of the CF from the LRS to the HRS is schematically depicted in Fig. 1(c). Starting from a very wide CF in the LRS, the first stage of the reset process consists in the reduction of the width of the CF in its most constrictive part to a limit in which only one or few oxygen vacancy paths connect the electrodes. This stage is followed by the opening of a gap in CF.

The Pt/Ti/HfO_2/Pt structures include a thin Ti layer between the top Pt electrode and the HfO_2 layer. The Ti film is believed to act as an oxygen extraction layer and to introduce a high density of oxygen vacancies in the HfO_2. The vacancy profile is thought to be rather asymmetric with a much higher concentration near the top interface.

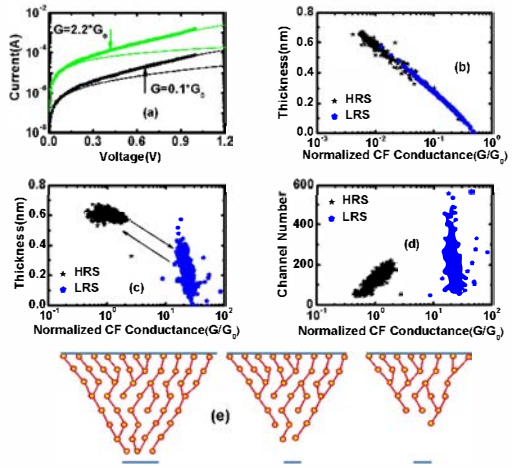

Figure 2: (a) Demonstration that fitting with N=1 (dashed black line) is not possible in the HRS nor it is possible to fit the I-V assuming linear conduction for $G>G_0$ (green dashed line) in the LRS. (b) Extracted QPC model parameters of Pt/Ti/HfO_2/Pt structures: gap thickness versus conductance per channel. (c) Gap thickness and (d) Channel number versus CF conductance. (e) Schematic representation of CF structure in bipolar experiments.

The fitting of the I-V curves to the QPC model is excellent, but the linear fit is not possible when $G > G_0$ nor it is possible to assume $N = 1$ for $G < G_0$, as explicitly shown in Fig. 2(a). In this particular case, the extraction of the QPC parameters was done under the assumption that $\beta = 1$. This value gives the best fitting results and is consistent with the strong asymmetry of the CF shape in structures which contain an oxygen extraction layer. Fig. 2(b) show that the average gap thickness per conducting mode is found to converge to zero for $G/N \sim G_0$, as required by the QPC model. Fig. 2(c) shows the extracted gap thickness versus CF conductance in the HRS and the LRS. We can see the average gap thickness is 0.59nm in the HRS and 0.25nm in the LRS; this is to say, there are about two or three re-oxidized vacancies in the HRS and one re-oxidized vacancy in the LRS. The number of CF paths versus conductance is shown in Fig. 2(d), many conduction paths are found to be active in the HRS but they show a

gap with an average thickness corresponding to two or three vacancies.

In order to deepen into the relation between conduction properties and geometry of the CF, a simple geometrical model for the microscopic structure of the CF is proposed and it is used to track the change of the conducting properties during the SET/RESET transitions. Given the asymmetry of the Pt/Ti/HfO_2/Pt structure, the CF is assumed to be a truncated cone with the tip contacting the bottom electrode which is the active region during switching. The CF shape is described by three parameters, the upper base $x_0' = a_0\sqrt{N}$ (a_0 being the minimum distance between two vacancies in HfO_2 and N being the number of channels), the lower base of the cone (x_0) and the gap between CF and the bottom electrode (h_0) (see Fig. 3).

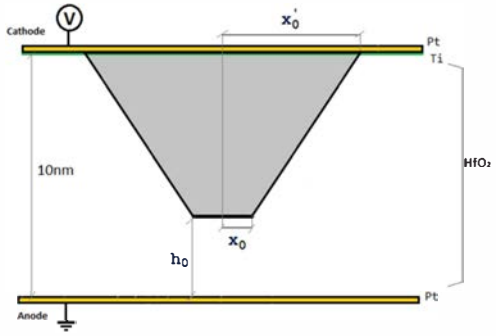

Figure 3: Definition of the geometrical model (with its parameters x_0, h_0, and x_0' used to describe the CF.

By varying these three parameters and calculating the CF current by superposition of the different channels with their corresponding gap thickness, we are able to reproduce the experimental cloud of QPC model parameters (see Fig. 4), thus being able to extract the CF shape. All points that are included within the experimental cloud, have a similar geometrical configuration, the values of h_0 are similar to the gap thickness extracted of the QPC model and the value for x_0 is a high percentage of the value of x_0'. Therefore we can conclude that the geometrical evolution is similar to the one shown in Fig. 2(e).

In order to further check the applicability of the QPC model, we have obtained current characteristics of single CFs by measuring the local conductivity of different HfO_2 blankets (without top electrode) using a conductive atomic force microscope (CAFM) working in controlled atmosphere connected to a semiconductor parameter analyzer (SPA) [16]. This setup is necessary because a standard CAFM present some limitations that impede measuring RS (specially bipolar). All commercially available AFMs can only measure small currents up to some nanoamperes, and cannot apply current limitation (necessary to avoid irreversible breakdown).

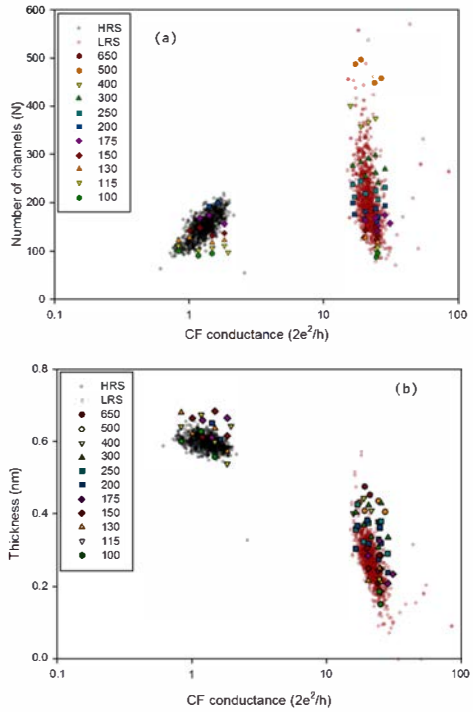

Figure 4: (a) Channel number and (b) gap thickness versus CF conductance for HRS and LRS extracted from experimental data are compared to different simulations which assume the geometric model of Fig. 3 varying N from 100 to 650 channels.

Moreover, local anodic oxidation measuring in air atmosphere impedes measuring currents by injecting electrons from the tip [17, 18]. The current limitations can be solved using the SPA, while local anodic oxidation can be solved measuring in an atmosphere with reduced humidity. In this work we used dry Nitrogen, but high and ultra-high vacuum also showed similar performance.

Using the tip of the CAFM as a top electrode, the dielectric breakdown has been induced at different locations of the sample, and further cyclic voltammograms with different polarities have been applied to explore the presence of RS [19]. It is worth noting that not all locations of the HfO_2 stack showed resistance recovery, but only some specific locations with a specially low breakdown voltage did (similar to that measured at the device level). Once the reset process has been identified, the currents in LRS and HRS have been fitted to the model above presented, and the results

are displayed in Fig. 5. The parameters used to fit each curve are the following: HRS: $\alpha=3eV^{-1}$, $\beta=0.62$, $\Phi=1.2eV$, $N=1$, barrier thickness=0.61nm (with $m^*=0.44m$); and LRS: $\alpha=4.5eV^{-1}$, $\beta=0.6$, $\Phi=0.3eV$, $N=1$, barrier thickness=0.46nm (with $m^*=0.44m$). As it can be observed, a high degree of accuracy can be achieved, indicating that the current through a single CF can be actually fitted by this methodology.

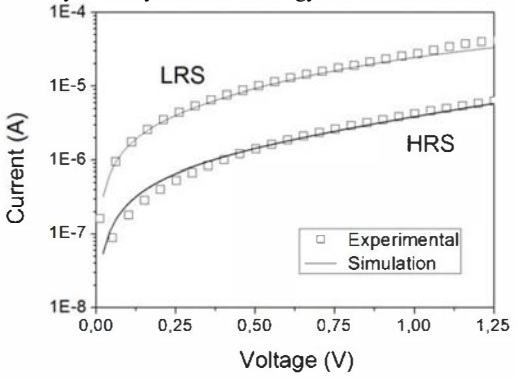

Figure 5: Experimental currents measured with the CAFM through a single CF in LRS and HRS formed in a HfO_2 stack.

Special interesting is the fitting of the HRS. By looking to Figs. 2a and 5 it can be concluded that the model is able to fit the currents in HRS both at the device level and nanoscale. One would expect a perfect fitting at the nanoscale (Fig. 5), since the current measured corresponds to a single filament; but, since multiple partially formed CFs (soft breakdown) are present in the MIM capacitor at the device level, one could expect not so perfect fitting. The fact that the model fits the currents at the device level is indeed indicating that the current through multiple partially formed CFs can be also understood as a unique filament with averaged properties.

CONCLUSIONS

A multi-scale QPC model has been presented and has been applied to extract the relevant parameters in the HRS and the LRS during unipolar and bipolar resistive switching. The conduction properties have been related to the geometry of the CF. The model has been further tested by fitting experimental currents measured at the nanoscale through single CFs using an enhanced CAFM.

ACKNOWLEDGEMENTS

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ARTICLE **CDE17**

SPICE simulation of 1T1R structures based on a logistic hysteresis operator

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SPICE Simulation of 1T1R Structures Based on a Logistic Hysteresis Operator

G.A. Patterson,
A. Rodriguez-Fernandez,
J. Suñé, and E. Miranda
Departament d'Enginyeria Electrònica,
Universitat Autònoma de Barcelona, Spain
Email: enrique.miranda@uab.cat

C. Cagli
and L. Perniola
CEA, LETI, MINATEC Campus, France
Email: carlo.cagli@cea.fr

***Abstract*—In this paper a SPICE (Simulation Program with Integrated Circuit Emphasis) implementation of a memristor model able to describe the major and minor current-voltage loops in bipolar resistive switches is reported. In particular, this work addresses the implementation of one transistor-one resistor (1T1R) structures for RRAM applications by means of SPICE simulations. Specifically, the dependence of the low-resistive state on the compliance current is investigated. The model is based on the combination of a diode-like device as the switching element and the logistic hysteron formalism for the memory effect. It is shown how the proposed circuit for the 1T1R structure reproduces the main features of the experimental output curves.**

***Keywords*—1T1R structure, RRAM, SPICE, compliance current.**

I. Introduction

Memristive elements are two-terminal passive devices that present nonvolatile variable resistance. There is wide agreement that these elements are the most promising candidates to succeed current memory technologies. The aforementioned change of resistance depends on the history of the device, that is, a hysteretic behavior is the signature of these structures. Moreover, when these elements are combined in complex circuits, a large number of potential applications emerge such as memory devices, neuromorphic systems, analog and chaotic circuits, computational logic units, etc. In particular, this work addresses the implementation of one transistor-one resistor (1T1R) structures for RRAM applications by means of SPICE simulations and it presents an analysis of how the low-resistive state changes with the compliance current. The R element represents the switching device while the series access transistor T has been demonstrated to improve the capability of controlling the switching behavior [1], [2], [3], [4]. The memristor model proposed in this work is based on a non-rectifying diode-like structure for the electron transport and the hysteron formalism for the memory effect. This combination allows the possibility of simulating major (maximum input signal) and minor (bounded input signals) loops in the current-voltage characteristic [5]. This approach assumes multichannel conduction (single or multifilamentary structures), with SET and RESET voltages of the individual channels given by Gaussian distributions. The transport equation, under the appropriate model parameters, can switch between an exponential (high resistive state) and a linear (low resistive state) response curve.

Here the SPICE implementation of the switching device is presented as well as the characterization of the 1T1R structure. The transistor gate voltage is used to set the compliance current and thus to control the resistive state during the SET process. SPICE simulations are compared to experimental data obtained from HfO_2-based switching devices.

II. Model Description

The device model consists in a transport equation that switches between a high resistive state (HRS) and a low resistive state (LRS) as it is depicted in Fig. 1a. The underlying physical mechanism is assumed to be multichannel conduction, where the SET and RESET voltages of the individual channels follow a Gaussian distribution. Other distributions are possible within this framework. Notice that this does not refer to the SET and RESET voltage distributions obtained from multiple loops. The transport equation can be reduced as two identical opposite-biased diodes in series with a resistor. An approximate solution for this system, neglecting the inverse saturation currents of the diodes, is given by

$$I = \mathrm{sign}(V) I_0 \left\{ \frac{W\left[\phi \exp\left(\alpha|V| + \phi\right)\right]}{\phi} - 1 \right\} , \quad (1)$$

with $\phi = \alpha R_\mathrm{s} I_0$, where I_0 is the current amplitude factor, α a parameter related to the specific physical conduction mechanism, R_s the series resistance, and W the Lambert function. In order to include the hysteretic behavior, the hysteron formalism is introduced. In this way, the internal state λ is defined by the operator

$$\lambda\left(t_n\right) = \min\left\{ \Gamma^-\left(V(t_n)\right), \max\left[\lambda\left(t_{n-1}\right), \Gamma^+\left(V(t_n)\right)\right] \right\} , \quad (2)$$

where $\lambda(t_{n-1})$ is the value of λ in the previous time step. The ridge functions $\Gamma^\pm$, shown in Fig. 1b are logistic functions representing the sequential creation $(+)$ or destruction $(-)$ of the conductive channels as a function of the applied

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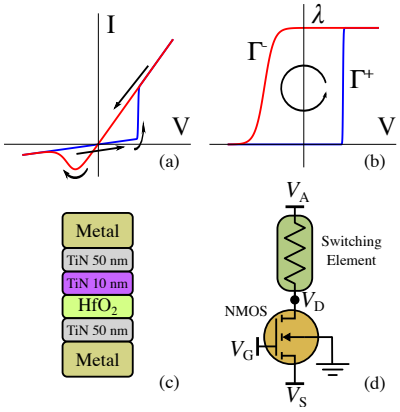

Fig. 1. (a) Schematic I-V characteristic curve. (b) Hysteron model for the internal state variable λ. (c) Switching element stack. (d) Proposed 1T1R configuration.

voltage. The logistic behavior arises from the integration of the Gaussian distribution. The ridge functions are given by

$$\Gamma^{\pm}\left(V(t_n)\right) = \left\{1 + \exp\left[-\eta^{\pm}\left(V(t_n) - V^{\pm}\right)\right]\right\}^{-1} \quad , \quad (3)$$

where $\eta^{\pm}$ are the transition rates, and $V^{\pm}$ the threshold voltages. The state of the hysteresis is described by the vector $\Omega = (I_0, \alpha, R_s)$ which in turn is a linear function of λ and is defined as $\Omega = \Omega^{\text{set}} + \lambda\left(\Omega^{\text{reset}} - \Omega^{\text{set}}\right)$, where $\Omega^{\text{set}} = (I_0^{\text{set}}, \alpha^{\text{set}}, R_s^{\text{set}})$ and $\Omega^{\text{reset}} = (I_0^{\text{reset}}, \alpha^{\text{reset}}, R_s^{\text{reset}})$ are the end points of the vector Ω, for the SET and RESET state, respectively. This simplified approach allows modeling samples that present threshold resistive switching, where it is necessary to overcome a certain voltage level to switch the resistive state.

Finally, in order to simplify the calculations, the Lambert function is approximated by [6]

$$W(x) \approx \ln(1+x)\left(1 - \frac{\ln\left[1+\ln(1+x)\right]}{2+\ln(1+x)}\right) \quad . \quad (4)$$

III. Experimental Setup

The resistive switching structure and the device arrangement for the experiments is shown in Figs. 1c and 1d, respectively. The structure consists of a 10 nm-thick ALD HfO_2 layer sandwiched between two electrodes (Ti and TiN) and a n-type MOSFET transistor [3]. Data were obtained from quasi-static measurements. A Keithley 4200-SCS was used to apply and measure the signals of interest. The input signals are schematized in Fig. 3a, 3b, and 3c.

IV. SPICE Model

The circuit schematic for the memory element is shown in Fig. 2. The two ports PLUS and MINUS represent the positive and negative terminals of the device, respectively. The source G_M provides a current given by Eq. (1) taking into account

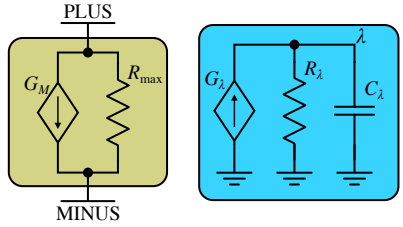

Fig. 2. SPICE circuit schematic. Current source G_M drives the I-V response, while the evolution of the internal state λ is solved by means of a RC circuit.

the voltage drop between PLUS and MINUS and the value of the internal state variable λ which, in turn, is described by the voltage drop across the capacitor C_λ. Resistor $R_{\max}$ accounts for the non-ideal behavior of the current source and it is necessary to overcome iteration problems and divide-by-zero errors when trying to combine with other circuit elements.

Equation (2) describes the evolution of the state variable $\lambda(t_n)$ as a function of the applied voltage $V(t_n)$ and the previous value $\lambda(t_{n-1})$. This equation is solved by means of a current source and a RC-delay circuit as shown in Fig. 2. The output of the current source G_λ is set equal to Eq. (2) and $R_\lambda = 1\ \Omega$. It should be pointed out that the RC circuit is not aimed to integrate the signal provided by the current source G_M as considered in several previous works [7], [8], [9], but to introduce the delay required to compute Eq. (2). Because in a RC circuit the current is ahead with respect to the voltage, the previous value $\lambda(t_{n-1})$ is associated with the voltage drop across the capacitor. The output port L tracks the value of the internal state λ.

The code of the subcircuit is presented in Table I. It has been implemented in the free analog circuit simulator LTspice IV [10].

Regarding the transistor characteristics, for illustrative purposes, a level 1 MOSFET model was used. Under this approach, the saturation current is given by

$$I_{\text{DS-sat}} = \frac{1}{2}\kappa\frac{w}{l}\left(V_{\text{GS}} - V_{\text{t}}\right)^2 \quad , \quad (5)$$

where κ is a fitting parameter, V_{t} is the transistor threshold, and w and l are the channel width and length, respectively. The voltage V_{GS} is the voltage drop across the gate and source terminals. The values of the parameters used are shown in the caption of Fig. 4.

V. Results

Figure 3 shows the input protocol applied to the 1T1R structure. The gate voltage is shown in Fig. 3a, the voltage corresponding to terminal A is depicted in Fig. 3b, and the source voltage in Fig. 3c. During the SET process, the source terminal is fixed to ground, while a positive sweeping voltage is applied to terminal A. The limiting current is set by the gate voltage which, for this purpose, must be larger than the transistor threshold voltage V_{t} as shown in Fig. 3f. Figure 3g shows the current flowing through the switching element. As

TABLE I
SPICE MODEL CODE

```
* Resistive Switching device SPICE model
   .subckt res_switch PLUS MINUS L
** Block 1 - Model parameters **
* vp/vm: plus/minus threshold
* np/nm: plus/minus transition rate
* iset/ires: I0_set and I0_res
* aset/ires: alpha_set and alpha_res
* rset/rres: Rs_set and Rs_res
* l0: initial condition
   .params vp=0.84    np=235      vm= -0.57
   + nm=7.23          l0=0
   + iset=7.96e-04    aset=0.66   rset=6.36
   + ires=1.03e-06    ares=1.75   rres=2768
* Auxiliary parameters
* Rl: R_lambda
* Cl: C_lambda
* Rm: R_max
   .params Rl=1       Cl=1e-4     Rm=1e10

** Block 2 - Declare functions **
* gp/gm: plus/minus ridge function
* w: Lambert W function
* I0: current amplitude factor
* a: alpha parameter
* Rs: series resistance
   .func gp(V)=1/(1+exp(-np*(V-vp)))
   .func gm(V)=1/(1+exp(-nm*(V-vm)))
   .func w(x)=log(1+x)*(1-
(log(1+log(1+x)))/(2+log(1+x)))
   .func I0(l)=iset*l+ires*(1-l)
   .func a(l)=aset*l+ares*(1-l)
   .func Rs(l)=rset*l+rres*(1-l)

** Block 3 - Current source - state variable **
   Gl 0 L value={min(gm(V(PLUS,MINUS)),
max(gp(V(PLUS,MINUS)),V(L)))}
   R L 0 {Rl}
   C L 0 {Cl}
   .ic V(aux)=l0
** Block 4 - Current source - memristor **
   Gmem PLUS MINUS value={(sgn(V(PLUS,MINUS))*
(1/(a(V(L))*Rs(V(L)))*w(a(V(L))*Rs(V(L))*I0(V(L))*
exp(a(V(L))*(abs(V(PLUS,MINUS))+Rs(V(L))*
I0(V(L)))))-I0(V(L))))}
   Rmax PLUS MINUS {Rm}
   .ends res_switch
```

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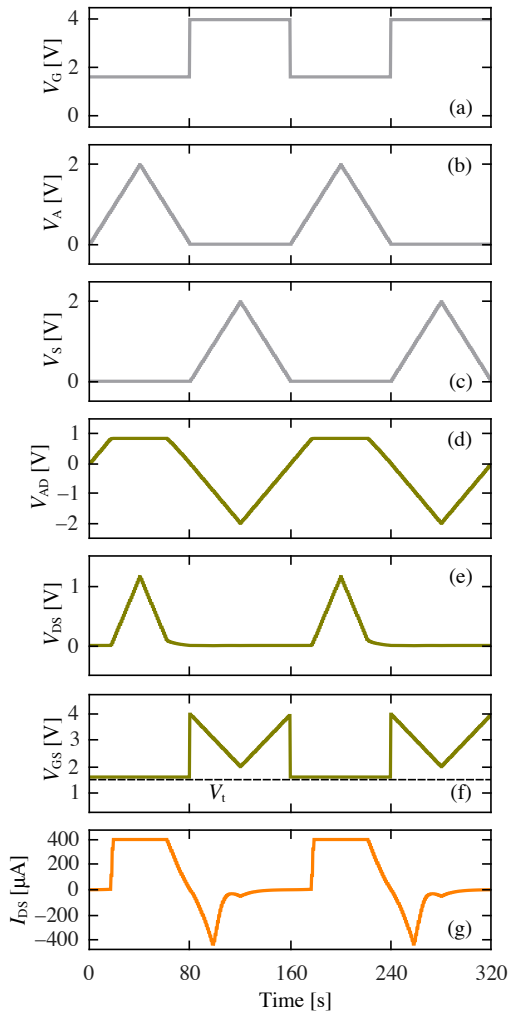

Fig. 3. (a), (b), and (c) show the applied voltages corresponding to nodes G, A and S. (d), (e), and (f) are the voltage drops across the switching element, the drain-source nodes, and the gate-source nodes, respectively. (g) shows the current flowing through the switching element.

it can be seen, when the current reaches the limit value (in this particular case $I_{DS} = 400$ μA), the voltage drop across the drain and source nodes (Fig. 3e) increases, while the voltage across the switching element remains constant (Fig.3d). On the other hand, the RESET process is carried out as follows. The voltage in terminal A is now grounded and the sweeping signal (positive) is applied to the transistor source terminal. During this procedure, the gate voltage is such that the voltage difference between the gate and source terminals is positive.

Experimental results regarding the characteristic curve of the 1T1R structure are shown in Fig. 4. Four different compliance currents were considered by changing the gate voltage during the SET procedure. As it can be seen, there are stable SET transitions and the slopes related to the LRS show a clear dependence with the limiting current. The figure also presents numerical results where the model parameters were obtained by fitting the experimental data corresponding for the cycle limited to 400 μA. Remarkably, despite having used the same set of parameters in the four cycles, there is a very good agreement between simulations and experiments. In addtion, notice that neither the transistor model nor the hysteron shape (probability distributions) have been optimized for this exercise.

Results can be interpreted as follows. The transistor limits

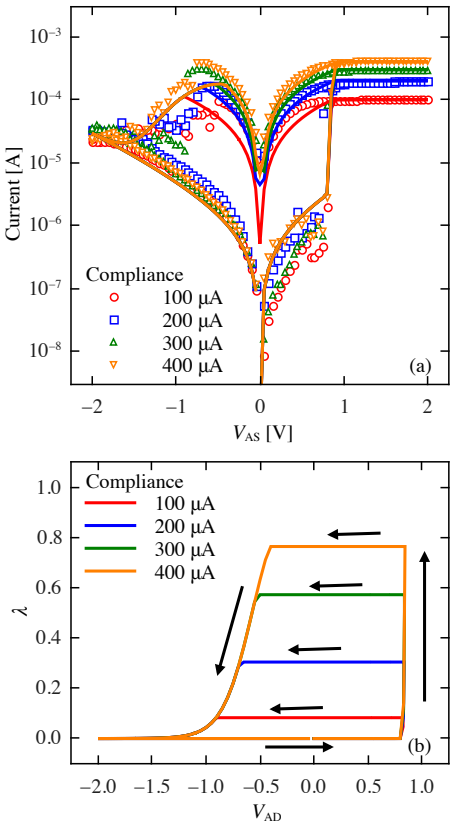

Fig. 4. Experimental and SPICE results. (a) shows the I-V characteristics of the 1T1R configuration under different current compliances. Symbols stand for experimental data while solid lines stand for numerical results. (b) shows the evolution of the internal state λ for the considered limiting currents. The parameters are: $I_0^{\text{set}} = 796$ µA, $I_0^{\text{reset}} = 1.03$ µA, $\alpha^{\text{set}} = 0.66$ V^{-1}, $\alpha^{\text{reset}} = 1.75$ V^{-1}, $R_s^{\text{set}} = 6.36$ Ω, $R_s^{\text{reset}} = 2768$ Ω, $V^+ = 0.84$ V, $V^- = -0.57$ V, $\eta^+ = 235$ V^{-1}, $\eta^- = 7.23$ V^{-1}, $\kappa w/l = 80$ µA·V^{-2}, and $V_t = 1.5$ V.

the current that flows across the switching device and in this way the voltage between terminals A and D is also limited. As the evolution of the internal state is governed by V_{AD}, partial transitions can occur giving rise to intermediate non-volatile states. Figure 4b shows the evolution of the internal state λ as a function of the compliance current. It can be seen that the internal state λ reaches a different value which increases with increasing compliance current. More conducting channels are activated as the damage caused to the device increases. This introduces the aforementioned dependence between the LRS slopes and the limiting current.

VI. Conclusion

This paper presented the SPICE implementation of a switching device model based on a logistic hysteresis operator that accounts for partial resistive transitions. In particular, the switching element was combined in a 1T1R configuration so as to limit the maximum SET current. As observed in experimental results, it was found that the LRS is highly sensitive to the compliance current suggesting a possible solution to enhance the device stability and reproducibility of the switching loop. The model reproduces successfully experimental data from HfO_2 devices, and proves to be a useful tool to address more complex applications.

Acknowledgment

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ARTICLE **DCIS17**

SPICE model for the ramp rate effect in the reset characteristic of memeristive devices

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SPICE Model for the Ramp Rate Effect in the Reset Characteristic of Memristive Devices

Alberto Rodriguez-Fernandez, Jordi Suñé, Enrique Miranda
Dept. Enginyeria Electrònica
Universitat Autònoma de Barcelona
Spain

Mireia Bargalló Gonzalez, Francesca Campabadal
Institut de Microelectrònica de Barcelona, IMB-CNM (CSIC)
Campus UAB
Spain

Mohamad Moner Al Chawa, Rodrigo Picos
Dept. Física
Universitat de les Illes Balears
Spain

***Abstract*—This paper addresses the role played by the voltage ramp rate in the reset transient of resistive switching TiN/Ti/HfO_2/W devices. The reset parameters extracted from experimental current-voltage (*I-V*) characteristics were analyzed in the charge-flux domain typical of memristive structures. The obtained results allowed proposing an analytic expression for the reset voltage as a function of the ramp rate. This relationship was included in the memdiode model for the SPICE simulator. Close agreement between simulations and experimental results was achieved.**

Keywords—memristor; ramp rate; Resistive Random Access Memory (RRAM)

I. Introduction

Resistive switching memories (RRAMs) are two-terminal passive devices that present nonvolatile variable resistance. In the last years, RRAMs have received great attention due to their remarkable features such as the low program/erase currents, fast speed, endurance, viability for 3D memory stacks and CMOS technology compatibility [1,2]. These devices in combination with complex circuits make up a larger number of potential applications such as memory devices, neuromorphic systems, computational logic units, etc. Very often, RRAM devices are solely characterized in the *I-V* domain. However, representation in the charge-flux (*Q-ϕ)* domain, typical of memristive devices [3] allows differentiating temporal behavior effects hidden in the *I-V* plot. In addition, a compact model for the hysteretic *I-V* loops in resistive switching was recently proposed by one of the co-authors [4]. The model is modular and requires the inclusion of particular features for the temporal behavior associated with the device under consideration. In this work, the *Q-ϕ* domain is used to include dynamic-type improvements in the model. The effect of the ramp rate (*RR*) on the reset voltage of memristive devices obtained from the analysis of curves in the *Q-ϕ* space was included in the memdiode model for SPICE simulator.

II. Fabricated Devices

The devices investigated in this work are 200nm-TiN/10nm-Ti/10nm-HfO_2/200nm-W structures. The HfO_2 layer was deposited at 225ºC by ALD using TDMAH and H_2O as precursors, and N_2 as carrier purge gas. The top and bottom electrodes were deposited by magnetron sputtering. Notice that a 10nm Ti layer was employed as oxygen getter material. The resulting structures are square cells of 15x15µm^2. A schematic cross-section of the fabricated devices is shown in Fig. 1(a). The studied devices exhibit a typical bipolar resistive switching behavior [5]. The physical phenomenon is attributed to the formation and partial disruption of oxygen-deficient conductive filaments due to field and temperature-assisted oxygen vacancy/ion generation and diffusion processes [5].

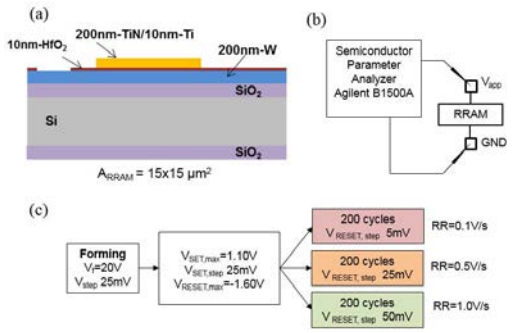

Fig. 1. (a) Cross-section of the fabricated devices. (b) Scheme of the measurement set-up. (c) Flux chart of the measurement procedure.

III. Measurement Procedure

The *I-V* characteristics were measured using an Agilent B1500A Semiconductor Parameter Analyzer (SPA). The voltage ramp was applied to the top electrode, while the bottom electrode was grounded. A scheme of the measurement setup is shown in Fig. 1(b). In order to perform the measurements, first, a forming process was carried out. This process consists in the application of a positive voltage ramp to the top electrode until a current of 5mA is reached. During this step a conductive filament (CF) between both electrodes is

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formed allowing the current to flow through the device and leading the device to the low resistance state (LRS). After that, the reset process was performed by means of a negative voltage ramp that partially destroys the filamentary path and allows reaching the high resistance state (HRS) of the device. Subsequently, a positive voltage ramp was applied to induce the set process, rebuilding the CF and reaching again the LRS.

In this work, the set and reset processes were repeated for 600 cycles. The ramp rate of the reset process was varied by applying a negative voltage ramp up to -1.6V with three different voltage steps of 5, 25 and 50mV. For the set process, a positive voltage ramp with a voltage step of 25 mV was applied up to +1.1V (to avoid cross-correlation with the reset process). The time resolution of the SPA allows obtaining *RR* of 0.1, 0.5 and 1 V/s for the reset process and a 0.35 V/s for the set process (see Fig. 2. (a)). 200 cycles were performed for each *RR*. Figure 1(c) shows a schematic diagram of the measurement conditions of the experiment.

Figure 2 (b) shows a typical bipolar switching for the studied devices, where abrupt set and gradual reset transitions are observed. Notice that V_{reset} increases as *RR* increases. This behavior is consistent with field and thermally activated set and reset mechanisms [6–8]. It is belived that higher *RR* causes a lower heating of the device and therefore a higher current is needed to trigger the reset event.

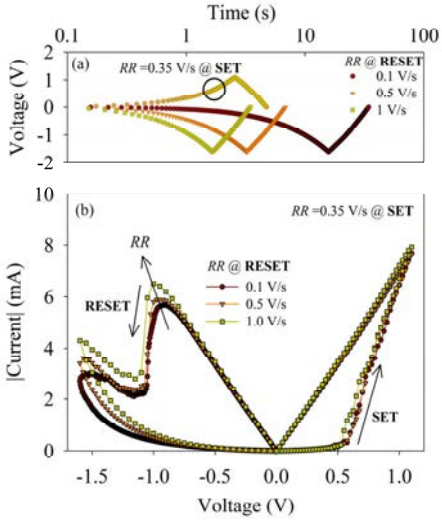

Fig. 2. (a) Applied voltage-time characteristics for set and reset processes at different rates. (b) Measured set and reset current-voltage characteristics for the different applied RR values during the reset process. The set *RR* is kept constant at 0.35 V/s.

IV. Computation of Reset Voltage

Figure 3 shows the *I-V* characteristic reported in Fig. 2 (b) but in the charge-flux (*Q-ϕ*) domain. As proposed by L. Chua and others [3, 9–11], the *Q-ϕ* space for memristor devices allows obtaining useful correlations between variables that can be incorporated into the compact conduction model described in Section V. The charge and the flux magnitudes are defined as the time (*t*) integrals of current and voltage [10], respectively.

The reset point corresponds to the maximum reset current in the *I-V* domain (see Fig. 2. (b)). This value, which is strongly dependent on *RR*, is studied in the *Q-ϕ* domain in order to establish a correlation with *RR* (see Fig. 3(a)). It can be seen that in the *Q-ϕ* space, the charge increase reduces considerably after the reset point is reached. This reduction is due to the small contribution to the time integral of the current after reset. Fig. 3. (b) shows the set process in the *Q-ϕ* space. The set point is indicated. In this case, as expected, once the set point is reached, the charge largely increases.

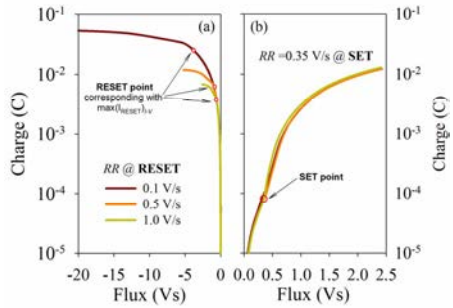

Fig. 3. Q-ϕ characteristics for the (a) reset process and (b) set process.

Figure 4. (a)-(b) show the values for the reset and set charges as a function of the flux for each *RR*. A linear dependence of Q_{reset} as a function of ϕ_{reset} is observed, where the slope ~6mS indicates the conductance in the LRS. The histograms of Q_{reset} for the different *RR* are represented in Fig. 4(c), indicating a clear impact of *RR* on Q_{reset}. In the case of Q_{set} as a function of ϕ_{set}, similar values are obtained for the 600 cycles. This behavior can be attributed to the fact that *RR* during the set process was kept constant. From these results it can be concluded that modifications of *RR* in the reset process do not significantly affect the set point. The conductance value in HRS is 0.16mS.

Since Q_{reset} is the charge needed to activate the reset process and defining τ_{reset} as the corresponding reset time, Q_{reset} reads:

$$Q_{reset} = \int_0^{\tau_{reset}} I \cdot dt \qquad (1)$$

Now taking into account $I=V/R$, R is the LRS resistance (assumed constant), $V(t)=RR \cdot t$, and integrating Eq. (1), the following relationship is obtained:

$$Q_{reset} = \frac{RR \cdot \tau_{reset}^2}{2 \cdot R_{reset}} \qquad (2)$$

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where R_{reset} is the reset resistance. In Fig. 4 (d) Q_{reset} vs. RR is shown, where a power law dependence has been empirically fitted. Considering that $V_{reset}=RR\cdot\tau_{reset}$, V_{reset} can be expressed as follows:

$$V_{reset} = \sqrt{2 \cdot R_{reset} \cdot 2.896 \cdot 10^{-3} \cdot RR^{+0.0295}} \qquad (3)$$

Previous studies suggest an exponential law for RR as a function of V_{reset} [8,12,13] (see Fig. 4 (d)). In our case an empirical law between both parameters, including R_{reset}, was obtained for the studied TiN/Ti/HfO_2/W memristive structures. It is also worth mentioning that from the time-integral of a signal, V_{reset} for an arbitrary input signal other than a ramp can be extracted.

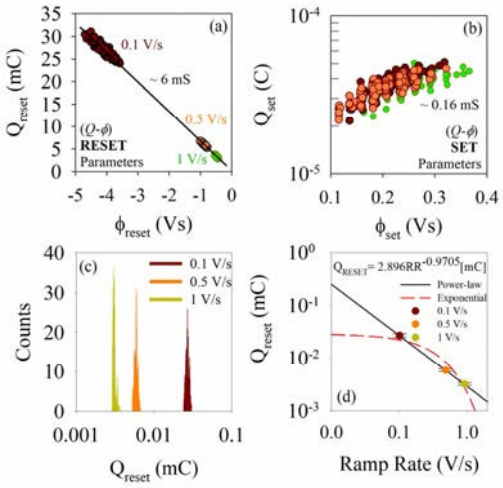

Fig. 4. (a) Q_{reset} vs ϕ_{reset} for the studied RR conditions. (b) Q_{set} vs ϕ_{set} for each RR condition. (c) Histogram of Q_{reset} values. (d) Fitting of Q_{reset} as a function of the RR under power-law (black curve) and exponential (red curve)

V. Simulation Results

The expression for V_{reset} as a function of the RR obtained in the previous Section has been included in a recently proposed model for the I-V curve of voltage-driven memristors [4]. The memdiode model is based on a non-rectifying diode-like expression for the electron transport and the hysteron formalism for the memory state [4]. The model uses two coupled equations, one for the electron transport, expressed as:

$$I = (\alpha R_S)^{-1} W\{\alpha R_S I_0(\lambda) \exp[\alpha(V + R_S I_0(\lambda))]\} - I_0(\lambda) \qquad (4)$$

being α a fitting constant, R_S a series resistance, and $I_0(\lambda)=I_{0max}\lambda+ I_{0min}(1-\lambda)$ the diode amplitude factor. I_{0max} and I_{0min} are the maximum and minimum values of I_0, respectively. Similar expressions as a function of λ can be used for $\alpha(\lambda)$ and $R_S(\lambda)$. Within this approach, the memory state of the device ($0\leq\lambda\leq1$), is expressed as [4]:

$$\lambda_t = \min\{\Gamma^-(V_t), \max[\lambda_{t-1}, \Gamma^+(V_t)]\} \quad t = 1,2,3,... \qquad (5)$$

being λ_t and V_t the discretized values of the state variable and the input signal, respectively. $\Gamma^{\pm}$ are the ridge functions (hysteron's edges) which depend on RR through $V^+=V_{set}$ and $V^-=V_{reset}$ [4]. In its simple form, $\Gamma^{\pm}$ is a logistic function with threshold voltages.

The SPICE circuit schematic for the memristive device is shown in Fig. 5 (a). The circuit is formed by a voltage-driven current source G_M that gives the I-V response and it has two ports PLUS and MINUS that represent the positive and negative terminals of the device, respectively. The evolution of the internal state λ is solved and given by the circuit on the right-hand side, which also contains a voltage-driven current source G_λ. The code for the subcircuit is reported in table I and the SPICE circuit example is shown in Fig. 5 (b). Terminal L gives the hysteron curve.

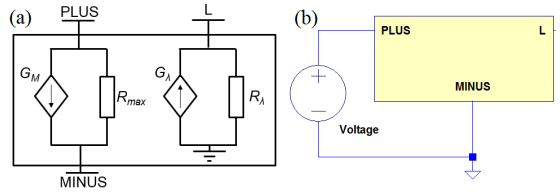

Fig. 5. (a) SPICE circuit schematic. Current source G_M gives the I-V response. The internal state of the memory is given by G_λ. (b) Circuit example where the memristor (yellow box) is used to emulate the behaviour of memristors.

TABLE I. SPICE MODEL CODE

```
* Resistive switching device LTspice model
.subckt res_switch PLUS MINUS L
** Block 1 - Model parameters **
* vset: set threshold
* nset/nres: plus/minus transition rate
* ion/ioff: I0_LRS and I0_HRS
* aon/aoff: alpha_LRS and alpha_HRS
* ron/roff: Rs_LRS and Rs_HRS
* rrst: reset point resistance
* kset/kres: plus/minus sigmoid parameter
* del: delay parameter
    .params
    + ion=1e-2 aon=3.7 ron=130
    + ioff=3.5e-5 aoff=2.0 roff=100
    + kset=-0.2 nset=10 vset=0.82
    + kres=+0.8 nres=30 rres=160
    + del=0.01
** Block 2 - Declare functions **
* w: Lambert W function
* I0: current amplitude factor
* a: alpha factor
* RS: Series resistance factor
* D: delay function
* GGD/S/R: ridge function for plus/minus fuctions
* VRST: reset voltage as a function of RR
    .func w(x)=log(1+x)*(1-(log(1+log(1+x)))/(2+log(1+x)))
    .func I0(x)=ion*x+ioff*(1-x)
    .func a(x)=aon*x+aoff*(1-x)
    .func RS(x)=ron*x+roff*(1-x)
    .func D(x)=delay(x,del)
    .func GGD(x,y,z,k)=1/(1+exp(1.702*log(1-k*z*(x-y))/k))
    .func VRST(x,y)=-abs(ddt(x))*
    + sqrt(2*y*(0.002896*abs(ddt(x))**(-1.9705)))
    .func S(x)=GGD(x,vset,nset,kset)
    .func R(x)=GGD(x,VRST(x,rres),nres,kres)
** Block 3 - Current source - state variable **
* Initial condition
    .ic V(L)=0
    BH 0 L I=min(R(V(PLUS,MINUS)),max(S(V(PLUS,MINUS)),D(V(L)))) Rpar=1
    BR PLUS MINUS I=sgn(V(PLUS,MINUS))*(1/(a(V(L))*RS(V(L)))*w(a(V(L))*
    + RS(V(L))*I0(V(L))*exp(a(V(L))*(abs(V(PLUS,MINUS))+RS(V(L))*
    + I0(V(L))))-I0(V(L))) Rpar=1e10
.ends res_switch
```

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Figure 6 shows experimental and simulated *I-V* curves. The simulation also accounts for the implementation of the charge calculation in the model (VRST in Table I). The model parameters employed for the simulated curve are included in the figure. Good agreement between simulation and experimental results is found. Notice that the simulated reset point is consistent with the experimental data.

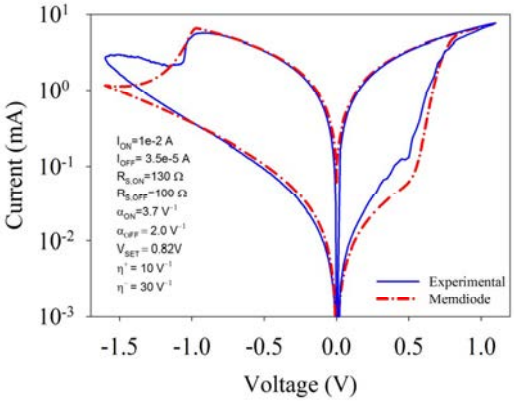

Fig. 6. Simulated I-V characteristics (dash line) and the experimental I-V measures (solid line).

Figure 7 (a) illustrates the model *I-V* response for the investigated ramp rates: 0.1, 0.5 and 1 V/s. V_{RESET} values obtained from simulations are compared with the experimental mean values for each *RR* (see Fig. 7 (b)). The good agreement between the model and experimental data points out the feasibility of the charge-flux method for determining the reset transition point and the viability of the modelization of the ramp rate effect in memristive devices using SPICE.

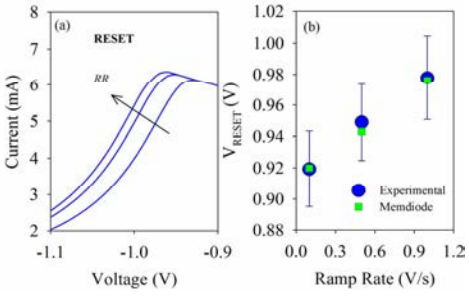

Fig. 7. (a) Simulated I-V characteristics during the reset process for different ramp rates of 0.1, 0.5 and 1V/s. (b) V_{RESET} as a function of RR for the experimental data and simulated Memdiode results.

VI. Conclusions

The current-voltage characteristics of TiN/Ti/HfO_2/W memristive devices were investigated under different *RR* conditions. The results were analyzed in the charge-flux domain and an empirical relationship for the RESET voltages as a function of *RR* was obtained. The memdiode model for hysteretic *I-V* loops in resistive switching structures was modified to account for this effect. The simulated RESET voltages computed via the model were shown to be in good agreement with the experimental results. Future investigations will focus on an extended range of *RR*.

Acknowledgment

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ARTICLE **MEE18**

Characterization of HfO_2-based devices with indication of second order memristor effects

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Characterization of HfO_2-based devices with indication of second order memristor effects

A. Rodriguez-Fernandez[1], C. Cagli[2], L. Perniola[2], E. Miranda[1], and J. Suñé[1]

[1]*UAB NEUROMORPHICS, Departament d'Enginyeria Electrònica, Universitat Autònoma de Barcelona, Cerdanyola del Vallès, Spain*

[2]*CEA, LETI, MINATEC Campus, Grenoble, France*

Abstract

Resistive switching is investigated in TiN/Ti/HfO_2(10nm)/TiN devices in series with a NMOS transistor as selector in a 1T1R configuration. A complete electrical characterization of the devices is carried out using DC voltage loops, constant-voltage stressed and pulses with varying voltage amplitude and time width. Good control of the ON resistance is achieved by applying different transistor gate voltages and multiple OFF states are controllably reached by varying the maximum reset voltage. The on/off resistance ratio is successfully controlled by changing the pulse amplitude and time duration. However, significant memory effects are reported, showing that the switching of a device depends on its switching history. Exploring the on/off ratio for different set and reset voltage amplitudes in otherwise identical set/reset pulse experiments is shown to depend on the order of application of the different stress conditions so that the on/off resistance map in the V_{SET}/V_{RESET} space is not unique. We interpret these results as an evidence of second-order memristive effects.

Keywords: ReRAM, memristor, resistive switching

E-mail address of corresponding author: jordi.suñe@uab.cat

1. Introduction

In the last 15 years novel device technologies have emerged with the aim of replacing or complementing charge-based memories which have an intrinsic scaling issue due to the inability to keep charge within extremely thin barriers [1]. Devices such as random resistive switching memory (RRAM) [2], phase change memory (PCM) [3], and spin-transfer torque memories (STTRAM) [4] have emerged, each of them presenting advantages in terms of scaling and speed. All these memories share the fact that the resistance is used as a probed state variable. The resistance can be changed by application of electrical signals and, in RRAM, the most common situation is that the resistance changes following the state of a conductive filament (CF) created during electro forming within the insulating oxide layer. Since these are very simple two-terminal devices, they can be disposed in a crossbar array, which can be fabricated in the back-end of the line of CMOS processes. This leads to an extremely small bit area of only $4F^2$, where F is the minimum feature size accessible by lithography [5]. Another main advantage of RRAM is that, having short switching times, combined with relatively low-voltage operation, they are suitable for low-power applications. For all these reasons, resistive memories are very promising not only for nonvolatile memories, but also for computing memories, allowing fast data access to overcome the von Neumann bottleneck [6], and in particular for neuromorphic networks [7]. With respect to other candidate devices, RRAM has a good cycling endurance [8], moderately high speed [9], an extremely simple structure (only an insulator between two metal layers), ease of fabrication and good scaling behavior.

In this work, resistive switching is investigated in Ti/HfO_2(10nm)/TiN RRAM devices fabricated at LETI with a NMOS transistor as selector in a 1T1R configuration. These structures are ideal for embedded non-volatile memory applications because the transistor allows to limit endurance issues due to excessive currents, and allows an easy reading without the sneak-path problem. Here we present a full characterization of the performance of these devices using different electrical characterization signals. Voltage Sweep Mode (VSM) experiments are performed to explore the effects of transistor current compliance limit during set (this allows to reach different values of ON resistance), to demonstrate the possibility of controlling several resistance states (multi-state memory) by changing the maximum voltage applied during reset (this allows controlling the OFF resistance within two orders of magnitude) and to study the influence of ramp rate during set and reset. By means of these ramp-rate experiments, information is extracted about the strongly non-linear time-voltage relationship. Pulsed experiments are also performed in a range of ~1V in voltage amplitude and three orders of magnitude in time pulse width (from 100ns to 100μs). It is demonstrated that the R_{OFF}/R_{ON} ratio can be controlled by changing the reset pulse characteristics and that the pulse characteristics have a significant impact on endurance. A maximum endurance of 10^8 is demonstrated. Finally, some experimental indications of the appearance of second-order memristor effects are presented. Second order effects might be very useful for neuromorphics applications [10,11] but might have also an impact on RRAM performance. These second-order effects are intrinsic to the switching mechanisms and a detailed understanding is required for proper device characterization.

2. Experimental details

The samples investigated in this work are 1T1R devices fabricated at LETI (CEA). The MIM structure, sketched in Fig. 1 (a), is formed by a 10 nm-thick ALD HfO_2 layer sandwiched between two metal electrodes (Ti and TiN). To prevent irreversible cell

breakdown and to control the low resistance state (LRS), an NMOS transistor (W/L=5μs/0.35μm) is used in series with the ReRAM device, embedding a 1T1R structure. The transistor does not play any role for the high resistance state (HRS). To activate the adequate switching property a forming step with gate voltage of 1.3 V is required. Quasi-static measurements were performed using the Keithley 4200-SCS semiconductor parameter analyzer equipped with a 4225-RPM PGU (pulse generator unit). Typical *I-V* characteristics for the 1T1R configuration after the forming process are shown in Fig. 1 (b) and Fig. 1 (c) for log-linear and linear-linear representation, respectively, where fifty cycles (gray solid line) were performed with a ramp rate (RR) of 50 Vs^{-1}. The heavy solid line represents the median curve of these cycles (blue solid line). As it can be seen, the devices exhibit bipolar switching with abrupt set and gradual reset transitions. It should be noted that V_{SET} and V_{RESET} are lower than 0.8 V, which suggests that the devices investigated here are suitable for low voltage applications [12]. Notice also the transistor action for positive bias $V > 0.75$ V. The limit imposed by the transistor saturation current allows controlling the damage caused to the ReRAM during the set process.

3. Data analysis and discussion

Figure 2. (a) illustrates the control of the set by the transistor gate voltage. The current compliance level (I_C) is adjusted by setting the transistor gate voltage from 1.2 V to 1.6 V in steps of 0.1 V for set and 4 V for reset condition in any case, being their corresponding I_C levels 140 μA, 240 μA, 352 μA, 470 μA, 600 μA for the set gate conditions and 3.5 mA for the reset gate conditions. Note that since the reset process is thermally activated, the reset gate voltage must be high enough to allow reaching the desired reset current level [13–15]. Notice also the ability to control the compliance current, as well as R_{ON} and I_{RESET}. Figure 2. (b) shows measured reset current as a function of I_C. Reset current scales linearly with I_C, since reset voltage controls the temperature and it has a dependence on the CF size formed during the compliance [1,16]. In addition, Figure 3 shows how the maximum reset voltage controls R_{OFF}. In this case, cycles were performed varying the maximum reset voltage from 0.8 V to 1.2 V. Multiple resistance states can be achived by this procedure. These observations agree with recent publications on the control of HRS [12,17,18].

The devices were also characterized under Constant Voltage Stress (CVS) conditions. Since the set consists in the breakdown of the thin insulator remaining between two CF stumps after the reset, time to set can be identified as the time to breakdown (t_{BD}). These experiments consist in a typical CVS experiment for the set process (positive bias), and a ramp voltage stress for the reset process (negative bias). The experiment consists in 100 cycles performed for each CVS condition (V_{CVS}=0.45 0.50, 0.55, 0.60, and 0.65V). The results of t_{BD} as a function of stress voltage are shown in Figure 4(a). As it can be noticed, an increase of 50 mV in the CVS condition translates into a decrease of an order of magnitude in t_{BD}. On the other hand, if the samples are stressed with a typical VSM experiment for different ramp rates (RR), similar information can be extracted, as shown in Fig. 4(b). I-V-t data were obtained using pulsed measurements with pulse widths ranging from 1 μs to 1 ms, which in combination with a ramp step voltage of 50 mV, yields RR values ranging from 5·104 Vs^{-1} to 50 Vs^{-1}, respectively. V_{SET} and V_{RESET} follow the same logarithmic dependence with RR [19], as it can be seen in Fig. 4 (b). This results are in close agreement with the results reported in [20–23]. Both set of experiments reveal the same trend of one-time decade per 50 mV.

Resistance ratio can be adjusted during pulse measurements by changing pulse amplitude and pulse time duration, as it is demonstrated in Fig. 5. In this case, keeping the set conditions fixed at 1.5 V pulse amplitude and 5μs time width, we vary the reset pulse width time from 100 ns to 100 μs for three different reset pulse amplitudes of 1 V, 1.5 V and 2 V. Each point with its error bar corresponds to the statistics of 200 identical stress cycles. The measurements were performed in a single device. The voltage pulse amplitude affects more significantly the R_{OFF}/R_{ON} ratio that the pulse time width even if voltage is only changed in ~1 V while the time width changes by three orders of magnitude. Note that the R_{ON} value is independent of the reset pulse amplitude as a consequence of the transistor effect. Figure 6 shows the cycle-to-cycle CDF of R_{OFF} for the same data shown in Figure 5. Same variability can be observed for each particular condition. This is due to the highly non-linear time-voltage dependence. Note that this kind of extremely non-linear dependence is a requirement for the successful application of RRAM because of the set-speed/read-disturb trade-off. In these experiments, the on/off ratio is increased by increasing pulse height or width, i.e. by increasing the reset stress and the off-resistance. However, there is a trade-off between high resistance ratio and endurance. The best conditions for high endurance are obtained for a relatively small pulse amplitude. Fig. 7 demonstrates more than 100 Mcycles for V_{pulse}=1.25 V and $t_{RESET} = t_{SET} = 10$ μs.

RRAM devices are memristors [24], i.e. two-terminal electrical devices whose states are described by internal state variables and which are governed by dynamic ionic processes that finally determine and control the electrical conduction properties of the device. Usually, when described mathematically, RRAM devices have been treated as first-order memristors, i.e as having only one internal state variable, namely the device resistance, R. Mathematically, a first-order memristor can be described by

$$\frac{dR}{dt} = f(R,V,t) \tag{1}$$

However, internal switching mechanisms are usually not that simple, and more variables can play a significant role during switching so that a higher-order description might be necessary. In particular, it has been recently shown that temperature T or another variable related to the ionic conductivity in the CF might play a significant role [10,11]. Whenever two variables have significant relevance to determine the internal state of the device, a second-order memristor model is required which is mathematically described as

$$\frac{dR}{dt} = f(R,T,V,t) \tag{2}$$

where T represents the second internal variable which can be the temperature or another variable. Second order memristor effects have been recently shown to allow biorealistic emulation of synaptic functions which can be very useful in neuromorphic circuits showing not only long-term memory but also short-term plasticity [10,11].

In the characterization of our RRAM devices, we have found some experimental results which suggest the occurrence of second-order memristive effects. Fig. 8 shows the results of pulsed experiments in which the voltage pulse amplitude is the same for set and reset (V_{SET}=V_{RESET}) and we explore how R_{OFF}/R_{ON} depends on pulse amplitude and time width. In this experiment, the pulse voltage is monotonously increased from 0.75 to 2.25 V and, for each voltage, the pulse width is increased from 100ns to 10μs and 200 pulses are applied for each stress condition (to obtain a distribution of results for each represented data point). The results are shown in Fig. 8 and it follows that, consistently with what reported in

Fig. 5 and 6, off-resistance and on-off ratio increases with both voltage and pulse width. However, when, at the end of the stress, after applying the most severe reset conditions and reaching a maximum ratio $R_{OFF}/R_{ON} \sim 10^2$, the pulse voltage sequence is repeated for a lower pulse amplitude of 1.25V (in the same time-width space) we find that the results are significantly different (almost one order of magnitude) from what previously found in the same experiment. This is an indication of a dependence of the device performance on its switching history. This indicates that the overall shape of the CF or the ionic mobility or the local stress or any, for the time being unknown, property shows long-term changes which depend on how the device has been stressed and which somehow determine its ulterior switching behaviour. This is a clear case of second-order memristor effects [10,11]. In this particular case, we can in principle discard the temperature as the second state variable because the time scales of our experiments are much longer than expected for heat dissipation [10]. Further investigation is required to unveil the details of high-order memristive effects in these devices but some other results further confirm our conclusions. Figure 9 shows a colour diagram of the resistance ratio (in logarithmic scale) in a V_{SET} vs. V_{RESET} plane. The experiment consisted in the application of pulses with $t_{SET}=t_{RESET}=10$ μs and varying V_{SET} and V_{RESET}. In Fig. 9 (a) V_{RESET} is swept from 0.75V to 2V for each constant value of V_{SET} beginning with the smallest value of V_{SET} and increasing its value after each reset voltage sweep. Alternatively, in Fig. 9 (b) V_{SET} is swept from 0.75V to 2V for each constant value of V_{RESET}. Although one would expect to find the same results for each pair of V_{SET} and V_{RESET} independently of the order that these two variables are changed, the fact is that significant differences are found between the two-colour maps. This provides an independent indication of the fact that switching depends on the previous switching history so that the system cannot be modelled as a first-order memristor. Again, these second-order effects are not likely related to local temperature changes in the CF because heat dissipation is expected to occur in a time scale much shorter than that of the times involved in the experiment. A final experiment consisted in the application of a train of pulses with increasing voltage and constant pulse width but with a variable delay time between them (see inset of Fig. 10 for signal definition). For a first-order memristor, one would expect that changing the delay time would not have any significant effect on the results since only a small voltage is applied to measure the state of the device after each stress pulse. Nevertheless, as shown in Figure 10, decreasing the delay time between pulses accelerates the set transition, and this is exactly what would expect for a second-order memristor. When there is a second variable affecting the internal state of the device, the separation of successive pulses is relevant because the application of one pulse leaves the device in a situation in which it is more prone to potentiation (conductance increase) or depression (conductance decrease) when the following pulse arrives. Since the effects of the second state variable, T in equation 2, usually decay in a shorter time scale and do not cause permanent long-term changes in the memristor internal state, if the separation between successive pulses is long enough, second-order memristor effects are expected to be negligible for long delay times. This is exactly what is found in Fig. 10, in the which the results obtained for the longer values of delay time (100 μs and 1 ms) almost fully coincide while a shift to lower reset voltages and a deeper change of device conductance is progressively found when the delay time is shortened (10 μs and 1 μs). This is another piece of

evidence to support the existence of second-order memristor effects in the RRAM devices studied in this work.

5. Conclusions

We have electrically characterized ReRAM devices with a Ti/HfO_2(10nm)/TiN structure in a 1T1R configuration. We have demonstrated the strongly non-linear relation (~50 mV per time decade) between voltage and set switching time using voltage ramps and constant-voltage experiments. We have checked the efficiency of the transistor in controlling the maximum current during set and the on-resistance. Multiple resistance states are accomplished by varying the maximum reset voltage in VSM experiments. Pulse-based experiments have demonstrated that it is possible to change the on-off resistance ratio by changing pulse width and, more efficiently, the pulse voltage amplitude. However, a set of three different kinds of experiments revealed the existence of second-order memristor effects. This means that there is a second internal state variable that cannot be ignored during device operation or characterization. These effects can be very useful for the operation of these devices in neuromorphic circuits and cannot be ignored when operating the devices as non-volatile resistive memories or for their electrical characterization. Although determining the nature of this second state variable requires a deeper study, we speculate that the stress history determines the geometry of the CF which in turn changes the switching properties in second order.

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Figure captions

1. (a) Cross-section of the fabricated stack. I-V characteristics for quasi-static sweeps (RR = $50Vs^{-1}$), 50 curves (light solid lines) and its median (heavy solid line) in (b) semi-log representation, (c) linear representation.
2. (a) The measured I-V characteristics for a HfO_2 RRAM device at a variable compliance current I_C ranging from 1.2 to 1.6 V. Inset: Scheme of the measurement set-up. (b) Measured reset current as a function of I_C.
3. I-V characteristics show the control of R_{OFF} by maximum reset voltage.
4. (a) Exponential voltage dependence of set (breakdown) time on CVS experiments. Each point represents 100 cycles. (b) Experimental data and trend line for set and reset voltage as a function of RR ranging from $50Vs^{-1}$ to 50 KVs^{-1}.
5. R_{OFF} and R_{ON} in single pulse experiments with different reset pulse amplitude, V_{RESET}=1 V, V_{RESET}=1.5 V and V_{RESET}=2 V (from left to right), and t_{RESET} changing from 100 ns to 100μs. Set pulse kept constant (V_{SET} =1.5 V t_{SET}=5 μs).
6. Cumulative distribution functions (CDF) of R_{OFF} for the collected data in Figure 5.
7. Statistics for the endurance characteristic of the 1T1R device. The resistance ratios of HRS to LRS are more than 10 during the 100M cycles of fatigue test.
8. R_{OFF} and R_{ON} in pulsed (V_{SET}=V_{RESET}) experiments with voltage ranges from 0.75 to 2.25V. Reset time sweeps from 100 ns to 10μs in all the cases. 200 pulses per experiment. Notice that behaviour at 1.25V after applying higher voltages yields different results than after low voltages.

9. Resistance ratio (Log(R_{OFF}/R_{ON}) in pulsed experiments with $t_{SET}=t_{RESET}=10\mu s$ and varying V_{SET} and V_{RESET}. (a) In experiment V_{RESET} is swept from 0.75V to 2V for each constant value of V_{SET}. Alternatively, (b) experiment V_{SET} is swept from 0.75V to 2V for each constant value of V_{RESET}.
10. I-V characteristics keeping the pulse width time fixed to 1μs, and ranging the pulse delay time from 1μs to 1ms. V_G=1.2 V.

FIGURES

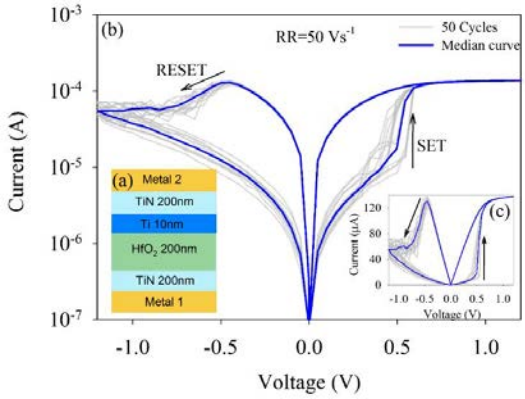
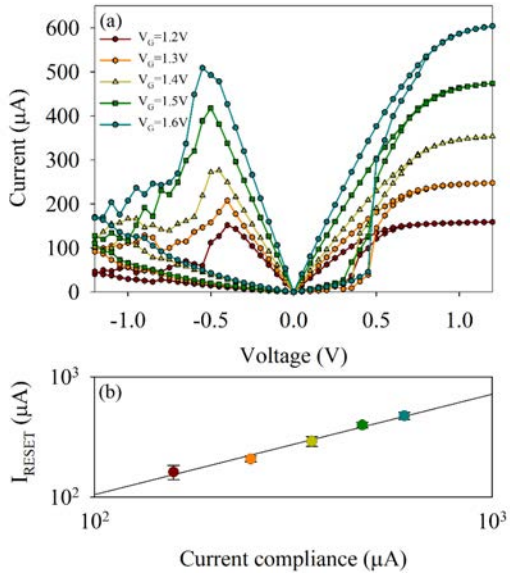


FIGURE 1



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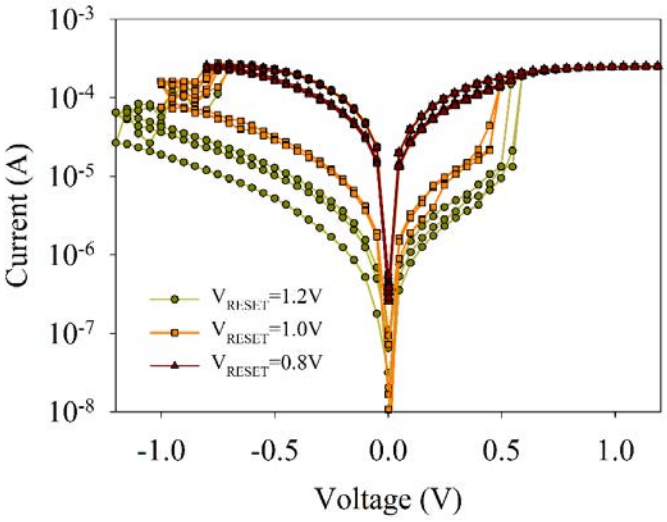

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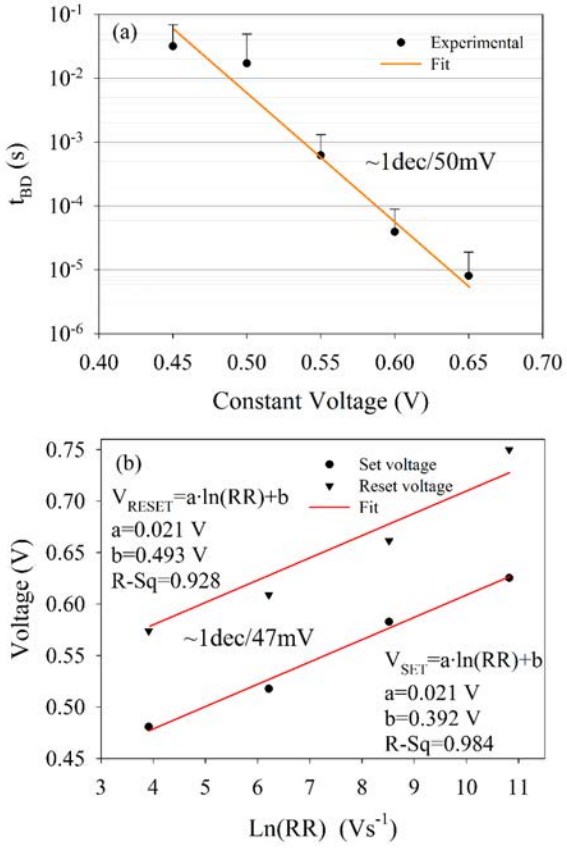

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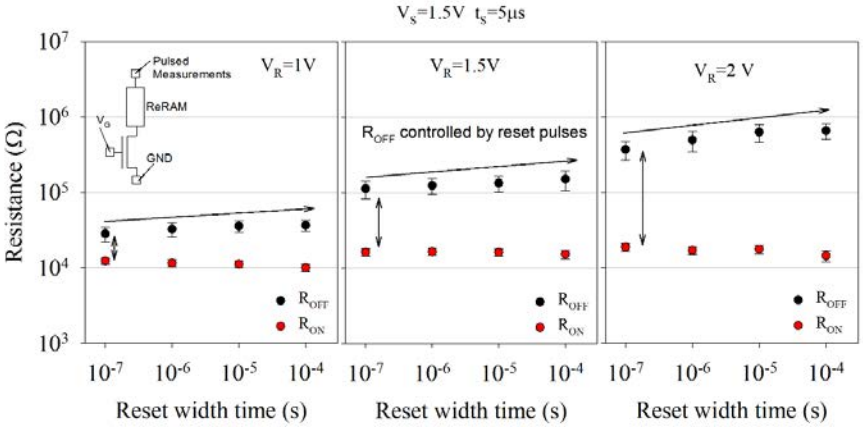

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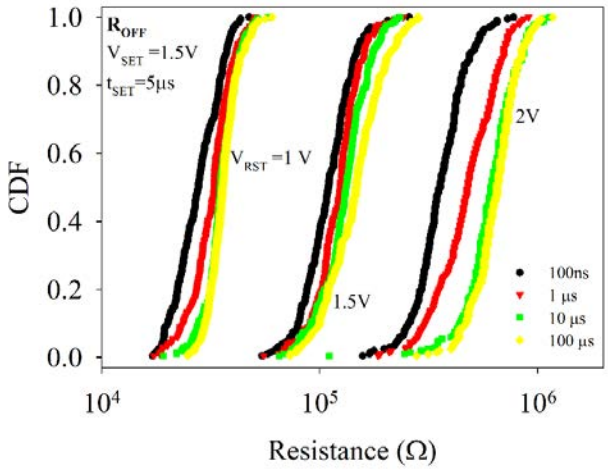

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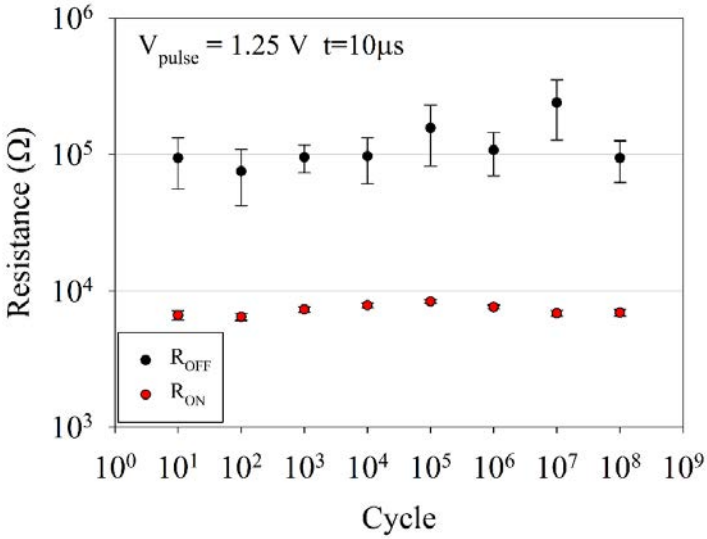

FIGURE 7

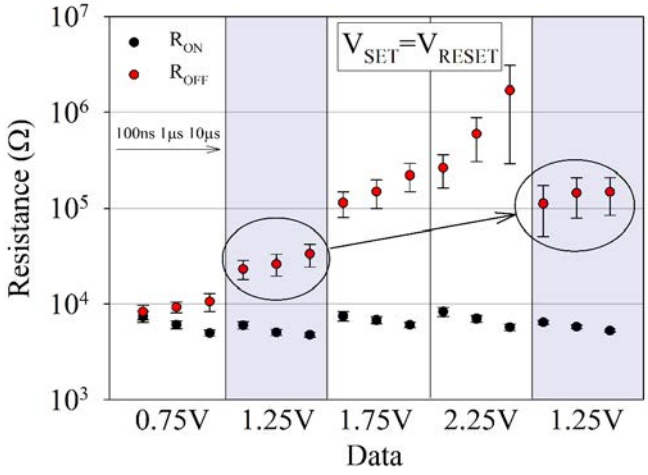

FIGURE 8

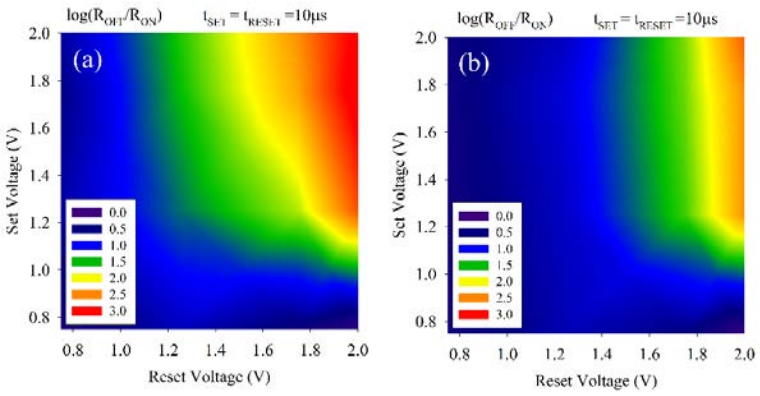

FIGURE 9

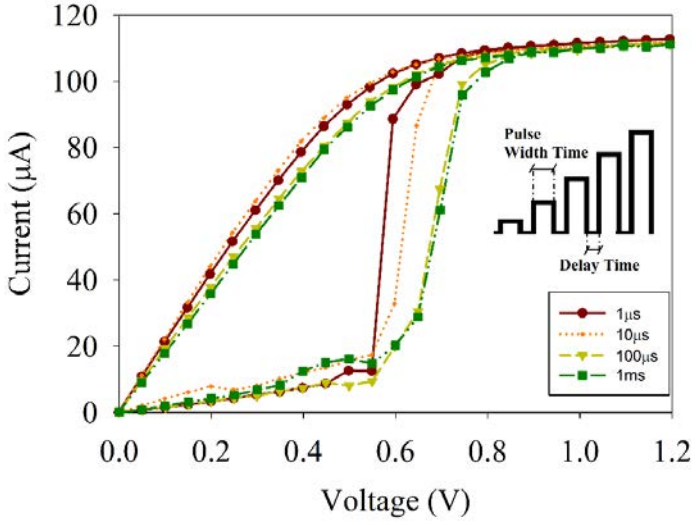

FIGURE 10

ARTICLE **JPD17**

A 3D kinetic Monte Carlo simulation study of resistive switching processes in $Ni/HfO_2/Si\text{-}n^+$-based RRAMs

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A 3D kinetic Monte Carlo simulation study of resistive switching processes in Ni/HfO_2/Si-n^+-based RRAMs

S Aldana[1], P García-Fernández[1], Alberto Rodríguez-Fernández[4], R Romero-Zaliz[3], M B González[2], F Jiménez-Molinos[1], F Campabadal[2], F Gómez-Campos[1] and J B Roldán[1]

[1] Facultad de Ciencias, Departamento de Electrónica y Tecnología de Computadores, Universidad de Granada, Avd. Fuentenueva s/n, 18071 Granada, Spain
[2] Institut de Microelectrònica de Barcelona, IMB-CNM (CSIC), Campus UAB, 08193 Bellaterra, Spain
[3] Departamento de Ciencias de la Computación e Inteligencia Artificial, Escuela Técnica Superior de Ingenierías Informática y de Telecomunicación, Universidad de Granada, 18071 Granada, Spain
[4] Dept. Enginyeria Electrònica, Universitat Autònoma de Barcelona, Edifici Q, 08193 Bellaterra, Spain

E-mail: jroldan@ugr.es

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Abstract

A new RRAM simulation tool based on a 3D kinetic Monte Carlo algorithm has been implemented. The redox reactions and migration of cations are developed taking into consideration the temperature and electric potential 3D distributions within the device dielectric at each simulation time step. The filamentary conduction has been described by obtaining the percolation paths formed by metallic atoms. Ni/HfO_2/Si-n^+ unipolar devices have been fabricated and measured. The different experimental characteristics of the devices under study have been reproduced with accuracy by means of simulations. The main physical variables can be extracted at any simulation time to clarify the physics behind resistive switching; in particular, the final conductive filament shape can be studied in detail.

Keywords: resistive switching memory, variability, simulation, conductive filaments, kinetic Monte Carlo

(Some figures may appear in colour only in the online journal)

1. Introduction

Resistive RAMs (RRAMs) are promising candidates for the next generation of high-density non-volatile memories. Because of their outstanding potential, the scientific community has been following the great number of research works devoted to unveiling the physics behind their operation. RRAMs have a simple structure, excellent scalability, low power, fast speed, the possibility of fabrication in 3D memory stacks and compatibility with the BEOL of CMOS processes [1–14]. The viability of resistive RAMs has been proved at the device level and also in the integrated circuit arena, as reported in [15–17]. The advantages of this technology with respect to flash devices lie in the remarkable improvements they make to the reading/writing speed, endurance, operation power, etc. Nevertheless, several hurdles, such as the poor switching uniformity control, have to be overcome before RRAMs can be incorporated into industrialization lines. This lack of uniformity implies variations in the forming, set and reset voltages as well as in the resistance distribution [1, 7, 13, 14]. Great research effort is needed to clarify the mechanisms behind the physics of resistive switching (RS) and consequently behind device variability. In this context, the availability of simulation tools to analyse the main RRAM operation characteristics linked to charge transport, temperature distribution, etc, is essential in order to deepen the technological development needed prior to commercialization. To contribute to this issue, in this paper we introduce a physically based 3D simulator to describe RRAM operation at a microscopic level.

RRAMs are formed by a dielectric sandwiched between two electrodes. If RS operation is filamentary, as in the most common case, the devices switch between two different resistance states that are obtained by means of the formation and destruction of one or more conductive filaments (CFs). There are different mechanisms for explaining CF formation/disruption; one of these methods is connected with the oxidation and reduction of atoms coming from the active electrode within an electrochemical regime [6, 14, 18]. In this kind of device, after a forming process on a pristine dielectric, it changes from a high-resistance state (HRS) to a low-resistance state (LRS). The device can be switched again to an HRS thanks to the partial dissolution of the CF (reset) and from an HRS to an LRS through a process that regenerates it (set) [1, 4, 6–8, 19, 20]. As a consequence of its simple structure, an RRAM can easily be integrated into a passive crossbar array with a size of $4F^2$, where F is the minimum feature size achievable by lithography. In addition, this size can be reduced to $4F^2/n$ with vertically stacked architectures, where n is the stacking layer number of the crossbar array [1].

For the electrochemical operation mechanism reported above, the set and forming processes are based on the generation of cations by oxidizing active electrode atoms. These cations are dragged by the electric field through the dielectric medium where they can be reduced, usually when they reach the inert electrode. This process forms the CF that bridges the electrodes [3, 9, 21]. If the cation mobility in the dielectric is low enough, instead of travelling along the whole structure, the ions can be reduced close to the active electrode, forming a layer of the same atoms found in it. This layer can be treated as an extension of the electrode, and it is called a virtual electrode [11]; the CF remnants in contact with the electrodes after a reset process can also be considered as virtual electrodes. In devices with the features of the latter, the CFs are formed from the active electrode (the wider part of it is close to the active electrode) to the inert electrode. CFs can also be formed the other way around in high ion mobility dielectrics [1].

There are two types of RRAM, depending on the voltage polarity needed to produce the RS processes: bipolar and unipolar. In unipolar devices, the same polarity is employed for set and reset, whereas for bipolar devices a different polarity is needed [8, 20, 22]. For unipolar devices based on electrochemical mechanisms, the creation of the CF is related to ion generation at the active electrode interface and ion reduction in the dielectric till the CF is fully formed. However, CF destruction is based mainly on thermal phenomena [1, 19]. In this respect, the temperature increase produced in the reset process increases the oxidation and ion diffusion velocities and accelerates the processes that lead to the disruption of the CF. It is clear, then, that the physical description of device operation requires an accurate thermal description of the device, and therefore, the 3D solution of the heat equation.

As explained above, in this work we have introduced a new microscopic simulator to delve into the RRAM physics. Several microscopic RRAM simulators have been developed so far; some of them rely on a 2D description [1, 6, 7], others have been developed in a 3D scheme [8]. A few of them are based on ion generation in the active electrode and a description of their migration as well as the corresponding reduction processes that lead to CF formation [1, 6, 21]. Others describe CF formation by means of oxygen vacancies [7, 8] in the valence change memories; in most cases, the simulator core is based on kinetic Monte Carlo algorithms. Some tools based on the physical description of oxide vacancy CFs are employed to describe complete RS processes, including the initial forming process [7, 8]. However, as far as we know, there are no electrochemical RRAM 3D simulation tools that can describe a forming process followed by several complete RS cycles. Some of them can simulate the forming and set transitions, but cannot reset [6]; others only describe the forming [21] in a partial manner, since the number of simulated ions employed is low [1]. In this context, the inclusion of 3D heat and Poisson equations to account for the RS dynamics is needed [6–8, 19, 20]. Charge transport is described by trap-assisted tunnelling models in certain tools [6–8], while in others a model based on ohmic conduction is employed; in the ohmic conduction case, the CF resistance, the set-up and the Maxwell series resistance components are included [19, 20].

In the simulator, we present here a 3D description for ion generation, and migration is employed within a kinetic Monte Carlo (KMC) algorithm. The 3D Poisson and heat equations are solved at every simulation step. The forming and subsequent complete cycles of the set and reset processes can be simulated continuously for a unipolar device.

The fabricated devices and measurement process are explained in section 2, the simulator features are detailed in section 3 and the main results and discussion are reported in section 4; finally, some conclusions are drawn in section 5.

2. Device description and measurement

The Ni/HfO_2/Si devices were fabricated on (1 0 0) n-type CZ silicon wafers with a resistivity of (0.007–0.013) Ω cm following a field-isolated process. Atomic layer deposition at 225 °C using tetrakis (dimethylamido)-hafnium (TDMAH) and H_2O as precursors was employed to deposit 5 nm thick HfO_2 layers. The top Ni electrode, with a 200 nm thickness, was deposited by magnetron sputtering [25].

The current–voltage (I–V) characteristics were measured at 300 K by means of a HP-4155B semiconductor parameter analyser controlled by GPIB with a PC, using MATLAB. In addition, constant voltage stress measurements (CVS) were performed in order to evaluate the forming time of the devices. The CVS curves were measured using a Keysight B1500 semiconductor parameter analyser, equipped with the waveform generator fast measurement unit (WGFMU) module. The Si substrate was grounded and a positive voltage was applied to the Ni electrode.

The I–V curves of the device measured for positive voltages correspond to an operation regime that is characterized by electrochemical mechanisms that lead to conductive filament formation and disruption (see the I–V formation curve and the several set/reset cycles that follow in figure 1(a)). The use of a positive forming voltage leads to a substrate injection forming (SIF) regime linked to Ni electromigration, as

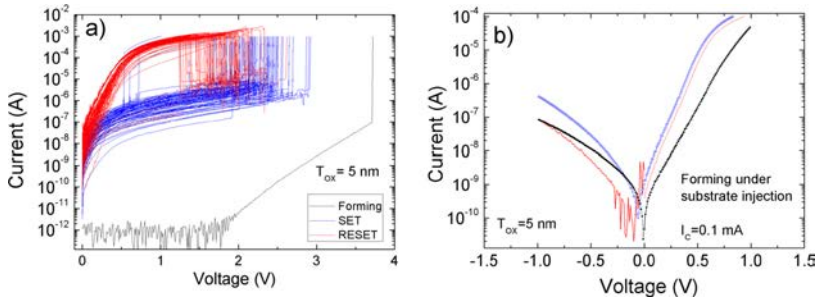

Figure 1. (a) The experimental current versus applied voltage in the RRAMs under study. A forming process and several RS cycles are shown. (b) *I–V* curves (in the LRS state) after a forming process under the regime of substrate injection forming. Self-rectifying behaviour is evident due to the Schottky barrier built between the Ni-based CF and the semiconductor (for the current difference, two decades are obtained for an external voltage of ±0.3 V). The oxide thickness (T_{ox}) is 5 nm.

reported in [25]. The impact of cation migration on Ni-based CF formation has also been studied in [25–28], and can be extended to the case we are presenting here. In our devices, a self-rectifying effect was observed due to the presence of a Schottky barrier between the metallic CF and the semiconductor. The curves in the LRS after a forming process are shown in figure 1(b). Nevertheless, in this manuscript we will only pay attention to the unipolar operation for positive voltages; i.e. the forward bias operation regime.

In the next section we describe a physically based simulation tool and the experimental comparisons needed to tune the main model parameters. We assume that the unipolar operation of the RRAMs reported above is based on redox processes and Ni cation migration.

3. Simulation description

As with the majority of microscopic solid state systems, the dynamics can be characterized reasonably well by the transitions between different states. Due to this, a KMC algorithm is proposed to describe the physics behind the operation of the fabricated RRAMs. A KMC approach takes into account the transition rates between the states found in conventional device operation [29]. This simulation scheme reproduces device RS variability in a natural manner since the physical processes involved in the simulation of the device operation are generated within a stochastic algorithm. The set processes depend on previous reset processes, because the new CF formation uses the remnants of the previous reset as a starting point. The stochasticity of the RS simulation is also linked to the thermal evolution of the device.

The different processes that take place within the system are modelled by the transition state theory (TST), which introduces the rate calculation as in equation (1),

$$\Gamma = \nu \exp\left(-\frac{E_A}{k_B T}\right) \tag{1}$$

following the Maxwell–Boltzmann statistics [6]. Here Γ stands for the transition rate, ν stands for a vibration constant, E_A is the energy barrier height, k_B the Boltzmann constant and T is the temperature. The transition rate corresponds to the inverse of the time needed for a determined mechanism to take place. The activation energy will depend on the electric field and other local characteristics described by the simulator such as the presence of CFs or electrodes. The system can be considered memoryless, and consequently the probability of a determined action taking place for a time duration t can be expressed as follows [6]:

$$P = 1 - \exp\left(-\Gamma \cdot t\right). \tag{2}$$

In the simulations performed, the RRAM physics is described by means of reduction/oxidation reactions, metallic ion movement, ion and atom clustering and the formation and disruption of conductive filaments made of reduced ions.

In the forming and set processes, some important mechanisms are involved like the anodic dissolution of the Ni electrode [1, 5, 9, 18, 21]. This oxidation process is linked to the formation of an ion starting from a neutral atom, which can occur at the electrode's interface or in the dielectric (in the latter case considering atoms linked to previous RS cycles). The reduction process consists of electron capture by the ion, and can occur anywhere. In our case, for the generation of ions we assume that the activation energy depends on the electrode current which induces ion drift within the electrode [2]. The migration of Ni ions through the dielectric toward the bottom electrode and the growth of the Ni filaments is electrically controlled [2, 9, 18]. The formation of CFs bridges the electrodes and makes the device resistance state change from HRS to LRS. After that, the Ni-based CF will be destroyed by Joule heating [1, 3, 19, 30], since this process is carried out with the same polarity as the forming and set process. After the Joule heating process, which increases ion oxidation, there will be ion diffusion and drift till the CF is broken. After the rupture of the CF and the corresponding current drop, the temperature of the device decreases swiftly [3].

Each ion can migrate to any one of the adjacent null sites around it (grid sites without ions or reduced atoms). The ion mobility depends on the energy barrier for ion hopping, whose value is assumed to be the same in all directions and is modulated by the electric field as follows [6]:

$$E_h = E_h\left(V = 0\right) - \frac{Qd\epsilon\left(x,\ y, z\right)}{2} \tag{3}$$

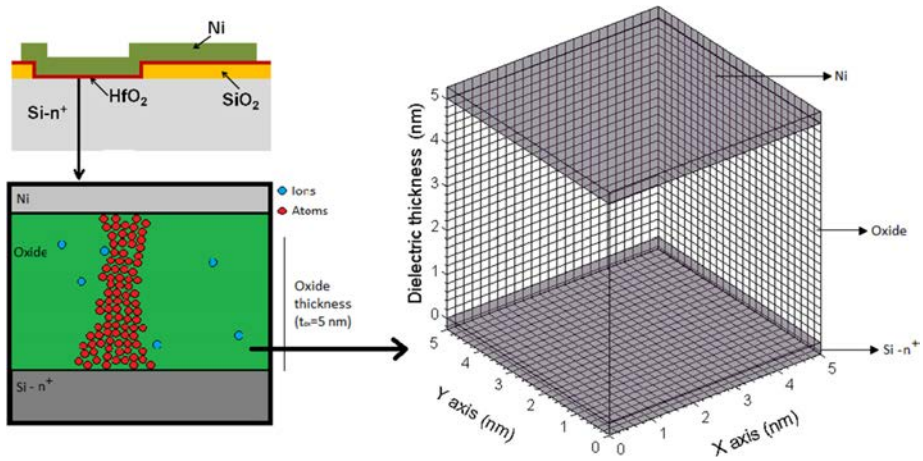

Figure 2. (a) A cross section of the fabricated RRAM and the scheme employed in the simulations. Below, the RRAM stack is shown with a Ni active electrode, an inert Si electrode and a dielectric (HfO_2) in between, where the conductive filament is formed and ruptured. (b) Simulation domain with a 3D grid: the electrodes are shown for clarity. In the simulation domain, the 3D Poisson and 3D heat equations are solved making use of mixed boundary conditions.

where Q is the ion charge, d is the physical distance between the two states, ϵ is the applied electric field and $E_h\,(V=0)$ is the energy barrier for ion hopping in the absence of an electric field. For our simulations we have employed a value of $E_h(V=0)=0.91\,\text{eV}$. Under this simulation approach, a determined electric field enhances ion movement in one direction and hinders the opposite movement.

The activation energy for ion reduction (E_R) or the oxidation of a Ni atom (E_{ox}) is related to the number of atoms surrounding it (n). If the diagonals are not considered, the maximum of atoms that can surround the ion or atom is n_max ($n\_\text{max}=6$). This means that the energy would vary in the following way: $E_R(n)=E_R(0)-n*\frac{0.2}{n\_\text{max}}$ for the reduction energy and $E_{ox}(n)=E_{ox}(0)+n*\frac{0.2}{n\_\text{max}}$ for the oxidation energy (see [1], a 3D generalization has been included here). In our case, the values introduced in our simulation tool are $E_R(0)=0.8\,\text{eV}$ and $E_{ox}(0)=1.0\,\text{eV}$. These energies are important parameters, as their values and connection to other energies influence the final shape of the CF [1]; nevertheless, as we shall show below, the most important processes to consider in the determination of the CF shape are the activation energies linked to ion mobility and generation. In this respect, the relation of the parameters of the latter can make the CF formation start close to the top electrode and grow towards the bottom one, or the other way around. The migration of atoms is ignored since atoms move much more slowly than ions under the influence of an external electric field [1].

Once the ions reach the bottom electrode, it is quite difficult for them to reoxidize, so, the bottom electrode should enhance the reduction of ions and hinder the oxidation of atoms [21, 30]. Taking into consideration these facts, implementation of this phenomenon is reasonable by decreasing the activation energy of the reduction for all the ions that reach the bottom electrode and form a virtual one (the atom cluster formed close to the electrode and connected to it by at least one atom).

Another mechanism included in the simulator accounts for the relation between the external voltage and ion generation. It has been highlighted that there exists a voltage threshold for the forming and set processes [1, 4, 10, 18, 21]. In addition, other studies show that the current through the active electrode produces a potential gradient inside it which drags ions to the sub-surface [2]. We have followed the approach of the latter by using the following expression for the corresponding activation energy:

$$E_g = E_g\,(V=0) - FR_{TE}I_{RRAM} \tag{4}$$

where $E_g\,(V=0)=0.96\,\text{eV}$, R_{TE} stands for the top electrode ohmic resistance (assumed to be 20 Ω) and I_{RRAM} is the total device current; F is a fitting parameter.

The geometric structure of the RRAMs under study is sketched in figure 2(a) [24]. We selected a 3D cubic simulation domain (SD), where the dielectric and the electrode interfaces are included (figure 1(b)). Since the HfO_2 dielectric is 5 nm thick, a 20 point grid is needed on every axis, since the atomic radius of Ni is around 0.125 nm. The z axis in figure 2(b) is perpendicular to the device stack.

The temperature determination is performed by solving the 3D heat equation (expression (5))

$$P(x,y,z) = -K_{th}(x,y,z)\left[\frac{\partial^2 T(x,y,z)}{\partial x^2}+\frac{\partial^2 T(x,y,z)}{\partial y^2}+\frac{\partial^2 T(x,y,z)}{\partial z^2}\right] \tag{5}$$

where $K_{th}\,(x,y,z)=0.49\ \text{W m}^{-1}\,\text{K}^{-1}$ is the thermal conductivity of hafnium oxide [31] and $P(x,\,y,\,z)$ is the power density dissipated at each grid point. Mixed boundary conditions are employed to solve equation (5). A constant temperature is assumed at the electrodes, and adiabatic boundary conditions are used at the lateral faces of the SD. Based on previous work related to the thermal behaviour of RRAM devices [32], we have simplified the calculations linked to the determination of the temperature's temporal evolution.

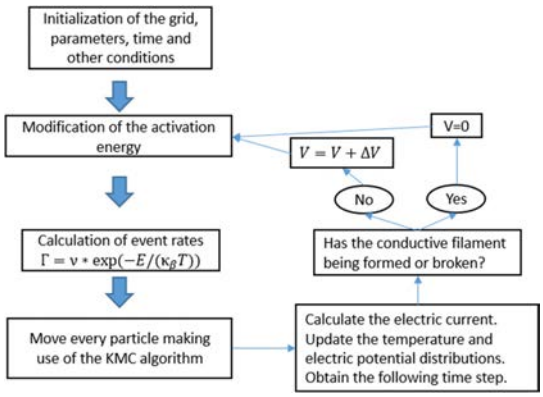

Figure 3. Simulation flow-graph. The KMC algorithm is the key module in the simulator.

For the 3D Poisson equation, we have also employed mixed boundary conditions: a constant voltage is assumed at the electrode interfaces and the Neumann boundary conditions at the lateral faces of the SD. A simplification scheme based on [7] can be used to improve computing-time issues.

In order to use the KMC algorithm, the first step is to calculate all the transition rates to weigh each process statistically. Once the transition rates have been calculated, we can determine an optimized iteration duration time t as follows [6]:

$$t = -\frac{\ln(1 - \text{randm})}{\sum \Gamma}. \tag{6}$$

A random number (randm) between 0 and 1 is employed and the value generated corresponds to the probability of at least one event occurring. As can be deduced, the bigger the sum of all the mechanism rates, the smaller the iteration time t.

In order to select the occurring event we compare the calculated number $r \cdot \Gamma_{\text{Total}}$ (r is a randomly generated number) with the elements of a vector formed by the partial sums of the transition rates $s(j) = \sum_{q=1}^{j} \Gamma_q$. Then, the first event that fulfils the following condition (equation (7)) is chosen,

$$s(j) > r \cdot \Gamma_{\text{Total}}. \tag{7}$$

After the movement of the set of ions within the simulation domain, the simulation flow goes on as depicted in figure 3. We calculated the current and potential at the same time, as in [6], to save computation time.

We have included the calculation of virtual electrodes in the simulator; i.e. the Ni atom clusters within the dielectric in contact with an electrode. In this manner, the effects and phenomena occurring at the electrodes have been transferred to the interface of the virtual electrode. Therefore, the electrode border and the gap between the electrodes changes dynamically along with the simulation.

In the pristine state and the HRS, the main conduction mechanism is described by the Poole–Frenkel model. However, when a fully formed CF shorts the electrodes, the QPC [19, 23]

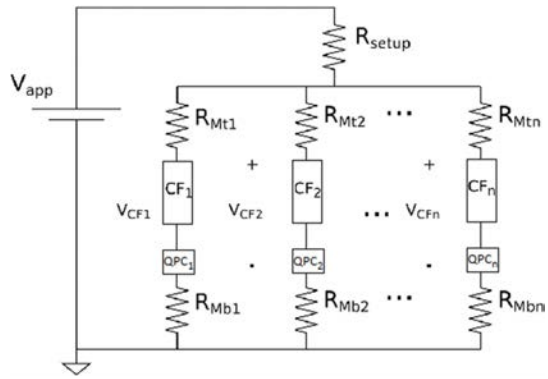

Figure 4. The electrical equivalent circuit considered in the simulator for the current calculation in the ohmic regime (after one or several percolation paths are found). R_{setup} is the resistance that accounts for the electrode resistance, and CF_i is the ith conductive filament across the insulator, QPC_i represents a constriction, and the current through it is described by means of the quantum point contact model [19, 23]. R_{Mti} and R_{Mbi} are the Maxwell resistances in the top and bottom electrodes respectively.

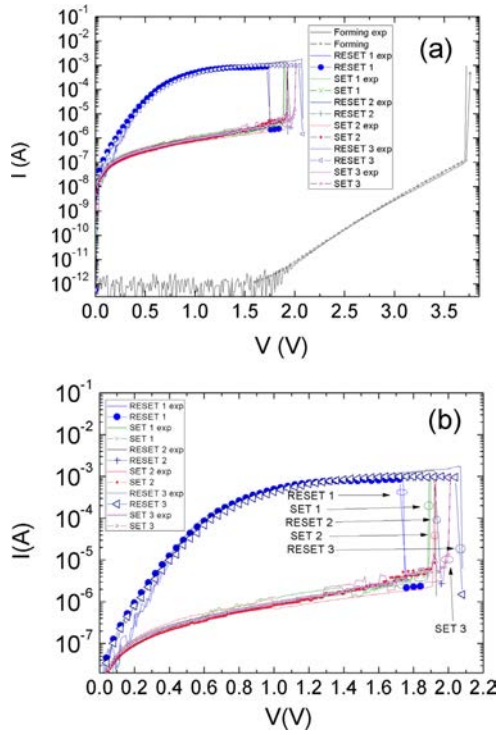

Figure 5. Current versus applied voltage in the RRAM under study. (a) Experimental and simulated data including a forming process and three cycles with their corresponding reset and set processes, (b) the isolated representation of RS curves corresponding to the reset and set processes; the accuracy of the experimental data fit is remarkable.

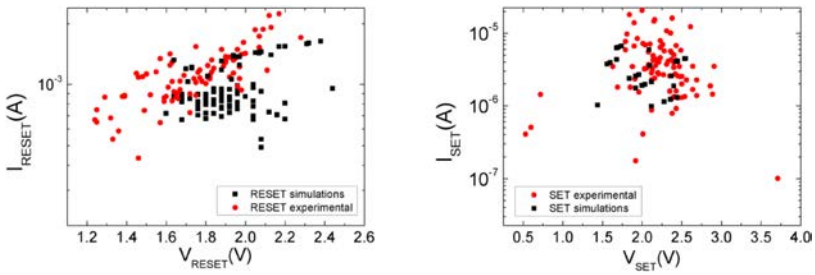

Figure 6. (a) The reset current versus the reset voltage for the RRAMs under study; experimental and simulated data are included. (b) The set current versus the set voltage for the RRAMs under study; experimental and simulated data are included.

and ohmic conduction mechanisms are included, in addition to the Poole–Frenkel model, which is clearly masked by the conduction mechanisms linked to the conductive filaments.

In the ohmic operation regime, after one or more percolation paths are found, we calculate the device current making use of the equivalent circuit shown in figure 4. The simulator can deal with an arbitrary number of CFs and can calculate their time evolution simultaneously. The CF resistance (R_{CF}) is obtained by considering the contribution of each Ni atom to the total CF resistance; therefore, we recalculate this resistance at each simulation step.

A common resistance ($R_{setup} = 40\ \Omega$) is added to model the effect of both the top and bottom electrode resistances, see figure 4. Finally, in series with each CF, Maxwell resistances have been added in order to take into account the funnelling of the current lines from the large electrodes to the narrow CFs [20, 33]. For the sake of generality we have split the Maxwell resistance for each CF into two contributions, since the electrodes are different: R_{Mti} and R_{Mbi} (where i stands for the number of the considered filament). The Maxwell resistances are then given by [33] as:

$$R_{Mt,bi} = \frac{1}{4 r_{\min\_i} \sigma_{t,b}} \tag{8}$$

where $r_{\min\_i}$ is the radius of the narrowest section along the CF and $\sigma_t = 1.43 \cdot 10^7$ S m^{-1} is the conductivity of the top (or bottom $\sigma_b = 1.2016 \cdot 10^5$ S m^{-1}) electrode. In our case, to calculate $r_{\min\_i}$, the narrowest CF section is considered to obtain an equivalent circular area.

The electric conductivity of the cluster of atoms is also supposed to be dependent on the temperature, and is described as:

$$\sigma(x,y,z) = \frac{\sigma_0}{1 + \alpha_T [T(x,y,z) - T_0]} \tag{9}$$

where σ_0 is the electrical conductivity at the reference temperature $T_0 = 300$ K and α_T is the temperature coefficient of conductivity (a value of $\alpha_T = 0.001\,\mathrm{K}^{-1}$ is assumed). The electrical conductivity has been considered as a fitting parameter since the conductive nature of the CF in the ohmic regime is not well understood and is obviously affected by the final CF configuration; in our case a value of $\sigma_0 = 0.5 \times 10^7\ \Omega^{-1}$ m^{-1} was employed.

We included a charge transport mechanism according to the Poole–Frenkel model in addition to the ohmic conduction [34]. The current component in the forming process is described with

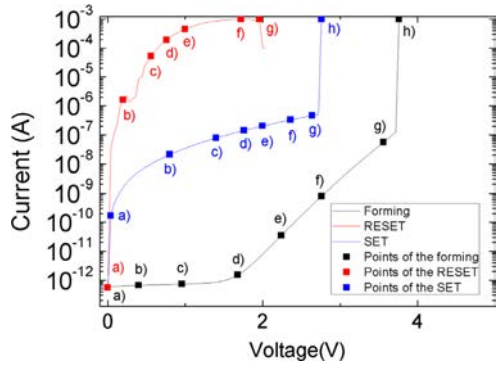

Figure 7. The simulated current versus the applied voltage. The letters along the curves correspond to the stages of the distributions plotted in figures 8–10. A fixed current value has been assumed in the forming curve at low voltages in connection with the minimum resolution of the measurement set-up.

the Poole–Frenkel model [35], making use of the following parameters: $i_0 = 5 \cdot 10^{-12}\,\mathrm{A\,m\,V^{-1}}$ and $\varphi_B = 0.85$ V. For the set curves, the current can also be described in an effective manner by means of the Poole–Frenkel model. We employed an average electric field between the virtual electrodes for this model. When a percolation path was found, the circuit shown in figure 4 was used. For the QPC model we used the following parameters $N = 10$, $\alpha = 4\,\mathrm{eV^{-1}}$, $\beta = 0.9$ and $\Phi = 1.8$ eV. For the reset cycles, when the device is in the LRS, in addition to the previous components, as explained above, we employ the circuit shown in figure 4.

In each iteration, the existence of a percolation path is sought in the simulation domain. The algorithms for the percolation path search [36] (Hoshen–Kopelman in our case) are based on the consideration of classical clusters, where only horizontal and vertical neighbours are considered. Our algorithm also considers the possibility of having more than one percolative path in the same simulation domain. These alternative paths have no cells in common with each other.

4. Results and discussion

Once the simulator had been developed (see supplementary explanation in [37] with the visualization of the 3D KMC simulation), the first step in the tuning process of our simulation

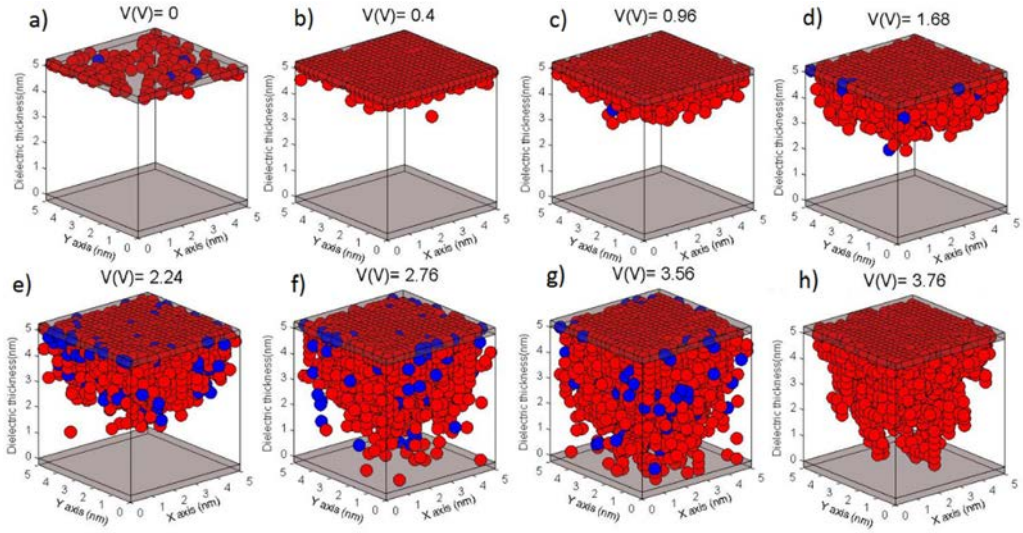

Figure 8. The forming process of the simulated RRAM. The formation of the conductive filament is shown at different stages. Red balls represent Ni atoms, blue ones represent Ni cations; once the filament is formed (h) the only elements shown are the atoms within the percolation path.

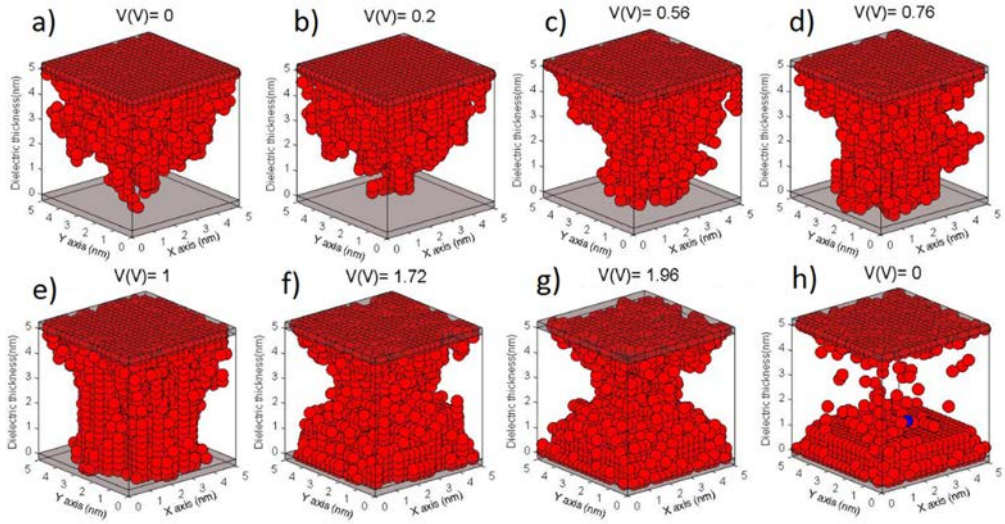

Figure 9. Different stages in a reset process in the simulated RRAM. Red balls represent Ni atoms and blue ones Ni ions. The reset starts at the stage when the forming process was stopped by limiting the device current; after the rupture of the CF the set curve starts with a new ramped voltage.

tool was based on the fitting of different experimental current curves. We were able to reproduce a forming process and an arbitrary number of RS cycles in accordance with the measured data, see figure 5.

In figure 6, the reset current versus the reset voltage and the set current versus the set voltages are plotted both for the experimental (non-consecutive cycles) and simulated data (see [38] for the numerical process of extracting these parameters from the experimental curves). The spread of experimental data in these plots is higher than the simulation results due to the consideration of bigger dielectric areas in comparison with the simulation domain; consequently, several CFs of different sizes can take place at once and the experimental parameter cloud spreads out further. In addition, for the set curves, it must be taken into account that the CF formation process is stochastic and the remnants of previous broken filaments are different in each cycle affecting the set voltages and currents. In figure 6 we can observe a reasonable agreement between the experimental and simulated data, which share a common range of values.

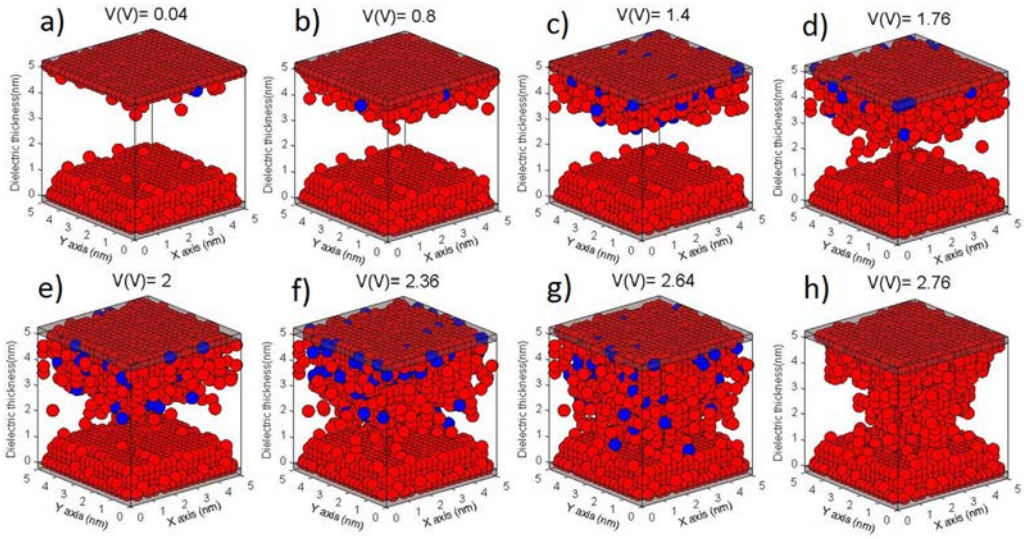

Figure 10. The set process in the simulated RRAM. Red balls represent Ni atoms and blue ones Ni ions. The formation of conductive filaments is shown at different stages.

In figure 7, we plot the simulated *I*–*V* curves of a forming process and the complete RS cycle that follows, consisting of a reset and a set process. Figures 8–10 show the ion and atom microscopic distribution corresponding to the microscopic states of the *I*–*V* curves in figure 7 (marked with letters). In addition, the CF evolution can be seen in figures 8–10.

Within the simulation scheme we follow, it is important to understand that the parameter fitting is not a mechanic process (such as the parameter extraction algorithms that are commonly employed for certain compact models), but a progressive process using many *I*–*V* curves (figure 5), I_{Reset}–V_{Reset} and I_{Set}–V_{Set} distributions (figure 6), etc. Additionally, the basic functioning of these devices presents a high degree of variability due to the stochastic nature of the CF formation/rupture procedures. These characteristics hinder the calculation of a closed set of parameters in a deterministic manner.

In figure 8, we show the different CF creation stages within a forming process. The formation starts close to the interface of the active electrode, because the combination of activation energies controlling the redox reactions and the ion migration processes makes the atoms nucleate close to the active electrode. Therefore, the CF grows towards the counter electrode.

Taking into consideration the stochastic nature of a forming process, a CF with an irregular surface is expected, as can be seen in figure 8. Once the forming process is completed (figure 8(h)), a reset process is started using a ramped voltage again (figure 9). The filament is ruptured by means of thermal mechanisms that are triggered by Joule heating. The temperatures obtained (on the order of 972 K in the hottest spots) are in line with previous results given by other authors [39].

During the reset process, there might be stages where the CF grows in the narrower part (figures 9(c)–(e)), consequently reducing device resistance and increasing current and Joule heating. Later on, the final thermally triggered process takes place till the CF is ruptured (figure 9(h)).

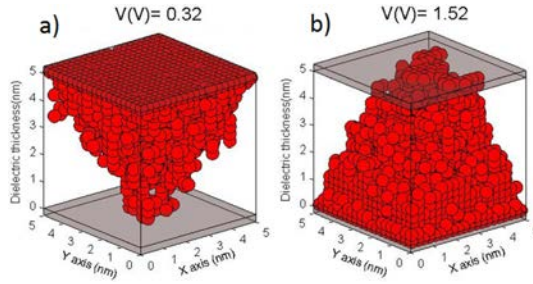

Figure 11. Different CF formation features depending on the activation energies linked to the ion generation rate and ion mobility in the dielectric. (a) $E_{\mathrm{g}} = 0.451\,\mathrm{eV}$ and $E_{\mathrm{h}} = 0.48\,\mathrm{eV}$, (b) $E_{\mathrm{g}} = 0.465\,\mathrm{eV}$ and $E_{\mathrm{h}} = 0.35\,\mathrm{eV}$. The voltage employed for comparison is higher in figure (b) since the time needed to form the CF (the ramped voltages are similar) in case (b) is longer.

Once the reset is over, a set process is launched again with a ramped voltage, making use of the CF remnants shown in figure 9(h) as a starting point (figure 10). Because of the presence of the partially formed CF, the set voltage is lower than the forming voltage, as it should be. In addition, the current in the set process, at low voltages, is much higher than in the forming case since the gap in the dielectric between the virtual electrodes is lower than in pristine devices. Notice that we consider the Ni atom clusters that are in contact with the electrodes to be electrode extensions.

As can be observed in figure 10, the CF reconstruction process is quite similar to what we obtained in the initial forming stage (figure 8). An irregular CF shape was obtained when the percolation path was found, figure 10(h).

This simulator allows the study of different devices (changing the materials and geometric parameters) and operation regimes since it is a versatile tool. Apart from analysing the different physical mechanisms, it allows a model to be developed and

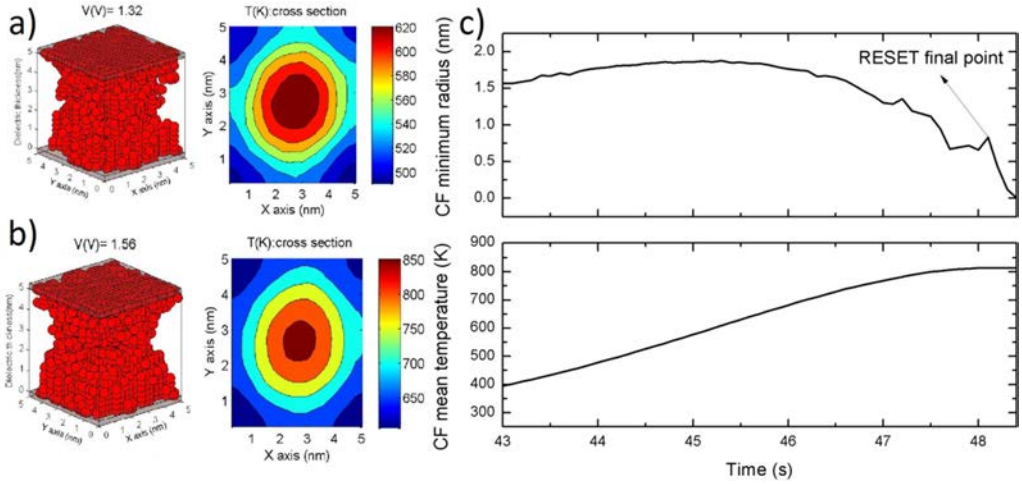

Figure 12. (a) and (b) The CF shapes and corresponding temperature distributions for different voltages corresponding to the reset curve shown in figure 7 (red curve). (c) The CF minimum average radius and CF mean temperature versus time for a transient simulation of a CF rupture, using a constant voltage of $V_{RRAM} = 2$ V. The simulation was initiated just after the percolation path was formed and the narrow region of the CF grows to a 1.5 nm radius.

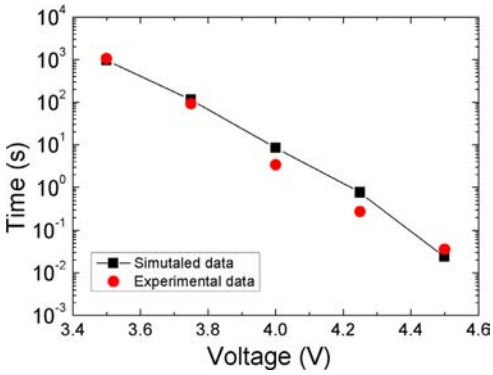

Figure 13. The forming time versus the voltage for constant voltage stress. An exponential dependence of the forming time is obtained with the applied voltage.

helps with parameter extraction in compact modelling for circuit simulation purposes. As an example of these applications, the shape of the CFs can be studied, as shown in figure 11. Different CF formation directions are shown depending on the ion generation and hopping features. It is observed that the activation energies determine the final CF shape that grows from the active to the bottom electrode, or the other way around.

The time evolution of the minimum average radius of the CF (the CFs are not circular, therefore, each CF atomic layer is approximated by a disk of a similar area) and the mean temperature in a CF rupture simulation are shown in figure 12(c). The temperature distributions for two different voltages in a reset curve are plotted in figures 12(a) and (b).

Figure 13 shows the experimental and simulated forming time of the studied devices under CVS conditions. The simulation takes into account the activation energy reduction induced by the electric field, giving rise to excellent agreement with the experimental data. Looking at equation (6), we can observe that the simulation step time is calculated through the transition rates of the processes that take place within the KMC algorithm. These depend exponentially on the activation energy, as shown in equation (1); so, an exponential dependence is inherent in the thermally activated processes behind the physical description of the device (an exponential dependence is seen in figure 13). Besides this, we can find the relationship in previous works [3, 6, 9, 18].

5. Conclusions

A new 3D kinetic Monte Carlo RRAM simulator has been developed and presented here. The 3D Poisson and heat equations are solved to correctly implement the redox, ion migration and nucleation processes that allow the description of the physics behind the operation of resistive memories based on electrochemical processes. Ni/HfO_2/Si unipolar devices have been fabricated and characterized. The measured data was employed to tune the simulator. Different characteristics of the devices under study have been reproduced with accuracy. The evolution of the conductive filaments along the forming, reset and set processes have been analysed in detail. The formation direction of the filament and its shape have also been discussed in terms of the value of the activation energies linked to the ion generation rate and ion mobility in the dielectric.

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Acronyms

Acronym	Description	Page
1R	One Resistor	67
1T–1R	One Transistor–One Resistor	67
AE	Active Electrode	22
AFI	Acceleration Factor Integral	18
ALD	Atomic Layer Deposition	38
BD	Breakdown	9
BE	Bottom Electrode	10
C–V	Capacitance – Voltage	52
CC	Current Compliance	26
CDF	Cumulative Distribution Function	14
CE	Counter-Electrode	22
CF	Conductive Filament	9
CMOS	Complementary Metal-Oxide-Semiconductor	9
CVS	Constant Voltage Stress	12
ECM	Electromechanical Metallization	22
F-N	Fowler–Nordheim	16
GIF	Gate Injection Forming	45
GPIB	General Purpose Interface Bus	13
HBD	Hard Breakdown	10
High-K	High Permittivity	9
HPP	Homogeneous Poisson Process	15
HRS	High Resistive State	20
I–t	Current – Time	52
IT	Interarrival Time	54
I–V–t	Current – Voltage – Time	12
I–V	Current – Voltage	11

Acronym	Description	Page
LRS	Low Resistive State	20
MIM	Metal-Insulator-Metal	10
MIS	Metal-Insulator-Semiconductor	10
MS	Memory Switching	20
NHPP	Non-Homogeneous Poisson Process	15
NVM	Non-Volatile Memory	27
OT	Occurrence Time	54
OTP	One-Time-Programmable	52
OX-ReRAM	Oxide Resistive Random-Access Memory	24
PBD	Progressive Breakdown	10
QPC	Quantum Point Contact	25
ReRAM	Resistive Random Access Memory	9
RR	Ramp Rate	12
RS	Resistive Switching	9
RVS	Ramp Voltage Stress	12
SBD	Soft Breakdown	10
SH	Step Height	54
SIF	Substrate Injection Forming	45
SILC	Stress Induced Leakage Current	10
SMU	Source-Measurement Units	12
SPA	Semiconductor Parameter Analyzer	12
STDP	Spike-Timing Dependent Plasticity	30
TCM	Thermochemical Reaction	22
TDDB	Time-Dependent Dielectric Breakdown	15
TE	Top Electrode	10
TMO	Transition Metal Oxides	19
TS	Threshold Switching	20
V–t	Voltage – Time	70
VCM	Valence Change	22
WGFMU	Waveform Generator and Fast Measurement Unit	12