Universitat Autònoma de Barcelona

ANALYSIS AND MODELING OF FILAMENTARY CONDUCTION IN HfO2-BASED STRUCTURES

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Universitat Autònoma
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DOCTORAL THESIS

ANALYSIS AND MODELING OF FILAMENTARY CONDUCTION IN HfO_2-BASED STRUCTURES

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CERTIFICAN:

que la Tesis titulada "Analysis and Modeling of Filamentary Conduction in HfO_2-Based Structures" ha sido escrita por el Sr. **Alberto Rodríguez Fernández** bajo su supervisión, en cumplimiento de los requisitos del Programa de Doctorado en Ingeniería Electrónica y de Telecomunicación.

Y para certificarlo, firman la presente.

Dr. Enrique Miranda Castellano

Dra. Mireia Bargalló González

Alberto Rodríguez Fernández

Bellaterra, Junio de 2018

A mi familia,

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"Hay tres cosas que cada persona debería hacer durante su vida: plantar un árbol, tener un hijo y escribir un libro" recomendaba el poeta cubano José Martí. Lo que no decía era que nada de ello se puede, ni se debe, hacer solo. Por este motivo me gustaría brindar unas palabras de agradecimiento a todos aquellos que han estado a mi lado durante todo este tiempo.

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Alberto Rodríguez Fernández
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Abstract

We are currently facing a revolution in the fields of microelectronics and information technologies that will surely affect our way of life in the years to come. In this regard, the proposal of a memory device based on the combined action of ions and electrons is considered to be a breakthrough of our time. The basic idea is that an electrical stimulus applied to the device can modulate its resistance state and that this state remains unaltered even when power is turned off. This non-volatile effect can not only be used for storing information but also as a synaptic weight in neuromorphic circuits.

In particular, this Thesis deals with filamentary-based resistive switching cells which rely on the creation and partial dissolution of nanoscale conductive pathways spanning an insulator film. They are often called ReRAMs. The physical principles behind the resistive switching mechanism can be manifold including ion migration and diffusion, chemical reactions, local temperature increase due to Joule heating, and many others. The material investigated in this Thesis is basically HfO_2 but multilayer dielectrics using HfO_2/Al_2O_3 grown by Atomic-Layer deposition are also considered. The structures analyzed are two-terminal metal-insulator-semiconductor and metal-insulator-metal devices, which have been electrically characterized and modeled. Even though an extense part of this work deals with devices that exhibit the resistive switching phenomenon, multilayer stacks were explored as well because of the connection of multifilamentary conduction with one-time programmable memories.

In general terms, the goals of this Thesis have been to increase our knowledge and understanding on the generation of conductive filaments in thin insulating layers and to condense all this information in a compact model able to represent the electrical behavior of the devices.

Resumen

Actualmente nos enfrentamos a una revolución en los campos de la microelectrónica y las tecnologías de la información y la comunicación, que seguramente afectarán nuestra forma de vida en los años venideros. En este sentido, la propuesta de un dispositivo de memoria basado en la acción combinada de iones y electrones se considera un gran avance de nuestro tiempo. La idea principal es que un estímulo eléctrico aplicado de manera adecuada al dispositivo, puede modular su estado de resistencia, el cual puede permanecer inalterado incluso cuando se desconecta la alimentación. Este efecto no volátil no solo puede usarse para almacenar información sino también como un peso sináptico en circuitos neuromórficos.

En particular, esta Tesis se centra en dispositivos que presentan el fenómeno de la conmutación resistiva, mediante la creación y disolución parcial de filamentos de tamaño nanomé trico. Dichos dispositivos son conocidos como ReRAM. Los principios físicos detrás del mecanismo de conmutación resistiva pueden ser múltiples, incluida la migración y difusión de iones, las reacciones químicas, el aumento de la temperatura local debido al calentamiento de Joule y muchos otros. Las estructuras analizadas son dispositivos metal-aislante-semiconductor y metal-aislante-metal, las cuales se han caracterizado y modelado eléctricamente. El material investigado es básicamente HfO_2, aunque también se han estudiado dieléctricos multicapa basados en HfO_2/Al_2O_3, ambos fabricados mediante la técnica de deposición atómica de capas. En esta Tesis tambien se estudian estructuras multicapa, debido a la conexión de la conducción multifilamentaria con memorias programables de una sola vez.

En términos generales, los objetivos de esta Tesis han sido aumentar nuestro conocimiento y comprensión sobre la generación de filamentos conductores en capas aislantes delgadas y condensar toda esta información en un modelo compacto capaz de representar el comportamiento eléctrico de los dispositivos.

Contents

Publications related to this Thesis

Compendium of publications included in this Thesis

1. **A. Rodriguez-Fernandez**, C. Cagli, J. Suñé, and E. Miranda, "Switching voltage and time statistics of filamentary conductive paths in HfO_2-based ReRAM Devices," *IEEE Electron Device Letters*, vol. 39, no. 5, pp. 656-659, May 2018.

2. **A. Rodriguez-Fernandez**, C. Cagli, L. Perniola, J. Suñé, and E. Miranda, "Identification of the generation/rupture mechanism of filamentary conductive paths in ReRAM devices using oxide failure analysis," *Microelectronic Reliability*, vol. 76-77, pp. 178-183, September 2017.

3. **A. Rodríguez-Fernández**, S. Aldana, F. Campabadal, J. Suñé, E. Miranda, F. Jiménez Molinos, J. B. Roldán and M. B. Gonzalez, "Resistive switching with self-rectifying tunability and influence of the oxide layer thickness in Ni/HfO_2/n^+-Si RRAM Devices," *IEEE Transactions on Electron Devices*, vol. 64, no. 8, pp. 3159-3166, August 2017.

4. **A. Rodriguez-Fernandez**, C. Cagli, L. Perniola, J. Suñé, and E. Miranda, "Effect of the voltage ramp rate on the set and reset voltages of ReRAM devices," *Microelectronic Engineering*, vol. 178, pp. 61-65, May 2017.

5. **A. Rodriguez-Fernandez**, J. Suñé, E. Miranda, M. B. González, and F. Campabadal, "Function -fit model for the rate of conducting filament generation in constant voltage-stressed multilayer oxide stacks," *Journal of Vacuum Science & Technology B, Nanotechnology and Microelectronics*, vol. 35, no. 1, p. 01A108, January 2017.

6. **A. Rodríguez**, M. B. Gonzalez, F. Campabadal, J. Suñé, and E. Miranda, "Electrical

characterization of multiple leakage current paths in HfO_2/Al_2O_3-based nanolaminates," *Microelectronic Reliability*, vol. 55, pp. 1442-1445, August 2015.

7. **A. Rodriguez**, M. B. Gonzalez, E. Miranda, F. Campabadal, and J. Suñé, "Temperature and polarity dependence of the switching behavior of Ni/HfO_2-based RRAM devices," *Microelectronic Engineering*, vol. 147, pp. 75-78, April 2015.

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9. **A. Rodriguez-Fernandez**, C. Cagli, L. Perniola, E. Miranda and J. Suñé, "Characterization of HfO_2-based devices with indication of second order memristor effects," in Press, Accepted Manuscript in *Microelectronic Engineering*, April 2018.

10. **A. Rodriguez-Fernandez**, J. Suñé, E. Miranda, M. B. González, F. Campabadal, M. M. Al Chawa and R. Picos, "SPICE model for the ramp rate effect in the reset characteristic of memeristive devices," IEEE Conference Proceedings in *32nd Conference on Design of Circuits and Integrated Systems, DCIS*, November 2017.

11. S. Aldana, P. García-Fernández, **A. Rodríguez-Fernández**, R. Romero-Zaliz, M. B. Gonzalez, F. Jiménez-Molinos, F. Campabadal, F. Gómez-Campos and J. B. Roldán, "A 3D kinetic Monte Carlo simulation study of resistive switching processes in Ni/HfO_2 /Si-n^+-based RRAMs," *Journal of Physics D: Applied Physics*, vol. 50, no. 33, p. 335103, July 2017.

12. G. A. Patterson, **A. Rodriguez-Fernandez**, J. Suñé, E. Miranda, C. Cagli and L. Perniola, "SPICE simulation of 1T1R structures based on a logistic hysteresis operator," IEEE Conference Proceedings in *Spanish Conference on Electron Devices, CDE*, April 2017.

13. X. Lian, M. Lanza, **A. Rodríguez**, E. Miranda and J. Suñé, "On the properties of conducting filament in ReRAM," Conference Proceeding in *IEEE 12th International Conference on Solid-State and Integrated Circuit Technology, ICSICT*, October 2014.

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1. **A. Rodriguez-Fernandez**, J. Muñoz-Gorriz, J. Suñé and E. Miranda, "A new method for estimating the conductive filament temperature in OxRAM devices based on escape rate theory," –Accepted– 29th European Symposium on Reliability of Electron Devices, Failure Physics and Analysis (ESREF18), Aalborg, Denmark, October 2018.

2. J. Cordero, D. G. Romero, I. G. Portillo, J. Muñoz and **A. Rodriguez-Fernandez**, "Modelling of the current compliance effects in the I-V characteristics of memristors devices," 3rd Scientific Meeting of BNC-b PhD Students in Nanoscience, Barcelona, Spain, November 2017.

3. P. Febrer, E. Abellán, A. Aranda, C. Cagli, L. Perniola, J. Muñoz and **A. Rodriguez-Fernandez**, "Indication of second order memristor effects in HfO_2-based devices," 3rd Scientific Meeting of BNC-b PhD Students in Nanoscience, Barcelona, Spain, November 2017.

4. **A. Rodriguez-Fernandez**, C. Cagli, L. Perniola, J. Suñe and E. Miranda, "Identification of the generation/rupture mechanism of filamentary conductive paths in ReRAM devices using oxide failure analysis," 28th European Symposium on Reliability of Electron Devices, Failure Physics and Analysis (ESREF17), Bordeaux, France, September 2017.

5. **A. Rodriguez-Fernandez**, J. Suñe, E. Miranda, M. B. Gonzalez, F. Campabadal, Mohamad Moner Al Chawa and R. Picos, "SPICE Model for the ramp rate effect in the reset characteristic of memristive devices," Design of circuits and integrated systems conference (DCIS17), Barcelona, Spain, November 2017.

6. M. M. Al Chawa, **A. Rodriguez-Fernandez**, F. Campabadal, M. B. Gonzalez, S. Stavrinides, R. Picos, E. Garcia-Moreno and C. de Benito, "Waveform and frequency effects on reset transition in bipolar ReRAM in flux-charge space," International Conference on Memristive Materials, Devices & Systems (MEMRISYS17), Athens, Greece, April 2017

7. **A. Rodriguez-Fernandez**, J. Suñé, C. Cagli, L. Perniola and E. Miranda, "Characterization and modelling of HfO_2-based devices showing second order memristor effects," International Conference on Memristive Materials, Devices & Systems (MEMRISYS17), Athens, Greece, April 2017.

8. **A. Rodriguez-Fernandez**, C. Cagli, L. Perniola, J. Suñe and E. Miranda, "Effect of the voltage ramp rate on the set and reset voltages of ReRAMs devices," 20th Conference on Insulating Films on Semiconductors (INFOS17), Potsdam, Germany, June 2017.

9. G. A. Patterson, **A. Rodriguez-Fernandez**, J. Suñe, E. Miranda, C. Cagli and L. Perniola. "SPICE simulation of 1T1R structures based on a logistic hysteresis operator," Spanish conference on electron devices (CDE17), Barcelona, Spain, February 2017.

10. **A. Rodriguez-Fernandez**, S. Monaghan, J. Suñé, P.K. Hurley, X. Aymerich and E. Miranda, "Nonhomogeneous generation of filamentary paths in High-K oxide films caused by localized electrical stress," International Workshop on Oxide Electronics (IWOE23), China, October 2016.

11. **A. Rodriguez-Fernandez**, M. B. Gonzalez, F. Campabadal, J. Suñe and E. Miranda. "Function -fit model for the generation of conductive filaments in constant voltage stressed multilayer oxide stacks," 19th workshop on dielectrics in microelectronics (WoDiM16), Italy, July 2016.

12. **A. Rodriguez**, M. B. Gonzalez, F. Campabadal, J. Suñe and E. Miranda, "Electrical characterization of multiple leakage current paths in HfO_2/Al_2O_3-based nanolaminates," 26th European Symposium on Reliability of Electron Devices, Failure Physics and Analysis (ESREF15), France, October 2015.

13. **A. Rodriguez**, M. B. Gonzalez, E. Miranda, F. Campabadal and J. Suñe, "Temperature and polarity dependence of the switching behavior of Ni/HfO_2-based RRAM devices," 19th Conference on Insulating Films on Semiconductors (INFOS15), Udine, Italy, June 2015.

14. **A. Rodriguez**, M.B. Gonzalez, F. Campabadal, J. Suñe and E. Miranda, "Breakdown time statistics of successive failure events in constant voltage-stressed Al_2O_3/ HfO_2," 19th Conference on Insulating Films on Semiconductors (INFOS15), Udine, Italy, June 2015.

Preface

Four years ago, when I read the draft of my project Thesis for the first time, I had never heard about the term "filamentary conduction". Back then, I was captivated by the idea of investigating oxide-based ion/electron devices with very tiny active areas acting as central elements in Non-Volatile Memories (NVM). These devices, which rely on the combined action of ions (store the information) and electrons (carry the current), are expected to become in the coming years a paradigm in the field of information storage and neuromorphic computation. Looking back makes me realize that indeed "filamentary conduction" has been the guiding thread of my work at the UAB.

This Thesis focuses on the behavior of Metal-Insulator-Semiconductor (MIS) and Metal-Insulator-Metal (MIM) devices based on Conductive Filaments (CF), whose electron transmission properties can be modified by means of electrical stimuli. The materials investigated were HfO_2 thin films and multilayer dielectrics using HfO_2/Al_2O_3 grown by Atomic-Layer Deposition (ALD). The structures were electrically characterized, analyzed, and modeled. An extense part of this work deals with devices that exhibits the Resistive Switching (RS) phenomenon, which consists in the reversible creation and destruction of a conductive filament in the dielectric. These devices have a potential application as NVM, the so-called (ReRAM) devices. Multilayer structures were also investigated in this Thesis because of the connection of multifilamentary conduction with one-time programmable (OTP) memories. In general terms, the goals of this Thesis have been to increase our knowledge on the generation of CFs and on modeling the electrical behavior of devices based on these kinds of structures.

The obtained results were published in peer-review journals and presented in conferences on the field. This Thesis is organized in the following Chapters:

Chapter 1 provides a general overview about filamentary conduction through a review of the Breakdown (BD) processes and the RS phenomenon of thin films. The failure modes

in ultra-thin oxides which arise as a consequence of the generation of a CF are reported. In addition, some statistical techniques such as the Weibull distribution analysis are described. In case of RS, the generation and annihilation of a CF is a reversible process that can be repeated millions of times. The RS phenomenon shows different operation modes depending on the physical mechanisms involved. Furthermore, the main RS mechanism will be described in this Chapter. A brief introduction to the principal applications of RS devices is also addressed and some issues related to compact modeling of RS devices are introduced.

Chapter 2 is divided into two Sections. The first Section is related to Ni/HfO_2/n^+-Si devices where the RS phenomenon is experimentally studied, including an investigation on the impact of the temperature and the voltage polarity on the RS phenomenology. Attention is focused on the electrical and thermal stability of the CFs. This study is included in paper **MEE15**. Moreover, an in-depth investigation of the electrical behavior of devices with thickness ranging from 5 to 20 nm is presented. This analysis sheds light on the microscopic nature and properties of the CF pathway and the associated electron transport mechanism. This latest study forms part of paper **TED17**. The second Section explores the generation of multiple BD events in Al_2O_3/HfO_2 nanolaminates subjected to constant electrical stress. The BD events arise from the progressive accumulation of defects within the nanolaminate which leads to the formation of filamentary paths for the electron transport. A thorough study of the BD time statistics was carried out. The results of this activity are included in paper **MEE15B**. The role played by the initial leakage current magnitude on the current evolution and a study about the degradation process with the time are also reported in paper **MER15**. Finally, a function fit-model for the generation rate of CF is presented, where the experimental results and analysis can be found in paper **JVS17**.

Chapter 3 deals with RS in MIM devices. The Chapter is subdivided into two Sections again: the first one for one resistor (1R) and the second one for one transistor-one resistor (1T-1R) structures. Both Sections focus on the RS characterization applying fast voltage ramps. In the first part, the RS phenomenon in TiN/Ti/HfO_2/W structures is investigated. The main goal is to obtain information about physical mechanism behind the RS phenomenon and the capability to modulate the conductance. In the second part, TiN/Ti/HfO_2/TiN structures in series with an NMOS transistor are investigated. In papers **MEE17**, **MER17**, **EDL18**, investigations of the switching voltage and time statistics of the filamentary conductive paths by means of oxide failure analysis are reported.

Chapter 4 reports a compact model for the conduction characteristic of ReRAM devices based on a diode-like structure with memory properties, i.e.: the *Memdiode*. Here, the detailed characterization performed in Chapter 3 is incorporated into the compact model

equations, mainly the temporal information. The developed model accurately reproduce the experimental results of 1T-1R and 1R devices.

Finally, **Conclusions** summarize the main contributions of the present Thesis.

The Thesis has been carried out under the framework of the following projects:

• OXITRONICS: Oxide-based ion/electron devices for non-volatile memory and reconfigurable nanoelectronics. Funding institution: Ministerio de Economía y Competitividad and was co-funded by the European Union under the FEDER program. Project coordinator: Jordi Suñe. REF: TEC2012-32305.

• PANACHE: Pilot line for Advanced Nonvolatile memory technologies for Automotive microControllers, High security applications and general electronics. Funding institution: European Comission (JU: ENIAC). UAB local project coordinator: Jordi Suñe.

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Chapter 1

Introduction

THIS Thesis deals with electron devices whose resistance can be altered by the application of an electrical stimulus. In particular, we will focus the attention on filamentary-type conduction devices and High Permittivity (High-K) insulators. To understand the general framework of this work we need to distinguish two closely related phenomena. The first one is called dielectric Breakdown (BD), which is often associated with an irreversible reduction of the electrical resistance of the material. The second one is referred to as Resistive Switching (RS), which is a kind of reversible dielectric BD with volatile or non-volatile properties. In the latest case, the device can be switched on and off many times and it remains in the last resistive state when power is turned off. These phenomena will be the subject of this work.

The BD of thin insulators has been studied for decades due to its importance for Complementary Metal-Oxide-Semiconductor (CMOS) reliability forecast and technology qualification [1]. Much has been learned about the physics and statistics of BD and also about the conduction properties after the BD occurrence. On the other hand, RS properties of thin oxides have been studied since the early sixties and they are the basis of promising non-volatile devices such as the Resistive Random Access Memory (ReRAM). ReRAMs are based on the ON/OFF switching of a localized Conductive Filament (CF) which is created by a soft-breakdown event occurring during the so-called electroforming process. Because of this connection, many findings concerning the BD physics are useful to improve our understanding of RS and are of great help for the development of new non-volatile memory technologies.

In this introductory Chapter, we will present a general overview of filamentary conduction in oxide films, due to BD processes and the RS phenomenon. We will first review the basics of thin-oxide BD mechanism, including some techniques used to measure and analyze the time-to-BD and BD voltage distributions. A brief review about the typical dielectric degradation models is also presented. In addition, the RS modes and their associated physical mechanisms will be presented as well as the possible applications of RS devices. Finally, some issues related to develop a compact model for RS devices is discussed. This Chapter will present some basic concepts and terminologies for RS to introduce the coming Chapters and the compendium of publications included in this Thesis.

1.1 Phenomenology of dielectric breakdown

Dielectric BD of an oxide film consists in the sudden or progressive loss of its local insulating properties compared to those originally exhibited by the fresh material. One of the major features of the BD phenomenon which will be invoked many times along this Thesis is its local nature. The BD phenomenon involves the creation of a CF, which severely affects its insulating property.

Along this work, we deal with two-terminal devices formed by a three-level stack: the Top Electrode (TE), the Bottom Electrode (BE) and the dielectric layer sandwiched in between them. The resulting structures are: Metal-Insulator-Semiconductor (MIS) or Metal-Insulator-Metal (MIM) which are schematically shown in Figure 1.1 (a) and (b), respectively. The BD phenomenon, reversible or irreversible, takes place in the dielectric layer. However, the observation of such phenomenon strongly depends on the electrode and dielectric material combinations. In the next Section, the different failure modes that can occur in such devices are described.

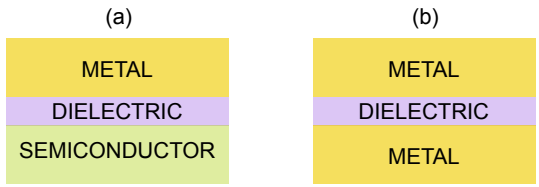

Figure 1.1: Schematic of (a) MIS and (b) MIM structures.

1.1.1 Breakdown modes of thin oxide films

When a stress voltage is applied to an oxide layer, a gradual degradation of the oxide properties occurs, resulting at the end in a sudden local destruction of the film [2]. As it can be seen in Fig. 1.2 (a), the insulating properties of the oxide layer changes mainly in two stages: (1) oxide degradation or wear-out phase (which is area distributed) and (2) oxide Progressive Breakdown (PBD) (which is localized) [3]. At the beginning of stress, in the wear-out phase, traps generated in the material progressively increase the tunneling current flowing through the oxide. This phenomenon, called Stress Induced Leakage Current (SILC) has been extensively investigated in the past [4] since it provides information about the oxide degradation mechanism [5] and its effects on circuit reliability [6].

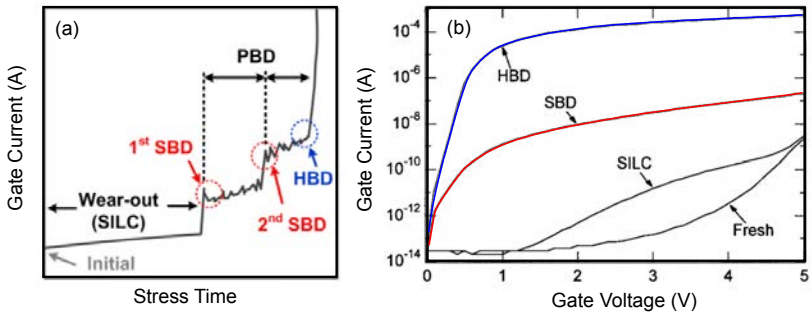

Figure 1.2: (a) Typical behavior for the leakage current as a function of the stress time and (b) typical Gate Current-Gate Voltage (I_G-V_G) characteristics during electrical stress for a capacitor with oxide thickness 4.5 nm [3]. A comparison is made between the current in the fresh device, after stress (SILC), after Soft Breakdown (SBD) and after Hard Breakdown (HBD) [2].

Steady-state SILC is often associated with trap-assisted tunneling from cathode to anode. While in thick oxides, the electrons become trapped by the generated defects and are not easily detrapped, in thin oxides, this current component can be large enough to be detected [2, 7]. For long stress times and high degradation levels in the dielectric, a critical density of traps is locally generated and the current experiences a sudden jump. Depending on the magnitude of the BD event and therefore on the magnitude of the localized current flow, the oxide BD is classified as SBD or HBD. SBD is a partial or quasi-breakdown phenomenon and is associated with a low conduction state. Furthermore, it has been shown that the gate current after SBD is independent of area, indicating that it is a localized effect [8]. HBD is also termed final, catastrophic or total breakdown and is associated with a high conduction level. The Current – Voltage (I–V) characteristic of the dielectric after a SBD

can be described by a power or exponential law while the conduction after a HBD becomes linear, as illustrated in Fig. 1.2 (b) [2].

1.1.2 Electrical characterization methods and experimental setup

1.1.2.1 Characterization techniques

Because of the stochastic nature of BD, a statistically significant number of fresh devices needs to be stressed to obtain a well-defined statistical BD distribution. To this aim, two stress methods are often considered for thin oxide layers. The most straightforward method for characterizing the BD process consists in the application of a Constant Voltage Stress (CVS) while periodically reading the current until BD is detected as a current jump. Then, the time-to-breakdown, t_{BD}, is registered as the natural BD variable (see Fig. 1.3 (left)). A second widely used method to characterize BD is the application of a Ramp Voltage Stress (RVS). In this case, the BD is detected as a current jump during an I–V sweep that determines the BD voltage, V_{BD} (see Fig. 1.3 (right)). As we will see along this work, a critical parameter in the study of the BD phenomenon and the RS behavior is the Ramp Rate (RR), defined as RR = dV/dt. Note also that both CVS and RVS experiments can be much complex depending of the experiment performed, e.g: pulsed ramps. For this reason at the beginning of each Chapter the measurement conditions as well as the electrical characterization method will be presented.

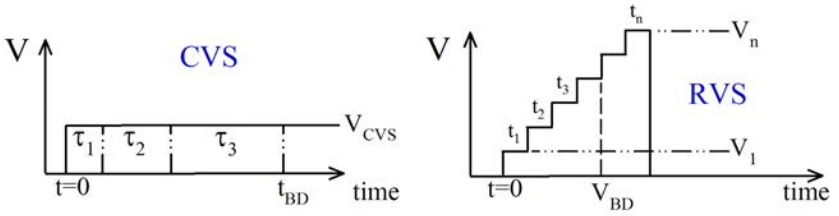

Figure 1.3: Schematic for a CVS experiment (left) and RVS experiment (right).

1.1.2.2 Measurement equipment

The experimental results reported in this work were mainly done during the doctoral research at IMB-CNM (CSIC), Barcelona, Spain and during the research stay at LETI (CEA), Grenoble, France, where two different measurement setups were employed:

♢ Electrical measurements performed at **IMB-CNM (CSIC)**: Most of the measurements were performed at room temperature using a Karl Suss PA200 probe station. A second probe station used was a Cascade Microtech Summit with a Espec. ETC-200L thermal system which enables measurements from -70 °C to 210 °C. Both probe stations are protected from electromagnetic interference by a Faraday box and have triax connectors that allow the connection between the probes and the measurement equipment. For the Current – Voltage – Time (I–V–t) measurements two Semiconductor Parameter Analyzer (SPA) were used. For CVS and quasi-static measurements (no ultra-fast measurements) a HP 4155B SPA was used. The HP 4155B incorporates Source-Measurement Units (SMU) which apply and measure both, voltages and currents at the probe, depending on the selected mode. Moreover, by a code developed in Matlab, temporal information was obtained when measuring each spot current. On other hand, to perform the ultra-fast measurements, the equipment employed was a Keysight B1500A SPA equipped with SMUs and a Waveform Generator and Fast Measurement Unit (WGFMU) which enables high speed I–V measurements with 10 ns programmable resolution.

♢ Electrical measurements performed at **LETI (CEA)**: All the measurements were performed at room temperature using a Cascade Microtech Summit probe station. For the I–V–t measurements a Keithley 4200-SCS SPA was used which incorporates conventional SMUs. The 4200-SCS was also equipped with a 4225-RPM PGU (Pulse Generator Unit). This system was used for applying fast square pulses with a specific waveform and to register data in the time domain, which allow us to obtain important information about the temporal behavior of the samples.

All the measurements obtained by means of these characterization methods will be thoroughly discussed in the following Chapters.

1.1.2.3 Software for instrument control and data analysis

To control the instrumentation and to analyze the obtained data, different software tools were used: In the case of I–V–t measurements, the HP 4155B was controlled via General Purpose Interface Bus (GPIB) using Matlab to automatically perform successive measurements. As the procedure of each experiment was different, for each measurement, the Matlab code had to be conditioned to match the new experiment. For the ultra-fast measurement case with the Keysight B1500A SPA, the measurements were performed and acquired by using the EasyEXPERT software tool. For the Keithley 4200-SCS case, the experiments were performed by means of the Keithley Interactive Test Environment (KITE).

For the data analysis, a Matlab and R code were developed in order to be able to process and analyze thousands of experimental data, and to extract the required parameters. In addition, these developed tools perform the graphical representation of the obtained results.

1.1.3 Weibull and Poisson statistics

Being related to the random generation of defects within the insulator, the BD phenomenon has a random nature and therefore requires a statistical description. t_{BD} is a statistically distributed parameter which can be represented in a histogram. Nevertheless, it is more convenient to plot the Cumulative Distribution Function (CDF), $F(t)$ [2], or even better, a transformation of F. The Weibull distribution is generally accepted as the best statistical model to describe t_{BD} [1]. The Weibull distribution is a weakest-link type distribution. This means that the failure of the whole device is dominated by the failure of the weakest region of the dielectric film [9]. The Weibull CDF is expressed as:

$$F(t) = 1 - \exp\left\{-\left(\frac{t}{\eta}\right)^{\beta}\right\} \tag{1.1}$$

where β is the shape factor of the distribution (indicative of the data spread), or often called the Weibull slope, and η the scale factor or 63rd percentile of the distribution. The interpretation of this type of distribution is usually carried out using the so-called Weibull (Gumbel) plot, in which the Weibit, defined as $W(t) \equiv ln(-ln(1 - F(t))$, is represented versus $ln(t)$ to yield a straight line with a slope β, that is:

$$W(t) \equiv ln[-ln(1 - F(t))] = \beta \cdot ln(t) - \beta \cdot ln(\eta) \tag{1.2}$$

An example of cumulative t_{BD}-distributions is given in Fig. 1.4 for several oxide thicknesses, ranging between 1.7 and 7.8 nm [10]. Fig. 1.4 shows that the t_{BD} distributions are linear when data are represented in a Weibull plot. It can be seen that the parameters β and η depend on the oxide thickness. β decrease with decreasing oxide thickness, in agreement with the percolation model for dielectric BD [11]. An important consequence of the decrease of the Weibull slope for thinner oxides is the strong increase of data dispersion. As mentioned above, Weibull distribution is compatible with the weakest-link property of BD. According to this property, the BD distributions of structures with areas A_1 and A_2 are related to the Weibit values by $W_1 = W_2 + ln(A_1/A_2)$, provided that defect generation is

uniform in area [12]. This is equivalent to:

$$t_{\mathrm{BD}}(A_1) = t_{\mathrm{BD}}(A_2)\left[\frac{A_1}{A_2}\right]^{\frac{1}{\beta}} \tag{1.3}$$

This is also known as Poisson area scaling, which has been experimentally demonstrated for the distributions of t_{BD} and Charge-to-BD Q_{BD} [13].

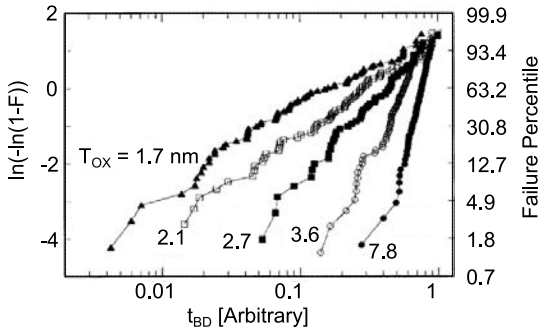

Figure 1.4: Weibull representation for normalized t_{BD}-distributions for oxide thickness from 1.7 nm to 7.8 nm [10].

In Chapter 2, the t_{BD} distributions will be extensively investigated to develop an algorithm for the generation of t_{BD}-times. In this case we will use the Poisson process (in time) which is one of the most widely-used counting processes. It is usually used for scenarios in which we are counting the occurrences of certain events that appear to happen at a certain rate, but completely at random (without a given structure). In our case, the events will be identified with the BD times. Recall that a Poisson distribution is a discrete probability distribution which expresses the probability of a given number of events occurring in a fixed interval of time and whose cumulative density function is given by:

$$F(t) = 1 - \exp(-\lambda t) \tag{1.4}$$

where λ is the failure rate or intensity process (average number of events per unit of time). In a Poisson process with constant λ, the interarrival BD times are exponentially distributed. In this case, we talk about a Homogeneous Poisson Process (HPP). However, λ could also be a function of time ($\lambda(t)$) (called failure rate function). Such counting process is called Non-Homogeneous Poisson Process (NHPP). This kind of Poisson process can be a useful tool to investigate the arrival of events, in particular BD events.

1.1.4 Time dependent dielectric breakdown models

Time-Dependent Dielectric Breakdown (TDDB) refers to the physical process whereby a dielectric subjected to a constant electric field, less than the materials breakdown strength, will breakdown with time. It is important to select the best t_{BD} voltage dependence (acceleration law) model since otherwise the predicted lifetime of a device can deviate several orders of magnitude, specially at the lowest BD percentiles. TDDB is a very important reliability aspect for MOS technologies [14]. Next, the most frequently used TDDB models, which will be used in this Thesis as a phenomenology description and therefore, following an heuristic approach, are explained.

1.1.4.1 Exponential E-model

The E-model, also called thermochemical model, was originally introduced as an empirical model and was later given a theoretical foundation. In this model the cause of low-field ($<$10 MV/cm) and high temperature TDDB is due to field-enhanced thermal bond-breakage. Since the field reduces the activation energy required to break a bond, then the degradation rate is expected to increase exponentially with field. Therefore, t_{BD} occurs when a localized density of broken bonds (or percolation sites) becomes sufficiently high to cause a conductive path to form from anode to cathode [9]. The t_{BD} equation, which is the inverse of degradation rate, decreases exponentially with field,

$$t_{\mathrm{BD}} \propto \exp\left(-\gamma E\right) \tag{1.5}$$

where, γ is the field acceleration parameter and E is the electric field in the oxide which can be estimated as the voltage drop across the dielectric divided by the oxide thickness.

1.1.4.2 Exponential 1/E-model

In the 1/E-Model for TDDB, the damage is assumed to be caused by the current flow through the dielectric (Fowler–Nordheim (F-N) conduction). Electrons, which are F-N injected from the cathode into the conduction band of the dielectric, are accelerated toward the anode. As the electrons are accelerated through the dielectric, because of impact ionization, some damage to the dielectric might be expected. Also, when these accelerated electrons finally reach the anode, hot holes (in the case of semiconductors) can be produced which may tunnel back into the dielectric causing damage (hot-hole anode-injection model). Since both

electrons (from the cathode) and hot holes (from the anode) are the result of F-N conduction, then the t_{BD} is expected to show an exponential dependence on the reciprocal of the electric field, 1/E,

$$t_{\mathrm{BD}} \propto \exp\left(\delta/E\right) \tag{1.6}$$

where, δ is a field acceleration parameter for the 1/E-model [9].

1.1.4.3 Power-law voltage V-model

A power-law voltage model for TDDB has been widely used for gate oxide lifetime projection, specially for very thin oxides [9]. This model is also referred to as the anode hydrogen release model which was originally proposed for hyper-thin dielectrics where ballistic transport dominates [15]. In this case,

$$t_{\mathrm{BD}} \propto V^{-n} \tag{1.7}$$

where n is a field acceleration parameter. For hyper-thin oxide films, the observed exponent is generally in the range: n = 40 - 48.

1.1.4.4 Exponential $\sqrt{E}$-model

For high quality SiO_2, the dominant current flow is nearly always F-N conduction and thus the damage is assumed to follow a 1/E-Model. However, for other dielectrics, or even poor quality SiO_2 dielectrics the conduction mechanism may be Poole-Frenkel or Schottky conduction. Thus, based on current-induced degradation, one might expect a TDDB model of the form,

$$t_{\mathrm{BD}} \propto \exp\left(-\xi \cdot \sqrt{E}\right) \tag{1.8}$$

where ξ is the field acceleration parameter of the $\sqrt{E}$-model [9].

Figure 1.5 shows a comparison between the discussed models in their present state of development [15]. The E-model gives the shortest time-to-failure when the results are extrapolated to the lowest electric fields. The 1/E model gives the longest time-to-failure. One could describe the E-model as being the most conservative and the 1/E-model as being the most optimistic.

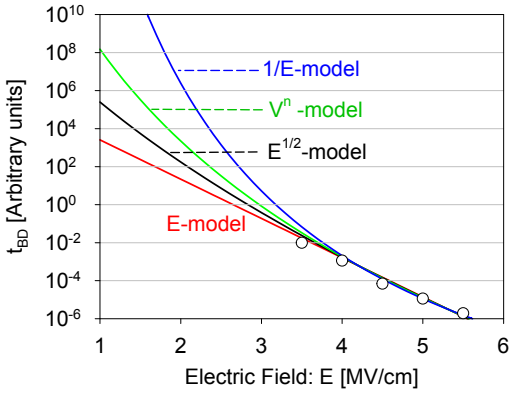

Figure 1.5: The figure shows different acceleration models for TDDB data.

1.1.5 The acceleration factor integral (AFI) method

In reliability physics and engineering, the development and use of the acceleration factor (A_f) is crucial for the theory of accelerated testing. A_f permits one to transform t_{BD} data obtained under different accelerated stress conditions.

In this Thesis, A_f is used for obtaining a relationship between the CVS and RVS methods. In this way, the statistical results obtained from the CVS and RVS methods can be directly related to one another by considering the relation of the BD times with a proper TDDB model. The RVS method is equivalent to a series of discrete CVS with linearly increasing stress voltages. In this way, the Acceleration Factor Integral (AFI) method is used to transform CVS data (V_{CVS}, t_{BD}) into its equivalent RVS data (V_{BD}, RR). Following [16], t_{BD} can be expressed as (see Fig. 1.3):

$$t_{\mathrm{BD}} = \sum_k \tau_k \tag{1.9}$$

where τ_k is the stress time for each voltage step V_k.

$$\tau_k = \Delta t_k \cdot A_f \tag{1.10}$$

and Δt_k is the stress time per step during RVS. A_f is defined as the ratio of the expected t_{BD} under CVS operating conditions to the t_{BD} under RVS stress conditions. Taking into account

that $V = RR \cdot t$, for instance, and using the E-model:

$$A_f(\text{E-model}) = \frac{t_{\text{BD}}^{\text{CVS}}}{t_{\text{BD}}^{\text{RVS}}} = \frac{\exp(-\gamma \cdot V_{\text{CVS}})}{\exp(-\gamma \cdot RR \cdot t)} = \exp(\gamma[RR \cdot t - V_{\text{CVS}}]) \tag{1.11}$$

Converting the sum 1.9 into an integral with limits t = 0 and t = t_{BD} yields:

$$t_{\text{BD}} = \frac{\exp(\gamma[RR \cdot t_{\text{BD}} - V_{\text{CVS}}])}{\gamma \cdot RR} \tag{1.12}$$

This Equation can be manipulated to find interesting correlations between RVS and CVS parameters, since $V_{\text{BD}} = RR \cdot t_{\text{BD}}$.

By means of the AFI method and the appropriate statistics from experiments, we can improve our understanding about the physical mechanism responsible for an eventual breakdown. Although the exact physical mechanism responsible for wear-out and breakdown is still an open question, it is generally assumed that a driving force such as the applied voltage or the resulting tunneling electrons create eletrically active defects in the volume of the oxide film. The defects are accumulated with the stress time and eventually a critical density is reached triggering a sudden loss of the dielectric insulating properties [9].

1.2 Phenomenology of resistive switching

RS alludes to a physical phenomenon in which an insulating material changes its electric resistance by the action of an electric field or current. This change of resistance is characterized by being reversible and non-volatile. The reversibility is achieved by repeated applications of suitable stimuli, which control the resistance value between two or more levels; and non-volatility means that the resistance change remains for a long time after the stimulus has been released.

Historically, studies of RS phenomenon can be dated back to the earlies 1960s. The effect was first reported by T. W. Hickmott (1962) [17] and later by J. G. Simmons and R. R. Verderber (1967) [18] where the phenomenon was observed in MIM stacks with oxide insulators, such as SiO_x, Al_2O_3, Ta_2O_5, ZrO_2 and TiO_2 [17]. During the 1960s and 1970s, multiples studies about RS were performed due to the great interest raised by the phenomenon. Many dielectric materials exhibited these resistance changes and different physical mechanisms were proposed to explain its origin. However, in the 1980s and the beginning of 1990s, research interest in RS declined significantly. This was partly due to the slow progress in understanding the physics of RS and in controlling the RS phenomena.

However, a new era in research on RS gradually started in the mid-1990s. Investigating the magnetoresistive properties of $Pr_xCa_{1-x}MO_3$ (PCMO) in 1997 the Tokura group showed electrically triggered RS [19]. Some time later, in 2002, Zhuang et al. reported the fabrication of the first integrated ReRAM memory, a 64-bit array, using a 500 nm CMOS technology [20] and Baek et al. found the first RS behavior in binary Transition Metal Oxides (TMO) [21]. Moreover, Samsung successfully demonstrated a high-density ReRAM chip using a 180 nm technology and relevant investigations about the redox-based RS mechanism were done by Waser's group in 2006 [22]. From these years on, many works about RS have been published extending the materials showing RS characteristics; proposing new physical mechanisms or completing the existing ones to better describe the RS phenomenon.

1.2.1 Principles of resistive switching

The most described RS mechanism in the literature is filamentary switching, that is, formation and partial dissolution of a CF that act as a switch between the TE and BE. The RS cell can be electrically switched between at least two different resistance states, after an initial electroforming cycle which is usually required to activate the switching property. The forming is generally considered as a SBD of the oxide layer and the initialization of the CF. By applying an appropriate programming voltage pulses or RVS, a cell in its High Resistive State (HRS) can be "set" to a Low Resistive State (LRS) or "reset" back into the HRS. The reset is considered as the partial recovery of the previously induced CF and the set restores the CF in the oxide. Figure 1.6 illustrates a schematic diagram of how the CF is formed and broken. Note, that the reset never takes back the cell resistance to the level of the fresh device, indicating a deep structural change induced by the first programming step (forming). Proof of this is also the higher voltage required during the forming as compared to the set/reset transitions [Cel14, Cel16]. The state of the RS device is detected by applying a read voltage, but this "read pulse" should be not change the resistance state of the RS cell. Notice that for multilevel applications, intermediate resistance states are needed as well. There are several types of RS that will be presented in the next sub-Section.

1.2.1.1 Operation modes

Electroformed oxides present two main types of RS, which are called Memory Switching (MS) and Threshold Switching (TS). They are also known as operation modes. Concretely, the Thesis focuses in MS which is a non-volatile phenomenon, with the two resistance states

being stable at zero bias. While TS phenomenon is volatile and occurs in a limited voltage range.

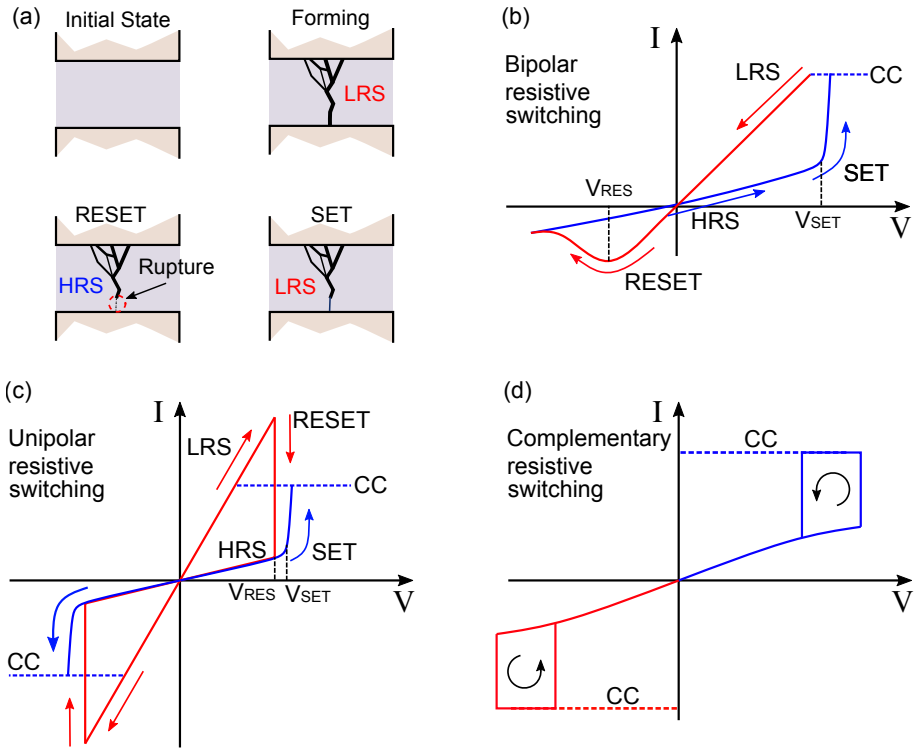

Figure 1.6: (a) Schematics of the forming, reset and set processes. Characteristic I–V sweep for the three most common operation modes of RS elements. (b) Bipolar RS, (c) Unipolar RS and (d) Complementary RS.

Figure 1.6 (b)-(d) shows schematically I–V characteristic diagrams performed by sequential voltage sweeps. Note that the I–V representation is helpful for obtaining an overview of the switching characteristics. In the case of Fig. 1.6 (b) corresponding to bipolar RS, the set process occurs at one polarity and the reset process occurs at the opposite polarity while in the case of unipolar RS (Fig. 1.6 (c)) the set and reset processes occur at the same bias polarity. The structure of the device, i.e. the dielectric/electrode material combinations, determines the RS operation mode. It is generally accepted that the RS phenomenon tends to be bipolar if the electric field plays a significant role, whereas unipolar if only thermal effects take place [23, 24]. Finally, the TS mode shown in Fig. 1.6 (d) is related to complementary RS which can be obtained by connecting two bipolar RS-type ReRAM cells in an anti-serial manner as suggested by Linn et al. [25]. In some cases, such a complementary RS behavior

is also obtained by suitable processing and operation of single RS cells [12, 26]. In Chapter 2 and 3, unipolar and bipolar modes will be investigated, respectively. Complementary RS cases will not be studied in this Thesis.

1.2.2 Physical resistive switching mechanism

In order to explain the RS effect observed in a wide range of materials, several physical mechanisms that govern the set and reset processes have been suggested [27, 28]. The classification of the switching mechanisms which are considered for RS devices are given in Fig. 1.7.

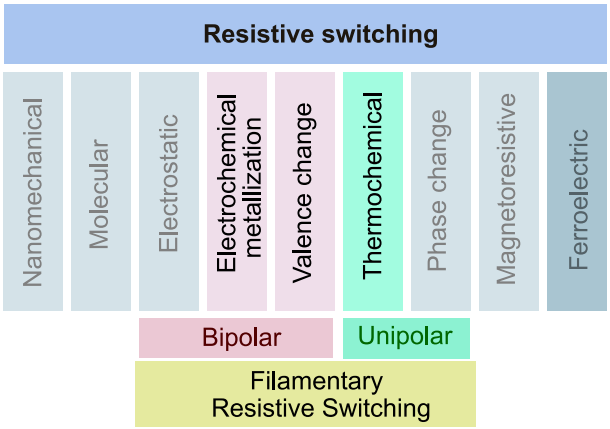

Figure 1.7: Classification of the RS mechanisms which are considered for RS devices.

From all of them, only the three main mechanisms associated to the filamentary devices analyzed along this Thesis will be described. These mechanisms: Electromechanical Metallization (ECM), Valence Change (VCM) and Thermochemical Reaction (TCM) are very similar since the resistance changes of the dielectric are a consequence of the creation/ dissolution of a CF along the dielectric that connects the TE and BE of the RS device. The difference between these three mechanisms stems from the physical processes involved in the creation and disruption of the CF. These processes depend on the material combination of the dielectric layer and the TE and BE as well as the polarity of the applied voltage required to induce the RS. Notice that the same dielectric/electrode material combination, can show more than one switching behavior, for instance, the coexistence of VCM and TCM mechanisms were demonstrated in TiO_2 [29] and HfO_2 [30]. This indicates that the switching behavior is dictated not only by the material type but also by the electrical operation and structural and stoichiometric properties of the dielectric [12].

1.2.2.1 Electrochemical metallization memory

ECM bases its operation on metal cation transport for the filament formation. In this type of cells an electrochemical metal deposition and dissolution is employed to perform the RS operation. The memory element is based on a MIM cell, where a thin dielectric is sandwiched between an Active Electrode (AE) and an Counter-Electrode (CE). Ag, Cu, or Ni are commonly used as the AE; The CE is generally made of Pt, W, Au or TiN. Figure 1.8 schematically shows the basic principle of operation of an ECM memory cell, some important stages (Fresh, LRS, RESET, HRS and SET) of the structure are included.

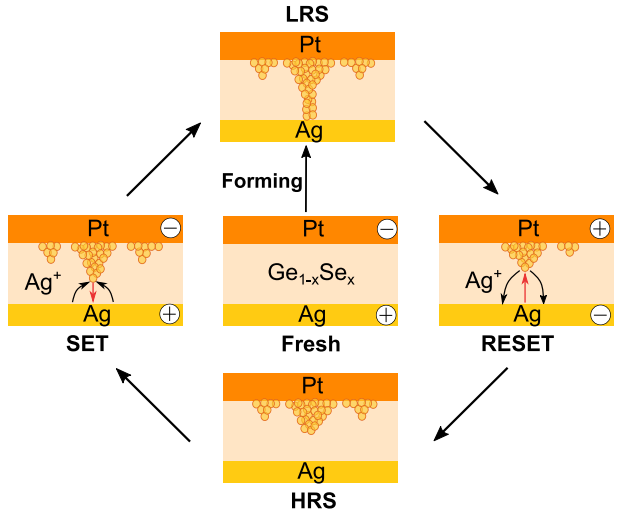

Figure 1.8: Schematic of ECM mechanism where the different stages of the switching procedure are shown.

Initially, when no voltage bias is applied, the device is at a pristine state (Fresh) and no metal ions migrate from the AE into the dielectric layer. Later, by applying a positive voltage to AE, a field-assisted injection and transport of cations begins. Metal atoms are electrochemically dissolved and metal cations are formed. The cations migrate subsequently through the dielectric being, then, deposited on the surface of CE (Forming/set process). This leads to the creation of the CF inside the switching layer, which is called forming/set process as it was explained before. When a sufficient positive voltage is applied to the AE, and an adequate number of cations have migrated and deposited, the metal-based CF is created. The presence of the CF lowers dramatically the resistance of the device thereby defining a LRS. The CF can be dissolved by applying a negative voltage to the AE and thus restoring

the HRS and, therefore, performing the reset process. The resistance change occurs due to an electrochemical dissolution of the metalic CF (reset process) assisted by Joule heating at the narrowest parts of the filament. When the CF has been partially dissolved, the device can be switched back to LRS by applying positive voltages again what performs the set process. Applying successively positive and negative voltages, the device can be switched to HRS and LRS, and vice versa, leading to the creation and partial dissolution of a metallic filament [24, 31].

1.2.2.2 Valence change memory

VCM is based on a redox process involving anion migration (opposite to ECM). In the majority of oxides such as TMO for instance, the oxygen ions are considered more mobile than the metal species [32]. RS is observed in a long list of oxides, including large bandgap dielectrics (SiO_2), most of the existing TMOs (HfO_2, WO_3, TiO_2, Ta_2O_5), rare-earths oxides (CeO_2) and perovskites ($SrTiO_3$, $SrZnO_3$) [23, 28, 33]. The local motion of these defects, typically oxygen anions toward the anode (or described by migration oxygen vacancies toward the cathode), leads change of stoichiometry and a valence change of the cation sublatice associated with a modified electric conductivity. For this reason oxide-based VCM are also referred as Oxide Resistive Random-Access Memory (OX-ReRAM) [27, 33].

In common with ECM, the CF is created during the electroforming process, when the pristine cell is activated. Subsequent set and reset switching can be respectively triggered by means of opposite voltages applied to the device (see Fig. 1.9) [24]. In the ECM case, metal cations are introduced into a solid electrolyte to short the two electrodes in a metallic filamentary path, while in the VCM case, an intrinsic type of defect, oxygen vacancies, are generated in the oxide layer in order to short the electrodes by a conductive path (metallic-rich phase).

The switching mechanism in VCM is generally interpreted as a reversible SBD of an oxide, associated with the generation and migration of oxygen vacancies (V_o) [24] through a field-assisted thermally activated hopping. On a pristine device, the high electric field during forming generates defects in the bulk of the oxide. When subjected to high enough energy, oxygen atoms start to leave their lattice position and drift towards the anode leaving behind a locally conductive path. In Fig. 1.9 (Fresh) a schematic of the VCM mechanism in TiN/Ti/HfO_2 devices is shown. The filament growth is similar to the growth of a virtual cathode, due to the progressive extension of the reduced valence change in the filament location. During the reset process, the oxygen ions migrate back and partially recombine with

the V_o rich filamentary path, switching the memory to the HRS (see Fig. 1.9 (reset)). Applying an appropiate voltage bias again, the device can be switched to LRS state performing the set process and reconstructing the filamentary path (see Fig. 1.9 (set)). The electric-field-induced ionic motion is responsible of the RS phenomenon in VCM as schematically illustrated in Fig. 1.9. Although the electrochemistry is the basis of RS also for VCM, the electrical conduction in the CF will be determined by the transport of electrons in a defect-rich oxide [24].

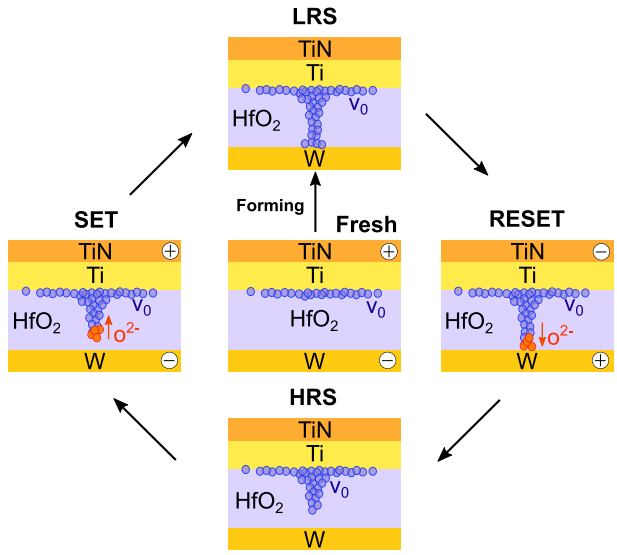

Figure 1.9: Schematic of VCM mechanism in TiN/Ti/HfO_2/W devices. (Fresh) Initial state with a non-uniform distribution of oxygen vacancies. An oxygen deficient region is present in the adjacent region of the Ti layer. (Forming) Local accumulation of oxygen vacancies between BE and the Ti layer, leading to the device to the LRS when set (or forming) process has been performed by applying positive voltage bias to the TE. (Reset) HRS state of the device reached after the application of a negative voltage bias to the TE provoking the reset process.

It has been recognized that RS in VCM or ECM has many similarities with bias-induced dielectric degradation which is generally described by percolation theory [34]. Indeed most of the stress-induced leakage measured in High-K dielectrics for instance, can be attributed among other defects to oxygen vacancies [35]. An analytic model based on filamentary conduction named Quantum Point Contact (QPC) [36] was originally developed by Miranda and J. Suñe [37] for the oxide post-breakdown conduction. This model can be adapted to model the CF in VCM and is based on the idea that the CF behaves as a quantum wire. This model has shown to adequately describe the conduction in the LRS and in the HRS of filamentary ReRAM devices [38, 39].

1.2.2.3 Thermochemical memory

In some cases the switching is not dominated by the electric field but by thermally controlled diffusion and redox reaction. The major microscopic difference between VCM, ECM and TCM mechanisms is revealed by the different switching operation mode. While VCM or ECM based devices need the use of opposite voltage polarities for programming the LRS and HRS states, this change in polarity is not required in TCM systems. Therefore, TCM concepts are inherently unipolar RS mechanisms. Note however, that TCM might be considered as a combination of ECM and VCM since depending on the polarity of the applied voltage during forming and set processes the created filament can be based on metal ions (ECM) or oxygen vacancies (VCM). Consequently, the set process is governed by the diffusion of metal ions or by the migration of V_os. However, for the reset process, the rupture of the CF is considered to be governed purely by thermal diffusion instead of ion dissolution. Notice that the TCM systems need high current levels to produce the reset process. Physically, this type of RS mechanism will be deeply studied in Chapter 2 (for Ni/HfO_2/Si structures).

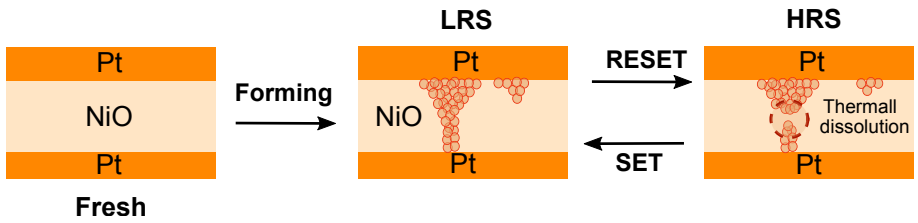

Figure 1.10: Schematic for the fundamentals of the storage mechanism in unipolar RS devices, including preliminary forming for initiating the localized filament, a reset process for the filament thermal rupture and a subsequent set process for the structural recovery of the filament.

Figure 1.10 schematically shows the mechanisms of the switching process in TCM devices. The RS is initiated by the forming operation which results in the formation of a localized breakdown spot, consisting of a highly conductive filamentary path, usually showing a metallic behavior with low resistance. The current increase during the formation (and also during the later set processes) is limited by the Current Compliance (CC) applied during the process, and this in turn, controls the CF diameter. During the reset process, a voltage is applied without a limiting CC. The current increases above the original value of the CC during forming (or set) and a thermally activated reset process due to joule heating results in a partial or total breakdown of the conductive path and subsequent increase of the resistance. As sketched in Figure 1.10, the difference between the pristine state and the HRS is that the filament still exists but is disrupted. The CF can finally be restored during a set transition

consisting of a new dielectric BD of the insulating phase between the residual stubs of the disrupted CF.

1.2.3 Applications of resistive switching phenomenon

RS devices have been proposed to be implemented in many applications such as Non-Volatile Memory (NVM) for crossbar memories, digital logic or artificial neural networks. In this sub-Section issues affecting the NVM functionality are numerated and new emerging applications will be described a bit more extensively.

1.2.3.1 ReRAM devices for non-volatile memories

Among the several applications that stems from RS phenomenon, the most important one is as NVM. NVM is one of the most essential elements of modern electronics. Since the 1990s, the dominant form of NVM has been FLASH memory due to its scalability and fast read/write speeds. However, FLASH memory approaches scaling limit and introduces complexity for integration of high-density memory application. Diverse types of non-volatile random-access (RAM) memory devices, such as phase change RAM (PCRAM), magnetoresistive RAM, (MRAM), ferroelectric RAM (FeRAM), and resistive RAM (ReRAM), have been actively studied in a last couple of decades to find alternative to FLASH. Among these, ReRAM devices based on non-volatile RS have attracted attention due to their scalability, lower power consumption, faster switching speeds, longer retention times, and simpler device structure. Additionally, ReRAM can be easily integrated into solid-state circuits, is compatible with CMOS technology and possesses all the properties required for universal memory.

However, for any memory technology, reliability is a major concern. Most widely known reliability characteristics of ReRAM devices are the data retention (ability to store data for extended periods of time in a specified temperature range), the endurance (ability to rewrite the data multiple times) and program variability [12]. A brief description of these concepts is given as follows:

► **Retention:** RS devices are mainly characterized by the non-volatile behavior of their states. However, the retention of those states is not boundless. The increase of the temperature, the operation time or simply the aging can provoke variations on HRS and LRS resistances which originate the retention failure. Typical nonvolatile memory requires 5–10 years data retention up to 85 – 125 °C [12].

► **Endurance:** Most memory applications require the ability to rewrite stored data. Conceptually, endurance refers to the maximum number of switching cycles performed by a device until the decrease of the resistance window to an unacceptable value or to its complete closure, mostly related to the final failure of the device. Endurance and data retention are two of the most important reliability characteristics defining the application domain of a certain memory technology. Filamentary-based bipolar switching TMO ReRAM, in general, demonstrates good cyclability (currently $\sim 10^{10}$ cycles) [12].

► **Variability:** Variability is understood as those fluctuations of RS operation parameters such as forming, set and reset voltages or resistance states (or related currents). Fluctuations refer to any change in the value of a parameter appearing due to the stochasticity of the RS operations mechanisms. They can be observed between different devices (device-to-device), known as spatial variability, or in a single device between the subsequent set/reset cycles (cycle-to-cycle), known as temporal variability. Another reason for the RS parameters variability is the impact of fixed parameters such as CC which can provoke fluctuations in operation parameters when its value is varied.

In the context of RS devices as NVM, crossbars, which are implemented with mutually perpendicular layers of parallel wires (electrodes) with integrated thin-film devices at the cross points, have the best scaling prospects (see Fig. 1.11 (a)). According to the international technology roadmap of semiconductors (ITRS), crossbar memory is a potential candidate to become a universal memory, which would combine the best characteristics of other types of memories [40]. The basic operation of crossbar memories can be explained using simplified equivalent circuits as shown in Fig. 1.11 (b) and (c).

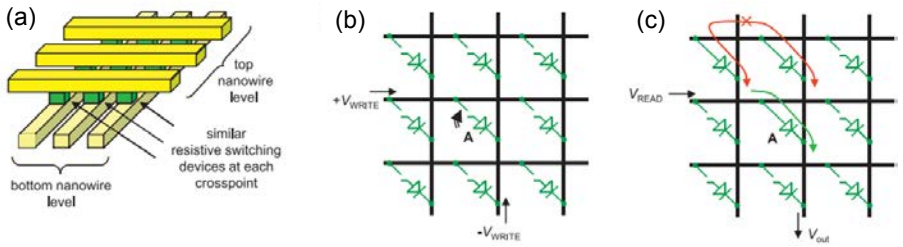

Figure 1.11: Passive crossbar array: (a) A schematic of the structure and the procedure of (b) writing and (c) reading a particular bit. The green arrow in (c) indicates the currents via the selected device, while red arrows show the leakage current [40].

Note that the memory cell of conventional (active) memories includes a transistor that provides "selection" functionality (i.e., the ability to select a given cell in the array). The density scaling of such memories is therefore, at best, limited by the scaling of the transistor.

The transistor has two critical dimensions and therefore cannot be scaled aggressively. On the other hand, there might be only one critical dimension (i.e., film thickness) for memristive devices.

1.2.3.2 Digital logic applications

The most basic and straightforward application of ReRAMs for logic circuits is probably the construction of logic gates using ReRAM cells. In initial studies, the construction of logic gates usually required more than one ReRAM cell and other essential circuit elements such as resistors and capacitors, and the function of a given gate configuration. For example, two ReRAM cells and one resistor were adopted by Terabe et al. [41] to construct both AND and OR gates, but the ReRAM cells in these two gate configurations are just opposite in orientation. To simplify gate configuration and to realise multiple functions in a single gate configuration, single ReRAM cells were subsequently introduced to implement logic operations [42]. For instance, Linn et al. [42] demonstrated that 14 of 16 Boolean logic functions can be realised within a single bipolar RS or complementary RS in at most three sequential cycles, but the other two operations (i.e., XOR and XNOR functions) are theoretically exclusive within a single bipolar RS or complementary RS. Recently, taking advantage of both positive and negative reading biases, You et al. [43] reported the realization of all 16 Boolean logic functions in a single switchable diode in three logic cycles. Although this study is indeed of great importance, switchable diode is very rare, and consequently its prospects for practical application are uncertain. Another concept called material implication (IMP), which leads to a new logic gate labeled as IMPLY, has been proposed to be developed using RS devices [31].

1.2.3.3 ReRAM-based neuromorphic approaches

The basic idea in most ReRAM-based neuromorphic approaches is to consider ReRAM devices, or small ReRAM-based circuits, as artificial synapses. The idea of using ReRAM devices for neuromorphic applications goes back to Likharev [44], who introduced the concept of "Crossnets", where ReRAM devices serve as programmable interconnects, that is, binary synapses [12]. In a more general approach, the tunable resistive state of ReRAM device is used as a synaptic weight, which can be adapted by suitable methods for changing ReRAM resistance in analogy with synaptic plasticity rules. This is schematically shown in Fig. 1.12 (a): by updating the weight of the synapses, the electrical connection between a

presynaptic neuron and a postsynaptic neuron changes, thus enabling the possibility of implementing a variety of learning models for pattern recognition and memory storage [12].

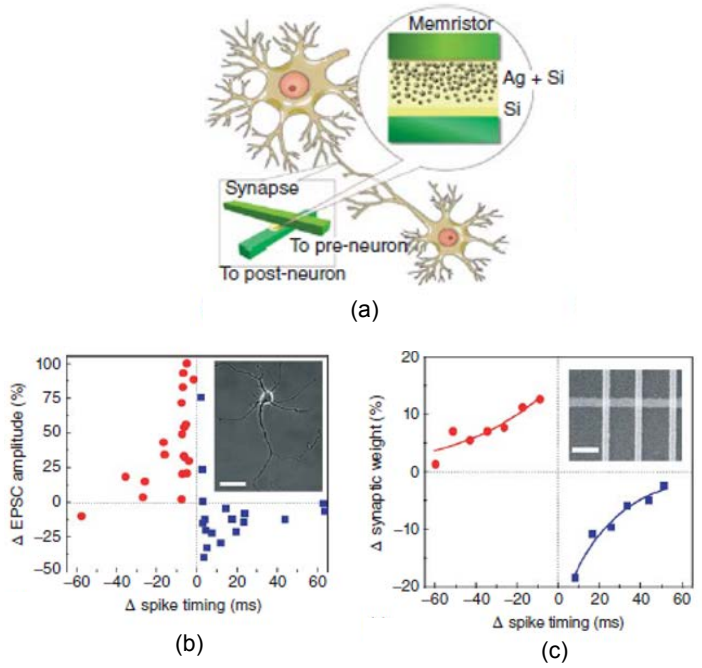

Figure 1.12: (a) Schematic description of the role of the ReRAM as a synapse between two neurons. (b) Experimental change of excitatory postsynaptic current (EPSC) of rat hippocampal neurons as a function of the relative spike timing.(c) Experimental ReRAM STDP curve. The exponential behavior is comparable to biological measurements in (b) [45].

The weight of the synapses is typically updated following the learning rule called Spike-Timing Dependent Plasticity (STDP), where the conductance change of the synapse depends on the relative timing of the electrical pulses delivered from the presynaptic neuron and the postsynaptic neuron. If the presynaptic spike precedes the postsynaptic one, the synapse conductance is enhanced, whereas if the postsynaptic spike precedes the presynaptic one, the synapse is depressed [46]. Experimental results measured from a rat-hippocampal neuron are shown in Fig. 1.12 (b) [47]. The first experimental evidence of the feasibility of the STDP learning curve with RS devices was reported by Jo et al. [48]. Figure 1.12 (c) shows the experimentally measured STDP, namely the conductance update as a function of inter spike delay. The STDP characteristic shows a conductance increase for a time delay, that is, for the presynaptic spike preceding the postsynaptic spike ($\Delta t > 0$). Conversely, when the presynaptic spike precedes the postsynaptic ($\Delta t < 0$), the ReRAM conductance

is decreased. The resulting STDP characteristic shows an exponentially decaying behavior, which is consistent with biological data in Fig. 1.12 (b) [12]. According to this idealized scheme, a single spike cannot alter the resistive state of the synapse, and a weight update requires the presence of a postsynaptic spike and a presynaptic spike overlapping in time [12].

1.3 Compact modeling of resistive switching devices

In Chapter 4 a compact model is presented for the major and minor I–V loops of bipolar RS devices, called *Memdiode*. The model was reported for the first time in the year 2015 by Enrique Miranda and is able to qualitatively and cuantitatively reproduce the experimental results for several bipolar RS devices. This sub-Section attempts to introduce the reader to this model, conceptually, explaining what is a memristive device, what it involves and describe the first model developed in this framework. Then, the reader will be ready to deal with the *Memdiode* in the Chapter 4.

1.3.1 Memristive devices

Phenomenologically, the RS phenomenon is provoked by stimulus that affects an internal state of the RS element which controls the resistance. This kind of devices are called memristive elements. The most used and important memristive device is the memristor (contraction of memory and resistor). This device was postulated in 1971 by Leon Chua as the 4th fundamental circuit element [49], which would relate charge q to magnetic flux φ and would have the distinction of being the first non-linear circuit element (where the non-linearity arises because q and φ are integrals of the circuit measurable, current, I and voltage, V). Thus, there should be four basic circuit elements (I, V, q and φ) described by the remaining relations between the variables (Fig. 1.13). The memristor, with memristance M provides a functional relation between charge and flux, $d\varphi = Mdq$. M depends on the hystory of the device and retains its value even if the power is turned off. In the case of linear elements, in which M is a constant, memristance is identical to resistance and, thus, is of no special interest. However, if M is itself a function of q, yielding a nonlinear circuit element, then the relation between q and φ for a sinusoidal input is generally a frequency-dependent Lissajous figure [50]. Unlike capacitors and inductors, memristors do not store energy and can not be constructed by combining the other devices.

Memristive devices are defined in terms of two coupled equations:

$$y(t) = g(x, u, t) \cdot u(t) \tag{1.13}$$

$$\frac{dx}{dt} = f(x, u, t) \tag{1.14}$$

where $u(t)$ is the input signal (current or voltage), $y(t)$ is the output signal (voltage or current) and x is the variable which describes the state of the device. g and f are continuous functions. These two equations identify a linear memristive system if f and g are linear [51].

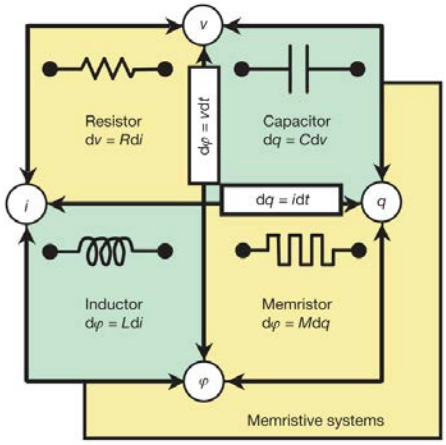

Figure 1.13: The four fundamental two-terminal circuit elements: resistor, capacitor, inductor and memristor. Resistors and memristors are subsets of a more general class of dynamical devices, memristive systems. Note that R, C, L and M can be functions of the independent variable in their defining equations, yielding nonlinear elements. For example, a charge-controlled memristor is defined by a single-valued function $M(q)$ [50].

According to Chua, all 2-terminal devices based on RS are memristors, regardless of the device material and physical operating mechanism, they all exhibit a distinctive "fingerprint" characterized by a pinched hysteresis loop in the I–V plane when driven by any bipolar periodic voltage and for any initial condition of the memristor [52]. On the other hand, both industry and academia communities look for novel applications for RS devices and need precise models that describe their behavior. Therefore, it could be said that the modeling, simulation and prediction of the behavior of memristors are fundamental pieces of the development and validation of new memristor applications. For instance, after the Nature's publication on the successful implementation of memristor in TiO_2 [50], the interest in this element skyrocketed and Strukov introduced the first model for their device.

1.3.2 Linear ion drift model

The physical model developed by Strukov et al., schematically described in Fig. 1.14 and known as Linear ion drift model, is characterized by an equivalent time-dependent resistor whose resistance is proportional to the quantity of charge q that passed through it. The model consisted of a two-layer thin film (size D $\approx$ 10 nm) of TiO_2 behaving as a semiconductor and an insulator, sandwiched between platinum contacts where the total resistance of the device is equivalent to two variable resistors connected in series (Fig. 1.14 (a)), where the resistances were given for the full-length D of the device. Specifically, the semiconductor film had a region with a high concentration of dopants (in this example assumed to be positive ions) having low resistance R_{ON} -LRS- and the remainder was an undoped region, behaving as an insulator, and therefore with much higher resistance R_{OFF} – HRS (see Fig. 1.14 (b)).

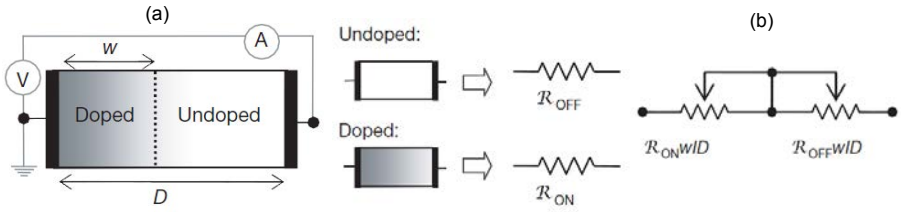

Figure 1.14: Linear ion drift model. (a) Diagram with a simplified equivalent circuit of the HP memristor model. V, voltmeter; A, amperemeter. (b) Simplified HP memristor model [50].

After applying a bias voltage across the device, the boundary between the regions moved and therefore, the state variable w changed. This is caused by the drift of charged dopants. This model assumed a linear ion drift in a uniform field [50]. According to the memristive system definition (1.13) and (1.14), the model is described, respectively, by:

$$v(t) = \left(R_{\text{ON}} \cdot \frac{w(t)}{D} + R_{\text{OFF}} \cdot \left(1 - \frac{w(t)}{D} \right) \right) \cdot i(t) \tag{1.15}$$

$$\frac{dw(t)}{dt} = \mu_V \frac{R_{\text{ON}}}{D} \cdot i(t) \tag{1.16}$$

Integrating the equation 1.16 with respect to the time t, gives the definition:

$$w(t) = \mu_V \frac{R_{\text{ON}}}{D} \cdot q(t) \tag{1.17}$$

where μ_V is the average ion mobility. Fig. 1.15 shows the applied voltage (blue) and resulting current (green) as a function of time t. The applied voltage is $v_0 \cdot sin(w_0 t)$ and the

resistance ratio is R_{OFF}/R_{ON} = 160, where v_0 is the magnitude of the applied voltage and w_0 is the frequency. In each plot the axes are dimensionless, with voltage, current, time, flux and charge expressed in units of v_0 =1 V, $i_0 = v_0/R_{ON} \sim 10$ mA, $t_0 = 2\pi/v_0$; $D^2/\mu_V v_0 = 10$ ms, $v_0 t_0$ and $i_0 t_0$, respectively. Here i_0 denotes the maximum possible current through the device, and t_0 is the shortest time required for linear drift of dopants across the full device length in a uniform field v_0/D, for example with D = 10 nm and $\mu_V = 10^{-10}$ cm^2 s^{-1}V^{-1}. We note that, for the parameters chosen, the applied bias never forces either of the two resistive regions to collapse; for example, w/D does not approach zero or one (shown with dashed lines in the middle plots in 1.15 (a)). Also, the dashed I–V plot in (b) demonstrates the hysteresis collapse observed with a tenfold increase in sweep frequency. The insets in the I–V plots in (b) show that for this example the charge is a single-valued function of the flux, as it must be in a memristor [50].

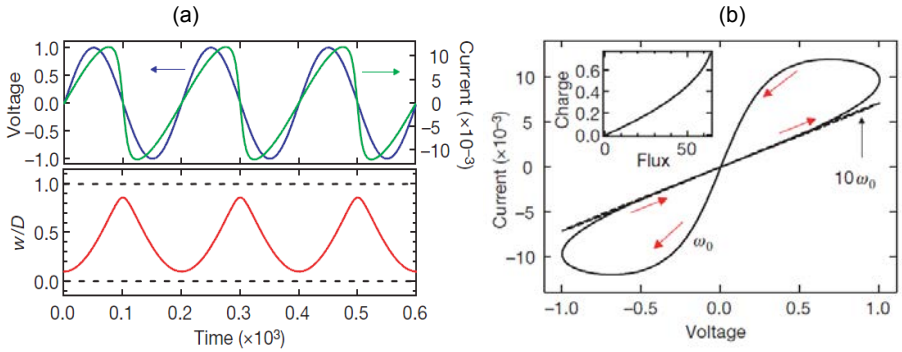

Figure 1.15: Linear ion drift model. (a) Diagram with a simplified equivalent circuit of the HP memristor model. V, voltmeter; A, amperemeter. (b) Simplified HP memristor model [50].

Small voltages applied in a nanoscale device can yield huge electric fields, which can produce significant non-linearities in ionic transport [50]. For simulation of non-linearity, when the state variable is close to the bounds (Zero and D), this model is completed with a window function. A common approach to model memristive systems is to include empirical window functions to describe the nonlinear mechanism that affect the change in the memristance and limits its range of values [53]. After Strukov published the Linear ion drift model, also several other window functions were defined, and they are named after their inventors, as for example Strukov [50], Prodromakis [54], and TEAM, or Kvatinski [55] windows. Each window function completes the state variable equation with a non-linear function, and depends on the state as well as on the direction of the current within the circuit. However, the

windows functions have not a physical justification and it can lead to serious mathematical problems. In the following years, new models that reproduced the dynamic characteristics of memristive devices were developed in SPICE environments (the traditional standard for circuit designers) employing physics-based formulations. In the case of the Linear ion drift model, it was first implemented in SPICE by Biolek. et al [56] in 2009.

Just like the model developed by Strukov, our memristive model presented in Chapter 4, relies on two equations according to the memristive system definition. As opposed to the former model, in which window functions have to be incorporated to overcome converge problems, our model considers the integrated expressions which eliminates them. Moreover, in the new version, no capacitor is needed to store the memory variable as in the past. The model is fully explained in Chapter 4.

1.4 Conclusions

In this introductory Chapter an overview about filamentary conduction on two closely related phenomena, the BD process of thin films and the reversible RS phenomenon which take place in thin oxide films, has been presented. Some techniques used to measure and analyze the BD parameters (time-to-BD and BD-voltages) have been reviewed as well as the typical degradation models (TDDB). In the case of RS, their modes and their associated physical mechanism have been reviewed. A brief introduction to the principal applications of RS devices was also addressed and some issues related to compact modeling of RS devices such as memristive devices and the first memristive model were introduced.

Chapter 2

Metal-Insulator-Semiconductor (MIS) Devices

It is well known that filamentary-type ReRAM is considered among the most promising candidates to replace current flash memory technology due to its simpler stack structure (MIS or MIM), compatibility with CMOS technology, lower power consumption, longer data retention, higher endurance, and lower fabrication cost [27, 57–59]. Nevertheless, several issues for this emerging technology still require serious consideration.

Among these issues we can mention switching variability and device reliability. These handicaps are connected with the fluctuations of the switching parameters associated with the random nature of CF formation and dissolution through percolation processes. The occurrence of these fluctuations in memory applications can cause severe operation errors [60]. Hence, for the practical application of Ni/HfO_2-based ReRAM technology, it is crucial to keep a good control of the reversible aspect of the CF. This requires a better understanding of the key mechanisms governing the device stability. In addition, another important issue that deserves to be mentioned is the occurrence of multiple sneak paths between ReRAM cells when placed in crossbar array architectures. This can lead to severe readout errors [25, 61]. To overcome this problem, an additional selector device, such as a rectifying diode or pass transistor needs to be integrated into each memory cell to suppress the crosstalk effect [62, 63]. This selector, however, significantly increases the unitary cell size and enhances the fabrication process complexity [64, 65]. An alternative solution to the implementation of a selector device consist in using a ReRAM cell with intrinsic self-rectifying

properties.

Apart from that, extensive efforts have been devoted to investigating alternative High-K dielectrics for MIS or MIM devices and for a wide range of micro/nanoelectronics applications, such as dynamic random-access memories [66], emerging nanodevices [67, 68], organic light emitting structures [69], silicon solar cells [70], and microelectromechanical systems [71]. For all these applications, it becomes necessary to have a deposition technique capable of producing high-quality films with good dielectric properties, large uniform areas and conformality, as well as an accurate control of the oxide film thickness. In that respect, Atomic Layer Deposition (ALD) has been shown to meet most of these demands [72]. Therefore, taking advantage of the ALD unique properties, it is possible to deposit alternately very thin layers of different High-K materials, i.e., ALD-grown Al_2O_3/HfO_2 nanolaminates, so that they can be used to tailor the dielectric properties of the whole stack. The interest in this kind of nanolaminates stems from the possibility of achieving a gate stack that shares the properties of both Al_2O_3 (high conduction band offset from Si, $\Phi \approx 2.8 - 3.3$ eV [73]) and HfO_2 (high permittivity oxide, $\kappa \approx 22$ [73]).

This Chapter is divided into two Sections well differentiated. The first Section is related to RS behavior of HfO_2-based MIS structures. The second Section explores the generation of multiple BD events in Al_2O_3/HfO_2 nanolaminates subjected to constant electrical stress.

2.1 HfO_2-based MIS structures

In this Section, the effect of temperature and voltage polarity on the electrical behavior of Ni/HfO_2-based RS structures will be analyzed. Besides the switching variability, attention will also be focused on the electrical and thermal stability of the CF. This part of the study is included in paper **MEE15**. Subsequently, an in-depth investigation of the LRS currents and switching properties of $Ni/HfO_2/n^+$-Si devices with HfO_2 thickness ranging from 5 to 20 nm is carried out. Special attention is given to the influence of the forming polarity and CC on the post-forming characteristics. The analysis sheds light on the microscopic nature and properties of the CF pathway and the associated electron transport mechanism, providing a deeper understanding of the switching processes behind the self-rectifying ReRAM cells. This study forms part of paper **TED17**.

2.1.1 Electrical characterization

2.1.1.1 Structures and measurement conditions

The MIS devices were fabricated at the Institut de Microelectronica de Barcelona (IMB-CNM-CSIC). A schematic representation of the device cross-section is shown in Fig. 2.1. The samples consist in Ni/HfO_2/n^+-Si structures. The structures were fabricated on (100) n-type CZ silicon wafers with resistivity between 0.007 Ω·cm and 0.013 Ω·cm following a field isolated MIS process. After a standard wafer cleaning, a wet thermal oxidation process was carried out at 1100 °C leading to a 200 nm-thick SiO_2 layer. This field oxide was patterned by photolithography and wet etching. Prior to the HfO_2 deposition, a cleaning in H_2O_2/H_2SO_4 and a dip in HF (5%) were done. Then, a HfO_2 layer with a thickness of 5 nm, 10 nm or 20 nm was grown by ALD at 225 °C using TDMAH and H_2O as precursors, and N_2 as carrier and purge gas. The 200 nm-thick Ni electrode was deposited by magnetron sputtering and patterned by a lift-off process [74]. The resulting device structures are square cells of 5x5 μm^2.

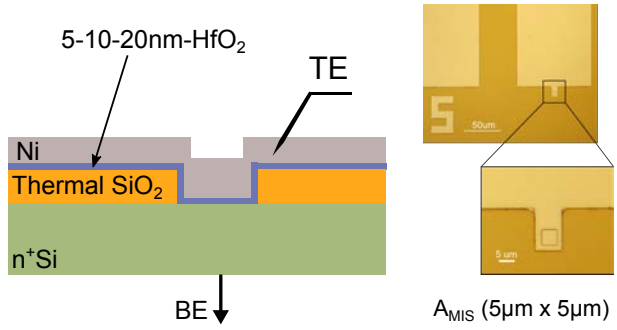

Figure 2.1: Schematic representation of the device cross-section of the studied Ni/HfO_2/n^+-Si devices and top view optical microscope image of such devices.

The RS I–V measurements were performed using a HP-4155B SPA. The voltage was applied to the top Ni electrode, while the Si substrate was grounded. During the forming step and the subsequent set processes the current was limited to avoid catastrophic irreversible damage to the device as a consequence of the high current flux. Both set and reset processes were induced by means of a voltage sweep. Note that to evaluate the cycle-to-cycle variability, a large number of cycles and measurements need to be assessed. For this purpose, a software tool was developed and implemented in Matlab to control the instrumentation via GPIB.

2.1.1.2 Resistive switching characterization

In this sub-Section, the RS phenomenon of Ni/HfO_2/n^+-Si devices is investigated for devices with an oxide thickness of 5 nm, 10 nm and 20 nm. Figure 2.2 (a)-(b) show the forming I–V and first reset process for both switching polarities, corresponding to a forming process with CC = 100 μA, and the subsequent LRS characteristics measured under the same forming polarity. As it was investigated in paper **TED17**, the forming voltage (V_F) increases with the HfO_2 thickness following a linear trend with slope $\sim$ 0.3 V/nm as illustrated in Fig. 2.3 (a). The breakdown strength is in close agreement with published results for HfO_2 [75]. Notice that in the post-forming characteristics the reset voltage and the LRS current level increase for thicker thickness (Fig. 2.2 (a)-(b)). The higher LRS currents for thicker oxide films can be explained by the higher V_F required to activate the switching property of the device. Therefore, it is surmised, that the larger dissipated power during the set process gives rise to an increased dielectric damage [76].

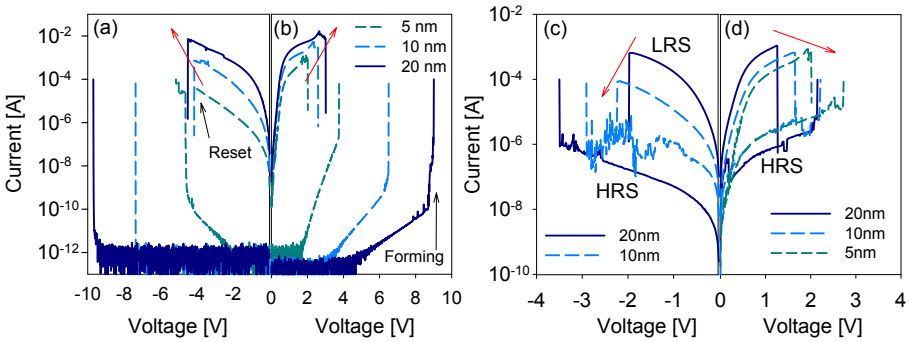

Figure 2.2: I–V characteristics corresponding to Ni/HfO_2/n^+-Si devices with three different dielectric thickness: 5 nm, 10 nm and 20 nm. The I–V curves correspond to a forming process with CC = 100 μA under (a) negative and (b) positive polarity and the subsequent LRS characteristics measured under the same polarity. Typical unipolar RS curves under (c) negative and (d) positive polarity for different HfO_2 thickness. In each case, the forming process was performed under the same polarity of the switching curves [77].

Typical unipolar RS for both polarities is illustrated in Fig. 2.2 (c)-(d). The RS exhibited by these devices corresponds to the CFs formation assisted by oxygen ion drift [78] and subsequent Ni diffusion/migration from the top metal electrode into the dielectric [78, 79]. With respect to the CFs dissolution, it can be explained by thermally enhanced diffusion of Ni atoms induced by local joule heating in the CF [80, 81]. In the studied devices, the LRS does not show linear conduction with the applied bias. This result was studied in **MEE15** and agrees with a published work [82], where the on-state current (I_{ON}) was modeled by

tunneling-based conduction considering the QPC theory for atomic-sized constrictions [37]. In these constrictions, the first quantized sub-band behaves as a potential barrier for the injected electrons [37, 82].

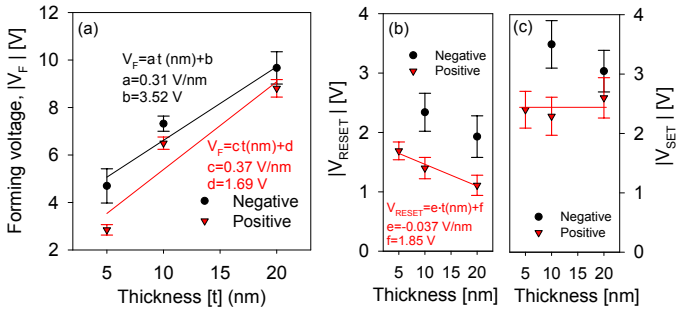

Figure 2.3: (a) V_F as a function of the HfO_2 thickness (t) under both polarities, where 10 devices for each condition were measured. (b) reset and (c) set voltages as a function of the HfO_2 thickness (t) under positive and negative unipolar switching operation. For each case, the forming was done under the same polarity as the set and reset curves. The current compliance employed during forming and set processes was CC = 100 μA. The values have been calculated from the results of 50 RS cycles in 10 different devices, where 20 cycles were firstly performed to stabilize the sample. The error bar represents the standard deviation.

It should be mentioned that for devices with 10 nm and 20 nm-thick HfO_2, the RS phenomenon was observed under different set/reset polarity combinations, indicating a non-polar switching behavior as it can be seen in Fig. 2.2 (c) and (d). Notice that high current levels are observed for both polarities [74, 83] which favors the reset process due to joule heating. On the contrary, the 5 nm-thick oxide devices only exhibit positive unipolar switching. In this case, the LRS current under negative stress polarity is not high enough to initiate a reset transition through Joule heating. Simulations results for the reset process using the macroscopic model developed in Refs. [80,82,84], which includes filamentary transport with quantum effects, indicate that the temperature reached in the CF of the 5 nm-thick oxide device is significantly lower than in the rest of the devices. Therefore, the temperature required to trigger the reset process it is not achieved for the 5 nm device formed under negative bias.

It can also be observed higher reset voltages (V_{RESET}) in the first cycle (see Fig. 2.2 (a)-(b)) than after the RS stabilization (see Fig. 2.2 (c)-(d)) where reset voltage slightly decreases with the increase of the HfO_2 thickness with a coefficient $\sim$ 0.04 V/nm (see Fig. 2.3 (b)). This dependence can be attributed to the higher LRS currents in thicker layers, which likely accelerates the thermochemical dissolution of the CF. However, as it was studied in **TED17** no clear correlation between the set voltage (V_{SET}) with the oxide thickness is detected, suggesting that after the reset process a partial dissolution of the CF at the HfO_2/n^+-Si

interface takes place (see Fig. 2.3 (c)). As a consequence, the CF would need to be locally reconstructed instead of fully rebuilt [85]. Note also that the spatial gap is independent of the oxide thickness, a fact also supported by other studies [86].

In addition, as investigated in paper **MEE15**, for both polarities abrupt resets are obtained due to thermally activated processes induced by Joule heating. Finally, it is worth mentioning that a decrease of the HfO_2 thickness leads to a reduction of the memory window between LRS and HRS [85], this reduction being more significant for negative than for positive biases as it is depicted in Fig. 2.2 (c) and (d).

2.1.1.3 Switching variability

The cycle-to-cycle variability in the studied devices is associated with the Ni diffusion and migration processes in the samples. The connection was investigated in papers **MEE15** and **TED17**. In **TED17**, different CC in the range 1 μA - 1 mA were tested. It was observed that for both switching polarities, CC values between 100 μA and 1 mA showed lower cycle-to-cycle variability than for lower CC values in the range from 1 μA to 10 μA. In addition, it was found that the cycling variability decreases for 20 nm-thick oxide films compared to 10 nm and 5 nm-based devices. Besides, lower variability was observed for the LRS than for the HRS of the devices.

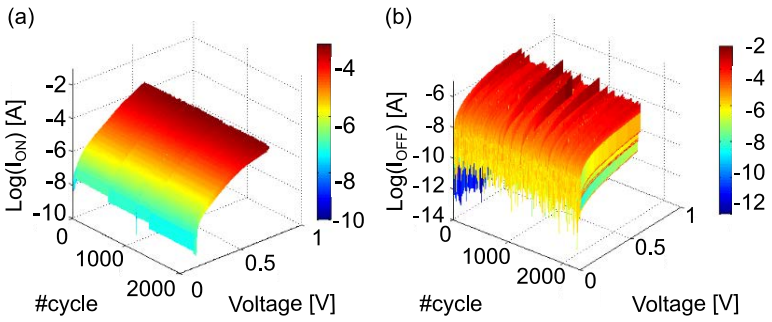

Figure 2.4: I–V (a)-(b) 3-Dimensional plots of I_{ON} and I_{OFF} versus applied voltage and cycle number corresponding to 2300 cycles of unipolar switching under positive bias with CC = 100 μA.

Figure 2.4 (a) and (b) show the evolution of I_{ON} and off-state current (I_{OFF}), respectively, as a function of the voltage and cycle number for a total of 2300 cycles of positive switching (20 nm-based devices), showing a significantly larger cycle-to-cycle variability in the HRS than in the LRS for the whole voltage range investigated. This result is likely caused by the

fact that in the HRS the partial dissolution of CFs takes place and a physical gap is opened. Then the observed enhanced variability in the HRS seems to be related to the cycle-to-cycle variations of the gap distances.

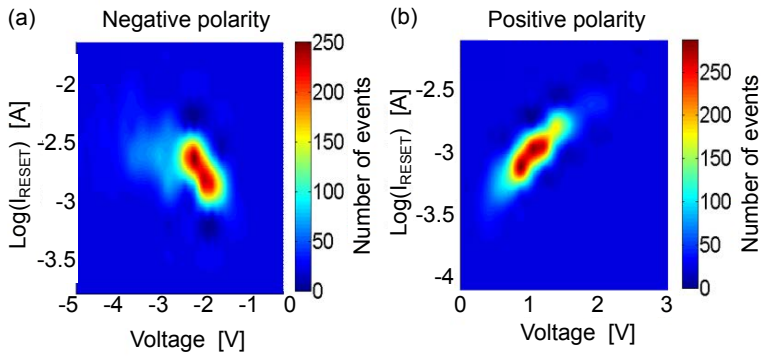

Figure 2.5: (a) I_{RESET} as a function of V_{RESET} corresponding to 2200 cycles under negative voltage ramps and (b) 2300 cycles under positive voltage ramps at T = 25 °C. The color maps indicate the number of events.

Moreover, special attention has been given to the study of the reset currents (I_{RESET}) and voltages, which impacts the metallic diffusion in the CF through local joule heating [80, 81]. As shown in Fig. 2.5 the most likely I_{RESET} vs. V_{RESET} combination for 20 nm-based devices under 2200 cycles of negative switching are located at $V_{RESET} \sim$ -1.96 V and $I_{RESET} \sim$ 1.10 mA, and in the case of positive switching, the most likely combination is $V_{RESET} \sim$ 1.13 V and $I_{RESET} \sim$ 1.20 mA. In **MEE15** was concluded that different regions of the color map linked to different reset parameters, correspond to different CFs configurations and contributions to the device resistance.

2.1.1.4 Temperature dependence of the switching properties and variability

In **MEE15**, the impact of the temperature on the stability and variability of devices was investigated. The results explained in this sub-Section are based on a 20 nm-thick layer and positive polarity. Similar results are obtained for negative polarity. Thermal measurements were carried out during switching at temperatures ranging from -40 °C to 175 °C. The measurements started at -40 °C and the temperature was raised from 25 °C to 175 °C in 25 °C steps.

Figure 2.6 (a) shows the temperature dependence of HRS and subsequent LRS for the same device during the RS cycling. It can be seen that both reset and set voltages decrease

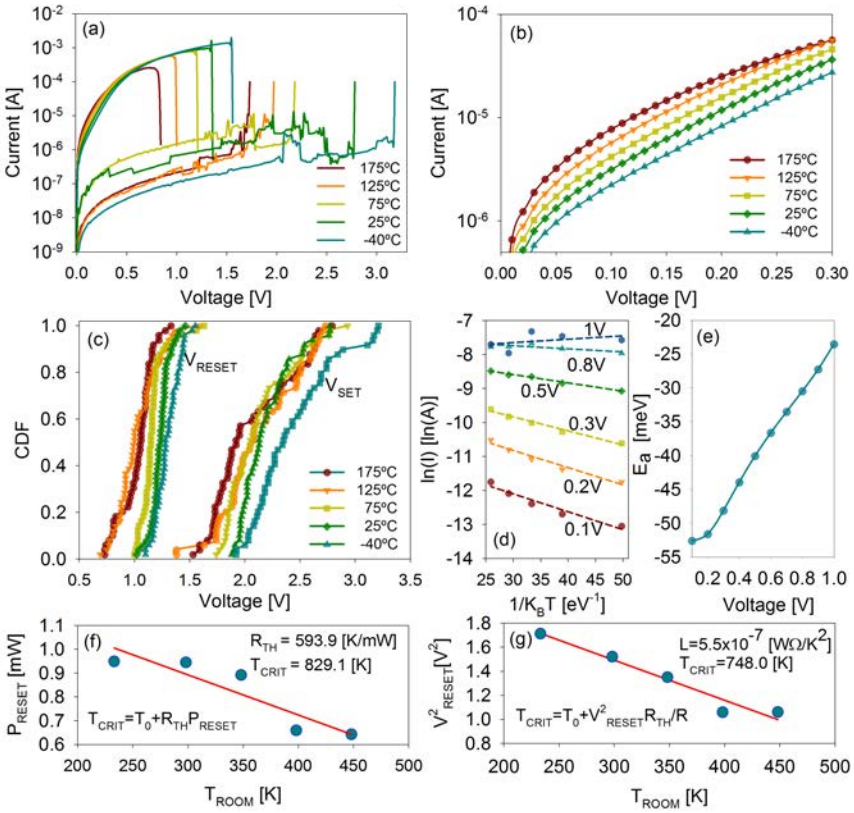

Figure 2.6: (a) Temperature dependence of HRS and subsequent LRS on RS cycling. (b) Zoom for LRS current from 0 to 0.3 V of Fig. 2.4 (a). (c) CDF for both set and reset voltages (50 cycles per temperature). (d) Arrhenius plots for currents at different bias. (e) Activation energy (E_a) at different positive bias. (f) P_{RESET} and (g) V_{RESET} square as a function of measured temperature.

when temperature increases. In addition, Fig. 2.6 (b) shows a zoomed view for LRS from 0 to 0.3 V, where a significant increase of I_{ON} with temperature is observed. Notice that the thermal dependence of the LRS current leads to a slight increase of the $I_{\mathrm{ON}}/I_{\mathrm{OFF}}$ ratio at higher temperatures. These results are in agreement with previous observations for QPC conduction [38, 87]. As expected, the increase of external temperature which increases the filamentary temperature can be translated to a potential barrier change associated to the filamentary constriction and the consequent current rise. Figure 2.6 (c) illustrates the distribution of both reset and set voltages during cycling, where a larger variability during the set process is observed for all the temperatures compared to the reset process which is influenced by the larger variability obtained for the HRS compared to the LRS (see Section 2.1.1.3). There, it was shown that the cycle-to-cycle variability is significantly enhanced

at 175 °C, while it is reduced once 25 °C is reached again. This phenomenon could be attributed to large variations in the conductivity, shape, size and length of the CFs during cycling at high temperatures. Notice that during the set process, an increase of temperature can give rise to an enhanced defect generation rate [14, 88], thus influencing the I_{ON} variability.

Temperature activation behavior is bias dependent as illustrated in Fig. 2.6 (d). Besides, consistent with previous QPC works [89], LRS current at V $<$ 0.6 V has very weak temperature dependence with almost zero activation energy. Figure 2.6 (e) illustrates how E_a decreases as the electric field increases. Moreover, in the case of negative polarity E_a is found to be temperature dependent. Figure 2.6 (f) shows that the reset power (P_{RESET}) decreases with increasing temperature. This result supports the Joule heating model for thermochemical reset, where the reset is achieved once a critical temperature is reached at one point of the CF [90]. According to this model, the critical temperature (T_{CRIT}) is related to P_{RESET}, as $T_{CRIT} = T_0 + R_{TH} \cdot P_{RESET}$, where T_0 is the ambient temperature and T_{TH} is the CF equivalent thermal resistance. Consequently, a decrease of P_{RESET} is expected when the temperature increases [91]. This decrease is attributed to the impact of the ambient temperature on the accelerated CF dissolution process. Figure 2.6 (g) shows the square of the set voltage as a function of the room temperature leading to T_{CRIT} values around 800 K.

2.1.1.5 Influence of the dielectric thickness and forming polarity on the electrical behavior

The impact of the forming polarity on the post-forming I–V characteristics was investigated in paper **TED17**. Figure 2.7 shows the post-forming LRS curves for both polarities in devices with 5 nm, 10 nm, and 20 nm HfO_2 thickness when a forming process with CC = 100 μA is performed under (a) negative polarity or Gate Injection Forming (GIF) and (b) positive polarity or Substrate Injection Forming (SIF). The voltage ramps were stopped at $\pm$1 V in order not to damage or alter the CF morphology.

In the GIF case (Fig. 2.7 (a)), it is observed that the current is symmetric with respect to the applied bias polarity and that it increases with the dielectric thickness. This current increase is related to the higher dielectric degradation induced by the required higher forming voltages, being more favorable the thermal diffusion of Ni into the dielectric in both forming polarities. However, in the SIF case (Fig. 2.7 (b)), a self-rectifying behavior is clearly observed with the reverse current being partially reduced by more than 2 orders of magnitude at $\pm$0.5 V. This fact suggests the formation of a Schottky barrier between a Ni-based CF and the semiconductor, generating an intrinsic diode with the n^+-Si.

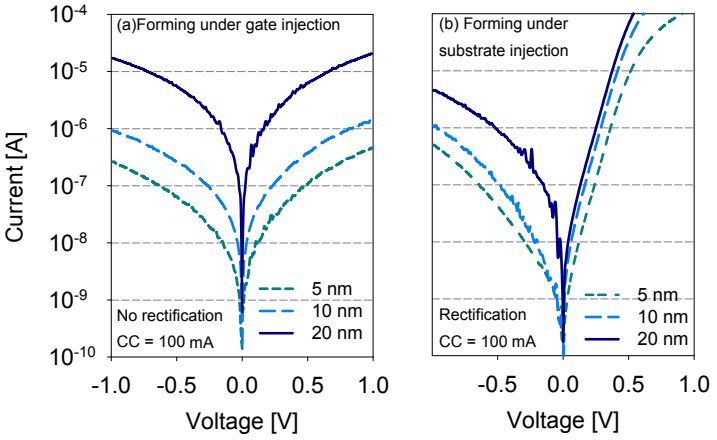

Figure 2.7: I–V curves obtained after (a) negative forming (GIF) and (b) positive forming (SIF) for devices with 5 nm, 10 nm and 20 nm HfO_2 thickness.

This current asymmetry is more pronounced for the 5 nm-thick case. The different behavior observed in Figs. 2.7 (a) and (b) points out the impact of the forming polarity on the CF electron transmission properties. In this regard, the conduction characteristics after GIF can be understood by the QPC filamentary conduction model [37], while the curves after SIF require an additional rectifying element. This latest behavior seems to indicate the formation of a Schottky-like barrier between the metallic CF and the semiconductor electrode [92–94]. It is known that the presence of Ni in the dielectric can lead to Ni-based CFs and that they can be affected by the metal cation migration driven by the electric field and temperature enhanced metal diffusion [79, 95–97]. Moreover ,recently, the impact of the forming polarity on the Ni electromigration process in TiN/HfO_2/Ni-silicide structures has been reported [98]. Here, larger Ni concentration in the dielectric was observed after a forming process with negative biased TiN electrodes than for positively biased, suggesting the impact of cation migration on the Ni-based CF formation [79, 95–97]. Similarly, for Cu electrodes, metal cation migration has also been detected leading to Cu-based CFs [97, 99]. Notice that the I–V characteristics of Cu-based ReRAM devices can exhibit a self-rectifying behavior as well [93, 94].

Figure 2.8 shows a schematic representation of the CF formation in the studied Ni/HfO_2(5 nm)/n^+-Si devices under GIF and SIF processes with CC = 100 μA. In both cases, oxygen atoms are expected to be displaced by the electric field generating oxygen vacancy rich paths [78]. However, in the case of SIF, Ni metallization of the percolation path is more favorable than in GIF due to cation migration [79, 95–97]. In this latest case, a self-rectifying

behavior is detected (see Fig. 2.7 (b)), suggesting the formation of Ni-based CFs. This is consistent with previously published work on TiN/TaN/HfO_2-based MOSFETs [100], in which it was shown that Ta/Ta^+ metal filament formation of the breakdown path only takes place under substrate injection stress [100].

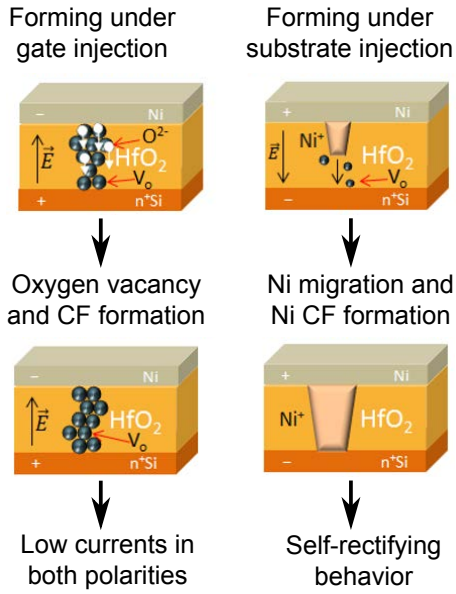

Figure 2.8: Schematic representation of the sequence of CF formation for the studied Ni/5 nm-HfO_2/n^+-Si under (left) gate injection and (right) substrate injection forming processes with CC = 100 μA.

2.1.2 Identification of the conduction mechanism

2.1.2.1 Schottky-diode behavior

The study of the temperature dependence of the I–V characteristics in the LRS is a useful technique to evaluate the dominant conduction mechanism in this regime and allows to get further insight into the nature/size of the CF and the properties of the self-rectifying behavior. In **TED17** the analysis focused on the 5 nm HfO_2-based devices, since this case showed the biggest differences in the LRS characteristics after GIF and SIF. Figure 2.9 shows the impact of temperature on the post-forming I–V characteristics after (a) GIF and (b) SIF. At the end of the experiment, the temperature was decreased again to 25 °C with the purpose of evaluating the impact of the electrical stress and ambient temperature on the CF morphology.

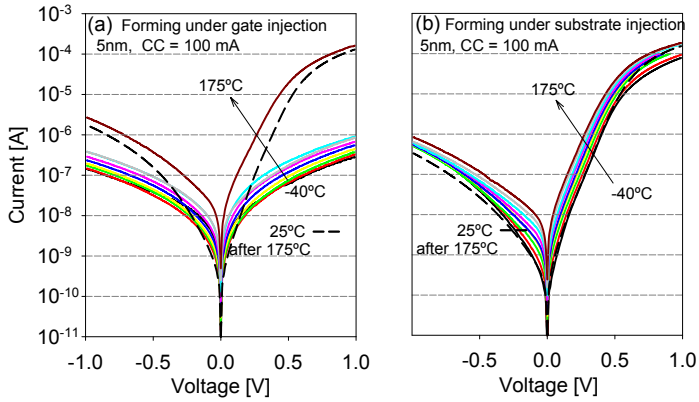

Figure 2.9: Temperature dependence for I–V curves obtained after (a) negative forming (GIF) and (b) positive forming (SIF) for two different devices with 5 nm-thick HfO_2. The different curves have been measured with the sequence: -40 °C, -10 °C, 25 °C, 50 °C, 75 °C, 100 °C, 125 °C, 150 °C, 175 °C and 25 °C again (dotted line) [101].

The experimental results show that for both injection polarities the LRS current increases with temperature. In the case of GIF (Fig. 2.9 (a)), the current increases in a temperature range up to 150 °C supporting the contribution of the QPC conduction for atomic-sized constrictions [37, 87]. This result is in agreement with the behavior observed in Ni/(20 nm)-HfO_2/n^+-Si devices under GIF (see Section 2.1.1.4). However, in the case of SIF it is worth emphasizing that the almost symmetric conduction with respect to the applied bias after GIF is not observed when the temperature is raised to 175 °C. At this temperature, very similar self-rectifying I–V characteristics like those obtained under SIF are observed. After setting the device at 175 °C, the temperature was reduced again, and the self-rectifying behavior did not disappear indicating that a chemical or morphological change of the CF occurred at this temperature. This change indicates the thermal inducement of the self-rectifying mechanism, which can be explained by the impact of temperature on Ni migration/diffusion within the dielectric film [95]. In the case of GIF, the CF is formed by oxygen vacancies and Ni atoms (see Section 2.1.1.5). The movement of Ni ions is due to diffusion in the dielectric, from the region close to the Ni electrode toward the bottom electrode [78, 102–104]. Since the diffusion process is thermally controlled, a higher concentration of Ni ions in the CF is expected in a region closer to the silicon electrode. Consequently, a Schottky barrier could be formed at the interface between the CF and the bottom electrode at the highest temperatures. A dynamical simulation for the CF generation was performed by the team from UGR. Qualitative results that help to understand the formation of a CF by means of Ni ions diffusion in a null electric field are shown in Ref. [105]. This work points out that

the diffusion process is more efficient at higher temperature and supports the presence of the self-rectifying behavior observed at 175 °C in GIF. For the SIF case a schematic energy diagram of the Schottky barrier between the CF and the substrate is illustrated in Fig. 2.10 (a).

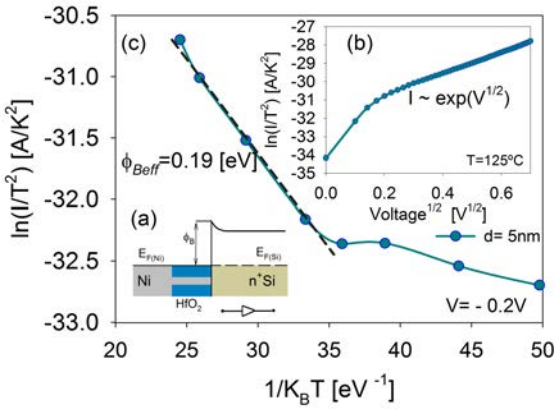

Figure 2.10: (a) Schematic of the energy diagram of the Schottky barrier between the Ni-based CF and the n^+-Si substrate for Ni/5 nm-HfO_2/n^+-Si devices after SIF with CC = 100 μA. (b) Temperature dependence of reverse current at -0.2 V. (c) Reverse current of LRS characterized by the Schottky emission model.

Notice that under SIF, the current increases with the temperature and decreases when the temperature is reduced again (dotted line), indicating no significant changes of the CF nature/size during the experiment. The I–V characteristic for the Schottky emission mechanism is given by [106]:

$$I = S \cdot A^* \cdot T^2 \cdot exp\left[\frac{-q \cdot \phi_{\text{Beff}}}{k_B T}\right] \tag{2.1}$$

$$A^* = \frac{4\pi q k_B^2 m^*}{h^3} = \frac{120 m^*}{m_0} \tag{2.2}$$

$$\phi_{\text{Beff}} = \phi_B - \sqrt{qE/4\pi\epsilon_r\epsilon_0} \tag{2.3}$$

where I is the current, S the area, A^* the effective Richardson constant, T the absolute temperature, q the electron charge, ϕ_{Beff} the effective Schottky barrier height, k_B the Boltzmann constant, m^* the effective electron mass in the dielectric, m_0 the free electron mass, h the Planck's constant, ϕ_B the potential barrier height, E the electric field, ϵ_0 the vacuum permittivity, and ϵ_r the optical dielectric constant. From Eq. 2.1, the plot $ln(I/T^2)$ vs. $V^{1/2}$ should be linear. Figure 2.10 (b) shows that the experimental data obtained above 0.2 V at

high temperatures support the Schottky emission model. Furthermore, ϕ_{Beff}, a parameter strongly related to the self-rectifying effect, can be estimated from the slope of the $ln(I/T^2)$ vs. $1/k_BT$ curve at fixed bias. ϕ_{Beff} ~0.19 eV was obtained at -0.2 V in the temperature range [50 °C, 200 °C] (see Fig. 2.10 (c))).

2.1.2.2 Influence of the current compliance on the self-rectifying ratio

Since the current compliance [103, 104] significantly affects the size and composition of the CFs, it is worth investigating the effects of CC on the device self-rectifying characteristics. To evaluate the influence of the CC on the LRS current, since CC controls the CF strength (size and shape), different CC in the range 100 μA -10 mA were tested. The distinctive behavior observed among devices subjected to GIF (Fig. 2.11 (a)) and SIF (Fig. 2.11 (b)) indicates that the degradation process is different for both injection polarities.

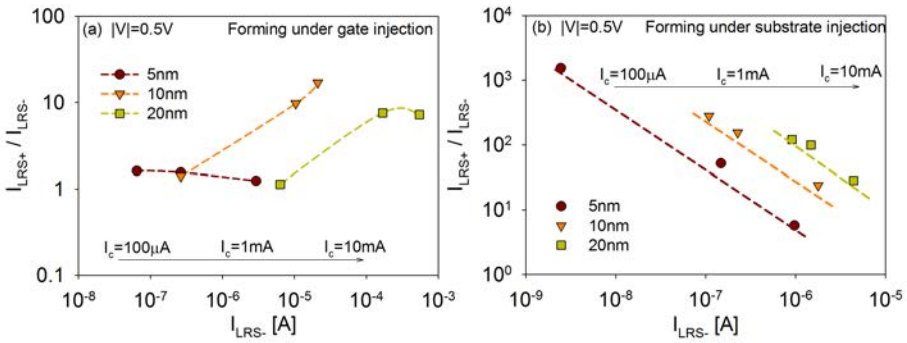

Figure 2.11: Ratio between the positive ($I_{\text{LRS+}}$) and negative ($I_{\text{LRS-}}$) current vs. $I_{\text{LRS-}}$ obtained at $|\ V_{\text{read}}\ |$ = 0.5 V after a forming process with CC = 100 μA, CC = 1 mA and CC = 10 mA under (a) gate injection and (b) substrate injection for devices with 5 nm, 10 nm and 20 nm HfO_2. The values have been extracted from the post-forming I–V characteristics of pristine devices, where two devices were measured at each condition, being the average value represented in the plots.

In the GIF case (Fig. 2.11 (a)), the LRS characteristics do not show rectification, except for CC values higher than 1 mA and HfO_2 layers thicker than 10 nm. Under this circumstance, larger thermal migration of Ni into the dielectric is expected [103, 104]. However, in the SIF case (Fig. 2.11 (b)) higher ratios than those obtained under GIF are observed for all the considered conditions. The largest ratio ($> 10^3$@$\pm$0.5 V) was obtained for 5 nm-thick HfO_2 devices after a SIF process with CC $\leq$ 500 μA. Furthermore, Fig. 2.11 (b) shows that $I_{\text{LRS+}}/I_{\text{LRS-}}$ decreases for thicker dielectric layers and/or larger CC, or in other words, when longer metal filaments and higher currents are present in the dielectric. This fact can be

explained in terms of the resulting physical damage at the CF/semiconductor interface [104], leading to a negligible impact of the Schottky barrier [107].

2.1.3 Conclusions

In this sub-Section several conclusions can be drawn:

- The polarity-dependent switching behavior and the thermal stability of Ni/20 nm-HfO_2/n^+-Si devices have been analyzed.
    - A clear increase of I_{ON} with temperature was observed for both switching polarities, supporting the model of a filamentary path with a narrow constriction.
    - In the case of the HRS, for all the temperatures assessed, large data dispersion was obtained related to cycle-to-cycle variations of the physical gap distances.
    - In addition, it was observed that measuring the device at high temperatures significantly enhances the variability in the LRS, providing an additional support to the joule heating model for thermochemical reset in Ni/HfO_2-based ReRAM devices.
- The self-rectifying effect was also investigated in Ni/HfO_2/Si devices with three different thicknesses, 5 nm, 10 nm and 20 nm. The obtained results showed that the forming conditions (compliance and polarity) as well as the HfO_2 thickness have a marked impact on the LRS currents and their self-rectifying behavior.
    - In the 20 nm-thick oxide case, for both forming polarities, higher post-forming currents were observed than for thinner layers. These higher currents lead to a faster reset process through Joule heating.
    - Data analysis revealed an increased self-rectifying ratio for devices subjected to a substrate injection forming process, suggesting the favored formation of metallic filaments. This observation could be explained by the Ni cation migration driven by the electric field and temperature enhanced Ni diffusion.
    - Conduction measurements performed as a function of the temperature in 5 nm-thick oxide devices indicated that, under negative forming (GIF) symmetric conduction is observed until the temperature is raised to 175 °C, then very similar self-rectifying I–V characteristics like those obtained under positive forming (SIF) are observed. The results indicate that depending on the forming polarity, the electron transport mechanism changed from tunneling through a narrow

constriction under gate injection forming, to Schottky emission under substrate injection forming owing to the presence of a barrier between the Ni-based CF and the n^+-Si.

- Finally, the roles played by the CC and dielectric thickness on the self-rectifying properties were discussed.

2.2 MIS structure with HfO_2/Al_2O_3-based nanolaminates

In this Section of the Chapter, we are going to explore the generation of multiple failure events in atomic layer deposited HfO_2/Al_2O_3 nanolaminates subjected to constant electrical stress. The stepwise behavior exhibited by the Current – Time (I–t) characteristic of such High-K nanolaminates is a direct consequence of the successive opening of localized leakage current pathways across the dielectric film. The BD events arise from the progressive accumulation of defects within the nanolaminate and the formation of filamentary paths for the electron transport. The triggering of these events was analyzed in the past using order statistics [108] but it was limited to a few number of events per device (up to ten). In order to shed light on this issue the breakdown dynamics involved in this phenomenon is revisited. First, a BD time statistics study will be carried out showing that the arrival rate of the failure events during CVS is consistent with a NHPP as is reflected in paper **MEE15B**. Afterwards, we will focus on the role played by the initial current magnitude on the current evolution and the fundamental change in the resistance exhibited by the device. This will allow us to develop a method to obtain the failure times. Next a simple circuit model consisting in array of parallel and series resistances to account for the I–t characteristics of these devices is described. This study forms part of paper **MER15**. In addition, a second model is proposed in order to determine the stress time required to set the device to a given current level. This part is based in article **JVS17**. This is of primarily importance for the programming operation of multilevel One-Time-Programmable (OTP) memory devices based on the creation of multiple uncorrelated BD paths.

2.2.1 Electrical characterization

2.2.1.1 Structures and measurement conditions

The nanolaminated devices were fabricated at the Institut de Microelectrònica de Barcelona (IMB-CNM-CSIC). These devices are MIS capacitors with a 5-layer nanolaminated insula-

tor (Al_2O_3 /HfO_2/Al_2O_3/HfO_2/Al_2O_3) deposited by ALD onto a p-type Si substrate (0.1 – 1.4 Ωcm). A field oxide of 400 nm was grown by thermal oxidation at 1100 °C and windows were opened for the Al_2O_3/HfO_2 stack by photolithography and wet etching. Before deposition, the samples were first cleaned for 10 minutes with H_2O_2/H_2SO_4 and subsequently for 10 seconds with HF. The ALD process was performed in 100 cycles (20 alternated cycles of each material) at a constant temperature of 225 °C, using trimethylaluminium (TMA) and water (H_2O) as precursors for the Al_2O_3 deposition, and tetrakis dimethylamido-hafnium (TDMAH) and water (H_2O) for the HfO_2 deposition. After removal of the oxide from the back side, both wafer sides were metalized with Al - 0.5% Cu and the front side patterned to get capacitors in the active areas and contact pads on the field oxide. In the TEM image shows in Fig. 2.12 (a), no SiO_2 layer at the silicon interface is observed, as expected, since the ALD process was made immediately after native oxide removal [109], however, as it will be seen later the results point out that exists a very thin SiO_x residual layer.

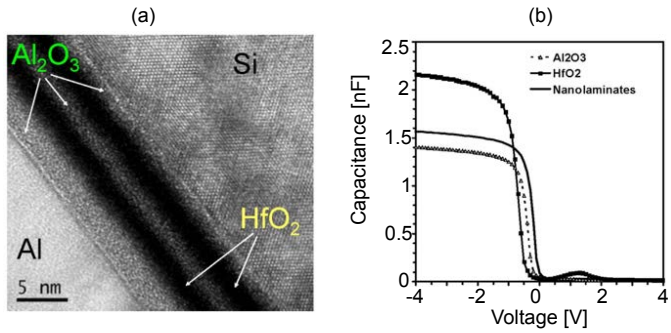

Figure 2.12: (a) High-resolution cross-sectional TEM image of the Al_2O_3-HfO_2-based nanolaminate on the p-type silicon substrate, capped with an aluminum layer. (b) Capacitance – Voltage (C–V) characteristics at 100 kHz of the three types of MOS capacitors (Al_2O_3, HfO_2, and Al_2O_3-HfO_2-based nanolaminate show in Fig. 2.12 (a)). Capacitor area is $2.3{\cdot}10^{-3}$ cm^2 [109].

An example of the typical C–V characteristics obtained, resulting from three types of materials, is shown in Fig. 2.12 (b). The measured C–V curves are useful to calculate the equivalent oxide thickness of deposited dielectric layers from the maximum value of the capacitance in accumulation resulting in an oxide thickness of about 9 nm [109]. A complete study of the fabricated devices from a materials perspective can be found in [109, 110]. The areas of the devices investigated in this Section are: $9.6{\cdot}10^{-3}$, $2.3{\cdot}10^{-3}$, $3.2{\cdot}10^{-4}$, $1.4{\cdot}10^{-4}$, and $6.4{\cdot}10^{-5}$ cm^2.

Typical electrical conduction through the dielectric layers is shown in Fig. 2.13. The experimental results were obtained from MIS structures with an area of $6.4{\cdot}10^{-5}$ cm^2 in [109]. Comparison of the conduction behavior of the different dielectrics shows some general

trends: HfO_2 layers exhibit higher leakage current than Al_2O_3 or nanolaminates. When comparing Al_2O_3 with the nanolaminate, two regions are distinguished: for low voltages, lower leakage is obtained for Al_2O_3 than for the nanolaminate, and the contrary occurs for large voltages. As for the predominant conduction mechanism, it depends on the gate voltage region, going from tunneling at low voltages to Poole–Frenkel emission for high voltages [111].

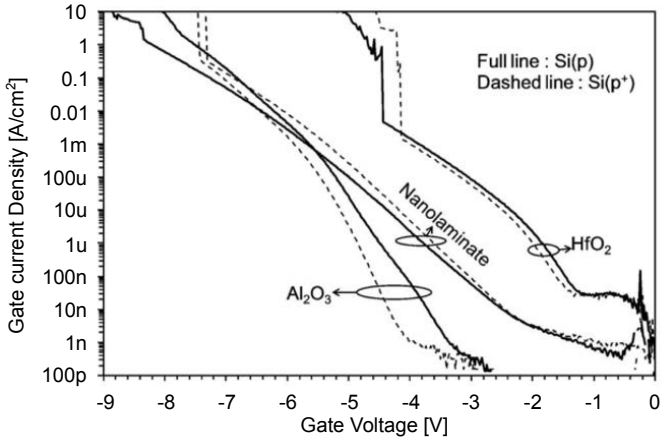

Figure 2.13: Typical C–V characteristics of Al_2O_3, HfO_2, and nanolaminate dielectrics for MIS structures for injection from the gate electrode (p-type silicon substrate) [109].

The measurements performed in this work were carried out using a HP-4155B SPA. The devices were measured biasing the samples in accumulation, i.e., applying constant negative voltages to the metal gate with respect to the p-type substrate. Then, the fresh devices were subjected to CVS with the substrate terminal grounded. For practical reasons, the range of stress voltages that can be evaluated is very limited: -6.75, -7.0 and -7.25 V. While for the lowest voltages the degradation process is too low, for the highest voltages the generation rate of failure sites is extremely fast.

2.2.1.2 Breakdown dynamics

The devices exhibit stepwise I–t characteristics which indicate the formation of multiple leakage current paths spanning the insulating film. Typical I–t characteristics with multiple BD steps are shown in Fig. 2.14 (a). Some devices occasionally exhibit large jumps associated with catastrophic events but in general the jumps are small and countable. For comparison purposes, we considered only devices that exhibit small jumps. The devices

with an area of $9.6{\cdot}10^{-3}$ cm^2 were stressed at -7 V applied to the top electrode. The initial current magnitude is approximately larger than 10 μA with a first current jump of about 1 mA in the first 50 s (see Fig. 2.14 (b)). The time-to-first BD event is Weibull-distributed after screening the data in terms of the initial leakage current [108]. To obtain qualitative results, devices with initial current higher than 9 μA are considered in this study.

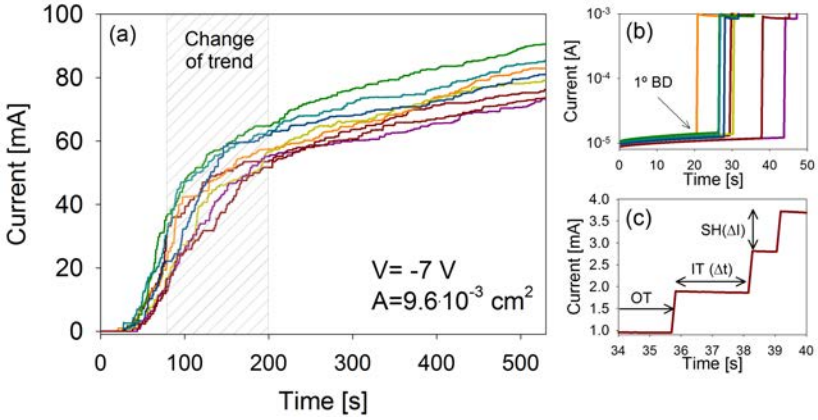

Figure 2.14: (a) I–t characteristics corresponding to several devices. (b) First BD event where it is possible to distinguish the variation of the initial leakage current magnitude. The time-to-first BD increases for smaller leakage currents. (c) Details of the leakage current paths formation of one sample and definition of the magnitudes of interest: occurrence time (Occurrence Time (OT)), interarrival time (Interarrival Time (IT)) and step height (Step Height (SH)).

After this initial step, several BD events can be observed until a total leakage current of about 80-100 mA is reached. As it can be seen, a large number of successive BDs are registered in a time span of 540 s (see Fig. 2.14 (a)). Remarkably, the height of the steps decreases as the degradation proceeds, which indicates that the history of the device is relevant for the description of the current behavior. It is also worth noting that the initial leakage current magnitude severely affects the first time-to-BD: the highest currents are associated with the shortest BD times. This issue was extensively investigated in [108] and was attributed to the presence of more or less defective cells. A remarkable point in Fig. 2.14 (a) is the change of trend of the I–t curves that takes place around 100-200 s in all the devices considered in this study. The modification of the slopes of the curves indicates that some fundamental change in the degradation process occurs during this intermediate phase of degradation. This fact will be discussed below. Along this sub-Chapter some acronyms will be used. The OT (measured from the outset of degradation), IT, and SH are indicated in Fig. 2.14 (c).

The roles played by the stress voltage and the device area are illustrated in Fig. 2.15 (a)

and (b), respectively. Here, I–t measurements for devices with identical areas and different stress voltages (see Fig. 2.15 (a)) and for devices with different areas and identical stress voltages (see Fig. 2.15 (b)) are reported. The measurements reveal that the arrival rate of the failure events increases with the device area and with the magnitude of the stress voltage. The overall behavior is consistent with the area scaling property of Poisson statistics and with the voltage acceleration factor associated with the electrical degradation of MIS devices [112].

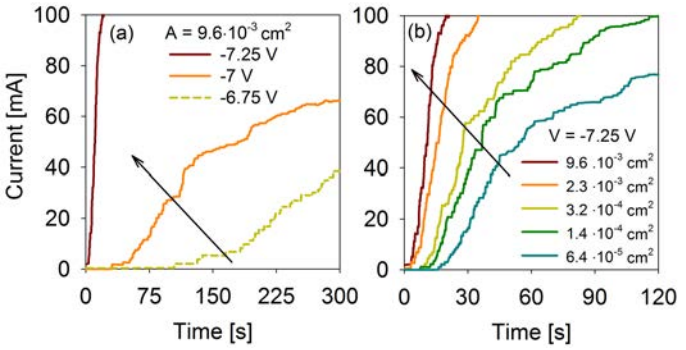

Figure 2.15: (a) Evolution of the current for (a) different applied voltages and (b) different device areas.

2.2.2 Breakdown time statistics

In order to characterize the BD dynamics phenomenon and to model the device behavior we focused on the arrival time of failure events. The studies included in paper **MEE15B** reveal a positive correlation between IT and OT which indicates that the BD events are not identically distributed in time as the degradation proceeds. This observation is confirmed since ITs exhibit underdispersion with respect to the memoryless exponential probability distribution function. This indicates that a HPP can be ruled out for the investigated process [113]. In other words, the failure events are not homogeneously distributed along time. In order to get an expression for the time-dependent generation rate of defects, the OT frequency distribution was fitted using a double power-law model, which is a standard approach in failure analysis [114]. The proposed intensity function reads:

$$\lambda(t) = \left(\frac{t - t_0}{\theta_1}\right)^{\beta_1} - \left(\frac{t - t_0}{\theta_2}\right)^{\beta_2} \tag{2.4}$$

which corresponds to a double power-law model with characteristic times θ_1 and θ_2, and exponents β_1 and β_2. Taking t_0 = 10 s as the dead time during which the oxide degradation

takes place without any failure occurrence, θ_1 = 224.23 s, β_1 = -1.30, θ_2 = 190.82 s, and β_2 = -1.41 provide the best fitting results to our data. Notice that, taking into account the superposition principle of uncorrelated NHPPs, 2.4 was normalized to the number of processes (N = 34) with a bin size of 10 s (see Fig. 2.16 (a)). The model parameters were found using a nonlinear least-squares method for the family of curves defined by Eq. 2.4.

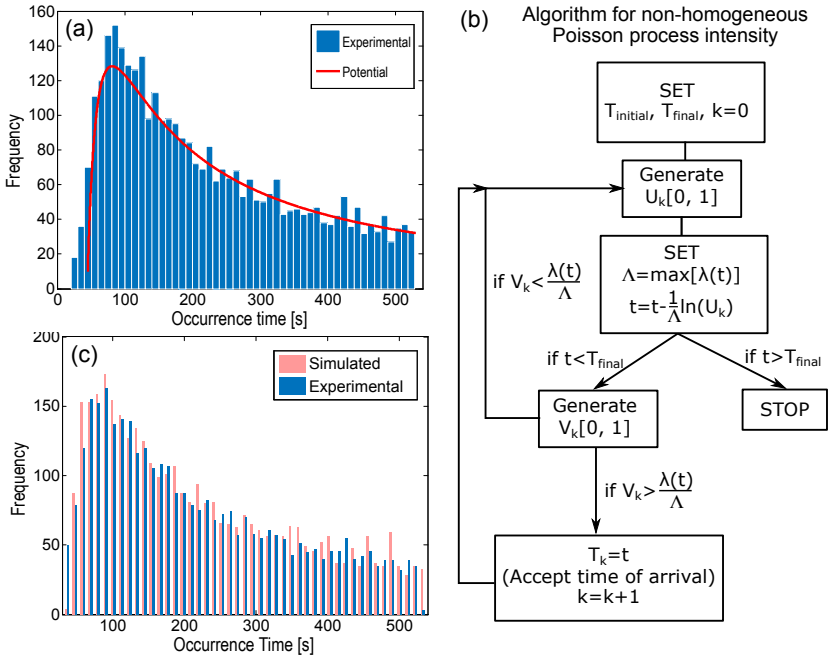

Figure 2.16: (a) Frequency plot for the occurrence times (OT) and global fitting model (bin size of 10 s). (b) Thinning algorithm used for calculating the arrival time of the failure events according to the NHPP given by Eq. 2.4. (c) Histogram for the experimental and simulation results using the thinning algorithm described in (b) [115].

The overall behavior described by Eq. 2.4 is the result of two effects: in the short time scale there is an apparent increment of the failure rate caused by the spread of the time-to-first BD, however, in the long run, a decrease of the failure rate is clearly observed (see Fig. 2.16 (a)). This second effect can be ascribed to the reduction of the oxide voltage originated by the opening of multiple leakage current paths. In other words, as a consequence of the current increase, part of the applied voltage drops across the series resistance of the device. This can explain the reduction of the process intensity (defined as the number of failure events per unit of time) with the degradation time. In paper **MEE15B** it was shown that SH also levels off around an equivalent resistance value of 18 kΩ per filament created.

In order to generate a sequence of arrival times consistent with the NHPP defined by Eq. 2.4, the so-called thinning method was considered [116]. The method is applicable for any given rate function $\lambda(t)$ and is based on the controlled elimination of events of an HPP whose rate function dominates $\lambda(t)$. In particular, $\Lambda = max[\lambda(t)]$ can be used as the thinning function. The algorithm is schematically described in Fig. 2.16 (b). U and V are uniform distributions in the range [0,1]. The distribution of the generated failure times (scaled to the number of devices and bin size) is illustrated in Fig. 2.16 (c). Notice the good agreement between the experimental and simulated data.

2.2.3 Modeling of multi-filamentary conduction

2.2.3.1 Modeling of the initial phase of degradation

In this Section, the attention will be exclusively focused on the current jumps associated with the generation of the filaments in the short time scale where there is an apparent increment of the failure rate caused by the spread of the time-to-first BD. In order to check the accuracy of the proposed model, the failure times were assumed known since only the current jumps are modeled. As mentioned before, the well-defined stepwise I–t characteristics are typical of a system with sequentially triggered parallel leakage current paths. Therefore, the resulting BD dynamics can be simulated assuming multifilamentary conduction. To demonstrate the validity of such approach an equivalent circuit model for the I–t curves consisting in an array of series and parallel resistances was proposed as illustrated in Fig. 2.17 (a). The I–V characteristic can be simply expressed as:

$$I = \left[R_S + \left(\frac{n}{R} + \frac{1}{R_P} \right)^{-1} \right]^{-1} \cdot V \tag{2.5}$$

where R_S and R_P are the series and parallel resistances, respectively. R is the resistance associated with the appearance of the leakage current path n ≥ 1. R_P represents the leakage current flowing through the device before the first BD event. As shown in Fig. 2.17 (b) and (c), Eq. 2.5 can reproduce the evolution of the current steps ΔI as the degradation proceeds. Fig. 2.17 (b) and (c) show typical I–t characteristics that correspond to devices with area $9.6{\cdot}10^{-3}$ cm^2 (CVS @ -6.75 V) and area $2.3{\cdot}10^{-3}$ cm^2 (CVS @ -7 V), respectively. At the end, the magnitude of the steps in combination with the failure times determine the overall shape of the I–t characteristics.

In paper **MER15**, a model which can be used to determine the stress time required to

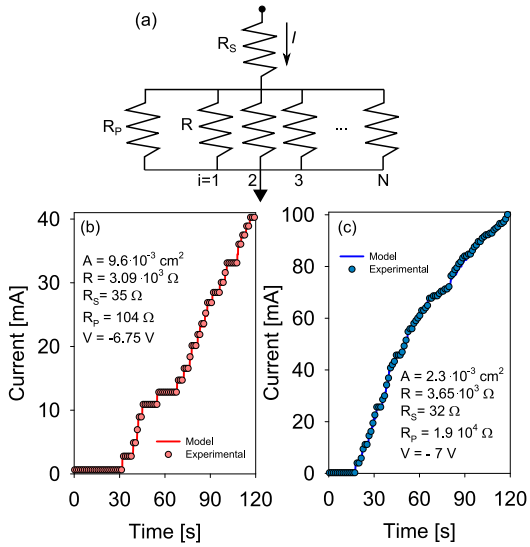

Figure 2.17: (a) Equivalent circuit model with sequentially formed BD paths. R_S and R_P are series and parallel resistance, respectively. R is the resistance of a single filament. Typical I–t characteristics and model results. (b) Device area A = $9.6{\cdot}10^{-3}$ cm^2 and stress voltage V = -6.75 V. (c) Device area A = $2.3{\cdot}10^{-5}$ cm^2 and stress voltage V = -7 V [117].

set the device to a given current level was proposed. First it is assumed that the filaments are generated at a constant rate in the time range investigated ($<$ 130 s). The time span investigated is 130 s because for longer times the failure events exhibit correlation effects. According to this observation, we can express the number of filaments n at time t as:

$$n(t) \approx \alpha(t - t_0) \tag{2.6}$$

where α is the arrival rate of the failure events and t_0 the dead time in which no event is detected. As expected, experimental data reveal that α increases with the area of the device and with the magnitude of the stress voltage (see Fig. 2.15). The model parameters R_S and R can be obtained from Eq. 2.5, neglecting R_P, from the transformed expression:

$$\frac{V}{I_n} \approx R_S + \frac{R}{n} \tag{2.7}$$

where I_n is the current measured immediately after the occurrence of the *n*th event. Note that R (the single filament resistance) is in the range of several kΩ, R_S is two orders of magnitude lower. As expected, R_S determines the long-run behavior (Fig. 2.18 (a)) and R the initial slope of the curves (Fig. 2.18 (b)).

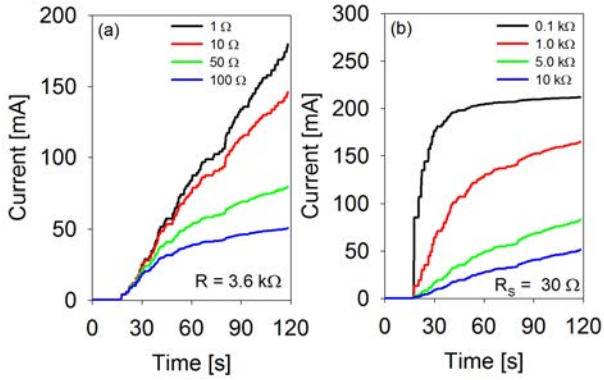

Figure 2.18: Effect of the model parameters a) R_S and b) single filament R on the simulated curves using Eq. 2.5.

Taking into account the BD dynamics expressed by Eqs. 2.5 and 2.6, it is possible to extrapolate the device behavior to the continuous degradation case, i.e. smaller jumps at a proportionally larger failure rate. As the result of this exercise, we can write:

$$I(t) \approx \left[R_S + \alpha^{-1} R (t - t_0)^{-1}\right]^{-1} \cdot V \tag{2.8}$$

which is represented by the solid lines in Figs. 2.19 (a) and (b). Now, Eq. 2.7 can be used to assess the programming time t_P necessary to reach a given current level I_P:

$$t_P(I_P) \approx \alpha^{-1} R I_P (V - R_S) I_P)^{-1} + t_0 \tag{2.9}$$

which, equivalently, corresponds to a number of steps given by:

$$n_P(t_P) \approx R I_P (V - R_S) I_P)^{-1} \tag{2.10}$$

Expressions 2.9 and 2.10 are plotted in Fig. 2.20 for the two samples investigated. Notice that the number of steps is almost identical in both cases, which gives further support to the proposed BD picture. The model can be used to determine the stress time required to set the device to a given current level. This is of primarily importance for the programming operation of multilevel non-volatile memory devices, or OTP memories, based on the creation of multiple uncorrelated breakdown paths.

In paper **MER15**, we concluded that one important feature of the proposed model, which is surprising at first glance, is that the voltage drop across the array of parallel resistances $V - I \cdot R_S$ is not the only variable governing the generation of failure events. Since the

failure arrival rate is almost constant in the short time (< 130 s), the oxide stack cannot be exclusively identified with the array of parallel resistances. On the contrary, it is likely that the whole circuit depicted in Fig. 2.17 (a) describes the insulator behavior under stress. It is worth mentioning that in a previous work [108], in order to explain the anomalous statistics exhibited by the time-to-first BD event, the presence of a residual thin SiO_x interfacial layer had to be assumed. It is not clear yet from the available data whether this layer would break down in a multifilamentary pattern and the Al_2O_3/HfO_2 nanolaminate performs as the series resistance.

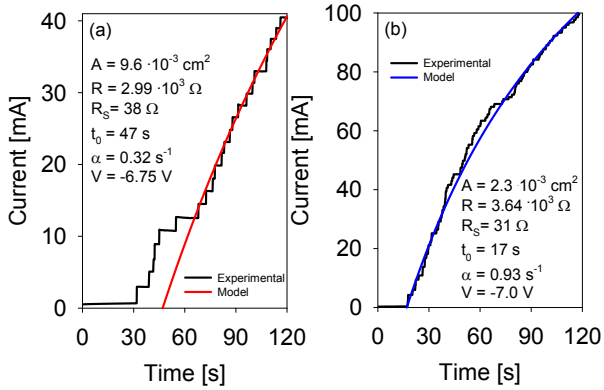

Figure 2.19: Continuous model approximation (Eq. 2.8): a) data from Fig. 2.17.(b) and b) data from Fig. 2.17 (c)

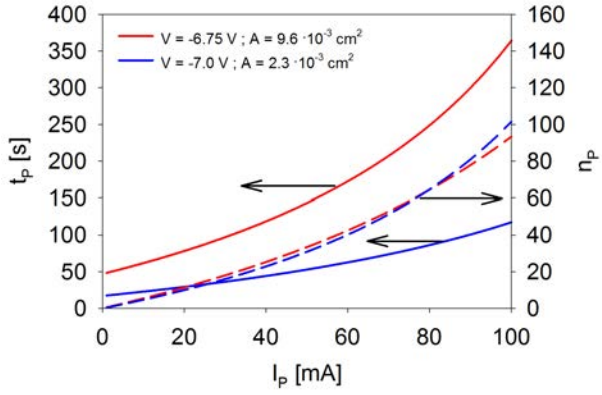

Figure 2.20: Programming time t_P and number of filaments n_P as a function of the target current level I_P for devices in Fig. 2.19. Model parameters in Fig. 2.19.

2.2.3.2 Modeling the overall breakdown behavior: function fit-model for the generation rate of conducting filaments

As it was mentioned in the previous Section 2.2.2, the remarkable change of trend in the I–t curves that takes place around 100-200 s for all the devices considered in this study indicates that some fundamental modification in the degradation process occurs during this intermediate phase of degradation. In order to illustrate in more detail this change of trend, Fig. 2.21 shows the number of registered BD events and the corresponding device resistance reduction as a function of time for a particular device. Two phases can be easily recognized. In the first phase, the resistance of the device sharply drops about two orders of magnitude, whereas in the second phase the resistance levels off around 10^2 Ω. Both phases can also be linked to a significant change in the number of registered events. No saturation effect in the number of events is observed in this latter case. This remarkable difference between both degradation phases might be indicative of the exhaustion of a particular kind of filaments rather than solely a series resistance effect, which is expected to be a continuous effect.

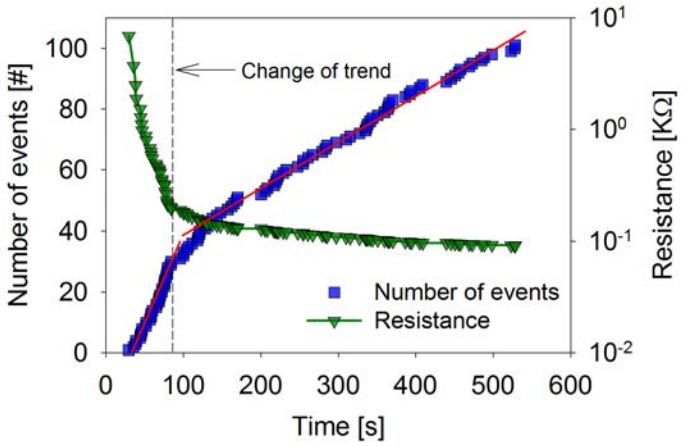

Figure 2.21: Number of failure events (■) and resistance values (▼) registered as a function of time. The dashed line points out the change of trend. The solid lines are guides to the eye.

As it is shown in this Section of the Chapter, this modification of the failure rate is simplified by assuming a non-linear failure generation model for the whole degradation process. The measurements reveal that the arrival rate of the failure events increases with the device area and with the magnitude of the stress voltage and that a correlation between the time-to-first filament formation and the initial current density for devices stressed at different voltages and with different areas exists (see paper **JVS17**). The obtained results quantita-

tively confirm that the onset of the filamentation process is a function of the initial leakage current condition of the device.

In order to reproduce the experimental results, a simple phenomenological model for the arrival rate of failure events is presented next. As illustrated in Fig. 2.22 (a), the number of generated filaments $n(t)$ can be approximately fitted using a power-law model of the form:

$$n(t) = \alpha t^{\beta} + \gamma \tag{2.11}$$

where α, β and γ are fitting constants for a particular realization. γ deals with the dispersion of the initial leakage current magnitude. α, β and γ depend on the device area and stress voltage. The model parameters for the average experimental curve shown in Fig. 2.22 (a) are included in the figure's inset. From 2.11, the failure arrival rate $\lambda(t)$ can be found as:

$$\lambda(t) = \frac{dn(t)}{dt} = \alpha\beta t^{\beta-1} \tag{2.12}$$

Notice that when β = 1, 2.12 reduces to a HPP [113]. Figure 2.22 (b) shows the algorithm used to add the stochastic dimension to the above expression.

The proposed algorithm is based on a time-dependent Poisson arrival process characterized by a deterministic function $\lambda(t)$ that describes how the intensity of the process changes over time. First, a BD time is generated in a finite time interval [T_{initial}, T_{final}]. Second, a random number in the range [0, 1] is generated and a new BD time is generated in a time length inversely proportional to the failure rate of the deterministic process. This is repeated several times until the process ends. For illustrative purposes, Fig. 2.22 (c) shows a sample curve generated by the function-fit approach (Eq. 2.12) in combination with the equivalent circuit proposed in Fig. 2.17 (a). Because of the non-linearity introduced by expression 2.12, the model is able to deal with the reduction of the failure rate already discussed in connection with Fig. 2.21. Notice the good agreement between the generated stepwise I–t curve and the experimental ones.

In addition, the dependencies of the filamentation process on the device area and stress voltage were explored in more detail in paper **JVS17**. There, the number of generated filaments $n(t)$ was fitted to the experimental data for different device areas and stress voltages using expression 2.11. After this, the failure arrival rate $\lambda(t)$ was calculated using 2.12. Power-law dependence are obtained for the three fitting parameters under consideration. A similar dependence with the stress voltage seems to hold but the voltage range investigated does not allow withdrawing precise conclusions.

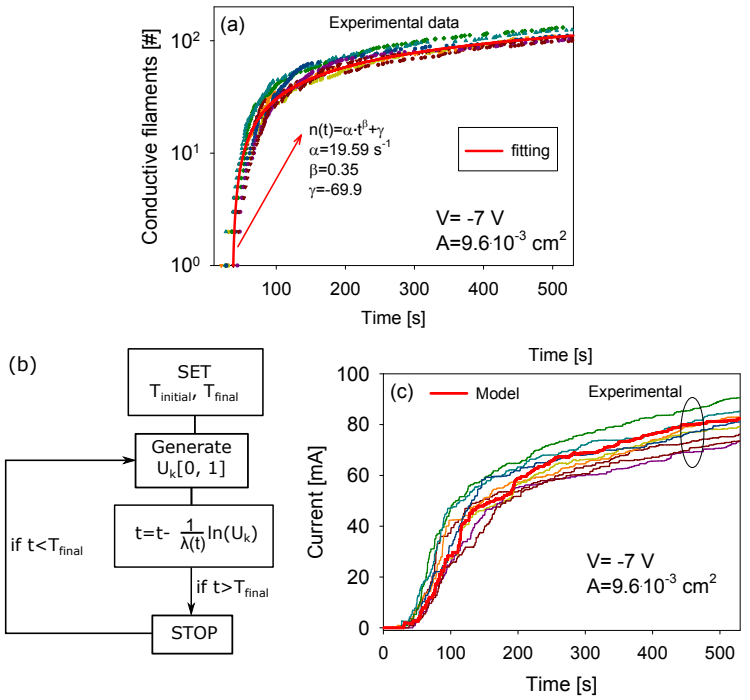

Figure 2.22: (a) Number of conducting filaments as a function of time. The solid line indicates the fitting to the experimental data. (b) Algorithm used for the simulation of the failure event arrival times. (c) Experimental and simulated I–t characteristics. The red solid line corresponding to the model was calculated from the generated events and the circuit representation of the device [118].

2.2.4 Conclusions

The main conclusions obtained in this sub-Section are the following:

- The breakdown time statistics of successive failure events in ALD-grown Al_2O_3/HfO_2 nanolaminates showed that the arrival rate of the failure events during a CVS was consistent with a NHPP.
- The number of failure events per time of this process was expressed as a combination of two individual power-law intensity functions.
    - The model parameters were found taking into account the superposition principle of multiple uncorrelated processes.
    - In order to demonstrate the adequacy of the proposed expression, simulated data obtained by the thinning method were compared to the experimental results.

- A simple circuit model consisting in an array of parallel and series resistances to account for the I–t characteristic of these devices was proposed.
    - The model can be used to determine the stress time required to set the device to a given current level.
    - This was of primarily importance for the programming operation of multilevel NVM devices based on the creation of multiple uncorrelated breakdown paths.
- In order to model the overall breakdown behavior, a deterministic function-fit model for the arrival rate of conducting filaments was proposed.
    - The stochastic dimension of the model was obtained by means of an iterative algorithm based on a NHPP for the arrival rate of the individual failure events.
    - This information was introduced into a circuital representation of the device and the current was calculated.
    - The experimental data confirmed that the arrival rate of the failure events depends on the device area and stress voltage, though the data was strongly affected by the initial leakage current. This information could be incorporated into the model parameters as well.
- Finally, it is worth noting that precise control of the number of failure sites can open the path for these investigated structures to be used in multilevel NVM devices as OTP memories.

Chapter 3

Metal-Insulator-Metal (MIM) Structures

In the last years, a wide variety of dielectric/electrode material combinations have been tested with the aim of achieving a ReRAM device with the best figures of merit in terms of cycle-to-cycle and device-to-device variability, accuracy in the definition of intermediate resistance states, compatibility with standard CMOS processes, and reliability. A number of studies point out that TiN/Ti/HfO_2-based ReRAM ranks among the best candidates [119, 120]. In addition, this stack complies with the main requirements to replace conventional nonvolatile memories for embedded applications [121–123]. They have been thoroughly tested for inter-cell variability [124], forming conditions [125] and characterized using high speed dynamical techniques [123]. In particular, the devices show bipolar switching behavior with high-speed operation ($<$10 ns), large ON/OFF ratio ($>$100), reliable endurance ($>$1 Mcycles), long high-temperature lifetime, multibit storage, and high device yield ($\sim$100 %) [126]. Nevertheless, a deep physics-based understanding is still needed. This understanding can emerge from the application of advanced characterization techniques and oxide reliability studies.

In this Chapter, we will focus the attention on TiN/Ti/HfO_2-based One Resistor (1R) and One Transistor–One Resistor (1T–1R) structures. We will evaluate the capability of both structures to store multiple bits and we will attempt to understand several issues behind the RS physical process. The obtained results will be useful to understand the capability to store multiple bits in ReRAM devices and to assess the feasibility of the studied devices to be

employed as artificial synapses in biological inspired neuromorphic systems. The goal also is to incorporate this understanding into a compact model suitable for circuit simulators. This model will be presented in Chapter 4.

3.1 1R-based MIM structures

This Section focuses on TiN/Ti/HfO_2/W (1R) structures. Firstly, the studied 1R-based MIM devices and their bipolar switching characteristics in the I–V and Q-ϕ domains will be presented. After that, the measurement conditions and setup employed to perform ultra-fast measurements will be described. The next part of the Section will focus in the analysis of the RS behavior through RVS performed with ultra-fast pulsed trains, where the evolution of the conductivity during the reset pulsed ramp and the energy required to perform the reset process will be in-depth analyzed. Finally, the capability to modulate the conductance of 1R devices will be discussed, which can be understood in terms of variations in the CF size and stoichiometry. The measurements will allow us to obtain a better insight into the physics behind the RS phenomenon and to evaluate the presence of multilevel states in the studied devices.

3.1.1 Electrical characterization

3.1.1.1 Device description

The devices investigated are 200nm-TiN/10nm-Ti/10nm-HfO_2/200nm-W MIM structures fabricated at IMB-CNM-CSIC, Spain (see Fig. 3.1). HfO_2 films were deposited by ALD at 225 °C using TDMAH and H_2O as oxidant precursors. TiN, Ti and W layers were deposited by magnetron sputtering. No post deposition thermal annealing processes were performed.

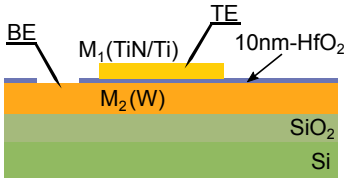

Figure 3.1: Schematic cross-section of the TiN/Ti/HfO_2/W structures.

The resulting structures are square cells of 5 x 5 μm^2. Notice that the Ti capping layer acts as an oxygen scavenger, favoring the creation and disruption of oxygen deficient conductive filaments in the HfO_2 layer.

3.1.1.2 Bipolar resistive switching characterization of 1R structures

The TiN/Ti/HfO_2/W samples show bipolar RS owing to the creation and destruction of oxygen deficient conductive filaments due to field and temperature assisted set and reset processes [127]. The top Ti electrode is the active electrode and acts as an O^{2-} reservoir that can release O^{2-} [128].

During the forming process a positive bias (V_F) is applied to the TiN/Ti top electrode, while the BE is grounded. In this former process, metal-oxide bonds break and oxygen-vacancy pairs are generated. The forming electric field leads to the migration of oxygen anions to the scavenging Ti layer, resulting in an oxygen deficient conductive path through the oxide and, thus, programming the cell to the LRS (see Figure 1.9 of the introduction Chapter). The reverse electric field (negative bias to the TiN/Ti electrode) and high temperature present during the reset process drives oxygen anions back to the conductive path partially recombining with the oxygen vacancies and, thus, programming the cell to the HRS. Finally, a set process is performed, applying again positive bias to the TiN/Ti electrode, where a CC of 1 mA has been employed. In this process the oxygen ions drift again to the Ti scavenging layer, programming the cell to the LRS [129].

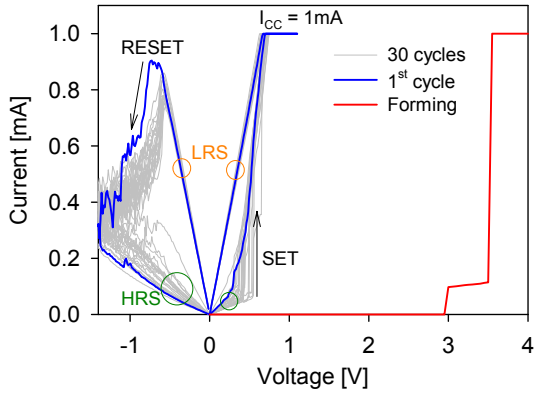

Figure 3.2: Bipolar RS behavior during successive set and reset cycles using quasi-static sweeps. First cycle (blue solid line), 30 curves (grey solid lines), and the forming process (red solid line) are shown.

Typical bipolar RS characteristics for the studied devices are shown in Fig. 3.2. An initial forming step is required in order to activate the switching properties. This is done using a conventional voltage ramp up to $V_F \sim 3.5$ V with a CC of 1 mA. Then RS cycles can be performed. It can be observed that the I–V curves exhibit larger cycle-to-cycle variability in the HRS than in the LRS. This observation agrees with previous investigations in Ti/HfO_2-

based devices [130]. The larger variability in the HRS compared to the LRS can be explained by larger morphological and stoichiometric variations of the CFs from cycle to cycle in the HRS. Notice that in the studied devices, the set process exhibits a sharp transition, while the reset process is more progressive [131, 132].

3.1.1.3 Flux-charge domain

Very often, RS devices are solely characterized in the I–V domain. However, representation in the Charge-Flux (Q-ϕ) domain, typical of memristive devices [52], can be found in the literature [133]. During my research stay at the Universitat de les Illes Balears (UiB) under supervision of Prof. Rodrígo Picos, I had the opportunity to become familiar with the Q-ϕ domain. Next, I will present an example of the Q-ϕ characterization carried out during the stay for the studied TiN/Ti/HfO_2/W devices.

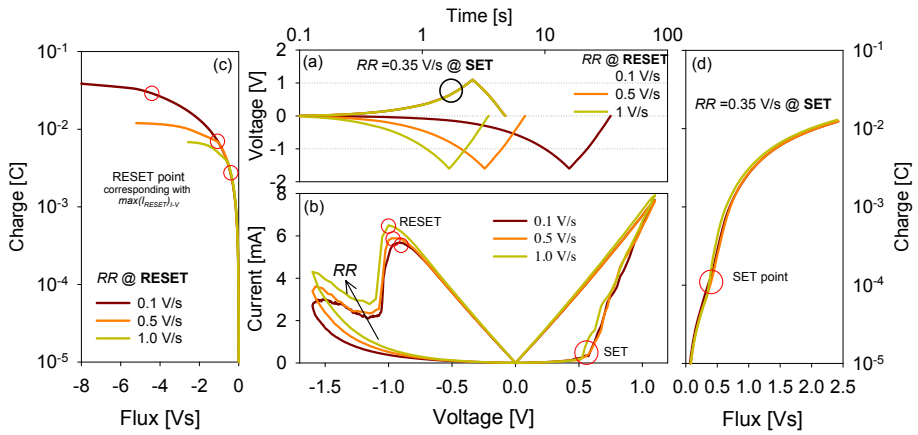

Figure 3.3: (a) Applied Voltage – Time (V–t) characteristics for set and reset processes at different rates. (b) Measured set and reset I–V characteristics for the different applied RR values applied during the reset process. The set RR is kept constant at 0.35 V/s. Q-ϕ characteristics for the (c) reset process and (d) set process.

In this example, the set and reset processes were repeated for 600 cycles. The RR of the reset process was varied by applying a negative voltage ramp up to -1.6 V with three different RR of 0.1, 0.5 and 1 V/s (200 cycles were performed for each RR). For the set process, a positive voltage ramp with a RR = 0.35 V/s was applied up to +1.1 V during the 600 cycles. This value was kept constant to avoid cross-correlation with the reset process. For these experiments maximum a CC of 100 mA was employed. The applied V–t are depicted in Fig. 3.3 (a).

The Q and the ϕ magnitudes are defined as the time integrals of current and voltage respectively [133]. The reset point corresponds to the maximum reset current in the I–V domain (see Fig. 3.3 (b)). This value, which is strongly dependent on RR, can be studied in the Q-ϕ domain in order to establish a correlation with RR (see Fig. 3.3 (c)). It can be seen that in the Q-ϕ space, the charge increases with flux considerably until the reset point is reached. At this point, the charge increase with flux is reduces significantly. This reduction is due to the small contribution to the time integral of the current after reset. Fig. 3.3 (d) shows the set process in the Q-ϕ space. The set point is indicated. In this case, as expected, once the set point is reached, the charge largely increases with flux.

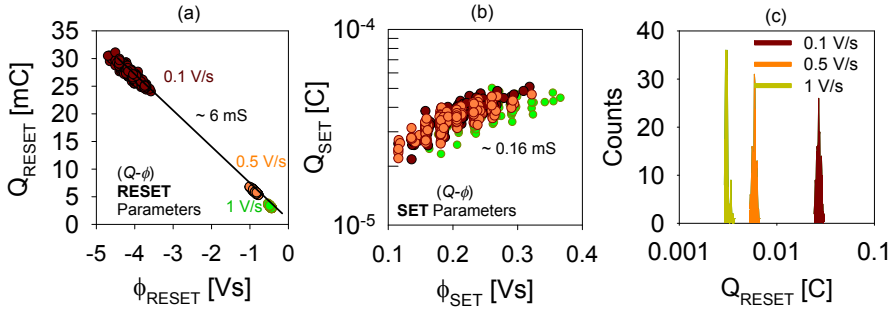

Figure 3.4: (a) Q_{RESET} vs ϕ_{RESET} for the studied RR conditions. (b) Q_{SET} vs ϕ_{SET} for each RR condition. (c) Histogram of Q_{RESET} values.

Figure 3.4 (a)-(b) show the values for the reset and set charges as a function of the flux for different RRs. Notice that a linear dependence of Q_{RESET} as a function of ϕ_{RESET} is observed, where the slope ∼6 mS indicates the conductance in the LRS. The histograms of Q_{RESET} for the different RRs are represented in Fig. 3.4 (c), indicating a clear decrease of Q_{RESET} when RR increases. In the case of Q_{SET} as a function of ϕ_{SET}, similar values between the different RRs are obtained for the 600 cycles. This behavior can be attributed to the fact that RR during the set process was kept constant. Notice that a conductance value in HRS was found to be 0.16 mS. From these results it can be concluded that modifications of RR in the reset process do not significantly affect the set point.

Finally, we can conclude that using the Q-ϕ domain it is possible differentiate temporal behavior effects hidden in the I–V plot. This information can be included to model the I–V curves, such as it can be seen in Ref. [134] where the effect of the RR on the reset voltage obtained from the analysis of curves in the Q-ϕ space was included in the *Memdiode* model for SPICE simulators (presented in Chapter 4).

3.1.1.4 Advanced characterization: ultra-fast pulsed ramps

The main objective of the advanced characterization was to evaluate the impact of the RR on the device response by applying ultra-fast pulsed ramps. For this purpose, during the experiment the ultra-fast signals were applied during the reset process, while the set process was performed using quasi-static measurement conditions.

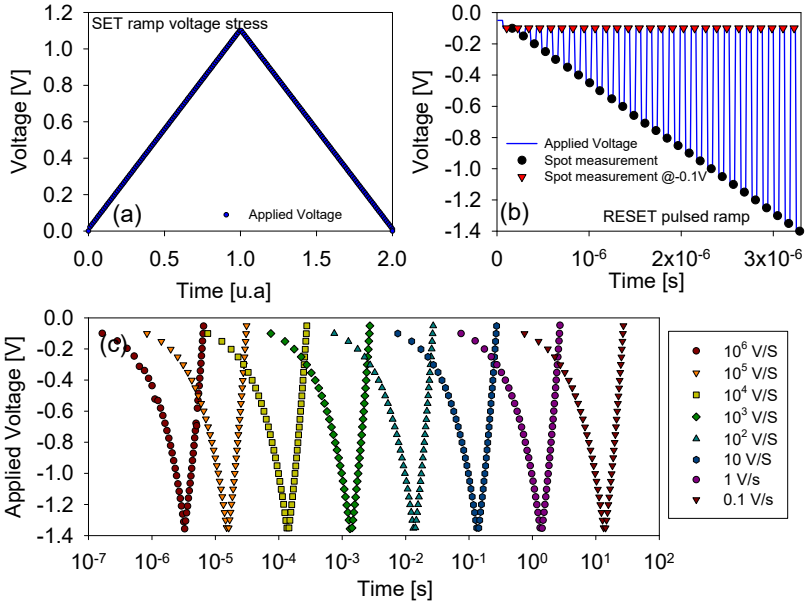

Figure 3.5: (a) Input signal (V-t) employed to perform the set process. (b) Applied voltage waveform programmed to perform the reset process through ultra-fast pulsed ramps. The spot measurements are acquired at the height of the pulse to evaluate the switching characteristics during the pulsed ramp, while the conductance is measured @-0.1 V. (c) Ranging the pulse width from 50 ns to 50 ms in combination with a ramp step voltage of 50 mV, yields to RR values ranging from 1 MV/s to 0.1 V/s, respectively. Rise/fall times are 10 ns.

For the RS characterization, quasi-static double-sweep voltage ramps were applied from 0 to 1.1 V for the set operation (see Fig. 3.5 (a)). Notice that a CC of 1 mA was employed during the set process to prevent irreversible cell breakdown and to limit the conductance of the LRS through the experiment. For the reset process, ultra-fast pulsed measurements were programmed from 0 to -1.4 V (Fig. 3.5 (b)), where I–V–t data were registered during the pulsed trains, enabling an accurate control of the conductance vs. time during the measurements. Between the pulses a reading step at -0.1 V during 50 ns was performed in order to evaluate the evolution of the device conductance through the pulsed ramp (Fig. 3.5 (b)). The ultra-fast electrical measurements were performed by using a Keysight B1500 semicon-

ductor parameter analyzer, equipped with the pulse generator module WGFMU. The voltage was applied to the TiN/Ti TE with the W BE grounded. The use of WGFMU setup allowed us to measure the conductance in both, during the pulsed ramps and at the reading step -0.1 V (see Fig. 3.5 (b)). Figure 3.5 (c) shows that varying the pulse width from 50 ns to 50 ms and including a voltage ramp step of 50 mV, yields to RR values ranging from 1 MV/s to 0.1 V/s, respectively. The rise and fall time are 10 ns, which can be neglected to calculate the RR. It should be remarked that there are 7 orders of magnitude between the minimum and maximum RR used.

3.1.2 Device response to pulsed ramps during the reset process

3.1.2.1 Reset ramp rate effect on the switching characteristics

The experimental reset characteristics for different pulsed RR values are shown in Fig. 3.6 (a), where each of the represented I–V curves correspond to the median of 30 curves. The measurements are shown for RRs ranging from 10^6 V/s to 0.1 V/s. First, the RR was decreased from 10^6 V/s to 0.1 V in steps of one decade. After that, the RR was increased again to 10^6 V/s in order to evaluate the impact of cycling on the measurement results. It should be noted that during the set process the RR was kept constant, and that the reset point (voltage and current) was obtained from the maximum reset current. Several observations can be extracted from the results shown in Fig. 3.6:

Firstly, the I–V response plotted in Fig. 3.6 (a) shows that the reset voltage increases as RR increases. Furthermore, when RR is increased again both curves for RR = 10^6 V/s show similar current level (reproducing results), indicating that the observed increase of the reset voltage with the RR can be attributed to the measurement speed instead of aging mechanisms during device operation. According to the thermal and field-driven migration mechanism in bipolar VCM RS devices, the reset time can be determined by Eq. 3.1, where a voltage dependent activation energy is described to define ion migration process [135].

$$t_{\text{reset}} = \frac{\phi^2}{D_0} \exp\left(\frac{E_a - q\alpha V}{k_B T}\right) \tag{3.1}$$

where ϕ is the filamentary diameter, α is a coefficient controlling the voltage induced barrier lowering for hopping, k_B is the Boltzmann constant, E_a the thermal activation energy, D_0 is a constant indicating the pre-exponential factor of diffusivity and T the absolute temperature.

In Fig. 3.6 (a) it can be observed that higher reset currents are reached when RR increases (see Fig. 3.6 (c)). This fact can be explained because for higher RRs, less time is spent at

each voltage, and therefore lower CF temperatures can be reached during the pulsed ramps, thus according to Eq. 3.1 larger voltages to shrink the filamentary path are required.

Moreover, it has been found that the reset voltages as a function of the RR follow a logarithmic dependence (Fig. 3.6 (b)). These results are consistent with thermally and field activated reset mechanisms [136] and are in close agreement with the results reported in [137, 138] and with the experimental trends observed for 1T–1R (see Section 3.2.2.1 and paper **MEE17**).

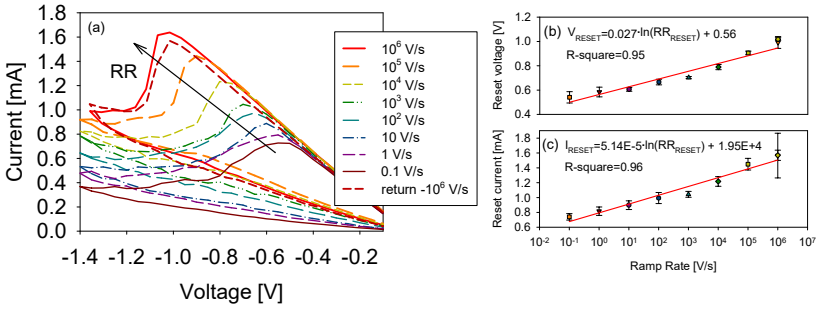

Figure 3.6: (a) Measured I–V characteristics during reset process for different pulsed RR values. The set RR is kept constant. Experimental data and logarithmic fitting for reset. Each curve represents the median of 30 cycles. (b) Reset voltage and (c) current as a function of RR. Notice that the logarithmic slope 0.027 V of Fig. 3.6 (b) is in good agreement with the experimental trends observed for 1T–1R devices shown in Section 3.2.2.1 and the paper **MEE17**.

Secondly, Figure 3.6 (a) shows that higher RR provokes sharper reset transitions. The gradual decrease of the resistance during the reset process observed for lower RRs can be understood in terms of slower transport of O^{-2} due to lower reset voltages and currents [139].

Once analyzed the effect of the RR on the reset characteristics, we will investigate the impact of the reset RR on the set process. Figure 3.7 (a) shows the complete I–V characteristics during the pulsed ramps for the reset process and the quasi-static ramps for the set process. As expected, for a given RR, both polarities show a symmetrical LRS and HRS conduction. However, the higher RR in the reset process results in higher HRS current, and consequently lower set voltages. In addition, the impact of the reset RR in the set voltage is shown in Fig. 3.7 (d), where a logarithmic dependence, with negative slope, is found. This dependence may influence the conduction of the LRS after the set process in spite of a CC of 1 mA is reached once the set process is completed (see Fig. 3.7 (b)-(c)).

Furthermore, as shown in Fig. 3.8 (a), a clear correlation between the conductance in

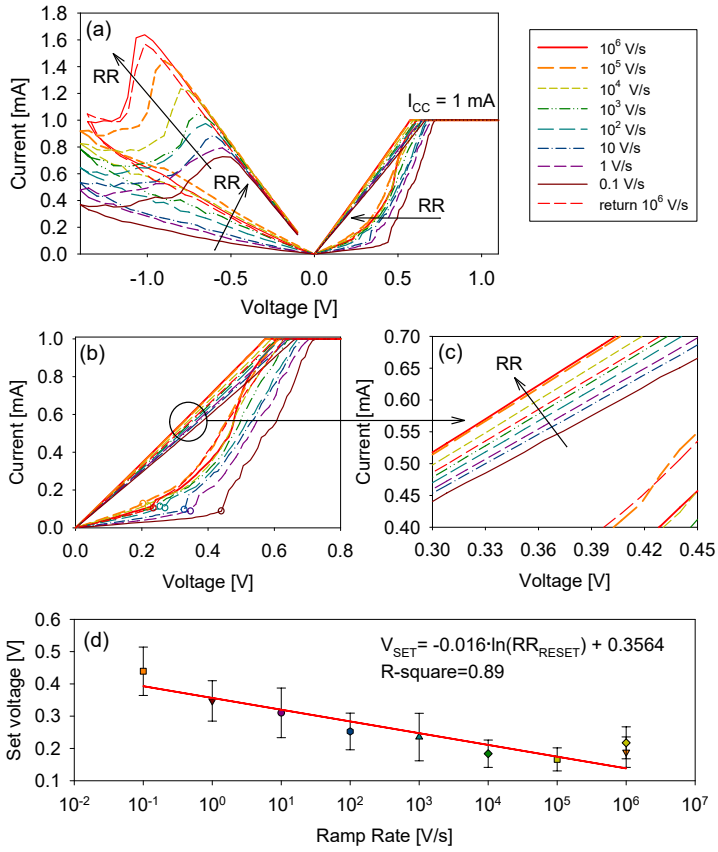

Figure 3.7: (a) I–V curves for pulsed RR during the reset process ranging from 1 MV/S to 0.1 V/s. The RR during the set process is kept constant. (b) Influence of the pulsed RR values during the previous reset process in the LRS current level. (c) Zoom of the pulsed Fig. 3.7 (c). (d) Set voltage as a function of the previous reset RR.

HRS and the RR values employed during the pulsed RR process exists. Similar results are reported in [138] where a logarithmic dependence is observed with the saturation HRS current. This observation points out that the RR determines the maximum conductance allowed in the HRS. In order to investigate if this trend is a result of the RR employed or the device aging, measurements with random RR were performed. Fig. 3.8 (b) shows the measured I–V curves during the reset process for sequential cycles with a random reset RR, confirming the reproducibility of the impact of the RR on the reset process shown in Fig. 3.6 (a), and demonstrating that the observed trends are a result of the employed reset RR instead of cycling aging.

To further evaluate the impact of the RR on the reset mechanisms, the energy dissipated

in the devices during the reset process and the reset time for the different RRs was extracted by means of $E_{reset} = \int_0^{t_{reset}} Pdt$, where $P = V \cdot I$ is the power. Figure 3.9 shows the measured reset time and experimental reset energies as a function of the reset voltage for the different RRs evaluated. Notice that a $log(t_{reset})$ vs. reset voltage dependence is observed and points out that larger reset voltages reduce the reset time, and consequently the energy consumption for switching [140]. This result is in agreement with the Arrhenius dependence of the physical mechanisms responsible of the bipolar RS behavior in VCM devices (see Eq. 3.1) [141].

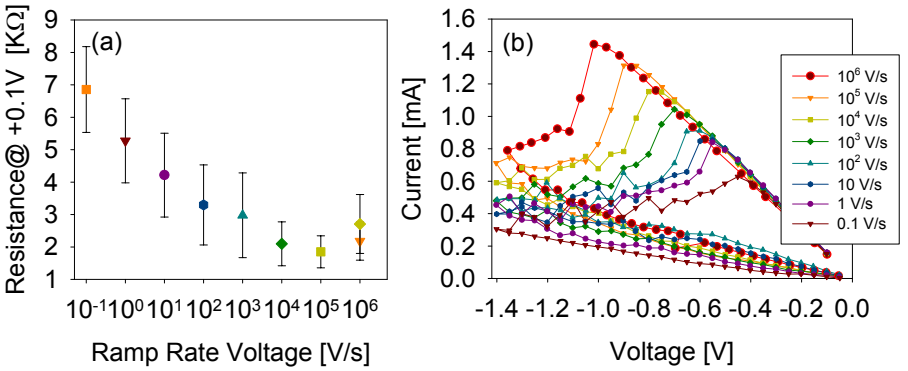

Figure 3.8: (a) Resistance at -0.1V in the HRS as a function of the pulsed RR used in the previous reset processes (b) Measured I–V characteristics during the reset process for consecutive cycles with a random RR. The measurement procedure employed is depicted in Fig. 3.5 (c)

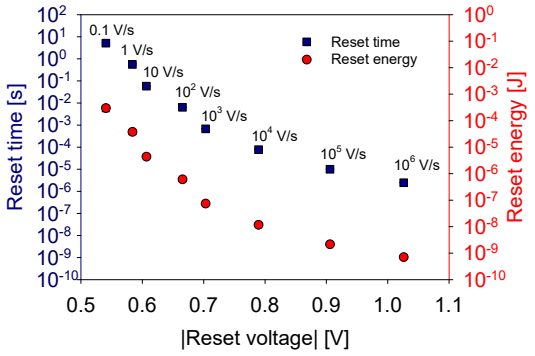

Figure 3.9: Measured reset time and reset energy as a function of voltage for the pulsed RR measurements. The corresponding RR values are shown.

3.1.2.2 Modulation of the device conductance during the reset process

The conductance evolution of the LRS and the HRS measured at -0.1 V during the reset process for the different RRs is studied in this sub-Section. Figure 3.10 illustrates the conductance evolution monitored (@-0.1 V) after each high pulse during the reset process for RR ranging from 10^6 V/s to 0.1 V/s.

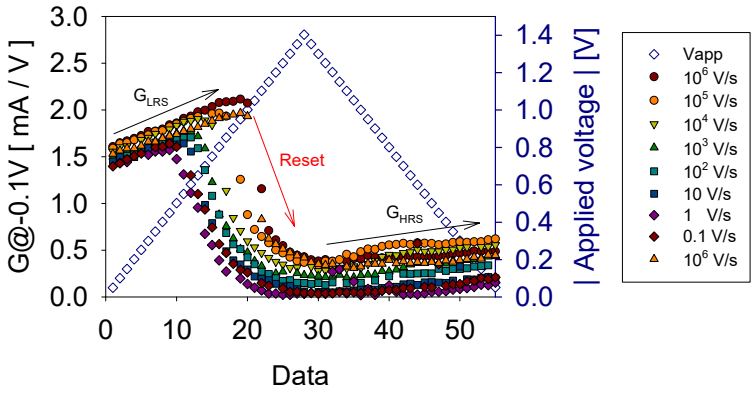

Figure 3.10: Conductance (G) during the reset process measured at -0.1 V after each reset pulse with an amplitude of V_{app}.

As it can be seen the conductance changes abrupter, from LRS to HRS, for higher RR compared to lower RR values. This agrees with the trends observed from the measurements during the high spot pulse presented in Fig. 3.6 (a). Besides that, the conductance in the LRS sligthly increases with the pulse amplitude during the pulsed ramp. The obtained results suggest that the application of an electrical stress can imply small variations in the resistance prior to the reset process, in the sense that the cell can slightly vary its conductance state during the electrical stress indicating morphological and stoichiometric changes of the CFs.

The analysis of the conductance properties of the filamentary path provides useful information if it is studied in terms of the quantum conductance G_0 = 2e^2/h = $(12.9K\Omega)^{-1}$. A qualitative explanation of the evolution of the CF structure in terms of the G_0 is given in the schematic diagram of Fig. 3.11.

In the LRS ($G \gg G_0$), a large number of conductive defects (oxygen vacancies) form a wide CF with metallic conducting properties (Ohmic behavior). During the application of the pulsed ramp, a critical temperature is reached and induces the reset process, and causes a significant narrowing of the CF. After this, the CF conductance progressively evolves until

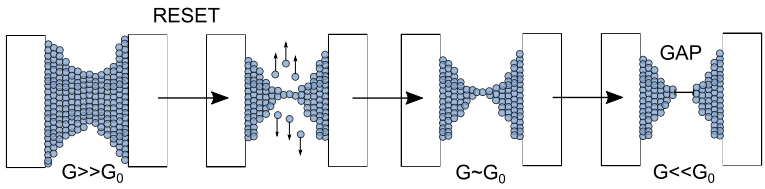

Figure 3.11: Schematic representation of the evolution of the CF structure during the reset transient.

the CF is only composed by one or few single defect paths ($G \backsim G_0$). The final transition to the HRS occurs when a gap is opened in the CF ($G \ll G_0$). In this figure, we have arbitrarily assumed that the CF becomes narrower in the center of the insulator film. However, asymmetric CF shapes are also possible, and this should not significantly alter the results [89].

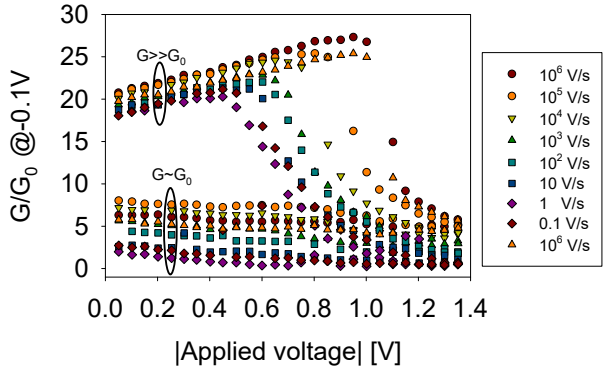

Figure 3.12: G/G_0 during the reset process measured at -0.1 V after each reset pulse with an amplitude of V_{app}.

As it can be seen in Fig. 3.12 in the studied 1R devices, the LRS show G values around $\backsim$ 25 G_0, indicating a wide and fully formed CF. While the HRS includes G values of the order of G_0, which can be interpreted as the signature of atomic-size configurations of the filamentary path without a spatial gap [89]. Notice that the obtained values for the CF conductance are few times G_0, suggesting the presence a CF cross-section corresponding to few atomic size conducting defects. Therefore, during the reset process a progressive narrowing of the CF up to the limit of a quantum wire (with at least one conducting channel with $G \backsim G_0$) can be reached. These results may suggest the contribution of a non-linear regime in the HRS of the devices which can be linked to the presence of a potential barrier associated to the atomic-size constriction according to the QPC Model [142]. From the

results observed it can be concluded that the conductance during the reset process of the devices can be tuned between $G/G_0 \sim 25$ to $G/G_0 \sim 1$, where lower conductance can be obtained for lower RR values. This result points out the potential of the studied devices for multilevel and neuromorphic applications.

3.1.3 Conclusions

In this sub-Section several conclusions can be drawn:

- The reset process in TiN/Ti/HfO_2/W bipolar resistive switching 1R devices performed through RVS with ultra-fast pulsed trains has been analyzed.
    - A logarithmic increase of the reset voltage with RR has been observed, supporting the thermal and field activated reset mechanism.
    - The set and reset process show symmetrical LRS and HRS conduction.
    - It has been proved a correlation between the conductance in HRS and the pulsed RR values employed during the previous reset process, indicating that the RR controls the conductance in the HRS.
    - The analysis of the I–V curves during the reset process for consecutive cycles with a random reset RR, confirm the reproducibility of the results, indicating that the observed trends can be attributed to the measurement speed instead of aging mechanisms during device operation.
    - Reset time and energy present a logarithmic correlation with reset voltage. This fact is connected to the Arrhenius dependence of the physical mechanisms behind bipolar VCM devices.
- The modulation of the conductance due to CF size variations during reset process was also investigated:
    - The conductance changes abrupter from LRS to HRS, for higher RR compared to lower RR values.
    - The device can slightly vary its conductance state during the pulsed ramp previous to the reset processes, suggesting small changes in the CF size and stoichiometry.
    - The HRS includes values of CF conductance of the order of G_0 during the reset transition, suggesting the presence of a CF cross-section corresponding to few atomic size conducting defects.

- The conductance during the reset process of the studied 1R devices, can be tuned from $G/G_0 \backsim 25$ to $G/G_0 \backsim 1$, in the RRs ranging from 0.1 to 10^6 V/s, where lower conductance was observed for lower RR values. This result points out the potential of the studied devices for multilevel applications.

3.2 1T-1R-based MIM structures

In this Section, a detailed characterization of the 1T–1R structures will be presented. This will include the techniques used to measure the time-to-BD and BD voltage distributions. Measurements are aimed to determine the conduction properties of RS filamentary conduction in connection with the signal applied to the device terminals. Then failure physics investigation will carried out on the devices under study. Given that BD is ultimately related to the generation of defects in the oxide layer, it will also discuss the physics behind this process and the corresponding BD statistics in the framework of the time-to-failure thermochemical model. This Section ends with a discussion of the key findings that will be relevant for improving the compact model aforementioned.

3.2.1 Electrical characterization

3.2.1.1 Device description and experimental methods

The ReRAM devices investigated as part of this PhD Thesis are 1T–1R devices fabricated at LETI-CEA, France (see Fig. 3.13 (a)). The MIM structure, sketched in Fig. 3.13 (b), is formed by a 10 nm-thick ALD HfO_2 layer sandwiched between two metal electrodes (Ti and TiN), acting the Ti as an oxygen scavenging layer. To prevent irreversible cell breakdown and to control the maximum current that can flow through the memory cell [143] in the LRS, an integrated n-type MOSFET is used in series with the ReRAM cell. Notice that the transistor does not play any role in the HRS of the switching device. I–V–t measurements were performed using a Keithley 4200-SCS semiconductor parameter analyzer equipped with a 4225-RPM PGU (pulse generator unit). The setup used for all measurements is shown in Fig. 3.13 (c). Three different experimental procedures were used, one for each type of experiment, and which will be explained next:

RVS experiments: For RVS measurements, the CC level is adjusted by setting the transistor gate voltage (V_G) to 1.2 V for set conditions. V_G =4 V is used to avoid any current limitation during the reset transition. To activate the switching property a forming step with

gate voltage of 1.2 V is required. Fig. 3.13 (d) shows the input signal used for the RVS experiments. I–V–t data were obtained using pulsed signals which enables accurate control of the time measurements. This allow us to obtain conductance values at +0.1 V after each high spot measurement. For the set process, the BE is grounded, and the input signal is applied to the TE. Opposite connections are used for the reset process. In both processes, the input signal has positive sign. This procedure is used to control the CC established by the N-MOS transistor and to avoid possible leakage currents. Data were then obtained using pulsed measurements (ΔV = 50 mV) with pulse widths (Δt) ranging from 1 μs to 1 ms corresponding to RR in the range from 50 Vs^{-1} to 50 KVs^{-1}. The delay time between two high pulses is 100 ns.

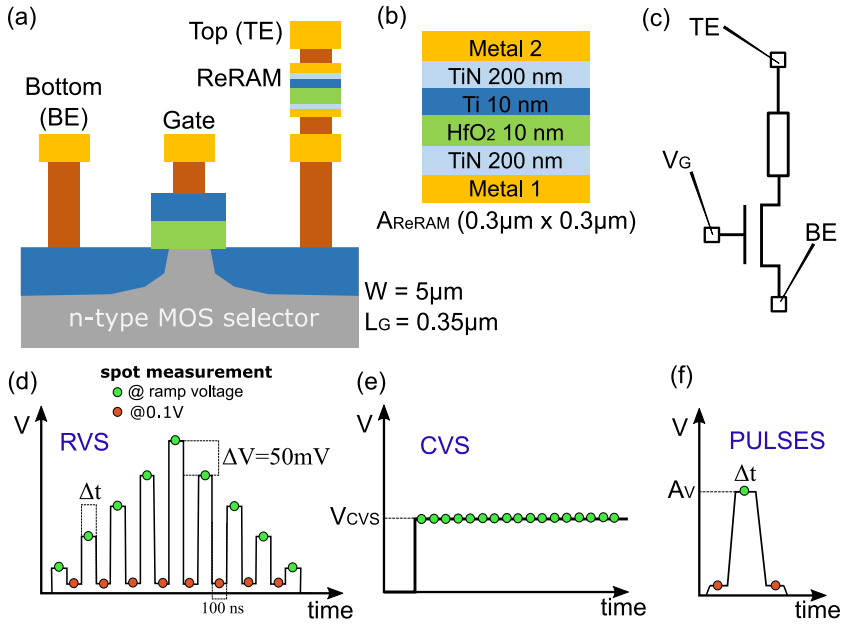

Figure 3.13: (a) Schematic representation of the 1T–1R structure. (b) Device stack. (c) Scheme of the setup used. Schematic for the different stress modes used: (d) RVS experiment (e) CVS experiment and (f) PULSED experiments.

CVS experiments: In this case, the experiment consisted in switching the state of the device from the HRS to the LRS (set condition) by means of a CVS (see Figure 3.13 (e)) with V_G = 1.2 V. The switching from LRS to HRS (reset condition) was induced by a RVS. These two stages make up a cycle. 100 cycles were performed per CVS at 8 different set voltages V_{CVS}: 0.30 V, 0.35 V, 0.40 V, 0.45 V, 0.50 V, 0.55 V, 0.60 V and 0.65 V. During the CVS experiment the voltage was applied to the TE while the BE was grounded. Since the set consists in the breakdown of the filament gap, the time-to-set (t_S) is identified with the

time-to-BD of the electroformed device.

PULSED experiments: We have also performed set and reset pulsed measurements with different pulse duration (Δt) ranging from 100 ns to 100 μs and a with a pulse amplitude (A_V) ranging from 0.75 V to 2.25 V (see Fig. 3.13 (e)). Conductance at +0.1 V is obtained before and after each high spot (pulse) measurement. Similar to the RVS experiments, BE and TE are grounded or biased depending on whether we are dealing with the set or reset process. V_G = 1.2 V and 4 V were used for the set and reset conditions, respectively.

3.2.1.2 Bipolar resistive switching characterization of 1T-1R structures

The operational principle of the ReRAMs has been widely investigated and relies on the repetitive formation (LRS) and rupture (HRS) of a conductive pathway spanning the oxide film. The formation of the filament occurs during the initial forming procedure by the local accumulation of oxygen vacancies and it is destroyed by a recombination process with oxygen ions, which can be restored during set process. The transition between states is associated with the appearance of a gap region in the formed filament whose width (t_{GAP}) is independent of the oxide layer thickness (t_{OX}) (see Fig. 3.14 (a)). Within these processes, the oxide electric field plays a fundamental role as the driving force for the displacement of atomic species [14]. This affirmation will be further discussed along this Section.

The device under investigation (see papers **MEE17**, **MER17** and **EDL18**) exhibits bipolar switching with abrupt set and gradual reset transitions. Typical I–V RS characteristics for the 1T–1R configuration after the forming process, which takes place at ≈3.8 V, are shown in Fig. 3.14 (b), where fifty cycles (gray solid line) were performed with a RR of 50 Vs^{-1}. The heavy solid line represents the median curve of these cycles (blue solid line). It should be noted that set and reset voltages are almost symmetric ($\approx \pm 0.5$ V@50 V/s), which indicates a common triggering mechanism for both polarities. This would indicate voltage controlled processes for HfO_2 in agreement with the results reported in [138] and with the indirect deductions reported in [141], in which both set and reset are voltage controlled processes occurring at constant and similar voltages. In [141], both processes were modeled by voltage-driven CF growth and dissolution, respectively, and it was strongly supported the common nature of the set and reset mechanisms. Notice also the transistor action for positive bias V $>$ 0.75 V. The limit imposed by the transistor saturation current allows controlling the damage caused to the ReRAM during the set process. As it will be shown below, this damage is also determined by the RR of the input signal for identical CC.

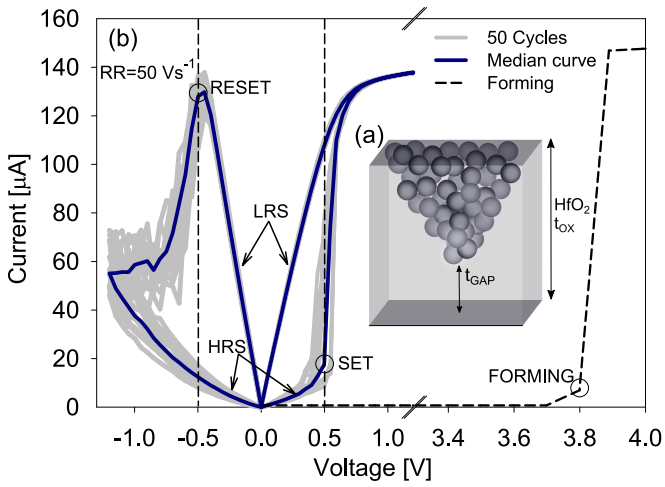

Figure 3.14: (a) Schematic representation of the conductive path, representing the distance t_{GAP} within the oxide layer thickness t_{OX}. (b) 50 quasi-static I–V characteristics (RR = 50 Vs^{-1}). The heavy solid line is the median curve.

3.2.1.3 NMOS transistor and multilevel operation

The NMOS transistor used to control the current flow was also characterized. Figure 3.15 (a) shows the $I_{DS} - V_{DS}$ curve for different V_{GS}. Figure 3.15. (b) illustrates the control of the set by means of the transistor gate voltage. CC is adjusted by setting the transistor gate voltage from 1.2 V to 1.6 V in steps of 0.1 V for set and employing 4 V for reset condition in any case, being their corresponding CC levels 140 μA, 240 μA, 352 μA, 470 μA, 600 μA for the set gate conditions and 3.5 mA for the reset gate conditions. The reset gate voltage must be high enough to allow reaching the desired reset current level [81, 82, 91]. Notice also the ability to control the CC as well as the ON resistance (R_{ON}) and reset current. R_{ON} decreases and the reset current increases for increasing CC, that is the maximum current during set [126, 136, 144]. In particular, the set transition is dictated by a constant product $R_{ON} \cdot CC \sim 0.40$ V, this is the voltage across the ReRAM at the end of the set transient, thus suggesting a voltage controlled dynamics of set, in agreement again with [141].

Figure 3.15 (c) shows the measured reset current as a function of CC. Reset current scales linearly with CC such as it has been widely reported [141, 145]. The similar values for CC and reset current strongly support the common nature of set and reset mechanism, which is the basis for the switching model used in [146]. In addition, Figure 3.15 (d) shows how the maximum reset voltage controls the OFF resistance (R_{OFF}). In this case, cycling was performed with the maximum reset voltage (0.8 V, 1.0 V or 1.2 V). Both procedures shown

in Fig. 3.15 (b) and 3.15. (d) allow us to achieve multiple resistance states which is of relevant importance for neuromorphic applications.

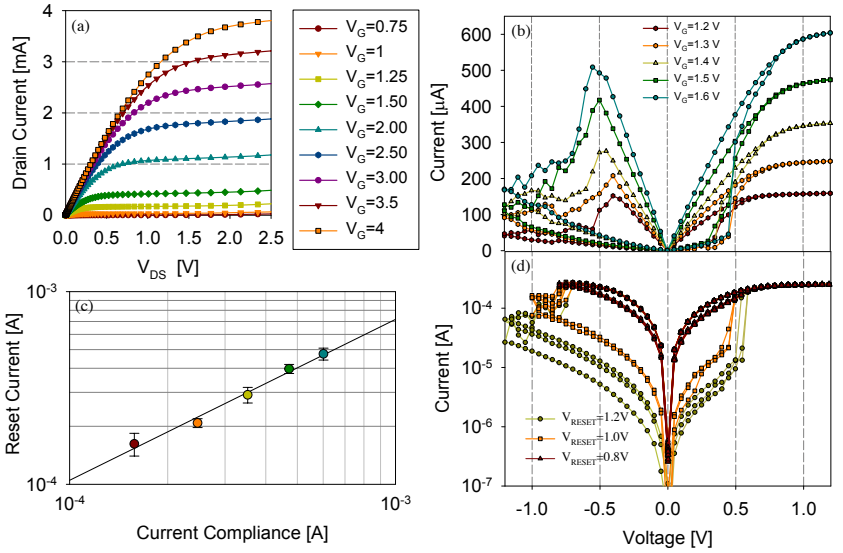

Figure 3.15: (a) $I_{DS} - V_{DS}$ characteristics for NMOS transistor. (b) I–V characteristics at a variable compliance current CC defined by V_G ranging from 1.2 to 1.6 V. (c) Measured reset current as a function of CC. (d) I–V characteristics show the control of R_{OFF} by maximum reset voltage.

3.2.2 Switching statistics

3.2.2.1 Effect of the voltage ramp rate on the switching voltages

In paper **MEE17** we investigated the influence of the voltage ramp rate, defined as the ratio $RR = \Delta V/\Delta t$, on the switching characteristics. Figure 3.16 (a) and (b) illustrates the effects of RR on the set and reset I–V characteristics, respectively. Note that the reset RR and the set RR are kept constant at 50 V/s, respectively. Clearly, both set and reset voltages exponentially increase with RR in a similar fashion, which seems to be consistent with the experimental results reported in [137, 147, 148] and in the previous Section 3.1.2.1, where the influence of the RR on set and reset voltages is studied for MIM structures. Intuitively, this seems to imply that in order to grow the filament (during set) at faster RR, we need a higher "power", because there is insufficient time for defects to nucleate and evolve at lower voltages for high RRs [12]. Likewise, a similar higher "power" is required to start diluting the filament during reset. As the same defect species are responsible for the two processes,

indeed similar voltage dependence can be expected. Further, faster reset will also allow less time for effective deconstruction of the filament, in agreement with the observed increase of saturation current @-1.2 V.

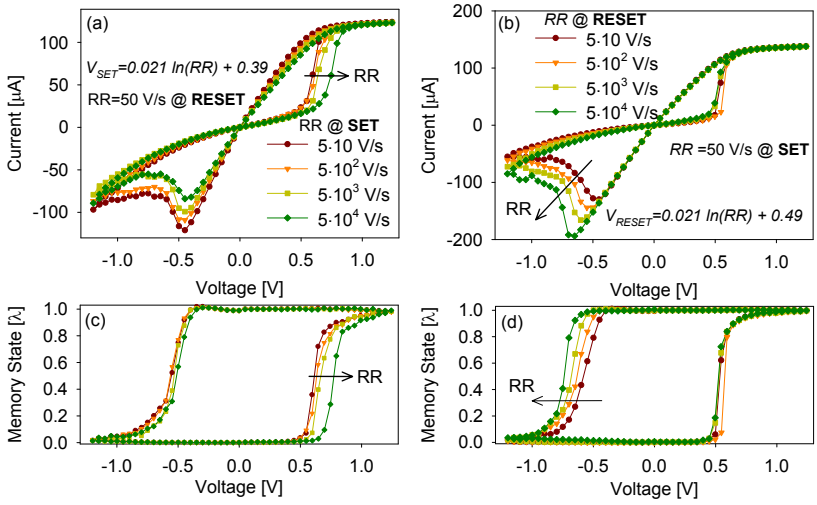

Figure 3.16: (a) Measured I–V characteristics for different RR values during the set process. The reset RR is kept constant at 50 Vs^{-1}. (b) Measured I–V characteristics for different RR values during the reset process. The set RR is kept constant at 50 Vs^{-1}. Each curve corresponding to the median of fifty complete cycles. Normalized current @+0.1 V as a function of the previous applied voltage pulse: (c) set process, (d) reset process [149].

For the case of the set process (Fig. 3.16 (a)), in spite of the transistor action over the LRS current during the set process [150, 151], it is demonstrated that RR also determines the maximum current allowed for lower biases. This can be seen as a reduction of the LRS current for higher RR values and in consequence as a reduction of reset voltage in the negative bias quadrant. From these observations, it is clear that a higher RR causes a lower accumulated damage to the structure. In the case of the reset process (Fig. 3.16 (b)), notice also that there is a difference in the HRS currents, but this is a consequence of incomplete resets. High negative voltages to completely reset the device can cause irreversible damage to the structure [136,152]. In addition to the generation of the dynamic I–V curve, the current flowing through the ReRAM is also measured at a very low positive voltage (@+0.1 V) in between the increasing/decreasing voltage pulses. This latest measurement when plotted as a function of the previous applied bias allows obtaining, after a proper normalization, the hysteron loop that represents the memory state of the device ($0 \leq \lambda \leq 1$) [153]. The hysteron map was extracted from the experimental data illustrated in Fig. 3.16 (a) and (b) and represented in Fig. 3.16 (c) and (d), respectively. The effects of RR on the hysteron's

transition edges are clearly visible. These results will be used in the next Chapter to simulate the I–V curves in connection with the *Memdiode* model for ReRAM devices.

3.2.2.2 Identification of the CF generation/rupture mechanism

The stochastic nature of the atom rearrangements is reflected in the set and reset voltages and switching times of the devices. These rearrangements can be due to meta-stable states that can change over time because of dielectric degradation. The rate of degradation of the materials can be accelerated by a higher stress and/or an elevated temperature. From the reliability point of view the development and use of the acceleration models is of utmost importance to identify the degradation mechanism involved.
Because of the random generation of defects in the insulator, the CF development has a random nature and requires a statistical description. In order to examine the voltage-dependent acceleration law in the framework of voltage-driven oxide BD, we consider different acceleration models for the generation and rupture of the filamentary pathways. They were explored with the aim of clarifying their activation mechanism and the connection with oxide breakdown theories. The acceleration laws considered here are: the V power-law, E-model, $E^{1/2}$ model and 1/E-model, where E is the applied electric field [9]. Instead of E, the applied voltage V is the variable used for the analysis because of the initial uncertainty in t_{GAP}. Accordingly, Figure 3.17 (a) shows Weibull plots for t_S obtained by CVS ranging from 0.3 V to 0.65 V in steps of 50 mV. The associated Weibits can be expressed as:

$$ln(-ln(1-F)) = \beta \cdot ln(t_S/t_{63\%}) \tag{3.2}$$

where F is the CDF, β the shape factor, and $t_{63\%}$ the scale factor. Weibull plots exhibit average shape factor β = 1.17 $\pm$ 0.13, which corresponds to a HfO_2 film with thickness $t_{OX} \approx$ 2 nm [154]. Therefore, a partially formed filament with an insulating region of about $t_{GAP} \approx$ 2 nm can be assumed in the HRS.

Notice that the number of data points for 0.30 V and 0.35 V in Fig. 3.17 (a) is low because of type I censoring effects (t_S longer than the time-of-test-termination). This uncertainty was corrected using parametric survival analysis considering uniform acceleration (voltage-independent β) [156]. Note that acceleration models usually only deal with the scale factors because the Weibull slope is found to be independent of voltage and temperature [13]. The standard plot $t_{63\%}$ vs V_{CVS} does yield such conclusive results. Following McPherson's analysis for the breakdown of thin oxides [9], Fig. 3.17 (b) and (c) show t_{S63} and $\gamma_V = -dln(t_{S63})/dV_{CVS}$, respectively, as a function of V_{CVS} for the acceleration

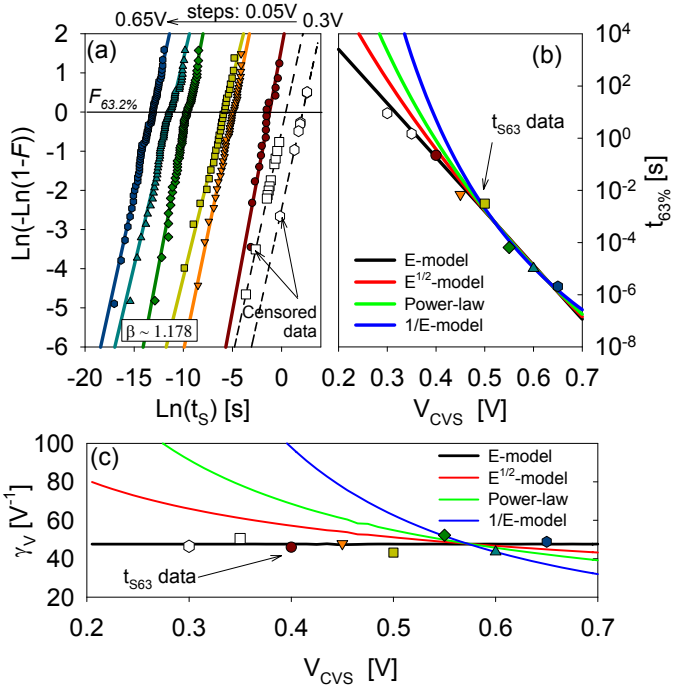

Figure 3.17: (a) t_S distributions for CVS experiments ranging from 0.3 V to 0.65 V in steps of 50 mV. Symbols are experimental data. Solid and dashed lines are fitting results. F is the cumulative probability. (b) Projection of t_S for a CVS failure percentile for the E-model ($t_S \sim \exp(-\gamma V)$), $E^{1/2}$-model ($t_S \sim \sqrt{\delta V}$), 1/E-model ($t_S \sim \exp(-\beta/V)$) and power-law model ($t_S \sim V^{-n}$). The symbols refer to the $t_{63\%}$ by multiples CVS used. (c) $\gamma_V = dln(t_{S63})/dV_{CVS}$ as a function of V_{CVS} for different acceleration models [155].

models mentioned above. Available data confirm that the best fitting result corresponds to the E-model:

$$t_{S63} = t_0 \exp(-\gamma_V V_{CVS}) \tag{3.3}$$

where a voltage acceleration parameter γ_V = 47.59 V^{-1} is found and t_0 = 3.49 $\cdot 10^7$ s is a constant. Importantly, 3.3 is an empirical relationship that overrides the temperature dependence. The non-Arrhenius dependence of γ_V has been extensively reviewed in [9] and [157]. But this topic should be treated with tact. For some time, it was assumed that the temperature dependence of time-dependent dielectric BD followed an Arrhenius relationship, i.e., $t_S \sim \exp(E_a/k_B T)$. Where E_a is a thermal activation energy of the defect generation process. Indeed, the dependence was observed in many early studies of oxide BD. E_a was observed to decrease for increasing applied gate voltage or electric field [158–160] which

was predicted by the thermochemical model [158]. In some reports E_a was observed to change with temperature [161]. Definitively, the obtained results indicate that the E-model (associated with the thermochemical model for dielectric BD) is closely connected with the formation and rupture of the atomic bridges that switch the oxide conduction state.

In order to complete the analysis, CVS and RVS experiments were compared. Experiments reveal that both the 63% set (V_{S63}) and reset (V_{R63}) voltages linearly increase with $ln(RR)$ (see Fig. 3.18 (a)). This indicates not only that a faster damaging process requires a higher field to meet the switching condition but also that the triggering mechanisms exhibit similar behavior regardless of the bias sign (identical acceleration factor $\Gamma_{S,R} \approx 44.2$ V^{-1}) [138] indicating the suitability of the thermochemical model. The statistical results obtained from CVS and RVS methods can be directly related to one another by considering the relation of the BD to the cumulative defect generation [16]. Data obtained from CVS and RVS experiments can be jointly assessed by means of the AFI method explained in paper **MER17**. The method allows representing CVS data (t_S,V_{CVS}) in terms of its equivalent RVS data (V_S, RR). In particular, for the E-model, the AFI method reads:

$$t_S = \int_0^{t_S} A_f \cdot dt = \int_0^{t_S} \exp\left[\Gamma_S \left(RR \cdot t - V_{CVS}\right)\right] dt \tag{3.4}$$

where A_f is the acceleration law. Since $V_S = RR \cdot t_S$, 3.4 yields:

$$V_S = \frac{1}{\Gamma_S}\left[ln(RR) + ln(t_0 \cdot \Gamma_S)\right] \tag{3.5}$$

which is consistent with the experimental data shown in Fig. 3.18 (a). Figure 3.18 (b) shows $\Gamma_S = \{dV_{S63}/dln(RR)\}^{-1}$ for the different acceleration models under consideration. Again, the E-model exhibits the best agreement with the experimental data ($\Gamma_S = 44.2$ V^{-1}).

3.2.2.3 Ionic transport

The E-model not only seems to provide the best fitting results for our samples but it is also one of the most popular models used to describe defect generation through the thermochemical model [162–165]. The model is based on defects (traps) which are fundamentally oxygen vacancies that arise from the breakage of Hf-O bonds. Then, the reason behind the exponential and logarithmic dependencies for the switching voltage and time statistics can be found in the migration of oxygen ions within the oxide layer through field-assisted and thermally-activated hopping [148, 166]. To support this idea, the ion current (i_{ion}) can be calculated

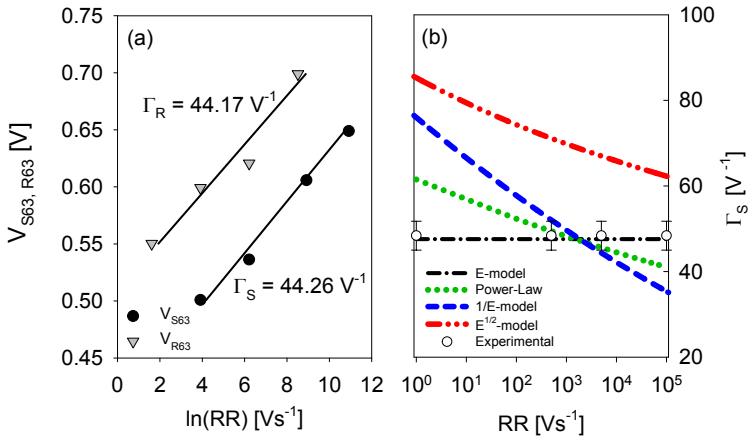

Figure 3.18: (a) V_{S63} and V_{R63} as a function of $ln(RR)$. (b) Γ_S as a function of RR for the different acceleration models under consideration.

from the generation probability of oxygen vacancies [128]. The charge required to reach the set condition, Q_S, can be approximately expressed as:

$$Q_S = \int_0^{t_S} i_{\text{ion}} \cdot dt \approx \int_0^{t_S} i_0 \exp\left(\frac{\alpha z e}{k_B T} V\right) dt \tag{3.6}$$

where i_0 is a constant, $0 \leq \alpha \leq 1$ the symmetry factor, z the number of exchanged electrons, e the electron charge, and $k_B T$ the thermal voltage. From 3.6, t_S under CVS reads:

$$t_S = \frac{Q_S}{i_0} \exp\left(-\frac{\alpha Z e}{k_B T} V_{\text{CVS}}\right) \tag{3.7}$$

which is formally equivalent to 3.3 for a fixed temperature. Assuming z = 2 and T = 300 K, α = 0.61 is obtained from the experimental data. Similarly, for RVS, $dt = dV/RR$ so that 3.6 yields:

$$V_S = \frac{k_B T}{\alpha z e}\left[ln(RR) + ln\left(\frac{Q_S}{i_0} \cdot \frac{k_B T}{\alpha z e}\right)\right] \tag{3.8}$$

which closely resembles 3.5. In this case, for z = 2 and T = 300 K, α = 0.57 is obtained from the experimental results. In both cases, $\alpha \neq 0.5$ indicates a slightly asymmetrical diffusion barrier for the ions. Since both 3.3 and 3.7, and 3.5 and 3.8, share the same dependence with V_{CVS} and RR, respectively, it is worth discussing the connection between the E-model and the ion transport equation. According to McPherson-Berman's approach [167] it is found

that for a variety of oxides, the product

$$\gamma_E E_{BD} = E_a/k_B T \tag{3.9}$$

is a constant independent of the material permittivity κ. γ_E is the field acceleration parameter, E_{BD} the breakdown field. E_a is the energy required for ion displacement from its normal local bonding environment in the absence of applied field. Experimentally [167, 168],

$$\gamma_E = 1.58\kappa^{0.66} \tag{3.10}$$

$$E_{BD} = 29.9\kappa^{-0.65} \tag{3.11}$$

Since $\kappa \approx$ 22-25 for HfO_2 [73], γ_E = 12.15 - 13.22 cm/MV and E_{BD} = 4.0 - 3.7 MV/cm are found from 3.10 and 3.11, respectively. These latter values are close to the electroforming field E_{BD} = 3.8 MV/cm obtained from Fig. 3.14 (b) (10 nm thick-layer). Now, using 3.3 and 3.10, $t_{GAP} \approx \gamma_E/\gamma_V$ = 2.55 - 2.77 nm in agreement with the results obtained from the Weibull slopes shown in Fig. 3.17 (a). Moreover, since $\beta \approx t_{GAP}/a_0$ (cell-size) [167], a percolation cell-size a_0 = 2.17 nm is found. In addition, from Eq. 3.9, E_a(300 K) = 1.25 eV is obtained, which coincides with the barrier height reported in [136].

From the oxide reliability viewpoint, the dissolution of the gap can be regarded as a transition in the reaction space from a meta-stable state towards a degraded state characterized by a lower free energy (see Fig. 3.19 (a)). This lower energy arises from a molecular dipole-field interaction [167]. On the other hand, from the ion migration viewpoint, the formation/destruction of the conducting atomic bridge is the consequence of a thermal-assisted hopping mechanism with barrier lowering (see Fig. 3.19 (b)). The link between both visions is ultimately Kramers' escape rate theory [168, 170] which relates the transitions to the probability of a particle jumping from one potential well to another by passing over a barrier. From Kramers' theory [165]:

$$t_S^{-1} = k = k_0 \exp\left[-(E_a - e\alpha V)/k_B T\right] \tag{3.12}$$

where k is the reaction rate and $k_0 \sim 7.10^{13}$ Hz is the Hf-O bond vibration frequency [171]. 3.12 arises from a diffusive dynamic with vertical thermalization (inside the well) much more rapid than the horizontal outflow [172]. Matching the empirical law 3.3 with the theoretical expression 3.12 provides a new method to obtain a rough estimation of the filament temperature as a function of the applied voltage. The obtained range, 300 K - 600 K (see Fig. 3.19 (c)), is in agreement with thermal simulations [90]. Here, Temperature is

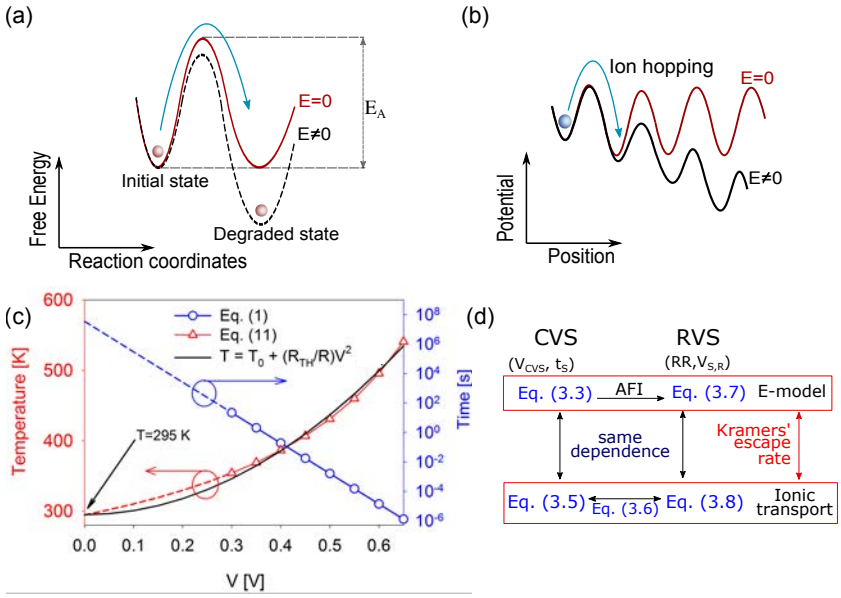

Figure 3.19: (a) Free energy description associated with the material degradation. (b) Schematic representation of random ionic jump over a potential barrier. (c) Filament temperature as a function of the applied voltage. T_0 = 295 K, R_{TH}/R = 567 K/V^2 (Empirically extracted) (d) Schematic relationships between the model equations [169].

extracted from Eq. 3.12 and gives as result the Eq. 3.12. Our results confirm that Kramers' theory provides a consistent framework for analyzing constant and ramped voltage stress experiments in the context of ReRAM devices.

For the sake of clarity, the link among the corresponding models and equations are depicted in Fig. 3.19 (d). In order to achieve better insight into the model results, a closed-form expression for the CF temperature can be obtained from Eq. 3.12. In this case, the temperature reads:

$$T = \frac{E_a - e\alpha V}{k_B[ln(t_S \cdot k_0)]} \tag{3.13}$$

which yields T(0V) = 295 K as expected for equilibrium conditions.

3.2.2.4 Pulsed experiments

Pulsed experiments were also performed in a range of $\sim$ 1 - 2 V in voltage amplitude and three orders of magnitude in time pulse width (from 100 ns to 100 μs). Resistance ratio can be adjusted during pulse measurements by changing pulse amplitude and pulse time duration,

as it is demonstrated in Fig. 3.20 (a). In this case, keeping the set conditions fixed at 1.5 V pulse amplitude and 5 μs time width, we vary the reset pulse width time from 100 ns to 100 μs for three different reset pulse amplitudes of 1 V, 1.5 V and 2 V. Each point with its error bar corresponds to the statistics of 200 identical stress cycles. Figure 8 (b) shows the CDF for R_{OFF} using the same data shown in Figure 3.20 (a). The voltage pulse amplitude affects more significantly the $R_{\mathrm{OFF}}/R_{\mathrm{ON}}$ ratio than the pulse time width even if voltage is only changed in $\sim$1 V while the time width changes by three orders of magnitude. This is due to the highly non-linear time-voltage dependence. Note that this kind of extremely non-linear dependence is a requirement for the successful application of ReRAM because of the set-speed/read-disturb trade-off. In these experiments, the on/off ratio is increased by increasing the pulse height or width, i.e. by increasing the reset stress and the off-resistance. A trade-off between the high resistance ratio and the endurance is observed. The best conditions for high endurance are obtained for a relatively small pulse amplitude. Figure 3.20 (c) shows the effects of more than 100 Mcycles for V_{pulse} = 1.25 V and $t_{\mathrm{RESET}} = t_{\mathrm{SET}}$ = 10 μs where the device presents a large endurance.

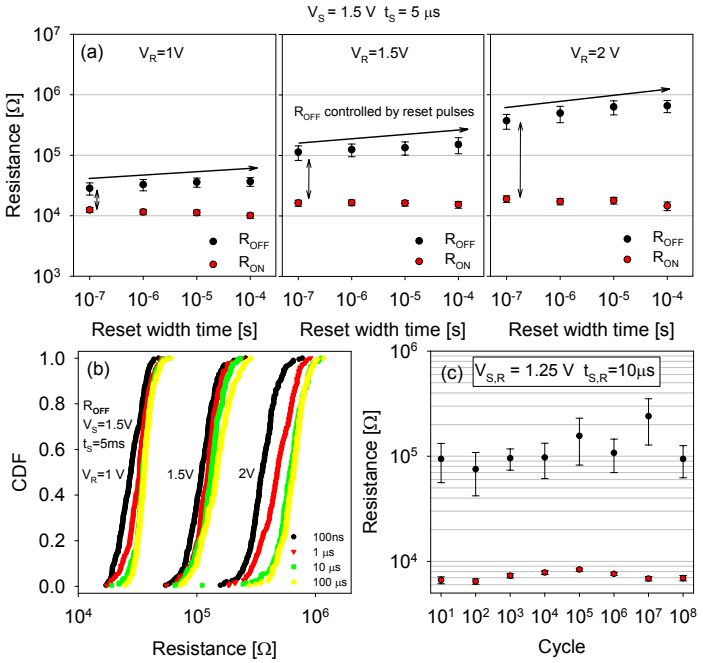

Figure 3.20: (a) R_{OFF} and R_{ON} in single pulse experiments with different reset pulse amplitudes, V_{RESET} = 1 V, V_{RESET} = 1.5 V and V_{RESET} = 2 V (from left to right), and t_{RESET} changing from 100 ns to 100 μs. The set pulse was kept constant (V_{SET} = 1.5 V t_{SET} = 5 μs). (b) CDF of R_{OFF} for the collected data in Fig 3.20 (a). (c) Statistics for the endurance characteristic of the 1T–1R device. The resistance ratios of HRS to LRS are more than 10 during the 100 Mcycles of fatigue test [173].

3.2.2.5 Second-order memristor effects

As it was seen at the introduction Chapter, ReRAM devices are memristors [174], i.e. two-terminal electrical devices whose conduction properties depend on internal state variables which are governed by dynamic ionic processes. Usually, when described mathematically, ReRAM devices are treated as first-order memristors, i.e as having only one internal state variable, namely the device resistance, R. A first-order memristor follows the equation:

$$\frac{dR}{dt} = f(R, V, t) \tag{3.14}$$

However, internal switching mechanisms are usually not that simple, and other variables can play a significant role during switching so that a higher-order description might be necessary. In particular, it has been recently shown that temperature T or another variable related to the ionic conductivity in the CF might play a significant role [175, 176]. Whenever two variables have significant relevance to determine the internal state of the device, a second-order memristor model is required which can be mathematically described as:

$$\frac{dR}{dt} = f(R, T, V, t) \tag{3.15}$$

where T represents the second internal variable (temperature or another variable). Second order memristor effects have been recently shown to allow biorealistic emulation of synaptic functions which can be very useful in neuromorphic circuits showing not only long-term memory but also short-term plasticity [175, 176]. In the characterization of our ReRAM devices, we have found some experimental results which suggest the occurrence of second-order memristive effects. Figure 3.21 (a) shows the results of pulsed experiments in which the voltage pulse amplitude is the same for set and reset (V_S = V_R). We have explored how $R_{\text{OFF}}/R_{\text{ON}}$ depends on the pulse amplitude and time width. In this experiment, the pulse voltage is monotonously increased from 0.75 to 2.25 V and, for each voltage, the pulse width is increased from 100 ns to 10 μs and 200 pulses are applied for each stress condition (to obtain a distribution of results for each represented data point). The results are shown in Fig. 3.21 (a) and it follows that, consistently with what is reported in Fig. 3.20 (a) and (b), the off-resistance and on-off ratio increases with both voltage and pulse width. However, when, at the end of the stress, after applying the most severe reset conditions and reaching a maximum ratio $R_{\text{OFF}}/R_{\text{ON}} \sim 10^2$, the pulse voltage sequence is repeated for a lower pulse amplitude of 1.25 V (in the same time-width space) we find that the results are significantly different (almost one order of magnitude) from what was previously found in

the same experiment. This is an indication of a dependence of the device performance on its switching history and that the overall shape of the CF or the ionic mobility shows long-term changes which depend on how the device was stressed. This is a clear case of second-order memristor effects [175, 176]. In this particular case, we can in principle discard the temperature as the second state variable because the time scales of our experiments are much longer than expected for heat dissipation [175]. Further investigation is required to unveil the details of high-order memristive effects in these devices. This provides an independent indication on the fact that current switching depends on the previous switching history so that the system cannot be modeled as a first-order memristor.

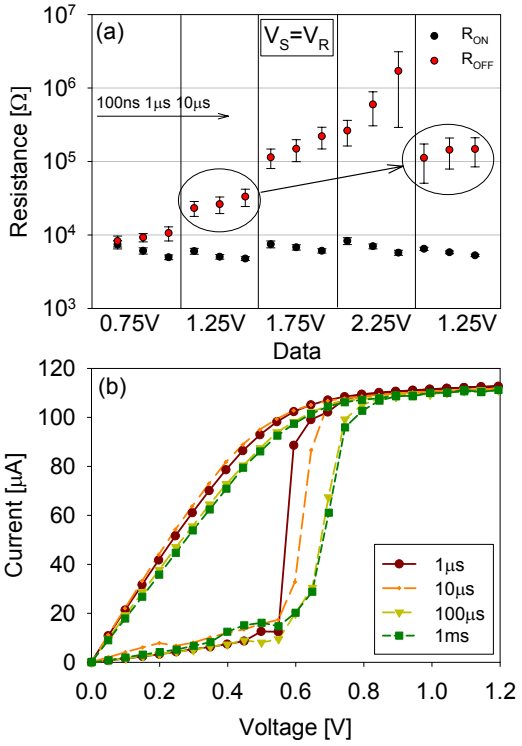

Figure 3.21: (a) R_{OFF} and R_{ON} in pulsed ($V_{SET} = V_{RESET}$) experiments with voltage ranges from 0.75 to 2.25 V. Reset time sweeps from 100 ns to 10 μs in all the cases. 200 pulses per experiment. Notice that behavior at 1.25 V after applying higher voltages yields different results than after low voltages. (b) I–V characteristics during the set process, keeping the pulse width time fixed to 1 μs, and ranging the pulse delay time from 1 μs to 1 ms.

A final experiment carried out consisted in the application of a train of pulses with increasing voltage and constant pulse width but with a variable delay time in between them. For a first-order memristor, one would expect that changing the delay time would not have

any significant effect on the results since only a small voltage is applied to measure the state of the device after each stress pulse. Nevertheless, as shown in Figure 3.21 (b), decreasing the delay time between pulses accelerates the set transition, and this is exactly what could be expected for a second-order memristor. When there is a second variable affecting the internal state of the device, the separation of successive pulses is relevant because the application of one pulse leaves the device in a situation in which it is more prone to potentiation (conductance increase) or depression (conductance decrease) when the following pulse arrives. Since the effects of the second state variable, T in equation 3.14, usually decay in a shorter time scale and do not cause permanent long-term changes in the memristor internal state, if the separation between successive pulses is long enough, second-order memristor effects are expected to be negligible for long delay times. This is exactly what is found in Fig. 3.21 (b), in the which the results obtained for the longer values of delay time (100 μs and 1 ms) almost fully coincide while a shift to lower reset voltages and a deeper change of device conductance is progressively found when the delay time is shortened (10 μs and 1 μs). This is another piece of evidence to support the existence of second-order memristor effects in the ReRAM devices studied in this work.

3.2.3 Conclusions

- We have electrically characterized ReRAM devices with a Ti/HfO_2(10 nm)/TiN structure in a 1T–1R configuration. We have assessed the transistor action in what concerns the control of the maximum current during set and the on-resistance. Multiple resistance states can be reached by varying the maximum reset voltage in RVS experiments.

- We have investigated the influence of the voltage RR on the set and reset transition voltages of ReRAM devices. It was shown that they can be described by a logarithmic relationship. This seems to indicate a common physical origin for both kind of transitions.

- From the oxide reliability viewpoint, constant and ramped voltage stress experiments provide strong support to the so-called E-model, which is shown to be in line with current theories relating the reversibility of the conduction states in ReRAM devices with ionic drift and ultimately with Kramers' escape rate theory. It is shown how the switching statistics can be used to estimate the width and formation energy of the gap in the filament as well as its temperature.

- Pulse-based experiments have demonstrated that it is possible to change the on-off re-

sistance ratio by changing the reset pulse width and, more efficiently, the reset pulse voltage amplitude. However, a set of two different kinds of experiments revealed the existence of second-order memristor effects. This means that there is at least a second internal state variable that cannot be ignored during device operation or characterization. These effects can be very useful for the operation of these devices in neuromorphic circuits and cannot be ignored when operating the devices as non-volatile resistive memories.

Chapter 4

Compact Modeling of Resistive Switching and Simulation Results

ONE of the goals of device engineers is to formulate compact models of electronic devices that can be used later for the purposes of optimization, prediction, and circuit simulations. While such models should be simple enough for practical programming, for example, in popular SPICE environments, they should also include the necessary physics to account for the device behavior. Otherwise, the model predictive power becomes limited and reduces to a fitting model. Depending on the degree of knowledge one has on the device physics, either a black-box modeling approach (if one has little idea on how the device works) or a white-box modeling (if the device physics is well understood) can be applied. To develop highly accurate ReRAM device models, a combination of black- and white-box modeling is in general acceptable since device operations are only partly understood. In this regard, the most frequent case is the gray-box method, that is when some parameters have a clear physical meaning while others have solely an electrical meaning in the context of the model used. Thus, a gray-box approach using some prior knowledge and its combination with experimental data seem to be a suitable approach for ReRAM modeling [12].

This Chapter reports a compact model for the conduction characteristic of bipolar ReRAM devices based on a diode-like structure with memory properties. As the starting point we have used a compact model developed by *E. Miranda* in which the hysteretic behavior associated with the set and reset processes is implemented using a recursive operator [153]. The original model is able to qualitatively reproduce the experimental results in several bipolar

RS devices [177] but it is unable to account for the progressive evolution of the memory state and the effect of the signal frequency. In Chapter 3 a detailed characterization of the 1R and 1T–1R MIM-based structures was presented with the aim of incorporating detailed information into the compact model concerning the generation/rupture process of the filament as well as the temporal information, with the aim of following a gray-box approach. An updated version of the model that includes the temporal behavior is reported here. This new version is able to deal with arbitrary input signals and it is simple enough to be easily implemented in any programming language. In our case we have chosen the free and popular simulation software LTSPICE but any other language is feasible. The model has been fitted to data measured on 1R and 1T–1R devices fabricated at IMB-CNM-CSIC, Barcelona, Spain; and LETI-CEA, Grenoble, France, respectively.

4.1 Introduction to the Memdiode model

In ReRAM devices the change of the resistance depends on the history of the device, that is, it exhibits a hysteretic relationship between the applied electric field and the current through it. Associated with this kind of behavior there is a huge variety of potential applications in which memristive devices can be used: memory devices, neuromorphic systems, analog and chaotic circuits, and computational logic, among others. Numerical simulations are of great benefit when designing and characterizing circuits involving memristive elements. For such, a simple and accurate model that embodies the major fingerprints observed in experiments was recently developed [153]. As the starting point of this Chapter, the *Memdiode* model is described.

4.1.1 Model equations

As we saw in the introduction Chapter, many SPICE models reported in the literature are commonly associated with the first memristor definition put forward by Strukov et al. [50, 178,179]. However, these models do not account for many of the features observed in experiments, for instance, threshold-type switching [178]. The *Memdiode* model which is based on a non-rectifying diode-like (exponential behavior) structure for the electron transport and the hysteron formalism for the memory state [153], takes into account voltage-dependent hysteresis, and it is able to describe the major and minor I–V loops in bipolar resistive switches. The electron transport equation is based on the diode equation with series resistance I–V

which expresses as:

$$I(V) = sgn(V)\left[\frac{1}{\alpha R_S} W\left\{\alpha R_S I_0(\lambda)\cdot \exp\left[\alpha\left(\mid V \mid + R_S I_0(\lambda)\right)\right]\right\} - I_0(\lambda)\right] \tag{4.1}$$

where *sgn* is the sign function, α a fitting constant, R_S the series resistance, and $I_0(\lambda) = I_{max}\cdot\lambda + I_{min}\cdot(1-\lambda)$ the current amplitude factor. I_{max} and I_{min} are the maximum and minimum current values of I_0, respectively. Notice that α and R_S can have similar dependence on λ. $\alpha(\lambda) = \alpha_{max}\cdot\lambda + \alpha_{min}\cdot(1-\lambda)$ and $R_S(\lambda) = R_{S,max}\cdot\lambda + R_{S,min}\cdot(1-\lambda)$, respectively. Notice that, as expected for a memristive system, Eq. 4.1 always yields a pinched I–V curve ($I(V=0)=0$) regardless of its parameter values [153]. W is the Lambert function, which can be approximated by:

$$W(x) \approx ln(1+x)\cdot\left(1 - \frac{ln(1+ln(1+x))}{2+ln(1+x)}\right) \tag{4.2}$$

Equation 4.1 can switch between an exponential HRS and a linear LRS response curve (see Fig. 4.1 (a)). For the memory map ($\lambda - V$), which controls $I_0(\lambda)$ in 4.1, channel conduction (single or multifilamentary) is assumed, with set and reset voltages of the individual channels given by Gaussian distributions. The memory state is expressed as:

$$\lambda_t = min\left\{\Gamma^-(V_t), max[\lambda_{t-1}, \Gamma^+(V_t)]\right\} \;\; t = 1,2,3,\cdots \tag{4.3}$$

where $\lambda_t \in$ [0,1] and V_t are the discretized values of the state variable and input signal, respectively. $\Gamma^{\pm}$ are the so-called ridge functions (hysteron's edges) which are logistic functions representing the sequential creation or destruction of the conductive channels as a function of the applied voltage. The logistic behavior arises from the integration of the Gaussian distribution. The ridge functions are given by:

$$\Gamma^{\pm}(V_t) = \left\{1 + \exp\left[-\eta^{\pm}\left(V_t - V^{\pm}\right)\right]\right\}^{-1} \tag{4.4}$$

where $\eta^{\pm}$ are the transition rates, and $V^{\pm}$ the threshold voltages. This defines the hysteron curve shown in Fig. 4.1 (b). The hysteron in turn controls the diode parameters in a linear fashion, i.e: $I_0(\lambda)$. Equation 4.3 corresponds to the case where the characteristic time for channels generation is very large compared to the characteristic time of the applied signal, that is why the state variable moves horizontally within the hysteron map. This is an approximation. Equations 4.1 and 4.3 define the *Memdiode* as a memristive system. In order to have a better picture of the model overall behavior, Fig. 4.2 shows the influence of the model

parameters on the I–V characteristics [177].

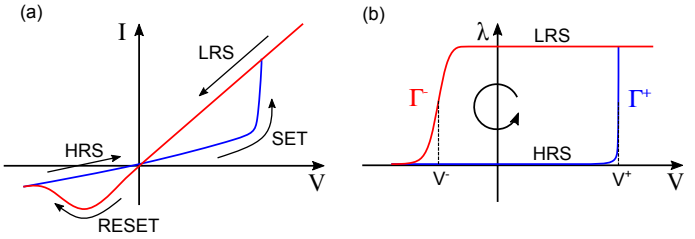

Figure 4.1: (a) Schematic I–V characteristic curve. (b) Hysteron model for the internal state variable $\lambda \in [0,1]$.

The input signal is sinusoidal with amplitude 3.5 V and angular frequency 2π rad/s. As it can be seen in Fig. 4.2 (a) the threshold voltages determine the value at which the transitions occur.

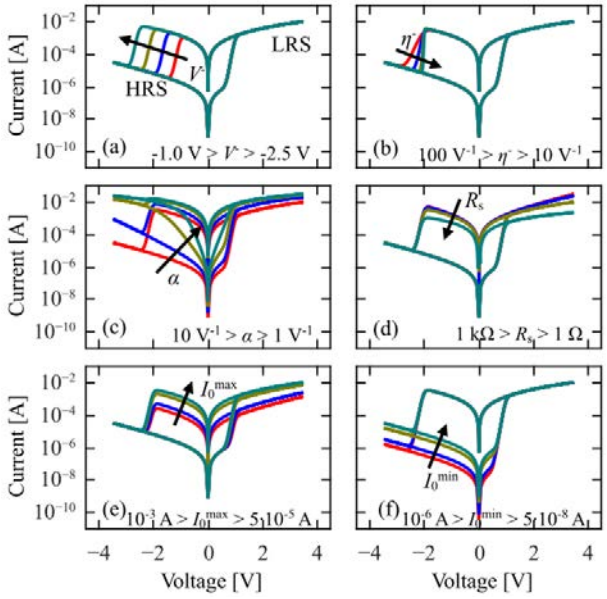

Figure 4.2: Influence of parameters on the I–V characteristic curves. (a) and (b) show the influence of the threshold potential and the transition rate, respectively. (c) and (d) depict the effect of α and R_S. (e) and (f) show the impact of the maximum and minimum current amplitude factor. Arrows indicate the direction of growth of the parameter. The model parameters employed in these simulations are: V^+ = 1 V, V^- = -2 V, η^+ = 20 V^{-1}, η^- = 20 V^{-1}, I_{min} = 10^{-6} A, I_{max} = 10^{-3} A, α = 3 V^{-1}, R_{min} = 100 Ω, and R_{max} = 1010 Ω [177].

The rate of these transitions is given by $\eta^{\pm}$ as shown in Fig. 4.2 (b). The parameter α, which is related to the physical conduction mechanism assumed (Schottky, tunneling,

quantum point-contact, etc.), tunes the non-linear response of the device (see Fig. 4.2 (c)). The series resistor R_S provides a minimum resistance value further influencing the LRS as depicted in Fig. 4.2 (d). Figures 4.2 (e) and 4.2 (f) show how I_{max} and I_{min} modulate the high- and low-conductive states [177].

4.1.2 Implementation in LTSPICE

In this Section, the main features of the model and its implementation in LTSPICE will be presented. Figure 4.3 (a) illustrates the 1T–1R configuration. Notice that the 1R configuration case has a similar implementation replacing the transistor by a compliance box. Concerning the transistor characteristics, a function-fit model was used for simulation purposes. The circuit schematic for the RS element is shown in Fig. 4.3 (b). The two ports PLUS and MINUS represent the positive and negative terminals of the memristive device, respectively. The current source G_{mem} produces a current given by Eq. 4.1 taking into account the potential drop across PLUS and MINUS. The value of the internal state variable λ, is described by the potential across the capacitor C_L. Note that λ is adimensional, and it is used in LTSPICE to store the memory state. Resistor R_{max} accounts for the non-ideal behavior of the current source and it is necessary to overcome iteration problems and divide-by-zero errors when trying to combine more than one *Memdiode* in an electric circuit.

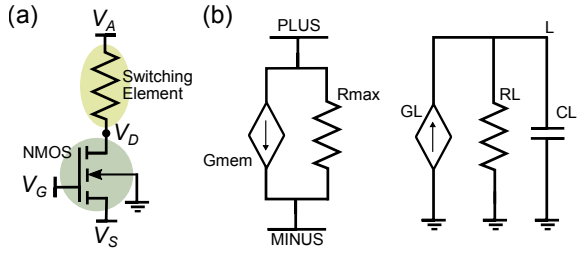

Figure 4.3: (a) 1T–1R configuration. (b) SPICE circuit schematic. Current source G_{mem} drives the I–V response, while the evolution of the internal state λ, equivalent to L, is solved by means of a RC circuit.

Notice that, alternatively, it is also possible to invert Eq. 4.1 and design a subcircuit comprising a voltage source driven by the current through the device. The rightmost circuit corresponds to the memory state represented by the hysteron, implemented by means of the current source G_L and a parallel RC circuit. The circuit cutoff frequency is given by the inverse of the characteristic time $\tau = R_L \cdot C_L$. The output of the current source G_L is set equal to Eq. 4.3 divided by the value of R_L. In this way, for input frequencies much

lower than the cutoff frequency, the RC-output voltage follows the input-signal absolute magnitude.

Next the code of the subcircuit is presented. Figure 4.4 shows the device script and input protocol applied to the 1T–1R structure shown in Fig. 4.3 (a).

```
* Resistive Switching device SPICE model
   .subckt res_switch PLUS MINUS L
** Block 1 - Model parameters **
* vp/vm: plus/minus threshold
* np/nm: plus/minus transition rate
* iset/ires: I0_set and I0_res
* aset/ires: alpha_set and alpha_res
* rset/rres: Rs_set and Rs_res
* I0: initial condition
   .params vp=0.84    np=235      vm= -0.57
   + nm=7.23          I0=0
   + iset=7.96e-04    aset=0.66   rset=6.36
   + ires=1.03e-06    ares=1.75   rres=2768
* Auxiliary parameters
* Rl: R_lambda
* Cl: C_lambda
* Rm: R_max
   .params Rl=1       Cl=1e-4     Rm=1e10

** Block 2 - Declare functions **
* gp/gm: plus/minus ridge function
* w: Lambert W function
* I0: current amplitude factor
* a: alpha parameter
* Rs: series resistance
   .func gp(V)=1/(1+exp(-np*(V-vp)))
   .func gm(V)=1/(1+exp(-nm*(V-vm)))
   .func w(x)=log(1+x)*(1-
(log(1+log(1+x)))/(2+log(1+x)))
   .func I0(l)=iset*l+ires*(1-l)
   .func a(l)=aset*l+ares*(1-l)
   .func Rs(l)=rset*l+rres*(1-l)

** Block 3 - Current source - state variable **
   Gl 0 L value={min(gm(V(PLUS,MINUS)),
max(gp(V(PLUS,MINUS)),V(L)))}
   R L 0 {Rl}
   C L 0 {Cl}
   .ic V(aux)=10
** Block 4 - Current source - memristor **
   Gmem PLUS MINUS value={(sgn(V(PLUS,MINUS))*
(1/(a(V(L))*Rs(V(L)))*w(a(V(L))*Rs(V(L))*I0(V(L))*
exp(a(V(L))*(abs(V(PLUS,MINUS))+Rs(V(L))*
I0(V(L)))))-I0(V(L))))}
   Rmax PLUS MINUS {Rm}
   .ends res_switch
```

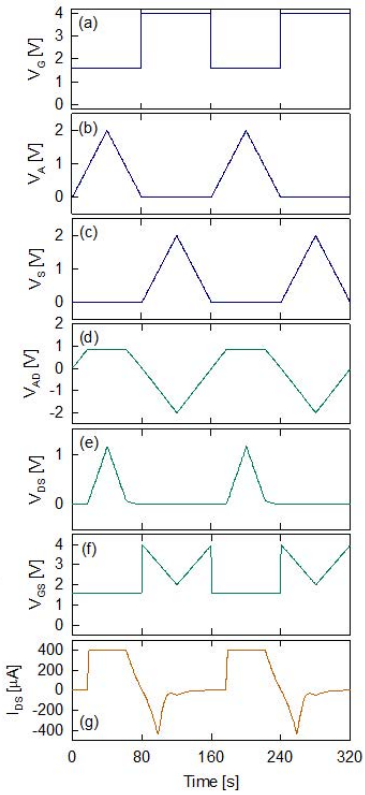

Figure 4.4: Left side: SPICE model code. Right side: (a), (b), and (c) show the applied voltages corresponding to nodes G, A and S. (d), (e), and (f) are the voltage drops across the switching element (V_{AD}), the drain-source nodes (V_{DS}), and the gate-source nodes (V_{GS}), respectively. (g) shows the current flowing through the switching element [180].

The gate voltage is shown in Fig. 4.4 (a), the voltage corresponding to terminal A is depicted in Fig. 4.4 (b), and the source voltage in Fig. 4.4 (c). During the set process, the source terminal is fixed to ground, while a positive sweeping voltage is applied to terminal A. The limiting current is set by the gate voltage which, for this purpose, must be larger than the transistor threshold voltage V_{th} as shown in Fig. 4.4 (f). Figure 4.4 (g) shows the current flowing through the switching element. As it can be seen, when the current reaches the limit value (in this particular case $I_{DS} = 400\mu A$), the voltage drops across the drain and

source nodes Fig. 4.4 (e) increases, while the voltage across the switching element remains constant (Fig. 4.4 (d)). The reset process is carried out as follows: the voltage in terminal A is now grounded and the sweeping signal (positive) is applied to the transistor source terminal. During this procedure, the gate voltage is such that the voltage difference between the gate and source terminals is positive [180].

As an example of the powerful of the model, the experimental results regarding the characteristic curve of the 1T–1R structure are shown in Fig. 4.5 (a). Four different compliance currents were considered (100, 200, 300 and 400 μA) by changing the gate voltage during the set procedure. As it can be seen, there are stable set transitions and the slopes related to the LRS show a clear dependence with the limiting current. The Figure also presents numerical results where the model parameters were obtained by fitting the experimental data corresponding for the cycle limited to 400 μA. Remarkably, despite having used the same set of parameters in the four cycles, there is good agreement between simulations and experiments. Figure 4.5 (b) shows the evolution of the internal state λ as a function of the compliance current. It can be seen that λ reaches different maximum values depending on the compliance current. More channels are activated as the damage caused to the device increases [177].

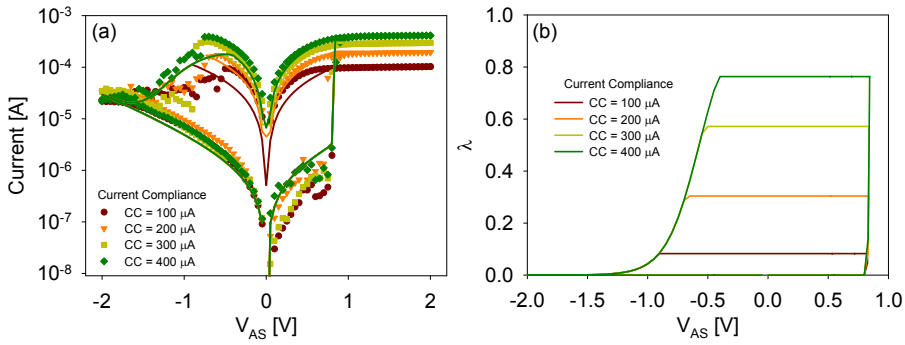

Figure 4.5: Experimental and SPICE results. (a) shows the I–V characteristics of the 1T–1R configuration under different CC. Symbols stand for experimental data while solid lines stand for numerical results. (b) shows the evolution of the internal state λ for the considered limiting currents. The model parameters employed are: I_{max} = 796 μA, I_{min} = 1.03 μA, α_{max} = 0.66 V^{-1}, α_{min} = 1.75 V^{-1}, R_{max} = 6.36 Ω, R_{min} = 2768 Ω, V^{+} = 0.84 V, V^{-} = 0.57 V, η^{+} = 235 V^{-1}, η^{-} = 7.23 V^{-1}, kw/l = 80 μAV^{-2}, and V_{th} = 1.5 V.

The model described above is a static model which does not take into account the temporal behavior of the device. In that concern, the connection between the switching voltages with the RR investigated in the previous Chapter were implemented in the new model ver-

sion. Set and reset voltages increase with the RR according to a logarithmic rule which has been initially linked to a hysteron shift. Figure 4.6 (a) shows the simulated hysterons as a function of RR. To implement the RR effect is enough to add a $V^{\pm}$ parameter by means of a LTSPICE function which varies logarithmically with the derivative from the voltage with respect to the time. Figure 4.6 (b) shows the simulated I–V curves. Importantly, the simulation results were not optimized since the transistor/compliance action was not taken into account for this exercise. As it can be seen, the proposed model was able to qualitatively reproduce the results shown in the experimental Section, but the model needed to be improved in order to deal with arbitrary input signals.

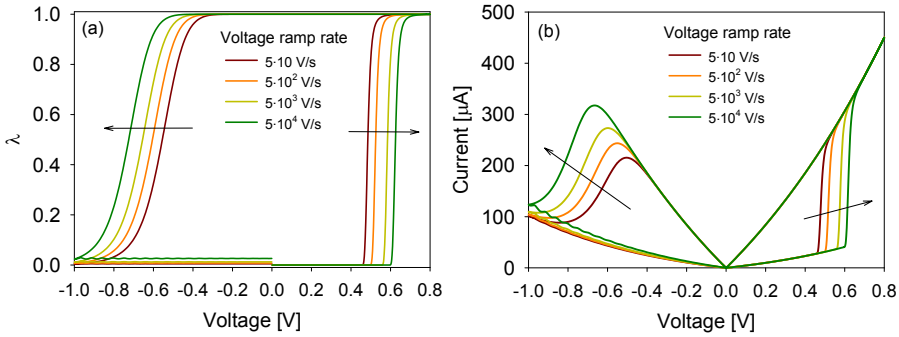

Figure 4.6: (a) Simulated memory map (hysteron) as a function of the applied voltage. (b) Simulated I-V characteristics for different RR values. Model parameters employed to simulate the curves shown are: R_{max} = R_{min} = 100 Ω, α_{max} = 1 V^{-1}, α_{min} = 1.49 V^{-1}, I_{max} = 4·10^{-4} A, I_{min} = 2.85·10^{-5} A, η^{+} = 80 V^{-1}, η^{-} = 10 V^{-1}.

In the case of the static behavior it has been demonstrated that the *Memdiode* can fit accurately the experimental data [177, 181–183]. However, the memory equation needs to be modified considering what was found in the previous Sections in order to account for the temporal behavior (progressive evolution and frequency effects).

4.2 Proposed modifications to the Memdiode model

In order to develop a more general model that includes the time behavior some considerations must be taken into account first. The electron transport equation 4.1 holds unaltered, however $I_0(\lambda)$ is now expressed as:

$$I_0(\lambda) = \left(\frac{1-\lambda}{2}\right) \cdot I_{min} + \left(\frac{1+\lambda}{2}\right) \cdot I_{max} \tag{4.5}$$

where I_{max} and I_{min} are the maximum and minimum values of I_0, respectively. Similar expressions can be used for $\alpha(\lambda)$ and $R_S(\lambda)$ as follows:

$$\alpha(\lambda) = \left(\frac{1-\lambda}{2}\right) \cdot \alpha_{min} + \left(\frac{1+\lambda}{2}\right) \cdot \alpha_{max} \tag{4.6}$$

$$R_S(\lambda) = \left(\frac{1-\lambda}{2}\right) \cdot R_{min} + \left(\frac{1+\lambda}{2}\right) \cdot R_{max} \tag{4.7}$$

In order to obtain the equation that describes the memory state of the device we will consider a first order differential equation for the generation of defects, conductive channels, etc., as:

$$\frac{d\lambda}{dt} = \frac{(1-\lambda)}{\tau} \tag{4.8}$$

Other expressions can be used as well. Equation 4.8 corresponds to a self-saturation process with characteristic time τ. The initial state is:

$$\lambda(t=0) = \lambda_0 \tag{4.9}$$

Regardless of the initial state, $\lambda = 1$ is a fixed point (attractor) of the dynamical system for infinite time. The solution to equation 4.8 is therefore:

$$\lambda(t) = (\lambda_0 - 1)\exp(-t/\tau) + 1 \tag{4.10}$$

Similarly to 4.8, for the destruction of defects, channels, etc., we will consider a first order differential equation that in this case reads:

$$\frac{d\lambda}{dt} = -\frac{(1+\lambda)}{\tau} \tag{4.11}$$

and whose solution is:

$$\lambda(t) = (\lambda_0 + 1)\exp(-t/\tau) - 1 \tag{4.12}$$

Notice that now λ runs between -1 and 1, and not from 0 and 1 as in previous approaches [153, 177]. This simplifies the description of the hysteron into a single compact expression:

$$\lambda(t) = [\lambda_0 - sgn(V(t))]\exp(-t/\tau) + sgn(V(t)) \tag{4.13}$$

For the simulator, a discretized version of 4.13 is required so that the initial state acts as the previous state (memory map):

$$\lambda_t = [\lambda_{t-1} - sgn(V_t)] \exp\left(-\Delta t/\tau\right) + sgn(V_t) \tag{4.14}$$

This latest expression substitutes the hysteretic operator used in previous versions of the model. Notice that for $\tau \gg \Delta t$, Eq. 4.3 is recovered. One relevant point is that the integrated solution is discretized, not the differential equation as in previous memristive models. Expression 4.13 is used to control the variable λ in 4.5, 4.6 and 4.7 which in turn controls the current via expression 4.1.

As it was reported in papers **MER17** and **EDL18**, experimental data confirmed that the best fitting result for the characteristic time of the switching process corresponds to the exponential acceleration model (see Chapter 3, Section 3.2.2.2). Notice that other acceleration models do not provide good fitting results. Then we can write τ as a function of the applied voltage as:

$$\tau = \tau_0 \exp(-\gamma V) \tag{4.15}$$

With this new approach V^+, V^-, η^+ and η^- are replaced by τ_0 and γ.

4.2.1 Implementation in LTSPICE

The model described above was implemented in LTSPICE as a delay equation that replaces the recursive operator for hysteresis used in previous approaches. Now the parallel capacitor required for storing the information is eliminated. Full continuity of derivatives is achieved (except at the turning points). The code is simplified since the series resistance is placed outside the gray-box model (see Fig. 4.7). Notice that most of the lines are comment lines (green color). Importantly, the proposed model has been improved by considering γ and τ_0 parameters different for set (γ_{SET}, τ_{SET}) and reset (γ_{RESET}, τ_{RESET}) processes, since depending of the sample the physics associated with the transitions can be different.

Remarkably, the new approach significantly simplifies previous versions of the *Memdiode*. Figure 4.7 (b) illustrates the circuit model considered for simulations. It is worth mentioning that in the current model, the delay parameter *del*, which is used to calculate the value λ_{t-1} in Eq. 4.14, is a critical parameter of the model. Figure 4.8 shows different I–V curves simulated for different *del* values. As it can be seen for *del* = 0.1 s and *del* = 0.01 s the time step used is too large to represent the I–V response. For small values of *del*, the

results do not longer depend on *del* so caution should be exercised with the selection of this parameter. The maximum frequency of the input signal determines the *del* value.

```
* Resistive switching device LTSpice model
.subckt mdtime + -H
** Block 1 -Model parameters **
* imax/imin: I0_LRS and I0_HRS
* amax/amin: alpha_LRS and alpha_HRS
* gset/greset: Voltage acceleration parameter
* tset/treset: Effective time parameter
* del: Delay parameter
.params
+ imax=1e-4 amax=4
+ imin=3e-5 amin=1
+ del=1e-3
+ greset=100 gset=50
+ treset=5e+19 tset=1e+7
** Block 2 -Declare functions **
* I0: Current amplitude factor
* aa: Alpha factor
* D: Delay function
* gma and tau:Select process,set or reset
* ID: Current function
* t: Characteristic time function
.func I0(x) = imax*(1+x)/2+imin*(1-x)/2
.func aa(x) = amax*(1+x)/2+amin*(1-x)/2
.func D(x) = delay(x,del)
.func gma(x,y) = if(sgn(x)>=0,gset, greset*(1+y)/2+gset*(1-y)/2)
.func tau(x,y) = if(sgn(x)>=0, tset, treset)
.func ID(x,y)= sgn(x)*I0(y)*(exp(aa(y)*abs(x))-1)
.func t(x,y) = tau(x,y)*exp(-gma(x,y)*abs(x))
** Block 3 -Current source -state variable **
* Initial condition
.ic V(H)=-1
BH 0 H I=(D(V(H,0))-sgn(V(+,-)))*exp(-del/t(V(+,-),V(H,0)))+sgn(V(+,-)) Rpar=1
BR + -I=ID(V(+,-),V(H,0)) Rpar=1e+12
.ends mdtime
```

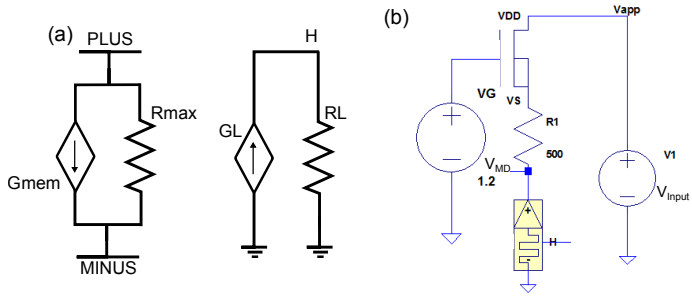

Figure 4.7: LTSPICE model code and schematic of the LTSPICE compact model. (a) The *Memdiode* device consist of one current sources G_{mem} and one resistor R_{max}. The current source is driven by the voltage potential across PLUS-MINUS and the internal potential H. The latter is the voltage drop produced by the current source G_L across R_L. (b) LTSPICE schematic used for fitting the experimental data. The NMOS transistor was developed with a sub-circuit which is able to replicate the experimental $I_{DS} - V_{DS}$ curves.

In order to have a more complete picture of the overall behavior of the model, the figures below show the influence of the new model parameters on the I–V characteristics for a typical 1T–1R structure. The input signal is the experimental voltage ramp used to generate the experimental data. As it can be seen τ_{RESET} and τ_{SET} determine the values at which the transitions occur (see Fig. 4.9). The transition rate is given by the γ_{RESET} and γ_{SET} as shown in Fig. 4.10.

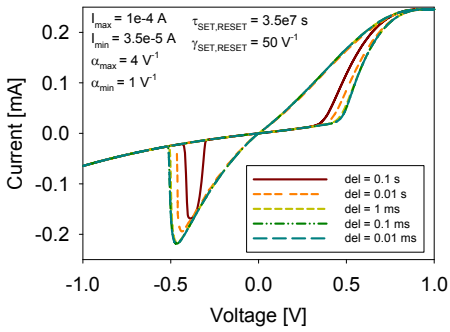

Figure 4.8: Simulated I–V characteristics for different *del* values. A *del* minimum of 10^{-3} s is needed to get adequate I–V curves. R_S = 500 Ω.

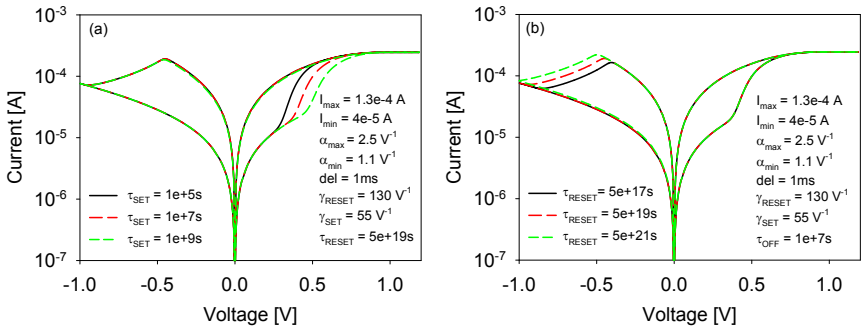

Figure 4.9: Influence of parameters on the I–V curves where it is show the influence of the (a) τ_{SET} and (b) τ_{RESET} parameters. R_S = 500 Ω.

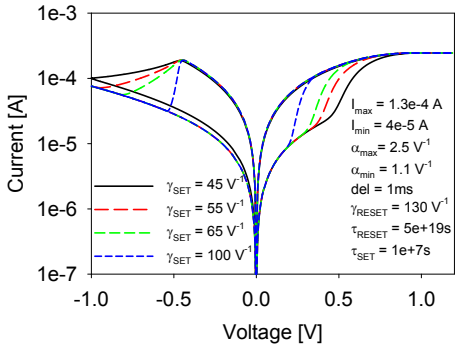

Figure 4.10: Influence of parameters on the I–V curves where it is show the influence of the parameter γ_{SET} and γ_{RESET} on the transition rate. R_S = 500 Ω.

4.3 Simulations of 1R MIM-based devices

Firstly, the modifications introduced to the *Memdiode* model discussed in the previous Section are used now to model the 1R MIM structures discussed in Chapter 3. The experimental and model results are shown in Fig. 4.11 (a) and (b). The results are plotted in linear and log axes, respectively. The experimental data were measured with a RR = 0.1 V/s. The LTSPICE schematic and model used are shown in Fig. 4.7. Notice that the compliance box was not required and that instead a series resistance of 110 Ω was assumed. The model exhibits good agreement with the experimental data yet the reset process requires an extra modification. This feature will be explained later.

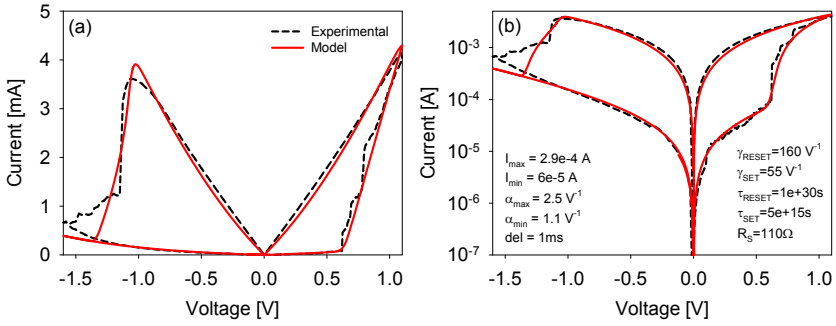

Figure 4.11: Experimental I–V characteristics (RR = 0.1 V/s) and simulated I–V characteristics in (a) linear-linear and (b) log-linear representation.

Second, though there are no experimental data available at the moment of writing this document, we are going to show one important characteristic contemplated by the model. Fig. 4.12 (a) and (b) show the response of the *Memdiode* driven by a voltage source in linear and log representations, respectively, where three different amplitudes are considered for the reset process. The maximum amplitude values are indicated in the figure. The model curves exhibit well-defined intermediate conductive states, that is, minor I–V loops arising from partial transitions of the state variable. In addition, as illustrated in Fig. 4.13 (a) and (b), the model complies with the experimental observation that higher RR leads to higher set and reset voltages.

Next, experimental data presented in Chapter 3 (in 1R structure Section) will be modeled. In this case, the reset process will be exclusively considered. As it was commented above, the reset process requires a correction in the model so as to achieve good agreement with the experimental data. Importantly, this correction is particular to this set of devices and is not a general feature of the model.

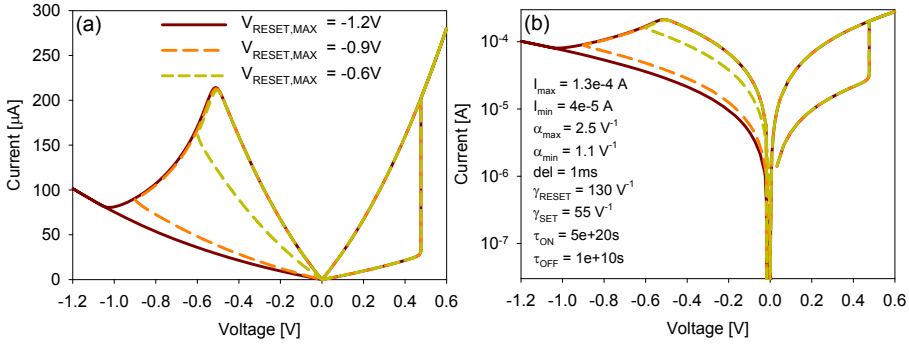

Figure 4.12: Experimental I–V characteristics (RR = 10 V/s) and simulated I–V characteristics in (a) linear-linear and (b) log-linear representation. R_S = 500 Ω.

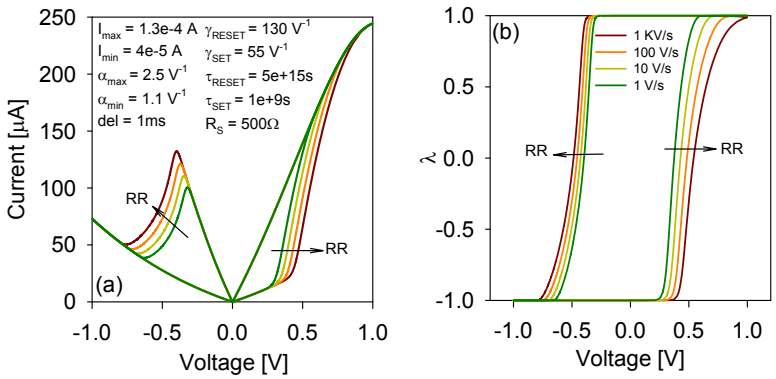

Figure 4.13: (a) Simulated I–V characteristics and (b) simulated memory map as a function of the applied voltage for different RR.

Figure 4.14 shows the simulated I–V characteristics for different RR values. Some considerations have been taken into account in order to achieve good agreement between model and experimental results. Firstly, the initial memory state must be initiated at different values. As it was studied in the previous Chapter, RR affects the degradation state of the device (in LRS), so that higher RR has been initiated at memory states as a function of the RR as follow:

$$\lambda(RR) = 0.75 \cdot ln(RR) + 0.0184 \tag{4.16}$$

As it was investigated in **EDL18**, γ_{RESET} depends inversely on the gap width ($t_{\text{GAP}} \approx 1/\gamma$), which can also be assumed proportional to the memory state. For this reason, the

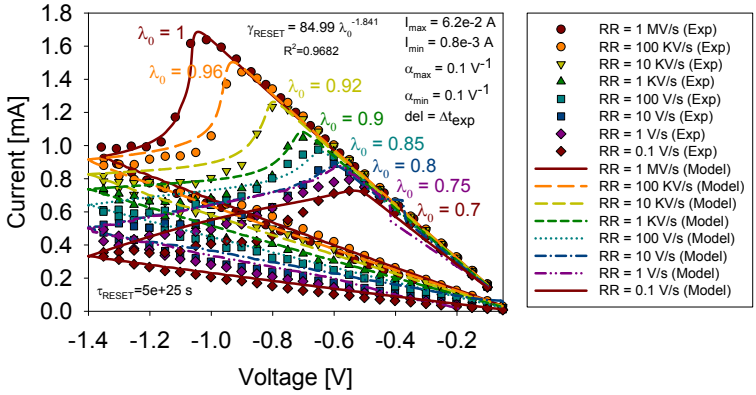

Figure 4.14: Measured I–V characteristics during reset process for different pulsed RR values and their simulated I–V characteristics. The experimental results correspond to the CNM devices investigated in Chapter 3.

following relationship is considered:

$$\gamma_{\text{RESET}} = 84.99 \cdot \lambda_0^{-1.84} \tag{4.17}$$

The LRS and the reset starting point can be well fitted to the experimental data. In order to get a good agreement with the experimental results a sigmoidal function similar to Eq. 4.4 needs to be implemented for the complete reset process.

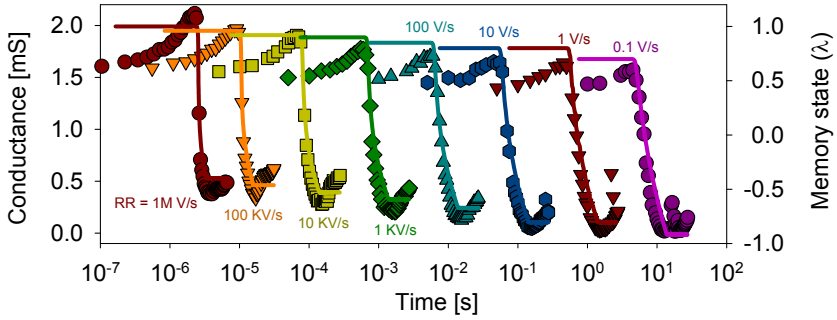

Figure 4.15: Measured $G-t$ conductance at -0.1 V during reset process for different pulsed RR values and their simulated I–V characteristics.

In our case, due to the wide range of RR considered, it is not possible to fit the whole range of experimental data represented. The best fitting results are obtained for RR from 1 MV/s to 100 V/s. Finally, the experimental and modeled conductance response as a function

of time is represented in Fig. 4.15. Since in the low bias regime, from 4.1, the current reads $I = I_0 \alpha V$ with $I_0 = G/\alpha$ where α is constant. Then, a comparison between the conductance at -0.1 V and the memory state vs time for different pulsed RR values can be done. Figure 4.15 shows the memory state in close time-agreement with the conductance.

4.4 Simulations of 1T-1R MIM-based devices

In this Section, we present model results for the 1T–1R MIM structures described in Chapter 3. The I–V modeled responses are illustrated in Fig. 4.16 (a) and (b). The results are plotted in linear and log axes, respectively. Notice the good agreement between experiment and model results.

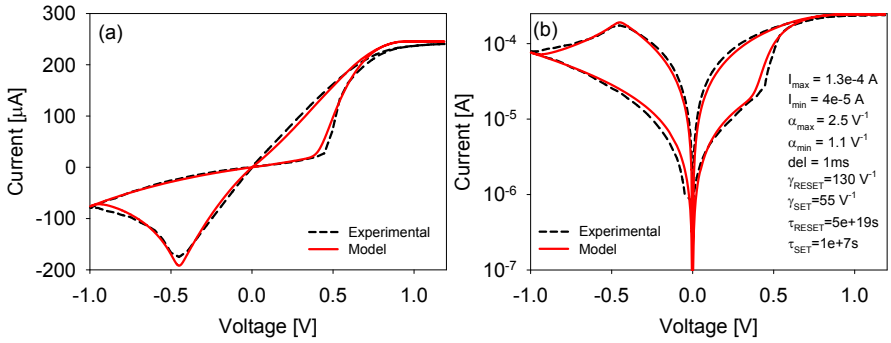

Figure 4.16: Experimental I–V characteristics (RR = 50 V/s) and simulated I–V characteristics in (a) linear-linear and (b) log-linear representation. R_S = 500 Ω.

Figure 4.17 shows experimental (symbols) and model results (lines) for different RR values during the set process. The experimental results correspond to LETI technology investigated in Chapter 3. The model responds in the same way for CVS experiments and train of pulses. To illustrate this point, Figure 4.18 shows the current, the simulated memory map and the results for a train of pulses with the same amplitude and time duration. Notice the progressive increase of the current and the memory state with the accumulation of pulses. This behavior is what is expected for a memristive behavior (intermediate memory states) required for neuromorphic systems. Again, the same results can be obtained with just a single pulse with equal characteristics. Pulsed experiments with different DUTY cycle have not been performed yet due to this reason.

Figure 4.18 shows the simulated memory map and the effects for different amplitudes of a train of pulses. Since the memory function 4.13 follows an exponential dependence,

the model needs to be improved in order to take into account abrupt transitions to LRS. For the LETI devices, the effect of a sequence of pulses is a direct transition to the LRS state. To solve this problem, two minor changes were introduced in the LTSPICE code. The `gma` function which accounts for accelerated process and it is expressed by

```
.func gma(x)= greset*1/(1+exp(-200*(time-t63(x))))
```

and the `t63` function which indicates the set time (based on the previous experimental results). `t63` is expressed as:

```
.func t63(x) = 4.39*10**(7)*exp(-47.59*x)
```

With these modifications, a comparison between the model and the experimental results is illustrated in Fig. 4.19. Notice the good agreement between both results.

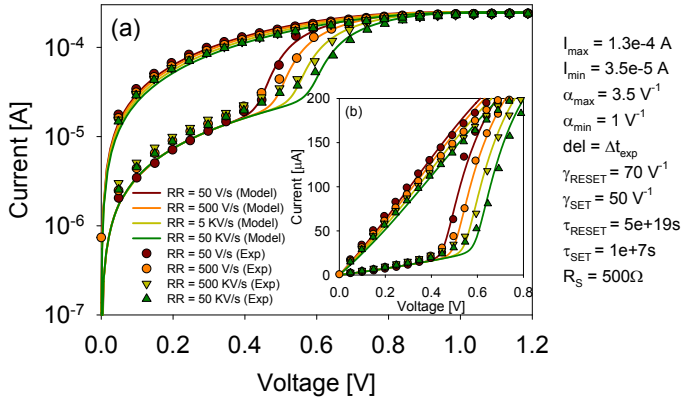

Figure 4.17: Simulated I–V characteristics in log-lin (a) and lin-lin (b) plots for different RR values. The simulations are in agreement with the experimental results.

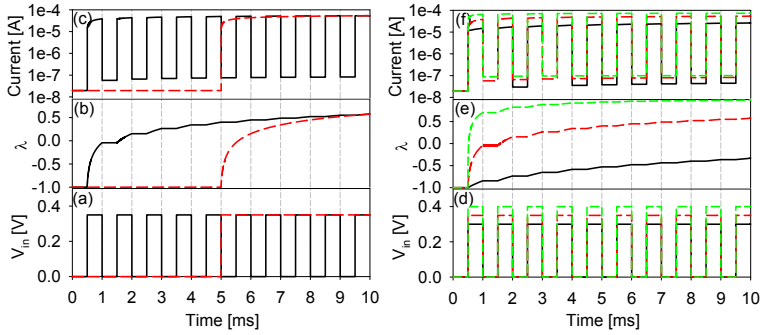

Figure 4.18: (a) Input voltage as a function of time; trains of pulses (solid line black) and constant voltage stress (dash line red) at 0.3 V. (b) The memory state of the device and (c) the current are plotted as a function of time. (d) Trains of pulses with different amplitudes 0.30 V (black), 0.35 V (red) and 0.40 V (green).(e) The memory state of the device and (f) the current are plotted as a function of time.

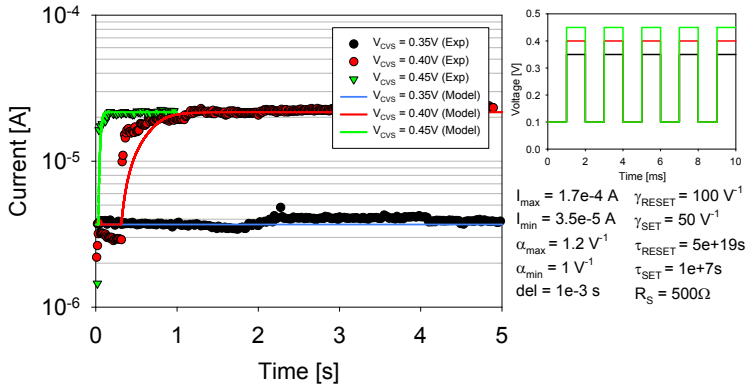

Figure 4.19: Simulated I–t characteristics for different CVS voltages. The modeled data are in reasonable agreement with the experimental results.

4.5 Conclusions

In this Chapter the following conclusions can be withdraw:

- A compact model for the I–V characteristic of memristive devices based on a diode-like structure with memory properties and which is able to account for the progressive evolution of the memory state as well as the effect of the input signal frequency has been developed.
- This new time-dependent version is able to deal with arbitrary input signals and it is simple enough to be easily implemented in any programming language. In our case we have chosen the free and popular simulation software LTSPICE but any other language is feasible.
- The model has been fitted to data measured on 1R and 1T–1R devices fabricated at the IMB-CNM (Spain) and the LETI-CEA (France), respectively. The model is able to reproduce the experimental results in several bipolar RS devices and under different experimental conditions, RVS, CVS or PULSED.

Conclusions

Filamentary-based resistive switching devices represent a fascinating emerging class of electronic devices, with great potential in future memories, logic gates and artificial neural networks applications. Based on ion migration and solid state electrochemical reactions at the nanoscale, their study is an exiting challenge for the scientific community. In this way, Breakdown and Resistive Switching constitute two of the most relevant phenomena for the improvement of the current electronic technology. These two phenomena represent the backbone of this work.

This Thesis dealt with the electrical characterization and modeling of filamentary conduction in HfO_2- and Al_2O_3/HfO_2-based MIS and MIM devices. In these devices, the filament spanning the dielectric film is generated by the action of electrical stress. Sometimes, a partial recovery can be achieved as in the case of resistive RAMs (ReRAMs). In other cases, once a breakdown occurs, the device remains in this state permanently. This is the case of one-time-programmable (OTP) memories. In both cases, the phenomenon can be used to store single or multibit information in the form of a change of resistance.

The reported document was divided into three parts. In the first part, Chapter 2, our focus of attention were the MIS structures, where Ni/20nm-HfO_2/n^+-Si devices with three different thicknesses (5, 10 and 20 nm) were electrical characterized and modeled. We analyzed the dependence of the filament formation on the bias polarity, its thermal stability, and the self-rectifying effect. Subsequently, the generation of multiple BD events in Al_2O_3/HfO_2 nanolaminates subjected to constant electrical stress was studied. A simple circuital approach to determine the stress time required to set the device to a given current level was proposed. The model consists in a number of parallel and series resistances which are progressively turned on as a consequence of degradation. This is of primarily importance for the programming operation of multilevel NVM devices based on the creation of multiple uncorrelated breakdown paths. In addition, a deterministic function-fit model for the arrival rate of conducting filaments was reported.

The second part, Chapter 3, was dedicated to the electrical characterization of the TiN/Ti/HfO_2-based MIM structures. Concretely, 1R and 1T–1R structures. Both Sections focused on the RS characterization applying ultra-fast pulsed trains. In first place and concerning to TiN/Ti/HfO_2(10 nm)/W 1R

structures, the investigations pay special attention to the reset process. Experimental data supporting a thermal and field activated reset mechanism was presented. The attention was also placed on the capability of the device to modulate its conductance value. This result points out the potential of the studied devices for multilevel applications. In connection with the 1T–1R structures, Ti/HfO_2(10nm)/TiN structures were investigated. In this case, the switching voltage and time statistics of the filamentary conductive paths were analyzed by means of oxide failure methods. The obtained results seem to indicate a common physical origin for both set and reset transitions. From an oxide reliability viewpoint, constant and ramped voltage stress experiments provide strong support to the so-called E-model, which was shown to be in line with current theories relating the reversibility of the conduction states in ReRAM devices with ionic drift and ultimately with Kramers' escape rate theory. Second order effects in memristors were also investigated by means of pulsed experiments.

In the third part, Chapter 4, a compact model for the I–V characteristics of ReRAM devices was presented. The original version of the model was improved considering the detailed characterization of the devices carried out in Chapter 3. In the current version, the *Memdiode* model is able to deal with the progressive evolution of the memory state as well as with the effect of the input signal frequency. The model is still able to work with arbitrary input signals. The model was implemented in LTSPICE and was fitted to data measured on 1R and 1T–1R devices. The results are very promising due to its capability to reproduce experimental results.

In conclusions, this Thesis provides a deep insight into the physics of the switching and conduction mechanism of filamentary HfO_2-based structures. Most of the results included in this Thesis have been published in international journals and conferences, which gives strong support to the ideas and developments presented herein.

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Appendix I:
Compendium of publications included in this Thesis

ARTICLE **MEE15**

Temperature and polarity dependence of the switching behavior of Ni/HfO_2-based RRAM devices

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Temperature and polarity dependence of the switching behavior of Ni/HfO_2-based RRAM devices

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ABSTRACT

In this work, the impact of temperature and switching polarity on the stability and variability of Ni/HfO_2-based RRAM structures has been investigated for temperatures ranging from −40 °C to 175 °C. Special attention is given to the analysis of the variability and thermal behavior of the reset currents and voltages. The experimental results show that the temperature plays a key role in the reset operation, owing to the self-accelerated dissolution process of the conductive filament. Furthermore, for both polarities, a larger instability of the on-state current at high temperatures is evidenced.

1. Introduction

Filamentary-type resistive random access memories (RRAM) are considered the most promising candidate to replace flash technology in next-generation and highly-scalable non-volatile memory devices. However, switching variability and device reliability are two major concerns in this emerging technology. These handicaps are connected to the fluctuations of the switching parameters due to the random nature of conductive filament formation and dissolution through percolation processes. The occurrence of these fluctuations in memory applications can cause severe operation or read errors [1]. Hence, for the industrial application of Ni/HfO_2-based RRAM technology, it is crucial to keep a good control of the reversible conductive filament (CF) formation, and to obtain a better understanding of the key mechanisms involved in device stability. While progress has been made in understanding the transport mechanisms controlling the switching phenomenon [2–6], little is known on the thermal stability of the conductive paths and the polarity and temperature dependence of switching variability. The objective of this paper is to analyze the effect of temperature and polarity on the electrical behavior of Ni/HfO_2-based resistive switching structures. Besides the switching variability, attention is also focused on the electrical and thermal stability of the conductive filaments.

2. Experimental

The Ni/HfO_2/Si devices were fabricated on (100) n-type CZ silicon wafers with resistivity between 0.007 Ω·cm and 0.013 Ω cm following a field isolated MIS process. The 20 nm-thick HfO_2 layer was deposited by atomic layer deposition (ALD) using TDMAH and H_2O as precursors. The 200 nm-thick Ni electrode was deposited by magnetron sputtering. The resulting device structures are square cells of $5 \times 5\ \mu m^2$. More detailed information about the process flow can be found in Ref. [7].

The current–voltage (I–V) measurements were performed using a HP-4155B semiconductor parameter analyzer at temperatures from −40 °C to 175 °C. The voltage was applied to the top Ni electrode, while the Si substrate was grounded. In order to evaluate the cycle-to-cycle variability, numerous cycles and measurements need to be assessed. For this purpose, a software tool has been developed and implemented in Matlab to control the instrumentation via GPIB (General Purpose Instrumentation Bus) and to smartly detect the set and reset currents.

3. Results and discussion

Fig. 1 shows a typical unipolar resistive switching behavior for both switching polarities in the studied Ni/HfO_2-based structures. The mechanism responsible for the resistive switching behavior in filamentary RRAM is the formation and partial dissolution of a

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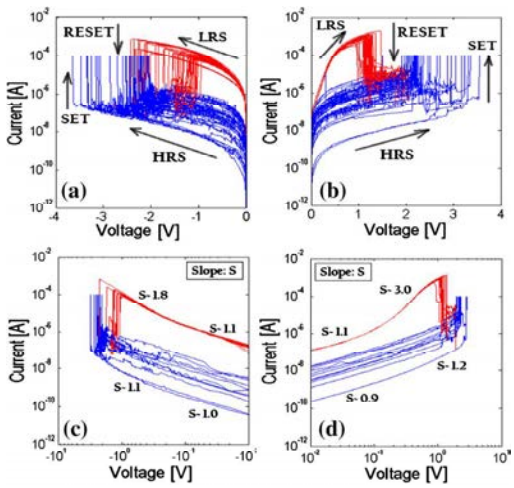

Fig. 1. (a) and -(b) Unipolar resistive switching behavior during successive set and reset cycles for the studied Ni/HfO_2-based RRAM devices with I_C = 100 μA, and their corresponding (c) and -(d) double logarithmic plots.

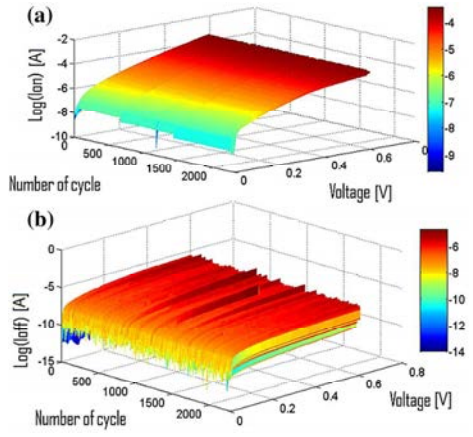

Fig. 2. (a) and -(b) 3-Dimensional plots of I_{on} and I_{off} versus. applied voltage and cycle number corresponding to 2300 cycles of unipolar switching under positive bias with I_C = 100 μA.

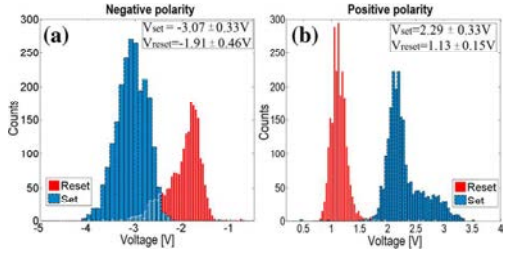

Fig. 3. (a) Histograms of V_{reset} and V_{set} obtained from 2200 cycles of negative switching and (b) 2300 cycles of positive switching at T = 25 °C. The corresponding mean and standard deviation values are also indicated.

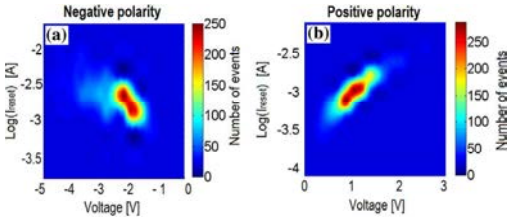

Fig. 4. (a) I_{reset} as a function of V_{reset} corresponding to 2200 cycles under negative voltage ramps and (b) 2300 cycles under positive voltage ramps at T = 25 °C. The color maps indicate the number of events. (For interpretation of the references to colour in this figure legend, the reader is referred to the web version of this article.)

conductive path between the top and bottom electrodes. These nano-filaments are composed of structural and chemical defects, which strongly depend on the material combinations and material properties of the devices. Different physical mechanisms based on electrochemical and thermochemical effects may cause the switching behavior. In Ni/HfO_2-based devices, the resistance switching effect is attributed to the CFs formation owing to oxygen ion drift [2] and subsequent Ni diffusion/migration from the top metal electrode into the dielectric [2,3]. With respect to the CFs dissolution, it can be explained by thermally enhanced diffusion of Ni atoms induced by local joule heating in the CF [4,5]. Note that a compliance current (I_C) during the set process was employed to control the conductive filament strength (size and shape). It should be mentioned that for both switching polarities I_C values between 100 μA and 1 mA showed the lowest cycle-to-cycle variability.

In Fig. 1 it is also observed that the low resistive state (LRS) does not show linear conduction, a result that agrees with a recently published work [6], where the on-state current (I_{on}) was modeled by tunneling-based conduction considering the quantum point contact (QPC) theory for atomic-sized constrictions [8]. In these constrictions, the first quantized sub-band behaves as a potential barrier for the transit of electrons [6,8]. The different slopes in the double logarithmic plots of Fig. 1 indicate different CF configurations and different dominant contributions to the current [6].

Notice that the I_{on}/I_{off} ratio is larger for negative polarity than for positive polarity for voltages lower than $V = |0.5|$ V.

To analyzse the cycle-to-cycle variability associated with the Ni diffusion and migration processes in Ni/HfO_2-based RRAM devices, the stability of the switching parameters during successive measurements is evaluated. Fig. 2 shows the evolution of I_{on} and I_{off} vs. voltage and cycle number for 2300 cycles of positive switching, indicating a significantly larger cycle-to-cycle variability in the high resistive state (HRS) than in the LRS, in the whole voltage range assessed. It should be mentioned that the mean and standard deviation of I_{on} and I_{off} under positive/negative switching at $V = 0.8/-0.8$ V are $I_{on} = 0.49 \pm 0.08$ mA/ $I_{on} = 0.19 \pm 0.06$ mA and $\log_{10}(I_{off}) = -6.24 \pm 0.46$ / $\log_{10}(I_{off}) = -7.54 \pm 0.41$ A. Since in the HRS the partial dissolution of CFs takes place and a physical gap is opened, the observed enhanced variability in the HRS can be attributed to the cycle-to-cycle variations of the gap distances.

Fig 3 shows the histograms of the switching voltages for both polarities and their corresponding mean and standard deviation values.

Furthermore, special attention is given to the study of the reset currents and voltages, which impacts the metallic diffusion from the conductive filament through local joule heating [4,5]. Fig. 4 shows the reset current (I_{reset}) as a function of the reset voltages (V_{reset}) under positive (Fig. 4a) and negative (Fig. 4b) voltage ramps with the color map indicating the number of events. Note that the most probable reset current vs. reset voltage combination is located at $V_{reset} \sim -1.96$ V and $I_{reset} \sim 1.10$ mA for negative

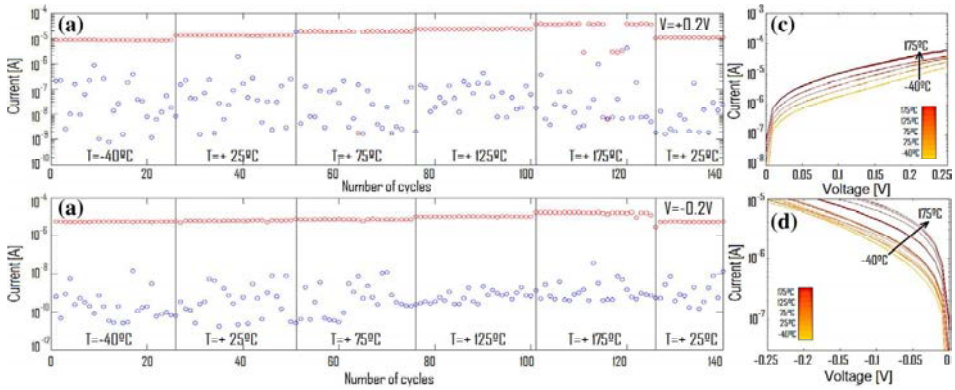

Fig. 5. Evolution of I_{on} and I_{off} at fixed bias during cycling for several temperatures under (a) positive and (b) negative switching, and the obtained I_{on}–V characteristics at the different temperatures (c) and -(d).

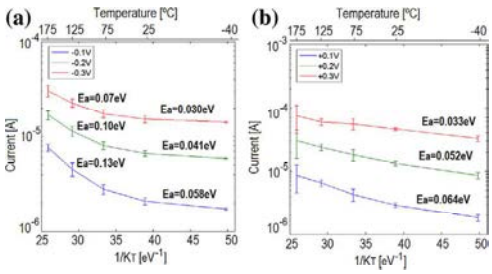

Fig. 6. Arrhenius plots of the I_{on} current for temperature ranging from −40 °C to 175 °C, at fixed bias under (a) negative and (b) positive switching.

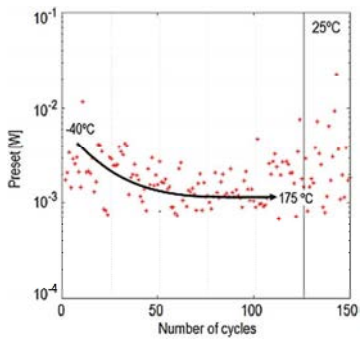

Fig. 7. Evolution P_{reset} during cycling for the studied temperatures.

switching, and in the case of positive switching, the most probable combination is $V_{reset} \sim 1.13$ V and $I_{reset} \sim 1.20$ mA. The different regions observed in the reset plot correspond to different CFs configurations and contributions to the device resistance [6].

In order to evaluate the impact of temperature on the switching stability, 140 successive cycles were measured at five different temperatures. The measurements started at −40 °C, where 25 cycles were firstly performed. After that, every 25 cycles the temperature was raised from 25 °C to 175 °C in 50 °C steps. Subsequently, the temperature was reduced again to 25 °C, and the last 15 cycles were performed. This measurement procedure allowed separating the impact of cycling from thermal effects. Fig. 5 (a) and -(b) shows the thermal evolution of I_{on} and I_{off} at $V = |0.2|$ V. A clear increase of I_{on} with temperature is observed for both switching polarities. This result is in agreement with previous observations for QPC conduction [9,10]. The thermal dependence of the LRS current leads to a significant increase of the I_{on}/I_{off} ratio in the temperature range from −40 °C to 125 °C, being larger for the negative polarity. On the other hand, it is observed that the I_{on} variability is significantly enhanced at 175 °C, while it is reduced once 25 °C is reached again. The observed enhanced I_{on} variability at high temperatures could be attributed to variations in the conductivity, shape, size and length of the conductive filaments. During the set process, an increase of temperature can give rise to an enhanced defect generation rate [11,12], thus influencing the I_{on} variability.

In addition, Fig. 6 shows the Arrhenius plots of I_{on} current for the studied temperatures at fixed bias and their corresponding activation energies (E_a), which have been extracted from the current values obtained during cycling. Notice that E_a decreases as the electric field increases. Moreover, in the case of negative polarity, E_a is found to be temperature dependent, where two different slopes are clearly observed in the temperature ranges ([−40 °C, 75 °C)] and ([75 °C,175 °C)].

On the other hand, the reset power (P_{reset}) decreases with increasing temperature (Fig. 7). This result supports the joule heating model for thermochemical reset, where the reset is achieved once a critical temperature is reached at one point of the CF [5]. According to this model, the critical temperature (T_{crit}) is related to P_{reset}, as $T_{crit} = T_0 + R_{th}P_{reset}$, where T_0 is the ambient temperature and R_{th} is the CF equivalent thermal resistance. Consequently, a decrease of P_{reset} is expected when the temperature increases [13]. This decrease is attributed to the impact of the ambient temperature on the accelerated CF dissolution process.

4. Conclusions

This work analyzes the thermal stability and polarity-dependent switching behavior of unipolar Ni/HfO_2-based devices. A clear increase of I_{on} with temperature is observed for both switching polarities, supporting the model of a filamentary path with a narrow constriction. In the case of the HRS, for all the temperatures assessed, large data dispersion is obtained related to cycle-to-cycle variations of the physical gap distances.

In addition, it is observed that measuring the device at high temperatures significantly enhances the variability in the LRS.

Furthermore, these results provide additional support to the joule heating model for thermochemical reset in Ni/HfO_2-based RRAM devices.

Acknowledgments

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ARTICLE **MEE15B**

Breakdown time statistics of successive failure events in constant voltage-stressed Al_2O_3/ HfO_2 nanolaminates

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Breakdown time statistics of successive failure events in constant voltage-stressed Al_2O_3/HfO_2 nanolaminates

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ABSTRACT

The breakdown time statistics of successive failure events in constant voltage-stressed Al_2O_3/HfO_2 nanolaminates grown by atomic layer deposition (ALD) is investigated. The oxide stack was deposited on a p-type Si substrate and Al was used as the top metal electrode. It is shown that the devices exhibit stepwise current–time characteristics which indicate the formation of multiple leakage current paths spanning the insulating film. It is demonstrated that the arrival rate of the breakdown events can be modeled as a combination of two power-law intensity functions within the framework of a nonhomogeneous Poisson process (NHPP). The change of trend observed during degradation is ascribed to the increasing role played by the series resistance effect in the voltage drop across the nanolaminate. A simple algorithm for calculating the arrival rate of the failure events based on a thinning method is discussed.

1. Introduction

The dielectric breakdown (BD) phenomenon in ALD-grown Al_2O_3/HfO_2 nanolaminates is investigated in this work, with special emphasis on the BD time statistics of successive failure events. The interest in this kind of nanolaminates stems from the possibility of achieving a gate stack that shares the properties of both Al_2O_3 (high conduction band offset from Si, $\phi \approx 2.8$–3.3 eV [1,2]) and HfO_2 (high permittivity oxide, $k \approx 22$ [2]). Remarkably, it has been reported that the electrical characteristics of these films can be engineered to some extent by a proper combination of the individual materials [3]. However, reliability analysis relating the stability of these oxide stacks against long-term electrical stress is still a pending issue. Metal–insulator–semiconductor (MIS) devices were fabricated that exhibit stepwise I–t characteristics when subjected to constant voltage stress (CVS). The steps correspond to BD events that occur randomly in time but which can be described by a deterministic time-dependent arrival rate. Each failure event contributes significantly to the total current in such a way that hundreds of them can be individually characterized by their occurrence time and magnitude of the current jump. Similar jumps, but fewer, detected in the I–V [4] and I–t [5] characteristics of SiO_2 layers in MIS structures were also shown to be related to local BD events. In a previous paper [6], we demonstrated that for the first few events ($\leqslant 10$) the theory of uncorrelated successive BD events could be applied to the same devices investigated here after an appropriate data screening in terms of the initial leakage current. In this work, a different viewpoint of analysis is adopted, interpreting the successive arrival of BD events as a nonhomogeneous Poisson process (NHPP) [7,8]. The final objective of this report is to provide a plausible expression for the process intensity function $\lambda(t)$, *i.e.* the expected number of BD events per unit time, by considering the superposition principle of multiple uncorrelated NHPPs. After determining the functional form of $\lambda(t)$, a simple method for generating the corresponding BD times from a thinned homogeneous Poisson process (HPP) is discussed.

2. Devices and sample path measurements

The devices investigated in this work are MIS capacitors with a 5-layer nanolaminated insulator ($Al_2O_3/HfO_2/Al_2O_3/HfO_2/Al_2O_3$) deposited by ALD onto a p-type Si substrate (0.1–1.4 Ω cm) [3]. A field oxide of 400 nm was grown by thermal oxidation at 1100 °C and windows were opened for the Al_2O_3/HfO_2 stack by photolithography and wet etching. Before deposition, the samples were first cleaned for 10 min with H_2O_2/H_2SO_4 and subsequently for 10 s with HF. The ALD process was performed in 100 cycles (20 alternated cycles of each material) at a constant temperature of 225 °C, using trimethylaluminium (TMA) and water (H_2O) as precursors for the Al_2O_3 deposition, and tetrakis dimethylamido-hafnium (TDMAH) and water (H_2O) for the HfO_2 deposition,

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resulting in an oxide thickness of about 9 nm [9]. After removal of the oxide from the back side, both wafer sides were metalized with Al–0.5% Cu and the front side patterned to get capacitors in the active areas and bonding pads on the field oxide. When subjected to CVS@-7V, successive BD events are registered (34 devices) as illustrated in the time censored (540 s) experiment shown in Fig. 1. The effect of the stress voltage on the time-to-BD distributions was also investigated in [10]. Some devices occasionally exhibit large jumps associated with catastrophic events but in general the jumps are small and countable. Devices exhibiting small jumps are exclusively considered in this work. The details for one typical sample path I–t are illustrated in Fig. 2. The definitions of the occurrence time (OT) (measured from the outset of degradation), interarrival time (IT), and step height (SH) are indicated in the inset. Notice the important change of slope that takes place around 100–150 s.

3. Data analysis and discussion

Fig. 3 shows the event plot (failure times in each device) corresponding to Fig. 1. The vertical dashed line indicates the dead time (t_0) during which the oxide degradation takes place without any failure occurrence. Within our approach, t_0 is used as global a fitting parameter. Importantly, as it was reported in Ref. [6], the time-to-first BD event is Weibull-distributed after screening the data in terms of the initial leakage current. Here, the screening method is not applied since failure times are not analyzed using order statistics [11]. As it can be seen from Fig. 3 there is an important accumulation of points in the time range 20–150 s. In this regard, the scatterplot in Fig. 4 reveals that there is a positive correlation between IT and OT which indicates that the BD events are not identically distributed in time as the degradation proceeds. This is further confirmed by analyzing the IT histogram (see Fig. 5). The plot shows that the ITs exhibit underdispersion with respect to the *memoryless* exponential probability distribution function so that an HPP can be ruled out for the investigated process [8]. Fig. 6 shows several fitting models (solid lines) for the OT frequency distribution (symbols): power, exponential and logarithmic laws. Although the logarithmic model provides the best fitting results (largest R^2 coefficient) for OT >100 s, we opted for the power-law model because it is a standard approach in failure analysis [12] which smoothly fits to the linear arrival rate observed for short OTs. The proposed expression for the intensity function is:

$$\lambda(t) = \left(\frac{t-t_0}{\theta_1}\right)^{\beta_1} - \left(\frac{t-t_0}{\theta_2}\right)^{\beta_2} \quad (1)$$

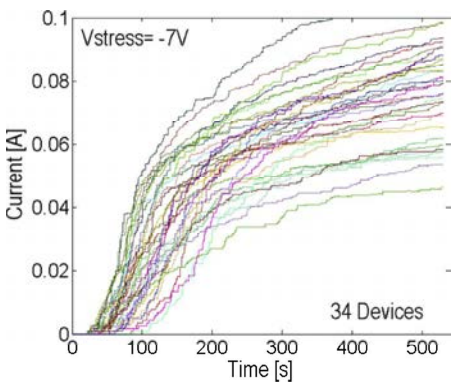

Fig. 1. Current–time characteristics corresponding to the 34 devices investigated in this work. The devices were stressed at −7 V during 540 s.

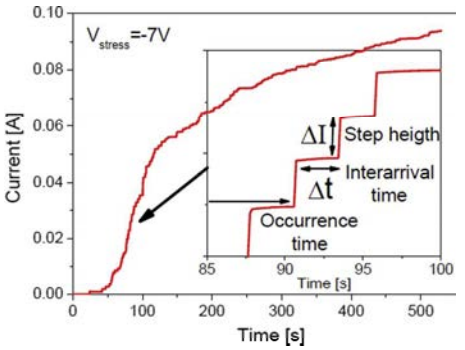

Fig. 2. Details of one sample path and definition of the magnitudes of interest: occurrence time (OT), interarrival time (IT) and step height (SH).

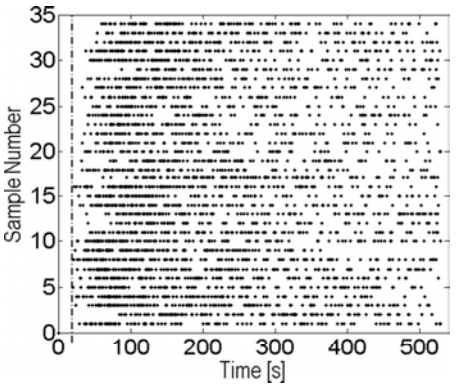

Fig. 3. Event plot for the sample paths shown in Fig. 1. The dashed line corresponds to the dead time during which no failure event is detected.

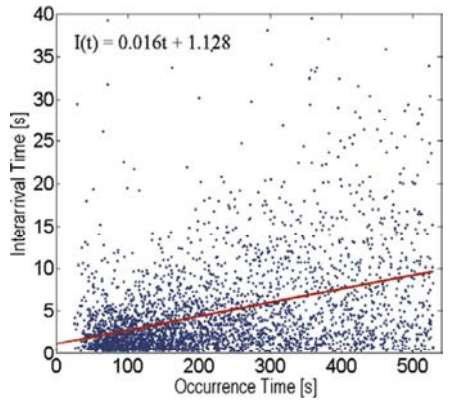

Fig. 4. Scatterplot for the interarrival time vs. occurrence time. The solid line is a line trend obtained by the least squares method.

which corresponds to a double power-law model with characteristic times θ_1 and θ_2, and exponents β_1 and β_2. $t_0 = 10$ s, $\theta_1 = 224.23$ s, $\beta_1 = -1.30$, $\theta_2 = 190.82$ s, and $\beta_2 = -1.41$ provide the best fitting results to our data. Notice that, taking into account the superposition principle of uncorrelated NHPPs, (1) was normalized to the

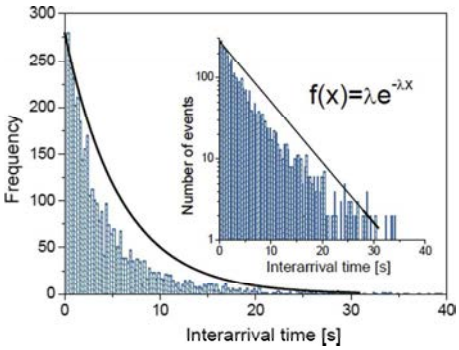

Fig. 5. Frequency plot for the interarrival times (bin size of 10 s). The inset shows the same plot in log-linear axis. The solid line corresponds to an exponential distribution with a constant parameter λ.

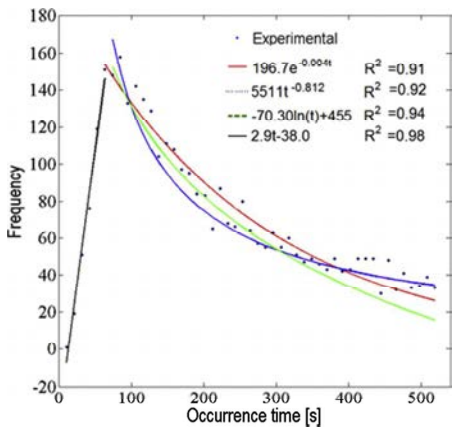

Fig. 6. Frequency plot for the occurrence times (symbols). The solid lines correspond to different fitting models.

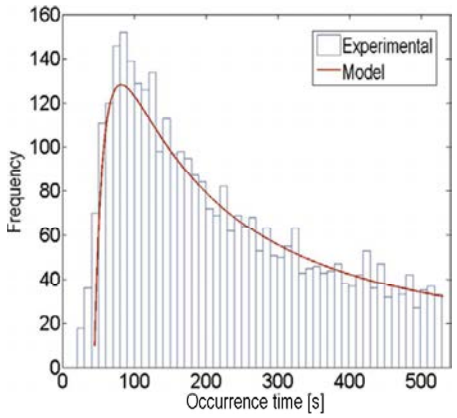

Fig. 7. Frequency plot for the occurrence times and global fitting model (bin size of 10 s). The solid line corresponds to the function $f(t) = 4.15 \times 10^5 (t-10)^{-1.3026} - 6.12 \times 10^5 (t-10)^{-1.4165}$.

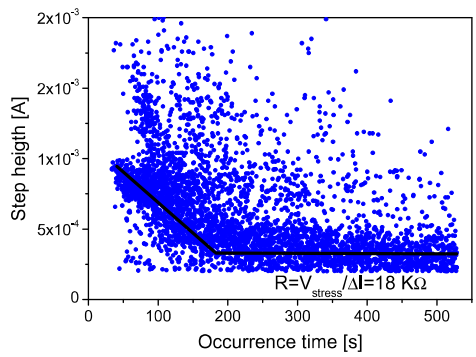

Fig. 8. Scatterplot of the step height SH as a function of occurrence time OT. The solid line is a guide to the eye.

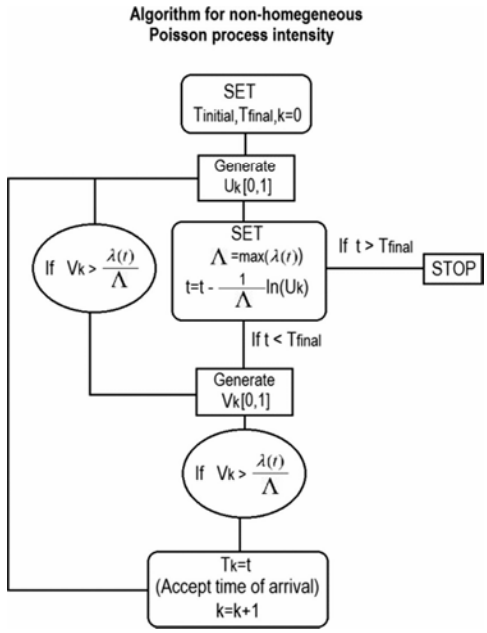

Fig. 9. Thinning algorithm used for calculating the arrival time of the failure events according to the NHPP given by Eq. (1).

number of processes ($N = 34$) and bin size (10 s) considered in Fig. 7. The model parameters were found using a nonlinear least squares method for the family of curves defined by Eq. (1) with the aid of the initial guesses reported in Fig. 6. The overall behavior described by Eq. (1) is the result of two effects: in the short time scale there is an apparent increment of the failure rate caused by the spread of the time-to-first BD, however, in the long run, a progressive decrease of the failure rate is clearly observed. This second effect can be ascribed to the reduction of the oxide voltage originated in the opening of multiple leakage current paths. In other words, as a consequence of the current increase, part of the applied voltage drops across the series resistance of the device. This can explain the reduction of the process intensity with the degradation time. As illustrated in Fig. 8, in the long run, the step height SH also levels

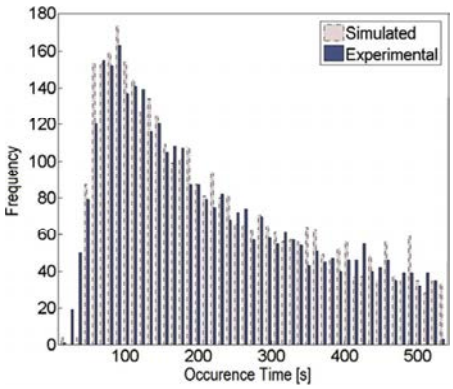

Fig. 10. Histogram for the experimental and simulation results using the thinning algorithm described in Fig. 9.

off around an equivalent resistance value of 18 kΩ per filament created.

Finally, in order to generate a sequence of arrival times consistent with the NHPP defined by Eq. (1), the so-called thinning method is considered [13]. The method is applicable for any given rate function $\lambda(t)$ and is based on controlled deletion of events of an HPP whose rate function dominates $\lambda(t)$. In particular, $\Lambda = max[\lambda(t)]$ can be used as the thinning function. The algorithm is schematically described in Fig. 9. U and V are uniform distributions in the range [0,1]. The distribution of the generated failure times (scaled to the number of devices and bin size) is illustrated in Fig. 10. Notice the good agreement between the experimental and simulated data.

4. Conclusions

The breakdown time statistics of successive failure events in ALD-grown Al_2O_3/HfO_2 nanolaminates was investigated. It was shown that the arrival rate of the failure events during a constant voltage stress is consistent with a nonhomogeneous Poisson process. The intensity function of this process is expressed as a combination of two individual power-law intensity functions. The model parameters were found taking into account the superposition principle of multiple uncorrelated processes. In order to demonstrate the adequacy of the proposed expression, simulated data obtained by the thinning method were compared to the experimental results.

Acknowledgements

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ARTICLE **MER15**

Electrical characterization of multiple leakage current paths in HfO_2/Al_2O_3-based nanolaminates

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Electrical characterization of multiple leakage current paths in HfO_2/Al_2O_3-based nanolaminates

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ABSTRACT

The generation of multiple leakage current paths in metal–insulator–semiconductor (MIS) structures with a HfO_2/Al_2O_3-based nanolaminate grown by the ALD technique as insulator material was investigated. The devices were stressed at selected constant voltages in order to achieve accurate values for the occurrence time of every single breakdown event in a time range spanning around 120 s. The final result of the degradation experiment is a current-time characteristic with well-defined current steps. It is shown that using an equivalent circuit model formed by an array of series and parallel resistances we are capable of replicating the current increase exhibited by the investigated structures. Taking into account the obtained results for the discrete failure events, the model is extrapolated to the quasi-continuous breakdown case, which provides an even simpler relationship for the leakage current evolution. In this connection, an approximate expression for the time required to reach a given current level is proposed.

1. Introduction

Thin oxide reliability analysis in metal–insulator–semiconductor (MIS) devices often involves the application of constant voltage stress (CVS) until the detection of a failure event. This is called Time-Dependent-Dielectric Breakdown (TDDB) test. In most of the cases, the test is stopped after the detection of the first breakdown (BD) event, which does not allow exploring the generation of successive failure events in the same device. In this work, the generation of multiple BD events in MIS structures with a HfO_2/Al_2O_3-based nanolaminate as insulator material is investigated using an extended TDDB test. The interest in this kind of nanolaminate for its use in MOS transistors stems from the possibility of achieving a gate stack that shares the properties of both Al_2O_3 (high conduction band offset from Si, $\phi \approx 2.8$–3.3 eV [1,2]) and HfO_2 (high permittivity oxide, $\kappa \approx 22$ [2]). Moreover, given the observed post-BD behavior, which will be discussed along the following Sections, nanolaminates of this kind could also be relevant for the fabrication of multilevel one-time programmable non-volatile memory devices (antifuse NVMs) [3]. It is shown in the present work that the application of CVS to our devices generates well-defined stepwise current–time (I–t) characteristics typical of a system with sequentially triggered parallel leakage current paths (see Fig. 1a and b). The resulting BD dynamics can be simulated assuming multifilamentary conduction. To demonstrate the validity of such approach an equivalent circuit model for the I–t curves consisting of an array of series and parallel resistances is proposed. It is worth pointing out that here, the attention will be exclusively focused on the current jumps associated with the generation of the filaments so that their corresponding failure times will be assumed known. Readers interested in a thorough analysis of the BD order statistics (successive BD statistics) in the HfO_2/Al_2O_3-based nanolaminates can refer to [4].

2. The devices

The devices investigated in this work are MIS capacitors with a 5-layer nanolaminated layer (Al_2O_3/HfO_2/Al_2O_3/HfO_2/Al_2O_3) deposited by ALD onto a p-type Si substrate (0.1–1.4 Ω cm). A field oxide of 400 nm was grown by thermal oxidation at 1100 °C and windows were opened for the Al_2O_3/HfO_2 stack by photolithography and wet etching. Before deposition, the samples were first cleaned for 10 min with H_2O_2/H_2SO_4 and subsequently for 10 s with HF. The ALD process was performed in 100 cycles (20 alternated cycles of each material) at a constant temperature of 225 °C, using trimethylaluminium (TMA) and water (H_2O) as precursors for the Al_2O_3 deposition, and tetrakis dimethylamido-hafnium (TDMAH) and water (H_2O) for the HfO_2 deposition, resulting in an oxide thickness of 9 nm. After removal of the oxide from the back side, both wafer sides were metalized with Al–0.5% Cu and the front side patterned to get capacitors in the active areas and bonding pads on the field oxide. A complete study on the fabricated devices from a material point of view can be found in [5]. In what follows, two typical I–t characteristics will be examined. They correspond to devices with areas $9.6 \cdot 10^{-3}$ cm^{-2} (CVS@—6.75 V) and $2.3 \cdot 10^{-3}$ cm^{-2}

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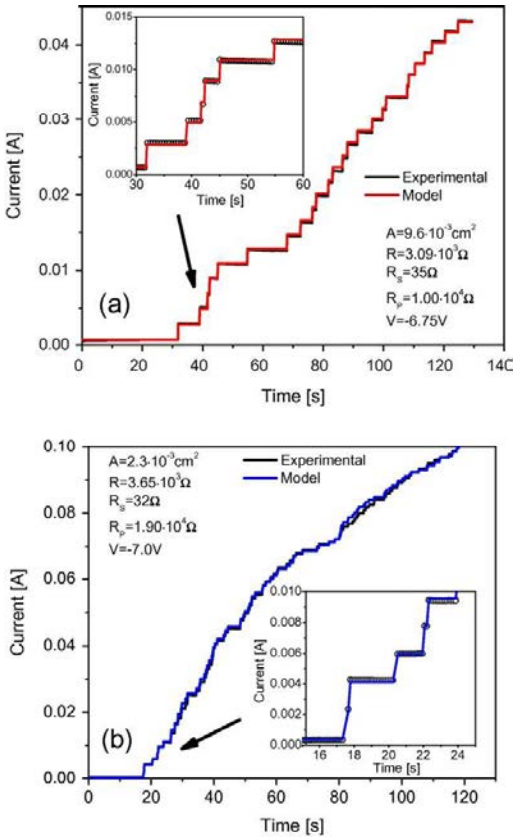

Fig. 1. Typical current–time characteristics and model results. (a) Device area $A = 9.6 \cdot 10^{-3}$ cm^{-2} and stress voltage $V = -6.75$ V and (b) device area $A = 2.3 \cdot 10^{-3}$ cm^{-2} and stress voltage $V = -7.0$ V.

(CVS@−7 V). The BD dynamics are illustrated in Fig. 1a and b, respectively. The time range investigated is 120 s because for longer times the BD times exhibit some correlation effects.

3. Model results and discussion

As mentioned in Section 1, the broken down devices are modeled using an array of series and parallel resistances. According to the schematic shown in Fig. 2, the current–voltage (I–V) characteristic of the nanolaminates can be expressed as:

$$I = \left[R_S + \left(\frac{n}{R} + \frac{1}{R_P} \right)^{-1} \right]^{-1} V \tag{1}$$

where R_S and R_P are the series and parallel resistances, respectively. R is the resistance associated with the appearance of the leakage current path $n \geq 1$. R_P represents the leakage current flowing through the device before the first BD event. As shown in Fig. 3, Eq. (1) can reproduce the evolution of the current steps ΔI as the degradation proceeds. These steps determine the overall shape of the I–t characteristics since the filaments, for the timespan investigated, are generated at a constant rate (see Fig. 4). According to this observation, we can express the number of filaments n at a time t as:

$$n(t) \approx \alpha (t - t_0) \tag{2}$$

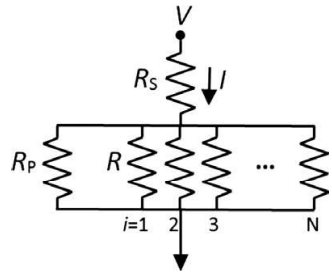

Fig. 2. Equivalent circuit model with sequentially formed BD paths. R_S and R_P are series and parallel resistances, respectively. R is the resistance of a single filament.

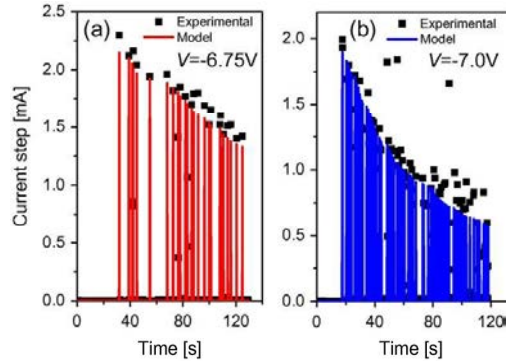

Fig. 3. Current steps for the I–t curves shown in (a) Fig. 1a and (b) Fig. 1b. Symbols and solid lines correspond to experimental data and simulations, respectively.

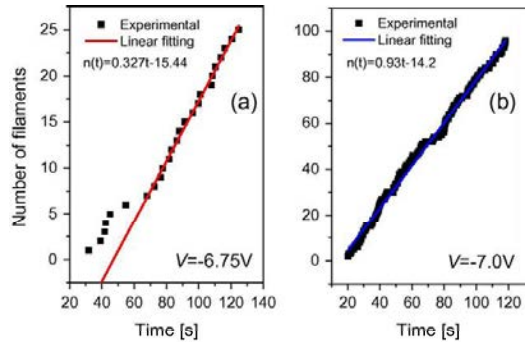

Fig. 4. Evolution of the number of filaments as a function of time: (a) data from Fig. 1a and (b) data from Fig. 1b.

where α is the arrival rate of the failure events and t_0 the dead time in which no event is detected. As expected, experimental data reveal that α increases with the area of the device (Fig. 5a) and with the magnitude of the stress voltage (Fig. 5b). Neglecting R_P, the model parameters R_S and R can be obtained from Eq. (1) as:

$$\frac{V}{I_n} \approx R_S + \frac{R}{n} \tag{3}$$

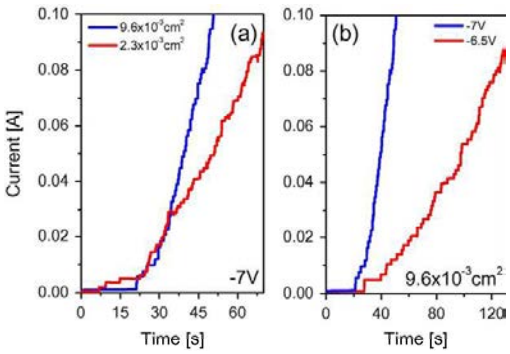

Fig. 5. (a) Evolution of the current for different device area (same stress voltage) and (b) evolution of the current for different applied voltages (same device area).

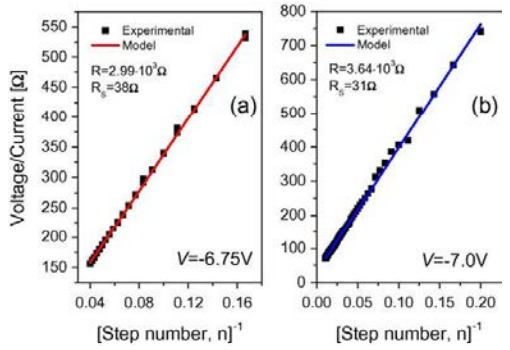

Fig. 6. Evolution of the device resistance as a function of time: (a) data from Fig. 1a and (b) data from Fig. 1b.

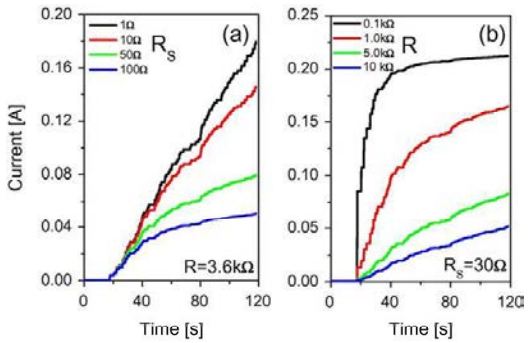

Fig. 7. Effect of the model parameters (a) R_S and (b) R on the simulated curves using Eq. (1).

where I_n is the current measured immediately after the occurrence of the nth event. Eq. (3) is represented in Fig. 6. While R is in the range of several kΩ, R_S is two orders of magnitude lower. Fig. 7 illustrates how these two model parameters affect the simulated I–t characteristics: R determines the initial slope of the curves (Fig. 7b) and R_S the long-run behavior (Fig. 7a).

Taking into account the BD dynamics determined by Eqs. (1) and (2), it is possible to extrapolate the device behavior to the continuous

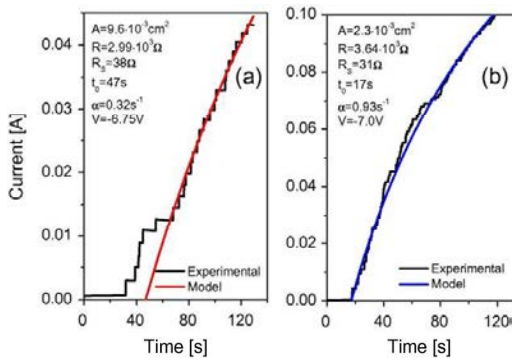

Fig. 8. Continuous model approximation (Eq. (4)): (a) data from Fig. 1a and (b) data from Fig. 1b.

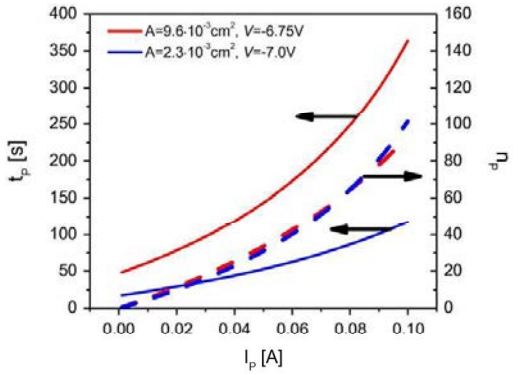

Fig. 9. Programming time t_P and number of filaments n_P as a function of the target current level I_P. Model parameters in Fig. 8.

degradation case, *i.e.* smaller jumps at a proportionally larger failure rate. As the result of this exercise, we can rewrite (1) as:

$$I(t) \approx \left[R_S + \alpha^{-1} R (t - t_0)^{-1}\right]^{-1} V \tag{4}$$

which is represented by the solid lines in Fig. 8a and b. Now, Eq. (4) can be used to assess the programming time t_P necessary to reach a given current level I_P:

$$t_P(I_P) \approx \alpha^{-1} R I_P (V - R_S I_P)^{-1} + t_0 \tag{5}$$

which, equivalently, corresponds to a number of steps:

$$n_P(t_P) \approx R I_P (V - R_S I_P)^{-1} \tag{6}$$

Expressions (5) and (6) are plotted in Fig. 9 for the two samples investigated. Notice that the number of steps is almost identical in both cases, which gives further support to the proposed model for the leakage current evolution.

One important feature of the model described above, which is surprising at first glance, is that the voltage drop across the array of parallel resistances V–IR_S is not the variable governing the generation of failure events. This is clearly illustrated in Fig. 10, in which the remarkable potential drop occurring in this part of the system is monitored as a function of the stress time. Since the failure arrival rate is almost constant (see Fig. 4), the oxide stack cannot be exclusively identified with the

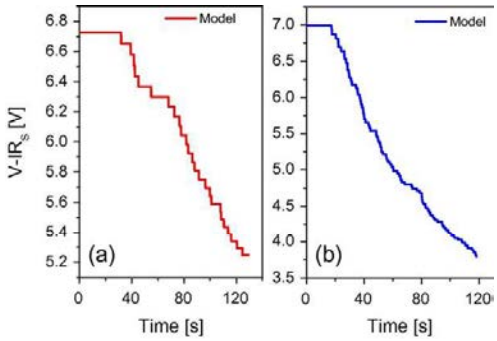

Fig. 10. Evolution of the potential drop in the array of parallel resistances as a function of time: (a) data from Fig. 1a and (b) data from Fig. 1b.

array of parallel resistances. On the contrary, it is likely that the whole circuit depicted in Fig. 2 describes the filamentation process of the insulator. It is worth mentioning that in a previous work [4], in order to explain the anomalous statistics exhibited by the time-to-first BD event, the presence of a 1.5–2.0 nm SiO_x interfacial layer had to be assumed. It is not clear yet from the available data whether this layer actually breaks down in a multifilamentary pattern and the Al_2O_3/HfO_2 nanolaminate performs as the series resistance. This issue is still under investigation but preliminary results indicate that the observation of current jumps similar to those analyzed here is mainly associated with the presence of the Al_2O_3 layer. The presence of a SiO_x interface layer cannot be ruled out in this case. However, best results in terms of current jumps are observed in the nanolaminated system.

4. Conclusions

The generation of multiple breakdown events in Al_2O_3/HfO_2-based nanolaminates in MIS devices was investigated. A simple circuit model consisting in an array of parallel and series resistances to account for the current–time characteristic of these devices was proposed. The model can be used to determine the stress time required to set the device to a given current level. This is of primarily importance for the programming operation of multilevel non-volatile memory devices based on the creation of multiple uncorrelated breakdown paths.

Acknowledgements

This work was funded in part by Projects PCIN2013-076, TEC2012-32305, TEC2011-27292-C02-02 of the Spanish Ministerio de Economía y Competitividad, the ENIAC Joint Undertaking and the DURSI of the Generalitat de Catalunya (2014SGR384). Project TEC2012-32305 was co-funded by the EU under the FEDER program.

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ARTICLE **JVS17**

Function-fit model for the rate of conducting filament generation in constant voltage-stressed multilayer oxide stacks

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Function-fit model for the rate of conducting filament generation in constant voltage-stressed multilayer oxide stacks

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A simple function-fit model is proposed for the rate of conducting filament generation in Al_2O_3/HfO_2-based multilayer stacks subjected to a constant voltage stress. During degradation, the devices exhibit stepwise current–time (I-t) characteristics that can be straightforwardly linked to the triggering of multiple breakdown events. The stochastic nature of this stepwise behavior is phenomenologically modeled by means of a nonhomogeneous Poisson process for the arrival rate of the individual failure events. In this work, it is shown that a power-law model for the failure rate in combination with an equivalent circuit representation of the device under stress accounts for the evolution of the I-t curve, providing a first-order estimation of the stress time required to reach a targeted leakage current level. The roles played by the device area and stress voltage on the breakdown dynamics are also investigated. © *2016 American Vacuum Society*.
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I. INTRODUCTION

The generation rate of multiple failure events in atomic-layer-deposited Al_2O_3/HfO_2 nanolaminates subjected to constant electrical stress is investigated in this work by means of a phenomenological approach. The central idea behind the use of a material combination such as this is to achieve a gate stack that shares the properties of both the Al_2O_3 (high conduction band offset from Si, $\phi = 2.8$–3.3 eV)[1,2] and the HfO_2 (high permittivity oxide, $k = 22$).[2] This technique has been explored by Wei *et al.*[3] It has been found that the stepwise behavior exhibited by the current–time (I-t) characteristics of this high-permittivity (high-k) nanolaminate is a direct consequence of the successive opening of localized leakage current pathways across the dielectric film. Further, the breakdown (BD) events have been found to arise from the progressive accumulation of defects within the bulk oxide and the formation of filamentary paths for electron transport. The connection between the generation of defects and the magnitude of the leakage current has also been thoroughly investigated.[4–6] For our devices, the triggering of successive BD events was analyzed in the past using order statistics[7] and time-dependent arrival processes.[8] In recent works,[7,8] the analysis was limited to a few events per device (up to ten) and the role played by the initial current magnitude on the current evolution was emphasized; in addition, the arrival rate of failure events was assumed to be a combination of time-dependent Poisson-type arrival processes with different intensities depending on the phase of degradation (initial or long-run). In those papers, however, modeling of the I-t curve was not considered. Modeling the I-t curve requires not only a model for the generation of events but also a circuital representation for the leakage current of the device. In addition, the roles played by the device area and stress voltage were totally disregarded in those previous studies, which is a severe limitation for understanding of the breakdown dynamics. Although a detailed explanation of the physics behind the degradation process is currently unavailable, new experimental and simulation results using a phenomenological approach are presented. This study provides a more comprehensive picture of the generation of conducting filaments (CFs) randomly distributed over the device area and their effect on the leakage current magnitude. This issue is also relevant for downscaled devices.[9] It is worth mentioning that the observation of similar successive BD events is not limited to high-k materials, but it has been reported to occur in ultrathin SiO_2 layers,[10] and in more complex structures as well.[11] Interestingly, the controlled generation of multifilamentary conducting structures in dielectric films could pave the way for the fabrication of multilevel one-time programmable nonvolatile memory devices.[12] Multilevel conduction has also been observed in nonvolatile memory devices such as resistive random-access memory devices.[13]

II. DEVICES AND EXPERIMENTAL SETUP

The devices investigated in this work were metal-insulator-semiconductor capacitors with a five-layer nanolaminated insulator ($Al_2O_3/HfO_2/Al_2O_3/HfO_2/Al_2O_3$) grown by atomic layer deposition onto a p-type Si substrate (0.1–1.4 Ω cm).[14] A field oxide of 400 nm was grown by thermal oxidation at 1100 °C and windows were opened for the Al_2O_3/HfO_2 stack by photolithography and wet etching. Before deposition, the samples were initially cleaned for 10 min with H_2O_2/H_2SO_4 and subsequently for 10 s with HF.

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Atomic layer deposition was performed in 100 cycles (20 alternated cycles for each material) at a constant temperature of 225 °C, using trimethylaluminium and H_2O as precursors for the Al_2O_3 deposition and tetrakis dimethylamido-hafnium and H_2O for the HfO_2 deposition, resulting in an oxide thickness of about 9 nm.[15] After removal of the oxide from the back side, both wafer sides were metallized with Al-0.5% Cu and the front side was patterned to produce capacitors in the active areas and bonding pads on the field oxide. The devices investigated possessed areas varying as 9.6×10^{-3}, 2.3×10^{-3}, 3.2×10^{-4}, 1.4×10^{-4}, and 6.4×10^{-5} cm^2. All of the measurements were carried out using a HP-4155B semiconductor parameter analyzer, and the fresh devices were subjected to constant voltage stress with the substrate terminal grounded. For practical reasons, the range of stress voltages that could be evaluated was very limited, and included the values −6.75, −7.0, and −7.25 V. It was found that at voltages higher than this range, the degradation process was too fast, while at lower voltages the rate of failure site generation was extremely low. For these applied voltages, the Si electrode was under accumulation conditions.

III. EXPERIMENTAL RESULTS AND PROPOSED MODEL

Typical *I-t* characteristics exhibiting multiple BD steps are shown in Fig. 1, wherein the devices were stressed with −7.0 V applied to the top electrode. The initial current magnitude is approximately 10 μA for the 9.6×10^{-3} cm^2 devices with an initial current jump of about 1 mA in the first 50 s (see the Fig. 1 inset). After this initial step, several BD events can be observed until a total leakage current of about 80–100 mA is reached. As can be seen, a large number of successive BDs are registered in a time span of 540 s. The step height decreases as the degradation proceeds, which indicates that the history of the device is relevant for the description of the current evolutionary behavior. It is worth noting that the initial leakage current magnitude strongly affects the initial time-to-breakdown: the highest currents are associated with the shortest BD times. This issue was extensively investigated[7] and was attributed to the presence of more or less defective devices. Dispersion of the oxide thickness value cannot be ruled out. A remarkable aspect in Fig. 1 is the change of the trend in the *I-t* curves that takes place around 100–200 s in all of the devices considered in this study. The modification of the curve slopes indicates that some fundamental change in the degradation process occurs during this intermediate phase of degradation. To illustrate this change of behavior in more detail, Fig. 2 shows the number of registered BD events and the corresponding device resistance reduction as a function of time for a particular device. Two phases can be easily recognized: In the first phase, the resistance of the device drops sharply by about 2 orders of magnitude, whereas in the second phase, the resistance levels off at around 10^2 Ω. Both phases can also be linked to a significant change in the number of registered events. Further, no saturation effect is observed in this latter phase. This remarkable difference between these degradation phases might be owing to the exhaustion of a particular kind of filament rather than solely to a series resistance effect, where the latter is expected to be a continuous effect. As is shown below, this modification of the failure rate is simplified by assuming a nonlinear failure generation model for the entire degradation process. To shed more light upon the roles played by the device area and the stress voltage, Fig. 3 plots the *I-t* measurements for devices with identical areas and different stress voltages [Fig. 3(a)] and for devices with different areas and identical stress voltages [Fig. 3(b)]. These measurements reveal that the arrival rate of the failure events increases with the device area and also with the magnitude of the stress voltage. The overall behavior is consistent with the area scaling property of Poisson statistics and with the voltage acceleration factor associated with the electrical degradation of metal-insulator-semiconductor devices.[16] Figures 3(c) and 3(d) show the correlation between the time-to-first filament formation and the initial current density for devices with different areas stressed

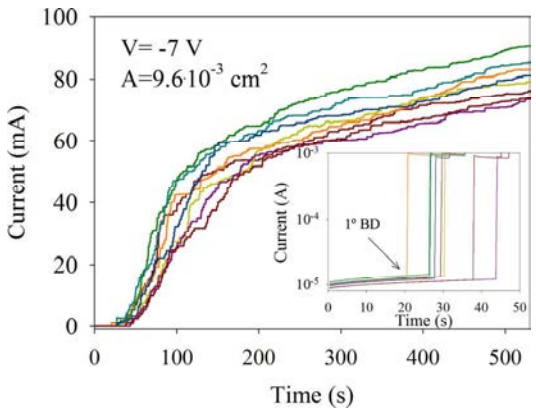

FIG. 1. (Color online) Current–time characteristics corresponding to several devices. The inset illustrates the initial breakdown event where it is possible to distinguish the variation of the initial leakage current magnitude. The time-to-first breakdown increases for smaller leakage currents.

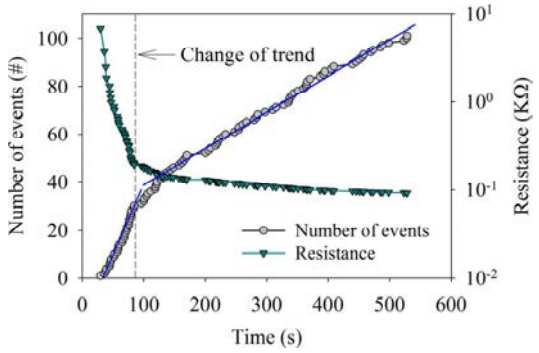

FIG. 2. (Color online) Number of events (circles) and resistance values (triangles) registered as a function of time. The dashed line points out the change of trend. The solid lines are guides to the eye.

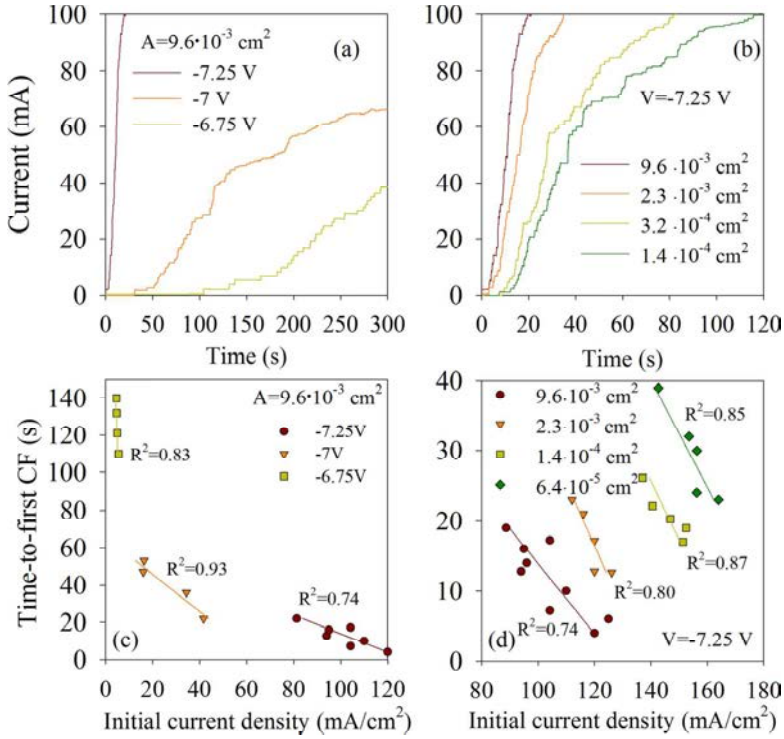

FIG. 3. (Color online) Evolution of the current for (a) different applied voltages and (b) different device areas. Scatterplot for the time-to-first filament formation vs the initial current density for (c) different stress voltages and (d) for different device areas. The solid lines are linear fittings to the experimental data. R^2 is the linear correlation coefficient.

at different voltages, respectively, where R^2 is the linear correlation coefficient. These results quantitatively confirm that the onset of the filamentation process is a function of the initial leakage current condition of the device.

To simulate the results discussed above, a simple phenomenological model for the arrival rate of failure events is presented here. As illustrated in Fig. 4(a), the number of generated filaments $n(t)$ can be fitted using a power-law model of the form

$$n(t) = \alpha t^{\beta} + \gamma, \tag{1}$$

where α, β, and γ are fitting constants, wherein γ deals with the dispersion of the initial leakage current magnitude. α and β depend on the device area and stress voltage, respectively. The model parameters for the average experimental curve shown in Fig. 4(a) are included in its inset. From Eq. (1), the failure arrival rate $\lambda(t)$ can be found as

$$\lambda(t) = \frac{dn(t)}{dt} = \alpha\beta t^{\beta-1}. \tag{2}$$

Notice that when $\beta = 1$, this model reduces to a homogeneous Poisson process.[17] Figure 4(b) shows the algorithm used to add the stochastic dimension to the above expression. The proposed algorithm is based on a time-dependent Poisson arrival process characterized by a deterministic function $\lambda(t)$ that describes how the intensity of the process changes over time. First, a BD time is generated in a finite time interval $[T_{initial}, T_{final}]$. Second, a random number in the range [0,1] is generated, and a new BD time is generated in a time length inversely proportional to the failure rate of the deterministic process. This is repeated several times until the process ends. The experimental and model curves are compared in Fig. 5(a), where the solid line corresponds to the average curve calculated from 100 simulations and the dashed lines correspond to a 20% variation of the central curve. For illustrative purposes, Fig. 5(b) plots a sample curve generated by the function-fit model in Eq. (2) in combination with the equivalent circuit proposed in a previous work.[18] The electrical model basically comprises an array of series and parallel resistances [see the inset in Fig. 5(b)]. Each parallel resistance R represents the generation of a new CF according to the proposed power-law model, where R_S is a common series resistance and R_P the initial resistance of the device. Because of the nonlinearity introduced by Eq. (2), the model is able to deal with the reduction of the failure rate already discussed in connection with Fig. 2. The

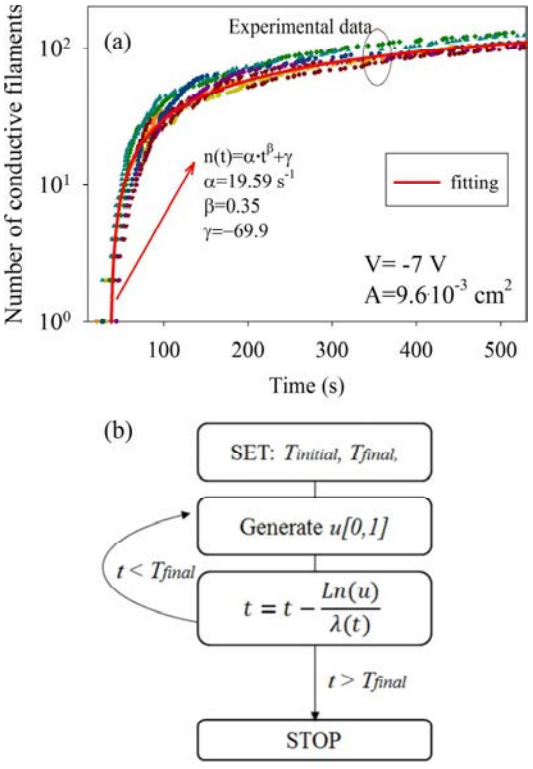

FIG. 4. (Color online) (a) Number of conducting filaments as a function of time. The solid line indicates the fitting to the experimental data. (b) Algorithm used for the simulation of the failure event arrival times.

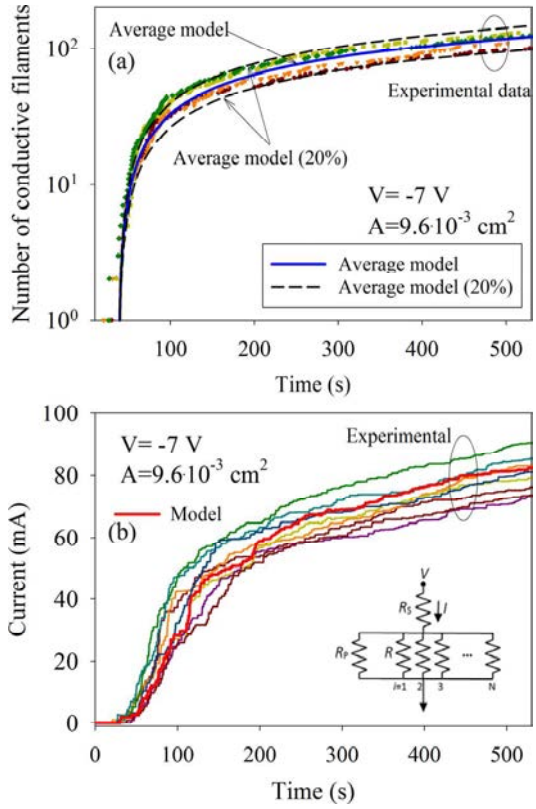

FIG. 5. (Color online) (a) Comparison between simulations and experimental results using the data and the algorithm shown in Fig. 4. (b) Current–time characteristics. The red solid line was calculated from the generated events and the circuit representation of the device.

similarity between the generated stepwise *I-t* curve and the experimental ones can be easily seen.

IV. ADDITIONAL MODEL RESULTS AND DISCUSSION

Herein, additional experimental and simulation results are presented in view of the model proposed above. In Fig. 6, the filamentation process as a function of the device area [Figs. 6(a) and 6(b)] and stress voltage [Figs. 6(c) and 6(d)] are explored in more detail. In both cases, as an initial step the number of generated filaments $n(t)$ is fitted to the experimental data using Eq. (1) [Figs. 6(a) and 6(c)], after which the failure arrival rate $\lambda(t)$ is calculated using Eq. (2). The model curves are then simulated using the algorithm described in Fig. 4(b) and compared to the original data [Figs. 6(b) and 6(d)]. Figure 6(a) shows the dependence of the model parameters α, β, and γ on the device area, where power-law dependences are obtained for the three parameters under consideration. A similar dependence with the stress voltage seems to hold, but the results are not conclusive owing to the limited range of voltages. In addition, as shown in Fig. 7(a), it is possible to establish an empirical relationship for the number of generated filaments as a function of the current that flows through the device such that

$$n(I) = aI^b, \tag{3}$$

where a and b are fitting constants. From the power-law model $n(t)$ described in Fig. 4(a) and Eq. (3), the stress time required to reach a certain current magnitude can be obtained. Figure 7(b) shows the number of CFs as a function of the current $[n(I)]$ in a linear scale and the stress time required to reach a given current $[t(I)]$. Notice that whereas $n(I)$ is almost linear ($b = 1.16$), $t(I)$ exhibits an exponential trend which stresses the idea that the failure rate reduces in the long run owing to a possible increase in the series resistance effect. However, as explained in Sec. III, this series resistance effect is not constant and seems to depend on the particular stage of degradation. The connection with the exhaustion of particular kinds of filaments during degradation is still under investigation. As described in a recent work,[18] a constant value of R_S could lead to a significant

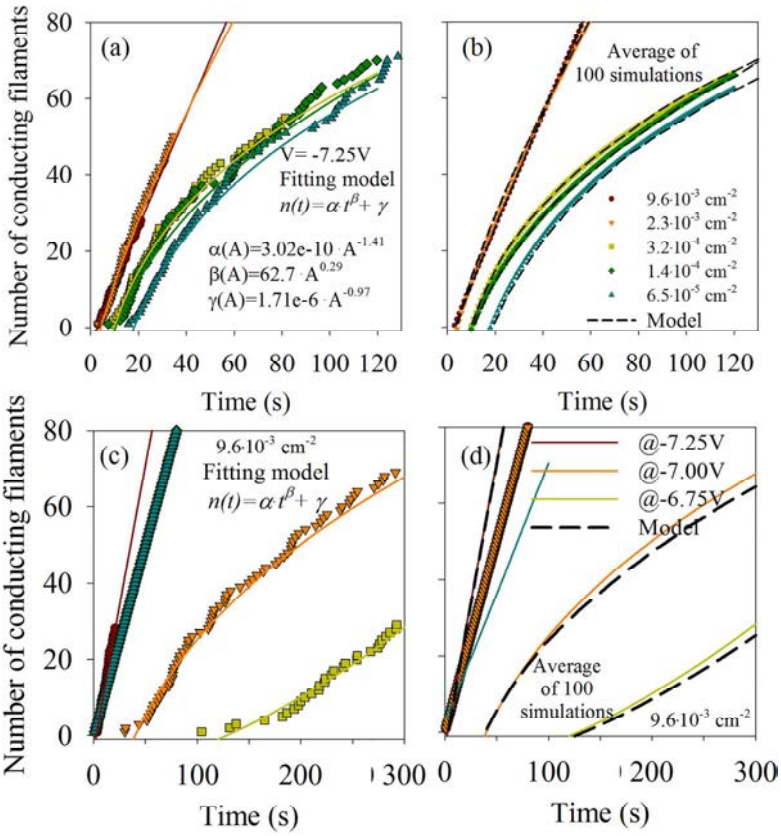

FIG. 6. (Color online) Conducting filaments generation as a function of device area (a) experimental data (symbols) with the fitting results (solid lines), and the (b) fitting of the experimental results (solid lines) from (a) and their average simulation model (dashed line). The conducting filament generation as a function of the stress voltage (c) experimental data (symbols) with the fitting results (solid lines) and the (d) fitting of experimental results (solid lines) from (c) and their average simulation model (dashed line).

reduction of the effective potential drop responsible for the generation of new CFs, which is incompatible with the experimental observations. If properly calibrated, Eq. (3) can be used for assessing the writing time of multilevel one-time programmable memory devices based on multifilamentary conduction.

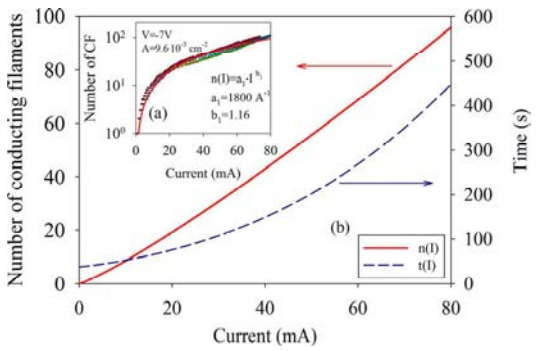

FIG. 7. (Color online) (a) Model parameters for the number of conducting filaments vs current magnitude. (b) Programming time and corresponding number of conducting filaments as a function of the targeted current.

V. CONCLUSIONS

In this work, the generation rate of multiple breakdown events in Al_2O_3/HfO_2 nanolaminates was investigated, and a deterministic function-fit model for the arrival rate of conducting filaments was proposed. The stochastic dimension of the model was obtained by means of an iterative algorithm based on a nonhomogeneous Poisson process for the arrival rate of the individual failure events. This information was introduced into a circuital representation of the device and the current was calculated. The experimental data confirmed that the arrival rate of the failure events depends on the device area and stress voltage, though the data are strongly affected by the initial leakage current. This information could be incorporated into the model parameters as well. Finally, it is worth noting that precise control of the number of failure sites can open the path for these investigated structures to be used in multilevel nonvolatile memory devices.

ACKNOWLEDGMENTS

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